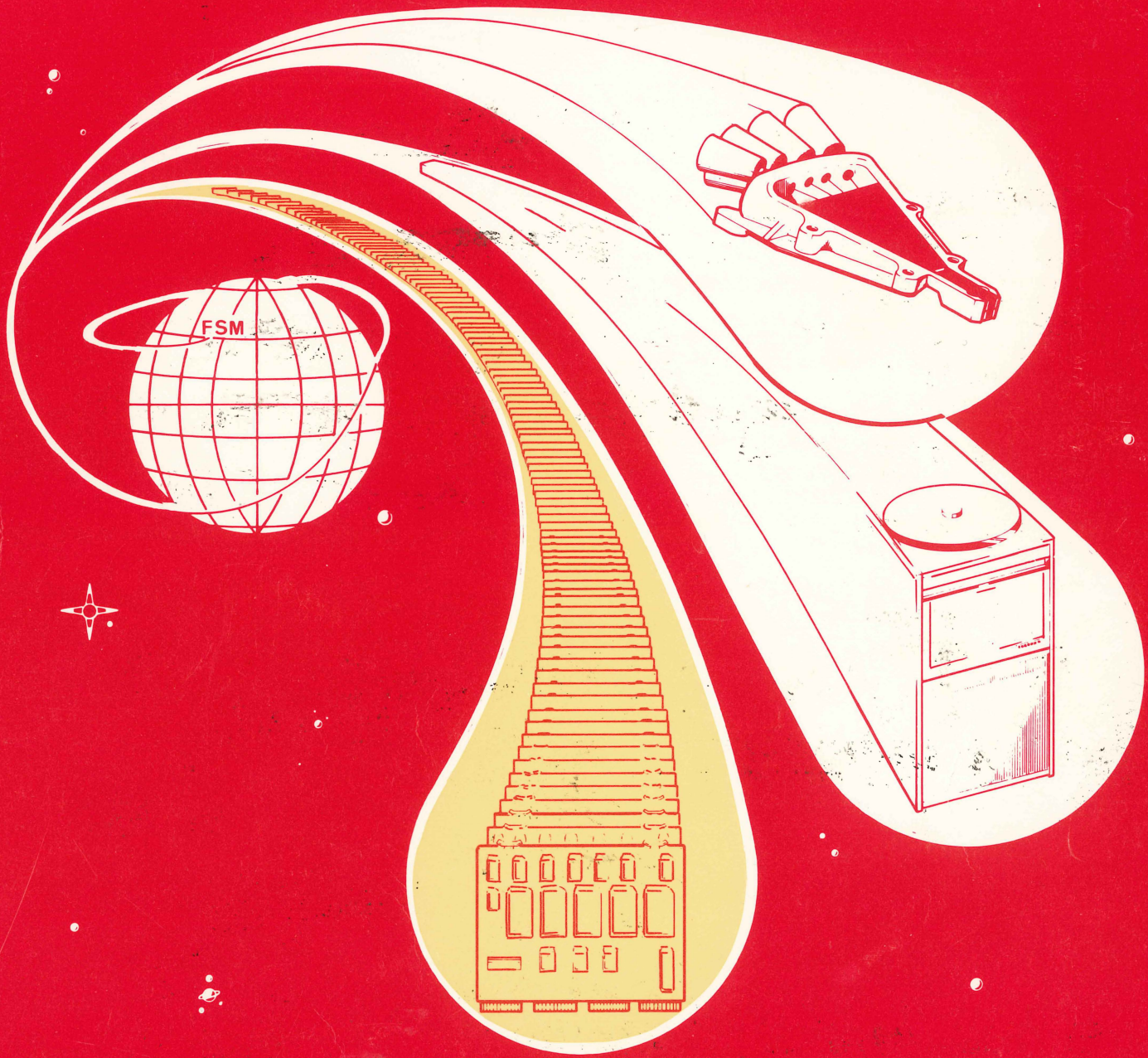
FIELD SERVICE LOGISTICS



REPAIR PROCESS

digital

SC780/B1 SC780/B3

(RM03/RM05/RM80 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

SC 751

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Part Number: SKLSC78B1

Edit Date: 28-Dec-83
Revision : D

Qty.	Part Number	Description
1	SC7851001	SC780/B1 SC780/B3 Technical manual
1	VD9951001	VAX driver installation and user's guide
1	VX9951001	VAX diagnostic instruction manual

Section 1
INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC780/B Disk Controller. In addition, this manual provides diagnostic and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC780/B Disk Controller is a one-board controller which is a component of the V-MASTER/780. The V-MASTER/780 is a unique new approach for interfacing mass storage peripherals to Digital Equipment Corporation's VAX-11/780 computer. It consists of two SBI interface boards and up to two SC780 disk or TC780 tape controllers in a compact 4-slot card cage which mounts directly in the VAX-11/780 CPU cabinet. In conjunction with the V-MASTER, the SC780 controller serves as an interface between the computer and up to four large disk drives with Storage Module Drive (SMD) interfaces. The SC780/B controller emulates the RH780 with attached DEC RM03, RM05 and/or RM80 Massbus disk subsystems. The Emulex controller is capable of operating with disk drives having different characteristics from those used in the DEC disk subsystems. The SC780/B controllers provide the capability of operating with a mixture of disks having storage capacity of 80 to 600 megabytes.

1.2.2 Controller Models

The SC780/B Controller is available with either /B1 or /B3 firmware. The difference between the two models lies in their support of the 2351A Fujitsu Disk Drive. The /B1 firmware supports a 44 sector configuration of the 2351A. The /B3 firmware supports a 48 sector configuration of the 2351A, allowing use of an additional 40 Mb of capacity. The 2351A Fujitsu must be hard sectored according to specification in Appendix A. See paragraph 3.2.6 for more information.

1.3 FEATURES

1.3.1 The V-MASTER/780

The SC780/B is designed to interface to the VAX-11/780 through the V-MASTER/780. The V-MASTER/780 consists of a Bus Interface PCBA and a Bus Translator PCBA. Those two boards occupy two slots in a four-slot card cage which is in turn mounted directly in the VAX-11/780 CPU cabinet. The two additional slots may each contain

a SC780 disk or TC780 tape controller. This architecture allows Emulex to install two SC780s in the same space that a single DEC RH780 occupies.

1.3.2 Microprocessor Design

The SC780/B design incorporates a unique 16-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.3 Packaging

The SC780/B is constructed on a single extended hex-size multi-layer PC board. The SC780/B plugs into the V-MASTER which is in turn mounted in the VAX-11/780 CPU cabinet. The V-MASTER/780 consists of a 4-slot card cage which mounts in the VAX-11/780 cabinet or an expansion cabinet. It also contains the Bus Interface Board and the Bus Translator Board and has room for an additional controller board. Each controller has an associated cable paddle board which plugs into the back of the card cage.

1.3.4 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the Fault LED ON and the controller cannot be addressed from the CPU.

1.3.5 Buffering

The controller contains a 1K x 16 high-speed RAM buffer used to store the MBA and map registers of the controller, the drive registers for eight drives, and one sector of data buffering.

1.3.6 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the error pattern and then passes this information back to the VAX-11/780 which actually performs the correction of the erroneous data. A 16-bit CRC is employed with the header of every sector.

1.3.7 Option and Configuration Switches

Three eight-pole DIP switches are used to configure the controller for various disk sizes, certain firmware options, MBA number and arbitration level. It is possible to select one of 32 possible combinations of disk characteristics for the four drives which can be handled by the controller, including mixtures of disk sizes and drive type codes.

1.3.8 Get Characteristics Capability

Since the SC780/B series of controllers can handle a number of different drive sizes, a capability has been provided to read out the maximum cylinder, maximum track, and maximum sector address, as well as the selected drive type code. This allows self configuring software to handle different drive configurations and sizes on the same controller.

1.3.9 Dual Port Capability

The controller can operate with disk drives having dual port capability which allows a second controller to have access to the drive on a priority basis.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Functionality

The SC780/B1 is functionally compatible with the DEC RH780 Massbus Adapter with one or more RM type disk drives attached, except that the controller does not execute the diagnostic mode of the RH780 or the maintenance mode of the RM drive. The absence of the diagnostic mode prevents running the complete RH780 diagnostic program.

1.4.2 Media Compatibility

The SC780/B1 is media compatible with the DEC RM02/RM03 packs when using a CDC 9762 drive or equivalent and with the DEC RM05 when using a CDC 9766 drive or equivalent. There is no need for media compatibility with the RM80 since it is a fixed-media drive, but the format is the same as used by the DEC RM80.

1.4.3 Diagnostics

The controller executes the following standard DEC RM03, RM05 and RM80 diagnostics:

EVRAA	VAX RP/RK/RM/RX/TU58 Reliability
EVRAC	Disk Formatter
EVRDA	RM03/5 RM80 Diskless Diagnostic

EVRDB	RM03/5 Functional Diagnostic
EVRGA	RM80 Formatter
EVRGB	RM80 Functional Diagnostic

1.4.4 Operating Systems

When emulating standard size RM03, RM05 or RM80 drives, the controller is compatible with the VAX/VMS operating system. Non-standard size drives can be used by appropriate patching to the disk driver and booting facility.

Table 1-1

GENERAL SPECIFICATIONS

Functional	
Emulation	DEC RM03, RM05 and RM80
Media Compatability	DEC RM03 and RM05 when using appropriate disk drives.
Drive Interface	SMD
Drive Ports	4
Error Control	32-bit ECC for data and 16-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	512 bytes
Sectors/Track	32
Tracks/Cylinder	Selectable for each drive.
Cylinders/Drive	Selectable for each drive.
Drive Type Code	Selectable for each drive.
Computer Interface	Controller: VMI (VAX-11/780) V-MASTER/780: SBI
Nexus Address	TR4-TR11 (see Appendix E for hex equivalents)
Interrupt Priority	4, 5, 6 or 7
Data Buffering	1 full sector
Data Transfer	64-bit DMA via SBI
Self-Test	Extensive internal self-test on powering up.
Indicators	Activity and Fault LEDs

Table 1-1 (cont'd)

Design	High-speed bipolar microprocessor using 2901 bit-slice components.
Physical	
Packaging	Controller: one extended hex size V-MASTER/780: two extended hex, plus one or two controllers.
Mounting	V-MASTER/780 Chassis.
Disk Connection	Paddle board on rear of backplane has connectors for A cable and four B cables.
Electrical	
SBI Interface	DEC approved line drivers and receivers.
Drive Interfaces	Differential line drivers and receivers. A cable accumulative length to 100 feet. B cable length to 50 feet.
Power	+5 v, 25 A with one 4-port controller. +5 v, 36 A with two 4-port controllers. -5.2 v, 1 A

2.1 ORGANIZATION

A block diagram showing the major functional elements of the V-MASTER is shown in Figure 2-1. The block diagram shows the relationship of the Bus Translator and Interface boards to the SC780 controller. Figure 2-2 is a detailed block diagram of the SC780 Controller itself.

2.1.1 V-MASTER/780

The Bus Interface board (SU7810401) provides the conventional interface to the Synchronous Backplane Interconnect (SBI) of the VAX-11/780. It provides bus transceivers, parity generation and checking, address tag and I.D. decoding, sequence state logic, interface and read data timeouts, and SBI fault detection.

The Bus Translator board (SU7810402) provides a translation between the SBI type output of the Bus Interface board and the SC780 controller board. The SC780 interfaces with the Bus Translator via the V-MASTER Interface (VMI). It is the VMI bus which permits two controllers to be used as part of the V-MASTER/780. The translator board provides the SBI arbitration logic, storage for programmed I/O address and data, and storage of DMA addresses and data. Its primary function is to buffer between the quadword DMA on the SBI and the dualword transfer of the VMI. When doing disk write operations, the memory data is automatically prefetched to the buffers of the translator board for more efficient operations on the VMI bus. The translator board provides DMA buffering for two controllers.

2.1.2 SC780/B1 Controller

The SC780/B1 is implemented with the same hardware as is Emulex's SC750/B1. The firmware that drives the SC780/B1 is, however, unique to that controller. The SC780 and SC750 are not functional equivalents.

The controller is organized around a 16-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with twelve 2K x 4 PROMs.

The controller incorporates a 1K x 16 high-speed RAM buffer which is used to store the controller's MBA and drive registers, map registers and one sector of data buffering.

The A Cable Register (ACR) provides the storage of all A cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

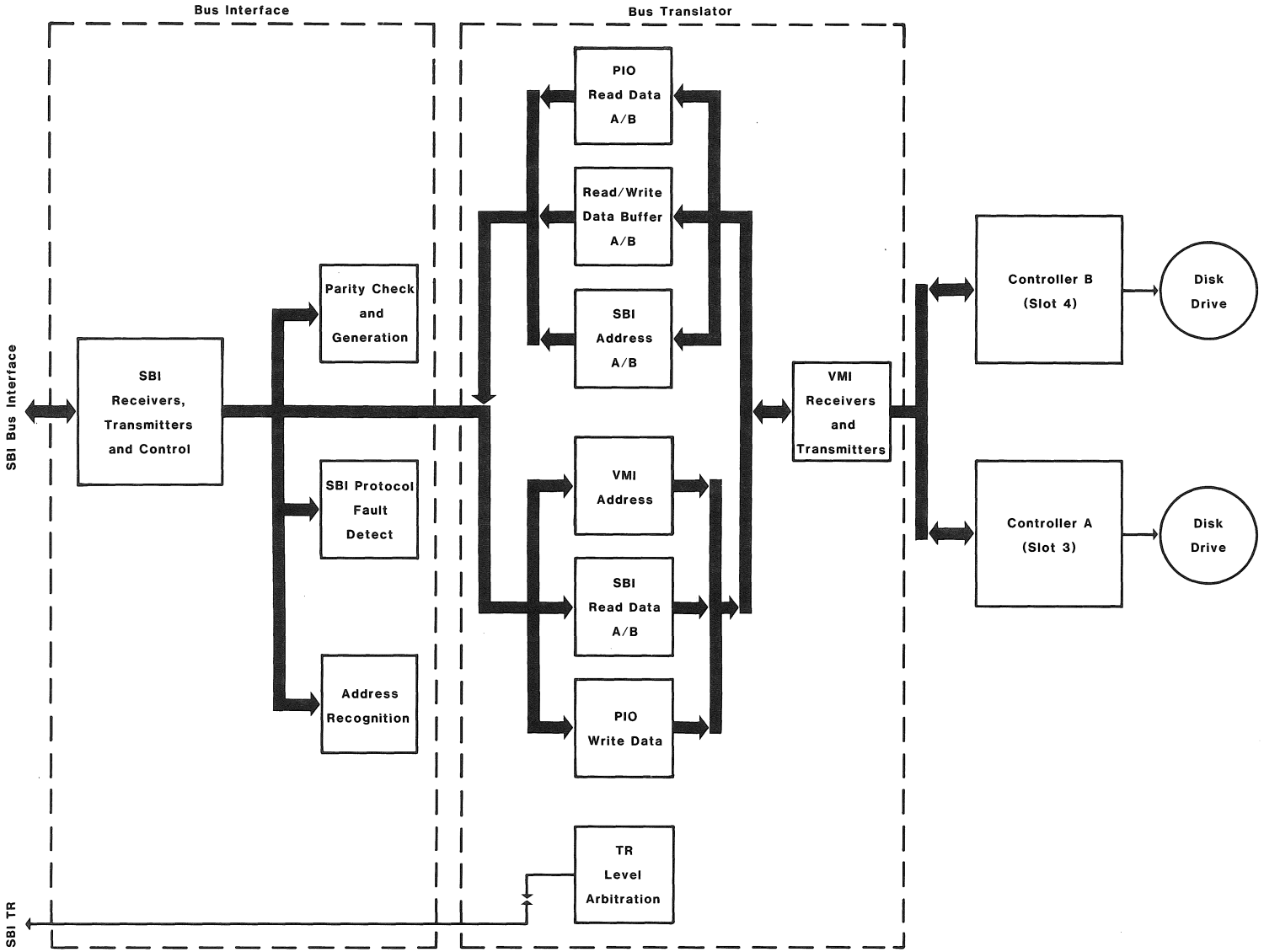

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Figure 2-1. V-MASTER Block Diagram

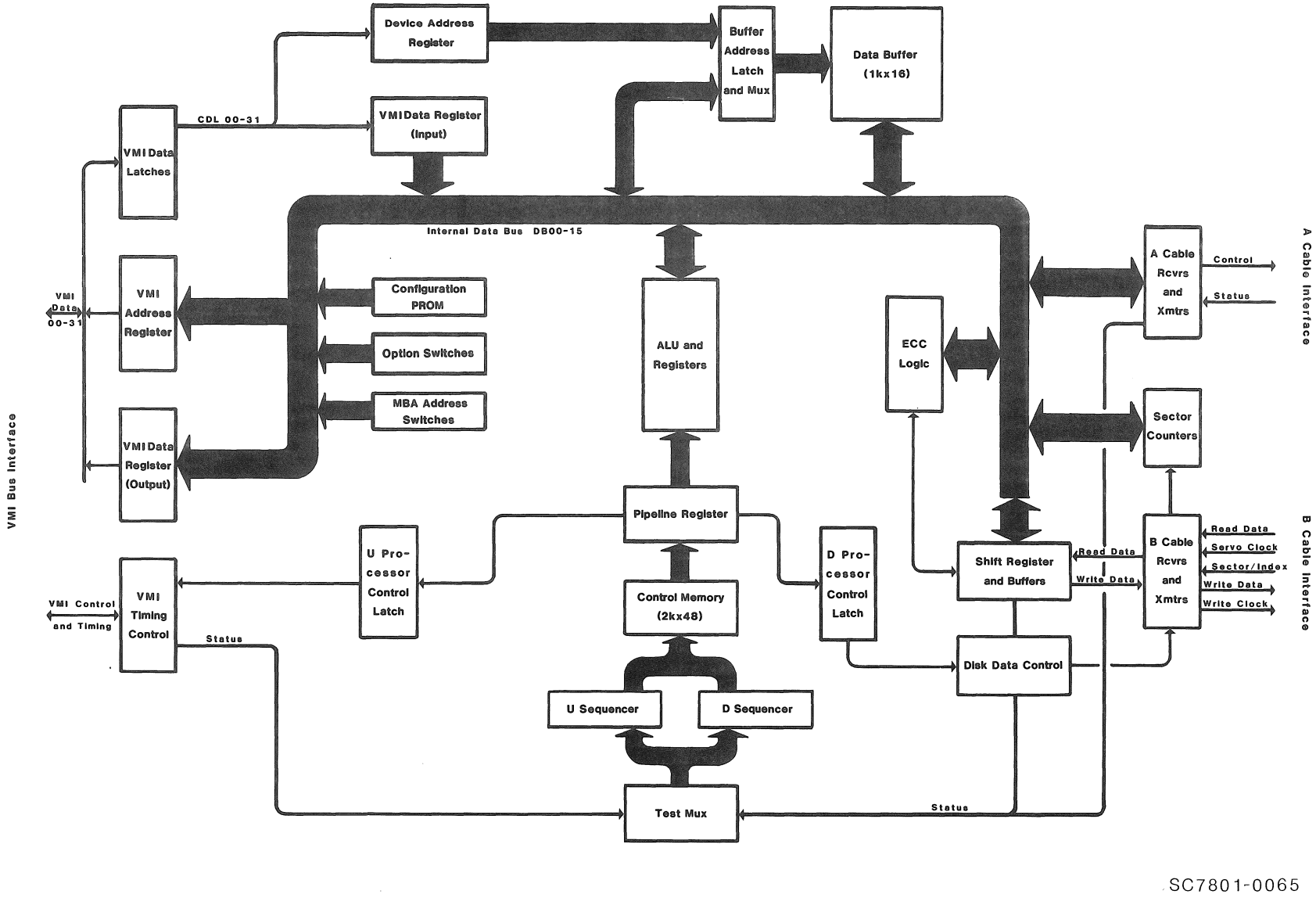


Figure 2-2. SC780 Block Diagram

Serial data from the drive is converted into 16-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC polynomial operation is done independently of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

A configuration PROM is a source to the data bus. This PROM configures the maximum cylinder address, maximum track address and drive type code for each of the logical drives.

The computer interface to the V-MASTER/780 is a 32-bit wide VMI bus over which addresses and data are transferred. DMA operations transfer 32-bit words to the V-MASTER/780, which does 64-bit quadword transfers to the SBI. The VMI bus is used for programmed I/O and DMA data transfers. The microprocessor responds to all programmed I/O and carries out the functions required for the addressed controller register. The microprocessor controls all DMA operations and transfers data between the VMI and the internal buffer.

2.2 PHYSICAL DESCRIPTION

The V-MASTER/780 is shown in Figure 2-3 with the SC780 Controller PCBA, the Emulex SBI Terminator and the Cable Paddle Board.

2.2.1 V-MASTER/780

The V-MASTER/780 assembly consists of a four-slot wire-frame card cage with an integral backplane and the Bus Interface and Bus Translator PCBAs. The Interface Board is installed in slot 1 and the Translator Board in slot 2. The remaining two slots are used for the controller PCBAs. The card cage is designed to mount in the DEC/11-780 CPU chassis in place of the DEC RH780 or SBI terminator. Its overall dimensions are 3.125 x 20 x 13.375 inches.

2.2.1.1 Connectors

The SBI enters the V-MASTER backplane via headers J7 through J12 on the right hand edge of the backplane. The SBI exits at headers J1 through J6 on the lefthand edge of the backplane. See Figure 2-4 for SBI signal identification.

The two sets of headers on the backplane associated with slots 3 and 4 are for interfacing the cable paddle boards to the controllers.

Connectors J13 and J14 are both used to carry -5.2 vDC to or from the V-MASTER. J15 connects the AC/DC Low harness to the V-MASTER. B-plus and ground are provided using the two sets of studs and solder pads below the connectors.

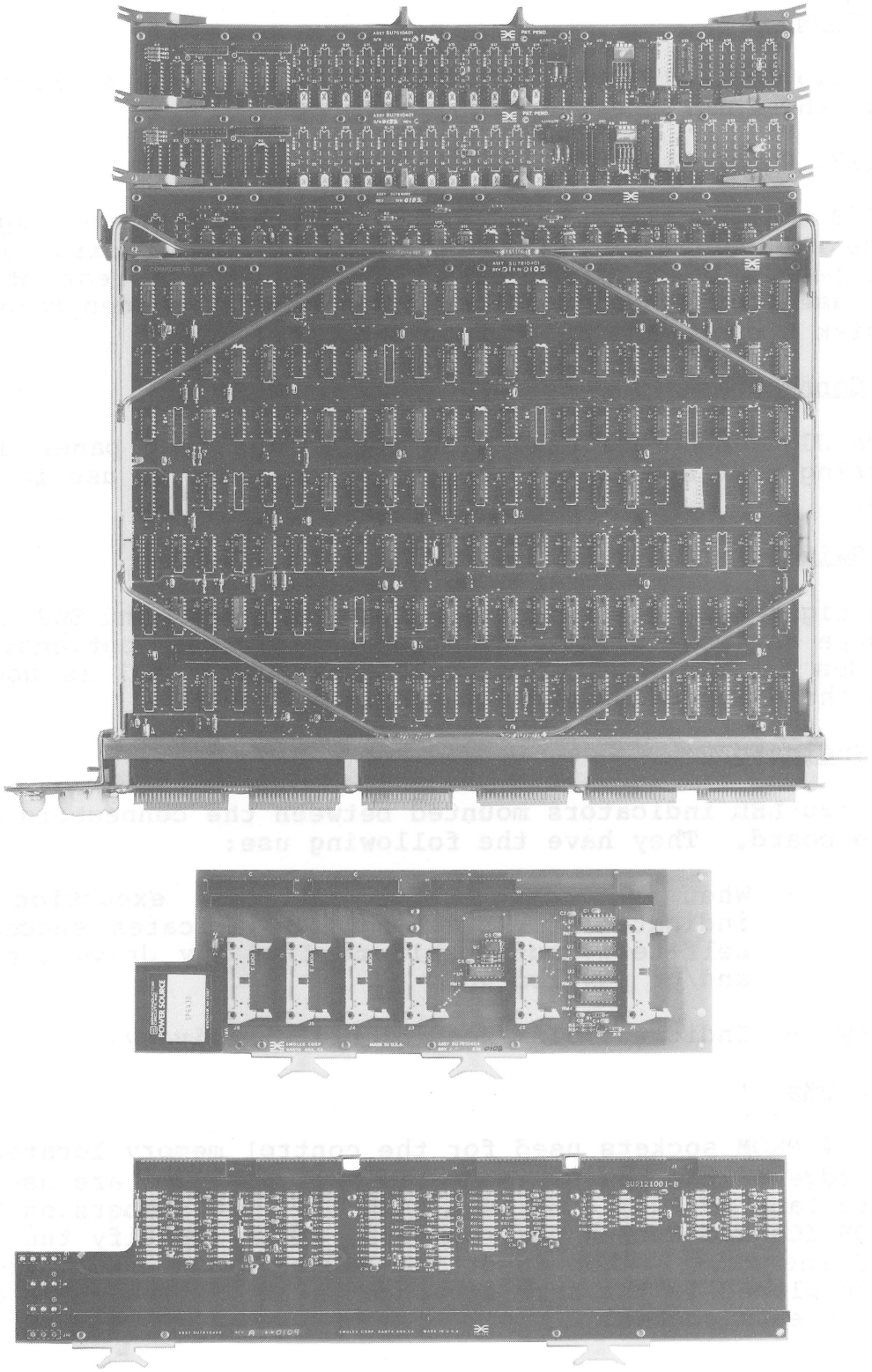


Figure 2-3 V-MASTER/780

SC7801-0066

2.2.1.2 Switches

The Interface Board (SU7810401) has a single DIP switch, SW1. The switch is used to select the TR number for the NEXUS.

2.2.1.3 PROMs

There are two control PROMs, 591 and 592, located in sockets at U76 and U78 on the Interface Board.

2.2.2 SC780 Controller

The SC780/B controller consists of a single board which plugs into one of the two controller slots of the V-MASTER/780 card cage. A connector paddle board plugs onto the pins at the rear of the connector used for the controller. This board provides connection for the disk A cable and up to four B cables.

2.2.2.1 Connectors

Connectors J1 and J2 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2.2 Switches

The three eight-pole DIP switches labeled SW1, SW2 and SW3 are used to configure the controller. SW1 provides firmware options, while SW2 provides selection of drive configurations. SW3 is used to configure the MBA address and SBI arbitrate level.

2.2.2.3 Indicators

There are two LED indicators mounted between the connectors at the top of the board. They have the following use:

Fault - When ON, unsuccessful self-test execution is indicated. A flashing LED indicates successful self-test, but unable to find any drive connected and/or powered-up.

Activity - Indicates disk read or write activity.

2.2.2.4 PROMs

There are 24 PROM sockets used for the control memory located along the right edge of the board. Normally only 12 PROMs are used. The sockets are labeled PROM 0 through PROM 11. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

2.2.3 Paddle Board

2.2.3.1 A Cable Connectors

The 34-pin flat cable connector labeled J1 and the 26 pin connector labeled J2 at the top edge of the board are used for the A cable which daisy-chains to all the drives for control and status. Two connectors are used for the 60-conductor A cable to reduce the size of the paddle board. This does require a special A cable. Pin 1 is located on the left side of the connectors. The circuitry on the board are the A cable drivers.

2.2.3.2 B Cable Connectors

The four 26-pin flat cable connectors labeled J3, J4, J5 and J6 are for the radial B cables to each of four physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The four B cable ports are all identical and any drive may be plugged into any connector.

2.3 INTERFACES

2.3.1 Disk Interface

The A cable signals are taken off the controller board on the lower half of the backplane B connector (pins 53-92). The four sets of B cable signals are taken off the controller board on the backplane C connector (pins 3-42 and 53-92).

The controller implements the eleventh cylinder bit on the normally spare A cable pins 30 and 60.

The controller's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatible with these drives electrically and in timing.

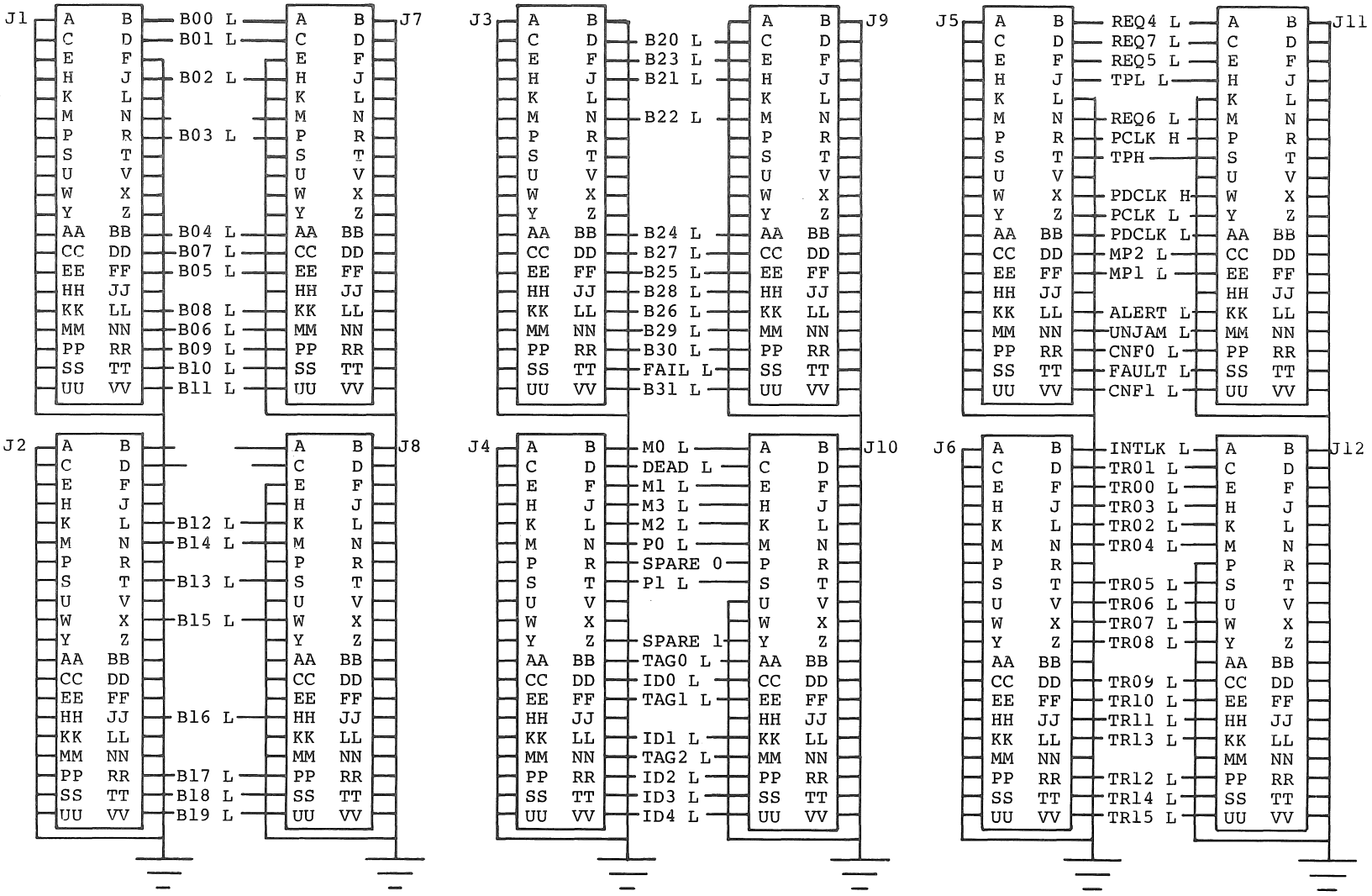
The following paragraphs define the electrical interface and the recommended cables.

2.3.1.1 Drivers and Receivers

The drivers for the A and B cables are MC3453, which are equivalent to the 75110A. The receivers are MC3450 quad differential receivers, which are equivalent to 75108 receivers. The lines of the A cable are terminated with 82 ohms to ground. The lines of the B cable are terminated with 56 ohms to ground.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		To
2,32	Tag 2		To
3,33	Tag 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Address Mark Found		From
21,51	Busy (dual port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Seek End		From
22,9	Unit Selected		From
12,24	Index		From
13,26	Sector		From



SC7801-0067

Figure 2-4. SBI Signal Names and Pin Assignments

2.3.1.2 A Cable

The 60-conductor A cable is daisy-chained to all drives and is terminated at the last drive. The signals carried by this cable are listed in Table 2-1. Signal function when the control tag (Tag 3) is asserted is also indicated. The A cable should be 30 twisted pair flat cable with an impedance of 100 ohms and an cumulative length of no greater than 100 feet.

2.3.1.3 B Cable

The 26-conductor B cable is a radial to each drive and contains the data and clock signals. In addition, it contains sector and index signal to drive the sector counter for the drive. The signals and grounds in this cable are listed in Table 2-1. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 50 feet.

2.3.1.4 Pick and Hold Signals

The Pick and Hold signals which control the starting of the disk drive when it is remote are activated when the controller is not being reset by DCLO.

2.3.2 SBI Interface

The Synchronous Backplane Interconnect (SBI) is a 32-bit synchronous (clocked) bus on which information is transferred in 200 ns. time slots. It transfers data and addresses in a multiplexed manner. The CPU accesses the controller by means of this interface for reads and writes of the controller's registers and the controller uses it for DMA data transfers with memory. See Figure 2-4.

2.3.2.1 Transfer Request (TR) Number

Each NEXUS on the bus is assigned a transfer request number which represents its priority for accessing the bus and bits <14:11> of the NEXUS' (controller's) physical address. Numbers 8, 9, 10 and 11 are normally used by MBA's. This number is assigned by SW1-1 thru SW1-4 on the Emulex Bus Interface Board.

2.3.2.2 Interrupt Priority Level

Each NEXUS is assigned a interrupt priority level of 4, 5, 6 or 7. This assignment is done by SW1-5 and SW1-6 on the Bus Interface Board.

2.3.2.3 Register Address

The controller's base address is determined by the TR number assigned to the NEXUS. The four bases normally used are: 20010000, 20012000, 20014000 and 20016000. Four additional NEXUS bases are

available in the 20008000 to 2000E000 range (see Appendix E). When two controllers are to be used in the same chassis, they must be an even and odd TR pair. The even TR is assigned to the controller in slot 3.

2.4 DISK FORMAT

2.4.1 Disk Organization

The SC780/B1 emulates one or two logical RM drive units per physical drive. In all cases the number of sectors formatted per track is typically 32. The unit number of the physical drive must be in the range of 0-3.

When a physical drive has two logical RM units mapped onto it, the first logical unit will be mapped onto the first half of the heads and have a unit number the same as the physical unit number. The second logical unit will be mapped onto the second half of the heads and have a unit number which is four greater than the physical unit number.

2.4.2 Track and Cylinder Mapping

When the number of heads on the physical drive is equal to the number of tracks on the RM drive being emulated, there is a one to one correspondence between tracks and cylinders. This is essential for media compatible disk packs such as RM03 and RM05. When the physical drive has a number of heads which is different than the RM drive, the controller operates in a mapped track and cylinder mode. When operating in this mode with RM03/RM05 emulations, the drive should be configured for one extra sector so that there is additional time at the end of each track to do the mapping.

2.4.3 Sector Organization

Figure 2-5 shows the sector format used by the controller. Each track of 20,160 bytes is typically divided into 32 sectors of 630 bytes. The four byte header is preceded by a preamble of 30 bytes ending in the sync byte and is followed by a two byte CRC. The 256 word data field is preceded by a preamble of 20 bytes ending in the sync byte, and is followed by four bytes of ECC. This format is compatible with that of the DEC RM02/RM03 and RM05.

If the actual size of the useful data information is less than 512 bytes, the remainder of the data field will be filled with zeros until 512 bytes have been written. During disk formatting procedures, each data track is located and recorded with header information by means of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual or groups of sectors should not be reformatted unless absolutely necessary.

Sector Length 630 Bytes						
Preamble+Sync	Header	CRC	Preamble+Sync	Data Field	ECC	Recovery
30	4	2	20	512	4	58

Figure 2-5. Sector Format

Header Word 1:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	SSF	1	0	0	Cylinder Address									

Header Word 2:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Track Address								Sector Address							

Header Word 3:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Cyclic Redundancy Code (CRC)															

Figure 2-6. Header Format

2.4.4 Header

2.4.4.1 Header Description

Figure 2-6 shows the header format, which consists of the following three words:

Word One -

This word contains the cylinder address. It contains a one-bit in bit 12 to identify 16-bit format to the software and one-bits in bit positions 14 and 15 to identify a good sector. For RM80 emulations, a one in bit 13 indicates that the data for this sector has been relocated to the next sector.

Word Two -

The low-order eight bits of this word contain the sector address. Each track on the drive typically contains 32 sectors. The upper byte of this word contains the track address.

Word Three -

This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

2.4.4.2 Header Field Handling

After the drive reports that it is on cylinder, the controller locates the desired sector by means of sector counters that are maintained in the controller. A counter is maintained for each drive. The controller compares the first two words of the header against the desired track, sector and cylinder and then checks the CRC word for errors. An error in the header field is indicated by turning on the appropriate error bit in the error register (format error, header compare error, bad sector error, skip sector error or CRC error). A header error is only valid when the sector count field of the RMLA register and the sector field of the RMDA have already matched. It is immaterial where a CRC error occurs in the header field since the controller cannot determine its location in the field. However, software may read the header to memory by means of a Read Header and Data command. The header compare may be inhibited by setting the HCI bit in the RMOF register.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

The controller can be cleared using the following methods.

a. Controller Clear - Controller Clear is performed by writing a one-bit into the INIT bit of the MBACR or by UBUS DCLO. This causes the following to be cleared or set:

- MBACR, MBASR, MBABC, MDACSR bits <31:16>. Set MBADR to BF_{16}.

- In all drives: RMCS1 bits <06:00>; RMER1; RMER2; RMDA; RMAS ATA bit; RMEC2; RMDS ATA, ERR and LST bits; RMMR1 bits <15:04>, <02:00>. Sets bit 03 of RMMR1 and DRY of RMDS.

b. Error Clear - The error bits in MBASR are cleared by writing a one-bit into the bit position and by the start of another data transfer operation.

c. Drive Clear - The Drive Clear is a command (Code 9). This causes the following registers in the addressed drive to be cleared:

   - RMER1; RMER2; RMAS ATA bit; RMEC2; RMDS ATA and ERR bits; RMMR1 bits <15:04>, <02:00>. Sets bit 03 of RMMR1.

2.5.2 Interrupt Conditions

The controller generates a CPU interrupt if the Interrupt Enable (IE) bit is set upon the following conditions:

a. Upon termination of a data transfer, either normally or abnormally.

b. Upon assertion of any of the drive attention bits.

c. Upon occurrence of a Programming Error (PGE), Non-Existent Drive (NED), Missed Transfer Error (MXE), Power Down (PDN) or Power UP (PUP). A Power Up will set IE and generate an interrupt.

The interrupt condition will persist until the interrupting status bits are cleared.

2.5.3 Termination of Data Transfers

A data transfer which has been successfully started may terminate in the following ways:

a. Normal Termination - Byte count overflows to zero and the controller becomes ready at the end of the current sector.

b. Controller Error - One or more of the following MBASR bits are set:

Data Transfer Abort (DTA)
Data Late (DLT)
Write Check Upper Error (WCU)
Write Check Lower Error (WCL)
Missed Transfer Error (MXE)
Exception (EXC)
Invalid Map (IM)
Error Confirmation (EC)
No Response Status (ITO or RTO)

c. Drive Error - The ERR bit in the RMDS register and at least one bit in RMER1 or RMER2 register is set. The ATA for the drive doing the data transfer becomes asserted.

d. Program-Caused Abort - By setting the Abort or INIT bits in MBACR the program can terminate a data transfer operation.

2.5.4 Ready Bits

There is no ready bit for the controller. Data Transfer Busy (DTB) in MBASR is set when a data transfer operation is underway. It is cleared when the data transfer is terminated. On read operations this occurs when the last word has been transferred to memory. On write operations this occurs when the last sector has been written. Data Transfer Complete (DTC) is set when the operation terminates.

DRY (RMDS, bit 07) is the ready indicator for the selected drive and is the complement of the drive's GO bit. To successfully initiate a data transfer command this bit must be asserted. However, a non-data transfer command (Search, Drive Clear) may be issued to a drive at any time DRY is asserted, regardless of the state of the DTB bit.

When a data transfer command is initiated DRY becomes negated and DTB becomes asserted.

2.6 DUAL CONTROLLER OPERATION

SMD drives may be equipped with a dual port option which provides the capability for two controllers (generally on separate computers) to access the drive. The SC780/B controller supports this type of operation as a standard feature. This mode of controller operation is selected by setting SW1-6 ON. Most of the dual port functions of the DEC controller being emulated are supported, and those which are not should be transparent to a properly written dual port driver. Table 2-2 summarizes the controller register responses in dual port operation.

2.6.1 Dual Port Drives

The two drive ports are known as Channel I and Channel II. Because only one controller at a time may access the drive, access is granted on a first-come, first-served basis. Once a controller has gained access to the drive, the other controller is denied access

until the first controller's operation is complete. However, each channel has a physical disable switch which can disable the port and prevent the associated controller from having access to it.

2.6.2 Unseized State

The drive is in the unseized state when it is not connected to either controller. The CPU must issue a request for the controller to seize the drive. This request is done in one of the following ways:

a. Writing into any drive register, including read-only registers.

b. Writing a one-bit into the drive's ATA bit in RMAS. The bit does not have to be set.

2.6.3 Seized State

The drive is seized when it is logically connected to one of the controllers. At that time DVA (RMCS1, bit 11) is set indicating that the drive is ready to communicate with the controller which has seized it. If the drive has already been seized by the other controller, then the DVA bit will not set, all the drive registers will read as zeros and any write to a register will be ignored. Attempts to seize a drive which is busy with the other port are remembered and then acted upon when the drive is released by the other controller.

2.6.4 Returning to the Unseized State

The drive is released and returned to the unseized state by issuing a release command. In addition, a one second timer in the controller will timeout and release the drive if one of the events listed in section 2.6.2 for seizing the drive is not performed periodically to keep resetting the timeout timer. Reading the RMCS1 register will also reset the timeout timer if the drive is currently seized. This allows the CPU to check a drive's seized state, and if seized, not have to worry about a time-out release occurring.

When the controller sees a previously busy drive becoming unseized, it checks its request flag. If the flag is set (the drive had been requested while busy on the other port), the controller will seize the drive and set ATA causing an interrupt to the CPU if the IE bit is set. If the CPU does not respond to the attention within one second the drive will be released, but ATA remains set.

2.6.5 DEC Compatibility

The SC780/B controller differs from the equivalent DEC controller in three important areas.

First, there is no neutral state. Since the SC780 does not have instantaneous access to all drives at the same time (a limitation of the daisy-chained A cable and the microprocessor organization of the controller), the controller assumes the drive is busy on the other port if the controller has not already seized it. Thus, a read of RMCS1 will always indicate that the drive is seized by the other controller (DVA, bit 11 equals zero) unless the drive has been previously requested. The CPU must request the drive by writing into any drive register and waiting until the ATA bit is set. This indicates that the controller has seized the drive. If the drive was in reality not seized by the other controller, the ATA bit will set almost immediately. The DEC controllers, however, can switch from neutral to seized state within the time required to do a single read or write of a drive register. Thus, if the drive is not already seized, no ATA is set and the drive is immediately available to the seizing controller.

Second, the release command is not instantaneous since the controller takes a few microseconds to execute the command. During this time the drive will appear to be unseized.

Third, during a data transfer the timeout timers will not operate and the drives can not be polled to see if they are not busy. Therefore no drives are seized or released during the execution of a data transfer.

The software driver should not issue a Release command and then attempt to save the current status of a drive, since the Release command will immediately show the drive in the unseized state, thus returning zero data for the drive registers. In order to allow the other controller time to poll the drive, the CPU should not communicate with any of the released drive's registers until required to seize the drive again.

2.6.6 Dual Port Drives in Single Port Mode

When using an operating system which does not have dual port drive software support, it may still be advantageous to use dual port drives while operating in the controller in single-port mode. This will allow for a non-dynamic type of operation between two CPUs. In this type of operation the controller does not unseize the drive and, in effect, it is seized by both controllers all the time.

The one-second timer (and the release command) operate exactly as stated in paragraph 2.6.4. Even when released, a drive will still appear to be seized to the releasing controller. No attention is generated when the other controller finds the drive not busy. Should a command be issued to a controller while a drive is busy on the other port, the controller will wait until the drive becomes unbusy before executing the command. No timer exists in this case.

This mode of operation eliminates the need for manually switching the drive from one controller to another.

2.6.7 Dual Access Mode (Firmware Revision C and above)

In order to provide compatability with VMS when it is configured for dual access, the dual access mode is provided (SW4-4 ON). When in this mode, the controller sets Dual Port Mode (Drive Type Register) and Programmable (Drive Status Register) to imitate the DEC neutral state. The controller still functions in single-port mode as described in paragraph 2.6.6, above.

When DPM and PGM are set, the operating system will attempt to seize a drive by simply writing a command to it. If the drive is unbusy the command is executed. If the drive is already busy on its other port, the controller simply waits until it is released and then seizes and commands it. VMS has a timer with a sufficiently long period to prevent causing a timeout when it is forced to wait.

The first time the SC780 sees a drive it is ignored for one second. This one-second stall occurs once for each drive on the controller. It prevents the controller from seeing erroneous status information when power is applied to the drive after the controller has been powered up. For a drive in dual port mode the stall will prevent the other CPU from accessing the drive until the stall completes. The dual access option switch by-passes the stall in all cases. For proper system operation with the dual access option switch ON, all drives must have power applied before either controller is powered-up.

Setting the Dual Port Option switch overrides the Dual Access Option except for the power-on stall.

Table 2-2
Register Access on Dual Controller Operation

Drive State:	Response With Respect To Action On Ch. I
Read RMCS1	
Drive Not Seized:	Reads all zeros. No request flag is set.
Drive Seized by Ch. I:	DVA = 1; reads the register. Resets timer.
Drive Seized by Ch. II:	DVA = 0; reads all zeros. No request flag is set.
Read any other drive register	
Drive Not Seized:	Reads all zeros.
Drive Seized by Ch. I:	Reads the register.
Drive Seized by Ch. II:	Reads all zeros.
Write RMCS1	
Drive Not Seized:	The function code is attempted if GO = 1 and a port request flag is set.
Drive Seized by Ch. I:	Loads the function code. (Switches to unseized if the function is a Release).
Drive Seized by Ch. II:	The function code is attempted if GO = 1 and a port request flag is set.
Write any drive register except RMCS1	
Drive Not Seized:	The write is ignored, and a port request flag is set.
Drive Seized by Ch. I:	Loads the register if not a read-only register. Resets timer.
Drive Seized by Ch. II:	The write is ignored, and a port request flag is set.

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Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC780/B Disk Controller in a VAX-11/780 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item two, Inspect the SC780, is covered in paragraph 3.2).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Introduction to the VAX-11/780 hardware.
2. Inspect the V-MASTER.
3. Prepare the disk drives.
4. Check the DEC MBA priority plugs and address range jumper.
5. Prepare the V-MASTER/780.
6. Prepare the SC780 controller.
7. Install the V-MASTER assembly.
8. Cable the VAX backplane.
9. Route the drive I/O cables.
10. Test the controller.

3.1 AN INTRODUCTION TO THE VAX-11/780

The VAX-11/780 is contained in a freestanding cabinet which provides power distribution and cooling as well as a chassis for mounting the various wire-frame card cages that hold the 11/780's electronics. The basic VAX-11/780 chassis is designed to accommodate five card cages. Leftmost is the KA780 CPU card cage which has 29 slots. To the right of the CPU is the DW780 Unibus Adaptor, a six slot card cage. Next in line to the right is the MS780 memory card cage with 20 slots. The next two slots are reserved for six-slot RH780 Massbus Adaptors. The final and right-most slot is used for the DEC SBI terminator. Figure 3-1 shows a VAX-11/780 with all of the above installed. Figure 3-2 shows the backplane in the same configuration.

Each wire-frame card cage makes up a segment of the Synchronous Backplane Interconnect (SBI). The various segments of the SBI are connected together using coaxial connectors. Consequently, it is a simple matter to remove or add card cages as required.

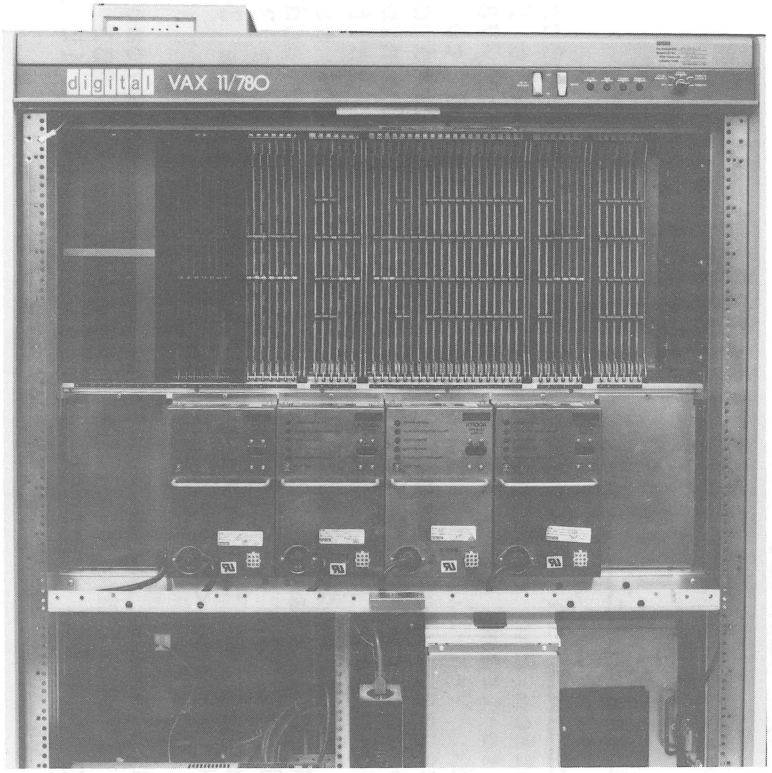


Figure 3-1 VAX-11/780
Standard Configuration (Front View)

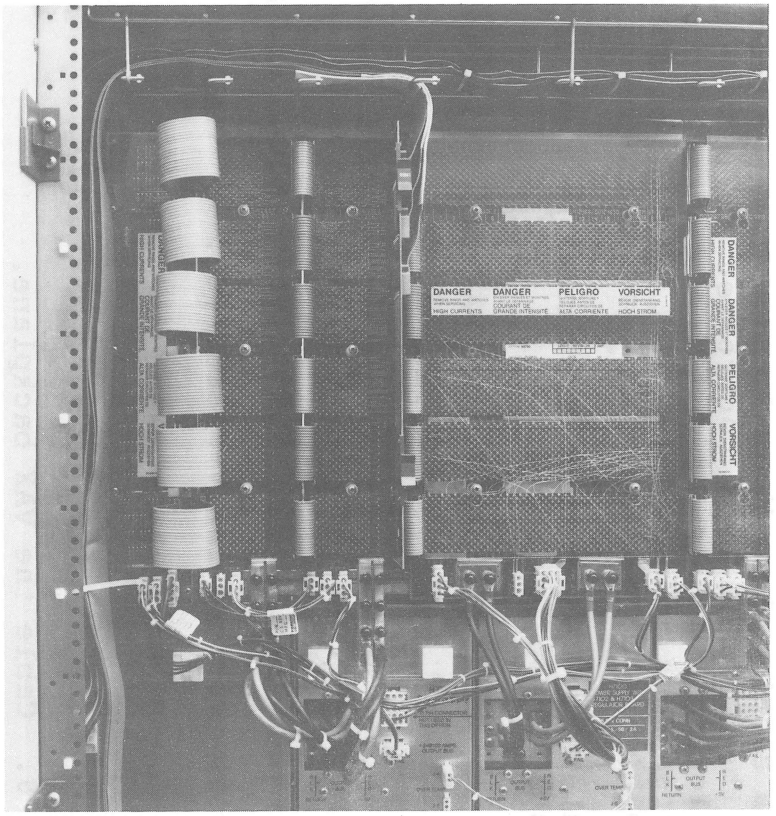


Figure 3-2 VAX-11/780
Standard Configuration (Rear View)

As noted above, the VAX-11/780s are designed to accommodate two RH780 Massbus adaptors. Most are delivered with one RH780 which is located in the leftmost of the two available slots. This leaves the second slot open for the installation of an Emulex V-MASTER 780. Should both RH780 slots be occupied, however, a V-MASTER 780 can be installed in the slot occupied by the DEC SBI Terminator. The DEC terminator is then replaced by a more space efficient Emulex terminator. This second option allows up to three Massbus adaptors to be installed in the main cabinet. If desired, one or more V-MASTERs can be installed in an expansion cabinet.

3.2 INSPECTION

Before unpacking the V-MASTER chassis, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

Make a visual inspection of the board after unpacking. Check specifically for bent or broken connector pins, damaged components or any other evidence of physical damage. Examine the PROMs to insure that they are firmly and completely seated in their sockets.

3.3 DISK DRIVE PREPARATION

3.3.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC780. This allows the I/O cable routing and length to be accurately judged. Place the drives side by side to make installation of the daisy-chained A Cable simpler.

3.3.2 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive front panel (local) or the controller (remote). Place the switch in the REMOTE position. With the VAX-11/780 powered down, press the START switch on the front panel of each of the drives (the START LED will light, but the drive will not spin up and become ready). When the VAX is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the remote mode the drives will power down when the VAX is powered down. While the VAX is powered on, the drives may be powered up and down individually (to change disk media, for example) using the drive START switch.

3.3.3 Sectoring

When using drives that allow the emulation to produce a one-to-one correspondence between the physical and logical (that is, emulated) recording heads, the drives are typically configured for 32 sectors per track.

When the physical drive has a different number of heads than the emulated RM drive, there is no one-to-one correspondence between the physical and logical heads. To accomplish this the controller operates in a mapped track and cylinder mode. When operating in this mode the drive is configured for one extra sector so that there is additional time at the end of each track to do the mapping.

The disk drives must be hard sectored as indicated in the SECTS column of Table A-1.

Because the procedure for entering the sector numbers differs from drive to drive, consult the drive manufacturer's installation manual for instructions.

NOTE: See paragraph A.2.3 for information regarding the sectoring of CDC and the Fujitsu 2351A models.

3.3.4 Drive Numbering

An address from 0 to 3 must be selected for each drive. Be careful that no two drives are assigned the same number. Drive addresses are selected by means of an ID plug or have their addresses selected by switches on one of the logic cards. Consult the particular drive manual for the exact procedure.

3.3.5 Sector and Index Modifications

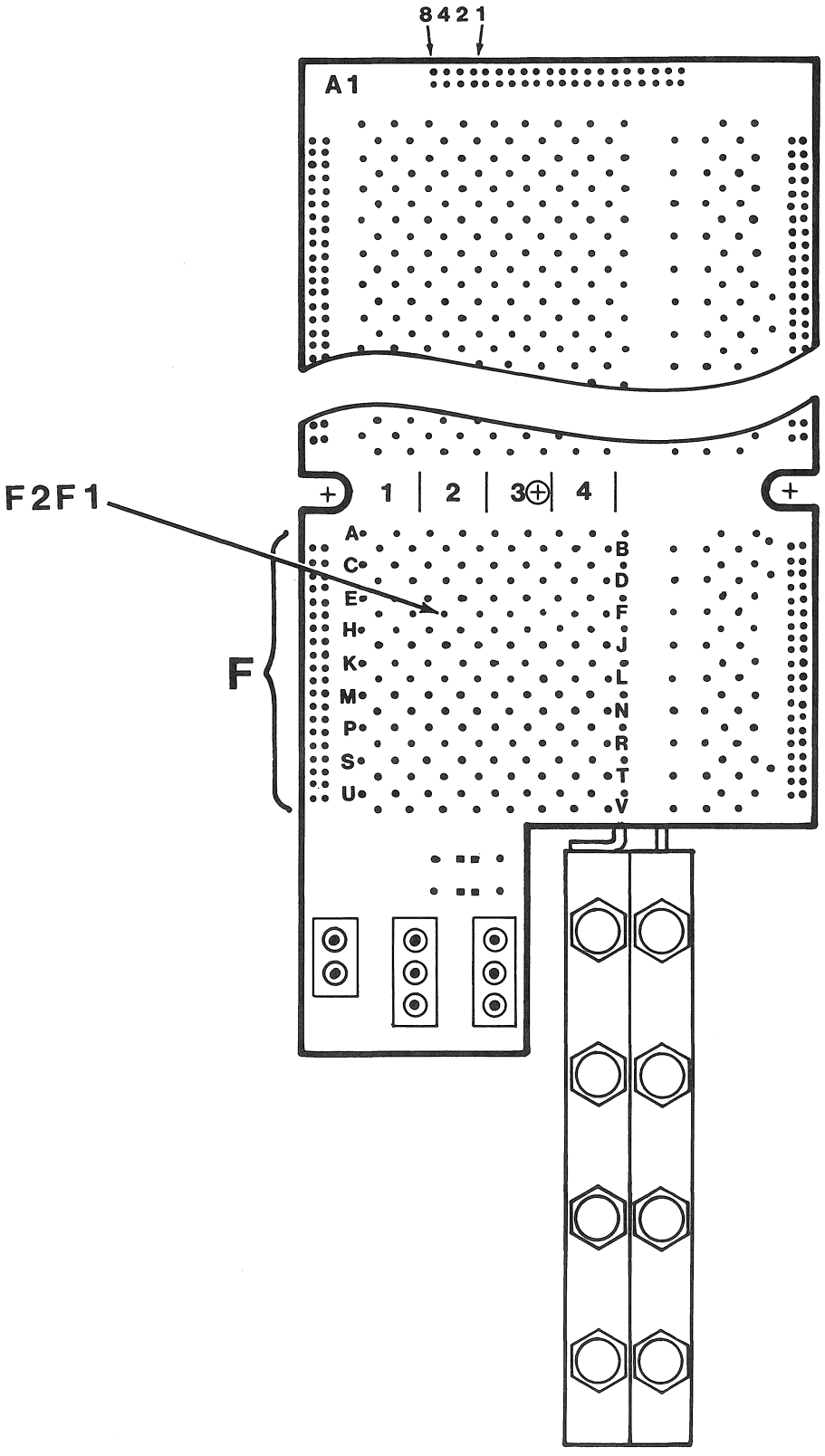
The SC780 is designed to receive the sector and index signals from each drive on the B cable (see paragraph 3.6.5). Depending on the disk drive, the index and sector pulse signals may be carried on the A instead of the B cable. However, in most cases they are easily moved to the B cable by minor rewiring of the drive backplane, or this configuration may be ordered from the factory.

The procedure for moving the sector and index signals from the A to the B cables for several of the more common drives is described in Appendix B. If the procedure for the drive in question is not covered there, it is generally described in the drive manual.

NOTE: To prevent significant performance degradation when using more than one drive, Emulex strongly recommends modifying the drive to place the sector and index signals on the B cable if the drive is not delivered in that configuration.

3.3.6 Sectoring the 2351A Fujitsu for the SC780/B

The setting of the number of sectors for the 2351A Fujitsu (Eagle) will be dependent upon the type of Emulex SC780/B firmware the user has. Users with the /B1 firmware must configure the Eagle for 44 hard sectors. Those with /B3 firmware must configure the Eagle for 48 sectors. This 48 sector configuration supports an additional 40 Mb of capacity. See Table A-2 for the list of configurations supported by the SC780/B. Note that in Table A-2 configurations



SC7801-0070

Figure 3-3. RH780 Backplane

for the 2351A Fujitsu (key 470) are listed as being configured for 44/48 sectors. Those configurations are supported at 44 sectors per track by the /B1 firmware and 48 sectors per track by the /B3 firmware.

NOTE: See paragraph A.2.3 for more information concerning the sectoring of the 2351A Fujitsu.

3.4 DEC MBA PRIORITY

Before the installation of an additional NEXUS (V-MASTER, DEC MBA, DEC UBA), the TR level and address range of all previously installed NEXUSes must be determined to prevent assigning the new devices the same TR level or address.

By convention, DEC TR levels are associated with the various NEXUS address ranges as shown below:

Base Address	TR Level	Setting Number	Base Address	TR Level	Setting Number
20008000	TR4	3	20010000	TR8	7
2000A000	TR5	4	20012000	TR9	8
2000C000	TR6	5	20014000	TR10	9
2000E000	TR7	6	20016000	TR11	10

For DEC MBAs, the TR level and the address range are selected separately.

A combination of pin/plugs at the top of the DEC MBA chassis backplane are used to determine the base address for that MBA. The pin/plugs are weighted, starting with the leftmost pair of pins and counting four pairs to the right: 8, 4, 2 and 1. The sum of the pin/plugs equals the Setting Number for the desired address as shown in the table above. For example, if the desired address is 20010000, the 4, 2 and 1 pin/plugs would be installed. Pins to the right of these four pairs are used for Bus Request (BR) level selection. It is not necessary to determine the BR level of the RH780 or select a different one for the V-MASTER.

A jumper wire on the second module slot of the MBA backplane determines the TR level. The different jumper installations are shown below:

F2F1 to F2C1 = TR1	F2F1 to F2J2 = TR7
F2F1 to F2D1 = TR2	F2F1 to F2M1 = TR8
F2F1 to F2E1 = TR3	F2F1 to F2N1 = TR9
F2F1 to F2F2 = TR4	F2F1 to F2P1 = TR10
F2F1 to F2H2 = TR5	F2F1 to F2P2 = TR11
F2F1 to F2J1 = TR6	F2F1 to F2S2 = TR12

The explanation below describes pin location designation and should be used in conjunction with Figure 3-3. The pictorial representation of the backplane includes letters which are not actually shown on the board itself. They are included in the figure to help identify pin locations. Also the numbers shown in the figure do not appear in the same location on the backplane; rather, they are located in about the center of the board, not directly above block "F."

Jumper locations are defined by a series of numbers and letters which define pin locations by block, column and row. The first letter designates the block. The blocks of pins are lettered sequentially, beginning with "A" at the top, and proceeding to the bottom block, which is "F." The next character is a number and designates the column which is four pins wide. Thus, the first four columns at the left are in column "1." The next letter indicates a row of pins. Each row is labeled in the figure. Note that the each row of pins is offset from the row immediately above and below it. The last character differentiates between the two pins on the same row that are covered by the same column number. A "1" indicates the left pin of that column in a particular row, and a "2" designates the right pin. In Figure 3-3 pin F2F1 is indicated by an arrow.

Normally it will not be necessary to change the TR level of an installed DEC MBA, since it is desirable to have the V-MASTER at a lower TR level (TR10 or TR11) because of its full sector buffer.

3.5 V-MASTER/780 SETUP

The V-MASTER/780 consists of a wire chassis and an Emulex VMI backplane capable of accepting four PCBAs. Two of the PCBA slots are dedicated to the hardware necessary to interface the DEC SBI to the Emulex controller(s). The boards, the Interface PCBA (SU7810401) and Translator PCBA (SU7810402), are considered part of the V-MASTER assembly. These paragraphs describe the steps necessary to configure those PCBAs for a particular application. The remaining two chassis slots are reserved for the SC780 controller hardware (SC7510401). The procedure for setting up the controller hardware is contained in paragraph 3.6.

3.5.1 PCBA Removal

Remove the Interface PCBA from the V-MASTER chassis to gain access to SW1, the DIP switch necessary to configure the subsystem. It is not necessary to remove the Translator PCBA.

3.5.2 SBI Arbitration (TR No.) Level

Each NEXUS on the SBI is assigned a number which is its transfer request (TR) arbitration level (essentially the controller's address). The MBA controllers are normally assigned addresses in the range 8-11. (The controller can handle numbers 4-11.) When a

pair of controllers are to be used in the V-MASTER, the two MBA controllers that they represent must be assigned an even-odd pair of addresses such as 6 and 7 or 10 and 11. (The DEC MBA is generally assigned to TR8.) The TR level setting is made for the even addressed controller (slot 3); the second controller (slot 4) is assigned the odd address (see paragraph 3.6.2, below). This even-odd arrangement applies only to dual controller installations; a single controller may have either an even or an odd TR level selected. The TR number is assigned by SW1-1 thru SW1-4 on the Bus Interface board as shown in the table below. See Figure 3-4 for the location of SW1 on the Interface PCBA.

TR		SW1-4	SW1-3	SW1-2	SW1-1
4	-	O	C	O	O
5	-	O	C	O	C
6	-	O	C	C	O
7	-	O	C	C	C
8	-	C	O	O	O
9	-	C	O	O	C
10	-	C	O	C	O
11	-	C	O	C	C

3.5.3 SBI Interrupt Request Level

The one or two MBA controllers are assigned interrupt request levels by means of SW1-5 and SW1-6 on the Bus Interface board. Normally level 5 should be used.

Level		SW1-6	SW1-5
4	-	O	O
5	-	O	C
6	-	C	O
7	-	C	C

3.5.4 Bus Translator Board

Revsion C of the Bus Translator Board differs from previous revisions of the board in that it contains a switch which allows two new features to be selected. The revision level of the board is printed on the solder side of the board near the part number, on the left side. Revision C includes a DIP 'piano' switch (SW1), located at the edge of the board. This switch may be accessed without removing the PCBA from the chassis. The paragraphs below describe the switch-selectable features.

3.5.4.1 Early Transfer Request

Revision C of the Bus Translator Board provides early Transfer Request (TR) arbitration for the controllers in slots 3 and 4. This feature will assert the V-MASTER's TR level 800 nanoseconds prior to the issuance of an SBI command. The early TR assertion prevents any NEXUS with an arbitration level which is lower in priority than the V-MASTER from using the bus. If after the V-MASTER's assertion, no other NEXUS with a higher arbitration level requests the bus, the V-MASTER will use the bus for its Data Transfer. Since the CPU is always set for the lowest arbitration level (TR15), a small amount of processing time will be lost when this feature is enabled. The amount of time lost will be relative to the type of memory controller installed on the system and the intensity of CPU or I/O processing. Users may want to run a benchmark test to determine if use of this feature is desirable with their system. An early TR arbitration may be useful to users of disk drives with high transfer rates (i.e., the Fujitsu 2351A Eagle when set for 48 sectors per track). This feature may be enabled for the controller in slot 3 by setting switch SW1-1 ON (closed), and for the controller in slot 4 by setting switch SW1-2 ON (closed).

3.5.4.2 Continuous Clock Generation

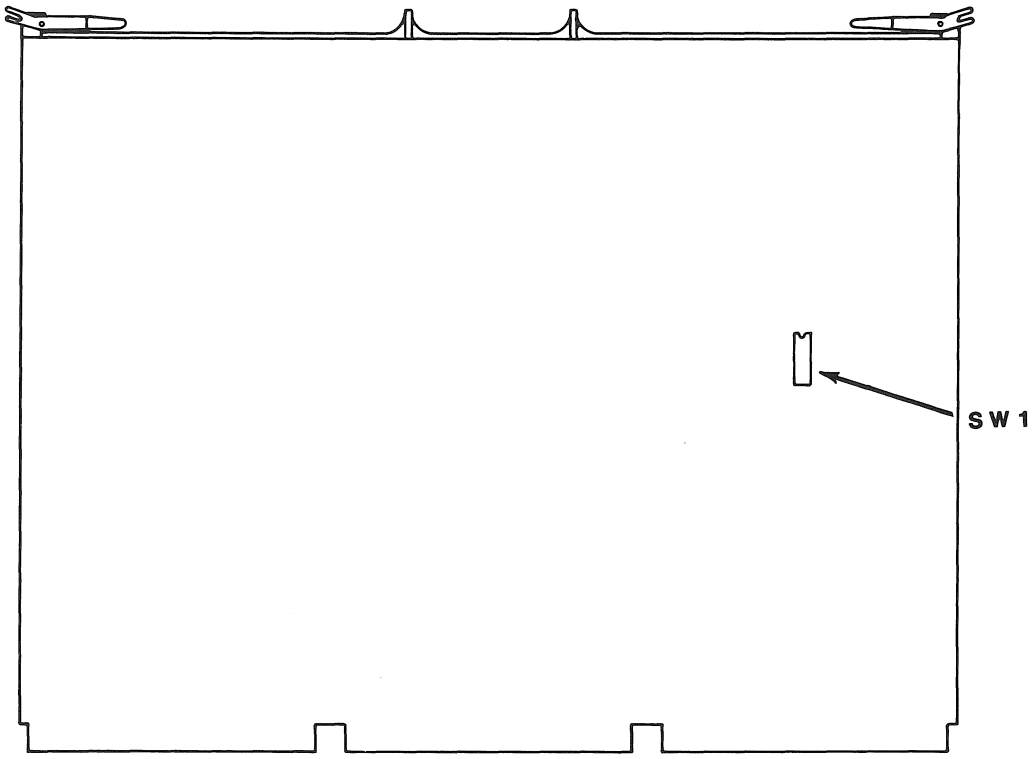
Revision C of the Bus Translator Board provides for continuous clock generation for both controllers. Enabling this feature causes the Fualt LED to remain OFF during a system boot or the running of micro-diagnostics. This feature is enabled by setting switch SW1-3 OFF (open). When SW1-3 is ON (closed), the controllers will not have continuous clock generation, and the Fault LED will blink during a system boot or the running of micro-diagnostics.

3.5.4 PCBA Installation

Reinstall the Interface PCBA in slot 1 (rightmost, as viewed from the front) of the V-MASTER chassis. (The Translator PCBA is installed in slot 2.) The components of the board should be oriented in the same direction as the other modules in the VAX cabinet. Be sure that the board is properly positioned in the throat of the backplane connectors before attempting to seat the board by means of the extractor handles.

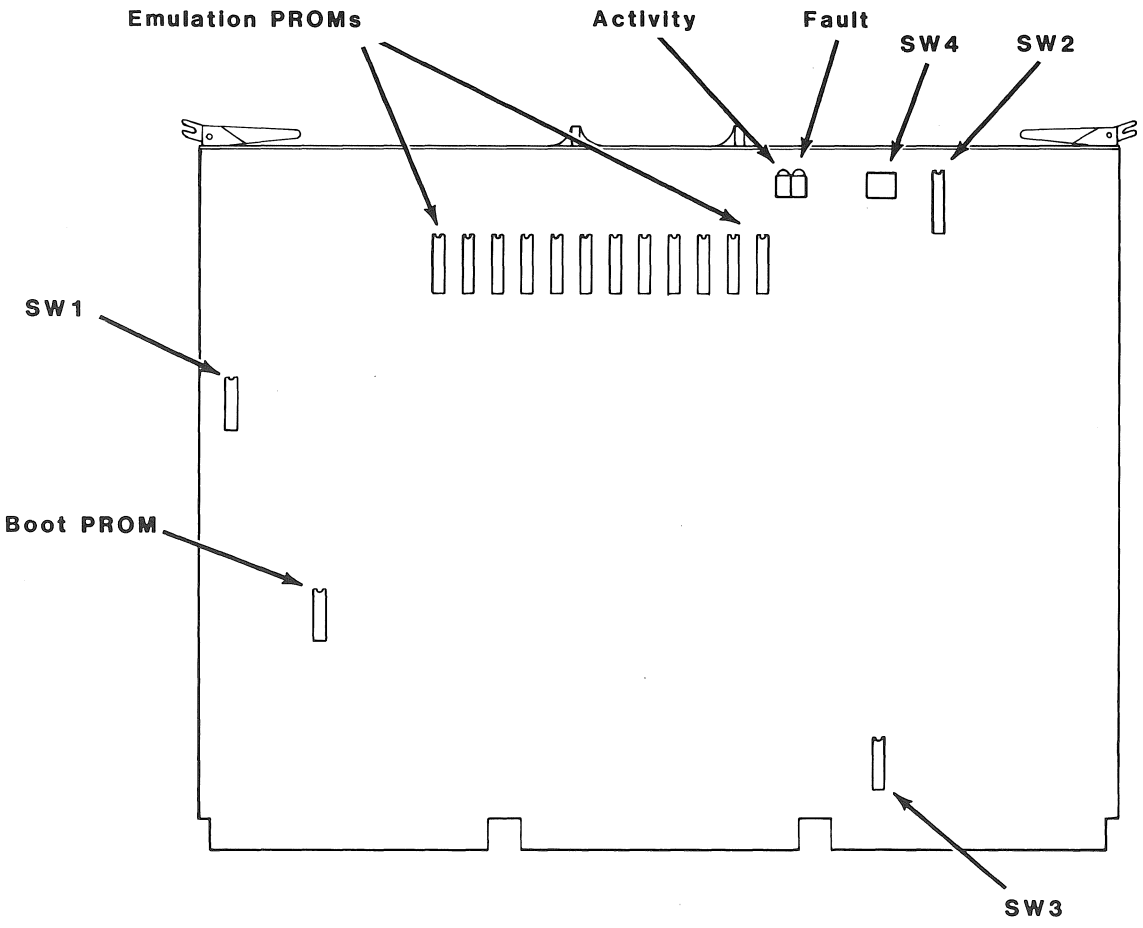
3.6 SC780 CONTROLLER SETUP

One or two SC780 controller PCBAs may be plugged into the VMI bus created by the Interface and Translator PCBAs of the V-MASTER/780 assembly. The controllers need to be configured for the particular application. The paragraphs below contain the configuration procedures. Refer to Figure 3-5 for switch locations on the SC780 PCBA.



SC7801-0071

Figure 3-4. Bus Interface Board Assembly



SC7801-0072

Figure 3-5. SC780 Controller Assembly

3.6.1 PCBA Removal

Remove the SC780 Controller PCBA(s) (SC7510401) from the V-MASTER chassis to gain access to the DIP switches required to configure the subsystem.

3.6.2 Controller Address

The controller address is selected with respect to the V-MASTER slot in which it is installed. SW3-8 is used to make the selection. See the switch setting table in paragraph 3.6.3, below. For single controller installations, slot number 3 should be used to facilitate cable paddle board installation.

3.6.3 Arbitration Level

The controller must be assigned VMI arbitration level 2 or 1 depending on whether it is in slot 3 (right controller slot) or slot 4 (left controller slot) in the V-MASTER/780. The SC780 controller may be used in either controller slot of the card cage. However, it is recommended that, in a single controller installation, the controller be placed in slot 3. This allows the mounting hardware supplied with the cable paddle board to be used. THIS SETTING IS NOT RELATED TO THE SBI ARBITRATION LEVEL DESCRIBED IN PARAGRAPH 3.5.2, ABOVE. These switch settings are made on the controller board as follows:

	SW3-						
Cont.	1	2	3	4	5	6	7	8
Slot 3 (R) - C	O	C	O	O	O	O	O
Slot 4 (L) - C	O	O	C	C	O	O	C

3.6.4 Drive Configuration

The phrase "drive configuration selection" describes the process that is used to select the logical disk drives that will be emulated by the SC780 using a given set of physical disk drives. That is, you have a particular set of physical disk drives. Using those disk drives and the SC780, you wish to emulate a specific type and arrangement of DEC subsystems. (The emulated subsystem is referred to as a logical disk drive.) Setting SW2-1 through SW2-5 on the controller allows you to select the logical disk drive configuration (limited by the physical disk drives available).

For ease of manual maintenance, the configuration table and instructions for its use are both contained in Appendix A.

3.6.5 Index and Sector Pulse Selection

The SC780 controller is designed to receive the Index and Sector signals on the B cable from each physical drive. The signals are necessary for proper operation of the sector counters associated with each drive. The RM emulation requires an updated sector counter which can be read by the VAX-11/780. Failure to have a valid sector counter may cause incorrect operation of the rotational position sensing software.

It is possible to operate with the index and sector signals on the A cable by placing switch SW1-8 (located on the SC780) in the ON position. This feature is useful for initial evaluation of the controller with a disk drive that only provides the sector and index signals on the A cable. However, when operating in this manner there is a substantial loss of capabilities and performance including: the Search command operates as a Seek; the sector counter in RMLA will be incorrect; and each transfer must wait for an index pulse to sync-up the sector counter. Also, some of the lower level diagnostics will produce some errors. Emulex strongly recommends modifying the drive to place sector and index signals on the B cable if the drive is not delivered in that configuration.

3.6.6 Option Switches

There are a number of SC780 options that can be selected by the user.

3.6.6.1 Dual Access Mode

In order to provide compatibility with VMS when it is configured for dual access, the dual access mode is provided (SW4-4 ON). This mode should only be selected when the disk drive has dual ports and is configured for dual port operation.

See paragraph 2.6.7 for programming information.

3.6.6.2 Dual Port Mode

dual port mode is selected by setting SW1-6 ON. This option should only be selected when used in conjunction with a properly written dual port driver. See paragraph 2.6. In addition, this mode should only be selected when the disk drive has dual ports and is configured for dual port operation.

3.6.7 PCBA Installation

The SC780 Controller PCBA can be reinstalled in either controller slot 3 or 4 as described in paragraphs 3.6.2 and 3.6.3, above. The components of the board should be oriented in the same direction as the other modules in the VAX cabinet. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the backplane connectors before attempting to seat the board by means of the extractor handles.

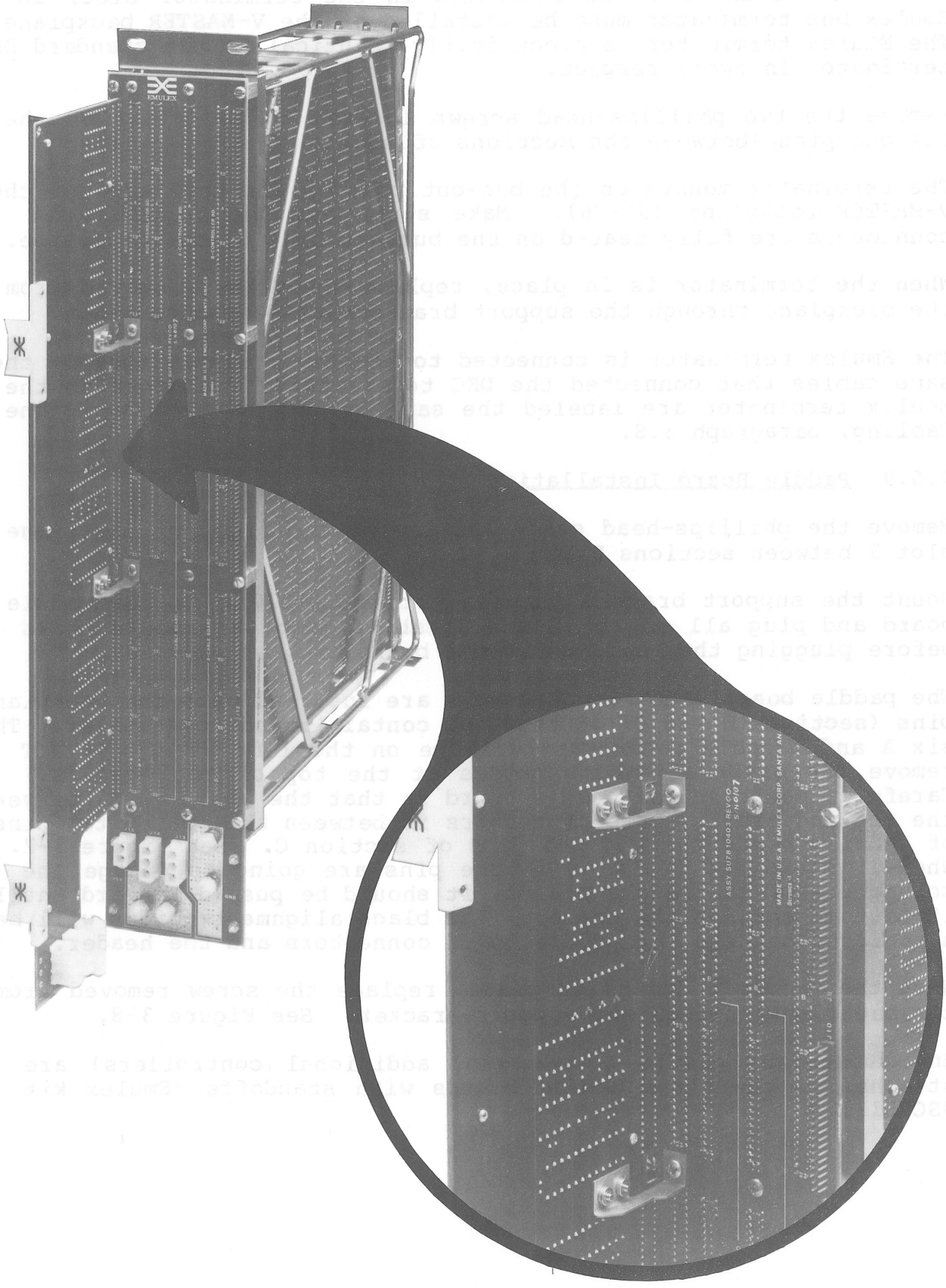


Figure 3-6 Emulex Terminator Mounting

SC7801-0073

3.6.8 Installing the Emulex Bus Terminator

If the V-MASTER is to be installed in the terminator slot, an Emulex bus terminator must be installed on the V-MASTER backplane. The Emulex terminator is electrically identical to the standard DEC terminator in every respect.

Remove the two phillips-head screws located to the right of the bus-out pins (between the sections of slot 1).

The terminator mounts on the bus-out pins on the left edge of the V-MASTER backplane (J1-J6). Make sure that the terminator's connectors are fully seated on the bus-out pins of the backplane.

When the terminator is in place, replace the screws removed from the backplane through the support brackets. See Figure 3-6.

The Emulex terminator is connected to the power supply(ies) by the same cables that connected the DEC terminator. The jacks on the Emulex terminator are labeled the same as DEC's. See Backplane Cabling, paragraph 3.8.

3.6.9 Paddle Board Installation

Remove the phillips-head screw located to the right of backplane slot 3 between sections B and C.

Mount the support bracket (Emulex kit #SC7513101) on the paddle board and plug all of the A and B cables into the paddle board before plugging the board on to the backplane.

The paddle board's three connectors are inserted onto the backplane pins (sections B and C) of the slot containing the controller. The six A and B cable connectors will be on the left side. Do NOT remove the black alignment guides at the top of the headers. Carefully position the paddle board so that the white guide between the top and middle board connectors is between the bottom two pins of section B and the top two pins of section C. See Figure 3-7. When it looks and feels as if the pins are going to engage the connectors of the paddle boards, it should be pushed forward until it bottoms against the header. The black alignment guides will be sandwiched between the paddle board connectors and the header.

When the paddle board is in place, replace the screw removed from the backplane through the support bracket. See Figure 3-8.

Any subsequent paddle boards (for additional controllers) are attached to the first paddle boards with standoffs (Emulex kit #SC7513102).

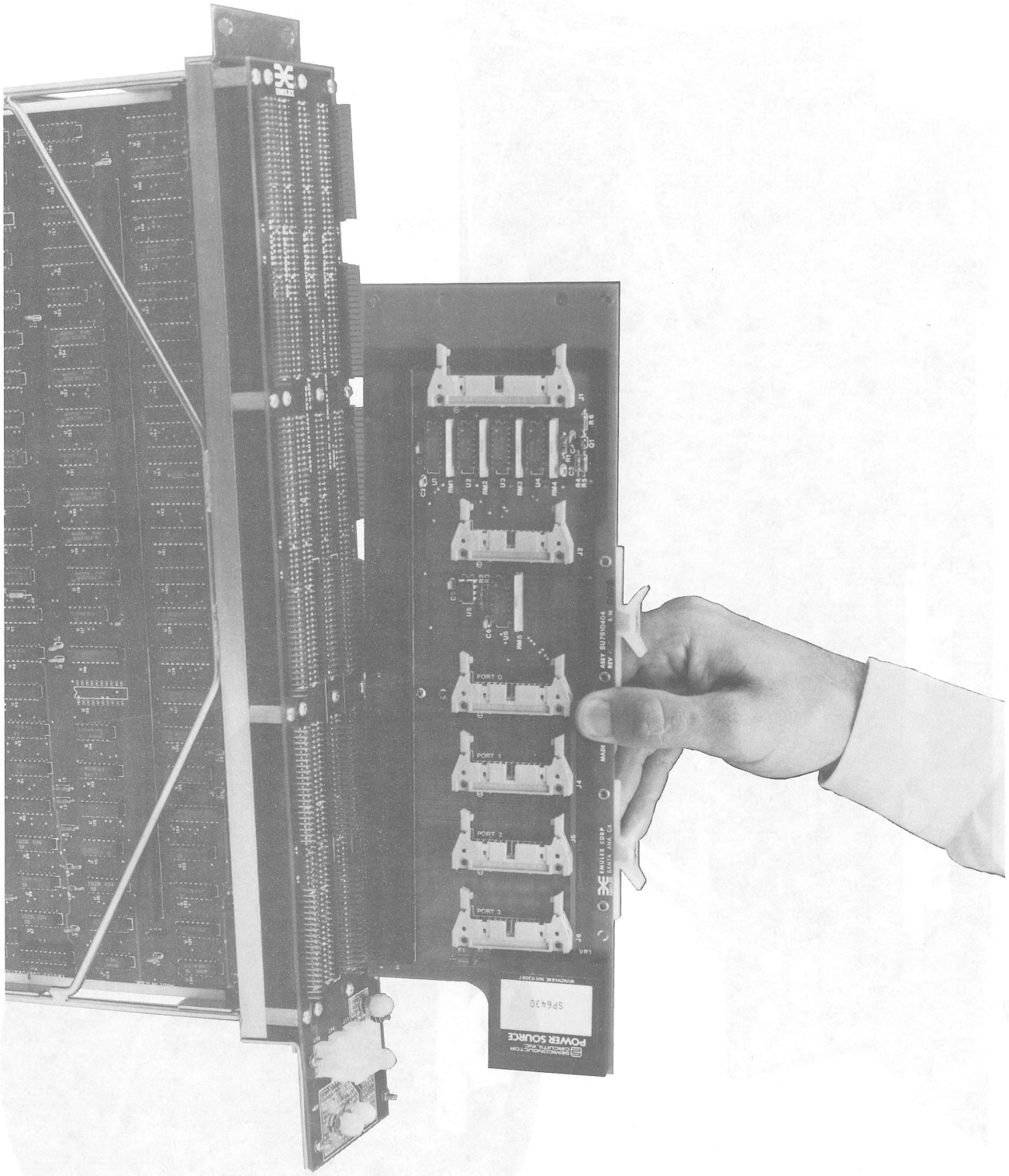


Figure 3-7 Paddle Board Installation

SC7801-0074

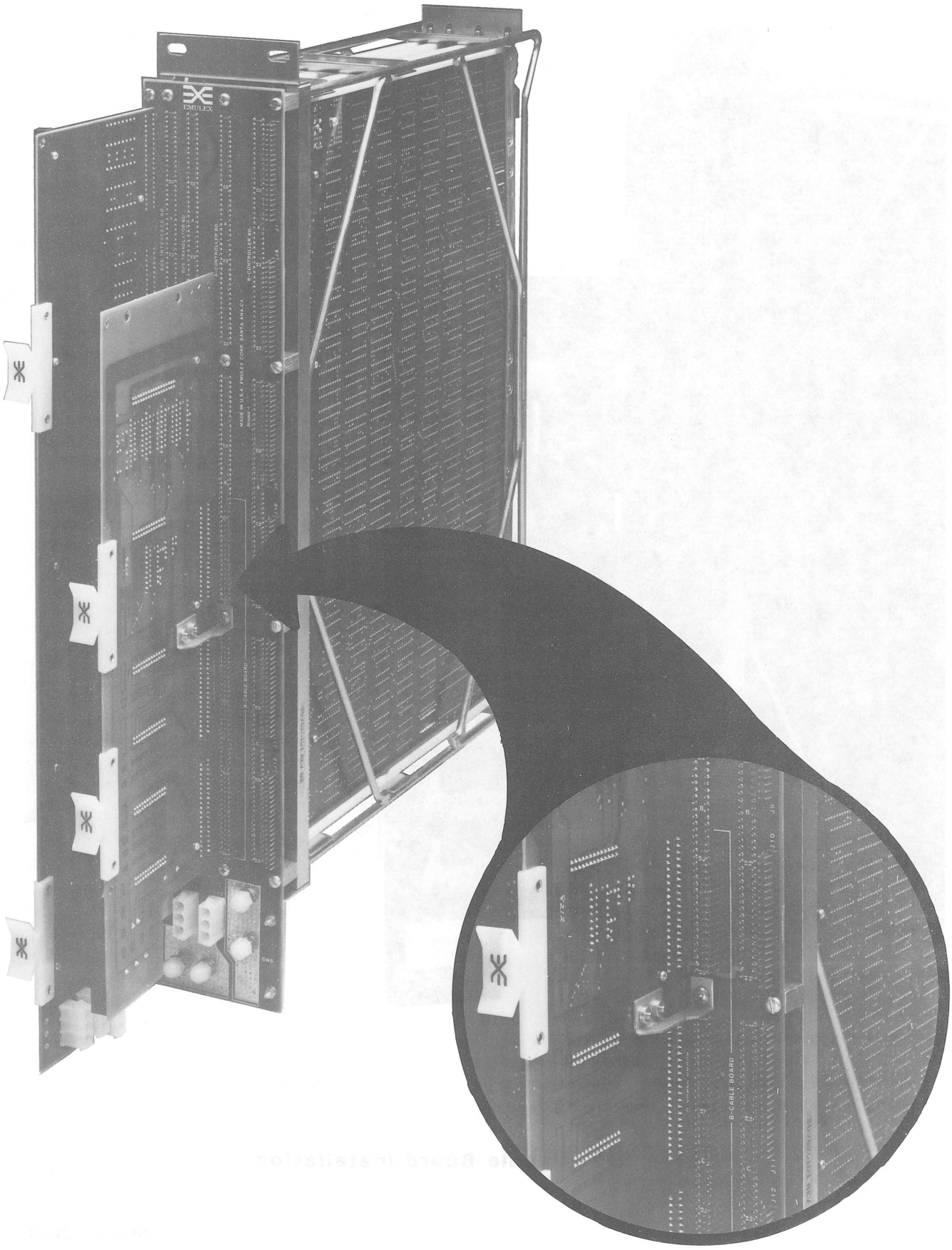


Figure 3-8 Paddle Board Mounting

SC7801-0075

3.7 V-MASTER/780 INSTALLATION

The V-MASTER may be installed in one of two locations in the VAX-11/780 CPU cabinet.

The most common VAX configuration as delivered by DEC leaves an open MBA slot in between MBA 0 and the bus terminator assembly (see Figure 3-9). That is the installation that will be described in detail here.

If that slot is not available, however, the V-MASTER may be installed in the slot occupied by the standard DEC bus terminator. The DEC terminator is replaced by an Emulex equivalent that attaches to the V-MASTER's backplane. This installation also requires an additional power supply.

3.7.1 V-MASTER Installations in MBA Slot 1

3.7.1.1 Preparing the CPU Cabinet

Remove the empty DEC MBA chassis from MBA slot 1. This is done by unplugging the coaxial SBI bus cables that link the chassis to the bus and disconnecting all power supply cables that connect to the chassis. Leave the cables connected to the power supply as they will be used to connect the V-MASTER to the supply. Remove the four phillips-head screws that hold the chassis in place (two upper back and two lower front) and slide the chassis backwards out of the cabinet. Save the screws.

3.7.1.2 Installing the V-MASTER

From the back of the CPU cabinet, slide the V-MASTER into place. Secure it using the four screws removed when the DEC MBA dummy was taken out. See paragraph 3.8 for cabling instructions.

3.7.2 V-MASTER Installations in the Bus Terminator Slot

If there are no unused slots in the CPU cabinet, the V-MASTER may be installed in the DEC terminator slot and an Emulex SBI terminator installed, see paragraph 3.6.8. An additional power supply is required.

3.7.2.1 Preparing the CPU

Remove the DEC SBI terminator from the CPU cabinet. The terminator is unfastened and removed in the same way that the dummy MBA chassis is removed. See paragraph 3.7.1.1, above.

3.7.2.2 Installing the V-MASTER

The V-MASTER is then installed in the bus terminator slot in the same manner as it would be in MBA slot 1. See paragraph 3.8 for cabling instructions.

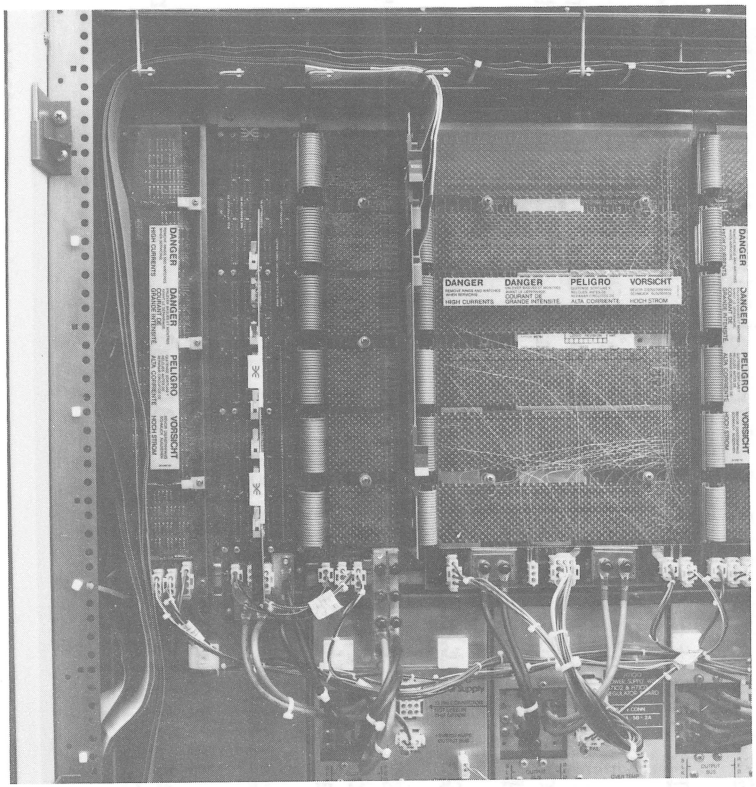


Figure 3-9 Single V-MASTER Installation

SC7801-0076

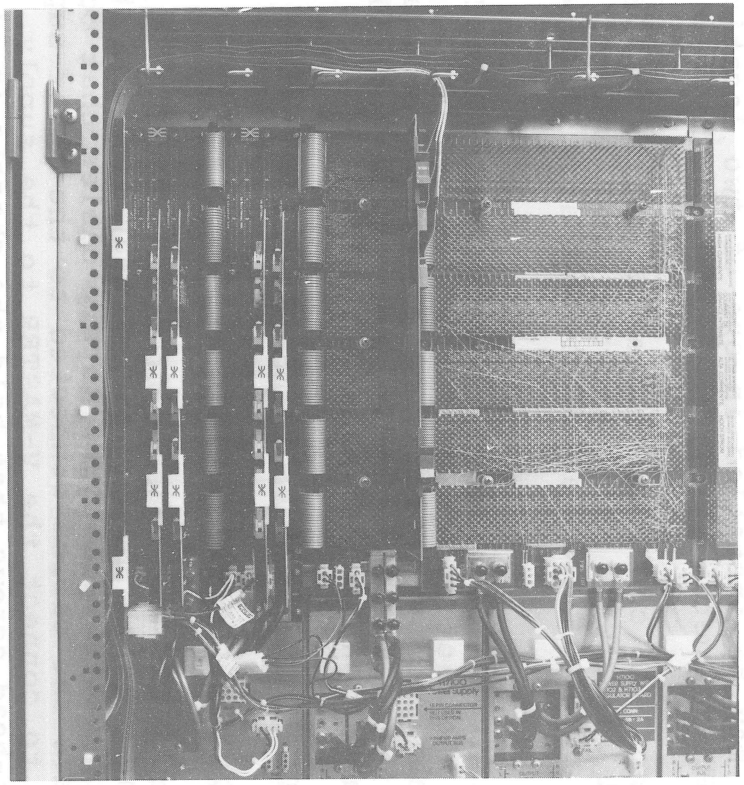


Figure 3-10 Dual V-MASTER Installation

SC7801-0077

3.7.2.3 Installing the Additional Power Supply

Installation of an additional power supply is straightforward. The dummy power supply at the far left end of the CPU cabinet (as viewed from behind) is removed by releasing the clasp (rear, center bottom) by moving it to the right, unscrewing the single phillips-head screw (front, center top), and then sliding the dummy out the front of the cabinet.

The power supply is installed by reversing the steps taken to remove the dummy. See paragraph 3.8 for cabling instructions.

A choice of two different power supplies are available from Emulex. To ensure that you have the correct type, check the version number of the power supply. Version -01 denotes a 125V power supply and version -02 denotes a 220V power supply. The version number follows the part number, which is located on the back side of the power supply near the Emulex logo. (Connectors J3 through J7 are located on the back side).

3.8 BACKPLANE CABLING

When reading each of the following paragraphs, refer to the Backplane Cabling Schematic, Figure 3-11.

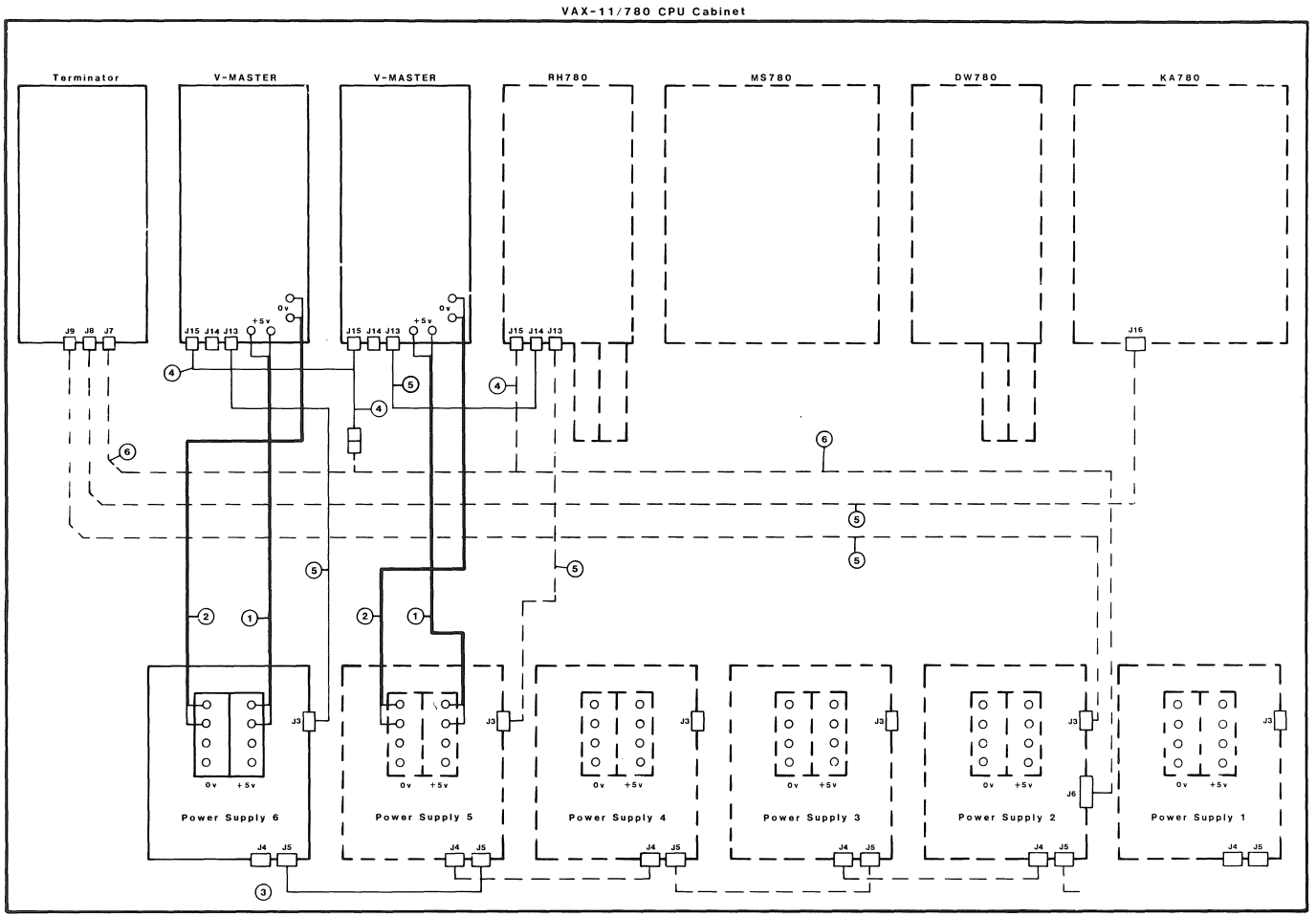
3.8.1 +5 vDC Power Cables

Each V-MASTER is connected to the appropriate power supply by four eight-gauge cables, two for +5v side of the supply and two for the ground side of the supply. The +5v cables (red) are run from the studs on the backplane to the +5v side of the power supply where they are attached using #10 machine screws. The screws should be in place on the supply; however, spare screws are supplied with the V-MASTER should they be missing. The black ground cables are connected in the same way between the GND studs on the backplane to the ground side of the power supply.

3.8.2 -5.2 vDC Cable

The -5.2 cable originates at J6 of power supply two and supplies J15 of the V-MASTER or RH780 from a connector (blue and black wires) in the area of the RH780. The connector plugs into J15 of the V-MASTER or RH780. A jumper cable (Emulex #SU78l1206) is included with the V-MASTER to allow a single connector to service two Massbus Adaptors.

A combined -5.2/+5 vDC cable terminates at J7 of the SBI terminator.



Legend

No.	Description	Color
1	+5vDC	Red
2	0vDC	Black
3	Over Temp	Grey/White
4	-5.2vDC	Blue/Black
5	AC/DC Low	Yellow/Violet/Black
6	-5.2/5 vDC	Red/Black/Blue/Black

——— DEC Harness and Hardware

——— Emulex Harness and Hardware

SC7801-0078

Figure 3-11. Backplane Cabling Schematic

3.8.3 AC/DC Low Cables

The AC/DC Low cable originates at J3 of the power supply for that Massbus Adaptor. It terminates at J13 on the adaptor backplane. If more than one adaptor is serviced by the power supply, the second adaptor receives its AC/DC Low signal via a jumper from J14 of the first adaptor to J13 of the second adaptor.

A second set of two AC/DC Low cables form a loop that originates at J3 of power supply number two, connects directly to J9 of the SBI Terminator, and then returns from J8 of the Terminator to J16 of the DEC KA780 CPU modual backplane.

3.8.4 Coaxial SBI Bus Cables

Each chassis in the CPU cabinet is linked together by the six coaxial cables that carry the SBI.

The cables originate at J1 through J6 on the left edge of each chassis and terminate at J7 through J12 on the right edge of the succeeding chassis. The header for each SBI cable is self-aligning to insure that no pins are bent when the header is installed. As part of this feature, however, the header will allow a pair of pins to be open above or below the header, and it will allow an entire row to the left or right of the header to be missed.

After pressing home each header and before powering up the system, carefully inspect each header with a flashlight to insure that it is properly installed.

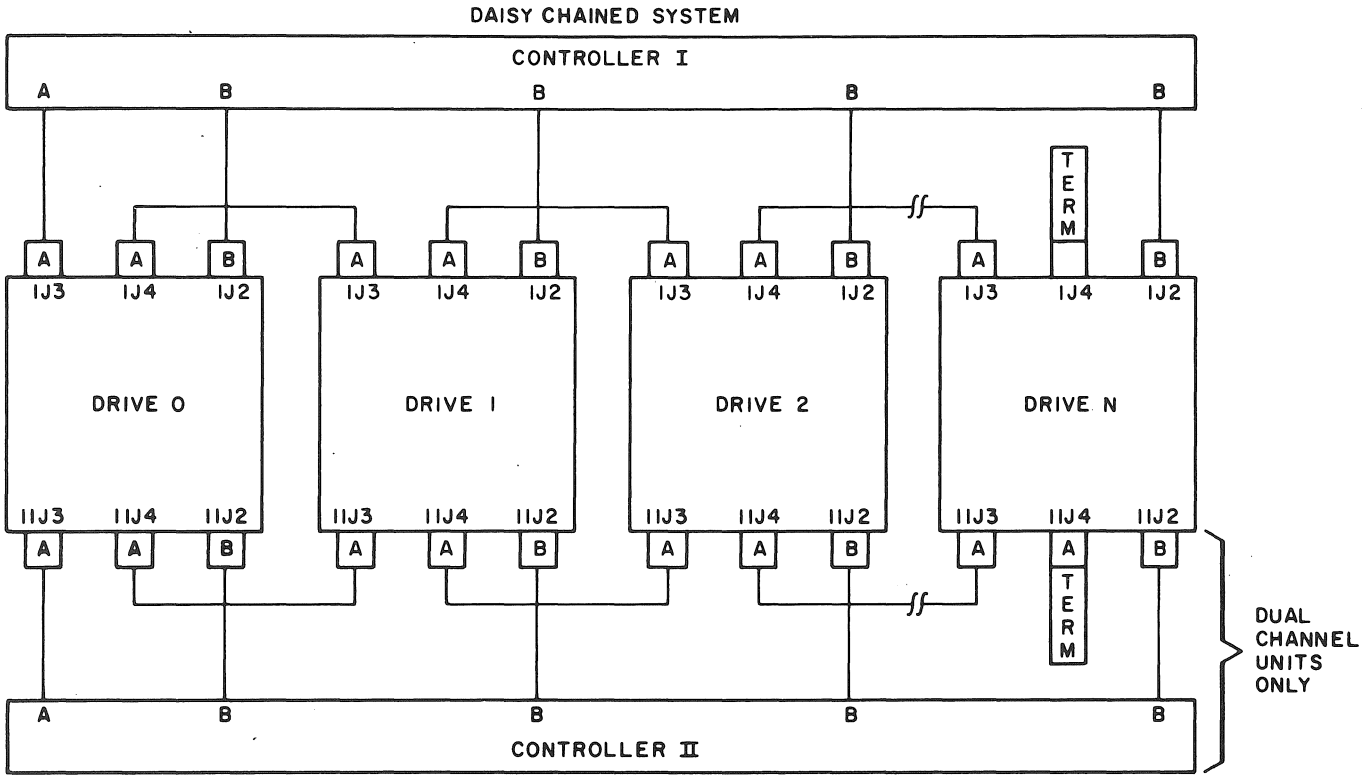
3.9 DRIVE CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-12.

3.9.1 A Cable

Route the A cable from the drive nearest the CPU through the opening in the lower right-hand corner (below the I/O panel) of the cabinet back. From the opening in the cabinet run the cable up and over the cable rack into the space behind the backplane. The paddle board end of the 60-wire A cable is divided into two connectors. They should be plugged into their connectors on the paddle board before the paddle board is installed on the backplane. Align the plugs and jacks by matching the triangles molded into both connectors.

If more than one drive is used, the A cable is daisy-chained from the first drive to the other drives. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors



NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

SC7801-0000

Figure 3-12. Drive Cabling Schematic

in the terminator. Pin one of the drive connector is on the left. Pin one of the cable connector has a notch on the connector body to identify it.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.9.2 B Cable

Route a B cable from each drive to the CPU through the opening in the lower right-hand corner (below the I/O panel) of the cabinet. From the opening in the cabinet run the cables up and over the cable rack into the space behind the backplane. The 26-wire B cables should be plugged into their connectors on the paddle board before the paddle board is installed on the backplane. It makes no difference which B port connection is used by a drive. Aline the plugs and jacks by matching the triangles molded into both connectors.

At the drive end of the B cable, pin one of the cable connector has a notch on the connector body to identify it. Pin one of the drive connector is on the left. No external terminators are used with the B cable.

NOTE: Observe the same caution on connector reversal given in paragraph 3.9.1.

3.9.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.10 TESTING

3.10.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. If the self-test has been executed successfully, the Fault LED on the top edge of the controller board will be OFF or flashing. The Fault LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the A and B cables are not properly plugged in, a drive is powered-up without a code plug, or two drives have an identical code plug. If the Fault LED is ON steadily, the controller did not pass its self-test and cannot be addressed from the CPU. The self-test will fail if the paddle board is not properly installed.

3.10.2 Register Examination

Before formatting the disk or running diagnostics, a quick check should be made to ensure that the controller registers can be read from the CPU console. Power up the CPU. When the CPU has loaded the WCS from its floppy disk drive, LOAD DONE will be printed at the console and a >>> prompt will be issued. The console is then in the console I/O mode. Check the Fault indicators on the SC780s. If they are not ON steadily, examine the first controller's first MBA register. For TR10 this can be done by typing:

```
>>> E/L/P 20014000<cr>
```

Use 20012000 for TR9 or 20016000 for TR11. If the controller can not be accessed at the base address, the console will return an invalid response, otherwise it will return 00000020 which is the contents of the first MBA register.

Both the data path between the SBI and the controller and the controller's firmware can also be verified by loading a word (4 hex digits) into the Byte Count Register (base address + 10_h). When the register is subsequently examined, the firmware should have copied the word deposited into the lower half of the longword register into the upper half. Various combinations of digits should be exercised to insure that the data is deposited correctly.

If the controller fails any of the above checks (self-test, register deposit/examination, see the Troubleshooting Guide, Appendix E.

3.10.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and zero data in all sectors of the disk. This format does not verify the data or headers nor does it write a Bad Sector File on the last track of the last cylinder.

The console should already be in the console I/O mode as described in paragraph 3.10.2 (indicated by the >>> prompt). If it is not, type CNTL P to place the console in that mode.

In determining the drive's register addresses remember that the base address for the first drive on TR8 is 20010400, on TR9 it is 20012400 and on TR10 it is 20014400. Add 80_{16} for each drive after the first.

If the drive is on-line and there are no drive errors, the formatting is carried out as follows (the addresses in the example are those of drive zero on TR10, <cr> indicates a carriage return, place spaces as indicated):

1. Deposit 0001 in MBACR (MBA base address + 4) to initialize the V-MASTER:

   >>>D/L/P 20014004 0001<cr>

2. Deposit 0009 in RMCS1 (drive base address) to clear the drive:

   >>>D/L/P 20014400 0009<cr>

3. Deposit 0013 (Pack Acknowledge command) in RMCS1 (drive base address):

   >>>D/L/P 20014400 0013<cr>

4. Examine RMDS (drive base address + 4) to check drive status:

   >>>E/L/P 20014404<cr>

The console should print out:

P 20014404 000011C0

This response indicates that the medium is on-line, the drive is present and ready, and the volume is valid.

5. Deposit FFFF (enables optional Format command) in RMHR (drive base address + 2C):

>>> D/L/P 2001442C FFFF<cr>

6. Deposit 003F (Format command) in RMCS1 (drive base address):

>>> D/W/P 20014400 003F<cr>

The Activity LED will flash as long as the formatting is underway.

7. When the Activity LED stops flashing, examine RMDS (drive base + 4) to see if ERR (bit 14) is set indicating an error:

>>> E/L/P 20014404<cr>

If there has been no error, the register will contain 15C0. If there is an error resulting from the format operation, RMER1 and RMER2 should be examined to determine the cause of the error, and RMDA and RMDC should be examined to see how far the formatting progressed.

The time to format the disk is as follows: RM03 - 1.8 min., RM05 - 5.5 min. and RM80 - 4.5 min.

3.10.4 DEC Diagnostics

The controller will execute the DEC diagnostics as indicated below if the drive is a standard RM03, RM05 or RM80 size. Consult Appendix C for more detailed information on operation of the DEC disk diagnostics listed below which are applicable to the SC780.

ESCAA - VAX-11/780 RH780 Diagnostic

This program tests only the RH780 portion of the SC780 controller. Most of the test is executed with the controller in diagnostic mode which allows for simulation of an attached Massbus. Since the SC780 has no Massbus, it does not simulate one and therefore only tests 1-3, 5-6 and 11 run without errors. Test 11 requires drive 0 to be on line.

EVRDA - RM03/5 RM80 Diskless Diagnostic

This program tests the drive portion of the controller's logic.

No data transfers are performed. A portion of this program uses the diagnostic mode of the DEC drives. The diagnostic mode is not fully implemented in the SC780 controller. Consequently, with the drive cycled down only tests 1-23 will run without errors.

EVRAC - Disk Formatter

This program will format RM03 and RM05 type drives. A different format program is used for RM80s.

EVRDB - RM03/5 Functional

This program does simple operations, including data transfers, with an attached RM03 or RM05 type drive.

EVRGA - RM80 Formatter

This program does the formatting of the RM80 type drives.

EVRGB - RM80 Functional Diagnostic

This program does simple operations, including data transfers, with an attached RM80 type drive.

EVRAA - VAX RP/RK/RM/RX/TU58 Reliability

This program is a general purpose data reliability test program which will handle the RM drives.

There are 32 device registers for each of the drives, plus seven Massbus Adaptor (MBA) registers in the SC780/B controller. The registers are used to interface the controller to the drives and the CPU. The registers are loaded and/or read under program control in order to initiate drive commands, set-up for DMA data transfers, and monitor status and error conditions. The MBA registers and the 32 drive registers are read and written as long words. The drive registers return the upper half of MBASR in bits <31:16> when read.

In addition there are 256 map registers which control the virtual to physical mapping for DMA transfers.

This section shows the format of each of the registers and explains the use and the meaning of each of the bits. The addresses for the registers are for the first MBA and drive 0, and they are given as hexadecimal offsets from the base address. See Appendix E for the base address as it relates to TR level and for offsets for additional MBAs and drives.

4.1 MBA CONFIGURATION/STATUS REGISTER (MBACSR) base address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PE	WDS	URD	0	MT	XF	0	0	PD	PU	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

SBI Parity Error (PE) - Bit 31

This bit is set when an SBI parity error is detected. Cleared by power fail or the deassertion of the fault signal. Setting of this bit will cause fault to be asserted on the SBI.

Write Data Sequence (WDS) - Bit 30

This bit is set when no write data is received following a write command. Cleared by power fail or the deassertion of the fault signal. The setting of this bit will cause the assertion of fault on the SBI.

Unexpected Read Data (URD) - Bit 29

This bit is set when read data is received when it is not expected. Cleared by power fail or the deassertion of the fault signal. The setting of this bit will cause assertion of the the fault signal on the SBI.

Multiple Transmitter (MT) - Bit 27

This bit is set when the ID on the SBI does not compare with the ID transmitted by the MBA during that write cycle. Cleared by power fail or the deassertion of fault signal. The setting of this bit will cause the assertion of fault on the SBI.

Transmit Fault (XF) - Bit 26

This bit is set when SBI fault is detected and the controller is transmitting information on the bus. Cleared by power fail or the deassertion of the fault signal.

Controller Power Down (PD) - Bit 23

This bit is set when the controller receives assertion of AC LO. Cleared when the controller power goes on. Cleared by assertion of INIT, UNJAM, DC LO or writing one to the bit. The setting of this bit will cause an interrupt to the CPU if IE is set.

Controller Power Up (PU) - Bit 22

This bit is set when the controller receives the deassertion of AC LO. Reset when the power goes down. Cleared by INIT, UNJAM, DC LO or writing a one to this bit. The setting of this bit will set IE bit in MBACR and interrupt the CPU.

Adaptor Code - Bits <07:00>

Each type of adaptor is assigned a unique code to identify it. The MBA code is 00100000.

4.2 MBA CONTROL REGISTER (MBACR) base address + 4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	MMM	IE	ABT	INIT

This register provides four control bits for the MBA functions of the controller. All bits are cleared by INIT.

MBA Maintenance Mode (MMM) - Bit 03

Setting this bit puts the controller in the maintenance mode, which will allow the diagnostic programmer to exercise and examine the

controller registers. The controller can not be put in maintenance mode while a data transfer is in progress. The maintenance mode is only partially emulated.

Interrupt Enable (IE) - Bit 02

When this bit is set the controller can interrupt the CPU when certain conditions occur. Cleared by writing a zero, by INIT or UNJAM.

Abort (ABT) - Bit 01

Setting this bit will initiate the data transfer abort sequence which will stop the data transfer and interrupt the CPU if the IE bit is set.

Initialize (INIT) - Bit 00

Setting this bit will clear the controller including any pending commands, abort any data transfer, and clear registers as well as this bit. See paragraph 2.5.1.

4.3 MBA STATUS REGISTER (MBASR) base address + 8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	NRC	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	EC	RDS	ITO	RTO

Data Transfer Busy (DTB) - Bit 31

This bit is set when a data transfer command is received. It is cleared when the data transfer is terminated normally or when it is aborted. This is a read-only bit.

No Response Confirmation (NRC) - Bit 30

This bit is set when the controller receives a no response confirmation for the command or write data sent on the SBI. It is cleared by writing a one to the bit or INIT. The setting of this bit will cause retry of the command.

Corrected Read Data (CRD) - Bit 29

This bit is set when the data received from memory has been corrected. It is cleared by writing a one or by INIT. It is also cleared by subsequent receipt of a valid data transfer command.

Programming Error (PGE) - Bit 19

This bit is set when one or more of the following conditions exists:

1. Program tries to initiate a data transfer when the controller is currently performing one, or

2. Program tries to load MBAVAR, MBABCR or map registers when the controller is currently performing a data transfer operation, or

3. Program tries to set Maintenance Mode during a data transfer.

This bit is cleared by writing a one to it, or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will cause an interrupt to the CPU if IE is set.

Nonexistent Drive (NED) - Bit 18

This bit is set when the program addresses any drive register for a drive which does not exist. The bit is cleared by writing a one to it or by INIT. Setting this bit will send zero drive data back to the CPU and interrupt the CPU if IE is set.

Massbus Control Bus Parity Error (MCPE) - Bit 17

This bit is set when NED is set.

Attention (ATTN) - Bit 16

This bit is asserted if any of the Attention bits in RMAS are asserted indicating that a drive requires attention. Asserting this bit will cause an interrupt to the CPU if IE is set. This bit is read-only.

Data Transfer Completed (DTC) - Bit 13

This bit is set when the data transfer is terminated either due to an error or normal completion. It is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will cause an interrupt to the CPU if IE is set.

Data Transfer Aborted (DTA) - Bit 12

This bit is set when the data transfer is aborted for any reason. This bit is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will cause an interrupt to the CPU if IE is set.

Data Late (DLT) - Bit 11

Set during a read if the buffer overflows. Set during a write or write check if the buffer underflows. This bit is cleared by writing a one or by INIT. It is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Write Check Upper Error (WCU) - Bit 10

This bit is set when a compare error is detected in the upper byte while the controller is performing a write check operation. It is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Write Check Lower Error (WCL) - Bit 09

This bit is set when a compare error is detected in the lower byte while the controller is performing a write check operation. It is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Missed Transfer Error (MXE) - Bit 08

Set when an illegal command in the range 2D-3F is received. It is also set if a data transfer command is attempted with ERR set, MOL clear or VV clear. ILF in RMER1 will also be set. IVC and MXE are set if ERR is clear and either MOL or VV is clear. MXE is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Exception (EXC) - Bit 07

The exception signal indicates an error condition during a data transfer between the controller and the drive. It is cleared by writing a one or by INIT. It is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Invalid Map (IM) - Bit 04

This bit is set when the valid bit of the next frame number is zero and the byte count is not zero. It is cleared by writing a one or INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Error Confirmation (EC) - Bit 03

This bit is set when the controller receives an error confirmation for a read or write command. It is cleared by writing a one to

this bit or INIT. The setting of this bit will cause the data transfer operation to be aborted.

Read Data Substitute (RDS) - Bit 02

This bit is set when the read data received from memory is indicated to be read data substitute. It is cleared by writing a one to this bit or INIT. The setting of this bit will cause the data transfer operation to be aborted.

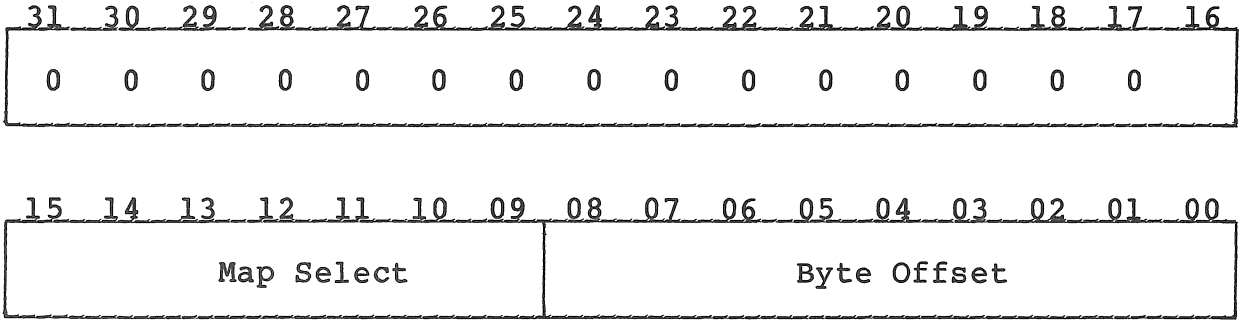
Interface Sequence Timeout (ITO) - Bit 01

This bit is set when an error confirmation is received or no response confirmation is received for 102.4 microseconds after the command is initially sent on the SBI. The setting of this bit will cause data transfer abort. Cleared by writing a one to this bit or INIT.

Read Data Timeout (RTO) - Bit 00

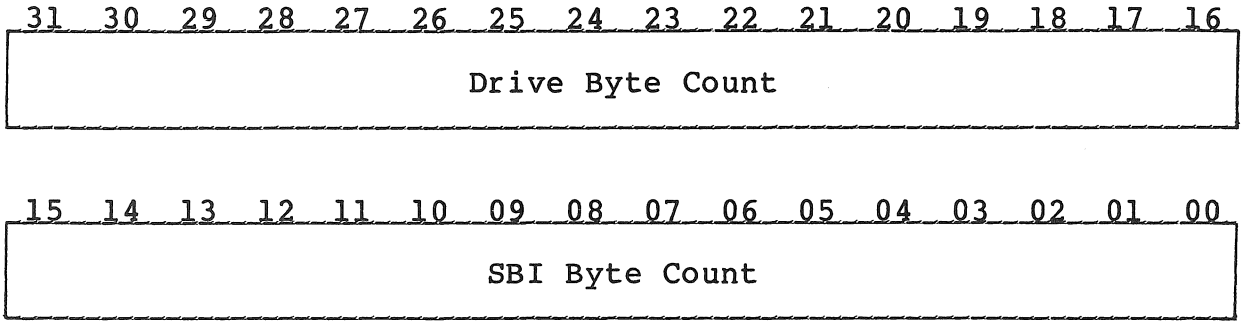
This bit is set when no read data is received in 102.4 microseconds after the command is initially sent on the SBI. The setting of this bit will cause data transfer abort. Cleared by writing a one to this bit or INIT.

4.4 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) base address + C



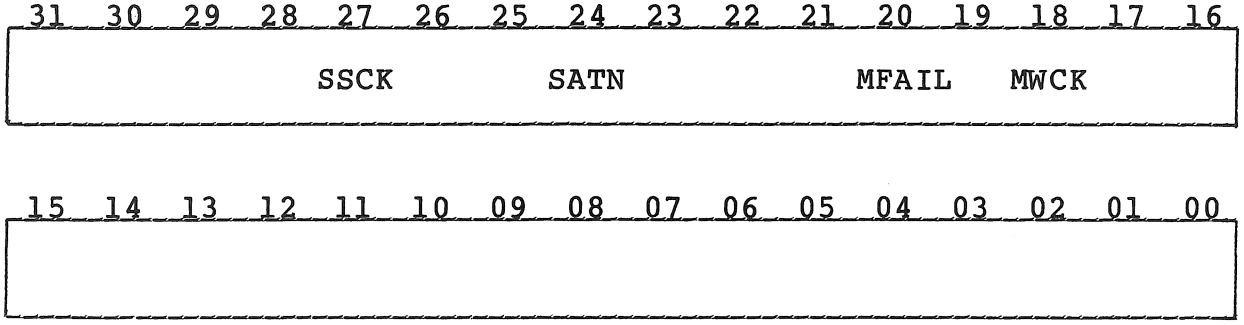
This register contains the 17-bit virtual address for the data transfer. Bits <08:00> select the byte within the page and bits <16:09> select one of the 256 map registers. The MS seven bits of the nine-bit byte offset is concatinated with the 21-bit physical page address obtained from the addressed map register to form the 28-bit physical VMI address. The virtual address is incremented by four after every memory read or write and will not point to the next byte to be transferred if the transfer does not end on a longword boundary. Also, upon a write check error, the virtual address register will not point to the failing memory address due to the preloading of the data buffer. The virtual address of the bad data may be found by determining the number of bytes actually transferred by the drive and adding the difference to the initial virtual address.

4.5 MBA BYTE COUNTER (MBABCR) base address + 10



This register contains the byte count for the number of bytes transferred to or from the drive and the number of bytes transferred to or from memory. The two transfers stop when the byte counts reach zero. The program initially loads the two's complement of the number of bytes for the data transfer into bits <15:00> of this register. The controller then loads this value into bits <31:16>.

4.6 MBA DIAGNOSTIC REGISTER (MBADR) base address + 14



This register cannot be written into unless MMM in MBACR is set. Unless explicitly written into, this register will read 'BF' for data. Cleared to a 'BF' whenever INIT is set. Only bits <31:21> are read/write. All others are read-only. Only the bits described are emulated.

Simulated SCLK (SSCK) - Bit 27

Setting this bit sets MWCK (Bit 18).

Simulated ATTN (SATN) - Bit 24

Setting this bit sets ATTN in MBASR.

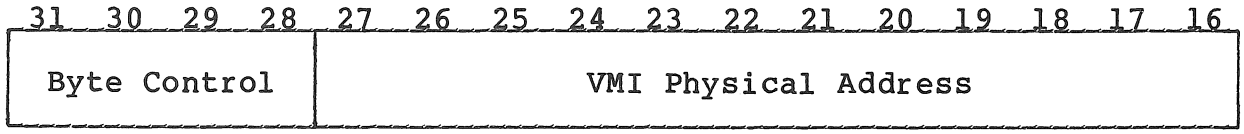
Massbus Fail (MFAIL) - Bit 20

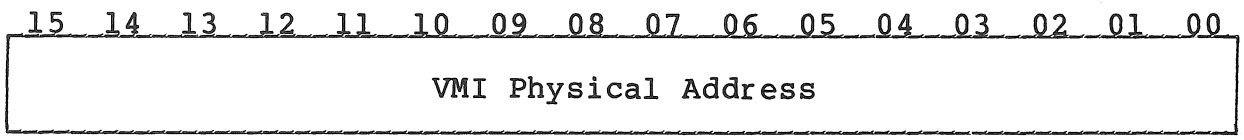
This bit is a reflection of the MMM bit in MBACR.

Maintenance Write Clock (MWCK) - Bit 18

This bit is a reflection of SSCK (Bit 27)

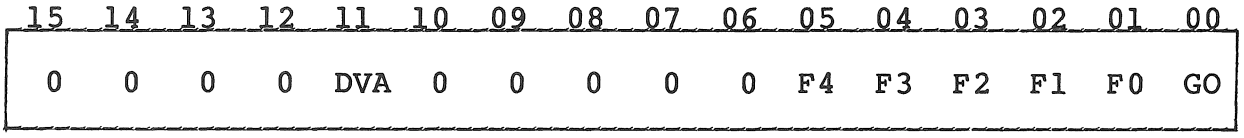
4.7 MBA COMMAND ADDRESS REGISTER (MBACAR) base address + 1C





This register is read-only and valid only when DT Busy (bit 31 of the MBA Status Register) is set. This register contains the byte controls and physical address of the last DMA operation.

4.8 CONTROL/STATUS REGISTER 1 (RMCS1) base address + 400



The RMCS1 register can be read or written by program control, and is used to store the current disk command function code. Setting the GO bit will cause the controller to recognize the function code in the register and initiate the operation for the corresponding drive. The actual start of execution of the command does not begin when the function code is loaded into the control register but commences when the controller has finished any previous operation and polls through the drive RMCS1s in search of a command needing initiation.

Drive Available (DVA) - Bit 11

This read-only bit is set when the drive is seized by the controller. When not in dual port mode, the drive is seized as long as it is powered-up.

Function Code (F4-F0) - Bits <05:01>

F4-F0 and the GO bit make up the function (command) code which determines the action to be performed by the controller and drive as shown below:

01	No Operation	29	Write Check Data
05	Seek Command	2B	Write Check Header and Data
07	Recalibrate	31	Write Data
09	Drive Clear	33	Write Header and Data
0B	Release	39	Read Data
0D	Offset Command	3B	Read Header and Data
0F	Return to Centerline	3F	Format (Optional)
11	Read-in Preset		
13	Pack Acknowledge		
19	Search Command		

GO (GO) - Bit 00

The GO bit must be set to cause the controller to respond to a command. The GO bit is reset after command termination.

4.9 DRIVE STATUS REGISTER (RMDS) base address + 404

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OFM

This register contains various status indicators for the addressed drive. The register is a read-only register.

Attention Active (ATA) - Bit 15

An attention condition will set the ATA bit in this register and in the Attention Summary Register (RMAS). It is cleared by INIT, controller clear, loading a command with the GO bit set or loading a one bit in RMAS register corresponding to the drive's unit number. The last method of clearing the ATA bit will not clear the error indicators.

An attention condition is caused by: an error in the error registers, the completion of a positioning operation, the change of state of the MOL bit, dual port operation with the drive presently available if previously not available, or correct sector identification for the Search command.

Error (ERR) - Bit 14

Set when one or more of the errors in the error registers (RMER1 or RMER2) for a selected drive is set. While ERR is asserted, commands other than Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

Set when a positioning command is accepted. These commands are: Seek, Recalibrate, and Search. Cleared when the moving function is completed at the time the DRY and ATA bits are set. For RM03/5 emulations; this bit is set when MOL is reset. Set during a mid-transfer seek during a data transfer command.

Medium On-Line (MOL) - Bit 12

Set when the unit ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the drive. Cleared when the spindle is powered down or the drive is off-line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the write-protected line from the drive is asserted as enabled by a switch located on the drive. A write command on a write-locked drive will cause the write-lock error bit (WLE, bit 11 of RMER1) to be set. For RM80 emulations, this bit is set when MOL is reset.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been read or written. Cleared when a new write to RMDA is received.

At the time LST is set, the RMDA register is reset to zero and the RMDC register increments by one to the first illegal cylinder address. If the byte count is not zero, a mid transfer seek is aborted which will cause the AOE status bit (RMER1, bit 09) to be set indicating that the desired cylinder register overflowed during a read or write.

Programmable (PGM) - Bit 09

This bit is set when dual port or dual access operation is enabled.

Drive Present (DPR) - Bit 08

This bit is set if the controller has seized the drive and is reset when the other controller has seized the drive. This bit is a reflection of the DVA bit in RMCS1.

Drive Ready (DRY) - Bit 07

Set at the completion of every command and cleared at the initiation of a command. When set, this bit indicates the readiness of the drive to accept a command. If a mechanical movement command was initiated, the ATA bit will also be set when DRY is set. This bit is the complement of the drive's GO bit.

Volume Valid (VV) - Bit 06

Set by the Pack Acknowledge or Read-in Present commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates that the drive has been off-line and a disk pack may have been changed.

Offset Mode (OFM) - Bit 00

Set by the offset command to indicate that a read will be done with the heads in the offset position as determined by RMOF, bit 07. Cleared by a Read-in Preset, Return-to-Centerline, Recalibrate or write command, or a mid-transfer seek. Also cleared whenever the drive cycles up.

4.10 ERROR REGISTER 1 (RMER1) base address + 408

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

The RMER1 register is a read/write register that is used to store the error status for the addressed drive. The RMER1 register can only be written as a word. If the program attempts to write into this register while the drive is busy, an RMR (RMER1 register, bit 02) error is set, and the contents of the register are not otherwise modified. Writing zeros into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

Data Check (DCK) - Bit 15

Set during a read operation when the ECC hardware detects an ECC error. The data transfer terminates with the current sector. If the Error Correction Inhibit (ECI) bit is off, the controller will go into the error correction process, and the DRY bit will not be set until the end of the process. If ECI bit is on, the error correction process is inhibited, and DRY is set immediately.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the unsafe and seek incomplete error conditions in the RMER2 register. With UNS set, correct results on any operation cannot be guaranteed. Some faults must be cleared by manual intervention at the drive.

Operation Incomplete (OPI) - Bit 13

Set when a read or write command involving header search cannot find the physical sector within three index pulses. Also set during a search operation where a sector count match is not made within three index pulses. In dual port mode, OPI is set when a seek, search or data transfer command is issued to a drive that is busy. When set, the GO bit is cleared and the DRY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. When DTE is set, the GO bit will be cleared and the DRY bit set. Also set if a sector pulse occurs before the end of the data field.

Write Lock Error (WLE) - Bit 11

Set when a write command is issued to a write-locked drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in RMDC or RMDA is invalid and a Seek, Search or data transfer command is initiated.

Address Overflow Error (AOE) - Bit 09

Set when the RMDC register overflows during a read or write operation indicating that the address has exceeded the cylinder address limit. With AOE set, the controller will terminate the operation when the last sector of the last cylinder has been read or written.

Header CRC Error (HCRC) - Bit 08

Set by a CRC error in the header. If a CRC error is detected during a read or write command, the controller will not make any data transfer. In the event of a CRC error during a read/write-check header and data command, the entire sector including header will be transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 07

Set when the first two words of the header read at the sector whose count is equal to the desired sector field of RMDA do not match the contents of RMDC and RMDA. If the HCE bit is set during a read or write command, the controller will not perform any data transfer. In the event of a read/write-check header and data command, the entire sector will be transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 06

Set when the error correction procedure indicates that the error was a non-correctable ECC error. DCK (bit 15) is also set.

Write Clock Fail (WCF) - Bit 05

This bit is normally a zero unless written into.

Format Error (FER) - Bit 04

Set if the FMT16 bit in RMOF does not match bit 12 in Word 1 of a sector's header. Although the controller implements both 30 and 32 sector formats, all sectors contain 256 16-bit words in either format. If FER is set, then HCE may not be set.

Massbus Parity Error (PAR) - Bit 03

This bit is normally a zero unless written into.

Register Modification Refused (RMR) - Bit 02

Set when a write is attempted to any drive register (except RMAS) with DRY equal to zero. The drive operation in progress continues.

Illegal Register (ILR) - Bit 01

This bit is set when addressing an illegal drive register. Only registers 0 to 15 are legal. The upper 16 registers are illegal.

Illegal Function (ILF) - Bit 00

Set when an illegal function code (with GO) is written into RMCS1.

4.11 MAINTENANCE REGISTER 1 (RMMR1) base address + 40C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	X	0	0	0

The maintenance mode is not emulated. Writing to RMMR1 can occur at any time regardless of the status of the drive. A drive or controller clear resets this register except for bit 03, which is set.

4.12 ATTENTION SUMMARY REGISTER (RMAS) base address + 410

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

The RMAS register allows the program to examine the attention status of all drives with only one register read operation. It also provides a means of resetting the attention logic in a selected group of drives. The eight low-order bits of this register correspond to the ATA bits in the RMDS of the drive having the same unit number as the bit position of this register.

A drive's ATA bit can be reset by loading a one into the bit position corresponding to the drive's unit number. Loading a zero has no effect. For a program to use the RMAS without losing status information, the program must use MOV instructions for all writes to this register. An instruction that does a read-restore (such as BIS) may cause bits that were asserted just prior to the read to be lost. This register can be read or written at any time. This register is replicated for every drive, and can be accessed with any drive address without causing NED errors.

A persistent error, just like any error condition, will cause the ATA bit to be reasserted. Attempts by the controller to clear the error will not work in this case.

4.13 DISK ADDRESS REGISTER (RMDA) base address + 414

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Track Address								Sector Address							

This register is used to address the sector and track on the disk which is desired for a data transfer. The RMDA is incremented each time a sector of data is transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred. At the end of a transfer, RMDA contains the address of the sector following the last one involved in data transfer.

The RMDA contains a sector counter that provides for up to 256 sectors per track. The register also contains a track counter which is incremented by one every time the sector counter overflows. When the sector address and the track address reach their maximum counts, they are reset to zero and the RMDC is incremented by one. The invalid address error (IAE, RMER1, bit 10) is set if the address in the RMDA is invalid when a data transfer, Seek, or Search function is initiated. The maximum sector and track addresses are obtained from the selected configuration.

4.14 DRIVE TYPE REGISTER (RMDT) base address + 418

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

Moving Head (MOH) - Bit 13

This bit is always a one indicating that the drive is a moving head device.

Dual Port Mode (DPM) - Bit 11

This bit signifies that the drive is operating in dual port mode as enabled by SW1-6 or dual access as enabled by SW4-4.

Drive Type Code - Bits <07:00>

This code specifies the type of drive as follows:

14 - RM03, 15 - RM02, 16 - RM80, 17 - RM05.

4.15 LOOK-AHEAD REGISTER (RMLA) base address + 41C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Sector Counter					0	0	0	0	0	0

The RMLA register contains the drive sector counter and is used to present the angular position of the disk relative to the read/write heads for the addressed drive. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays. The counter typically counts from zero to maximum sector or from zero to maximum sector minus two, depending on the status of the FMT16 bit in RMOF.

4.16 SERIAL NUMBER REGISTER (RMSN) base address + 420

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW1 -8	SW1 -7	SW1 -6	SW1 -5	SW1 -4	SW1 -3	SW1 -2	SW1 -1	Firmware Rev.				Port Number			

The purpose of the RMSN register in a DEC RM drive is to distinguish a drive from similar drives attached to the controller by means of a four decade serial number. Here it contains the controller port number to which the drive is attached, the firmware revision level, and the eight SW1 switch settings.

4.17 OFFSET REGISTER (RMOF) base address + 424

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT 16	ECI	HCI	SEI	0	OFD	0	0	0	0	0	0	0

The RMOF register contains three inhibit bits and the drive offset direction bit. The offset direction bit determines if a read will be done with the heads advanced or retarded from normal centerline position. The actual offset determination is done by the status of RMDS, bit 00. All bits of this register are cleared by Read-In Preset command.

Format Bit (FMT 16) - Bit 12

Set for 31/32 sector (16 bit) mode and reset for 30 sector (18 bit) mode. Since the controller only handles 16-bits-per-word format, this bit should always be a one. When this bit is set, an RM80 emulation operates with one less sector per track than the track contains. The extra sector is a skip sector that is used when a bad sector is found. When set, this bit typically allows for 32 sectors per track on RM03/RM05 emulations. Some configurations allow 48 sectors per track.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit header compare and CRC check. With HCI set, the controller depends only on the sector count for sector identification. It is recommended that the HCI bit be reset during a write operation.

Skip Sector Error Inhibit (SEI) - Bit 09

For RM80 emulations only. Set to inhibit skip sector errors during a header check. When this bit is set the drive operates on all sectors per track. This bit is reset whenever a data transfer command increments RMDA to a new track address. This bit cannot be set unless the FMT 16 bit is already set.

Offset Direction (OFD) - Bit 07

Set under software control to select the direction of positioner offset. A one retards the heads, and a zero advances the heads.

4.18 DESIRED CYLINDER REGISTER (RMDC) base address + 428

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	Desired Cylinder Address									

The RMDC register contains the address of the cylinder to which the positioner is to move. The RMDC register will be cleared by the Read-in Preset command. Following an initial load, the value in the RMDC register will be incremented by one whenever the RMDA register is reset to zero during a data transfer. When the RMDC register is incremented and the RMWC register is not equal to zero, a mid-transfer seek is initiated by the controller.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the RMDC register contains an address greater than the largest addressable cylinder.

4.19 HOLDING REGISTER (RMHR) base address + 42C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RMHR is a read-only register except as follows: If the register is written into with one of the values listed below, the configured size of the addressed drive is read-out as indicated:

8017 - Maximum cylinder address
8018 - Maximum track address
8019 - Maximum sector address (per RMOF contents)

Writing a FFFF into the register enables the optional Format command to be executed when loaded into RMCS1. The enable is cleared when any data transfer command terminates. Whenever data is written into RMDA, the complement of that data is placed in RMHR.

4.20 MAINTENANCE REGISTER 2 (RMMR2) base address + 430

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
$13FF_{16}$															

RMMR2 is a read-only register that always returns $13FF_{16}$ when read.

4.21 ERROR REGISTER 2 (RMER2) base address + 434

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	DCU	DVC	ACU	SSE	0	DPE	0	0	0

Error Register 2 is a read/write register that contains status information relating to the electromechanical performance of the addressed drive. If any bit is set in this register, then the ERR bit in RMDS is also set. In some cases, the UNS bit in RMER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A drive clear or a controller clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RMER1 will be set and the write will be ignored.

Bad Sector Error (BSE) - Bit 15

Set whenever the controller detects a zero in bit 14 or 15 of the first header word and the HCI bit in RMOF equals zero.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Seek Error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. Can be cleared by issuing a drive clear.

Invalid Command (IVC) - Bit 12

Set whenever any command is issued to a drive with ERR set and MOL clear. Set whenever any command except a Read-in Preset, Pack Acknowledge or NOP is issued to a drive with VV equal zero.

Loss of Sector Clock (LSC) - Bit 11

Set when the controller detects more than 63 Sector pulses without an Index pulse (Sector and Index on B cable).

Loss of Bit Clock (LBC) - Bit 10

Set if the controller does not detect at least 16 servo clocks within 3.0 microseconds.

Multiple Drive Select (MDS) - Bit 09

Set when more than one drive responds to a logical address on the A cable. This bit cannot be set by a programmed I/O write.

D.C. Power Unsafe (DCU) - Bit 08

Set if the -5 vDC power supply to the cable drivers and receivers is not proper. This bit cannot be set by a programmed I/O write.

Device Check (DVC) - Bit 07

Set if a Fault indication is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Fault is detected.

AC Power Unsafe (ACU) - Bit 06

Set if an ACLO indication is received from the bus. This bit cannot be set by a programmed I/O write.

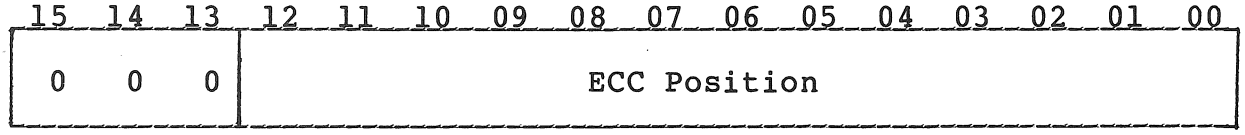
Skip Sector Error (SSE) - Bit 05

For RM80 emulations only. Set whenever bit 13 of the header Word 1 is set and bit 09 of RMOF is reset. This error indicates that the sector has been skipped and the data resides in the next sector. This bit cannot be written into unless the drive is an RM80.

Data Parity Error (DPE) - Bit 03

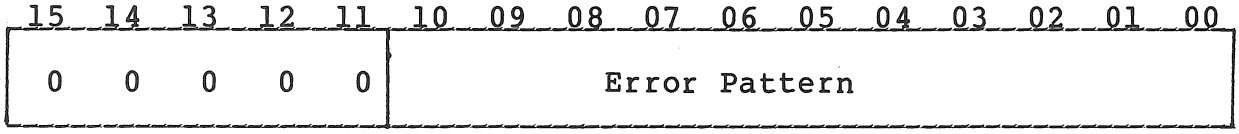
This bit is normally a zero unless written into.

4.22 ECC POSITION REGISTER (RMEC1) base address + 438



The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector's data field to (and including) the right most bit position of the error pattern stored in RMEC2. If the detected error is not correctable using ECC, the ECH error bit in RMER1 will be set.

4.23 ECC PATTERN REGISTER (RMEC2) base address + 43C

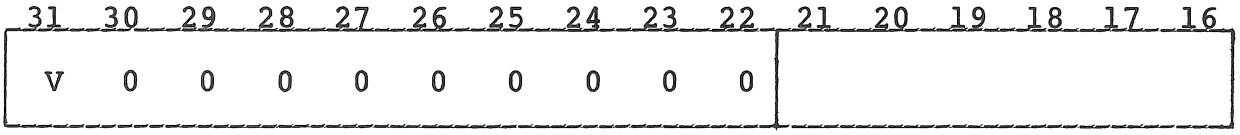


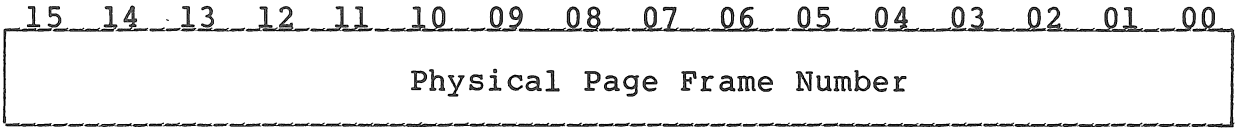
The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A one in the error pattern indicates that a bit of the data in memory from the last read sector is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right most bit of the pattern is determined by the bit count in RMEC1. The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

4.24 ILLEGAL DRIVE REGISTERS

The top 16 drive registers (addresses 20010440 to 2001047C) are illegal addresses. Access to these locations will set ILR (bit 01, RMER1).

4.25 MBA MAP REGISTERS base address + (800:BFC)





The controller contains 256 map registers which are used to form the SBI physical memory address from the 17-bit virtual address contained in MBAVAR. Map registers can only be written when there

is no data transfer operation in progress. A write to a map register during a data transfer will be ignored and cause PGE to set in MBA SR.

Valid Bit (V) - Bit 31

This bit indicates that the entry is a valid PFN.

Physical Page Frame Number (PFN) - Bits <21:00>

High-order 22 bits of the physical memory address.

Operations are initiated on the addressed drive by loading the function code and GO bit into RMCS1. The function code specifies a specific command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping commands. Commands and their corresponding function codes (always odd since the GO bit must be asserted to execute the command) are described below.

5.1 DATA TRANSFER COMMANDS

These commands involve data transfers to or from the disk and are designated by function codes 29 through 3F.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a seek will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the data transfer. On all commands except the Write Header and Data command (which is the format operation) and Read or Write/Check Header and Data commands, a match of the sector header must be made before the data transfer is started. If the header compare inhibit (HCI, bit 10 in RMOF) is set, the header will not be compared or checked and, like the Write Header and Data command, the transfer will be started based on the pre-recorded sector pulses. With the HCI bit set, header errors will not be reported. With the HCI bit cleared, the transfer will be aborted if a header error is detected. The Read/Write Check Header and Data commands abort only the transfers following the sector that caused the error.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek.

The data transfer commands are described below.

5.1.1 Write Check Data (29)

This command reads data from the selected drive and compares it on a byte by byte basis with that obtained from memory. If the data fails to compare, the WCU or WCL status bit is set and the command is terminated immediately. For additional information on write check errors see Sections 4.2 and 4.3.

5.1.2 Write Check Header and Data (2B)

This command reads the header field and data field from the selected drive and compares it on a byte by byte basis with data obtained from memory. If the header and data fail to compare, the WCU or WCL status bit is set and the command is terminated immediately.

5.1.3 Write Data (31)

This command writes the 512-byte data field of the selected sector with data obtained from memory. A two-word ECC is appended to each sector. If the byte count goes to zero during the sector, the rest of the sector is zero filled. After a sector transfer the byte count is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated.

5.1.4 Write Header and Data (format) (33)

This command writes the four-byte header field and the 512-byte data field of the selected sector with data obtained from memory. A one word CRC is appended to each header field, and a two word ECC is appended to each data field. After a sector transfer the byte count is checked, and if not zero, the transfer is continued to the next sector; otherwise the command is terminated. If byte count goes to zero during the sector, the rest of the sector is zero filled.

5.1.5 Read Data (39)

This command reads the 512-byte data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the read command is terminated to allow software to apply the correction information. If no data errors are detected, the byte count is checked; if the byte count is not zero, the data transfer operation is repeated with the next sector. If the byte count goes to zero during the sector, the rest of the sector is not transferred.

5.1.6 Read Header and Data (3B)

This command transfers the four-byte sector header field and the 512-byte data field from the selected sector to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. If no data errors are detected, the byte count is checked; if the byte count is not zero, the data transfer operation is repeated with the next sector.

5.2 POSITIONING COMMANDS

Positioning commands are mechanical movement commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the positioning commands, the controller will set the PIP bit and reset the DRY bit. Upon completion of the positioning operation, the controller resets the PIP and GO bits, sets the DRY and ATA bits. The positioning commands are described below.

5.2.1 Seek Command (5)

This command causes the heads to be moved to the cylinder address specified by the contents of RMDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Any attempt to write into RMDC while the seek is in progress will cause the RMR bit to be set and RMDC will not be modified. Upon completion of the seek operation, the ATA and DRY bits in RMDS are set, and the GO bit is reset. If the drive is unable to complete a move within 500 milliseconds or if it has moved the carriage to a position outside the recording field, the drive asserts the seek error signal and the controller sets the SKI error bit in RMER2 and the ERR, ATA and DRY bits in RMDS. The controller will automatically issue a Fault Clear and a Return-to-Zero to the drive so that a Drive Clear command can clear the error.

5.2.2 Recalibrate (7)

This command will cause the drive positioner to position the heads over cylinder zero. A Return-to-Zero is automatically performed with each head load sequence and whenever a Fault or Seek Error is detected. This command clears the OFM bit in RMDS.

5.2.3 Offset Command (D)

This command causes the OFM bit in RMDS to be set. Subsequent reads will be done with the heads offset from track centerline in the direction specified by RMOF bit seven. This operation allows additional data recovery attempts over that provided by the ECC capability when an ECC error is detected. If an ECC hard error occurs, two offset positions should be used. At the completion of the offset command, the ATA bit is set indicating that a read command should be issued to the cylinder and track in order to recover data.

The OFM bit in RMDS will be cleared by any one of the following:

1. Seek to another cylinder by means of implied or mid-transfer seek,
2. Write command,
3. Return-to-centerline command,
4. Recalibrate command,

5. Read-in preset command, or
6. Whenever the drive cycles up from the OFF state.

5.2.4 Return-to-Centerline Command (F)

This command is used to clear the OFM bit and set the ATA bit in RMDS. It also resets the OFD bit in RMOF.

5.2.5. Search Command (19)

The search command causes the controller to first perform a seek to the desired cylinder and then compare the sector counter with the desired sector in the RMDA register. When they match, it sets the ATA bit causing an interrupt to the computer if IE in MBACR is set. An unsuccessful completion of a search command occurs when a sector count and desired sector address match is not made during the interval of three index pulses, in which case the OPI bit is set.

5.3 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually takes only a few microseconds to execute. The housekeeping commands are listed below.

5.3.1 NO OP (1)

This command does not perform any operation, except to clear the ATA bit.

5.3.2 Drive Clear (9)

This command causes the following registers and conditions associated with the drive selected to be cleared: ATA and ERR in RMDS, RMER1, RMER2, RMEC2, RMMR1 (except bit three which is set) and ATA bit in RMAS.

5.3.3 Release Command (B)

This command performs a drive clear function, and then releases the drive for use by the other port.

5.3.4 Read-In Preset (11)

This command sets the VV (volume valid) bit, clears the RMDC and RMDA registers, clears the RMOF register, and clears the OFM bit in the RMDS register.

5.3.5 Pack Acknowledge (13)

This command sets the VV bit for the command controller. This command or a Read-in Preset command must be issued before any data transfer or positioning command can be given if the pack has gone off-line and then on-line (i.e., MOL change of state). It is primarily intended to avoid unknown pack changes.

5.4 OPTIONAL COMMANDS

The Format command can be executed only after writing an FFFF into RMHR.

5.4.1 Format (3F)

This command executes a Return-to-Zero, clears RMDC and RMDA, and formats the entire pack in standard format. Each sector has bits 14, 15 and the FMT16 bit set in Header Word 1 and an all zeros data field. RMDC will be set to the last cylinder number plus one at completion, the LST bit in RMDS will be set, and the FMT16 bit in RMOF will be set. This command will format full tracks for all emulations. No Bad Sector File or Skip Sector File is written.

5.5 OVERLAPPED SEEKS AND SEARCHES

Normally, overlapped Seeks and Searches terminate and raise the drive's ATA bit as soon as the drive is properly positioned. On systems with two logical units per physical unit there is a slight change. In those cases where overlapped Seeks or Searches are issued to two logical units on the same physical drive, the following rules apply:

1) The first logical unit to be issued a seek or search command will do the physical seek. The other logical unit will simulate the seek.

2) For seek commands, the logical unit that did the physical seek will raise its ATA bit first. The other logical unit will raise its ATA bit about 45 usec later.

3) For search commands, if option switch SW1-4 is OFF then the first logical unit that finds a rotational match after the physical seek has ended will raise its ATA first. If option switch SW1-4 is ON, then the logical unit that did the physical seek will raise its ATA bit first when a rotational match occurs after the physical seek has ended. The other logical unit will raise its ATA bit after the first logical unit raises its ATA bit and a rotational match subsequently occurs. This allows the user to service the logical unit actually on cylinder first, thus minimizing physical seeks.

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APPENDIX A

SC780/B1 CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the user of the SC780/B1 the greatest amount of flexibility in selecting disk drives for his system, the SC780/B1 supports a wide variety of disk types and offers a number of other user selectable options. This appendix is designed as a quick reference to the various switches which make this flexibility possible.

A.2 CONTROLLER CONFIGURATION

The SC780/B1 unit is capable of controlling a wide variety of disk drives of various sizes and types. The various drives that are supported are defined by the Configuration PROM. Table A-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuration switch SW2. The correct switch settings for each of the various configurations are given in Table A-2.

A.2.1 SC780 /B1 vs /B3 Firmware

The setting of the number of sectors for the 2351A Fujitsu (Eagle) will be dependent upon the type of Emulex SC780/B firmware the user has. Users with the /B1 firmware must configure the Eagle for 44 hard sectors. Those with /B3 firmware must configure the Eagle for 48 sectors. This 48 sector configuration supports an additional 40 Mb of capacity. See Table A-2 for the list of configurations supported by the SC780/B. Note that in Table A-2 configurations for the 2351A Fujitsu (key 470) are listed as being configured for 44/48 sectors. Those configurations are supported at 44 sectors per track by the /B1 firmware and 48 sectors per track by the /B3 firmware. See paragraph A.2.3 for important information on sectoring the Fujitsu Eagle.

A.2.2 Physical vs Logical Disk Numbering

One of the primary features of the SC780/B1 is that it can emulate up to eight DEC disk subsystems using only four physical disk drives. This is accomplished by mapping two logical disk subsystems on to one disk drive that has double the capacity of the standard DEC subsystem. In such cases the logical units are mapped on to the physical units as follows:

Physical Unit Number	Logical Unit Numbers
0	0 and 4
1	1 and 5
2	2 and 6
3	3 and 7

The physical/logical assignments for specific disk configurations can be found by comparing the Physical drive column to the Logical drive column in Table A-2.

A.2.3 Sectoring CDC Drives and the 2351A Fujitsu

To allow CDC drives and the 2351A Fujitsu to function properly with the SC780/B, some alterations must be made to the sector select switch settings found in their manuals.

To configure CDC drives for 33 sectors, switch 0 must be CLOSED, with all other switch settings as per the CDC manual. To configure the 2351A Fujitsu for 48 sectors the jumpers at location BC7 must be set such that bit one is jumpered 2-3 (rather than 3-4) and bit 2 is jumpered 6-7 (rather than 5-6), with all other jumpers set as per the Fujitsu manual.

A.2.4 Drive Configuration Selection

The SC780/B1 emulates three different DEC disk subsystems, the RM03, the RM05 and the RM80. The RM03 subsystem has an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb. The RM80 has a capacity of 160 Mb.

There are essentially three different types of drive configurations. In the first case, each emulated DEC drive exists on one physical drive. In the second case, two emulated drives are mapped on to one physical drive (see paragraph A.2.1). The third case is a combination of the first two.

With the exception of configurations noted, none require patches to the operating system or diagnostics. The other require patches to the disk driver to include the expanded block counts and sector counts where applicable. Note that the DEC VMS driver cannot be patched for more than 32 sectors per track. Emulex has a VMS driver that automatically self-sizes to each drive. The Emulex driver can handle up to 64 sectors per track. Note that neither the diskless nor the functional diagnostics will run on non-standard size drives.

To find the configuration switch setting that is suitable for your disk installation, use the following process. Note that some configurations require drives set with 32 hard sectors and some require drives set with 33 or 44 or 48 hard sectors (Physical SEC column of Table A-2). See the drive manufacturer's installation manual for instructions. Note also that use of a Trident type drive requires that SW1-5 be closed.

1. Locate your drive type and size in Table A-1. Note down the KEY assigned to your drive. If you intend to use more than one type of drive, note down their assigned KEYs as well. Make sure your drive is hard sectored as indicated in the SEC column of Table A-2.

2. Scan down the KEY column of Table A-2 until you find your drive's number. Check the type of emulation in the Logical drive column. If the emulation is not the one you require, continue to scan down the KEY column, etc., until you find the required emulation.

3. When you find a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. You do not need to use all four drive ports.

4. When you find a suitable configuration, set the Configuration Switches (SW2) as indicated.

TABLE A-1
DRIVES SUPPORTED

Model Numbers	KEY	Sects
Ampex/330	330	32/33
Ampex/9300	301	32
Century/T82RM	80	32
Century/T302RM	300	32
CDC/9730-80	80	32
CDC/9730-160	160	32/33[1]
CDC/9762	80	32
CDC/9766	300	32
CDC/9775	675	32/33[1]
Fujitsu/2312	84	32/33
Fujitsu/2280	80	32
Fujitsu/2294	330	32/33
Fujitsu/M2284	160	32/33
Fujitsu/2351A	470	44/48[2]
NEC/D1510	331	32/33
STC/8775	673	32
Techstor/S160	162	32/33

[1]See paragraph A.2.3.

[2]See paragraphs A.2.1 and A.2.3.

TABLE A-2
DRIVE CONFIGURATIONS, PROM No. 496

CONF NO.	SW2- 6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
00	O	O	O	O	O	O	80	0	32	0 = RM03	A
							80	1	32	1 = RM03	A
							80	2	32	2 = RM03	A
							80	3	32	3 = RM03	A
01	O	O	O	O	O	C	160	0	33	0 = RM80	A
							160	1	33	1 = RM80	A
							160	2	33	2 = RM80	A
							160	3	33	3 = RM80	A
02	O	O	O	O	C	O	300	0	32	0 = RM05	A
							300	1	32	1 = RM05	A
							300	2	32	2 = RM05	A
							300	3	32	3 = RM05	A
03	O	O	O	O	C	C	160	0	33	0,4 = RM03	A
							160	1	33	1,5 = RM03	A
							160	2	33	2,6 = RM03	A
							160	3	33	3,7 = RM03	A
04	O	O	O	C	O	O	675	0	33	0,4 = RM05	A
							675	1	33	1,5 = RM05	A
							675	2	33	2,6 = RM05	A
							675	3	33	3,7 = RM05	A
05	O	O	O	C	O	C	673	0	32	0,4 = RM05	A
							673	1	32	1,5 = RM05	A
							673	2	32	2,6 = RM05	A
							673	3	32	3,7 = RM05	A
06	O	O	O	C	C	O	330	0	33	0,4 = RM80	A
							330	1	33	1,5 = RM80	A
							330	2	33	2,6 = RM80	A
							330	3	33	3,7 = RM80	A
07	O	O	O	C	C	C	80	0	32	0 = RM03	A
							80	1	32	1 = RM03	A
							300	2	32	2 = RM05	A
							300	3	32	3 = RM05	A
08	O	O	C	O	O	O	80	0	32	0 = RM03	A
							300	1	32	1 = RM05	A
							300	2	32	2 = RM05	A
							300	3	32	3 = RM05	A
09	O	O	C	O	O	C	300	0	32	0 = RM05	A
							300	1	32	1 = RM05	A
							80	2	32	2 = RM03	A
							80	3	32	3 = RM03	A
0A	O	O	C	O	C	O	300	0	32	0 = RM05	A
							300	1	32	1 = RM05	A
							300	2	32	2 = RM05	A
							80	3	32	3 = RM03	A
0B	O	O	C	O	C	C	160	0	33	0,4 = RM03	A
							160	1	33	1,5 = RM03	A
							80	2	32	2 = RM03	A
							80	3	32	3 = RM03	A

TABLE A-2, cont.

CONF NO.	SW2- 6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
0C	O	O	C	C	O	O	160	0	33	0,4 = RM03	A
							160	1	33	1,5 = RM03	A
							160	2	33	2,6 = RM03	A
							80	3	32	3 = RM03	A
0D	O	O	C	C	O	C	160	0	33	0 = RM80	A
							160	1	33	1 = RM80	A
							80	2	32	2 = RM03	A
							80	3	32	3 = RM03	A
0E	O	O	C	C	C	O	160	0	33	0 = RM80	A
							160	1	33	1 = RM80	A
							160	2	33	2 = RM80	A
							80	3	32	3 = RM03	A
0F	O	O	C	C	C	C	675	0	33	0,4 = RM05	A
							675	1	33	1,5 = RM05	A
							300	2	32	2 = RM05	A
							300	3	32	3 = RM05	A
10	O	C	O	O	O	O	675	0	33	0,4 = RM05	A
							675	1	33	1,5 = RM05	A
							675	2	33	2,6 = RM05	A
							300	3	32	3 = RM05	A
11	O	C	O	O	O	C	300	0	32	0 = RM05	A
							300	1	32	1 = RM05	A
							675	2	33	2,6 = RM05	A
							675	3	33	3,7 = RM05	A
12	O	C	O	O	C	O	300	0	32	0 = RM05	A
							675	1	33	1,5 = RM05	A
							675	2	33	2,6 = RM05	A
							675	3	33	3,7 = RM05	A
13	O	C	O	O	C	C	160	0	33	0 = RM80	A
							160	1	33	1 = RM80	A
							300	2	32	2 = RM05	A
							300	3	32	3 = RM05	A
14	O	C	O	C	O	O	160	0	33	0 = RM80	A
							160	1	33	1 = RM80	A
							160	2	33	2 = RM80	A
							300	3	32	3 = RM05	A
15	O	C	O	C	O	C	330	0	33	0 = RM05[1]	A
							330	1	33	1 = RM05[1]	A
							330	2	33	2 = RM05[1]	A
							330	3	33	3 = RM05[1]	A
16	O	C	O	C	C	O	160	0	32	0 = RM02[2]	B
							160	1	32	1 = RM02[2]	B
							160	2	32	2 = RM02[2]	B
							160	3	32	3 = RM02[2]	B
17	O	C	O	C	C	C	330	0	32	0 = RM02[3]	B
							330	1	32	1 = RM02[3]	B
							330	2	32	2 = RM02[3]	B
							330	3	32	3 = RM02[3]	B

TABLE A-2, cont.

CONF NO.	SW2- 6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
18	O	C	C	O	O	O	330	0	33	0 = RM05	C
							300	1	32	1 = RM05	C
							300	2	32	2 = RM05	C
							300	3	32	3 = RM05	C
19	O	C	C	O	O	C	330	0	33	0 = RM05	C
							330	1	33	1 = RM05	C
							300	2	32	2 = RM05	C
							300	3	32	3 = RM05	C
1A	O	C	C	O	C	O	330	0	33	0 = RM05	C
							330	1	33	1 = RM05	C
							330	2	33	2 = RM05	C
							300	3	32	3 = RM05	C
1B	O	C	C	O	C	C	162	0	33	0,4 = RM03	C
							162	1	33	1,5 = RM03	C
							162	2	33	2,6 = RM03	C
							80	3	32	3 = RM03	C
1C	O	C	C	C	O	O	162	0	33	0 = RM80	C
							162	1	33	1 = RM80	C
							162	2	33	2 = RM80	C
							162	3	33	3 = RM80	C
1D	O	C	C	C	O	C	160	0	33	0 = RM80	C
							330	1	33	1 = RM05	C
							330	2	33	2 = RM05	C
							330	3	33	3 = RM05	C
1E	O	C	C	C	C	O	160	0	33	0 = RM80	C
							330	1	33	1,5 = RM80	C
							330	2	33	2,6 = RM80	C
							330	3	33	3,7 = RM80	C
1F	O	C	C	C	C	C	160	0	33	0,4 = RM03	C
							160	1	33	1,5 = RM03	C
							330	2	33	2 = RM05	C
							330	3	33	3 = RM05	C
20	C	O	O	O	O	O	470	0	44/48	0 = RM80[4]	D
							470	1	44/48	1 = RM80[4]	D
							470	2	44/48	2 = RM80[4]	D
							470	3	44/48	3 = RM80[4]	D
21	C	O	O	O	O	C	470	0	44/48	0 = RM80[4]	D
							470	1	44/48	1 = RM80[4]	D
							470	2	44/48	2 = RM80[4]	D
							300	3	32	3 = RM05	D
22	C	O	O	O	C	O	470	0	44/48	0 = RM80[4]	D
							470	1	44/48	1 = RM80[4]	D
							470	2	44/48	2 = RM80[4]	D
							80	3	32	3 = RM03	D
23	C	O	O	O	C	C	84	0	33	0 = RM03	D
							84	1	33	1 = RM03	D
							84	2	33	2 = RM03	D
							84	3	33	3 = RM03	D

TABLE A-2, cont.

CONF NO.	SW2- 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
24	C O O C O O	84	0	33	0 = RM03	D
		84	1	33	1 = RM03	D
		84	2	33	2 = RM03	D
		80	3	33	3 = RM03	D
25	C O O C O C	301	0	32	0 = RM02[5]	E
		301	1	32	1 = RM02[5]	E
		301	2	32	2 = RM02[5]	E
		301	3	32	3 = RM02[5]	E
26	C O O C C O	160	0	32	0 = RM02[2]	E
		160	1	32	1 = RM02[2]	E
		301	2	32	2 = RM02[5]	E
		301	3	32	3 = RM02[5]	E
27	C O O C C C	80	0	32	0 = RM03	F
		80	1	32	1 = RM03	F
		330	2	33	2 = RM05	F
		330	3	33	3 = RM05	F
28	C O C O O O	160	0	33	0 = RM80	G
		160	1	33	1 = RM80	G
		470	2	44/48	2 = RM80[4]	G
		470	3	44/48	3 = RM80[4]	G
29	C O C O O C	160	0	33	0 = RM80	G
		470	1	44/48	1 = RM80[4]	G
		470	2	44/48	2 = RM80[4]	G
		470	3	44/48	3 = RM80[4]	G
2A	C O C O C O	470	0	44/48	0 = RM80[4]	G
		470	1	44/48	1 = RM80[4]	G
		80	2	32	2 = RM03	G
		80	3	32	3 = RM03	G
2B	C O C O C C	470	0	44/48	0 = RM80[4]	G
		470	1	44/48	1 = RM80[4]	G
		300	2	32	2 = RM05	G
		300	3	32	3 = RM05	G
2C	C O C C O O	331	0	33	0 = RM05	G
		331	1	33	1 = RM05	G
		331	2	33	2 = RM05	G
		331	3	33	3 = RM05	G
2D	C O C C O C	470	0	44/48	0 = RM02[6]	H
		470	1	44/48	1 = RM02[6]	H
		470	2	44/48	2 = RM02[6]	H
		470	3	44/48	3 = RM02[6]	H
2E	C O C C C O	470	0	44/48	0 = RM02[6]	H
		470	1	44/48	1 = RM02[6]	H
		470	2	44/48	2 = RM02[6]	H
		300	3	32	3 = RM05	H
2F	C O C C C C	160	0	33	0,4 = RM03	H
		160	1	33	1,5 = RM03	H
		300	2	32	2 = RM05	H
		300	3	32	3 = RM05	H

TABLE A-2, cont.

CONF NO.	SW2- 6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) =	Dr Type	Rev
30	C	C	O	O	O	O	160	0	33	0 =	RM80	J
							160	1	33	1 =	RM80	J
							300	2	32	2 =	RM05	J
							80	3	32	3 =	RM03	J
31	C	C	O	O	O	C	160	0	33	0,4 =	RM03	J
							160	1	33	1,5 =	RM03	J
							300	2	32	2 =	RM05	J
							80	3	32	3 =	RM03	J
32	C	C	O	O	C	O	300	0	32	0 =	RM05	J
							300	1	32	1 =	RM05	J
							160	2	33	2,6 =	RM03	J
							160	3	33	3,7 =	RM03	J
33	C	C	O	O	C	C	80	0	32	0 =	RM03	K
							160	1	33	1 =	RM80	K
							160	2	33	2 =	RM80	K
							160	3	33	3 =	RM80	K
34	C	C	O	C	O	O	470	0	44/48	0 =	RM02[6,7]	L
							300	1	32	1 =	RM05[7]	L
							300	2	32	2 =	RM05[7]	L
							300	3	32	3 =	RM05[7]	L
35	C	C	O	C	O	C	470	0	44/48	0 =	RM80[4]	L
							300	1	32	1 =	RM05	L
							300	2	32	2 =	RM05	L
							300	3	32	3 =	RM05[4]	L
36	C	C	O	C	C	O	470	0	44/48	0 =	RM80[4]	M
							470	1	44/48	1 =	RM80[4]	M
							160	2	33	2,9 =	RM03	M
							160	3	33	3,7 =	RM03[7]	M
37	C	C	O	C	C	C	160	0	33	0 =	RM80[6]	N
							470	1	44/48	1 =	RM02[6]	N
							470	2	44/48	2 =	RM02[6]	N
							470	3	44/48	3 =	RM02[6]	N
38	C	C	C	O	O	O	470	0	44/48	0 =	RM02[6,7]	P
							300	1	32	1 =	RM05[7]	P
							80	2	32	2 =	RM03[7]	P
							80	3	32	3 =	RM03[6]	P
39	C	C	C	O	O	C	470	0	44/48	0 =	RM02[6]	P
							470	1	44/48	1 =	RM02[6,7]	P
							300	2	32	2 =	RM05[7]	P
							80	3	32	3 =	RM03[7]	P
3A	C	C	C	O	C	O	470	0	44/48	0 =	RM02[6]	R
							470	1	44/48	1 =	RM02[6]	R
							470	2	44/48	2 =	RM02[6,7]	R
							80	3	32	3 =	RM03[8]	R
3B	C	C	C	O	C	C	675	0	32	0 =	RM05[8]	S
							675	1	32	1 =	RM05[8]	S
							675	2	32	2 =	RM05[8]	S
							675	3	32	3 =	RM05[8]	S

TABLE A-2, cont.

CONF NO.	SW2- 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
3C	C C C C O O	80	0	32	0 = RM03	S
		80	1	32	1 = RM03	S
		80	2	32	2 = RM03[9]	S
		470	3	44/48	3 = RM80[10]	S
3D	C C C C O C	470	0	44/48	0,4 = RM03[10]	S
		470	1	44/48	1,5 = RM03[10]	S
		300	2	33	2 = RM05	S
		300	3	33	3 = RM05	S

[1]This emulation has 862 logical cylinders.

[2]This RM emulation has 823 cylinders, 10 heads and a DTC of 15_{16}. This emulation is not supported by VMS, but was specifically included for use with Berkeley UNIX.

[3]This RM emulation has 1024 cylinders, 16 heads, and a DTC of 15_{16}. This emulation is not supported by VMS, but was specifically included for use with Berkeley UNIX.

[4]This RM80 emulation has 842 cylinders, 20 heads, 44 (/B1) or 48 (/B3) sectors and a DTC of 16_{16}. It has the skip characteristics of the RM80.

[5]This RM02 emulation has 815 cylinders, 19 heads and a DTC of 15_{16}.

[6]This RM02 emulation has 842 cylinders, 20 heads and a DTC of 15_{16}. This emulation is not supported by VMS, but was specifically included for use with Berkely UNIX.

[7]For UNIX systems. Not compatible with VMS.

[8]This RM05 has 842 cylinders, 40 heads and a DTC of 17_{16} (unmapped).

[9]This RM80 has 842 cylinders, 20 heads, 43 sectors and a DTC of 16_{16}. It is an expanded RM80 with the skip sector feature.

[10]This RM03 has 842 cylinders, 10 heads and a DTC of 14_{16}.

C = Closed (ON) O = Open (OFF).

A.3 SC780/B1 USER SELECTABLE OPTIONS

Several other options for the SC780/B1 can be user selected. The functions of the switches that select those options are defined in Tables A-3, A-4, A-5 and A-6, below.

TABLE A-3
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1			Not used[1]
SW1-2			Not used[1]
SW1-3			Not used[1]
SW1-4	Disable	Enable	Delay on overlapped searches to the same physical drive.
SW1-5	Disable	Enable	CDS Trident drive compatibility.
SW1-6	Disabled	Enabled	Dual port mode
SW1-7			SC780 address mode[3]
SW1-8	B Cable	A Cable	Sector and Index signals[2]

[1]All unused switches MUST BE OFF.
[2]See paragraphs 3.3.5 and 3.6.5.
3Must be closed (ON).

TABLE A-4
OPTION SWITCH SW2 SETTINGS

Option Sw	Open	Closed	Function
SW2-1			Drive Configuration[2]
SW2-2			Drive Configuration[2]
SW2-3			Drive Configuration[2]
SW2-4			Drive Configuration[2]
SW2-5			Drive Configuration[2]
SW2-6			Drive Configuration[2]
SW2-7			Not used[1]
SW2-8			Not used[1]
SW2-9			Not used[1]
SW2-10			Not used[1]

[1]All unused switches MUST BE OFF.
[2]See Table A-1.

TABLE A-5
OPTION SWITCH SW3 SETTINGS

Option Sw	Open	Closed	Function
SW3-1	750	780	SC780 Compatibility Mode[4]
SW3-2			MBA arbitration level[2]
SW3-3			MBA arbitration level[2]
SW3-4			MBA arbitration level[2]
SW3-5			MBA arbitration level[2]
SW3-6			MBA arbitration level[2]
SW3-7			Not used[1]
SW3-8	Slot 3	Slot 4	Controller Address[3]

[1]All unused switches MUST BE OFF.
[2]See paragraph 3.6.3.
[3]See paragraph 3.6.2.
[4]MUST BE CLOSED (ON)

TABLE A-6
OPTION SWITCH SW4 SETTINGS

Option Sw	Open	Closed	Function
SW4-1	Run	Halt-Reset	Controller Run/Halt-Reset[2]
SW4-2			Not used[1]
SW4-3			Not used[1]
SW4-4	Disable	Enable	Dual Access (Rev C and above)

[1]All unused switches MUST BE OFF.

A.4 INTERFACE PCBA OPTION SWITCHES

TABLE A-7
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1			SBI Arbitration (TR no.) Level[2]
SW1-2			SBI Arbitration (TR no.) Level[2]
SW1-3			SBI Arbitration (TR no.) Level[2]
SW1-4			SBI Arbitration (TR no.) Level[2]
SW1-5			SBI Interrupt Request Level[3]
SW1-6			SBI Interrupt Request Level[3]
SW1-7			Not used[1]
SW1-8			Not used[1]

[1]All unused switches MUST BE OFF.
[2]See paragraph 3.5.2 for settings.
[3]See paragraph 3.5.3 for settings.

A.5 BUS TRANSLATOR PCBA OPTION SWITCHES

TABLE A-8
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1	Disable	Enable	Early TR (slot 3)[1]
SW1-2	Disable	Enable	Early TR (slot 4)[1]
SW1-3	Enable	Disable	Continuous Clock
SW1-4			Not used

[1] See paragraph 3.5.4.1.

APPENDIX B

DRIVE MODIFICATIONS

This appendix provides modifications to commonly used drives for moving the Sector and Index signals from the A cable to the B cable.

B.1 CDC 9762

Remove (Ch. I)	Add (Ch. I)
B01-06B to JA82-18B	B01-06B to JA82-43B
B01-06A to JA82-18A	B01-06A to JA82-44A
B01-05B to JA82-25B	B01-05B to JA82-45B
B01-05A to JA82-25A	B01-05A to JA82-45A

Remove (Ch. II)	Add (Ch. II)
B03-06B to JA83-18B	B03-06B to JA83-43B
B03-06A to JA83-18A	B03-06A to JA83-44A
B03-05B to JA83-25B	B03-05B to JA83-45B
B03-05A to JA83-25A	B03-05A to JA83-45A

Rework transmitter card FTVV in location B01 (Ch. I) and B03 (Ch. II). Locate jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark a "G" in its place so that the card type becomes GTVV.

NOTE - Starting with S/N 78,989 CDC will ship units with an enhancement feature which will allow easy switchover to the B cable as follows: Remove the jumper plug on (B07) of the logic chassis backpanel.

B.2 CDC 9730

Rework transmitter-receiver card CFAX in location A04 (Ch. I) and B04 (Ch. II). When viewing card with connector on the right, locate four jumpers to the left of the I/O connectors and above the terminator ground lug. The bottom end of the jumpers must be removed from the holes to which they are soldered and moved to the holes immediately above. Next, find the small jumper to the right of the third IC from the connector edge of the board on the bottom row of ICs. This jumper must be removed and reinserted so that it connects the top and middle holes rather than the original connection of the bottom and middle. This connection ungates the sector and index driver.

Remove the letter "C" from the card type designation CFAX and mark a "D" in its place so that the card type becomes DFAX.

B.3 CDC 9766

Remove (Ch. I)		Remove (Ch. II)	
Sector +	J4-55	Sector +	J4-55
Sector -	J4-25	Sector -	J4-25
Index +	J4-48	Index +	J4-48
Index -	J4-18	Index -	J4-18

Move Wire (Ch. I)	Orgin	From	To
Sector +	PA01-5B	J3-55	J2-26
Sector -	PA01-5A	J3-25	J2-13
Index +	PA01-6B	J3-48	J2-24
Index -	PA01-6A	J3-18	J2-12

Move Wire (Ch. II)	Orgin	From	To
Sector +	PA03-5B	J3-55	J2-26
Sector -	PA03-5A	J3-25	J2-13
Index +	PA03-6B	J3-48	J2-24
Index -	PA03-6A	J3-18	J2-12

Rework transmitter card FTVV in location A01 (Ch. I) and A03 (Ch. II). Locate the jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark "G" in its place so that the card type becomes GTVV.

NOTE - Starting with S/N 15,382 CDC will ship units with an enhancement feature which will allow easy switchover to the B cable as follows: Cut the cable tie securing PD90 to the I/O cable and plug PD90 into JD90 pins 13 and 14 (Ch. I) and pins 11 and 12 (Ch. II) as indicated on the top of the connector.

B.4 CDC 9448

Sector and Index are on both the A and B cables.

B.5 TRIDENT DRIVES

Sector and Index are on both the A and B cables.

B.6 FUJITSU DRIVES

Sector and Index are on both the A and B cables.

B.7 AMPEX CAPRICORN

To place the sector and index signals on both the A and B cables make the following jumper connections on the I/O board: E1 to E2, E3 to E4, E5 to E6 and E7 to E8.

APPENDIX C

OPERATION OF DIAGNOSTICS

C.1 INTRODUCTION

The following is a step-by-step procedure for running the DEC RH780 and RM03/RM05/RM80 diagnostics. Emulex recommends running the diagnostic programs in the order presented (skip the programs not intended for your drive). Additional information on the Diagnostic Supervisor and running of the diagnostic programs can be found in the "VAX Diagnostic System User's Guide" (DEC Publication No. EK-VX11D-UG-001) or by typing HELP when in the Diagnostic Supervisor.

C.2 LOADING AND STARTING

To allow the diagnostic supervisor to be booted on a command from the system consol, the console must be in the console I/O mode (indicated by a >>> prompt). If that prompt is not present, type CTRL P. That will place the console in the I/O mode.

To load the Diagnostic Supervisor from a floppy disk, load the DS diskette into the floppy drive and type "B" at the console. If the DS is on the system disk, typing "B SBO" cause it to be loaded.

Once the diagnostic supervisor has been loaded it will prompt with DS>.

If the supervisor was booted from a floppy disk, remove the floppy from the drive and replace it with the floppy that contains the RH780 diagnostics.

The Massbus Adaptors (RHn) and drives to be tested (DRBn) must be ATTACHed to inform the diagnostic supervisor of their presence and type.

1. ATTACH the RH780 (SC780): specify its device type (RH780), its link to the CPU (SBI), its generic device name and address (RH0, RH1 or RH2), TR level (8, 9, 10 or 11) and BR level (5):

   DS> ATTACH RH780 SBI RH1 10 5

2. ATTACH the disk drive: specify the type (RM03, RM05 or RM80), link to the CPU (RH0, RH1 or RH3) and generic device name (DBB0, DBB1, DBB2 or DBB3):

   DS> ATTACH RM03 RH1 DBB0

You must ATTACH a Massbus Adaptor in order to ATTACH a drive that is connected to it even if you do not intend to run diagnostics on the adaptor. One ATTACH statement is required for each device. Substitute the appropriate variable for each new statement.

After ATTACHing the group of devices to be tested, you must SELECT the specific devices that are to be tested.

3. SELECT the Massbus Adaptor to be tested: use its generic device name:

```
DS>  SELECT RH1
```

4. SELECT the disk drive to be tested: use its generic device name:

```
DS>  SELECT DBB0
```

All devices that are to be tested must be SELECTed using individual SELECT statements. When more than one device of the same type has been SELECTed, tests run against that type of device are run sequentially, lowest numbered device first.

To allow the operator to monitor the progress of the testing, the trace option should be SET.

5. SET the trace option:

```
DS>  SET TRACE
```

The next step is to LOAD the diagnostics. The default load device is the device from which the supervisor was booted.

6. LOAD a diagnostic program (in this case ESCAA) is as follows:

```
DS>  LOAD ESCAA
```

Only one program may be LOADed at a time.

Once LOADed, the program may be STARTed (or restarted) in any section or test any number of times (without redoing any of the the above operations).

7. START the test that is currently in memory by typing:

```
DS>  START
```

   All tests and/or sections will be run one time.

8. START the diagnostic: specify the TEST number(s) to be run by typing:

```
DS>  START/TEST:first:last
```

   Substitute the decimal number of the first test to be run for the word first and the number for the last test to run for the word last. All of the tests between those two numbers will be run. To run only one test, the first and last numbers are the same.

9. START the diagnostic: specify the TEST numbers and to specify the number of PASSes of all the tests selected by typing:

```
DS>  START/TEST:first:last/PASS:n
```

Substitute a decimal number for the letter n.

10. START the diagnostic: specify a SECTION name by typing:

```
DS>  START/SECTION:name
```

Substitute the name of a SECTION of the diagnostic for the word name.

The program can be returned to the Diagnostic Supervisor by typing CTRL C. The program may then be aborted by typing ABORT or the program can be resumed (after possible flag changing) by typing CONT.

C.3 ESCAA - RH780 DIAGNOSTIC

To run this diagnostic SELECT the appropriate RH780 (RH0, RH1 or RH3). It is not necessary to ATTACH or SELECT a drive.

This diagnostic provides for functional verification and testing of the RH780 Massbus Adapter (MBA) portion of the controller. Much of the diagnostic makes use of the Diagnostic Register which simulates signals from the Massbus. Since the SC780 does not have an actual Massbus, it is not possible to run those test which make use of the Massbus simulation function. Tests 1-3 and 5-6 will run without error and test the MBA controller registers and the map registers.

C.4 EVRDA - RM03/5 RM80 DISKLESS DIAGNOSTIC

This diagnostic is a stand alone program which uses functional and diagnostic means to verify the operability of the controller independently of the drive.

Part of this diagnostic operates the drive in diagnostic mode which is not fully implemented in the SC780. Consequently, with the drive cycled down only tests 1-23 will run without errors. The functions performed by this diagnostic are very limited and do not involve any data transfers.

C.5 EVRAC VAX (RM03/5) DISK FORMATTER

The formatter consists of six sections made up of one or more common parts or tests. When the formatter is started, the

initialization code requests a channel be assigned for the selected disk, builds a device dependent table and then reads the homeblock. If the pack is labeled SCRATCH the program will proceed. If the program is unable to read the homeblock or the pack is not labeled SCRATCH the user will be asked whether to proceed or not.

Initialization adjusts QIO buffer sizes dependent on which mode the program is running in. If the program is running in user mode under VMS the buffer size will be set to 35 pages. This will allow one track transfers for the largest disk. If the program is running in stand-alone the buffer size will be set to 110 pages. This will allow multi-track transfers.

The following is a description of each of the sections:

PACKINIT

This section formats and writes a bad sector file with zero entries on all sectors of the last track. The section then reads the bad sector file and verifies that the file conforms to the proper format and that all physical disk addresses are within the limits of the drive. (If the file cannot be read or is corrupt the program will be aborted).

After successfully reading the bad sector file, the disk pack is formatted a track at a time. At the completion of the format process a write/read sequence is performed on every sector of the disk pack. During this surface analysis any bad sector discovered is flagged and added to the bad sector file. The homeblock is written with the name SCRATCH in a form that allows disk diagnostics to see a valid label name, but makes the homeblock appear invalid to VMS.

This section should never be run unless the user has verified that the disk subsystem is functioning correctly and that the bad sector file in indeed missing or corrupt. This section will have to be used on all foreign packs and on those packs that have not had bad sector files previously written on the pack. The user should be aware that the updated bad sector file is not written on the pack until the end of the verify operation.

FORMAT

This section reads and validates the bad sector file. If the file cannot be read or is corrupt the program will abort. After successfully reading the bad sector file the disk pack is formatted a track at a time. At the completion of the format process a surface analysis is performed and any bad sector discovered is flagged and added to the bad sector file. The homeblock is written with the name SCRATCH.

VERIFY

This section reads and validates the bad sector file. (If the file cannot be read or is corrupt the program will be aborted.) After successfully reading the bad sector file the disk pack is surface analyzed, and any bad sector discovered is flagged and added to the bad sector file. The homeblock is written with the name SCRATCH.

The user should be aware that the updated bad sector file is not written on the pack until the end of the verify section.

READALL

This section reads every sector on a pack and prints any data errors found in a head map error report. On a known good disk drive, this section can be used to search for data errors on a pack. Conversely, using a known good pack or one with known errors, this section can be used to check the read capability of the drive.

FLAGBAD

This section allows the user to manually update the bad sector file. The section prompts the user for the address of the bad block. After the user has selected all the bad blocks he wishes to flag, the program re-writes the bad block file and clears the bad sector flag in the header word of the bad block. The program then re-writes the homeblock to destroy the file directory. This is done to ensure that no files will contain holes. The program then reads the bad block file and displays its contents.

This section should not be used unless the user is familiar with the structure of the bad sector file and understands the significance of updating the file. Any data on the disk will not be preserved. The homeblock is re-written with the name SCRATCH.

HELP

This is the default section. Section names are identified along with their function.

Program and Event Flags

Quick - The quick flag reduces the number of data patterns used in verify from three to one.

Event Flag 23 - Causes the starting disk address to be printed for each step in a section.

Event Flag 22 - Causes the starting disk address to be printed once every 100 cylinders.

Event Flag 21 - Causes error messages to be printed in brief format.

Event Flag 20 - Causes single track transfers in the surface analysis test (stand-alone mode only).

Format and Verify Time

Drive	Normal	Quick
RM03	14 min.	7 min.
RM05	60 min.	37 min.

C.6 EVRDB - VAX RM03/5 FUNCTIONAL

The program contains a set of 40 tests which will verify the integrity of the controller and drives under test. The set of tests included are: data transfer tests, seek tests, timing tests, and manual intervention tests. Tests 34-37 are manual intervention tests and are invoked by running the section called MANUAL.

The program requires that there be a scratch pack mounted and online.

C.7 EVRGA - RM80 FORMATTER

The function of this program is to format the RM80 HDA. EVRGA is a section selectable formatter rather than test selectable to prevent accidental destruction of data. When the formatter is started, the initialization code requests that a channel be assigned for the selected disk, builds a device dependent table and then reads the homeblock. If the pack is labeled SCRATCH the program will proceed. If the program is unable to read the homeblock or if the pack is not labeled SCRATCH the program will ask if you wish to override the protection check. If the program is running under VMS, the buffer will be set to 35 pages. This will allow one track transfers of the largest disk. If the program is running in stand-alone, the buffer size will be set to 110 pages. This will allow multi-track transfers (up to 3 tracks on an RM80).

The following is a description of each of the seven sections:

HDAINIT

This section will first ask the user which files are to be initialized, the skip sector file or the bad sector file. Once this has been determined the track that the file resides on is formatted and a zero entry bad or skip sector file is written and verified.

This section should never be run unless the user has verified that the disk subsystem is functioning correctly and that the bad or skip sector file is indeed missing or corrupt. This section will have to be used on all foreign HDA's and on those HDA's that have

not had a bad sector file previously written on the HDA. The bad sector file and the skip sector file must have the same serial number.

FORMAT

This section reads and validates both sector files. (If the files cannot be read or are corrupt the program will abort). After successfully reading both sector files, the disk HDA is formatted a track at a time. A surface analysis is performed at the completion of the format process, and any bad sector discovered is flagged and added to the bad sector file or the skip sector file. This is dependent on the error type and position. The homeblock is written with the name SCRATCH.

VERIFY

This section reads and validates both sector files. (If the files cannot be read or are corrupt the program will be aborted.) After successfully reading the bad sector and skip sector files, the disk pack is surface analyzed and any bad sector discovered is flagged and added to the bad sector file or skip sector file. This is dependent on the error type and position of the error. The homeblock is written with the name SCRATCH.

The user should be aware that the updated bad sector file is not written on the pack until the end of the verify section.

READALL

This section reads every sector on the HDA and prints any data errors found in a head map error report. On a known good drive, this section can be used to search for data errors on a HDA. Conversely, using a known good HDA or one with known errors, this section can be used to check the read capability of the drive and controller.

UPDATE

This section allows the user to manually update the bad sector file or skip sector file. The section prompts the user for the address of the bad block. After the user has selected all the bad blocks he wishes to flag, the program re-writes the bad block file or skip sector file. This section should not be used unless the user is familiar with the skip sectoring algorithm incorporated by the RM80. The user must also understand the structure of the bad sector file and the significance of updating the file. Any data on the disk will not be preserved.

REBUILD

This section allows the user to rebuild a bad or skip sector file should one become destroyed. First the track where the selected file is located is formatted, then a zero entry file is written on that track. From this point on the procedure is in accordance with the Update section.

HELP

This is the default section. Section names are identified along with their function.

Program and Event Flags

Quick - The quick flag reduces the number of track reads from five to one.

Event Flag 23 - Causes the starting disk address to be printed for each step in a section.

Event Flag 22 - Causes the starting disk address to be printed once every 100 cylinders.

Event Flag 21 - Causes error messages to be printed in brief format.

Event Flag 20 - Causes single track transfers in the surface analysis test (stand-alone mode only).

Event Flag 19 - Causes only the FE cylinders to be formatted.

Event Flag 18 - Causes FORMAT section to bypass verification.

Format and Verify Time

Drive	Normal	Quick
RM80	33 min.	16 min.

C.8 EVRGB - RM80 FUNCTIONAL DIAGNOSTIC

The program contains a set of 40 tests which verify the integrity of the controller and drives under test. The set of tests includes: data transfer tests, seek tests, timing tests and manual intervention tests. The tests require that the drive be online. Test 40 is a manual intervention test which is invoked by running the section called MANUAL.

C.9 EVRAA - RM DISK RELIABILITY TEST

The program requires that a formatted pack (or HDA) be on each drive under test. The packs should not be "mounted." Each pack must have a volume name of SCRATCH or DIAGNOSTIC. If either name is not recorded on the pack's home block, the program will abort any further activities on all drives. If the pack is not formatted or it is desired to run the test using a pack with some other volume name, then the appropriate formatter program must be run first. The formatter program will give the volume a name of SCRATCH after the format operation is complete.

The following paragraphs describe the various sections to this diagnostic. Only one section is run for each START.

QUALIFICATION

This section will issue each of the drive functions to ensure that the drive(s) under test will support all of the drive commands. After all non-data transfer functions have been tested the test will issue a write, write-check and read sequence to a group of disk addresses. The goal of the read/write portion of this test is to access a sector on every cylinder of every track without destroying the homeblock or the bad block file located on the last track of the last cylinder. The test must complete in less than a minute.

SEEK TIMING

This section will perform seeks between cylinder 0 and following cylinders: 1, 2, 4, 8, 16, 32, 64, 128, 256 and last cylinder. Each seek range is timed and an average time is calculated. The results are presented.

MEDIA TEST

This section will write and write check every sector on the disk using an entire track for each operation. Any block in error will not be reported if it is in the bad block file located on the last track of the last cylinder. Five patterns are written onto each sector over the entire disk pack. Each pattern consists of a quadword which is replicated 64 times in each sector. The patterns used are:

1. F00FF00FF00FF00F ;worst case for RH780
2. EC6DEC6DEC6DEC6D ;worst case for media
3. A5A5A5A5A5A5A5A5 ;alternating ones and zeros
4. 123456789ABCDEF0
5. FEDCBA9876543210

After all sectors have been written using the above patterns, the test enters a random mode where random patterns are written to random disk addresses.

MULTI-DRIVE TEST

This section will test up to eight drives by transferring random data to random disk addresses for all selected drives at the same time. That is, all transfers are issued in parallel for those drives attached to the controller. The function sequence is:

1. Drive clear
2. Write random data
3. Write check data
4. Read data
5. Data compare

NOCUSTOMER TEST

This test is the same as the multi-drive test with this exception: on an RM80 fixed media drive, the entire physical area of the media--not just the FE cylinders--is used.

CONVERSATION MODE

The conversation mode section is a set of routines designed to allow the user to design and run simple tests with a minimum of difficulty. The program prompts the user on the information needed to customize the test. Data pattern code 3 selects random data. Functions may be a sequence of READ, WRITE, etc. and must end with END.

Running default disk addresses will eventually destroy the homeblock and the bad sector file. Errors occuring in sectors which are flagged in the bad sector file are not inhibited as is the case with the multi-drive test.

Appendix D

FAULT SYMPTOMS AND CAUSES

There are three symptoms that are easily observed (do not require special instruments) by the installing technician: Fault LED ON or blinking, impossible to read controller registers from console and diagnostics produce random errors.

SYMPTOM	POSSIBLE CAUSE
Fault LED ON	D.1, D.8, D.6, D.7
Fault LED Blinking	D.5
Controller Registers can not be addressed or return unexpected data.	D.1, D.2, D.3
Diagnostics produce hard and repeatable errors.	D.1, D.4, D.2
Diagnostics produce random errors.	D.2, D.1

D.1 SBI Coaxial Cables

An improperly installed or faulty SBI coaxial cable can be indicated by a range of symptoms from the inability of the controller to pass self-test to the intermittent failure of diagnostics.

D.1.1 Improperly Installed SBI Cables

The header for each SBI coax cable is designed to insure that a pin is not bent when the header is misaligned. The header will allow a pair of pins to be open above or below the header, as well as an entire row to the left or right of the header. A very careful visual check with a flashlight, while power is off, is strongly advised before power is applied after installation and at the first sign of trouble.

D.1.2 Open Coaxial Cables

The coaxial cable assemblies are subject to internal failure from fatigue or mishandling. If a conductor in one of the cables becomes open, the corresponding signal will not be propagated past the break. A missing signal may prevent the controller from completing self-test or cause errors during verification exercises. A broken line downstream of the V-MASTER will also prevent proper termination of that line.

If the controller does not pass self-test (Fault LED ON), the clocks from the SBI bus may not be received. Connector J2, pin 8 on the SC780 should be checked with an oscilloscope and show a 150 ns period. J2 is accessible from the front with the controller plugged into the V-MASTER. J2 is the top of two sets of pins with pin 8 being the fourth pin up on the side closest to the outside. This clock is logically derived on the translator board (SU7810402) from the four clock lines of the SBI bus. The most common cause for bad clocks are incorrectly installed SBI cables or terminator (see paragraph 2).

If the diagnostics run with intermittent and random failures, the cause may be related to improper termination of the SBI. Both ends of the SBI bus have PULL UP/PULL DOWN termination resistors: at the extreme left end the resistors are on a module of the CPU and at the extreme right on a terminator board. Every line on the bus but the four clock lines (PDCLK H/L and PCLK H/L) should measure 37 ohms to ground. If 72 ohms is measured it would indicate that the line is connected to only one of the two terminators. The clocks are terminated only at the terminator (right) end and should show 72 ohms to ground. The SBI signal lines are identified on the V-MASTER backplane in Tables D-1 and D-2 for the Bus Interface Board slot and the Bus Translator Board slot, respectively.

D.2 Terminator Problems

If the terminator is improperly installed diagnostics may produce intermittent errors. If problems are observed, check to make sure that the terminator is properly seated on the bus out pins of the V-MASTER backplane (Emulex terminator) or that the coaxial cables are properly installed on the DEC terminator (see D.1 above). If the visual checks are satisfactory and a terminator problem is still suspected, the following checks will help to isolate the problems. Also, check to insure that there are no broken coaxial cables as described in paragraph D.1.2.

The terminator receives it's power from the main frame power supply. J7, pin 1 on the terminator should measure +5 vDC to ground and J7, pin 3 should measure -5.2V. J7, pin 2 and J7, pin 4 are system ground.

The main frame power supplies also provide to the terminal an "AC LOW" signal which can be measured on the terminator at J8, pin 1 and J9, pin 1 at -10 vDC, and "DC LOW" at J8, pin 2 and J9, pin 2 at -10 vDC. J8, pin 3 and J9, pin 3 are system ground. The signal derived from the DC LOW is "BUS SBI DEAD L" and should have a level of at least +2 v (TTL high) at B60 of slot 2 (Translator Board) of all V-masters in the system.

The signal "BUS SBI FAIL L" is derived on the terminator from "AC LOW" and should be at +2 v (TTL high) at SBI connector J3 - TT (second from the bottom).

D.3 Interface or Translator Board Malfunction

If the controller does not respond when addressed from the console, the problem may lie with the Interface or Translator PCBAs rather than with the controller. The data and address paths through those boards may be verified by following the following procedure.

Place the controller(s) in slots 3 (and 4) of the V-MASTER in forced reset (SW4-1 ON). When the controller(s) are unable to respond to addresses on the V-MASTER's internal bus, the address associated with the Examine of a controller register is echoed back to the console as data. For example:

```
>>> E/L/P 20014414
    P  20014414   F0F28414
```

This is an Examine of the Disk Address Register of drive zero (offset = 414) on TR10 (20014000). The translator board converts the SBI address to an address which is compatible with the V-MASTER's VMI bus. If the controller is in slot 3 of the V-MASTER, the address will be converted to F0F28XXX. The LS three digits of the SBI address are passed through unchanged. With the controller reset and unable to respond, the "data" read by the examine is F0F28414.

If the controller is in slot 4 (SW3-8 ON), the SBI address will be translated to F0F2AXXX. Of course, the SBI address used to access the V-MASTER is dependent on the TR level that the Interface Board is configured to. Remember that, if there are two controllers in the V-MASTER, the even TR will be associated with the controller in slot 3 and the odd with the controller is slot 4.

The purpose of this exercise is to determine whether or not the SBI address is being translated properly. A controller in the V-MASTER would not be expected to respond if this did not happening.

In the event that you are unable to successfully examine a controller register, the CPU internal registers should be examined to determine the type of failure:

```
>>> E/I 30
       30   00040000

>>> E/I 34
       34   00008002 (or 00000002)
```

The above responses indicate no error status.

Internal Register 30, bit 31 (MSB) indicates SBI parity error; bit 29 = unexpected read data; bit 27 = multi-transmitter fault; bit 26 = transmit fault; bit 17 = fault signal.

Internal Register 34, bit 8 indicates central processor confirmation response; bit 6 = bus time out.

Internal Register 30 can be cleared by a deposit of "F0000":

```
>>> D/I 30 F0000
```

Internal Register 34 can be cleared by a deposit of "FFFF":

```
>>> D/I 34 FFFF
```

D.4 Reversed B Cable

Read data failures from the drive could be caused by reversed "B" cable. With the drive cycled down, remove the "A" cable and the fault light on the controller should blink. If not, the "B" cable is probably in backwards on one end.

D.5 Drive Problems

A blinking Fault LED is a indication that no disk drive is cabled in and powered up.

A slow blinking Fault LED indicates that two disc drives are assigned the same drive number. The number plug or switch setting must be changed on the disk drive.

D.6 No -5.2 vDC

The -5.2 vDC line from the main frame power supply may not be cabled properly to the V-MASTER chassis. Check on the backplane J15, pin 1 relative to J15, pin 2 for this voltage. This voltage can also be checked at pin C82 + C79 of the Bus Interface slot (slot 1), and C79 of the Translator slot (slot 2).

D.7 AC and DC Low Asserted

AC and DC low signals from the power supply may not be pulled to a logical "OK" state of -7 vDC by the power supply. Check these voltages on the back plane at J14, pin 1 (PS ACLO H) and J14, pin 2 (PS DCLO H) which are also etched to J13, pins 1 and 2, respectively. Pin 3 is ground on both J13 and J14.

D.8 Cable Paddle Board Not Installed or Incorrectly Installed

Minus 5 vDC is supplied by the power converter pack on the rear mounted adaptor board. The SELT-TEST firmware of the controller, which starts on power up, looks for -5 vDC as part of it's test. The Fault LED will stay on until all tests pass correctly. Check to insure that the backplane pins are aligned with the board socket and that the board is inserted flush to the backplane surface. The -5 vDC can be measured at B91 on the backplane of the controller or pin 9 of ICs U1 through U5 on the cable paddle board.

TABLE D-1
SU78 BUS INTERFACE BOARD
PIN LIST

A			B			C		
1	2		1	2		1	2	BUS SBI REQ 4 L
3	4	BUS SBI B00 L	3	4	BUS SBI B20 L	3	4	BUS SBI REQ 7 L
5	6	BUS SBI B01 L	5	6	BUS SBI B23 L	5	6	BUS SBI REQ 5 L
7	8		7	8	BUS SBI B21 L	7	8	BUS SBI TP L
9	10	BUS SBI B02 L	9	10		9	10	
11	12		11	12	BUS SBI B22 L	11	12	BUS SBI REQ 6 L
13	14		13	14		13	14	BUS SBI PCLK H
15	16	BUS SBI B03 L	15	16		15	16	BUS SBI TP H
17	18		17	18		17	18	
19	20		19	20		19	20	BUS SBI PDCLK L
21	22		21	22	BUS SBI B24 L	21	22	BUS SBI PCLK L
23	24		23	24		23	24	
25	26	BUS SBI B04 L	25	26	BUS SBI B27 L	25	26	BUS SBI PDCLK L
27	28	BUS SBI B07 L	27	28	BUS SBI B25 L	27	28	
29	30	BUS SBI B05 L	29	30	BUS SBI B28 L	29	30	
31	32	BUS SBI B08 L	31	32	BUS SBI B26 L	31	32	
33	34	BUS SBI B06 L	33	34	BUS SBI B29 L	33	34	BUS SBI UNJAM L
35	36	BUS SBI B09 L	35	36	BUS SBI B30 L	35	36	BUS SBI CONFO L
37	38		37	38		37	38	BUS SBI FAULT L
39	40	BUS SBI B10 L	39	40	BUS SBI B31 L	39	40	BUS SBI CONFI L
41	42	BUS SBI B11 L	41	42		41	42	
43	44		43	44		43	44	
45	46		45	46		45	46	
47	48		47	48		47	48	
49	50		49	50		49	50	
51	52		51	52		51	52	
53	54		53	54		53	54	
55	56		55	56		55	56	
57	58		57	58		57	58	
59	60		59	60	BUS SBI M0 L	59	60	
61	62		61	62	BUS SBI M1 L	61	62	
63	64	BUS SBI B12 L	63	64	BUS SBI M3 L	63	64	
65	66	BUS SBI B14 L	65	66	BUS SBI M2 L	65	66	
67	68		67	68	BUS SBI P0 L	67	68	
69	70	BUS SBI B13 L	69	70		69	70	
71	72		71	72		71	72	
73	74	BUS SBI B15 L	73	74	BUS SBI P1 L	73	74	
75	76		75	76		75	76	
77	78		77	78	BUS SBI TAG 0 L	77	78	
79	80		79	80	BUS SBI ID 0 L	79	80	
81	82		81	82	BUS SBI TAG 1 L	81	82	
83	84		83	84	BUS SBI ID 1 L	83	84	
85	86	BUS SBI B16 L	85	86	BUS SBI TAG 2 L	85	86	
87	88		87	88	BUS SBI ID 2 L	87	88	
89	90	BUS SBI B17 L	89	90	BUS SBI ID 3 L	89	90	
91	92	BUS SBI B18 L	91	92	BUS SBI ID 4 L	91	92	
93	94	BUS SBI B19 L	93	94		93	94	

TABLE D-2
SU78 BUS TRANSLATOR BOARD
PIN LIST

A	B	C	
1 2	1 2	1 2	
3 4	3 4	3 4	
5 6	5 6	5 6	
7 8	7 8	7 8	
9 10	9 10	9 10	
11 12	11 12	11 12	
13 14	13 14	13 14	
15 16	15 16	15 16	
17 18	17 18	17 18	
19 20	19 20	19 20	
21 22	21 22	21 22	
23 24	23 24	23 24	
25 26	25 26	25 26	
27 28	27 28	27 28	
29 30	29 30	29 30	
31 32	31 32	31 32	
33 34	33 34	33 34	
35 36	35 36	35 36	
37 38	37 38	37 38	
39 40	39 40	39 40	
41 42	41 42	41 42	
43 44	43 44	43 44	
45 46	45 46	45 46	
47 48	47 48	47 48	
49 50	49 50	49 50	
51 52	51 52	51 52	
53 54	53 54	53 54	
55 56	55 56	55 56	
57 58	57 58	57 58	BUS SBI TR01 L
59 60	59 60	59 60	BUS SBI TR00 L
61 62	61 62	61 62	BUS SBI TR03 L
63 64	63 64	63 64	BUS SBI TR02 L
65 66	65 66	65 66	BUS SBI TR04 L
67 68	67 68	67 68	BUS SBI TR05 L
69 70	69 70	69 70	BUS SBI TR06 L
71 72	71 72	71 72	
73 74	73 74	73 74	BUS SBI TR07 L
75 76	75 76	75 76	BUS SBI TR08 L
77 78	77 78	77 78	
79 80	79 80	79 80	BUS SBI TR09 L
81 82	81 82	81 82	BUS SBI TR10 L
83 84	83 84	83 84	BUS SBI TR11 L
85 86	85 86	85 86	
87 88	87 88	87 88	
89 90	89 90	89 90	
91 92	91 92	91 92	
93 94	93 94	93 94	

Appendix E

VAX NUMBERS QUICK REFERENCE

780 Base Address	750 Base Address
20008000 - TR4	F28000 MBA 0
2000A000 - TR5	F2A000 MBA 1
2000C000 - TR6	F2C000 MBA 2
2000E000 - TR7	
20010000 - TR8	
20012000 - TR9	
20014000 - TR10	
20016000 - TR11	

Internal Register Byte Offsets (Hex)

00 - MBA Configuration/Status Register (MBA CSR) [780 only]
04 - MBA Control Register (MBACR)
08 - MBA Status Register (MBASR)
0C - MBA Virtual Address Register (MBAVAR)
10 - MBA Byte Count Register (MBABCR)
14 - MBA Diagnostic Register (MBADR)
18 - MBA Selected Map Register (MBASMR) [780 only]
1C - MBA Command Address Register (MBACAR)

800 to BFC - MBA Map Registers

External (Drive) Register Byte Offsets (Hex)

Register	0	1	2	3	4	5	6	7
Control/Status1 - RMCS1	400	480	500	580	600	680	700	780
Drive Status - RMDS	404	484	504	584	604	684	704	784
Error 1 - RMER1	408	488	508	588	608	688	708	788
Maintenance1 - RMMR1	40C	48C	50C	58C	60C	68C	70C	78C
Attention Summary - RMAS	410	490	510	590	610	690	710	790
Disk Address - RMDA	414	494	514	594	614	694	714	794
Drive Type - RMDT	418	498	518	598	618	698	718	798
Look Ahead - RMLA	41C	49C	51C	59C	61C	69C	71C	79C
Serial Number - RMSN	420	4A0	520	5A0	620	6A0	720	7A0
Offset - RMOF	424	4A4	524	5A4	624	6A4	724	7A4
Desired Cylinder - RMDC	428	4A8	528	5A8	628	6A8	728	7A8
Holding - RMHR	42C	4AC	52C	5AC	62C	6AC	72C	7AC
Maintenance 2 - RMMR2	430	4B0	530	5B0	630	6B0	730	7B0
Error 2 - RMER2	434	4B4	534	5B4	634	6B4	734	7B4
ECC Position - RMEC1	438	4B8	538	5B8	638	6B8	738	7B8
ECC Pattern - RMEC2	43C	4BC	53C	5BC	63C	6BC	73C	7BC

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