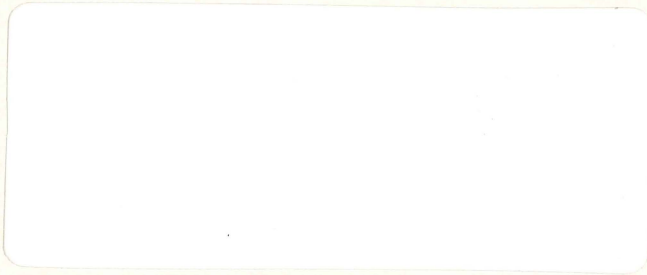# pdp11

**TMB11/TU10W
DECmagtape system
maintenance manual
(TMB11-E/F system)**

digital

TMB11/TU10W
DECmagtape system
maintenance manual
(TMB11-E/F system)

digital equipment corporation • maynard, massachusetts

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

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CONTENTS (CONT)

CONTENTS (CONT)

CONTENTS (CONT)

FIGURES

FIGURES (CONT)

FIGURES (CONT)

FIGURES (CONT)

TABLES

PREFACE

Chapters 1 through 5 of the *TMB11/TU10W DECmagtape System Maintenance Manual* cover the description, installation, operation, and maintenance of the TMB11/TU10W as a system. Chapters 6, 7, and 8 describe the theory of operation of the TMB11 Controller, M8926 Interface Module, and the TU10W Tape Transport. These chapters describe the respective units in detail, with only general references to other areas of the system. They contain functional block diagrams and flow diagrams to illustrate the operational sequences occurring within these units. A glossary of the symbology used in the flow diagrams is contained in Appendix C.
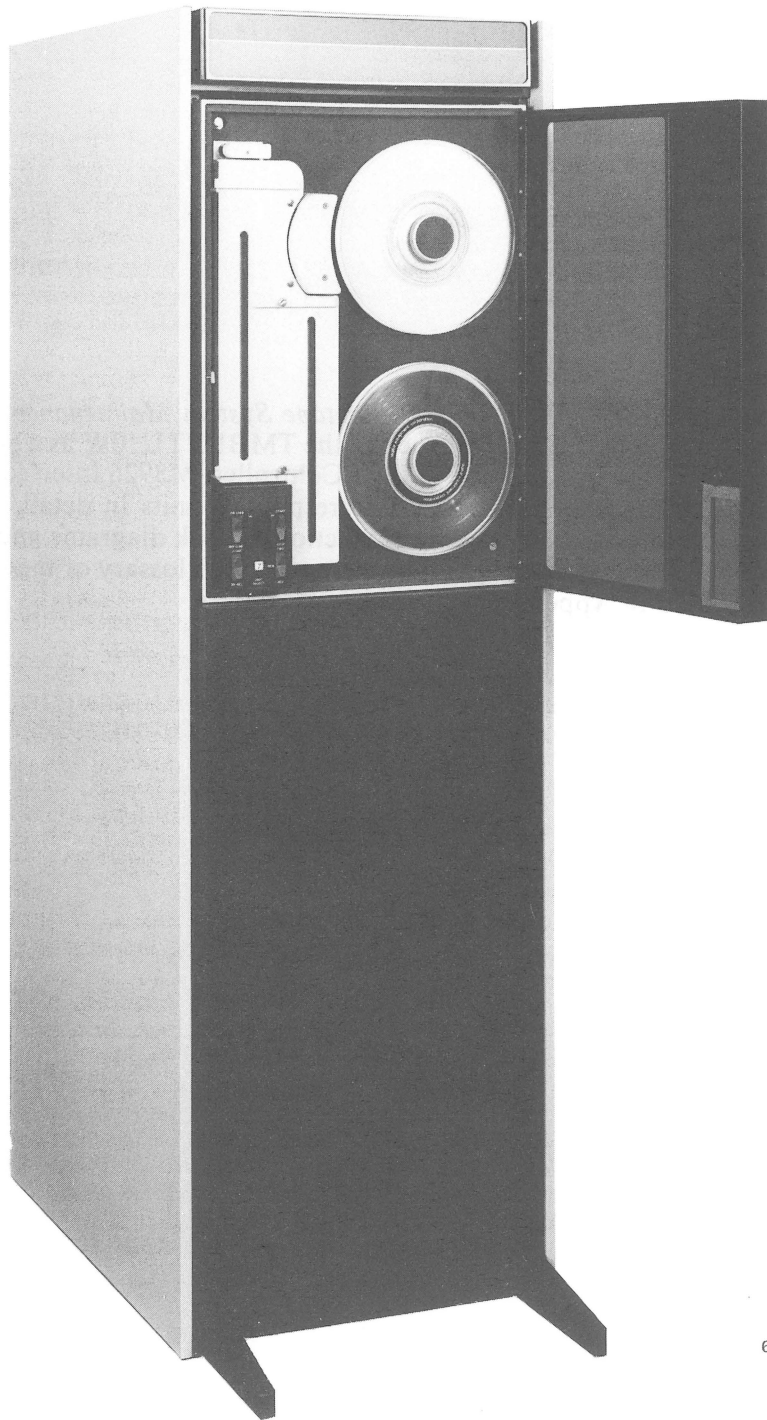
6999-2

TMB11/TU10W DECmagtape System

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The TMB11-EX/FX* DECmagtape System (TMB11/TU10W†) is a magnetic tape storage system that interfaces with the PDP-11 family of processors and peripherals and provides storage for digital information. The system reads and records digital data in a forward direction in an industry-compatible NRZI format at a maximum data transfer rate of 36,000 tape characters per second. Tape density and tape character format are program selectable. Forward/reverse tape speed is 114 cm (45 inches) per second while rewind is performed at 381 cm (150 inches) per second. The TMB11/TU10W Tape Drive System has forward and reverse spacing capability.

1.2 GENERAL DESCRIPTION

1.2.1 System Configuration

The basic TMB11/TU10W DECmagtape System configuration is a TMB11 Controller and a TU10W Master Tape Transport. From one to seven "slave" transports may be added to make a maximum possible configuration of one TMB11 Controller and eight tape transports. The master tape transport is composed of a "host" transport and an M8926 Interface module. The M8926 interfaces the "host" transport and the slave transports (if any) to the TMB11 via the BC11A master bus cable. All the tape transports are "daisy chained" on the slave bus, making them essentially parallel with each other. Figure 1-1 is an illustration of the TMB11/TU10W system configuration.

1.2.2 Physical Description

The TMB11 consists of the following six modules:

1. M105 Address Selector Module
2. M795 Word Count and Bus Address Module
3. M796 Unibus Master Control
4. M7821 Interrupt Control Module
5. M7911 Tape Drive Interface
6. M7912 TMB11 Unibus Registers

---

*The TMB11-EX is a 9-track system. The TMB11-FX is a 7-track system. "X" specifies the system voltage and frequency requirements (Table 1-1).

†The TMB11-EX/FX system is commonly referred to by its component subunits, the TMB11 and TU10W, hence the manual title *TMB11/TU10W DECmagtape System Maintenance Manual*. Within this manual, the system is referred to as the TMB11/TU10W.
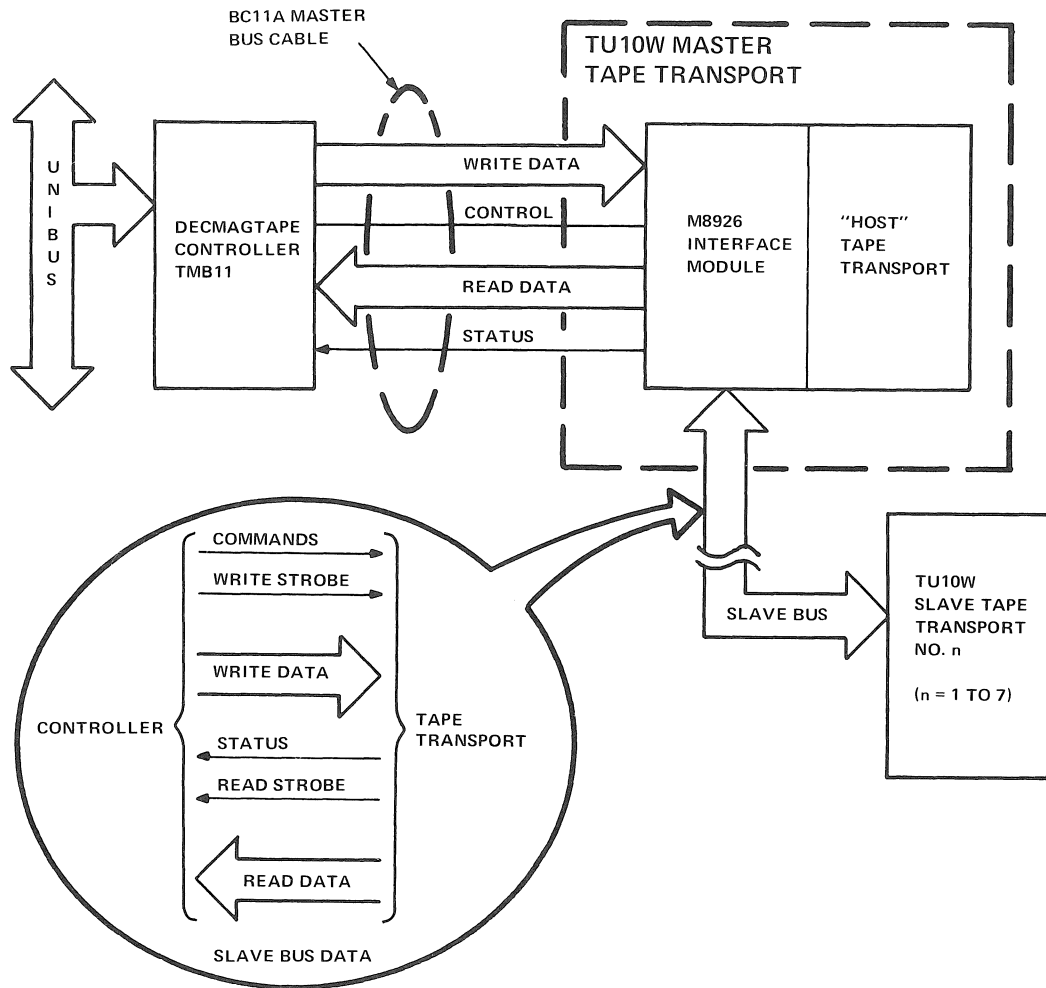
Figure 1-1   TMB11/TU10W Tape Drive System Configuration

The six modules are plugged into a TMB11 system unit that is mounted in an expander box (Figure 1-2). Unibus input, Unibus output, and tape transport cabling also connect to the system unit. The TMB11 Controller interfaces the DECmagtape system to the PDP-11 Unibus. It controls data transfers, issues control commands to the TU10W master, and monitors system operation. Each TMB11 can control one master transport and up to seven slave transports.

The TU10W Tape Transport is contained in a single 48.3-cm (19-inch) cabinet along with an 861 Power Controller (Figure 1-3). Figures 1-4 and 1-5 illustrate front, rear, and side views of the transport and identify many of the TU10W components and subassemblies.
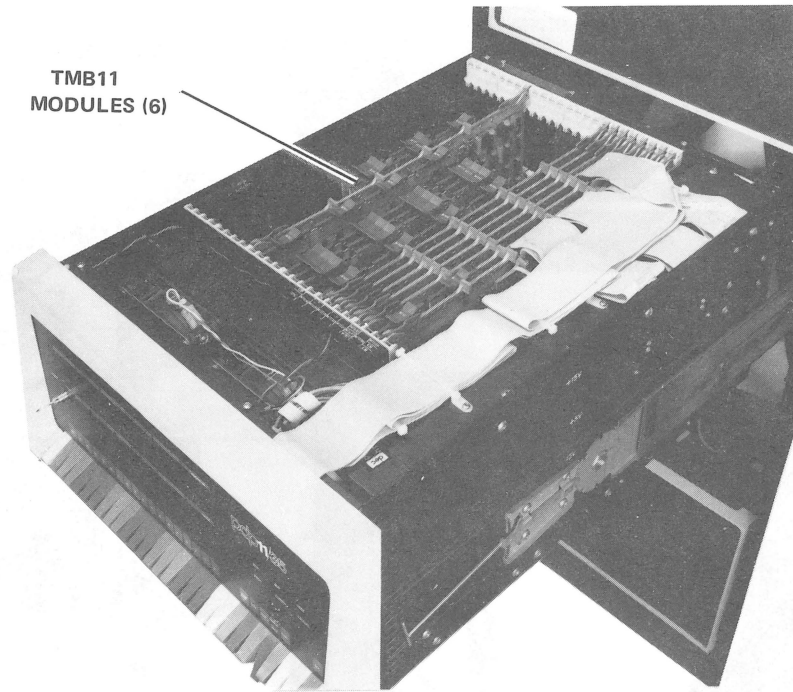
TMB11
MODULES (6)

7941-6

a. Installed in BA11K Expander Box
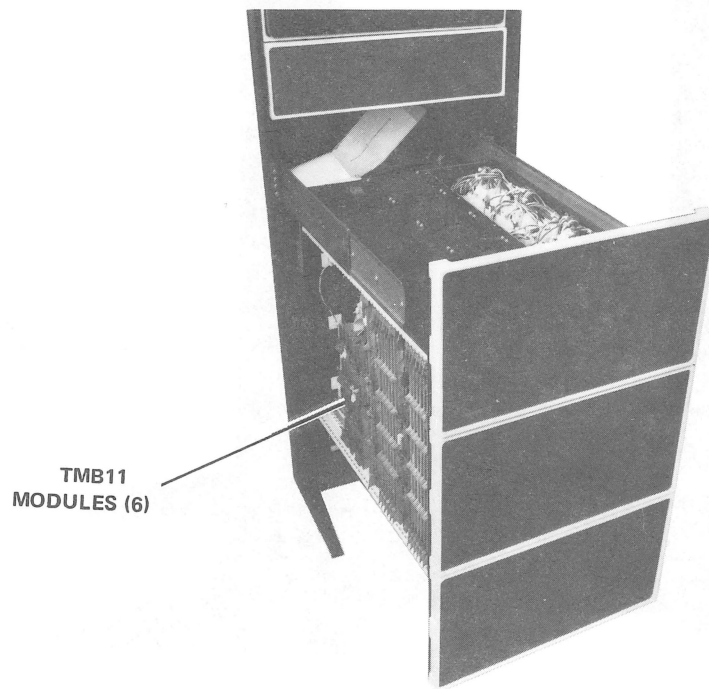
TMB11
MODULES (6)

7997-2

b. Installed in BA11F Expander Box

Figure 1-2 TMB11 Controller

1-3

TAPE TRANSPORT

VACUUM MOTOR

861 POWER CONTROLLER
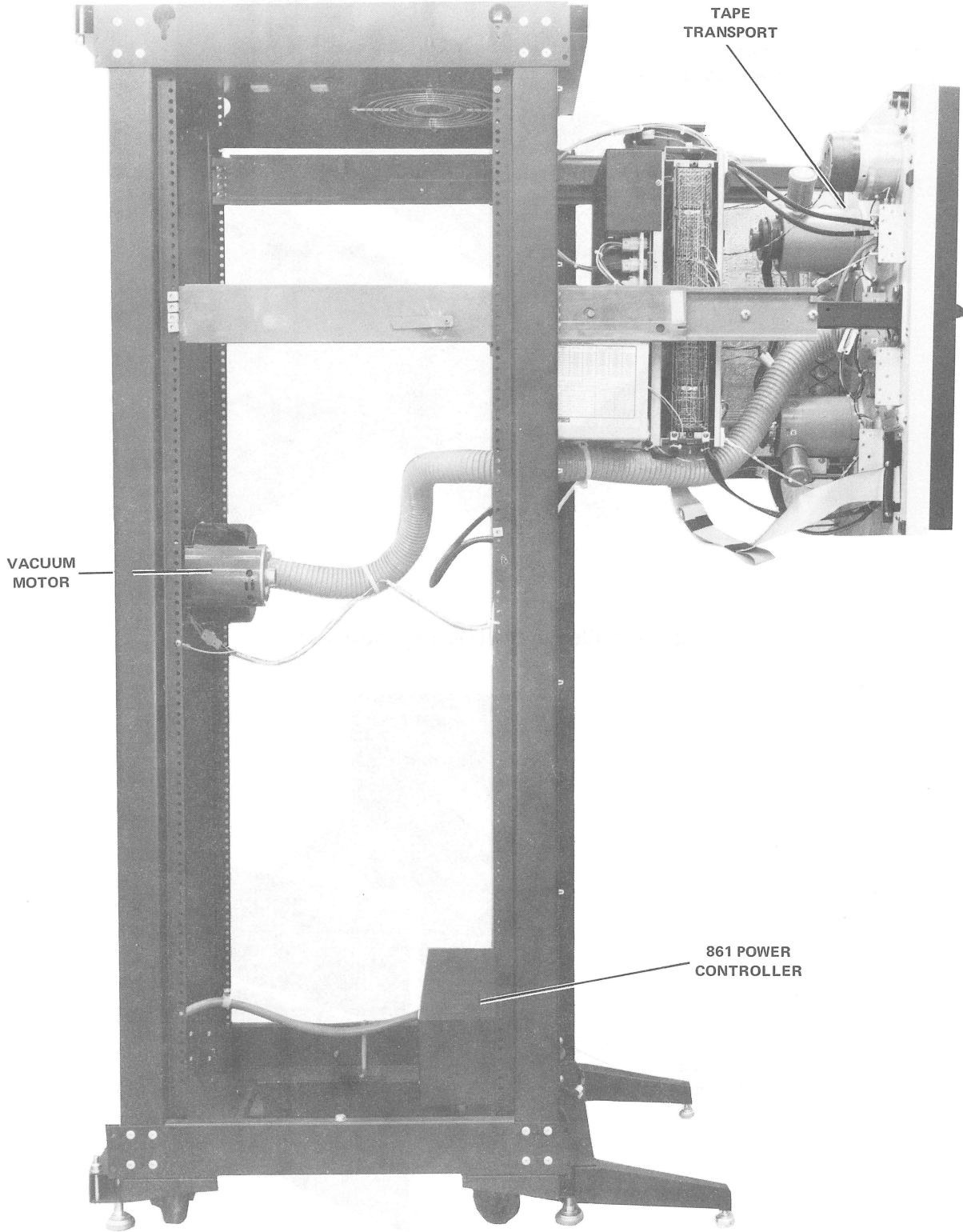
8209-4

Figure 1-3   TU10W with Transport Extended
and Side Panels Removed

TRANSPORT
SERVICE
LOCK

CAPSTAN

VACUUM DOOR
(OPEN)

TAPE CLEANER

HEAD PLATE ASSEMBLY
(COVER REMOVED)

EOT/BOT
ASSEMBLY

CONTROL PANEL

TRANSPORT
SERVICE
LOCK

7660-22-A0580

a. Front View

CABINET FAN

LOGIC ASSEMBLY
FAN

POWER SUPPLY
REGULATOR BOARD

DANGER
HIGH
VOLTAGE

SHIPPING
BRACKETS

VACUUM HOSE

TRANSFORMER/CAPACITOR
ASSEMBLY

8209-9
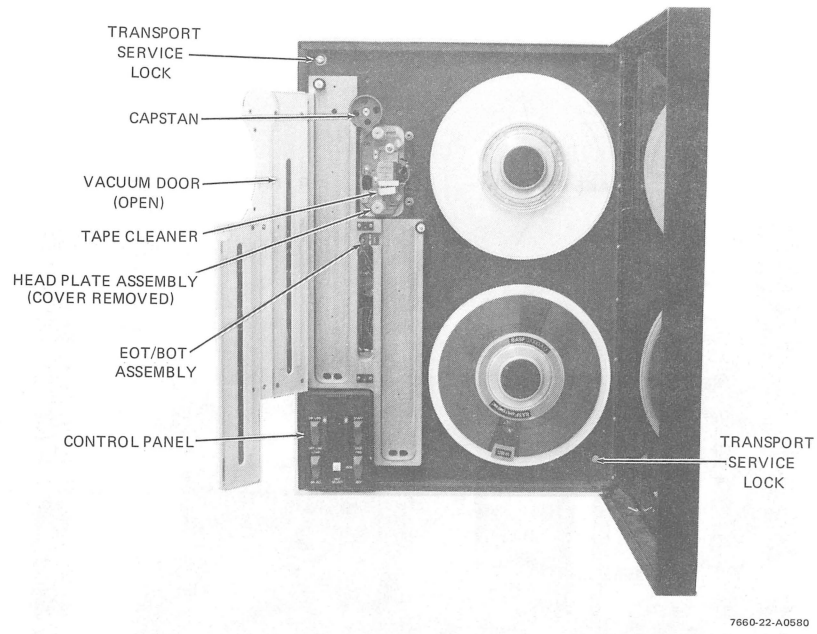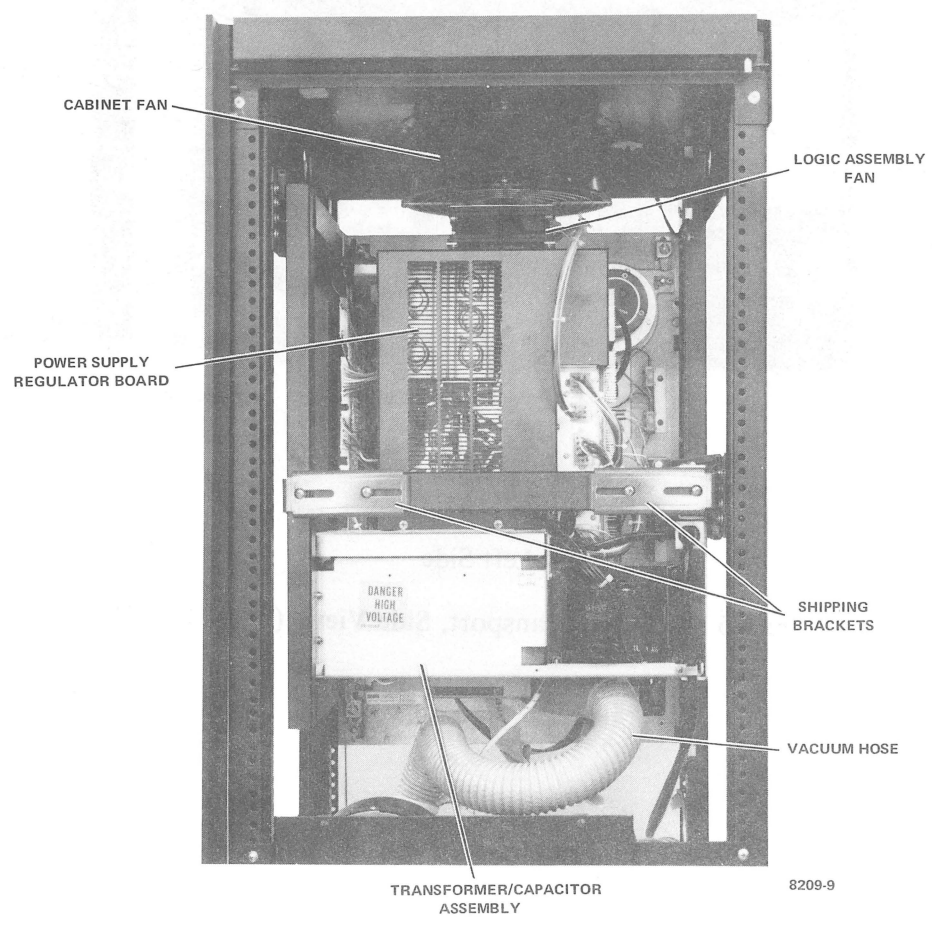
b.   Rear View

Figure 1-4   TU10W Transport, Front and Rear Views

LOGIC FAN ASSEMBLY

BRAKE ASSEMBLY

AIR FILTER

TACHOMETER

SERVICE LOCK

CAPSTAN MOTOR

H606 POWER BOARD

LOGIC BACKPLANE ASSEMBLY

TAKE-UP REEL MOTOR

VACUUM SWITCHES

POWER SUPPLY REGULATOR BOARD

FILE REEL MOTOR

VACUUM SWITCHES

TRANSFORMER-CAPACITOR ASSEMBLY

VACUUM HOSE (TO VACUUM MOTOR)

READ/WRITE INTERLOCK

BRAKE ASSEMBLY

AIR FILTER
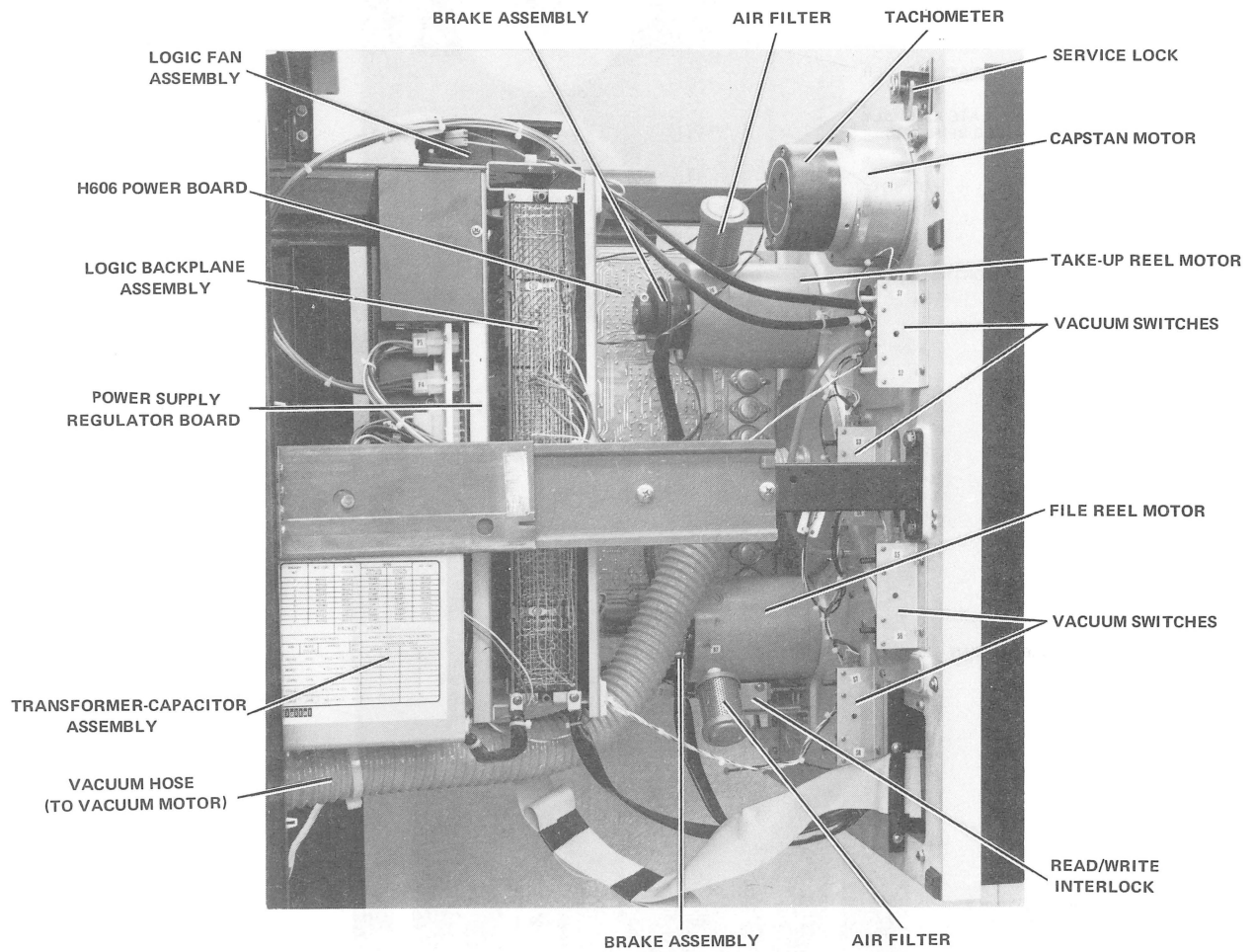
8209-5

a. Left Side

Figure 1-5   TU10W Transport, Side Views (Sheet 1 of 2)
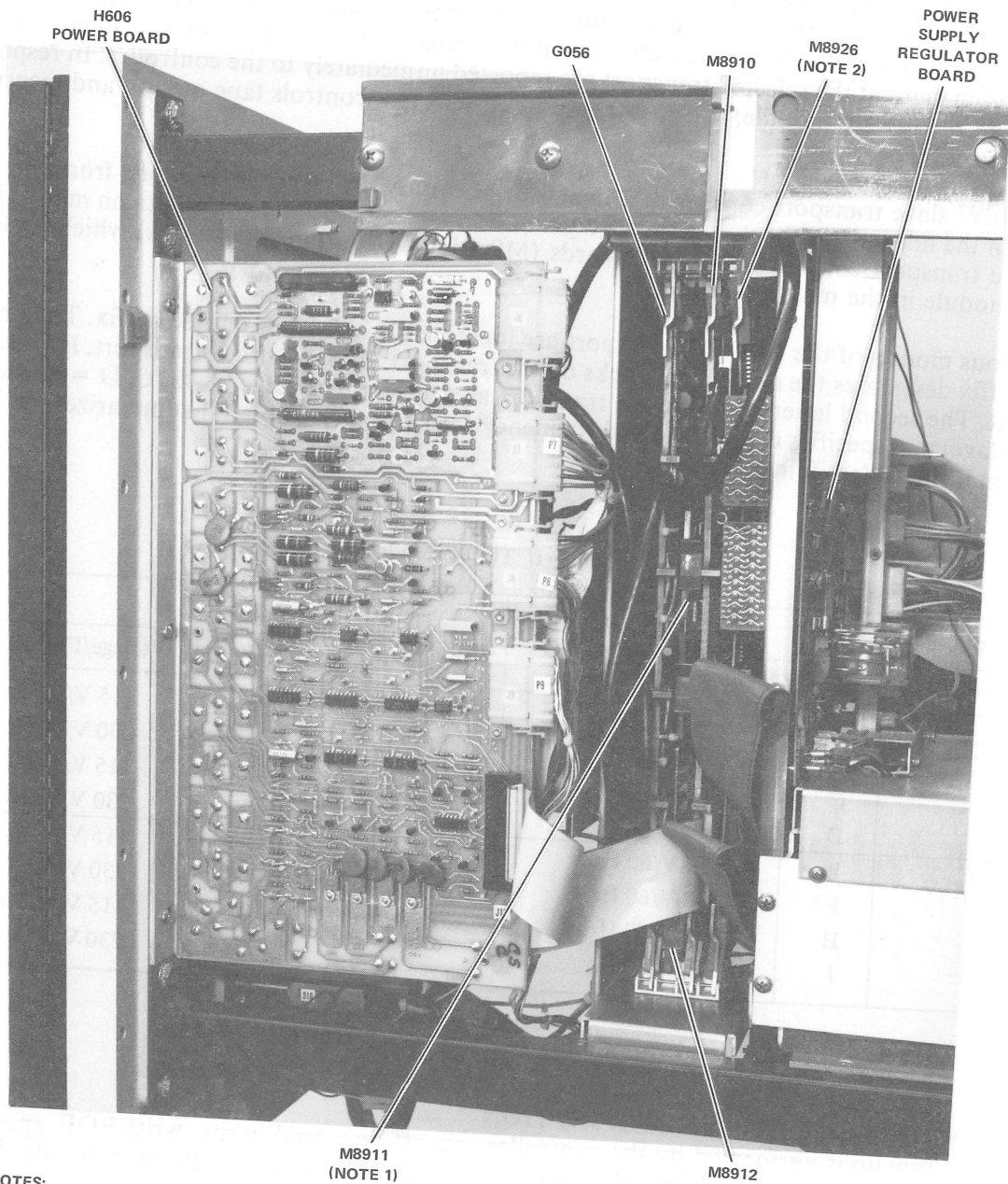
NOTES:
1. 9 track transports only. M8911-YA used for 7-track transports.
2. Master transport only. Slave transport contains cable cards M9001, M8913 and M9001-YA in this slot.

b. Right Side

Figure 1-5   TU10W Transport, Side Views (Sheet 2 of 2)

The TU10W master transport consists of an M8926 Interface module and a "host" transport. The M8926 processes commands from the controller and issues motion and read/write commands to the host and slave transports; the M8926 also monitors status lines from the host and slave transports. Any status changes at the selected transport are reported immediately to the controller. In response to inputs from the M8926 module, the host transport (if selected) controls tape motion and records and reads data on magnetic tape.

The TU10W slave transport consists of a tape transport only. In response to inputs from the M8926 module in the master transport, it controls tape motion and records and reads data on magnetic tape. The slave transport contains three cable cards (M9001, M8913, and M9001-YA) which replace the M8926 module in the master transport.

The various models of the TU10W Transport are identified by a 2-letter dashed suffix. The first letter of the suffix designates the number of tracks on the transport: E for a 9-track transport, F for a 7-track transport. The second letter identifies the transport as a master or a slave (A, B, C, D = master; E, F, H, J = slave) and specifies the voltage and frequency requirements. Table 1-1 summarizes the TU10W models and their identifying suffix.

Table 1-1   TU10W Models

TU10W-EX (9-track)			TU10W-FX (7-track)		
Master/Slave	X=	Voltage/Frequency	Master/Slave	X=	Voltage/Frequency
Master	A	115 V/60 Hz	Master	A	115 V/60 Hz
	B	230 V/60 Hz		B	230 V/60 Hz
	C	115 V/50 Hz		C	115 V/50 Hz
	D	230 V/50 Hz		D	230 V/50 Hz
Slave	E	115 V/60 Hz	Slave	E	115 V/60 Hz
	F	230 V/60 Hz		F	230 V/60 Hz
	H	115 V/50 Hz		H	115 V/50 Hz
	J	230 V/50 Hz		J	230 V/50 Hz

1.3   SYSTEM FUNCTIONAL DESCRIPTION

The basic functions performed by the controller are: off-line, read, write, write EOF, space forward, space reverse, write-with-extended-IRG, and rewind. Each of these functions is briefly described in Table 1-2.

Table 1-2 Controller Functions

Function	Description
Off-Line	The off-line function is used to return control to the tape transport so that tape can be rewound, reels changed, etc. without using processor time.
	The off-line function places the selected tape transport in the off-line (local) mode and causes it to begin a rewind operation.
	The controller cannot write on or read from the magnetic tape when the off-line function is used. Manual intervention is required to return the drive to on-line status, i.e., the ON-LINE button must be pressed.
Read	This function permits reading from the magnetic tape. During the read operation, the data portion of the record is loaded into the controller data buffer for transfer to the memory. The LRC and CRC characters are read but not transferred into memory.
Write	This function permits writing on the magnetic tape. During the write operation, data from the bus is loaded into the controller data buffer register. The controller then transfers the data to the tape transport write heads. The necessary LRC and CRC characters are generated by the master transport and written on the tape following the data. The write function advances the tape one record.
Write EOF	This function writes an end-of-file (EOF) mark on the tape. When selected, this function erases a 3-inch segment of tape prior to writing the first character. The EOF mark and the associated LRC character are considered one record. The EOF mark is an octal 23 character (9-track drive) or octal 17 character (7-track drive) followed by an octal 23 (or octal 17) LRC character.
Space Forward	This function is used to skip over a number of records to find a specific record on the tape. When selected, the space forward function causes the tape transport to advance a specified number of records. The program loads the byte record counter with the two's complement of the number of records to be spaced over. Detection of the end-of-file mark terminates a space operation.
	Space forward is used for tape positioning only and, therefore, does not affect information stored on the tape or in memory.

Table 1-2 Controller Functions (Cont)

Function	Description
Space Reverse	This function is identical to the space forward function except the tape moves in the reverse rather than in the forward direction.
Write-with-Extended-IRG	This function is identical to the write function except that a 7.62-cm (3-inch) segment of tape is erased before writing the first character.
Rewind	This function is used for rewinding the tape on the feed reel so that the tape can either be unloaded from the transport or operation can start at the beginning of the tape. When this function is used, the tape moves in the reverse direction, at a much higher speed (3.81 meters/second, 150 inches/second) than for other functions, until the beginning-of-tape (BOT) marker is detected. When the BOT marker is detected, the tape slows down and comes to a complete stop at a point beyond the BOT marker. It then moves forward until the BOT marker is again detected, which is when it comes to a final stop. Rewind is used for tape positioning only and has no effect on information stored on the tape or in the memory.

Figure 1-6 is a functional block diagram of the TMB11/TU10W DECmagtape System. The processor initiates a TMB11/TU10W operation by addressing the TMB11 registers via the address decoder and loading the operation parameters into the registers. The BUS C0-C1 bits specify an out transfer (with respect to the processor), causing SEL OUT to be asserted for the particular register addressed. As each register is selected, the processor places the appropriate data on the Unibus data lines; the data is then loaded into the register with the SEL OUT strobe. Thus, the command register receives the type of operation to be performed; the byte record count register receives the number of bytes to be transferred; and the current memory address register receives the memory address of the first byte to be transferred.

The command register selects which transport is to be involved in the transfer via the SEL 0-SEL 2 lines, supplies the function command to the command decoder which generates the required commands for the tape transport, and asserts the GO bit to the start logic. When the start logic senses that the tape transport has been selected (SELR) and is ready (TUR), it asserts SET to the M8926 Interface, which then asserts SLAVE SET PLS to the transport to start the operation. If a read, write, or space forward operation is commanded, the transport command logic asserts FOR to the tape drive system which drives the capstan servo and moves the tape forward. When the tape is up to speed, the M8926 read channels are enabled by READING and start to transfer data from the read heads to the controller. The read data from the tape transport (RD0-RD7, RDP) is checked for CRC, LRC, and vertical parity errors by the M8926 board.

If any such errors are detected, the TMB11 error logic is notified (CRCE, LRCE, VPE) for appropriate corrective action. The read data is supplied to the controller along with a read strobe (RDS), which signifies the availability of read data from the transport. RD0-RD7 are routed through transport receivers and become CHAN 0-CHAN 7.

If a read operation is commanded by the command register, the CHAN 0–CHAN 7 read data is gated to the data buffer register where it is loaded into the register by RDS. RDS also requests an NPR transfer from the NPR logic. When the request is granted, BUS BBSY is asserted by the logic along with DATA → BUS, which gates the output of the data buffer to the Unibus data bus (BUS D00–D15) via the register select output multiplexer. DATA → BUS accomplishes this by asserting either HI DATA BYTE or LO DATA BYTE from the read byte select logic according to whether the CMA register is addressing the low byte or the high byte in memory. Thus, the data byte from the data buffer will output on either BUS D00–D07 or BUS D08–D15. The next character read will output on the alternate half of the data bus. When the NPR logic receives BUS SSYN from memory, it asserts NPR CLEAR BBSY, which increments the byte record counter and the CMA register to prepare for the next transfer.

When the M8926 read logic detects the end of a record, it asserts CRCS (9-track only) and LRCS to the controller and RD CLR PLS to the motion control logic. The motion control logic asserts EMD and STOP to the drive to stop the capstan servo motor.

If a write operation is commanded by the command register, the GO bit, in addition to enabling the start operation logic, requests an NPR transfer from the NPR logic. When the request is granted, the logic asserts BUS BBSY and BUS MSYN. The memory responds with SSYN to indicate that the first data character is on the data bus (BUS D00–D15). The NPR logic asserts DATA STB 2, which loads the data character into the data buffer, thus making it available to the transport as WD0–WD7. The data character enters the data buffer via one of two gates. In the write mode CMA BIT 00 asserts either SEL LO BYTE or SEL HI BYTE, according to whether the CMA register is addressing the low byte or the high byte in memory, thereby enabling the gate corresponding to the location of the character on the data bus.

Meanwhile, the start operation logic has asserted SET to the M8926 Interface, which sends SLAVE SET PLS to the transport, causing the transport command logic to assert FOR and start the capstan servo system moving forward. When the tape is up to speed, the drive sends WRT CLK pulses to the M8926 write channels and writing of the data characters begins. WDR (write data ready) from the controller enables the write channels that transfer the write data from the controller to the write heads in the tape drive. The write channel logic produces REC pulses which record the data characters on tape via the write heads. A parity bit is generated for each character and is recorded on tape along with the character. When all the data has been transferred to tape, WDR negates, enabling the end-of-record generator which functions to place the CRC character (9-track only) and the LRC character on tape.

Each time a data character (not the CRC or LRC character) is written on tape, a WRS pulse is issued to the controller, requesting the next character to be written. The WRS pulse makes an NPR request from the NPR logic and the cycle is repeated. Note that in a write operation, the GO bit makes the first NPR request and the WRS strobes make the second and subsequent requests. After the NPR logic issues DATA STB 2, it asserts NPR CLEAR BBSY, which increments the byte record counter and the CMA register to prepare for the next transfer. When the byte record counter senses that the desired number of bytes have been transferred (written), it asserts CARRY OUT 2, which negates WDR to the transport, thereby signaling the M8926 write logic to write the end-of-record check characters (CRC and LRC).

The M8926 read logic is enabled during a write operation and reads each character approximately 3 ms after it is written. The read heads are displaced from the write heads by 3.8 mm (0.15 inches). Thus, depending on density, from 30 to 120 characters are written between the time a given character is written and read back. When the read logic detects (reads) the end of the record, it issues a CRCS (9-track only) and LRCS strobe to the controller.
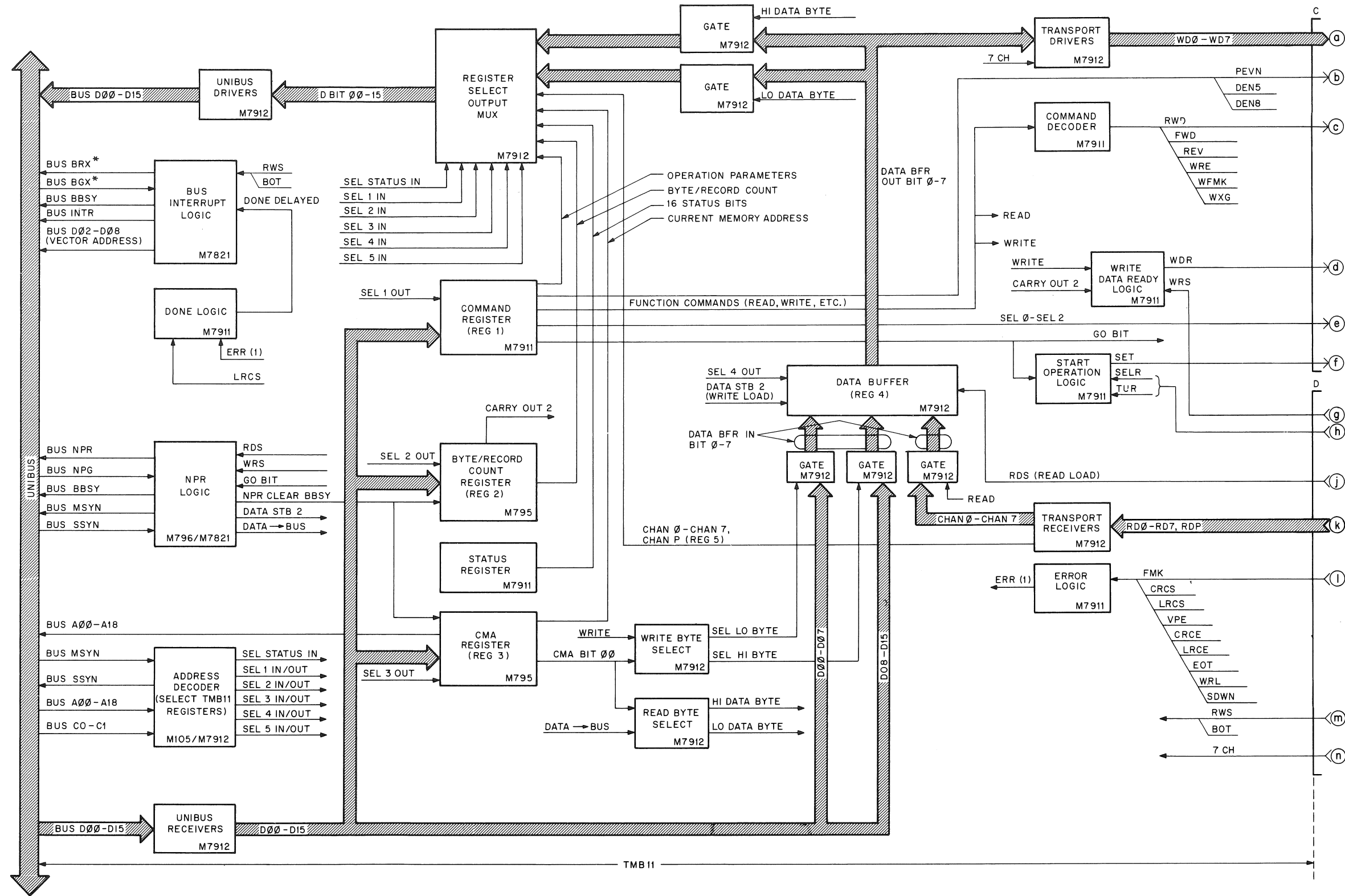
Figure 1-6 TMB11/TU10W
Functional Block Diagram
(Sheet 1 of 2)

11-3988
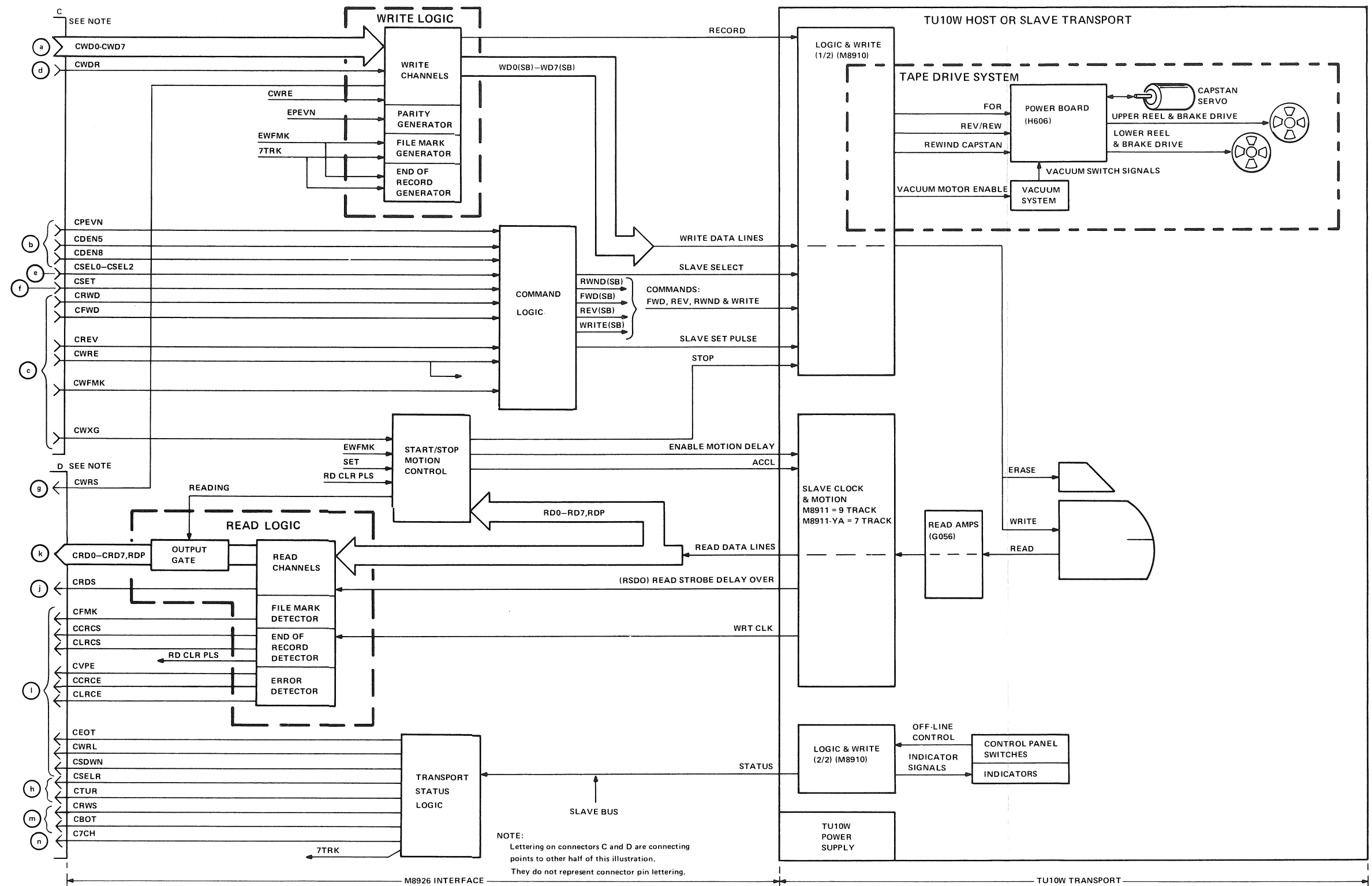
Figure 1-6 TMB11/TU10W
Functional Block Diagram
(Sheet 2 of 2)

1-13

The LRCS strobe at the end of the record indicates to the controller that the data transfer is complete. The LRCS strobe is applied to the done logic, which then asserts DONE DELAYED to the bus interrupt logic. The interrupt logic requests a bus interrupt to notify the processor that the command operation has been completed and the TMB11/TU10W is ready for another command.

The TMB11 error logic monitors transport status including parity, CRC, and LRC errors and asserts ERR (1) to the done logic if an error condition exists. Some types of errors warrant terminating an operation before it is complete while others wait until the end of the operation before asserting ERR (1).

The processor can read the TMB11 registers by addressing the registers and requesting an in-transfer (with respect to the processor) via the BUS C0–C1 bits. The address decoder then asserts SEL IN for the particular register selected; this gates the register bits out to the data bus via the register select output multiplexer.

Detailed operation of the TMB11 is given in Chapter 6 of this manual. Detailed operation of the M8926 Interface board and the TU10W Tape Transport are given in Chapters 7 and 8. Figure 1-6 can be used along with the functional block diagrams and flow diagrams contained therein.

1.4 APPLICABLE DOCUMENTS
Table 1-3 lists documents that are applicable to the TMB11/TU10W DECmagtape System.

Table 1-3 Applicable Documents

Title	Number	Description
861-A,B,C Power Controller Maintenance Manual	EK-861AB-MM-002	Contains theory of operation and maintenance instructions for the 861 Power Controller.
PDP-11 Processor and Systems Manual	*	A series of maintenance and theory manuals that provide a detailed description of the basic PDP-11 system.
PDP-11 Processor Handbook	†	A general handbook that discusses system architecture, addressing modes, the instruction set, programming techniques, and software.
PDP-11 Peripherals Handbook	112-00973-2908	A handbook devoted to a discussion of the various peripherals used with PDP-11 systems. It also provides detailed theory, flow, and logic descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces.
DIGITAL Logic Handbook, 1973–74 Edition		Presents functions and specifications of the M-series logic modules, accessories, and connectors used in the TMB11 Controller and the TU10W DECmagtape Transport. Includes other types of logic produced by DIGITAL but not used with PDP-11 devices.
Paper-Tape Software Programming Handbook	DEC-11-GGPB-D	Provides a detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming; and the floating-point and math package.

*Applicable manuals are furnished with the system at the time of installation.
 The document number depends on the specific PDP-11 family processor.

†Use the processor handbook unique to the actual CPU.

1.5 SPECIFICATIONS

Table 1-4 contains operational, environmental, mechanical, and electrical specifications for the TMB11/TU10W Tape Drive System.

Table 1-4 TMB11/TU10W Specifications

Title	Number	Description
Main Specifications	Storage medium	1.27-cm (1/2-inch) wide magnetic tape (industry-compatible)
	Capacity/tape reel	23 million characters
	Data transfer rate	36,000 char/second
	Drives/control, maximum	8
Data Organization	Number of tracks	7 or 9
	Recording density	200, 556, 800 bits/inch; program-selectable
	Interrecord gap	1.27 cm (0.5 inch) minimum; 1.65 cm (0.65 inch) nominal
	Recording method	NRZI: industry-compatible
Tape Motion	Speed (forward and reverse)	1.14 m/second (45 inches/second)
	Rewind speed	3.8 m/second (150 inches/second)
	Tape drive	Single capstan; vacuum columns
	Start/stop distance	6.3 mm (0.25 inches)
	Start/stop time	8 ms maximum
Tape Characteristics	Width	1.27 cm (0.5 inches)
	Length	731.6 m (2400 ft)
	Type	Mylar base, iron-oxide coated
	Thickness	0.038 mm (1.5 mils)
	Tension	227 g (8.0 oz)
	Reel diameter	26.7 cm (10.5 inches)
	Reel hub	9.37 cm (3.69 inches) diameter (industry standard)
Mechanical	TMB11 Controller	Mounts in a single 41.9 × 5.7 cm (16-1/2 × 2-1/4 inch) system unit
	Tape drive, mounting	Mounts on slides in a standard 48.3-cm (19-inch) cabinet

Table 1-4 TMB11/TU10W Specifications (Cont)

Title	Number	Description
Mechanical (Cont)	TU10W Transport (without cabinet)	
	Depth	0.64 m (25 inches)
	Width	0.48 m (19 inches)
	Height	0.66 m (26 inches)
	Weight	70 kg (150 lb)
	861 Power Controller	
	Depth	0.20 m (8 inches)
	Width	0.48 m (19 inches)
	Height	0.13 m (5 inches)
	Weight	4.54 kg (10 lb)
Interchannel Displacement	Write	1.9 μm (75 μin) maximum
	Read	1.9 μm (75 μin) maximum
	Erase head	Full width
Power	Input current (TMB11)	5 A at +5 Vdc
	Input current (TU10W)	8 A at 115 V; 4 A at 230 V
	Input Power (TU10W)	920 VA
	Voltage	115/230 Vac ± 10%
	Frequency	47 to 63 Hz; single phase
Operating Environment	Temperature	15° to 32° C*
	Relative humidity	20 to 80%, with maximum wet bulb 25° C and minimum dew point 2° C (no condensation)*
	Altitude	2438 m (8000 ft) maximum
Miscellaneous	BOT, EOT detection	Photoelectric sensing of reflective strip, industry-compatible
	Broken tape detection	Vacuum fail-safe
	Read/write head displacement	3.8 mm (0.15 inch)
	Electrical skew	Write deskew only. Read skew mechanically aligned

*Magnetic tape operation is more reliable if the temperature is limited to 18° to 24° C (65° to 75° F) and the relative humidity to 40 to 60%.

CHAPTER 2
UNPACKING, INSTALLATION,
AND ACCEPTANCE TESTING

2.1 SITE PLANNING AND CONSIDERATIONS

2.1.1 Space Requirements
Figure 2-1 illustrates the space and service clearances required for the TU10W cabinet. Adequate space must be provided to slide the equipment out of the rack for servicing and to open the front door on the TU10W DECmagtape Transport. The TMB11 is housed in the processor cabinet or in an expansion cabinet.

2.1.2 Power Requirements
The TMB11/TU10W DECmagtape System can be operated from a nominal 115 or 230 Vac, 50/60 Hz power source. Line voltage should be maintained to within 10 percent of the nominal value and the frequency should not vary more than 3 Hz.

2.1.3 Environmental Requirements
The TU10W DECmagtape Transport should be located in an area free of excessive dust, dirt, corrosive fumes, and vapors. To ensure proper cooling, the bottom of the cabinet and the fan inlet at the top of the cabinet must not be obstructed. The operating environment should have cool, well-filtered, humidified air; a temperature range of 15° to 27° C; and relative humidity of 40 to 60 percent.

2.2 UNPACKING
The TMB11 may be shipped in two different configurations: installed in an equipment rack or packaged separately. Unpacking and installation procedures vary depending on the system configuration. For example, if the user has ordered a complete PDP-11 system, the TMB11 is shipped installed in its appropriate rack. However, if only a part of the system is shipped because the user already has a basic PDP-11 system, then the TMB11 is shipped separately with the appropriate cables.

2.2.1 TU10W Cabinet Unpacking
To unpack the cabinet, proceed as follows:

1.   Remove the outer shipping container.

   NOTE
   **The container may be either heavy corrugated card-
   board or plywood. In either case, remove all metal
   straps first, then remove any fasteners and cleats
   securing the container to the skid. If applicable,
   remove wood framing and supports from around the
   cabinet perimeter.**

2.   Remove the polyethylene cover from the cabinet.

SWINGING DOOR
(RH) NOTE 1

SWINGING DOOR
(LH) NOTE 1

$18\frac{7}{32}"$
(46.35 cm)

REMOVABLE
END PANEL

REMOVABLE
END PANEL

$48\frac{7}{32}"$
(122.47 cm)

FAN
PORTS

CABLE ACCESS

30"
(76.2 cm)

LEVELER
4 PLACES

CASTER SWIVEL
RADIUS $2\frac{13}{32}"$
(4) CASTERS

$21\frac{11}{16}$
(54.87 cm)

TU10W EXTENDED
FROM CABINET

25"
(63.5 cm)

NOTES:
1. Door may be L.H. or R.H.
   Allow space for either case.
2. Cabinet $71\frac{7}{16}"$ (182.28 cm) high
   (floor line to cabinet top).
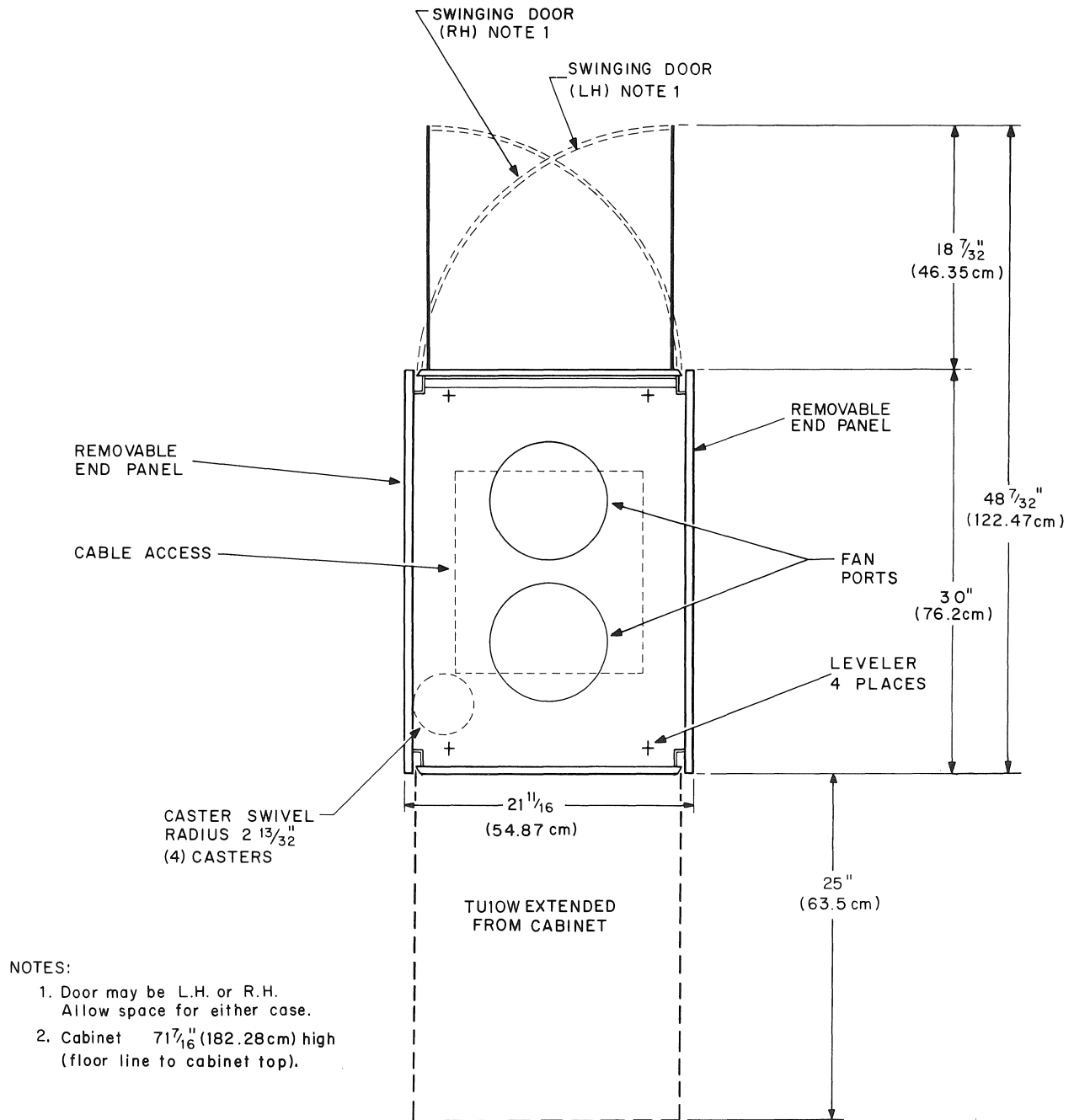
11-4800

Figure 2-1 Space and Service Clearance, Top View

3. Unbolt cabinet(s) from the shipping skid. The bolts are located on the lower supporting side rails and are exposed by opening the access door(s). Remove the bolts.

4. Raise the leveling feet above the level of the roll-around casters.

5. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.

6. Roll the system to the proper location for installation.

2.2.2 TMB11 Unpacking
Before unpacking the TMB11 Controller, check the shipping list to ensure that the correct number of packages has been received. Check the shipping list for the correct TMB11 module types. Carefully remove each device from its shipping carton.

2.3 INSPECTION
After removing the equipment from its container(s), inspect it and report any damage to the responsible shipper and the local DIGITAL Sales Office. Inspect as follows:

1. Inspect all switches, indicators, and panels for damage.

2. Remove equipment covers where necessary and inspect for loose or broken modules, blower or fan damage, and loose nuts, bolts, screws, etc.

3. Inspect the wiring side of logic panels for bent pins, broken wires, loose external components, and foreign material.

4. Check the TU10W Transport(s) for any foreign material that may have lodged in the reel hubs or other moving parts.

5. Check the TU10W power supply for proper seating of fuses and power connectors.

6. Inspect each TMB11 module for shipping damage.

2.4 TU10W CABINET INSTALLATION
To install the TU10W cabinet, proceed as follows:

1. Lower the leveling feet so that the cabinet is resting on the floor, not on the roll-around casters.

2. Use a spirit level to level the cabinet; ensure that all leveling feet are firmly on the floor.

3. Remove the shipping screws that secure the equipment to the cabinet.

4. If two or more cabinets are to be bolted together, install filler strips (P/N H952-G) between the cabinets as shown in Figure 2-2. Tighten the bolts that secure the cabinet groups together and then recheck that the cabinets are level.

71 7/16

20 1/4

.30

FILLER STRIPS

NOTE:
ALL DIMENSIONS IN INCHES

15-0098
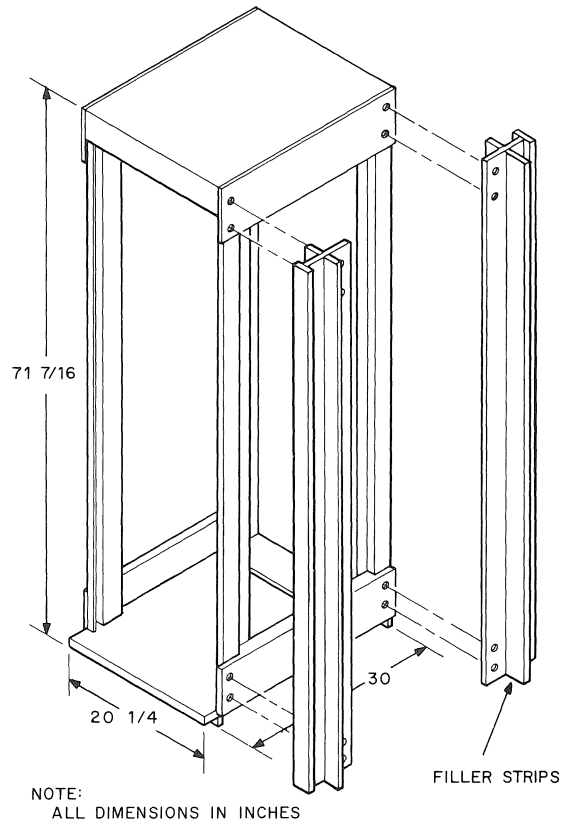
Figure 2-2   Installation of Filler Strips

5.   Remove the plastic shipping pin from the top of the cabinet rear access door.

6.   Ensure that the TU10W cabinet and the cabinet that contains the TMB11 are tied to the same ground or install a ground strap between the cabinets.

7.   After the TU10W has been positioned per the site plan, open the TU10W front door and unscrew the two service locks located in the upper left and lower right corners of the transport front panel (Figure 1-4a).

8.   Loosen the two shipping brackets that secure the transport to the rear of the cabinet frame. Slide the brackets toward the center of the cruciform as shown in Figure 2-3, and tighten.

NOTE
**Do not remove the shipping brackets. If the TU10W
is to be reshipped or installed in a new location, the
shipping brackets must be repositioned over the verti-
cal members and tightened.**

9.   If necessary, clean all outer surfaces.

TRANSPORT
CRUCIFORM

H950 CABINET
VERTICAL MOUNTING
MEMBER

DANGER
HIGH
VOLTAGE

SHIPPING BRACKETS (2)
(IN STORED POSITION)

CABLE STRAIN
RELIEF
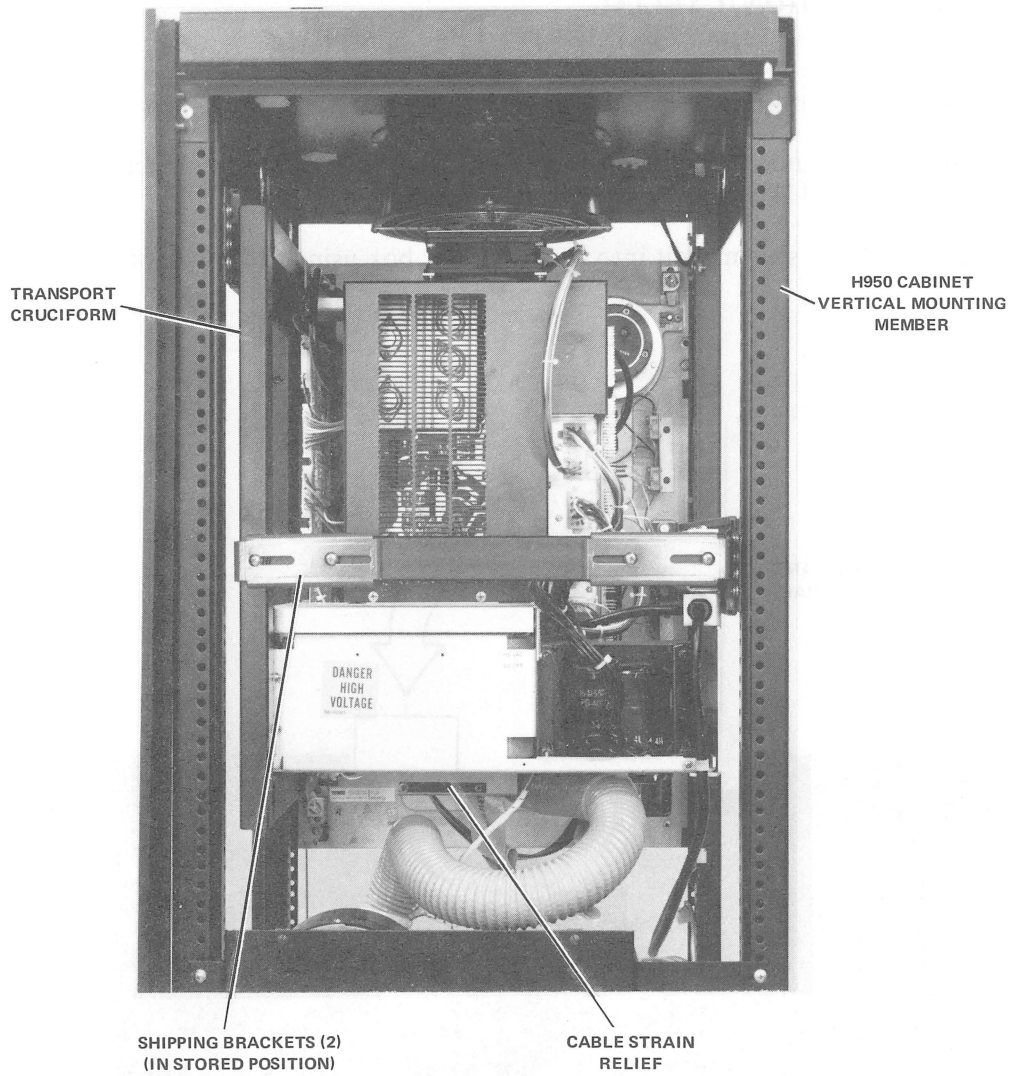
8209-9A

Figure 2-3   Transport Hold-Down Shipping Brackets

2.5 TMB11 INSTALLATION/CABLING
Ensure that power is removed from the PDP-11.

2.5.1 System Unit Installation

1. Extend the expander box on its slides and remove the module access cover. (Extended BA11K and BA11F boxes are shown in Figure 1-2.)

2. Install a TMB11 system unit into the expander box using the two captive screws (Figure 2-4).
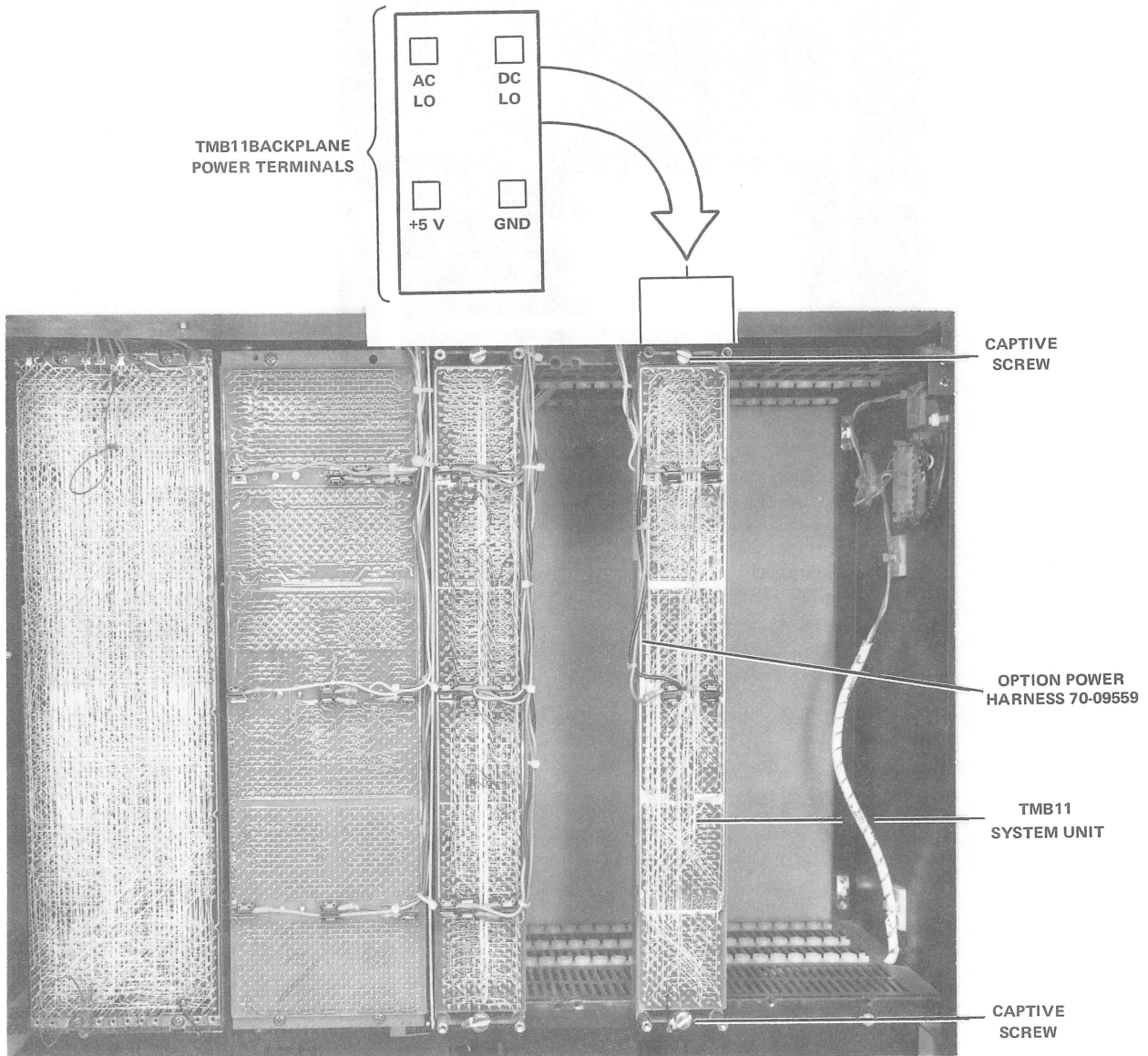
Figure 2-4   Expander Box Backplane (BA11F box shown)

3. Install the option power harness by connecting the Faston connectors to the system unit backplane and the harness plug(s) to the expander box (Figure 2-5).

4. Dress the option power harness along the top of the BA11F expander box as shown in Figure 2-5. If a BA11K box is used, dress the harness under the expander box.
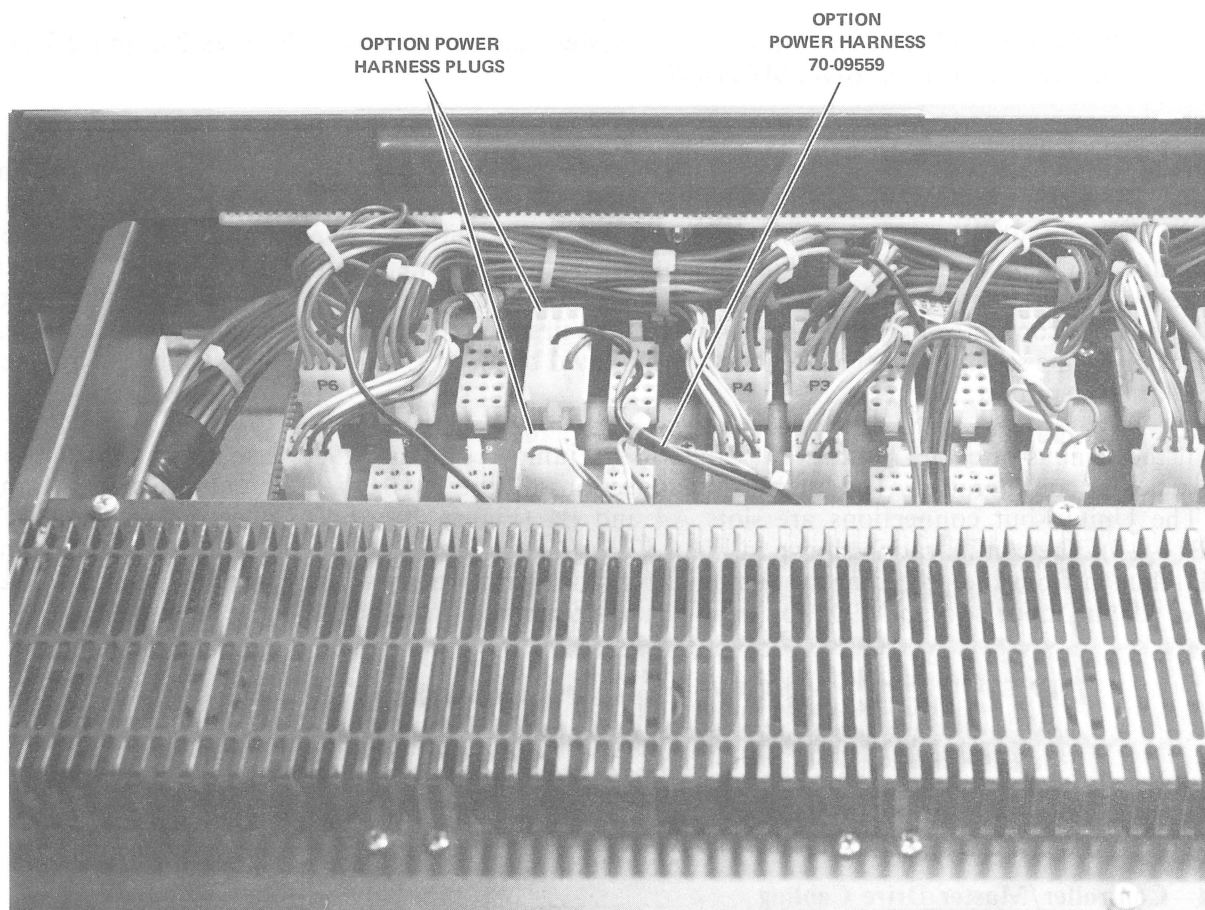
Figure 2-5   Power Cabling of TMB11 System Unit in BA11F Box

2.5.2 Module Installation

1. Check the jumpers on the M7821 module for a bus interrupt address of 224.

2. Check the priority jumper on the M7912 module for the correct interrupt priority level (usually BR5).

3. Check the jumpers on the M105 module for the correct address range for the TMB11 registers (772520 to 772536).

4. Plug the six TMB11 modules into the system unit according to Figures 2-6 and 2-7 and engineering drawing BD-TMB11-0-7.

2.5.3 Unibus Cabling

System units are connected to the Unibus in daisy-chain fashion as shown in Figure 2-8. Each unit has a Unibus-in and a Unibus-out jack. A BC11A cable connects the Unibus into the first system unit. M920 jumper modules connect the Unibus to the other system units in a given configuration. An M930 terminator module is installed in the Unibus-out jack of the last system unit in the chain. If the Unibus is to be carried onto another expander box, a BC11A Unibus cable is used to connect the Unibus from the Unibus-out connector of the last system unit in the first box to the Unibus-in connector of the first system unit in the second box. The Unibus is terminated by an M930 module installed in the out jack of the last system unit.

Install the Unibus-in cable, Unibus-out cable, M920 jumper, and/or M930 terminator according to the particular configuration. The Unibus-in connections on the TMB11 system unit are slots A1 and B1. The Unibus-out connections are slots A4 and B4 (Figure 2-9 and engineering drawing BD-TMB11-0-7). The configuration shown in Figure 2-6 utilizes a Unibus-out cable and an M920 to bring the Unibus in from the preceding system unit. The configuration shown in Figure 2-7 uses an M920 jumper for the input and an M930 for the output to terminate the Unibus.

NOTE
BC11A cable connectors will plug into the system units either way but will not fully seat if incorrectly installed. Make sure the connectors are fully seated and that the notches on the connector edges are up against the system unit slots.

2.5.4 Controller/Master Drive Cabling

Connect the BC11A master bus cable to slots E4 and F4 on the system unit (Figure 2-9). Install an M930 terminator module into slots E3 and F3 to terminate the master bus cable (Figures 2-6 and 2-7 and engineering drawing BD-TMB11-0-7).

CABLE STRAIN RELIEF

BC11A UNIBUS OUT CABLE

M7821

M920

M796

M105

M795

BC11A MASTER BUS CABLE TO TAPE TRANSPORT

M930 MASTER BUS TERMINATOR

M7912

M7911
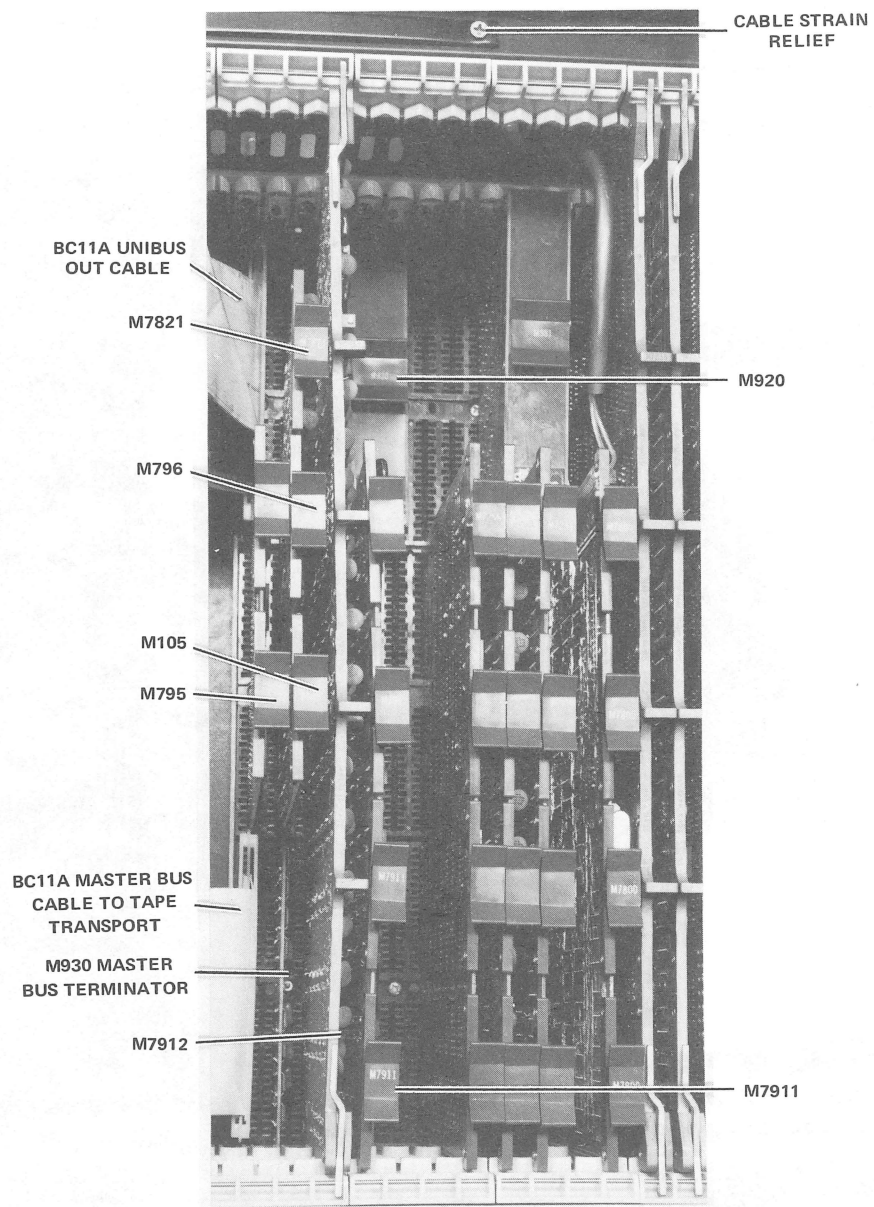
7941-5

Figure 2-6   TMB11 Module Location and Cabling in BA11K Box

M7821

M930 (UNIBUS TERMINATOR)

M7912

M920

M795

M796

M7911

M105

BC11A (MASTER BUS TO TAPE TRANSPORT)

M930 (MASTER BUS TERMINATOR)
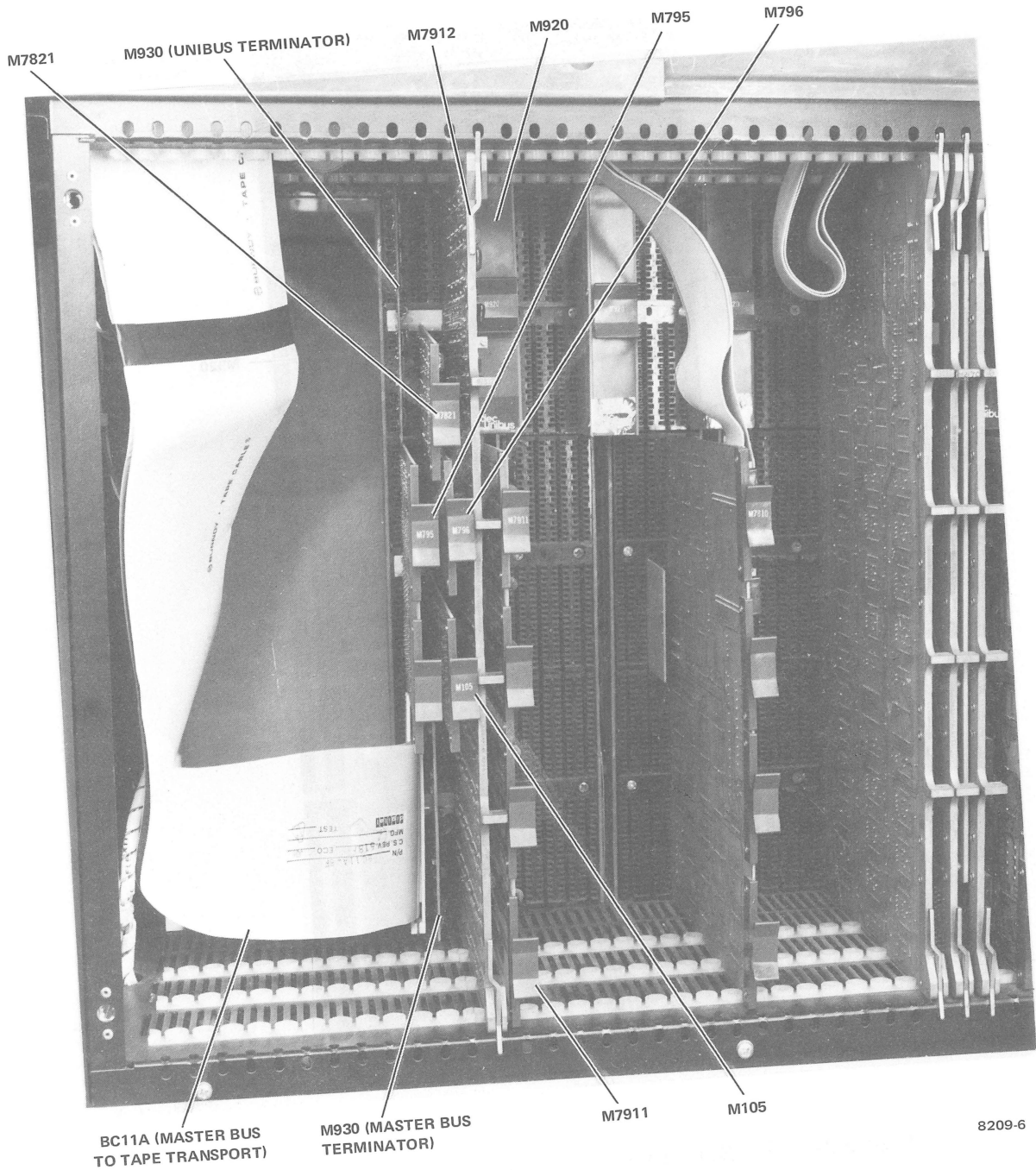
8209-6

Figure 2-7   TMB11 Module Location and Cabling in BA11F Box

BC11A
UNIBUS
CABLE

M930
UNIBUS
TERMINATOR
MODULE

TO NEXT
EXPANDER
BOX
(IF USED)

M920
UNIBUS JUMPER
MODULES

BC11A
UNIBUS
CABLE

OUT

IN

OUT

IN

OUT

IN
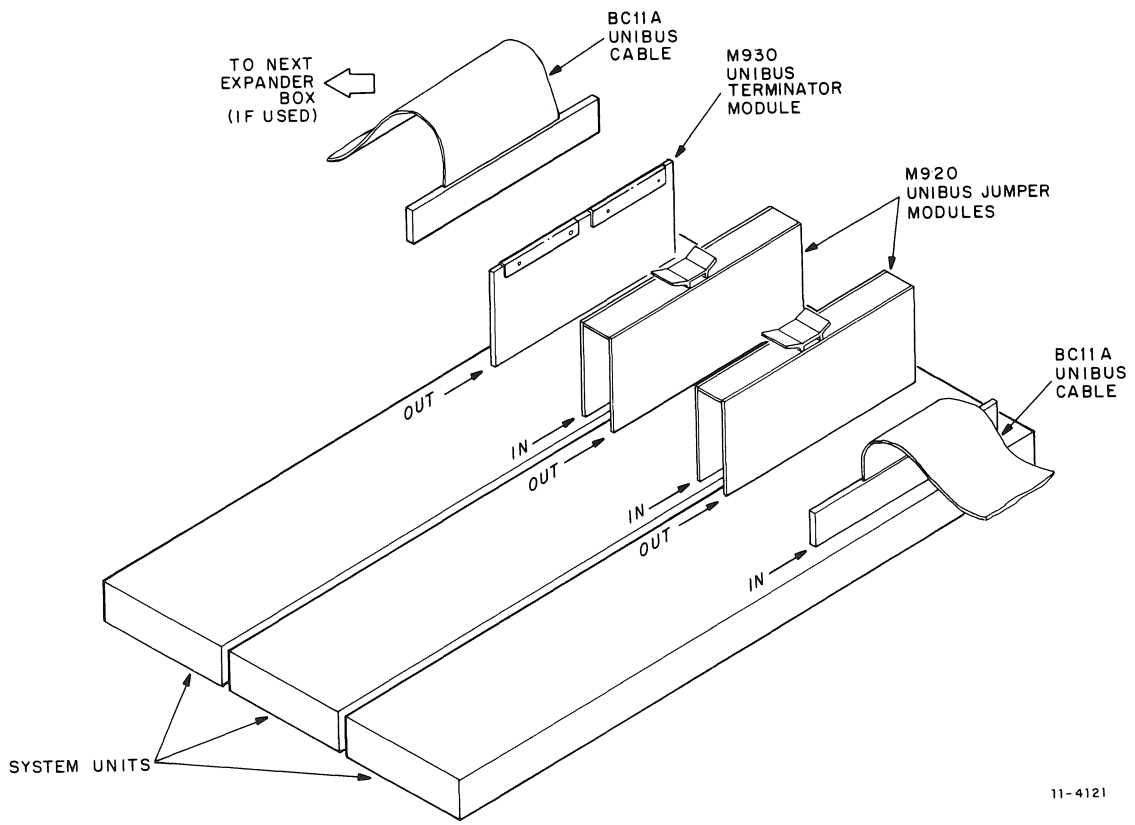
SYSTEM UNITS

11-4121

Figure 2-8   Unibus Cabling
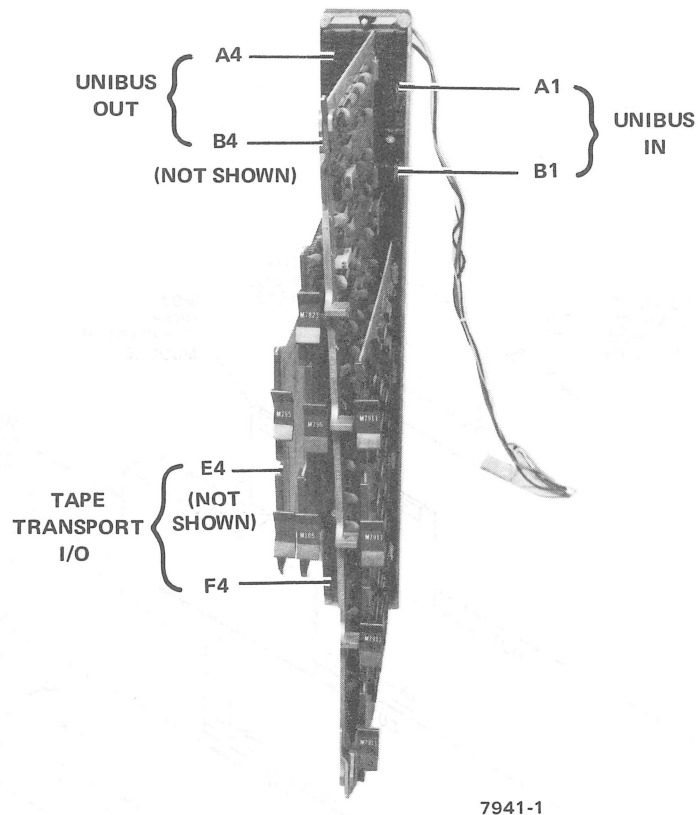
Figure 2-9   TMB11 Mounted in System Unit

2.5.5   Securing Cables

If the installation is performed in a BA11F expander box, lift the cable trough cover and feed the BC11A cable(s) through the trough and the cable holding bracket.

If the installation is performed in a BA11K expander box, perform the following:

1. Remove one screw from the center strain relief and loosen the other (Figure 2-6).

2. Swing the strain relief out and place the BC11A cable(s) up against the edge of the chassis.

3. Swing the strain relief back into place.

4. Insert the removed screw and tighten both screws.

2.6   TU10W CABLING FOR A ONE-DRIVE SYSTEM

1. Slide the TU10W Master Transport out of the cabinet.

2. Remove the M8926 Interface board from the transport system unit assembly.

3. Install H851 edge connectors on the J and K jacks of the M8926 board (Figure 2-10).
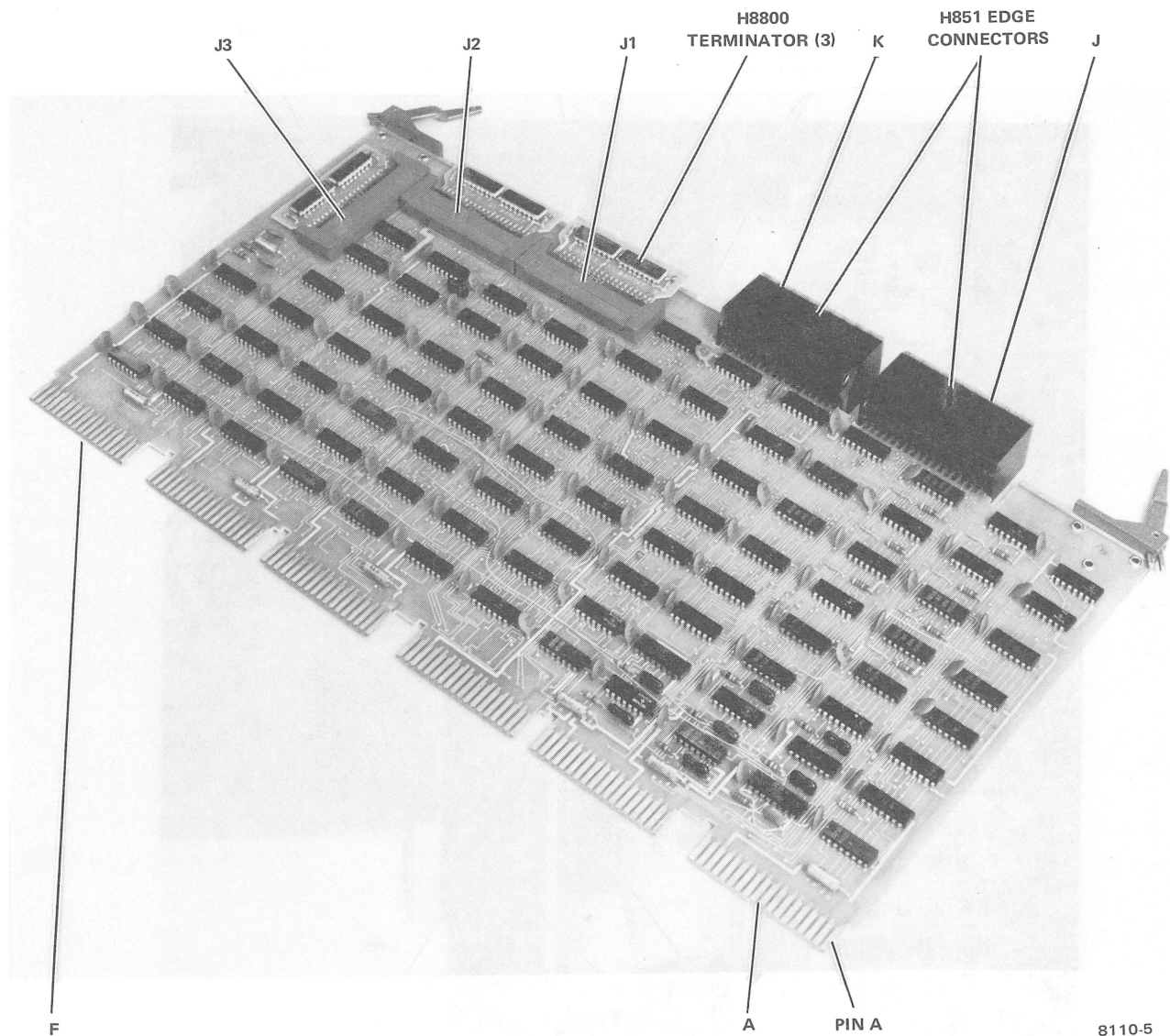
Figure 2-10   M8926 with H851 Edge Connectors and H8800 Terminators

4. Install three H8800 terminators into jacks J1, J2, and J3 as shown in Figure 2-10.

5. Feed the BC11A master bus cable from the TMB11 through the slot between the logic system unit and the sheet metal chassis (Figure 2-11).

6. Position the M8926 board in its approximate location as shown in Figure 2-11, and connect the BC11A master bus cable to the H851 edge connectors on the M8926.

7. Insert the M8926 board into the system unit.

8. Plug the 861 power cord into a power receptacle.

H851 EDGE
CONNECTORS

M8926 (PARTIALLY REMOVED)

BC11A MASTER BUS
CABLE FROM
FORMATTER

COLORED
STRIPE

COLORED STRIPE

BC06R
SLAVE BUS
CABLES TO
TAPE TRANSPORT

8209-10
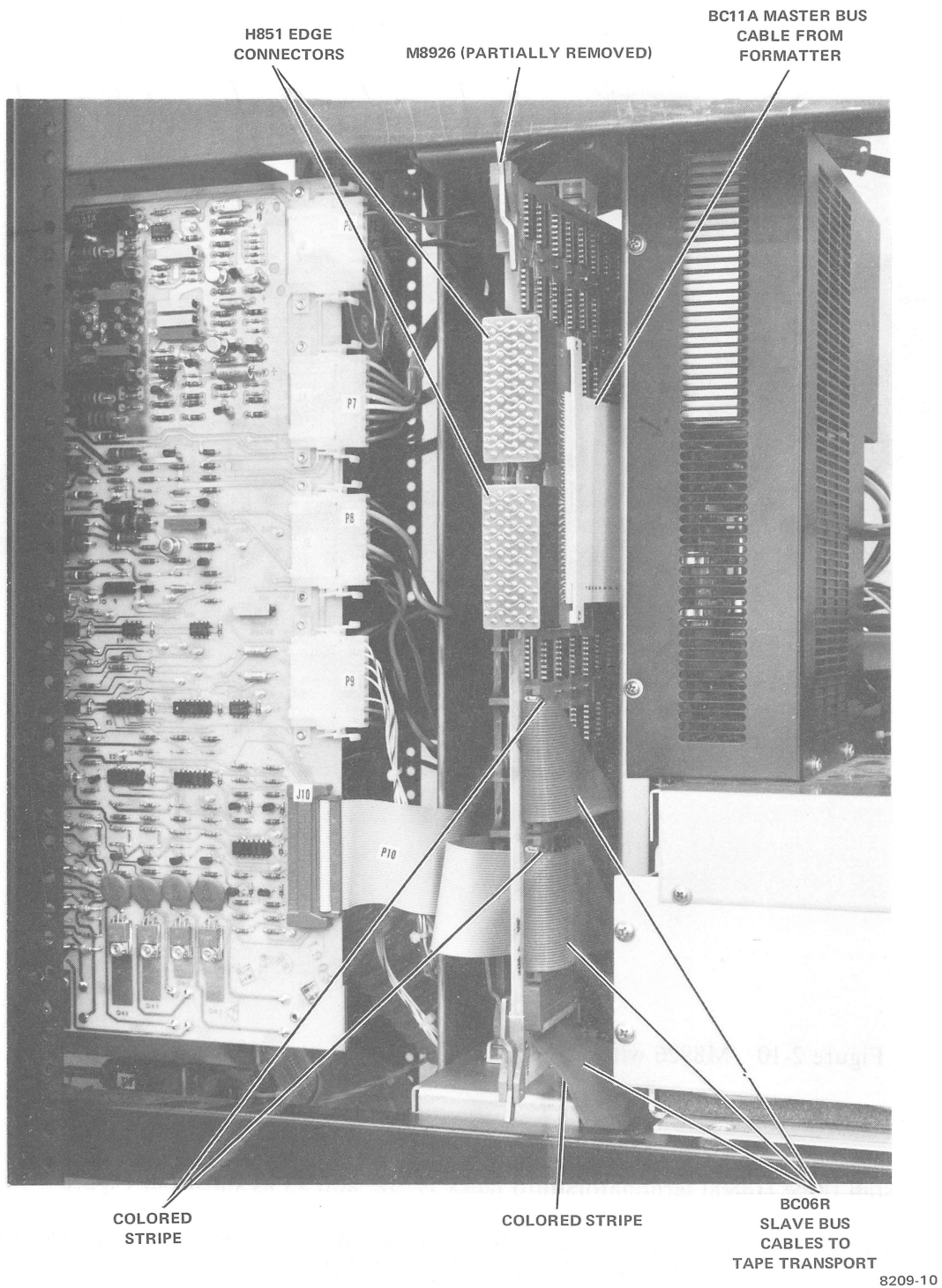
Figure 2-11   M8926 Cabling

9. Set the 861 circuit breaker to the ON position.

10. Slide the TU10W Transport back into the cabinet.

2.7 TU10W CABLING FOR A MULTIDRIVE SYSTEM

1. Slide the TU10W Master Transport out of the cabinet.

2. Remove the M8926 Interface board from the transport system unit assembly.

3. Install H851 edge connectors on the J and K jacks of the M8926 board (Figure 2-10).

4. Feed the BC11A master bus cable from the TMB11 through the slot between the logic system unit and the sheet metal chassis (Figure 2-11).

5. Route three BC06R slave bus cables through the same slot used in step 5 but from underneath.

6. Position the M8926 board in its approximate location as shown in Figure 2-11, and connect the BC11A master bus cable to the H851 edge connectors on the M8926.

7. Connect the three BC06R slave cables to J1, J2, and J3 on the M8926 board. Connect the J1 and J2 cables so that the rough side is down against the board and the colored stripe is up. Connect the J3 cable so that the rough side is down against the board and the colored stripe is out. Because the J1 and J2 cables are folded back, the rough sides are visible in Figure 2-11. The J3 cable is not folded back, and hence the smooth side is visible.

NOTE
It is important to observe the rough side/smooth side and colored stripe orientation in step 7. The plugs on the BC06R slave cables are not keyed and can be incorrectly inserted.

8. Mark the BC06R slave cables.

9. Insert the M8926 board into the system unit.

10. Secure the slave cables with the cable strain relief located below the transformer/capacitor assembly (Figure 2-3).

11. Slide the TU10W slave transport out of the cabinet.

12. Remove M9001, M8913, and M9001-YA from the slave transport system unit (Figure 2-12).

13. Route the three BC06R slave bus cables up through the slot between the logic system unit and the sheet metal chassis.

A. MASTER DRIVE

	1	2	3	4
A	M8926	M8910		G056
B				
C			M8911 (M8911-YA NOTE 1)	
D				
E			M8912 (NOTE 2)	
F				

B. SLAVE DRIVE

	1	2	3	4
A	M9001	M8910		G056
B				
C	M8913		M8911 (M8911-YA NOTE 1)	
D				
E	M9001-YA		M8912 (NOTE 2)	
F				
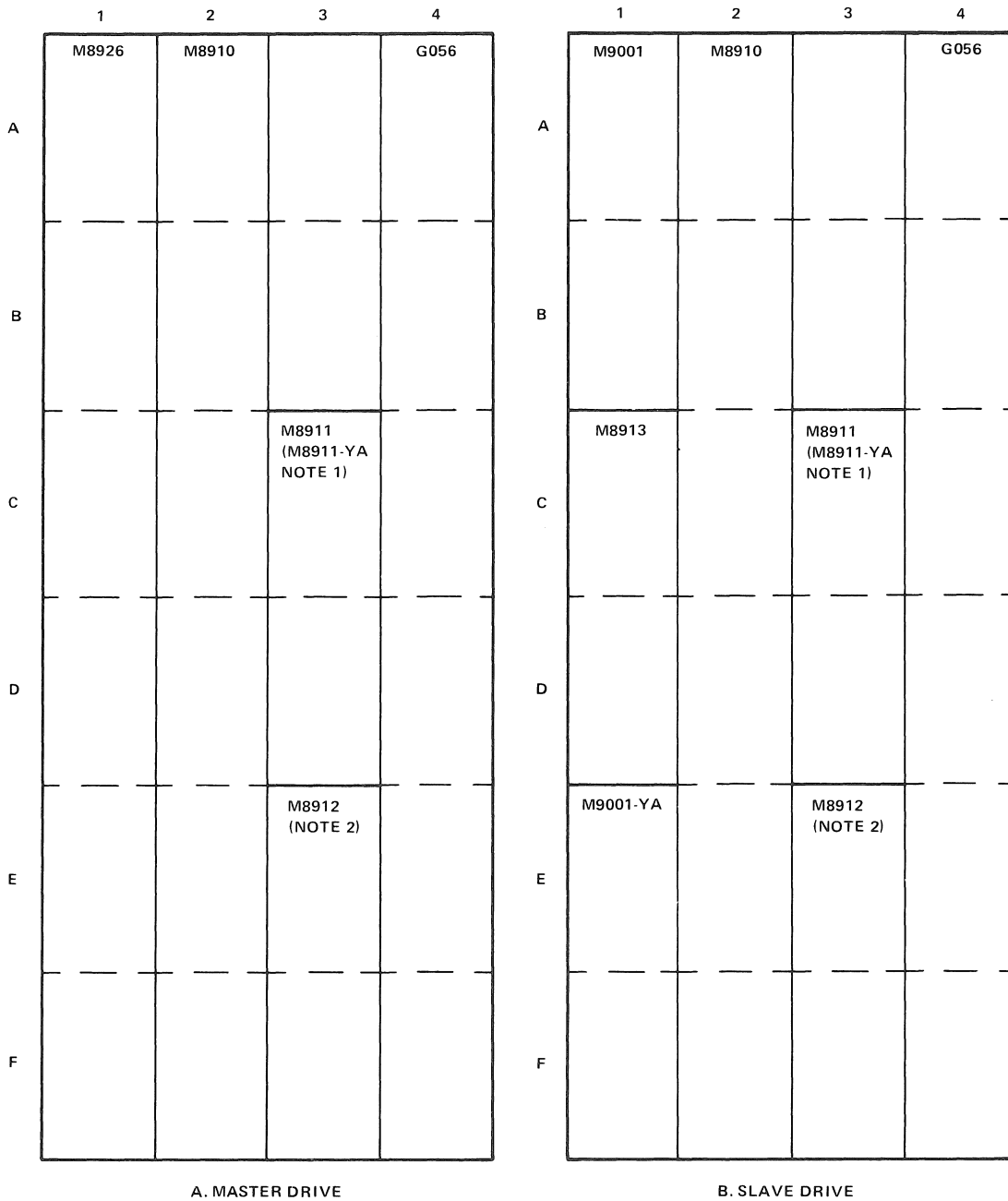
NOTES:

1. M8911 = 9 track drives; M8911-YA = 7 track drive
2. M8912 must be in the E/F position for on-line operation. In the off-line mode it can be used in position A/B as an off-line exerciser.

11-4784

Figure 2-12   TU10W System Unit Module Location,
Viewed from Backplane

14. Position the M9001-YA module in its approximate location and connect the BC06R cable from M8926-J3 to input jack J2 on M9001-YA. Follow the rough side/smooth side and colored stripe orientation of Figure 2-13.

15. If this is a 2-drive system, install an H8800 terminator in the M9001-YA output jack (J1). If another drive is to be cabled up, connect a BC06R slave bus cable to output jack J1 in accordance with Figure 2-13 and mark the cable.

16. Insert M9001-YA into the system unit.

17. Repeat steps 14, 15, and 16 to connect M8926-J2 to card M8913, and M8926-J1 to card M9001.

18. If the system contains more than two drives, install BC06R cables in daisy-chain fashion from one drive to the other, observing the colored stripe and smooth side/rough side orientation shown in Figure 2-13. The smooth side/rough side orientation for the slave drive cable cards is: smooth side against the board for input cable to J2 and rough side against the board for output cable from J1. Install H8800 terminators in the M9001, M8913, and M9001-YA output jacks of the last drive in the chain.

19. Plug the 861 power cords into a power receptacle.

20. Set the 861 circuit breakers to the ON position.

21. Slide the TU10W Transports back into the cabinet.

2.8 ACCEPTANCE TESTING
Refer to Acceptance Procedure, Engineering Drawing No. A-SP-TU10W-0-3, for the acceptance test procedures for the TMB11/TU10W Tape Drive System.
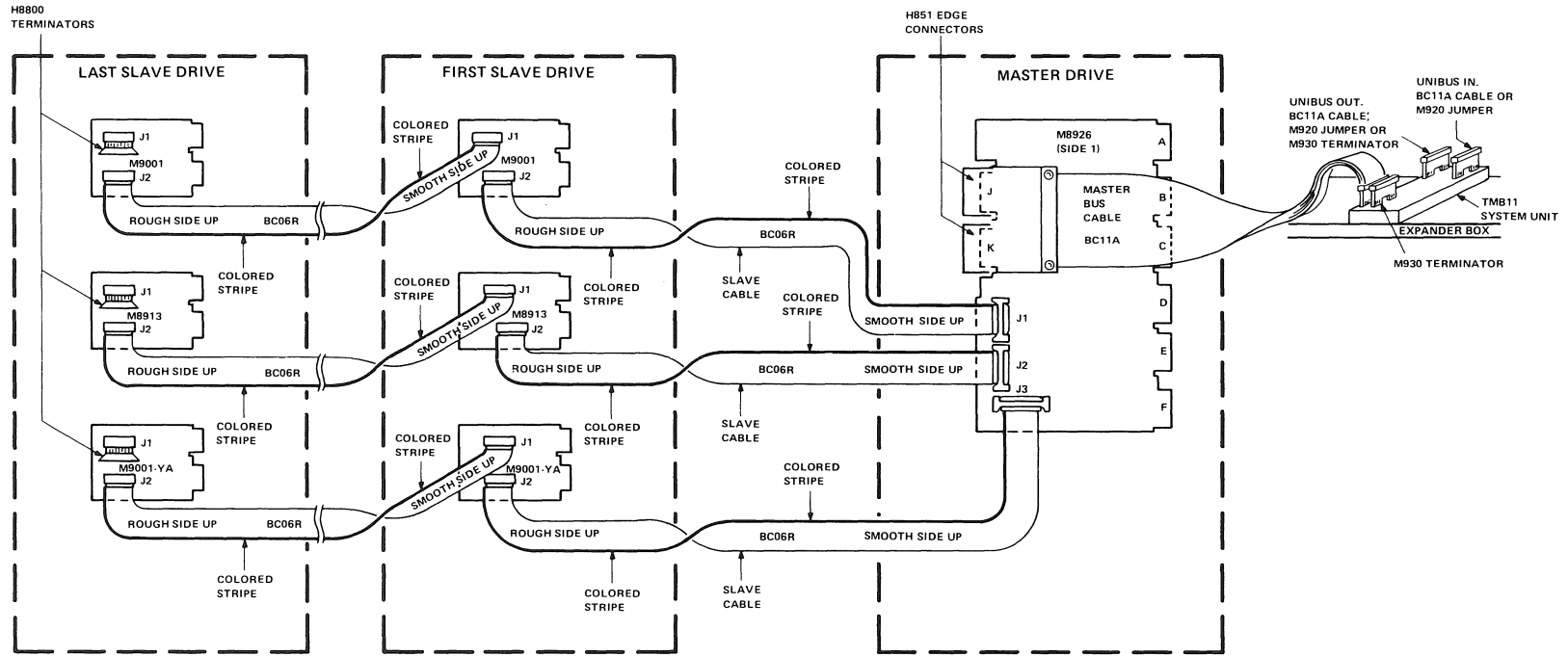
Figure 2-13   TMB11/TU10W Master/TU10W Slave Cabling Diagram

CHAPTER 3
SYSTEM OPERATING INSTRUCTIONS

3.1 CONTROLS AND INDICATORS

The operator control box (Figure 3-1) is located at the left of the file reel. The functions of the control box switches and indicators are listed in Tables 3-1 and 3-2.
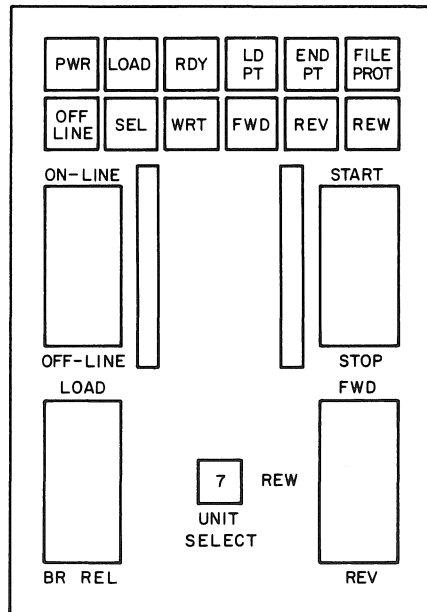
Figure 3-1   Operator Control Box

3.2 OPERATING PROCEDURES

3.2.1 Application of Power

If the 861 Power Controller REMOTE ON/OFF/LOCAL ON switch is in the REMOTE ON position, TU10W power is controlled by the processor POWER key switch. This method is used in normal operation.

Table 3-1 TU10W Control Box Switches

Switch	Function
LOAD/BR REL	
LOAD position	Enables vacuum motor and pulses reel motors which draw tape into the buffer columns.
Center position	Disables vacuum motor; brakes are full on.
BR REL position	Releases brakes.
ON-LINE/OFF-LINE	
ON-LINE position	Selects remote operation
OFF-LINE position	Selects local operation.
FWD/REW/REV	
FWD position	Selects, but does not initiate, forward tape motion when transport is off-line.
REW position	Selects, but does not initiate, tape rewind when transport is off-line.
REV position	Selects, but does not initiate, reverse tape motion when transport is off-line.
START/STOP	
START position	Initiates tape motion selected by FWD/REW/REV switch when transport is off-line.
STOP position	Clears any motion commands when transport is off-line.
UNIT SELECT (plug activated)	Selects the tape transport unit by number (0–7); this number is used in the program to address the tape transport (slave address).

Table 3-2 Status Indicators

Indicator	Function
PWR	Indicates power has been applied to the transport.
LOAD	Indicates the vacuum is on and the tape is loaded into the buffer columns.
RDY	Indicates that the tape transport is ready and on-line (vacuum on and settle-down delay complete); no tape motion.
LD PT	Indicates that the tape is at load point (beginning-of-tape, BOT).
END PT	Indicates that the tape is at end point (end-of-tape, EOT).
FILE PROT	Indicates that write operations are inhibited because the write enable ring is not mounted on the file reel.
OFF-LINE	Indicates local operation by the control box.
SEL	Indicates the tape transport is selected by the controller (program).
WRT	Indicates that a write operation is in progress.
FWD	Indicates that a forward command is in progress.
REV	Indicates that a reverse command is in progress.
REW	Indicates that a rewind command is in progress.

If the processor POWER key switch is not activated, TU10W power may be turned on locally by setting the 861 Power Controller REMOTE ON/OFF/LOCAL ON switch to LOCAL ON. This method may be used during maintenance.

3.2.2 Loading and Threading Tape
Use the following procedure to mount and thread magnetic tape.

1. Place the ON-LINE/OFF-LINE switch in OFF-LINE position. Apply power to the transport. Place the LOAD/BR REL switch to the center position.

2. Place a write enable ring in the tape reel groove if data is to be written on the tape. Ensure that there is no ring in the groove if data on the tape is *not* to be erased or written over.

3. Mount the file reel onto the lower hub, with the groove facing the back (away from the operator). Ensure that the reel is firmly seated against the flange of the hub and that the reel hub is securely tightened by hand. To tighten the reel hub, turn it clockwise. Do not grip the reel by the outer flanges. Ensure that brakes are on while tightening the hub.

3-3

4. Install the take-up reel (at the top) using the same procedure used in step 3.

5. Place the LOAD/BR REL switch in the BR REL position.

6. Manually unwind tape from the file reel and thread the tape by the tape guides and head assembly as shown in Figure 3-2.

TAPE GUIDES (2)

TAKE-UP REEL
(UPPER MOTOR)

CAPSTAN

HEAD TAPE GUIDES (2)

R/W ERASE
HEAD ASSEMBLY

TAPE MOVES INTO BOTH
VACUUM COLUMNS
WHEN "LOAD" SWITCH
IS PRESSED

TAPE PATH
WHEN LOADING

FILE REEL
(LOWER MOTOR)

10-1308
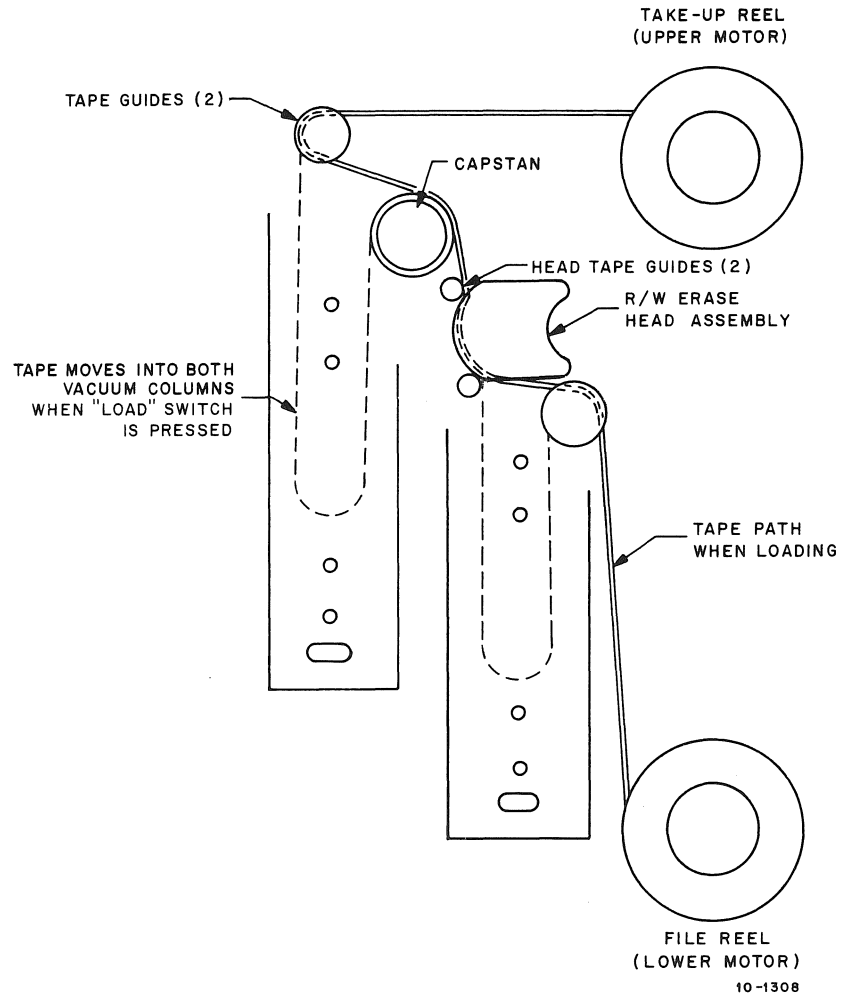
Figure 3-2   Tape Loading Path

7. Wind about four turns of tape onto the take-up reel. Ensure that the tape is in the guides.

CAUTION
**Wind tape flat onto the take-up reel. Do not bend
tape back or place tape end outside of reel (out the
window). While winding tape on the take-up reel,
simultaneously unwind the file reel to relieve tension
on the tape. Rotate the reels gently. Do not jerk the
tape as this could cause the tape to stretch.**

8. Place the LOAD/BR REL switch in the LOAD position to draw tape into the vacuum columns.

9. Select FWD and press START to advance the tape to the load point. When the BOT marker is sensed, tape motion stops, the FWD indicator goes out, and the LD PT indicator comes on.

NOTE
**If tape motion continues for more than 10 seconds, it
is possible that originally too much tape was wound
by hand onto the take-up reel, passing the BOT
marker. If this happens, press STOP, select REV
(reverse), and press START. The tape should move
to the BOT marker (load point) and stop.**

3.2.3 Unloading Tape
Different procedures are used to unload tapes, depending on whether or not the tape is at BOT.

Unloading Tape at BOT – To unload a tape which is at the BOT marker, perform the following procedure:

1. Place the LOAD/BR REL switch in the BR REL position to release the brakes.

2. Gently hand wind the file reel (lower) in a counterclockwise direction until all of the tape is wound onto the reel.

CAUTION
**While winding tape on the file reel, simultaneously
unwind the take-up reel to relieve tension on the tape.
Rotate the reels gently. Do not jerk the tape as this
could cause the tape to stretch.**

3. Remove the file reel from the hub assembly. Turn the hub counterclockwise to loosen it.

Unloading Tape Not at BOT – To unload a tape which is not at the BOT marker, perform the following procedure:

1. Place the ON-LINE/OFF-LINE switch in the OFF-LINE position.

2. Press STOP; select REW.

3. Press START. The tape should rewind until the BOT marker is reached.

4. Place the LOAD/BR REL switch in the BR REL position to release the brakes.

5. Gently hand wind the file (lower) reel in a counterclockwise direction until all of the tape is wound onto the reel.

<div align="center">

CAUTION
While winding tape on the file reel, simultaneously
unwind the take-up reel to relieve tension on the tape.
Rotate the reels gently. Do not jerk the tape as this
could cause the tape to stretch.

</div>

6. Remove the file reel from the hub assembly. Turn the hub counterclockwise to loosen it.

3.2.4 Restart After Power Failure

In the event of a power failure, the TU10W automatically shuts down and tape motion stops without physical damage to the tape. However, if the TU10W was on-line and was either reading or writing at the time of the power failure, the last record was probably lost; refer to system recovery procedures documentation if this happens. To restart the transport, proceed as follows.

<div align="center">

NOTE
Return of power is indicated when the PWR
indicator lights.

</div>

1. Set the ON-LINE/OFF-LINE switch to OFF-LINE.

2. Place the LOAD/BR REL switch in the BR REL position to release the brakes.

3. Manually wind the reels to take up any slack in the tape.

4. Set the LOAD/BR REL switch to the LOAD position to draw tape back into vacuum columns.

5. Set the ON-LINE/OFF-LINE switch to the desired position.

3.2.5 Restart After Fail-Safe

If the tape loop in either buffer column exceeds the limit shown in Figure 3-3, the vacuum system automatically shuts down and tape motion stops without damage to the tape. When this fail-safe condition occurs, the TU10W does not respond to either on-line or off-line commands. To restart the transport, refer to Paragraph 3.2.4.

VACUUM
SWITCHES

SHORT LOOP
(TRANSPORT
WILL SHUTDOWN)

BUFFER
COLUMN

LONG LOOP
(TRANSPORT
WILL SHUTDOWN)
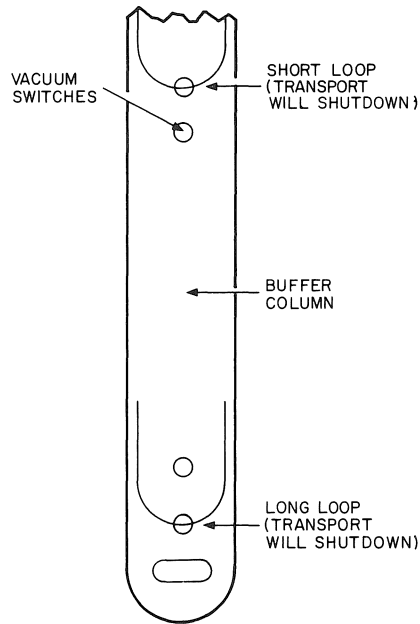
IO-I268

Figure 3-3   Fail-Safe Limits

3.3   OPERATOR TROUBLESHOOTING

Before calling maintenance personnel to correct a problem, the operator can make several checks with minimal effort. These steps may isolate an easily correctable error:

1.   Ensure that the vacuum door (Figure 1-4) is closed and sealed properly.

2.   If the tape does not stop at BOT, be certain the tape has a BOT marker.

3.   Ensure that the write enable ring is inserted in the tape reel if a write operation is to be performed.

4.   Clean the tape path according to the daily (8-hour) preventive maintenance procedures in Chapter 4.

CHAPTER 4
CUSTOMER CARE
AND PREVENTIVE MAINTENANCE

4.1 CUSTOMER RESPONSIBILITIES

The customer is directly responsible for:

1. Obtaining operating supplies, including disk cartriges, disk packs and filters, magnetic tape, DECtape, paper tape, cassettes, printer paper, printer ribbons, plotter paper, etc.

2. Supplying accessories, including disk storage racks, DECtape storage racks, carrying cases for disk cartridges and DECtape, cabinetry, tables, and chairs.

> **NOTE**
> Users of Digital Equipment Corporation equipment
> may obtain the proper operating supplies and acces-
> sories by contacting:
> Digital Equipment Corporation
> DEC Supplies Order Processing
> 146 Main Street
> Maynard, Massachusetts 01754
> Phone: (617) 897-5111, Ext. 5218, 5907
> Boston Area: (617) 890-0330
> TWX: 710-347-0212
> Cable: Digital Mayn
> Telex: 94-8457

3. Maintaining the required logs and report files consistently and accurately.

4. Making the necessary documentation available in a location convenient to the system.

5. Keeping the exterior of the system and the surrounding area clean.

6. Turning off the teletypewriter and/or line printer when these devices are not in use.

7. Ensuring that ac plugs are securely plugged in each time equipment is used.

8. Performing the specific equipment care operations described in Paragraphs 4.2 and 4.3 at the suggested frequencies or more often if usage and environment warrant.

4.2 CARE OF MAGNETIC TAPE

1. Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head; it is imperative that the tape be kept clean.

2. Always store tape reels inside containers when not in use; keep the empty containers tightly closed to keep out dust and dirt.

3. Never touch the portion of tape between the BOT and EOT markers; oil from fingers attracts dust and dirt.

4. Never use a contaminated reel of tape; this will spread dirt to clean tape reels and could have an adverse effect on tape transport reliability.

5. Always handle tape reels by the hub hole; squeezing the reel flanges could lead to tape edge damage in winding or unwinding tapes.

6. Do not smoke near the tape transport or storage area; tobacco smoke and ashes are especially damaging to tapes.

7. Do not place magnetic tape near any line printer or other device that produces paper dust.

8. Do not place magnetic tape on top of the tape transport, or in any other location where it might be affected by hot air.

9. Do not store magnetic tape in the vicinity of electric motors.

4.3 CUSTOMER PREVENTIVE MAINTENANCE OF TU10W TAPE TRANSPORT

4.3.1 General
Digital Equipment Corporation tape transports are highly reliable precision instruments that will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The following information will assist the customer in caring for his equipment and ensure the highest level of performance and reliability.

4.3.2 Preventive Maintenance
To ensure trouble-free operation, a preventive maintenance schedule should be kept. Preventive maintenance consists of cleaning only a few items, but the cleanliness of these items is very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport. Therefore, a rigid schedule applying to all machines is difficult to define. Daily cleaning is recommended for units in constant operation in ordinary environments. This schedule should be modified if experience shows other periods are more suitable. Paragraph 4.3.4 contains the cleaning instructions.

Before performing any cleaning operation, remove the file reel and store it properly. All items in the tape path should be cleaned on a daily basis. In cleaning, it is important to be thorough yet gentle and to avoid certain dangerous practices. It should be remembered that some tape cleaners are strong cleaning agents and should not come in contact with painted surfaces or plastic.

CAUTION
Do not use acetone or lacquer thinner, rubbing alcohol, or excessive cleaner. Be extremely careful not to allow the cleaner to penetrate ball bearings and motors.

4.3.3 Magnetic Tape Drive Cleaning Kit

A magnetic tape drive cleaning kit has been carefully configured to provide cleaning materials that will not harm tape equipment and will not leave any residue behind to interfere with data reliability. The hints contained in the following few paragraphs will ensure that the very best results possible will be obtained from the kit.

The Freon® TF113 cleaning fluid in this kit is one of the safest and best degreasing agents available. It will not adversely affect any part of DIGITAL's tape equipment. To prepare the can of fluid for service, unscrew the top and punch a small hole in the metal seal covering the pour spout.

WARNING
TF113 is a non-restricted, non-hazardous substance. However, when using TF113, avoid excessive skin contact, do not allow TF113 to come in contact with the eyes, and do not swallow it. Use TF113 only in a well ventilated area.

When cleaning tape equipment, never dip a contaminated cleaning swab or wipe into the can. To transfer fluid onto the swab, pour a little out into the screw cap and dip the swab into the cap. Discard the remaining fluid in the cap when the cleaning operation is complete.

Always keep the can of fluid tightly closed when not in use, because Freon TF113 evaporates rapidly when exposed to air.

Use the cleaning materials contained in the kit to clean tape heads, tape guides, the tape cleaner, reel hubs and any part of the drive where a dirty residue could ultimately come in contact with tape. To clean other parts of the drive, such as the exterior surfaces of doors or the friction pads of brakes, use any reasonable clean, lint-free material with or without cleaning fluid.

NOTE
If you encounter an unusually stubborn dirt deposit that appears to resist TF113, try a mild soap and water solution to dislodge it. After using soap, be sure to wash down the affected area thoroughly with TF113 to remove soapy residues.

4.3.4 Cleaning the TU10W DECmagtape Drive

1. Dismount the tape from the unit.

2. Clean the following components of the drive using a foam-tipped swab soaked in cleaning fluid (Figure 4-1):

    a. Read/write head (Location A)
    b. Erase head (Location B)
    c. Tape cleaner (Location C)
    d. Upper roller guide (Location D)
    e. Lower roller guide (Location E)

NOTE
Be careful to keep cleaning fluid only on the tape-bearing surface of roller guides to prevent degreasing the roller guide bearings.

®Freon is a registered trademark of Dow Chemical Co.
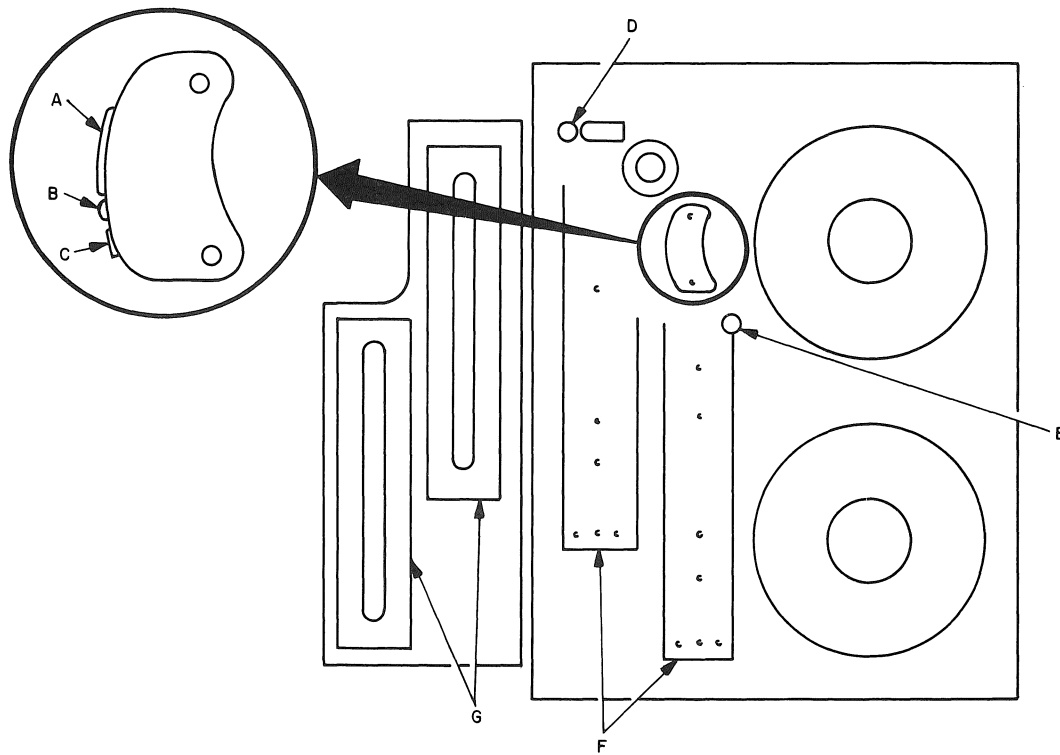
Figure 4-1   Location of Read/Write and Erase Heads and Tape Cleaner

3.   When cleaning the head area, avoid the spring-loaded ceramic washers on the tape drive assemblies. If it appears necessary to run the swab over the tape bearing surface of these guides to remove oxide deposits, do so; however, when cleaning is complete, be sure that the washer is pressed snugly up against the tape guide surface and not "hung up" on its shaft (Figure 4-2).

4.   Next, clean the vacuum pockets (F) and the inner surface of the vacuum door (G) using a lint-free wipe and cleaning fluid. Pass another lint-free wipe over the head using a polishing action to remove any remaining deposits.
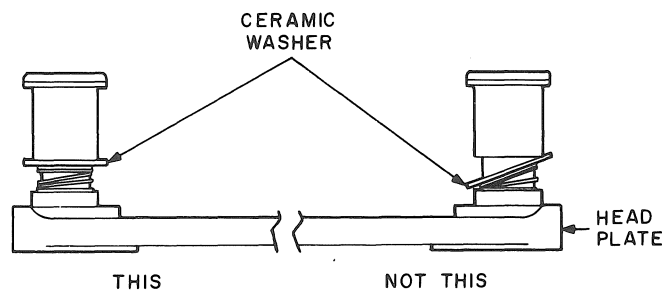
Figure 4-2   Proper Ceramic Washer Positioning

CHAPTER 5
SYSTEM MAINTENANCE

5.1 SCOPE

This chapter provides a complete description of TMB11/TU10W preventive and corrective mainte-
nance procedures. The major TU10W assemblies referenced throughout this chapter are shown in
Figure 5-1. Access to the interior components of the TU10W is gained by rotating the service locks on
the upper left and lower right sides of the TU10W to release the unit from the cabinet (Figure 5-2).

7660-22-A0580
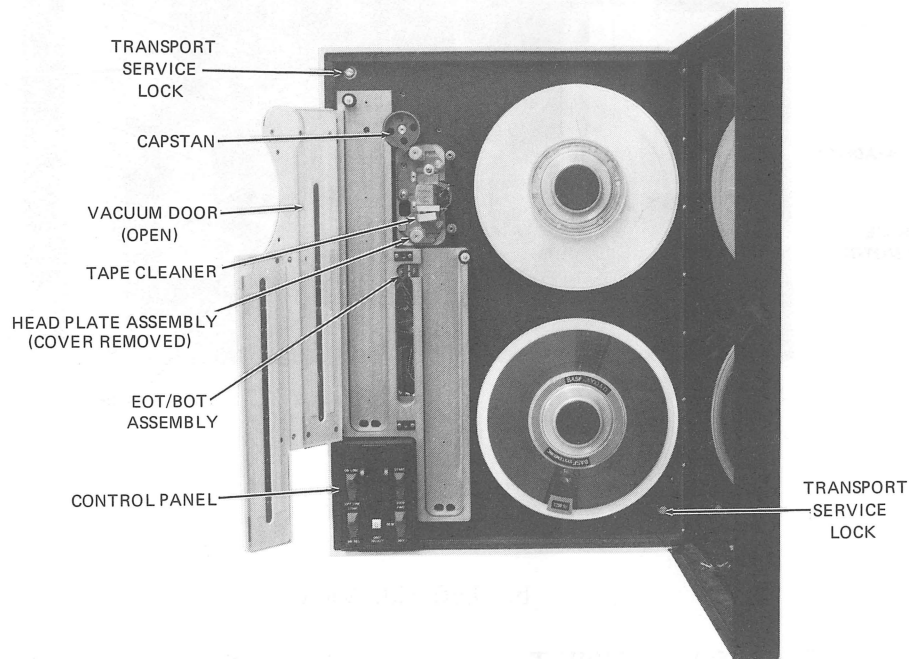
a. Front View

Figure 5-1   TU10W Tape Transport Assemblies (Sheet 1 of 2)

BRAKE ASSEMBLY   AIR FILTER   TACHOMETER

LOGIC FAN
ASSEMBLY

SERVICE LOCK

CAPSTAN MOTOR

H606 POWER BOARD

LOGIC BACKPLANE
ASSEMBLY

TAKE-UP REEL MOTOR

VACUUM SWITCHES

POWER SUPPLY
REGULATOR BOARD

FILE REEL MOTOR

VACUUM SWITCHES

TRANSFORMER-CAPACITOR
ASSEMBLY

VACUUM HOSE
(TO VACUUM MOTOR)

READ/WRITE
INTERLOCK

BRAKE ASSEMBLY   AIR FILTER
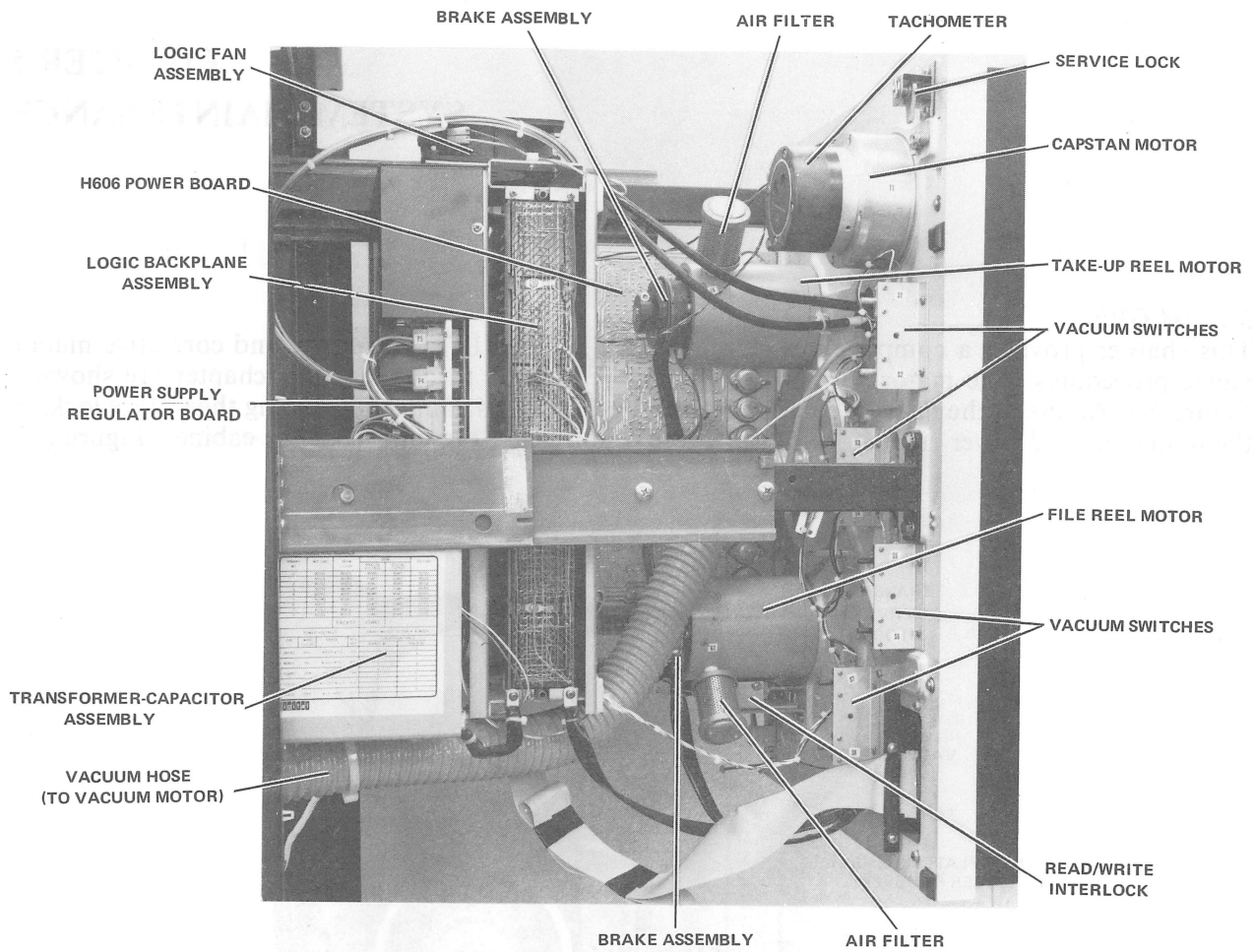
8209-5

b.   Left Side View

Figure 5-1   TU10W Tape Transport Assemblies (Sheet 2 of 2)
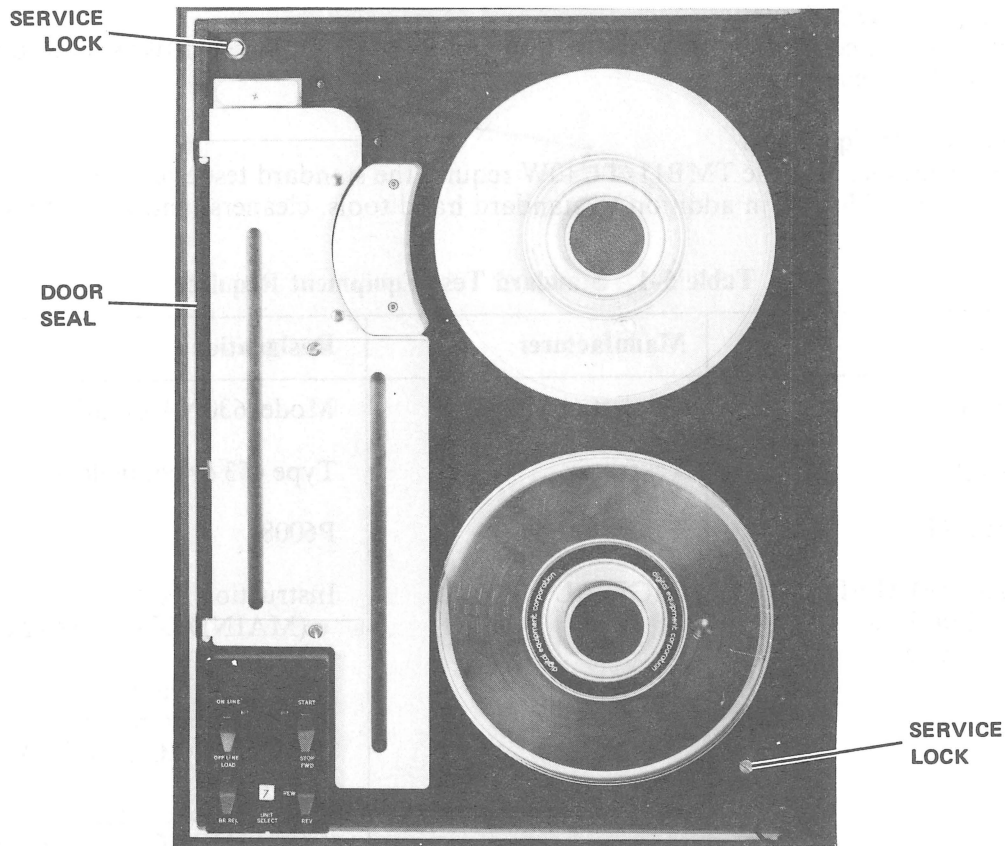
Figure 5-2   Transport Casting, Front View

5.2   TMB11/TU10W MAINTENANCE PHILOSOPHY

The TMB11/TU10W DECmagtape System is a highly reliable system that will provide years of trouble-free performance when it is properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability.

The preventive maintenance required on the TMB11 differs from that required on the TU10W Transport. The TMB11 Controller and the M8926 Interface module are total solid-state units with no moving parts; therefore, no preventive maintenance is required on these units. The TU10W Transport, however, requires daily customer care, consisting of head and tape path cleaning. (Refer to Paragraph 4.3.) Otherwise, the transport requires few adjustments, which should not be performed unless problems are encountered in transport operation. Refer to Paragraph 5.4 for the recommended preventive maintenance procedures.

Corrective maintenance consists of troubleshooting at the system level (using system diagnostics and visual methods) to localize the failure to a particular unit, whether it is the TMB11 Controller, M8926 Interface, or TU10W Transport. Once a faulty unit is identified, unit level troubleshooting can be performed using unit functional block diagrams, flow diagrams, timing diagrams, and engineering logic diagrams to localize the failure to an electrical area (module) or a mechanical part. Then, when the faulty module or mechanical part is located, it should be replaced.

5.3 TEST EQUIPMENT
Two categories of test equipment are required to maintain the TMB11/TU10W: standard test equipment and special test equipment.

5.3.1 Standard Test Equipment
Maintenance procedures for the TMB11/TU10W require the standard test equipment and diagnostic programs listed in Table 5-1, in addition to standard hand tools, cleaners, and test cables.

<p align="center">Table 5-1 Standard Test Equipment Required</p>

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630NA or 260
Oscilloscope	Tektronix	Type 453 or equivalent
X10 Probes (2)	Tektronix	P6008
Diagnostics (MAINDECS)** (Use revision listed, or a higher one.)	DIGITAL	Instruction Test (MAINDEC-11-DZTMA-*H) Multidrive Data Reliability Exerciser (MAINDEC-11-DZTMH-*E) Drive Function Timer (MAINDEC-11-DZTME-*C) Supplemental Instruction Test (MAINDEC-11-DZTMF-*D) Utility Drive (MAINDEC-11-DZTMG-*C)

*Revision level
**Refer to Table 5-6 for a description of diagnostics.

5.3.2 Special Test Equipment
The special test equipment and tools required are listed in Table 5-2. Usage of the special tools and equipment is also provided in the table.

5.4 PREVENTIVE MAINTENANCE
The TMB11 Controller and M8926 Interface module are all electronic assemblies that require no preventive maintenance. Care and preventive maintenance of the TU10W to be performed by the user are listed in Chapter 4. TU10W preventive maintenance to be performed by the service technician is provided in this section.

The recommended frequencies for performing the PM steps in this procedure are based on moderate usage of the equipment. In cases where usage is heavy, certain steps should be performed more frequently.

For example, in Paragraphs 5.4.2.1 and 5.4.2.7 through 5.4.2.13 of the quarterly procedure, assume that tape motion will not exceed 150 hours/quarter; if tape motion exceeds that figure, the steps should be performed more often. (Tape motion = time spent actually moving tape; this time must be decreased by 1/2 if the software is not double-buffered, or if two drives exist on the same controller.)

The semiannual procedure assumes that tape motion will not exceed 300 hours during a 6-month period; if tape motion exceeds that figure, these steps should be performed more frequently.

Table 5-2   Special Tools and Equipment and Their Use

Item		Part No.	Usage*				
			1	2	3	4	5
1.	Skew Tape (800 bits/inch)						
	365.8 m (1200 ft)	29-19224	X				X
	182.9 m (600 ft)	29-22020	X				X
2.	Reel Hub Tool	29-18611					X
3.	Roller Guide Tool	29-18607					X
4.	Microscope	29-20273				X	X
5.	Magna-See	29-16871				X	X
6.	Penlight†	29-10780	X	X	X	X	X
7.	Alignment Glass	74-13969					X
8.	Depth Micrometer	29-22039					X
9.	Shim Stock						
	0.001	48-50023-01					X
	0.002 (red)	48-50023-03					X
	0.003 (green)	48-50023-04					X
	0.004 (tan)	48-50023-05					X
	0.005 (blue)	48-50023-06					X
	0.0075 (transparent)	48-50023-07					X
	0.010 (brown)	48-50023-08					X
10.	TMB11/TU10W Module Swap Kit		X				
11.	Feeler Gauge Set†	29-13515	X		X	X	X
12.	Allen Wrench Set		X		X	X	X
13.	EOT/BOT Markers (Reflective Strips)	90-09177				X	X
14.	Deleted						
15.	Vacuum Belt Tension Gauge	29-22265	X				
16.	Capstan Alignment Tool	29-18609					X

*Usage Legend:
1. Routine Corrective Maintenance
2. Monthly PM
3. Quarterly PM
4. Semiannual PM
5. Major Tape Path Alignment
†Contained in standard tool kit.

5.4.1 Monthly PM Schedule

The items listed in this section are to be performed on a monthly basis:

5.4.1.1 Tape Path Cleaning and Inspection – Clean the tape path and inspect it for wear as follows:

1. Turn power off in the 861 power controller. Remove and clean the take-up reel, using a Kimwipe dampened with water; inspect the take-up reel for cracks or loose center ring (hub interface). Replace if defective.

2. Remove the supply reel (if installed). Using water-dampened Kimwipes, clean the deckplate surfaces and front door.

<div align="center">

CAUTION

Be careful not to saturate the fiberglass lining on the vacuum column walls with fluid; this could cause damage to the lining.

</div>

3. Remove the head cover and open the vacuum door.

4. Using a penlight, inspect the read/write head and erase head for oxide accumulation. A worn head will normally show oxide accumulation on the worn spot. If the read/write head is unevenly worn or if the erase head shows any wear, replace the head plate assembly. (Refer to Figure 5-3 shiny spots indicate uneven wear.)
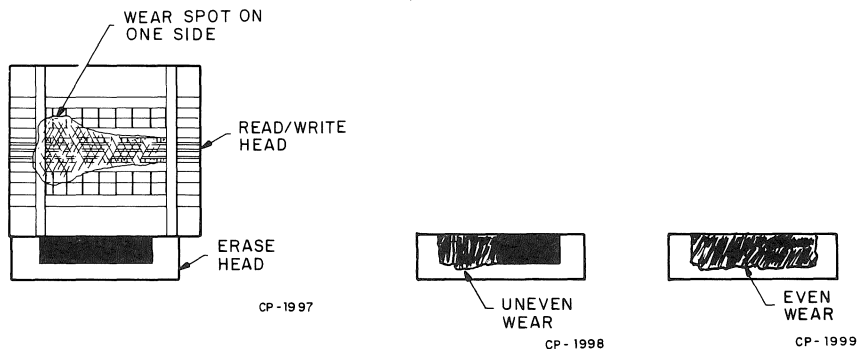
Figure 5-3   Examples of Unacceptable Head Assembly Wear

5. Using Freon TF113 and cotton-tipped wooden swabs, clean any accumulated oxide from the read/write head, erase head, tape cleaner, and fixed guides. (Pay particular attention to removing oxide buildup from ceramic surfaces of the fixed guides.)

NOTE
Ensure that the inner (spring-loaded) guides move freely after cleaning and that they are not jammed under the fixed guides.

6. Clean vacuum columns and vacuum column doors with Freon TF113 and Kimwipes. Clean roller guides with cotton swabs and Freon TF113.

NOTE
Wear spots of any kind on the erase head are unacceptable.

5.4.1.2 Reel Hub Inspection and Lubrication – Lubricate and inspect the reel hubs as follows (Figure 5-4).
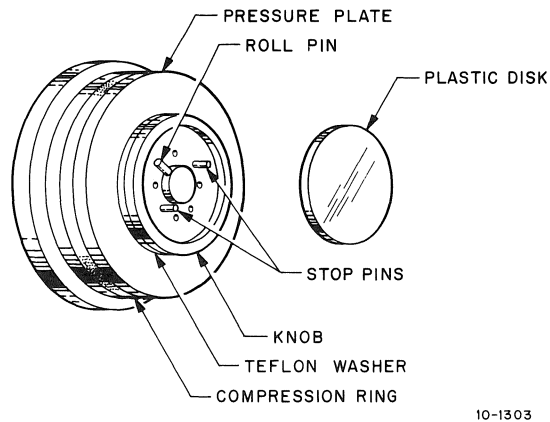
Figure 5-4 Hub Composition

5-7

1. Lubricate the upper and lower reel hub compression rings by applying silicon grease generously and rubbing it in. Wipe away excess with Kimwipe.

2. Place the take-up reel on the lower hub. Turn the hub lock until it hits the stop pin (PN 90-06527). Hold the hub with one hand and attempt to turn the reel counterclockwise with the other hand.

3. If the hub lock does not hit the stop when tightened, or if the reel turns while the hub is being held stationary, readjust the hub pin and replace the compression ring according to the following procedure.

    a. Remove power from the TU10W Tape Transport and remove the tape reel.

    b. Carefully snap out the plastic disk (PN 12-09212-00) from the reel hub.

    c. Mark the position of the center roll pin (PN 90-06526) in the hub guide.

    d. Using a pair of heavy duty diagonal pliers, carefully remove the center roll pin.

    e. Grasp the reel hub and unscrew the knob from the hub.

    f. Remove (in order) the Teflon washer, pressure plate, and rubber compression ring.

    g. Lightly lubricate the flat surfaces of a new compression ring with silicon grease. Wipe all excess grease from the ring with a lint-free cloth.

    h. Install (in order) the new compression ring, pressure plate, and Teflon washer.

    i. Lightly tighten the knob on the hub until the compression ring is compressed and fully seated.

    j. Loosen the knob until it is free of the Teflon washer. Then gently screw it in until it just touches the washer.

    k. Reinstall the roll pin in the same hole from which it was removed (Step d).

    l. Turn the knob counterclockwise until the roll pin makes contact with one of the two hub stop pins.

    m. Try to install a tape reel on the hub. If the tape reel does not easily slip on the hub, move the stop pin back one hole at a time until the knob can be released far enough to permit the tape reel to slip on the hub.

    n. With a tape reel installed, tighten the knob (clockwise) until the roll pin contacts the other hub stop pin. If the tape reel is not secure, move the stop pin ahead until the knob can be tightened correctly.

4. Place the take-up reel on the upper hub. Repeat the above procedure from Step 2 for the upper hub take-up.

5.4.1.3 Operator Panel Check – Check the operator panel switches and indicators as follows. (Replace switches and/or indicators as required.)

1. Apply power to the 861 power controller; ensure that the OFF-LINE and PWR indicators on the control panel are ON.

2. Place a scratch tape (with write ring) on the lower hub and secure the hub lock. Set the LOAD/BR REL switch to LOAD and then back to BR REL. Ensure that both reels turn freely and that the FILE PROT light does not light as the supply reel is rotated.

3. Thread the scratch tape through the tape path and make two wraps around the take-up reel. Set the LOAD/BR REL switch to LOAD; ensure that the LOAD indicator on the control panel comes on.

4. Place the FWD/REW/REV switch to FWD; place the START/STOP switch to STOP and then back to START. Ensure that the FWD indicator is lit while the drive is moving the tape toward BOT, and that the LD PT indicator lights when the drive stops at BOT.

5. Run the tape forward for approximately 30 seconds; set the START/STOP switch to STOP.

6. Set the FWD/REW/REV switch to REV; press START. Allow the tape to run in reverse for approximately 10 seconds and ensure that the REV indicator is on. Place the START/STOP switch in the STOP position.

7. Set the FWD/REW/REV switch to REW; press START. Ensure that the REW indicator is on.

8. Set the ON-LINE/OFF-LINE switch to ON-LINE. When the drive has completed the rewind operation in Step 7 check that the RDY indicator comes on. Check that the SEL indicator also comes on if the controller is currently selecting this TU10W.

9. Set the ON-LINE/OFF-LINE switch to OFF-LINE and the LOAD/BR REL switch to BR REL. Dismount the tape and remove the write enable ring. Mount the tape and ensure that the FILE PROT indicator is on. Rotate the reel; ensure that the FILE PROT indicator remains on.

NOTE
If a quarterly PM procedure is scheduled, proceed to Paragraph 5.4.2; if not, continue with Paragraph 5.4.1.4.

5.4.1.4 NRZ Diagnostic – Position tape at BOT; place the unit ON-LINE. Run the Multi-Drive Data Reliability Exerciser (DZTMH) for 10 minutes of NRZ (800 bits/inch). If any soft errors occur, run a complete pass again to determine whether the frequency of soft errors is within specifications; no hard read errors are allowed.

NOTE
The acceptable soft error rate for one 731.6 m (2400-foot) reel of tape is:

1. **Read: 2**
2. **Write: 5**

Retries on the same spot do not increase the soft error tally, i.e., a read error on block 1, record 1 that required three retries to recover is recorded as one soft read error.

5.4.2 Quarterly PM Schedule

The items listed in this section are to be performed on a quarterly basis.

5.4.2.1 Reel Motor Brakes/Vacuum System Belt

1. Disassemble, clean, and reassemble the reel motor brakes according to the following procedure:

   a. With power off, pull the transport out on its slides. (Access brakes from the left side of the transport; operation is identical for both reel motors.)

   b. Loosen the Allen screw located on the clamp (Figure 5-5).

   c. Remove the spring and brake assembly. Push a cotton swab through each of the inserts (locating holes) that hold the rotor disk and rotor to ensure that they are securely held in the rotor and that they do not protrude in such a way as to interfere with operation of the rotor disk. If inserts are loose, replace the brake assembly.

   d. Using a clean, dry, lint-free cloth or wipe, clean the following:

      (1) The brake surface of the stator. (Stator is still on motor.)

      (2) Both sides of the rotor disk, including location pins.

      (3) The face of the rotor next to the rotor disk.

NOTE
Avoid skin contact with brake surfaces; body oils are detrimental to brake function.

   e. Install the rotor disk into the rotor; select the mating combination that allows for smoothest insertion and retraction of rotor disk pins into the rotor locating holes. Try each of the 120-degree intervals for best fit.

.010" CLEARANCE

SPRING

REEL MOTOR

MOTOR SHAFT

CLAMP

$^3/_{16}$" SPACER

ROTOR

ROTOR DISC

STATOR SLOT
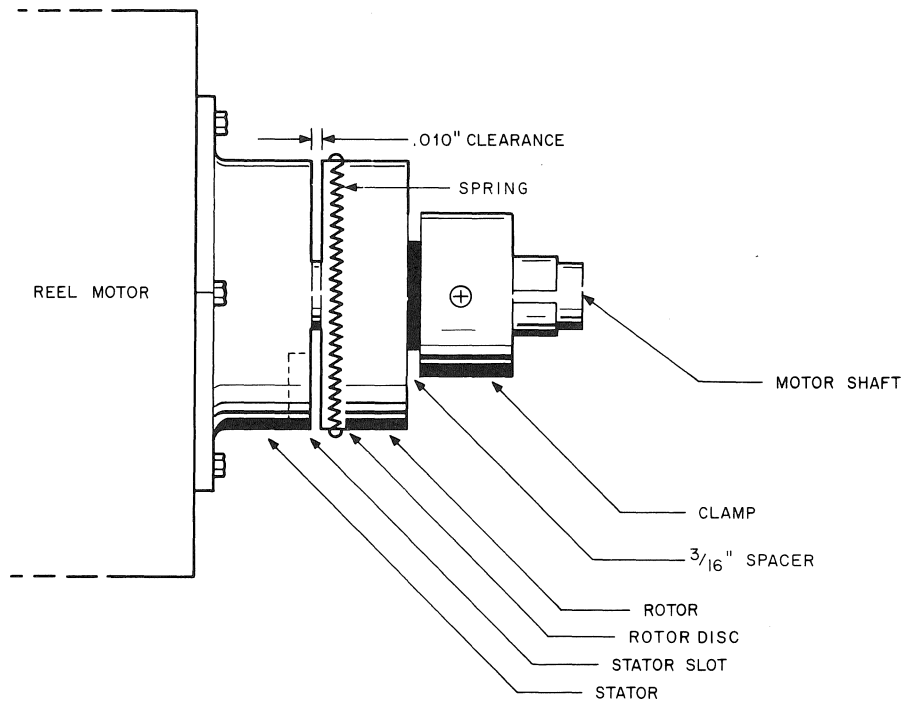
STATOR

11-4672

Figure 5-5 Reel Motor Brake Assembly

f.   Replace the brake, leaving a clearance of 0.025 cm (0.010 inch) between the rotor disk and the stator and a 0.475-cm (3/16-inch) clearance between the rotor and the clamp. In this position, the clamp should be clamping on the splits cut into the sleeve of the rotor, ensuring that the rotor is fastened securely to the reel motor shaft. When clearances are correct, tighten the Allen screw.

g.   With the 0.025-cm (0.010-inch) feeler gauge inserted between the stator and the rotor,4 rotate the reel motor manually from the front of the unit to see that the brake is spaced uniformly all around. If necessary, rotate the brake at 120-degree intervals to determine the best position for uniform separation. (An excessively high or low spot is cause for replacing the brake assembly.)

h.   Remount the rotor spring between the rotor disk and the rotor.

i.   When the above steps have been completed for both reels, rotate both reels, feeling for free rotation and listening to ensure that there is no squealing from stator/rotor disk contact.

5-11

2. With the power off, check for correct vacuum system belt tension as follows:

   a. Position the belt tension gauge as shown in Figure 5-6.
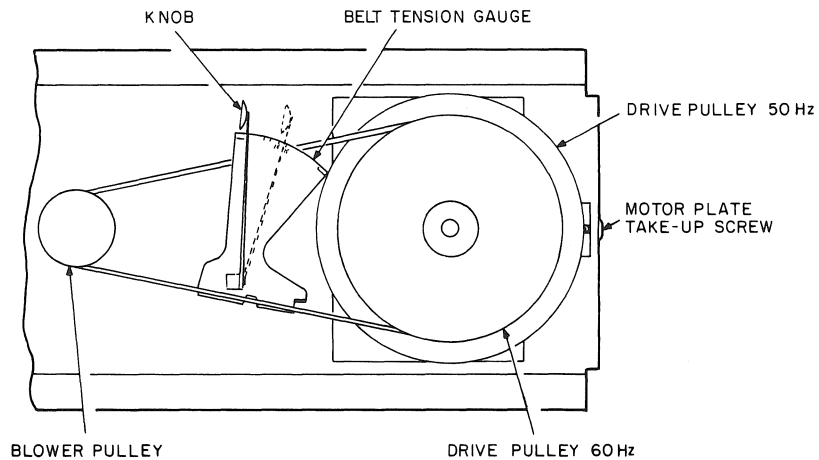
Figure 5-6 Belt Tension Gauge

   b. Push against the knob at the end of the spring until the third tab on the gauge just touches the belt.

   c. Read the tension from the scale just under the spring. If the reading is not between 2.25 and 3.6 kg (5 and 8 lb), adjust the belt tension adjustment screw for 2.25 kg (5 lb).

5.4.2.2 Voltage Check Setup – Set up as follows to check voltages:

1. Turn power off; remove M8912 [Test Function Generator (TFG)] from slot EF3 and place it on the module extender in slot AB3.

2. Place the SSRD, SSWRT, and WRT switches down; turn power on.

NOTE
In all voltage checks, refer to Figure 5-7 for the location of the potentiometers that control adjustments. If any voltages cannot be adjusted to meet specifications, repair or replace the regulator boards.
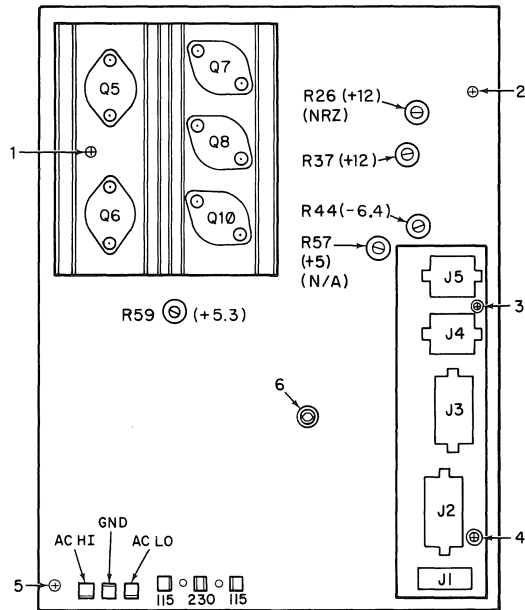
NOTES:
1) 1-5 represent 5 Phillips head screws.

2) 6 represent Allen screw—must be secured very tightly, or damage to the power supply may result.

11-4683

Figure 5-7   TU10W Power Supply Regulator Board

5.4.2.3   +5 Vdc Check (Drive Logic) – Check the +5 Vdc drive logic voltage:

Reference Point   D01A2 (red wire)
Nominal Value   +5.25 ± 0.05 V

If adjustment is necessary, adjust potentiometer R59.

5.4.2.4   +12 Vdc Check (Drive Logic) – Check the +12 Vdc drive voltage.

Reference Point   A04V1 (yellow wire)
Nominal Value   +12.05 Vdc ± 0.05 V

If adjustment is necessary, adjust potentiometer R37.

5.4.2.5   –6.4 V Check – Check the –6.4 Vdc drive voltage.

Reference Point   C04N2 (green wire)
Nominal Value   –6.35 Vdc ± 0.05 V

If adjustment is necessary, adjust potentiometer R44.

5.4.2.6 +12 Vdc Check (NRZ) – With S5-9 (M8912) on, check the +12 Vdc (NRZ) drive voltage:

Reference Point   C02J2 (orange wire)
Nominal Value   +11.875 Vdc ± 0.125 Vdc

If adjustment is necessary, adjust potentiometer R26.

NOTE
**The remaining steps in this PM procedure require a
well-calibrated oscilloscope. It is advisable to check
the voltage and frequency calibration at this time,
with the probes intended for use.**

5.4.2.7 Forward Tape Speed and DC Balance Check – Check forward tape speed and dc balance:

1. Turn power off; disconnect the erase head cable (the 2-pin connector located just below the read/write head) and the write head cable (located directly above the erase head connector).

2. Turn power on; load a master skew tape and position it at BOT.

3. Set the vertical gain of the oscilloscope to 50 mV/cm.

4. Slowly adjust R21 (BAL) on the H606 power board to obtain 0.0 V ± 0.04 V at test point 2.

NOTE
**50 mV of ac ripple will be displayed; center the ac
ripple on ground to obtain a 0 Vdc level.**

5. Set the oscilloscope as follows:

    10 μs/cm
    Channel 1   2 V/cm
    Triggering   Normal
                       Negative slope
                       Channel 1 triggered

    Channel 1 probe to C4-U1.

6. Initiate FWD tape motion; check that negative pulses are 55--57 μs apart (Figure 5-8). If not, adjust FWD potentiometer R13 on H606 for 56 μs.
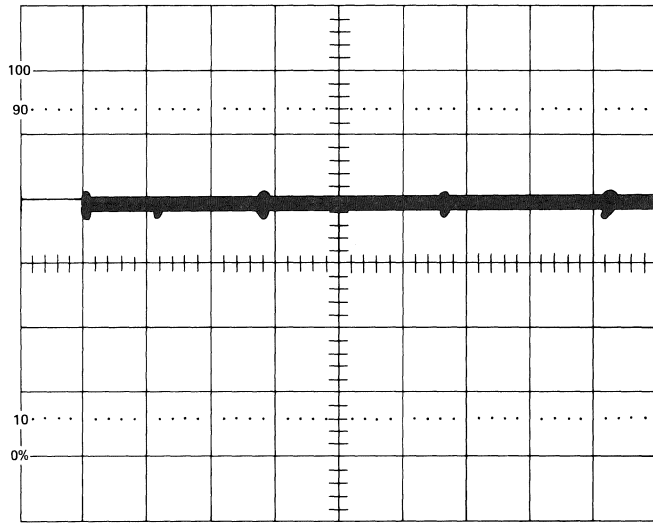
BU-0614

Figure 5-8   Tape Speed Check

5.4.2.8   Reverse Tape Speed Check – Initiate REV tape motion; check that negative pulses are 55–57 μs apart. If not, adjust REV potentiometer R12 on H606 for 56 μs.

5.4.2.9   Forward Jitter Check – Check forward jitter as follows:

1.   Change sweep to 20 μs/cm; initiate FWD tape motion. Check that four negative pulses appear on the oscilloscope screen (Figure 5-9).
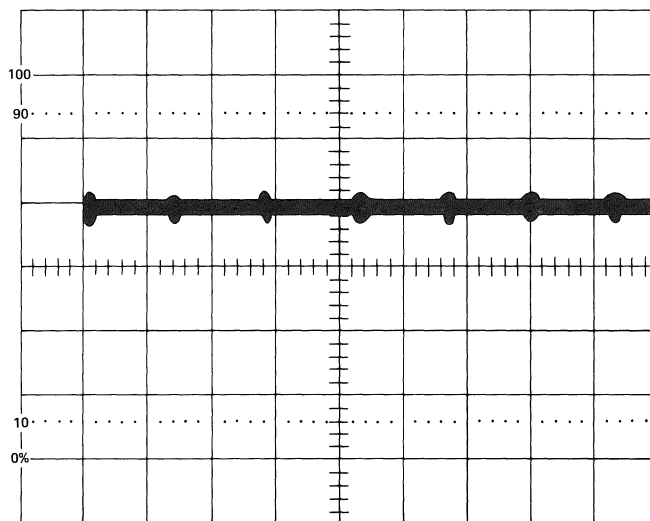
BU-0615

Figure 5-9   Jitter Check

2. Use the horizontal X10 magnifier to increase the horizontal display. Using the horizontal position knob, place the third pulse in the center of the screen. Check that the jitter is less than 6 μs (3 cm on the scope, as indicated in Figure 5-10). If jitter exceeds 6 μs (as in Figure 5-11), replace the capstan motor.

NOTE
If it is necessary to replace the capstan motor, tape path alignment must be performed at the same time.
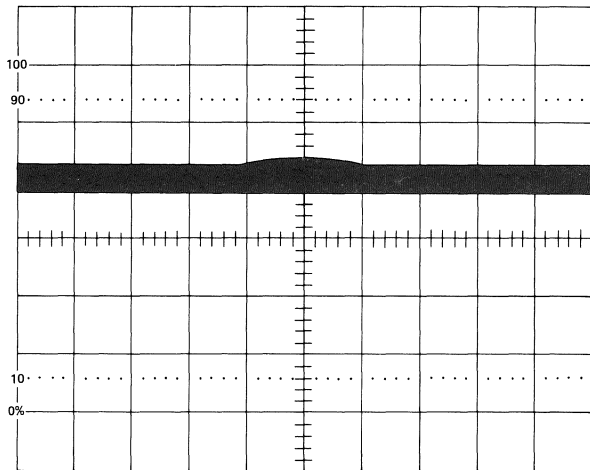
BU-0616

Figure 5-10   Good Capstan Motor
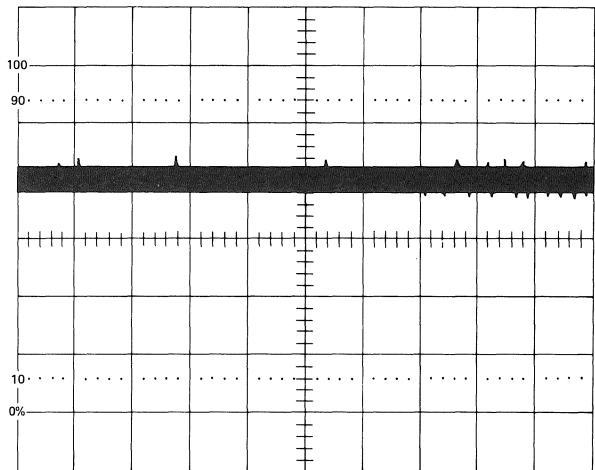
BU-0617

Figure 5-11   Bad Capstan Motor

5.4.2.10   Reverse Jitter Check – Initiate REV tape motion; repeat the procedure outlined in Paragraph 5.2.4.9 to check reverse jitter. Remove the X10 horizontal magnification on the oscilloscope.

5.4.2.11   Forward Skew Check – Perform mechanical skew (head azimuth) adjustment as follows:

1. Set up oscilloscope as follows:

   1 μs/cm
   Channel 1   2 V/cm
   Triggering   Normal
                    Positive slope
                    Channel 1 triggered
   Channel 1 probe to E4K1 (PACKET H).

2. Initiate FWD motion; synchronize the scope. Adjust the Phillips head screw on the head plate for minimum PACKET width (must be less that 2.5 μs). (See Figures 5-12 and 5-13.)

5-16
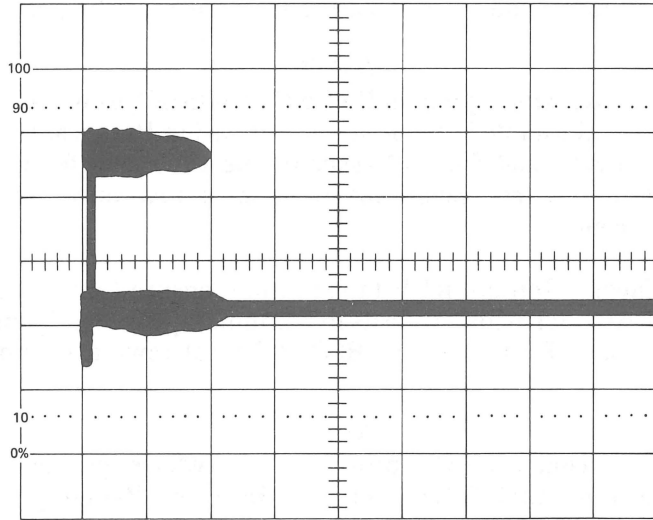
BU-0618

Figure 5-12   PACKET Waveform
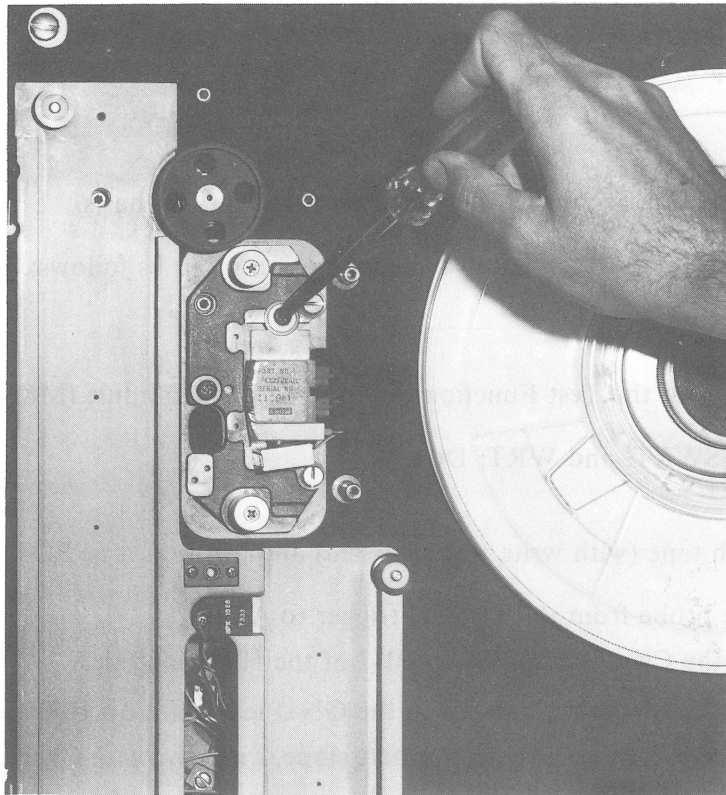
Figure 5-13   Adjusting Mechanical Skew

If adjustment cannot be made, tape path alignment must be performed at this time.

NOTE
An occasional jump in PACKET width of 1 μs is usually allowable in the procedures listed in Paragraphs 5.4.2.11 and 5.4.2.12 (usually due to tape defect); however, this should not occur more than once per second.

5.4.2.12 Reverse Skew Check – Initiate REV tape motion; ensure that width is less than 3.5 μs. (No adjustment is possible; if PACKET width exceeds maximum, tape path alignment must be performed.) Allow skew tape to continue in REV mode to BOT. (Do not rewind.) Remove skew tape. Connect write and erase heads.

NOTE
If a semiannual PM procedure is scheduled, proceed to Paragraph 5.4.3; if not, continue with Paragraph 5.4.2.13.

5.4.2.13 Test Function Generator (TFG) Relocation – Relocate the TFG as follows:

1. Turn power off.
2. Remove the TFG from slot AB03 and plug it into slot EF03.
3. Turn power on.

NOTE
Return to Paragraph 5.4.1.4 of the monthly PM procedures.

5.4.3 Semiannual PM Schedule
The items listed in this section are to be performed on a semiannual basis.

5.4.3.1 Forward Ramp Check – Adjust forward acceleration ramp as follows:

1. Connect the oscilloscope.

2. Set the switches of the Test Function Generator (TFG) module (M8912) as follows:

    SSRD, SSWRT, and WRT: Down
    S4-9: OFF

3. Load a scratch tape (with write ring installed) and position it at BOT.

    a. Place the probe from the external trigger to A3S1.
    b. Connect the Channel 1 probe to P1-7 of the H606 module.
    c. Connect the Channel 1 ground to the GND test point on H606 (adjacent to P3-4).
    d. Set the scope to external sync, negative slope, 2 ms/cm, with Channel 1 to 0.2 V/cm (20 mV/cm if X10 probe is used).

4. Set FWD/REW/REV switch to FWD. Place the SSRD switch on TFG (M8912) up. Observe a negative slope of 7–8 ms (Figure 5-14.) Adjust –CUR potentiometer on H606, if necessary.
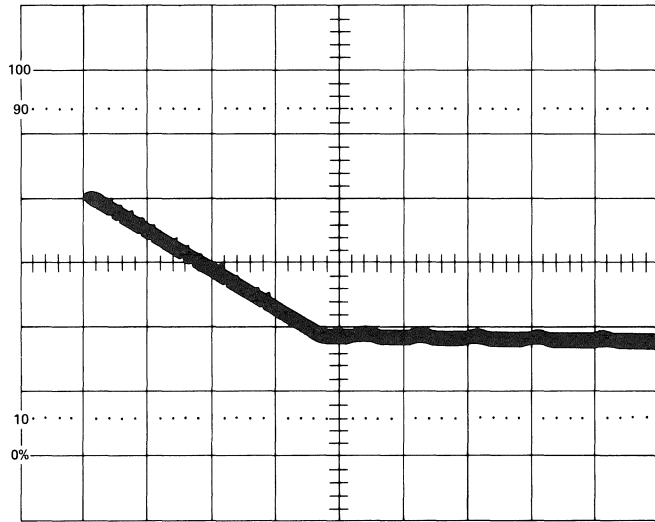
BU-0619

Figure 5-14   Forward Acceleration Ramp

5.4.3.2   Reverse Ramp Check – Adjust reverse acceleration ramp as follows:

1.   Set FWD/REW/REV switch to REV. Observe positive slope of 7–8 ms (Figure 5-15.)

2.   Adjust +CUR potentiometer on H606, if necessary.
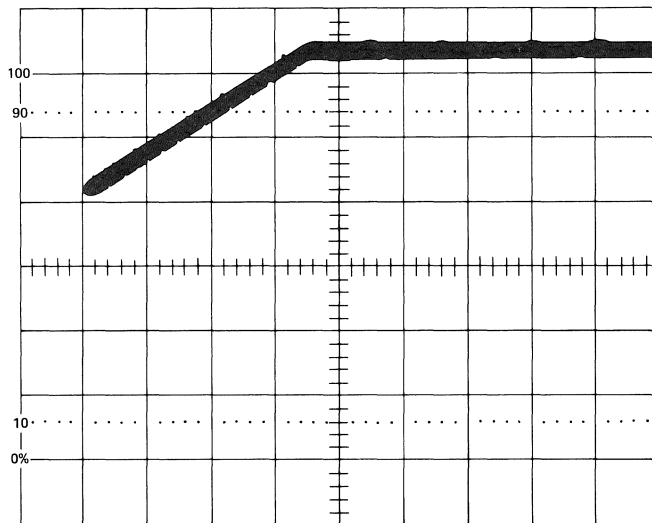
BU-0620

Figure 5-15   Reverse Acceleration Ramp

5.4.3.3 Tracking Check – Place SSRD switch on TFG (M8912) down. Rewind tape. Remove the float from scope ground. Check the industry-compatible tape tracking as follows:

1. Set up the TFG as follows:

    SSWRT, SSRD, and WRT: Down
    S5: 1-8 OFF
    S5: 9 and 10 ON
    S6: 1-10 OFF

2. Set the FWD/REW/REV switch to FWD. Place SSRD momentarily up, then down. (This loads data into the TFG write buffer.)

3. Position tape at BOT.

4. Place the WRT switch of the TFG up; press FWD and START on the control panel.

5. Allow the tape to be written for 10 seconds; ensure that the WRT indicator on the control panel is on as the tape is being written.

6. Place the WRT switch down; rewind tape.

7. Remove the tape from the drive, take it to a work area, and proceed as follows:

    a. Unwind tape until you reach the BOT marker; cut the tape with scissors.

    b. Unwind 93 cm (3 feet) of tape beyond the BOT marker; cut the tape again.

    c. Shake Magna-See solution vigorously.

    d. Dip the 93-cm (3-foot) section of tape in Magna-See solution (Figure 5-16.) Try to keep a loop of tape at the bottom of the can.
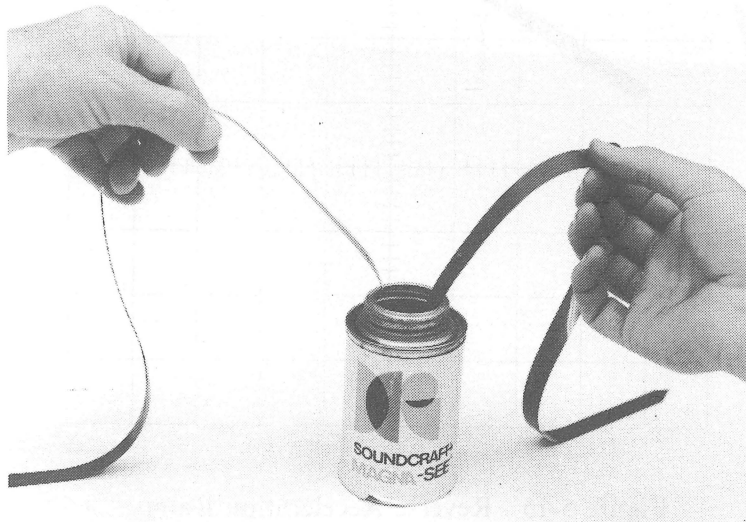
7660-24

Figure 5-16   Developing Magnetic Tape

e. Work the tape back and forth until the entire 3-foot section (except for the ends being held) has been dipped into the solution.

f. Allow the tape to dry. Data written on the tape should appear as the solution dries (Figure 5-17.) If necessary, dip the tape again.


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7660-27
TU45A/TM03
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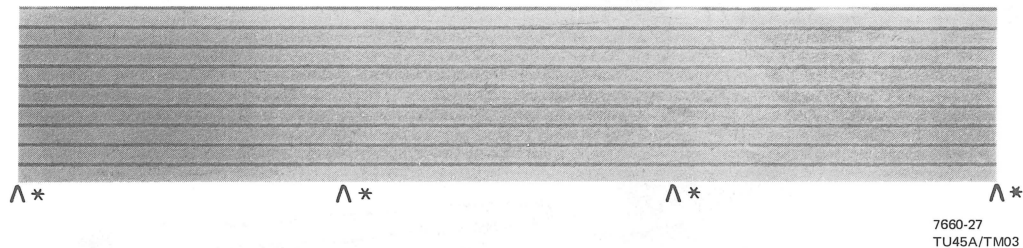
Figure 5-17   Developed Magnetic Tape

8. When the tape has been developed, proceed as follows:

a. Place the developed tape flat on a white background (e.g., white sheet of paper).

b. Make sure that the tape is flat, then place a weight on each end.

c. Check four points along the reference edge (edge with BOT marker) 3.8 cm (1-1/2 inches) apart. (Refer again to Figure 5-17.)

d. Set up a microscope according to Figure 5-19; lay the penlight flat on the table, positioned so that it shines on the reflector.

e. Ensure a distance of 0.178 ± 0.076 mm (0.007 ± 0.003 inch) from the reference edge to track 1 (inset in Figure 5-18) at each of the four points mentioned in Step c, above.

NOTE
If the tracking check described above fails, tape path alignment must be performed at this time.

9. Install a new BOT marker 4.58 m (15 feet) from the front of the tape on the non-oxide side, against the reference edge. (The reference edge faces the operator when the tape is installed on the transport.)
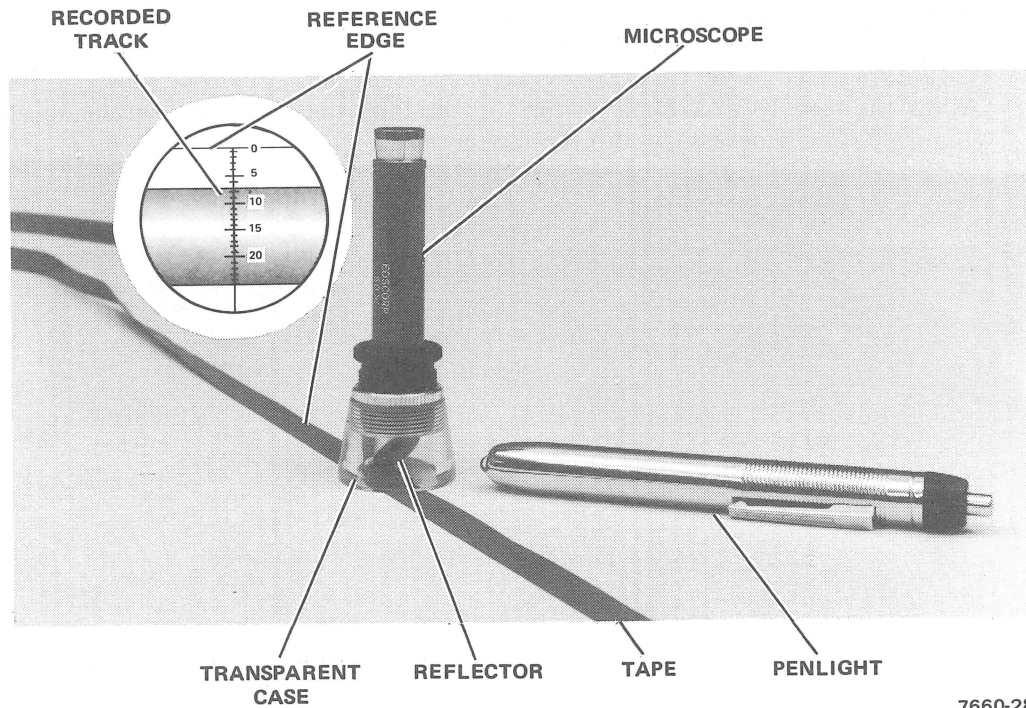
Figure 5-18   Track No. 1 to Reference Edge Measurement

5.4.3.4 Erase Head Check – Check the erase head function as follows:

1. Load the tape and position it at BOT.

2. Set up TFG as follows:

      SSWRT, SSRD, and WRT: Down
      S5: 1-8 OFF
      S5: 9 and 10 ON
      S6: 1-10 OFF

3. Set the FWD/REW/REV switch to FWD. Place SSRD momentarily up, then down.

4. Place the WRT switch on the TFG up; press FWD and START on the control panel. Allow tape to be written for 30 seconds.

NOTE
Steps 1 through 4, above, are recording an all-1s tape at low density (full saturation). The steps below check the ability of the TU10W to erase a saturated tape.

5-22

5. Press STOP on the control panel. Place the WRT switch down. Rewind tape.

6. Set up the TFG as follows:

  S4: 1-8 ON
  S4: 9 and 10 OFF
  S5: 1-8 ON
  S5: 9 and 10 OFF
  S6: 1-10 ON
  SSWRT, SSRD, and WRT: Down

7. Press FWD on the control panel and place SSWRT on the TFG up; allow tape to be written for 1 minute.

8. Lower the SSWRT switch; rewind tape.

9. Set up the oscilloscope as follows:

  1 ms/cm
  Channel 1   50 mV/cm
  Triggering   Auto, Channel 1 triggered
  Channel 1 probe on A4-L1
  Channel 1 probe ground on B4-C2.

10. Press FWD and START on the control panel.

11. Measure unerased signal level for maximum level. (Ensure good scope ground.) Maximum level must be less than 300 mV. Failure of this check will require replacement of the head plate assembly. (Tape path alignment must be performed at this time.) Figure 5-19 is an example of acceptable erasure.
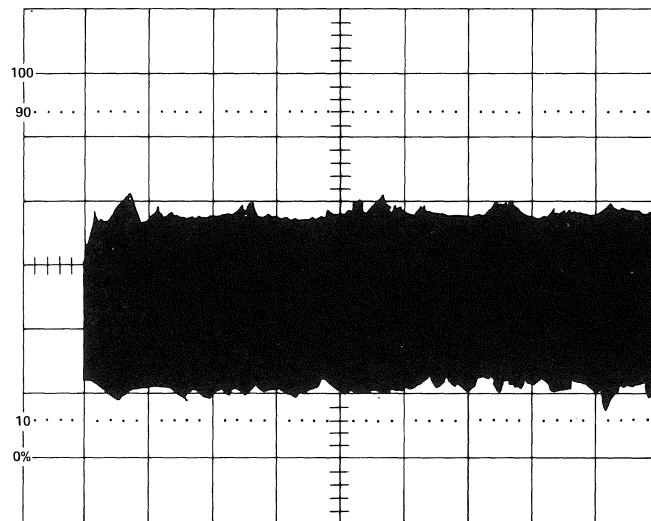
BU-0621

Figure 5-19   Acceptably Erased Signal

12. Rewind tape. Place the Channel 1 scope probe on C4-L1. (Ensure good ground.) Initiate forward motion. Check unerased signal level (max = 300 mV).

13. Rewind tape. Place the Channel 1 scope probe on F4-R1. (Ensure good ground.) Initiate forward motion. Check unerased signal level (max = 300 mV).

NOTE
The remaining tests require comparison of read amplifier outputs under varied conditions. Photocopy the table shown in Figure 5-20, or prepare a similar table.

Track	Pin No.	Read Amplitude	Residual Amplitude	Reverse Amplitude
1	A4-L1			
2	B4-B1		N/A	N/A
3	B4-M1		N/A	N/A
4	C4-K1		N/A	N/A
5	C4-L1			
6	D4-P1		N/A	N/A
7	D4-R1		N/A	N/A
8	F4-P1		N/A	N/A
9	F4-R1			

Figure 5-20   Sample Table for Read Amplifier Comparisons

5.4.3.5 Read Amplifier Check – Check read amplifier outputs as follows:

1. Rewind the tape and remove from transport.

2. Clean the read/write head, erase head, and tape cleaner.

3. Load a good quality tape, positioned at BOT; set up the scope as follows:

Channel 1	2 V/cm
Sweep speed	2 ms/cm
Trigger	Normal, Channel 1 triggered

4. Set the switches on the TFG as follows:

   S4: 1-8 ON
   S4: 9 and 10 OFF
   S5: 1-8 OFF
   S5: 9 and 10 ON
   S6: 1-8 OFF
   S6: 9 and 10 ON
   SSWRT, SSRD, and WRT: Down

5. Place the SSWRT switch in the TFG up and place the Channel 1 probe on A4-L1. The scope presentation should resemble Figure 5-21.
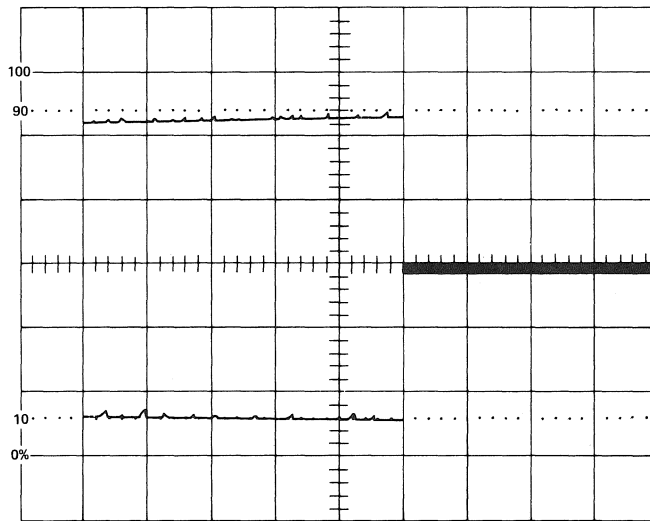
BU-0622

Figure 5-21   Read Amplifier Output

6. Increase vertical sensitivity to 1 V/cm and place interrecord gap 1 cm down from top. Measure negative half of read amplifier output (using the interrecord gap as the baseline). The peak amplitude of the negative-going signal should be from –4.45 to –4.75 V (Figure 5-22.) Record the results in the Read Amplitude column of the table (photostated from Figure 5-20 or prepared previously) beside Track 1.

BU-0623
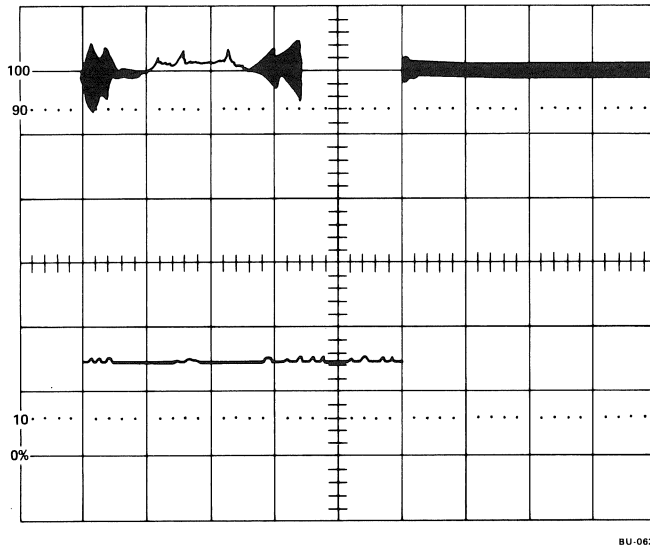
Figure 5-22   Negative Half of Read Amplifier Output

7.   Repeat Step 6 for all nine tracks, recording the results in the same table. If any track is out of the acceptable range (–4.45 to –4.75 V), adjust all nine channels to –4.6 V. Such adjustment requires the following procedure:

a.   Turn power off.

b.   Take the TFG off the extender.

c.   Place G056 on the extenders.

d.   Turn power on.

e.   Adjust all read amplifiers to –4.6 V. (Potentiometers are arranged sequentially from top to bottom, starting with Track 1.)

NOTE
If any channel cannot be adjusted within range, the TU10W input preamplifier resistors may have to be changed.

8.   Place the SSWRT switch on the TFG down; rewind the tape.

5.4.3.6   Residual Amplitude Check – Perform the residual amplitude check as follows. (Residual amplitude is the amplitude left on the tape after several read operations. Some amount of erasure can be expected during the first few read passes, due to residual magnetism in the write and erase heads.)

1.   Press FWD; raise SSWRT. Allow start/stop data to be recorded for at least 20 seconds, then place SSWRT down and rewind tape.

2.   Initiate FWD tape motion; allow the tape to run in the forward direction for 10 seconds. Rewind tape. Repeat this operation ten times.

3. Leave scope setup as it was after the last step of Paragraph 5.3.4.5. Place the Channel 1 probe on A4-L1. Initiate FWD motion. Record the negative read amplifier output in the Residual Amplitude column of the table. Rewind tape.

4. Place the Channel 1 probe on C4-L1. Initiate FWD motion. Record the negative read amplifier output in the Residual Amplitude column of the table. Rewind tape.

5. Place the Channel 1 probe on F4-R1. Initiate FWD motion. Record the negative read amplifier output in the Residual Amplitude column of the table.

NOTE
It is assumed that tape did not run more than 10 seconds forward during Steps 3, 4, and 5, above. If there is any doubt of this, rewind tape and recheck residual amplitude.

6. Compare the entries in the Residual Amplitude column of the table with the entries in the Read Amplitude column. If the Residual Amplitude entries show a decrease of greater than 20 percent on any of the three tracks, replace the head plate assembly.

5.4.3.7 Reverse Amplitude Check – Perform the reverse amplitude check as follows:

1. Rewind tape.

2. Place the Channel 1 probe on A4-L1; run tape FWD from BOT for 10 seconds. Initiate REV tape motion; record the negative read amplifier output in the Reverse Amplitude column of the table.

3. Place the Channel 1 probe on C4-L1; run tape FWD from BOT for 10 seconds. Initiate REV tape motion; record the negative read amplifier output in the Reverse Amplitude column of the table.

4. Place the Channel 1 probe on F4-R1; run tape FWD from BOT for 10 seconds. Initiate REV tape motion; record the negative read amplifier output in the Reverse Amplitude column of the table.

5. Compare entries in the Reverse Amplitude column of the table to the entries in the Residual Amplitude column. If the Reverse Amplitude entries show a decrease of greater than 10 percent, the tape path alignment must be performed at this time.

NOTE
Perform Paragraph 5.4.2.13 at this time.

5.5 ADJUSTMENTS AND ALIGNMENT PROCEDURES
No adjustments exist for the M8926 Interface module. Adjustments and alignment procedures relative to the TU10W Host Drive and the TMB11 Controller are provided in this section.

5.5.1 Adjustment Procedure
This section contains all the procedures required to adjust the TMB11/TU10W DECmagtape System. Paragraphs 5.5.1.1 through 5.5.1.11 relate to the TU10W, while Paragraph 5.5.1.12 relates to the TMB11.

5.5.1.1 TU10W Power Supply – Four adjustments to the power supply adjust the four dc output voltages: +5.3 V, +12 V, + 12 V, and –6.4 V. A small screwdriver is all that is required. Clockwise adjustment of any of the potentiometers increases voltage. All potentiometers are located on top of the TU10W power supply board. Refer to Figure 5-7 for the respective locations and to Table 5-3 for adjustment values. Do not make adjustments if voltages are within tolerances of Table 5-3.

Use a calibrated voltmeter, preferably a digital voltmeter. Voltages should be adjusted to the values indicated in Table 5-3.

CAUTION
Do not adjust voltages beyond their 105 percent rating and adjust slowly to avoid overvoltage crowbar.

Table 5-3   TU10W Power Supply Regulated Voltages

J5 Connector Pin Number	Adjustment Potentiometer	Voltage (Under Load) (Volts)	Wire Color Code
1	R59	5.2 to 5.3	RED
4	R44	–6.3 to –6.4	GRN
5	R37	12.0 to 12.1	YEL
8	R26	12.0 to 12.4 (NRZ)	ORN

5.5.1.2   Capstan Servo DC Balance – To perform the capstan servo dc balance adjustment, proceed as follows:

1. Pull the TU10W Tape Transport out on its slide mount.

2. Apply power to the TU10W and place the unit off-line.

3. Place the control panel START/STOP switch on STOP.

4. Set up to measure the voltage at test point 2 of the TU10W's H606 power board.

5. Slowly adjust R21 on the H606 power board to obtain 0.0 V ± 0.04 V at test point 2.

6. Check capstan speed (Paragraph 5.5.1.3).

5.5.1.3   Capstan Speed – Potentiometers are located on the H606 to adjust the FWD, REV, and REW speeds. To check and adjust capstan speed, proceed as follows:

1. Load a master skew tape (800 bits/inch).

2. Place an oscilloscope probe on pin CU1 of the Read Amplifier (G056).

3. Initiate FWD tape motion and measure a 100- to 400-ns pulse with a period of 56.0 μs as shown in Figure 5-23.

—56.0 μs—
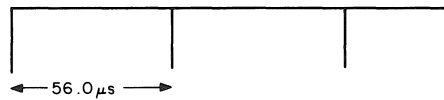
11-4673

Figure 5-23   Capstan FWD and REV Speed Waveforms

4. If necessary, adjust the FWD potentiometer (R13).

5. Initiate REV tape motion; conditions should be identical to those observed in Step 3.

6. If necessary, adjust the REV potentiometer, R12.

7. Remove the master skew tape and load a scratch tape.

8. With the TFG configured for 800 bits/inch, write an all 1s pattern on the tape.

9. After ensuring that there is adequate tape on the take-up reel, run the TU10W in REW. Observe a wave pattern similar to that shown in Figure 5-23, except that the period between pulses is approximately 16.6 μs.

10. If necessary, adjust the REW potentiometer (R11).

11. Perform capstan acceleration and deceleration adjustment (Paragraph 5.5.1.4).

5.5.1.4 Capstan Acceleration and Deceleration Times – Capstan acceleration and deceleration times are best measured while running the SSRD test with the Test Function Generator. To check the capstan acceleration and deceleration times, proceed as follows:

1. Connect oscilloscope channel A to the tachometer signal found on the H606 at P1 pin 7.

2. Connect the oscilloscope EXT TRIG to pin A3S1 (FIRST ONE SHOT L) of the TU10W backplane.

3. Set the scope controls as follows:

        Channel A   0.2 V/cm
        Time/Div   2 ms/cm
        A TRIG   EXT, negative slope

4. With the Test Function Generator (TFG) module, initiate an SSRD function in the FWD direction, and adjust R89 on the H606 to obtain a negative slope of 7–8 ms duration on the scope (Figure 5-24a).

5. With the TFG, initiate an SSRD function in the REV direction, and adjust R90 on the H606 to obtain a positive slope of 7–8 ms duration on the scope (Figure 5-24b).

NOTE
Deceleration times are not adjustable, and will be somewhat shorter than the acceleration times.
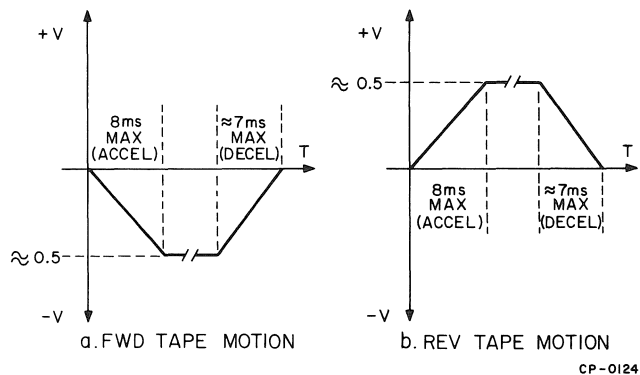
Figure 5-24   Acceleration and Deceleration Times

5.5.1.5   Brake Adjustment (Electrical) – To ensure proper operation of the TU10W, an adjustment to the brake circuit may be necessary after normal wear or long periods of inactivity. In addition, brake operation must be checked after cleaning the brake armature. The TU10W brake circuitry has two adjustments that affect brake operation during rewind. Both adjustments affect only the upper brake and upper vacuum column.

Proceed as follows to perform a visual check of the rewind operation:

1. Place the TU10W in the off-line mode and move tape to EOT.

2. Initiate the rewind operation from EOT several times. Allow the operations to continue approximately 10 seconds before returning to EOT.

3. Initiate the rewind operation and continue to the BOT marker. Check for an improperly adjusted brake circuit by watching for any of the following symptoms during the rewind operation:

   a. Any vacuum column failure.

   b. More than two or three tape loop excursions exceeding approximately one-third of the distance into the brake zone. During acceleration from EOT, two or three large excursions are normal.

   c. Normal tape loop excursions during acceleration but a sluggish return of the tape loop from the reel motor zone to the brake zone.

   d. Erratic tape loop excursions during the continuous rewind operation exceeding 3.17 cm (1-1/4 inches) above the upper vacuum column upper vacuum switch. Tape motion will always be somewhat erratic, but the magnitude of the loop "jumps" should be less than 3.17 cm (1-1/4 inches).

In almost every case, a tape loop failure can be diagnosed as an extreme example of symptoms b, c, or d.

Continuous large tape loop excursions (symptom b) are probably due to one of the following:

1. High current rewind time is too short. The high current rewind time is measured as a negative pulse at test point 18 of the H606 power board during a rewind operation. Typical pulse width is 20–25 ms. It is adjusted using the REW PULSE potentiometer (R61) on the H606 power board.

2. Low current rewind amplitude is too low. The amplitude is adjusted using the LOW CURRENT ADJ potentiometer (R79) on the H606 power board. Clockwise rotation of the potentiometer increases the current to the brake. Adjustment should be made at intervals not greater than two turns of the potentiometer.

Symptom c is an indication that the low current rewind amplitude is too high. Counterclockwise adjustment of the LOW CURRENT ADJ potentiometer (R79) on the H606 power board will decrease the amplitude. The effects of the potentiometer adjustment should be observed at intervals of two turns of the potentiometer.

Symptom d is an indication that the high current rewind time is either above or below the ideal operating range. The 20–25 ms range is a helpful guideline, but is not absolute, and will depend on the operation of the brakes.

5.5.1.6 **Read Amplitude Adjustment**

1. Check capstan speed (Paragraph 5.5.1.3) and adjust if necessary.

2. Rewind the tape and remove it from the transport.

3. Clean the read/write head, erase head, and tape cleaner.

4. Load a good quality tape, positioned at BOT; set up the scope as follows:

Channel 1	2 V/cm
Sweep Speed	2 ms/cm
Trigger	Normal, Channel 1 triggered

5. Set the switches on the TFG as follows:

    S4: 1-8 ON
    S4: 9 and 10 OFF
    S5: 1-8 OFF
    S5: 9 and 10 ON
    S6: 1-8 OFF
    S6: 9 and 10 ON
    SSWRT, SSRD, and WRT: Down

6. Place the SSWRT switch in the TFG up, and place the Channel 1 probe on A4-L1. The scope presentation should resemble Figure 5-25.

BU-0622
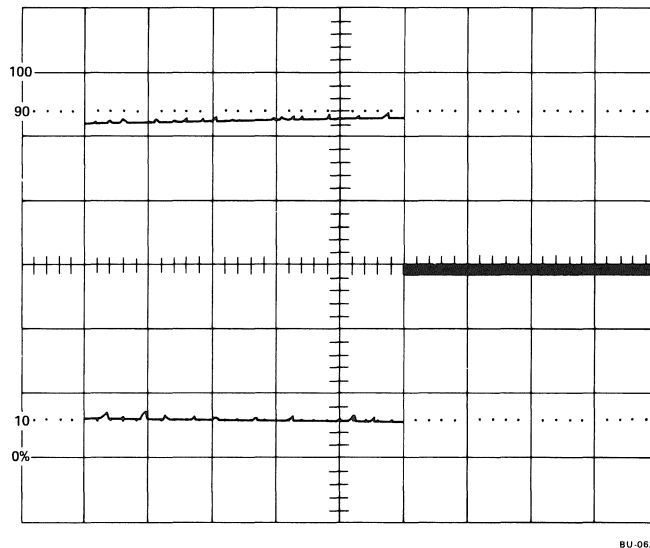
Figure 5-25   Read Amplifier Output

7. Increase vertical sensitivity to 1 V/cm and place the inter-record gap 1 cm down from the top. Measure the negative half of the read amplifier output (using the inter-record gap as the baseline). The peak amplitude of the negative-going signal should be from –4.45 to –4.75 V (Figure 5-26).

8. Repeat Step 7 for all 9 tracks. See Table 5-4.

BU-0623
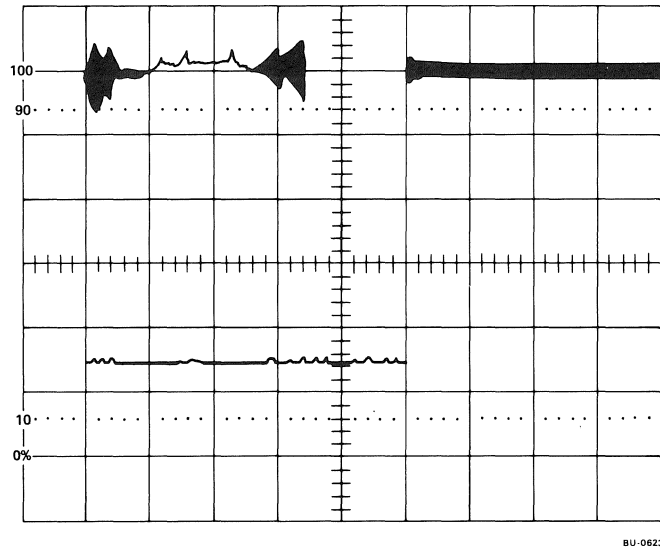
Figure 5-26   Negative Half of Read Amplifier Output

Table 5-4   Read Amplitude Test Points

Track	Pin
1	A4-L1
2	B4-B1
3	B4-M1
4	C4-K1
5	C4-L1
6	D4-P1
7	D4-R1
8	F4-P1
9	F4-R1

If any track is out of the acceptable range (−4.45 to −4.75 V), adjust all nine channels to −4.6 V. Such adjustment requires the following procedure:

a.   Turn power off.

b.   Take the TFG off the extender.

c.   Place G056 on extenders.

d.   Turn power on.

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e. Adjust all read amplifiers to –4.6 V. (Potentiometers are arranged sequentially from top to bottom, starting with Track 1.)

NOTE
If any channel cannot be adjusted within range, the TU10W input preamplifier resistors may have to be changed.

9. Place the SSWRT switch on the TFG down; rewind the tape.

5.5.1.7 Write Skew Adjustment – The procedure should be performed only after completing the read skew adjustment (Quarterly PM item in Paragraph 5.4.2). Write skew adjustment is only required upon replacement of the head plate assembly, or when excessive wear in the head plate assembly is suspected.

1. Slide the TU10W Tape Transport out of the cabinet.

2. With power removed from the transport, remove the Test Function Generator (TFG) module (M8912) from section EF of slot 3.

3. Set the TFG switches as follows:

    S5: 1-8 OFF
    S5: 9 ON
    S5: 10 OFF
    S6: 1-8 OFF

4. Insert TFG into section AB of slot 3.

5. Ensure that the SSRD, WRT, and SSWRT switches at the upper portion of the module are in the lowered position.

6. Apply power to the TU10W. The LED indicator on the TFG should light.

7. Load write-protected IBM skew tape (800 bits/inch) on the transport.

8. Initiate forward tape motion from the transport control panel.

9. Connect the channel A input of an oscilloscope to pin E4K1 (PACKET), using internal sync, negative slope. PACKET is a composite signal, comprised of read amplifier outputs of all nine tracks.

10. Monitor the pulses which comprise PACKET on Channel B of the scope, using chopped mode. Note and tabulate their positions, in microseconds, with respect to the leading edge of PACKET (Figure 5-27). Table 5-5 lists the pins to be monitored for each track; it also contains a column, left blank, for listing the position of the monitored pulses relative to PACKET, and can therefore serve as a model to the user.
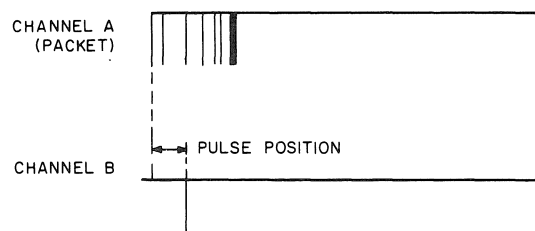
Figure 5-27 Measurement of Pulse Positions Relative to Packet

Table 5-5 Write Deskew Parameters

Track No.	Pin	Measured Pulse Position (μs)
1	A4J1	
2	A4H1	
3	B4N1	
4	B4L1	
5	C4U1	
6	C4S1	
7	E4H1	
8	E4F1	
9	F4M1	

11. After tabulating the data for all nine tracks, terminate tape motion.

12. Unload the skew tape and load a scratch tape on the transport.

13. Raise and lower the TFG SSRD switch; this loads the preselected data pattern.

14. Raise the TFG WRT switch. Now initiate forward tape motion from the transport control panel. The TU10W will perform a continuous write operation.

15. Monitor the pins that were monitored in Step 10. Note the position of the displayed pulses relative to the leading edge of PACKET. If the position measured now differs from the position measured in Step 10 by more than 2 μs, alter the write deskew jumper configuration on the TU10W backplane. The jumpers connect the write deskew buffer (refer to drawing M8910, sheets 3 and 4) to four record pulses (SK CLK A, SK CLK B, SK CLK C, and SK CLK D) which are shift delayed in increments of 0.9 μs. These pulses are available at the following pins:

SK CLK A	A2R1 and A2R2
SK CLK B	A2N1 and A2N2
SK CLK C	A2L1 and A2L2
SK CLK D	A2B1 and A2B2

The jumper configuration must be modified so that the position of the monitored pulse with respect to the leading edge of PACKET does not vary by more than 2 μs from that obtained in Step 10.

16. After performing the write skew adjustment, remove power from the transport and replace the TFG module in section EF of slot 3.

5.5.1.8 Read/Write Interlock Assembly – Proceed as follows to perform the read/write interlock assembly adjustment (Figure 5-28):

1. Loosen the two screws securing the switch to the bracket just enough to allow the switch to be moved.

2. Loosen the locknut and adjusting screw several turns (see detail B, Figure 5-28).

3. Insert the small end of the setting gauge (29-18610) in front of the roll pin through the bottom of the bracket body edge. Tighten the adjusting screw until the switch just actuates.

4. Tighten the two screws securing the switch to the bracket and lock the adjusting screw using the locknut.

5. Loosen the two solenoid mounting screws (detail A, Figure 5-28).

6. Insert the large end of the setting gauge in front of the roll pin as described in Step 3. Push the solenoid body forward until the plunger bottoms out; then tighten the solenoid mounting screws, keeping the solenoid body parallel to the upper edge of the bracket.

7. Loosen the bottom screws securing the interlock assembly to the mounting bracket (detail C, Figure 5-28).

8. Insert the ring gauge (29-18608) on the reel, lock it, and spin the reel to check for even rotation.

9. Push the interlock assembly forward until the shaft bottoms in the solenoid and the small spring is fully depressed.

10. Tighten the screws securing the assembly to the bracket, remove the ring gauge, and check for free movement of the solenoid shaft in the casting.

5.5.1.9 Vacuum Motor Belt Adjustment – Proceed as follows to adjust the vacuum motor belt:

1. Tighten the four motor plate mounting nuts.

2. Using gauge 74-16187, set the pulley height to 1.32 cm or 2.08 cm (0.520 inch or 0.820 inch).

NOTE
The pulley is positioned either **1.32 cm or 2.08 cm
(0.520 inch or 0.820 inch)** above the mounting assembly to accommodate 60 or 50 Hz operation, respectively (selects one of two pulley diameters). For further information, refer to the vacuum assembly drawing E-AD-7009638-0-0.

SOLENOID WIRES

A

SOLENOID (ADJUSTABLE)

SOLENOID MOUNTING BRACKET

SOLENOID SHAFT

B   C

SWITCH (ADJUSTABLE)

SWITCH
CONNECTING
PINS (3)

C

INTERLOCK ASSEMBLY
ADJUSTMENT
SCREWS
(UNDERSIDE OF
MOUNTING BRACKET)

A

SOLENOID
ADJUSTMENT
SCREWS (LEFT OF
INTERLOCK ASSEMBLY
AS VIEWED FROM
FRONT OF TU16)

B

SWITCH
ADJUSTMENT
SCREW
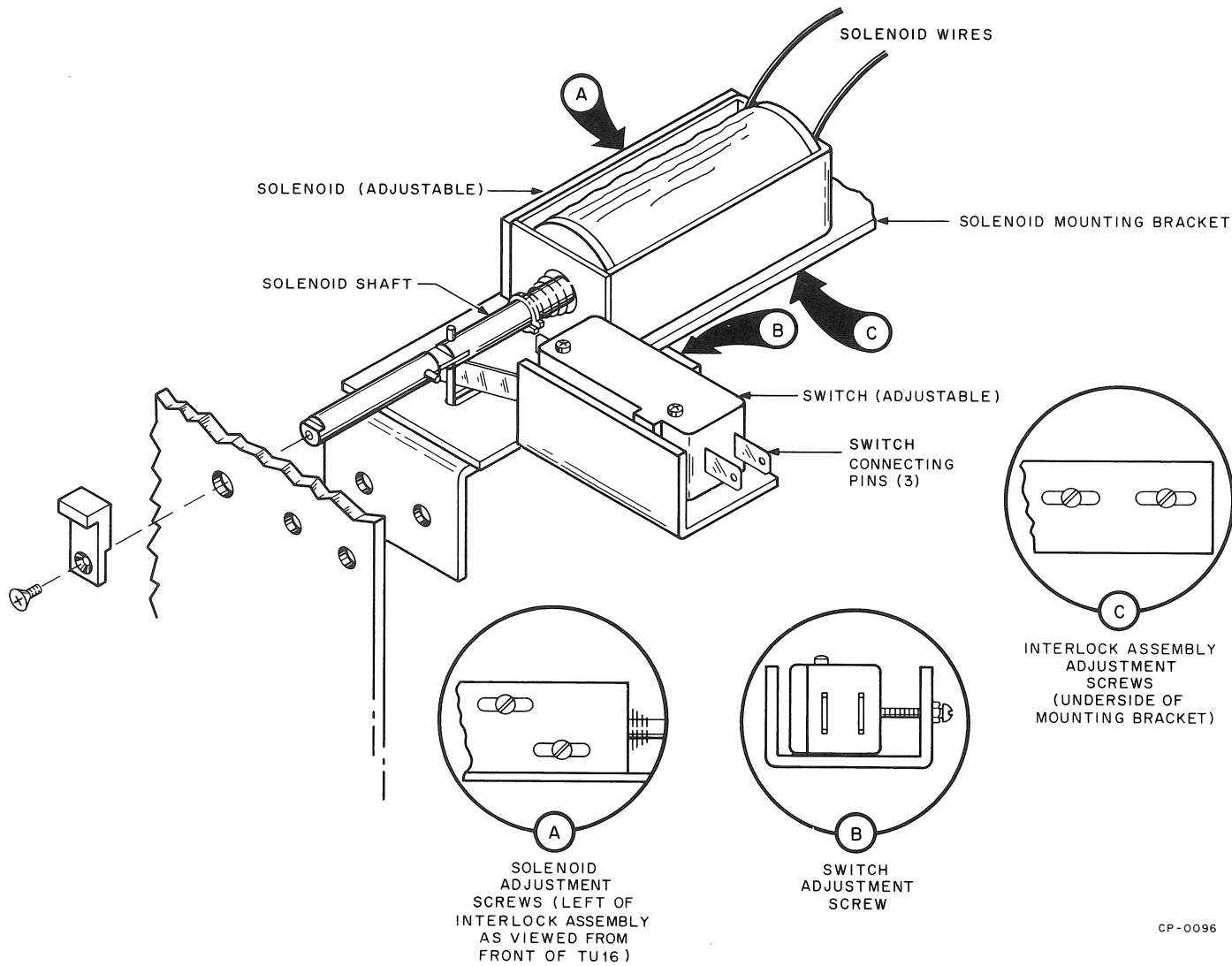
CP-0096

Figure 5-28   Read/Write Interlock Assembly

3.   Place the belt tension gauge on the belt.

4.   Pull the belt tension gauge knob until surface "A" touches the belt (Figure 5-29).
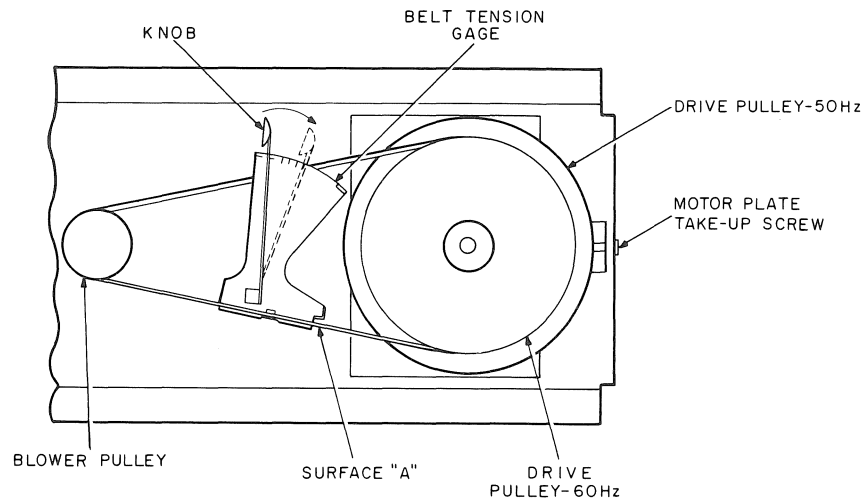
Figure 5-29   Vacuum Motor Belt Adjustment

5.   Tension should read 2.25 to 3.6 kg (5 to 8 lb).

6.   If tension is out of tolerance, loosen the four motor plate mounting nuts and adjust the motor plate take up screw until a 2.25 kg (5 lb) reading is obtained. Tighten the motor plate mounting nuts.

7.   If the belt adjustment was performed after installing a new belt, the new belt must be "run in" for 30 minutes and then readjusted according to steps 3, 4, 5, and 6 above.

5.5.1.10   Read Circuitry Adjustment – The only adjustments directly affecting the proper operation of the TMB11/TU10W read circuitry are the read amplitude adjustment (Paragraph 5.5.1.6), the read skew adjustments (Paragraphs 5.4.2.11 and 5.4.2.12) and the +12 V NRZI threshold adjustment (R26) on the regulator board (Paragraph 5.5.1.1).

5.5.1.11   Write Circuitry Adjustment – The only adjustment directly affecting the proper operation of the TMB11/TU10W write circuitry is the write skew adjustment (Paragraph 5.5.1.7). The adjustment should only be performed after replacing the head plate assembly, or when excessive wear in the head plate assembly is suspected. Note that before adjusting write skew, the read skew adjustment (Paragraphs 5.4.2.11 and 5.4.2.12) must be performed.

5.5.1.12 TMB11 Adjustment Procedure – The TMB11 Controller has two adjustments located on the M7912 Unibus registers module. These are the drive function timer adjustment (Figure 6-13) and the time-out adjustment (Figure 6-16).

1. To adjust the drive function timer, apply power to the TMB11 and scope E41 pin 9 [D9 TIMER (1) H]. Adjust R7 (lower potentiometer) for a 50 μs positive pulse.

2. To adjust the time-out period, perform the following steps:

    a. Load the utility driver program (MAINDEC-11-DZTMG) into memory.

    b. Load address 700_8. Deposit 060400.

    c. Install a 1 plug into the UNIT SELECT socket of an on-line TU10W (master or slave). Unit 0 must be off-line.

    d. Load address 200_8 and start the program.

    e. With probe for trace 1, scope pin C02P1 of the TMB11.

    f. Use an internal negative trigger. Set the horizontal sweep for 5 μs/cm.

    g. Adjust R2 (upper potentiometer) for a 28 μs negative pulse.

5.5.2 Alignment Procedure
A TU10W tape path alignment procedure should be performed when:

1. A capstan, capstan motor, roller guide, or head plate is replaced.

2. Forward and/or reverse skew is found to exceed specifications. (Refer to Paragraphs 5.4.2.11 and 5.4.2.12.)

3. An amplitude difference of more than 10 percent is seen between forward and reverse read amplifier output.

4. A visible change in the tape's path across the capstan is apparent when changing from forward to reverse tape motion.

5. Measurement of reference edge to track 1 of a developed (with Magna-See solution) tape shows a result different from 0.178 ± 0.076 mm (0.007 ± 0.003 inch). Refer to Paragraph 5.4.3.3.

6. After performing a tape speed adjustment (Paragraphs 5.4.2.7 and 5.4.2.8) and mechanical skew adjustment (Paragraphs 5.4.2.11 and 5.4.2.12) under quarterly preventive mainte-nance, and performing capstan ramp adjustment (Paragraphs 5.4.3.1 and 5.4.3.2) and read amplitude adjustment (Paragraph 5.4.3.5) under semiannual preventive maintenance, and running all TU10W diagnostics, you are still encountering incompatibility with other tape transports.

5.5.2.1 Objectives – The objectives of the tape path alignment procedure are listed below:

1. To establish a single plane for tape to travel from supply reel to take-up reel, independent of the capstan and fixed guides (part of the head plate assembly). This is accomplished by aligning reel hubs and roller guides.

2. To mount the head plate in the plane established in Step 1. This is accomplished by establishing the relationship between the reference surfaces used in Step 1 and the surface onto which the head plate is to be mounted. If this relationship is nominal, the head plate is simply mounted. If the relationship is not nominal, appropriate shims are placed under the head plate in order to bring the reference edges of the fixed guides into the proper plane.

3. To minimize the amount of distortion to the tape as it travels through the plane established in Steps 1 and 2. This is accomplished by shimming the capstan motor so that the capstan motor shaft becomes perpendicular to the tape path.

NOTE
The effect of accomplishing the above steps is to minimize static skew, dynamic skew, and tracking errors in both forward and reverse directions. Skew is the total amount of non-perpendicularity of characters written on tape. Tracking is defined by ANSI standards as the measurement from the reference edge to each track center line. Improper tracking takes two forms:

Read – A tape transport that is tracking incorrectly will not have its read head elements centered over tracks correctly written by another tape transport.

Write – A tape transport tracking incorrectly will write tracks of data that are not correctly spaced from the reference edge of the tape. Therefore, a transport with proper tracking alignment would not have its read head elements centered on the incorrectly written tracks.

5.5.2.2 Tools Required for Tape Path Alignment – A list of tools specifically required for aligning the tape path is provided below:

Tool Name	DEC Part No.	Tool Name	DEC Part No.
Skew Tape (800 bits/inch)		Depth Micrometer	29-22039
365.8 m (1200 ft)	29-19224	Shim Stock	
182.9 m (600 ft)	29-22020	0.001	48-50023-01
Reel Hub Tool	29-18611	0.002 (red)	48-50023-03
Roller Guide Tool	29-18607	0.003 (green)	48-50023-04
Microscope	29-20273	0.004 (tan)	48-50023-05
Magna-See	29-16871	0.005 (blue)	48-50023-06
Penlight	29-10780	0.0075 (transparent)	48-50023-07
Alignment Glass	74-13969	0.0010 (brown)	48-50023-08

5.5.2.3 Procedures – Perform the following steps to establish a basic tape path plane:

1. Remove both the supply and take-up reels.

2. Use the reel hub alignment tool to check alignment of both reel hubs. You should feel a small amount of friction when sliding the tool in and out between alignment boss and reel hub. You should not be able to move tool back and forth between hub and alignment boss. Loosen Allen screws and adjust the hub if necessary. Refer to Figure 5-30.

5-40

a.   Front View

REEL HUB ALIGNMENT
GAUGE #29-18611
(Should feel friction
in vertical ( ) axis.
Gauge should not move
in horizontal (←→) axis.)

HUB LOCKING SCREW
ACCESS OPENING

REEL HUB ALLEN
LOCKING SCREWS (2)

TOP
OF
TRANSPORT

MACHINED
ALIGNMENT
BOSS

TEFLON WASHER

3/16 INCH KEY

REEL MOTOR
DRIVE SHAFT

REEL HUB ASSEMBLY

FRONT OF
TRANSPORT
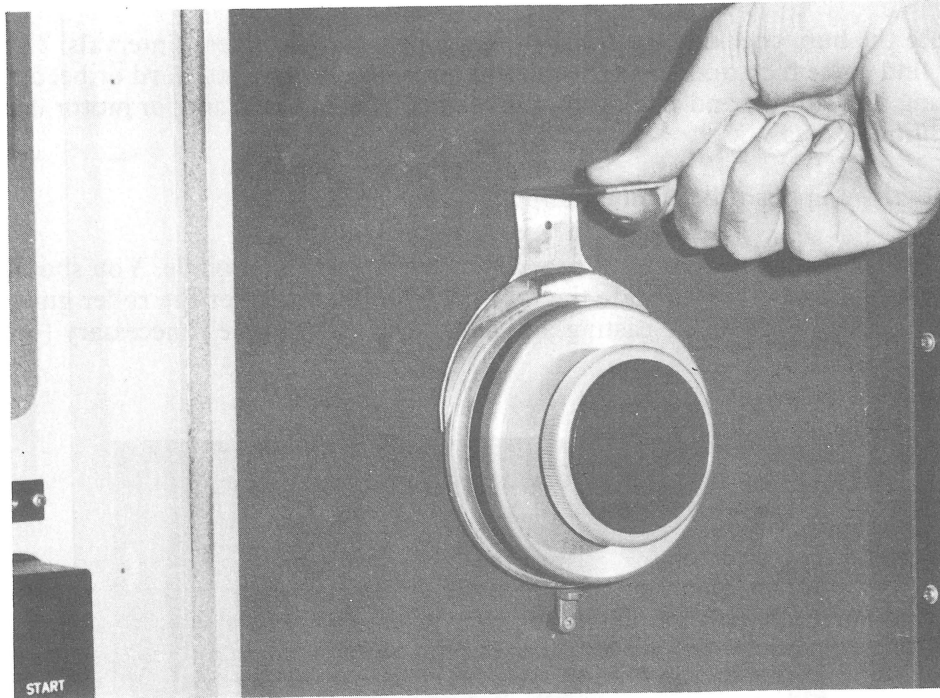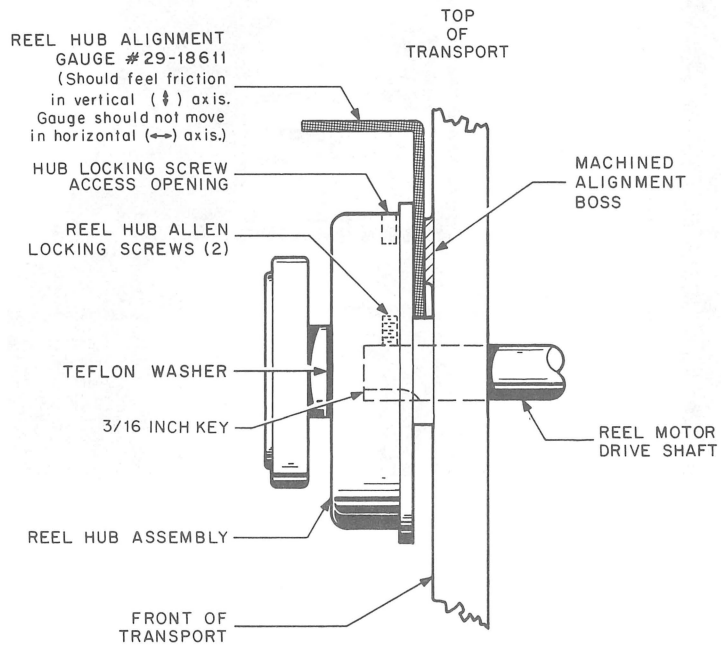
CP-0104

b.   Side View

Figure 5-30   Reel Hub Adjustment

5-41

3. Rotate the hub, checking the fit of the alignment tool at several intervals. There will probably find some high and low spots but the tool should not bind hard or become loose when moving tool toward and away from the casting. Replace hub and/or motor if either of these conditions exists.

4. Remove the upper roller guide ramp (Figure 5-31).

5. Slide the roller guide alignment tool under the upper roller guide. You should feel a small amount of friction as you slide the tool back and forth under the roller guide. Loosen the clamp on back side of the casting and adjust the roller guide if necessary (Figure 5-32).
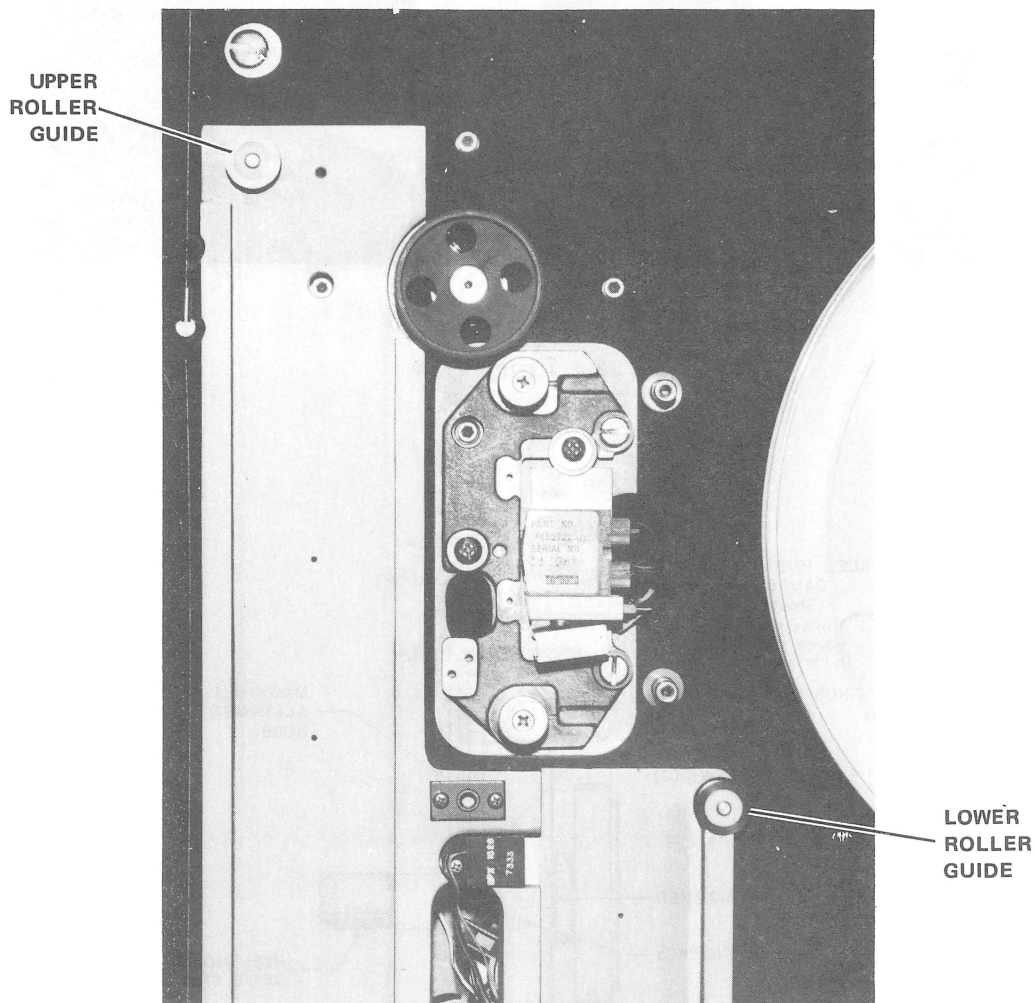
Figure 5-31   Location of Upper and Lower Roller Guides
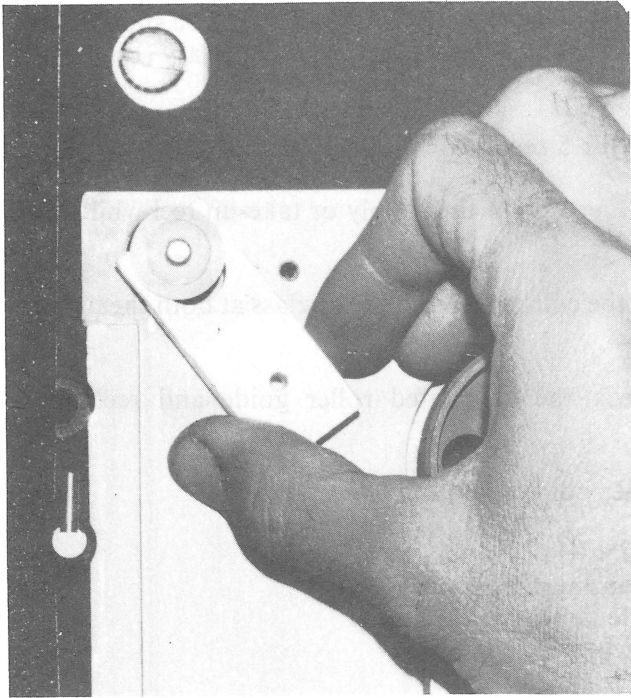
7660-1

a. Upper Roller Guide Adjustment
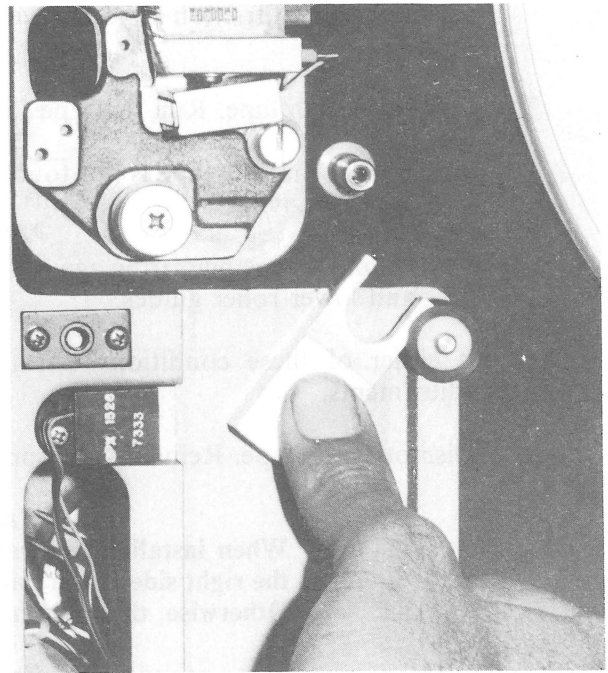
7660-5

b. Lower Roller Guide Adjustment

FRONT OF TRANSPORT

TAPE ROLLER GUIDE ALIGNMENT GAUGE # 29-18607

TAPE GUIDE ROLLER

ROLLER SHAFT LOCK CLAMP

6 X 32 X 1/2" ALLEN CLAMP LOCK SCREW

EXERT PRESSURE AT THIS POINT DURING ALIGNMENT

TAPE GUIDE ROLLER SHAFT

CLAMP MOUNTING SCREW
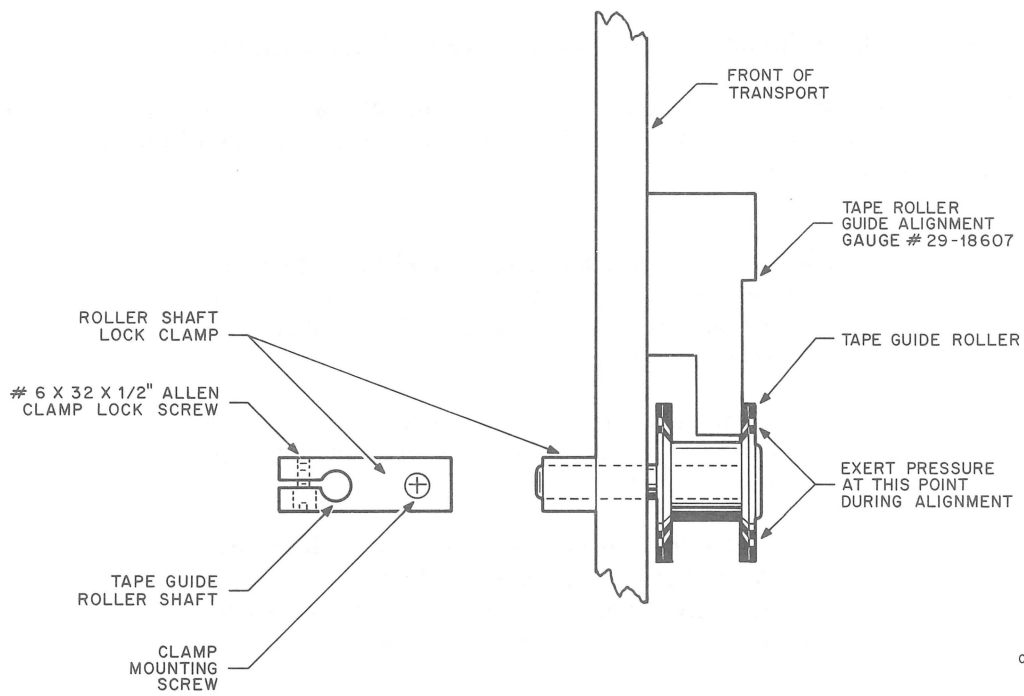
CP-0105

c. Side View of Roller Guide Tool Insertion

Figure 5-32   Roller Guide Adjustments

6. Slide one side of the roller guide alignment tool under the lower roller guide. You should feel slight amount of friction as you move the tool back and forth. Adjust if necessary (Figure 5-32).

7. Load a scratch tape. Run the tape forward for 5 seconds.

    a. Ensure that the tape is not touching either side of the supply or take-up reel while the tape is moving.

    b. Look for tape puckering against either the column floor or door glass at both the upper and lower roller guides.

    If either of these conditions exists, recheck the associated roller guide and reel hub adjustments.

8. Dismount the tape. Reinstall the upper roller guide ramp.

CAUTION
When installing the ramp, you must push down on the right side of the ramp while tightening the screw. Otherwise, the ramp may touch the tape.

Perform the following steps to mount a head plate in the tape path plane:

1. Remove the head plate cover.

2. Disconnect the write, read and erase head cables from the head.

3. Loosen the three shoulder screws and remove the head assembly.

4. Measure the depth from the outer surface of the left vacuum column to the surface onto which the head plate was mounted. Nominal value is 2.84 cm (1.12 inches). Call this value "HMS" (Figure 5-33).

NOTE
You may find this measurement difficult to make because you can only seat one side of the micrometer on the vacuum column surface. It is, therefore, advised that you:

1. **Place the micrometer base at a 45-degree angle with the vacuum column surface (gives greater seating area).**

2. **Make the measurement with the micrometer shaft as close as possible to the vacuum column wall (gives more leverage to keep the micrometer base seated and has distance to project error).**

3. **Repeat the measurement several times to verify results.**

DEPTH MICROMETER

HEAD PLATE MOUNTING SURFACE

LEFT VACUUM COLUMN
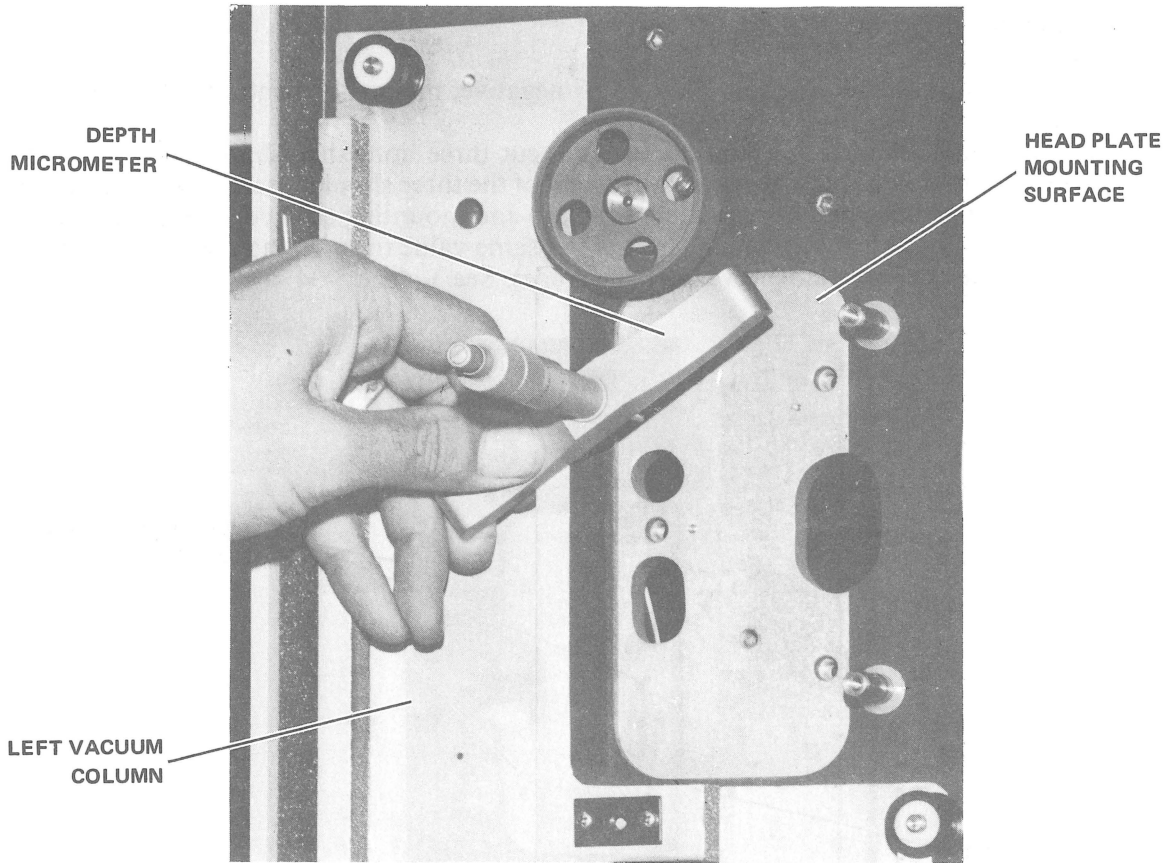
7660-18

a.   Placement of Depth Micrometer

DEPTH MICROMETER

LEFT VACUUM COLUMN

HMS

HEAD PLATE MOUNTING SURFACE
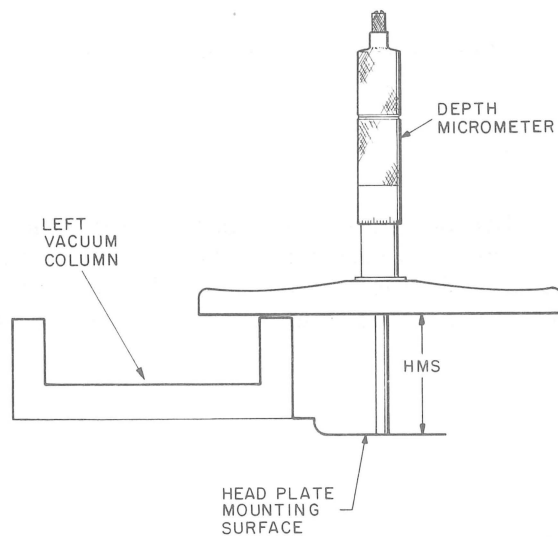
CP-1991

b.   Bottom View of HMS Measurement

Figure 5-33   Measurement of Head Plate Mounting Surface (HMS)

5. Subtract 1.120 from HMS.

6. If the result obtained in Step 5 is zero or negative, mount the head plate* without shims.

    If the result obtained in Step 5 is positive, cut three horseshoe-shaped shims of the value obtained in Step 5 and place one under each of the three shoulder screws when mounting the head plate* (shims go between the head plate and mounting surface). See Paragraph 5.5.2.2 for shim color codes. Also cut a shim of the same value to surround the vacuum port which goes to the tape cleaner (prevents air leakage). See Figure 5-34.

HOLES FOR MOUNTING SCREWS (3)

VACUUM PORT

7660-20
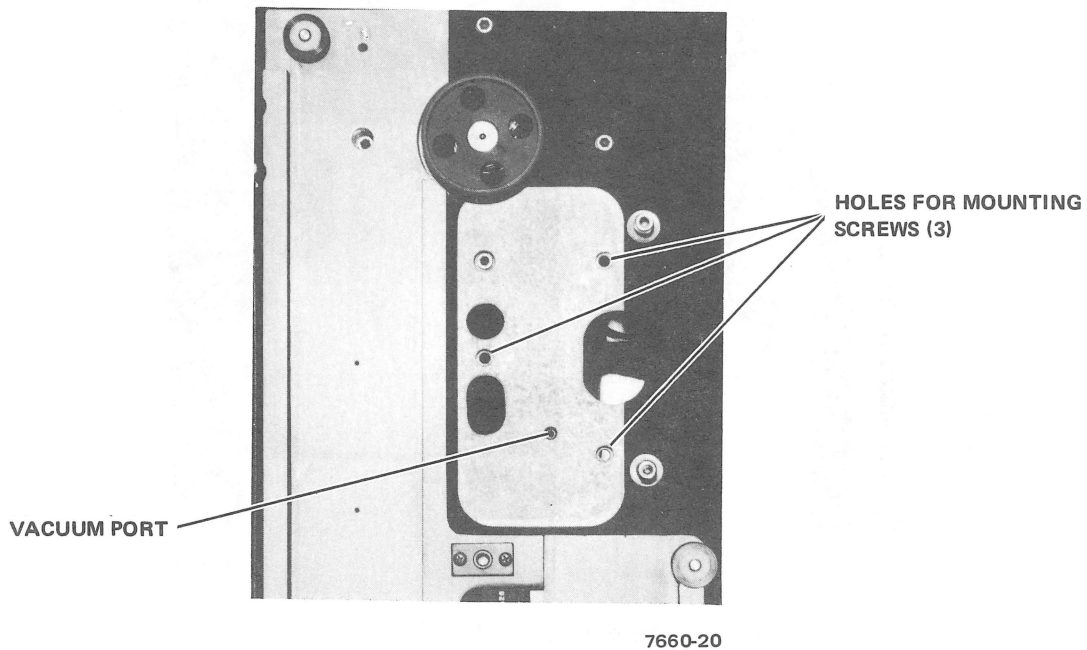
Figure 5-34   Location of Shims under Head Plate Assembly

Thus far, this section has described how to set the reel hubs and roller guides in the same plane as vacuum columns (Figure 5-35) and how to set the reference edge of the fixed guides into the plane of the tape coming out of the vacuum columns. (Figure 5-36). The following paragraph will describe how to set the shaft of the capstan motor perpendicular to the tape path so as to minimize distortion of the plane already established.

---

*If a new head assembly is mounted, electrical wire deskew will have to be performed. This should be done after the read mechanical skew adjustment (quarterly items 11 and 12 in preventive maintenance section).
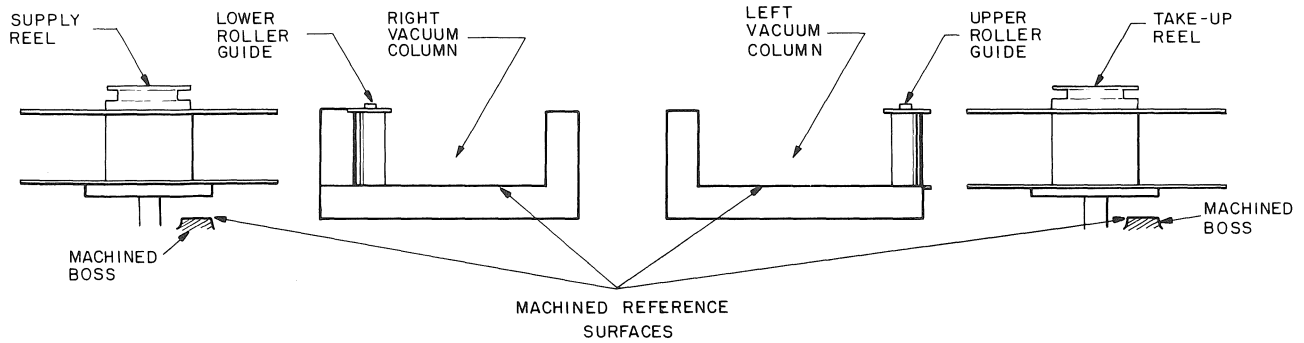
SUPPLY REEL • LOWER ROLLER GUIDE • RIGHT VACUUM COLUMN • LEFT VACUUM COLUMN • UPPER ROLLER GUIDE • TAKE-UP REEL • MACHINED BOSS • MACHINED BOSS • MACHINED REFERENCE SURFACES • CP-1993

Figure 5-35   Machined Reference Surfaces Used to
Establish Tape Path Plane

READ/WRITE HEAD • FIXED GUIDE ON REFERENCE EDGE • 0.500** • 0.498 • 1.118* • HEAD MOUNTING SURFACE • DOTTED LINE INDICATES TAPE PATH • SPRING LOADED GUIDE
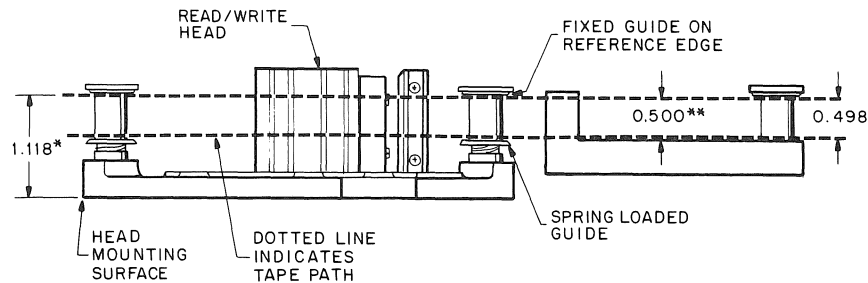
*Dimension from reference edge of fixed guide to mounting surface set up by head plate jigging in factory.

**Nominal vacuum column depth is 0.502; nominal tape width is 0.498; one edge of tape should be 0.002 from floor of vacuum column; other edge should be 0.002 from glass.

CP-1983

Figure 5-36   Head Plate Assembly Mounted in the
Plane of the Tape Path

Steps 1 through 21 ensure that the capstan motor shaft is perpendicular to the tape path. Two conditions can cause non-perpendicularity of the motor shaft to the tape path. One is the capstan motor shaft not being perpendicular to the mounting face of the motor. Figure 5-37a and 5-37c are examples of this condition. [Specifications allow 0.127 mm (0.005 inch) of non-perpendicularity of the motor shaft.] The other condition is non-parallelism between the motor mounting surface on the back of the casting and the front surface of the casting. Figure 5-37b illustrates this situation. [Specifications allow 0.102 mm (0.004 inch) of non-parallelism between the machined surfaces on the front and back of the casting.]

5-47
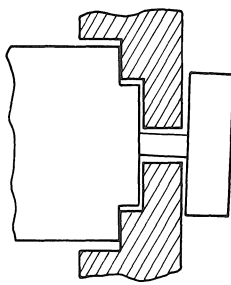
CP-1994

CP-1995

CP-1996

a. Side View –
Capstan Motor Shaft Pointing
Down due to Non-Per-
pendicularity of Shaft
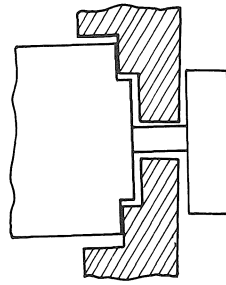
b. Side View–
Capstan Motor Shaft Pointing
Up due to Non-Parallelism of
Machined Motor Mounting
Surfaces
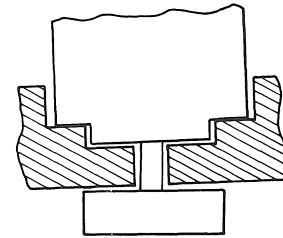
c. Top View –
Capstan Tipped Toward Cas-
ting on Left Side and Away
from Casting on Right Side
due to Non-Perpendicularity
of Motor Shaft

Figure 5-37   Examples of Capstan Non-Perpendicularity

The effect of the capstan motor shaft not being perpendicular to the tape path depends on the direction of the non-perpendicularity, i.e., whether the motor shaft is pointing up, down, toward the left, or toward the right. When the shaft is pointing down (Figure 5-37a), the top of the capstan is away from the casting, causing the tape to track away from the casting. Hard guiding occurs on the vacuum door glass and the fixed guides in both forward and reverse directions. When the shaft is pointing up (Figure 5-37b), the bottom of the capstan is away from the casting, causing the tape to track toward the casting. Hard guiding occurs on the vacuum column floor and the spring-loaded guides in both forward and reverse directions. When the shaft is pointing toward the left (Figure 5-37c), the tape tracks away from the casting in the forward direction and toward the casting in the reverse direction. If the shaft were pointing toward the right, the opposite would be true, i.e., the tape would track toward the casting in the forward direction and away from the casting in the reverse direction.

Figure 5-48 is a flowchart of capstan alignment, summarizing and complementing this alignment procedure. Refer to it while reading this section.

Perform the following steps to align the capstan motor shaft perpendicular to the tape path.

1. Remove the capstan by loosening the capstan locking clamp with an Allen wrench and remove the capstan and clamp.

NOTE
If the capstan is hard to remove, it may be bent and should be replaced. The inside of the capstan should be checked for burrs in the area of the slots. The end of the capstan motor shaft should be checked for burrs also. See Figure 5-38.

5-48

CAPSTAN MOTOR
SHAFT

BURRS TO BE
REMOVED

CP-1987
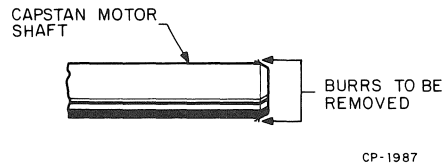
Figure 5-38   Location of Possible Capstan Burrs

2. Remove the capstan motor by unplugging P1 from the H606 power board and removing the four bolts holding the capstan motor on the casting.

CAUTION
Because the bolt heads are in front of the casting and the motor is on the rear, caution should be used so that the motor does not fall when the screws are removed.

Do not attempt to remove the tachometer portion of the motor; the two are replaced as an assembly.

3. Check the capstan motor and casting for the following:

   a. The capstan motor specification template does not interfere with the motor mounting on the casting. If there is interference, remove the template.

   b. The motor does not have any burrs on the mounting surface that would prevent it from mounting squarely on the casting.

   c. Ensure that the mounting surface of both the motor and casting are free of dirt, gummy substances and burrs pushed up by machining operations.

4. Lift up and remove the vacuum column door.

5. Measure the depth from the outer surface of the left vacuum column to the floor of the left vacuum column. [Nominal depth = 1.275 cm (0.502 inch).] Call this value "LVC." See Figure 5-39.

6. Subtract 0.500 from LVC; call the resulting value "X." Record the value "X," as it will be used in Step 16.

NOTE
X is the distance that the inside edge of the tape should be from the floor of the left vacuum column when the outside edge is 0.051 mm (0.002 inch) from the outer surface of the left vacuum column. If the capstan motor shaft is perpendicular to the tape path, the adjustments described earlier in this section were performed correctly; X is equal to this distance.
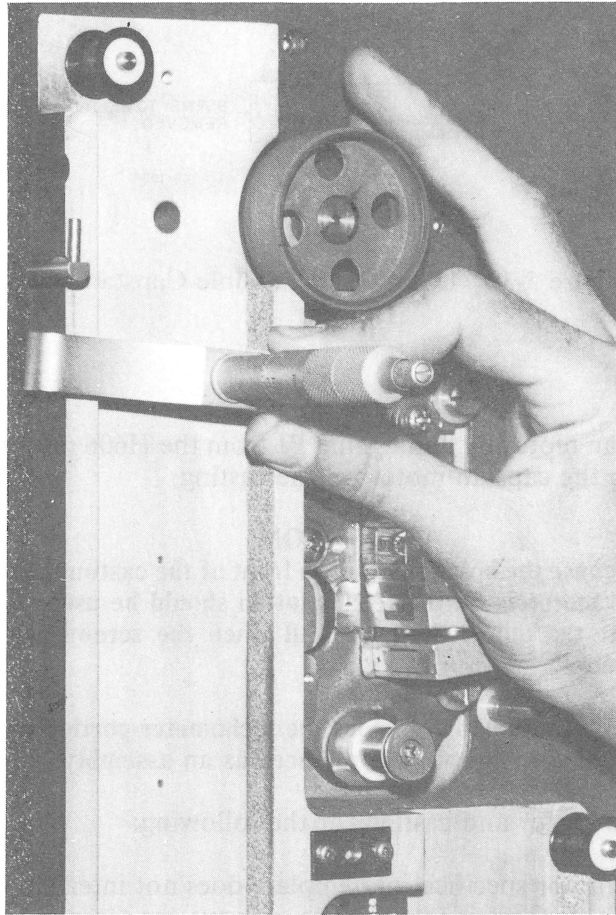
7660-11

a. Placement of Depth Micrometer

DEPTH
MICROMETER

"LVC"
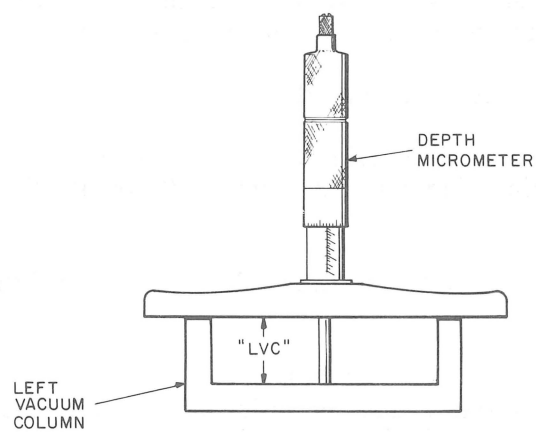
LEFT
VACUUM
COLUMN

CP-1990

b. Top View of LVC Measurement

Figure 5-39   Measuring Depth of Left Vacuum Column (LVC)

7. Remount the capstan motor on the casting (four bolts). Tighten the mounting bolts.

8. Clean the capstan with a water-dampened Kimwipe or lint-free cloth. Do not use any cleaner other than water on the capstan.

9. Reposition the capstan on the capstan motor shaft. Tighten the clamp.

10. Load a good quality tape using the alignment glass (Figure 5-40). It will be necessary to hold the glass doors with one hand while pressing "LOAD" with the other (Figure 5-41).

IF THERE IS MASKING TAPE ON
ALIGNMENT GLASS, REMOVE IT
TAPE IS DETRIMENTAL TO
PROPER ALIGNMENT

←2.7"→   ←2.7"→

14"   14"

MATERIAL IS
0.12" THICK
LEXAN

a. LEFT COLUMN GLASS   b. RIGHT COLUMN GLASS

CP-1989
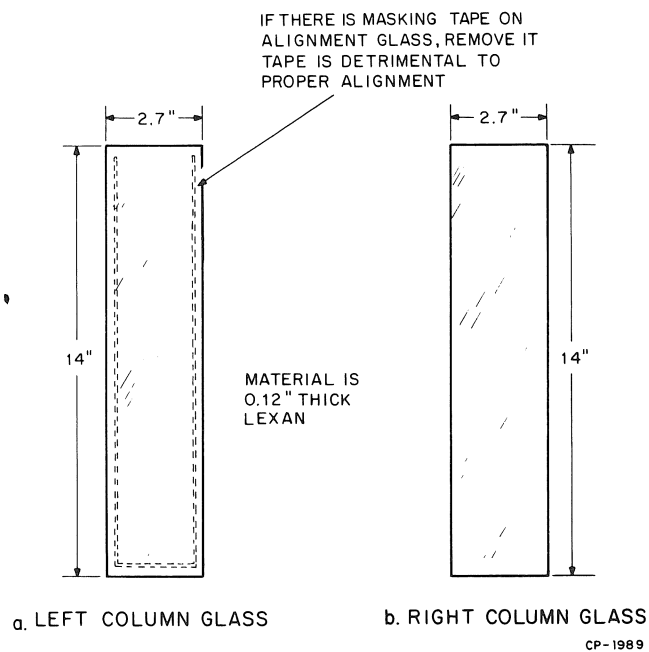
Figure 5-40   Alignment Glass

LEFT COLUMN
GLASS

TAPE

RIGHT COLUMN
GLASS

ON LINE

START

OFF LINE
LOAD

STOP
FWD

REW

BR REL

UNIT
SELECT

REV
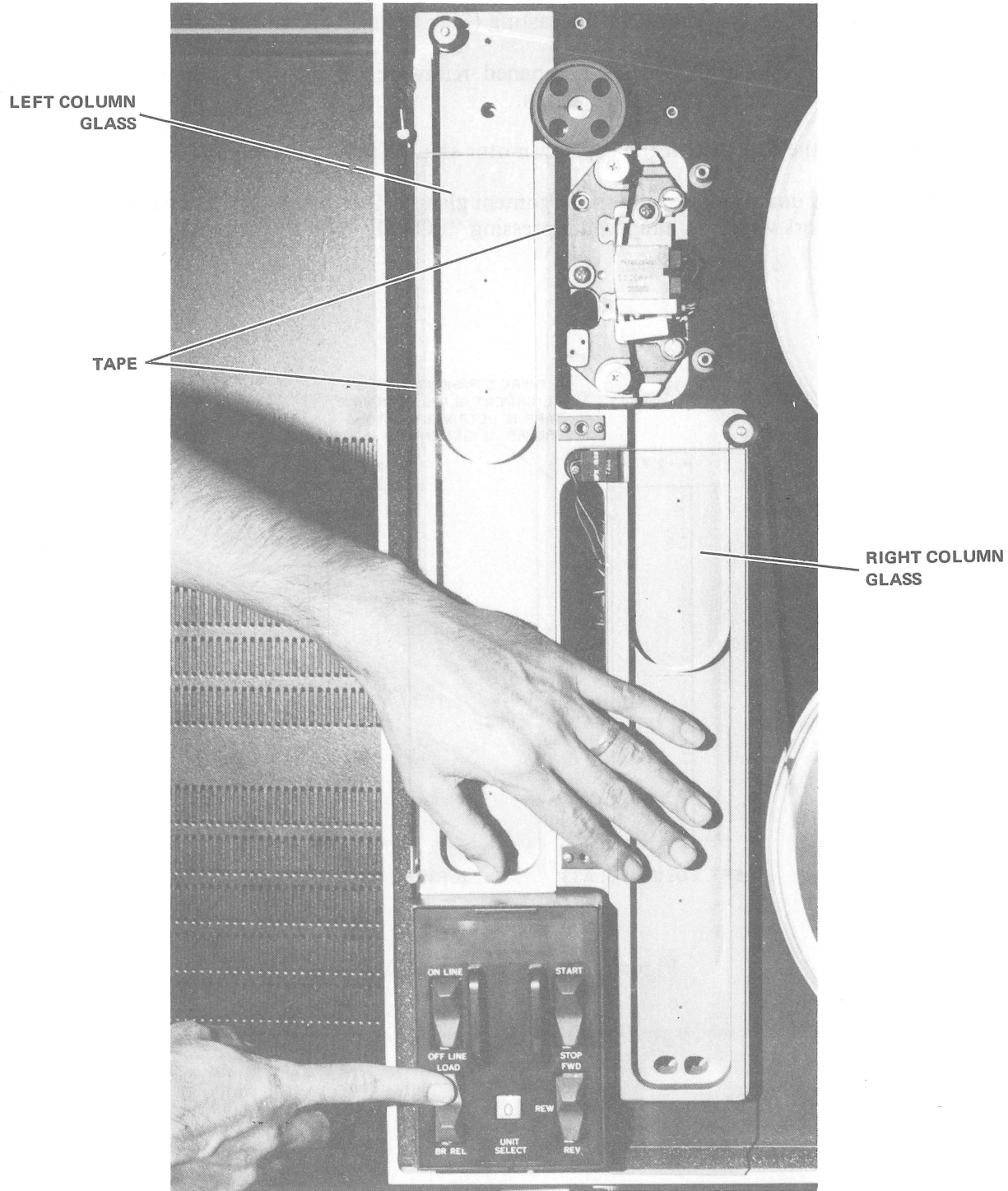
7660-17

Figure 5-41   Using Alignment Glass to Load Tape

11. Ensure that the tape rides in the center of the capstan. This can be done by running the tape forward several feet and "eyeballing" the tape position on the capstan. The capstan can be moved in or out to ensure that the tape is in the middle of the capstan. The capstan alignment tool (29-18609) can be used for coarse adjustment. Ensure that the capstan is clamped securely to the capstan motor shaft.

12. Align the capstan motor shaft (make it perpendicular to tape path) by placing shims between the capstan motor mounting face and the casting surface onto which the capstan motor is mounted. Shims are placed in the vertical axis to correct for capstan steering when both forward and reverse tape motion produces the same steering characteristic, i.e., tape steers toward the deck plate or toward the vacuum column glass in both directions. Shims are placed in the horizontal axis if forward and reverse tape motion show opposite steering characteristics. Figure 5-42 shows shim placements.

NOTE
A few tips will assist in performing the procedure in the shortest possible time:

1. The sequence of tightening the bolts on the capstan motor is important. Each time the bolts are tightened in a particular procedure, they must be tightened in the same order. This allows the procedure to be repeated while keeping the motor in the exact same position.

2. The use of sharp scissors on the plastic shim stock is necessary to keep the edges from curling up. The plastic shim stock sizes are identifiable by the color coding as follows:

Amber	0.0254 mm (0.001 inch)
Red	0.0508 mm (0.002 inch)
Green	0.0762 mm (0.003 inch)
Tan	0.1016 mm (0.004 inch)
Blue	0.1270 mm (0.005 inch)
Transparent	0.1905 mm (0.0075 inch)
Brown	0.254 mm (0.010 inch)

3. The use of a good quality tape is necessary for correct capstan alignment. A used or abused tape does not run true over the capstan, causing false readings during the capstan alignment procedure.

13. Cut one piece of each type of shim stock as indicated in Figure 5-43. Exact dimensions of shim stock are not critical; the main idea is to have a manageable size to use as a feeler gauge. The blunt point shown in Figure 5-43 also minimizes curling of the end that will be used.

SHIM

DECK
PLATE

CAPSTAN
MOTOR

CAPSTAN

a. SIDE VIEW

12   MOUNTING
SCREWS

9   3

6

b. FRONT VIEW
Shim placed in horizontal
axis when forward and
reverse steering are
opposite.

12

9   3

6

c. FRONT VIEW
Shims placed in vertical
axis when forward and
reverse steering are
similar.
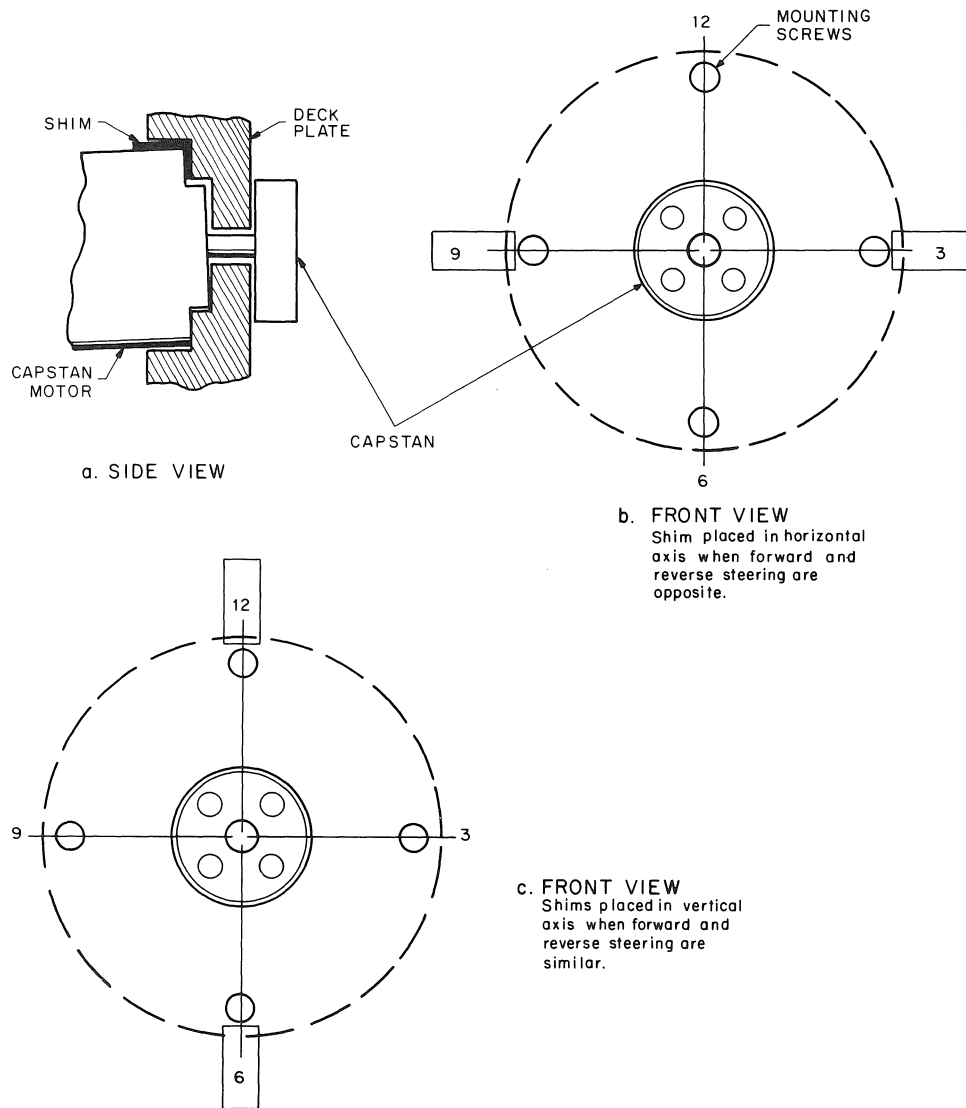
CP-2121

Figure 5-42   Capstan Motor Shim Placement

3/8"   BLUNT
POINT

2"

CP-1988
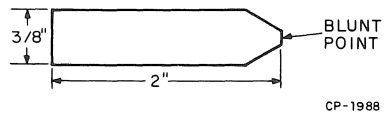
Figure 5-43   Capstan Motor Shim

5-54

14. Run tape forward from BOT for 5 seconds.

15. Using shim stock and a penlight, determine the spacing (Y) between the inside edge of the tape and the floor of the left vacuum column (Figure 5-44). The method of measuring space Y is shown in Figure 5-45 and is described in Steps a, b, and c below.

   a. Slide the shim stock under the inside edge of tape at the slot between the top of the left column and capstan.

   b. Shine the light onto the full width of tape while moving the shim stock back and forth; look for puckering.

   c. Measurement has been obtained when you select a piece of shim stock which causes a small amount of friction when sliding back and forth, yet no visible pucker.

NOTE
Value "Y" (obtained in Step 15) must be equal to the value "X" (obtained in Step 6). The tolerance for the value "Y" is 0.0508 mm (±0.002 inch). In no case shall "Y" be less than 0.0254 mm (0.001 inch). Continue with the procedure to determine corrective action.
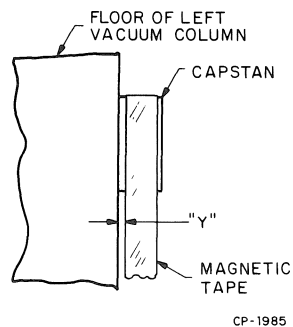
Figure 5-44   Gap (Y) from Tape to Floor of Left Column
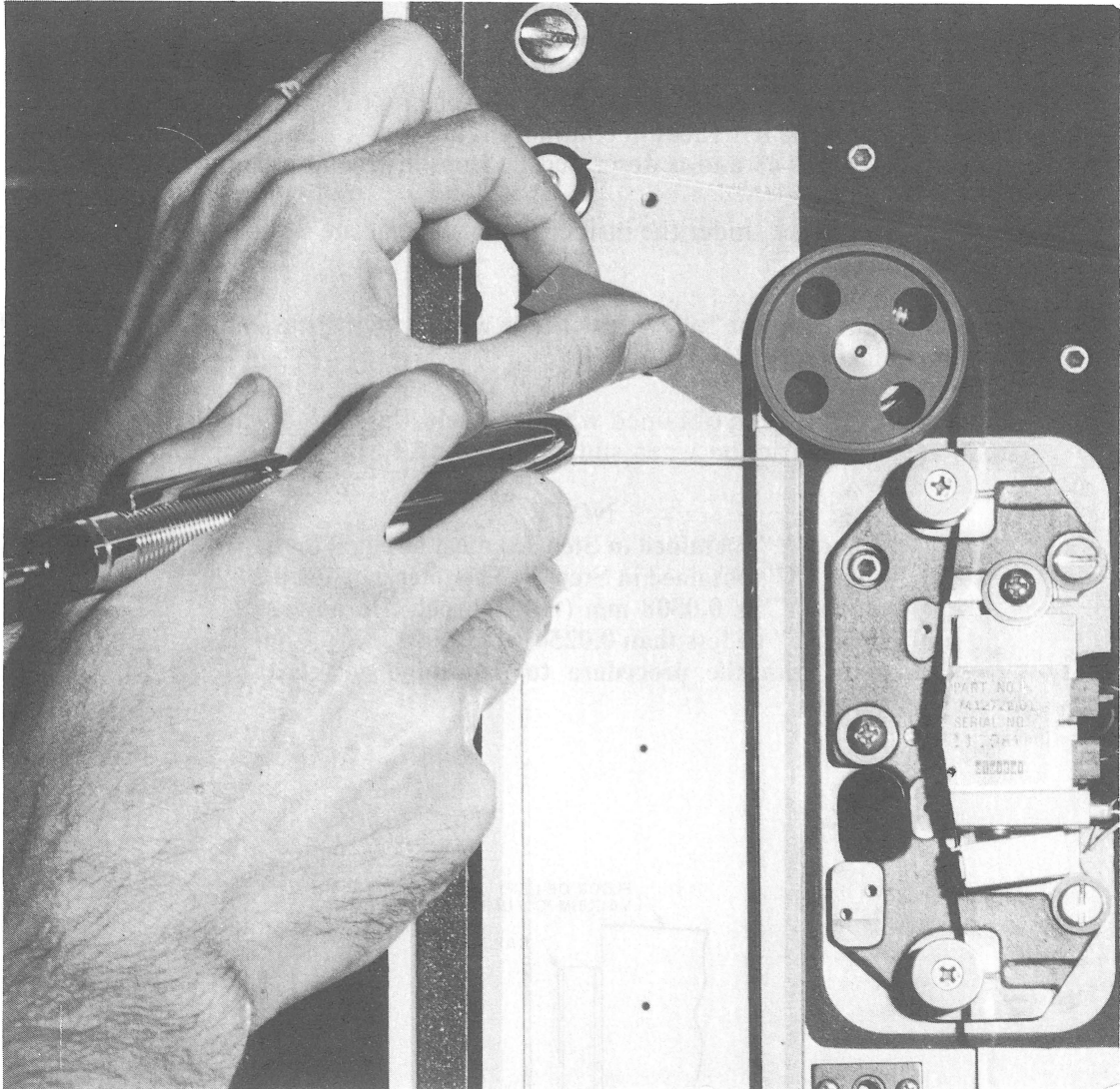
7660-15

Figure 5-45   Measurement of Tape Gap (Y) with Penlight and Shim

16. Run the tape in reverse for 5 seconds. Measure the tape-to-column spacing to obtain value "Y."

The value "Y" obtained in Step 15 must equal the value "Y" obtained in Step 6, ±0.0254 mm (±0.001 inch).

a. Basically, the capstan motor must continually be shimmed, as described in Step 12, until value "Y" is:

- No greater than "X" plus 0.0508 mm (0.002 inch) in forward or reverse.

- No less than "X" minus 0.0508 mm (0.002 inch) in forward or reverse [no less than 0.0254 mm (0.001 inch) in any case.]

•. The difference between forward and reverse does not exceed 0.0254 mm (0.001 inch).

b. Shimming is accomplished as follows:

- If the tape is too close to the casting in forward and reverse, loosen the motor mounting bolts, place a shim under the motor adjacent to the bolt at 6 o'clock, tighten the bolts, and repeat Steps 14, 15, and 16.

- If the tape is too far from the casting in both forward and reverse, loosen the motor mounting bolts, place a shim under the motor adjacent to the bolt at 12 o'clock, tighten the bolts, and repeat Steps 14, 15, and 16.

- If the tape is too close to the casting in forward and too far from the casting in reverse, loosen the motor mounting bolts, place a shim under the motor adjacent to the bolt at 3 o'clock, tighten the bolts, and repeat Steps 14, 15, and 16.

- If the tape is too far from the casting in forward and too close to the casting in reverse, loosen the motor mounting bolts, place a shim under the motor adjacent to the bolt at 9 o'clock, tighten the bolts, and repeat Steps 14, 15, and 16.

- If measurements meet the criteria stated in Step a, go to Step 17.

c. The following guidelines should be adhered to:

- A 0.127 mm (0.005-inch) shim is usually a good starting point, but almost any size shim [up to 0.254 mm (0.010 inch)] may be necessary to accomplish the criteria stated in Step a.

- If a shim size greater than 0.254 mm (0.010-inch) is called for, it is advisable to either rotate the motor mounting 90 degrees and try again or change the motor.

- In no case should there be a shim at the two ends of the same axis, e.g., at 3 and 9 o'clock, or 6 and 12 o'clock. If the formula in Step b. calls for a shim to be placed at 6 o'clock and there is already a shim at 12 o'clock, decrease the shim size at 12 o'clock.

- It is quite normal to have one shim in each of the two axes. In fact, it is desirable, as this will make the procedure less subject to irregularities due to variations in bolt tightening sequences (a shim in the vertical axis will allow the motor to rock in the horizontal axis). For this reason, when you start a shimming session, place a shim of half the value in the horizontal axis if a shim is placed in the vertical axis due to the formula in Step a (or vice versa); this is only a time-saving starting point, and both shims may need adjustment on reruns through Steps 15 and 16.

- It is acceptable to use multiple shims under a given bolt to obtain the desired value, e.g., placing 0.127-mm (0.005-inch) and 0.1016-mm (0.004-inch) shims together to obtain a 0.2286-mm (0.009-inch) shim.

- If Steps 15 and 16 seem impossible to accomplish, or if measurements taken in these steps are inconsistent, see Step 19 for an explanation of capstan and tape phenomena.

- It should be noted that, while a guiding surface exists on the right side of the capstan (the head plate guides), none exists on the left side (left vacuum column). This will tend to make forward capstan steering look less severe than reverse. You will find, therefore, that small differences between forward and reverse are sometimes better corrected by shims in the vertical axis.

17. Mount a skew tape, and adjust mechanical skew per Paragraph 5.4.2.11.

18. With a skew tape mounted, scoping "PACKET" (E4-K1), evaluate capstan alignment as follows:

    a. Run the tape forward looking at the PACKET signal on the scope. PACKET width must be less than 2.5 μs.

    b. While the tape is running forward, move the upper spring-loaded guide away from the tape. PACKET width should not increase more than 2 μs. (Take care not to touch tape.) See Figure 5-46.

CAPSTAN

UPPER
SRING-LOADED
GUIDE

READ/WRITE
HEAD

CP-2131
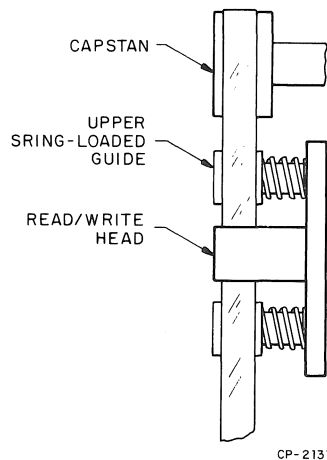
Figure 5-46   Upper Spring-Loaded Guide Location

c. While the tape is running forward, look at the tape interface to the upper fixed guide (use a penlight to reflect light off the tape surface); ensure that no puckering exists.

d. Run the tape in reverse, looking at the PACKET signal on the scope. PACKET width must be less than 2.5 μs.

e. While the tape is running in reverse, move the upper spring-loaded guide away from the tape. PACKET width must not increase more than 2 μs.

f. While the tape is running in reverse, look at the tape interface to the upper fixed guide; ensure that no puckering exists.

The following steps describe corrective action that may be taken when necessary:

a. If the PACKET width increases by more than 2 μs in either forward or reverse when the spring guide is depressed, it should be assumed the tape is running too close to the casting in that direction of tape travel.

b. If the tape is puckering on the guide in either forward or reverse, or if the PACKET width is excessive in forward or reverse, yet does not increase when the upper spring guide is depressed, it should be assumed that the tape is running too far from the casting in that direction of tape motion.

c. If neither a nor b exists, go to Step 19.

d. If a or b exists, make final shimming corrections according to the procedure in Step 16b.

NOTE
After all shimming is completed in this step, it will be necessary to verify that the criteria in Step 16a (tape-to-column spacing) are still met.

19. Run the tape forward. Look in the slot between the inside tape edge and the left vacuum column floor while the tape is moving forward. If room light is not adequate, shine a penlight through from inside the vacuum column (Figure 5-47).

You should see a constant space (width of light) in this slot as the tape moves forward. Periodic width change at a very low frequency (less than one per second) is probably due to tape defects; do not worry about these unless they are very repetitive and cause wide excursions. Higher frequency width changes (5 to 10 times per second) are usually caused by a bent capstan. If this occurs, it will be necessary to replace the capstan and recheck the tape-to-column spacing with shim stock feeler gauges.

20. Run the tape in reverse. Check the slot width to the same criteria as in Step 19.

21. Replace the vacuum column door. Run the skew tape forward and ensure that the PACKET width does not exceed 2 μs. Run the tape in reverse and ensure that the PACKET width does not exceed 2.5 μs. If either criterion fails, suspect roller guide adjustment problem.

22. To return the tape transport to good working condition now that the tape path has been aligned, it may be necessary to perform a number of electrical checks and adjustments (depending on which parts have been replaced in this alignment procedure). Figure 5-48 indicates which checks should be made, and the order in which they should be accomplished.

SHINE
LIGHT
HERE IF
NECESSARY

LOOK
THROUGH
SLOT HERE

CP-1984

a. Front View

CAPSTAN

TAPE

SLOT

RIGHT WALL OF
LEFT VACUUM
COLUMN

CP-1986

b. Right Side View
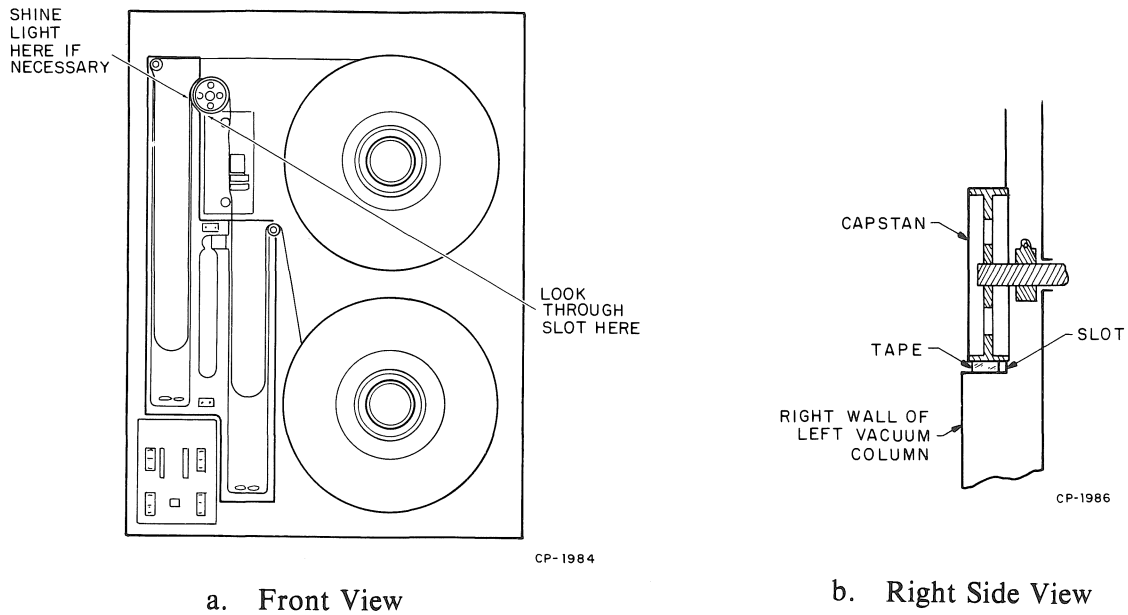
Figure 5-47   Capstan Wobble Check

ENTRY POINTS

CAPSTAN MOTOR
REPLACED

ADJUST DC BALANCE
TAPE SPEED—
QUARTERLY PM
SECTIONS 5.4.2.7
THROUGH 5.4.2.10

ADJUST CAPSTAN
RAMPS SEMIANNUAL
PM SECTIONS 5.4.3.1
AND 5.4.3.2

HEAD PLATE
ASSEMBLY
REPLACED

WRITE SKEW ADJUST.
SECTION 5.5.1.7

NEITHER CAPSTAN
MOTOR NOR HEAD
REPLACED

PERFORM TRACKING
CHECK, ERASE HEAD
CHECK, READ AMP
CHECK, RESIDUAL
AMPLITUDE CHECK,
ON-LINE AND EVALUA-
TION NRZ. SEMIANNUAL
PM SECTIONS 5.4.3.3
THROUGH 5.4.3.7

11-4667

Figure 5-48   Summary, Capstan Alignment Flow Diagram

5.6 CORRECTIVE MAINTENANCE

Corrective maintenance information is provided to guide and assist the field service engineer when he is isolating and repairing faults. The information includes five troubleshooting aids:

1. TMB11/TU10W Diagnostics
2. Corrective Action Flow Diagram
3. Functional Block Diagram
4. TMB11 Troubleshooting
5. TU10W Troubleshooting

5.6.1 TMB11/TU10W Diagnostics

Diagnostics, consisting of a paper tape and documentation, are provided with each system. The documentation includes instructions on loading, running, and interpreting diagnostic printouts. The diagnostics provided with the TMB11/TU10W are listed and described in Table 5-6. Appendix B contains the diagnostic documentation without the program listings.

5.6.2 Corrective Action Flow Diagram

Figure 5-49 provides sequential TMB11/TU10W troubleshooting procedures.

Table 5-6 Diagnostic Descriptions

Number (MAINDEC-11-)	Title	Description
DZTMA-*H	TM,A,B-11/TS03,TU10,N,W Instruction Test	A series of basic tests that checks TMB11 registers for proper operation.
DZTMH-*E	TM,A,B-11 Multidrive Data Reliability Exerciser	Tests all TMB11/TU10W functions for evaluation and debugging.
DZTME-*C	TM,A,B-11/TU10,W,N Drive Function Timer	Selected TMB11/TU10W operations are executed, timed, and the times are then printed.
DZTMF-*D	TM,A,B-11/TU10,N,W Supplemental Instruction Test	Four tests that check special data transfers of the TMB11/TU10W.
DZTMG-*C	TM,A,B-11 Utility Driver	Executes designated operation regardless of errors or results.

*Revision level.
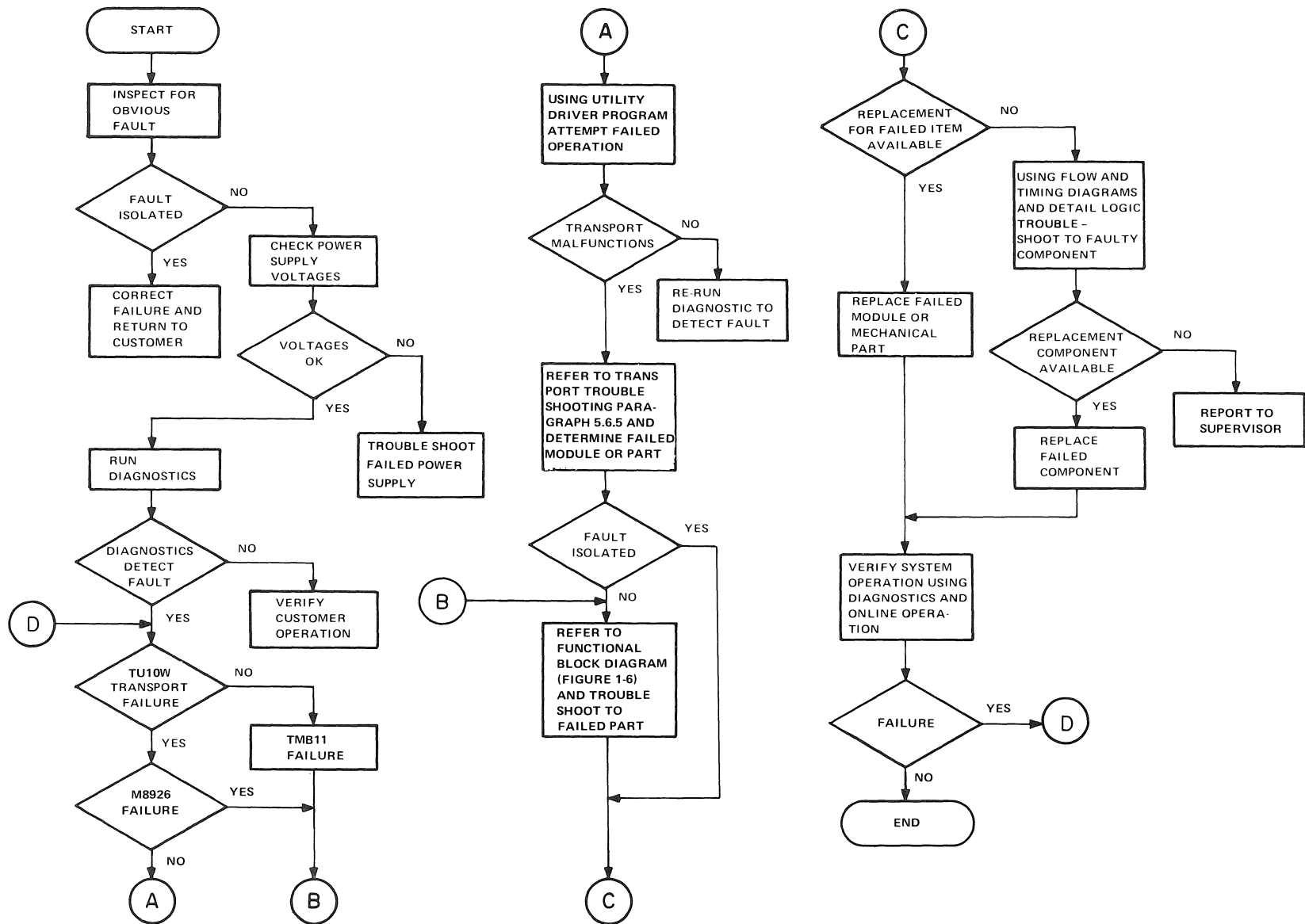
Figure 5-49   TMB11/TU10W Corrective Action Flow Diagram

5-62

11 4671

5.6.3 Functional Block Diagram

Figure 1-6 functionally separates the circuitry comprising the three major units (TMB11, M8926, TU10W) into blocks, depicting signal flow among those blocks within each unit. It also depicts interfacing between each unit and between the TMB11 and the Unibus. The functional block diagram should be used with Figure 5-48 for both troubleshooting and maintenance.

5.6.4 TMB11/TU10W Troubleshooting Procedures

The diagnostics listed in Table 5-6 test all TMB11 functions. Using the diagnostics while relating to the functional block diagram (Figure 1-6) is the major aid to be used by the field service engineer in isolating and repairing equipment faults.

Table 5-7 is a list of possible TU10W related problems and some hints that may prove helpful when troubleshooting.

Table 5-7   TU10W DECmagtape Transport Troubleshooting Hints

Problem	Hints
General	Problems in the TU10W Transport can usually be classified as either mechanical or electrical; often, however, the classification may be confusing because a basically mechanical problem can cause what appears to be an electronic malfunction and vice versa. In any case, the problem should be thoroughly analyzed before any adjustments are made.
	Electronic troubleshooting is greatly facilitated by the modular construction – a new card may be substituted and the effect observed. Most difficult, of course, are subtle problems and those of an intermittent nature.
	Visualizing solution (Magna-See) is useful under certain conditions for troubleshooting. At high densities, the data cannot be satisfactorily resolved, but such problems as a dead track, improper gap length, etc., can be isolated rapidly by its use.
	If a tape has had visualizing solution applied to it, do *not* reuse that portion of the tape, as it will contaminate the head and the remainder of the tape. Cut the visualized portion off, discard it, and apply a new BOT marker.
	To use visualizing solution, shake the can thoroughly, remove the top, and pass the portion to be visualized through the solution. Snap the tape vigorously to remove excess solution and let dry. Iron powder will be left in magnetized areas. This can be picked off using transparent tape and then applied to a sheet of paper for a permanent record.

Table 5-7 TU10W DECmagtape Transport Troubleshooting Hints (Cont)

Problem	Hints
High Error Rate	Usually the more difficult problems involve a higher than permissible error rate for which no obvious reason exists. If operating properly with good tape, the transport should make very few errors in writing and, if rewriting is included in the program, it should make no read errors. Useful clues are: 1. In what mode (read or write) are many errors occurring? 2. At what point in the block does the error occur? 3. What is the nature of the error: vertical parity, CRC, LRC? 4. Are the error patterns related? 5. Do errors occur only on certain sets of commands? The first thing to be done is to inspect the head and other items in the tape path for dirt accumulations. Be sure everything is clean. Check the tape being used and try a new reel if tape is doubtful. Check the interface connections for broken wires or bad contacts.
Compatibility	The TU10W Transport accepts and produces tapes conforming to ANSI standards. Occasionally, compatibility problems can arise: 1. Tapes written by and acceptable to the TU10W Transport are not acceptable to another transport. 2. Foreign tapes cannot be read by the TU10W Transport but its own tapes can be read satisfactorily. Four items may be involved: skew, speed, ramp times, and tape path alignment. These should be checked as described in the adjustment procedures (Paragraph 5.5.1).

5.7 REMOVAL AND REPLACEMENT PROCEDURES

This section outlines the removal and replacement procedures for the TMB11/TU10W DECmagtape System. The major TU10W assemblies referenced throughout this section are shown in Figure 5-1. Table 5-2 lists the tools and equipment required for performing these procedures.

NOTE
The capstan, capstan motor, roller guides, and head plate directly affect the path of the tape as it moves through the tape transport. If any one of these items requires replacement, an entire tape path alignment is necessary. Refer to Paragraph 5.5.2.3 for tape path alignment and for the conditions that require a tape path alignment.

5.7.1 Operator Control Panel

To replace burnt-out bulbs in the operator control panel, proceed as follows:

1. Remove power from the TU10W Tape Transport.

2. Loosen the screw at the bottom-center of the control box and remove the panel.

3. Use a bulb extracting tool (DEC 12-09195-01) to remove and replace defective bulbs.

4. Mount the panel on the control box and tighten the screw.

The procedure for removing the control box is:

1. Remove power from the TU10W Tape Transport.

CAUTION
**This procedure should be done carefully, since the
cable clamp bracket and control box can both fall
and become damaged.**

2. Disconnect the cable that runs from the rear of the control box to the M8910 module.

3. Remove the two cable clamp screws.

4. Loosen and remove the four nuts securing the control box to the casting.

5. Carefully remove the control box to ensure the connecting cable is not damaged.

6. Reverse Steps (in order) 5 through 2 to install the control box.

5.7.2 Door Seal (Front Casting Perimeter)

Proceed as follows to replace the door seal along the casting perimeter (Figure 5-2):

1. Remove power from the TU10W Tape Transport.

2. Remove any tape reels to avoid possible contamination of the tape.

3. Pull the old foam stripping from the front casting.

4. Remove all adhesive residue from the casting with Freon or another suitable solvent.

5. Cut the new foam stripping to the proper length before removing the protective backing.

6. Remove the protective backing from each strip and carefully press each strip into place
    around the casting perimeter.

7. Close the glass door to ensure correct latching and to ensure against binding the stripping.

5.7.3 EOT/BOT Assembly

To remove the EOT/BOT assembly, proceed as follows:

1. Remove power from the TU10W Tape Transport.

2. Open the glass vacuum column door.

3. Use a small screwdriver to loosen the EOT/BOT assembly mounting screw.

4. Disconnect the wires from the back panel.

Red	C02A2
Orange	C02D1
Yellow	C02C1
Brown	C02D2

5. Carefully remove the assembly.

6. Replace the faulty assembly and install by reversing steps 3 through 5.

7. Check for proper alignment by ensuring that the EOT and BOT markers are sensed; adjust the assembly if necessary.

5.7.4 Reel Motor Filter Elements

The procedure for replacing the reel motor filter elements (Figure 5-50) is:

1. Remove power from the TU10W Tape Transport.

2. Release the service locks and pull the transport out (forward) on the cabinet slides.

3. Reach in from the left side (as viewed from the front) of the transport and unscrew the filters from the reel motors (one filter from each motor).

4. Wrap one turn of Teflon tape on the mounting threads of each new filter assembly and screw them into the servo motors.

CAUTION
Hand tighten only! Do not use a wrench.

5.7.5 Reel Hub Compression Ring and Teflon Washer

Proceed as follows to replace the reel hub compression ring and Teflon washer (Figure 5-51):

1. Remove power from the TU10W Tape Transport and remove the tape reel.

2. Carefully snap out the plastic disk (PN 12-09212-00) from the reel hub.

3. Mark the position of the center roll pin (PN 90-06526) in the hub guide.

4. Using a pair of heavy duty diagonal pliers, carefully remove the center roll pin.

5. Grasp the reel hub and unscrew the knob from the hub.

6. Remove (in order) the Teflon washer, pressure plate, and rubber compression ring.

MOTOR AIR FILTER
(DEC part number
12-09956)

REEL MOTOR

TEFLON
TAPE ON
THREADS

H606
POWER
BOARD

TAKEUP REEL

BRAKE
ASSEMBLY

TRANSPORT

TEFLON
TAPE ON
THREADS

FEED REEL

MOTOR AIR FILTER
(DEC part number
12-09956)

10-1300
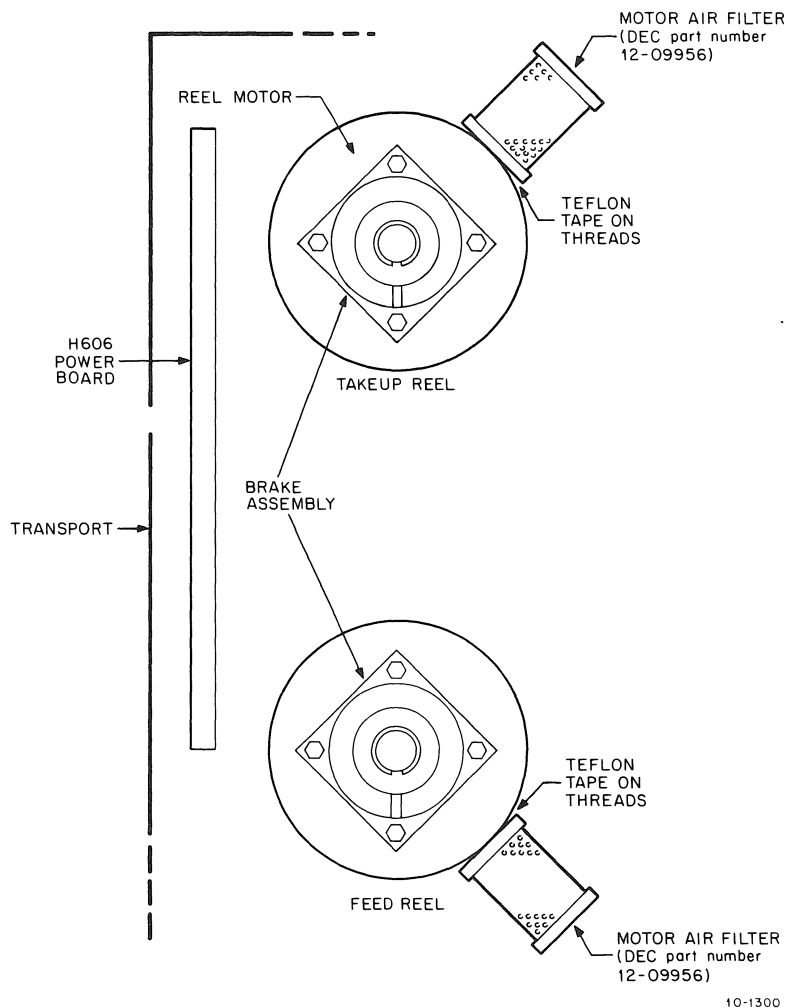
Figure 5-50   Reel Motors, Rear View

PRESSURE PLATE
ROLL PIN
PLASTIC DISK

STOP PINS

KNOB
TEFLON WASHER
COMPRESSION RING

10-1303
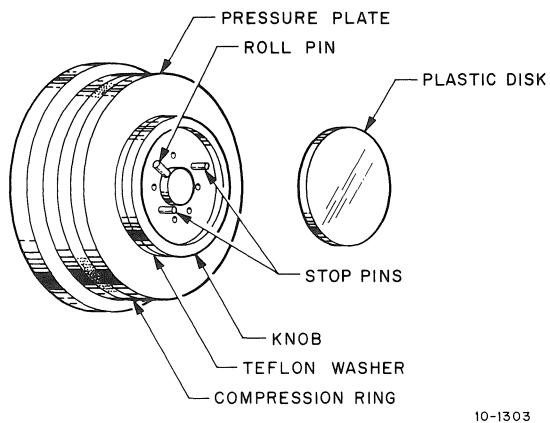
Figure 5-51   Hub Composition

7. Lightly lubricate the flat surfaces of a new compression ring with silicon grease (DEC 90-09299). Wipe all excess grease from the ring with a lint-free cloth.

8. Install (in order) the new compression ring, pressure plate, and a new Teflon washer.

9. Rotate the knob on the hub until the compression ring is compressed and fully seated.

10. Loosen the knob until it is free of the Teflon washer. Then gently screw it in until it just touches the washer.

11. Reinstall the roll pin in the same hole from which it was removed (Step 4).

12. Turn the knob counterclockwise until the roll pin makes contact with one of the two hub stop pins (PN 90-06527).

13. Try to install a tape reel on the hub. If the tape reel does not easily slip on the hub, move the stop pin back one hole at a time until the knob can be released far enough to permit the tape reel to slip on the hub.

14. With a tape reel installed, tighten the knob (clockwise) until the roll pin contacts the other hub stop pin. If the tape reel is not secure, the stop pin must be moved ahead until the knob can be tightened correctly.

5.7.6 Reel Hub Assembly
Proceed as follows to replace the reel hub assembly (Figure 5-52):
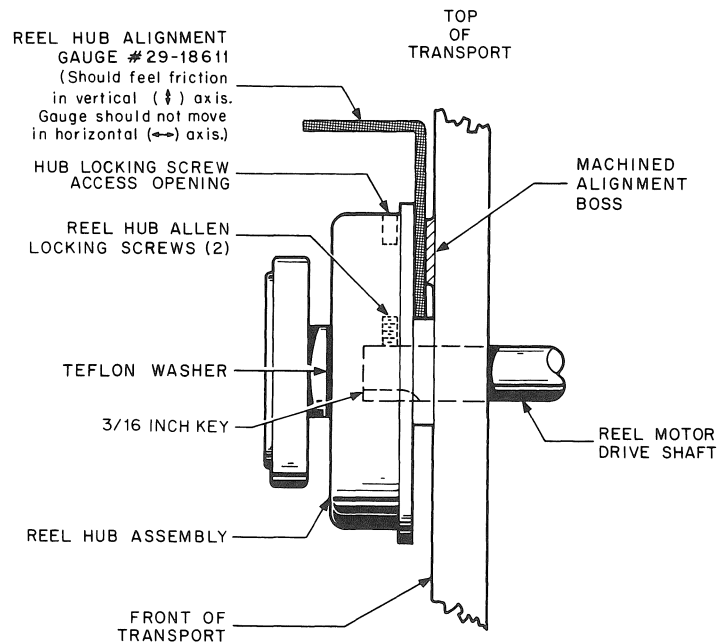
Figure 5-52   Reel Hub

1. Remove power from the TU10W Tape Transport and remove the tape reel.

2. Loosen the two Allen locking screws that secure the reel hub to the reel motor drive shaft. (Access holes for the locking screws are located on the side of the hub.)

3. Remove the reel hub assembly, along with the 0.475 cm (3/16-inch) key (by pulling carefully) and carefully remove any burrs from the motor shaft.

4. Install a new reel hub assembly and the 0.475 cm (3/16-inch) key on the motor shaft and, using the reel hub alignment gauge, set the clearance between the back surface on the hub assembly and the machined boss on the main casting.

5. Tighten the two Allen locking screws.

5.7.7 Reel Motor

Proceed as follows to remove and replace a reel motor (Figure 5-1):

NOTE
The reel motor brushes are not field replaceable.

1. Remove power from the TU10W Tape Transport.

2. Remove the reel hub assembly. Refer to Paragraph 5.7.6.

3. Unplug the P3 connector from the rear of the H606 power board.

4. Remove the pins from the P3 plug and observe that the motor and brake wires are now disconnected from the connector.

5. Remove the four captive screws that secure the motor to the deck casting. Remove the motor.

CAUTION
When removing these four screws, it is necessary to support the motor from the rear. If support is not supplied, the motor will fall when the screws are removed.

6. Remove the air filter(s) from the motor(s).

7. Using the brake assembly removal procedure, remove the brake assembly.

8. Reinstall the brake assembly and air filter on the new reel motor.

9. Replace the reel motor and tighten the four captive screws to a torque value of 1.13 N-m (10 in-lb).

10. Reinstall the reel hub assembly and replace the pins in P3 plug. (Refer to Paragraph 5.7.6.)

5.7.8 Reel Motor Brakes

If the stator slot is worn away, proceed as follows to remove and replace the reel motor brakes:

1. Remove power from the TU10W Tape Transport.

2. Unplug the brake (P3) connector from the rear of the H606 power board.

3. Remove the pins (from P3) holding the wires for the particular brake being removed. Observe that the wires for that particular brake are now disconnected from their respective P3 pin locations.

4. Loosen the hub clamp with an Allen wrench and withdraw the clamp, spacer, rotor, rotor disk, and spring (Figure 5-53).

5. Remove the four 10-32 screws securing the stator to the reel motor.

6. Replace the reel motor and secure the stator to the motor assembly using four 10-32 screws. Ensure that the stator slot is at the 6 o'clock position.

7. Slide the rotor disk, rotor, spacer, and clamp onto the motor shaft. Insert a 0.254-mm (0.010-inch) feeler gauge between the stator and rotor disk face and rotate the disk face 360 degrees to obtain the required clearance at all points between the stator and rotor disk face.

8. Tighten the hub clamp.

9. Replace the spring as shown in Figure 5-53

10. Reinsert the brake wires into the brake connector (P3). Insert the connector back in its correct location on the H606 power board.

NOTE
The armature is driven by three pins on the hub. It is important that the armature does not bind on the pins.

5.7.9 Vacuum Switches and Rubber Sleeves

Proceed as follows to replace the vacuum switches and/or rubber sleeves on the switches (Figure 5-54):

1. Remove power from the TU10W Tape Transport.

2. Release the service locks and pull the transport out on the cabinet slides.

3. Carefully detach the pair of Faston connectors from each switch and note their respective positions for reassembly purposes.

4. Remove the switch from the bracket by removing the two 2-56 screws and nuts.

5. Replace the rubber sleeve on each switch with a 2.22-cm (7/8-inch) length of tubing. Replace the switch when necessary.

STATOR MUST
BE MOUNTED
WITH SLOT IN
DOWNWARD
POSITION

REAR VIEW

REEL MOTOR
BRUSH RETAINER

.010"
CLEARANCE

SPRING

GAP SUCH THAT CLAMP
IS OVER SLOTTED
SECTION OF ROTOR
SLEEVE.

REEL MOTOR

MOTOR SHAFT

CLAMP

3/16" SPACER

ROTOR

ROTOR DISC

STATOR SLOT

STATOR

REEL MOTOR
BRUSH RETAINER

MOTOR DRIVE
WIRES
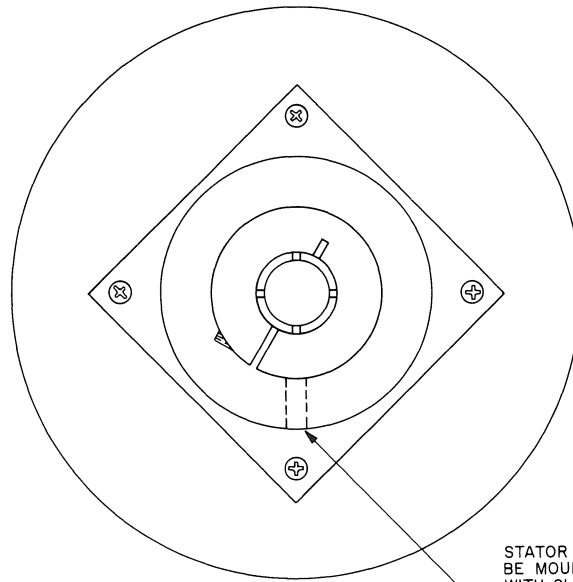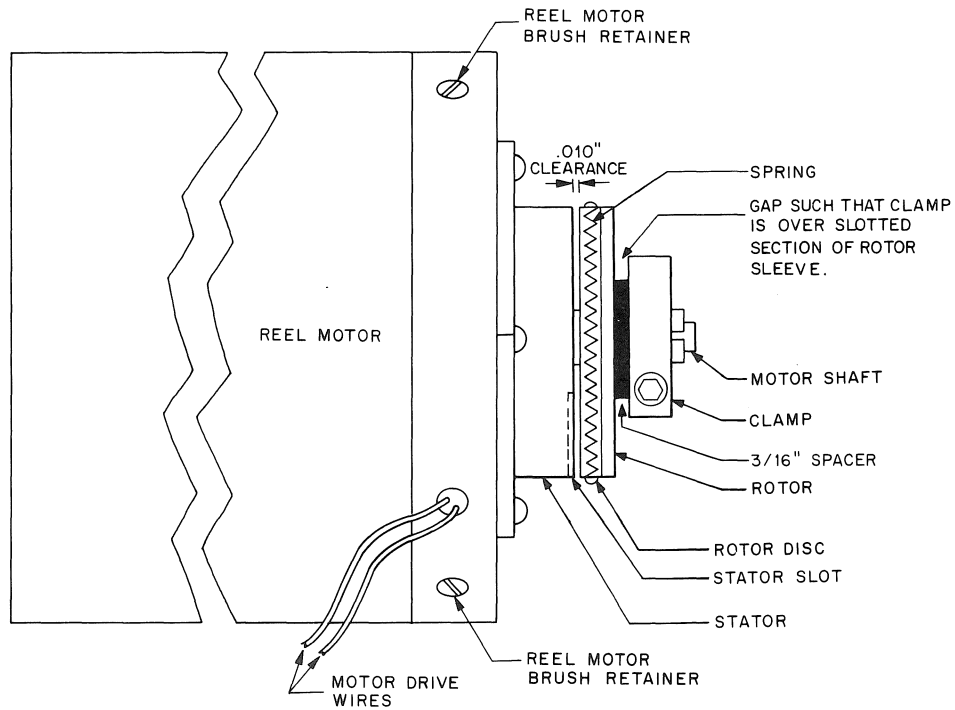
SIDE VIEW

11-4801

Figure 5-53   Reel Motor Brush Locations and Brake Assembly

5-71

MOUNTING SCREW & NUT
(2 PER SWITCH)

LOW OUTLET

RUBBER SLEEVE
(HOSE)

TRANSPORT
MOUNTING
BRACKET

LOW OUTLET
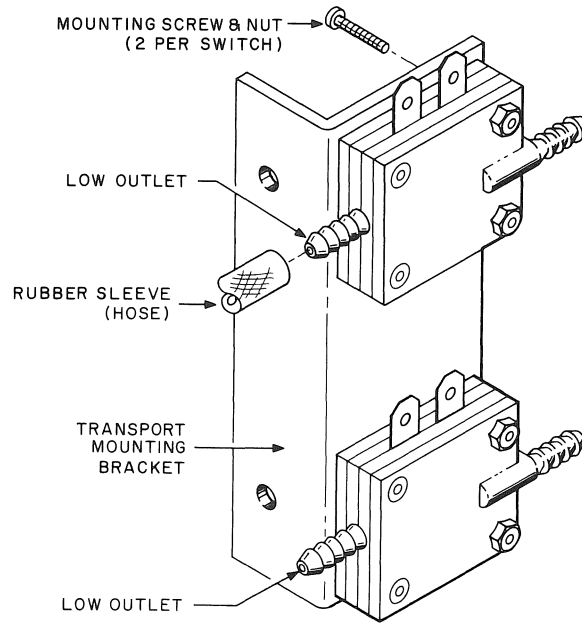
CP-0103

Figure 5-54   Vacuum Switches

6. Mount the switch to the bracket with two 2-56 screws and nuts.

CAUTION
**Guide the switch assemblies so each switch sleeve fits
snugly into its respective hole in the casting without
any lateral strain. Never overtighten the screws
securing the vacuum switches to the bracket. Dam-
age to the switch may result.**

7. Reconnect the Faston connectors to all switches.

8. Operate the transport off-line to verify switch functions.

5.7.10   Vacuum Motor Assembly
Proceed as follows to remove and/or replace the vacuum motor assembly (70-09638-01, 2):

1. Remove power from the TU10W by turning the circuit breaker on the 861 power control
    off.

2. Slide the transport forward on its slides to facilitate access.

3. Unplug power connector P9 from J9 at the vacuum assembly from the rear of the cabinet.

4. Loosen the hose clamp at the vacuum pump and slide the hose off the shroud.

5. Disconnect the ground wire from the rear of the drive motor.

6. While supporting the vacuum assembly from underneath, remove the four screws holding it to the cabinet. Remove the assembly.

7. To replace the assembly, reverse steps 3 through 6.

5.7.11 TU10W Power Supply Regulator Board

To remove and/or replace the TU10W power supply regulator board (Figure 5-1), proceed as follows:

1. Ensure that power to the TU10W is turned off; then unplug the TU10W from its outlet.

2. Approach the TU10W power supply from the rear of the TU10W cabinet.

3. Remove all connectors (J1–J5) from the TU10W power supply board.

4. Remove the regulator board cover.

5. Unplug the three power connections (AC HI, AC LO, and GND) from the bottom left corner of the regulator board.

6. Remove the five Phillips head mounting screws and the single Allen mounting screw (Figure 5-7).

7. Carefully lift the regulator board out of the cabinet.

8. To reinstall the regulator board, perform Steps 1–7 in reverse.

> CAUTION
>
> **When replacing a TU10W power supply regulator board, apply a thin coat of Wakefield No. 128 compound or Dow silicon grease to the diode pack heat sink, and ensure that the Allen screw is secured very tightly. This provides adequate heat flow, and prevents the diode packs from overheating.**

Next to the AC HI, AC LO, and GND connector tabs in the lower left corner of power supply regulator board are three additional tab connectors and two wires. Two of the tabs are marked "115"; the other (central) tab is marked "230". If you are operating from a 115 V source, the two wires are connected to the two outside tabs (marked 115); for 230 V operation, the wires are connected to the two tabs on the central connector (marked 230).

5.7.12 TU10W Transformer-Capacitor Assembly (7009636)

The procedure for removing and/or replacing the TU10W transformer-capacitor assembly (Figure 5-1) is:

1. Ensure that power to the TU10W is turned off; then unplug the TU10W from its outlet.

2. If possible, approach the TU10W transformer-capacitor assembly from the rear of the TU10W cabinet. If this is not possible, pull the transport forward on its slides and work from either side.

3. Remove connectors J2 and J3 from the TU10W power supply board.

4. Remove the regulator board cover.

5. Remove the transformer-capacitor assembly cover.

6. Unplug the three power connections (AC HI, AC LO, and GND) from the bottom left corner of the regulator board.

7. Remove the four Phillips head mounting screws that hold the transformer-capacitor assembly.

NOTE
Do not remove the two Phillips head screws that hold
the transformer-capacitor assembly bracket.

8. Remove the Phillips head screw holding the ground strap in place.

9. Carefully lift the transformer-capacitor assembly out of the cabinet.

10. To reinstall the transformer-capacitor assembly, reverse Steps 1 through 8.

CHAPTER 6
TMB11 THEORY OF OPERATION

6.1 INTRODUCTION

The TMB11 Controller has three main functions: handling data transfers, issuing control commands, and monitoring operation of the system.

During data transfer functions, the controller assembles the data word from the magnetic tape and places it on the bus (read operation) or assembles it from the bus and loads it into the tape transport read/write heads (write operation) for recording on magnetic tape. The commands necessary to perform the specified operation are generated by the controller under program control.

Normal data word transfers are performed by direct memory access transactions at the NPR level. If the controller is ready to begin a new function or if an error condition exists, it issues an interrupt request so that it can be serviced by the program.

In addition to the commands required for data transfers, the controller may issue other commands governing tape unit selection, direction of tape travel, rewind, space forward, space reverse, write end-of-file mark, etc. The controller also monitors various functions and provides an indication of error conditions. The status of the monitored functions is stored in the status register.

6.2 GENERAL OPERATION

The prime function of the TMB11 Controller is to control transfers of information so that digital data can either be taken from the bus and recorded on magnetic tape (write operation) or read from the magnetic tape and transferred to the bus for use by another device such as memory (read operation). In addition, the controller performs tape transport selection, tape positioning, tape formatting, and system monitoring functions.

The controller contains a command register, which allows the program to specify desired operations by loading control data (transport selection, packing density, function, etc.) into the register. System status information (end-of-tape, errors, tape unit ready, etc.) is loaded into a status register, which can be read from the bus.

Data transfers are controlled by a byte record counter (MTBRC) and a current memory address register (MTCMA). The program loads the byte record counter with the 2's complement of the desired number of data transfers. The counter is incremented before each transfer; therefore, the byte transfer that causes the byte count overflow (MTBRC becomes zero) is the last transfer to take place. The byte counter is also used to count the number of records during space forward and space reverse operations.

The current memory address register is also incremented before each transfer and, therefore, always points to the next higher address than the one most recently accessed. Thus, when the entire record is transferred, the register contains the address plus 1 of the last character in the record. For certain error conditions, the register contains the address of the location in which the failure occurred.

6.2.1 Read

During read operations, the controller assembles bytes from successive characters read from the tape channels. When reading a 7-channel tape, the 6 data bits are assembled in a data buffer register for temporary storage. The parity bit is read but not loaded into memory. Because the PDP-11 uses 8-bit bytes, the remaining 2 bits in the buffer are forced to 0. When the byte is assembled, it is placed on the bus for transfer to memory. If an NPR transfer is used, bytes from the data buffer are alternately stored into the low and high byte portions of memory.

When reading 9-channel tape, operation is identical except that 8 data bits are assembled. It is not necessary to force any bits to 0, because the 8 data bits constitute a complete PDP-11 byte. In the case of both 7-channel and 9-channel tapes, the parity bit can be loaded into the data buffer but is not loaded into memory.

When reading 9-channel tapes, either the CRC character or the LRC character at the end of a record is stored in the data buffer, depending on the state of bit 14 in the MTRD. If this bit is 0, the CRC character is loaded into the data buffer and can be used for error detection. If the bit is 1, then the data buffer contains the LRC character at the end of the record. When reading a 7-channel tape, bit 14 in the MTRD operates in a similar manner. If bit 14 is set, the LRC character is present, and when bit 14 is cleared, the last data character is present in the data buffer.

6.2.2 Write

During write operations, the controller disassembles 8-bit bytes from the bus and distributes the bits so that they can be recorded on successive frames of the tape. The controller selects one of three recording densities (200, 556, or 800 bpi) for 7-channel tapes. All 9-channel tapes are written at a density of 800 bpi. There are three possible write functions: write, write-with-extended-IRG, and write end-of-file (EOF) mark.

When a write function is selected, the program loads the byte record counter with the 2's complement of the number of bytes to be written in the record. Although the parity bit is generated by the master tape transport, the polarity of the bit is determined by the controller so that either odd or even parity can be selected. When the buffer is loaded, the controller transmits the byte to the master tape transport, which places the byte on the read/write heads of the selected slave transport so that data can be written on the magnetic tape.

The write-with-extended-IRG function is identical to the write function except that a 3-in. gap, rather than the normal gap is used between records. When this function is selected, a 3-in. segment of tape is erased before writing begins.

The write end-of-file (EOF) function is used to indicate that a block of records is complete. When this function is selected, a special EOF character is written on the tape followed by an LRC character. In 7-channel mode the EOF and LRC characters are octal 17. In 9-channel mode the EOF character (and the LRC character) are octal 23. These two characters constitute a complete record. This command causes a 3-in. gap to be placed before the EOF mark. The XIRG command must be absent to have this gap written.

6.2.3 System Monitoring

System monitoring functions are performed by the controller status register. The 16 bits in this register retain error and tape status information. Some status data is combined, such as lateral and longitudinal parity errors, or has a combined meaning, such as illegal command, for optimum use of the available bits. The status register only monitors the tape transport selected by the command register; therefore, other units that may be rewinding do not interrupt the system when ready for data.

6.2.4 Interrupts

The TMB11 Controller uses NPR or BR interrupts to gain control of the bus in order to perform data transfers or to cause a vectored interrupt, thereby causing a branch to a handling routine. The NPR requests are used for direct memory access whenever it is desired to transfer data between memory and the data buffer register without processor intervention. The BR requests are made when processor servicing is required for completed operations or error conditions.

6.2.4.1 NPR Requests – The controller issues an NPR request whenever it is necessary to transfer data between memory and the data buffer register. During a read operation, the direction of transfer is from the data buffer to the core memory. The RDS pulse (read strobe, from master tape transport to controller), which is used to strobe data from the tape transport into the data buffer register, generates the NPR request. When the request is granted, the controller performs a DATOB bus cycle and transfers information from the data buffer into memory.

During a write (or write-with-extended-IRG) operation, the NPR request is generated by the write strobe (WRS) pulse from the transport. When the request is granted, the controller performs a DATI bus cycle and transfers a byte from core memory into the data buffer register.

During both read and write operations, the address in memory that data is read from or loaded into is determined by the value in the current memory address register (MTCMA).

6.2.4.2 BR Requests – A BR interrupt can occur only if the interrupt enable (INT ENB) bit in the command register is set. With INT ENB set, setting the CU RDY bit in the command register, or completing a rewind operation initiates an interrupt request.

When CU RDY is set, it indicates that the controller is ready to perform another command.

When ERR is set, it indicates that some type of error condition exists. In this case, an interrupt is used to cause the program to branch to an error handling routine.

If a function command is issued with the GO bit cleared and INT ENB set, an interrupt is initiated.

If the selected tape unit (as indicated by the SEL bits in the command register) completes the rewind operation before a new command to that unit is received and INT ENB is set, an interrupt is initiated.

If the interrupt is enabled (INT ENB set) and selection of the tape unit is not changed (as indicated by the SEL bits), then a rewind command causes two interrupts: an interrupt when the rewind function begins and an interrupt when the tape unit completes the rewind function. If, however, the tape unit is already at the BOT marker when rewind is issued, only one interrupt occurs.

6.3 FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

The TMB11 flow diagram (Figure 6-1) provides a brief functional description of the controller. This diagram should be read in its entirety while referencing the controller functional block diagram, Figure 6-2.

6.4 TMB11 REGISTERS

All software control of the magtape system is performed by means of six device registers within the controller. These registers have been assigned bus addresses and can be read or loaded using any PDP-11 instruction that refers to their address. The six device registers are listed in Table 6-1. The register addresses are determined by jumpers on the M105 address selector module. Any programs that refer to these addresses must be modified accordingly if the jumpers are changed.
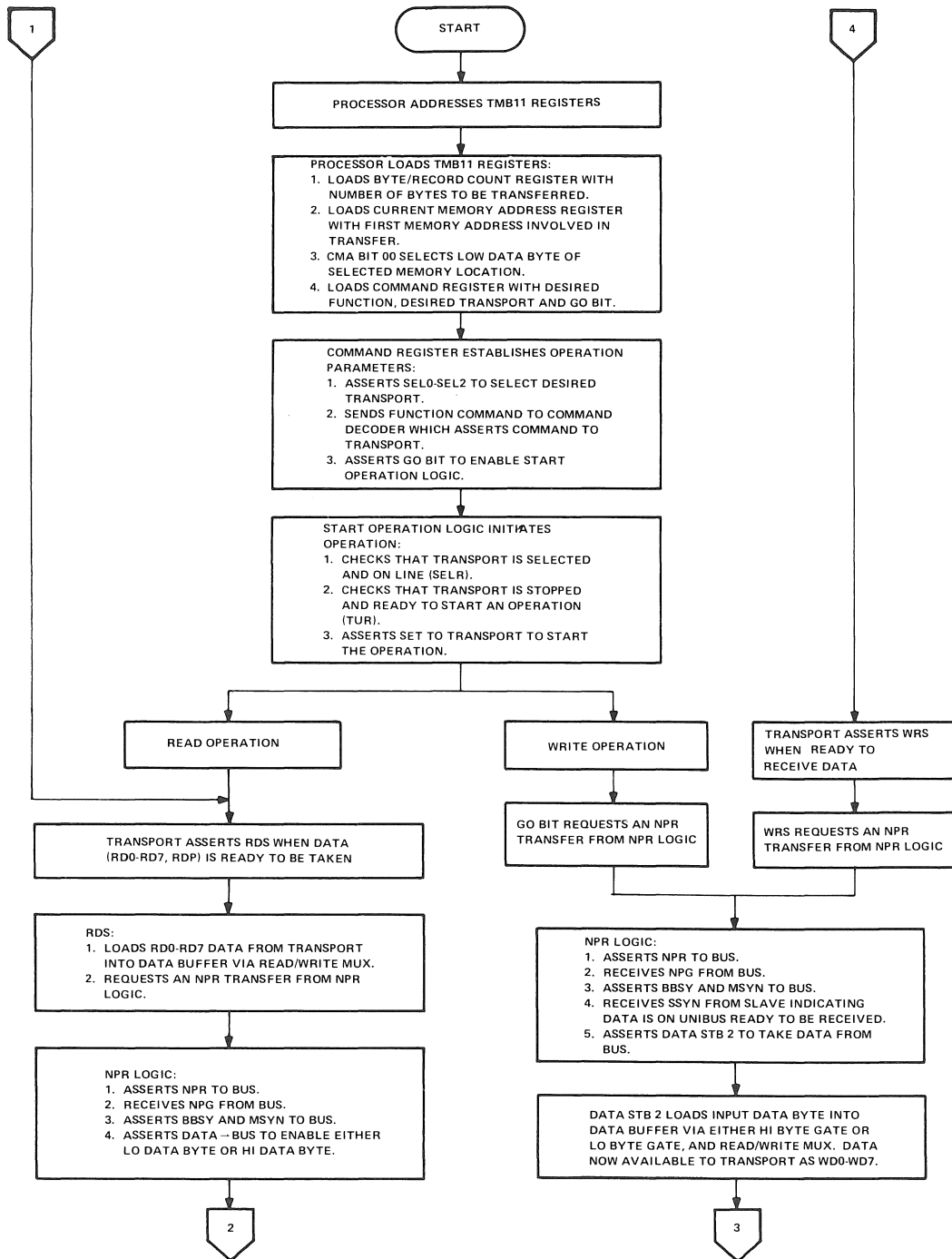
Figure 6-1 TMB11 Flow Diagram (Sheet 1 of 2)
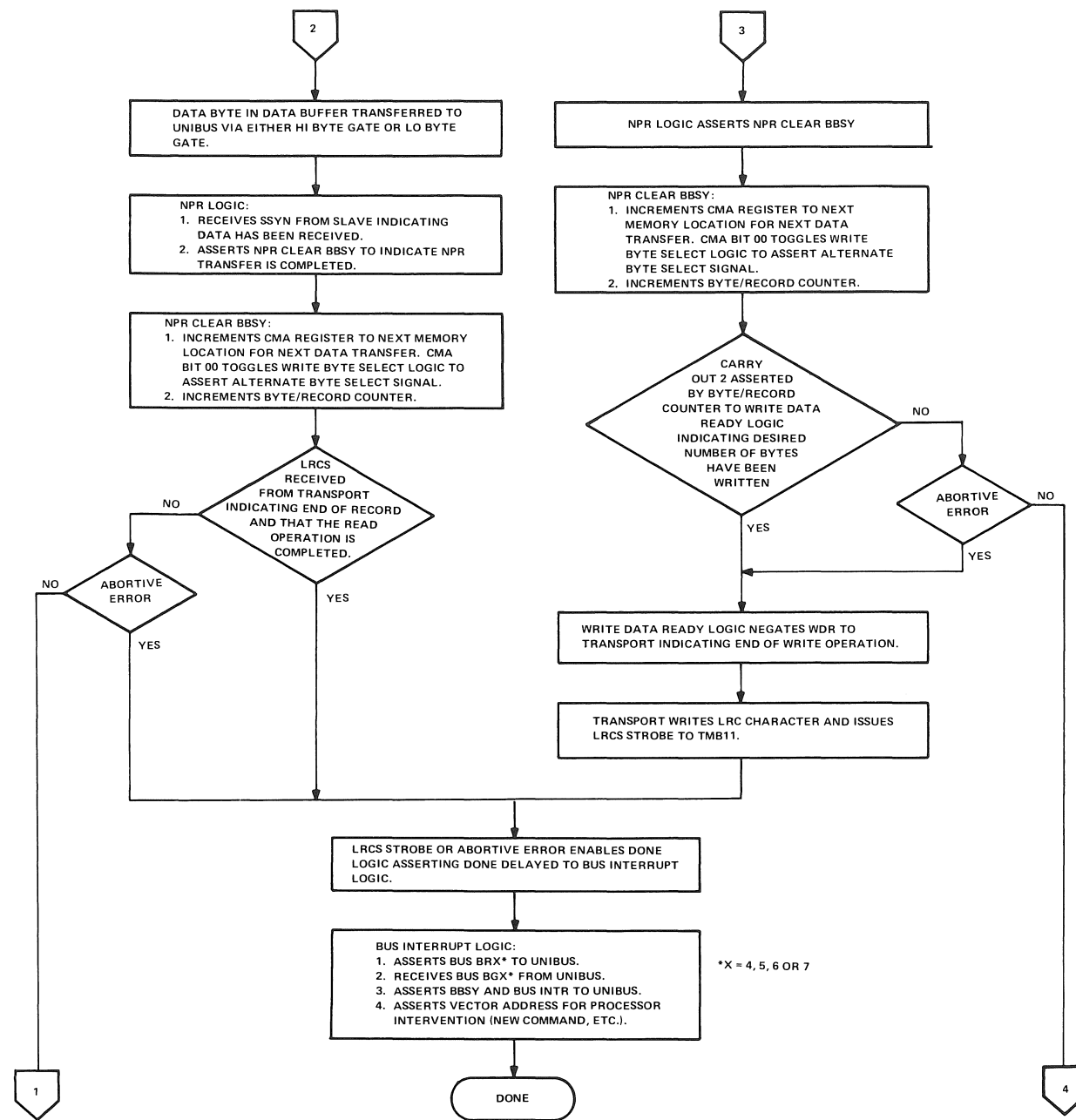
Figure 6-1   TMB11 Flow Diagram (Sheet 2 of 2)
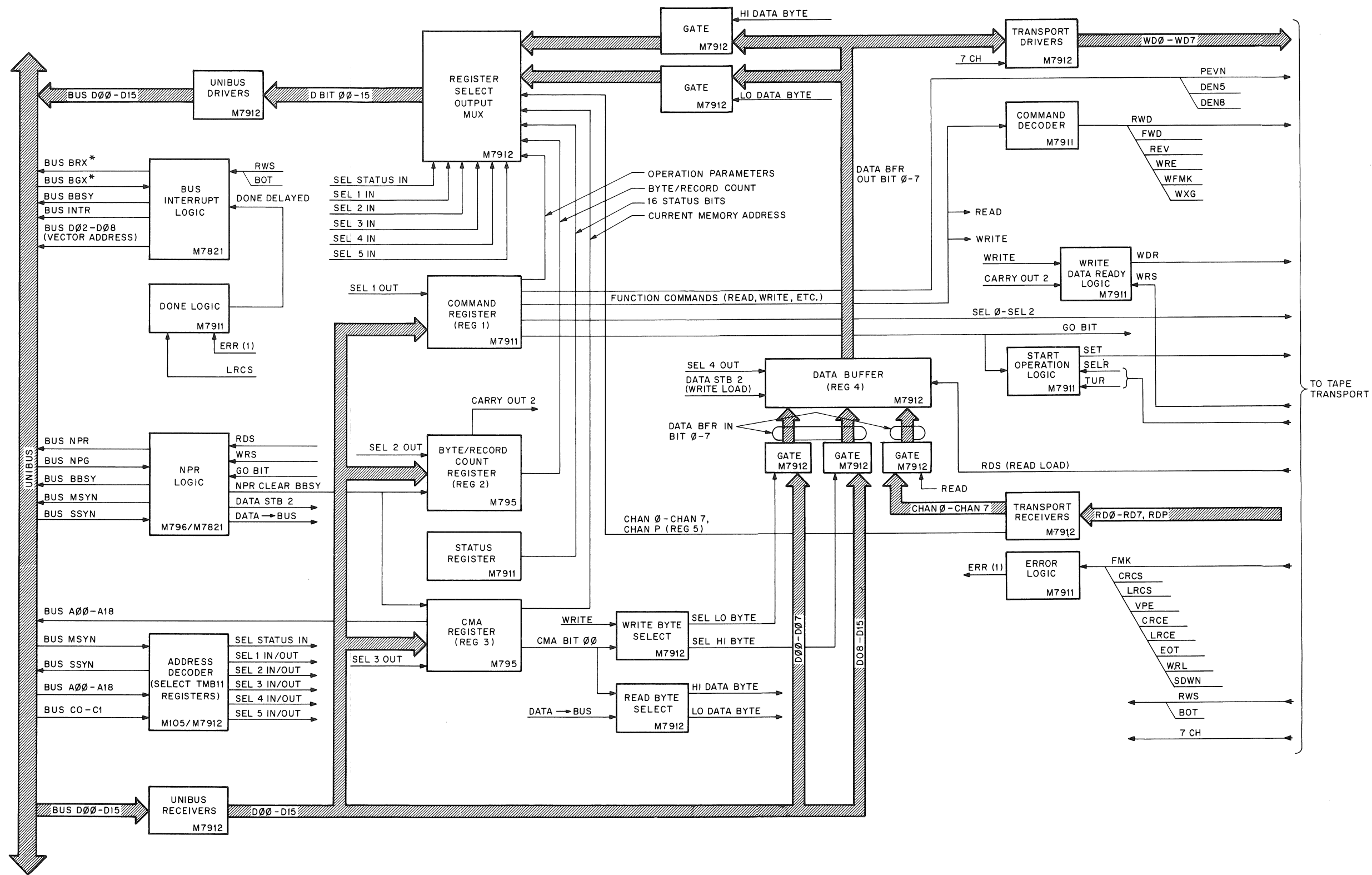
Figure 6-2 TMB11 Functional Block Diagram

Table 6-1   Device Register Functions

Register	Address	Mnemonic	Function
Status Register	772520	MTS	Provides detailed information on the status of the controller. Such information includes error indications and tape unit status indications.
Command Register	772522	MTC	This is the main control register in the controller. Specifies the operation to be performed on the tape unit, selects the tape bit packing density, and selects the tape unit to be used. Indicates when the controller is ready, when an error condition exists, and when the controller is cleared. Provides the two extended address bits for bus addresses.
Byte Record Counter	772524	MTBRC	Counts the number of bytes in any write operation, the number of records in a space forward or space reverse operation, and the number of bytes in a read operation. Desired byte count is preset by the program. When the register counts the number of specified bytes, it prevents further transfers.
Current Memory Address Register	772526	MTCMA	Specifies the bus or memory address to or from which data is transferred during read and write operations. After each transfer is completed, the register is automatically incremented by 1 (next byte location). When BGL or NXM errors occur, the register contains the address of the location in which the failure occurred. Note that this register is incremented by 1, and therefore, accesses byte, rather than word, locations.
Data Buffer Register	772530	MTD	Contains the information read from or written on the tape. Serves as a buffer between the tape unit and the memory.
Tape Unit Read Lines	772532	MTRD	Permits storage of data read from the tape transport. A parity bit indicates the occurrence of a parity error and the channel containing the error. A character selector bit is used to select the last character of a record that is to be loaded into the data buffer register. A timer bit is used for diagnostic purposes by measuring the time duration of the tape operations. A BTE/OPI bit is used to set transfer done prematurely in order to provide a bad tape error indication.

Figures 6-3 through 6-9 show the bit assignments within the six device registers. Except in the case of the data buffer register, the "unused" and "load only" bits are always read as 0s. Loading "unused" or "read only" bits has no effect on the bit position.

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction; depressing the START switch on the processor console; or occurrence of a power-up or power-down condition of either the processor power supply or the controller power supply.

The INIT signal clears the entire system; however, the INIT signal produced by a RESET instruction does not clear the processor. Clearing only the controller and the tape units can be accomplished by loading a 1 into bit 12 (POWER CLEAR) of the command register (MTC).

NOTE
INIT and POWER CLEAR deselect the current
tape unit and select tape unit 0. Also, a rewind oper-
ation in progress continues to the load point.

6.4.1 Status Register (MTS)
Address = 772520. All bits are read only.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ILC	EOF	CRE	PAE	BGL	EOT	RLE	OPI/BTE	NXM	SELR	BOT	7CH	SDWN	WRL	RWS	TUR

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Figure 6-3   Status Register (MTS) Bit Assignments

Bit   Meaning and Operation

15   ILC – Illegal command bit. Indicates an illegal command. This bit is set whenever one of the following illegal commands occur:

a.   Any DATO or DATOB transfer to the command register (MTC) during tape operation (CU RDY bit clear). The register cannot accept a new command while in the process of executing another command.

b.   A write, write end-of-file, or write-with-extended-IRG (command register functions 2, 3, and 6, respectively), when the WRL (write lock) bit is set. Writing is inhibited with WRL set, and write commands are illegal.

c.   Any command to a tape unit that has its SELR bit clear is illegal, because SELR clear indicates that the unit is not on-line.

d.   Any time the SELR bit becomes 0 during any operation except off-line, it sets the ILC bit, because no command can be issued to a unit that is not on-line.

If any of the illegal commands listed in a through c above occur, the command is loaded into the command register.

In all of the above cases, the ILC bit and the ERR bit (bit 15 in the command register) are set simultaneously.

Cleared by INIT or by the GO pulse to the tape unit.

6-8

Bit	Meaning and Operation

14   EOF – End-of-file bit, used to indicate that the tape has reached the end of the file. An end-of-file (EOF) character is detected during a read, space forward, or space reverse operation. During the read or space forward operations, the EOF bit is set when the EOF character is read. During a space reverse operation, the EOF bit is set when the LRC character following the EOF character is read. The ERR bit (bit 15 in the command register) is set when the LRC character following the EOF character is detected. It is also set during WRITE EOF command.

The EOF bit is set only by the tape unit logic; it is cleared by INIT or by the GO pulse to the tape unit.

The EOF character is loaded into memory during read operations.

13   CRE – Cyclic redundancy error bit. A cyclic redundancy error can be detected during either a read or write operation. This check compares the CRC character, written on a 9-channel tape during a write or a write-with-extended-IRG operation, with the CRC character generated during a read operation.

If the two CRC characters are not the same, the CRCE from the tape unit becomes a 1, forcing the CRE bit to a 1. The ERR bit in the command register, however, is not set until the LRC character is detected.

Cleared by INIT or by the GO pulse to the tape unit.

12   PAE – Parity error bit. When set, this bit indicates that a parity error exists. The PAE bit is the logical OR of both vertical and longitudinal parity errors.

A vertical parity error is indicated on any character in a record; a longitudinal parity error occurs only after the LRC is detected.

A vertical parity error does not affect the transfer of data. In other words, the entire record is transferred to the tape during a write operation or transferred into memory during a read operation.

Both vertical and longitudinal parity errors are detected during read, write, and write-with-extended-IRG operations. The entire record is checked, including the CRC and LRC characters.

Longitudinal parity occurs when an odd number of 1s is detected on any channel in the record. Vertical parity error occurs when an even number of 1s is detected on any character, provided the PEVN bit (bit 11 in the command register) is clear, or if an odd number of 1s is detected when the PEVN bit is set.

When a parity error occurs, PAE is set, and the ERR bit (bit 15 in the command register) is set after the LRC character has been detected.

Cleared by INIT or by the GO pulse to the tape unit.

Bit	Meaning and Operation

11   BGL – Bus grant late bit. If the controller issues a request for the bus and does not receive a bus grant before it must issue another bus request for the following tape character, a bus grant late error occurs.

This error condition is tested only for NPRs (non-processor requests). The BGL bit is set if an NPR bus request is not honored before the controller receives a WRS pulse for a write operation or an RDS pulse for a read operation.

The BGL bit and the ERR bit (bit 15 in the MTC) are set simultaneously, halting the operation.

If the BGL error occurred during a write or write-with-extended-IRG operation, the controller does not send the WDR signal to the master tape unit to allow the master tape unit to write data characters on the tape.

Cleared by INIT or by the GO pulse to the tape unit.

10   EOT – End-of-tape bit. The EOT bit is set as soon as the EOT marker is detected, when the tape is moving in the forward direction. It is cleared as soon as the EOT marker is detected, when the tape is moving in the reverse direction.

The EOT is an error condition if the tape is moving forward. Therefore, when EOT is set, ERR bit is also set when the LRC character is read.

Cleared by tape transport head passing over EOT marker when tape is moving in the reverse direction.

09   RLE – Record length error bit. The record length error is tested only during read operations. An error is indicated as soon as the byte record counter (MTBRC) attempts to increment beyond 0.

When a record length error occurs, the RLE bit is set, incrementation of the MTBRC and the current memory address register (MTCMA) ceases, and the ERR bit is set when the LRC character is read.

The CU RDY (bit 07 of the command register) remains cleared until the LRC character is read at which time CU RDY is set.

Cleared by INIT or by the GO pulse to the tape unit.

If the exact record length is desired following the occurrence of a record length error, it can be found by setting the MTBRC to a value so large as not to generate an RLE and re-reading the record. Record length can be derived by subtracting the current value of the MTBRC from its initial setting.

Bit	Meaning and Operation

08   BTE/OPI – Bad tape error operation incomplete bit. A bad tape error occurs when a character is detected (RDS pulse) during the gap shutdown or settle down period for any tape function except rewind.

During write, write EOF, or write-with-extended-IRG operations, a bad tape error sets both the BTE/OPI and ERR bits immediately on detecting the error.

During both read and space forward or space reverse operations, the BTE/OPI bit is set immediately on detection of bad tape.

During a read operation, the MTBRC increments continuously and words are read into memory until the MTBRC overflows. During a space operation, the MTBRC stops incrementing as soon as BTE occurs. When BTE is discovered, the tape unit stops, regardless of the state of the MTBRC.

Because it is not possible to artificially generate bad tape, bad tape may be indicated by setting the CU RDY bit prematurely, thereby producing the gap shutdown period while the data is still being read. The CU RDY bit is set by loading a 1 into bit 13 of the MTRD. If bit 13 of the MTRD is set during a record for either a read or write operation, a bad tape error indication occurs.

Any initiated tape operation other than a REWIND or OFF-LINE command that does not detect an LRC character within seven seconds results in setting the BTE/OPI bit. This 7-second time-out is called Operation Incomplete. Any legal size record with a legal size gap results in detection of an LRC character within seven seconds. During a spacing operation, the OPI timer is restarted at each interrecord gap. When the 7-second time-out occurs, the tape unit in operation is RESET by CINIT. The BTE/OPI bit is set and at TUR the CU RDY bit is set.

Cleared by INIT or GO.

07   NXM – Nonexistent memory bit. This error condition occurs when the controller is bus master during NPR transfers and does not receive an SSYN response within 20 μs after asserting MSYN.

The NXM bit and the ERR bit are set simultaneously, halting the operation.

Cleared by INIT or by the GO pulse to the tape unit.

06   SELR – Select remote bit. The SELR bit is set when the tape unit has been properly selected. The SELR bit is 0 if the tape unit that is addressed does not exist (UNIT SELECT setting does not correspond to SEL bits), if the selected tape unit is off-line (ON-LINE/OFF-LINE switch set to OFF-LINE), or if the tape unit power is off.

05   BOT – Beginning-of-tape bit. The BOT bit is set as soon as the BOT marker is detected. When BOT is set, it has no effect on the ERR bit. The BOT bit remains cleared whenever the BOT marker is not being read.

This bit is set and cleared only by the tape transport.

Bit	Meaning and Operation

04   7CH – 7-channel bit. This bit is cleared or set by the tape transport to indicate whether a 7-channel or 9-channel tape is being used.

When 7CH bit is set, it indicates a 7-channel tape; when it is clear, it indicates a 9-channel tape.

The 7CH bit is also used in conjunction with the DEN 8 and DEN 5 bits in the command register to cause the core dump mode of operation. When the 7CH, DEN 8, and DEN 5 bits are all set, the core dump mode of operation is used.

03   SDWN – Settle down bit. The settling down period is provided to allow the tape to fully stop prior to starting a new operation. This settling down period sets the SDWN bit. When the tape unit stops, SDWN is cleared, and the tape unit ready (TUR) bit is set.

During a tape reverse operation (this does not include rewind operations), the gap shutdown period begins immediately after the first gap encountered after spacing over a record.

02   WRL – Write lock bit. The write lock bit is under control of the tape transport. When set, it prevents the controller from writing information on the tape.

01   RWS – Rewind status bit. This bit is under control of the tape unit. It is set at the start of a rewind operation and clears as soon as the rewind sequence is complete.

00   TUR – Tape unit ready bit. This bit is under control of the tape transport. Whenever the selected tape unit is being used (such as rewind), this bit is cleared. When the tape unit is stopped and ready to receive a new command, the tape transport sets the TUR bit.

NOTE
Status register bits 00 – 05 are cleared or set by the
tape transport, not the controller.

6.4.2 Command Register (MTC)
Address = 772522. Bit 07 is read-only. All others are read/write.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	DEN 8	DEN 5	PWR CLR	PEVN	SEL 2	SEL 1	SEL 0	CU RDY	INT ENB	ADRS BIT 17	ADRS BIT 16	FCTN BIT 2	FCTN BIT 1	FCTN BIT 0	GO

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Figure 6-4   Command Register (MTC) Bit Assignments

Bit	Meaning and Operation

15   ERR – Indicates an error condition that is the inclusive OR of all error conditions (bits 15 – 07 in the Status Register, MTS). Causes an interrupt if enabled (see bit 06). The ERR bit is not set for some errors until the longitudinal redundancy check (LRC) character is read, in order to allow the current operation to be completed. Specific error conditions are described in the status register bit assignments (Figure 6-3).

When ERR is set, it sets bit 07 (CU RDY) when the tape unit asserts TUR.

Cleared by INIT or by the next GO command (bit 00).

14   DEN 8 – This bit, in conjunction with bit 13, selects the bit packing density of the tape. These combinations are shown below. Note that this bit, in conjunction with DEN 5 and 7CH in the MTS, can be used to select the core dump mode for 7-channel tape.

Bit 14 (DEN 8)	Bit 13 (DEN 5)	Density (bpi)	
0	0	200	⎫
0	1	556	⎬ 7-channel tape
1	0	800	⎭
1	1	800	9-channel tape/7-channel core dump

13   DEN 5 – This bit, in conjunction with bit 14, selects the bit packing density of the tape. See bit 14 above for combinations.

12   PWR CLR – When a 1 is loaded into this bit position, it clears the controller logic and all tape units. This bit becomes a 1 for 1 μs during a processor DATO cycle, provided the corresponding bit on the bus is a 1. Always read by processor as a 0.

11   PEVN – This is the even parity bit. This bit is set whenever the selected tape unit is to write or read even vertical parity on or from the tape. The bit is 0 whenever the selected tape unit is to write or read odd vertical parity on or from the tape.

A search for parity error is made whenever the tape moves. The controller ignores parity errors during space forward, space reverse, or rewind operations.

Cleared by INIT or by loading with a 0.

10–08   SEL – These three unit select bits specify the number of the tape unit that is to function as the unit under program control. These three bits (SEL 2, SEL 1, and SEL 0) are set or cleared to represent an octal code that corresponds to the unit number of the tape unit to be used. The tape unit number is selected by the UNIT SELECT plug on the tape transport.

Cleared by INIT or by loading with a 0.

Bit	Meaning and Operation
07	CU RDY – When set, indicates that the controller is ready to receive a new command. This bit is set at the end of a tape operation (indicating that a new operation can be started) and is cleared at the beginning of a tape operation (indicating that the controller is not ready for new commands).

This bit is also set (indicating CU RDY) whenever ILC (bit 15 of MTS) is set or whenever INIT is generated. |
| 06 | INT ENB – Interrupt enable bit. This bit, when set, allows an interrupt to occur, provided either CU RDY (bit 07) or ILC (bit 15 of MTS) is set. With INT ENB set, a REWIND command can cause two interrupts – one at initiation and one at completion.

An interrupt also occurs whenever an instruction sets the INT ENB bit but does not set the GO bit (bit 00). Interrupts are described in Paragraph 6.2.4.

Cleared by INIT or by loading with a 0. |
05	ADRS BIT 17 – Extended bus address bit 17. Used to specify address line 17 in direct memory transfers. Increments with the current memory address register (MTCMA). Cleared by INIT.
04	ADRS BIT 16 – Extended bus address bit 16. Function is the same as ADRS BIT 17 (bit 05 above).
03–01	FUNCTION – These bits specify a command to be performed by the selected tape unit. These functions are:

	Function Bits			
Octal No.	03	02	01	Function
0	0	0	0	Off-line
1	0	0	1	Read
2	0	1	0	Write
3	0	1	1	Write end-of-file
4	1	0	0	Space forward
5	1	0	1	Space reverse
6	1	1	0	Write-with-extended IRG
7	1	1	1	Rewind

All function bits cleared by INIT.

Bit	Meaning and Operation
00	GO – Loaded with a 1 from the bus to initiate the function selected. Clears CU RDY bit.

Cleared when GO pulse is sent to tape transport. Normal time duration of bit is 1 μs, but this time may extend to as long as several minutes in the case where the bit is loaded for a tape unit that is in the process of rewinding.

Also cleared by INIT or cleared whenever ILC in the status register is set. |

6.4.3 Byte/Record Counter (MTBRC)
Address = 772524. All bits are read/write.

```
15                                                                    00
┌──────────────────────────────────────────────────────────────────────┐
│        2's  COMPLEMENT OF NUMBER OF BYTES ( OR RECORDS) TO BE COUNTED   │
└──────────────────────────────────────────────────────────────────────┘
                                                              II-0432
```
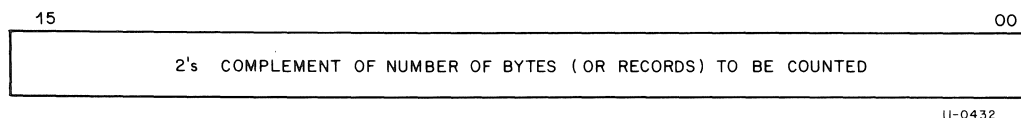
Figure 6-5   Byte/Record Counter (MTBRC) Bit Assignments

Bit	Meaning and Operation
15–00	Contains the 2's complement of the number of bytes or records to be transferred. The desired value is loaded by the program on a processor DATO. Cleared by INIT. Increments by 1 after each memory access.

The byte record counter (MTBRC) is a 16-bit binary counter used to count bytes in a read or write operation and used to count records in space forward or reverse operations.

When used in a write or write-with-extended-IRG operation, this register is set by the program to the 2's complement of the number of bytes to be written on the tape. After the last byte of the record has been strobed from memory, the MTBRC becomes 0. Thus, when the next write strobe signal is received from the master tape transport, the controller lowers the write data ready line to indicate to the master transport that there are no more data characters in the record.

When used in a read operation, the MTBRC is set to a number equal to or greater than the 2's complement of the number of words to be loaded into memory. A record length error, which occurs for long records only, occurs whenever a read pulse is generated after the MTBRC is at 0. Neither the CRC or LRC character is loaded into memory during a read operation, although both characters are checked for parity errors.

When used in a space forward or space reverse operation, the MTBRC is loaded with the 2's complement of the number of *records* to be spaced. The counter is incremented by 1 at LRC time, regardless of tape direction.

6.4.4 Current Memory Address Register (MTCMA)
Address = 772526. All bits are read/write.

```
15                                                                    00
┌──────────────────────────────────────────────────────────────────────┐
│                              BUS  ADDRESS                               │
└──────────────────────────────────────────────────────────────────────┘
                                                              II-0433
```
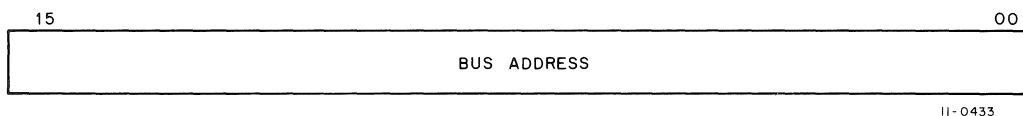
Figure 6-6   Current Memory Address Register (MTCMA) Bit Assignments

| Bit | Meaning and Operation |

15–01   These bits specify the bus or memory address to or from which data is to be transferred during write or read operations. Only bits 01–15 of the MTCMA are accessible by the program, although bits 00–15 participate in NPR transfers. Bit 00 always starts in the cleared or even byte state because all NPR transfers access even boundaries for a starting byte address. Therefore, MTCMA must be initially loaded with an even address.The MTCMA contains 16 of the possible 18 memory address bits. The remaining two bits (16 and 17) are part of the command register.

Before issuing a command, the program loads the MTCMA with the memory address that is to receive the first byte of data (read operation) or with the memory address from which the first byte is to be taken (write operation). After each memory access (read or write), the MTCMA is immediately incremented by 1 (the next byte boundary). Therefore, at any given time, the MTCMA points to the next memory byte address that is to be accessed. On completion of the record transfer, the MTCMA points to the address plus 1 of the last character in the record.

If a bus grant late (BGL) or nonexistent memory (NXM) error occurs, the MTCMA contains the address of the location in which the failure occurred.

If an 18-bit memory address is required, the program loads the appropriate address into bits 01–15 of the MTCMA and into extended address bits 16 and 17 of the command register. The extended address bits are a logical extension to the MTCMA register and participate in any required incrementation.

6.4.5 Data Buffer Register (MTD)
Address = 772530. All bits are read/write.
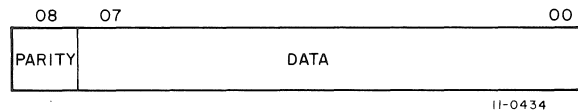
Figure 6-7   Data Buffer Register (MTD) Bit Assignments

| Bit | Meaning and Operation |

15–09
(not shown)   Correspond to bits 07–01 respectively on a processor DATI cycle. Example: Bit 15 = bit 7, bit 14 = bit 6, etc.

08   Correspond to the parity bit of the CRC and LRC characters. During a processor read operation, this bit is stored in memory. During NPR operations, this bit is read by the controller but not loaded into memory. If the CHAR SEL bit (bit 14) of the read lines register is a 1, bit 08 is the parity bit of the LRC character. If the CHAR SEL bit is 0, bit 08 is the parity bit of the CRC character (9-track only).

6-16
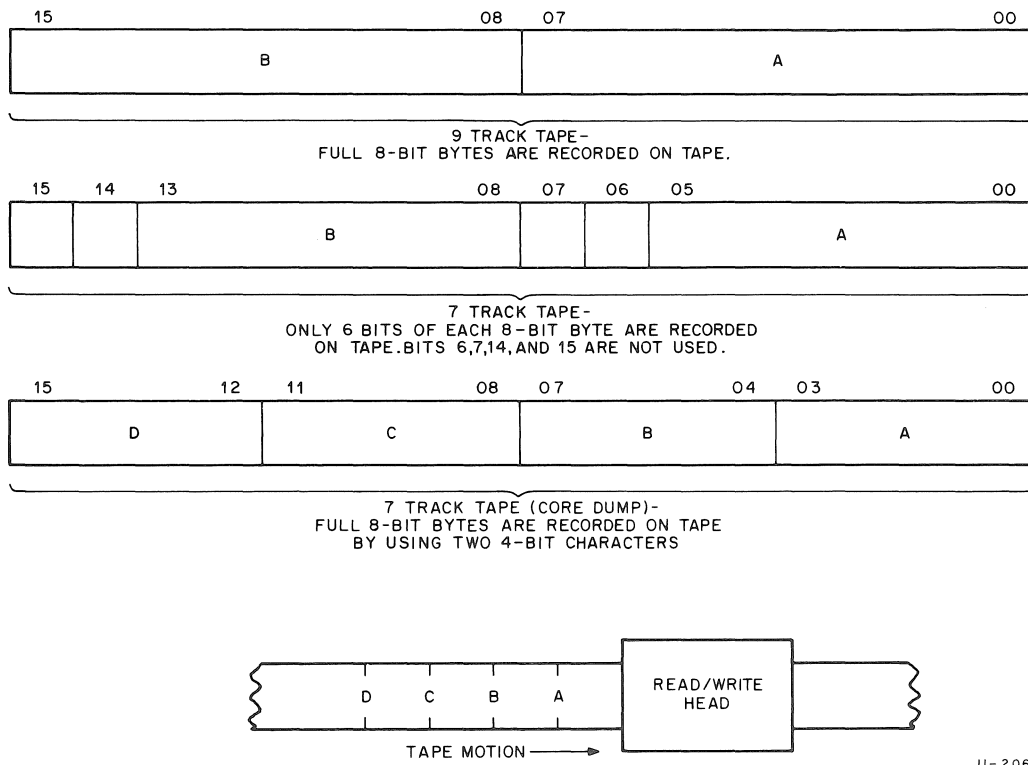
Figure 6-8   Relationship Between Tape Characters and Memory Byte Characters

Bit	Meaning and Operation
07–00	During read operations, these bits are used for temporary storage of characters read from tape prior to loading into memory. During write operations, these bits are used for temporary storage of data from memory before writing on tape.

During read operations, the LRC character enters the data buffer when bit 14 of the address location for the read lines register is a 1; the LRC character is prevented from entering the data buffer when bit 14 is a 0. Thus, after reading a 9-channel tape, the data buffer contains an LRC character (if bit 14 is a 1) or a CRC character (if bit 14 is a 0). After reading a 7-channel tape, the data buffer contains either the LRC character (if bit 14 is a 1) or the last data character (if bit 14 is a 0). After reading an EOF character, the data buffer contains either all 0s (bit 14 is a 1) or the EOF character (bit 14 is a 0).

The data buffer can store only bytes; therefore, two bus cycles are required to transfer a word. During NPR operation the data bits are written into or read from alternate low and high byte positions. The relationship between tape characters and high and low memory byte characters is shown in Figure 6-8.

6.4.6   Read Lines Register (MTRD)
Address = 772532. Read/write function contained in bit descriptions.
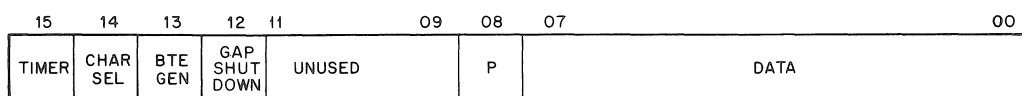
Figure 6-9   Read Lines Register (MTRD) Bit Assignments

6-17

Bit	Meaning and Operation

15   TIMER – The timer bit is used for diagnostic purposes by measuring the time duration of the tape operations. The timer signal is a 100 μs signal with a 50% duty cycle and is generated by the controller. It is read as bit 15 in the memory location reserved for the read data lines register. Read only bit.

14   CHAR SEL – This bit is used to select the last character of a record that is to be loaded into the data buffer. Read/write bit. Selection is as follows:

	7-channel	9-channel
Set	LRC character	LRC character
Clear	Last data character	CRC character

13   BTE GEN – Bad tape error generator bit. Actually, bad tape cannot be artificaly generated. When set, this bit sets the CU RDY bit. With CU RDY set, a premature gap shutdown is generated, which produces a bad tape error indication when data is read during this period. Write only bit.

12   GAP SHUTDOWN – Read only bit. When set, indicates a gap shutdown period.

11–09   Unused.

08   PARITY – Corresponds to the parity bit read from the tape by the master tape transport. Used in conjunction with bits 07–00 to indicate a longitudinal parity error. After a read or write operation, bits 08–00 should all be 0. If one or more of these bits remains a 1 after the operation is complete, it indicates a longitudinal parity error. The bit position containing the 1 indicates the tape channel containing the error. Read only bit.

07–00   DATA – These bit positions contain information read from the magnetic tape transport. After these positions are read by the processor, all bit positions clear unless a parity error exists.

              Bits 07–00 in the read lines register correspond to tape channels 00–07, respectively. Read only bits.

6.5 PROGRAMMING NOTES

In normal programming practice no attempt should be made to modify one record in the middle of a file. This practice could result in overwriting the boundary of the record and destroying part of the next record. Also, a read operation should never directly follow a write operation without at least one intervening tape move operation. This prevents generating a BTE/OPI if the previous operation involved the last record on the tape. If it is desired to read a record that was just written, a space reverse command should be issued before the read command. New commands are issued only when CU RDY is set, which is true after interrupts.

Attempting to write an all zero character with even parity on a 7-track or 9-track tape unit causes the zero character to be converted to a tape character of 20. When reading this character from tape, a 20 is read instead of zero.

ASCII standards provide for a 25-ft trailer following the end-of-tape marker. This allows approximately 10 ft of writing space after passing EOT. Care should be taken when attempting to write past the EOT marker if the operator is not familiar with the tape that he is working with, because after a tape has been used, the reflctive markers are often changed, possibly decreasing the length of the standard 25-ft trailer.

Because the physical displacement of the heads differ between 7-channel and 9-channel drives, records written on one cannot be read by the other. However, a tape that is recorded on one can be re-recorded by the other, providing you begin at the load point.

If two drives are sharing one controller, care should be taken not to allow both drives to have the same unit number selected on the unit select plugs. If they are both set to the same number and a command is issued, they will both attempt to respond and data transfers will become totally confused.

The industry-standard packing density for 9-channel drives is 800 bpi. However, 9-channel drives may be recorded at 200, 556, or 800 bpi, providing the data is read back at the same rate.

A SPACE REVERSE or REWIND command issued while the tape is at the load point will cause an immediate interrupt.

6.5.1 Rewind Operation

Assume drive 0 is to be rewound. The command to rewind drive 0 is issued to the controller. At this time the master tape unit asserts bit 1 (RWS) in the status register. If bit 6 (INT ENB) in the command register was set at the start of the rewind operation, an interrupt occurs from the controller as soon as bit 7 (CU RDY) of the command register has been set by RWS. This informs the program that the controller is ready to accept a new command. By testing bit 1 (RWS) in the status register, the program can determine if this interrupt was issued as a result of drive 0 completing its rewind operation or just beginning it.

When the reflective marker, signifying BOT, is sensed, bit 5 (BOT) is asserted in the status register only for the duration of time that the reflective marker is being read. Tape motion does not stop at this time.

Drive 0, still moving in the reverse direction, passes over the reflective marker, reverses its direction, and proceeds in the forward direction back to the load point. Upon sensing the reflective marker while proceeding in the forward direction, drive 0 halts tape motion, asserts bit 3 (SDWN) allowing the tape to fully deskew, and then sets bit 0 (TUR) in the status register.

An interrupt is issued coincident with bit 0 (TUR) being asserted in the status register, providing the following conditions have been met.

1.   Bit 6 (INT ENB) in the command register is set,

2.   The drive has not been deselected by changing the status of bits 10–8 in the command register since issuing the REWIND command.

If multiple transports are used, it is not necessary to wait for a REWIND command to be completed on one transport before switching to another. After a REWIND is issued, another transport can be switched to as soon as RWS is set.

When operations on the second transport have been completed, a switch to the rewinding transport can be made as soon as SDWN or TUR is true on the second transport (so the status bits will be from the rewinding unit). Only the unit select bits in the command register have to be changed to the unit that is rewinding to get its status. If the rewind is complete when the unit is selected, TUR is set in the status register. If the RWS bit is still set, the software can either work on another transport or load the next command to be executed in bits 1–3 of the command register where it is buffered until the rewind is completed. If INT ENB is set at this time, the completion of the buffered command causes an interrupt to occur. A REWIND command may take from 3 to 5 minutes to complete.

6.5.2 New Drive Selection

Figure 6-10 is a flowchart for new drive selection.

```
                    ┌─────────────┐
                    │  START NEW  │
                    │  OPERATION  │
                    └──────┬──────┘
                           │
                           ▼
                    ╱─────────────╲         YES
                   ╱  NEW UNIT =   ╲──────────────┐
                   ╲   OLD UNIT    ╱              │
                    ╲      ?      ╱               │
                     ╲───────────╱                │
                           │ NO                   │
                           ▼                      │
                    ┌──────────────┐              │
                    │LOAD NEW UNIT#│              │
                    │AND CLEAR INT.│              │
                    │ENB.          │              │
                    └──────┬───────┘              │
                           │                      │
                           ▼                      │
                    ┌──────────────┐              │
                    │ DELAY ≥ 28 μs│              │
                    └──────┬───────┘              │
                           │◄─────────────────────┘
                           ▼
                    ╱─────────────╲     NO
                   ╱   SELR = 1    ╲─────────► ERROR
                   ╲      ?        ╱
                    ╲─────────────╱
                           │ YES
                           ▼
                    ┌──────────────┐
                    │  LOAD NEW    │
                    │  COMMAND     │
                    │  AND INT.ENB.│
                    └──────────────┘
```
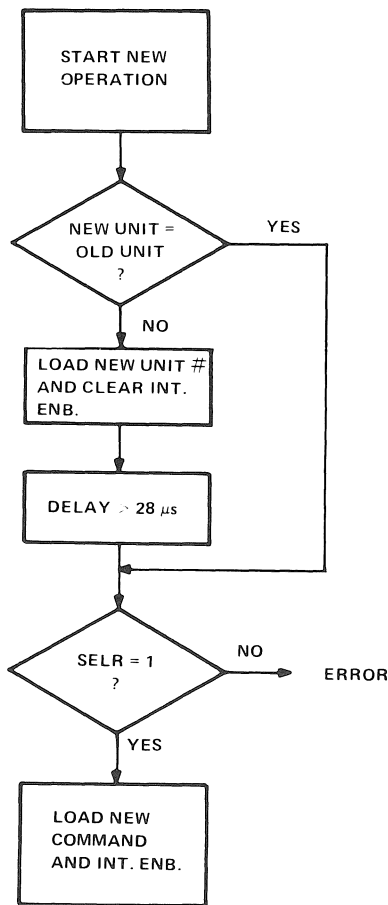
11-2673

Figure 6-10   New Drive Selection Flowchart

Other programming restrictions occur when using select remote along with tape unit ready. The select remote lines for all tape units that are not addressed are at 0. A tape operation may be performed only on a selected tape unit and one whose SELR line is a 1. Thus, whenever a command is sent to a different tape unit from the one presently indicated by the unit select bits, the SELR line becomes 0 almost immediately (less than one instruction time later) and becomes a 1 from 1 to 28 microseconds later.

6.5.3 Error Handling

6.5.3.1 Write Operations

1. ILC – Illegal Command

   - If SELR (bit 6 of MTS) is not set to a 1, or WRL (bit 2 of MTS) is set to a 1, then operator intervention is required to ensure that the drive to be used is properly selected and is not write locked.

   - If SELR (bit 6 of MTS) is set to a 1 and WRL (bit 2 of MTS) is not set to a 1, then a command has been issued while CU RDY (bit 7 of MTC) was cleared. Try the operation again, ensuring first that CU RDY is set before issuing a new command.

2. EOF – End-of-File   N/A

3. CRE – Cyclic Redundancy Error
   Backspace and try operation again with extended IRG.

4. PAE – Parity Error
   Backspace and try operation again with extended IRG.

5. BGL – Bus Grant Late
   Backspace and try operation N times.

6. EOT – End-of-Tape
   The reflective marker signifying the end-of-tape has been passed. Operations past this point are not illegal; however, they are not recommended unless the programmer is familiar with the tape being used and is knowledgeable about the length of tape existing past the EOT marker. Conducting any write operations past the EOT marker leaves the programmer open to the possibility of running the tape off of the reel.

7. RLE – Record Length Error   N/A

8. BTE/OPI – Bad Tape Error/Operation Incomplete
   Regain a known tape position and try the operation again with extended IRG.

> **NOTE**
> A known tape position refers to BOT, header records, or EOF marks.

9. NXM –Nonexistent Memory
   Resolve the memory discrepancy and try the operation again.

6.5.3.2 Read Operations

1. ILC – Illegal Command

   - If SELR (bit 6 of MTS) is not set, then operator intervention is required to ensure that the drive to be used is properly selected.

   - If SELR (bit 6 of MTS) is set, then a command has been issued while CU RDY (bit 7 of MTC) was cleared. Try the operation again ensuring that CU RDY is set prior to issuing the new command.

2. EOF – End-of-File
   The characters signifying the end of a file have been read.

3. CRE – Cyclic Redundancy Error
   Backspace and try the operation N times.

4. PAE – Parity Error
   Backspace and try the operation N times.

5. BGL – Bus Grant Late
   Backspace and try the operation N times.

6. EOT – End-of-Tape
   The reflective marker signifying the end-of-tape has been passed. Continue only if it is certain that an EOF mark exists after the EOT marker, or the tape will run off of the reel.

7. RLE – Record Length Error
   Reset the MTBRC to a value that is equal to or greater than the number of bytes in the record, backspace, and try the operation again.

8. BTE/OPI – Bad Tape Error/Operation Incomplete
   Regain a known tape position and try the operation again. If, after doing so, the condition still persists, the data from the failing point to the next known tape position is lost.

9. NXM –Nonexistent Memory
   Resolve the memory location discrepancy and try the operation again.

6.5.3.3 Write End-of-File Operation

BTE/OPI – Bad Tape Error/Operation Incomplete.
Regain a known tape position and try the operation again.

6.5.3.4 Spacing Operations

1. ILC – Illegal Command
   Same as read operation.

2. EOF – End-of-File
   The characters signifying the end of a file have been read. Detection of the EOF marks stops a spacing operation even if the MTBRC is not equal to zero.

3. EOT – End-of-Tape
   Same as read operation.

4. BTE/OPI – Bad Tape Error/Operation Incomplete
   Regain a known tape position and try N times.

6.5.3.5 Write-with-Extended-IRG Operation – Same as write operation.

6.5.3.6 Rewind Operation – Once a rewind operation is started, it continues until complete, regardless of errors or unit deselection.

6.6 FUNCTIONAL DESCRIPTIONS

The TMB11 Controller may be divided into eight functional areas as follows:

1. Processor Data Transfer – The reading or writing of TMB11 registers by the processor (DATI/DATO).

2. Operation Start – The sequence from setting the GO bit to issuing SET to the transport to start tape motion.

3. NPR Bus Cycle – Acquiring bus mastership for an NPR transfer.

4. NPR Read (DATO) – The transfer of characters from the tape transport to memory.

5. NPR Write (DATI) – The transfer of characters from memory to the tape transport.

6. Operation Done – The terminating sequence of a TMB11 operation.

7. Error Sequence – The system errors detected by the controller and how they occur.

8. Interrupt Bus Cycle – Acquiring bus mastership for a processor interrupt.

These eight functional areas are discussed in the following paragraphs. Block diagrams, flow diagrams, and timing diagrams complement the discussions.

NOTE

The block diagrams that follow use logical AND and OR symbols. It does not necessarily follow that a corresponding gate exists on the controller logic prints. The assertion of inputs A and B causing the assertion of output C may be represented on a block diagram by a single AND gate yet the engineering drawing may show that several circuit stages are involved in the ANDing operation.

The signal names used on the functional block diagrams are the names used on the engineering circuit schematics (CS prints). Where other signal names or notes are used they are enclosed in parentheses.

Integrated circuit data sheets are contained in Appendix E.

6.6.1 Processor Data Transfer

6.6.1.1 Processor Out (DATO) Transfer (TMB11 Register Write) (Figures 6-12 and 6-13) – The processor selects the TMB11 for a data transfer by asserting the proper address on BUS A04–A17 to the TMB11 address decoder (address range = 772520 to 772536.*) When the decoder recognizes the proper address it enables the address MSYN gate which asserts ADDR DEC MSYN when BUS MSYN is received from the processor. ADDR DEC MSYN enables the select in/out logic which looks at BUS A01–A03 to select one of the six controller registers. The control select logic looks at BUS C0–C1 and BUS A00 and asserts OUT HI, OUT LO, or neither according to whether a high byte is to be written, a low byte is to be written, or a processor read operation is to occur. The control select output enables the corresponding portion of the select in/out logic which outputs the loading strobe for the selected register.

---

*Address locations 772534 and 772536 are not used.

When an "out" transfer is commanded, the SEL (1,4,5) OUT HI strobes will load their respective registers, when selected.* The SEL 2 OUT HI, SEL 3 OUT HI, and SEL 1 OUT LO through SEL 4 OUT LO strobes are ANDed with SSYN INH to produce corresponding SLCT loading strobes. SSYN INH is produced by inverting ADDR DEC MSYN on the M105 module. A delay occurs with the inversion, thus the loading of registers with SLCT strobes will be later (with respect to BUS MSYN) than the loading of those with SEL strobes.

The information is strobed into the selected register a byte at a time; D00 – D07 = low byte, D08 – D15 = high byte.

SSYN INH becomes BUS SSYN to notify the processor that the information on the data bus has been strobed into the selected register.

The command register contains the type of operation to be performed and the operation parameters. D13 and D14 are the density bits outputting DEN 5 and DEN 8. The processor sets these bits according to the desired mode of operation as shown in Table 6-2.

Table 6-2   Modes of Operation

Mode	DEN 5	DEN 8
200 bpi, 7-track	0	0
556 bpi, 7-track	1	0
800 bpi, 7-track	0	1
800 bpi, 9-track	1	1

The core dump mode is enabled when the program asserts both DEN 5 and DEN 8 while the 7-channel (7CH) signal from the tape transport is true (indicating that a 7-channel tape transport is being used). DEN 5 (1) and DEN 8 (1) are applied to an AND gate that is enabled by the 7CH signal from the transport. The output from this AND gate is CORE DUMP which, when true, inhibits the DEN 5 AND gate thereby negating DEN 5. Thus, an 01 density code is sent to the tape transport indicating an 800 bpi data transfer.

The command register also specifies even or odd parity to the transport (PEVN), selects the desired transport (SEL0–SEL2), enables or inhibits BR cycles (INT ENB), and specifies the function that the transport is to perform via a 3-bit function decoder. In addition, the command register carries 2 memory address bits to extend the current memory address register to 18 bits. Bit 00 of the command register is the GO bit which initiates the commanded operation.

Other registers addressed during a processor out-operation are:

- The current memory address register, which is loaded with the address of the first byte to be transferred

- The byte record counter, which is loaded with the 2's complement of the number of bytes to be transferred

- The LRC ENB (1) bit of the read lines register which, when set, allows the LRC character to be read into the data buffer.

---

*See Figure 6-27 for processor write of register 4.

6.6.1.2 Command Decoder (Figure 6-11) – The command decoder converts the eight functions generated by the command register function decoder into the six commands required by the tape transport. Figure 6-11 illustrates the functions that make up each of the transport commands. Table 6-3 illustrates the conversion in tabular form.
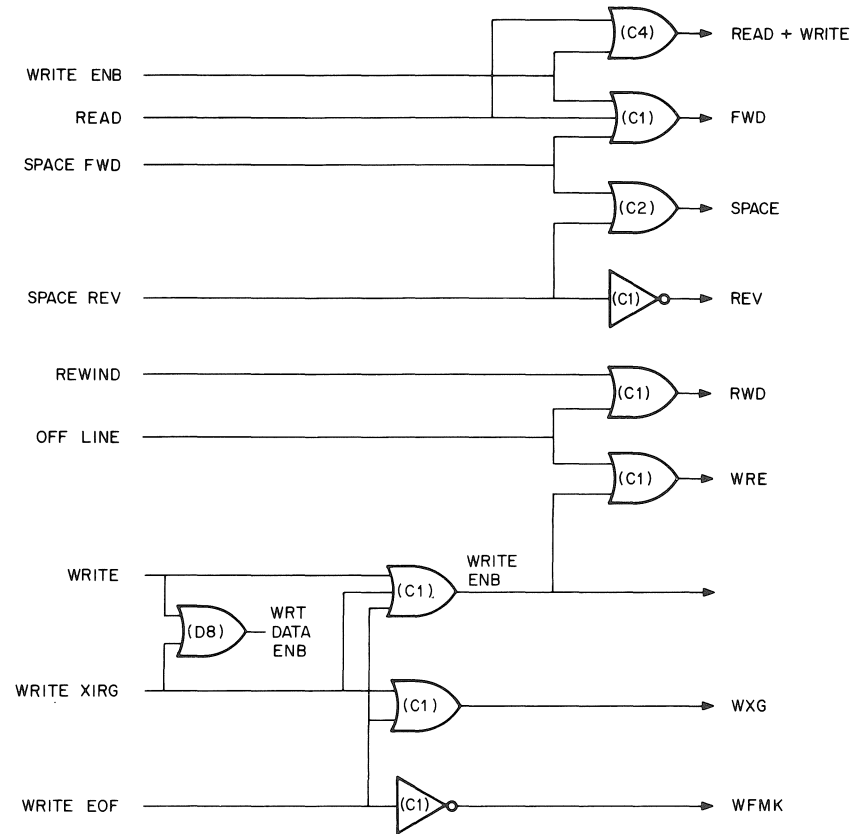
NOTE:
Designations in parenthesis refer to engineering drawings
containing corresponding logic.

11-4129

Figure 6-11   Command Decoder Logic Diagram

Table 6-3   Function Decoder Output vs Transport Commands

COMMAND DECODER FUNCTIONS	TRANSPORT COMMANDS					
	FWD	REV	RWD	WRE	WXG	WFMK
OFF LINE			X	X		
READ	X					
WRITE	X			X		
WRITE EOF	X			X	X	X
SPACE FWD	X					
SPACE REV		X				
WRITE XIRG	X			X	X	
REWIND			X			

6-25

The conversion is mostly ORing and is straightforward except for the OFF LINE function. If the processor orders an OFF LINE function, RWD (rewind) and WRE (write enable) are asserted to the transport. Writing during a rewind is an impossible situation that the transport interprets as an OFF LINE command. Four other signals are generated in the command decoder for use throughout the TMB11. These signals are OR functions of decoder commands as shown in Table 6-4.

Table 6-4   Decoder ORed Functions for TMB11

TMB11 Signal	ORed Function
WRITE DATA ENB	WRITE WRITE XIRG
WRITE ENB	WRITE WRITE XIRG WRITE EOF
READ + WRITE	WRITE WRITE XIRG WRITE EOF READ
SPACE	SPACE FWD SPACE REV

6.6.1.3   Processor In (DATI) Transfer (TMB11 register read) (Figures 6-12 and 6-14) – When an "in" transfer is commanded by the processor, OUT HI and OUT LO from the control select logic are negated thereby enabling the select in logic. BUS A01–A03 selects one of the six controller registers and outputs the corresponding SEL IN gating strobe to the output select multiplexer. Accordingly the 16 bits of the status register, register 1, 2, 3, 4, or the 12 bits of register 5 are gated out to the Unibus via the Unibus drivers (see Figure 6-23 for processor read of register 4).

START

1. BUS A04-A17 SELECTS DEVICE VIA ADDRESS DECODER.
2. BUS A01-A03 SELECTS ONE OF 6 TMB11 REGISTERS.
3. BUS C0-C1, A00 ASSERTS OUT HI, OUT LO, OR NEITHER

PROCESSOR ASSERTS BUS MSYN INDICATING DATA IS AVAILABLE ON UNIBUS

ADDR DEC MSYN

IN TRANSFER SELECTED BY BUS C0-C1.

NO — OUT HI TRANSFER SELECTED BY BUS A00. — YES

NO — YES

YES → ASSERTS SEL STATUS IN OR SEL (1:5) IN AS SELECTED BY BUS A01-A03.

SELECTED REGISTER GATED THROUGH OUTPUT MUX TO UNIBUS VIA UNIBUS DRIVERS.

OUT LO

OUT HI

ASSERTS SEL(1:4) OUT LO AS SELECTED BY BUS A01-A03

ASSERTS SEL(1:5) OUT HI AS SELECTED BY BUS A01-A03

LOADS BITS 1, 2, 3 AND 6 OF REGISTER 1 IF SELECTED.

HI BYTE LOADED INTO SELECTED REGISTER IF REGISTER 1, 4 OR 5 SELECTED.

SSYN INH

SSYN INH

ASSERTS SLCT(1:4) OUT LO ACCORDING TO REGISTER SELECTED.

ASSERTS SLCT(2:3) OUT HI IF REGISTER 2 OR 3 SELECTED.

LO BYTE LOADED INTO SELECTED REGISTER.

HI BYTE LOADED INTO REGISTER 2 OR 3.

DONE

NOTE:
During processor address of the TMB11 an IN transfer is a processor in transfer or a read of the TMB11. An OUT transfer is a processor out transfer or a write into the TMB11.

11-4145

Figure 6-12   Processor In/Out Flow Diagram (DATI/DATO)

6-27
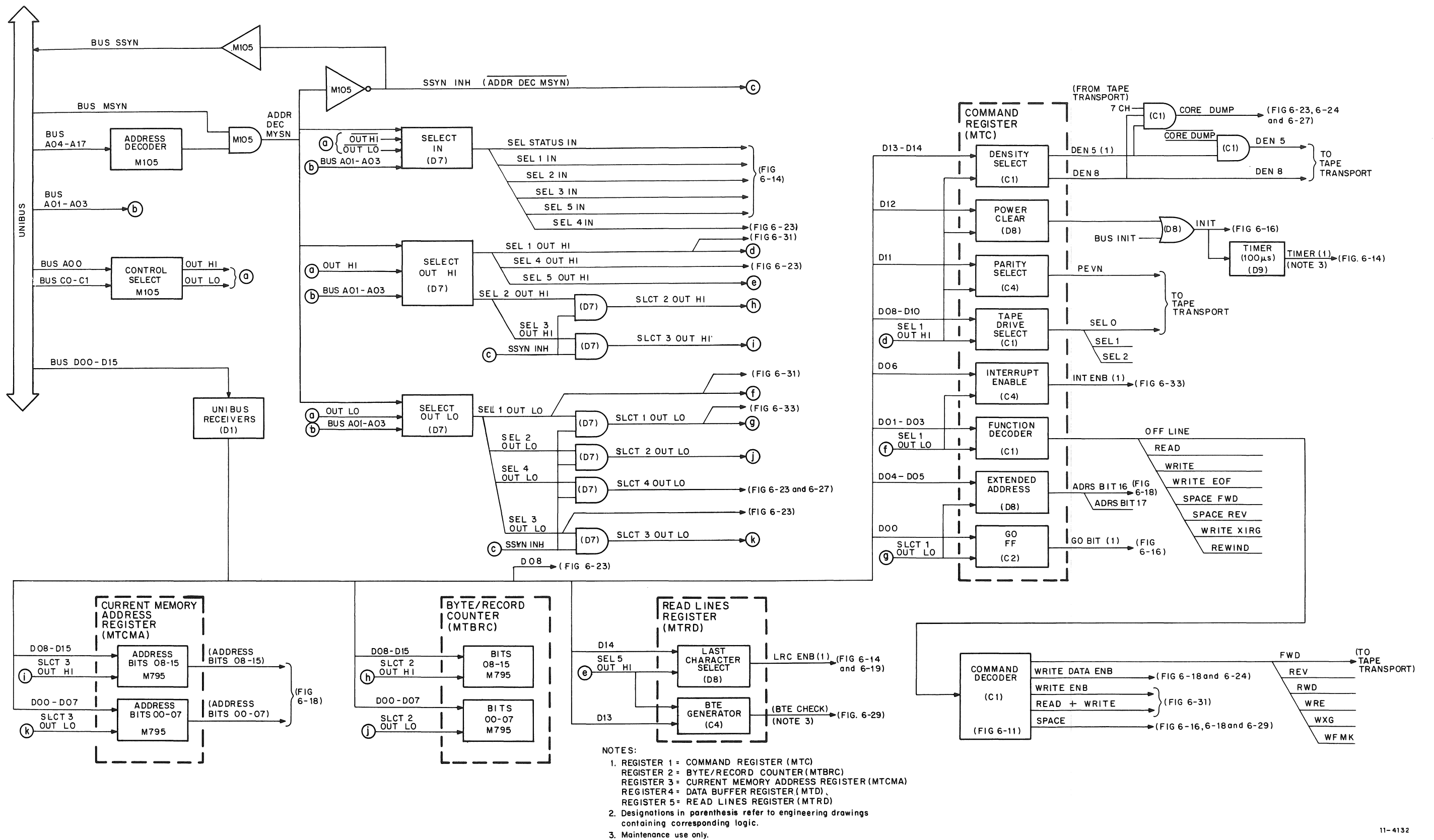
Figure 6-13   Processor Out (DATO)
Block Diagram
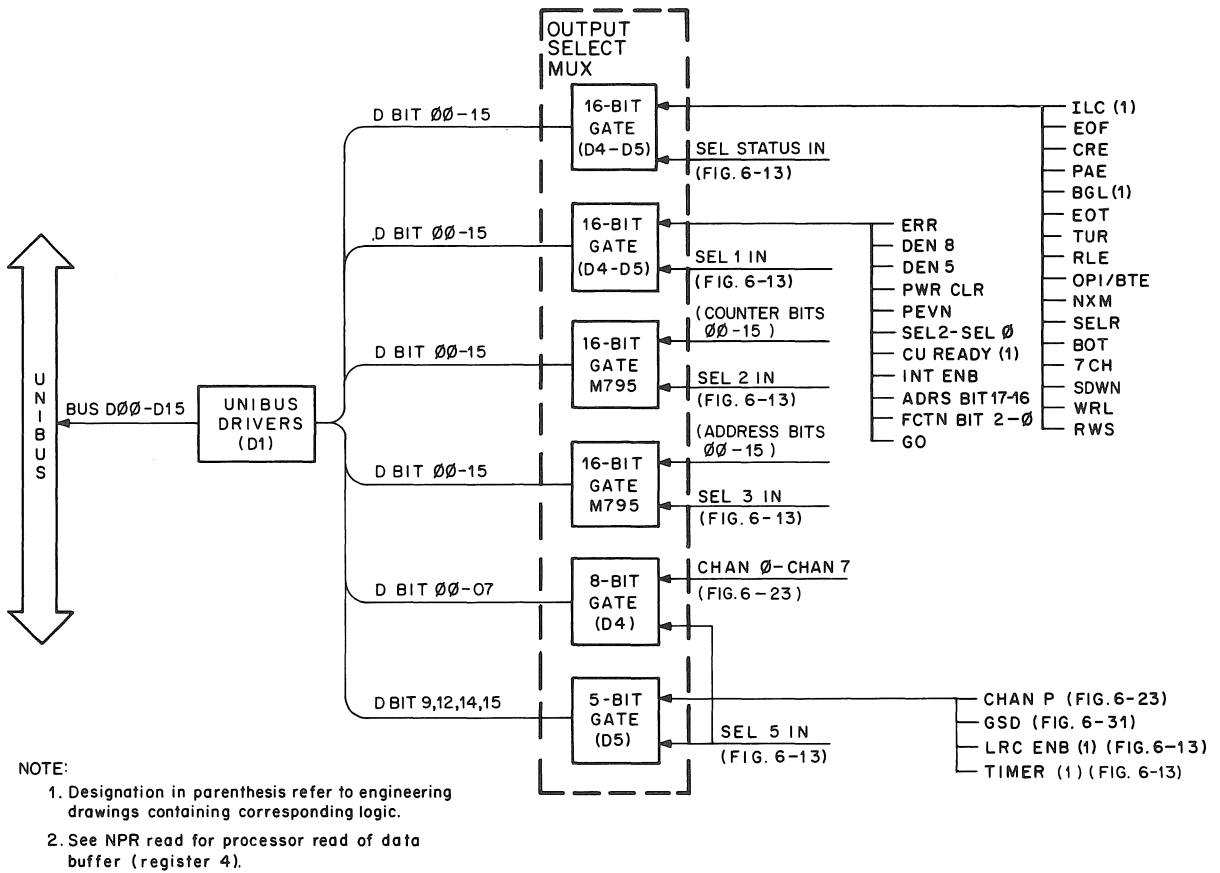
Figure 6-14   Processor In (DATI) Block Diagram

11-4124

6.6.2 Operation Start (Figure 6-15 and 6-16)

6.6.2.1 Basic Sequence – When the command register GO bit is set by the processor a command start sequence is initiated. GO BIT (1) resets the CU ready bit in the command register indicating that the TMB11 is processing a command. If the tape transport is not rewinding and TUR is true, GO BIT (1) triggers the GO strobe 1 one-shot. If the tape transport is rewinding (RWS true) GO BIT (1) will not trigger the one-shot due to the "0" output from the transport rewinding flip-flop. When the rewind is complete, TUR asserts resetting the rewinding flip-flop thereby triggering the GO strobe 1 one-shot. The GO STROBE 1 output of the one-shot resets the request store flip-flop and if SELR is true, the "0" output of the request store flip-flop triggers the GO strobe 2 one-shot. When GO STROBE 2 (1) asserts, the following occurs:

1. SET is asserted to the tape transport if there is no illegal command and if the function is not REWIND or SPACE REV while the tape transport is at BOT (REV BOT false).

2. The GO flip-flop is reset and the request store flip-flop is set in preparation for another GO command from the processor.

3. The trailing edge of GO STROBE 2 (1) resets the CUR delay flip-flop. CUR DEL (1) is negated indicating to the error logic and the done logic that a transport operation is now in progress.

6.6.2.2 Time Out – If the transport is not selected or is not on-line (SELR false), the output of the request store flip-flop will not trigger the GO strobe 2 one-shot. In this case, GO BIT (1) initiates a 28 μs delay after which TIME OUT (1) asserts and triggers the GO strobe 2 one-shot. The assertion of GO STROBE 2 (1) while SELR is negated causes the assertion of SET ILC and ILC (Paragraph 6.6.7) which respectively inhibit the assertion of SET to the transport and initiate a done sequence (Paragraph 6.6.6).

6.6.2.3 Restart – If the system is performing a spacing operation, either forward or reverse, the tape will space through records without coming to a stop at each interrecord gap.

In this case the SET commands required by the transport are generated by RESTART which triggers the GO STROBE 1 one-shot without the necessity of TUR being true. RESTART asserts in the SPACE mode of operation each time SDWN is sensed and the following errors are false: BTE, BGL, NXM, ILC (1), OVERFLOW (1), EOFF (1), and BOT.

6.6.2.4 OPI/BTE – When GO STROBE 2 (1) asserts, a 7-second delay is initiated. If the 7-second time period elapses before an LRCS terminating strobe occurs, OPI is asserted indicating an operation incomplete error. OPI asserts the OPI/BTE bit in the status register and also CINIT to the tape transport resetting the transport logic circuits. The 7-second delay sequence is inhibited during a rewind operation (RWD true) as rewinding the tape could exceed 7 seconds.

6.6.2.5 Initialize – GO STROBE 1 (or an INIT from the processor) asserts INIT + GO which causes a general reset of the TMB11 logic circuits. A general reset of the tape transport is caused by CINIT which is asserted by any of the following conditions:

1. The processor asserts INIT.
2. BOT is reached during a space reverse operation.
3. OPI is asserted.

START

1 → GO BIT (1)

0 → CU READY (1)

SELR — YES

NO

28 µs

TIME OUT (1)

7 SEC

RWD — YES

NO

LRCS — YES

NO

OPI

1 → OPI/BTE (1)

CINIT

TRANSPORT REWINDING — YES

NO

TUR — NO

YES

(START)

1 → GO STROBE 1

RESETS REQUEST STORE FF

SLER — NO

YES

1 → GO STROBE 2 (1)

0 → GO BIT (1) SETS REQUEST STORE FF

A

↑ SDWN

SPACE — NO

YES

※ — YES

NO

RESTART

INIT

INIT + GO

↑ GENERAL TMB11 RESET

A

ILC — YES

NO

1 → ERR (1) DONE DELAYED

REV BOT — YES

NO

SET

0 → GO STROBE 2 (1)

0 → CUR DEL (1)

DONE

※ Any one of the following:
BTE
BGL (1)
NXM
ILC (1)
OVERFLOW (1)
EOFF (1)
BOT

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Figure 6-15   Operation Start Flow Diagram
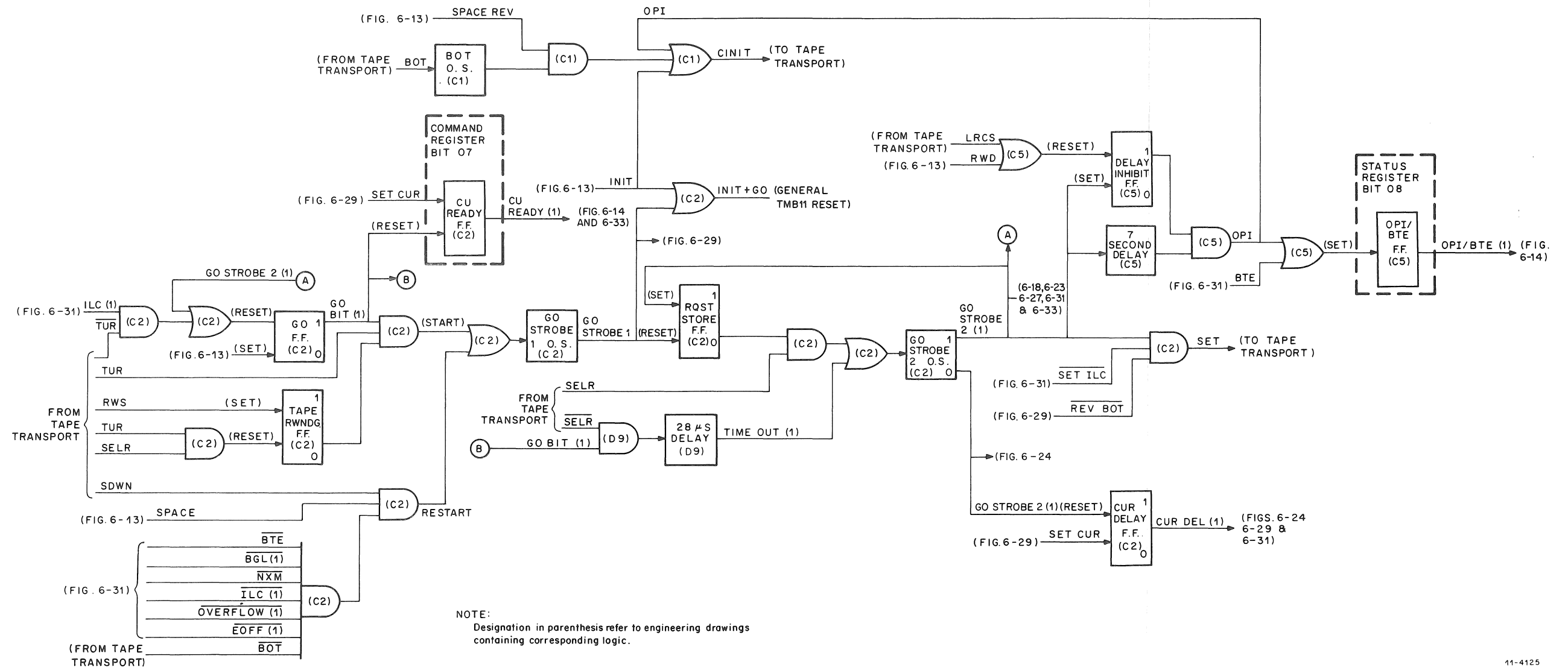
Figure 6-16 Operation Start
Block Diagram

6.6.3 NPR Bus Cycle (Figures 6-17 and 6-18)

6.6.3.1 Basic Sequence – An NPR bus cycle is initiated via the NPR request logic. The request logic generates NPR ENB (1) if:

1. No inhibiting condition exists.
2. The logic is enabled.
3. NPR SET is asserted.

The request logic is inhibited if OVERFLOW (1) is true (the desired number of data records have already been transferred), BGL or NXM is true from the last NPR request, or CRCS or LRCS are asserted (CRC and LRC characters are not transferred to memory). The request logic is enabled by EVEN CHAR STB which is always high in normal 7-track or 9-track modes but only high during even character transfers in core dump mode. Thus in core dump, two characters are read from (or written onto) tape for each NPR bus cycle.

The request logic is set by read strobes or write strobes (RDS + WRS) from the tape transport. If a write operation is being executed (WRITE DATA ENB true) GO STROBE 2 (1) triggers the first NPR bus cycle as the first write strobe is not generated until the first character is written on tape.

The request logic asserts NPR ENB (1) to the Unibus NPR acquisition logic which requests control of the Unibus by asserting BUS NPR. When the processor responds with BUS NPG IN the acquisition logic asserts BUS SACK and the processor responds by negating BUS NPG IN. The acquisition logic checks for BUS BBSY true (by some other device) and if it finds the bus free asserts BUS BBSY (indicating bus mastership) and NPR MASTER to enable the NPR master logic.

When the NPR master logic is enabled the following actions occur.

1. ADRS → BUS becomes true and gates the address register and the two extended address bits of the command register to the Unibus as BUS A00 – A17.

2. BUS C0 – C1 is gated to the Unibus. If a read operation is to occur, READ is true and BUS C0 – C1 are high. If a write operation is commanded, READ is false and BUS C0 – C1 are low.

3. If the transfer is a read operation, DATA → BUS is asserted and gates the character in the data buffer out to the Unibus.

4. Another output from the master logic undergoes a 150 ns delay (to allow for deskewing on the Unibus address lines) and then sets the MSYN logic circuit.

The MSYN logic asserts BUS MSYN to the slave device which then returns BUS SSYN to the TMB11. BUS SSYN becomes SSYN and is applied to the read and write termination circuits. If a read operation is being performed the read termination circuit asserts an input to the termination OR logic. If a write operation is being performed (READ false) the write termination circuit asserts DATA STB 1 which undergoes a 150 ns delay (for input data deskewing) and then becomes DATA STB 2. DATA STB 2 loads the data buffer with the input character that is to be written on tape. DATA STB 2 also asserts an input to the terminator OR logic. The asserted output of the OR logic is delayed 75 ns (for data deskewing into the data buffer) and then triggers the NPR clear logic.

The NPR clear logic asserts NPR CLR BBSY which resets the NPR request logic and increments the bus address register and the byte/record counter for the next character transfer. If a spacing operation is in progress the byte/record counter is incremented by LRCSD and no bus cycle is involved.

6.6.3.2 Bus Grant Late (BGL) and Nonexistent Memory (NXM) – When NPR ENB (1) is asserted the bus grant flip-flop is conditioned to set. If another NPR SET is asserted to the NPR request logic before the logic is reset, the bus grant late flip-flop will set asserting BGL (1) which in turn asserts BGL + NXM to the error logic.

If the MSYN logic is not reset within 20 μs after being set, NXM asserts and terminates the bus cycle by asserting the termination OR logic output. NXM also asserts BGL + NXM to the error logic.

6.6.3.3 BUS NPG OUT – An NPG from the processor is passed from one system device to another in daisy-chain fashion until it reaches the device that issued the BUS NPR. A BUS NPG IN received by the TMB11 is gated back to the Unibus as BUS NPG OUT under either of the following conditions:

1. NPR MASTER is true (TMB11 is presently bus master), or

2. NPR ENB is false (TMB11 did not issue the BUS NPR that caused the BUS NPG IN).
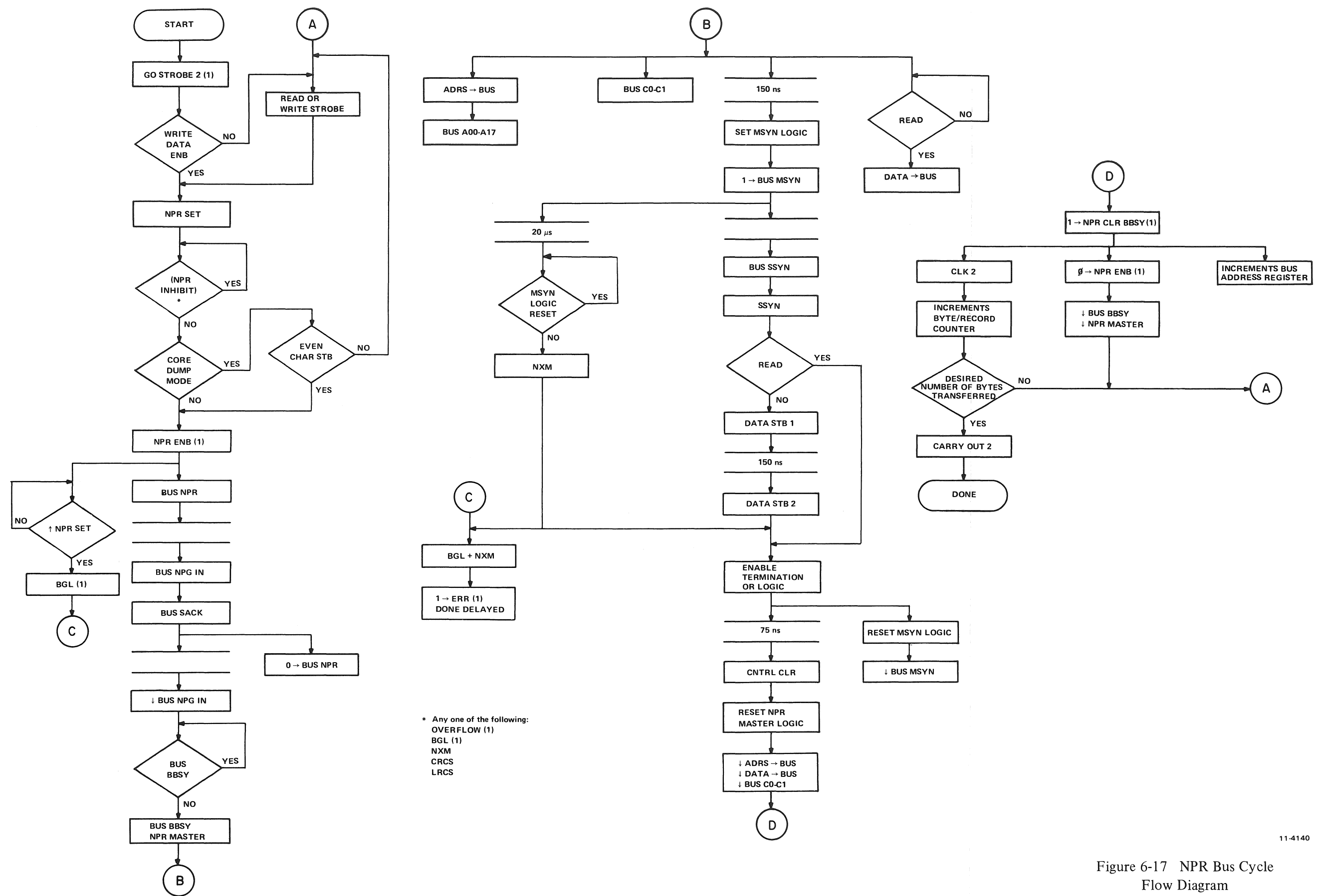
Figure 6-17 NPR Bus Cycle
Flow Diagram

Figure 6-18 NPR Bus Cycle
Block Diagram

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6.6.4 NPR Read (DATO)

6.6.4.1 Transport Strobe Processing (Figure 6-19) – Various strobes from the tape transport are used for a read function and in other functional areas of the TMB11. Many of the strobes are combined and/or modified before being used in the controller. This strobe processing is illustrated in a separate figure due to its common application to the TMB11 functions. Note the generation of READ STB. It is asserted by RDS when READ is true, however, the RDS strobe associated with the LRC character will not assert a READ STB pulse due to $\overline{LRCS}$ unless the LRC ENB bit is set in the read lines register.
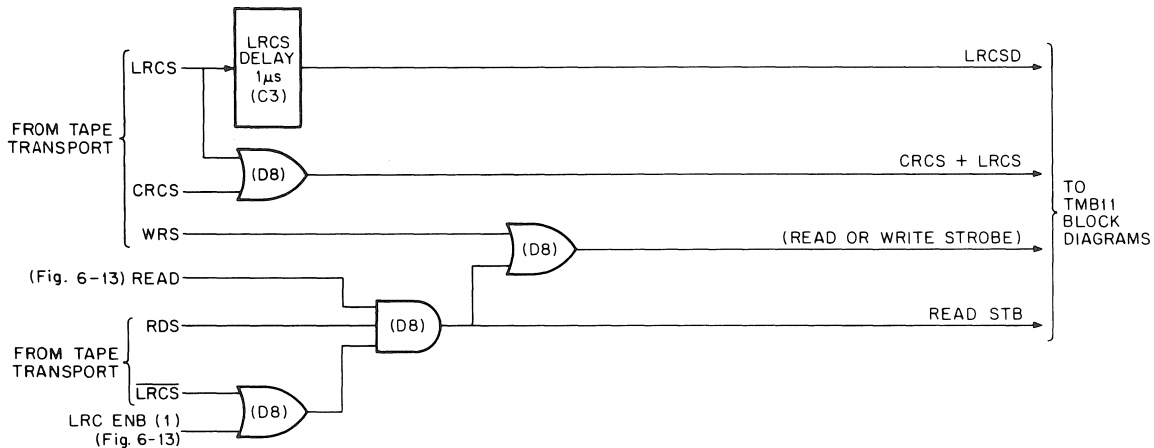
NOTE:
Designations in parenthesis refer to engineering drawings containing corresponding logic.

11-4128

Figure 6-19   Strobe Processing

6.6.4.2   9-Track and 7-Track Normal Operation (Figures 6-22 and 6-23) – When a character is received from the tape transport, READ STB asserts setting the select read flip-flop and causing SEL READ DATA to become true. In 9-track operation SEL READ DATA enables gates A, B, and C which respectively gate CHAN 0-3*, CHAN 4-5*, and CHAN 6-7* to become DATA BFR IN BIT 0-3, DATA BFR IN BIT 4-5, and DATA BFR IN BIT 6-7. The data buffer is divided into two halves with each half of the buffer loaded by a separate strobe. DATA BFR STB 1 loads buffer bits 0-3 and DATA BFR STB 2 loads buffer bits 4-7. The input READ STB asserts DATA BFR STB 1 (via the even character strobe logic) and DATA BFR STB 2 which load both halves of the data buffer and provide DATA BFR OUT BIT 0-7 to the high and low data byte gates. Table 6-5 summarizes the gating action associated with the data buffer.

DATA → BUS is asserted during the NPR bus cycle and enables either the high data byte gate or the low data byte gate according to the state of bit 00 in the current memory address register. When LO DATA BYTE is true the data buffer output is gated to the Unibus drivers as D BIT 00-07 and thence to the Unibus. On the next NPR bus cycle HI DATA BYTE becomes true and the buffer output is gated to the Unibus as D BIT 08-15.

---

*A channel reversal occurs in the input read amplifiers where RD7 – RD0 corresponds to CHAN 0 – CHAN 7 respectively.

The 7-track operation is identical to the 9-track operation except that the buffer input gate C is inhibited. (See Table 6-5.) Consequently CHAN 6-7 are not loaded into the data buffer and there is no data on buffer output lines DATA BFR OUT BIT 6-7, or on Unibus driver input lines D BIT 06-07 (low data byte) and D BIT 14-15 (high data byte).

Table 6-5   Data Multiplexing in 9-Track, 7-Track Normal, and Core Dump Modes

Mode of Operation		Enabled Gates	Channel Bits From Transport	DATA BFR OUT BITS – From Data Buffer	Number of Output Bits per Data Cycle
9-Channel		A	CHAN 0-3	0-3	
		B	CHAN 4-5	4-5	8
		C	CHAN 6-7	6-7	
7-Channel (Normal)		A	CHAN 0-3	0-3	
		B	CHAN 4-5	4-5	6
7-Channel (Core Dump)	First Cycle	A	CHAN 0-3	0-3	4
	Second Cycle	D	CHAN 0-3	4-7	4

6.6.4.3   Core Dump Operation (Figures 6-22 and 6-23) – Core dump operation can be implemented only in the 7-track mode, thus both 7 CH and CORE DUMP are true throughout this discussion.

When the first character is received from the transport, READ STB sets the select read flip-flop, SEL READ DATA becomes true, and gates A and D are enabled. CHAN 0-3 are passed through both gates to become DATA BFR IN BIT 0-3 and DATA BFR IN BIT 4-7 into the data buffer. The input READ STB asserts DATA BFR STB 1 (via the even character strobe logic) and DATA BFR STB 2 thereby loading both halves of the data buffer with the same character. The second character received from the transport triggers the same sequence except no read strobe is issued from the even character strobe logic and DATA BFR STB 1 is not asserted. DATA BFR STB 2 is asserted and loads bit 4-7 of the data buffer with the second tape character. (See Table 6-5.) The read strobe associated with the second character initiates an NPR bus cycle causing DATA → BUS to go true and gate the contents of the data buffer out to the Unibus. Thus, NPR bus cycles are initiated after each even numbered character is read from tape thereby allowing the two characters to be assembled into a byte in the data buffer before being gated out to the Unibus.

6.6.4.4   Processor Read (Figure 6-23) – During a processor read of the data buffer SEL 4 IN asserts both HI DATA BYTE and LO DATA BYTE. The latter gates the 7 bits of the data buffer to the Unibus while the former serves to gate D BIT 08 IN to D BIT 08 on the Unibus. During a processor read (NPR ENB false) D BIT 08 IN reflects the state of the parity flip-flop as determined by the parity bit of the LRC character.

6.6.4.5 Even Character Strobe Logic (Figure 6-20 and 6-21) – The even character strobe logic is enabled in the core dump mode and function to:

1. Suppress even numbered read strobes allowing read strobes no. 1, 3, 5, etc. as output; this is used to asssemble two tape characters into a data byte

2. Toggles EVEN CHAR STB L to disassemble an input data byte into two 4-bit data characters (write operation)

3. Enables an NPR bus cycle only on even numbered read strobes (or write strobes).

GO STROBE 2 L and INIT + GO L set the even character and strobe switch flip-flops. The first read strobe passes to the output through enabled gate D2. The same read strobe toggles the even character flip-flop to the reset state thereby conditioning the switch flip-flop to reset. The trailing edge of the first read strobe clocks the switch flip-flop to the reset state which inhibits gate D2. The second read strobe therefore does not appear in the output. It does toggle the even character flip-flop back to the set state thus conditioning the switch flip-flop to set. The trailing edge of the second read strobe sets the switch flip-flop thereby enabling gate D2 once again. The third read strobe will pass to the output through gate D2 and the cycle is repeated. The read strobes (or write strobes) toggle the even character flip-flop causing EVEN CHAR STB L to take on a square waveform. The timing diagram (Figure 6-21) illustrates the foregoing sequence.

When not in the core dump mode, EVEN CHAR STB L is held in a high state keeping the strobe switch flip-flop set thereby allowing all read strobes to pass to the output.
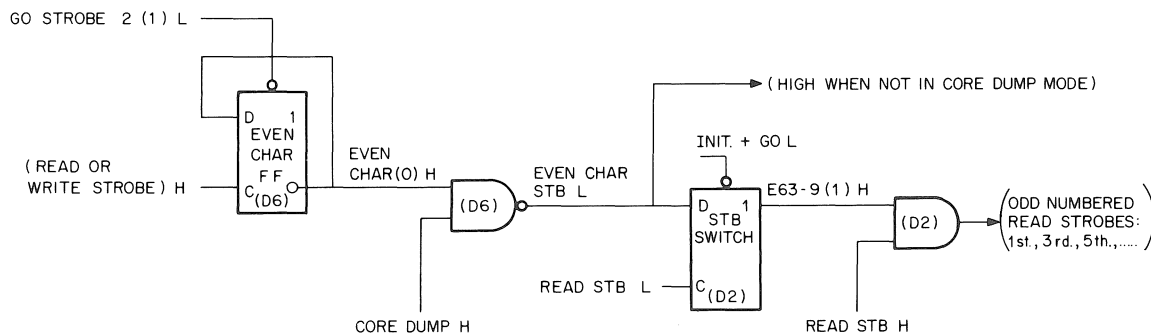
Figure 6-20   Even Character Strobe Logic Diagram

GO STROBE 2 L (O.S.)

EVEN CHAR (∅) H

EVEN CHAR STB L

EVEN CHAR STB H

RDS H

READ STB L

READ STB H

(READ OR WRITE STROBE) H

INIT + GO L

E 63 - 9 (1) H

NPR ENB (1) H

1 µs

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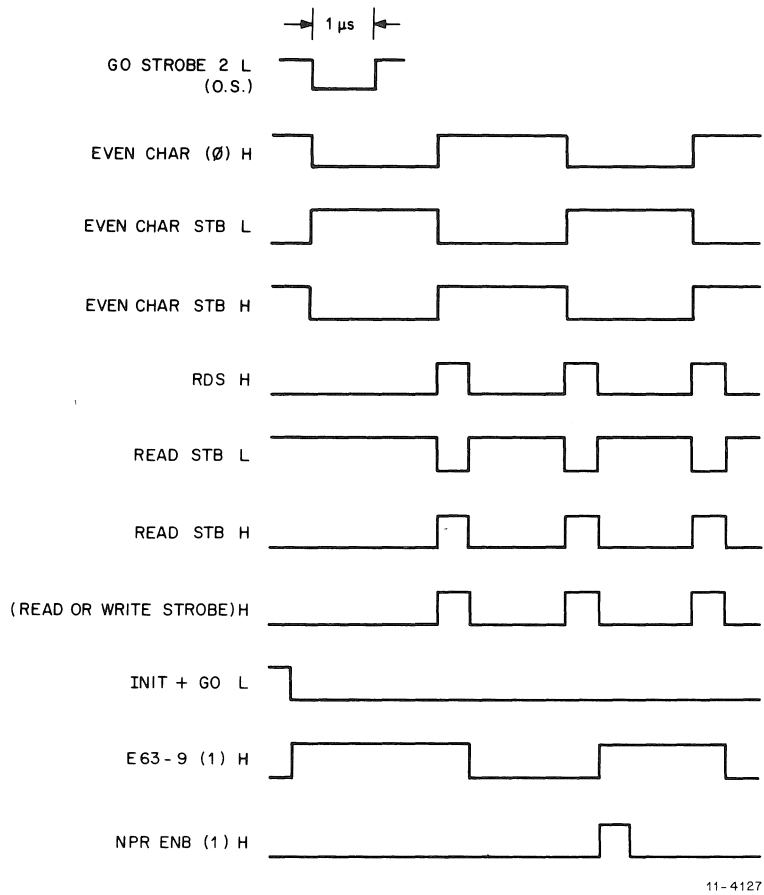
Figure 6-21   Even Character Strobe Timing Diagram

6-44
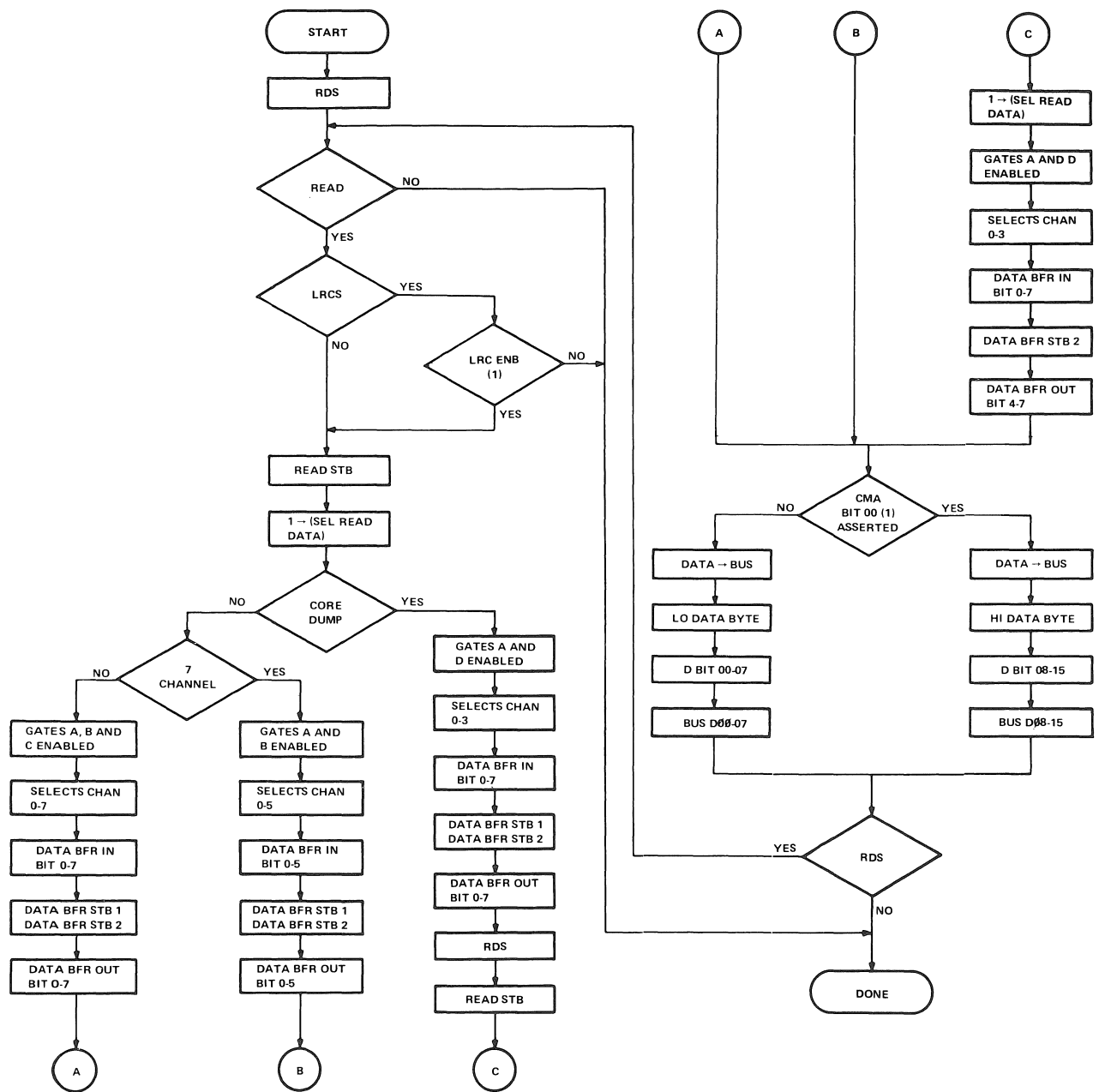
Figure 6-22   NPR Read (DATO) Flow Diagram
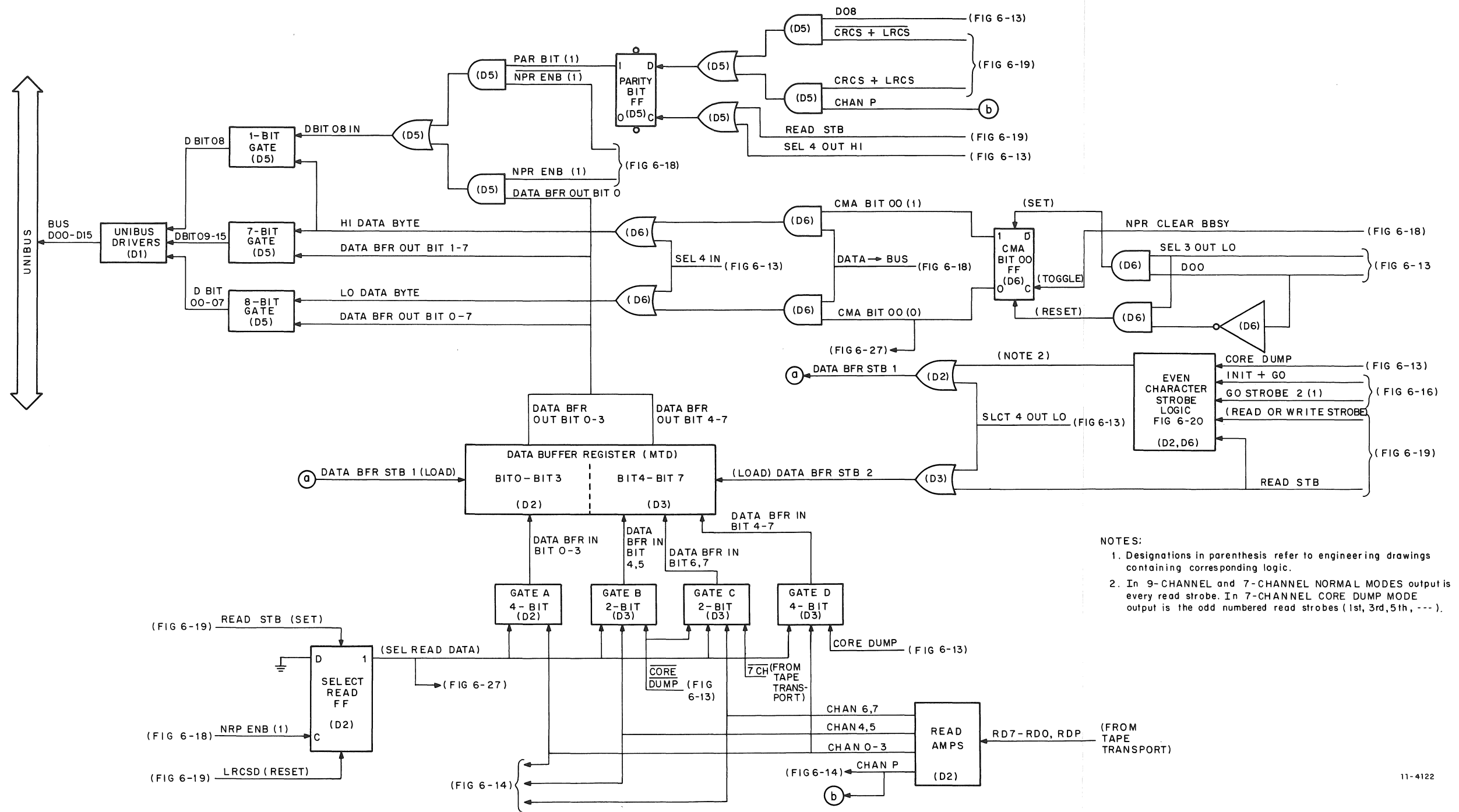
11-4143

Figure 6-23   NPR Read (DATO)
Block Diagram

11-4122

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6.6.5 NPR Write (DATI) (Figures 6-26 and 6-27)

6.6.5.1   9-Track and 7-Track Normal Operation – An NPR request must be made (NPR ENB true) before a write operation (READ false) can be initiated. With NPR ENB true and READ false either SEL LO BYTE WRITE DATA or SEL HI BYTE WRITE DATA asserts to gate respectively D00–D07 or D08–D15 from the Unibus to the input of the data buffer. The state of bit 00 in the current memory address register determines whether the high byte or the low byte is gated to the buffer. During the write NPR bus cycle DATA STB 2 is asserted (Paragraph 6.6.3.1) and asserts DATA BFR STB 1, 2 which loads the data buffer with the selected input byte. DATA BFR OUT BIT 0–7 is now available to gates A, B, C, and D. In 9-track operation gates B, C, and D are enabled gating DATA BFR OUT BIT 0–7 to the tape transport as WD7–WD0. (Note the reversal in the bit/track numbering sequence at the write gate outputs.) The 7-track normal write data sequence is identical to the 9-track sequence except that write gate D is inhibited. Thus DATA BFR OUT BIT 0–5 are gated to the transport as WD7–WD2. Table 6-6 summarizes the gating action for all modes of operation.

Table 6-6   Write Data Gating for 9-Track, 7-Track Normal and Core Dump Modes

Mode		Enabled Write Gates	DATA BFR OUT BITS – From Data Buffer	Write Data To Transport Register	Number of Input Bits per Data Cycle
9-Track		B C D	0–3 4–5 6–7	WD7–WD4 WD3–WD2 WD1–WD0	8
7-Track (Normal)		B C	0–3 4–5	WD7–WD4 WD3–WD2	6
7-Track (Core Dump)	First Cycle	B	0–3	WD7–WD4	4
	Second Cycle	A	4–7	WD7–WD4	4

6.6.5.2   Core Dump Operation – Core dump operation is identical to 9-track and 7-track normal operation with regard to the input gating and loading of the data buffer. The difference is that only write gates A and B are enabled and they are alternated by EVEN CHAR STB so when one gate is on the other is off. With CORE DUMP true, the even character strobe logic is enabled and EVEN CHAR STB is a square wave with its alternations switched by write strobes. (See Paragraph 6.6.4.5.)

A sequence is started by GO STROBE 2 (1) which sets EVEN CHAR STB to a high level and triggers the first NPR write bus cycle. DATA STB 2 asserts during the bus cycle asserting DATA BFR STB 1, 2 which loads the data byte into the buffer register. DATA BFR OUT BIT 0–3 is gated through gate B and passes into the tape transport as WD7–WD4. The first character is written on tape and the first write strobe is generated. The first write strobe sets EVEN CHAR STB to the low state thereby inhibiting gate B and enabling gate A which gates DATA BFR OUT BIT 4–7 to the transport as WD7–WD4 and the second character is written on tape. The low state of EVEN CHAR STB inhibits another NPR bus cycle. The second write strobe will set EVEN CHAR STB high enabling gate B once again and triggering the second NPR bus cycle. Thus, the even character strobe logic disassembles the input data byte into two 4-bit characters for the tape transport while inhibiting an NPR bus cycle on the odd numbered write strobes.

6.6.5.3 Processor Write – If a processor write is being executed, SEL READ DATA and NPR ENB (1) are false, thereby asserting SEL LO BYTE WRITE DATA and gating the low data byte from the Unibus to the buffer register. SLCT 4 OUT LO then asserts (Paragraph 6.6.1.1) in turn asserting DATA BFR STB 1, 2 which loads the buffer register with the input data.

6.6.5.4 Write Data Ready (Figures 6-24 and 6-25) – WDR to the tape transport must be true to enable the write logic within the transport. The write data ready logic supplies WDR to the transport, under the proper conditions, and assures a minimum record length of three characters in normal operation and four characters in core dump. Also during core dump, when OVERFLOW (1) occurs, indicating that the last character has been transferred to the controller, the logic holds WDR true for one more write strobe to allow the second half of the last data byte to be written on the tape.

WDR is asserted true by the third stage output of a 3-stage counter or by the asserted output of a 5-input AND gate. When a write operation is initiated GO STROBE 2 (1) L is asserted and resets the counter. The third stage output of the counter asserts WDR via the OR gate. OVERFLOW (1) H is false, thereby conditioning the first stage of the counter to set. The first three write strobes set the counter stages in order. The third write strobe sets the third stage causing its output to the OR gate to assert high; however, the AND gate is now enabled and holds WDR true. Note that WDR is held true for three write strobes regardless of the state of OVERFLOW (1) H.

When the desired number of characters have been transferred to tape, OVERFLOW (1) H goes true, conditioning the first stage of the counter to reset. The next WRS strobe resets the first stage inhibiting the AND gate causing WDR to go false. If CORE DUMP L is asserted the AND gate will not be inhibited until the next WRS strobe when the second stage is reset. Thus, in core dump mode WDR is held true for one more write strobe after OVERFLOW (1) H asserts.
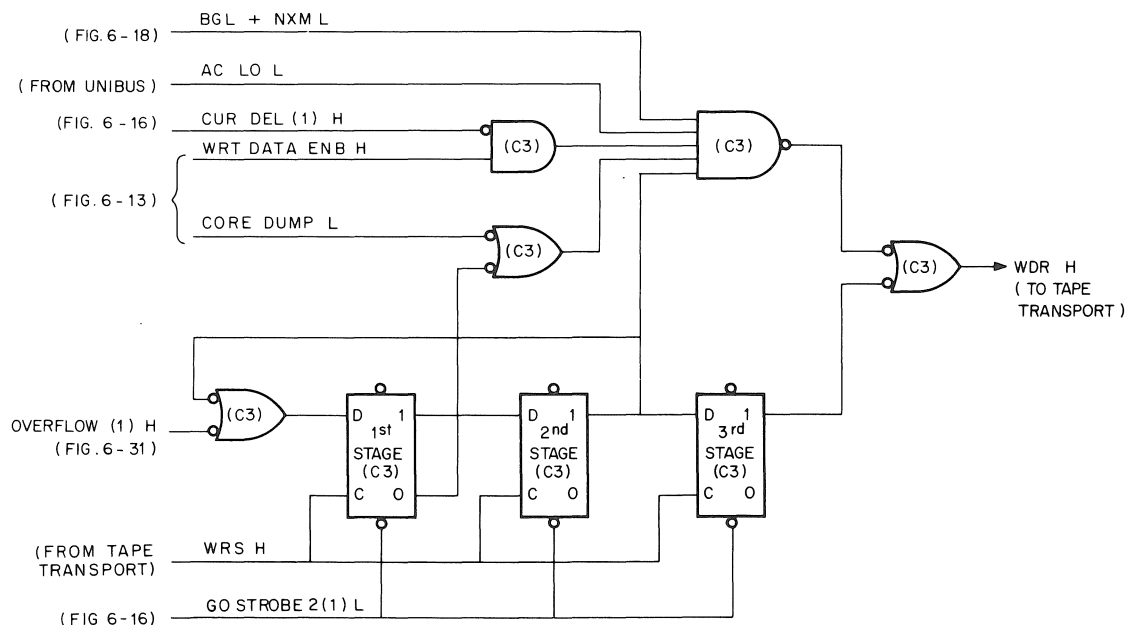
NOTE :
Designations in parenthesis refer to engineering drawings
containing corresponding logic.   11 - 4131

Figure 6-24   Write Data Ready Logic Diagram

6-50
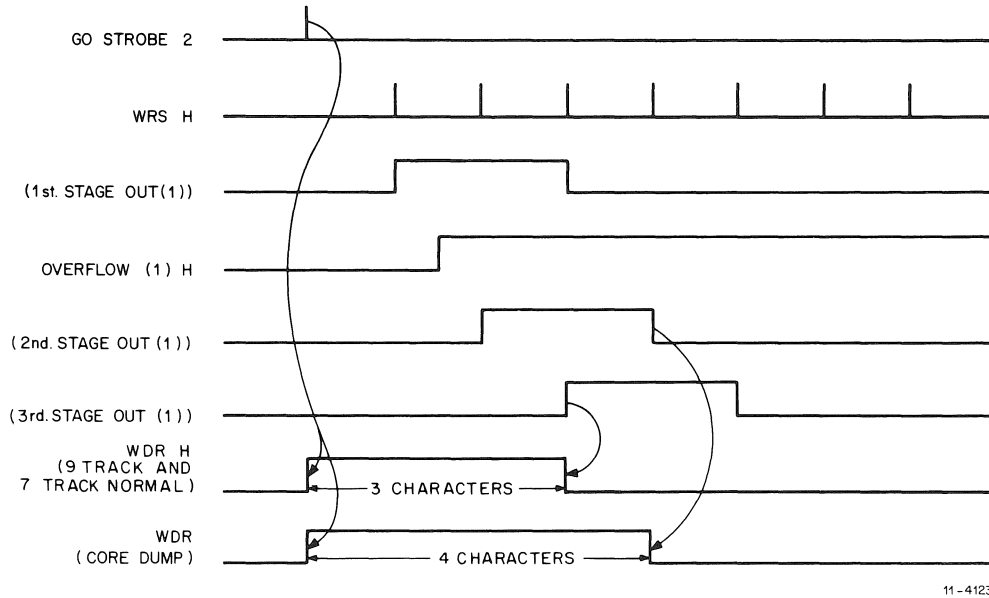
Figure 6-25   Write Data Ready Timing Diagram

Due to feedback from the second counter stage to the first, two write strobes must occur (to set the second stage) before the first stage can be reset. Consider the case where OVERFLOW (1) H asserts after the first or second write strobe (Figure 6-25). The first stage will reset on the third WRS which also sets the third stage. If, in core dump mode, the AND gate holds WDR true until the fourth WRS strobe which resets the second stage thereby negating WDR. Thus at least four write strobes are assured in core dump operation.
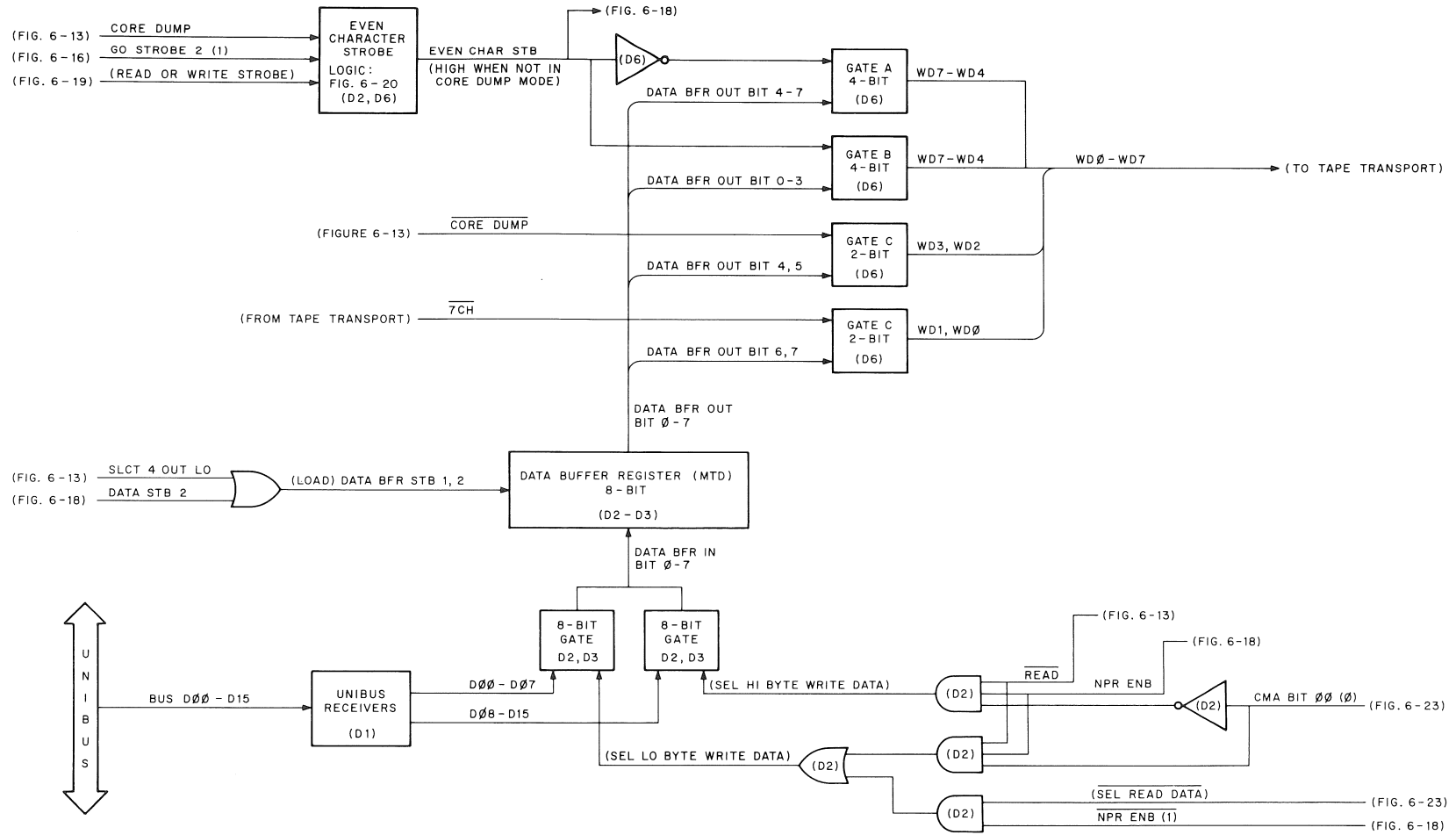
Figure 6-26   NPR Write (DATI)   Flow Diagram

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Figure 6-27 NPR Write (DATI) Block Diagram

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6.6.6 Done Logic (Figures 6-28 and 6-29)

The done flip-flop senses the completion of an operation and functions to assert control unit ready (for another command) and issue an interrupt request to the interrupt logic.

If a spacing operation was being executed CARRY OUT 2 signifies the completion of the operation by asserting when the desired number of records has been spaced over. If a read or write operation was being executed (SPACE false) the assertion of LRCSD signifies the operation is over.

In both cases the done flip-flop is set and DONE (1) is asserted. If ERR (1) asserts during the operation a done sequence will be triggered before the operation is completed. Certain errors will interrupt an operation by asserting ERR (1) as soon as they are detected. Other errors will allow the operation to terminate normally. (See Paragraph 6.6.7.)

When DONE (1) asserts and the tape transport comes to a stop (TUR true) DONE DELAYED (1) asserts in turn asserting (GET NEW CMD) to the bus interrupt logic and SET CUR to the operation start logic.

Some conditions that will assert DONE DELAYED (1) without waiting for TUR to come true are:

1. An illegal command [ILC (1)]
2. Reaching BOT during a space reverse operation
3. Reaching BOT during a rewind operation that was commanded by the processor
4. Deselecting the drive
5. When the transport starts a rewind from a local command.
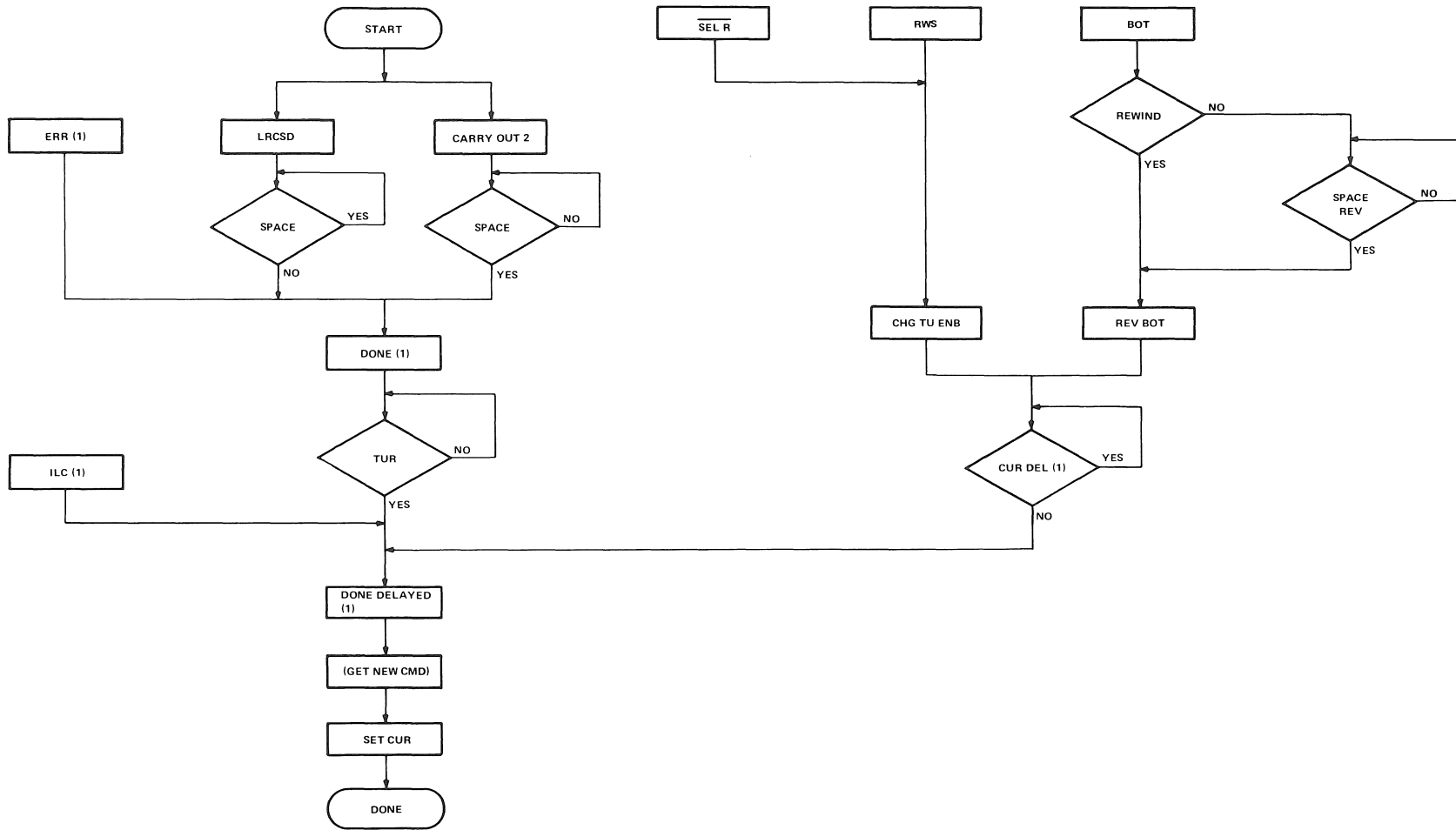
Figure 6-28   Operation Done Flow Diagram
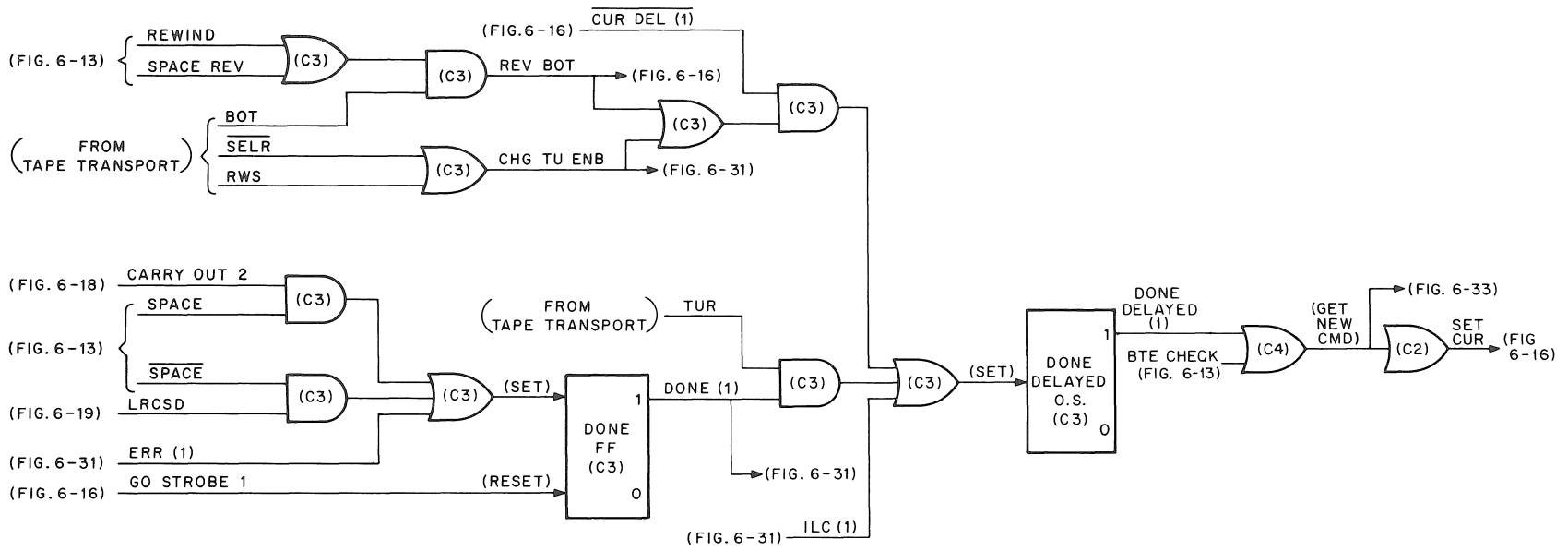
6-55

11-4142

NOTE
Designations in parenthesis refer to engineering drawings
containing corresponding logic.

11-4133

Figure 6-29   Operation Done Block Diagram

6.6.7 Error Logic (Figures 6-30 and 6-31)

ERR (1) is asserted by any of the error conditions that could arise within the system. When ERR (1) comes true it sets bit 15 in the command register and triggers a done sequence. The error conditions that assert ERR (1) are in two classes: those that assert ERR (1) immediately and abort the current operation, and those that allow the operation to terminate normally. In the latter case ERR (1) will become true with the assertion of LRCSD.

Errors that abort an operation are:
NXM
BGL
ILC
BTE

Errors that allow an operation to terminate normally are:
RLE
CRE
PAE
EOFF
End of Tape Error

NXM and BGL are error conditions that arise from the execution of an NPR bus cycle.

ILC is asserted under the following circumstances:

- When the processor attempts to access the command register while the controller is busy executing a command (SEL 1 OUT asserted while CUR DEL 1 is false).

- When an on-line transport is deselected while an operation is being executed (SELR negates while OFF LINE and CUR DEL 1 are false).

- The controller attempts to initiate an operation on a deselected transport (GO STROBE 2 (1) asserts while SELR is false).

- The controller attempts to initiate a write operation on a write protected transport (GO STROBE 2 (1) asserts while WRITE ENB and WRL are true).

BTE is asserted when a read strobe occurs during the gap shutdown or settle down periods provided no BGL, NXM, or ILC errors exist. (RDS asserts when either SDWN or GSD is true and the following are false: BGL, NXM, ILC.) Gap shutdown is the period between the end of a record and the beginning of the settle down interval (from the assertion of LRCS to the assertion of SDWN).

RLE (1) is asserted when a read strobe occurs after an overflow condition has been sensed except if the read strobe is a CRC or an LRC strobe (READ STB asserts when OVERFLOW (1) is true and CRCS + LRCS is false).

CRE (1) is asserted during a read or a write operation when a read strobe occurs and a CRC error exists. (RDS asserts while CRCE and READ + WRITE are true.)

PAE (1) is asserted during a read or a write operation when a read strobe occurs and either a vertical parity error or a longitudinal redundancy check error exists. (RDS asserts while either VPE or LRCE is true and READ + WRITE is true.)

EOFF (1) is asserted when a file mark (FMK) is received from the tape transport.

An end-of-tape error is asserted when the end-of-tape marker is sensed during a transport operation other than rewind or space reverse (EOT asserts when REWIND and SPACE REV are false).
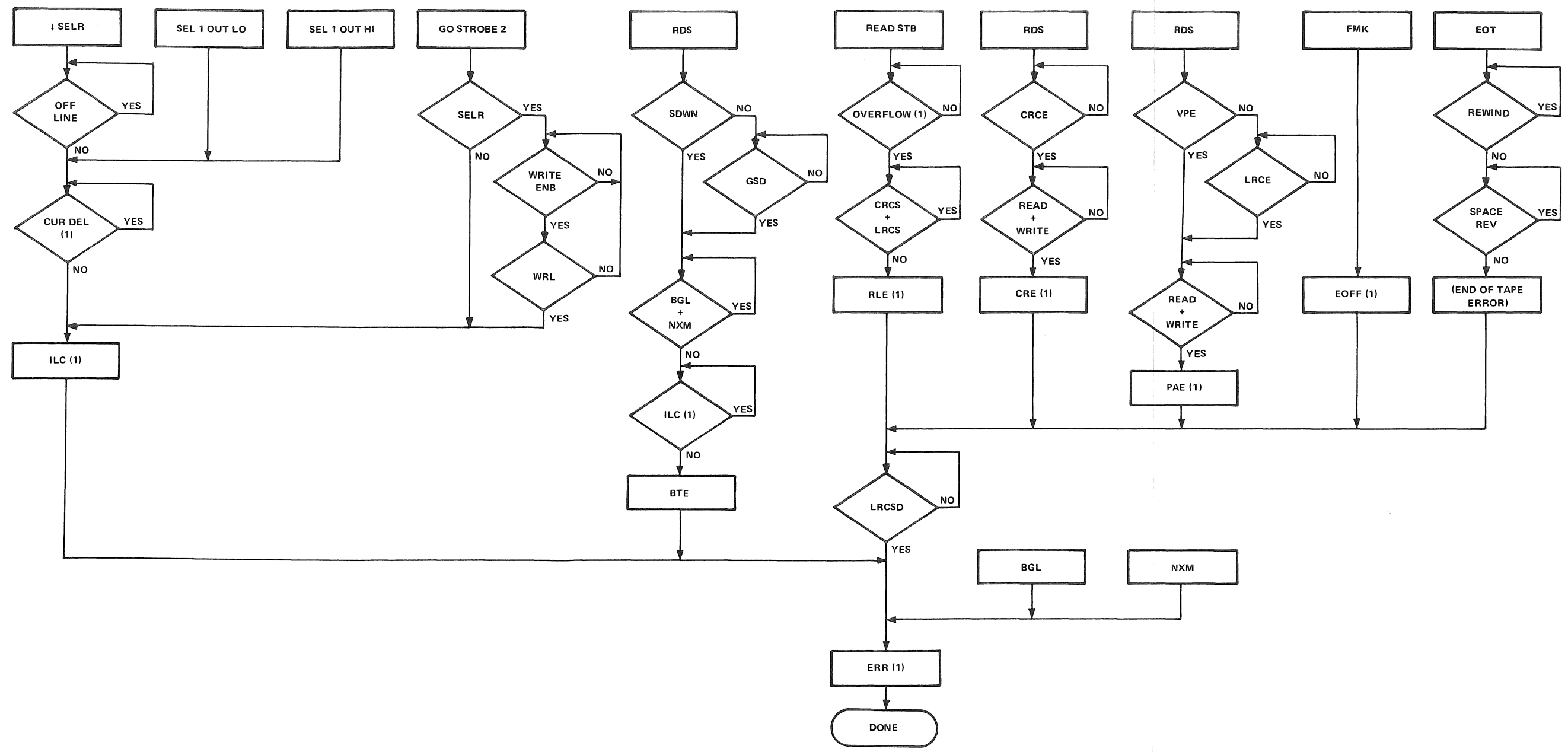
Figure 6-30 Error Sequence Flow Diagram
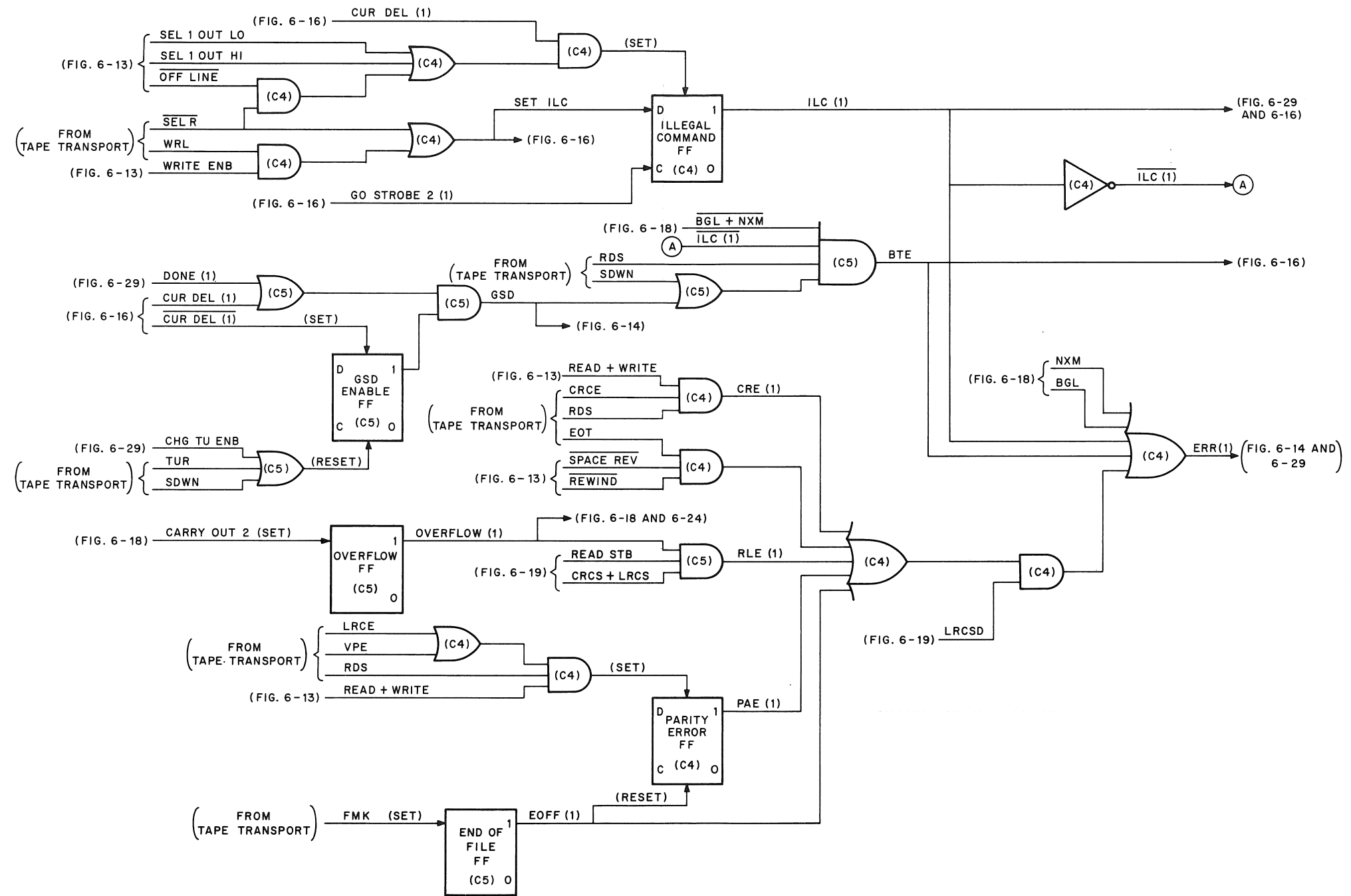
11-4137

Figure 6-31   Error Sequence Block Diagram

NOTE

Designations in parenthesis refer to engineering drawings containing corresponding logic.

11-4135

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6.6.8 Interrupt Bus Cycle (Figures 6-32 and 6-33)

An interrupt bus cycle is initiated if the interrupt enable bit (bit 06) in the command register is set and any one of the following occurs:

1. GET NEW CMD asserts from the done logic.

2. The tape comes to a stop (TUR asserts) after a rewind operation.

3. The processor requests an interrupt.

The setting of the BR interrupt flip-flop starts the interrupt sequence. The flip-flop is set via a gate enabled by INT ENB (1) from the command register. The other gate input comes from the set interrupt one-shot or from the processor. The set interrupt one-shot is triggered by GET NEW CMD from the done logic (if an interrupt bus cycle is not already in progress) or when the tape transport stops (TUR asserts) after a rewind operation (BOT is reached when CU READY and RWS are true). The processor initiated interrupt is accomplished by the processor asserting SLCT 1 OUT LO and D00 after it has set the interrupt enable bit in the command register.

NOTE
Processor initiation of an interrupt is done for special software purposes and is not a normal occurrence of tape system operation.

When the BR interrupt flip-flop is set, BR INT (1) asserts enabling the Unibus request logic. The Unibus request logic asserts BR OUT which becomes BUS BRX to the Unibus. The value of X is determined by the priority jumpers and may be 4, 5, 6, or 7 (usually 5). The processor responds to the bus request with BUS BGX IN which becomes BG IN and enables the Unibus acquisition logic. The Unibus acquisition logic asserts BUS SACK to the processor which responds by negating BUS BGX IN. The acquisition logic checks for BUS BBSY (by some other device) and if it finds the bus free asserts BUS BBSY to the Unibus (indicating bus mastership) and BR MASTER to the interrupt circuits. BR MASTER becomes BUS INTR and is placed on the Unibus along with BUS D02-D08, thereby commanding the processor to initiate an interrupt routine starting at the address specified by BUS D02-D08 (address = 224). Processor acceptance of this data is indicated by its assertion of BUS SSYN to the TMB11. BUS SSYN becomes SSYN and triggers the interrupt done logic. The interrupt done logic asserts INT DONE B which completes the interrupt bus cycle by resetting the interrupt flip-flop and acquisition circuits.

6.6.8.1 BUS BGX OUT

A BUS BGX IN from the processor is passed from one system device to another in daisy-chain fashion until it reaches the device that issued the BUS BRX. A BUS BGX IN received by the TMB11 is gated back to the Unibus as BUS BGX OUT if the controller is not making an NPR bus request (BUS NPR false) (NPR requests take priority over all BR requests) and one of the following conditions exist:

1. BR MASTER is true (TMB11 is presently bus master).

2. BR INT (1) is false (TMB11 did not issue the BUS BRX that caused the BUS BGX IN).
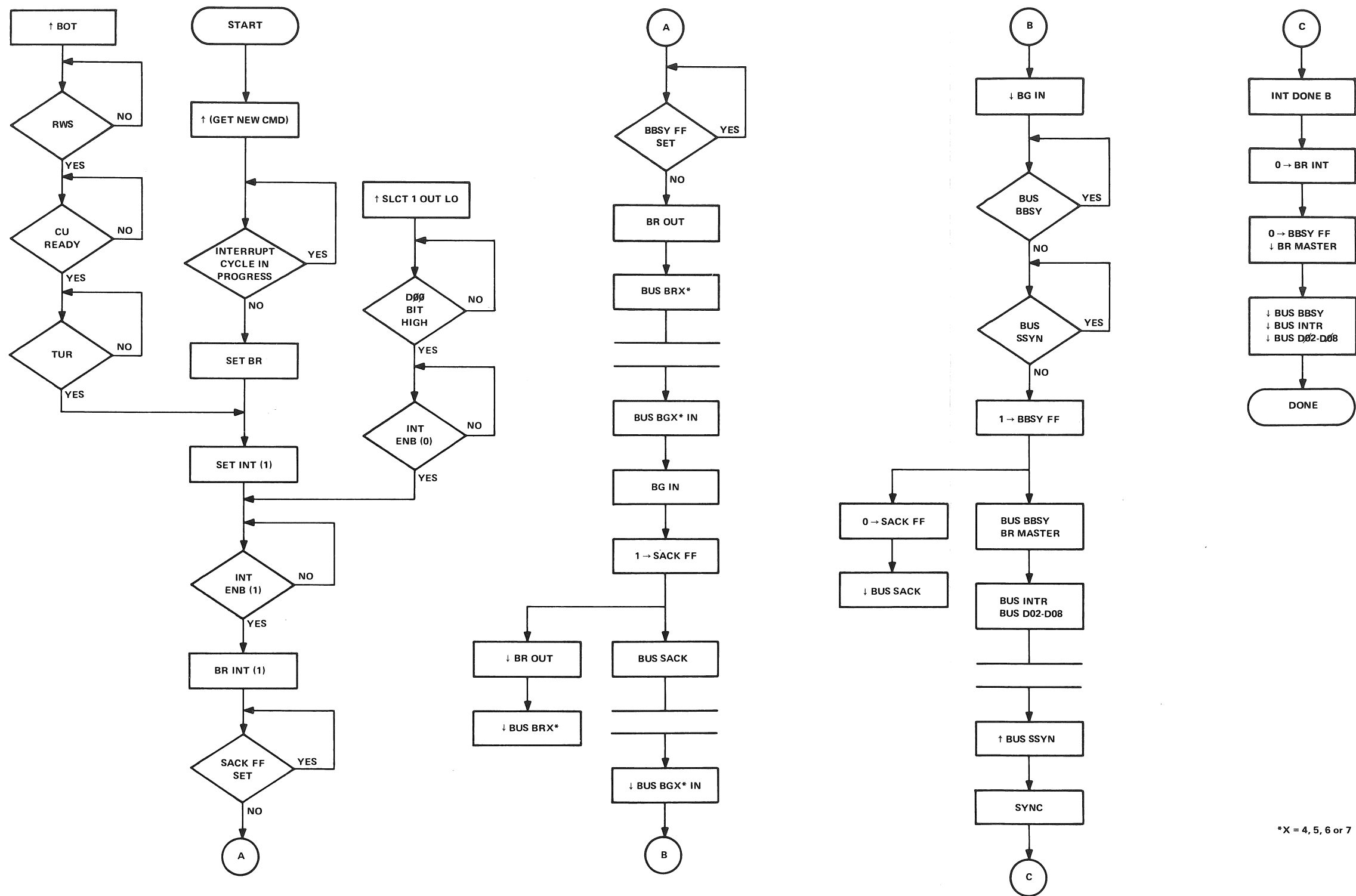
Figure 6-32 Interrupt Bus Cycle
Flow Diagram

*X = 4, 5, 6 or 7

11-4138

6-63

Figure 6-33 Interrupt Bus Cycle
Block Diagram

NOTE
Designations in parenthesis refer to engineering drawings
containing corresponding logic.

* X = 4,5,6 or 7.

11-4130

6-64

6.6.9 Timing Diagrams

Timing diagrams of various tape operations are shown in Figures 6-34 through 6-41. These diagrams portray specific tape operations such as reading a record of three data characters, reading a record of two tape characters in the core dump mode, etc. The purpose of these diagrams is to illustrate overall TMB11 operation as described in previous paragraphs.
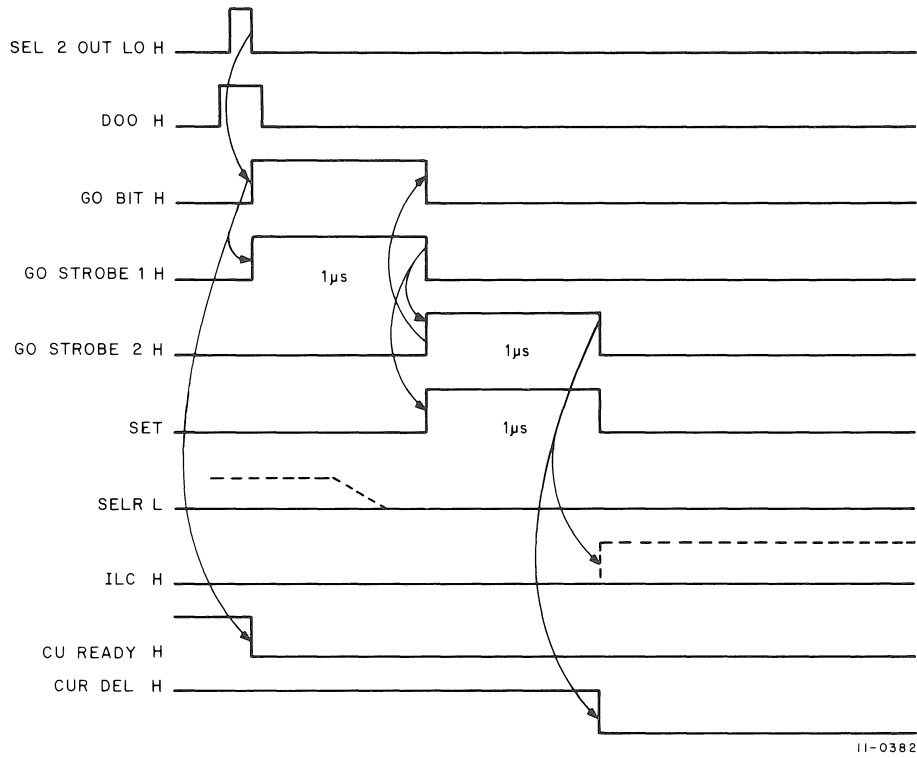
Figure 6-34 Start of Tape Operation
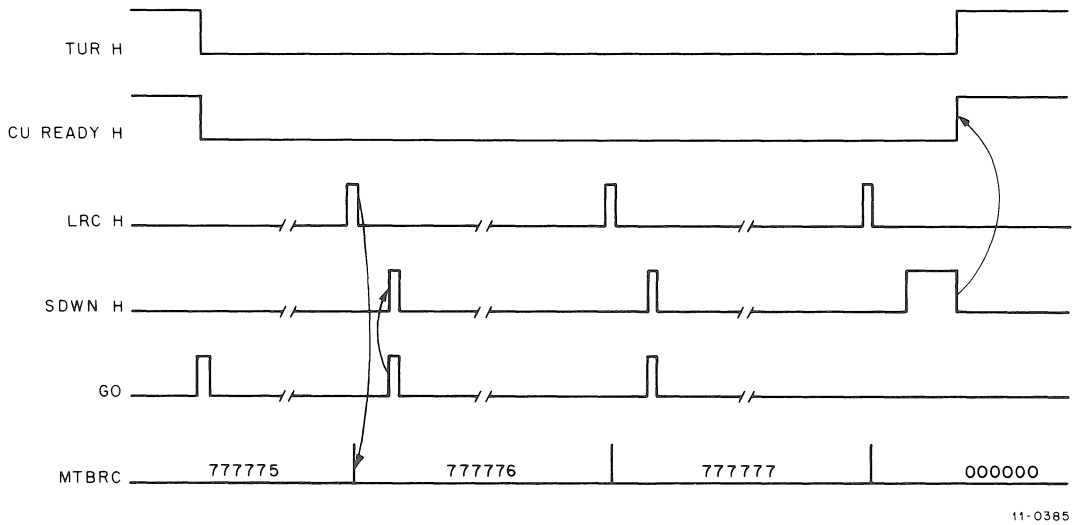
Figure 6-35 Spacing Forward Three Records
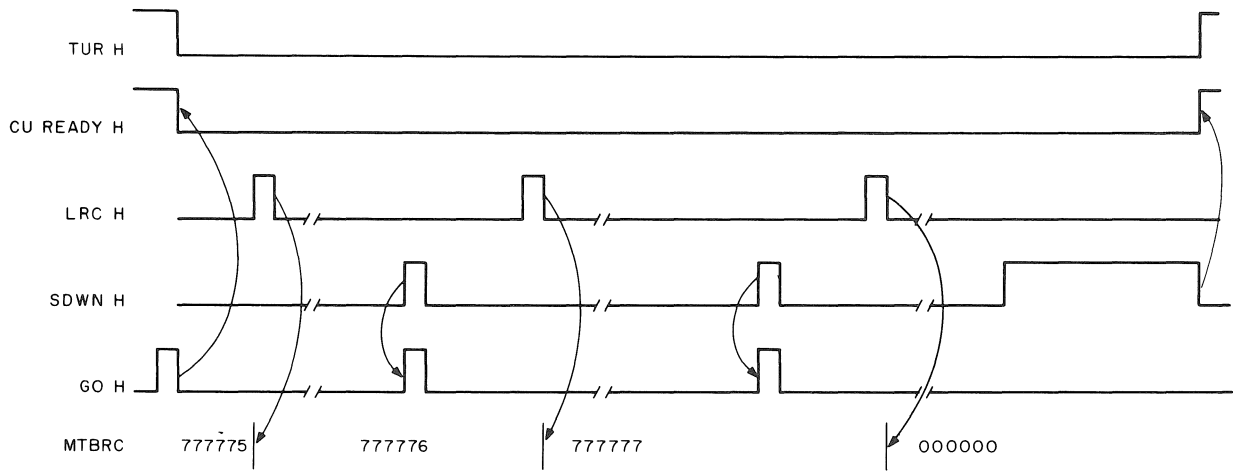
Figure 6-36 Spacing Reverse Three Records
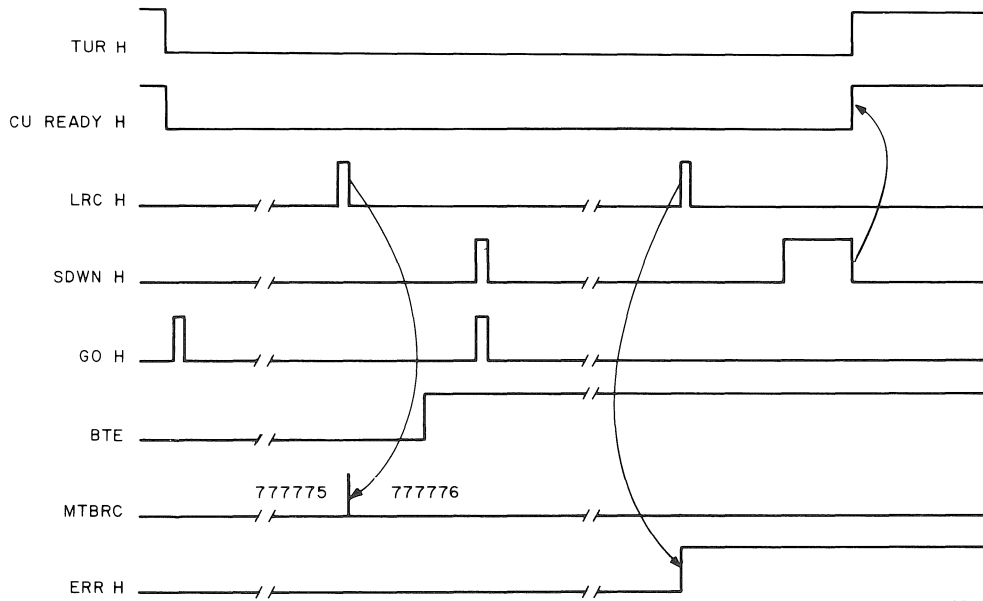
Figure 6-37 Spacing Forward Three Records, Bad Tape Error Appearing in First Record
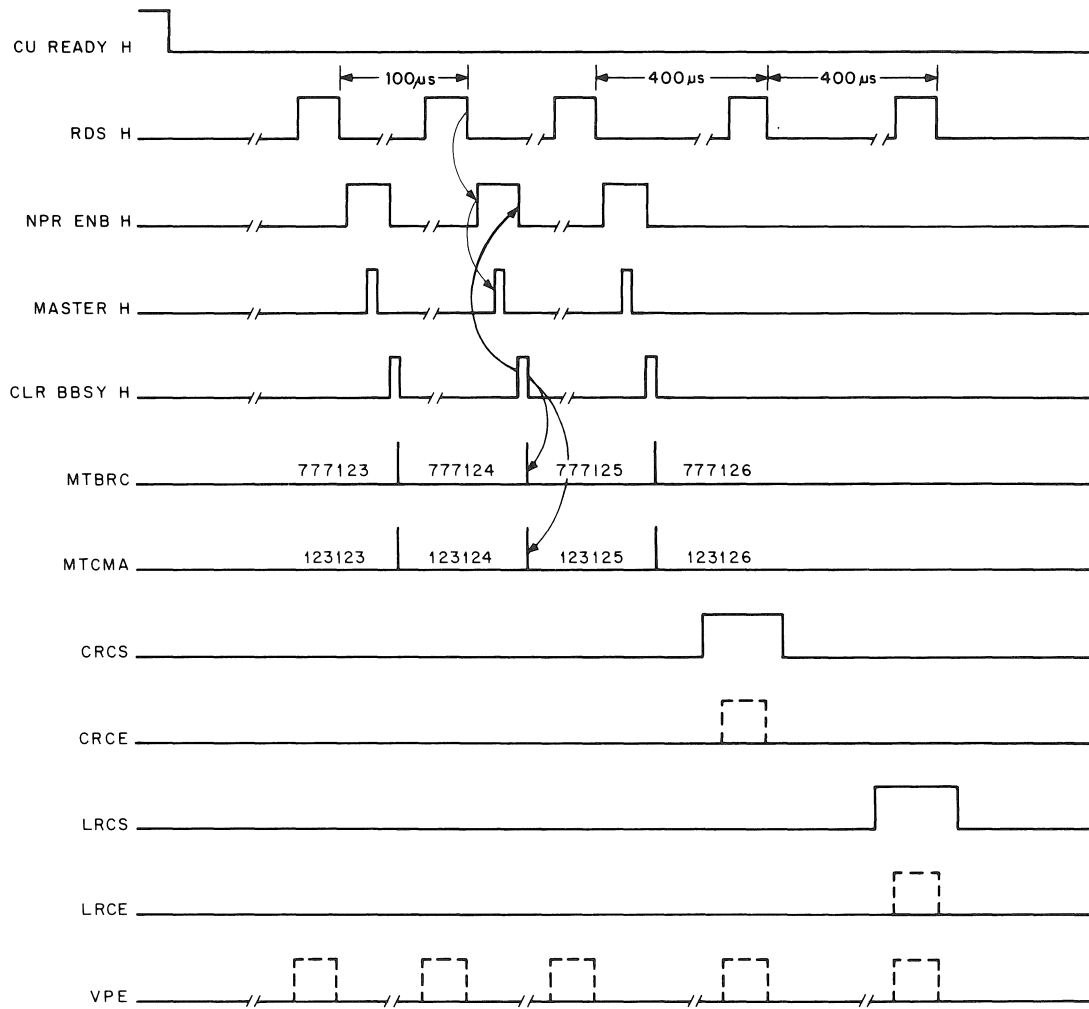
Figure 6-38   Reading Record of Three Data Characters
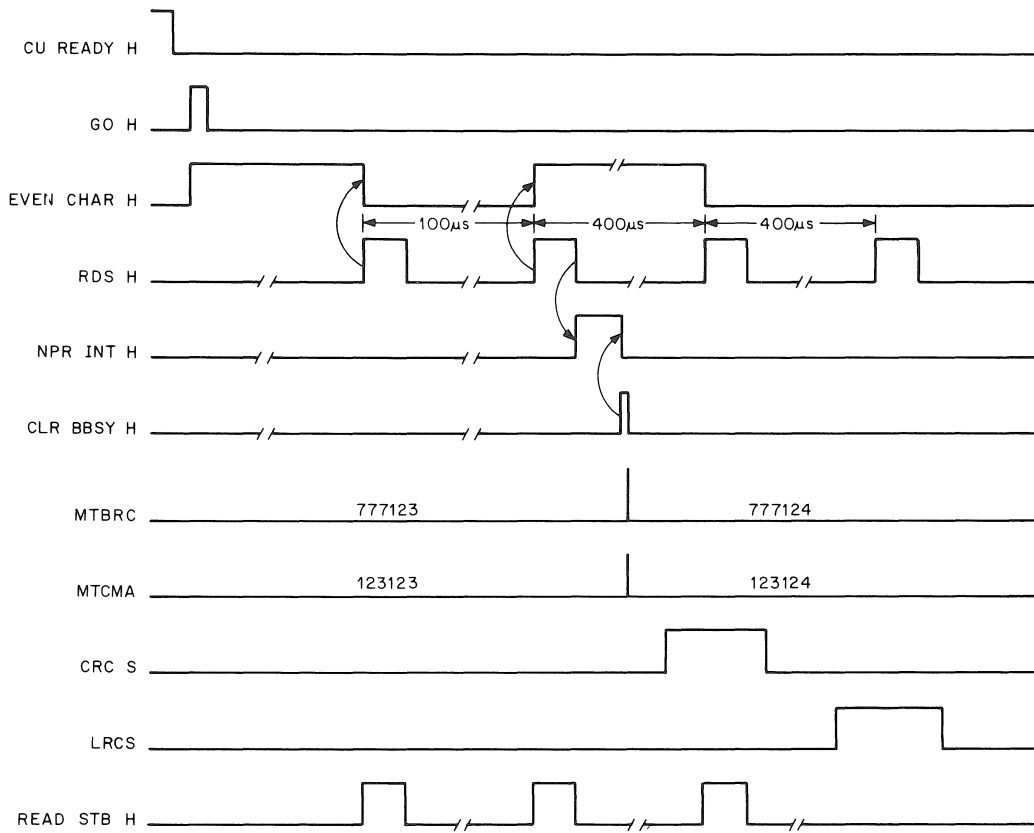
11-0383

Figure 6-39   Reading Record of Two Tape Characters in Core Dump Mode
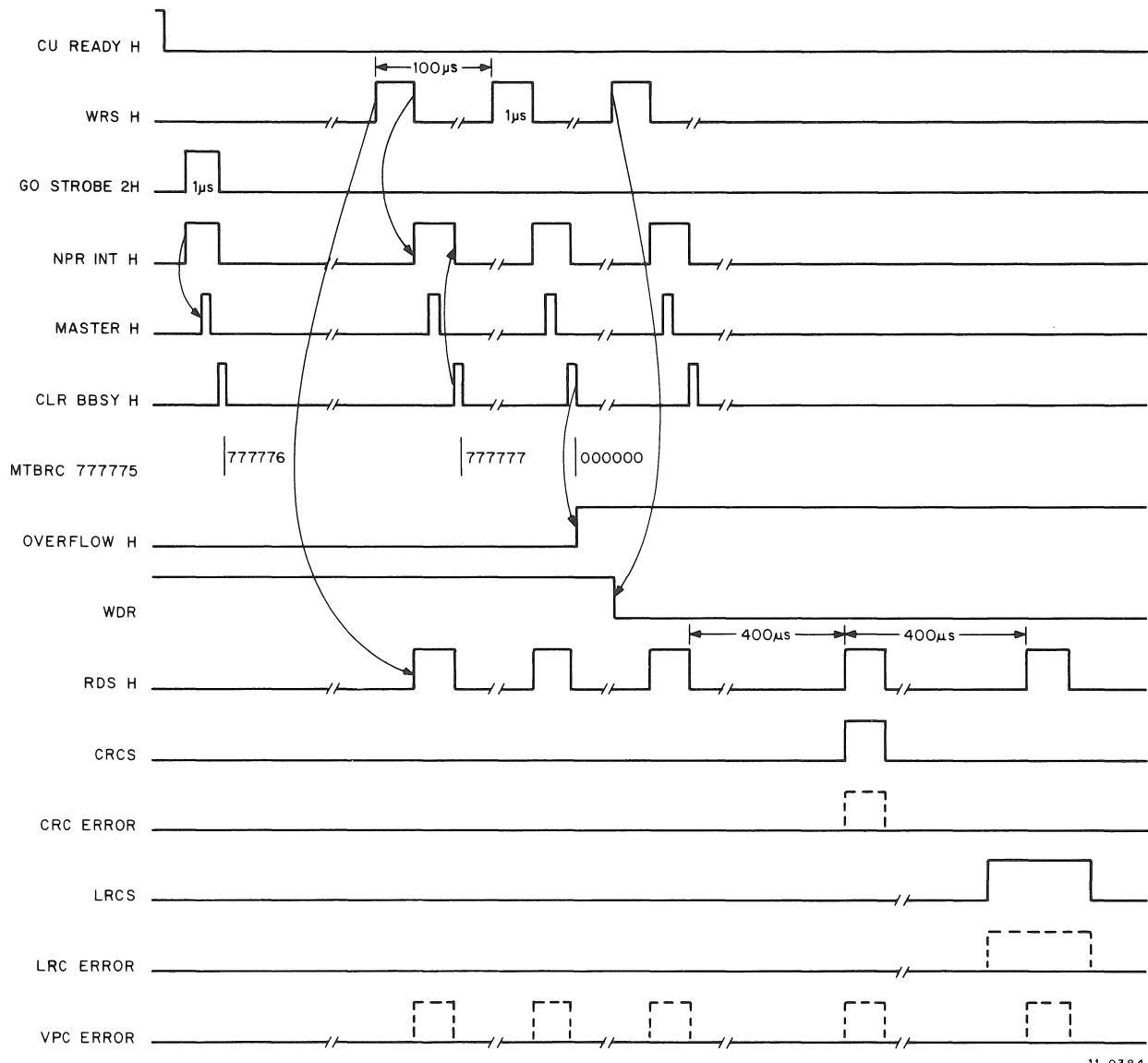
Figure 6-40   Writing Record of Three Data Characters

Figure 6-41   Writing Record of Two Tape Characters in Core Dump Mode

11-3993

CHAPTER 7
M8926 THEORY OF OPERATION

7.1 GENERAL (Figures 7-1, 7-2, and 7-3)

Figure 7-1 is a simplified flow diagram of the M8926 Interface board. The CSET command from the controller triggers a drive start-up sequence. The start-up sequence signals the drive to start the capstan motor and introduces a delay period for the capstan motor to get up to speed [1.14 m/second (45 inches/second)] before enabling a read or write sequence.

All commands from the controller except rewind will cause a read sequence to occur. The read sequence transfers data from the drive to the M8926 board. A write command (CWRE) must be asserted by the controller to enable a write sequence. If a write command is asserted by the controller, data is transferred from the controller to the drive to be written on tape (write sequence). The data written on tape is then read back via the read sequence. This read-after-write feature allows the recorded data to be checked for errors by the M8926 board. The read-after-write data is made available to the controller where it can be accessed by the processor for maintenance purposes. During normal operation, read data is not accepted by the controller unless a read command is asserted.

When the read circuits detect the end of the record, a drive stop sequence is triggered. The stop sequence signals the drive to stop the capstan motor and initiates another delay period. The delay allows the capstan motor to slow down to a stop before the command operation is terminated.

The M8926 detailed flow diagram (Figure 7-2) provides a more detailed functional description of the M8926 Interface board. This diagram should be read in its entirety while referencing the functional block diagram, Figure 7-3. Subsequent sections in this chapter treat the M8926 board according to the functional divisions shown in Figures 7-1, 7-2, and 7-3:

1. Status/Command Logic
2. Drive Start-Up
3. Write Sequence
4. Read Sequence
5. Drive Stop

It will be helpful to reference Figures 7-2 and 7-3 as an overview while reading through Chapter 7.

NOTE

The block diagrams that follow use logical AND and OR symbols. It does not necessarily follow that a corresponding gate exists on the controller logic prints. The assertion of inputs A and B that cause the assertion of output C may be represented on a block diagram by a single AND gate, yet the engineering drawing may show that several circuit stages are involved in the ANDing operation.

The signal names used on the functional block diagrams are the names used on the engineering circuit schematics (CS prints). Where other signal names or notes are used, they are enclosed in parentheses.

11-4780

Figure 7-1   M8926 Simplified Flow Diagram

7-2

START

CSET

SET

MOTION CONTROL LOGIC (Drive up to speed):
1. Negates STOP(SB) and asserts EMD(SB) and SLAVE SET PLS(SB) to drive.
2. Loads start-up time from the read channels
   (and CWXG or EWFMK if asserted)
   into motion delay counter.
3. Allows CLOCK(SB) to clock motion delay counter.
4. When counter counts out delay period, counting stops and:
   A. ACCL(SB) negates gating WRT CLK(SB) from drive to M8926
   B. READING asserts enabling read channels.

Latch up commands
to Drive

READING

↓ ACCL(SB)

READ LOGIC:
1. Transfers data characters and read strobes
   from tape transport to controller.
2. Checks for vertical parity errors.
3. Detects file mark if present.
4. Detects end of record.

WRT CLK(SB)

CWRE — NO / YES

END OF RECORD — NO / YES

End of record logic:
1. Generates CRCS and LRCS for controller.
2. Checks for CRC and LRC errors.
3. Generates read strobes (CRDS) for CRC and LRC characters.
4. Initiates end of record decision delay.
5. Asserts RD CLR PLS after decision delay to initiate
   drive stop sequence.

WRITE LOGIC:
1. Transfers data characters from controller to tape transport.
2. Generates vertical parity bit for each character.
3. Generates CWRS pulses for controller.
4. Generates REC(SB) pulses for tape transport.
5. Generates CRC character.
6. Generates file mark character if WFMK command asserted.

RD CLR PLS

CWDR — YES / NO

MOTION CONTROL LOGIC (Drive stop)
1. Asserts EMD(SB) to drive.
2. Negates READING thus inhibiting read channels.
3. Loads stopping time into motion delay counter
   via read channels.
4. Allows CLOCK(SB) to clock motion delay counter.
5. When counter counts out delay period, counting stops and:
   A. ACCL(SB) asserts inhibiting WRT CLK(SB) from drive to M8926
   B. MOVE negates.

Write end of record:
1. Transfers CRC character to tape transport.
2. Generates REC(SB) pulses for CRC and LRC characters.
3. Generates LRC STRB(SB) for tape transport.

↓ MOVE

M8926 general reset.
STOP(SB) asserted to drive.

DONE

11-4777

Figure 7-2   M8926 Detailed Flow Diagram

7-3

Figure 7-3 M8926 Block Diagram

7.2 STATUS/COMMAND LOGIC (Figures 7-5 and 7-6)

7.2.1 Command Logic

Some operational commands are coupled from the controller to the drive via passive logic circuits. Other commands that must stay asserted during the entire operation are latched up in flip-flops set by CSET from the controller. Note the conversion of CDEN5 to DEN0 (SB) and CDEN8 to DEN1 (SB) during the latch-up process.

CSEL0–CSEL2 select a slave unit via a 3-bit code. The 3-bit code is latched up in the slave select latch-up flip-flops which output SS0 (SB) – SS2 (SB) to the drive. The input code from the controller is compared to the output code in the slave select comparator. If the two codes do not match, the latch-up flip-flops are clocked, forcing SS0 (SB) – SS2 (SB) to agree with the select code from the controller. An AND gate must be enabled by MOVE before clocking of the flip-flops can occur. MOVE is asserted true during every command operation except rewind. Thus a new slave drive cannot be selected during a read, write, or spacing operation. Note that a bit reversal takes place in the latch-up flip-flops where the CSEL0, 1, and 2 input bits become bits SS2 (SB), 1, and 0, respectively, in the output.

Figure 7-6 shows four signal lines coupling fixed potentials to the host drive. These signal lines are not used but the host drive requires that the lines be held at a fixed voltage level. Three of the lines [DRV CLR PLS (SB), INIT PLS (SB), 1 RD (SB)] are tied to +3 V and the fourth (SLAVE BUS ENBL) is tied to ground.

7.2.2 Status Logic

Some status signals are directly coupled from the drive to the controller while others such as RWS (SB) and MOL (SB) undergo conditional gating. Rewind status, RWS (SB), from the drive negates at the end of SDWN (SB) simultaneously with the assertion of TUR (SB) (Figure 7-4). A timing requirement within the controller demands that CRWS negate before CTUR asserts. This requirement is met by ANDing RWS (SB) with SDWN DELAYED, thus producing the proper CRWS timing as shown in Figure 7-4. SDWN is delayed approximately 100 ns, producing SDWN DELAYED, before being ANDed with RWS (SB). This is done to eliminate the possibility of a spurious assertion of CRWS should SDWN (SB) negate while RWS is still true.
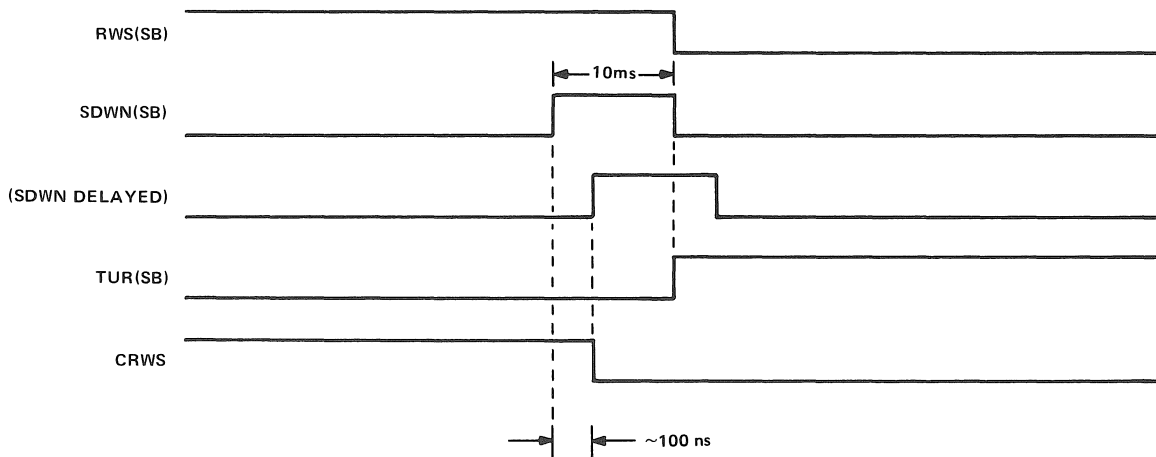
11-4779

Figure 7-4   RWS (SB) and CRWS Timing Diagram

CSELR is negated for 1 μs while a new drive is being selected by the slave select logic. This is accomplished by the gating of MOL (SB) with the 0 output of the slave select one-shot. The 1 μs delay allows settling of the select code before CSELR is asserted for the new drive.

When a 7-track drive is being used, 7CH (SB) is asserted from the drive, causing the assertion of C7CH to the controller and R7CH to the 7TRK flip-flop. When SET asserts, 7TRK becomes true to indicate the presence of a 7-track slave drive to the M8926 board. Note that the assertion of EDEN5 will also cause 7TRK to become true at SET time. Compatibility between the TU10 and TU10W drives requires that both EDEN5 and R7CH cause the assertion of 7TRK at SET pulse time.

```
                              ┌─────────────┐
                             ( START        )
                              └──────┬──────┘
                              ┌──────┴──────┐
                              │    CSET     │
                              └──────┬──────┘
                              ┌──────┴──────┐
                              │    SET      │
                              └──────┬──────┘
```

START

CSET

SET

CWRE — NO / YES

WRITING (WRITE FLOW)

WRITE(SB)

CWFMK — NO / YES

EWFMK (WRITE FLOW)

R7CH — NO / YES

CDEN5 — NO / YES

EDEN5

DEN0(SB)

7 TRK (WRITE AND READ FLOWS)

CDEN8 — NO / YES

DEN1(SB)

CPEVN — NO / YES

EPEVN

CFWD — NO / YES

(FILE MARK CHARACTER) (READ FLOW)

EFOR (READ FLOW)

FWD(SB)

(FIG. 7-8)

11-4778
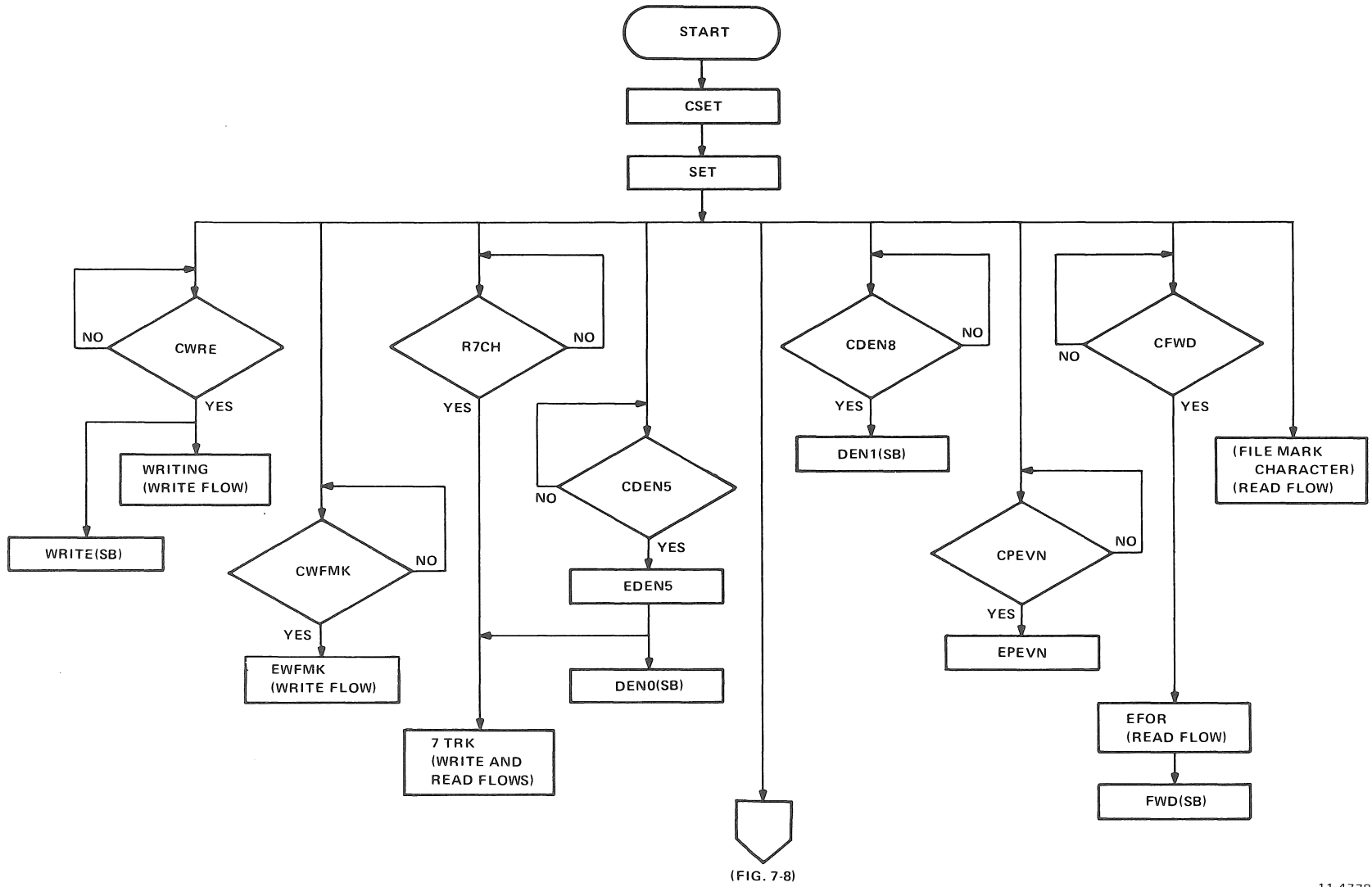
Figure 7-5   Command Latch-Up Flow Diagram

A. STATUS

CBOT (3) BOT(SB)

CEOT (3) END PT(SB)

CWRL (2) WRL(SB)

CTUR (2) TUR(SB)

TO CONTROLLER

FROM TAPE DRIVE

CRWS (2) (SDWN DELAYED) DELAY (2) (SDWN) (2) RWS (SB)

CSDWN (2) SDWN(SB)

CSELR (2) (A) MOL(SB)

C7CH (2) R7CH (2) 7CH(SB)

(FIGURES 7-12, 7-14 AND 7-21) 7TRK D 7 TRK FF (4) C (4) EDEN5 (B) SET (C)

A. STATUS

11-4795

B. COMMAND

+3V O DRV CLR PLS(SB)

INIT PLS(SB)

IRD(SB)

SLAVE BUS ENBL

TO HOST DRIVE

CSEL2–CSEL0 SLAVE SELECT LATCH UP FF (2) SS0(SB)–SS2(SB)

(CLOCK)

(FIG 7-9) MOVE (A≠B) (2) SLAVE SELECT O.S. (2) 1

A SLAVE SELECT COMPARATOR B (2) 0 (A)

CREV (1) REV (SB)

CRWD (1) RWND(SB)

CINIT (HOST DRIVE) PCLR (2) MASTER CLEAR (GENERAL DRIVE RESET)

FROM CONTROLLER

TO TAPE DRIVE

CWRE WRITE(SB)

CFWD COMMAND LATCH UP FFS (1) EFOR (1) FWD(SB)

(FIG 7-14)

CWFMK EWFMK (FIG 7-9 AND 7-12)

CPEVN EPEVN (FIG 7-12 AND 7-14)

CDEN 5 EDEN 5 (1) DEN0(SB)

(B)

CDEN 8 DEN1(SB)

DEN2(SB)

CSET (1) SET (CLOCK)

(FIGURES 7-9, 7-12 AND 7-14)

NOTE
Designations in parenthesis refer to engineering drawings
containing corresponding logic.

B. COMMAND

11-4796

Figure 7-6   Status/Command Block Diagram

7-9

7.3 DRIVE START-UP (Figures 7-7, 7-8, and 7-9)

7.3.1 Drive Start Signals
The SET pulse starts the command operation in the drive by:

1. Setting the EMD flip-flop and asserting EMD (SB) to the drive

2. Asserting SLAVE SET PLS (SB) to the drive

3. Setting the MOVE flip-flop, thereby negating STOP (SB) to the drive.

MOVE remains asserted and holds STOP (SB) false during the entire command operation. During a rewind operation, the MOVE flip-flop is not set. In this case, SLAVE SET PLS negates STOP (SB) at SET time, which is sufficient for the drive to start the rewind sequence.

7.3.2 Start-Up Delay
The output of the EMD flip-flop loads the motion delay counter with delay data set onto read lines RRD0–RRD6, RRDP by the drive. Bit 13 of the counter is preset to a 1 and gates in the clock pulses. The clock pulses are obtained from a divide-by-four counter which receives CLOCK (SB) pulses from the slave bus. An output from the divide-by-four counter is obtained after the first two CLOCK (SB) pulses and every four CLOCK (SB) pulses thereafter. When the delay counter has been clocked through the delay period, bit 13 of the delay counter is counted down to 0 and bit 14 is asserted. At this time:

1. Input clock pulses to the delay counter are inhibited.

2. READING is asserted, enabling the read sequence.

3. ACCL (SB) is negated to the drive, thus gating WRT CLK (SB) pulses in from the drive for the write sequence.

If the command is CWXG or CWFMK, an extended interrecord gap is generated prior to writing the record. CWXG or EWFMK, if asserted, inputs into the delay counter, increasing the delay time and allowing the tape to travel an extra distance before the read and write sequences are enabled. The delay increase is from 8.99 to 95.00 ms for a 9-track drive, and from 15.26 to 101.3 ms for a 7-track drive. The CWXG and EWFMK inputs to the delay counter are via a gate enabled by ACCL. Thus only the start-up time or gap prior to the record is extended.
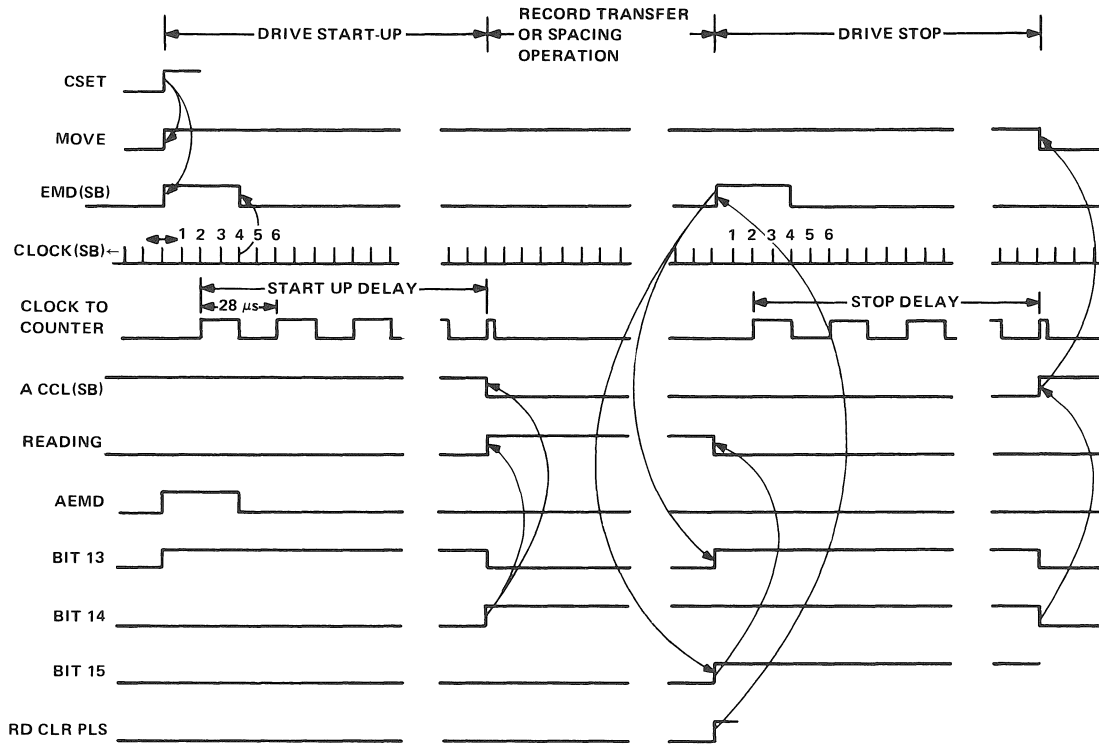
Figure 7-7   M8926 Timing Diagram
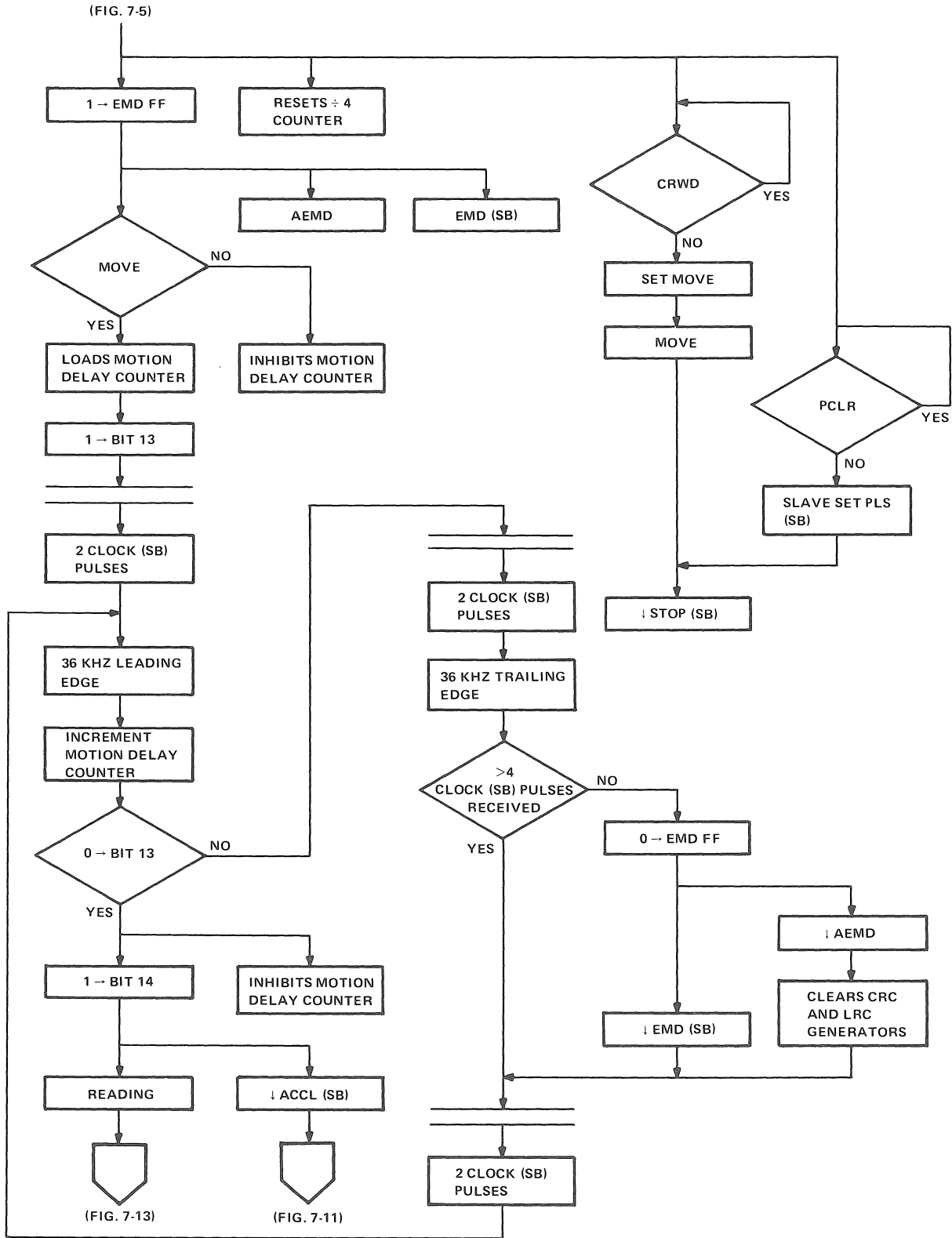
Figure 7-8   Drive Start-Up Flow Diagram
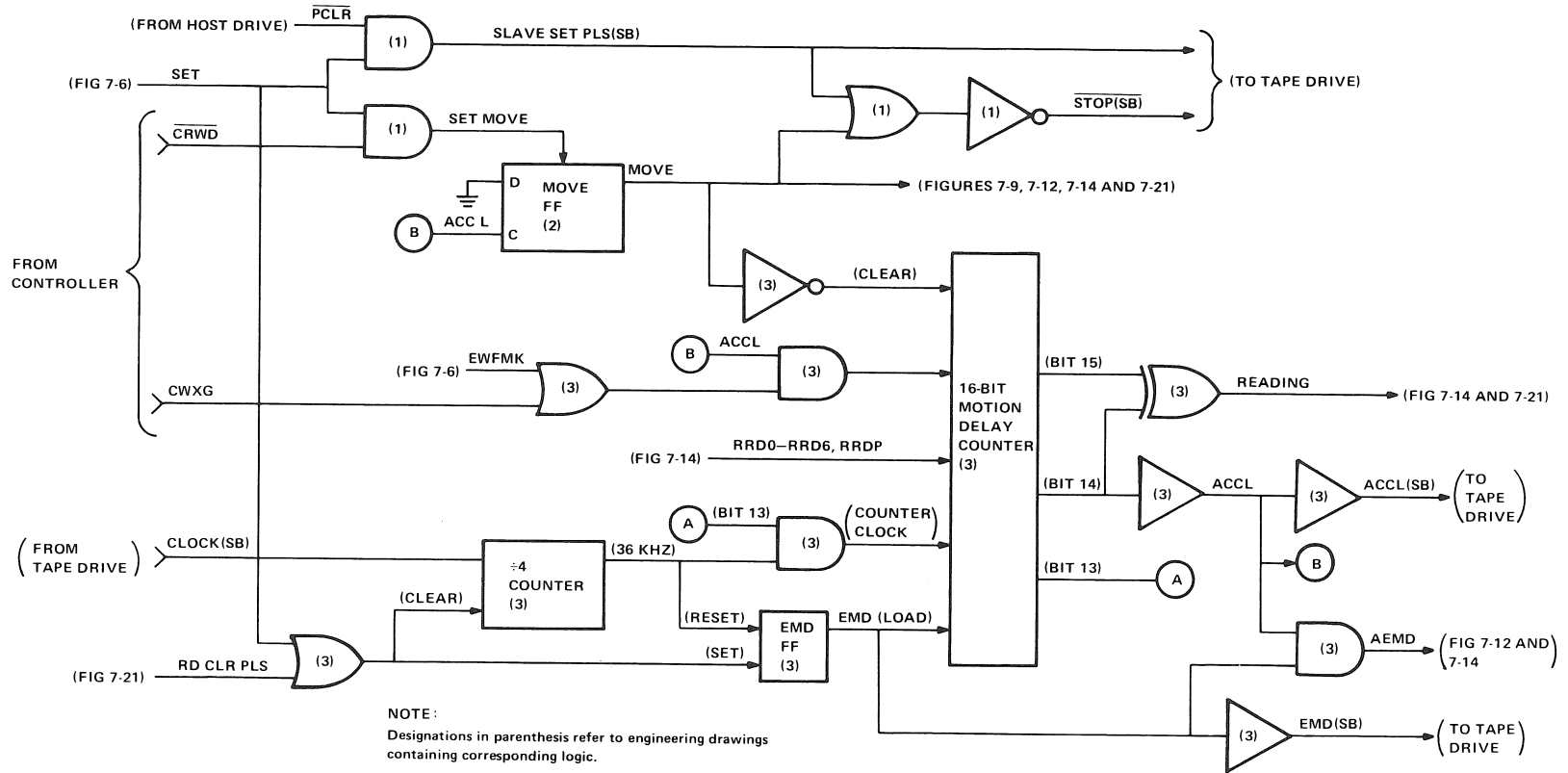
Figure 7-9   Start/Stop Control Block Diagram

7.4 WRITE SEQUENCE (Figures 7-10, 7-11, and 7-12)

7.4.1 Nine-Track Normal

7.4.1.1 Write Data – If a write command is asserted by the controller, CWRE will be true, allowing the SET pulse to set the WRITING flip-flop. The assertion of WRITING loads the end-of-record counter, which is preset to a count of 8. The 8-bit output from the counter gates R WRT CLK pulses from the drive to produce WRITE STROBE pulses. The assertion of each WRITE STROBE pulse will:

1. Latch up write data from the controller, making it available to the drive via the output gates.

2. Assert CWRS to the controller to extract the next character from memory.

3. Assert REC (SB) to the drive and to the CRC generator.

Vertical parity is produced by a parity generator that monitors the eight write lines and outputs a true or false parity bit according to the number of 1 bits and whether odd or even parity is specified (EPEVN).

The write logic contains a circuit to detect a zero-character condition when even parity is specified. Such a condition results in a blank space on the tape which cannot be sensed by the read logic. Should an attempt be made to write a zero character with even parity, the zero character detector output would assert WRX3, thereby generating a 1 bit on the third write channel. A single bit character demands a 1 parity bit when EPEVN is true. The parity bit is also artificially generated via the zero character detector output, which asserts WRXP to the parity write channel.

The CRC generator receives each data character from the write channels. REC (SB) pulses clock the generator which develops the CRC character during the body of the record.

7.4.1.2 Write-End-of-Record – When the data transfer has been completed, CWDR and WRITING are negated, and REC and CWRS strobes are inhibited. The sequence is illustrated in the data transfer timing diagram (Figure 7-10). It can be seen in Figure 7-12 that data characters are moved from memory to tape in two steps: first from memory to the write data latch-up register, and then from the register to the transport write logic. The last four characters of a record are shown in Figure 7-10. CWRS 1 issued to the controller extracts data character 2 from memory, which moves through the controller and over to the M8926 write data latch-up register. The next write clock pulse (R WRT CLK 2) generates WRITE STROBE 2, REC 2, and CWRS 2. WRITE STROBE 2 latches up data character 2 in the register, making it available to the transport write logic; REC 2 records data character 2 on tape; and CWRS 2 extracts data character 3 from memory. The next CWRS pulse (CWRS 3) extracts the last character (data character 4) from memory. R WRT CLK 4 generates WRITE STROBE 4 to latch up the last character, and REC 4 to record it on tape. CWRS 4 is issued to the controller which, having sensed that the last character has been transferred, inhibits a data extraction from memory (no NPR bus cycle) and negates CWDR. The negation of CWDR conditions the WRITING flip-flop to reset. The trailing edge of R WRT CLK 4 clocks the flip-flop reset, thus negating WRITING. When WRITING negates:

1. CWRS pulses to the controller are inhibited.

2. REC (SB) pulses to the drive are inhibited.

3. The end-of-record counter is enabled.

R WRT CLK

WRITE
STROBE

REC(SB)

CWRS

DATA
CHARACTER
1

DATA
CHARACTER 2

From memory to
LU register

Latched up & sent to heads
Recorded on tape

DATA CHARACTER 3

From memory to
latch-up register

Latched-up & sent to heads
Recorded on tape

DATA CHARACTER 4

From memory to
latch-up register

Latched-up & sent to heads
Recorded on tape

CONTROLLER SENSES
THIS IS LAST DATA
CHARACTER

CWDR

WRITING

NOTE:

Each R WRT CLK pulse generates WRITE STROBE which generates REC and CWRS. Arrows
shown only for R WRT CLK 1.

11-4776

Figure 7-10   Write Data Timing Diagram

7-16

WRITE STROBE pulses clock the end-of-record counter. When the counter reaches a count of 3, CHK CHAR STRB asserts and:

1. Switches the CRC character onto the write lines via the write data/CRC multiplexer

2. Enables the REC AND gate

The next WRITE STROBE pulse latches up the CRC character and generates a REC (SB) pulse for the drive to record the CRC character. Three WRITE STROBEs later, the counter is at a count of 7 and again asserts CHK CHAR STRB which:

1. Enables the REC AND gate

2. Asserts LRC STROBE via the enabled LRC STROBE AND gate

LRC STROBE asserts LRC STRB (SB) to the drive and resets the write data latch-up register, setting all the write lines to zero. (The LRC character is generated in the drive.) The next WRITE STROBE asserts REC (SB) to record the LRC character, and resets the end-of-record counter, thereby inhibiting any further WRITE STROBE pulses.

7.4.2 Seven-Track Normal
Seven-track normal operation is identical to nine-track normal except for the write-end-of-record sequence. In 7-track operation, both bits 4 and 8 of the end-of-record counter are preset to a 1. Thus when the counter reaches a count of 3, the same conditions exist as a count of 7 in 9-track operation. The 7-track end-of-record sequence is:

1. The last data character

2. Three blank spaces

3. The LRC character

4. Reset end-of-record counter to terminate the write sequence

7.4.3 Nine-Track File Mark

7.4.3.1 Write Data – In file mark operation, EWFMK is true and forces the write data CRC multiplexer to output all 1s into the write data latch-up register. After the 1s are clocked into the register, they are applied to the output gates. With EWFMK true and 7TRK false, all the output gates are inhibited except 0, 1, and 4, thus outputting an octal 23 (9-track file mark) to the drive.

CWRE is true and CWDR is false for a CWFMK command. CWRE allows the SET pulse to set the WRITING flip-flop. The first WRT CLK (SB) pulse asserts WRITE STROBE and then REC (SB) but, due to CWDR being false, also resets the WRITING flip-flop. Thus one WRITE STROBE and one REC pulse are issued for the file mark character.

No CWRS pulses are returned to the controller in file mark operation.

7.4.3.2   Write-End-of-Record – The write-end-of-record sequence for a 9-track file mark is identical to the write-end-of-record sequence for 9-track normal except that the CRC character is skipped and only the LRC character is written. The end-of-record counter must reach a count of 7 before a CHK CHR STRB is asserted. At this point, the same conditions exist as in the 9-track normal mode; thus the LRC character is recorded and the write sequence is terminated. The 9-track file mark end-of-record sequence is:

1.   The last data character (the file mark character)
2.   Seven blank spaces
3.   The LRC character
4.   Reset end-of-record counter to terminate the write sequence

7.4.4   Seven-Track File Mark
The write data sequence for the 7-track file mark is identical to that for the 9-track file mark except that 7TRK is asserted to the output gates via the enabled EWFMK gate. Output gates now enabled are 0, 1, 2, and 3, thus outputting an octal 17 (7-track file mark) to the drive.

The end-of-record sequence for the 7-track file mark is identical to that for a 7-track normal sequence.
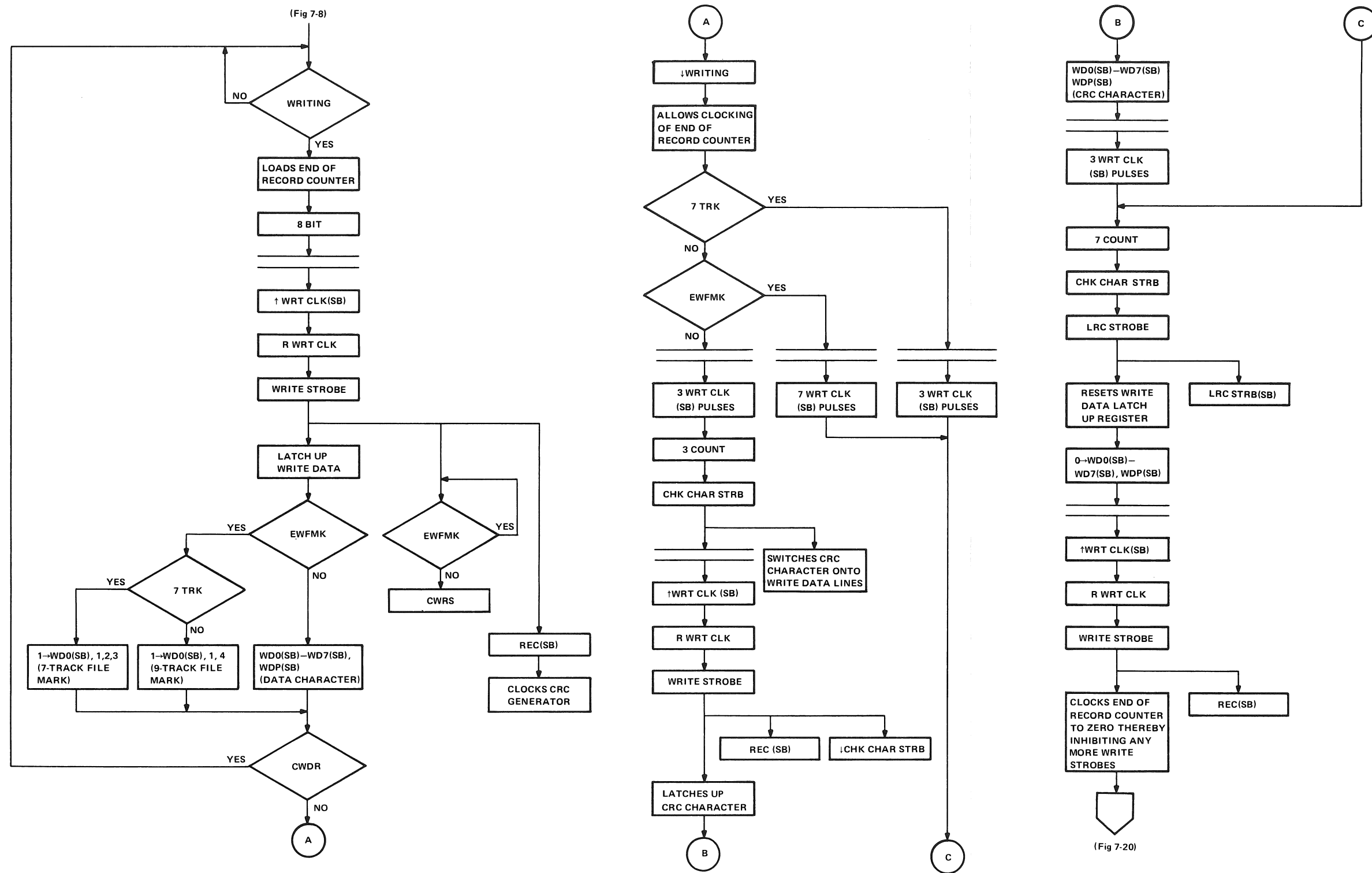
Figure 7-11 Write Flow Diagram

11-4792
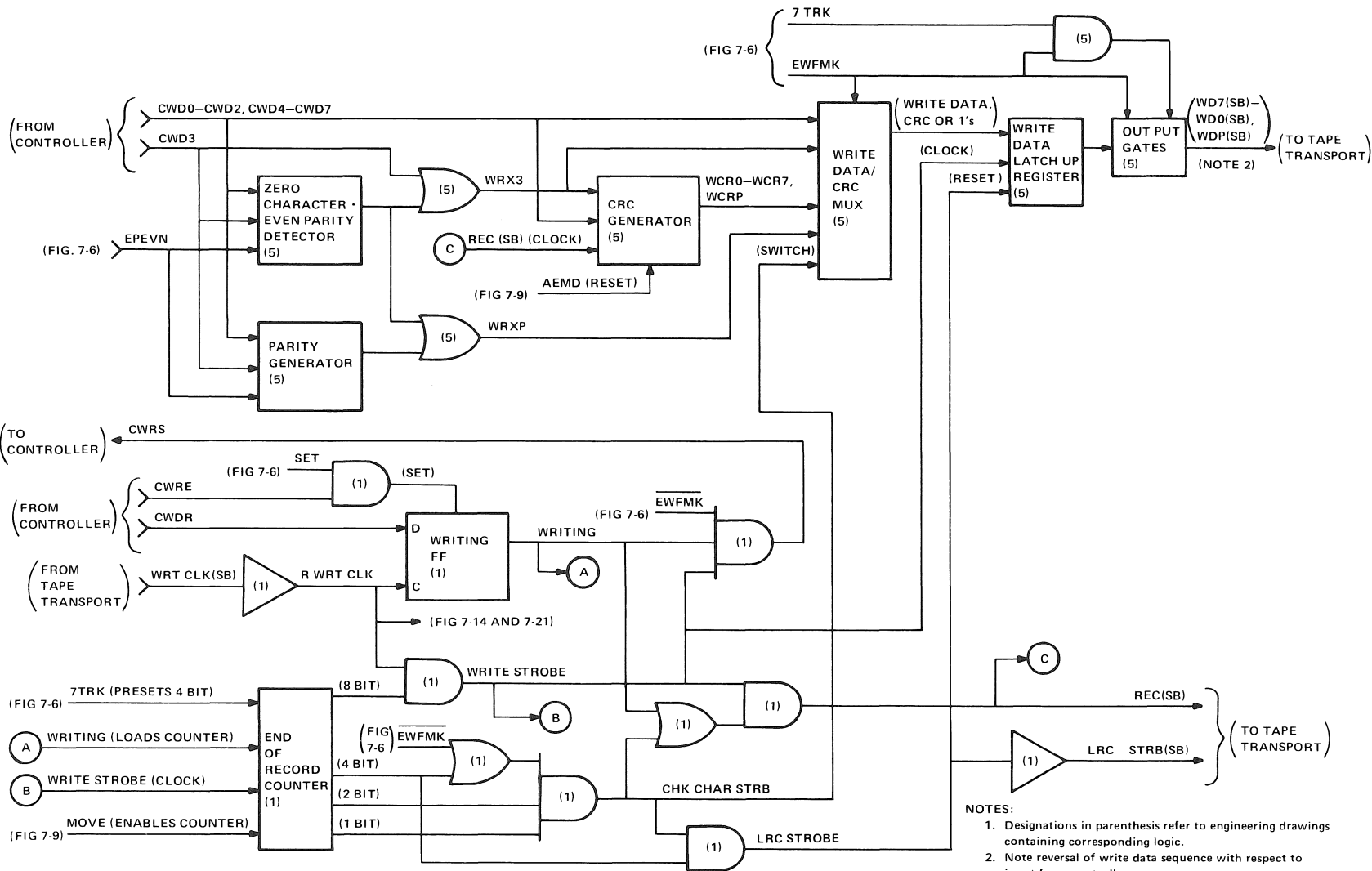
Figure 7-12   Write Block Diagram

11-4794

7.5 READ SEQUENCE

7.5.1 Read Data (Figures 7-13 and 7-14)
RSDO (SB) pulses from the drive assert COMP RD STRB which:

1. Clocks the read data latch-up register

2. Triggers the read strobe one-shot, asserting CRDS to the controller.

3. Uses a second output from the read strobe one-shot (CHECK REG PLS) to clock the CRC generator and the LRC generator (and the LRCS flip-flop in the end-of-record detection sequence, Paragraph 7.5.4).

When the read data latch-up register is clocked by COMP RD STRB, read data is made available to the controller via the read data output multiplexer. (Note the order reversal of the read data in the latch-up register.) When READING is true, the multiplexer selects the data character from the read lines for the controller. When READING is false (for example, after a data transfer operation), the LRC character is output to the controller for maintenance purposes.

7.5.2 Error Detection (Figures 7-13 and 7-14)
Read data ERD7-ERD0, ERDP are checked for CRC, LRC, and vertical parity errors. Each data character is clocked into the CRC and LRC generators by the CHECK REG PLS. At the end of the record, the CRC character is compared with the contents of the CRC generator, causing the CR7-CR0, CRP output to be all zeros. The CRC error detector looks for an all zero output from the comparison. If the CRC generator output is not all zeros when CRCS is true, CCRCE is asserted to the controller, indicating a CRC error.

In a similar manner, the LRC character is compared with the contents of the LRC generator, causing the LR7-LR0, LRP output to be all zeros. The LRC error detector looks for an all zero output from the comparison. If the LRC generator output is not all zeros when LRCS is true, CLRCE is asserted to the controller, indicating an LRC error.

CRC and LRC error outputs are enabled only when the drive is executing a forward motion command. (This is due to the location of the CRC and LRC characters at the end of the record.) Accordingly, EFOR must be true for CCRCE or CLRCE to assert.

Each data character occurring during the body of a record is checked for vertical parity error by a vertical parity error detector circuit. If a parity error is sensed by the detector, CVPE is asserted to the controller. CVPE is inhibited during CRCS and LRCS times as the ERDP bit does not represent vertical parity of the CRC and LRC characters.

7.5.3 File Mark Detection (Figures 7-13 and 7-14)
The file mark detection logic monitors the read data and outputs CFMK to the controller if a file mark is detected. Three conditions must be met before the record is identified as a file mark:

1. There must be two characters and only two characters to the record.

2. Both characters must be file mark characters.

3. The second file mark character must be followed by at least eight blank spaces.

To meet condition 2, read data (ERD7–ERD0, ERDP) is examined by the file mark character detector which outputs FMK CHR if a file mark character is sensed. A file mark character flip-flop is set by the SET pulse at the start of the operation and then clocked by RRSDO pulses. The flip-flop is conditioned to set by FMK CHR, via an AND gate, so that if the flip-flop is clocked to the reset state it cannot be set again during the current operation. Thus the first two characters read must be file mark characters in order to keep the file mark character flip-flop set.

Conditions 1 and 3 are met by means of a file mark gap detector and a read strobe counter. When the read strobe counter reaches a count of two, the file mark gap detector is enabled and starts counting R WRT CLK pulses. When the strobe counter reaches a count of three, RSDO > 2 asserts and resets the gap detector. If the gap detector reaches a count of eight, it outputs 8 BLANK SPACES and CFMK is asserted to the controller via an enabled AND gate. If a third RSDO pulse occurs before the gap detector reaches eight, the detector is cleared and the file mark character flip-flop is reset, indicating that the record is not a file mark and a normal record transfer is in progress.

The end-of-record detection sequence is enabled from the read data channels via a record active OR gate. If a normal record transfer is in progress (RSDO > 2 is true) or a file mark has been detected (FMK true), RECORD ACTIVE is asserted and enables (but does not start) the end-of-record detection sequence.

(FIG. 7-8)

C

RSDO (SB) — NO

YES

RRSDO

COMP RD STRB

CRDS

CHECK REG PLS

ERD7–ERD0, ERDP

CLOCKS CRC GENERATOR

CLOCKS LRC GENERATOR

7 TRK — NO / YES

023 PAR=0 — NO

017 PAR=0 — NO

YES / YES

↓(FILE MARK CHARACTER)

>2 RRSDO PULSES — NO → A

YES

B

FMK CHR

C

READING — NO

SWITCHES LRC7–LRC0, LRCP ONTO READ OUTPUT LINES

YES

CRD7–CRD0, CRDP DATA CHARACTER

CRD7–CRD0, CRDP (LRC GENERATOR OUTPUT; FOR MAINTENANCE USE)

A

VERTICAL PARITY ERROR — NO

YES

CVPE

↓(FILE MARK CHARACTER) — YES

TWO RRSDO PULSES RECEIVED — NO

YES

ENABLES FILE MARK GAP DETECTOR

3RD RRSDO PULSE — YES

NO

DISABLES FILE MARK GAP DETECTOR

↓R WRT CLK

B

8TH R WRT CLK PULSE SINCE 2ND RRSDO PULSE — NO

YES

8 BLANK SPACES

FMK

CFMK

RECORD ACTIVE

LAST DATA CHARACTER TRANSFERRED — NO

YES

(FIG. 7-20)

11-4790

Figure 7-13   Read Flow Diagram

Figure 7-14 Read Block Diagram

11-4823

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7.5.4 End-of-Record Detection (Figures 7-20 and 7-21)

7.5.4.1 Nine-Track Normal (Figure 7-15) – The end of a record is detected by looking for the three blank spaces that occur between the last data character and the CRC character (LRC character for 7-track). The blank spaces are detected by an end-of-record counter that is clocked by R WRT CLK pulses and effectively reset by COMP RD STRB pulses. (Actually the COMP RD STRB pulses load the counter with a count of 8.) COMP RD STRB pulses are asserted by RRSDO pulses from the drive. The R WRT CLK pulse and the RRSDO pulse are not necessarily in sync but they are of the same frequency. Hence the end-of-record counter is continually being clocked and "reset" during the body of a record. Two R WRT CLK pulses might squeeze in between two RRSDO pulses, thereby clocking the counter to a count of two before it is reset, but it should never reach a count higher than two during the body of a record. If the counter does reach a count of three (three R WRT CLK pulses with no RRSDO pulse) 3 COUNT is asserted, signifying that this is the end of the record and the end-of-record sequence is started.

Figure 7-15 End-of-Record Timing, Non-Zero CRC and LRC

The assertion of 3 COUNT clocks the CRCS flip-flop set, outputting CCRCS to the controller to indicate that the next character will be the CRC character. The next RRSDO pulse will be the CRC character strobe, which will:

1. Latch up the CRC character in the read data latch-up register
2. "Reset" the end-of-record counter
3. Assert CRDS to the controller
4. Assert CHECK REG PLS, which clocks the LRCS flip-flop to the asserted state

The asserted output of the LRCS flip-flop will reset the CRCS flip-flop and assert CLRCS to the controller, indicating that the next character will be the LRC character. The next RRSDO will be the LRC character strobe, which will:

1. Latch up the LRC character in the read data latch-up register
2. "Reset" the end-of-record counter
3. Assert CRDS to the controller
4. Assert CHECK REG PLS, which resets the LRCS flip-flop

7-27

The negation of LRCS sets the end-of-record flip-flop, asserting END OF RECORD which locks the CRCS flip-flop in the reset state until the next operation.

When END OF RECORD asserts, a decision delay period begins. The decision delay period is a time interval (normally eight R WRT CLK pulses long) between the assertion of END OF RECORD and the assertion of RD CLR PLS. The delay period is a "last chance" look for more RRSDO pulses before triggering the drive stop sequence. At the start of the decision delay, the end-of-record counter is "reset" (preset to a count of 8) and starts counting R WRT CLK pulses. When the counter reaches a count of 8, it overflows into the decision delay counter which then asserts RD CLR PLS to the drive stop logic. Should RRSDO pulses re-occur any time during the decision delay period, the end-of-record counter will be "reset" and the read sequence will continue. When the actual end-of-record does occur, the decision delay count will start again but the end-of-record sequence will not repeat.

The end-of-record sequence is inhibited if a write operation is in progress (WRITING true). During a write operation, defective spots in the tape may simulate a gap and erroneously trigger the end of record sequence. In this case, the end-of-record logic is functioning to stop the drive while the controller is still trying to write data. To prevent this, $\overline{\text{WRITING}}$ is gated with the R WRT CLK pulses into the end-of-record counter, thereby allowing the counter to operate only if WRITING is false.

7.5.4.2 Zero CRC or LRC Characters – The CRC or the LRC character may be a zero character resulting in no corresponding RRSDO pulse being received from the drive. In this case, a COMP RD STRB pulse is generated artifically so clocking of the end-of-record sequence can continue. If no RRSDO pulse is received to "reset" the end-of-record counter, counting will continue up to six, at which time COMP RD STRB will be asserted via a gate enabled by CRCS or LRCS. Figures 7-16 and 7-17 illustrate the timing sequence for a zero CRC and a zero LRC character, respectively.
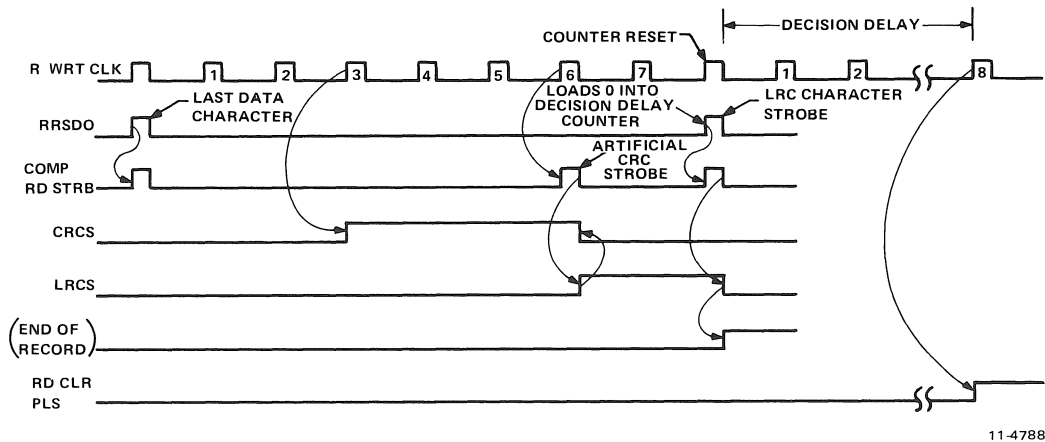
11-4788

Figure 7-16   End-of-Record Timing, Zero CRC
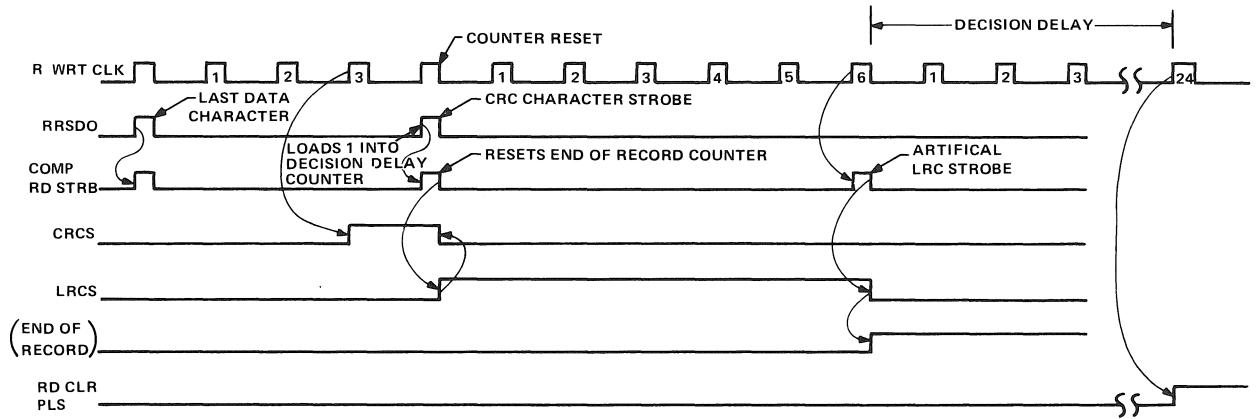
Figure 7-17 End-of-Record Timing, Zero LRC

The decision delay is normally eight R WRT CLK pulses long but is extended to 24 pulses if no LRC character is detected. Failure to detect an LRC character may be due to the character being zero, but it could also be due to a bad area in the tape. Thus when no LRC character is detected, some doubt exists on whether the end of the record has been reached. Extending the decision distance to 24 pulses provides extra assurance that the end of the record has been reached. The decision delay counter is a count-down counter that is loaded by each RRSDO pulse. The counter is loaded with zeros except for the 1 bit, which is loaded with $\overline{LRCS}$. If there is an LRC character, then LRCS is true during the last RRSDO pulse (Figure 7-15) and the counter is loaded with all zeros. If there is no LRC character, then LRCS is false during the last RRSDO pulse (Figure 7-17) and the delay counter is loaded with a 1. In this case, the end-of-record counter must count an additional 16 pulses to count down the 1 and assert RD CLR PLS.

7.5.4.3 Seven-Track and File Mark (Figures 7-18 and 7-19) – In 7-track or file mark operation, the end-of-record sequence is modified to eliminate the CRC character from the sequence. With either FMK or 7TRK true, the 3 COUNT output from the end-of-record counter directly sets the LRCS flip-flop, which in turn holds the CRCS flip-flop reset. Also, when in file mark operation, the decision delay is extended to 24 R WRT CLK pulses as there is no RRSDO pulse associated with the assertion of LRCS.

7-29
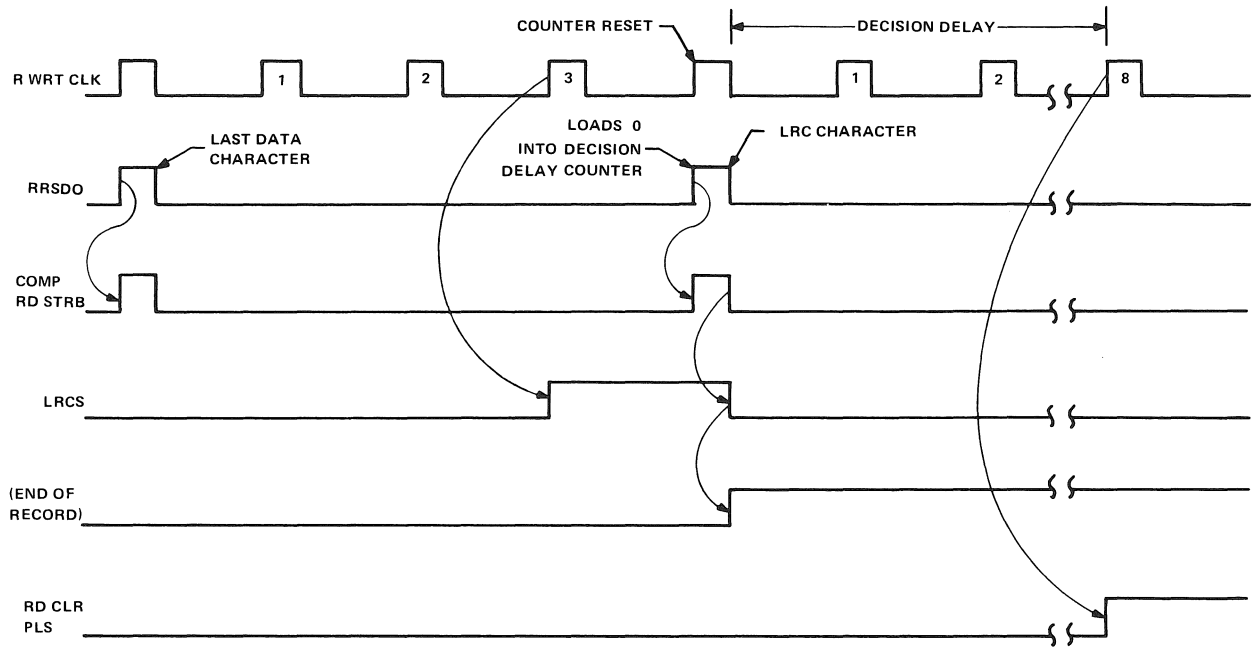
Figure 7-18   End-of-Record Timing, Seven-Track
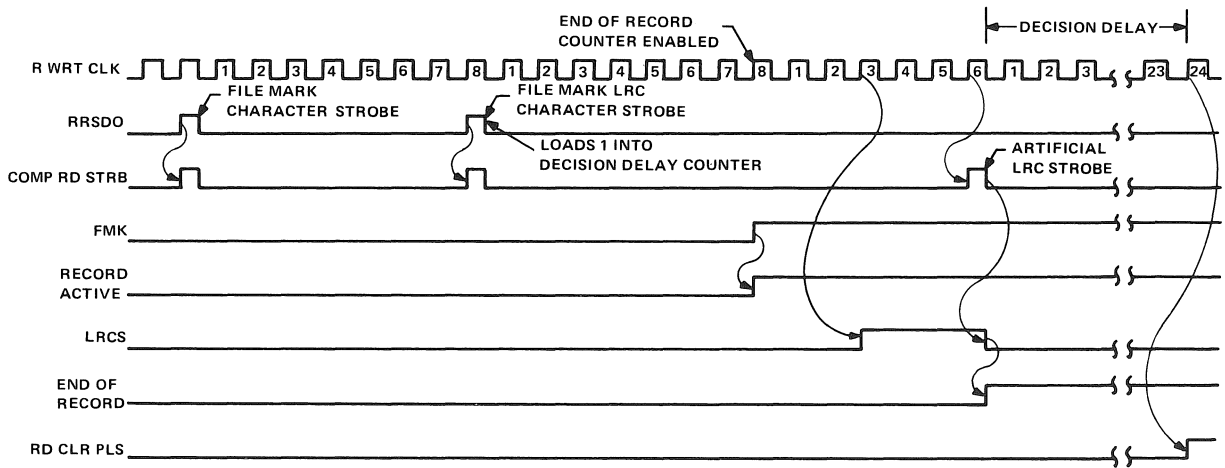
Figure 7-19   File Mark Timing
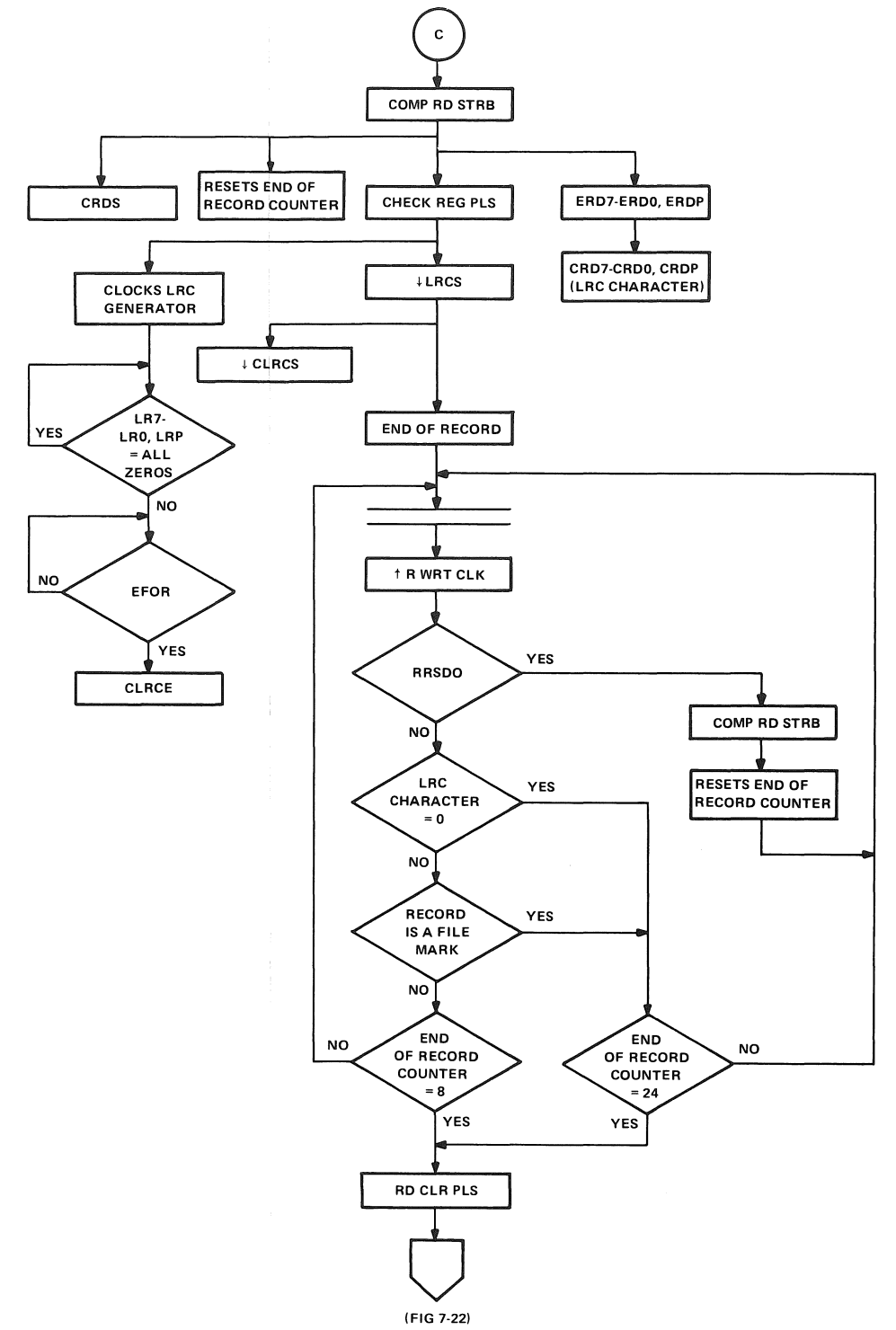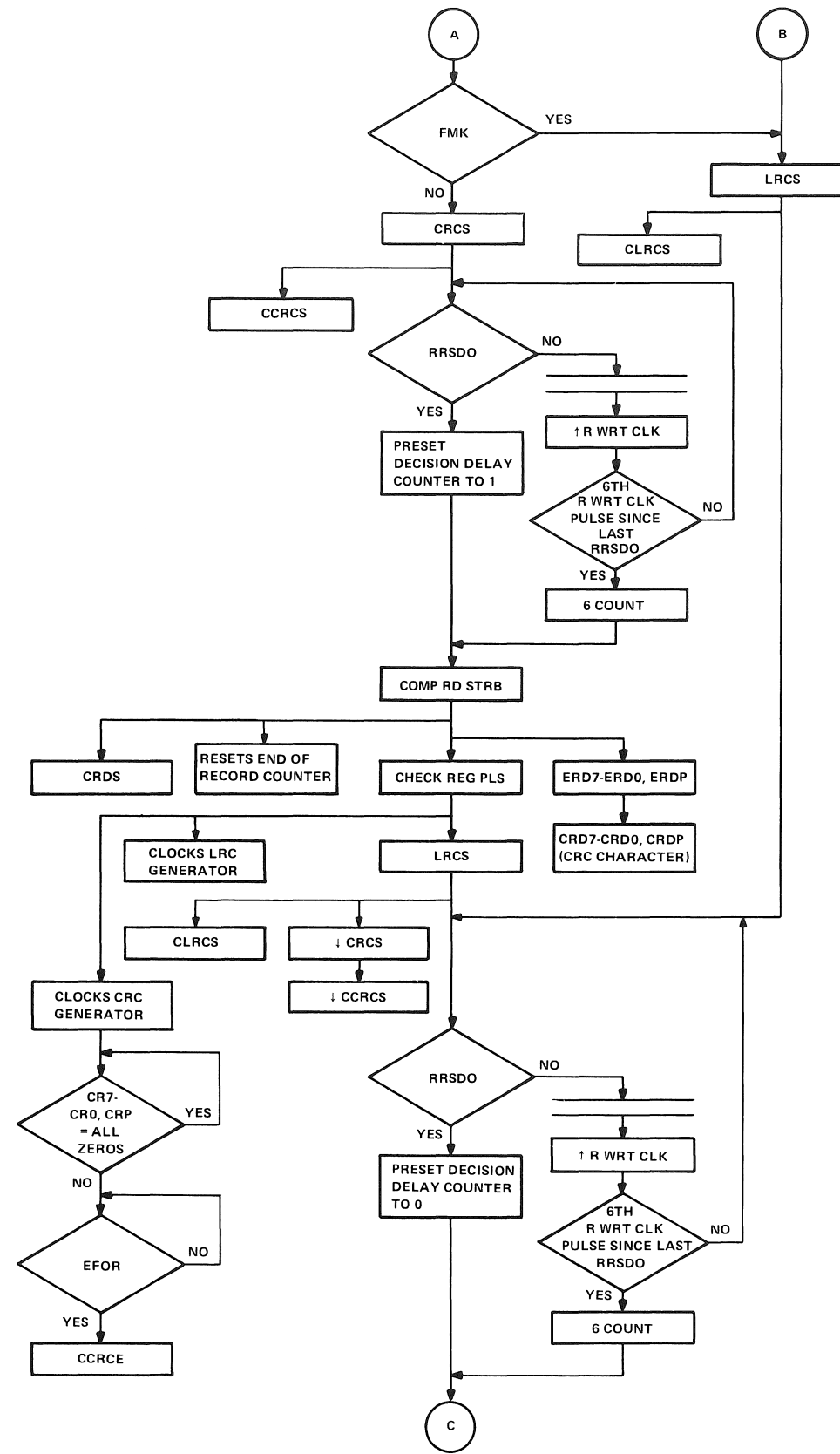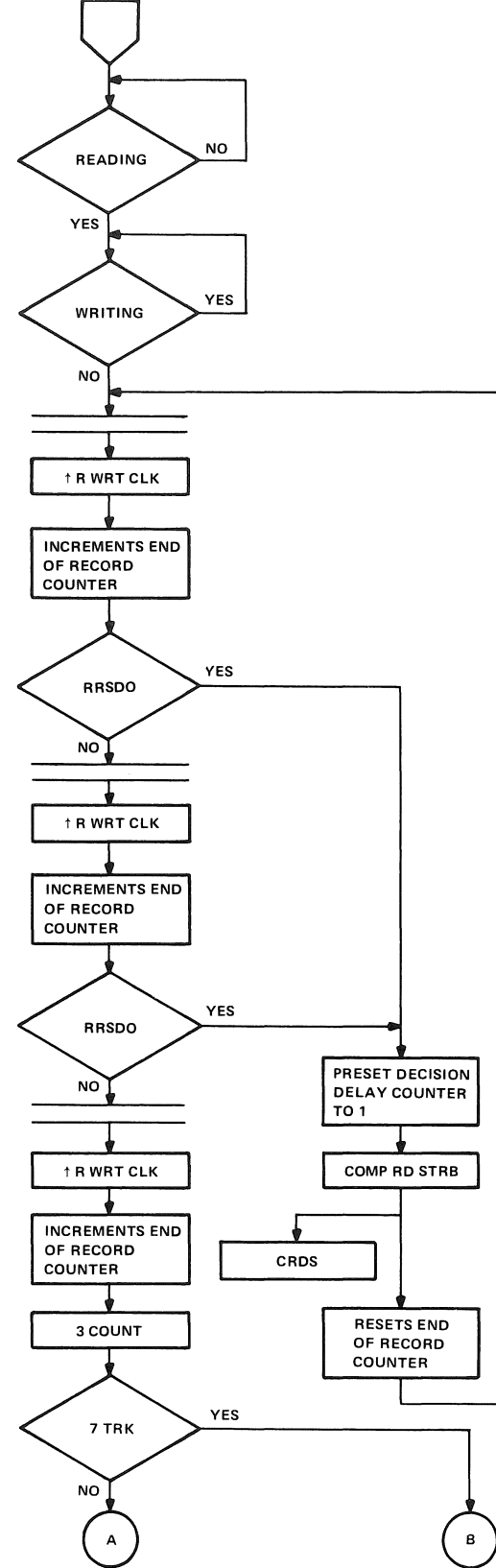
Figure 7-20   End-of-Record Flow Diagram

11-4791

7-31
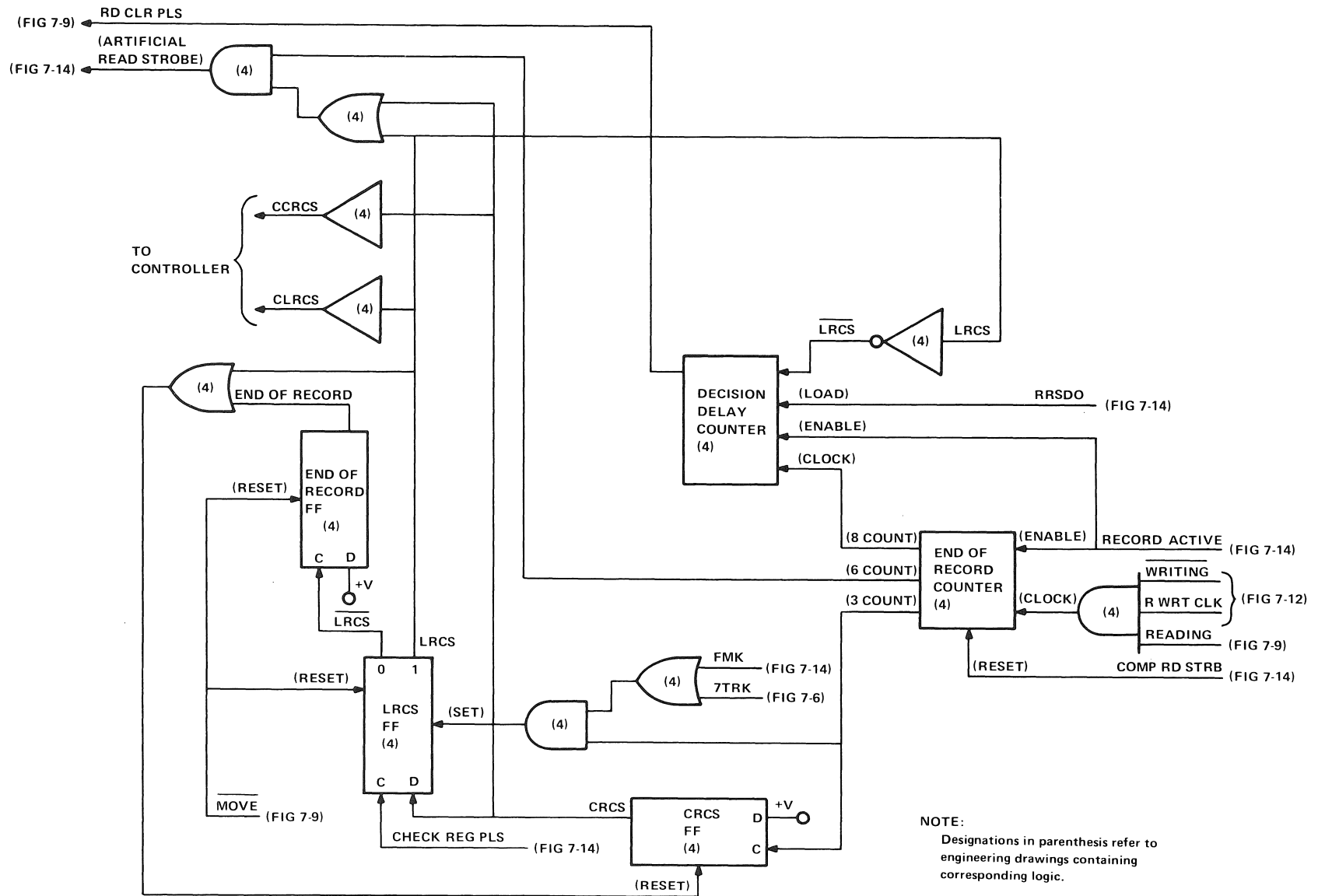
Figure 7-21   End-of-Record Block Diagram

7-33

11-4773

7.6 DRIVE STOP (Figures 7-7, 7-9, and 7-22)

RD CLR PLS triggers the drive stop sequence by setting the EMD flip-flop and asserting EMD (SB) to the drive. The output of the EMD flip-flop also loads the motion delay counter with data set onto read lines RRD0–RRD6, RRDP by the drive. Bit 13 of the counter is preset to a 1. The bit 14 output, which has been a 1 during the record transfer, is connected to the data input of bits 14 and 15. Thus when EMD loads the counter, output bits 13, 14, and 15 become 1s. READING negates due to exclusive ORing of output bits 14 and 15, while bit 13 gates clock pulses into the counter from the divide-by-four counter. The divide-by-four counter receives CLOCK (SB) pulses from the slave bus. An output from the divide-by-four counter is obtained after the first two CLOCK (SB) pulses and every four CLOCK (SB) pulses thereafter. After the delay period, the motion delay counter is clocked reset and:

1. Input clock pulses to the delay counter are inhibited (bit 13 = 0).

2. ACCL (SB) is asserted to the drive (bit 14 = 0) and inhibits WRT CLK (SB) pulses from the drive to the write logic.

The assertion of ACCL resets the MOVE flip-flop, which negates MOVE and asserts STOP (SB) to the drive, thereby terminating the command operation.

(FIG 7-20)

```
  ┌──────────────┐          ┌──────────────┐
  │ RESETS ÷ 4   │          │ 1 → EMD FF   │
  │ COUNTER      │          └──────────────┘
  └──────────────┘

  ┌──────────────┐          ┌──────────────┐
  │ LOADS MOTION │          │ EMD (SB)     │
  │ DELAY COUNTER│          └──────────────┘
  └──────────────┘

  ┌──────────┐   ┌──────────┐   ┌──────────┐
  │1 → BIT 13│   │1 → BIT 14│   │1 → BIT 15│
  └──────────┘   └──────────┘   └──────────┘

                                ┌──────────┐
                                │↓ READING │
                                └──────────┘

  ┌──────────────┐
  │ 2 CLOCK (SB) │
  │ PULSES       │
  └──────────────┘

  ┌──────────────┐
  │ 36 KHZ LEADING│
  │ EDGE         │
  └──────────────┘

  ┌──────────────┐
  │ INCREMENT    │
  │ MOTION DELAY │
  │ COUNTER      │
  └──────────────┘

        ◇ BIT 13 = 0 ◇ ──NO──→

       YES                        ┌──────────────┐
                                  │ 2 CLOCK (SB) │
                                  │ PULSES       │
                                  └──────────────┘

                                  ┌──────────────┐
                                  │ 36 KHZ       │
                                  │ TRAILING EDGE│
                                  └──────────────┘

  ┌──────────────┐  ┌──────────┐   ◇ >4 CLOCK (SB)
  │ INHIBITS     │  │0 → BIT 14│     PULSES        ◇ ──NO──→
  │ MOTION DELAY │  └──────────┘     RECEIVED
  │ COUNTER      │                 YES            ┌──────────────┐
  └──────────────┘  ┌──────────┐                 │ 0 → EMD FF   │
                    │ACCL (SB) │                 └──────────────┘
                    └──────────┘
                    ┌──────────┐                 ┌──────────────┐
                    │↓ MOVE    │                 │ ↓ EMD (SB)   │
                    └──────────┘                 └──────────────┘
                    ┌──────────┐
                    │STOP (SB) │
                    └──────────┘
                                                 ┌──────────────┐
                    (  DONE  )                   │ 2 CLOCK (SB) │
                                                 │ PULSES       │
                                                 └──────────────┘
```
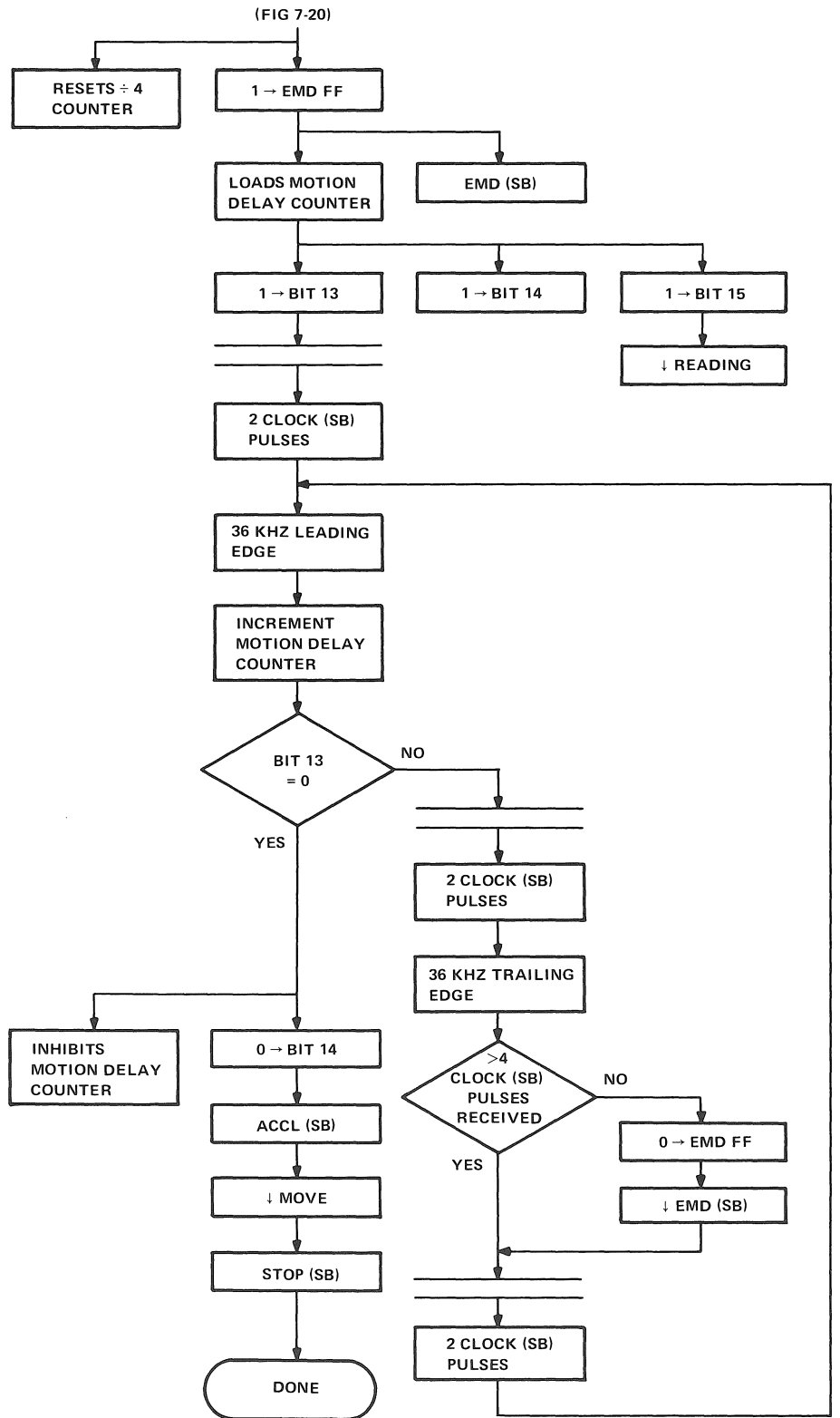
11-4782

Figure 7-22 Drive Stop Flow Diagram

TU10W HOST TRANSPORT THEORY OF OPERATION

8.1 INTRODUCTION

The TU10W is the tape transport used in this magnetic tape storage system. A slave bus connects the host TU10W to the M8926 Interface board logic, and also to any slave TU10W Transports used in the system. Refer to Figure 8-1, the TU10W system block diagram.
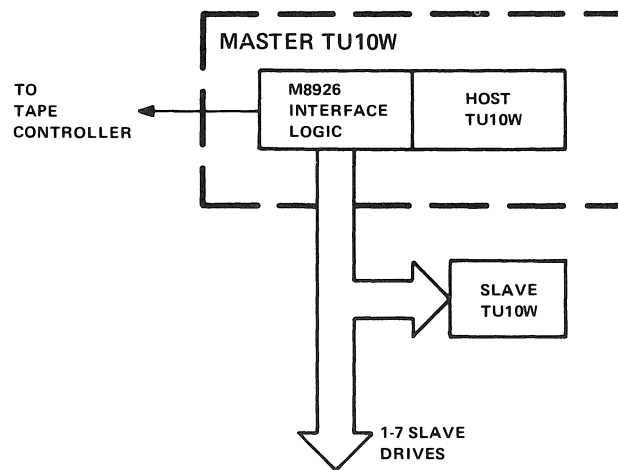
11-4669

Figure 8-1   TU10W System Block Diagram

The slave bus consists of slave (TU10W) select lines, write data lines, read data lines, transport control lines, and additional transport status lines. Figure 8-2 and Table 8-1 show and list the slave bus interface signals, respectively.
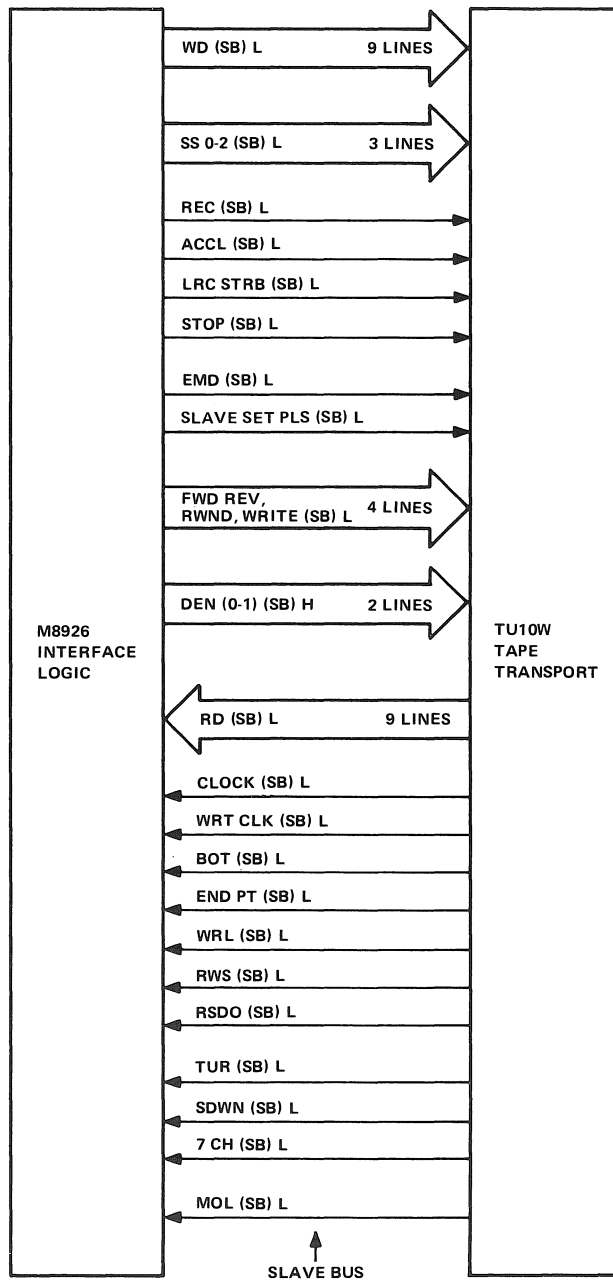
Figure 8-2   Slave Bus Interface Signals

Table 8-1 Slave Bus Interface Signals

Slave Bus Signal	Function
Slave Select [SS(0:2) (SB)]	These lines select one of eight possible TU10W Transports for command execution.
Forward [FWD (SB)] Reverse [REV (SB)] Rewind [RWND (SB)] Write Enable [WRITE (SB)]	These are the four command lines which determine TU10W operation.
Slave Set Pulse [SLAVE SET PLS (SB)]	This signal initiates TU10W response to the four command lines.
Stop [STOP (SB)]	This signal causes the TU10W to terminate motion. (Does not apply to rewind, which terminates independently.)
Enable Motion Delay [EMD (SB)]	This signal enables the TU10W to gate out a coded motion delay preset onto the read lines.
Accelerate [ACCL (SB)]	Asserted by the controller while the transport is getting up to speed or not moving tape.
Write Data [WD (0:7, P) (SB)]	These nine lines transmit data to be written by the TU10W.
Record [REC (SB)]	A pulse that causes data to be written on tape.
Density Select [DEN (0:1) (SB)]	These two lines control the density at which data is written on tape. They must also represent the density of tape data during a read operation.
Clock [CLOCK (SB)]	A 144-kHz clock, generated in the TU10W, present at all times when the unit is on-line.
Write Clock [WRT CLK (SB)]	This clock is transmitted to the controller by a powered, on-line TU10W loaded with tape when it is running at speed (ACCL not asserted). The frequency of WRT CLK is a function of the DEN lines, and controls the write timing frequency.
LRC Strobe [LRC STRB (SB)]	Asserted by the interface logic prior to the REC pulse that writes the LRC character.
Read Data [RD (0:7, P) (SB)]	These nine lines transmit read data from the TU10W to the controller. (They also transmit the motion delay preset.)
Read Strobe Delay Over [RSDO (SB)]	A read strobe pulse generated by the transport at the end of the skew delay in NRZ mode.
Beginning of Tape [BOT (SB)]	Asserted when the TU10W detects the beginning-of-tape marker.

Table 8-1   Slave Bus Interface Signals (Cont)

Slave Bus Signal	Function
End of Tape [EOT (SB)]	Asserted when the TU10W detects the end-of-tape marker.
Rewind Status [RWS (SB)]	Asserted while the selected TU10W is performing a rewind operation.
7-Channel [7CH (SB)]	Asserted when the selected drive is a 7-track transport.
Medium On-Line [MOL (SB)]	Asserted by a selected, powered TU10W which is loaded with tape.
Tape Unit Ready [TUR (SB)]	Asserted by a selected TU10W to indicate that tape motion has stopped.
Settle Down [SDWN (SB)]	Asserted while the transport is decelerating, until it has stopped.
Write Lock [WRL (SB)]	Asserted when the selected TU10W detects that the write enable ring has been removed from the tape reel.

8.2   TRANSPORT OPERATION
Figure 8-3 is a block diagram of the TU10W, showing the major functional groups, control lines, and data paths. The following paragraphs describe these functional groups.

8.2.1   Logic and Write (LAW) Module (M8910)
The LAW module (M8910) interfaces the controller motion control signals and write data path to the TU10W.

Write Data Path – Input to the LAW circuitry of each track is the data line corresponding to that track, plus a delayed REC pulse. (The delay is prewired and corrects for static write skew errors in the write head itself.) NRZ write data is still in binary mode and is converted to NRZ mode (transition for 1s, no transition for 0s) in the LAW module. The write data signals are then applied to the write heads.

Tape Motion – The signals that control the power board (H606), which, in turn, controls capstan and tape reel motion, are generated on the LAW module. The LAW module contains Motion Control flip-flops and additional sequencing circuits. The sequencing circuits provide smooth mechanical operation, which protects data and hardware. The flip-flops enable reel motion and vacuum operation, determine the direction and speed of capstan rotation, and light control panel indicators. These flip-flops are controlled by the controller via the slave bus when the TU10W is on-line, and by the TU10W control panel when the transport is off-line. When the TU10W is on-line and receives a motion/write command from the controller, the flip-flop corresponding to that command will be set upon receipt of SLAVE SET PLS (SB), at which time the motion will commence/the write amplifiers will be enabled. Receipt of STOP L from the controller causes the Motion flip-flops to be reset and the motion terminated.
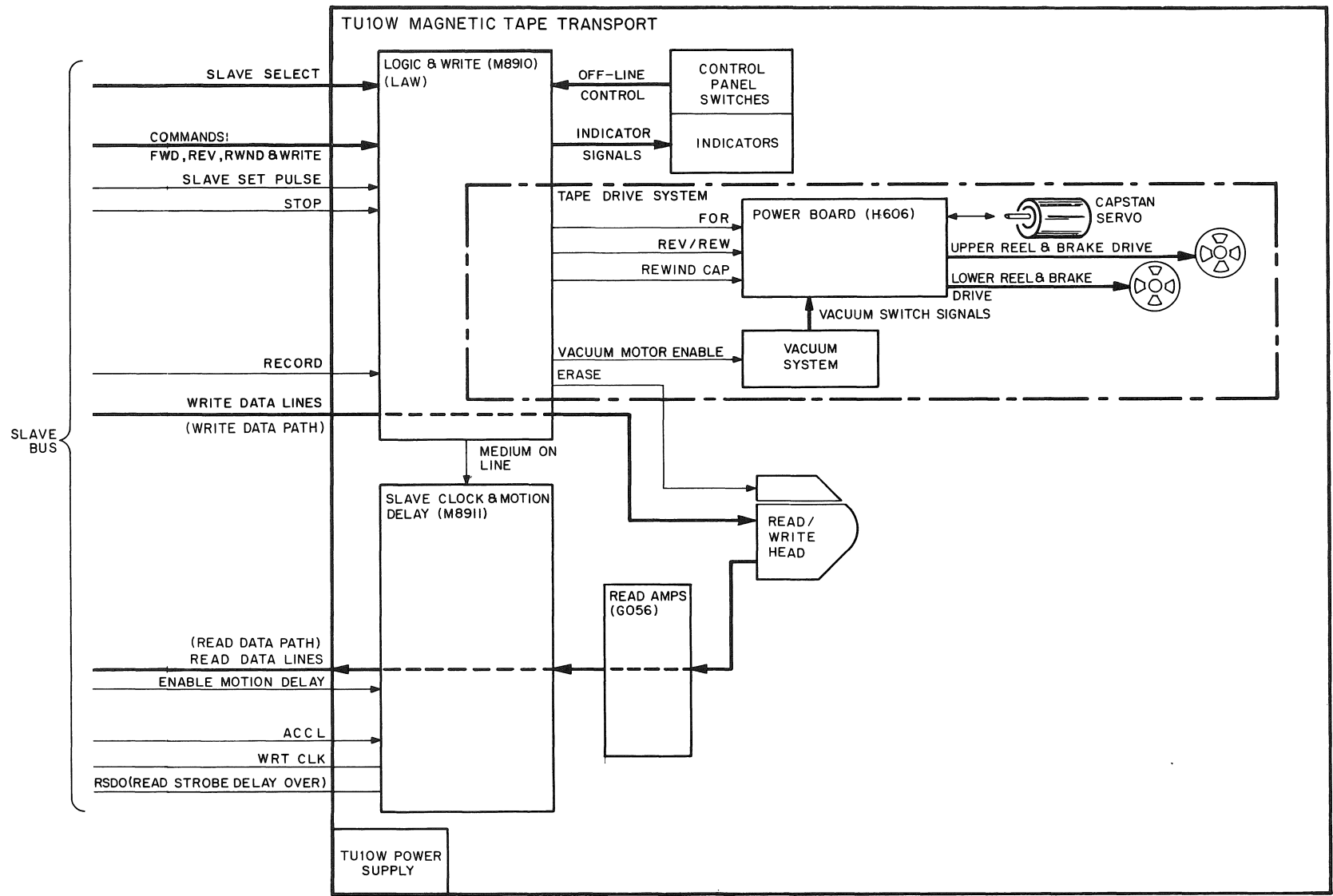
Figure 8-3 TU10W Tape Transport Block Diagram

11-4678

8.2.2 Slave Clock and Motion Delay Module (M8911)

The slave clock and motion delay module (M8911) generates clock signals (CLOCK and WRT CLK). Signal CLOCK is a 144-kHz clock transmitted over the slave bus by a selected, on-line, and powered TU10W loaded with tape. The CLOCK signal is used in the interface module to generate other clock signals, which perform various housekeeping functions. The frequency of WRT CLK depends on the density. It is transmitted to the interface module by a selected, on-line TU10W loaded with tape when it is running at operating speed. Signal WRT CLK plays a crucial role in the interface module during read and write operations. The slave clock and motion delay module also generates presets for the motion delay counter in the interface logic. The presets are multiplexed onto the slave bus read data lines whenever the TU10W receives EMD (enable motion delay) from the interface logic.

8.2.3 Read Head and Read Amplifiers

The read head converts changes in magnetic flux on the tape into voltage signals, which are then amplified by the read amplifiers (G056).

When reading in NRZ mode, the read amplifier of each track produces a high output level for each change of magnetic flux on its tape track (Figure 8-4). These levels are strobed into the interface read logic. Zero bits are recognized by no change in flux on a track (i.e., no high level) when at least one other track has flux change. Because of parity conventions, each character on the tape will have at least one flux change on one of the tape tracks.
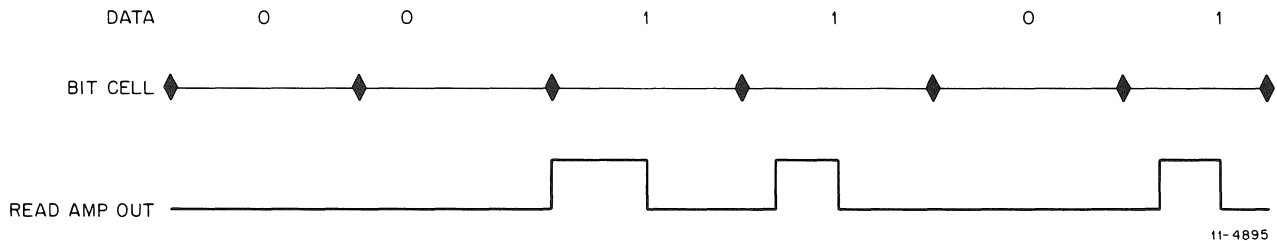
Figure 8-4   Read Amplifier Output

8.2.4 TU10W Power Board

The TU10W power board (H606) contains circuits that control and drive the capstan and tape reels. The capstan motor is part of a servo loop, of which the inputs are motion signals (FOR, REV/REW, and REWIND CAP) from the LAW module. These motion signals control the direction and speed of the capstan motor, which controls the direction and speed of the tape relative to the heads. The tape reel drives, do not control tape direction or speed. The tape reel drives function is to maintain the proper amount of tape in the vacuum columns.

A TU10W Tape Transport has two tape reel drive systems, each one operating independently of the other. The upper tape reel drive operates with the upper vacuum column vacuum switches as inputs. When the tape is too high in the column, the switches activate the tape reel motor to supply tape to the column. When the tape is too low in the column, the tape reel motor is activated to take up tape. The lower tape reel drive operates with the lower vacuum column switches in an identical manner.

8.3 WRITE DATA PATH
The write data path, shown in the TU10W block diagram (Figure 8-3), is discussed in greater detail in this section (Figure 8-5).

The slave bus write data line signals are received by slave bus receivers on the logic and write (LAW) module (M8910), and then input to the LAW write data multiplex, through which they pass to the LAW write deskew buffer.

Timing for the interface logic is derived from WRT CLK, which is generated in the TU10W. Signal WRT CLK is also gated in the interface logic to produce REC pulses, which are transmitted back to the TU10W. These REC pulses are input to a delay, which is tapped (hardwired at manufacture), and connected to the clock inputs of the write deskew buffer. This arrangement provides write deskew; it compensates for errors inherent in the manufacture of tape heads that prevent the heads for all the tape tracks from ideally lining up.

The write deskew buffer circuitry also converts the binary NRZ data to its NRZ form, i.e., transition for 1s, no transition for 0s. The write deskew buffer output is then driven to the write heads.

8.4 READ DATA PATH
The read data path, shown in the TU10W block diagram (Figure 8-3), is discussed in greater detail in this section (Figure 8-6).

As tape moves past the read heads, flux transitions on the tape cause the read heads to produce positive and negative current pulse outputs. These current pulses are processed in the read amplifiers (G056) to yield voltage levels. The voltage levels are then transmitted by line drivers in the TU10W through the slave bus and the interface board to the controller.

8.5 TEST FUNCTION GENERATOR
The test function generator (TFG) module (M8912) is used for off-line testing of the TU10W Tape Transport. During normal, on-line operation of the TU10W, the module must be located in section EF of slot 3 of the TU10W backplane. For use as an off-line tester, the TFG module must be moved to section AB of slot 3.

8.5.1 Functional Modes
An operating procedure for the TFG is presented in flowchart form in Figure 8-7. Figure 8-8 provides additional information on TFG switch settings. The TFG module is illustrated in Figure 8-9.

TU1OW TAPE TRANSPORT

LOGIC AND WRITE (M8910)

WRITE DESKEW BUFFER

INTERFACE LOGIC

P/O SLAVE BUS
WRITE DATA LINES 9 BITS

SLAVE BUS CONNECTOR

9 BITS

SLAVE BUS RECEIVERS

WRITE DATA MUX

WD 0
WD 1
WD 2
WD 3
WD 4
WD 5
WD 6
WD 7
WD P

RECORD PULSE

WRT CLK

TEST DATA

TEST FUNCTION GENERATOR (M8912)

SLAVE CLOCK AND MOTION DELAY (M8911)

TAPPED DELAY

SKEW CLOCK

WRITE HEAD
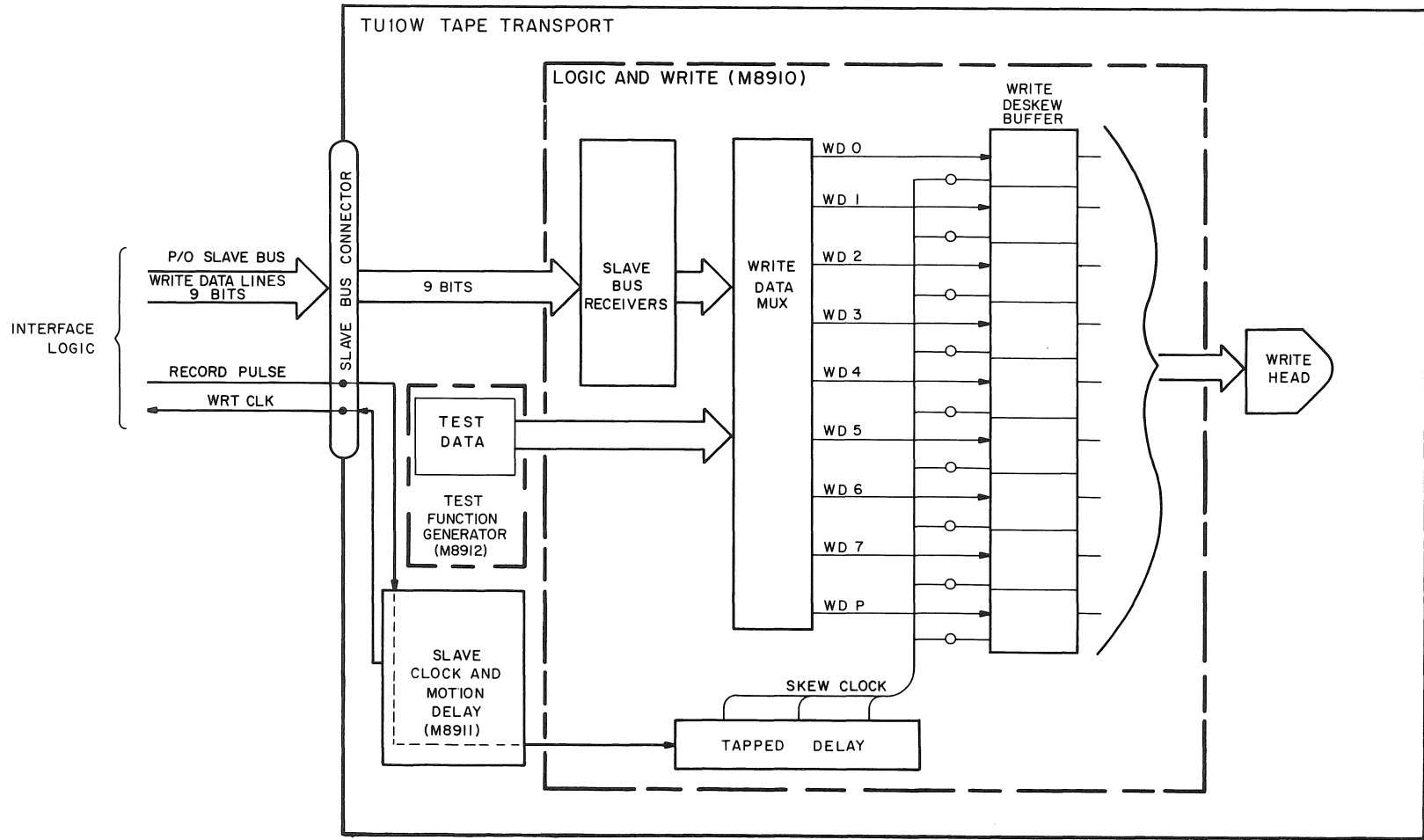
11-4676

Figure 8-5   Write Data Path

Figure 8-6   Read Data Path

```
                          ┌──────────────────┐
                          │  REMOVE POWER    │
                          └──────────────────┘
                                   │
                          ┌──────────────────┐
                          │ REMOVE TFG       │
                          │ FROM SLOT EF3    │
                          │ EXTEND MODULE    │
                          │ IN SLOT AB3      │
                          └──────────────────┘
                                   │
                          ┌──────────────────┐
                          │ PLACE WRT,       │
                          │ SS WRT, AND SS   │
                          │ RD SWITCHES      │
                          │ IN DOWN          │
                          │ POSITION         │
                          └──────────────────┘
                                   │
                          ┌──────────────────┐
                          │ RESTORE POWER    │
                          │ AND LOAD TAPE    │
                          └──────────────────┘
                                   │
                          ┌──────────────────┐
                          │ CONFIGURE S5-9   │
                          │ & S5-10 FOR      │
                          │ DENSITY          │
                          └──────────────────┘
```

Figure 8-7   TFG Operating Procedure Sequence
```
   WRITE                                    READ

CONFIGURE DATA                                              CONTINUOUS
PATTERN IN S5 &                                            READ
S6
                                     START
                                     -STOP
           START-STOP WRITE         READ
CONTINUOUS                                           INITIATE
WRITE                                                FWD OR REV
                                                     TAPE MOTION
PLACE SS RD          LOAD FRAME      LOAD FRAME       AT FRONT
SWITCH UP MO-        COUNT INTO      COUNT INTO       PANEL
MENTARILY           S4 1-8          S4 1-8
THEN DOWN
(LOADS DATA
PATTERN)

                    SET FRONT       SELECT FWD OR
                    PANEL FWD/      REV TAPE MO-
PLACE WRT           REW/REV         TION AT FRONT
SWITCH UP           SWITCH          PANEL
                    TO FWD

INITIATE FWD        PLACE SS WRT    PLACE SS RD
TAPE MOTION         SWITCH UP       SWITCH UP
FROM FRONT
PANEL

                    SET S4-9 TO ON IF
                    LONG DELAY BE-
                    TWEEN START-
                    STOP OPERATIONS
                    IS DESIRED.
                    ADJUST R23 AS
                    DESIRED
```

11-4675

Figure 8-7   TFG Operating Procedure Sequence
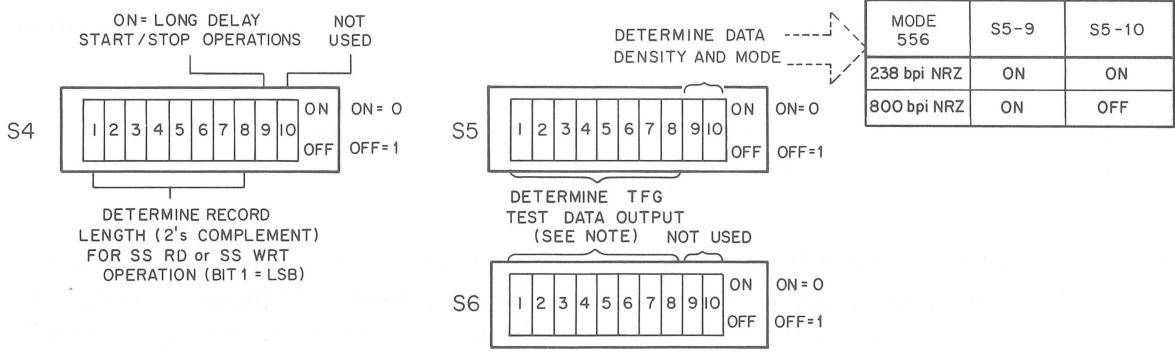
Figure 8-8 TFG Switch Settings
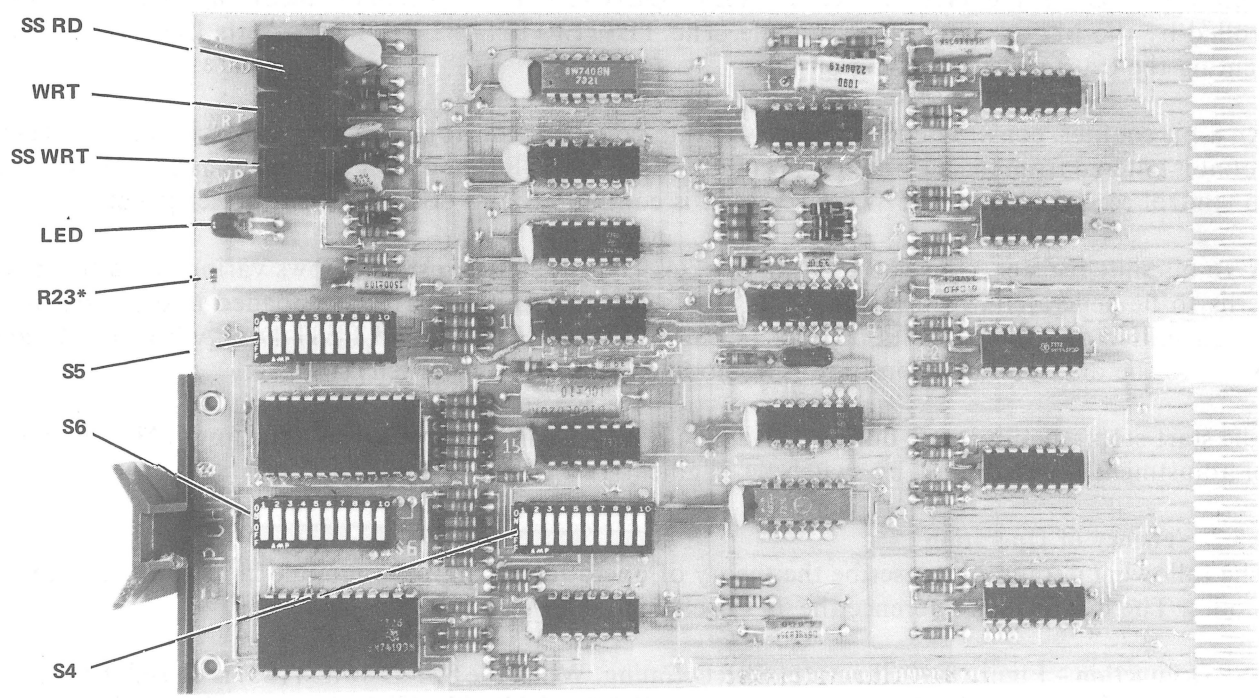
*Adjusts start-stop time.

Figure 8-9 Test Function Generator Module

As an off-line tester, the TFG module (Figure 8-9) controls tape motion, enables TU10W read and write circuitry, and generates test patterns to be written on tape. Three modes of operation are possible:

1. Start-Stop Read (SSRD) – When the SSRD switch (S3) is activated (raised), tape motion is initiated; a record of predetermined length is read; tape motion is then terminated. This cycle is repeated as long as the SSRD switch is up.

2. Start-Stop Write (SSWRT) – When the SSWRT switch (S2) is activated (raised), tape motion is initiated; a record of predetermined length, consisting of preselected characters, is written on tape; tape motion is then terminated. This cycle is repeated as long as the SSWRT switch is up.

3. Continuous Write (WRT) – When the WRT switch (S1) is activated (raised), power is supplied to the write drivers and they are continuously driven with a preselected pattern. Tape motion is controlled from the TU10W front panel.

When the tester card is located in the TU10W, location AB, the pin labeled TESTER ENABLE L is at ground potential (drawing M8912, sheet 3). This enables the TEST PE H and TEST DEN H switches. With the LED on, the TEST PE H and TEST DEN H switches affect the recording density as controlled by the M8911 slave clock module. The TESTER ENABLE L level asserts LOCAL H, preventing the transport from going on-line.

An 8-bit counter, constructed from two 74197 up-counters, controls a preset record length. The preset count is entered from the S4 switches [S4 (1–8)]. Both the SSRD and SSWRT functions use the counter to control record length. The WRT function is continuous and does not use a preset panel.

A 16-bit shift register, constructed from two 74199 8-bit shift registers, allows various data test patterns to be generated. Switches on S5 and S6 select the data pattern to be loaded into the register. When shifted out, the test data patterns (TEST DATA A H and L and TEST DATA B H and L) are wired to the data multiplex on the LAW module (M8910) and written on tape.

The start-stop repetition rate during SSRD and SSWRT can be modified by adjusting R23. The range of adjustment is determined by switch S4, segment 9.

8.5.2 Theory of Operation
The following paragraphs describe the theory of operation of the TFG module in its three functional modes. The discussions reference the TFG schematic (TFG3).

SSRD Function – Figure 8-10 illustrates SSRD timing. When the SSRD switch (S3) is closed, E1-pin 10 goes low and triggers the first one-shot delay. FIRST ONE SHOT L, input to the LAW module (M8910), initiates tape motion; the direction of tape motion is determined by the direction switch on the TU10W control box. FIRST ONE SHOT also presets the 8-bit counter (E15 and E22) and loads the 16-bit shift register (E13 and E23).
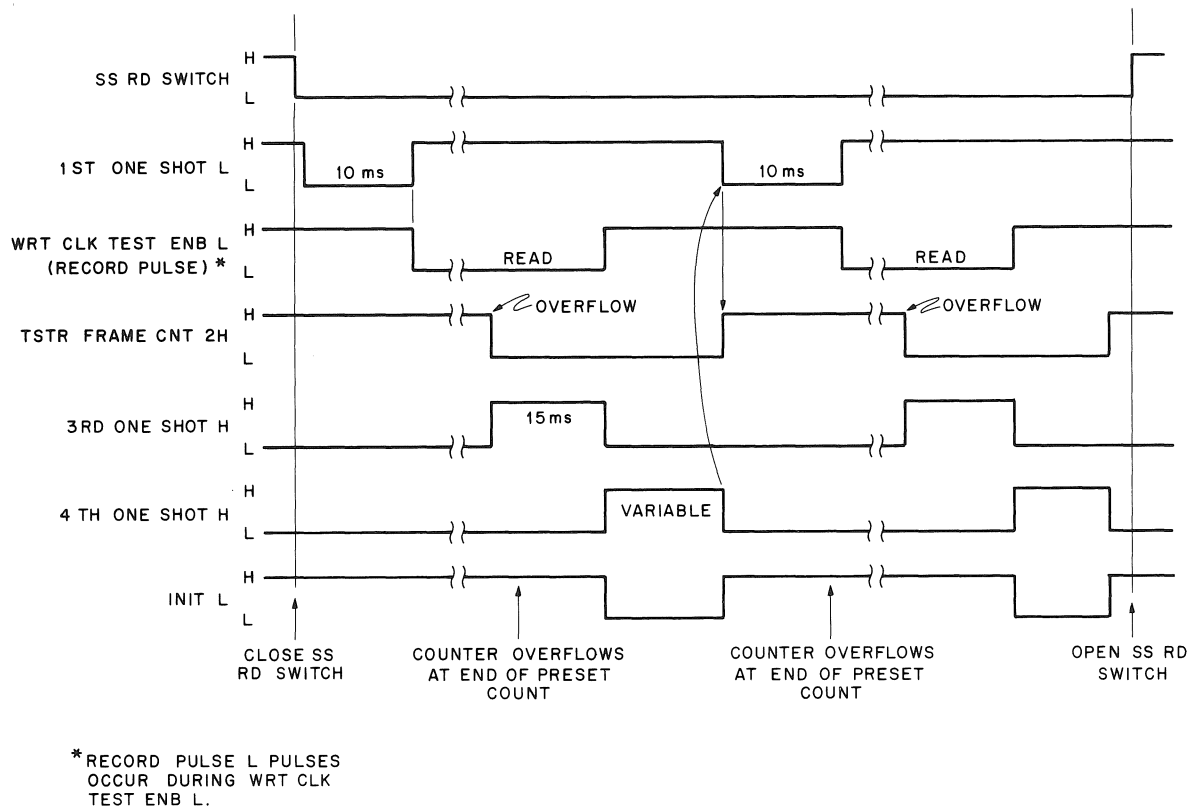
Figure 8-10   SSRD Function

When FIRST ONE SHOT times out, flip-flop E8 is clocked set and asserts WRT CLK TEST ENB L. This signal is used in the slave clock and motion delay module (M8911) to enable WRT CLK and RECORD PULSE L pulses. The RECORD PULSE L pulses now clock the TFG 8-bit counter and 16-bit shift register. When the counter overflows, the third one-shot delay is triggered and negates WRT CLK TEST ENB L, inhibiting further RECORD PULSE L pulses.

When THIRD ONE SHOT times out, FOURTH ONE SHOT H is generated, and causes tape motion to terminate. When FOURTH ONE SHOT times out, the first one-shot is again triggered; the cycle begins again. The start-read-stop cycle continues as long as the SSRD switch is depressed.

SSWRT Function – Figure 8-11 illustrates SSWRT timing. The start-stop write function operates in a manner similar to the SSRD function, except that SET TEST WRE L is asserted along with WRT CLK TEST ENB L. SET TEST WRE L causes the write and erase heads to be energized. When RECORD PULSE L pulses clock the shift register (E13 and E23), the contents of the register are rotated. The shift register outputs (TEST DATA A H and L and TEST DATA B H and L) can be jumpered to the LAW data write multiplex and written on tape.
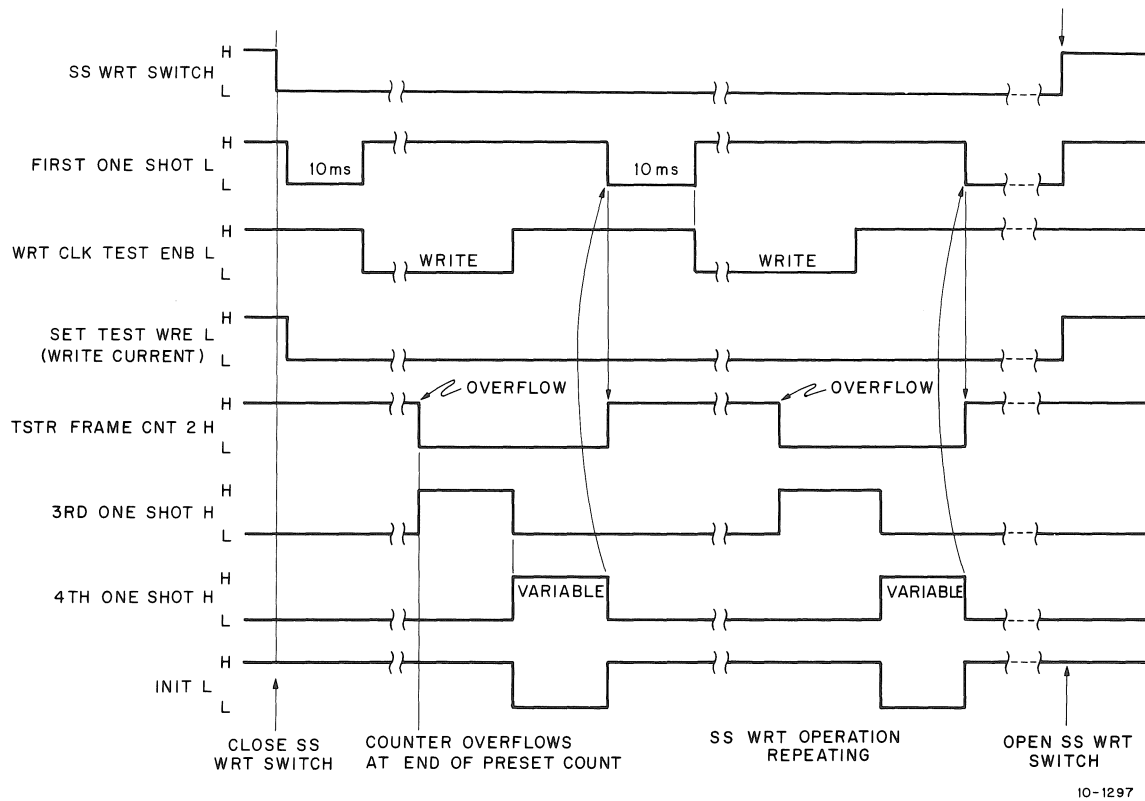
Figure 8-11   SSWRT Function

Continuous Write Function – The continuous write function works differently than the SSWRT function in that in the continuous test mode, no starting and stopping occurs. One continuous write operation commences with the setting of the WRT switch and ends with the opening of the switch. Tape motion (starting and stopping) is controlled at the TU10W control panel.

As the WRT switch is closed, WRT CLK TEST ENB L and SET TEST WRE L are asserted. This enables RECORD PULSE L pulses and passes write current to the heads. The 8-bit counters are not used in the continuous write operation. Instead, the shift registers are clocked by inverted RECORD PULSE L pulses and whatever data pattern was in the shift register switches is shifted out on the TEST DATA lines to be written and observed. The THIRD ONE SHOT delay is inhibited, which eliminates the start-stop operations.

If the operator desires a test data pattern other than the pattern presently in the shift register switches, he must first run an SSRD operation with the desired test data pattern. It is the only method for loading new information from the switches into the shift register.

The continuous write operation continues until the WRT switch is opened; this clears the WRT flip-flop and removes the write current and record pulses.

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8.6 CLOCKS
System and write clocks are discussed in the following paragraphs.

8.6.1 System Clocks
All free-running system clock waveforms used in the TU10W/controller are generated from a 2.3-MHz, crystal-controlled clock located on the TU10W slave clock and motion delay module (M8911). The 2.3- MHz clock is divided down to 144 kHz, and is transmitted to the interface logic over the slave bus [CLOCK (SB)] by an on-line, selected transport loaded with tape.

8.6.2 Write Clock
A TU10W/controller is capable of reading and writing data at several bit densities. To do this, a separate clock signal, the frequency of which depends on the tape density data, must be developed; WRT CLK is this signal. WRT CLK is transmitted to the M8926 Interface module.

The WRT CLK signal is developed in the following manner. A number is preset into a 74161 (synchronously loaded) binary counter (SC 3), which is then upcounted at 575 kHz. When the counter overflows, WRT CLK H is asserted and causes the counter to be preset at the leading edge of the next 575-kHz clock pulse. With the counter preset, WRT CLK is negated by the trailing edge of that same 575-kHz clock pulse. The counter is clocked up as before, until overflow, and the cycle is repeated.

The presets of the 74161 counter are determined by various signals and conditions. These are listed in Table 8-2, along with the resulting counter presets, WRT CLK frequency, and density.

Table 8-2   Write Clock Frequencies

	DEN 1	DEN 0	Test PE	Test DEN	WRT CLK Counter Presets LSB MSB	Frequency kHz (bpi)
On-Line	0	0	1	1	10000011	9(200)
	0	1	1	1	01010111	28(556)
	1	0	1	1	10001111	36(800)
	1	1	1	1	10001111	36(800)
	0	0	1	1	10111111	N/A
	0	1	1	1	00111111	N/A
	1	0	1	1	10111111	N/A
	1	1	1	1	10111111	N/A
Off-Line	x	x	0	0	01010011	10.7(238)
	x	x	0	1	10001111	36(800)
	x	x	1	0	00111111	N/A
	x	x	1	1	10111111	N/A

Obviously, the frequency of the cycle will vary with the magnitude of the preset. Figure 8-12 shows timing diagrams for presets of –1 (–n = 2's complement of n), –2, and –3. Note that for a preset of –n, the frequency of WRT CLK, $f_{WRT\ CLK} = [575/(n+1)$ kHz.
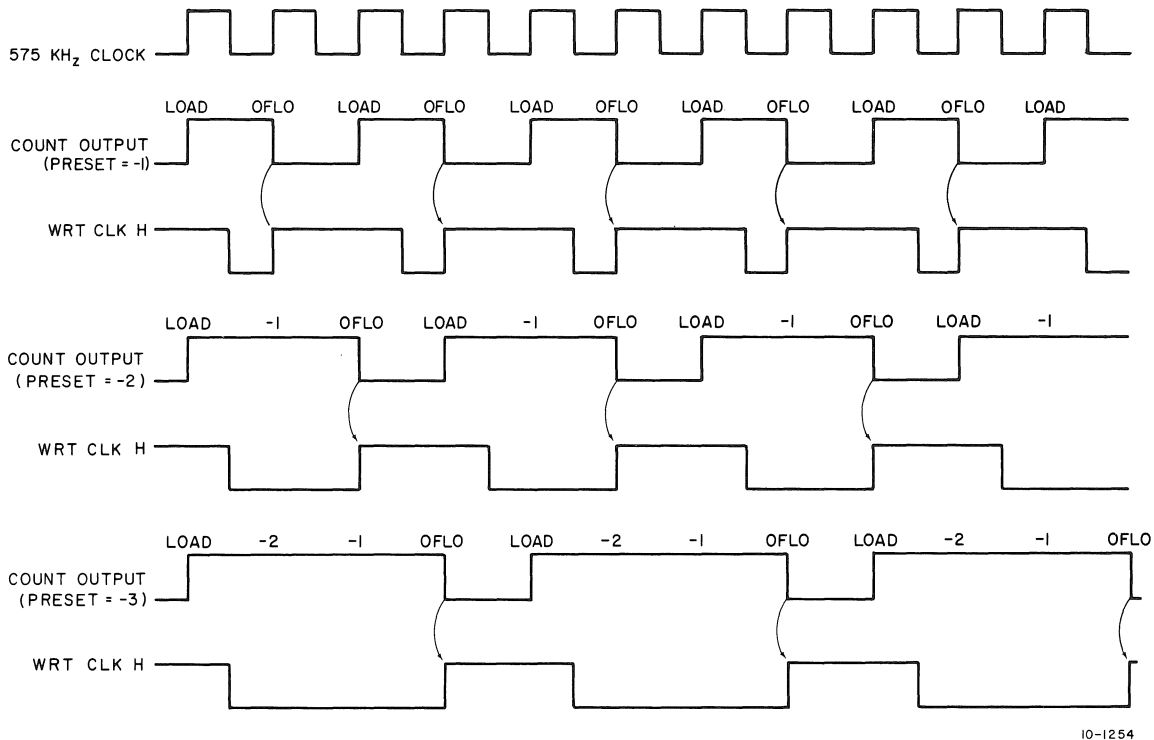
Figure 8-12   WRT CLK Generation Timing

8.7   TAPE MOTION

TU10W tape motion can be controlled by the controller via the slave bus, or by the TU10W control panel switches (Figure 8-13), depending on whether the transport is on-line or off-line. The motion control logic in the LAW module (M8910) provides proper sequencing and control during TU10W operations. It enables the vacuum motor and provides the signals that control the capstan drive circuitry.

The H606 power board contains the capstan drive circuitry and the tape reel braking and motor control circuits. The direction and velocity of capstan rotation are determined by three signals (FOR H, REV/REW H, and REWIND CAP H) from the motion control logic. These signals, therefore, determine the direction and speed of tape motion. The tape reel braking and motor control circuits activated by the vacuum switches in the vacuum columns operate to maintain a reservoir of tape within the columns. The vacuum system operates to supply tape to the capstan at constant tension.

8.7.1   TU10W Power Board (H606)

The TU10W power board (H606) is divided into two main areas: capstan servo control and driver circuits and the tape reel braking and motor control circuits; the discussions reference the H606-0-1 schematics.

```
┌──────────────────────────────────────────────────────────────────────┐
│  TU10W TAPE TRANSPORT                                                   │
│   ┌──────────────┐         ┌──────────────┐                            │
│   │  LAW         │         │   TU10W      │                            │
│   │  (M8910)     │         │  CONTROL     │              CAPSTAN       │
│   │              │ OFF-LINE│   PANEL      │              MOTOR         │
│   │──────────────│◄────────│  SWITCHES    │                            │
│   │  TAPE        │ CONTROL └──────────────┘                            │
│   │  MOTION      │  FOR      ┌──────────────────┐                      │
│   │              │ REV/REW   │ TU10W POWER BOARD │                     │
│   │              │ REWIND CAP│ (H606)           │                      │
│   │              │           │  CAPSTAN         │                      │
│   └──────────────┘           │  SERVO CONTROL   │                      │
│                              │  AND DRIVE       │                      │
│   ┌──────────────┐  VACUUM   ├──────────────────┤      REEL MOTORS     │
│   │  VACUUM      │           │  REEL BRAKE      │      AND BRAKES      │
│   │  SWITCHES    │  SWITCHES │  AND MOTOR       │                     │
│   └──────────────┘           │  CONTROL         │                     │
│                              └──────────────────┘                     │
└──────────────────────────────────────────────────────────────────────┘
```
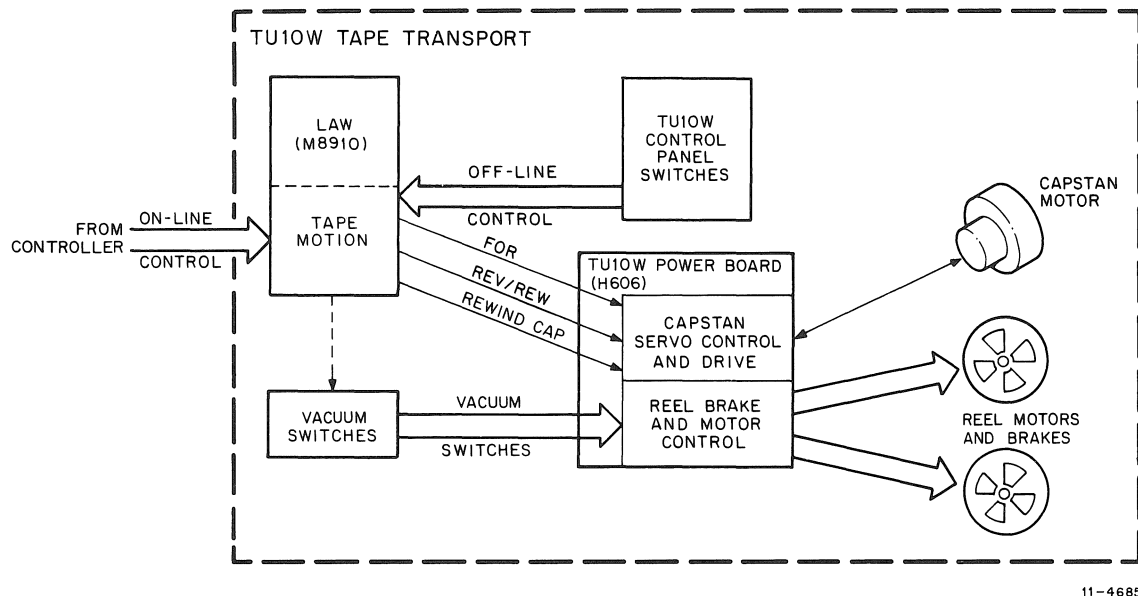
Figure 8-13   Tape Motion Control Block Diagram

8.7.1.1 Capstan Servo Control and Driver

8.7.1.1 Capstan Servo Control and Driver – The heart of the transport mechanism is the capstan subsystem, which transports the tape across the read/write/erase head assembly at the desired speed. The capstan is controlled by a velocity-feedback servo loop, shown in Figure 8-14. Refer also to sheet 3 of the H606-0-1 schematics. As a forward command enters the logic (FOR H), Q1 is biased correctly to turn on. With Q1 turned on, the voltage present at the base of Q7 is higher than the –8 V at the emitter, resulting in Q7 being turned on. If either reverse or rewind is selected, signal REV/REW H becomes true and turns Q2 on, while forward selects Q7. Notice that the collectors of both Q2 and Q7 are tied together. That output line is the running speed line going to the "–" input of the operational amplifier. Diodes D7 and D10 detect the more positive and more negative levels from Q2 and Q7, respectively, when selected. Therefore, when Q2 is on (Q7 off), D7 conducts and when Q7 is on (Q2 off), D10 conducts. Resistors R12 and R13 are the reverse and forward speed adjustments. They are each adjusted to move tape at 11.4 m (45 inches) per second.

Transistors Q8, Q9, and Q10 constitute a –8 V series regulator that biases the forward (Q7) logic. Transistors Q4, Q5, and Q6 make up a +8 V series regulator, which supplies regulated +8 V to the reverse (Q2) logic. Circuit schematic DRVR 3 (H606, sheet 3) lists test points available for checking these supplies.

The tachometer feedback signal (TACH V) is filtered and applied to the "+" input of the operational amplifier (comparator). The tachometer produces an output voltage (TACH V) proportional to the velocity of the capstan. The capstan servo amplifier (72741 at E11) compares the tachometer output with a reference voltage that is proportional to the desired capstan velocity and generates an appropriate error voltage. The error voltage (SERVO SIGNAL) is further amplified by the capstan motor driver, which drives the capstan motor. Thus, if the capstan is running slower than the desired speed, the SERVO SIGNAL and, consequently, the voltage impressed on the capstan motor increase, speeding up the capstan. If the capstan is running too fast, the capstan velocity is similarly decreased.
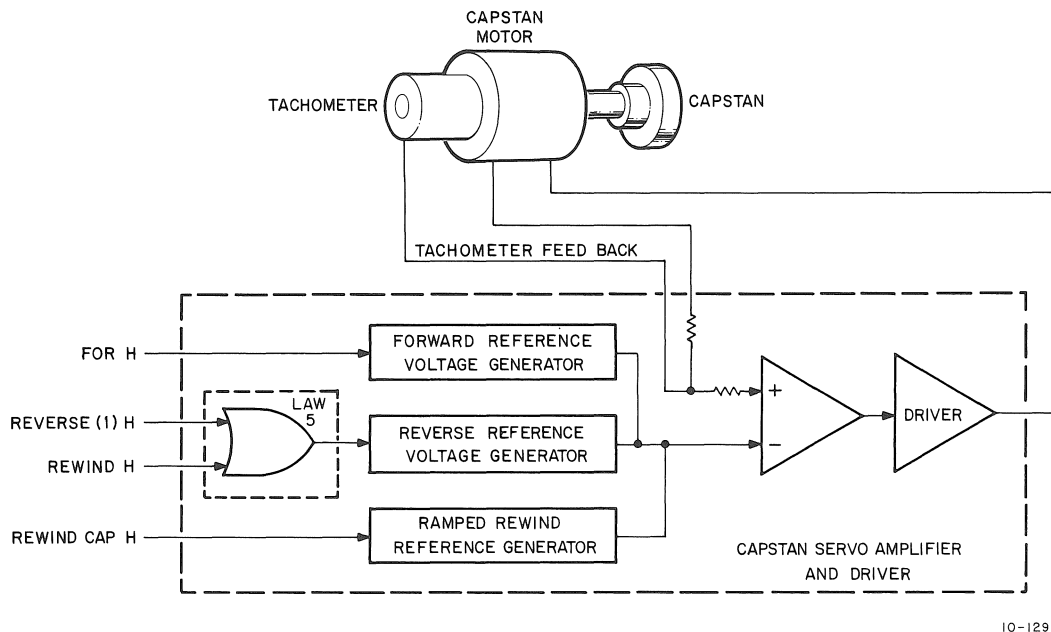
Figure 8-14   Servo Feedback Loop

When the capstan is at rest and a forward command is issued, the difference between TACH V (0 V) and the forward (Q7) circuitry is quite large. This causes the error voltage comparator to produce SERVO SIGNAL, which goes on to the driver circuitry to allow the capstan velocity to approach 1.14 m (45 inches) per second forward velocity.

Resistor R21 is the balance adjustment resistor found in the comparator feedback loop. It is adjusted for zero capstan creep with no input.

Due to the danger of "spooking" (slippage between adjacent layers of tape on the reels), which can damage tape by stretching or buckling it, the tape reels cannot be accelerated as quickly as the capstan for high-speed (rewind) operation. For normal [1.14 m (45 inches) per second forward and reverse] operation, the vacuum columns buffer enough tape to allow time for the reels to catch up with the rapid accelerations and decelerations of the capstan. However, the buffer columns cannot contain enough tape to allow the capstan to accelerate and decelerate at its normal high rates to and from the 3.81 m (150 inches) per second rewind velocity. For this reason, the rewind command logic uses two signals (REV/REW H and REWIND CAP H) to control the rewind velocity of the capstan.

When a rewind command is issued, signal REV/REW H is asserted, causing the capstan to accelerate immediately to 1.14 m (45 inches) per second just as in a normal reverse operation. Then REWIND CAP H is asserted; transistor Q3 is turned on, placing an increasing current on the running speed line. This causes a ramped rewind reference voltage generator (R10/C13 time constant) to gradually increase the rewind speed, exponentially approaching 3.81 m (150 inches) per second at a rate at which the reels can be accelerated. Resistor R11 is used to fine-adjust the rewind speed.

Refer now to sheet 4 of schematic H606-0-1. This is the circuitry that drives the capstan motor. When SERVO SIGNAL enters, it splits and goes to both the right and left sides of the drawing. Transistors Q31 and Q32 sense the SERVO SIGNAL polarity for the forward (+) and reverse (−) directions, respectively. The circuitry involving transistors Q33, Q34, and Q35 provides current amplification for the forward direction, providing MOTOR with the current necessary to drive the motor. Transistors Q36, Q37, and Q38 operate in a similar manner for the reverse direction.

The SERVO SIGNAL line also goes to the left of the drawing; diode D38 shunts a positive SERVO SIGNAL for forward and diode D39 shunts negative levels for reverse. These two diodes are connected to the collectors of the two differential amplifiers (Q24 and Q26). The current (MOTOR) through the motor and, consequently, its acceleration rate, would be functions of such loosely controlled parameters as power supply voltage, motor armature resistance (a function of temperature), and the back emf of the motor if some precautions were not taken. By current-limiting the output of the power current amplifier, the acceleration and deceleration rates of the capstan in normal (i.e., forward and reverse) operation become accurately controlled. The SERVO SIGNAL line is full of the large variations mentioned previously. Resistor R85 (0.1 ohm, 1%) in the MOTOR RETURN line senses current through the motor and supplies a feedback signal (through R94) to the bases of the Q24 and Q26 differential amplifiers. The selected amplifier (Q24 forward; Q26 reverse) limits the current to the capstan motor and keeps the current between MOTOR and MOTOR RETURN constant.

Transistor Q24 is used in the forward line; Q26 operates in the reverse. Resistor R89 is the + current adjustment used to fine-tune the forward running current, eliminating large changes in the MOTOR RETURN line. Resistor R90 adjusts negative current for reverse direction, following a similar philosophy.

8.7.1.2 Tape Reel Braking and Motor Control Circuits – Sheets 5 and 6 of schematic H606-0-1 illustrate the braking and motor control circuits. As explained in the previous paragraphs, it is necessary to buffer a small amount of tape past the read/write/erase head assembly without "spooking" the tape on the file and take-up reels. For this purpose, vacuum-buffer columns are used. The capstan does not directly move tape from one reel to another; rather, it removes tape from one vacuum column and deposits it in another. Each reel motion servo system endeavors to keep its associated vacuum-buffer column half-filled with tape, ready either to supply or to take up tape, as might be required by a sudden acceleration of the capstan.

Figure 8-15 shows the tape transport vacuum-buffer columns and the respective tape-positioning-sensing vacuum switches; this figure is referred to again later in this section. A vacuum port at the bottom of each vacuum-buffer column provides the vacuum that draws the tape loop into the column with a constant tension, independent of the position or velocity of the tape loop. This ensures a good, uniform wrap of the tape on the reel. In normal operation, the position of the tape loop in each vacuum column is sensed by a vacuum switch located near the top of each column, i.e., the upper motor upper vacuum switch (take-up reel column) and lower motor upper vacuum switch (the file reel column). These vacuum switches close when subject to a vacuum exceeding 25.4 cm (10 inches) of water and open when exposed to ambient air pressure. Thus, if the tape loop is above the upper vacuum switch in the buffer column, the switch is exposed to vacuum; the switch is then closed and its corresponding signal (UVS for the upper vacuum switches and LVS for the two additional lower vacuum switches) is at ground. If, however, the tape loop is below a vacuum switch in either column, the switch is exposed to ambient air pressure; it opens and the corresponding signal is high.

The reel servo systems endeavor to keep the respective tape loops in the brake zones (i.e., between the UVS and LVS of each column). Thus, if the capstan stops, each reel comes to rest with the tape loop in its brake zone.

TAKE-UP REEL
(UPPER MOTOR)

TAPE GUIDE

CAPSTAN

UPPER FAIL SAFE
TRANSPORT WILL
AUTOMATICALLY SHUT-DOWN
(FAIL-SAFE CONDITION)

HEAD TAPE GUIDES (2)

R/W ERASE
HEAD ASSEMBLY

UPR MOTOR UVS
TAPE WILL BE SUPPLIED TO
COLUMN (TAKE-UP REEL
TURNED OFF)

TAPE GUIDE

FAIL SAFE
TAPE SUPPLIED
TO COLUMN

UPR MOTOR LVS
TAPE WILL BE EXTRACTED
FROM COLUMN
(TAKE-UP REEL TURNED ON)

LOWER FAIL SAFE
TRANSPORT WILL
AUTOMATICALLY SHUT DOWN
(FAIL-SAFE CONDITION)

VACUUM CHAMBER
PORT

LEFT VACUUM
COLUMN

TAPE EXTRACTED
FROM COLUMN

FAIL SAFE

VACUUM CHAMBER
PORT

RIGHT VACUUM
COLUMN

FILE REEL
(LOWER MOTOR)

10-1293

Figure 8-15   Tape Transport Mechanism

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If, then, the capstan begins to put tape into a buffer, the loop moves down until it passes over the column LVS and enters the lower zone. At that point, braking is removed and a command is sent to the reel motor amplifier to accelerate the reel in order to empty tape from the buffer.

The tape loop continues to move down into the lower zone until the reel is emptying tape out of the buffer columns as fast as the capstan is putting it in. As the motor continues to accelerate the reel, the tape loop begins to move up again until it passes the LVS and enters the braking zone. The motor is then turned off and braking is again applied. The tape loop continues to move up into the brake zone until the rate at which the reel motor is removing tape from the buffer column is again equal to the rate at which the capstan is putting tape in and, as the reel continues to decelerate, the cycle repeats. Thus, the tape loop oscillates about the position of the LVS. If the capstan instead removes tape from the buffer, the tape loop similarly oscillates about the UVS as the motor and brake alternately accelerate and decelerate the reel while supplying tape to the buffer column at the average rate at which the capstan is removing it. Figure 8-15 also shows the additional fail-safe vacuum switches used. These switches, located above and below the UVS and LVS in each column, are used to detect a failure in the tape transport mechanism that threatens to damage the tape.

Figure 8-16 shows an equivalent circuit of the reel motor drive. Each reel motor is connected across a transistor bridge, which can connect the motor between the –17 V and +17 V INT power supplies in either direction. Under normal operating conditions, REEL MTR ENABLE L is asserted and the reel motor responds to control by the vacuum switch signals. When a UVS is low (closed), the reel motor is connected across the power supplies in the direction that drives tape into the buffer column. When a UVS is high (open) and an LVS is low, indicating that the tape is in the braking region, the reel motor is shut off. When both a UVS and LVS are high, the reel motor is connected across the power supply in the direction that removes tape from a buffer.
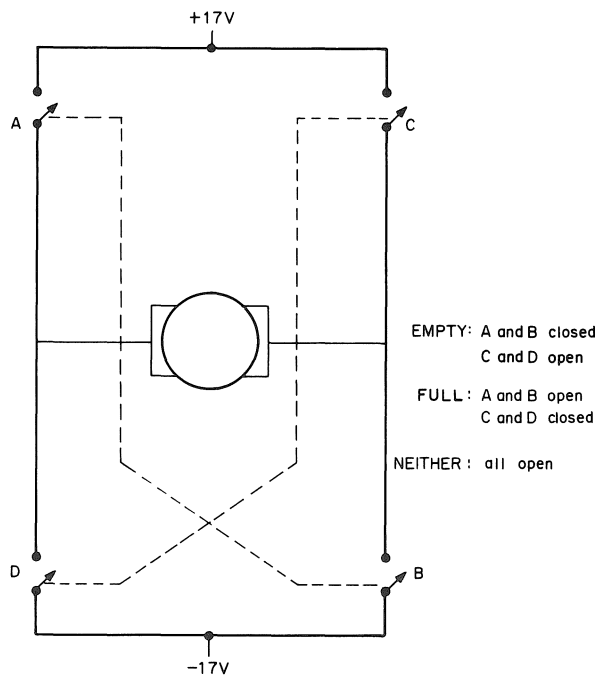
Figure 8-16   Reel Motor Amplifier Equivalent Circuit

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Each reel motor amplifier has an additional input, REEL MTR PLS H, which is used during the loading sequence to start tape into the vacuum column. The REEL MTR PLS signal is asserted during the tape loading sequence to cause the reel motor to feed a few inches of slack tape into the buffer column sealing the buffer column and allowing vacuum to build up in the column. The loading sequence is explained in more detail later.

When tape is not loaded, or when a failure is detected by the fail-safe switches, REEL MTR ENABLE L is negated, disabling the vacuum switch signals. The +17 V INT is interrupted, removing power from the reel motors.

Tape Reel Motor Control Operation – The reel motor's circuit operation still references sheets 5 and 6 of schematic H606-0-1 and Figure 8-15. Because the upper motor circuitry (take-up reel) functions identically to the lower motor circuitry (file reel), only the lower motor circuitry is detailed in this section.

Referring to Figure 8-15, notice that the file reel is associated with the right vacuum column. The column is numbered 1, 2, and 3 with respect to what happens when tape is in one of those numbered areas. The three possibilities are described in the following paragraphs.

1. Supplying Tape to the Vacuum Column – Refer to the H606-0-1 schematic, sheet 5. When tape is in position 1, both the LWR MTR UVS and LWR MTR LVS are exposed to the vacuum and are, therefore, low. This places low levels at the bases of both Q11 and Q12, keeping them turned off and resulting in high level outputs from both collectors. With both LWR MTR UPR SW (LWR MTR UVS inverted) and E1-pin 11 high, signal LWR MTR UVS/LVS is low.

    Refer to H606, sheet 6. Signal LWR MTR UVS/LVS low puts a low level at the input (base) of Q28, keeping Q28 off. This indicates the column is empty. The LWR MTR UPR SW high level and REEL MTR ENABLE low make REEL MTR PLS high at the base of Q45, turning Q45 on. The base of transistor Q43 is clamped approximately three diode drops below +17 V. The base of Q43 is lower in potential than the emitter potential, so it turns on. This results in a voltage divider network from +17 V INT down through R141, R143, and R144 to –17 V, resulting in approximately +15 V on the collector of Q43 and –15 V at the junction of R143 and R144. The +15 V is also present on the base of Q42, turning it on; –15 V on the base of Q41 turns it on. Transistor Q42 places +17 V INT on the LWR MTR RT line. Transistor Q41 places –17 V on the LWR MTR line, resulting in 34 V across LWR MTR. The LWR MTR (file reel) turns in a clockwise direction, placing tape into the right vacuum column.

2. No Action – As soon as the tape enters the area marked 2 on Figure 8-15, the UVS is no longer exposed to vacuum pressure, but instead is exposed to open air. This makes the LWR MTR UVS line high, turning on Q11 and making LWR MTR UPR SW low. With LWR MTR UPR SW low and TP8 still high, signal LWR MTR UVS/LVS remains low. Now both the LWR MTR UVS/LVS and LWR MTR UPR SW lines are low.

    The LWR MTR UVS/LVS low level keeps Q28 off. The LWR MTR UPR SW low level keeps Q45 off. With both Q28 and Q45 off, no paths are connected to drive the LWR MTR, so nothing happens (motor does not turn).

3. Remove Tape from the Vacuum Column – If tape continues to go into the right vacuum column (the capstan may be putting it in), it passes point 3. Now both the UVS and LVS are exposed to air pressure, putting ground levels at the bases of Q11 and Q12, turning them on; LWR MTR UVS/LVS becomes high and LWR MTR UPR SW becomes low. The high level of LWR MTR UVS/LVS turns Q28 on and LWR MTR UPR SW low makes REEL MTR PLS low, turning Q45 off. Transistor Q28 turned on creates a voltage divider from +17 V INT, through R120 and R119 to ground. The base of Q40 is clamped in the same way Q43 was, placing about +15 V at its base; this turns Q40 on. The approximate voltage of +15 V at the base of Q39 turns Q39 on. The –15 V at the base of Q44 turns Q44 on. Transistors Q39 and Q44 operate in a manner similar to the Q41-Q42 combination (when the tape was in position 1). However, in this instance, the +17 V INT is connected to the LWR MTR line (through Q39) and the –17 V is connected to the LWR MTR RT line (through Q44). This puts +34 V across the LWR MTR with polarity opposite that of the supplying tape case, resulting in the reel motor turning in the opposite (counterclockwise) direction and removing tape from the right vacuum column.

Take-Up Reel Operation – The theory and logic operation for supplying and removing tape from the left vacuum column (take-up reel) is almost identical to the file reel operation. The exception is that when supplying tape to the column, the take-up reel turns counterclockwise (as opposed to clockwise for the file reel), and, when removing tape, it turns clockwise.

Transistors Q47 and Q50 create the network to place +17 V INT on the UPR MTR RT line and –17 V on the UPR MTR lines, turning the UPR MTR counterclockwise to supply tape to the left vacuum column. Transistors Q46 and Q51 reverse the polarity of the voltage across the UPR MTR and turn it clockwise removing tape from the left vacuum column.

Brake Control Operation – The brake control logic is illustrated on schematic H606-1, sheet 5. The brakes used on the TU10W are electromagnetically operated friction brakes. In normal 1.14 m (45 inches) per second operation, when UPR MTR UVS is high and UPR MTR LVS is low (i.e., when the tape loop is in the braking zone), approximately 310 mA of current is driven through the brake winding. With signal UPR MTR UVS high and signal UPR MTR LVS low, UPR MTR UVS/LVS becomes low. Tracing the AND of UPR MTR UVS/LVS and UPR MTR UPR SW through, note that UPPER BRK ON H is true. This high level turns Q19 on; this turns Q18 on which, in turn, allows the Q20 current driver to apply 310 mA of current to the brake winding (as UPPER BRK OUT). This produces enough torque to rapidly stop the take-up reel.

When the tape loop moves out of the brake zone, the current is shut off. Because the braking current tends to produce a significant residual magnetism in the brakes, a short (15 ms) pulse of about 150 mA current is applied in the reverse direction when the brakes are released to ensure complete demagnetization and release of braking. As the tape moves out of the brake zone, UPPER BRK ON goes away. This low transition is ac coupled through C25 to Q21 and Q22 (as UPPER BRK ON), resulting in the short pulse. Zener diode D25 and R71 (the collector resistor) cause the smaller (150 mA) current.

During high-speed rewind, the operation of the brake circuitry must be modified somewhat to avoid stopping the reel whenever the tape loop enters the braking zone. Without this modification, the reel motor could not accelerate the reel to 38.1 m (150 inches) per second rapidly enough to prevent failure. For this reason, when REWIND CAP H is asserted and the tape loop enters the brake zone, only a short pulse of braking is applied to the reel to slow it down but not to bring it to a halt. In the case of the take-up reel servo, if the tape loop remains in the braking zone longer than about 50 ms, a low current of about 60 mA is applied to the brake, further decelerating the reel. As REWIND CAP H becomes asserted, signal LOW REWIND BRK L is asserted, placing a low level input to the base of Q23. This turns Q23 on and allows Q20 to pass an additional low current out UPPER BRK OUT. In the case of the lower (file) reel, this additional stop current is not necessary. The file reel brake control logic otherwise operates identically to the take-up reel braking system. Signal LOWER BRK OUT is the line to the file reel brake coil. The path for normal braking (when LOWER BRK ON high is asserted) is through transistors Q15 and Q16 to drive 310 mA out of the LOWER BRK OUT line. To compensate for the residual magnetism in the brake coil, when LOWER BRK ON is negated, the LOWER BRK ON low transition is ac coupled through Q53, allowing Q17 to apply the necessary reverse current to LOWER BRK OUT.

The difference in braking of the two reel systems occurs because the upper reel is dumping tape into the buffer during rewind and is, therefore, accelerated by torque resulting from the tape tension produced by the vacuum column. The lower reel, however, is removing tape from its buffer and, therefore, the tape tension tends to decelerate the lower reel, making low drag braking unnecessary.

Figure 8-17 shows the brake current waveforms of each reel system during both 11.4 m (45 inches) per second and rewind operations. Whenever tape is not loaded or the fail-safe switches detect a failure, and the LOAD/(OFF)/BR REL switch is not in the BR REL position, signal FORCE BRK ON low is asserted. This signal causes high (310 mA) braking to be applied to both reels, regardless of the signals from the vacuum switches.
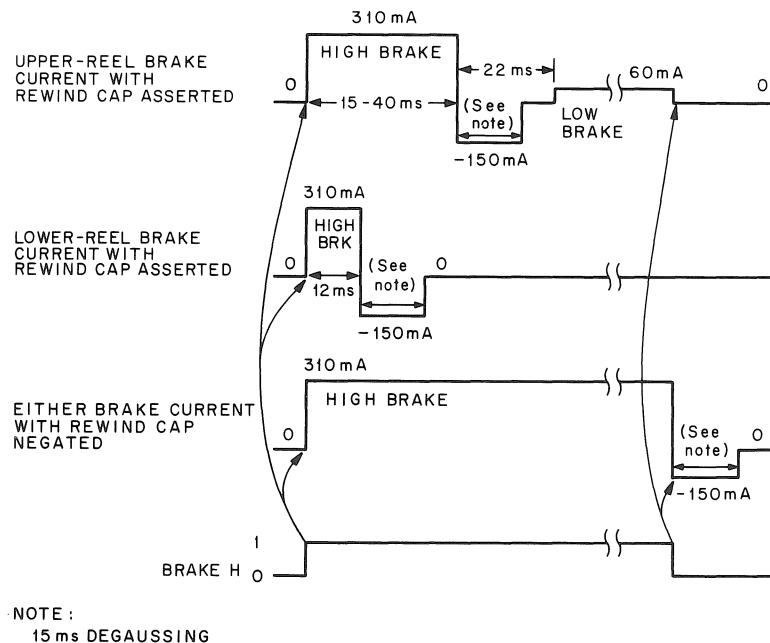
Figure 8-17   Brake Current Waveforms

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8.7.2 Motion Control Logic

The motion control logic, shown on the M8910 (LAW) drawings, provides the necessary sequencing and control for loading tape rewinding, brake release, and shutting down the TU10W if power or the tape unit itself should fail. Its main sections are listed and explained below.

Power Clear – The power clear circuitry consists of a power transient detector and one-shot. When the +5 V power supply is turned on, the circuit produces P CLR L, which produces LOCAL H; this produces a 15-ms clear pulse (DELAYED LOCAL L) that resets all of the various status flip-flops of the TU10W to the idle, unloaded, off-line condition, keeps all motors turned off, and asserts braking on the reels. Similarly, when the +5 V power supply drops to approximately 4.4 V, a PWR CLR pulse is produced that lasts for 20 ms, or until the power supply drops too low to operate the power clear circuitry (approximately 3 V).

Servo System Failure Detection – As explained in previous text, two fail-safe switches, located in each vacuum-buffer column, define the permissible limits of excursion of the tape into those columns. If the tape loop in either buffer column goes below the lower fail-safe switch, the switch opens and LFS H is asserted. If either tape loop is above its upper fail-safe switch, then UFS L is asserted. When VACUUM ON (0) L is asserted, indicating that tape is loaded, and either LFS H goes to 1 or UFS L goes to 0, then the FAIL flip-flop (LAW 5) is set. The effect of FAIL (1) is essentially the same as that of the CLR PLS pulse, except that FAIL (1) is a level and remains asserted, preventing tape unit operation until manually reset by moving the LOAD/(OFF)/BRK REL switch to its central OFF position.

Loading Sequence Logic – Initiation and shutting down of the reel motors, brakes, and function control logic is controlled by the loading sequence logic. The loading sequence logic consists of the RELAY ENABLE flip-flop, the REEL MTR ENABLE L and VACUUM ON L one-shots, and their associated gating. The RELAY ENABLE flip-flop is reset by either FAIL (1) or the LOAD/(OFF)/BRK REL switch being in the OFF position. When RELAY ENABLE is reset, the vacuum motor is turned off. Also, the power supply interrupts PWR COM INT and +17 V INT, which turns off power to the reel and capstan motors. The REEL MTR ENABLE L one-shot is held to its 1 state, negating REEL MTR ENABLE L; the VACUUM ON L integrating one-shot is held to its 1 state, negating VACUUM ON L. These prevent the function control logic from responding to any command.

The RELAY ENABLE flip-flop is set by LOAD PULSE L, a pulse produced when the LOAD/(OFF)/BRK REL switch is brought to the LOAD position. When the RELAY ENABLE flip-flop is set, the vacuum motor is turned on; RELAY ENABLE L is asserted, clearing FORCE BRK ON and generating REEL MTR PLS (H606, sheet 6). Both PWR COM INT and +17 V INT are restored. Signal REEL MTR PLS causes each reel motor to dump a small amount of tape into the top of its buffer column, sealing it and allowing vacuum to build up in the column. When the lower fail-safe switches in both vacuum columns sense vacuum, the REEL MTR ENABLE L and VACUUM ON L delays are allowed to begin timing out. Approximately 100 ms is allowed for the vacuum to build up and stabilize before the REEL MTR ENABLE L one-shot times out, asserting REEL MTR ENABLE. When REEL MTR ENABLE is asserted, the reel servos can function normally, bringing the tape loops to the middle of the buffer columns.

Approximately 3 seconds later, the VACUUM ON L one-shot times out, asserting VACUUM ON. This allows the function control logic to accept commands and also enables failure detection. The tape loading sequence is then complete, and the transport remains loaded until the RELAY ENABLE flip-flop is reset.

Brake Release – When the FORCE BRK ON flip-flop is set, full braking is applied to both reels. It is set whenever the RELAY ENABLE flip-flop is reset, and is cleared whenever RELAY ENABLE is set. The FORCE BRK ON flip-flop can also be cleared by BRK REL SW L, the signal asserted when the LOAD/(OFF)/BRK REL switch is in the BRK REL position, provided that LFS H is asserted. Thus, the lower vacuum switches prevent brake release until the vacuum has drained out of the buffer columns. Moving the LOAD/(OFF)/BRK REL switch from BRK REL to the center OFF position causes RELAY ENABLE L to be asserted, again setting the FORCE BRK ON flip-flop.

Rewind Control – Due to the limited rate at which the reels can be accelerated and decelerated, a special sequence of control signals must be generated to perform a high-speed rewind operation. The sequence is shown in Figure 8-18. When the function control logic accepts a rewind command, it asserts (see drawing LAW 7) signal SET RWD CMD L, which direct sets the RWS flip-flop.
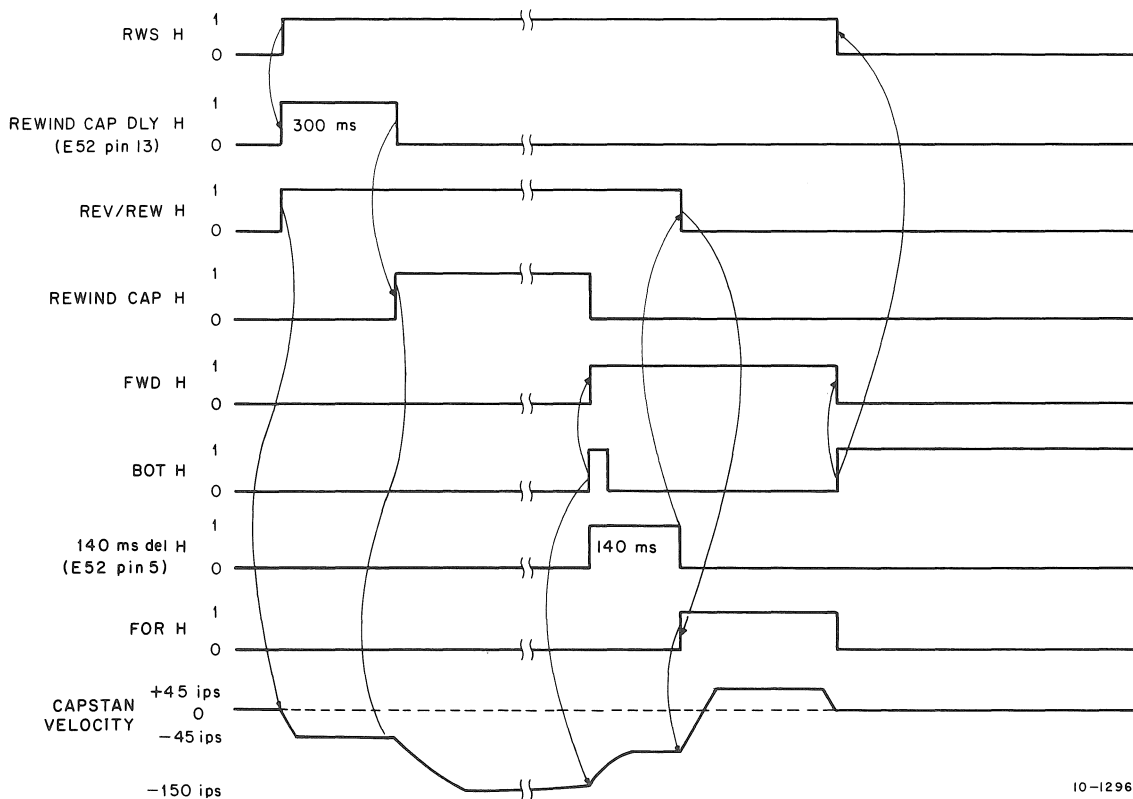
Figure 8-18   Rewind Sequence Timing

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A high level is presented to the pin 12 input of the 7400 gate in location E41 (LAW 5). This asserts signal REV/REW H, which accelerates the capstan servo to 11.4 m (45 inches) per second in the reverse direction. At the same time, RWS H triggers a 300-ms delay, which allows the reels to stabilize at 11.4 m (45 inches) per second. When the delay times out, it asserts signal REWIND CAP H. The REWIND CAP H signal causes the capstan servo to gradually accelerate to 38.1 m (150 inches) per second in the reverse direction.

Normally, rewinding continues until the function control logic detects the beginning-of-tape (BOT) marker. When BOT is detected, the function control logic asserts FWD L (LAW 7) and removes REWIND CAP H. The assertion of FWD L triggers the 140-ms delay (enabled by RWS H). Normal braking is applied and the capstan servo gradually decelerates toward 11.4 m (45 inches) per second, still traveling in the reverse direction past BOT.

When this delay times out, the forward command is passed on to the capstan servo as FOR H (LAW 5). The capstan accelerates from 11.4 m (45 inches) per second in the reverse direction to 11.4 m (45 inches) per second forward. The tape then moves forward until the BOT marker is again detected. At this point, the function control logic clears FWD L, FOR H, and RWS H, and the capstan comes to a stop, terminating the rewind.

The rewind control logic is designed so that if the rewind is terminated at any point in the sequence, the operation stops without failure and without danger of "spooking" the tape.

Tape Unit Ready and Transport Settling Down – The RUNNING H and signals indicate whether the transport is idle (ready to begin an operation) or settling down (coming to a halt after performing an operation). When the tape transport is on-line and selected by its controller, it transmits the signals to the controller to notify the controller when it is able to accept another command.

Whenever an operation is being performed, the function control logic asserts MOTION H. The OR of MOTION H (operation in progress) and LOCAL H (unit off line) sets the RUNNING H one-shot delay (LAW 5), thereby asserting RUNNING H and also inhibiting the settle-down signal, SDWN (SB) L. When both MOTION H and LOCAL H are negated, the RUNNING H one-shot begins to time out and SDWN (SB) L is asserted, indicating the transport is ready to accept a command to move tape in the same direction as the previous command. After approximately 13 ms, when the capstan has had time to come to a complete stop following any previous operation, the RUNNING H one-shot times out, negating SDWN (SB) L and, provided MOL H is asserted, asserting Tape Unit Ready [TUR (SB) L], thereby indicating that the unit is ready to accept any command.

8.7.3 Manual Control Operation
Manual operation of the TU10W Tape Transport is effected by the operator control box switches. The detailed operation of each of the switches is explained in this section.

LOAD/(OFF)/BR REL – This switch has three operations. In its center, or OFF position, signal OFF L is asserted to clear the FAIL and RELAY ENABLE flip-flops. When the switch is brought to the LOAD position, signal OFF L is negated and LOAD PULSE L is asserted for a few microseconds, setting RELAY ENABLE H and initiating the tape loading sequence. When the switch is brought to the BR REL position, OFF L is asserted again and the BRK REL SW signal is asserted low for brakerelease. For a more detailed explanation of these operations, see the relevant sections of Paragraph 8.7.2.

ON-LINE/OFF-LINE – When this switch is quiescent in either position, no output occurs to change the state of the transport. When it is moved from the ON-LINE to the OFF-LINE position, OFF LINE SW is momentarily asserted low, setting LOCAL H (LAW 6). When the ON-LINE/OFF-LINE switch is moved from its OFF-LINE to its ON-LINE position, ON LINE SW is asserted low momentarily, negating LOCAL H.

Unless a rewind operation is in progress, the assertion of either OFF LINE SW L or ON LINE SW L causes the assertion of INIT L (LAW 8). The assertion of INIT L clears the FWD, RWS and REV flip-flops and brings tape motion to a halt.

The LOCAL signal controls the operating mode of the TU10W Tape Transport. When LOCAL L is negated, the transport is on-line and all operations of the transport are directed by the controller via the slave bus (SB). When LOCAL H is asserted, the transport is off-line and is, effectively, isolated from the slave bus. In this mode, tape motion is controlled by the FWD/REW/REV and START/STOP switches, as discussed below.

FWD/REW/REV – This 3-position switch selects the direction of tape motion for off-line operations (LAW 7). When it is in the FWD position, MANUAL FWD L is asserted; in the REW position, MANUAL REW L is asserted; and in the REV position, MANUAL REV L is asserted. These signals do not initiate tape motion, but are strobed by the START L pulse as explained below.

START/STOP – When this switch is moved from its START position to the STOP position, signal STOP L is asserted for a few microseconds. If the transport is off-line (LOCAL H asserted), this causes a corresponding pulse at INIT L, clearing the FWD, REW, and REV flip-flops and bringing tape motion to a halt. When the START/STOP switch is moved to the START position, START L is asserted, directly setting a flip-flop (at coordinates D-7 of drawing LAW 7). The high-going transition of this flip-flop is ANDed with LOCAL H (transport off-line) and MOTION L (no operation in progress) to produce a pulse that strobes the MANUAL FWD, REV, and REW lines in an 8266 multiplexer. The assertion of one of these lines causes the FWD, REV, or RWS flip-flop to be set, initiating tape motion in the indicated direction. Note, however, that if BOT H is asserted, the signal that sets the RWS flip-flop is gated off because the tape is already at BOT. Note also that if END PT H is asserted and FWD H is set, then INIT L is asserted to clear the FWD flip-flop and prevent running off the end of the tape.

8.7.4 Tape Unit Status Sensors
The tape status (EOT/BOT) and write lock sensor features are discussed in this section.

EOT/BOT Sensor – To locate the beginning and end of the recording area on the tape, the load and end points are marked by reflective strips mounted on the nonoxide side of the tape. The dimensions and placement of these strips are shown in Figure 8-19.

The strips are detected by the phototransistors of the EOT/BOT sensor assembly. The EOT/BOT assembly is located in the wall of the lower vacuum column. It consists of an EOT sensor phototransistor, located to detect light reflected from the EOT strip; a BOT sensor phototransistor, located to detect light reflected from the BOT strip; and two light-emitting diodes (LEDs), which illuminate the EOT and BOT strips. The LEDs operate in the infrared region and, therefore, produce no visible light. The outputs of the EOT/BOT assembly are amplified, filtered, and converted to logic levels, as shown on drawing M8910 (LAW), sheet 6, producing signals BOT (SB) L, END PT H, and END PT (SB) L.
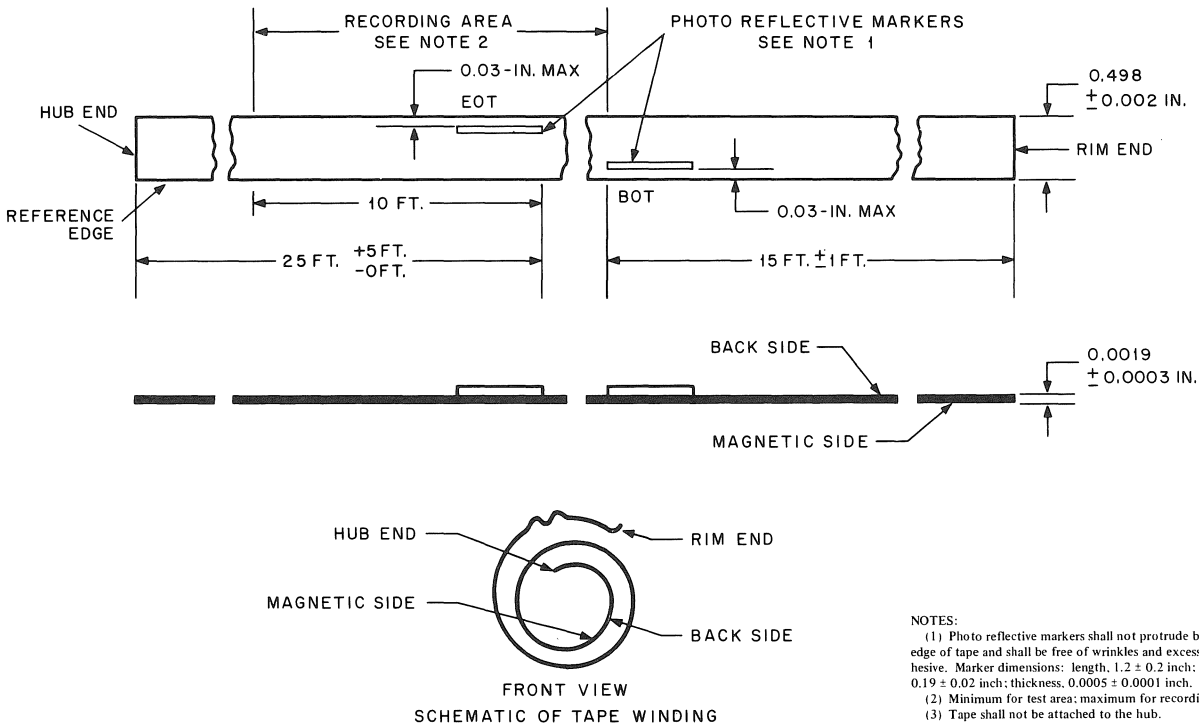
Figure 8-19   Tape Markers, Recording Area, and Tape Wind

The assertion of END PT H sets a flip-flop that remains set until either the tape is rewound or EOT is negated while the tape is traveling in the reverse direction. Thus, if the tape is moved forward past the EOT marker, the END PT flip-flop remains set even after the marker is passed and is cleared only by rewinding or reversing the tape back past the EOT marker. Setting the END PT flip-flop has the following effects:

1.   If the TU10W is off-line (LOCAL H asserted), forward tape motion stops and the transport does not accept manual forward commands until the tape is rewound or reversed off the EOT marker.

2.   The End Point indicator lamp is lit.

3.   If the TU10W is on-line and selected by the controller, the TU10W signal END PT (SB) L is asserted, indicating to the controller that it has passed the end point.

NOTE
Notice that if the TU10W is on-line, it does not stop automatically upon detecting EOT. It is permissible to write data up to 3 m (10 ft) past the end point. It is up to the program to ensure that the tape does not run past this point.

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The assertion of BOT H has the following effects:

1. The TU10W accepts no new rewind commands.

2. When the TU10W rewinds into BOT (i.e., RWS H is asserted, FWD L is negated, and BOT H becomes asserted), the FWD flip-flop is set (drawing LAW 7); refer also to the description of rewind operation, Paragraph 8.7.2.

3. When the TU10W moves forward into BOT, the FWD flip-flop is cleared. (If the RWS flip-flop is set at this time, clearing FWD also clears RWS, terminating the rewind sequence.)

4. The LD PT indicator is lit.

5. If the TU10W is on-line (i.e., LOCAL L negated) and selected by the controller, it asserts the transport bus signal BOT (SB) L, indicating to the controller that it is at BOT.

Write Lock – To protect tapes from inadvertent erasure, tape reels are provided with a write enable ring. If a reel of tape is mounted on the TU10W Tape Transport with its write enable ring removed, this condition is sensed and the transport refuses to honor any write commands. Further, if the transport is on-line and selected by its controller, it asserts WRL (SB) L to the controller, indicating to the controller that it is write-locked.

The physical write-lock assembly consists of the write-lock solenoid and the write-lock switch. When no write enable ring is inserted in the file reel, a feeler attached to the end of the solenoid shaft extends into the write-lock slot on the back of the reel. This feeler puts the write-lock switch in its normally closed position, asserting WR LOCK L (drawing LAW 8). When a write enable ring is inserted in the file reel, the ring pushes back the solenoid shaft, actuating the write-lock switch and negating WR LOCK L. If the write enable switch is actuated, +17 V INT is turned on (i.e., when tape is loaded in the buffer columns) and the write-lock solenoid is engaged and withdraws the write-lock feeler from contact with the ring. This keeps the write-lock switch actuated until the tape is unloaded and reduces wear of the write-lock assembly and write enable ring during tape unit operation.

8.7.5 On-Line Operation
When signal LOCAL L is negated, the TU10W is on-line. In this state, all transport operations are directed by the controller via the slave bus. The slave bus connects the controller to up to eight TU10W Tape Transports.

8.7.5.1 Transport Selection and Status Reporting
– All of the tape transports in a system communicate with the same slave bus, but only one transport can be logically connected to the bus at one time, i.e., only one transport can transmit its status to the controller and respond to commands, and only one transport can be reading or writing data at a given time.

To select the particular tape transport to converse with the tape controller, the controller transmits a binary code on bus lines SEL 1 L, SEL 2 L, and SEL 4 L. As shown on drawing M8910 (LAW), sheet 6, each transport on the bus compares this code to the transport number determined by the unit select plug (signals SW1, SW2, and SW4). If the selection code transmitted by the controller matches the transport number, and the transport is on-line, the SELECT lamp lights and the transport logically connects itself to the slave bus. All other transports remain logically disconnected and neither transmit nor respond to bus signals.

When a particular transport is logically connected to the slave bus, it transmits status information to the tape control as follows:

7CH (SB) L	Asserted when a 7-track tape drive has been selected.
BOT (SB) L	Asserted when the tape is positioned at load point (beginning of tape).
END PT (SB) L	Asserted when the End Point flip-flop is set.
WRL (SB) L	Asserted when the TU10W Tape Transport is write-locked.
RWS (SB) L	Asserted when the Rewind Status (RWS) flip-flop is set.
SDWN (SB) L	Asserted when the transport is settling down following an operation, i.e., asserted for about 13.5 ms following the command to terminate an operation while the capstan is coming to a halt.
TUR (SB) L	Asserted when the tape unit is ready to receive any command, i.e., when the transport is neither performing an operation nor settling down following an operation.

8.7.6 Tape Motion Initiation (On-Line)
Refer to Figures 8-20 and 8-21 while reading this section.
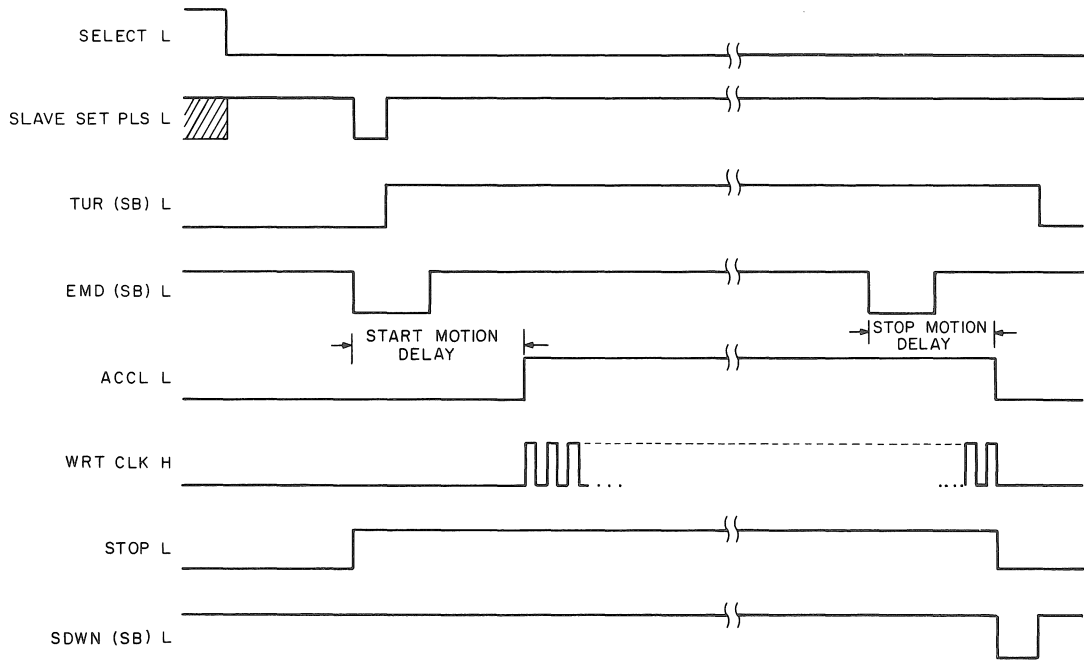
11-4688

Figure 8-20   Tape Motion Timing

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CONTROLLER   TU10W

```
┌─────────────┐
│   CONTROL   │
│  REGISTER   │
│   LOADED    │
│ (GO BIT SET)│
└─────────────┘
       │
       ▼
┌─────────────┐
│  SET PULSE  │
└─────────────┘
```

INTERFACE

```
┌─────────────┐
│ SLAVE SET   │
│   PULSE     │
└─────────────┘
```

```
     ╱╲                    ╱╲                              ╱╲
    ╱  ╲                  ╱  ╲                            ╱  ╲
   ╱ SB ╲  NO            ╱ SB ╲  NO                      ╱ SB ╲  NO
  ╱ FWD  ╲──            ╱ REV  ╲──                      ╱RWND  ╲──
  ╲ASSERTED╱           ╲ASSERTED╱                       ╲ASSERTED╱
   ╲  ?  ╱              ╲  ?  ╱                          ╲  ?  ╱
    ╲  ╱                 ╲  ╱                             ╲  ╱
     YES                  YES                              YES
```

```
┌─────────────┐
│   ENABLE    │
│   MOTION    │
│   DELAY     │
└─────────────┘
```

SB WRITE ASSERTED ?   NO

SB WRITE ASSERTED ?   NO   YES

YES

```
┌─────────────┐  ┌─────────────┐  ┌─────────────┐  ┌─────────────┐  ┌──────────────┐
│ SET FWD  FF │  │ SET REV FF  │  │ SET RWS FF  │  │SET LOCAL FF │  │SET WR ENAB FF│
└─────────────┘  └─────────────┘  └─────────────┘  └─────────────┘  └──────────────┘
```

```
┌─────────────┐  ┌─────────────┐                   ┌─────────────┐  ┌──────────────┐
│  GATE OUT   │  │GENERATE FOR,│                   │ PLACE TU10W │  │ENERGIZE WRITE│
│MOTION DELAY │  │ REV/REW &   │                   │  OFF-LINE   │  │ & ERASE HEADS│
│  PRESETS    │  │ REWIND CAP  │                   └─────────────┘  └──────────────┘
└─────────────┘  └─────────────┘
```

```
┌─────────────┐                   ┌─────────────┐
│ LOAD MOTION │                   │DRIVE CAPSTAN│
│DELAY COUNTER│                   │   SERVO     │
└─────────────┘                   └─────────────┘
```

```
┌─────────────┐
│  COUNT UP   │
│  UNTIL BIT  │
│   14 SETS   │
└─────────────┘
```

```
┌──────────────┬─────────────┐
│              │   ASSERT    │
│ NEGATE ACCL L│  READING L  │
└──────────────┴─────────────┘
```

11-4687

Figure 8-21   Tape Motion Initiation Flowchart

If a TU10W is selected, on-line, and loaded with tape (MOL H asserted), it responds to DRV SET PLS and the FWD, REV, and RWND command lines of the slave bus by setting the corresponding motion control flip-flops [i.e., FWD, REV, and RWS (rewind status) flip-flops on LAW 7]. If the WRITE command line is asserted, along with the RWND command line, SET OFFLINE L is generated, setting the LOCAL flip-flop (LAW 6). If WRITE is asserted but RWND is not, SLAVE SET PLS produces SET WRE (Set Write Enable), which sets the WR ENAB flip-flop (LAW 8).

The outputs of the Motion Control flip-flops produce FOR H, REV/REW H, and REWIND CAP H (LAW 5) signals, which control the capstan servo and drive circuits as described in Paragraph 8.7.1.1. At the same time, the WR ENAB flip-flop, if set, generates WRITE ENABLE H, which shunts WRITE voltage to the write and erase heads, thereby energizing the heads. This causes tape to be erased, generating IRG as the tape comes up to speed and the start motion delay times out. Simultaneous with motion initiation, EMD L gates the motion delay presets onto the read data lines of the slave bus (SC 2) and loads them into a motion delay counter in the interface logic. When EMD L is negated, the counter is upcounted until bit 14 sets, at which time ACCL H and READING L are asserted, and further clocking is inhibited. The presets of the counter determine the time interval necessary to reach the count, and hence the duration of the motion delay. When write extended IRG or write tape mark operation is performed, the presets to the motion delay may be modified. Modification occurs only when starting in the forward direction, not from BOT (E60 pins 3, 4, 5, and 6); this produces an extended IRG on tape. The presets depend on the type of operation performed (read/write), the direction of tape motion, and other parameters. Table 8-3 lists the motion delays generated under the various conditions. READING L enables the read circuitry in the interface logic. ACCL L is transmitted to the TU10W, where it enables generation of WRT CLOCK and other read and write functions.

Table 8-3 Start and Stop Motion Delays

| Start/Stop | Mode | Operation Times (ms) | |
		9-Track	7-Track
Start Motion Delays	Write from BOT	184.60	200.70
	Write	8.99	15.26
	Read from BOT	150.60	86.94
	READ/SPACE FWD/SPACE REV	2.72	0.924
Stop Motion Delays	WXG/WFMK/WRITE	2.72	2.72
	READ/SPACE FWD/SPACE REV	1.82	1.82

Once forward or reverse tape motion is initiated, it continues (unless a TU10W mechanical or power failure is sensed) until the interface logic transmits STOP L asserted to the transport.

If a rewind operation is being performed, STOP L is asserted as soon as SLAVE SET PLS is negated. However, since the Rewind Status flip-flop is already set, this does *not* produce an INIT L pulse (LAW 8) and does not terminate motion. Once the Rewind Status flip-flop is set, the TU10W performs the rewind operation independently, as described in Paragraph 8.7.2. The TU10W notifies the controller that it is performing a rewind by asserting RWS (SB) L on the slave bus. When the rewind control sequence is over, motion terminates automatically.

8.7.7 Tape Motion Termination (On-Line)
The TU10W terminates tape motion when an INIT L pulse (generated on LAW 8) clears the Motion Control flip-flops (LAW 7). Several sequences cause this to happen, depending on the type of operation being performed (Figure 8-22). The various sequences are discussed in the following paragraphs.
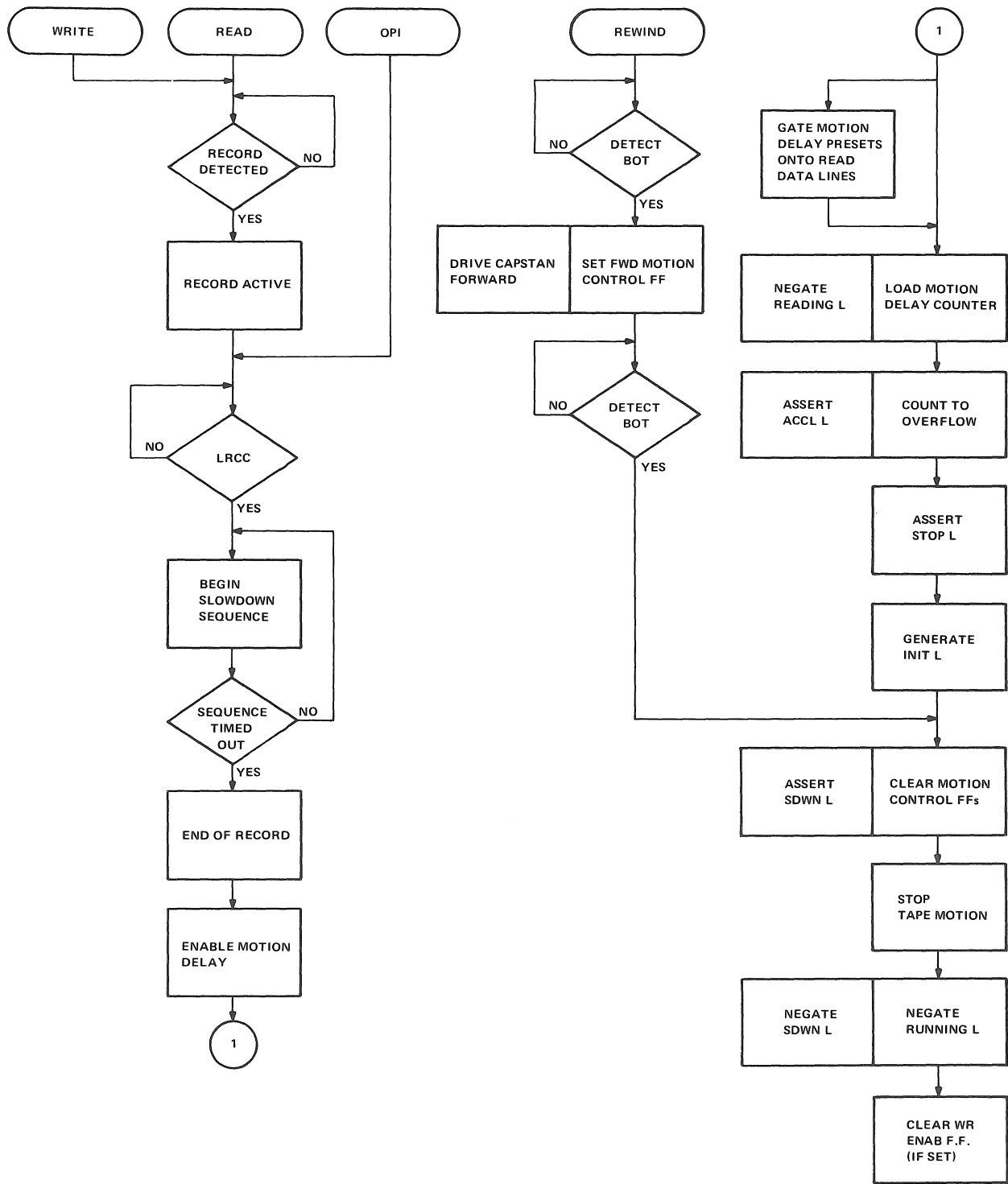
Figure 8-22 Tape Motion Termination Flowchart

11-4668

8.7.7.1 Read – During a read operation, the motion termination sequence begins when the drive receives a STOP pulse. An explanation of how the controller shutdown sequence functions is provided in the interface logic theory section of this manual.

At the completion of the shutdown sequence, STOP L is asserted and transmitted to the TU10W. STOP L produces the INIT L pulse (LAW 8), which clears the FWD or REV Motion Control flip-flop and thereby causes the capstan activating signal to be removed. As tape motion slows down, SDWN L is asserted by the TU10W and transmitted to the controller. When tape motion stops, RUNNING H is negated, while TUR L is asserted and transmitted to the controller.

8.7.7.2 Write – Motion termination during a write is almost identical to that during a read. When tape motion ceases, RUNNING L is negated and clocks the WR ENAB flip-flop clear, thereby de-energizing the write and erase heads.

8.7.7.3 Space – Termination during a space is similar to that of a read. Each time an LRCC is detected, a stop motion delay is generated and STOP L is transmitted to the TU10W, clearing the Motion Control flip-flop. However, once the drive begins to slow down, a start motion delay is triggered. This causes the Motion Control flip-flop to be set once again. Thus, start motion delays and stop motion delays are produced as each record is spaced.

8.7.7.4 Rewind –Once the RWS flip-flop in the TU10W is set, the transport independently performs the rewind operation. The transport rewinds past the BOT marker, then spaces forward until it encounters the BOT marker again. This causes INIT L to be generated (LAW 8), which clears the RWS and FWD Motion Control flip-flops (LAW 7). When tape motion ceases, RWS (SB) L is negated on the slave bus.

8.8 READ (NRZ)
This section discusses the operation of the TU10W read circuitry when operating in NRZ mode.

8.8.1 Read Heads and Amplifiers
As tape moves past the read heads, flux transitions on the tape cause the read heads to produce voltage pulses; the direction of flux transitions determine the polarity of the output pulses. The read pre-amplifier (Figure 8-23 and G056 schematic), consisting of two type 72733 differential amplifiers, then inverts the read head signals. Each differential output of the read preamplifier is inverted and further amplified by a group of three transistors; the final two transistors operate in push-pull mode. The resulting amplified differential signals are then input to opposite sides of a delay line. A phase shift of about 6 degrees (Figure 8-24) occurs across the delay line; this phase shift is utilized by the peak detector. The peak detector is a comparator circuit whose output changes state when the relative magnitude of its inputs change (i.e., when one input becomes greater or less than the other); this occurs at the peaks of the read head signals.

Peak detector circuit output transitions are converted into pulses by the dual edge pulse amplifier; these pulses strobe the dual threshold gate. The dual threshold gate compares its input (amplifier output) to positive and negative threshold voltages (Figure 8-25). If the input is more positive than the POS RD THRESHOLD at strobe time, a negative pulse is produced at the + output. If the input is more negative than the NEG RD THRESHOLD, a negative pulse is produced at the – output.

Read threshold voltages are determined by the signal WRE H input to a 74156 data selector chip (Figure 8-25). Depending on these inputs, one of two transistors is turned on. (Only two of four transistors are used in this setup.) Because each transistor has a different collector resistor, a programmable current (+ Threshold Voltage) is obtained. The + Threshold Voltage is fed to a 72741 operational amplifier to produce an equal but opposite polarity – Threshold Voltage. These threshold levels are used by the read amplifiers to establish the lowest acceptable signal level.
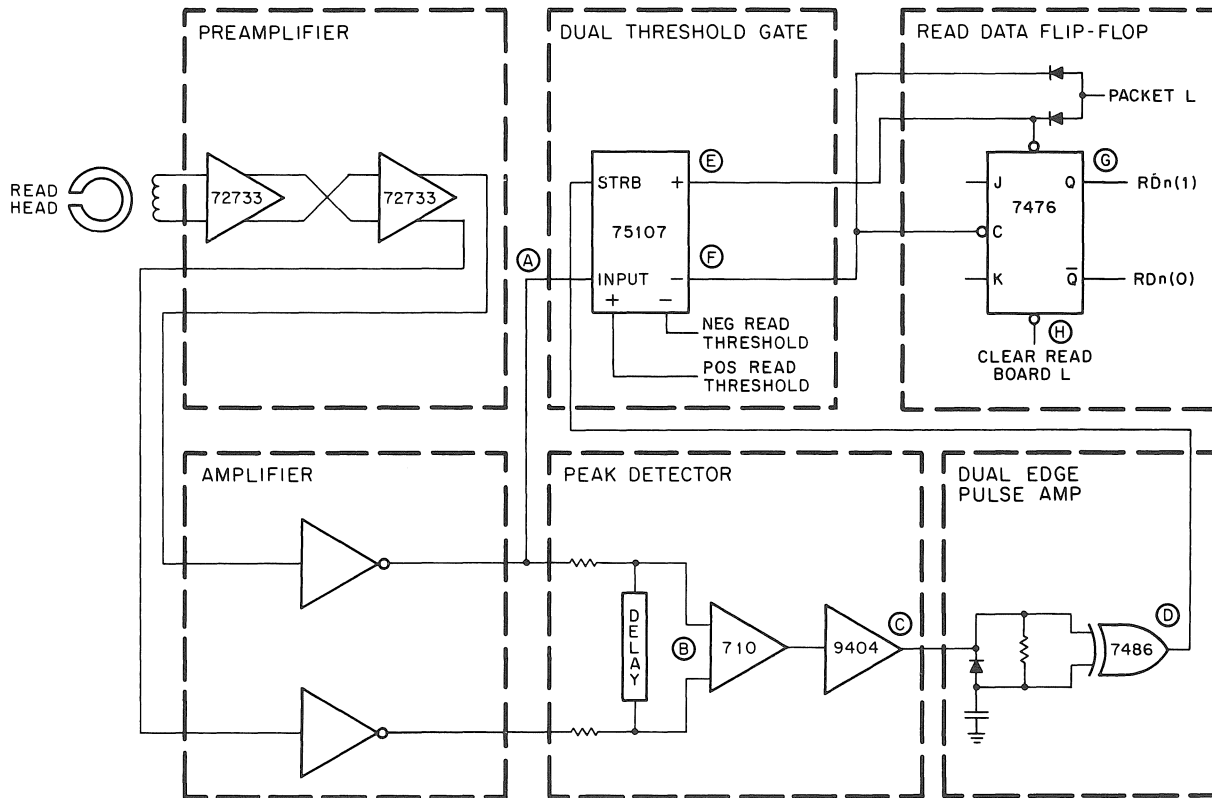
Figure 8-23   Equivalent Circuit of Read Circuitry for One Track
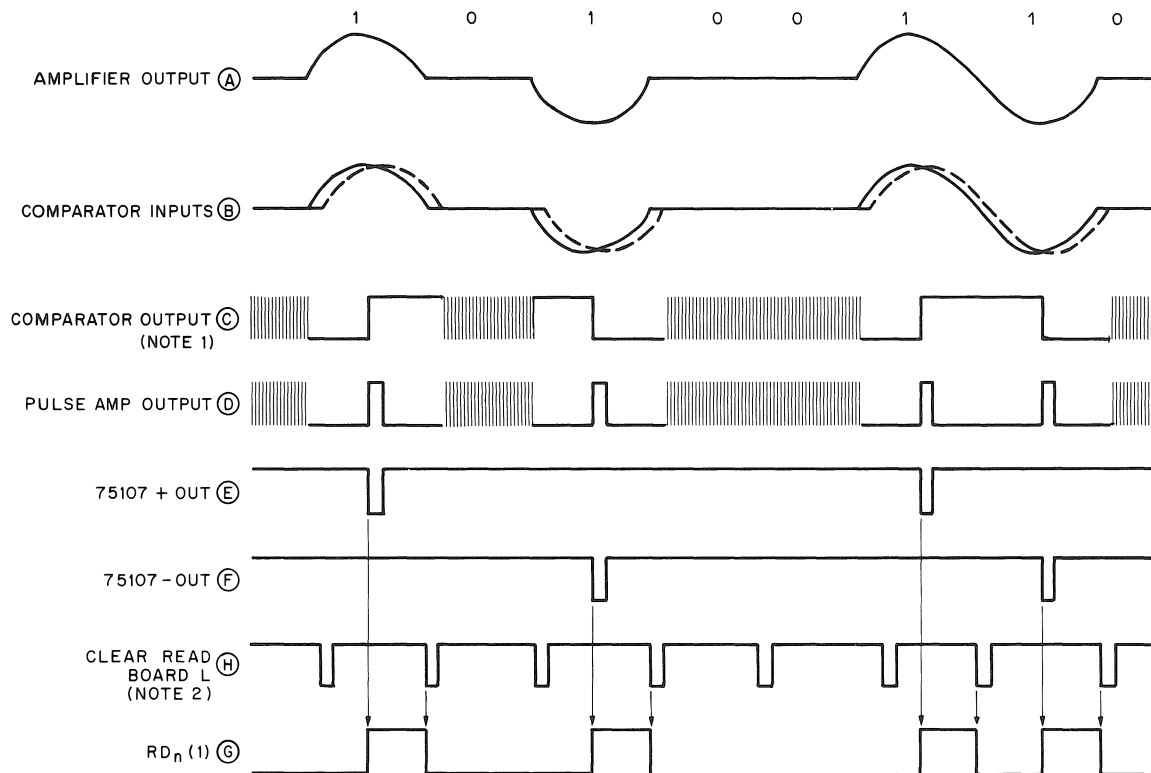
Figure 8-24   Read Amplifier Waveforms (NRZ)

	WRE H B	Y_3	Y_2	Y_1	Y_0
NRZ·$\overline{\text{WRE}}$	0	1	0	1	1
NRZ·WRE	1	0	1	1	1
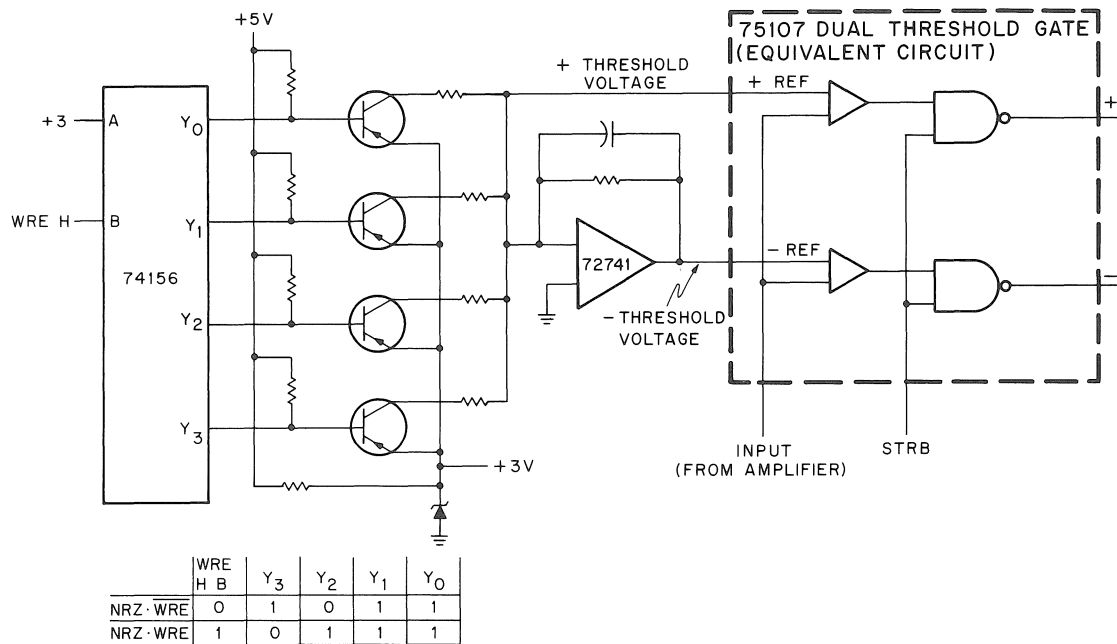
11-4684

Figure 8-25   Programmable Threshold

Whenever the dual threshold gate produces an output pulse, PACKET L is asserted, and the Read Data flip-flop is set. This signifies that a one-bit has been detected on the tape track. Because of parity conventions, at least one of the TU10W's read amplifiers will detect a flux transition (a one-bit) as a tape character is read. When the first one-bit of a tape character is read, and the corresponding Read Data flip-flop is set, START SKEW DELAY is asserted. This sets the Skew flip-flop and initiates a read deskew timing sequence, at the end of which SDO H (Skew Delay Over) and RSDO (Read Strobe Delay Over) are asserted.

SDO H generates CLEAR READ BOARD L, which clears the Read Data flip-flop in each read amplifier. RSDO L is transmitted via the slave bus to the interface logic where it is used to generate CRDS H (Read Strobe) for the controller.

The read deskew timing sequence during a read data operation differs from that of a write operation. During a read data operation, the skew delay counter (two 74197s) loaded with a preset that depends on the tape data density is up-clocked at 1.15 MHz when the Skew flip-flop is set. When the counter reaches a count of 100, SDO H is asserted; this occurs approximately 50 percent into the data cell.

With SDO H asserted, the Skew flip-flop is reset on the next negative-going clock edge. This causes the counter to be reloaded; SDO H is thereby negated. The deskew timing sequence will reoccur each time a tape character is read.

8-38

During a write operation, the counter presets are greater and as a result, SDO H is generated 35 percent sooner. When SDO H is generated, the counter is reloaded and upcounted until NTZO H (Non-Trespass Zone Over) is asserted. At this time, the Skew flip-flop is reset and the deskew timing sequence is over. If the read amplifiers detect a data transition (PACKET L asserted) while SDO H is asserted, SET VPE L is generated and transmitted to the controller.

The outputs of the G056 read amplifier are routed to the slave bus via a type 8266 multiplexer on the slave clock and motion delay module (SC 2). The read data signals are then transmitted to the controller.

8.9 WRITE (NRZ)
This section discusses operation of the TU10W write circuitry when operating in NRZ mode.

8.9.1 NRZ Data Write
The slave bus write data (WD) lines are received in the TU10W by receivers in the LAW (M8910) module (refer to LAW 3 and 4). The data is then gated by the write data multiplex (E5, E13 and E19) to the write deskew buffer and nine XOR gates. The XOR gates cause the write deskew buffer to be complemented for each 1 that is written. The write deskew buffer is clocked by SK CLK (skew clock) pulses (LAW 4). These pulses are actually delayed REC L pulses, jumpered to compensate for static skew in the write head. The write deskew buffer outputs are then driven to the write head.

8.9.2 NRZ Data Write Timing
Once a write data function is decoded, WRITE and FWD commands are placed on the slave bus by the interface logic. Also, a SLAVE SET PLS is sent to the TU10W. This initiates tape motion and sets the Write Enable flip-flop (LAW 8). WRITE ENABLE switches current to the write and erase heads (LAW 3). Because no flux reversals can be effected until WRT CLK (SC3) pulses are produced, the tape is dc erased as it accelerates.

When the transport is up to speed (ACCL H negated), the TU10W begins to transmit WRT CLK pulses to the interface logic. The logic returns REC L pulses to the TU10W, which causes the tape character presently in the interface logic to be transferred to tape.

8.9.3 NRZ Tape Mark Generation
The interface performs the write tape mark operation; the tape mark character forced on the WD lines is 23 (9-channel NRZ format). Refer to the interface logic theory section of this manual for details.

8.9.4 Tape Mark Write Timing
When the SLAVE SET PLS is produced, the write and erase heads are energized, causing the tape to be erased throughout the start motion delay. At the completion of the delay, an REC L pulse clocks the TU10W write deskew buffer and transfers the tape mark character to tape. Refer to the interface logic theory section of this manual for details.

8.10 TU10W POWER SUPPLY
The TU10W power supply is a forced air-cooled unit that converts single-phase, 115 V or 230 V nominal, 47–63 Hz line voltage to four regulated output dc voltages (+5.3 V, +12 V, +12 V, and –6.4 V) and four unregulated voltages (±16 V and ±17 V). The power supply is controlled by an 861 power control. Each of the regulated voltages has short circuit (current foldback) protection. Overvoltage (CROWBAR) protection is incorporated in the +5.3 V, –6.4 V, and one of the +12 V circuits.

The power supply is divided into two sections (Figure 1-5): the ac input circuitry, consisting of the transformer and large filter capacitors (transformer-capacitor assembly); and a regulator board, which contains the remaining circuitry. The power supply circuit description references schematic D-CS-5412242-0-1. The regulator board (Figure 8-26 and 8-27) contains all the circuitry between the transformer secondary winding and the power supply output cables. A 4-pin Mate-N-Lok connector (J1) supplies voltage to the fans and vacuum motor. Connector J2 connects the transformer secondary winding outputs to the regulator board, while J3 adds the large filter capacitors to the circuitry. Connector J4 connects the supply to the H606 power board servo circuitry and J5 supplies voltages to the TU10W backplane.
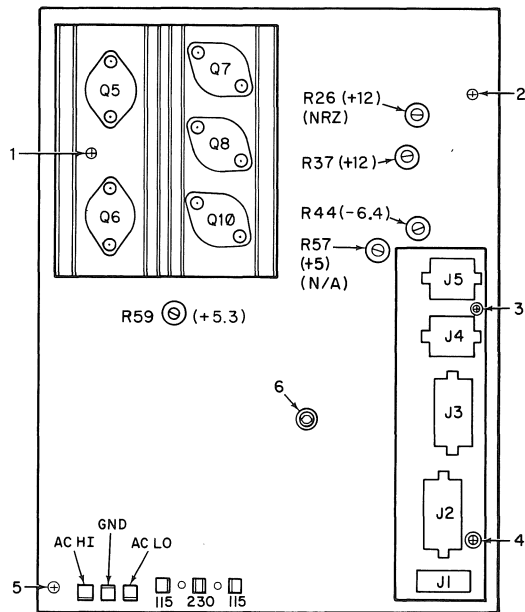
NOTES:
1) 1-5 represent 5 Phillips head screws.

2) 6   represent Allen screw—must be secured very tightly, or
                  damage to the power supply may
                  result.

11-4683

Figure 8-26   TU10W Power Supply Regulator Board

FAN POWER WIRING

LOGIC ASSEMBLY FAN

Q6

R59; +5 V ADJUSTMENT
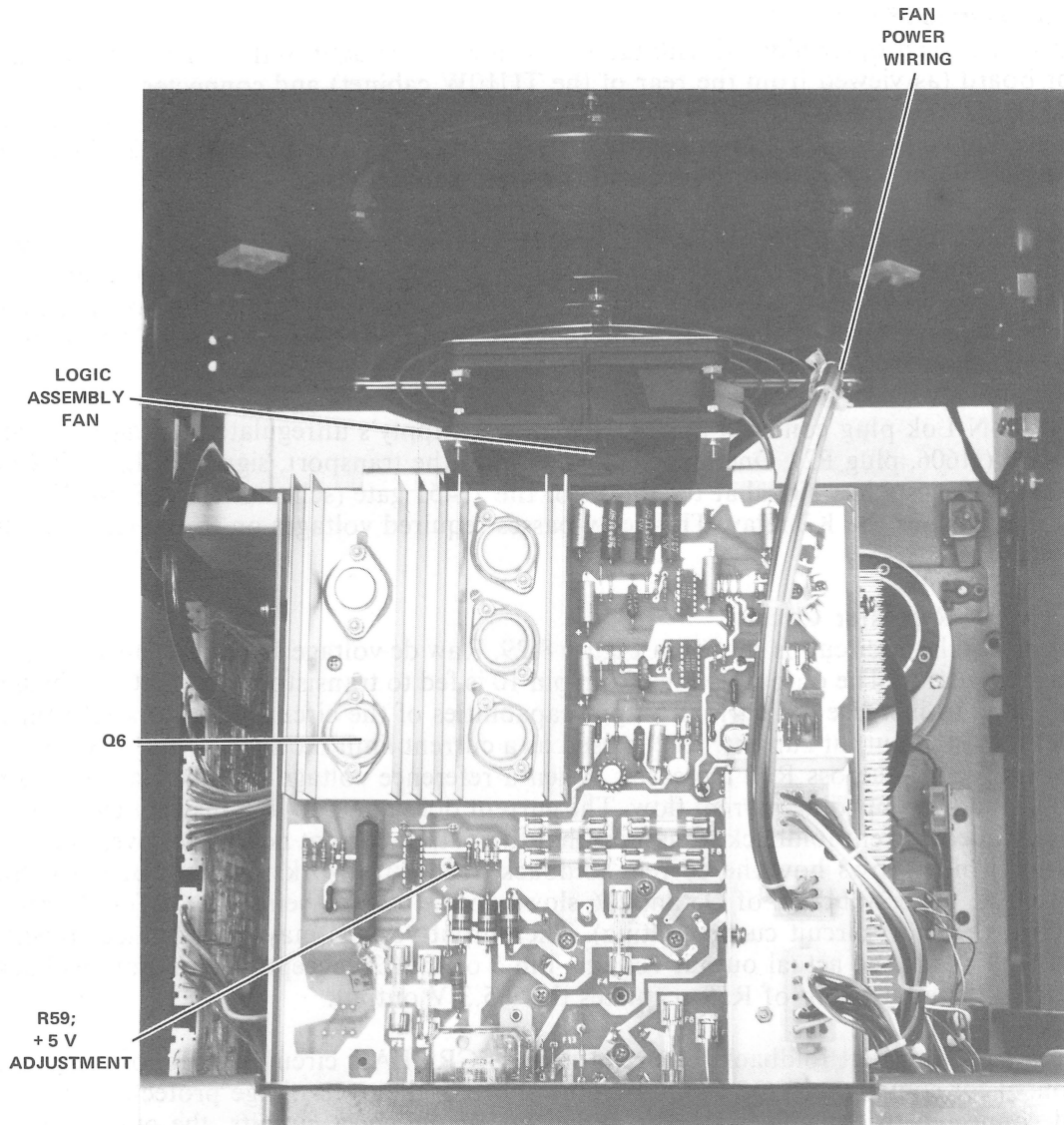
8209-8

Figure 8-27   TU10W Regulator Board (Cover Removed) and Fan

8.10.1 Generation of Raw ±DC

The ac power line cord, terminated with tab connectors, is brought to the lower left-hand area of the regulator board (as viewed from the rear of the TU10W cabinet) and connected to the input power tabs (AC HI, GND, and AC LO). Two wires (in the same area) connect to either the 230 V tab or the 115 V tabs, and configure the power supply for 115 V or 230 V operation. The J2 Mate-N-Lok connector interconnects the regulator board and the main transformer.

A general block diagram of the TU10W power supply is shown in Figure 8-28. The center-tapped transformer voltage is fused, rectified, and filtered prior to being fed to the various voltage regulators and J4. The fuses do not normally blow when an output is shorted because of an overcurrent (current foldback) protection. Overvoltage protection (CROBAR) is also used on all regulated outputs except the +12 (NRZ) output, which does not require it.

The J4 Mate-N-Lok plug connects the TU10W power supply's unregulated voltages to the TU10W power board (H606, plug P2). Once tape is loaded onto the transport, signal RELAY ENABLE L is asserted. This places a low signal at the inputs of the 75451 gate (schematic D-CS-5412242-0-1, location A7) that enables the K2 relay. This relay passes required voltages on to the H606 module when tape is loaded.

8.10.2 +5 Vdc Regulator Circuit

The +5 Vdc regulator circuit is shown in Figure 8-29. Raw dc voltage is input to pins 11 and 12 of the 723 voltage regulator. The output voltage from pin 10 is fed to transistors Q6 and Q5, which are series regulators used to increase the current output capabilities of the circuit. Resistors R62 through R66 (inclusive) sense the output current. R62 is used as a current limit monitor by the 723. As the current increases, the voltage across R62 increases. When a reference voltage is exceeded, the 723 begins to turn off Q6 and Q5, impeding current flow. The current does not stop, but instead decreases to a safer level; this is called current foldback. It assures that the output current never goes over 10.0 A. Refer to Figure 8-30, which shows how the current foldback procedure works. As the current surpasses the limit of 10.0 A, the conduction of Q5 and Q6 slows down (toward being shut off) until no voltage is produced (at the short circuit current rating). The output voltage may be regulated. Resistors R58, R59, and R60 divide the actual output voltage. Pin 5 of the 723 accepts the output feedback voltage through R59; the adjustment of R59 regulates the +5.3 V output.

In addition to the current foldback feature, a voltage CROBAR circuit is used, offering overvoltage protection. If for some reason Q5 or Q6 become shorted, the overvoltage protection circuit protects any load connected to the power supply. When Q5 or Q6 short circuits, the output voltage starts increasing very rapidly. As the voltage across the D16 zener diode becomes greater than 6.8 V, it breaks down and begins conducting; it does not conduct during normal operation. Current now begins to flow through R22. When the voltage at the junction of D16 and R22 becomes greater than approximately 0.7 V (at the gate of D15), the SCR fires and begins conducting. This offers a path for current from the output to ground, shunting any load, thus protecting it. The SCR continues conducting until the power supply is turned off or the 15 A fuse (F12) is blown.

8.10.3 +12 Vdc Regulator Circuit (Write Circuits)

The +12 Vdc regulator circuit is shown in Figure 8-31. It operates in a manner similar, but not identical, to the +5 Vdc regulator circuit discussed previously. In the case of the +12 Vdc regulator, a type 723 regulator is again used.
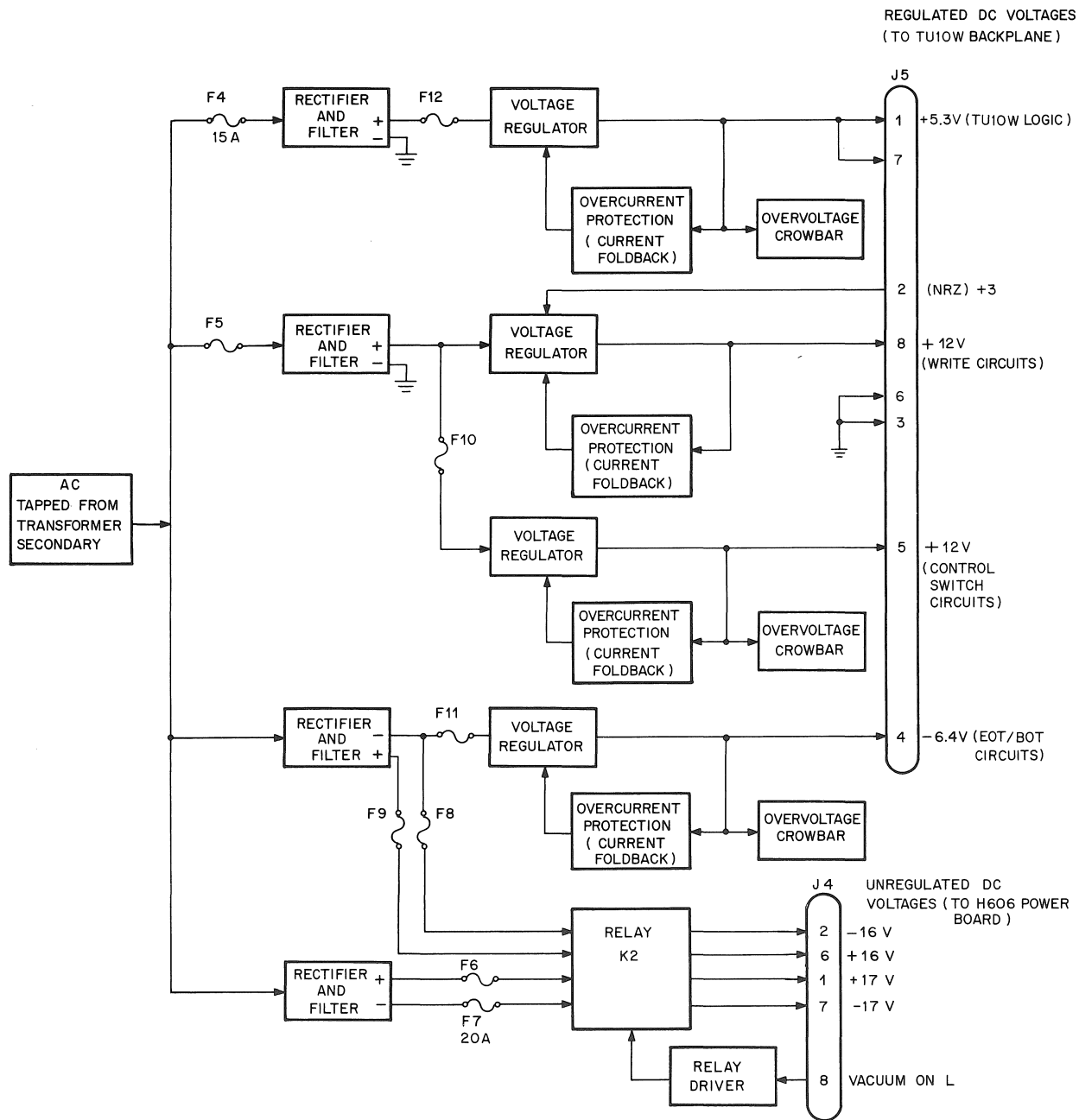
Figure 8-28   TU10W Power Supply Block Diagram
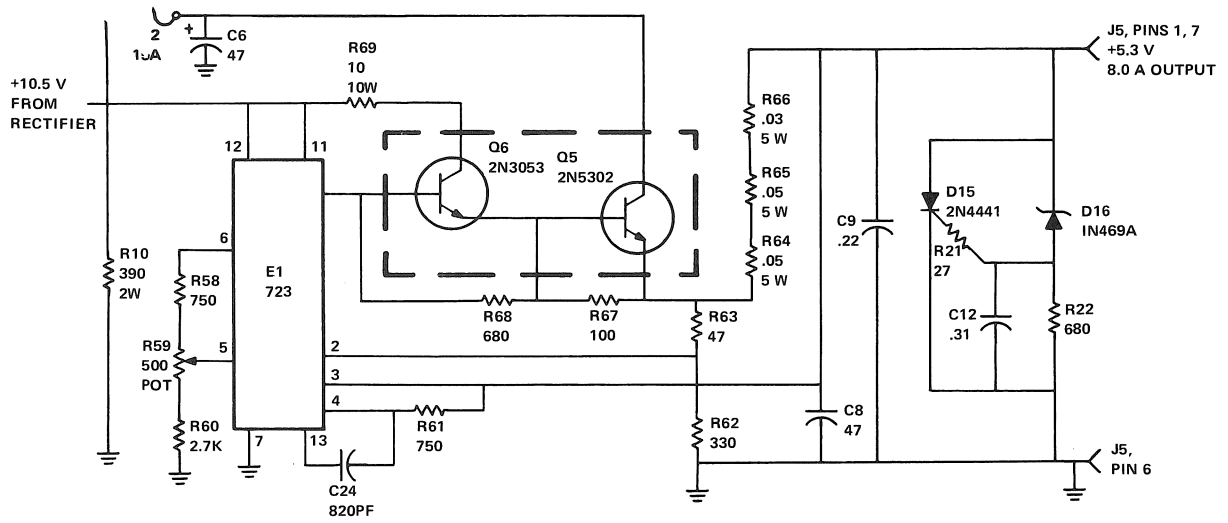
Figure 8-29   +5.3 Vdc Regulator Circuit
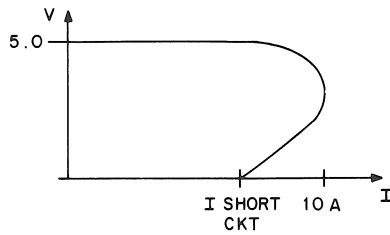
Figure 8-30   Current Foldback Operation
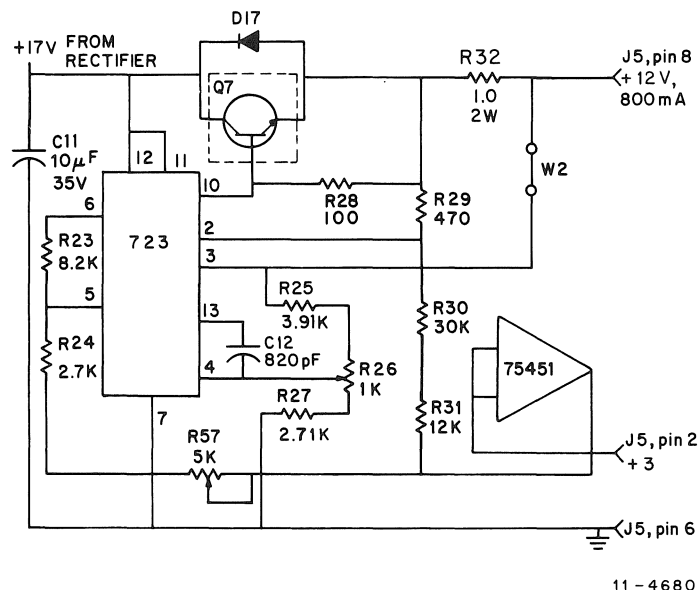
Figure 8-31 +12 V Regulator Circuit

The 723 is a precision voltage regulator. It is a 2-level regulator, in that it can output two selectable voltages. Raw dc from the bridge rectifier network enters pins 12 and 11 of the 723. The TU10W write driver circuits require +12 V for NRZ. A high level is presented through J5, pin 2, to the inputs of the 75451, which outputs a high level through R57 by R23 and R24 and lets the full reference voltage from pin 6 of the 723 enter the noninverting input (pin 5). A +15 V output is produced.

The output (from pin 10) of the 723 is applied to Q7, where higher current is produced for the output. The current foldback and sense circuits operate in a manner similar to those of the +5 V regulator. Output voltage is divided by R25, R26, and R27, and is adjusted by R26. Adjustment R57 is not used in the TU10W.

As output current increases, the voltage across R30 and R31 also increases. As the voltage reaches the limit of the 723, it is sensed at pin 2. The output from the 723 starts reducing, starting to shut off Q7 and keeping the output current from reaching unsafe levels.

No overvoltage protection is provided in the +12 V power supply section because it is not necessary. The circuit that this supply feeds can stand voltage higher than this regulator can supply.

8.10.4 +12 Vdc Regulator Circuit (Control Switch Circuits)
The type 723 regulator used in this +12 V supply operates in exactly the same way as the previous 723 regulator (Figure 8-32).
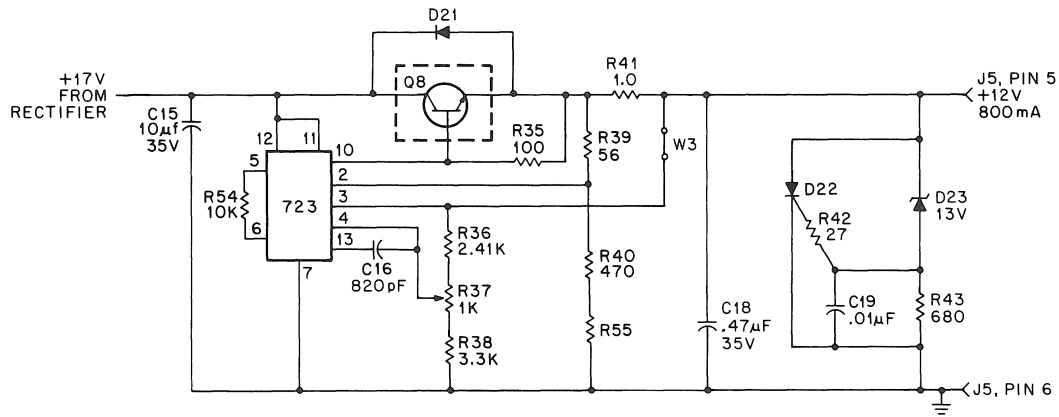
Figure 8-32   +12 V Regulator Circuit

In the +12 V regulator circuit, resistor R37 is the fine adjustment for the output voltage. Resistors R41, R39, R40, and R55 offer the sense for the current foldback network. The overvoltage network acts in the same way as the network in the +5 V supply, except the zener diode (D23) does not conduct until the voltage across it becomes greater than 15 V. Then the SCR fires and offers a path for output current, if Q8 becomes shorted for some reason.

8.10.5   –6.4 Vdc Regulator Circuit
The TU10W power supply also furnishes a regulated –6.4 V (Figure 8-33). The LM304 is intended for systems requiring regulated negative voltages. Rectified negative voltage is presented to the LM304 from the negative output of the D11 diode bridge.

The LM304 output from pin 7 goes to the base of transistor Q11. Transistor Q11, connected with Q10, looks and acts like a normal PNP device; the combination supplies high current to the output.

Transistor Q12 is used in the current foldback network. Output current is sensed by R50, the V_{eb} of Q11, R49, and R51. As the output increases (becomes more negative), the voltage at the base of Q12 also increases (becomes more negative). Transistor Q12 starts to turn on and, as it does, shunts LM304 output current away from Q11-Q12, limiting output current. Then, as the output decreases, Q12 begins to shut off and allows the output current to rise again.

The overvoltage protection works identically to the other networks. Zener diode D20 begins conduction at approximately –8.2 V, which fires the SCR (D26) and creates a path to ground if Q10 and/or Q11 should short out. Again, the supply must be turned off to allow C22 to discharge before D26 stops conducting. Diodes D24 and D25 protect the LM304 against any overvoltage surges.

8.10.6   Specifications
Tables 8-4 and 8-5 list the power supply specifications.
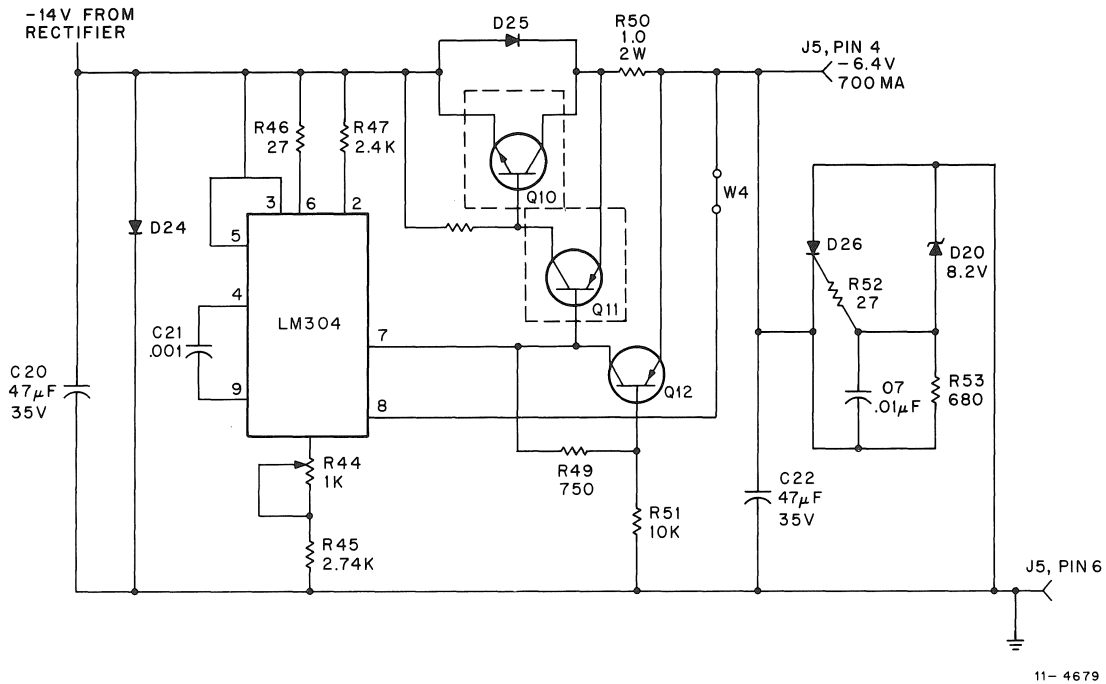
Figure 8-33   –6.4 V Regulator Circuit

Table 8-4   Power Supply Input Specifications

Parameter	Specification
Input Voltage (1 phase, 2 wires, and ground)	95–132/190–264 V
Input Frequency	47–63 Hz
Input Current	7 A nominal at 115 V, 60 Hz
Inrush	85 A at 115 Vrms, 60 Hz

Table 8-5 Power Supply Output Specifications

Parameter	Specification
+5 V Regulator Circuit	
Load Range	8 A maximum
Overvoltage Crowbar	6.4 V, 10%
Current Foldback at 25° C	3 A nominal
Backup Fuse	5 A
Adjustment	5% minimum
Regulation	Less than 2%
+12 V Regulator Circuit	
Load Range	0.75 A
Overvoltage Crowbar	None
Current Foldback at 25° C	0.5 A
Backup Fuse	1 A
Adjustment	35% minimum
Regulation	Less than 3%
+12 V Regulator Circuit	
Load Range	0.75 A
Overvoltage Crowbar	15.5 V, 10%
Current Foldback at 25° C	0.75 A to 0.3 A
Backup Fuse	0.75 A
Adjustment	10% minimum
Regulation	Less than 3%
–6.4 V Regulator Circuit	
Load Range	0.75 A
Overvoltage Crowbar	8 V
Current Foldback at 25° C	0.75 A to 0.3 A
Backup Fuse	0.75 A
Adjustment	10% minimum
Regulation	Less than 3%

A.1 MAGNETIC TAPE FUNDAMENTALS – DEFINITIONS

1. Reference Edge – The edge of the tape as defined by Figure A-1. For tape loaded on a tape transport, the reference edge is toward the observer.
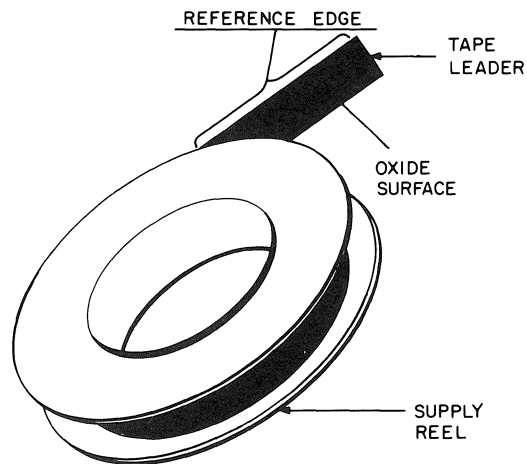
Figure A-1   Reference Edge of Tape

2. BOT (Beginning-of-Tape) Marker – A reflective strip placed on the nonoxide side of the tape, against the reference edge, 15 ft, ±1 ft (457 cm, ±30.5 cm) from the beginning of the tape.

3. EOT (End-of-Tape) Marker – A reflective strip placed on the nonoxide side of the tape, against the nonreference edge, 25 to 30 ft (762 to 914 cm) from the trailing edge of the tape.

4. 9-Channel Recording – Eight tracks of data plus one track of vertical parity. Figure A-2 shows the relationship between track and bit weight for a 9-channel transport.*

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*When the track vs bit channel standard was adopted, the outer tracks were more susceptible to bit dropping errors. Consequently, channels containing the least 1s were assigned the outer locations on the tape.
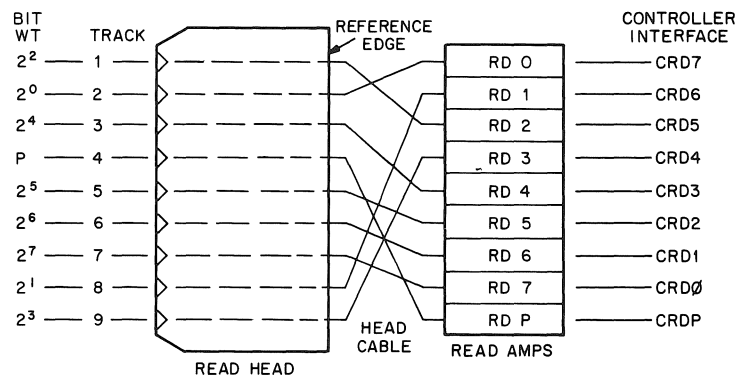
Figure A-2   Track-Bit Weight Relationship for 9-Channel Transport

5. Tape Character – A bit recorded in each of the nine channels.

6. Record – A series of consecutive tape characters.

7. File – An undefined number of records (minimum = zero, no maximum).

8. Interrecord Gap (IRG) – A length of erased tape used to separate records [0.5 in. (1.27 cm) minimum for 9-track; maximum IRG is 25 ft (762 cm)].

9. Extended IRG – A length of erased tape [3 in. (7.62 cm) minimum] optionally used to separate records.

10. Tape Speed – The speed at which tape moves past the read/write heads; normally stated in inches per second.

11. Tape Density – The density of sequential characters on the tape. It is normally specified in bytes per inch (bpi), which is equivalent to characters per inch.

12. Write Enable Ring – A ring that must be inserted on the supply reel to allow the transport to write on the particular tape. This safety feature helps prevent accidental destruction of previously recorded data.

13. Tape Mark (TM) – A record written on the tape to designate the end of a file; sometimes referred to as a file mark (FMK).

A.2   RECORDING METHODS AND DECmagtape FORMATS

The DECmagtape system is an on-line mass storage system for programs or data. Data is recorded on tape in vertical rows called characters. Each character consists of eight data bits and one vertical parity bit. The vertical parity bit is program-selected as even or odd. The odd parity bit guarantees that each character records at least one 1 bit.

The parity bit is generated according to the rule that the number of 1s in a character (parity bit included) is odd or even. For example, if odd parity is used and the character contains an even number of 1 bits, the parity bit is generated as a 1 bit and an odd number of 1 bits are recorded; then, if an even number of bits are read back from tape, a vertical parity error is generated to notify the program that the data is in error.

A-2

The data characters are recorded in blocks of characters termed records (Figure A-3). Each record contains a specified number of characters determined by the word count.

A. FILE MARK AND GAP FORMAT

✱ = 3 CHAR. SPACE
✱✱ = 7 CHAR. SPACE

B. IRG FORMAT
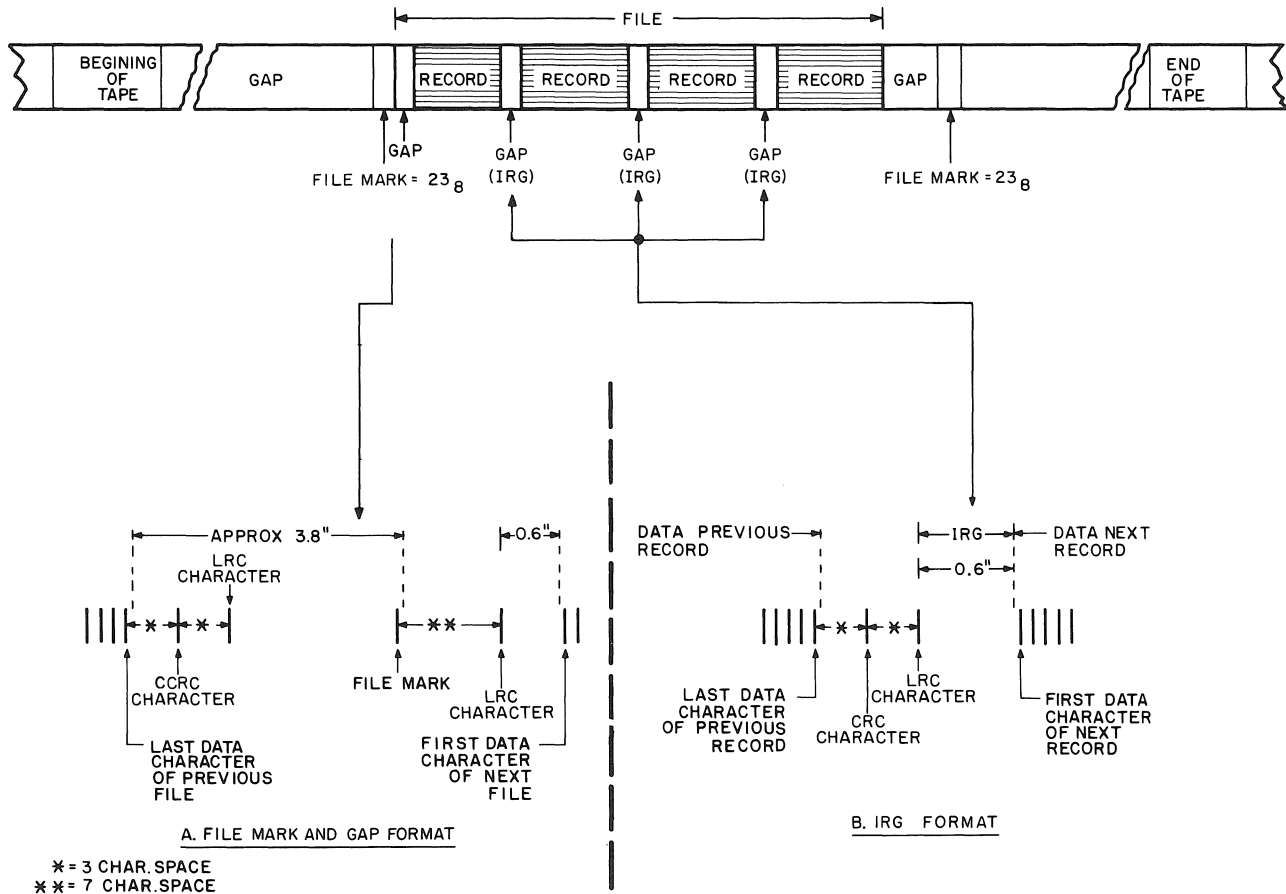
II-3069

Figure A-3   Data Recording Scheme

Records are separated by interrecord gaps (IRGs). The IRG is 0.5 in. (1.27 cm) minimum [approximately 0.6 in. (1.5 cm) in normal operation], but may be extended to 3 in. (7.62 cm) by performing an extended gap operation. Tape IRGs (unrecorded areas) provide areas on the tape for the transport to start or stop and also separate data records.

A.2.1   NRZI Recording Method (non-return-to-zero inverted)
In the NRZI recording method, a 1 bit is represented by a reversal in the direction of tape magnetization on a track; a 0 bit is represented by no change in tape magnetization.

A.2.2   9-Channel Tape Format

The format (Figure A-4) is composed of from 18* to 2048 nine-bit characters spaced 1/800 in. (3 mm) apart, followed by 3 character spaces, a CRC character, 3 more spaces and an LRC character. This unit of data is called a record. At 800 characters per inch, the record is between 1/32 in. (79 mm) minimum and 5 in. (12.7 cm) maximum. Between each record is a gap of at least 1/2 in.† The tape structure consists of a number of records followed by a file mark (Figure A-3). Since data is recorded and read at high speed, IRGs are used to provide space for starting and stopping a tape transport. A transport accelerates from standstill to full speed in approximately 0.2 in. (0.5 cm) of tape and decelerates from full speed to standstill in 0.2 in. (0.5 cm) of tape; thus, the minimum IRG of 0.5 in. (1.27 cm) provides adequate space for starting and stopping the tape transport.
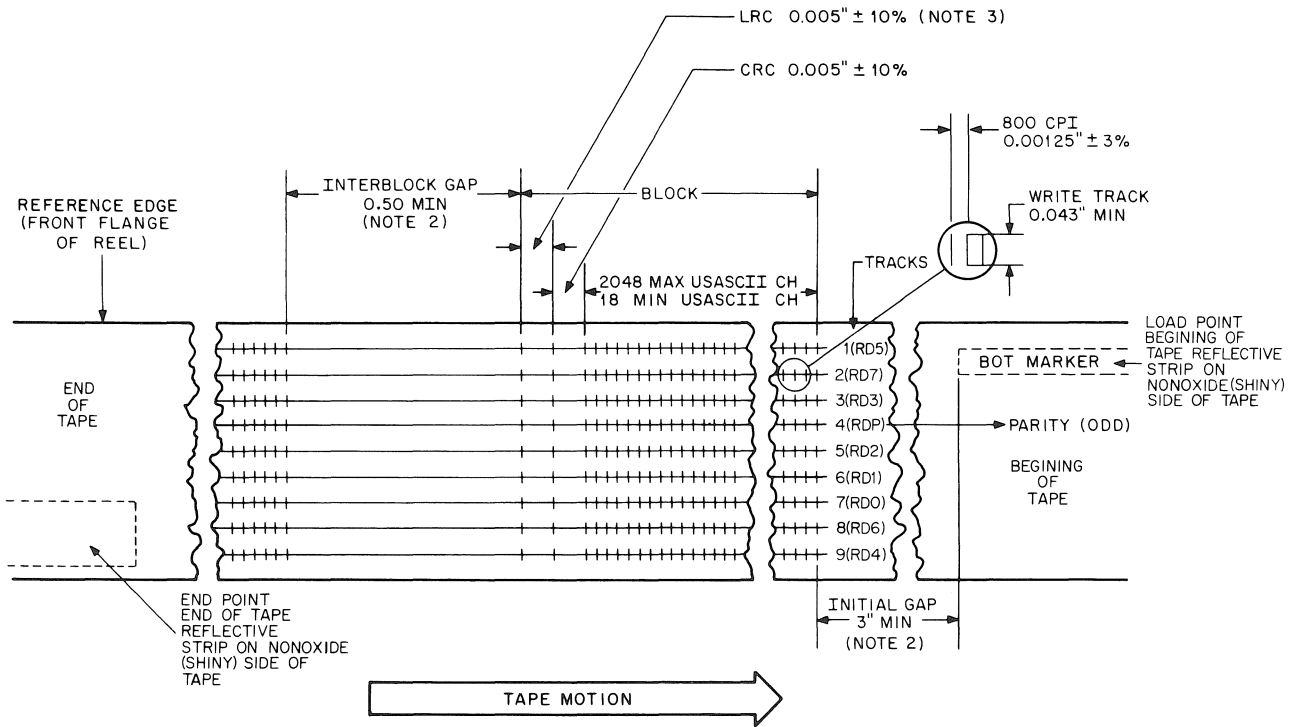
LEGEND:

BPI	Tape Bits per Inch
BOT	Beginning of Tape
LRC	Longitudinal Redundancy Check
CRC	Cyclic Redundancy Check

NOTES:

1. Tape is shown with oxide side up, read/write head on same side as oxide. Tape is shown representing 1 bits in all NRZI recording; 1 bit produced by reversal of flux polarity, tape fully saturated in each direction.

2. Tape to be fully saturated in the erased direction in the interrecord gap and the initial gap.

3. An LRC bit is written in any track if the longitudinal count in that track is odd.. Character parity is ignored in the LRC character.

4. CRC – Parity of CRC character is odd if an even number of data characters are written, and even if an odd number of characters are written.

Figure A-4   Tape Recording Format

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*USASCII program standards, not a hardware limit.

†0.5 in. (1.27 cm) minimum; 0.6 in. (1.5 cm) nominal.

The CRC character is generated during a write operation and written at the end of a record. The check character performs the same function to a record as the parity bit does to a character.

The LRC character is the final character in the record and is generated so that for each track the sum of 1 bits (CRC character included) is even. The LRC character is written on tape by clearing the write buffer in the tape transport after the CRC character is written. The LRC strobe resets the write buffer, causing a 1 to be written on each track containing an odd number of 1s; a 0 is written on each track containing an even number of 1s.

A.2.3 7-Channel Tape Format

Each character frame in a 7-channel tape (Figure A-5) consists of six character bits (B, A, 8, 4, 2, 1) in descending order of significance. The parity bit, or check bit (C), is the seventh bit and is set or cleared by the transport write head. One byte of a data word corresponds to one tape character. However, because one byte contains eight bits and a tape character contains only six data bits, two bits within each byte are not used. During a read operation, the extra bits are forced to 0; during a write operation, the bits remain unchanged. During the core dump mode of operation, one byte corresponds to two tape characters. Thus, all bits within the byte are used; however, the two most significant bits on the tape are not used.
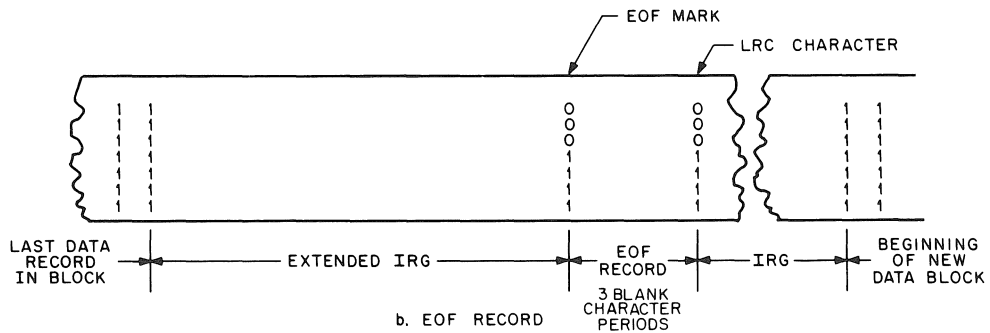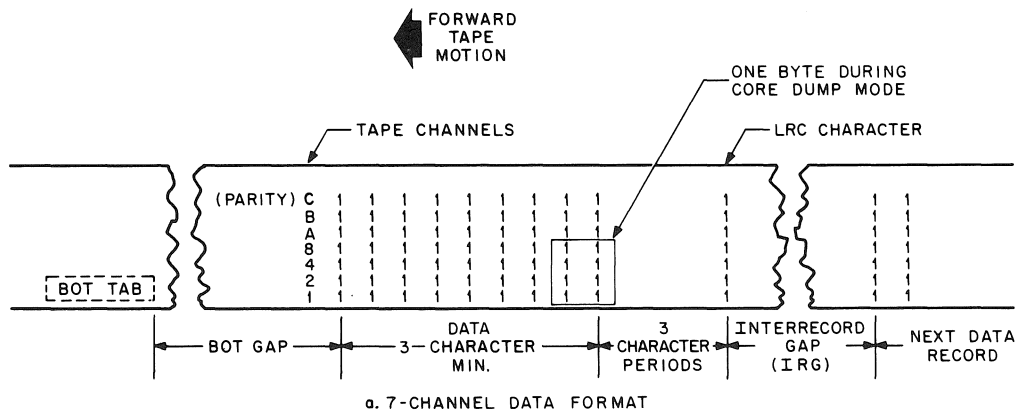
Figure A-5   7-Channel Tape Format

The magnetic tape is divided into data records, each record separated by an interrecord gap (IRG). In a block format, a number of records are written together with an IRG before the first record and after the last record. In either case, the IRG is an unused portion of tape preceding and following the record or the block.

The longitudinal redundancy check (LRC) character is written after the data and is separated from the data by three character spaces. Each bit in the LRC is such that the total number of bits in any specific channel is even.

The end of a block of records is indicated by an end-of-file mark character. The end-of-file (EOF) mark is separated from the data by an extended IRG. The extended IRG is a 3-in. strip of blank tape compared to the standard 3/4-in. IRG for 7-channel tape and the 1/2-in. IRG for 9-channel tape. The EOF mark and associated LRC character are considered to be one complete record.

The 9-channel tape format (Figure A-6) is similar to the 7-channel format; however, because each character consists of eight data bits and one parity bit, a byte corresponds to a tape character. Therefore, there is no need for a core dump mode, because information can be transferred from the system to the tape on a one-to-one ratio. In addition, the 9-channel format includes a cyclic redundancy check (CRC) character. Data is followed by three blank character periods, the CRC character, three more blank character periods, and the LRC character. The LRC character is followed by an IRG as before.
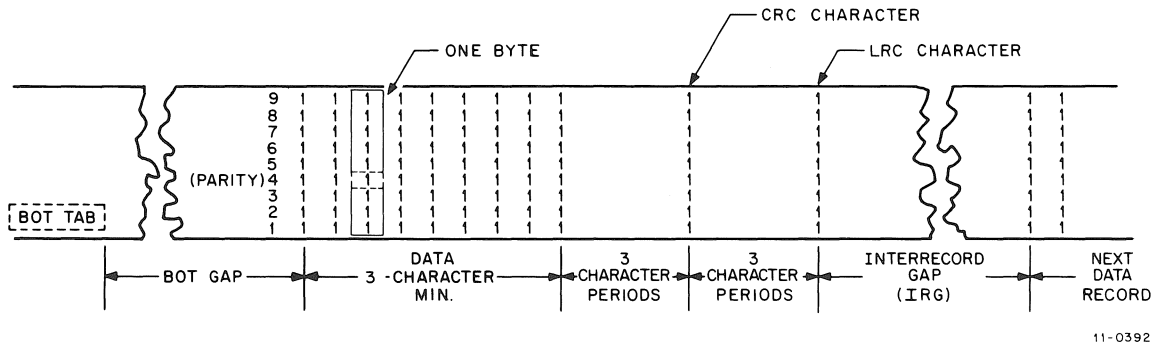
Figure A-6 9-Channel Tape Format

A.3 CYCLIC REDUNDANCY CHECK (CRC) CHARACTERS

The CRC character provides a method of error detection and correction on magtape transports. The code has nine check bits that form a check character at the end of each record. To perform a correction, a record in which an error has been detected must be reread into memory with the LRC and CRC character for program evaluation. Errors involving more than one track can be detected but not corrected.

The CRC character is generated as follows:

1. The CRC register is cleared at the beginning of each record. As each data bit is written on tape, it is exclusively ORed with its corresponding bit in the CRC register.

2. The CRC register is shifted one position to the right after the exclusive OR operation has taken place.

3. The bits entering CRC 2, CRC 3, CRC 4, and CRC 5 of the CRC register are inverted if the bit entering CRCP is a 1. Data is shown in Table A-1; the resultant CRC character is shown in Table A-2.

Table A-1   Five-Character Record

Bit	Characters				
	Data Character 0	Data Character 2	Data Character 3	Data Character 4	Data Character 5
P	0	0	1	0	1
0	1	0	0	1	0
1	0	1	0	1	0
2	0	1	0	1	1
3	1	0	1	1	0
4	0	1	1	0	1
5	0	1	1	0	1
6	1	0	1	0	1
7	0	1	0	1	0

Table A-2   CRC Character in Register When Writing

CRC Bits	CRC Register						CRC Character On Tape
	Cleared	Character 1	Character 2	Character 3	Character 4	Final	
CRCP	0	0	0	0	1	1	0
CRC0	0	0	0	1	0	0	1
CRC1	0	1	0	0	0	0	1
CRC2	0	0	0	0	0	1	1
CRC3	0	0	1	0	0	0	1
CRC4	0	1	0	0	0	1	1
CRC5	0	0	0	1	1	0	1
CRC6	0	0	1	1	1	0	1
CRC7	0	1	0	0	1	0	1

4. Steps 1 – 3 are repeated for each data character of record.

5. At CRC time, all positions of the CRC register, except CRC2 and CRC4, are complemented and the resultant CRC character is written on tape.

6. The CRC register is cleared for the next record.

A.4 LONGITUDINAL REDUNCANCY CHECK (LRC) CHARACTER

The LRC character is written three spaces after the CRC character. The vertical parity bit is always written on the LRC character; the vertical parity of LRC is never checked. The LRC character makes the longitudinal parity even for the entire record, including the CRC. The LRC character is generated by the LRC register in the following manner:

1. The LRC register is cleared at the beginning of a record.

2. As characters are written on tape, corresponding 1 bits complement the LRC register at the time data is written on tape.

3. At LRC time, the LRC strobe clears the write buffer and 1s are written on tape in only those channels for which the write buffer is set prior to clearing.

4. Following this method, the LRC character forces an even number of bits to be recorded on each track of the tape. The CRC character is included in determining the LRC character.

A.5 DATA FILES

As previously stated, a record is a group of characters preceded by an IRG and terminated by three spaces, a CRC character, three more spaces, and an LRC character. A file is a group of records separated by IRGs and terminated by a 3 in. (7.62 cm) gap followed by a file mark. The file mark is a record consisting of a single data character [the end-of-file (EOF) character] followed by seven blank characters and an LRC character. The CRC character is not written on an EOF record. The LRC character with a file mark is a duplicate of the EOF character (23_8).

A.6 TRACK ASSIGNMENTS

The track assignments for read, write, and parity bits are shown in Table A-3.

Table A-3 Track Assignments for Data and Parity

Transport Track Number	Write Data Bits*	Read Data Bits*	Binary Weight
1 furthest from transport	CWD5	CRD5	2^2
2	CWD7	CRD7	2^0
3	CWD3	CRD3	2^4
4	CWDP	CRDP	–
5	CWD2	CRD2	2^5
6	CWD1	CRD1	2^6
7	CWD0	CRD0	2^7
8	CWD6	CRD6	2^1
9 closest to transport	CWD4	CRD4	2^3

*At controller interface.

APPENDIX B
SYSTEM DIAGNOSTICS

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZTMA-H-D

PRODUCT TITLE: TM,A,B-11/TS03,TU10,N,W INSTRUCTION TEST

PROGRAM DATE: AUGUST 1976

MAINTAINER: DIAGNOSTIC ENGINEERING

AUTHOR: JOHN RODENHISER

REVISED: JIM LACEY/JIM KAPADIA/B. BURGESS/K. LIND/R. BARNES
                 SAM CARPENTER/R. SOLER

1.   ABSTRACT

THE TM,A,,B-11 INSTRUCTION TEST CONTAINS A SERIES OF BASIC TESTS
THAT CHECK REGISTERS FOR PROPER OPERATION WHILE NOT INVOLVING
TAPE MOTION, ALL TAPE MOTION FUNCTIONS, DATA TRANSFERS, EXTENDED
MEMORY, AND MANUAL INTERVENTION TESTS OF THE TU10 OR TS03 TRANSPORTS.
MANUAL INTERVENTION TESTS ARE SKIPPED IN CHAIN MODE

2.   REQUIREMENTS

2.1   EQUIPMENT

PDP-11 WITH TM,A,B-11 CONTROL UNIT AND 1 TS03,TU10,N,W TAPE UNIT.

2.2   STORAGE

2.2.1   PROGRAM STORAGE

THE ROUTINE REQUIRES 4K OF MEMORY.

3.   LOADING PROCEDURE

3.1   METHOD

A. PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED.

B. PROGRAM IS LOADABLE AND CHAINABLE IN 8K OF MEMORY.

4.   STARTING PROCEDURE

4.1   CONTROL SWITCH SETTINGS

STARTING AT LOC. 200 ALL SWITCHES SHOULD BE DOWN OR ZERO.
SOFTWARE SWITCH REGISTER IS LOCATED AT LOC. 176 IF NEEDED.

4.2   STARTING ADDRESS

200

4.3   PROGRAM AND/OR OPERATOR ACTION

        1. LOAD PROGRAM INTO MEMORY.
        2. PLACE ONE TAPE UNIT, ON-LINE, AT LOAD POINT (BOT), UNIT 0 SELECTED.
        3. LOAD STARTING ADDRESS
        4. START PROGRAM
        PROGRAM WILL TYPE "SET SW0=1 IF 7 CHANNEL".(IF NOT CHAIN MODE)
        CHAIN MODE DEFAULT IS DRIVE 0 9TRK ONLY.
        IF APPROPRIATE SET SW0 AND THEN PRESS CONTINUE OR
        ***IF SOFTWARE SWITCH REGISTER IS USED TYPE CNTL G AND THEN CONTINUE
           -THIS WILL ALLOW THE MODIFICATION OF THE SOFTWARE SWITCH REGISTER (REFER TO SECT. 5.1)
        THE PROGRAM WILL BEGIN TESTING.

5.   OPERATING PROCEDURE

5.1   OPERATIONAL SWITCH SETTINGS
                IF THE DIAGNOSTIC IS RUN ON A CPU WITHOUT A SWITCH
                REGISTER THEN A SOFTWARE SWITCH REGISTER IS USED WHICH ALLOWS
                THE USER THE SAME SWITCH OPTIONS AS THE HARDWARE SWITCH REGISTER.
                IF THE HARDWARE SWITCH REGISTER DOES NOT EXIST OR IF ONE DOES
                AND IT CONTAINS ALL ONES (177777) THEN THE SOFTWARE SWITCH
                REGISTER (LOC. 176) IS USED.

        CONTROL:

        THIS PROGRAM ALSO SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH
        REGISTER (LOC. 176) FROM THE TTY. THIS CAN BE ACCOMPLISHED BY
        DOING THE FOLLOWING:

        1) TYPE CONTROL G <^G>; THIS WILL ALLOW THE TTY TO ENTER DATA INTO
           LOC. 176 AT SELECTED POINTS WITHIN THE PROGRAM.

        2) THE MACHINE WILL THEN TYPE: SWR=XXXXXXNEW= (XXXXX IS THE OCTAL CONTENTS
           OF THE SOFTWARE SWITCH REGISTER.)

        3) AFTER THE ''NEW='' HAS BEEN TYPED THEN THE OPERATOR CAN DO ONE
           OF THE FOLLOWING AT THE TTY:

              A) TYPE A NUMBER TO BE LOADED INTO LOC. 176 FOLLOWED BY A <CR>.
                 (ONLY NUMBERS BETWEEN 0-7 WILL BE ACCEPTED AND ONLY 6 NUMBERS
                 WILL BE ALLOWED)
                 IF A <CR> IS THE FIRST KEY DEPRESSED THE SOFTWARE SWITCH
                 REGISTER CONTENTS WILL NOT BE CHANGED.

              B) IF A CONTROL U <^U> IS DEPRESSED THEN THE PROGRAM WILL SEND YOU
                 BACK TO STEP 2.

5.1.1   WITH ALL SWITCHES DOWN THE PROGRAM WILL PRINT OUT ON ERRORS AND
        CONTINUE IN TEST. (END OF PASS WILL PRINT ON EACH PASS)

5.1.2   SWITCH SETTINGS ARE:

        SW15 (100000) = 1 OR UP ... HALT ON ERROR
        SW14 (040000) = 1 OR UP ... SCOPE LOOP
        SW13 (020000) = 1 OR UP ... INHIBIT PRINTOUT.
        SW12 (010000) = 1 OR UP ... INHIBIT SUB-TEST INTERATION,
        SW11 (004000) = 1 OR UP ... SINGLE PASS
        SW10 (002000) = 1 OR UP ... INHIBIT MANUAL INTERVENTION TEST
        SW9 (001000) = 1 OR UP ... FOR TS03 TAPE DRIVES
        SW0 (000001) = 1 OR UP ... TEST 7 CHANNEL TAPE UNIT.

5.1.3   MANUAL INTERVENTION TEST

        THIS TEST WILL REQUIRE THE OPERATOR TO PERFORM CERTAIN OPERATIONS
        WITH THE TRANSPORT AS DIRECTED BY MESSAGES PRINTED ON THE
        TELETYPE.

5.2   SUBROUTINE ABSTRACTS

5.2.1   SCOPE

        THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUB-TEST IN THE INSTRUCTION
        SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT IS
        BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE
        START OF THE SUB-TEST THAT THE SCOPE LOOP IS REQUESTING.
        ***CNTL G WILL BE RECOGNIZED IN THIS ROUTINE (REFER TO SECT 5.1)

5.2.2   HLT

        THIS SUBROUTINE CALL PRINTS THE ADDRESS THAT TAGS THE FAILING
        SUBTEST AND THE CONTENTS OF ALL THE TM,A,B-11 REGISTERS.
        ***THIS ROUTINE RECOGNIZES CNTL G FUNCTION (REFER TO SECT. 5.1)

6.0 ERRORS

6.1 ERROR PRINTOUT FORMAT

WITH SW13=0 (OR DOWN) THE FOLLOWING PRINTOUT WILL APPEAR ON AN ERROR:

```
  PC     STATUS  COMAND BYTE   CA     DATA B  READ L  TEMP   CRC CAL
XXXXXX   XXXXXX  XXXXXX XXXXXX XXXXXX XXXXXX  XXXXXX  XXXXXX XXXXXX
```

PC	=	ADDRESS OF TEST WHERE ERROR OCCURED
STATUS	=	CONTENTS OF STATUS REGISTER AT TIME OF ERROR
COMAND	=	CONTENTS OF COMMAND REGISTER AT TIME OF ERROR
BYTE	=	CONTENTS OF BYTE COUNTER AT TIME OF ERROR
CA	=	CONTENTS OF CURRENT MEMORY ADDRESS AT TIME OF ERROR
DATA B	=	CONTENTS OF DATA BUFFER AT TIME OF ERROR
READ L	=	CONTENTS OF READ LINES AT TIME OF ERROR
TEMP	=	CONTENTS OF ADDRESS "TEMP" USED BY SOME TESTS
CRC CAL	=	CRC CHARACTER CALCULATED (USEFUL ONLY FOR CRC TEST)

NOTE THAT NOT ALL OF THE INFORMATION PRINTED IS INTENDED TO BE
USEFUL FOR EVERY TYPE OF ERROR. THIS IS SIMPLY A STANDARD ERROR
REPORT FOR ALL ERRORS. THE OPERATOR MUST REFER TO THE PROGRAM
LISTING AT THE ADDRESS OF THE ERROR FOR A DESCRIPTION OF THE
CAUSE OF THE ERROR. IT IS THEN UP TO HIM TO DETERMINE WHICH
OF THE INFORMATION IS USEFUL.

6.2 ERROR RECOVERY

WITH SW15=1 OR UP THE PROGRAM WILL HALT ON AN ERROR. DEPRESS
CONTINUE SWITCH TO RESTART TEST.

7.   RESTRICTIONS

7.1   STARTING RESTRICTION

        BEFORE STARTING PROGRAM THE OPERATOR MUST MAKE CERTAIN THAT THE
        TRANSPORT HAS DRIVE 0 SELECTED "ON-LINE".

7.2   OPERATIONAL RESTRICTIONS

        MANUAL INTERVENTION TEST MUST BE PERFORMED ON EACH PASS THRU
        THE PROGRAM UNLESS INHIBITED WITH SW10=1 (OR UP).
        IF UNIT IS A TS03 SW9 MUST BE 1 (OR UP).

8.0   MISCELLANEOUS

8.1   EXECUTION TIME

        WITH MANUAL INTERVENTION TEST INHIBITED IT TAKES 1 MINUTE
        FOR ONE PASS THRU PROGRAM. MANUAL INTERVENTION TEST IS
        OPERATOR DEPENDENT BUT SHOULD TAKE APPROXIMATELY 2 MINUTES.

9.0   PROGRAM DESCRIPTION

10.0   LISTING

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZTMH-E-D

PRODUCT TITLE: TM,A,B-11 MULTIDRIVE DATA RELIABILITY EXERCISER

DATE CREATED: FEB 1977

MAINTAINER: DIAGNOSTIC GROUP

AUTHOR: R. B. BARNES/RON PLATUKIS/R. SOLER

TABLE OF CONTENTS

1.   ABSTRACT

      THIS PROGRAM IS DESIGNED TO BE USED BY AN EXPERIENCED ENGINEER
      /TECHNICIAN FOR EVALUATION AND DEBUGGING OF MAG TAPE DRIVES.
      THE PROGRAM IS CAPABLE OF EXERCISING ANY TAPE DRIVE THAT CAN
      BE OPERATED ON A UNIBUS PDP-11 SYSTEM THROUGH THE TM,A,B-11 MAG
      TAPE CONTROLLER. ANY TYPE OF TAPE DRIVE; 7 OR 9 TRACK MAY BE USED.
      ANY NUMBER OF DRIVES, SINGLE OR MULTIDRIVE SYSTEMS, UP TO EIGHT
      (8), MAY BE TESTED BY A SINGLE EXECUTION OF THE PROGRAM. THIS
      FLEXIBILITY IS POSSIBLE BECAUSE THE PROGRAM HAS NO FIXED PARAMETERS
      OR TESTING SEQUENCE. THE ENTIRE TEST PLAN, INCLUDING PARAMETERS
      AND OPERATING SEQUENCE, IS DETERMINED BY THE OPERATOR THROUGH
      RESPONSES TO TELETYPE REQUESTS AND SETTING OF CONSOLE SWITCHES.

      THE PROGRAM PROVIDES FOR TESTING OF ALL TAPE DRIVE FUNCTIONS
      SUCH AS WRITING,READING,REWINDING,TAPE POSITIONING,EOT - BOT
      SENSING AND ASSUMES A GOOD CONTROLLER.

      HOWEVER, THE CONTROLLER IS TESTED SOMEWHAT INTRINSICALLY
      DURING THE TEST CYCLE IN ORDER TO PROVIDE FULL INFORMATION
      ABOUT ANY ERROR CONDITIONS DETECTED.

      DURING A TEST CYCLE, CHECKS ARE MADE FOR STATUS ERRORS,DATA ERRORS,
      POSITION ERRORS,WORD COUNT AND CURRENT MEMORY ADDRESS ERRORS
      WHEREVER APPLICABLE.

2.   REQUIREMENTS (HARDWARE)

      A. ANY PDP-11 PROCESSER
      B. 8K OF CORE
      C. TELETYPE
      D. TM,A,B-11 TAPE CONTROL UNIT
      E. 1 TO 8 TS03 OR TU10,N,W MAG TAPE DRIVES

3.   LOADING PROCEDURE

      A. USE STANDARD PROCEDURE FOR LOADING BINARY TAPES
      B. PROGRAM IS LOADABLE AND CHAINABLE IN 8K OF MEMORY.
         DEFAULT CHAIN MODE IS A SINGLE PASS ON DRIVE 0
         AT 9TRK,800 BPI,100 RECORDS OF 200 CHARACTES EACH,
         WITH PATTERN ONE AND ALL SWITCHES 0.

4.   STARTING PROCEDURE

      THERE ARE FOUR (4) STARTING ADDRESSES THAT MAY BE USED;
      200(8), 204(8), 210(8), AND 240(8):

      A. 200(8):   THIS ADDRESS MUST BE USED ON INITIAL START FROM
                       LOAD AS ALL PARAMETERS ARE ENTERED FROM HERE.
                       REQUESTS ARE PRINTED ON THE TELETYPE FOR ENTRY OF
                       CONTROLLER REGISTER STARTING ADDRESS, VECTOR ADDRESS,
                       UNIT NUMBER, DENSITY,PAPITY,RECORD COUNT,CHARACTER
                       COUNT,PATTERN NUMBER, TAPE MARK (EOF) OPTION,AND STALL
                       FOR READ, WRITE, AND TURNAROUND. ALL REPONSES SHOULD
                       BE MADE IN OCTAL AND WITHIN THE LIMITS OF THE PARAMETER.
                       A QUESTION MARK (?) WILL BE TYPED IF ANY
                       CHARACTER ENTERED IS NOT BETWEEN 0 THRU 7 (OCTAL).
                       THE CHARACTER MAY BE RETYPED FOLLOWING THE QUESTION
                       MARK. IF THE RESPONSE IS NOT WITHIN ITS LIMITS, A
                       QUESTION MARK (?) IS TYPED AND THE ENTIRE RESPONSE
                       MAY BE RENTERED. SOME RESPONSES REQUIRE MORE THAN ONE
                       (1) CHARACTER, BUT NONE REQUIRES MORE THAN SIX (6).
                       RESPONSES NEED NOT HAVE
                       LEADING ZEROS AND SHOULD BE TERMINATED BY A CARRIAGE
                       RETURN IF LESS THAN THE MAXIMUM NUMBER OF CHARACTERS
                       IS INPUT.

      B. 204(8):   THIS ADDRESS SHOULD BE USED ANYTIME A RESTART
                       OF THE PROGRAM IS NECESSARY AND THE PARAMETERS
                       ENTERED AT THE INITIAL START OF 200(8) NEED NOT
                       BE CHANGED. ALSO NOTE THAT ANY DATA PATTERN WHICH
                       HAD BEEN GENERATED BY SETTING THE RANDOM DATA
                       SWITCH (CONSOLE SWITCH EIGHT) WILL NOT BE OVERWRITTEN
                       AND THERFORE IS HELD IN CORE FOR USE UNTIL
                       CONSOLE SWITCH EIGHT(8) IS AGAIN SET.

      C. 210(8):   THIS ADDRESS IS THE SAME AS USING 204(8) IN THAT THE
                       PREVIOUSLY SET PARAMETERS ARE USED; HOWEVER, THE DATA
                       PATTERN IS RETURNED TO THE FIXED PATTERN ORIGINALLY
                       CALLED FOR AT THE 200(8) START. ALSO ALL STATISTICS
                       PREVIOUSLY GATHERED WILL BE CLEARED.

      D. 240(8):   THIS IS A SPECIAL ADDRESS WHICH WILL CAUSE THE
                       PROGRAM TO EXECUTE A PREDETERMINED TEST PLAN ON
                       ALL AVAILABLE UNITS. THE ONLY INPUT REQUIRED
                       BY THE OPERATOR IS A RESPONSE TO REQUESTS FOR THE
                       CONTROLLER ADDRESS, VECTOR ADDRESS, AND CONTINUOUS
                       OPERATION OF THE SEQUENCE.

                       SEE ITEM 11, (PAGE 22) FOR FULL DETAILS.

(PAGE 3)

THE FOLLOWING IS AN EXPLANATION OF THE INITIAL
START (200 OCTAL) REQUESTS AND RESPONSES:

REGISTER START: THE RESPONSE REQUIRED FOR THIS REQUEST IS TO
ENTER THE ADDRESS OF THE FIRST CONTROLLER REGISTER
(MTS) AS A SIX DIGIT UNIBUS ADDRESS.

VECTOR ADDRESS: THE RESPONSE FOR THIS REQUEST IS TO ENTER THE
INTERRUPT VECTOR ADDRESS USED BY THE CONTROLLER
AS A THREE (3) DIGIT ADDRESS.

UNIT NUMBER: THE UNIT NUMBER IS ENTERED AS ONE (1) OCTAL
CHARACTER AND MUST BE WITHIN THE LIMITS OF 0
THROUGH 7. WHEN THE UNIT NUMBER HAS BEEN ENTERED
AND IS LEGAL, THE PROGRAM TESTS FOR THE PRESENCE
OF A UNIT OF THAT NUMBER. IF THE UNIT IS
AVAILABLE A PRINTOUT OF 7 CHANNEL OR 9 CHANNEL
WILL BE MADE TO ASSIST THE OPERATOR IN SETTING
DENSITY AND PARITY. IF THE UNIT IS NOT AVAILABLE,
A MESSAGE STATING SO WILL BE PRINTED AND A NEW
UNIT NUMBER REQUEST WILL BE ISSUED. WHEN A
GOOD UNIT NUMBER HAS BEEN ENTERED, REQUESTS FOR
OPERATING DENSITY AND PARITY ARE MADE FOR
THAT UNIT AND SHOULD BE RESPONDED TO ACCORDING
TO THAT PARTICULAR UNIT'S NEEDS. AS MANY AS
EIGHT (8) UNIT NUMBER REQUESTS MAY BE USED,
HOWEVER, AT LEAST ONE MUST BE USED. THE UNIT
NUMBER AND THEIR RESPECTIVE DENSITY AND PARITY
MAY BE ENTERED IN ANY ORDER. THE INFORMATION
FOR EACH UNIT ENTERED IS LOADED INTO A TABLE
FOR REFERENCE IN TESTING. IF LESS THAN EIGHT(8)
UNITS ARE REQUIRED, THEN RESPONDING TO THE
UNIT NUMBER REQUEST WITH A CARRIAGE RETURN WILL
TERMINATE THE UNIT ENTRIES AND CONTINUE
TO THE NEXT PARAMETER. IT SHOULD BE REMEMBERED
THAT AT LEAST ONE UNIT NUMBER REQUEST MUST BE
ENTERED. IF THE FIRST REQUEST IS RESPONDED
TO BY A CARRIAGE RETURN, THEN THE REQUEST
WILL BE REPEATED.

DENSITY: THE DENSITY REQUEST IS RESPONDED TO BY ONE (1) OCTAL
CHARACTER AND MUST BE WITHIN THE LIMITS OF 0 THRU 3.
AS EACH UNIT NUMBER IS ENTERED, A REQUEST FOR THE
OPERATING DENSITY FOR THAT UNIT IS TYPED. THE
RESPONSE MEANINGS ARE AS FOLLOWING:

A. 0 = 200BPI, 7 CHANNEL NRZ1
B. 1 = 556BPI, 7 CHANNEL NRZI
C. 2 = 800BPI, 7 CHANNEL NRZI
D. 3 = 800BPI, 9 CHANNEL NRZI

B-13

(PAGE 4)

PARITY: THE PARITY REQUEST IS RESPONDED TO BY ONE (1)
                 OCTAL CHARACTER AND MUST BE EITHER 0 OR 1.

                         A. 1 = EVEN PARITY
                         B. 0 = ODD PARITY

RECORD COUNT: THIS REQUEST IS RESPONDED TO BY A SIX (6) CHARACTER
                 OCTAL NUMBER FROM 1 TO 177777. REMEMBER LEADING
                 ZEROS ARE NOT REQUIRED AND IF LESS THAN SIX
                 CHARACTERS ARE ENTERED, A CARRIAGE RETURN
                 WILL TERMINATE THE RESPONSE. THE RECORD COUNT
                 IS USED IN CONJUCTION WITH THE CHARACTER COUNT
                 TO ESTABLISH A BLOCKING FACTOR FOR USE IN READ OR
                 WRITE CYCLES.

CHARACTER COUNT: THIS RESPONSE IS ENTERED AS FOUR (4) OCTAL
                 CHARACTERS WITHIN THE LIMITS OF 4 THRU 4000. AGAIN
                 LEADING ZEROS ARE NOT REQUIRED AND A CARRIAGE
                 RETURN TERMINATES A LESS THAN FOUR (4) CHARACTER
                 RESPONSE. THE CHARACTER COUNT IN CONJUNCTION
                 WITH THE RECORD COUNT IS USED TO ESTABLISH
                 THE BLOCK SIZE (CHARACTERS PER RECORD, AND
                 RECORDS PER BLOCK) USED IN READ AND WRITE CYCLES
                 THE SAME BLOCKING IS USED ON ALL AVAILABLE UNITS.

PATTERN NUMBER: THIS RESPONSE IS A TWO (2) CHARACTER OCTAL
                 NUMBER WITHIN THE LIMITS OF 0 THRU 20(8).
                 THE NUMBER ENTERED WILL CAUSE A SPECIFIC DATA
                 PATTERN TO BE USED FOR ALL READING AND WRITING. THIS
                 DATA PATTERN IS NOT CHANGED UNLESS RANDOM DATA
                 IS REQUESTED BY SETTING CONSOLE SWITCH EIGHT (8)
                 TO A ONE. RESETTING OF THE RANDOM DATA SWITCH
                 DOES NOT CAUSE REVERSION TO THE FIXED PATTERN,
                 BUT WILL HOLD THE LAST GENERATED PATTERN UNTIL
                 A RESTART IS DONE FROM LOCATION 210(8) OR 200(8).
                 THE SELECTION OF DATA PATTERN ZERO (0) HAS A
                 SPECIAL USE. PATTERN NUMBER ZERO (0) WILL
                 CAUSE TO BE READ IN AT THE HIGH SPEED PAPER
                 TAPE READER ANY DATA PATTERN DESIRED.
                 THE EXTERNAL INPUT DATA THOUGH THE READER
                 IS DONE BY PREPARING A PAPER TAPE WITH A PROGRAM
                 CALLED DTC. (MAINDEC-11-DZTUF) ANY CONFIGURATION
                 OF BITS AND CHARACTERS MAY BE USED AND A LIMIT
                 OF 377(8) CHARATERS IS IMPOSED. WHEN EXTERNAL
                 DATA IS INPUT, THE ENTIRE WRITE BUFFER IN
                 CORE IS FILLED WITH THE PATTERN SO THAT ANY
                 SIZE RECORD MAY BE USED. DATA PATTERN
                 ZERO (0) EXTERNAL PAPER TAPE NEED ONLY
                 BE READ ONCE AT INITIAL START OF 200(8), AND
                 NEED NOT BE READ AGAIN UNLESS OVERWRITTEN BY
                 RANDOM DATA. BE SURE TO LOAD THE READER
                 BEFORE PRESSING START.

                 SEE ITEM 5, (PAGE 7) FOR A DESCRIPTION OF THE
                 DATA PATTERNS.

TAPE MARK: THE TAPE MARK REQUEST IS USED TO DETERMINE IF
THE OPERATOR WISHES TO HAVE EACH DATA BLOCK
SEPARATED BY A TAPE MARK (OFTEN CALLED EOF FOR
END OF FILE). IF RESPONDED TO BY A ONE(1) THE
TAPE MARK WILL BE WRITTEN AND WHEN READING WILL
BE EXPECTED AT THE END OF EACH DATA BLOCK. A
ZERO(0) RESPONSE WILL DISALLOW THE TAPE MARK
OPTION. PLEASE NOTE THAT THE TAPE MARK RECORD
INCREASES THE BLOCK SIZE BY ONE(1) RECORD;
IN OTHER WORDS, A BLOCK OF 100 RECORDS WILL
HAVE THE TAPE MARK AS RECORD 101.

SINGLE PASS: IF RESPONDED TO WITH A ONE, THE PROGRAM WILL HALT
AND PRINT AN END OF PASS MESSAGE WHEN THE LAST
AVAILABLE UNIT REACHES END OF TAPE AND IS REWOUND.

STALLS: THE STALL REQUESTS ARE RESPONDED TO BY A SIX (6)
CHARACTER OCTAL NUMBER WITHIN THE LIMITS OF 1
THRU 177777. LEADING ZEROS ARE NOT REQUIRED AND
AN ENTRY OF LESS THAN SIX (6) CHARACTERS SHOULD
BE TERMINATED BY A CARRIAGE RETURN. EACH INCREMENT
OF THE VALUE ADDS ABOUT 2.6 MICSEC TO THE DELAY.

                READ: THE TIME DELAY BETWEEN EACH RECORD READ
                WRITE: THE TIME DELAY BETWEEN EACH RECORD WRITTEN
                TURN AROUND: TIME DELAY BETWEEN CHANGES OF
                              TAPE DIRECTION (FORWARD,TO REVERSE,ETC.)
                              AND BETWEEN BLOCKS.

FIXED PARAMETERS: IT SHOULD BE NOTED THAT ALL PARAMETERS EXCEPT
FOR THE UNIT DESCRIPTION VALUES (UNIT
NUMBER, DENSITY, AND PARITY) HAVE NOMINAL
VALUES ALREADY STORED IN THE PROGRAM.
AS EACH PARAMETER REQUEST (PATTERN NUMBER, RECORD
COUNT, CHARACTER COUNT, AND STALLS) IS TYPED.
ITS PRESENT STORED VALUE IS ALSO PRINTED.
IF THESE VALUES NEED NOT BE CHANGED, SIMPLY
TYPE A CARRIAGE RETURN AS RESPONSE AND NO
CHANGE WILL BE MADE. EACH START OF THE PROGRAM
AT 200(8) WILL SHOW THE CURRENT VALUES OF THESE
PARAMETERS AS PER THE LAST ENTRY. WHEN A
FRESH LOAD OF THE PAPER TAPE IS DONE. THE
PARAMETERS WILL REFLECT THE FIXED VALUES STORED
IN THE PROGRAM.

         A. RECORD COUNT = 100
         B. CHARACTER COUNT = 200
         C. PATTERN NUMBER = 1
         D. READ STALL = 1
         E. WRITE = 1
         F. TURN AROUND = 1

SAMPLE START AT 200(8):

       THE FOLLOWING IS A SAMPLE OF THE
       PRINTED REQUESTS AND THEIR RESPONSES.
       RESPONSES ARE ENCLOSED IN PARENS FOR
       CLARITY ONLY AND (CR) MEANS CARRIAGE RETURN

LOAD ADDRESS 200(8), SET CONSOLE SWITCHES, PRESS START SWITCH:

       TM,A,B=11;TS03 OR TU10,N,W MULTIDRIVE DATA RELIABILTY EXERCISER
       ENTER CONDITIONS IN OCTAL
       REGISTER START = 172520 (CR)
       VECTOR ADDRESS = 224 (CR)
       UNIT NUMBER=(5) 9 TRK
       DENSITY=(3)
       PARITY=(0)
       UNIT NUMBER=(2) 7 TRK
       DENSITY=(2)
       PARITY=(1)
       UNIT NUMBER=(CR)
       RECORD COUNT=100 (500)(CR)
       CHARACTER COUNT=201 (38)?(7)(CR)
       PATTERN NUMBER=1 (22)
       ?
       (6)(CR)
       TAPE MARK = 0 (1)(CR)
       SINGLE PASS = 0(CR)

       ENTER STALLS
       READ=1 (CR)
       WRITE=1 (CR)
       TURN AROUND=1 (3000)(CR)

THE PROGRAM WILL NOW PERFORM THE TEST CYCLE SET IN
THE CONSOLE SWITCHES ON UNIT FIVE (5) THEN TWO (2),
ONE BLOCK ON EACH UNIT PER CYCLE, USING DATA PATTERN
NUMBER SIX (6) WITH A BLOCKING FACTOR OF 37 CHARACTERS
PER RECORD AND 500 RECORDS PER BLOCK. THE DELAYS ARE SET
FOR MINIMUM ON READ AND WRITE, AND APPROXIMATELY .75
SECONDS ON TURN AROUND.

5.   DATA PATTERNS

       THERE ARE TWENTY DATA PATTERN GENERATORS STORED IN CORE
       AND ANY ONE OF THESE MAY BE SELECTED. THE ONE UNIQUE
       CASE IS PATTERN ZERO(0); SELECTION OF PATTERN ZERO(0)
       REQUIRES THAT A PREVIOUSLY PREPARED PAPER TAPE BE
       ENTERED AT THE HIGH SPEED READER. THIS TAPE CONTAINS
       A DATA PATTERN OF NO MORE THAN 377 OCTAL
       CHARACTERS. THE FIRST CHARACTER READ IN IS THE
       NUMBER OF ACTUAL DATA CHARACTERS THAT ARE CONTAINED
       ON THE TAPE. EACH DATA CHARACTER MAY BE ANY
       COMBINATION OF BITS AND WILL BE LOADED INTO CORE
       AS THEY APPEAR ON THE TAPE. NO MATTER HOW MANY
       CHARACTERS ARE ON TAPE, THE ENTIRE WRITE BUFFER (2000 CHARACTERS)
       WILL BE FILLED WITH THE PATTERN ENTERED SO THAT ANY
       SIZE RECORD CAN BE USED.

       THE FOLLOWING IS A LIST OF THE DATA PATTERNS AVAILABLE:

       DATA0:   EXTERNAL INPUT THRU HIGH SPEED READER (SEE DTC; MAINDEC-11-DZTUF-A)
       DATA1:   ALL ONE BITS IN ALL CHARACTERS
       DATA2:   ALL ZERO BITS IN ALL CHARACTERS
       DATA3:   A ONE BIT WALKING FROM RIGHT TO LEFT IN A FIELD OF ZEROS
       DATA4:   A ZERO BIT WALKING FROM RIGHT TO LEFT IN A FIELD OF ONES.
       DATA5:   ALTERNATING ONE AND ZERO BITS IN EACH CHARACTER
       DATA6:   ALTERNATING ZERO AND ONE BITS IN EACH CHARACTER
       DATA7:   SAME AS DATA5 BUT WITH EVERY OTHER CHARACTER COMPLEMENTED
       DATA10: SAME AS DATA6 BUT WITH EVERY OTHER CHARACTER COMPLEMENTED
       DATA11: INCREMENTING CHARACTERS (000-377)
       DATA12: DECREMENTING CHARACTERS (377-000)
       DATA13: ALTERNATING CHARACTERS OF ALL ZERO AND ALL ONE BITS
       DATA14: ALTERNATING CHARACTERS OF ALL ONE AND ALL ZERO BITS
       DATA15: SPECIAL PATTERN OF A WALKING ZERO BIT REPEATED 4 TIMES
       DATA16: IBM COMPAT PATTERN 1: RIPPLE
       DATA17: IBM COMPAT PATTERN 2: FIXED (ABCDEF)
       DATA20: IBM COMPAT PATTERN 3: FIXED (J)

6.   RANDOMIZATION

THERE ARE THREE (3) VALUES THAT MAY BE GENERATED RANDOMLY;
DATA, CHARACTER COUNT, AND RECORD COUNT. THESE ARE NORMALLY SET TO
SOME FIXED VALUE BUT MAY BE RANDOMIZED BY SETTING THE APPROPRIATE
CONSOLE SWITCHES.

        A. RANDOM DATA: (CONSOLE SWITCH 8)
            GENERATES AN ENTIRE BUFFER, CHARACTER BY
            CHARACTER, OF RANDOM DATA WHEN SWITCH 8
            IS SET TO A ONE. ONCE SET, THE RESETTING OF
            SWITCH 8 CAUSES THE LAST GENERATED PATTERN
            TO BE RETAINED IN CORE. A RESTART AT LOCATION
            200(8) OR 210(8) WILL CAUSE REVERSION OF THE
            DATA TO THE FIXED PATTERN REQUESTED INITIALLY.
            A RESTART AT LOCATION 204(8) WILL HOLD
            THE LAST GENERATED PATTERN IN CORE UNTIL SWITCH
            8 IS AGAIN SET.
            ALTHOUGH THE DATA IS GENERATED AS RANDOM,
            THE PROGRESSION OF RANDOM CHARACTERS IS ALWAYS
            THE SAME FROM THE OUTSET OF RANDOMIZATION.
            THEREFORE IT IS POSSIBLE TO GENERATE ONE TAPE REEL
            OF RANDOM DATA ON ONE UNIT, RESTART THE
            PROGRAM TO RE-ESTABLISH THE OUTSET POINT, AND
            READ THE RANDOM TAPE REEL ON ANOTHER UNIT FOR
            COMPATABILITY TESTING. IN MULTIDRIVE SYSTEMS THE SAME
            BLOCK OF DATA, WHETHER RANDOM OR FIXED, IS
            WRITTEN OR READ ON EACH AVAILABLE UNIT IN THE
            ORDER THAT THEY WERE ENTERED, BEFORE BEING CHANGED.

        B. RANDOM CHARACTER COUNT: (CONSOLE SWITCH 7)
            GENERATES A DIFFERENT NUMBER OF CHARACTERS
            PER RECORD TO BE WRITTEN ON EACH BLOCK CYCLE.
            THE SAME NUMBER OF CHARACTERS PER RECORD IS
            WRITTEN OR READ ON EACH AVAILABLE UNIT BEFORE
            BEING CHANGED. RESETTING SWITCH 7 HOLDS THE
            LAST VALUE GENERATED.

        C. RANDOM RECORD COUNT: (CONSOLE SWITCH 6)
            GENERATES A DIFFERENT NUMBER OF RECORDS
            FOR EACH BLOCK OF DATA WRITTEN OR READ ON
            EACH BLOCK CYCLE. THE SAME NUMBER OF RECORDS
            IS WRITTEN OR READ ON EACH AVAILABLE UNIT BEFORE
            BEING CHANGED. RESETTING SWITCH 6 HOLDS LAST VALUE
            GENERATED.

7.   DYNAMIC PARAMETERS:

          THE THREE (3) STALL VALUES ARE CONSIDERED TO BE DYNAMIC
          PARAMETERS AS THEY MAY BE CHANGED WHILE THE PROGRAM IS
          RUNNING BY TYPING A CONTROL C CHARACTER AT THE TELETYPE.
          AS SOON AS THE BUS IS RELEASED BY THE MAG TAPE OPERATION
          IN PROGRESS, THE PROGRAM WILL RESPOND TO THE CONTROL C INPUT
          BY TYPING A REQUEST FOR NEW STALL PARAMETERS. THE LAST VALUES
          THAT WERE ENTERED WILL BE PRINTED AS THE STORED VALUES AND MAY
          BE CHANGED BY ENTERING NEW VALUES OR LEFT UNCHANGED BY
          TYPING A CARRIAGE RETURN.

****

8.   THIS PROGRAM HAS BEEN MODIFIED TO RUN ON A PROCESSOR WITH OR WITHOUT
          A HARDWARE SWITCH REGISTER. WHEN FIRST EXECUTED THE PROGRAM TESTS
          THE EXISTENCE OF A HARDWARE SWITCH REGISTER. IF NOT FOUND A
          SOFTWARE SWITCH REGISTER LOCATION (SWREG=LOC. 176) IS DEFAULTED TO.
          IF THIS IS THE CASE, UPON EXECUTION THE CONTENTS OF THE SWREG ARE
          DUMPED IN OCTAL ON THE CONSOLE TTY AND ANY CHANGES ARE REQUESTED

                   (IE)   SWR=XXXXXX NEW=

          POSSIBLE RESPONSES ARE:

          1.   <CR>   IF NO CHANGES ARE TO BE MADE
          2.   6 DIGITS 0-7   TO REPRESENT IN OCTAL THE NEW SWITCH REGISTER
                                 VALUE ;LAST DIGIT FOLLOWED BY <CR>.
          3.   ^U   TO ALLOW REENTERING VALUE IF ERROR IS COMMITTED
                                 KEYING IN SWREG VALUE.
          4.   <LF>   ONLY VALID FOR ACT-11 SYSTEMS-DO NOT USE

          BUILT INTO THE PROGRAM IS THE ABILITY TO DYNAMICALLY CHANGE THE
          CONTENTS OF SWREG DURING PROGRAM EXECUTION. BY STRIKING ^G
          (CNTL G) ON CONSOLE TTY THE OPERATOR SETS A REQUEST FLAG TO CHANGE
          THE CONTENTS OF SWREG, WHICH IS PROCESSED IN KEY AREAS OF THE PROGRAM
          CODE (IE) ERROR ROUTINES, AFTER HALTS END OF PASS, AND OTHER
          APPLICABLE AREAS.

****

8.1 CONSOLE SWITCH SETTINGS

THE CONSOLE SWITCHES ARE USED TO SET UP THE TEST CYCLE
DESIRED, TO GENERATE RANDOM VALUES, AND TO CONTROL ERROR
RESPONSES. THE SWITCHES SHOULD BE SET IN THE DESIRED
MANNER BEFORE PRESSING THE START SWITCH BECAUSE THEY
ARE ALL DYNAMIC AND WILL RUN THE PROGRAM IN ANY
CONFIGURATION. ALL SWITCHES SET TO ZERO(0) IS NORMAL.

SW15:   1=STOP ON ERROR
        0=CONTINUE ON ERROR

SW14:   1=YOZZLE ON CURRENT BLOCK
        0=DO NOT YOZZLE ON BLOCK

SW13:   1=DO NOT CHECK DATA ERRORS
        0=CHECK DATA ERRORS

SW12:   1=DO NOT CHECK WRITE STATUS ERRORS
        0=CHECK WRITE STATUS ERRORS

SW11:   1=DO NOT CHECK READ STATUS ERRORS
        0=CHECK READ STATUS ERRORS

SW10:   1=DO NOT PRINT ANY ERRORS
        0=PRINT ALL ERRORS

SW9:   1=REWIND ALL AVAILABLE TAPES
        0=DO NOT REWIND

SW8:   1=GENERATE RANDOM DATA
        0=USED FIXED DATA

SW7:   1=GENERATE RANDOM CHARACTER COUNT
        0=USE FIXED CHARACTER COUNT

SW6:   1=GENERATE RANDOM RECORD COUNT
        0=USED FIXED RECORD COUNT

SW5:   1=YOZZLE ON CURRENT RECORD
        0=DO NOT YOZZLE ON RECORD

SW4:   1=PRINT STATISTICS
        0=DO NOT PRINT STATISTICS

SW3:   1=DO NOT READ
        0=READ

SW2:   NOT USED

SW1:   1=DISABLE WRITE AND READ RETRY OPTION
        0=ENABLE WRITE AND READ RETRY OPTION

SW0:   1=DO NOT WRITE
        0=WRITE

SWITCH EXPLANATION AND EXAMPLES:

SW0+SW3:   THESE SWITCHES ARE USED TO CONTROL THE SEQUENCE
OF MAG TAPE OPERATIONS PREFORMED ON EACH AVAILABLE
UNIT. THE BLOCK OF DATA DESCRIBED THROUGH
THE RESPONSES TO TELETYPE REQUESTS AT INITIAL START
WILL BE EITHER WRITTEN OR READ FROM EACH AVAILABLE
UNIT IN THE ORDER THAT THEY WERE ENTERED. THE SEQUENCE
OF OPERATIONS IS CALLED A CYCLE, AND WILL BE PERFORMED
CONTINUOUSLY UNTIL STOPPED BY THE OPERATOR. WHEN END
OF TAPE IS REACHED, THE UNIT WILL BE REWOUND AND
FLAGGED AS UNAVAILABLE FOR TEST UNTIL ALL UNITS HAVE
REACHED EOT, AT WHICH TIME TESTING IS RESUMED ON ALL
AVAILABLE UNITS.

      EXAMPLES: SW0+SW3

        A. SW0=0,SW3=1   WRITE ONLY X RECORDS OF Y CHARACTERS
        B. SW0=1,SW3=0   READ ONLY X RECORDS OF Y CHARACTERS
        C. SW0=0,SW3=0   WRITE THEN BACKSPACE AND READ X RECORDS

SW1:   SWITCH ONE(1), WHEN SET TO A ZERO (0), WILL
CAUSE ANY DATA RELATED WRITE ERROR TO BE RETRIED.
THE RETRY SCHEME CONSISTS OF REWRITING THE RECORD
IN THE SAME SPOT ON THE TAPE FOUR (4) TIMES. IF
ALL FOUR (4) REPEATS ARE SUCCESSFUL, THE RECORD
IS CONSIDERED RECOVERED, AND A TAPE WRITE ERROR
IS LOGGED. IF ANY OF THE FOUR (4) REPEATS
IS UNSUCCESSFUL, A WRITE WITH EXTENDED
INTERRECORD GAP IS DONE, A SUSPECTED BAD TAPE
SPOT LOGGED AT THIS BLOCK AND RECORD NUMBER,
AND A SECOND RETRY OF FOUR REPEATS IS DONE.
IF AFTER FOUR (4) RETRIES, THE RECORD CANNOT
BE RECOVERED A NOTIFICATION IS PRINTED, AND
TESTING IS RESUMED ON THE NEXT RECORD.
IF 20(8) BAD TAPE SPOTS ARE FOUND, THE UNIT
WILL BE REWOUND AND REMOVED FROM TESTING WITH
AN APPROPRIATE MESSAGE PRINTED.

        SWITCH ONE (1), WHEN SET TO A ZERO (0), WILL ALSO
CAUSE ANY DATA RELATED READ ERROR TO BE RETRIED.
THE RETRY SCHEME CONSISTS OF REREADING THE RECORD
A MAXIMUM OF FOUR (4) TIMES. IF THE RECORD IS
SUCCESSFULLY RECOVERED ON ANY OF THE REREADS
IT IS CONSIDERED FOR STATISTICS PURPOSES TO BE
A SOFT READ ERROR AND TESTING CONTINUES IF THE
REREADS FAIL TO RECOVER THE RECORD, THE ERROR
IS LOGGED AS A HARD READ ERROR.

SW4:   SWITCH FOUR (4) WHEN SET WILL PRINT THE
STATISTICS GATHERED FOR EACH UNIT. THE NUMBER
WILL BE PRINTED AT THE END OF A BLOCK CYCLE.

        SEE ITEM 10, PAGE 20 FOR FULL DETAILS.

SW5: SWITCH FIVE (5) WHEN SET DURING A READ
OPERATION WILL CAUSE THE PROGRAM TO
CONTINUOUSLY READ THE CURRENT RECORD BY
SPACING REVERSE OVER THE RECORD AND
REREADING THAT RECORD. THIS TAPE MOVEMENT
IS CALLED YOZZLING. THERE IS A SOFTWARE
DELAY EXECUTED BETWEEN EACH SPACE/READ
OF THE RECORD AND IT MAY BE VARIED BY
TYPING CONTROL C ON THE TELETYPE DURING
THE EXECUTION OF THE YOZZLE AND RESPONDING
TO THE PRINTED REQUEST WITH A SIX (6)
DIGIT VALUE. THE YOZZLE STALL IS PRESET
TO A VALUE OF 1000 IN THE PROGRAM TO
PREVENT EXCESSIVE TAPE WEAR, BUT MAY BE
SET TO ANY VALUE THROUGH THE TELETYPE.

SW6-8: THESE THREE (3) SWITCHES CONTROL THE RANDOMIZATION
OF DATA AND BLOCK SIZE AND MAY BE SET
AND RESET AT ANY TIME. THE ACTUAL CHANGE
WILL TAKE PLACE BETWEEN BLOCK CYCLES.

SW9: SWITCH NINE (9) WHEN SET WILL CAUSE ALL
AVAILABLE TAPE UNITS TO BE REWOUND AT
THE END OF THE CURRENT BLOCK CYCLE, TESTING
WILL BE RESUMED AT A BLOCK COUNT OF
ONE (1) WHEN ALL UNITS HAVE REACHED BOT.

SW10-13: THESE SWITCHES ARE USED TO CONTROL THE
ERROR HANDLING TO BE DONE ON THE TAPE
OPERATION DESCRIBED BY SWITCHES 0+3.

A. SWITCH TEN (10) WHEN SET TO A ONE
WILL DISALLOW ANY ERROR PRINTOUTS MADE
ON THE OPERATION IN PROGRESS. CATASTROPHIC
FAILURES AND INFORMATION PRINTOUTS WILL
STILL OCCUR. IE: UNIT NOT AVAILABLE, ILLEGAL
BOT, DROP OR PICK OVERFLOW, AND EOT REWIND.

B. SWITCH ELEVEN (11) WHEN SET TO A ONE
WILL DISALLOW THE CHECKING FOR STATUS
ERRORS ON READ OPERATIONS.

C. SWITCH TWELVE (12) WHEN SET TO A ONE
WILL DISALLOW THE CHECKING FOR STATUS
ERRORS ON WRITE OPERATIONS.

D. SWITCH THIRTEEN (13) WHEN SET TO A ONE
WILL DISALLOW THE CHECKING OF READ
DATA. THIS SWITCH HAS NO EFFECT ON
STATUS CHECKING.

(PAGE 13)

SW14: SWITCH FOURTEEN (14) IS USED DURING A
READ ONLY OPERATION; WHEN SET, THE
BLOCK OF DATA BEING READ WILL CONTINUOUSLY
BE READ AND SPACED OVER SO THAT TAPE WILL
REMAIN AT THE SAME BLOCK. WHEN RESET, THE
TAPE WILL BE ALLOWED TO MOVE FORWARD AND DATA
BLOCKS WILL BE READ PROGRESSIVELY.
THIS IS A BLOCK YOZZLE.

SW15: SWITCH FIFTEEN (15) WHEN SET TO A ONE,
WILL CAUSE THE PROGRAM TO HALT ON ANY
ERROR DETECTED BY THE OPERATION IN PROGRESS.
IF BOTH SWITCH TEN (10) AND FIFTEEN (15)
ARE SET, THE ACTUAL ERROR DETECTED WILL
NOT BE PRINTED BUT WILL CAUSE A HALT.
IF SWITCH TEN (10) IS RESET BEFORE PRESSING
CONTINUE, THE ERROR WHICH CAUSED THE HALT
WILL BE PRINTED BEFORE TESTING IS RESUMED.

9.   ERROR PRINTOUTS

       THERE ARE THREE TYPES OF ERROR PRINTOUTS MADE BY
       THE PROGRAM; OPERATION ERRORS, DATA ERRORS, AND CONDITION
       ERRORS. EACH ERROR MESSAGE PRINTED IS PRECEDED BY A
       HEADER WHICH CONTAINS THE UNIT NUMBER, BLOCK COUNT NUMBER,
       BAD RECORD NUMBER PLUS TOTAL NUMBER OF RECORDS, SIZE OF
       RECORD, AND TYPE OF OPERATION WHICH CAUSED ERROR.

       A. OPERATION ERRORS:

               THESE ARE ERRORS WHICH CAN OCCUR AS A DIRECT
               RESULT OF A TAPE OPERATION.

               1. READ/WRITE STATUS ERRORS: THESE ARE INDICATED BY THE ERROR BIT
                                                 (BIT 15) OF THE TAPE COMMAND REGISTER
                                                 BEING SET TO A ONE.

               2. RECORD LENGTH ERRORS: THESE ARE INDICATED BY A BYTE COUNT
                                                 OTHER THAN ZERO (0) OR AN INCORRECT
                                                 CURRENT MEMORY ADDRESS OR BOTH

               3. TAPE POSITIONING ERRORS: THESE ARE INDICATED BY A SPACE
                                                 COUNT OTHER THAN ZERO (0), NO BOT FOUND
                                                 FROM A REWIND, OR NO TAPE UNIT
                                                 READY AT THE END OF REWIND.

       B. DATA ERRORS:

               DATA ERRORS WILL OCCUR WHEN TAPE IS
               BEING READ AND THE DATA DOES NOT MATCH
               THE EXPECTED DATA.

       BECAUSE DATA RECORDS CAN BE UP TO TWO THOUSAND
       CHARACTERS LONG, AN ERROR CONDITION WHICH WILL CAUSE
       THE ENTIRE RECORD TO READ INCORRECTLY COULD CAUSE A VERY
       LENGTHY PRINTOUT. THEREFORE, A COUNTER OF SUCCESSIVE
       BAD CHARACTERS IS EMPLOYED. IF TEN (10) CHARACTERS
       IN SUCCESSION ARE BAD, A NOTIFICATION IS PRINTED
       (BAD RECORD) AND THE NEXT TWENTY (20) CHARACTERS
       ARE SKIPPED BEFORE CHECKING IS RESUMED. IF THE BAD
       RECORD CONDITION OCCURS THREE (3) TIMES IN ONE
       RECORD, THE REST OF THE RECORD IS SKIPPED, DOWN
       TO THE LAST TEN (10) CHARACTERS, WHICH WILL BE
       CHECKED. THE SKIPPING AND RESUMPTION OF CHECKING WILL
       ONLY BE DONE ON RECORDS WHICH ARE LONG ENOUGH
       TO ALLOW IT.

C. CONDITION ERRORS: THESE ERRORS REFLECT THE STATE OF THE TAPE
                       SYSTEMBEFORE AND AFTER AN OPERATION.

    1. EOT: WHEN AN EOT (END OF TAPE) IS ENCOUNTERED DURING
        EITHER A READ OR A WRITE, THAT UNIT IS FLAGGED AS
        UNAVAILABLE FOR TESTING AND IS REWOUND UNTIL ALL
        AVAILABLE UNITS HAVE REACHED EOT. AT WHICH TIME
        TESTING IS RESUMED ON ALL AVAILABLE UNITS.

    2. ILLEGAL BOT: WHEN A UNIT ENCOUNTERS BEGINNING OF TAPE (BOT)
        DURING A READ OPERATION THE ERROR IS
        PRINTED AND THE UNIT DROPPED FROM TESTING
        UNTIL ALL ARE RESTARTED ON THE NEXT PASS.

    3. DROP DRIVE:UNIT BECOMES UNAVAILABLE DUE TO LOSE OF SELECT REMOTE,
        BOT DURING REWIND,OR NO TUR WHEN MAKING INITIAL SELECTION
        UNIT IS DROPPED,STATISTICS PRINTED, TESTING WILL RESUME
        AT BEGINNING OF NEXT PASS.

    4. CONTROLLER NOT READY: BEFORE ANY OPERATION IS ATTEMPTED THE CONTROLLER
        IS CHECKED FOR READY. IF IT IS NOT READY, AN
        ERROR WILL BE PRINTED AND THE PROGRAM WILL STOP.

    5. NO INTERRUPT RETURNED: EACH TAPE OPERATION SHOULD BE TERMINATED BY
        SETTING AN INTERRUPT IN THE CPU. IF NO
        INTERRUPT IS RETURNED WITHIN THE APPROPIATE
        TIME, AN ERROR IS PRINTED.

    6. NO MORE UNITS TO TEST: IF ALL UNITS HAVE BEEN DROPPED
        FOR CATASTROPHIC ERRORS, THE PROGRAM WILL STOP.

E. EXAMPLES:

    GLOSSARY: BN = BLOCK NUMBER
                 RN = RECORD NUMBER (X) OF A TOTAL OF (Y)
                 RS = RECORD SIZE IN CHARACTERS PER RECORD
                 WE = WRITE ERROR
                 RE = READ ERROR
                 SE = SPACE ERROR
                 F = FORWARD
                 CR = COMMAND REGISTER
                 CS = STATUS REGISTER
                 WC = BYTE COUNTER
                 CA = CURRENT MEMORY ADDRESS POINTER AND EXPECTED VALUE
                 CN = CHARACTER NUMBER
                 G = GOOD DATA (SHOWN IN BIT FORMAT AS IN CORE)
                 B = BAD DATA (SHOWN IN BIT FORMAT AS IN CORE)
                 ERR AMT = NUMBER LEFT TO SPACE
                 TM = TAPE MARK (OFTEN CALLED EOF FOR END OF FILE)
                 LPC = LONGITUDINAL PARITY CHECK (RECEIVED - EXPECTED)
                 PATTRN = DATA PATTERN (R=RANDOM)

EXAMPLE 1

EXAMPLE 1: IN THIS EXAMPLE A TAPE VERTICAL PARITY ERROR
           WAS DETECTED DURING A WRITE OPERATION OF THE
           TWELVTH (12) RECORD OF THE BLOCK. THE WORD
           COUNT AND CURRENT MEMORY ADDRESS ARE CORRECT.
           THE RETRY OPTION WAS DISABLED.

UNIT NO. 3 *DEN 1 *PAR 0 *PATTRN 1
BN 406*RN 12-200*RS 2000*WE
COMD 1010001111000100
STAT 0001000001000001
WC 0
CA 14436-14436

EXAMPLE 2

EXAMPLE 2: IN THIS EXAMPLE A RECORD LENGTH ERROR WAS
           DETECTED WHILE READING THE FIRST RECORD OF
           THE BLOCK. THE RETRY OPTION WAS DISABLED. THE
           WORD COUNT SHOWS A COUNT OF 20 CHARACTERS
           LEFT TO BE TRANSFERRED. THE CURRENT MEMORY
           ADDRESS REFLECTS THAT A SHORTAGE OF 20
           CHARACTERS TRANSFERRED HAD OCCURRED. IN
           THIS EXAMPLE THE STATUS AND COMMAND
           REGISTERS DO NOT SHOW ANY ERROR, BUT
           THE LPC IS SHOWN TO BE INCORRECT.

UNIT NO. 7 *DEN 2 *PAR 0 *PATTRN 6
BN 10*RN 1-100*RS 50*RE F***
COMD 0100011111000100
STAT 0000000001000001
WC 20
CA 12466-12506
LPC 337 -147

EXAMPLE 3

EXAMPLE 3: IN THIS EXAMPLE THE TAPE UNIT WAS TRYING
           TO SPACE OVER THE 15 RECORDS IN
           THE BLOCK IN ORDER TO ESTABLISH PROPER
           POSITION TO BEGIN READING.
           THE OPERATION WAS TERMINATED
           BEFORE THE ENTIRE 15 RECORDS WERE TRAVERSED
           AND AN ERROR SHOWN BECAUSE THE TAPE IS
           NOT IN PROPER POSITION TO BEGIN READING.

UNIT NO. 0 *PATTRN R
BN 2*RN 15-15*RS 23 *SE
ERR AMT 4

EXAMPLE 4

EXAMPLE 4: IN THIS EXAMPLE UNIT NUMBER ONE (1) HAD BEEN
           REWOUND VIA CONSOLE SWITCH NINE (9) AND AT THE
           COMPLETION OF THE OPERATION BOT WAS NOT SET IN
           THE STATUS REGISTER.

UNIT NO. 1 *DEN 3 *PAR 0 *PATTRN R
BN 3002*RN 65-65*RS 10
NO BOT ON REWIND-HALT

EXAMPLE 5

EXAMPLE 5: IN THIS EXAMPLE TWO BAD CHARACTERS WERE
           READ FROM TAPE IN THE FORWARD DIRECTION.
           THE FIRST (0) AND THE THIRTEENTH (13) CHARACTERS
           OF THE TOTAL NUMBER OF SIXTEEN (16) CHARACTERS
           IN THE BLOCK ARE BAD. CHARACTER NUMBER
           ZERO (0) HAS DROPPED BIT NUMBER FIVE (5) AND
           CHARACTER NUMBER TWELVE (12) HAS PICKED UP
           BIT NUMBER SEVEN (7).

UNIT NO. 5 *DEN 3 *PAR 0 *PATTRN 5
BN 12*RN 3-10*RS 15*DE-F**
CN 0
G; 10101010
B; 10001010
CN 12
G; 01010101
B; 11010101

        EXAMPLE 6

EXAMPLE 6: IN THIS EXAMPLE UNIT NUMBER SIX (6) HAS
        REACHED END OF TAPE (EOT) FOR THE 1ST TIME AND WILL BE REWOUND.
        TESTING WILL RESTART ON UNIT NUMBER SIX (6)
        WHEN ALL UNITS HAVE REACHED EOT.

UNIT NO. 6 *DEN 3 *PAR 0 *PATTRN   R
BN 677 *RN 25-600*RS 1566
EOT NO. 1
UNIT WILL REWIND AND BE
RESTARTED ON BLOCK ONE
WHEN ALL AVAIL UNITS REACH EOT

        EXAMPLE 7

EXAMPLE 7: IN THIS EXAMPLE UNIT NUMBER TWO (2) HAS
        ENCOUNTERED BEGINNING OF TAPE (BOT). DRIVE WILL BE DROPPED
        STATISTICS WILL BE PRINTED, TESTING RESUMED
        AT BEGINNING OF NEXT PASS.

UNIT NO. 2 *DEN 2 *PAR 0 *PATTRN 2
BN 56*RN 2-4*RS 1200
ILLEGAL BOT

        EXAMPLE 8

EXAMPLE 8: IN THIS EXAMPLE THE SELECTED UNIT (NUMBER 0)
        HAS BECOME UNAVAILABLE.UNIT WILL BE DROPPED
        STATISTICS WILL BE PRINTED,TESTING WILL RESUME AT
        BEGINNING OF NEXT PASS.

UNIT NO. 3 *DEN 1 *PAR 0 *PATTRN 4
BN 1*PN 0-200*RS 66 NOT AVAIL
(OR LOST SELECT REMOTE, NO BOT ON REWIND)

        EXAMPLE 9

EXAMPLE 9: IN THIS EXAMPLE THE WRITE OPERATION EXECUTED ON
        UNIT NUMBER SIX (6) WAS NOT COMPLETED AND NO
        INTERRUPT WAS RETURNED.

UNIT NO. 6 *DEN 2 *PAR 0 *PATTRN R
BN 12*RN 3-4*RS 100*WE
NO INTERRUPT RETURNED

EXAMPLE 10

EXAMPLE: 10   THIS EXAMPLE SHOWS A READ ERROR WHICH
         RECOVERED ON THE SECOND RETRY. THIS
         ERROR WILL BE LOGGED AS A RDERR BUT WILL BE
         CATEGORIZED AS A SOFT ERROR. THE REGISTERS
         SHOW A PARITY ERROR WAS THE CAUSE OF THE ERROR.

UNIT NO. 1 *DEN 3 *PAR 1 *PATTRN R
*BN 10 *RN 2-100 *RS 1117 *RE F***
COMD 1110100110000010
STAT 0011000001000001
WC 0
LPC 337-147
ORIGINAL ERROR

UNIT NO. 1 *DEN 3 *PAR 0 *PATTRN R
*BN 10 *RN 2-100 *RS 1117 *RE F***
COMD 1110100110000010
STAT 0011000001000001
WC 0
LPC 337-147
READ FAILED--RETRY: 1
REREAD SUCCESSFUL--RETRY: 2

EXAMPLE 11

EXAMPLE 11:   THIS EXAMPLE SHOWS A WRITE ERROR WHICH
         WAS NOT RECOVERED BY SUCCESSFULLY REWRITING
         THE RECORD FOUR TIMES AT THAT LOCATION. THE
         RECORD WAS SUCCESSFULLY WRITTEN AFTER 3
         INCHES OF TAPE WAS ERASED. THIS ERROR
         WILL BE LOGGED AS A BAD TAPE SPOT.

UNIT NO. 0 *DEN 3 *PAR 0 *PATTRN R
*BN 2 *RN 370 -461 *RS 2407 *WE
COMD 1110000010000100
STAT 0011000001000001
WC 0
CA 25613 -25613
ORIGINAL ERROR

UNIT NO. 0 *DEN 3 *PAR 0 *PATTRN R
*BN 2 *RN 370 -461 *RS 2407 *WE
COMD 1110000010000100
STAT 0011000001000001
WC 0
CA 25613 -25613
SUSPECT BAD TAPE
RETRY: 0
REPEAT: 0
RECOVERED
RETRY: 1

10.   STATISTICS PRINTOUT
        ---------- --------

        THE PROGRAM GATHERS A VARIETY OF STATISTICS DURING
        THE COURSE OF ITS TESTING. THE STATISTICS ARE KEPT
        ON A UNIT BY UNIT BASIS AND ARE SUMMARIZED IN A
        STATISTICS PRINTOUT. STATISTIC PRINTOUTS CAN BE
        PRINTED AT THE END OF EACH BLOCK CYCLE BY SETTING
        SWITCH FOUR (4) TO 1. A STATISTIC PRINTOUT IS AUTOMATICALLY
        PRINTED WHEN A UNIT REACHES EOT AND IS REWOUND.

        HERE IS AN EXPLANATION OF THE STATISTIC SUMMARY.

        DROPS: THE NUMBER OF BITS DROPPED ON A PER TRACK
                BASIS. DROPS ARE COLLECTED DURING THE DATA
                CHECK ROUTINE.

        PICKS: THE NUMBER OF BITS PICKED ON A PER TRACK
                BASIS. DROPS ARE COLLECTED DURING THE DATA
                CHECK ROUTINE.

        WTERR: THE NUMBER OF RECORDS IN WHICH A WRITE ERROR
                OCCURRED. IF WRITE RETRY WAS ENABLED, WTERR
                WILL CONTAIN ONLY THOSE RECORDS WHICH WERE
                NOT RECOVERED AFTER ONE RETRY.

         RTRY: THE NUMBER OF RETRIES INITIATED UNDER THE
                WRITE RETRY OPTION. (SEE ITEM 8., SW1:)

        RDERR: THE TOTAL NUMBER OF RECORDS IN WHICH A
                READ ERROR OCCURRED.

         SOFT: THE NUMBER OF READ ERRORS WHICH WERE
                RECOVERED WITHIN A MAXIMUM OF FOUR
                REREADS OF A RECORD UNDER THE READ RETRY
                OPTION. (SEE ITEM 8., SW1:)
                **NOTE: SOFT READ ERRORS ARE ONLY CATEGORIZED
                FOR THOSE READ ERRORS OCCURRING WHEN CONSOLE
                SWITCH 1 IS SET TO ZERO.

         HARD: THE NUMBER OF READ ERRORS WHICH REMAINED
                UNRECOVERED UNDER THE READ RETRY SCHEME.
                (SEE ITEM 8., SW1:)
                **NOTE: HARD READ ERRORS ARE ONLY CATEGORIZED
                FOR THOSE READ ERRORS OCCURRING WHEN CONSOLE
                SWITCH 1 IS SET TO ZERO.

        DTERR: THE NUMBER OF DATA ERRORS FOUND FOR THIS UNIT.
                **NOTE: DATA ERRORS ARE ONLY FOUND FOR THOSE
                RECORDS WHICH WERE READ WITH SWITCH 11 RESET TO
                ZERO.

BAD TAPE SPOTS: A COUNT OF THE NUMBER OF TAPE SPOTS
        WHERE A RECORD COULD NOT BE REWRITTEN SUCCESSFULLY
        UNDER THE WRITE RETRY OPTION (SEE ITEM8., SW1;)
        FOLLOWING THE COUNT IS A LIST OF THE BAD TAPE
        LOCATIONS IDENTIFIED BY THE BLOCK AND RECORD NUMBER
        WHEN THE BAD TAPE SPOT WAS LOGGED.

        EXAMPLE

DROPS: 0 0 0 0 7 0 0 0
PICKS: 0 0 0 2 0 0 0 0
WTERR: 3
 RTRY: 4
RDERR: 6
 SOFT: 1
 HARD: 5
DTERR: 10
1 BAD TAPE SPOTS
0 *BN 16 *RN 41

11.   AUTO SEQUENCE
        ==============

        THE AUTO SEQUENCE (START AT ADDRESS 240) WILL EXECUTE A
        PREDETERMINED TEST PLAN ON ALL AVAILABLE UNITS. THE ONLY
        OPERATOR RESPONSE REQUIRED IS TO THE TYPED REQUESTS
        FOR THE CONTROLLER ADDRESS AND VECTOR AND CONTINUOUS OR
        SINGLE CYCLE. ALL SWITCHES REMAIN ACTIVE AND MAY BE
        USED NORMALLY; HOWEVER, THE INTENT IS TO LEAVE ALL SWITCHES
        DOWN AND ALLOW FULL EXECUTION OF THE TEST PLAN FOR
        SYSTEM CHECKOUT.

        SAMPLE START AT 240(8):   AUTO SEQUENCE

        LOAD ADDRESS 240(8), SET SWITCHES TO ZERO, PRESS START:

                TM,A,B-11 AUTO SEQUENCE TEST
                ENTER RESPONSES IN OCTAL

                REGISTER START = 172520 (CR)
                VECTOR = 224 (CR)
                AUTO CONT: 0 (1)

        THIS EXAMPLE SHOWS AN AUTO SEQUENCE START WITH THE CONTROLLER
        AT BUS ADDRESS 172520 AND A VECTOR OR 224. ALL AVAILABLE
        UNITS WILL BE TESTED CONTINUOUSLY.

        AS EACH PASS IS COMPLETED A DIVIDER LINE OF ASTERISKS
        WILL BE PRINTED FOLLOWED BY AN END OF PASS MESSAGE
        INDICATING HOW MANY PASSES HAVE BEEN COMPLETED SINCE
        THE AUTO SEQUENCE WAS BEGUN. AT THE START OF EACH
        PASS THE UNITS BEING TESTED ARE PRINTED.

        AUTO SEQUENCE TEST PLAN:

        THE AUTO SEQUENCER WILL EXECUTE A PASS CONSISTING OF
        THE WRITING, READING, AND CHECKING OF SEVERAL
        DIFFERENT DATA PATTERNS. EACH PASS WILL START AT BOT
        AND PROCESS AN ENTIRE MAG TAPE BEFORE REWINDING

        THE UNITS WILL BE SET UP TO WRITE 800 BPI IN NINE
        TRACK FORMAT. ODD PARITY WILL BE USED AND NO
        TAPE MARKS WILL BE WRITTEN.

        THE DATA PATTERNS WILL BE AS FOLLOWS:

        THREE FIXED DATA PATTERNS:

        EACH PATTERN WILL BE USED FOR SIX BLOCKS.
        EACH BLOCK CONSISTS OF (100) 4000 CHARACTER RECORDS.

        PATTERN 3:   WALKING ONE BIT
        PATTERN 7:   ALTERNATING ONE AND ZERO BITS
        PATTERN 11:   INCREMENTING CHARACTERS (000-377)

RANDOM DATA:

FOLLOWING THE FIXED DATA PATTERNS, RANDOM
DATA WILL BE WRITTEN IN THE SAME BLOCK STRUCTURE
UNTIL EOT IS REACHED.
IT IS IMPORTANT THAT THE TAPE USED FOR THE TEST
BE OF SUFFICIENT LENGTH TO ACCOMODATE ALL OF
THE FIXED DATA PATTERNS AND AT LEAST ONE
RECORD OF RANDOM DATA; OTHERWISE, THE TAPE WILL
BE REWOUND UNTIL ALL OF THE DATA PATTERNS
HAVE BEEN TESTED.

12.   TESTING PROCEDURES

        AS PREVIOUSLY STATED THIS PROGRAM CONTAINS NO
        FIXED TESTS. THE ENTIRE TEST CYCLE TO BE EXECUTED
        IS DESCRIBED BY THE OPERATOR THOUGH RESPONSES TO
        TELETYPE REQUESTS FOR PARAMETERS AND CONSOLE SWITCH
        SETTINGS FOR OPERATION. THE OPERATION SELECTED WILL
        BE EXECUTED WITH THE PARAMETERS ENTERED CONTINUOUSLY
        ON EACH AVAILABLE UNIT, ONE BLOCK AT A TIME, UNTIL
        STOPPED BY THE OPERATOR. THE OPERATION MAY BE CHANGED
        DYNAMICALLY BY CHANGING THE CONSOLE SWITCHES AT ANY
        TIME. THE PROGRAM WILL ATTEMPT TO PERFORM ANY OPERATION
        SET AND THEREFORE CAUTION SHOULD BE TAKEN TO ASSURE THAT
        THE UNIT IS CAPABLE OF PERFORMING AS REQUESTED. FOR
        INSTANCE, ONE SHOULD NOT ATTEMPT TO PERFORM READ OPERATIONS
        ON A TAPE WHICH HAS NOT BEEN WRITTEN AS THE DATA, IF ANY,
        IS UNPREDICTABLE. HOWEVER, IF A TAPE HAS BEEN WRITTEN WITH
        THIS PROGRAM, IT CAN BE READ AS OFTEN AS DESIRED WITHOUT
        BEING REWRITTEN. THIS IS A GOOD PROCEDURE TO USE FOR
        TESTING TAPE COMPATABILITY. SCOPING OF TAPE UNITS BECOMES
        SIMPLE; BY SETTING THE DESIRED OPERATION AND ITS PARAMETER,
        A UNIT MAY BE CONTINUOUSLY EXERCISED IN ANY MANNER DESIRED.
        BY USING THE VARIOUS ERROR CONTROL SWITCHES AND ENTERING
        THE NEEDED STALL, ANY FUNCTION CAN BE SCOPED RATHER
        EASILY. RELIABILITY TESTING CAN BE PREFORMED BY USE
        OF THE RANDOMIZATION CAPABILITY. PERHAPS A CYCLE OF
        RANDOM TESTING MIGHT BE SET UP AND ALLOWED TO RUN
        FOR SOME PERIOD OF TIME, THE STATISTICAL COLLECTION
        OF DROPS AND PICKS IS THEN SIGNIFICANT. INTERMITTANT
        PROBLEMS CAN BE FOUND BY SETTING THE DESIRED OPERATION
        IN MOTION AND DISALLOWING ERROR PRINTOUTS WHILE ALLOWING
        A HALT ON ERROR. THE ERROR THAT CAUSED THE HALT CAN
        BE PRINTED BY RESETTING CONSOLE SWITCH TEN AND PRESSING
        CONTINUE. IF SOME PARTICULAR DATA PATTERN SHOULD BE
        CAUSING DATA ERROR, USE OF THE YOZZLE SWITCH AND ITS
        ASSOCIATED STALL CAN BE USED TO ALLOW SCOPING OF THIS
        PARTICULAR RECORD.

        AS YOU SEE, THERE ARE MYRIAD TESTING PROCEDURES WHICH
        COULD BE PERFORMED. THE PARAMETERS, TAPE OPERATIONS, ERROR
        EXAMINATION AND REPORTING ARE ALL AT YOUR DISCRETION.

        TRY IT, YOU'LL LIKE IT.

13.   LISTING

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZTME-C-D

PRODUCT NAME: TM,A,B-11/TU10,W,N DRIVE FUNCTION TIMER

DATE :   AUGUST 1976

MAINTAINER: DIAGNOSTIC ENGINEERING

AUTHOR: R. B. BARNES

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                   MAYNARD, MASS 01754

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1.   ABSTRACT

      THE DRIVE FUNCTION TIMER ASSISTS IN THE TESTING OF THE TM-11
      OR TMA,B-11 CONTROL UNIT AND TU10 OR TU10W OR TU10N TAPE UNITS.
      OPERATIONS ARE EXECUTED, TIMED, AND THE TIMES ARE THEN
      PRINTED (IN MILLISECONDS). THERE IS NO LIMIT OR ERROR
      TESTING FACILITIES IN THE PROGRAM, THE DECISION ON THE
      VALIDITY OF TIMES MEASURED MUST BE MADE BY THE OPERATOR.
      ANY CONFIGURATION OF UP TO 8 TU10,W,N TAPE UNITS (7 AND 9
      CHANNEL) MAY BE SELECTED.

2.   REQUIREMENTS

2.1   EQUIPMENT

      PDP-11;TM,A,B-11 TAPE CONTROL UNIT AND 1 TO 8 TAPE DRIVES.
      (TU10,N,W AND ANY CONFIGURATION OF 7 OR 9 CHANNEL DRIVES)
      *NOTE: TU10W TAPE UNITS WILL GO IN COMBINATION W/TMA,B-11
              CONTROL UNITS ONLY.

2.2   STORAGE

2.2.1 PROGRAM STORAGE

      THE PROGRAM REQUIRES 4K OF MEMORY.

3.   LOADING PROCEDURE

3.1   METHOD

      A. PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED
      B. PROGRAM IS LOADABLE AND CHAINABLE IN 8K OF MEMORY,
         DEFAULT IS DRIVE 0 9TRK ONLY.

4.   STARTING PROCEDURE

4.1   BEFORE STARTING PROGRAM SET LOC. 176 WITH DESIRED
          CONTROL SETTINGS. (DEFAULT=200;DRIVE 0,9 TRK)

          BITS 15-0 ARE USED TO INDICATE THE TAPE UNIT CONFIGURATION.

              15=1   HAVE UNIT 0   SELECTED,   7 TRACK
              14=1   "   1   "   "
              13=1   "   2   "   "
              12=1   "   3   "   "
              11=1   "   4   "   "
              10=1   "   5   "   "
               9=1   "   6   "   "
               8=1   "   7   "   "
               7=1   HAVE UNIT 0   SELECTED,   9 TRACK
               6=1   "   1   "   "
               5=1   "   2   "   "
               4=1   "   3   "   "
               3=1   "   4   "   "
               2=1   "   5   "   "
               1=1   "   6   "   "
               0=1   "   7   "   "

4.2   STARTING ADDRESS

          200

4.3   PROGRAM AND/OR OPERATOR ACTION

          LOAD PROGRAM INTO MEMORY.
          SET DESIRED TAPE UNITS ON-LINE.
          LOAD LOC. 176 WITH CONTROL SETTINGS (SEE 4.1)
          LOAD STARTING ADDRESS.
          PRESS START.
          THE PROGRAM WILL BEGIN TIMING FUNCTIONS.
          ON COMPLETION OF ALL TESTS "END OF TIMING" WILL BE PRINTED AND
          THE PROCESSOR WILL HALT.
          TO REPEAT TEST; IF SAME CONTROL SETTINGS ARE DESIRED SIMPLY PRESS CONTINUE.
          IF DIFFERENT SETTINGS ARE NECESSARY RELOAD LOC.176 AND LOAD ADDRESS 200-START.

5.   OPERATING PROCEDURE

5.1   OPERATIONAL SWITCH SETTINGS

          NONE

6.   ERRORS

          THE PROGRAM HAS NO INTERNAL ERROR DETECTION FACILITIES AND,
          THEREFORE, NO ACTUAL ERROR TYPEOUTS. THE VALIDITY OF THE
          TIMES MEASURED MUST BE DETERMINED BY THE OPERATOR.

6.1   TIME RELATIONSHIPS

          A. "READ SHUTDOWN" MUST BE < "WRITE SHUTDOWN".
          B. GAPS MUST = 8>7>6>5>4>3, 3=2=1 (1.5).
          C. "WRITE EOF" SHOULD BE SLIGHTLY > "WRITE XIRG".
          *NOTE:
                   1. TU10 TIMING INFO REFERENCE 6.2
                   2. TU10W (M8926) TIMING INFO REFERENCE 6.3
                   3. TU10N (M8927) TIMING INFO REFERENCE 6.4

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                                ****************
6.2      TIME LIMITS AND PRINTOUT FORMAT *** TU10 ONLY ***
                                ****************

         TIMES INDICATED UNDER "UNIT A" ARE STANDARD FOR A 9 CHANNEL UNIT
         AND "UNIT B" FOR A 7 CHANNEL UNIT.  TIMES ARE IN MILLISECONDS,
         TOLERANCES INDICATED WITHIN "()" ARE PLUS OR MINUS.

         FUNCTION                 UNIT A  (9 CHANNEL)   UNIT B  (7 CHANNEL)
         WRITE FROM BOT DELAY     180.0    (15.0)       SAME
         WRITE SHUTDOWN             7.1    ( 1.0)       10.4      ( 1.0)
         WRITE START                8.9    ( 0.4)       12.6      ( 0.5)
         SETTLE DOWN DELAY         12.0    ( 4.0)       SAME
         WRITE TO ERASE HEAD       11.0    ( 4.0)       SAME
         BACKSPACE SHUTDOWN         2.2    ( 0.3)        6.5      ( 0.5)
         READ SHUTDOWN              2.2    ( 0.3)       SAME
         GAPS SHOULD = 8>7>6>5>4>3, 3=2=1 (1.5).
         GAP 1                     13.4    SEE          20.1
         GAP 2                     13.4    NOTE         20.1
         GAP 3                     13.4    ABOVE        20.1
         GAP 4                     16.8                 26.7
         GAP 5                     20.2                 33.3
         GAP 6                     23.4                 39.9
         GAP 7                     26.5                 46.5
         GAP 8                     30.2                 53.1
         WRITE START                8.9    ( 0.4)       12.6      ( 0.5)
         WRITE XIRG                95.0    (10.0)       SAME
         READ FROM BOT DELAY       90.0    (10.0)       SAME
         WRITE EOF                114.0    (10.0)      118.0      (10.0)
         EOR TO EOF SP TIME       100.0    (10.0)       SAME
         SPACE SHUTDOWN             2.2    ( 0.3)       SAME
         ONE INCH DATA TIME        22.3    ( 1.0)       SAME
        *FUNCTIONS AT 556 BPI
         WRITE FROM BOT             .0                 185.0      (15.0)
         ONE INCH DATA TIME         .0                  22.0      ( 0.8)
         WRITE SHUTDOWN             .0                  10.4      ( 1.0)
         BACKSPACE SHUTDOWN         .0                   6.7      ( 0.5)
         READ SHUTDOWN              .0                   2.3      ( 0.3)
        *FUNCTIONS AT 200 BPI
         WRITE FROM BOT             .0                 185.0      (15.0)
         ONE INCH DATA TIME         .0                  22.0      ( 1.0)
         WRITE SHUTDOWN             .0                  10.4      ( 1.0)
         BACKSPACE SHUTDOWN         .0                   7.5      ( 0.5)
         READ SHUTDOWN              .0                   3.1      ( 0.3)
         END OF TIMING
```

* NOTE: THESE TIMES ONLY PRINTED WHEN ONE OR MORE 7 CHANNEL
         TAPE UNITS ARE SELECTED.

```
                               *******************
6.3      TIME LIMITS AND PRINTOUT FORMAT *** TU10W (M8926) ONLY ***
                               *******************

         TIMES INDICATED UNDER "UNIT A" ARE STANDARD FOR A 9 CHANNEL UNIT
         AND "UNIT B" FOR A 7 CHANNEL UNIT.  TIMES ARE IN MILLISECONDS.
         TOLERANCES INDICATED WITHIN "()" ARE PLUS OR MINUS.

         FUNCTION              UNIT A  (9 CHANNEL)   UNIT B  (7 CHANNEL)
         WRITE FROM BOT DELAY   184.6   (15.0)        200.7    (15.0)
         WRITE SHUTDOWN           6.5   ( 0.6)          6.8    ( 0.6)
         WRITE START             8.9   ( 0.8)         15.1    ( 1.3)
         SETTLE DOWN DELAY       12.0   ( 4.0)         SAME
         WRITE TO ERASE HEAD     11.0   ( 5.0)         SAME
         BACKSPACE SHUTDOWN       2.2   ( 0.2)          6.6    ( 0.6)
         READ SHUTDOWN            2.2   ( 0.2)         SAME
         GAPS SHOULD = 8>7>6>5>4>3, 3=2=1 (1.5)       (1.6)
         GAP 1                   13.2   SEE            19.1
         GAP 2                   13.2   NOTE           19.1
         GAP 3                   13.2   ABOVE          19.1
         GAP 4                   16.8                  26.7
         GAP 5                   20.2                  33.3
         GAP 6                   23.4                  39.9
         GAP 7                   26.5                  46.5
         GAP 8                   30.2                  53.1
         WRITE START             8.9   ( 0.8)         15.1    ( 1.3)
         WRITE XIRG              95.0   ( 9.0)         98.6    ( 9.0)
         READ FROM BOT DELAY    150.6   (13.0)         90.0    ( 9.0)
         WRITE EOF              114.0   (15.0)        117.2    (15.0)
         EOR TO EOF SP TIME     100.9   ( 9.0)        104.4    ( 9.0)
         SPACE SHUTDOWN           2.2   ( 0.2)         SAME
         ONE INCH DATA TIME      22.3   ( 1.0)         SAME
        *FUNCTIONS AT 556 BPI
         WRITE FROM BOT           .0                  200.7    (15.0)
         ONE INCH DATA TIME       .0                   22.3    ( 1.0)
         WRITE SHUTDOWN           .0                    7.2    ( 0.7)
         BACKSPACE SHUTDOWN       .0                    6.9    ( 0.6)
         READ SHUTDOWN            .0                    2.3    ( 0.2)
        *FUNCTIONS AT 200 BPI
         WRITE FROM BOT           .0                  200.7    (15.0)
         ONE INCH DATA TIME       .0                   22.3    ( 1.0)
         WRITE SHUTDOWN           .0                    9.4    ( 1.0)
         BACKSPACE SHUTDOWN       .0                    7.9    ( 0.7)
         READ SHUTDOWN            .0                    3.3    ( 0.3)
         END OF TIMING
```

* NOTE: THESE TIMES ONLY PRINTED WHEN ONE OR MORE 7 CHANNEL
         TAPE UNITS ARE SELECTED.

```
                              ******************
6.4      TIME LIMITS AND PRINTOUT FORMAT *** TU10N (M8927) ONLY ***
                              ******************

         TIMES INDICATED UNDER "UNIT A" ARE STANDARD FOR A 9 CHANNEL UNIT
         AND "UNIT B" FOR A 7 CHANNEL UNIT.  TIMES ARE IN MILLISECONDS.
         TOLERANCES INDICATED WITHIN "()" ARE PLUS OR MINUS.

         FUNCTION            UNIT A  (9 CHANNEL)   UNIT B  (7 CHANNEL)
         WRITE FROM BOT DELAY 180.0  (15.0)        SAME
         WRITE SHUTDOWN         7.1  ( 1.0)          7.1    ( 1.0)
         WRITE START           8.9  ( 0.4)         15.3    ( 0.5)
         SETTLE DOWN DELAY     12.0  ( 4.0)        SAME
         WRITE TO ERASE HEAD   11.0  ( 4.0)        SAME
         BACKSPACE SHUTDOWN     2.2  ( 0.3)          6.5    ( 0.5)
         READ SHUTDOWN          2.2  ( 0.3)        SAME
         GAPS SHOULD = 8>7>6>5>4>3, 3=2=1 (1.5).
         GAP 1                 13.4  SEE            20.1
         GAP 2                 13.4  NOTE           20.1
         GAP 3                 13.4  ABOVE          20.1
         GAP 4                 16.8                 26.7
         GAP 5                 20.2                 33.3
         GAP 6                 23.4                 39.9
         GAP 7                 26.5                 46.5
         GAP 8                 30.2                 53.1
         WRITE START           8.9  ( 0.4)         15.3    ( 0.5)
         WRITE XIRG           95.0  (10.0)        SAME
         READ FROM BOT DELAY  90.0  (10.0)        SAME
         WRITE EOF           114.0  (10.0)        118.0    (10.0)
         EOR TO EOF SP TIME  100.0  (10.0)        SAME
         SPACE SHUTDOWN         2.2  ( 0.3)        SAME
         ONE INCH DATA TIME    22.3  ( 1.0)        SAME
        *FUNCTIONS AT 556 BPI
         WRITE FROM BOT          .0                185.0    (15.0)
         ONE INCH DATA TIME      .0                 22.0    ( 0.8)
         WRITE SHUTDOWN          .0                  7.1    ( 1.0)
         BACKSPACE SHUTDOWN      .0                  6.7    ( 0.5)
         READ SHUTDOWN           .0                  2.3    ( 0.3)
        *FUNCTIONS AT 200 BPI
         WRITE FROM BOT          .0                185.0    (15.0)
         ONE INCH DATA TIME      .0                 22.0    ( 1.0)
         WRITE SHUTDOWN          .0                  7.1    ( 1.0)
         BACKSPACE SHUTDOWN      .0                  7.5    ( 0.5)
         READ SHUTDOWN           .0                  3.1    ( 0.3)
         END OF TIMING

   * NOTE:  THESE TIMES ONLY PRINTED WHEN ONE OR MORE 7 CHANNEL
            TAPE UNITS ARE SELECTED.
```

7.   RESTRICTIONS

7.1   STARTING RESTRICTIONS

          AT LEAST ONE TU10 TAPE UNIT MUST BE "ON-LINE" AND SELECTED
          BY SWITCHES PER 4.1. ALSO MAKE CERTAIN THAT EACH TM10
          THAT IS "ON-LINE" HAS A UNIQUE UNIT NUMBER SELECTED.

7.2   OPERATING RESTRICTIONS

          THE INSTRUCTION TEST MUST RUN WITHOUT ERRORS BEFORE ATTEMPTING
          TO OPERATE THIS PROGRAM. (DZTMA)

8.   MISCELLANEOUS

8.1   EXECUTION TIME

          NOT APPLICABLE

9.0   PROGRAM DESCRIPTION

9.1   WRITE FROM BOT DELAY

        WRITE FROM BOT DELAY IS THE TIME NECESSARY TO MOVE THE BEGINNING
        OF TAPE (BOT) MARKER APPROXIMATELY 6 INCHES PAST THE WRITE HEAD.
        THE FIRST RECORD ON TAPE MUST BE WRITTEN AT LEAST 3 INCHES AWAY
        FROM THE BOT MARKER.

        PROCEDURE TO MEASURE TIME:

        A.   IF TU10 IS NOT AT BOT IT IS REWOUND TO BOT.
        B.   INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS
             REGISTER.
        C.   ISSUE WRITE FUNCTION, 800 BPI, SET "GO".
        D.   MONITOR CURRENT MEMORY ADDRESS REGISTER TO DETERMINE WHEN
             2ND BYTE IS OUTPUT.
        E.   THE TIME FROM "GO" UNTIL 2ND BYTE IS OUTPUT IS
             APPROXIMATELY EQUAL TO "WRITE FROM BOT DELAY".

9.2   WRITE SHUTDOWN

        WRITE SHUTDOWN IS THE AMOUNT OF TIME NECESSARY TO CONTINUE
        MOVING TAPE AFTER A RECORD IS WRITTEN SO THAT THE PROPER
        INTERRECORD GAP WILL EXIST BETWEEN RECORDS.

        PROCEDURE TO MEASURE TIME:

        A.   THE PROGRAM USES THE SAME RECORD THAT WAS WRITTEN TO TIME
             "WRITE FROM BOT DELAY".
        B.   AFTER THE LAST BYTE (BC=0), INDICATING THE END OF THE
             RECORD, MONITOR "SETTLEDOWN" UNTIL IT BECOMES A 1.
        C.   THE TIME FROM "BC=0" UNTIL "SETTLEDOWN" IS "WRITE
             SHUTDOWN".

9.3   WRITE START

WRITE START IS THE TIME NECESSARY FOR TAPE TO ACCELERATE TO
FULL SPEED AND GUARANTEE A 1/2 INCH INTERRECORD GAP.

PROCEDURE TO MEASURE TIME:

SAME AS "WRITE FROM BOT" EXCEPT NOW WE ARE NOT AT BOT.
A.   INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS
     REGISTER.
B.   ISSUE WRITE FUNCTION, 800 BPI, SET "GO".
C.   MONITOR CURRENT MEMORY ADDRESS REGISTER TO DETERMINE WHEN
     2ND BYTE IS OUTPUT.
D.   THE TIME FROM "GO" UNTIL 2ND BYTE IS OUTPUT IS APPROXIMATELY
     EQUAL TO "WRITE START".

9.4   SETTLEDOWN DELAY

TAPE DOES NOT ACTUALLY COME TO A COMPLETE STOP UNTIL SOME
PERIOD OF TIME AFTER SHUTDOWN HAS ENDED. ALSO, AFTER TAPE HAS
FULLY STOPPED, AN ADDITIONAL PERIOD OF TIME IS NECESSARY FOR THE
TAPE AND HARDWARE TO "SETTLEDOWN" AND BECOME STABLE. THE
"SETTLEDOWN DELAY" IS THE PERIOD OF TIME NECESSARY FOR THE TAPE
AND MECHANICAL CHARACTERISTICS OF THE TU10 TO BECOME STABLE, SO
THAT THE UNIT CANNOT BE OPERATED, START/STOP, AT A FREQUENCY WHERE
IT IS MECHANICALLY RESONANT.

PROCEDURE TO MEASURE TIME:

A.   THE PROGRAM USES THE SAME RECORD THAT WAS WRITTEN TO TIME
     "WRITE START"
B.   AFTER "SETTLEDOWN" BECOMES A 1, INDICATING THE START OF
     SETTLEDOWN, MONITOR "TU READY" UNTIL IT BECOMES A 1.
C.   THE TIME FROM "SETTLEDOWN" UNTIL "TU READY" IS "SETTLEDOWN".

9.5   WRITE TO ERASE HEAD

THE PURPOSE OF THE ERASE HEAD IS TO INSURE THAT THE TAPE IS IN
THE SAME FLUX STATE AS THE WRITE HEADS. THIS IS NECESSARY FOR
SEVERAL REASONS.

1.   START/STOP CHARACTERISTICS VARY AMONG TAPE UNITS AND IT
     WOULD BE POSSIBLE TO LEAVE OLD DATA IN THE INTERRECORD GAPS
     WHEN USING A TAPE ON MORE THAN ONE UNIT.
2.   A TAPE PREVIOUSLY USED AT ONE RECORDING DENSITY COULD NOT BE
     USED LATER AT ANOTHER DENSITY.
3.   TRACK ALIGNMENT AND HEAD WIDTH VARY FROM TAPE UNIT TO
     TAPE UNIT AND IT WOULD BE POSSIBLE FOR DATA TO BE LEFT ON
     THE TRACK EDGES FROM OLD RECORDS.

THE "WRITE TO ERASE HEAD" TEST INSURES THAT THE TAPE IN FRONT OF
THE WRITE HEAD IS ERASED DURING A WRITE OPERATION.

PROCEDURE TO MEASURE TIME:

A.   A LONG RECORD HAS BEEN WRITTEN FROM BOT. SAME RECORD THAT
     WAS USED TO TIME "WRITE FROM BOT DELAY".
B.   TAPE IS REWOUND TO BOT.
C.   BYTE RECORD COUNTER IS INITIALIZED FOR A 3 BYTE RECORD
     AND CURRENT MEMORY ADDRESS REGISTER IS INITIALIZED.
D.   ISSUE WRITE FUNCTION, 800 BPI, SET "GO".
E.   MONITOR BYTE RECORD COUNTER UNTIL IT = 0 INDICATING THAT 2
     BYTES ARE WRITTEN IMMEDIATELY ISSUE A POWER CLEAR WHICH
     STOPS ALL DATA TRANSFERS AND CAUSES THE DRIVE TO SHUTDOWN.
F.   TAPE IS REWOUND TO BOT
G.   INITIALIZE BYTE RECORD COUNTER (3 BYTES) AND CURRENT
     MEMORY ADDRESS REGISTER.
H.   ISSUE READ FUNCTION, 800 BPI, SET GO
I.   MONITOR BYTE RECORD COUNTER UNTIL IT = -1 AND THEN TIME
     UNIT IT = 0. THIS TIME WILL INDICATE THE DISTANCE BETWEEN THE
     2ND BYTE AND THE 3RD BYTE WHICH IS ALSO THE AMOUNT OF TAPE
     THAT WAS ERASED BY THE ERASE HEAD DURING THE WRITE OPERATION
     OR "WRITE TO ERASE HEAD".

9.6   BACKSPACE SHUTDOWN

"BACKSPACE SHUTDOWN" IS THE LENGTH OF TIME NECESSARY TO GUARANTEE
THAT IF A WRITE OPERATION FOLLOWS A BACKSPACE THE TAPE WILL BE
POSITIONED SUCH THAT ALL PREVIOUS DATA IS IN FRONT OF THE WRITE
AND ERASE HEADS AND WILL BE ERASED. "BACKSPACE SHUTDOWN" MUST
BE LESS THAN "WRITE START" SO THAT INTERRECORD GAPS WILL INCREASE
IF A BACKSPACE/REWRITE OPERATION IS INITIATED.

PROCEDURE TO MEASURE TIME:

A.   INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS
     REGISTER.
B.   ISSUE WRITE EOF FUNCTION, 800 BPI, SET "GO"
C.   AFTER EOF RECORD IS WRITTEN WAIT FOR "TU READY".
D.   SET BYTE RECORD COUNTER TO BACKSPACE 1 RECORD.
E.   ISSUE BACKSPACE FUNCTION, SET "GO".
F.   AFTER "EOF" BECOMES A 1, INDICATING THE RECOGNITION OF
     THE "EOF" RECORD, MONITOR "SETTLEDOWN" UNTIL IT BECOMES A 1.
G.   THE TIME FROM "EOF" UNTIL "SETTLEDOWN" IS "BACKSPACE
     SHUTDOWN".

9.7   READ SHUTDOWN

READ SHUTDOWN IS THE AMOUNT OF TIME NECESSARY TO CONTINUE MOVING
TAPE AFTER A RECORD IS READ SO THAT THERE IS ENOUGH GAP FOR TAPE
TO BE FULLY ACCELERATED IF A READ IS FOLLOWED BY A BACKSPACE.
"READ SHUTDOWN" MUST ALSO BE LESS THAN "WRITE SHUTDOWN" TO
GUARANTEE THAT THE WRITE AND ERASE HEADS WILL BE POSITIONED
SUCH THAT ALL PREVIOUS DATA IS IN FRONT OF THE HEADS AND
WILL BE ERASED IF A WRITE FOLLOWS A READ. IN ADDITION, WHEN A
WRITE FOLLOWS A READ THE INTERRECORD GAP MUST STILL BE AT LEAST
1/2 OF AN INCH.

PROCEDURE TO MEASURE TIME:

A.   RECORD PREVIOUSLY USED IN "BACKSPACE SHUTDOWN" IS READ.
B.   INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS
     REGISTER
C.   ISSUE READ FUNCTION, 800 BPI, SET "GO".
D.   AFTER "EOF" BECOMES A 1, INDICATING THE END OF THE
     RECORD, MONITOR "SETTLEDOWN" UNTIL IT BECOMES A 1.
E.   THE TIME FROM "EOF" UNTIL "SETTLEDOWN" IS "READ
     SHUTDOWN"

9.8   GAP CONSISTENCY

FOR PROPER OPERATION, THE INTERRECORD GAPS ON TAPE MUST ALWAYS
BE AT LEAST 1/2 OF AN INCH. THIS WILL ALLOW DATA WRITTEN USING
ONE TAPE UNIT TO BE READ ON ANOTHER TAPE UNIT WHEN THE START/STOP
CHARACTERISTICS OF EACH UNIT ARE DIFFERENT. THE MINIMUM
GAP SIZE OF 1/2 INCH IS GENERATED WHEN A WRITE FOLLOWS A READ.
ALL OTHER GAPS SHOULD BE LARGER DEPENDING ON HOW THEY WERE
WRITTEN.

PROCEDURE TO MEASURE TIME:

A.   A TOTAL OF NINE RECORDS ARE WRITTEN ON TAPE (FROM BOT)
     UTILIZING DIFFERENT SEQUENCES TO GENERATE THE INTERRECORD GAPS.
B.   THE TAPE IS REWOUND TO BOT.
C.   INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS
     REGISTER.
D.   ISSUE READ FUNCTION, 800 BPI, SET "GO".
E.   WAIT FOR "CU READY" TO BECOME A 1, THEN REPEAT STEP C AND
     RESET "GO" TO CONTINUE.
F.   MONITOR CURRENT MEMORY ADDRESS TO DETERMINE WHEN 2ND BYTE IS
     INPUT.
G.   THE TIME FROM WHEN "GO" IS RESET UNTIL THE 2ND BYTE IS INPUT
     WILL REFLECT THE SIZE OF THE GAP.
H.   STEPS E, F ARE REPEATED UNTIL ALL 8 GAPS ARE MEASURED.

PROGRAM SEQUENCE FOR EACH GAP:

GAP 1   WRITE FOLLOWED BY A WRITE (START/STOP).

GAP 2   WRITE FOLLOWED BY A WRITE (START/STOP).

GAP 3   READ FOLLOWED BY A WRITE (START/STOP).

GAP 4   WRITE-BACKSPACE FOLLOWED BY A WRITE (START/STOP).

GAP 5   SAME AS GAP 4 EXCEPT WRITE-BACKSPACE REPEATED 2
               TIMES.

GAP 6   SAME AS GAP 4 EXCEPT WRITE-BACKSPACE REPEATED 3
               TIMES.

GAP 7   SAME AS GAP 4 EXCEPT WRITE-BACKSPACE REPEATED 4
               TIMES.

GAP 8   SAME AS GAP 4 EXCEPT WRITE-BACKSPACE REPEATED 5
               TIMES.

GAP LENGTHS SHOULD REFLECT THE FOLLOWING RELATIONSHIP:

     8>7>6>5>4>3, 3≡2≡1 (1.5).

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9.9   WRITE START

THIS IS A REPEAT OF THE "WRITE START" TEST PREVIOUSLY COMPLETED
(REFERENCE 9.3). IT'S PURPOSE IS TO DETERMINE IF TAPE WILL
DRIFT BACKWARDS TO BOT IF A "POWER CLEAR" IS ISSUED AS SOON
AS BOT DISAPPEARS WHEN MOVING FORWARD FROM BOT. TIME SHOULD
EQUAL "WRITE START" AS MEASURED IN 9.3.

9.10   WRITE XIRG

WRITE WITH AN EXTENDED INTERRECORD GAP IS A FUNCTION THAT CAUSES
THE GENERATION OF AN INTERRECORD GAP THAT IS AT LEAST 3 INCH LONG
AS COMPARED WITH THE NORMAL 3/5 INCH GAP. THE PURPOSE IS TO
ELIMINATE WRITE ERRORS THAT MAY BE CAUSED BY A DEFECTIVE AREA
ON TAPE. NORMALLY ONE REWRITE WITH XIRG WOULD BE SUFFICIENT TO
MOVE PAST THE BAD SPOT, HOWEVER IF IT ISN'T, THE PROCEDURE
WOULD BE TO REPEAT THE "BACKSPACE-REWRITE WITH XIRG" SEQUENCE UNTIL
A RECORD IS WRITTEN WITHOUT ERRORS. EACH SUCCESSIVE REWRITE WOULD
ADD 3 INCHES TO THE INTERRECORD GAP UNTIL "GOOD" TAPE WAS REACHED.

PROCEDURE TO MEASURE TIME:

A. TAPE IS NOT AT BOT
B. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS
    REGISTER.
C. ISSUE WRITE WITH XIRG FUNCTION, 800 BPI, SET "GO".
D. MONITOR CURRENT MEMORY ADDRESS REGISTER TO DETERMINE WHEN
    2ND BYTE IS OUTPUT.
E. THE TIME FROM "GO" UNIT 2ND BYTE IS OUTPUT IS "WRITE WITH
    XIRG".

9.11   READ FROM BOT

THE FIRST RECORD WRITTEN ON TAPE IS SUPPOSED TO BE AT LEAST 6
INCHES FROM THE BOT MARKER. IN THE EVENT THAT THIS CONDITION
WASN'T MET IT IS STILL DESIREABLE TO READ THE RECORD. READ FROM
BOT IS THE TIME FROM WHEN A READ FUNCTION IS ISSUED UNTIL THE
2ND BYTE IS INPUT.

PROCEDURE TO MEASURE TIME:

A. THE RECORD THAT WAS WRITTEN JUST OFF BOT DURING "WRITE
    START" (REFERENCE 9.10) IS USED.
B. TAPE IS REWOUND TO BOT
C. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS
    REGISTER.
D. ISSUE READ FUNCTION, 800 BPI, SET "GO".
E. MONITOR CURRENT MEMORY ADDRESS REGISTER TO DETERMINE WHEN
    2ND BYTE IS INPUT.
F. THE TIME FROM "GO" UNTIL 2ND BYTE IS INPUT IS "READ FROM
    BOT".

9.12   WRITE EOF.

TO WRITE AN END OF FILE MARK IT IS NECESSARY FOR TAPE TO
MOVE 3 INCHES BEFORE WRITING. IN THAT RESPECT IT IS SIMILAR
TO WRITING A RECORD WITH EXTENDED INTERRECORD GAP, HOWEVER, AN
EOF MARK CORRESPONDS TO A 1 BYTE RECORD. THE TIME SHOULD BE
SLIGHTLY LARGER THAN "WRITE XIRG".

PROCEDURE TO MEASURE TIME:

A.   TAPE UNIT IS REWOUND TO BOT.
B.   INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER.
C.   ISSUE WRITE FUNCTION, 800 BPI, SET "GO".
D.   WAIT FOR "CU READY" AND THEN "TU READY" TO BECOME A 1.
E.   ISSUE WRITE EOF FUNCTION, 800 BPI, SET "GO".
F.   WAIT FOR "TU READY" TO BECOME A 1.
G.   THE TIME FROM "GO" UNTIL "TU READY" IS "WRITE EOF".

9.13   EOR TO EOF SPACE TIME

EOR TO EOF SPACE TIME IS THE TIME NEEDED TO MOVE TAPE FROM THE
END OF A RECORD TO AN END OF FILE MARK WRITTEN AFTER IT. THE
PROCEDURE USED TURNS OUT TO BE A TEST OF THE WRITE AND ERASE HEAD
POLARITIES. IF THE TIME PRINTED IS EQUAL TO ZERO IT IS AN INDICA-
TION THAT THE EOF WAS NOT FOUND WHEN "TU READY" BECAME A 1.

THIS COULD INDICATE ONE OR MORE OF THE FOLLOWING PROBLEMS:

1.   ERASE HEAD POLARITY REVERSED.
2.   ERASE HEAD TURRENT NOT SUFFICIENT TO FULLY SATURATE TAPE.
3.   ONE OR MORE OF WRITE HEAD TRACKS POLARITY REVERSED.
4.   ONE OR MORE SENSITIVE READ AMPLIFIERS.
5.   WRITE EOF FUNCTION DIDN'T REALLY WRITE AN EOF MARK.
     OTHERWISE "EOR TO EOF SPACE TIME" SHOULD BE SLIGHTLY LARGER
     THAN "WRITE EOF".

PROCEDURE TO MEASURE TIME:

A.   A RECORD AND EOF WAS PREVIOUSLY WRITTEN FROM BOT FOR "WRITE
     EOF" (REFERENCE 9.14).
B.   TAPE IS REWOUND TO BOT.
C.   REWRITE RECORD OVER PREVIOUSLY WRITTEN RECORD.
D.   BACKSPACE OVER RECORD JUST WRITTEN.
E.   SET BYTE RECORD COUNTER TO SPACE 2 RECORDS.
F.   ISSUE SPACE FORWARD FUNCTION, SET "GO".
G.   WAIT FOR BYTE RECORD COUNTER TO INDICATE THAT 1ST RECORD
     HAS BEEN SPACED OVER THEN MONITOR "TU READY" UNTIL IT BECOMES
     A 1. AFTER "TU READY" CHECK TO SEE IF "EOF" IS A 1
     IN STATUS REGISTER. IF "EOF" NOT SET THEN ZERO TIME COUNTER.
H.   TIME FROM BYTE RECORD COUNTER =1 UNTIL "TU READY" IS "EOR
     TO EOF SPACE TIME".

9.14   SPACE SHUTDOWN

        SPACE SHUTDOWN IS THE AMOUNT OF TIME NECESSARY TO
        CONTINUE MOVING TAPE AFTER A RECORD IS SPACED OVER IN THE
        FORWARD DIRECTION FOR THE SAME REASONS AS "READ SHUTDOWN"

        PROCEDURE TO MEASURE TIME:

        A.   SPACE FORWARD FUNCTION USED TO TIME "EOR TO EOF SPACE TIME"
              IS USED.
        B.   AFTER "EOF" BECOMES A 1, INDICATING THE END OF THE
              RECORD (EOF), MONITOR "SETTLEDOWN" UNTIL IT BECOMES A 1.
        C.   THE TIME FROM "EOF" UNTIL "SETTLEDOWN" IS "SPACE
              SHUTDOWN".

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9.15   ONE INCH DATA TIME

        ONE INCH OF DATA, 800 BYTES (ALSO 556 AND 200 IF 7 CHANNEL
        UNIT), IS WRITTEN AND TIMED TO DETERMING IF TAPE IS MOVING AT
        PROPER SPEED.

        PROCEDURE TO MEASURE TIME:

        A.   INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS.

        B.   ISSUE WRITE FUNCTION, 800 BPI (OR 556, OR 200), SET "GO".

        C.   WAIT FOR CURRENT MEMORY ADDRESS REGISTER TO INDICATE 2ND
             BYTE IS OUTPUT AND THEN MONITOR BYTE RECORD COUNTER UNTIL
             EQUAL TO ZERO.

        D.   TIME FROM 2ND BYTE OUTPUT UNTIL BYTE RECORD COUNTER = 0
             IS "ONE INCH DATA TIME"

9.16   FUNCTIONS AT 556 BPI

        ALL OF THE PREVIOUS TESTS USED THE DENSTIY OF 800 BPI. IF A 7
        CHANNEL DRIVE IS SELECTED IT IS USEFUL TO RUN SEVERAL OF THE TESTS
        AGAIN USING DENSITY OF 556 BPI. REFERENCE THE PROPER PARAGRAPHS
        FOR A DESCRIPTION OF EACH TEST.

9.17   FUNCTIONS AT 200 BPI

        SAME AS ABOVE. REFERENCE 9.17, "FUNCTIONS AT 556 BPI"

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10.   STATUS AND COMMAND REGISTER BIT ASSIGNMENTS

                         COMMAND REGISTER

15   ERROR

14   DEN 8   00 = 200 BPI 7 TRACK   10 = 800 BPI 7 TRACK
13   DEN 5   01 = 556 BPI 7 TRACK   11 = 800 BPI 9 TRACK
12   POWER CLEAR

11   PARITY   0 = ODD   1 = EVEN
10   UNIT SEL. BIT 2
9   UNIT SEL. BIT 1

8   UNIT SEL. BIT 0
7   CONTROL UNIT READY
6   INTERRUPT ENABLE

5   ADDRESS BIT 17
4   ADDRESS BIT 16
3   FUNCTION BIT 2 000 = OFF LINE   100 = SPACE FORWARD
                         001 = READ   101 = SPACE REVERSE
2   FUNCTION BIT 1 010 = WRITE   110 = WRITE XIRG
1   FUNCTION BIT 0 011 = WRITE EOF   111 = REWIND
0   GO

                         STATUS REGISTER

15   ILLEGAL COMMAND (ILC)

14   END OF FILE (EOF)
13   CYCLICAL REDUNDANCY ERROR (CRE)
12   PARITY ERROR (PAE)

11   BUS GRANT LATE (BGL)
10   END OF TAPE (EOT)
9   RECORD LENGTH ERROR (RLE)

8   BAD TAPE ERROR (BTE)
7   NON EXISTENT MEMORY (NXM)
6   SELECT REMOTE (SELR)

5   BEGINNING OF TAPE (BOT)
4   7 CHANNEL (7CH)
3   SETTLE DOWN (SDWN)

2   WRITE LOCK (WRL)
1   REWIND STATUS (RWS)
0   TAPE UNIT READY (TUR)
         .ENDR

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZTMF-D-D

PRODUCT NAME: TMA,B-11/TU10,N,W SUPPLEMENTAL INST, TEST

PROGRAM DATE: AUGUST 1976

MAINTAINER: DIAGNOSTIC ENGINEERING

AUTHOR: R. B. BARNES

REVISED BY: RON PLATUKIS/R. SOLER

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1.   ABSTRACT

      THIS PROGRAM IS INTENDED TO BE USED IN ADDITION TO
      THE TMA,B-11 INSTRUCTION TEST (MAINDEC-11-DZTMA)
      TO COMPLETE TESTING OF THE MAG TAPE CONTROLLER.
      THE PROGRAM CONSISTS OF ONLY FOUR (4) TESTS WHICH
      CHECK ONLY THE TMA,B-11 FEATURES OF DATA TRANSFER AT ODD
      BYTE STARTING ADDRESS AND OPERATION INCOMPLETE TIME OUT.

2.   REQUIREMENTS

      A. ANY PDP-11 PROCESSOR
      B. 4K OF CORE
      C. CONSOLE TTY
      D. TMA-11 OR TMB-11 TAPE CONTROLLER (ONLY)
      E. 1-8 TAPE TRANSPORTS (TU10,N,W)

3.   LOADING PROCEDURE

      A. USE STANDARD PROCEDURE FOR LOADING BINARY PAPER TAPE
      B. THIS PROGRAM IS LOADABLE AND CHAINABLE PER XXDP, ACT11,
      AND SLIDE, IN 8K OF MEMORY. (SEE 7.1)

4.   STARTING PROCEDURE

      THERE ARE TWO (2) STARTING ADDRESSES THAT MAY BE USED;
      200(8) AND 210(8).

      A. 200(8):   STARTING AT THIS ADDRESS WILL CAUSE A PROGRAM
                      IDENTIFICATION HEADER TO BE PRINTED AND ALSO A
                      REQUEST FOR ENTRY OF THE UNIT NUMBER (TAPE TRANSPORT SELECT).
                      THE DEFAULT SELECTION OF UNIT ZERO (0) IS DISPLAYED, AND
                      MAY BE CHANGED TO ANY NUMBER (0-7) OR UNCHANGED BY
                      TYPING THE DESIRED NUMBER OR A CARRIAGE RETURN.
                      IF THE SELECTED UNIT IS NOT AVAILABLE, A MESSAGE WILL
                      BE PRINTED SO STATING, AND THE UNIT SELECT REQUEST REPEATED.

      B. 210(8):   STARTING AT THIS ADDRESS WILL NOT PRINT THE HEADER OR THE
                      UNIT SELECT REQUEST AND IS INTENDED AS A RESTART ADDRESS ONLY.

5.   CONSOLE SWITCH SETTING
          ===========================

          ALL SWITCHES EXCEPT 3-9 ARE USED AND THE NORMAL, OR DEFAULT, RUN
          IS DONE WITH ALL SWITCHES SET TO ZERO (0).
          ALL SWITCHES ARE DYNAMIC AND MAY BE CHANGED AT ANY TIME.

          SW15:   1=HALT ON ERROR
                   0=CONTINUE
          SW14:   1=LOOP ON ERROR (SCOPE)
                   0=CONTINUE
          SW13:   1=INHIBIT ERROR TYPE OUT
                   0=PRINT ALL ERRORS
          SW12:   1=INHIBIT ITERATION**(FIRST PASS IS SINGLE ITERATION)**
                   0=ITERATE EACH TEST ITS ASSIGNED AMOUNT
          SW11:   1=CONTINUOUS CYCLE
                   0=HALT AT END OF PASS
          SW10:   1=HALT AT END OF CURRENT TEST
                   0=CONTINUE
          SW9-3:   NOT USED
          SW2-0:   SELECT INDIVIDUAL TEST (1-4)** 00 = DO ALL TESTS

5.1   THIS PROGRAM HAS BEEN MODIFIED TO RUN ON A PROCESSOR WITH OR WITHOUT
          A HARDWARE SWITCH REGISTER. WHEN FIRST EXECUTED THE PROGRAM TESTS
          THE EXISTENCE OF A HARDWARE SWITCH REGISTER. IF NOT FOUND A
          SOFTWARE SWITCH REGISTER LOCATION (SWREG=LOC. 176) IS DEFAULTED TO.
          IF THIS IS THE CASE, UPON EXECUTION THE CONTENTS OF THE SWREG ARE
          DUMPED IN OCTAL ON THE CONSOLE TTY AND ANY CHANGES ARE REQUESTED

                        (IE)   SWR=XXXXXX   NEW=

          POSSIBLE RESPONSES ARE:

          1.   <CR>   IF NO CHANGES ARE TO BE MADE
          2.   6 DIGITS 0-7   TO REPRESENT IN OCTAL THE NEW SWITCH REGISTER
                                  VALUE ,LAST DIGIT FOLLOWED BY <CR>.
          3.   -U   TO ALLOW REENTERING VALUE IF ERROR IS COMMITTED
                                  KEYING IN SWREG VALUE.
          4.   <LF>   ONLY VALID FOR ACT-11 SYSTEMS-DO NOT USE

          BUILT INTO THE PROGRAM IS THE ABILITY TO DYNAMICALLY CHANGE THE
          CONTENTS OF SWREG DURING PROGRAM EXECUTION, BY STRIKING -G
          (CNTL G) ON CONSOLE TTY THE OPERATOR SETS A REQUEST FLAG TO CHANGE
          THE CONTENTS OF SWREG, WHICH IS PROCESSED IN KEY AREAS OF THE PROGRAM
          CODE (IE) ERROR ROUTINES, AFTER HALTS END OF PASS, AND OTHER
          APPLICABLE AREAS.

6.   ERROR PRINTOUTS

        THERE ARE THREE (3) TYPES OF ERROR PRINTOUTS WHICH MAY
        APPEAR: STATUS ERROR, DATA ERROR, POSITION ERROR.

        A. STATUS ERROR: ANY READ, WRITE, OR SPACE OPERATION WHICH
                                RESULTS IN SOME BAD STATUS (BIT 15 OF MTC),
                                OR UNEXPECTED BUS ADDRESS, OR INCORRECT
                                BYTE COUNT, WILL BE PRINTED.

        B. DATA ERROR: ANY READ OPERATION WHICH RESULTS IN UNEXPECTED
                                DATA WILL BE PRINTED.

        C. POSITION ERROR: ANY SPACE OR REWIND OPERATION RESULTING IN
                                UNEXPECTED STATUS WILL BE PRINTED.

        EXAMPLES***

        1. THE FOLLOWING EXAMPLE SHOWS A TYPICAL STATUS ERROR.

        TEST1: WRITE FROM ODD BYTE
        WRITE ERROR   THIS PRINT SHOWS THAT WHILE EXECUTING
        MTS: 10101   TEST 1 ON UNIT 2 AT 800 BPI, A WRITE
        MTC: 161204   PARITY ERROR OCCURED. THE BYTE COUNT
        MTBC: 0   IS ZERO AS IT SHOULD BE AND THE CURRENT
        MTCA: 6003 6003   ADDRESS IS AS EXPECTED.

        2. THE FOLLOWING EXAMPLE SHOWS A TYPICAL DATA ERROR.

        TEST 2: READ TO ODD BYTE
        DATA ERROR   THIS PRINT SHOWS THAT A SINGLE BIT WAS
        CN: 0   PICKED UP IN BOTH CHARACTER NUMBER ZERO
        G: 00000000   (0) AND CHARACTER NUMBER THREE (3).
        B: 01000000
        CN: 3
        G: 00000011
        B: 01000011

        3. THE FOLLOWING EXAMPLE SHOWS AN ERROR DURING A REWIND OPERATION.

        TEST4: OPI TOO LONG
        REWIND ERROR: NO BOT

7.   OPERATION

        THE PROCEDURES FOR OPERATING THIS PROGRAM ARE QUITE
        SIMPLE AND REQUIRE ONLY A FEW STEPS:

                1. LOAD ADDRESS 200 OR 210
                2. SET SWICHES FOR DESIRED TEST SEQUENCE
                3. PRESS START

        ALL CONSOLE SWITCHES ARE DYNAMIC AND MAY BE CHANGED
        AT ANY TIME. THE NORMAL OPERATING SEQUENCE IS ALL SWITCHES
        DOWN (Ø). THE PROGRAM WILL TAKE APPROXIMATELY 1.25 MINUTES
        TO RUN; HOWEVER, IF ITERATIONS ARE INHIBITED (SW11=1), THE
        PROGRAM WILL RUN IN ABOUT .75 MINUTES. THE END OF PASS
        IS NOTED BY A PRINTOUT STATING END OF PASS AND THE NUMBER OF
        THAT PASS.

        SINGLE TEST SELECTION: (SWØ-SW3)

        WHEN SWØ-3 ARE SET TO ZERO (Ø), THE SCHEDULAR WILL
        EXECUTE ALL TESTS (1-4) IN SEQUENCE AS A SINGLE PASS.
        IF SWØ-3 ARE SET TO SOME NUMBER BETWEEN 1 AND 4,
        THEN THAT PARTICULAR TEST WILL BE EXECUTED CONTINUOUSLY.
        THE PROGRAM MAY BE STOPPED AT THE END OF THE CURRENT
        TEST (EITHER IN SEQUENCE OR SINGLE TEST MODE) BY SETTING
        SWITCH TEN (SW10) TO A ONE (1). YOU MAY SELECT TEST
        NUMBERS IN ANY ORDER (UP OR DOWN) BECAUSE EACH TEST
        IS SELF CONTAINED.
7.1   CHAIN MODE RUNS A SINGLE PASS ON DRIVE Ø WITH 7 OR 9 TRACK
        AT THE STANDARD UNIBUS ADDRESS.

8.   TEST DESCRIPTION
        ••••••••••••••••

        TEST1: WRITE FROM ODD BYTE

                THE PURPOSE OF THIS TEST IS TO ASSURE THAT DATA MAY BE
                TRANSFERRED FROM MEMORY TO TAPE STARTING FROM AN ODD
                BYTE ADDRESS. THE TEST WILL WRITE A SIX (6) BYTE RECORD
                FROM AN ODD ADDRESS (WDATA+1) AND READ THAT RECORD
                BACK INTO AN EVEN ADDRESS (RDATA). NO STATUS ERROR SHOULD
                OCCUR, AND THE READ DATA SHOULD BE POSITIONED PROPERLY.
                THE RECORD IS SIX BYES LONG, EACH BYTE IS ITS NUMBER (0,1,2,3,4,5)

        TEST2: READ TO ODD BYTE

                THE PURPOSE OF THIS TEST IS TO ASSURE THAT DATA MAY BE
                TRANSFERRED FROM TAPE TO MEMORY STARTING AT AN ODD BYTE
                ADDRESS. THE PROCEDURE IS THE SAME AS IN TEST ONE (1),
                EXCEPT THAT THE WRITE IS FROM AN EVEN ADDRESS (WDATA)
                AND THE READ IS TO AN ODD ADDRESS (RDATA+1).

        TEST3: OPI TOO LONG   (OPI = BIT 8 OF MTS)

                THE PURPOSE OF THIS TEST IS TO ASSURE THAT THE OPI TIMER
                WILL SHUTDOWN THE DRIVE BEFORE THIRTY FIVE FEET OF BLANK
                TAPE IS PASSED. THE PROCEDURE IS TO PERFORM A WRITE WITH
                IRG, BACKSPACE, WRITE WITH IRG 105(10) TIMES IN ORDER
                TO ERASE 35 FEET OF TAPE. AFTER REWIND, ISSUE A READ
                COMMAND AND OPI SHOULD TIME OUT BEFORE THE FIRST RECORD
                (35 FEET DOWN TAPE) IS FOUND. THE NOMINAL VALUE FOR OPI
                IS SEVEN SECONDS (7SEC) OR ABOUT TWENTY-SIX FEET (26 FT)
                OF TAPE. THIRTY-FIVE FEET OF TAPE REFLECTS THE MAXIMUM
                TOLERANCE FOR OPI.

        TEST4: OPI TOO SHORT   (OPI = BIT 8 OF MTS)

                THE PURPOSE OF THIS TEST IS TO ASSURE THAT THE OPI TIMER
                WILL NOT SHUTDOWN THE DRIVE BEFORE SIXTEEN FEET (16 FT)
                OF BLANK TAPE IS PASSED. THE PROCEDURE IS THE SAME
                AS IN TEST THREE (3), HOWEVER OPI IS NOT EXPECTED BEFORE
                THE FIRST RECORD IS FOUND (16 FEET DOWN TAPE). THE
                SIXTEEN FEET OF TAPE RELECTS THE MINIMUM TOLERANCE FOR OPI.

9.   LISTING
        •••••••

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZTMG-C-D

PRODUCT NAME: TM,A,B-11 UTILITY DRIVER

PROGRAM DATE: AUGUST 1976

MAINTAINER: DIAGNOSTIC ENGINEERING

AUTHOR: G. B. JOHNSON

REVISED BY: RON PLATUKIS/R. SOLER

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1.   ABSTRACT

        THIS PROGRAM IS INTENDED AS A BRUTE FORCE ROUTINE
        TO EXECUTE AN OPERATION OR SERIES OF OPERATIONS, CONTINUOUSLY
        REGARDLESS OF THE RESULTS OF THE OPERATION.
        THIS UTILITY DRIVER WILL ALLOW AN OPERATOR
        TO EXECUTE ANYTHING DESIRED IN ANY ORDER. THERE ARE
        NO ERROR CHECKS OR PRINTOUTS MADE, AND ANY VARIATION
        FROM PRESET SEQUENCES AND VALUES ARE MADE BY
        CHANGING THE APPROPIATE MEMORY LOCATIONS.
        THIS PROGRAM IS NOT ELIGABLE FOR CHAIN MODE.

2.   REQUIREMENTS

2.1   HARDWARE:

        A.   ANY PDP-11 PROCESSOR
        B.   TM,A,B-11 TAPE CONTROLLER
        C.   AT LEAST ONE TU10,N,W MAG TAPE DRIVE

2.2   STORAGE:

        THIS PROGRAM REQUIRES AT LEAST 1K OF CORE

3.   LOADING PROCEDURE:

        USE STANDARD BINARY LOADING PROCEDURE

4.   STARTING PROCEDURE

        THE PROGRAM IS ALWAYS STARTED AT LOCATION 200 (8)

5.   CONTROL SWITCH SETTINGS (LOC. 176)

        BIT 0: 1=STOP AFTER EACH OPERATION
                0=PROCEED
        BIT 1: 1=STOP AT THE END OF THE OPERATION SEQUENCE
                0=PROCEED

6.   OPERATION

          THE PROGRAM OPERATION IS QUITE SIMPLE, BUT DOES
          REQUIRE THE OPERATOR TO HAVE KNOWLEDGE OF THE
          MAG TAPE SYSTEM AS OPERATED ON THE TMA-11 OR TM-11
          CONTROLLER. THE OPERATOR MUST BE ABLE TO DECIDE
          WHICH SEQUENCE OF OPERATION IS REQUIRED, AND
          WHAT VALUES TO ASSIGN TO THE VARIOUS PARAMETERS
          REQUIRED TO EXECUTE THEM. THE OPERATION SEQUENCE
          IS SET UP BY LOADING A TABLE WITH THE FUNCTION
          CODES OF THE DESIRED OPERATIONS AND SETTING THE
          NUMBER OF OPERATIONS IN A COUNTER. THE PROGRAM IS
          SET UP TO DO A WRITE OF TWENTY (20) FRAMES OF ALL
          ONES DATA TO TAPE UNIT ZERO (0) WITH
          A DENSITY OF 800 BPI IN A NINE TRACK DRIVE.
          THE DATA ADDRESS IS 3000 (8). THE OPERATION SEQUENCE
          IS SET TO DO A SINGLE WRITE. IF LOADED AND STARTED
          AT 200(8) WITH NO CHANGES MADE AND LOC. 176
          SET TO A ZERO (0), THIS OPERATION WILL BE EXECUTED
          CONTINUOUSLY.
          THE FOLLOWING IS THE LIST OF PARAMETERS WHICH MAY
          BE VARIED AND A DESCRIPTION OF EACH ALONG WITH THEIR
          CORE LOACATION:

PARAMETER	LOCATION	DESCRIPTION
CONTROL SETTINGS	176	PRESET FOR CONTINUOUS OPERATION
TM,A,B-11 ADDRESS	600	ADDRESS OF TM,A,B-11 (THE FIRST REGISTER ADDRESS: MTS)
UNIT DESCRIPTION	700	SET SELECTED SLAVE NUMBER (0-7) IN BITS 8,9,10 SELECT PARITY IN BIT 11 (0=ODD 1=EVEN) SELECT DENSITY IN BITS 13,14
BYTE COUNT	702	SET NUMBER OF BYTES PER RECORD IN TWOS' COMPLEMENT
READ ADDRESS	704	SET DESIRED ADDRESS FOR START OF READ BUFFER.
WRITE ADDRESS	706	SET DESIRED ADDRESS FOR START OF WRITE BUFFER.
SPACE COUNT	710	SET NUMBER OF RECORDS TO SPACE ON SPACE COMMAND IN TWO'S COMPLEMENT. NOTE: WHEN SPACING MULTIPLE RECORDS INSURE THAT SUFFICIENT TIME IS ALLOWED BY SETTING THE READY MULTIPLIER TO THE NUMBER OF RECORDS SPACED.

READY DELAY	712	THIS DELAY VALUE IS USED BY THE PROGRAM TO ESTABLISH A MAXIMUM TIME TO AWAIT THE COMPLETION OF AN OPERATION BEFORE PROCEEDING TO THE NEXT
READY MULTIPLIER	714	IF THE VALUE SET INTO 712 DOES NOT ALLOW ENOUGH TIME, INCREASE THE SIZE OF THE MULTIPLIER. EACH INCREMENT OF THE MULTIPLIER WILL CAUSE THE 712 DELAY TO BE EXECUTED THAT MANY MORE TIMES.
OPERATION DELAY	716	THIS DELAY IS USED TO ALLOW FOR SOME AMOUNT OF TIME BETWEEN THE EXECUTION OF EACH OPERATION. IT IS LOADED AND USED JUST AS IN THE READY DELAY(712)
OPER MULTIPLIER	720	THIS IS USED JUST AS THE READY DELAY MULTIPLIER(714)
OPERATION NUMBER	722	THIS IS THE NUMBER OF OPERATIONS TO BE PERFORMED IN A SEQUENCE AND SHOULD REFLECT THE NUMBERS OF OPERATIONS SET INTO THE OPERATION TABLE.
OPERATION TABLE	724-754	THIS TABLE (CONSISTING OF 15 LOCATIONS) IS TO BE LOADED WITH THE FUNCTION CODES FOR EACH OPERATION TO BE PERFORMED IN SEQUENCE. THE NUMBER OF ENTIRES MAY BE FROM ONE (1) TO FIFTEEN (15). MAKE SURE THAT THE NUMBER OF FUNCTION CODES SET IN THE TABLE IS REFLECTED BY THE NUMBER IN LOCATION 722 (OPNUM)

6.1   FUNCTION CODES

        0=OFFLINE
        1=READ
        2=WRITE
        3=WRITE EOF
        4=SPACE FORWARD
        5=SPACE REVERSE
        6=WRITE WITH EXTENDED IRG
        7=REWIND

6.2   DENSITY (BITS 13,14 OF UNIT DESCRIPTION)

        00=200 BPI -- 7 TRACK
        01=556 BPI -- 7 TRACK
        02=800 BPI -- 7 TRACK
        03=800 BPI -- 9 TRACK

6.3   PARITY (BIT 11 OF UNIT DESCRIPTION)

        1=EVEN PARITY
        0=ODD PARITY

6.4   UNIT SELECT (BITS 8,9,10 OF UNIT DESCRIPTIONS)

        SET TO DESIRED UNIT NUMBER (0-7)

7.   PROGRAM DESCRIPTION

        IN ORDER TO MAINTAIN THE CONTINUOUS EXECUTION OF
        THE OPERATIONS DESCRIBED THE PROGRAM IS ORGANIZED AS
        FOLLOWS:

        START
        INITIALIZE THE TM,A,B-11
        SET UP TAPE PARAMETERS (DENSITY, PARITY, BYTE COUNT, DATA ADDRESS)
        SELECT DEVICE TO TEST   (UNIT NUMBER)
        EXECUTE OPERATION   (SET FUNCTION FROM OP TABLE AND SET GO=1)
        AWAIT END OF OPERATION (TAPE UNIT READY)
        STOP IF LOC. 176 BIT 0:=1
        DO OPERATION DELAY (OP DELAY)
        STOP IF LAST OPERATION IN SEQUENCE AND LOC 176 BIT 1:=1
        POINT TO NEXT FUNCTION CODE IN OP TABLE
        JUMP BACK TO START
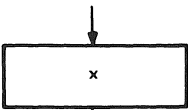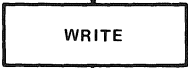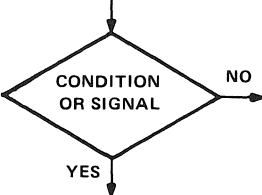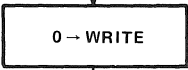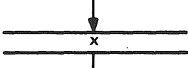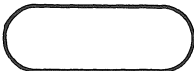
7.1   FLOW: START: HOUSEKEEPING
                INIT: CLEAR TM,A,B-11
                SET UP: SET UP REQUIRED REGISTERS
                EXECUTE: SET FUNCTION AND GO=1
                AWAIT END: LOOP ON TUR=0 AS LONG AS ALLOWED BY READY DELAY
                STOP: IF BIT 0:=1 (LOC 176)
                DELAY: PER OP DELAY
                END OF SEQUENCE? IF NOT JUMP TO START
                STOP: IF BIT 1:=1 (LOC 176)
                JUMP TO START RESTART SEQUENCE

8.   LISTING

.ENDR

APPENDIX C
FLOW DIAGRAM GLOSSARY

FLOW DIAGRAM GLOSSARY

☐ x	x = Description of an event or action (lower case).
☐ WRITE	The signal level WRITE is asserted.
☐ ↓ WRITE	The signal level WRITE is negated.
◇ CONDITION OR SIGNAL (NO / YES)	If condition or signal is true flow follows YES branch, otherwise flow follows NO branch.
☐ 1 → WRITE	A flip-flop is set asserting WRITE.
☐ 0 → WRITE	A flip-flop is reset negating WRITE.
═ x ═	Delay. x = amount of delay or delay range.
○	On page connector.
⬠	Off page connector.
⬭	Beginning or ending point of a flow diagram

11-4781
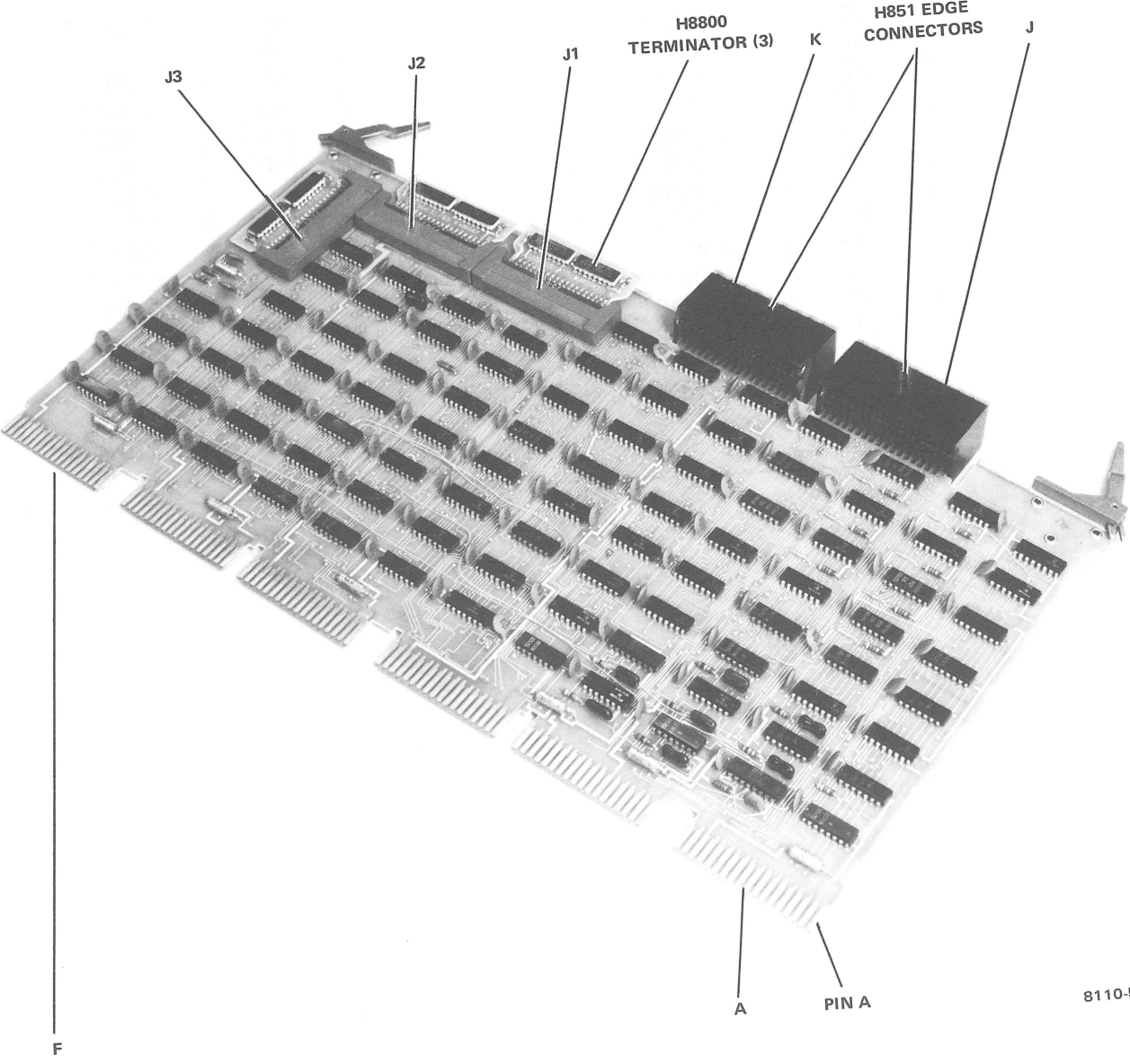
Figure D-1   M8926 Input/Output Connectors

Table D-1 M8926/TMB11 Interface Signals

Connector	Pin	Signal	Connector	Pin	Signal
J	JB1	CWFMK	K	KB1	CLRCS
	JC1	CPEVN		KC1	CLRCE
	JD1	CWDR		KD1	CCRCE
	JE1	CSET		KD2	CFMK
	JF1	CINIT		KE1	CEOT
	JH1	CREV		KE2	CRDP
	JJ1	CWD7		KF1	C7CH
	JJ2	CWRE		KF2	CRD7
	JK1	CWD6		KH1	CSELR
	JK2	CRWD		KH2	CRD6
	JL1	CWD5		KJ1	CVPE
	JL2	CFWD		KJ2	CRD5
	JM1	CWD4		KK1	CWRL
	JM2	CWXG		KK2	CRD4
	JN1	CWD3		KL1	CBOT
	JP1	CWD2		KL2	CRD3
	JP2	CDEN5		KM2	CRD2
	JR1	CWD1		KN2	CRD1
	JR2	CDEN8		KP1	CRWS
	JS1	CWD0		KP2	CRD0
	JT2	CSEL2		KR1	CCRCS
	JU2	CSEL1		KS1	CWRS
	JV2	CSEL0		KT2	CTUR
				KU2	CSDWN
				KV2	CRDS

Table D-2 M8926/Slave Bus Interface Signals

Connector	Pin	Signal	Connector	Pin	Signal
J1	A	WD0 (SB)	J2	A	RD0 (SB)
	C	WDP (SB)		C	RDP (SB)
	E	WD1 (SB)		E	RD1 (SB)
	H	WD7 (SB)		H	RD7 (SB)
	K	WD2 (SB)		K	RD2 (SB)
	M	WD6 (SB)		M	RD6 (SB)
	P	REC (SB)		P	RD3 (SB)
	S	ACCL (SB)		S	RD5 (SB)
	U	SS1 (SB)		U	RD4 (SB)
	W	LRC STRB (SB)		W	RSDO (SB)
	Y	SS2 (SB)		Y	BOT (SB)
	AA	WD5 (SB)		AA	END PT (SB)
	CC	WD4 (SB)		EE	RWND (SB)
	EE	WD3 (SB)		KK	TUR (SB)
	HH	SS0 (SB)		MM	WRT CLK (SB)
	KK	SLAVE SET PLS (SB)		PP	FWD (SB)
	MM	EMD (SB)		RR	CLOCK (SB)
	UU	STOP (SB)		SS	WRITE (SB)
				UU	REV (SB)
			J3	A	MOL (SB)
				C	7CH (SB)
				Y	RWS (SB)
				CC	WRL (SB)
				EE	DEN0 (SB)
				KK	SDWN (SB)
				SS*	DEN 2 (SB)
				UU	DEN 1 (SB)

*Tied to ground on M8926

D-3

Table D-3   M8926/Host TU10W Interface Signals

| Connector	Pin	Signal	Connector	Pin	Signal
A	D2	WDP (SB)	D	D2	WRITE (SB)
	E2	WD7 (SB)		E1	CLOCK (SB)
	F2	WD6 (SB)		E2	WRT CLK (SB)
	K2	LRC STRB (SB)		M2	BOT (SB)
	H2	ACCL (SB)		P2	MRD4
	M2	WD5 (SB)		R2	MRD3
	P2	WD3 (SB)		S2	MRD2
	S2	SLAVE SET PLS (SB)		U2	MRD1
	U2*	INIT PLS (SB)		V2	MRD0
	V2	STOP (SB)			
B	D2*	DRV CLR PLS (SB)	E	D2	7CH (SB)
	E2	EMD (SB)		P2	DEN 0 (SB)
	H1†	SLAVE BUS ENBL		S2	SDWN (SB)
	H2	SS0 (SB)		U2*	1 RD (SB)
	K2	WD4 (SB)		V2	DEN 1 (SB)
	M2	SS2 (SB)			
	P2	SS1 (SB)	F	D2†	DEN 2 (SB)
	R2	REC (SB)		K2	WRL (SB)
	S2	WD2 (SB)		M2	RWS (SB)
	U2	WD1 (SB)		V2	MOL (SB)
	V2	WD0 (SB)			
C	D2	MRDP			
	E2	MRD7			
	F2	MRD6			
	H2	MRD5			
	K2	RSDO			
	M2	END PT (SB)			
	P2	RWND (SB)			
	S2	TUR (SB)			
	U2	FWD (SB)			
	V2	REV (SB)			

*Tied to +3 V on M8926
†Tied to ground on M8926

APPENDIX E
TMB11/TU10W DATA SHEETS

7475 4-BIT BISTABLE LATCH

The 7475 latches are used for temporary storage of binary information. Information present at a data (D) input is transferred to the R output when the clock is high, and the R output will follow the data input as long as the clock remains high. When the clock goes low, the information present at the data input at the time of the transition is retained at the R output until the clock is permitted to go high. Input ENB1 is the clock input for data inputs D0 and D1. ENB2 is the clock input for data inputs D2 and D3.
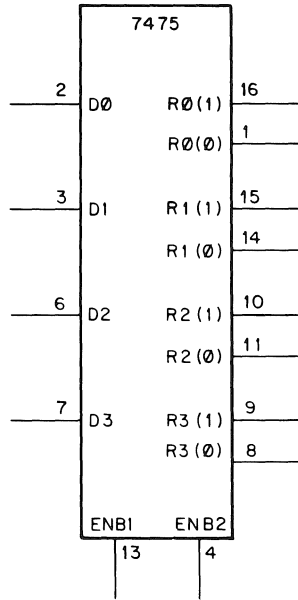
DN INPUTS		RN (1) OUTPUTS		CLOCK INPUTS
D0	0 1	0 1	R0	ENB1
D1	0 1	0 1	R1	
D2	0 1	0 1	R2	ENB2
D3	0 1	0 1	R3	

VCC PIN 5
GND PIN 12

NOTE:
1. RN (0) Outputs = inverted RN (1) outputs.
2. ENB1 and ENB2 clock on negative going edge.

IC-7475

E-2

7485 4-BIT COMPARATOR

The 7485 performs magnitude comparison of straight binary or straight BCD codes. Three fully decoded decisions (A > B, A < B, A = B) about two 4-bit words (A,B) are made and externally available at three outputs.

```
                    ┌──────────────────┐
                    │      7485         │
              Ø1     │                  │
         ────────┤ B3 │                  │
              15     │                  │
         ────────┤ A3 │                  │
              14     │                  │         Ø5
         ────────┤ B2 │          A > B ├────────
              13     │                  │         Ø6
         ────────┤ A2 │          A = B ├────────
              11     │                  │         Ø7
         ────────┤ B1 │          A < B ├────────
              12     │                  │
         ────────┤ A1 │                  │
              Ø9     │                  │
         ────────┤ B0 │                  │
              1Ø     │                  │
         ────────┤ A0 │                  │
                    │  IN >  IN =  IN <  │
                    └───┬──────┬──────┬──┘
                        │Ø4    │Ø3    │Ø2
```
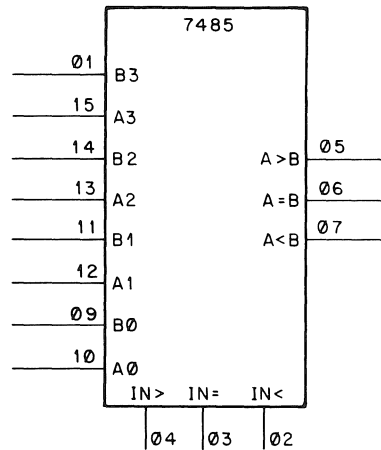
VCC = PIN 16
OND = PIN Ø8

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	IN >	IN <	IN =	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

IC-7485

E-3

8251 4 TO 10 DECODER

8751 TRUTH TABLE

| INPUT				f OUTPUT									
D0	D1	D2	D3	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	0	1
1	1	0	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0

1 = High
0 = Low
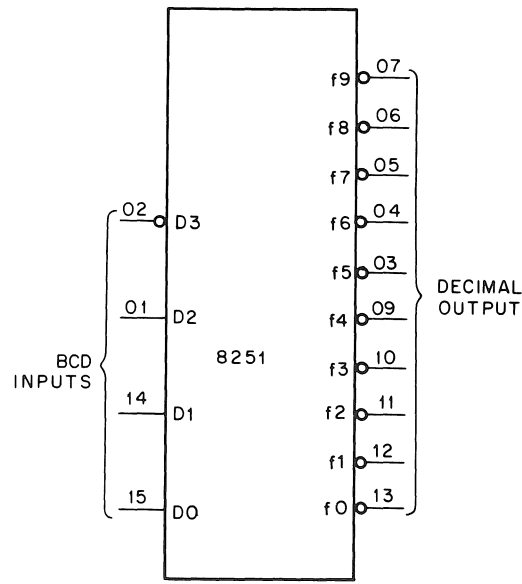
VCC = PIN 16
GND = PIN 08

IC-8251

E-4

8266 2-INPUT, 4-BIT DIGITAL MULTIPLEXER

The multiplxer is able to choose from two different input sources, each containing 4 bits: A = (A0, A1, A2, A3), B = (B0, B1, B2 B3). The selection is controlled by the input S0, while the seccond control input, S1, is held at zero.
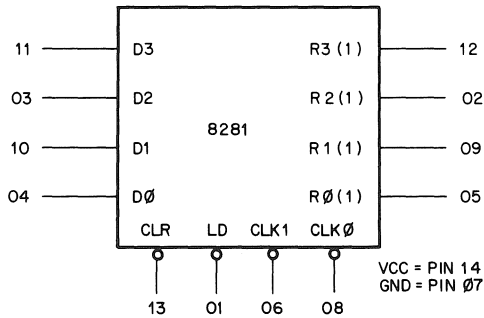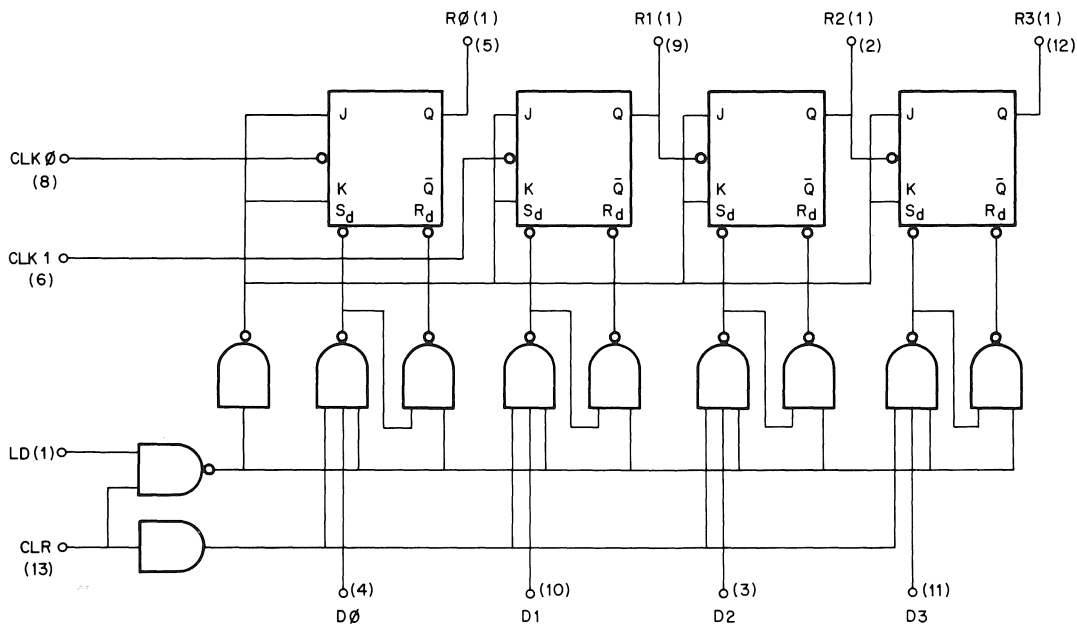
TRUTH TABLE

SELECT LINES		OUTPUTS
S0	S1	$F_n(0, 1, 2, 3)$
0	0	B_n
0	1	B_n
1	0	$\bar{A}_n$
1	1	1

VCC = PIN 16
GND = PIN 08
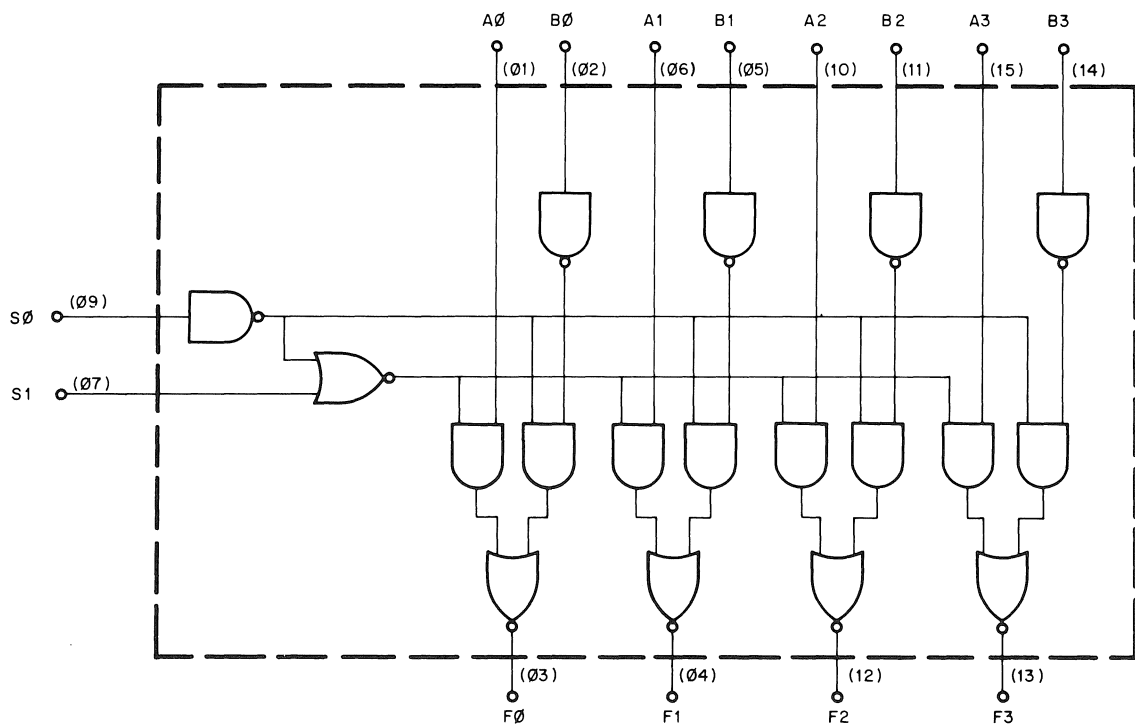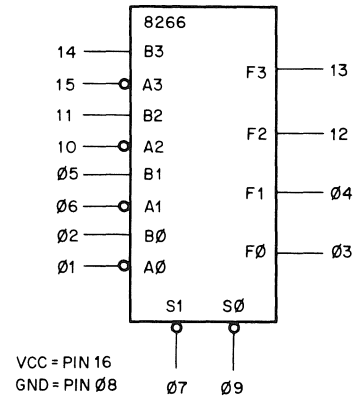
IC- 8266

8281 4-BIT BINARY COUNTER/STORAGE ELEMENT

The 8281 Binary Counter may be connected as a divide-by-two, eight, or sixteen counter. The counter has a strobed parallel entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the LD input is put at the "0" level. It has a reset (CLR) input which is common to all four bits. A "0" on the CLR line produces "0" at all four outputs. The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

TRUTH TABLE					
COUNT (CLKØ)	LD	RØ(1)	R1(1)	R2(1)	R3(1)
	L	DØ	D1	D2	D3
0	H	L	L	L	L
1	H	H	L	L	L
2	H	L	H	L	L
3	H	H	H	L	L
4	H	L	L	H	L
5	H	H	L	H	L
6	H	L	H	H	L
7	H	H	H	H	L
8	H	L	L	L	H
9	H	H	L	L	H
10	H	L	H	L	H
11	H	H	H	L	H
12	H	L	L	H	H
13	H	H	L	H	H
14	H	L	H	H	H
15	H	H	H	H	H

NOTES:
1. Output RØ(1) connected to input CLK1.
2. H = high; L = low

VCC = PIN 14
GND = PIN Ø7

IC-8281

E-6

9301 1 OF 10 DECODER

The 9301 Decoder accepts four active HIGH BCD inputs and provides 10 mutally exclusive active LOW outputs. The logic design of the 9301 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs. The most significant D3 input produces a useful inhibit function when the 9301 is used as a 1 of 8 decoder.

TRUTH TABLE

DØ	D1	D2	D3	fØ	f1	f2	f3	f4	f5	f6	f7	f8	f9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

IC-9301

E-7
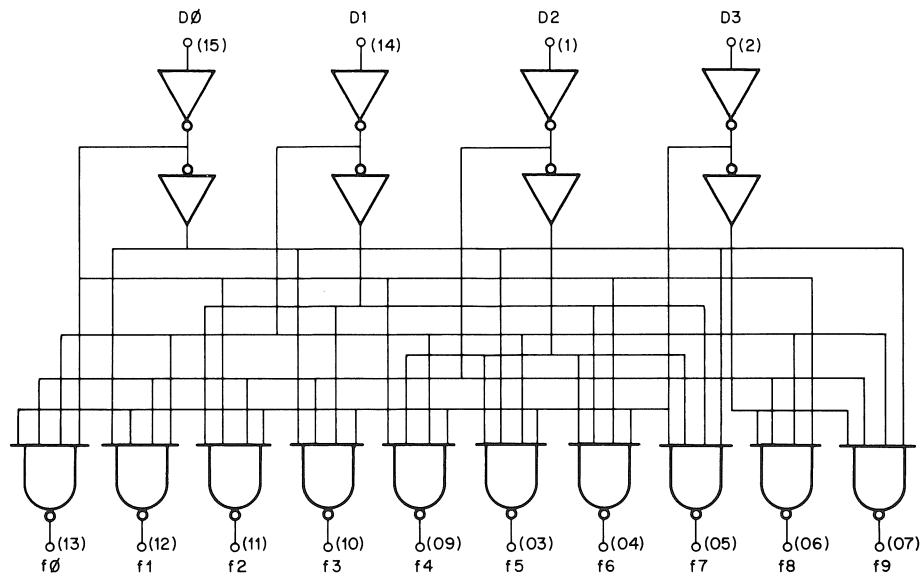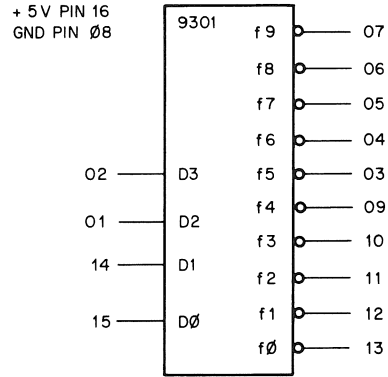
74157 QUAD 2 TO 1 MULTIPLEXER

INPUTS				OUTPUT
STB	S0	A	B	f
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant.

```
  13 ─┤ B3                        06 ─┤ B1
                                      
  14 ─┤ A3        f3 ├─ 12        05 ─┤ A1        f1 ├─ 07
          74157                          74157
  10 ─┤ B2        f2 ├─ 09        03 ─┤ B0        f0 ├─ 14
                                      
  11 ─┤ A2                        02 ─┤ A0
        STB    S0                      STB    S0
         ○                              ○
         15   │01                       15   │01
```
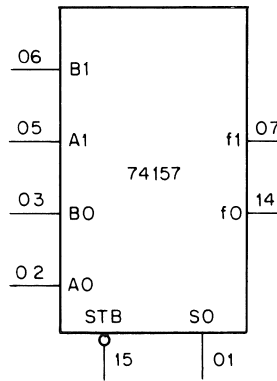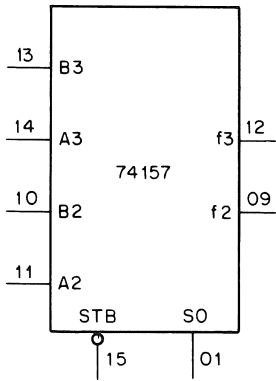
VCC = PIN 16
GND = PIN 08

IC-74157

74161 SYNCHRONOUS 4-BIT COUNTER

```
                    3  ┌─────────────┐ 14
         ┌────────────│ DO    RO(1) │────────┐
         │          4 │             │ 13     │
   DATA ─┤ ───────────│ D1    R1(1) │──────  ├─ OUTPUTS
  INPUTS │          5 │             │ 12     │
         │ ───────────│ D2    R2(1) │──────  │
         │          6 │             │ 11     │
         └────────────│ D3    R3(1) │────────┘
                      │─────────────│
                      │    74161    │
                    1 │             │
    CLEAR ───────────○│ CLR         │
                    9 │             │
     LOAD ───────────○│ LD          │
                    2 │             │
    CLOCK ───────────│ CLK          │
 ENABLE P ─── 7 ─╮   │ CNT EN       │
 ENABLE T ─── 10 ─╯   │             │
                      │ CRY EN   CO │ 15 ── CARRY
                      └─────────────┘       OUTPUT
```

GND = PIN 8
+5V = PIN 16
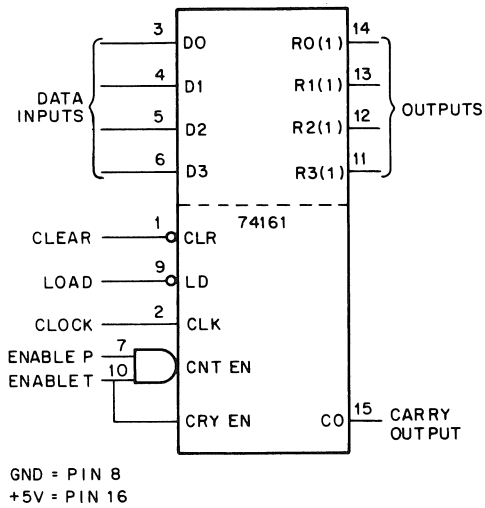
typical clear, preset, count, and inhibit sequences for 74161

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit
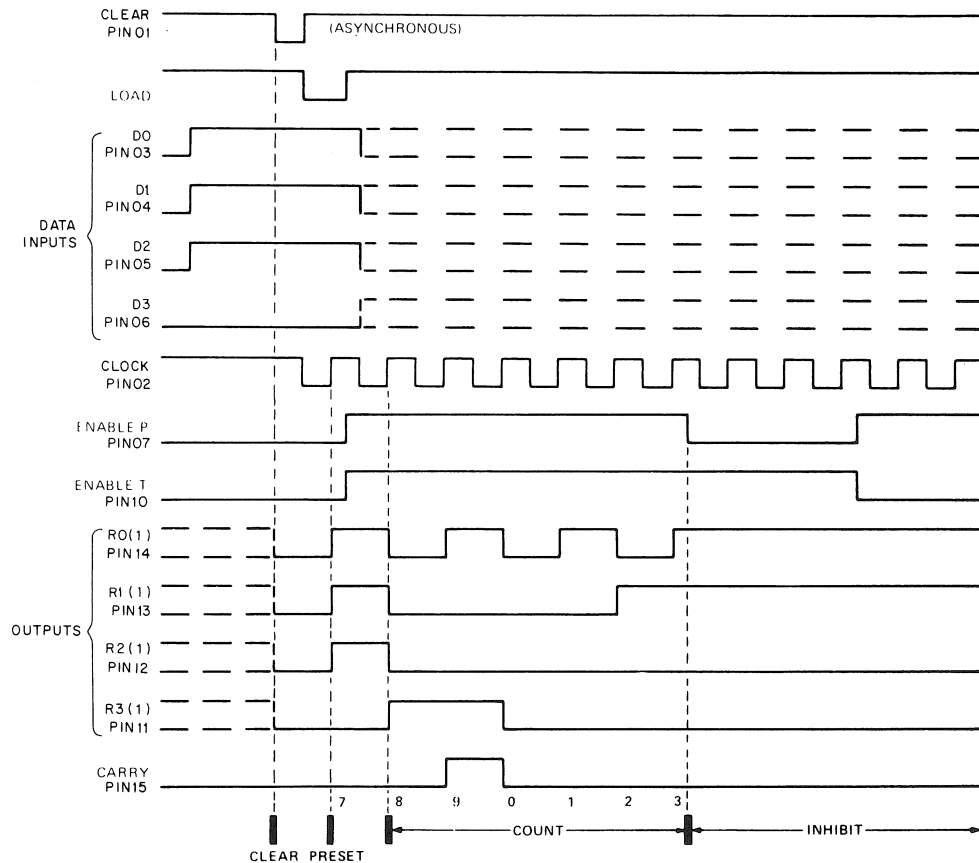
IC-74161

74164   8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input.

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	R∅(1)
H	H	H
L	H	L
H	L	L
L	L	L

+5V = PIN 14
GND = PIN ∅7
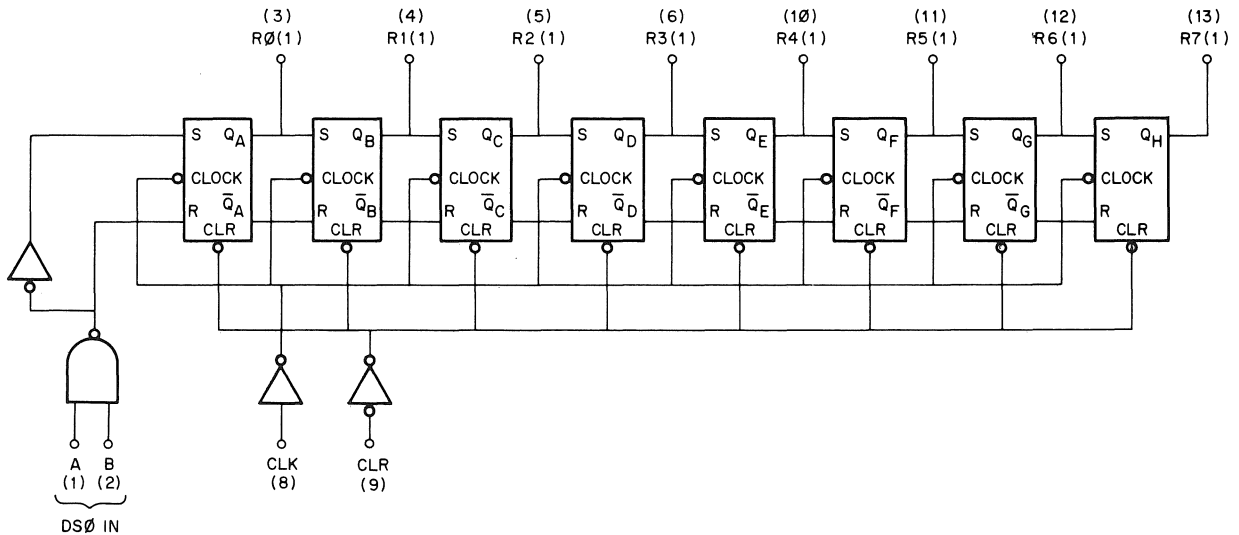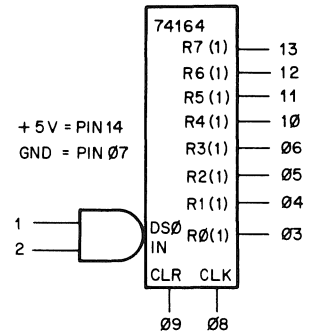
IC-74164

74174 HEX D FLIP-FLOP REGISTER

TRUTH TABLE

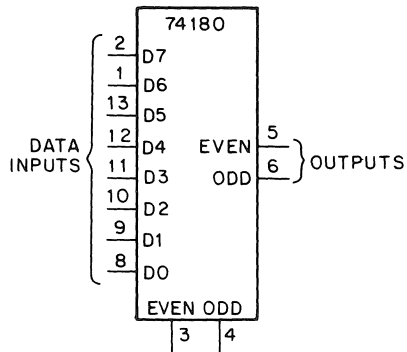| INPUT t_n	OUTPUT t_n+1
D	R(1)
H	H
L	L

t_n = Bit time before clock pulse.

t_n+1 = Bit time after clock pulse.
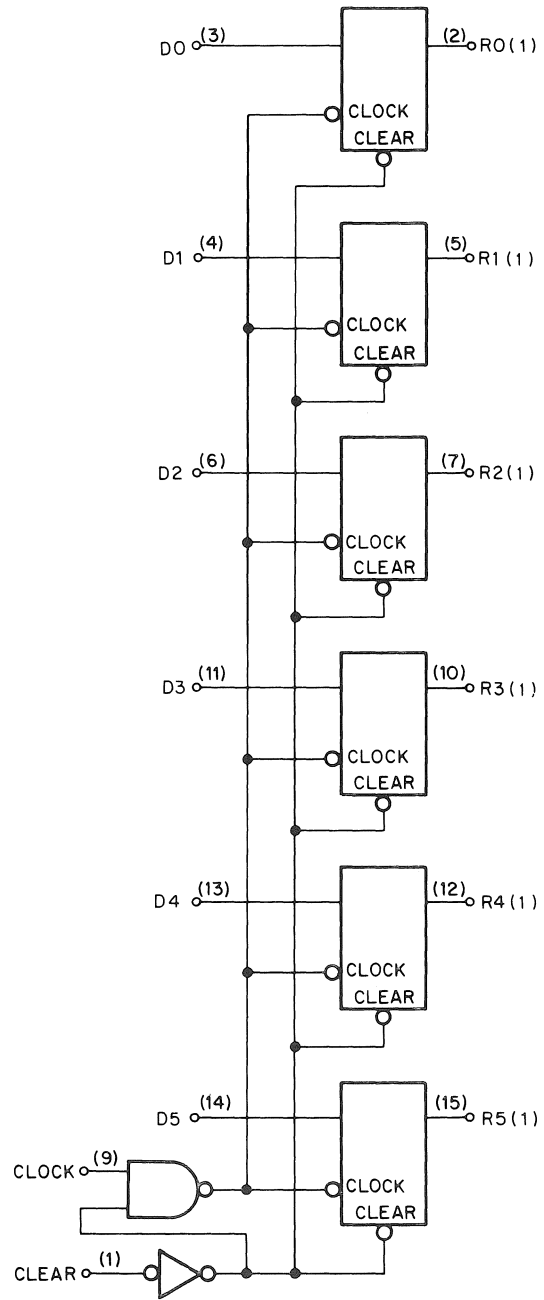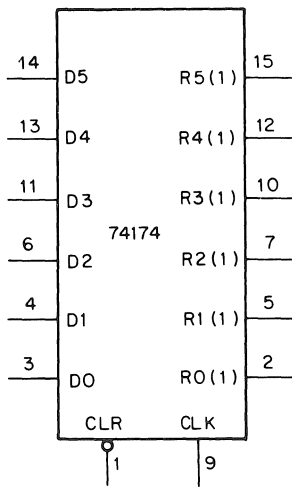
Pin (16) = V_{CC}, Pin (8) = GND

IC-74174.

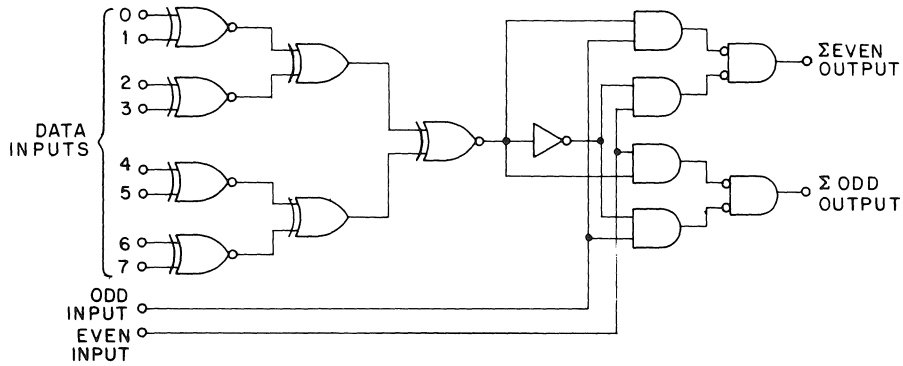## 74180   9-BIT ODD/EVEN PARITY GENERATOR/CHECKER


```
            ┌ 2
            │──── D7
            │ 1
            │──── D6
            │ 13
            │──── D5        74180
  DATA      │ 12
  INPUTS ───┤──── D4    EVEN ─── 5
            │ 11                        } OUTPUTS
            │──── D3    ODD  ─── 6
            │ 10
            │──── D2
            │ 9
            │──── D1
            └ 8
             ──── D0
                  EVEN  ODD
                   3    4
```

V_{CC} = PIN 14
GND = PIN 7

TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = IRRELEVANT

IC-74180

E-12

74193 4-BIT UP/DOWN COUNTER

The 74193 Binary Counter has an individual asynchronous preset to each flip-flop, a fully independent clear input, internal cascading circuitry, and provides synchronous counting operations.

typical clear, load, and count sequences for 74193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
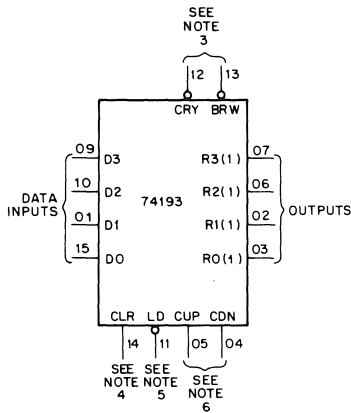
NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count down input must be high; when counting down, count-up input must be high.
3. Produce pulses equal to width of count pulses during: Underflow (BORROW)
   Overflow (CARRY)
4. CLR input high forces all outputs low. CLR overrides load, data and DN/UP inputs.
5. Preset to any state by applying input data with load input low. Output changes to agree with inputs independent of count pulses.
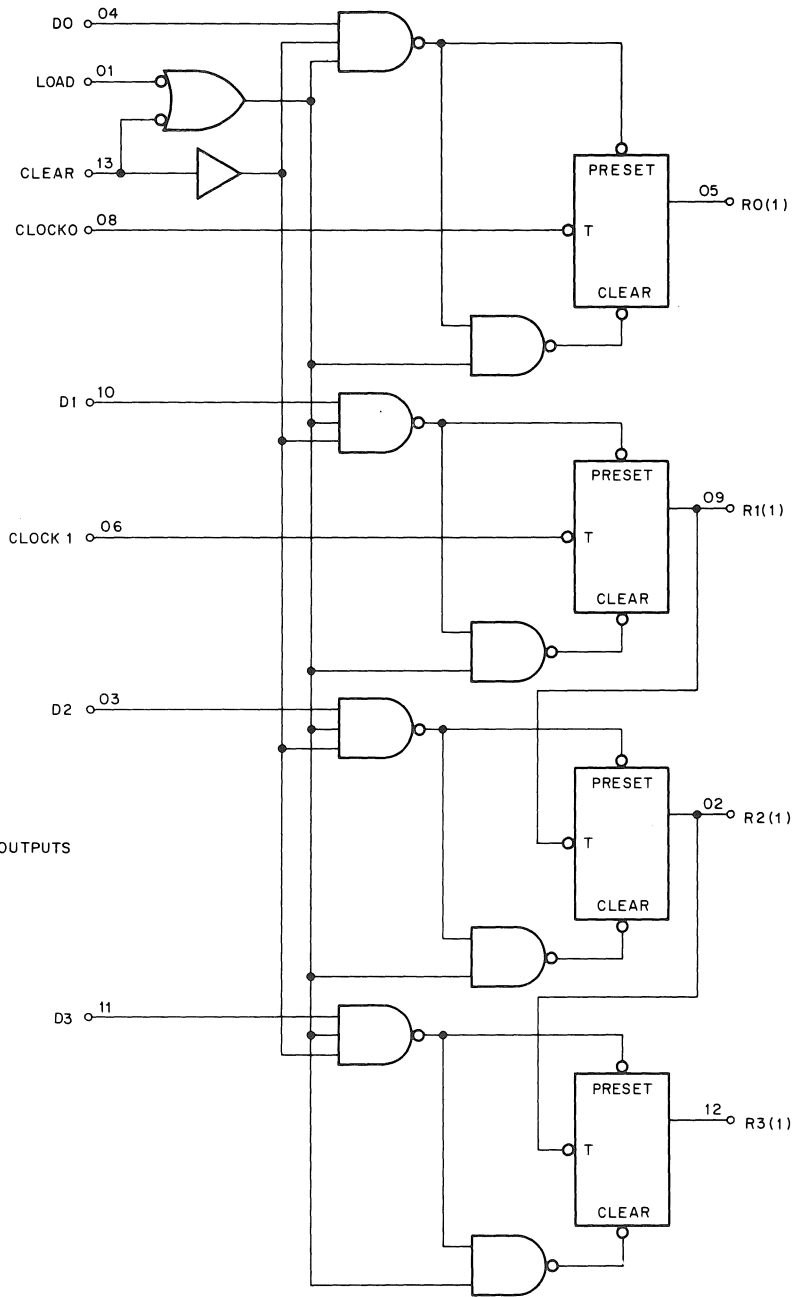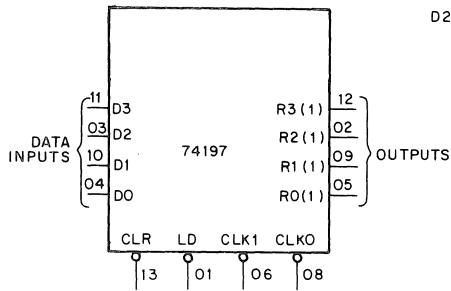6. Select DN or UP clock while other is held high.
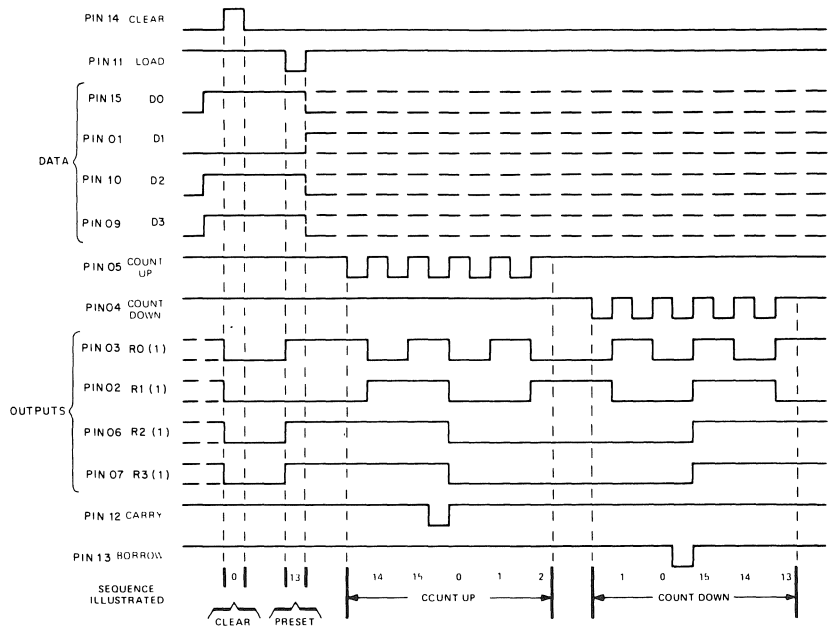
E-13
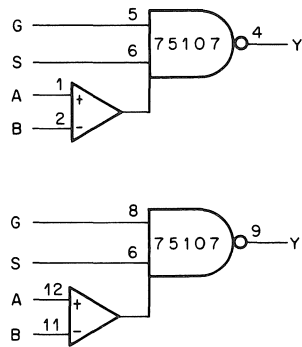
74197 4-BIT COUNTER

74197 TRUTH TABLE

COUNT	OUTPUT			
CLOCK 1 INPUT	R3 (1)	R2 (1)	R1 (1)	RO (1)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

RO (1) connected to CLOCK 2 input.

IC-74197

E-14

75107 SENSE AMPLIFIER (DUAL-IN-LINE)


```
G ———————5 ╲
            ╲ 75107 ⊸4
S ———————6  ╱         Y
A ——1 ┃+╲
      ┃  ╲
B ——2 ┃  ╱
      ┃-╱

G ———————8 ╲
            ╲ 75107 ⊸9
S ———————6  ╱         Y
A ——12 ┃+╲
       ┃  ╲
B ——11 ┃  ╱
       ┃-╱
```

GND = 7
-VCC = 13
+VCC = 14

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geqslant 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leqslant -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

IC-75107

E-15

TMB11/TU10W DECmagtape SYSTEM
MAINTENANCE MANUAL (TMB11-E/F SYSTEM)
EK-TMBEF-MM-002

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_____
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What faults or errors have you found in the manual?_____
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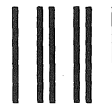Accessories and Supplies Group
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