MS11-E–J MOS memory maintenance manual

digital

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MS11-E–J MOS memory maintenance manual

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CHAPTER 1
INTRODUCTION

The MS11-E – MS11-J (referred to herein as MS11) memories comprise a group of MOS semi-conductor, random-access memories that are designed to be used with the PDP-11 Unibus. Each memory assumes the role of a slave device to the PDP-11 processor or to any peripheral device that is designated bus master. The group provides storage for 16- or 18-bit data words (two parity bits are included in the 18-bit word), with capacity ranging from 4096 (4K) words to 16,384 (16K) words in 4K blocks. An MS11 memory can be assigned adjacent 4K blocks of addresses anywhere within the 124K Unibus address space. A special feature of the 16K MS11 allows the assignment of part of the I/O page to memory, although this can be done only for processors without memory management. Table 1-1 lists the significant specifications of an MS11 system.

The logic components of an MS11 memory are mounted on a single hex printed circuit board; the module has DEC designation M7847. The storage elements are 4096 × 1-bit, N-channel, MOS memory devices. A row of 18 of these devices is mounted on a module for each 4K block of addresses that is assigned to the memory; e.g., a 16K memory has 4 rows of 18 devices, an 8K memory has but 2 rows of devices. Table 1-2 lists the available MS11 options and the respective bit and word capacities.

The use of MOS memory circuits provides advantages (both economical and operational) not available with core memory systems. The cost-per-bit for MOS memories is low and, unlike core memory, this cost remains approximately constant with size.

Unlike core, MOS memory provides non-destructive readouts; consequently, the write-after-read cycle time associated with core memory is eliminated. Furthermore, with dynamic MOS devices such as those used in the MS11, power consumption is much lower than with core memory. The disadvantage of MOS storage volatility (i.e., data is not retained when power is lost) is compensated for by the availability of battery-supported power supplies that enable data retention for as long as several hours. The MS11 is designed for a special low-power mode to maximize the effectiveness of battery-powered operation.

Because the data storage element is a capacitor in the MOS storage device, all memory locations in the MOS memory must be periodically refreshed so that the data remains valid. The controller on the memory module includes the logic and timing circuits to carry out the periodic refreshing operation.

Table 1-1
Significant System Specifications

Characteristic	Specification	
Storage Capacity	4096 (4K) to 16,384 (16K) words, in 4K blocks	
Data Word Length	16 data bits, 2 parity bits	
Maximum Access Time (ns)		
Normal Operation	550	
Refresh Conflict*	1250	
Maximum Cycle Time (ns)		
Normal Operation	700	
Refresh Conflict*	1400	
Refresh Cycle Rate	One cycle every 25 μs (typical); maximum of one cycle every 22.5 μs	
Maximum Power Consumption (watts)	Idle	700 ns Cycle
MS11-E	12.3	23.5
MS11-F	13.0	24.3
MS11-H	13.8	25.0
MS11-J	14.5	25.8
Maximum Current Drain (mA)	Idle	700 ns Cycle
MS11-E		
+5 Vdc	1500	1500
BB+5 Vdc	500	500
+15 Vdc	50	800
-15 Vdc	100	100
MS11-F		
+5 Vdc	1500	1500
BB+5 Vdc	500	500
+15 Vdc	100	850
-15 Vdc	100	100
MS11-H		
+5 Vdc	1500	1500
BB+5 Vdc	500	500
+15 Vdc	150	900
-15 Vdc	100	100
MS11-J		
+5 Vdc	1500	1500
BB+5 Vdc	500	500
+15 Vdc	200	950
-15 Vdc	100	100

*A characteristic of dynamic MOS memory devices is that they must be cycled periodically to ensure data validity. These cycles are known as refresh cycles and the controller on these memory modules has all the logic and timing circuits necessary to ensure that these cycles are performed. Should a processor or NPR request (MSYN) come during a refresh cycle, it is held up until the refresh cycle is completed and then processed. The Refresh Conflict time is the maximum amount of time that a normal cycle may be held up by a refresh cycle. The amount of time lost to bus masters because of refresh is dependent on the bus activity. For a system that uses the bus at a maximum rate (700 ns cycles) the loss of memory availability is less than 3 percent. For a system with an average bus cycle every 1.4 μs, the loss of availability is typically less than 3/4 percent.

Table 1-2
MS11 Options

Option Designation	Word Bit Length	Data Word Capacity
MS11-E	16	4K
MS11-EP	18	4K
MS11-F	16	8K
MS11-FP	18	8K
MS11-H	16	12K
MS11-HP	18	12K
MS11-J	16	16K
MS11-JP	18	16K

NOTE
18-bit words include two parity bits; an M7850 Parity Control module must be used with the parity options.

CHAPTER 2
INSTALLATION

2.1 GENERAL

Installation of the MS11 is relatively simple. First, the user should verify that factory-installed jumper wires relating to the number of memory chip banks are in place. Next, certain switches must be arranged to assign Unibus address space to the MS11. The backplane should then be checked to ensure that the required dc voltages are available. Finally, the module is inserted into the backplane and a diagnostic check is carried out to assure correct operation. These procedures are discussed more fully in following paragraphs.

Figure 2-1 shows the MS11 module (an 8K memory is illustrated). The array of chips is located in the upper-right quarter of the board. At the left-center of the board are eyelets W1 - W6, into which appropriate jumpers are inserted. To the lower-right of the eyelets is the DIP switch (E111) which is configured according to the MS11 address assignment. E111 has eight individual contacts that may be identified by numbers or letters on the switch; however, the contacts are identified by etched letters A - J on the printed circuit board (this notation is followed throughout the text and in the logic drawings).

2.2 JUMPER VERIFICATION

The MS11 Memory is shipped with factory installed jumpers appropriate for the memory size. The user should check the module to ensure that the correct jumpers are in place. Table 2-1 lists the memories by size and indicates the jumpers that are installed for each. A 16K memory will normally operate with switch H closed, in addition to the installed jumpers; however, a 16K memory installed in a 32K PDP-11 requires special consideration. Refer to Section 4.2, Address Decoding logic.

2.3 SWITCH ARRANGEMENT

The MS11 Memory is assigned Unibus address space by the arrangement of switches A - E. *The switches must be arranged by the user before the memory is installed.* Read Section 4.2 before attempting to assign address space to the MS11.

2.4 VOLTAGE CHECK

Before the module is inserted in the backplane, check the backplane to ensure that the required dc voltages are present and within tolerance. The dc voltages are listed in Table 2-2; Table 2-3 lists the MS11 pin-outs.

All four dc voltages must be supplied for system operation. If data retention is desired when the ac power is removed, the +5 Vdc supply can be powered down and the other supplies maintained.

Table 2-1
Module Jumper Installation

Memory Designation	Memory Size	Eyelet Pairs Connected by Jumpers		
		W3-W4	W1-W2	W5-W6
MS11-E/EP	4K	X		
MS11-F/FP	8K	X	X	
MS11-H/HP	12K	X	X	X
MS11-J/JP	16K	X	X	X

Table 2-2
MS11 DC Voltage Tolerances

DC Voltage	Minimum	Maximum
+5	4.75	5.25
+15	14.50	16.50
-15	-16.50	-13.50
BB+5	4.75	5.25

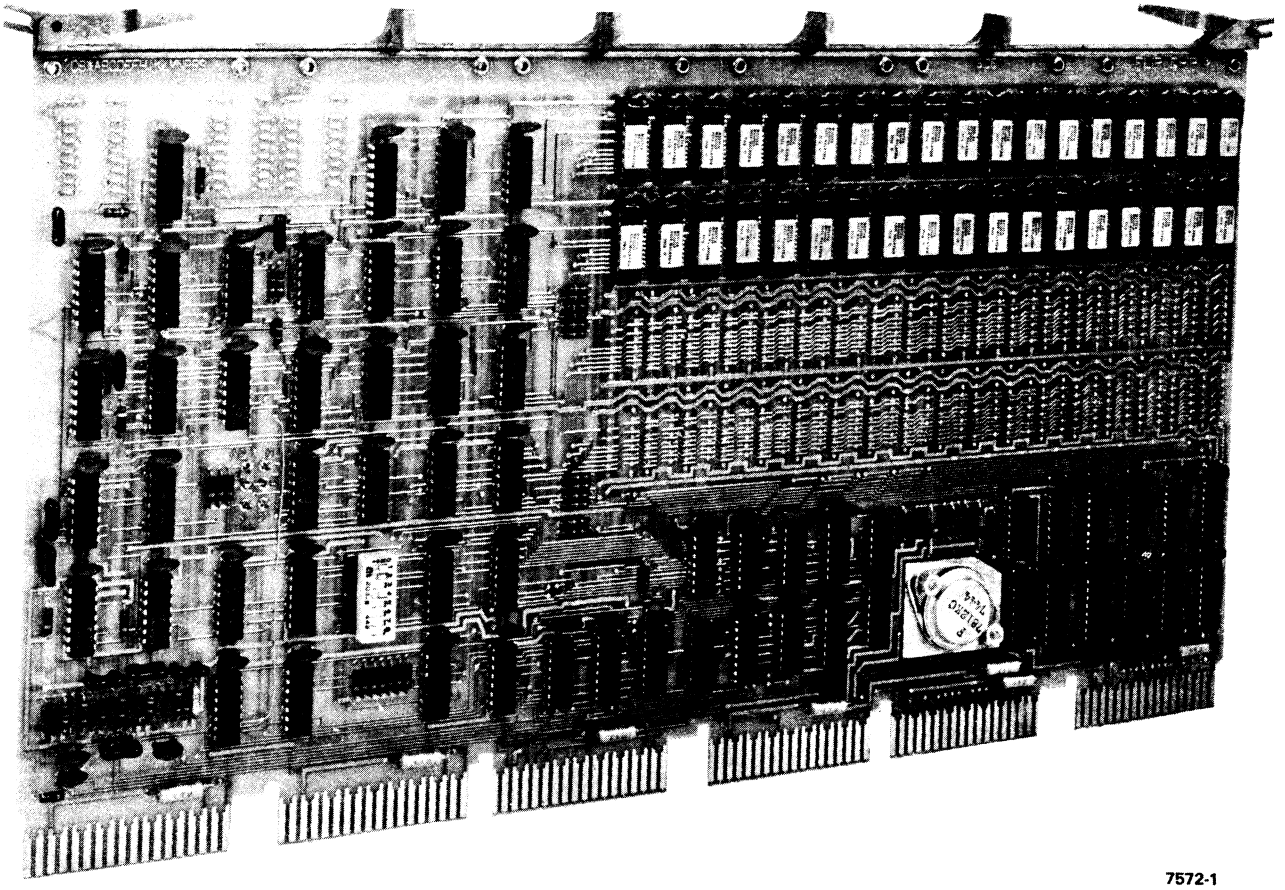


Figure 2-1 MS11-F Module

Table 2-3
MS11 Memory Pinouts

	A		B		C		D		E		F	
	1	2	1	2	1	2	1	2	1	2	1	2
A		+5		+5	*]	+5	TP	+5		+5		+5
B		TP		TP	]		TP					
C	D00	GND		GND		GND		GND		GND		GND
D	D02	D01	BB+5									
E	D04	D03	INT SSYN	PAR DET	TP							
F	D06	D05		DC LO	TP							
H	D08	D07	A01	A00								
J	D10	D09	A03	A02								
K	D12	D11	A05	A04	TP			*]				
L	D14	D13	A07	A06				]				
M		D15	A09	A08	TP			*]				
N	P1		A11	A10				]				
P	P0		A13	A12			TP	*]				
R	+15		A15	A14			TP	]				
S	-15		A17	A16			TP	*]				
T	GND		GND	C1	GND		GND	]	GND		GND	
U			SSYN	C0			TP					
V			MSYN									

*Points marked by] are tied together to provide grant continuity on backplane.

2.5 BACKPLANE INSTALLATION

When the dc voltages have been verified, insert the MS11 into the Unibus backplane. Presently, three backplanes can be used with the MS11, although other backplanes may become available; these three are DD11-C, DD11-D, and DD11-P. The DD11-C is a 4-slot backplane; the MS11 can be inserted into slot 2 or slot 3. The DD11-D is a 9-slot backplane; slots 2 - 8 can be used for the MS11. The DD11-P is another 9-slot backplane, which is used with the PDP-11/04 or PDP-11/34. If an M7850 Parity Control module is to be used with the MS11, it must be installed in the same backplane; the M7850 can occupy any of the backplane slots that are available to the MS11.

2.6 DIAGNOSTIC CHECK

When the memory is connected to the Unibus, run the MS11 diagnostic program to verify that the memory is operable. If a problem arises, follow the instructions in the diagnostic.

CHAPTER 3
CHIP DESCRIPTION

3.1 PHYSICAL DESCRIPTION

The MOS memory device used with the MS11 is a 4096-bit, dynamic, random-access memory circuit. The circuit is packaged in a standard 16-pin DIP that provides high system bit density and is compatible with available automatic testing and insertion equipment. Figure 3-1 is an outline drawing of the chip, showing pin connections. Table 3-1 lists the chip supply voltages.

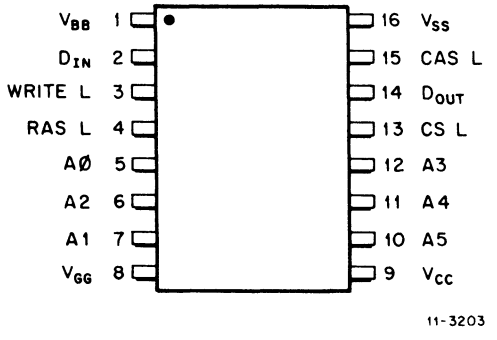


Figure 3-1 Chip Pin Connections

Table 3-1
Chip Supply Voltages

Voltage	Operating Level
V_{GG}	+12 Vdc
V_{CC}	+5 Vdc
V_{SS}	Ground
V_{BB}	–9 V/–5 V*

*Depending on chip type.

3.2 OPERATING DESCRIPTION

A functional block diagram of the chip is shown in Figure 3-2. The 4096 storage locations are arranged in a 64-row by 64-column array. Thus, a cell location can be specified by a 6-bit row address and a 6-bit column address. Because address information is latched into on-chip registers, the chip can be driven by only 6 address lines. The MS11 logic multiplexes 12 address bits, 6 at a time, onto the A0–A5 lines. The RAS L (Row Address Strobe) signal causes row address information to be latched into a 6-bit register, while the CAS L (Column Address Strobe) signal causes column address information, as well as the CS L (Chip Select) signal, to be latched into a 7-bit register. Enable signals applied to 1-of-64 decoders result in one of the 4096 cell locations being selected for a data transfer.

A simplified representation of the chip is shown in Figure 3-3 (all the switches are merely symbolic of more detailed chip operation). The basic cell storage element is a capacitor; a charge voltage of 0–6 V represents logic 0, while a voltage of 6–12 V represents logic 1. Because the charge on the capacitor dissipates with time, it is continually refreshed so that the data it represents remains valid. Any read or write cycle results in a refresh of the data in the addressed locations. During such a cycle, the row address is latched first, and then the 1-of-64 decoder closes all the switches in the selected row. The charge voltage on each capacitor in the row is applied to a Sense Amplifier (SA), which refreshes the data by restoring the charge voltage to its original level. For example, the maximum charge voltage on

a cell capacitor is 12 V, representing logic 1. When the cell is addressed, a portion of the full charge may have leaked off so that the voltage has decreased to, for example, 8 V. The SA forces the voltage back to its full-charge value of 12 V. Similarly, any voltage between 0 and 6 V is restored to a logic 0 level of 0 V.

After the data in the selected row is accessed and refreshed, the column address is latched; the multiplexer selects one of the 64 columns, and the amplified charge voltage on a single capacitor is applied to point "A" in Figure 3-3. If the cycle is a "read", the data is strobed into the tri-state output latch and remains valid until the next time CAS L goes low. If the cycle is a "write", the input buffer/latch drives point A, overriding the SA output and charging the selected cell capacitor.

Since a cell may be addressed infrequently, if at all, during normal read/write operations, a special timing cycle – a refresh cycle – is carried out at regular intervals. In the MS11 Memory, such a cycle occurs approximately every 25 μs. A different row address is supplied by the MS11 logic during each refresh cycle so that the data in all 64 row addresses is refreshed about every 2 ms. The refresh operation is the same as during a read or write cycle, i.e., the row address is latched; the data in each cell of the row is refreshed; the column address is latched (the column address supplied by the MS11 logic is the same during all 64 different refresh cycles); and the cell data is read out to point A. However, during a refresh cycle, the CS L signal is disabled so that neither the input circuit nor the output circuit is enabled. The output latch will go to its high-impedance state, ensuring that power consumption is minimal.

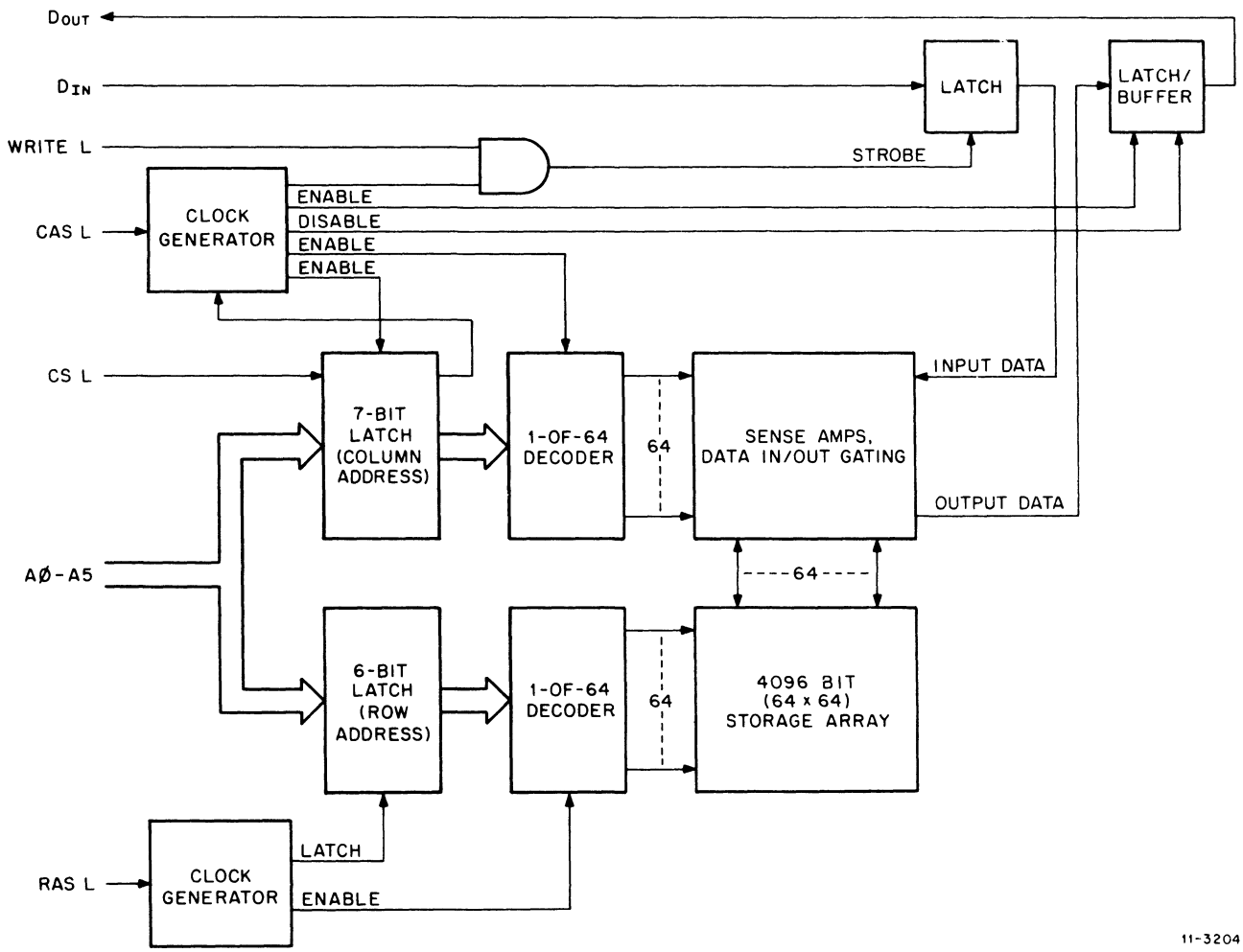


Figure 3-2 (4096 × 1) Bit MOS Chip, Block Diagram

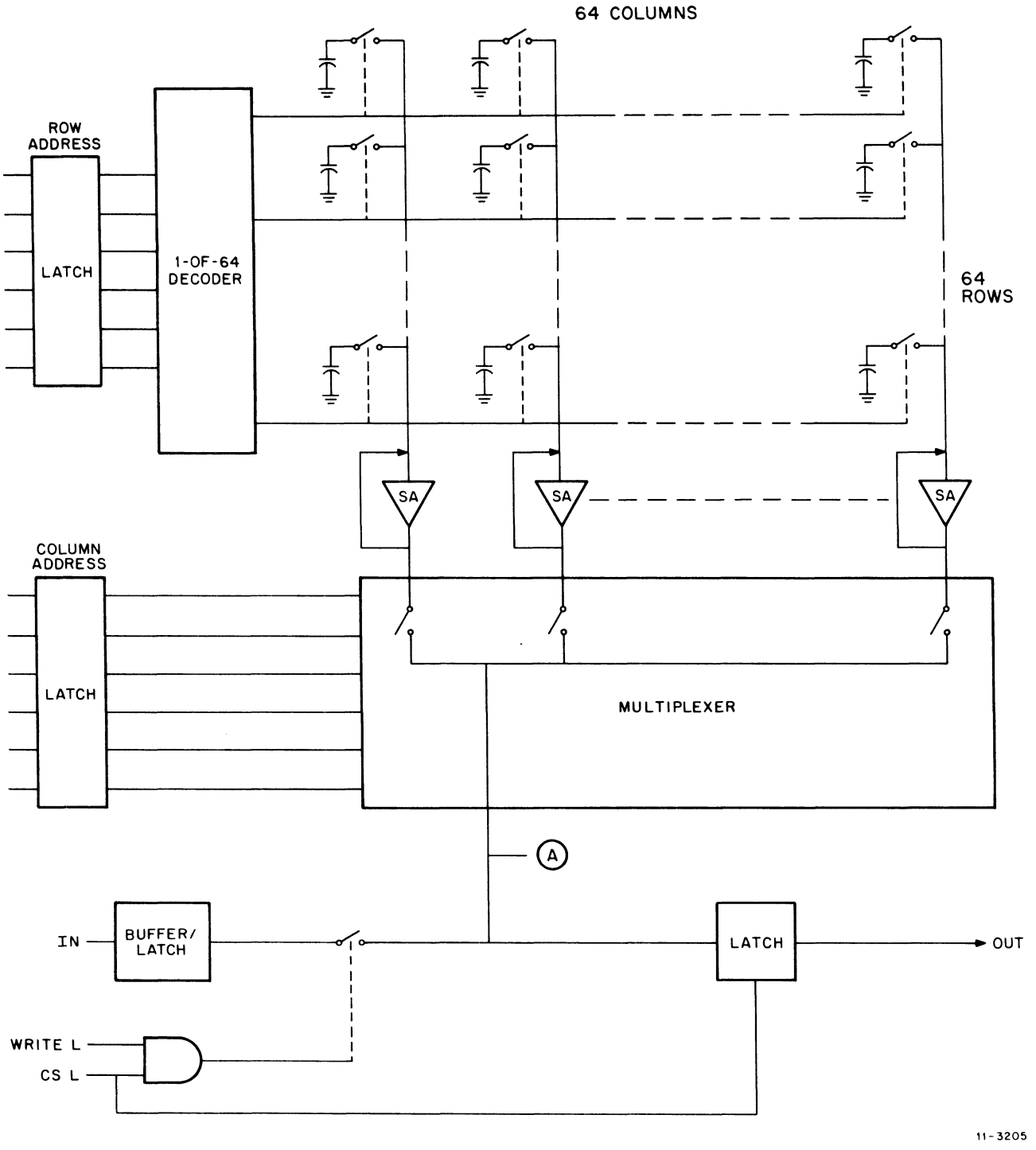
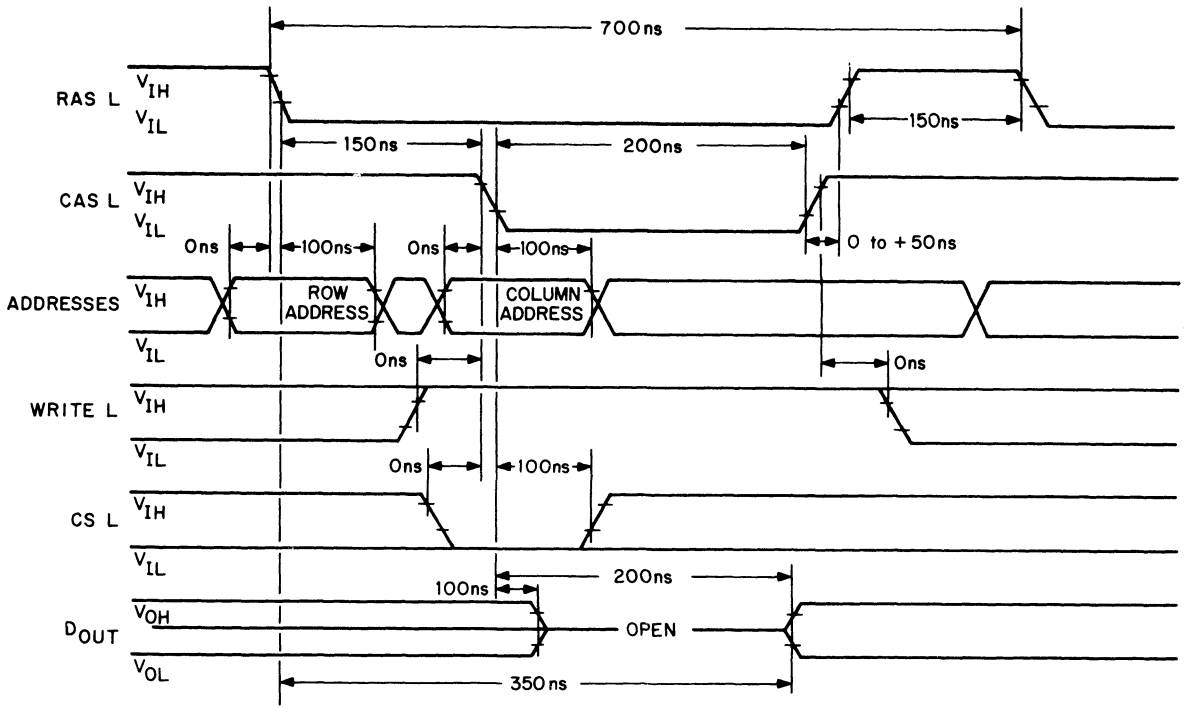


Figure 3-3 MOS Chip, Simplified Data Gating

READ CYCLE (minimum timing)



WRITE CYCLE (minimum timing)

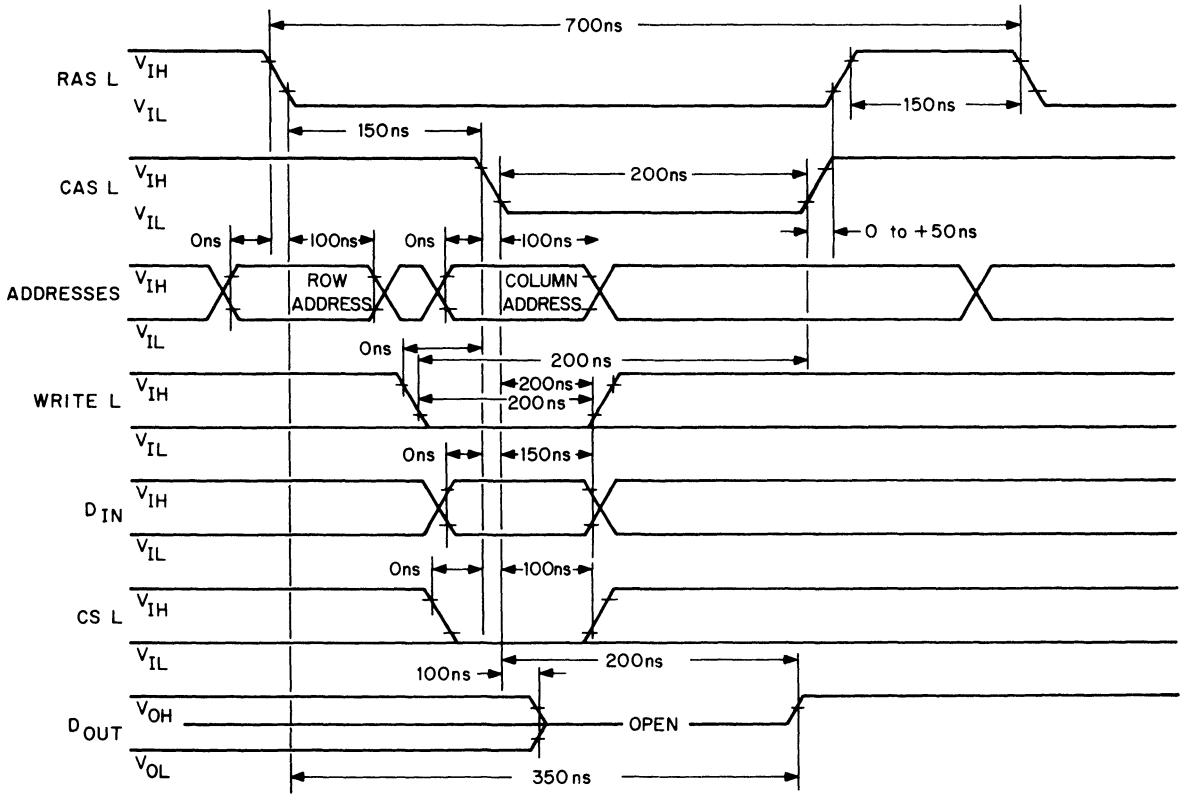


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Figure 3-4 Chip Read/Write Timing

The timing of both a read cycle and a write cycle is illustrated in Figure 3-4. The RAS L signal starts the timing cycle internally. To reduce the overall system power, RAS L is decoded in the MS11 logic and supplied to only the selected bank of chips. The CAS L signal is supplied to all chips, but chips that do not receive a RAS L signal will go to their high-impedance output states.

If data is to be read from the addressed location, the WRITE L signal must be high and the CS L signal must be asserted. The data is strobed into the output latch/buffer at access time (350 ns after RAS L is asserted) and remains valid until CAS L goes negative during a subsequent timing cycle. A write cycle requires that the WRITE L signal go low before access time; the WRITE L command is accepted by the chip only if CS L has been asserted. The data on the D_{IN} line is strobed into an input latch by the negative transition of the CAS L signal. Note that the output latch/buffer goes to logic 1 at access time.

CHAPTER 4
LOGIC DESCRIPTION

4.1 BLOCK DIAGRAM

A block diagram of the MS11 Memory is shown in Figure 4-1. Data is stored in the chip array, which can comprise from one to four rows of chips, each row consisting of 18 chips (a data word contains 16 data bits and two parity bits, if parity checking is employed). The data can be stored or retrieved under control of a bus master. The master specifies the address of a memory location to or from which the data is to be transferred. The Address Decoder logic determines if the address is assigned to the MS11. If it is, timing signals are generated by the timing logic to strobe the address into latches in the Address Path logic. Other timing signals then gate the address information to the storage array where the addressed location is selected.

The bus master supplies Unibus control signals that describe the data transfer direction. These control signals are decoded by the Data Path Control Signal logic, which then generates signals that control the direction of data flow through the Data Path logic. If data is to be placed in the addressed location, the bus master provides the data along with the Unibus control signals. The data is strobed into input latches in the Data Path logic and placed on the Data In (DI) lines. When the addressed location is selected, the data is stored therein. If, instead, data is to be removed from the array, it is placed on the Data Out (DO) lines when the location is selected, strobed into output latches in the Data Path logic, and placed on the Unibus. If parity checking is employed, a Parity Control module generates parity bits during a write operation and checks parity bits during a read operation. In both operations, the parity information is latched into the Data Path logic along with the data itself.

The cell matrix must be refreshed periodically to ensure that the stored data remains valid; consequently, every 25 μs, a refresh operation is performed. During this operation, an address is supplied by the Refresh logic and is applied to the multiplexers in the Address Path logic. The Timing logic signals gate this address information to the cell array. The data in all 64 cells in the row specified by the address is refreshed. At the end of the operation, a register in the Refresh logic is incremented, updating the refresh address by one; during the next operation, the 64 cells in the new row address are refreshed.

The logic represented by each block in Figure 4-1 is shown in detail in the referenced figures. The logic is described in the sections that follow.

4.2 ADDRESS DECODING LOGIC

The Address Decoding logic examines the five most significant bits of the Unibus address to determine if the address is one that has been assigned to the MS11 Memory. If such is the case, the logic generates both the ADDRESS PRESENT H signal, which enables MSYN H to start the MS11 timing sequence, and either RSA L, RSB L, RSC L, or RSD L, which results in one row of memory chips being selected for the data transfer.

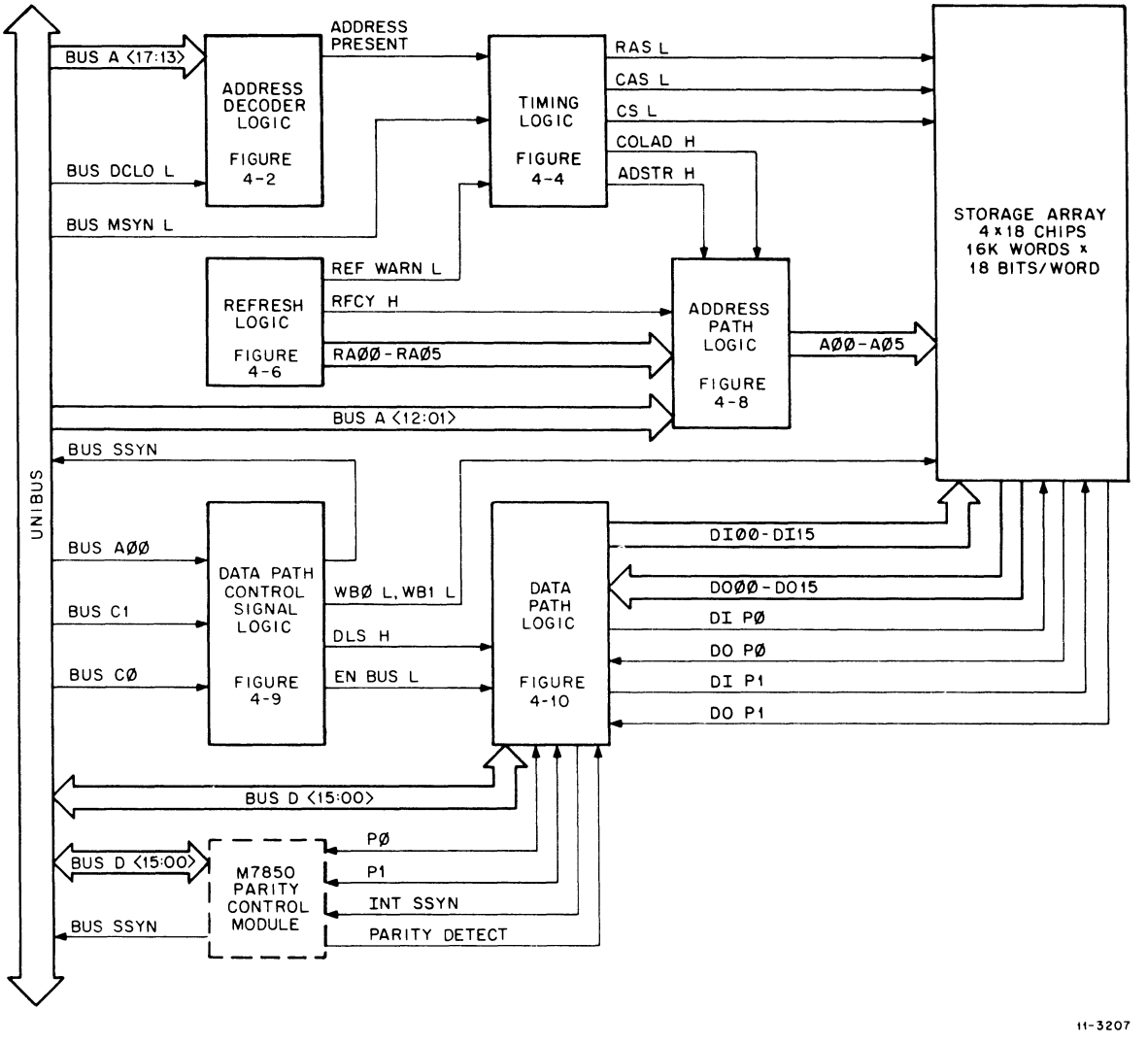


Figure 4-1 MS11 Block Diagram

The Unibus address space assigned to the MS11 depends on how large the memory is, i.e., what its bit capacity is, and what Unibus address is selected as the MS11 starting address. This starting address can be any one that begins a 4K block of addresses; for example, 000000_8 (0K), 040000_8 (8K), 120000_8 (20K), etc. The starting address is assigned by arranging switches E111-A through E111-E (Figure 4-2) so that when this address appears on the BUS A(17:00) lines, the adder network produces five output signals (at point A) that have the binary logic levels 11100. These five signals enable NAND gate E112-A and, because a jumper is in place between W3 and W4, NAND gate E123. If both the Unibus and the MS11 timing logic are not busy, the ADDRESS PRESENT H signal will start the timing chain (Figure 4-4). When the output of E112-A went low, latch E119 generated RSA L, which results in the first row of chips being selected; the ADSTR H timing signal will latch E119 in this state, keeping RSA L asserted until the timing cycle is completed. Data can be transferred to or from the memory location specified by the starting address. All addresses in the 4K block that begins with the starting address are identical in bits BUS A13L - BUS A17L; consequently, all addresses in this 4K block cause ADDRESS PRESENT H and RSA L to be asserted.

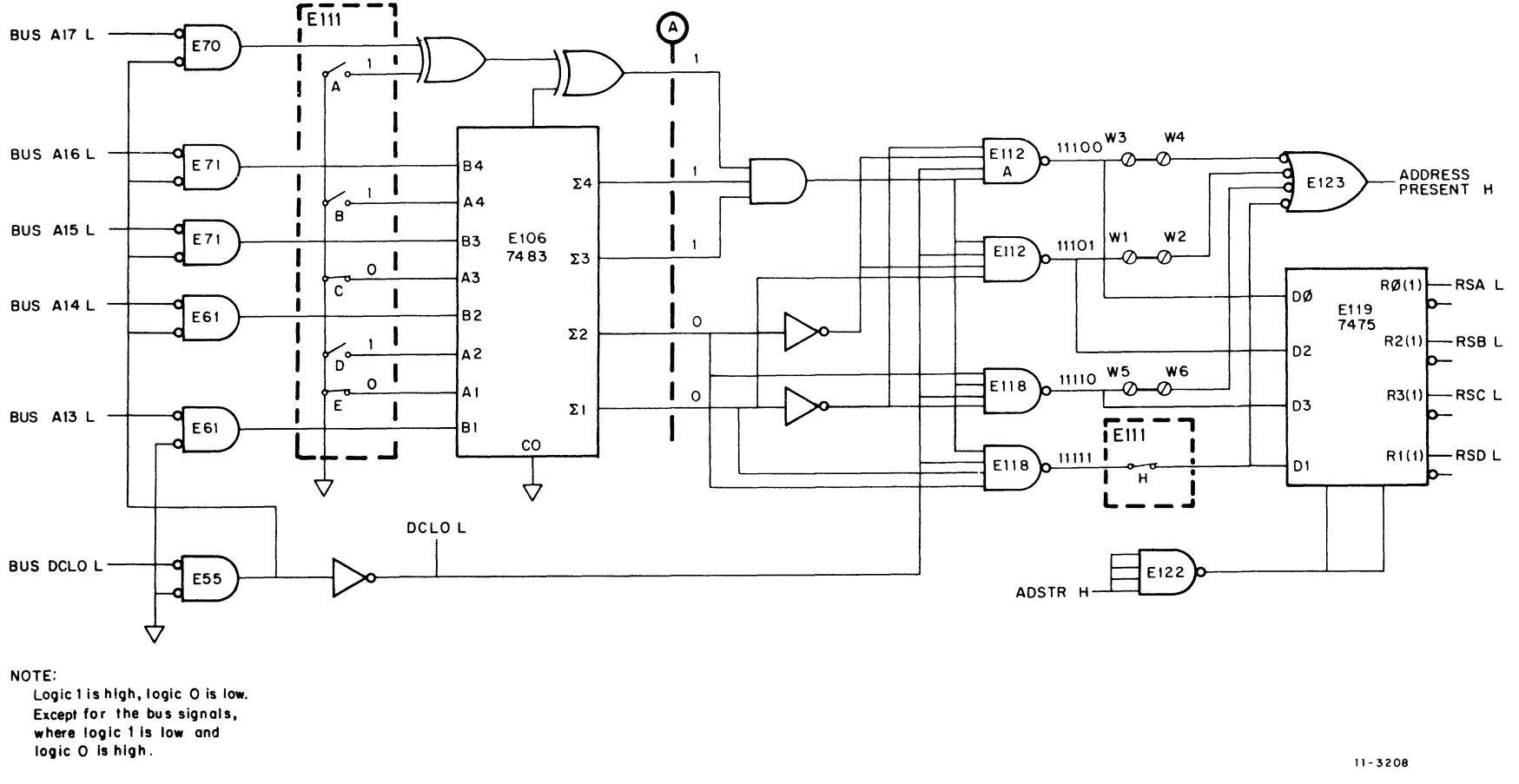


Figure 4-2 Address Decoding Logic

If the MS11 in question has a word capacity of 8K, i.e., two rows of memory chips are installed on the module, all addresses in the next higher 4K block of Unibus addresses will also be assigned to the MS11. When any one of the addresses in this 4K block appears on the BUS A(17:00) lines, the adder network produces an output represented by 11101_2. The RSB L signal is asserted, selecting the second row of chips. A jumper is connected between W1 and W2; thus, ADDRESS PRESENT H is asserted and data can be transferred to or from a memory location in the second bank of chips.

A third and fourth row of memory chips can be added to the MS11, increasing its word capacity to as much as 16K. Additional Unibus address space is assigned by adding a jumper between W5 and W6 for the third row of chips and closing switch E111-H for the fourth row. Table 4-1 relates the memory size, the adder output signal binary representation, and the jumper/switch E111-H arrangement. Appendix A lists the required switch settings for E111-A through E111-E for all of the 31 possible MS11 starting addresses.

Table 4-1
Address Space Assignment

MS11 Capacity	Required Adder Output	Eyelet Pairs Connected by Jumpers
4K	11100	W3-W4
8K	11101	W3-W4, W1-W2
12K	11110	W3-W4, W1-W2, W5-W6
16K	11111	W3-W4, W1-W2, W5-W6 (switch E111-H closed)

A specific example will promote further understanding. Consider the MS11-J, a 16K memory. Four 4K blocks of Unibus address space can be assigned to the MS11-J. The lowest 4K block is assigned by selecting a starting address, e.g., 040000_8 (8K). Switches E111-A - E111-E are set so that the adder output is 11100_2 when address 040000_8 appears on the Unibus address lines (Figure 4-2). Any address in the 4K block of addresses beginning with 040000_8 and ending with 057777_8 (i.e., 8K to 12K) will cause ADDRESS PRESENT H to be asserted.

The first address in the next highest 4K block of addresses (12K to 16K) is 060000_8. When this address appears on the Unibus, the output from adder E106 becomes 11101_2. With a jumper connected between W1 and W2, this address, and each address up to and including 077777_8, also causes the ADDRESS PRESENT H signal to be asserted.

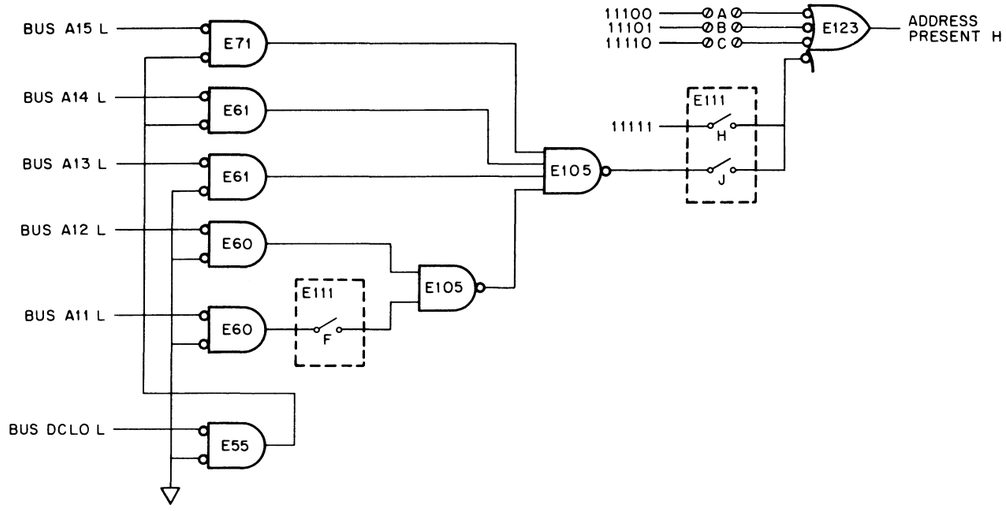
Each succeedingly higher 4K block of addresses causes the adder output to increase by 1_2. Thus, addresses from 16K to 20K result in an adder output of 11110_2, while those from 20K to 24K produce an output of 11111_2. Each address within these blocks can cause the ADDRESS PRESENT H signal to be asserted if the appropriate jumper is connected. (Or if the switch is closed, in the case of the fourth block. This difference is explained shortly.)

The uppermost 4K of Unibus address space is reserved for internal general registers and peripheral devices. A special feature of this memory allows part of this address space to be assigned to the MS11 (in processors without memory management). Figure 4-3 shows part of the Address Decoding logic, modified so that certain addresses in the reserved space can be assigned to the MS11-J Memory. If the memory has been assigned addresses in such a way that the uppermost 4K block of addresses coincides with the reserved area (i.e., when a 16K memory is assigned space from 16K to 32K in a 32K machine), switch E111-H must be placed in the open position.

A small system with few peripherals may not need all of the reserved 4K address space. Switches E111-F and E111-J can be closed selectively to allow the use of the lower 2K or lower 3K addresses of the reserved 4K block. Specifically, when E111-J is closed and E111-F is open, addresses from 28K to 30K (160000_8 - 167777_8) will cause the ADDRESS PRESENT H signal to be asserted. When both E111-J and E111-F are closed, addresses from 28K to 31K (160000_8 - 173777_8) will be assigned to the MS11-J. Appendix A relates the switch settings to the MS11 options and the desired I/O page operations.

NOTE

If a user is considering use of the reserved I/O page of addresses, he should check carefully to ensure that no peripheral devices (including bootstrap ROMs) are assigned any of the reserved addresses.



NOTE:
Logic 1 is HIGH, logic Ø is LOW, except for the bus signals, where logic 1 is LOW and logic Ø is HIGH.

11-3209

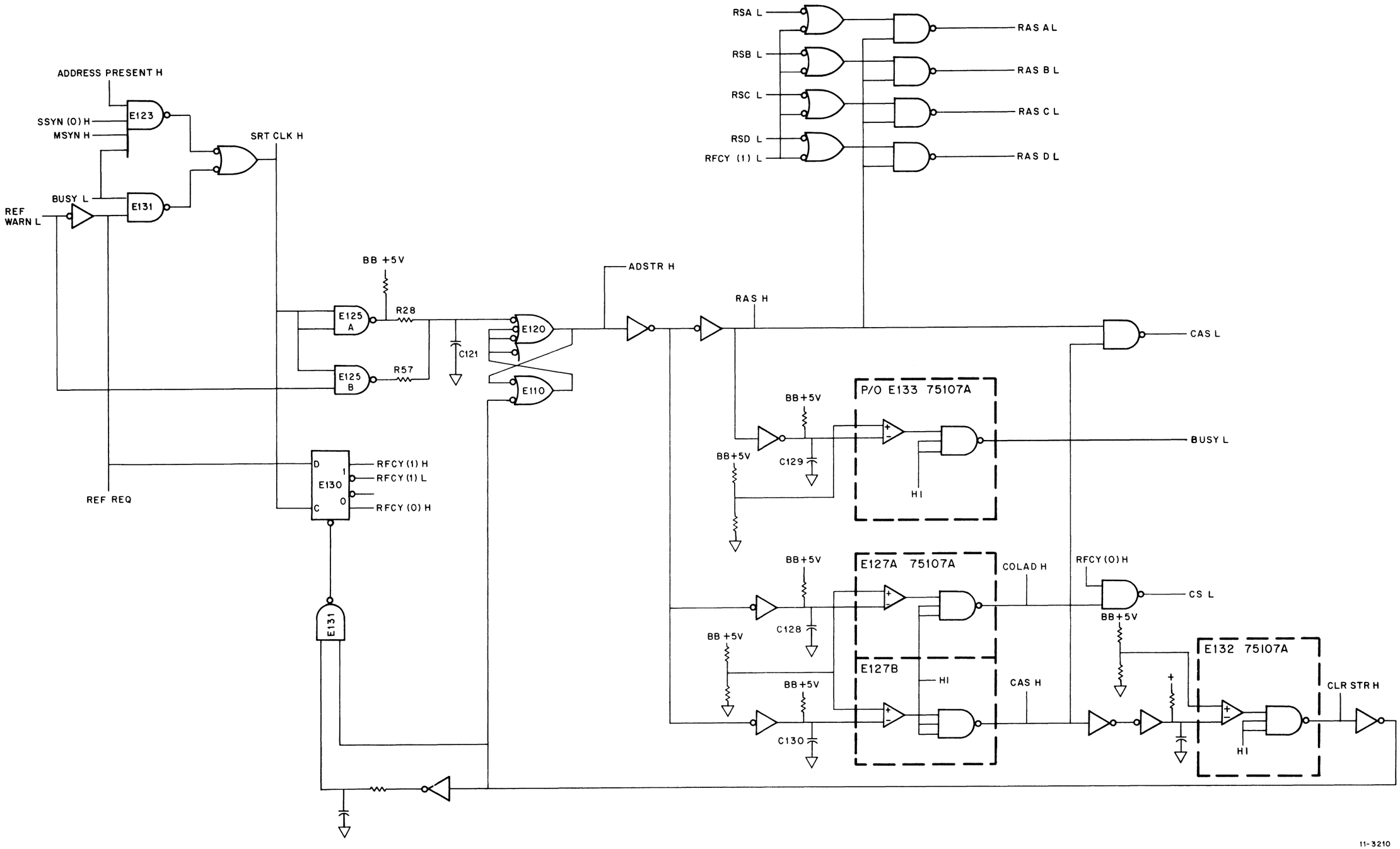
Figure 4-3 Address Decoding, I/O Address Space Logic

4.3 TIMING SIGNAL LOGIC

Three kinds of timing cycles are carried out by the MS11 logic: a bus read cycle, a bus write cycle, and a refresh cycle. Each cycle uses the same basic timing signals to select the addressed memory location. These timing signals are generated by the logic shown in Figure 4-4. Of primary importance are the ADSTR H, COLAD H, and RFCY signals, which are instrumental in gating the address information to the on-chip row and column address latches, and the RAS, CAS L, and CS L signals, which strobe the address information into these address latches.

The timing chain is started when the SRT CLK H signal is generated by either MSYN H, in the case of a bus cycle, or the Refresh logic, in the case of a refresh cycle. A bus cycle is prescribed when the bus master places on the Unibus an address that has been assigned to the MS11. The address information is decoded by the Address Decoding logic, which asserts ADDRESS PRESENT H. When the bus master asserts BUS MSYN, the Timing Signal logic generates SRT CLK H to begin the timing sequence. Every 25 μs, the Refresh logic (Figure 4-6) asserts the REF WARN L signal and attempts to initiate a refresh cycle. If a bus cycle is in progress at the time, the Refresh logic waits until the BUSY L signal is negated, indicating that the bus cycle has just been completed. Then, the Refresh logic asserts the SRT CLK H signal.

Because bus cycles are carried out more often than refresh cycles, the logic is always preconditioned for a bus cycle. When a refresh cycle is initiated, certain logic elements must be changed from their preconditioned state. One of these elements is flip-flop E130 in Figure 4-4. This flip-flop remains in the clear state until the SRT CLK H signal is generated by the Refresh logic; at that time, since REF WARN L is low, the flip-flop is set, asserting the RFCY(1) H signal. The RFCY(1) H signal, along with the COLAD H signal, controls the multiplexers in the Address Path logic (Figure 4-8), selecting either the address specified by the bus master or the address specified by the Refresh logic. Thus, the multiplexers also change from their preconditioned state. To ensure that both flip-flop E130 and the multiplexers have passed through the transient period into their refresh cycle conditions,



11-3210

Figure 4-4 Timing Signal Logic

the beginning of the timing chain is delayed; i.e., the time duration between the respective assertions of SRT CLK H and ADSTR H is longer for a refresh cycle than for a bus cycle. This time delay is introduced between the leading edges of the two signals by the integrating capacitor, C121. At the start of a bus cycle (the REF WARN L signal is negated) the SRT CLK H signal enables NAND gate E125-B and C121 can discharge rapidly to ground through a very small resistance (R57 is an 18-ohm resistor). However, at the start of a refresh cycle, REF WARN L is asserted; consequently, E125-B remains disabled and C121 must discharge through the added resistance of R28 (560 ohms), increasing the delay time before ADSTR H is asserted.

The timing signals are illustrated in Figures 4-5 and 4-7. Figure 4-5 is oriented to a bus cycle and is the basis for the remaining discussion in this section. Figure 4-7 is oriented to a refresh cycle and is the basis for the discussion in Section 4.4. The timing diagrams have the same time scales so that the common signals can be compared, and each diagram relates the appropriate address signals and the multiplexer outputs to the timing signals.

When ADSTR H is asserted, it gates the address information from the multiplexer outputs onto the A00–A05 lines. It also clocks latch E119. One output of E119 is latched low, indicating which 4K block of addresses contains the decoded address. When the RAS H signal goes high after ADSTR H, only the bank of chips that corresponds to the selected 4K block of addresses will receive the RAS signal. This selectivity reduces the overall system power dissipation, since chips that receive no RAS signal do not cycle internally and thus use less power.

The RAS signal strobes the information on the A00–A05 lines into the on-chip row address latches of the selected bank of chips. After the chip row address hold time requirement has been met, the information on the A00–A05 lines can be changed to reflect the column address. Thus, the COLAD H signal is asserted after a sufficient delay has been introduced by the integrating capacitor C128 and its associated circuit components. One of these components is half of a 75107A Dual-Line Receiver, which is being used as a level comparator. When the voltage at the non-inverting input is greater than that at the inverting input, the output is low; this is the condition that exists before the ADSTR H signal is asserted. Shortly after ADSTR H goes high, the voltage at the inverting input of E127-A begins to rise. About 100 ns later, when it has risen to a value greater than the reference voltage at the non-inverting input, the COLAD H signal is asserted.

When COLAD H goes high, the address multiplexers in the Address Path logic select the column address information; this information is placed on the A00–A05 lines and later strobed into the on-chip column address latches by the CAS signal. CAS is sent to all chips in the array. Chips that receive a CAS but no RAS will have their outputs go into a high-impedance state.

The last signal in the timing chain to go active is the CLR STR H signal. This signal not only resets the timing chain by clearing the cross-coupled flip-flop (E120/E110) but also causes NAND gate E131 to generate a pulse sufficiently wide to clear flip-flop E130, thus conditioning it for a subsequent bus cycle (the flip-flop is cleared at the end of each and every timing cycle).

The end of the timing cycle is signalled when BUSY L is negated. Unlike the other capacitor-controlled delay circuits in the timing diagram, the circuit including C129 is concerned with the trailing edge of the signal. Thus, the trailing edge of BUSY L goes high quite some time after RAS H is negated (approximately 130 ns). This satisfies a chip specification that requires RAS to be high for a minimum of 150 ns at the end of a timing cycle.

4.4 REFRESH LOGIC

The Refresh logic is shown in Figure 4-6; Figure 4-7 relates the significant signals (Figures 4-7 and 4-5 have the same time scales so that common signals can be compared). A refresh timing cycle is initiated every 25 μs when E133 generates the REF CLK L signal. This signal clears flip-flop E135, thereby asserting REF WARN L. If the memory is not busy, the SRT CLK H signal will be asserted, setting flip-flop E130 and starting the timing chain (the SRT CLK H signal might already be high as a result of the Address Decoding logic having recognized an MS11 address; if so, even though BUSY L may still be high, the refresh timing cycle will be delayed until the normal memory cycle has been completed).

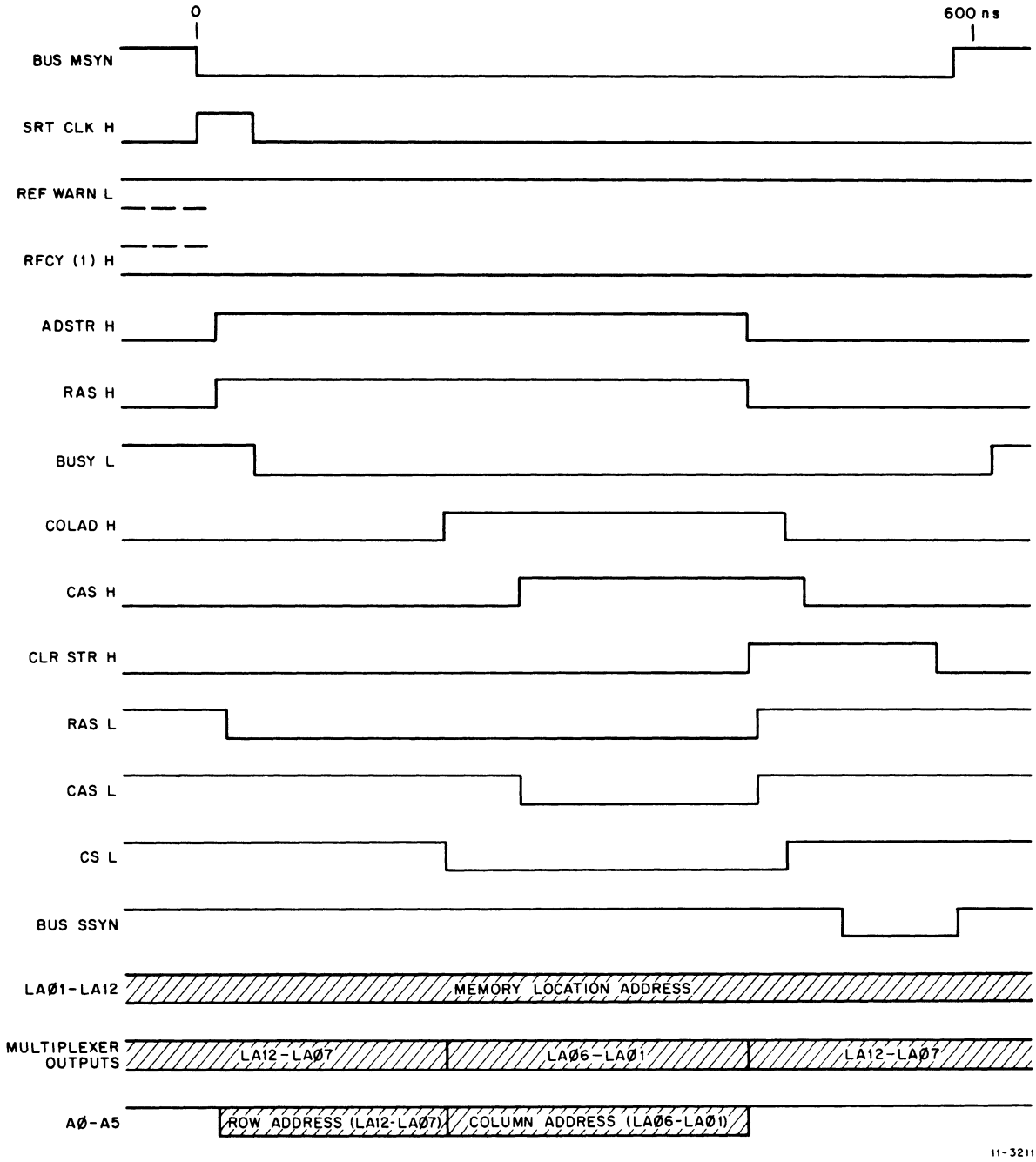


Figure 4-5 Bus Cycle Timing Signals

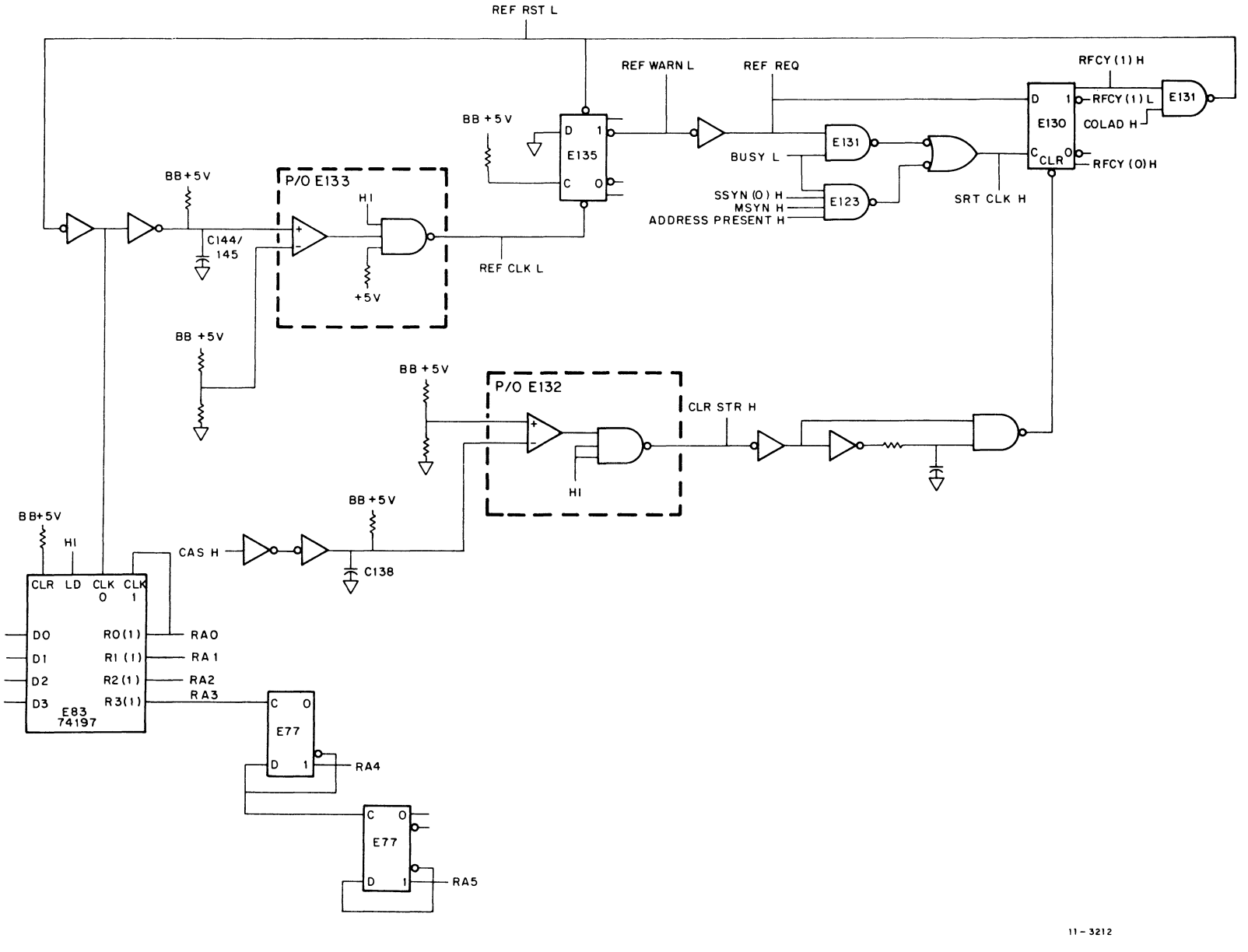


Figure 4-6 Refresh Logic

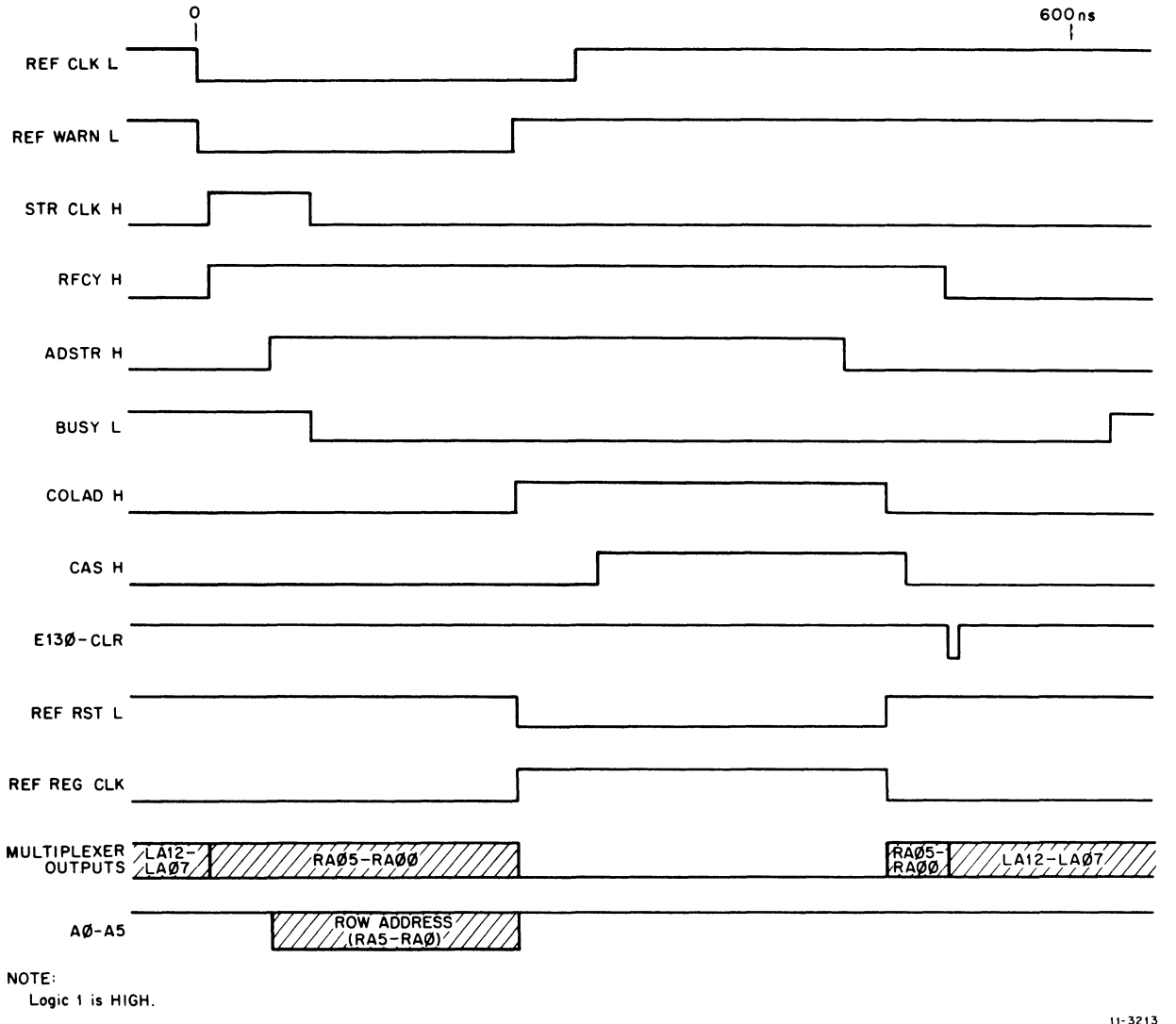


Figure 4-7 Refresh Cycle Timing Signals

The RFCY(1) H signal, generated when flip-flop E130 is set, causes the refresh address bits RA00–RA05 to be placed on the output lines of the multiplexers in the Address Path logic. When the timing chain asserts ADSTR H, after a delay that is long enough to ensure that both the RFCY flip-flop (E130) and the multiplexer output lines have settled, the refresh address is gated onto the A00–A05 lines. The address is then latched into the on-chip row address latch by the RAS signal; all 64 cells located on the addressed row are refreshed. When the timing chain asserts COLAD H, the multiplexer outputs go to ground. The A00–A05 lines go high and are left in this state in preparation for the next memory timing cycle.

The COLAD H signal also resets the REF CLK L signal timer by enabling NAND gate E131, thereby asserting REF RST L. This signal sets flip-flop E135 and causes the timing capacitor, C144/145, to discharge. When the voltage at the non-inverting input of E133 drops below the reference voltage at the inverting input, REF CLK L is negated. When COLAD H later goes low, C144/145 starts charging; in 25 μs, it will have charged to such a potential that E133 again asserts the REF CLK L signal and another refresh timing cycle is initiated. Also, when COLAD H goes low, the 6-stage counter comprising binary counter E83 and flip-flops E77 is clocked. The next consecutive refresh address is placed on the RA00–RA05 lines and the 64 cells located at that row address will be refreshed during the next refresh cycle.

One of the last events to occur during the refresh cycle is the clearing of flip-flop E130, with the resulting negation of RFCY(1) H. Finally, the BUSY L signal is negated to identify the end of the refresh cycle and the availability of the logic for a bus cycle.

4.5 ADDRESS PATH LOGIC

When an address is placed on the Unibus, the Address Decoding logic determines if the address is located within any of the 4K blocks of addresses assigned to the MS11. The specific address within the 4K block is represented by the BUS A1 L - BUS A12 L signals, illustrated in Figure 4-8, the Address Path logic.

The address information is applied to three 7475 latches (E76, E88, and E82). The 1-output of a latch follows the respective input when the latch clock input is high; when the clock input goes low, the state of the D-input at the time of the clock transition is stored on the 1-output.

The address information is applied to the latch D-inputs before the timing cycle is initiated by the SRT CLK H signal, i.e., before ADSTR H is asserted. Hence, the address is placed on the LA01-LA12 lines before the timing signals are generated. At this time, both COLAD H and RFCY(1) H are low; thus, the signals at the A-inputs of the 74S153 multiplexers (LA07-LA12) are gated to the f-outputs. When the ADSTR H signal goes high, shortly after SRT CLK H is asserted, the address is stored on the 1-outputs of the latches, and the multiplexer f-outputs are gated to the A00-A05 lines. These 6 bits represent the row address and are latched into the on-chip row address latch by the RAS signal.

The timing logic next asserts the COLAD H signal. Now, the signals at the B-inputs of the multiplexers (LA01-LA06) are gated through the multiplexers and placed on the A00-A05 lines. These 6 bits represent the column address and are latched into the on-chip column address latch by the CAS signal. Now that the memory location has been selected, data can be read from or written into memory.

The dynamic technique used to store information in the chip single-transistor cells makes periodic refreshing of the stored data necessary. Every 25 μs, a refresh cycle is carried out at one of the 64 row addresses. During this refresh timing cycle, the RFCY(1) H signal is asserted by the Refresh logic. While COLAD H is low, at the beginning of the cycle, the signals at the C-inputs of the multiplexers (RA00-RA05) are gated to the f-outputs; from there, they are gated onto the A00-A05 lines when ADSTR H goes high. This row address is latched into the on-chip row ddress latch by the RAS signal; all 64 cells located on the specified row are refreshed (column addresses do not matter during the refresh cycle).

4.6 DATA PATH LOGIC

The logic shown in Figure 4-9 generates signals that control the flow of read/write data within the MS11 memory. These signals are developed in response to Unibus signals BUS A00 L, BUS C0 L, and BUS C1 L, issued by the bus master. The table in Figure 4-9 lists the possible combinations of BUS C0 L and BUS C1 L and the type of transfer specified by each combination. Related to these entries are, first, the 7475 latch (E115) outputs and, second, the control signals that gate data to and from the memory chips. These control signals are applied to the logic shown in Figure 4-10, the Data Path logic, which is illustrated only for data bit 15.

In Figure 4-10 four chips are shown, one for each possible bank of chips. For example: A 4K memory would have a row of 16 or 18 chips installed on the module, chip E97 being the left-most chip in the row; a 12K memory would have three rows of chips installed, chips E97, E96, and E95 being the left-most in their respective rows. All chips are provided with the same address and control lines, except for the Row Address Strobe lines, which are different for each bank of chips; those chips that receive no RAS input do not cycle internally. All chips that comprise the upper byte of the data word (i.e., bits 15 - 08, and parity bit P1) are supplied with the WB1 L signal, while the lower byte chips are supplied with the WB0 L signal.

If a DATO operation is to be performed, the bus master places the memory address, the data, and the control bits (BUS C0 L and BUS C1 L) on the Unibus (Figure 4-11 shows the timing of a DATO operation). The Data Path Control Signal logic asserts the DLS H signal near the beginning of the cycle; later in the cycle it asserts the WB0 L and WB1 L signals. DLS H clocks the data from the BUS D15 line into hex flip-flop E36; then WB1 L and CAS L jointly strobe the data from the DI15 line into the chip selected by the RAS X L signal (the WB0 L signal clocks bus data into the chips of the lower byte of the data word).

Shortly after DLS H is asserted, flip-flop E135 (Figure 4-9) is set, asserting both SSYN(0) H and INT SSYN L. If the memory is equipped for parity operation, the INT SSYN L signal causes the Parity Control Module to assert BUS SSYN L (this module grounds the PARITY DETECT L line to prevent the MS11 from generating BUS SSYN L). If the memory is not so equipped, BUS SSYN L is asserted by bus driver E35.

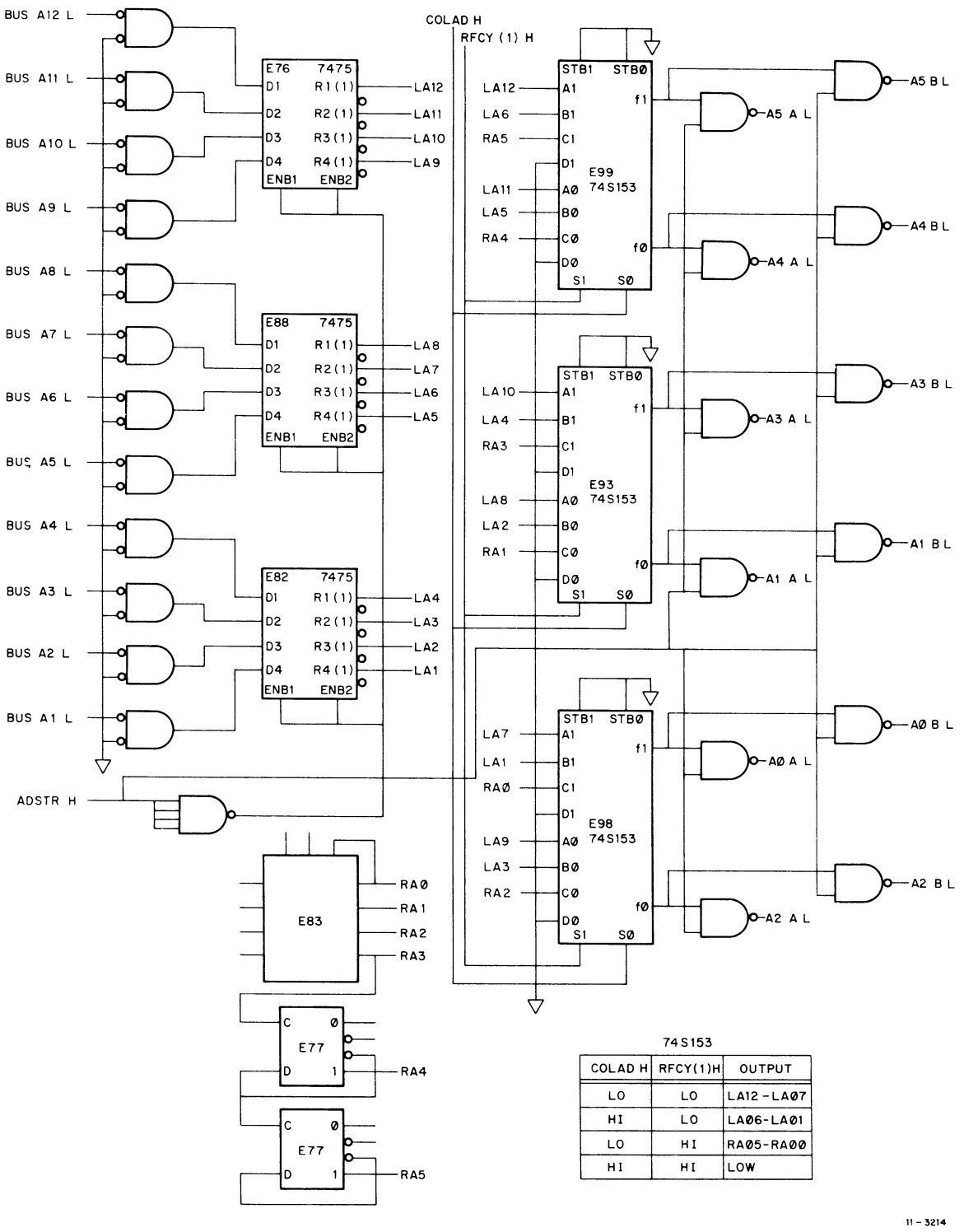
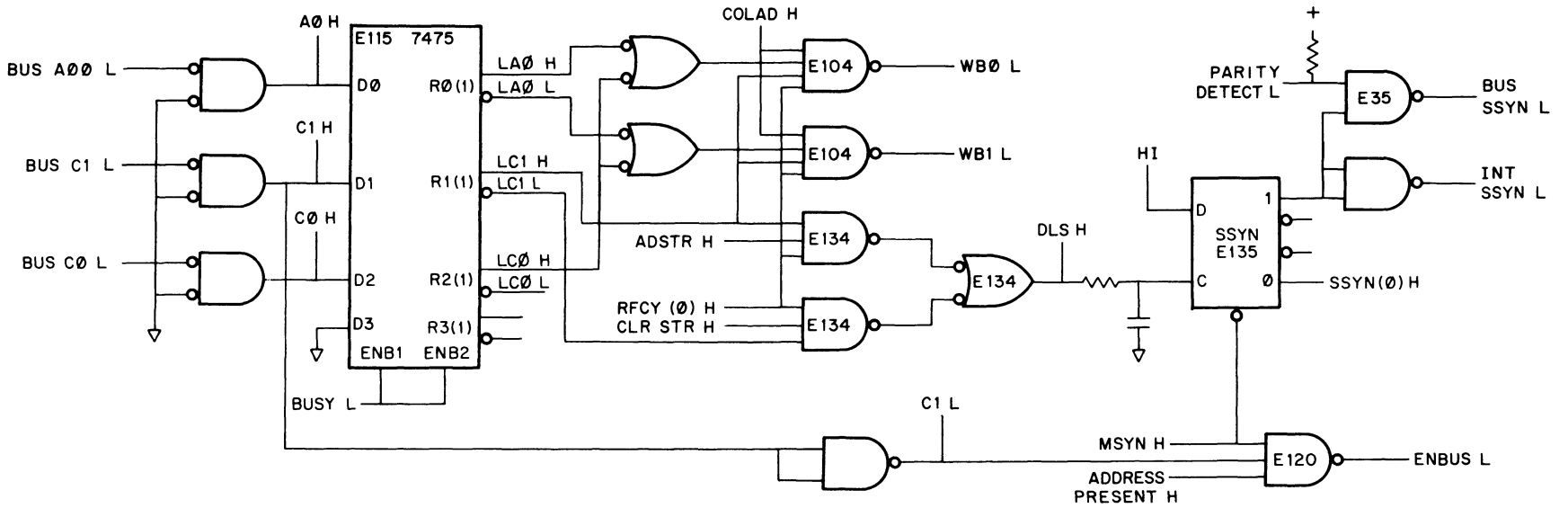


Figure 4-8 Address Path Logic



BUS C1	BUS C0	TRANSFER DIRECTION	LA0 H	LA0 L	LC1 H	LC1 L	LC0 H	LC0 L	CONTROL SIGNAL
HI	HI	DATA WORD FROM SLAVE TO MASTER (DATI)	–	–	LO	HI	LO	HI	ENBUS L DLS H
HI	LO	DATA WORD FROM SLAVE TO MASTER, FOLLOWED BY DATO OR DATOB TO SAME LOCATION (DATIP)	–	–	LO	HI	HI	LO	ENBUS L DLS H
LO	HI	DATA WORD FROM MASTER TO SLAVE (DATO)	–	–	HI	LO	LO	HI	WB1 L, WB0 L DLS H
LO	LO	DATA BYTE FROM MASTER TO SLAVE (DATOB); DATA TRANSFERRED ON D<15:08> WHEN BUS A00 IS LO ON D<07:00> WHEN BUS A00 IS HI	HI	LO	HI	LO	HI	LO	WB1 L DLS H
			LO	HI					WB0 L DLS H

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Figure 4-9 Data Path Control Signal Logic

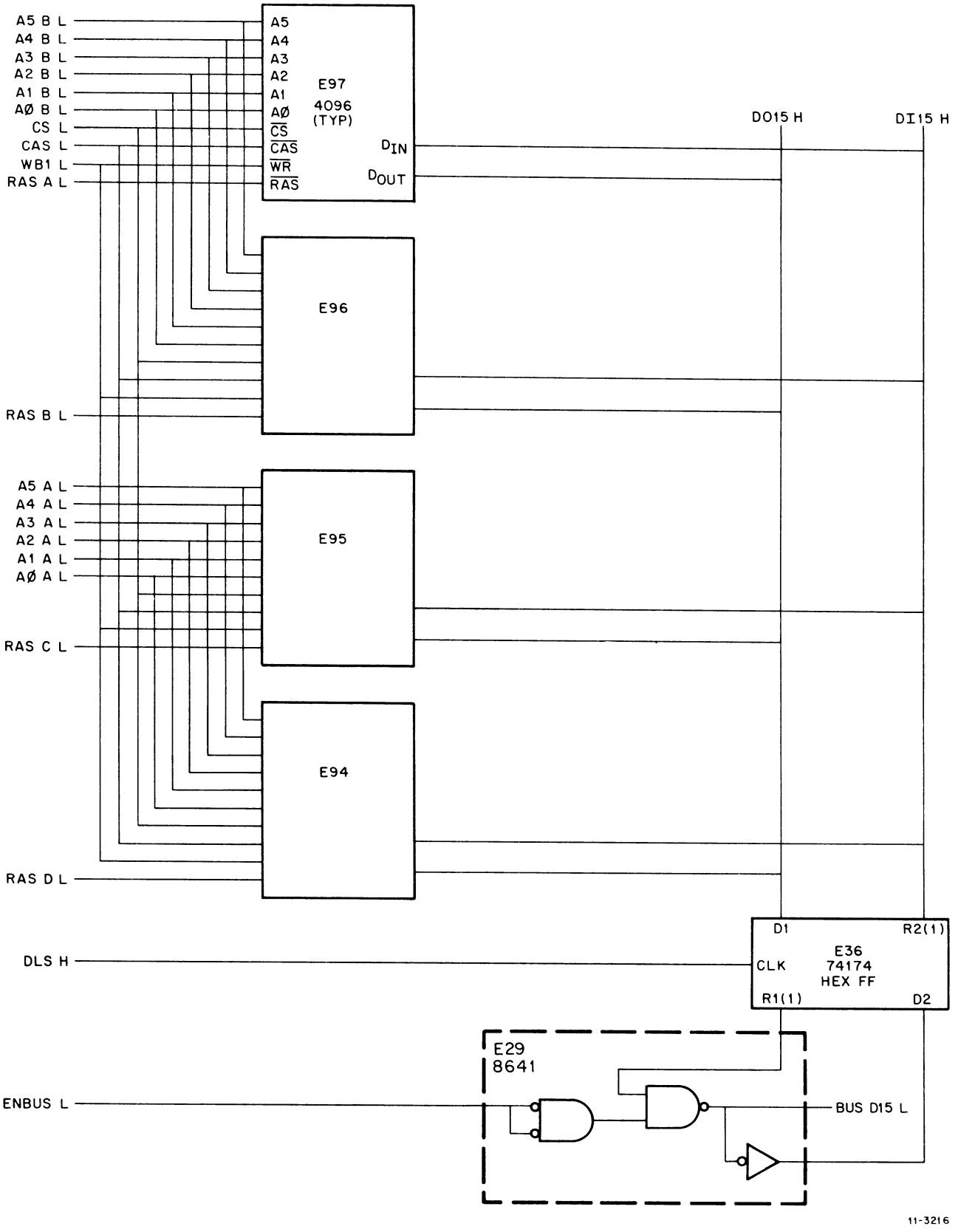


Figure 4-10 Data Path Logic [Bit D(15)]

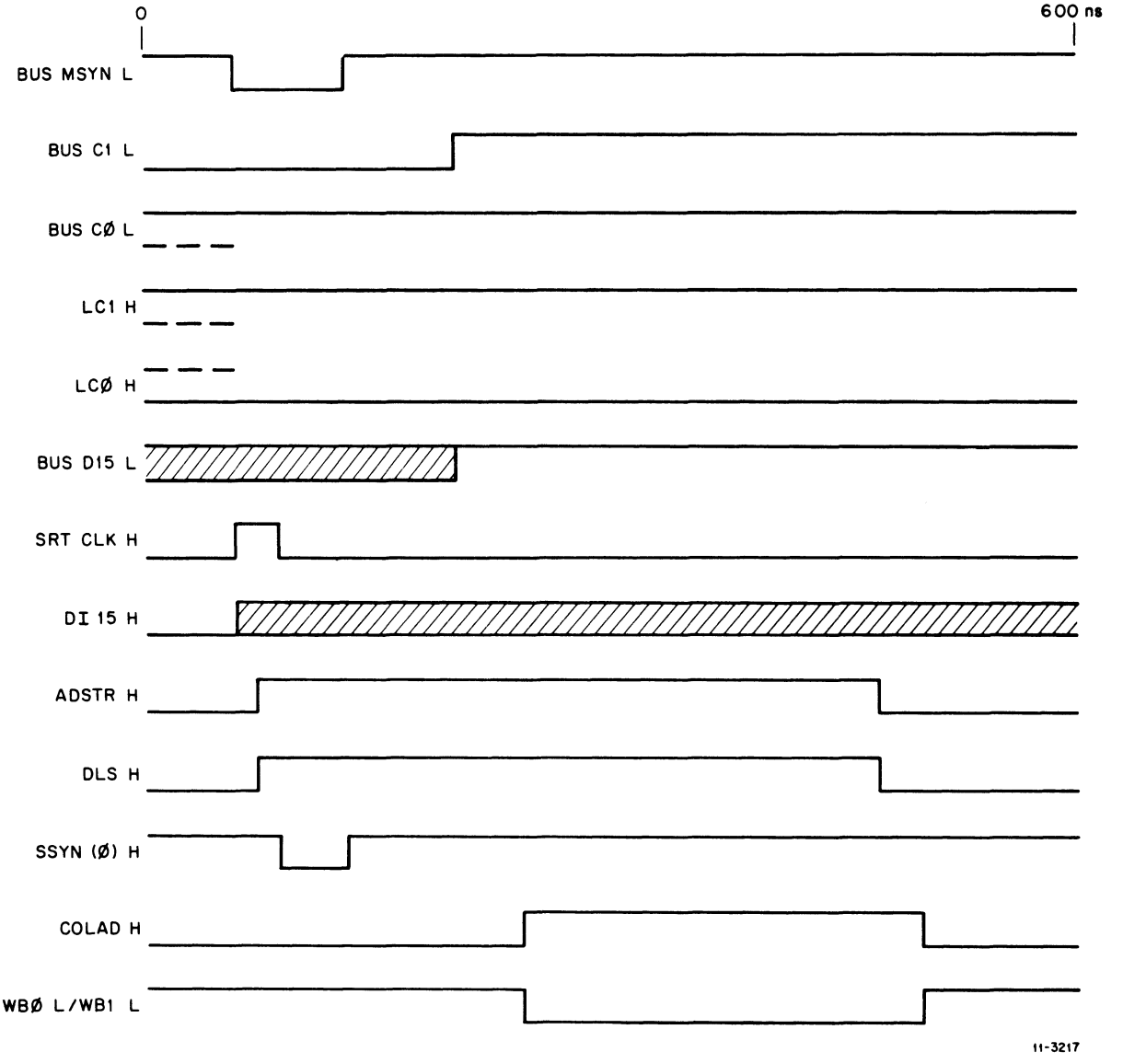


Figure 4-11 Data Write Timing (DATO

The Data Path logic functions the same way for a DATOB operation if the BUS A00 L signal is asserted by the bus master. In this situation, a data byte is transferred on the BUS D (15:08) lines, WB1 L is generated, and the data is strobed into the upper-byte chips. If BUS A00 L is not asserted, only WB0 L is generated and data is strobed into the lower-byte chips.

Figure 4-12 shows the timing for either a DATI or a DATIP operation; the two are treated identically by the memory. The DLS H signal again clocks flip-flop E36, in this instance loading the information on the DO15 line into the flip-flop. The ENBUS L signal, generated near the start of the bus cycle, gates the data from the flip-flop output onto the BUS D15 line.

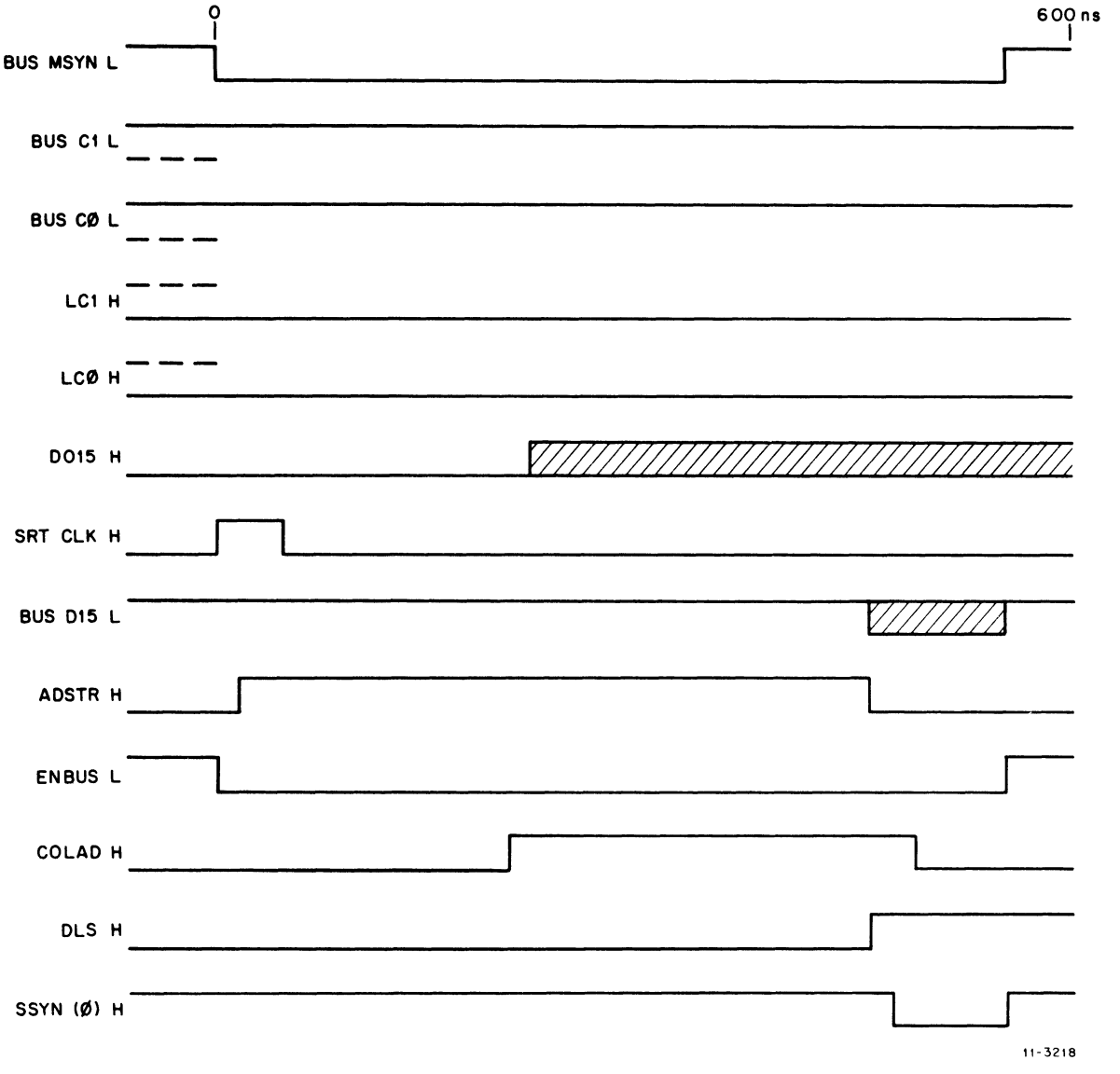


Figure 4-12 Data Read Timing (DATI)

CHAPTER 5
TROUBLESHOOTING HINTS

5.1 GENERAL

The information in this chapter is designed to supplement the technician's knowledge of the MS11 by suggesting possible courses of action for troubleshooting the memory. These suggestions are based on the assumption that the system fault has been traced to the memory module by some means, e.g., module swapping or system troubleshooting procedures.

If the diagnostic program can be loaded and executed, the problem will generally be solved. However, it might not be possible to load the diagnostic; or, the diagnostic might not execute correctly after being loaded. This chapter deals with these two problems by providing troubleshooting hints of two broad classes: those dealing with faults that prevent the diagnostic from being loaded, and those dealing with faults that prevent the diagnostic from being executed. The first class of faults is covered in Section 5.2, the second is discussed in Section 5.3.

5.2 DIAGNOSTIC LOADING PROBLEMS

5.2.1 BUS SSYN L Not Asserted

When the operator tries to load the diagnostic program, the memory should respond by asserting the BUS SSYN L signal. A trap in the program indicates when BUS SSYN L is not returned by the memory.

In order for the MS11 to generate BUS SSYN L, the Address Decoding logic (Figure 4-4) must be working. Set the address selection switches (E111A-E111E) for a starting address of 000000_8, and halt the processor. Use a scope to check the following signals at the input of the Timing Signal logic (NAND gate E123).

Signal	Expected Logic Level
ADDRESS PRESENT H	HIGH
MSYN H	LOW
SSYN (0) H	HIGH

The state of the ADDRESS PRESENT H signal will show if the memory address has been decoded; the other two signals relate to the state of the SSYN flip-flop in the Data Path Control Signal logic (Figure 4-9). If any of these signals do not have the expected logic level, follow the lead suggested until the fault is found.

If these signals are good, check the Timing Signal logic. Even though the processor is not running, the Timing Signal logic is generating signals during the periodic refresh cycles. The SRT CLK H signal is asserted about every 25 μs to begin such a cycle (Figure 4-7, Refresh Cycle Timing Signals).

If the problem cannot be traced to either of these two groups of logic, devise some method of checking the condition of the BUS MSYN bus receiver, the SSYN flip-flop logic, and NAND gate E123 (Figure 4-4), which is enabled at the start of a bus cycle.

5.2.2 BUS SSYN L Asserted

If the memory issues BUS SSYN when addressed but the diagnostic cannot be loaded, five areas are suspect: refresh circuits, data circuits, address circuits, write logic, and loader memory locations.

5.2.2.1 Refresh Circuits - Check the Refresh logic (Figure 4-6). Ensure that the refresh cycles are occurring every 24 μs. Scope the outputs of the refresh counter (E83 and E77, Figure 4-6); the counter outputs should look like the waveforms illustrated in Figure 5-1.

5.2.2.2 Data Circuits - The simple tests described in this section will check the MS11 data in/out paths. Use memory location 000000_8. Deposit and examine all 1s, then deposit and examine all 0s. If unexpected results occur, follow up on the symptoms.

Again, use memory location 000000_8. Check for shorts by depositing and examining, successively, the following data words: 000001, 000002, 000004, 000010, 000020, 000040, 000100, 000200, 000400, 001000, 002000, 004000, 010000, 020000, 040000, 100000.

5.2.2.3 Address Circuits - The simple test described in this section will check the MS11 address circuits

Step 1 Deposit data word 000000 in the following locations: 000000, 000002, 000004, 000010, 000020, 000040, 000100, 000200, 000400, 001000, 002000, 004000, 010000, 020000.

Step 2 Deposit 777777 in location 000000.

Step 3 Examine location 000002; the data should be 000000, as deposited in Step 1. If the data is 777777, the current address bit is stuck low or high, or shorted to a previous address bit.

Step 4 Deposit 777777 in location 000002.

Step 5 Examine location 000004; the data should be 000000, as deposited in Step 1. If the data is 777777, the current address bit is stuck low or high, or shorted to a previous address bit.

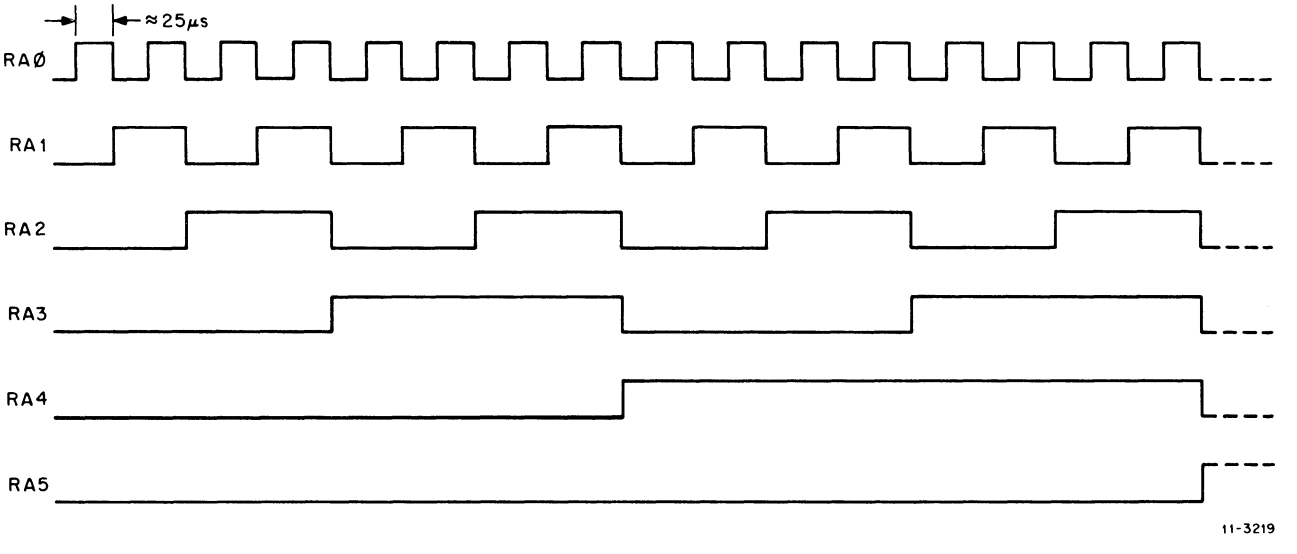


Figure 5-1 Refresh Counter Timing

Step 6 Carry on the sequence begun in Step 2. That is: deposit 777777 in one of the memory locations listed in Step 1 (000004 is next); then, examine the next location to make sure that the data in that location is still 000000.

5.2.2.4 Write Logic - To check the write logic, toggle in the routine listed below, beginning at location 000100. Scope the circuit illustrated in Figure 4-9 between the C0 L, C1 L, and A0 L bus receivers and the WB1 L/WB0 L signals.

```
012700      MOV #1, %0
000001
005001      CLR %1
110110  A:  MOVB %1, (0)
010111      MOVB %1, (1)
000765      BR A
```

5.2.2.5 Loader Memory Space - Load the program listed below. This routine verifies that all bits can hold a 0 or a 1, and that writing into any address does not affect the contents of any other address. It does not check for bit-to-bit shorts within a word; that test was done by Section 5.2.2.3.

The test carried out loops continuously until a failure occurs. It can be made to halt at the end of a pass by changing location 74 to 0. A pass takes about one second. When the test halts because of a failure, R2 holds the failing address and R3 holds the bad data. If the test halts with the PC=50, R4 has the good data; if it halts with the PC=62, R5 has the good data.

	Location	Contents
10*	012700	MOV#(Low) R0
12	000076**	
14	012701	MOV#(High+2) R1
16	020000**	
20	005004	CLR R4
22	005005	CLR R5
24	005105	COM R5
26	010002	A: MOV R0, R2
30	010422	B: MOV R4, (R2)+
32	020201	CMP R2, R1
34	001375	BNE B:
36	010002	MOV R0, R2
40	011203	C: MOV (R2), R3
42	020304	CMP R3, R4
44	001401	BEQ D
46	000000	HALT
50	010512	D: MOV R5, (R2)
52	011203	MOV (R2), R3
54	020305	CMP R3, R5
56	001401	BEQ E
60	000000	HALT
62	005722	E: TST (R2)+
64	020201	CMP R2, R1
66	001364	BNE C
70	005104	F: COM R4
72	005105	COM R5
74	000754	BR A

* If the general registers can be loaded from the console, load them as follows (locations 10 - 24 need not be loaded); then load the rest of the program beginning at location 26.

R0 - Lowest test address (generally 000076)
R1 - Highest test address plus 2 (020000 for 4K of memory)
R4 - 0s
R5 - 1s

**Location 12 contains the lowest address to be tested; location 16 contains the highest address to be tested (plus 2).

5.3 DIAGNOSTIC EXECUTION PROBLEMS

If the diagnostic program cannot be executed as directed by the program documentation, the refresh circuits may not be working, or a portion of the array may be faulty. Check the refresh circuits first (refer to Paragraph 5.2.2.1). If the Refresh logic appears to be operating correctly, use the following procedure to check on the array (the memory capacity must be 8K or greater).

The program loader is stored in the upper 4K of memory, while the diagnostic is stored in the lower 4K (assume an 8K memory). If either bank of chips is suspected of being faulty, that bank can be removed from the circuit. For example, the upper 4K can be removed by disconnecting the jumper at location W1-W4. Then, both the program loader and the diagnostic will be loaded into the lower 4K. If the diagnostic executes correctly, the upper 4K was indeed faulty and can be examined more closely. To remove the lower 4K from the circuit, set the address selection switches, E111-A - E111-E, for 11101; then remove the jumper at location W3-W4. This, in effect, moves the upper 4K down so that it becomes the lower 4K. Both the diagnostic and the loader will be placed in the new lower 4K. If the diagnostic executes correctly, the original lower 4K was faulty.

The same technique can be used for 12K and 16K memories. To remove the highest 4K, disconnect the jumper at location W5-W6 (12K memory) or open switch E111-H (16K memory); to remove the lowest 4K, set 11101 and disconnect jumper W3-W4.

APPENDIX A
MS11 SWITCH SETTINGS

Table A-1 first lists the 31 addresses that can be assigned as the starting address on the MS11 module. Listed next is the number of Unibus addresses below the MS11 starting address; e.g., there are 8096 (8K) Unibus addresses below starting address 040000_8. Finally, the third column lists the switch settings that will produce the desired address assignment. The MS11 ending address is automatically determined by the starting address and the memory size. Table A-2 shows how switches H, J, and F must be arranged for normal operation and when I/O page space is assigned to the MS11.

Table A-1
Switch Settings for MS11 Starting Addresses

MS11 Starting Address (Octal)	Unibus Addresses Below Starting Address	Switch Selection (Switch OFF = Logic 1)				
		A	B	C	D	E
000000	0K	1	1	1	0	0
020000	4K	1	1	0	1	1
040000	8K	1	1	0	1	0
060000	12K	1	1	0	0	1
100000	16K	1	1	0	0	0
120000	20K	1	0	1	1	1
140000	24K	1	0	1	1	0
160000	28K	1	0	1	0	1
200000	32K	1	0	1	0	0
220000	36K	1	0	0	1	1
240000	40K	1	0	0	1	0
260000	44K	1	0	0	0	1
300000	48K	1	0	0	0	0
320000	52K	0	1	1	1	1
340000	56K	0	1	1	1	0
360000	60K	0	1	1	0	1
400000	64K	0	1	1	0	0
420000	68K	0	1	0	1	1
440000	72K	0	1	0	1	0
460000	76K	0	1	0	0	1
500000	80K	0	1	0	0	0
520000	84K	0	0	1	1	1
540000	88K	0	0	1	1	0
560000	92K	0	0	1	0	1
600000	96K	0	0	1	0	0
620000	100K	0	0	0	1	1
640000	104K	0	0	0	1	0
660000	108K	0	0	0	0	1
700000	112K	0	0	0	0	0
720000	116K	1	1	1	1	1
740000	120K	1	1	1	1	0

NOTE
Switch contacts are open when switch is in OFF position

Table A-2
Switch Settings for I/O Page Operation
Memory Size Determination

Memory Option	Switch		
	F	H	J
MS11-E/EP, MS11-F/FP, MS11-H/HP	OFF	OFF	OFF
MS11-J/JP, Normal Use	OFF	ON	OFF
MS11-J/JP, Lower 2K of I/O page assigned to memory*	OFF	OFF	ON
MS11-J/JP, Lower 3K of I/O page assigned to memory*	ON	OFF	ON

*Set switches A through E for a starting address of 100000_8.

NOTE
Switch contacts are open when switch is in OFF position.

APPENDIX B
IC DESCRIPTIONS

This appendix contains descriptions of several integrated circuits used in the MS11 logic. Only those ICs of an unusual nature are described; the more common types, i.e., NAND gates, inverters, flip-flops, etc..., should be familiar to the reader.

7475 4-BIT BISTABLE LATCH

The 7475 is a 4-bit bistable latch. Information present at the data input (D) of a latch is transferred to the 1 output when the clock input (C) goes high. If the C input remains high, the 1 output follows the D input. When the C input goes low, the 1 output holds the state it was in prior to the transition. The logic diagram, a truth table, and a pin locator are shown in Figure B-1.

7483 Binary Full-Adder

The 7483 is a 4-bit binary full-adder used for parallel-add/serial-carry applications. It adds two 4-bit binary numbers (A and B) and provides a sum (S) output for each bit. The resultant carry (CARRY OUT) is taken from the last bit of each adder. The logic diagram and a pin locator are shown in Figure B-2.

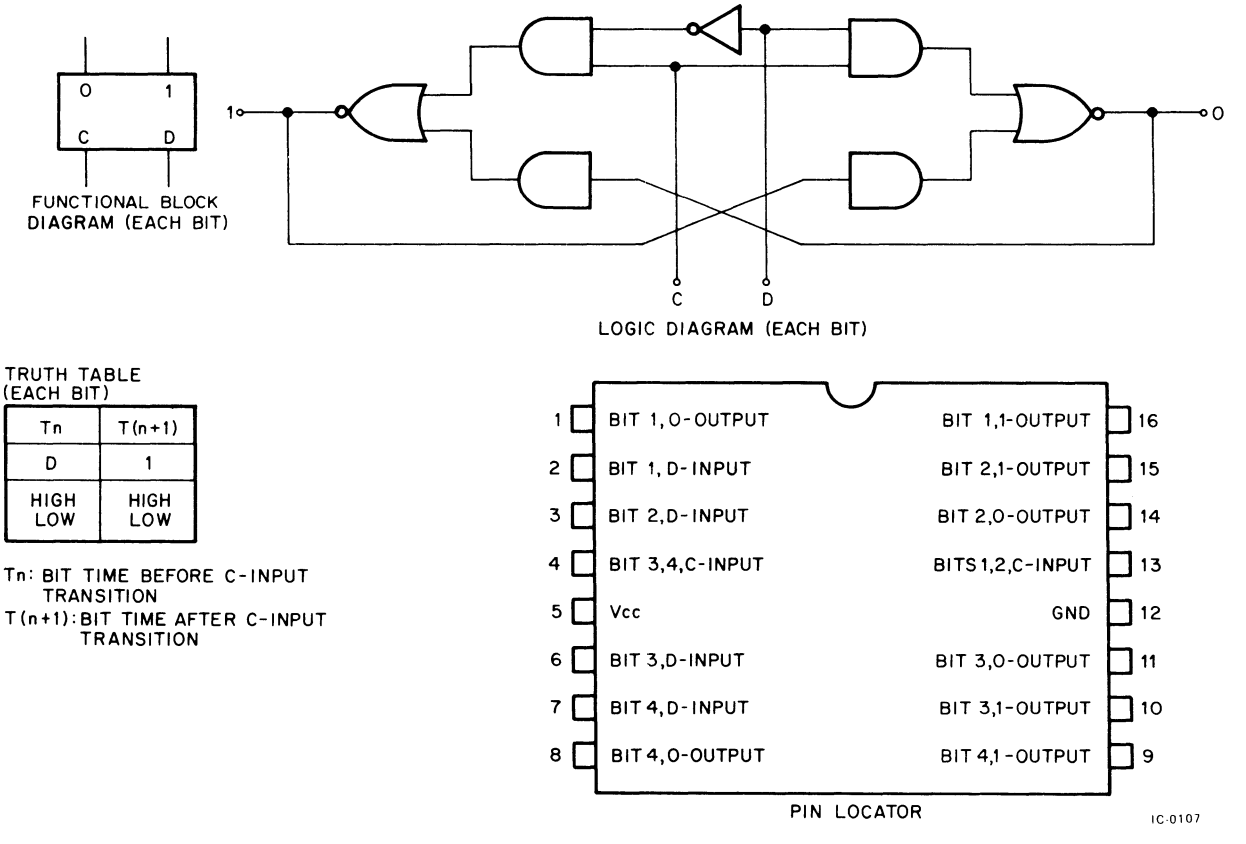
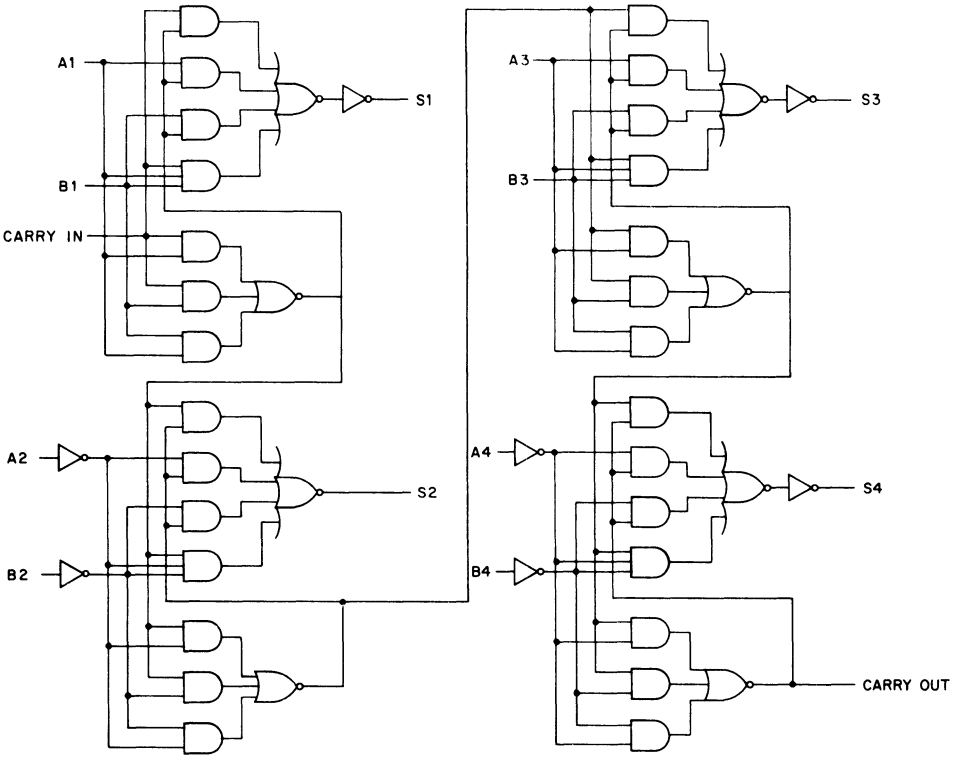


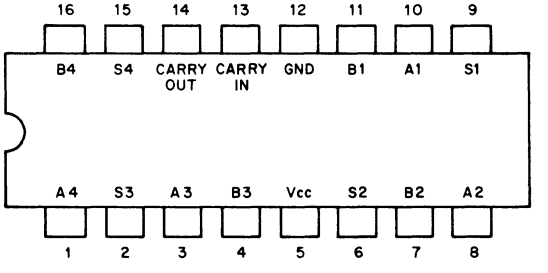
Figure B-1 7475 4-Bit Bistable Latch



INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 0$		
					WHEN $C_0 = 0$			WHEN $C_0 = 0$	
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

LOGIC DIAGRAM



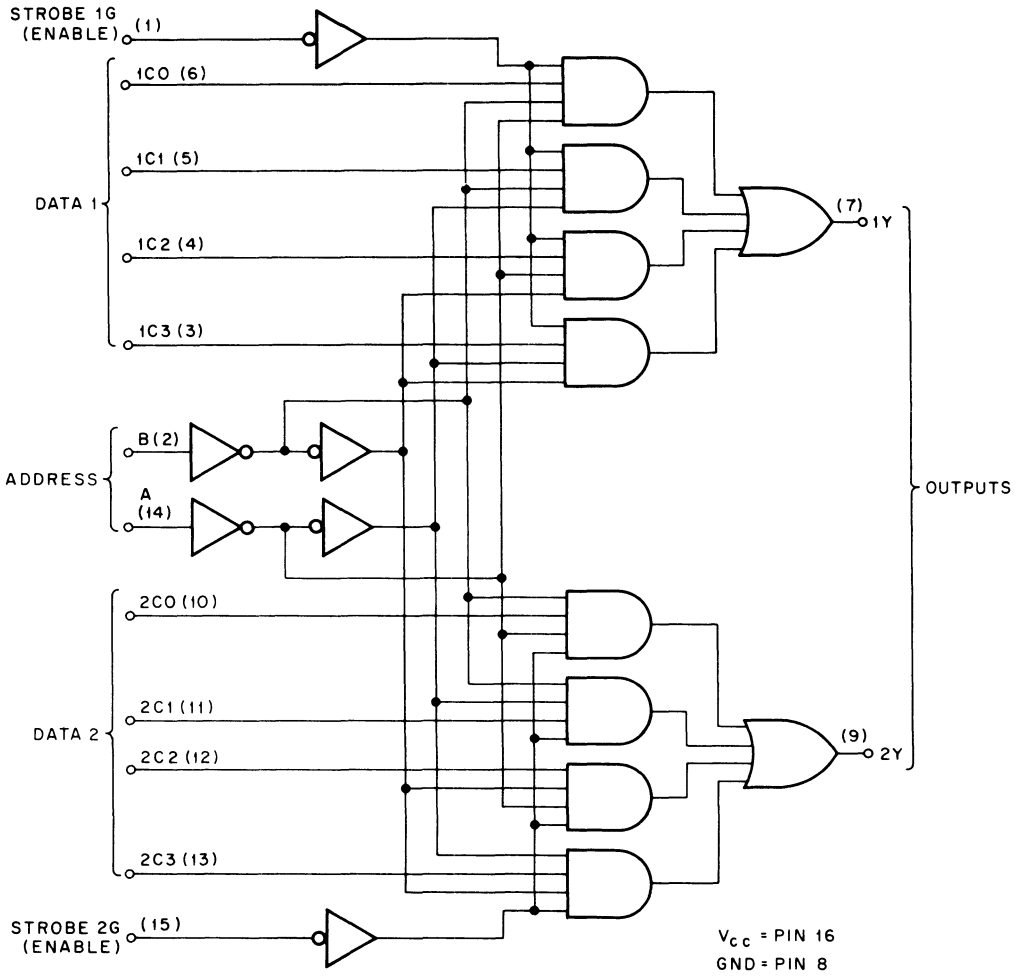
PIN LOCATOR
(TOP VIEW OF IC)

IC 0093

Figure B-2 7483 Binary Full Adder

74S153 Data Selector/Multiplexer

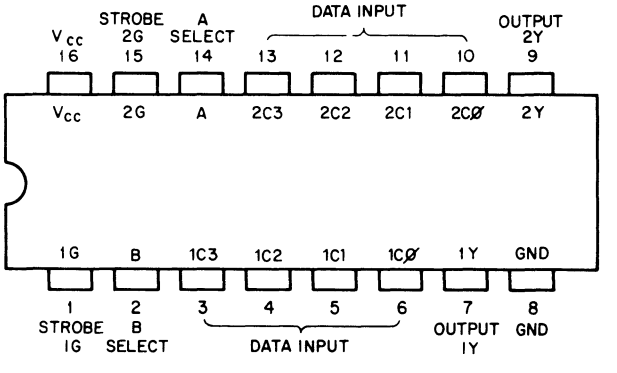
The 74S153 is a dual, 4-bit data selector/multiplexer that provides a single output for each input section. The logic diagram, a truth table, and a pin locator are shown in Figure B-3.



LOGIC DIAGRAM

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



IC 0096

Figure B-3 74S153 Data Selector/Multiplexer

74197 PRESETTABLE BINARY COUNTER

The 74197 is a presettable binary counter that can also be used as a latch. The IC consists of four dc-coupled, master/slave flip-flops connected to provide a divide-by-two counter and a divide-by-eight counter. The logic diagram, a truth table, and a pin locator are shown in Figure B-4.

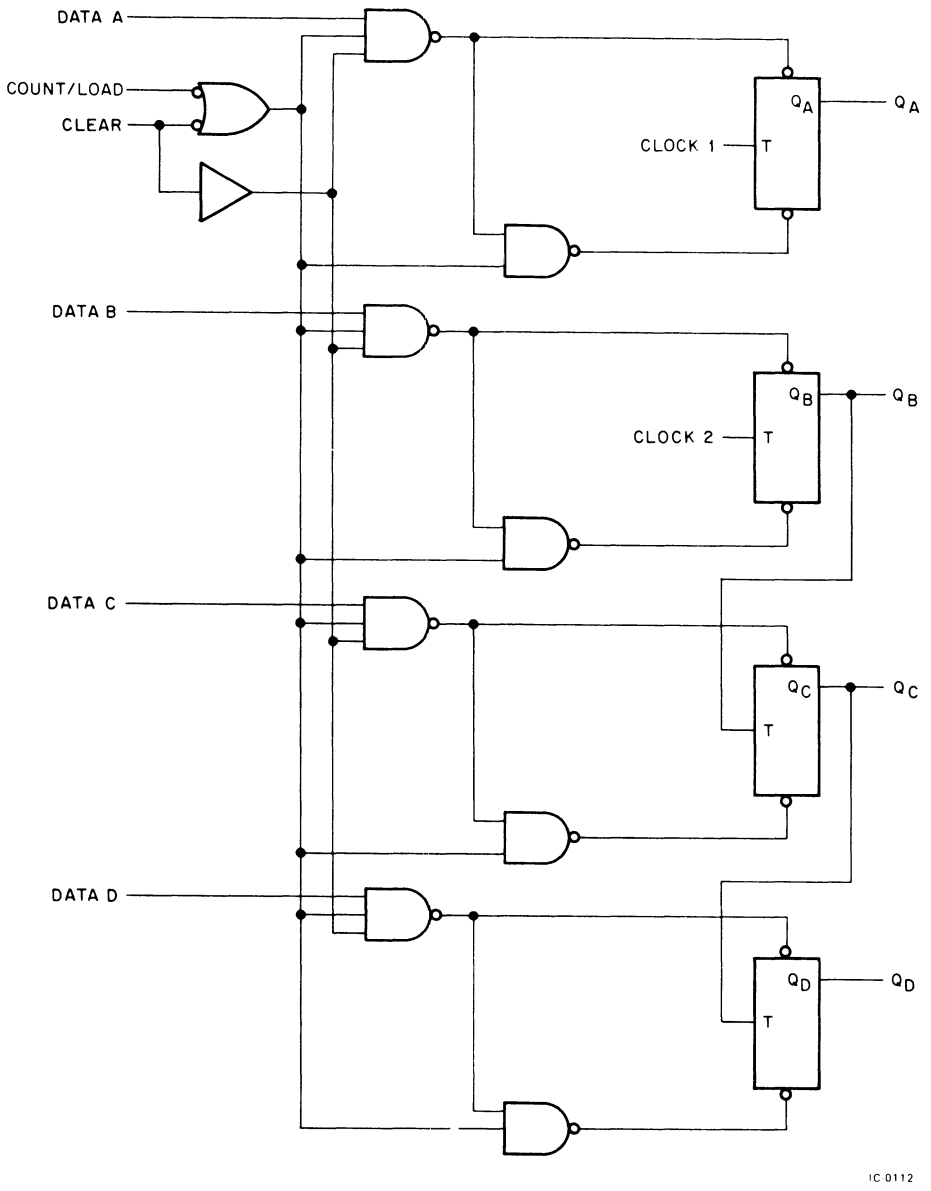


Figure B-4 74197 Logic Diagram (Sheet 1 of 2)

TRUTH TABLE

COUNT	OUTPUT			
CLOCK 1 INPUT	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Q_A connected to CLOCK 2 input.

PIN LOCATOR

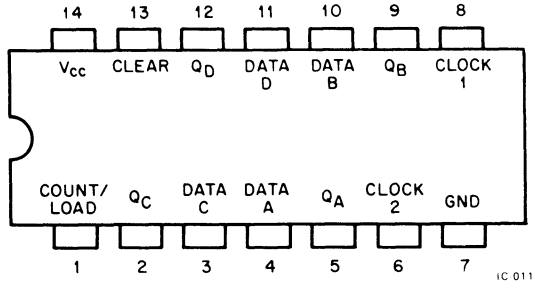


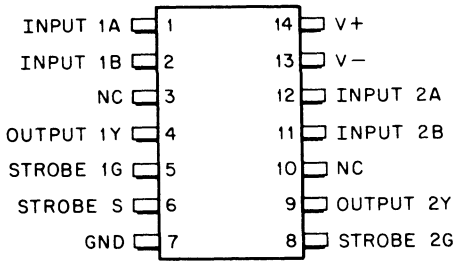
Figure B-4 74197 Truth Table and Pin Locator (Sheet 2 of 2)

The 74197 can be used in any one of three modes: the divide-by-two/divide-by-eight mode (requiring no external interconnection of IC pins), the latch mode, and the binary counter mode. Only the binary counter mode is used in the MS11. Pin 5 must be externally connected to pin 6. The clock input is applied at pin 8. The initial count can be preset to any value by placing a low on pin 1 and entering the data on pins 4, 10, 3, and 11. When pin 13 is a taken low, all outputs are set low, regardless of the state of the clock inputs.

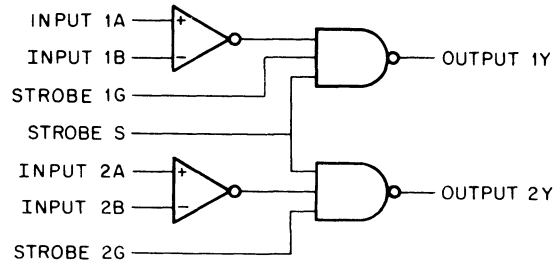
75107A Dual Line Receiver

The 75107A is a high-speed, two-channel line receiver with common voltage supply and ground terminals. It is designed to detect input signals of 25 mV amplitude, or greater, and convert the polarity of the signal into appropriate TTL-compatible output logic levels. An outline drawing of the chip, giving pin connections, a logic diagram, and a truth table as are shown in Figure B-5.

PIN CONNECTIONS



LOGIC DIAGRAM



TRUTH TABLE

DIFFERENTIAL INPUTS A–B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25mV$	L or H	L or H	H
$-25mV < V_{ID} < 25mV$	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25mV$	L or H	L	H
	L	L or H	H
	H	H	L

NOTE:
V_{ID} represents the voltage at the non-inverting input with respect to the inverting input.

11-3220

Figure B-5 75107A Dual Line Receiver

7812 Voltage Regulator

The 7812 is a 3-terminal, positive voltage regulator. In the MS11, the 7812 uses the +15 Vdc supply as its input and provides a regulated +12 Vdc output, which is used as the chip V_{gg} source.

An outline drawing, locating input and output pins, is shown in Figure B-6. Table B-1 lists some significant electrical characteristics of the IC.

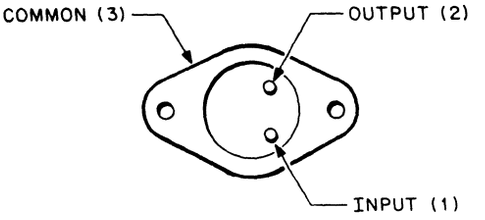


Figure B-6 7812 Outline Drawing (Top View)

Table B-1
7812 Electrical Characteristics

Parameter	Conditions		Min.	Typ.	Max	Units
Output Voltage	Tj = 25° C		11.5	12.0	12.5	V
Line Regulation	Tj = 25° C	14.5 V ≤ V_{IN} ≤ 30 V		10	120	mV
		16 V ≤ V_{IN} ≤ 22 V		3.0	60	mV
Load Regulation	Tj = 25° C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	120	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		4.0	60	mV

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