EK-DHQ11-TM-01

DHQ11
Technical Manual

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of
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PREFACE

The *DHQ11 Technical Manual* provides reference information on physical layout, system configuration, installation and testing, programming characteristics, and maintenance. There is also a glossary of technical terms generally used in DIGITAL technical manuals. The manual is divided into five chapters as follows:

CHAPTER 1 INTRODUCTION. This chapter gives a physical description of the DHQ11, explains how it can be configured, and explains how it interfaces with the system bus and serial data lines.

CHAPTER 2 INSTALLATION. Chapter 2 describes how to install a DHQ11 option, with detailed information on device and vector address selection, backplane positioning, cables and connectors, and testing after installation.

CHAPTER 3 PROGRAMMING. This chapter describes the DHQ11 registers. Some programming examples are also included.

CHAPTER 4 TROUBLESHOOTING. Chapter 4 explains the maintenance strategy, and how to use diagnostic programs to locate a faulty module.

CHAPTER 5 TECHNICAL DESCRIPTION. This chapter gives a technical description of the DHQ11 asynchronous multiplexer. It is assumed that you have some knowledge of Q-bus operations.

APPENDICES. These include additional information on topics discussed in this manual:

APPENDIX A	–	MODEM CONTROL
APPENDIX B	–	FLOATING ADDRESSES
APPENDIX C	–	AUTOMATIC FLOW CONTROL
APPENDIX D	–	GLOSSARY OF TERMS
APPENDIX E	–	DHQ11 BUS CONNECTIONS
APPENDIX F	–	CONTROL CHIP AND OCTART

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This chapter gives an overview of the DHQ11 asynchronous multiplexer, describes the features that it offers, and defines its physical parameters and electrical requirements.

1.2 OVERVIEW

1.2.1 General Description

The DHQ11 option is a serial-line interface which provides eight full-duplex serial data channels on Q-bus systems. The DHQ11 option consists of a single Q-bus module, and one of two groups of cabinet kits, depending on the communication standard supported. The cabinet kits contain the cabinet bulkhead panels and connecting cables.

The main application of the DHQ11 is for interactive terminal handling; it can also be used for data concentration and real-time processing. The DHQ11 register set is compatible with the register set of the DHV11. The main features of the DHQ11 are:

- Eight full-duplex asynchronous data channels
- For transmission: DMA transfers, or program transfers to a 1-character transmit buffer, for each line
- For receive: a 256-entry FIFO buffer for received characters, dataset status changes, and diagnostic information
- It supports EIA-232-D/V.28 or DEC423, with the appropriate cabinet kit.

NOTE

DEC423 is a term used in this manual to indicate a data-leads-only implementation of the RS-423-A electrical standard. DEC423 uses MMJ connectors instead of the 37-way connectors specified by RS-449.

- It is compatible with all DIGITAL DHV11 device drivers
- It can auto-answer on a switched line
- The transmit and receive baud rates for each line can be individually programmed
- It has a total module throughput of 60,000 characters per second, using 8-bit characters, with all channels operating at 38.4 kbaud for both character reception and transmission
- The DHQ11 supports 16-, 18-, or 22-bit addressing, including block-mode data transfer with suitable memories

- The DHQ11 can be programmed to filter XON/XOFF characters from the received data flow
- Self-test and background monitor testing
- Dual-height module, M3107
- Switchpacks for selecting the Q-bus base address and vector address

All other functions are selected by program.

1.2.1.1 Modem Control Facility – All eight channels have sufficient modem control to allow auto-answer dial-up operation over the public switched telephone network using suitable modems, such as DIGITAL's DF124, or Bell models 103, 113, 212. Equivalent modems from other manufacturers can also be used. The DHQ11 is designed to minimize software requirements for modem link control. Appendix A gives further information on modem control. Modem control can be used for driving modems over both public and private lines. Please note that, in some countries, modems must be approved by the PTT for that country for connection to the public network.

1.2.1.2 Self-Test Facility – The DHQ11 incorporates self-test sequencers which operate independently of the host. The result of the self-test is provided to the host system through the receive FIFO buffer. A green LED indicates GO/NO-GO status for the device. More details are given in Section 4.3.

1.2.1.3 Diagnostic Programs – A full range of diagnostic programs is available. These run under the MicroPDP-11 diagnostic supervisor or MicroVAX II maintenance system. Loopback test connectors are not needed when running the user-mode diagnostics. Service-mode diagnostics and loopback connectors are available from DIGITAL.

1.2.1.4 Preventing Data Loss – The DHQ11 can be programmed for automatic XON and XOFF operation, to prevent the loss of data at high throughput. The reporting of received XON/XOFF characters to the software driver can be enabled or disabled.

1.2.2 Physical Description

The DHQ11 is an M3107 dual-height Q-bus module. It is 21.6 cm (8.51 inches) long and 13.2 cm (5.19 inches) wide. Figure 1-1 shows the layout. Connectors A and B are for the Q-bus, while connectors J1 and J2 interface to the communications lines via BC05L-xx cables and distribution panels. Two distribution panels are supplied with an EIA-232-D option, and a single panel is supplied with a DEC423 option. Connector J3 provides power to the active distribution panel supplied with DEC423 options. This connector is not used with EIA-232-D options. Mixed use, that is, one EIA-232-D and one DEC423 panel connected to a single module, is not supported by DIGITAL.

1.2.2.1 On-Board Switchpacks – The DHQ11 has two on-board switchpacks to select the following functions.

- Switchpack E-19 (10-position)

  Switches 2 to 10 select the device address.

- Switchpack E-11 (8-position)

  Switch 1 enables the on-board oscillator. This is a manufacturing test switch, and is closed for normal operation.

Switch 2 selects manufacturing self-test mode. This is a manufacturing test switch, and is open for normal operation.

Switches 3 to 8 select the device vector address.

Chapter 2 gives further information about these switchpacks.

1.2.2.2 Communications Standard – The serial drivers on the M3107 module are compatible with EIA-232-D. However, the CK-DHQ11-W cabinet kits provide level conversion for DEC423.

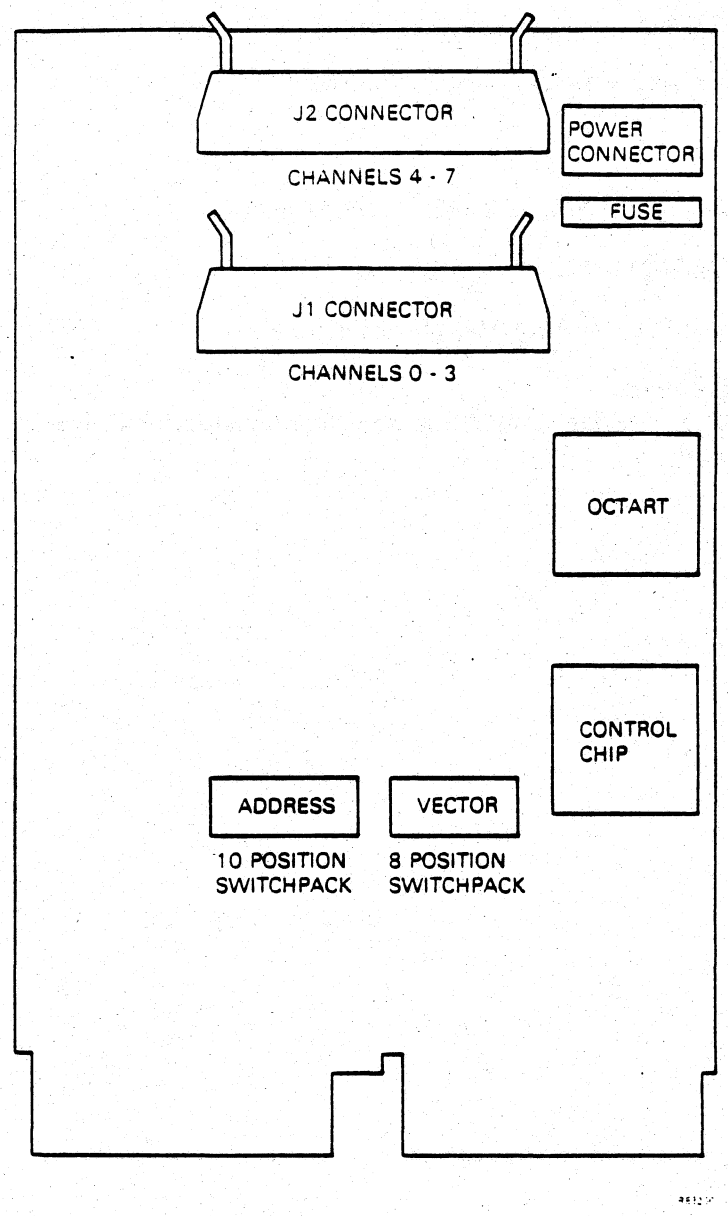

Figure 1-1 Layout of the DHQ11 Module

1.2.3 Versions Of The DHQ11

The DHQ11-M option consists of the M3107 Q-bus module and the *User Guide*. It can be used with one of six cabinet kits. The choice of kit depends on the type of system cabinet, and on whether a EIA-232-D or a DEC423 communication interface is needed.

The cabinet kits available for use with the DHQ11-M are:

EIA-232-D

- CK-DHQ11-AA for BA123 BA11-M boxes
- CK-DHQ11-AB for BA23 boxes
- CK-DHQ11-AF for H9642 cabinets

DEC423

- CK-DHQ11-WA for BA123 BA11-M boxes
- CK-DHQ11-WB for BA23 boxes
- CK-DHQ11-WF for H9642 cabinets

1.2.4 Configurations

The DHQ11 can be used in many different system configurations. Figure 1-2 shows a typical EIA-232-D application.

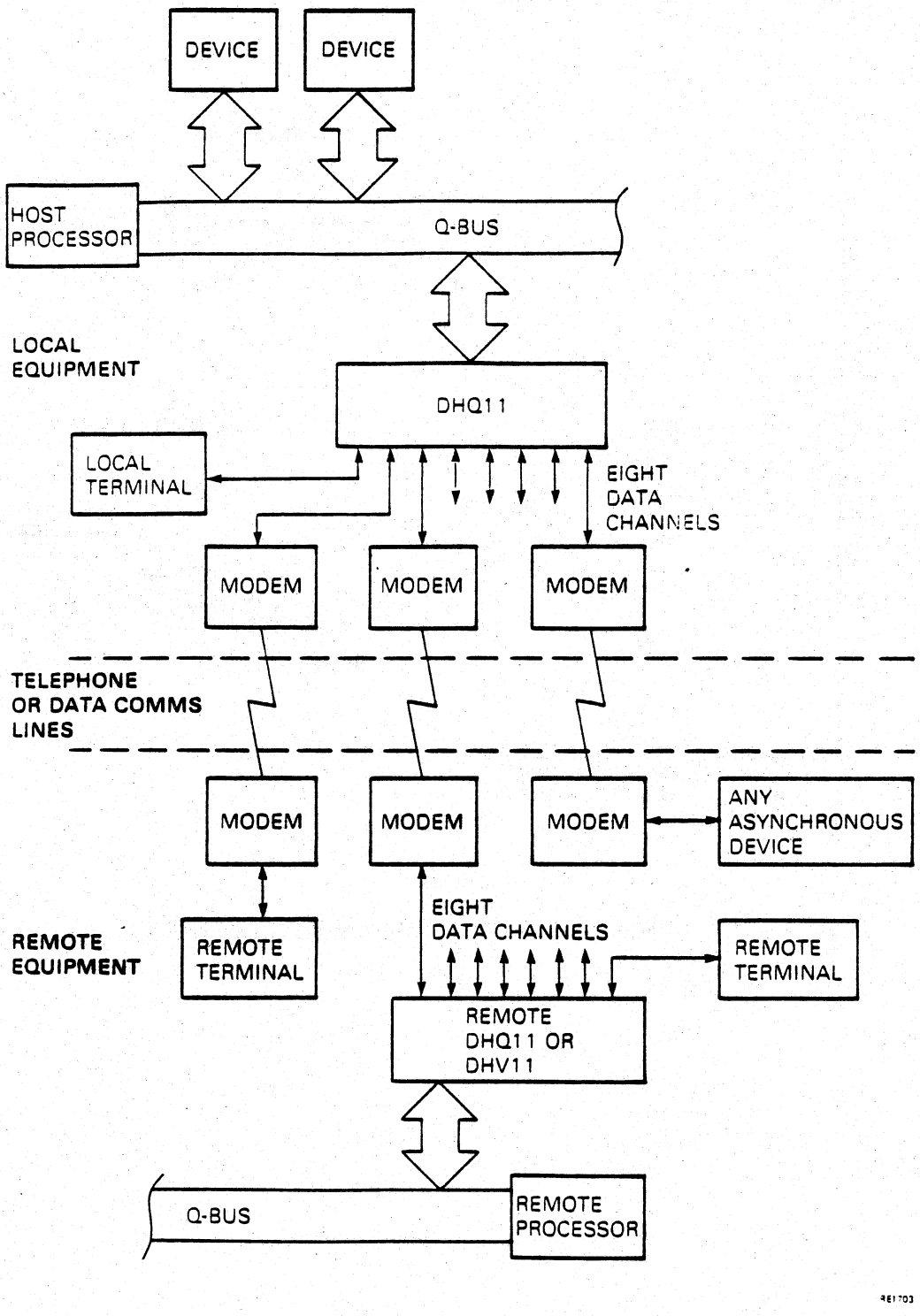

Figure 1-2 Example of a DHQ11 Configuration

1.2.5 Connections

The DHQ11 module is connected directly to the Q-bus by connectors A and B. Figures 1-3 and 1-4 show the interconnections for EIA-232-D and DEC423.

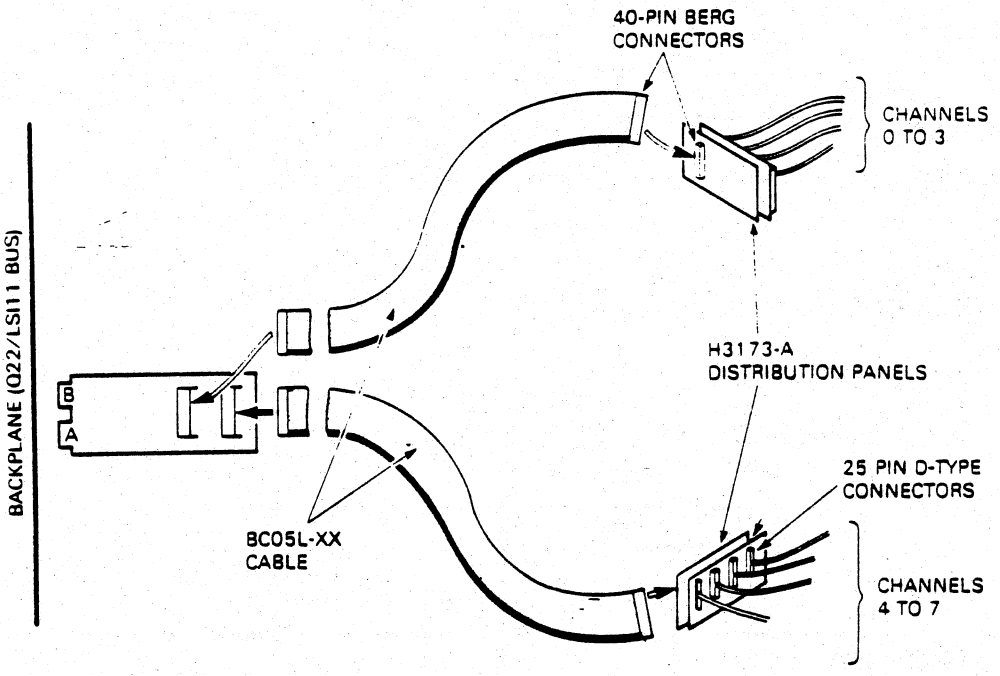

Figure 1-3 DHQ11 Connections (EIA-232-D)

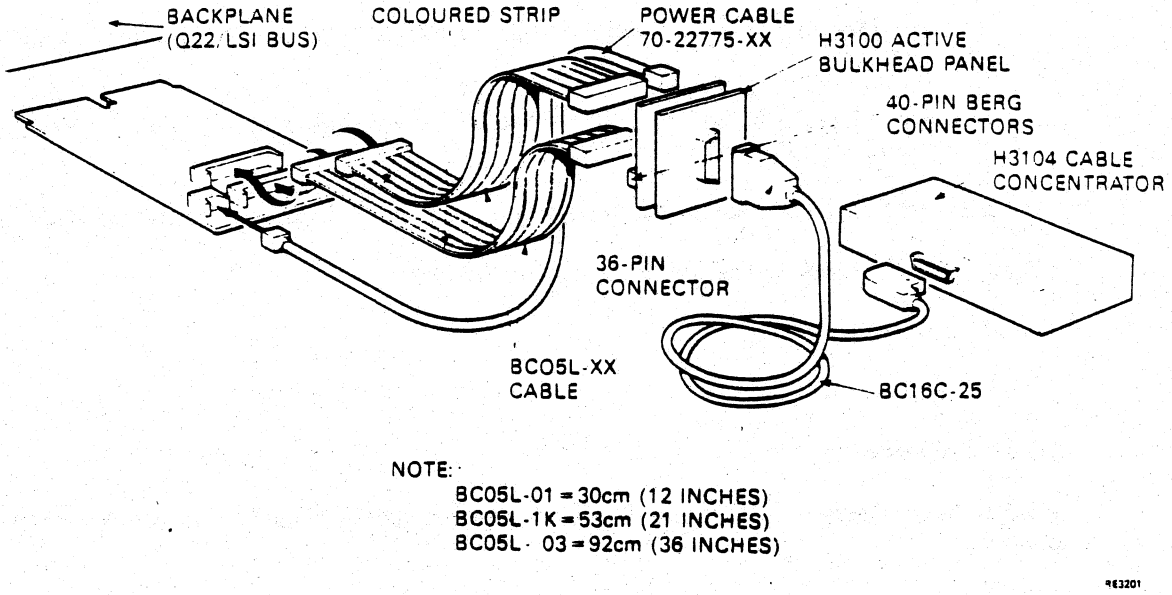

Figure 1-4 DHQ11 Connections (DEC423)

1.3 SPECIFICATION

1.3.1 Environmental Conditions

The following environmental constraints for storage and operation apply to the DHQ11.

- The storage temperature must be within the range 0 degrees C to 66 degrees C (32 degrees F to 151 degrees F).
- The operating temperature must be within the range 5 degrees C to 60 degrees C (41 degrees F to 140 degrees F).
- When operating, the relative humidity must be within the range 10 percent to 95 percent, non-condensing, at a maximum wet-bulb temperature of 32 degrees C and a minimum dew point of 2 degrees C.

DIGITAL normally defines the operating temperature range for a system as 5 degrees C to 50 degrees C (41 degrees F to 122 degrees F); the 10 degrees C difference between the upper limits quoted allows for the temperature gradient within the system box.

The maximum operating temperatures must be derated by 1.8 degrees C/1000 m above sea level (1 degree F/1000 ft) for operation at high-altitude sites.

1.3.2 Electrical Requirements

The DHQ11 needs the following electrical supplies.

- For EIA-232-D options: 5 volts dc plus or minus 5 percent at 1.8 A maximum current, 1.4 A typical
- For DEC423 options: 5 volts dc plus or minus 5 percent at 2.3 A maximum current, 1.9 A typical
- For EIA-232-D and DEC423 options: 12 volts dc plus or minus 5 percent at 380 mA maximum, 300 mA typical

An on-board switched-mode power supply generates a –10 V supply for the serial-line drivers.

1.3.2.1 Q-bus Loads – The loads applied to the Q-bus are:

- 3.2 ac loads
- 0.5 dc loads

1.3.3 Performance

1.3.3.1 Data Rates – Each channel can be separately programmed to operate at one of 16 speeds (in bits/s):

50	1800
75	2000
110	2400
134.5	4800
150	7200
300	9600
600	19200
1200	38400

NOTE

See also Section 1.4.4 (Speed and Distance Considerations).

Chapter 3 contains further information on data rates for EIA-232-D.

1.3.3.2 Throughput – Each channel is capable of full-duplex operation at the maximum data rate. The following maximum throughput is obtainable:

- At 7 bits per character, with 1 start bit, 1 stop bit, and 1 parity bit, the throughput is 61440 characters per second.

- At 5 bits per character, with 1 start bit, 1 stop bit, and no parity, the throughput is 87771 characters per second.

This throughput may be limited by your driver software.

1.4 SERIAL INTERFACES

1.4.1 Interface Standards

The DHQ11 provides modem control signals which conform to EIA/CCITT standard EIA-232-D V.24. The electrical characteristics of the data signal lines conform either to EIA-232-D V.24 or to RS-423-A/V.28, depending on which cabinet kit is fitted. The interface is compatible with X.26 V.10 standards. The slew-rate requirements for RS-423-A V.28 are different from the slew-rate requirements for X.26 V.10.

Connections to external equipment are made via 25-pin male subminiature D-type connectors, as specified for EIA-232-D, or 6-pin MMJ connectors for DEC423.

NOTE

The H3173-A distribution panel does not support separate transmit and receive grounds.

Table 1-1 shows how the signals in EIA-232-D, V.24, and RS-449 are related, and lists the pin connections for male subminiature D-type connectors.

Table 1-1 EIA/CCITT Signal Relationships

Signal Name		D-type Pin	EIA-232-D	Circuit CCITT V.24	Circuit RS-449
Signal Ground	(SIG GND)	7	AB	102	SG
RS-423-A Receive Common		*	RC	102B	
Transmitted Data	(TXD)	2	BA	103	SD
Received Data	(RXD)	3	BB	104	RD
Request To Send	(RTS)	4	CA	105	RS
Clear To Send	(CTS)	5	CB	106	CS

* Not Connected

Table 1-1 EIA/CCITT Signal Relationships (Cont.)

Signal Name		D-type Pin	EIA-232-D	Circuit CCITT V.24	Circuit RS-449
Ring Indicator	(RI)	22	CE	125	IC
Data Set Ready	(DSR)	6	CC	107	DM
Data Terminal Ready	(DTR)	20	CD	108.2	TR
Data Carrier Detect	(DCD)	8	CF	109	RR

1.4.2 Line Receivers

The DHQ11 uses octal serial-line receivers which convert line input signals to TTL levels for the OCTART. Signals are inverted by the receivers.

1.4.3 Line Transmitters

The DHQ11 uses EIA transmitters which convert TTL level signals from the OCTART to line levels on the data lines.

1.4.4 Speed And Distance Considerations

As of December 1985, the Electronics Industries Association (EIA) have replaced the "RS-" identifier for RS-232-C with "EIA". Therefore RS-232-C has been replaced by EIA-232-D. These two standards are compatible with each other. This manual uses EIA-232-D.

The RS-232-C/CCITT V.28 standard was originally designed to specify the connection between a local interface and a modem. It was not intended to be used for connecting to terminals over long distances. The maximum specified cable length is 50 feet (15 metres). Shielded cable must be used in order to meet the requirements of FCC and VDE Radio Frequency Interference (RFI) regulations.

Although cable lengths greater than 50 feet can be used with reasonable success, cable capacitance, noise and ground potential difference restrict the line speed as the distances increase. Consequently, the performance of long-distance communications to a terminal using EIA-232-D often does not meet today's requirements for terminal wiring.

DEC423 is a data-leads-only implementation of the RS-423-A/CCITT V.10 standard. RS-423-A has a different grounding and signal return path arrangement from EIA-232-D.

DEC423 uses line driver and receiver chips which have better filtering and tighter level tolerances than those specified by RS-423-A. In addition, DEC423 devices include transient suppressors for electrical overstress (EOS) and electrostatic discharge (ESD) protection. DEC423 devices may also be connected with unshielded cable.

The features provided by DEC423 devices are reliable data communication over increased distances, typically 1000 feet (300 metres) at 9600 baud. See Table 1-2 for maximum-distance guidelines.

Table 1-2 Maximum Distance Guidelines for DHQ11

	Up to 4.8 Kb	9.6 Kb	19.2 Kb	38.4 Kb
DEC423 to DEC423	1000 ft 300 m	1000 ft 300 m	1000 ft 300 m	500 ft 150 m
DEC423 to EIA-232-D	250 ft 75 m	200 ft 60 m	-	-

The DEC423 standard is for data-leads-only connections to terminal equipment, and is not suitable for connection to modems or other Wide Area Network equipment. The standard also specifies the use of a 6-pin Modified Modular Jack (MMJ) connector, instead of the much larger 37-pin D-type connector used with RS-423-A.

DEC423 is signal-compatible with the EIA-232-D standard when used for data-leads-only interconnection, in that interconnection between devices using the different standards is possible. However, the restrictions on the speed and distance of EIA-232-D will still apply.

DEC423 should always be used in preference to EIA-232-D for direct terminal connection over extended distances.

NOTE

An H3105 active terminal adapter is necessary when using an EIA-232-D terminal with a DEC 423 interface if the longer cable lengths obtainable with DEC423 are required.

The recommended cable for DEC423 is BC16E-XX, which is available with 6-pin MMJ plugs at each end, in lengths up to 100 feet. This cable is also available without MMJ connectors in 1000-foot reels, DIGITAL part number H8220. Unshielded four-twisted-pair cable can also be used. This is available in 1000-foot reels, DIGITAL part number H8245-A.

NOTE

DEC423 to EIA-232-D is intended for local communication. In general, communication devices can become non-operational or be damaged if the total cable length exceeds 300 metres (1000 feet) for DEC423 devices. The cable should not be run outside the building, and the low-voltage data wiring must be separated from ac power wiring. The installation or sites may require additional devices to correct problems in communication.

NOTE

Under ideal conditions, DEC423 devices can drive cables considerably longer than the 1000-foot maximum stated above. However, differences in ground potential, pick-up from mains ac power cabling, and risk of induced interference limit the maximum distance for reliable communications in most practical situations.

1.5 FUNCTIONAL DESCRIPTION

1.5.1 General

The DHQ11 functional blocks are shown in Figure 1-5. Most of the functions are provided by two chips: the control chip and the OCTART chip.

Q-bus buffering uses six DC021 bidirectional buffers. Serial-line interface buffering uses five octal line receivers (5180) and three octal line transmitters (5170), used for data and modem signals.

A 2k × 8 static RAM chip (2018D-45) provides the memory requirements. Switchpacks provide vector address and module address.

1.5.2 Main Functions

The main functions of the DHQ11 are:

- Transmission — Single characters can be transmitted using programmed transfers. Characters can also be transferred by DMA.
- Reception — Received characters are deserialized by the OCTART and transferred to a four-character area in the RAM (one such area per line) by the control chip's OCTART sequencer, following an interrupt from the OCTART. The control chip's OCTART sequencer later removes characters from the bottom of the 4-character FIFO, and places them in the 256 × 16 receive FIFO, which can be read by the host.
- Modem Control — The modem control latches are external to the control chip. Data is written to the latches from RAM by the UART interface sequencer. The sequencer also samples modem status lines every 10 milliseconds and reports on changes via the STAT register (and also via the receive FIFO, if programmed to do so).

1.5.3 Control Chip

The control chip contains the following functional blocks.

- Q-bus Interface — Matches addresses, generates vector addresses, and handles interrupts. It also interfaces the Q-bus signals to other functional blocks
- Data I/O Sequencer — Controls host access to device registers
- OCTART Sequencers — Transfers data between the OCTART and RAM, and handles flow control
- Self-Test Power-Up Sequencer — This section powers-up the module to a fixed set of initial conditions, such as 9600 baud rate on all lines; it also handles self-test

- DMA Sequencer — Initiates and manages all DMA data transfers to the module
- RAM Arbitrator — Provides RAM and OCTART bus access to the various sequencers.

1.5.4 OCTART Chip

This chip contains eight UARTs, which perform parallel-to-serial and serial-to-parallel data conversions. It interfaces with the control chip through eight registers. Four are read-only and four are write-only. An index register is used to access individual lines. The OCTART chip shares the RAM bus with the control chip, and the RAM itself. The OCTART chip also includes:

- Receive and transmit control blocks
- Interrupt logic for interfacing with the control chip
- A 16-output baud-rate generator
- All necessary line-parameter registers
- Diagnostic loopback logic
- Modem status multiplexers.

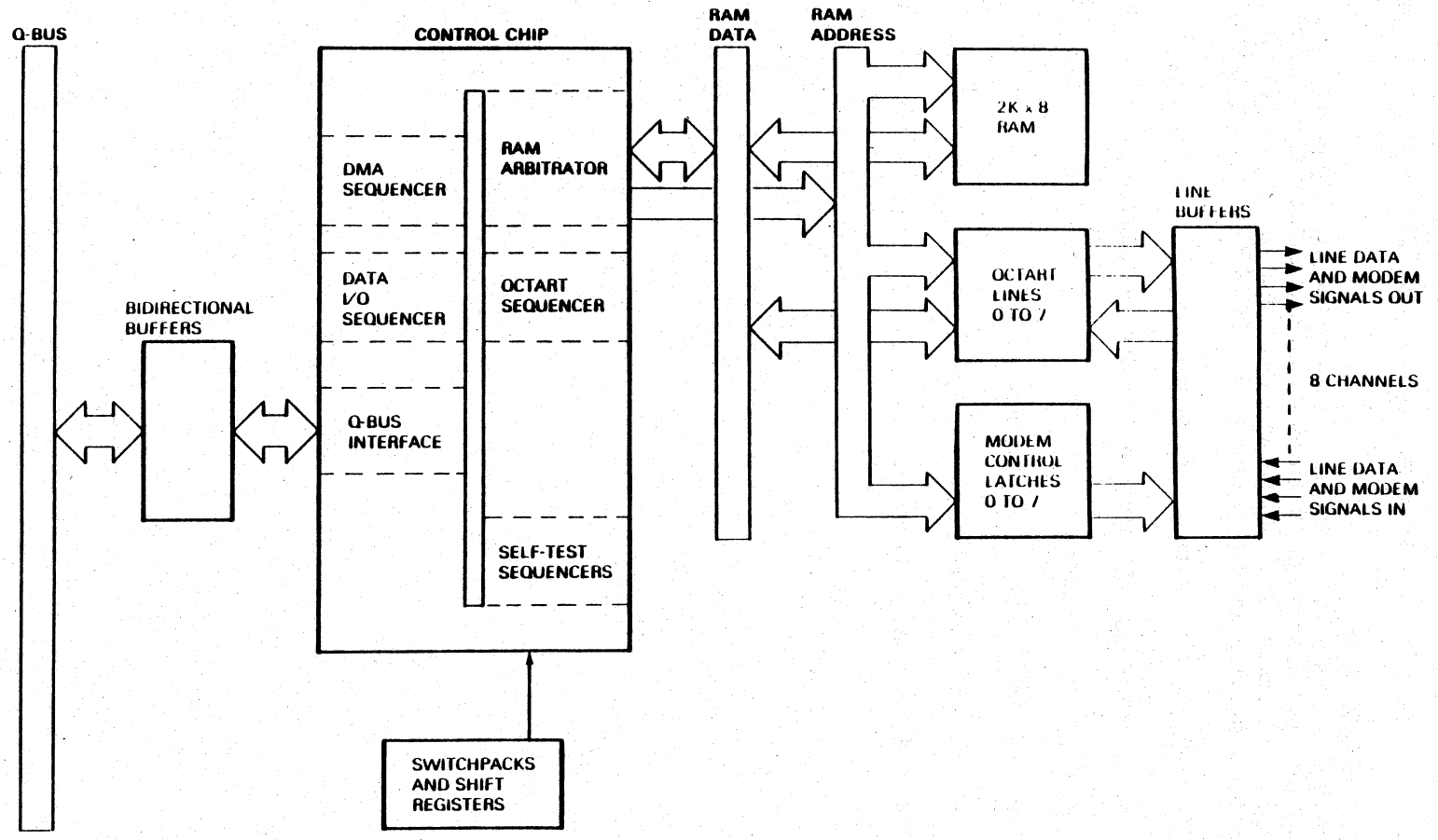

Figure 1-5 DHQ11 Functional Block Diagram

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter describes the preparation and installation of the DHQ11 option. It contains the following sections.

- Unpacking
- Preparation
- Installation
- Testing

2.2 UNPACKING AND INSPECTION

If ordered as part of a system, the DHQ11 will already be installed, and you should refer to the instructions for unpacking the system.

If ordered as an add-on option to an existing system, a DHQ11-M (Q-bus module) will be supplied together with a cabinet kit, distribution panels, and interconnecting cables. The choice of cabinet kit depends on the type of system and on whether EIA-232-D or DEC423 connection standards apply (Table 2-1 gives details of these options).

NOTE

DEC423 is a term used in this manual to indicate a data-leads-only implementation of the RS-423-A electrical interface standard.

If the equipment is to be installed by DIGITAL Field Service, the customer should not open the packages.

If the DHQ11 was ordered as an add-on option, find the carton marked OPEN FIRST and carefully unpack it. There is a shipping list inside the carton.

Undo each package and examine the contents for physical damage. Check that the contents of each package are complete. Report any damaged or missing items to the shipping agent and to the DIGITAL representative. Do not dispose of the packing material until the unit has been installed and is operational.

Table 2-1 DHQ11 Options

DHQ11-M	**M3107 module + DHQ11 User Guide (EK-DHQ11-UG) (Base Option)**			
	EIA-232-D Cabinet Kits			
CK-DHQ11-AA	BA123 boxes			
CK-DHQ11-AB	BA23 boxes			
CK-DHQ11-AF	H9624 cabinets			
Contents				
H3173A	4-line 25-way distribution panel	2	2	2
BC05L-1K	40-way ribbon cable, 21 inch			2
BC05L-01	40-way ribbon cable, 12 inch		2	
BCO5L-03	40-way ribbon cable, 36 inch	2		
	DEC423 Cabinet Kits			
CK-DHQ11-WA	BA123 boxes			
CK-DHQ11-WB	BA23 boxes			
CK-DHQ11-WF	H9624 cabinets			
Contents				
H3100	Active bulkhead panel	1	1	1
BC05L-1K	Ribbon cable — 2"			2
BC05L-01	Ribbon cable — 12"		2	
BC05L-03	Ribbon cable — 36"	2		
70-22775-1K	Bulkhead power cable			1
70-22775-01	Bulkhead power cable		1	
70-22775-03	Bulkhead power cable	1		
H3104	Cable concentrator	1	1	1
BC16C-25	Multiway cable	1	1	1
H3101	Multiway cable loopback	1	1	1

2.3 PREPARING THE DHQ11 MODULE

Please check that your system has sufficient power and bus load capacity before installing additional modules; see your system manual. Before installing the DHQ11, you must define two parameters by selecting them on the DHQ11 on-board switchpacks. The parameters are:

- Module address

- Interrupt vector

NOTE

Ensure that you are wearing an antistatic wriststrap, part number 29-11762-00.

2.3.1 Address And Vector Assignment

The DHQ11 has a floating device address and vector. It is shipped from the factory with a device address of 17760440_8 and a vector of 300_8. These assignments are determined by the floating address and vector rules. The factory settings are only correct if no other floating address option is installed in the system. Otherwise, the proper rules for address assignment must be applied; these are given in Appendix C.

2.3.2 Setting The Address Switches

The device address for the DHQ11 is set on the 10-position switchpack E19; the location of this switchpack is shown in Figure 2-1. SW-1 is not used and must be set OFF (open).

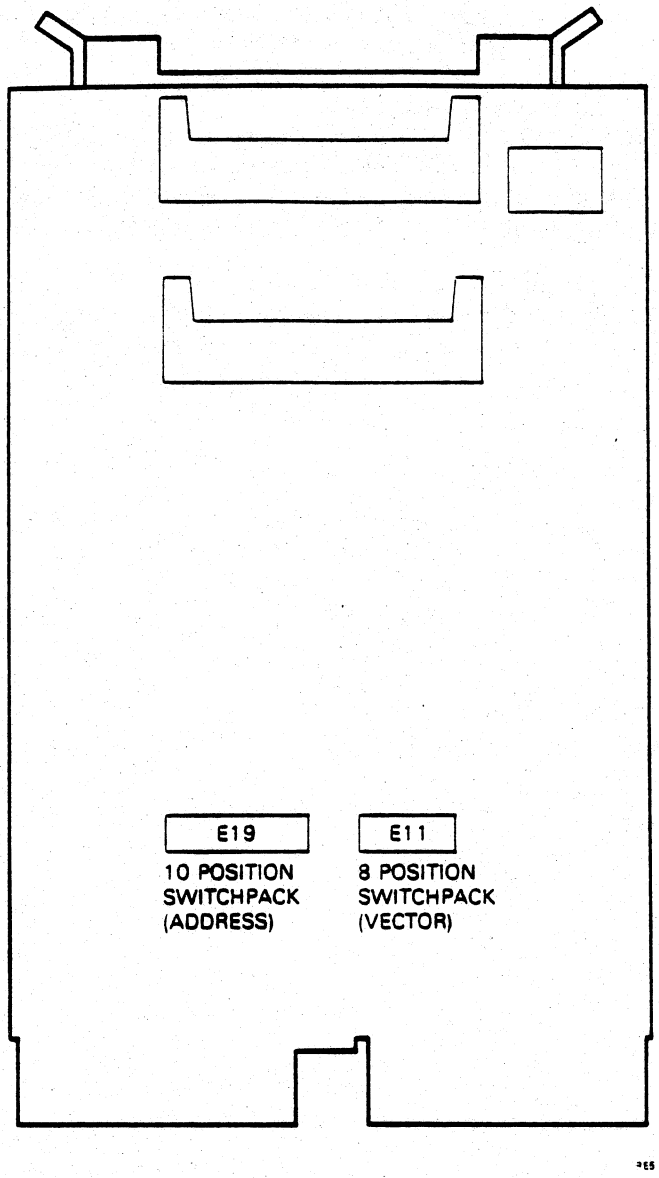

Figure 2-1. Location of Switchpacks

Figure 2-2 shows how to set the device address on the switchpack. The example shown is for the factory-set address of 17760440_8.

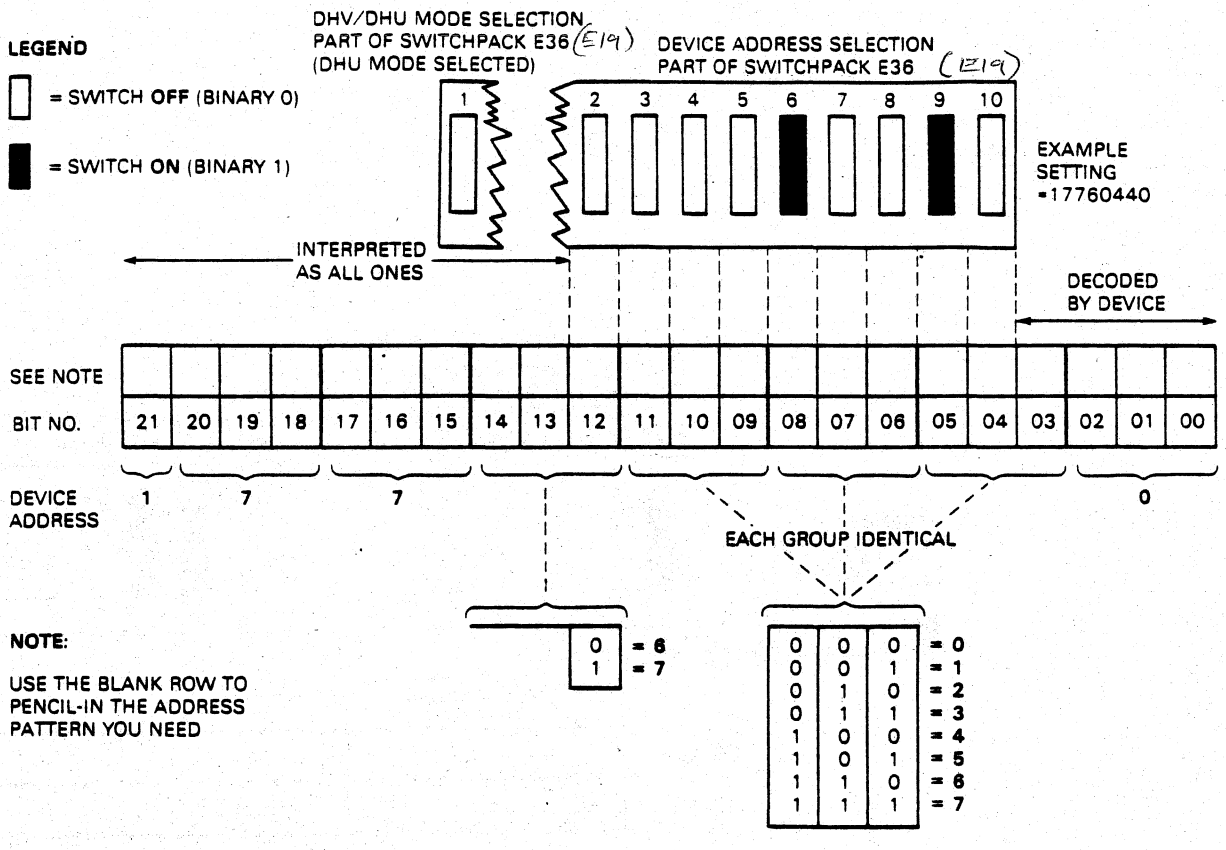

Figure 2-2 Setting the Device Address

2.3.3 Setting The Vector Switches

The six high-order bits of the interrupt are set on the eight-position switchpack E11. Figure 2-1 shows the location of this switchpack. Figure 2-3 shows an example of these switches set to the factory setting of 300_8. Switches 1 and 2 are used during manufacture, SW-1 must be set ON (closed), and SW-2 must be set OFF (open) for correct operation of the DHQ11.

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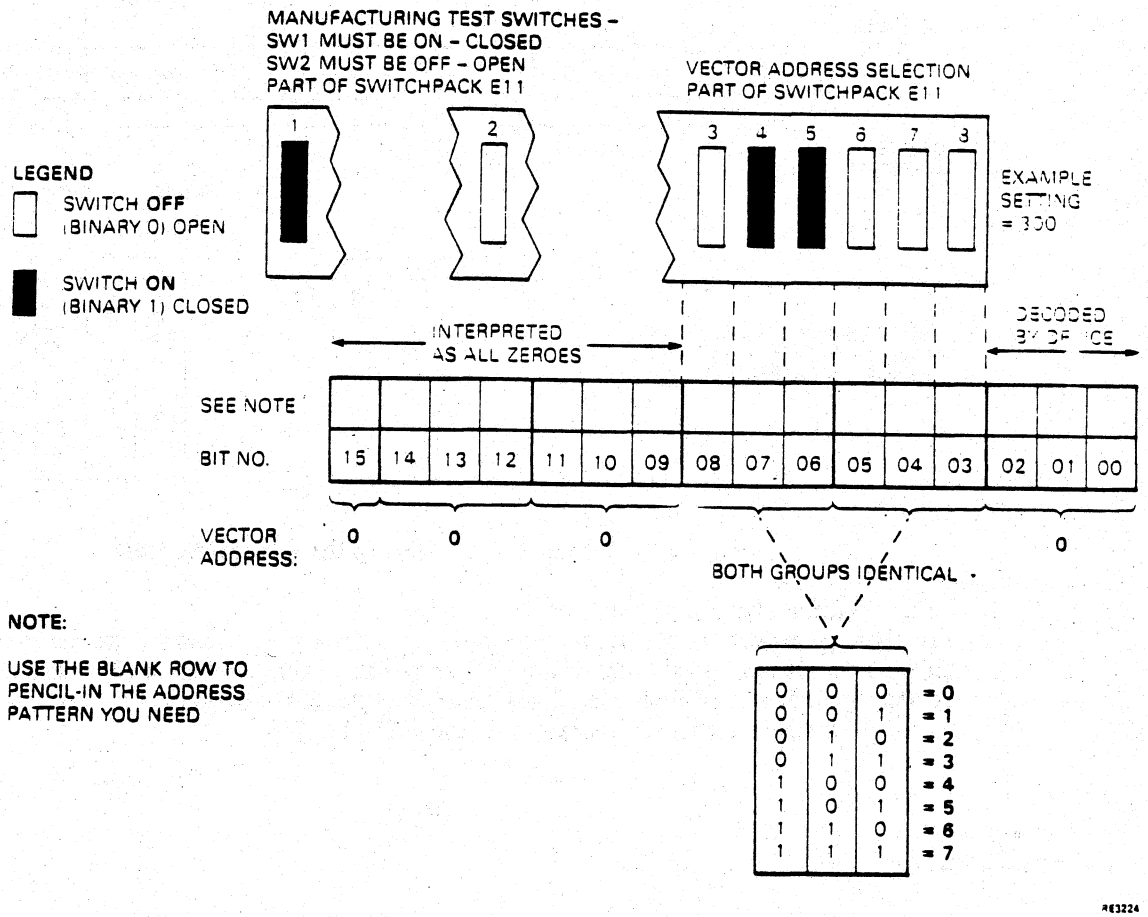


Figure 2-3 Setting the Vector Address

2.4 BUS CONTINUITY

Bus grant continuity jumper cards (M9047) are used in vacant backplane slots to provide bus continuity (see Figure 2-4).

NOTE

To find out the type of backplane on your system, consult your system manual.

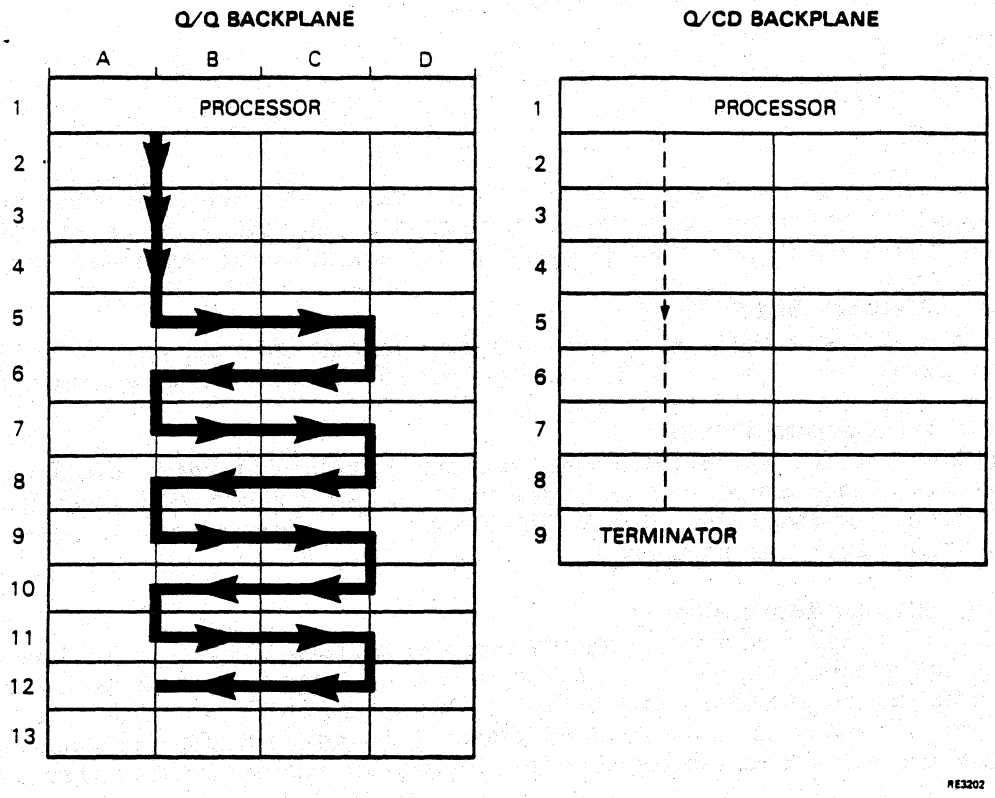


Figure 2-4 Bus Grant Continuity

2.4.1 Bus Grant Continuity Jumpers

Backplanes suitable for DHQ11 fall into two groups.

Q/CD – Q-bus on A and B connectors, user-defined signals on C and D

Q/Q – Q-bus on A and B, and C and D connectors.

In Q/CD backplanes, bus grant signals pass through each installed module via the A and C connectors of each bus slot.

Q/Q backplanes are designed so that two dual-height options can be installed in a quad-height bus slot. The Q-bus lines are routed as follows.

1. AB, first slot
2. CD, first slot
3. CD, second slot
4. AB, second slot

and so on.

Each dual-height module extends the continuity of the bus grant signals BIAK and BDMG to the next module. Therefore, with a Q/Q backplane, if a quad module (DHV11) is replaced with a dual module (DHQ11), a Q-bus grant continuity card M9047 is needed for the vacant slot.

2.5 PRIORITY SELECTION

The bus (backplane) position may be a compromise between DMA and interrupt priority requirements. As a general rule, consider DMA request priorities first, and then consider interrupt (bus) requests.

2.5.1 DMA Request Priority

DMA request priority is usually assigned according to throughput. Faster devices (higher throughput) usually have priority over slower DMA devices; for example, disk has priority over tape, which itself has priority over communications devices. This is because fast devices usually reach overrun or underrun conditions sooner than slower ones.

2.5.2 Interrupt Request Priority

The DHQ11 has a fixed interrupt priority level of 4, and cannot be changed to other priority levels. It does not monitor any of the higher-level interrupt request lines. Because of this, both the interrupt-request and DMA (non-processor request) priorities of the DHQ11 are selected by the position of the DHQ11 on the bus; it must therefore be positioned after any device that does monitor any of the request lines. Devices closest to the processor module have the highest priority.

2.5.3 Recommendations

In general the DHQ11 bus position is not critical. However, it is recommended that you place the module after any mass-storage interfaces and high-speed synchronous communications options; these are more sensitive to bus position.

2.6 INSTALLING THE DHQ11

Once you have defined the backplane position for the DHQ11, you can begin to install the DHQ11 module.

2.6.1 Installing The M3107 Module

WARNING

Shut off the system power and disconnect the main system power cord before performing any procedure in this chapter.

ATTENTION

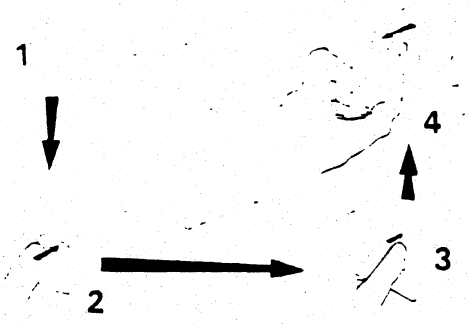
Avant d'effectuer l'une des procédures de ce chapitre, mettez le système hors tension et débranchez le cordon d'alimentation.

VORSICHT!

Schalten Sie das System ab, und ziehen Sie das Netzkabel, bevor Sie die in diesem Kapitel beschriebenen Anweisungen ausführen.

ATENCION

Apague el sistema y desconecte el cable principal de alimentación antes de realizar ningún procedimiento de este capítulo.



1. Connect the BC05L cables to J1 and J2. Figure 2-5 for EIA-232-D installations and Figure 2-6 for DEC423 installations show how the parts of the option connect together.
2. Install the module in its correct backplane position as previously defined.

NOTE

Be careful not to snag module components on the card guides or adjacent modules.

3. Check that bus continuity exists. If necessary, install bus grant continuity cards.
4. Do not connect the cables to the bulkhead panels.

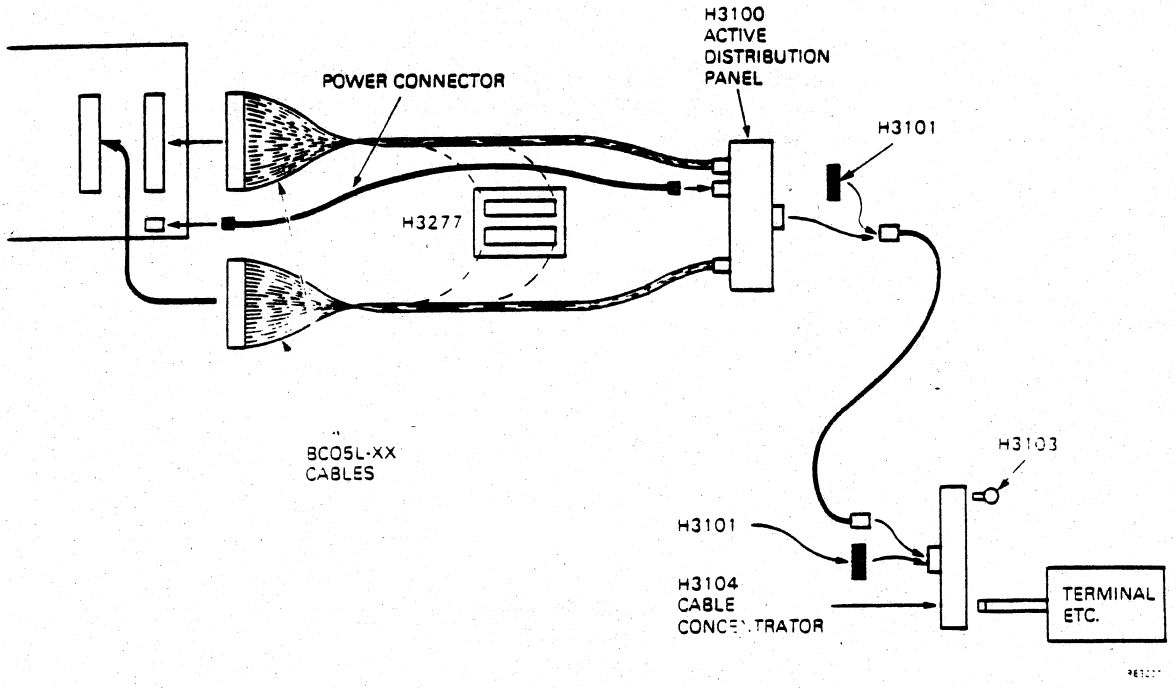


Figure 2-5 Installing the DHQ11 (EIA-232-D)

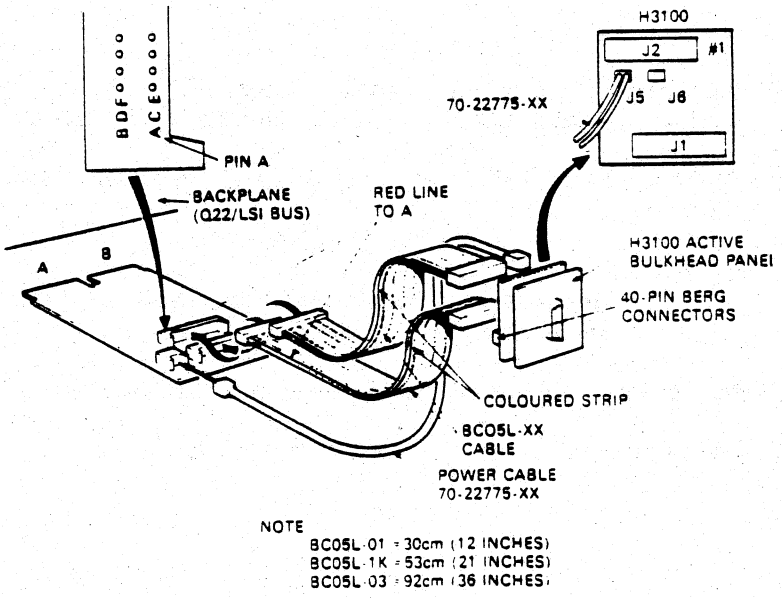


Figure 2-6 Installing the DHQ11 (DEC423)

2.6.2 Distribution Panels

The rear I/O distribution panel has six cutouts: two type-A cutouts and four type-B cutouts. In addition, a removable bracket between the third and fourth cutout allows you to install three more type-A insert panels by mounting an adapter plate. Figure 2-7 shows typical type-A and type-B insert panels, and the adapter plate.

2.6.3 Installing The EIA-232-D Distribution Panels

The DHQ11 has two type-B distribution panels. Figure 2-7 shows how these are installed in a BA23 box. Installation in BA123 and H9642 cabinets is similar.

To fit the distribution panels:

1. Remove the two type-B blanking panels.
2. Bolt the two H3173-A distribution panels into the cutouts.
3. Connect the free end of the BC05L-XX cable from connector J1 of the module to the first distribution panel.
4. Connect the free end of the BC05L-XX cable from connector J2 of the module to the second distribution panel.

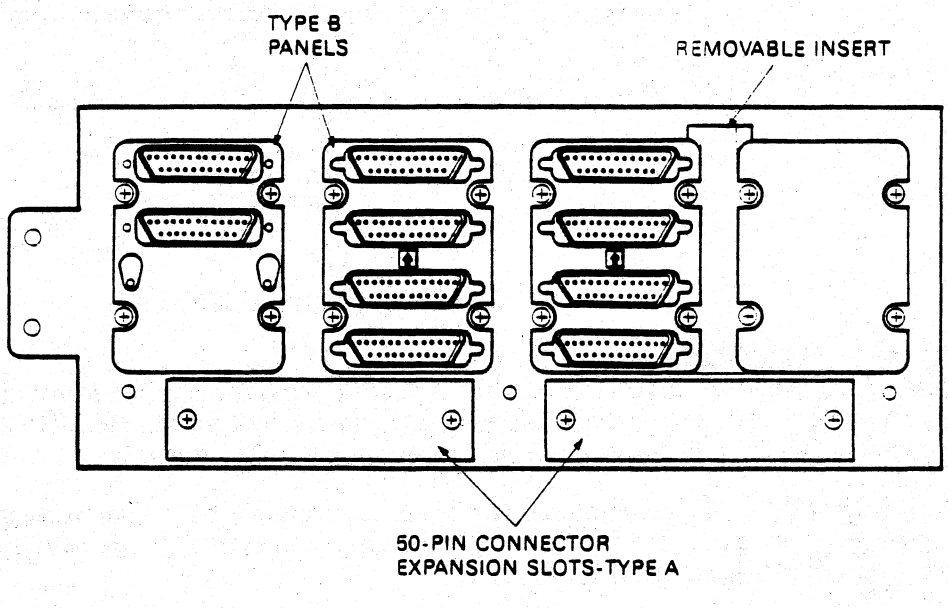


Figure 2-7 I/O Insert Panels and Adapter Plate (EIA-232-D)

2.6.4 Installing The DEC423 Distribution Panels

The DHQ11 has one type-B distribution panel. Figure 2-8 shows how this is installed in a BA23 box. Installation in BA123 and H9642 cabinets is similar.

To fit the distribution panels:

1. Remove a type-B blanking panel.

2. Bolt the H3100 active distribution panel into the cutout.

3. Connect the free end of the BC05L-XX cable from connector J1 of the module to the upper (J2) connector on the distribution panel.

4. Connect the free end of the BC05L-XX cable from connector J2 of the module to the lower (J1) connector on the distribution panel.

5. Connect the free end of the power cable (70-22775-XX) to the left-hand power connector (J5) on the distribution panel.

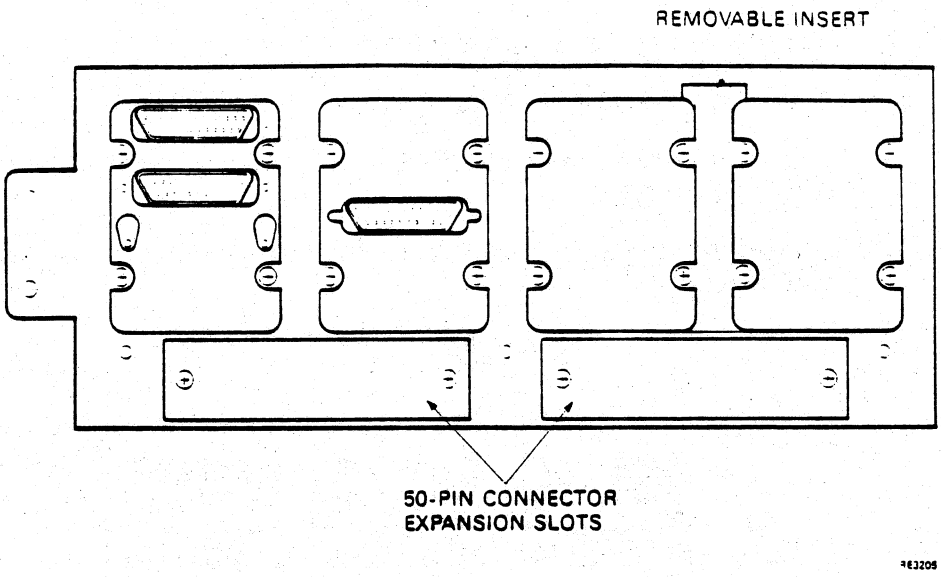


Figure 2-8 I/O Insert Panel (DEC423)

2.7 INSTALLATION TESTING

This section details the diagnostics used to test the option during and after installation. The diagnostics are also used to test other Q-bus modules in the same family, for example, DHV11. The diagnostics will automatically 'size' the option to determine which one is being tested.

Both MicroPDP-11 and MicroVAX II diagnostics are described. After successful completion of the appropriate system test, the DHQ11 may be connected to external equipment. Further information on the diagnostics is given in Chapter 4.

2.7.1 Installation Tests On MicroPDP-11 Systems

To verify that the MicroPDP-11 system and the DHQ11 module are functioning correctly:

1. Switch on the system.

2. After 2 seconds, check that the green self-test LED on the DHQ11 module is on. If it does not come on, call DIGITAL Field Service.

3. Boot the Micro-11 Customer Diagnostic media. Refer to your *MicroPDP-11 System Manual* for further information.

4. Type 'I' at the main menu to allow the diagnostics to identify the new module, and add it to the configuration file.

NOTE

Look at the list of devices displayed, and make sure that the new module is included. If it is not included, repeat the installation sequence, and make sure that the module switches have been set correctly.

5. Type 'T' at the main menu to run the system tests. These should complete without error; if an error occurs, call DIGITAL Field Service.

A MicroPDP-11 Maintenance Kit is available, and may be ordered from your local DIGITAL office. This kit allows trained personnel to run individual diagnostic programs under the XXDP+ diagnostic monitor, and to configure and run DECX11 system test programs. The XXDP+ functional diagnostic is VHQA**.BIN, and the DECX11 module is XDHV**.OBJ.

2.7.2 Testing In MicroVAX II Systems

To verify that the MicroVAX II system and the DHQ11 module are functioning correctly:

1. Check that the green self-test LED on the DHQ11 module is on.

2. Boot the MicroVAX Maintenance System media. Refer to your *MicroVAX II System Manual* for further information.

3. Type '2' at the main menu to show the system configuration and devices.

NOTE

Look at the list of devices displayed, and make sure that the new module is included. If it is not included, repeat the installation sequence, and make sure that the module switches have been set correctly.

4. Type '1' at the main menu to run the system tests. These should complete without error; if an error occurs, call DIGITAL Field Service.

2.8 DIAGNOSTIC TEST CONNECTORS

2.8.1 Staggered Loopback Test Connector H3277

The H3277 test connector (see Figure 2-9) is used during service-mode diagnostic tests on either EIA-232-D or DEC423 installations. It allows all channels to be tested. Using this connector, you can trace a channel fault to one of two channels.

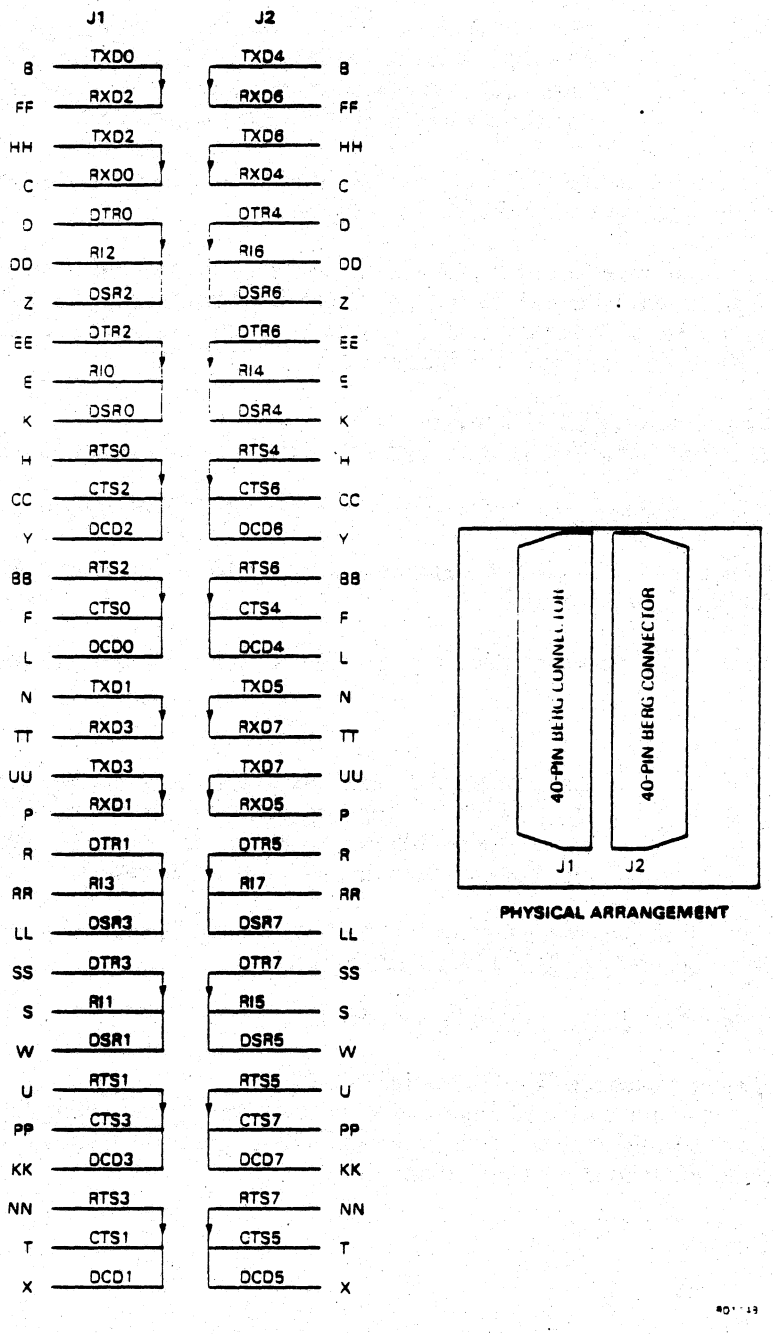


Figure 2-9 H3277 Staggered Loopback Test Connector

2.8.2 Line Loopback Test Connector H3197

This connector is shown in Figure 2-10. It can be used during service-mode diagnostic tests to trace a fault to a single channel for EIA-232-D installations. The older-style H325 test connector provides the same signal loopbacks as the H3179, and may be used in place of it.

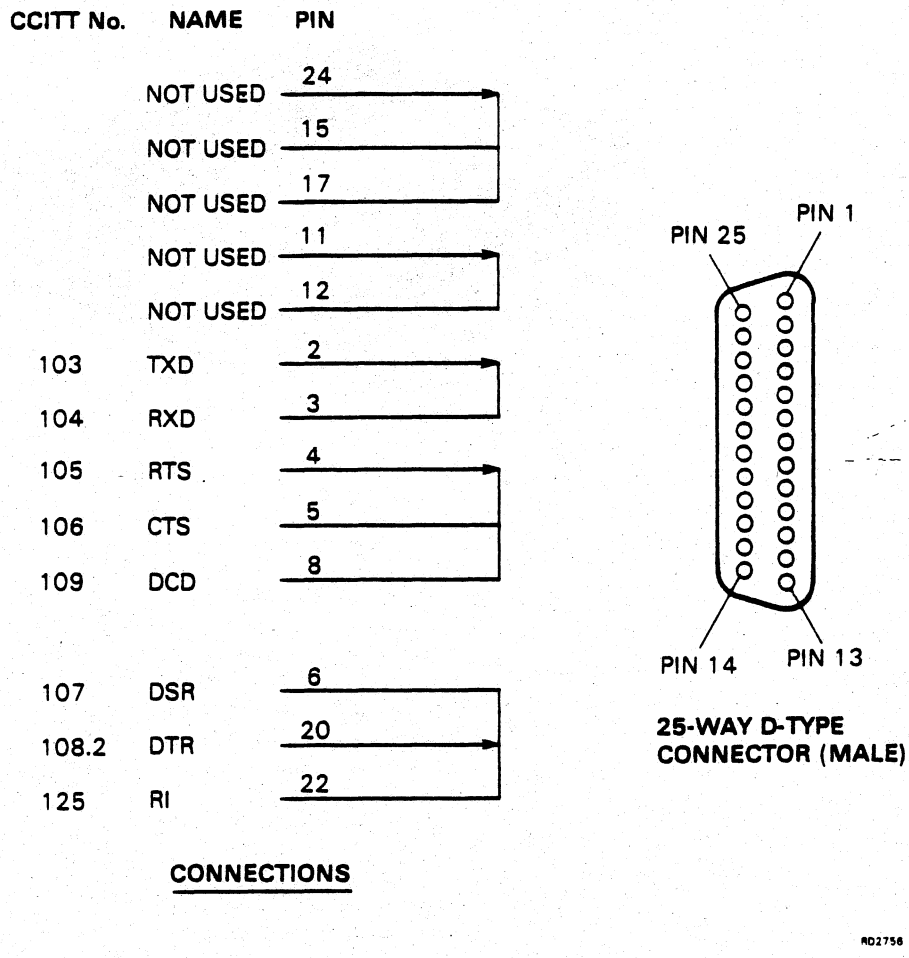
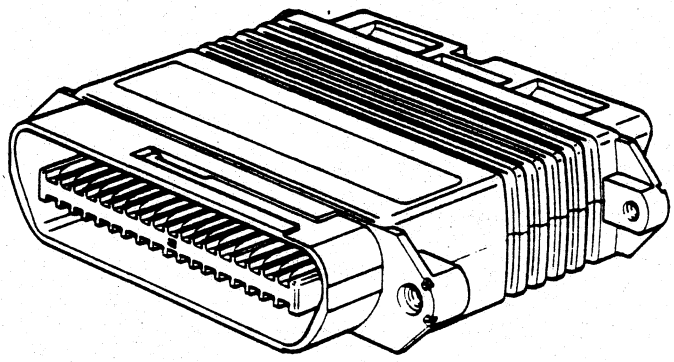


Figure 2-10 H3197 Line Loopback Test Connector

2.8.3 H3101 Loopback Connector

The H3101 loopback connector (see Figure 2-11) is used during diagnostic tests for DEC423 installations. It is two loopback connectors in one package, and consists of a female 36-way loopback connector and a male 36-way loopback connector. It can be inserted into the cabling at the distribution panel, or at the cable concentrator. To test the cables, type characters at the keyboard and make sure that they are echoed to the screen (refer to Chapter 4).



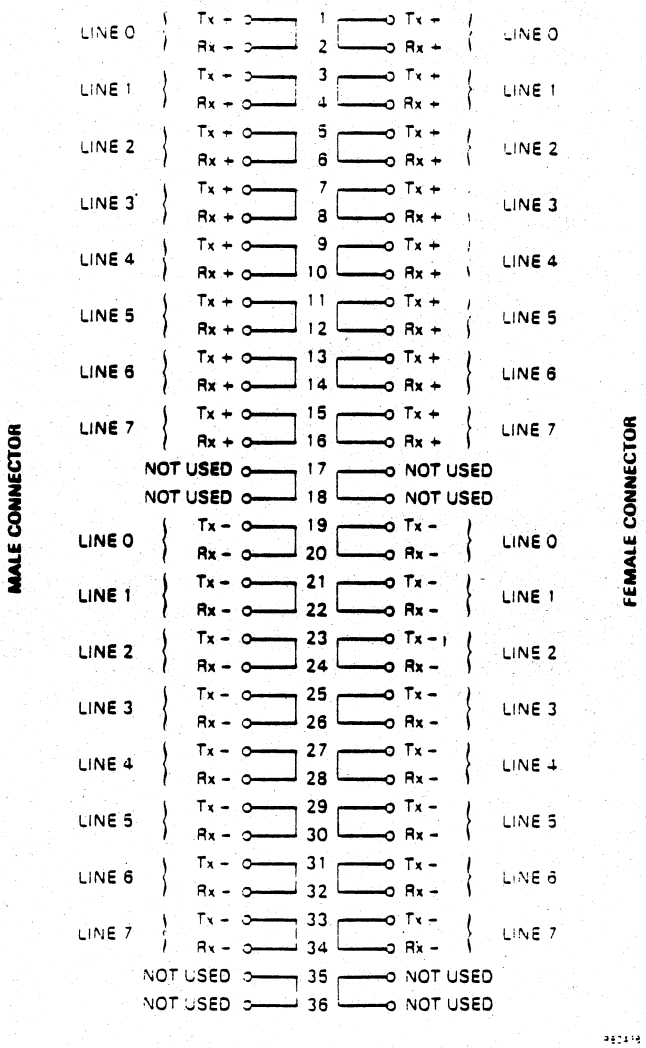
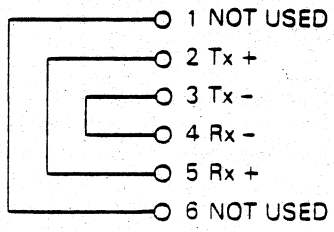


Figure 2-11 H3101 Loopback Connector

2.8.4 H3103 Loopback Connector

The H3103 loopback connector (see Figure 2-12) is used during service-mode diagnostic testing with DEC423 installations to test each line from the DHQ11 at the output from the H3104 cable concentrator.



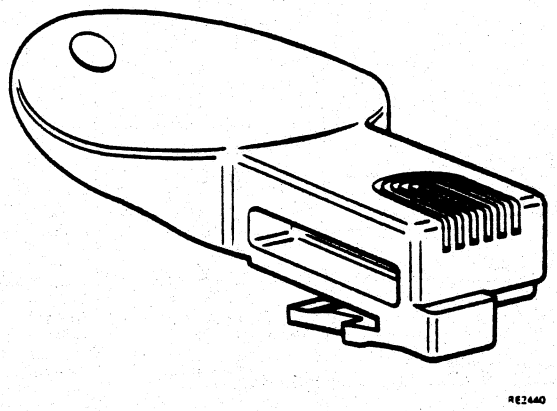


Figure 2-12 H3103 Line Loopback Test Connector

2.9 CABLES AND CONNECTORS — EIA-232-D

2.9.1 Distribution Panel

Each H3173-A distribution panel adapts one of the DHQ11 Berg connectors to four subminiature D-type EIA-232-D connectors. Noise filtering is provided on each pin of the EIA-232-D connectors. This reduces electromagnetic radiation from the cables and also provides the logic with some protection against static discharge.

Figure 2-13 shows the circuit of the H3173-A. There is no CCITT equivalent of EIA circuit AA (Protective Ground). You can remove the 0-ohm link W1 to disconnect this circuit if necessary.

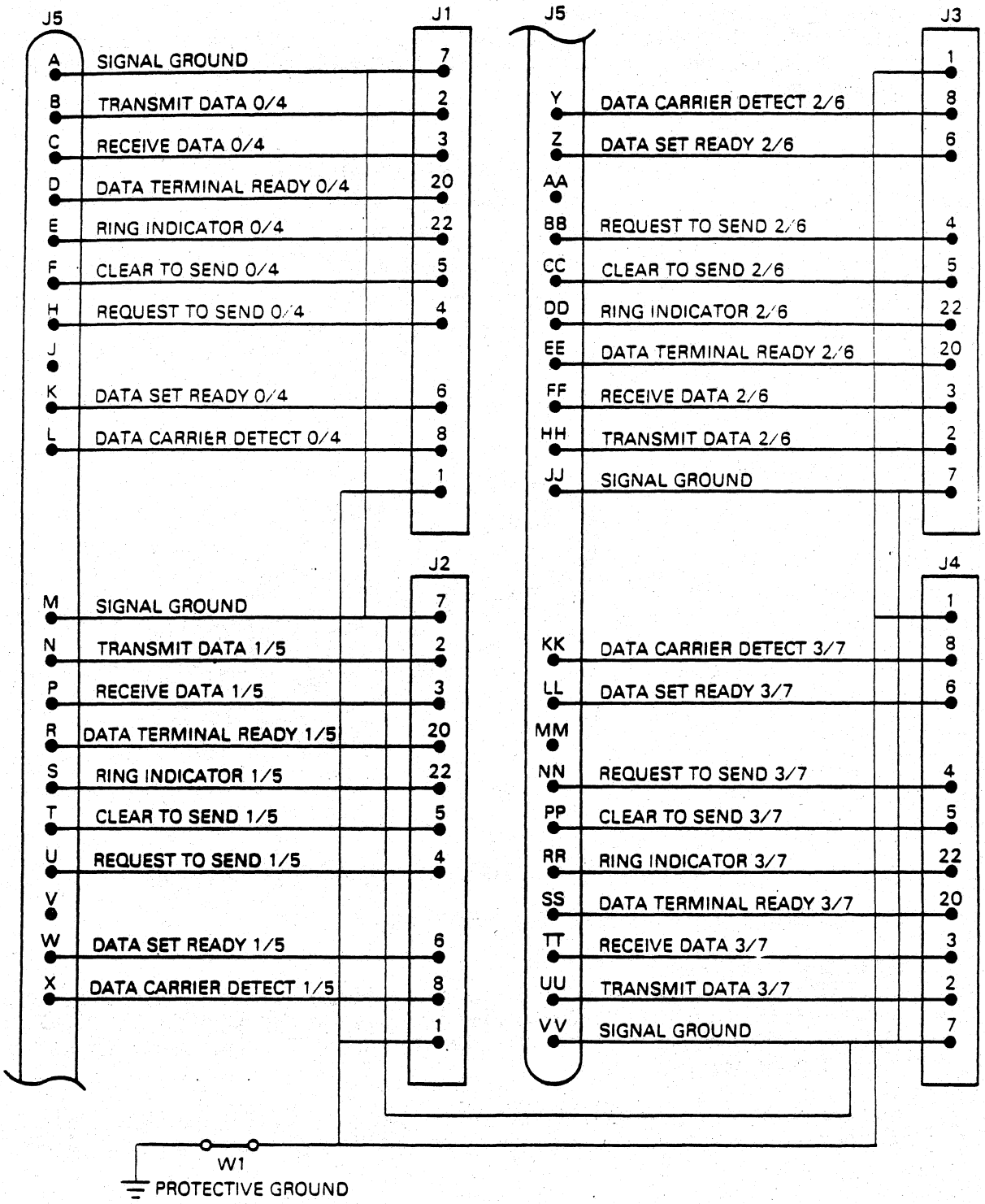


Figure 2-13 H3173-A Circuit Diagram

Table 2-2 is for two distribution panels. The numbers within parentheses apply to channels 4 to 7.

Table 2-2 H3173-A Connections

Signal	Name	Circuit No.	J5 Pin No.
SIG GND 0(4)		102	1-A (2-A)
TXD0(4)	Transmitted Data	103	1-B (2-B)
RXD0(4)	Received Data	104	1-C (2-C)
DTR0(4)	Data Terminal Ready	108.2	1-D (2-D)
RI0(4)	Ringing Indicator	125	1-E (2-E)
CTS0(4)	Clear to Send	106	1-F (2-F)
RTS0(4)	Request to Send	105	1-H (2-H)
DSR0(4)	Data Set Ready	107	1-K (2-K)
DCD0(4)	Data Carrier Detected	109	1-L (2-L)
SIG GND 1(5)		102	1-M (2-M)
TXD1(5)		103	1-N (2-N)
RXD1(5)		104	1-P (2-P)
DTR1(5)		108.2	1-R (2-R)
RI1(5)		125	1-S (2-S)
CTS1(5)		106	1-T (2-T)
RTS1(5)		105	1-U (2-U)
DSR1(5)		107	1-W (2-W)
DCD1(5)		109	1-X (2-X)
DCD2(6)		109	1-Y (2-Y)
DSR2(6)		107	1-Z (2-Z)
RTS2(6)		105	1-BB (2-BB)
CTS2(6)		106	1-CC (2-CC)
RI2(6)		125	1-DD (2-DD)
DTR2(6)		108/2	1-EE (2-EE)
RXD2(6)		104	1-FF (2-FF)
TXD2(6)		103	1-HH (2-HH)
SIG GND 2(6)		102	1-JJ (2-JJ)
DCD3(7)		109	1-KK (2-KK)
DSR3(7)		107	1-LL (2-LL)
RTS3(7)		105	1-NN (2-NN)
CTS3(7)		106	1-PP (2-PP)
RI3(7)		125	1-RR (2-RR)
DTR3(7)		108/2	1-SS (2-SS)
RXD3(7)		104	1-TT (2-TT)
TXD3(7)		103	1-UU (2-UU)
SIG GND 3(7)		102	1-VV (2-VV)

The following examples show how to use Table 2-2.

Signal TXD0 is the transmitted data line for channel 0; the CCITT circuit number is 103 and it is connected to J5 pin B on the first H3173-A for channels 0 to 3.

Signal TXD4 is the transmitted data line for channel 4; the CCITT circuit number is 103 and it is connected to J5 pin B on the second H3173-A for channels 4 to 7.

2.9.2 Null Modem Cables

Null modem cables are used for local EIA-232-D connection, when a modem is not used. Because of Federal Communications Commission (FCC) regulations, the cable specifications for the United States and Canada are different from those for non-FCC countries. Other countries may also have similar electromagnetic interference (EMI) control regulations. EMC/RFI shielded cabinets are now available for systems which conform to FCC requirements.

Recommended null modem cables are as follows.

1. BC22D (for EMC RFI shielded cabinets)

   - Rounded 6-conductor fully shielded cable to FCC specification
   - Subminiature 25-pin D-type female connector moulded on each end
   - Lengths available:

BC22D-10	3.1 m	(10 ft)
BC22D-25	7.6 m	(25 ft)
BC22D-35	10.7 m	(35 ft)
BC22D-50	15.2 m	(50 ft)
BC22D-75	22.9 m	(75 ft)
BC22D-A0	30.5 m	(100 ft)
BC22D-B5	76.2 m	(250 ft)

2. BC03M

   - Round 6-conductor (three twisted pairs), each pair shielded
   - Cables over 30.5 m (100 ft) have a 25-pin subminiature D-type female connector at one end. The other end is unterminated, for passing through the conduit
   - Cables 30.5 m (100 ft) and less have a similar connector at each end
   - Lengths available:

BC03M-25	7.6 m	(25 ft)
BC03M-A0	30.5 m	(100 ft)
BC03M-B5	76.2 m	(250 ft)
BC03M-E0	152.4 m	(500 ft)
BC03M-L0	304.8 m	(1000 ft)

3. BC22A

   - Round 6-conductor cable
   - Subminiature 25-pin D-type female connector moulded at each end

- Lengths available:

BC22A-10	3.1 m	(10 ft)
BC22A-25	7.6 m	(25 ft)

Cables of groups 1, 2, and 3 are all connected as in Figure 2-14. The cables are not polarized. They can be connected either way round.

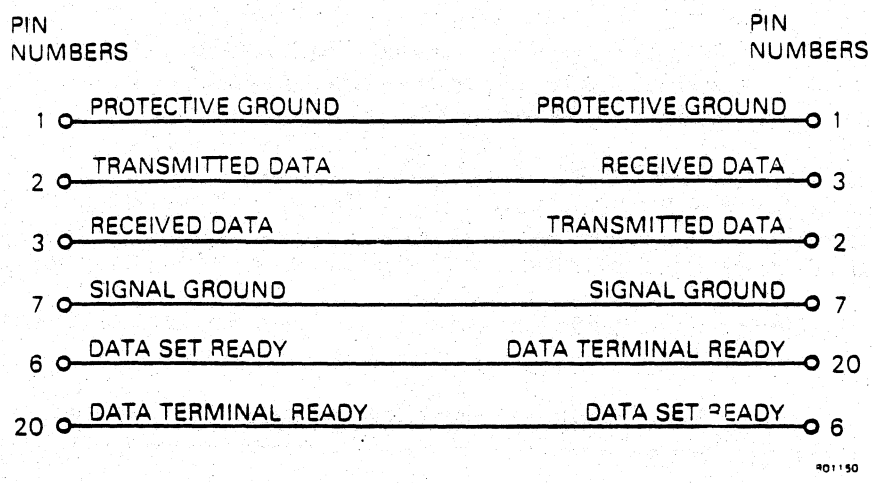


Figure 2-14 Null Modem Cable Connections

2.9.3 Full Modem Cables

Recommended full modem cables are as follows:

1. BC22F (for EMC/RFI-shielded cabinets)

   - Rounded 25-conductor fully shielded cable
   - Subminiature 25-pin D-type female connector on one end, male connector on the other
   - Lengths available:

BC22F-10	3.1 m	(10 ft)
BC22F-25	7.6 m	(25 ft)
BC22F-35	10.7 m	(35 ft)
BC22F-50	15.2 m	(50 ft)
BC22F-75	22.9 m	(75 ft)

2. BC05D

   - Round 25-conductor cable
   - Subminiature 25-pin D-type, female connector on one end, male connector on the other

- Lengths available:

BC05D-10	3.1 m	(10 ft)
BC05D-25	7.6 m	(25 ft)
BC05D-50	15.2 m	(50 ft)
BC05D-60	18.6 m	(60 ft)
BC05D-A0	30.5 m	(100 ft)

NOTE

In some countries, protective hardware may be needed when connecting to certain lines. Refer to the national regulations before making a connection.

2.10 CABLES AND CONNECTORS — DEC423

The H3100 active distribution panel adapts the two DHQ11 Berg connectors to one 36-way AMP connector. Noise filtering is provided on each pin of the connector. This reduces electromagnetic radiation from the cables and also provides the logic with some protection against static discharge.

Table 2-3 shows connections to the 36-pin AMP filtered connectors used on DHQ11 with DEC423 installations.

Table 2-3 Serial-Line Connections for the 36-Pin Connector

1	Blu/Wht	Line 0	Transmit +	19	Wht Blu	Line 0	Transmit –
2	Org/Wht	Line 0	Receive +	20	Wht Org	Line 0	Receive –
3	Grn/Wht	Line 1	Transmit +	21	Wht/Grn	Line 1	Transmit –
4	Brn/Wht	Line 1	Receive +	22	Wht/Brn	Line 1	Receive –
5	Slt/Wht	Line 2	Transmit +	23	Wht/Slt	Line 2	Transmit –
6	Blu/Red	Line 2	Receive +	24	Red/Blu	Line 2	Receive –
7	Org/Red	Line 3	Transmit +	25	Red/Org	Line 3	Transmit –
8	Grn/Red	Line 3	Receive +	26	Red/Grn	Line 3	Receive –
9	Brn/Red	Line 4	Transmit +	27	Red/Brn	Line 4	Transmit –
10	Slt/Red	Line 4	Receive +	28	Red/Slt	Line 4	Receive –
11	Blu/Blk	Line 5	Transmit +	29	Blk/Blu	Line 5	Transmit –
12	Org/Blk	Line 5	Receive +	30	Blk/Org	Line 5	Receive –
13	Grn/Blk	Line 6	Transmit +	31	Blk/Grn	Line 6	Transmit –
14	Brn/Blk	Line 6	Receive +	32	Blk Brn	Line 6	Receive –
15	Slt/Blk	Line 7	Transmit +	33	Blk Slt	Line 7	Transmit –
16	Blu/Yel	Line 7	Receive +	34	Yel Blu	Line 7	Receive –
17	Org/Yel	Spare		35	Yel Org	Spare	
18	Grn/Yel	Spare		36	Yel Grn	Spare	

CHAPTER 3
PROGRAMMING

3.1 SCOPE

This chapter describes the device registers, and how they are used to control and monitor the DHQ11. The chapter covers:

- The bit functions and format of each register
- Programming features available to the host.

Some programming examples are also included.

3.2 REGISTERS

The host system controls and monitors the DHQ11 module through several Q-bus-addressable registers.

Command words or bytes written to the registers are interpreted and executed by the module. Status reports and data are also transferred through the registers.

3.2.1 Register Access

The DHQ11 registers occupy 8 words (16 bytes) of Q-bus memory-mapped I/O space.

The base physical address of the eight DHQ11 registers is selected by using switches on the module. The address selected is in the peripheral I/O space. The term 'base' means the lowest I/O address on the module; that is to say, when the four low-order address bits = 0.

Table 3-1 lists the DHQ11 registers and their addresses. The suffix (I) means that there are eight of these registers, one for each channel. When an (I) register is accessed, the contents of CSR<3:0> selects which of the eight registers at that address is actually accessed.

NOTE

CSR<3:0> allows up to 16 channels to be addressed. However, only the lower eight channels are used. Therefore CSR bit 3 must always be 0.

Table 3-1 DHQ11 Registers

Register		Address (Octal)	Type
Control and Status Register	(CSR)	Base	Read Write
Receive Buffer	(RBUF)	Base+2	Read Only
Transmit Character	(TXCHAR)	Base+2 (I)	Write Only

Table 3-1 DHQ11 Registers (Cont.)

Register		Address (Octal)	Type
Line-Parameter Register	(LPR)	Base + 4 (I)	Read/Write
Line Status	(STAT)	Base + 6 (I)	Read Only
Line Control	(LNCTRL)	Base + 10(I)	Read Write
Transmit Buffer Address 1	(TBUFFAD1)	Base + 12(I)	Read Write
Transmit Buffer Address 2	(TBUFFAD2)	Base + 14(I)	Read Write
Transmit Buffer Count	(TBUFFCT)	Base + 16(I)	Read Write

NOTE

It is possible to write to the line-status register. However, the host should not write to this register.

There are eight line-parameter registers, only one of which is accessed at any one time. The register which is accessed is associated with the line selected using CSR<3:0>.

For example, to read the line-parameter register of channel 3, the following I/O commands would be executed:

```
MOVB #CHAN,@#BASE      ;WRITE CHANNEL NUMBER (SEE BELOW) TO CSR
MOVB @#BASE+4,R0       ;READ THE LINE PARAMETER REGISTER
```

In the above example, CHAN = 0*er*0011(binary)

Where:

e	=	the RXIE bit of the CSR
r	=	the MASTER.RESET bit (which would be 0)
0011	=	channel number 3

NOTE

1. **Not all register bits are used. In a write action, all unused bits must be written as 0s. In a read action, unused bits are undefined.**

2. **Read-modify-write instructions may be used on all registers except CSR and RBUF.**

3.2.2 Register Bit Definitions

Registers which are modified by reset sequences are coded as shown in Figure 3-1.

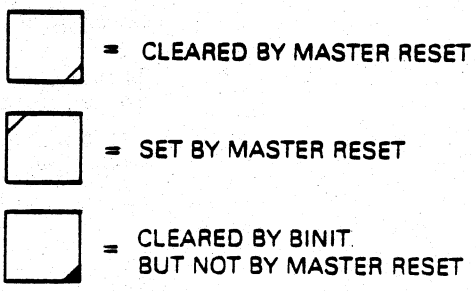
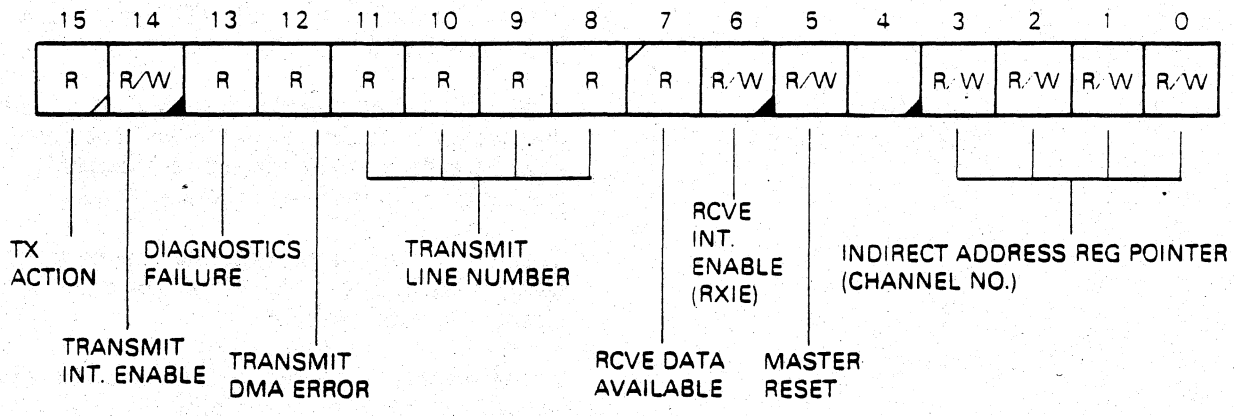


Figure 3-1 Register Coding

3.2.2.1 Control And Status Register (CSR) –

CSR (BASE)



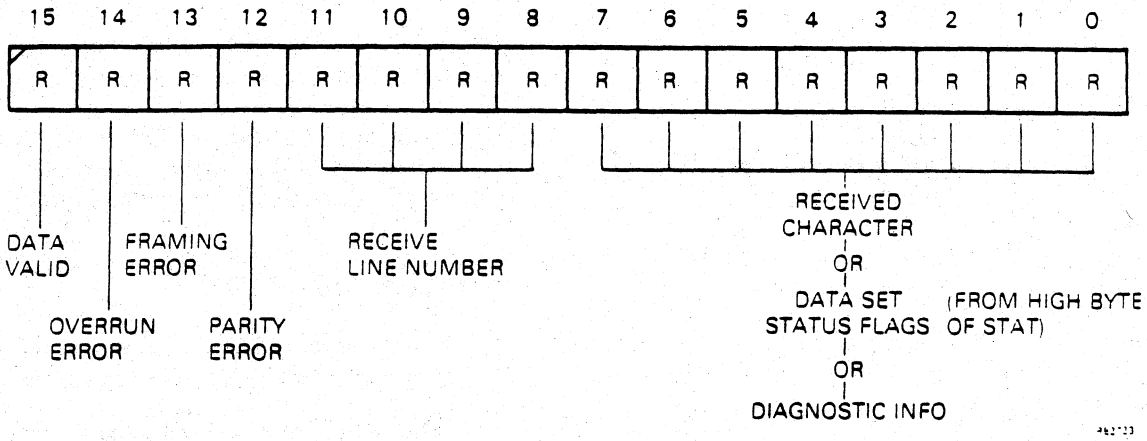
Bit	Name	Description
15	TX.ACTION (Transmitter Action) (R)	This bit is set by the DHQ11 when: 1. The last character of a DMA buffer has left the OCTART. 2. A DMA transfer has been aborted. 3. A DMA transfer has been terminated by the DHQ11 because non-existent memory has been addressed, or because of a host memory parity error. 4. A single-character programmed output has been accepted; that is to say, the character has been taken from TX.CHAR.

Bit	Name	Description
		The bit is cleared if the host reads the CSR after the TX.ACTION FIFO has become empty. To avoid losing TX.ACTION reports, the host must not let more than 16 reports accumulate. It is advisable to read the CSR until TX.ACTION becomes clear.
		NOTE **TX.ACTION reports may be lost if the upper byte of the CSR is discarded following a read of the CSR.**
14	TXIE (Transmit Interrupt Enable) (R/W)	When set, this bit allows the DHQ11 to interrupt the host when CSR<15> (TX.ACTION) becomes set. It is cleared by BINIT, but not by MASTER.RESET.
13	DIAG.FAIL (Diagnostic Fail) (R)	When set, this bit indicates that the DHQ11 internal diagnostics have detected an error. The error may have been detected by the self-test sequencer or by the background monitor program (BMP). This bit is associated with the diagnostic-passed LED. When it is set, the LED will be off. When it is cleared, the LED will be on. The bit is set by MASTER.RESET. It is cleared after the self-test has run successfully. Not valid if MASTER.RESET is set.
12	TX.DMA.ERROR (Transmit DMA Error) (R)	If this bit is set and TX.ACTION is also set, either the channel indicated by CSR<11:8> has failed to transfer DMA data within 10 microseconds of the bus request being acknowledged, OR there is a host memory parity error. The TBUFFAD1 and TBUFFAD2 registers will contain the address of the memory location at which the error occurred. TBUFFCT will be cleared.
<11:8>	TX.LINE (Transmit Line Number) (R)	If TX.ACTION is set, these bits hold the line number to which TX.ACTION refers.

Bit	Name	Description
7	RX.DATA.AVAIL (Received Data Available) (R)	When set, this bit indicates that a received character is available. It is clear when the receive FIFO is empty. It is used to request a receive interrupt. It is set after MASTER.RESET because the receive FIFO contains diagnostic information.
6	RXIE (Receiver Interrupt Enable) (R/W)	When set, this bit allows the DHQ11 to interrupt the host when RX.DATA.AVAIL is set. An interrupt is generated under the following conditions. 1. RXIE is set and a character is placed into an empty receive FIFO. 2. The receive FIFO contains one or more characters, and RXIE is changed from 0 to 1. It is cleared by BINIT but not by MASTER.RESET.
5	MASTER.RESET (Master Reset) (R/W)	This bit is set by the host to reset the module. It stays set while the DHQ11 runs the self-test and performs an initialization sequence. The bit is then cleared to tell the host that the process is complete. This bit can be set directly by the host, or indirectly by BINIT (bus initialization signal).
<3:0>	IND.ADDR.REG (Indirect Address Register) (R/W)	For indexed registers, these bits select one of eight channels.

3.2.2.2 Receive Buffer (RBUF) – A read from 'base + 2' is interpreted by the DHQ11 hardware as a read from the receive FIFO. Therefore RBUF is a 256-character register with a 1-word address. The least-significant bit (LSB) of the character is in bit 0.

RBUF (READ BASE + 2)



Bit	Name	Description
15	DATA.VALID (Data Valid) (R)	This bit is set if there is data in the receive FIFO. When this bit is clear, the contents of RBUF<14:0> is not valid. After self-test, diagnostic information is loaded into the receive FIFO. Therefore, this bit is always set after a successful master reset sequence.
14	OVERRUN.ERR (Overrun Error) (R)	This bit is set if one or more previous characters of the channel indicated by bits <11:8> were lost because of a full receive FIFO.

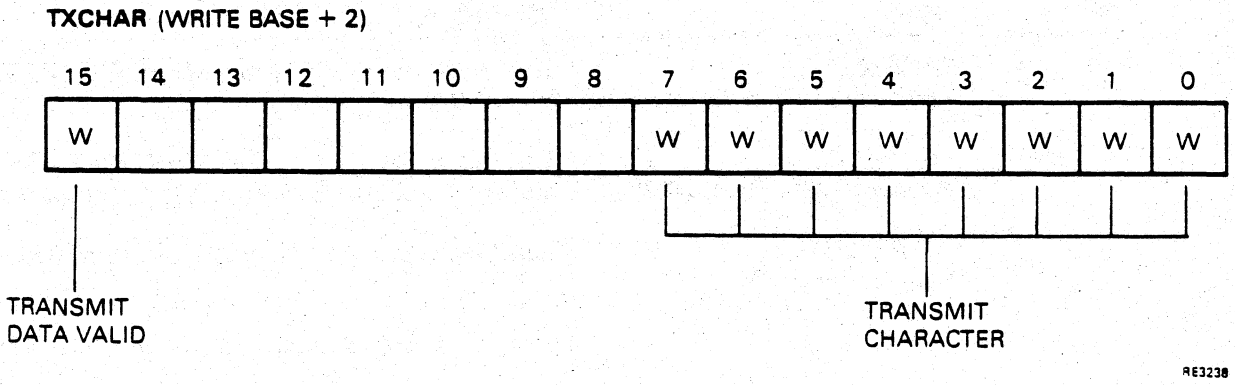
NOTE

The 'all 1s' code for bits <14:12> is reserved. This code indicates that RBUF<7:0> holds modem status or diagnostic information.

13	FRAME.ERR (Framing Error) (R)	This bit is set if the first stop bit of the received character was not detected (also see RX.CHAR).
12	PARITY.ERR (Parity Error) (R)	This bit is set if this character has a parity error, and if parity is enabled for the channel indicated by bits <11:8> (also see RX.CHAR).

Bit	Name	Description
<11:8>	RX.LINE (Receive Line Number) (R)	These bits hold the binary number of the channel on which the character of RBUF<7:0> was received, or on which a data-set change was reported.
<7:0>	RX.CHAR (Received Character) (R)	If RBUF<14:12> = 000, these eight bits contain the oldest character in the receive FIFO. The character is good. If RBUF<14:12> = 001, 010, or 011, these eight bits contain the oldest character in the receive FIFO. The character is bad. If RBUF<14:12> = 111, these eight bits contain diagnostic or modem status information. In this case, RBUF<0> has the following meanings. 0 = Modem status in RBUF<7:1> 1 = Diagnostic information in RBUF<7:1> If there is an overrun condition, the four-character UART receive buffer for that channel will be cleared. This data will be lost. A null character is placed in the receive FIFO, and RBUF<14> is set. The DHQ11 does not have a break-detect bit. A line break is indicated to the program as a null character with FRAME.ERR set, and overrun is clear.

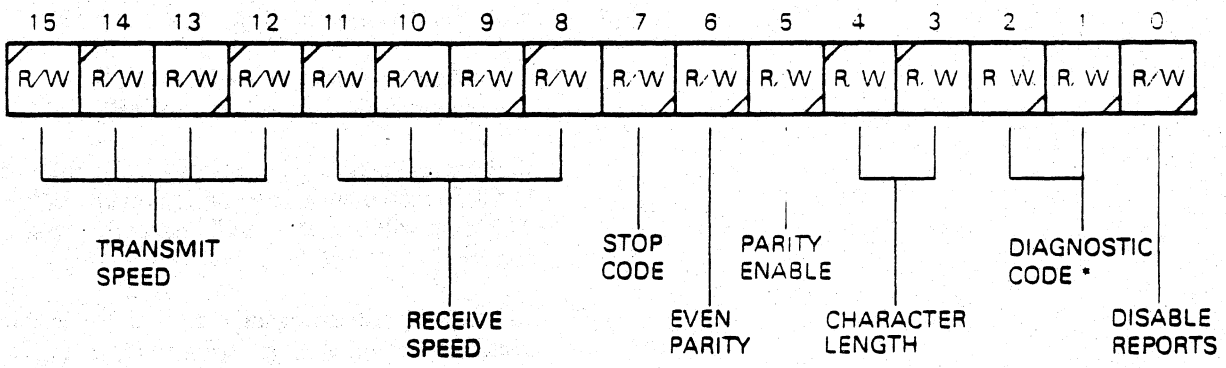
3.2.2.3 Transmit Character Register (TXCHAR) – Single-character programmed transfers are made through the transmit character register.



Bit	Name	Description
15	TX.DATA.VALID (Transmit Data Valid) (W)	When set, this bit instructs the DHQ11 to transmit the character held in bits <7:0>. The bit is sensed by the DHQ11, which then transfers the character, clears the bit, and sets TX.ACTION. TX.DATA.VALID and TX.CHAR can be written together, or by separate MOVB instructions.
<7:0>	TX.CHAR (Transmit Character) (W)	This contains the character to be transmitted. The LSB is bit 0.

3.2.2.4 Line-Parameter Register (LPR) – This register is used to configure its associated channel.

LPR (BASE + 4)



* 00 = NORMAL OPERATION
01 = SCREEN RECEIVED XON/XOFF CHARACTERS FROM ENTRY INTO RECEIVER BUFFER IF 0 AUTO IS SET

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Bit	Name	Description
<15:12>	TX.SPEED (Transmitted Data Rate) (R/W)	This bit is set to 1101 by MASTER.RESET (9600 bits/s). It defines the transmit data rate (Table 3-2).
<11:8>	RX.SPEED (Received Data Rate) (R/W)	This bit is set to 1101 by MASTER.RESET (9600 bits/s). It defines the receive data rate (Table 3-2).
7	STOP.CODE (Stop Code) (R/W)	This bit defines the length of the transmitted stop bit. 0 = 1 stop bit for 5-, 6-, 7-, or 8-bit characters 1 = 2 stop bits for 6-, 7-, or 8-bit characters, or 1.5 stop bits for 5-bit characters

Bit	Name	Description
		The bit is cleared by MASTER.RESET.
6	EVEN.PARITY (Even Parity) (R/W)	If LPR<5> is set, this bit defines the type of parity. 1 = Even parity 0 = Odd parity The bit is cleared by MASTER.RESET.
5	PARITY.ENAB (Parity Enable) (R/W)	This bit causes a parity bit to be generated on transmit, and checked and stripped on receive. 1 = Parity enabled 0 = Parity disabled The bit is cleared by MASTER.RESET.
<4:3>	CHAR.LGTH Character Length) (R/W)	These two bits define the length of characters. The length does not include start, stop, and parity bits. 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits They are set to 11 by MASTER.RESET.
<2:1>	DIAG (Diagnostic Code) (R/W)	Diagnostic control codes are are used by the host as follows. 00 = Normal operation 01 = Causes the background monitor program (BMP) to report the DHQ11 status through the receive FIFO. Other codes are reserved.
<0>	DISAB.XRPT (Disable XON/XOFF Reporting) (R/W)	0 = XON and XOFF characters are reported on all channels. 1 = If LNCTRL<4> is also set for a particular channel, these characters are filtered from the received data stream, to relieve the host of the need to do so.

Bit	Name	Description
		On initialization, this bit is cleared. In order to read or write to this bit, CSR<3:0> must equal zero.

NOTE

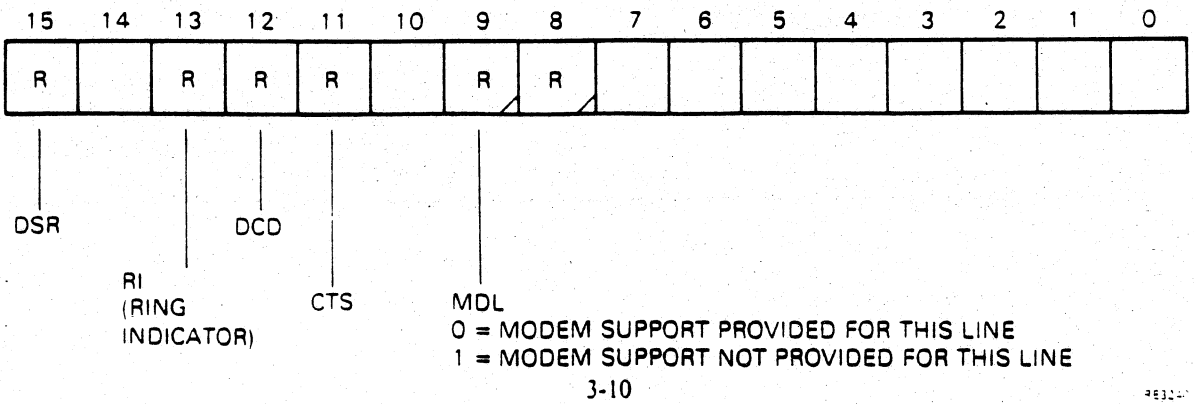
An XON code = 21_8 = DC = CTRL/Q. An XOFF code = 23_8 = DC3 = CTRL/S. No other codes are specified for the interface.

Table 3-2 Data Rates

Code	Data Rate (Bits/s)	Maximum Error (%)
0000	50	0.01
0001	75	0.01
0010	110	0.08
0011	134.5	0.07
0100	150	0.01
0101	300	0.01
0110	600	0.01
0111	1200	0.01
1000	1800	0.01
1001	2000	0.19
1010	2400	0.01
1011	4800	0.01
1100	7200	0.01
1101	9600	0.01
1110	19200	0.01
1111	38400	0.01

3.2.2.5 Line-Status Register (STAT) – The high byte of this register holds modem status information. The low byte is undefined.

STAT (READ BASE+6)



Bit	Name	Description
15	DSR (Data Set Ready) (R)	This bit gives the present status of the Data Set Ready (DSR) signal from the modem. 1 = ON 0 = OFF
		NOTE **In order to report a change of modem status, the DHQ11 writes the high byte of STAT into the low byte of RBUF. RBUF<14:12> = 111 indicates to the host that RBUF<7:0> holds modem status information instead of a received character.**
13	RI (Ring Indicator) (R)	This bit gives the present status of the Ring Indicator (RI) signal from the modem. 1 = ON 0 = OFF
12	DCD (Data Carrier Detected) (R)	This bit gives the present status of the Data Carrier Detected (DCD) signal from the modem. 1 = ON 0 = OFF
11	CTS (Clear to Send) (R)	This bit gives the present status of the Clear To Send (CTS) signal from the modem. 1 = ON 0 = OFF

Bit	Name	Description
9	MDL (MDL Modem Support Low) (R)	Always reads as 0 for DHQ11, to indicate that the module has modem support capability.

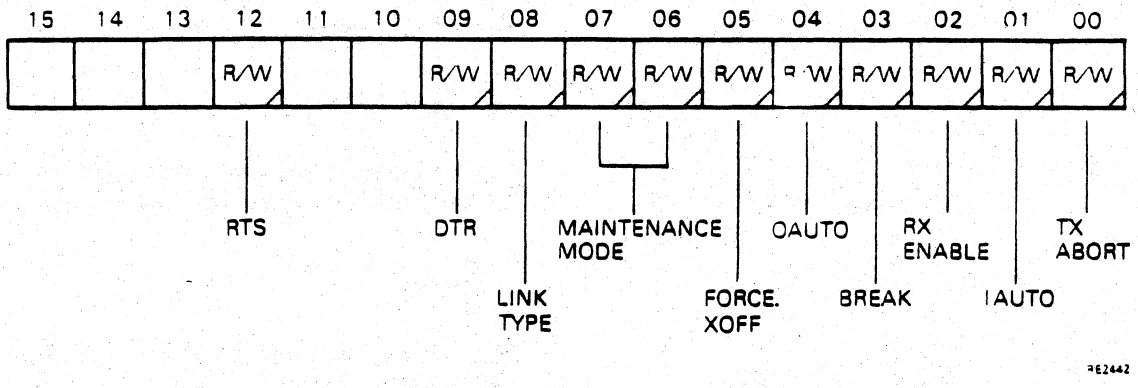
NOTE

It is only necessary to read the modem support status for one line, since all the other lines will have the same setting.

8	Reserved	This bit is set to zero on factory-issued boards.

3.2.2.6 Line-Control Register (LNCTRL) – The main function of this register is to control the line interface.

LNCTRL (BASE + 10)



Bit	Name	Description
12	RTS (Request To Send) (R/W)	This bit controls the Request To Send (RTS) signal. 1 = ON 0 = OFF
9	DTR (Data Terminal Ready) (R/W)	This bit controls the Data Terminal Ready (DTR) signal. 1 = ON 0 = OFF

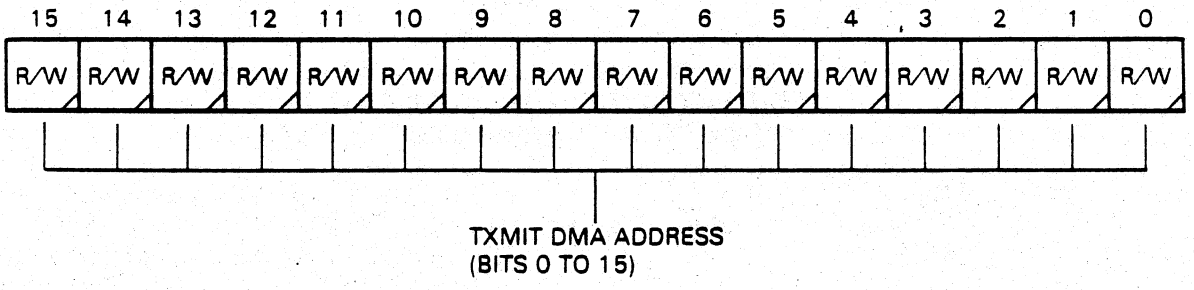
Bit	Name	Description
8	LINK.TYPE (Link Type) (R/W)	This bit must be set if the channel is to be connected to a modem. When the bit is set, any change in modem status will be reported through the receive FIFO as well as the STAT register. If this bit is cleared, this channel becomes a 'data-leads-only' channel. Modem status information is loaded in the high byte of STAT, but is not placed in the receive FIFO.
<7:6>	MAINT (Maintenance Mode) (R/W)	These bits can be written by the driver or test programs, in order to test the channel. The coding is as follows: 00 = Normal operation 01 = Automatic echo mode — Received data is looped back to the terminal (regardless of the state of TX.ENA) at the data rate selected for the receiver. The received characters are processed normally and placed in the receive FIFO. Any data that the host attempts to transmit on this channel will be discarded by the OCTART. The RX.ENA bit must be set when operating in this mode. 10 = Local loopback — Data transmitted by the host is looped back to the receive buffer. Data received from the terminal is ignored, and the transmit data line to the terminal is held in the mark condition. The data rate selected for the transmitter is used for both transmission and reception. The TX.ENA bit still controls transmission in this mode. The RX.ENA bit is ignored. 11 = Remote loopback — In this mode, data received from the terminal is looped back to the terminal at a clock rate equal to the received clock rate. The data is not placed in the receive FIFO. The state of TX.ENA is ignored. The RX.ENA bit must be set on this channel.

Bit	Name	Description
5	FORCE.XOFF (Force XOFF) (R/W)	This bit can be set by the program to indicate that this channel is congested at the host system (for example, if the typeahead buffer is full). When it sees this bit set, the DHQ11 will send an XOFF code. Until the bit is cleared, XOFFs will be sent after every alternate character received on this channel. When the bit is cleared, an XON will be sent unless IAUTO is set and the receive FIFO is critical.
4	OAUTO (Outgoing Auto Flow) (R/W)	This bit is the auto-flow control bit for outgoing characters. When set, if RX.ENA is also set, the DHQ11 will automatically respond to XON and XOFF codes received from a channel. The DHQ11 uses the TX.ENA bit in TBUFFAD2 to stop and start the flow. If DISAB.XRPT is also set, XON XOFF codes are not entered in the receive FIFO.
3	BREAK (Break Control) (R/W)	If set, this bit forces the transmitter of this channel to the spacing state. If this bit is set while a character is being transmitted, transmission is completed before break is asserted on the line. Transmission is re-enabled when the bit is cleared. **NOTE** **If the line is idle, there may be a delay of up to 170 microseconds between writing the bit and the channel changing state. If a character is already being transmitted by the OCTART, the BREAK signal will be transmitted immediately afterwards.**
2	RX.ENA (Receiver Enable) (R/W)	If this bit is set, this receiver channel is enabled. If this bit is cleared when this channel is assembling a character, that character is lost. The bit is cleared by MASTER.RESET.
1	IAUTO (Incoming Auto Flow) (R/W)	This is the auto-flow control bit for incoming characters. If it is set, the DHQ11 will control incoming characters by transmitting XON and XOFF codes.

Bit	Name	Description
		If the receive FIFO becomes more than three-quarters full, the DHQ11 will send an XOFF code to that channel, and to any other channel which receives a character and has the IAUTO bit set. When FIFO becomes less than half full, an XON will be sent to all channels which had previously been sent an XOFF.
0	TX.ABORT (Transmit Abort) (R/W)	This bit is set by the driver program to halt data transmission. If a DMA transfer was in progress, the DMA address and count registers (TBUFFAD1, TBUFFAD2, and TBUFFCT) will be updated to reflect the number of characters which have been transmitted. The transfer can be continued by clearing TX.ABORT, and then setting TX.DMA.START in TBUFFAD2. No characters will be lost. If DMA is not in progress, no action is taken. When an abort sequence has been completed, the DHQ11 will set the TX.ACTION bit in the CSR. If the transmitter interrupt is enabled, the program will be interrupted at the transmit vector. The program must make sure that TX.ABORT is clear before setting TX.DMA.START, otherwise the transfer will be aborted before any characters are transmitted. The bit is cleared by MASTER.RESET.

3.2.2.7 Transmit Buffer Address Register Number 1 (TBUFFAD1) –

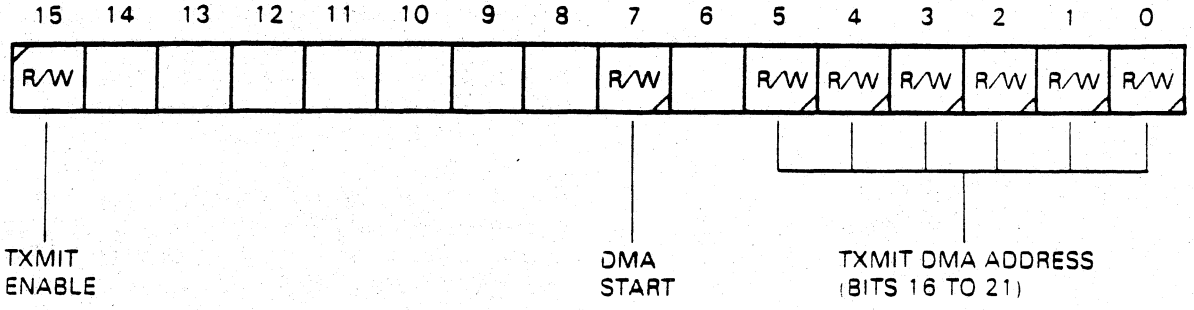
TBUFFAD1 (BASE + 12)



Bit	Name	Description
<15:0>	TBUFFAD<15:0> (Transmit Buffer Address [Low]) (R/W)	Bits <15:0> of the DMA address.

3.2.2.8 Transmit Buffer Address Register Number 2 (TBUFFAD2) –

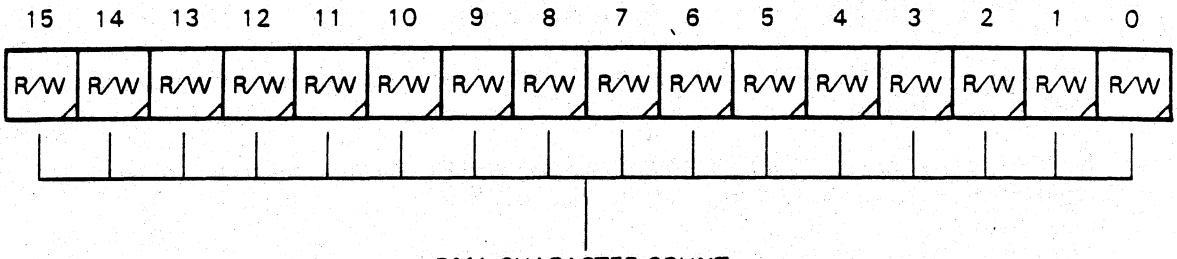
TBUFFAD2 (BASE + 14)



Bit	Name	Description
15	TX.ENA (Transmitter Enable) (R/W)	When this bit is set, the DHQ11 will transmit all characters. When this bit is cleared, the DHQ11 will only transmit **internally** generated flow-control characters. The bit is set by MASTER.RESET. In the OAUTO mode, this bit is used by the DHQ11 to control outgoing characters.
7	TX.DMA.START (Transmit DMA Start) (R/W)	This bit is set by the host to start a DMA transfer. The DHQ11 will clear the bit before returning TX.ACTION. The bit is cleared by MASTER.RESET.
	NOTE **After setting this bit, the host must not write to TBUFFCT, TBUFFAD1, or TBUFFAD2 <7:0> until the TX.ACTION report has been returned.**	
<5:0>	TBUFFAD<21:16> (Transmit Buffer Address [High]) (R/W)	Bits <21:16> of the DMA address. Before a DMA transfer, TBUFFAD1 and the low byte of TBUFFAD2 are loaded with the start address of the DMA buffer. This address will be continuously changing during a DMA transfer and has no meaning. Once TX.ACTION has been returned, the register contains the final DMA transfer address.

3.2.2.9 Transmit DMA Buffer Counter (TBUFFCT) –

TBUFFCT (BASE + 16)



Bit	Name	Description
<15:0>	TX.CHAR.CT (Transmit Character Count) (R/W)	This word is loaded with the number of characters to be transferred by DMA. The number of characters is specified as a 16-bit unsigned integer. After a DMA transfer has been aborted, this location will hold the number of characters still to be transferred. See also the previous NOTE.

3.3 PROGRAMMING FEATURES

3.3.1 Initialization

The DHQ11 is initialized by its on-board sequencers.

Initialization takes place after a bus reset sequence, or when the host sets CSR<5> (MASTER.RESET).

Before starting initialization, the on-board sequencers perform a self-test. The results of this test are reported by eight diagnostic bytes in the receive FIFO.

The DHQ11 state, after a successful self-test, is as follows.

1. Eight diagnostic codes are placed in the receive FIFO
2. The diagnostic fail bit (CSR<13>) is clear
3. All channels are set for:
   a. Send and receive 9600 bits s
   b. Eight data bits
   c. One stop bit
   d. No parity
   e. Parity odd
   f. Auto-flow off
   g. Receive disabled
   h. Transmit enabled
   i. No break on line
   j. No loopback
   k. Link type set to data-leads-only
   l. DTR and RTS off
   m. DMA character counter zero
   n. DMA start address registers zero
   o. TX.DMA.START cleared
   p. TX.ABORT cleared
   q. Auto-flow reports enabled

The DHQ11 clears the MASTER.RESET bit (CSR<5>) when initialization and self-test are complete.

3.3.2 Configuration

After DHQ11 self-initialization, the driver program can configure the DHQ11 as needed. This is done through the LPR and LNCTRL registers.

The line characteristics for a channel can be set up by writing to the LPR and LNCTRL registers associated with this channel. These are:

- Transmit speed
- Receive speed
- Number of stop bits
- Parity type or parity disabled
- Character length
- Flow-control characteristics
- Normal or maintenance mode
- Receiver enable/disable
- Modem or data-leads-only

NOTE

If RX.ENA is reset while a received character is being assembled, that character will be lost.

3.3.3 Transmitting

Each DHQ11 channel can be set up to transfer the characters by DMA or under program control.

3.3.3.1 DMA Transfers – Before setting up the transfer of a DMA buffer, the program should make sure that TX.DMA.START is not set. TBUFFCT, TBUFFAD1, and TBUFFAD2 should not be written unless TX.DMA.START is clear.

Transmission will start when the program sets TX.DMA.START. The size of the DMA buffer, and its start address, can be written to TBUFFCT, TBUFFAD1, and TBUFFAD2 in any order, provided that the TX.DMA start bit (TBUFFAD2<7>) is not set. However, TBUFFAD2 contains TX.ENA and TX.DMA.START, so it is probably simpler to write TBUFFAD2 last. By using byte operations on this register, TX.ENA and TX.DMA.START can be separated.

The DHQ11 will perform the transfer, and set TX.ACTION when it is complete. If TXIE is set, the program will be interrupted at the transmit vector. Otherwise, TX.ACTION must be polled. TX.ACTION is not returned until the UART has completely transmitted the last character of the DMA buffer.

To abort a DMA transfer, the program must set TX.ABORT. The DHQ11 will stop transmission, and update TBUFFCT, TBUFFAD1, and TBUFFAD2<7:0> to reflect the number of characters which have been transmitted. TX.DMA.START will be cleared. If TXIE is set, TX.ACTION will interrupt the program at the transmit vector. If the program clears TX.ABORT and sets TX.DMA.START, the transfer can be continued without loss of characters.

If a DMA transfer fails because of a host memory error, the transmission will be terminated. TBUFFAD1 and TBUFFAD2 will point to the failing location. TBUFFCT will be cleared.

3.3.3.2 Programmed I/O – Single characters are transferred through the channel TX.CHAR register. The character and the DATA.VALID bit must be written as defined in Section 3.2.2.3. Note that the character and the DATA.VALID bit can be written by separate MOVB instructions.

When the DHQ11 removes the character from TX.CHAR, it returns TX.ACTION. This will generate an interrupt if TXIE is set.

NOTE

In single-character mode, TX.ACTION is returned when the DHQ11 accepts the character, not when it has been transmitted. Each channel can buffer up to three characters. Therefore, if line parameters are changed immediately after the last TX.ACTION of a message, the end of the message could be lost unless three null characters are added to the end of each single-character programmed transfer message.

3.3.4 Receiving

Received characters, tagged with the channel number, error information and DATA.VALID, are placed in the receive FIFO. RX.DATA.AVAIL is clear when the receive FIFO is empty. When a character is put into the empty receive FIFO, the DHQ11 sets RX.DATA.AVAIL. A receive interrupt is generated if RXIE is set. RX.DATA.AVAIL stays set while there is valid data in the receive FIFO. It is recommended that the receive character routine continues to read characters from the receive FIFO until DATA.VALID is clear.

NOTE

The interrupt is dynamic. It is raised as RX.DATA.AVAIL is set after RXIE, or as RXIE is set after RX.DATA.AVAIL. If the interrupt routine does not empty the receive FIFO, RXIE must be toggled to raise another interrupt.

If RXIE is not set, the program must poll RBUF often enough to prevent data loss.

3.3.5 Interrupt Control

The DHQ11 provides one of two vector addresses during a bus interrupt sequence. The receive vector address is the address set up on the vector address switches. The transmit vector address is the receive vector address + 4.

The receive interrupt vector is generated when:

- RXIE is set and a character is placed into an empty receive FIFO
- RXIE is changed from 0 to 1, and the receive FIFO contains one or more characters.

The transmit interrupt vector is generated when:

- TXIE is set and TX.ACTION becomes set
- TXIE is changed from 0 to 1 while TX.ACTION is set

NOTE

Up to 16 TX.ACTION reports are buffered. It is therefore recommended that your program reads the CSR until the TX.ACTION bit becomes clear, otherwise TX.ACTION will be lost.

At the two vectors, the host must provide the addresses of suitable routines to deal with the above conditions.

3.3.6 Auto XON And XOFF

XON and XOFF characters are commonly used to control data flow on communications channels. To use this facility, interfaces must have suitable decoding hardware or software.

A channel using flow control that receives an XOFF stops sending characters until it receives an XON.

If the receive FIFO becomes more than three-quarters full, the DHQ11 will send an XOFF code to that channel, and to any other channel which receives a character and has the IAUTO bit set. When FIFO becomes less than half full, an XON will be sent to all channels which had previously been sent an XOFF.

The DHQ11 automatically controls character flow when programmed accordingly (auto-flow). Four bits control this function:

- IAUTO — LNCTRL<1>
- FORCE.XOFF — LNCTRL<5>
- OAUTO — LNCTRL<4>
- DISAB.XRPT — LPR<0>

IAUTO and FORCE.XOFF both control incoming characters. IAUTO is an enable bit which allows the level of the receive FIFO to control the generation of XOFF and XON characters. The FORCE.XOFF bit is a direct command from the program to control the incomimg data stream.

3.3.6.1 IAUTO – The DHQ11 hardware recognizes when the receive FIFO is three-quarters full and half full. The logic uses these states for auto-flow control.

Each channel has a separate IAUTO bit. If there are 191 or more characters in the receive FIFO, and a character is received on a channel with IAUTO set, an XOFF character is sent. If the channel does not respond to the XOFF, the DHQ11 will send another XOFF in response to every alternate character received. An XON will be sent when the receive FIFO contains less than 128 characters, unless the FORCE.XOFF bit for that channel is set. XONs are only sent to channels to which an XOFF has previously been sent.

By inserting XON and XOFF characters into the data stream, the program can perform flow control directly. However, if the DHQ11 is in IAUTO mode, the results will be unpredictable.

In IAUTO mode, if RX.ENA is set, XON and XOFF characters will be transmitted even if TX.ENA is cleared.

3.3.6.2 **FORCE.XOFF** – When FORCE.XOFF is set, the DHQ11 sends an XOFF and then acts as if IAUTO is set and the receive FIFO is critical (was three-quarters full, and is not yet less than half full). When FORCE.XOFF is reset, an XON will be sent unless the receive FIFO is critical and IAUTO is set.

3.3.6.3 **OAUTO** – If the program sets OAUTO, the DHQ11 will automatically respond to XON and XOFF characters from the channel. It does this by clearing or setting the TX.ENA bit.

The program may also control the TX.ENA bit, so in this case it is important to keep track of received XON and XOFF characters.

Received XON and XOFF characters will always be reported through the receive FIFO, unless the DISAB.XRPT bit is set. It is possible, during read-modify-write operations by the program, for the DHQ11 to change the TX.ENA bit between the read and the write actions. For this reason, if DMA transfers are started while OAUTO is set, it is advisable to write to the low byte of TBUFFAD2 only.

3.3.6.4 **DISAB.XRPT** – If DISAB.XRPT is clear, XON and XOFF characters will be processed as normal characters and are entered into the receive FIFO. DISAB.XRPT allows the individual line OAUTO bits to control whether XON or XOFF characters received on that channel are discarded. When DISAB.XRPT is set and OAUTO is set, this filtering is enabled.

NOTES

1. **When checking for flow-control characters, the DHQ11 only checks characters which do not contain transmission errors. The parity bit is stripped, and the remaining bits are checked for XON (21_8) and XOFF (23_8) codes.**

2. **Auto flow-control does not absolutely guarantee that overrun errors will not occur. These errors may still occur if the transmitting devices do not respond to the XOFF immediately.**

3.3.7 Error Indication

Four bits inform the program of transmission and reception errors.

- TX.DMA.ERR — CSR<12>.

- PARITY.ERR — RBUF<12>.
- FRAME.ERR — RBUF<13>.
- OVERRUN.ERR — RBUF<14>.

RBUF<14:12> also identify a diagnostic or modem status code.

3.3.8 Modem Control

Each channel of the module provides modem control bits for RTS and DTR. Also on each channel are modem status inputs CTS, DSR, RI, and DCD. These bits are used for modem control (see Section 3.2.2.5).

CTS, DSR, and DCD are sampled every 10 ms. Therefore, for a change to be detected, these bits must stay steady for at least 10 ms. RI is also sampled every 10 ms, but a change is not reported unless the new state is held for three consecutive samples. Modem signals must be coordinated under program control; there is no hardware modem control logic. Modem status change reports are placed in the receive FIFO only if LINK.TYPE is set, but any changes are updated in STAT irrespective of the state of LINK.TYPE.

Appendix A gives more details of modem control.

By clearing LINK.TYPE, a channel is selected as a 'data-lines only' channel. Modem control and status bits can still be managed by the program, but status bits must be polled at the line-status register. Changes of modem status will **not** be reported to the program.

Status change reporting is done through the receive FIFO as follows.

- When OVERRUN.ERR, FRAME.ERR, and PARITY.ERR are all set, the eight low-order bits contain either status change or diagnostic information. In this case:
- If RBUF<0> = 0, RBUF<7:1> holds STAT<15:9> (see Section 3.2.2.5)
- If RBUF<0> = 1, RBUF<7:1> holds diagnostic information (see Section 3.3.10).

3.3.9 Maintenance Programming

The host can set bits 7 and 6 of LNCTRL to allow each channel to be configured in normal, automatic echo, local loopback, and remote loopback modes. These modes allow an individual data channel to be looped back to the host, or to be looped back to the terminal to assist in isolating communication problems.

The host must provide suitable software to use these modes.

3.3.10 Diagnostic Codes

3.3.10.1 Self-Test Diagnostic Codes – After bus reset or master reset, the DHQ11 executes a self-test and initialization sequence. During the sequence, eight diagnostic codes are put in the receive FIFO, and RX.DATA.AVAIL is set.

After an error-free test, DIAG.FAIL will be reset and the 'diagnostic passed' LED will be on. If an error is detected, DIAG.FAIL will be set and the LED will be off.

3.3.10.2 Interpretation Of Self-Test Codes – The high byte of diagnostic codes in RBUF can be interpreted as in Section 3.2.2.2, except that bits <11:8> are not the line number. They indicate the sequence of the diagnostic byte, that is to say, 0 = first byte, 1 = second byte, and so on. Table 3-3 shows the meaning of each of the error codes.

Table 3-3 DHQ11 Self-Test Error Codes

Code (Octal) bits <7:0>	Test
201	Self-test null code (used as a filler)
211	OCTART error
225	RAM error
231	RTS-CTS-DCD error
235	DTR-RI-DSR error

All other error codes should be treated as an undefined error.

If bit 7 = 0 and bit 0 = 1, then bits <5:2> contain circuit revision information.

Bit 6 always reads 1 for the DHQ11, and indicates that the circuit contains control and OCTART chips.

Bit 1 indicates to which chip the information refers: 0 = Control, 1 = OCTART.

After self-test, the eight FIFO codes consist of six diagnostic codes and two circuit revision codes. If there are less than six errors to report, null codes (201_8) fill the unused places.

After an error-free test, six null codes and two circuit revision codes will be returned.

Self-test may be 'skipped' to shorten the initialization cycle (see Section 3.3.10.3).

The module is still tested, even if self-test is skipped. The reset delay is much shorter, but test coverage is not affected; therefore skipping self-test is advantageous.

After 'skip self-test' self-test, the eight FIFO codes consist of six diagnostic codes and two circuit revision codes. If there are less than six errors to report, 203_8 codes fill the unused places.

After an error-free test, six 203_8 codes and two circuit revision codes will be returned.

3.3.10.3 Skipping Self-Test – The following method is used:

1. The program resets the DHQ11.
2. The program waits 10 ms (± 1 ms) after issuing reset, and then attempts to write 052525_8 to any of the control registers, except the CSR, within the next 4 ms.

3. Following self-test, the DHQ11 hardware checks whether an attempt was made to write the skip code to the registers during the 4 ms window after reset (see step 2 above). If an attempt was made, the MASTER.RESET bit is cleared at 30 ms after issuing a reset instead of 1.2 s. The 1.2 s reset time was retained for compatibility with the DHV11.

NOTE

The program must not write to the CSR, or to the control registers, during the period starting 15 ms after reset, and ending when the MASTER.RESET bit is cleared. Writing during this period could cause a diagnostic fail condition.

3.3.10.4 Background Monitor Program (BMP) – The DHQ11 BMP logic performs background self-tests by checking for OCTART interrupts. One of two codes is returned to the receive FIFO:

1. 305_8 — DHQ11 running
   307_8 — DHQ11 defective (also LED off)

A single diagnostic word is returned to the receive FIFO. The low byte contains the diagnostic code. In the high byte, OVERRUN.ERR, FRAME.ERR, and PARITY.ERR are all set to indicate that bits<7:0> do not hold a normal character. The line number (RBUF<11:8>) = 0.

BMP normally only reports when it finds an error. However, the program can get a BMP report at any time to check the DHQ11. This is done by setting DIAG (LPR <2:1>) of any channel to 01.The line number returned is that of the LPR used to request the report.

On completing the check, BMP clears this 01 code. The host should not write to the LPR of that channel until LPR<2:1> becomes 00.

3.4 PROGRAMMING EXAMPLES

These programs are not presented as the only way of driving the option. and are neither guaranteed nor supported.

3.4.1 Resetting The DHQ11

In the following example:

- DIAGC is a routine to check the diagnostic codes. It returns with CARRY set if it detects an error code.
- The loop at 1S takes 1.2 seconds. so the programmer could poll through a timer or poll at interrupt level zero.

```
;
; A ROUTINE TO RESET THE DHQ11 AND CHECK THAT IT IS FUNCTIONING
; CORRECTLY.
;

DHQRES::
        MOV     #40,@#DHQCSR            ; SET MASTER.RESET AND
                                        ; CLEAR INTERRUPT ENABLES.
1$:     BIT     #40,@#DHQCSR            ; WAIT FOR MASTER.RESET TO
        BNE     1$                      ; CLEAR.
        BIT     #20000,@#DHQCSR         ; CHECK THE DIAGNOSTICS
        BNE     DIAGER                  ; FAIL BIT.
                                        ; NOTE: TEST INSTRUCTION IS
                                        ; OK BECAUSE THERE ARE
                                        ; NO TRANSMIT.ACTS PENDING.
        MOV     #8.,R5                  ; SET UP A COUNT.
                                        ;
2$:     MOV     @#RBUFF,R0              ; GET NEXT DIAGNOSTIC CODE.
        JSR     PC,DIAG                 ; PROCESS IT.
        BCS     DIAGER                  ; CARRY SET - MUST HAVE
                                        ; BEEN AN ERROR.
        SOB     R5,2$                   ; GO BACK FOR NEXT CODE.

        RTS     PC                      ; RETURN - CARD IS RESET.

;
; DHQ11 HAS FAILED TO RESET PROPERLY, SO HALT AND WAIT FOR
; THE FIELD SERVICE ENGINEER.
;

DIAGER: HALT
        BR      DIAGER
```

3.4.2 Configuration

This routine sets the characteristics of channel 1 as follows:

1. Transmit and receive at 300 bits/s
2. Seven data bits with even parity and one stop bit
3. Transmitters and receivers enabled
4. No modem control
5. No automatic flow control.

```
SETUP::
        MOV     #1,@#DHQCSR             ; LOAD INDEX REG
                                        ; WITH CHANNEL NO.
        MOV     #052560,@#LPR           ; DATA RATE, STOP BITS,
                                        ; PARITY AND LENGTH.
        MOV     #4,@#LNCTRL             ; ENABLE THE RECEIVER.
        MOVB    #200,@#TBFAD2+1         ; ENABLE THE TRANSMITTER.

        RTS     PC                      ; RETURN - CHANNEL 1 DONE.
```

3.4.3 Transmitting

3.4.3.1 Single-Character Programmed Transfer – This is a program to send a message on channel 1. The message (MESG) is an ASCII string with a null character as terminator.

Polling is used, but a TX.ACTION interrupt could also be used.

This program would function on a DHQ11 with only this channel active. Otherwise it would lose TX.ACTION reports of other channels. However, a program to control all channels would be too big to use as an example.

```
;
; A ROUTINE TO WRITE A MESSAGE TO CHANNEL 1 USING SINGLE-CHARACTER
; MODE.
;

SINGOT::
        MOV     #1,@#DHQCSR             ; LOAD INDEX REG WITH
                                        ; CHANNEL NO.
        MOV     #MESG,R0                ; POINT TO MESSAGE.
1$:
        MOVB    (R0)+,@#TXCHAR          ; MOVE CHARACTER TO TRANSMIT
                                        ; BUFFER.
        BEQ     3$                      ; GO RETURN IF ALL CHARACTERS
                                        ; GONE.
        MOVB    #200,@#TXCHAR+1         ; SET DATA VALID BIT TO START.
2$:
        MOV     @#DHQCSR,R1             ; WAIT FOR TX.ACT
        BPL     2$

        BIC     #174377,R1              ; ISOLATE CHANNEL NUMBER.
        CMP     #000400,R1
TXI     BNE     2$                      ; IGNORE THE TX.ACT IF IT IS
                                        ; NOT OURS (SHOULD NOT HAPPEN).
        BR      1$                      ; GO BACK FOR NEXT CHARACTER.

3$:
        RTS     PC                      ; MESSAGE SENT.

MESG:   .ASCIZ /A SINGLE-CHARACTER MESSAGE FOR CHANNEL 1/
```

3.4.3.2 DMA Transfer –

```
;
; THIS PROGRAM SENDS A MESSAGE OUT ON EACH LINE OF  THE  DHQ11  AND
; HALTS THE MACHINE WHEN ALL TRANSMISSIONS HAVE COMPLETED.
;
; THE MESSAGES ARE TRANSMITTED USING DMA MODE,  AND INTERRUPTS  ARE
; USED TO SIGNAL TRANSMISSION COMPLETION.
;

DMAINT::
        MOV     #TXINT,@#TXVECT  ; SET UP THE INTERRUPT VECTORS.
        MOV     #200,@#TXPSW     ; INTERRUPT PRIORITY FOUR.
        MOV     #8.,R0           ; EIGHT LINES TO START.
        CLR     R1               ; START AT LINE ZERO.
1$:
        MOVB    R1,@#DHQCSR      ; SELECT THE REGISTER BANK.
        MOV     #DMASIZ,@#TBFCNT ; SET LENGTH OF MESSAGE.
        MOV     #DMAMES,@#TBFAD1 ; SET LOWER 16 ADDRESS BITS.
        MOV     #100200,@#TBFAD2 ; START DMA WITH TRANSMITTER
                                 ; ENABLED (ASSUME UPPER ADDRESS
                                 ; BITS ARE ZERO).
        INC     R1               ; POINT TO NEXT CHANNEL.
        SOB     R0,1$            ; REPEAT FOR ALL LINES.

        CLR     R5               ; R5 IS USED BY INTERRUPT ROUTINE.
        MOVB    #100,@#DHQCSR+1  ; ENABLE TRANSMITTER INTERRUPTS.
2$:
        CMP     #8.,R5           ; WAIT FOR ALL LINES TO FINISH.
        BNE     2$
3$:
        HALT                     ; ALL DONE, SO STOP.
        BR      3$


;
; TRANSMITTER INTERRUPT ROUTINE.
;
; R5 IS INCREMENTED AS EACH LINE COMPLETES.
;

TXINT::
        MOV     @#DHQCSR,R0 ; GET LINE NUMBER OF FINISHED LINE.
        BIT     #100000,R0  ; CHECK FOR (ANOTHER) TX.ACTION.
        BEQ     4$          ; IF NOT, GO RETURN AND WAIT.

        INC     R5          ; FLAG THAT ANOTHER LINE HAS FINISHED.
        BR      TXINT
4$:
        RTI
5$:
        HALT                ; MEMORY PROBLEM
        BR      5$

DMAMES: .ASCII  <15><12><7><7><7>/SYSTEM CLOSING DOWN NOW/
DMASIZ  =       .-DMAMES
        .EVEN
```

3.4.3.3 Aborting A Transmission –

```
;
; THIS ROUTINE IS CALLED TO ABORT A  TRANSMISSION  (EITHER  DMA  OR
; FIFO)  IN  PROGRESS  ON A SPECIFIED LINE.  THIS ROUTINE MAKES THE
; (RATHER RASH) ASSUMPTION THAT THERE ARE  NO  OTHER  TRANSFERS  IN
; PROGRESS.
;
; ON ENTRY,  R0 CONTAINS THE NUMBER OF THE LINE TO BE ABORTED.
;

TXABRT::
        MOV     R0,@#DHQCSR     ; POINT TO THE CHANNEL TO BE ABORTED.
        BIS     #1,@#LNCTRL     ; SET THE TRANSMIT ABORT BIT.
1$:
        MOV     @#DHQCSR,R1     ; WAIT FOR THE TX.ACT.
        BPL     1$
        SWAB    R1              ; CHECK IT IS OUR LINE.
        BIC     #177760,R1
        CMP     R0,R1
        BNE     1$              ; IGNORE IT IF IT IS NOT (OUR
                                ; ASSUMPTION WAS WRONG!)

        BIC      1,@#LNCTRL     ; CLEAR DOWN THE ABORT FLAG
                                ; FOR NEXT TIME.

        RTS     PC              ; BUFFER COMPLETELY ABORTED.
                                ; IF A DMA WAS IN PROGRESS, THE
                                ; DMA REGISTERS REFLECT WHERE
                                ; THE DHQ11 HAD GOT TO.
```

3.4.4 Receiving

```
;
; THIS ROUTINE PROCESSES RECEIVED CHARACTERS UNDER INTERRUPT
; CONTROL.  IF AN XOFF IS RECEIVED,  THE TRANSMITTER FOR THAT
; CHANNEL IS TURNED OFF.  IF AN XON IS RECEIVED,  THE TRANSMITTER
; IS TURNED BACK ON.  ALL OTHER CHARACTERS ARE IGNORED.
;
; THIS IS JUST AN EXAMPLE.  A BETTER WAY TO PERFORM FLOW CONTROL IS
; TO USE THE AUTOMATIC CAPABILITIES OF THE DHQ11.
;

RXAUTO::
        MOV     #RXINT,@#RXVECT  ; SET UP THE INTERRUPT VECTORS.
        MOV     #200,@#RXPSW     ; INTERRUPT PRIORITY FOUR.
        MOV     #8.,R0           ; ENABLE ALL THE RECEIVERS,
        CLR     R1               ; STARTING AT CHANNEL ZERO,
1$:
        MOVB    R1,@#DHQCSR      ; SELECT THE LINE.
        BIS     #4,@#LNCTRL      ; ENABLE THIS RECEIVER.
        INC     R1               ; SET POINTER TO NEXT CHANNEL.
        SOB     R0,1$

        MOVB    #100,@#DHQCSR    ; ENABLE THE RECEIVER INTERRUPTS.

        RTS     PC               ; RETURN - INTERRUPTS DO THE RESET.
```

```
;
; INTERRUPT ROUTINE TO DO THE MAIN TASK.
;

RXINT::
        MOV     R0,-(SP)        ; SAVE CALLER'S REGISTERS.
RXNXTC:
        MOV     @#RBUFF,R0      ; GET THE CHARACTER.
        BPL     RXIEND          ; IF NO DATA VALID, WE HAVE FINISHED.
        MOV     R0,-(SP)        ; CHECK FOR ERRORS, MODEM AND
        BIC     #107777,(SP)+   ; DIAGNOSTICS CODES.
        BNE     RXNXTC          ;  - JUST IGNORE THEM (BAD PRACTICE).

        BIC     #170200,R0      ; REMOVE UNNECESSARY BITS.
        SWAB    R0              ; POINT TO THIS CHARACTER'S LINE.
        BIS     #100,R0         ; (ADD THE INTERRUPT ENABLE BIT.)
        MOVB    R0,@#DHQCSR
        SWAB    R0              ; PUT CHARACTER BACK IN LOWER BYTE.
        CMPB    #21,R0          ; WAS IT AN "XON"?
        BNE     1$              ; NO - GO CHECK FOR AN "XOFF"

        BISB    #200,@#TBFAD2+1 ; ENABLE THE TRANSMITTER.
        BR      RXNXTC          ; GO CHECK FOR MORE CHARACTERS.
1$:
        CMPB    #23,R0          ; WAS IT AN "XOFF"?
        BNE     RXNXTC          ; NO - GO CHECK FOR MORE CHARACTERS.

        BICB    #200,@#TBFAD2+1 ; DISABLE THE TRANSMITTER.
        BR      RXNXTC          ; GO CHECK FOR MORE CHARACTERS.

RXIEND:
        MOV     (SP)+,R0        ; RESTORE THE DESTROYED REGISTER.
        RTI
```

3.4.5 Auto XON And XOFF

```
;
; THIS PROGRAM SENDS A MESSAGE OUT ON EACH LINE OF THE DHQ11 AND
; HALTS THE MACHINE WHEN ALL TRANSMISSIONS HAVE COMPLETED.
;
; THE MESSAGES ARE TRANSMITTED USING DMA MODE, AND INTERRUPTS ARE
; USED TO SIGNAL TRANSMISSION COMPLETION.
;
; AUTOMATIC FLOW CONTROL IS ENABLED ON THE OUTGOING DATA.
;

TXAUTO::
        MOV     #ATOINT,@#TXVECT ; SET UP THE INTERRUPT VECTORS.
        MOV     #200,@#TXPSW     ; INTERRUPT PRIORITY FOUR.
        MOV     #8.,R0           ; EIGHT LINES TO START.
        CLR     R1               ; START AT LINE ZERO.
1$:
        MOVB    R1,@#DHQCSR      ; SELECT THE REGISTER BANK.
        BIS     #24,@#LNCTRL     ; ENABLE AUTOMATIC FLOW CONTROL
                                 ; ON THE TRANSMITTED DATA.
        MOV     #AUTOSZ,@#TBFCNT ; SET LENGTH OF MESSAGE.
        MOV     #AUTOMS,@#TBFAD1 ; SET LOWER 16 ADDRESS BITS.
        MOV     #100200,@#TBFAD2 ; START DMA WITH TRANSMITTER
                                 ; ENABLED (ASSUME UPPER ADDRESS
                                 ; BITS ARE ZERO).
        INC     R1               ; POINT TO NEXT CHANNEL.
        SOB     R0,1$            ; REPEAT FOR ALL LINES.

        CLR     R5               ; R5 IS USED BY INTERRUPT ROUTINE.
        MOVB    #100,@#DHQCSR+1  ; ENABLE TRANSMITTER INTERRUPTS.
2$:
        CMP     #8.,R5           ; WAIT FOR ALL LINES TO FINISH.
        BNE     2$
3$:
        HALT                     ; ALL DONE, SO STOP.
        BR      3$
```

```
;
; TRANSMITTER INTERRUPT ROUTINE.
;
; R5 IS INCREMENTED AS EACH LINE COMPLETES.
;

ATOINT::
        MOV     @#DHQCSR,R0     ; GET LINE NUMBER OF FINISHED LINE.

        BIT     #10000,R0       ; CHECK FOR DMA FAILURE.
        BNE     4$              ; GO HALT - MEMORY PROBLEM.

        INC     R5              ; FLAG THAT ANOTHER LINE HAS FINISHED.

2$:
        RTI
4$:
        HALT                    ; MEMORY PROBLEM
        BR      4$

AUTOMS: .ASCII  <15><12><7><7><7>/SYSTEM CLOSING DOWN NOW/
AUTOSZ  =       .-AUTOMS
        .EVEN
```

3.4.6 Checking Diagnostic Codes

```
;
; THIS ROUTINE CHECKS  THE  DIAGNOSTICS  CODES  RETURNED  FROM  THE
; DHQ11.   ON  ENTRY,   R0 CONTAINS THE CHARACTER RECEIVED FROM THE
; DHQ11.  ON EXIT,  THE CARRY BIT WILL BE CLEAR FOR  SUCCESS,   SET
; FOR FAILURE.
;

DIAG::
        MOV     R0,-(SP)        ; SAVE THE CODE FOR LATER.

        BIC     #107776,R0      ; CHECK THAT IT IS A DIAG. CODE.
        CMP     #070001,R0
        BNE     DIAGEX          ; IF NOT, JUST EXIT NORMALLY.

        MOV     (SP),R0         ; GET THE CODE BACK.

        BITB    #200,R0         ; CHECK FOR CHIP VERSION NUMBER.
        BEQ     DIAGEX
        CMPB    #201,R0         ; SELF-TEST NULL CODE.
        BEQ     DIAGEX
        CMPB    #203,R0         ; SELF-TEST SKIPPED CODE.
        BEQ     DIAGEX

        CMPB    #305,R0         ; DHQ RUNNING CODE.
        BEQ     DIAGEX
                                ; ALL THE REST ARE ERROR CODES.

        SEC                     ; AN ERROR CODE WAS RECEIVED, SO
        BR      DIAGXX          ; SET THE CARRY FLAG.

DIAGEX:
        CLC                     ; EVERYTHING OK, SO CLEAR CARRY.
DIAGXX:
        MOV     (SP)+,R0        ; RESTORE THE CHARACTER/INFO.
        RTS     PC
```

CHAPTER 4
TROUBLESHOOTING

4.1 SCOPE

This chapter explains how to isolate the cause of a communications problem between the DHQ11 and the equipment to which it is connected.

4.2 PREVENTIVE MAINTENANCE

No preventive maintenance is needed for this option. However, you should always ensure that all cables are clear of danger, and that all the connectors are secure.

Make sure that all cables are clearly labelled, so that you can easily identify which channel number and which DHQ11 module are associated with each terminal.

4.3 TROUBLESHOOTING PROCEDURES

Troubleshooting procedures are to identify whether the problem is caused by:

- The module
- A terminal
- The cabling and distribution panels.

First decide whether the problem is associated with one channel, a group of four channels, or all eight channels.

If all channels are faulty, run the user diagnostics to test the module. Also check whether your software has a driver for the DHQ11.

If a group of four channels are faulty, check the BC05L-xx cable connected to the module.

For single-channel problems (EIA-232-D):

1. Check for loose cables and connectors.
2. Verify that the terminal is working correctly. If necessary, swap it with another one.
3. When a modem line is suspect, check that the modem is correctly configured for modem signals supported by the DHQ11. Also check that the software driver has the correct baud-rate setting and that modem support is enabled for that line.
4. If the problem cannot be solved, call DIGITAL Field Service.

For single-channel problems (DEC423)

1. Check for loose cables and connectors.

2. Verify that the terminal is working correctly. If necessary, swap it with another one.

3. Disconnect the BC16C-XX cable from the distribution panel, and connect it to the H3101 loopback connector.

4. Type characters at the terminal connected to the suspect line. If characters are echoed back when the H3101 is connected, the cables and terminal are working. If characters are not echoed back, the fault lies with the cable connection to the terminal, or with the terminal itself.

5. Rectify the cable or terminal fault, if there is one. If not, make sure that the user diagnostics for the module run correctly.

6. If the problem cannot be solved, call DIGITAL Field Service.

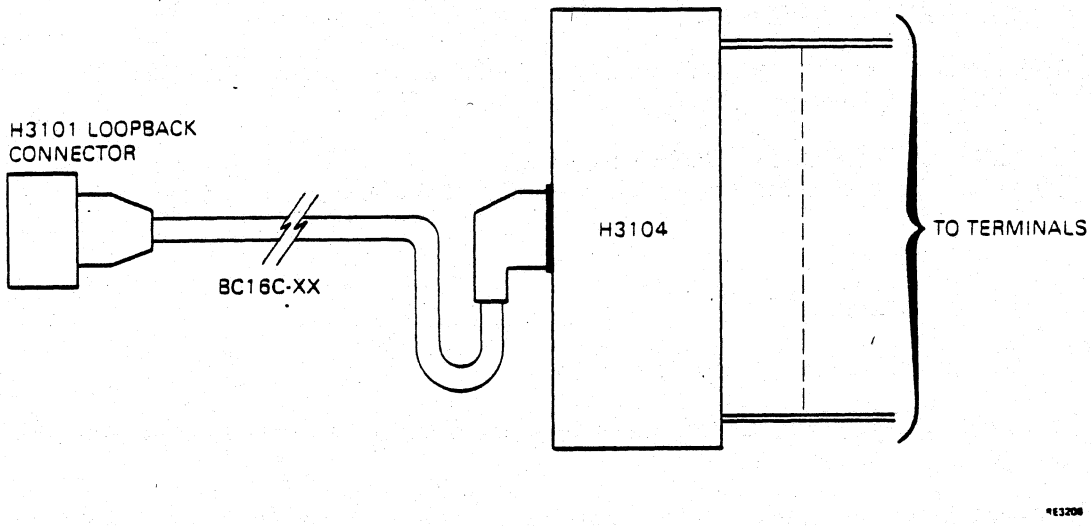


Figure 4-1 Troubleshooting DEC423 Installations

4.4 INTERNAL DIAGNOSTICS

Internal diagnostics run without intervention from the operator. There are two tests: the self-test and the background monitor program (BMP).

4.4.1 Self-Test

The self-test starts immediately after the Q-bus or module has been reset. It performs a comprehensive internal logic test but does not test the Q-bus interface. The DIAG.FAIL bit and the 'diagnostics passed' LED on the module give an indication of a successful self-test. The self-test also reports error or status information to the host via the receive FIFO.

The self-test has completed successfully if the LED is ON 1.2 seconds after the self-test has been initiated. The module is initiated by powering up the module, by resetting the module through the program interface, or by a Q-bus initialization sequence. The LED is turned off while the self-test sequencer is executing; it will flicker during this time. The duration of the OFF period depends on whether or not the self-test was invoked using the self-test skip feature of the program interface, but it will not exceed 1.2 seconds.

Self-test provides a high level of confidence that the majority of the module logic is working. The user diagnostics must also be used to test the Q-bus interface and verify that the switch settings on the module switchpacks are correct.

4.4.2 Background Monitor Program (BMP)

When the DHQ11 is not doing other tasks, the BMP carries out tests on the module. If an error is detected, the BMP reports to the host via the FIFO, and also switches OFF the 'diagnostics passed' LED.

By writing codes to the line-parameter register, the host can cause the BMP to report the status of the device, even if an error has not been detected. This facility is used if the host suspects that the option is faulty.

NOTE

More information on the self-test and BMP diagnostics is given in Chapter 3 of this manual.

4.5 MicroPDP-11 DIAGNOSTICS

4.5.1 User-Mode Diagnostics

These tests can be used by an untrained operator to verify the basic operation of the option. User-mode tests do not cause any disruption to data networks or devices to which the DHQ11 may be connected. Such networks and devices do not have to be disconnected from the DHQ11 during the tests. The MicroPDP-11 system manuals describe how to load and run these diagnostics.

4.5.1.1 Running User-Mode Tests – All user-mode tests are run by selection from the test menu displayed when the user diagnostics are booted. See Chapter 2 for more details.

A MicroPDP-11 Maintenance Kit is available, which allows trained personnel to run individual diagnostic programs under the XXDP+ diagnostic monitor, and to configure and run DECX11 system test programs. The XXDP+ functional diagnostic is VHQA**.BIN, and the DECX11 module is XDHV**.OBJ.

4.6 MicroVAX II DIAGNOSTICS

Diagnostics for MicroVAX II systems all run under the MicroVAX Maintenance System (MMS). The MicroVAX II system manuals describe how to load the MMS into the MicroVAX II, and how to run MMS diagnostics. All the tests can be run by selection from the test menus displayed when MMS is booted.

4.6.1 User-Mode Tests

These tests can be used by an untrained operator to verify the basic operation of the option. User-mode tests do not cause any disruption to data networks or devices to which the DHQ11 may be connected. Such networks and devices do not have to be disconnected from the DHQ11 during the tests. See Chapter 2 for more details.

4.7 USING THE LOOPBACKS

4.7.1 H3277 Staggered Loopback Test Connector

The H3277 is used during maintenance diagnostic tests on either EIA-232-D or DEC423 installations (see Figure 4-2 and Figure 4-3). It allows all channels to be tested.

4.7.2 H3197 Line Loopback Test Connector

The H3197 is used during maintenance-mode diagnostic tests on EIA-232-D installations (see Figure 4-2) to trace a fault to a single channel. The older style H325 test connector provides the same signal loopbacks as the H3179, and may be used in its place.

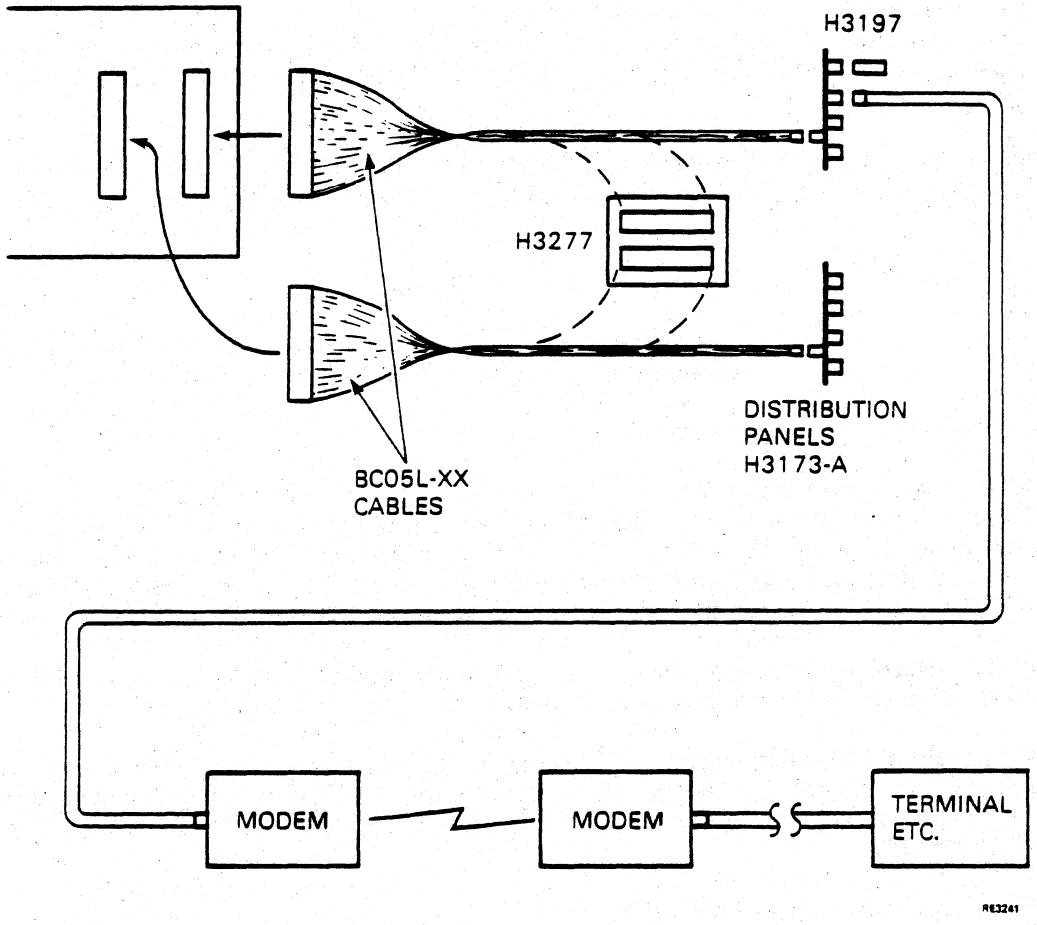


Figure 4-2 Using Loopback Connectors in EIA-232-D Installations

4.7.3 H3101 Loopback Connector

The H3101 loopback connector (see Figure 4-3) is used during diagnostic tests for DEC423 installations. It is two loopback connectors in one package, and consists of a female 36-way loopback connector and a male 36-way loopback connector. It can be connected either to the active bulkhead panel or to the 8-way distribution panel.

4.7.4 H3103 Loopback Connector

The H3103 loopback connector (see Figure 4-3) is used during maintenance diagnostic testing with DEC423 installations to test each line from the DHQ11 at the output from the H3104 cable concentrator.

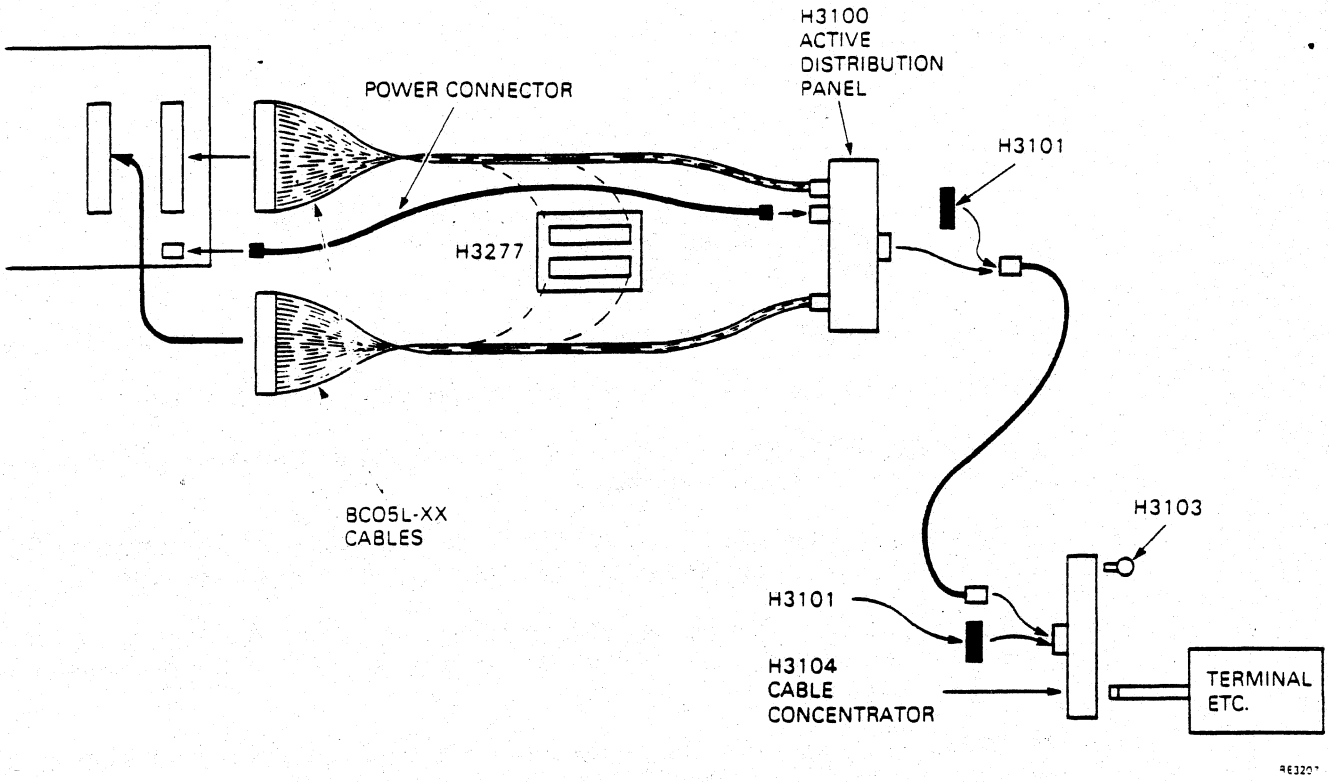


Figure 4-3 Using Loopback Connectors in DEC423 Installations

4.8 MicroPDP-11 SERVICE-MODE DIAGNOSTICS

4.8.1 MicroPDP-11 Functional Diagnostic

The functional diagnostic for the MicroPDP-11 is VHQA**.BIN. This also tests other modules in the same family, for example, the DHV11.

After booting, the program asks you four questions about the hardware configuration. These are:

- CSR address
- Vector address
- Active line bitmap
- Loopback type

The diagnostic will then 'size' the option to determine modem or data-leads-only, 8 or 16 lines, and then print this information. The control chip and OCTART revision levels are also printed. Always check that the unit 'sizes' correctly.

4.8.1.1 Test Summaries – The following list summarizes the MicroPDP-11 function diagnostic tests.

NOTE

These test numbers are only given as a guide. For details of the tests for the revision you are using, see the appropriate diagnostic listing.

1. Register Address Test — Verifies that the Q-bus can read and write to the unit under test.
2. MASTER.RESET Test — Verifies that a master reset clears within 5 seconds.
3. MASTER.RESET (Skip Self-Test) Test — Verifies that a master reset clears in approximately 20 ms when the skip-self-test sequence is used.
4. RX.CHARACTER Field Test — Verifies that the data bits of the codes in the receive FIFO after a master reset and skip-self-test are consistent with the skip-self-test codes.
5. RX.FLAG Field Test — Verifies that the three data status bits (overrun, framing, and parity error) are all set on each of the skip-self-test codes in the FIFO after a master-reset and skip-self-test sequence.
6. RX.DATA.AVAIL Test — Verifies that the RX.DATA.AVAIL bit is set when the skip-self-test codes are in the FIFO, and that it clears after they have been read.
7. RX.DATA.VALID Test — Verifies that the RX.DATA.VALID bit is set for all the codes in the FIFO, and clear after all the codes have been read.
8. —RX.LINE Field Test — Verifies that the RX.LINE line fields are correct for the skip-self-test codes.
9. BMP Check Test — Verifies that the unit does not immediately fail the background monitor program, as this may invalidate further tests.
10. Skip Self-Test Test — Verifies that the unit skips the self-test in the time allowed, and that the FIFO contains the correct codes after its completion.
11. DIAGNOSTIC.FAIL Test — Verifies that, by using the skip-self-test sequence, the DIAG.FAIL bit sets and clears with the allowed times.
12. Self-Test Test — Verifies that the unit's self-test executes within the correct time, and that the correct codes are returned in the FIFO after its completion.
13. Self-Test Fail Test — Verifies that the unit will report errors when it is forced to fail by using the special fail self-test sequence (decimal 146314 written to transmit buffer count register). The DIAG.FAIL bit sets, and at least one self-test failure code(231) is in the receive FIFO.
14. Chip Version Number — Verifies that the chip version numbers are reported correctly, and, if requested, prints them out.
15. Not used.
16. Word Access Read/Write Test — Verifies that the registers respond correctly to read and write accesses.

17. Word Access Read/Modify/Write Test — Verifies that the registers will respond correctly to read/modify/write accesses.

18. Byte Access Read/Write Test — Verifies that the registers will respond correctly to byte read/write accesses.

19. Byte Access Read/Modify/Write — Verifies that the registers will respond correctly to byte read/modify/write accesses.

20. TX.DATA Invalid Test — Verifies that, if a character is written to the transmit character register (TXCHAR) without TX.DATA.VALID<15> set, no TX.ACTION occurs.

21. TX.DATA Valid Test — Verifies that if a character is written to the transmit character register (TXCHAR) with TX.DATA.VALID<15> set, a TX.ACTION occurs.

22. TX.ENABLE (Inactive) Test — Verifies that when a line's TX.ENBL bit is clear, transmission will not take place on that line.

23. TX.ENABLE (Active) Test — Verifies that when a line's TX.ENBL bit is set, transmission will take place on that line.

24. DMA.START Test — Verifies that each DMA start bit will initiate a DMA transmission on a line.

25. DMA.ABORT Test — Verifies that each DMA abort bit will stop a DMA transmission, return a TX.ACTION, and successfully restart the DMA.

26. DMA.ERROR Test — Verifies that the DMA error bit in the CSR reports DMA errors correctly when they occur.

27. FIFO Data Test — Verifies that the FIFO will hold 256 characters without corrupting data, and that the overrun set is clear.

28. O.AUTO Inactive Test — verifies that the unit will not respond to incoming XON and XOFF characters when O.AUTO is clear.

29. O.AUTO Active Test — Verifies that the unit responds correctly to incoming flow-control characters when active.

30. I.AUTO Inactive Test — Verifies that the unit will not generate XON and XOFF characters in response to the appropriate FIFO conditions when I.AUTO is inactive.

31. I.AUTO Active Test — Verifies that the unit will generate XON and XOFF characters in response to the appropriate FIFO conditions when I.AUTO is active.

32. XON-XOFF Filtering Test — Verifies that when LPR<0> DISAB.XRPT and LNCTRL<4> OAUTO are set, XON-XOFF characters are not placed in the receive silo.

33. Interrupt Test — Verifies that the unit will generate reception and transmission interrupts correctly.

34. Diagnostic Field (BMP) Test — Verifies that a request to the unit to report BMP status codes is complied with within the specified time. All active lines are tested.

35. FIFO 3/4 Level Inactive Test — Verifies that the 3/4 level alarm does not become active below the 3/4 level.

36. FIFO 3/4 Level Active Test — Verifies that the 3/4 level alarm becomes active when the FIFO is 3/4 full.

37. FIFO 3/4 Level Active/Inactive Test — Verifies that the 3/4 level alarm, once activated, remains active until the FIFO is reduced below the 1/2 level.

38. FIFO 1/2 Level Test — Verifies that the FIFO 1/2 level alarm system becomes active and inactive at the correct levels.

39. Break Generation Test — Verifies that all serial transmit lines can generate a break by setting the BRK bit in the associated LNCTRL register.

40. No Overrun Error Test — Verifies that the unit under test will not report data overrun errors when they do not occur.

41. Overrun Error Test — Verifies that the unit will report data overrun errors when 257 characters are received.

42. DTR Test — If modem control available, verifies that changing the state of the DTR bit affects the state of the DTR control line.

43. RTS Test — If modem control available, verifies that changing the state of the RTS bit affects the state of the RTS control line.

44. DSR Test — If modem control available, verifies that the DSR status signal correctly reports the state of the looped-back DTR control line.

45. RI Test — If modem control available, verifies that the RI status signal correctly reports the state of the looped-back DTR control line.

46. CTS Test — If modem control available, verifies that the CTS status signal correctly reports the state of the looped-back RTS control line.

47. DCD Test — If modem control available, verifies that the DCD status signal correctly reports the state of the looped-back RTS control line.

48. DTR Interactions Test — If modem control available, verifies that changing the state of the DTR control signal on any line does not affect the state of any status signals that it is not looped-back to.

49. RTS Interactions Test — If modem control available, verifies that changing the state of the RTS control signal on any line does not affect the state of any status signals that it is not looped-back to.

50. Transmit Line Test — Verifies that the transmit lines and receive lines are working correctly through the device cables, distribution panel and loopback connectors. Executed only if external mode is selected.

51. Transmit Lines Interaction Test — Looks for any interaction between lines. Executed only if one of the external loopbacks is selected.

52. Receive Timer Test — Verifies that the hold-off timer for receive interrupts is operating correctly, and that the 3/4-full level overrides the timer.

53. Not used.

54. Not used.

55. DMA Address Test — Verifies that the unit can access the full memory which is on the machine via DMA access.

56. Modem Loopback Test — If modem control available, allows the operator to test modem links which are attached to the unit serial ports.

57. Keyboard Echo Test — Allows the operator to test terminal links (or other communications links), which are attached to unit serial ports, from remote ends of the links.

58. Single Character Test — Verifies that the unit will transmit and receive correctly using non-DMA mode at various line parameters.

59. DMA Mode Test — Verifies that the unit will transmit and receive correctly using DMA at various line parameters.

60. Framing Error Test — Verifies that forced framing errors are reported correctly. H3277 staggered loopback only.

61. Parity Error Test — Verifies that forced parity errors are reported correctly. H3277 staggered loopback only.

62. Split Speed Test — Verifies that the unit will function correctly using different transmit and receive speeds on each active line. H3277 staggered loopback only.

63. Report BMP Codes Test — This pseudo-test reports the first 32 characters which were discovered in the FIFO during the execution of the other tests. This avoids interruption of the other tests by these codes, if they are not critical to the performance of the tests.

4.8.2 DECX11 Object Module

The DHQ11 Object Module is the same as for the DHV11, XDHV**.OBJ.

NOTE

Early versions of this module DO NOT support the DHQ11.

The minimum parameters which must be specified are:

1. DVA (Device Address)
2. VCT (Vector Address)
3. DVC (Device Count), if more than one.

The default operating mode is with all lines looped back internally at 9600 baud.

4.9 MicroVAX II SERVICE-MODE DIAGNOSTICS

The DHQ11 uses the same diagnostic module as for the DHV11, NADHA*.

4.9.1 Configuration Tests

The module is 'sized' to check the number of lines (8 or 16), and whether it supports modems or is data-leads-only. This information, together with the control chip and OCTART revision levels, is added to the system configuration file.

4.9.2 Field Service Functional Tests

Before the diagnostic runs a field service test, the set-up procedure for the DHQ11 diagnostic is executed. You will be prompted to attach any loopback connectors or cables (for instance, bulkhead loopback connectors). On pressing the RETURN key, all ports are sized to see to which ports (on the same controller) the loopbacks are attached. This information is then displayed, and the field service tests are started. This set-up procedure is run only once after configuration of the diagnostic system. There are 10 tests. Numbers 1 to 5 are verify-mode tests, numbers 6 to 10 are service-mode tests.

TEST 1: In this test, the DHQ11 is initialized and addressability checks are made on various registers.

TEST 2: Uses loopback connectors and cables sized during the setup procedure to send single characters in programmed output mode over port 0; using baud rates of 300, 1200, 9600 and 38.4k bauds; and with various data lengths, stop bit sizes, and parity options. It should be noted that, due to execution time constraints, this is the only test, other than the utilities, which exercises the entire range of character options.

TEST 3: Performs extensive DMA testing through loopback connectors and cables sized during the setup procedure, using different buffer sizes. All ports are tested simultaneously at 19.2 kbytes/s. FIFO overrun and DMA abort are tested. In addition, if a port is determined to be connected to a port other than itself, a more thorough test of outgoing data flow-control is performed.

TEST 4: This test uses loopback connectors and cables sized during the setup procedure to perform extensive flow-control testing. OAUTO, IAUTO, and FORCE.XOFF functions are exercised. The break signal function is also tested.

TEST 5: This test exercises the modem control signals for each of the connected channels that were determined to be looped back during the setup procedure. This ensures that the corresponding input signals are valid and that the DHQ11 may be configured to interrupt when a modem control signal is asserted.

Test 6: This is the same as test 1, except that testing occurs through cables and loopback connectors sized during the setup procedure with baud rates of 300, 1200, 9600, and 38.4K.

Test 7: This is the same as test 2, except that testing occurs through the cables and loopback connectors.

Test 8: This is the same as test 3, except that testing occurs through the cables and loopback connectors.

Test 9: This test exercises the modem control signals for each port, ensuring that the DHQ11 may be configured to interrupt on the transition of a modem signal.

Test 10: This is the same as test 5, except that testing occurs through the cables and loopback connectors.

4.9.3 Field Service Exerciser Tests

The exerciser test is designed to stress the system by simulating normal system operation. This is achieved by exercising several devices simultaneously.

Test 1 is a combination of the verify-mode tests.

Test 2 is a combination of the verify- and service-mode tests.

These tests are run at 19.2 kbytes s only, using cables and loopback connectors found during set-up.

4.9.4 Utilities

The three utilities provide simple routines to:

- Run echo tests and terminal tests on specific lines.
- Locate cable faults, using the loopback connectors to loop data back to the module
- Check that a terminal, or remote equipment, is correctly transmitting and receiving characters

Utility 1 This utility permits staged testing of the DHQ11 and associated cables/connectors. The diagnostic requests configuration parameters from the operator, and then repeatedly tests the port(s) for data loopback integrity. The operator may, by strategically placing loopback connectors at various points in the communications path, isolate defective units. The operator is not prompted as to where to place the loopback connectors, nor does the diagnostic interpret the results of the tests.

Utility 2 This utility permits testing of remote communications devices. The diagnostic puts all ports into remote loopback maintenance mode. All characters sent to any port will be echoed back to the sender, at baud rates up to 9600 baud. No operator configuration is necessary. Because of inherent DHQ11 buffering limitations, characters may be lost if transmitted too rapidly by the terminal.

Utility 3 This utility sends test strings to the port(s) specified by the operator to aid diagnoses of remote communications devices. The operator may choose any baud rate or character specifics. The port under test is configured with auto-flow control for outgoing characters.

4.10 FIELD-REPLACEABLE UNITS (FRUS)

The FRUs are:

Reference No.	Item
M3107	Dual-height DHQ11 module
BC05L-xx	Flat cable, 40 conductor
For EIA-232-D Installationsdnobold	
H3173-A	Distribution panel
For DEC423 Installations	
H3100	Active distribution panel
BC16C-25	Multiway cable
H3104	Cable concentrator
70-22775-XX	Power cable

CHAPTER 5
TECHNICAL DESCRIPTION

5.1 SCOPE

This chapter gives a technical description of the DHQ11 asynchronous multiplexer. Figure 5-1 shows a block diagram of the DHQ11, and each block identified in the diagram is described in this chapter. While reading this chapter, you may find it useful to have access to a DHQ11 printset (part number MP-02380).

5.2 OVERVIEW

Figure 5-1 shows a block diagram of the DHQ11. It can be broken down into the following sections:

- RAM — stores control information and provides the data buffers
- OCTART — contains eight asynchronous receiver/transmitters, baud-rate generators, and interface logic
- Control Chip — contains sequencers and other logic to implement all the functions of the DHQ11 outside of the OCTART
- Switchpack and Shift Register Section — defines the device address and vector, and the mode of operation
- Q-bus Drivers and Receivers — provide the electrical interface to the Q-bus
- Modem Latches — latches the RTS and DTR modem control signals
- Line Interface — converts signals to and from line levels
- Power Converter — provides positive and negative 10 V supplies for the line interface.

Each of these blocks is described in more detail in Section 5.3. Section 5.4 describes the flow of data through the module.

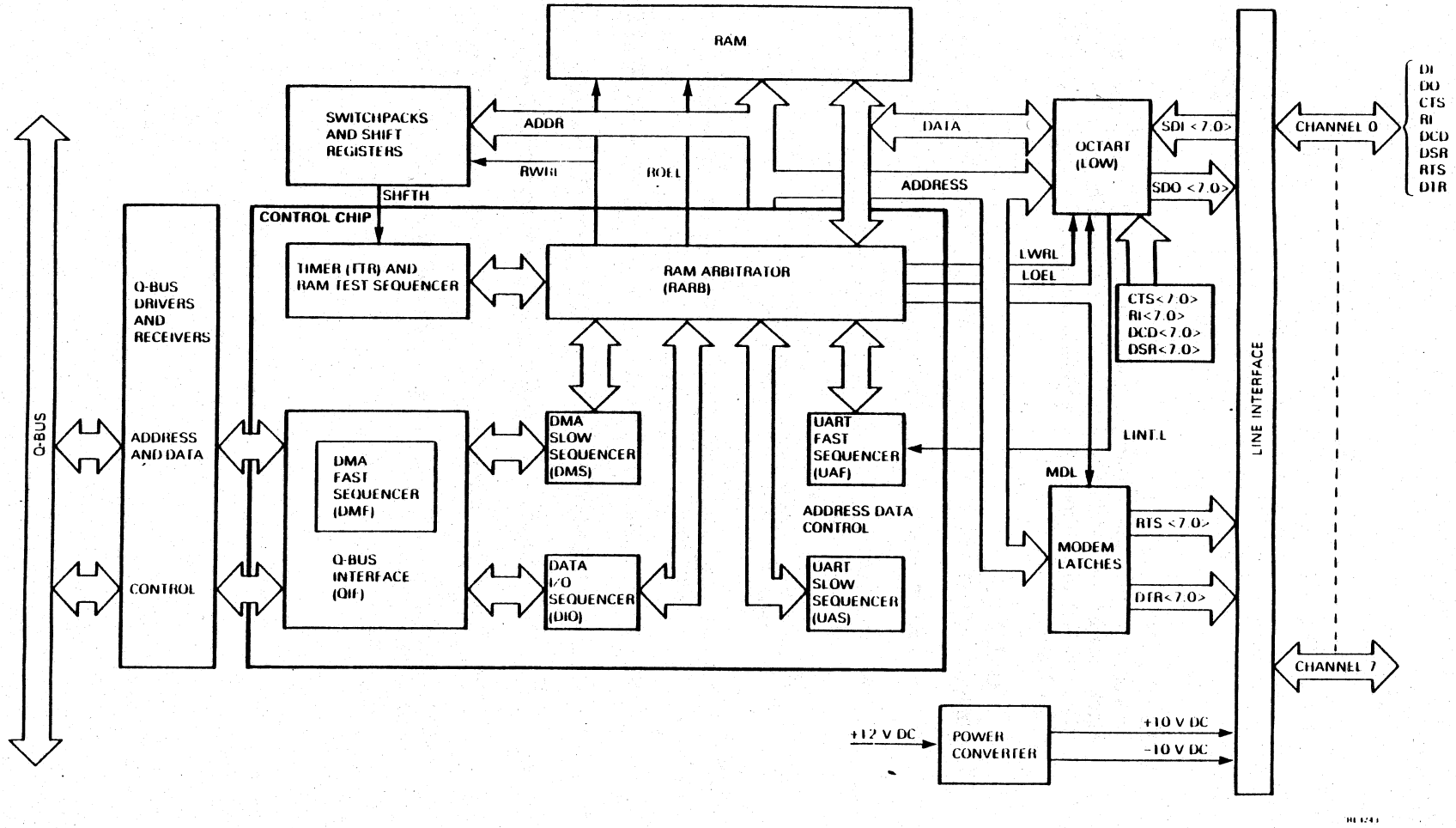


Figure 5-1 DHQ11 Block Diagram

5.3 DHQ11 FUNCTIONAL BLOCKS

5.3.1 RAM

Figure 5-2 shows the way in which the RAM is assigned to the various functions. Two kbyte of RAM is used, which is divided into three main sections:

- The top 1 kbyte contains the 64-character transmit FIFOs, one per channel. The DHQ11 uses only eight channels, and the rest of this area is unused.
- The next 512 bytes contain the 256-word receive FIFO. The low byte of each word contains a received character, and the high byte contains status information, such as channel number and error status.
- The bottom 512 bytes contain the 32-byte control register areas, one per channel. These registers control the data flow through the DHQ11, using the sequencers in the control chip.

5.3.2 OCTART

The OCTART contains 8 asynchronous receiver/transmitters, a 16-output baud-rate generator, and interface logic. The UARTs are compatible from a serial-line viewpoint with those in the 2681 DUART. Each channel has only a single buffer on both transmit and receive. The UART fast sequencer on the control chip (see Section 5.3.3.6), together with the RAM, provides double buffering for the transmitters and a 4-word-per-line FIFO for each receiver, thus completing compatibility with the 2681 DUART.

The OCTART is shown in greater detail in Figure 5-3.

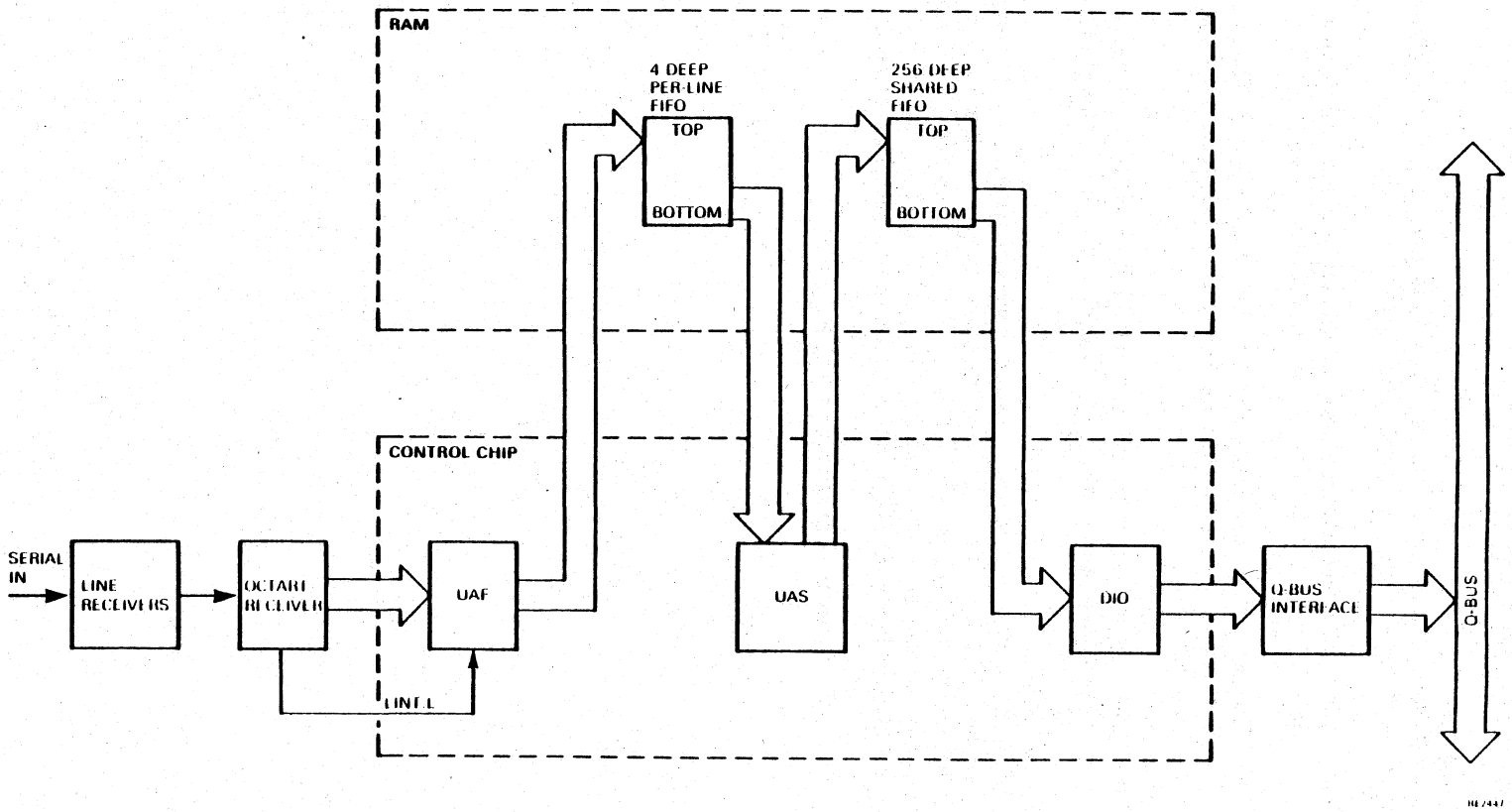


Figure 5-2 RAM Assignment

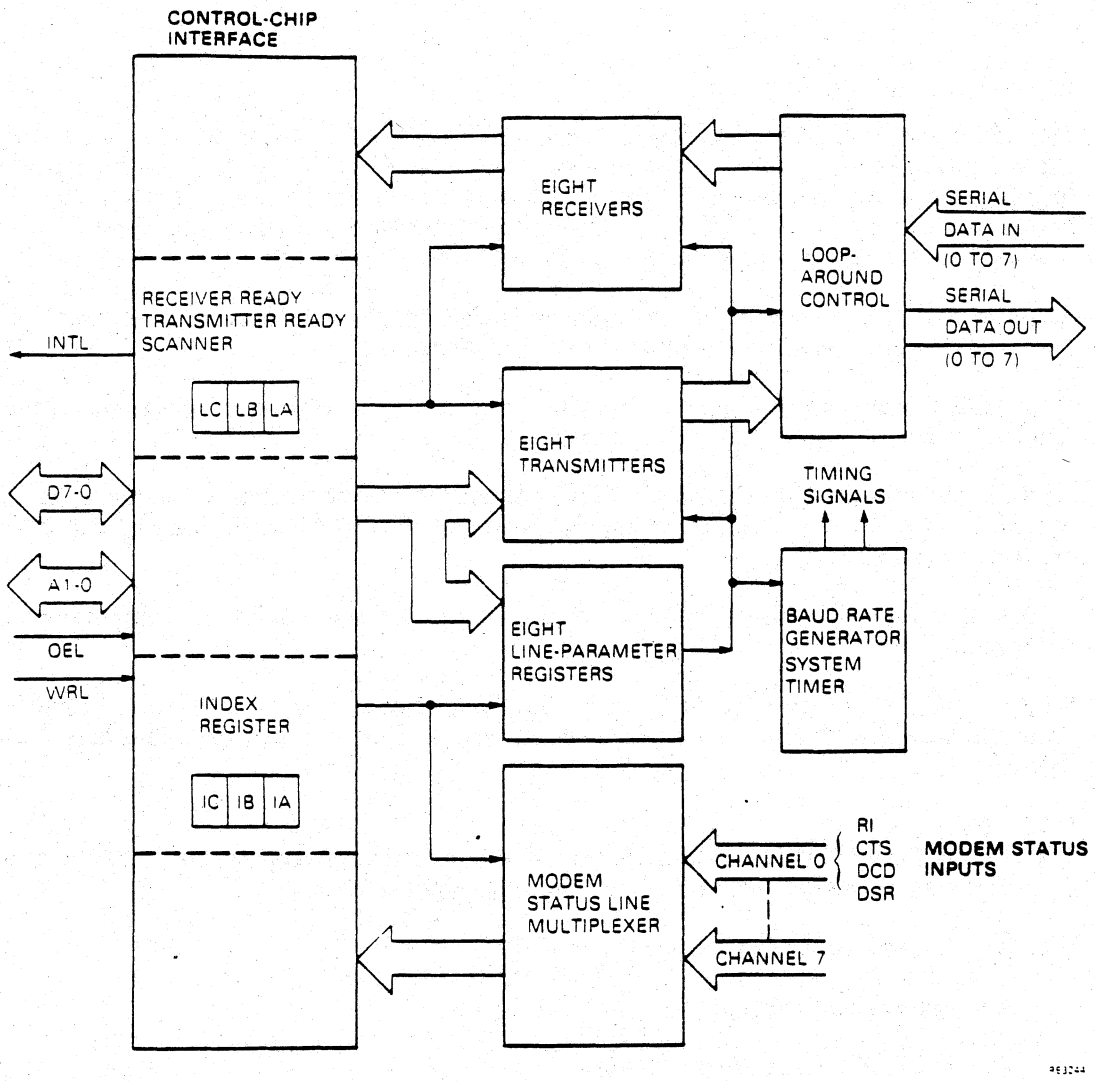


Figure 5-3 OCTART

5.3.2.1 Control-Chip Interface – This manages two separate sources of information for the OCTARTs; they are:

- Receiver/Transmitter-Ready Scanner Register bits L<C:A>, together with the receiver-ready bit
- Index Register bits I<C:A>.

The scanner logic scans each channel in turn until it locates a channel needing servicing. It then asserts the interrupt line to the control chip. A channel is ready for servicing when either it is free to accept a character for transmission, or a character has been received, as indicated by the receiver ready bit.

During the servicing of this interrupt by the control chip, the L<C:A> bits tell the control chip which channel has interrupted. If it is a receive interrupt, the received character is presented on the D<7:0> lines. If it is a transmit interrupt, the control chip will either present a character on D<7:0>, or performs a dummy transfer, which has the effect of temporarily disabling transmit interrupts from that channel. Note that the receivers are given priority over transmitters.

Register bits I<C:A> select one of eight channels during a register access. Address lines A<1:0> select one of four registers associated with that channel.

5.3.2.2 Line-Parameter Register – Each line has its own line-parameter register derived from the Q-bus-accessible LPR and LNCTRL registers.

5.3.2.3 Modem-Status Multiplexer – This presents to the control-chip interface the four modem control inputs for the channel being addressed by I<C:A> when the control chip reads the modem-status register.

5.3.2.4 Loop-Around Control – This implements the functions of the maintenance mode bits (see Section 3.2.2.6).

5.3.2.5 Baud-Rate Generator – This provides 16 independent baud rates for transmit and receive. Transmitter baud rates are independent from the receive rates, and there is no interdependency between channels.

5.3.3 Control Chip

The control chip contains all the necessary logic and sequencers to control the operation of the DHQ11. The functions of this IC can be broken down into eight blocks:

- Timer and RAM Test Sequencer (TTR)
- Q-bus Interface (QIF)
- DMA Slow Sequencer (DMS)
- DMA Fast Sequencer (DMF)
- Data I/O Sequencer (DIO)
- UART Fast Sequencer (UAF)
- UART Slow Sequencer (UAS)
- RAM Arbitrator (RARB).

5.3.3.1 Timer And RAM Test Sequencer (TTR) – This sequencer controls the power-up sequence of the module. On power-up, the TTR:

- Resets the OCTART
- Resets the modem latches

- Clocks the switchpack settings into the control chip. RAM address lines are used to select the shift register operation, and RWR.L (RAM write) is used to clock the shift register (see Section 5.3.4 for more information)

- Tests the RAM (which takes 26 ms) and leaves it in a defined state which reflects the power-up state described in Section 3.3.1.

The sequencer also generates internal timing signals for the control chip.

5.3.3.2 Q-bus Interface (QIF) – This block contains the logic to handle data I/O and interrupt operations, and also DMA operations through its DMF sequencer, described in Section 5.3.3.3.

The QIF also includes other functions, such as:

- A special data-out handler, so that the Q-bus is given a fast response time without having to wait for RAM access

- Logic to handle interrupt request generation and vector assertion (using data read from the switches at power-up).

Some device register bits are also implemented in this block, such as:

- Indirect address register pointers

- Interrupt enable bits.

5.3.3.3 DMA Fast Sequencer (DMF) – DMA operations are controlled by a combination of the DMF (DMA-Fast) sequencer described here, and the DMS (DMA-Slow) sequencer (described in Section 5.3.3.4).

The function of the DMF sequencer is to become Q-bus master and then acquire characters from the Q-bus at maximum Q-bus speeds. At an average rate of 1 word every 850 ns in block-mode DMA, the DMF acquires up to 8 words (16 characters) during its bus mastership. In non-block operations, up to 4 words are acquired while it is bus master. These characters are transferred to the transmit FIFO under the control of the DMS sequencer. The DMF sequencer operates as a slave to the DMS sequencer.

5.3.3.4 DMA Slow Sequencer (DMS) – This sequencer has three independent functions:

- To scan the channels until it detects the need for a DMA operation

- To handle a DMA transfer by controlling the DMF sequencer

- To handle an ABORT request

- To report a TX.ACTION at the end of a DMA operation (this includes successful operations, aborted operations, and operations terminated after a bus error).

5.3.3.5 Data I/O Sequencer (DIO) – This sequencer waits in an idle loop until signals from the Q-bus (through the QIF) cause it to perform one of the Q-bus data I/O operations — DATI, DATO(B), and DATIO(B).

This sequencer also detects operations on certain registers and takes appropriate action. For example, after a write operation to an LPR or LNCTRL register, it sets a bit in the RAM control area for that channel to indicate to the UAS sequencer that the contents may have changed.

5.3.3.6 UART Fast Sequencer (UAF) – This sequencer handles interrupts from the OCTART. When an interrupt is received, the UAF reads the OCTART status register to find the channel number, and to ascertain whether it is a receive or transmit interrupt.

For a transmit interrupt, having checked that there is a character ready to transmit, the UAF transfers the character directly from the RAM to the OCTART. For a receive interrupt, the UAF transfers the character directly from the OCTART to the top of the 4-word FIFO in RAM (low byte). Then the error status, which had previously been read from the OCTART status register, is written to the FIFO (high byte).

5.3.3.7 UART Slow Sequencer (UAS) – This sequencer scans all 8 channels (in 160 us, to guarantee operation on all channels at maximum possible data rates). For each channel, the UAS:

1. Moves received characters from the bottom of the 4-word FIFO in RAM into the 256-word shared receive FIFO. It also handles received XON/XOFF control characters.

2. Implements one of the following six actions (listed in priority order) before repeating step 1 for the next channel: Modem service — it checks modem status every 10 ms

    - Line-Parameter Register written check — it checks whether this register has been changed by the DIO sequencer
    - Line-Parameter Register change — if during the last pass it detected that this register had been changed, it now updates the OCTART registers with the new information
    - BMP Report — generates a Background Monitor Program report
    - Transmits a single character from the TXCHAR register, or transmits an XON or XOFF character
    - Transmits from the transmit FIFO

The UAS block also includes:

- RBUF FIFO control
- TX.ACTION FIFO control
- Background Monitor Program (BMP) logic.

5.3.3.8 RAM Arbitrator (RARB) – This arbitrates between the five RAM access sequencers described in sections 5.3.3.1 and 5.3.3.4 to 5.3.3.7, giving one of them access to the RAM/OCTART data bus, depending on the priority scheme described here.

The TTR sequencer has the top priority, so that it gets 100% RAM access for the first 26 ms after power-up. This guarantees that the RAM will be powered-up to an operational state before any other sequencer can begin. After 26 ms this sequencer idles.

Although it cannot gain access to RAM during the 26 ms power-up time, the DIO sequencer still operates. This is needed for CSR access and skip-self-test operations from the Q-bus (see Section 3.2.2.1).

To ensure that the progress of each sequencer is predictable, RAM access is alternated between the two UART sequencers (UAF and UAS) and the two CPU sequencers (DIO and DMS). During 'CPU-time', only CPU sequencers are granted access. During 'UART-time', UART sequencers have priority, but if neither UART sequencer requires access, a CPU sequencer can steal the cycle. The overall effect of this is that:

- The UART sequencers progress at a predictable rate. This guarantees service to each channel at a rate fast enough to maintain maximum throughput, while still allowing a required minimum time between OCTART write operations

- Access by the CPU sequencers is maximized (and hence Q-bus BRPLY delay times minimized) by allowing them RAM access during unused UART cycles, along with normal CPU cycles.

In 'UART-time', the UAF has priority over the UAS to make sure all data transfers to and from the OCTART are done as quickly as possible. Of the CPU sequencers, the DIO has priority over the DMS to guarantee minimum delay in asserting BRPLY.

5.3.4 Switchpack And Shift Registers

The TTR sequencer shifts-in the contents of the shift registers after the module has been reset (by BINIT or MASTER.RESET). Since the switchpack contents are only examined at this time, the module must be reset (BINIT or MASTER.RESET) in order to set new values.

The TTR sequencer in the control chip has been designed for use in several different applications and therefore needs to determine whether the module has 8 or 16 channels, and whether it is a Q-bus or UNIBUS application (the DHQ11 is set up for 8 channels on Q-bus). Figure 5-4 shows a simplified diagram of the switchpack and shift register logic, which can be used with the following explanation.

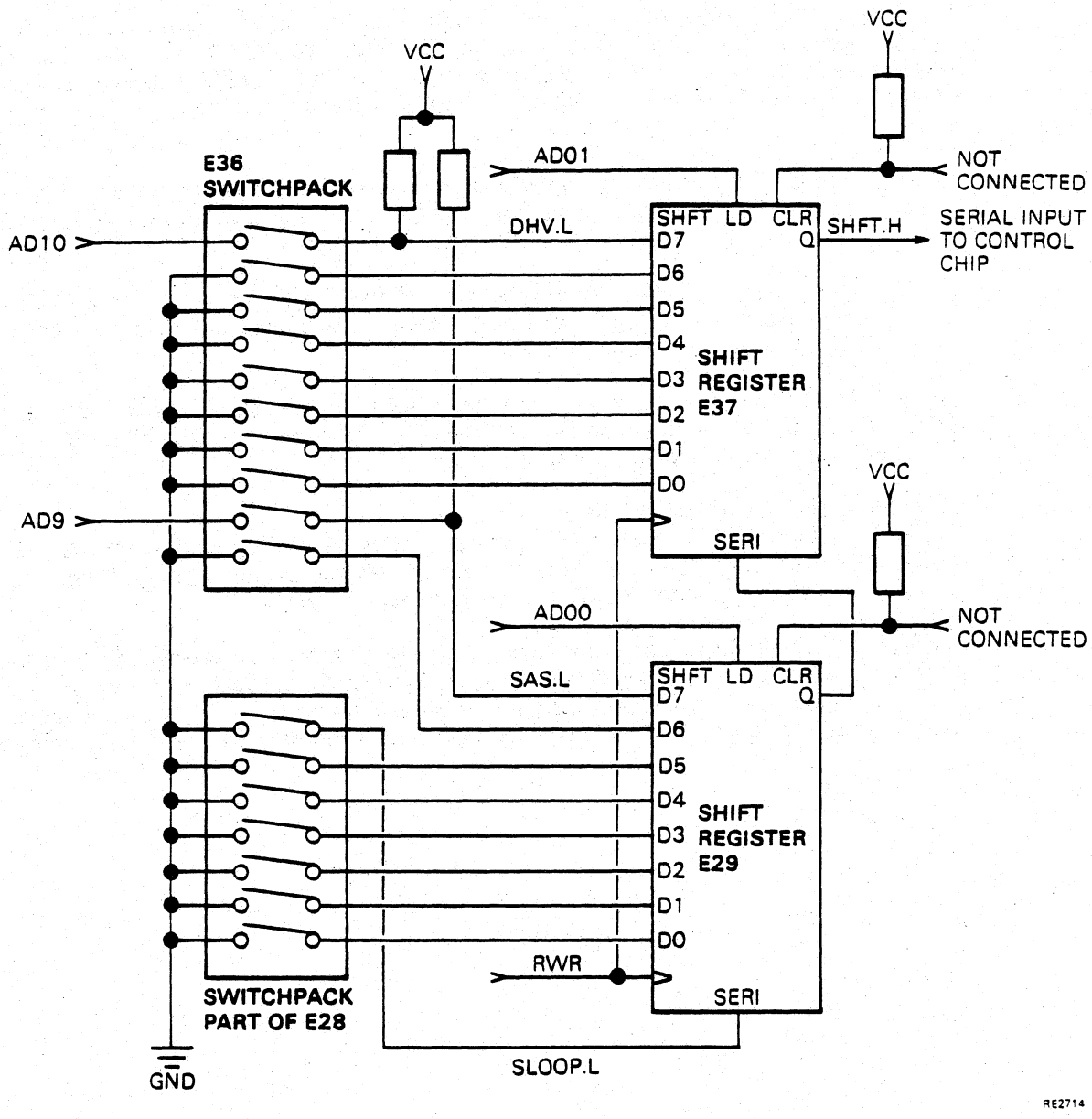


Figure 5-4 Switchpack and Shift Register Logic

First, the switch settings connected to the D<7:0> inputs of the shift registers are synchronously loaded into the shift registers. This is done by holding AD00 and AD01 low while pulsing RWR.L. The switch settings are clocked into the shift registers by the trailing edge of RWR.L. AD09 and AD10 are held low during this first operation to ensure that the respective D7 settings (DHV.L and SA5.L) are loaded in the same way as all the other switches. On DHQ11, the switch generating DHV.L is held electrically closed by jumper W1, which locks the module in the DHV11 mode of operation.

After this load, the first bit (D7 of shift register E20) is present at the SHFT.H input to the control chip, and is latched internally by the TTR sequencer. Then 16 RWR.L pulses are applied with AD00 and AD01 high (this selects the shift function). The remaining bits in the shift register are thus clocked into the control chip and latched by the TTR, including the last shifted-in setting (SERI input) to the E12 shift-register (SLOOP.L), making a total of 17 bits.

Two further settings need to be determined:

- Whether the device supports 8 lines (as does DHQ11) or 16 lines
- Whether the device operates on the Q-bus (as does DHQ11) or on the UNIBUS.

After the 17 switch settings have been latched, the control chip sets AD09 and AD10 high. It then selects the load function (AD00 and AD01 low) and pulses RWR.L. Because of the high level on AD09 and AD10, a high level is latched into D7 of both shift registers, regardless of the switch setting.

The control chip now tries to clear these two bits. If the device supports 16 lines, AD08 is connected to the CLR input of E20. If the device operates on the UNIBUS, AD02 is connected to the CLR input of E12. The control chip therefore pulses AD02 and AD08 low to try and clear the registers. On the DHQ11 neither of these connections is made (both CLR inputs are simply pulled high); therefore the registers do not clear. The control chip can now test the state of the SHFT.H line and determine (since SHFT.H is high) that the DHQ11 has eight lines. After applying eight RWR.L pulses, a second test of the SHFT.H line shows that the DHQ11 operates on Q-bus (SHFT.H is again high).

5.3.5 Q-bus Drivers And Receivers

Six DC021 Q-bus driver/receiver chips are used. E10 is wired for receive only and E2 for transmit only. The direction (transmit or receive) of the other four (E1, E9, E17, E22) is controlled by signals from the control chip. To avoid bus contention, the change of state of the signals from the control chip from tri-state to active is carefully timed before and after changing the direction. In addition, E1 and E9 are disabled by EN1.L and EN2.L while changing the direction. This avoids the possibility of accidentally asserting control signals such as BSYNC.L or BRPLY.L on the Q-bus while changing direction.

5.3.6 Modem Latches

Two 8-bit addressable latches are used to latch the modem control signals. When the control chip wants to write the modem control signals (RTS and DTR) it selects the appropriate channel using address lines AD<7:5> (see Figure 5-5). At the same time, AD04 writes the value for RTS.L, and AD03 writes the value for DTR.L, to their respective addressable latches. The control chip then asserts MDL to latch these two values. The RTS.L and DTR.L signals are written active low as they are inverted by the line drivers.

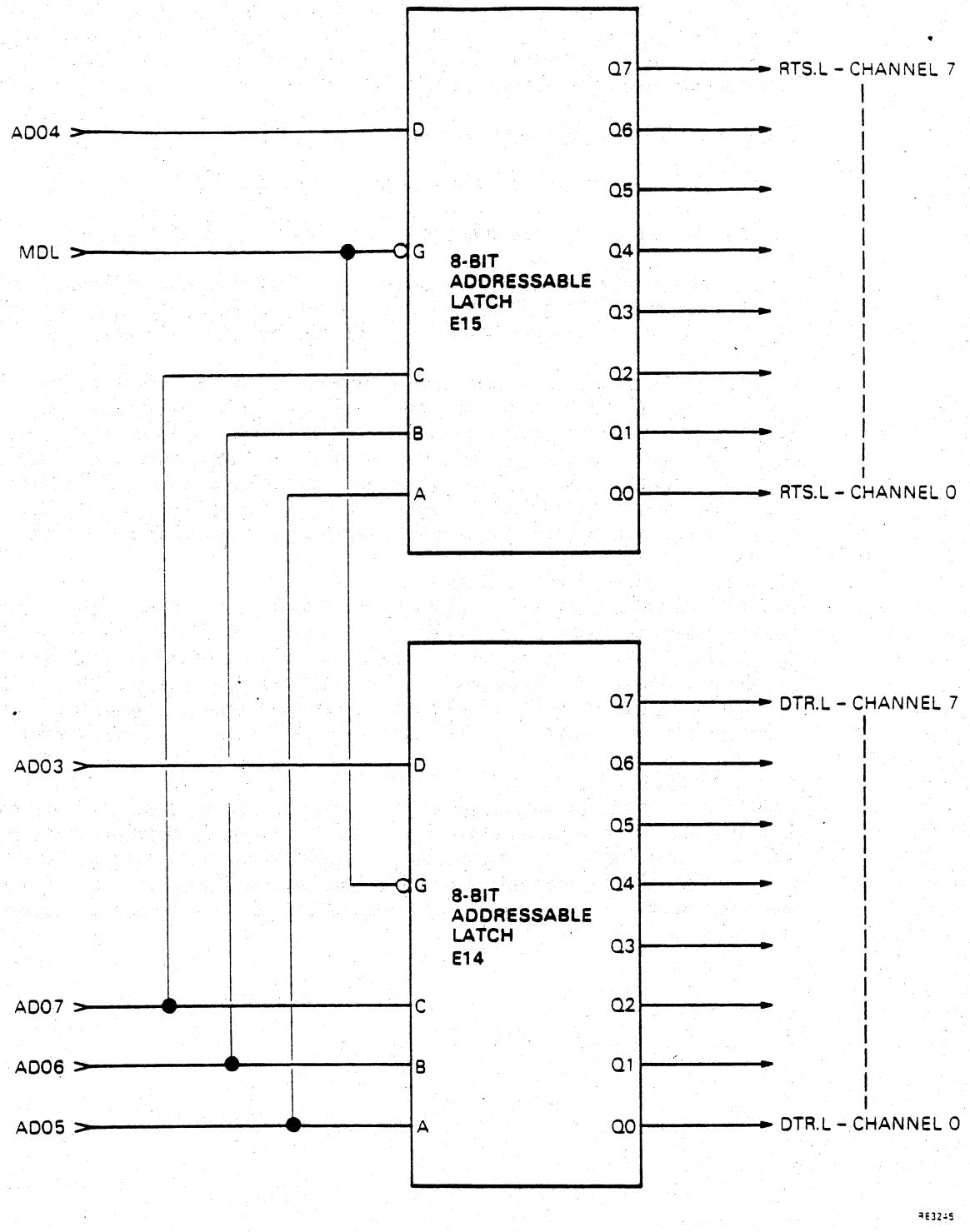


Figure 5-5 Modem Latches

5.3.7 Line Interfaces

The interface to the serial lines is provided by five octal line receiver chips (type 5180) and three octal line driver chips (type 5170). These are inverting buffers which convert between line levels at the J1 and J2 connectors and TTL levels at the OCTART and modem latches.

5.3.8 Power Converter

The line drivers require + and −10 volts dc. The Q-bus backplane supplies only + 12 volts dc. A nominal + 10 volts is generated by dropping down the + 12 volts across two diodes. The −10 volts is derived from + 12 volts by a voltage converter. This device uses switched-mode power-supply techniques to generate the negative voltage. The circuit is built around a TL494 switching regulator (see Figure 5-5). This uses pulse-width modulation to regulate the −10 volt output.

Switching-pulses from the modulator switch a transistor (Q1) to convert a dc input to a pulsed dc current in an inductor. When Q1 is switched on, point X becomes positive, causing current to flow through L. During this period, energy is stored in the inductor. When Q1 is switched off, the polarity of the voltage across the inductor is inverted, and the energy stored in the inductor is transferred through the now forward-biased diode to the smoothing capacitors. As current is transferred to the output, the voltage at X rises until the diode is cut off again. The circuit will stay in this state until the next switching pulse turns Q1 on.

The inset of Figure 5-6 shows typical inductor current waveforms. With Q1 switched on, current rises linearly until Q1 is switched off again. With Q1 switched off, the collapsing field in the inductor maintains current flow, which reduces linearly as it is transferred to the output. The wider the switching pulses, the more power that is transferred to the output.

Feedback from the output is compared with a reference. If the output is too high, the pulse width is reduced; if too low, the pulse width is increased. This feedback action maintains output voltage regulation for varying loads. This same method of comparison is used to implement over-current protection. The inductor current is sensed across Rc. If this exceeds a preset limit, the switching pulse width is reduced. The switching frequency (60 kHz) is selected by Rs and Cs. If the oscillator is working, a sawtooth waveform can be seen at pin 5.

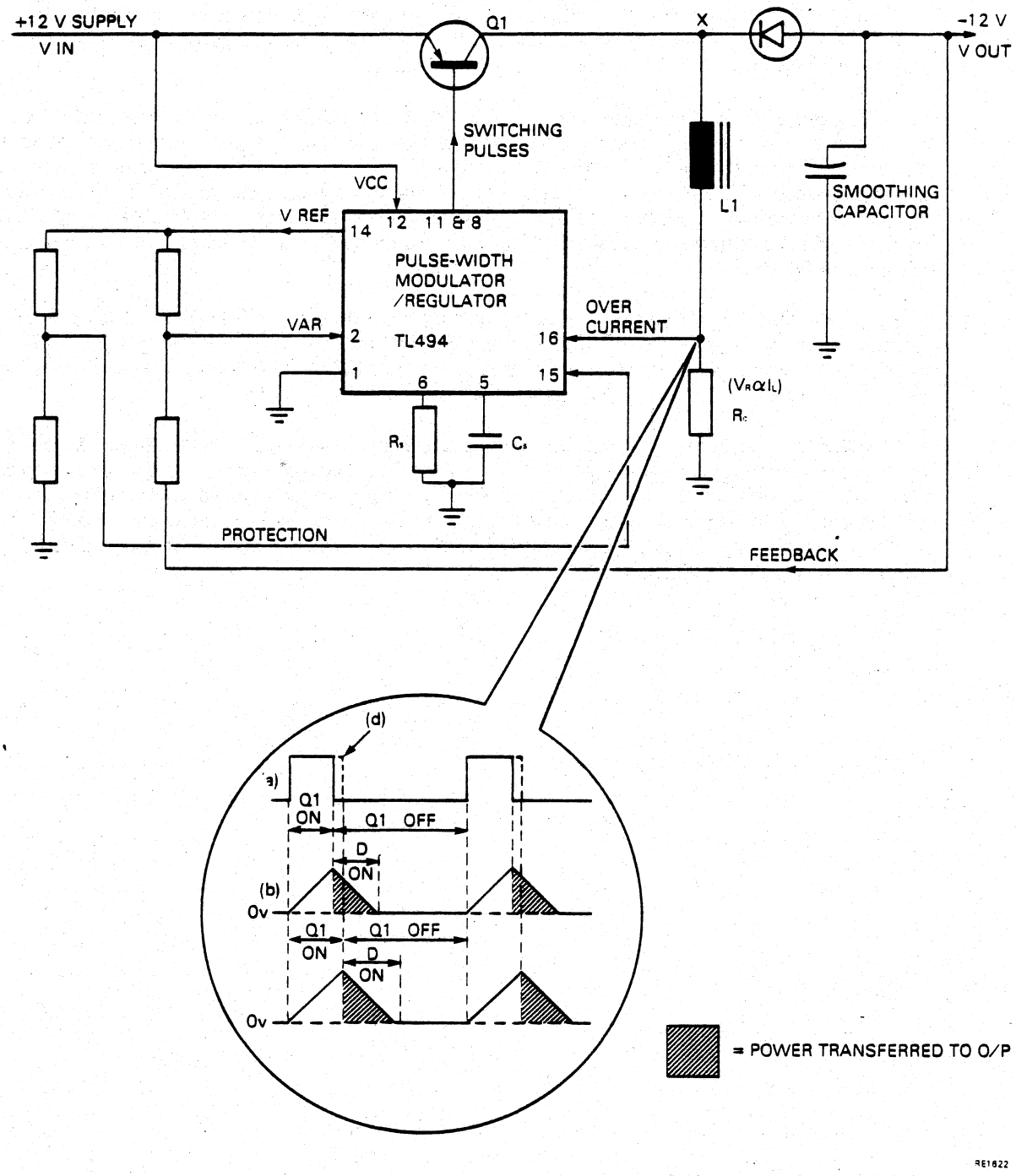


Figure 5-6 Voltage Converter

5.4 DATA FLOW

This section describes the general flow of data through the DHQ11 between the Q-bus and the serial lines, for both the receive and the transmit operations.

5.4.1 Data Flow For Character Reception

Data is clocked into the OCTART in serial form. When the OCTART has completed the serial-to-parallel conversion, it generates an interrupt (LINT.L) to the control chip (see Figure 5-7). The UAF sequencer quickly transfers the data into the four-word FIFO for the appropriate channel in RAM, and sets a receive-data-available flag. The UAS sequencer sees this flag and processes the character by moving it, together with the channel number and error information, to the top of the 256-word shared receive FIFO.

The CPU accesses the bottom of the receive FIFO by reading the RBUF register. This transfer is handled by the DIO sequencer.

5.4.2 Data Flow For Character Transmission

5.4.2.1 DMA Operation – The CPU starts a DMA operation by writing the start address for the channel into TBUFFAD1 and TBUFFAD2, writing the number of characters to be transmitted into TBUFFCNT, and then setting the DMA.START bit. The DMS sequencer detects DMA.START being set, and begins the DMA transfer to the appropriate transmit FIFO with the aid of the DMF sequencer. The UAS sequencer reads the status of that channel's transmit FIFO, removes the character (assuming there is one) from the bottom of the FIFO, places it in the Transmit Holding Register (THR), and sets the transmit-character-available flag for the channel. The THR is contained in RAM as an element of the control register area.

The OCTART interrupts the control chip when it is able to handle a transmit character. The UAF sequencer reads the transmit-character-available flag and, if it is set, transfers the character from the THR to the OCTART. The OCTART converts it to serial format, and transmits it to the line drivers.

5.4.2.2 Programmed I/O Operation – The host writes a single character to the TXCHAR register and sets the TX.VALID bit. Characters to be transmitted are handled by the DIO sequencer. The UAS sequencer removes this character from the TXCHAR register, places it in the THR, clears the TVD bit, and sets TX.ACTION. Transfer to the serial line then continues as described above for DMA transfers.

Subsequent TXCHAR transfers must only be initiated after the TX.ACTION has been set for the previous transfer.

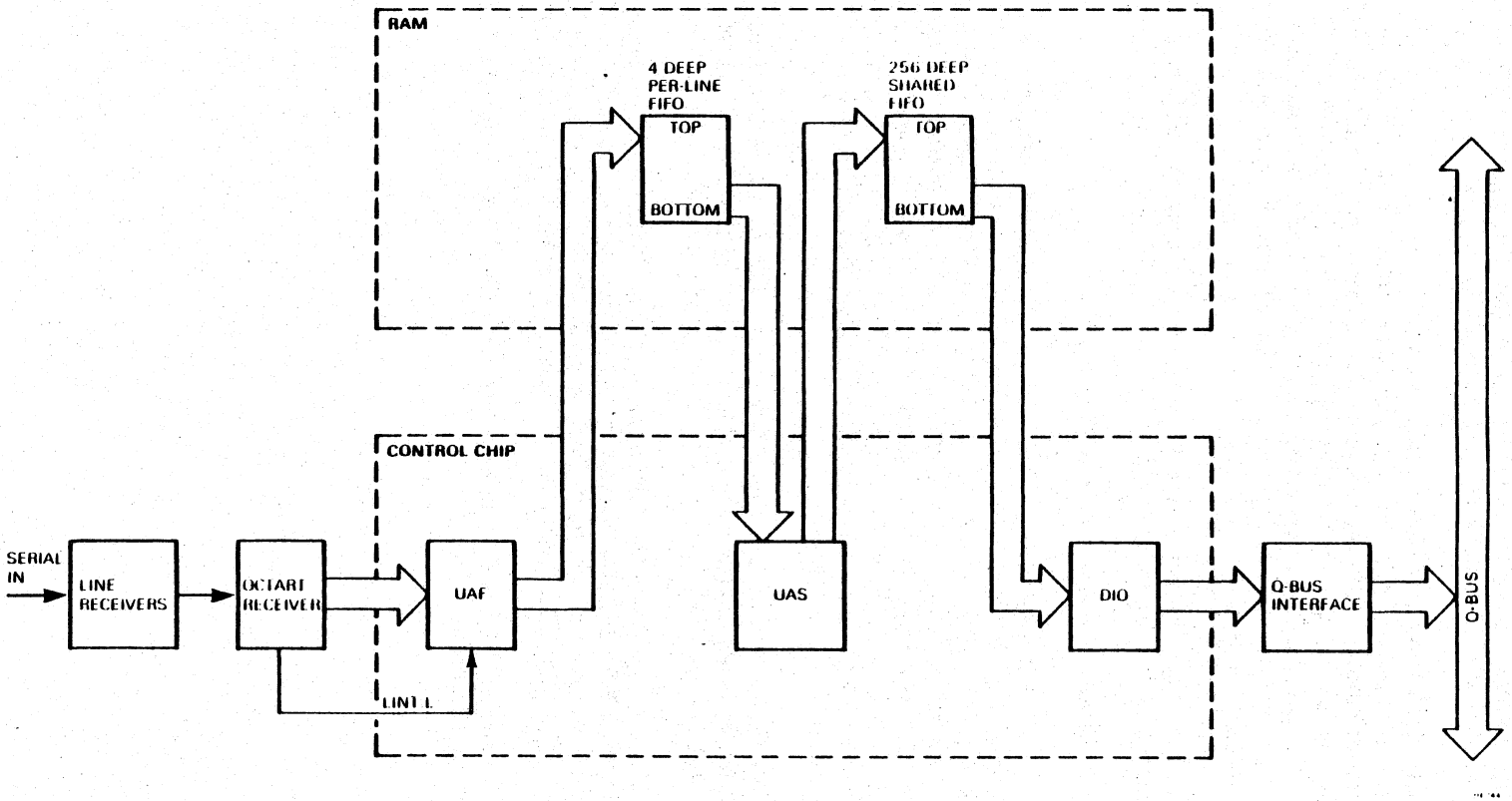


Figure 5-7 Receive Character Data Flow

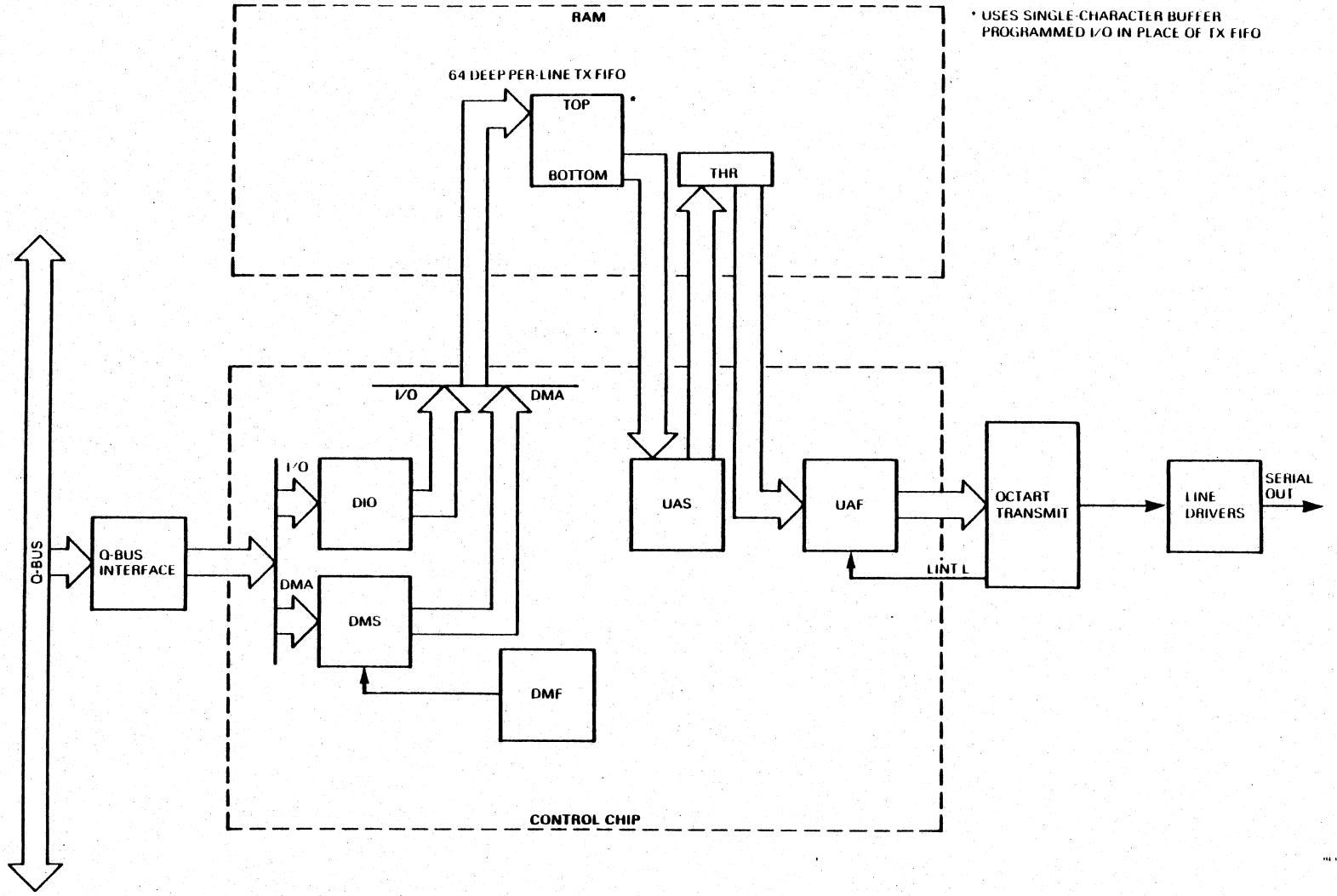


Figure 5-8 Transmit Character Data Flow

APPENDIX A
MODEM CONTROL

A.1 SCOPE

This appendix contains information useful to both the programmer and the engineer. It defines control signals, describes typical modem control methods, and warns against likely network faults. A detailed example of auto-answer operation is included.

A.2 MODEM CONTROL

The DHQ11 supports sufficient modem control to permit full-duplex operation over the public switched telephone network (PSTN) and over private telephone lines. Table A-1 lists the control leads supported by the DHQ11, together with an explanation of their use and purpose. In this appendix, the terms **modem** and **dataset** have the same meaning. They refer to the device which is used to modulate and demodulate the signals transmitted over the communications circuits.

Table A-1 Modem Control Leads

Name	EIA-232-D	V.24	25-Pin	Definition
GND	AB	102	7	Signal Ground. This is a reference level for the data and control signals used at the line interface.
TXD	BA	103	2	From DHQ11 to modem. This signal contains the serial bit stream to be transmitted to the remote station.
RXD	BB	104	3	From modem to DHQ11. This signal is the serial bit stream received by the modem from the remote station.
RTS	CA	105	4	From DHQ11 to modem. Causes the modem's carrier to be placed on the line.
CTS	CB	106	5	From modem to DHQ11. Indicates that the modem has successfully placed its carrier on the line, and that data presented on circuit BA will be transmitted to the communication channel.
DSR	CC	107	6	From modem to DHQ11. Indicates that the modem has completed all call establishment functions and is successfully connected to a communications channel.

Table A-1 Modem Control Leads (Cont.)

Name	EIA-232-D	V.24	25-Pin	Definition
DTR	CD	108/2	20	From DHQ11 to modem. Indicates to the modem that the DHQ11 is powered up and ready to answer an incoming call.
DCD	CF	109	8	From modem to DHQ11. Indicates to the DHQ11 that the remote station's carrier signal has been detected and is within appropriate limits.
RI	CE	125	22	From modem to DHQ11. Indicates that a new incoming call is being received by the modem.

The DHQ11 modem control interface can be used in many applications. These include control of serial line printers, terminal cluster controllers, and industrial I/O equipment, in addition to the more usual applications in telephone networks. The use of the control leads described in Table A-1 is therefore completely dependent on the application, although there are international standards which telephone network applications should obey. There are no hardware interlocks between the modem control logic and the transmitter and receiver logic. Program control manages these actions, as necessary.

A subset of the leads listed in Table A-1 could be used to establish a communications link using modems connected to the switched telephone network. Ring Indicator (RI), Data Terminal Ready (DTR), and Data Carrier Detected (DCD) are the absolute minimum requirements. In some countries Dataset Ready (DSR) is also needed. It is usually desirable, however, to implement modem control protocols which will operate over most telephone systems in the world. Also, some protection should be included to guard against network faults, particularly in applications such as dial-up timesharing systems. Such faults include:

- Making a channel permanently busy (hung) because of a misdialed connection from a non-data station
- Connecting a new incoming call on an in-use channel. This fault might occur, for example, after a temporary carrier loss, if the host system assumed that the carrier was reasserted by the original caller.

Modem control with some protection against common faults, and which is compatible with the telephone networks in most geographic areas, can be implemented by using all the signals listed in Table A-1, in the way described by the CCITT V.24 recommendations. Section A.2.1 describes a method of implementing a full-duplex auto-answer communications link through modems over the PSTN. It is provided here only to show the operation and interaction of DHQ11 modem control leads in a typical application.

A.2.1 Example Of Auto-Answer Modem Control For The PSTN

The system operator determines which DHQ11 channels should be configured for either local or remote operation. Local operation implies control of data-leads-only, while remote operation implies that modem control will be supported. The host software will assert DTR and RTS together with the LINK.TYPE bit in the LNCTRL register for all DHQ11 channels configured for remote operation. DTR informs the modem that the DHQ11 is powered up and ready to acknowledge control signals from

the modem. RTS is asserted for the full-duplex mode of operation, and causes the modem to place its carrier on the telephone line when the modem answers a call. Link Type (LNCTRL<8>) enables modem status information to be placed in the receive character FIFO, where it will be handled by an interrupt service routine. Modem status changes are always reported in the STAT register regardless of the state of LNCTRL<8>. The modem is now prepared to auto-answer an incoming call.

Dialing the modem's number causes RI to be asserted at the line interface. This informs the DHQ11 that a new call is being received. RI has to be in a stable state for at least 30 ms, or the change will not be reported by the DHQ11. Since DTR is already asserted, the modem will auto-answer the incoming call and start its handshaking sequence with the calling station. The time needed to complete the handshaking sequence can be in the order of tens of seconds if fallback-mode speed selection and satellite links are involved. The modem will assert DSR to indicate to the DHQ11 that the call has been successfully answered and a connection established.

NOTE

On some older types of modem used on the PSTN, the opposite effect is also true. The RI signal may be very short, or it may not even occur if DTR was previously asserted. When this type of modem answers an incoming call, it asserts DSR almost immediately and deasserts RI at the line interface. Programs must therefore expect RI or DSR or DCD as the first dataset status change received from the modem when establishing a connection.

As RTS was previously asserted, the modem's carrier will be placed on the line when DSR is asserted. When the modem has successfully placed its carrier on the line it will assert CTS. This indicates to the DHQ11 that it can start to transmit data. If the incoming call is the result of a misdialed number, a carrier signal may never be received. To guard against this, the host starts a timer when it detects RI or DSR. This is usually in the range 15 to 40 seconds, within which time the carrier must be detected. When the modem detects the remote modem's carrier signal on the line, it will assert DCD. This indicates to the DHQ11 that data is valid on the RXD line.

The modem can now exchange data between the DHQ11 and the calling station for as long as DCD, DSR, and CTS stay asserted. If any of these three signals disappears, or if RI is detected during normal transmission, a fault condition is indicated. A change of state of any of these signals causes an interrupt through the receive FIFO.

The handling of the fault conditions now becomes country-specific, since some telephone systems tolerate a transient carrier loss, while others do not. In the USA it is usual to proceed with a call if carrier resumes within two seconds. In non-USA areas it is possible for telephone supervisory signals, such as dial-tone, to be misinterpreted by the modem as a resumption of carrier. In this case the host program would assume that the connection had been re-established to the original caller and would cause a 'hung' channel. To prevent this, DTR should be deasserted immediately after the loss of DCD, CTS, or DSR, to abort the connection. DTR should stay deasserted for at least two seconds, after which time a new call could be answered.

APPENDIX B
FLOATING ADDRESSES

B.1 FLOATING DEVICE ADDRESSES

On Q-bus systems a block of addresses in the top 4K words of address space is reserved for options with floating device addresses. This range is from 17760010_8 to 17763776_8.

Options which can be assigned floating device addresses are listed in Table B-1. This table gives the sequence of addresses for both UNIBUS and Q-bus options. For example, the address sequences could be:

DJ11
DH11
DQ11
DU11/DUV11 and so on.

Having one list allows us to use one set of configuration rules and one configuration program.

Table B-1 Floating Device Address Assignments

Rank	Device	Size (Decimal)	Modulus (Octal)	Address
1	DJ11 gap	4	10	17760010
2	DH11 gap	8	20	17760020
3	DQ11 gap	4	10	17760030
4	DU11, DUV11 gap	4	10	17760040
5	DUP11 gap	4	10	17760050
6	LK11A gap	4	10	17760060
7	DMC11/DMR11 gap	4	10	17760070
8	DZ11/DZV11/DZS11/DZ32 gap	4	10 ***	17760100
9	KMC11 gap	4	10	17760110
10	LPP11 gap	4	10	17760120
11	VMV21 gap	4	10	17760130
12	VMV31 gap	8	20	17760140
13	DWR70 gap	4	10	17760150
14	RL11, RLV11 gap	4	10 *	17760160
15	LPA11-K gap	8	20 *	17760200
16	KW11-C gap	4	10	17760210
17	VSV21 gap	4	10	17760220
18	RX11/RX211/RXV11/RXV21 gap	4	10 *	17760230

Table B-1 Floating Device Address Assignments (Cont.)

Rank	Device	Size (Decimal)	Modulus (Octal)	Address
19	DR11-W gap	4	10	17760240
20	DR11-B gap	4	10 **	17760250
21	DMP11 gap	4	10	17760260
22	DPV11 gap	4	10	17760270
23	ISB11 gap	4	10	17760300
24	DMV11 gap	8	20	17760320
25	DEUNA gap	4	10 *	17760330
26	KDA50/UDA50/RQDX3 gap	2	4 *	17760334
27	DMF32 gap	16	40	17760340
28	KMS11 gap	6	20	17760360
29	VS100 gap	8	20	17760400
30	TU81 gap	2	4	17760404
31	KMV11 gap	8	20	17760420
32	DHV11/DHU11/DHQ11 gap	8	20	17760440

* The first device of this type has a fixed address. Any extra devices have a floating address.

** The first two devices of this type have a fixed address. Any extra devices have a floating address.

*** The DZ11-E and DZ11-F are treated as two DZ11s.

The address assignment rules are as follows.

1. Addresses, starting at 17760010_8 for Q-bus systems, are assigned according to the sequence of Table B-1.

2. Option and gap addresses are assigned according to the octal modulus as follows.

   - Devices with an octal modulus of 4 are assigned an address on a 4_8 boundary (the two lowest-order address bits = 0)
   - Devices with an octal modulus of 10 are assigned an address on a 10_8 boundary (the three lowest-order address bits = 0)
   - Devices with an octal modulus of 20 are assigned an address on a 20_8) boundary (the four lowest-order address bits = 0)
   - Devices with an octal modulus of 40 are assigned an address on a 40_8 boundary (the five lowest-order address bits = 0)

3. Address space equal to the device's modulus must be allowed for each device which is connected to the bus.

4. A 1-word gap, assigned according to rule 2, must be allowed after the last device of each type. This gap could be bigger when rule 2 is applied to the following rank.

5. A 1-word gap, assigned according to rule 2, must be allowed for each unused rank on the list if a device with a higher address is used. This gap could be bigger when rule 2 is applied to the following rank.

If extra devices are added to a system, the floating addresses may have to be reassigned in agreement with these rules.

B.2 FLOATING VECTORS

Each device needs two 16-bit locations for each vector. For example, a device with one receive and one transmit vector needs four words of vector space.

The vector assignment rules are as follows:

1. Each device occupies vector address space equal to 'Size' words. For example, the DLV11-J occupies 16 words of vector space. If its vector were 300_8, the next available vector would be at 340_8.

2. There are no gaps, except those needed to align an octal modulus.

Table B-2 Floating Vector Address Assignments

Rank	Device	Size (Decimal)	Modulus (Octal)
1	DC11	4	10
1	TU58	4	10
2	KL11	4	10 **
2	DL11-A	4	10 **
2	DL11-B	4	10 **
2	DLV11-J	16	10
2	DLV11, DLV11-F	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	DM11-BB/BA	2	4
7	DH11 modem control	2	4
8	DR11-A, DRV11-B	4	10
9	DR11-C, DRV11	4	10
10	PA611 (reader + punch)	8	10
11	LPD11	4	10
12	DT07	4	10
13	DX11	4	10
14	DL11-C to DLV11-E	4	10
15	DJ11	4	10
16	DH11	4	10
17	VT40	8	10
17	VSV11	8	10
18	LPS11	12	10

Table B-2 Floating Vector Address Assignments (Cont.)

Rank	Device	Size (Decimal)	Modulus (Octal)
19	DQ11	4	10
20	KW11-W, KWV11	4	10
21	DU11, DUV11	4	10
22	DUP11	4	10
23	DV11 + modem control	6	10
24	LK11-A	4	10
25	DWUN	4	10
26	DMC11/DMR11	4	10
27	DZ11/DZS11/DZV11, DZ32	4	10
28	KMC11	4	10
29	LPP11	4	10
30	VMV21	4	10
31	VMV31	4	10
32	VTV01	4	10
33	DWR70	4	10
34	RL11/RLV11	2	4 *
35	TS11, TU80	2	4 *
36	LPA11-K	4	10
37	IP11/IP300	2	4 *
38	KW11-C	4	10
39	RX11/RX211 RXV11/RXV21	2	4 *
40	DR11-W	2	4
41	DR11-B	2	4 *
42	DMP11	4	10
43	DPV11	4	10
44	ML11	2	4 ***
45	ISB11	4	10
46	DMV11	4	10
47	DEUNA	2	4 *
48	KDA50/RQDX3	2	4 *
49	DMF32	16	4
50	KMS11	6	10
51	PCL11-B	4	10
52	VS100	2	4
53	TU81	2	4
54	KMV11	4	10
55	KCT32	4	10
56	IEX	4	10
57	DHV11/DHU11/DHQ11	4	10

Table B-2 Floating Vector Address Assignments (Cont.)

Rank	Device	Size (Decimal)	Modulus (Octal)
58	DMZ32/CPI32(async)	12	4
59	CPI32(sync)	12	4
60	QNA	12	4
61	QVSS	4	10
62	VS31	2	4
63	LNV11	2	4
64	QPSS	2	4
65	QTA	2	4
66	DSV11	2	4

* The first device of this type has a fixed vector. Any extra devices have a floating vector.

** If a KL11 or DL11 is used as the console, it has a fixed vector.

*** ML11 is a MASSBUS device which can connect to UNIBUS via a bus adapter.

APPENDIX C
AUTOMATIC FLOW CONTROL

C.1 OVERVIEW

Flow control is the control of the flow of data along a communications line, to prevent an overspill of queues or buffers, or to prevent the loss of data which the receiver is unable to accept.

The method of flow control adopted for the DHQ11 is datastream-embedded ASCII control characters. The control characters used are XOFF (octal 023) and XON (octal 021). XOFF stops transmission and XON starts transmission. The codes are transmitted in the opposite direction to that of the data they control.

The DHQ11 has one mode of operation for transmitted data (received flow-control characters) and two modes of operation for received data (transmitted flow-control characters). Each mode can be enabled on a 'per channel' basis. Each direction of flow is discussed separately within this appendix.

C.2 CONTROL OF TRANSMITTED DATA

The transmitted-data mode of flow control is the simplest of the three flow-control modes of the DHQ11.

When the DHQ11 receives an XOFF character for a particular channel, the TX.ENA bit for that channel is cleared. When this bit is clear, the DHQ11 will not transmit any data on that channel; however, internally generated flow-control characters will still be transmitted. When an XON character is received, the TX.ENA bit for that channel is set. Figure C-1 illustrates the operation of the transmitted data flow control.

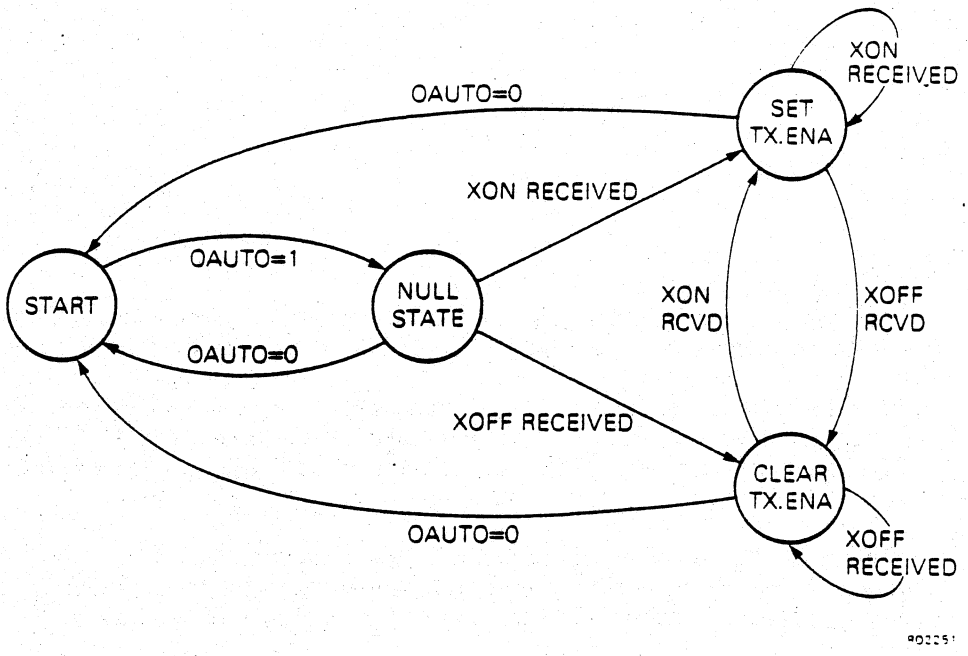


Figure C-1 Transmitted Data Flow Control

Only characters without transmission errors are checked for XON and XOFF codes. The characters have their parity bit stripped before comparison.

NOTE

For the automatic flow control to operate correctly, the terminal must also recognize and respond to flow-control characters.

The transmitted-data mode of flow control is enabled by setting OAUTO (bit 4 of the line control register), and is disabled by clearing it. The default for this mode is disabled.

Received flow-control characters are processed in the same way as normal characters, and are placed into the receive FIFO. This is not affected by OAUTO, but these characters can be filtered out by setting DISAB.XRPT. If DISAB.XRPT is set, you do not need a routine in your software driver to filter flow-control characters from the data stream.

C.3 CONTROL OF RECEIVED DATA

Received-data flow control is slightly more complicated than transmitted-data flow control. Therefore the two modes of received-data flow control are described separately.

C.3.1 Flow Control By The Level Of The Receive FIFO

Occasionally, the program may not be able to empty the receive FIFO as fast as the received data is filling it. Because the program does not know how full the receive FIFO is, it cannot take action to prevent data loss. To overcome this problem, the DHQ11 can be programmed on a 'per channel' basis. When the receive FIFO becomes three-quarters full, an XOFF is sent to the channels from which data is

received. An XOFF character is then sent in response to every second received character, until the receive FIFO level drops below half full. An XON character is then transmitted. The operation of receive FIFO-level flow control is shown in Figure C-2.

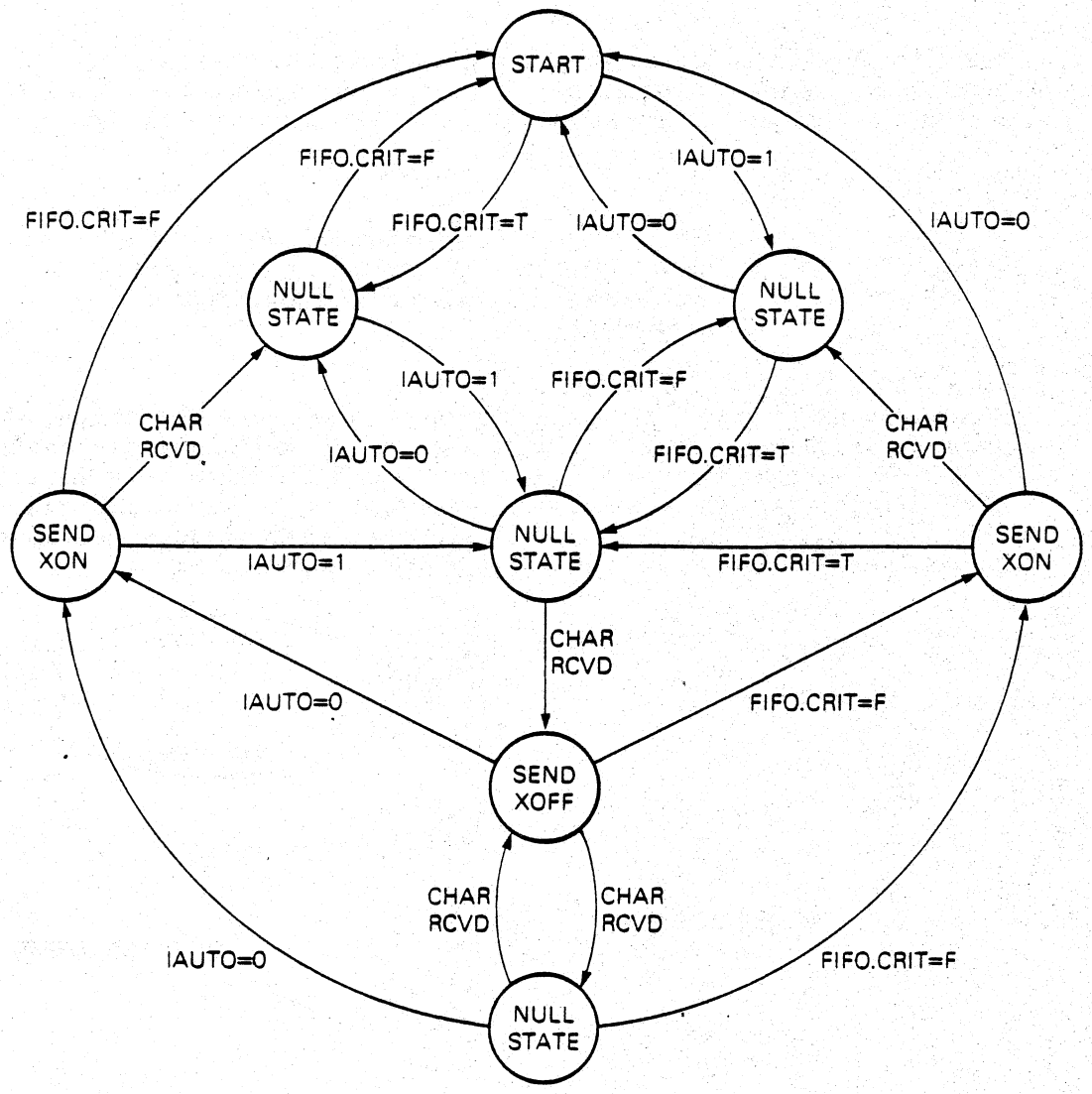


Figure C-2 Receive FIFO-Level Flow Control

The receive FIFO-level flow-control mode is enabled by setting IAUTO (bit 1 of the line control register), and disabled by clearing the bit. The default for this mode is disabled. If IAUTO is cleared after an XOFF is sent, but before the receive FIFO level drops below half full, an XON is still sent.

NOTE

FIFO.CRIT is set (T) when the receive FIFO is being filled, and contains 192 characters. It is cleared (F) when receive FIFO reaches 127 characters as it is being emptied.

C.3.2 Flow Control By Program Initiation

Occasionally, the program itself may need to invoke flow control, for example, when host buffers become full. To allow this, the DHQ11 has a FORCE.XOFF bit (bit 5 of the line control register). When the FORCE.XOFF bit is set, the DHQ11 transmits an XOFF character for that channel. A further XOFF bit is transmitted for every second character received on the channel afterwards. An XON is sent when the FORCE.XOFF bit is cleared. Figure C-3 shows the operation of program-initiated flow control. The FORCE.XOFF bit is cleared by a DHQ11 reset sequence.

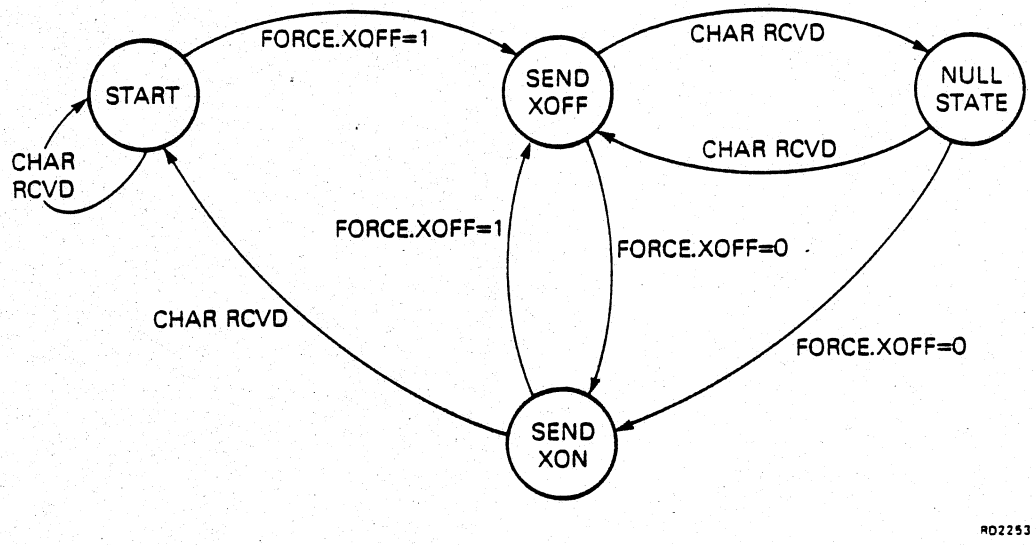


Figure C-3 Program-Initiated Flow Control

NOTE

If the program sets the FORCE.XOFF bit and then immediately clears it, the XOFF code may not be transmitted. This is because there is a delay of up to 350 microseconds before the DHQ11 detects the need to send an XOFF. If the conditions for sending an XOFF clear before within this time delay, no XOFF code will be sent.

C.3.3 Mixing The Two Types Of Received-Data Flow Control

To calculate the effect of using the two modes, they should be logically ORed together: an XON will not be sent until both sources are inactive. An XOFF will be sent when FORCE.XOFF is set, even if FIFO-critical mode is active and an XOFF has already been sent on that channel. If the receive FIFO critical mode becomes active whilst FORCE.XOFF is set, then another XOFF is sent in response to the next received character.

APPENDIX D
GLOSSARY OF TERMS

D.1 SCOPE

This appendix contains a glossary of terms used in this manual and in other DIGITAL technical manuals in this series. The terms are in alphabetical order for easy reference.

D.2 GLOSSARY

Asynchronous. A method of serial transmission in which data is preceded by a start bit and followed by a stop bit. The receiver provides the intermediate timing to identify the data bits.

Auto-answer. A facility of a **modem** or terminal to answer a call automaticallly.

Auto-flow. Automatic flow control. A method by which the DHQ11 controls the flow of data by means of special characters within the data stream.

Backward channel. A channel which transmits in the opposite direction to the usual data flow. Normally used for supervisory or control signals.

Base address. The Q-bus address of the first (lowest) device register (CSR).

BMP. Background Monitor Program.

CCITT. Comité Consultatif International de Téléphonie et de Télégraphie. An international standards committee for telephone, telegraph, and data communications networks.

Dataset. See **modem**.

DMA. Direct Memory Access. A method which allows a bus master to transfer data to or from system memory without using the host CPU.

Duplex. A method of transmitting and receiving on the same channel at the same time.

EIA. Electrical Industries Association. An American organization with the same function as the CCITT.

FCC. Federal Communications Commission. An American organization which regulates and licenses communications equipment.

FIFO. First In First Out. The term describes a register or memory from which the oldest data is removed first.

Floating address. An address assigned to an option which does not have a fixed address allocated. The address is dependent on other floating address devices connected to the bus.

Floating vector. An interrupt vector assigned to an option which does not have a fixed vector allocated. The vector is dependent on other floating vector devices connected to the bus.

FRU. Field-Replaceable Unit.

IC. Integrated Circuit.

I/O. Input/Output.

LSB. Least-Significant Bit.

MMJ. Modified Modular Jack.

Modem. The word is a contraction of MOdulator DEModulator. A modem interfaces a terminal to a transmission line. A modem is sometimes called a **dataset**.

MSB. Most Significant Bit.

Multiplexer. A device which allows a number of inputs to share one common output.

Null modem. A cable which allows two terminals which use **modem** control signals to be connected together directly. It is only possible over short distances.

OCTART. A single **IC** containing eight **UARTs**.

PCB. Printed Circuit Board.

Protocol. A set of rules which define the control and flow of data in a communications system.

PSTN. Public Switched Telephone Network.

Q-bus. A global term for a specific DIGITAL bus on which the address and data are multiplexed.

RAM. Random Access Memory.

RFI. Radio Frequency Interference.

ROM. Read Only Memory.

Split-speed. A facility of a data communications channel which can transmit data at a different speed from the received data.

UART. Universal Asynchronous Receiver Transmitter. A device which converts between serial and parallel data, used for transmission and reception of serial **asynchronous** data on a channel.

XOFF. A control code (23_8) used to disable a transmitter. Special hardware or software is needed for this function.

XON. A control code (21_8) used to enable a transmitter which has been disabled by an **XOFF** code.

APPENDIX E
DHQ11 Q-BUS CONNECTIONS

Table E-1 DHQ11 Q-Bus Connections

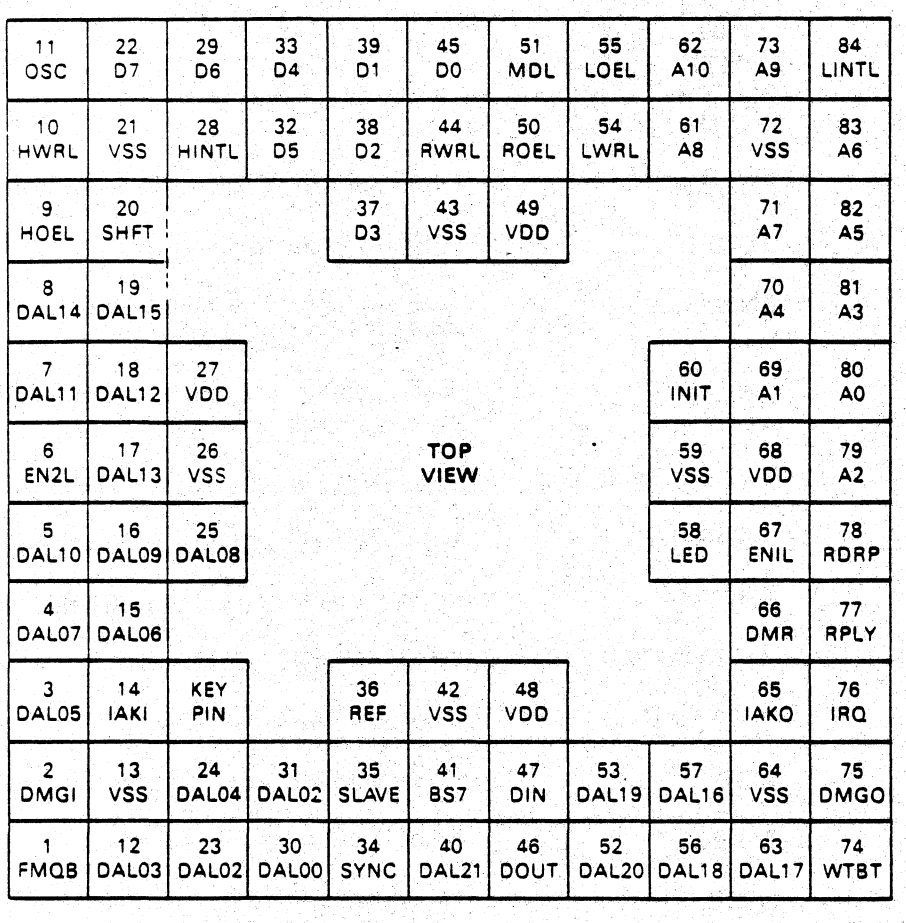
Category	Signal	Function	Pin Number
Data/Address	BDAL0.L — 1.L	Data/Address Lines	AU2 — AV2
	BDAL2.L — 15.L		BE2 — BV2
	BDAL16.L — 17.L		AC1 — AD1
	BDAL18.L — 21.L		BC1 — BF1
Data Control	BDOUT.L	Data Output Strobe	AE2
	BRPLY.L	Reply Handshake	AF2
	BDIN.L	Data Input Strobe	AH2
	BSYNC.L	Synchronize Strobe	AJ2
	BWTBT.L	Write Byte Control	AK2
	BBS7.L	I/O Page Select	AP2
Interrupt Control	BIRQ.L	Int. Req. Level 4	AL2
	BIAKI.L	Int. Ack. Input	AM2
	BIAKO.L	Int. Ack. Output	AN2
DMA Control	BDMR.L	DMA Request	AN1
	BDMGI.L	DMA Grant Input	AR2
	BDMGO.L	DMA Grant Output	AS2
	BSACK.L	Bus Grant Acknowledge	BN1
	BREF.L	Refresh and Block Mode	AR1
System Control	BINIT.L	Initialization Strobe	AT2
Power Supplies	+5 V	Dc volts	AA2 — DA2
	+12 V	Dc volts	AD2, BD2
Grounds	GND	Ground Connections	AC2 — DC2
	GND	Ground Connections	AT1 — DT1
	GND	Ground Connections	AJ1 — BJ1
	GND	Ground Connections	AM1 — BM1

APPENDIX F
CONTROL CHIP AND OCTART — PINOUTS

F.1 SCOPE

This appendix describes the signals associated with the control chip and the OCTART. It is to be used in conjunction with the maintenance printset.

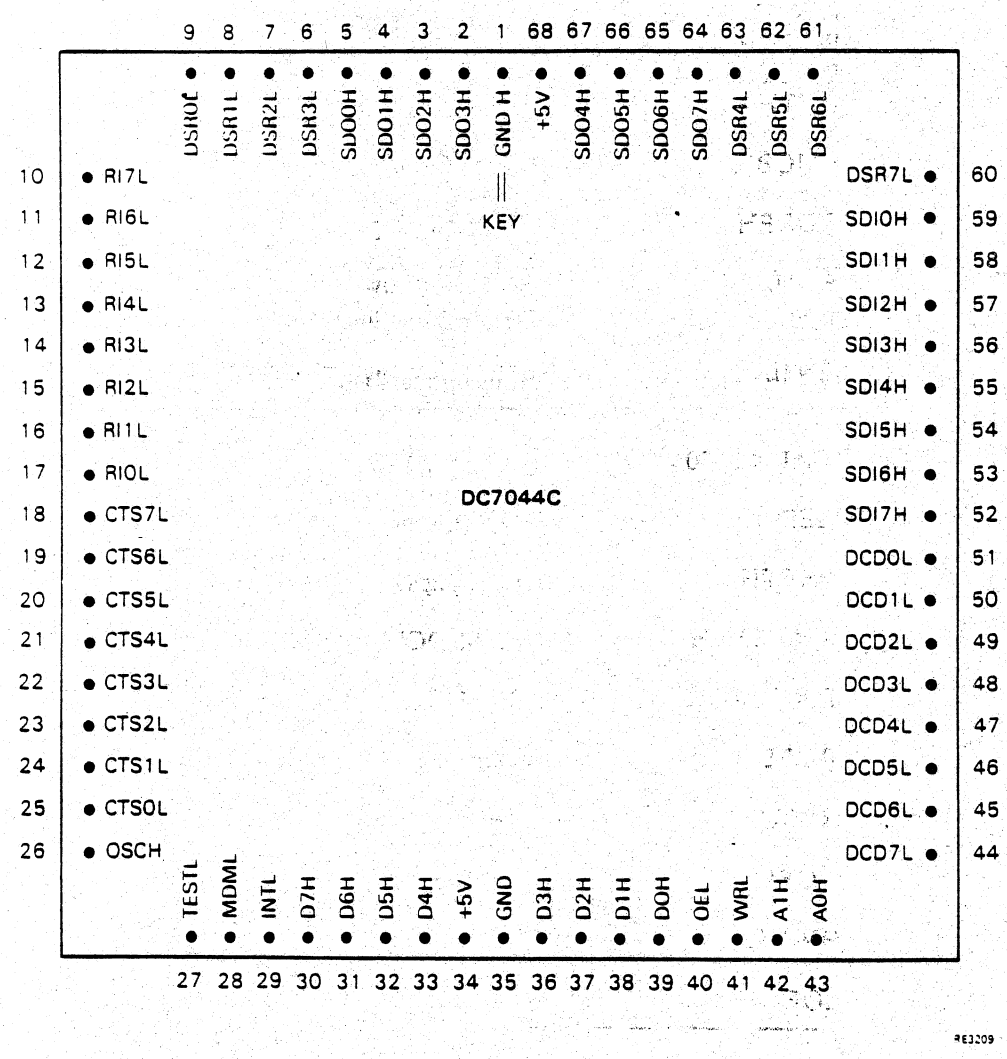
F.2 CONTROL CHIP



Signal Name	Description
SLAVEH	Controls the direction of Q-bus transceiver E9. Deasserted during bus mastership since TSACKH is a pull-up. this asserts BSACKl on the Q-bus
RPLYH DMRH IRQH DMG0H IAK0H SYNCH BS7H DINH REFH DMGIH IAKIH WTBTH DOUTH INITH	Q-bus signals. See Appendix E for details
FMQBH	From Q-bus (normally high) — affects the direction of DAL<15:00>.
RDRPH	Normally high, set low to select Q-bus transceiver E1 as a transmitter.
EN1L	Normally low, is set high to disable the Q-bus transceiver E1 when RDRPH is changing state.
EN2L	Normally low, is set high to disable the Q-bus transceiver E9 when SLAVEH is changing state.
DAL<21:00>H	Buffered Q-bus data and address lines.
LEDH	Self-test output to LED (through DC021 driver).
SHFTH	Shift register input (from switchpack shift registers).
A<10:0>H	RAM OCTART address bus
D<7:0>H	RAM OCTART data bus
ROEL	RAM output enable — active low (read strobe)
RWRL	RAM write strobe — active low
HOEL	Not used by DHQ11
HWRL	Not used by DHQ11
LOEL	Low-OCTART read strobe

Signal Name	Description
LWRL	Low-OCTART write strobe
HINTL	Not ~~used~~ by DHQ11
LINTL	Low-OCTART interrupt to control chip
MDL	Modem latch write, active low
OSCH	14.7456 MHz oscillator input

F.3 OCTART



Signal Name	Description
D<7:0>H	RAM OCTART data bus
A<1:0>H	Address pins for register selection
TESTL	Used for manufacturing test
MDML	Modem support — asserted to enable modem control lines
OEL	Read strobe
WRL	Write strobe
OSCH	14.7456 MHz oscillator input
INTL	Interrupt output
SDO<7:0>H	Serial data out
SDI<7:0>H	Serial data in
CTS<7:0>L	Clear to send
DSR<7:0>L	Data set ready
DCD<7:0>L	Data carrier detect
RI<7:0>L	Ring indicator

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