INSTRUCTION MANUAL

DF32
DISK FILE AND CONTROL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

DEC-D8-IDFA-D

DF32

DISK FILE AND CONTROL INSTRUCTION MANUAL

March 1968

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Typical PDP-8/S and Disk File Installation

CHAPTER 1
INTRODUCTION

The Type DF32 Disk File and Control, manufactured by Digital Equipment Corporation, Maynard, Massachusetts is a fast, random or sequential access, bulk storage device used with the PDP-8, PDP-8/S, or PDP-8/I computers for memory expansion. The DF32 provides a capacity of 32,768 13-bit words which are stored on a rotating disk.

Up to three type DS32 Extender Disks can be attached to the DF32, each of which extends the bit capacity by 32K for a total of 131,072 13-bit words as shown in Figure 1-1.

The disk file is a program controlled device used in conjunction with the PDP-8, PDP-8/S, or PDP-8/I, and operates through the 3-cycle data break facility of the computers.

1.1 PURPOSE AND SCOPE

This manual and the referenced documents herein provides operation, programming, and maintenance information on both the Type DF32 Disk File and Control and DS32 Extender Disk. The programming information, which includes sample programs for storage access, is presented in sufficient detail to allow operating programs to be written. Although references throughout this manual are primarily made to the PDP-8 computer, the information may be assumed to apply equally to the PDP-8/I and PDP-8/S except where specifically noted otherwise.

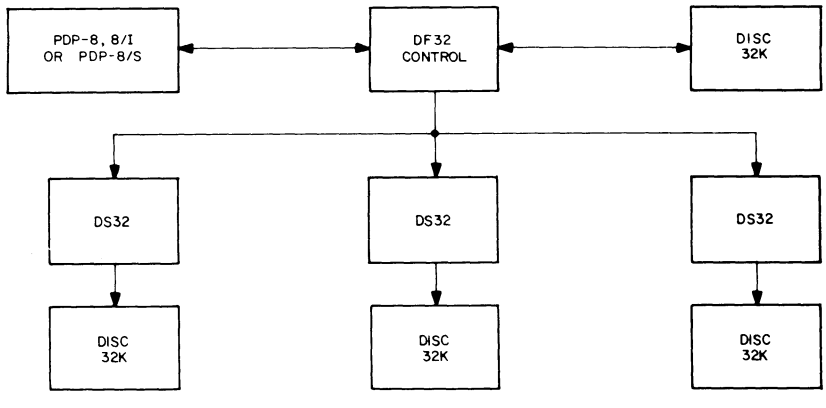


Figure 1-1 DF32 System Block Diagram

The information in this manual is intended for use by persons familiar with DEC digital logic and the operation of the PDP-8, PDP-8/S, and PDP-8/I computers. The maintenance information and routines require knowledge of the operation of bulk storage devices.

1.2 REFERENCE DOCUMENTS AND PROGRAMS

1.2.1 Manuals

Table 1-1 is a listing of the available publications which augment the information contained in this manual. These publications may be obtained upon request from the nearest DEC office or from the following address:

Digital Equipment Corporation
Main Street
Maynard, Massachusetts

Table 1-1
Reference Documents

Document	Description
Digital Logic Handbook (C105)	Function and specifications of FLIP-CHIP modules, cabinets, power supplies and accessories.
PDP-8 Maintenance Manual (F87)	Theory, operation, and maintenance information on the PDP-8 Processor.
PDP-8/S Maintenance Manual (F87S)	Theory, operation, and maintenance information on the PDP-8/S Processor.
PDP-8/I Maintenance Manual	Theory, operation, and maintenace information on PDP-8/I Processor.
Small Computer Handbook (C500)	Describes operation and programming of PDP-8 and PDP-8/S computers.

1.2.2 Operation and Maintenance Programs

Table 1-2 lists the operating and maintenance programs available for the DF32 and DS32 systems.

Table 1-2
Operation and Maintenance Programs

Program	Description
DF32 Software Package	Perforated program tapes and description of symbolic assembly, assembly language, and utility subroutines.
DF32 Diskless Logic Tests (Maintenance)	Tests master and extender logic without the disk in operation.
DF32 Disk Data, Mini Disk (Maintenance)	Tests the entire disk logic and disk including the interface, addressing and data.

1.3 SYSTEM SPECIFICATIONS

The general specifications for the disk file systems are listed in Table 1-3.

Table 1-3
Disk File System Specifications

Storage capacity	DF32 32,768 13-bit words DS32 32,768 13-bit words per DS32 for a total of 131,072 words per system
	60-Hz power 50-Hz power
Data transfer rate	66 μs per word 80 μs per word
Average access time	16.67 ms 20.0 ms
Write lock switches	Inhibit writing on lower and/or upper 16K of any 32K disk surface, and can inhibit one or more, or all disks in an expanded memory system.
Addressing scheme	Random or sequential addressing from 0 to 32,768 words, with variable block size from one word to 4,096 words.
Data assembly	Read/write to and from disk is in serial, with external transfer in parallel, by word.
Timing track	One, with one spare.
Address track	One, with one spare.
Data tracks	16
Words per track	2,048
Recording method	NRZI
Density	1100 bpi
Operating environment	Ambient temperature: Maximum: 32 to 130°F Recommended: 70 to 85°F Relative humidity: 20 to 80%
Heat dissipation	500W
Power requirements	117V, 60 Hz, single phase, ac, for DF32 or DS32 117V, 50 Hz, single phase, ac, for DF32A or DS32A

1.4 PHYSICAL DESCRIPTION

The DF32 interface, control logic, and mechanical components are mounted as an integral unit on a separate frame as shown on Figure 1-2. This unit can be installed within a DEC standard cabinet or any 19-in. relay rack. Track slides, attached on the side, allow the unit to be extended for servicing. The basic DF32 unit consists of two mounting panels for the DEC modules, with the wiring side facing the front of the unit. The disk file, consisting of a disk, drive motor, read/write heads, and photo cell amplifier are mounted separately at the rear of the unit. The overall dimensions of the DF32 are as follows: 10-1/2 in. high, 19 in. wide, 23-1/4 in. deep (21-1/4 in. deep from mounting surface, and 2-3/8 in. in front of mounting surface).

Each DS32 Extender is mounted on a similar frame with track slides and has the same dimensions as listed for the DF32. The DS32 unit, however, containing the disk file and analog-to-digital conversion logic, is controlled by signals and data supplied from the DF32. A complete extended memory system consisting of one DF32, three DS32 units, a Type 728 Power Supply and power control panel can be housed in a single bay of a standard rack or cabinet. When installed, sufficient cooling is provided by a fan mounted on the bottom of each unit. Additional system arrangements are also available to suit customer requirements.

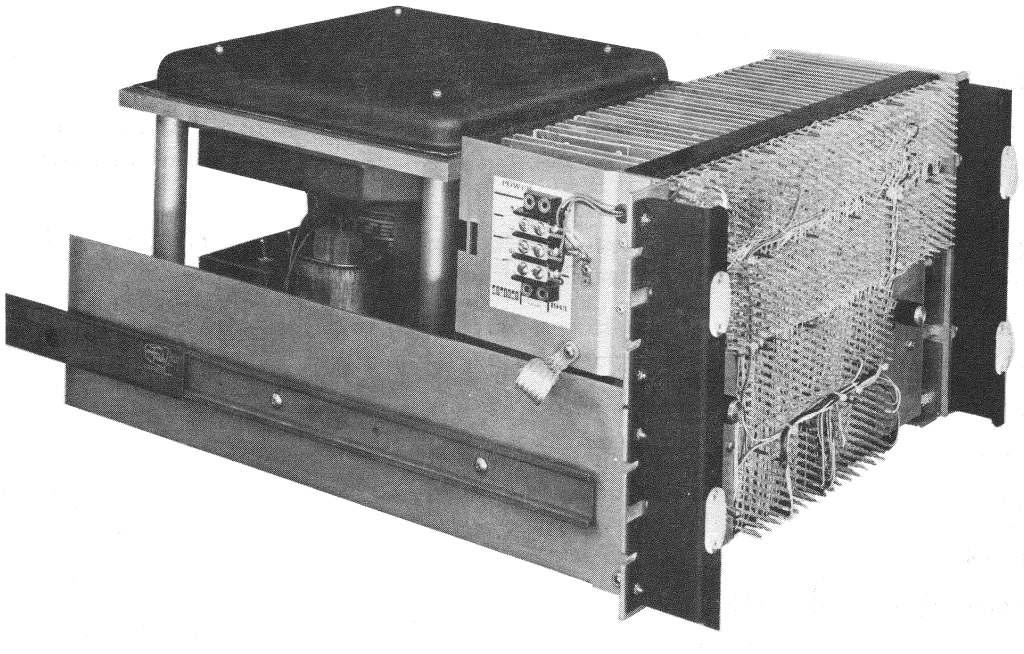


Figure 1-2 DF32 Unit, Rack Mounted on Slide

1.4.1 Disk File Assembly

The disk file assembly is shown on Figure 1-3. The 16 read/write heads, four timing and address heads, photocell amplifier circuit, and drive motor are attached to the base plate which is suspended on four shock-absorbing mounts. The storage device is a nickel-cobalt plated disk that rotates with the motor shaft. The base plate and mounted components are completely enclosed by removable dust covers on the top and bottom as shown. Two connector cards provide timing, address signals, and data to the read/write heads cable. The physical position of the read/write heads on the base plate is shown on Figure 1-4.

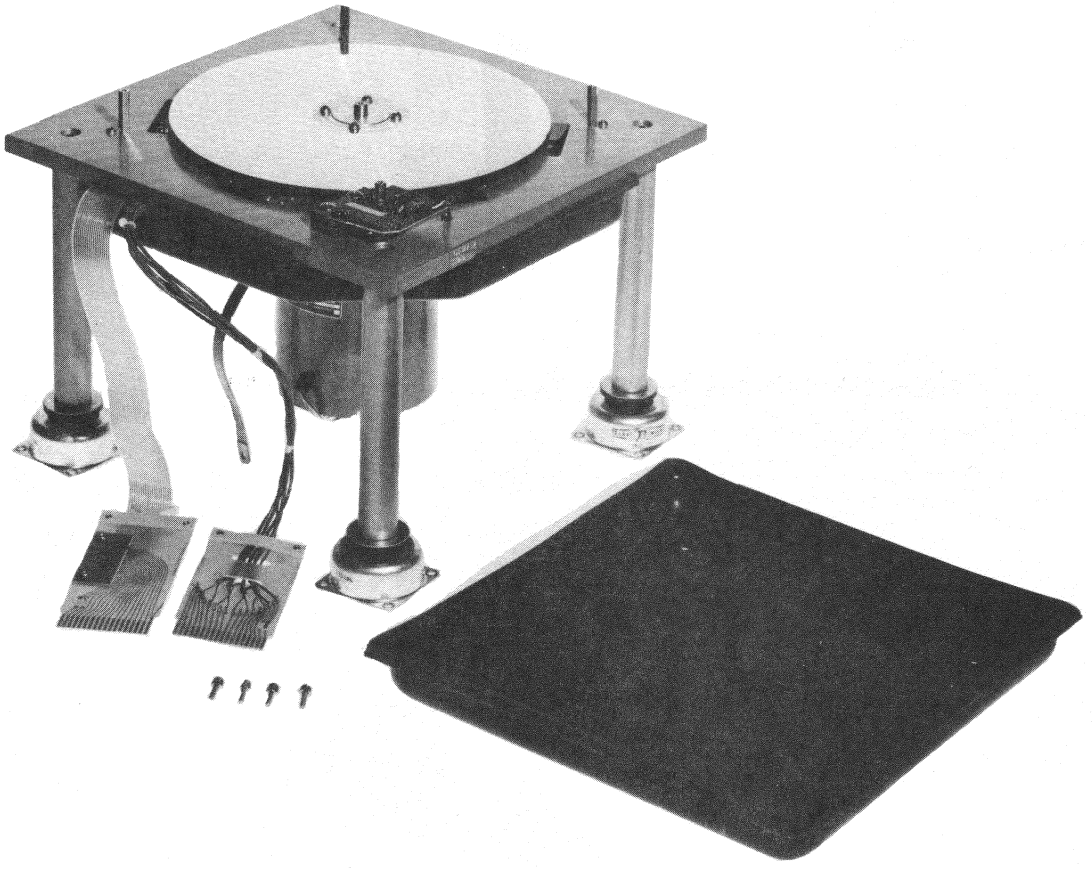
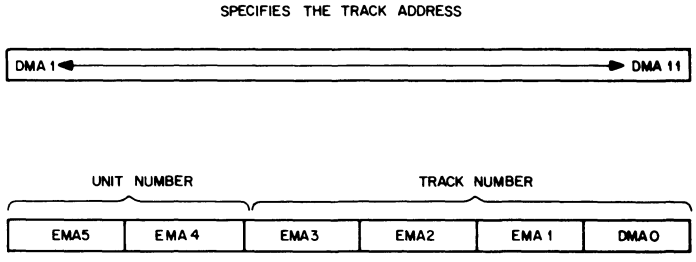


Figure 1-3 Disk File Assembly (Cover Removed)

Figure 1-4 Disk File Assembly, Read/Write Head Locations

CHAPTER 2
OPERATION AND PROGRAMMING

The programming of the DF32 is typical of an I/O device attached to the PDP-8. It uses the IOT instructions to control operation and the 3-cycle data break facility of the PDP-8 to transfer data between core memory and the DF32. The WC register (memory address 7750) of the data break facility specifies the number of word transfers, and the CA register (memory address 7751) of the data break facility specifies the current address of core memory that is to receive or send a word. The DF32 contains a memory buffer (DMB) to buffer the data between core memory and the disk; and a DMA (disk memory address) to specify the track address; the EMA (extended memory address) to specify the track and unit number. The formats of these registers are shown below.



There can be as many as four disk files within a system: one DF32 and up to three DS32 disk extenders. The disk extenders operate under the control of the DF32; therefore, only one disk file can be selected at any one time for data transfers (i.e., the control circuits handle only one block transfer at any one time).

The programming of each disk is functionally identical. Unit number assignment for each disk within the system is accomplished by the setting of a selection switch, provided on the front panel of each disk file unit. The program selects the desired unit by appropriately programming the EMA register. To ensure proper operation, each disk file within a particular system must be assigned its own unique unit number.

The storage capacity of each disk is 32,768 13-bit words, or 16 tracks of 2,048 13-bit words. If the specified data transfer encompasses more than one track, the data transfer operation continues automatically to the next track following one revolution of latency (33 ms). Similarly, operation continues to the next unit when the last track and track address have been accessed, provided that a next unit exists.

2.1 OPERATING CONTROLS

Tables 2-1 and 2-2 show the operating controls for the DF32 and DS32, respectively. Figures 2-1 and 2-2 show the control panels for the DF32 and the DS32, respectively.

2.2 IOT INSTRUCTIONS

Table 2-3 shows the IOT instructions for the DF32 system, and Table 2-4 shows a complete analysis of the IOT instructions.

Table 2-1
DF32 Control Panel Functions

Number	Controls	Function
1	Upper write lockout	Inhibits writing on the upper 16K word position of the DF32.
2	Unit select	Assigns disk address 0, 1, 2, or 3.
3	Lower write lockout	Inhibits writing on the lower 16K word position of the DF32.
4	Disk lockout 0	Enables write lockout selection on unit 0.
5	Disk lockout 1	Enables write lockout selection on unit 1.
6	Disk lockout 2	Enables write lockout selection on unit 2.
7	Disk lockout 3	Enables write lockout selection on unit 3.
8	PDP-8, PDP-8/I or PDP-8/S	Processor selection enables the system, through interface, to be employed with both processors.

Table 2-2
DS32 Control Panel Functions

Number	Controls	Function
1	Upper write lockout	Inhibits writing on the upper 16K word positions on the extension unit.
2	Unit select	Assigns disk address, permitting the extender unit to be operated with the master unit or as an additional extender unit.
3	Lower write lockout	Inhibits writing on the lower 16K word position on the extender unit.

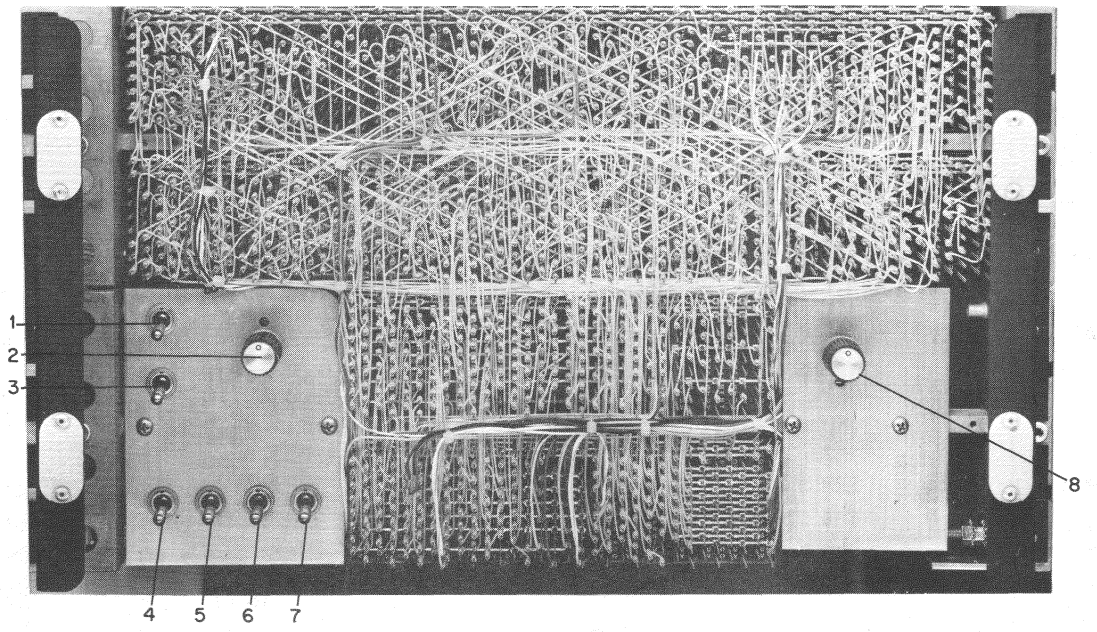


Figure 2-1 DF32 Operating Control Panels

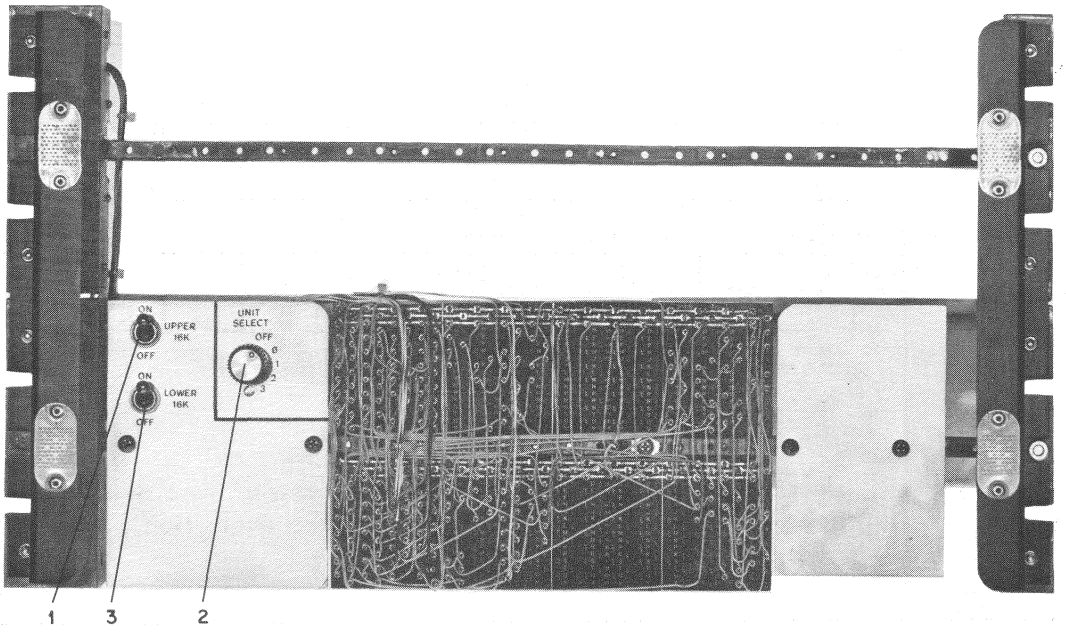
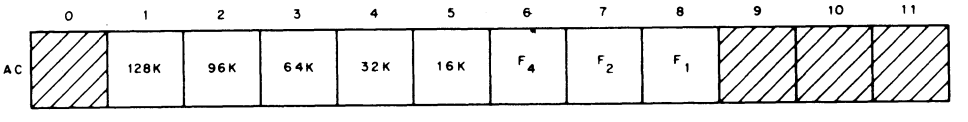


Figure 2-2 DS32 Operating Control Panel

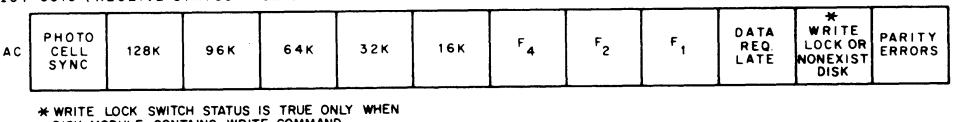
Table 2-3
IOT Instructions

Mnemonic	Octal Code	Operation
DCMA	6601	Clear the disk memory address register, parity error, and completion flags. This instruction clears the disk memory request flag and interrupt flags.
DMAR	6603	Load the disk memory address with information (initial address) in the accumulator. Then clear the AC. Begin to read information from the disk into the specified core location. Clear parity error and completion flags. Clear interrupt flags AC_{0-11} DMA_{0-11}.
DMAW	6605	Load the disk memory address register with information (initial address) in the accumulator (AC); then clear the AC. Begin to write information onto the disk from the specified core location. Clear parity error and completion flags. Clear interrupt flags. AC_{0-11} DMA_{0-11}.
DCEA	6611	Clear the disk extended address and memory address extension register.
DSAC	6612	Skip next instruction if the address confirmed flag is a 1. Flag is set for 16 μs (AC is cleared).
DEAL	6615	Clear the disk extended address and memory address extension register. Then load the disk extended address and memory address extension registers with the track address data held in the accumulator.
DEAC	6616	Clear the accumulator. Then load the contents of the disk extended address register into the accumulator to allow program evaluation. Skip next instruction if address confirmed flag is a 1.

IOT 6615 (TRANSMIT TO DF32)



IOT 6616 (RECEIVE STATUS FROM DF32)



* WRITE LOCK SWITCH STATUS IS TRUE ONLY WHEN DISK MODULE CONTAINS WRITE COMMAND.

Table 2-3 (Cont)
IOT Instructions

Mnemonic	Octal Code	Operation
DFSE	6621	Skip next instruction if the parity error, data request late, or write lock switch flag is a 0 (no error).
DFSC	6622	Skip next instruction if the completion flag is a 1 (data transfer is complete).
DMAC	6626	Clear the accumulator. Then load the contents of the disk memory address register into the accumulator to allow program evaluation. $DMA_{0-11} \longrightarrow AC_{0-11}$ During read the final address will be the last address transferred +1. During write the final address will be the last address transferred.

Table 2-4
IOT Instruction Analysis

IOT INSTRUCTIONS

a. 6601: DCMA

(1) Generates SCL (start clear) which clears:

(a) TRC flip-flop — Transfer Complete
(b) NED flip-flop — Nonexistent Disk
(c) MRS flip-flop — Memory Request Sync
(d) ADC flip-flop — Address Confirmed
(e) ACH flip-flop — Address Compare Hold
(f) DRL flip-flop — Data Request Late
(g) PER flip-flop — Parity Error

(2) Generates DTC (Disk Time Clear) which clears:

(a) MWR flip-flop — Memory Word Request
(b) TCA flip-flop — Time Counter "A"
(c) TCB flip-flop — Time Counter "B"

(3) Clears the disk memory address register

b. 6602:

(1) Clears the accumulator

(2) Clears the R/W (read/write) flip-flop setting transfer direction to read.

(3) Generates LAD (load address) which:

(a) Does ones transfer from the accumulator to the disk memory address register.
(b) Clears WCO flip-flop (word count overflow)
(c) Sets MRS flip-flop

Table 2-4 (Cont)
IOT Instruction Analysis

c. 6604:

(1) Clears the accumulator

(2) Sets the R/W flip-flop, setting transfer direction to write.

(3) Generates LAD (see Section b, Paragraph 3).

(4) Sets DBR flip-flop (data break request).

NOTE

Combinations of the 660X IOT's are

6603	DMAR	(Read)
6605	DMA$\overline{W}$	(Write)

d. 6611: DCEA

(1) Clears disk extended memory address register.

(2) Clears extended address register (for extended memory in computer).

e. 6612: DSAC

(1) Enables skip bus if ADC flip-flop is set (used primarily in diagnostic programming).

(2) Clears the accumulator

f. 6614:

(1) Does ones transfer from accumulator bits 1 through 5 to the disk extended address register.

(2) Does ones transfer from disk "status register" to accumulator bits 0 through 11.

NOTE

Combinations of 661X IOT's are

6615	DEAL	(Clear and Load disk EMA register)
6616	DEAC	(0--AC, load AC with disk EMA)

g. 6621: DFSE

(1) Enables skip bus if no error flags are up (skip on no error)

h. 6622: DFSC

(1) Enables skip bus if the TRC flip-flop is set and computer MB bit 9 is a zero (IOT 6622 used alone).

(2) Enables clear bus if computer MB bit 9 is a one. (IOT 6622 used with IOT 6624.)

Table 2-4 (Cont)
IOT Instructions

i. 6624:

(1) Does a ones transfer from disk memory address register to accumulator bits 0 through 11.

NOTE

Combinations of 662X IOT's are

6626 DMAC (0--AC and load AC with DMAR)

Maintenance IOT Instructions

a. 6631: TAS (TTA simulator)

Generates false TTA pulses for static logic test.

b. 6632: TBS (TTB simulator)

Generates false TTB pulses for static logic test.

c. 6634: DBRS

Sets data break request flip-flop for static logic test.

2.3 INTERRUPT FLAGS

There are two flags that generate an interrupt: the NED (nonexistent disk) and the TRC (transfer complete) flags. The NED flag is set when the program selects (via EMA) a unit which does not exist, or the data transfer operation increments the EMA to next unit and it does not exist. A nonexistent unit means that the program has selected a unit number and no disk file is set to that unit number.

The TRC flag signifies the end of the data transfer. It is set at the completion of the last word transfer by the disk, following a word count overflow of the WC register. The completion flag can be sensed by the DFSC instruction.

2.4 ERROR FLAGS

The error flags can be sensed by the IOT 6621 instruction. The program skips when no error exists. The error flags are described in the following paragraphs.

2.4.1 DRL Flag

The DRL (data request late) flag signifies: 1) that a data transfer operation occurred between the disk DMB and the disk before the previous transfer was handled by the data break facility, 2) that address accepted was not received back from the computer, leaving the break request flag up.

2.4.2 PER Flag

The PER (parity error) signifies that a parity error occurred before the read operation.

2.4.3 WIA Flag

This flag signifies that a write operation was attempted on the lower 16K memory addresses of the DF32 when they were locked out by the write lockout switches.

2.4.4 WIB Flag

Same as WIA except on upper 16K of disk memory.

2.4.5 EWL Flag

Signifies that a WIA or WIB error occurred on a selected disk expander.

When sensed by the DEAC instruction, WIA, WIB, and EWL are contained in the same list.

2.5 ADC FLAG

The ADC (address confirmed) flag is used only in diagnostic programming. It signifies that the DMA corresponds to the track address currently passing under the read/write heads and is available for only 16 μs. It can be sensed by the IOT 6612 instruction which skips if the flag is set.

2.6 STATUS EVALUATION

The status of certain conditions can be evaluated by using the IOT 6614 instruction. The IOT 6614 (DEAC) loads the AC with the status as shown below.

AC0	PSM (photo sync mark) which specifies that the disk gap is presently passing under the read/write head. It is available for 200 μs.
AC1-AC5	Respectively, EM5 through EM1.
AC6-AC8	Respectively, EA3 through EA1.
AC9	DRL flag
AC10	NED or EWL flag
AC11	PER flag

2.7 PROGRAMMING EXAMPLE

A programming example that writes a block of data onto the disk is shown below. For simplicity, the example assumes that all data and instructions are within the same page, but in actual practice this may not be true.

```
        /CALLING SEQUENCE
SUB,    JMS     WRT     /JUMP TO WRITE SUBROUTINE
        Ø               /CONTAINS WORD COUNT
        Ø               /CONTAINS INITIAL CORE MEMORY ADDRESS
        Ø               /CONTAINS TRACK AND UNIT NUMBER
        Ø               /CONTAINS TRACK ADDRESS
        XXX             /CONTINUE WITH MAIN PROGRAM

        /WRITE SUBROUTINE
WRT,    Ø               /ENTER WRITE SUBROUTINE
        TAD I   WRT     /FETCH WORD COUNT
        DCA     WC      /DEPOSIT IN WORD COUNT REGISTER
        ISZ     WRT     /INCREMENT POINTER
        TAD I   WRT     /FETCH INITIAL CORE MEMORY ADDRESS
        DCA     CA      /DEPOSIT INTO CURRENT ADDRESS REGISTER
        ISZ     WRT     /INCREMENT POINTER
        TAD I   WRT     /FETCH TRACK AND UNIT NUMBER
        DEAL            /DEPOSIT INTO REGISTER IN DF32 CONTROL
        CLA             /CLEAR AC
        ISZ     WRT     /INCREMENT POINTER
        TAD I   WRT     /FETCH TRACK ADDRESS
        DMAW            /TRACK ADDRESS TO DMA IN DISC; START
                        /WRITE OPERATION
        DFSC            /JOB DONE?
        JMP .-1         /NO, WAIT
        DFSE            /ANY ERRORS?
        JMP     ERR     /YES, GO TO ERROR SUBROUTINE
        ISZ     WRT     /NO, INCREMENT POINTER TO EXIT ADDRESS
        JMP I   WRT     /EXIT PROGRAM
```

The calling subroutine must be set up so that the subsequent locations to SUB (SUB+1, SUB+2, etc.) contain the parameters as shown in the comments column. The format of location SUB+3 must conform to that shown in Table 2-3 for the DEAC instruction.

The JMS WRT instruction causes a subroutine jump to location WRT with the contents of the PC+1 (which contains symbolic address SUB+1) deposited into location WRT. Since location WRT now contains SUB+1, the first instruction of the subroutine (TAD I WRT) loads the AC with the contents of SUB+1 which is the word count. The word count is then deposited into the WC register. Similarly, the initial address is deposited into the CA register. The program then proceeds to set up the EMA and DMA registers and start the write operation. After the DMAW instruction is issued, the data transfer operation begins and continues independently of the program; it operates under the control of the data break facility to transfer data. When the transfer is complete, the TRC (transfer complete) flag comes up and, when sensed by the DFSC control, passes to the DFSE instruction. DFSE then senses for errors, and if any, control jumps to an error or diagnostic (not shown) routine. If no errors, control exits from the subroutine back to the main program to resume main processing.

It should be noted that since the data transfer operates independently of the program, the subroutine could be exited following the DMAW instruction. An interrupt subroutine could handle the post data transfer processing since the TRC flag generates an interrupt.

An identical program could handle data transfers for a read operation except that the DMAW instruction is replaced by the DMAR instruction.

CHAPTER 3
PRINCIPLES OF OPERATION

This chapter describes the principles of operation of the DF32 Disk File System. Descriptions of the logic circuits in this chapter refer to the logic drawings included in Chapter 6.

A disk file system can consist of one DF32 Disk File and up to three DS32 Disk Extenders. The Disk Extender is a disk file that operates under the control of the DF32. Each of the disk files has a unit select switch whereby a disk can be assigned a unit number by the operator. The disk file executive program then selects the unit for a data transfer operation. If the program selects a disk file that is not selected by the unit select switch, no data transfer occurs, and the program is notified of this NED (nonexistent disk) condition by an interrupt.

The DF32 system uses the three-cycle data break facility of the PDP-8 to transfer data. The WC (word count) and CA (current address) registers are used to specify the number located in the memory core of the computer and the core memory address, respectively, of the data transfer. Initially, the program loads the WC register with the 2's complement of the number of word transfers and the CA register with the initial core memory address -1. Thereafter, the CA and WC are incremented after each data transfer.

After the program sets up the WC and CA registers, it issues a DEAL instruction to load the EMA (extended memory address) which specifies the track number and the unit number (Dwg No. D-BD-DF32-0-9). If a write operation is specified, the DMAW instruction is issued to load the DMA (disk memory address) register to specify the track word address that is to receive the word transfer. The DMAW also initiates a data break request so that the first word to be recorded is loaded into the DMB (disk memory buffer). The write operation then transfers the content of the DMB to the addressed track. After each transfer, the DMA is incremented to address the next track address. Operation continues until the WC register is reduced to zero. When this occurs, a WCO (word count overflow) signal is sent to DF32 control to terminate operation.

3.1 DISK FORMAT

The disk format is shown in Dwg. No. D-TD-DF32-0-11. There are 16 data tracks on which data may be recorded or read. Each track can record 2048 13-bit words (12 data bits plus a parity bit). To synchronize recording or reading, the disk contains two TTA (including one spare) and TTB (including one spare) timing tracks. The TTB track contains the track address information and during operation the TTB pulses provide the control circuits with the track address presently passing under the track head. It requires one track address period (time for the TTB serial pulses to define a track address) for the control circuits to determine the present track address. For example, if the track address is 0000, by the

time address 0000 is recognized, 1000 is passing under the track head. Therefore, data is always written (or read) on the track address following the one specified. To provide an optimum transfer rate, the track addresses are not sequential. Instead, they are 0000, 1000, 2000, 3000, 0001, 1001, etc., as shown in the format diagram.

3.2 NRZI RECORDING

The technique of recording on the magnetic disk surface is called NRZI (non-return to zero inhibit) recording. In this method, a reversal of the direction of magnetic flux represents a 1 bit and a lack of change represents a 0 bit. Writing is achieved by using a flip-flop to control the direction of magnetizing current on the track. The flip-flop is called the write flip-flop (WFF). By applying the 1's output of the DMB to the complement input of the WFF, the WFF is complemented as each 1 bit is shifted out of the DMB (Figure 3-1). The WFF causes the writer to reverse the flux direction on the disk surface each time the WFF is complemented. After all 12 bits are recorded on the disk surface, the writer records the 13th bit which is the parity bit. Since parity is even, resetting the WFF writes the parity bit. For example, if an odd number of 1's were recorded for the 12 bit word, then the WFF is in the set state; therefore, resetting the WFF reverses the flux on the disk to record a 1 parity bit. If the recorded character contains an even number of 1's, then resetting the WFF does not change its state. Therefore, a 0 parity bit is written.

When data is read from the track, the read head senses the flux changes of the disk to produce bipolar pulses. The pulses are rectified and shaped to produce data pulses. A pulse is defined as a 1 bit and no pulse is a 0 bit.

3.3 GENERAL OPERATION OF SEARCH, READ, AND WRITE

Before explaining the detailed logic of the disk, this paragraph will describe the general operation of read and write (Figure 3-2). To write on the disk file, the DMA (disk memory address) register is loaded with the track address, and the EMA (extended memory address) register is loaded with the track and unit number. This is accomplished by the DEAL and the DMAW instructions. The DMAW instruction, which specifies the write mode, also initiates operation, enables the writer for the write mode, and generates a break request so that the first data word to be written is loaded into the DMB (disk memory buffer).

A search process then begins, whereby the track addresses are examined to determine when the track address passing under the write head is the correct word. This is accomplished by decoding the track-address pulses which come from the disk in serial fashion. The decoded track address bits are applied to a serial comparator. At the same time, the DMA is shifted end-around (recirculated). The DMA bits are also applied to the serial comparator so that the track address is compared to the address

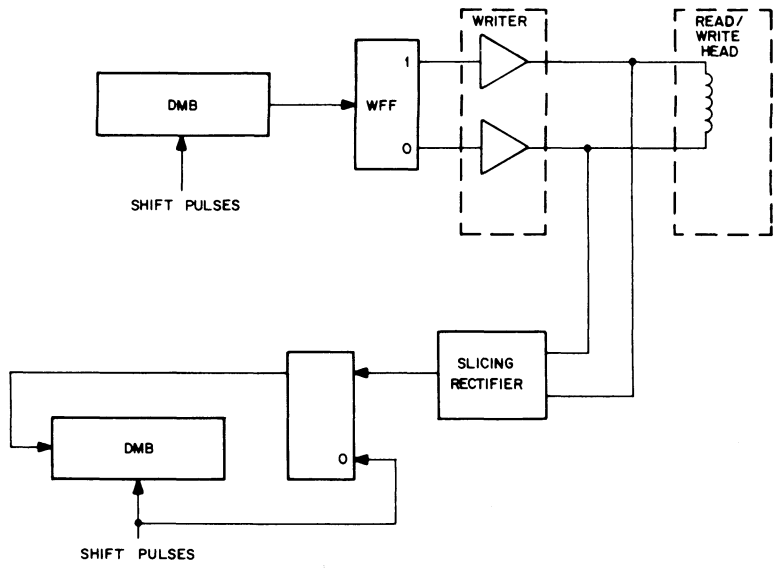


Figure 3-1 Simplified Diagram of NRZI Recording

in the DMA. When the two addresses compare identically for the 11 bits shifted through the comparator, a signal is generated to enable the write operation. The DMB is shifted, and as the bits are shifted out of the DMB, they are applied to the write flip-flop (WFF). For each 1 bit shifted, the WFF is complemented, and for each 0 bit shifted, the WFF flip-flop remains in the same state. The output of the WFF flip-flop is applied to the writer to write the indicated bits in NRZI format.

After the word is written, the DMA must be incremented to address the next word, and a break request generated to fetch the next word from memory. Incrementing the DMA is accomplished on the next recirculation of the DMA. As the DMA is shifted end-around, it passes through a serial adder circuit so that it can be incremented. If, at this time, the DMA increments from 3777 to 0000 (meaning a change to the next track), a carry pulse is propagated. This pulse increments the EMA register so that the next track (and, if indicated, the next unit) will be addressed. Writing therefore commences on the next sequential track at address 0000, following one revolution of the disk.

The read operation is similar to the write operation in that the DMA and EMA are loaded to specify the track address, track number, and unit number. The search operation is initiated to find the addressed track word. When the addressed track word is found, the track data is read serially into the data buffer, and a break request is generated so that the data in the data buffer can be transferred to the computer memory. The operation thereafter is similar to the write mode except for the data transfer direction.

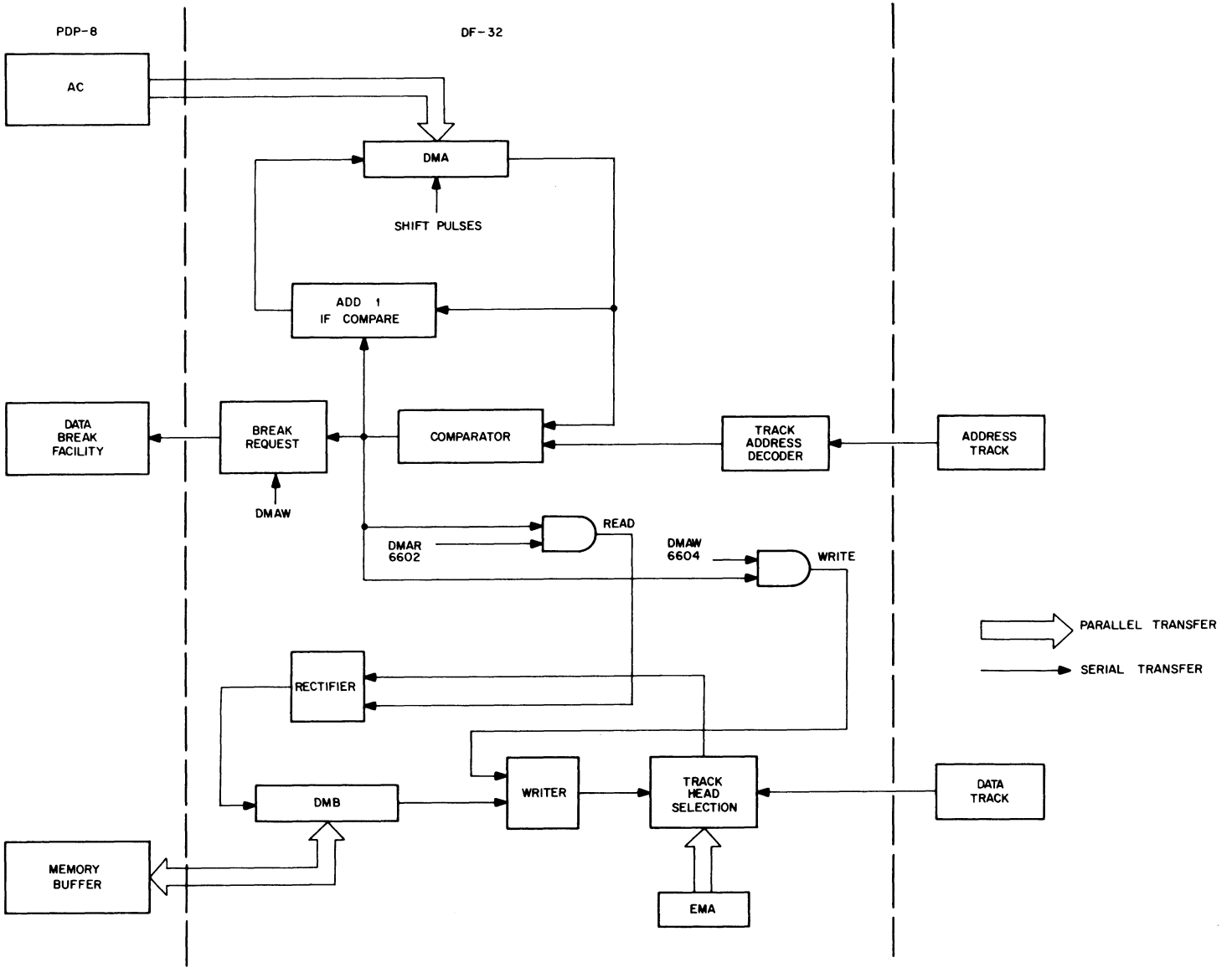


Figure 3-2 Simplified Diagram of Read and Write

3.4 TIMING PULSES

There are two timing tracks on the disk that provide timing pulses to control operation of the disk. They are the TTA and TTB analog signals which are 90° apart (refer to Dwg. No. D-TD-DF32-0-10 and Dwg. No. D-BS-DF32-0-1). The TTB signals contain the track address information. Both the TTA and TTB analog signals are applied to a SLICE RECTIFIER which provides rectified and clipped signals (TAS for TTA and TBS for TTB). The clipped signals are provided when the analog signal crosses the 50% slice level threshold. The pulse width of the TAS and TBS are reduced by PA to 400 ns and 100 ns, respectively.

The TTB pulses define the current track address; therefore, the occurrence of TTB pulses fluctuates with the current track address. Note that there are 13 TTA pulses separated by an interval of no TTA pulse. There are always three TTB pulses that are used for control functions for every track address period. The TTA and TTB pulses are combined to produce a TP1 pulse* every track word address period. The TP1 pulse defines the beginning of a word address period. The TP1 pulse is produced by a TTB pulse when the ABD (address-bit decoder) flip-flop is set. The ABD flip-flop serves a dual purpose; it decodes the address bits during a track address search operation, and it is used in the production of TP1. The TTB pulse sets the ABD flip-flop and TTA resets it. Note on the timing diagram that the first two of the three TTB pulses that always occur do so during the period of no TTA pulse. Therefore, the first TTB pulse sets ABD and since ABD remains set when the second TTB pulse occurs, the second TTB pulse produces a TP1 pulse. The TTA, TTB, and TP1 pulses are used to control the operation of the disk file as explained in subsequent paragraphs.

3.5 DETAILED LOGIC DISCUSSION

This section provides a complete logic discussion of the operation of the disk file. As a supplement to this discussion, the reader is referred to Table 2-4 which provides an analysis of each IOT instruction, and Table 3-1 which provides a mnemonic list.

Table 3-1
Mnemonic Codes for DF32 Disk System

Mnemonic	Name and Description
ABC	Address Bit Compare: This flip-flop is set when BCE is positive (comparison untrue or not matched).
ABD	Address Bit Detector: This flip-flop is set when a one is read from the address track (TTB).
ACE	Address Confirmed Enable: If this level is positive at TP1 time, it indicates address found.

* This is a signal used in the peripheral control logic and should not be confused with "TP1" in the PDP-8/I processor logic.

Table 3-1 (Cont)
Mnemonic Codes for DF32 Disk System

Mnemonic	Name and Description
ACH	Address Compare Hold: Cleared, it enables an end around shift in DMA register. Set, it enables address increment while shifting.
ADC	Address Confirmed: Set to indicate address search completed.
BCE	Bit Compare Enable: Positive when ABD and MA11 do not compare.
CMB	Clear Memory Buffer
DBR	Data Break Request: Signals computer when disk is ready to transfer data.
DEP	Data End Pulse: After word time in which data was transferred between DMB and disk; in or out. Also on disk overflow.
DMA	Disk Memory Address: Disk memory address register.
DMB	Disk Memory Buffer: Disk memory buffer register.
DOP	Data Ones Pulse: Each pulse indicates a one read from the disk data tracks.
DRL	Data Request Late: This error flag indicates a timing problem between disk and computer.
DRS	Data Request Synchronizer: Effectively inhibits SAD while data is being transferred (DMB-DISK).
DSL	Data Sense Lines: Connection between reader G083, writer G284, and heads on disk deck.
DSP	Data Strobe Pulse: Qualifies slicing rectifier at peak of data signal from readers.
DTC	Disk Timer Clear: Generated by SCL or when switching disks. Clears TCA, TCB and MWR.
EA	Extended Address: Computer data field.
EMA	Extended Memory Address: Disk extended memory address register (track and disk selectors).
GRD	Ground for write current.
LAD	Load Address: Loads DMA from BAC.
LMB	Load Memory Buffer: Loads DMB from BMB.
MAD	Memory Address Deposit: Special case, used only when DMA register overflows from 3777 to 0000.
MBC	Memory Buffer Clear: Decoder output goes positive indicating when to write parity.
MBE	Memory Buffer Enable: Qualifies WFF when a 1 is to be written on disk.
MBI	Memory Buffer In: Data from disk to DMB comes in through this flip-flop.

Table 3-1 (Cont)
Mnemonic Codes for DF32 Disk System

Mnemonic	Name and Description
MRS	Memory Request Sync: Controls input to TCA
MWR	Memory Word Request: Set during all disk read or write operations (set by TCB overflow).
NED	Nonexistent Disk: Indicates disk overflow, raises interrupt, and sets TRC flip-flop.
NEX	Nonexistent: This level positive indicates unit selection does not exist. (No unit).
PAR	Parity: This flip-flop reads parity from disk.
PCL	Power Clear: From PDP-8 computer. (Initialize in PDP-8/I)
PCA	Photo Cell Amplifier: Located on disk-deck. Amplifies and sets width of photo sync mark.
PER	Parity Error: This flip-flop is set when an odd number of bits is read in one word.
PSM	Photo Sync Mark: Output of PCA used to synchronize disk operation.
RDE	Read Enable: Stabilizes timing logic.
R/W	Read/Write: Transfer direction = write when set; read when cleared.
SAD	Search Address: This flip-flop is set each word time by the second TTA pulse (except when ADC = 1).
SAP	Shift Address Pulse: These pulses are generated by the second through thirteenth TTA pulses (except when ADC = 1).
SCL	Start Clear: Is generated by PCL or IOT 6601.
SDP	Shift Data Pulse: Generated by TTA during both read and write when ADC = 1 (Burst of 13).
SEL	Select: True when unit select and $\overline{PSM}$ are true.
SHE	Shift Enable: Is time when ADC = 1 and R/W is = 0 (read).
SLT	Select: True when unit select is true.
TCA TCB	Time Counter "A": Time Counter "B": } Used together to allow a four word time delay when switching from control unit to expander.
TRC	Transfer Complete: This flip-flop is set when WCO is true; or when NED is set and WCO = 0.
TTA	Timing Track "A": A burst of 13 pulses and a one pulse time space recorded on the disk (timing).
TTB	Timing Track "B": Address information recorded on the disk (11 bits absolute address, 3 bits to generate TP1 and set DRS).
WCE	Word Count Enable: Effectively combines MWR=1 and DRS=1 to qualify gating on SAD flip-flop.

Table 3-1 (Cont)
Mnemonic Codes for DF32 Disk System

Mnemonic	Name and Description
WCO	Word Count Overflow
WCP	Word Count Pulse: Writes parity if WFF = 1 after 12-bit data word has been written.
WFF	Write Flip-Flop: Is complimented by SDP if MBE is true (to write a one in NRZ method).
WIA	Write Inhibit "A": Write lockout tracks 0 through 7.
WIB	Write Inhibit "B": Write lockout tracks 10 through 17.
WTE	Write Enable: True when ADC = 1 and R/W = 1 (write) (starts current flowing in head).

3.5.1 Address Searching

The read or write operation is initiated upon the occurrence of the DEAL and the DMAW for writing, or DMAR for reading. The DEAL IOT instruction is decoded by the device selector (Dwg No. DF32-0-1) to produce the IOT 611 and 614 pulses. The IOT 611 (ECL) pulse clears the EMA and EA registers (Dwg. No. DF32-0-3), and the IOT 614 pulse loads these registers from the PDP-8 AC. The EMA_4 and EMA_5 bits are decoded to provide the unit number selected by the program. If the UNIT SELECT SWITCH for the DF32 disk file is set to this number, signal SLT becomes 1. (Similarly, if any one of the DS32 disk expander selection switches are set to this number, it is energized.) Signal SEL then becomes 1 (except during the 200-μs gap period) to enable the disk timing cirucits.

Assuming that there is a read operation, the DMAR instruction is issued to start the operation. DMAR generates IOT 601 (SCL) and IOT 602 which perform the functions outlined in Table 2-4. As shown, DMAR loads the DMA with the disk track address and sets the MRS (memory request sync) flip-flop to initiate the search operation.

Four TP1 timing pulses are necessary before the transition of flip-flop TCB (as it is set) sets the MWR (memory request) flip-flop. (A complete timing diagram is shown in Dwg. No. D-TD-DF32-0-10 in Chapter 6.)

With MWR set, the immediate sequence of events are as follows.

a. TTB sets DRS (data request sync).

b. The transition of DRS sets WCE (word count enable).

c. WCE enables the next TTA pulse to set SAD (search address).

With SAD set, the circuits are ready to start shifting the DMA so that the address in the DMA can be compared to the disk track address. SAD enables the TTA pulses to generate the shift address pulses (SAP) that shift the DMA (Dwg. No. DF32-0-2). Note that there are 11 TTA pulses that produce 11 SAP

pulses so that the 11 track address bits of the DMA can recirculate. Between each SAP interval the TTB pulses (which specify the track address) may or may not occur; i.e., for each bit position where the track address specifies a 1 there is a TTB pulse; for each track address bit position that is 0, there is no TTB pulse. The occurrence of a TTB pulse sets the ABD (address bit detector) flip-flop and TTA resets the flip-flop. Therefore, the ABD signal (if a 1 is specified) is present during the interval of a TTA pulse. As the low-order bits from the DMA are shifted out of DMA11 they are compared to the ABD signal; the exclusive-OR circuit (output BCE) performs this comparison. If during the interval of recirculating the DMA through the comparator there is 1 bit that does not compare to ABD, signal BCE goes to ground potential for that comparison and allows the SAP pulse to set the ABC flip-flop. Thus, if ABC (address bit compare) is set after the 11 shifts of the DMA, the DMA address does not compare to the track address. In this case, the circuits again will set up as previously described to repeat the comparison; i.e., TTB sets DRS, and so forth.

When the DMA and disk track address compare identically for the 11 shifts, the ABC flip-flop will remain reset since there were no non-bit comparisons to allow a SAP to set ABC. Therefore, at the end of this interval, the TP1 pulse sets ADC (address confirmed). Signal ADC then enables the read or write operation as described in ensuing paragraphs. The data transfer either to or from the disk occurs on the next TP1 interval. During this interval, signal ADC prevents the DRS flip-flop from being set so that address comparison does not occur at the same time as the data transfer (refer to Figure 3-3).

After the comparison of the DMA to the track address and the data transfer, the DMA must be incremented to address the next sequential track address. To accomplish this, a 1 is added to the DMA by a serial adder on its next recirculation. The addition is described as follows. With ADC set, the next TP1 pulse generates the DEP (data end) pulse which sets ACH (address compare hold) assuming that there is no word count overflow. Note that the DEP pulse also sets the DBR (data break) flip-flop to initiate a data break cycle. The same TP1 pulse that generates DEP also resets ADC. With ADC reset, the next TTB pulse can set DRS to initiate the search address operation. With ACH set, the first bit shifted out of DMA11 is incremented by 1: ACH(1) and DMA11(1) are ANDed so that if DMA11(1) is 1, a 0 is shifted into DMA1 (since 1 + 1 = 0 with a 1 to carry). The carry is implemented by maintaining ACH in the 1 state until DMA11 shifts out a 0; at this time the SAP resets ACH and allows normal search address operation thereafter.

A special case arises when the DMA increments from 3777 to 0000. Throughout this shift interval the ACH remains set to propagate the carry and it remains set after this interval. On the next shift interval the 0000 is shifted and ACH being set would specify a 1 to be added to the low order. To prevent this, the MAD flip-flop (which is set by resetting of SAD when ACH was 1) inhibits a 1 from being shifted into DMA1 on the first shift. Since a 0 is shifted out of DMA11 on the first shift, ACH is reset to permit normal operation thereafter.

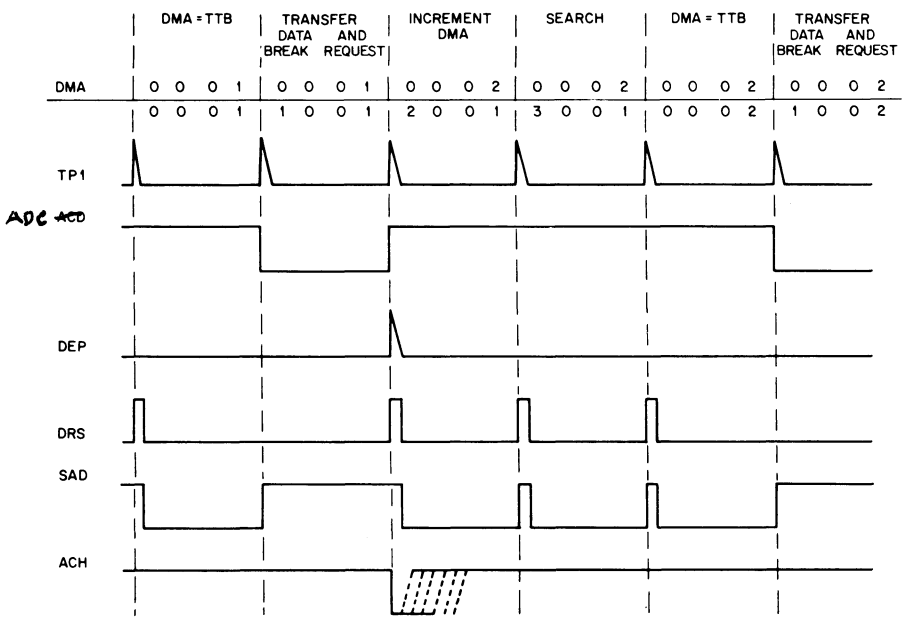


Figure 3-3 Timing Diagram

3.5.2 Read

The DMAR instruction initiates address searching as previously described; it also clears the R/W (read/write) flip-flop to specify a read operation and clears the WCO (word-count overflow) flip-flop.

When the DMA and track address compare, the ADC flip-flop is set and signal SHE goes to 0V and enables the DSP (delayed TTA pulse) pulses to generate SDP (shift data pulses) pulses (Dwg. No. DF32-0-4). The DSP pulses shift the DMB as data is read from the disk track. According to NRZI recording methods, a 1 read from the track is represented by a pulse which is the result of a phase reversal on the magnetic surface, a 0 is the result of no phase reversal and therefore no pulse is generated. The output from the read head that senses the magnetic information on the disk track is sensed by the slice rectifier. The slice rectifier transforms the bipolar signal read from the track into a pulse output. The output of the slice rectifier is enabled by SEL and SHE to produce DOP (data ONEs pulses). The DOP pulse sets the MBI flip-flop. If a 1 is read from the track, MBI is set and the SDP pulse shifts a 1 into DMB_0. If a 0 is read from the track, MBI remains reset and a 0 is shifted into DMB_0. Thus, the 13 DSP pulses shift the words read from the disk track into the DMB. The thirteenth SDP shifts the last bit of data from MBI into DMB_0 and parity ends up in MBI.

After the complete word has been read, parity is checked (parity is checked only in the read mode). As the data bits are read from the track, each DOP pulse complements the PAR (parity) flip-flop. Since parity is even, the PAR flip-flop should be in the reset state after a complete word is read; if not, the DEP pulse sets the PER (parity error) flip-flop to signify a parity error.

The read operation continues in this manner until all words specified by the WC (word count) register have been written. When this occurs, the WCO (word count overflow) flip-flop is set and inhibits the DEP pulse from setting the DBR flip-flop. Thus no further data break occurs. The DEP pulse is enabled WCO(1) to set the TRC (transfer complete) flip-flop. The TRC signal then generates an interrupt to notify the program that the data transfer is complete.

3.5.3 Write

The DMAW instructions initiate the write mode by starting the address search operation as previously described; it also sets the R/W flip-flop to signify the write mode to the data break facility in the PDP-8 computer. The DMAW instruction also sets the DBR flip-flop to generate a break request to load the DMB with the first word to be written. The PDP-8 data break facility responds by generating (B)BREAK which is enabled by R/W to load the DMB. The address accepted pulse resets DBR.

When an address comparison is found, signal ADC(1) enabled by R/W(1) causes signal WTE to go to 0V, and TTA generates SDP pulses. Signal WTE is applied to the writer to enable writing on the selected disk track. The SDP pulses shift the DMB register. As the DMB11 bit is shifted out of the DMB register, it is applied to the WFF (write flip-flop). If DMA11 is a 1, and the level MBC (complemented) is present, the SDP pulse complements WFF which in turn causes the write head to reverse the flux direction on the magnetic surface on the disk. If DMB11 is a 0, the WFF does not change and no flux reversal occurs. Thus 12 bits are written on the selected disk track. After the 12 data bits are written, the parity bit must be written. This is accomplished as follows.

The LMB (load memory buffer) pulse that loads the DMB also generates the DOP pulse which sets the MBI flip-flop. Therefore, on the first shift of the DMB (when the first bit is recorded on the disk), a 1 is shifted into DMB0. Zeroes are shifted thereafter into the DMB as the data bits are recorded. After 12 shifts, the 1 that was inserted into DMB0 by MBI is now in DMB11 with the rest of the DMB (DMB through DMB10) containing 0s. The DMB0 through DMB10 condition is sensed for all 0s, and when 0, the signal MBC becomes true. This inhibits the DMB11 pulse from complementing WFF. Signal MBC enables the last shift pulse to reset WFF which writes the even parity bit.

The write operation continues in this manner until all words specified by the WC register have been written. When this occurs, the WCO (word count overflow) flip-flop is set and inhibits the DEP pulse from setting the DBR flip-flop. Thus no further data break cycles occur. The DEP pulse is enabled by WCO(1) to set the TRC flip-flop which generates a skip condition or interrupt to notify the program that the write operation is completed.

3.5.4 Track Head Selection

For both the read and write operations, the track head selection is accomplished by bits EMA3, EMA2, EMA1, and DMA0. The DMA0, EMA1, and EMA2 bits are applied to an octal decoder as shown in Dwg. No. DF32-0-5. Each octal decoder output is applied to a pair of heads. Bit EMA3 and its complement are also applied to the heads to complete the selection. For example, if the track selection bits contain 0000, then the low-order bits (EMA2, EMA1, and DMA0) are decoded to select heads 0 and 10; however, since EMA3 is 0, only head 0 is selected for the data transfer.

For the write mode, the write lock switches permit either the upper 16K addresses or the lower 16K addresses to be protected from being written upon. The WRITE LOCK SELECTOR switch permits any or all disk files to be selected for write lock protection. The EM0-EM3 signals (when selected by WRITE LOCK SELECTOR) are OR gated and ANDed with the R/W(1) signal to generate signal WLO (write lockout). WLO is then applied to the WRITE LOCK switches ANDed with EMA3 to provide the write lock protection on either the upper or lower 16K of the selected disk file.

3.5.5 Continuous Data Transfers

When the data transfer address for a particular track reaches 3777, then the next data transfer will occur at address 0000 of the next sequential track. This is accomplished as follows. When the DMA reaches 3777, the recirculation of the DMA through the serial adder causes 0000 to be shifted into the DMA. During this recirculation interval, the ACH flip-flop is set and remains set after this interval and, as SAD is reset, its transition SAD(0) provides a pulse to DMA0. This pulse is enabled by ACH(1) to increment the DMA0 and EMA register so that the next sequential track is addressed. Similarly, when all tracks have been accessed for a particular disk file, the overflow of EMA3 will increment EMA4 (and possibly EMA5) so that the next sequential disk file will be addressed.

3.5.6 Disk Expander Operation

The EMA4 and EMA5 bits select one of four disk files for data transfers - either the DF32 or one of three DS32 Disk Expanders. The EMA4 and EMA5 bits are decoded as shown on Dwg. No. DF32-0-3 to produce EM0, EM1, EM2, and EM3. These bits (EM0-EM4) are applied to each of the disk files in the system. If the UNIT SELECT switch is set to the same decoded selection (i.e., EM0-EM4), then that unit is selected for data transfer. For example, if EM1 is selected by the program and a disk file (refer to Dwg. No. DS32-0-1) UNIT SELECT switch is set to EM1, then that disk file is selected for operation. The TTA and TTB pulses from that unit are sent to DF32 control (Dwg. No. DF32-0-1) to control operation. Data transfer operations are then similar to that previously described. The DSP (data shift pulse) is sent to DF32 control to shift the DMB. In a read operation, the DMP1 pulses from the disk

expander are coupled back to DF32 control (via D15-K) to produce the DOP pulses that provide the read data for the DMB. In the write mode, the WFF output from the DF32 control is coupled to the disk expander writer to provide the same function as previously described.

When the EMA register overflows to address the next unit or disk expander, ACH(1) enables EMA3(0) to reset MWR (Dwg. No. DF32-0-1). ACH(1) also enables EMA3(0) to set MRS so that the control circuits have time to synchronize to a different set of TTA and TTB pulses.

3.5.7 Errors

There are three errors that may be sensed by the IOT 6621 instruction. They are parity error, data request late (DRL), or write lock switch flag. The parity error may occur during the read operation as previously described. The DRL error is the result of a data break request, whereby no word transfer occurred before the next DEP (data end pulse). This means that a data transfer occurred between DMB and the disk track before the previous transfer was handled by the data break facility or ADDRESS ACCEPTED pulse was never received from computer. In this case, the DRL flip-flop (Dwg. No. DF32-0-3) is set to signify the error. The write lock switch flags are WIA, WIB, and EWL. WIA signifies that a write is attempted on the lower 16K of the DF32 when the lower 16K address is locked out by the write lock selection switches. Similarly, WIB signifies the same for the lower 16K. The EWL flag is the combination of the WIA and WIB flags from all disk expanders.

3.5.8 Timing Track Writer

The time track writer writes both the timing track and address track on the disk of the DF32 system. The recording is accomplished in NRZI format. That is, a recorded 1 changes the direction of magnetization and a 0 is the absence of the magnetization change. Table 3-2 provides a mnemonic list of the signals on the block schematics of the timing track writer.

Operation of the timing track writer starts when the PCA (photo cell amplifier) output goes negative to signify the end of photo sync pulse (Dwg. No. D-BS-TW32-0-1). This provides a PSB (photo sync beginning) and a PSE (photo sync end) pulse. The PSE pulse clears the track counter TC0-TC4. The PSB pulse triggers the WED (write enable delay) multivibrator which is adjusted to provide the guard band for photo sync mark. PSB also triggers the CED (clock enable delay) one-shot multivibrator (Dwg. No. D-BS-TW32-0-1 (Sheet 2)).

After WEB times out, it sets the WEB (write enable) flip-flop if the WRITE 2 switch is depressed. The WEB signal then enables the G284 writers to write the specified data on the timing and address tracks. WEB(1) also enables the CED signal (Dwg. No. D-BS-TW32-0-1 (Sheet 2)) to set the TCE (time clock enable) flip-flop which enables the R401 clock module to produce clock pulses (TCP).

Table 3-2
Mnemonic Codes for DF32 DECdisk Timing Track Writer

Mnemonic	Name and Description
ACH	Address Compare Hold: when clear allows end around shift in MA register. When set allows increment of address.
AMA	Add Memory Address: this level being negative allows 1s to be written in the 11-bit absolute address, and 1s to be shifted into MA1.
CED	Clock Enable Delay: adjusted to establish guard band for photo sync mark.
CTC	Clear Time Counter: comes once per word to zero time count register and WAD flip-flop.
FBE	First Bit Enable: positive to enable first TTB bit to be written.
PCA	Photo Cell Amplifier: negative level except at photo sync time.
PSB	Photo Sync Begin: pulse in response to leading edge of photo sync mark.
PSE	Photo Sync End: pulse in response to trailing edge of photo sync mark.
SAP	Shift Address Pulse: a burst of 11 pulses used to shift MA register.
SBE	Second Bit Enable: positive to enable second TTB bit to be written.
TCE	Time Clock Enable: set to enable clock.
TCP	Time Count Pulse: clock output.
TEP	Time Enable Pulse: initializes the timing track writer.
WAD	Write Address: This flip-flop is set during the time that the 11-bit absolute address is written.
WAE	Write Address Enable: this level is positive to allow WAD to be set.
WAP	Write Address Pulse: 14 per word to complement WFB.
WEB	Write Enable: qualifies writers when true.
WED	Write Enable Delay: adjusted to establish guard band for photo sync mark.
WEE	Word End Enable: positive during last TTA and TTB bit times.
WEP	Word End Pulse: comes once per word at the end of the word.
WFA	Write Flip-Flop "A": is complemented to write TTA bits on disk (timing).
WFB	Write Flip-Flop "B": is complemented to write TTB bits on disk (address).

The TCP pulses now start to toggle the TC0-TC4 counter. This counter is used to establish time relations between the TTA and TTB pulses that are to be recorded. Since there is a pulse difference between the TTA and TTB pulses, alternate counts of the TC0-TC4 counter establish the basic TTA and TTB pulse rates.

Since operation is starting, the TC0-TC4 counter will be all zero. With TC0-TC3 all zero, signal FBE (first bit enable) is 0V and enables the WAP (write address pulse) to complement WFB and write the first TTB pulse. Note that the WAP is generated during TC4(1) time. After the second TCP pulse, signal FBE goes negative and permits the succeeding TCP pulse, when TC4(0) is true, to complement the WFA flip-flop and write the TTA pulses.

Next, signal SBE becomes 0V and enables the next WAP pulse to complement WFB which writes the second TTB pulse onto the address track.

The fourth TCP pulse steps the TC counter so that signal WAE goes to 0V and enables the next TCP pulse to set the WAD (write address) flip-flop. With WAD set, the address data is written on to the address track. Signal WAD(1) is ANDed with AMA to permit the WAP pulse to complement WFB. If AMA is 1, the WFB flip-flop is complemented by WAP to write the appropriate address bit. If AMA is 0, the flip-flop remains in its present state for that pulse period to write a 0 for that address bit.

Operation continues in this manner, with TCP pulses writing a TTA pulse when TC4 (0) is true, and the WAP pulse writing the specified address until the 13 TTA pulses and the address data have been written for this period. Operator terminates for the address period when the WEE circuit senses a 1101 count in TC0-TC3. Signal WEE goes to 0V at this count and enables the WAP pulse to reset the TC0-TC4 counter to 0 to establish initial conditions for writing the next TTA and TTB sequence.

The address data that is written into the address track is derived from the MA register drawing (Sheet 2). Following the photo sync mark, the MA register is clear and writes all 0s for the first address sequence. The MA register is shifted during the time the address data is written into the address track by SAP. SAP is derived from ANDing TCP, WAD(1) and TC4(0). If a 1 is shifted out of MA11, signal AMA goes to 0V and allows WFB to be complemented to write the 1. If a 0 is shifted out of MA11, signal AMA inhibits WFB from being complemented and a 0 is written.

Since the disk address written on the disk is 0000, 1000, 2000, 3000, 0001, etc., the MA register is incremented in the following manner. At the end of each address period, the WEP pulse strobes MA2 and MA1 which are connected as a 2-stage binary counter, hence, the 0000, 1000, 2000, 3000. When the count reaches 3000 a 1 must be added to the low order bits. This is accomplished as follows:

With MA(1) and MA(2) both true, the WEP pulse sets ACH. On the next recirculation of MA register, the ACH and MA11 signals enable the exclusive-OR circuit that produces AMA to implement the addition of a 1 to the low-order bits in the same manner as described previously for the DMA register of the disk file.

When a 3777 address has been written, the TCE flip-flop is reset to terminate the operation. An operating procedure for the timing track writer appears in Chapter 5.

3.6 SPECIAL CIRCUITS

The special-circuit modules used in the DF32 system have not been incorporated in the DEC Logic Handbook. Therefore, brief discussions of the pertinent special circuit modules are provided in the following paragraphs. The schematics for the special circuit modules are shown in Chapter 6 with the engineering drawings.

3.6.1 G083 Differential Preamplifier

The G083 contains two ac-coupled differential preamplifiers as shown in Figure 3-4. The G083 provides the gain (adjustable from 1 to 10) and common-mode noise rejection required to preamplify the signals generated by the disk read/write heads during the read-from-disk mode.

During the write cycle, a diode protection network prevents the amplifier from saturation. The amplifier has a bandwidth of 200 kHz to 1 MHz, with a maximum recovery time of 15 μs.

The outputs of the dual preamplifiers are connected directly to the differential inputs of the W532 Difference Amplifiers. Since the W532 Mod B preamplifier has an operating frequency of 600 kHz, amplifiers W532 Mod A and B are not interchangeable. A bandpass-limiting capacitor of 180 pF (C2) is provided on the G083 Amplifier output when the DF32 contains a W532 Mod A Amplifier. This capacitor is removed when the DF32 contains the W532 Mod B Amplifier.

The power requirements for the G083 are shown below.

Pin	Normal Voltage	Marginal Check Limits		Current (mA)
		Min.	Max.	
A	+10	+6	+14	25
B	-15	-10	-20	30
V	+ 8.5	-6	-14	--

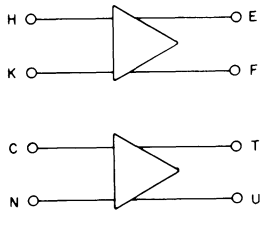


Figure 3-4 Block Diagram, G083 Differential Preamplifier Module

3.6.2 G284 Disk Writer

The G284 Disk Writer is used to control the direction of the magnetizing current in order to write data in the NRZI format. In conjunction with the G285 and G286 selection modules, the G284 controls the magnetizing current on the selected disk track. The G284 contains two separate circuits that share a common emitter; each circuit is capable of driving 150 mA. Each circuit is driven by complementary outputs of a flip-flop; therefore, only one circuit of the writer is enabled at any one time.

The steady state magnetizing current flows from +10V through the G286, G285, and G284 to -15. Current transitions flow the same way, but ground return is accomplished by AC coupling on separate wires that are isolated from system ground by 10 ohms.

Standard DEC levels enable the G284 with a wave propagation time of less than 50 ns to full rise time at 150 mA write current. The input load is 1 mA shared among the inputs that are at ground potential.

The power requirements for the G284 are shown below.

Pin	Normal Voltage	Marginal Check Limits		Current (mA)
		Min.	Max.	
A	+10	+ 5	+15	2
B	-15	-10	-20	125

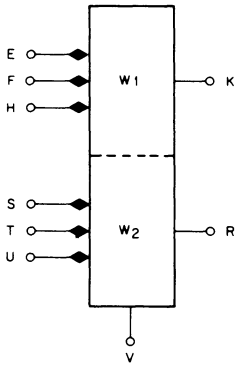


Figure 3-5 Block Diagram, G284 Disk Writer Module

3.6.3 G285 Series Selector Switch

The G285 Series Selector Switch is used with the G286 Center Tap Selector for the selection of the addressed read/write head. The G285 contains two identical circuits, each circuit acts as a

double-pole single-throw switch capable of switching up to 150 mA at 25V. Current flow is unidirectional. The head matrix side of the switch must be biased positive (normally+9V) and the other side negative (normally -13V) with respect to ground.

Standard DEC levels are inputs to the G285. The input load is 1 mA shared among the inputs that are at ground. The input gates at each switch operate as negative AND circuits.

The power requirements for the G285 are shown below.

Pins	Normal Voltage	Marginal Check Limits		Current (mA)
		Min.	Max.	
A	+10	+ 5	+15	25
B	-15	+10	-20	35

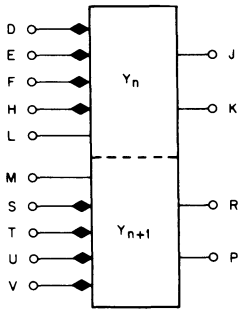


Figure 3-6 Block Diagram, G285 Series Selector Switch Module

3.6.4 G286 Center Tap Selector

The G286 Center Tap Selector is used with the G285 Series Selector Switch to select the addressed read/write head. Each G286 module contains four identical circuits, each capable of supplying 150 mA to the matrix.

Standard DEC levels are inputs to the G286 module. Each input circuit operates as a negative AND circuit. Input load is 1 mA, shared among the inputs that are at ground potential. Inputs F and H may be loaded with up to 4 mA. Ground wave propagation through each circuit is 500 ns maximum for both turn-on and turn-off time.

When not selected, the outputs are biased to -15V. A selected output is +4V. Each circuit can drive a maximum of 150 mA with an external load voltage of up to -15V in reference to +9V.

The power requirements are shown below.

Pins	Normal Voltage	Marginal Check Limits Min.	Marginal Check Limits Max.	Current (mA)
A	+10	+15	+15	100
B	-15	-10	-20	20

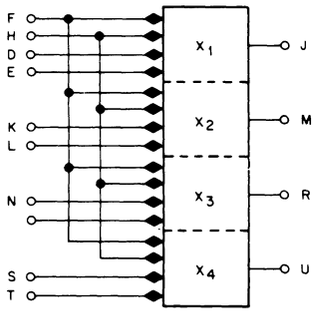


Figure 3-7 Block Diagram, G286 Center Tap Selector Module

3.6.5 G702 Disk Simulator

The G702 Disk Simulator (lamp) Module is used to indicate the ability of the disk logic to select the read/write heads, replacing the disk during the diskless diagnostic maintenance program. The module contains 16 indicators directly associated with the heads 0 through 17 (octal count). The module also simulates the photo sync mark. Pin C is grounded when the switch is closed manually. The associated photo sync circuit receives a simulated sync mark. The lamp module replaces the interconnecting cable between the logic and the disk head assembly. Use of the lamp module permits the field service personnel to test the disk logic without the disk. Associated circuits tested with the lamp module are the X-Y matrix (G285 and G286) and the writer (G284), together with their associated circuits.

The lamp module gives the operator a visual indication of the head matrix selection. The lamps can cycle in sequence, with proper operation of the matrix and associated circuits. If a lamp does not illuminate or is lit out of sequence, the matrix of its associated circuit is defective. The current flow to light the lamps is comparable with that observed while writing.

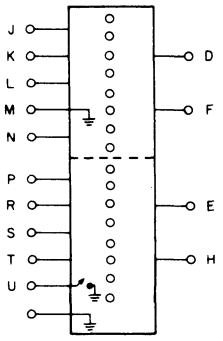


Figure 3-8 Block Diagram, G702 Disk Simulator Module

3.6.6 54-4073 Photocell Amplifier

The photocell is designed to mount directly on the DF32 base assembly. The amplifier detects the presence of a reflective spot on the disk edge, denoting the beginning of timing, address, and data tracks. The module contains the photocell light bulb and amplifier circuit on the same integrated printed circuit board. The circuit contains circuitry to maintain thermal stability, ±5V margin on the +10, -15 supply and output signal width adjustment. This assembly is adjustable near the disk edge to compensate for mechanical tolerances.

The photo diode has a pickup surface of 1 cm square. The reflective gap on the disk edge is approximately 0.125 x 0.25 in., and activates the photo diode for approximately 200 μs. In conjunction with the photo amplifier the output signal is adjustable.

The signal output is grounded when the reflective surface is in front of the photo diode. When the reflective surface is away from the photo diode, the signal goes towards -15V. An external clamp voltage of -3V must be connected at the terminal end of the output line and must not exceed 5 mA. Output rise and fall times are 2 μs. The photo-amplifier output signal is adjustable over a range of 100 to 300 μs.

The power requirements are shown below.

Pins	Normal Voltage	Marginal Check Limits		Current (mA)
		Min.	Max.	
A	+10	+ 5	+15	100
B	-15	-10	-20	7

3.6.7 G680 Disk Head and Matrix

The G680 circuit is mounted on the underside of the base plate assembly and consists of the read/write head, shock mount, and the resistor/diode matrix circuit board. The entire assembly is adjustable on the vertical axis to select the proper tracks and on the horizontal axis, to adjust the flying head gimbal tension. Each assembly contains four read/write heads. The matrix circuit is designed to operate with the G285 and G286 Matrix Selectors. The matrix circuit is capable of withstanding 100V reverse bias when not selected. Resistive values are set to permit 70 mA peak-to-peak current through the head when writing.

The read/write head and the resistor/diode matrix are connected in a delta network configuration. Two legs of the three-leg configuration are resistive legs, and the third is the head coil. This is advantageous because it does not require a center-tap head coil. Therefore, head balance is maintained via the precision resistance of the resistors. The delta network maintains a constant terminal impedance relative to the G083 preamplifier input.

The load is approximately 1000 ohms resistive and 5400 ohms reactive. High frequency noise causes the reactive load to increase to a point where the L/R ratio attenuates the noise amplitude.

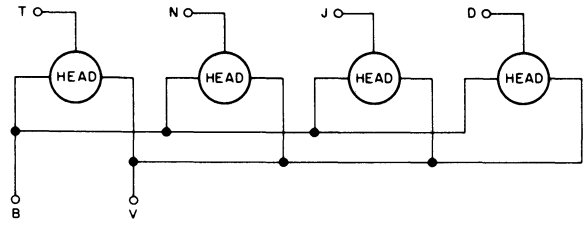


Figure 3-9 Block Diagram, G680 Disk Head and Matrix Module

CHAPTER 4
INSTALLATION

The DF32 and DS32 have been designed to mount in a standard DEC cabinet using "Chassis Track" slides number C-300-S-20. The slides are mounted on the rear of the front mounting rails and the side of the rear corner posts. This configuration allows the whole unit to be pulled out of the cabinet on slides. The two mounting panels on the front tilt forward approximately 30 degrees for access to modules.

The depth of the units is 21-1/4 in. from the mounting surface to the rear. At least 1 in. of additional space should be allowed for cables to turn over the back edge of the unit. It is impossible to mount any equipment on the rear door of a DEC cabinet behind the unit.

If a single DF32 unit is being installed, it can mount anywhere in a cabinet provided the above mentioned restrictions are adhered to. If a DF32 and one or more DS32s are being installed, they should be mounted with the DF32 on top and the additional units below. In most instances, a separate cabinet will be required for this configuration.

When shipped with a system, the disk unit will be shipped in a separate box rather than in the system cabinet and must be installed on site. In this configuration the tracks are already in the cabinet and there should be no problem assembling the system. In the event that the unit is to be "field installed" in a DEC cabinet on an existing system, it may be necessary to drill eight 1/4 in. holes and install 10-32 "Rivinuts" according to the dimensions in Figure 4-1.

4.1 POWER AND CABLE REQUIREMENTS

The disk system is equipped with a 728 power supply (for 60 cycle ac) or a 728A Power Supply (for 50 cycle ac). Other peripheral devices may use power from this supply if it is available. Care should be taken to insure that in the event of later expansion of the disk system the necessary power will be available. If there is a 128K disk system, there will be no dc power surplus from the 728/728A supply.

For 50 cycle systems, a 1725 Multitap transformer is used to provide the 118V, 50 cycle ac power for the disk motors.

The I/O cabling is mylar Flexprint. These mylar cables should be kept within the confines of the system cabinetry. Should it be necessary to route cables outside of the cabinet, the heavy black coaxial cables are used. With these heavy cables, extreme caution should be exercised when withdrawing the unit on slides or tilting the front panel. When it is used on a PDP-8 or PDP-8/I this system requires 11 I/O cables; on a PDP-8/S, it requires 13 I/O cables (from the PDP-8/S 3-cycle break logic to the

disk logic). The I/O cabling between DF32 and DS32 requires 5-1/2 ft when they are mounted one above the other. (See Figure 4-2 for I/O cable connections.)

The ac power for the disk motor should be supplied directly from the input to the computer and not from the power control. Disk motor power should not be turned off and on any more than is absolutely necessary because of the contact start-stop between the heads and disk. Excessive start-stop creates excessive wear.

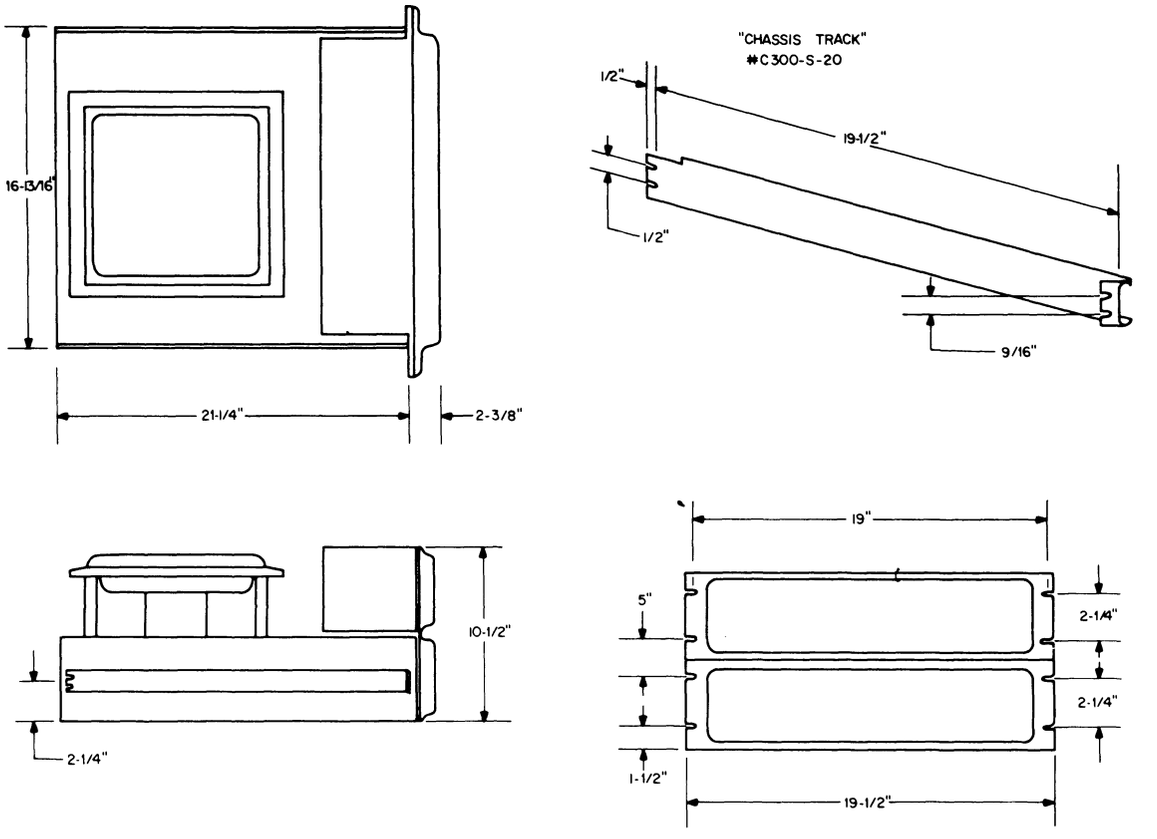


Figure 4-1 Mounting Dimensions

4.2 MOUNTING SUGGESTIONS

A single disk unit will fit in a CAB-8 configuration, below the table, and the remaining space will accommodate an 804 Logic Rack. This configuration should be avoided if possible because of the poor accessibility of the units.

The mounting suggestion, and spare-assignment priorities for DF32/DS32 installation with a PDP-8/I processor are discussed in the 1968 edition of Small Computer Handbook (C-800).

In an expanded disk system the units should be mounted one below the other with the DF32 on top. This makes the neatest, most efficient use of the cables which go between units.

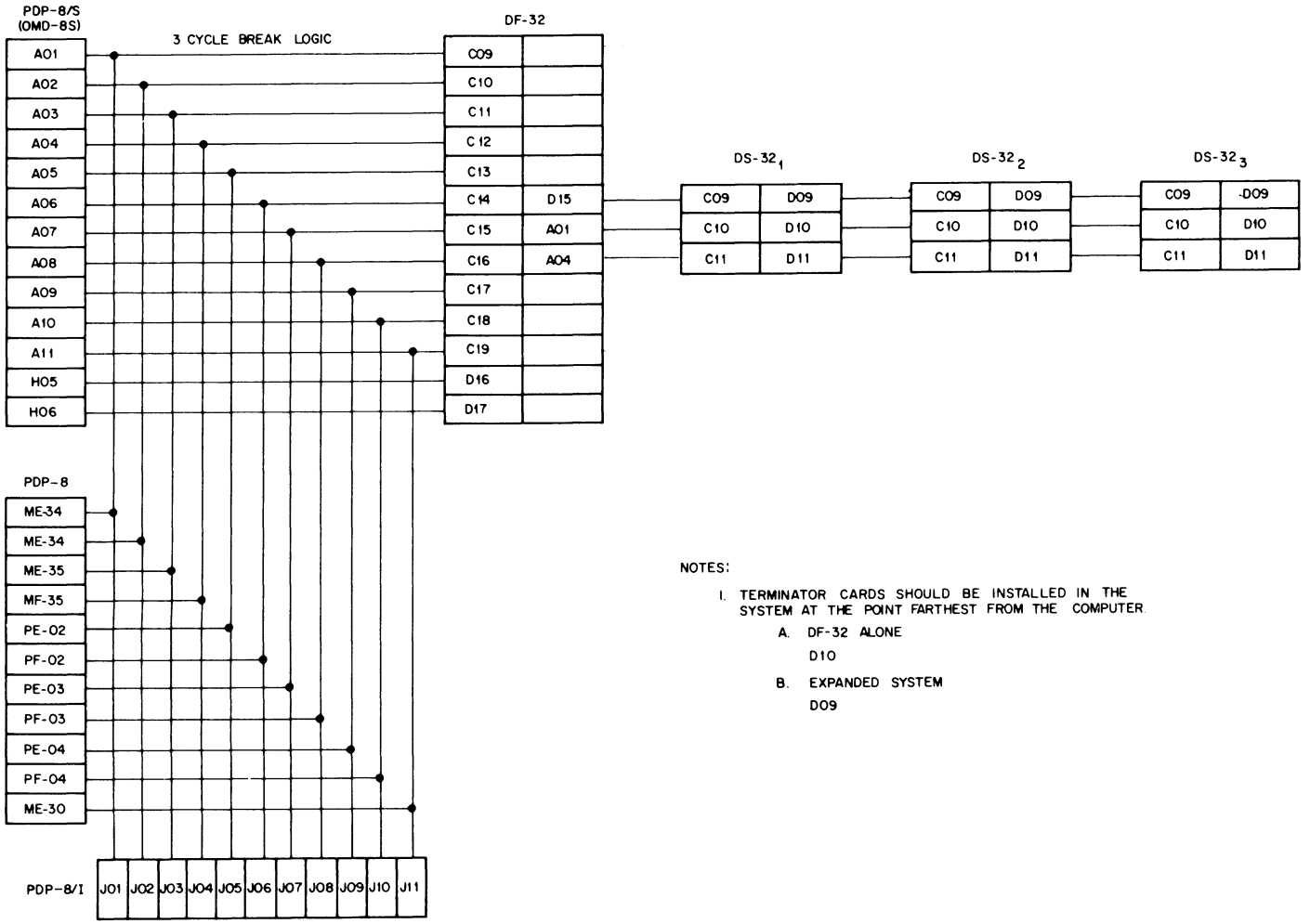


Figure 4-2 PDP-8, PDP-8/S, PDP-8/I Cabling

CHAPTER 5
MAINTENANCE

The information contained in the following paragraphs is presented as an aid to servicing the DF32 Disk File. Proper and efficient maintenance requires a thorough understanding of system operation with the PDP-8/I, and PDP-8/S processors. General and typical descriptive maintenance procedures for standard DEC products are available from the PDP-8, PDP-8/I, and PDP-8/S Maintenance Manuals and in the Digital Logic Handbook (C-105). This chapter does not attempt to duplicate information contained in these source books.

5.1 DISK/HEAD CLEANING PROCEDURE

The following steps must be accomplished before the user performs the cleaning procedure.

a. Turn off all power to the logic circuits.

b. Turn off the disk motor.

c. Carefully pull the unit out on the slides making sure that the cables do not bind.

d. Carefully remove the top dust cover.

e. Put on cotton or nylon gloves for the work that follows.

5.1.1 Disk Removal

The disk unit and associated parts are extremely critical and maintenance/cleaning should proceed with extreme care and absolute adherence to the instructions for handling and cleaning.

a. To remove the disk, brace one edge of it with one hand to prevent its turning when you loosen the four mounting screws. With all four mounting screws out, place your hands on opposite edges of the disk (Figure 5-1) and lift it off the hub with a slight twisting motion. Be certain that the disk remains parallel with the table top at all times during this operation.

NOTE

It is imperative that the disk be reinstalled with the same side up that was up before removal.

b. To clean the disk surface, use the soft paper towels in the Potter cleaning solvent kit. Moisten one part of the towels and wipe the disk surfaces clean. Then place the disk on a smooth surface with some clean soft paper towels beneath it. Cover it also.

c. To clean the heads, support the head/gimbal unit very gently with one hand (Figure 5-2). Clean head surfaces with cotton swab dipped in magnetic-head cleaning solvent. After cleaning the

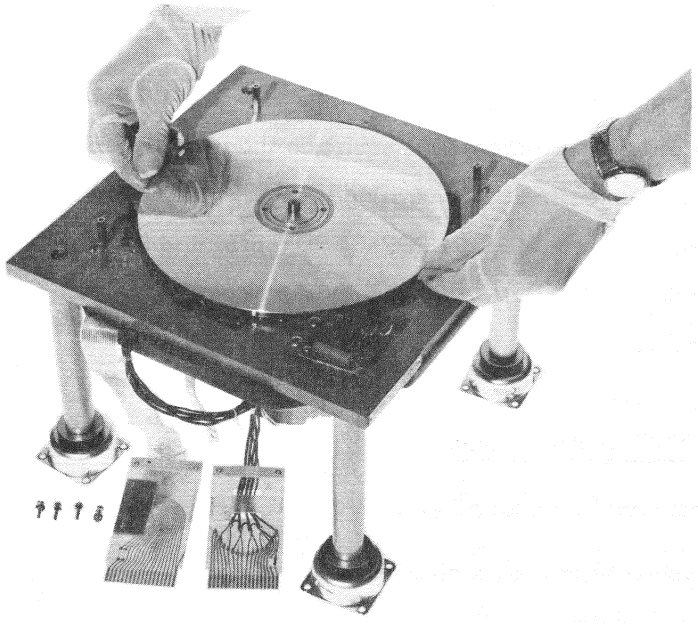


Figure 5-1 Disk Removal

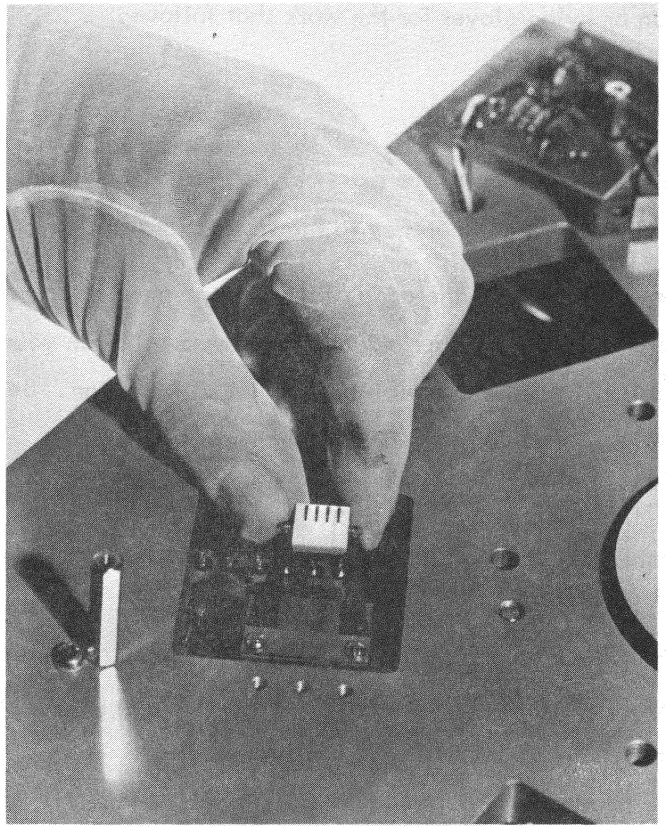


Figure 5-2 Head Cleaning

heads, wipe the head/shoe surface very gently with soft tissue paper to remove film. Repeat this procedure for all five pads/shoes.

Before reinstalling disk, wipe the table top clean with paper towel moistened with cleaning solvent. Be careful not to hit gimbal/shoe unit. Wipe the inside of the top dust cover also.

d. To reinstall the disk, make certain that the correct side is up. Grasp the disk in the same manner as for removal and place it back on the hub. The disk should remain parallel with the table top during this operation. Insert the four mounting screws and start them with your fingers.

NOTE

Some disks, due to differences in thickness of plating, have more space between hub and disk inside diameter than others. To insure centering of the disk, insert strips of paper or cardboard between the hub and disk at three points equally spaced around the circumference of the hub. With a screwdriver snug the screws while bracing the disk so that it will not turn. With all four screws snug, place a pencil, eraser down, on the table very close to the outside edge of the disk. Watch closely the clearance between the pencil and the disk while you rotate the disk by hand in a clockwise direction. If the gap appears to remain constant, remove the paper or cardboard and tighten the four mounting screws, taking care that the disk does not rotate while doing so.

e. Reinstall the top dust cover making certain that the access hole for the PSM adjustment pot is in the correct position. Check that the dust cover seal is tight.

f. Turn the disk motor on and listen for any unusual noise from the disk/head area.

g. Slide the unit back into the cabinet. Be careful not to damage the I/O cables.

5.2 TROUBLESHOOTING

The following listing is presented as an aid in the isolation of malfunctions that may occur in the system. This information pertains to either the disk and/or the logic circuits.

a. If an error typeout indicates that one address has failed within the whole disk, then the following possible conclusions can be drawn.

(1) The disk surface has begun to corrode in a spot.

(2) The data read preamp output has dropped marginally enough to cause error in reading this address.

(3) The head flying characteristics have changed.

(4) The write current has deteriorated.

(5) Dust or other surface contamination of the disk has occurred in one small spot.

b. When a series of address failures appear related to the disk position, the following possible conclusions can be drawn.

(1) A scratch has appeared on the disk.

(2) Either the timing or address track has been destroyed at this point on the disk.

(3) A large contamination has occurred.

(4) The timing or address track preamps have deteriorated.

(5) The timing address head has changed aerodynamically.

c. When a read failure occurs on all data tracks within a four-address span, one of the following conclusions may be drawn.

(1) A scratch has appeared along a radius of the disk.

(2) Timing relationships have changed on the timing and address tracks from write to read.

(3) A disk coating variation is apparent.

d. When a series of data words fail relating to a particular track, the following conclusions are drawn.

(1) The flying characteristics of the shoe pad containing the addressed track are unstable.

(2) The head involved has different playback characteristics than the others within the shoe or system.

(3) A circumferential surface scratch has appeared under this track only.

(4) The data read amplifier acceptance level is marginal to this track.

(5) The combination of low amplitude playback and surface contamination makes this track fail.

(6) The data strobe window pulse is not centered to the peaks of the playback signal on this track.

(7) The power level has dropped.

e. When a series of data typeouts appear consecutive where the data has shifted by 1, 2, 4, 8, 16 ATC addresses, but the data is good, then the following conclusions may be drawn.

(1) Address track TTB is low in amplitude therefore causing the bad data typeout to shift down in correlation with the good data as the result of dropping a bit.

(2) TTB track is high in amplitude and therefore susceptible to noise therefore causing a bit pickup resulting in a shift upward on the bad data typeout in relation to the good data.

(3) A logic failure has resulted relating to TP1, RDE, ABC, ABD, and TTA or TTB.

f. When nonconsecutive addresses fail, but do not repeatedly fail, it is considered a random address failure and the following conclusions can be drawn.

(1) A dust speck appeared instantaneously.

(2) The disk and head assemblies received a momentary shock or vibration.

(3) A line transient occurred, causing either electrostatic or electromagnetic fields.

(4) A poor connection exists in the logic system.

(5) A circuit component has deteriorated to the marginal point.

(6) Photocell noise injected a momentary disable.

(7) Assuming all random data is stored, a worst case pattern may exist during playback causing a marginal failure.

g. When a data failure appears to follow a certain pattern, the following conclusions may be drawn.

(1) The head to disk flying characteristics have changed, causing a drop in head resolution.

(2) Disk surface has become dirty.

(3) Cabling, the head, or read preamp may have changed characteristics.

(4) Deterioration of the read amplifiers for the data track only may cause a drop of bits.

(5) The data strobe delay may not be centered over the playback peaks.

(6) The data buffering logic may be sensitive to a certain pattern of data.

(7) Disk surface wear may cause data dropouts.

h. When the disk logic hangs in a loop looking for an address, the following conclusions may be drawn.

(1) A portion of the timing or address track may be erased.

(2) The amplitude adjustment of TTA and/or TTB may be not correct.

(3) Timing relationship between TTA and TTB may be such that a particular address cannot be found.

(4) The photocell sync mark may be too wide and disabling a portion of the address track.

(5) A logic failure is apparent either in the address register or the associated control logic.

i. When addressing seems to work well but data errors are considerable, the following conculsions may be drawn.

(1) One of the matrix circuits is failing.

(2) The data preamp or rectifying slicer circuits are failing.

(3) Poor write current rise time is causing poor playback signals.

(4) There is an aerodynamic failure in the head to disk relationship.

(5) Complete lack of data playback due to a short or open in the read/write logic.

j. When data parity errors appear, but no data errors, the following conclusions may be drawn.

(1) The write flip-flop and associated clear logic is faulty.

(2) The read parity detection logic is not complementing correctly.

(3) At parity strobe time, a data signal noise bit is being detected.

(4) The timing strobe for the parity bit is offset due to a poor resolution head causing peak shift.

k. Disk Head Misalignment

Using the all 1s data test, it is possible to detect an overlap of tracks. This is accomplished by comparing the readcheck against the read-after-write in the program, while observing the scope on the data amplifier.

For example, assume a condition where head 11 is actually on track 7. Using the all 1s data test and observing the program, the following events will occur.

Each read-after-write appears good until track 7 is written. During the writing of track 7, the previous history can be seen as the result of track 11. When track 7 is completely written with all 1s, the playback during the read cycle is good. After indexing up to track 11, and commencing to write, the same signal envelope appears. This envelope has the appearance of extremely low-amplitude signals associated with noise. After writing track 11, however, the read playback appears good.

Assuming that all other tracks are good, tracks 1 through 6 are confirmed during the readcheck. Track 7, however, shows a complete lack of signal, or the addition of an out-of-phase signal. This is caused by track 11 data being added to that previously existing on track 7. It should be noted that, during readcheck, track 11 is confirmed as operational.

Through analysis of the sequence of events and observation of the oscilloscope, it can be determined that any one of three possible failures could cause these indications. They are as follows.

(1) Failure of the matrix selection circuits in the logic. This failure can be eliminated or isolated through the use of a light-board test.

(2) A short or malfunction in the head and matrix cable connecting the logic to the disk. This failure can be isolated or eliminated through the use of the matrix-head cable tester.

(3) Pad misalignment causing track overlapping. This failure can be isolated or eliminated through the use of a program which writes the address of each track on that particular track. By calling out the data written in each track, the observer can readily determine whether or not track overlapping is occurring. During this test, the ADC flip-flop is used as the synchronizing point.

The final conclusion which can be drawn from the foregoing is that if no failures occur while reading after writing, but a failure appears during the readcheck, the most likely possibility is an overlapping track.

5.3 DISK OPERATING PROCEDURE FOR TIMING TRACK WRITER, DF32

a. Disk logic connected to disk assembly.

(1) Turn all dc power off.

(2) Remove the timing track cable from disk logic location B32 or B31.

(3) Plug this cable into the timing track writer, C2.

(4) Remove the matrix harness cable from disk logic location A5.

(5) Plug this cable into the timing track writer, labeled C1.

(6) Set the photocell switch position to up.

(7) Turn the disk motor ac power on.

(8) With dc power jumper cables plug the timing track writer power into the disk logic power tabs.

(9) Turn the dc power on.

(10) Press the WRITE 1 switch down to turn the write enable off if it is not already off. The pushbutton light should be off.

(11) Using an equivalent to the 543A oscilloscope plug the scope sync lead into the red banana plug labeled number 5.

(12) Place the scope sync external negative AC (slow).

(13) Using probe A in banana jack number 6 red, set the scope to 50 μs/cm horizontal and 2V/cm vertical.

(14) The output being observed is the photocell. Readjust the photocell if necessary for a 200 μs time period. The adjustment is located through the top cover of the mechanical assembly.

(15) Change the scope to alternate sweep and plug probe B into banana jack number 8. This test point is the write disable delay which is initiated at the beginning of the photocell and terminates in the middle of photocell area.

(16) The associated adjustment with banana jack number 8 is P2, located directly along side of the jack. With a screwdriver adjust this delay time to 100 μs and observe on the scope the two traces ot the photocell and the delay together. If the signal from jack 8 appears to initiate at the end of the photocell time, then the photocell switch is in the wrong position.

(17) After adjusting the P2 delay, remove probe B from jack 8 and place it in jack 9. Leave the scope settings the same. This output is the write track enable delay and is initiated at the beginning of the photocell time. The associated adjustment for this delay is P3.

(18) Adjust the delay for 250 μs. In relation to the phtocell it would be 50 μs more.

(19) Remove probe B and place it in jack 1. Jack 1 and 2 are used to observe the amplified signal from the timing track TTA. During this step, however, jack 1 will be used for adjusting the clock rate on the timing track through the adjust of the P1 pot.

(20) Turn the WRITE 1 switch on. The indicator light should be on.

(21) Change the scope timer per centimeter to 5 ms. Set the scope channels to algebraic add and invert channel B. There should be a single track in the scope where there are two indications of a photocell. With a horizontal adjustment, place the second photocell mark in the direct middle of the scope face. Turn the magnifier to 100 X with the photocell remaining on the scope trace.

(22) Press the WRITE 2 button and hold it down while observing the scope. Clock pulses should be observed 50 μs following the end of the photocell and should continue off the edge of the scope face to the right.

(23) The area to the left of the photocell clock pulses should also be observed. By adjusting the P1 potentiometer, the clock pulses termination on the left of the photocell can be moved left or right. The time observed on the scope is 50 μs/cm. The termination of clock pulses to the left of the photocell should appear approximately 50 μs prior to the initiation of the photocell signal. The adjustment must be done while the WRITE 2 button is pressed.

(24) Once this adjustment has been made, remove the screwdriver and let go of the WRITE 2 button. Both timing and address tracks have now been written. The writing process simultaneously wrote the normal TTA track and the spare TTA track as well as the TTB tracks.

(25) Remove probe A from jack 6 and place it in jack 2. Change the time per centimeter magnifier back to 1. The total TTA track can now be observed on the scope trace. (See Figure 5-3.)

(26) By careful observation, one can observe bit dropouts or sections of the disk that may be low in amplitude and warrant readjustment of the timing track head. Should it be necessary to rewrite the timing tracks, repeat Steps 21 to 26 until a good track is written.

(27) To observe the spare TTA track, place the switch above jack 1 to the opposite position and check the signal characteristics of this track.

(28) Move probe A from jack 1 to jack 3. Move probe B from jack 2 to jack 4. Observe the signal characteristics as expressed in Steps 26 and 27.

(29) If all signals look good turn off the write enable labeled WRITE 1 by pressing the button. The indicator light should go off.

(30) Remove the timing and address track cable and the data head matrix cable from the timing track writer.

(31) Turn dc power off.

(32) Place the timing track cable plug into location B32 of the disk logic.

(33) Place the head matrix cable plug into location A5 of the logic on the master control.

(34) Unplug the dc power to the timing track writer.

(35) The disk system should now be ready for operational tests.

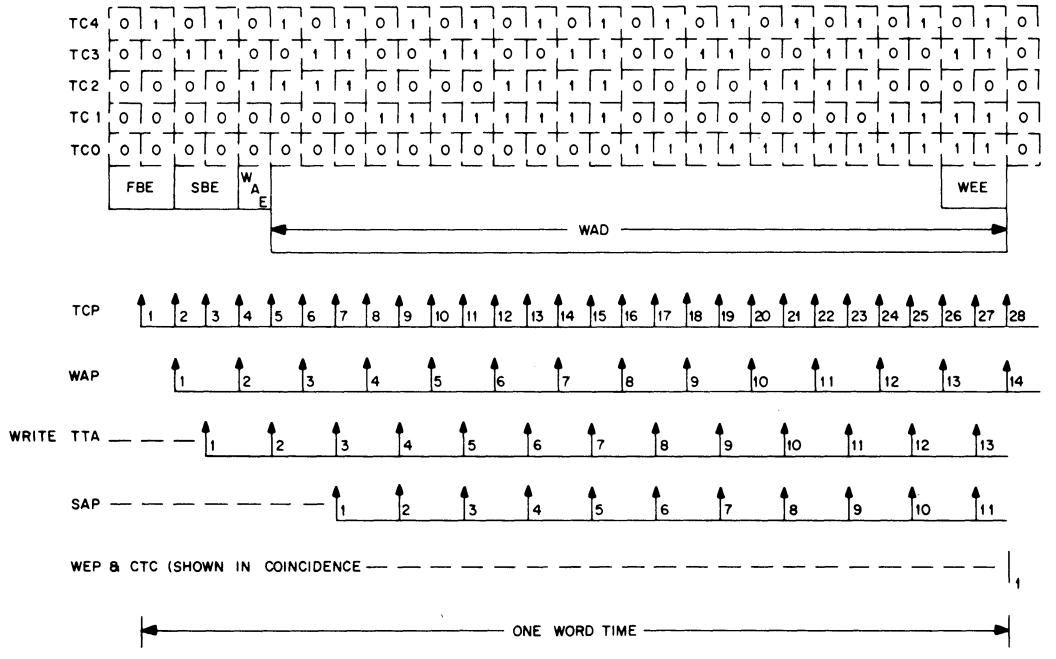


Figure 5-3 Timing Diagram for DF32 Disk Timing Track Writer

CHAPTER 6
ENGINEERING DRAWINGS

This chapter contains the standard block schematics, circuit schematics and engineering drawings necessary for understanding and maintaining the DF32 Disk File and Control. A list of the drawings as they appear in this chapter follows.

ENGINEERING DRAWINGS

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D-BS-DF32-0-1	Disk Control	C	6-3
D-BS-DF32-0-2	Disk Memory Address	A	6-5
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D-BS-DF32-0-4	Disk Memory Buffer	A	6-9
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D-TD-DF32-0-11	Disk Electrical Aid	A	6-25
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D-MU-DS32-0-2	Disk Expander UML	C	6-29
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D-BS-TW32-0-1	Timing Track Writer (Sheet 2)	B	6-33
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D-TD-TW32-0-3	Timing Track Writer Timing Diagram		6-37

CIRCUIT SCHEMATICS

B-CS-G083-0-1	Disk Preamplifier G083	D	6-39
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B-CS-G285-0-1	Series Switch G285		6-40
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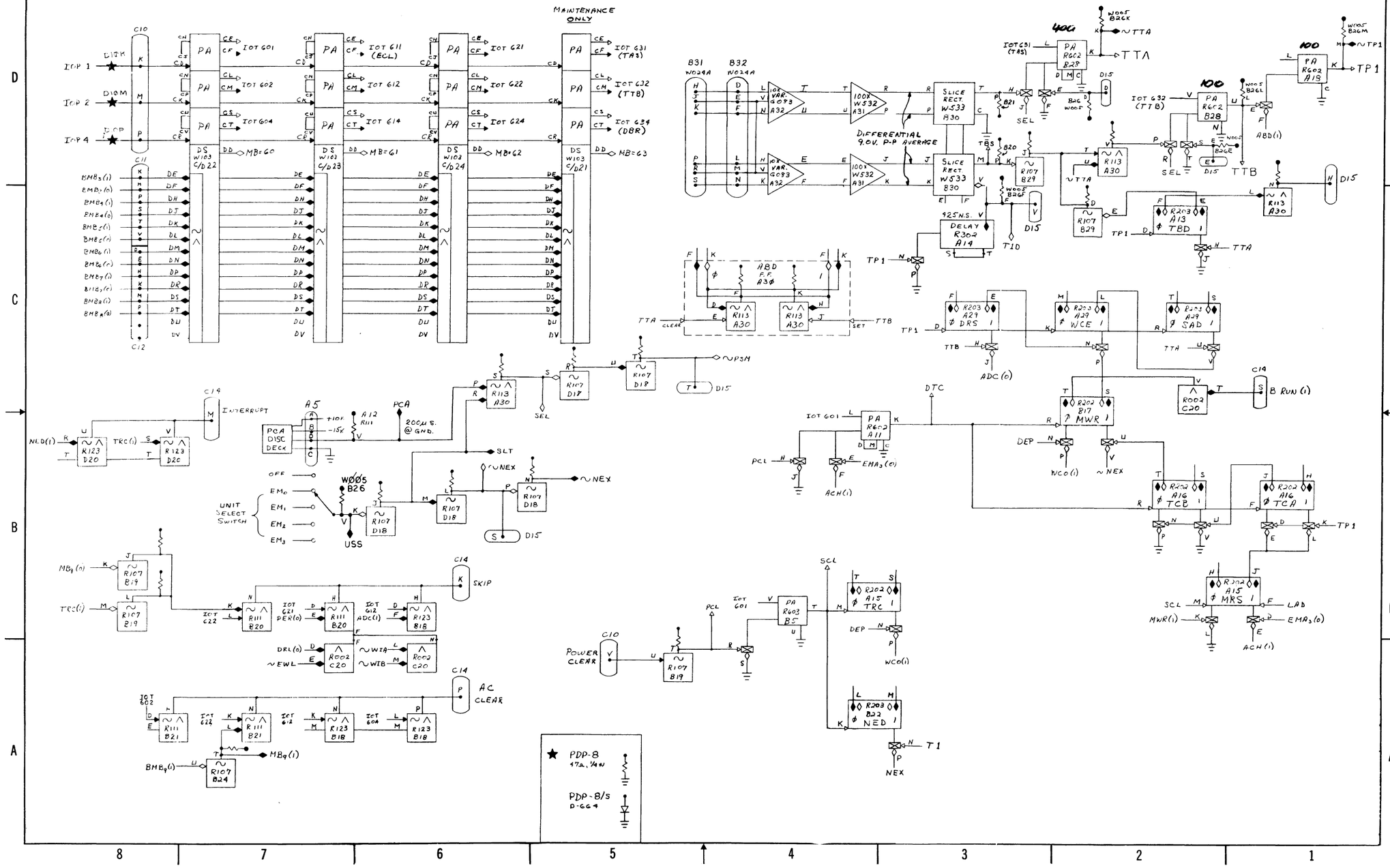
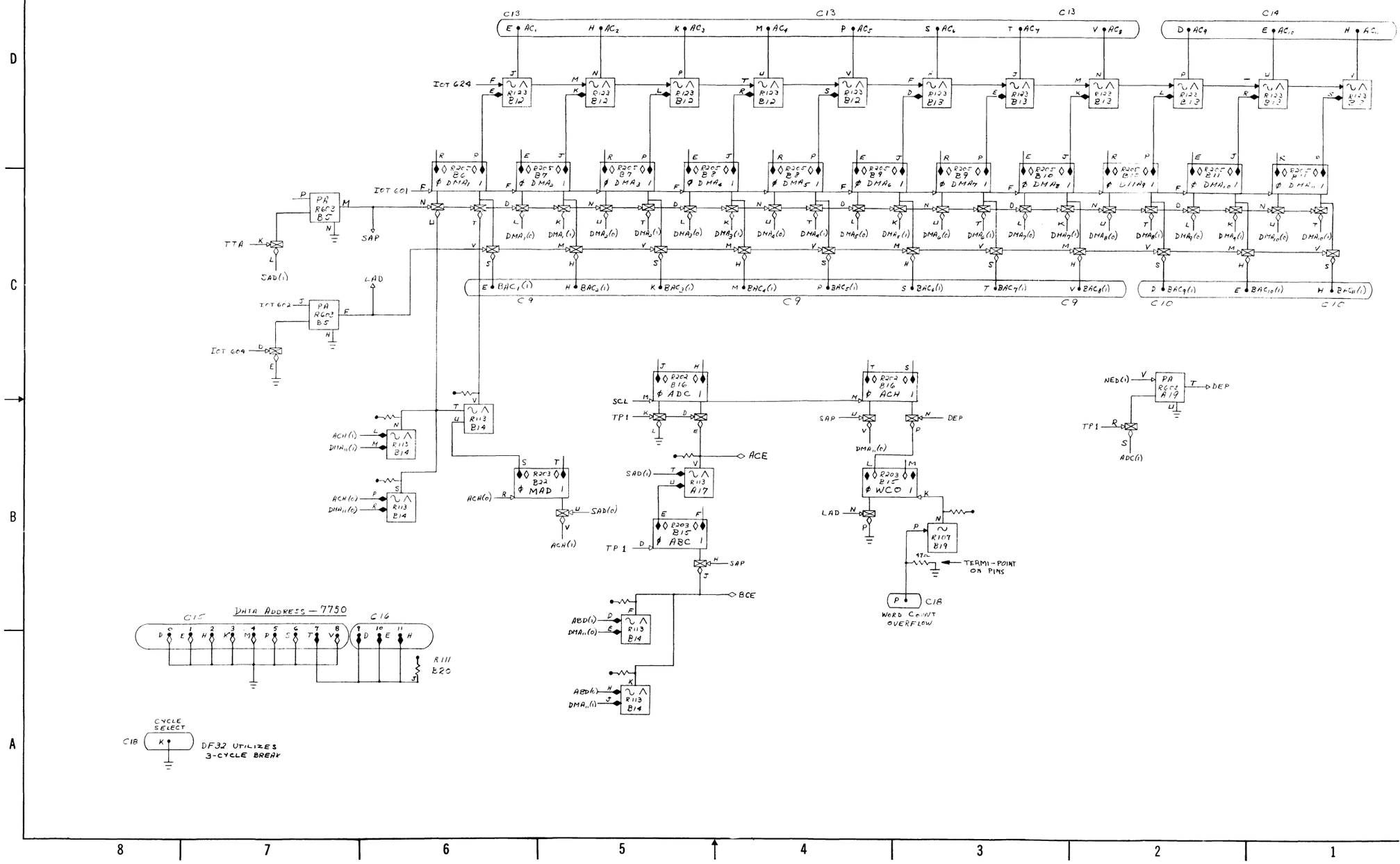
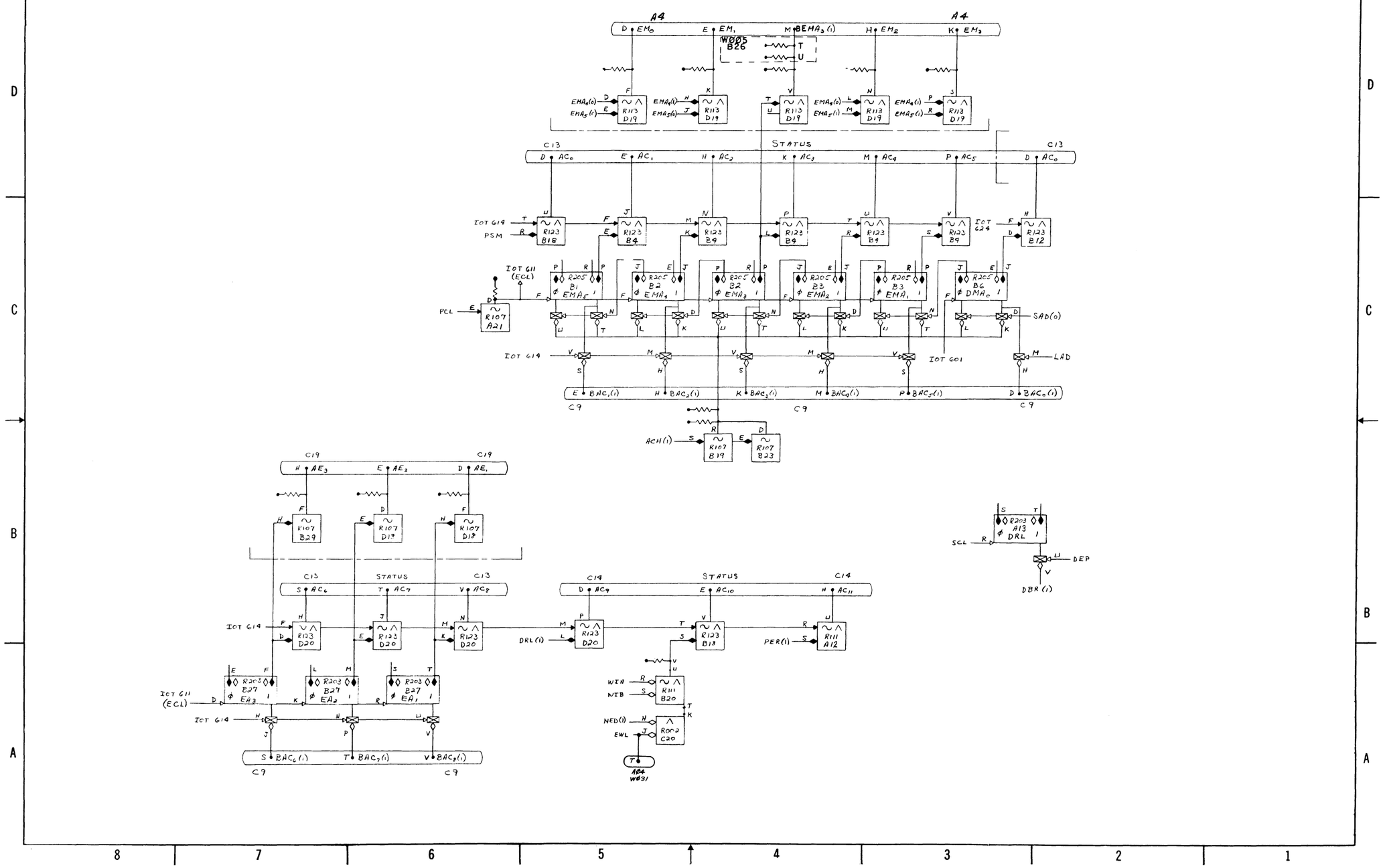
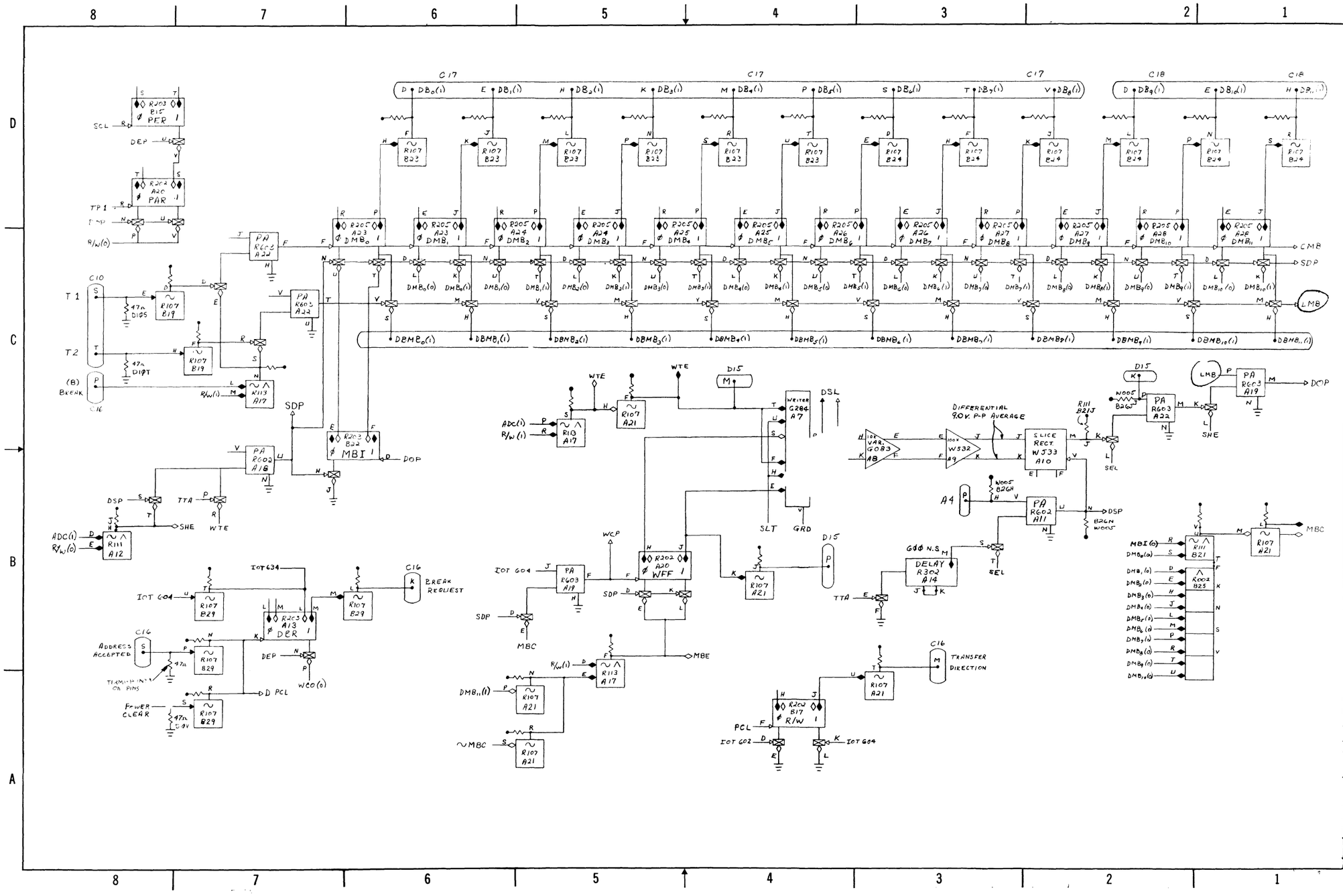
B-CS-G702-0-1	Disk Simulator G702	A	6-41
B-CS-5404073-0-1	Photo Cell Amplifier 5404073	C	6-42



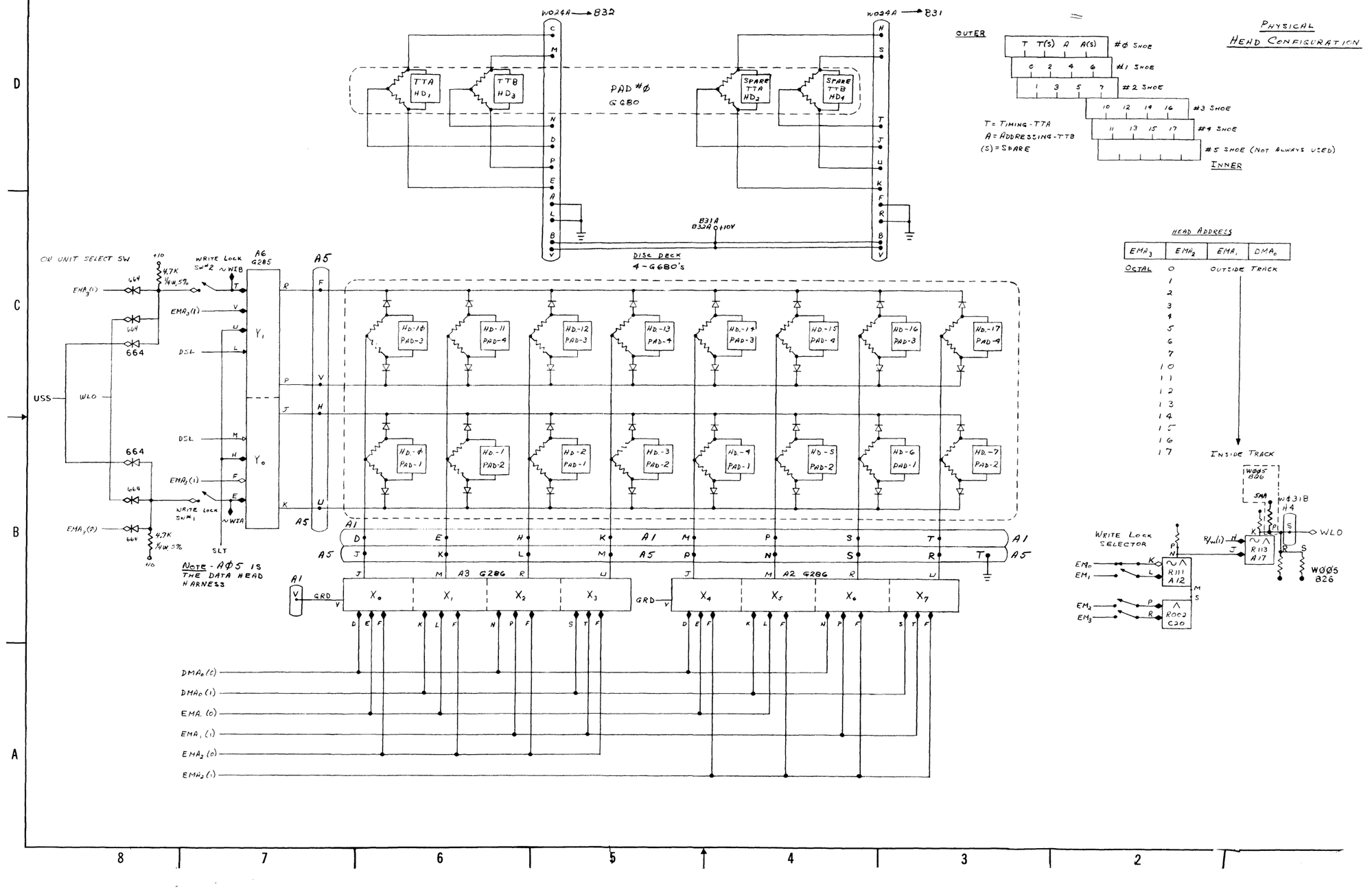
D-BS-DF32-0-1 Disk Control


C13
C14
IOT 624
IOT 601
IOT 602
IOT 604
TTA
SAD(i)
SAP
LAD
BAC1(i)
BAC2(i)
BAC3(i)
BAC4(i)
BAC5(i)
BAC6(i)
BAC7(i)
BAC8(i)
BAC9(i)
BAC10(i)
BAC11(i)
C9
C10
C16
ACH(i)
ACH(o)
SAD(o)
SCL
TP1
ACE
SAP
DEP
LAD
BCE
TP 1
NED(i)
DEP
ADC(i)
TERMI-POINT ON PINS
C18
WORD COUNT OVERFLOW
C15
DATA ADDRESS — 7750
C16
CYCLE SELECT
C18
DF32 UTILIZES 3-CYCLE BREAK

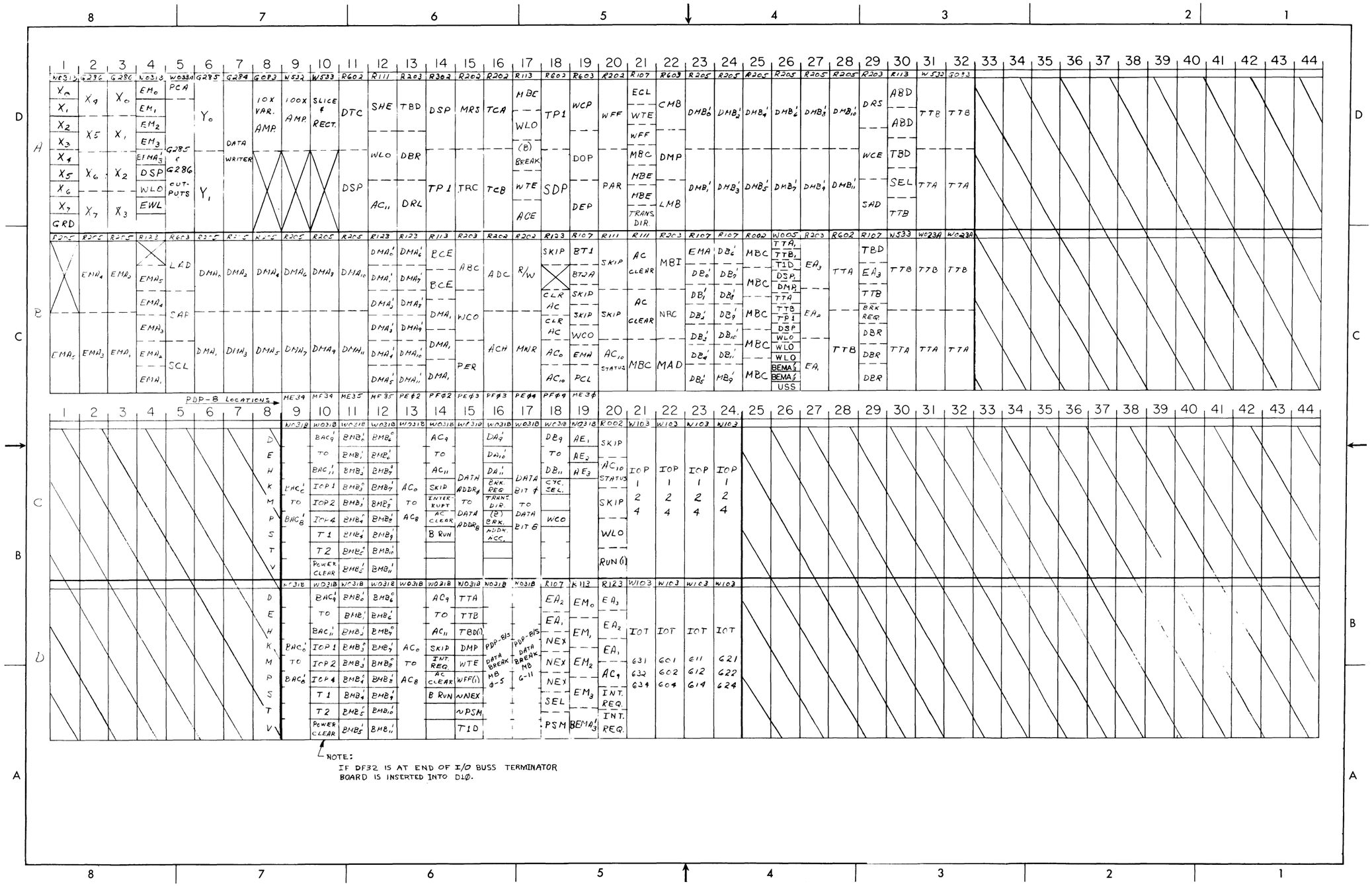

A4
A4
EM0
EM1
BEMA3 (1)
EM2
EM3
WØØ5
B26
T
U
EMA4(0)
EMA5(1)
EMA4(1)
EMA5(0)
R113
D19
STATUS
C13
AC0
AC1
AC2
AC3
AC4
AC5
IOT 619
PSM
IOT 624
R123
B18
B4
B9
B12
IOT 611
(ECL)
R205
B1
B2
B3
B6
ØEMA5
ØEMA4
ØEMA3
ØEMA2
ØEMA1
ØDMA0
PCL
R107
A21
SAD(0)
IOT 619
IOT 601
LAD
BAC0(1)
BAC1(1)
BAC2(1)
BAC3(1)
BAC4(1)
BAC5(1)
C9
ACH(1)
B19
B23
C19
AE3
AE2
AE1
B29
D18
STATUS
AC6
AC7
AC8
AC9
AC10
AC11
D20
DRL(1)
PER(1)
A12
WIA
WIB
NED(1)
EWL
R111
B20
R202
C20
ABA
WØ31
SCL
R203
A13
ØDRL
DEP
DBR(1)

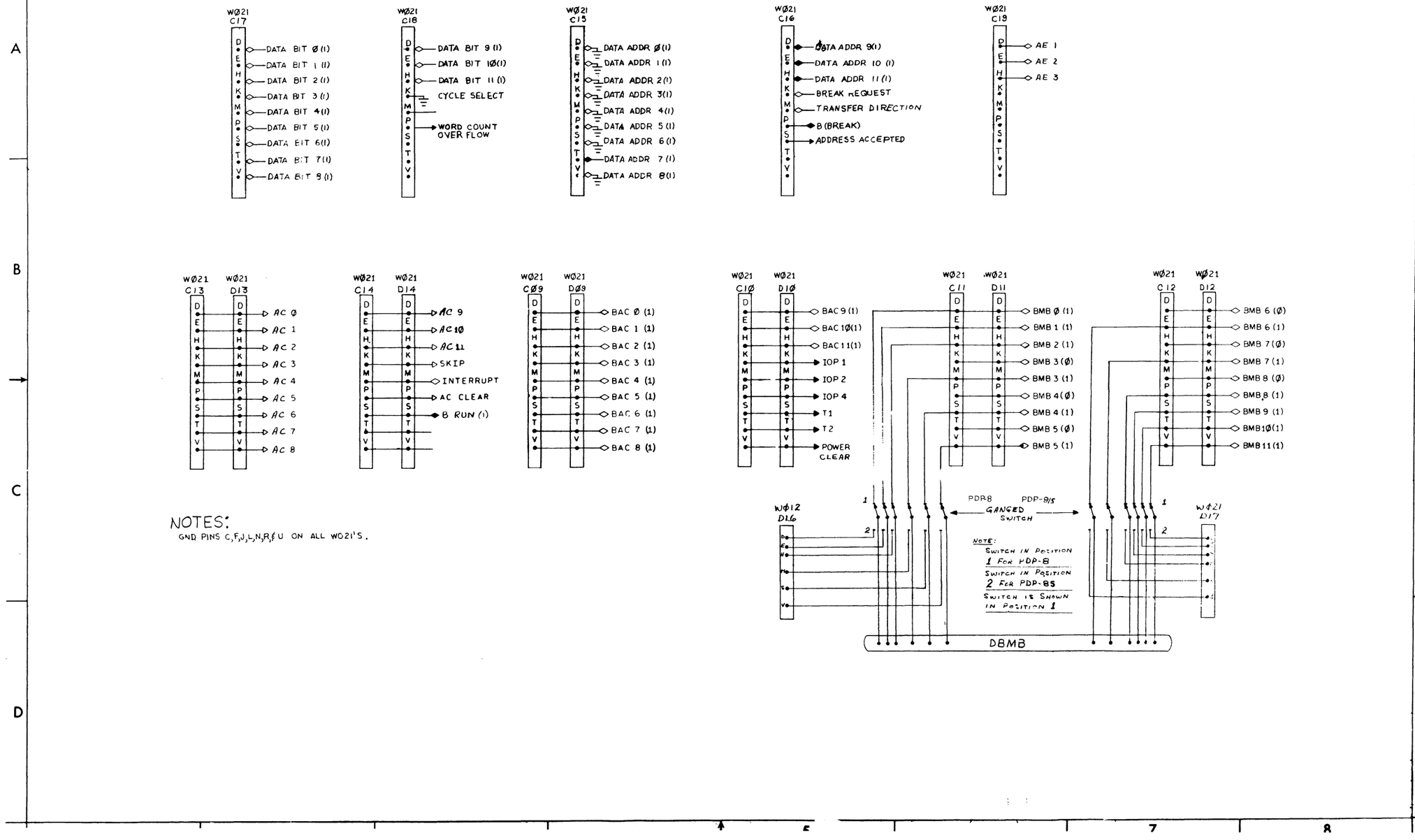


D-BS-DF32-0-4 Disk Memory Buffer

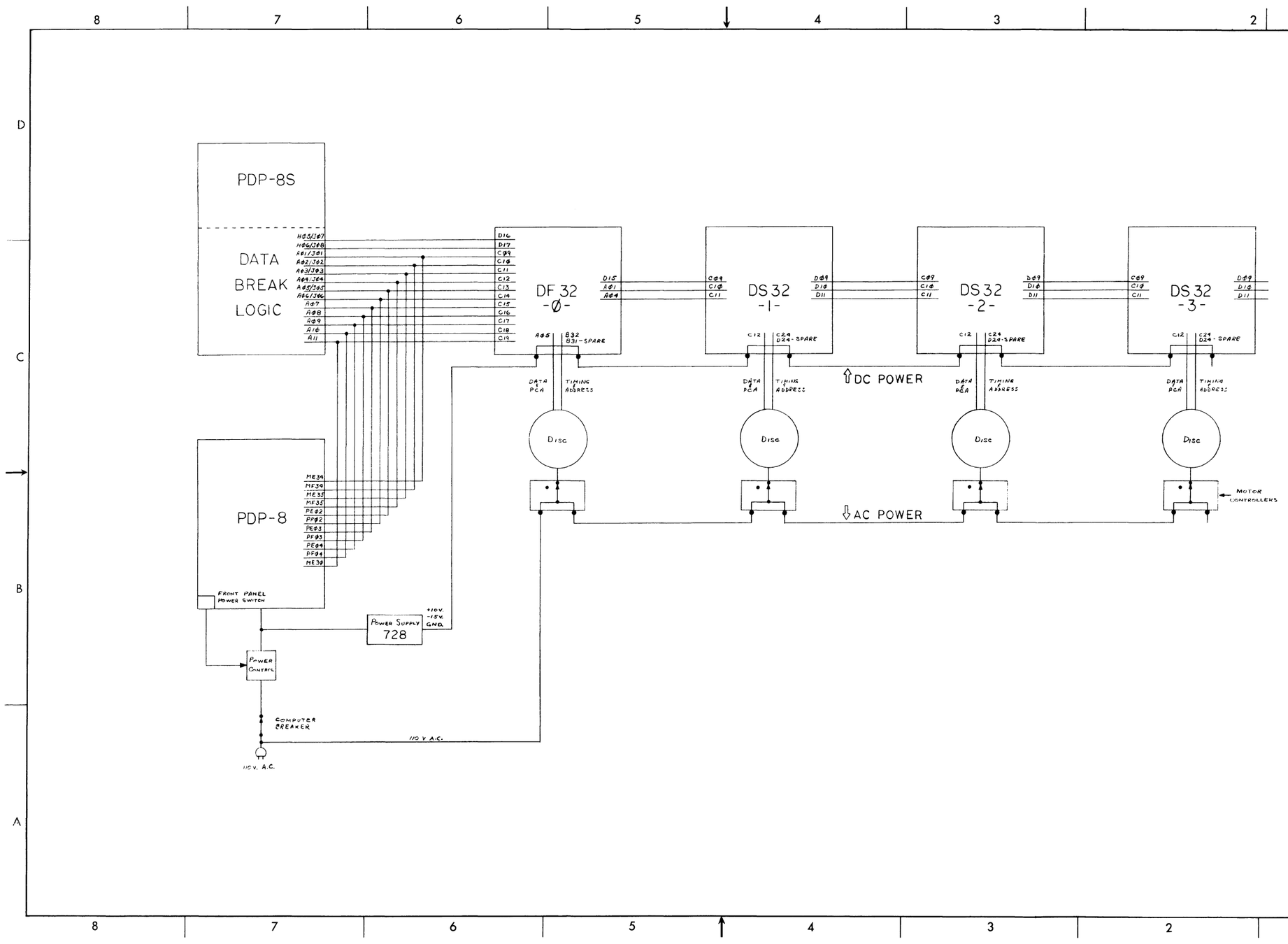


D-BS-DF32-0-5 Disk Head Diode Switch Matr

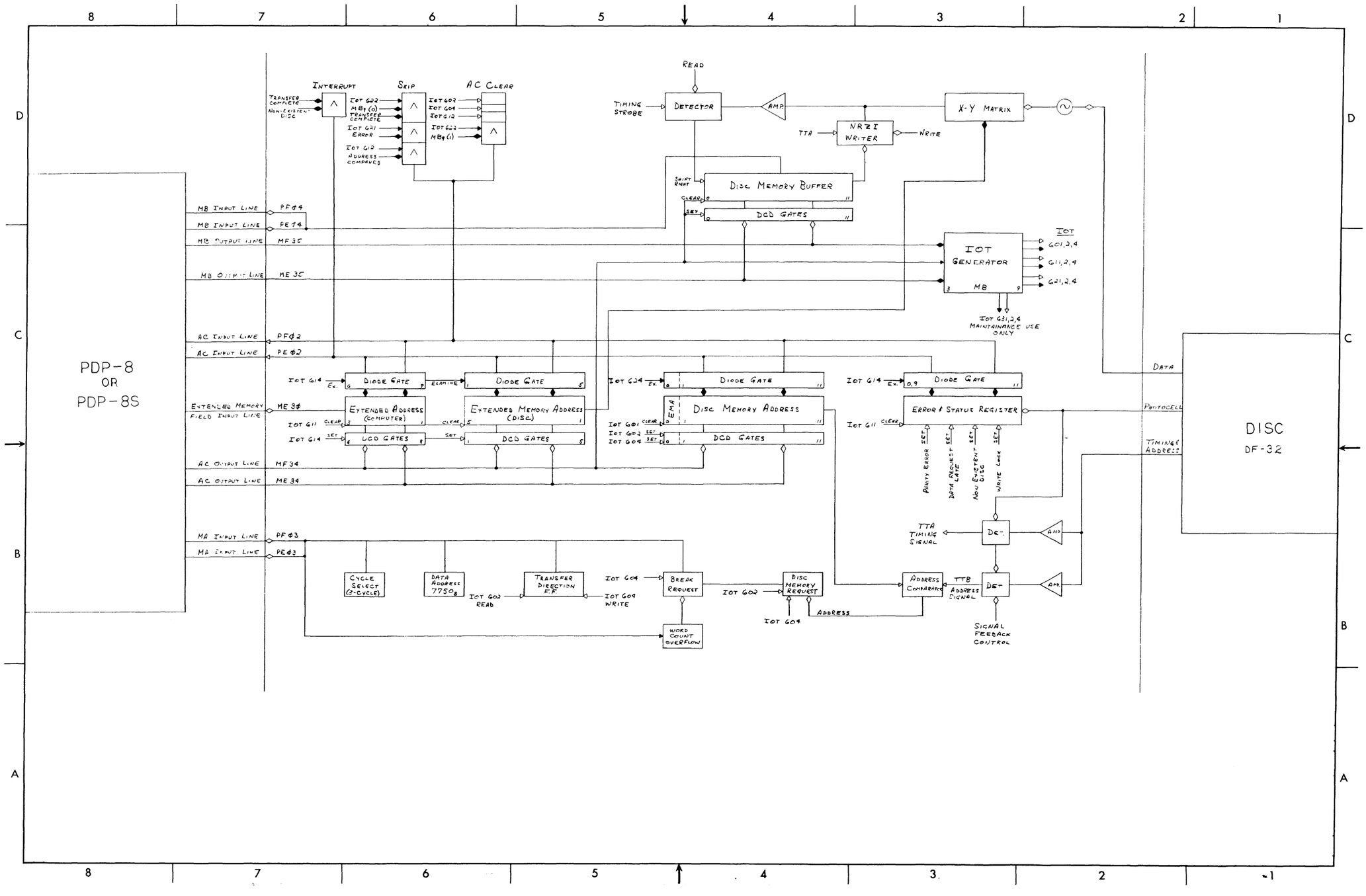

PDP-B LOCATIONS
NOTE:
IF DF32 IS AT END OF I/O BUSS TERMINATOR BOARD IS INSERTED INTO DLØ.



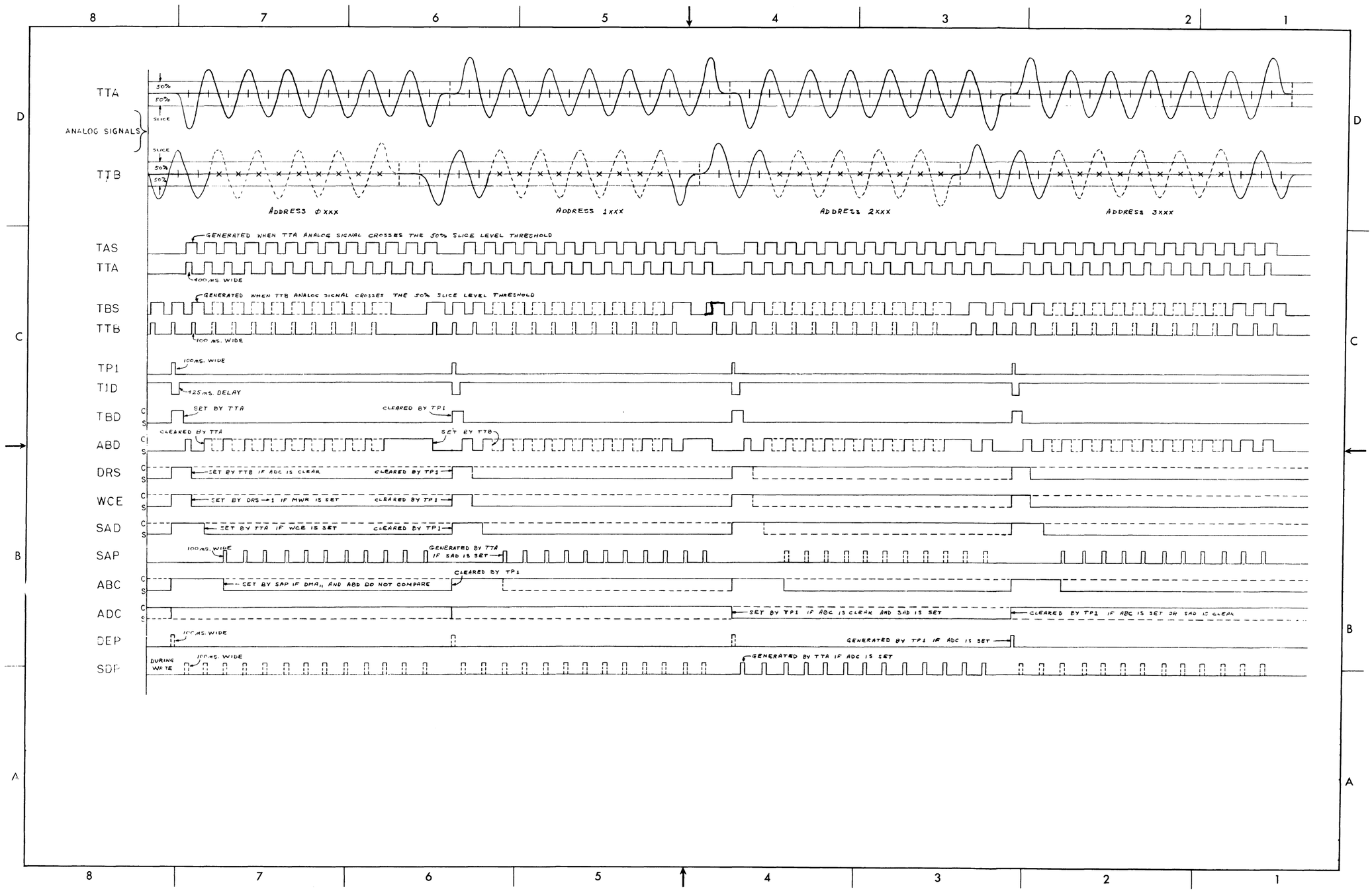
NOTES:
GND PINS C,F,J,L,N,R,&U ON ALL WØ21'S.



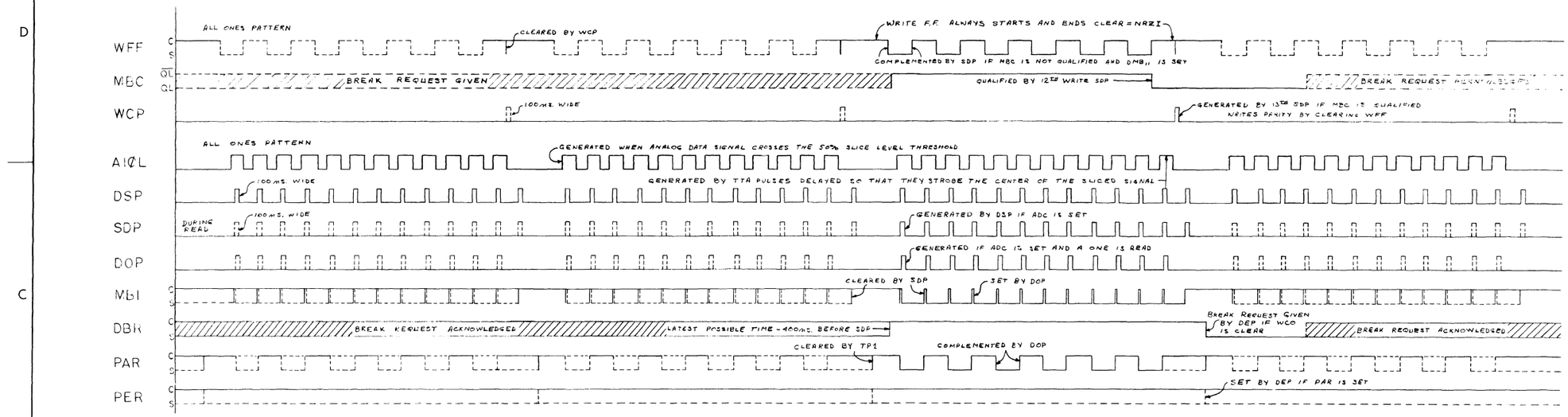
D-IC-DF32-0-8 Disk System Interconnection



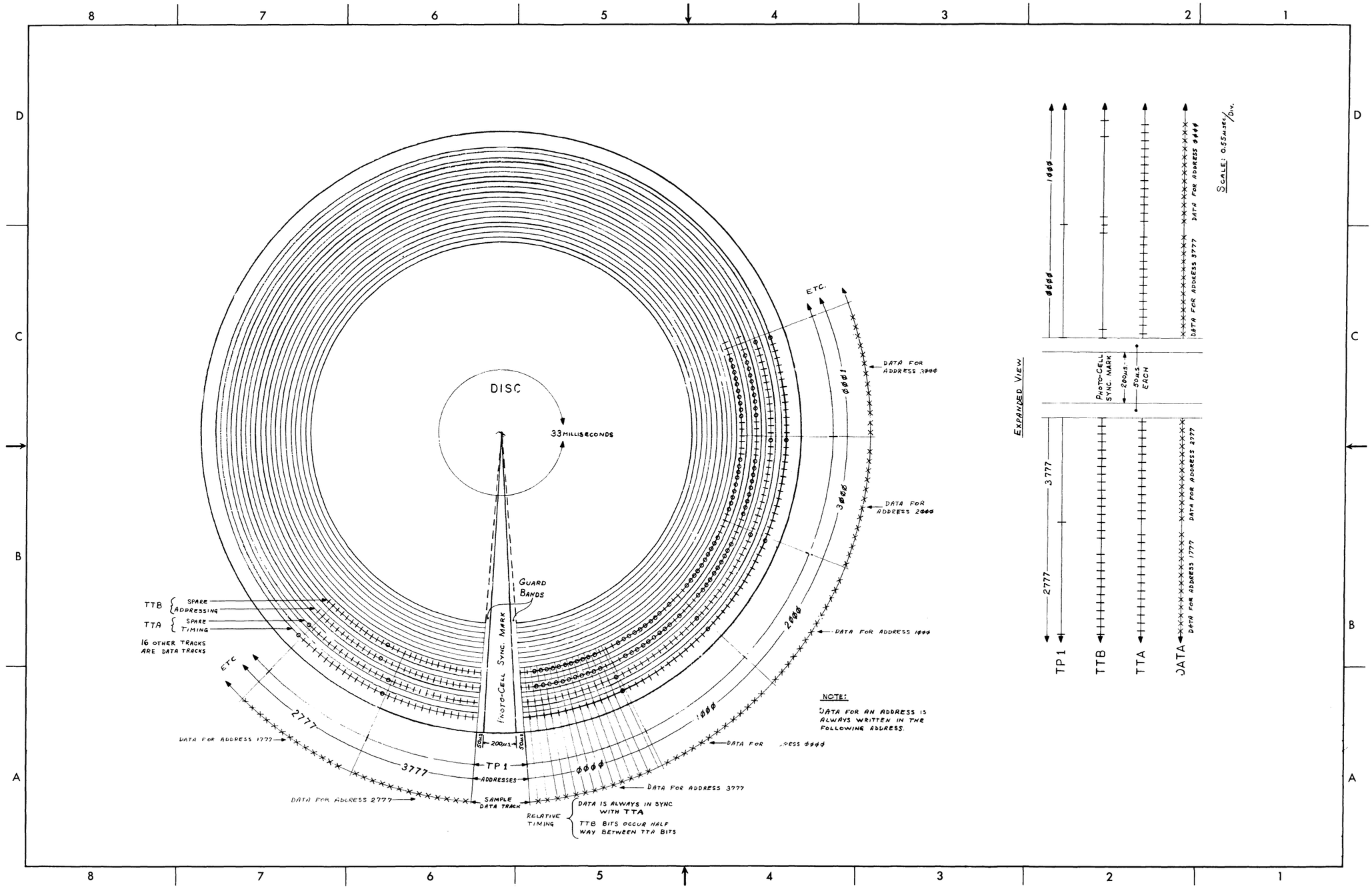
D-BD-DF32-0-9 Disk Block Diagram

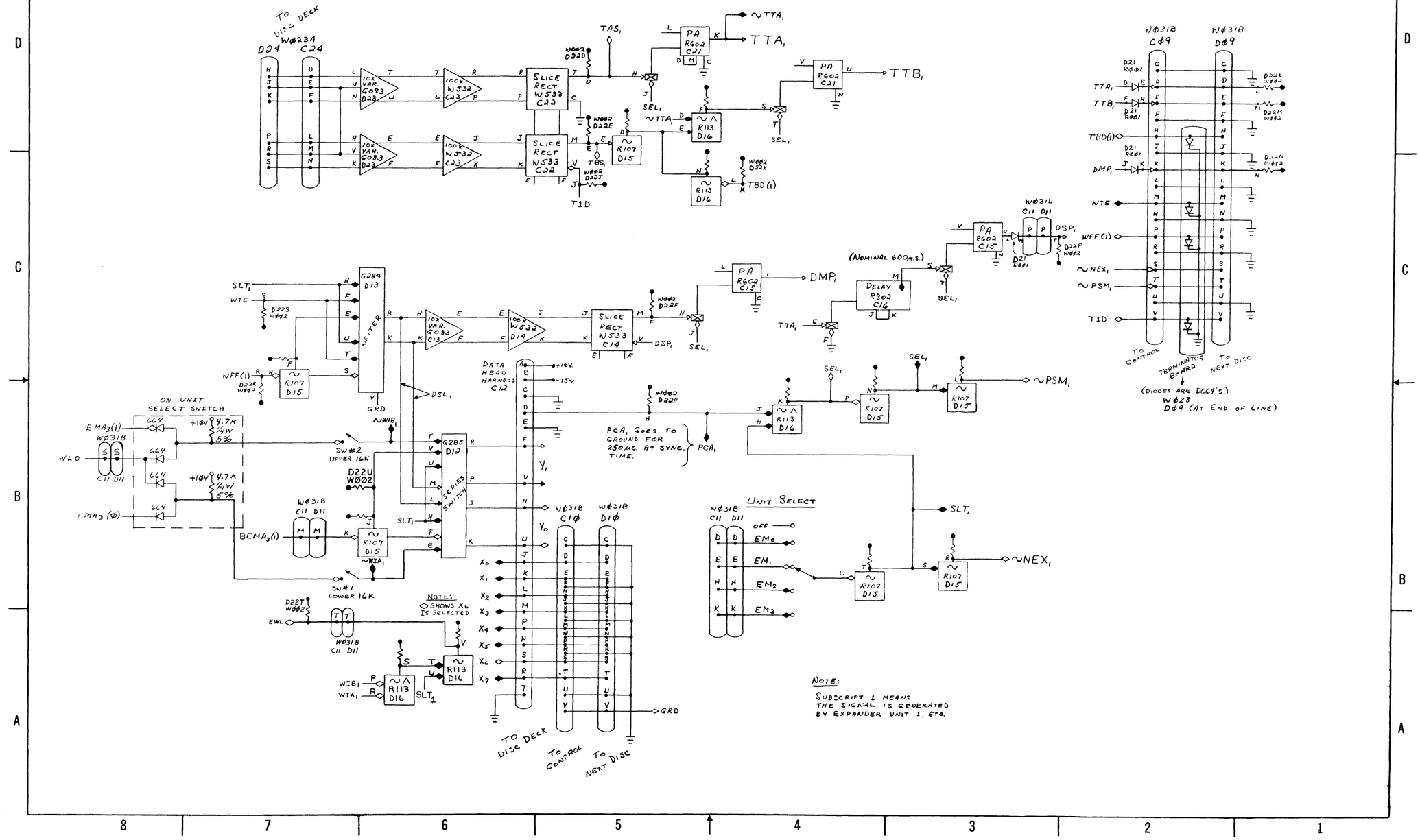


D-TD-DF32-0-10 Disk Timing (Sheet 1)

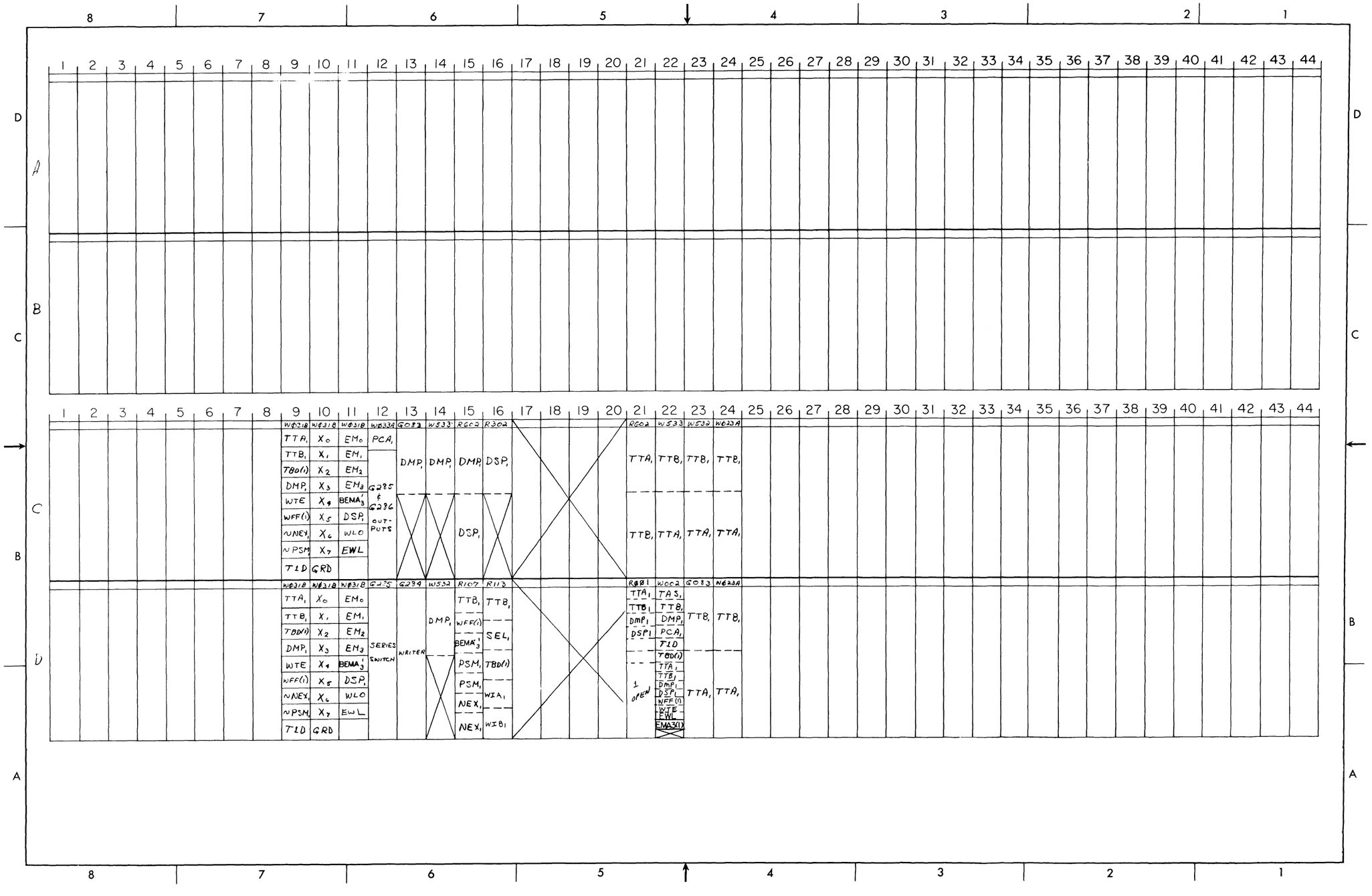


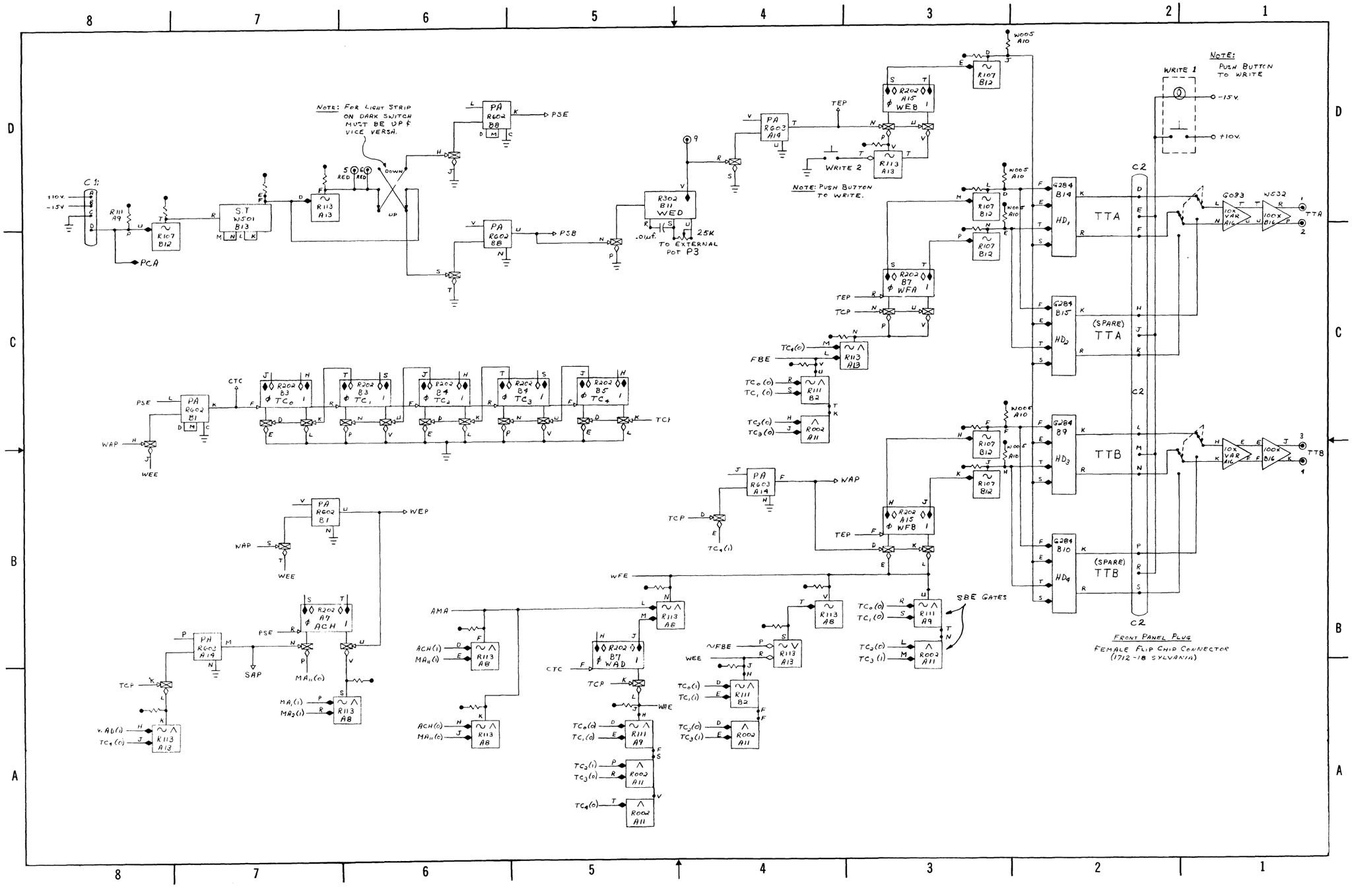
D-TD-DF32-0-10 Disk Timing (Sheet 2)


DISC
33 MILLISECONDS
GUARD BANDS
PHOTO-CELL SYNC. MARK
TTB
SPARE
ADDRESSING
TTA
SPARE
TIMING
16 OTHER TRACKS ARE DATA TRACKS
ETC.
DATA FOR ADDRESS 1777
2777
3777
TP 1
ADDRESSES
SAMPLE DATA TRACK
DATA FOR ADDRESS 2777
DATA FOR ADDRESS 3777
DATA FOR ADDRESS 0000
0001
3000
DATA FOR ADDRESS 2000
2000
DATA FOR ADDRESS 1000
1000
0000
DATA FOR ADDRESS 0000
50μs
200μs
50μs
RELATIVE TIMING
DATA IS ALWAYS IN SYNC WITH TTA
TTB BITS OCCUR HALF WAY BETWEEN TTA BITS
NOTE:
DATA FOR AN ADDRESS IS ALWAYS WRITTEN IN THE FOLLOWING ADDRESS.
EXPANDED VIEW
SCALE: 0.65μsec/DIV.
1000
0000
PHOTO-CELL SYNC. MARK
200μs
50μs EACH
DATA FOR ADDRESS 3777
DATA FOR ADDRESS 0000
3777
2777
DATA FOR ADDRESS 2777
DATA FOR ADDRESS 1777
TP 1
TTB
TTA
DATA

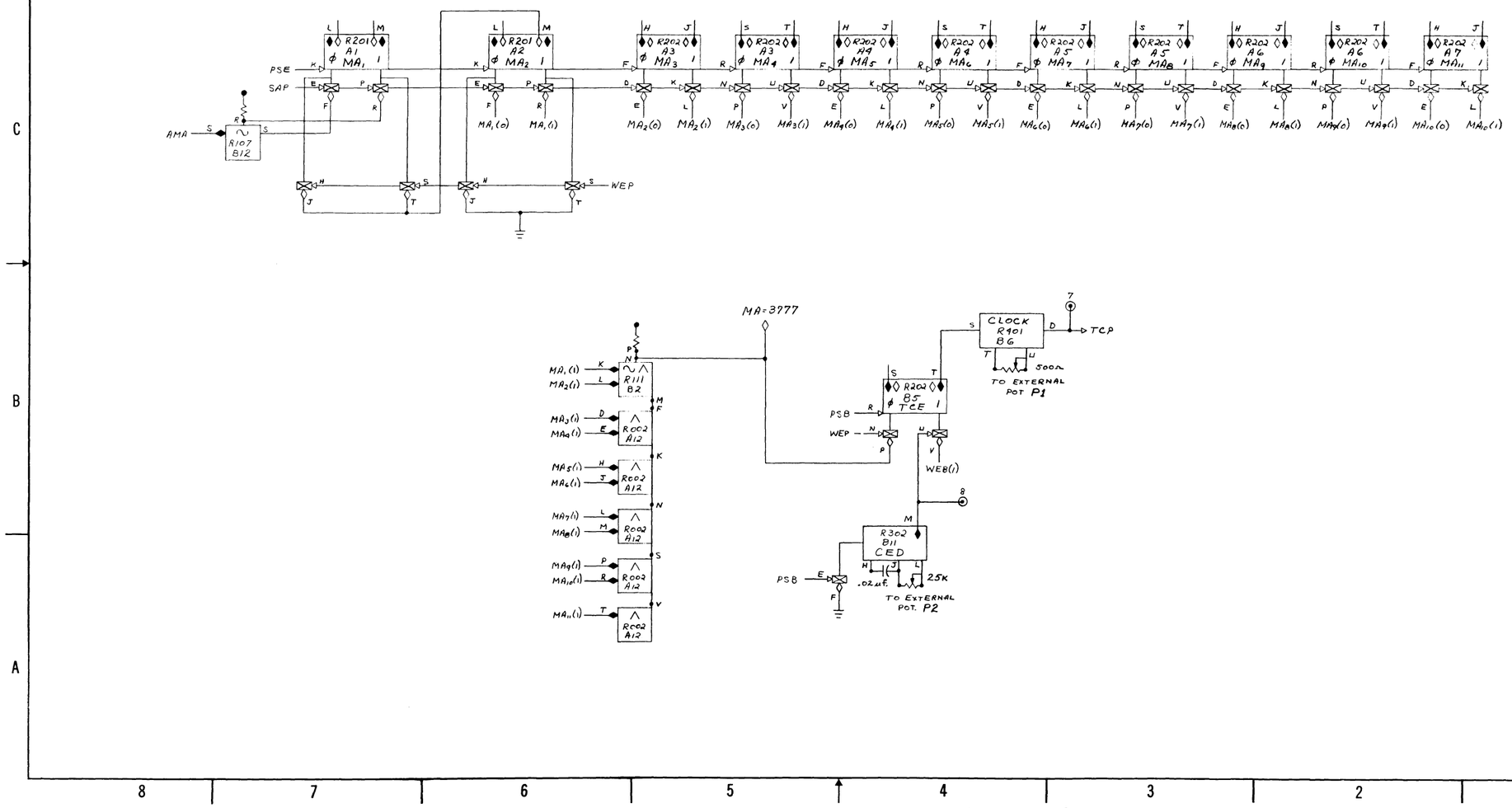


D-BS-DS32-0-1 Disk Expander

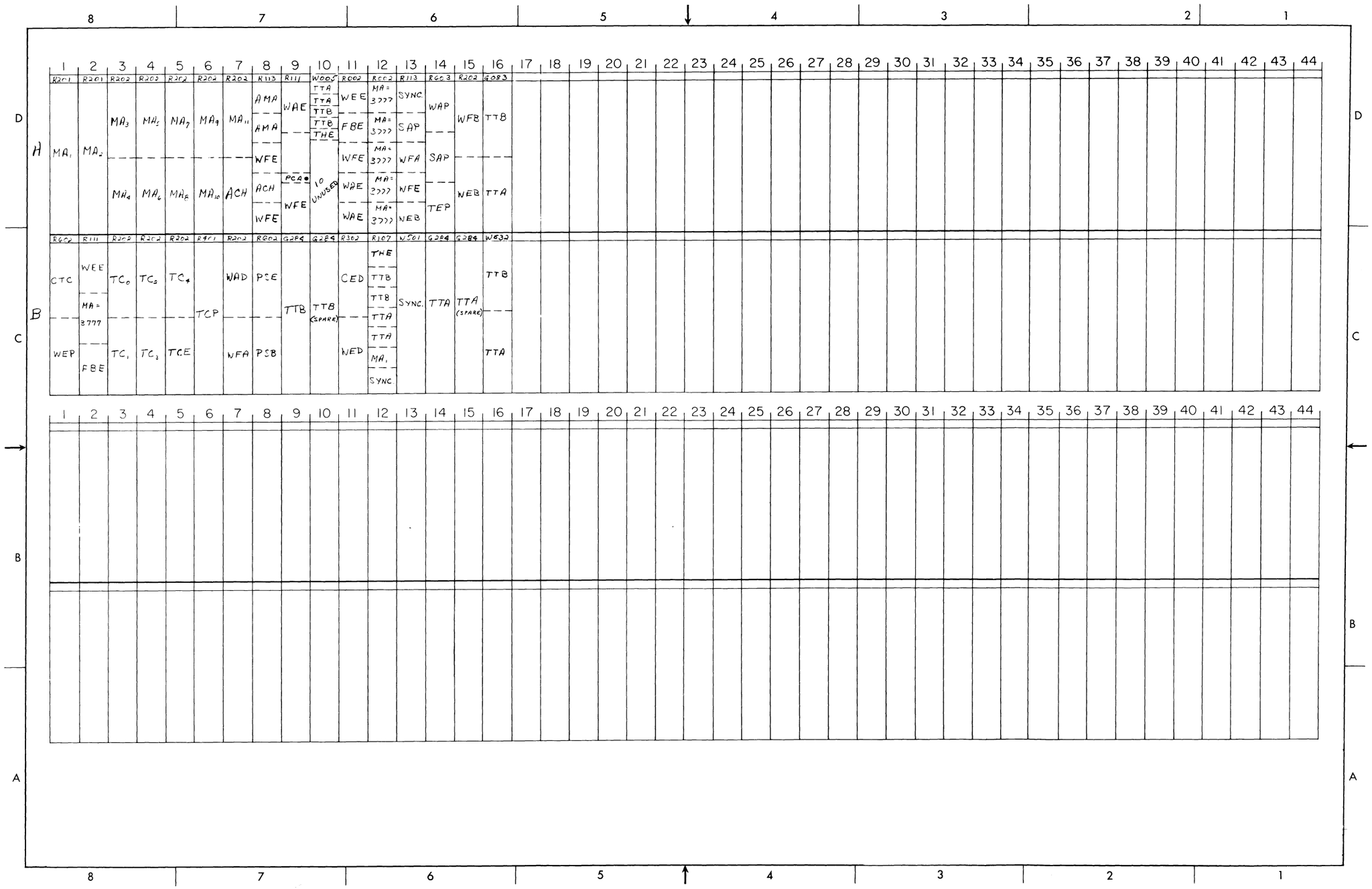

WQ318 WQ318 WQ318 WQ33A GQ83 WS33 RG02 R302
TTA1 X0 EM0 PCA1
TTB1 X1 EM1
TBD(1) X2 EM2
DMP1 X3 EM3 GQ85 & GQ86 OUTPUTS
WTE X4 BEMA3
WFF(1) X5 DSP1
NNEX1 X6 WLO
NPSM1 X7 EWL
TID GRD
DMP1 DMP1 DMP1 DSP1
DSP1
RG02 WS33 WS30 WQ33A
TTA1 TTB1 TTB1 TTB1
TTB1 TTA1 TTA1 TTA1
WQ318 WQ318 WQ318 GQ35 GQ39 WS32 R107 R113
TTA1 X0 EM0
TTB1 X1 EM1
TBD(1) X2 EM2
DMP1 X3 EM3
WTE X4 BEMA3
WFF(1) X5 DSP1
NNEX1 X6 WLO
NPSM1 X7 EWL
TID GRD
SERIES SWITCH
WRITER
DMP1
TTB1 TTB1
WFF(1)
BEMA3 SEL1
PSM1 TBD(1)
PSM1 WIA1
NEX1
NEX1 WIB1
RG01 WQC2 GQ83 N623A
TTA1 TAS1
TTB1 TTB1
DMP1 DMP1 TTB1 TTB1
DSP1 PCA1
TID
TBD(1)
TTA1
TTB1
DMP1
DSP1 TTA1 TTA1
WFF(1)
WTE
EWL
EMA3(1)
1 open

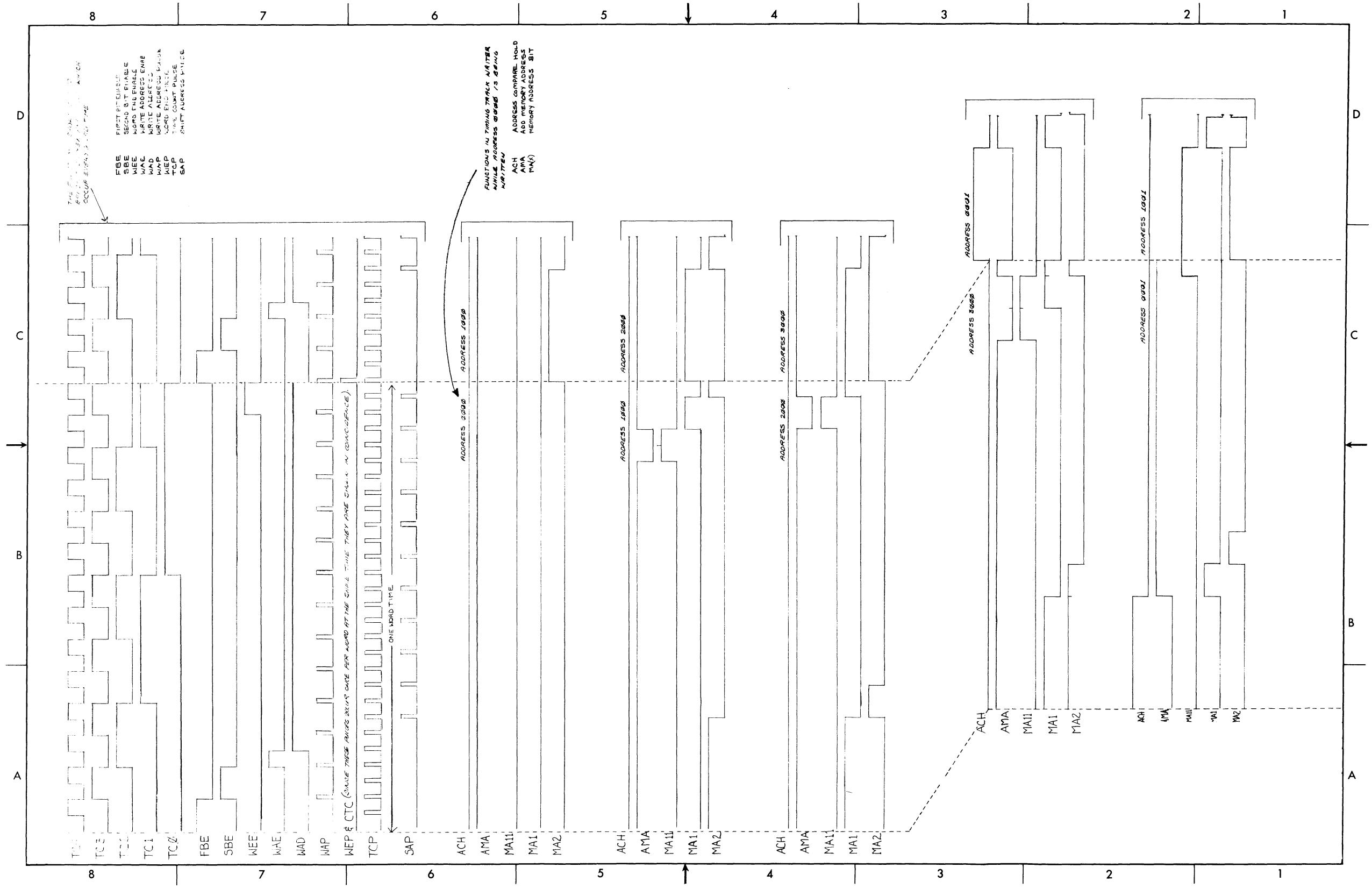


D-BS-TW32-0-1 Timing Track Writer (Sheet 1)

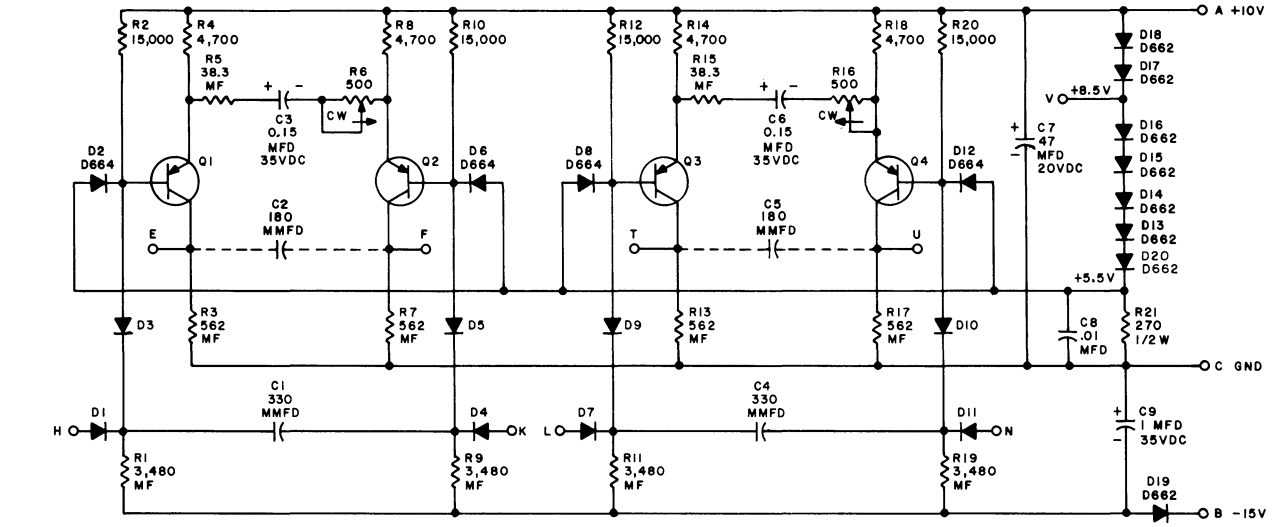


D-BS-TW32-0-1 Timing Track Writer (Sheet 2)


8 7 6 5 4 3 2 1
D C B A
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44
R201 R201 R202 R203 R202 R202 R202 R113 R111 W005 R002 R002 R113 R603 R202 G083
MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10 MA11 ACH AMA AMA WFE WFE WAE PCA 10 UNUSED WEE WEE FBE WFE WAE SYNC. WAP SAP SAP TEP WFB WEB TTB TTA
R602 R111 R202 R202 R202 R401 R202 R602 G284 G284 R302 R107 W501 G284 G284 W632
CTC WEP WEE MA= 3777 FBE TC0 TC1 TC2 TC3 TC4 TCP TCE WAD WFA PSE PSB TTB TTB (SPARE) CED WED THE TTB TTB TTA TTA TTA MA1 SYNC. SYNC. TTA TTA (SPARE) TTB TTA

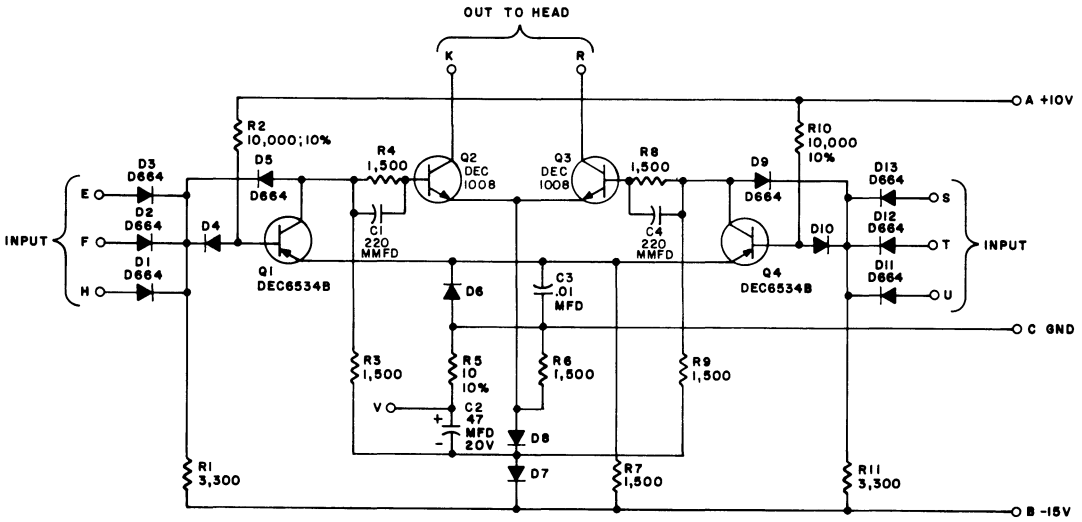


D-TD-TW32-0-3 Timing Track Writer Timing Diagram



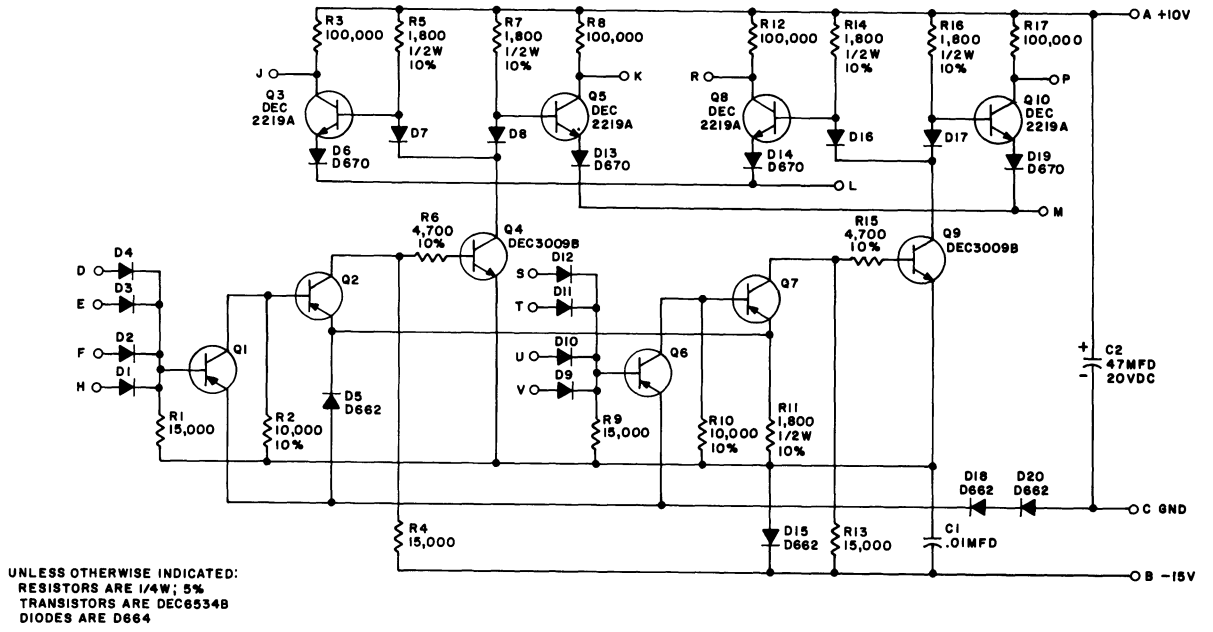
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC6534B
DIODES ARE D670
RESISTORS ARE 1/4W, 5%
MF RESISTORS ARE 1/8W, 1%
R6 & R16 ARE HELITRIM 79PR500 OR BOURNS 3012P-1-501
C2 & C5 ARE USED FOR PEAKING R/W
HEADS. NORMALLY NOT NECESSARY

B-CS-G083-0-1 Disk Preamplifier G083

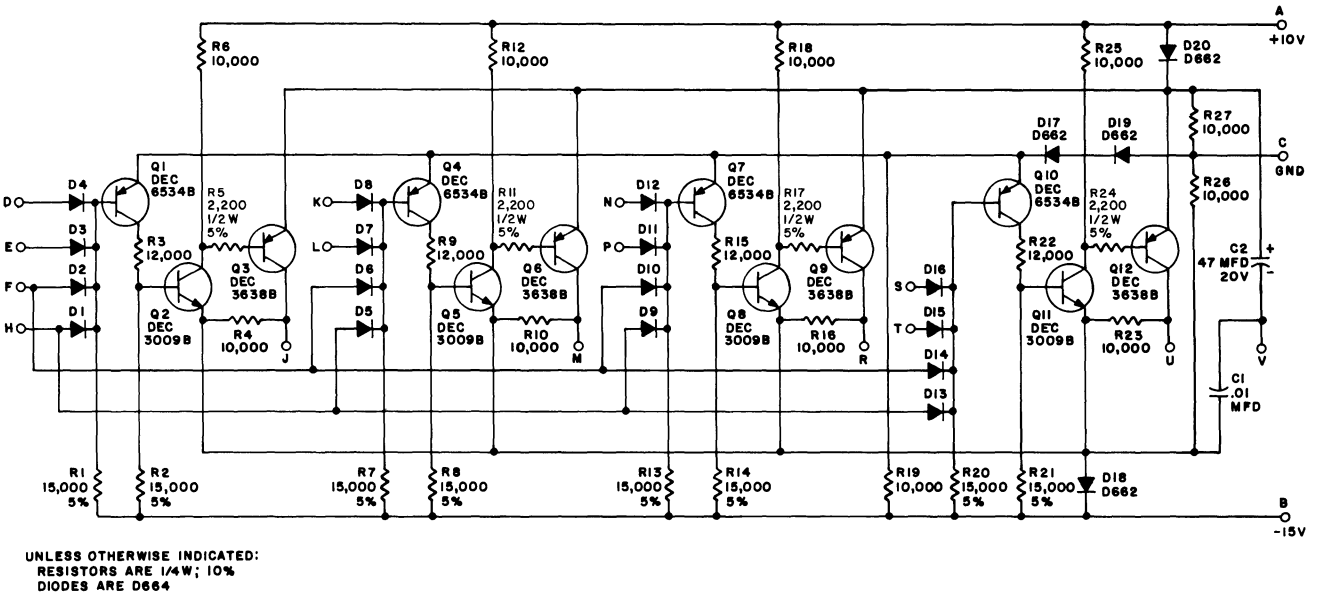


UNLESS OTHERWISE INDICATED:
DIODES ARE D662
RESISTORS ARE 1/4W; 5%

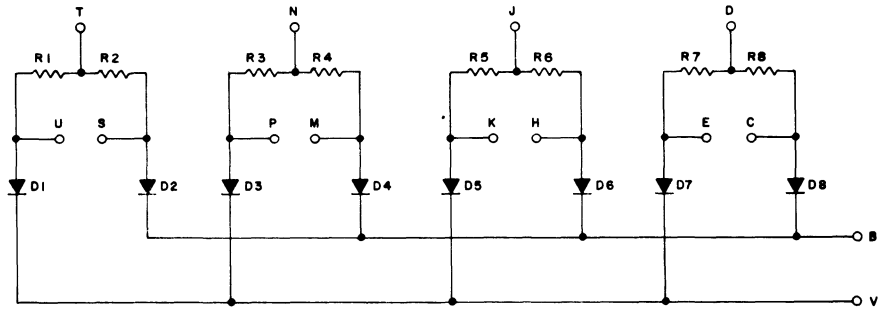
B-CS-G284-0-1 Disk Writer G284



B-CS-G285-0-1 Series Switch G285

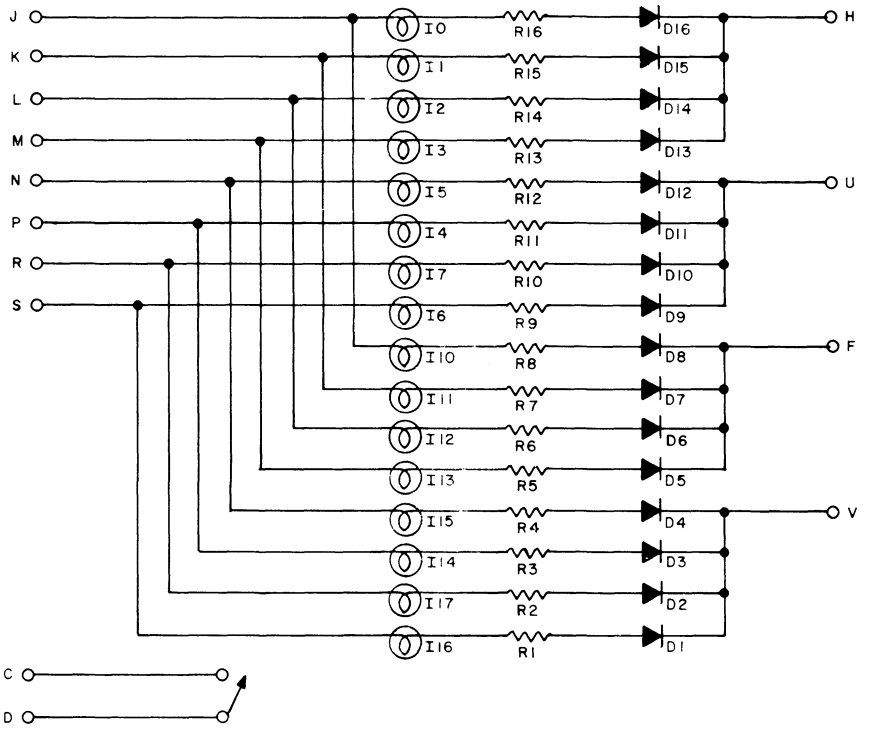


B-CS-G286-0-1 Center Tap Selector G286



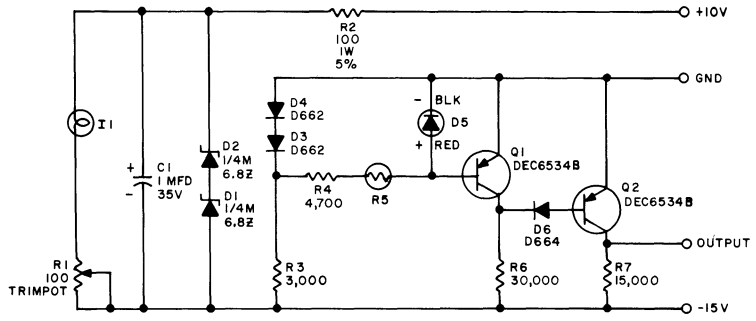
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 562, 1/8W, 1% MF 100 PPM
DIODES ARE D670

B-CS-G680-0-1 Disk Head and Matrix G680



UNLESS OTHERWISE INDICATED:
DIODES ARE D662
RESISTORS ARE 330, 1/2W, 5%
LAMPS ARE 12-2231, 18V

B-CS-G702-0-1 Disk Simulator G702



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
R5 IS A FENWAL THERMISTOR #KA31J1
D5 IS A HR1135
I1 IS A 18V LAMP

B-CS-5404073-0-1 Photo Cell Amplifier 5404073

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