ME11-L
core memory
system manual

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INTRODUCTION

The ME11-L Core Memory System is a Unibus-compatible PDP-11 family peripheral. Throughout this manual the ME11-L Memory System is referred to as the ME11-L and core memory is referred to as the memory. The ME11-L consists of a basic 8K MM11-L Read/Write Core Memory, a Power Supply, and a mounting box. The memory within the mounting box, powered by the Power Supply, is expandable in 8K (MM11-L) increments to 24K.

This manual provides the user with the theory of operation and maintenance information necessary to understand the ME11-L. The level of discussion assumes that the user is familiar with basic digital computer theory and basic PDP-11 use.

Signals and data are transferred between the ME11-L and the PDP-11 Unibus; however, this manual does not describe the operation of the Unibus. A detailed description of the Unibus is found in the *PDP-11 Peripherals and Interfacing Handbook.*

Engineering drawings are referenced by drawing number and may be found in the *ME11-L Engineering Drawing Manual.*

This manual is divided into three chapters. Chapter 1 provides a functional description, a physical description, ME11-L specifications, and installation information. Chapter 2 contains the general description, detailed description, and maintenance information regarding the Power Supply of the ME11-L. Chapter 3 provides a general description, a detailed description, and maintenance information regarding the 8K MM11-L Memory used in the ME11-L. Appendix A contains integrated circuit (IC) descriptions for the ICs used in the ME11-L.

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The ME11-L is a 900-ns memory system for the PDP-11 computer family. The basic system consists of an 8K, 16-bit, read/write memory contained in its own mounting box with a Power Supply. The memory may be expanded in 8K (MM11-L) increments to 24K. All the necessary cables are included with the rack-mountable 5-1/4 X 19 inch mounting box. By containing its own power supply, the memory unit saves up to 8.1A of power in the processor box.

1.2 FUNCTIONAL DESCRIPTION

Figure 1-1 shows the functional block diagram of the ME11-L unit. The additional memories are the optional 8K increments to the basic ME11-L unit. Two configurations of the ME11-L are possible depending on the power source to the unit: ME11-LA is for a power source of 115 Vac, 60 Hz; and the ME11-LB is for a power source of 230 Vac, 50 Hz. The additional 8K memory increments, optional for the ME11-L, are designated as the MM11-L Memory. The functional units of the ME11-L are the Unibus, the memory, the Power Supply, and the mounting box.

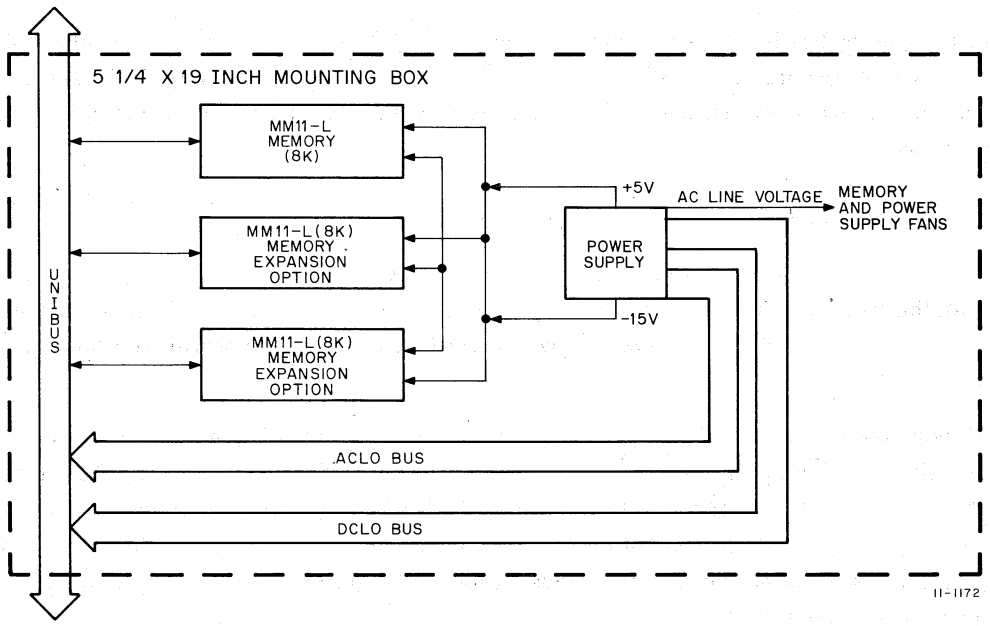


Figure 1-1 ME11-L Functional Block Diagram

1.2.1 Unibus

The Unibus is an asynchronous, single high-speed bus. All PDP-11 components and peripherals communicate through the Unibus on its bi-directional lines. Like all PDP-11 peripherals, the ME11-L has its own bus addresses which are the memory location addresses. Communications via the Unibus do not require timing pulses; therefore, DEC-designed memories of various speeds can be combined in the same PDP-11 System. Because all peripherals share the Unibus, the system includes direct memory accessing (DMA) which is implemented through non-processor requests (NPRs). Data rate on the Unibus is 40 megabits per second or 2.5 million words per second with a cycle of 400 ns. For detailed information regarding the Unibus, refer to the *PDP-11 Peripherals and Interfacing Handbook.*

1.2.2 Memory

The basic 8K memory unit for the ME11-L is the MM11-L, a 16-bit read/write core-type memory. It provides 8192 (8K) 16-bit words that are word and byte addressable. Unibus address lines 14 through 17 are the ME11-L device portion of the address. This portion of the address is assigned to the ME11-L according to its use in the system. The remaining portion of the address (address lines 0 through 13) refers to the specific memory location. The memory consists of three modules: the G110 Hex Module contains the memory control logic; the G231 Hex Module contains the memory driver logic; and the H214 Quad Module is the memory core stack. The G231 is located between the G110 and the H214. See Chapter 3 for more detailed information on the memory. Paragraph 1.3 describes the memory modules in their ME11-L configuration.

1.2.3 Power Supply

The Power Supply for the ME11-L supplies four outputs to the unit. These outputs are: +5V which provides the memory logic levels; −15V which supplies the memory drive circuits; and BUS AC LO and BUS DC LO which provide the power fail signals to the Unibus. The Power Supply is discussed in detail in Chapter 2.

1.2.4 Mounting Box

The ME11-L mounting box is a 5-1/4 inch high, 19 inch wide, by 20 inch deep cabinet. It contains all the cabling necessary to interface the units of the ME11-L and provide power. It also provides for the Unibus connection and contains the backplane for interconnection of the memory modules. Details of the mounting box are discussed in Paragraph 1.3.

1.3 PHYSICAL DESCRIPTION

The ME11-L Memory System is shipped in the ME11-L mounting box shown in Figure 1-2. Through the use of photographs, this paragraph describes the ME11-L components and their location in the mounting box. Engineering drawings in the *ME11-L Engineering Drawing Manual* are referenced to provide additional physical information.

Figure 1-3 shows the rear of the ME11-L mounting box. The Power Supply is behind the vents on the left side of the box. All connections to the ME11-L unit are made at the rear of the mounting box. Power is supplied through the line cord to the Power Control unit (115 or 230 Vac). The Unibus enters and is secured to the ME11-L on the right side of the top rear of the mounting box. The reset button resets the Power Control circuit breaker, which opens when the line current exceeds 7A for the 115-Vac Power Control option or 4A for the 230-Vac Power Control option.

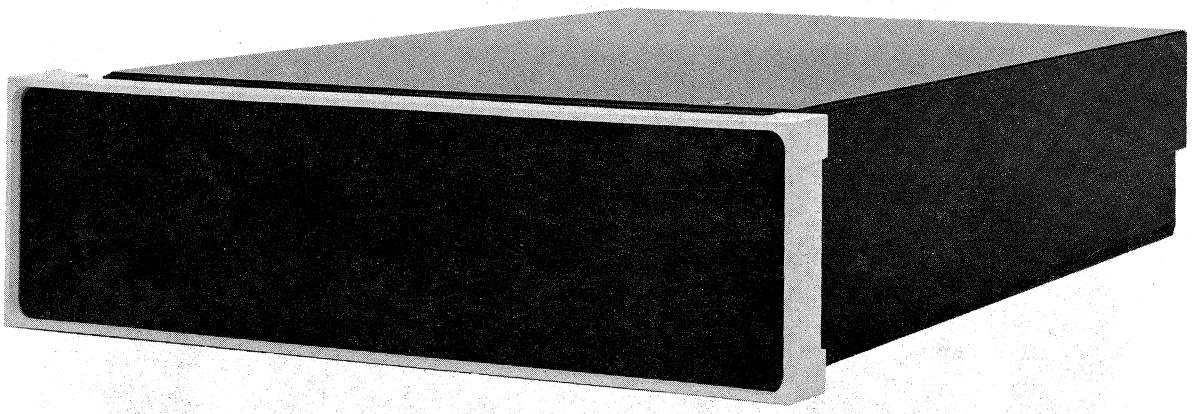


Figure 1-2 ME11-L Mounting Box

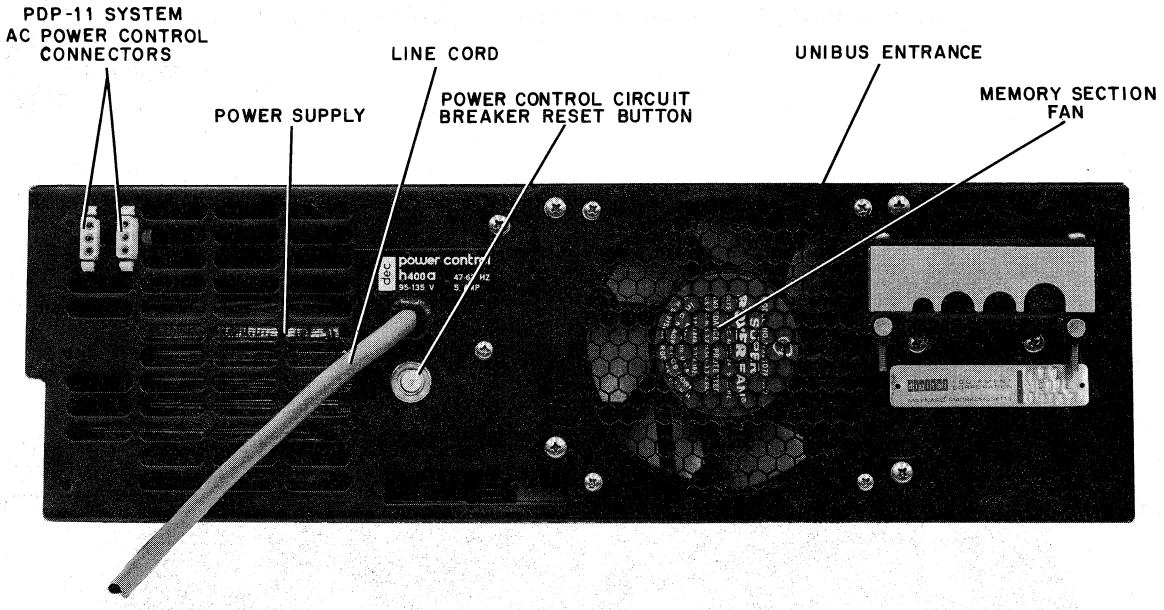


Figure 1-3 Rear View of ME11-L

Figure 1-4 shows the memory side of the mounting box without any modules plugged into the module slots. When looking at the front of the unit, the memory side is on the left. The backplane divides the memory section of the unit from the Power Supply. The module slots of the backplane unit and the module guides secure the modules in the unit. Figure 1-5 shows the memory section again, but with modules for a basic 8K (MM11-L) of memory plugged into the unit. (Refer to engineering drawing D-MU-ME11-L-01 for module utilization information.)

Figure 1-6 shows the Power Supply section of the ME11-L mounting box. This includes the Power Supply fan at the front of the unit, the DC Regulator Module, and the Power Control Mate-N-Lok output connector. (Refer to engineering drawing E-IA-5409728-0-0 for DC Regulator Module assembly information. The wiring side of

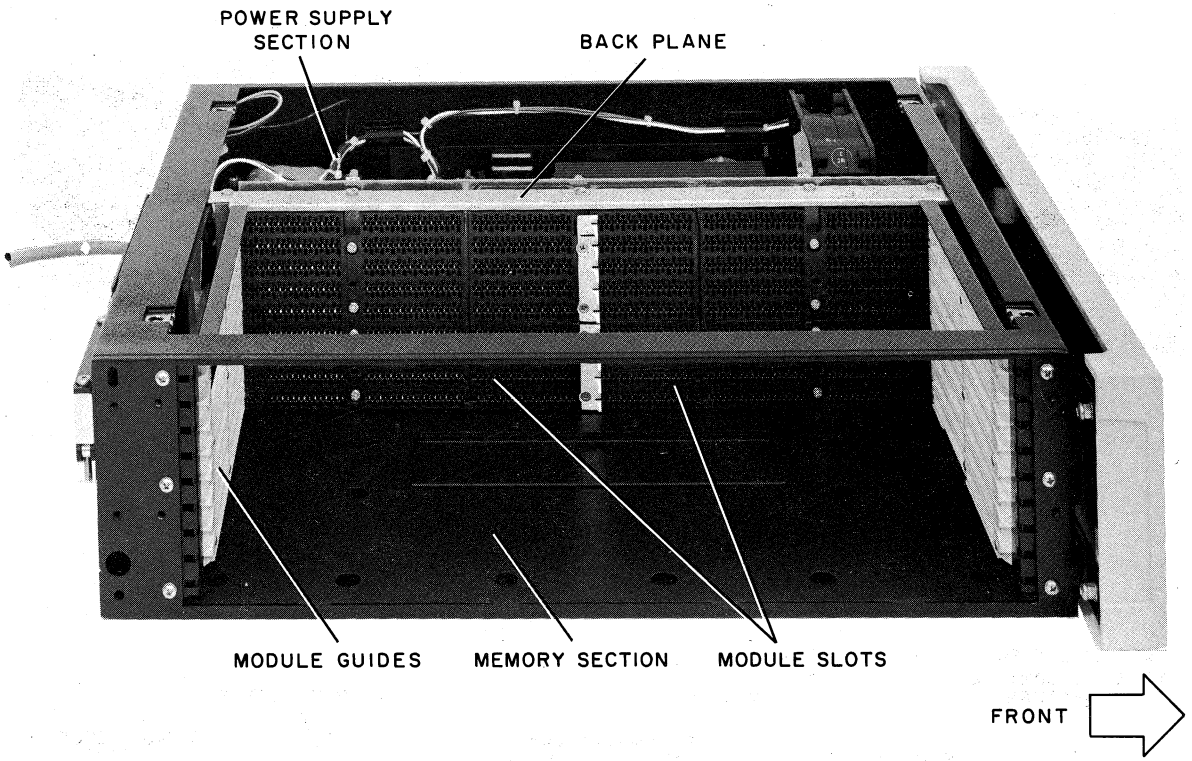


Figure 1-4 ME11-L without Memory Modules

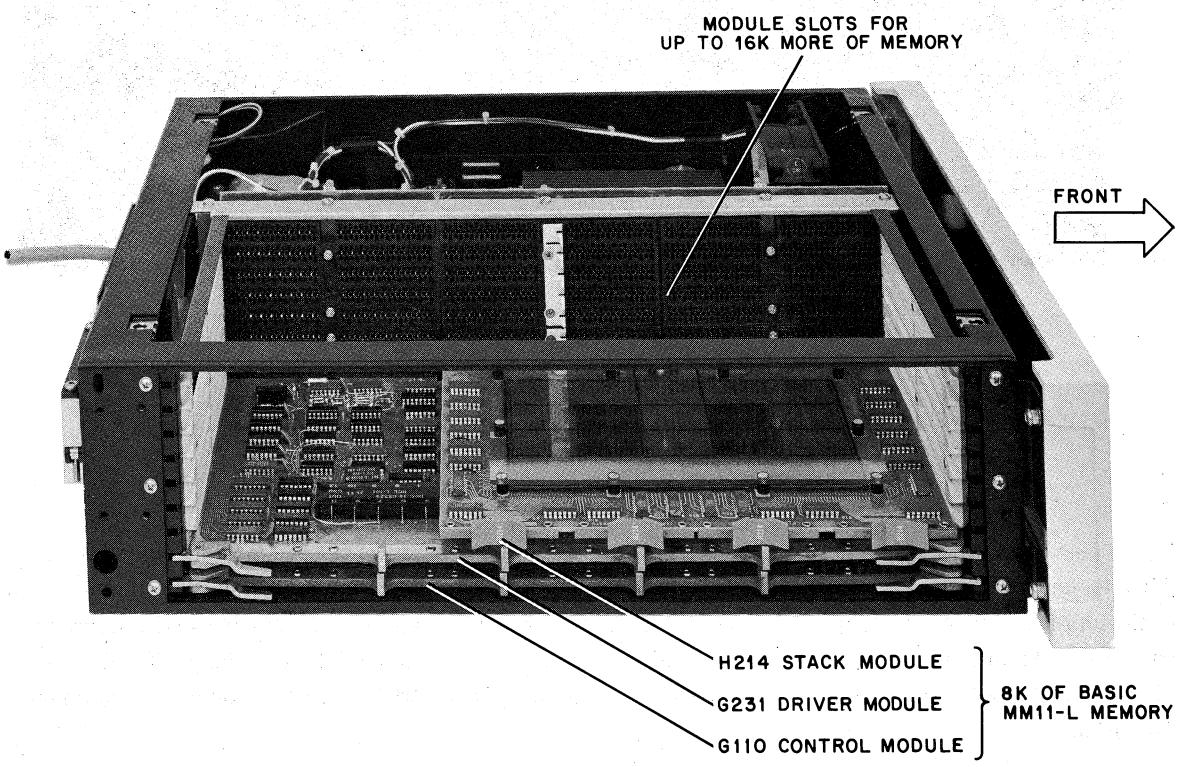


Figure 1-5 Memory Section ME11-L

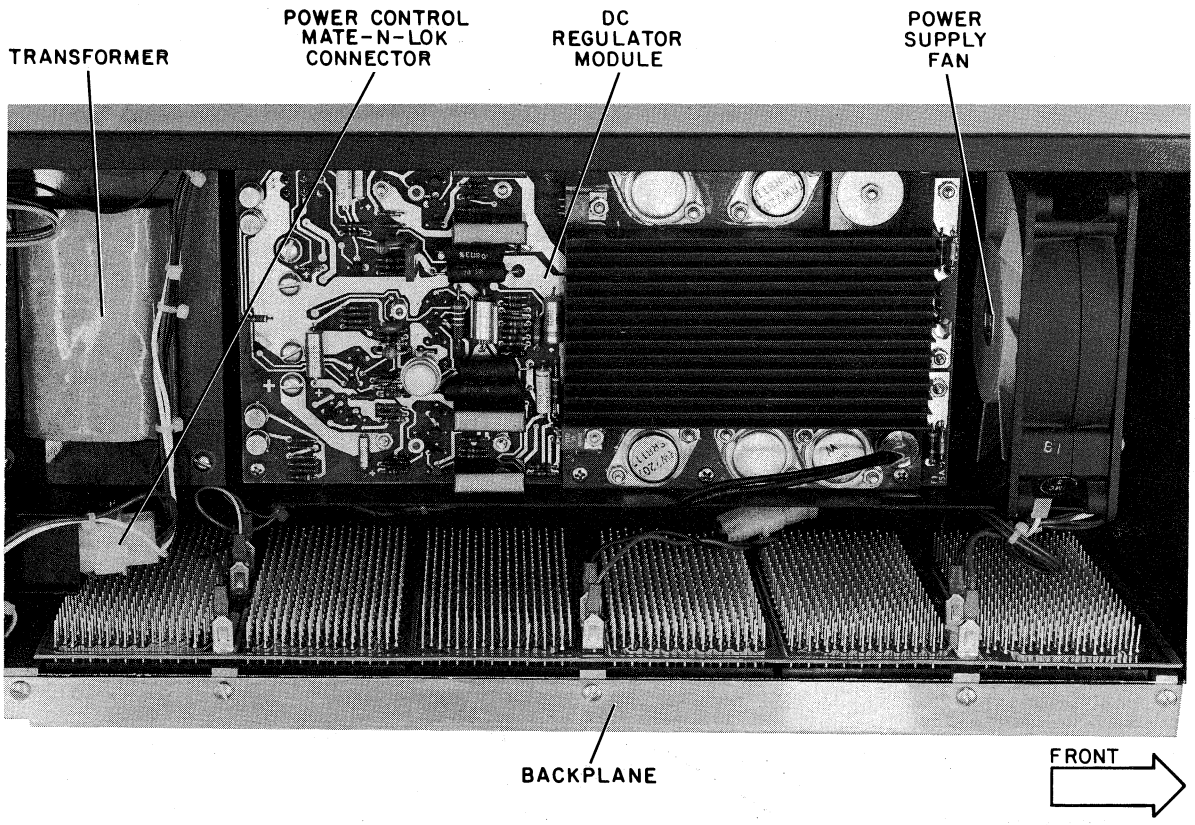


Figure 1-6 Power Supply Section of ME11-L

the backplane and the Power Supply connections to the backplane are also shown in Figure 1-6. The ME11-L unit is shown on engineering drawing D-UA-ME11-L-0 (2 sheets).

1.4 ME11-L SPECIFICATIONS

The basic specifications for the ME11-L as a unit are listed in Table 1-1. Detailed specifications for the Power Supply and the memory are provided in Paragraphs 2.2.2, and Table 3-1.

1.5 INSTALLATION

The ME11-L is shipped, ready to operate, in the protective carton shown in Figure 1-7. There are no special shipping mounts internal to the carton. Additional hardware is included, however, to rack mount the ME11-L mounting box.

Prior to final electrical testing, each ME11-L is thermal cycled, vibrated, and subjected to mechanical shock with all modules in place.

The 5-1/2 by 19 inch by 20 inch ME11-L mounting box includes rack mountable slides. The removable top

Table 1-1
ME11-L Basic Specifications

Specifications	Description
Cycle Time	900 ns
Power	350W
Voltage	115/230V
Temperature	32 to 122°F (0 to 50°C)
Dimensions	5-1/4 in. (13.3 cm) high 19 in. (48.3 cm) wide 20 in. (50.8 cm) deep
Weight	45 lb (20.6 kg)

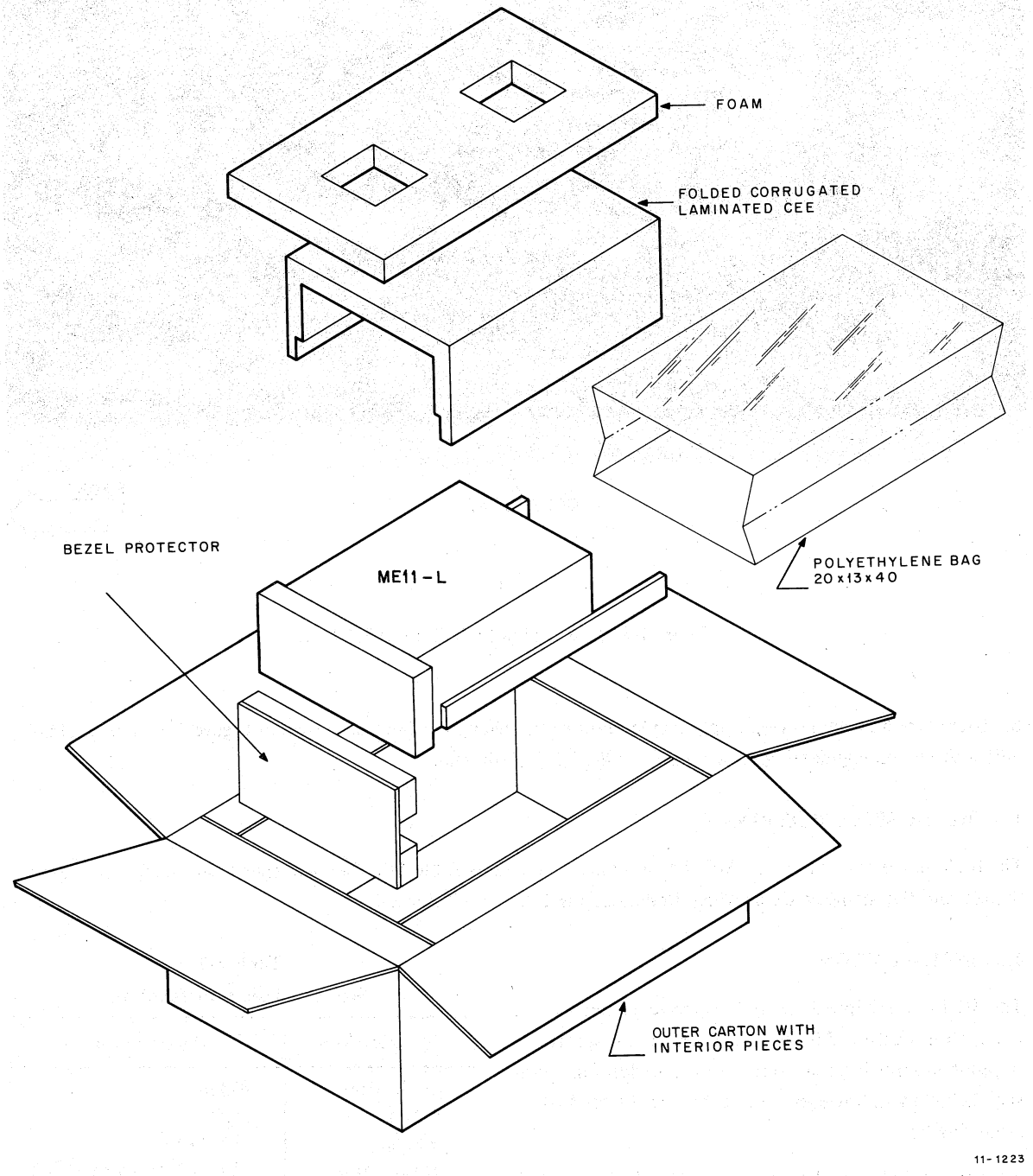


Figure 1-7 ME11-L Shipping Carton

cover of the mounting box is fastened by four Cam-Loc screws. The removable side panel is fastened by four Phillips Head screws.

The ME11-L is designed to be mounted in a standard 19 inch wide by 20 inch deep equipment bay. The ME11-L is mounted on slides for easy service. To mount the unit it is first necessary to attach the fixed portion of the slides to the cabinet. The fixed portion of the slides can be removed from the ME11-L by actuating the slide release which is located toward the rear of the mounting box, when the slides are fully extended. Be sure to mount the slides such that the fixed guides are parallel and level with the ground.

1.5.1 Mounting the Computer on Installed Slides

Once the slide guides have been securely fastened in the cabinet using all eight screws, lift the ME11-L and slide it carefully on to the slide guides until the slide release locks. Carefully lift the slide release and push the ME11-L fully into the rack, being careful not to tear any existing cabling.

The ME11-L should then be fully extended until the slide release locks. The covers on the top and side of the ME11-L should be removed to permit installation of the Unibus. The covers are removed by loosening four Cam-Loc and Phillips Head screws, respectively.

1.5.2 Installation of Side and Top Cover

Attached to the side cover is the continuation of the left-hand slide. All four 8-32 screws that hold the cover in place should be inserted and tightened securely. The top cover can now be installed using the four Cam-Loc screws.

1.5.3 Connection of the AC Power Supply

The ME11-L is designed for use on 115-Vac circuits in the United States and is equipped with a 3-pronged connector. This connector, when inserted into a properly wired 115-Vac outlet, grounds the mounting box. It is dangerous to operate the ME11-L unless the mounting box is grounded because normal leakage current from the Power Supply flows into metal parts of the chassis.

If there is any question about the integrity of the ground circuit, the user is advised to measure the potential between the ME11-L mounting box and a known ground with an ac voltmeter.

1.5.4 Instructions for Connection to Other Than 115V

The ME11-L operates at voltages ranging from 95V to 135V and from 190V to 270V 47 Hz–63 Hz, providing the proper power control is connected. The unit is ordered for nominal voltages of 115 or 230. The standard 3-pronged connector for 115V is identical with that found on most household appliances. A different 3-pronged connector is used for 230V.

On installations outside of the United States or where the National Electrical Code does not govern building wiring, the user is advised to proceed with caution.

1.5.5 Quality of AC Power Source

The ME11-L is a complex electronic device. Computer systems consisting of a processor, memory, and peripherals are often sensitive to interference present on some ac power lines. If a computer system is to be installed in

an electrically "noisy" environment, it may be necessary to condition the ac power line. DEC Field Service engineers can assist in determining if the ac line is satisfactory.

1.5.6 ME11-L Power Control

The ME11-L contains two standard 3-pin connectors used for ac power control in PDP-11 Systems. These connectors are not used in the ME11-L. They do not affect the power in the ME11-L mounting box, nor does the status of the power in the ME11-L affect the power bus. The ME11-L must be plugged into a source of switched ac power in order for its power to rise and fall with the rest of the system.

1.5.7 Installing the Unibus Cable

The wide BC11A Unibus Cable should be folded as shown in Figure 1-8 and routed over and through the clamp attached to the top of the fan. Note that there is a guide extending over the fan from the rear of the mounting box that prevents the Unibus cable from blocking the air flow of the ME11-L.

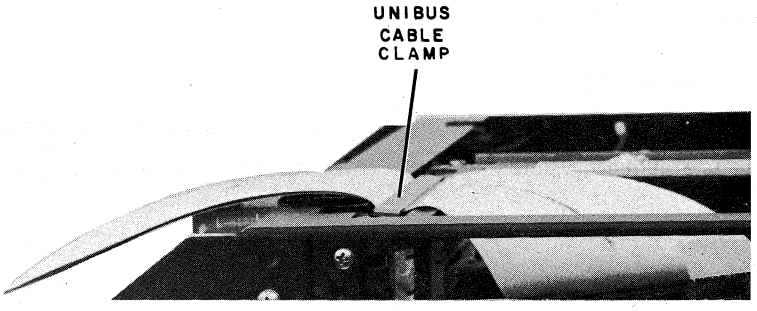


Figure 1-8 Unibus Cable Connection

CHAPTER 2
POWER SUPPLY

2.1 INTRODUCTION

This chapter is divided into three sections: general description, detailed description, and maintenance. The general description section provides a functional description, physical description, and specifications for the Power Supply unit. The detailed description section provides a circuit level description of the AC Input Circuit and the DC Regulator Module of the Power Supply. Finally, the maintenance section provides information necessary for troubleshooting the Power Supply and for parts identification.

2.2 GENERAL DESCRIPTION

The Power Supply is a forced-air-cooled unit which converts single phase 115V or 230V nominal 47 to 63 Hz line voltage to the two regulated output voltages required by the memories. The output voltages and their principal uses and characteristics are: +5V for IC logic (switching regulated, overvoltage and overcurrent protected), and -15V for core memory (switching regulated, overvoltage and overcurrent protected).

The supply is used in conjunction with two Power Control Assemblies which contain a line cord, circuit breaker, and RFI capacitors.

The power circuitry also generates BUS AC LO L and DC LO L power fail early warning signals.

A thermal control mounted on the heat sink will interrupt the ac input should the heat sink temperature become excessive due to fan failure or other cause.

2.2.1 Physical Description

The Power Supply comprises three major subassemblies and two cables: the Power Control, Power Chassis Assembly, DC Regulator Module, DC Cable, and AC Cable.

2.2.1.1 **Power Control Unit** – The Power Control Unit (drawing H400-0-0) is mounted on the rear of the computer by two screws. It contains a line cord, circuit breaker, RFI capacitors, 115V or 230V connections for the Power Supply transformer and a 6-socket Mate-N-Lok output connector. Physically, it consists of a sheet-metal bracket and a slide-on cover which is locked in place by one screw. A single-pole thermal breaker and a line cord strain relief grommet are mounted on the flange of the bracket making the line cord and breaker reset button accessible on the rear of the computer.

A small printed circuit (PC) card is mounted directly to the breaker terminals. This card interconnects and mounts the RFI dual-disc ceramic capacitor, the Mate-N-Lok output connector, and three fast-tabs for ac input and ground connections. A dual fast-tab is connected directly to the bracket. The black and white line cord wires are connected via fast-tab to the PC card; the green (ground) line cord wire is connected to the dual fast-tab, which in turn is connected to the third fast-tab on the PC card.

The 115V and 230V models differ in only two respects: breaker current rating and (printed circuit) jumpers for parallel or series connection of the Power Supply transformer primaries.

Power Control part numbers are: BC05HXX for the 115V, 7A assembly; and BC05JXX for the 230V, 4A assembly. Line cord length is variable and is denoted by XX; e.g., BC05H06 has a 6-foot line cord.

2.2.1.2 **Power Chassis Assembly** – The 7008731 Power Chassis Assembly (Figure 2-1) consists of a long inverted-U-shaped chassis, 7008726 power transformer, and a 5-inch fan. It is secured to the bottom of the ME11-L by four 8-32 X 3/8 inch Phillips Pan Head bolts.

The chassis is mounted to the right (when viewed from the front) of the connector blocks and airflow is from front to rear. The fan is held to one end of the chassis by two screws; the transformer may be removed by loosening four nuts that are accessible through large holes on the bottom of the chassis.

The DC Regulator Module is mounted to the chassis assembly by six screws and must be removed for cable access. The DC Cable enters a slot on the connector block side of the chassis; the AC Cable enters a slot on the other side.

Connections to the fan are made by small fast-tabs. Connections to the transformer are made via Mate-N-Lok connectors: 6-pin for primary, 3-socket for secondary.

2.2.1.3 **DC Regulator Module** – The 5409728 DC Regulator Module (Figure 2-2) is a printed circuit assembly that is mounted to the Power Chassis Assembly by four 6-32 X 9/16 inch and two 6-32 X 1/4 inch Phillips Pan Head screws. It contains all the circuitry between the transformer secondary winding and the Power Supply output cable.

ME11-Ls that were shipped during the first three or four months of production of the unit use a DC Regulator Module designated 5409728-YA-0; later shipments use a module designated 5409728-0-0, E revision. There are differences in component values on the two modules. The discussion of the DC Regulator Module circuits in this manual is directed to the later module, designated 5409728-0-0. Engineering drawings applicable to the module used are shipped with each equipment. These drawings provide schematics and component values of the DC Regulator Module used in a specific unit.

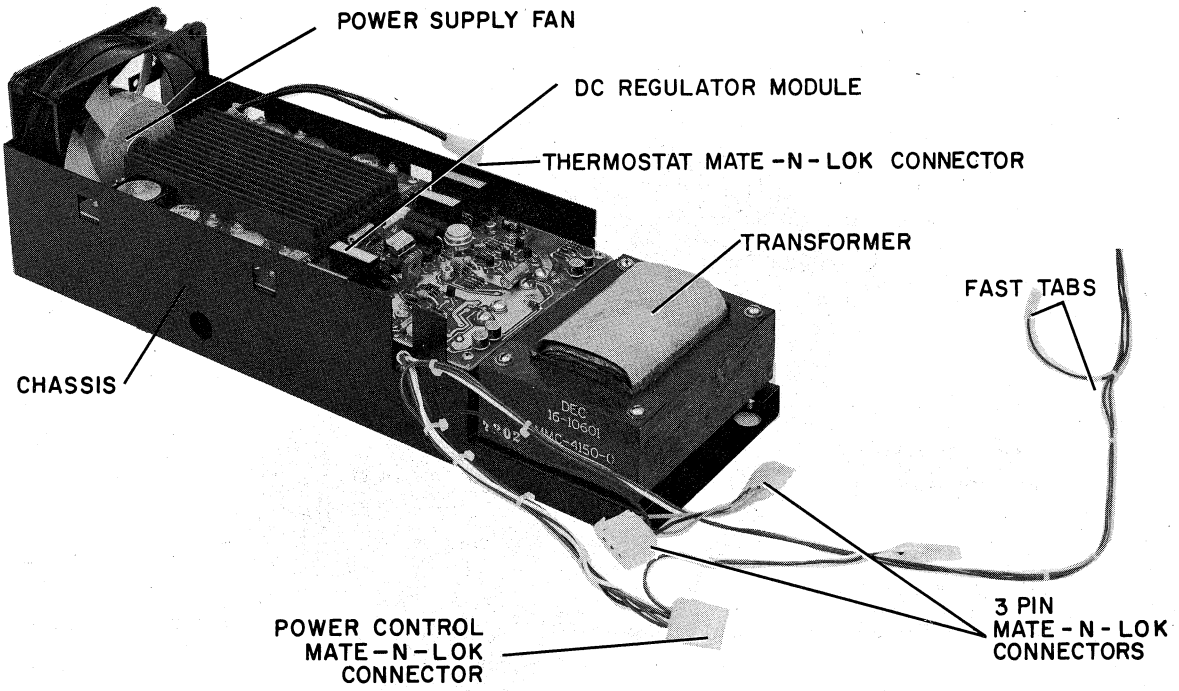
The transformer secondary 3-socket Mate-N-Lok connector is plugged into a mating connector which is soldered directly to the printed circuit board and is accessible underneath it. The 9-pin Mate-N-Lok connector on the dc output cable to the memory is similarly mated to a connector underneath the other end of the board.

The DC Regulator Module may be probed for troubleshooting purposes from the top; all points on the circuit are accessible. It may also be removed from the top for cable access and for parts replacement by removing the six mounting screws.

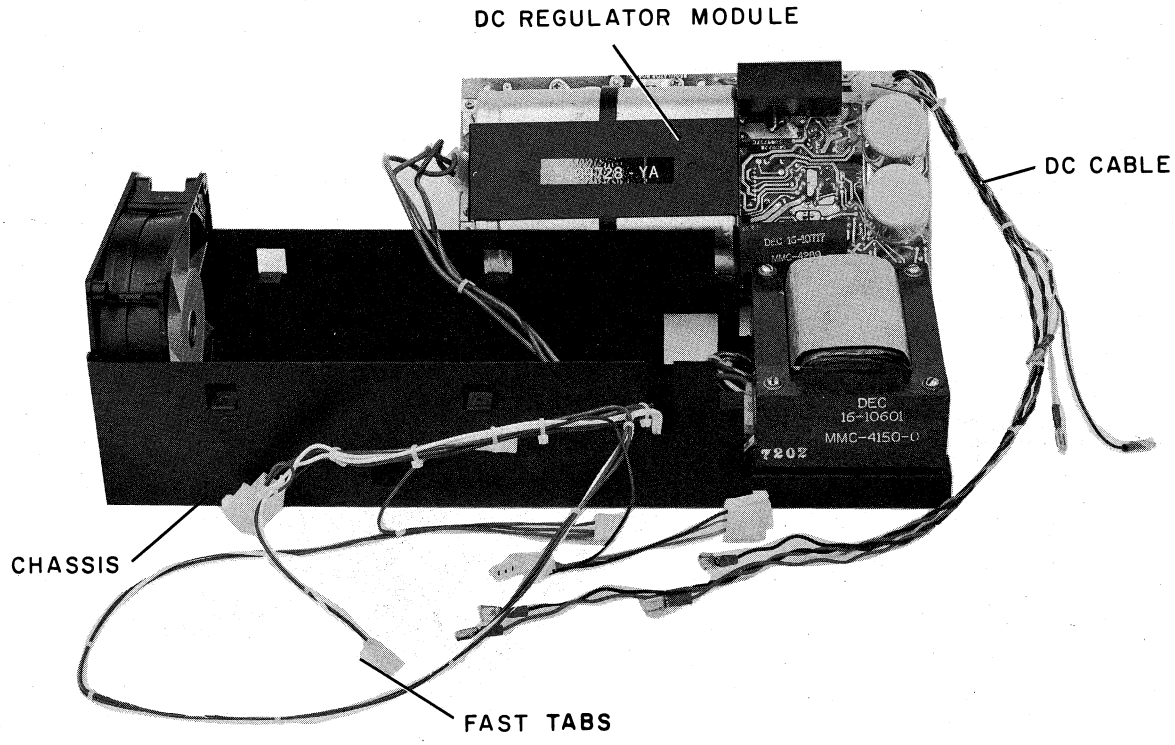
The printed circuit is approximately 5 X 10 inches, with about half of the top surface devoted to the heat sink. The power transistors and power rectifiers are bolted to two shelves on the sides of the heat sink and make contact with the circuit board directly underneath via solder and screw connections. The heat sink is hard anodized for electrical insulation.

The other half of the top surface is devoted to interconnecting and mounting the balance of the circuit. Three small output voltage adjustment potentiometers are accessible on this top portion of the board.

Two small Pico fuses are mounted on the top of the PC board on the fan end. These fast-acting fuses will typically only blow when some component is defective or when the +5 or –15 voltage is set too high.

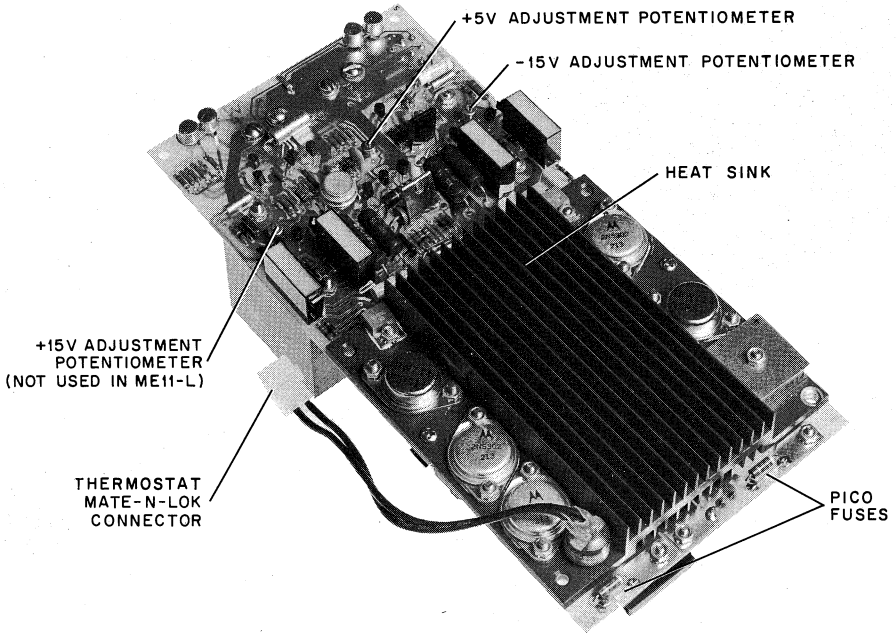


With DC Regulator Module

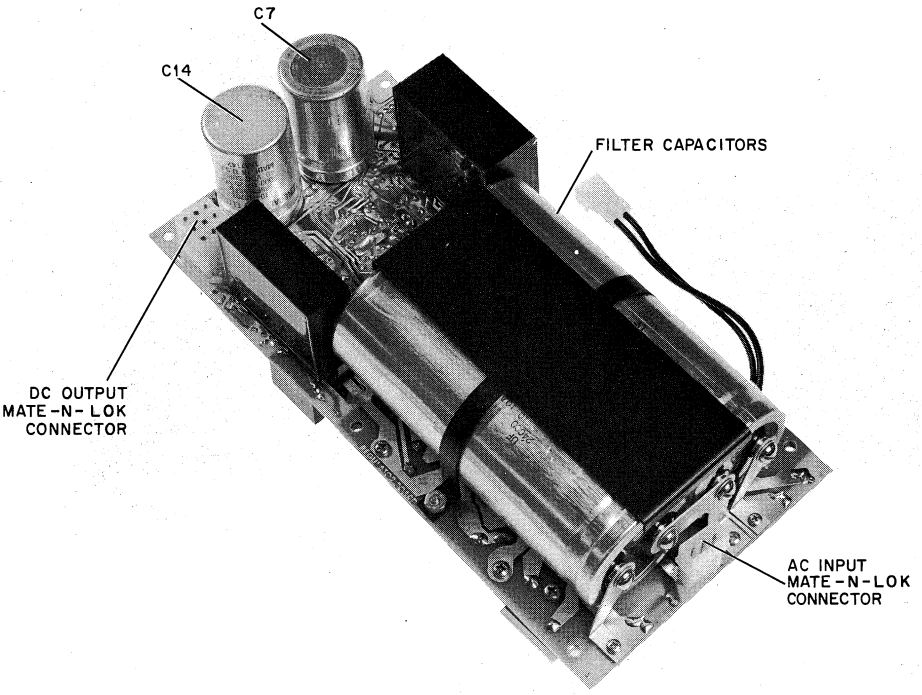


With DC Regulator Module Removed

Figure 2-1 Power Chassis Assembly



Top View



Bottom View

Figure 2-2 DC Regulator Module

The two input filter capacitors are held to the under side of the board by a bracket and are connected to the circuit via jumper tabs on the fan end.

The +5V and −15V output filter capacitors and inductors are also mounted under the board, the former by screws and the latter by nuts.

Care must be taken to ensure that all electrical and mechanical connections are made securely.

2.2.1.4 **DC Cable** – This is a simple cable connecting the backplane to the DC Regulator Module via a 9-pin Mate-N-Lok connector. The latter is made accessible by loosening the six mounting screws and lifting out the DC Regulator Module.

Cable access is through a slot on the module side of the power chassis.

2.2.1.5 **AC Cable** – This cable connects all ac portions of the ME11-L chassis, which are as follows:

a. Power supply Fan – two fast-tabs
b. Power Supply Thermostat – one 2-pin Mate-N-Lok
c. Memory Section Fan – two fast-tabs
d. Transformer Primary – one 6-socket Mate-N-Lok
e. Power Control – one 6-pin Mate-N-Lok
f. PDP-11 System AC Power Control – two 3-pin Mate-N-Lok connectors on rear of mounting box (not used).

The ac cable is located on the right-hand side and rear of the ME11-L mounting box and is inherently shielded by the Power Supply chassis, and the mounting box.

2.2.2 Specifications

Tables 2-1, 2-2, and 2-3 list all the Power Supply specifications according to input, output, and mechanical and environmental specifications.

Table 2-1
Power Supply Input Specifications

Parameters	Specifications
*Input Voltage (1 phase, 2 wires and ground)	95–135/190–270V
Input Frequency	47–63 Hz
Input Current	5/2.5A RMS
Input Power	325W at full load
Inrush	80/40A peak, 1 cycle
Rise Time of Output Voltages	30 ms max. at full load, low line
Input Overvoltage Transient	180/360V, 1 sec 360/720V, 1 ms
Storage After Line Failure	25 ms min., starting at low line, full load
Input Breaker (part of BC05 Power Control)	7A/4A single-pole, manually reset, thermal

*Input voltage selection, 115V or 230V, is made by specifying the appropriate AC Input Box, DEC Model BC05 (Paragraph 2.2.1.1). All specifications are with respect to the BC05 input.

(continued on next page)

Table 2-1 (Cont)
Power Supply Input Specifications

Parameter	Specification
Thermostat Mounted on Heat Sink (opens transformer and fan power)	277V 7.2A contacts Opens 98–105°C Automatically resets 56–69°C
Input Connections	Line cord on BC05 Power Control, length and plug type specified with BC05 (Paragraph 2.2.1.1)
Turn-On/Turn-Off	Application or removal of power
Hipot (input to chassis and output)	2.1 kV/dc, 60 sec

Table 2-2
Power Supply Output Specifications

Parameter	Specification
+5V	
Load Range	
Static	0–15A
Dynamic #1	±5A (within 0–17A load range)
Dynamic #2	No load – full load
Max. Bypass Capacitance in load for 30-ms turn-on	2000 μF
Overvoltage Crowbar (blows fuse)	5.7–6.8V actuate (7V abs. max. output)
Current Limit at 25°C	24–29.4A (–0.1A/°C)
Backup Fuse (series with raw dc)	15A
Adjustment Range	±5% min.
Regulation	
Line	±0.5%
Static Load	3%
Dynamic Load #1	±2%
Dynamic Load #2	±10%
Ripple and Noise	4% peak-to-peak
1000 Hour Drift	±0.25%
Temperature (0–60°)	±1%
–15V	
Load Range	
Static	0–7A
Dynamic #1	ΔI = 5A (0.5A/μs)
Dynamic #2	No load – full load (0.5A/μs)

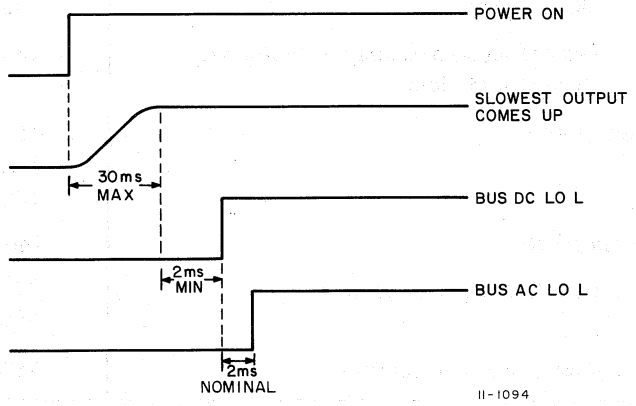
(continued on next page)

Table 2-2 (Cont)
Power Supply Output Specifications

Parameter	Specification
-15V (Cont)	
Max. Bypass Capacitance in load for 30-ms turn-on	1000 μF
Overvoltage Crowbar (blows fuse)	17.4–20.5V (22V abs. max. output)
Current Limit at 25°C	10–13.3A (–0.03 A/°C)
Backup Fuse (series with raw dc)	5A
Adjustment Range	±5% min.
Regulation	
Line and Static Load	±1%
Dynamic Load #1	±2.5%
Dynamic Load #2	±3%
Ripple and Noise	3% peak-to-peak
1000 Hour Drift	±0.25%
Temperature (0–60°C)	±1%
BUS DC LO L and BUS AC LO L	
Static Performance at Full Load (for 230V connection, double below voltages)	
BUS DC LO L goes to high	74–80 Vac line voltage
BUS AC LO L goes to high	8–11V higher
BUS AC LO L drops to low	80–86 Vac line voltage
BUS DC LO L drops to low	7–10V lower
Hysteresis (contained in above specifications)	3–4 Vac
Output voltages still good	70 Vac line voltage

Dynamic Performance

Worst case on power-up is high line, full load.



(continued on next page)

Table 2-2 (Cont)
Power Supply Output Specifications

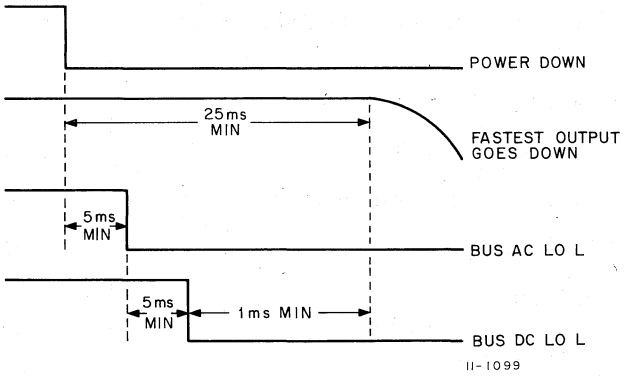
Parameter	Specification
BUS DC LO L and BUS AC LO L (Cont)	
Worst case on power-down is low line, full load.	
Output Characteristics	
Open Collector	50 mA sinking capability +0.4V max. offset
Pull-Up Voltage on Unibus	5V nominal, 180Ω impedance
Rise and Fall Times	1 μs max. Outputs shall remain in 0 state subsequent to power failure until power is restored despite Unibus pulling voltages remaining.

Table 2-3
Mechanical and Environmental Specifications

Parameter	Specification
Weight	
DC Regulator	7 lb approx.
Power Chassis Assembly including AC Regulator Module	18 lb approx.
Dimensions	16.50 in. length 5.19 in. width 3.25 in. height
Cooling Means	Integral 5 in. fan
Minimum Cooling Requirements	375 CFM through heat sink 250 CFM over caps, chokes, and transformer
Rated Heat Sink Temperature	95°C max.

(continued on next page)

Table 2-3 (Cont)
Mechanical and Environmental Specifications

Parameter	Specification
Shock, Non-Operating	40G (duration 30 ms) 1/2 sine in each of six orientations
Vibration, Non-Operating	1.89G RMS average, 8G peak; varying from 10 to 50 Hz, 8 dB/octave roll-off 50–200 Hz; each of six directions
Ambient Temperature	0 to +60°C operating -40 to +71°C storage
Relative Humidity	95% max. (without condensation)
Altitude	10K ft

Output parameters are specified at the pins of the 9-pin Mate-N-Lok connector (Figure 2-3) which plugs into the output connector on the 5409728 module. All output voltages are given with respect to the common ground pin on this connector. IR drops in the distribution wiring are minimized to achieve good regulation at the load. Recommended distribution loss is 3 percent maximum.

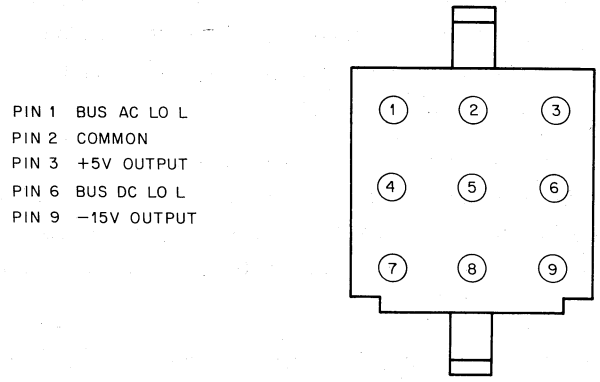


Figure 2-3 H740 Output Connector (5409728 Regulator Module)

2.3 DETAILED DESCRIPTION

The following paragraphs discuss the AC Input Circuit and the DC Regulator Module. A detailed circuit level description is provided. The AC Input Circuit description discusses the Power Supply interconnections, Power Control, transformer, Power Control circuit breaker, and the Power Supply thermostat. The DC Regulator Module description discusses the generation at the circuit level of each of the three Power Supply outputs.

2.3.1 AC Input Circuit

A detailed ac interconnection diagram is shown in Figure 2-4. Figures 2-5 and 2-6 illustrate the connections in schematic form.

The line cord, single-pole breaker, RFI capacitors, and connections for transformer 115V or 230V wiring are contained in the Power Control Unit. To select 115V input or 230V input, use the BC05H or BC05J Power Control, respectively.

The transformer is rated for 47 to 63 Hz and is equipped with two windings that are connected by the Power Control in parallel for 115V operation, and in series for 230V. The fans are connected across half of the primary so that they are always provided with 115V nominal. There is an electrostatic shield between primary and secondary of the transformers.

The Power Control Unit contains a single-pole thermal circuit breaker which protects against input overload and is reset by pressing a button on the rear of the computer.

The thermostat is mounted on the Power Supply heat sink. It will open one side of the primary circuit and de-energize the Power Supply if the heat sink temperature rises to about 100°C. It will automatically reset at about 63°C.

2.3.2 DC Regulator Module Operation

The discussion of the DC Regulator Module circuits in this manual is directed to the module designated 5409728-0-0, rather than the earlier module designated 5409728-YA-0. A block diagram of this module is shown in Figure 2-7. The center tapped output of the power transformer is applied to positive and negative rectifier and filter circuits. The rectifier circuits produce +28V and –28V nominal raw dc voltages which are unregulated but well filtered by the input storage capacitors.

The +28 Vdc is used by an efficient switching regulator circuit to produce the +5 Vdc output. Provisions for overcurrent detection are incorporated in the regulator circuit so that excess current is limited when there is a malfunction in the load. The +5V output is also protected against overvoltage by a crowbar circuit which limits the output to under 7V; before the output gets to this value, the crowbar circuit blows the fuse in the output circuit of the rectifier.

The –28 Vdc is used by the –15V circuit which is similar in operation to the +5V regulator circuit. The –15V crowbar circuit limits the output to 22V.

The BUS AC LO L and BUS DC LO L signals are used to warn the Unibus of imminent power failure. Circuits on the regulator module detect the transformer secondary voltage and generate two timed TTL-compatible open-collector signals that are used for power fail functions by devices on the Unibus. Note that this circuit does not detect the regulated dc output voltages as in some other PDP-11 processors and peripherals.

2.3.2.1 Generation of ± Raw DC – As stated in the previous paragraph the center-tapped transformer secondary voltage is rectified and filtered prior to being fed to the two DC Regulator Module circuits.

The circuitry involved is shown in Figure 2-8. The bridge rectifier D14 is mounted on the heat sink and the input capacitors C1 and C2 are mounted on the bottom of the regulator module. These capacitors filter the dc input and are large enough to provide at least 25-ms storage when the input power is short circuited or fails.

A fuse is used on each output to protect the regulator and load during faults. The fuses will not normally blow when a regulator output is shorted since the three outputs are electronically overcurrent protected. However the appropriate fuse will blow in the case of a +5V or –15V overvoltage crowbar or a failure in one of the over-current circuits.

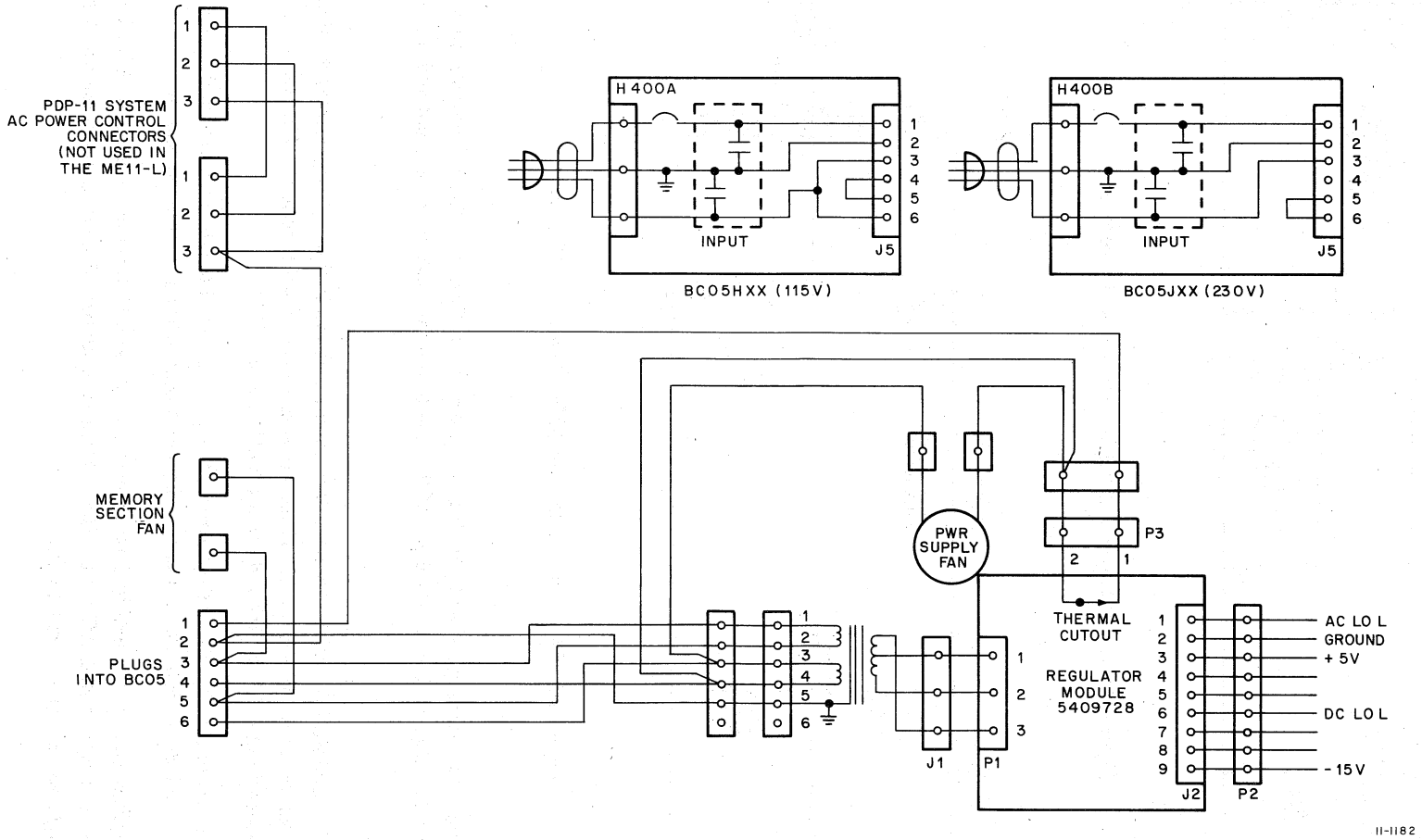


Figure 2-4 AC Interconnection Diagram

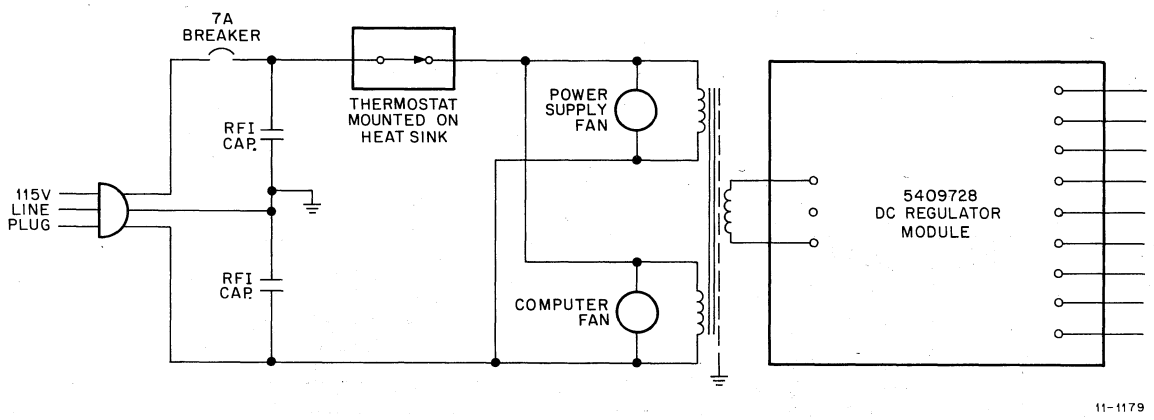


Figure 2-5 115V Connections, Simplified Schematic Diagram

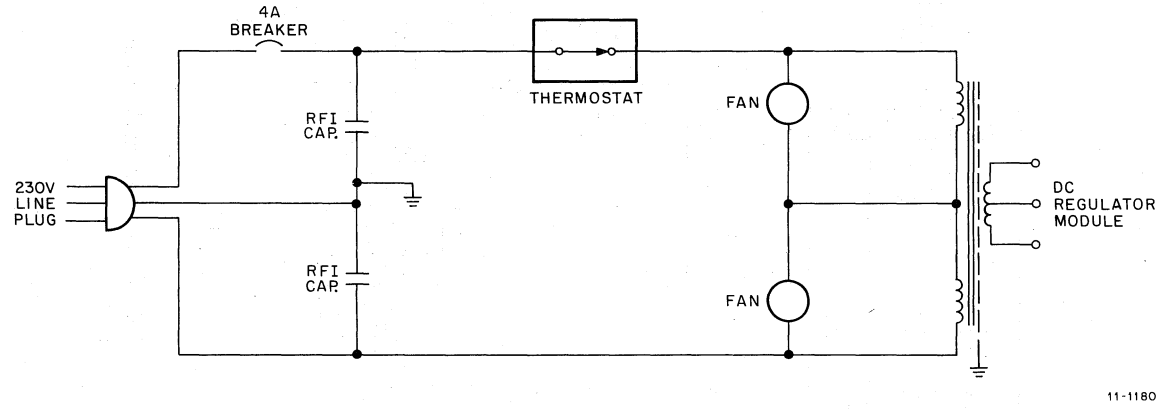


Figure 2-6 230V Connection, Simplified Schematic Diagram

The resistor across each fuse provides a slow (100–150 sec) discharge of C1 or C2 after the power is turned off, should a fuse blow. The capacitors are placed ahead of the fuse to limit the energy in any fault and thus better protect the outputs.

2.3.2.2 BUS AC LO L and BUS DC LO L Circuits – The circuitry shown in Figure 2-9 generates the timed Unibus power status signals described in Table 2-2. These are used for power fail functions. The transformer secondary voltage is rectified by D1 and D2 and filtered by C9 and R1, R14.

Circuit parameters are chosen so that the voltage across C9 will rise slower than the two regulated output voltages on power-up, and will decay faster than the two regulated output voltages on power-down.

Two differential amplifier circuits are used to detect power status: Q17, Q18 is used to generate BUS DC LO L; and Q15, Q16 is used to generate BUS AC LO L. The differential amplifiers share common reference Zener diode D3 which is fed approximately 1 mA by R3.

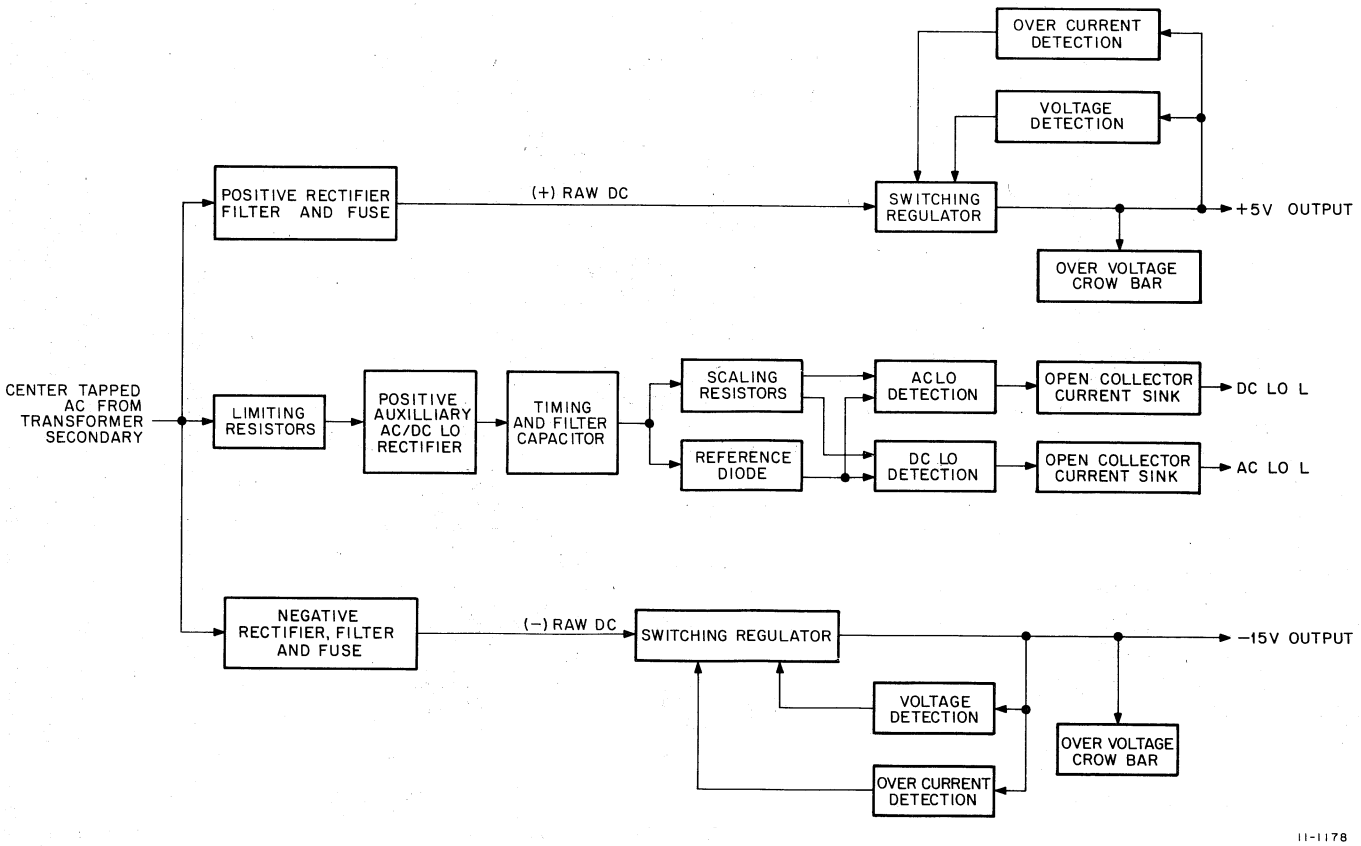


Figure 2-7 DC Regulator Module, Block Diagram

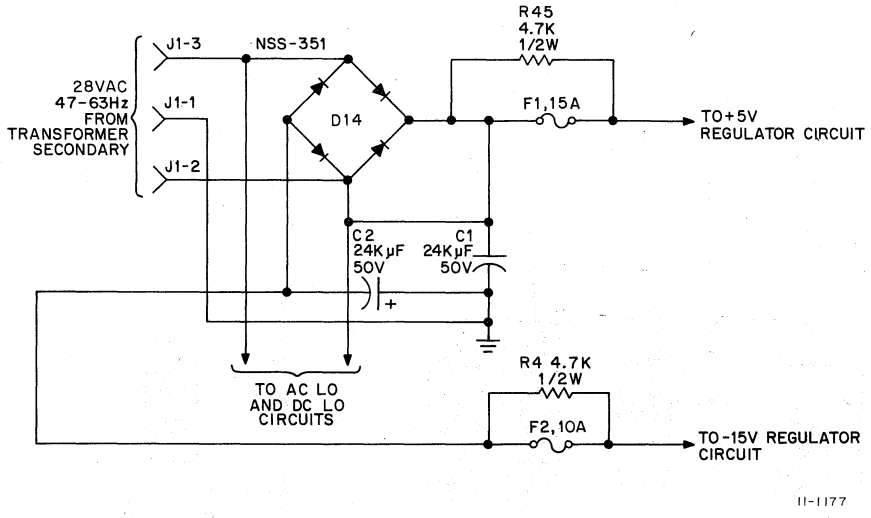


Figure 2-8 Rectifier Circuit

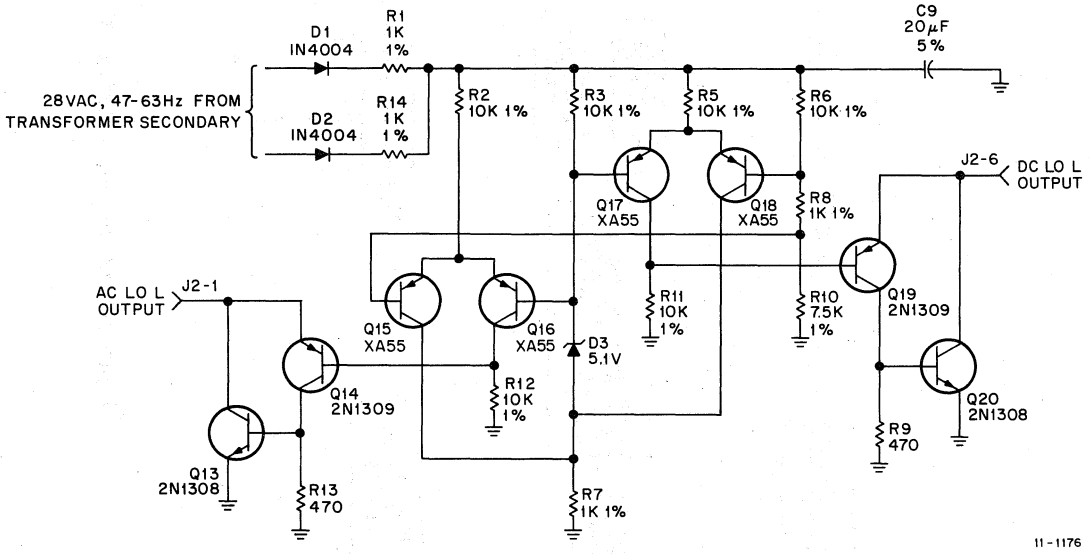


Figure 2-9 BUS AC LO and BUS DC LO Circuits

As C9 charges subsequent to power-up, first Q17, Q18 and then Q15, Q16 change states; the reverse is true during power-down. When C9 starts to charge, Q17 and Q16 are on and Q15 and Q18 are not conducting. As C9 charges further, Q18 starts to conduct into R7 and raises the voltage on the D3 cathode. This acts as a positive feedback and snaps Q17 off and Q18 on more solidly. A few milliseconds later, the voltage across C9 has risen sufficiently for the same process to take place in differential amplifier Q15, Q16. The status of each differential amplifier is followed by the germanium transistor open-collector output stages Q19, Q20 for DC LO L, and Q13, Q14 for AC LO L. These stages clamp the Unibus at about +0.4V until the differential amplifier circuits

sequentially signal them across R11 and R12 that power is up. The outputs then rise sequentially to about +5V as dictated by the Unibus loading and pull-up termination resistors. The sequence is as follows:

power-up → then BUS DC LO L = 0 → then AC LO L = 0 0 = High (+5V)
power-down → then BUS AC LO L = 1 → then DC LO L = 1 1 = Low (+0.4V)

There is sufficient storage in the regulator output capacitors C1 and C2 so that when BUS DC LO L and BUS AC LO L = 0, the output voltage is maintained long enough to permit power fail circuits to operate. Note that the open collector stages are designed to clamp the Unibus to 0.4V maximum, even when there is no ac input to the regulator. They are inherently biased by R11 and R12 until the differential amplifiers signal that power is okay.

2.3.2.3 +5V Regulator Circuit – The +5V regulator samples the output voltage and compares it to the voltage across a reference Zener with a voltage detector transistor, which in turn controls the drivers for the main pass transistor. The +5V regulator circuit is shown in Figure 2-10. An overcurrent circuit is employed.

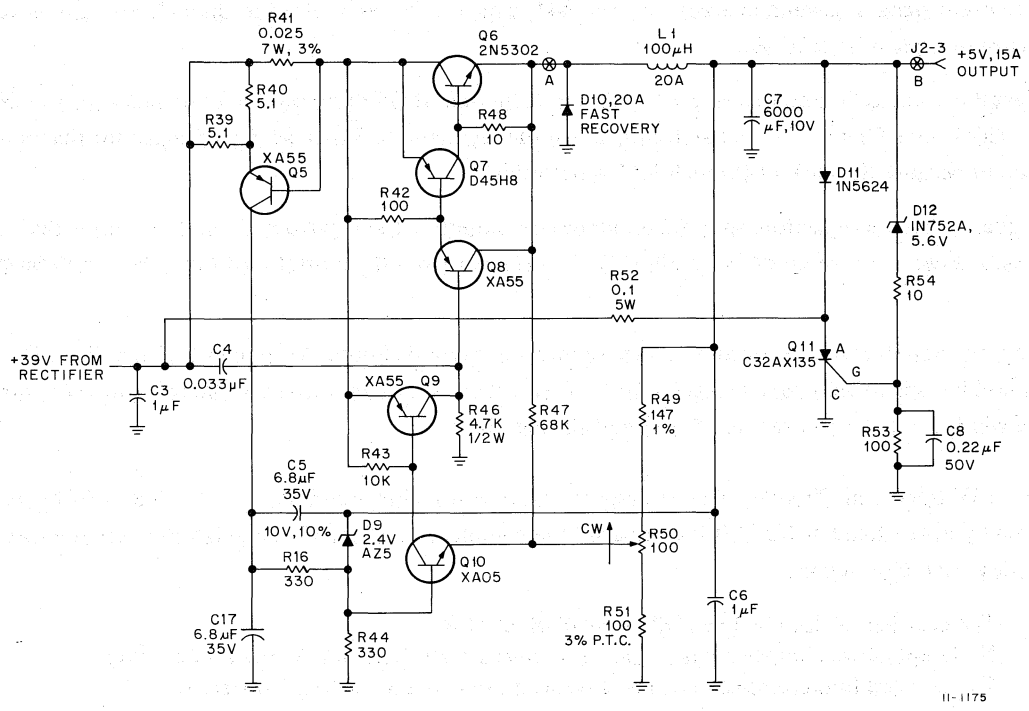


Figure 2-10 +5V Regulator Circuit

The viewing chain consists of R49, 50, 51; the reference Zener is D9 which is fed by R44. Q10 is the detector amplifier. The pass transistor Q6 is turned on by R46. The current is diverted from the base of Q8 by off-driver Q9 which is controlled by Q10. The tendency for the output voltage to rise results in more conduction through Q10 and resultant limiting of conduction through Q6.

The +5V circuit is a regulator that operates in the switching mode for increased efficiency. To switch the regulator, positive feedback is applied to the voltage detector input via R47.

Thus, the whole regulator acts as a Schmitt trigger and is turned either completely on or off, depending on whether the output voltage is too high or too low.

When Q6 is on, it supplies current through filter choke L1 to the output smoothing capacitor C7 and the load. When Q6 is off, the L1 current decays through commutating diode D10 which becomes forward biased by the back emf of L1. The waveform across D10 is a 30V nominal rectangle pulse train. The filtered output across C7 is thus +5V with about a 200 mV peak-to-peak, 10 kHz nominal sawtooth of superimposed ripple. At the crest of the ripple, Q6 turns off, and at the valley, Q6 turns on.

This switching mode of operation limits the dissipation in the circuit to the saturated forward losses of Q6 and D10 and the switching losses of Q6. The resultant high efficiency allows the use of a small heat sink and few semiconductors.

R50 is the voltage adjustment potentiometer. R51 is a positive temperature coefficient wirewound resistor, which compensates for the negative voltage temperature coefficients of the Q10 base-emitter junction and the reference diode D9.

The overcurrent signal is generated across resistor R41, which is in series with the Q6 collector, and is detected by Q5, current limited by R39, 40.

Output fault current is limited to a safe value since conduction of Q5 decreases the reference voltage across D9 to zero. This causes Q10 to conduct and shuts down the regulator. C5 is an averaging capacitor that is necessary in the circuit because the current through R41 is pulsating.

High-frequency bypass capacitors are used on input and output of the regulator, C3 and C6, respectively. C4 is used to slow down the turn-on of Q6 to allow D10 to recover from the on state without a large reverse current spike.

Should a malfunction cause the output voltage to increase beyond about 6.8V nominal, Zener diode D2 will conduct and fire silicon-controlled rectifier Q11. This will crowbar the output voltage to a low value through D11 and will blow fuse F1 in the rectifier circuit through R52.

2.3.2.4 -15V Regulator Circuit – The -15V regulator circuit is shown in Figure 2-11. The -15V output voltage is adjusted by potentiometer R26. It is essentially the complement of the +5V regulator circuit and differs only in the following minor details:

a. The crowbar device is a Triac Q27 instead of an SCR
b. No temperature compensating resistor is required since Q26 and D4 track each other
c. The detailed interconnection of the drivers and the circuit values are different

2.4 MAINTENANCE

This paragraph discusses the adjustments, circuit waveforms, troubleshooting, and parts identification necessary to maintain the Power Supply. The adjustments section discusses the two output potentiometers. The circuit waveforms section provides a guide to proper operation at various places in the circuit. The troubleshooting section provides rules, hints, and a troubleshooting chart as a maintenance aid in isolating Power Supply malfunctions. Finally, the parts identification section provides a directive to obtaining parts information for the entire Power Supply unit through a parts location directory to the mechanical engineering drawings in the *ME11-L Engineering Drawing Manual.*

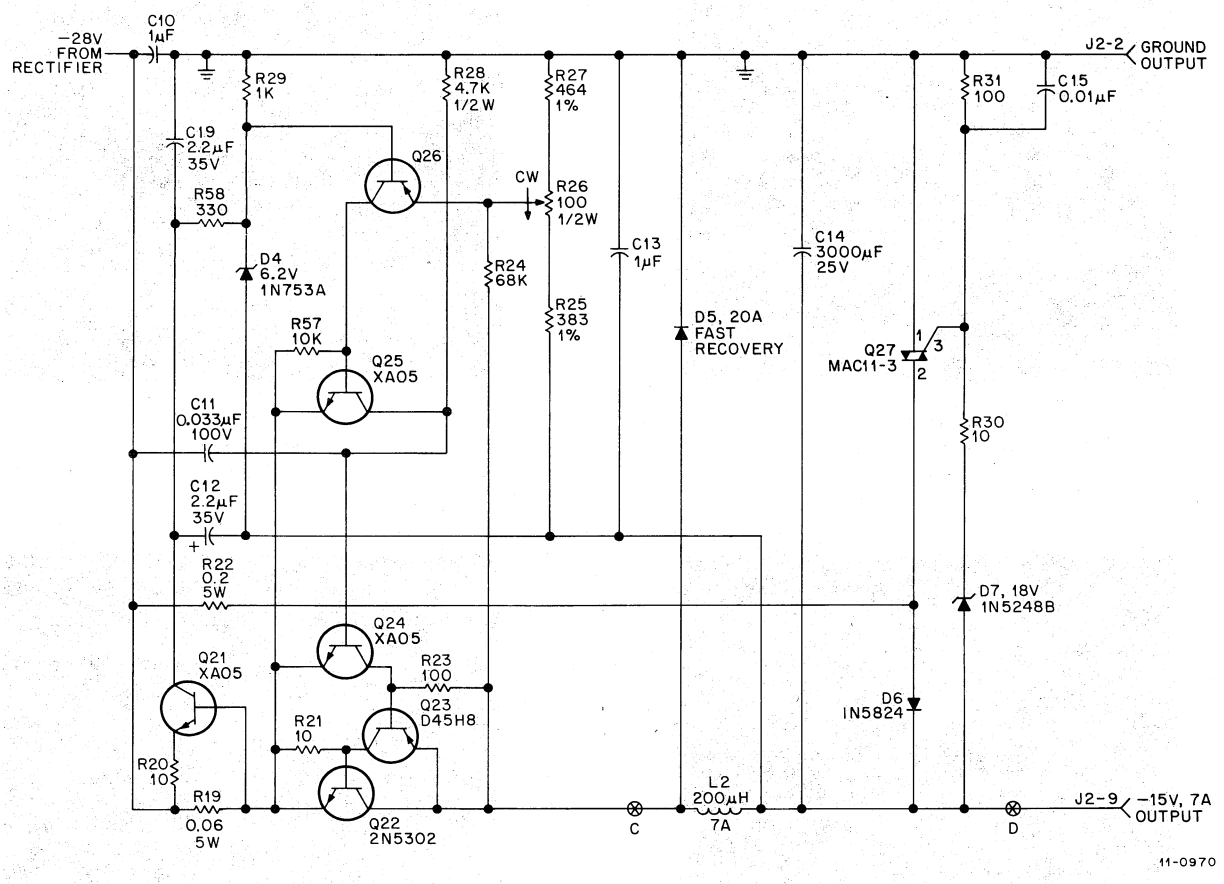


Figure 2-11 -15V Regulator Circuit

2.4.1 Adjustments

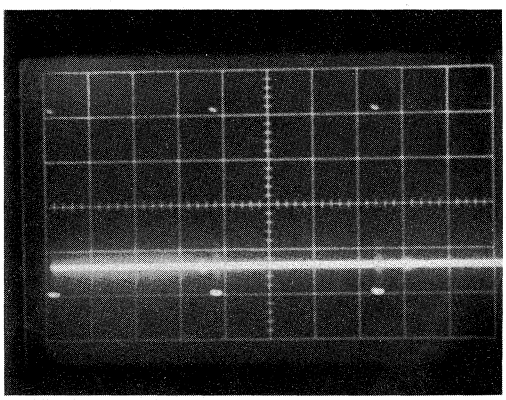
There are only two adjustments to the Power Supply for the +5V and –15V dc output voltages. (A small screwdriver is all that is required for adjustment.) Clockwise adjustment of any of the potentiometers increases voltage. The potentiometers are located on the top side of the DC Regulator Module and are designated as R50 for +5V and R26 for –15V. A +15V adjustment potentiometer and circuitry are also located on the DC Regulator Module, but this supply voltage is not used in the ME11-L and it is not necessary to adjust the +15V potentiometer.

CAUTION

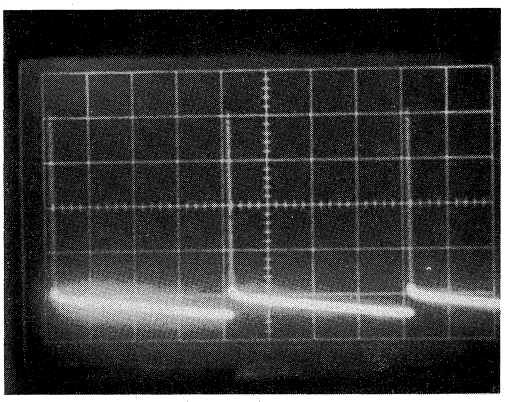
***Do not* adjust voltages beyond their 105 percent rating. Adjust slowly in order to avoid overvoltage crowbar blowing dc output fuses. *Do* use a calibrated voltmeter; preferably a digital voltmeter. Voltages should be adjusted to their center values: +5.0, and -15.0; all under load at the DC Cable termination on the system unit.**

2.4.2 Circuit Waveforms

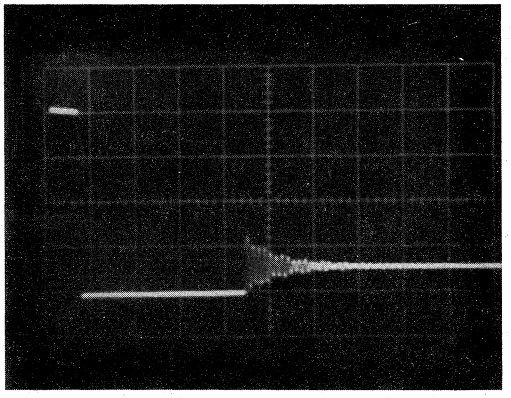
The two basic regulator circuits used on the DC Regulator Module generate +5V and -15V. Figure 2-12 shows six waveforms of the +5V regulator circuit taken at two points (A and B) in the circuit (Figure 2-10). Waveforms a, b, and c are taken at point A, which is the +5V circuit, Q6 transistor output. Waveforms d, e, and f are taken at point B, which is the +5V Power Supply output (J2-3). Figure 2-12 also indicates the load conditions and time



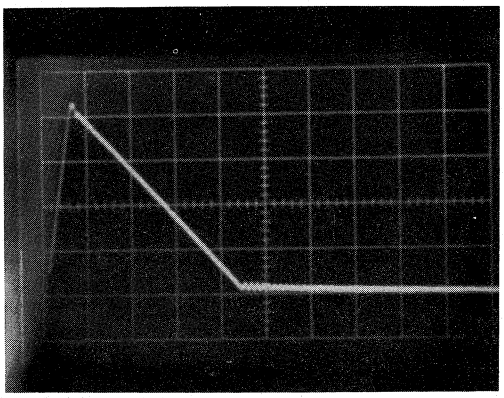
a) Point A, No load,
2 ms/div, and
10V/div.



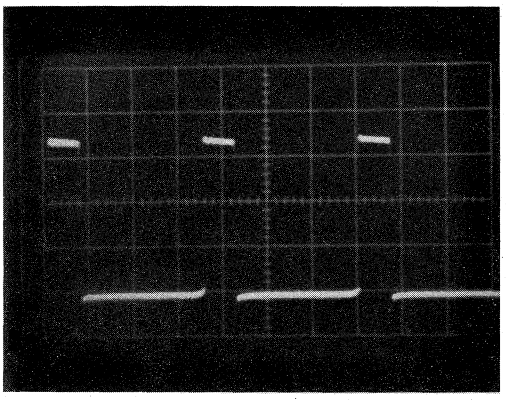
d) Point B, No load,
2 ms/div, and
50 mV/div.



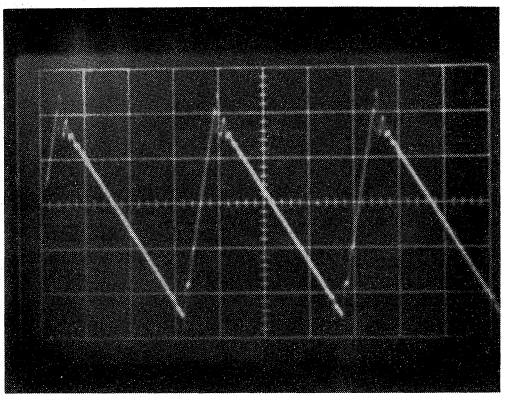
b) Point A, No load,
20 μs/div, and
10V/div.



e) Point B, No load,
20 μs/div, and
50 mV/div.



c) Point A, 20A load.
20 μs/div, and
10V/div.



f) Point B, 20A load,
20 μs/div, and
50 mV/div.

Figure 2-12 +5V Regulator Circuit Waveforms

scales for each waveform. Figure 2-13 shows six waveforms of the -15V regulator circuit taken at two points (C and D) in the circuit (Figure 2-11). Waveforms a, b, and c are taken at point C, which is the -15V circuit, Q22 transistor output. Waveforms d, e, and f are taken at point D, which is the -15V Power Supply output (J2-9). The load conditions and time scales of the respective waveforms are also indicated in Figure 2-13. These waveforms were taken on a Tektronix Model 453 oscilloscope.

2.4.3 Troubleshooting

Troubleshooting information for the Power Supply consists of rules, hints, and a troubleshooting chart. This information provides a maintenance aid for isolating Power Supply malfunctions.

2.4.3.1 Troubleshooting Rules – Troubleshooting rules for the Power Supply are as follows:

a. Be sure that power is turned off and unplugged before servicing the Power Supply.

b. Be sure that input capacitors C1 and C2 are discharged before servicing the Power Supply. A 10 to 100Ω, 10W resistor can be used to speed up discharge of the capacitors. (Be sure power is *off*.)

c. The DC Regulator Module is not internally grounded to the chassis. Shorts to ground can be located after disconnecting the dc output cable from the system unit.

d. The dc output fuses F1 and F2 can be replaced without removing the DC Regulator Module. Before unsoldering the fuses, observe the cautions described in a and b above.

e. For proper operation, all hardware must be secured tightly with about 12 inch-pounds torque (i.e., capacitors, chokes, semiconductors). All hardware should be replaced with identical hardware replacement parts.

f. The DC Regulator Module may be removed from the top of the Power Chassis Assembly while the latter is still bolted to the ME11-L chassis.

g. When replacing power semiconductor components that are secured to the heat sink, apply a thin coat of Wakefield #128 compound or Dow Silicone Grease to heat sink contact side (bottom) of the semiconductor.

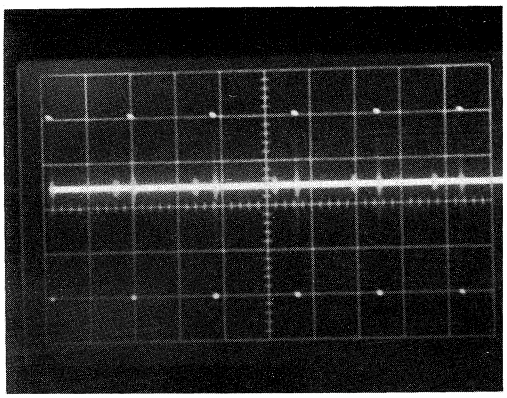
2.4.3.2 Troubleshooting Hints

CAUTION
Unplug ME11-L before servicing.

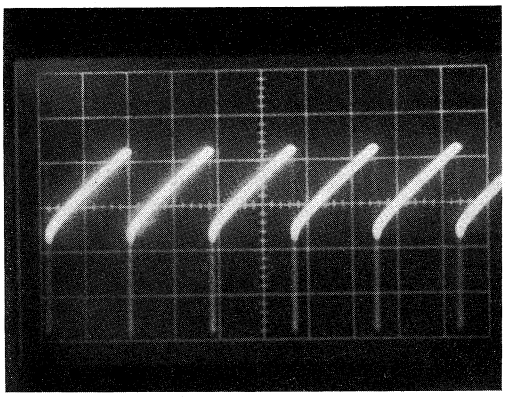
The most likely source of Power Supply malfunction is the DC Regulator Module. A quick remedy for a malfunction may be to replace the entire module. The problem, however, could be a short in the system unit, a defective component, or a problem in the ac input circuit.

The +5V and -15V regulators contain overvoltage detection circuitry. If R50 or R26 are adjusted too far clockwise, the corresponding crowbar circuit trips and blows a fuse. To correct this condition, adjust the potentiometer fully counter-clockwise, replace the blown fuse, and re-adjust according to Paragraph 2.4.1.

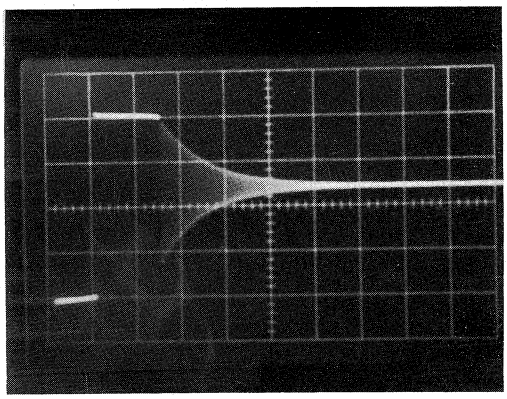
Make a visual examination of the circuitry. Check for burned resistors, cracked transistors, burned printed circuit board etch, oil leaking from capacitors, and loose connections. If a malfunction is caused by something of this nature, a visual check can quickly locate it.



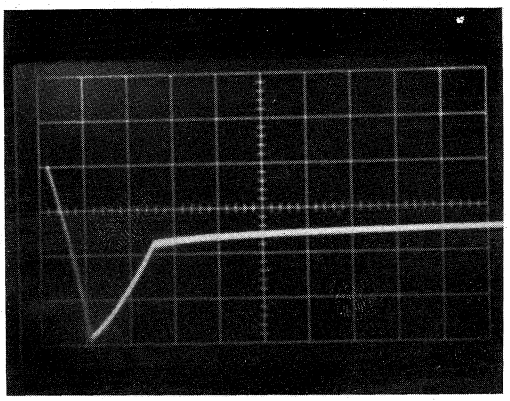
a) Point C, No load,
5 ms/div, and
10V/div.



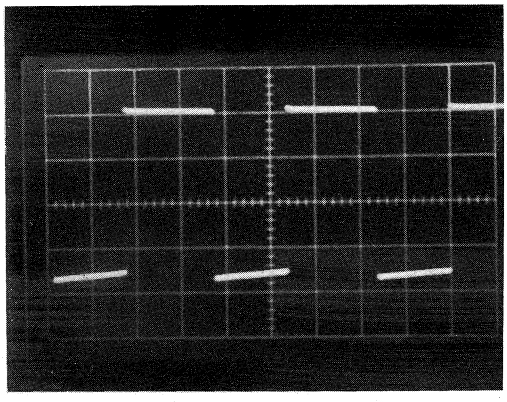
d) Point D, No load,
5 ms/div, and
50 mV/div.



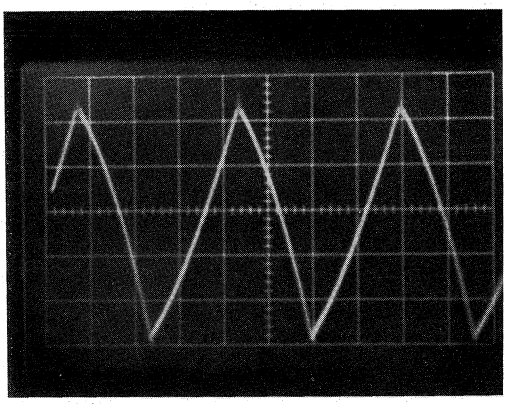
b) Point C, No load,
50 μs/div, and
10V/div.



e) Point D, No load,
50 μs/div, and
50 mV/div.



c) Point C, 5A load,
50 μs/div, and
10V/div.



f) Point D, 5A load,
50 μs/div, and
50 mV/div.

Figure 2-13 – 15V Regulator Circuit Waveforms

2.4.3.3 Troubleshooting Chart – In checking the various areas of the Power Supply, the rules listed in Paragraph 2.4.3.1 should be followed. The waveforms referenced in Paragraph 2.4.2 provide a comparison for the troubleshooting readings. Table 2-4 provides a chart of problems and causes for troubleshooting the Power Supply.

Table 2-4
Power Supply Troubleshooting Chart

Problem	Cause
No +5V Output	F1 opened D14 or transformer opened +5V adjusted too high*
+5V Output Too Low	Q5, D9, Q10, Q9, Q11, D2, or D10 shorted C5 or C7 shorted R49, R50, R51, R46, or R44 opened Q6, Q7, Q8, or D11 shorted Q9, Q10, or D9 opened
No –15V Output	F2 opened D14 or transformer opened –15V adjusted too high*
–15V Output Too Low	Q25, D4, Q26, Q21, Q27, D7, or D5 shorted C14 or C12 shorted R22, R26, R25, R27, or R29 opened Q22, Q23, Q24, or D6 shorted Q25, Q26, or D4 opened
BUS AC LO L Will Not Go High	Q13, Q14, or Q15 shorted Q16 or D3 opened R7, R3, R6, or R8 opened C9 shorted
BUS AC LO L Will Not Go Low and/or Acts Erratically on Power-On/Power-Off	Q13, Q14, or Q16 opened Q15 or D3 shorted R12, R13, R7, or R10 opened
BUS DC LO L Will Not Go High	Q19, Q20, or Q18 shorted Q17 or D3 opened R7, R3, or R6 opened C9 shorted
BUS DC LO L Will Not Go Low and/or Acts Erratically on Power-On/Power-Off	Q19, Q20, or Q17 opened Q18 or D3 shorted R9, R10, R11, or R8 opened

* These causes make the crowbar fire, which in turn blows the appropriate fuse.

2.4.4 Parts Identification

Parts identification for the Power Supply is provided in the *ME11-L Engineering Drawing Manual.* The assembly drawings and associated parts lists provide the respective unit parts, their part designations, and DEC part numbers. These drawings and their numbers are as follows:

Module Utilization	D-MU-ME11-L-01
15-Bit 18-Mil Memory	B-DD-MM11-L
Regulator Board	E-IA-5409728-0-0
Circuit Schematic	D-CS-5409728-0-1
Circuit Schematic	C-CS-5409959-0-1
Line Set BC05H	B-DD-BC05H-0
AC Input Harness	E-IA-7008889-0-0
DC Harness Assembly	D-IA-7008857-0-0
Unit Assembly ME11-L	D-UA-ME11-L-0
Power Supply H740	D-AD-7008731-0-0
Power Supply Assembly (Parts List)	A-PL-7008731-0-0
Software List	A-SL-ME11-L-4
Accessory List	A-AL-ME11-L-3

CHAPTER 3
MM11-L CORE MEMORIES

3.1 INTRODUCTION

This chapter provides the user with the theory of operation and logic diagrams necessary to understand and maintain the MM11-L Read/Write Core Memories. The level of discussion assumes that the reader is familiar with basic digital computer theory. Both general and detailed descriptions of the core memories are included.

Although memory control signals and data pass through the Unibus, it is beyond the scope of this manual to describe the operation of the Unibus itself. A detailed description of the Unibus is presented in the *PDP-11 Peripherals and Interfacing Handbook.*

A complete set of engineering logic drawings is shipped with each core memory. These drawings are bound in a separate volume entitled *MM11-L Core Memories, Engineering Drawings.* The drawings reflect the latest print revisions and correspond to the specific memory shipped to the user.

This chapter of the manual is divided into three sections: General Description, Detailed Description, and Maintenance.

3.2 GENERAL DESCRIPTION

This paragraph provides a physical description and specifications for the memory. The major functional units of each memory are briefly described and the basic memory operations are discussed.

3.2.1 Physical Description

The MM11-L provides 8192 (8K) 16-bit words. This requires three standard 8-1/2 inch wide modules: two are hex-height and one is quad-height. The quad-height module contains the memory stack: module H214 for 8K. One hex-height module (G110) contains the control logic, inhibit drivers, sense amplifiers, and 16-bit data register; the other hex-height module (G231) contains the address selection logic, current generator, and switches and drivers. Pin-to-pin compatibility exists between the C, D, E, and F connectors on both these modules and the stack module connectors. The pins on the A and B connectors of both these modules are also compatible with the standard Unibus pin assignments.

The modules are installed in the ME11-L mounting box. It is recommended that the Driver Module (G231) be installed between the Control Module (G110) and the Stack Module (H214). Photographs of the component side of the modules are shown in Figures 3-1, 3-2, and 3-3.

3.2.2 Specifications

The general memory specifications are listed in Table 3-1.

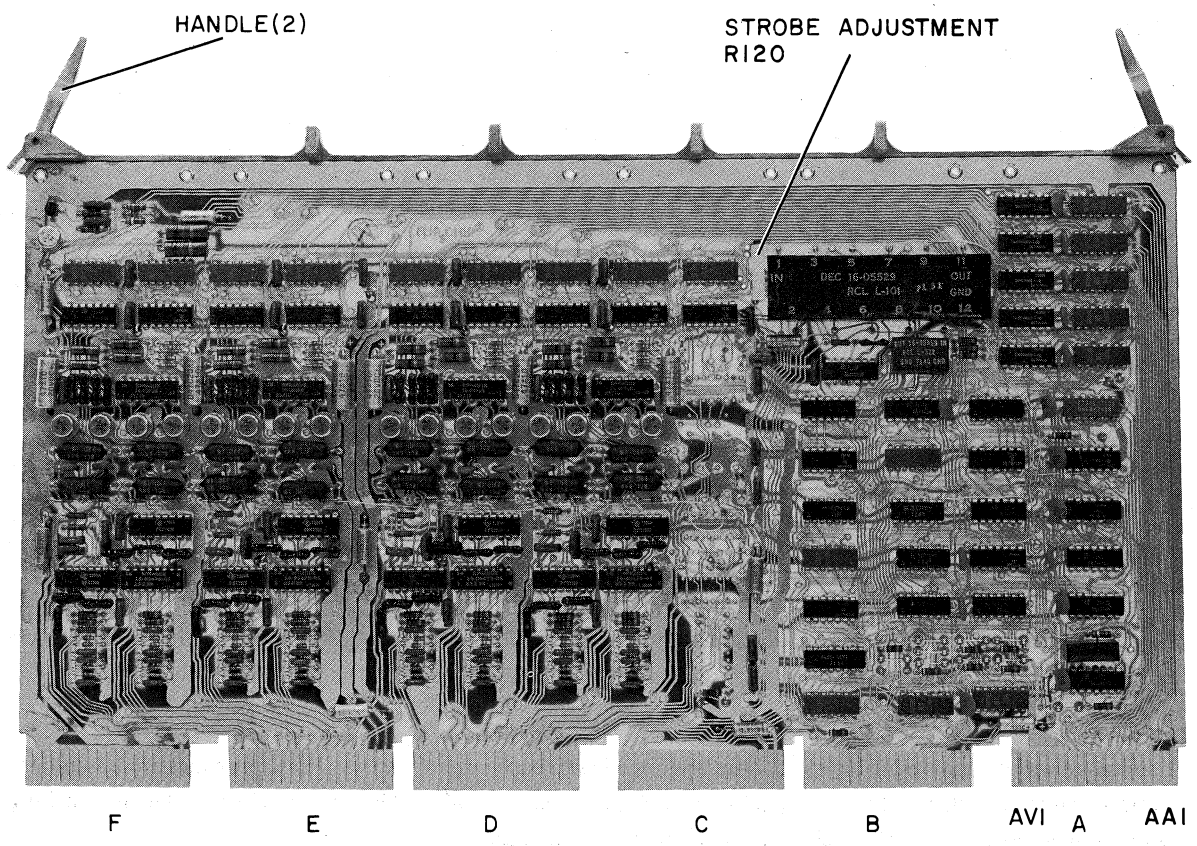


Figure 3-1 Component Side of Control Module G110

3.2.3 Functional Description

3.2.3.1 **Introduction** – The memory is a read/write, random access coincident current, magnetic core type with a cycle time of 900 ns and an access time of 400 ns. It is organized in a 3D, 3-wire planar configuration. Word length is 16 bits: MM11-L contains 8192 (8K) words.

The major functional units of the memory (Figure 3-4) are briefly described in the following paragraphs.

3.2.3.2 **Control Module (G110)** – The Control Module (G110) contains the memory control circuits, inhibit drivers, sense amplifiers, data register, threshold circuit, - 5V supply, and device selector.

a. *Memory Control Circuits* – Control circuits are provided to acknowledge the request of the master device; determine which of the four basic operations (DATI, DATIP, DATO or DATOB) is to be performed; and set up the appropriate timing and control logic to perform the desired read or write operation. If a byte operation has been selected, address line A00 L determines the byte to be selected. The actual read or write operation is selected by control lines (C00 and C01). The memory control logic also transfers data to and from the Unibus.

b. *Inhibit Drivers* – Each bit mat contains a single inhibit/sense line that passes through all cores on the mat. To write a 0 into a selected bit, an inhibit current is passed through the inhibit/sense line that cancels the write current in the Y line. The core does not switch so it remains in the 0 state. With no inhibit current, the currents in the X and Y lines switch the core to the 1 state.

c. *Sense Amplifiers* – During a read operation, the sense amplifier picks up a voltage induced in the sense/inhibit winding when a core is switched from a 1 to a 0. This signal is detected and amplified by the sense amplifier whose output sets a data register flip-flop to store a 1. In effect, a 1 is read but the core is switched to the 0 state. Cores which were previously set to 0 are not affected.

d. *Data Register* – The data register is a 16-bit flip-flop register used to store the contents of a word after it is destructively read out of the memory; the same word can then be written back into memory (restored) when in the DATI mode. The register is also used to accept data from the Unibus lines to accommodate the loading of incoming data into the core memory during the DATO or DATOB cycles.

e. *Device Selector* – The device address (bus lines A14 through A17) is decoded in the device selector to determine if the memory bank has been addressed.

f. *Threshold Circuit and -5V Supply* – The threshold circuit provides a reference threshold voltage to the sense amplifiers. During a read operation, if the threshold voltage (±20 mV) is exceeded, the sense amplifier produces an output. The -5V supply provides a negative voltage for the sense amplifiers.

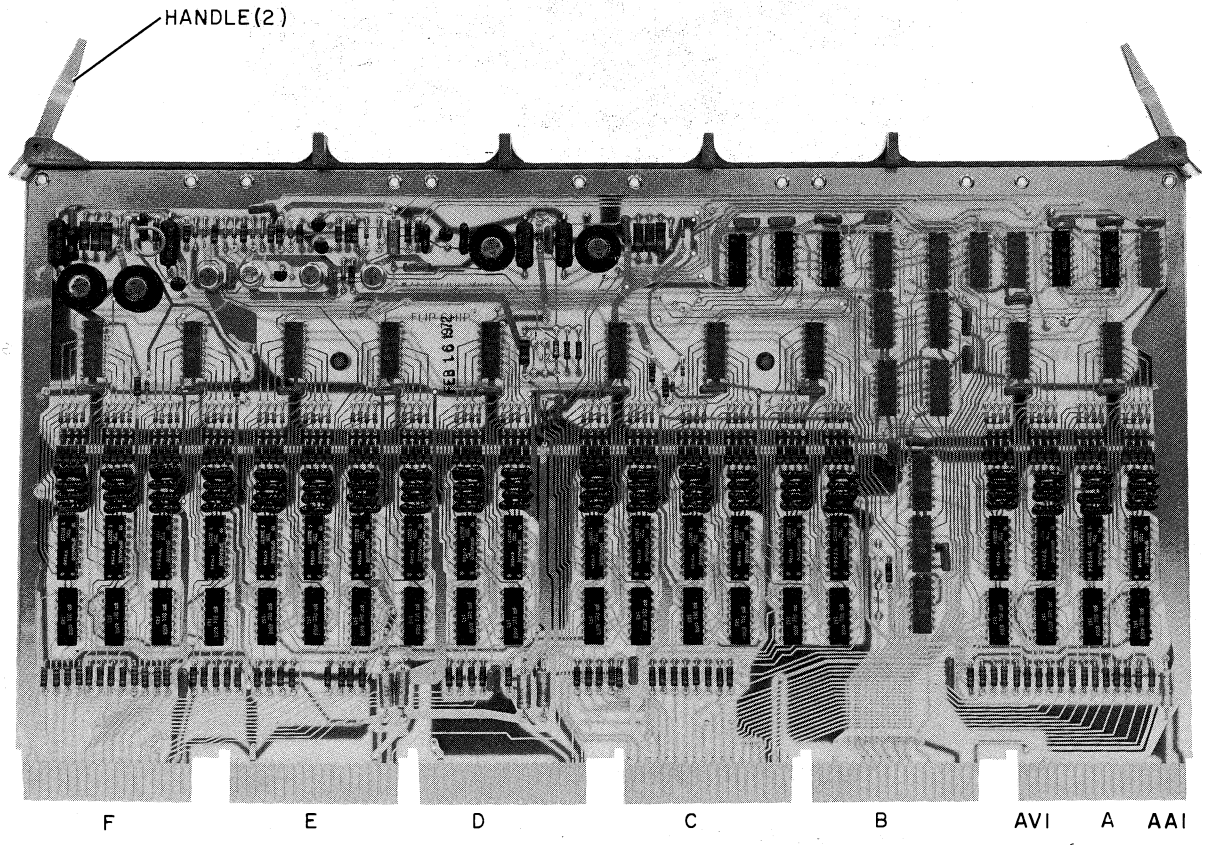


Figure 3-2 Component Side of Driver Module G231

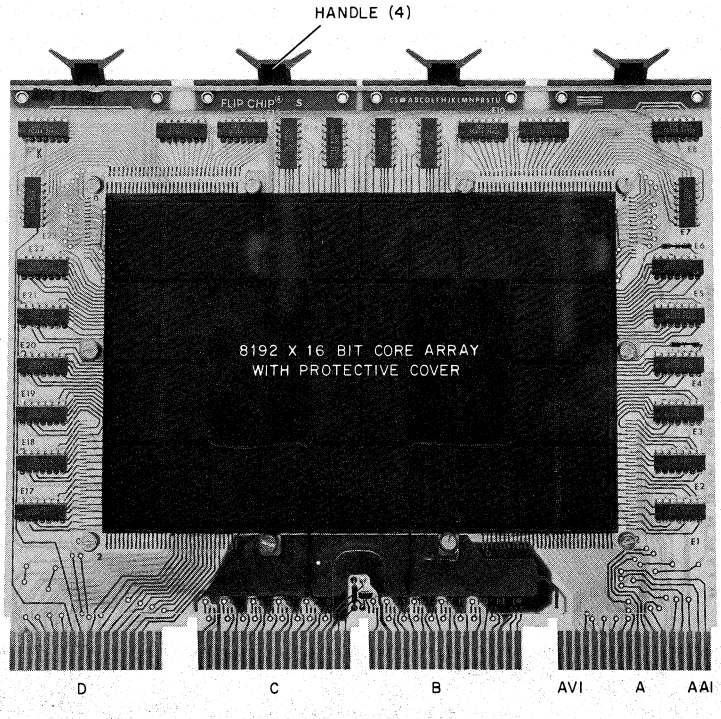


Figure 3-3 Component Side of 8K Stack Module H214

Table 3-1
MM11-L Memory Specifications

Type:

Magnetic core, read/write, coincident current, random access

Organization:

Planar, 3D, 3-wire

Capacity:

8192 (8K) words for MM11-L

Access Time and Cycle Time:

Bus Mode	Cycle Time Non-Interleaved	Access Time
DATI	900 ns	400 ns
DATIP	450 ns	400 ns
DATO-DATOB (PAUSE L)	900 ns	200 ns
DATO-DATOB (PAUSE H)	450 ns	200 ns

(continued on next page)

Table 3-1 (Cont)
MM11-L Memory Specifications

X-Y Current Margins:

±6% @ 0°C, ±7% @ 25°C, ±6% @ 50°C

Strobe Pulse Margins:

±30 ns @ 0°C, ±40 ns @ 25°C, ±30 ns @ 50°C

Voltage Requirements:

+5V ±5% with less than 0.05V ripple
-15V ±5% with less than 0.05V ripple

Average Current Requirements:

Stand by
+5V: 1.7A
-15V: 0.5A

Memory Active
+5V: 3.4A
-15V: 6.0A

Power Dissipation (worst case):

Control Module (G110): = 60W
Drive Module (G231): = 40W
Stack Module (H214): = 20W
Total at maximum repetition rate: 120W

Environment:

Ambient temperature: 0°C to 50°C (32°F to 122°F)
Relative Humidity: 0–90% (non-condensing)

3.2.3.3 **Driver Module (G231)** – The Driver Module (G231) contains the address selection logic, switches and drivers, current generator, stack discharge circuit, and DC LO protection circuit.

a. *Address Selection Logic* – The core memory receives an 18-bit address from the master device. The address is latched and decoded to determine if the memory is the selected device and to determine the core location specifically addressed. If the operation is a byte operation, bus line A00 L indicates the byte to be used. The X and Y portion of the address is decoded through selection switches and a diode matrix to enable passage of read/write current through the selected X and Y drive lines of the memory. The coincidence of these currents selects the specific 16-bit core memory location desired.

b. *Switches and Drivers* – The switches and drivers direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because a single read/write line is used, and the current for a write operation is opposite in polarity to the current required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

c. *Current Generators* – X and Y current generators provide the current necessary to change the state of the magnetic cores. The linear rise time and amplitude of the output-current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

(continued on page 3-7)

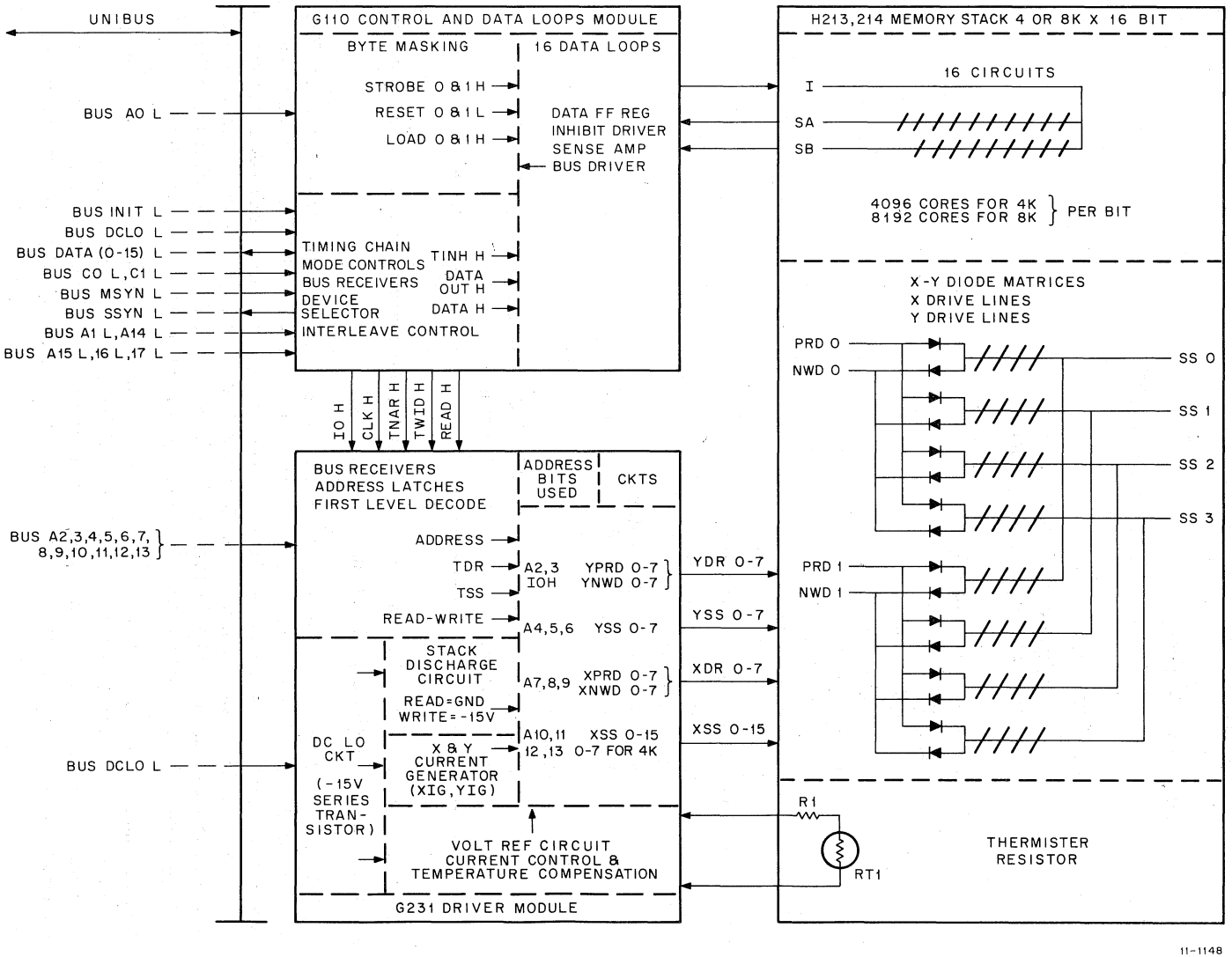


Figure 3-4 MM11-L Memory Block Diagram

d. *Stack Discharge Circuit* – The stack discharge circuit maintains the proper stack charge voltage during operation: approximately 0V during a read operation and approximately -14V during a write operation.

e. *DC LO Protection Circuit* – If the ac input voltage is out of tolerance, DC LO L is asserted on the Unibus. It is sensed by the DC LO protection circuit which inhibits the memory operation by opening the -15V line to the current source. This prevents spurious memory operation.

3.2.3.4 Stack Module (H214) – The Stack Module contains the ferrite core array and the X-Y diode matrices. 16 core mats, each wired in a 128 X 64 matrix are used for the 8K memory (H214). The stack also contains the resistor-thermistor combination to control the G231 X-Y current generator temperature compensation.

3.2.4 Basic Memory Operations

The core memory has four basic modes of operation. The main function of the memory is simply to read and write data. Additional modes are provided, however, to allow for byte operation and to eliminate the restore cycle when it is not needed, thereby increasing overall system efficiency. The four basic memory operations are:

a. Read/restore (DATI)
b. Read pause (DATIP)
c. Write (DATO)
d. Write byte (DATOB)

These four modes are discussed briefly in the following paragraphs.

NOTE

In the following discussions, all operations refer to the master (controlling) device. For example, the term "data out" indicates data flowing out of the master and into the memory.

3.2.4.1 Data In (DATI) Cycle – The DATI cycle is a read/restore memory cycle. During this operation, the memory reads the information from the selected core location, transfers it to the Unibus, and then writes the information back into the memory location. This last step is necessary because the core memory is a destructive readout device. During the first part of the cycle, the memory loads the data into a register; at the same time, the memory applies the data to the Unibus. Then, during the second part of the cycle, the memory takes the data from the register and writes it back into the memory location.

3.2.4.2 Data In, Pause (DATIP) Cycle – Normally in reading memory, the information is destroyed in the particular location accessed, and the data must be restored. However, sometimes it is not actually necessary to restore the information after reading because the location is to have new data written into it. In this instance, eliminating the restore operation decreases the memory cycle time by approximately 50 percent. The DATIP operation is used for this purpose. The data is read from memory and the restore cycle is inhibited. Because no restore cycle is used, a DATIP must always be followed by a write cycle (either DATO or DATOB) on the same address or data in both addresses will be destroyed, the memory controller will be unable to control the bus, and other devices will be unable to access the bus (this is known as hanging the bus).

3.2.4.3 Data Out (DATO) Cycle – The DATO cycle is a write memory cycle used by the master device to transfer data into core memory. To ensure that proper data is stored, the memory unit must first be cleared by reading the cores (thereby setting them all to 0) before writing in the new data. During a normal DATO, the memory first performs the read operation to clear the cores and then performs a write cycle to transfer data from the bus into the selected core location. If a DATO follows a DATIP (rather than a DATI), the sequence is not the same. The DATIP clears core and generates a pause flag; the DATO skips the read cycle and immediately begins the write cycle. This process reduces DATO cycle time by approximately 50 percent.

3.2.4.4 **Data Out, Byte (DATOB) Cycle** – The DATOB cycle is similar in function to the DATO cycle except that during DATOB, data is transferred into the core memory from the bus in byte form rather than as a full word. During the read cycle, the non-selected byte is saved by reading it into the data register while the selected byte is transferred into the register from the bus. During the write cycle, only the selected byte portion of the word is loaded into the memory location from the bus. At the same time, the non-selected byte is restored from the data register into the memory location. In effect, the memory is first cleared and then simultaneously performs a restore cycle for the non-selected byte and a write cycle for the selected byte. This mode can follow a DATIP as described above.

3.3 DETAILED DESCRIPTION

This paragraph provides a detailed description of the MM11-L memories. The detailed description covers the core array, device and word selection, switches and drivers, current generation, stack discharge circuit, DC LO circuit, sense/inhibit circuitry, control and timing logic, and memory operating cycles.

3.3.1 Core Array

The ferrite-core array for the 8K memory consists of 16 mats arranged in a planar configuration. Each mat contains 8192 ferrite cores arranged in a 128-by-64 array. Each mat represents a single bit position of a word. This planar configuration provides a total of 8192 16-bit word locations. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or a binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals. The outside diameter of each core is 18 mil; the inside diameter is approximately 11 mil. Each core is 4.5 mil thick.

Selection and switching of the cores is provided by three wires traversing each core in a special selection technique. An X-axis read/write winding passes through all cores in each horizontal row for all 16 mats. A Y-axis read/write winding passes through all cores in each vertical row for all 16 mats. Through the use of selection circuits which control the current applied to specific X-Y windings, any one of the 8192 word locations can be addressed for writing data into memory or reading data out of memory. A third line passes through each core on a mat to provide the sense/inhibit functions. There is one sense/inhibit line per mat. This single sense/inhibit line, as well as the selection circuits, are discussed in subsequent paragraphs.

3.3.2 Memory Operation

Figure 3-5 illustrates a typical portion of the core memory. An X and Y winding pass through each core in the mat. The current passing through any one winding is such that no single winding produces a magnetic field strong enough to cause a core to change its magnetic state. Only the reinforcing magnetic field caused by the coincident current of both an X and a Y winding can cause the core located at the point of intersection to change states. It is this principle that allows the relatively simple winding arrangement to select one and only one memory core out of the total contained on each mat. The current passing through either an X or Y winding is referred to as the half-select current.

A half-select current passing through the X3 winding (Figure 3-5) from left to right produces a magnetic field that tends to change all cores in that horizontal row from the 0 to 1 state. The flux produced by the current is, however, insufficient to complete the state transition in any core. Simultaneously passing a half-select current through the Y2 winding from top to bottom produces the same effect on all cores in that particular vertical row. Note, however, that both currents pass through only one core which is located at the intersection of the X3 and Y2 windings. This is the selected core and the combined current values are sufficient to change the state of the core. The arrows in Figure 3-5 show current direction for the write cycle.

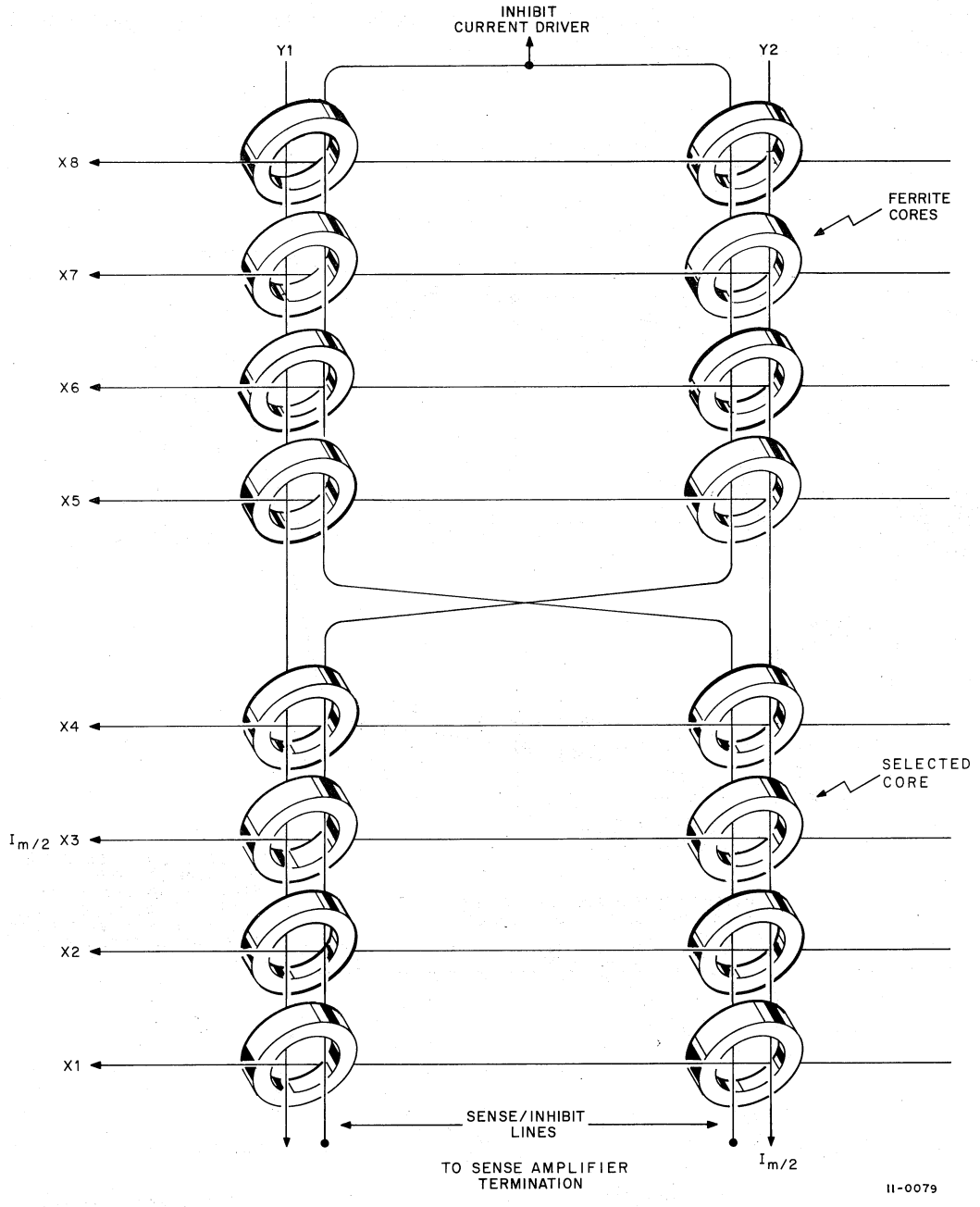


Figure 3-5 Three-Wire Memory Configuration

All X and Y windings are arranged in such a manner that whenever a half-select current is passed through each, the resultant magnetic fields combine in the core at the point of intersection. This combined, full-select current ensures that the selected core is left in the binary 1 state. The currents used to select the core are referred to as write currents. A typical hysteresis loop for a core is shown in Figure 3-6.

In the MM11-L Core Memory, the X3 windings in all 16 mats are connected in series as are the Y2 windings. Therefore, whenever a full-select current flows through a selected core on one mat, it also flows through an

identical core on the other 15 mats. The X3-Y2 cores on all mats switch to a binary 1, causing each of the 16 cores to become one bit of a 16-bit storage cell.

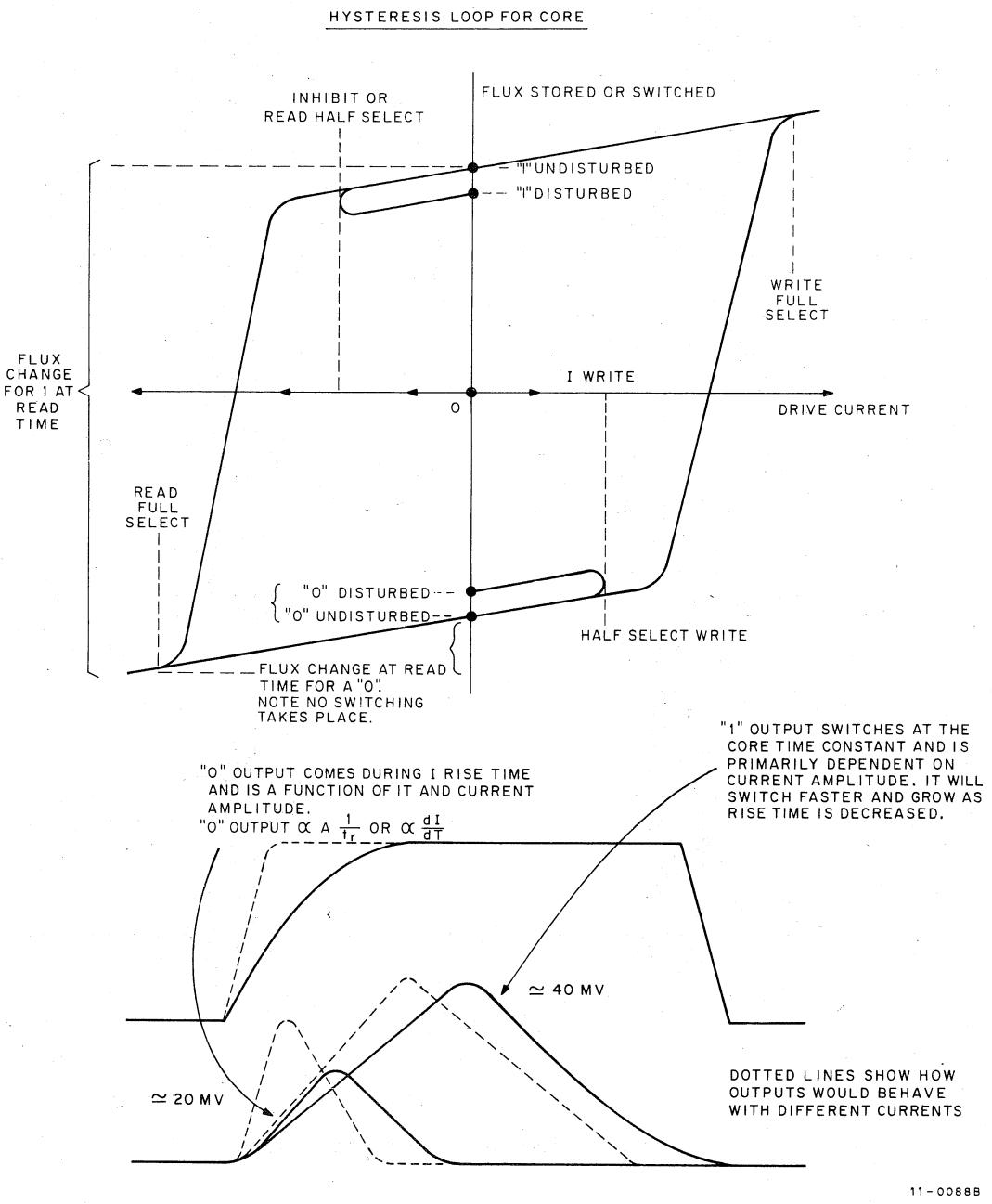


Figure 3-6 Hysteresis Loop for Core

Because of the serial nature of the X-Y windings a method is used that allows cores to remain in the 0 state during a write operation; otherwise, every 16-bit word selected would be all 1s. The method used in the MM11-L Core Memories is to first clear all cores to the 0 state by reading and then, by using an inhibit winding during the

write operation, to inhibit cores on particular mats. The inhibited cores remain 0s even when identical cores on other mats are set to 1s.

The half-select current for the inhibit lines is applied from an inhibit current driver, which is a switch and a resistor between the inhibit line and - 15V. The current in the inhibit line flows in the opposite direction from the write current in all Y-lines and cancels out the write current in any Y-line. There is a separate inhibit driver for each memory mat, and each mat represents one bit position of a word; thus, selected bits can be inhibited to produce any combination of binary 1s and 0s desired in the 16-bit word. It must be remembered that the inhibit function is active only during write time.

The sense/inhibit lines are also used to read out information in a selected 16-bit memory cell. The specific core is selected at read time in the same manner as during the write cycle with one notable exception: the X and Y currents are in the opposite direction. These opposite half-select currents cause all cores previously set to 1 to change to 0; cores previously set to 0 are not affected. Whenever the core changes from 1 to 0, the flux change induces a current in the sense winding of that mat. This current is detected and amplified by a sense amplifier. The amplifier output is strobed into the data register for eventual transfer to the Unibus.

Figure 3-7 shows a 16-word by 4-bit planar memory. The MM11-L Core Memory (8K) functions in the same manner, except that it has 128 X-lines, 64 Y-lines, and 16 core mats. The core stringing is identical, and the sense windings are strung through all 8192 cores with the interchange between X63 and X64 instead of between X1 and X2.

3.3.3 Device and Word Selection

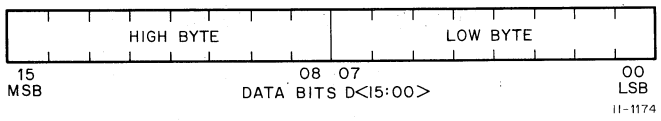
When the processor or a peripheral device is to perform a transaction with the memory, the processor asserts an 18-bit address on Unibus address lines A⟨17:00⟩. Four of the 18 bits (A⟨17:14⟩) indicate the address of the memory as a device. Thirteen of the 14 remaining bits (A⟨13:01⟩) indicate the address of a specific word within the memory. Address bit A00 is used to select the byte (8 bits) transactions when in the DATOB mode.

The memory address is decoded by the device selection circuit on the Control Module (G110). The word address is stored in a register on the Driver Module (G231) whose output is decoded to activate the X-Y line switches and drivers which select the addressed word. These circuits contain jumpers which are included or excluded to configure the memory to establish a specific device address.

Table 3-2 lists the function of each address bit. Figure 3-8 is a simplified block diagram of the device and word address selection circuits.

3.3.3.1 Memory Organization and Addressing Conventions – Prior to a detailed discussion of the address selection logic, it is important to understand memory organization and addressing conventions.

The memory is organized in 16-bit words each consisting of two 8-bit bytes. The bytes are identified as low and high as shown below.



Each byte is addressable and has its own address location: low bytes are even numbered and high bytes are odd numbered. Words are addressed at even-numbered locations only; the high (odd) byte is automatically included.

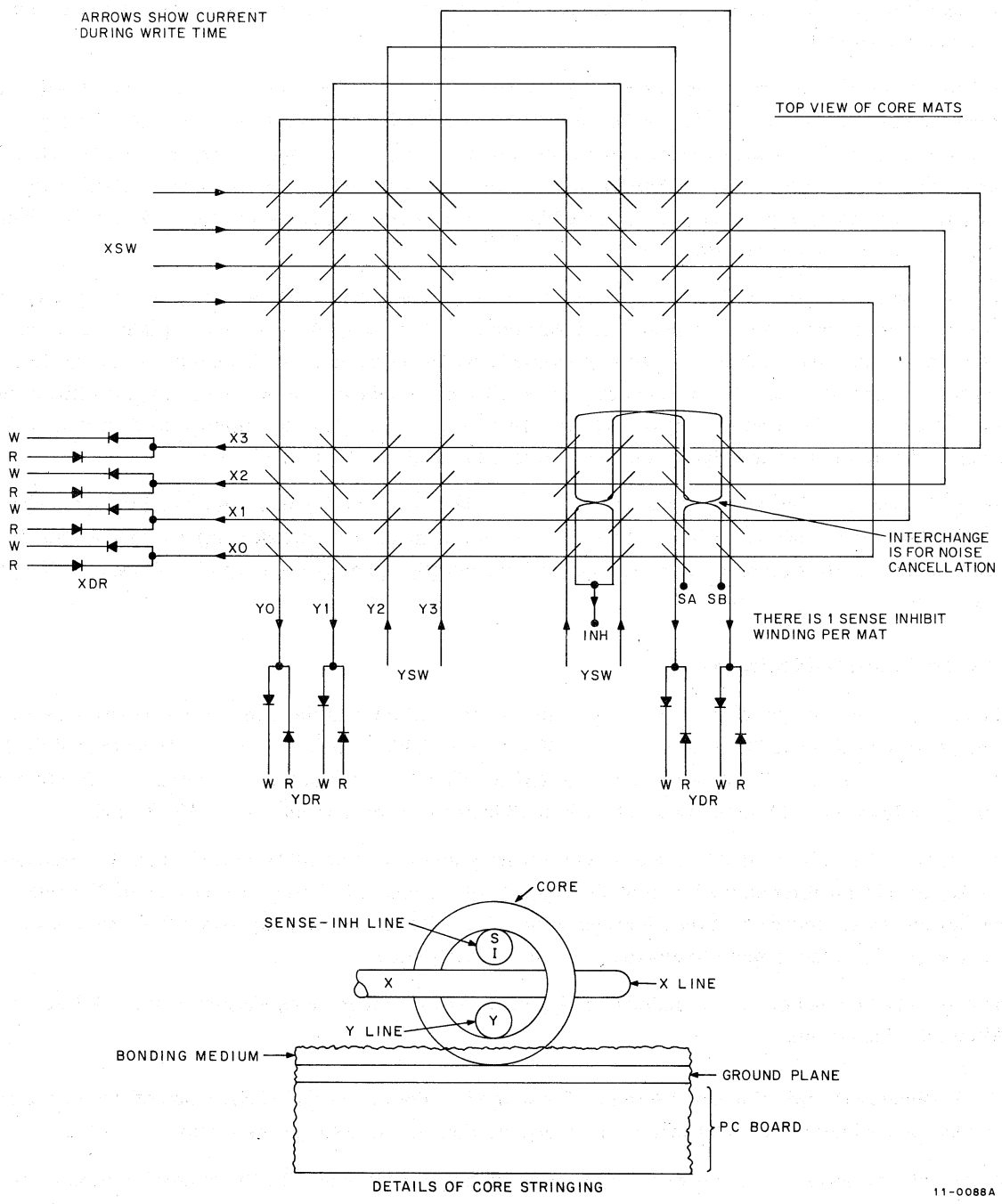


Figure 3-7 Three-Wire 3D Memory, Four Mats
Shown for a 16-Word by 4-Bit Memory

For example, an 8K word memory has 8192 words or 16,384 bytes; therefore, 16,384 locations are assigned. The address locations are specified as 6-digit octal numbers. The 16,384 locations for the 8K memory are designated 000000 through 037777. Figure 3-9 shows the organization for an 8K memory.

Table 3-2
Addressing Functions

Bus Address	Function
A00	Controls byte mode
A02, A03, A01	Decode Y-Drivers
A04, A05, A06	Decode Y-Switches
A07, A08, A09	Decode X-Drivers
A10, A11, A12	Decode X-Switches
A13	Decodes X-Switches
A14, A15, A16, A17	Go to device selector

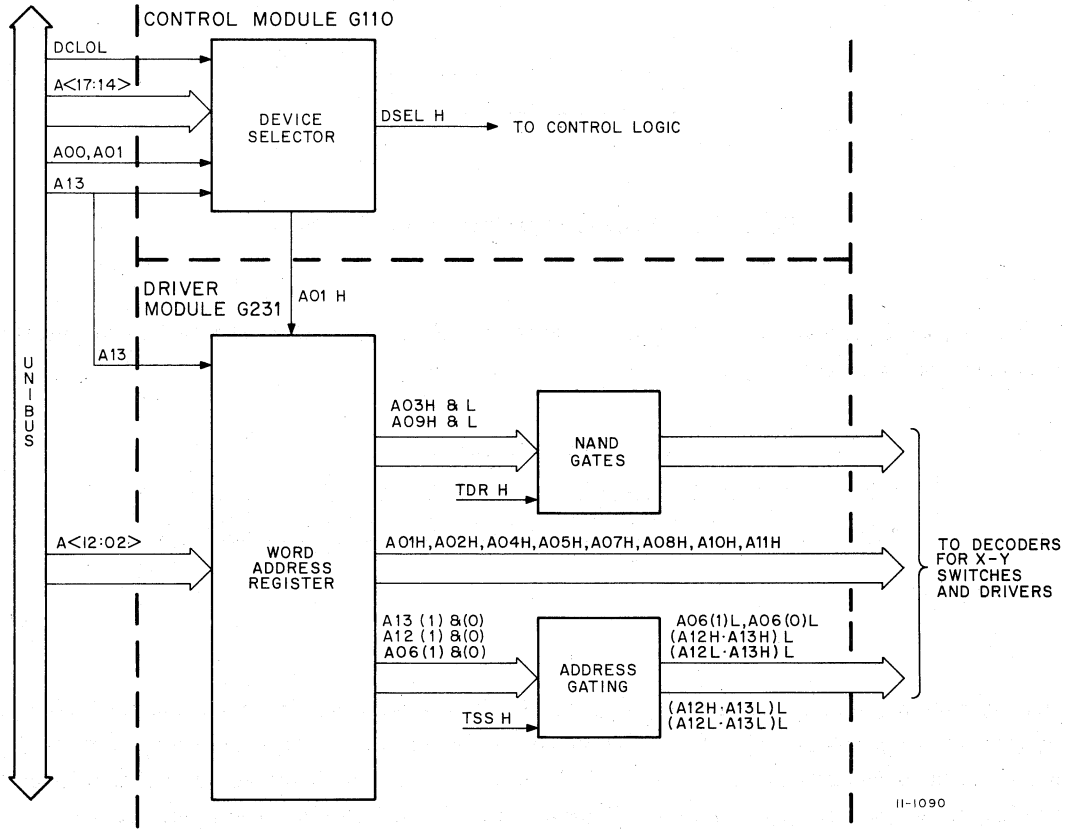


Figure 3-8 Device and Word Address Selection Logic, Block Diagram

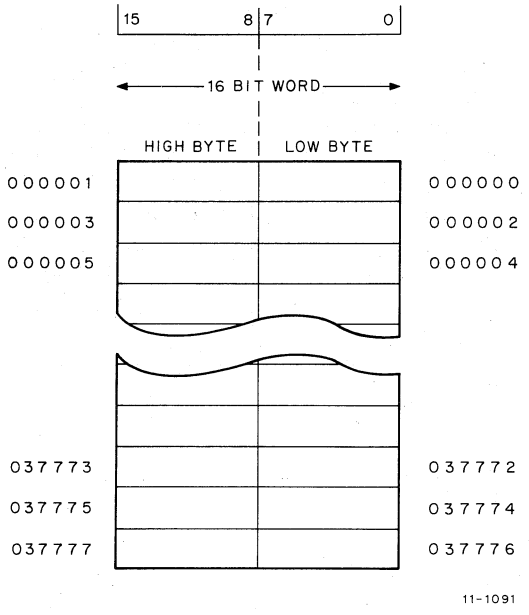


Figure 3-9 Memory Organization for 8K Words

The address selection logic responds to the binary equivalent of the octal address. The binary equivalent of 017772 is shown below as an example.

ADDRESS BITS A<17:00>

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BIT POSITION
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	BINARY
0			1			7			7			7			2			OCTAL

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Each memory bank requires its own unique device address. For example, assume that a system contains three 8K memory banks (Figure 3-10). The device selector for the 8K memory decodes four address lines (A⟨17:14⟩). Examination of the binary states of bits A14 and A15 allow the selection of a unique combination for each bank. The combination, which is the device address, is hardware selected by jumpers in the device selector.

During system operation, the processor asserts the binary equivalent of the octal address on Unibus address lines A⟨17:00⟩. The processor uses positive logic and the Unibus uses negative logic.

Processor (Positive Logic)
Signal Asserted: High = Logical 1 = +3V
Signal at Rest: Low = Logical 0 = 0V

Unibus (Negative Logic)
Signal Asserted: Low = Logical 1 = 0V
Signal at Rest: High = Logical 0 = +3V

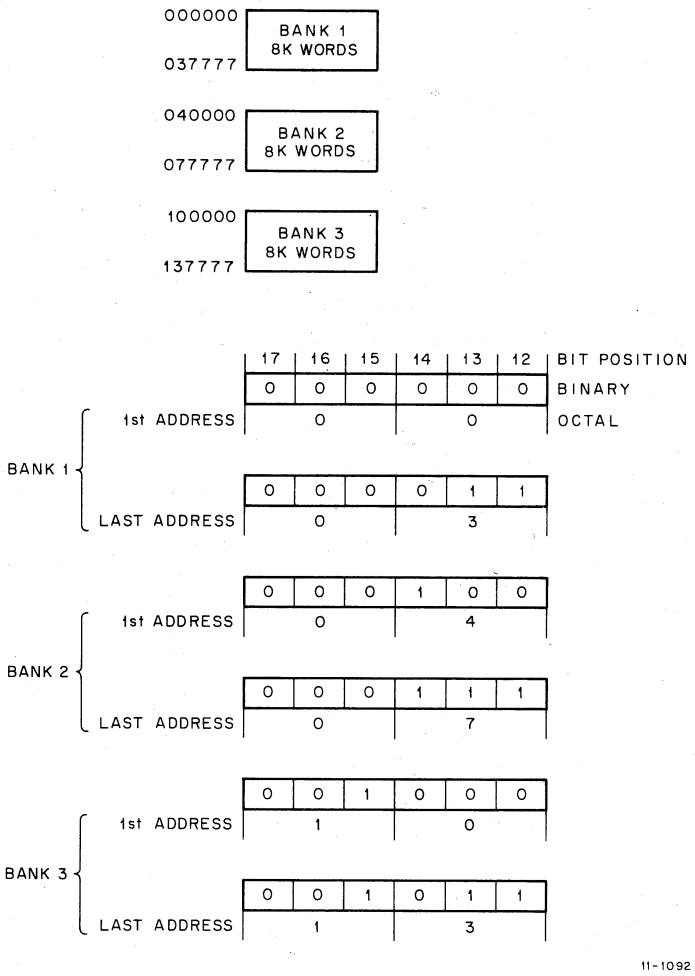


Figure 3-10 Address Assignments for Three Banks of 8K Words Each

3.3.3.2 **Device Selector** – The device selector is located on the Control Module (drawing G110-0-1, sheet 2). Address bits A⟨17:14⟩ are decoded in the device selector to provide the device selection signal D SEL H that is used in the control logic.

Each memory bank must have its own unique device address. Four jumpers (W2, W3, W4, and W6) in the device selector provide this capability. On drawing G110-0-1, sheet 2, all the jumpers are shown in place and the device selector responds only when high signals appear on the Unibus address lines A⟨17:14⟩. Some jumpers can be removed to allow the device selector to respond to a particular combination of high and low signals on these address lines.

All highs at the inputs of the 7380 Unibus receivers (E12 and E23) give lows at their outputs. Each receiver output goes to one input of a type 8242 exclusive-NOR gate. Because of jumpers W7 and W8, bit A14 is decoded. An additional receiver is used to sense BUS DC LO L and its output (E23 pin 14) is sent to an 8242 gate (E24 pin 5). BUS DC LO L is asserted only when the ac input voltage to the Power Supply drops below the specified limit.

The other input of the 8242 gates associated with bits A14, A15, A16, and A17 can be connected to +5V or ground depending on whether or not jumpers W2 through W4 and W6 are installed. The input is low (ground) with the jumper in; with the jumper removed, the input is high (+5V). Each 8242 gate is used as a digital comparator: its output is high only when both inputs are identical. The 8242 gates have open collectors and they are connected in common; therefore, the comparator output D SEL H is high only when all gates detect matched inputs (both lows or both highs).

An installed jumper requires a low signal at the output of the 7380 Unibus receiver. The 7380 is connected as an inverter so this signal is reflected as a high on the Unibus (logical 0 or asserted state for the Unibus). To configure the jumpers for a specific device address, find the binary equivalent of the assigned octal address and insert a jumper in each bit position that contains a 0. A specific jumper configuration is shown in Figure 3-11.

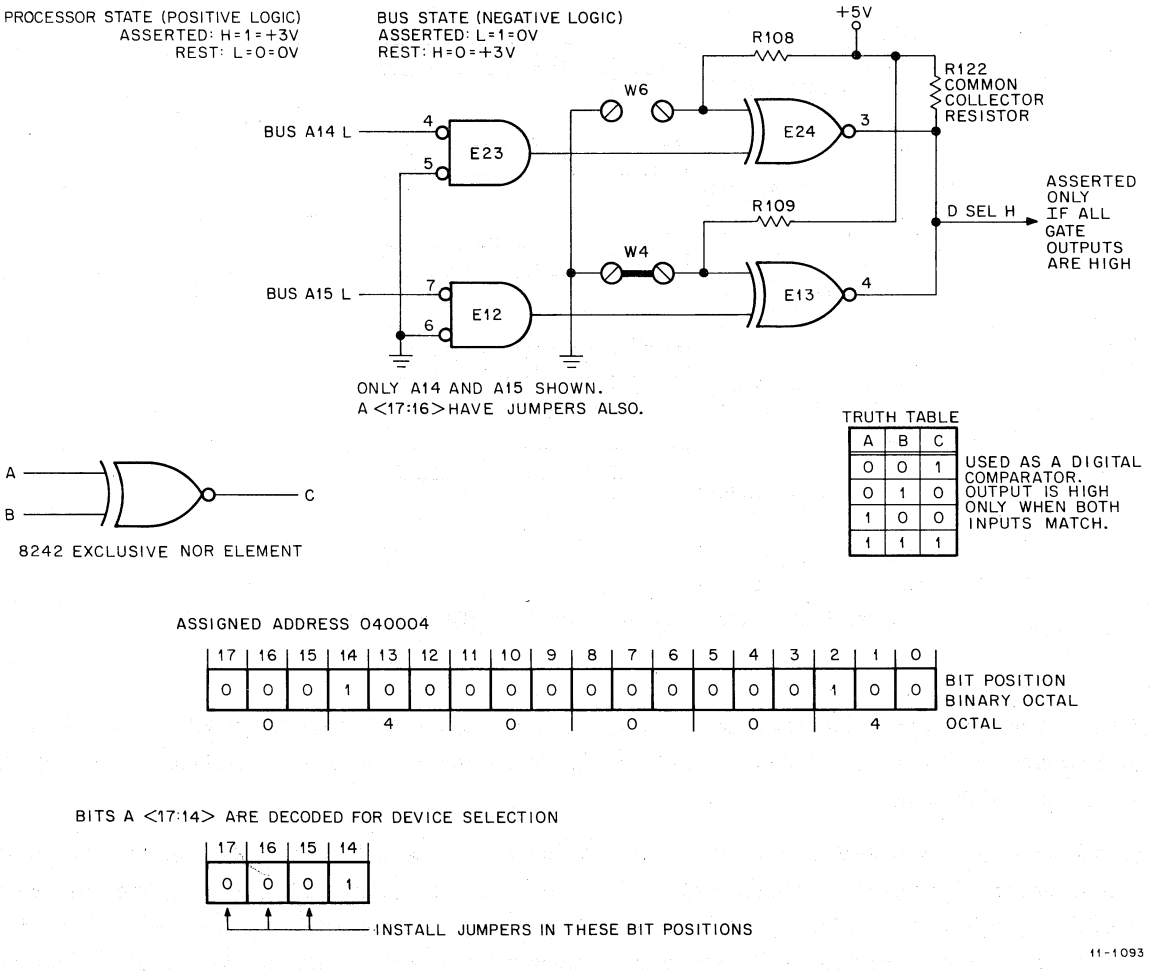
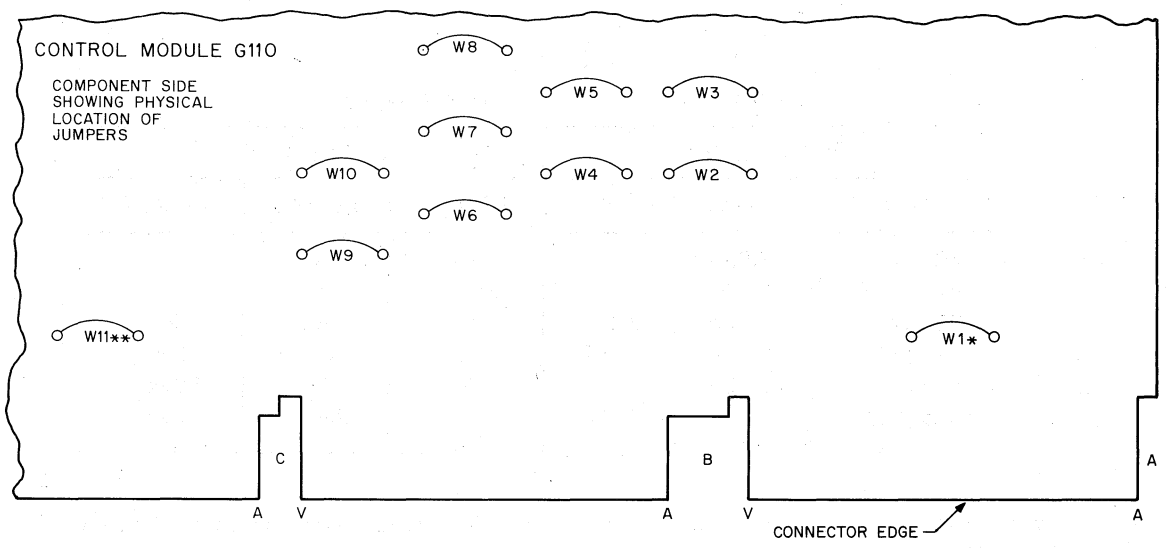


Figure 3-11 Jumper Configuration for a Specific Memory Address

In the 8K memory configuration, jumper W9 is removed and W10 is installed. The input of Unibus receiver E12 on G110 is +5V via resistor R107. This receiver output (pin 14) always remains low so that jumper W5 must remain installed to ensure a match on pins 12 and 13 of gate E13. The jumper configurations for memory systems up to 128K words are shown in Figure 3-12.

Memory Bank (words)	Machine Address (words)	Device Address Jumpers			
		W6 A14 or A01	W4 A15	W3 A16	W2 A17L
0–8K	000000–037776	In	In	In	In
8–16K	040000–077776	Out	In	In	In
16–24K	100000–137776	In	Out	In	In
24–32K	140000–177776	Out	Out	In	In
32–40K	200000–237776	In	In	Out	In
40–48K	240000–277776	Out	In	Out	In
48–56K	300000–337776	In	Out	Out	In
56–64K	340000–377776	Out	Out	Out	In
64–72K	400000–437776	In	In	In	Out
72–80K	440000–477776	Out	In	In	Out
80–88K	500000–537776	In	Out	In	Out
88–96K	540000–577776	Out	Out	In	Out
96–104K	600000–637776	In	In	Out	Out
104–112K	640000–677776	Out	In	Out	Out
112–120K	700000–737776	In	Out	Out	Out
120–128K	740000–777776	Out	Out	Out	Out



*Jumper W1 is for test purposes only. It must be installed for normal operation.

**Jumper W11 should be removed for normal operation. When installed the memory responds to DATI only, regardless of state of control lines C00 and C01.

NOTE:
Jumpers W5, W7, and W8 must remain in the factory installed positions.

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Figure 3-12 Device Decoding Guide

3.3.3.3 Word Selection – Word selection requires two levels of decoding. The word address bits are placed in the 13-bit word address register; some bits from the register output are combined in a gating network. The outputs from the gating network and some outputs directly from the register are used as inputs to a group of decoders (Figure 3-8). The outputs of the decoders select the proper X and Y read/write switches and drivers. The word selection logic is discussed in four parts as follows:

a. *Word Address Register and Gating Logic* – The word address register and gating logic are contained on the Driver Module (G231). The circuit schematic is shown in drawing G231-0-1, sheet 2. The register is composed of thirteen 74H74 dual D-type edge-triggered flip-flops. They are identified as E11, E12, E13, E14, E18, E19, and E20. The output (pin 3) of gate E9 provides a high signal on the preset input (pin 4 or pin 10) of each flip-flop which prevents direct presetting of the flip-flop. Direct clearing of each flip-flop is prevented by a high signal on the clear input (pin 1 or pin 13) via the output (pin 2) of gate E9. The register cannot be directly cleared or preset because its output responds only to the signal at its data (D) input. Address bits A⟨13:01⟩ are picked off the Unibus via type 7380 receivers (E15, E16, and E17). The receiver outputs are sent to the corresponding flip-flop D-inputs. The 8K memory requires J4 in and J3 out. The flip-flop (E11) associated with bit A01 receives its input from the device selector (drawing G110-0-1, sheet 2). The input signal is A01H which is obtained from bit A01 Unibus receiver for an 8K memory.

The register flip-flops are clocked synchronously by CLK 1 H from the control logic (drawing G110-0-1, sheet 2). Clocking occurs on the positive-going edge of CLK 1 H. The generation and timing of this clock signal is discussed in Paragraph 3.3.7. When the register is clocked, the outputs of flip-flops A01, A02, A04, A05, A07, A08, A10, and A11 are sent to the type 8251 X-Y line decoders on the Driver Module (drawing G231-0-1, sheets 3 and 4). The outputs of flip-flops A06, A12 and A13 are combined in a group of six type 74H10 NAND gates (three E22s and three E25s) which are enabled by the signal TSS H. Table 3-3 lists the states of flip-flops A06, A12, and A13 that are required to enable these gates. The outputs of flip-flops A03 and A09 are gated with the TDR H in high-speed, 2-input NAND gates and then applied to the decoders for the drivers only.

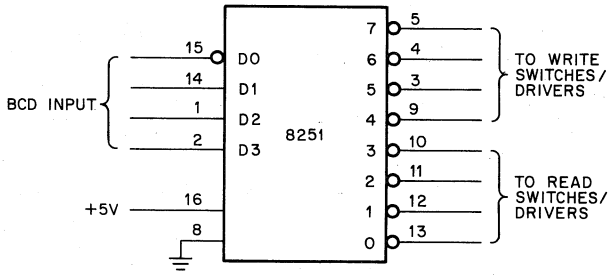
Table 3-3
Enabling Signals for Word Register Gating

Output Signals		Enabling Signals		
Gate	**Asserted Signal**	**FF A06**	**FF A12**	**FF A13**
E22 pin 12	(A06H) L	Set	X	X
E22 pin 8	A06L	Reset	X	X
E22 pin 6	(A12H · A13H) L	X	Set	Set
E25 pin 12	(A12L · A13H) L	X	Reset	Set
E25 pin 8	(A12H · A13L) L	X	Set	Reset
E25 pin 6	(A12L · A13L) L	X	Reset	Reset

The six signals listed in Table 3-3 are sent only to the X-Y line read/write switch decoders on the Driver Module.

TSS H is generated at the output (pin 3) of negative input OR gate E4 during a read or write operation. During a read operation, the enabling signal is produced at NAND gate E4, pin 8 by ANDing READ H and TNAR H. During a write operation, the enabling signal is produced at NAND gate E4, pin 6 by ANDing WRITE H and TWID H. READ, TNAR, and TWID are generated by the control logic on the Control Module. WRITE is the complement of READ (produced by inverter E6). READ H comes from the 1 output of read/write flip-flop E13 (drawing G110-0-1, sheet 2): READ H is produced when the flip-flop is set. When the read/write flip-flop is cleared, READ H is low and it is inverted by E6 to produce WRITE H.

b. *X- and Y-Line Decoding* – The basic decoding unit is a type 8251 BCD-to-decimal decoder. It converts a 4-bit BCD input code to a one-of-ten output; however, only eight outputs are used. Figure 3-13 shows an 8251 decoder and an associated truth table. The inputs are D0, D1, D2, and D3; they are weighted 1, 2, 4, and 8 with D0 being the least significant bit. The outputs are 0–7 and are mutually exclusive. The selected output is low and all others are high.



TRUTH TABLE

INPUTS				OUTPUTS							
D3	D2	D1	D0	0	1	2	3	4	5	6	7
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	X	X	X	1	1	1	1	1	1	1	1

X = IRREVELANT

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Figure 3-13 Type 8251 Decoder, Pin Designation and Truth Table

For the 8K memory, ten decoders are used: six for the X-axis and four for the Y-axis. Each decoder controls four read/write switch-pairs. Each pair is associated with a specific switch or driver. This switch matrix is combined with the stack X-Y diode matrix to allow selection of any location out of the total 8192 locations (see stack drawing DCS-H214-0-1 for interconnections). The X- and Y-line switches are first differentiated as switches and drivers. The drivers are those switches that are connected to the diode end of the stack. Drivers and switches are further differentiated by function: either read or write. Another differentiation is made by polarity: negative or positive, depending on the physical connection. Read drivers and write switches are connected to the current generator outputs and are considered positive; write drivers and read switches are connected to - 15V and are considered negative.

Figure 3-14 shows the decoders associated with Y-line read and write switches 4–7 and Y-line read and write drivers 4–7. (Refer also to the truth table in Figure 3-13.) In both decoders (E28 for switches and E8 for drivers), the signal to input D3 selects the block of switch pairs. This signal must be low for any output to be selected. The signal to input D2, which is READ L for all decoders, controls the selection of read or write switches/drivers. When READ L is low, outputs 0–3 can be selected; these are read switches and read drivers. When READ L is high, outputs 4–7 can be selected; these are write switches and write drivers. The four combinations of the states of inputs D0 and D1 select the particular switch/driver.

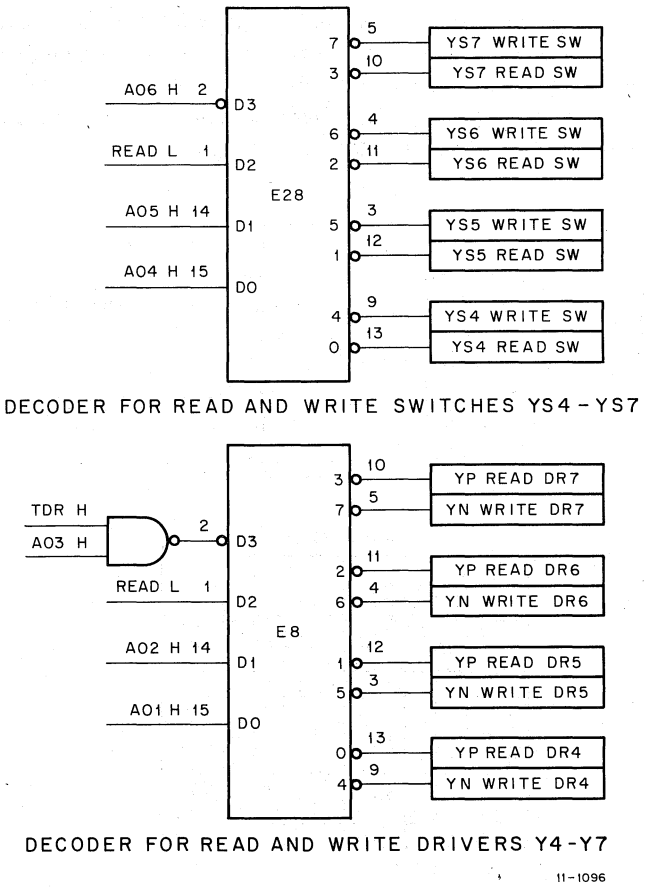

Figure 3-14 Decoding of Read/Write Switches and Drivers Y4–Y7

b. (cont) The four driver decoders (E3, E8, E43, and E46 on drawing G231-0-1, sheets 3 and 4) have a NAND gate connected to input D3. Signal TDR H is an input to each gate; therefore, the driver decoders cannot be enabled unless TDR H is high. This signal is generated on the Driver Module (drawing G231-0-1, sheet 2, coordinates A-B) by ANDing TWID H and READ H or TNAR H and WRITE H.

Each switch/driver is connected to the decoder output by means of a transformer-coupled base drive circuit. When the decoder output is at ground (low), the switch/driver is turned on; it is turned off when the decoder output is at +3.5V (high). The base drive circuit for write switch YS7 shown in Figure 3-15 is typical.

In this example, the decoder inputs have selected output 7 which is at ground. Current i_1 flows into this decoder output circuit from the +5V supply via resistor R11 and the primary winding (terminals 4 and 3) of transformer T8. The value of i_1 is determined by the value of R11 and the voltage reflected into the transformer primary (approximately 1.0V). An equal current, i_2, is induced in base-emitter circuit of write switch E29 which is connected to the transformer secondary winding (terminals 13 and 14). This current turns on E29. All the base current for E29 is provided by this circuit; i_3 is the collector current. When the decoder is turned off, its output pull-up transistor tries to drive the turn-off current i_4 in the opposite direction. This reverse current removes the forward bias from the base of E29 and turns it off. Capacitor C30 allows the decoder to pump reverse current i_4 into the transformer primary; it also speeds up turn-on current i_1. Diode D1 prevents reverse breakdown of the base-emitter junction of E29; it also protects the decoder output.

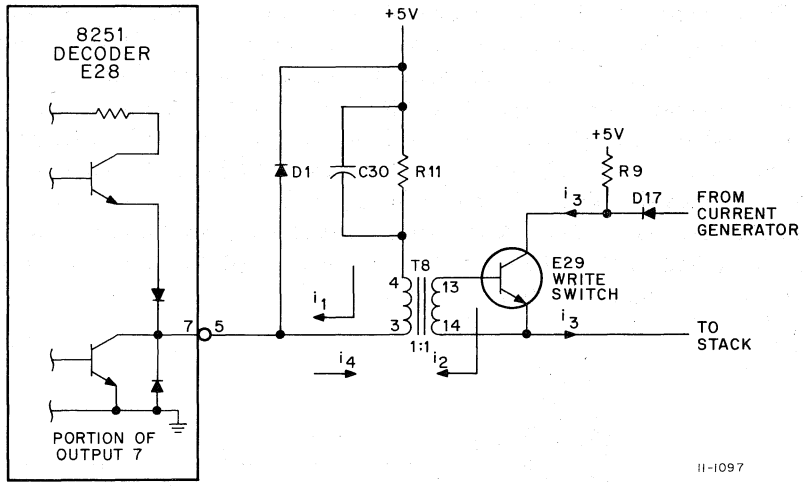

Figure 3-15 Switch or Driver Base Drive Circuit

c. *Drivers and Switches* – Drivers and switches direct the current through the X- and Y-lines in the proper direction as selected by the read and write operations.

For an 8K memory, sixteen pairs of read/write switches and eight pairs of read/write drivers are provided in the X-axis; eight pairs of read/write switches and eight pairs of read/write drivers are provided in the Y-axis. In conjunction with the stack diode matrix (drawing H214-0-1, sheet 2), one driver and any one of sixteen switches select sixteen lines in the X-axis; one driver and any one of eight switches select eight lines in the Y-axis. This allows selection of 128 lines in the X-axis and 64 lines in the Y-axis. This provides a 128 X 64 matrix that selects any location out of 8192 locations.

Figure 3-16 is one-fourth of a Y-selection matrix showing the interconnection of the diodes and the lines from the switches and drivers. It shows how four pairs of switches and drivers are connected to select sixteen locations. (Refer to drawing H213-0-1, sheet 2 for an extension of this method that uses eight pairs of switches and drivers to select 64 locations.)

Figure 3-16 shows four pairs of drivers and four pairs of switches for the Y-axis only; polarities are shown for convenience.

The diodes are identified to assist in associating them with the drivers and switches. Each line from a twin diode interconnection to a read/write switch pair passes through 64 cores and represents one line on each bit mat. Assume that a write operation is to be performed and the word address decoders have selected write switch WYS00 and write driver YNWD1. The Y-current generator sends current through write switch WYS00 (conventional flow) which puts a positive voltage on the anodes of diodes 03W, 02W, 01W, and 00W. The non-selected write drivers (YNWD3, YNWD2, and YNWD0) provide a positive voltage on the cathodes of their associated diodes (03W, 02W, and 00W respectively) which reverse biases them and prevents conduction. Write driver YNWD1, which has been selected, turns on and makes the cathode of diode 01W negative with respect to the anode which forward biases it. The diode conducts and allows current to flow to write driver YNWD1. A half-select current now flows through this line that links 64 cores per bit mat (1024 total for 16 mats).

Figure 3-17 is a simplified schematic of two pairs of switches and drivers interconnected with the core stack and current generator. Read/write switches YS07 and read/write drivers YD7 are used as examples. These switches and drivers are chosen for convenience. For a read or write operation, there are 64 switch/driver combinations available on the Y axis and 128 on the X axis. For a read operation, decoder E8 selects positive read driver E7 via transformer T3, and decoder E28 selects negative read

c. (cont) switch E26 via transformer T7. Both E7 and E26 are turned on when they are selected. E7 conducts and removes the reverse bias on diode D67 which allows current from the Y-current generator to flow through D67, E7, the associated matrix diode, and the cores on the selected line. After passing through the cores, the current flows through E26 and R27 to the –15V line. For a write operation, decoder E28 selects positive write switch E29 via transformer T8, and decoder E8 selects negative write drivers E10 via transformer T4. Both E29 and E10 are turned on. E29 conducts and removes the reverse bias on diode D17 which allows current from the Y-current generator to flow in the opposite direction through D17, E29, and the cores. After passing through the cores, the current flows through the associated matrix diode, E10, and R140 to the –15V line. Read current flow is shown as a solid line; a broken line shows write current flow.

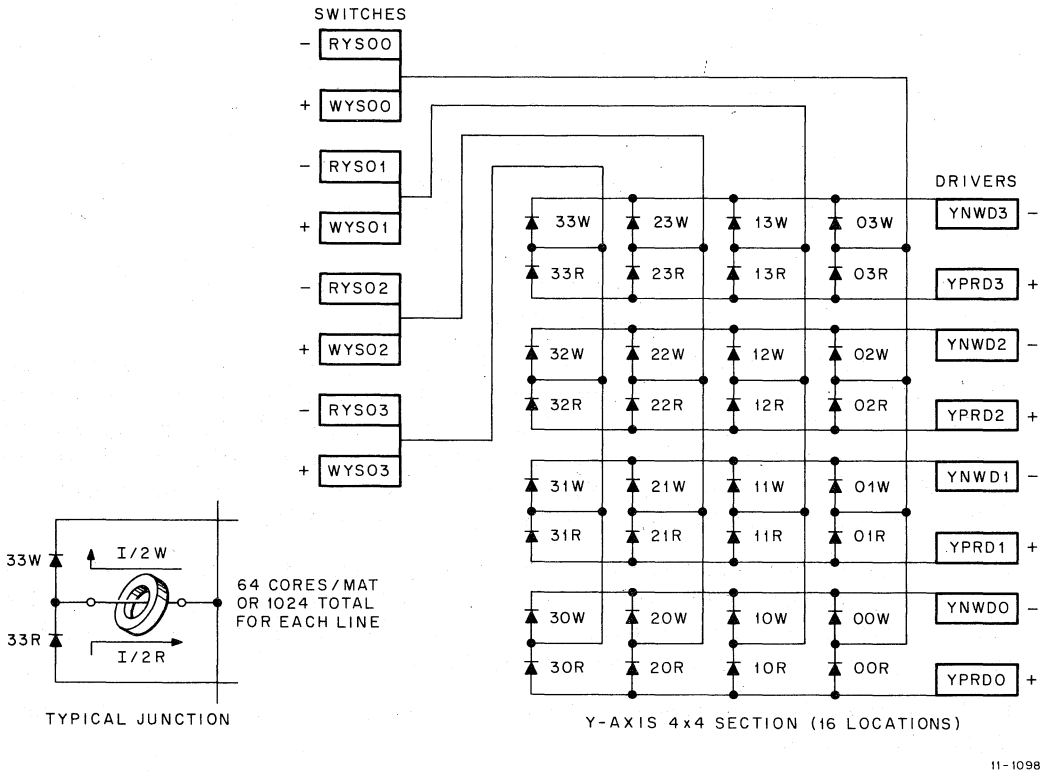

Figure 3-16 Y-Line Selection Stack Diode Matrix

d. *Word Address Decoding and Selection Sequence* – This paragraph takes a specific word address through the decoding and X- and Y-line selection sequence.

The word address is 017772 and it is assumed that a specific 8K memory bank has been selected. The binary equivalent of the address is shown below. A read operation is to be performed.

ADDRESS BITS A<17:00>

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BIT POSITION
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	BINARY
0			1			7			7			7			2			OCTAL

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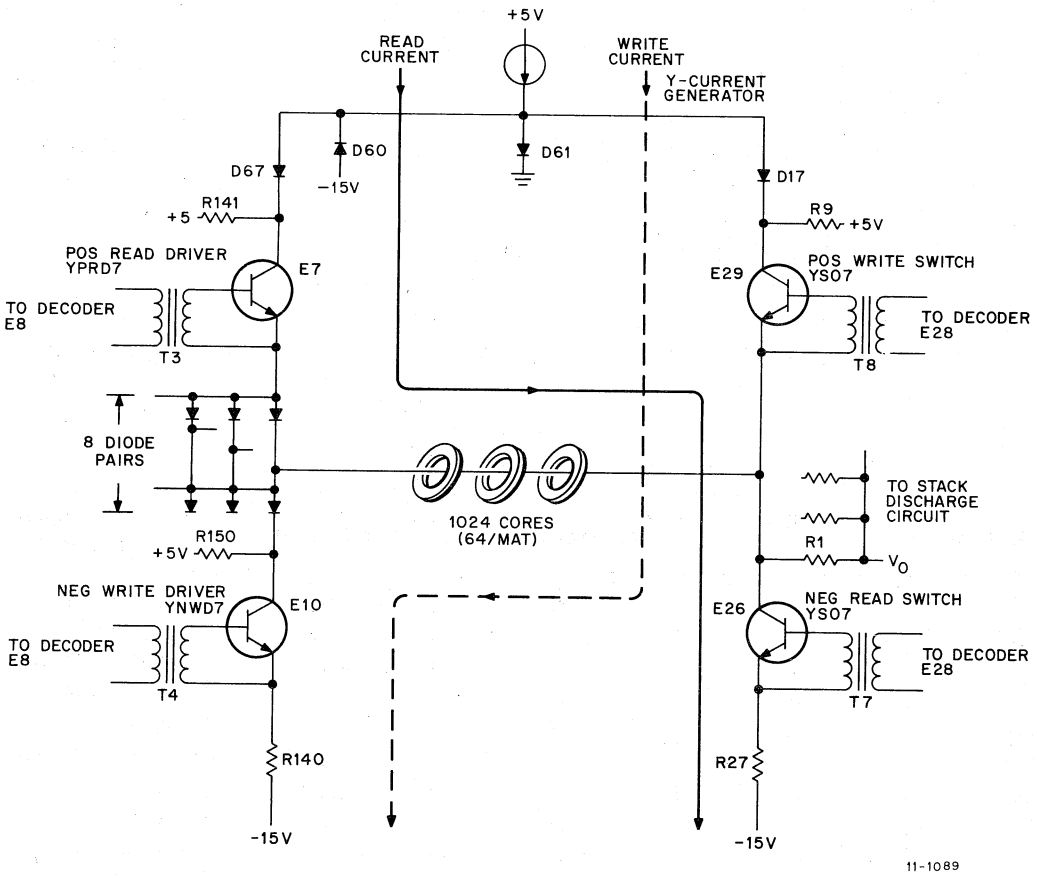


Figure 3-17 Typical Y-Line Read/Write Switches and Drivers

d. (cont) Bits A⟨13:01⟩ are used to decode the word address. Bit A01 is sent to the device selector (drawing G110-0-1, sheet 2) and appears at word address flip-flop E11 pin 2 as A01 H (drawing G231-0-1, sheet 2). Bits A⟨13:01⟩ are sent to the Unibus receivers which are inputs to the associated word address flip-flops. J3 is out and J4 is in. Table 3-4 shows the state of bits A⟨13:01⟩ and the decoding signals generated by the word address flip-flops after they are clocked.

The output signals from flip-flops A06, A12, and A13 are not used directly from the flip-flops. They are sent to gating logic (E22 and E25) and are ANDed with signal TSS H. In this case, only two out of a possible six signals are generated: A06H is low from E22 pin 12 and (A12H · A13L) L is low from E25 pin 8. These signals and the outputs from the other word address flip-flops are sent to the inputs of the type 8251 decoders to select the appropriate switches and drivers. READ L is an input to each 8251 decoder. A read operation is to be performed; therefore, READ L is low.

The decoders, switches, and drivers are shown in drawing G231-0-1, sheets 3 and 4. Using the decoding signals in Table 3-4 and the operating characteristics of the decoders, it is possible to determine which decoders have been selected for word address 017772. A decoder is selected only when its D3 input is low. In this case, the selected decoders are E34 and E46 for the X-line (drawing G231-0-1, sheet 3), and E23 and E8 for the Y-line (drawing G231-0-1, sheet 4). READ L is low and is sent to input D2 of each decoder; it selects read drivers and switches in this case. To verify this point, refer to the truth table and diagram in Figure 3-13. Decoder inputs D0 and D1 select the particular switch or driver as shown below.

d. (cont)

Decoder E34

D1 is high, D0 is high: Selects output 3 (pin 10) which is read switch XS07

Decoder E46

D1 is high, D0 is high: Selects output 3 (pin 10) which is read driver XPRD7

Decoder E23

D1 is high, D0 is high: Selects output 3 (pin 10) which is read switch YS03

Decoder E8

D1 is low, D0 is high: Selects output 1 (pin 12) which is read driver YPRD5

Table 3-4
Word Address Decoding Signals

Address Bit	Unibus Receiver Input	Receiver Output	Flip-Flop State	Flip-Flop Output Signals
A01	L	H	set	A01H = H
A02	H	L	reset	A02H = L
A03	L	H	set	A03H = H, A03L = L
A04	L	H	set	A04H = H
A05	L	H	set	A05H = H
A06	L	H	set	A06H = H, A06L = L
A07	L	H	set	A07H = H
A08	L	H	set	A08H = H
A09	L	H	set	A09H = H, A09L = L
A10	L	H	set	A10H = H
A11	L	H	set	A11H = H
A12	L	H	set	A12H = H, A12L = L
A13	--	–	reset	A13H = L, A13L = H

The last step is to follow the outputs of the drivers and switches to the stack diode matrix (drawing H213-0-1, sheet 2). For the X-line, the circuit is from driver XPRD7 to diode junction E7-11, across termination 35 to switch XS07. For the Y-line, the circuit is from driver YPRD5 to diode junction E4-9, across termination 15 to switch YS03. The terminations indicate the point on the stack printed-circuit board where the X- or Y-line is soldered. Physically, the wire that is connected across the termination is strung through 64 cores per bit mat (total of 1024 cores in series for 16-bit memory).

3.3.4 Read/Write Current Generation and Sensing

Aside from the addressing and control logic, four functional units are involved in generating current to switch the cores and detect their state. The X- and Y-line current generators supply the drive current (via switches and drivers); the inhibit drivers allow 0s to be written during a write operation; the sense amplifiers detect 1s during a read operation; and the memory data register (MDR) temporarily stores data to be written or data that has been read from the memory. This paragraph describes each functional unit and discusses their interrelation.

3.3.4.1 Read/Write Operations – The discussion of the read/write operations shows the interrelation of the current generator, inhibit drivers, sense amplifiers, and memory data register. Details of the operation of each functional unit are discussed in subsequent paragraphs. Several control signals are mentioned; however, details of their generation and timing are described in Paragraph 3.3.7.

For clarity, one data bit (D07) of the selected word is discussed and the text is referenced to Figure 3-18, which is a simplified block diagram. Detailed logic for the MDR, Unibus receivers and drivers, sense amplifiers, and inhibit drivers for all 16 data bits is shown on drawings G110-0-1, sheets 3 and 4.

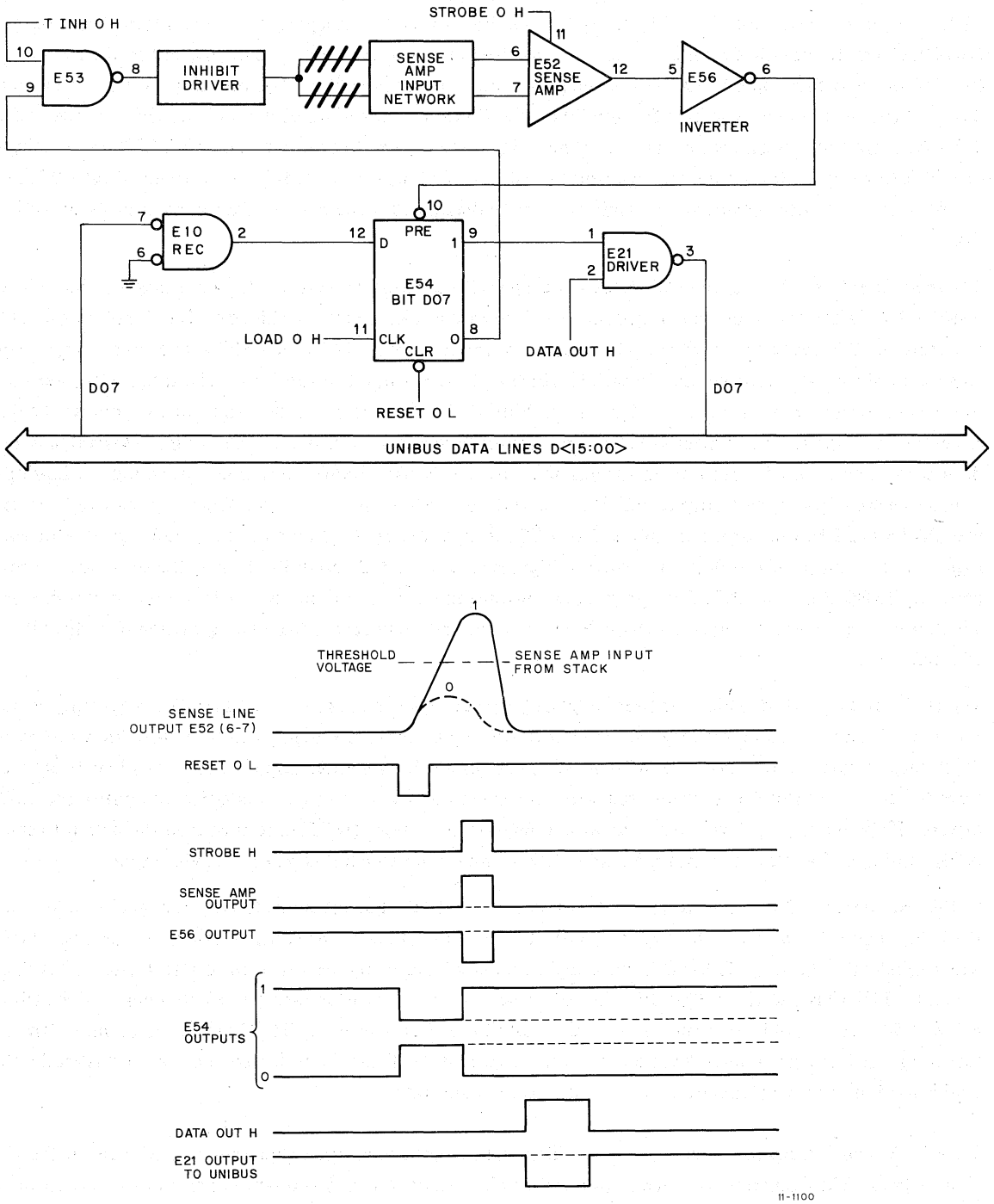


Figure 3-18 Interconnection of Unibus, Data Register, Sense Amplifier, and Inhibit Driver

During a read operation, half-select currents flow in the X- and Y-lines for the selected word in each bit mat. These currents flow opposite to the write currents; therefore, cores in the 1 state are switched to the 0 state and cores in the 0 state are unchanged. Switching the core from the 1 state to the 0 state induces a voltage pulse in the sense winding. This pulse is detected by sense amplifier E52 as a differential voltage on input pins 6 and 7 that exceeds the threshold reference voltage. This pulse is amplified and when STROBE 0H is generated at pin 11 the output of sense amplifier E52 goes high. Just prior to the strobe signal, the control logic generates RESET 0 which clears (resets) flip-flop E54. The sense amplifier output is inverted by E56 and sent to the preset input (pin 10) of MDR flip-flop E54. A low on the preset input sets the flip-flop; its 1 output (pin 9) is a high and its 0 output (pin 8) is a low. The high from pin 9 of the flip-flop is sent to input pin 1 of the Unibus driver E21. The other input to this gate is the data out signal. When the control logic generates DATA OUT H, the output of E21 is low (logical 0 for memory logic and logical 1 for Unibus logic). This is the read-out of bit D07 and it is sent to the requesting device via the Unibus. Timing diagrams for the sense operation are also shown in Figure 3-18.

The read operation is destructive: all cores at the specified location are now 0. The data that was read must be restored by a write operation which immediately follows the read operation. Flip-flop E54 is still in the set state; therefore, its 0 output (pin 8), which is low, is sent to input pin 9 of NAND gate E53. The control logic generates the inhibit driver control signal TINH0 H which is the other input to gate E53. The gate is not asserted (pin 8 is high) and the inhibit driver is not turned on. With no inhibit current in the inhibit line to oppose the half-select Y-line current, a 1 is written back into the appropriate cores. In this example, if bit D07 is a 0 in core, it does not switch during the read operation and the output of sense amplifier E52 does not go high. Flip-flop E54 remains cleared (reset); its 1 output (pin 9) is low and its 0 output (pin 8) is high. When the control logic generates DATA OUT H, the output of Unibus driver E21 is high (logical 1 for memory logic and logical 0 for Unibus logic). The 0 output of flip-flop E54, which is high, is sent to NAND gate E53. During the subsequent write operation, TINH0 H is generated. This produces a low output signal at E53 pin 8 to activate the inhibit driver which produces a current that opposes the Y-line current and prevents a 1 from being written into this bit of the selected word.

The read/write operation which has been discussed is a read/restore operation (DATI). The requesting device wants to read a word from memory and, as an internal requirement, the memory must restore the word by writing it back in core. In this case, the MDR flip-flops are preset by the sense amplifier outputs when 1s are read from the core. The flip-flop outputs are used in the subsequent write (restore) operation to control the inhibit drivers. If the requesting device wants to write a word into memory (DATO), it must load the data into the MDR flip-flops. The device asserts the data on the Unibus from which it is picked off via Unibus receivers.

In this example, bit D07 is sent to pin 7 of Unibus receiver E10. The bit is inverted by the receiver and sent to the D-input (pin 12) of flip-flop E54. At the start of the DATO cycle, the control logic generates LOAD 0 H which clocks the flip-flop. If the D-input is high, E54 is set and its 0 output is low. Control gate E53 is not asserted by TINH0 H and the inhibit driver is not turned on. A 1 is written into the selected core. If the D-input is low, E54 is reset and its 0 output is high. Control gate E53 is asserted by TINH0 H and the inhibit driver is turned on. A 0 is written into the selected core. Because RESET and STROBE are inactive in this mode, the read is used only to magnetically clear the cores to the zero state.

3.3.4.2 **X- and Y-Current Generators** – Two identical current generators are provided: one each for the X- and Y-drive lines. They generate the current pulses that are used during read and write operations to switch the cores. The current generators and associated reference voltage supply are shown in drawing G231-0-1, sheet 2. This discussion refers to Figure 3-19 which shows the Y-current generator and reference voltage supply.

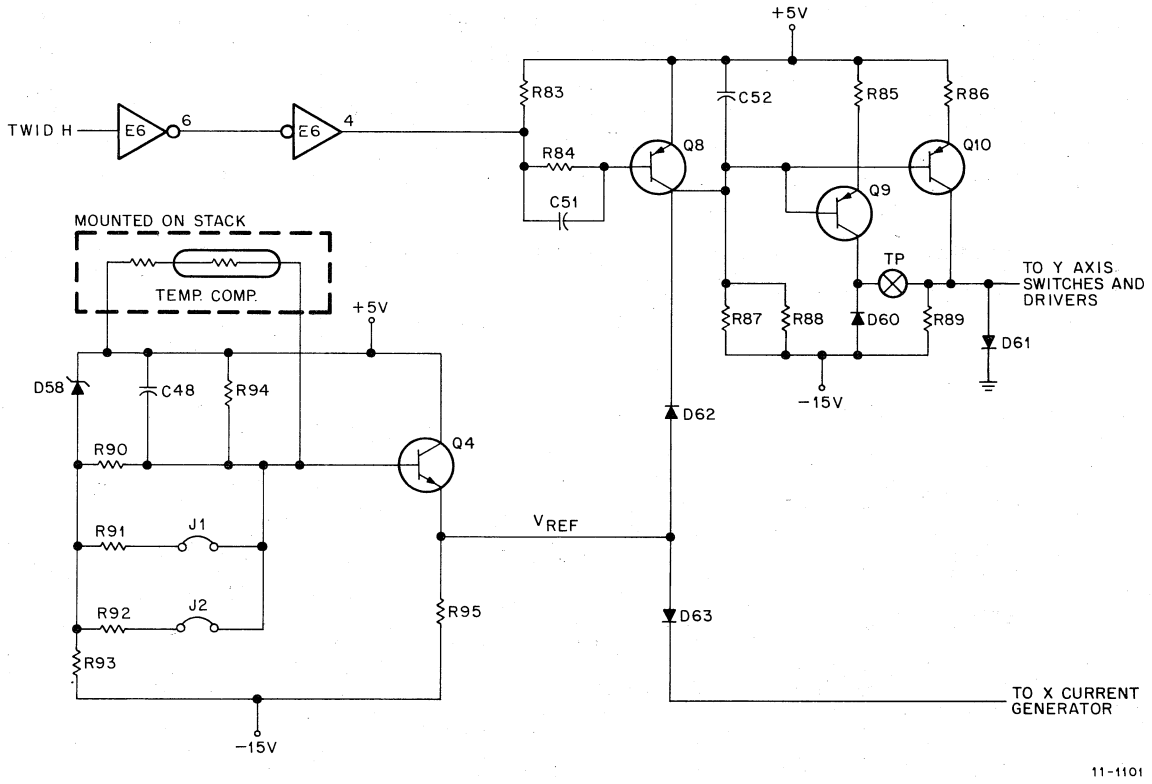


Figure 3-19 Y-Current Generator and Reference Voltage Supply

Optimum core switching requires repeatable current pulses of constant amplitude with a linear rise time. The current generator and reference voltage circuit provide current pulses that meet these requirements. The amplitude of the output current pulse is determined by the reference voltage circuit; the rise time is determined by an RC circuit in the current generator; and pulse duration is determined by the length of the triggering pulse TWID H.

During the quiescent state of the current generator, input transistor Q8 is on; its collector voltage is 4.7V and is connected to the cathode of diode D62 which reverse biases it. The anode of D62 is connected to the emitter of transistor Q4 which is the output of the reference voltage circuit. In this state, D62 blocks the output from the reference voltage circuit to the current generator. With Q8 on, both output transistors Q9 and Q10 are turned off; the current generator is off.

Operation of the current generator is triggered by a high TWID H signal from the control logic. TWID H is double inverted by two E6 inverters and sent to the base of Q8 which turns it off. When Q8 is cut off, capacitor C52 starts charging. This provides base drive to output transistors Q9 and Q10 and they start to conduct. With Q8 off, its collector goes negative until it reaches the forward bias level of D62 which is the value of the reference voltage minus the voltage drop across D62. The rise time of the current pulse is determined by the time constant of C52, R87, and R88. The amplitude of the pulse is determined by the value of the reference voltage. When TWID H goes low again, the current generator is turned off and the output pulse is terminated.

A resistor network in the base circuit of Q4 in the reference supply is used to set the amplitude of the current generator to approximately 410 mA. The total resistance of parallel network R90, R91, and R92 is changed by

the configuration of jumpers J1 and J2. The amplitude of the current generator output pulse is factory set as close as possible to 410 mA at 25°C. It should not be changed in the field.

The base circuit of Q4 is temperature compensated by a resistor and thermistor that are mounted on the stack. This ensures that the amplitude of the current generator output pulse remains within specified tolerances over the temperature range of 0°C to 50°C. This temperature compensation is approximately -0.8 mA/°C.

3.3.4.3 **Inhibit Driver** – A detailed schematic of the inhibit driver for bit D07 is shown in Figure 3-20; it is typical of all 16 inhibit drivers (drawing G110-0-1, sheets 3 and 4).

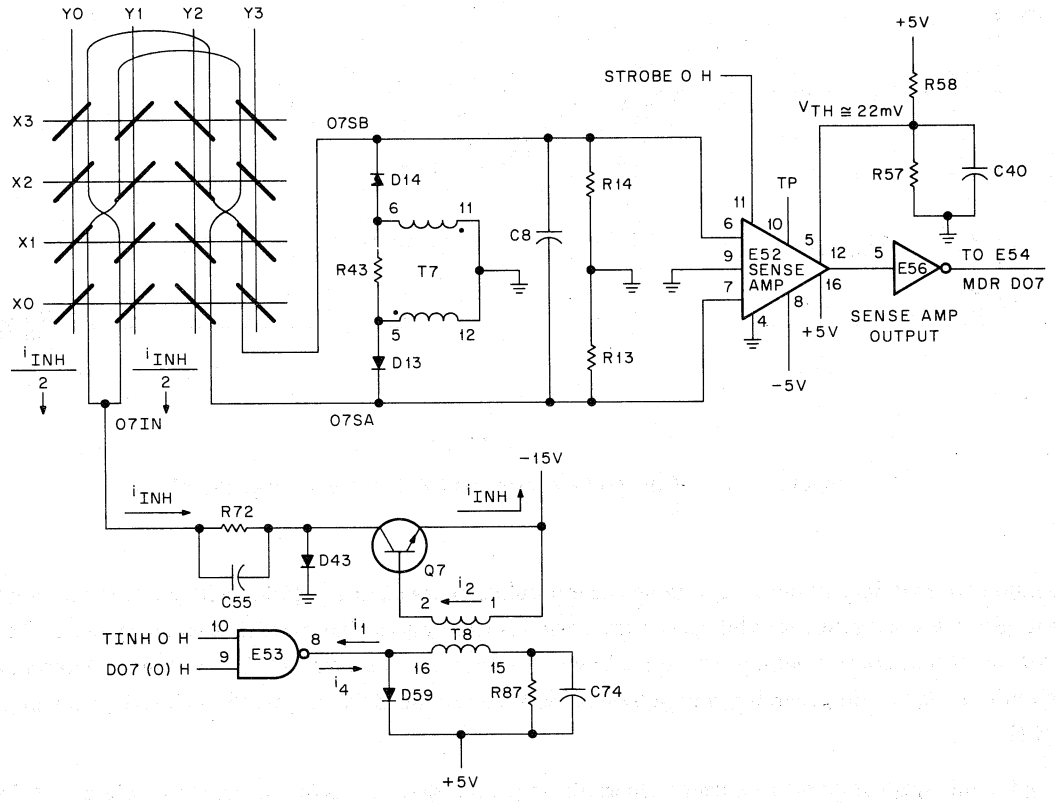


Figure 3-20 Sense Amplifier and Inhibit Driver

When the inhibit driver is off, none of the currents shown in the schematic are flowing. Transistor Q7 is held off by the negative voltage on its base. The output of NAND gate E53 goes low (ground) when this inhibit driver is selected. Current i_1 flows into the output circuit of E53 from the +5V supply via resistor R87 and the primary winding (terminals 15 and 16) of transformer T8. An equal current is induced in the base-emitter circuit of Q7 which is connected to the transformer secondary winding (terminals 1 and 2). This base current overcomes the reverse bias voltage and turns on Q7. Current i_1, and therefore induced current i_2, is determined by resistor R87 and the reflected base-emitter voltage V_{be} of Q7. When Q7 is turned on, current flows from ground through Balun transformer T7, isolation diodes D13 and D14, and the sense/inhibit winding to the common inhibit

terminal (07IN). The Balun transformer balances the two inhibit half currents. At terminal 07IN, the full inhibit current flows through resistor R72 and Q7 to –15V. The value for inhibit current is calculated as follows:

$$i_{inh} \cong \frac{15V - V_{ce\ sat\ Q7} - V_{be\ diodes}}{R72 + R_{core\ mat}}$$

$$\cong \frac{15 - 0.8 - 1.2}{13 + 4.5} \cong \frac{13}{17.5} \cong 740\ mA$$

Each leg of the sense/inhibit sees half the inhibit current: approximately 370 mA. Capacitor C55 decreases the rise time of the current.

The inhibit driver is turned off when the output (pin 8) of gate E53 goes from low to high. At turn-off time, the back emf caused by the stack inductive reactance tries to drive the collector of Q7 highly positive; however, diode D43 clamps this voltage to ground. When the output of E53 goes high (approximately +3.2V), its output pull-up transistor (an integral part of the gate circuit) tries to drive the turn-off current i_4 in the opposite direction through the transformer primary winding. An equal current induced in the secondary winding removes the forward bias from the base of Q7 and turns it off. With Q7 off, all dynamic current flow ceases in the circuit and the negative voltage on the base of Q7 keeps it turned off until the output of gate E53 goes low again.

Capacitor C74 allows the gate to pump reverse current i_4 into the transformer primary; it also helps to decrease the turn-on time of Q7. Diode D59 prevents reverse breakdown of the base-emitter junction of Q7.

3.3.4.4 Sense Amplifier – A detailed schematic of the sense amplifier circuit for bit D07 is shown in Figure 3-20; it is typical of all 16 sense amplifier circuits (drawing G110-0-1, sheets 3 and 4). It consists of the sense amplifier, terminating network for the sense/inhibit winding, and threshold voltage network.

The sense amplifier input (E52 pins 6 and 7) is across the sense/inhibit winding (points 07SB and 07SA). Resistors R13 and R14 are matched to terminate the sense/inhibit line in the desired impedance. Practically speaking, during the sense operation, the inhibit driver connection is an open circuit through the driver transistor Q7. The effect of the inhibit driver circuit, Balun transformer T7, and isolation diodes D13 and D14 can be ignored during the sense operation, because the diodes are reverse biased.

Sense amplifier E52 is one-half of a dual IC package (type 7528). A simplified block diagram of the package is shown in Figure 3-21. The two identical circuits are marked 1 and 2. Each one consists of a preamplifier and sense amplifier. The output of the preamplifier is available as a test point to observe the amplified core signal and to facilitate accurate strobe timing. Both circuits share a reference voltage (or threshold voltage) amplifier (pins 4 and 5). In this application, pin 4 is grounded and a positive threshold voltage of approximately 20 mV is supplied to pin 5. This voltage is obtained from the +5V supply through resistor voltage divider R57 and R58; C40 is a bypass capacitor. Operation of the sense amplifier is discussed in Paragraph 3.3.4.1.

3.3.4.5 Memory Data Register – The memory data register (MDR) is a 16-bit flip-flop register that is used to store a word after it is read out of the memory, or to store a word from the Unibus prior to its being written into the memory. It is composed of eight 74H74 dual high-speed D-type flip-flops. Bits D00–D07 are shown in drawing G110-0-1, sheet 3 and are identified as E54, E57, E60, and E63; bits D08–D15 are shown in drawing G110-0-1, sheet 4 and are identified as E42, E45, E48, and E51.

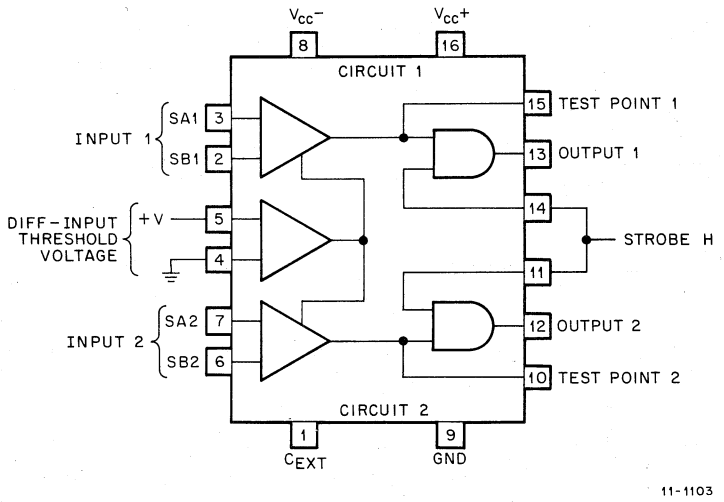


Figure 3-21 Type 7528 Dual Sense Amplifiers with Preamplifier Test Points

At the start of a memory operation, the MDR is cleared directly via the CLEAR input (pin 1 or pin 13) of each flip-flop; the clear signal is RESET 0 L for bits D00–D07 and RESET 1 L for bits D08–D15.

The operation of the MDR during a read/restore operation (DATI) and a write operation (DATO) is discussed in Paragraph 3.3.4.1.

3.3.5 Stack Discharge Circuit

The stack discharge circuit assists the stack capacitance in recovering and shortens the rise time of the stack current. It also reduces unwanted currents in the seven unselected lines associated with the selected driver.

Figure 3-22 shows the stack discharge circuit. Its output is taken from the emitter of transistor Q2 and goes to the junction of each X and Y read/write switch pair via a resistor. This common interconnection is labeled V_0. It is desired that $V_0 \cong 0V$ (ground) during a read operation, and $V_0 \cong -15V$ during a write operation. The effective stack capacitance associated with each line is shown as C_{stack}.

During a write operation, READ H is low; it is inverted and ANDed with TWID H at NAND gate E4. The low output (pin 11) of E4 is inverted by E6 and sent to the cathode of diode D51 which reverse biases it. The emitter of Q1 becomes more positive, overcomes the constant positive base bias, and turns on transistor Q1. When Q1 conducts, it provides base drive for Q3 which also turns on. When Q3 conducts, it reduces the base drive on Q2 and it turns off. The emitter voltage of Q2 goes to approximately –14V which is V_0 on the switch node for the stack. Diode D57 prevents hard saturation of Q3. Diode D55 holds Q2 off. During a write operation, $V_0 \cong -14V$ and the stack discharge circuit is considered to be turned on (input transistor Q1 is on).

During a read operation, READ H is high; it is inverted and ANDed with TWID H at NAND gate E4. The gate is not asserted and its output (pin 11) is high. This signal is inverted by E6 and sent to the cathode of diode D51 which forward biases it. The voltage on the emitter of Q1 produced by the current through R77 and D51 is not enough to overcome the constant positive bias and Q1 is turned off. With Q1 off, Q3 loses its base drive and turns off. Now, D55 cannot hold Q2 off. As long as the stack capacitance is charged negatively, base current exists for Q2 and it remains on. The stack capacitance now charges in the positive direction until it reaches

ground potential. During a read operation, $V_0 \cong 0V$ and the stack discharge circuit is considered to be off (input transistor Q1 is off).

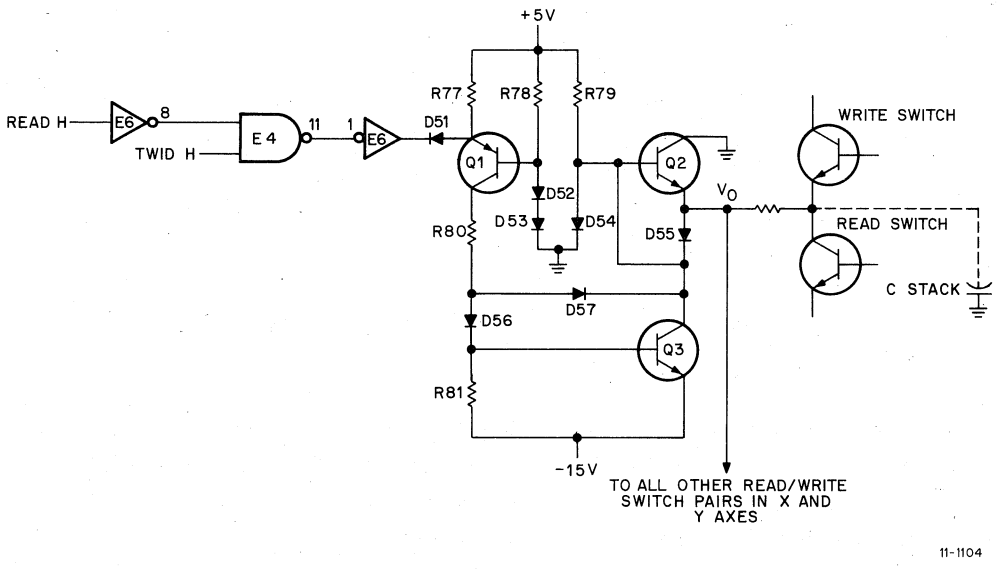


Figure 3-22 Stack Discharge Circuit

To see how the stack discharge circuit reduces unwanted currents on the seven unselected lines associated with the selected driver, see Figure 3-17.

During a read operation, the stack discharge circuit is off and $V_0 \cong 0V$. The current generator drives the read driver node of the stack towards ground; the current generator output is clamped to ground by diode D61 (Figure 3-19). The anodes of the eight read diodes are at ground. The stack discharge circuit is on and the cathodes of the seven unselected diodes are also at ground which back biases them; therefore, they are off. The read switch pulls the cathode of the selected line towards –14V which forward biases it and allows conduction through the diode. Current flows only through the selected line. Reverse biasing of the diodes in the unselected lines prevents current from flowing between the unselected nodes and the selected read driver.

The stack discharge circuit performs the same task during the write operation by back biasing the anodes of the diodes in the unselected lines with - 14V.

3.3.6 DC LO Circuit

A circuit on the Driver Module (drawing G231-0-1, sheet 2) opens the - 15V supply line to the current generators when power is interrupted to the Power Supply. When power is interrupted, the +5V supply is lost and the operation of all logic is indeterminate. In this state, it is necessary to cut off the - 15V supply to the X- and Y-line current generators to prevent them from destroying stored data. The circuit that performs the - 15V cut off is called the DC LO circuit (Figure 3-23).

The - 15V supply for the X- and Y-line current generators passes through transistor Q7 in the DC LO circuit. Q7 must be turned on for the - 15V to reach the current generators.

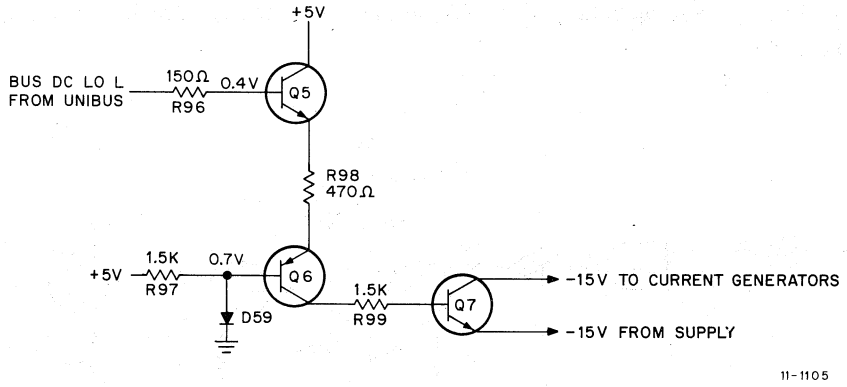


Figure 3-23 DC LO Circuit, Schematic Diagram

The circuit monitors BUS DC LO L from the Power Supply via the Unibus. This signal is sent to the base of transistor Q5. When power is on, BUS DC LO L is high (not asserted). The voltage across R96 forward biases Q5 and it turns on, which turns on Q6. The conduction through Q5 and Q6 forward biases Q7, which turns it on. The - 15V flows through Q7 to the X- and Y-line current generators.

When power is interrupted, BUS DC LO L goes low (asserted). Q5 is now reverse biased and it turns off, which turns off Q6. With Q5 and Q6 off, Q7 is also turned off which opens the - 15V line to the current generators. This circuit still functions when BUS DC LO L is asserted even if the +5 supply drops to 0.

3.3.7 Operating Mode Selection Logic

When the memory is addressed by the master device, one of four bus transactions is selected. The transaction (or operation) selected is determined by the states of control bits C01 and C00 and address bit A00 as placed on the Unibus by the master device. Table 3-5 shows the states of these bits for each transaction.

Table 3-5
Selection of Bus Transactions

Transaction	Mnemonic	Mode Control		Control A00	Function
		C 01:00	Octal		
Data In	DATI	00	0	X	Data from memory to master. Memory performs read and restore operations.
Data In, Pause	DATIP	01	1	X	Data from memory to master. Restore operation is inhibited. Must be followed by DATO or DATOB. Read operation is inhibited.
Data Out	DATO	10	2	X	Data from master to memory (words).
Data Out, High Byte	DATOB	11	3	1	Data from master to memory. High byte on data lines D⟨15:08⟩.
Data Out, Low Byte	DATOB	11	3	0	Data from master to memory. Low byte on data lines D⟨07:00⟩.

The logic that decodes the mode and byte control bits is shown in drawing G110-0-1, sheet 2; it appears at the bottom of the sheet and is identified as the byte masking logic. Bits BUS C01, BUS C00, and BUS A00 are taken from the Unibus to three E29 receivers. One input of each gate associated with C01 and C00 is connected to the output of the PROTECT LOW gate (E29 pin 3). Both inputs to this gate are tied to +5V so that its output is always low. For troubleshooting purposes, a jumper (W11) can be installed that makes the gate output high, which allows only DATI operations to be performed regardless of the states of bits C01 and C00. This jumper hardwires the memory as a read-only device.

The outputs of the three E29 receivers (C01, C00, and A00) are sent to the byte masking logic to generate LOAD 0 H and LOAD 1 H and to qualify a group of gates, which are enabled by control signals to generate RESET 0 L, RESET 1 L, STROBE 0 H, STROBE 1 H, and DATA OUT H. The logic also conditions the D-input of the PAUSE flip-flop (E4 pin 12) to allow it to be set or reset. It also applies conditioning signals to the wired-AND that provides the clocking signal to the Slave Sync (SSYN) flip-flop. The PAUSE flip-flop and the SSYN flip-flop are part of the control logic.

The signals generated for each bus transaction are shown in Table 3-6. The memory operational sequences are discussed in subsequent paragraphs. To avoid confusion in interpreting the transactions listed in Table 3-6, the purpose of the PAUSE flip-flop is discussed briefly.

During DATIP, the PAUSE flip-flop is set during the read operation which inhibits the restore (write) operation. The DATIP must be followed by a DATO or DATOB on the same address. The DATO or DATOB that follows a DATIP is shorter than a standard DATO or DATOB because the initial read operation is eliminated. In Table 3-6, the suffix PAUSE L identifies the standard transactions; the suffix PAUSE H identifies the DATO and DATOB transactions that must follow a DATIP.

3.3.8 Control Logic

The control logic generates the precisely timed signals that initiate and stop the memory operations that are requested as a result of the decoding of the bus transaction. The heart of the control logic is the delay line timing circuit. For better understanding, the timing circuit, slave sync circuit, pause/write restart circuit, and strobe generating circuit are described separately. Then, each bus transaction is discussed in detail. The discussion is to the detailed logic level but the signals are not traced through each component. The text is referenced to logic drawing G110-0-1, sheet 2, and the timing diagrams in drawing MM11-L-3.

3.3.8.1 **Timing Circuit** – The heart of the memory control logic is the timing circuit. When activated, it generates a series of precisely timed signals that control memory operation. The major component of the timing circuit is a delay line (DL1) with multiple 25-ns taps (drawing G110-0-1, sheet 2). The delay line outputs are gated to produce the control signals. Figure 3-24 shows the timing of the delay line outputs and the timing for the control signals obtained by gating these outputs. A brief statement of the function of each control signal is included. Absolute timing is obtained from the engineering timing diagram (drawing MM11-L-3).

The discussion is referenced to Figure 3-24 and the control logic drawing G110-0-1.

When the system is turned on, the processor asserts BUS INIT L on the Unibus. This initializing signal is sent to pins 6 and 7 of bus receiver E7. It is inverted by E7 to produce a high which is sent to pins 9 and 10 of the memory select reset (MSEL RESET) gate E16. The output (pin 8) of E16 is a low which is used to clear (reset) MSEL flip-flop E2 via the 100-ns delay DL3. The output of E7 is also inverted by E18 to provide a low which clears read/write (R/W) flip-flop E3. The output of E7 is also inverted by E15 to provide a low which clears PAUSE flip-flop E4. The low output of E15 is double inverted by two E38 gates to clear the DEL flip-flop E28. The master places the address, mode control state, and data (if required) on the Unibus. The device address is decoded and DSEL H is generated and sent to pin 13 of E1 which is one of four input signals (pins 10, 11, 12,

and 13). Pin 11 is high via the 0-output of MSEL flip-flop E2. SSYN flip-flop E4 is preset and it makes pin 10 of E1 high via its 1-output (pin 5). When the master asserts BUS MSYN L to bus receiver E23, pin 12 of E1 is high also. The output of E1 (pin 8) goes low which is sent to pin 13 of E5, pins 4 and 5 of E14, and pin 1 of delay line DL2. E14 inverts the low from E1 to start the positive CLK 1 H pulse. DL2 provides a 30-ns delay for the low signal from E1 which is inverted by E15 to start the positive CLK 2 H pulse. The output (pin 3) of DL2 is sent to the preset input (pin 4) of MSEL flip-flop E2. This low signal directly sets E2 and pin 6 goes low which is fed back to pin 10 of E1 to disable it. The output (pin 8) of E1 is now high and this signal terminates both clock pulses (CLK 1 H and CLK 2 H) via gates E14 and E15. These clock pulses are approximately 50-ns wide.

Table 3-6
Generation of Memory Operating Signals

Mode	Byte Control A00	Mode Control		State of PAUSE Flip-Flop	Signals Generated							Operational Sequence
		C01	C00		STROBE 0	STROBE 1	RESET 0	RESET 1	LOAD 0	LOAD 1	DATA OUT H	
DATI	X	0	0	Reset	X	X	X	X			X	Read-restore.
DATIP	X	0	1	Reset-Set	X	X	X	X			X	Read-pause. Restore inhibited by PAUSE flip-flop.
DATO PAUSE L	X	1	0	Reset					X	X		Clear-write.
DATO PAUSE H	X	1	0	Set					X	X		Write. Must follow DATIP.
DATOB PAUSE L	0	1	1	Reset		X		X	X			Clear-write selected byte 0. Clear-restore nonselected byte 1.
DATOB PAUSE H	0	1	1	Set		X		X	X			Write selected byte 0. Restore nonselected byte 1. Must follow DATIP.
DATOB PAUSE L	1	1	1	Reset	X		X			X		Clear-write selected byte 1. Clear-restore nonselected byte 0.
DATOB PAUSE H	1	1	1	Set	X		X			X		Write selected byte 1. Restore nonselected byte 0. Must follow DATIP.

Gate E5 also inverts the low from E1 because pin 12 (WRITE RESTART L) of E5 is high. The positive transition at the output (pin 11) of E5 clocks delay (DEL) flip-flop E28 which sets it. Pin 5 of E28 is high and it is connected to pins 1 and 2 of DL1 driver gate E34. The low from the output (pin 3) of E34 is the input to delay line DL1. This signal remains low for approximately 225 ns until DEL flip-flop E28 is cleared by DELAY FF RESET. This provides a negative pulse that propagates through the delay line and can be picked off at 25-ns intervals.

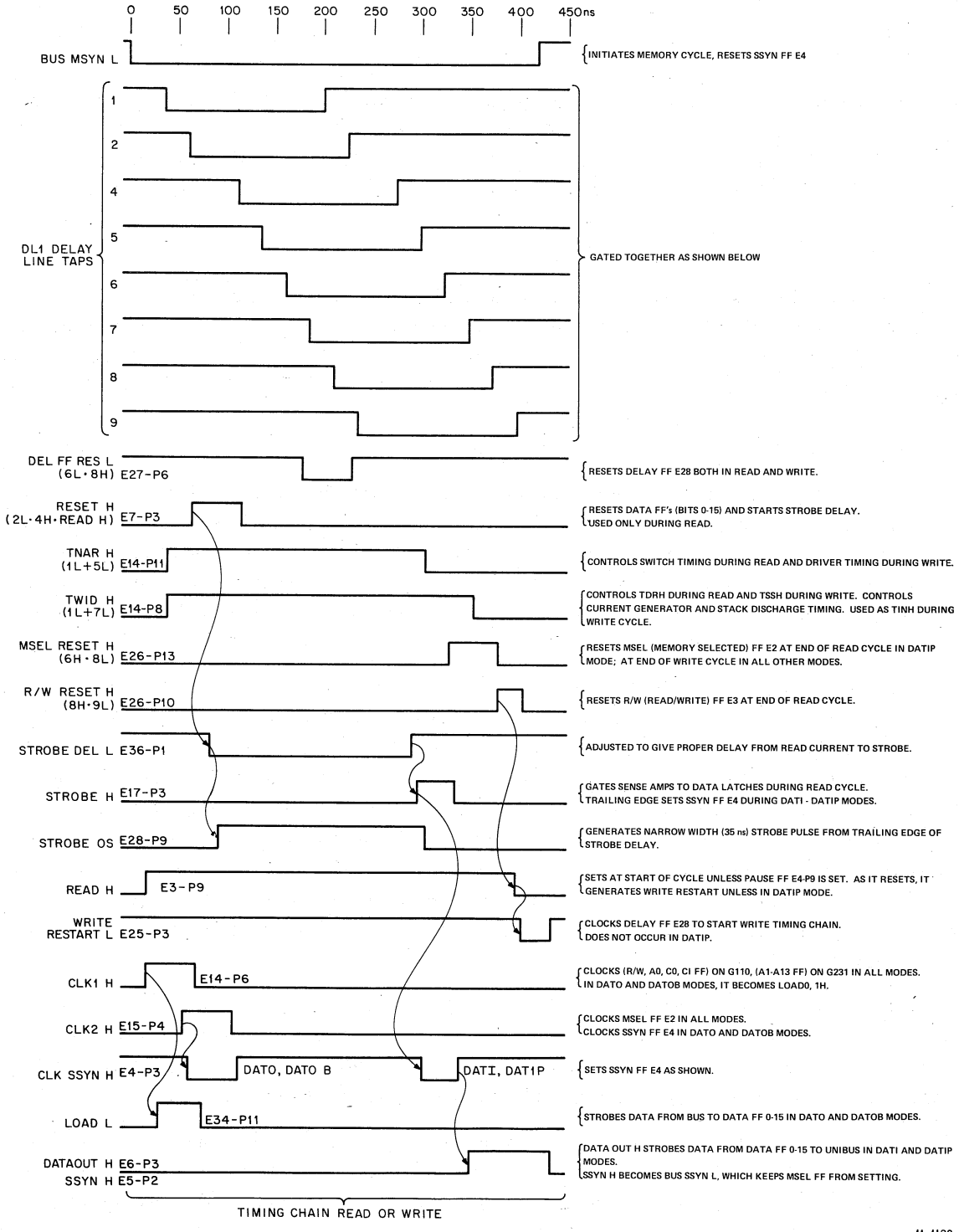


Figure 3-24 Basic Timing and Control Signal Functions

DL1 taps 2, 4, 5, 6, 7, 8, and 9 are used to generate control signals. Using Figure 3-24 as a guide, each control signal discussed is related to the logic drawing (G110-0-1, sheet 2).

DELAY FF RESET

Tap 6L is inverted by E15 and sent to pins 3 and 5 of 3-input NAND gate E27; the third input (pin 4) is tap 8H. The output (pin 6) of E27 is the signal that clears DEL flip-flop E28; however, it is ORed with INIT L in gate E38 (pins 9 and 10) and inverted by E38 pin 11 so that either (6L · 8H) or BUS INIT L can produce DELAY FF RESET which clears E28 via its clear input (pin 1). This signal is generated in both read and write operations.

RESET H

Tap 2L, tap 4H, and READ H are gated to generate RESET H which triggers the strobe delay circuit and generates RESET 0 L and RESET 1 L during the read operation only. Tap 4H and READ H (high during read operation) are ANDed at pins 10 and 9 of E17. The low output of E17 is ANDed with tap 2L in gate E7. The high output (pin 3) is RESET H.

TWID H and TNAR H

The 0-output of DEL flip-flop E28 is ORed with tap 5L and tap 7L in separate gates (E14) to produce TWID H and TNAR H. Tap 5L is sent to pin 13 of E14; the other input to this gate (pin 12) is from the 0-output of DEL flip-flop E28. Tap 7L is sent to pin 10 of another E14 gate; pin 9 of this gate also is connected to the 0-output of DEL flip-flop E28. These gates are 2-input NAND gates (type 7437); however, they are shown as logically equivalent negated-input OR gates because it is desired to have them asserted high (logical 1) when TWID H or TNAR H is asserted.

At the start of a read or write cycle, just before E28 is set, TNAR and TWID are low because both inputs to each gate are high. E28 is set and pins 23 and 9 of E14 go low; TNAR and TWID are both high, which starts the positive TNAR and TWID pulses simultaneously. When taps 5 and 7 go low (E28 is still set), TNAR and TWID remain high. At the end of the read or write cycle, E28 is cleared (taps 5 and 7 are still low) and TNAR and TWID still remain high. When tap 5 is high again, TNAR goes low because both inputs (pins 12 and 13) of E14 are high. This terminates the positive TNAR pulse. Approximately 50-ns later, tap 7 is high again and TWID goes low which terminates the positive TWID pulse. To summarize TNAR H and TWID H are started together by the setting of DEL flip-flop E28 before taps 5 and 7 are low; they are not affected when taps 5 and 7 go low. TNAR H and TWID H are terminated when taps 5 and 7 return high. The intervening clearing of E28 does not affect TNAR H or TWID H.

TNAR H and TWID H provide various control functions related to the operation of the switches, drivers, current generators, inhibit drivers, and stack discharge circuit. At this point, the discussion digresses to follow TNAR H and TWID H through some additional logic to understand their functions. The logic is spread throughout several engineering drawings. To simplify the discussion, all the logic is shown in Figure 3-25.

TWID H is ANDed with the 0-output (pin 8) of R/W flip-flop E3 at pins 9 and 10 of gate E25. With TWID H high, E25 is asserted only when E3 pin 8 is high; this occurs only during a write operation. The output (pin 8) of E25 is inverted by E14 to produce TINH 0 H and TINH 1 H. The output of E14 is physically divided into two paths: TINH 0 H activates the inhibit drivers for bits D⟨07:00⟩ and TINH 1 H activates the inhibit drivers for bits D⟨15:08⟩. These signals do not leave the Control Module because the inhibit drivers are on this module also.

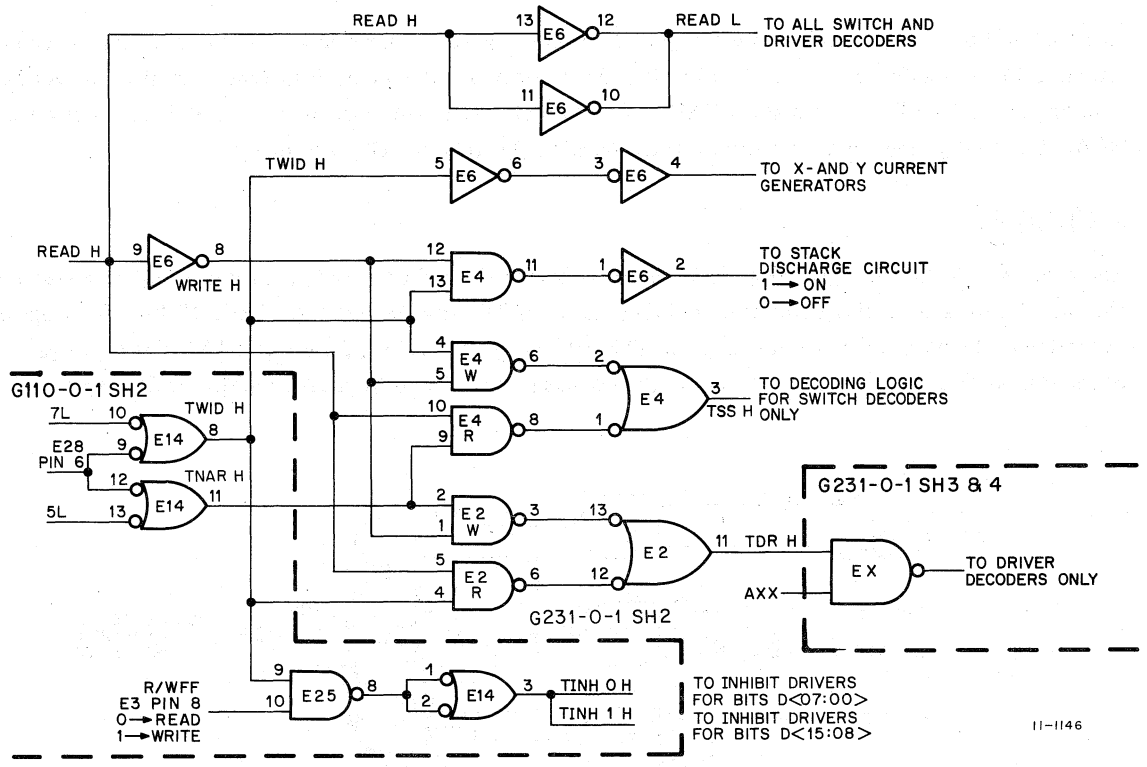


Figure 3-25 TWID H and TNAR H Control Logic

TWID H and TNAR H leave the Control Module (G110) and are sent to the Driver Module (G231). TWID H is sent to pin 4 of E2R and TNAR H is sent to pin 2 of E2W. Gates E2 and E4 are marked W and R in Figure 3-25 to show their association with write or read operations. READ H is sent from the 1-output (pin 9) of R/W flip-flop E3 on the Control Module to pin 9 of inverter E6 on the Driver Module. READ H is high during a read operation and low during a write operation. Assume that a read operation is selected. READ H is high at pin 9 of E6 and is sent to pin 5 of E2R to be ANDed with TWID H. This gate is asserted and its low output is sent to pin 12 of negative-input NOR gate E2 which inverts it to produce TDR H. This signal is a decoding input for the memory read/write drivers only. Gate E2W is not asserted because WRITE H, which is the inversion of READ H, is low. Therefore, TWID H controls decoding signal TDR H during a read operation. During a write operation READ H is low and WRITE H is high. TDR H is asserted via the output of gate E2W using the ANDing of WRITE H and TNAR H. Decoding signal TDR H is controlled by TNAR H during a write operation.

A similar logic network is used to control signal TSS H which enables six decoding signals that are used to control memory read/write switches only. Gates E4W, E4R, and E4 are used; TSS H is generated at the output (pin 3) of E4. During a read operation, TNAR H controls enabling signal TSS H; TWID H controls TSS H during a write operation. TWID H controls the operation of the X- and Y-current generators. During read and write operations, when TWID H is high, it is double inverted by two E6 inverters to turn on both current generators.

TWID H also controls the operation of the stack discharge circuit. It is ANDed with WRITE H at pins 13 and 12 of NAND gate E4. The output (pin 11) of E4 is inverted by E6 to control the stack discharge circuit. This circuit is considered to be turned on when the output (pin 2) of E6 is high. This occurs during a write operation; TWID H and WRITE H both high.

Although not part of the timing circuit, Figure 3-25 shows READ H inverted by two E6 inverters to become READ L which is a decoding input to all type 8251 decoders for the memory switches and drivers. During a read operation, READ H is high and READ L is low which selects only read switches and drivers; conversely, READ L is high during a write operation which selects only write switches and drivers.

MSEL RESET

The memory select (MSEL) flip-flop E2 is cleared (reset) at the end of a read operation in DATIP mode and at the end of a write operation in all other modes (DATI, DATO, and DATOB) by MSEL RESET. This signal is generated at the output (pin 8) of gate E16. This gate is a type 74H53 2-2-2-3 input AND-OR-invert gate. Three of its four AND inputs are used to facilitate the various methods used to generate MSEL RESET (Figure 3-26).

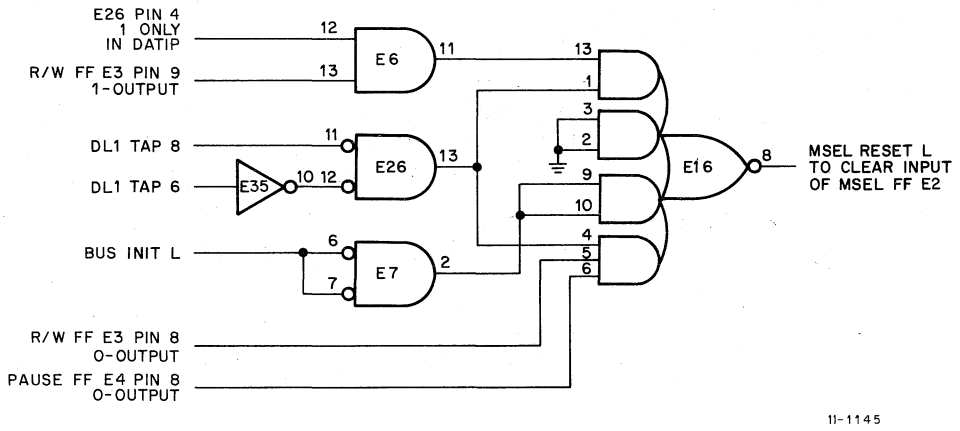


Figure 3-26 Generation of MSEL RESET L

When the system is turned on, the processor asserts BUS INIT L on the Unibus. The output of bus receiver E7 is a high which is sent to pins 9 and 10 of E16 to generate MSEL RESET L at its output (pin 8). MSEL RESET L is passed through a 100-ns delay line (DL3) to the clear input (pin 1) of MSEL flip-flop E2 which directly clears (resets) it. All memory operations start with E2 cleared; however, it is set shortly (approximately 75 ns) after the processor asserts BUS MSYN L. It remains set until it is cleared by one of the following operations.

In the DATIP mode, pin 12 of AND gate E6 is high; in all other modes it is low, which disqualifies E6. A read operation is performed in DATIP so R/W flip-flop E3 is set. The 1-output of E3 is sent to pin 13 of E6. At this time pin 13 is high and a high is asserted at the output (pin 11) of E6. This signal is sent to pin 13 of E16. This AND input is qualified when pin 1 is also high. This occurs when DL1 tap 6 is high and DL1 tap 8 is low. Tap 6H is inverted by E35 and sent to pin 12 of E26. Tap 8L is sent directly to the other input (pin 11) and the gate is asserted, which sends a high to pin 1 of E16. This asserts MSEL RESET L at the output (pin 8) of E16. This low signal clears MSEL flip-flop E2 at the end of the read operation (timed by 6H and 8L).

In all other modes (DATI, DATO, and DATOB), MSEL RESET L is asserted at the end of the write operation. Each of the three modes starts with a read operation (except DATO or DATOB following a DATIP). The R/W flip-flop is set so its 0-output (pin 8) is low which disqualifies the 3-input (pins 4, 5, and 6) AND gate in E16. Taps 6H and 8L cannot qualify this AND input nor can they qualify the other AND input (pins 1 and 13) because the memory is not in the DATIP mode. Therefore, the read operation is completed and MSEL RESET L

is not generated. The write operation is now started and the R/W flip-flop is cleared. This puts a high on input 5 of E16; input 6 is high because the PAUSE flip-flop is reset (pin 8 is a 1). Now, when tap 6 is high and tap 8 is low, input 4 of E16 is high. This generates MSEL RESET L to clear MSEL flip-flop E2 at the end of the write operation. This circuit performs the function of a memory bus flip-flop.

R/W RESET

The timing for the generation of the signal to clear (reset) R/W flip-flop E3 is obtained from taps 8 and 9 of DL1 (drawing G110-0-1, sheet 2). Tap 9 is sent directly to pin 8 of E26. Tap 8 is inverted by E35 and sent to pin 9 of E26. When tap 9 is low and tap 8 is high, E26 is asserted (output pin 10 is high). This signal is sometimes called R/W RESET H. It is ANDed with READ H at pins 2 and 1 of NAND gate E18 to generate R/W RESET L. When this signal is a low, it directly resets R/W flip-flop E3 via its clear input (pin 13). READ H is high when the R/W flip-flop is set because it comes from the 1-output (pin 9). The remainder of the control signals shown in Figure 3-24 are discussed in the circuit descriptions contained in Paragraph 3.3.8.2, Slave Synchronization Circuit; Paragraph 3.3.8.3, Pause/Write Restart Circuit; and Paragraph 3.3.8.4, Strobe Generating Circuit.

3.3.8.2 Slave Synchronization (SSYN) Circuit – Slave synchronization (SSYN) is the slave device's response to the master: usually a response to master synchronization (MSYN). The master places address information, mode control information, and data (if a DATO or DATOB is selected) on the Unibus. It then asserts MSYN only if SSYN from the slave is cleared, which indicates that the slave can participate in a bus transaction. The slave asserts SSYN when it has data to send (DATI or DATIP) or when it has received data (DATO or DATOB). The master receives SSYN in both cases and clears MSYN. When the slave receives the cleared MSYN it clears SSYN which frees the bus. This brief statement of the SSYN/MSYN interaction is necessary to understand the operation of the memory SSYN circuit. Details of the SSYN/MSYN interaction during all bus transactions can be found in the *PDP-11 Peripherals and Interfacing Handbook.*

The SSYN circuit is shown in drawing G110-0-1, sheet 2; however, for clarity, only the SSYN circuit is shown in Figure 3-27 along with appropriate timing diagrams.

During a DATI or DATIP transaction, BUS SSYN L is asserted by the memory when the data is placed on the Unibus by the memory data register. During a DATO or DATOB transaction, BUS SSYN L is asserted by the memory when it takes in the data from the Unibus.

At the start of each transaction, the master first places the memory address (device and word) and mode control information on the Unibus. (Data is included if the transaction is DATO or DATOB.) For a DATI or DATIP, BUS C01L is high at pin 10 of bus receiver E29. The output (pin 14) of E29 is low and it is sent to the D-input (pin 6) of C01 latch E30 and to pin 5 of the E5 WRITE gate. BUS MSYN L has not been asserted yet so the output (pin 13) of bus receiver E23 is low. This signal is sent to pin 2 of NOR gate E26; the other input (pin 3) of this gate is always low because MSYNA L is normally not connected. The output (pin 1) of E26 is inverted by E15 to produce SSYN RESET L which sets the SSYN flip-flop E4 via its preset input (pin 4). The 0-output (pin 6) is low and is sent to both inputs of bus driver E5. The output of this gate is the slave synchronization signal (BUS SSYN L) and, at this point, it is not asserted. As long as BUS MSYN L is not asserted, the SSYN flip-flop is preset. Now, the master asserts BUS MSYN L which disables the preset signal to the SSYN flip-flop (SSYN RESET L is high). Clock signal CLK 1 H is generated and clocks C01 latch E30. The latch is reset and its 0-output (pin 11) is a high which is sent to pin 10 of the E5 READ gate. The wired-AND output is CLK SSYN which is high. It remains high as long as both E5 NAND gate outputs are high; this occurs when at least one input of each gate is low. The output of E5 WRITE remains high because input pin 5 is held low by the output of C01 receiver E29. The output of this gate is not changed when the CLK 2 H pulse appears at pin 4. The output of E5 READ remains high until STROBE H goes high, at which point its output goes low.

When STROBE H goes low again, the wired-AND output is high again. This positive transition clocks the SSYN flip-flop which now resets because its D-input is tied to ground (low). The 0-output (pin 6) of the SSYN flip-flop is high which asserts BUS SSYN L at the output (pin 3) of bus driver 5. The master receives the asserted BUS SSYN L signal and clears BUS MSYN L. The memory receives the cleared BUS MSYN L at bus receiver E23 and generates SSYN RESET L via gates E26 and E15 to set the SSYN flip-flop. The memory is now ready for the next transaction.

For a DATO or DATOB, the sequence is the same except that BUS C01 L is low at pin 10 of bus receiver E29. This conditions the wired-AND so that the output of E5 READ remains a 1. In this case, the CLK 2 H pulse generates the CLK SSYN pulse that clocks the SSYN flip-flop via E5 WRITE.

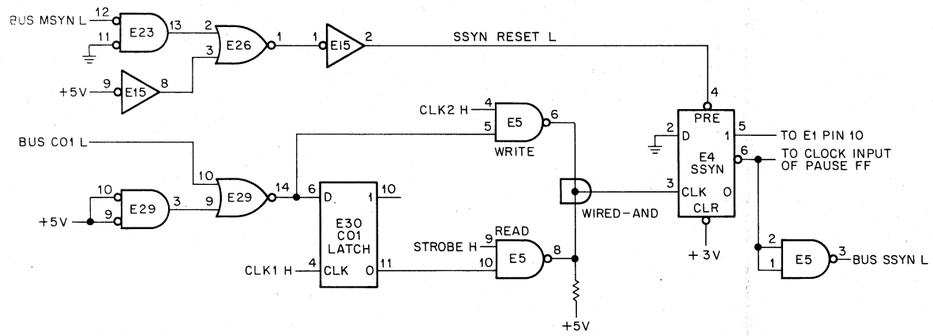
3.3.8.3 **Pause/Write Restart Circuit** – The PAUSE flip-flop (E4) is used to inhibit the restore (write) operation during a DATIP. This transaction is used to advantage when it is not necessary to restore the data after reading because the location is to have new data written into it. Eliminating the restore operation decreases the memory cycle time by approximately 50 percent. A DATIP must always be followed by a DATO or DATOB. In this case, the DATO or DATOB is shortened by eliminating the normal clear (read) operation that is performed prior to the write operation. The location has been cleared previously by the DATIP so the DATO or DATOB performs only the write operation.

The pause/write restart circuit is shown in drawing G110-0-1, sheet 2; however, for clarity, only the pause/write restart circuit is shown in Figure 3-28.

At the start of all bus transactions, the PAUSE flip-flop is reset and it remains in this state during the whole transaction except for a DATIP during which it is set after the read operation. The PAUSE flip-flop is clocked by the 0-output (pin 6) of the SSYN flip-flop when it is reset. The state (set or reset) of the PAUSE flip-flop is determined by its D-input (pin 12): D is high to set and D is low to reset. The D-input state is controlled by the Unibus mode control bits C01 and C00; only the mode control representing a DATIP provides a high to the D-input of the PAUSE flip-flop. During a DATIP, C01 is high and C00 is low at bus receivers E29 pin 10 and E29 pin 7. These signals are inverted by the receivers and applied to the D-inputs of the C01 and C00 latches: C00 latch E30 pin 3 is high and C01 latch E30 pin 6 is low. When the latches are clocked by CLK 1 H, latch C01 is reset and C00 is set. This puts a low on each input of negative input AND gate E26 which generates a high output. This is the D-input to the PAUSE flip-flop. The PAUSE flip-flop is now conditioned to set when it is clocked.

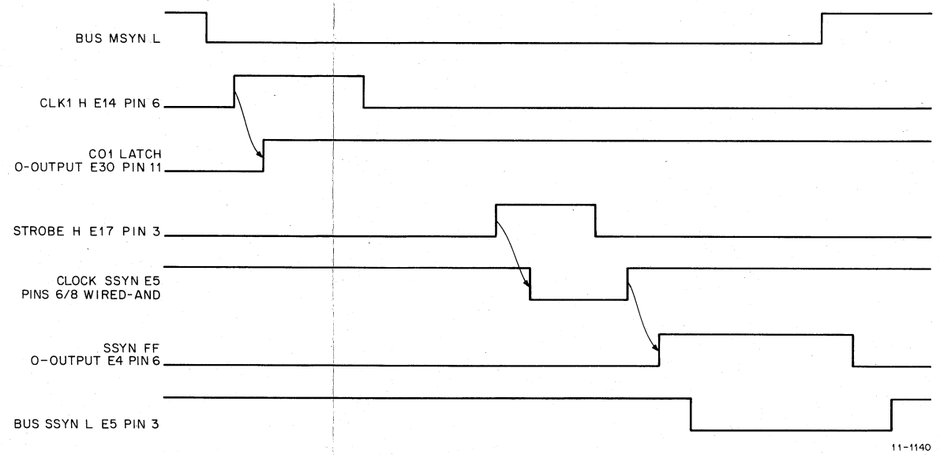
Going back to the start of the DATIP, the PAUSE flip-flop is reset. Its D-input is conditioned (D is high) but it has not been clocked so its 0-output (pin 8) is high. This output goes to the D-input of the read/write flip-flop (R/W E3). It is clocked early in the sequence by CLK 1 H so it is set, which permits a read operation. The 0-output (pin 8) of the R/W flip-flop is low and is sent to pin 4 of E17. The other input (pin 5) of E17 comes from the 0-output (pin 8) of the PAUSE flip-flop and it is a high at this time. The output of E17 is a high and is inverted by E15 which puts a low on the clear input of the write restart flip-flop (WR RS E2). The output of E15 also goes to input 2 of E25. The WR RS flip-flop is cleared (reset) and its 0-output (pin 8) is a high which is sent to the other input (pin 1) of E25. The output of E25 is the WRITE RESTART L signal which is produced to trigger the timing circuit and produce a write operation. It is high now, which is proper, because a read operation is being performed.

At the end of the read operation, the SSYN flip-flop is clocked, which resets it. The positive transition at its 0-output (pin 6) clocks the PAUSE flip-flop which sets it and puts a low on pin 5 of E17. The timing circuit clears (resets) the R/W flip-flop which puts a high on pin 4 of E17. The output of E17 remains high which inhibits the WRITE RESTART L signal and prevents the initiation of a write operation.



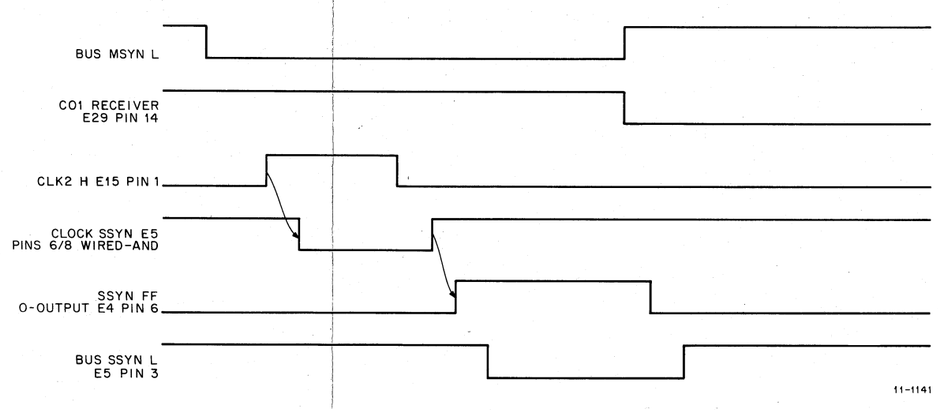
11-1139

Slave Synchronization (SSYN) Circuit



11-1140

Timing Diagram for SSYN Circuit
During DATI and DATIP



11-1141

Timing Diagram for SSYN Circuit
During DATO and DATOB

Figure 3-27 Slave Synchronization (SSYN) Circuit and Timing Diagrams

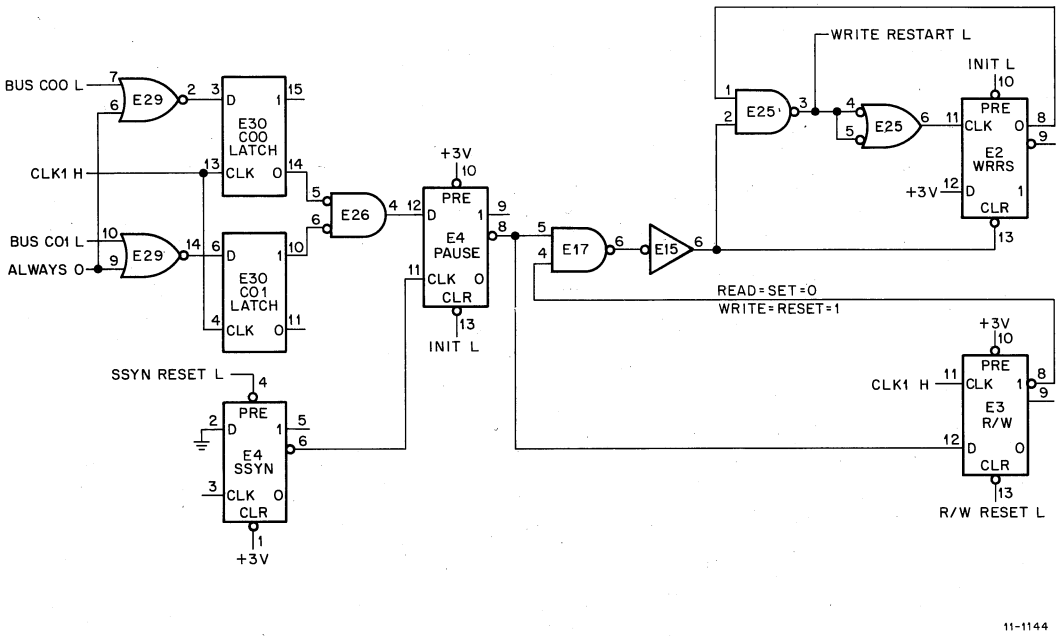


Figure 3-28 Pause/Write Restart Circuit

For any other transaction (DATI, DATO, or DATOB) the PAUSE flip-flop is not set when it is clocked because its D-input is low. It remains reset which keeps a high on pin 5 of E17. When the R/W flip-flop is cleared it puts a high on pin 4 of E17. Now, the output of E17 is a low which is inverted by E15 and sent to pin 2 of E25. The WR RS flip-flop is reset so pin 1 of E25 is also high. The output (pin 3) of E25 goes low which generates WRITE RESTART L. This starts the formation of a low WRITE RESTART pulse. This output is inverted by E25 pin 6 and clocks the WR RS flip-flop which sets it because its D-input is connected to +3V. Pin 8 of the WR RS now goes low and is fed to pin 1 of E25. This makes the output of E25 high again which terminates the low WRITE RESTART L pulse. This pulse triggers the timing circuit and initiates a write operation.

For a DATO or DATOB following a DATIP, the PAUSE flip-flop is reset by the SSYN flip-flop because the DATO or DATOB transaction started with the PAUSE flip-flop set previously by the DATIP.

3.3.8.4 Strobe Generating Circuit – The strobe generating circuit produces a narrow positive pulse (STROBE H) during the read operation to enable the STROBE 0 H and STROBE 1 H signals for the sense amplifiers.

The strobe generating circuit is shown in drawing G110-0-1, sheet 2; however, for clarity, only the strobe generating circuit is shown in Figure 3-29 along with an appropriate timing diagram.

During the read operation, the timing circuit generates RESET H which is a positive pulse. It is sent to pin 5 of the strobe delay one-shot (ST DEL E36). This type 74121 one-shot provides complementary outputs but only the $\overline{Q}$ (negative pulse) output (pin 1) is used. Pins 3 and 4 of the ST DEL one-shot are connected to ground so that only a positive-going edge at pin 5 triggers it.

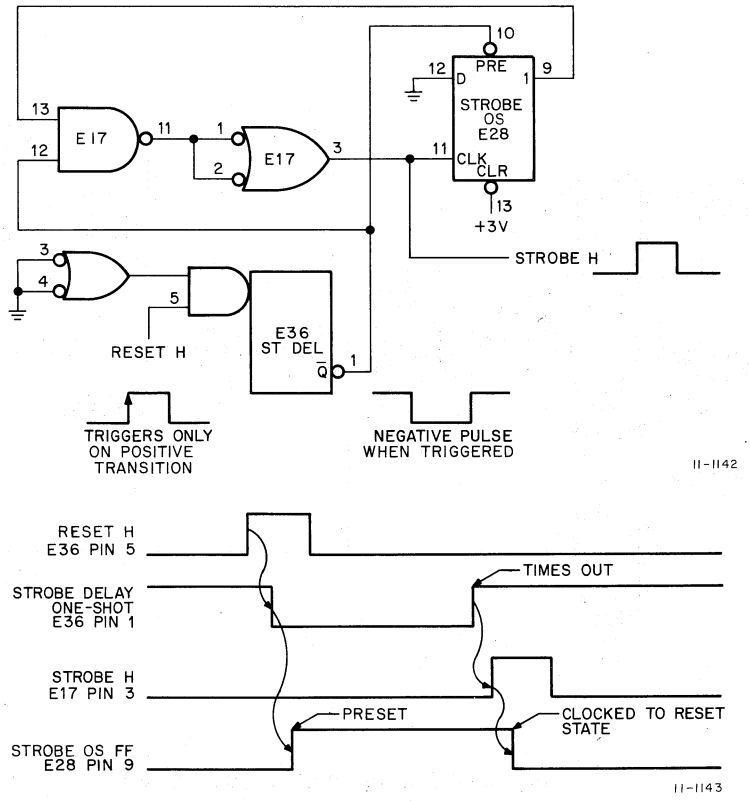


Figure 3-29 Strobe Generating Circuit and Timing Diagram

Prior to receiving the triggering signal (RESET H), the strobe generating circuit is in the quiescent state. The STROBE 0S flip-flop E28 is in the reset state. (When the memory is powered up, E28 is driven to the reset state by E36 if it did not come up reset randomly.) The 1-output (pin 9) of E28 is low and is sent to pin 13 of E17. The ST DEL one-shot is inhibited, so its $\overline{Q}$ output (pin 1) is a high which is sent to pin 12 of E17. The output (pin 11) of E17 is high and is inverted by the next E17 gate (pin 3). This is the STROBE H signal and it is low at this time.

The timing circuit generates a positive RESET H pulse that is sent to pin 5 of E36. The positive edge of RESET H triggers E36 and its $\overline{Q}$ output (pin 1) goes to low. This is the start of a single negative pulse whose duration is determined by an external RC circuit connected to pins 10 and 11 of E36. The output of E36 directly sets STROBE 0S flip-flop E28 via its preset input (pin 10). The 1-output (pin 9) of E28 goes high and is sent to pin 13 of E17. The other input to this gate (pin 12) is now low. E17 pin 11 is high and is inverted so E17 pin 3 is still low (no strobe pulse yet). When E36 times out, its output (pin 1) goes high again. Pins 12 and 13 of E17 are now both high and the output (pin 11) of E17 is low. This signal is inverted and E17 pin 3 is high. This is the beginning of the STROBE H pulse. The positive transition at E17 pin 3 also clocks flip-flop E28. It is reset because its D-input is connected to ground (low). Pin 9 of E28 is now low. It is fed back to pin 13 of E17 which makes E17 pin 3 low again. This terminates the positive STROBE H pulse. The circuit is back to its quiescent state where it remains until another RESET H pulse triggers ST DEL one-shot E36.

3.3.8.5 Data In (DATI) Operation – The discussion of the DATI operation, as well as the DATIP, DATO, and DATOB operation, is descriptive. Signals are not traced through circuit components; rather, various events are integrated to describe a complete memory operating cycle. All the circuits involved have been discussed in detail in the preceding paragraphs of this chapter. Refer to engineering logic drawings G110-0-1, sheets 2, 3, and 4; G231-0-1, sheets 2, 3, and 4; MM11-L3 (timing diagram); and Figure 3-30, which is a flow chart for memory operation.

In a DATI operation, the master requests that a selected memory location be read and the information transferred to the master via the Unibus. The readout is destructive because the read operation forces all cores in the selected location to 0. However, during readout, the information is temporarily stored in the memory data register (MDR) and is automatically restored to the selected location by a write operation that immediately follows the read operation.

At the start of the DATI, the MSEL, DEL, R/W, and PAUSE flip-flops are reset, and SSYN flip-flop is set. The address lines and mode control lines (C01 and C00) are decoded. The master asserts BUS MSYN L and the cycle begins. CLK 1 H is generated, the DEL flip-flop is set, and the R/W flip-flop is set. Setting the DEL flip-flop initiates the timing chain via delay line DL1. The timing chain generates TWID H and TNAR H. CLK 2 H is generated at the same time and it presets the MSEL flip-flop, which prevents the start of another cycle until it is reset. Signal READ H from the R/W flip-flop and signals TNAR H and TWID H go to the driver module to select the appropriate read drivers and switches, turn on the X- and Y-current generators, and control the stack discharge circuit. As a result of these signals, the X- and Y-half currents are directed to the selected memory location and all 16 cores (one per bit plane) are set to 0. Just prior to this event, the timing chain generates RESET 0 L and RESET 1 L which clear the memory data register. The timing chain generates STROBE H which asserts STROBE 0 H and STROBE 1 H which are sent to the sense amplifiers. The strobe pulses are timed to arrive at the same time as the pulses induced in the sense/inhibit line. If a selected core was a 1, a pulse is induced in the sense/inhibit line that exceeds the sense amplifier threshold and it produces an amplified positive pulse. This output is inverted, presets its associated MDR flip-flop, and a 1 is stored in the flip-flop. STROBE H also clocks the SSYN flip-flop which resets. The SSYN flip-flop output asserts DATA OUT H and BUS SSYN L. Signal DATA OUT H gates the output of the memory data register to the Unibus. BUS SSYN L is a Unibus signal that informs the master that the memory has read the selected location and placed the data on the Unibus. The master takes the data and clears BUS MSYN L which generates SSYN RESET L to set the SSYN flip-flop. BUS SSYN L is cleared to indicate that the Unibus is free; however, another bus transaction cannot be initiated even if the master asserts BUS MSYN L because of the lockout feature of the MSEL flip-flop, which is still set. Prior to the assertion of BUS SSYN L, the timing chain generates DELAY FF RESET L which resets the DEL flip-flop and allows the TNAR H and TWID H pulses to terminate as a function of taps 5 and 7 of the delay line. The timing chain also generates R/W RESET L which resets the R/W flip-flop.

The memory now enters the write (or restore) cycle. With the R/W flip-flop and PAUSE flip-flop both reset, the pause/write restart circuit generates WRITE RESTART L which initiates another timing cycle by setting the DEL flip-flop.

The timing chain generates TWID H and TNAR H. These signals plus a low READ H signal from the R/W flip-flop go to the driver module to select the appropriate write drivers and switches, turn on the X- and Y-current generators, and control the stack discharge circuit. In addition, TWID H and an output from the R/W flip-flop are ANDed to generate TINH 0 H and TINH 1 H. These signals control the operation of the inhibit drivers. TINH 0 H and TINH 1 H are ANDed with the outputs of the MDR flip-flops. If a 1 is stored in the MDR flip-flop, the associated inhibit driver is not turned on and a 1 is written into this bit of the selected memory location. If a 0 is stored in the MDR flip-flop, the associated inhibit driver is turned on and produces a current that opposes the Y-line current and prevents a 1 from being written into this bit. The timing chain generates

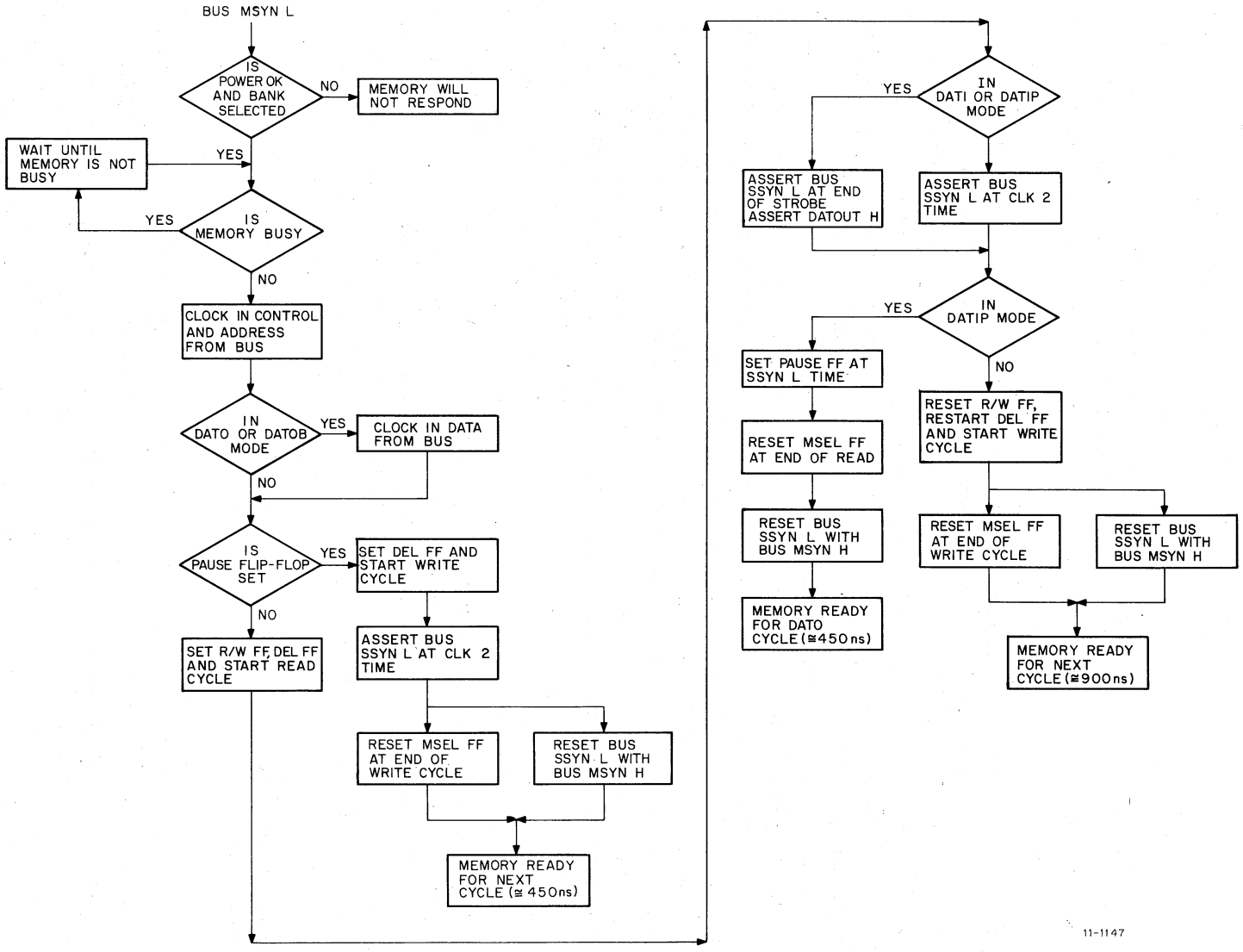


Figure 3-30 Flow Chart for Memory Operation

DELAY FF RESET L which resets the DEL flip-flop and allows TNAR H, TWID H, and the inhibit pulses (TINH 0 H and TINH 1 H) to terminate. The timing chain also generates MSEL RESET L which resets the MSEL flip-flop.

3.3.8.6 **Data In Pause (DATIP) Operation** – In a DATIP operation, the master requests that a selected memory location be read and the information transferred to the master via the Unibus. However, unlike the DATI, this information is not to be restored after reading; this location is to have new information written into it. The DATIP performs only a read operation, the write operation is inhibited. A DATIP must always be followed by a write transaction (either DATO or DATOB).

The read operation of a DATIP is identical to that of a DATI (Paragraph 3.3.8.5) until the time the SSYN flip-flop is reset (clocked by STROBE H). At this time, the SSYN flip-flop output clocks the PAUSE flip-flop which sets it because its D-input is a 1 (only during DATIP due to the state of mode control bits C01 and C00). The timing chain generates R/W RESET L which resets the R/W flip-flop. The outputs of the PAUSE flip-flop and R/W flip-flop prevent the pause/write restart circuit from generating WRITE RESTART L. With this signal inhibited, the write operation is not produced. The timing chain generates DELAY FF RESET L which resets the DEL flip-flop and terminates TNAR H and TWID H. The timing chain also generates MSEL RESET L which resets the MSEL flip-flop. The memory is now ready to accept another request from the master. The next cycle is required to be a DATO or DATOB. Normally, a DATO or DATOB starts with a read operation to set all selected cores to 0 (clear) before writing new information into them. A DATO or DATOB following a DATIP has this initial clear operation eliminated because the cores have been cleared by the previous DATIP operation.

The DATO or DATOB following a DATIP starts when the master asserts BUS MSYN L. Pulse CLK 1 is generated but it does not set the R/W flip-flop because the PAUSE flip-flop is set. The master places the information to be written on the Unibus where it is picked off by bus receivers and sent to the D-input of the memory address register flip-flops. Decoding the mode control bits (C01 and C00) for a DATO or DATOB generates LOAD 0 H and LOAD 1 H which clock the MDR flip-flops. The outputs of the MDR flip-flops are gated with TINH 0 H and TINH 1 H to control the associated inhibit drivers to write 1s or 0s into the selected memory location. As in the write operation of a DATI, the timing chain generates TWID H and TNAR H which select the appropriate write drivers and switches, turn on the X- and Y-current generators, and control the stack discharge circuit. They also generate inhibit driver control signals TINH 0 H and TINH 1 H. Signal CLK 2 H clocks the SSYN flip-flop (resets it) which asserts BUS SSYN L to tell the master that the data has been taken from the Unibus. When the master clears BUS MSYN, the SSYN flip-flop is reset, which in turn resets the PAUSE flip-flop. At the end of the write operation, the timing chain generates DELAY FF RESET L and MSEL RESET L to restore the control signals to their original states.

3.3.8.7 **Data Out (DATO) Operation** – In a DATO operation, the master sends a word of 16 bits to be written into the selected memory location. The transaction starts with a read (clear) operation to set the selected cores to 0 before writing new data into them. The standard DATO consists of a read operation followed by a write operation. (As described in Paragraph 3.3.8.6, a DATO following a DATIP does not perform the read operation.)

The read operation of a DATO is similar to a read operation of a DATI except that no RESET 0 L, RESET 1 L, STROBE 0 H, and STROBE 1 H pulses are generated. The memory data register is not cleared and the sense amplifiers are not strobed. This read operation is required only to clear the memory location by setting all the selected cores to 0; it is not necessary to readout and store the information in the MDR.

The information on the Unibus data lines is sent to the inputs of the MDR flip-flops. Decoding the mode control bits (C01 and C00) generates LOAD 0 H and LOAD 1 H which clock the MDR flip-flops. The MDR outputs (16 bits) are gated with TINH 0 H and TINH 1 H to control the associated inhibit drivers. The timing chain

generates the other control signals that provide the selection of the appropriate write drivers and switches and a write operation is initiated. This write operation is the same as that described in Paragraph 3.3.8.6 for a DATO following a DATIP.

3.3.8.8 **Data Out Byte (DATOB) Operation** – In a DATOB operation, the master sends a byte (8 bits) to be written into the selected memory location. A high byte (bits D⟨15:08⟩) or a low byte (bits D⟨07:00⟩) can be selected. Byte selection is made by the state of address bit A00.

A DATOB is the same as a DATO except that the selected and non-selected bits are handled differently.

Assume that the low byte (bits D⟨07:00⟩) is selected (A00 = 0). Neither RESET 0 L or STROBE 0 H are generated for the selected byte because new data is to be written into bits D⟨07:00⟩ (low byte). LOAD 0 H is generated so that the data on Unibus bits D⟨07:00⟩ can be written into the selected byte location.

The non-selected byte (bits D⟨15:08⟩) is to be restored so RESET 1 L and STROBE 1 H are generated. These signals strobe the byte into the MDR for restoration during the write operation. Restoration is necessary because this byte does not receive new data. LOAD 1 H is not generated; therefore, any data on Unibus bits D⟨15:08⟩ has no effect on the non-selected byte.

When the DATOB is complete, the selected byte contains new data and the non-selected byte remains unchanged.

A DATOB operation following a DATIP is the same, except that the read portion is eliminated.

3.4 MAINTENANCE

This section discusses the preventive and corrective maintenance procedures that apply to the MM11-L memories. A major point in the maintenance philosophy of this manual is that the user understand the normal operation of the memory. Paragraph 3.3 provides this understanding. This knowledge, plus the maintenance information, aids the user in isolating and correcting malfunctions.

For maintenance purposes, the backplane unit is wired in such a way that an MM11-L can be plugged into, and run, in any one of three groups of module slots. These groups consist of slots 1, 2, and 3; slots 4, 5, and 6; or slots 7, 8, and 9. Therefore, an MM11-L, which consists of the G110, G231, and H214 modules, can be plugged into any of the three groups of slots described. The individual MM11-L modules work in any slot in either of the three slot groups. This allows a module to be plugged into slot 1 for easy troubleshooting or adjustment of the strobe. As an example, suppose it is necessary to adjust the strobe on the MM11-L plugged into slots 7, 8, and 9. Slot 7 contains the H214, slot 8 contains the G231, and slot 9 contains the G110. The G110 module contains the test point and strobe adjustment; therefore, it is necessary to move the G110 to slot 1 for easy access from the top of the ME11-L unit. To test the G110 in slot 1, the entire MM11-L must be moved from slots 7, 8, and 9 to slots 1, 2, and 3. Any MM11-L in slots 1, 2, and 3 is plugged into the slot group vacated.

With the modules in the proper slots (G110 in slot 1 and the H214 and G231 in opposite slots 2 or 3), the G110 is easily accessed from the top of the ME11-L unit and any adjustment can be made easily. When maintenance is complete, be sure each MM11-L has the G231 module between the G110 and H214 modules. This is the recommended operating configuration.

3.4.1 Preventive Maintenance

Preventive maintenance consists of specific tasks performed at intervals to detect conditions that could lead to subsequent performance deterioration or malfunction. The following tasks are considered preventive maintenance items:

a. Visual inspection of modules for broken wires, connectors, or other obvious defects
b. +5V and - 15V checks; both must be within ±3 percent
c. X- and Y-current generator check (Paragraph 3.4.1.2)

Two pieces of test equipment are recommended for checking and troubleshooting the memory. They are: Tektronix 453 Dual Trace Oscilloscope or equivalent, and Honeywell 33R Digital Voltmeter or equivalent with 0.5 percent accuracy.

3.4.1.1 Initial Procedures – Before attempting to check, adjust, or troubleshoot the memory, perform the following steps.

NOTE
All tests and adjustments must be performed in an ambient temperature range of 20°C to 30°C (68°F to 86°F).

1. Verify that all modules are properly and securely installed.

CAUTION
Make sure all power is off before installing or removing modules.

2. Visually check modules and backplane for broken wires, connectors, or other obvious defects.
3. Verify that power buses are not shorted together.
4. Turn on primary power and check that both the - 15V and +5V power are present and within tolerances (±3 percent).
5. Start the system. The memory should operate without errors. If not, check the output of the current generator (Paragraph 3.4.1.2). If the memory still does not operate properly, a malfunction has occurred. Proceed with corrective maintenance (Paragraph 3.4.2).

3.4.1.2 Checking Output of Current Generators – The amplitude of the current pulse from each current generator (X and Y) is factory set at 410 ±5 mA. It is not adjustable in the field.

The X- and Y-current generators are located on the Driver Module (G231). Each output has a current loop on its output line for attaching a test probe. Loop J5 is for the Y-generator and loop J6 is for the X-generator (drawing G231-0-1, sheet 2). The amplitude of each read current pulse should be 410 ±5 mA. At the time of measurement, - 15V and +5V power must be within the specified tolerance of ±3 percent.

3.4.2 Corrective Maintenance

This paragraph includes the strobe delay adjustment which is a specific corrective maintenance procedure. It also includes aids for performing corrective maintenance: a troubleshooting chart, and waveforms for the drive circuits and the sense/inhibit circuits.

3.4.2.1 Strobe Delay Check and Adjustment

CAUTION

Strobe delay is factory adjusted and should be adjusted only when one of the three modules is replaced. It is a critical adjustment and must be done carefully.

The strobe must be set while cycling the Worst Case Noise Test (MAINDEC-11-D1GA). The proper setting is mid-way between the two end points where the memory starts to error as strobe time is moved from earliest to latest. As the strobe time is varied, allow adequate time to cycle completely through the Worst Case Noise Test at each strobe position. Figure 3-31 shows the strobe pulse waveform and the READ pulse waveform and the points at which they are picked off for display. The potentiometer (R120) for adjusting the strobe is on the G110 module next to the large delay line (DL1) and is accessible without putting the module on an extender.

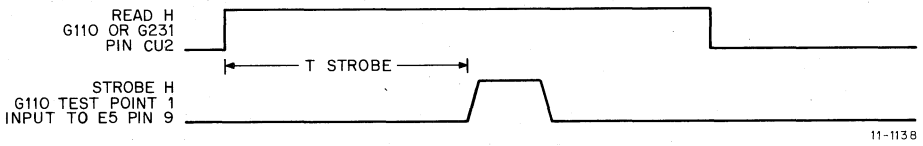


Figure 3-31 Strobe Pulse Waveform

3.4.2.2 Corrective Maintenance Aids – Figure 3-32 is a troubleshooting chart arranged as a 2-axis grid that identifies faults versus cause location. Figure 3-33 illustrates the sense/inhibit waveforms and Figure 3-34 illustrates the drive waveforms. Both figures include schematics to indicate the points in the circuit where the waveforms occur. In addition to nominal waveforms, dotted lines are used to indicate waveforms that appear if specific components are faulty.

3.4.3 Programming Tests

Certain DEC programs can be used to test various memory operations as an aid to troubleshooting. The purpose of each of these memory-related test programs, as well as the program abstract, is given in the following paragraphs. Each program contains instructions for its use.

3.4.3.1 Address Test Up (MAINDEC-11-D1A) – The purpose of the Address Test Up program is to demonstrate that the selected memory area is capable of basic read and write operations when address propagation is upward through memory.

This test program writes the address of each memory location (within the test limits) into itself and then increments through memory until the address corresponding to the high limit is reached. After this location has been written, the memory enters the read cycle. The read cycle starts with the high limit location and reads and compares each word location, decrementing down to the low limit location. The program halts on an error.

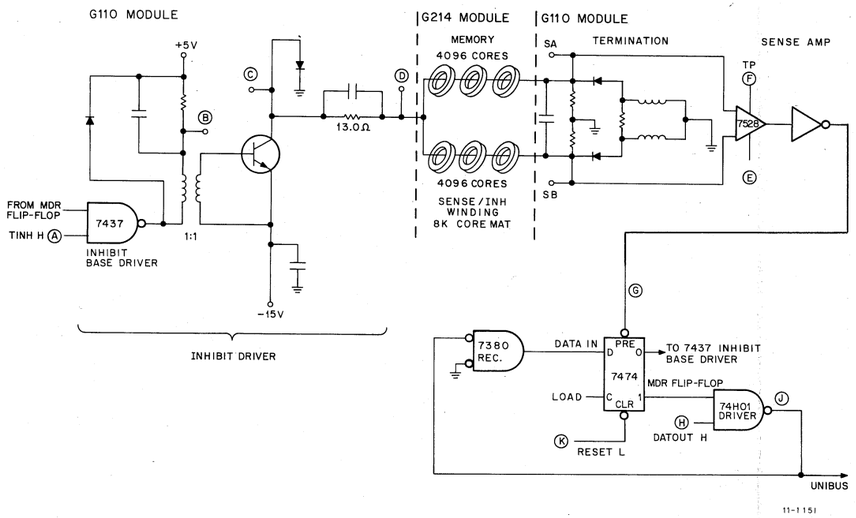
This program checks that all addresses are selectable and can also be used to isolate bad switches, wiring errors, or address selection errors. It will also find double selection errors when two bus addresses select the same core address.

Loc.	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	S	S	S	S	D	D	D	D	D	D	D	D	D	D	D				
Possible Circuit / Failure Symptom	−5.1V	Device Selection or Jumpers	DELAY Flip-Flop or DELAY Line	MSEL Flip-Flop	SSYN Flip-Flop	PAUSE Flip-Flop	READ Flip-Flop	Write Restart Flip-Flop	STROBE H	RESET L	LOAD H	TINH H	DATA OUT H	INIT L Circuit	BALUN Transformer	Bus Receiver-Driver	Sense Amplifier or Terminator	Data Latch	Inhibit Driver	20-mV Threshold		Stack S/I Line	Stack X-Y Line	Stack Diode	Stack Resistor-Thermistor		X-Y Volt Reference Circuit	Stack Discharge Circuit	X I Generator	Y I Generator	YDR	YSS	XDR	XSS	TDR-TSSH	DC LO L Circuit	4K–8K Jumper		Backplane	+5V	−15V
Memory Does Not Respond to MSYNL		X	X	X	X				X	X				X		X																			X		X	X	
Memory Hangs Bus					X																																			
DATO Fails											X			X		C00 C01		X																				X		
DATIP Fails						X								X		C00 C01																						X		
Many Bits Fail	X											X								+5 FA2																		X	X
Picks Bits	Lo								Lo									X	X							Lo	X	Hi	Hi										Lo
Drops Bits	Hi								Hi																	Hi	X	Lo	Lo										
Byte Failures									X	X	X	X				A0																							
4 Bits Fail															X	X				X																			
2 Bits Fail																	X	X																					
1 Bit Fails																		X	X			X																X		
Fails All Addresses	X	X											X											X		X	X	X	X					X	X			X	X	X
A1–A3 Common																							X	X					X											
A4–A6 Common																							X	X					X				X							
A7–A9 Common																							X	X						X	X									
A10–A13 Common																							X	X						X		X								
READ Waveforms Wrong																											X		X	X	X	X	X	X	X					
WRITE Waveforms Wrong												X															X		X	X	X	X	X	X	X					
No Inhibit												X							X			X																		X

Location { C = G110 Sense Control; S = Stack; D = G231 Driver }

X = Indicates Circuit Not Operable
Lo = Measured Parameter Too Low or Early
Hi = Measured Parameter Too High or Late

Figure 3-32 Troubleshooting Chart



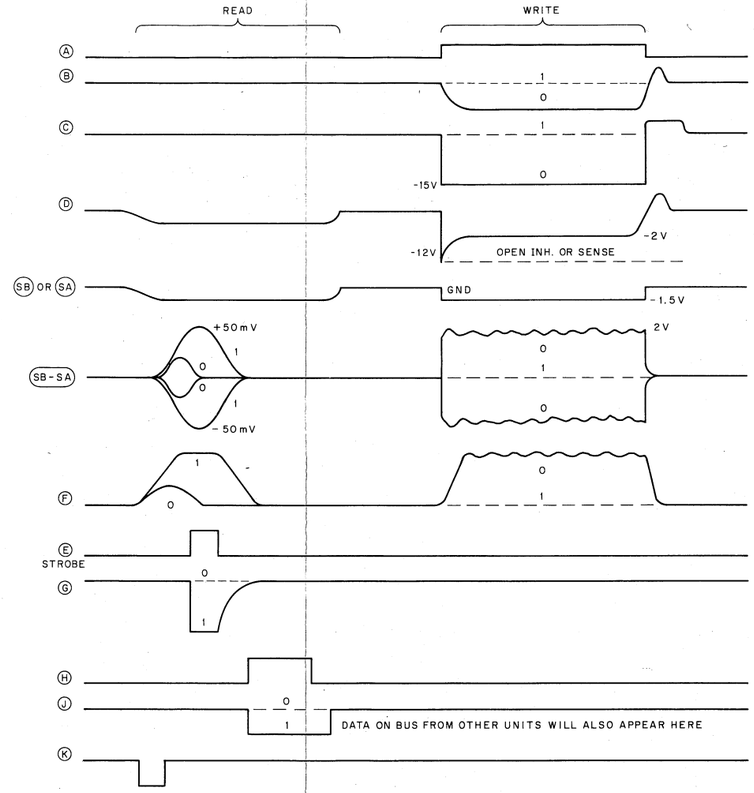
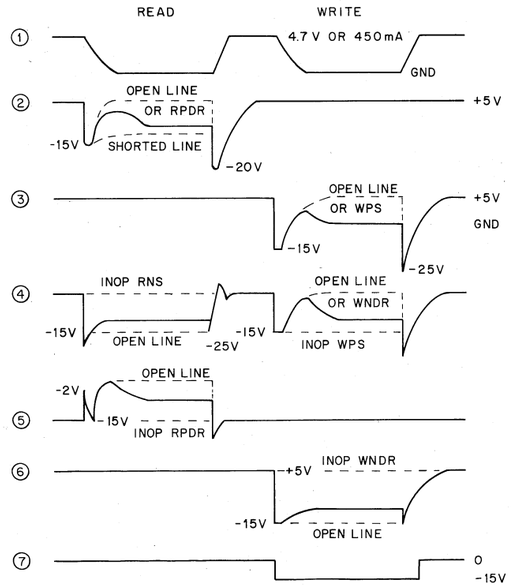
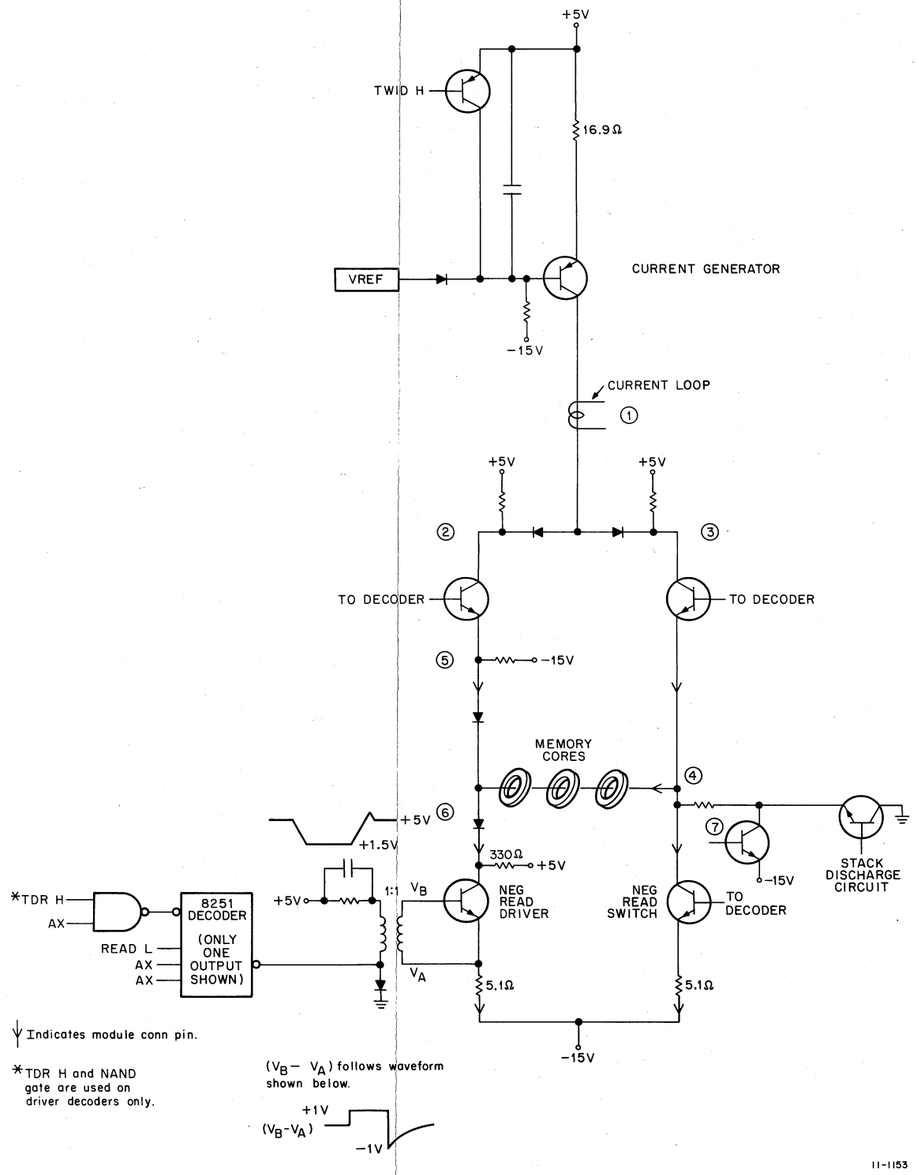


Figure 3-33 MM11-L Sense/Inhibit Waveforms



----Dotted line show possible failure waveforms.

11-1154



11-1153

Figure 3-34 Drive Waveforms

3.4.3.2 Address Test Down (MAINDEC-11-D1B) – The purpose of the Address Test Down program is to demonstrate that the selected memory area is capable of basic read and write operations when address propagation is downward through memory. It is a companion test to the Address Test Up program (Paragraph 3.4.3.1).

This test program writes the address of each location into itself, downward through memory. After writing down, the program reads and checks back up through the memory test area. The program halts on an error.

The Address Test Down program resides in the high portion of core memory. It does not check memory below address 100, as these locations are reserved for trap and vector locations. The program verifies that all modules can perform their basic functions, checks that all addresses are selectable, and can also be used to isolate faulty switches, wiring errors, or address selection errors.

3.4.3.3 No Dual Address Test (MAINDEC-11-D1C) – The purpose of the No Dual Address Test program is to check the unique selection of each memory address tested.

This test is divided into two parts. The first portion of the test fills the test field with 1s and writes 0s into the first test location. This is followed by a read check from this location. The program then checks each field location to ensure that there are no variations from the 1s configuration. Upon completion of this test, the test location pointer is incremented. The next location is then write-read exercised with 0s and the test field rechecked for any change in content. When the selected test field has been tested in this mode, the program sets a flag and the second portion of the test is begun. The program fills the test field with 0s and the field is then tested with a write-read exercised with 1s.

This program checks for faulty switches or wiring errors, checks the complete address selection scheme, and checks all 16 bits in the data field for 1s and 0s operation.

3.4.3.4 Basic Memory Patterns Test (MAINDEC-11-D1D) – The Basic Memory Patterns Test program has two main purposes:

a. Verify that the selected memory test field is capable of writing and reading fixed data patterns.
b. Verify that the memory plane is properly strung.

This test program writes a specific pattern throughout a given memory zone, then reads the pattern back and compares it with the original for correctness. If the pattern read fails to compare correctly with the original, the program initiates a call to the error subroutine. After completely checking the pattern, the program continues on to the next pattern test.

3.4.3.5 Worst Case Noise Test (MAINDEC-11-D1G) – The purpose of the Worst Case Noise Test program is to generate the maximum possible amount of plane noise during execution of memory reference instructions to check system operation under worst case conditions.

This test program is designed to produce the greatest amount of plane noise possible during memory read and write cycles. The noise parameters are effected by a number of factors: the noise generated is distributed across the core plane algebraically and adds to the normal dynamic noise present on the sense lines. This can cause misreading of data (within the plane) that is in the low (1) or high (0) category. The sense windings of most memories are such that worst case patterns can be caused by alternately writing -1 and 0 data configurations throughout memory. Under these conditions, worst case noise is generated by performing a read, write, complement, read, write, complement, operation at each location. The test is repeated after complementing all of the pattern data stored in the memory test zone, so that all cores are worst case tested as both 1s and 0s. The pattern, or its complement, is written into the memory test zone as determined by the exclusive-OR between address bits 3 and 9.

The Worst Case Noise Test program is divided into two parts. Part 1 is run first and, during this part of the program, a -1 configuration is written into all locations having an address with an exclusive-OR state between bits 3 and 9. All other locations are loaded with the 0 configuration. After the test zone has been loaded, the memory is rescanned. This time, each location is read, complemented, read, and complemented (RCRC). Any location detected as being disturbed by a previous RCRC operation is flagged as an error. Upon conclusion of the read scan loop, the program automatically switches to Part 2.

During Part 2 of the program, the data patterns stored in memory are complemented. In other words, 0 patterns are stored in locations having addresses with an exclusive-OR between bits 3 and 9. All other locations are loaded with the -1 configuration.

The exclusive-OR pattern distribution for Parts 1 and 2 is summarized for reference as follows:

Part 1

Exclusive-OR (3 and 9) = -1 pattern
No Exclusive-OR (3 and 9) = 0 pattern

Part 2

Exclusive-OR (3 and 9) = 0 pattern
No Exclusive-OR (3 and 9) = -1 pattern

After memory is loaded, it is scanned again with a read, complement, read, complement (RCRC) loop as described previously. Any location detected as being disturbed by a previous RCRC operation is flagged as an error.

Before writing or reading any location (in either part of the program), the program issues a call to subroutine XORCK (exclusive-OR check) which tests bits 3 and 9 and sets the XORFLG if the exclusive-OR condition is present.

Subroutine ERRORA is called for any location disturbed from the -1 configuration; subroutine ERRORB is called for any location disturbed from the 0 configuration.

The program prints out errors and repeats when complete without interruption. Upon completion, the program rings the Teletype® bell and then halts if switch 12 is present. A continue from the halt initiates another pass.

If the program indicates an error, use the troubleshooting chart as a guide to locating the fault.

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APPENDIX A
INTEGRATED CIRCUIT DESCRIPTIONS

A.1 INTRODUCTION

In the ME11-L, two integrated circuits (ICs) are shown as boxes in the engineering drawings. All other components are shown in the engineering drawings in logic symbology (gates, inverters, flip-flops). The two ME11-L ICs are the SN74121 Monostable Multivibrator (DEC No. 19-10230) and the SN7528 Dual Sense Amplifier (DEC No. 19-10687). These ICs are described in the following paragraphs, which include an IC package drawing with number designations, an IC circuit equivalent logic diagram, and for the SN74121, a brief description. These descriptions provide lower level logic description as a maintenance aid for troubleshooting the unit to the IC level.

A.2 SN74121 MONOSTABLE MULTIVIBRATOR

This monolithic TTL monostable multivibrator features dc triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fanout to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt trigger input circuitry (TTL-compatible and featuring temperature-independent backlash) for the B-input allows jitter-free triggering from inputs with transition times as slow as 1V/second, providing the circuit with an excellent noise immunity of typically 1.2V. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal latching circuitry.

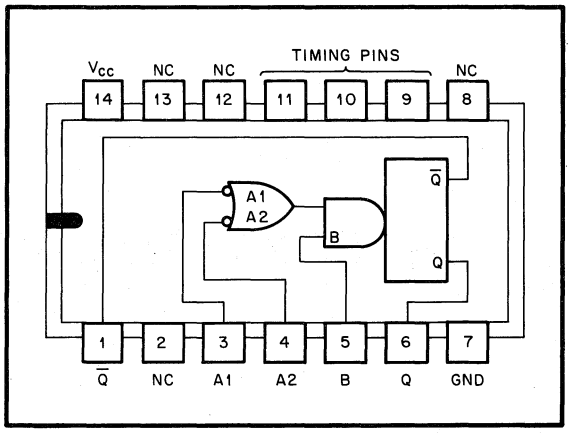
Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 ns to 40 sec by choosing appropriate timing components. With no external timing components (i.e., pin 9 connected to pin 14, pins 10, 11 open), an output pulse of typically 30 ns is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	0	1	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

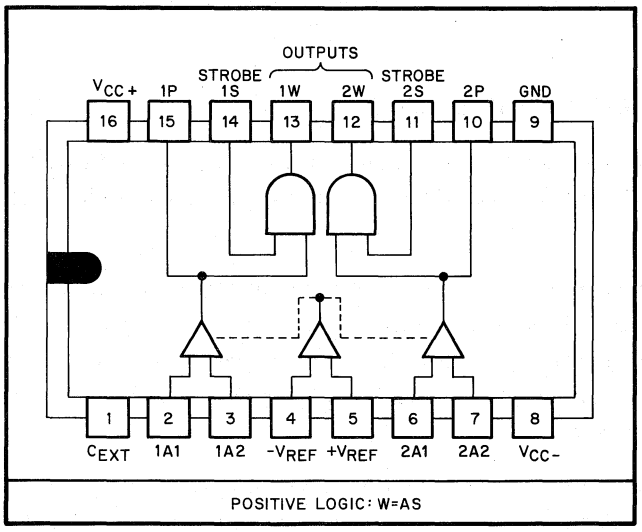
1= $V_{in(1)} \geq 2V$

0= $V_{in(0)} \leq 0.8V$



11-1119

A.3 SN7528 DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS



DEFINITION OF LOGIC LEVEL

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ MAX	$V_{ID} \leq V_T$ MIN	IRRELEVANT
S	$V_I \geq V_{IH}$ MIN	$V_I \leq V_{IL}$ MAX	IRRELEVANT

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

TRUTH TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

11-1122

READER'S COMMENTS

ME11-L CORE MEMORY SYSTEM MANUAL
DEC-11-HMELA-B-D

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