STANDARD WARRANTY

Jorway Corporation, warrants to the original purchaser that equipment of its manufacture is free from defects in material and workmanship. This warranty is effective for a period of one year after shipment of the instrument to the original purchaser.

Liability under this warranty is limited to servicing or adjusting any instrument returned to the Jorway Corporation factory for this purpose. Equipment to be returned for repair under warranty shall be returned transportation charges prepaid. If factory inspection discloses that defect developed under normal and proper use and within the warranty period, repair will be made and equipment returned with transportation charges paid by Jorway. Return shipment will be made via UPS where available or via insured parcel post. Other modes of shipment can be made at the customers request and then only on a collect basis.

If equipment is not covered under the warranty terms, an estimated cost of repair will be submitted to the customer, and upon his authorization, repairs will be accomplished and billed at cost, including U.S.Customs clearance charges and return insured transportation charges, F.O.B. Westbury, New York, U.S.A.

Equipment sold outside the U.S.A. will not be accepted for warranty repair unless prior approval and shipping instructions have been obtained from the Jorway Corporation. If equipment is covered under warranty, shipments will be returned prepaid to the foreign port of entry.

This warranty is expressly in lieu of all other obligations or liabilities on the part of Jorway Corporation. Jorway Corporation does not assume, nor authorize any other person, including representatives of Jorway Corporation to assume for them, any other liabilities in connection with the sale of Jorway instruments.

SECTION I

INTRODUCTION

1.1 PURPOSE OF MANUAL

The purpose of this instruction manual is to present information required for understanding the functions, the electrical and mechanical characteristics and basic principles of the Model 220 Eight Channel Delay Generator (see Figure 1.1). This manual assumes that the reader has some knowledge of CAMAC principles. Complete details on the CAMAC specifications which apply to the Model 220 are contained in references 1 and 3 of Appendix A 1. Additional references of Appendix A 1 provide a broad understanding of CAMAC principles and usage.

1.2 APPLICATION

The Model 220 Delay Generator is a CAMAC module intended to be used to provide a selectable digital delay. A versatile set of controls allow the 8 multiple delay channels to be arranged in a variety of ways. Delay clock can be in terms of N number of events or in terms of time for a real timeclock. Manual controls provide for manually setting or altering any of the eight delays. Delay values may also be set by dataway controls.

The Model 220 may be used in applications requiring selectable or alterable delays, which are related either to a master signal or to each other. For example, trigger pulses staggered in time can be generated by the 220 and used to sequence external equipment.

1.3 MODULE DESCRIPTION

The Model 220 Delay Generator is a triple width CAMAC module providing eight (8) individual delay channels. Each delay channel provides an output pulse which is delayed by N times input clock interval. N may be set from 0 to 99. Each channel has an individual clock and an individual start input. For delays longer than N = 99, channels may be cascaded by connecting the output of one channel to the start input of the next channel.

Channel delays may be set manually by a front panel thumbwheel switch or by appropriate commands on the CAMAC dataway. Delay set from the dataway are in binary form for integers 0 to decimal 99. Each channel has a two digit display showing the current delay in appropriate channel. Delays set are not cleared by clear or initialize functions. Clearing and initialize stop the delay generator and reload the stored delay in each appropriate channel for the next operation.

Delay begins at the next negative going clock transition after a start (negative going) pulse has been applied. If the clock is already low (approximately 0.4 volts) the delay will begin with the start pulse. This assures the negative going delay output can be used to synchronously start cascaded channels.

A common start and clear function are provided for controlling all channels simultaneously.

SECTION II

EQUIPMENT CHARACTERISTICS

2.1 MODEL 220 SPECIFICATIONS

Delay Channels:	Eight individual delay channels.
Channel Delay:	Delay of N between 0 and 99.
Delay Clock:	Delay Clock from 0 to 10MHz. Delay based on negative going edge of clock. Input is TTL[1].
Delay Start:	Negative going edge of start signal begins delay interval. Interval will begin on next negative going edge of clock or with start signal if clock is low. Delay will stop with negative going edge of clock when N is reached. Input is TTL[1].
Delay Output:	Negative going pulse approximately 80 nano second wide when N delay is reached. Output is TTL.
Common Start, Manual:	Front panel pushbutton starts all channels.
Electrical:	Lemo input starts all channels on negative going edge of applied TTL[1] signal.
Common Clear, Manual:	Front panel pushbutton clears all delays to initial conditions reloading current delay number.
Electrical:	Lemo input clears all delays as above by a low TTL[1] signal.
Thumbwheels Delay:	Manual entry of channel delay. Left thumbwheel selects channel number. Two right thumbwheels select channel delay.
Manual Preset:	Front panel pushbutton sets delay in channel selected by thumbwheels.
CAMAC Commands:	
N·F(9)·A(0)·S1	Common Clear, clears all delay channels, presetting stored delay interval in each respective channel.
N·F(16)·A(0)+A(1)+A(2)+A(3)+A(4)+A(5)+A(6)+A(7)·S1	Stores delay interval in binary form from dataway lines W1 thru W7 in each respective channel, A(0) for channel 0 etc. W1 is LSB. Binary numbers higher than decimal 99 are prohibited.

N·F(28)·A(0)·S1	Common Start, Enables start input on all channels. Delay begins on next negative edge of clock pulse or at S1 if clock is low.
Z S2	Initialize performs same function as N·F(9) A(0)·S1.
N	Front panel light flashes when module is addressed.
X	Command accepted response is generated for all the above commands excluding Z.
Power Requirements	+6 volts @ 3000 ma.
Size	Three (3) width CAMAC module with protective side shields.

SECTION III

OPERATING INSTRUCTIONS

3.1 GENERAL

The Model 220 Delay Generator contains a versatile set of controls and indicators for both operating the generator as well as determining its status. The operation of the Model 220 may be considered as being either under manual or dataway control. The manual controls are however always active and can be used to alter any operation in progress.

3.2 INSTALLATION

3.2.1 DATAWAY CONNECTIONS

The Model 220 must be installed in the control station and adjacent normal station of a Camac crate, thereby having access to all Dataway lines. The following installation procedure is recommended:

Preferably with the power off, insert the Model 220 into the crate guides. The module should slide freely and easily engage the Dataway connector. Do not use the jackscrew to force the module into the connector! Take up on the jackscrew until resistance is felt, then press on the front panel to engage the module into the mating connector as far as it will go. Repeat this procedure until the module is fully seated in the connectors.

CAUTION: If the module does not easily engage with the Dataway connector, check the appropriate crate dimensions against the Camac specifications. All Jorway modules are aligned in a jig to assure proper dimensions before they are shipped. Under no circumstances should the module's finger area be filed in an attempt to engage the module with the Dataway!

3.3 MANUAL OPERATION

3.3.1 MANUAL DELAY LOADING

Upon application of power to the Model 220, the display may come up in a undetermined state. The delay storage registers are not cleared by Z·S2 on the dataway or by the front panel clear. This is done so that preset delay intervals are not lost during system initialization. Each delay interval must be loaded into their respective channels. Manually each channel is loaded by selecting the appropriate channel number on the left thumbwheel and the delay value on the two right thumbwheels. The preset pushbutton when depressed loads the delay value into the appropriate channel. The actual value of the delay is indicated by a two decimal digit display for each channel.

3.3.2 MANUAL START

Depressing the Manual Start pushbutton will initiate the delay interval in all eight channels.

3.3.3 MANUAL CLEAR

Depressing the Manual Clear pushbutton will terminate all delay intervals in progress and set up all circuits for the next start.

3.4 SIGNAL INPUTS AND OUTPUTS

3.4.1 CLOCK INPUTS

Lemo inputs are provided for each individual delay channel. Each input can accomodate a clock frequency up to 10MHz.

3.4.2 START INPUTS

Lemo inputs are provided for each individual delay channel. Each start input may be used to begin the delay interval for that channel without regard to the operation occuring in other channels.

A common start Lemo input may be used to start all delay channels.

3.4.3 DELAY OUTPUTS

Lemo outputs are provided for each individual delay channel. Each output will occur at the delay setting N times the input clock interval. The delay may be used to drive external circuits or may also be connected to other channal start inputs for nested delays.

3.4.4 CLEAR INPUT

A single clear input Lemo may be used to terminate all delays in progress and set up all channels for a start input.

3.5 DISPLAYS

3.5.1 CHANNEL DELAY

The value of each channel delay is displayed on a 2 decimal digit LED display. This display shows the current delay value regardless of whether the delay value occured from either the dataway or the manual loading.

3.6 DATAWAY OPERATION

Dataway commands are available to provide control of most functions of the Model 220. Controls provide the following actions.

Common Clear;	Dataway signal equivalent to section 3.4.4.
Common Start;	Dataway signal equivalent to section 3.4.3.
Load Delay Interval;	Dataway command writes delay interval to each channel as determined by subaddress. The Model 220 makes a binary to decimal conversion for the dataway delay value(in binary) before loading the dealy interval. Binary delay values greater than 99 will give incorrect results.

SECTION IV

PRINCIPLES OF OPERATION

4.1 GENERAL

The following circuit description is intended primarily as an aid for those who may be required to service the Model 220 in the event that a malfunction occurs. Others however, may also find it of interest. The appropriate schematic should be used in conjunction with the text in order to follow the description. It should be noted that the schematic is implemented in positive logic. Thus logic "1" represents a high signal and logic "0" a low signal. This is done to more easily conform to the TTL logic descriptions commonly in use. Dataway pin designations however, are negative logic consistant with the CAMAC standards.

4.2 BLOCK DIAGRAM DESCRIPTION

4.2.1 SIMPLIFIED DELAY CHANNEL DESCRIPTION; MODEL 220A

Figure 4-1 illustrates in a simplified manner, the operation of a delay channel. Common START, CLEAR and a number of specific dataway commands are not shown. These functions are covered in Section 4.3.

CLOCK INPUT pulses applied to "AND" gate A are inhibited from triggering the monostable by a flip-flop when it is in the set state. Upon application of a START INPUT the flip-flop is reset and clock pulses now trigger the monostable. The monostable is used to standardize count pulses applied to the counter. The counter having been loaded with a number equal to the selected delay, increments down for each count pulse. Upon reaching zero, the next clock pulse (N + 1 clocks = N clock intervals) passes through the counter as a borrow clock and becomes the DELAY OUTPUT. The borrow also initiates a command to set the flip-flop terminating the delay interval and reloads the counter with the current delay value held in a 8 bit latch. Each channel has a storage latch which can be loaded upon commands from either the front panel MANUAL PRESET or the Dataway. Data for the latch comes from the thumbwheel switches in BCD form or from the Dataway. In the case of dataway data, binary coded data on the dataway is converted to a 2 decimal digit BCD form for loading into a channel latch.

A self cycling multiplexer interogates the latches for all channels and displays the current delay value for each channel on a two decimal digit display.

4.3 DETAILED CIRCUIT DESCRIPTION

The following circuit description should be used in conjunction with schematic drawing 220-J-007, 220-D-006

4.3.1 DELAY CHANNEL FRONT END CIRCUITS; MODEL 220A (Dwg 220-D-006)

Each of the eight delay channels have identical front end circuits. Some IC's are paired between channels i.e. channel 0 & 2, 1 & 3, 4 & 6 etc. This description is given for channel 0, but applies to any input channel except for the actual IC pin assignments which differ for the paired channel.

Assuming that a clear or initialize has occured, flip-flop 24 will be preset via pin 2 so that the Q output at pin 15 is high.

This preset will have occured when a low signal (stop) was present at IC 80-11 (dwg. 007). This signal may occur as a result of a borrow from the channel counter at IC 80-13. The preset signal may also occur by a common CLEAR at IC 81-0 or a positive pulse at IC 81-8, whenever the channel delay is loaded. With the Q output of flip-flop 24 high, gate 23-2 will be closed. At a negative transition of the START INPUT applied to 24-1, the Q goes low enabling gate 23-2. If the CLOCK INPUT MONO is low the negative transistion of Q causes mono IC 15 to trigger because of the positive transition at 15-12. If the CLOCK INPUT is high when 23-2 goes low, the mono will trigger on the next negative transition of 23-3. These signal conditions are illustrated in Fig. 4-2 and 4-3. A start input may also occur by a COMMON START. This COMMON START clears the flip-flop by a negative signal at the clear input (IC 24-3, dwg. -006).

The gate associated with the CLOCK INPUT (23 - 1 on dwg. -006) may have a start and clock signal which are not synchronous. As a result a narrow pulse i.e., shorter than that required to trigger the mono, from 23-1 may occur under some start conditions. The behavior of generally all monostables under these conditions is to issue at their output a narrow pulse instead of actually triggering. To prevent this narrow pulse from falsely triggering the counter, an integrator is provided by R5 and C3. In order to trigger the counter the mono stable must have a full output with a negative signal at IC 8-5 and a delayed negative signal caused by the integrator at 8-6. These signal conditions are illustrated in fig. 4-0.

The use of the integrator necessitates a longer monostable pulse than would otherwise be required. At clock rates approaching 10MHz the monostable duty cycle begins to approach 100%. To provide the counter input with a minimum width clock pulse; a schottky monostable consisting of IC 7-3 and IC 8-13 (dwg -006) is employeed. At each negative transistion of the CLOCK INPUT a negative pulse from this monostable at IC 16-10 cuts-off the gate output at 16 - 8 for its duration.

For high duty cycle operation of mono IC 15, this action assures a minimum negative count pulse width.

4.3.2 DELAY COUNTER CIRCUITS

Each delay channel is composed of two decade presetable counters (IC44 and 71 for channel 0) and two 4 bit latches (IC28 and 53 for channel 0) which holds the channel delay value. When a channel delay value is loaded, a positive clock pulse occurs at IC28 and 53 pin 4. This clock pulse loads the contents of the data at the D inputs of IC53 (unit digit) and IC28 (tens digit) into the latches. This data is transferred to the latch Q outputs at the rising edge of the clock. The clock is also applied as a negative clock at the counter load inputs (pin 11 of IC44 and 71) through gates IC81-8 and IC80-10. This initially loads the counter with the correct delay value. As the monostable fires, a positive going pulse approximately 80ns in width is applied to the down clock input of the unit digit counter, IC71-4. The counter is incremented downward at each trailing edge (positive going) of the monostable pulse. When the counter reaches a count of zero, the next down clock is passed onto the tens digit counter (IC44) via the borrow output (IC71 pin 13). The down counting process continues until both counters reach zero. At this time the next clock will be passed through both counters and appear as a borrow from the tens digit counter (IC44-13). This negative going borrow pulse is applied to IC89 pin 7 via gate 80-13. This presets flip-flop 89 gating off monostable IC90-4 and terminating the delay interval. This borrow output pulse is also passed through inverter IC20-13 for channel 0 becoming a positive going pulse. This positive pulse is again inverted by IC 81 pin 11 and 12 to drive the DELAY OUTPUT Lemo. The trailing edge of the pulse at IC20-12 is differentiated by C6, R42, and R43 and applied to IC80-9. The resulting negative pulse at IC80-8 forms a load pulse for both counters, reloading them with the correct delay value for the next operation.

4.3.3 DATAWAY CIRCUITS

Dataway circuits are enabled by the N line signal going low at IC2-5. The N signal is also applied to a monostable composed of IC8A-13 and Q9. This monostable illuminates the N indicator CR3 for approximately 100ms or the duration of N, whichever is longer. F2 and A8 are gated with N at IC2-6 so IC2-4 is high for $N \cdot \overline{F2} \cdot \overline{A8}$. As a result the module does not respond to any codes with either A8 or F2 being true (logic 1 dataway level). Unless a manual PRESET operation has been initiated, IC5-4 will be high. When IC5-5 goes high in response to $N \cdot \overline{F2} \cdot \overline{A8}$, the output IC5-6 goes low. This low signal is applied to IC73-10 which inhibits any manual preset requests, which have not already started. If a manual PRESET operation is in progress when a $N \cdot \overline{F2} \cdot \overline{A8}$ occurs, the preset mono with output at IC63-6 will be low and gate IC5-6 will remain

high until IC63-6 goes back to its quiescent high state. When IC5-6 does go low, it causes the multiplexer IC4 to switch to the A input,thus gating the subaddress lines A1, A2, and A4 to the decoder IC12. At any time a dataway operation is not occuring, the decoder A12 responds to the binary address from the thumbwheel address switch thru the B inputs of multiplexer IC4. Dataway decoding for A(0) thru A(7) are performed in IC1 with A(0) corresponding to Channel 0, A(1) to Channel 1 etc. Subaddress above A(7) are not effective because A8 is included in the enable gate IC5-10. The manual address switch is restricted to addresses 0 thru 7.

Function decoding is performed in IC3 with pin 11 low for F(9) + F(11), pin 9 low for F(16) + F(18) and pin 5 low for F(28) + F(30). The codes of F(11), F(18) or F(30) are not effective since F2 is included in the enable gate IC5-9. The function code F(16) is applied to gate IC2-9. When the module enable gate IC5-6 also goes low, the output IC2-10 will go high enabling gate IC1-10. A positve pulse (dataway S1) applied to IC1-9 results in a low going pulse at IC1-8 which passes through IC5-2 and IC13-8 and is applied to all gates in IC10 and 11. One output of IC12 will be low selecting an appropriate channel. Using Channel 0 as an example, IC11-4 will go high for the duration of S1. This signal is applied as a load clock to the latches IC28 and 53 for Channel 0. These latches store the data which is present at their D inputs.

Unless a dataway write command ($N \cdot F(16) \cdot \overline{A8}$) is present, the common line to gates in IC 7 and 15 will be high allowing the thumbwheel to control the data applied to the channel delay latches. Thumbwheel delay data is in BCD form so the delay is stored directly in BCD. The high signal which enables the preset gates, also disables IC14 and 16 via their strobe input pin 15. IC9-4 is also disabled by a low signal at pin 6. IC14, 16, and IC9-4 perform the function of a 2 decimal digit binary to BCD decoder. When a $N \cdot F(16) \cdot \overline{A8}$ command is present, the high signal at IC2-10 enables gate IC9-6 and the remainder of binary to BCD decoder through IC13- 6. The thumbwheel switch gates IC7 and 15 are now disabled by a low on their common line.

During dataway address operations, IC12 responds to subaddresses. A A(0) 11 result in a low at IC13-13 and a high at IC5-13. This results in a low at IC5-11 and IC2-3 and 12. This low in combination with the decoded F(9) results in a high at IC2-13 for $N \cdot F(9) \cdot A(0)$ or with the decoded F(28) results in a high at IC2-1 for $N \cdot F(28) \cdot A(0)$.

A $N \cdot F(9) \cdot A(0)$ signal generating a high at IC2-13 enables IC1-1. At dataway S1 time, the positive going S1 strobe at IC1-2 is gated thru IC1-3, IC1-6,IC72-13 and IC63-3, resulting in a common clear signal for all channels, i.e. a positive pulse at IC81-9 for channel 0. A dataway $Z \cdot S2$ can also generate a common clear. In this case Z and S2 are combined in gate IC8A-10 to cause a positive pulse, the duration of S2 on the common clear line.

A $N \cdot F(28) \cdot A(0)$ signal generating a high at IC2-1 enables IC1-13. At dataway S1 time, the positive going S1 strobe at IC1-12 is gated through IC1-11, IC13-10 and inverted by IC72-1 to drive the common start line of all channels, i.e. IC89-8 for channel 0.

X line decoding is performed in IC9-1,10,13. Each of the three dataway functions $F(9) \cdot A(0)$, $F(28) \cdot A(0)$, and $F(16) \cdot A(0\text{-}7)$ are coupled to the dataway by an open collector IC9 gate.

4.3.4 MANUAL AND FRONT PANEL CONTROLS

Common CLEAR can be achieved by application of a negative going signal to the CLEAR Lemo connector or by depressing the CLEAR Pushbutton. Either signal results in IC73-6 going high. This high signal passes through gate IC72-13 and IC63-3 as a common clear for all channels i.e. through IC81-9 for Channel 0 etc. IC82-8 forms a flip-flop with IC73-6 to debounce the CLEAR switch.

Common START can be achieved by application of a negative going signal to the START Lemo connector or by depressing the START Pushbutton. Either signal results in IC73-12 going high. The leading edge of this high going signal triggers a monostable comprised of IC72-4 and IC72-10. The monostable generates a positive pulse at IC72-10 which is inverted at IC72-1 and becomes a common start signal for all channels e.g. IC89-8 for Channel 0. IC82-3 forms a flip-flop with IC73-12 to debounce the START switch.

Manual PRESET is used to manually load any of the Model 220 channels. The channel to be loaded is selected by the "Channel" Thumbwheel switch while the data is set on the Channel "Delay" thumbwheel. The selection of an addressed channel and multiplexing of data to the appropriate channel is explained in Section 4.3.3.

When the PRESET pushbutton is depressed Gate IC82-11 will go high. If there is no addressed dataway operation in progress IC73-10 will also be high and IC73-8 will go low. The cross coupling back to IC82-12 forms a debouncing flip-flop for the PRESET switch. If an addressed dataway operation is in progress when the PRESET pushbutton is depressed, gate input IC73-10 will be low. Not until the dataway operation is completed will IC73-10 return to a high state. If the PRESET pushbutton is still depressed, the output IC73-8 will then go low as the IC73-10 goes high. When IC73-8 goes low it forms a trigger for a monostable comprised of IC82-6 and IC63-6. When, triggered, this monostable issues a negative pulse at IC63-6 which is applied to IC5-4 and IC5-1. At IC5-4 this negative signal inhibits dataway cycle from being processed for the duration of the negative pulse. The duration of this inhibit is always short enough for the dataway cycle to commence before S1 time. The negative pulse at IC5-1 passes through IC5-3 and IC13-8 and is applied to IC10 and 11. The pulse will pass through the appropriate gate in IC10 and 11 as a load latch signal, in accordance with the address selected by the channel thumbwheel e.g. IC11-4 for channel 0.

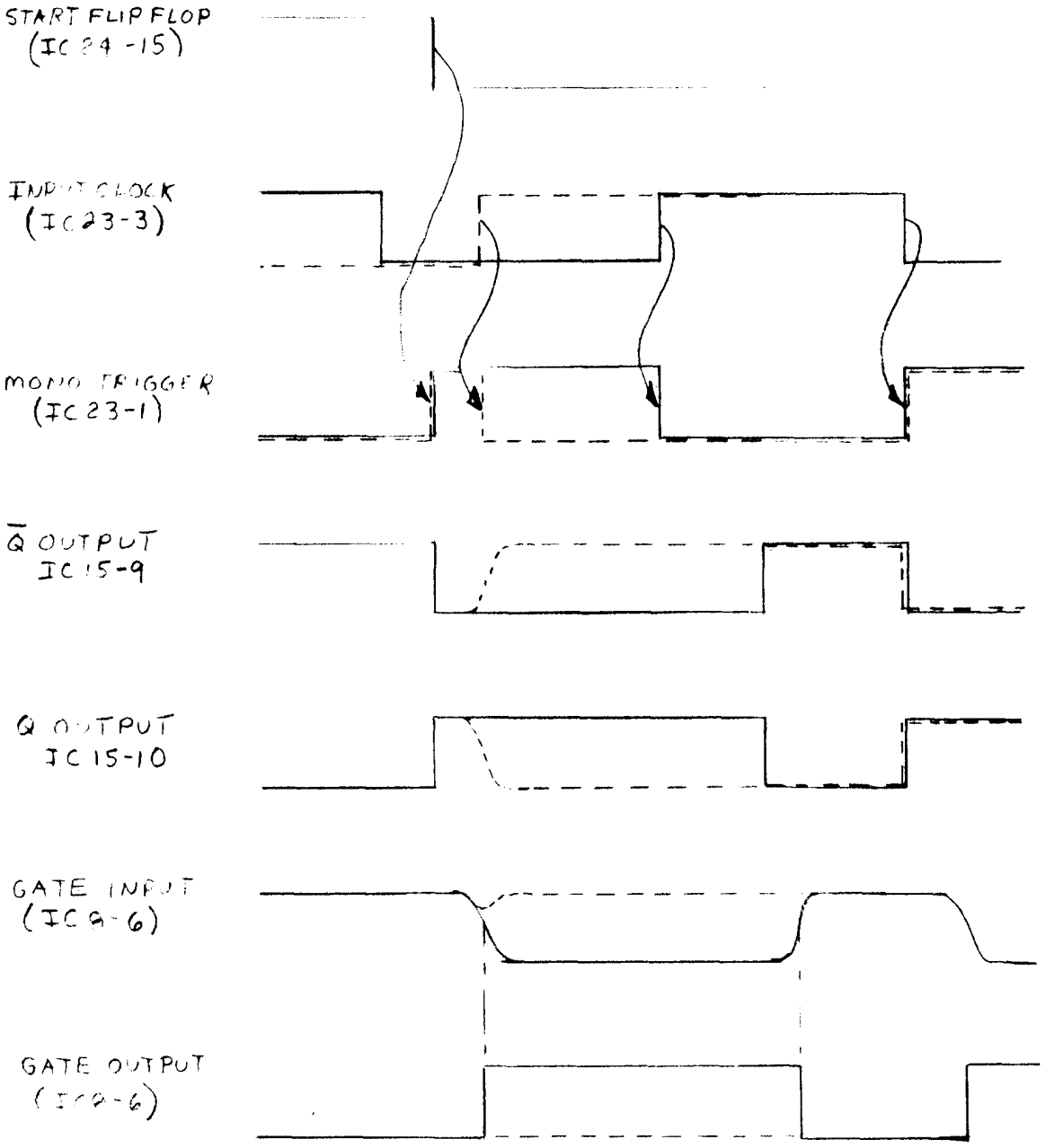
4.3.5 DISPLAY CIRCUITRY

Each Delay Channel has a two decimal digit display. The data for this display comes from the units and tens digit latch for each channel. Each channel contains a set of four gates for the units digit and four gates for the tens digit which are used to gate data onto a units display bus and a tens display bus respectively. For example, IC62 gates channel 0 units data onto a units display bus associated with the outputs of IC62. Similarly, IC36 gates channel 0 tens data onto a tens display bus

The LED display chip utilized in this Model 220 is a 4 decimal digit chip in which access to the digits is by multiplexing. Since only one digit in the chip can be driven at one time, the units and tens data for a specific channel cannot be displayed at the same moment. For this reason channels are paired so that as the units digit from one channel is being displayed, the tens data for the paired channel in the second 4 digit chip is being displayed. Using Channel 0 as a reference,Gates in IC62 are enabled (e.g. IC62-11 high) as Gates in IC35 are enabled for Channel 2 tens

data (e.g. IC35-3 high). In a similar manner gates in IC36 for Channel 0 tens data are enabled (e.g. IC36-3 high) as gates in IC61 are enabled for Channel 2 units data (e.g. IC61-11 high). As each channel data is gated onto the display busses, IC17 turns on the appropriate digits to be displayed via Q1 thru Q8.

Display multiplexing is driven by an IC oscillator consisting of IC63-11 and IC 63-8. This oscillator drives a binary 3 digit display counter IC8 (D output not used) which in turn is decoded by a 3 to 8 line decoder IC17 (D input not used). As the display counter advances, the outputs of IC17 turn on the appropriate channel data gates and pull low one transistor of the group Q1 thru Q8. These transistors serve to turn on a pair of LED digits, one digit for a tens display and one digit for a units display. Multiplexers IC45 and IC54 serve to provide at their output either tens data or ones data depending on the state of the select input IC45 and 54 pin 1. This pin is connected to the A input of IC17 so that the multiplexers alternate input selections as the display counter advances. The outputs of IC45 and 54 as well as Q1 thru Q8 emitters are connected to a display board which contains additional circuitry (Refer to schematic 220-C-002). On schematic 220-C-002 data from the multiplexer is coupled to an appropriate 4 to 7 line decoder IC3 and 4 for generation of the 7 line code for the LED digit displays. 7 line coded signals are buffered by emitter followers in IC1 and 2 which provide sufficient drive for a multiplexed display. Transistors Q1 thru Q8 are connected to appropriate digits in the LED display. Table figure 4-4 indicates the display sequence for all channels and their relationship to the outputs of IC17 on schematic 220-J-001.



INPUT MONOSTABLE WAVEFORMS

FIG 4-0

SIMPLIFIED BLOCK DIAGRAM OF DELAY CHANNEL

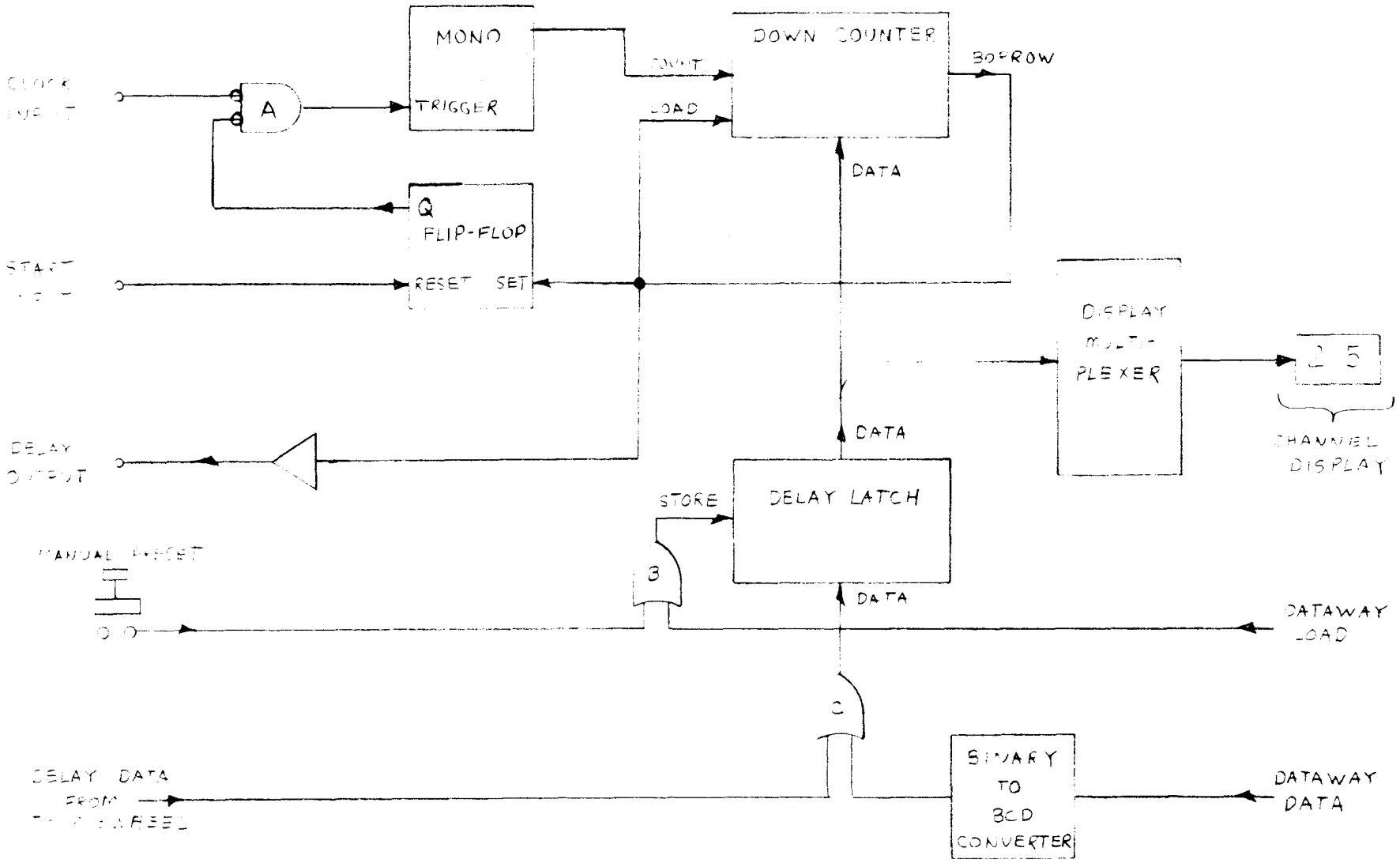


FIG. 4-

INITIAL FIRING FROM START INPUT

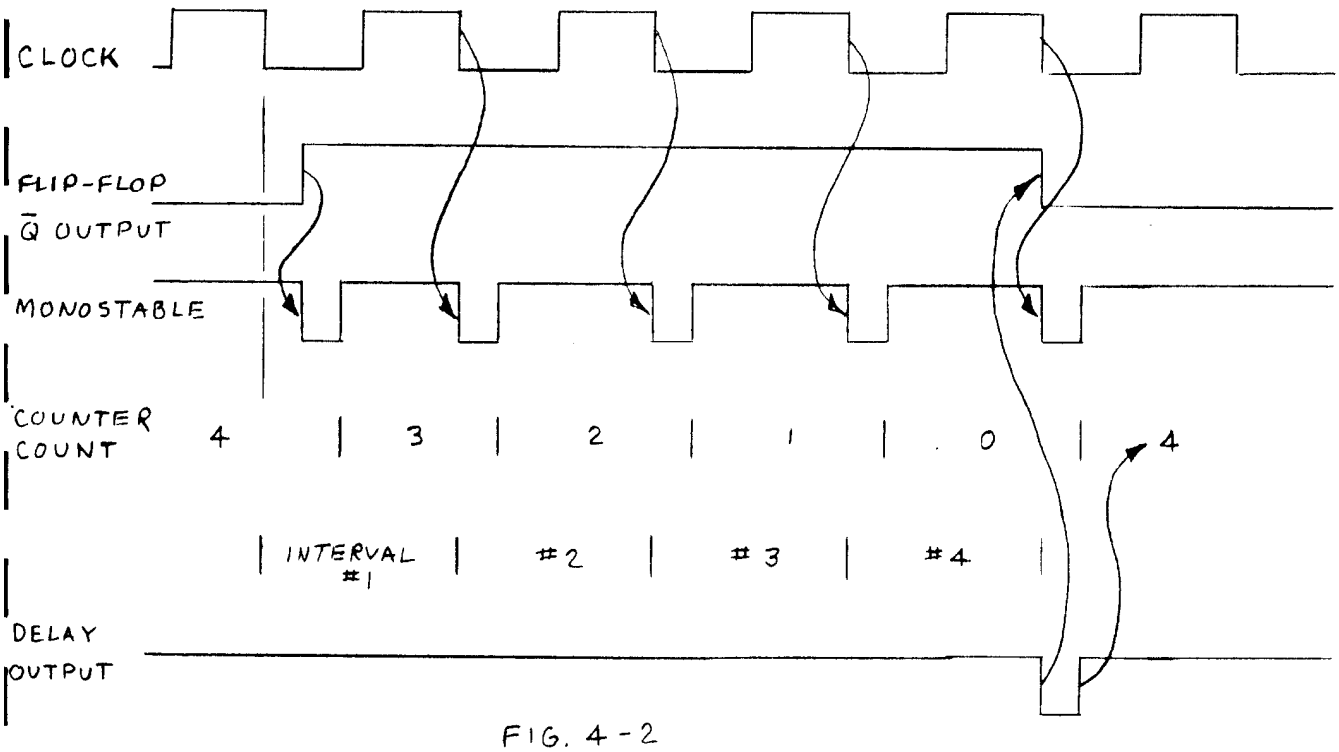


FIG. 4-2

INITIAL FIRING FROM CLOCK INPUT

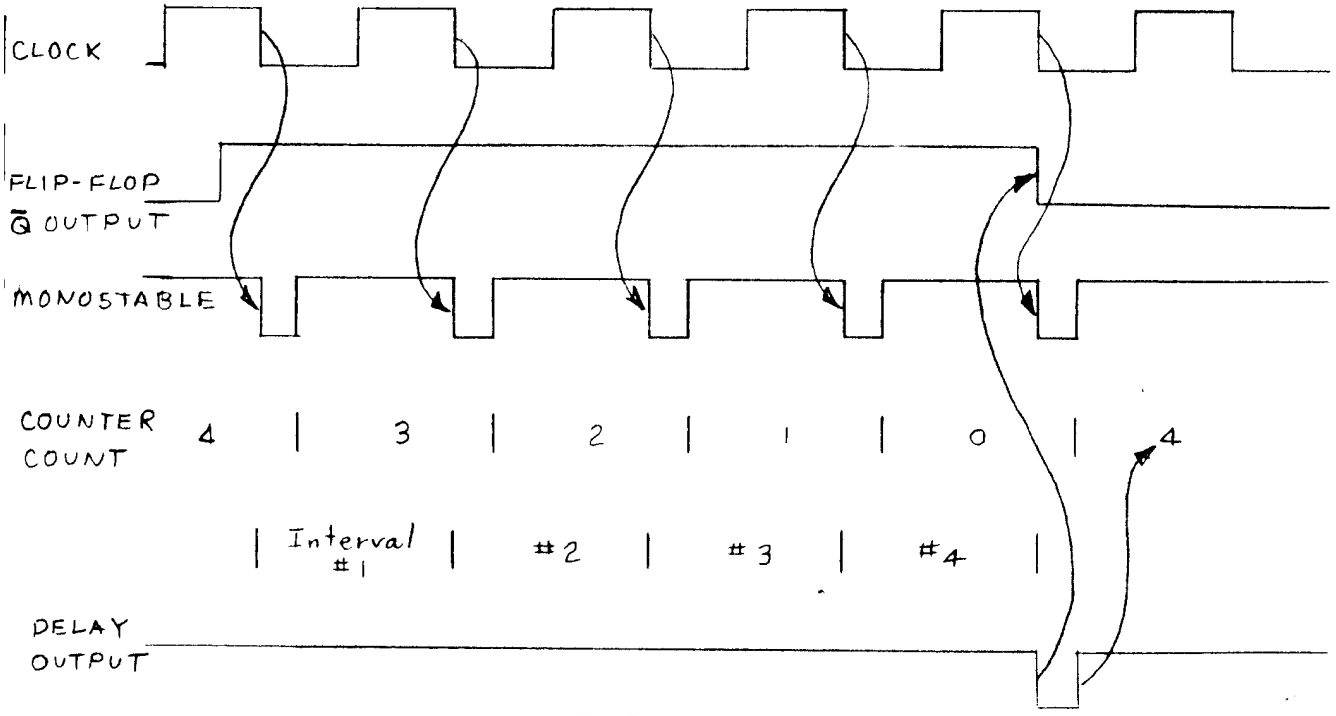


FIG. 4-3

SECTION V

SERVICE

5.1 GENERAL

Jorway instruments are conservatively designed using quality components with high reliability as a prime objective. In addition, all units are manufactured to rigid quality control standards and are thoroughly tested and run in before shipment. As a result, long life and trouble-free operation can be expected. Nevertheless, occasional malfunctions may occur, necessitating service of the unit.

Most Jorway products are covered by our standard one year warranty. Instruments requiring service within the warranty period should be returned to the factory for repair under its terms (see warranty printed elsewhere in this manual). We also strongly recommend that instruments which are out of warranty be returned to the factory when service is necessary. Jorway personnel, being intimately familiar with our products, are able to efficiently isolate any problem and restore the unit to proper operating condition.

If, for any reason, the user decides to repair an instrument it should be done by qualified personnel, experienced in working with this type of equipment. The information contained in this manual should be read and understood before attempting to troubleshoot the unit, since familiarity with the principles of operation and circuitry are essential. Utilizing the schematic diagrams and other material in the manual, it should be possible for a skilled technician to determine the cause of a malfunction and effect its repair.

5.3 COMPONENT REPLACEMENT

If it is necessary to replace a component on the circuit boards, extreme care should be exercized so that the board is not damaged. Most important is that excessive heat is not applied to the printed circuitry. Use the minimum amount of heat necessary to melt the solder. Multilead components, such as dual in-line integrated circuits are difficult do remove and it is usually better to cut the leads of suspected compo-

nents and remove the remaining pieces one by one from the component holes. The use of a suitable solder extracting device will also greatly aid in the removal of such components. The holes should be thoroughly cleaned out before the new component is inserted. Do not use force in either removal or insertion of components as damage to the plated through holes may result. Component or IC leads should be free and not attached to the side of a plated through hole before an attempt is made to extract the component or pin.

SECTION VI

OPTIONS

6.1 GENERAL

Standard instruments which contain options carry a model designation with a suffix X. In general the serial tag on the side cover of the module will indicate the option or options which have been incorporated in the module. When consulting the factory, please indicate the serial number and options included in the module in question.

6.2 OPTION 1; +15 VOLT OUTPUT

6.2.1 DESCRIPTION

Model 220 Delay Generators containing this option, provide in addition to the normal TTL DELAY OUTPUT signal at the front panel, an additional high power output. This option 1 output is via a p.c.card 36 pin edge connector at the rear of the module,(type 3VH18/1JND5 Viking or equiv.). These outputs are often used to drive external devices such as SCR circuits. The output from each channel provides a +15 volt minimum amplitude pulse into a 50 ohm load to ground. Pulse width at the 50% amplitude point is approximately 100ns. Rise time is approximately 20ns.

6.2.2 OPERATION

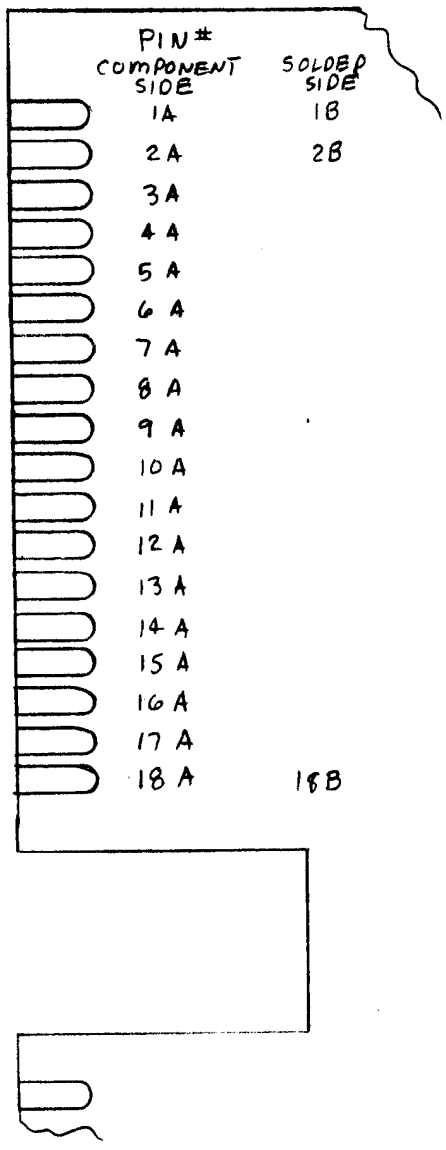
Use of the high power outputs is accomplished by connecting the external load to the appropriate signal pair on the rear connector. A separate ground return is provided for each output channel. Signal assignments are shown in Table 6-1.

6.2.3 PRINCIPLES OF OPERATION

With reference to schematic 220-J-002 and the description paragraph 4.3.2, positive borrow pulses are the tens counter inverter (e.g. IC20-12 for Channel 0) are connected to an auxiliary p.c. board. The circuitry for this board is shown on schematic 220-D-003. The positive borrow pulse is applied to a inverter(e.g. IC1-5 for Channel 0). As the inverter goes low it causes the driver transistor base to go negative with respect to its emitter. An external load is in turn pulsed with approximately +15 volts as the driver saturates. A current limiting resistor in the emitter circuit controls the maximum saturation current and protects the driver from shorts. As the driver saturates, the majority of the supplied energy is provided by a .1 mfd capacitor (C2 for Channel 0). After approximately 100ns, the borrow pulse terminates and the driver transistor goes off. The .1 capacitor now recharges through a 220 ohm resistor connected to the +24 volt supply. This procedure eliminates the loading of the +24 volt supply of up to 2.5 amps if all outputs should trigger at the same time.

CHANNEL NO.	PIN #	
	SIGNAL	SIGNAL RETURN
0	11B	11A
1	10B	10A
2	9B	9A
3	8B	8A
4	7B	7A
5	6B	6A
6	5B	5A
7	4B	4A

AUXILLARY CONNECTOR



VIEW FROM COMPONENT SIDE

TABLE 6-1

OPTION 1 PIN ASSIGNMENTS

6.3 OPTION 2; RECYCLE MODE

Option 2 provides the Model 220A with a user selectable alternative mode of operation. Activating this mode allows the unit to operate as a Divide by N counter rather than the normal Delay by N function. Individual channels may be chosen to operate in either mode, thus permitting mixed operation with some channels functioning as delay channels and others as divide by N channels.

In the Divide by N or RECYCLE mode, the input CLOCK frequency is divided by the value N, set either by Dataway command or manually via the front panel thumbwheel switches. The divided frequency appears at the front panel OUTPUT connector as a negative going TTL level pulse approximately 80 ns wide. The START input is not used in the RECYCLE mode; the counter continuously recycles as long as an input clock signal is applied. Input clock frequency in this mode is limited to a maximum of 2.5 MHz and for proper operation the input clock should be low for a minimum of 300 ns. Although in the NORMAL or delay mode channels may be cascaded for additive delays, in the RECYCLE mode cascading of channels is not normally permitted.

The Model 220A is shipped from the factory set for NORMAL (delay by N) operation. To select the RECYCLE (divide by N) mode, it is required that the left side (viewed from the front) cover be removed to gain access to the selection switches which are internally mounted on the circuit board. To remove the cover remove the six (6) flat head screws securing the cover and lift it off Locate the four (4) miniature rocker switch assemblies mounted at the edge of the circuit board closest to the front panel. Each of the four switch assemblies contains two independant switches. Each switch controls a single channel. The channel affected is marked in front of each switch.

Depressing the rocker at the rear of the switch selects the NORMAL mode, while depressing the rocker at the front selects the RECYCLE mode (see Fig 2-1). After the channel(s) have been selected to operate in the desired modes, replace the left side cover.

Although it is stated above that cascading of channels is not normally permitted, it is possible to cascade channels (the OUTPUT of one channel connected to the CLOCK input of another) with the following provision. The output of the second or succeeding channels will not produce a frequency equal to $\frac{f}{N}$, but will result in an output of $\frac{f}{N+1}$. To achieve a divide by N factor it is necessary to load N - 1 into the channel's delay register. The first channel remains a divide by N channel provided the requirement that the clock be low for greater than 300 ns is maintained. If the clock to the first channel (whether or not it is cascaded) is low for less than 300 ns this too will result in a divide by N + 1 output.

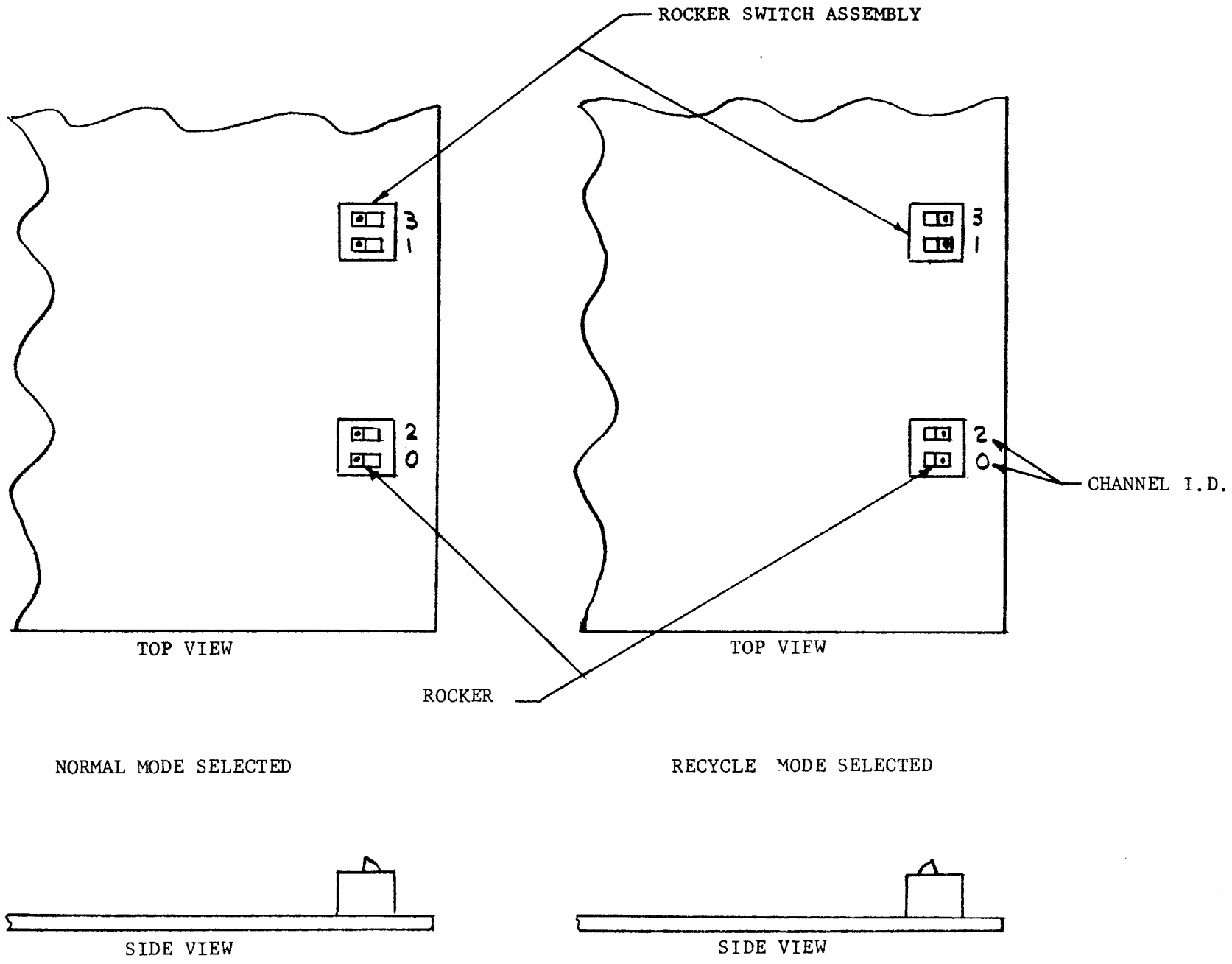


FIG. 6-2 MODEL 220A MODE SELECTION

6.4 OPTION 3; DATAWAY READBACK OF DELAY VALUE

Option 3 equips the Model 220A with the ability to read out the delay values set in each of the eight channels. An additional Dataway command, N·F(0) A(X), where X = the channel number 0 through 7, is provided to accomplish the readback function. Execution of a Read Data command gates appropriate data (in binary format) onto Dataway Read lines R1 through R7. Dataway X = 1 and Q = 1 are asserted in response to a valid read command.

Delay data loaded into the Model 220A is stored in BCD format in 16 data latches (Tens and Units for each channel). To read out the delay data in a conventional manner, i.e., gate each channel's data from the latches, would require an inordinate amount of wiring to be added to an already complex instrument. A more efficient design, permitting much simpler construction, is used which derives the delay data from the existing display multiplexer. The multiplexer contains all the required data on time shared basis. Only eight data lines (instead of 64 using the conventional approach) need to be wired to the readback circuitry utilizing this scheme.

Tens and Units BCD data are demultiplexed and stored in a 32 word x 4 bit register file (memory). On receipt of a Read Data command the desired channel data is accessed from the memory via appropriate subaddress. After a BCD to binary conversion, the data is transferred to the Dataway Read lines.

One complete multiplexer cycle is required to write all data into the memory, the multiplexer operating at a rather slow rate (3 millisecond cycle time). In most cases this causes no problem since the memory is continuously being refreshed with the same data. However, when a change in data occurs, it can take up to one multiplexer cycle for the new data to be written into the memory. This imposes a constraint on the time that data is available for readback after new data is loaded. Data should not be read less than 4 milliseconds after a change in delay. This assures that sufficient time has elapsed so that data read out will be current. Therefore, a Read command should not follow a Write command by less than 4 milliseconds. When programming commands to the Model 220A, one should bear this in mind. If this cannot be assured, a feature has been incorporated into the Option 3 design which will warn of the readout of possible erroneous data. If a Read command follows a load data operation (either from the Dataway or manual load) by less than 4 $\pm$ 20% milliseconds, Dataway Q = 0 will be asserted instead of the usual Q = 1. Thus, the state of Dataway Q in response to a Read Data command indicates the validity of the data being read out. This feature is implemented by triggering a 4ms monostable whenever data is loaded. During the active time of the mono, Q response is inhibited causing Q = 0 to be asserted. To prevent Dataway Q from being reasserted in the middle of a Dataway Read cycle if the mono should expire at such time, Q = 0 is staticized until the end of the Read command.

The circuitry for Option 3 is located on a circuit board mounted one CAMAC station to the left of the main board. Communication with the Dataway for Readout, X, Q, and most of the F and A lines is via this board. Dataway N (and several A and F lines) come from the main board so that the read data command is addressed (N) at the right hand station number as are all other commands to the module.

6.5 OPTION 4

6.5.1 GENERAL DESCRIPTION

Option 4 is designed to provide additional versatility to the Model 220A, thereby extending its usefulness to applications beyond the standard unit's capabilities. The salient features of this option are described in the following paragraphs.

Three modes of operation are provided and may be selected by the user: Pulse, Gate, and Toggle. Selection is made by means of a pair of internal switches for each channel. Intermixed operation is permitted, i.e. some channels may be set to operate in the pulse mode, while others may be set for gate or toggle operation.

6.5.1.1. PULSE MODE

The pulse mode is the way the Model 220A operates when not equipped with Option 4. Due to circuitry constraints, the standard unit's output pulse width is limited to approximately 50 to 80 ns and may vary from channel to channel within this range. Option 4 units have a more uniform output pulse width which is set at nominally 100ns. By installing an appropriate value capacitor in a space provided on the circuit board, and implementing a jumper strapping arrangement, the user can obtain virtually any output pulse width. Each channel has provision for its own capacitor and jumper strap. Thus, any or all of the channels may be selected to output a wider pulse, all channels being independant of each other. The normal (100 ns wide) pulses can be restored to any channel by simply removing the jumper strap associated with that channel. The added capacitor need not be removed but can be left in place for future utilization.

Through the use of a pair of unique matrix switches, any of the eight delay signals generated by the Model 220A may be routed to any of the front panel output connectors. If desired, a single delay output can be routed to multiple output connectors providing additional fan out capabilities and eliminating the need for T connectors.

In addition to the usual output signals generated at the selected delay intervals, the Common Start signal may also be used to generate an output pulse at any of the output connectors.

6.5.1.2 GATE MODE

Gate mode operation uses any two delay channel signals (or the Common Start signal) to form a gate. By means of the matrix switches, signals desired to start (set) and stop (reset) the gate are selected and switch the gate to the chosen output connector.

6.5.1.3 TOGGLE MODE

Toggle mode operation uses one delay signal (or the Common Start signal) to toggle an output from one state to the other with each applied signal. As in the other modes, any resulting signal can be routed to any output connector.

6.5.2 OPERATION

The Model 220A as shipped from the factory is programmed to operate in a "transparent" manner, i.e., it behaves as if Option 4 is not installed. The only difference between this and a standard Model 220A is that as described previously the output pulses are somewhat wider (100 ns instead of the standard unit's 50 to 80 ns). Drawing 220-A-602 shows the mode and matrix switches set for the above condition.

If it is desired to operate in any other mode it will be necessary to program the Option 4 circuitry accordingly. This will necessitate removal of the left hand (viewed from the front) side cover. To remove the cover, remove the six (6) flat head screws securing it and lift the cover off. The board containing the Option 4 circuitry will be visible with the cover removed. This board, (220-204) also contains the circuitry for Options 1 and 3 when they are included in the unit. Positioning the module with the Dataway contact fingers to the left, the Option 4 circuitry is at the right hand side of board 220-204. Referring to drawing 220-B-602, the following components may be identified:

A. Mode switch assemblies, S2, S4, S5, and S6.
B. Matrix switches, S1 and S3.
C. Strap sockets, X0 through X7.
D. Strap carrier, J3.
E. Timing components C46, R57, C44, R54. These are for channels 0 and 1 respectively, but are typical and repeated for the other six channels in similar locations with different reference designations.

6.5.2.1 MODE SELECTION

Selection of the desired mode of operation, Pulse, Gate, or Toggle is made via the mode switches. Each channel may be set to operate in any mode independently of the other channels. Referring to drawing 220-B-602 it will be noted that each mode switch assembly contains four (4) switches, 2 for each channel. These two switches are referred to as the "A" switch and the "B" switch. The table below shows the proper setting of the two switches for each mode of operation.

MODE	A	B
PULSE	ON	ON
GATE	ON	OFF
TOGGLE	OFF	ON

6.5.2.2. MATRIX SWITCH SELECTION

The two matrix switches are configured as an 8 x 10 matrix, having ten inputs and eight outputs. Inputs are arranged vertically on the switch and numbered "1" through "10" (10 is actually labeled "0"). The odd numbers are shown on the left side of the switch body and the even numbers on the right, however each input is common to all eight switch sections. Each of the eight sliders are connected to a switch output and can be set to connect to any input. The sliders can be set by inserting a small pointed tool in the center of the red area and moving the slider to the desired position so that the center of the red area lines up with the position indicator marks on the switch body. The following table shows the switch

labels and the inputs to which they are connected.

SWITCH LABEL	INPUT
1	Channel 0
2	Channel 1
3	Channel 2
4	Channel 3
5	Channel 4
6	Channel 5
7	Channel 6
8	Channel 7
9	Common Start
0	Off

As shown on drawing 220-B-602 slider outputs are used in pairs, one "SET" and one "RESET" for each output channel. The top matrix switch (S1) is used for channels 0 through 3, and the bottom switch (S3) for channels 4 through 7.

When operating in pulse or toggle modes only the "SET" sliders are used; the "RESET" sliders should be set to the "OFF" position. Position the "SET" slider to the desired input. The output will appear at the front panel output connector corresponding to the slider used.

When operating in the gate mode, position the "SET" slider to the input desired to start the gate, and the "RESET" slider to the input desired to terminate the gate. The gate output will appear at the front panel output connector corresponding to the pair of sliders used.

6.5.2.3 WIDE PULSE OPERATION

This is effective in the pulse mode only, therefore that mode should be selected by the mode switch for the particular channel (s) being set up. Pulse mode operation, whether normal (100 ns) or wide pulse, uses a mono to generate the output pulse. Each mono has a resistor and capacitor associated with it which sets the normal(100ns) pulse width. For wider pulse operation, a second capacitor is connected in parallel with the normal one to create a wider pulse. To allow easy restoration of the normal pulse, a jumper strap in a socket is used to complete or break the parallel connection. As shipped from the factory the second capacitor is installed in each channel, but the jumper must be implemented by the user. Thus, as shipped, normal pulse width outputs are generated. The second capacitor (factory installed) will provide pulse width of approximately 1 μs.

The following procedure for generating wider output pulses will be described for channel 0. Use the same procedure for other channels substituting corresponding components as appropriate.

To activate the wider output pulse as installed by the factory, proceed as follows:

A. Locate jumper socket, XO
B. Locate strap carrier, J3
C. Remove one small wire jumper from the carrier and install it in XO.

NOTE: J3 is simply a socket provided to hold eight jumper wires when not in use and serves no other function.

A 1 μs wide pulse should appear at the front panel channel 0 output connector. If a different pulse width output is desired, it is necessary to change capacitor C46 (for channel 0) to an appropriate value. C46 is mounted on a pair of standoffs so that it can be easily changed from the top of the board. The value of the required capacitor can be calculated from the following equation:

$$Tw\ (out) \approx 0.7\ RC$$

where:

Tw (out)	=	output pulse width in ns
R	=	value of R57 in Kohms = 12K
C	=	value of C46 in pf

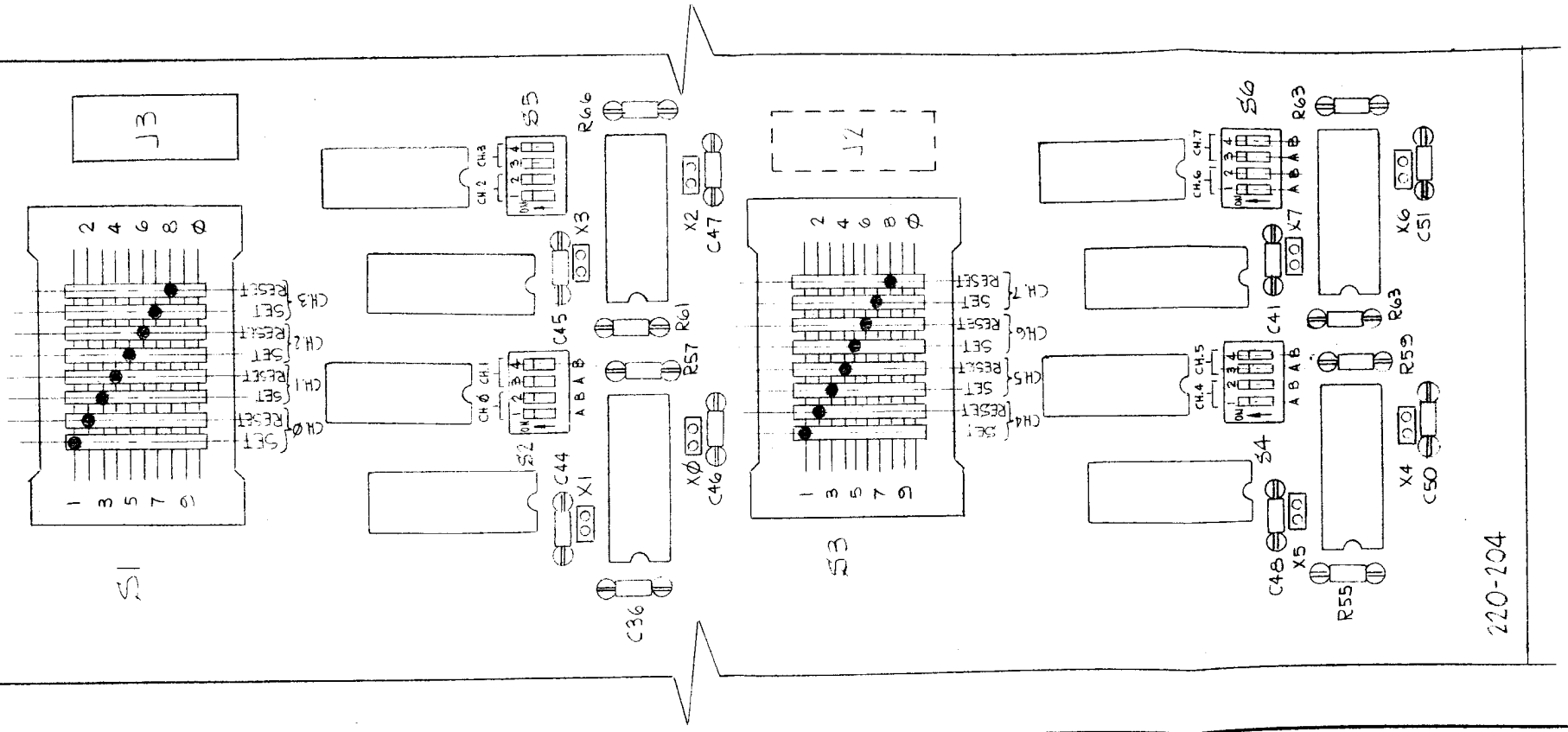
Actually, C46 is in parallel with the normal pulse width capacitor. This can usually be ignored for pulses less than 1 μs. The normal capacitor is 10 pf (plus an additional approximately 5 pf stray capacitance) and has negligable effect except where narrow pulses are to be generated.

Although a sufficient range of pulse widths can be obtained by changing C46, R57 may also be changed and it too is mounted on standoffs for this purpose. It should be noted, however, that changing the value of R57 affects the normal output pulse width. R57 should not be made smaller than 2K nor larger than 100K.

6.5.1.4 COMMON CLEAR

The Common Clear function, either front panel (manual or electrical), or via Camac command has the effect of setting any output signal to the logic 0 state. A pulse which has been triggered, but not yet completed, will be terminated at the time the Clear is applied. When operating in the Gate or Toggle mode the output will be randomly set to either state after power is applied to the module. Therefore, a Clear function should be executed after module power up to assure proper initial conditions before operation is commenced. A clear may also be generated at any time during normal operation, and will override all other factors, returning the output to the logic 0 state.

REVISIONS			
REV	DESCRIPTION	DATE	APPR. BY
A	REVISED PER E.C. NO. 362	1/26/81	Roy Hamm



NOTES:
1. SETTING FOR MATRIX SWITCH IS SHOWN FOR STANDARD OPERATION.

JORWAY CORPORATION

SCALE 2:1	APPROVED BY:	DRAWN BY Roy Hamm
DATE 12/18/80		REVISED

MODEL 220A, OPTION 4 COMPONENT IDENTIFICATION

DRAWING NUMBER 220-B-60

APPENDIX 1

TABLE A1-1 CONTACT ALLOCATION AT A NORMAL STATION

(Viewed from front of crate)

Bus-line	Free Bus-line	P1	B	Busy	Bus-line
Bus-line	Free Bus-line	P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual line	Station Number	N	A2	Sub-address	Bus-line
Individual line	Look-at-Me	L	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialise	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
24 Write Bus-lines		W16	W15		
		W14	W13		
W1 = least significant bit		W12	W11		
W24 = most significant bit		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
24 Read Bus-lines		R16	R15		
		R14	R13		
R1 = least significant bit		R12	R11		
R24 = most significant bit		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
	-12V d.c.	-12	-24	-24V d.c.	
	+200V d.c.	+200	-6	-6V d.c.	
Power	117V a.c. Live	ACL	ACN	117V a.c. Neutral	Power
Bus-lines	Reserved	Y1	E	Clean Earth	Bus-lines
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	0V (Power Return)	0	0	0V (Power Return)	

TABLE A1-2 CONTACT ALLOCATION AT THE CONTROL STATION

(Viewed from front of crate)

Individual patch contact		P1	B	Busy	Bus-line
Individual patch contact		P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual patch contact		P6	A2	Sub-address	Bus-line
Individual patch contact		P7	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialise	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
24 individual Look-at-Me lines		L13	N13	*24 individual Station Number lines*	
L1 from Station 1, etc.		L12	N12	N1 to Station 1, etc.	
		L11	N11		
		L10	N10		
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
	-12V d.c.	-12	-24	-24V d.c.	
	+200V d.c.	+200	-6	-6V d.c.	
Power	117V a.c. Live	ACL	ACN	117V a.c. Neutral	Power
Bus-lines	Reserved	Y1	E	Clean Earth	Bus-lines
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	0V (Power Return)	0	0	0V (Power Return)	