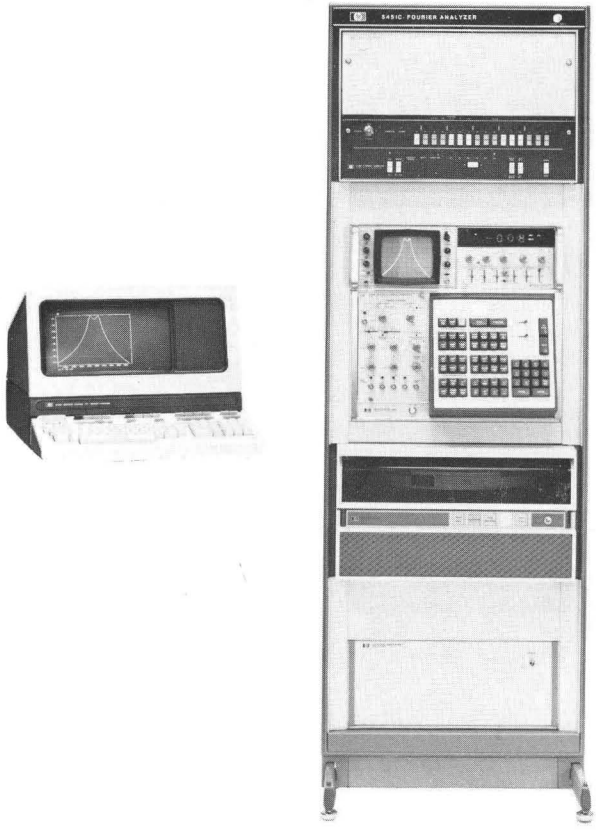
SYSTEM SERVICE MANUAL

FOURIER ANALYZER SYSTEM

5451C



MANUAL PART NO. 05451-90565
MICROFICHE PART NO. 05451-90566

Printed in U.S.A.

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its option, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

FOURIER ANALYZER SYSTEM

5451C

Software Date Code
2112A — 5475A
2112A — 5460A

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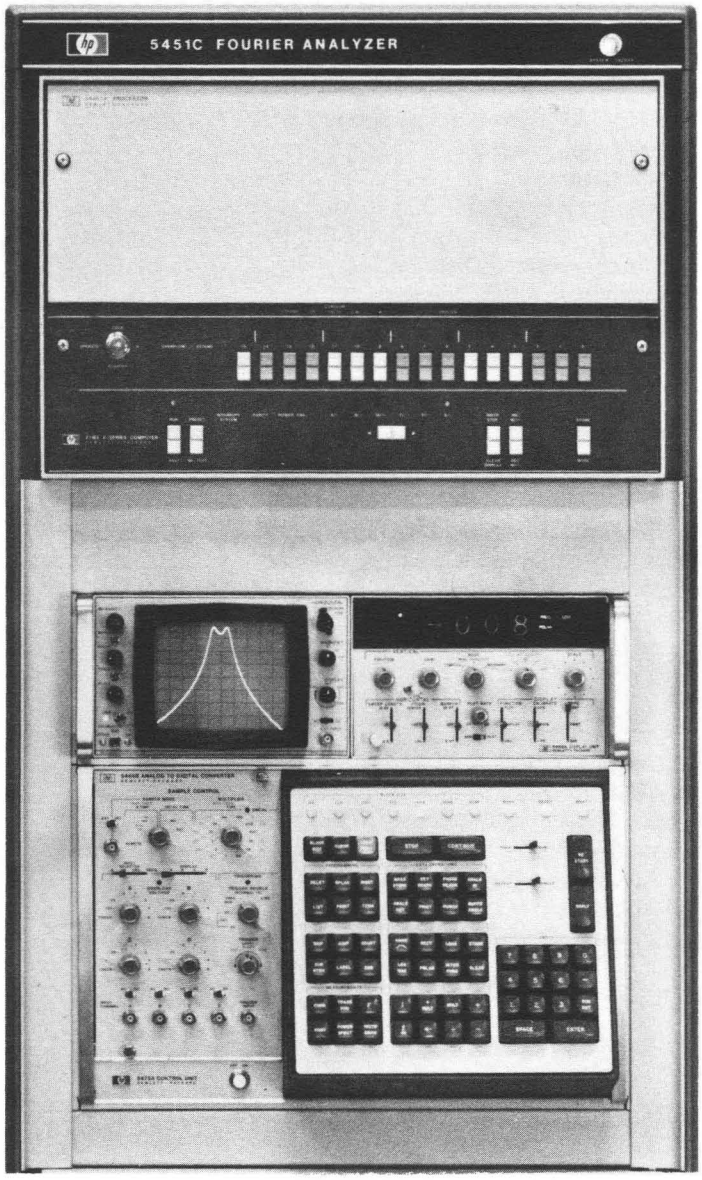
Figure 1-1. Model 5451C Fourier Analyzer System



SECTION 1
GENERAL INFORMATION

INTRODUCTION

This manual provides service information for the HP 5451C Fourier Analyzer System. It includes operating considerations, operating checkout procedures, circuit card adjustments, and troubleshooting information to the circuit card level. For applicable documents such as the system operating manual, unit hardware manuals, processor manuals and peripheral equipment instruction manuals, refer to the System Configuration Notice supplied with the system.

SYSTEM DESCRIPTION

The HP 5451C Fourier Analyzer System (Figure 1-1) performs analyses of time and frequency data containing frequencies from dc to 50 kHz. The system uses a processor for processing and storage of input data. The analyzer can take on a variety of configurations made up from a list of customer-selected add-on options.

ENVIRONMENTAL FACTORS

Environmental Limitations:

Without HP 7906A Disc Drive:

Ambient Temperature —
Operating: 0° to 40°C (32° to 104°F)
Non-operating: -40° to 75°C (-40° to 167°F)

Altitude —
Operating: 4572 metres (1,500 feet)
Non-operating: 12,192 metres (40,000 feet)

Relative Humidity —
25% to 95% at 25° to 40°C (77° to 104°F) without condensation
8% to 80% with maximum wet bulb temperature not to exceed 25.6°C (78°F), non-condensing 5% to 95%

With HP 7906A Disc Drive:

Ambient Temperature —
Operating: 10° to 40°C (54° to 104°F)
Non-operating: -40° to 65°C (-40° to 149°F)

Altitude —
Operating: 4572 metres (15,000 feet)
Non-operating: 12,192 metres (40,000 feet)

Relative Humidity —
25% to 95% at 25° to 40°C (77° to 104°F) without condensation
8% to 80% with maximum wet bulb temperature not to exceed 25.6°C (78°F), non-condensing 5% to 95%

Power Requirements

UNITS	WATTS	BTU/HR.	CURRENT @ 115V	CURRENT @ 230V
5475A/5466B	365	1245	3.2A	1.6A
H51-180DR/5460A	200	683	2.0A	1.0A
7900A*	500	1700	4.1A	2.0A
54451A/B	840	2876	7.3A	3.7A
7906A	520	1776	5.5A	2.8A

**Optional disc drive systems. Only one used.*

Dimensions (when rack mounted) —
Height: 1632 mm (64-1/4 inches)
Width: 533 mm (21 inches)

BASIC FOURIER ANALYZER SYSTEM AND REQUIRED OPTIONS

The specific units and required options to make up a minimum functional Fourier Analyzer System (5451C) are listed in Table 1-1. Additional information on available options can be obtained from any HP Sales or Service Office. Because of the wide variety of possible configuratons, a System Configuration Notice is shipped with each system. The System Configuration Notice defines the equipment supplied, and the options and software included in each system. To perform the service and diagnostic routines described herein, the following minimum equipment is required:

5451C Basic Units (see Table 1-1)
2648A Display Terminal
54451A/B Processor

INSTRUMENT IDENTIFICATION

MODEL NUMBER AND NAME

Each unit in the standard Fourier Analyzer System is identified by model or specification number and name as a separate instrument; for example:

Specification H51-180DR Oscilloscope
Model 54451A/B Processor
Model 2648A Display Terminal
Model 5460A Display Plug-in Unit
Model 5466B ADC Plug-in Unit
Model 5475A Control Unit

Table 1-1. 5451C Fourier Analyzer System Components

Description	HP Part Number	Quantity
BASIC UNITS		
Display Plug-in Unit	Model 5460A	1
Analog-to-Digital Converter (ADC) Plug-in 2-channel, 12-bit, 100 kHz max sample rate 4-channel, 12-bit, 100 kHz max sample rate	Model 5466B standard 5466B Opt. 001 (5451C Opt. 046)	1
Control Unit (Keyboard and Power Supply)	Model 5475A	1
Display Mainframe	Model H51-180DR	1
Microcircuit Interface Card Kit or Data/Control Interface Card	05451-60025	3
Processor (48K DMS, Memory Protect, DCPC, Fourier and ROMs and Fourier booster assy.)	Model 54451A	1
Cable Assembly (Keyboard-to-Processor)	05451-60026	1
Cable Assembly (Display Unit-to-Processor & Keyboard)	05450-60002	1
Cable Assembly (ADC-to-Processor)	05451-60069	1
Cable Assembly (Control Unit-to-Computer)	05451-60011	1
Cable Assembly (Display Terminal-to-Control Unit)	05451-60030	2
Display Terminal and I/O Card	Model 2648A and 12880A	1
Disc Drive	7900A or 7906A	1
Cabinet	29402B	1

Table 1-1. 5451C Fourier Analyzer System Components

Description	HP Part No.	Quantity
EXTENDED CAPABILITY OPTIONS		
64K Memory		1
Variable Persistence Oscilloscope	Model H51-181AR	1
Thermal Printer	Model 9866A	1
Digital Plotter	HP-IB Selectable Printer	1
Magnetic Tape Unit	Model 7970B or 7970E	1
Digital-to-Analog Converter	54420A	1
Filter	54440A	As Required
Pre-Processor	54470A	1
Universal Counter	5326A and 12604B Interface	1
Module Mainframe	5440B	As Required
System Control for Applications Package	5477A	1

SERIAL NUMBERS

Each Fourier Analyzer System is identified by a two-section system serial number (5451C-000). The number is found on a stick-on plate mounted on the inside rear of the system cabinet. The three-digit number is a serial number unique to each system, and the other portion provides the system model number.

Each unit including the processor and its peripherals, in the Fourier Analyzer System is identified by a two-section serial number on the rear panel of the unit. The serial number consists of nine digits and an alpha character (0000A00000). The four-digit prefix portion is used to document changes. The alpha character denotes the country of origin; i.e., A = U.S.A., E = England, G = West Germany, J = Japan, and U = United Kingdom. The five-digit suffix of the serial number is unique to each instrument. Include complete serial number, model number and instrument name in correspondence about any unit in your Fourier Analyzer System.

CATHODE RAY TUBE WARRANTY

The Cathode Ray Tube (CRT) is covered by a warranty separate from the rest of the system. The CRT warranty and warranty claim form are located in the H51-180DR Oscilloscope manual. Should the CRT fail within the time specified on the warranty, return the CRT with the warranty form completed.

STORAGE AND SHIPMENT

PACKAGING

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Your Hewlett-Packard Sales and Service Office can provide packing material such as that used for original factory packaging. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

ENVIRONMENT

Conditions during storage and shipment should normally be limited as follows:

1. Maximum altitude: 25,000 ft.
2. Maximum temperature: +167°F (+75°C).
3. Minimum temperature: -40°F (-40°C).

SYSTEM INTERCONNECTION

Figures 1-2 and 1-3 show system interconnections and cable locations for the Fourier Analyzer System.

MICROCIRCUIT CARD STRAPPING

The Processor Subsystem uses Interface Cards, in the Processor's I/O slots, to interface the ADC, Display, and Keyboard units. These cards, and the required jumper or switch settings on them, are listed in Table 1-2 below.

Table 1-2. 5451C Interface Jumpers and Strapping

Unit Interfaced	05451-60025 Data/Control Interface Setup	Unit Interfaced	05451-60025 Data/Control Interface Setup
ADC (data channel) 2 or 4 channel (NOTE: when using 05451-60068 ADC Interface, set board jumper to 51C position.)	W1 to C W2 to B W3 to B W4 to B W5 thru W8 removed W9 to A W10 to B W11 to A W12 and W13 removed	5477A System	W1 to A W2 to B W3 to B W4 to B W5 thru W8 installed W9 to A W10 to A W11 to A W12 and W13 removed
Display and Keyboard	W1 to C W2 to C W3 to B W4 to B W5 thru W8 removed W9 to A W10 to A W11 to A W12 and W13 removed	9866A Line Printer	W1 to A W2 to B W3 to A W4 to B W5 thru W8 removed W9 to A W10 to A W11 to A W12 and W13 removed
5440A/B Plug-In Module Channel	W1 to C W2 to B W3 to B W4 to B W5 thru W8 installed W9 to A W10 to pin D of W1 W11 to A W12 installed W13 removed	7210 Plotter	W1 to A W2 to A W3 to B W4 to B W5 thru W8 installed W9 to B W10 to A W11 to A W12 and W13 removed
		Terminal	12531 Jumpers W1 = B W2 thru W6 = OUT W7 = A

SERVICE AIDS

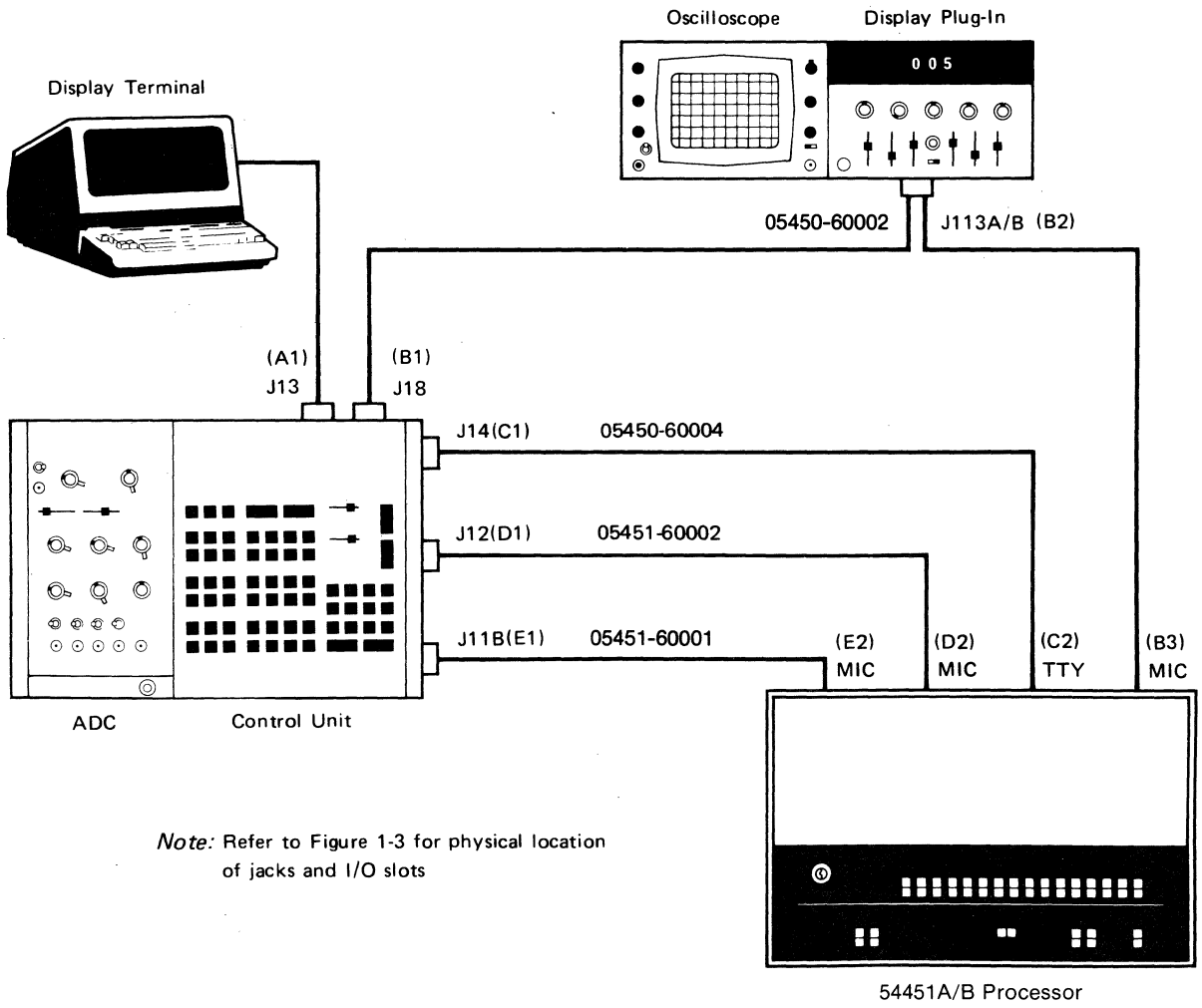
EXTENDERS, REPLACEMENT BOARDS, AND RECOMMENDED SPARE COMPONENTS

Table 1-3 lists extenders and the most often-needed replaceable boards and parts for the following units:

5460A Display Unit
5466B ADC Unit
5475A Control Unit

For circuit card schematics and parts lists, refer to the applicable unit service manual.

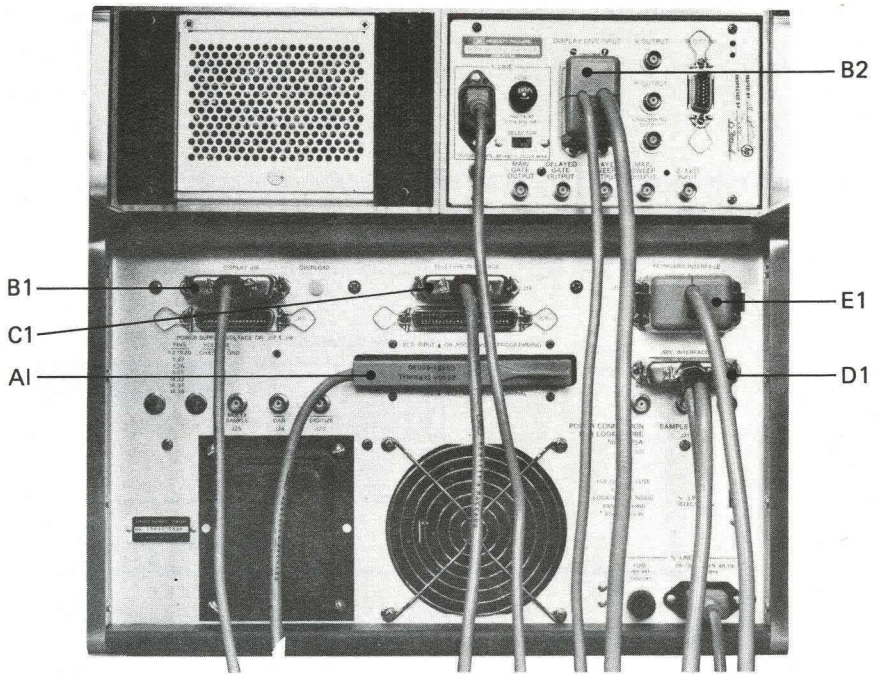
Figure 1-2. System Interconnection Diagram



Note: Refer to Figure 1-3 for physical location of jacks and I/O slots

Label	Cable	Connection
A1	Display Terminal	Control Unit J13 to Display Terminal
B1, B2, B3	05450-60002	Control Unit J18 to Display Plug-in J112A/B to Processor MIC I/O Slot
C1, C2	05450-60004	Control Unit J14 to Processor Terminal I/O Slot
D1, D2	05451-60002	Control Unit J12 to Processor MIC I/O Slot
E1, E2	05451-60001	Control Unit J11B to Processor MIC I/O Slot

Figure 1-3. System Cable Locations



REFER TO OPPOSITE PAGE FOR CABLE LABEL TABLE

TYPICAL CONFIGURATION

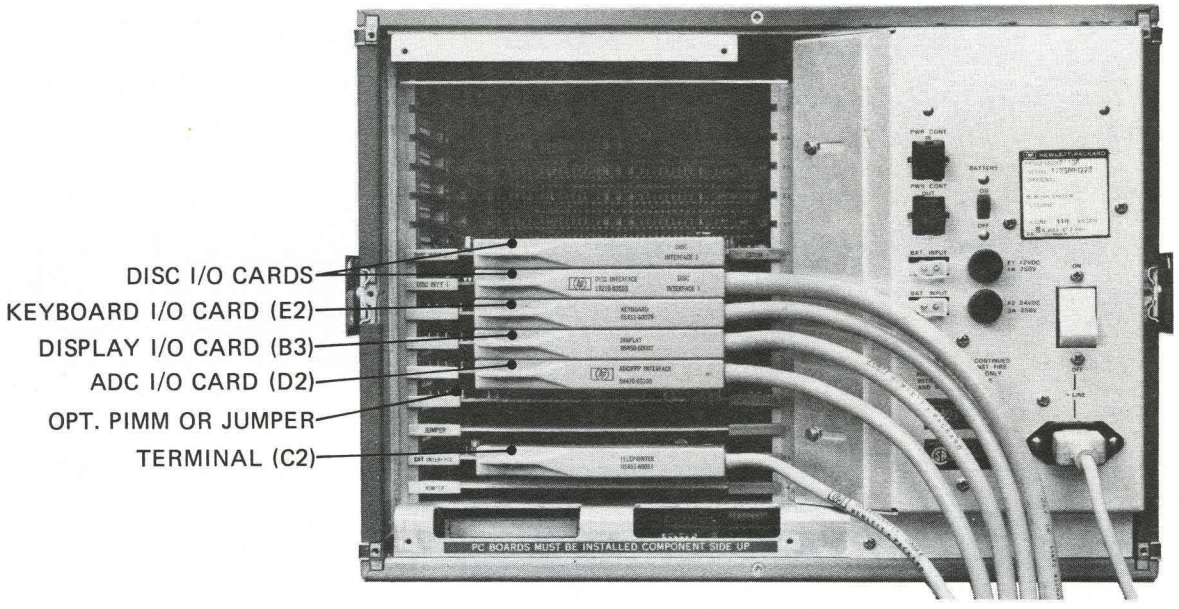


Table 1-3. Extenders, Replacement Boards, and Recommended Spare Components

GENERAL

A spare parts supply should include the items listed below. These are ordered separately by using the HP Part or Assembly Numbers shown.

EXTENDERS

HP ASSEMBLY NUMBER

Display Plug-in Extender Unit 05451-60071
Enables 5460A to be operated outside H51-180AR plug-in compartment

Extender Cards ..... 5060-0049(2)
..... 5060-0630(1)

ADC Extender Cable. Enables 5466 to be operated outside 5475A plug-in compartment 10628A

REPLACEMENT BOARDS

The HP Part Number column gives a cross reference between new and rebuilt board part numbers. (Refer to board exchange paragraph)

For 5460A Display Unit

Reference Designator	Description	HP Part Number
A1	Board Assembly: Vertical Amplifier	05460-60001 (new); 05460-60013 (rebuilt)
A2, A3	Board Assembly: DAC (Digital-to-Analog Converter)	05460-60002 (new); 05460-60014 (rebuilt)
A4	Board Assembly: Word Storage	05460-60003 (new); 05460-60015 (rebuilt)
A5	Board Assembly: Control	05460-60004 (new); 05460-60016 (rebuilt)
A6	Board Assembly: Reference Power Supply	05460-60005 (new); 05460-60017 (rebuilt)
A7	Board Assembly: Plot Control	05460-60020 (new); 05460-60520 (rebuilt)
A8	Board Assembly: Nixie® Display	05460-60006 (new); 05460-60018 (rebuilt)
A9	Board Assembly: Light Driver	05460-60007 (new); 05460-60019 (rebuilt)

Table 1-3. Extenders, Replacement Boards, and Recommended Spare Components (continued)

For 5466B ADC Unit

Reference Designator	Description	HP Part Number
A1, A2	Board Assembly: Input	Ø5466-6ØØ13 (new); Ø5466-6Ø513 (rebuilt)
A3, A4, A5, A6	Board Assembly: Digitizer, 12-bit, 1ØØ kHz	Ø5466-6ØØ14 (new); Ø5466-6Ø514 (rebuilt)
A3, A4, A5, A6	Board Assembly: Digitizer, 1Ø-bit, 2ØØ kHz	Ø5466-6ØØØ2 (new); Ø5466-6Ø5Ø2 (rebuilt)
A3, A4, A5, A6	Board Assembly: Digitizer, 12-bit, 2ØØ kHz	Ø5466-6ØØØ7 (new); Ø5466-6Ø5Ø7 (rebuilt)
A7	Board Assembly: Error	Ø5466-6ØØ15 (new)
A8	Board Assembly: Trigger	Ø5466-6ØØØ4 (new); Ø5466-6Ø5Ø4 (rebuilt)
A9	Board Assembly: Control	Ø5466-6ØØ16 (new)
AlØ	Board Assembly: Sample Generator	Ø5466-6ØØØ6 (new); Ø5466-6Ø5Ø6 (rebuilt)

For 5475A Control Unit

Reference Designator	Description	HP Part Number
A2	Board Assembly: Reference	Ø558Ø-6ØØ2 (new)
A4, A5, A6	Board Assembly: Regulator	Ø558Ø-6ØØ4 (new)
A12	Board Assembly: Matrix A	Ø5475-6ØØ45 (new); Ø5475-6Ø545 (rebuilt)
A13	Board Assembly: Matrix B	Ø5475-6ØØ46 (new); Ø5475-6Ø546 (rebuilt)
A14	Board Assembly: Shift Register	Ø5475-6Ø2Ø4 (new)
A15	Board Assembly: Function	Ø5475-6ØØ12 (new)
A16	Board Assembly: Switch Register	Ø5475-6ØØ41 (new)
A17	Board Assembly: Buffer	Ø5475-6Ø199 (new)

For 54451A Processor

Reference Designator	Description	HP Part Number
	Fourier Booster Board	54427-6ØØ5Ø (new); 54427-6Ø55Ø (rebuilt)
	ROMS (12)	1816-1Ø76 thru 1816-1Ø87 (Order Ø5427-6ØØ17 for all 12 ROMS)
	ADC I/O Board	05451-60068
	KYBD/DISPLY I/O Board	05451-60025

Table 1-3. Extenders, Replacement Boards, and Recommended Spare Components (continued)

RECOMMENDED SPARE COMPONENTS

RESISTORS

Part Number	*Quantity*
0811-0233	1
0811-0436	1
0811-1397	1
0811-1398	1
0811-1517	1
0960-0025	1
0960-0049	1

SUBASSEMBLIES

Part Number	*Quantity*
1813-0009 Sample/Track-and-hold	1
1813-0010 Digitizer, 12-bit, 200 kHz	1[1]
1813-0011 Digitizer, 10-bit, 200 kHz	1[2]

TRANSISTORS

Part Number	*Quantity*
1850-0099	1
1853-0012	1
1853-0015	1
1853-0020	4
1853-0027	1
1853-0034	1
1853-0036	2
1853-0051	1
1853-0052	1
1853-0073	1
1853-0088	2
1854-0003	2
1854-0005	1
1854-0019	2
1854-0020	1
1854-0022	1
1854-0039	2
1854-0063	1
1854-0072	1
1854-0092	2
1854-0092	2
1854-0094	2
1854-0215	2
1854-0300	1
1854-0313	1
1854-0326	2
1855-0010	1
1855-0020	2
1855-0049	1
1855-0051	1

RESISTOR ARRAY

Part Number	*Quantity*
1810-0041	1

INTEGRATED CIRCUITS

Part Number	*Quantity*
1820-0054	4
1820-0055	2
1820-0056	1
1820-0068	2
1820-0069	1
1820-0070	2
1820-0071	2
1820-0072	1
1820-0077	4
1820-0084	1
1820-0092	1
1820-0099	1
1820-0116	1
1820-0142	1
1820-0174	2
1820-0201	1
1820-0207	1
1820-0261	1
1820-0262	1
1820-0269	1
1820-0282	1
1820-0327	2
1820-0328	1
1820-0370	1
1820-0437	1
1820-0476	1
1820-0495	1
1820-1537	1
1820-0537	1
1820-0538	1
1820-0539	1
1820-0574	1
1820-0620	1
1820-0596	1
1820-0620	1
1820-0738	1
1820-0743	1
1820-0744	1
1820-0846	1
1820-0899	1
1826-0081	1
1826-0105	1
1826-0106	1
1826-0108	1

1. For 5466B Options 004, 005
2. For 5466B Options 002, 003

Table 1-3. Extenders, Replacement Boards, and Recommended Spare Components (continued)

RECOMMENDED SPARE COMPONENTS

SCR

Part Number	*Quantity*
1884-0063	1

DIODES

Part Number	*Quantity*
1901-0028	2
1901-0033	1
1901-0040	1
1901-0041	2
1901-0044	1
1901-0047	1
1901-0056	1
1901-0156	1
1901-0179	1
1901-0415	2
1901-0416	1
1902-0025	1
1902-0041	1
1902-0049	1
1902-0071	1
1902-0244	1
1902-0556	1
1902-3002	1
1902-3024	1
1902-3104	1
1902-3182	1
1902-3193	1
1902-3234	1
1902-3268	1
1902-3279	1

DIGITAL DISPLAY TUBES

Part Number	*Quantity*
1970-0009	1
1970-0012	1
1990-0687	1

LAMPS

Part Number	*Quantity*
1450-0494	1
1450-0745	2
2140-0213	1
2140-0300	1
2140-0244	1

FUSES

Part Number	*Quantity*
2110-0006	1
2110-0010	1
2110-0014	1
2110-0436	1

SWITCHES

Part Number	*Quantity*
3101-1238	2

LED ASSEMBLY

Part Number	*Quantity*
03320-68101	1

BOARD EXCHANGE

Hewlett-Packard provides exchange printed circuit boards for many of the Fourier Analyzer system units.

The board exchange program may be used either to replenish boards used from a spare board supply or as a replacement for a known inoperative board in the Fourier Analyzer System. Rebuilt exchange boards are available at a cost reduced from that of a new board. The price of the board is dependent upon return of the defective board to Hewlett-Packard.

The procedure for exchanging boards is as follows:

1. Repair Fourier Analyzer with a replacement board from a spare board supply. Tag the bad board with a description of trouble caused in system.

2. Order rebuilt board from your nearest Hewlett-Packard Sales and Service Office.

3. When replacement board ordered arrives, place it in the spare board supply. Save the box the board came in for return shipment of the faulty board.

4. The box in which you received your replacement board will also contain an address label to be used for returning the faulty board to the Central Repair Facility, a Module Repair Report to provide failure information, and a piece of tape to seal the box. Place the faulty board in the box, along with the completed Module Repair Report, and seal the box with the piece of tape provided. Stick the address label on the box and send the board to the Central Repair Facility.

ACCESS

The following paragraphs discuss the accessibility for repair and adjustments of the units that make up the 5451C Fourier Analyzer (see Figure 1-4). The discussion assumes cabinet mounting of the system. Always remove power before removing or replacing any system unit or circuit board.

PLUG-INS

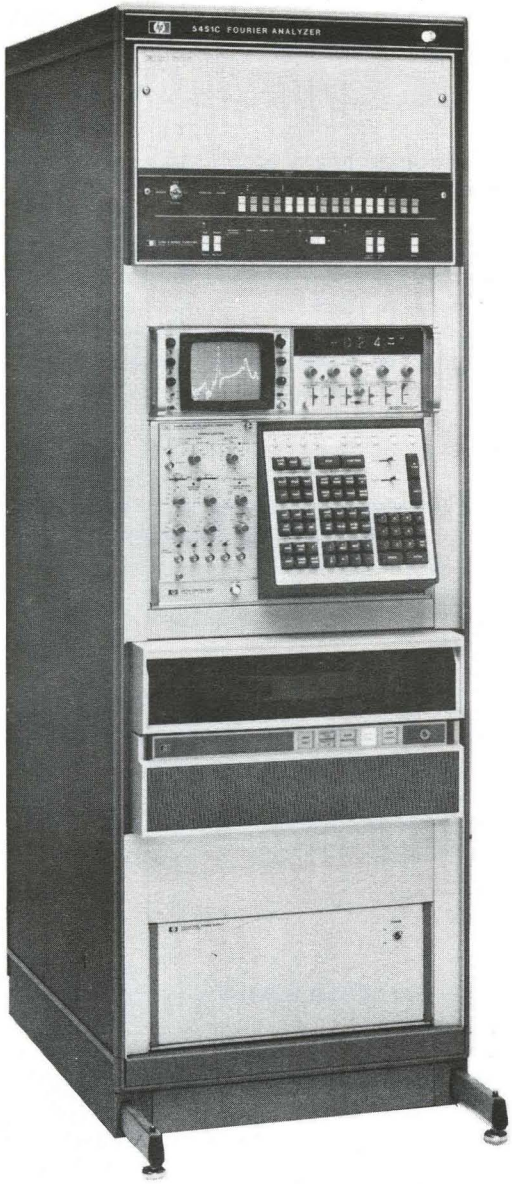
The Fourier Analyzer system contains two plug-ins: the 5460A Display and the 5466B ADC. One plug-in is mounted in the H51-180 Oscilloscope Mainframe; the other is in the 5475A Control Unit Mainframe. To remove either plug-in, turn off power and loosen the one or two knurled mounting screws that connect through to the mainframe unit. Pull out gently on the screw(s) for initial separation of the plug-in from the mainframe unit connector. Now grasp the plug-in at one or more convenient points and pull out from the mainframe unit. To replace a plug-in, reverse the above procedure.

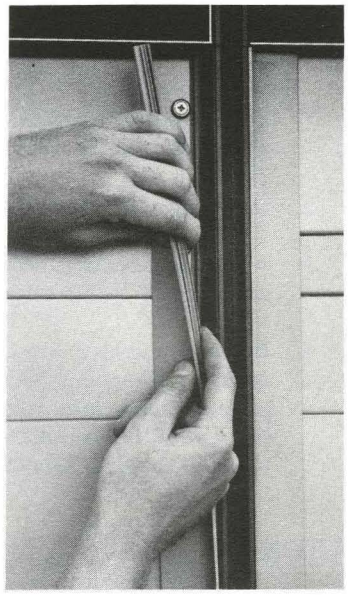
REAR DOOR

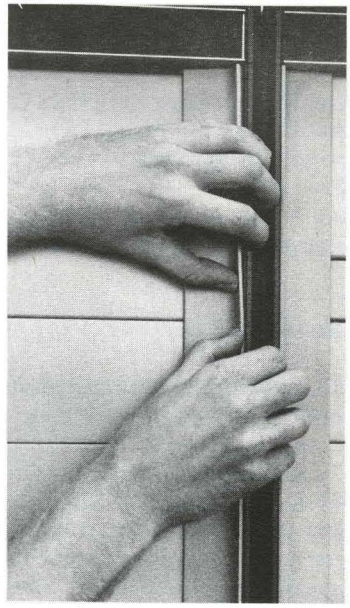
To prevent unauthorized access to connections at rear of system, the cabinet is fitted with a lockable rear door; two keys for the door are provided.

To remove door, pull down on handle of "L"-shaped upper hinge pin and separate upper hinged corner of door from cabinet. The door can be lifted out of its lower mounting bracket. To install the door, reverse the above procedure. The cabinet design allows the door to be mounted as either a right-hand-opening or left-hand-opening door. To reverse door mounting, remove door (as described above), move latching bracket to other side of cabinet rear, and install door so it opens as desired.

Figure 1-4. Access Information







REMOVING AN INSTRUMENT

To remove one of the rack-mounted units from the cabinet, proceed as follows:

1. Turn off system power.

2. Disconnect all cables from rear of the instrument to be removed.

3. Remove plastic trim strips at each side of cabinet front (see Figure 1-4). To remove the trim strip, use fingertips, large coin, or some other convenient wedge to pull one end out of cabinet channel in which it is mounted. Then carefully remove strip from the cabinet. Do not make any sharp bend in strip.

4. With both trim strips removed, all mounting screws are accessible. The unit may now be removed from the system and a new unit put in its place.

5. When installing a new unit in the cabinet, first put rack-mounting screws in the bottom holes of the rack-mounting brackets; then proceed upward with remaining screws. After attaching new unit to rack, connect cables as described in Figure 1-2.

6. Complete installation by replacing plastic trim strips removed in Step c. of this procedure. To replace a strip, place one end in the guide channel and press along its entire length. When replacing the trim strip, be sure it is mounted firmly in the channel so it will clear the pullout table.

TOP COVER

The cabinet top cover is held in place by four flathead screws. To remove the cover, remove retaining screws and screw-in eyebolts, if installed.

KEYBOARD REMOVAL

The 5475A Control Unit keyboard may be removed for maintenance (contact cleaning) or replacement.

1. Remove power.

2. Pull 5475A four to six inches forward from its normal rack-mounting position (see Removing an Instrument above).

3. Loosen three screws at top of keyboard unit.

4. Remove three screws at bottom of keyboard unit.

NOTE

Keyboard unit is connected to mainframe by two cables. When separating these two units, be careful to avoid straining cable or damaging connectors.

5. Gently separate keyboard unit from mainframe. Stop when you feel cable pull, reach behind keyboard unit and disconnect the two cables, then continue removing keyboard from mainframe.

   To replace keyboard, perform the above procedure in reverse.

TEST EQUIPMENT

Table 1-4 provides the specifications and recommended test equipment required to maintain the 5460A, 5466B, and 5475A units of the Fourier Analyzer System.

Table 1-4. Test Equipment Specifications

Equipment Type and Critical Specifications	Recommended Instrument	Used For*
AC Voltmeter Voltage Range: 1V to 100V Frequency Range: 10 Hz to 1 MHz	HP Model 5306B	1, 2, 3
DC Voltmeter Voltage Range: 1 to 100V Resolution: .1 mV Accuracy: 0.03 of reading	HP Model 5306B	2
Oscilloscope Frequency Range: dc to 75 MHz Sensitivity Range: 10 mV/div to 5 V/div Sweep Range: .1 μsec/div to 2 sec/div	HP Model 1707B	2, 3
Frequency Counter Frequency Range: dc to 50 MHz Accuracy: ±1 count Sensitivity: 0.1 Vrms Time Base Stability $<\pm 5 \times 10^{7}$, 0° to 50°C	HP Model 5300A, + HP Model 5303B, HP Option 001	1, 2, 3
Function Generator (Sine, Triangle)	HP Model 3311B	1, 2, 3
Precision Power Supply Output Range: 0 to 10V Resolution: 1 mV Accuracy: .025% +1 mV	HP Model 6115A	1, 2, 3
		* 1 = Operational Check 2 = Adjustments 3 = Troubleshooting

SECTION 2
PRINCIPLES OF OPERATION

INTRODUCTION

This section provides theory of operation for the 5451C Fourier Analyzer System. Since specific Fourier Analyzer Systems will reflect individual requirements, the detailed theory of operation of the processor, oscilloscope mainframe,display terminal, disc drive, I/O cards, and any additional peripherals supplied with each system are fully documented in separate manuals. On the other hand, specific unit theory of operation for the 5460A Display Unit plug-in, 5466B A/D Converter plug-in, and 5475A Control Unit are provided in this manual since these units are unique to the Fourier Analyzer Systems.

SYSTEM DESCRIPTION

The 5451C Fourier Analyzer System is used to analyze time-series data, using Fourier Analysis techniques. Analyses of this type may detect signals hidden in noise, or identify critical frequencies in transfer functions. Continuous or transient data may be processed. The system is controlled by software, and by special Fourier microcodes using a processor "booster" board and Ready-only Memory (ROM) devices. The control software is contained in the Fourier System Disc. The system can be operated manually, by pressing 5475A buttons for each operation to be performed; or operation can be automatic, working from a stored keyboard command program "stack". The following functions are standard in the Fourier Analyzer:

Forward and inverse Fourier transform
Power Spectrum
Magnitude and phase spectrum
Auto and cross correlation
Cepstrum
Digital filtering
Convolution
Histogram
Scaling
Hanning and other weighting functions
Ensemble averaging (time and frequency)

Six editing keys on the control unit provide on-line editing so that user written measurement programs can be changed on-line, without the need of off-line compiling or testing.

The Fourier Analyzer is a completely calibrated system. All displays and data outputs are accompanied by a scale factor relating them to physical units. This calibration is the result of using digital techniques in all computations.

The 5475A keyboard contains keys for input/output and basic analysis operations. Additional numeric address keys control data flow into and out of data block, and permit entry of numeric values into memory. All control and data entry operations use decimal numbers for data values and data identification.

Data can also be entered into the Fourier Analyzer as analog signals through the two-channel 5466B, A/D Converter, or as digital or binary information through the Processor input channels.

Data output is available through the oscilloscope, display terminal and other peripheral devices depending on system configuration.

FOURIER ANALYZER SYSTEM OPERATION

The operation of a Fourier Analyzer System (like most computing systems) can be separated into data input, data processing and control, and data output. This description will assume that an analog signal is applied to the 5466B A/D converter, digitized and stored in memory, manipulated under control of the 5475A Control Unit and system software, and displayed on the system oscilloscope. For a complete explanation of all controls and indicators on the 5460A, 5466B, and 5475A refer to the System Operating Manual. Refer to the mnemonic list (Table 2-12) placed at the end of this discussion for an explanation of signal names used in the system.

5466B A/D CONVERTER

The 5466B Fourier ADC produces two's-complement digital representation of sampled analog input signals, and transfers the resultant digital data words to the Processor. The ADC has three basic parts: input amplifiers, track/hold and digitizers, and control and sampling logic. Each of these parts is described in more detail below; a simplified block diagram of the ADC is given in Figure 2-1.

The input amplifier serves to provide sufficient gain so the input signal can drive the analog-to-digital converter; full-scale ADC output (positive or negative) requires plus or minus 10V at the output of the input amplifier. The track/hold and A-to-D converter module sample the analog input signal and convert its level to a digital word. The control and sampling logic serve to trigger the ADC, provide sampling signals to initiate conversions, transfer data words to the Processor, and detect erroneous sampling conditions and data patterns.

The 5466B is available in several different configurations. Some 5466B options, and the equivalent 5451C options, are listed in Table 2-1.

Table 2-1. 5466B and 5451C Options

Description	5466B Option Number	5451C Option Number (See configuration Notice)
2-channels, 12 bits, 100 kHz max sample rate	standard	standard
4-channels, 12 bits, 100 kHz max sample rate	001	046

ADC INTERFACE

Normally, the 5466B is installed in the plug-in compartment in the left-hand side of the 5475A Control Unit. One of the two rear-panel connectors (P15) mates with J15 in the 5475A, providing paths for all data, standard control and power between these units. If one of the application package options is ordered for the 5451C system, the connector to P21 of the 5466B, carries the signals that can be used to control the SAMPLE RATE and OVERLOAD VOLTAGE controls. The remote control signals interface via the optional 5477 System Control. Figure 2-2 presents a simplified diagram of the interface connections.

Figure 2-1. ADC Block Diagram

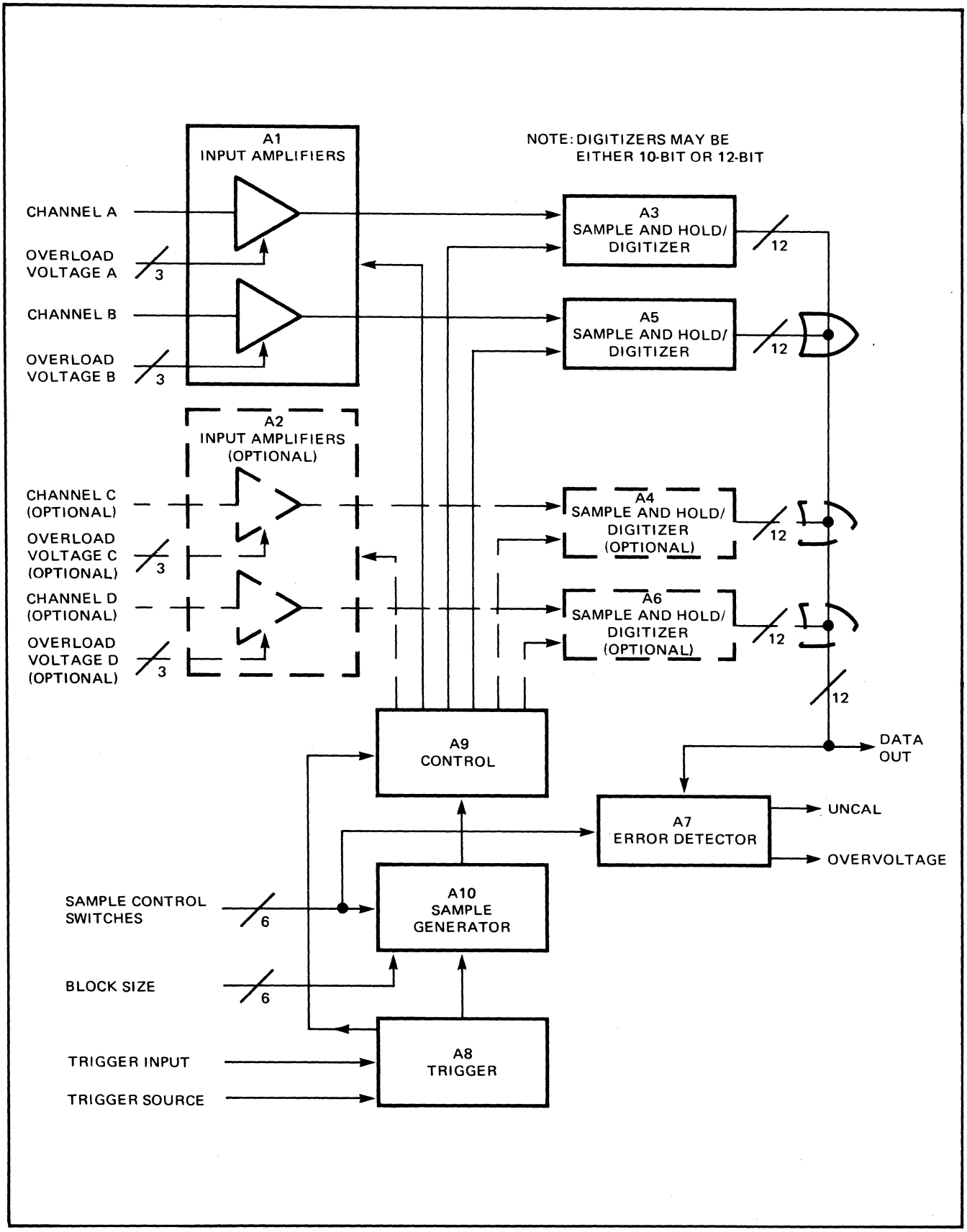
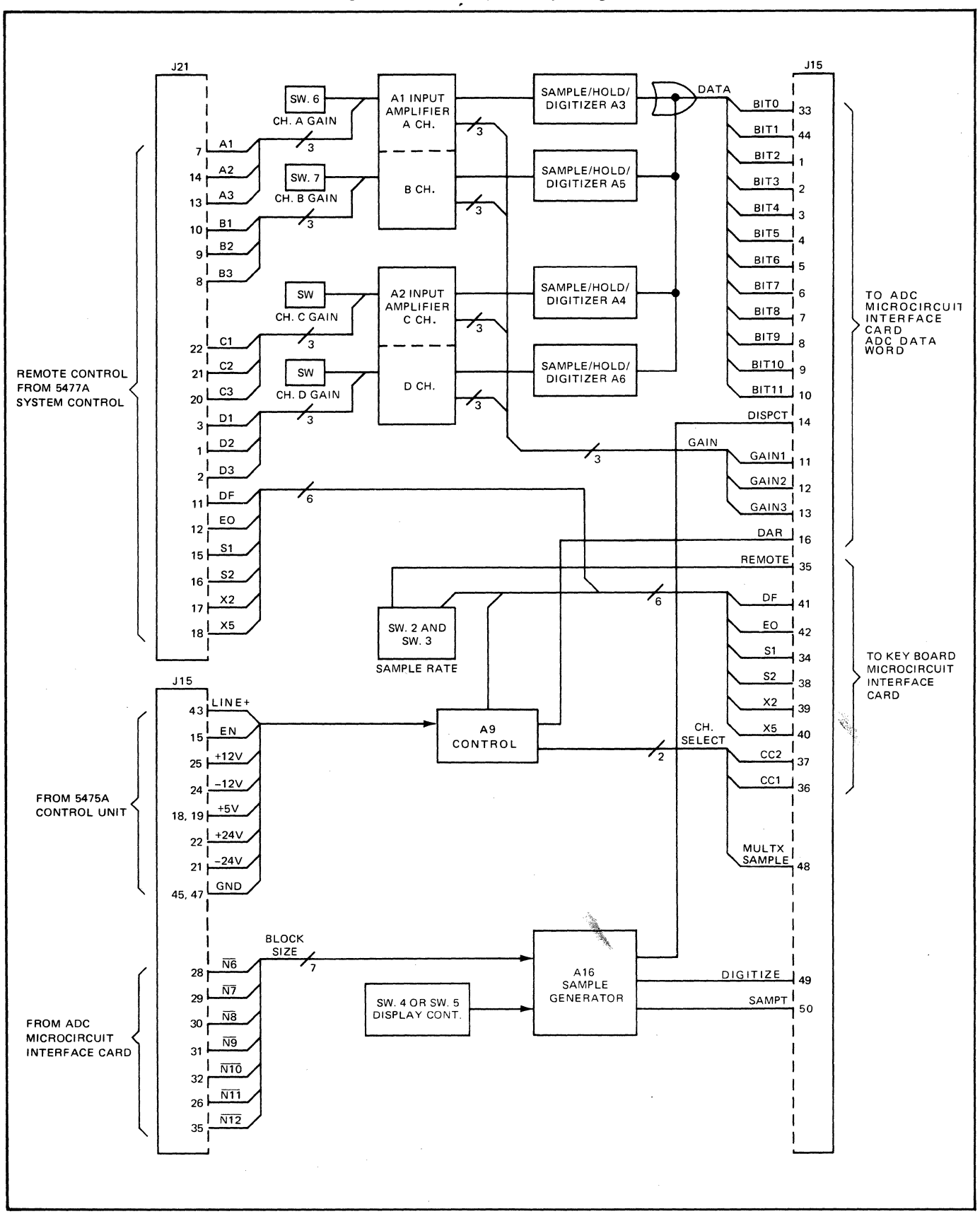


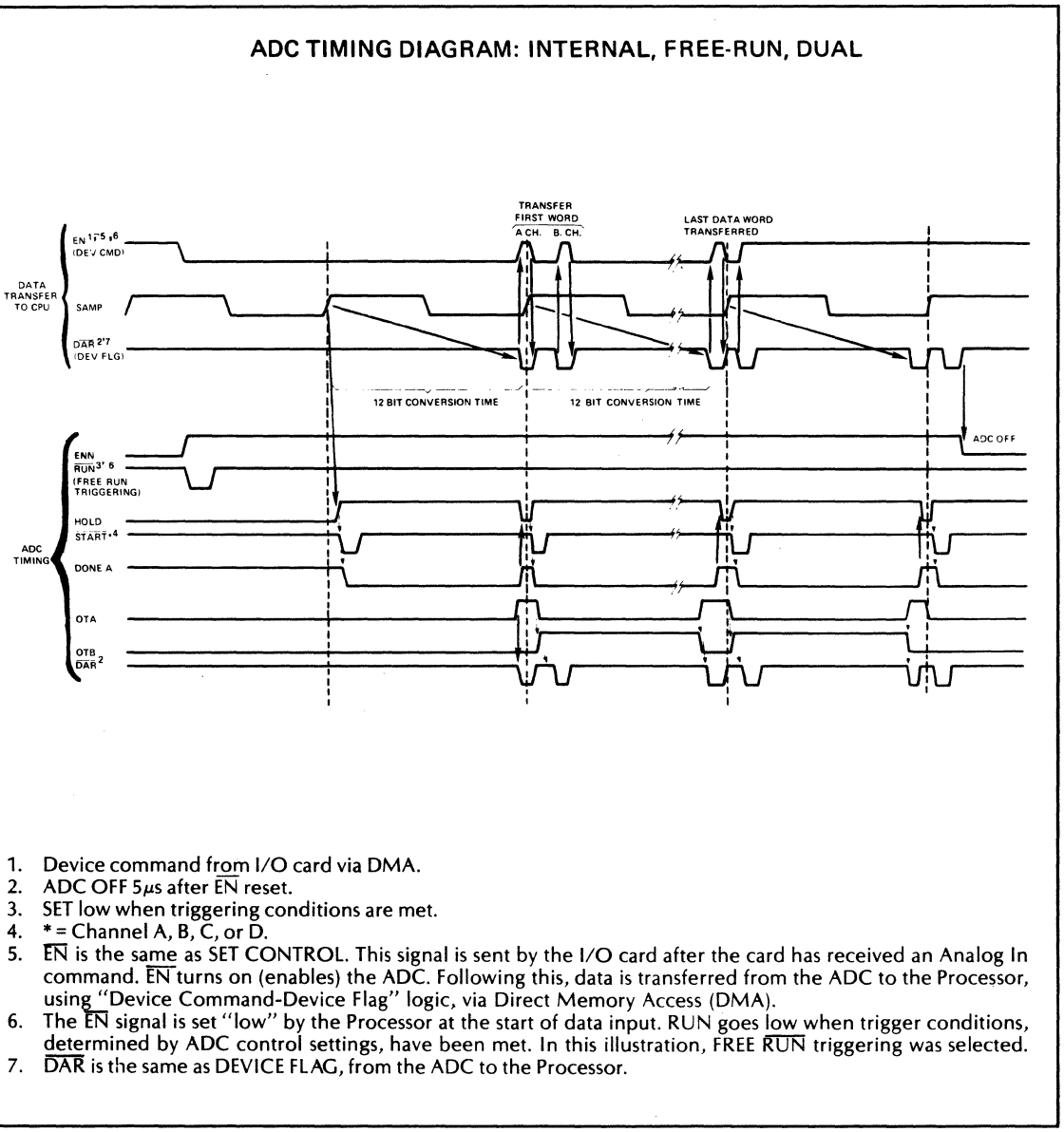
Figure 2-2. ADC Input/Output Signals



ADC DATA TRANSFER SEQUENCE

The basic timing diagram for the 5466B, in two channel operation, is given in Figure 2-3; arrows in the figure indicate causality between signals.

Figure 2-3. ADC Data Transfer Timing



1. Device command from I/O card via DMA.
2. ADC OFF 5μs after $\overline{EN}$ reset.
3. SET low when triggering conditions are met.
4. * = Channel A, B, C, or D.
5. $\overline{EN}$ is the same as SET CONTROL. This signal is sent by the I/O card after the card has received an Analog In command. $\overline{EN}$ turns on (enables) the ADC. Following this, data is transferred from the ADC to the Processor, using "Device Command-Device Flag" logic, via Direct Memory Access (DMA).
6. The $\overline{EN}$ signal is set "low" by the Processor at the start of data input. RUN goes low when trigger conditions, determined by ADC control settings, have been met. In this illustration, FREE $\overline{RUN}$ triggering was selected.
7. $\overline{DAR}$ is the same as DEVICE FLAG, from the ADC to the Processor.

The ADC is activated by the $\overline{EN}$code (or $\overline{EN}$) signal from the Processor going "low". This causes the ADC's internal "off-on" signal, ENN, to be "high". If the ADC (TRIGGER SOURCE switch) is not in FREE RUN mode, the ADC waits for one of the triggering conditions (internal, external, or line) to be satisfied. When this occurs, the $\overline{RUN}$ signal goes "low", allowing the sample pulses to start. If the ADC (TRIGGER SOURCE switch) is in FREE RUN, the ENN signal itself will initiate the samples. In either case, the sample pulses are enabled to clock the ADC only after a positive-going transition of the sample pulse itself has been detected. This assures that no partial sample pulses will be generated.

The sample pulse causes the HOLD command to go to its "high" state. The HOLD signal disconnects the track-and-hold module from the analog input signal and stores the last analog value on a capacitor. This process requires about 100 ns, so, 100 ns after HOLD goes "high" ("true"), the $\overline{\text{START}}$ signals go "low", initiating action of the analog-to-digital converter modules.

A $\overline{\text{START}}$ signal is sent to the A-to-D converter module for each channel selected by the 5466B's INPUT (or DISPLAY/INPUT) switch. In the example shown in Figure 2-3, two channels are being used, so $\overline{\text{START A}}$ and $\overline{\text{START B}}$ are sent.

When the $\overline{\text{START}}$ commands are received by the digitizer modules, they respond by setting their $\overline{\text{DONE}}$ signals "high". Analog-to-digital conversion requires approximately 2.5 μs for the 10-bit digitizers, or approximately 4 μs for the 12-bit digitizers. When the digitization is completed, the digitizer modules send their $\overline{\text{DONE}}$ signals to the "low" state.

$\overline{\text{DONE A}}$, the $\overline{\text{DONE}}$ signal from the Channel A digitizer, initiates the data transfer to the Processor. This signal enables sending of the $\overline{\text{DATA READY}}$ (or $\overline{\text{DAR}}$) signal to the Processor as OTA puts the Channel A data onto the data bus. When the Processor has accepted the data word, it returns $\overline{\text{EN}}$ to the ADC. If other data words (from Channel B, C, or D) are to be transmitted to the Processor, subsequent $\overline{\text{DAR}}$'s will be sent to the Processor and these words placed on the bus by the appropriate "OT" commands. The $\overline{\text{DONE}}$ signals also return HOLD to its "low" state, so the track-and-hold modules can prepare for another sampling of the input signal(s).

The ADC continues converting data points until it is stopped by the Processor when all the selected data blocks have been filled.

The ADC is turned OFF (ENN goes low) if one of the following occurs:

1. $\overline{\text{EN}}$ goes low without DAR being sent

2. Approximately 5 μs passes between the time a DAR is sent and an $\overline{\text{EN}}$ is received from the computer.

Control of ADC operation and data transfer to the Processor requires a Microcircuit Interface Card (MIC) for the ADC and a second MIC for the 5475A Keyboard; these cards are installed in Processor I/O slots, as indicated in Section I of this manual. The control words associated with these cards are "DATA" and "KEYBOARD", respectively.

A DATA word contains the digitized ADC output and the input range code. The ADC output is either 10-bits or 12-bits long, depending on the digitizers installed. The DATA word also contains the display code word, "DISPCT".

The KEYBOARD word transmits status signals concerning Sampling Rate, "EO", "DF", "X5", "X2", "S2", "S1", and the remote programming status word, "REMOTE", to the Processor. Block size information for the Sample Generator and for the 5475A indicator lamps is provided by Lines $\overline{\text{N6}}$ through $\overline{\text{N12}}$ from the Keyboard MIC.

ADC CIRCUIT CARDS

The 5466B ADC unit contains seven or ten circuit cards, depending on whether it is to be able to digitize two or four channels. Major signal flow is shown functionally in the diagram, Figure 2-2. Internal wiring is shown in Figure 2-11.

A1 (and A2) Input Assembly (05466-60013)

A two channel ADC will have one of these assemblies (installed as "A1"); a four channel ADC will have two of these assemblies (installed as "A1" and "A2").

The Input Board Assembly consists of two identical, independent, channels of amplification. Each channel consists of two amplifier stages; gains of these stages are controlled by decoding three binary signal lines, as indicated in Table 2-2.

Table 2-2. Input Amplifier Gain Selection

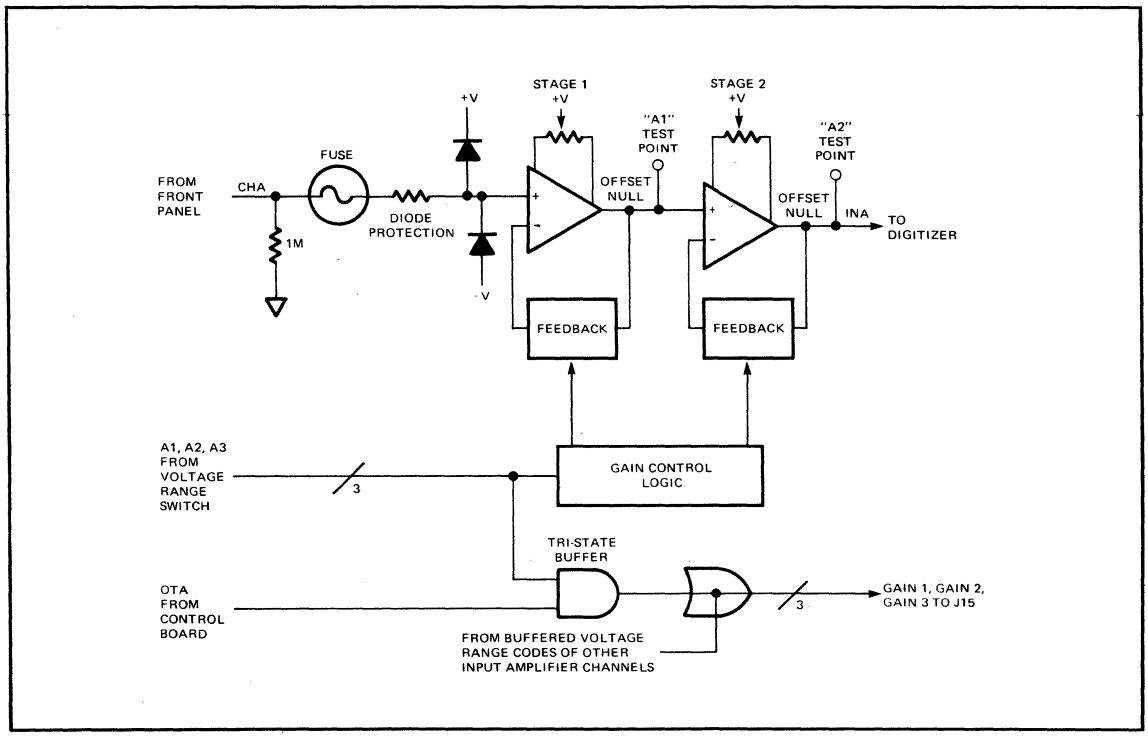
INPUT RANGE	A1, B1 C1, D1	A2, B2 C2, D2	A3, B3 C3, D3	GAIN STAGE 1	GAIN STAGE 2	GAIN OVERALL
8.00 Volts	1	1	1	1	1.25	1.25
4.00 Volts	1	1	0	2	1.25	2.50
2.00 Volts	1	0	1	4	1.25	5.00
1.00 Volts	1	0	0	8	1.25	10.00
0.50 Volt	0	0	1	8	2.50	20.00
0.25 Volt	0	1	0	8	5.00	40.00
0.125 Volt	0	1	1	8	10.00	80.00
CHECK	0	1	1	8	10.00	80.00

A block diagram of one of the two input channels on the Input Board Assembly is given in Figure 2-4. Voltage gain is provided by two similar stages of feedback amplification. The first stage uses a FET hybrid operational amplifier for gain, and a MOSFET multiplexer to select the desired amount of feedback. Depending on the amount of feedback, the first stage provides gains of 1, 2, 4, or 8. The second stage is the same as the first, except that it uses a monolithic operational amplifier, and provides gains of 1.25, 2.5, 5.0, or 10.

The three least-significant bits in the data word sent from the ADC to the Processor represent the gain code for the input channel in which the word originated; for example, if the digitized word is from Channel A, then the three least significant bits are A1, A2, and A3. These bits are transmitted by wire-ORing the outputs of tri-state buffers on the Input Board. When Channel A is being sent to the Processor, the OTA signal will enable the outputs of these buffers onto the input voltage range bus, Gain 1, Gain 2, and Gain 3. This bus transmits these bits directly to the Processor.

The 05466-60013 Input Board has a breakdown diode and a two-position jumper to allow its use in units having different positive-voltage power supplies. For the 5466B, this jumper must be installed in its "B" position.

Figure 2-4. Input Board — Block Diagram (One Channel) (05466-60013)



A3, A5 (and A4, A6) Digitizer Assemblies

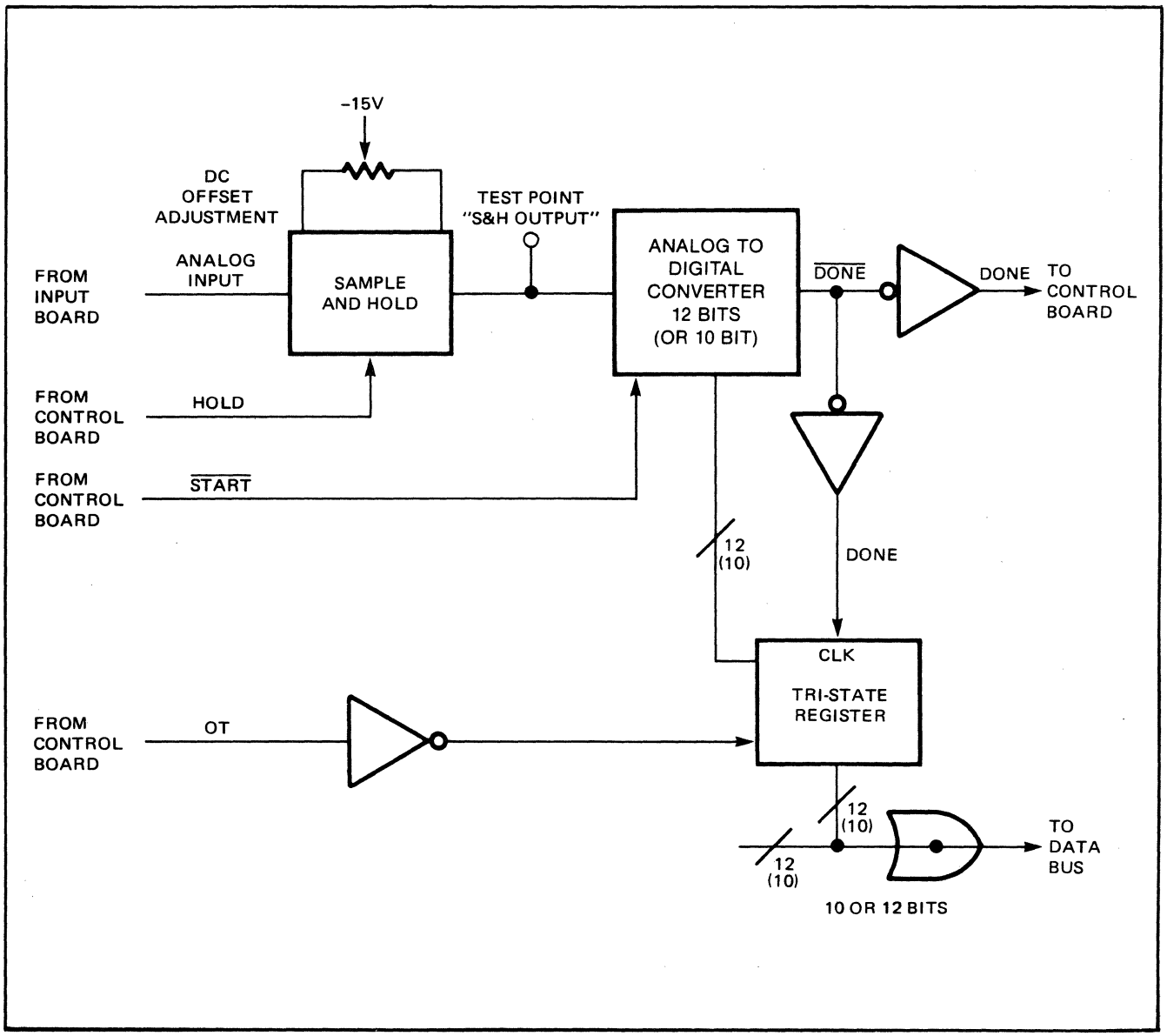
Each Digitizer Assembly handles one channel. For two-channel operation, only A3 and A5 are installed; for four-channel operation, all four digitizer slots are filled.

10-BIT, 200 kHz DIGITIZER (05466-60002) OR 12-BIT, 200 kHz DIGITIZER (05466-60007)

Either of the digitizers described in this manual subsection converts analog signal levels into corresponding digital data words; these data words are then transferred to the Processor for processing. The operation of the assembly is based on two major components: The track-and-hold module and a ten-bit or twelve-bit analog-to-digital converter. A block diagram of the digitizer board assembly is given in Figure 2-5.

When HOLD is "low", track-and-hold module's output is allowed to follow its input (which is the output of the input amplifier for that channel). The analog signal level at the instant HOLD goes "high" is stored on a capacitor, allowing analog-to-digital conversion of the input signal to be performed at definite points of time.

Figure 2-5. Digitizer Assembly — Block Diagram (05466-60002 or -60007)



Shortly after HOLD goes "high", $\overline{\text{START}}$ goes "low", initiating the a-to-d conversion. The converter module accepts the $\overline{\text{START}}$ command, starts its internal clock, and begins to digitize the analog value at its input, using the "successive approximation" technique. After a short time (approximately 2.5 μsec, for 10-bit conversion, or 4 μs for 12-bit conversion) the conversion is completed, and a $\overline{\text{DONE}}$ signal is generated by the module. This signal is inverted on the Digitizer board and sent to the Control Board Assembly (A9); the $\overline{\text{DONE}}$ signal is also inverted and used to clock the digitized word onto the output register.

The output register consists of four four-bit tri-state flip-flop IC's that store the data word until it is put onto the data bus for transmission to the Processor. Depending on the 5466B configuration, one or three other digitizers will also output data to the Processor via this data bus.

12-BIT, 100 kHz DIGITIZER (05466-60014)

The two major circuits on this board assembly, as shown in Figure 2-5a, are the track-and-hold (or sample-and-hold) amplifier and the twelve-bit Analog-to-Digital converter.

When the HOLD input signal is "low", the track-and-hold circuit's output is allowed to follow its input (which is the output of the input amplifier for that channel). The analog signal level at the instant HOLD goes "high" is stored on a capacitor, allowing analog-to-digital conversion of the input signal to be performed at definite points of time. The output of the track-and-hold circuit can be viewed at the "S/H OUT" (for "Sample-and-Hold Output") test point on the board.

CAUTION

Shorting the S/H test point to ground will DESTROY THE BUFFER AMPLIFIER, U1.

Shortly after HOLD goes "high", the START signal goes "low" initiating the a-to-d conversion. The converter circuit accepts the START command, starts its internal clock, and begins to digitize the analog voltage at its input using the "Successive Approximation" technique. After a short time (approximately 6 μs) the conversion is completed, and a DONE signal is generated by the converter. This signal is sent to the Control Board Assembly (A9); the DONE signal is also inverted and used to clock the digitized word into the output register.

A timing diagram for the 05466-60014 Digitizer Board Assembly is presented in Figure 2-5e.

More-detailed descriptions of the board's major circuits are presented below.

The block diagram for the track-and-hold circuit is presented in Figure 2-5b. The first stage of this circuit (A1) consists of a wide-band op-amp and current buffer connected to form an inverting amplifier with a gain of -.5. The input impedance is approximately 2.4K ohms. The current buffer is required to drive the low impedance second state without distortion.

Switches SW1 and SW2 are DMOS FET switches that open and close in phase. When these switches are closed, the op-amp and current buffer that compose A2 act as an inverting unity gain amplifier, presenting the input signal (at half its original amplitude) at the "S/H OUT" test point, which is also the input to the ADC portion of the Digitizer Board.

When SW1 is opened, the output of A1 is disconnected from the input of A2, and the capacitor (C_{HOLD}) from A2's output to its input causes A2 to hold the "S/H OUT" voltage at its present level until SW1 is closed again.

One characteristic of a FET switch is that a portion of the signal used to control the switch gets coupled through the switch when turning it off, thus appearing on the signal line. In this circuit, FET switch SW2 is used to couple the switching signal (only) to one A2 input, making this control signal a common-mode signal which will not appear at "S/H OUT". The pedestal adjust capacitor permits a more precise adjustment of the level of the switching signal presented at A2's input by SW2.

A block diagram of the ADC part of the Digitizer Board is presented in Figure 2-5c, and a block diagram of the DAC used in the ADC circuit is presented in Figure 2-5d.

Normal ADC circuit operation is described below.

When START goes low, it causes the Timing Locic to send RESET and one clock pulse to the Successive Approximation Register (SAR). In the SAR, RESET resets the twelve parallel data lines to "1000 0000 0000", representing zero volts, on the first positive-going clock edge. (In the SAR, "1111 1111 1111" represents the maximum full-scale positive voltage, and "0000 0000 0000" represents the maximum full-scale negative voltage.)

The SAR's output drives a 12-bit Digital-to-Analog (DAC) circuit. The DAC converts the 12-bit SAR output to a proportionate current level. The DAC's conversion gain is set by the digitizer board's "Full-scale" adjustment; this gain is set for 4 mA full-scale current (when the SAR output is "1111 1111 1111").

The DAC's output is applied as one input to the current summation node. A second input to this node is the output signal from the sample-and-hold circuit, a current proportional to the analog input voltage at the time the sample was taken. By working successively with one SAR bit at a time, beginning with the most-significant bit, twelve approximation operations are performed, each one with the aim of making the DAC output current as close as possible to the current from the sample-and-hold circuit. The Comparator's output is a logical "1" when the sample-and-hold's current is greater (i.e., more DAC current required) or "0" when the sample-and-hold's current is less (i.e., less DAC current required).

Each of the twelve successive approximations uses the same technique. First, the SAR bit to be tested is set to a logical "1", causing the DAC to put out a proportionate (or proportionately increased) current (see Figure 2-5d). The DAC's output is then compared against the current from the sample-and-hold circuit; the result of this comparison determines the Comparator's output logic level (as described in the preceding paragraph). During the next clock time, the Comparator's output logic level is strobed into the SAR bit position just tested, and the next-less-significant SAR bit is set to "1" to be tested. The successive approximation procedure is illustrated in a chart below. At the end of the 13th clock time, all 12 SAR bits will have been tested, and had their logic levels assigned by the Comparator. Now the SAR's contents are strobed into the tri-state buffer register and a DONE signal is sent to the ADC's control board. The buffer register's contents are allowed to be put out on the data bus by an OT (Output) signal (OT A, etc.) from the Control Board, directed to the Digitizer Board.

A more detailed description of SAR and DAC operation is presented below.

The DAC acts like a variable current source whose current is controlled by the contents of the SAR. It consists of twelve parallel current paths, each of which is controlled by one bit of the SAR. A logical "1" on the corresponding SAR bit allows current to flow, a logical "0" opens the circuit. The resistances are adjusted so the current through each path corresponds to the weighting of the SAR bit that controls it. For example, a "1" in the SAR MSB allows one-half of the DAC's maximum current to flow; a "1" in SAR bit 7 allows 1/32 of the DAC's maximum current to flow. The SAR contents are changed at each CLOCK time as indicated in the chart below.

SAR Operation

CLOCK TIME	COMPARATOR LOGIC LEVEL*	SAR CONTENTS*		
1 (RESET)	don't care	1000	0000	0000
2	A	A100	0000	0000
3	B	AB10	0000	0000
4	C	ABC1	0000	0000
5	D	ABCD	1000	0000
6	E	ABCD	E100	0000
7	F	ABCD	EF10	0000
8	G	ABCD	EFG1	0000
9	H	ABCD	EFGH	1000
10	J	ABCD	EFGH	J100
11	K	ABCD	EFGH	JK10
12	L	ABCD	EFGH	JKL1
13	M	ABCD	EFGH	JKLM

*Replace "A" through "M" with "0" or "1", representing the Comparator's output logic level at the corresponding clock time.

Figure 2-5a. Digitizer Assembly — Block Diagram (05466-60014)

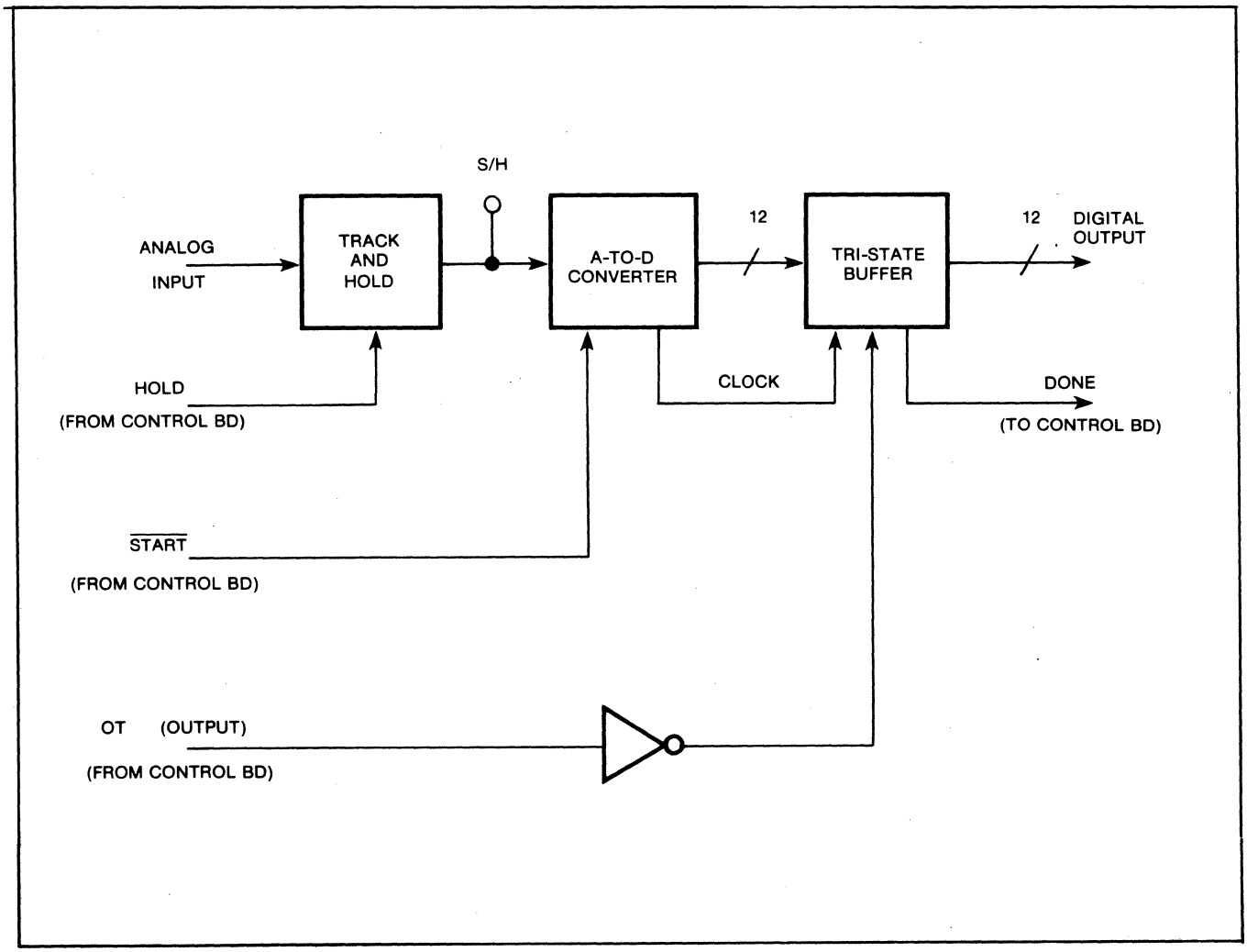


Figure 2-5b. Track-and-Hold Circuit—Block Diagram (05466-60014)

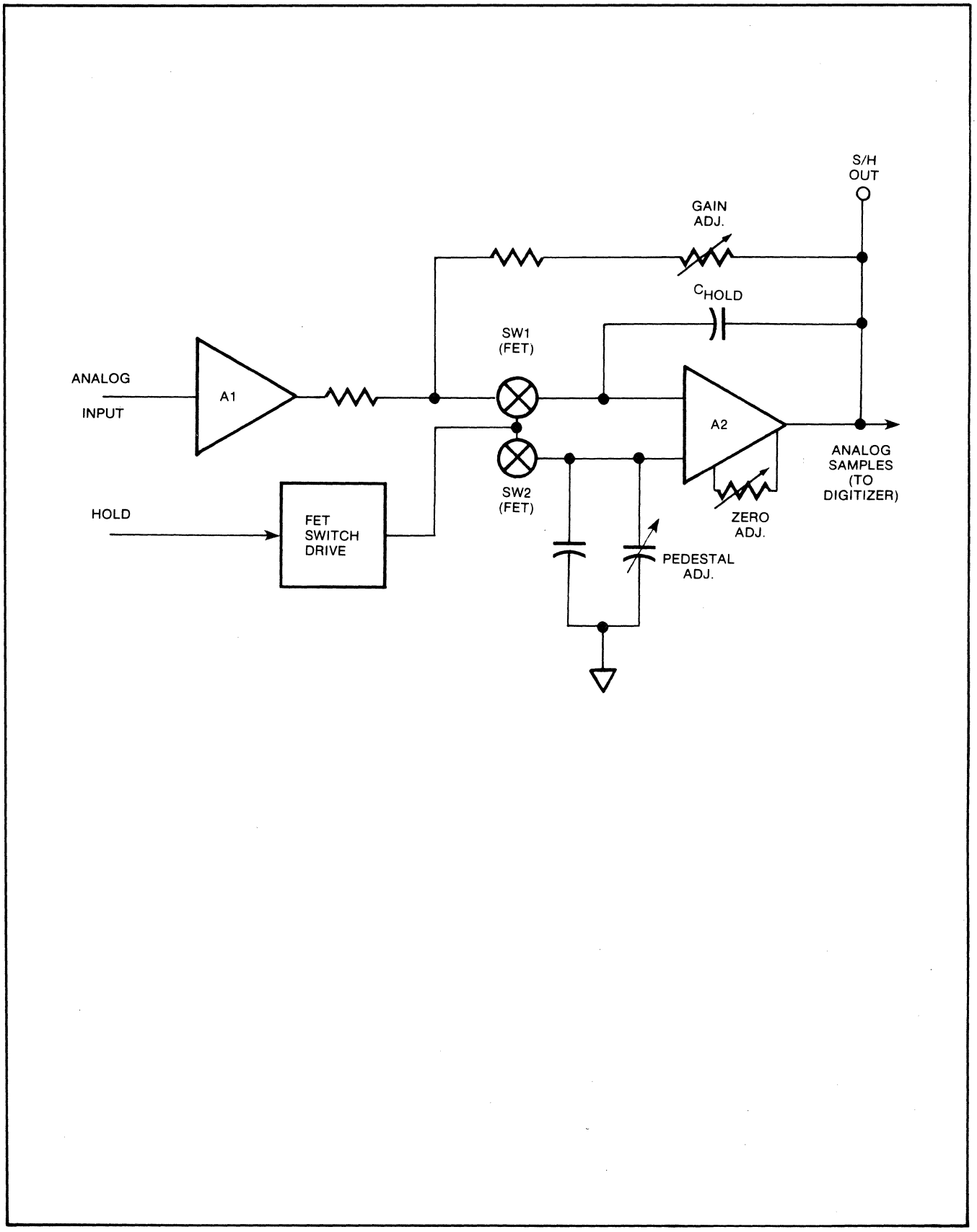


Figure 2-5c. ADC Circuit Block Diagram (05466-60014)

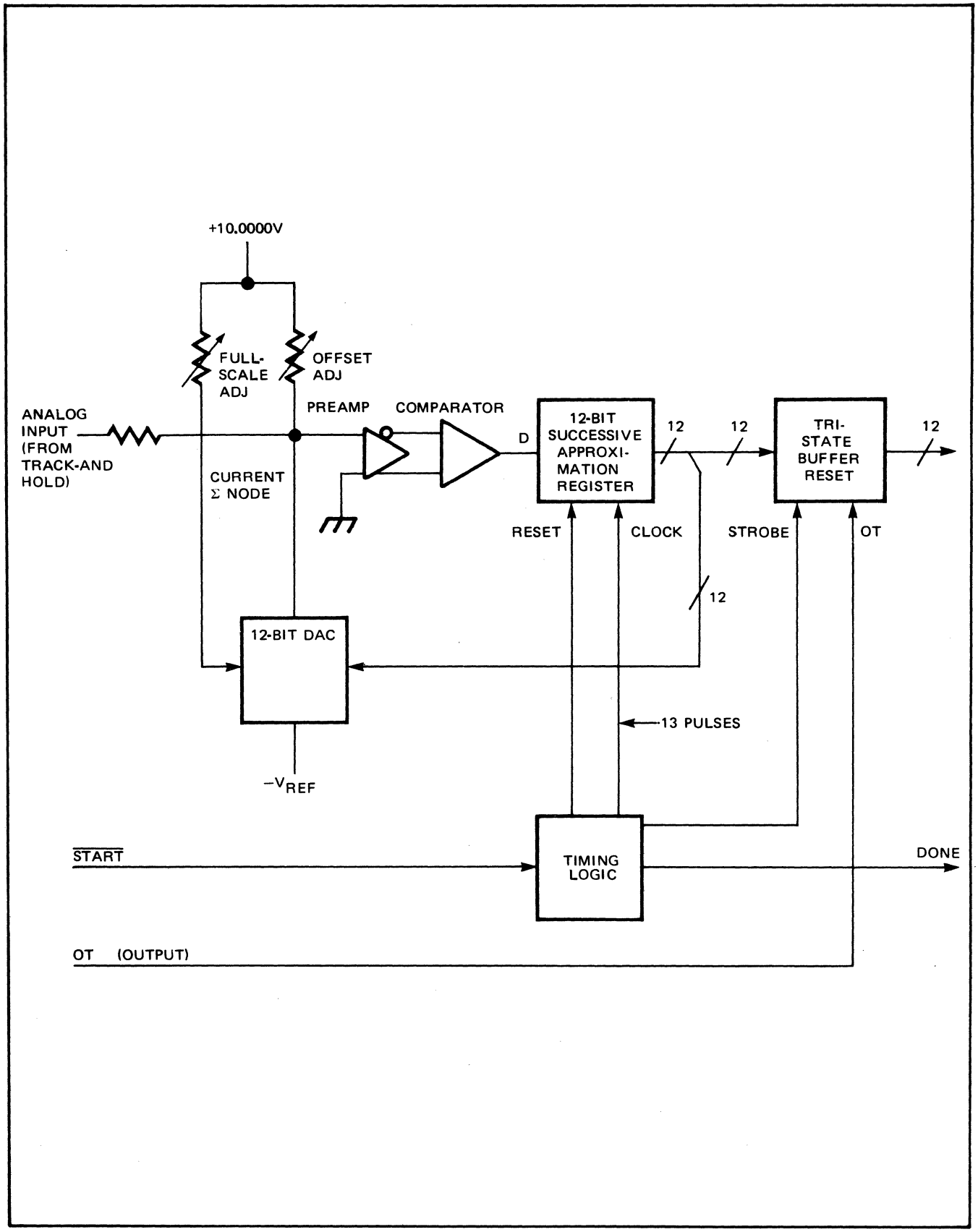
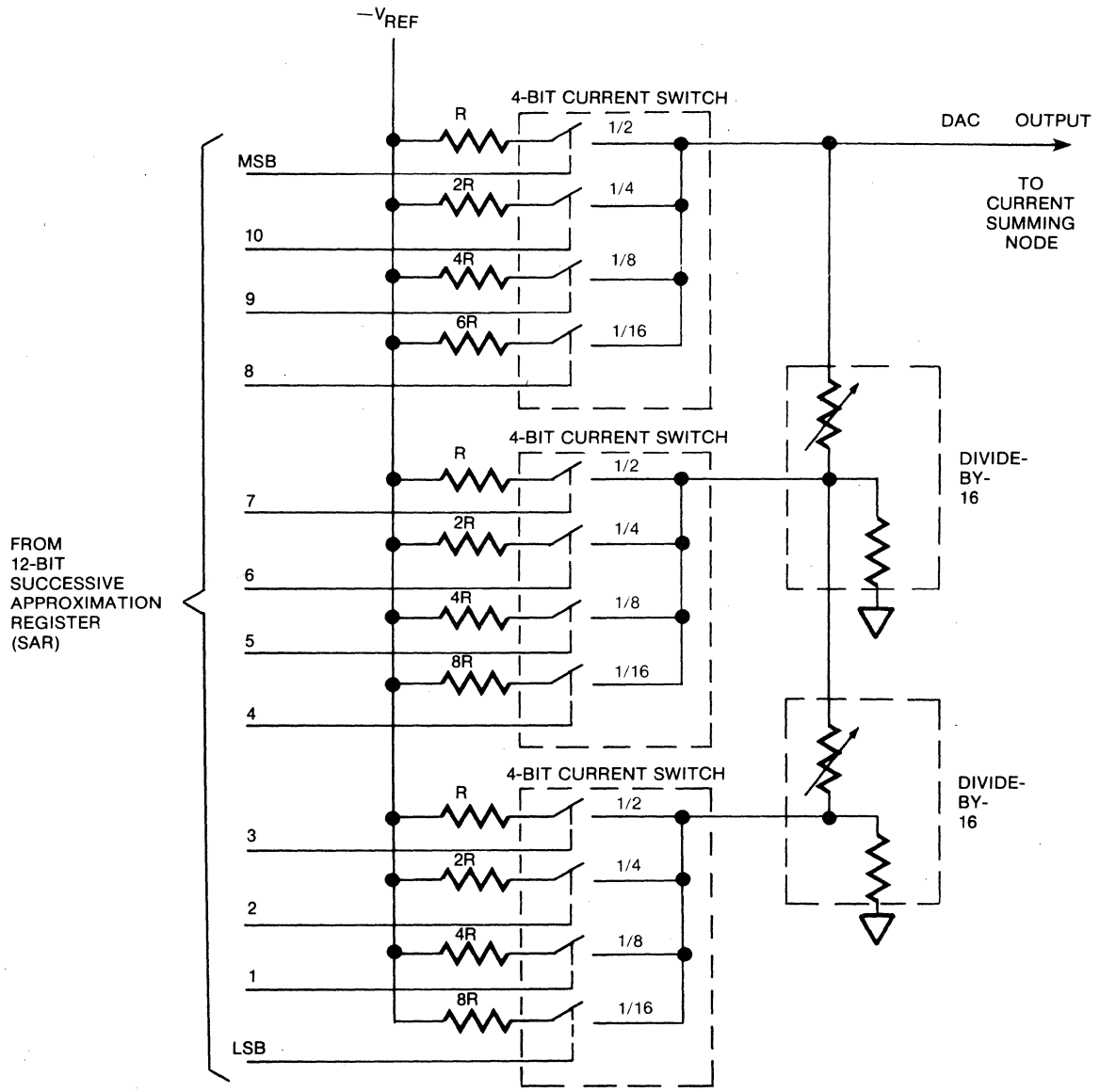
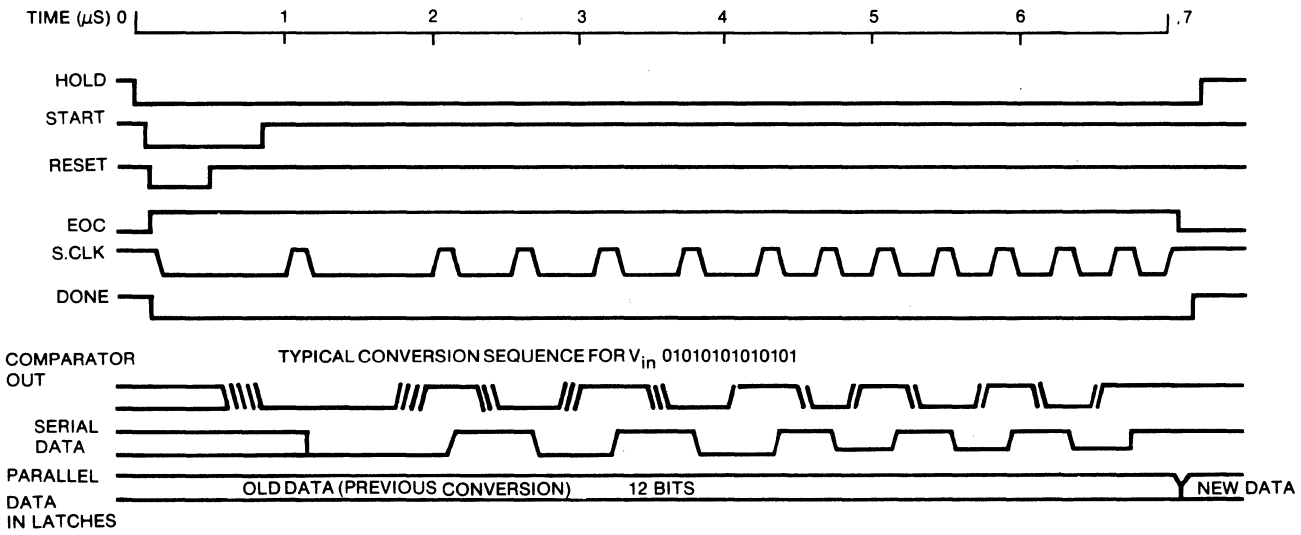


Figure 2-5d. DAC — Block Diagram (05466-60014)



NOTE: A LOGICAL "I" FROM THE SAR CLOSES THE ASSOCIATED SWITCH

Figure 2-5e. ADC Timing Diagram (with 05466-60014)



A7 Error Assembly (05466-60015)

This assembly responds to two operating conditions which are outside the 5466B's specifications. These conditions are: digitized word equal to "full-scale" value (indicating that "overflow" has occurred); and Sampling Rate set too high. A block diagram of the Error Assembly is given in Figure 2-6.

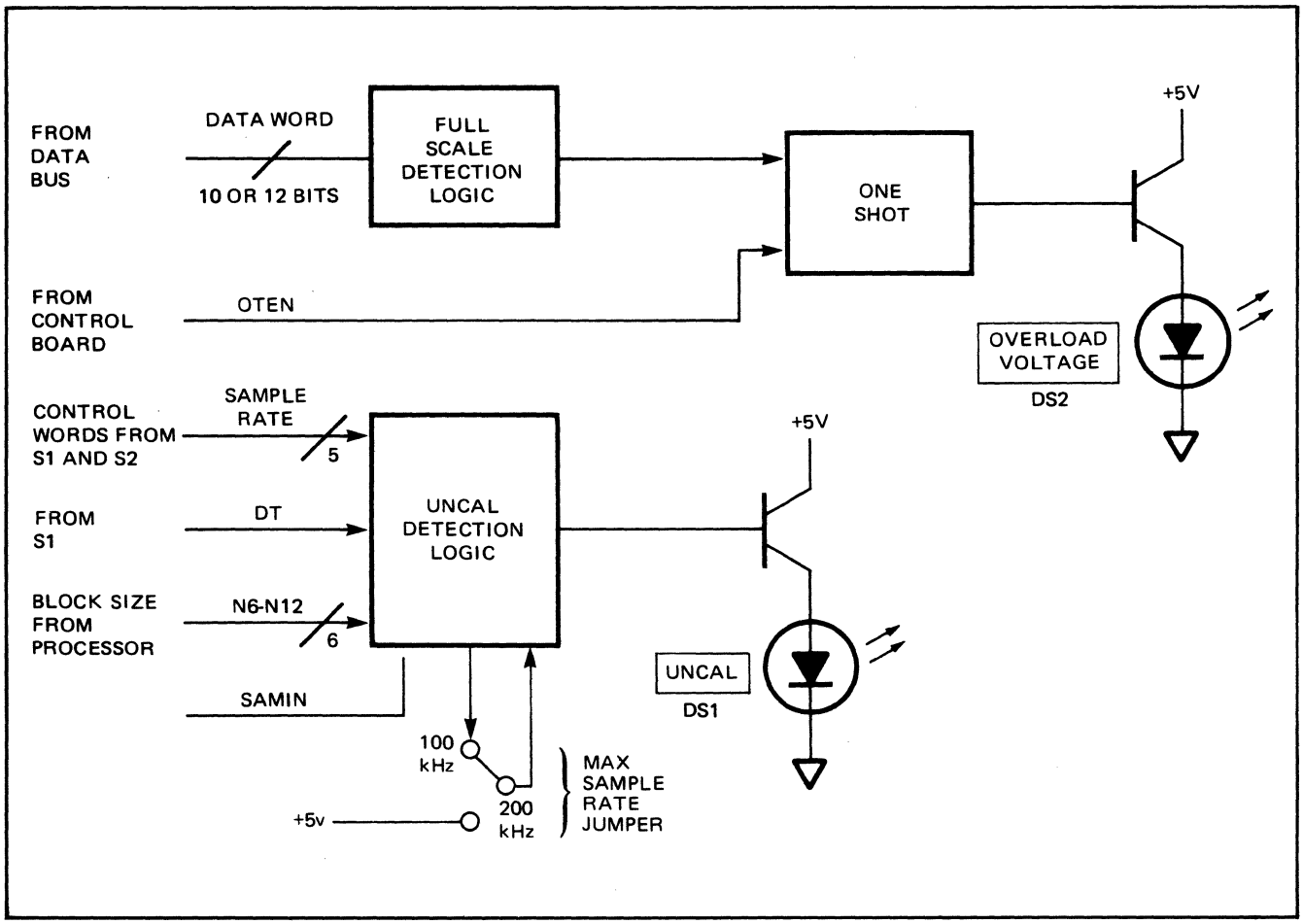
The OVERLOAD VOLTAGE lamp is lighted whenever the digital output word is equal to the positive or negative full-scale value. Combinational logic, using exclusive-OR and conventional logic, detects when the word on the data bus is "full-scale". To avoid spurious signals from this combinational logic as the data is placed on the bus, the signal "OTEN" (from the Control Board) is used to strobe the output of the logic. This strobed output is used to activate a monostable flip-flop, which lights the OVERLOAD VOLTAGE LED (light emitting diode) indicator on the 5466B's front panel. Jumpers on this board enable the user to set up the overload voltage detection logic for either 10-bit or 12-bit data words.

The UNCAL logic looks at the settings of the SAMPLE CONTROL switches, and the Block Size signals, and lights the UNCAL lamp if the sampling rate is too fast. The uncalibrated sample rates are listed in Table 2-3. The UNCAL condition is also indicated if the front-panel EXT/INT switch is set to EXT; in this case, the SAMIN signal will be "low". The 100/200 kHz jumper must be installed to correspond with the maximum sample rate of the ADC boards installed in A3 through A5.

Table 2-3. Uncalibrated Sample Rates/Block Sizes

SAMPLE MODE	MULTIPLIER	BLOCK SIZES
ΔTIME, kHz/μs	500/1K/1	ALL
ΔTIME, kHz/μs	250/500/2	ALL
ΔTIME, kHz/μs	100/200/5 (when 100/200 kHz A7 Jumper is in 100 kHz position)	ALL
ΔFREQ, Hz/ms	500/1K/1	256 ≤ ALL ≤ 4096
ΔFREQ, Hz/ms	250/500/2	512 ≤ ALL ≤ 4096
ΔFREQ, Hz/ms	100/250/5	1024, 2048, 4096
ΔFREQ, Hz/ms	50/100/10	2048, 4096
ΔFREQ, Hz/ms	25/50/20	4096 only

Figure 2-6. Error Assembly — Block Diagram (05466-60015)



A8 Trigger Assembly (05466-60004)

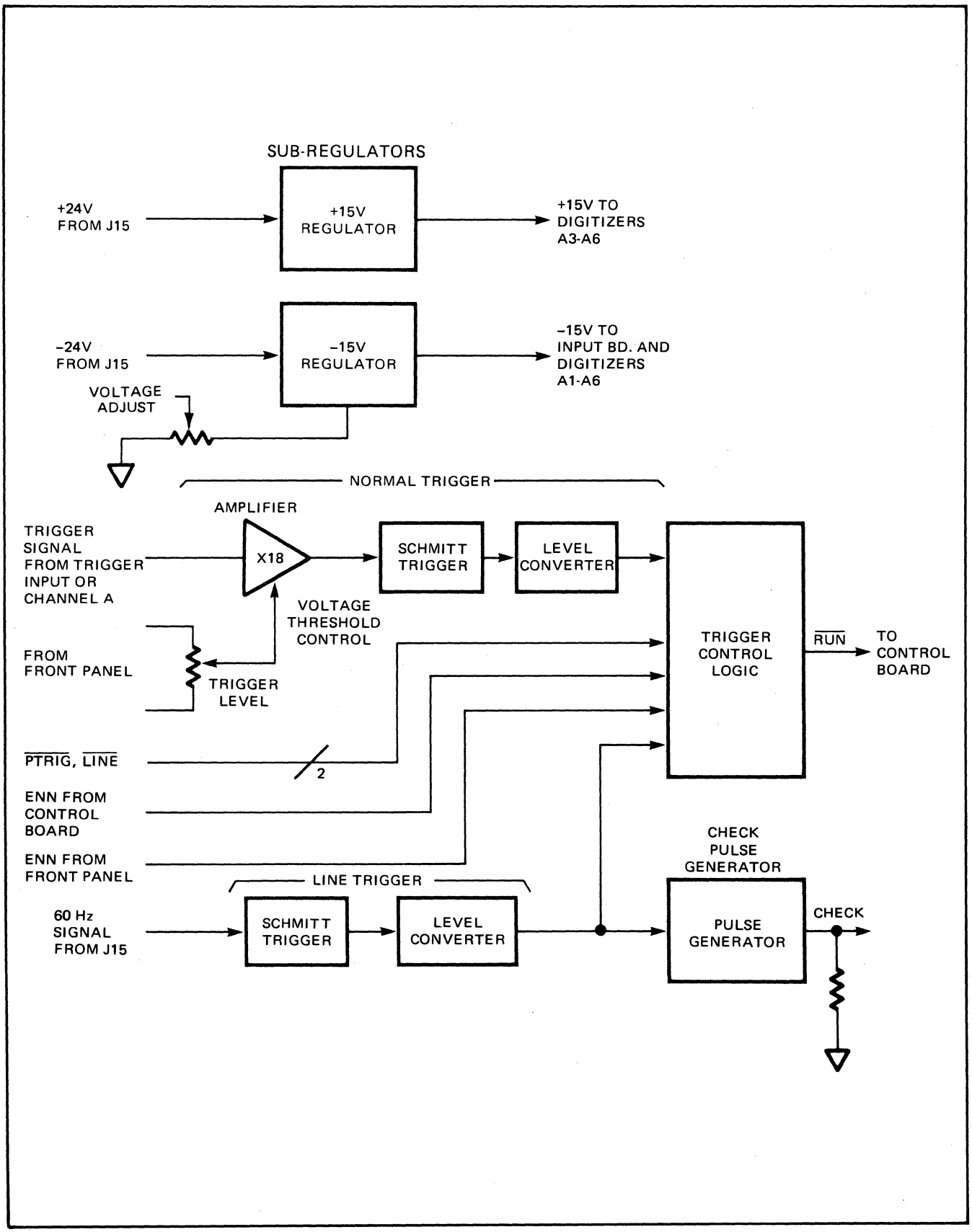
This assembly contains the signal conditioning and waveshaping circuitry to generate logic trigger pulses to start the ADC's operation. These pulses are generated from internal, external, and line trigger sources. The board also generates a self-CHECK calibrating signal for the ADC, and provides regulated plus-and-minus 15V power from plus-and-minus 24V inputs. A block diagram of the Trigger Board Assembly is given in Figure 2-7.

The "trigger" signal comes from the ADC's front-panel TRIGGER INPUT connector or from the output of Channel A's Input Amplifier. TRIGGER SOURCE selection is made by a switch on the ADC's front panel.

The "internal" or "external" trigger is amplified by a X18 amplifier. A level shifter associated with this amplifier allows its output to be shifted anywhere from approximately -10V to approximately +10V, so the following stage, a Schmitt Trigger, can trigger on any part of an ac waveform. The Schmitt trigger's output is passed through a level converter so it can be used by TTL control logic.

The "line" trigger circuitry operates from the 60-Hz sine wave signal available at the 5466B's rear-panel connector J15. A Schmitt trigger converts this signal to a 60-Hz square wave; this trigger's output is also passed through a level converter so it can be used by the TTL Trigger Control Logic circuit. The "line" "trigger" signal is also used to trigger a monostable pulse generator to produce the CHECK signal; this signal is a train of pulses approximately 51 mV high, 1100 μs wide, routed to each of the Input Amplifiers.

Figure 2-7. Trigger Assembly — Block Diagram (05466-60004)



The Trigger Control Logic processes the logic transitions produced by the "normal" ("internal" or "external") trigger or the "line" trigger. If the signal "$\overline{\text{LINE}}$" is "low", the "normal" trigger will be used to produce the signals that start the ADC's operation, and $\overline{\text{PTRIG}}$ will determine the slope (or transition) that will be the triggering edge; "low" $\overline{\text{PTRIG}}$ = "positive-going" transition triggers, "high" $\overline{\text{PTRIG}}$ = "negative-going" transition triggers. If "$\overline{\text{LINE}}$" is "high", the "line" trigger is used, and $\overline{\text{PTRIG}}$ has no effect.

$\overline{\text{RUN}}$ is produced when the Trigger Control Logic is armed by the "ENN" signal, and then detects the correct logic transition in the output of the selected trigger source.

A9 Control Assembly (05466-60008, 05466-60009, or 05466-60016)

The A9 Control Assembly may be any of three different boards. The 05466-60016 card is a universal type, capable of working with or without multiplexers. Some early systems use a 05466-60008 or an 05466-60009 A9 board. The 60008 is used in systems without a multiplexer. The 60009 board is used in systems with a multiplexer.

This assembly contains all the logic necessary to communicate with the Processor, start the digitizers, and transmit data words to the Processor. A block diagram of this assembly is given in Figure 2-8.

The ADC passes data to the Processor in a "handshake" manner. In this way, whenever the ADC is ready to transmit a data word to the Processor, it sends the DAR (Data Ready) signal to indicate this. This becomes the computer device flag signal. Similarly, when the Processor is ready to accept a data word, it sends the $\overline{\text{EN}}$ (ENcode) signal to the ADC. This is the computers device command signal. $\overline{\text{EN}}$ is also used initially to turn on the ADC. Because of this dual usage, special Control Board logic (the "ENN Detection Logic) is required to handle it.

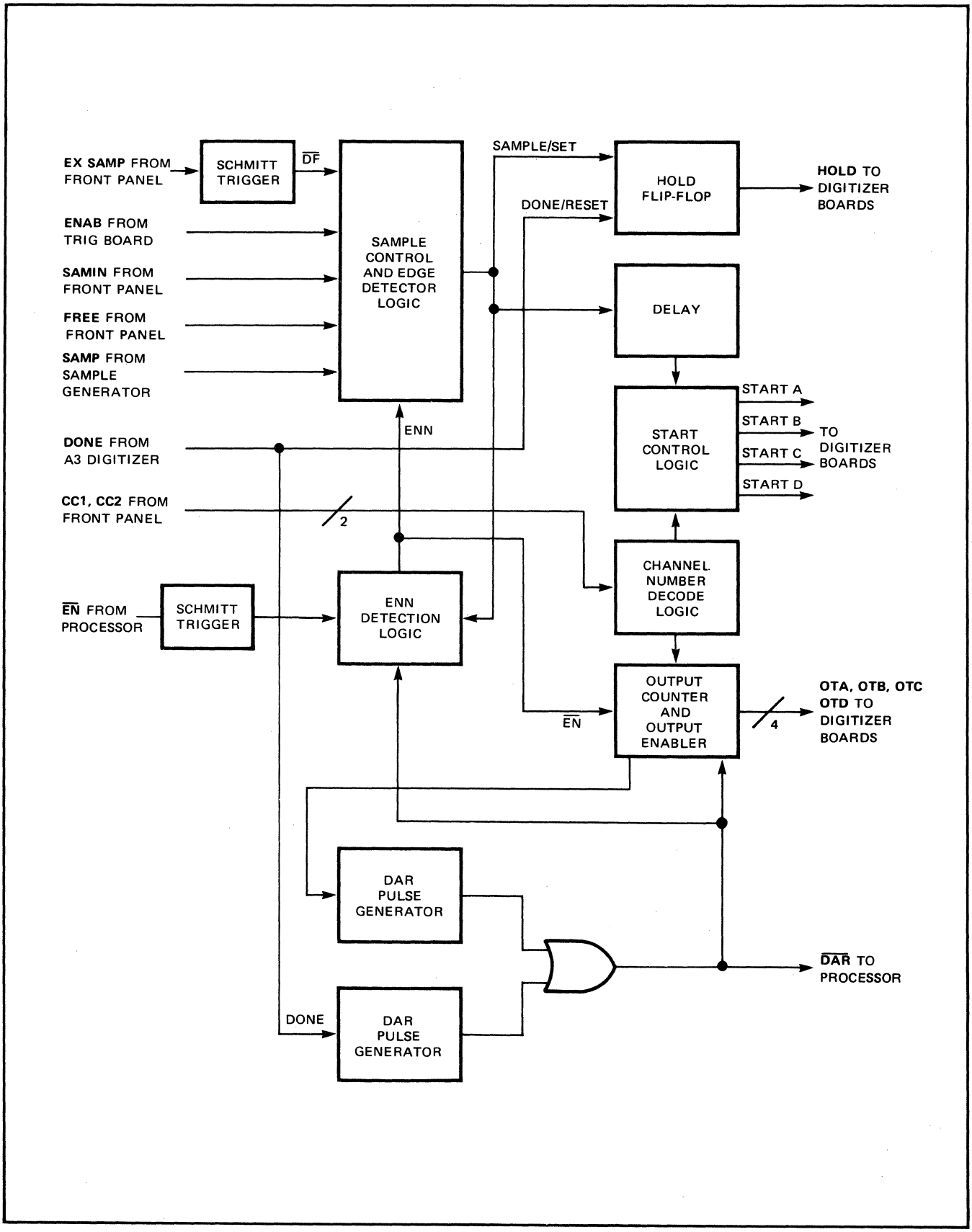
Whenever the ADC is turned "on", ENN is "high", as a result of an $\overline{\text{EN}}$ signal, it is held high until $\overline{\text{EN}}$ goes low without DAR occurring or approximately 5μs elapses since last $\overline{\text{EN}}$ goes low. This condition occurs only when the Processor will accept no more data words, and wants to turn the ADC "off".

The ENN signal, when "high", enables the Sample Control and Edge Detector Logic. SAMIN and FREE define four conditions handled by this logic, as shown in Table 2-4. For the "free" run" mode, with either "internal" or "external" sample control, the logic transmits samples starting with the first positive-going edge of the sample after ENN goes "high". For the "triggered" mode and "external" samples, the logic passes samples starting with the first positive-going edge of the sample after both ENN and the signal ENAB (from the Sample Generator Board) go "true". By waiting until the positive edges of pulses are received, the logic assures that no partial pulses are sent to other sections of the Control Board. For "triggered" mode and "internal" samples, the logic simply passes the pulses, because the sample Generator Board will not send partial pulses.

Table 2-4. Sample Conditions

SAMPLE TYPE		TRIGGER MODE		SIGNALS	
INT.	EXT.	FREE RUN	TRIGGERED	SAMIN	FREE
X		X		H	H
X			X	H	L
	X	X		L	H
	X		X	L	L

Figure 2-8. Control Assembly — Block Diagram



The sample pulses, after passing through the Sample Control and Edge Detector Logic, set the HOLD flip-flop. The HOLD command is sent to all digitizer boards. The sample pulses are delayed and used to send the START command to the appropriate digitizer board. Depending on the "number of input channels" information encoded on the lines "CC1" and "CC2", the START command is sent to 1, 2, 3, or 4 boards, as indicated in Table 2-5.

Table 2-5. Channel Number Encoding

CC1	CC2	NUMBER OF CHANNELS
Ø	1	1
1	1	2
Ø	Ø	3
1	Ø	4

When the Channel A digitizer accepts the START command, its DONE signal goes "low". When a conversion has been completed, DONE returns "high". This serves to reset the HOLD signal, allowing the track-and-hold modules to track the input signal again. It also triggers a monostable pulse generator which sends the $\overline{\text{DAR}}$ command to the Processor if $\overline{\text{EN}}$ is still low. When the Processor returns the ENcode signal, and if the Output Counter Enabling Logic indicates that other ADC channels have data words to be transferred, additional $\overline{\text{DAR}}$ signals are sent to the Processor. With each $\overline{\text{DAR}}$ signal, the appropriate "OT" command is generated, to place the correct A-to-D module data on the bus.

Jumper locations on the Control Board allow some flexibility to meet user operating requirements.

The two-position "ADC"/"MULTX" jumper selects whether the ADC's sample rate or an external multiplexer command will be used to start the digitizer; normally the "ADC" connection is the one that is used.

The two-position "INT"/"EXT" jumper selects the source of sample pulses that will be available at the 5475A's rear-panel SAMPLE OUT BNC connector. In the "EXT" position the SAMPLE OUT pulses are those which are actually controlling the sampling; the 5466B's front-panel EXT/INT switch determines whether these pulses are to come from an external source, or from the ADC's Sample Generator assembly (controlled by the SAMPLE CONTROLs). When this jumper is in its "INT" position, the SAMPLE OUT pulses come only from the 5466B's Sample Generator assembly output, regardless of whether or not it has been selected as the sample control source by the 5466B's EXT/INT switch.

The two-position "2CH"/"4CH" jumpers enable the timing of the return of $\overline{\text{DAR}}$ to the Processor.

A10 Sample Generator Assembly (05466-60006)

This assembly is the "master" timing source for the 5466A. It contains two crystal oscillators, several frequency dividers, sample inhibit logic, the trigger light driver, and the display flag generator. A block diagram of this assembly is given in Figure 2-9.

The 20 MHz oscillator's output is used to generate samples for the "Δt" sampling mode. This signal is divided down to 2 MHz before being passed into the divider chains.

The 8.192 MHz oscillator's output is used to generate samples for the "Δf" sampling mode. This signal is passed through a programmable frequency driver circuit (controlled by block size lines N6 through N12). Depending on the block size code the 8.192 MHz signal is divided by "1,", "2", "4", "8", "16", "32", or "64", as shown in Table 2-6.

Table 2-6. Programmable Divider Coding

For this BLOCK SIZE	This code line is "true"	So the Divider divides by
4096	N12	1
2048	N11	2
1024	N10	4
512	N9	8
256	N8	16
128	N7	32
64	N6	64

The signal "$\overline{DF}$" determines which oscillator's (divided) output is connected to the divider chains; "$\overline{DF}$" "high" = Δf (8.192 MHz oscillator), "$\overline{DF}$" "low" = Δt (20 MHz oscillator).

The first divider in the frequency divider chains is the X2, X5 Divider. Depending on the logic levels of the "X2" and "X5" bits, this circuit will divide by "1", "2", "4", or "10", as shown in Table 2-7. The next circuit will divide by "1", "10", "100", or "1000". The last divider, "EO", divides by "1" or "1000"; its output is the sample pulses that are sent to the Control Board Assembly.

Table 2-7. Coding of Divider Circuits

X2, X5 DIVIDER			S1, S2 DIVIDER			EO DIVIDER	
$\overline{X2}$	$\overline{X5}$	DIVIDE BY	$\overline{S1}$	$\overline{S2}$	DIVIDE BY	EO	DIVIDE BY
1	1	1	0	0	1	0	1000
0	1	2	1	1	10	1	1
1	0	4	0	1	100		
0	0	10	1	0	1000		

In the Sample Generator's composite form, sample pulses of a given frequency are generated for each combination of SAMPLE CONTROL switch settings, as shown in Table 2-8 (for "Δt" sampling) or Table 2-9 (for "Δf" sampling). Note that sampling rates which are too fast for proper ADC operation can be generated; these are indicated in the tables by an asterisk ("*"), and in actual 5466B operation by lighting of the front-panel "UNCAL" lamp.

The Sample Generator is allowed to operate at all times, when the ADC is in its "free run" mode. When not in FREE RUN the Sample Generator is turned "off" whenever the ADC, itself, is turned "off" by the Processor. This operation is controlled by the Sample Inhibit Logic, which also generates this signal which drives the 5466B's front-panel TRIGGERING lamp.

Figure 2-9. Sample Generator — Block Diagram

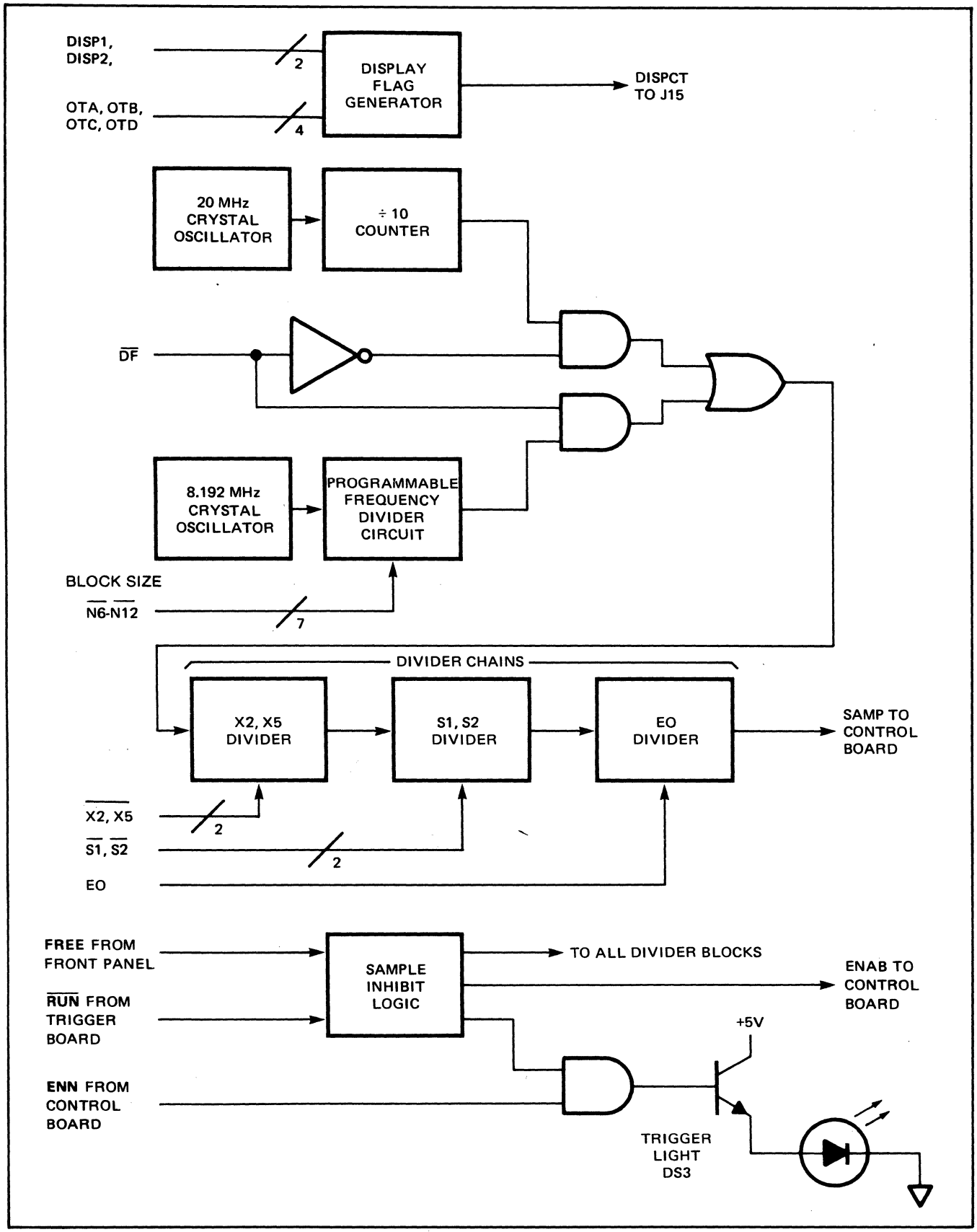


Table 2-8. Δt Sampling

Decimal	FREQUENCY CODE Binary EO (32)	DF (16)	X5 (8)	X2 (4)	S2 (2)	S1 (1)	OSC. FREQ.	DIVISION RATIOS X2, X5	S1, S2	EO	OUTPUT FREQ (Hz)	Δt	Fmax (Hz)
40	1	0	1	0	0	0	20 MHz	2	1	1	1M	1 μs	500k*(UNCAL)
36	1		0	1	0	0		4	1	1	500k	2 μs	250k*(UNCAL)
47	1		1	1	1	1		1	10	1	200k	5 μs	100k**(UNCAL)
43	1		1	0	1	1		2	10	1	100k	10 μs	50k
39	1		0	1	1	1		4	10	1	50k	20 μs	25k
46	1		1	1	1	0		1	100	1	20k	50 μs	10k
42	1		1	0	1	0		2	100	1	10k	100 μs	5k
38	1		0	1	1	0		4	100	1	5k	200 μs	2.5k
45	1		1	1	0	1		1	1000	1	2k	500 μs	1k
41	1		1	0	0	1		2	1000	1	1k	1 ms	500
8	0		1	0	0	0		2	1	1000	1k	1 ms	500
37	1		0	1	0	1		4	1000	1	500	2 ms	250
4	0		0	1	0	0		4	1	1000	500	2 ms	250
33	1		0	0	0	1		10	1000	1	200	5 ms	100
15	0		1	1	1	1		1	10	1000	200	5 ms	100
11	0		1	0	1	1		2	10	1000	100	10 ms	50
7	0		0	1	1	1		4	10	1000	50	20 ms	25
14	0		1	1	1	0		1	100	1000	20	50 ms	10
10	0		1	0	1	0		2	100	1000	10	100 ms	5
6	0		0	1	1	0		4	100	1000	5	200 ms	2.5
13	0		1	1	0	1		1	1000	1000	2	500 ms	1
9	0		1	0	0	1		2	1000	1000	1	1 sec	0.5
5	0	0	0	1	0	1		4	1000	1000	0.5	2 sec	0.25
1	0		0	0	0	1		10	1000	1000	0.2	5 sec	0.1

* = UNCAL for 100 kHz and 200 kHz
** = UNCAL for 100 kHz only

Table 2-9. Δf Sampling

Decimal	FREQUENCY CODE Binary EO (32)	DF (16)	X5 (8)	X2 (4)	S2 (2)	S1 (1)	OSC. FREQ.	DIVISION RATIOS X2, X5	S1, S2	EO	OUTPUT FREQ VS. BLOCK SIZE 4Ø96	2Ø48	1Ø24	512	256	128	64	ΔF	TOTAL TIME
56	1	1	1	Ø	Ø	Ø	8.192	2	1	1	4.Ø96 MHz*	2.Ø48 MHz*	1.Ø24 MHz*	512.Ø kHz*	256.Ø kHz*	128.Ø kHz	64.ØØ kHz	1 kHz	1 ms
52	1		Ø	1	Ø	Ø	MHz	4	1	1	2.Ø48 MHz*	1.Ø24 MHz*	512.Ø kHz*	256.Ø kHz*	128.Ø kHz	64.ØØ kHz	32.ØØ kHz	5ØØ Hz	2 ms
63	1		1	1	1	1		1	1Ø	1	819.2 kHz*	4Ø9.6 kHz*	2Ø4.8 kHz*	1Ø2.4 kHz	51.2Ø kHz	25.6Ø kHz	12.8Ø kHz	2ØØ Hz	5 ms
59	1		1	Ø	1	1		2	1Ø	1	4Ø9.6 kHz*	2Ø4.8 kHz*	1Ø2.4Ø kHz	51.2Ø kHz	25.6Ø kHz	12.8Ø kHz	6.4ØØ kHz	1ØØ Hz	1Ø ms
55	1		Ø	1	1	1		4	1Ø	1	2Ø4.8 kHz*	1Ø2.4 kHz	51.2Ø kHz	25.6Ø kHz	12.8Ø kHz	6.4ØØ kHz	3.2ØØ kHz	5Ø Hz	2Ø ms
62	1		1	1	1	Ø		1	1ØØ	1	81.92 kHz	4Ø.96 kHz	2Ø.48 kHz	1Ø.24 kHz	5.12Ø kHz	2.56Ø kHz	1.28Ø kHz	2Ø Hz	5Ø ms
58	1		1	Ø	1	Ø		2	1ØØ	1	4Ø.96 kHz	2Ø.48 kHz	1Ø.24 kHz	5.12Ø kHz	2.56Ø kHz	1.28Ø kHz	64Ø.Ø kHz	1Ø Hz	1ØØ ms
54	1		Ø	1	1	Ø		4	1ØØ	1	2Ø.48 kHz	1Ø.24 kHz	5.12Ø kHz	2.56Ø kHz	1.28Ø kHz	64Ø.Ø Hz	32Ø.Ø Hz	5 Hz	2ØØ ms
61	1		1	1	Ø	1		1	1ØØØ	1	8.192 kHz	4.Ø96 kHz	2.Ø48 kHz	1.Ø24 kHz	512.Ø Hz	256.Ø Hz	128.Ø Hz	2 Hz	5ØØ ms
57	1		1	Ø	Ø	1		2	1ØØØ	1	4.Ø96 kHz	2.Ø48 kHz	1.Ø24 kHz	512.Ø Hz	256.Ø Hz	128.Ø Hz	64.ØØ Hz	1 Hz	1 sec
24	Ø		1	Ø	Ø	Ø		2	1	1ØØØ									
53	1		Ø	1	Ø	1		4	1ØØØ	1	2.Ø48 kHz	1.Ø24 kHz	512.Ø Hz	256.Ø Hz	128.Ø Hz	64.ØØ Hz	32.ØØ Hz	.5 Hz	2 sec
2Ø	Ø		Ø	1	Ø	Ø		4	1	1ØØØ									
49	1		Ø	Ø	Ø	1		1Ø	1ØØØ	1	819.2 Hz	4Ø9.6 Hz	2Ø4.8 Hz	1Ø2.4 Hz	51.2Ø Hz	25.6Ø Hz	12.8Ø Hz	.2 Hz	5 sec
31	Ø		1	1	1	1		1	1Ø	1ØØØ									
27	Ø		1	Ø	1	1		2	1Ø	1ØØØ	4Ø9.6 Hz	2Ø4.8 Hz	1Ø2.4 Hz	51.2Ø Hz	25.6Ø Hz	12.8Ø Hz	6.4ØØ Hz	.1 Hz	1Ø sec
23	Ø		Ø	1	1	1		4	1Ø	1ØØØ	2Ø4.8 Hz	1Ø2.4 Hz	51.2Ø Hz	25.6Ø Hz	12.8Ø Hz	6.4ØØ Hz	3.2ØØ Hz	5Ø MHz	2Ø sec
3Ø	Ø		1	1	1	Ø		1	1ØØ	1ØØØ	81.92 Hz	4Ø.96 Hz	2Ø.48 Hz	1Ø.24 Hz	5.12Ø Hz	2.56Ø Hz	1.28Ø Hz	2Ø MHz	5Ø sec
26	Ø		1	Ø	1	Ø		2	1ØØ	1ØØØ	4Ø.96 Hz	2Ø.48 Hz	1Ø.24 Hz	5.12Ø Hz	2.56Ø Hz	1.28Ø Hz	.64ØØ Hz	1Ø MHz	1ØØ sec
22	Ø		Ø	1	1	Ø		4	1ØØ	1ØØØ	2Ø.48 Hz	1Ø.24 Hz	5.12Ø Hz	2.56Ø Hz	1.28Ø Hz	.64ØØ Hz	.32ØØ Hz	5 MHz	2ØØ sec
29	Ø		1	1	Ø	1		1	1ØØØ	1ØØØ	8.192 Hz	4.Ø96 Hz	2.Ø48 Hz	1.Ø24 Hz	.512Ø Hz	.256Ø Hz	.128Ø Hz	2 MHz	5ØØ sec
25	Ø		1	Ø	Ø	1		2	1ØØØ	1ØØØ	4.Ø96 Hz	2.Ø48 Hz	1.Ø24 Hz	.512Ø Hz	.256Ø Hz	.128Ø Hz	.Ø64Ø Hz	1 MHz	1k sec
21	Ø		Ø	1	Ø	1		4	1ØØØ	1ØØØ	2.Ø48 Hz	1.Ø24 Hz	.512Ø Hz	.256Ø Hz	.128Ø Hz	.Ø64Ø Hz	.Ø256 Hz	.5 MHz	2k sec
17	Ø		Ø	Ø	Ø	1		1Ø	1ØØØ	1ØØØ	.8192 Hz	.4Ø96 Hz	.2Ø48 Hz	.1Ø24 Hz	.Ø512 Hz	.Ø256 Hz	.Ø128 Hz	.2 MHz	5k sec

A10 Sample Generator Assembly (Cont'd)

The Display Control Logic on this board uses one bit of each data word passed to the Processor to indicate whether the channel associated with that word is to be displayed. The logic decodes the two words "DISP1" and "DISP2", as shown in Table 2-10, to detect which channel is to be displayed. It then checks the "OT" commands and generates the "DISPCT" signal at the same time the data word to be displayed is placed on the data bus.

Table 2-10. Display Coding

DISP 1	DISP 2	DISPLAY CHANNEL
1	1	A
Ø	1	B
1	Ø	C
Ø	Ø	D

HIGH SPEED ADC INTERFACE 05451-60068

The High Speed ADC Interface consists of printed circuit assembly 05451-60068 which is a standard processor size I/O board for use in the 5451C Fourier Analyzer System. Hereafter, the 05451-60068 will be referred to as the ADC Interface.

The ADC Interface provides a first in, first out memory (FIFO) buffered interface from the 5466B ADC to the 54451A System Controller. The ADC Interface contains a static output register to drive the 5475A Control Unit indicators plus all the required digital logic to transfer data from the 5466B ADC into the 54451A Processor. The primary functional features of the ADC Interface are:

1. A 16-bit, TTL level compatible, input bus. This input bus is buffered by a 17 storage level FIFO memory onto the processor backplane. Input words are read from the FIFO either by DMA or under program control via the LIA instruction.
2. A 16-bit, TTL level compatible, output bus. This output bus is buffered from the processor I/O backplane by a static holding register. This register holds the last word output on the output bus.
3. A TTL level compatible device command output line which can be used as a "ready for data" signal for input. This signal is initially activated by an STC instruction and thereafter is activated whenever the FIFO accepts an input word provided no CLC occurs. This output can be wire OR'ed (open collector).
4. A TTL level compatible device flag input line which can be used as an input "data ready" signal.
5. A standard processor flag and interrupt/DMA service request circuits which inform the processor when input data is available in the FIFO under programmed, interrupt, or DMA I/O control.
6. Three LED status indicators are visible on the device connector edge of the printed circuit assembly. When lit, the status indicators correspond to the following conditions:

   RED—An attempt was made to place a word into the FIFO when it was full or an attempt was made to transfer data into the processor when the FIFO was empty. (FIFO overrun)

   GREEN—The FIFO is not empty.

   YELLOW—The device command line is active (low).

The ADC Interface will support any transfer rate available from the device into the processor from 0 to 1.25 Megawords/sec. The device and processor transfer rates need not be equal. Since the FIFO buffer will hold 17 words, a latency from DMA service request/interrupt request or flag FF, (i.e., FIFO not empty) to the first IOI (DMA input cycle or LIA instruction) of the time for the device to output 17 words to the processor can be tolerated.

OPERATION

The following paragraphs describe jumper selectable options and programming information for the ADC.

Jumper Selectable Options

A 2-position jumper is provided to select between the following:

1. A SFC instruction operates normally. Marked 51C on board.
2. SFC instruction never skips regardless of the state of the Flagg FF. Marked not 51C on board.

Programming Information

When an input word is available in the FIFO memory (the FIFO is not empty) a DMA service request will be generated and the Flag FF will be set. This will result in:

1. Request a DMA input cycle.
2. Generate an interrupt (if the other interrupt enabling conditions are met).
3. Allow detection under program control via the SFS and SFC instructions (SFC is limited by the jumper described above).

An input word is removed from the FIFO by either a DMA input cycle or an LIA instruction.

An input data word is entered into the FIFO whenever two conditions are met:

1. The Input Active FF is set.
2. A negative-going device flag edge occurs (with minimum device flag pulse width).

If the Input Active FF is clear (reset), words cannot be entered into the FIFO. The Input Active FF is set by either an STC or a CLF instruction. An STC instruction will also issue a device command and a device command will be issued for each word input until the Control FF is reset (i.e., CLC instruction). Input may be desired when the Control FF is clear and consequently no device commands are issued. It is assumed for this mode of operation that the device command is generated by some external equipment.

The Input Active FF can be set in this case via the CLF instruction, thus any device flag received will enter the input to the FIFO. No device command will be issued. The device command is issued only if the Central FF is set.

The Input Active FF is reset (the input to the FIFO is disabled and no words are entered) if a CLC instruction is issued, or CRS is detected, or POPIO is detected. CRS is control reset from CLC 00. POPIO is power on preset.

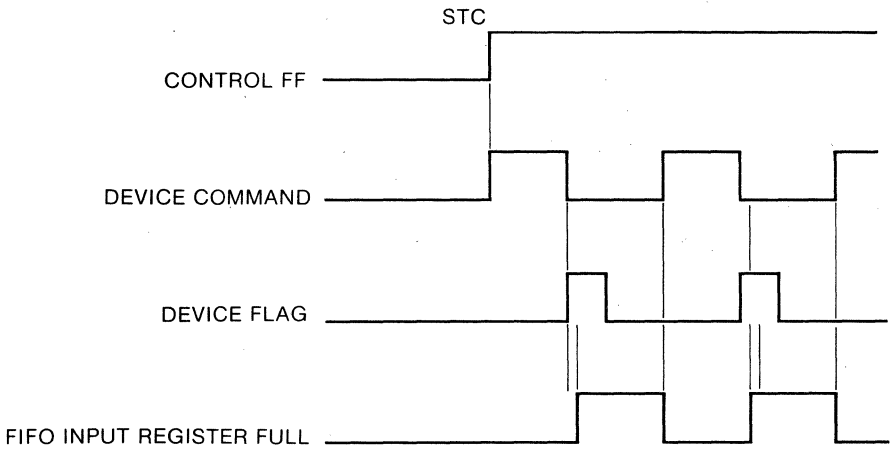
A conflict can arise for a CLC XX,C since CLC would try to clear the Input Active FF while the ,C would attempt to set it. This is resolved by allowing the CLC to dominate and the Input Active FF is reset.

Anytime the FIFO is not empty, the flag will be set on the I/O card. This can be detected by the interrupt system (if Control FF is set) or under program control by the SFS or SFC instruction.

Since device command is automatically issued if control is set, only an initial STC is required for a block of input. A typical input sequence for programmed I/O might be:

```
        LDA     BLKL    FETCH BLOCK LENGTH (2's complement)
        STA     CNTR    SET UP COUNTER
        STC     XX, C   ACTIVATE DEVICE
LOOP    EQU     *
        SFS     XX      INPUT AVAILABLE?
        JMP     *-1     NO, WAIT
        LIA     XX      FETCH INPUT
        STA     BUFR, I STORE INPUT
        ISZ     BUFR    BUMP POINTER
        ISZ     CNTR    DONE ?
        JMP     LOOP    NO
                        BLOCK DONE
```

Note that the setting of the Control FF will issue a device command (which will be reset by an arriving device flag). Therefore as long as the Control FF is set, a device command will be issued as soon as the word entered by the device flat which reset device command is removed from the FIFO Input Register. Refer to the timing diagram in the figure below.



Since device command is not under direct control of STC instruction as is common, if the input operation is under the control of DMA it is possible to have more device commands issued to the device than the number of words required to satisfy the DMA transfer request. This can occur since DMA can not issue a CLC to clear the Control FF until it has taken out of the FIFO the required number of words.

A similar situation is possible for programmed I/O also since by the time a CLC is issued (device command is automatically issued as long as the Control FF is set) additional words may have already been input. While DMA (or program) reads the final words from the FIFO required to complete the transfer, additional device commands can be issued as the FIFO accepts input words.

The OT* instruction outputs a word which is held on the output bus by the output holding register until another OT* changes the output bus.

THEORY OF OPERATION

Figure 2-9a shows the simplified block diagram of the ADC Interface card. The card consists of 3 major functional sections:

1. A 16-bit output data path.
2. A 16-bit input data path including a 16-word FIFO (first in, first out) memory.
3. The controlling logic which has 2 primary functions.
   a. Controlling the FIFO memory in the input data path.
   b. Providing a number of the logic functions required to interface to the processor.

Output Data Path

Refer to the schematic diagram in the 5451C System Hardware manual. The output data path is a 16-bit wide signal path from the Processor Output Bus to the device connected to the ADC Interface output part. Data on the Processor Output Bus is latched into the Output Register consisting of U302 and U402 on the falling edge of IOO addressed to the Interface.

Signals from the Processor addressed to the ADC Interface are detected by the coincidence of IOG, SCLL, and SCML by U304-6. U205-3 buffers this signal, called IOGSC, to provide additional fanout. U304-8 detects IOO addressed to the ADC Interface which is inverted by U103-9 to make OSTRB, the rising edge of which clocks data into the Output Register.

The contents of the Output Register are buffered by inverting line drivers U301 and U401 to provide high current, negative true output signals at the ADC Interface output port (edge connector). The 1K resistors to -2V which appear at the inputs to the Output Register (U302, U402) and on the inputs to any other signals coming from the computer backplane serve to provide solid TTL 0's since the drivers used to drive the backplane can only source current and thus cannot sink the required current to interface directly to TTL.

Input Data Path

The input data path is a 16-bit signal path from the device connected to the ADC Interface input port to the Processor Input bus. The input port is terminated by resistors R5, R6, R11 and R12 to minimize reflections of the cable connected to the port and to provide pullup to TTL 1 since the driving gates are typically TTL which can supply only a relatively small source current. Without the pullup, the risetime from TTL 0 to TTL 1 could be excessive. Note that the termination resistor values are a compromise between the requirements for:

1. Bias to a TTL 1.
2. Sink current required for a TTL 0.
3. Low ac impedance needed to minimize reflections.

To minimize noise sensitivity, the input signals from the input port are received by the Schmidt trigger inverters U501, U601, U701 and U801. In addition, the inversion converts the negative true input signals to positive true signals for input to the FIFO.

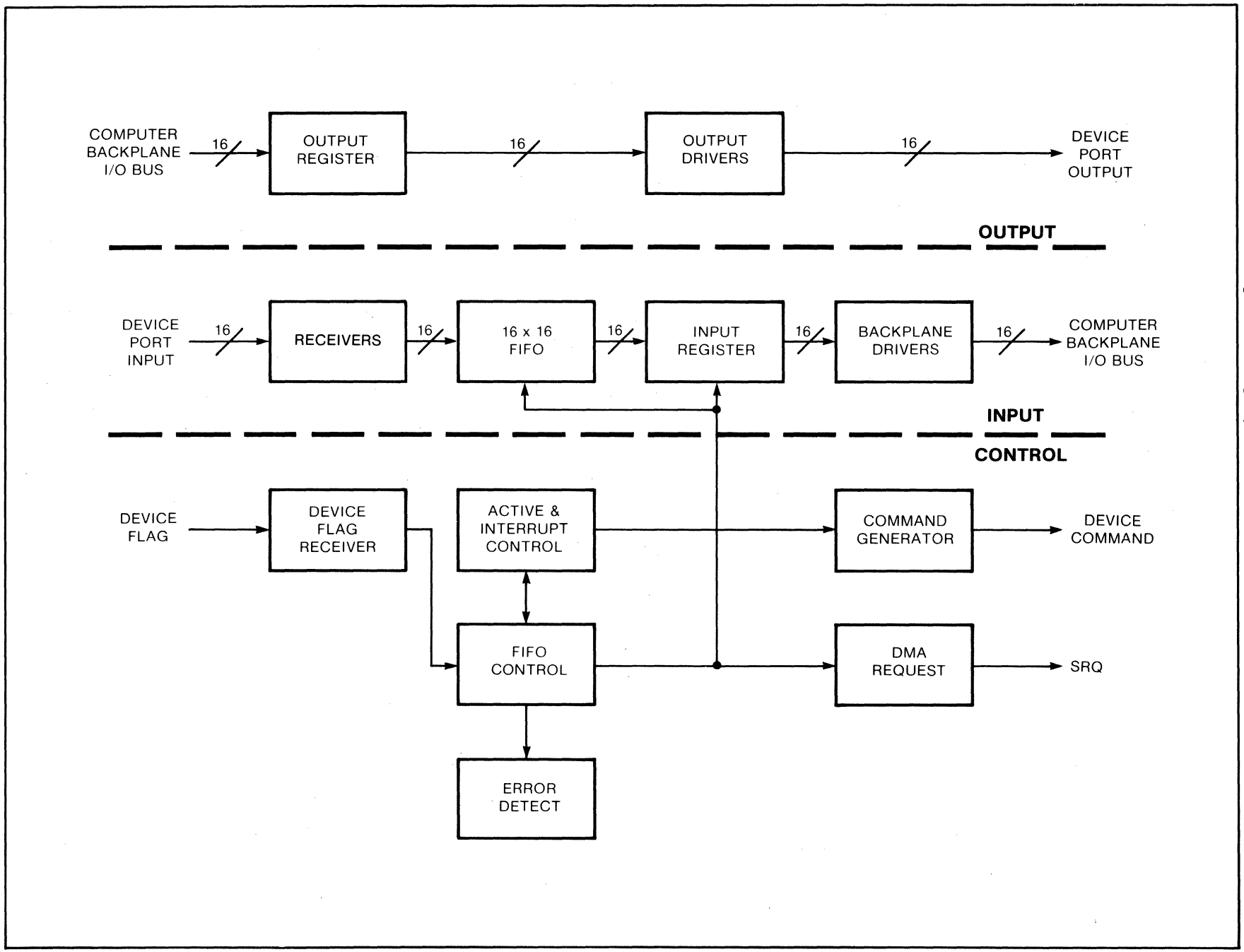


Figure 2-9a. High Speed ADC Interface Block Diagram

On the falling edge of the BFLG signal, the data at the input to the FIFO is latched into the FIFO's (U502, U602, U702, and U802) internal input register. When all FIFO IC's have latched data into their input registers, IRF NOT, U502-1 will go low. It is assured that all the FIFO IC's have latched data by the connections U802-1 to U702-9, U702-1 to U602-9 and U602-1 to U502-9. When U502-1 goes low, the data will be internally moved in the FIFO into the unoccupied level closest to the output. This is accomplished because of the connection of U502-1 to U502-10, U602-10, U702-10, U802-10.

The data at the output of the FIFO is clocked into the Input Register (U603 and U703) on the rising edge of TOP, U503-5. Data in the Input Register is gated onto the processor Input Bus during IOI addressed to the ADC Interface.

The Processor I/O bus is driven by the open emitter (high source current, no sink current) drivers U405, U504, U505, U604, U605, U704, U705, U804, U805. IOI is buffered from the Processor backplane by U205-11. U202-9 and U204-8 detect IOI addressed to the ADC Interface (IOI and IOGSC) to produce IOISC NOT. U202-9, labelled IOI DEGLITCH prevents a negative going glitch on IOGSC from generating an extra rising edge on IOISC NOT since this could cause a data word to be lost by the FIFO. This situation occurs in the 21MX and 21MX-E Processor. IOISC NOT is inverted and buffered by U404-6, U404-8, U404-10 and U404-12 to provide the gating signal to put the input register data onto the Processor Input Bus.

Controlling Logic

The controlling logic has several functional areas as described in the following paragraphs.

Flag Receiver

The negative true device flag is received by Schmidt trigger inverter U501-2. The flag input is terminated for the same reasons the data input lines are terminated. Different values were used for the terminating resistors since more current sink is available for the flag input. U501-2 drives an open collector output gate which in turn drives a low pass filter comprised of R9, R10, and C1. This filter provides additional noise immunity by ensuring that any flag signal less than 75 ns in duration is ignored. Note that the open collector drive and the 2 resistor filter were used since a TTL gate would be able to supply only a relatively small current to charge the capacitor to the TTL 1 state.

The filter output is converted back to a fast edge TTL signal in the Schmidt trigger inverter U501-6. At this point the flag signal is positive true, and a rising edge at U501-6 is detected by a U202-6 causing U202-6 to go high. U202-6 insures that the flag input is only edge sensitive. The rising edge of U202-6 causes U503-13 to go high. The high at U503-13 puts U202-6 back to the low state. This re-arms the Flag Edge Detecor U202-6. For each flag active flag edge, a 100 ns pulse is generated at U503-13, called BFLG. BFLG NOT is generated by U503-4.

FIFO Output Control

Output from the FIFO, (input to the Input Register U603 and U703) is controlled by U503-5, U203-5 and U205-8. To understand the operation of this logic, assume that U203-5 (RF), U503-5 (TOP) and U502-23 are low. When the internal output registers of all the FIFO IC's have data available, U502-23 will go high. The fact that all FIFO IC registers have valid data is ensured by the connection of U802-23 to U702-15, U702-23 to U602-15, U602-23 to U502-15.

When U502-23, called ORE NOT, goes high, U205-8 will go high. On the rising edge of U205-8, U503-5 will go high. The rising edge of U503-5 will clock the data at the output of the FIFO into the Input Register, U603 and U703. The low at U503-12 will cause U203-6 to go low and U203-5 to go high. U203-5 high indicates that the Input Register, U603 and U703, contains valid data. The result will be a 100 ns pulse on U503-5 and U503-12, positive and negative respectively.

The rising edge of U503-12 will cause the FIFO to put the next available data word on the FIFO output after the Processor reads the data word in the Input Register. The rising edge of IOISC NOT will cause U203-5 to go low, indicating that the data has been read. At this point the cycle is complete and the original state of U203-5 and U503-5 is obtained. Note that the output control logic and the FIFO can be forced to the empty state by a low on ACTV, U903-7. Note that if ACTV is low, the Input Register is forced to all zero.

FIFO Error Detection

FIFO errors can be one of two types, input overflow and output underflow, collectively referred to as FIFO overrun. Input overflow consists of an attempt to strobe a word into the FIFO when the FIFO is full. Output underflow is an attempt to read a word from the Input Register that has previously been read. The error indication on the Interface is strictly visual, with no status being available to the Processor. The error condition(s) is latched to aid manual diagnosis. The latches are cleared only by a CLC 00 or Computer PRESET, normally issued only when a software system is initiated.

Input overflow is detected by U203-9 and U403-8 which detect the coincidence of IRF and BFLG. The detection of input overflow causes a 100 pulse negative going pulse at U403-9. This pulse sets the Input Overflow FF, U303-9.

Output underflow is detected by U403-11 on the coincidence of RF NOT and IOISC. Detection causes a negative going pulse at U403-11 equal in duration to IOISC (depends on the Processor cycle time, typically 175 to 550 ns). This pulse sets the Output Underflow FF, U303-13.

The composite (OR) of input overflow and output underflow is available at the OVRN test point. This test point provides a pulse of at least 100 ns duration for either error and is useful for dynamic testing.

The outputs of the two error FF's are OR'd by U803-3 which drives the red ERROR LED thru open collector driver U901-3. This LED provides visual indication of any error since system initialization.

DMA Service Request (SRQ) Generation

DMA service request is generated by the following logic. SRQ is set whenever unread data is available in the Input Register. This is implemented by U305-9. On the rising edge of ENF (processor cycle T2) RF (unread data available signal from the RF FF) is strobed into the SRQ FF.

As long as unread data remains available, SRQ is true, with one exception. If IOISC and ORE is detected by U403-3, i.e., if there are no more words in the FIFO and the data in the Input Register is being read, then the last available word is being read so that another DMA cycle is not needed. In this case, the SRQ FF is forced low via the reset input, U305-13. The output of the SRQ FF is buffered by high source current backplane driver U405-7.

Data Available Logic

In addition to DMA service request, data available in the Input Register is also signaled to the Processor via the Flag FF, U303-7, allowing data to be emptied from the FIFO under SFS control. On each rising edge of TS NOT, U305-6 determines through U304-12 if the following conditions are met:

1. Is data available, i.e., is RF high.
2. Is the Flag FF not set, i.e., is U303-7 low.
3. If a CLF instruction not in progress.

If all these conditions are true, then U305-6 goes low to set the Flag Buffer FF. U305-6 remains low until the following T2.

If data is available in the Input Register, the green AVAIL LED provides a visual indication. The LED is driven by RF through the open collector driver U901-6.

Flag And Control Logic

The Interface flag and control logic are outlined below.

Control FF

The Control FF, U303-4, performs 2 primary functions on the ADC Interface:

1. Enabling and disabling of interrupts.
2. The enabling and disabling of the Device Command Generator.

U303-4 is set by the STC instruction addressed to the ADC Interface detected by U101-11. U303-4 is cleared by either a CLC 00 instruction (which generates CRS) or by the CLC instruction addressed to the ADC Interface detected by U101-8.

Flag FF

The Flag FF, U303-7, is set whenever the Flag Buffer FF, U903-9, is high during the occurrence of ENF (Processor cycle T2). The FLAG FF is used to create the interrupt request to the Processor. The Flag FF is reset by the CLF instruction addressed to the ADC Interface detected by U902-11.

Flag Buffer FF

The Flag Buffer FF, U903-9, is used to buffer requests to set the Flag FF so that the Flag FF is only set during Processor cycle T2 (ENF). In addition, the Flag Buffer FF conditions the interrupt request so that when an interrupt is granted and acknowledged, another will not be erroneously requested. U1003-6 OR's the conditions for setting U903-9.

The STF instruction addressed to the ADC Interface detected by U902-6 will set U903-9. POPIO, which occurs when the Processor PRESET is activated, will set U903-9. The SFB NOT will also set U903-9 whenever the Flag FF is not set and data is available in the Input Register. Two conditions can reset the Flag Buffer FF. The CLF instruction addressed to the ADC Interface detected by U902-11 can clear the Flag Buffer FF. The coincidence of IAK and IRQL detected by U902-8 can also clear it. The clearing conditions are OR'd by U1002-6.

Interrupt Request

The request for an interrupt by the Interface is signaled by the setting of the INT REQ FF, U903-13. The conditions are: Flag FF set AND Flag Buffer FF set AND PRH (priority high) high (i.e., no higher priority I/O card requesting an interrupt) and Control FF set AND IEN (interrupt system on) and Processor cycle T5, i.e., SIR.

The INT REQ FF is reset at each following T2 (ENF). Note that once an interrupt is granted by the Processor, it is acknowledged by occurrence of IAK. IAK clears Flag Buffer FF which removes a necessary condition for setting Int Req FF which prevents erroneously multiple interrupt requests. The output of Int Req FF is buffered as two backplane signals by high source current drivers U1005-7 and U905-9.

Priority Chain

As shown previously, PRH high is a necessary condition for requesting an interrupt since it assures that there is no conflict with a higher priority device requesting an interrupt simultaneously. Similarly, the Interface must signal lower priority I/O cards if it or an I/O card higher in the priority chain is requesting an interrupt. The AND input of the high source current backplane driver U1005-9 detects the condition PRH low (higher priority card requesting interrupt) OR Control FF and set AND Flag FF set AND IEN. Either condition will hold off interrupt requests by lower priority I/O cards by driving PRL low. (Note that PRL on the Interface becomes PRH on the next lower priority I/O card.)

SKF Logic (SFS AND SFC)

The SFS and SFC instructions are implemented by U905-7, U904-10 and U1004-3. Coincidence of the SFS instruction addressed to the Interface and FLAG high is detected by the high source current backplane driver U905-7. The coincidence drives U905-7 high, providing a true SKF signal to the Processor. Similarly,

the coincidence of the SFC instruction addressed to the Interface and the jumper is in the 51C NOT position. In the 51C position, the jumper will cause the SFC instruction never to take SKF high, i.e., SFC will never skip, regardless of the state of the Flag FF.

Input Active Logic

Since the FIFO isolates the input of the ADC Interface from the Processor in the sense that the Interface can get data from the input device without the Processor having read the previous data, a means must be provided to ensure that the data in the FIFO is the desired data. The Input Active FF provides for this by allowing the input port to be closed and the FIFO to be forced to the empty state.

The Input Active FF, U903-7, is set by either the STC instruction or the CLF instruction addressed to the ADC Interface. The OR of these signals appears at the output of U1002-8. U903-7 is cleared by the CLC instruction addressed to the ADC Interface. Note that in the case of a CLC, C instruction to the Interface there could be a conflict, since the CLC portion tries to clear Input Active FF and the C portion tries to set it.

To avoid this problem, the CLCC FF, U903-4, is used. In the case of a CLC ,C the desired action is to clear the Input Active FF. This is assured by U803-11 detecting the coincidence of CLC and ,C and setting the CLCC FF. The high at U903-4 in turn blocks the ,C input from setting the Input Active FF via U803-8. (The race inherent in this circuitry is of no consequence since the correct stable state will be reached with no adverse effects. U903-4 will be cleared at the beginning of the next T2 Processor cycle, in time for the next CLC instruction.

U803-6 guards against clearing the input register while the data is being read (IOISC).

Device Command Generator

In a typical I/O card, the device command is controlled via the STC and CLC instructions. The presence of the FIFO in the ADC Interface requires that the device command be independent of program control for the most part. The logic consisting primarily of U105 controls the generation of device command in the ADC Interface. The state of the Control FF enables or disables the device command generation. Device command generation is enabled only when the Control FF is set. The rising edge of CONTROL clocks U105-9, the 1ST Command FF, low. This propagates down the gate string to the open collector driver U901-8 to become the negative true device command, DCOM NOT.

The reception of a device flag by the Flag Receiver forces U105-9 high. This resets DCOM. As soon as the data word strobed into the FIFO by the device flag is transfered out of the FIFO's internal input register, a rising edge will occur on SDCOM NOT. This will trigger U104-4 low, providing a 100 ns negative true pulse. This has the effect of delaying the rising edge of SDCOM NOT by 100 ns, providing a safety margin between the set and clock inputs of U105-5. The rising edge of U104-4 clocks U105-5 low, which will be the next DCOM NOT. The next device flag will force U105-5 high, and so on. When Control FF is reset, both U105-5, U105-9 will be forced high and U1002-3 will be forced low. This disables the device command generation. U901-11 open collector driver drives the yellow DCOM LED that provides a visual indication that the DCOM is in its active state (i.e., DCOM NOT is low).

OTHER CIRCUITS

U1004-6 provides a buffered version of Processor cycle T3. This signal is not used by the ADC Interface.

U204-6 provides detection of EDT (end of DMA transfer) instruction addressed to the ADC Interface. This signal is not used by the ADC Interface.

Note that it is possible to enable the FIFO and input port of the ADC Interface without enabling the device command generator or issuing DCOM. In addition, since DCOM NOT is driven by an open collector driver pulled up to +5V, it is possible to input data from a device that is not under control of the ADC Interface but rather is being controlled by another device wire OR'd to DCOM NOT. The input enable without device command is accomplished by issuing only a CLF instruction rather than a STC or STC ,C instruction as is typical. This mode is used in the 5451C.

TROUBLESHOOTING

The 05451-60068 ADC Interface is difficult to troubleshoot without special test equipment, due to the timing considerations of the circuits. If the ADC Interface is suspect, one of the following procedures is recommended:

1. Substitute the board with a known properly functioning 05451-60068 board.
2. Substitute the board with a 05451-60025 board. This board is used as the ADC interface in earlier systems and may also be found in optional equiment such as the printer, plotter, 5477A and 5440B. When using an 05451-60025 board for substitution, strap the board as shown in Table 1-2.

   The 05451-60025 has a slower speed of operation so F_{max} must be limited to single channel operation at speeds of less than 50 kHz in the 5451C.

5475A CONTROL UNIT

The 5475A Control Unit provides the necessary pushbuttons and switches to control and manipulate the input data during operation as a Fourier Analyzer System. The Control Unit also provides interfacing between the ADC and the Processor. A complete explanation of each control and the proper operating procedure to perform the required functions is contained in the System Operating Manual.

The 5475A Control Unit consists of a chassis that houses the keyboard panel assembly, keyboard and control logic comprising seven circuit cards, a power supply consisting of six circuit cards, and a receptacle for the 5466B ADC plug-in. Refer to Figure 2-12 and Figure 2-13 for block diagrams and signal interconnection between the keyboard assembly and control unit circuit cards. The Control Unit cabinet can be mounted as one package in a standard rack cabinet.

CONTROL UNIT CONNECTORS

The 5475A Control Unit contains three connectors within the cabinet for internal connection, and four connectors at the rear of the unit for cable hookup. The three internal connectors are shown on the left side of the wiring diagram (Figure 2-13). The J15 connector is a 50-pin ribbon-type female connector that mates with the male connector on the installed A/D Converter. The J16 and J19 connectors are mounted on the baseplate of the control unit directly behind the keyboard panel. J16 is a 24-pin ribbon-type female connector that mates with a cable from the keyboard front panel lights and switches. J19 (A and B) consists of dual 50-pin ribbon-type female connectors that mate with a cable from the keyboard panel pushbuttons. The four rear panel connectors are shown on the right side of the wiring diagram. The J11 (A and B) connector consists of dual 36-pin ribbon-type female connectors that mate with a double male connector and cable to the Processor. The J11A connector is not used in the basic 5451C system. The J11B connector carries signals from front panel switches on the ADC and keyboard through to the Processor interface card. The J12 connector is a 36-pin ribbon-type female connector that mates with a cable from the Processor ADC/keyboard interface card. The J13 connector is a 48-pin etched-circuit male connector that mates with a cable from the Display Terminal I/O connector. The J14 connector is a 36-pin ribbon-type female connector that mates with a cable connected to the Processor interface card. Power connectors on the rear panel are described in the Power Supply Circuit (A1 through A6). "J2b" is a 50-pin ribbon connector which carries the remote control signals between the ADC and the 5477A system control (if installed).

A11 KEYBOARD ASSEMBLY

The keyboard is a self-contained assembly with a front panel enclosing 63 pushbuttons, 2 lever switches, a slide switch, and 10 indicator lights. The keyboard pushbuttons are connected to the Control Unit by a cable terminating in dual 50-pin connectors (P19/J19). The switches and indicator lights are connected to the Control unit by an additional cable terminated by a 24-pin connector (P16/J16).

The keyboard pushbuttons simulate the function of a teletypewriter. Sixty lines transfer signals from sixty pushbuttons on the keyboard to circuit cards A12 Matrix A and A13 Matrix B in the control unit. Three additional pushbuttons (RESTART, STOP, and CONTINUE) simulate functions of the Processor front panel. These signals are transferred from the keyboard to the A15 Function card in the Control Unit.

Lever switches RUN/STEP (S2) and SINGLE/REPEAT (S3) transfer ground level STEP and REPEAT signals to the A16 Switch Register card when placed in the $\overline{\text{STEP}}$ and $\overline{\text{REPEAT}}$ positions, respectively. Keyboard panel indicator lights (DS1-DS10) signifying block size of 64, 128, 256, 512, 1024, 2048, 4096 plus READY, BUSY, and WHAT? indications are activated by corresponding signals from the A17 Buffer card.

ADC/CONTROL UNIT INTERFACE

The 5466B Analog-to-Digital Converter transfers nine signals, representing its front-panel switch settings, to the 5475A Control Unit's A16 Switch Register Card; these signals are "CC1", "CC2", "S1", "S2", "X2", "X5", "$\overline{\text{DF}}$", and "EO". An additional 25 signals are transferred between the ADC and the Processor, passing from J15 directly through the 5475A to J12. For 5451C, the remote programming signals are connected via 5475A connectors J23 and J21.

CONTROL UNIT CIRCUIT CARDS

A16 Switch Register Assembly (05475-60041)

The switch register is inserted to provide continuity from the ADC and Control Unit keyboard to the microcircuit I/O card in the Processor. All functions are straight wired through A16, except for the RESTART IN signal.

A15 Function Assembly (05475-60012)

The function card is used to generate a STOP OUT or CONTINUE OUT under control of the Control Unit keyboard and provide a POW ON signal to A14 each time power is turned on. The $\overline{\text{FOURIER}}$ signal is used to enable the STOP OUT and CONTINUE OUT flip-flops.

A17 Buffer Assembly (05475-60199)

The buffer card contains 11 lamp drivers. The lamp drivers accept block size inputs ($\overline{\text{BS1}}$ $\overline{64}$-$\overline{4096}$) for output to connector J16 to light the block size indicators on the keyboard panel. The block size inputs are also routed from connector J12 to J15 to permit Processor control of block size dependent sample values in the ADC (refer to Table 2-14). A ground-level $\overline{\text{RDY I}}$ input signal results in a high level RDY O signals to light the keyboard panel READY light (DS9). A high-level RDY I input signal results in a high-level BUSY O signal to light the keyboard BUSY indicator (DS8). A high level STOP OUT signal from the A15 Function card results in a high-level STOP LIGHT signal, which in turn is jumpered to the RDY O signal. This causes the READY indicator to light after the STOP button is depressed to interrupt a program. A ground level $\overline{\text{WHAT}}$ I input signal results in a high-level WHAT O output signal to light the keyboard WHAT? indicator.

A12 Matrix A Assembly (05475-60045)

The matrix A card contains 29 diode arrays, with a possible 15 diodes in each array. The number and placement of diodes in each array is arranged to coincide with a specific code for two ASCII characters. Thus, an active ground-level input from a keyboard pushbutton over one of the 29 input lines activates a particular array and results in a ground-level coded output on the 15 signal lines $\overline{\text{M1}}$ through $\overline{\text{M15}}$ (two 7-bit ASCII words plus a start bit in parallel).

A13 Matrix B Assembly (05475-60046)

The matrix B card functions as an extension of the matrix A card, by accepting the remaining 31 keyboard input lines to encompass a total of 60 keyboard pushbuttons (excepting the 3 command pushbuttons sensed by the function card). The combination of matrix A and B constitutes 60 different vertical diode arrays. Fifteen horizontal lines divide the vertical arrays into 15 segments. The presence or absence of a diode in each segment (diode connecting vertical and horizontal line) determines the ASCII format for each vertical array. A ground input applied to a vertical line pulls down the diodes in the array and results in ground-level outputs on those horizontal lines connected to a diode. Each of the 60 different ASCII combinations on the 15 output lines $\overline{M1}$ through $\overline{M15}$ is sensed as a unique character by the A14 Shift Register.

A14 Shift Register (05475-60204)

The shift register card accepts the parallel ASCII double-character (representative of a Control Unit keyboard pushbutton) on input lines $\overline{M1}$ through $\overline{M15}$. The character is shifted through a 20-bit register and output serially on the TTY DATA OUT line to the Processor via connector J14. An active FOURIER signal from the keyboard enables the data shift. The data is clocked out at a 110 Hz rate by an internal oscillator, or at a higher rate, if clocked by a faster external terminal. The oscillator is enabled each time a data character enters the register and is disabled when the register is empty of information. ASCII character signals are accepted on the TTY DATA IN line and also transferred on the TTY DATA OUT line to the Processor.

The shift register contains logic to eliminate pushbutton contact bounce, and to prevent redundant or simultaneous keyboard inputs. The read-only-memory enable (ROM ENAB) signal provides a -5V level to energize the matrix diodes when a pushbutton is depressed. This permits transfer of the character through matrix A and B to the shift register. The POW ON signal from the function card assures that the logic circuits are set to the proper state upon system turn-on.

A18 Relay Board (05475-60010)

The relay and crowbar card contains a relay circuit to switch +12V on the TTY DATA IN line when the +12V sense line is opened. Opening of the sense line indicates that a display terminal is not connected to the system; placing +12V on the TTY DATA IN line assures that the Control Unit keyboard data can be transferred through the A14 Shift Register on the TTY DATA OUT line. (Display Terminal when connected supplies a nominal +12V through J13 pin 4). The crowbar circuit protects the +5V supply against overvoltage damage to the integrated circuits.

Power Supply Circuit (A1, A2, A3, A4, A5, A6)

The power supply (see Figure 2-14 is enclosed in the rear of the Control Unit cabinet and consists of the T1 transformer, a rectifier board (A1), and a motherboard (A3) with four plug-in cards (A2 and A4 through A6). The power supply generates plus and minus 24 volts, plus and minus 12 volts, and plus and minus 5 volts for distribution throughout the system. The supply voltages are provided through the rear panel connector J18 DISPLAY for distribution to the display subsystem and through connector J17 POWER SUPPLY for external distribution. Protection circuits are included to prevent damage to the instrument. In case of a voltage short to ground or another voltage, the OVERLOAD lamp DS2 on the rear panel of the Control Unit lights.

5460A DISPLAY UNIT

The 5460A Display Unit accepts 16-bit data words through the Processor interface card and displays the information in analog and digital form. The XY information is converted to analog for display on the system oscilloscope. Digital information is displayed on the 5460A front panel Nixie tubes and indicator lights. Front panel switches control various modes of display on the oscilloscope.

DISPLAY UNIT INTERFACE AND CONNECTORS

The 5460A Display Unit plugs into the right side of the H51-180D Oscilloscope Mainframe. Three rear panel connectors (P1, P3, P4) are aligned with three mating connectors (J1, J3, J4) at the rear of the mainframe. A fourth connector (P2) consists of a sliding PC contact on the upper left cabinet rail and mates with a spring contact (J2). This connector supplies a high voltage output to the oscilloscope vertical deflection plates. P1 consists of a 32-pin male ribbon connector that interfaces with the oscilloscope. P3 and P4 consist of 50-pin female ribbon connectors. P3 interfaces with the power supply and X-Y plotter device. P4 interfaces with the Processor. See Figure 2-17 Wiring Diagram, for Display Unit interconnection with the system.

DATA TRANSFER SEQUENCE

The display unit accepts and processes one processor word (16 bits) at a time. The first two words in a data sequence always contain information for the front panel incandescent and Nixie displays. The second two words (and subsequent pair of words) normally alternate one word of horizontal (X) data and one word of vertical (Y) data for the oscilloscope display. This transfer of XY data is continued until complete or interrupted by changing the front panel switch settings. See Figure 2-15, Operation Flow Diagram, during the ensuing discussion.

Data Word 1

If the data ready flag ($\overline{\text{DAR}}$ signal) in the Display Unit is active, a data transfer sequence is initiated with an encode command ($\overline{\text{EN}}$ signal) from the Processor. The $\overline{\text{DAR}}$ flag is cleared and $\overline{\text{BIT 0}}$ of the first word is examined. $\overline{\text{BIT 0}}$ is low for the first data word and high for all subsequent words in a sequence. (The low level signal is the active level for Processor interface cards and system devices.) $\overline{\text{Bit 0}}$ set low causes the data word counter to be cleared (set to 0) upon receipt of the first word (see Figure 2-15, column 2). The remainder of word 1 contains part of the information required for the front panel display and is stored. A delay of 35 microseconds is encountered between each word time to allow processing of the CRT beam. If the DISPLAY FUNCTION SWITCH is set to PLOT, signifying external plotter operation, the display unit will lock up until the switch is placed at ARM. At this point the unblanking circuit is cleared (not significant until the third and fourth words when the CRT beam is turned on). The settings of the HORIZONTAL ORIGIN, VERTICAL MODE, VERTICAL POLAR ANG/DIV, and VERTICAL SCALE switches are clocked into the Processor interface card when the data ready flag is set. Setting the data ready flag indicates completion of the first cycle and readiness to accept the second word.

Data Word 2

In the second word of the data transfer sequence (and all other words until the start of a new sequence) $\overline{\text{BIT 0}}$ is high. The balance of the front panel display information is in bits 1 through 15 of the second word. The encode command precedes the second word and causes the data ready flag to be reset during processing of the second word. Since $\overline{\text{BIT 0}}$ of the second word is high and the data word counter was set to 0 for data word 1, the data word counter now advances to 1 (see Figure 2-15, column 3). Data word 2 is received and stored, completing the information needed for the front panel displays. After a 35-microsecond delay, the unblanking circuit is cleared (neither function applicable to first two words), the front panel switches are again clocked in. The data ready flag is then set preparatory to receiving the next word.

Data Word 3

The third word in a data transfer sequence contains horizontal or X data for the oscilloscope (or plotter) display. An encode command precedes data word 3 and the data ready flag is cleared. $\overline{\text{BIT 0}}$ is high and with the data word counter left at a count of 1, internal logic advances the data word counter to 2 (see Figure 2-15, column 4). Bits 5 through 15 of the third word contain the X data and are temporarily stored. If the DISPLAY TYPE switch is set to CONT (X and Y data to be shown continuous) the X data remains stored until the following word containing Y data is received. With DISPLAY TYPE switch in any other position, the X data is transferred to the horizontal digital-to-analog converter. This transfer allows the X data to be positioned on the screen during the 35-microsecond delay. The beam is not turned on until the Y data in the next word completes the display; however, the unblanking circuit is cleared nonetheless. Front panel switch settings are again transferred to the Processor, and the data ready flag is set for the receipt of the next word.

Data Word 4

The fourth word in a data transfer sequence contains vertical or Y data for the oscilloscope display. An encode command precedes arrival of the word and clears the data ready flag. $\overline{\text{BIT 0}}$ is high and with the data word counter left at 2, the counter is advanced to 3 (see Figure 2-15, column 5). Data word 4 contains Y data in bits 5 through 15. These bits are not stored but sent directly to the vertical digital-to-analog (D/A) converter.

If the DISPLAY TYPE switch is set to CONT, the X data in the previous word is now transferred from word storage to the horizontal D/A converter. When the CRT beam is turned on, both X and Y information are displayed in continuous fashion during the 35-microsecond delay.

If the DISPLAY TYPE switch is set to POINT, a 25-microsecond delay is encountered before the beam is turned on, permitting the Y data to be positioned (X data positioned in previous cycle). The beam remains on for 10 microseconds to illuminate the X-Y point position.

If the VERTICAL MODE switch is set to COMPLEX, the X and Y data is displayed as described in the previous paragraph. This switch setting also overrides DISPLAY TYPE set to BAR position. If the switch is not set to COMPLEX, (and DISPLAY TYPE is not set to CONT or POINT) the BAR mode is indicated and the beam is turned on prior to the 35-microsecond delay. With input of subsequent Y data words, a vertical bar will be displayed (during the 35-microsecond delay after beam turn-on) from the mid-screen X position upward (or downward) to the Y position. In this mode the dot is reset each cycle to the midposition for the next bar display. After the Y data has been displayed on the oscilloscope, the unblanking circuit is cleared to turn off the beam.

For systems having the analog plotter option, during display, the position of the DISPLAY FUNCTION switch is tested. If the switch is in the PLOT position (after initially having been thrown to ARM), the word transfer sequence must wait until a completed plot signal (CP) is received from the external plotter accessory. After this pulse is received, signifying end of plotter arm movement, the front panel switch settings are sent to the computer as in previous word operation and the data ready flag is set.

Subsequent Data Words

Data transfer normally continues in word pairs alternating X and Y information until the display information is complete. Referring to Figure 2-15, top row, a data word subsequent to the fourth word ($\overline{\text{BIT}}$ 0 high) will decrement the data word counter from 3 to 2. This results in the processing of this data word for X information in a manner identical to data word 3. Similarly, the next data word ($\overline{\text{BIT 0}}$ high and Y information in the remaining bits) advances the data word counter to 3 and is processed for Y data identical to data word 4. This alternating sequence continues until all X and Y data are displayed as required. Each new data sequence begins with data words 1 and 2 containing new front panel display information and BIT 0 low in word 1.

Z Data Bits

Data words 3 and 4 also contain a provision to convey Z-axis information for modulating the intensity of the CRT beam under program direction. This type of control is required for modal application only.

DISPLAY UNIT CIRCUIT CARDS

The display unit contains nine printed circuit cards, mounted with discrete components and integrated circuits, that accomplish the display logic and control functions. The circuit card input/output functions are discussed in the following paragraphs. Refer to Figure 2-16 and 2-17 during the discussion. Signal names with a bar (e.g., $\overline{DAR}$) indicate that the active state of the signal is at ground level.

A1 Vertical Amplifiers Assembly (05460-60001)

The A1 Card converts the Y-axis -2.0 to +2.0V output of the A2 Vertical DAC (via VERTICAL GAIN control R2) to +30 to +100V to drive the CRT deflection plates. The BEAM signal represents the input from the FIND BEAM switch (S102 via P1) on the oscilloscope. The VOUTA+ signal originates from the front panel GAIN control (R2) and the VPOSN1,2,3 signals originate from the POSITION control (R1). The VSIGP and VSIGM signals represent the output voltage to the vertical deflection plates in the oscilloscope (via P2).

A2 Vertical DAC Assembly (05460-60002)

The A2 card accepts vertical or Y-axis information in digital form and converts the binary value into an equivalent analog signal (VOUT 1+) for output to the A1 Vertical Amplifier (via R2) and A5 Control. Similar signals VOUT 2+ and PLOTY+ convey the analog Y information to connectors P4 (for external output). and to P3 (for plotter output). Vertical information is received in digital form from the Processor via P4 over lines BIT 5 through BIT 15. The V LOAD input signal from A5 Control clocks the binary information into storage elements on the A2 card. The MID signal from A5 forces the vertical display to mid-scale after each point has been displayed in the DISPLAY TYPE BAR mode. Switch (S8) inputs DCORG, DCMFS, DCPFS represent switch positions DISPLAY CALIBRATE ORIGIN, DISPLAY CALIBRATE MINUS FULL SCALE, and DISPLAY CALIBRATE PLUS FULL SCALE respectively.

A3 Horizontal DAC Assembly (05460-60002)

The A3 card accepts horizontal or X-axis information in digital form and converts the binary value into an equivalent analog signal (HSIG+, HSIGE+, PLOTX+) for respective output to connectors P1 (oscilloscope), P4 (external BNC) and P3 (plotter). Horizontal information is received in digital form over bit lines XDT0 through XDT10 from word storage in the A4 card. The same information is initially input to the A4 card over lines BIT 5 through BIT 15 from the Processor. The HLOAD signal from A5 Control clocks the bits into A3 storage elements. Switch (S8) positions DCORG, DCMFS, and DCPFS apply equally to the horizontal information as referenced in the preceding paragraph for vertical data. Also applicable are switch (S4) positions representing HORIZONTAL SWEEP LENGTHS per centimeter of 12.8 (HS.8), 10.24 (HS.24), and 10 (HS10). With the VERTICAL MODE switch (S1) to COMPLEX, the HS8.0 signal is active, representing a horizontal sweep length of 8.0 centimeters.

A4 Word Storage Assembly (05460-60003)

The A4 card maintains a count of the incoming data words from the Processor, and directs the storage and distribution of the words according to the type of information involved. A data word counter on the A4 card counts the incoming words in a data transfer sequence (0-1-2-3, 2-3, 2-3, etc.) and outputs signals to A5 Control and A8 Nixie Display representative of the word counter sequence (DWCO through DWC3). The data words are received in binary format over digital lines BIT 0 through BIT 15. Each word is preceded by an encode (EN) command from the Processor that is recognized by A4 logic. Depending upon which data word counter signal (DWC0-DWC3) is active, the word is accepted by A3 Horizontal DAC (XDT0 through XDT10), A2 Vertical DAC (Bit 5 through BIT 15), A8 Display (BIT 1 through BIT 10), or A9 Light

Driver cards. Signals to A9 consist of decoded bits representing front panel incandescent lamp functions: Scale Factor Sign (SFS), Frequency (FREQ), Logarithmic (LOG) that also lights decibel (dB), Polar (PLAR), Rectangular (RECT) display, and scale factor multipliers ONE, TWO, FIVE (that also light X10). Signals to A5 Control consist of word counter outputs DWC0, DWC2, DWC3, a pulse from the encode signal (ENN), and Z-axis bit lines ZDT1 through ZDT5 (Z-axis not used in present configuration). Data word counter outputs (DWC0, DWC1) are also sent to A8 LED Display. Refer to Tble 2-11, Word Format, for bit configuration of each word.

Table 2-11. Data Word Format

BITS	Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12	13	14	15
DATA WORD 1	1	POLAR (Ø = RECT)	LOG & dB	FREQ	8 Units	—	—	8 Tens	—	—	8 Hund.	—	—	—	—	SFS
DATA WORD 2	Ø	1 Units	2 Units	4 Units	1 Tens	2 Tens	4 Tens	1 Hund.	2 Hund.	4 Hund.	—	—	—	No. "1"	No. "2"	No. "5"
DATA WORD 3	Ø	ZDT5	—	—	—	XDTØ	XDT1	XDT2	XDT3	XDT4	XDT5	XDT6	XDT7	XDT8	XDT9	XDT1Ø
DATA WORD 4	Ø	ZDT1	ZDT2	ZDT3	ZDT4	YDTØ	YDT1	YDT2	YDT3	YDT4	YDT5	YDT6	YDT7	YDT8	YDT9	YDT1Ø

A5 Control Assembly (05460-60004)

The A5 card contains timing and control logic to provide overall coordination of the front panel and oscilloscope displays. The DWC0 signal starts a marker clock on the A5 card; every eighth point or every thirty-second point is intensified according to HORIZONTAL MARKER switch (S6) setting 8 PT (HM8) or 32 PT (HM32). The DWC2 signal identifies the third or horizontal data word and enables the H LOAD clock signal to the A3 Horizontal DAC. The DWC3 signal identifies the fourth or vertical data word and enables the V LOAD clock signal to the A2 Vertical DAC. The MID signal sets the vertical DAC output to mid-scale when the DISPLAY TYPE switch (S9) is set to BAR (and VERTICAL MODE is not set to COMPLEX nor VERTICAL DISPLAY set to PLOT). These switch settings are determined in A5 logic circuits by switch inputs DTPNT, DTCNT, DFPLT, and VDMP2. The ENN signal from A4 Control represents an incoming Processor encode command that clears the data ready flag (DAR) and triggers a delay circuit to set the data ready flag again after 35 microseconds. An unblanking circuit on A5 is activated by each DWC3 and sends a BLANK signal to P1 for unblanking the oscilloscope and an EBLANK+ signal to P4 for external unblanking. DWC3 can occur every other word when only X and Y data is being transferred.

When an X-Y plotter device is used, DISPLAY FUNCTION switch (S7) provides an active DFPLT signal. With the ARM/PLOT switch (S11) to ARM an inactive PLOT 1 signal is applied to A5, inhibiting the DAR signal after the fourth word and causing the plotter arm to stop after the first point has been plotted. Placing the ARM/PLOT switch to PLOT provides an active PLOT1 signal that inhibits DAR after the first word, causing the plotter to stop after the last point has been plotted. Setting or resetting DAR also enables or disables the PLOT signal to A7 Plotter Control. Receipt of a complete plot pulse (CPP) from A7 sets DAR after the final fourth word. The PEN 1 or Pen 2 relay signal is active to control pen lift when PLOT 1 signal is active and DWC0 is inactive. The Z-AXIS signal provides a variable analog voltage output for modulating intensity of the CRT beam. An amplifier circuit on the A5 card controls Z-axis modulation by monitoring the rate of change of the A5 Vertical DAC output (VOUT 2+) with respect to time. This results in a stable intensity level regardless of length traveled. A digital-to-analog converter is included on the A5 card to accept digital information on ZDT1 through ZDT5 lines for Z-axis modulation; however, this form of Z-axis control is used only in modal applications.

A6 Reference Power Supply Assembly (05460-60005)

The A6 card uses the +15V supply voltage from P1 to produce a stable +10V reference output for the A2 Vertical DAC and A3 Horizontal DAC cards. The +5V input from P3 and -12.6V input from P1 are not connected.

A7 Plotter Control Board (05460-60020) (Available as an accessory for use with an X-Y plotter)

The A7 card controls an external X-Y plotting device by providing an enabling signal (SEEK) to P3 in response to an input signal (PLOT) from A5. Plot rate is controlled by the RATE X input from the PLOT RATE switch (S10) when rotated from EXT to 20. A completed plot signal (CP) from the plotter (via P3) is relayed to A5 control as the completed plot pulse (CPP).

A8 Display Assembly (05460-60006)

The A8 card controls display of the front panel incandescent and LED's lights. Input lines BIT 1 through BIT 10 transfer binary numbers during data words 1 and 2. The DWC0 signal clocks in the most significant bits and DWC1 clocks in the least significant bits. This binary information is converted to BCD format and displayed on LED's D57, D58, D59 at the end of word 2. Nine incandescent indicators are driven by the A9 Light Driver to display functional mode (as shown in Figure 2-17). The +170V supply voltage for the numerical Nixie tubes and minus-sign neon tube is also supplied from the A9 card. The incandescent lamps are driven with +5V from P3.

A9 Light Driver Assembly (05460-60007)

The A9 card converts incoming control signals from low voltage logic levels to levels sufficient to drive the front panel incandescent lamps.

Table 2-12. List of Mnemonics: Fourier Analyzer System

SIGNAL	DEFINITION
$\overline{A1}$, $\overline{A2}$, $\overline{A3}$	OVERLOAD VOLTAGE selector codes that indicate the input voltage position of the Channel A OVERLOAD VOLTAGE switch, S6.
ADJ1, ADJ3, ADJ4	Trigger level adjustment resistor R1 on S11.
$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	Code bits for Channel B input OVERLOAD VOLTAGE switch, S7, indicating setting of that switch.
$\overline{BEAM}$	FIND BEAM input from Oscilloscope mainframe.
$\overline{BIT\ 0}$—$\overline{11}$	Ten-bit or twelve-bit digital word defining amplitude of analog input signal. Refer to the data bus signals for A, B, C, and D inputs.
$\overline{BIT\ 0}$—$\overline{15}$	Sixteen-bit digital word defining display information from Processor to Display Unit.
BLANK	Unblanking signal to system oscilloscope from Display Unit's Control Card, A5.
BSO64—BSO4096 (See N6—N12)	Signals to light BLOCK SIZE indication on Control Unit keyboard, and input block size to ADC.
BUSY0	Signal to light BUSY indicator on Control Unit's keyboard.
$\overline{C1}$, $\overline{C2}$, $\overline{C3}$	Code bits for Channel C OVERLOAD VOLTAGE switch, S9, indicating setting of that switch.
CC1, CC2	Code to indicate the position of input switch S4 or S5, which selects how many channels of analog data are to be analyzed.
CHA, CHB, CHC, CHD	Analog input signals to the input boards.
CHECK	Pulse (approximately 51 mV, 110 ns wide) from Trigger Board Assembly. Serves as input test signal to ADC input channels.
CONT IN	Continue signal from keyboard to A15 (Function Generator) in Control Unit.
CONT OUT	Continue signal from A15 (Function Generator) to A16 (Switch Register) in Control Unit.
CP	Completed Plot signal from plotter to A7 (Plotter Control) in Display Unit.
CPP	Completed Plot Pulse from A7 (Plotter Control) to A5 (Control) in Display Unit.
$\overline{D1}$, $\overline{D2}$, $\overline{D3}$	Code bits for Channel D OVERLOAD VOLTAGE switch, S10, indicating setting of that switch.
$\overline{DAR}$ (ADC)	Data Ready signal, from ADC to Processor. Indicates data is ready to be transferred to Processor.
$\overline{DAREN0}$, $\overline{DAREN1}$	Signals generated, but not used, by ADC.
$\overline{DAR}$ DISP KEY	Signal from Display Unit to Processor to indicate readiness to accept data word from Processor for Display.
$\overline{DCMFS}$	DISPLAY CALIBRATE MINUS FULL SCALE switch position (S8) to A2 Vertical DAC.
$\overline{DCORG}$	DISPLAY CALIBRATE ORIGIN switch position (S8) on Display Unit to A2 Vertical DAC.

Table 2-12. List of Mnemonics: Fourier Analyzer System (continued)

SIGNAL	DEFINITION
$\overline{\text{DCPFS}}$	DISPLAY CALIBRATE PLUS FULL SCALE switch position (S8) on Display Unit to A2 Vertical DAC.
$\overline{\text{DFPLT}}$	"Low" level indicates DISPLAY FUNCTION switch S7 on Display Unit is in PLOT position.
DISP1, DISP2	Signals indicate position of the ADC DISPLAY switch. The channel selected for DISPLAY (A, B, C, or D) has bit "12" set for that ADC data word. Switch code is gated with OTA, OTB, OTC, or OTD, as selected on the A1Ø Sample Generator board in the ADC.
DISPCT	Indicates that the digital word being put onto the data bus should be displayed.
DONE A, DONE B, DONE C, DONE D	Indicate that the analog-to-digital conversion in the indicated channel has been completed.
$\overline{\text{DSBL}}$	Provides an enable/disable signal from the DISPLAY FUNCTION switch on the Display Unit to the external X-Y Plotter.
$\overline{\text{DF}}$	Indicates whether the SAMPLE MODE switch, S3, is in its "ΔFREQ" or "ΔTIME" position.
$\overline{\text{DTCNT}}$	"Low" level indicates DISPLAY TYPE switch (S9) on Display Unit is in its CONTinuous position.
$\overline{\text{DTPNT}}$	"Low" level indicates DISPLAY TYPE switch (S9) on Display Unit is in its POINT position.
$\overline{\text{DWCØ}}$—$\overline{\text{DWC3}}$	Contents of word counter on A4 board in Display Unit. If bit "15" of a data word sent to the Display Unit is set, the Data Word Counter is reset, indicating the first word of the display.
E BLANK+, E BLANK–, (GND)	Unblanking signals from A5 (Control) in Display Unit to external oscilloscope.
$\overline{\text{EN}}$	Encode signal from Processor to ADC or Display Unit to start processing input signals.
ENAB	Indicates that triggering conditions have been satisfied in "external" sample mode.
ENN	Display Unit's internal "encode" signal.
ENN	ADC internal "on/off" signal.
$\overline{\text{EO}}$	SAMPLE MODE switch (S2) positions which enable "÷1ØØØ" on A1Ø Sample Generator Board. EO = "low" in Hz/ms ($\Delta t/F_{max}$) and in the HMz/s (ΔF/TOTAL TIME).
$\overline{\text{EXPNT}}$	Signal indicates command from Processor to light "X1Ø" indicator on Display Unit.
EXT SAMP	External Sample input from J1 to the ADC.
FIVE, $\overline{\text{FIVEX}}$	Signal indicates decoder command from Processor to light "5" indicator on Display Unit.
$\overline{\text{FOURIER}}$	"Low" level signal indicates system is operating as a Fourier Analyzer System.
FREE	Indicates that TRIGGER MODE switch, S6, is in FREE RUN position.
FREQ, $\overline{\text{FREQX}}$	Signal indicates decoded command from Processor to light "FREQ" indicator on Display Unit.

Table 2-12. List of Mnemonics: Fourier Analyzer System (continued)

SIGNAL	DEFINITION
GAIN1, GAIN2, GAIN3	Signals indicate input OVERLOAD VOLTAGE switch setting of the digital word being put onto the data bus.
HLOAD	Clocks horizontal bits into A3 storage elements in Display Unit.
$\overline{\text{HM8}}$	"Low" level indicates HORIZONTAL MARKER switch (S6) on Display Unit is in the "8 PT" position, or "32 PT" position, and intensifies 8th or 32nd point on Oscilloscope display.
$\overline{\text{HOCTR}}$	Notifies Processor that HORIZONTAL ORIGIN switch (S5) on Display Unit is in the "CENTER" position, and display is to start at that point.
HOLD	Causes the sample-and-hold amplifier to disconnect from input signal and hold result on a capacitor.
$\overline{\text{HOLFT}}$	Notifies the Processor that the HORIZONTAL ORIGIN switch (S5) on Display Unit is in the "LEFT" position, and display is to start at that point.
$\overline{\text{HOLOG}}$	Notifies the Processor that the HORIZONTAL ORIGIN switch (S5) is in the LOG position, and horizontal display is to be logarithmic.
HSIG+, HSIG– (GND)	Horizontal output voltage from A3 (Horizontal DAC) in Display Unit to the system oscilloscope.
HSIGE+, HSIGE– (GND)	Horizontal output voltage from A3 (Horizontal DAC) in Display Unit to the external oscilloscope.
$\overline{\text{HSSHLD}}$	Ground connection for VERTICAL MODE switch (S1) on Display Unit.
HS8.Ø	"Low" level indicates Display Unit's VERTICAL MODE switch (S1) is in its "COMPLEX" position, and adjusts DAC gain for 8-cm sweep.
$\overline{\text{HS.8}}$, $\overline{\text{HS1Ø}}$, $\overline{\text{HS.24}}$	"Low" level indicates Display Unit's HORIZONTAL SWEEP LENGTH switch (S4) is in its "12.8", "1Ø", or "1Ø.24" position (respectively), and adjusts Horizontal DAC gain. Also indicates VERTICAL MODE switch (S1) is not in its "COMPLEX" position.
INA, INB, INC, IND	Analog output signals from input board to digitizer board, in ADC.
LINE+, LINE– (GND)	Line Frequency source from Control unit to ADC clock generator.
$\overline{\text{LINE}}$	Input from Trigger Mode switch, S8.
LOG, $\overline{\text{LOGX}}$	Signal indicates decoded command from Processor to light the "LOG" and "dB" indicators on the Display Unit.
$\overline{\text{MID}}$	Signal from A5 (Control) in Display Unit for centering oscilloscope beaming bar display mode.
$\overline{\text{M1}}$—$\overline{\text{M15}}$	Outputs from the diode matrices to define the necessary ASCII characters for sixty Control Unit keyboard pushbuttons.
$\overline{\text{N6}}$—$\overline{\text{N12}}$	Seven signals used to indicate Block Size selected ("64" to "4Ø96" words in binary increments). Same as BSO64-BSO4Ø96.
$\overline{\text{NEXT}}$, $\overline{\text{NEXT1}}$	Signals generated, but not used, by ADC.

Table 2-12. List of Mnemonics: Fourier Analyzer System (continued)

SIGNAL	DEFINITION
ONE, $\overline{\text{ONEX}}$	Signal indicates decoded command from Processor to light the "1" indicator on the Display Unit.
OTA, OTB, OTC, OTD	Serve to output the digital data associated with the particular channel onto the data bus.
OTEN	Indicates that data is being enabled onto the data bus.
OVOLT	Signal which drives the OVERLOAD VOLTAGE indicator, DS2.
OVT	Signal sent to J16, indicating OVERLOAD VOLTAGE condition.
PEN1, PEN2 (GND)	Provides pen control from A5 (Control) in Display Unit to Plotter during "plot" mode.
$\overline{\text{PLAR}}$, $\overline{\text{PLARX}}$	Indicates decoded command from Processor to light "POLAR" indicator on Display Unit.
PLOT X+, PLOT X–	Horizontal output voltage from A3 (Horizontal DAC) in Display Unit to the Plotter.
PLOT Y+, PLOT Y–	Vertical output voltage from A2 (Vertical DAC) in Display Unit to the Plotter.
POW ON	Used to reset A14 (Shift Register) in Control Unit when power is first applied.
$\overline{\text{PTRIG}}$	Input from TRIGGER SLOPE switch, S11.
RATEX	Input to A7 (Plotter Control) in Display Unit to determine plotting frequency.
RECT, $\overline{\text{RECTX}}$	Signal indicates decoded command from the Processor to light the "RECT" indicator on the Display Unit.
REMOTE	Indicates that the SAMPLE MODE switch (S2) is in its "REMOTE" position. Allows wired-OR signals from the remote control I/O card to control OVERLOAD VOLTAGE switch settings and SAMPLE MODE switch settings.
$\overline{\text{REPEAT}}$/(SINGLE)	"Low" level indicates that the REPEAT/SINGLE switch on the Control Unit's keyboard is in its "REPEAT" position. "High" level indicates the "SINGLE" position. Position information is routed to the Processor.
RESTART	Command from Control Unit's keyboard to restart the Fourier program.
RESTART IN	Interrupt command from Control Unit's keyboard through A15 and A16 to the Processor.
$\overline{\text{RDY}}$Ø	Lights "READY" indicator on Control Unit.
ROM ENAB	Read-only memory enable line from A14 (Shift Register) in Control Unit. Provides constant negative voltage to energize matrix diodes.
$\overline{\text{RUN}}$	ADC signal from AIØ Board indicating that trigger conditions have been satisfied.
$\overline{\text{S1}}$, $\overline{\text{S2}}$	With X2 and X5, indicate position of MULTIPLIER switch S3 (see *Table 3-2*).
SAMP	Output of Sample Generator, AIØ, which serves to initiate a-to-d conversions and data transfers.
SAMIN	Indicates whether the External clock switch, S1, is in its EXT or INT position.

Table 2-12. List of Mnemonics: Fourier Analyzer System (continued)

SIGNAL	DEFINITION
$\overline{\text{SAMPT}}$	Train of sample pulses from A10 (Sample Generator). Available at 5475A rear-panel BNC J21.
SEEK	Command from A7 (Plotter Control) in Display Unit enabling plotter to plot a specific point.
SFS, $\overline{\text{SFSX}}$	Signal indicates decoded command from the Processor to light the "-" indicator on the Display Unit.
$\overline{\text{START A}}$, $\overline{\text{START B}}$, $\overline{\text{START C}}$, $\overline{\text{START D}}$	Indicates digitizer is performing the analog-to-digital conversion on the indicated channel.
$\overline{\text{STEP}}$/(RUN)	"Low" level (STEP) causes program to proceed one step at a time. "High" level (RUN) causes program to proceed through steps automatically. From Control Unit keyboard switch position, to A16 (Switch Register) in Control Unit, to Processor.
STOP, STOP IN, STOP OUT	Keyboard command that relays a "halt" through the Control Unit to the Processor.
STOP LIGHT	Lights "READY" indicator on Control Unit's keyboard after STOP button has been pressed.
$\overline{\text{TRIG OUT}}$	Signal generated, but not used, by ADC.
TWO, $\overline{\text{TWOX}}$	Signal indicates decoded command from Processor to light "2" indicator on Display Unit.
UNCAL	Signal which drives the "UNCAL" LED, DS1. Derived on A7 (Error Board). Indicates that the selected combination of Block Size and SAMPLE CONTROL switch setting are beyond the range of the ADC.
$\overline{\text{VAS1}}$—$\overline{\text{VAS3}}$	Three-bit binary word defining position of VERTICAL POLAR ANG/DIV switch (S2) on Display Unit for Processor.
$\overline{\text{VDCMP1}}$	Notifies the Processor that the VERTICAL MODE switch (S1) on the Display Unit is in its "COMPLEX" position.
VDCMP2	Indicates to the Control Unit's A5 (Control) Board that the VERTICAL MODE switch is in its "COMPLEX" position.
$\overline{\text{VDI/P}}$	Notifies the Procesor that the VERTICAL MODE switch (S1) on the Control Unit is in the "IMAGINARY/PHASE" position.
$\overline{\text{VDR/M}}$	Notifies the Processor that the VERTICAL MODE switch (S1) on the Control Unit is in the "REAL/MAGNITUDE" position.
V LOAD	Vertical load signal to A2 (Vertical DAC) in Display Unit.
VOUT A+	Input to Display Unit A1 (Vertical Amplifier) from GAIN control.
VOUT 1+	Output from Display Unit A2 (Vertical DAC) to GAIN control.
VOUT 2+	Vertical voltage output from Display Unit A2 (Vertical DAC) to external oscilloscope.
VPOSN1—VPOSN3	Inputs to Display Unit A1 (Vertical Amplifier) from POSITION control.

Table 2-12. List of Mnemonics: Fourier Analyzer System (continued)

SIGNAL	DEFINITION
VSIGM, VSIGP	Output voltage to vertical deflection plates of system oscilloscope, from Display Unit A1 (Vertical Amplifier).
$\overline{VS1}$—$\overline{VS5}$	Five-bit binary word defining position of Display Unit's VERTICAL SCALE switch (S5) to Processor.
What Ø	Lights "WHAT?" indicator on Control Unit's keyboard.
$\overline{XDT0}$—$\overline{XDT10}$	Eleven-bit binary word defining horizontal display information to A3 (Horizontal DAC) in the Display Unit.
$\overline{X2}$, $\overline{X5}$	With S1 and S2, indicate position of MULTIPLIER switch S3 (see *Table 3-2*).
Z AXIS +, $\overline{ZDT1}$—$\overline{ZDT5}$	Z-axis CRT information (not used).

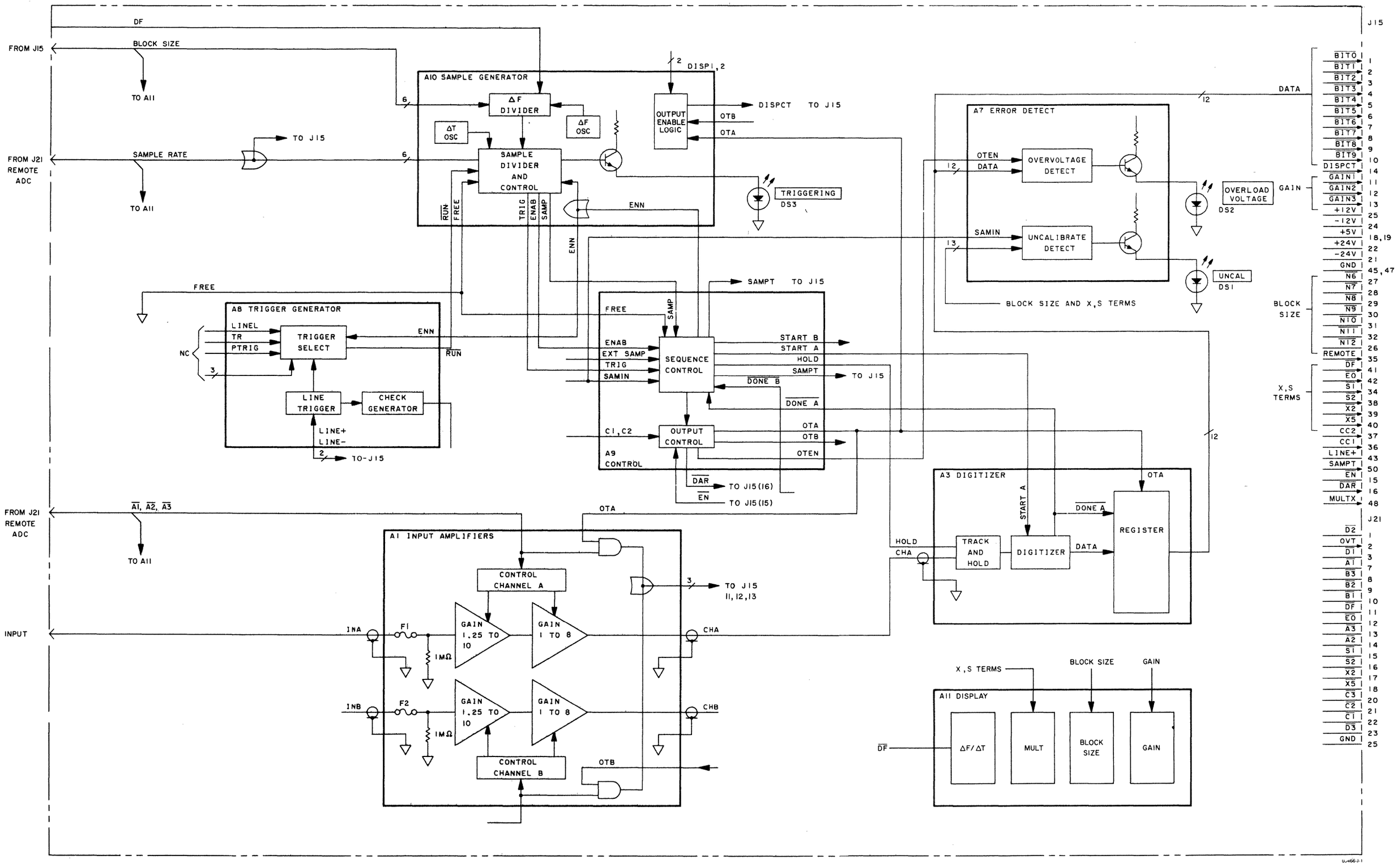


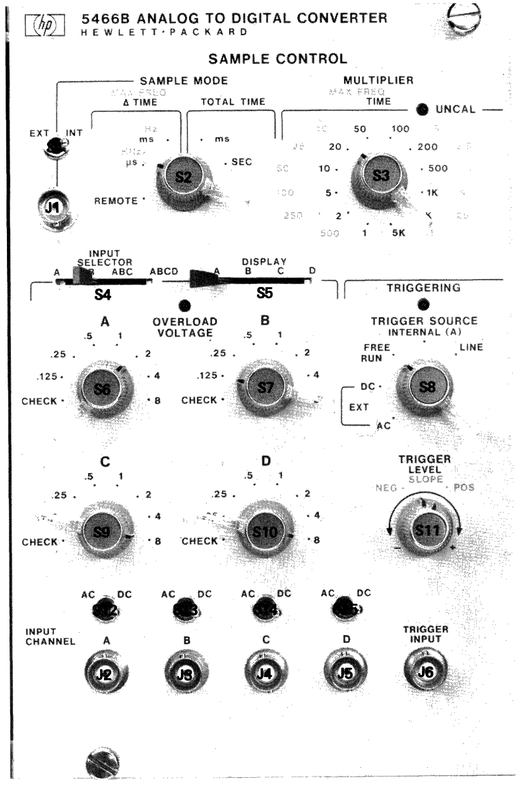
Figure 2-10
ADC FUNCTIONAL FLOW DIAGRAM
2-49

Table of Switches for Figure 2-11.

Switch/Mnemonic	Switch Position	Connected To
EXT/INT (S1)		
SAMIN	(2)	XA9(13)
SAMPLE CONTROL SAMPLE MODE (S2)		
REMOTE	AFR(11)	S3AFR(3), P15(35)
GND	AF(7)	ground
DF	AF(3)	XA7(B)
EO	AF(8)	XA7(K)
SAMPLE CONTROL MULTIPLIER (S3)		
GND	AF(2), AR(2), BF(2), BR(2)	REMOTE S2AF(2), AR(2)
X2	AF(9)	XA1Ø(6)
X5	AR(4)	XA1Ø(7)
S1	BF(8)	XA1Ø(3)
S2	BR(5)	XA1Ø(4)
INPUT (S4) (4 channel only)		
GND	AF(1, 2, 3, 1Ø, 11)	ground
CC1	AF(14)	XA9(21), J15(36)
CC2	AF(7)	XA9(2Ø), J15(37)
DISPLAY INPUT (2 channel) (S5)		
CC1	AF(5)	XA9(2)
DISP1	AF(3)	XA1Ø(J)
DISP2 (4 channel only)	AF(7)	XA1Ø(H)
A OVERLOAD VOLTAGE (S6)		
INPUT A	BR(1)	S12(1)
IN A	BF(3)	XA1(2Ø)
CHECK	B, FR(7)	XA8(15) [S9B, FR(7) 4 channel]
REMOTE	ARF(9)	S2AFR(11), S7AFR(9) [S9A, FR(9)]
GND	BF(2)	S7A, FR(9) [S7A, FR(9) 4 channel]
A1	AF(2, 3)	XA1(16) P21(7)
A2	AF(5)	XA1(15) P21(14)
A3	AR(6)	XA1(T)
B OVERLOAD VOLTAGE (S7)		
INPUT B	BR(1)	S14(2) [S13(2) 4 channel]
IN B	BFR(3)	XA1(4)
CHECK	BFR(7)	XA8(15), S6BFR(7)
REMOTE	AFR(9)	S2A, FR(11), S6AFR(9)
GND	BF(2)	S14(5), XA1(3)
B1	AF(2, 3)	XA1(9) P21(10)
B2	AF(5)	XA1(8) P21(9)
B3	AR(6)	XA1(K) P21(8)

Table of Switches for Figure 2-11 (continued)

Switch/Mnemonic	Switch Position	Connected To
TRIGGER SOURCE (S8)		
CHA	BR(1)	XA3(2Ø)
CHA	BR(7)	XA8(13)
TRIGGER INPUT	BR(3)	J6
FREE	AR(3)	XA9(P), XA1Ø(13)
GND	AR(4)	ground
LINE	AR(5)	XA8(S)
C OVERLOAD VOLTAGE (S9) (4 channel only)		
INPUT C	BR(1)	S14(2) [S6B, FR(7) S1ØB, FR (7)]
IN C	BFR(3)	XA2(2Ø)
CHECK	BFR(7)	XA8(15)
REMOTE	AFR(9)	S6AFR(9), S1ØAFR(9)
GND	BF(2)	J4, S14(5), ground
C1	AF(2, 3)	XA2(16) P21(22)
C2	AF(5)	XA2(15) P 21(21)
C3	AF(6)	XA2(T) P21(2Ø)
D OVERLOAD VOLTAGE (S1Ø) (4 channel ADC only)		
INPUT D	BR(1)	S15(2)
IN D	BR(3)	XA2(4)
CHECK	BFR(7)	XA8(15), S9BFR(7)
REMOTE	AFR(9)	S2A, FR(11), S9AFR(9)
GND	BF(2)	S14(5), XA2(13)
D1	AF(2, 3)	XA2(9) P21(3)
D2	AF(5)	XA2(8) P21(1)
D3	AR(6)	XA2(K) P21(23)
TRIGGER SLOPE (S11/R1)		
P TRIG	S11R(4)	XA8(T)
ADJ2	R1(1)	XA8(19)
ADJ3	R1(2)	XA8(X)
ADJ1	R1(3)	XA8(W)
AC/DC SELECTORS		
INA (AC)	S12(1)	S6BR(1)
A INPUT	S12(2)	J3
INA	S12(3)	S6BR(1)
INB (AC)	S13(1)	S7BR(1)
B INPUT	S13(2)	J4
INB	S13(3)	S7BR(1)
INC (AC)	S14(1)	S9BR(1)
C INPUT	S14(2)	J5
INC	S14(3)	S9BR(1)
IND (AC)	S15(1)	S1ØBR(1)
D INPUT	S15(2)	J6
IND	S15(3)	S1ØBR(1)



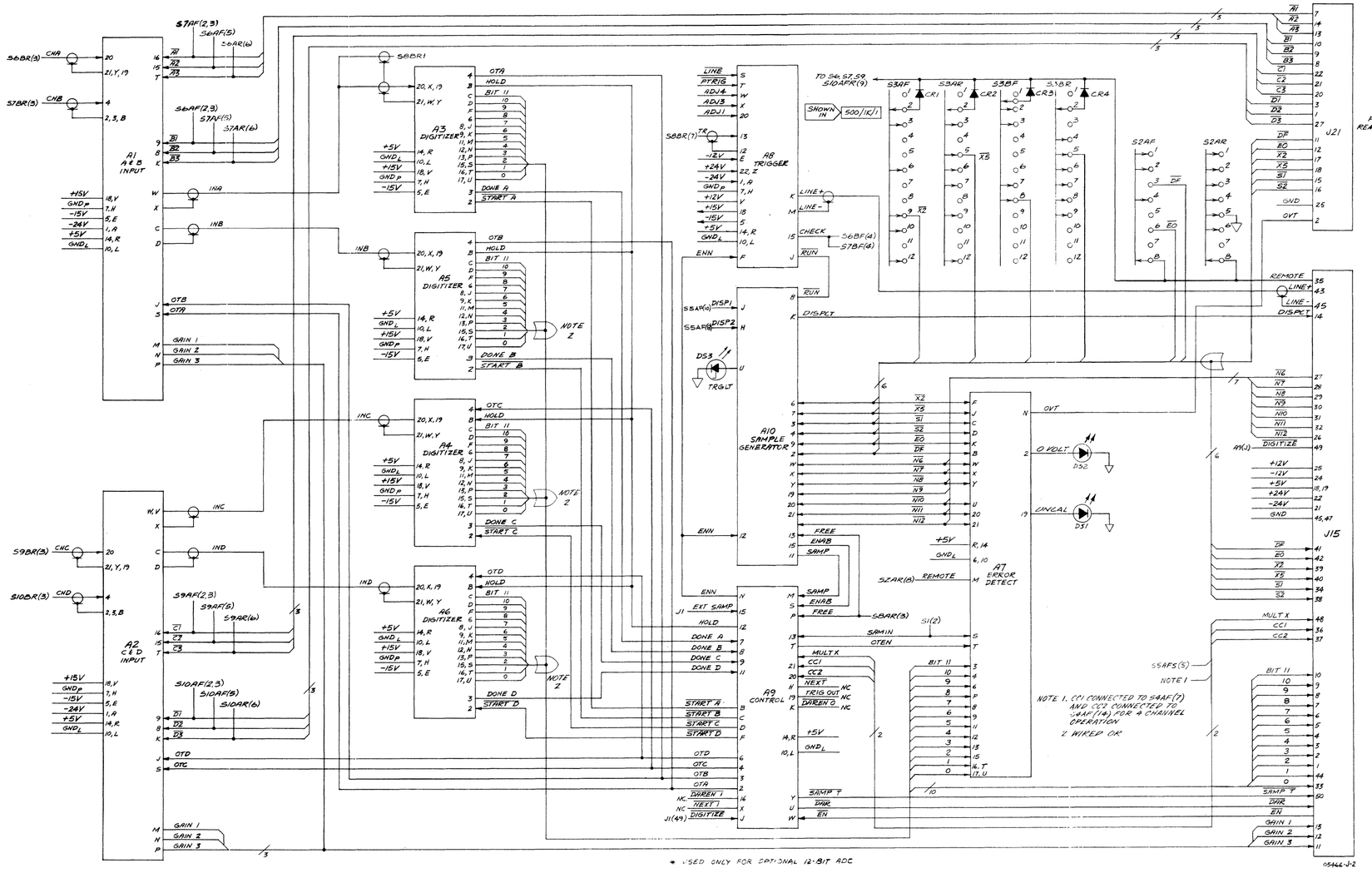


Figure 2-11
ADC WIRING DIAGRAM
2-53

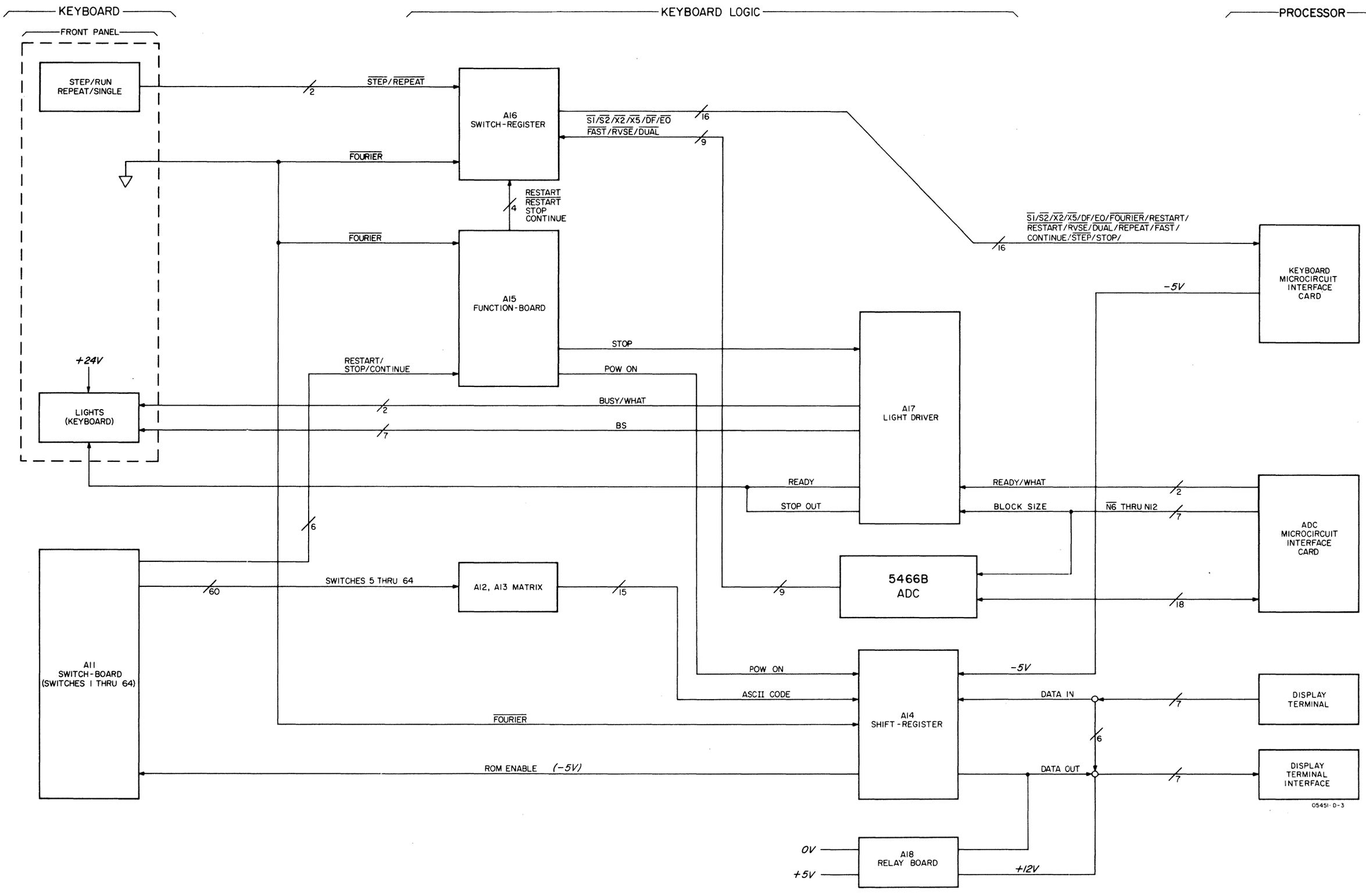


Figure 2-12
CONTROL UNIT BLOCK DIAGRAM

Table 2-13. Keyboard Signals to Matrix A and B

KEYBOARD CONNECTOR P19A/J19A	SIGNAL	MATRIX CONNECTOR	KEYBOARD CONNECTOR P19B/J19B	SIGNAL	MATRIX CONNECTOR
7	BLOCK SIZE	A12A(3)	11	SKIP	A12A(12)
8	POINT	A12A(4)	12	JUMP	A12A(13,P)
9	USER PROG	A12A(5)	13	COUNT	A12A(14,R)
11	DELET	A12A(6)	14	SUB RTRN	A12A(15)
12	RPLAC	A12A(7)	15	LABEL	A12A(S)
13	INSRT	A12A(8)	16	END	A12B(1,A)
14	LIST	A12A(9)	18	HISTOGRAM	A13A(C)
15	(?)	A12A(10)	19	RECT	A13A(D)
16	TERM	A12A(11)	20	LOAD	A13A(E)
18	MASS STORE	A12B(8,J)	21	STORE	A13A(F)
19	KEYBOARD	A12B(9,K)	22	LOG MAG	A13A(H)
20	PHOTO READR	A12B(10)	23	POLAR	A13A(J)
21	ANALG IN	A12B(11)	24	INTERCHNG	A13A(K)
22	ANALG OUT (OR BLANK)	A12B(12)	25	DSPLY	A13A(L)
23	PRINT	A12B(13)	36	(+)	A12B(2,B)
24	PUNCH	A12B(14)	37	(÷)	A12B(3,C)
25	BUFFD ANALG	A12B(15,S)	38	(←)	A12B(4,D)
35	ENTER	A13B(2)	39	(-)	A12B(5,E)
36	SPACE	A13B(3)	40	MULT	A12B(6,F)
37	CLEAR	A13B(4)	41	*MULT	A12B(7,H)
38	(-)	A13B(5)	43	(∫)	A13A(M)
39	RUB OUT	A13B(6)	44	HANN Ω	A13A(N)
41	(1)	A13B(8)	45	CONV	A13A(13)
42	(2)	A13B(9)	46	F	A13A(R)
43	(3)	A13B(L)	47	d/dx	A13A(S)
44	(4)	A13B(M)	48	TRANS FCN	A13A(14)
45	(5)	A13B(N)	49	CORR	A13A(15)
46	(6)	A13B(P)	50	POWER SPECT	A13B(1)
47	(7)	A13B(R)			
48	(8)	A13B(S)			
49	(9)	A13B(15)			
50	(0)	A13B(7)			

Table 2-14. Feedthru Signals — Computer to ADC

SIGNAL NAME	J15/P15 ADC CONNECTIONS	J12/P12 5475A CONNECTIONS	2 CH. 12566B I/O EDGE CONNECTIONS ①	4 CH. 12930A I/O CONNECTIONS ②
Signals from Computer:				
$\overline{N6}$ (BSI 64)	27	20	H	10
$\overline{N7}$ (BSI 128)	28	21	J	9
$\overline{N8}$ (BSI 256)	29	22	K	18
$\overline{N9}$ (BSI 512)	30	23	L	7
$\overline{N10}$ (BSI 1024)	31	24	M	6
$\overline{N11}$ (BSI 2048)	32	25	N	5
$\overline{N12}$ (BSI 4096)	26	8	P	4
$\overline{READY}$	NC	26	A	16
$\overline{WHAT}$	NC	27	B	15
GND	NC	19,1	24,BB	50
Signals to Computer:				
$\overline{BIT\ 0}$ ③	33	33	5	37B
$\overline{BIT\ 1}$ ③	44	35	6	36B
$\overline{BIT\ 2}$ ③ ($\overline{BIT\ 0}$) ④	1	18	7	35B
$\overline{BIT\ 3}$ ③ ($\overline{BIT\ 1}$) ④	2	17	8	34B
$\overline{BIT\ 4}$ ③ ($\overline{BIT\ 2}$) ④	3	16	9	33B
$\overline{BIT\ 5}$ ③ ($\overline{BIT\ 3}$) ④	4	15	10	32B
$\overline{BIT\ 6}$ ③ ($\overline{BIT\ 4}$) ④	5	14	11	31B
$\overline{BIT\ 7}$ ③ ($\overline{BIT\ 5}$) ④	6	13	12	30B
$\overline{BIT\ 8}$ ③ ($\overline{BIT\ 6}$) ④	7	12	13	29B
$\overline{BIT\ 9}$ ③ ($\overline{BIT\ 7}$) ④	8	11	14	28B
$\overline{BIT\ 10}$ ③ ($\overline{BIT\ 8}$) ④	9	10	15	27B
$\overline{BIT\ 11}$ ③ ($\overline{BIT\ 9}$) ④	10	9	16	26B
$\overline{GAIN\ 1}$	11	29	1	41B
$\overline{GAIN\ 2}$	12	30	2	40B
$\overline{GAIN\ 3}$	13	31	C,3	14B,39B
$\overline{DISPCT}$	14	32	4	38B
$\overline{EN}$	15	34	Z,22	24B
$\overline{DAR}$	16	36	AA,23	49B

①Used with HP Cable No. 05451-60002.
②Used with HP Cable No. 05451-60004.
③Bit Ø—11 are used in 12-bit ADC.
④Bit Ø—9 are used in 10-bit ADC.

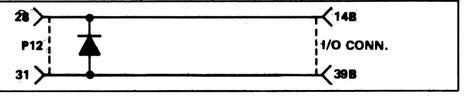


Table 2-15. Signal Outputs on Back of 5475A

SIGNAL	FROM	TO	5475A OPT.
SAMPLE OUT	J15(50)	J21	003, 004
$\overline{EN}$ OUT	J12(15)	J22	003, 004
DIGITIZE	J15(49)	J23	004
$\overline{DAR}$	J15(16)	J24	004
MULTX SAMPLE	J15(48)	J25	006

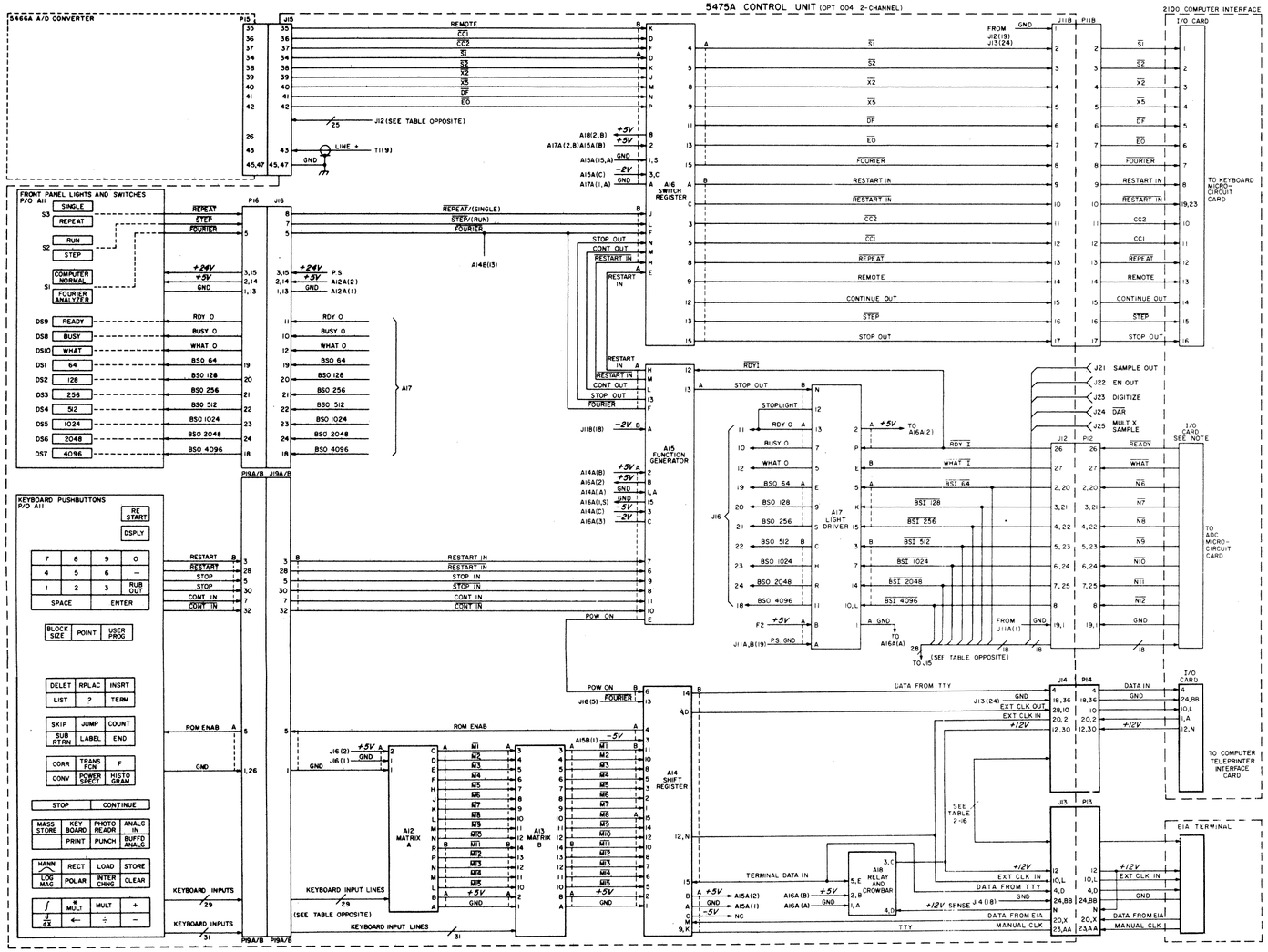


Figure 2-13
CONTROL UNIT WIRING DIAGRAM
(Sheet 1 of 2) 2-57

Table 2-16. Signals from Computer to Terminal

Signal Name	Terminal I/O Conn.	5475A J14	5475A J13 from/to Terminal	5475A Internal	Teleprinter or Terminal
DATA FROM TTY			4,D	A14B (15,S); A18(5E)	4
MANUAL CLOCK CONTROL			23,AA	A(9K)	24[1],BB
PUNCH (NOT USED)	6,F	24,6	6,F	N.C.	N.C.
PRINT (NOT USED)	8,J	26,8	8,J	N.C.	N.C.
EXT CLOCK	1,A(N.C.)	20,2	10,L	A14B (12,N)	10,L
CLOCK OUT		28,10		A14B(4,D)	
+12V	12,N	30,12	12	A18(3,C)	12,N
+12V SENSE			N	A18(4,D)	12,N
READ	13,P	31,B	N.C.	N.C.	N.C.
-12V	14,R	32,14	14,R		R,14
DATA TO TTY	16,T	34,16	16,T	N.C.	16,T
+12 FOR DATA PHONE	17,U	37,1F	17,U	N.C.	17,U
DATA FROM PINS 16,T	18,V	5,23	V	N.C.	V,18
DATA TO EIA DEVICE	19,W	19,1	W		W
DATA FROM EIA DEVICE	N.C.	N.C.	X	A14A(M)	N.C.

[1]A jumper to ground the MANUAL CLOCK CONTROL line must be installed in the cable connecting the Tektronix Terminal to the 5451, for proper operation of the "page full busy" terminal modification.

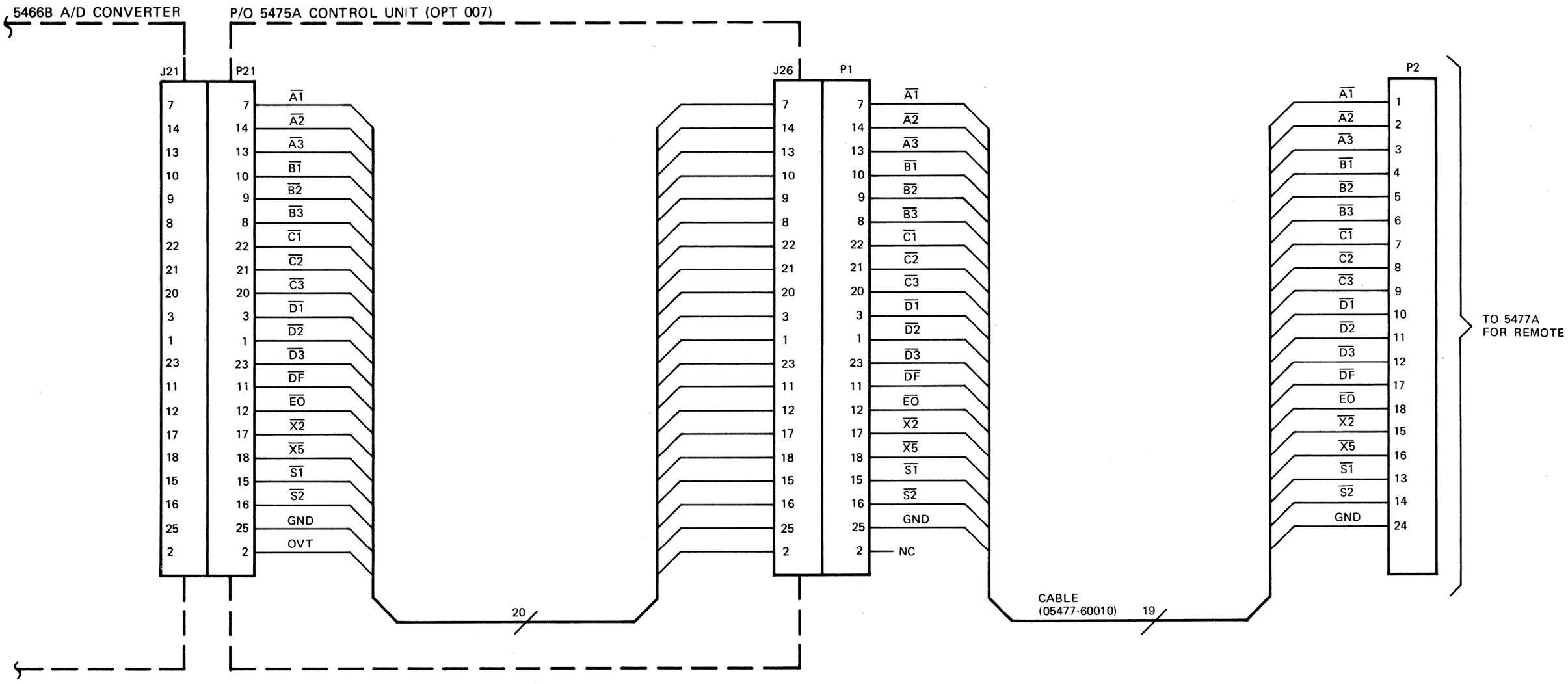


Figure 2-13
CONTROL UNIT WIRING DIAGRAM
(Sheet 2 of 2) 2-59

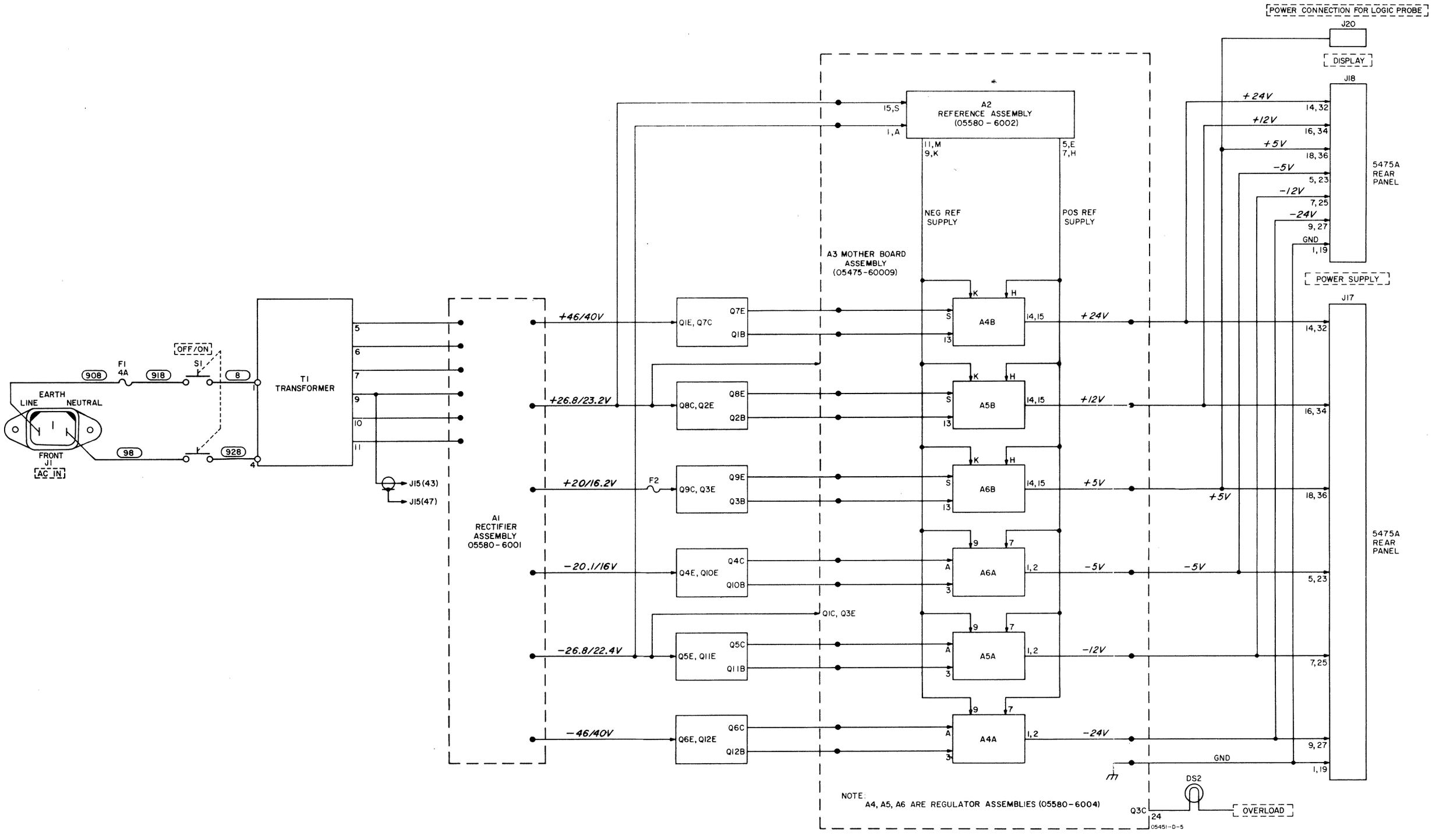


Figure 2-14
CONTROL UNIT POWER SUPPLY WIRING DIAGRAM

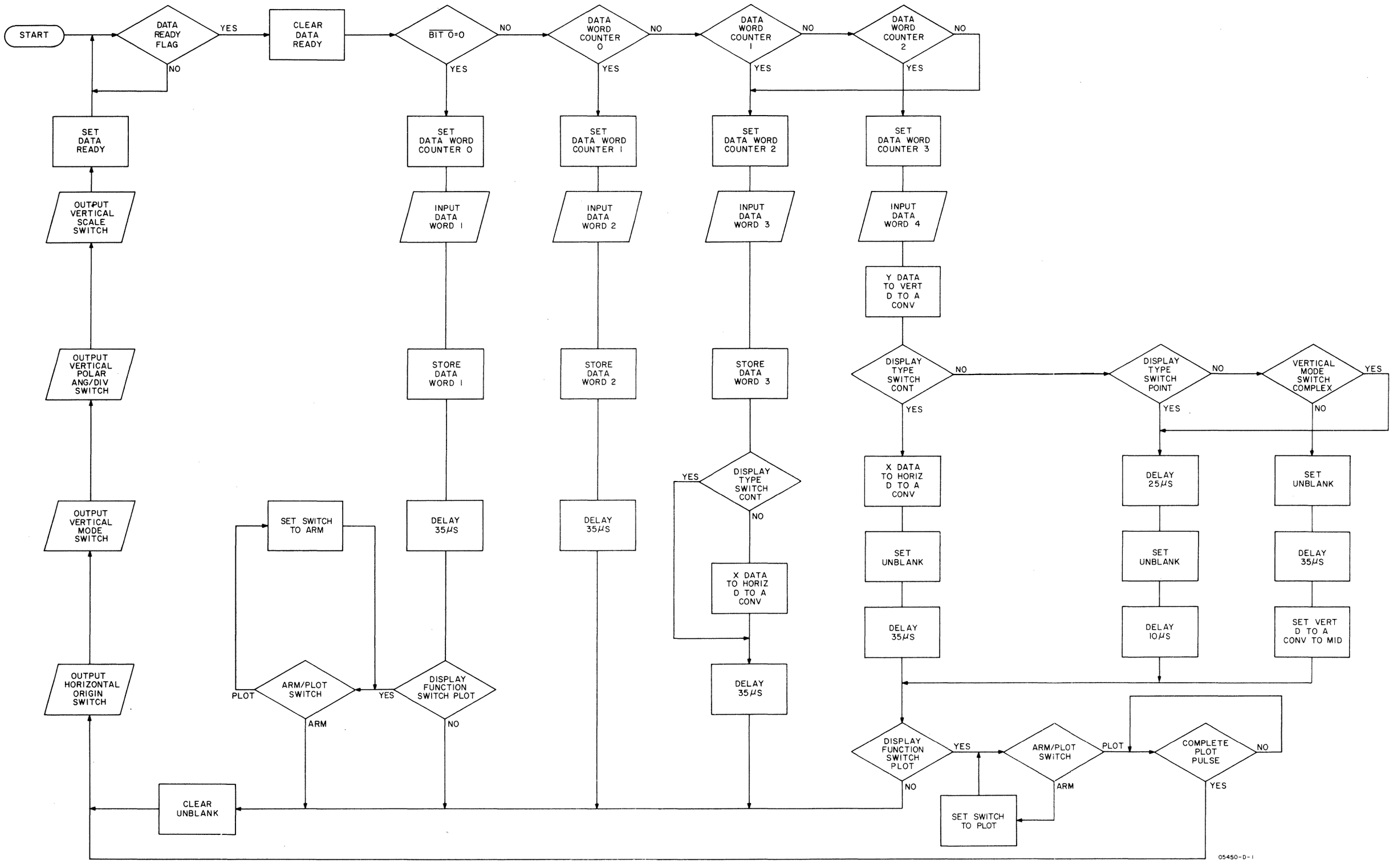


Figure 2-15
DISPLAY UNIT OPERATION FLOW DIAGRAM

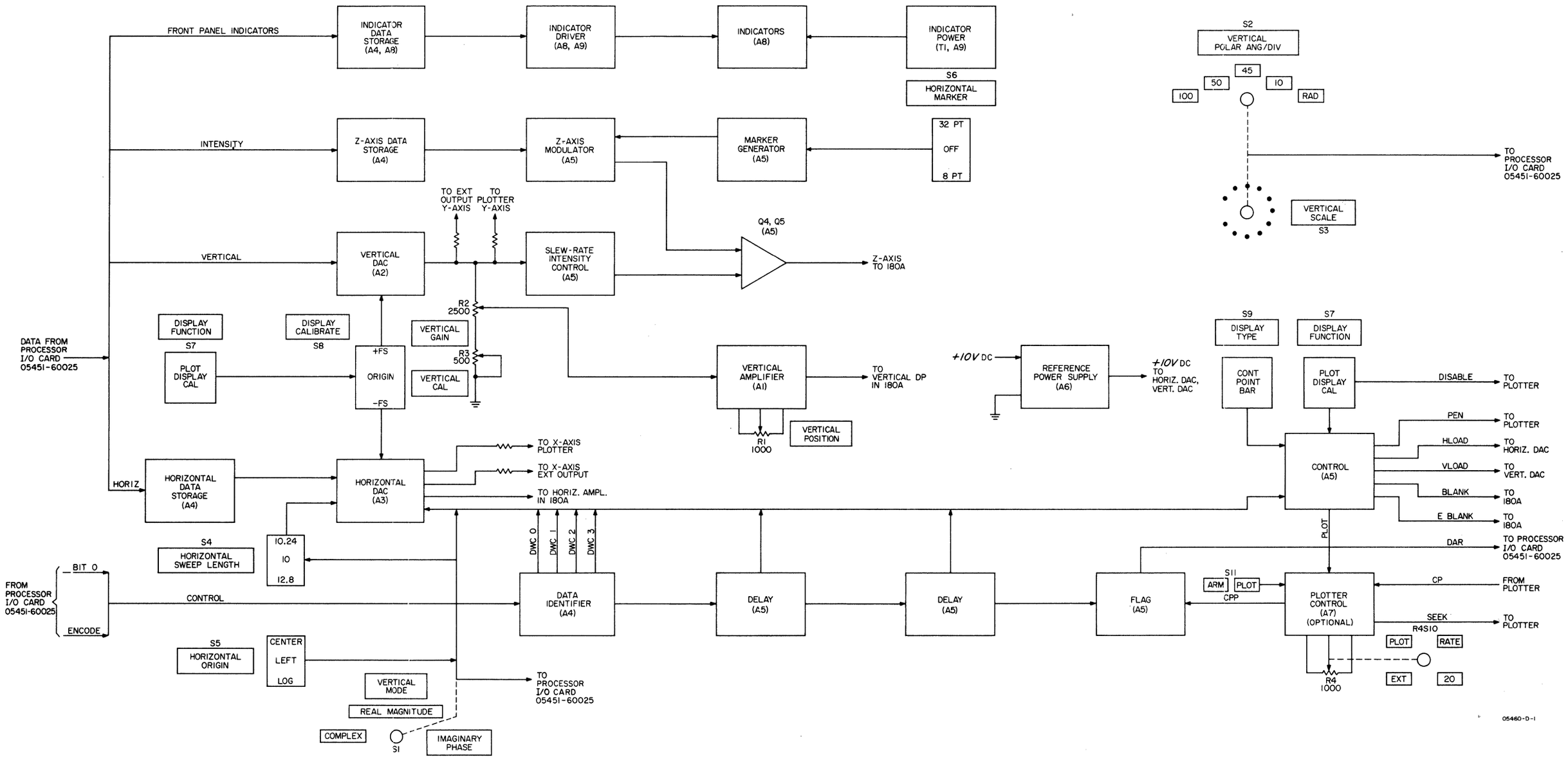


Figure 2-16
DISPLAY UNIT BLOCK DIAGRAM
2-65

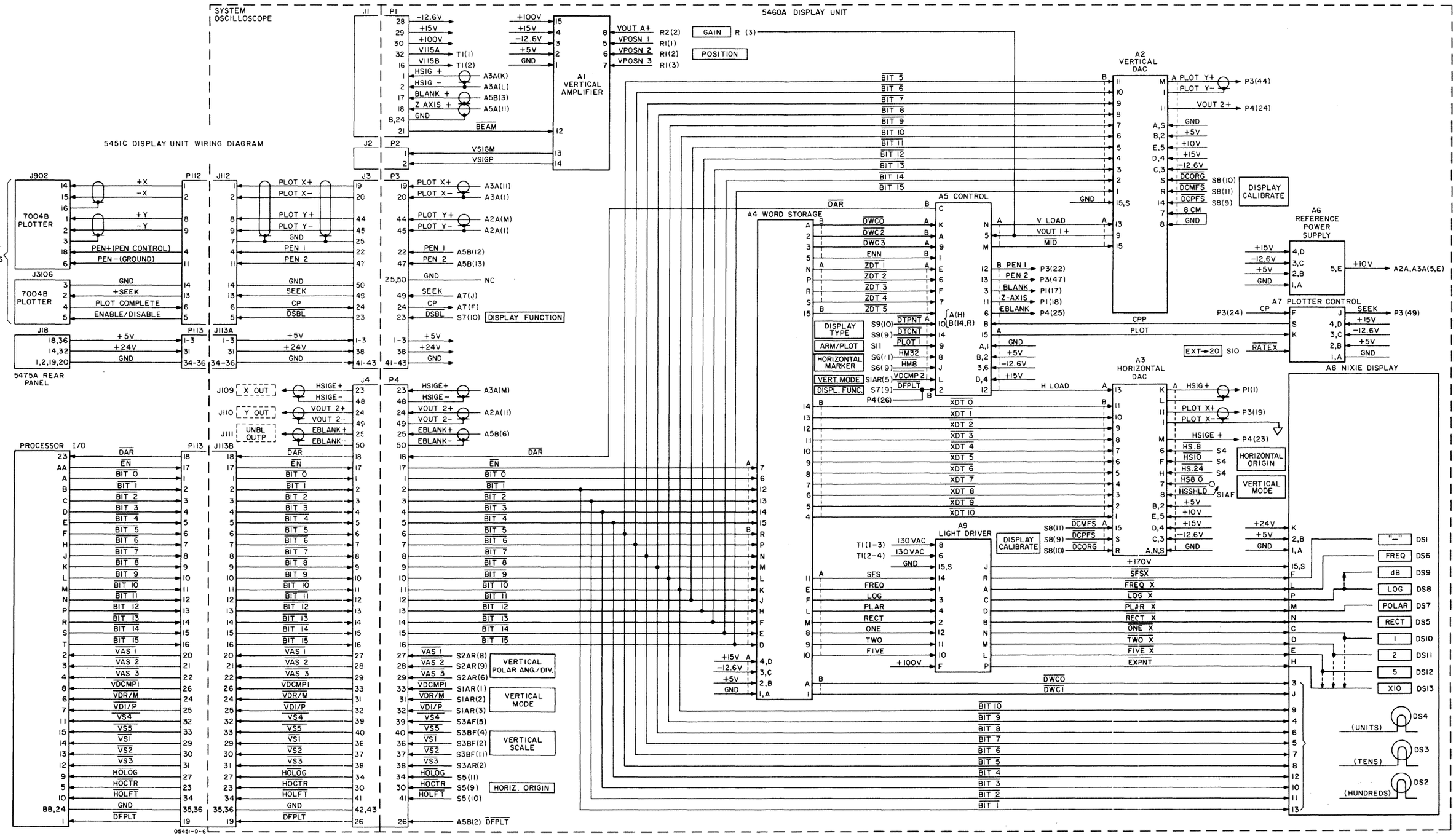


Figure 2-17
DISPLAY UNIT WIRING DIAGRAM
2-67

SECTION 3
CHECKS AND ADJUSTMENTS

INTRODUCTION

This section provides a system checkout procedure for the 5451C Fourier Analyzer System. For additional operational checks of peripheral equipment supplied with the system or for checks as a stand-alone computer, refer to the applicable manuals. Adjustment procedures are provided for the 5460A Display Unit, 5466B ADC, and 5475A Control Unit. Refer to Table 1-4 for a complete list of test equipment required.

SYSTEM TEST DIAGNOSTIC AND OPERATIONAL CHECK

The system disc supplied with each Fourier Analyzer System provides an operational check of the Display Unit, the ADC, and the Control Unit Keyboard. System testing is arranged in subroutines to check out the Processor input and output commands and data transfer lines to the system. The system disc writes over parts of the main Fourier Program, and does not check the system software that performs the Fourier transform, or any of the other functions implemented by the system software and called up via the keyboard; therefore the main Fourier Program must be reloaded to check these.

The system operational check verifies that the unique system units (5460A Display Unit, 5466B ADC and 5475A Control Unit) are functioning properly. If a unit fails to perform a specific test, refer to the applicable troubleshooting procedure in Section 4. The system test and operational check requires approximately 2 hours to perform.

POWER TURN-ON PROCEDURE

1. Turn on rack power by pressing SYSTEM ON/OFF pushbutton in upper right corner to on.

2. On oscilloscope, set LINE switch to ON.

3. On HP 5475A Control Unit, press ON-OFF pushbutton to ON.

4. Set the Processor ~POWER switch to OFF then ON. The Processor shoud perform a brief self test. When the test is complete, only the T register indicator should be on. If other indicators (A,B,M,P,S) are on, set the ~POWER switch to OFF then back to ON until the proper result is obtained. If unable to obtain the proper result, refer to the Processor Service Manual.

5. For 7900A, on HP 13215A Disc Power Supply, set POWER switch to ON. For 7906A, set the POWER switch on the back of the disc drive to 1.

6. On rear panel of HP 2648A Display Terminal, set ~LINE switch to ON. On terminal keyboard, set REMOTE, CAPS LOCK, and AUTO LF buttons to depressed position. All other control buttons in the up position.

7. Set Display Terminal for alpha-numeric mode as follows:
   a. Tap RESET TERMINAL twice quickly.
   b. Press STOP.
   c. Press SHIFT G DSP simultaneously.

SYSTEM TEST DIAGNOSTIC LOADING

1. For the HP 7900A Disc Drive Unit, set LOAD-UNLOAD switch to UNLOAD and wait for DOOR UNLOCKED indicator to light. For the HP 7906A Disc Drive, set RUN/STOP switch to STOP and wait for the DOOR UNLOCK light to indicate.

2. For the 7900A, open door on Disc Drive Unit and insert system disc pack (HP 54451-10001). Set LOAD-UNLOAD switch to LOAD and wait for DRIVE READY indicator to light. For 7906A, open the door, and insert system disc P/N 54451-10101. For mag tape system, P/N 54451-10102, set RUN/STOP switch to RUN and wait for the DRIVE READY indicator to light.

3. On HP 54451B, load disc basic binary loader (NIBBL) as follows:
   a. Press <Register Select> switch until S register is selected. Enter 101701_8 (7900A) or 111700 (7906A) in Display Register, then press STORE.
   b. Press PRESET, IBL, RUN.
   c. Processor should halt at 102076_8.

4. On 54451B Processor, load system test diagnostic as follows:

   NOTE

   For diagnostics other than the system test, see Appendix A.

   a. Select P register, enter 077600_8, STORE.
   b. Select S register, press CLEAR DISPLAY, STORE.
   c. Select A register, enter 000001_8, STORE.
   d. Select B register, enter 000041_8, STORE.
   e. Press PRESET, RUN.
   f. Processor should halt at 102011_8.
   g. Select P register, enter 004000_8, STORE.
   h. Select S register, enter Display Terminal Interface channel address (normally 000011_8), STORE.
   i. Press PRESET, RUN.

   NOTE

   If above procedure cannot be performed, check NIBBL listing in Appendix A.

5. The Display Terminal will display a series of statements requesting I/O channel locations. Answer each question by entering the appropriate channel number on the Display Terminal Keyboard. Use AUTO LF and press RETURN after each entry. If channel numbers are not known, refer to System Configuration Notice. Standard configuration is:

CHANNEL NO.	DEVICE	DISPLAY
14	ADC	ADC?
15	Display	DISPLAY?
16	Control Unit Keyboard	KEYBOARD INTERFACE?
Other channel assignments are: Display Terminal 11, Jumper or Line Printer 13, Photoreader 10, Tape Punch 12.		

Table 1-2 lists strapping requirements for the ADC Data, Display, and Keyboard interface cards.

6. Display Terminal prints out "CONFIGURATION IS COMPLETE, START".

7. The system is now ready for diagnostic testing. Subroutines available are:

   Control Unit — QK, SK
   Display Unit — SD, QD
   ADC — SA, QA, QM, SM

CONTROL UNIT TESTS AND SUBROUTINES

These checks test the Control Unit Keyboard functional operation. If a system fails any portion of these tests, refer to Control Unit troubleshooting in Section 4. The operational check troubleshooting is listed under the same heading as the test being performed. For example, troubleshooting for the preliminary keyboard test is contained in Section 4 under Preliminary Keyboard Troubleshooting.

Preliminary Keyboard Test

1. On 5475A Control Unit Keyboard, press keys as shown in Table 3-1 and then press ENTER. Verify that Display Terminal displays correct characters.

   NOTE

   The ASCII code for each character appears in the display register for each key depressed. In case of difficulty, see Table 4-3 for listing.

QK Subroutine Test

For this test, information is loaded through the keyboard interface card into the display register.

1. On the Display Terminal, type QK, RETURN.

   NOTE

   If BUSY light is on, perform step 2, then 3. If READY light is on, perform step 3, then 2.

2. Press STOP, On Processor, verify bit 15 is on for 3 seconds, READY is on and BUSY is off after 3 seconds.

3. Press CONTINUE. On Processor, verify bit 13 is on for 3 seconds, READY is off and BUSY is on after 3 seconds. Press STOP again to return to READY mode for next test.

4. Set switches according to Table 3-2 and verify bit lights.

SK Subroutine Test

This subroutine tests the Control Unit response to its command lines sent from the Processor through keyboard cable (J11).

1. Press RESTART. Verify Display Terminal displays START.

2. Type SK, RETURN. Verify each keyboard front panel lights in a repetitive sequence. Note that BUSY goes off only when READY goes on.

3. Press RESTART. Verify Display Terminal displays START and program jumps out of light test loop.

Table 3-1. Preliminary Keyboard Test

Signal Name	Teleprint	Signal Name	Teleprint
BLOCK SIZE	BS	HANN	H1
CURSR	/.	RECT	TR
USER PROG	Y ( ) †	LOAD	X<
DELET	/D	STORE	X>
RPLAC	/R	LOG MAG	TL
INSRT	/I	POLAR	TP
LIST	/L	INTER CHNG	X ( )
POINT	? ( )	CLEAR	CL
TERM	/ ( )	$\int$	$ ( )
SKIP	IF	*MULT	*-
JUMP	J ( )	MULT	* ( )
COUNT	# ( )	+	A+
SUB RTRN	< ( )	$\frac{d}{dx}$	% ( )
LABEL	L ( )		
END	. ( )	←	← ( )
CORR	CR	÷	: ( )
TRANS FCN	CH	-	A-
F	F ( )	1	1
CONV	CV	2	2
POWER SPECT	SP	3	3
HISTOGRAM	RH	4	4
MASS STORE	MS	5	5
KEYBOARD	K ( )	6	6
PHOTOREADR	R ( )	7	7
ANALG IN	RA	8	8
ANALG OUT	B ( )	9	9
PRINT	W ( )	0	0
PUNCH	P ( )	-	-
BUFFD ANALG	RB	RUBOUT	(BELL)
		SPACE	( )
		ENTER	CR LF

† ( ) indicates one character space; to test this, press the key twice.

DISPLAY UNIT TESTS AND SUBROUTINES

These checks test the Display Unit functional operation. If a system fails any portion of these tests, refer to Display Unit troubleshooting in Section 4. The operational check troubleshooting is listed under the same heading as the test being performed. For example, troubleshooting for the Display Unit SD subroutine test is contained in Section 4 under SD subroutine test troubleshooting.

SD Subroutine Test

This subroutine controls the output to the Display Unit from the Processors switch register.

1. On the Display Terminal, enter SD, RETURN.
2. Set Display Unit FUNCTION switch to DISPLAY. Verify bit 15 light is off.

NOTE

If bit 15 light is on, the data ready flag (DAR) is not responding. Repeat procedure. If bit 15 light remains on, refer to troubleshooting.

Table 3-2. Switch Verification

Instrument	Switch and Setting	Processor Display Register Lamps			
5475A	STEP/RUN = STEP STEP/RUN = RUN	14 lighted 14 off			
	REPEAT/SINGLE = REPEAT REPEAT/SINGLE = SINGLE	11 lighted 11 off			
5466B	SAMPLE MODE SWITCH	Bit 12 (Remote)	Bit 5 (EO)	Bit 4 (DF)	
	REMOTE	on	on	on (bits 3,2,1, and Ø also "on" for REMOTE)	
	kHz/μs	off	on	off	
	ΔTIME Hz/ms	off	off	off	
	ΔFREQ Hz/ms	off	on	on	
	mHz/sec	off	off	on	
	MULTIPLIER SWITCH	Bit 3 (X5)	Bit 2 (X2)	Bit 1 (S2)	Bit Ø (S1)
	500/1K/1 250/500/2 100/200/5 50/100/10	on off on on	off on on off	off off on on	off off on on
	25/50/20 10/20/50 100/10/5 200/5/2.5	off on on off	on on off on	on on on on	on off off off
	500/2/1 1K/1/.5 2K/.5/.25 5K/.2/.1	on on off off	on off on off	off off off off	on on on on
	DISPLAY/INPUT SWITCH (2-channel unit only)	Bit 10 (CC1)		Bit 9 (CC2)	
	A/A A/AB B/AB	off on on		on on on	
	INPUT SELECTOR SWITCH (4-channel unit only)	Bit 10 (CC1)		Bit 9 (CC2)	
	A AB ABC ABCD	off on off on		on on off off	

3. On Processor, clear the S register.
4. Set switches in the S register according to Table 3-3 and verify correct response.
5. Set up Display Unit controls as follows:

   VERTICAL POSITION to center trace
   (knob at approximately 11 o'clock)
   GAIN to CAL (switch engaged)
   PLOT RATE to MAX
   ARM/PLOT to ARM
   INTENSITY to approximately 4 o'clock

Place all other rotary switches to up position, and all slide switches to center position.

6. Press bit 11 on, all others off.

7. Set switches according to Table 3-4 and verify correct responses.

QD Subroutine Test

This test routine begins by sending out a display command word at all zeros. This word activates certain display indicators (e.g., RECT) then after 100 μsec, bit 15 should be cleared indicating an interrupt has been generated by the display through the Processor interface card. A data word containing the display unit front panel switch setting (see Table 3-5) is then sent through the Processor interface card and is displayed on the Processor display register. Each time a display unit switch setting is changed an interrupt is generated and the displayed word is checked against the table.

1. Type QD, RETURN.

2. Set switches according to Table 3-5 and verify correct response.

ADC TESTS AND SUBROUTINES

These checks test the ADC functional operation. If a system fails any portion of these tests, refer to ADC troubleshooting in Section 4. The oerational check troubleshooting is listed under the same heading as the test being performed. For example, troubleshooting for the SA subroutine test is contained in Section 4 under the listing of SA subroutine test troubleshooting.

SA Subroutine Test

This subroutine sends the Processor's switch register content out through the ADC microcircuit I/O card to control ADC functions. Switch register bit "15" sets or clears the control to the I/O card.

TRIGGERING TESTS

This check tests that all ADC triggering modes are operating. Activating bit "15" enables an ENcode signal to the ADC, arming the triggering cycle.

1. Type SA RETURN

Table 3-3. SD Subroutine Bit Test

Display Register	Pushbutton Light	Action
0	On	POLAR on. RECT off.
1	On	LOG on. dB on.
1	Off	LOG off. dB off.
2	On	FREQ on.
2	Off	FREQ off.
3	On	Units counts 1—9, then blanks for 6 counts.
3	Off	Units readout of last count.
4	On	Tens, same as units
4	Off	Tens, same as units
5	On	Hundreds, same as units.
5	Off	Hundreds, same as units.
6	On	Minus (-) on.
6	Off	Minus (-) off.
7	On	5 on. X10 on.
7	Off	5 off. X10 off.

Table 3-3. SD Subroutine Bit Test (continued)

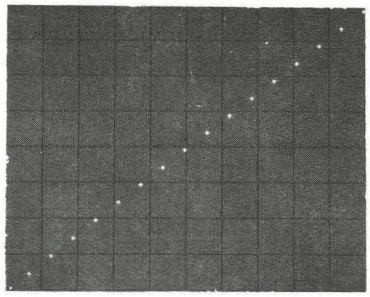
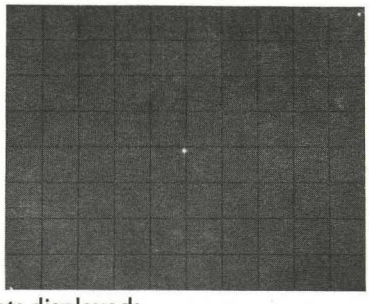
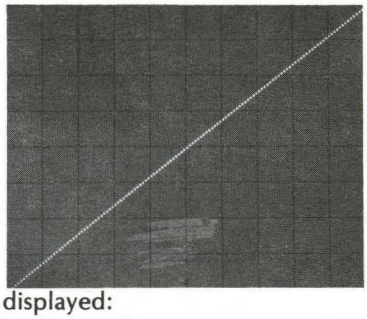
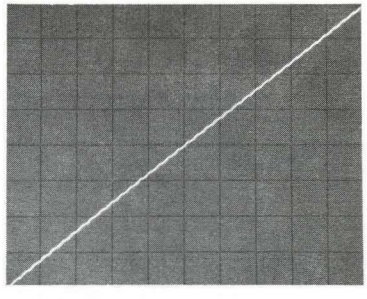
Display Register	Pushbutton Light	Action
8	On	2 on. X10 on.
8	Off	2 off. X10 off.
9	On	1 on. X10 on.
9	Off	1 off. X10 off.
10	On	17 points displayed:
(On Display Unit, set DISPLAY TYPE to point. If necessary, use HORIZONTAL POSITION on Display Unit to view points off screen.)		
10	Off	3 points displayed:
		
11	On	129 points displayed:
(Set DISPLAY TYPE to BAR, MARKER to 8 or 32 point for easier display interpretation.)		
11	Off	3 points displayed:
12	On	513 points displayed:
		

Table 3-3. SD Subroutine Bit Test (continued)

Display Register	Pushbutton Light	Action
12	Off	3 points displayed.
13	On	1025 points displayed.
13	Off	3 points displayed.
14	On	2049 points displayed.
14	Off	3 points displayed.

NOTE

When using switches 10—14, the result of having the most significant bit switch on will be displayed. When using switches 12—14 it is difficult to determine the number of points displayed. However the length of time it takes to sweep can be used to determine if the correct number of points is displayed (i.e., it takes twice as long to sweep 2049 points as to sweep 1025 points).

2. Set controls as follows:

   5466B:

   OVERLOAD VOLTAGE (all): ".125"
   TRIGGER LEVEL: "12 o'clock"
   SAMPLE MODE: INT., kHz/μs
   MULTIPLIER: 500/2/1
   INPUT SELECTOR: A

   Processor:

   Bit "15": off ("0")

3. Set 5466B TRIGGER SOURCE to FREE RUN.

   TRIGGERING lamp should be "off".

4. Set Processor bit "15" "on" ("1"). TRIGGERING lamp should light, indicating that the trigger circuit is armed.

5. Set Processor bit "15" "off" ("0").

   TRIGGERING lamp should turn "off".

6. Set 5466B TRIGGER SOURCE to LINE.

   Repeat steps "4" and "5" above.

7. Set 5466B TRIGGER SOURCE to INTERNAL (A). Set OVERLOAD VOLTAGE A to CHECK.

   Repeat steps "4" and "5". Slight TRIGGER LEVEL adjustment may be required.

8. Set controls as follows:

   5466B:

   TRIGGER SOURCE: EXT. DC

   Processor:

   Bit 15: "off"

9. Connect a 100 Hz, 100 mV rms sine wave from an external source through a 50-ohm feedthrough connector to the 5466B TRIGGER INPUT connector.

10. Repeat steps "4" and "5".

    Slight TRIGGER LEVEL adjustment may be necessary.

Table 3-4. SD Subroutine Display Test

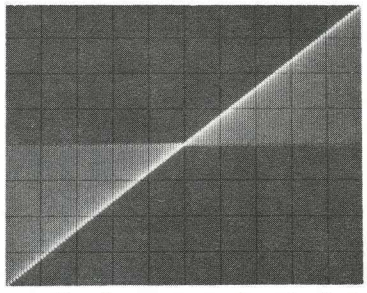
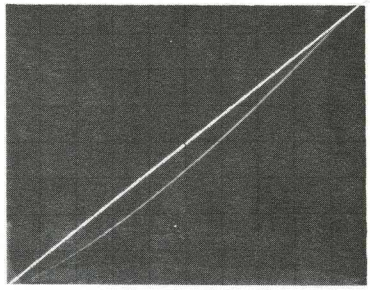
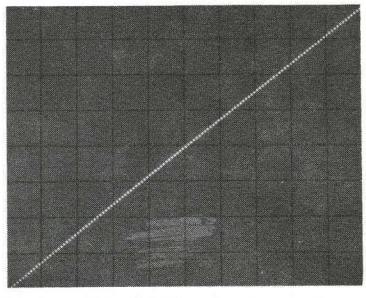
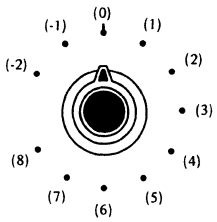
5460A Switch Setting	Switch Effect
	Note: Adjust intensity to detect markers if necessary.
HORIZONTAL MARKER to:	
32 PT	Intensified trace every 32nd point.
8 PT	Intensified trace every 8th point.
OFF	No intensification of trace.
DISPLAY TYPE to BAR	Vertical bars on CRT from mid-scale to point being displayed. (Note: VERTICAL MODE switch in COMPLEX will disable vertical bar.)
	
DISPLAY TYPE to CONT (Press bit 10 to on, all others off.)	Continuous line between each point being displayed. (Note: VERTICAL MODE must be set to REAL/MAGNITUDE.)
	
DISPLAY TYPE to POINT (Press bit 10 and 11 to on.)	Small dot at each point being displayed.
	
(Set DISPLAY FUNCTION to CAL and DISPLAY CALIBRATE to -FS)	(Point displayed on CRT at horizontal position.)
HORIZONTAL SWEEP LENGTH to: (Press bit 10 to off.)	
10.24	5.05 to 5.2 cm (from left most graticule line).
12.8	6.3 to 6.5 cm
10	4.95 to 5.05 cm
VERTICAL MODE to:	
COMPLEX	3.95 to 4.05 cm
REAL/MAGNITUDE	4.95 to 5.05 cm
IMAGINARY/PHASE	4.95 to 5.05 cm

Table 3-5. QD Subroutine Test

5460A Switch Setting	Bits Affected and State: X = on, O = off													
HORIZONTAL ORIGIN to:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
LEFT						X	O				O				
LOG						O	X				O				
CENTER						O	O				X				
VERTICAL MODE to:															
COMPLEX								X	O	O					
REAL/MAGNITUDE								O	O	X					
IMAGINARY/PHASE								O	X	O					
VERTICAL SCALE to:															
-2 (Full CCW)	X	O	O	X	O										
-1	X	O	O	O	X										
Ø	O	O	O	O	O										
1	O	O	O	O	X										
2	O	O	O	X	O										
3	O	O	O	X	X										
4	O	O	X	O	O										
5	O	O	X	O	X										
6	O	O	X	X	O										
7	O	O	X	X	X										
8 (Full CW)	O	X	O	O	O										
POLAR ANG/DIV to:															
100												O	X	O	O
50												X	O	O	O
45												O	O	O	O
10												O	O	X	O
RAD												X	X	O	O



11. Change TRIGGER INPUT signal to 10 kHz 100 mV rms (through the 51-ohm feed-through termination).

12. Repeat steps "4" and "5".

    Slight TRIGGER LEVEL adjustment may be required.

UNCAL TEST

Certain combinations of SAMPLE MODE and MULTIPLIER switch settings indicate a MAX FREQ or TOTAL TIME range that is beyond the sampling capability of the ADC. In these conditions, the analyzer is UNCALibrated. If you select one of these combinations, the UNCAL lamp lights. The UNCAL test is a part of the "SA" test.

1. Set switches according to Table 3-6.

2. Verify that the UNCAL lamp lights only at the appropriate switch settings.

QA Subroutine Test

The Query Analog subroutine transfers data from the ADC via the ADC's I/O channel. If bit "3" (DSPCT") of the ADC's data word is "1", the word will be presented on the Processor's display unit. The binary word is converted to a BCD word which is sent to the display channel to be displayed on the LED display. A word in which bit "6" ("BLOCK SIZE 64") is "1" and all other bits are "0" is then sent to the ADC channel, and, after a 50 msec delay, the cycle is repeated.

Table 3-6. UNCAL Test

5466B		Set Processor Switch Register Bits (All switches off unless noted.)	5466B
SAMPLE MODE	**MULTIPLIER**		**UNCAL Lamp Status**
INT.ΔTIME, kHz/μs	500/1K/1 250/500/2 100/200/5 All other settings	All switches off	On On On* Off
INT.ΔTIME, Hz/ms	All Settings	All switches off	Off
INT.ΔFREQ, Hz/ms	500/1K/1 250/500/2 100/200/5 50/100/10 25/50/20 All other settings	12 on	On On On On On Off
	500/1K/1 250/500/2 100/200/5 50/100/10 All other settings	11 on	On On On On Off
	500/1K/1 250/500/2 100/200/5 All other settings	10 on	On On On Off
	500/1K/1 250/500/2 All other settings	9 on	On On Off
	500/1K/1 All other settings	8 on	On Off
	All Settings	7 on, then 6 on	Off
INT.Δf mHz/sec	All Settings	6 thru 12 on	Off
EXT All settings	All Settings		On
*When A7 jumper is in 100 kHz position			

CALIBRATION CHECK (200 kHz DIGITIZERS)

This test receives information from the 5466B, and displays it as a digital number on the 5460A Display Plug-in's readout tubes. This portion of the QA test also checks operation of the DISPLAY switch.

Depending on the options, if any, that were ordered, the ADC may have two or four digitizing channels, and these channels will have either 10-bit or 12-bit digitizers. This procedure can be used to check any version.

The digitizers operate like zero-center voltmeters. A "zero-volt" input gives a readout of the binary equivalent of zero counts. "Full-scale" positive or negative input voltage on any input range gives an output equivalent of ± 512 counts for a 10-bit ADC, or ± 2048 counts for a 12-bit ADC.

The procedure below determines approximate accuracy of the 5466B ADC by using the CHECK pulse, supplied internally, and noting the ADC output. This 51 mV pulse is fed into the digitizer at the equivalent of the ".125" (volt) range. Table 3-7 is provided as a convenient worksheet for determining the approximate accuracy of your ADC's channels.

1. Type QA RETURN to begin the test routine.

2. Set controls as follows:

   Processor:

   For 12-bit digitizers, set bit "15" to "1".

   ADC:

   SAMPLE MODE: INT, kHz/μs
   MULTIPLIER: 10/20/50
   DISPLAY/INPUT (2-channel): A/AB
   DISPLAY (4 channel): A
   INPUT (4-channel): ABCD
   OVERLOAD VOLTAGE (all): CHECK
   TRIGGER SOURCE: INTERNAL (A)
   AC/DC (all); DC
   SLOPE: NEG
   TRIGGER LEVEL: approximately "2 o'clock"
   (verify that display indicators flicker)

3. Adjust TRIGGER LEVEL control until ADC triggers, indicated by 5460A readout changing.

4. Measure the dc zero offset of the CHECK signal by reading the number in the 5460A Display Unit's readout; this number should be 000 ± 8 counts for 10-bit ADC, or 000 ± 32 for 12-bit ADC.

   Record this "initial value" for the appropriate channel in the chart in Table 3-7.

5. Set 5466B SLOPE to POS.

6. If necessary, adjust TRIGGER LEVEL until ADC triggers.

7. Record the number now displayed on the 5460A as the "final value" in the chart in Table 3-7. The difference between this and the "initial value" must be 209 ± 5 counts for a 10-bit ADC, or 836 ± 10 counts for a 12-bit ADC.

8. Repeat steps "2" through "7" for the remaining ADC channels. For 2-channel unit, set DISPLAY/INPUT to B/AB to display channel B. For 4-channel unit, set DISPLAY successively to "B", "C", and "D".

Table 3-7. Calibration Check—Worksheet

	CHANNEL A	CHANNEL B	CHANNEL C	CHANNEL D
Final Value	_____	_____	_____	_____
Initial Value[1]	_____	_____	_____	_____
Difference[2] (Final—Initial)	_____	_____	_____	_____

[1,2]

Specs:	Initial Value[1]	Difference[2]
10-bit	000±8	209±5 (204-214)
12-bit	000±32	836±10 (826-846)

OVERLOAD VOLTAGE SWITCH TESTS

These tests are part of the "QA" test group. Each OVERLOAD VOLTAGE switch setting provides an output code to the Processor. These tests ensure that the OVERLOAD VOLTAGE gain codes are correct for all settings of all switches.

1. Type QA RETURN.

2. Set controls as follows:

   5466B:

   SAMPLE MODE: kHz/μs
   MULTIPLIER: 50/100/10
   TRIGGER SOURCE: FREE RUN

   Processor:

   For 12-bit ADC, bit "15" to "1".

3. Set INPUT SELECTOR to AB and DISPLAY to A.

4. Check Processor display for each OVERLOAD VOLTAGE A position. It should be as shown in Table 3-8.

5. Repeat step "4" for OVERLOAD VOLTAGE switches B, C, and D. (Set INPUT SELECTOR and DISPLAY controls to channel you want to check.)

Table 3-8. Attenuator Code Test

OVERLOAD VOLTAGE SETTING	COMPUTER DISPLAY REGISTER		
	Bit 2	Bit 1	Bit Ø
CHECK	ON	OFF	OFF
.125	ON	OFF	OFF
.25	ON	OFF	ON
.5	ON	ON	OFF
1	OFF	ON	ON
2	OFF	ON	OFF
4	OFF	OFF	ON
8	OFF	OFF	OFF

ADC GAIN CHECK

The gain check confirms that OVERLOAD VOLTAGE switch codes set up the corresponding gain in the input amplifiers.

1. Type QA RETURN.

2. Set controls as follows:

   Processor:

   Bit "10" "on" ("1")
   For 12-bit ADC, bit "15" to "1".

   5466B:

   SAMPLE MODE: INT.
   MULTIPLIER: 10/20/50
   ΔFREQ/TOTAL TIME: Hz/ms
   TRIGGERING: FREE RUN
   SLOPE: POS
   TRIGGER LEVEL: "12 o'clock"
   DISPLAY/INPUT SELECTOR (2-channel): A/AB
   INPUT (4-channel): ABCD
   DISPLAY (4-channel): A
   INPUT CHANNEL AC-DC to DC (all channels)

3. Connect the HP 6115A Precision Power Supply to all 5466B Inputs (A, B, C, D), either simultaneously or consecutively.

4. Set Power Supply output and 5466B OVERLOAD VOLTAGE A according to Table 3-9, and confirm readout.

Table 3-9. OVERLOAD VOLTAGE Gain Check

5466B OVERLOAD VOLTAGE SETTING	INPUT SIGNAL AMPLITUDE ("+" and "–")
8	6.400V
4	3.20V
2	1.60V
1	800 mV
.5	400 mV
.25	200 mV
.125	100 mV

For all combinations listed in Table 3-9, the readout should be:

- "409 ± 5" (404-414) for 10-bit digitizer
- "1636 ± 20" (1616-1656) for 12-bit digitizer (1 is displayed on annunciator and the last three digits are displayed on the LED's).

These numbers should be negative when the input voltages are negative.

5. Repeat steps "2" through "4" for Channels B, C, and D. Set DISPLAY and INPUT SELECTOR switches to display channel with which you are working.

SAMPLE RATE TEST

This test checks the sample frequency set up by the SAMPLE CONTROL switches. The SAMPLE MODE codes have already been checked (QK Test).

INTERNAL SAMPLE RATE TESTS

1. Type SA RETURN.

2. Set Controls as follows:

   5466B:

   TRIGGERING: FREE RUN
   SAMPLE MODE: INT

   Processor:

   All "S" bits "off".

3. Connect the Sample Out signal from 5475A rear-panel BNC connector to input of a HP 5300A/5303 Option 001 Counter. Set Counter's GATE TIME to 1 second. (As an alternate, the Counter's input could be connected to the "SAMP" test point on the 5466B's A10 Sample Generator Assembly.)

4. Set SAMPLE CONTROL switches according to Table 3-10. Observe results. Be sure to note that the sample frequency is divided down (see Calibration and Adjustments section for frequency adjustment).

Table 3-10. ΔTIME Sample Rate Test

5466A SAMPLE CONTROLS		FREQUENCY
kHz/μs	500/1K/1	1.000000 MHz ± .000005 MHz
	250/500/2	500.000 kHz ± .003 kHz
	100/200/5	200.000 kHz ± .002 kHz
	50/100/10	100.000 kHz ± .001 kHz
	25/50/20	50.000 kHz ± .001 kHz
	10/20/50	20.000 kHz ± .001 kHz
	100/10/5	10.000 kHz
	200/5/2.5	5.000 kHz
	500/2/1	2.000 kHz
	1K/1/.5	1.000 kHz
	2K/.5/.25	.500 kHz
	5K/.2/.1	.200 kHz
ms/Hz	500/1K/1	1.000 kHz
	250/500/2	.500 kHz
	100/200/5	.200 kHz

5. Set SAMPLE MODE TO ΔF, Hz/ms, and MULTIPLIER to 500/1K/1.

6. Set the Processor bit specified in Table 3-11 "on", and all other bits "off". (Retype SA RETURN if not able to turn off computer bits).

   Output frequency should correspond to that given in the Table.

Table 3-11. ΔFREQ Sample Rate Test

All Computer Bits "off", except:	FREQUENCY
12	4.096000 MHz ± .000010 MHz
11	2.048000 MHz ± .000005 MHz
10	1.024000 MHz ± .000003 MHz
9	512.000 kHz ± .002 kHz
8	256.000 kHz ± .001 kHz
7	128.000 kHz ± .001 kHz
6	64.000 kHz

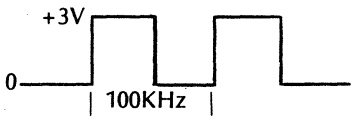
EXTERNAL SAMPLE TEST

This test runs the ADC at a very fast rate to "stress check" the ADC.

1. Set controls as follows:

   HP 3311B Function Generator:

   FUNCTION: Square Wave
   REP RATE: 100 kHz
   AMPLITUDE: 0 to +3V peak



NOTE

You can measure this amplitude (p-p) by connecting the 3311B's output to the EXT.HORIZ.INPUT of the 5451C's oscilloscope.

5466B:

SAMPLE MODE: EXT
TRIGGER MODE: FREE RUN

2. Connect the 3311B's Pulse Output to a 5300/5303A Counter (to measure the 3311B's output frequency). Set the Counter's GATE TIME to 1 second. Allow the 3311B to operate for at least five minutes before measuring its frequency.

3. Record the 3311B's output frequency (as indicated by the Counter display), following the required five-minute (minimum) warm-up period for the 3311B.

4. Disconnect the Counter from the 3311B, then connect the 3311B's output to the 5466B's EXT. sample input connector.

5. Type QA RETURN.

6. Observe that the 5466B's TRIGGERING lamp blinks *dimly* (shade LED to observe blinking).

7. Type SA RETURN.

8. Set the Processor's "S"-register bit "15" to "1" ("on").
9. Connect the 5300/5303A Counter's input to the 5375A's rear-panel SAMPLE OUT connector (J21).
10. The frequency indicated by the counter now must be within 10 Hz of the frequency noted in step "2" of this procedure.

Remote Programming Test (Optional)

This test checks the Remote Programming codes that are transmitted between the Processor and the ADC. This test is required only when the 5475A is wired to enable remote control of the ADC (see Table 2-1).

1. Set 5466B controls as follows:

   SAMPLE MODE: REMOTE
   TRIGGER MODE: FREE RUN
   OVERLOAD VOLTAGE (all): 8V

2. Type SM RETURN
3. For four-channel ADC, only, set bit "14" to "1".
4. Set bit "15" to "1". The Remote Programming test routine will run, and then type "START" on the Teleprinter. If an error occurs, the Processor will HALT.

   In case of a Processor HALT during this test, refer to "SM" in the "Troubleshooting" section of the manual.

FOURIER SYSTEM AND PROCESSOR TEST

HP 54451A PROCESSOR TEST

This test checks the booster card and firmware card in the HP 54451A Processor. To perform the test, proceed as follows:

1. On HP 7900A Disc Drive Unit, set LOAD-UNLOAD switch to UNLOAD and wait for DOOR UNLOCKED indicator to light. On 7906A, set RUN/STOP switch to STOP and wait for the DOOR UNLOCK light to indicate.
2. Open door on Disc Drive Unit and insert system disc pack. For standard systems, use disc pack HP 54451-10001 (7900A) or 54451-10101 (7906A); for standard systems with Magnetic Tape Units, use disc pack HP 54451-10002 or 54451-10102.
3. On 7900, set LOAD-UNLOAD switch to LOAD and wait for DRIVE READY indicator to light. On 7906A, set RUN/STOP switch to RUN and wait for DOOR UNLOCK light.
4. On HP 54451A, load disc basic binary loader (NIBBL) as follows:

a. Press <Register Select> switch until S register is selected. Enter 101701_8 (7900A) or 111700 (7906A) in Display Register, then press STORE. Bits 6 through 11 are the select code for the disc — (standard) is 17 as given above).

b. Press PRESET, IBL, RUN.

c. Processor should halt at 102076_8.

5. To load the test, proceed as follows:
   a. Select S register, CLEAR DISPLAY, STORE.
   b. Set A register to 000000_8 and B register to 000031_8.
   c. Press STORE, PRESET, RUN.
   d. Processor should halt at 102077_8.
6. Press RUN.

7. Display Terminal should display as follows*:

```
54427A PROCESSOR TEST

ON SWITCH REGISTER:
SET BIT 0 TO LOAD WCS
SET BIT 1 TO SUPPRESS BASIC I/O TEST
SET BIT 2 TO SUPPRESS ROM TEST
SET BIT 3 TO SUPPRESS BOOSTER TEST
SET BIT 4 TO SUPPRESS DMA TEST
SET BIT 11 TO SUPPRESS TTY OUTPUT
SET BIT 12 TO IGNORE STANDARD HALTS
SET BIT 14 TO IGNORE ERROR HALTS
```

*All terminal printouts that refer to 54427A are also applicable to 54451 processors.

8. Processor should halt at 102011_8.

9. On Processor, press <Register Select> to S.

10. Set appropriate bits in the Display Register to run desired tests.

NOTE

In all cases, set bits 1 and 4 in the Display Register. Never set bit 0. The Load WCS, Basic I/O Test, and DMA Tests require special test fixtures and should not be used.

11. Press STORE, RUN. (Booster test requires about 2 minutes to complete).

12. To repeat test, press RUN.

13. To change test selections:

    a. Press <Register Select> to P
    b. Press CLEAR DISPLAY
    c. Set bit 1 in the display register
    d. Press STORE
    e. Press RUN

14. If the test results are not correct and an error occurs, refer to the troubleshooting section in this manual. When the ROM test is complete, the terminal should display:

```
1) TESTING DMS MICROCODE ROMS A1-A6 TEST #1 COMPLETED
2) TESTING SCDLD MICROCODE ROMS C1-C3 TEST #2 COMPLETED
3) TESTING SCDLD MICROCODE ROMS C4-C6 TEST #3 COMPLETED
4) TESTING SCDLD MICROCODE ROMS D1-D3 TEST #4 COMPLETED
5) TESTING SCDLD MICROCODE ROMS D4-D6 TEST #5 COMPLETED
```

15. When the Booster Test is complete, the terminal should display:

```
54427A BOOSTER TEST

BOOSTER ERRORS =
DMA ERRORS =
TOTAL I/O ERRORS =
TOTAL ROM ERRORS =
TOTAL BOOSTER ERRORS =
TOTAL DMA ERRORS =
END OF PROCESSOR PASS =
```

FOURIER SAMPLE RATE TEST

This test ensures correct operation of the ADC in the main Fourier program by setting certain sample rates and inserting corresponding known input signals.

1. Connect 3310B oscillator sinewave output through 51 ohm feedthrough to all 5466B INPUTs (A,B,C,D). Set DC OFFSET to 0V.

   Monitor the oscillator's amplitude, to maintain 0.6V rms output at all frequencies.

2. Enter a block size of 128 by pressing BLOCK SIZE, 1, 2, 8, and ENTER, in that order.

   BLOCK SIZE 128 lamp should light.

3. Enter into the record-taking mode by pressing ANALG IN, and ENTER, in that order.

4. Observe the Display Unit's oscilloscope for each combination of 5466B control settings given in Table 3-12.

Table 3-12. ADC Sample Rate Test

DISPLAY/INPUT		5466B Switches		Oscillator	CRT Display (Sinewave May not be centered on Screen)
Two Channel	Four Channel	SAMPLE MODE	MULTIPLIER	Frequency at .6V	
A/AB	A/ABCD B/ABCD	ΔFREQ/TOTAL TIME Hz/ms	10/20/50	20 Hz	1
B/AB	B/ABCD C/ABCD D/ABCD	ΔFREQ/TOTAL TIME Hz/ms	10/20/50	20 Hz	1
A/AB	A/ABCD B/ABCD C/ABCD D/ABCD	ΔFREQ/TOTAL TIME Hz/ms	2.5/5/200	10 Hz	2
A/AB B/AB	A/ABCD D/ABCD	ΔFREQ/TOTAL TIME Hz/ms	5/10/100	10 Hz	1
A/AB B/AB	A/ABCD D/ABCD	MAX FREQ/ΔTIME kHz/μs	1k/1/.5	7.8 Hz	1
A/AB B/AB	A/ABCD D/ABCD	MAX FREQ/ΔTIME Hz/ms	50/100/10	7.8 Hz	10*
NOTE: Set DISPLAY TYPE to CONT to view 10 cycles of waveform.					

5. Set controls as follows:

   Display Unit:

   Set MODE switch to REAL MAGNITUDE

   Keyboard:

   REPEAT/SINGLE:SINGLE

   5466B:

   SAMPLE MODE: ΔFREQ Hz/ms
   MULTIPLIER:5/10/100

   NOTE

   In the ΔFREQ mode, changing a BLOCK SIZE does not affect the total time required to take a single record (make one complete sweep); therefore, no change in the period of the input will be noted when changing block sizes.

6. Set sine wave oscillator frequency to 10 Hz.

7. Enter sweeping mode by pressing ANALG IN, and ENTER in that order.

   CRT displays one cycle of sine wave.

8. Repeat the above procedure for block sizes 64, 256, 512, and 1024.

   The CRT displays one cycle of sine wave at each block size.

9. If your system's Processor's memory is large enough to enable other block sizes (e.g., 2048, 4096), check those block sizes, too. If these sizes are not available, "WHAT" will light.

DUAL SPECTRUM SUBTRACT TEST

This test ensures that all channels in the ADC are matched, by subtracting one input from another.

1. Set controls as follows:

   5466B:

   SAMPLE MODE: INT, kHz/μs
   MULTIPLIER: 25/50/20
   DISPLAY: A
   INPUT: AB (for two-channel ADC)
   ABCD (for four-channel ADC)
   TRIGGER SOURCE: FREE RUN
   TRIGGER SLOPE: POS
   OVERLOAD VOLTAGE (all): .125V
   AC/DC (all): AC

   5475A:
   REPEAT/SINGLE: SINGLE

   5460A:
   DISPLAY TYPE: POINT

   Test Oscillator:
   Frequency: 10 kHz
   Amplitude: 200 mV p-p

2. Connect the Oscillator's output through a 50Ω load to all input channels of the 5466B.

3. Enter the following program via the HP 5475A Keyboard; Press ENTER after each step:

```
REPLACE 0
LABEL 10
BLOCK SIZE 1024
JUMP -1
MINUS 1
POLAR 0
DSPLY 0
JUMP 10
LABEL 11
JUMP -1
LOAD 1
MINUS 2
POLAR 0
DSPLY 0
JUMP 11
LABEL 12
JUMP -1
LOAD 2
MINUS 3
POLAR 0
DSPLY 0
JUMP 12

LABEL -1
ANALG IN
F (Fourier) 01
F (Fourier) 23
SUB RTRN
END
TERM
```

LIST (Check that printout is as shown on following page)

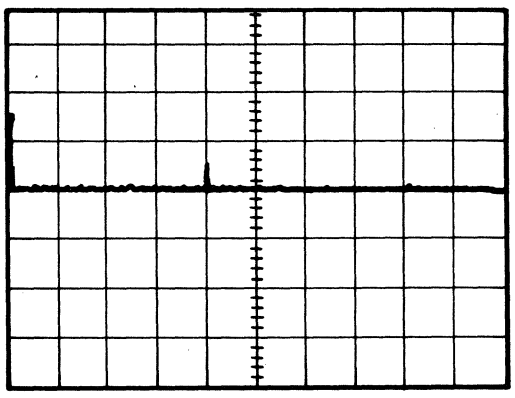
```
  1 L        10
  5 BS     1024
  9 J        -1
 13 A-         1
 17 TP         0
 21 D          0
 25 J         10
 29 L         11
 33 J         -1
 37 X<         1
 41 A-         2
 45 TP         0
 49 D          0
 53 J         11
 57 L         12
 61 J         -1
 65 X<         2
 69 A-         3
 73 TP         0
 77 D          0
 81 J         12
 85 L         -1
 89 RA
 92 F          0        1
 97 F          2        3
102 <
105 .
```

4. Enter the following command, via the 5475A's keyboard:

   JUMP 10 ENTER

   You should see a display like the one shown below. The maximum output voltage displayed must be less than or equal to $\pm 2 \times 10^{-4}$V. Disregard the left-most point in the display. This point is the dc component, and does not affect dynamic measurements. To correctly interpret the display, multiply the number of cm deflection on the CRT by the scale factor given by the digital display tubes.

   This test compares channels A and B.



5. Set all OVERLOAD VOLTAGE switches to 1V.

6. Adjust Test Oscillator for 10 kHz, 1.5V p-p output.

7. On 5475A Keyboard, enter JUMP 11 ENTER.

8. 5460A display should be similar to the illustration in step 4. The maximum output voltage displayed must be less than or equal to $\pm 2 \times 10^{-3}$V. This compares channels B and C.

9. Set all OVERLOAD VOLTAGE switches to 8V.

10. Adjust Test Oscillator for 10 kHz, 9V p-p output.

11. On 5475A Keyboard, enter JUMP 12 ENTER.

12. 5460A display should be similar to the illustration in step 4. The maximum output voltage displayed must be less than or equal to $\pm 2 \times 10^{-2}$V. This compares channels C and D.

ADC DIGITIZER TEST

1. Connect Function Generator output to Channel A of the 5466B.

2. Connect the sync output of the Function Generator to the 5466B's TRIGGER INPUT.

3. Set controls as follows:

   Function generator:

   FREQUENCY: 400 Hz
   FUNCTION: TRIANGLE

   5466B:

   SAMPLE MODE: INT, kHz/μs
   MULTIPLIER: 50/100/10
   DISPLAY/INPUT (2-channel): A/AB
   DISPLAY (4-CHANNEL): A
   INPUT (4-channel): ABCD
   OVERLOAD VOLTAGE (all): 8
   AC/DC (all): DC
   TRIGGER MODE: EXT. AC
   TRIGGER SLOPE: NEG

   Keyboard:

   SINGLE/REPEAT: REPEAT

4. Press BLOCK SIZE, 256, ENTER.

5. Press ANALG IN, ENTER.

6. The 5466B's TRIGGERING lamp should be blinking.

7. Approximately one cycle of a triangle wave should appear on the display oscilloscope. Adjust 5466B's TRIGGER LEVEL FOR display shown in Figure 3-1.

8. Adjust the Function Generator AMPLITUDE control until the 5466B's OVERLOAD lamp just starts to blink.

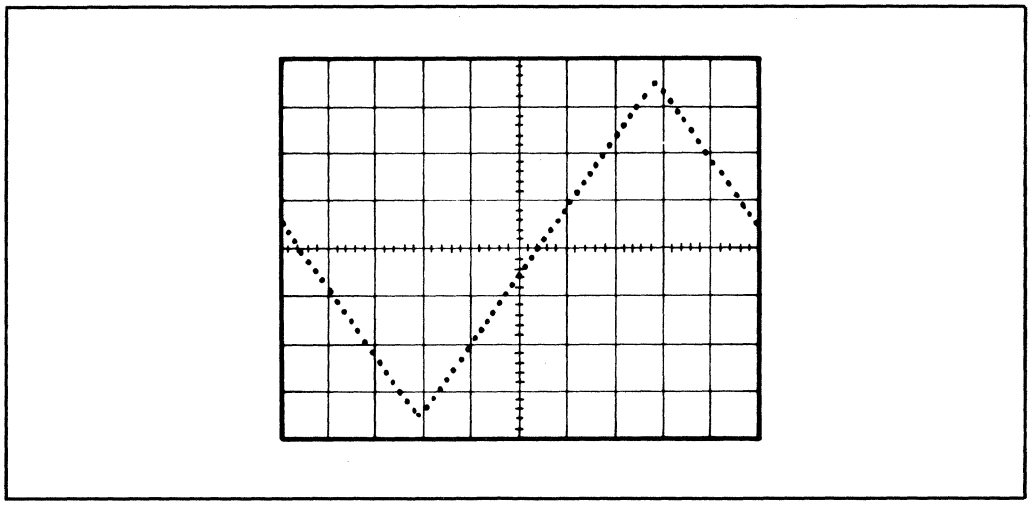
9. Move the Keyboard's SINGLE/REPEAT switch to SINGLE.

   All points of the waveform should be continuous, without missing levels or severe nonlinearities. The waveform should appear approximately like the one represented in Figure 3-1.

10. Set Keyboard's SINGLE/REPEAT switch to REPEAT, press ANALOG IN, ENTER.

11. Repeat the above procedure for the remaining ADC channels as follows:
    a. Disconnect the triangular signal from its current input, and connect it to the next higher channel.
    b. Set the INPUT SELECTOR and DISPLAY switches to the channel currently receiving the triangle input. The triangle wave should be displayed.

Figure 3-1. Triangle Waveform



ADJUSTMENTS

Adjustments and calibration for the 5460A Display Unit, 5466B ADC, and the 5475A Control Unit are contained in the following paragraphs. Table 3-13 summarizes the adjustments for each unit. Do not perform any adjustments not listed in the Table. Always remove power before removing or replacing any system units or circuit boards.

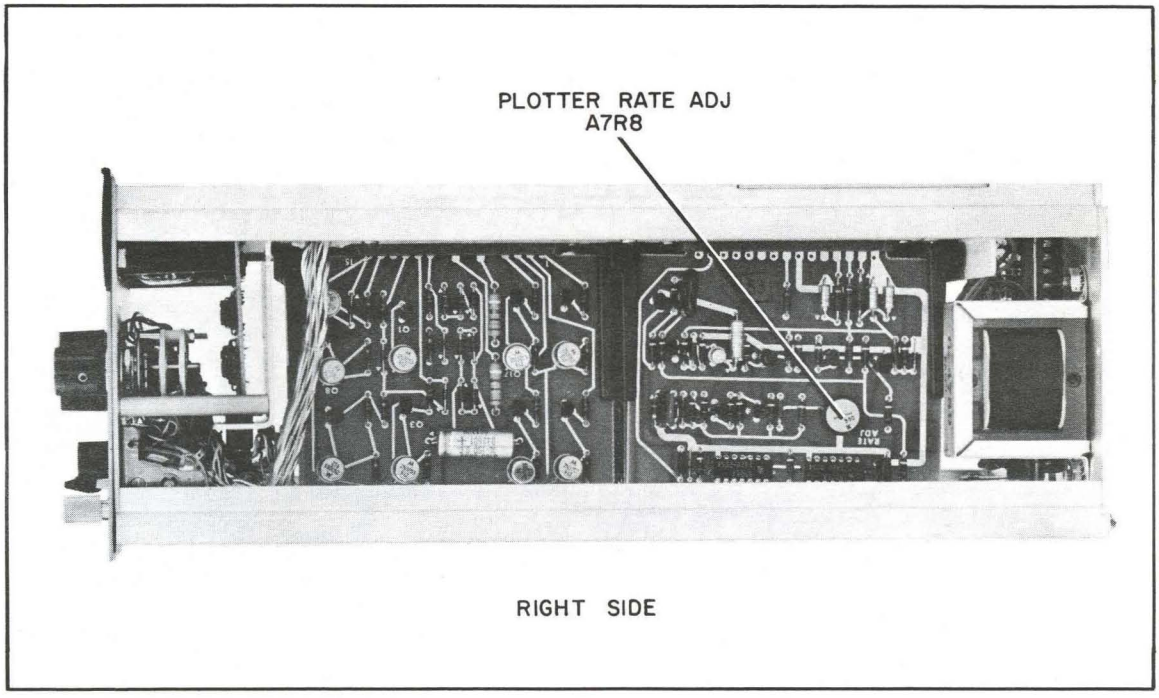
Table 3-13. Adjustments Procedures

UNIT	PROCEDURE
Display Unit	Bus Voltage Measurement Reference Voltage Adjustments Horizontal DAC Output Voltage Adjustments Horizontal CRT Gain Adjustments Vertical DAC Output Voltage Adjustments Vertical CRT Gain Calibration
ADC	A1 (and A2) Input Assembly Adjustments (DC Offset Adjustments) A3, A5 (and A4, A6) Digitizer Assembly Adjustments (DC Offset Adjustment) A10 Sample Generator Assembly Adjustments a. Adjust 20.00 MHz Crystal Oscillator. b. Adjust 8.192 MHz Crystal Oscillator.
Control Unit	Power Supply Adjustments a. Preliminary Instructions b. Voltage Adjustments c. Overcurrent Control Adjustment Oscillator Adjustment

DISPLAY UNIT ADJUSTMENT

The procedures required that the 5460A plug-in be removed from the oscilloscope mainframe and its top and bottom covers removed. The 5460A is assumed connected to the oscilloscope through the Display Service Extender (05451-60071). Refer to Section 1 of this manual for detailed access information. See Figure 3-2a for physical location of test points.

Figure 3-2a. Display Unit Test Points



Equipment Required

The following equipment or the equivalent is required to perform these procedures:

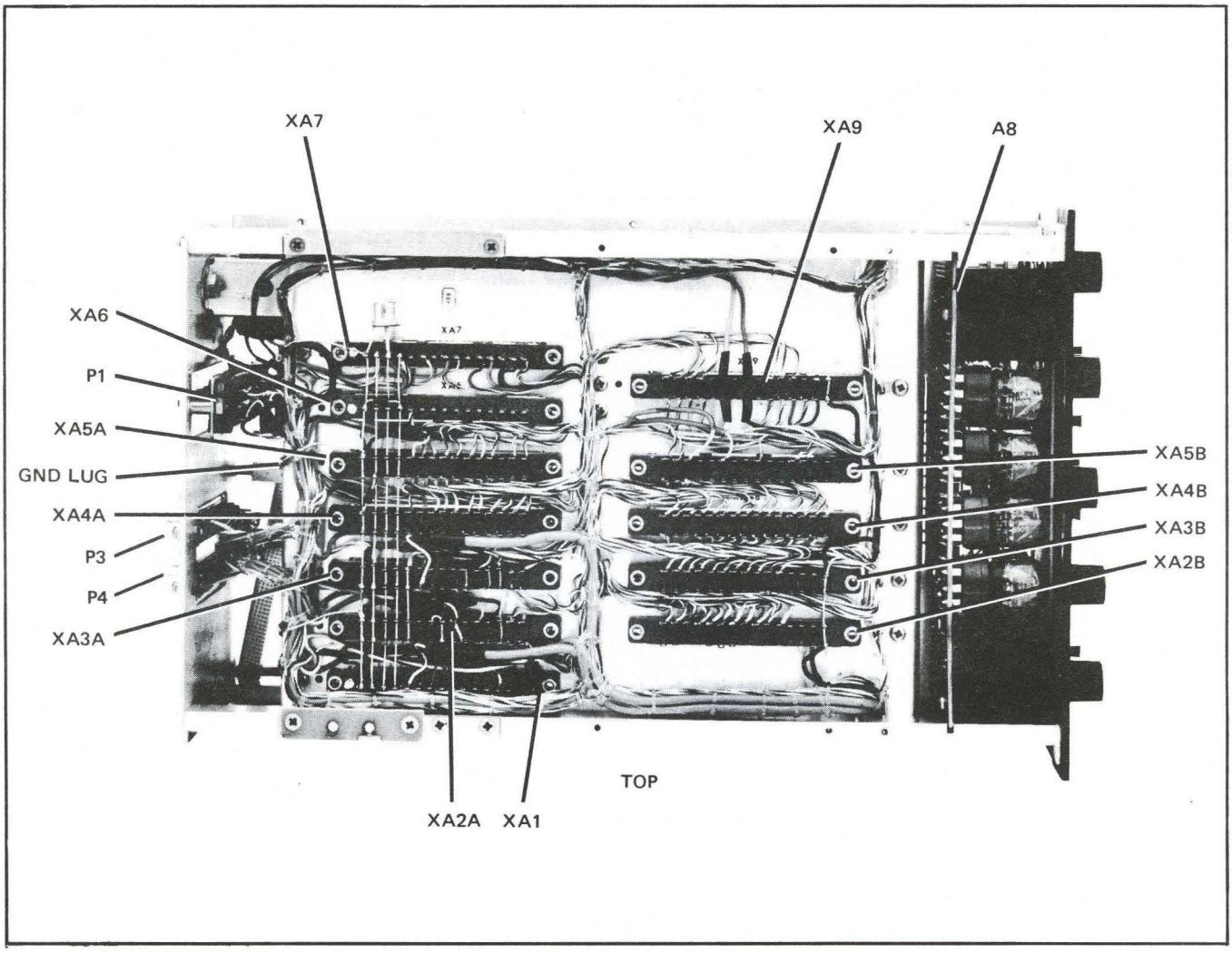
HP Model 5306B Voltmeter
Short Clip Lead
Service Extender Kit 05451-60071

Bus Voltage Measurements

The voltage readings listed below are those for normally operating power supplies. There are no voltage adjustments for these supplies in the 5460A unit. Refer to Control Unit adjustments and oscilloscope manual for adjustments. See Figure 3-2b for test point locations.

Test Point (all in 5460A)	Voltage (with respect to ground)
XA1(15)	+95V to +105V
XA8(15,S)	+165V to +180V
XA1(4)	+14.5V to +15.5V
XA1(3)	-12V to -13V
XA1(2)	+4.5V to +5.5V
XA8(2,B)	+4.5V to +5.5V
XA8(K)	+22V to +25V

Figure 3-2b. Display Unit Test Points (continued)



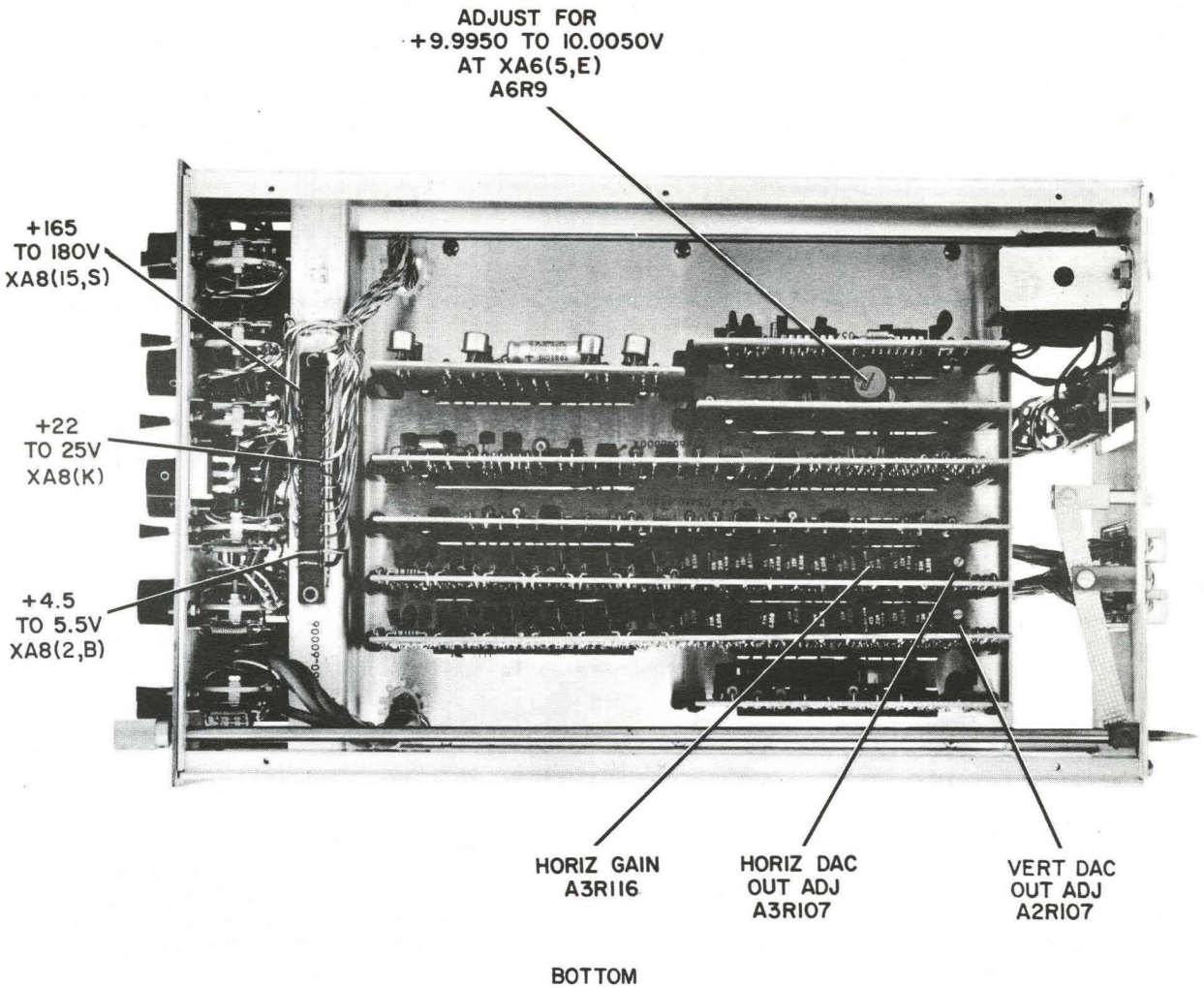
Reference Voltage Adjustment

1. Connect Digital Voltmeter (DVM) positive lead to XA6(5,E).
2. Voltage between XA6(5,E) and ground must be +9.9950V to +10.0050V.
3. Adjust A6R9, if necessary, to bring voltage within specified range. See Figure 3-2C for adjustment locations.

Horizontal DAC Output Voltage Adjustment

1. Connect DVM positive lead to oscilloscope rear-panel "X" output connector center conductor.
2. Set 5460A DISPLAY CALIBRATE to +FS.
3. Set 5460A DISPLAY FUNCTION to CAL.
4. DVM should read +2.5025V to +2.5050V.
5. If DVM reading is not correct, adjust 5460A A3R107 as required.

Figure 3-2c. Display Unit Test Points (continued)



Horizontal CRT Gain Adjustment

1. Set 5460A DISPLAY CALIBRATE to ORIGIN, DISPLAY FUNCTION to CAL.
2. Adjust oscilloscope HORIZONTAL POSITION for dot on vertical line at left-hand edge of graticule.
3. Set 5460A DISPLAY CALIBRATE to +FS.
4. Adjust 5460A A3R116 to place dot on center vertical line of graticule.
5. Repeat steps 1 through 4 above until A3R116 requires no further adjustment.

Vertical DAC Output Voltage Adjustment

1. Connect DVM positive lead to oscilloscope rear-panel "Y" output connector center conductor.
2. Set 5460A DISPLAY FUNCTION to CAL.

3. Set 5460A DISPLAY CALIBRATE to +FS.
4. Connect 5460A XA2A(12) to chassis.
5. DVM must indicate +4.0060V to +4.0100V.
6. If DVM reading is not within specification, adjust 5460A A2R107.
7. Remove clip lead from XA2(12).

Vertical CRT Gain Calibration

1. Set 5460A DISPLAY CALIBRATE switch to ORIGIN and DISPLAY FUNCTION to CAL.
2. Adjust 5460A VERTICAL POSITION to center dot on vertical line at left-hand edge of CRT graticule.
3. Set 5460A DISPLAY CALIBRATE switch to +FS.
4. Adjust 5460A VERTICAL CAL (front panel) to position dot on upper horizontal line of CRT graticule.
5. Set 5460A DISPLAY CALIBRATE to -FS. Dot should appear on lower horizontal line of CRT graticule.

CONTROL UNIT ADJUSTMENTS

Equipment Required

The following equipment or equivalent is required to perform these procedures:

HP Model 5306B Voltmeter
HP Model 5300A/5303A Counter
Short Clip Lead

Power Supply Adjustments

The Model 5475A power supplies should not normally require adjustment. However, the replacement of a malfunctioning component or long-term component aging may cause the Model 5475A to become out-of-adjustment. All power supply adjustments are on the regulator board assemblies.

The dc output voltages from the power supply regulator board assemblies are independent of each other. Therefore, when you are adjusting any one supply, it is not necessary that you check or adjust any other supply.

When adjusting any supply, you must make the voltage adjustment before you make the overcurrent adjustment.

If you are adjusting more than one supply, you can make all voltage adjustments first, then go back and make all overcurrent adjustments.

NOTE

While performing adjustments, the regulator board assemblies must be seated in their respective connectors and not on an extender board assembly. Stray inductance can induce oscillations when the board assembly is extended.

PRELIMINARY INSTRUCTIONS

The preliminary instructions are to be performed prior to any adjustments.

1. Remove 5466B plug-in from 5475A mainframe.

2. Adjust overcurrent control potentiometers associated with power supplies being adjusted to center of their travel (see Figure 3-3).

NOTE

The following list provides a quick-reference to locations of overcurrent control and voltage control potentiometers (see Figure 3-3).

a. Overcurrent control adjustments:

Negative: Extreme left of board, extreme rear of instrument.
Positive: Extreme right of board, extreme front of power supply section.

b. Voltage adjustments:

Negative: Second from left on board, second from rear of instrument.
Positive: Third from left on board, third from rear of instrument.

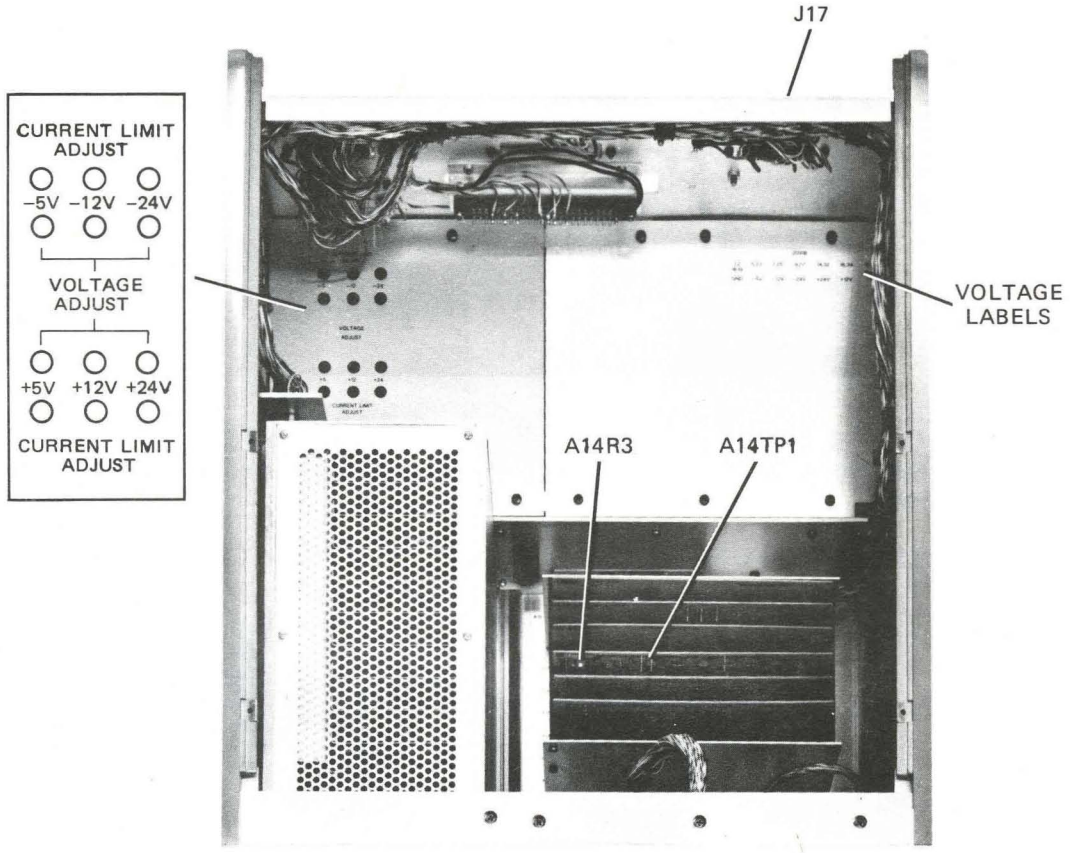
c. Assemblies

±24V: A4
±12V: A5
±5V: A6

3. Connect Digital Voltmeter (DVM) across pin number indicated and ground of first dc output voltage to be adjusted.

4. Turn on cabinet power and 5475A power.

Figure 3-3. Control Unit Test Points



+24V - J17(14,32) and ground*
–24V - J17(9,27) and ground*
+12V - J17(16,34) and ground*
–12V - J17(7,25) and ground*
+5V - J17(18,36) and ground*
–5V - J17(5,23) and ground*
*ground connections are J17(1,2,19,20)

VOLTAGE ADJUSTMENTS

To adjust any of the dc output voltages, perform the following procedures for the associated supply:

1. Perform preliminary instructions listed in the preceding paragraph.
2. Adjust associated voltage potentiometer for nearest value displayed on DVM to designated magnitude. Value displayed shall be within ± 0.5 percent of designated magnitude.
3. Repeat step 2 for each additional dc output voltage to be adjusted.
4. Disconnect all test equipment.

OVERCURRENT CONTROL ADJUSTMENT

To establish the point at which overcurrent from a supply is sensed, perform the following procedure:

NOTE

The 5475 must be connected to the display unit, and the 5466 plug-in must be installed, as required for normal system operation.

1. Be sure that the voltage adjustment for the power supply has been performed as described in the "Voltage Adjustments" paragraph above.
2. Adjust the overcurrent control for one supply until the 5475A's rear-panel OVERLOAD indicator lights; next back off the adjustment until the OVERLOAD indicator turns off, then turn the control an additional 90 degrees in the same direction (or until the limit of rotation is reached, whichever occurs first).
3. Perform steps "1" and "2" above for each additional power supply that is to have its overload control setting adjusted.

Oscillator Adjustment

This procedure synchronizes the shift register clock rate with the clock rate of the Display Terminal and the Display Terminal I/O card in the computer. The oscillator is located on the shift register board A14 (05475-60204).

1. Connect Model 5300A/5303A Counter leads between A14 test pins TP1 and TP4 (ground). See Figure 3-3. (Connect 1 kΩ resistor in series with TP1 counter lead to reduce cable capacitance effect on oscillator frequency.)
2. Adjust A14R3 potentiometer (Figure 3-3) so period of signal at TP1 is 1.1 ± 0.005 msec.

ADC ADJUSTMENTS

Before making any adjustments on the 5466B, be very sure that adjustment is needed, and that the 5475A power supply adjustments have been completed.

CAUTION

When connecting the 10628A Extender Cable, be sure to connect P15A on the 5466B to J15 in the rack. These connectors are located nearest to the outside of the rack. Failure to comply may result in damage to the 5466B.

The adjustment procedures require that the 5466B plug-in be removed from the 5475A Control unit, and that its right-hand side cover be removed. The 5466B is assumed to be connected to the 5475A through the HP 10628A Service Extender Cable. Connect the extender cable from P15A of the 5466B to J15 in the rack. Refer to Section 1 of this manual for detailed access information.

Equipment Required

The following equipment, or its equivalent, is required to perform these procedures:

HP Model 3470A Digital Voltmeter
HP Model 1707A Oscilloscope
HP Model 5300/5301 Electronic Counter
HP Model 3311B Function Generator
HP Model 6615A Precision Power Supply
HP Model 10628A Service Extender Cable

NOTE

These adjustments require use of the ADC Test Program. Enter the program by loading the System Diagnostic Tape, and typing SA, RETURN.

A1 (and A2) Input Assembly Adjustments (05466-60001 or 05466-60013)

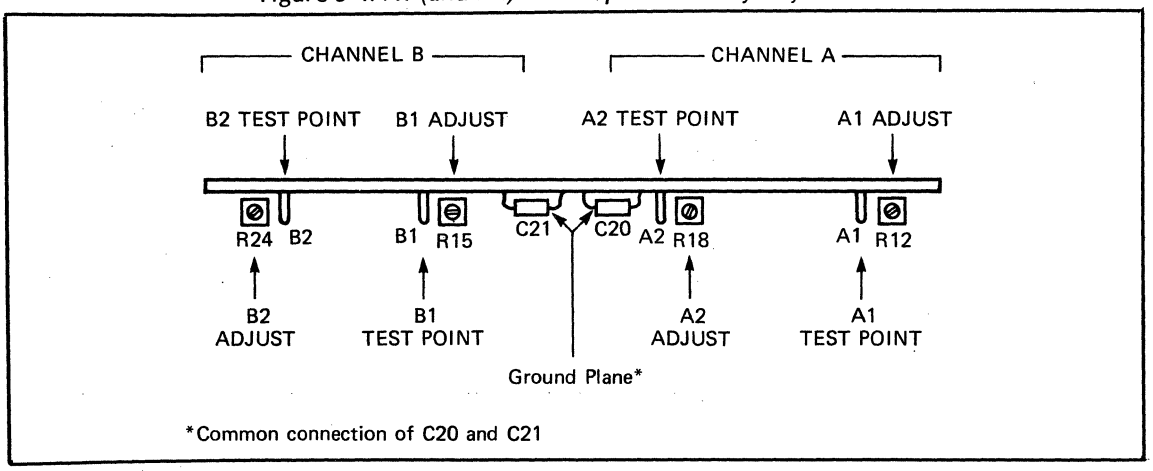
NOTE

Perform Power Supply Adjustments before proceeding.

CHANNEL A DC OFFSET

1. On A1 board, connect test lead from Digital Voltmeter to Test Point A2 ("TP A2") (see Figure 3-4).

Figure 3-4. A1 (and A2) ADC Input Assembly Adjustments



2. Connect the Voltmeter's Ground lead to ground on the board under test. (The best way to do this is to connect it to any component lead that is connected to the board's ground plane.)

3. Connect a 50-ohm terminatation BNC to the Channel A INPUT. Set the Channel A OVERLOAD VOLTAGE switch to ".125".

4. Set the AC/DC switch to DC.

5. The DC offset, measured by the DVM connected to Test Point A, should be less than ± 1.5 mV for all Channel A OVERLOAD VOLTAGE switch settings from ".125" to "1", and less than ± 5 mV for "2", "4" and "8". If all values are correct, go to Channel B dc offset, otherwise do "6" through "12" below.

6. Disconnect the DVM from TP A2, and connect the DVM to TP A1.

7. Set the Channel A OVERLOAD VOLTAGE switch to ".125".

8. Adjust R12 (next to Test Point A1) for a DVM reading of 0.0 ± 0.5 mV.

9. Disconnect the DVM from TP A1 and connect the DVM to TP A2.

10. Set the Channel A OVERLOAD VOLTAGE switch to "8".

11. Adjust R18 (next to Test Point A2) for a DVM reading of 0.0 ± 1 mV.

12. Repeat step "5".

CHANNEL B DC OFFSET

NOTE

If a voltmeter other than the one specified is used, the amplifier may oscillate at some OVERLOAD VOLTAGE settings. Oscillation can be eliminated by connecting a 1000-ohm resistor in series with the test lead.

1. On A1 board, connect test lead from Digital Voltmeter to Test Point B2 ("TP B2").

2. Connect a 50-ohm termination BNC to the Channel B INPUT. Set the Channel B OVERLOAD VOLTAGE switch to ".125".

3. Set the AC/DC switch to DC.

4. The DC offset, measured by the DVM connected to Test Point B2, should be less than ± 1.5 mV for all Channel B OVERLOAD VOLTAGE switch settings from ".125" to "1", and less than ±5 mV for "2", "4", and "8".

   If all values are correct, and —

   a. Yours is a 2-channel ADC: Go to A3, A5 (and A4, A6) Digitizer Adjustments and Calibration.

   b. Yours is a 4-channel ADC:

      1) Repeat Channel A dc offset on board assembly A2 for Channel C,

      2) Perform this procedure on board assembly A2 for Channel D, then go to A3, A5 (and A4, A6) Digitizer Adjustments and Calibration.

   Otherwise, perform steps "5" through "11".

5. Disconnect the DVM from TP B2 and connect the DVM to TP B1.

6. Set the Channel B OVERLOAD VOLTAGE switch to ".125".

7. Adjust R15 (next to TP B1) for a DC offset of 0.0 ± 0.5 mV.

8. Disconnect the DVM from TP B1 and connect the DVM to TP B2.

9. Set the Channel B OVERLOAD VOLTAGE switch to "8".

10. Adjust R24 (next to Test Point B2) for a DVM reading of 0.0 ± 1 mV.

11. Repeat step "4".

A3, A5 (and A4, A6) Digitizer Adjustments and Calibration

NOTE

Several different Digitizer Board assemblies are available for use in the 5466B. The adjustment procedures on these differ, too. The chart below indicates which procedure(s) should be used for adjusting a particular Digitizer Board assembly. Be sure to use the correct procedure(s) for the Digitizer Board assemblies in your 5466B.

Digitizer Adjustment Procedure Selection

HP Part Number of Digitizer Board Assembly	Procedure Description
05466-60002	10-bit, 200 kHz Samp. Rate
05466-60007	12-bit, 200 kHz Samp. Rate
05466-60014	12-bit, 100 kHz Samp. Rate

SAMPLE-AND-HOLD MODULE DC OFFSET ADJUSTMENT (200 kHz DIGITIZERS ONLY)

1. Set all OVERLOAD VOLTAGE switches to ".125".
2. Connect the 50-ohm termination to the 5466B's Channel A INPUT.
3. Connect the test lead from the Digital Voltmeter to test point A2 on the A1 board. DVM should read the DC offset voltage, 0.0 ± 1.5 mV; if not, perform Channel A dc offset of this adjustment procedure.
4. Connect the DVM test lead to A3 test point "S and H" (for "Sample and Hold"). (See Figure 3-5.)
5. Adjust A3R1 for DVM reading of 0.0 ± 1.5 mV.
6. Perform steps "1" through "5" above for 5466B Board Assembly A5 (and A4 and A6, if installed).

NOTE

In step "3" above, use A1 test point B2 for Channel B, A2 test point A2 for Channel C, A2 test point B2 for Channel D.

In step "4" above, use A5 for Channel B, A4 for Channel C, A6 for Channel D.

SAMPLE/HOLD ADJUSTMENTS (100 kHz DIGITIZERS ONLY)

NOTE

These adjustments require use of the ADC Test Program. Enter the Program by loading the System Diagnostic and typing SA, RETURN.

1. On Processor, set bit 15 to ON.
2. Set 5466B controls as follows:

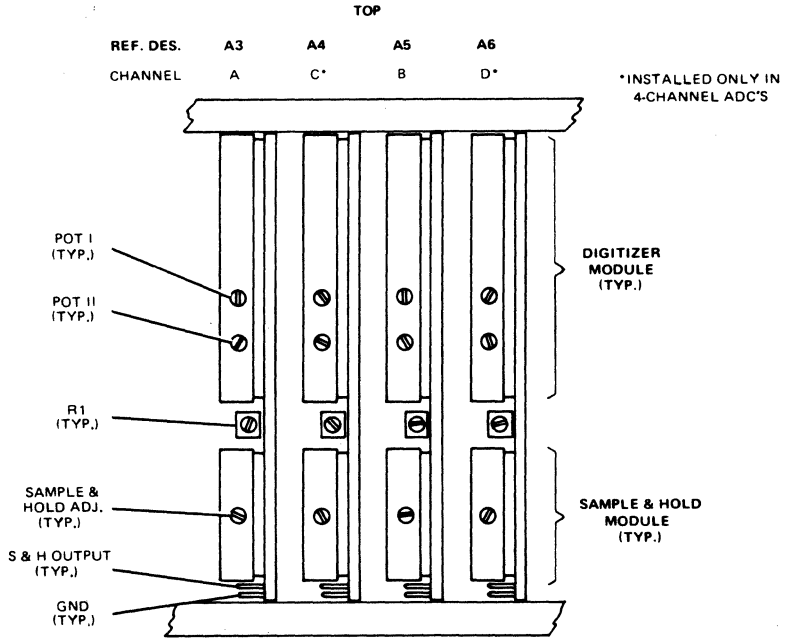
   OVERLOAD VOLTAGE switches to ".125".
   SAMPLE MODE to kHz μsec
   MULTIPLIER to 50/100/10
   TRIGGER to FREE RUN

3. Connect a 50-ohm termination to 5466B Channel A INPUT.

CAUTION

Do not connect a ground lead to the ground plane near the extractor ring on A3 through A6. A ground on the pc lead just above the ground plane will damage transistors Q9 and Q10.

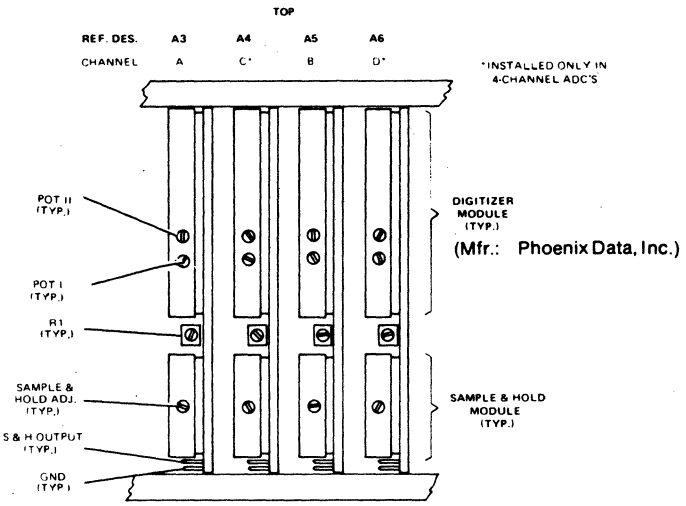
Figure 3-5. A3, A5 (and A4, A6) Digitizer Adjustments
(for 10-bit or 12-bit 200 kHz Digitizers)



NOTE

Some 05466-60007 (12-bit, 200 kHz) Digitizer Boards may have a digitizer module whose adjustments are "reversed" from those indicated in the diagram above. These modules are electrically identical to the one illustrated above, and have the same HP Part Number. They are made by Phoenix Data Inc, and have adjustment locations as illustrated below.

As an additional note, an error exists on the stick-on label on some of the Phoenix Data Inc. digitizer modules. The ANA IN pin is really pin "28", even though the label may indicate that the ANA IN is pin "29".



4. Using 1:1 probe, connect Oscilloscopes Channel A to "S/H OUT" test point on A3 board. Connect probe ground clip to ground plane on A2 pc board.

5. Using 1:1 probe, connect Oscilloscope's EXT TRIG to "SAMP" test point on A10 board. Connect probe ground clip to GND test point on A10.

6. Connect a ground clip from the 5466B chassis to Oscilloscope chassis.

7. Set Oscilloscope controls as follows:

   TRIGGER to EXTERNAL MINUS
   SWEEP RATE to 5 μSEC/DIV
   CHANNEL A attenuator to .02V/DIV

   The waveform may resemble that shown in Figure 3-5b below.

8. If necessary, adjust the "Pedestal Adjust' capacitor (see Figure 3-5a) to make the displayed waveform as straight a line as possible (see Figure 3-5c). The X10 sweep magnifier may be used for easier viewing.

9. Disconnect the Oscilloscope's probe from the "S/H OUT" test point.

10. Connect the Digital Voltmeter's negative lead to the A2 board's ground.

11. Connect the Digital Voltmeter's positive lead to the A3 board's "S/H OUT" test point.

12. Adjust the "Zero Adjust" resistor (see Figure 3-5a) to make the Digital Voltmeter's reading as close to zero as possible. (The final reading must be within ± 2 mV of 0V.)

13. Remove the 50-ohm termination from the Channel A INPUT.

14. Set the Channel A OVERLOAD VOLTAGE to "8V".

15. Set the DC Standard's VOLTAGE SET for +8.000 volts.

16. Connect the DC Standard to the ADC's Channel A input.

17. Adjust the A3 board's "S/H GAIN" pot until the DC voltage measured at the "S/H OUT" pin is between +4.998V and +5.002V.

18. Repeat procedure for Channel B (A5 board), Channel C (A4 board) and Channel D (A6).

Digitizer Module DC Offset Adjustment (All Digitizers)

1. Perform the sample-and-hold adjustments required by the board you are working on, using the appropriate procedures presented in the preceding paragraphs.

2. Type QA, RETURN, on the Display Terminal, to enter the "Query ADC" routine.

3. Set ADC controls as follows:

   SAMPLE MODE: INT kHz
   TRIGGER SOURCE: FREE RUN
   OVERLOAD VOLTAGE (all): 8
   INPUT SELECTOR (2-channel): AB or to ABCD (4 channel ADC's).
   DISPLAY (4-channel): A

Figure 3-5a. Adjustment Locations — 100 kHz Digitizer

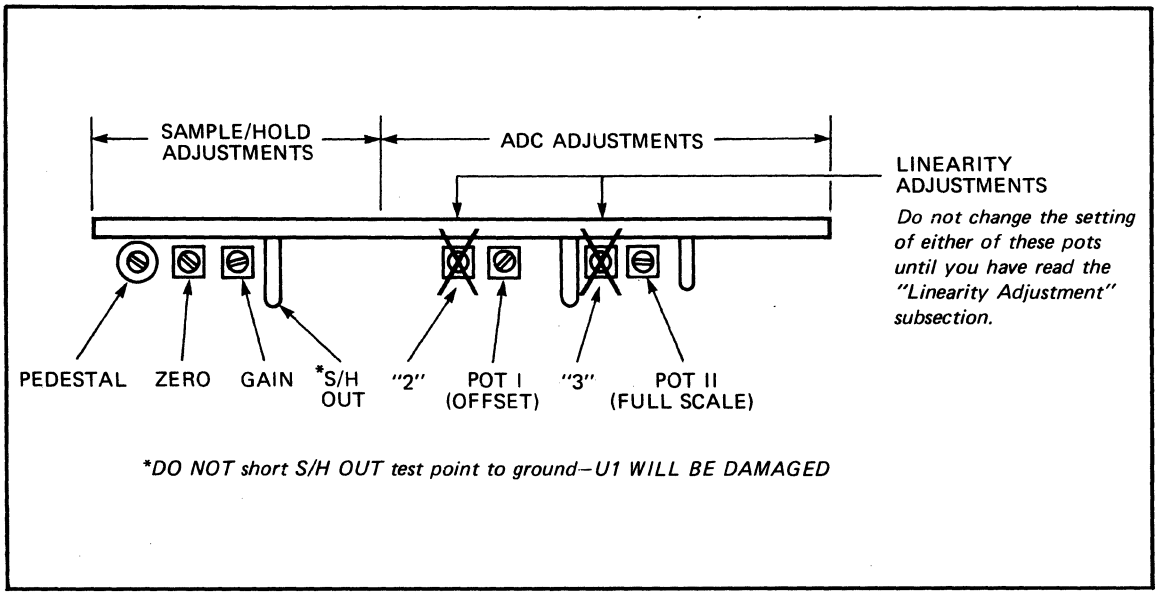


Figure 3-5b. Pedestal Adjustment Waveform Number 1

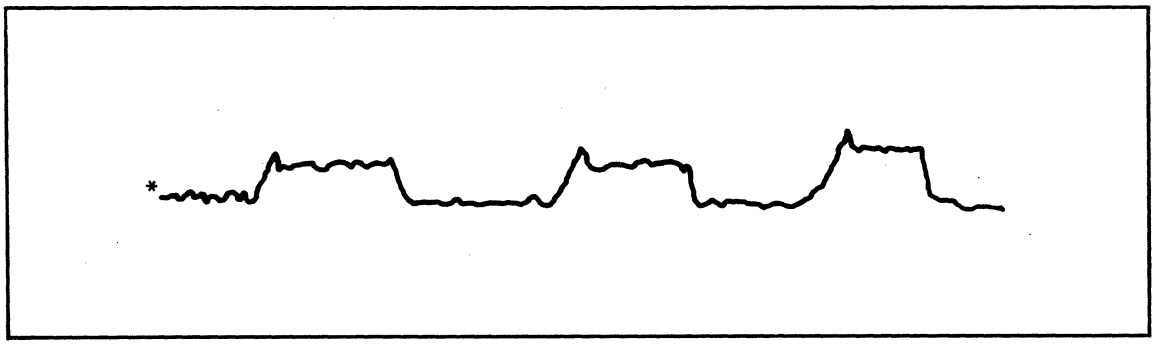
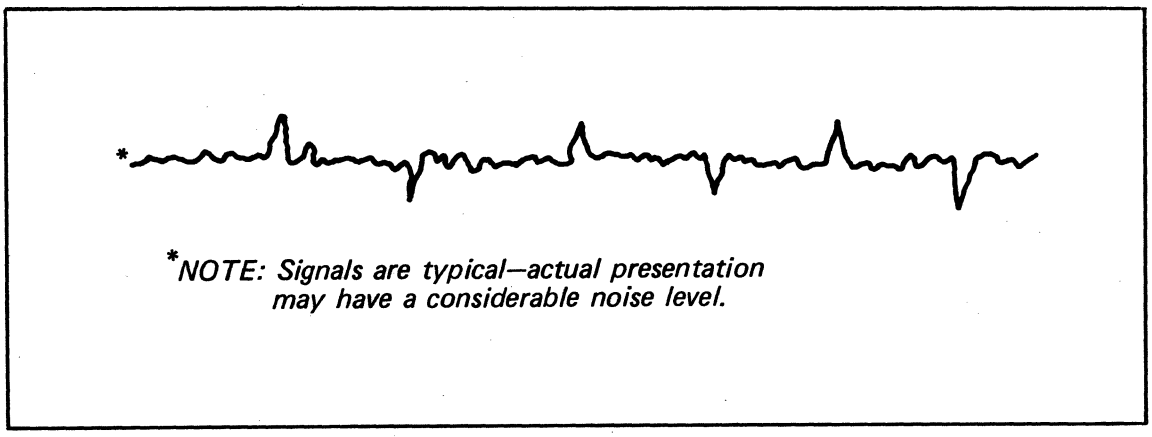


Figure 3-5c. Pedestal Adjustment Waveform Number 2



4. Connect 50-ohm load to Channel A INPUT.

5. Set Processor's switch register bit "10" to "1". If a 12-bit ADC is installed also set bit "15" to "1".

6. Adjust A3's "POT I" (see Figure 3-5 or 3-5a) for a reading of "000" ± "2" on the 5460A Display Unit's digital indicator tubes.

7. Remove the 50-ohm termination.

8. Repeat procedure with DISPLAY switch set to B and adjust A5's POT I. Connect the 50-ohm termination to channel B input.

9. Repeat procedure with DISPLAY switch set to C and adjust A4's POT I. Connect the 50-ohm termination to CHANNEL C INPUT.

10. Repeat procedure with DISPLAY switch set to D and adjust A6's POT I. Connect the 50-ohm termination to CHANNEL D INPUT.

DIGITIZER GAIN CALIBRATION (ALL DIGITIZERS)

NOTE

The DC Offset procedure above should be performed for the Digitizer Board assembly before you perform this calibration procedure.

1. Set all OVERLOAD VOLTAGE switches to "8".

2. Set the HP 6115A Precision Power Supply for 7.0000V output.

3. Set DISPLAY selector to "A".

4. Connect the 6115A's output to the 5466B's Channel A INPUT.

5. Adjust A3's "POT II" for the correct 5460A indication, as given below for your digitizer.

   10-bit: "448" ± "2"
   12-bit: "1792" ± "2"

6. Check ADC Channel linearity by setting the 6115A'S output level as indicated in Table 3-14, and checking the 5460A display for that voltage. The table includes a place to record the actual values you observe.

Table 3-14. ADC Channel Linearity Check

	5460A Display					
	Specification (See Note)		Actual			
CHANNEL INPUT (VOLTS) (6115A Output)	10-bit	12-bit	Channel A	Channel B	Channel C	Channel D
0.0	000 ± 2	000 ± 4	_____	_____	_____	_____
1.0	064 ± 2	256 ± 4	_____	_____	_____	_____
2.0	128 ± 2	512 ± 4	_____	_____	_____	_____
3.0	192 ± 2	768 ± 4	_____	_____	_____	_____
4.0	256 ± 2	†1024 ± 4	_____	_____	_____	_____
5.0	320 ± 2	†1280 ± 4	_____	_____	_____	_____
6.0	384 ± 2	†1536 ± 4	_____	_____	_____	_____
7.0	448 ± 2	†1792 ± 4	_____	_____	_____	_____

†The "1" is displayed with an annunciator and the last three digits are displayed on the NIXIE tubes.

NOTES:

1. In addition to the "Specifications" given above, the following linearity "spec" also applies: For any one volt *change* in INPUT signal level for any channel, the *change* in output (indicated on the 5460A Display Unit's tubes) must be:

   64 ± 1, for a 10-bit digitizer
   256 ± 2, for a 12-bit digitizer

2. If necessary, linearity of 100 kHz Digitizers can be adjusted, using the procedure presented below.

This completes the Digitizer Board Assembly adjustments for Channel A (Board Assembly A3). Perform the procedures for Channel B (Board Assembly A5) and, if yours is a four-channel ADC, for Channel C (Board Assembly A4) and Channel D (Board Assembly A6). For a two-channel plug-in, be sure to set the INPUT SELECTOR switch to B and AB respectively when you check Channel B. For a four channel plug-in, set the INPUT switch to "ABCD", and the DISPLAY switch to "B", "C", or "D", corresponding to the channel you are adjusting.

INTERNAL LINEARITY ADJUSTMENT (100 kHz DIGITIZERS ONLY)

NOTE

You should perform this procedure only if you have performed the ADC adjustment procedures for the 100 kHz Digitizer Board assembly, and the board did not pass the linearity check procedure.

The linearity adjustment is performed at the factory. We expect that the only time it will be necessary to perform this adjustment in the field is if the resistor array (R22) or any of the current switches (U5, U7, U10) is damaged or replaced, or if the setting of either one of the linearity adjust resistors is changed.

1. Enter the command QA RETURN via the Display Terminal.
2. Set bit 15 of the Processor's "S" register (to "1").
3. Connect the DC Standard to the 5466B's Channel A input.
4. Set the DC Standard's VOLTAGE SET for -8.0000V output.
5. Set the 5466B's DISPLAY to "A".
6. Adjust the A3 ADC's POT I (OFFSET) to make the 5460A's reading "-2047".
7. Set the DC Standard's VOLTAGE SET for +7.0000V output.
8. Adjust A3's POT II (FULL SCALE) to make the 5460A's reading "+1792".
9. Set the DC Standard's VOLTAGE SET for -7.0626V output.
10. Adjust A3's "2" Linearity Adjustment pot to make the 5460A's reading "-1808".
11. Set the DC Standard's VOLTAGE SET for -7.9414V out.
12. Adjust A3's '3' Linearity Adjustment pot to make the 5460A's reading "-2033".
13. Set the DC Standard's VOLTAGE SET for +8.0000V output.
14. Adjust A3's POT II (FULL SCALE) to make the 5460A's reading "+2047".

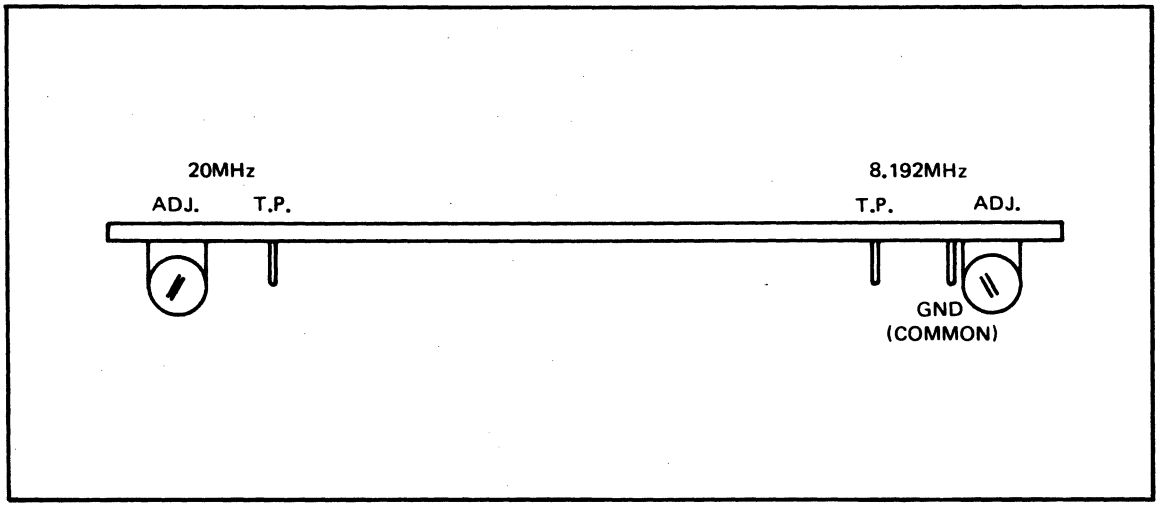
NOTE

To perform the procedures of this subsection for other channels — Channel B adjustments are made on the A5 board, Channel C adjustments on A4, and Channel D adjustments on A6.

Oscillator Adjustment

1. Connect the Counter's AC Input to the Test point labelled "20 MHz". (See Figure 3-6).
2. Set a one-second GATE time FREQUENCY measurement.
3. Adjust the capacitor next to the test point for a Counter reading of 20.000000 MHz ± .000050 MHz.
4. Connect the Counter's AC Input to the Test Point labelled "8.192 MHz".
5. Adjust the capacitor next to this test point for a reading of 8.192000 MHz ±0.000020 MHz.

Figure 3-6. A19 ADC Sample Generator (05466-60006) Adjustments



SECTION 4
TROUBLESHOOTING AND PREVENTIVE MAINTENANCE

INTRODUCTION

This section provides preventive maintenance and system troubleshooting procedures for troubleshooting to the circuit card level in the 5460A Display Unit, 5466B ADC or 5475A Control Unit (see Table 4-1). This procedure determines as quickly as possible whether the trouble lies in the system hardware or the Processor. Processor malfunction isolation, including all software and peripherals, is contained in separate manuals. Refer to the System Configuration Notice for a list of equipment and manuals supplied with your Fourier Analyzer System.

Table 4-1. System Troubleshooting Procedures

TEST EQUIPMENT REQUIRED

Table 1-3 provides a list of equipment required to troubleshoot the Fourier Analyzer System.

PREVENTIVE MAINTENANCE

Usually, the most common denominator associated with poorly performing systems is the lack of a sound preventive maintenance program. The following paragraphs give guidelines to help develop a meaningful P.M. plan for the Fourier System. A P.M. program is essential in obtaining a high on-the-air yield for your complex system and should be performed on a regularly scheduled basis to keep interruptions to a minimum.

The Field Preventive Maintenance Procedure which follows indicates the intervals at which P.M. routines should be performed, the approximate amount of time that the P.M. routine will require and a brief description of what is to be performed at each interval. These descriptions are intended to tell an experienced, trained CE "what" to do as opposed to "how" to do it. If additional information is needed, reference should be made to other sections of this manual or to the maintenance manual of the equipment involved.

The proper amount of P.M. is that which accomplishes the basic purpose of minimum interruptions and does so at minimum cost. Unnecessary P.M. is not only wasteful of time but also jeopardizing to equipment reliability. Consistent with this premise, P.M. should consist of cleaning, lubricating, visual inspection, replacement of determinable worn parts (air filter, etc.), observation of equipment operation, and one short pass of the diagnostic. Only adjustments which are known to require periodic attention should be *checked*. The time intervals below reflect one work shift usage under normal operating conditions. Good judgement and a firm understanding of system usage should be used to influence the use of these figures to arrive at a sensible P.M. schedule for a particular Fourier Analyzer System.

Preventive Maintenance Time Table Work Sheet

Month / Product	1	2	3	4	5	6	7	8	9	10	11	12
Processor						1						1
Display						.5						.5
Kybd. (5475)						.5						.5
ADC (5466B)						.5						.5
Disc			*			*			*			*
Cabinet			.25			.25			.25			.25
PIMM (5440B)						.25						.25
DAC (5442ØA)						.5						.5
Filters (5444ØA)						.25						.25
Preprocessor (5447ØA)						.5						.5
Terminal						*						*
Line Printer						*						*
Plotter						*						*
Mag Tape			*			*			*			*
Sys. Control (5477)						.5						.5
Counter						*						*
Total Hours												
Scheduled Rate & Hr.												

*See individual maintenance manual for PM procedure.

Preventive Maintenance action to be taken

Processor 54451A

1. Check voltages
2. Check fans
3. Run firmware diagnostic
4. Run booster diagnostic

5460A/5466B/5475A Display/AVC/Kybd.

1. Check 5475A fan
2. Check voltages on 5475A connector J17
   +24V ± 100mV between J17(14, 32) & ground
   +12V ± 50mV between J17(16, 34) & ground
   + 5V ± 5mV between J17(18, 36) & ground
   -24V ± 100mV between J17(9, 27) & ground
   -12V ± 50mV between J17(7, 25) & ground
   - 5V ± 5mV between J17(5, 23) & ground
   Ground connections are J17(1, 2, 19, 20)
3. Check lamps on 5475A and 5460A
   Press BS64 etc. for BS lights
   Repeat & RA for busy (check pulse at 1KHz etc.)
   Single switch for ready
   BS 1 for what
   Turn scale sw. for 1, 2, 5, & X10 lamps & rect.
   F for freq.
   Polar for polar lamp
   Log. Mag. — db and log lamps
4. Press all 5475A keys (except stop, cont. & restart)
   check characters on Terminal

Plug-In Mainframe Module (PIMM) 5440B

1. Check power supply on 5440B
2. Check fan on 5440B

Cabinet

1. Clean filters
2. Check on/off lamp

All other equipment

Check proper manual

TROUBLESHOOTING ASSUMPTIONS

The troubleshooting procedures make the following assumptions:

1. That, with the exception of general malfunction indications (e.g., no CRT beam even with BEAM FIND depressed), the system test diagnostic and operational check is used as a basis for for the troubleshooting procedures. If it is obvious that the processor or a related peripheral is malfunctioning, refer to the applicable manual. The system test diagnostic is configured to allow specific subroutines to be utilized as required. Always perform at least the unit operational check after repairing any unit.

2. That all system controls have been double checked to verify that they are in the proper positions. Also, that all cabling is correctly and firmly connected and that all processor interface cards are in the assigned I/O slots. The System Configuration Notice contains a record of the I/O slots for all the processor peripherals.

3. That interconnect wiring will be checked and cabling replaced or repaired as required if the directed troubleshooting does not correct malfunction.

4. That all processor bit indicators are functioning. If any doubt exists, load the entire register to verify that indicators are functioning correctly.

5. That power is removed prior to replacing any units or circuit cards.

GENERAL MALFUNCTION INDICATIONS TROUBLESHOOTING

Table 4-2 provides troubleshooting for malfunctions that can be identified without being in the operatonal check. Where possible, the corrective action is given without going through the entire operational check. This list is not intended to cover all possible malfunctions.

POWER TURN-ON TROUBLESHOOTING

If the Fourier Analyzer System is rack-mounted, check continuity of rack wiring before the individual units.

If power cannot be applied to the oscilloscope, refer to the oscilloscope manual.

If power cannot be applied to the Control Unit, refer to Figure 2-8. If the OVERLOAD lamp on the back of the Control Unit is lit, see Table 4-2.

SYSTEM DIAGNOSTIC LOADING TROUBLESHOOTING

If the system test diagnostic will not load, check the System Test Diagnostic Loading procedure in Section 3.

CONTROL UNIT TROUBLESHOOTING

These troubleshooting procedures are to be used if the Fourier Analyzer fails a portion of the Control Unit test in the operational check or if the Control Unit has performed correctly during the operatonal check but the keys fail to give correct operation in the Fourier Analyzer mode. Refer to one of the following tables for specific troubleshooting:

1. Table 4-3. Preliminary Keyboard Test Troubleshooting

2. Table 4-4. QK Subroutine Test Troubleshooting

3. Table 4-5. SK Subroutine Test Troubleshooting

DISPLAY UNIT TROUBLESHOOTING

These troubleshooting procedures are to be used only if the Fourier Analyzer fails a portion of the Display Unit test in the Operational check. If the Display Unit has performed correctly during the operational check but the plotter does not function properly or the display is jittery, refer to the general malfunction indications troubleshooting (Table 4-2). Refer to one of the following tables for specific troubleshooting:

1. Table 4-6. SD Subroutine Test Troubleshooting

2. Table 4-7. QD Subroutine Test Troubleshooting

ADC TROUBLESHOOTING

These troubleshooting procedures are to be used only if the Fourier Analyzer fails a portion of the ADC test in the operational checks.

Refer to one of the following tables for specific troubleshooting.

1. Table 4-8. SA Subroutine Test Troubleshooting
2. Table 4-9. QA Subroutine Test Troubleshooting
3. Table 4-10. QM Subroutine Test Troubleshooting
4. Table 4-11.SM Subroutine Test Troubleshooting

POWER-ON TEST TROUBLESHOOTING

If the system fails to return to the RUN mode, troubleshoot the computer. Refer to computer manuals.

If the system doesn't run, but HALTS with MEMORY DATA of 102050, 102051, 102052, 102053, 102055, 102056, 102057 displayed, see Table 4-12, Processor Test Troubleshooting, in this manual.
manual.

Table 4-2. General Malfunction Indications Troubleshooting

Problem	Action
a. Can't get any input through the ADC.	a. 1. Check fuses on A1 (and/or A2) board(s). a) Turn off system power. b) Remove ADC from Control Unit. c) Remove ADC right-hand side cover. d) Remove A1 (and/or A2) board(s). e) Exchange "bad" fuse with spare fuse on board. 2. Check to see if proper voltages are being supplied to the ADC from the 5475A. See section 3. 3. Check ADC's front-panel controls. a) If TRIGGER MODE switch is in INT or EXT, is there actually a trigger signal? b) Are the sample rate switches on a calibrated range? c) If external samples are being generated, are they within the EXT. sample specifications? 4. Check to see that 5451C system test diagnostic is "ok". (Best method is to reload the diagnostic). 5. Replace the following 5466B boards, in the order indicated, one at a time: a) A1Ø b) A9 c) A8 d) A3 } If ADC will not input, or inputs wrong data. e) A1 and/or A2 f) A4 through A6 g) A7 } If ADC inputs wrong data.
b. When turned on, the Display Terminal does not function.	b. 1. Verify cables are properly installed (see *Figure 1-2*). 2. Replace A14.
c. No action when RESTART is pressed.	c. 1. Replace keyboard microcircuit I/O card in processor. 2. Check processor, refer to processor manuals.
d. Control Unit keyboard does not perform correctly.	d. Refer to preliminary keyboard test troubleshooting for this problem.
e. No CRT display even with BEAM FIND pressed.	e. Refer to oscilloscope manual.

Table 4-2. General Malfunction Indications Troubleshooting (continued)

Problem	Action
f. OVERLOAD light on REAR of the Control Unit lights (indicates a power supply is overloaded.	f. To locate current overload perform the following: 1. Remove Display Unit plug-in. If OVERLOAD goes out, overload is in plug-in. Isolate and repair defective circuit. 2. Remove ADC plug-in. If OVERLOAD goes out, overload is in plug-in. Isolate and repair defective circuit. 3. One at a time, remove all cables from Control Unit rear panel. If disconnecting any cables causes the OVERLOAD indicator to go out, the problem is in the circuit served by that cable. Reconnect the cable. With a voltmeter and the Control Unit power supply adjustment procedure locate the supply being overloaded. If trouble is in the Control Unit, replace regulator board. If external, isolate and repair defective circuit.
g. Jittery display.	g. Check power supply voltages and clean board and plug contacts.
h. When System is turned on, the Display Terminal prints ".WHAT" repeatedly.	h. 1. Check +5V fuse inside 5475A Control Unit. 2. Replace Keyboard Microcircuit Interface Card.

Table 4-3. Preliminary Keyboard Test Troubleshooting

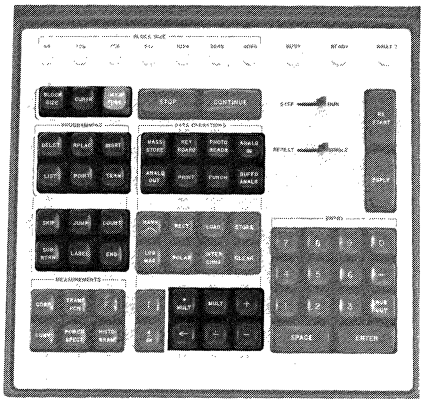
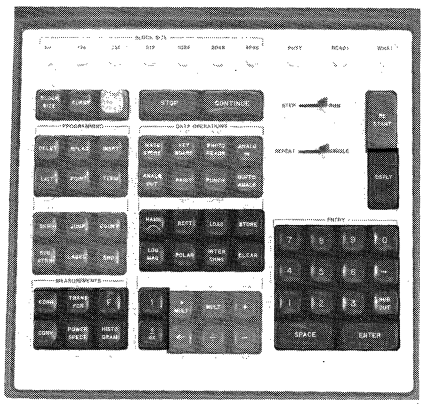
Problem	Action
a. Single Display Terminal key is intermittent or locks out all other keys.	a. 1. Check switch (adjust, if necessary). 2. Check Wiring.
	
GROUP A	**GROUP B**
b. No Display Terminal output for either GROUP A or GROUP B switches.	b. 1. Check or replace A18. 2. Replace A14. 3. Replace Terminal microcircuit I/O card in processor. 4. Check Display Terminal.
c. Wrong Display Terminal output for GROUP A and GROUP B switches.	c. 1. Adjust A14 Oscillator (see Control Unit Adjustments). 2. Replace A14.
d. Wrong or no Display Terminal output when a GROUP A switch is pressed. Display Terminal OK for GROUP B switches.	d. Replace A12.
e. Wrong or no Display Terminal output when a GROUP B switch is pressed. Display Terminal OK for GROUP A switches.	e. Replace A13.
f. Correct letters displayed when the keyboard buttons are pressed, but there is still a problem when returning to the main Fourier program (i.e., pushing a button does not perform the correct function), it is desirable to check the coding of the bits into the processor. In order to do this test, the system test diagnostic must be operating and the test subroutine entered by typing QK, RETURN, RETURN. Then press malfunctioning key. The octal code is displayed in the Display Register.	f. Observe octal code for ASCII character in Display Register (STOP, CONTINUE, & RESTART switches are uncoded and wired direct to A15).

Table 4-3. Preliminary Keyboard Test Troubleshooting (continued)

NOTE

Disregard bit 8 in binary count. That is, Block Size has a code of 102(3)23 but the computer may have 102(7)23.

Signal Name	Teleprint	ASCII Equivalent (Octal Code)
BLOCK SIZE	BS	102323
CURSR	/.	057256
USER PROG	Y	131240
DELET	/D	057304
REPLAC	/R	057322
INSRT	/I	057311
LIST	/L	057314
POINT	?	077240
TERM	/	057240
SKIP	IF	111306
JUMP	J	112240
COUNT	#	043240
SUB RTRN	<	074240
LABEL	L	114240
END	.	056240
CORR	CR	103322
TRANS FLN	CH	103310
F	F	106240
CONV	CV	103326
POWER SPECT (Note 1)	SP	123320
HISTO GRAM	RH	122310
MASS STORE	MS	115323
KEY BOARD	K	113240
PHOTO READR	R	122240
ANALOG IN	RA	122301
ANALG OUT	B	102240
PRINT	W	127240
PUNCH	P	120240
BUFFD ANALG	RB	122302
HANN Ω	HI	110261
RECT	TR	124322
LOAD	X<	130274
STORE	X>	130276
LOG MAG	TL	124314
POLAR	TP	124320
INTER CHNG	X	130240
CLEAR	CL	103314

Note 1: The next key pressed after the POWER SPECT key will require pressing 5 times to obtain the correct reading.

Table 4-3. Preliminary Keyboard Test Troubleshooting (continued)

Signal Name	Teleprint	ASCII Equivalent (Octal Code)
$\int$	$	044240
*MULT	*–	052255
MULT	–*	052240
+	A+	101253
$\frac{d}{dx}$	%	045240
←	—(Note 2)	137240
÷	:	072240
–	A–	101255
ENTER	CR LF	015212
SPACE		040000
DISPLAY	D	104240
RUBOUT	BELL	007377
1	1	061000
2	2	062000
3	3	063000
4	4	064000
5	5	065000
6	6	066000
7	7	067000
8	8	070000
9	9	071000
0	0	060000
-	-	055000

Note 2: Underscore on some terminals is ←".

g. Octal code as shown on processor register is incorrect but processor had correct printout.	g. Adjust A14 Oscillator (see Control Unit Adjustments).
h. Octal code as shown on processor register is correct.	h. Troubleshoot processor, refer to processor manuals.

Table 4-4. QK Subroutine Test Troubleshooting

Problem	Action
a. Pressing STOP does not light READY or pressing CONTINUE does not light BUSY and the corresponding bit (15 or 13) is lit in the processor register.	a. 1. Replace A17. 2. Replace ADC microcircuit I/O card in processor. 3. Check indicator continuity.
b. Pressing STOP does not light READY or pressing CONTINUE does not light BUSY and the corresponding bit (15 or 13) is not lit in the processor register.	b. 1. Replace A15. 2. Replace keyboard microcircuit I/O card in computer. 3. Check switch. 4. Check processor, refer to computer manuals.
c. STEP/RUN, REPEAT/SINGLE or any of the ADC switches called out in this test fail to light correct bits.	c. 1. Replace keyboard microcircuit I/O card in processor. 2. Check switch. 3. Check processor, refer to processor manuals.

Table 4-5. SK Subroutine Test Troubleshooting

Problem	Action
a. No action when RESTART is pressed.	a. Refer to general malfunction indication troubleshooting (*Table 4-2*).
b. A single indicator malfunctions.	b. 1. Check indicator. 2. Replace A17.
c. A group of indicators malfunction.	c. 1. Replace A17. 2. Replace ADC microcircuit I/O card in processor.

Table 4-6. SD Subroutine Test Troubleshooting

Problem	Action
1. a. Bit 15 remains on.	a. Replace A5. b. Replace display microcircuit I/O card in processor. c. Doublecheck switch settings.
2. LAMPS. Problem with one or more of the following 5460A lamps: POLAR, RECT, LOG, FREQ, 1, 2, 5, X10, dB.	
a. One or more of the lamps does not light.	a. Replace boards. 1. A8—lamps are mounted on this board. 2. A9—lamp drivers are on this board. 3. A4—T²L driver lines are on this board. 4. Display microcircuit I/O card in processor.
b. None of the lamps light.	b. 1. Replace ±24V Regulator in 5475A Control Unit. 2. Check +24V line at A8(K).
3. READ-OUT TUBES. Problem with one or more Digital Display Tubes.	
a. No Digital Display Tube is lighted and no "—" sign displayed.	a. 1. Replace A9. 2. Check +170V line from A8(J) to A9(15, S). 3. Check 130V ac at A9(6, 8).
b. All Digital Display Tubes function, but are dim.	b. Replace A9.
c. Any Digital Display Tube counts, but not in proper sequence (skips numbers or is dead for counts 0 through 9; or resets to 0 and recounts at the wrong time). Note: Normal operation includes blanking for 6 counts after "9", while the BCD counter counts back to "0".	c. Replace A8.
d. All Digital Display Tubes count, but sequence is bad.	d. 1. Replace A8. 2. Replace A4. 3. Replace display microcircuit I/O card in computer.
e. None of the tubes count.	e. 1. Replace A8. 2. Replace A4.

Table 4-6. SD Subroutine Test Troubleshooting (continued)

Problem	Action
f. "—" Indicator does not light.	f. 1. Replace A9. 2. Replace A8. 3. Replace A4.
4. CRT Display problems:	
a. No sweep, but dot appears.	a. 1. Replace A3. 2. Replace A4. 3. Replace display microcircuit I/O card in processor. 4. Reload test tape. 5. Refer to Processor Service Manual for processor checkout procedure.
b. No sweep, but dot or vertical line appears at left side of screen.	b. Verify that DISPLAY switch on scope mainframe is in INT position.
c. No CRT sweep or vertical deflection, and no spot.	c. Press Beam FIND. 1. If dot appears, and processor register bit 15 is flashing, be sure 5460A FUNCTION switch is set to DISPLAY, not to PLOT. 2. If dot appears, and processor register bit 15 is not flashing. a) Reload system test diagnostic. b) Replace display microcircuit I/O card in processor. c) Refer to processor checkout procedure computer service manual. 3. If dot does not appear. a) Replace A1. b) Check High Voltage to CRT—refer to oscilloscope manual.
d. Horizontal sweep, but VERTICAL GAIN, POSITION or CAL controls have no effect.	d. Replace A1.
e. Sweep nonlinear, either vertically or horizontally.	e. Interchange A2 and A3. 1. If problem changes. a) Replace A2 if problem is *now* Vertical nonlinearity. b) Replace A3 if problem is *now* Horizontal linearity. 2. If problem does not change. a) Replace A1 if problem is in Vertical deflection. b) Refer to oscilloscope manual if problem is in horizontal deflection.

Table 4-6. SD Subroutine Test Troubleshooting (continued)

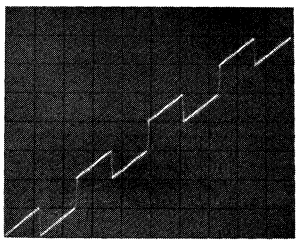
Problem	Action
f. If oscilloscope pattern resembles one shown below. **HORIZONTAL PROBLEM** 	f. Interchange A2 and A3. 1. If problem changes replace A2. 2. If problem doesn't change. a) Replace A4. b) Replace display microcircuit I/O card in processor. c) Check computer, refer to processor manuals.
g. If oscilloscope pattern resembles one shown below: **VERTICAL PROBLEM** 	g. Interchange A2 and A3. 1. If pattern changes, replace A3. 2. If pattern doesn't change. a) Replace display microcircuit I/O card in processor. b) Check processor, refer to processor manuals.
h. Sweeps, but HORIZONTAL POSITION and X5, X10, MAGNIFICATION controls have no effect.	h. Refer to oscilloscope manual.
i. Display is Vertical line.	i. 1. Replace A4. 2. Replace A5. 3. Replace A3. 4. Refer to oscilloscope manual.
j. Display is only Horizontal line.	j. 1. Replace A1. 2. Replace A4. 3. Replace A5. 4. Replace A3. 5. Refer to oscilloscope manual.
k. Sweeps OK but problem with vertical bars.	k. Interchange A2, A3. If problem is corrected, replace the board NOW in A3. If problem is not corrected, replace A5.
5. SWITCH problems:	
a. HORIZONTAL MARKER switch causes no intensification of trace in either 8PT or 32PT position.	a. 1. Replace A5. 2. Replace A4. 3. Z-axis problem in oscilloscope mainframe, refer to oscilloscope manual.

Table 4-6. SD Subroutine Test Troubleshooting (continued)

Problem	Action
b. HORIZONTAL MARKER switch causes intensification of trace only in 8 PT or 32 PT position, but not in both.	b. 1. Replace A5. 2. Check HORIZONTAL MARKER switch circuit for bad contacts or broken wires. 3. Check switch command lines A5(8) for $\overline{HM32}$ and A5(J) for HM8 signals.
c. DISPLAY TYPE "BAR" or "CONT" does not function.	c. 1. Replace A5. 2. Replace A2. 3. Check switch command lines A5A(14) for $\overline{DTLNT}$ and A5A(1Ø) for $\overline{DTPNT}$ signals.
d. HORIZONTAL SWEEP LENGTH switch does not change sweep length.	d. 1. Be sure VERTICAL MODE switch is not in COMPLEX setting. 2. Replace A3. 3. Check switch command lines 12.8 (signal $\overline{HS.8}$) to A3A(6), 1Ø (signal $\overline{HS1Ø}$) to A3A(F) and 1Ø.24 (signal $\overline{HS.24}$) to A3A(H).

Table 4-7. QD Subroutine Test Troubleshooting

Problem	Action
a. Any Display Unit switch called out in this test that fails to light correct bits.	a. 1. Check switch wiring. 2. Reload system test diagnostic. 3. Possible problems with input portion of the display or with the processor.

Table 4-8. SA Subroutine Test Troubleshooting

Problem	Action
NOTE Set ADC controls as follows: SAMPLE MODE to kHz. MULTIPLIER to 2.5/5/2ØØ. TRIGGERING to FREE RUN	
a. TRIGGERING indicator lights when bit 15 is off.	a. 1. Replace A1Ø, A9, A8. 2. Replace keyboard microcircuit I/O card in processor. 3. Check processor, refer to processor manuals.
b. TRIGGERING INDICATOR will not light in any position with bit 15 on.	b. 1. Check indicator. 2. Replace A8. 3. Replace A1Ø. 4. Replace A9. 5. Check switch. 6. Replace ADC microcircuit I/O card in processor. 7. Check processor, refer to processor manuals.
c. TRIGGERING indicator will not light, in LINE position only.	c. Replace A8. 2. Check Line plus signal from J15(43). 3. Check switch.

Table 4-8. SA Subroutine Test Troubleshooting (continued)

Problem	Action
d. TRIGGERING indicator will not light, in INTERNAL (A) position only.	d. 1. Replace A8, A9. 2. Check TRIGGER SOURCE switch.
e. TRIGGERING indicator does not work in FREE RUN.	e. 1. Replace A8. 2. Replace A10. 3. Check TRIGGER SOURCE switch.
f. TRIGGERING indicator does not work, in EXTERNAL.	f. 1. Check EXTERNAL switch. 2. Replace A8.
g. UNCAL indicator does not light, in any position.	g. 1. Check indicator. 2. Replace A7.
h. UNCAL indicator does not light, in some positions.	h. 1. Replace A7. 2. Check SAMPLE MODE switch.
i. The frequency, or group frequencies, are incorrect by a factor of 2, 10, etc.	i. 1. Check SAMPLE MODE switch codes in QK test. 2. Replace A10 Sample Generator board.

Table 4-9. QA Subroutine Test Troubleshooting

Problem	Action
a. ADC does not pass calibration check.	a. 1. Perform A1 (and/or A2) adjustments. 2. Perform A3, A5 (A4, A6) adjustments.
b. Wrong bit indications from OVERLOAD VOLTAGE attenuator switch(es).	b. 1. Check Switch(es). 2. Replace ADC microcircuit I/O card in processor. 3. Check processor, refer to processor manuals. 4. Replace A1 (A2).
c. Check pulse did not appear, for one or more of the DISPLAY (or DISPLAY/INPUT) switch positions.	c. 1. Replace A7 board. 2. Check switch. 3. Check line plus signal from J15(43).
d. OVERLOAD VOLTAGE gain codes incorrect.	d. 1. Replace A7. 2. Replace A10. 3. Disconnect Remote Programming cable. 4. Check Switch. 5. Check Remote Programming and ADC I/O microcircuit (refer to appropriate manuals).
e. Incorrect codes for OVERLOAD VOLTAGE switch settings, for one or more DISPLAY/INPUT (or DISPLAY and INPUT) switch settings.	e. 1. Replace A7 board. 2. Disconnect Remote Programming cable. 3. Replace Remote Programming I/O microcircuit card.

Table 4-9. QA Subroutine Test Troubleshooting (continued)

Problem	Action
f. ADC input gain test failed, for all input gain settings.	f. 1. Perform calibration procedure. 2. Check fuse on A1 (and/or A2) board. 3. Replace A1 (and/or A2) board. 4. Interchange A3, A5 (and/or A4, A6) Digitizer boards. If the fault is on the Digitizer, replace the Sample-and-Hold and/or Digitizer module as indicated. If the fault is on the data inverter and data buffers, plug "good" Sample-and-Hold and/or Digitizer module(s) from faulty board into replacement board.
g. Triangle wave input test failed.	g. 1. Interchange Digitizer boards (A3, A5, and/or A5, A6), as appropriate. 2. If the fault is on the Digitizer board, interchange Sample-and-Hold and/or Digitizer modules between "good" and "bad" boards. If fault indication is still present, load "good" Sample-and-Hold and/or Digitizer module(s) onto replacement board, and install board in the system.
h. ADC does not pass gain linearity part of adjustment and calibration procedure.	h. 1. Replace A1 (or A2) Input board. 2. If the fault is on the Digitizer board, interchange Sample-and-Hold and/or Digitizer modules between "good" and "bad" boards. If fault indication is still present, load "good" Sample-and-Hold and/or Digitizer module(s) onto replacement board, and install board in the system.
i. Does not pass EXTernal sample rate test.	i. 1. Check the INPUT signal for "noise" and overshoot. Be sure the levels are less than .3V and greater than 2V. 2. Replace A9 board. 3. Check Processor.

Table 4-10. QM Subroutine Test Troubleshooting

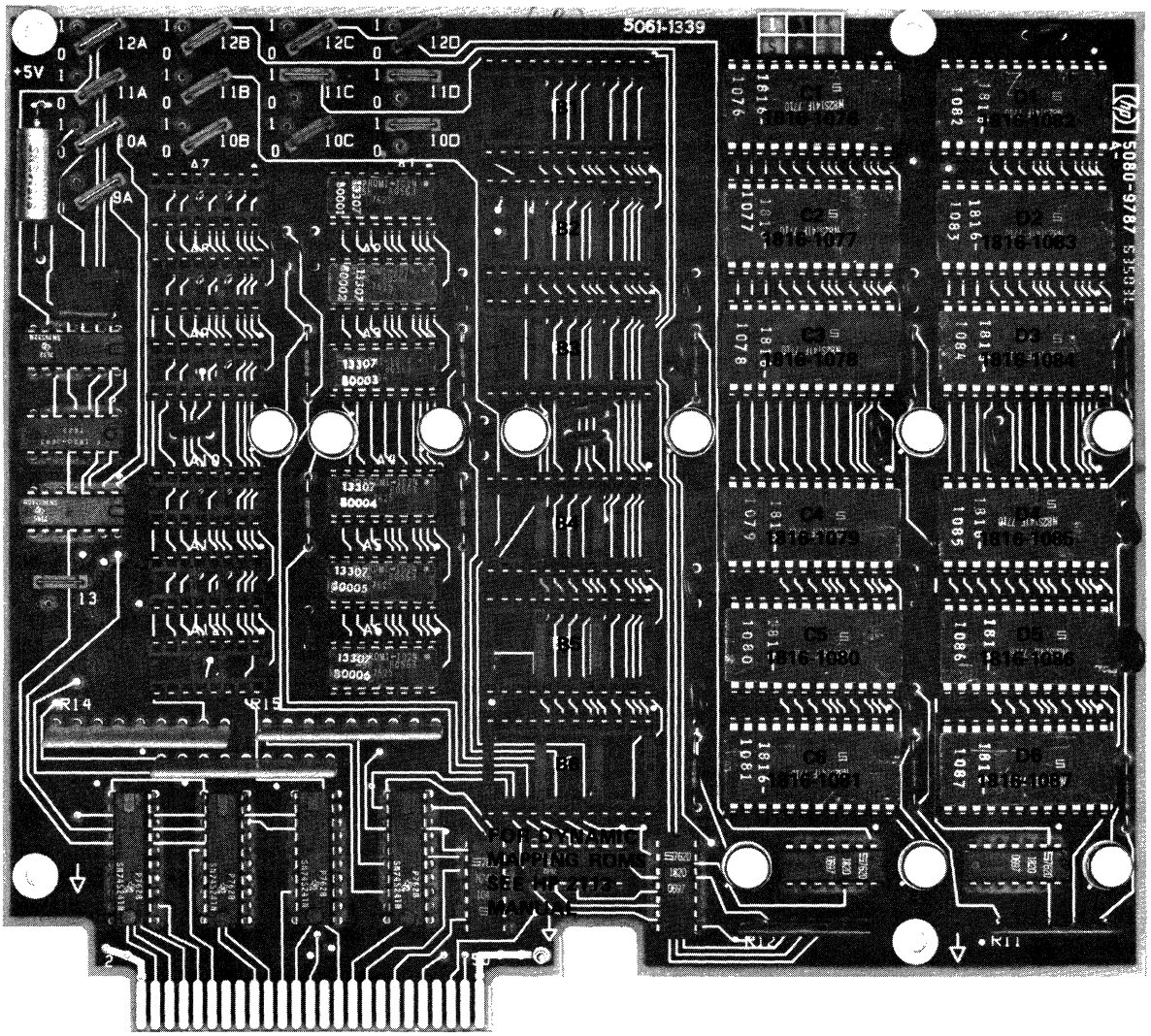
Problem	Action
Bit "2" does not light, or wrong bit pattern.	1. Confirm that proper cable is installed. (2-channel ADC uses 05451-60002; 4-channel ADC uses 05451-60004). Cable must have continuity between pin "C" and pin "3". 2. Check OVERLOAD VOLTAGE switches. 3. Replace ADC microcircuit I/O card in processor. 4. Check processor. Refer to processor manuals.

Table 4-11. SM Subroutine Test Troubleshooting

Problem	Action
Computer HALTS during SM test.	1. Press the Processor's "S" button to see "SM" bit error. If bit "15" = "Ø", then bits "11" through "Ø" will indicate signals which were in error. If bit "15" = "1", then bits "5" through "Ø" indicate signals associated with four-channel operation which were in error. Pressing RUN re-runs the program. Additional details are given below. 2. Confirm that proper cable is installed (2-channel ADC uses Ø5451-6ØØØ5; 4-channel ADC uses Ø5451-6ØØØ6). 3. Check OVERLOAD VOLTAGE switches. 4. Replace ADC microcircuit I/O card in processor. 5. Check processor. Refer to processor manuals.
"SM" ERROR (BIT "15" "OFF") 15 14 13 12 11 1Ø 9 8 7 6 5 4 3 2 1 Ø Ø B1 B2 B3 A1 A2 A3 EO DF X5 X2 S2 S1 Not Used Sample Rate Parameters Channel A INPUT Range Channel B INPUT Range	1. Check to be sure SAMPLE MODE switch is in its "REMOTE" position. 2. Check to see that all input range (OVERLOAD VOLTAGE) switches are in their "8" positions. 3. Replace Channel A and/or Channel B remote programming microcircuit interface card in processor. 4. Check wiring.
"SM" ERROR (BIT "15" "ON") 15 14 13 12 11 1Ø 9 8 7 6 5 4 3 2 1 Ø 1 D1 D2 D3 C1 C2 C3 Not Used Channel C INPUT Range Channel D INPUT Range	1. Check to make sure SAMPLE MODE switch is in its "REMOTE" position. 2. Check to see that all input range (OVERLOAD VOLTAGE switches are in their "8" positions. 3. Be sure 5466B four-channel capability exists, and is being used.

Table 4-12. HP54451A Processor Test Troubleshooting

Problem	Action
1. Error occured in LOAD WCS, BASIC I/O TEST, or DMA TEST.	1. Suppress these tests with appropriate switch register bits. These tests require special fixture and should not be run in the field.
2. Booster error occurs.	2. a. Run ROM test. b. Change booster board. c. Check cable to booster board. d. Run Diagnostic Configurator and all CPU diagnostics.



3. ROM test errors occur.	3. a. Change set of 3 ROMS as indicated on terminal until bad ROM(s) are found. b. Change connector cable. c. Run Diagnostic Configurator and all CPU diagnostics.

APPENDIX A
DIAGNOSTIC LOADING

This appendix contains information to load diagnostics for the following:

HP 54451A Processor
HP 5451C System Test (ADC, Display and Keyboard)
HP 54420A Digital-to-Analog Converter
HP 54470A Preprocessor
HP 7210A Digital Plotter
HP 5477 System Control
HP 12604B Data Source Interface

For the processor and other peripherals, see Diagnostic Configurator Reference manual (Diagnostic Reference Table) for further reference to applicable documentation.

LOADING PROCEDURES

1. On HP 7900A Disc Drive Unit, set LOAD-UNLOAD switch to UNLOAD and wait for DOOR UNLOCKED indicator to light. On 7906A Disc Drive Unit, set RUN/STOP switch to STOP and wait for the DOOR UNLOCK indicator to light.
2. Open door on Disc Drive Unit and insert system disc pack. For standard systems use disc pack HP 54451-10001 (7900A) or 54451-10101 (7906A); for standard systems with Magnetic Tape Units, use disc pack HP 54451-10002 or 54451-10102.
3. On 7900A, set LOAD-UNLOAD switch to LOAD and wait for DRIVE READY indicator to light. On 7906A, set RUN/STOP switch to RUN and wait for the DOOR UNLOCK indicator to light.
4. On HP 54451A, load disc basic binary loader (NIBBL) as follows:

   a. Press <Register Select> switch until S register is selected. Enter 101701_8 (7900A) or 111700_8 (7906A) in Display Register, then press STORE switch. Bits 6 through 11 are select code for disc (standard is 17).

   b. Press PRESET, IBL, RUN.

   c. Processor should halt at 102076_8.

5. To load diagnostics, proceed as follows:

   a. Select S register, CLEAR DISPLAY, STORE.

   b. Set the A and B registers for the desired diagostics as follows:

DIAGNOSTIC	A REGISTER (Sector Number)	B REGISTER (Cylinder Number)
HP 54451A Processor	000000_8	000031_8
HP 5451C System Test	000001_8	000041_8
HP 54420A DAC	000001_8	000042_8
HP 54470A Preprocessor	000000_8	000037_8
HP 5477A System Control	000001_8	000043_8
HP 7210A Digital Plotter	000001_8	000044_8
HP 12604B Data Source Interface	000001_8	000045_8
	Reserved For Future Diagnostics. Do Not Use.	000046_8 000047_8 000050_8 000051_8 000052_8

c. Press STORE, PRESET, RUN.

d. Processor should halt at 102011_8 (halt 102077 for Processor diagnostic)

4. See applicable operating and service manual for diagnostic procedure. For the 5451C system test, see Section III.

If the diagnostics do not load correctly there may be an error in NIBBL or the standard disc loader ROM (IBL initial binary loader).

To verify NIBBL or IBL instructions in memory, proceed as follows:

1. Press <Register Select> to M.

2. Enter 077600 in the Display Register for checking NIBBL or 077700 for standard disc loader.

3. Press STORE.

4. Press <Register Select> to T.

5. If necessary, change the register number displayed to agree with the corresponding number in Table A-1 (NIBBL) or A-2 (IBL).

6. Press STORE if changing contents in step 5.

7. Press INC (increments) M. This displays the contents of the next consecutive memory location.

8. Repeat steps 5 through 7 until satisfied that the program is correct.

NOTE

The <Register Select> may be set to M at any time to display the number of the current address. The DEC M switch can be used to reverse the NIBBL display.

Table A-1. Instructions for NIBBL

Address	0	1	2	3	4	5	6	7
077600	073700	002400	073676	063671	106717	017660	060001	001265
077610	017660	063700	102717	017660	063675	102606	063676	106702
077620	006321	001225	102602	001265	043677	073676	043701	003025
077630	002500	043677	003004	102702	102602	103706	063672	006020
077640	063673	106717	017660	102106	063674	106717	017660	102517
077650	073667	013670	002002	027665	006045	027603	067702	024001
077660	000000	103617	102317	027662	127660	063667	102011	000000
077670	017400	001000	002400	004000	001400	000017	000000	014000
077700	000000	100200	102077					

Table A-2. Instructions for Standard Binary Loader (IBL)

Address	0	1	2	3	4	5	6	7
077700	102501	106501	013764	005750	027740	1026CC	1037CC	1023DD
077710	027707	002004	053764	002001	027705	067776	047765	077776
077720	067760	1066DD	1037DD	1066CC	1037CC	1023DD	027725	006400
077730	102501	002311	047770	1066DD	1037DD	1023CC	027735	063704
077740	067776	106606	067761	077740	106602	102702	067763	106602
077750	002041	027766	1026CC	1037DD	103706	1037CC	037773	027773
077760	030000	102011	102055	164000	000007	120000	1067DD	001720
077770	001000	1036DD	103706	1023DD	027773	117762	000017	100100

DD = Disc Data Channel (standard is 17)
CC = D1 + 1 (standard is 20)

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