CodeTAP®-XA Emulator

For Motorola 68331 and 68332 Microcontrollers

Highlights

- Real-time in-circuit emulation permits non-intrusive debugging
  - Uses no target memory space
  - Provides Read/Write access to all registers and memory
  - Allows reliable single-stepping, even with interrupts enabled
- Intelligent dynamic trace disassembly captures information on-the-fly and shows register content changes along with trace display
- Powerful source-level debugger supports C and C++
- Sequential event system makes trapping complex bugs easy
- 256K or 1 MB overlay memory greatly facilitates debugging of PROM-based systems and makes it easier to debug RAM-based systems
- Ethernet communications for Sun and serial communications for PC make downloading fast and efficient
- Powered either from your target or a separate, isolated supply for convenience and safety
- Performance analysis tracks where the program spends its time
- External breakpoint outputs permit CodeTAPs to work together with logic analyzers, oscilloscopes and other CodeTAPs in multiprocessor targets
- Timesaving "Explode" command decodes register contents, eliminating the need to constantly refer to data books

Put the compact, feature-rich CodeTAP-XA in your tool kit.

CodeTAP-XA: Price and Performance

The new CodeTAP-XA (extended architecture) in-circuit embedded development tool introduces an unprecedented feature-set in its price class. CodeTAP-XA gives software engineers all the debugging functions they use most, such as software and hardware breakpoints and modification of memory and processor registers, in a low-cost, small-footprint device.

CodeTAP-XA also incorporates high-performance features such as trace disassembly including register contents, Ethernet communications, sequential Event System, and performance analysis. CodeTAP-XA's combination of low-cost and performance lets you equip every engineer, boost productivity, and reduce time to market.

Patented Emulation Technology

CodeTAP-XA uses a custom ASIC with advanced emulation technology to provide visibility and control for executing and debugging code. Because CodeTAP-XA doesn't require code modifications, target memory, interrupt vectors, or target I/O locations, you get a transparent, real-time view of your target.

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We also offer tools to support these Motorola products: 68000, 68020, 68030, 68040/040V, 68060/EC060/LC060, ColdFire MCF5102, 68302, 68330/340, 68360/EN/MH, CPU32

High-Level Debugger and Language Tools

Specifically engineered for CodeTAP-XA, Applied's MWX-ICE C/C++ source and assembly-level debugger gives you easy access to all hardware features. From the windowed interface you have access to high-level data structures and dynamic variables. You can selectively start and stop execution, display and modify CPU registers and memory, and construct powerful macros using a C-like command language.

With convenient, quickly installed interfaces to popular hosts and compilers, CodeTAP-XA fits easily into your environment. Supported software tools include a C/C++ cross-compiler, cross-assembler, disassembler, embedded linker, and object librarian.

Trace History and Display

A 4K deep trace buffer captures address, data, and status information on each clock cycle. Trace information can be captured and viewed without stopping the target processor (Non-Stop Emulation™) or trace can be qualified by turning it off *n* cycles after an event qualification signal. The trace display shows full source-level, assembly-level, or mixed source-and assembly instructions, along with timestamp information. A trace buffer search capability allows searching for frames containing any combination of address, data, and status information.

Overlay Memory

Mappable RAM overlay memory enables convenient debugging of target PROM and RAM-based target systems. Up to 1 MB of zero wait-state overlay memory is available. It can be segmented into 8 separate blocks, each mapped anywhere in memory on 16K or 64K byte boundaries. Your code is protected while running because writes are not allowed to overlay memory declared as ROM.

Breakpoints and Sequential Event System

CodeTAP-XA supports four hardware breakpoints. Each can be used to invoke either an execution, access, or data value breakpoint. Used together, they form a powerful, four-level sequential event system capable of generating breakpoints that quickly and efficiently pinpoint even tricky, intermittent problems. 64 software execution breakpoints can each be set to a specific address. Asynchronous breakpoints are controlled by the host debugger. External input and output breakpoints allow other devices to notify CodeTAP-XA to break execution or allow it to tell other devices it has stopped. The event system can be used to turn off trace *n* cycles after event qualification.

Trace Disassembly

Applied's Intelligent Trace Disassembler—an industry first—dramatically increases productivity by displaying instructions correlated with register values and bus cycles. CodeTAP-XA lets you easily isolate events that produce unexpected register values, without time-consuming single-stepping, manual calculations, or tedious references to data books. Detailed timing data for each instruction is also useful for analyzing code performance. For the most often-used registers, the convenient "Explode" command graphically displays the register, identifies each bit, and provides definitions.

CodeTAP-XA for Motorola 68331 and 68332 Microcontrollers

Microprocessor Support
Motorola MC68331 at up to 16.78 MHz
Motorola MC68332 at up to 16.78 MHz

Host Requirements
PC environment:
- Compatible with IBM PC-386 or later, MS-DOS or PC-DOS 5.0 or higher, 4MB RAM minimum, RS-232 serial port, VGA display

Sun environment:
- Sun 4, SPARCstation, 8MB RAM minimum, Sun OS 4.1.1 or higher, Ethernet port

Communications
PC environment:
- RS-232C serial interface, to 115.2K baud. Effective download speed to: 250K bytes per min.

Sun Environment:
- IEEE 802.3 10base2 and 10base5 (Ethernet Thin wire and Thick wire). Effective download speed to: 500 Kbytes /min

Power Requirements
2A at 5V maximum; 1.3A at 5V typical
Powered from target or external supply, jumper selectable

Physical Specifications
Dimensions (LHW): 5.6 x 1.0 x 3.0" (14.22 x 2.54 x 7.62cm)
Weight: 5 oz.
Ambient humidity: 0-90% non condensing
Operating temperature: 32-104° F (0 to 40° C)

Optional Software Development Tools
ANSI C/C++ Cross-Compiler
Cross-Assembler
Embedded Linking Loader
Object Module Librarian

High Level Debugger
Efficient source-level debug
Window-oriented interface (X-Window support on SUN SPARCstation)
Support for C/C++
Access to source code variables
Disassembled source view for machine-level debug and patch
Access to all global, local, stack-based and register-based symbols
Full C-typing features
Execution control and full access to all CodeTAP-XA hardware features
Execution breakpoints can be set on line numbers, C statements, program labels and memory addresses
Display trace in raw, disassembled, and high-level format
Monitor real and simulated I/O
High-level control of event system set-up and operation
In-line assembler/memory operations
Assemble code in target memory using Motorola mnemonics
Display and modify memory
Advanced testing and set up capabilities
Construct complex macros containing C-like statements and debugger commands
Record and play back debugging sessions
Explode command to display register contents with explanations
Performance Analysis
Statistical representation of relative time spent in functions
File format compatibility:
MRI tool chain

Overlay Memory
256K or 1 MB
16 MHz operation with zero wait states
Mapping based on Addresses or Chip Selects
Mappable on 16K byte boundaries (256K version) or 64K byte boundaries (1 MB version)
Mappable as Read/Write or Read Only

Trace
Depth: 4K clock cycles x 68 bits wide (address, data, and status signals)
Collected on clock cycles (typically 4 clocks per bus cycle)
Dynamic trace: trace can be read without stopping target processor
Qualified by turning trace off based on event system
IPIPE and IFETCH captured for accurate disassembly
Search trace for frames containing specific address, data, and status
Display address, data, status, and time stamp information with symbols

Intelligent Trace Disassembler
Infers and displays register contents correlated with instructions
Allows display of mixed source-level trace and assembler trace
Allows display of assembly instructions along with bus cycle and timing information

Breakpoint and Event System
4-stage sequential event system
4 hardware breakpoints
64 software execution breakpoints
Asynchronous breaking allowed under control of host debugger
External breakpoint trigger in and out
4 comparators used to trigger:
- Hardware execution breaks after instruction
- Hardware access breaks after bus cycle
- Trace system to stop tracing

Comparator inputs include:
- Address
- Data
- Chip select & CS Boot
- Function Code
- Data Strobe Acknowledge
- Read/Write
- Autovector
- Read-Modify-Write Cycle
- Size
- Interrupt Request
- External event input (LSA bit)

Stand-Alone Mode
When invoked, CodeTAP-XA behaves just as a bare processor without emulation capabilities

Target Hardware Adapters
Clip-on adapter, fits over 132-pin PQFP package in target
Ironwood two piece adapter; LCC bottom soldered to target
AMP adapter fits over AMP PQFP socket (P/N 821949-5) soldered to target

For more information, call 1-800-426-3925, e-mail info@amc.com, or browse http://www.amc.com

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