CodeICE Emulator

for Intel i960® H-Series Processors

Highlights

- Full-scale development system supports all HA, clock-doubled HD and clock-tripled HT processors with a single probe tip and user interface at full-rated processor speed
- Powerful multi-windowed MWX-ICE C/C++ debugger interface runs on Sun4, HP 9000/700, and PC hosts
- Debugger operates stand-alone or in the MRI MasterWorks™ environment
- RTOS-Link™ integrated interactive kernel support option
- Intuitive CPU Browser™ interface to fully configure, visualize, and change internal 960 Hx register states (DLMCON, PMCONs, ICON, MPARs, etc.)
- Performance Plus tools provide:
  - Convenient profiling and code coverage support for Intel's optimizing compilers
  - Integrated performance analysis for profiling real-time execution of unlimited system functions
- Unique Source-Level Trace capability automatically correlates execution history with source code
- High speed overlay memory options from 1–8 MB
- Seamless networking support for workstations and PCs
- Real-time trace with timestamp captures 128 bits x 32K frames of information at full speed with cache enabled
- Versatile run-control services target interrupts while the emulator is paused, allows user interaction with emulation functions without stopping execution, and runs isolated from the target system at full-speed
- 30 hardware access, 22 hardware execution break-points and virtually unlimited software breakpoints
- Flexible, powerful event system is easily configured to detect even the most exotic real-time system events
- Fully isolated probe tip, diagnostic functions, and scope loops help verify hardware design and diagnose problems

Companion Products

- CodeTEST™ embedded software verification tools for the 960 Hx offer developers and testers comprehensive software performance analysis, code coverage analysis, memory allocation analysis and software trace

Applied Microsystems Corporation

CodeICE for 80960 Hx—Serious speed puts the fun back in embedded development.

Built for Speed

"Speed . . . provides the one genuinely modern pleasure."[1] Speed *is* nice. In fact, it's essential for embedded development tools: fast enough to match the speed of your latest processor; fast enough to deliver massive code downloads; and fast enough so you can get your product done before the competition grabs the market.

CodeICE™ emulators are built for speed. And that doesn't just mean fast performance specs. We also designed in powerful ease-of-use features that help you work more easily, so you get more done in less time. CodeICE emulators also keep the cost of speeding down, too, using the latest in innovative emulation technology to provide a rich feature set at minimum expense.

Unique "Full-Power" Emulation Features

Features of the CodeICE emulator that speed development include the new, graphical CPU Browser™ register configuration interface, a self-configuring performance optimization tool set, Applied's unique source-level trace capability, flexible run-control, and optional integrated RTOS support.

The intuitive MWX-ICE debugger interface makes it easy to organize your environment for the way you work. The graphical debugger offers point-and-click access to the most powerful emulator features, and seamless integration with a graphical source explorer, editors, language tools and configuration management tools.

We also offer tools to support these Intel products: 80960 CA/CF/Jx; 80C186/188 XL, EA, EB, EC; 80L186/188 XL, EA, EB, EC; 80286; 80386 SX/DX; 386EX

[1] Aldous Huxley, "Wanted, a New Pleasure," in *Music at Night and Other Essays* (1949).

A Winning Combination

Meeting today's aggressive schedules and budgets takes cost-effective tools that offer both robust power and ease of use. CodeICE emulators represent a new approach to emulator technology that meets each of these requirements.

Just for Hx

Each CodeICE emulator is engineered for a single processor architecture. This processor-specific design makes it possible to reduce the number of components needed to build an emulator, yet significantly increase feature breadth and depth and achieve unmatched precision.

As a result, the CodeICE emulator for 960 Hx delivers affordable no-compromise performance—such as 75 MHz internal and 40 MHz external bus speeds and a rich feature set that supports the entire H-series with a single probe tip and debugger.

Power You Can Use

CodeICE features are designed to help you work more quickly and easily. Debugging embedded designs can actually be fun with tools like the CPU Browser graphical register configuration interface and RTOS-Link interactive kernel support. And with the intuitive MWX-ICE debugger interface you may even be home in time for dinner.

What's more, as the chart below shows, you can use the power of the emulator over the entire development cycle, which makes CodeICE an even better investment. Each team member, from software and hardware engineers to manufacturing and support technicians, can get information about your product they can't get as easily—or at all—with any other tool. And because each CodeICE can be installed on your workstation or PC network as its own node, everyone can have seamless access to the emulator.

Graphical Debugging Speeds Development

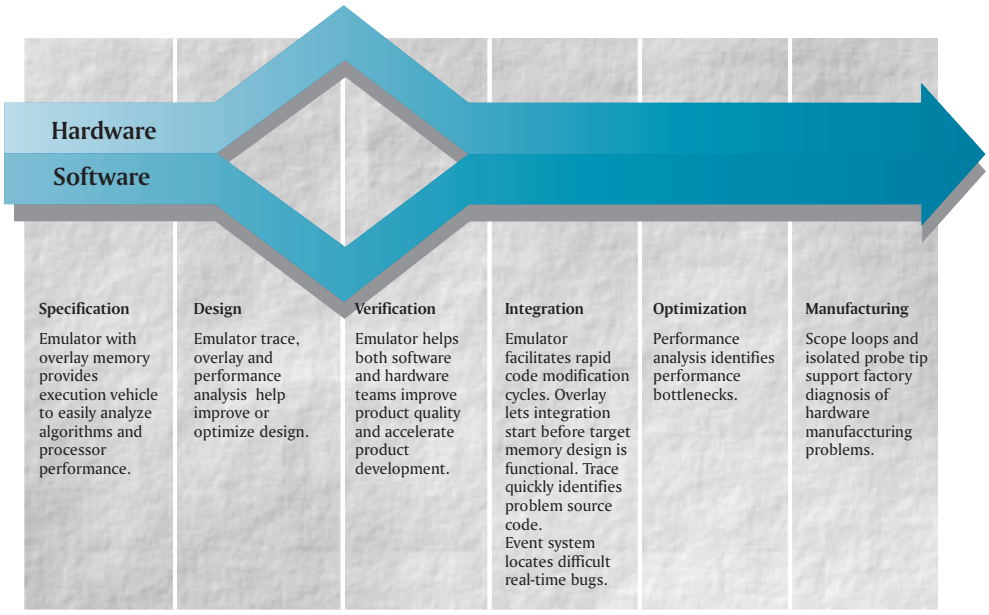
MWX-ICE is a function-rich C/C++, source- and assembly-level debugger. Available for PC , Sun4, or HP hosts, MWX-ICE gives you quick and easy visibility and control of code execution in your target.

This intuitive debugger combines a point-and-click windowed interface, extensive macro capabilities, and a comprehensive hypertext on-line help system with Applied's specially engineered support for all the features of the CodeICE emulator for 960 Hx. It gives you simple, straightforward control of your target and the emulator, whether you prefer to work with a mouse or from the command line.

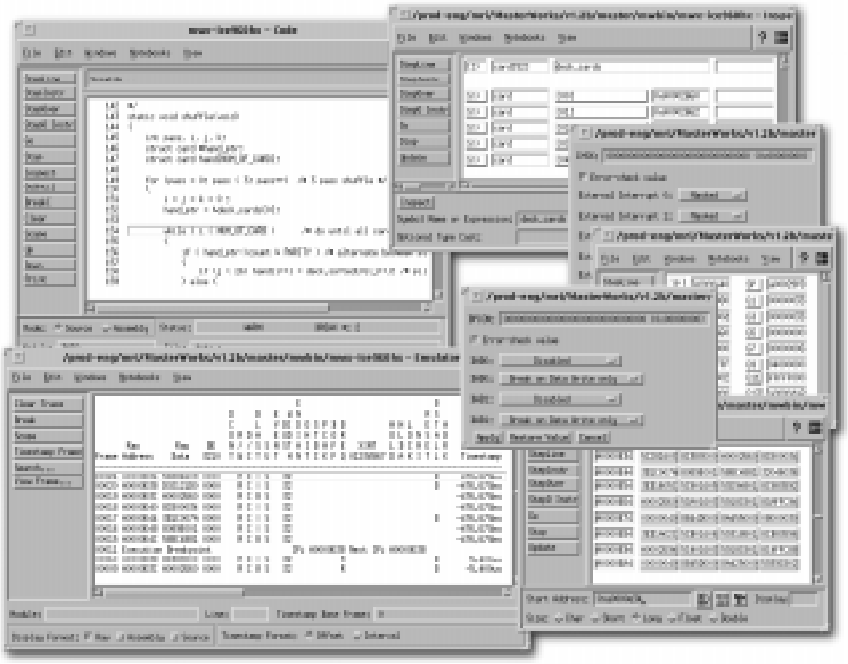
With the notebook feature, you don't have to remember debugger command language. Instead, you can build even complex command sequences just by pointing and clicking. And the context-sensitive hypertext help system means you don't waste time hunting through manuals.

The multi-windowed graphical interface lets you visually organize your debug environment for a more natural approach to debugging. For example, you can display source code together with the corresponding assembly language in separate windows to clarify the relationship between them and verify compiler performance.

MWX-ICE accepts executables from the popular tool chains, such as Intel's i960, GCC960 and MRI's C/C++ compilers.



The Utility of the CodeICE emulator spans the entire development cycle.



The multi-windowed debugger speeds development with simultaneous display including (clockwise from upper left): source code, symbolic representation of structure elements, register values, stack values, call tracing, CPU Browser register-configuration utility, memory, and interleaved trace.

Source-Level Trace Simplifies Debugging

To see what's really going on in your target, you need to see the relationship between source code and the processor instructions that execute in the target. With Applied's unique source-level trace capability, correlating execution history to source code has never been easier.

When viewing trace at source-level, you can also display the associated source modules and line numbers for quick and easy reference. For complete capture of execution history, the Trace system provides 128 bits of information about each cycle to a depth of 32K frames. With the optional Logic State Analysis Probe, you can trace an additional 16 external signals from your target concurrently with processor bus-level trace. This allows you to correlate the status and timing of external target events with processor bus and signal trace.

And when you need to locate a particular text string in the trace buffer, a menu-driven search capability finds any text, whether it's data, an address, or even a function name.

Register tracking, a pioneering technology in CodeICE emulators, records the state of processor registers during execution and aligns data movement to executed instructions. This unique capability helps boost productivity by providing accurate information about internal processor operations.

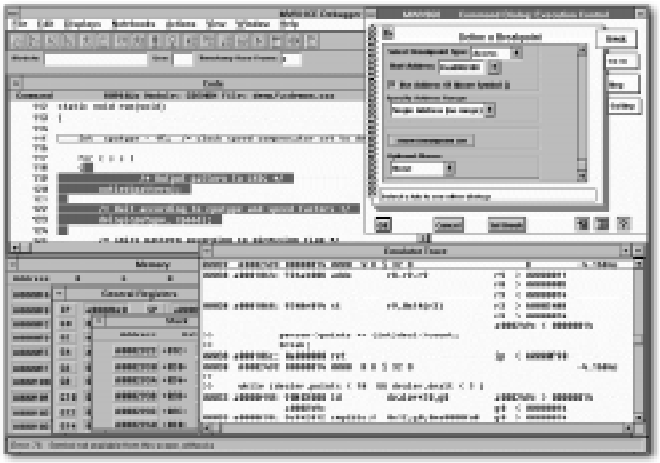
Trace With Cache Enabled

To debug code that makes the most of heavily cached processors, such as the Hx family, you need a means of seeing the instructions that were executed out of cache. Applied's trace system not only does that, but also disassembles cached instructions. You can then display information at source level, assembly level, bus/clock cycle level, or in mixed levels.

Event System Pinpoints Problems

The CodeICE Event System lets you readily determine the execution trail of code without having to modify your code with printf statements or semaphores. The system can be used to qualify trace so you can capture the specific context of a problem, not just the effect. And you can quickly and transparently place breakpoints anywhere, even for functions executed out of cache.

It's easy to configure the Event System using familiar names and symbolic references. The system supports a variety of qualifications in any combination. The When Event / Then Action statement format is both simple to understand and powerful. The full complement of event system actions furnishes a complete tool kit for isolating problems. Available actions include stop emulation,



The same array of MWX-ICE features is also available in a native Windows® debugger.

turn-on trace, turn-off trace, change state or group, increment counters, and generate an external trigger for operations such as synching an oscilloscope. The Logic State Analysis Probe option allows you to bring an additional 16 external signals in from your target to further qualify events.

In most targets, when you're using breakpoints to help pin down a problem you can't always afford to stop your application's whole world when you hit a breakpoint. The target still needs to service interrupts driven from other tasks while you determine where to set your next breakpoint. That's why the CodeICE emulator provides a capability called Interrupts During Pause (IDP). When this feature is enabled, the emulator services interrupts even when you have suspended emulation.

Overlay Memory Saves Time

High-speed overlay memory helps maximize your investment by extending the utility of the CodeICE emulator to the very early stages of development. Before your target hardware is ready, the emulator, probe tip, and overlay memory provide an execution vehicle so you can get going early.

Mapping overlay as target memory also eliminates time spent burning ROMs to verify a code fix. Overlay also simplifies and accelerates hardware-software integration by letting you gradually implement target memory. Simply use overlay until the target hardware is debugged. You can program segments of overlay memory with 64K granularity to mimic your target system read-only or read-write memory. Overlay capacities of up to 8 MB are available.

Performance Plus Tools Go Beyond Analysis

It takes more than just analysis to optimize performance. That's why the CodeICE system for 960 Hx includes a suite of tools to help you streamline your embedded design.

Applied teamed with Intel to offer convenient profiling and code coverage support for Intel's optimizing compilers. The result is a set of seamless, easy-to-use commands that automate the process of locating, extracting, formatting and uploading real-time profile data from memory back to your file system in a ready-to-go image.

Automated performance improvement may be all you need in many situations. But for critical applications you can make additional system performance measurements with an easy-to-use Performance Analysis tool. Because it places no demands on target operation or resources, the tool delivers an accurate view of where your code spends its time. It monitors an unlimited number of modules, gathering data to describe execution activity, code timing, interrupt timing and fault detection. Data is presented in easily understood histogram and statistical formats, and the tool generates reports to help document software and product performance.

Product validation is also an important component of every product life cycle. The CodeICE system includes an extensive macro language that lets you build automated test suites using emulator commands.

Once you've fine-tuned target performance and built up an arsenal of comprehensive test cases, you can use CodeICE profile support commands to gather test coverage information. Used together with Intel's coverage analyzer, CodeICE performance tools tailor the output of the code coverage report to your requirements, such as call graph listings, combinations of program-, module-, function-, and source-level coverage reports, hit or miss source line execution, and two-profile comparisons.

CPU Browser lets you keep the data books on the shelf.

CPU Browser Speeds Register Configuration

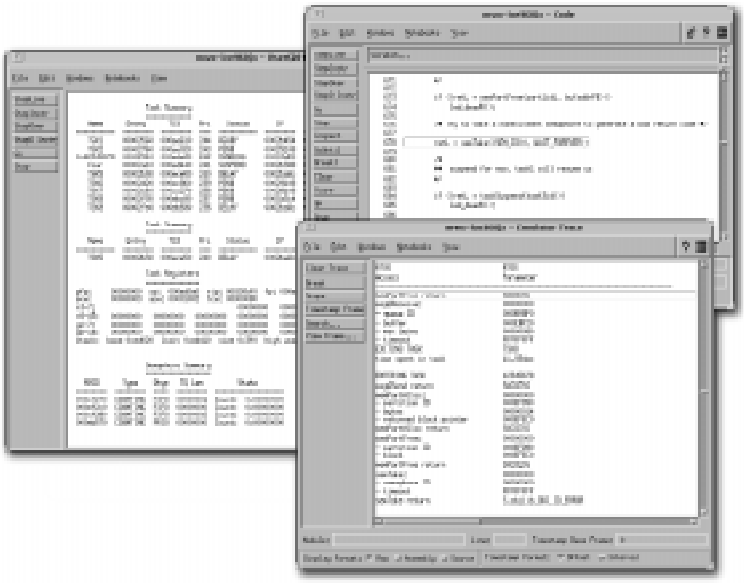
Nobody enjoys poring through data books full of register bit settings. The CPU Browser™ register configuration utility makes your life easier with an error-proof means to configure and visualize the states and meanings of internal 960 Hx registers, such as the DLMCON, PMCONs, ICON, and MPAR registers. Its graphical display shows current or proposed register configuration information, with point-and-click access to all configurable bit fields.

Preset hex and binary values for bit configuration prevent mis-keying, and error checking is performed on all changes before they are applied. The CPU Browser window includes clear descriptions of individual bit fields, and the register bit configuration display immediately previews the effects of enabling and disabling each bit state.

RTOS-Link Support Offers System-Level Visualization

CodeICE engineers work closely with industry-leading commercial kernel developers to provide comprehensive support packages for Real-Time Operating Systems (RTOS). RTOS visibility at the CodeICE level shows how the target, application, and RTOS interact with one another during execution in a thoroughly integrated, real-time environment.

Several broad categories of support are provided through RTOS-Link, including: real-time trace of RTOS activity, display of individual task context and other system structures, task-qualified breakpoints, task stack overflow detection, and task profiling support. The benefit of integrated RTOS support is a substantial reduction in the time required to debug and optimize your application as it runs in your target.



RTOS-Link provides visibility of configuration and activities in kernel-based systems. Views such as task execution trace, task profiling, and configuration detail help you quickly isolate even subtle system problems.

Helping You Succeed

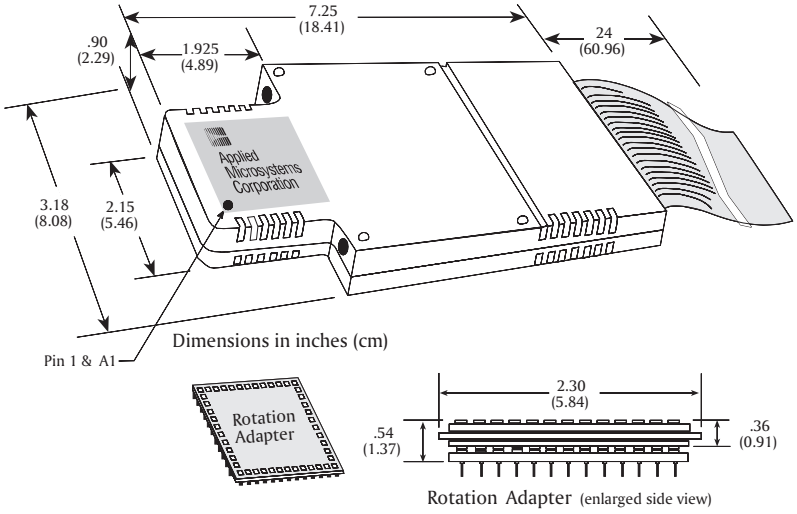
Because our success depends on your success, we take product support very seriously. In fact, at Applied Microsystems we call our program Customer Satisfaction.

Keeping you satisfied means more than just answering your questions. The leader in embedded development tools and the most experienced 960 market driver, Applied has the qualified and committed people it takes to provide thorough on-site training and superior engineering assistance, technical guidance on emulation issues, and expedited product service.

Our Applications Engineering Group is backed by a network of experienced Field Application Engineers, our own design teams,
and the commitment of the entire company. And with over 10,000 installed solutions and more than seventeen years of leadership in embedded hardware and software development tools, our team is an important asset to have on your team.

To see how the CodeICE emulator can accelerate your 960 Hx project, call 1–800–426–3925 for information or a demonstration. And put some genuine pleasure in your embedded development project.

Take the Time to Call Now



Dimensions of the CodeICE 960 Hx emulator probe tip.

CodeICE Emulator for Intel i960® H-Series Processors

Microprocessors Supported
Intel 80960HA, 80960HD, 80960HT; at 75 MHz

Packages Supported
PGA direct; PQFP with optional adapter

Minimum Host Requirements
PC 386 or better
Microsoft Windows 3.1 or higher, 12 MB RAM minimum, 16 MB recommended (1 vacant ISA or EISA slot for High-Speed Parallel)
Sun SPARC
16 MB RAM minimum, 20 MB swap, Sun OS 4.1.x, Solaris 2.2/2.3, Ethernet port
HP 9000/700
16 MB RAM minimum, 20 MB Swap, HP/UX 9.0 or later, Ethernet port

Communications
PC Environment:
Ethernet (Winsock 1.1, TCP/IP (incl. Novell)), IEEE 802.3 10base2, 10base5, 10baseT
High-Speed Parallel
Sun / HP Environment:
IEEE 802.3 10base2, 10base5, 10baseT

User Interface
Integrated Source Level Debugger
Multi-windowed interface (X-windows/ Motif/Open Windows on workstations, Windows on PC)
Support for Intel, GNU, and MRI C / C++ and assembly language
Access to all global, local, stack-based and register-based symbols with full data typing features
Flexible run-control: continue to service system interrupts while execution is paused; debug code without stopping the target system with Dynamic Run, Stop, and Update
Execution breakpoints can be set on line numbers, source statements, program labels and memory addresses
Performance Optimizing Tools
Profile support for Intel's optimizing C compilers and code coverage utilities
Integrated Performance Analysis
View statistics based upon the number of occurrences of functions and/or actual time spent in functions in convenient histogram and statistical formats
Real-Time Operating System Support Option
Integrated support for leading RTOS kernels
Display status of RTOS structures, profile tasks in real-time, trace the flow of RTOS activity, isolate defects based on RTOS activity, and more
CPU Browser
Graphical interface allows display and modification of internal memory, breakpoint, interrupt controller and timer unit register values

Trace System
Hardware
Trace depth 32K x 128 bits wide with programmable timestamp
Intelligent Trace Disassembler
Display instructions and register contents correlated with data
Trace Windows
Choose between bus cycle, assembly, and source trace display, on-the-fly, in any combination
Scrollable forward and backwards
Search trace for specified patterns
Connected to the event system to allow qualified tracing
Source-Level Trace
Unique capability displays which source lines were executed and correlated values while executing out of cache

Event System
Define external signals from your target to qualify events
4 independent groups and 4 independent, configurable states
2 32-bit counters
2 BNC Connectors: one trigger out, one trigger in
Supports qualification of event by value of variable, LSA input, address, instruction execution, data, CPU signal status, trigger in, trace full or counter
Event Actions:
Break — Trace on/off/one
Change group — Trigger out
Activate state/group
Increment/toggle/reset counter

Breakpoint System
Up to 30 hardware access breakpoints and an additional 22 hardware execution breakpoints for ROM or RAM (including access to on-chip breakpoints)
Virtually unlimited software execution breakpoints for code located in RAM
1 asynchronous breakpoint from keyboard

Overlay Memory
1 to 8 MB available
No overlay wait states to 20 MHz (one wait state at 20 MHz and above)
Map anywhere in 64K segments
Configurable as read-only and read-write to simulate ROM and RAM in the system

Target Hardware Debug Support
Fully buffered probe tip allows debug of dysfunctional target hardware
Predefined diagnostic routines and scope loops offer a suite of tools to quickly isolate defective hardware
Integrate up to 16 external signal lines from your target hardware into the CodeICE break, event and trace systems with optional Logic State Analysis Probe

Advanced Testing and Validation
C-like macro extension language allows you to construct and save target regression tests
Record and playback debugging sessions

Physical Specifications
Chassis: 16" X 13" X 5" (40.6 cm X 33 cm X 12.7 cm) [L x W x H]
Chassis weight: 14 lbs. (6.35 kg)
Probe Tip: 7.25" X 3.18" x 0.90" (18.41 cm X 8.07 cm X 2.29 cm) [L x W x H]
Probe Tip cable length: 24" (60.96 cm)

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