Latch functions.

37200A LATCH FUNCTIONS

REV H, 4/14/2004 LM3765G Latch Table.xls

128 64 32 16 8 4 2 1

No.	Latch Function	Old/ New	R/W	Load	Freq Table	Also Used On	Data D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	B5	B4	B3	B2	B1	GPIB Mnemonic	Notes
1	LO1 READ	OLD	R	NO	NO	A1	X	X	LOOP BACK	X	X	X	LOCK	X	0	1	0	1	1	1	1	1	1	O	DRL1 XX1	DRL=Read from latch # DWL= Write to latch # (byte xx1)
2	M1 (2O MODULUS)	OLD	W	YES	YES	A1	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	1	0	0	1	1	1	1	1	O	DWL 2 XX1 (byte XX1)	M20, LINE 970 OF FREQ PLAN ALGOR
3	M2 (21 MODULUS)	OLD	W	YES	YES	A1	D7 MSB	D6	D5 LOOP BACK	D4	D3	D2	D1	D0 LSB	0	1	0	0	0	1	1	1	1	O	DWL 3 XX1 (byte XX1)	M21 LINE 980 OF FREQ PLAN ALGOR
4	M3 (FRAC %M)/LBEN.	OLD/ NEW	W	YES	YES	A1	X	X	X	LBEN 1=LO, 0=NOR	D3 MSB	D2	D1	D0 LSB	0	1	0	1	0	1	1	1	1	O	DWL 4 XX1 (byte XX1)	MF LINE 990 OF FREQ PLAN ALGOR
4	M3 (FRAC %M)/LBEN.	OLD/ NEW	W	YES	YES	A2	X	X	X	LBEN 1=LO, 0=NOR	D3 MSB	D2	D1	D0 LSB	0	1	0	1	0	1	1	1	1	O	DWL 4 XX1 (byte XX1)	MF LINE 990 OF FREQ PLAN ALGOR
4	M3 (FRAC %M)/LBEN.	OLD/ NEW	W	YES	YES	A3	X	X	X	LBEN 1=LO, 0=NOR	D3 MSB	D2	D1	D0 LSB	0	1	0	1	0	1	1	1	1	O	DWL 4 XX1 (byte XX1)	MF LINE 990 OF FREQ PLAN ALGOR
4	M3 (FRAC %M)/LBEN.	OLD/ NEW	W	YES	YES	A4	X	X	X	LBEN 1=LO, 0=NOR	D3 MSB	D2	D1	D0 LSB	0	1	0	1	0	1	1	1	1	O	DWL 4 XX1 (byte XX1)	MF LINE 990 OF FREQ PLAN ALGOR
4	M3 (FRAC %M)/LBEN.	OLD/ NEW	W	YES	YES	A6	X	X	X	LBEN 1=LO, 0=NOR	D3 MSB	D2	D1	D0 LSB	0	1	0	1	0	1	1	1	1	O	DWL 4 XX1 (byte XX1)	MF LINE 990 OF FREQ PLAN ALGOR
4	M3 (FRAC %M)/LBEN.	OLD/ NEW	W	YES	YES	A7	X	X	X	LBEN 1=LO, 0=NOR	D3 MSB	D2	D1	D0 LSB	0	1	0	1	0	1	1	1	1	O	DWL 4 XX1 (byte XX1)	MF LINE 990 OF FREQ PLAN ALGOR
5	LO1 DAC PRESTEER	OLD	W	YES	YES	A1	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	1	0	0	0	1	0	1	1	1	DWL 5 XX1 (byte XX1)	MDAC LINE 1000 OF FREQ PLAN ALGOR
6	% L CONTROL/ HH/DIR	OLD	W	YES	YES	A1	X	X	SLCK/ STRCK*	HH / DIR*	X	X	MSB %L	LSB %L	0	1	0	1	0	1	0	1	1	1	DWL 6 XX1 (byte XX1)	L#, LINE 780 OF FREQ PLAN ALGOR
6	% L CONTROL/H H/DIR	OLD	W	YES	YES	A2	X	X	SLCK/ STRCK*	HH / DIR*	X	DITHER CNTRL	MSB %L	LSB %L	0	1	0	1	0	1	0	1	1	1	DWL 6 XX1 (byte XX1)	L#, LINE 780 OF FREQ PLAN ALGOR
6	% L CONTROL/H H/DIR	OLD	W	YES	YES	A8	X	X	SLCK/ STRCK*	HH / DIR*	X	X	MSB %L	LSB %L	0	1	0	1	0	1	0	1	1	1	DWL 6 XX1 (byte XX1)	L#, LINE 780 OF FREQ PLAN ALGOR
7	LO 2 READ	Old/N ew	R	No	NO	A2	X	X	LOOP BACK	DDS LOCK	MAIN LOCK	X	OFST LOCK	A2 ID	1	0	0	1	1	1	1	1	1	0	DRL 7 XX1	
8	K1 (M COUNTER)	NEW	W	YES	YES	A2	0	MSB D6	D5	D4	D3	D2	D1	LSB D0	1	0	0	0	1	1	1	1	1	0	DWL 8 XX1 (byte XX1)	KM, LINE 830 OF FREQ PLAN ALGOR
9	K2 (A&R COUNTERS)	NEW	W	YES	YES	A2	D7 MSB (R) 1	D6 (R) 0	D5 (R) 0	D4 LSB (R) 1	D3 MSB (A)	D2 (A)	D1 (A)	D0 LSB (A)	1	0	0	0	0	1	1	1	1	0	DWL 9 XX1 (byte XX1)	KA, LINE 840 OF FREQ PLAN ALGOR KR=9
10	CAL/TEST* READBACK/ SRC LCK LVL OK	OLD	R	NO	NO	A4	N/A	N/A	N/A	N/A	0	0	CAL/TST * READBA CK	SRC LOCK LVL OK	0	0	1	0	1	1	0	1	1	1	DRL 10 XX1	
11	LO2 MAIN DAC PRESTEER	OLD	W	YES	YES	A2	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	1	0	0	1	1	0	1	1	1	DWL 11 XX1 (byte XX1)	KDAC, LINE 900 OF FREQ PLAN ALGOR
12	TA PHASE BYTE	OLD	W	NO	NO	A3	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	0	0	0	1	1	1	1	0	1	DWL 12 XX1 (byte XX1)	TEST A/B IF/S.D. MOD SPEC.
13	CAL/TEST*/X FER SW CNTL	OLD/ NEW	W	NO	NO	A3	LOW BAND ENABLE	L TEST A*	LREF B*	CAL/TE ST*	REV LED	FWD LED	XFER SW REV	XFER SW FWD	1	0	0	1	1	1	0	1	1	1	DWL 13 XX1 (byte XX1)	
13	CAL/TEST*/X FER SW CNTL	OLD/ NEW	W	NO	NO	A4	LOW BAND ENABLE	L TEST A*	LREF B*	CAL/TE ST*	REV LED	FWD LED	XFER SW REV	XFER SW FWD	1	0	0	1	1	1	0	1	1	1	DWL 13 XX1 (byte XX1)	
13	CAL/TEST*/X FER SW CNTL	OLD/ NEW	W	NO	NO	A6	LOW BAND ENABLE	L TEST A*	LREF B*	CAL/TE ST*	REV LED	FWD LED	XFER SW REV	XFER SW FWD	1	0	0	1	1	1	0	1	1	1	DWL 13 XX1 (byte XX1)	
13	CAL/TEST*/X FER SW CNTL	OLD/ NEW	W	NO	NO	A8	LOW BAND ENABLE	L TEST A*	LREF B*	CAL/TE ST*	REV LED	FWD LED	XFER SW REV	XFER SW FWD	1	0	0	1	1	1	0	1	1	1	DWL 13 XX1 (byte XX1)	

14	TA AMP GAIN RANGE	OLD	W	NO	NO	A3	N/A	N/A	GAIN CHANGE	G5	G4	G3	G2	G1	0	1	0	1	1	1	0	1	1	1	DWL 14 XX1 (byte XX1)	
14	TA AMP GAIN RANGE	OLD	W	NO	NO	A8	N/A	N/A	GAIN CHANGE	G5	G4	G3	G2	G1	0	1	0	1	1	1	0	1	1	1	DWL 14 XX1 (byte XX1)	
15	TA IF LVL STATUS	OLD	R	NO	NO	A3	A3 LOOPBACK READ	0	0	0	0	L >= -24*	L >= -12*	L >= 0*	0	0	0	0	1	1	0	1	1	1	DRL 15 XX1	
16	TB PHASE BYTE	OLD	W	NO	NO	A6	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	1	0	0	1	1	1	1	0	1	DWL 16 XX1 (byte XX1)	
17	TB AMP GAIN RANGE	OLD	W	NO	NO	A6	N/A	N/A	GAIN CHANGE	G5	G4	G3	G2	G1	0	1	1	0	0	1	0	1	1	1	DWL 17 XX1 (byte XX1)	
17	TB AMP GAIN RANGE	OLD	W	NO	NO	A8	N/A	N/A	GAIN CHANGE	G5	G4	G3	G2	G1	0	1	1	0	0	1	0	1	1	1	DWL 17 XX1 (byte XX1)	
18	TB IF LVL STATUS	OLD	R	NO	NO	A6	A6 LOOPBACK READ	X	X	X	X	L >= -24*	L >= -12*	L >= 0*	0	0	0	1	0	1	0	1	1	1	DRL 18 XX1	
19	REF PHASE BYTE	OLD	W	NO	NO	A4	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	0	0	0	1	1	1	1	0	1	DWL 19 XX1 (byte XX1)	
20	PORT 1 SOURCE STEP ATTN	OLD	W	NO	NO	A8	NOT TESTA ENABL	NOT TESTB ENABL	X	X	D3 40 dB	D2 40 dB	D1 20 dB	D0 10 dB	1	0	0	1	0	1	0	1	1	1	DWL 20 XX1 (byte XX1)	
21	PORT 2 TEST STEP ATTN (OPT)	OLD	W	NO	NO	A8	X	X	X	X	BIAS TEE ENAB	D2 40 dB	D1 20 dB	D0 10 dB	1	0	0	0	0	1	0	1	1	1	DWL 21 XX1 (byte XX1)	
22	A/D STATUS PORT (12 BIT CONV COMPLETE)	OLD	R	NO	NO	A5	N/A	NA/	N/A	N/A	0	IF SYNC OK	PS SYNC OK	12 BIT CC	1	1	0	0	0	1	1	0	1	1	DRL 22 XX1	A/.D COM MOD. SPEC.
23	12 BIT A/D READ (LSD)	OLD	R	NO	NO	A5	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	1	0	0	1	1	1	0	1	1	DRL 23 XX1	A/.D COM MOD. SPEC.
24	12 BIT A/D READ (MSD)	OLD	R	NO	NO	A5	X	X	X	X	D11 MSB	D10	D9	D8	1	1	0	1	0	1	1	0	1	1	DRL 24 XX1	A/.D COM MOD. SPEC.
25	SAR OUTPUT (8 BIT A/D RESULT)	OLD	R	NO	NO	A5	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	1	0	1	1	1	1	0	1	1	DRL 25 XX1	A/.D COM MOD. SPEC.
26	STEERING DAC (MS OF 12 BITS)	OLD	W	NO	NO	A5	X	X	X	X	D11 MSB	D10	D9	D8	1	1	1	0	1	1	1	0	1	1	DWL 26 XX1 (byte XX1)	A/.D COM MOD. SPEC. ADDRESSES 26,27 REVERSED
27	STEERING DAC (LS OF 12 BITS)	OLD	W	NO	NO	A5	D7	D6	D5	D4	D3	D2	D1	D0 LSB	1	1	1	0	0	1	1	0	1	1	DWL 27 XX1 (byte XX1)	A/.D COM MOD. SPEC. ADDRESSES 26,27 REVERSED
28	8 BIT JAM	OLD	W		NO	A5	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	1	1	1	0	1	1	0	1	1	DWL 28 XX1 (byte XX1)	A/.D COM MOD. SPEC.
29	A/D MODE (8 BIT/20 BIT)	OLD	W	NO	NO	A5	X	X	X	X	2803 EN*	JAM EN	M2	M1	1	1	1	1	1	1	1	0	1	1	DWL 29 XX1 (byte XX1)	A/.D COM MOD. SPEC.
30	EXT ANAL OUTPUT 12-BIT D/A (MSD)	OLD	W	NO	NO	A5	X	X	X	X	D11 MSB	D10	D9	D8	1	0	0	0	1	1	1	0	1	1	DWL 30 XX1 (byte XX1)	A/.D COM MOD. SPEC.
31	EXT ANAL OUTPUT 12-BIT D/A (LSD)	OLD	W	NO	NO	A5	D7	D6	D5	D4	D3	D2	D1	D0 LSB	1	0	0	1	1	1	1	0	1	1	DWL 31 XX1 (byte XX1)	A/.D COM MOD. SPEC.
32	READ SERIAL NO ID (ON OLD A10)	OLD	R	NO	NO	A5	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	0	1	0	0	1	1	0	1	1	DRL 32 XX1	A/.D COM MOD. SPEC.
33	READ MODEL TYPE (ON OLD A6T)	OLD	R	NO	NO	A5	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	0	0	0	0	1	1	1	0	1	DRL 33 XX1	USED TO BE *BS4
34	A5 ANALOG MONITOR	NEW	W	NO	NO	A5	X	X	X	X	MON ENB	MON A2	MON A1	MON A0	1	0	0	0	0	1	1	0	1	1	DWL 34 XX1 (byte XX1)	USED TO BE ADDRESS 05H (00101)
35	VIDEO BW/MUX CTRL	OLD	W	NO	NO	A5	LOOP BACK WRITE	BW4 40 kHz	BW3 10 Hz	BW2 100 Hz	BW1 1K Hz	MPX A ENAB	MPX B ENAB	FET GATE ENAB	1	0	0	0	0	1	1	1	0	1	DWL 35 XX1 (byte XX1)	
36	PULSE CATCH	OLD	R	NO	NO	A5	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	1	0	1	1	0	1	1	DRL 36 XX1	
37	REF AMP GAIN RANGE	OLD	W	NO	NO	A4	X	X	GAIN CHNG	G5	G4	G3	G2	G1	0	1	1	0	1	1	0	1	1	1	DWL 37 XX1 (byte XX1)	REF IF MOD SPEC

39	REF IF LEVEL STATUS	OLD	R	NO	NO	A4	A4 LOOP BACK	N/A	N/A	N/A	N/A	L >= -24*	L >= -12*	L >= 0*	0	0	0	1	1	1	0	1	1	1	DRL 39 XX1
40	SOURCE LOCK THRESHOLD DAC	NEW	W	YES	YES	A4	D7 MSB	D6	D5	DE4	D3	D2	D1	D0	0	1	1	1	1	1	0	1	1	1	DWL 40 XX1 (byte XX1)
41	"SOURCE MODULE" READ	NEW	R	NO		A21	X	X	X	X	X	X	LVL STATUS	LOOP BACK BIT	0	1	1	0	0	1	1	1	1	O	DWL 41 XX1 (byte XX1)
43	A7 STATUS READ (ENABLE)	OLD/ NEW	R	NO	NO	A7	X	X	X	LOW BAND PHASE LOCK	LO3 PHASE LOCK	LOOP BACK	EXT REF	REF OK	0	0	0	0	0	1	1	0	1	1	DRL 43 XX1
44	CAL REFERENCE PHASE CONTROL	NEW	W	NO	NO	A7	D7 MSB	D6 LOOP BACK	D5	D4	D3	D2	D1	D0 LSB	0	0	0	1	0	1	1	0	1	1	DWL 44 XX1 (byte XX1)
45	CAL/LO3 SELECT	OLD	W	NO	YES	A7	X	X	X	X	X	X	CAL ENB	CAL/LO3 SEL	0	0	0	1	1	1	1	0	1	1	DWL 45 XX1 (byte XX1)
48	TUNING DAC (MSB)	NEW	W	YES	YES	A21	D15 MSB	D14	D13	D12	D11	D10	D9	D8 LSB	1	1	0	0	0	1	1	1	1	O	DWL 48 XX1 (byte XX1)
49	TUNING DAC (LSB)	NEW	W	YES	YES	A21	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	1	0	0	1	1	1	1	1	O	DWL 49 XX1 (byte XX1)
50	FM DAC/SRCE LOOP	OLD	W	NO	YES	A8	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	0	1	0	1	1	1	0	1	1	DWL 50 XX1 (byte XX1)
51	LOOP BACK/STATUS	OLD/ NEW	R	NO	NO	A8	X	X	X	X	X	LOOP BACK	ENHAN FILTER MEAS. IDENT.	SOURCE LOCK	1	0	1	1	0	1	1	0	1	1	DRL 51 XX1
52	SOURCE LOCK CONTROL	OLD	W	NO	YES	A8	SQM BAND	50GHz Sampler Bias		MULT/DIV. SEL	SRC LOOP GAIN/ FM PHASE DAC	SWP/ SYNTH*	S.L. POLARITY	LOOP BACK	1	0	1	1	1	1	1	0	1	1	DWL 52 XX1 (byte XX1)
53	STATE MACHINE TUNE DAC	NEW	W	NO	NO	A21	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	1	0	1	0	1	1	1	1	O	DWL 53 XX1 (byte XX1)
54	FM SENSITIVITY CAL DAC	NEW	W	YES	YES	A21	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	1	1	0	1	1	1	1	1	1	O	DWL 54 XX1 (byte XX1)
55	PIN CONTROL	NEW	W	YES	YES	A21	YIG NOTCH FILTER	SDM Y1	SDM Y0	SF Y4	SF Y3	SF Y2	SF Y1	SF Y0	1	1	1	0	0	1	1	1	1	0	DWL 55 XX1 (byte XX1)
57	BAND CONTROL, 8,20,40 GHz	NEW	W	YES	YES	A21	FM LOCK /2	FM LOCK /4	BAND 2	OSC & SF AMP	BAND 12	BAND 11	BAND 0	BAND L	1	1	1	1	0	1	1	1	1	O	DWL 57 XX1 (byte XX1)
57	BAND CONTROL, 3 GHz	NEW	W	YES	YES	A21	X	X	X	X	X	X	X	BAND L	1	1	1	1	0	1	1	1	1	O	DWL 57 XX1 (byte XX1)
58	POWER LEVEL DAC (MSB)	NEW	W	YES	YES	A21	D11 MSB	D10	D9	D8	D7	D6	D5	D4 LSB	0	0	0	0	0	1	1	1	1	0	DWL 58 XX1 (byte XX1)
59	POWER LEVEL DAC (LSB)	NEW	W	YES	YES	A21	X	X	X	X	D3 MSB	D2	D1	D0 LSB	0	0	0	0	1	1	1	1	1	0	DWL 59 XX1 (byte XX1)
60	SWITCHED FILTER SHAPER DAC	NEW	W	YES	YES	A21	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	0	0	1	0	1	1	1	1	0	DWL 60 XX1 (byte XX1)
61	ALC & FM CONTROL 8,20,40 GHz	NEW	W	NO	NO	A21	X	LEVEL STATUS ENA	L FM CAL BIT	L_FM ENA	X	L LVL ENABLE	L FXD GAIN	L RO	0	0	0	1	1	1	1	1	1	0	DRL 61 XX1
61	ALC & FM CONTROL 3 GHz	NEW	W	NO	NO	A21	L_RF OFF	LEVEL STATUS ENA	L FM CAL BIT	L_FM ENA	X	L LVL ENABLE	L FXD GAIN	L RO	0	0	0	1	1	1	1	1	1	0	DRL 61 XX1
62	DDS1 PHASE INC A (PIRA) BITS 0-7	NEW	W	YES	YES	A2	0.8 D7	0.4 D6	0.2 D5	0.1 D4	0.05 D3	0.025 D2	0.0125 D1	.00625 LSB D0	0	0	0	0	0	0	1	1	1	1	DWL 62 XX1 (byte XX1)
63	DDS1 PHASE INC A (PIRA) BITS 8-15	NEW	W	YES	YES	A2	204.8 D15	102.4 D14	51.2 D13	25.6 D12	12.8 D11	6.4 D10	3.2 D9	1.6 D8	0	0	0	0	1	0	1	1	1	1	DWL 63 XX1 (byte XX1)
64	DDS1 PHASE INC A (PIRA) BITS 16-23	NEW	W	YES	YES	A2	52428.8 D23	26214.4 D22	13107.2 D21	6553.6 D20	3276.8 D19	1638.4 D18	819.2 D17	409.6 D16	0	0	0	1	0	0	1	1	1	1	DWL 64 XX1 (byte XX1)

65	DDS1 PHASE INC A (PIRA) BITS 24-31	NEW	W	YES	NO	A2	13421 772.8 MSB D31	6710 886.4 D30	3355 443.2 D29	16777 21.6 D28	8388 60.8 D27	4194 30.4 D26	2097 15.2 D25	1048 57.6 D24	0	0	0	1	1	0	1	1	1	1	DWL 65 XX1 (byte XX1)	
66	DDS1 PHASE INC B (PIRB) BITS 0-7	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	0	0	1	0	0	0	1	1	1	1	DWL 66 XX1 (byte XX1)	* NOT USED
67	DDS1 PHASE INC B (PIRB) BITS 8-15	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	0	0	1	0	1	0	1	1	1	1	DWL 67 XX1 (byte XX1)	* NOT USED
68	DDS1 PHASE INC B (PIRB) BITS 16-23	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	0	0	1	1	0	0	1	1	1	1	DWL 68 XX1 (byte XX1)	* NOT USED
69	DDS1 PHASE INC B (PIRB) BITS 24-31	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	0	0	1	1	1	0	1	1	1	1	DWL 69 XX1 (byte XX1)	* NOT USED
70	DDS1 SYNCHRONOUS MODE CONTROL (SMC)	NEW	W	YES	NO	A2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	DWL 70 XX1 (byte XX1)	INITIALIZATION
71	DDS1 RESERVED	NEW			NO	A2									0	1	0	0	1	0	1	1	1	1		NOT USED
72	DDS1 ASYNCHRONOUS MODE CONTROL (AMC)	NEW	W	YES	NO	A2	0	0	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1	1	DWL 72 XX1 (byte XX1)	INITIALIZATION
73	DDS1 RESERVED	NEW			NO	A2									0	1	0	1	1	0	1	1	1	1		NOT USED
74	DDS1 ACCUMULATOR RESET REGISTER (ARR)	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	0	1	1	0	0	0	1	1	1	1	DWL 74 XX1 (byte XX1)	* NOT USED
75	DDS1 RESERVED	NEW			NO	A2									0	1	1	0	1	0	1	1	1	1		* NOT USED
76	DDS1 ASYNCHRONOUS HOP CLOCK	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	0	1	1	1	0	0	1	1	1	1	DWL 76 XX1 (byte XX1)	ALTERNATE TO LOAD PULSE FOR DDSI
77	DDS1 RESERVED	NEW			NO	A2									0	1	1	1	1	0	1	1	1	1		NOT USED
78	DDS2 PHASE INC A (PIRA) BITS 0-7	NEW	W	YES	NO	A2	0	0	0	0	0	0	0	0 LSB	1	0	0	0	0	0	1	1	1	1	DWL 78 XX1 (byte XX1)	INITIALIZATION
79	DDS2 PHASE INC A (PIRA) BITS 8-15	NEW	W	YES	NO	A2	0	0	1 51.2	0	0	1 6.4	0	0	1	0	0	0	1	0	1	1	1	1	DWL 79 XX1 (byte XX1)	INITIALIZATION
80	DDS2 PHASE INC A (PIRA) BITS 16-23	NEW	W	YES	NO	A2	1 52428.8	1 26214.4	1 13107.2	1 6553.6	0	1 1638.4	0	0	1	0	0	1	0	0	1	1	1	1	DWL 80 XX1 (byte XX1)	INITIALIZATION
81	DDS2 PHASE INC A (PIRA) BITS 24-31	NEW	W	YES	NO	A2	0 MSB	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	1	1	DWL 81 XX1 (byte XX1)	INITIALIZATION
82	DDS2 PHASE INC B (PIRB) BITS 0-7	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	1	0	1	0	0	0	1	1	1	1	DWL 82 XX1 (byte XX1)	* NOT USED
83	DDS2 PHASE INC B (PIRB) BITS 8-15	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	1	0	1	0	1	0	1	1	1	1	DWL 83 XX1 (byte XX1)	* NOT USED
84	SSD2 PHASE INC B (PIRB) BITS 16-23	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	1	0	1	1	0	0	1	1	1	1	DWL 84 XX1 (byte XX1)	* NOT USED
85	DDS2 PHASE INC B (PIRB) BITS 24-31	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	1	0	1	1	1	0	1	1	1	1	DWL 85 XX1 (byte XX1)	* NOT USED
86	DDS2 SYNCHRONOUS MODE CONTROL (SMC)	NEW	W	YES	NO	A2	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	DWL 86 XX1 (byte XX1)	INITIALIZATION
87	DDS2 RESERVED	NEW		YES	NO	A2									1	1	0	0	1	0	1	1	1	1		NOT USED
88	DDS2 ASYNCHRONOUS MODE CONTROL (AMC)	NEW	W	YES	NO	A2	0	0	0	0	1	1	1	0	1	1	0	1	0	0	1	1	1	1	DWL 88 XX1 (byte XX1)	INITIALIZATION

89	DDS2 RESERVED	NEW		YES	NO	A2									1	1	0	1	1	0	1	1	1	1		NOT USED
90	DDS2 ACCUMULATOR RESET REGISTER (ARR)	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	1	1	1	0	0	0	1	1	1	1	DWL 90 XX1 (byte XX1)	* NOT USED
91	DDS2 RESERVED	NEW		YES	NO	A2									1	1	1	0	1	0	1	1	1	1		NOT USED
92	DDS2 ASYNCHRONOUS HOP CLOCK	NEW	W	YES	NO	A2	X	X	X	X	X	X	X	X	1	1	1	1	0	0	1	1	1	1	DWL 92 XX1 (byte XX1)	ALTERNATE TO LOAD PULSE FOR DDS2
93	DDS2 RESERVED	NEW			NO	A2									1	1	1	1	1	0	1	1	1	1		NOT USED
94	ANALOG MONITOR & LOOP BACK	NEW	W	NO	NO	A21			LOOP BACK WRITE	X	MON ENA	MON A2	MON A1	MON A0	0	0	1	0	0	1	1	1	1	0	DWL 94 XX1 (byte XX1)	
95	ALC GAIN (CAL DAC)	NEW	W	YES	YES	A21	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	0	1	0	1	1	1	1	1	0	DWL 95 XX1 (byte XX1)	
96	A1 ANALOG MONITOR	NEW	W	NO	NO	A1	X	X	X	X	MON ENB	MON A2	MON A1	MON A0	1	1	1	1	1	1	1	1	1	0	DWL 96 XX1 (byte xx1)	
97	A2 ANALOG MONITOR	NEW	W	NO	NO	A2	X	X	X	X	MON ENB	MON A2	MON A1	MON A0	1	0	0	1	0	1	1	1	1	0	DWL 97 XX1 (byte xx1)	
98	A3 ANALOG MONITOR	NEW	W	NO	NO	A3	A3 LOOPBACK WRITE	X	X	X	MON ENB	MON A2	MON A1	MON A0	0	1	1	1	0	1	0	1	1	1	DWL 98 XX1 (byte xx1)	
99	A6 ANALOG MONITOR	NEW	W	NO	NO	A6	A6 LOOPBACK WRITE	X	X	X	MON ENB	MON A2	MON A1	MON A0	1	1	1	1	0	1	0	1	1	1	DWL 99 XX1 (byte xx1)	USED TO BE ADDRESS 11H (10001)
100	A4 ANALOG MONITOR	NEW	W	NO	NO	A4	A4 LOOPBACK WRITE	R-SET ON*	X	X	MON ENB	MON A2	MON A1	MON A0	0	0	1	0	0	1	0	1	1	1	DWL 100 XX1 (byte xx1)	
101	A8 ANALOG MONITOR	NEW	W	NO	NO	A8	SAMP BIAS A1	SAMP BIAS A0	X	W BAND	MON ENB	MON A2	MON A1	MON A0	1	0	1	0	0	1	0	1	1	1	DWL 101 XX1 (byte xx1)	USED TO BE ADDRESS 06H (00110)
104	A9 ANALOG MONITOR	NEW	W	NO	NO	A9			T	B	D															
105	A10 ANALOG	NEW	W	NO	NO	A10			T	B	D															
106	A7 ANALOG MONITOR	NEW	W	NO	NO	A7	X	X	X	X	MON ENB	MON A2	MON A1	MON A0	0	0	1	0	0	1	1	0	1	1	DWL 106 XX1 (byte xx1)	
107	SF SHAPER-LIMITER CAL DAC	NEW	W	YES	YES	A21	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	1	1	0	1	1	1	1	1	0	DWL 107 XX1 (byte XX1)	
108	LOG AMP ZERO CAL DAC	NEW	W	YES	NO	A21	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	0	1	1	1	0	1	1	1	1	0	DWL 108 XX1 (byte XX1)	
110	SQM SHAPER DAC	NEW	W	YES	YES	A21	D7	D6	D5	D4	D3	D2	D1	D0	1	0	1	0	0	1	1	1	1	O		
111	65 GHz ALC	NEW	W	YES	YES	A21	X	X	X	X	X	SF FIXED OUT	SQM BAND	FWD/ REV	1	0	1	0	1	1	1	1	1	0		
112	VIDEO BW/MUX CTRL RD	OLD	R	NO	NO	A5	A5 LOOP BACK READ	0	0	0	N/A	N/A	N/A	N/A	1	0	0	1	0	1	1	1	0	1	DWL 112 XX2 (byte XX1)	
114	LO2 OFFSET DAC PRESTEER	NEW	W	YES	YES	A2	D7 MSB	D6	D5 LOOP BACK	D4	D3	D2	D1	D0 LSB	1	0	1	1	1	1	1	1	1	0		

LINES THAT CHANGED:				
MIKE		10,15,22, 26,27,36, 39,112		
MARK		61		
OGGI		45,96,97, 106		
ALAN		14, 17, 20, 51	Aug-97	