2.6 SPECTRUM INTERFACES

2.6.1 SZV11 Multiplexer

The SZV11 is a Q-bus RS232C asynchronous 8-line multiplexer, functionally compatible with DEC's DZ11 or DZV11, but with many added features.

Use of dual UARTs and a microprogrammed state machine has enabled 8 lines to be compressed into a dual height board. Other features include:

Per-line programmable baud rate, character length, parity, stop bits, and transmitter enable. The SZV11 provides plug selectable options to the baud codes to permit access to newer faster rates (19,200 and 38,400 Baud) and to various popular split receive/transmit rate pairs.

Miniature movable configuration plugs permit easy selection of base address, interrupt vector, interrupt priority, and baud rate table; without the use of tools, and without the bad contacts and easy upsetting of DIP switches.

Received characters are stored in 4-character per-line first in first out silos, and then referred to a 64-character common silo. This allows substantial bursts of heavy input activity to be supported during periods of CPU unavailability and then efficiently processed later, eliminating the risk of lost input.

The SZV11-A circuit board communicates with external signals via a 50-way BERG style header. When the SZV11-B, -C, or -D options are present (refer SZV11 Configuration Options, paragraph 3.2), the eight communication lines are brought out individually to standard 25-way female RS232C connectors mounted on a distribution panel.

Sufficient I/O control lines (RING, CARRIER, and DTR) are provided for full duplex dial-up auto-answer operation.

2.7 NON-SPECTRUM INTERFACES

The backplane of the SPECTRUM ELEVEN is Q-bus compatible. Most independently sourced Q-bus interfaces (with the exception of memory) can be used in the Spectrum backplane.

INTRODUCTION

The SZV11 is a dual-height asynchronous multiplexer interface module that inter-connects the Q-bus with up to eight asynchronous serial data communications channels. It offers full modem control and EIA type interface. The SZV11 also features selectable baud rates of 50 to 38,400, and configuration for different serial data format parameters which includes character length, number of stop bits, and parity.

This chapter discusses the SZV11's internal registers and the function of each bit.

5.1 DEVICE REGISTERS

There are six addressable registers in the SZV11 which are addressed by only four addresses. These registers have been defined as:

- Control and Status Register (CSR)
- Receiver Buffer Register (RBUF)
- Line Parameter Register (LPR)
- Transmit Control Register (TCR)
- Modem Status Register (MSR)
- Transmit Data Register (TDR)

Registers RBUF and LPR, and MSR and TDR, are differentiated using Read Only and Write Only instructions. Consequently, DATIP (read-modify-write) instructions may not be used with addresses 76xxx2 and 76xxx6.

CONTROL AND STATUS REGISTER - (CSR)

The CSR register (Figure 5-1) contains the status of flags and control bits for line scanning, interrupts, and clearing. Write-only and not-used bits are read as zeros. Read-only bits are not affected by attempts to write into them.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TRDY	TIE	SA	SAE		TLINE C	TLINE B	TLINE A	DONE	RIE	MSE	CLR	MNT			

Figure 5-1 Control and Status Register (CSR)

CSR<03> - Maintenance (MNT)

When set, causes the serial data from the transmitters to be looped back to the corresponding receivers. Cleared by CLR or INIT. Note that there may be up to 40ns delay between setting this bit and the loopback function being invoked on all lines.

CSR<04> - Clear (CLR)

When set, clears the receiver silo, all UARTs, and the Control and Status Register. Following CLR, the CSR and line parameters must be loaded again.

CSR<05> - Master Scan Enable (MSE)

Enables scanning of receivers, transmitters, and silo. Cleared by CLR or INIT.

CSR<06> - Receiver Interrupt Enable (RIE)

Enables receiver interrupt. Cleared by CLR or INIT.

CSR<07> - Receiver Done (DONE)

DONE is set by hardware, generating a receive interrupt if RIE is set, and SAE is cleared. DONE is cleared when the RBUF is read and is set again when the next word reaches the RBUF. If RIE is cleared, DONE may be used to indicate that the silo contains a character. If SAE is set, DONE has the same effect but does not generate interrupts.

CSR<08-10> - Transmit Line (TLINE)

If TRDY is set, TLINE A, B, and C indicate the number of the line which is ready to transmit a character. TRDY is cleared when the character is loaded into the transmit buffer, but is set again if another line is ready to transmit. These bits return to select line 0 following CLR or INIT. The line numbers are read as follows:

BIT	10	09	08	=	LINE
	0	0	0	=	1
	0	0	1	=	2
	0	1	0	=	3
	0	1	1	=	4
	1	0	0	=	5
	1	0	1	=	6
	1	1	0	=	7
	1	1	1	=	8

CSR<12> - Silo Alarm Enable (SAE)

SAE enables the silo alarm, preventing DONE from generating interrupts. When RIE is set, SAE allows SA to cause an interrupt after 16 entries to the silo. If RIE is cleared, SA may be used as a flag. Cleared by CLR or INIT.

CSR<13> - Silo Alarm (SA)

SA is set by hardware when 16 characters have been entered into the silo. If RIE is set SA causes an interrupt. SA is cleared when the RBUF is read, and is cleared by either CLR or INIT. When SA is set, the silo must be emptied because SA will not be set again until 16 characters have again entered the silo.

CSR<14> - Transmit Interrupt Enable (TIE)

TIE allows an interrupt to be set if TRDY is set.

CSR<15> - Transmitter Ready (TRDY)

TRDY is set by hardware when the scanner finds a line with its transmit buffer empty, and with its line enable bit set. TRDY is cleared when the TBUF register is loaded, and is cleared by CLR or INIT.

RECEIVER BUFFER REGISTER - (RBUF)

The Receiver Buffer Register (Figure 5-2) contains the received character bits, along with line number, error status, and valid data flags. RBUFis accessed by a read-only operation, using only word (not byte) instructions. A character will be lost if either the TST or BIT instruction is used. MSE bit 05 in CSR must be set for RBUF to operate.

Each time RBUF is read, characters are advanced through the silo and the next character becomes available to the program. A CLR or INIT operation empties the silo and causes RBUF bits 00-14 to become invalid. DV is cleared to zero by either CLR or INIT.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DV	OVRN	FE	PE			RLINE		RB	RB	RB	RB	RB	RB	RB	RB
					C	B	A	D7	D6	D5	D4	D3	D2	D1	D0

Figure 5-2 Receiver Buffer Register (RBUF)

RBUF<00-07> - Received Character (RB)

The received character RB read from the bottom of the silo. If the character length is less than eight bits, the higher-order bits are forced to zero.

RBUF<08-10> - Line Number (RLINE)

Encoded number of the line (1-8) through which the character was received. The line numbers are read as follows:

BIT	10	09	08	=	LINE
	0	0	0	=	1
	0	0	1	=	2
	0	1	0	=	3
	0	1	1	=	4
	1	0	0	=	5
	1	0	1	=	6
	1	1	0	=	7
	1	1	1	=	8

RBUF<12> - Parity Error (PE)

Bit set if received character had a parity error. Parity error bit is generated by hardware and does not appear in the RB data character.

RBUF<13> - Framing Error (FE)

Bit set if Stop bit did not appear in the predicted position as the character was received. This bit may be used for Break detection.

RBUF<14> - Overrun Error (OVRN)

Bit set if a character is received by a full silo before the current RB is read, causing receiver buffer to overflow. A character is lost but the received character put in the silo is valid.

RBUF<15> - Data Valid (DV)

Bit set if character read from RB is valid. An empty silo (invalid character) is indicated when DV bit 15 is cleared. Cleared by CLR or INIT.

LINE PARAMETER REGISTER - (LPR)

The 16-bit write-only LPR (Figure 5-3) contains the programmed line parameters for each line. Bits 00-02 select the line for parameter loading. Parameters must be reloaded following CLR bit 04 in CSR or INIT. Note that BIS or BIC instructions, or byte operations, are not allowed.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
			RCVR ON		FREQ D	C	B	A	OEP	PE	STOP	CL	CL	LINE C	B	A

Figure 5-3 Line Parameter Register (LPR)

LPR<00-02> - Line Number (LINE)

Encodes the number of the serial line for which parameter information is to be loaded. The line numbers are read as follows:

BIT 02	01	00	=	LINE
0	0	0	=	1
0	0	1	=	2
0	1	0	=	3
0	1	1	=	4
1	0	0	=	5
1	0	1	=	6
1	1	0	=	7
1	1	1	=	8

LPR<03-04> - Character Length (CL)

Number of bits in the data character (not including parity bit). The character bits are as follows:

BIT 04	03	=	CHAR.BITS
0	0	=	5
0	1	=	6
1	0	=	7
1	1	=	8

LPR<05> - Stop Code (STOP)

Sets number of stop bits. 'Zero' = one-unit stop. 'One' = two-unit stop, or 1.5-unit stop for a 5-bit character length.

LPR<06> - Parity Enable (PE)

If set, parity is enabled for both transmit and receive. If not set, parity is disabled.

LPR<07> - Parity (OEP)

Set = odd parity. Not set = even parity. PE must be set to enable parity.

LPR<08-11> - Baud Rate Select (FREQ)

Plug selectable options permit various receive/transmit rate pairs.

Baud Rate Table Selection Plug (L1)

Baud Code	Plug L1=1		Plug L1=0	
Bits (11-08)	Receive	Transmit	Receive	Transmit
0000	75	600	50	50
0001	75	75	0	0
0010	110	110	110	110
0011	134.5	134.5	134.5	134.5
0100	150	150	200	200
0101	300	300	300	300
0110	600	600	600	600
0111	1200	1200	1200	1200
1000	1800	1800	1050	1050
1001	2000	2000	0	0
1010	2400	2400	2400	2400
1011	75	1200	0	0
1100	4800	4800	4800	4800
1101	75	2400	7200	7200
1110	9600	9600	9600	9600
1111	19200	19200	38400	38400

LPR<12> - Receiver On (RCVR ON)

If set, enables receiver. Bit is turned off by either CLR or INIT. (Note that the transmitter clock is always on).

TRANSMIT CONTROL REGISTER - (TCR) %xx04

15															00
DTR 7	DTR 6	DTR 5	DTR 4	DTR 3	DTR 2	DTR 1	DTR 0	LE 7	LE 6	LE 5	LE 4	LE 3	LE 2	LE 1	LE 0

Figure 5-4 Transmit Control Register (TCR)

The Transmit Control Register (Figure 5-4) contains two bytes. The low-byte contains eight bits selecting one of eight lines. The line is selected to transmit when the related bit is set. The low byte is cleared by either CLR or INIT. The high byte contains Data Terminal Ready bits, one for each line. Cleared only by INIT.

MODEM STATUS REGISTER - (MSR) 06

15															00
CO 7	CO 6	CO 5	CO 4	CO 3	CO 2	CO 1	CO 0	RI 7	RI 6	RI 5	RI 4	RI 3	RI 2	RI 1	RI 0

Figure 5-5 Modem Status Register - (MSR)

The read-only Modem Status Register (Figure 5-5) contains two bytes. The low byte monitors and contains the status of each line's Ring Indicator (RI) lead. The high byte monitors and contains the status of each line's Carrier (CO) lead.

The MSR is not cleared by either CLR or INIT.

TRANSMIT DATA REGISTER - (TDR) %xxx06

15															00
BRK 7	BRK 6	BRK 5	BRK 4	BRK 3	BRK 2	BRK 1	BRK 0	TB 7	TB 6	TB 5	TB 4	TB 3	TB 2	TB 1	TB 0

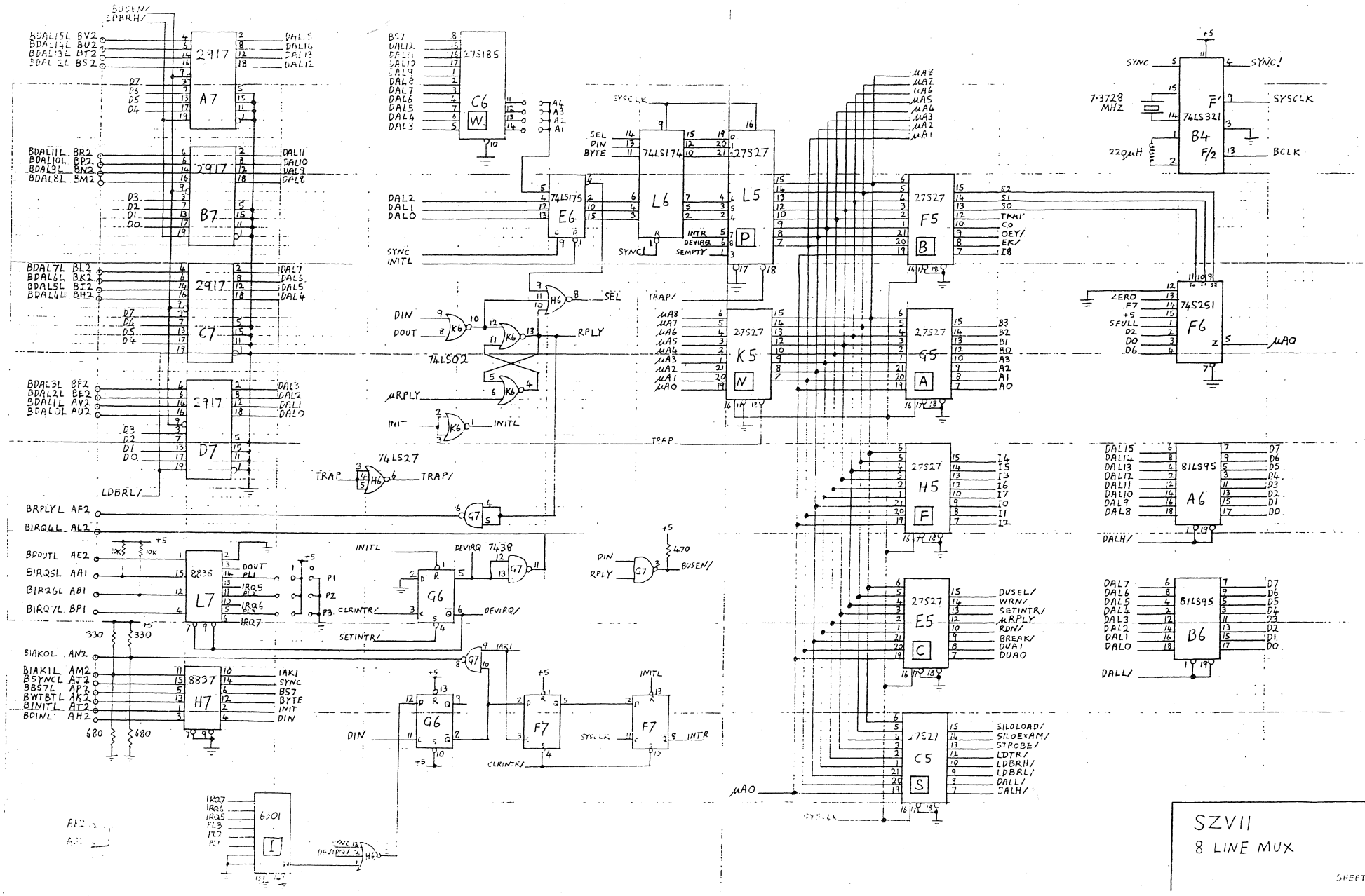
Figure 5-6 Transmit Data Register (TDR)

The Transmit Data Register (Figure 5-6) contains two bytes. The low byte is the transmitter buffer register (TB) and contains the character to be transmitted. The high byte contains a Break bit for each line. When a Break bit is set, the related line begins sending zeros continually until the bit is cleared. The entire register is cleared by either CLR or INIT.

BIS or BIC instructions cannot be used. A character loaded into the TB must be right-justified if it has fewer than eight bits.

5.4 SZV11 CONNECTIONS

Signal & Description	25-way RS232C	50-way BERG header Line 0	1	2	3	4	5	6	7
TRANSMIT DATA Data transmitted from SZV11 to external equipment	3	19	23	27	31	35	39	43	47
RECEIVE DATA Data transmitted from external equipment to SZV11	2	21	25	29	33	37	41	45	49
DATA TERMINAL READY Status sent by SZV11 to external equipment indicating readiness to receive data	20,4,25	1	3	5	7	9	11	13	15
CARRIER Status sent by external modem to SZV11 when carrier is detected on communications line	8	2	4	6	8	10	12	14	16
RING Status sent by external modem to SZV11 announcing an incoming call	22	20	24	28	32	36	40	44	48
GROUND Signal ground	1,7	22	26	30	34	38	42	46	50

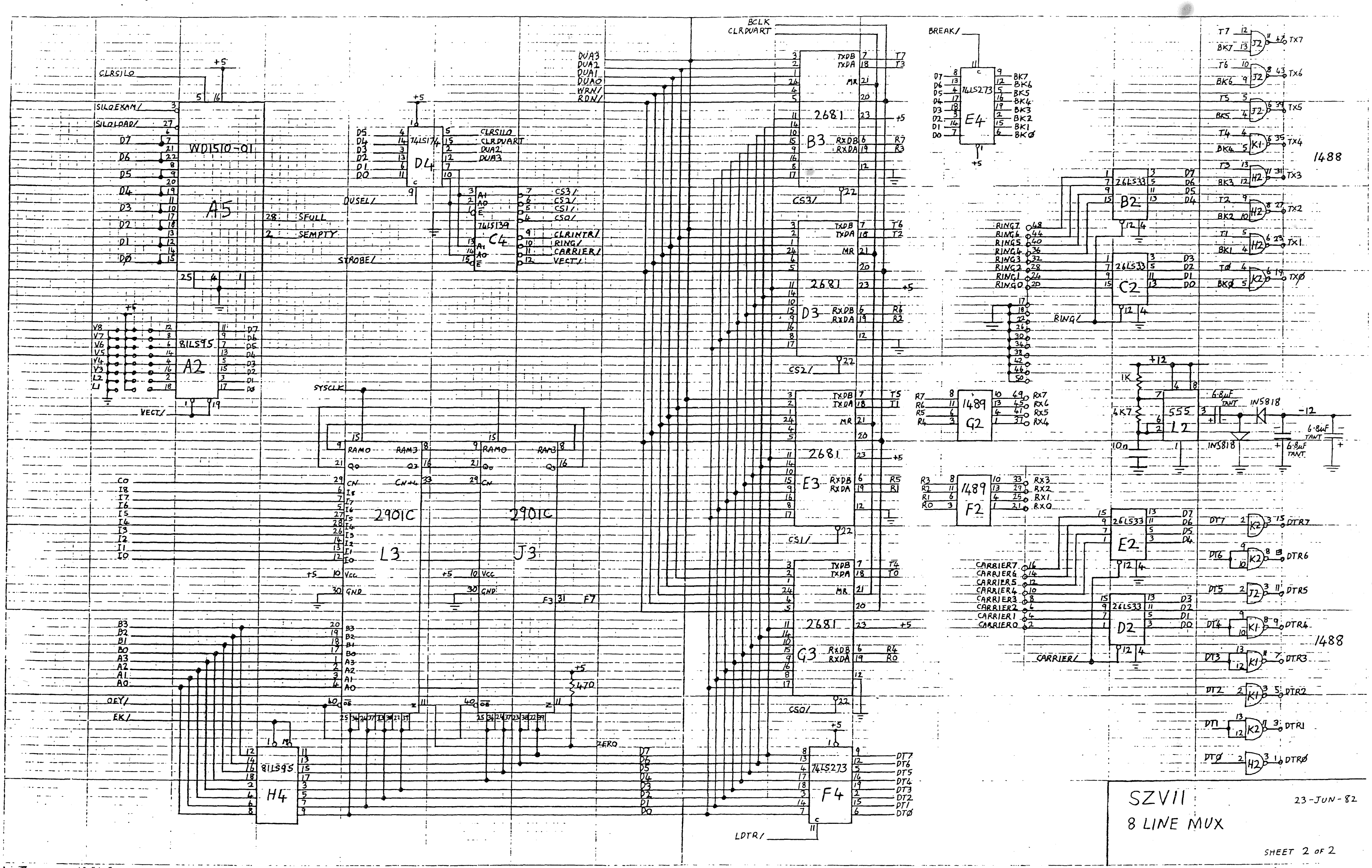


SZVII

8 LINE MUX

23-JUN-82

SHEET 1 OF 2



SZV11
8 LINE MUX

23-JUN-82

SHEET 2 OF 2