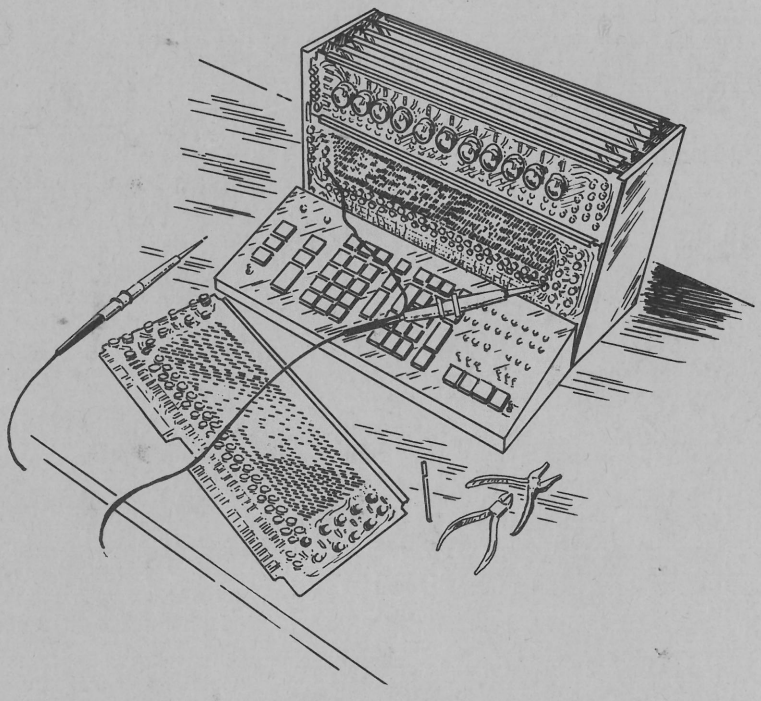
L55-67

Wang LOCI

Service Manual



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FOREWORD

This manual will be revised periodically for the purpose of providing accurate, up-to-date information to all field personnel and LOCI users.

Meanwhile, when new information is not of such volume as to require a complete revision of the manual, change pages will be distributed for easy insertion to keep the manual updated at all times pending the publication of the revised manual.

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I. INTRODUCTION

A. SCOPE

This manual is intended for use by those who have had experience in and some exposure to electronic computer technology. Specifically, its purpose is to aid repair personnel in LOCI malfunction isolation and/or correction and, in some cases, to provide enough information to enable the service man to correct the problem.

The manual contains general and technical description of the componentry, electronic and mechanical, of the LOCI. The information presented, together with discussion of some of the more common malfunctions, is deemed adequate to provide the LOCI user with the necessary knowledge to effect a solution for any problem.

Information contained in this manual shall not be construed by the user, however, as authorization to modify the design of the LOCI.

B. LOCI CONFIGURATIONS

LOCI–1 - No longer in production; it was the basic unit, having no storage or programming capabilities.

LOCI–2 - Now the basic unit; it has storage capability, as well as 80 steps of program capacity (one reader).

LOCI–2a - The basic LOCI–2, with 16 storage registers and 80 steps of program capacity (one reader).

LOCI–2s - The LOCI–2, without program option or storage capacity.

LOCI–2S2 - The LOCI–2, without program option, but with 2 storage registers.

LOCI–2S4 - The LOCI–2, without program option, but with 4 storage registers.

C. POSSIBLE COMBINATIONS

The following suffix letters indicate possible combinations with the basic LOCI, each suffix representing optional peripheral equipment which can be added to the basic unit.

(a) A second card reader option, possible with LOCI–2 or LOCI–2a.

NOTE: The following options are available only with the LOCI–2a.

(b) Teletype Model 33 Input/Output Writer.

(c) Presin Printer.

(d) Teletype and Control Unit 3 (CU-3).

II. COMMAND DEFINITIONS

LOCI Command	LOCI Key	LOCI Code	Definition
Clear Error	CLEAR ERROR	(01)	This command is given to clear or turn off the error indicator light, which becomes illuminated when the contents of the log register exceeds the limits. The log-register limits are -41.999 999999 to 41.999 999999.
Clear W-Register	CLEAR W	(02)	This command is given to clear the work, or display, register. When this command is executed, the LOCI will display zeros. It also returns the Memory Selection (MS) Counter to zero.
Clear Accumulator	CLEAR A	(03)	This command is given to clear the contents of the A-register only.
Square Root	$\sqrt{}$	(04)	This command is a mathematical operation which calculates the square root of the W-register and adds that root to the L-register. $L+\frac{1}{2}\log_e(W) \longrightarrow L$
Reciprocal of the square root	$1/\sqrt{}$	(05)	When this command is given, the LOCI takes the contents of the W-register, calculates the reciprocal of the square root, and adds the log of the reciprocal of that root to the L-register. $L-\frac{1}{2}\log_e(W) \longrightarrow L$
Square	$\square$	(06)	This command takes the contents of the W-register, calculates the square, then adds twice the log of the square in the L-register. $L+2\log_e(W) \longrightarrow L$
Reciprocal of the square	$1/\square$	(07)	When this command is given, the LOCI takes the contents of the W-register and calculates the reciprocal of the square, then adds the log of that reciprocal to the L-register. $L-2\log_e(W) \longrightarrow L$
Memory Selection Counter	STEP MSC	(10)	This is a command which selects or designates which group of storage registers is active. Each group has four registers and each group assumes an MS value which corresponds to the value of the first register in that group. MS values are 0, 4, 8, and 12. The quantity of storage registers is dependent on the type of LOCI used in the operation.

COMMAND DEFINITIONS

LOCI Command	LOCI Key	LOCI Code	Definition
Write	WRITE	(11)	The WRITE command obtains a printout of what is displayed on the W-register. Printouts can be obtained from connected Teletype machines, which can produce both a punched tape and/or a regular paper printout to command the Presin Printer to print.
Multiplication	X	(12)	This command multiplies the content of the W-register by the contents of the L-register. At the completion, the product will be in logarithmic form in the L-register. In fact, the × operation adds the log of W to L. $L+\log_e(W) \longrightarrow L$
Addition	+	(13)	This operation adds the contents of the W-register to the contents of the A-register. At completion, the sum, or total, is in the A-register. $A+W \longrightarrow A$
Anti-log	ANTI LOG	(14)	This command takes the anti-log of the contents of the log register and displays the answer in the log form. At completion of the command, the L-register is cleared.
Subtraction	–	(15)	This command subtracts the contents of the W-register from the contents of the A-register.
Decimal Point	.	(16)	This command places a decimal point in the LOCI at the appropriate place. It can be used only once on each display. The decimal point is entered in the W-register only.
Division	÷	(17)	This command divides the contents of the log register by the contents of the W-register.
Numbers 0 thru 9	0 1 2 3 4 5 6 7 8 9	(20) (21) (22) (23) (24) (25) (26) (27) (28) (29)	Each of these commands enters a digit into the W-register in succession, starting with the high-order number, or left-hand side of the display.

COMMAND DEFINITIONS

LOCI Command	LOCI Key	LOCI Code	Definition
Run	RUN	(32)	This operation is directly dependent on the Mode Selection Switch, which has three positions, STEP, AUTO, and MNL. When the switch is in any one of these positions, there are other dependents which must be considered. The switch advances the program by 1 step in STEP mode, continues the program which might have been stopped intentionally in the AUTO mode, and executes the command manually when indicated by toggle switches in MANL mode.
Sign $\pm$	CHANGE SIGN	(33)	This command changes the sign of the contents of the W-register only. It will not affect the contents of the register per se.
Input MX		(34)	These are special option commands used with peripheral equipment.
Output MX		(35)	
Prime	PRIME	(36)	This operation clears the W, A, and L registers and the Memory Selection Counter. It puts zeros into the three registers, and gives a zero value to the MSC.
Stop		(37)	This command stops the program. When it is given, the calculating halts, as does any equipment (Teletype, etc.) connected to the LOCI.
Work Register to Program Counter (PC) W $\longrightarrow$ PC		(40)	This command alters the value of the PC. It takes the first two digits regardless of the position of the decimal point in the W-register and places the number into the PC. This command gives freedom of movement within the program. (The PC is a light indicator which indicates the location of the command to be executed on the program.)
W $\longrightarrow$ XPC		(41)	This command is similar to the W $\longrightarrow$ PC with the exception that it changes the sign to negative, the reason being that this will select the second card reader. (It will also light up the X-light on the PC.)
Work Register to Decrement Counter (DC) W $\longrightarrow$ DC		(42)	This command puts the first two digits of the W-register into the DC if the decimal point is in the second position. If there is only one decimal point position, only one digit enters the DC. The functions of the DC are to control the number of iterations which has been predetermined, or to count the number of times a sequence has been performed.

COMMAND DEFINITIONS

LOCI Command	LOCI Key	LOCI Code	Definition
DC $\longrightarrow$ W		(43)	This command is the converse of W $\longrightarrow$ DC, and takes the contents of the DC and puts it in the W-register. This option does not destroy the contents in the DC.
Work Register to Accumulator Register W $\longrightarrow$ A		(44)	This command enters the contents of the W-register into the A-register. It does not destroy the contents of W.
Accumulator Register to Work Register A $\longrightarrow$ W		(45)	This command is the converse of W $\longrightarrow$ A, and it will not destroy the contents of A.
Work Register to Log Register W $\longrightarrow$ L		(46)	This command puts the log of the contents of W into L. It will not destroy the contents of W. However, if the contents of W are 100, the Error Indicator will light, indicating that the limits of L have been exceeded. If W 10.00000, W will be re-aligned to the xx. xxxxxxxx$_e$ format.
Log Register to Work Register L $\longrightarrow$ W		(47)	This command puts the contents of L into W, and clears the contents of L after the operation.
Store PC, DC, then W $\longrightarrow$ PC		(64)	This command causes the following events: PC $\longrightarrow$ PCS (PC Storage) DC $\longrightarrow$ DCS (DC Storage) W $\longrightarrow$ PC Information previously stored in PCS and DCS will be destroyed when this command is executed, and the contents of PC and DC will be put into the PCS and DCS registers. The DC register will remain the same, and the PC register will now have the contents of W.
Recall PC and DC		(65)	This command exchanges the contents of the PC and PCS, and puts the contents of DCS into the DC. PCS $\longleftrightarrow$ PC DCS $\longrightarrow$ DC
Decrement		(66)	This command reduces the contents of the DC by one.

COMMAND DEFINITIONS

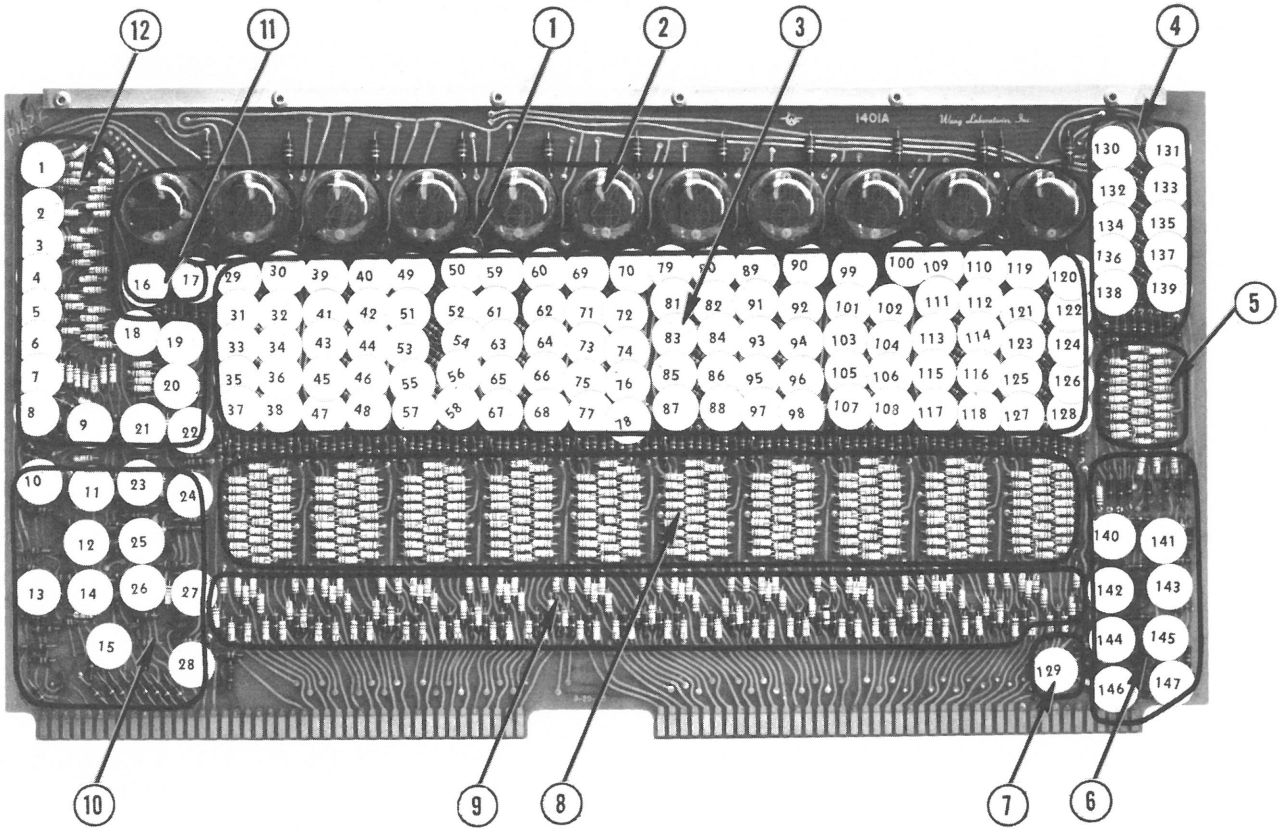
LOCI Command	LOCI Key	LOCI Code	Definition
The following test commands are program tools to maneuver within the program when certain conditions exist:			
Test Error:		(67)	If there is no overload of any register, this command advances the PC by four counts. If an overload exists, it advances the PC by one count. There is no effect on the contents of any register.
Test DC = 0		(70)	If DC is zero, this command advances the PC by four counts. If DC is not zero, it advances the PC by one count. There is no effect on the contents of any register.
Test A = 0		(71)	If A is zero, the command advances the PC by four counts. If A is not zero, it advances the PC by one count. There is no effect on the contents of any register.
Test W = 0		(72)	If W is zero, this command advances PC by four counts. If W is not zero, it advances PC by one count. There is no effect on the contents of any register.
Test W for - sign		(73)	If W is negative, the command advances the PC by four counts. If W is not negative, it advances the PC by one count. There is no effect on the contents of any register.
Test L for - exponent		(74)	If the contents of L are negative, the command advances PC by four counts. If L is not negative, it advances PC by one count. There is no effect on the contents of any register.
The following commands are used with some of the optional equipment available, namely, the Teletype:			
Carriage Return	CAR'GE RETURN	(75)	This command can make the Teletype carriage return, and also make it skip to a new line if needed.
Read	READ	(76)	This command obtains information from the Teletype machine reader, which supplies the LOCI with an input from a paper tape.
Read	READ	(77)	This command obtains information from a second tape reader which supplies the LOCI with an input from a paper tape.

III. CIRCUIT CARD DESCRIPTIONS

The LOCI (LOgarithmic Computing Instrument) is an electronic computing machine containing a number of printed cards. Each LOCI contains from 8 to 11 cards, depending upon the machine model. Each card is described herein in detail.

A. GENERAL, TECHNICAL, AND PHYSICAL

The descriptions on the following pages are accompanied by illustrations of the numbered cards which are to assist the user and the technician to locate specific circuitry.



1401A CARD

1. Decimal Point Position (Neon Bulb)
2. Readout Tubes
3. Transistor Drives for Readout Tubes
4. Blanking Circuit
5. Blanking Circuit Decoder Network
6. ER Counter Circuit
7. Input Driver to Blanking Circuit
8. Decoding Circuit for Readout Tubes
9. Control Circuits for Data Traveling between cards
10. DCN Counter Circuits
11. Sign Circuits (SN)
12. Decimal Point Positioning Circuits

Note 1:
(Number on the Transistor corresponding with the digit controlled by that transistor. Each of the ten circuits are the same)

1401A Card

This card contains 11 readout* tubes. The first card is for the sign (plus or minus); the others are for each of the 10 digits in the W-register.

There are 10 neon bulbs for positioning the decimal point. The card also contains associated decoding for displaying the sign, 10 digits, and a decimal point of the W-register. In addition, it contains the W-register decimal-point counter and a digital counter for processing the logarithmic operations.

The diagram of this card shows the locations of the various circuits. The 11 readout tubes are located across the top of the card, and directly below each readout tube is a series of transistors (either Type 35224 or Type S16393), which are used to drive the tubes.

Below the transistor drivers are the germanium diodes which, with the transistors, comprise the decoding circuits of the readout tubes.

At the bottom of the card, and centered, is a series of germanium diodes and resistors comprising the control circuits for the data traveling between cards.

In the lower right-hand corner of this card is the Entry Memory (EM) register counter circuit, which consists of four (4) flip-flop circuits. The ER counter indicates which digit is to be entered. It also is used to process either number-to-log or log-to-number functions. The ER is a binary coded decimal (BCD) counter, next to which is the transistor circuitry for entry to the card of the input-blanking signal.

The decimal-point position drivers and decoding circuits are located in the top left-hand corner of the card. The Work-Register (W) decimal counter (DCN) circuit is located in the lower left-hand corner. This circuit consists of four (4) flip-flop circuits.

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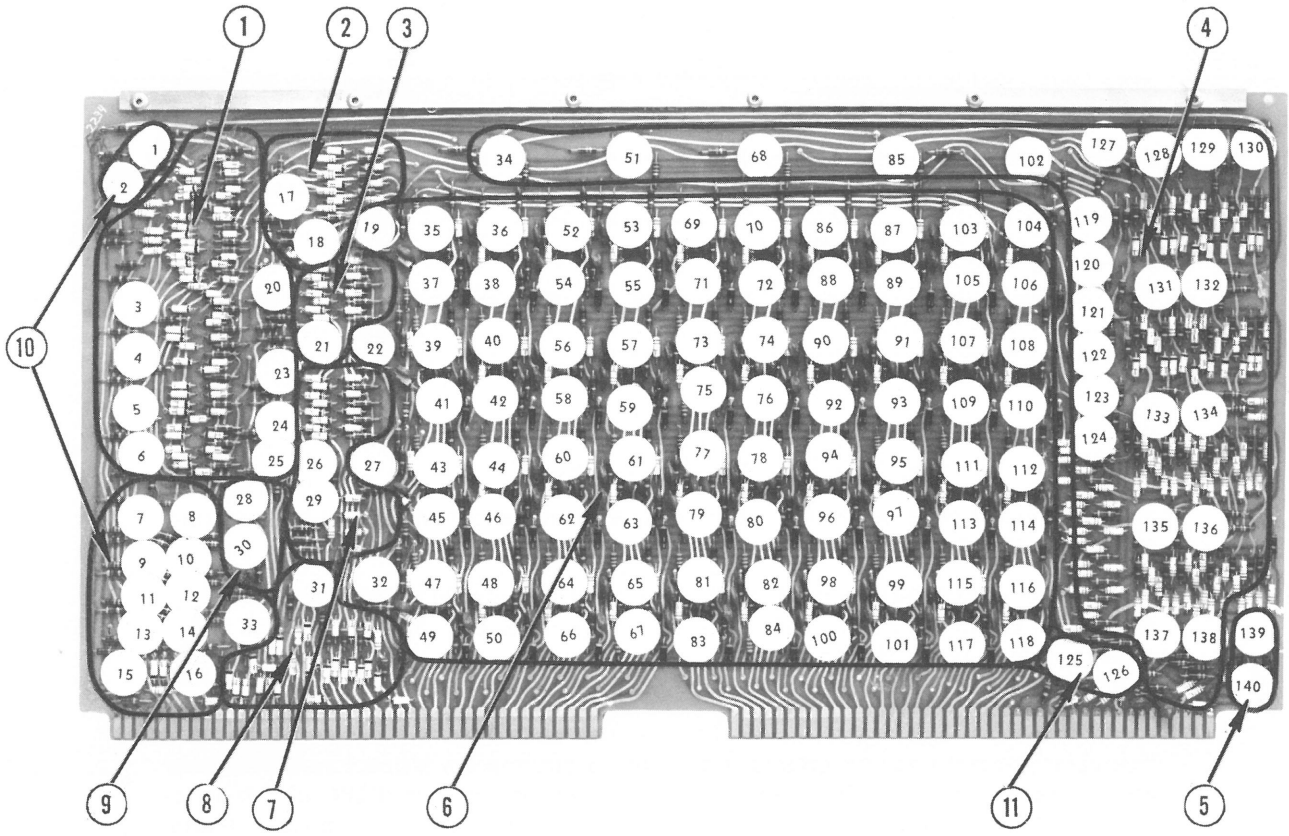
*These tubes heretofore had been called NIXIE tubes, but since NIXIE is a trade name of a component no longer used at Wang Laboratories the name has been changed in this manual to "readout" tubes to describe their function more closely.



1402A CARD

1. Number Register Adder Result circuit.
2. Number Register Result circuit. (ms, s19, nld, cai, ent, sm, ld.)
3. Control Circuit for the command A–W.
4. Binary Adder circuits.
5. Control circuit for one of the Anti-Log Function signals (CC).
6. Circuitry for the ten digits of the Work Register (NR).
7., 8. Control circuits for the following signals:
   a) Decoder for the log process output
   b) Memory Select
   c) Decrement Counter.
9. Shift Pulse Signal Circuit.
10. Adder input control signal.
11. Control to Accumulator Register. Stepping. (ASR)

1402A Card

This card contains the 10 digits of the W-register, plus the binary adder used in addition, subtraction, and processing of numbers during log and anti-log operations. It performs the steps for anti-log generation and also the carry-gate process for carry-over of digits.

The diagram indicates the location of the various circuits on this card, in the center of which are 80 transistors and the componentry to form the 10-digit W-register storage units.

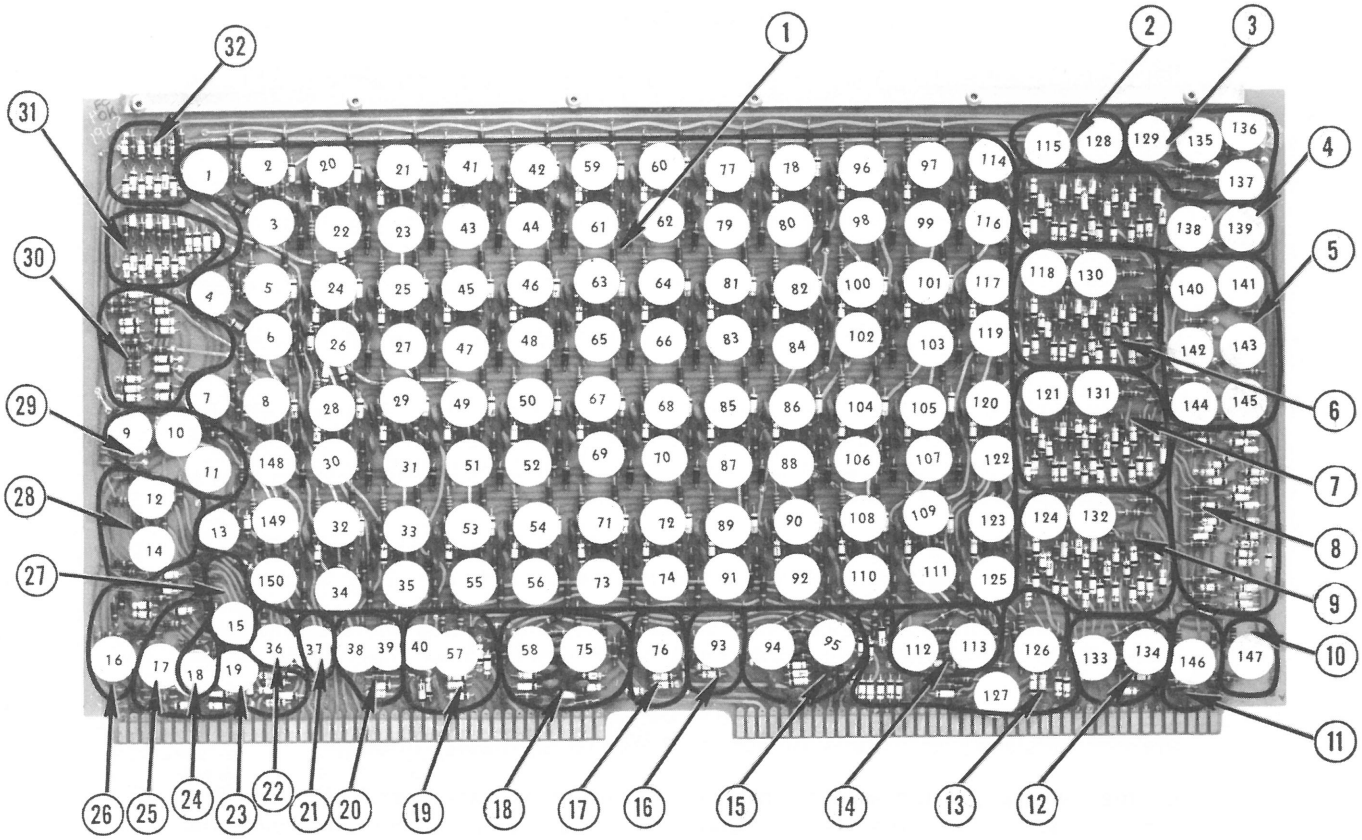
Directly to the left of these units are four transistors which comprise the input for the W-register storage.

The four transistors across the top center of the card and all transistors, with the exception of two on the right-hand side, form the Binary Adder circuit. The two transistors in the lower-right center are the DC level control of the 9's complement circuit, between the W-register and the W-register Adder and its indicator.

In the lower right-hand corner are two transistors which are part of a flip-flop network. When this network is OFF, it indicates that the W-register is over.9999999999.

The two transistors in the upper left-hand corner and the 11 transistors in the lower left-hand corner form the driver and decoding circuits for the Adder input signal. There are nine transistors which are located on the left-hand center of the card, which form the driver and decoding circuits for the Adder output signal. At the lower left-center are two transistors which form the number W-register shift-pulse circuit.

On the right-hand center are six transistors, of which four are used to drive the following signals: two drive the CAI, ENT, SM, and LD signals; the other two drive the MS, S19, and NLP 13 signals (refer to signal definitions).



1403A CARD

1. Circuitry for the storage of the log register information (Bin 1, 2, 4, 8)
2. Circuit for the log register shift pulse (LR)
3. Log Register Adder result circuit
4. Binary 8 (9's complement input circuit)
5. Binary 2, 4 and 8 Adder output
6. Binary 4 (9's complement input circuit)
7. Binary 2 (9's complement input circuit)
8. Log Register mixer circuit
9. Binary 1 (9's complement input circuit)
10. Binary 1 carry circuit
11. Gate circuit for the carrier memory of the log register
12. Carrier memory of the log register circuit (C1)
13. Blocking signal when error has accumulated circuit (LDE)
14. Same as thirteen (LDE)
15. Memory of number sign of the log register circuit (LSN)
16. Control gate for (#15) (LSN)
17. Control gate for (#18) (SN)
18. Memory of the sign of the work register (SN)
19. Main reset of the log register circuit (LRS)
20. Circuit which indicates zero in the log register (LR0)
21. Circuit indicating a number 1 or greater at the end of an anti-log operation (MS)
22. Circuit controlled by memory select used to shift a 1 into the Work Register under certain conditions (MSP)
23. 24. 25. Control circuits for "S" signals (S_1, S_2, S_{16})
26. Control gate for the error signal (ERR)
27. Pulse generator circuit (LTP)
28. Circuit for the error signal (ERR)
29. Circuit indicating positive or negative log (ML)
30. Decoder circuit for log and anti-log process (PA)
31. Control circuit for the W–L command (LD)
32. Control circuit for the Log Register Adder results and log and anti-log process (PA)

1403A Card

This card consists of 12 digits of log information, with a fixed decimal point of two places. It also contains a Binary Adder used to add and subtract log constants generated by the log generator. The card also contains the following miscellaneous circuits:

a) The sign of the W-register,
b) The error-light circuits,
c) The sign of the real numbers in the L-register, and
d) Shift pulse, S_1, S_2, S_{16} (refer to signal definitions).

The center of the 1403A card contains 96 transistors which, with associated components, make up 48 flip-flop networks, 12 each for Binary 1, Binary 2, Binary 4, and Binary 8.

In the upper right-hand corner are the circuits for the L-register shift pulse containing two of the transistors. The other four transistors are for the L-register adder results, one each for Binary 1, 2, 4, and 8.

Directly below these six transistors are 14 transistors, in groups of two. Four of these groups, with the associated components, form the Binary 1, 2, 3, and 8 circuitry for the 9's complement inputs. The other three groups are part of the Binary 2, 4, and 8 adder-output circuits.

Below the adder-output circuits are the components which form the L-register minus circuits.

The transistors in the lower right-hand corner are part of the Binary 1 carry circuit. Along the bottom of the card, moving from right to left, the second transistor is a part of the circuit which forms the gate for the carrier memory for the L-register adder. The next two transistors form the circuits for this carrier memory.

The next four transistors, of which two form a flip-flop network, are part of the circuit which serves as a blocking signal when an error has accumulated.

On the lower right center, there are three transistors which are part of the memory of the number sign of the L-register circuit. To the left of these are three transistors which are part of the memory of the sign of the W-register. Included in this circuitry is a flip-flop network.

Continuing to the right, the next two transistors are a part of the main reset of the L-register circuits. The next two are part of the circuit which performs function of giving the DC-level indicating zero in the L-register.

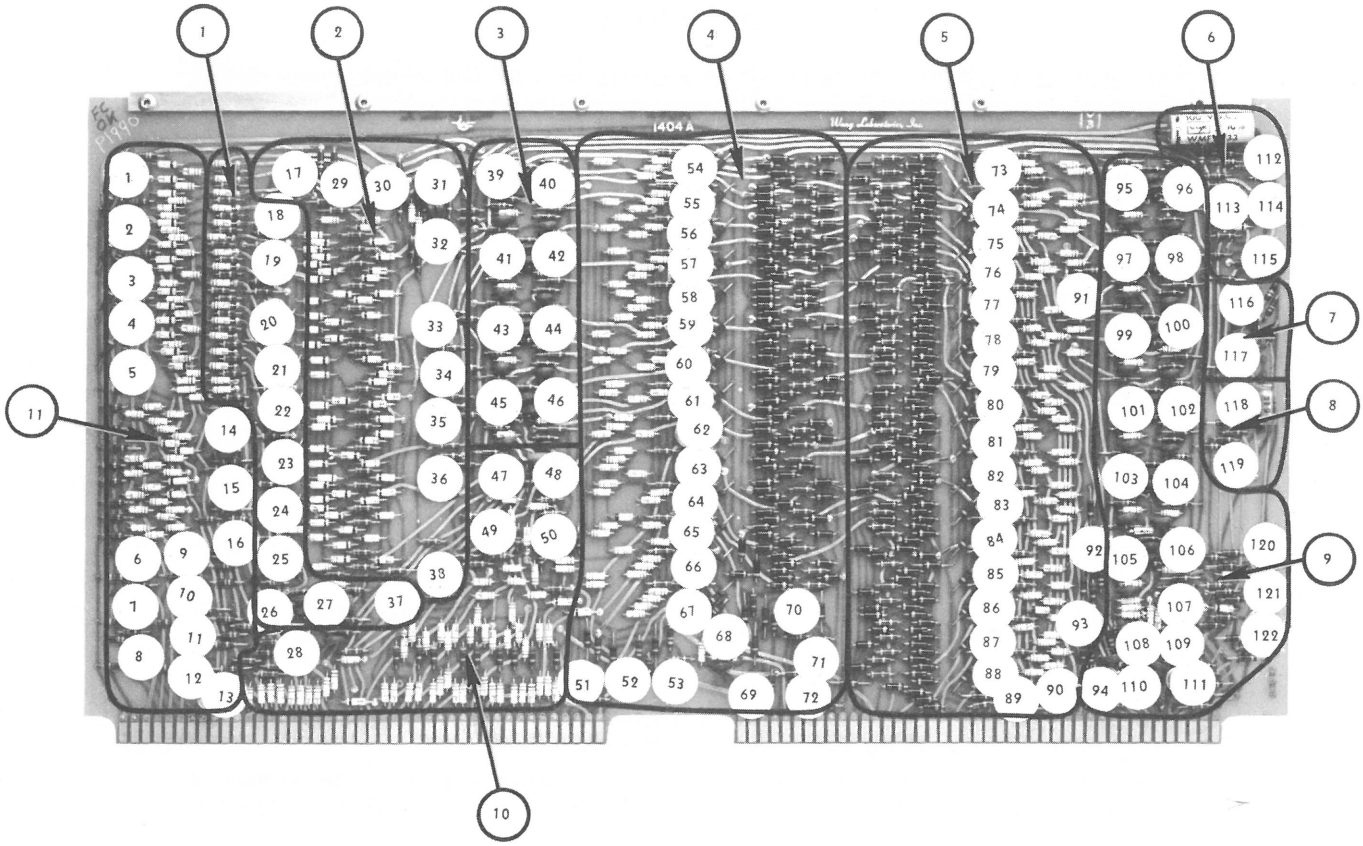
The next two are part of the memory-select circuit and the functions it performs. This gives a DC level, indicating that the number is greater than .9999999999 at the end of an anti-log operation. There also is a pulse, controlled by the memory select, which shifts a "1" into the W-register at the end of an anti-log operation, if the number is greater than .9999999999.

Of the next four transistors, one is for control of a 20-30 microsecond pulse, generated by the turning ON of the L-register transfer. The other three are S_1, S_2, and S_{16} signals, and their functions are as follows:

a) S_1 generates a pulse which steps the ER counter during the entrance of numbers.
b) S_2 generates a pulse which shifts the W-register during entrance of numbers.
c) S_{16} generates a pulse which shifts in the number of zeros left in the DCN, if the log was negative at the beginning of an anti-log.

The three transistors on the left-hand side, from bottom to top, are the error drivers and a flip-flop network. The next two are used in the circuit that gives the DC level, indicating a positive or a negative log.

Directly above these transistors is a group of components forming part of the pulse amplifier (PA) reset decoder circuit which is the master control flip-flop for log and anti-log processing. Above this circuit is the circuitry for control of the W-register to L-register transfer. In the upper left-hand corner is the circuitry for the L-register and the PA control.



1404A CARD

1. Timing control circuit for the entrance of numbers.
2. Timing control circuit for the binary numbers.
3. Log process (normally zero pulse) circuit. (CP)
4. Circuit for the decoded output of the log process. (NLP's 0-13)
5. Circuit for the decoding of the 16 step clock. (TD's 0-15)
6. Control circuit for a keyboard command and function pulse.
7. Circuit for the clock control signal.
8. Control circuit for a function pulse.
9. Circuitry for the two main timing pulse.
10. Control circuit for the log process (normally zero pulse) circuit.
11. Control circuit for control of the output of the LR's 9 complement signal.

1404A Card

This card contains the 16-step, main timing counter and associated timing pulses which control the entire LOCI. This card also contains the 14-step programmer and the log generator used in all log operations.

Along the left-hand side of the card are 16 transistors which comprise the circuitry for the L-register 9's complement. To the right of these complement circuits are two columns of transistors and their associated circuits, which are the decoding circuits for the following signals: EN_1, EN_2, EN_4, and EN_8, all of which originate on the 1405A card.

To the right of this circuitry, there are 13 transistors forming part of the log-process step (LPS), which is a pulse to step the log-process control.

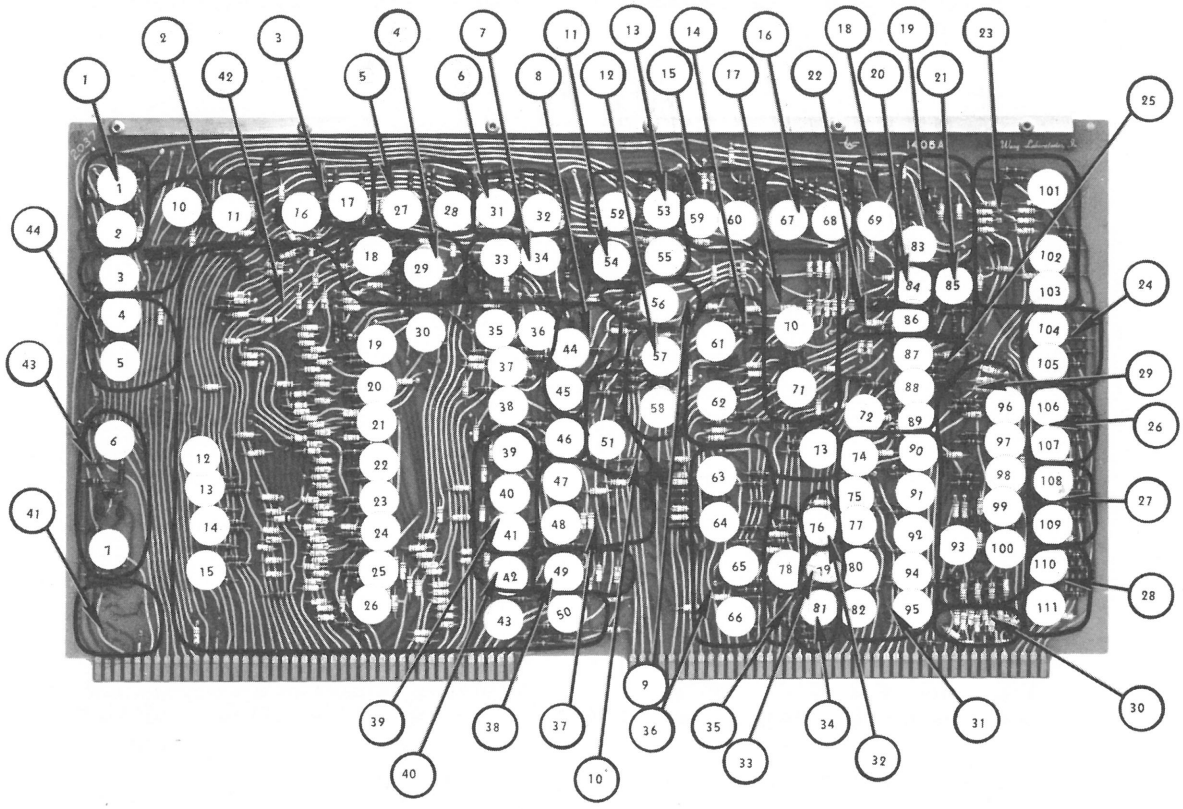
In the center of the card is a column of 14 transistors and eight more in a cluster at the bottom of the column. These 22 transistors form the circuitry which provides the decoded output of the log process.

To the right of this circuit a column of 16 transistors (five to the right of the column) forms the circuitry for decoding the 16-step clock used in each cycle of operation.

The next two columns and the three at the lower right-hand edge comprise the main timing-pulse circuits. They contain six flip-flop networks.

The four transistors in the top right-hand corner and the two just below the center on the right-hand edge form part of the circuitry for providing a signal to the keyboard.

There are two transistors just above the center of the right hand edge, and these are part of the clock control circuits.



1405A CARD

1. Gate control for the entrance of number. (ENT)
2. Circuit used to put zero's into the Work Register Adder. (NB)
3. Control circuit for the clock. (KC)
4. Control for the back space signal. (BS)
5. Circuit controlling the summing of the Work Register and the Accumulator Register. (SM)
6. Control circuit for aligning the decimal point between the Accumulator Register and the Work Register. (AD)
7. Pulse generator circuit (input is a DC level) (LND)
8. Circuitry controlling the transfer of the Log Register to the Work Register. (LT)
9. Circuit for memory of the negative log. (LND, ML)
10. Circuit for the carrier memory for the Work Register. (C1)
11. Circuit which controls the number to log or the log to number transfer. (LN)
12 Memory of negative log. (DM)
13. Circuit for controlling Work Register to Accumulator Register transfer. (LD)
14. Control circuit for the log and anti-log process. (NLD)
15. Circuit for the reset signal generated by RT. (RS)
16. Circuit that is set when the first number after an operation is entered into the LOCI. (RT)
17. Control circuits for Log and anti-log process. (DA)
18. Program reset circuit.
19. Nine's complement of number Register output control circuit. (NR)
20. Control circuit for functions from the Program.
21. Control circuit to blank the decimal light. (DCN)
22. Circuit to move decimal point to the left. (FM)
23, 24. Circuit for entrance of number control of log Generation and of add and subtract process. (EN1,2)
25. Control circuit for the number Register. (NR)
26, 27, 28. Same as #23. (EN2,4,8)
29. Same as #25. (NR)
30. Shift pulse circuit for the Log, Accumulator and the Number Register. (ACR, C, NR)
31. Control circuits for various signals coming from storage. (DCA AND DCN SET GATES)
32. Control circuit indicating a nine's complement signal between the Work Register and the Adder.
33. Control circuit for the main reset of the Log Register.
34. Circuit for the Accumulator Register reset. (ARS)
35. Circuit which moves the decimal point right.
36. Circuitry for the carrier memory of the Work Register. (C1)
37. Circuit for the memory of the Ro Gate. (R0)
38. Control circuit for a er shift pulse. (ER)
39. Control circuit for signals from storage to the decimal counter. (DCN)
40. Circuit to move decimal point to the right. (FP)
41. Pulse generator circuit. (not used)
42. Control circuits for S^S signals. (S^S)
43. Control circuit for a decoded output of the Log Process. (NCP2)
44. Control circuit for memory of the decimal point. (DP)

1405A Card

This card consists principally of miscellaneous circuits used throughout the entire LOCI. The majority of the circuits comprise shift pulses to control the A-, W-, and L-registers.

Because of the complexity of the circuits, the transistors have been numbered and these numbers coincide with the numbers on the diagram. A breakdown of the card circuitry follows:

Transistors 1 and 2 – These are part of the circuitry for the main gate-control flip-flop, for entrance of numbers.

Transistor 3 – This is part of the circuit which combines diode output of the L-register with output of a flip-flop, indicating number-to-log operation when OFF and log-to-number operation when ON.

Transistors 4 and 5 – These are part of the flip-flop network in a memory circuit used to enter the decimal point.

Transistors 6, 7, 8, and 9 – These are normally ON pulse generators.

Transistors 10 and 11 – These are part of a flip-flop network used to put zeros into the input of the W-register adder during the log operation.

Transistors 12 through 15, 19 through 26, 30, 35 through 38, 43, 46, and 50 – These transistors, and the associated components, form controls for some of the signals leaving the card.

Transistors 16 and 17 – These are part of the flip-flop network which controls the clock.

Transistors 18 and 29 – These are part of the flip-flop network used to control the back-space signal. (This circuit is not used on all LOCI models.)

Transistors 31 and 32 – These are part of the flip-flop network used to align the decimal point between the A- and W-registers.

Transistors 39, 40, and 41 – These are a part of a control circuit for the blank decimal lights.

Transistor 42 – This is part of the circuit which moves the decimal point to the right.

Transistors 44 and 45 – These are part of the flip-flop network used to control the transfer of the L-register to the W-register.

Transistors 47 and 48 – These are part of the flip-flop network used to control the signal from the W-register adder input, indicating a number of "5," or greater.

Transistor 49 – This is a part of a control circuit for the shift pulse to the W-register.

Transistor 51 – This is the control gate for the carrier memory of the W-register adder.

Transistors 52 and 53 – These are part of the flip-flop network used to control the W-register to L-register transfer.

Transistors 54 and 55 – These are part of a flip-flop network used to indicate number-to-log operation when OFF and log-to-number operation when ON.

Transistor 56 – This is a control for the memory of the negative log.

Transistors 57 and 58 – These are part of a flip-flop network used to control the memory signal of the negative log.

Transistors 59 and 60 – These are part of a control circuit for a reset signal generated by Transistors 67 and 68.

Transistors 61, 62, and 73 – These are drivers and controls for the master control flip-flop for log and anti-log processing.

Transistors 70 and 71 – These are the master control and flip-flop for log and anti-log processing.

Transistors 63, 64, and 76 – These are part of a flip-flop and control circuit for the carrier memory for the W-register adder.

Transistors 67 and 68 – These are part of a flip-flop network, set when the first number after a previous operation is entered into the LOCI.

Transistor 69 – This controls a signal used to reset the programmer.

Transistor 78 – This is a control which moves the decimal point to the right.

Transistor 79 – This is a control for the pulse used for resetting the W-register.

Transistor 81 – This is the reset control for the A-register.

Transistors 83 and 84 – These provide direct-current level control of the 9's complement circuit between the W-register and the W-register adder.

Transistor 85 – This provides control to blank the decimal lights.

Transistor 86 – This is part of the control circuit that moves the decimal point to the left.

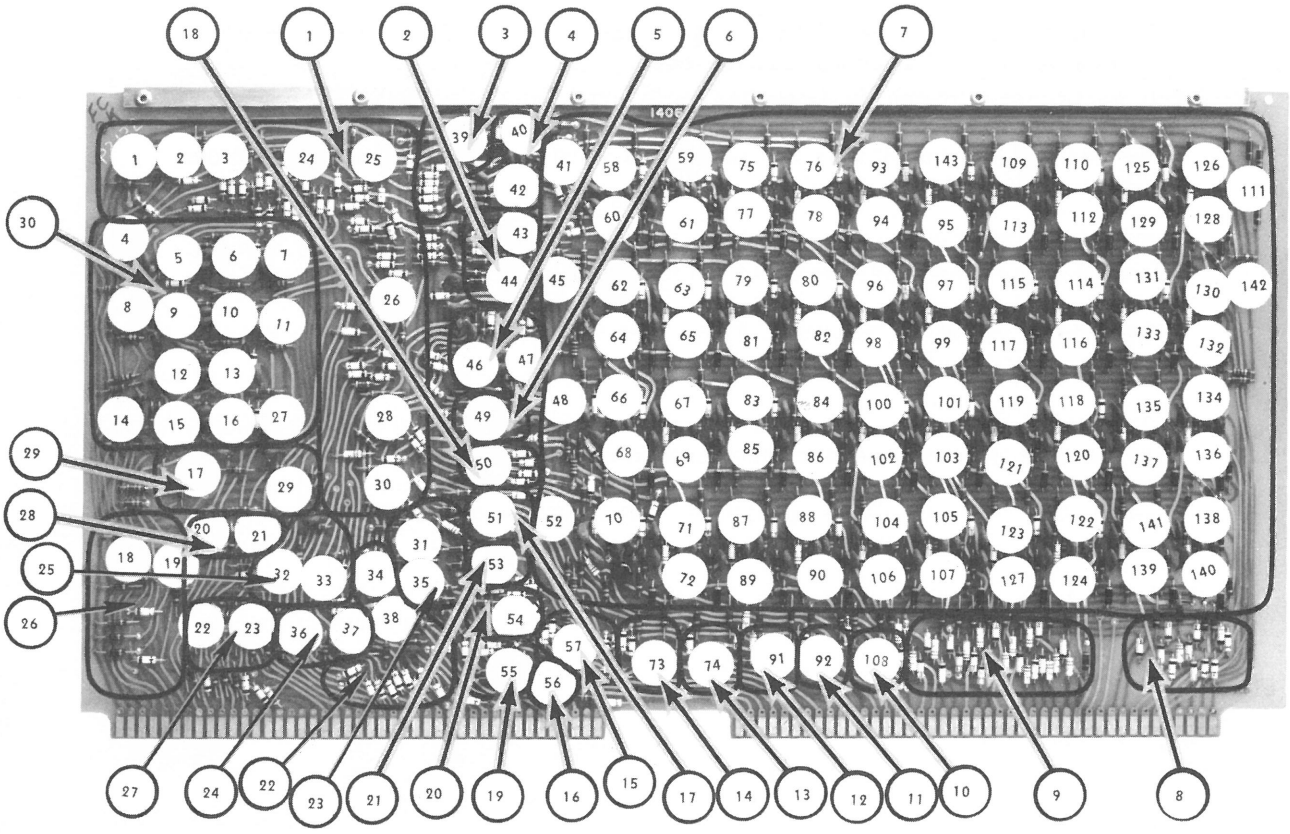
Transistors 72, 87, and 89 – These are part of the control circuit for the number-register reset and the decimal-counter reset.

Transistors 74, 75, 77, 80, 82, 90, 91, 92, 94, and 95 – These act as controls for various signals coming from the storage cards 1407A or 1410A, used to set the Work Register decimal counter.

Transistors 96 and 97 – These are used for the control of the entrance of numbers, control of log generation, and control of the adding and subtracting processes.

Transistors 93, 98, 99, and 100 – These form the control circuit for the number-register adder input.

Transistors 101 through 111 – These form the circuitry (including the flip-flops) of entrance of numbers, control of log generation, and control of the add and subtract processes.



1406A CARD

1. Circuit for the Accumulator decimal point counter. (DCN)
2. Control circuit for the A→W command. (ACD)

3 and 4. Control circuit for clearing leading insignificant digits in the accumulator Register. (ACS)

5. Control circuit indicating positive or negative number in the Accumulator Register. (ACN)
6. Circuit for one of the "S" signals.
7. Circuit that contains entry information of the Accumulator Register.
8. A Decoding circuit for the "S" signals.

10 through 15. Circuits for the "S" signals. (S18, 19, 21, 22, 28, 29, 31, 34, 36)

16. Driver circuits for the Accumulator Register signal. (ACR)

17 and 18. Same as #10.

19. A control circuit for the decimal point. (DCN)
20. Circuitry for the Accumulator Register Reset. (ARS)
21. Same as #10.
22. Same as #16.
23. One of the circuits of the sixteen step clock. (TD2)
24. Circuit that indicates the DCN is two or greater. (DCS)
25. Same as #20.
26. Accumulator decimal point circuits. (DCA)
27. Work Register decimal point circuits. (DCN)

28, 29. Same as #16.

30. Same as #26. (DCA)

1406A Card

This card contains the entire A-register, including 10 digits, a decimal point, and a sign. The card also has a comparator circuit used to align the floating decimal point during addition or subtraction, and it develops most of the control pulses in addition and subtraction processes.

The related schematic of the card indicates the location of some of the circuitry on the board. The right side of the card contains 80 transistors which form 40 flip-flop networks, and 6 transistors which are control drivers for the flip-flops. These 86 transistors and associated components form the binary storage circuits.

Across the bottom right-hand half of the card are six transistors which form six of the "S" signal circuits.

To the right of these are some of the decoding circuits for the binary storage. The upper left-hand portion of the card contains five transistors in a row. The first four, together with three down the left center, are part of the decimal-point counter circuit. The fifth is a part of the CAI signal circuit.

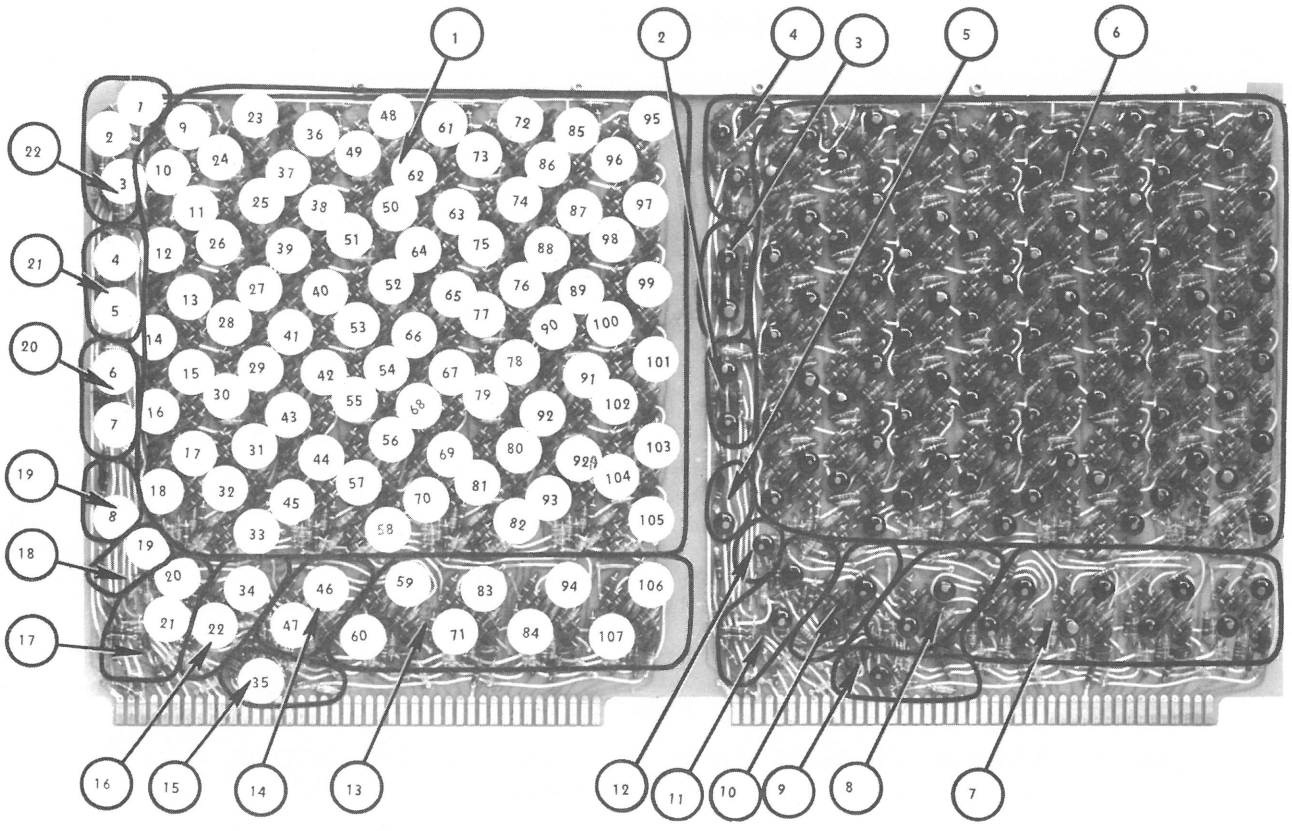
There is a group of seven transistors, of which three form part of the ACS signal circuit. Two are part of the ACD signal circuit, and two are used with the binary circuits.

The next two transistors under the ACD circuit form part of the A-register circuits.

Next are four transistors which form part of the "S" signal circuits.

Near the left-hand edge, in the center of the card, is a group of 14 transistors which form part of the DCA (Decimal Counter for the Accumulator) register circuitry.

There are 16 transistors positioned in the lower left-hand corner, five of which form part of the A-register circuit, two each for the DCA_0, DCN_0, DCS, TD2, and ARS signals, and one for the DCN signal.



1407A CARD

1. A complete storage register.
2. Control circuit for the store register. (CA1)
3. Circuit that indicates information is being transferred. (CP)
4. Shift pulse circuit for the ACR or N.R. signal.
5. Same as #2.
6. Same as #1.
7. Decimal point inputs (DCA or DCN) circuits.
8. Control circuit for the sign (ACN or SN).
9. Control circuit for one of the decoded sixteen step clock signals. (TD3)
10. Circuit indicating information is leaving the Decrement counter when it is on. (CA)
11. Same as #8.
12. Control circuit for the transfer of signals to or from the Program counter. (CP)
13. Same as #7.
14. Same as #8.
15. Same as #9.
16. Same as #10.
17. Same as #11.
18. Same as #12.
19. Same as #5.
20. Same as #2.
21. Same as #3.
22. Same as #4.

1407A Card

This card is used principally for storage. It has two complete transistor storage registers, each containing 10 digits, decimal point, and sign. The card also has four control circuits used by the programming features in the card.

The card is divided into two sections, with the circuitry identical in each section. The three flip-flop networks on each side are the only circuits not used for storage.

The three transistors located in the upper left-hand corner are part of the circuitry which provides a shift pulse for the A-register, or the number register. The two directly below these are part of a flip-flop network which is in the circuit that controls the information being transferred into, or out of, the program counter.

Continuing down the left-hand side, the next three are part of a flip-flop network and a driver in the circuitry which indicates that information is coming into the decrement counter, the program counter, or into storage.

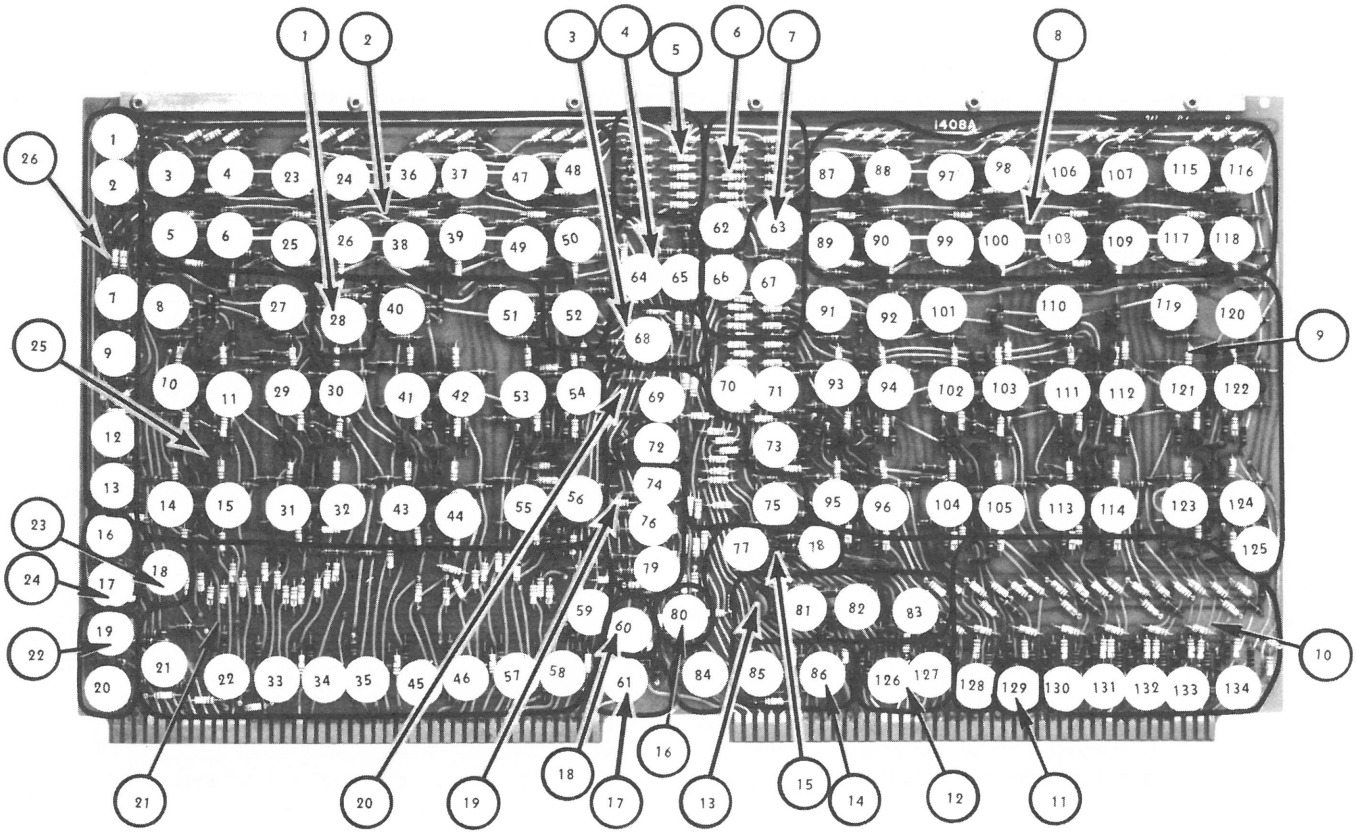
The two transistors in the lower left-hand corner are part of a control circuit for the sign. There are six flip-flop networks across the bottom of the card; the first in the circuitry indicating that information is going out of the decrement counter, or storage, when it is ON, and the next is part of the circuitry which indicates positive or negative numbers in the A-register.

Under this flip-flop, there is one control transistor for the decoding of the 16-step clock used in each cycle of operation.

The next four flip-flop networks are all part of the control of signals from storage to set the A-register, or the W-register.

There are 80 transistors making up 40 flip-flops for PC, PCS, DC, and DCS.

The circuitry on the right is the same except that the sixth and seventh transistors from the top and right-hand edge are part of a flip-flop which controls the signal for the store operation.



1408A CARD

1. Spare.
2. Program counter stepping circuit. (PCS)
3. Gate control of the number Register. (DCNS)
4. Stepping control circuit for the Program counter. (PCS)
5. Decoding circuit for the Program counter.
6. Circuit indicating Data is being received by the Decrement counter, Program counter or storage.
7. Part of #2.
8. Circuit that indicates DCN is greater than #2. (DCS)
9. Decrement counter circuits. (DC)
10. Control circuits for signals from the Keyboard. (LDET) (CRT) (NRT) (ACRT) (DCT)
11. Control circuit for the Decrement Counter. (DC)
12. Function set and reset.
13. Control circuit for Program code stepping if one of the six decision making tests is true. (PCP)
14. Pulse Generator circuit. (AFP)
15. Pulse Generator circuit. (triggered by the run Key) (RE)
16. Control signal circuit for the Program Counter.
17. One of the Decoding circuits for the sixteen step clock.
18. Stepping pulse of the Program counter.
19. Number Register shift pulse circuit. (NRSHIFT)
20. Circuit which indicates when information is being parallel shifted into or out of the Decrement counter. (CDC)
21. Control circuits for various signals coming from the Keyboard.
22. Circuit controlling the restore operation. (RST)
23. Spare.
24. Part of the Program counter stepping circuit. (PCS)
25. Circuitry of the Program counter.
26. Circuit controlling the stepping of the P.C. counter. (DCF)

1408A Card

This card is principally concerned with the 160-step program counter, the 100-step decrement counter, and their associated storages. The card also contains the decision-making circuits for looping and jumping.

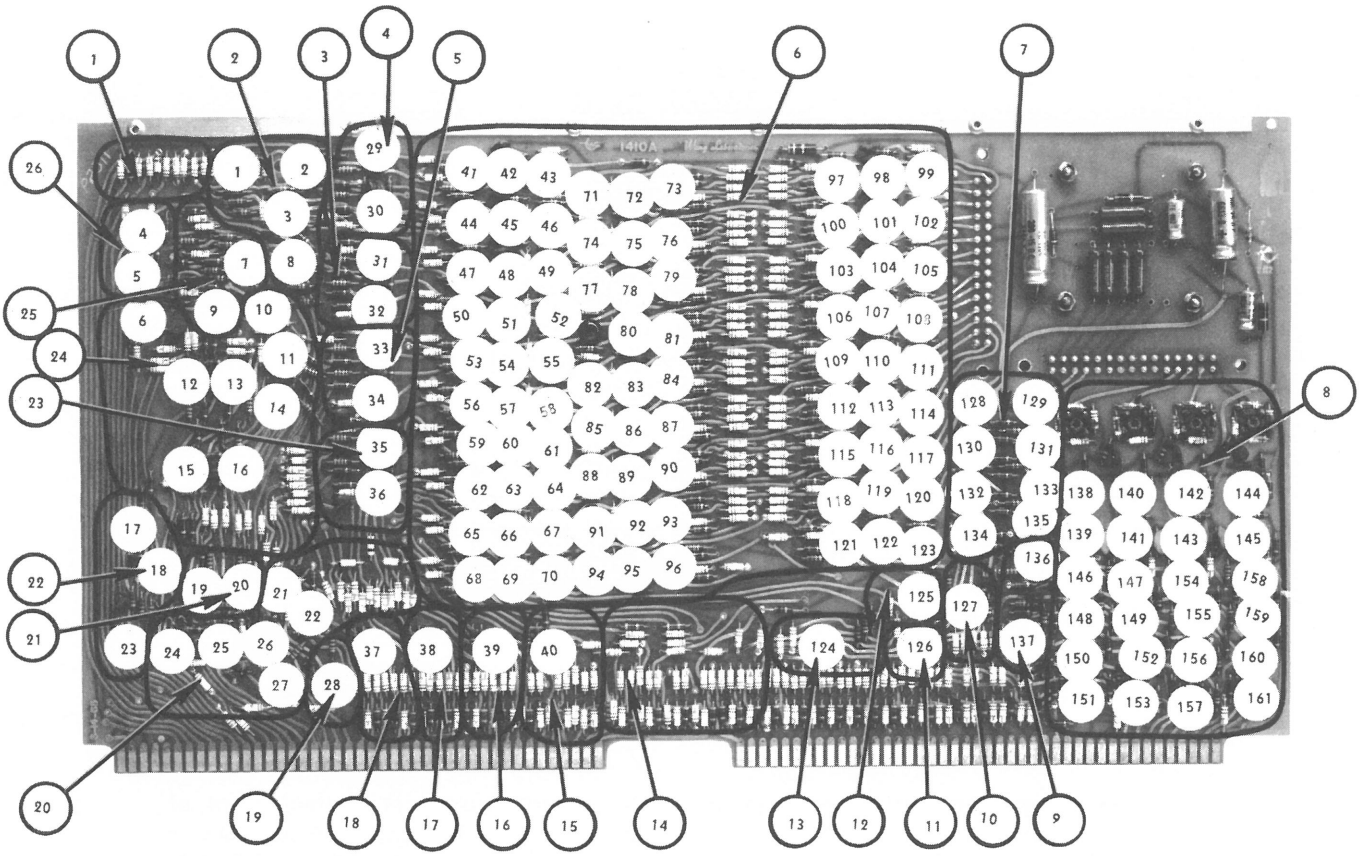
From the upper left-hand corner and coming down the side of the card, the first six transistors are part of the circuitry which includes a flip-flop to control the stepping of the program counter. The remaining two in this group are a flip-flop which is used to control the restore operation. Across the bottom left of the card are 10 transistors which are drivers for signals coming from the keyboard.

All other transistors, with the exception of two (which are spares), are part of the program counter, or program-counter storage circuits. In the center of the card are two transistors, of which one is the control indicating that information is flowing out of the decrement counter, or storage, when it is ON; and the other is for the gate control of the number register switch input from the decrement counter. Below this are three transistors which include a flip-flop network. This circuit is used to indicate that information is being parallel-shifted into, or out of, the decrement counter.

Continuing down the side of the card, the next three transistors are part of the circuitry which controls the W-register shift pulse. On the right-hand side are two transistors and these, together with one at the bottom of the card, control a delayed pulse generated by the RUN key.

In the lower right-hand corner, from right to left, there is a row of 11 transistors, of which the first five are control drivers for signals from the keyboard. The next one is part of the decrement-counter circuits; the next is a control driver for the signals coming from the keyboard. The next two are part of the function-reset circuits; and the last two are a control for the 30-microsecond pulse which gates on the input decoder.

Directly above this circuit, there are three transistors which control the program-counter stepping, if one of the six decision-making tests is true. The remainder of the transistors and circuitry are part of the decrement counter and the decrement-counter storage circuits.



1410A CARD

1. Output circuit for signals going to the 1501. (DCN)
2. Control circuit for the memory select counter. (T2)
3. Circuit for the $\overline{8}$ control of the core storage.
4. 5. Control circuit that selects the storage. (CS2, C33)
6. Components and circuitry of the memory core.
7. Memory core drivers circuits.
8. Circuits of the sensing amplifier.
9. Sensing amplifier gate reset circuit.
10. Set circuit for the positive or negative indication in the Accumulator Register. (ACN)
11. Control circuit for the signals from storage to set the Accumulator decimal counter. (DCA)
12. Control circuit for setting the memory of the sign of the Work Register. (SN)
13. Control circuit for signal from storage to set the Work Register decimal counter. (DCN)
14. DCN and DCA Decoding circuits.
15. Control circuit for the Work Register decimal counter. (DCN)
16. Control circuit for the Accumulator Register decimal counter. (DCA)
17. Control circuit for the Work Register counter. (NR)
18. Control circuit for the Accumulator Register counter.
19. Same as #17. (NR)
20. Control circuits for the store operations and indication information. (TD)
21. Control circuit for the decimal point in the Accumulator and Number Register.
22. Control circuit for one of the memory timing pulses. (T2)
23. Circuit $\overline{4}$ control of the core storage selection of the Decrement counter, Program counter or storage when on.
24. Circuit indication information going out or coming in to the Decrement counter, Program counter or storage when on. (CA1, CA)
25. Shift pulse circuit for the Accumulator and the Number Register.
26. Control circuit for the storage selection signals. (CS3, CS4, RS2)

1410A Card

This card consists of 16 complete core storage units. It also contains four control circuits which are used by the programming features of the 1408A card.

In the top center of the 1410A card are 83 transistors and associated components which make up the circuitry of the memory core.

In the lower right-hand section are 24 transistors and associated circuitry of the sensing amplifier.

To the left of the sensing amplifier, and to the right of the memory core, are 8 transistors which are the memory core drivers. Below these drivers are three transistors of which two are part of the circuit for the gate reset for the sensing amplifier. The remaining transistor is the set control for indicating positive or negative numbers in the A-register.

To the left of the set control for the sign memory of the W-register are two transistors which control signals from the storages to set the accumulator decimal counter.

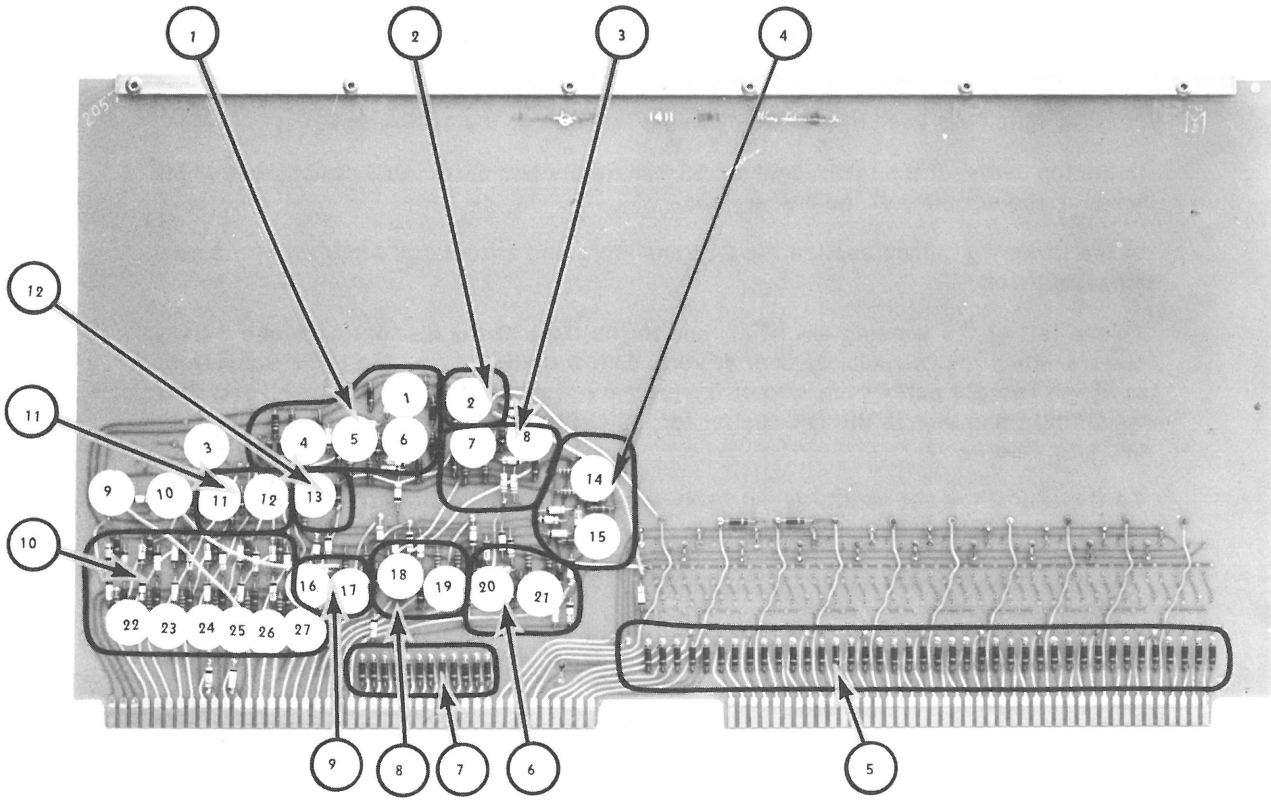
The next four transistors along the bottom of the card are control gates for the A-register and number register.

The next one to the left is a control driver for the combined switch inputs to the W-register.

To the left of the memory core circuits are four flip-flop networks which are core storage selection networks.

In the top left center and the lower left corner are four and three transistors, respectively, which are in the circuitry that controls one of two main timing pulses. To the left of these are eight transistors which are part of the control circuits for the following signals: data coming into the card to indicate that information is being transferred into, or out of, the program counter; and the signal which controls the store operation.

Directly above these eight transistors are eight more which include three flip-flop networks forming part of the control circuits for the signal for the master control flip-flop of the 16 storage registers; and a second signal for the flip-flop indicating information is coming into the decrement counter, program counter, or storage. The third signal is a flip-flop indicating that information is going out of the decrement counter, or storage, when it is ON. Directly above these are two transistors which are control drivers for the A-register shift pulse and the number-register shift pulse.



1411A CARD

1. Pulse generator control circuit used for reset. (RXP)
2. Control circuit for an Interrupt Pulse from an external source. (INT)
3. Control circuit for control of the input multiplexier. (MMC)
4. Control circuit for a pulse generated by the write key.
5. Load Register for various signals of the Number Register.
6. Control circuit for a pulse generated by the carriage return key. (PCB)
7. Same as #5.
8. Control circuit for a pulse generated to set the channel of the output multiplexier. (QMS)
9. Control circuit for a pulse generated to set the channel of the input multiplexier. (IMS)
10. Circuit for the operation code input signal.
11. Strobo pulse circuits.
12. Same as #1. (RXP)

1411A Card

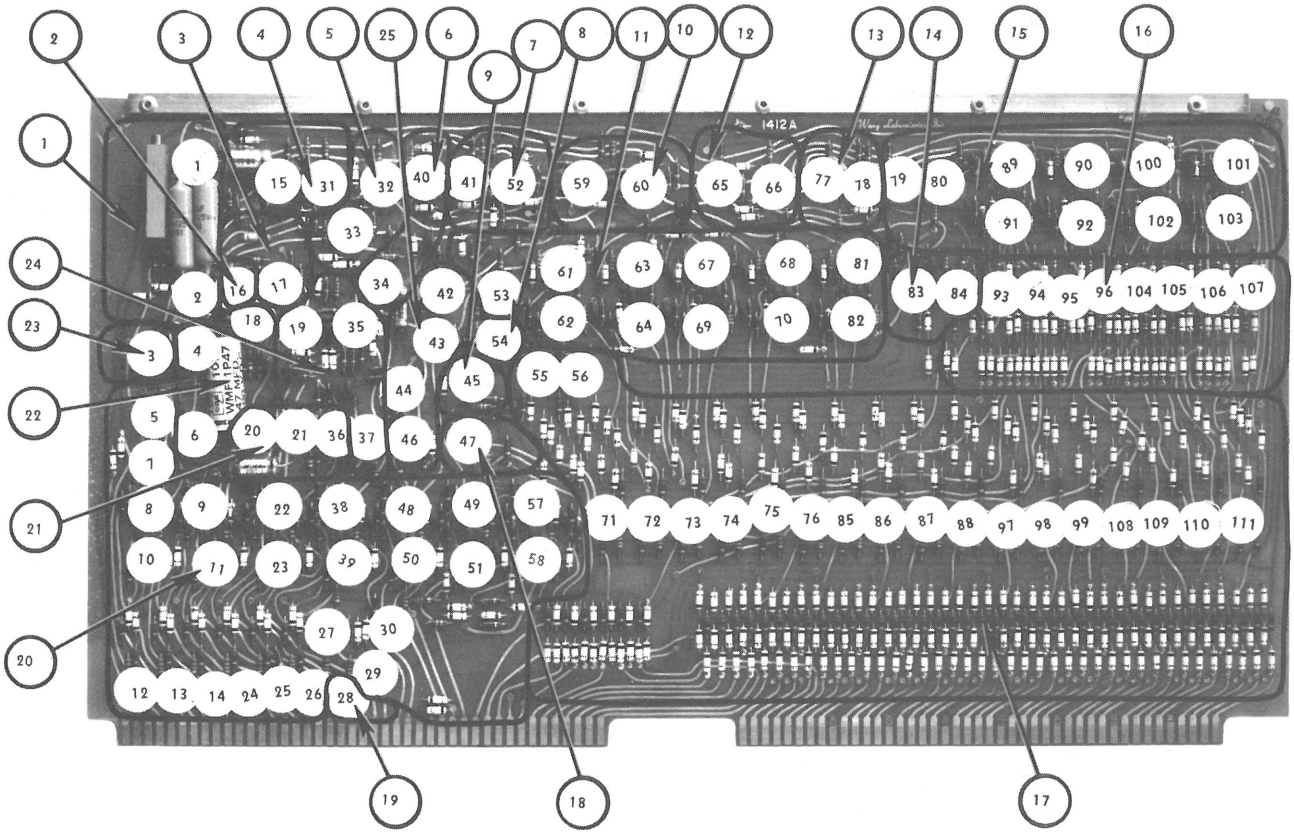
The 1411A card has all of the circuits concerned with the input-output interface. It has the least amount of circuitry of any of the cards and is used as an optional equipment card in the regular LOCI.

The circuitry is confined to the lower portion. Across the lower left-hand side are current-controlling circuits for the signals from the 1401A card.

In the lower right-hand corner are six transistors which control the signals coming from some of the peripheral equipment and going to the operation-code, flip-flop networks on the 1501 card.

Continuing across the bottom are eight transistors which are grouped two to a circuit. One circuit, commanded from the 1501 card, is used as a control pulse for the output multiplier. The other three are controls for the signals to the printer which is part of the optional equipment. It is, in fact, a pulse generator which is connected only when a Beckman-type printer is used.

The remaining transistors, which are in the upper left section of the circuitry, are control circuits for the input multiplier.



1412A CARD

1. Control circuitry for the Teletype card. (TMC)
2. Circuit for the read start control of the Teletype. (RDS)
3. Controlling operations of the Reader in the Teletype.
4. Oscillator circuit for the Teletype card. (OSC)
5. Circuit that controls the number of digits to be printed out, signal coming from the Teletype digit control switch. (NDP)
6. Control circuit for the pulse generated by the write key and the carriage return. (CR)
7. Master control circuit, circuit for the Teletype card. (TIME)
8, 9. Control circuit for the signal generated by the carriage return key. (PCB)
10. Print memory control circuit. (PMC)
11. Circuit for the Program stepper. (PS)
12. Control circuit for sign and decimal point in the printout. (PSN)
13. Control circuit for one of the Teletype stepping pulses. (TSD11)
14. Same as #13. (TSD9)
15. Same as #13. (TS)
16, 17. Circuit for the decoded output of the counter that selects digits to be serialized by the Teletype card. (PSD, PSN, PSD'S 0-13)
18. Control circuit for the pulse generated by the Write key. (PCA)
19. Control circuit for the Reader start control of the Teletype. (RDS)
20. Control circuit for the operation code input.
21, 22, 23. Pulse generator circuits. (100MS) (3MS)
24. Controlling operations of the READER in the Teletype. (RF)
25. Same as #2. (30MS)

1412A Card

The 1412A card contains all necessary circuits to transmit data and to receive instructions from a Teletype Model 33ASR. This card is a special option card.

The lower right-hand half of the card contains the circuitry for the 18 transistors controlling the decoded output of the counter, which selects the digit to be serialized by the Teletype card.

Above these, on the right-hand side, are eight transistors and associated circuitry of the control circuits for the decoded output which selects the digits to be serialized by the Teletype card.

In the upper right corner are eight transistors which are part of four flip-flop networks. These networks are all part of the Teletype switching circuitry.

To the left of the switching circuit are two transistors which are control drivers for the Teletype switch decoding circuit. There are two transistors to the left of this circuit for controlling the number in the program stepper.

To the left is a flip-flop network which is part of the print-memory control circuit. To the left and below the print memory are 11 transistors which include five flip-flops which are part of the circuitry that controls the program stepper.

On the lower left-hand side, the bottom transistor is for the Reader START control of the Teletype.

The 25 transistors located on the lower left-hand side of the card are part of the program code-control signals. This circuitry has seven flip-flop networks.

Above these seven networks are 12 transistors which form part of three pulse generator circuits. To the right of these are three transistors, of which two are for the control of the pulses generated by the Write key, and the other is for control of the pulses generated by the Carriage Return key.

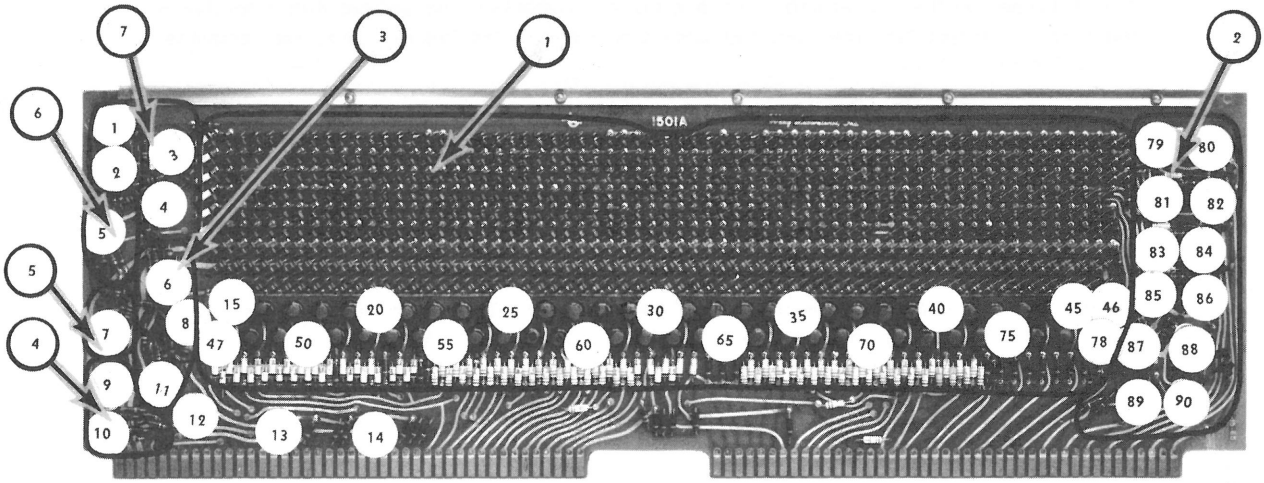
The three transistors above the pulse-generating circuitry, which include a flip-flop network, are for control of the Reader in the Teletype.

The upper left-hand corner has the circuitry for the control of the master control flip-flop in the Teletype card.

To the right, across the top, are the flip-flops for the oscillator 9.09 milliseconds for the Teletype card. Directly under this oscillator circuit is the circuit for the Reader START control of the Teletype.

To the right are the two transistors which control the number of digits to be printed out, the signal for which comes from the Teletype digit-control switch.

Continuing to the right are two transistors which are drivers for a signal controlled by a signal from the program memory control, and which is going to the Teletype.



1501A CARD

1. Input decoder circuit.
2. Circuit for the control of signals from the Reader output.
3. Pulse generator circuit that gates on the input decoder. (AFP)
4. Prime signal from the Keyboard. (LAMP)
5. Function reset circuits.
6. Function pulse circuits.
7. Function set circuits.

1501A Card

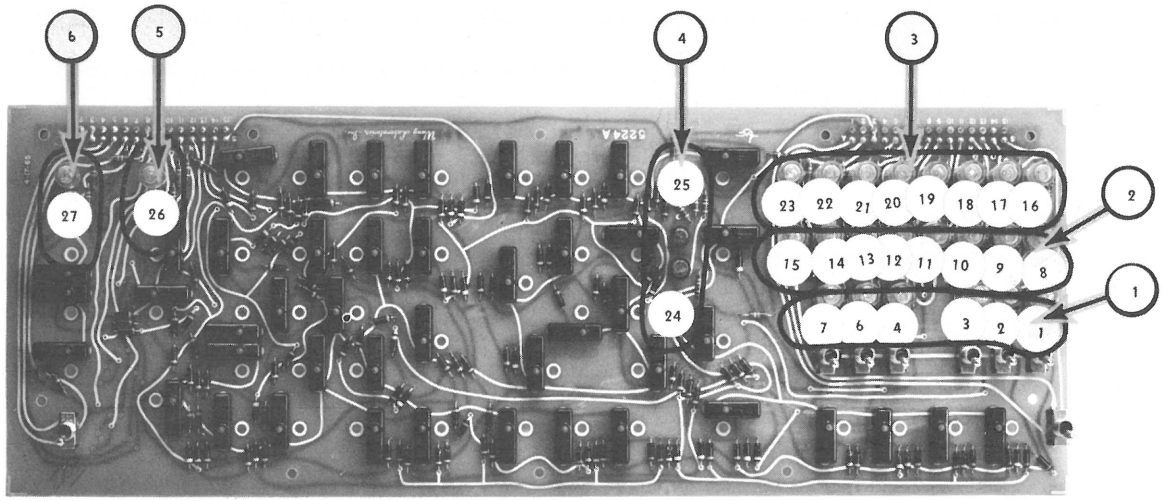
This card is the means of communication between certain external sources (such as the Keyboard, Card Reader, or Teletype) and the arithmetic processing and storage unit.

The card receives a six-bit octal code; it also has the storage facilities of the octal code, and it decodes this information and distributes it to the proper data and control points in the LOCI to initiate the indicated operation. A decoded electrical signal is generated for each operation. This card also receives the prime machine pulse from the keyboard, and the function controls, resets, and various decoder signals.

On the right-hand edge of the card are six flip-flops to receive the octal operation code from the card reader.

Across the center of the card is the input decoder circuit. On the top left are six transistors which are part of the control circuit for the functions Set and Reset.

The two transistors in the lower left-hand corner control the prime signal from the keyboard. To the right of these are three transistors which are part of the 30-microsecond pulse circuit for gating on the input decoder.



5224A CARD

1. Operation code indicator circuit.
2. Program code indicator circuit. (PC1, PC2, PC4, PC8, PC10, PC20, PC40, PC80)
3. Decrement counter indicator circuit. (DC1, DC2, DC4, DC8, DC10, DC20, DC40, DC80)
4. Memory select indicator circuit. (CS1, CS0)
5. Response indicator circuit.
6. Error indicator circuit. (err)

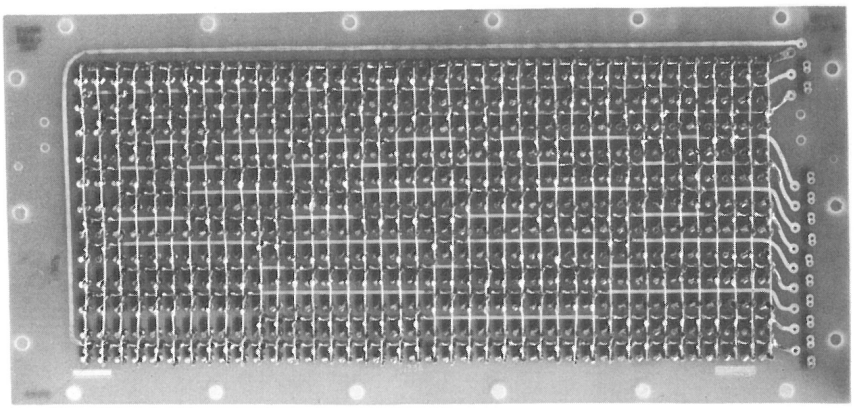
5224A Card

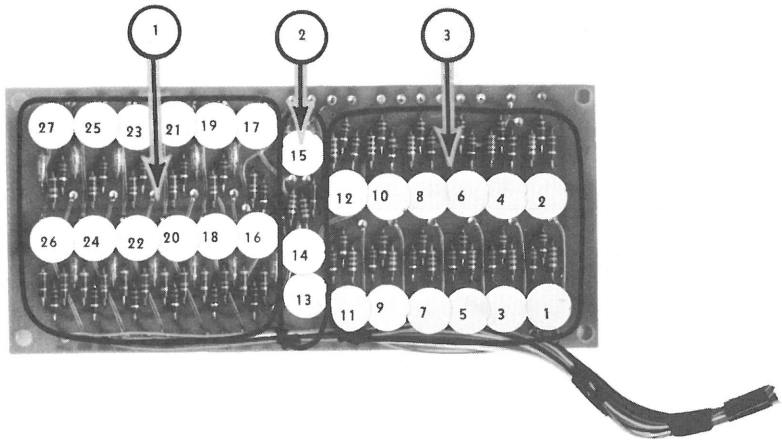
This is the keyboard card. It has all of the indicator lamps, and performs all manual operations.

The 46 microswitches located throughout this card set the operation code flip-flops on the 1501 card by pulling through the proper diodes. The eight toggle switches perform basically the same functions as the microswitches.

There are 26 indicator lamps, and each has a transistor which acts as a driver. The break-down of indicators and drivers is as follows:

8 – Decrement counter
8 – Program counter
6 – Program code
2 – Memory select
1 – Response signal
1 – Error signal





5123A & 5129A CARDS

1. Output circuitry.
2. Control drivers for the output of the Reader.
3. Input circuitry.

5123A, 5129A Cards

These two cards contain all of the electronic circuitry of the card reader. The card reader controls various signals used in the operation-code circuitry.

Looking at the 5129A card with the attached wires at the top right are two rows of six transistors each. These are drivers for the signals leaving the card reader. In the center of the card are three transistors: two are for the control of the output drivers; the third is a gate control for a second card reader output.

On the left of the card are two rows of six transistors each. These, and their associated components, are the control drivers for the signals coming into the card reader.

The 5123A card contains resistors and diodes only. These are used to control the signals passing through the program card.

IV. LOCI CU-3/CU-4 CIRCUIT DESCRIPTION

A. OUTPUT MULTIPLEX (Drawing 5485-10)

The output multiplex circuit accepts parallel output data from the LOCI W-register and distributes it to one of the three output channels. This circuit consists of an output multiplex (OM) switch, a buffer storage register, and assorted control circuits.

The three outputs of the OM switch (CD22) are designated OM_0 for tape leader, OM_1 for the format register, and OM_2 for the teletype. The switch is loaded by execution of LOCI Command 35, provided the sign of W is negative. This causes a negative level (M_Z) at J2, Pin 48, which acts through Gate D17 and pulse Generators D18 to Reset CD22 first, after which the channel number is set in by transferring the most significant digit of W into CD22 by acting through gated Drivers D21. Outputs of the OM switch control distribution of Write commands to the appropriate channel by acting on Gates D23.

Execution of Command 35, with W positive, acts on pulse Generators D19F to prime the CU-3.

Execution of LOCI Write and CR commands act through Gates D17 and pulse Generators D19 and D20 to generate control pulses for the teletype interface and timing circuits. Flip-Flop D-16 inhibits further outputs from the LOCI until typing is complete. LOCI output commands are acknowledged at J2, Pin 49 through diode Gates C24.

The output storage buffer is a serial shift register loaded in parallel from the LOCI upon receipt of a Write command. Shift register modules are AB22, AB24, CD27. Loading is through gated Drivers A23, B23, A25, B25, A27, C26, and D26. Following each Write operation, the shift register is cleared by a burst of clock pulses acting through gated pulse Generator D25 and Inverters C6M and D15S.

B. FORMAT LOGIC (Drawing 5485-11)

The format logic circuit controls the transfer of data from the output buffer-shift register to the teletype unit.

The format register is a three-digit storage register containing the control word governing output format. This register, consisting of Modules AB20 and BC15, is loaded from the four most significant digits of W by execution of a Write command, provided that the OM has been set to OM_1.

Prior to each typing operation, the contents of AB20, which correspond to the desired number of characters before the decimal point, are transferred into binary Counters B18 by Pulse SFC acting on gated Drivers B19. Simultaneously, the decimal point locator digit from J2 Pins 41, 42, 43, and 44 is loaded into Counters B17 through A17. Each of these counters had previously been reset by the Transfer pulse acting through A15H.

The actual writing sequence begins with the appearance of $\overline{AFT}$ pulses at A16KM. These pulses cause B17 and B18 to count up from their preset values. When B17 reaches a count of 10, it acts through B16NM, A16S, and A15K to prevent further counting, and through A16P and C19E to enable shift pulses for the storage-shift register. Simi-

larly, when B18 reaches 10 it stops counting and acts on Flip-Flop C20M and pulse Generator C14P to produce the Start Write Data pulse. Either B17 or B18 may be first to reach 10, depending on the format control word.

The occurrence of the decimal point in the writing sequence, as determined by the format timing circuit (Drawing 5485-12) causes the EDR pulse, which acts on Flip-Flop C20JE, to enable $\overline{AFT}$ pulses at A18K through C19N and C18K. This counter, which was previously reset by the Transfer pulse, then counts up until it equals the digit in Register AB20, which equals the number of desired characters after the decimal point. Comparison is accomplished by A19. Coincidence acts through C12E and C13F to produce the End Data pulse at C13H.

Counter C17 keeps track of the number of words per line. It is compared to the reference digit by C16. Coincidence acts through C18E to provide automatic carriage return.

C. FORMAT TIMING (Drawing 5485-12)

The format timing circuit controls the sequencing of sign, data, and decimal-point information to the Teletype unit. It also provides for insertion of Run and ± codes on the output tape, as well as the automatic carriage-return and line-feed commands.

Receipt of the Type signal from the output multiplex circuit acts on Flip-Flop D3EJ to enable D25J and allow clock pulses at D25K to appear at D2H. These pass through to D6P, causing high speed $\overline{AFT}$ pulses at D6R. Occurrence of the Start Write Data pulse at P24R acts on Flip-Flop D3 to disable D25J and enable D25N. This causes all subsequent $\overline{AFT}$ pulses to be derived from, and thus synchronized to, the teletype loop clock through D1H and D25N.

The Start Write Data pulse also acts through D5C to advance the format timing Generator CD11 to FT1. During FT1 time, the data sign is fed to the teletype unit. Upon completion of sign printout, format time is advanced to FT2 by the T-step pulse from D1 acting through D9S. FT2 time covers printout of all data characters which occur before the decimal point. The decimal point is printed during FT3 time, with the transition from FT2 to FT3 being initiated by the DPT pulse from C13M acting on D9K. The DPT pulse always occurs on the 12th $\overline{AFT}$ pulse, as determined by Counter D4. Transition from FT3 to FT4 is caused by the T-step pulse at D9J.

On the 13th $\overline{AFT}$ pulse, Signal EDR is generated at D6H and fed to the format logic (Drawing 5485-11) to initiate counting of characters after the decimal point.

The End Data pulse from format logic acts on Flip-Flop D8EH to enable $\overline{AFT}$ pulses to pass directly to the FT counter. This causes advancement to Steps FT5, FT6, and FT7. During FT5 time, a space is generated if W is positive, while a "±" code is generated if W is negative. During FT6, a run code is generated, and during FT7 a space is generated. Completion of Step FT7 acts through D25S to reset Flip-Flop D8H and terminate the printing sequence. Return of Flip-Flop D8 to the reset state acts on pulse Generator D6L to provide assorted reset pulses.

In the event that the word just completed was the last word of a line, the auto CR signal acts through D7K to block the reset pulse at D25P, and the format generator continues through Steps FT8 and FT9 and back to FT0 where the Flip-Flop D8 is

then reset by FT0 acting through D7H. During FT8 and FT9, the carriage-return and line-feed operations are carried out.

Execution of the LOCI CR command (Code 75) acts directly through D7E to set format time to FT8 and to set Flip-Flop D8. Again, the format generator counts through to FT8 and FT9 and back to FT0 where it stops, as before.

Flip-Flop D12 stores the sign of W. Gates D8 enable either plus (+) or minus (-) printout during FT1 time.

D. TELETYPE INTERFACE (Drawing 5485-13)

This circuit provides synchronizing pulses for the transfer of data to and from the teletype unit, and provides other teletype drive and control functions.

Information to and from the teletype unit is transmitted in the form of current through a closed loop. Each teletype character is transmitted serially by bit, where a closed-loop or current-flow condition is referred to a "mark", or Binary 1, and an open-loop, or no-current condition, is referred to as a "space", or Binary 0. Each character transmission is evenly divided into 11 units of time, where one unit is ideally 9.09 milliseconds. Of each character train, the first time unit is always occupied by a "space" and the last two are always "marks". The remaining eight units of time describe the transmitted character in standard ASCII code.

Due to the nature of the data transmission scheme, it is important that the sending device and the receiving device operate synchronously. This is accomplished by using an adjustable Clock A8, which is trimmed to oscillate with a period of 9.09 milliseconds. The clock is normally clamped in a non-oscillating state by Drivers C9S. Receipt of the Start Write Data pulse at C7E sets Flip-Flop C7EJ and relieves the clamped condition of A8. Oscillations at A8S begin immediately and always begin with a positive transition. These clock pulses are fed to Counter B8, which drives decimal Decoder AB9. In turn, AB9 produces 11 uniformly spaced timing pulses (X1 through X11), which are used to gate-code bits out to the teletype unit by acting on diode Gates A10, B10. Gate outputs act on Driver C9H to operate Relay A7D, which drives loop Contacts A7JK. Transmission is terminated by a stop signal at C7M, which enables a reset pulse from B7S at time X11.

Transmission of data from the Teletype unit back to the CU-3 unit is synchronized in similar fashion.

The leading space of the transmitted character acts on pulse Generator B7K through reading Contacts A7NP to produce a Start Clock pulse at B7J. The character is then shifted serially by bit into Register AB6 under control of synchronous clock pulses at AB6A. The stored character is then strobed in parallel to the LOCI by the C_X pulse, J3 Pin 9.

Flip-Flop C6EJ controls the teletype reader through Relay K1. Relay Contacts A7SR are used to inhibit typing during the reading of data and program from punched tape.

Tape reading is controlled by A_X pulses acting through C18M, C12R, C8E, and C19S.

E. CODE MATRIX (Drawing 5485-13A)

The code matrix generates ASCII codes in response to commands from format timing circuits. Control pulses act on Drivers A12, A13, and A15 to enable appropriate code patterns. Serial BCD data from the output multiplex shift register is gated through A11 under control of FT2 and FT4 pulses acting through C7 and C12. Flip-Flop D12 serves to suppress leading zeros.

Code matrix outputs are fed through Drivers B11 and B12 to the code serializer switches A10 and B10 of Drawing 5485-13.

F. READER CONTROL (Drawing 5485-14)

The reader control circuit performs the decoding functions essential to provide the three modes of reader operation described earlier.

Decoder Matrices AB4 (Drawing 13A) and AB5 (Drawing 14) detect specific code combinations by sampling the contents of the readout shift register (AB6,-13) at time X9*. Three of these critical codes are the flag codes, S_0, S_1, and S_2, which signal a change of reading mode. These codes act through Inverters C5 to set Mode Flip-Flops B2 and B3. Other decoding combinations distinguish between data and non-data, and detect specific code combinations for Space, Stop, S_3, and S_6.

Reception of a Space code causes the reader to advance automatically, thus providing for automatic skipping of blank tape. A detected Stop code acts through C3S and B11P to inhibit further reading by clamping off the LOCI Read (R_X) signal. Detection of S_3 or S_6 acts through Circuits D1, C1, D14, and B1 (Drawing 13A) to re-create the $\pm$ or Run codes, which they represent, before strobing to the LOCI.

Diode Gates C2 act on the above-mentioned control signals to direct reading or skipping of the punched tape, according to operating mode. Strobe pulses are developed at X9** time through C2D, C8P, C6R, and B7P.

The step-run switch provides single-step reader operation by clamping off the LOCI R_X signal following each strobe pulse.

V. PACKING AND SHIPPING

A. PACKING

The LOCI, or any part of it (e.g., printed circuit cards, etc.) shall be packed in a manner to insure against damage during transportation. Recommended packing procedure for the LOCI circuit cards follows:

1) Wrap individually.
2) Protect individually with foam rubber, crushed paper, or some other suitable material.
3) Double box – the boxes being at least of sturdy, corrugated cardboard and of a size to permit minimum movement of the cards.
4) The outer box shall be separated from the inner box by a shock-absorbing material.

The LOCI machine shall be packed in the same manner.

B. SHIPPING

The LOCI, or any part thereof, shall be shipped under the direction and control of the head shipper, unless arrangement has been made to the contrary, at the time of the sale, with Wang Laboratories, Inc.

VI. PROBLEMS

This section outlines some of the malfunctions and the possible procedures of isolating the malfunction. Although this information does not go into great detail, it will provide a method of solution and, in many cases, solve the problem. This manual is not intended to lead the repairman to the exact component that has failed, but to the circuitry in which the failure occured. Listed are some of the most common malfunctions, followed by a list of cards. The cards are listed in the order in which they should be checked for the malfunction.

Important Note

When a Malfunction becomes apparent, any indication on the response indicator will enable the repairman to go to the first card on the list after the particular malfunction. If the response indicator does not light, Cards 1501A and 5224A should be checked first.

The problem matrix follows:

Description of Malfunction	1st card to check	2nd card to check	3rd card to check
1) Error indicator on. Press CL error and nothing happens.	1403	1501	
2) Cannot CL A (clear Accumulator Register) But CL W (clear Work Register) is working properly.	1406	1405	
3) Cannot Prime (clear the Log Register)	1403	1405	
4) Cannot CL W (clear the Work Register) But the CL A (clear the Accumulator Register) works properly.	1402	1405	
5) Cannot key in decimal point.	1401	1405	
6) Cannot enter any digits 0-9	1405	1402	
7) When entering 2nd digit this operation destroys the first digit.	1402	1405	
8) Cannot change the sign.	1401	1405	1403
9) Response light on continuously.	1401	1405	1501
10) Commands W→A and A→W will not work ("0" are indicated).	1406	1405	
11) Commands W→L and L→W will not work ("0" are indicated).	1403	1405	
12) Cannot Subtract. But addition command works.	1406	1405	1402
13) Cannot add. But subtraction command works.	1406	1405	
14) Will not add or subtract some digits.	1406		
15) S_0 is faulty Wang results.	1410/1407	1406	1405

Description of Malfunction	1st card to check	2nd card to check	3rd card to check
16) Commands $W-S_1$ S_1-W are	1410/1407		
Commands $W-S_2$ S_2-W faulty	1410/1407		
Commands $W-S_3$ S_3-W Wang results	1410/1407		
17) Memory select. Operative in some modes, but not all the light indicates correct position.	1410		
18) Memory select light doesn't indicate.	1501	1410	5224
19) Log of number incorrect. Commands given [Key In] [X] [L→W]	1403	1404	1405
20) Anti-log incorrect. But log is correct.	1405	1402	1401
21) Commands squares	1404		
square root	1404		
one over the square	1404		
and one over the square root will not work.	1404		
22) PC and DC inoperative	1408		
23) P0, 1,2,3 inoperative	1408		

VII. CONCLUSION

The disclosure herein, as well as any other drawings or descriptions which may sometimes be furnished by Wang Laboratories, Inc., are to be used only for repair and maintenance.

No permission or rights to manufacture the equipment — in whole or in part — is granted or implied.

APPENDIX

Signal Source and Disposition

SIGNAL	SOURCE	CONTROL OR FUNCTION
ACD	1406	Control flip-flop for A→W
ACDP	1406	Reset W-register for A→W
ACN	1406	Control flip-flop indicating positive or negative number in A-register.
ACRO	1406	DC level negative indicates "0" in A-register.
ACS	1406	Control flip-flop for clearing leading insignificant digits in A-register.
$\overline{\text{ACT}}$	1501	Pulse to test if A-register equals zero.
AD	1405	Control flip-flop for aligning decimal point between A-register and W-register.
AFP	1501	30-microsecond pulse that gates on input decoder.
All process	1405	Negative direct-current signal during any function, except for entrance of numbers, that requires the clock to be turned on.
ARS	1405	A-register reset.
ASR	–	Direct-current level indicating that W-register is being 9's complimented between W-register and adder.
BS	1405	Control flip-flop for back space.
BSP	1501	Pulse to turn on BS.
C1	1405	Carrier memory for W-register adder.
C2	1403	Carrier memory for L-register adder.
CA	1407 or 1410	Flip-flop indicating information is going out of decrement counter or storage when on.
CAI	1407 or 1410	Flip-flop indicating information is coming in to the decrement counter, program counter, or storage.
CC	1402	When doing anti-log if flip-flop is off, it indicates that W-register is above .9999999999.
CDC	1408	Flip-flop indicates when information is being parallel-shifted into or out of the decrement counter.
Clock Control	1405	Indicates that clock is on.
CPC	1407 or 1410	Indicates that information is being transferred into or out of the program counter.
$\overline{\text{CP0}}$	1501	Selects storage #1
$\overline{\text{CP1}}$	1501	Selects storage #2
$\overline{\text{CP2}}$	1501	Selects storage #3
$\overline{\text{CP3}}$	1501	Selects storage #4
CSP	1501	Changes sign of W-register (SN).

SIGNAL	SOURCE	CONTROL OR FUNCTION
$\overline{CS0}$	1410	$\overline{4}$ flip-flop of core storage selection.
$\overline{CS1}$	1410	$\overline{8}$ flip-flop of core storage selection.
CPCS	1408	Controls shifting of decrement and program storages.
Channel In 0-5	Input Mult.	Input code to input multiplexer.
DCA0	1406	Indicates that accumulator decimal counter equals zero.
DCA set gates	1407 or 1410	Signals from storages to set accumulator decimal counter.
DCN0	1406	Indicates that W-register decimal counter equals zero.
DCN10	1406	Indicates that W-register decimal counter equals 10.
DCNS	1408	Gate control of NR switch input from decrement counter.
DCN set gate	1407 or 1410	Signals from storages to set W-register decimal counter.
DCN decoder ± common	1405	Control to blank decimal lights.
$\overline{DCP}$	1501	Decrement counter stepping pulse.
DCS	1406	Signal that indicates DCN is 2, or greater.
$\overline{DCT}$	1501	Signal to test if decrement counter equals zero.
DM	1405	Memory for negative log.
DP	1405	Flip-flop memory for entering decimal point.
$\overline{EC1}$	1501	Pulse to clear error flip-flop.
EN	1405	Flip-flop for entrance of numbers, control of log generation, and control of add and subtract processes.
ENT	1405	Main gate control flip-flop for entrance of numbers.
ERR	1403	Error flip-flop.
ER0	1401	Indicates zero in ER counter. Also used to reset ER counter.
ER counter	1401	BCD counter used for memory of which number is to be entered. Also used in the processing of a number to log or log to number.
FM	1405	Moves decimal point left.
FP	1405	Moves decimal point right.
Function Pulse	1404	DC gate indicating an operation is within the machine.
Function Reset	1501	A 30-microsecond pulse, initiated by the lagging edge at the function pulse, that resets the input flip-flop.
Function Set	1408	A 50-microsecond pulse, initiated by the lagging edge at the function reset pulse, that sets the input flip-flop.
$\overline{IMS}$	1501	Input multiplexer set channel pulse.
INT	1411	Interrupt pulse from external source.
KC	1405	Clock control flip-flop.

SIGNAL	SOURCE	CONTROL OR FUNCTION
KB common	1404	Common positive 2-volt direct-current signal applied to the keyboard keys.
KLC	1404	DC level signal indicating clock on when negative.
K2	1404	Second stage of clock counter.
$\overline{\text{LDET}}$	1501	Test pulse for testing error.
LANP	1501	Pulse generated for complete LOCI reset by keyboard prime.
LD	1405	Flip-flop controlling W-register to L-register transfer.
LDE	1403	Flip-flop that serves as a blocking signal when error is accumulated.
LN	1405	Flip-flop indicating number to log operation when OFF and log to number when ON.
LPS	1404	Normally zero pulse that step LP counter.
LR 1, 2, 4, 8, $\overline{1}$, $\overline{2}$, $\overline{4}$, $\overline{8}$	1403	Last stage output of L-register.
LR 9's Comp.	1404	DC level controlling LR's 9's complement circuits.
$\overline{\text{LRS}}$	1501	Main reset of log register.
LP1	1404	First stage of LP counter.
LP Counter	1404	Counter controlling steps of log processing.
LR sw. in	1403	Combined points of switch input to log register.
LR0	1403	DC level indicating zero in log register.
LSN	1403	Flip-flop memory of number sign of the log register.
LT	1405	Flip-flop controlling transfer of L-register to W-register.
LTP	1405	20 to 30 microsecond pulse generated by LT being turned on.
$\overline{\text{LRT}}$	1501	Test pulse for testing for negative log.
MCS	1410	Master control flip-flop of the 16 storage registers.
ML	1403	DC level indicating a positive or a negative log.
MMC	1411	DC level for master control of the input multiplexer.
Mode switch (Manual)	1408	Position of mode switch allowing use of code control switches when the key is operated.
Mode switch (One Step)	1408	Position of mode switch allowing one operation of the card reader for each time the run key is operated.
MPC	1411	DC level control telling the input multiplexer the LOCI is ready for further information.
MS	1403	DC level indicating that number is greater than .9999999999 at the end of an anti-log operation.

SIGNAL	SOURCE	CONTROL OR FUNCTION
MSP	1403	Pulse controlled by MS that shifts a number 1 into the W-register at the end of an anti-log operation if the number is greater than .9999999999.
MSC	1411	A pulse generated by the external input multiplexer indicating that the proper channel has been selected.
$\overline{\text{MIP}}$	1501	Pulse generated by the MS key that steps CS0 and CS1.
MTP	1411	Pulse that sets the channel of the output multiplexer.
NB	1405	Flip-flop used to put zeros into the input of the W-register adder during the log operations.
NLP signals	1404	Decoded output of LP.
NDP	1412	Number of digits to be printed out return from the teletype digit-control switch.
NR 10^9 to 10^0	1402	Complete W-register output 10^9 being the most significant digit and 10^0 being the least significant digit.
NR "0"	1402	Common point of diodes going to the non-bar side of the W-register. Used to indicate zero and for reset of W-register.
NR adder sw. in	1402	Combined points of the switched input to the W-register adder.
NR adder result	1402	Summed result of least significant digit position of W-register and input of W-register adder.
$\overline{\text{NRP}}$	1501	Pulse used for resetting W-register.
NR sw. in	1402	Combined points of the switched input to the W-register.
$\overline{\text{NRT}}$	1501	Test pulse for testing W-register equal to zero.
NR0	1405	DC level indicating zero in W-register.
NR 9's comp	1405	DC level control of 9's complement circuit between the W-register and the W-register adder.
NR out multiplexer 10^0 - 10^9	1411	W-register output to the output connector. Complete W-register non-bar output through 2.2k resistors.
NR in multiplexer 10^8 + 10^9	1411	2 most significant digit output through 2.2k resistors from W-register. Non-bar.
Option reset	1411	Variable time delay signal for use with printers.
OSC	1412	Oscillator (9.09 milliseconds) for teletype card.
$\overline{\text{OMS}}$	1501	Pulse generated to set the channel of the output multiplexer.
PSD	1412	Decoded output of counter that selects digit to be serialized by the teletype card.
PA	1405	Master control flip-flop for log and anti-log processing.
PC	1408	2 decade (units = BCD tens = binary) counter for selection of reader position.
PR0	1501	Presets PC to position 00.

SIGNAL	SOURCE	CONTROL OR FUNCTION
PR1	1501	Presets PC to position 03.
PR2	1501	Presets PC to position 06.
PR3	1501	Presets PC to position 09.
PR0-3	1501	Pulse generated by PR0, 1, 2, or 3.
PCA	1501	Pulse generated by write key.
PCB	1501	Pulse generated by CR key.
PCF	1408	Flip-flop controlling stepping of PC counter.
PCP	1408	Flip-flop that controls PC stepping if one of the six decision making tests are true.
PCT	1408	Stepping pulse of PC counter.
RDS	1412	Reader start control of teletype.
RE	1501	Pulse generated by the run key.
READ	1501	Pulse generated by READ key.
REP	1408	Delayed pulse generated by RE.
RF	1412	Flip-flop controlling operation of reader in the teletype.
RO gate	1402	Signal coming from W-register adder input indicating a number 5 or greater.
RO	1405	Flip-flop for memory of RO gate.
RS	1405	Reset signal generated by RT.
RST	1407 or 1410	Flip-flop controlling restore operation.
RT	1405	Flip-flop set when first number after an operation is entered into the LOCI.
RXP	1411	Pulse generated by LANP used for reset.
SA	1410	1, 2, 4, 8 flip-flop storage of sensing amplifier outputs.
SA gate	1410	Gates on correct sensing amplifier output to SA storages.
SA reset	1410	Signal generated by leading edge of SA gate to reset SA storages.
SM	1405	Flip-flop controlling summing of W-register and A-register.
SN	1403	Flip-flop memory of sign of W-register.
SNT	1501	Test pulse for testing of SN.
SN J1	1411	SN output through a 2.2k resistor to input connector.
SN J2	1411	SN output through a 2.2k resistor to output connector.
ST	1407 or 1410	Flip-flop control for store operation.
STP	1501	Pulse generated by stop code.
Strobe Pulse	Input Mult.	Pulse generated by input multiplexer to set the input control code into the LOCI.
S1	1403	Pulses that step ER counter during entrance of numbers.

SIGNAL	SOURCE	CONTROL OR FUNCTION
S2	1403	Pulses that shift W-register during entrance of numbers.
$\overline{S3}$	1405	Pulse probe to step LP counter during log operation.
S4	1405	Signal output controlled by LP1 that is o.v. during all even steps and -v. during all odd steps.
S7	1405	Pulse generated to omit NLPO step during number to log process.
S14	1405	DC level going negative during all of anti-log process except NLP0 or NLP1.
S16	1403	Pulses that shift in the number of zeros left in DCN if the log was negative at the beginning of an anti-log.
S18	1406	DC level when negative indicates that DCN is less than DCA during decimal alignment.
S19	1406	DC level when negative indicates that DCN is not equal to DCA during decimal alignment.
S21	1406	Pulse that adds a positive carrier to A-register at end of add cycle.
S22	1406	DC level for gating on portion of switch to insert positive or negative carrier in A-register.
S25	1406	Gates on NR adder result switch in A-register during add cycle.
S29	1406	Pulse that turns on ACN when the number in A-register is changed from positive to negative.
S30	1406	Pulse that turns off ACN when the number in A-register is changed from negative to positive.
S31	1406	Pulse that adds a negative carrier to A-register at end of subtract cycle.
S34	1406	DC level when negative indicates that DCN ='s DCA during transfer of A-register to W-register.
S36	1406	DC level indicating A-register is negative during transfer of A-register to W-register.
TI	1412	Input signal from the teletype to the 1412 card.
TMC	1412	Master control flip-flop in the teletype card.
TO	1412	Output signal from the 1412 card to the teletype.
TPO	1412	Driver output to a relay in the teletype that omits print out.
TSP	1412	Pulse that steps reader on teletype.
TSS	1412	Switch that gate controls reader of the teletype (one-step or continuous).
TSW output	1412	Teletype switch used for serializing W-register.
T1	1404	One of two main timing pulses.
T2	1404	One of two main timing pulses.
TD 0-16 out	—	Decoding of 16-step clock used in each cycle of operation.
Z gate	1501	Reader code input to LOCI.
Z out	1501	Control flip-flops that are set for the code input to the LOCI. They are the only means of controlling the operation of the LOCI.
0-9	1501	Pulse generated by any number input.

The LOCI has been designed to do many things. Discover what your LOCI can do for you.

NOTES

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