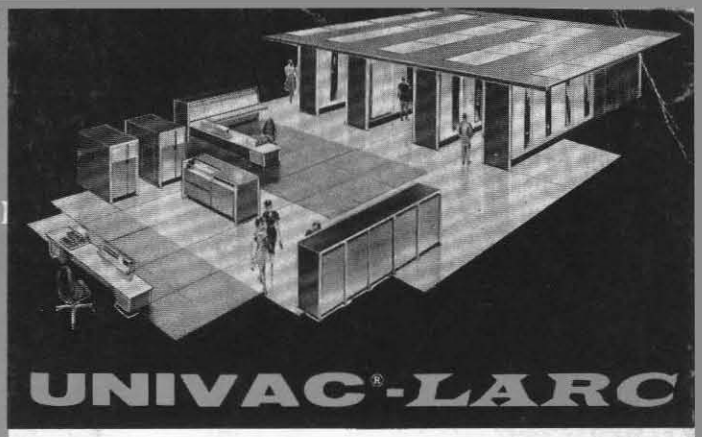

UNIVAC®-LARC

GENERAL DESCRIPTION

UNIVAC®-LARC System

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

GENERAL DESCRIPTION

The UNIVAC®-LARC System

Contents

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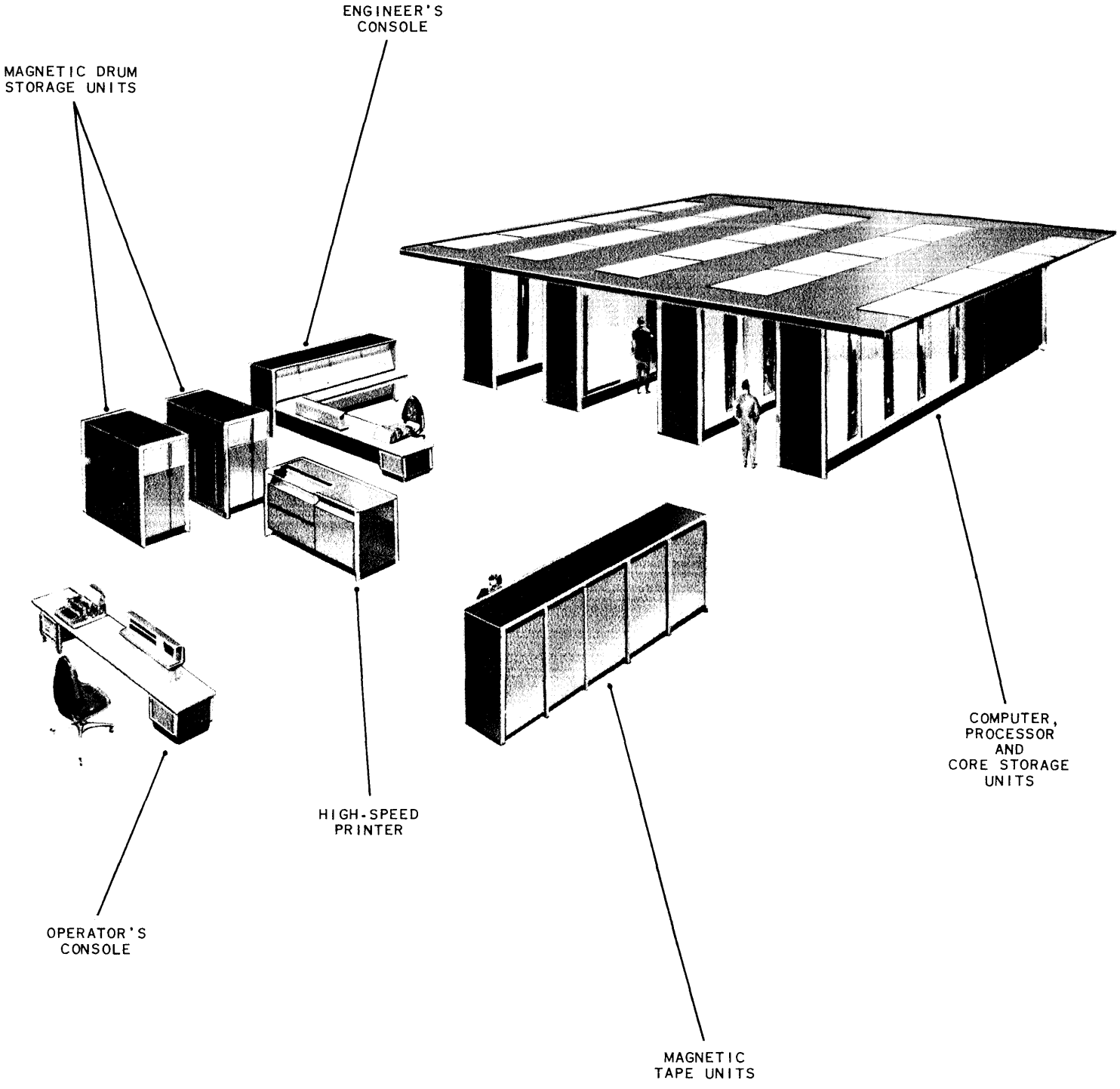


The UNIVAC-LARC

The Remington Rand UNIVAC-LARC is a general-purpose computing system designed to solve a wide variety of problems that are beyond the range of current large-scale systems. It is both a business and scientific data-processing system. In fact, this new Remington Rand System removes the line, established previously in both computer design and applicability, that has divided scientific and business data-processing systems. As scientific principles continue to be expanded and interrelated with the solution of business and industrial problems, this alone represents a tremendous advance.

The UNIVAC-LARC incorporates many modern electronic data-processing advances including modular construction, large data storage, versatile input-output, solid-state circuitry, "time-shared" operation, and extremely fast computation.

The wide range between the basic and expanded UNIVAC-LARC Systems allows the user to select a system to meet immediate needs while allowing for expansion in the future. A basic UNIVAC-LARC, for example, includes a Computer, for high-speed arithmetic and logical computations, and a Processor for handling input-output and "secondary" computing operations. In an expanded system, two Computers may be included for greatly increased computing capacity.

Supporting the computing units of the UNIVAC-LARC is an extensive high-speed data storage system. Comprised of magnetic ferrite-core and magnetic drum storage units, the UNIVAC-LARC storage is expandable to a capacity of over 73 million decimal digits of information.

The input-output units of the UNIVAC-LARC System offer magnetic tape input-output, high-speed punched-card input, output printers which produce printed lines at a rate of 600 per minute, and page recorders which record an entire page at a speed of 10,000 lines per minute. For even greater input-output versatility, the magnetic tape used with the UNIVAC-LARC is compatible with tapes used by UNIVAC I and II Systems and the broad complement of UNIVAC data-conversion devices.

The speed and reliability of solid-state circuitry and the efficiency of parallel input, processing, and output operations are combined in the UNIVAC-LARC System with a computing speed that is hundreds of times faster than most of today's large-scale data processors. Greater speed and reliability, coupled with the features of modular construction, large data storage, and application versatility, make the UNIVAC-LARC *the most powerful data-processing system commercially available today.*

COMPUTER AND PROCESSOR

A basic UNIVAC-LARC System contains a Computer and a Processor. Both have most of the attributes of a general-purpose computer but each performs specialized functions in the system. The primary function of the Processor is the control of all input-output operations and data transfers between the auxiliary storage and the main storage of the system. The Computer is designed to perform rapid arithmetic computation.

If increased computing capacity is required, the basic system may be expanded to include a second Computer. The Computers and the Processor are controlled by separate programs and operate cooperatively and independently with little direct communication.

The two Computers in an expanded system can be programmed to solve a single problem jointly or each Computer can solve independently one or more separate problems. The Processor is designed to accomodate the input, output, and auxiliary storage needs of both Computers. It can also perform any necessary editing of output data. If input-output demands are not excessive, the Processor can also perform sorting, merging and other operations simultaneously with the Computer programs.

STORAGE

A magnetic ferrite-core storage with a capacity of up to 97,500 12-digit words is accessible to both the Computer and Processor. With a word access time of 4 microseconds this storage serves as the main storage of the system and as a common communications link between the Computers, the Processor, the auxiliary magnetic drum storage and the input-output units.

The core storage is divided into independently operating modules. Instructions and operands are sent to and received from core storage at maximum speed and without interference. Any part of core storage not being used by the Computers can be used as an input-output buffer without slowing input-output data transfers for the Computers.

Since the Computers and the Processor have access to the same storage, they can alert one another to the presence of information in a particular part of storage. This permits an almost limitless degree of cooperation to be achieved between the Computers and the Processor.

The Computer can cause the Processor to transfer data between the main storage and a drum storage which has the capacity, speed, and reliability to keep abreast of the unusually high computing rates of the system.

INPUT AND OUTPUT

A full complement of both on-line and off-line input-output equipment can be provided with the system. The on-line equipment consists of:

1. *Magnetic Tape Read-Write Units* for fast introduction of data into the system and fast recording of output for subsequent conversion on an auxiliary device or for long-term storage.

2. *Electronic Page Recorders* for direct, fast recording of output data in either tabular or graphical form. The Page Recorder can represent output data as numeric or alpha-numeric characters in an edited or unedited format. It can also represent data in the form of plotted curves complete with call-outs, titles, scales, and grid patterns.

3. *On-line High-Speed Printers* for multiple-copy printing of numeric or alpha-numeric data in an edited or unedited format.

4. *A High-Speed Card Reader* for introducing data into the system directly from 80-column punched-cards at a speed of up to 450 cards per minute.

5 *Console Typewriter-Printers,* with an attached paper tape reader and punch, for communication between the Computer or Processor program and the operator.

UNIVAC-LARC off-line auxiliary equipment includes:

1. *The UNIVAC High-Speed Printer* for printing in an edited format data recorded on magnetic tape.

2. *The Unityper II* for direct keyboard-recording of data on magnetic tape.

3. *The Tape Verifier* for direct keyboard-recording of data on magnetic tape or verification and correction of data already recorded on magnetic tape.

4. *The Punched Card-to-Magnetic Tape Converter.*

5. *The Magnetic Tape-to-Punched Card Converter.*

6. *The Paper Tape-to-Magnetic Tape Converter.*

7. *The Magnetic Tape-to-Paper Tape Converter.*

8. *The Bi-Directional Paper-to-Magnetic Tape Converter.*

MODULAR CONSTRUCTION

The UNIVAC-LARC System consists of modular units ranging from solid-state component packages to input-output units, storage units, and complex computer units. These units can be joined together in various numbers and combinations to form a system balanced for a wide range of problems. The modular units of equipment that can be included in a UNIVAC-LARC System are listed in Table 1. With the exception of core storage, which must be added to the system in units of four, single units of each component may be added up to the maximum allowed for expansion.

Each cabinet within the system is self-contained and has its own power supplies, clock pulse generators, and heat exchangers. The Synchronizers are modular units of control represented by solid-state component packages contained within the Processor cabinet. The cabinet may contain all of the Synchronizers in the expanded system. Each of the storage and input-output units of the system is designed for off-line maintenance while the remainder of the system is operating. The tape, drum and core storage units are connected into the system by means of plugboards which make it possible to quickly substitute one unit for another of the same type.

Table 1. Modular Units of a Basic and Completely Expanded UNIVAC-LARC System.

EQUIPMENT NAME	BASIC	EXPANDED
Magnetic Core Storage Units (2500 words each)	8	39
Computers	1	2
Multipurpose Fast Registers (per Computer)	26	99
Processor	1	1
Drum-read Synchronizers	2	3
Drum-write Synchronizers	1	2
Tape Read-Write Synchronizers	2	4
Electronic Page Recorder Synchronizer	0	1
High-Speed Printer Synchronizer	1	2
Card Reader Synchronizer	0	1
Console Printer Synchronizer	1	1
Tape Positioning Checker	1	1
Magnetic Drum Storage Units (250,000 words each)	12	24
Uniservo II Magnetic Tape Units	4	40
Electronic Page Recorders	2	2
High-Speed Printers	1	2
High-Speed Card Readers	0	1
Operator Control Consoles	1	2
Numeric Keyboards (one per Console)	1	2
Alphanumeric Console Printers (one per Console)	1	2
Engineering Control Panel	1	1
Operator Control Panel	1	2
Numeric Keyboard	1	2
Alphanumeric Console Printers	1	2
Computer Engineer Control Panel	1	2
Processor Engineer Control Panel	1	1

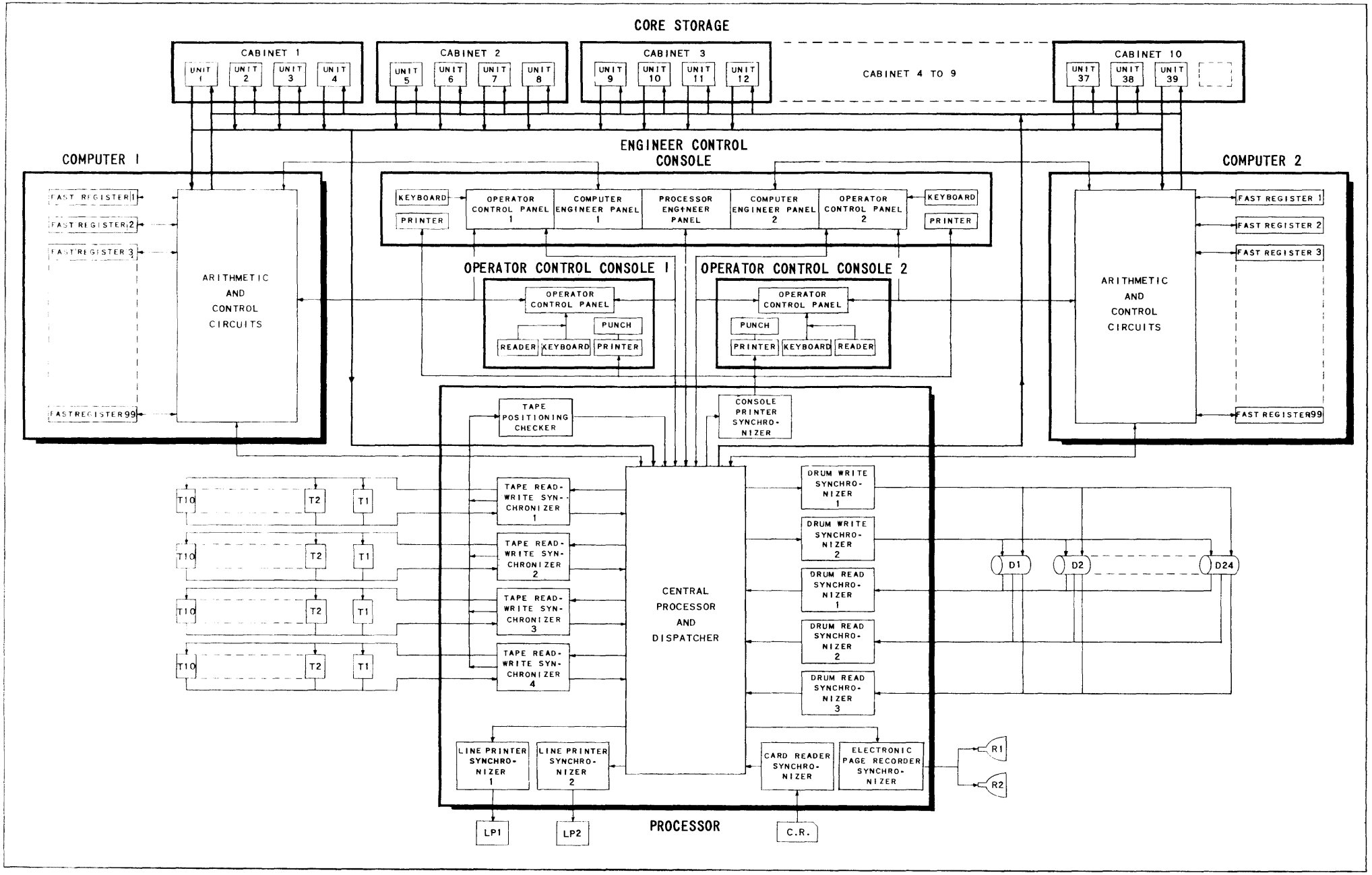


Figure 1. Block Diagram Of A Completely Expanded UNIVAC-LARC System

CHARACTER CODES

The basic internal code of the UNIVAC-LARC is a five-bit biquinary code in binary-coded decimal form. Alpha-numeric information is represented in the UNIVAC-LARC in *pairs* of numeric characters represented in the basic code. Thus, a word (12 digits) of alpha-numeric information actually consists of only six characters.

On UNIVAC Magnetic Tape, alpha-numeric characters are represented in the standard UNIVAC seven-bit excess-three code.

The numeric characters, when read into the LARC as alpha-numeric information, are expanded to digit pairs. The decimal digits are distinguishable in this mode because the most significant digit of the pair is always a 2.

UNIVAC CODE

LARC input data is represented on magnetic tape in the UNIVAC seven-bit excess-three code. Input information from the tapes is automatically translated to LARC internal code and output information that is to be recorded on tapes is automatically translated back the standard UNIVAC code.

The Tape Read-Write Synchronizers in the Processor can be instructed to translate a block of numeric input data into the LARC one-digit numeric code, or translate a block of alpha-numeric data into the LARC two-digit alpha-numeric code. Similarly, output can be translated from either the LARC one-digit numeric code or two-digit alpha-numeric code.

LARC ONE-DIGIT NUMERIC CODE

In the basic five-bit biquinary code of the UNIVAC-LARC, 15 digit combinations are allowed, any one of which may be stored in any digit position in storage.

The 15 combinations and the characters they normally represent are shown on the following page. The fifth bit of the code is a parity check bit. Only combinations containing an odd number of binary "ones" are allowed. The code combination 001101, although it contains an odd number of "ones", is not allowed.

In the Computer, all 15 digit combinations can be shifted, extracted or transferred. Except for a minus or period digit in the sign position, only the numerics 0 through 9 are allowed in the adder-comparator of the Computer. In the Processor adder-comparator, however, the non-numeric digits (plus, minus, space, period, and ignore) are allowed in any digit position of a word. When non-numerics are added, they appear in the result in accordance with a predetermined order of precedence. (Word formats for both the Computer and the Processor are explained in later sections of this manual.)

BIT POSITIONS	
5 4 3 2 1	Character
1 1 1 0 0	\ (ignore)
0 0 1 0 0	∧ (space)
0 0 0 1 0	– (minus)
1 0 0 0 0	0
0 0 0 0 1	1
1 0 0 1 1	2
0 0 1 1 1	3
1 0 1 1 0	4
0 1 0 0 0	5
1 1 0 0 1	6
0 1 0 1 1	7
1 1 1 1 1	8
0 1 1 1 0	9
1 1 0 1 0	. (period)
1 0 1 0 1	+ (plus)

LARC TWO-DIGIT ALPHA-NUMERIC CODE

An alpha-numeric character is represented in LARC by two adjacent numeric digits that are handled as a pair. An equivalent alpha-numeric character is represented on magnetic tape by a single 7-bit digit in UNIVAC magnetic tape code. The decimal equivalent of the LARC two-digit code is shown in Table 2.

ELECTRONIC PAGE RECORDER

The Electronic Page Recorder Synchronizer can operate in any one of the four following modes:

1. Numeric edited.
2. Numeric unedited.
3. Alpha-numeric edited.
4. Alpha-numeric unedited.

When the Synchronizer operates in the numeric modes (modes 1 and 2), a single LARC digit is decoded to perform a function or record a character. In the numeric edited mode, the ignore digit (11100) and the space digit (00100) are decoded to perform specific functions. The ignore digit performs an end-of-word function. For example, a 12-digit word containing an ignore digit in the ninth digit position is shortened to eight digits when it is recorded in the numeric edited mode. The space digit performs a space function (it leaves a single space in the printed copy). In the numeric unedited mode, the ignore and space digits are decoded to record as \ and ∧ , respectively.

When the Synchronizer operates in the alpha-numeric modes (modes 3 and 4), a LARC two-digit alpha-numeric combination is decoded to perform a function or record a character. In the alpha-numeric edited mode, the combinations 15, 16, and 35 (Table 2) are decoded to perform specific functions. A 15 performs an ignore function, that is, the Synchronizer neither prints a character nor leaves a space but ignores the combination. A 16 performs a space function. A 35 performs an end-of-ten-words function, that is, no more data are sent to the Recorder. In the alpha-numeric unedited mode, the two-digit combinations 15, 16 and 35 are decoded to record as \ , Λ , and ϵ , respectively.

ON-LINE HIGH-SPEED PRINTER

The On-line High-Speed Printer Synchronizer can operate in any one of the four following modes:

1. Numeric edited.
2. Numeric unedited.
3. Alpha-numeric edited.
4. Alpha-numeric unedited.

When the Printer operates in the numeric modes (modes 1 and 2), a single LARC digit is decoded to perform a function or print a character. In the numeric edited mode, both the ignore (11100) and the space (00100) digits are decoded to leave a space. In the numeric unedited mode, the ignore and space digits are decoded to print as I and Δ , respectively.

When the Synchronizer operates in the alpha-numeric modes (modes 3 and 4), a LARC two-digit alpha-numeric combination is decoded to perform a function or print a character. In the alpha-numeric edited mode, a 16 combination is decoded to leave a space. In the alpha-numeric unedited mode, a 16 combination is decoded to print as a W.

CONSOLE PRINTER CODE

Because the Console Printer is a relatively slow device, its Synchronizer is designed to operate only in the alpha-numeric mode. The form a print-out takes is determined by the Processor program. If numeric data is printed, it is first translated by the Processor program to the two-digit alpha-numeric code. The Printer Synchronizer decodes a LARC two-digit alpha-numeric combination to perform a function or print a character. Many of the two-digit combinations can print either of two characters depending upon whether the type basket of the printer is in the upper or lower case. The type basket is shifted to the upper case position by the two-digit combination 10 and is shifted to the lower case position by the combination 11.

The following two-digit combinations are decoded by the Synchronizer to perform specific functions. In each case the same function is performed regardless of whether the type basket is in the upper or lower case.

15 - neither prints a character nor leaves a space, but is ignored.
16 - leaves a space.
35 - returns the carriage to the left margin.
55 - advances the carriage to the next present tab stop.

The Console Printer may also be used to prepare punched paper tapes. With the type basket in the upper case position, all 15 LARC code combinations and several special code combinations may be punched on the paper tape.

CONSOLE KEYBOARD CODE

The keyboard on the Operator Control Console is used to manually enter data into either the five-digit or 12-digit display register. It consists of 18 keys. Fifteen keys are used to enter the 15 LARC code combinations into either display register; two keys are used to connect the keyboard to the proper display register, and one key is used to disconnect the keyboard from the display registers.

CONSOLE DECIMAL DISPLAYS

The decimal displays on the Operator Control Console display in decimal form the contents of the five-digit display register, the 12-digit display register, and a Computer control counter register. Characters representing all of the 15 LARC code combinations may be displayed. Since the number of single characters that can be displayed is limited to 12, the ignore, space, and period are represented by superimposing one character upon another. The ignore is represented by a 1 and 8 superimposed, the space by a 0 and — superimposed, and the period by a 1 and 0 superimposed.

TABLE 2. COMPARISON OF LARC CHARACTER CODES

UNIVAC CODE ON TAPE	LARC NUM. 1-DIGIT CODE	LARC ALPHA. 2-DIGIT CODE	STANDARD UNITYPER II	ELECTRONIC PAGE RECORDER NUM. MODE	ELECTRONIC PAGE RECORDER ALPHA. MODE	ON-LINE PRINTER NUM. MODE	ON-LINE PRINTER ALPHA. MODE	CONSOLE PRINTER (ALPHA.) UPPER CASE	CONSOLE PRINTER (ALPHA.) LOWER CASE	CONSOLE KEYBOARD (NUM.)	CONSOLE DECIMAL DISPLAYS (NUM.)
		10						UC	UC		
		11						LC	LC		
		2-						–	–		
		2Λ						Λ	π		
		2+						+	+		
		2.						.	.		
		2\						\	ρ		
1 00 0000	11100	15	i	EOW(\)	IG(\)	SP(I)		IG	IG	\	⊄
0 00 0001	00100	16	Λ	SP(Λ)	SP(Λ)	SP(Δ)	SP(W)	SP	SP	Λ	Θ
0 00 0010	00010	17	–	–	–	–	–	–	–	–	–
1 00 0011	10000	20	0	0	0	0	0	0	λ	0	0
0 00 0100	00001	21	1	1	1	1	1	1	U	1	1
1 00 0101	10011	22	2	2	2	2	2	2	I	2	2
1 00 0110	00111	23	3	3	3	3	3	3	3	3	3
0 00 0111	10110	24	4	4	4	4	4	4	J	4	4
0 00 1000	01000	25	5	5	5	5	5	5	K	5	5
1 00 1001	11001	26	6	6	6	6	6	6	L	6	6
1 00 1010	01011	27	7	7	7	7	7	7	M	7	7
0 00 1011	11111	28	8	8	8	8	8	8	,	8	8
1 00 1100	01110	29	9	9	9	9	9	9	/	9	9
0 00 1101		32	'		=		=		=		
0 00 1110		33	&		~		~	€	~		
1 00 1111		34	(		(		(		(		
0 01 0000		35	r		EOL(€)			CR	CR		
1 01 0001		36	,		,		,	8	,		
1 01 0010	11010	37	.	.	.	.	.	.	.	.	ϕ
0 01 0011		40	;		∇		∇		∇		
1 01 0100		41	A		A		A		A		
0 01 0101		42	B		B		B	>	B		
0 01 0110		43	C		C		C	*	C		
1 01 0111		44	D		D		D	→	D		
1 01 1000		45	E		E		E	Σ	E		
0 01 1001		46	F		F		F	η	F		
0 01 1010		47	G		G		G	:	G		
1 01 1011		48	H		H		H		H		
0 01 1100		49	I		I		I	2	I		
1 01 1101		52	#		<		<		<		
1 01 1110		53	¢		ρ			\	ρ		
0 01 1111		54	@		π			Λ	π		
0 10 0000		55	t		α			TAB	TAB		
1 10 0001		56	"		]				]		
1 10 0010		57	|		[			α	[		
0 10 0011		60	)		)		)	□	)		
1 10 0100		61	J		J		J	4	J		
0 10 0101		62	K		K		K	5	K		
0 10 0110		63	L		L		L	6	L		
1 10 0111		64	M		M		M	7	M		
1 10 1000		65	N		N		N		N		
0 10 1001		66	O		O		O	3	O		
0 10 1010		67	P		P		P		P		
1 10 1011		68	Q		Q		Q		Q		
0 10 1100		69	R		R		R		R		
1 10 1101		72	$		>		>				
1 10 1110		73	*		*		*				
0 10 1111		74	?		→						
1 11 0000		75	Σ		Σ						
0 11 0001		76	β		η						
0 11 0010		77	:		:		:				
1 11 0011	10101	80	+	+	+	+	+	+	+	+	+
0 11 0100		81	/		/		/	9	/		
1 11 0101		82	S		S		S		S		
1 11 0110		83	T		T		T		T		
0 11 0111		84	U		U		U	1	U		
0 11 1000		85	V		V		V		V		
1 11 1001		86	W		W		W		W		
1 11 1010		87	X		X		X		X		
0 11 1011		88	Y		Y		Y		Y		
1 11 1100		89	Z		Z		Z		Z		
0 11 1101		92	%		Δ		Δ		Δ		
0 11 1110		93	=		λ			0	λ		
1 11 1111		94			□						

ABBREVIATIONS

EOW - End of Word
SP - Space
IG - Ignore
EOL - End of Line (10-Words)
UC - Upper Case
LC - Lower Case
CR - Carriage Return
TAB - Tabulate

The Computer

The Computer of the UNIVAC-LARC System is specifically designed to rapidly and economically perform fixed or floating point arithmetic operations in single or double-precision. To accomplish this, many operations are performed in parallel including the transfer and processing of bits and digits of a Computer word. Secondary operations such as input, output, storage transfer, address modification, floating point, and error checking operations, which otherwise slow arithmetic and logical operations, are also performed in parallel with these operations.

COMPUTER WORD FORMAT

A Computer word usually consists of 11 decimal digits and an algebraic sign. Two Computer words may be combined for double-precision operation. The form of the words used in the system is shown in Figure 2.

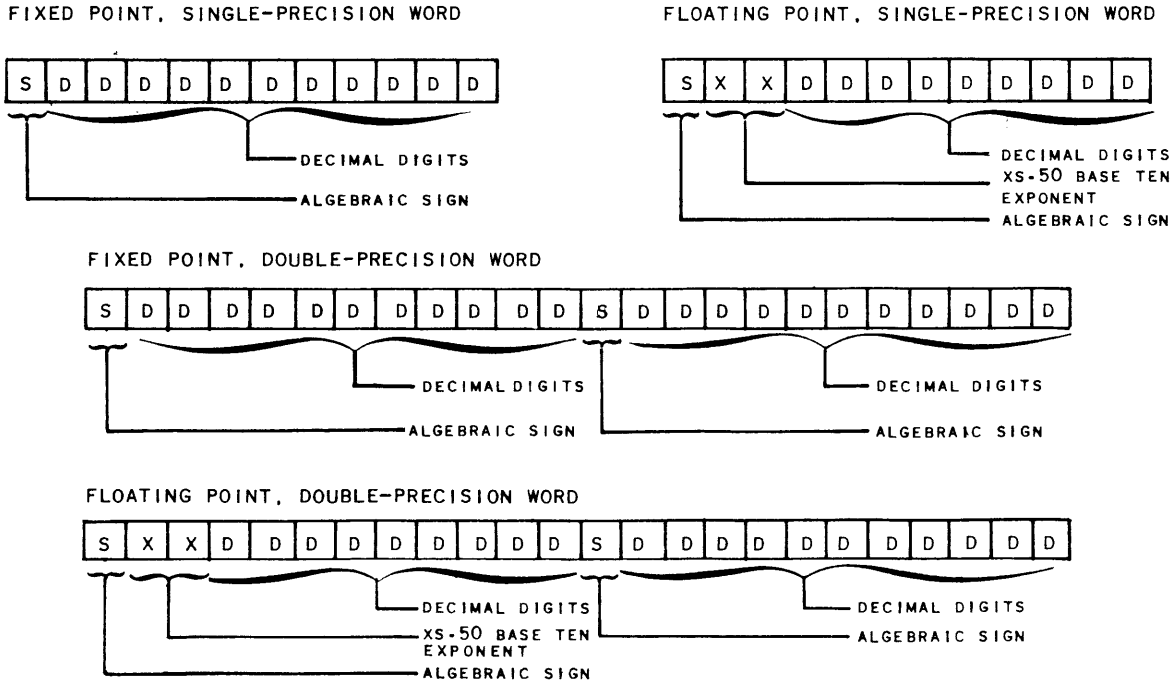


Figure 2. UNIVAC-LARC Computer Words

INSTRUCTIONS

The repertoire of the Computer includes 75 instructions. Many are variants of other instructions included to provide the programmer with a wide choice of alternatives to suit the requirements of a particular problem. They also increase the speed of computation by enabling operations to be performed with fewer instructions than would otherwise be required.

Many Computer instructions are, in effect, built-in subroutines. By designing into the instructions operations which formerly had to be programmed, more of the Computer program and the efforts of the programmer can be devoted to furthering the computations at hand rather than to organizing the computations or the program itself.

Table 3 contains performance times, expressed in microseconds, for representative Computer arithmetic instructions.

Table 3. Arithmetic Instruction Execution Times

	SINGLE-PRECISION		DOUBLE-PRECISION	
	FIXED POINT	FLOATING POINT	FIXED POINT	FLOATING POINT
ADD OR SUBTRACT	4	4	12	16
MULTIPLY	8	8	36	36
DIVIDE	32	28	184	168

The instruction times listed include the time required for storage access, address modification, error checking, etc. All input, output, and auxiliary storage operations may be assumed to be performed in parallel with the instructions. A complete list of computer

INSTRUCTION WORD FORMAT

A UNIVAC-LARC Computer instruction word is composed of 12 decimal digits. The format of an instruction word is illustrated in Figure 3, below:

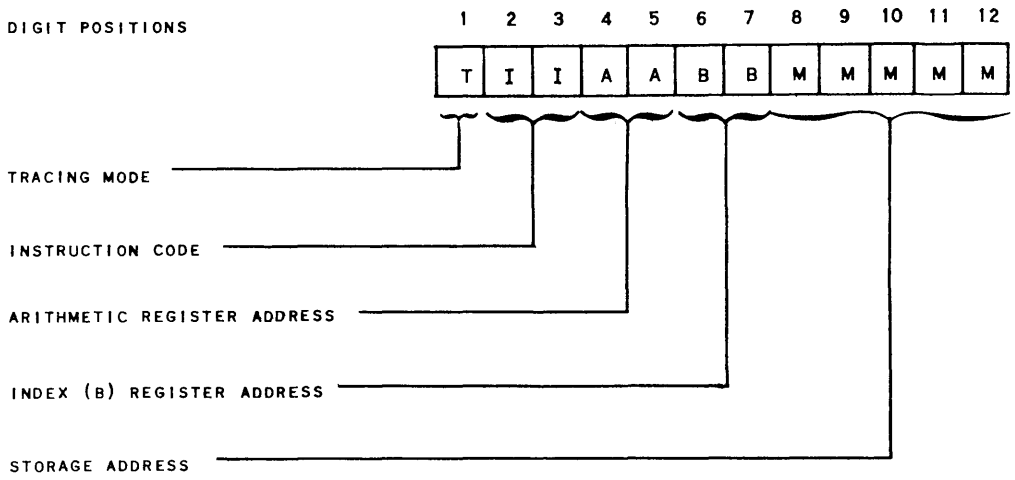


Figure 3. Instruction Word Format

Tracing Mode

Any Computer instruction may be tagged with any one of nine tracing mode digits (1-9). Just before an instruction is executed, the tracing mode digit is detected and, if the Computer is operating in the designated tracing mode, an automatic transfer of control will be effected to a routine associated with the tracing mode digit. At the completion of the routine, control is transferred back to the main program. Instructions are available which direct the Computer to enter or leave any one of the nine tracing modes.

An "enter tracing mode seven" instruction, for example, will cause all succeeding instructions that are tagged with a tracing mode seven digit to cause a transfer of control to an associated routine. Either the program directly or the operator indirectly, by a manual intervention routine, may instruct the Computer to enter or leave any one of the nine tracing modes. The tracing mode routines can be constructed to perform any number of functions. Usually these functions are related to debugging or monitoring a program.

Instruction Code

Digit positions two and three of a Computer instruction word contain the instruction code for the operations to be executed by the Computer. An instruction code not in the Computer repertoire of instructions will cause a transfer of control to an error routine.

Arithmetic Register Address

The address of one of the multipurpose fast registers is normally contained in digit positions four and five of a Computer instruction word when the register is to be used as an arithmetic register for storing operands and processing results.

Index Register Address

Instruction word digit positions six and seven normally specify the address of one of the multipurpose fast registers that is to be used as and index (B) register for storing an address modifier. The storage address (m) portion of an instruction is automatically modified by a modifier in the specified index register after the instruction is read from storage, but before the instruction is executed.

If the index register specified is 00, the m address is not modified. All normal Computer instructions containing an operand address may refer to an index register for modification of the address.

Storage Address

The storage address portion of the instruction, digit positions eight through 12, usually specifies the address of an operand. It may contain a main storage address or the address of a multipurpose fast register.

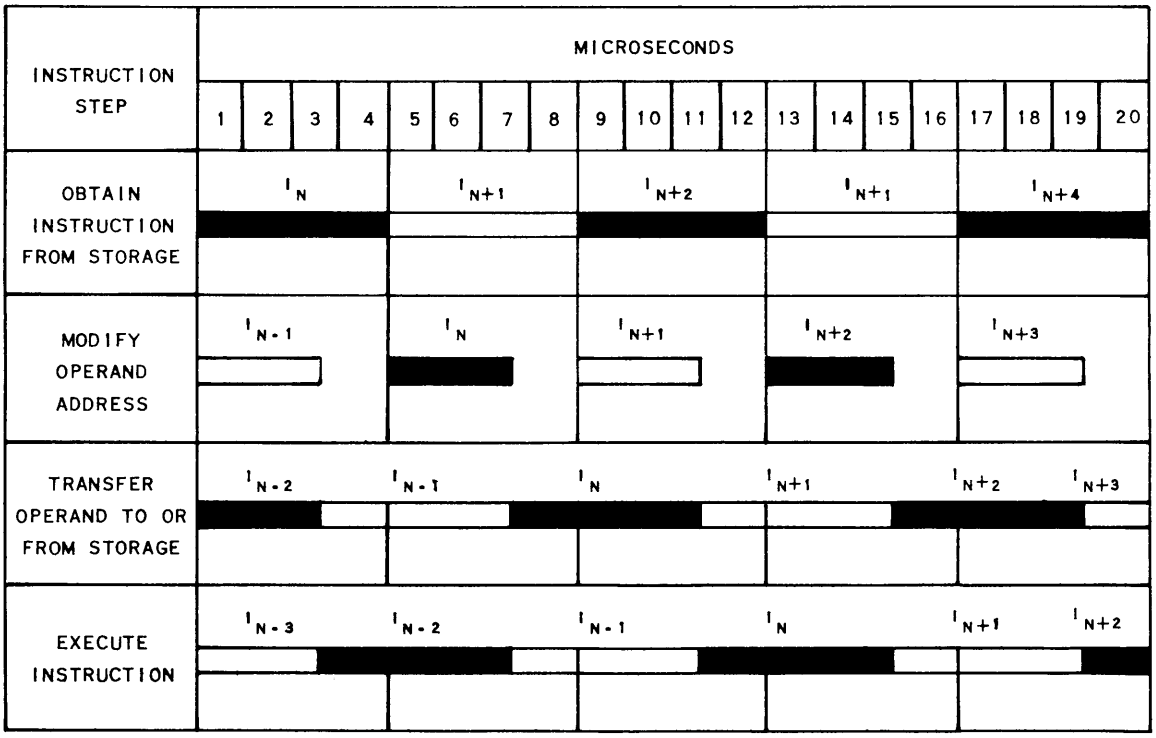
INSTRUCTION OVERLAPPING

The Computer is designed to process several instructions simultaneously and perform different steps of the several instructions in parallel. While one instruction is actually being executed, the operand of second instruction is being transferred to or from storage, the operand address of a third instruction is being modified, and a fourth instruction is being obtained from storage. This is illustrated in Table 4 which shows a simplified timing diagram for a series of addition instructions.

Although an add instruction actually takes more than four microseconds to perform, a series of these instructions are executed at the rate of one every four microseconds. For all practical purposes the total instruction time is four microseconds.

If control is transferred to a new sequence of instructions, the first instruction of the new sequence would require time to propagate through the several steps before it is executed. Therefore, whenever a transfer of control takes place, eight microseconds are added to the execution time of the instruction that caused the transfer.

Table 4. Simplified Timing Diagram of a Sequence of Four-Microsecond Computer Instructions



SENSE FLIP-FLOPS

The Computer instruction code contains instructions for setting or resetting any one of ten sense flip-flops together with transfer of control instructions that are conditional on the state of the sense flip-flops. The sense flip-flops have no predetermined function. Essentially, they are general-purpose single-bit storage units that may be used by the programmer in numerous ways. The sense flip-flops may be set directly by the program or indirectly through manual intervention by the operator.

ADDRESS MODIFICATION

Any Computer instruction that contains an operand address may be tagged with the address of any index register. Before such an instruction is executed, its operand address will be modified automatically by the addition of a constant contained within the specified index register. Arithmetic instructions also contain the address of an "accumulator" register which is used to store an operand involved in an instruction or the result of an instruction.

Iterative address modification techniques have been applied in the past only by sacrificing considerable computing time. Often such techniques were used merely as a convenient way of exchanging computing time for storage space in fitting a particular problem to the computer. The fast registers in the UNIVAC-LARC Computer not only enable the address modification operations to be completely overlapped with the execution time of the instruction, but they also enable extremely flexible control to be exercised over the iterative processes.

An instruction may be tagged to refer to any one of the fast registers for address modification. Since a fast register that is used as an index register may also be used in the role of an accumulator register, its contents are subject to all of the arithmetic, test, and other instructions in the computer repertoire. Special index instructions are also provided which are, in effect, small subroutines for controlling the entry, re-entry, and exit from the program loop using control information stored within the index register.

The UNIVAC-LARC Computer is a single address computer, since each instruction contains only one main storage address. However, any one (or two) of a number of fast registers may be addressed and used by an instruction either as an accumulator register or in the same way as a standard storage location. Arithmetic instructions are also available which take one operand from one fast register, a second operand from main storage, and place the result in an adjacent fast register. In practical use these features enable the Computer to be used as a three-address computer. Quantities can be accumulated in several fast registers and combined without recourse to separate instructions for returning intermediate partial results to the main storage.

MULTIPURPOSE FAST REGISTERS

The index and accumulator registers are multipurpose fast registers that are logically interposed between the main core storage and the arithmetic system of the Computer. They may be addressed and used interchangeably as index registers, as accumulator registers or as a standard core storage location.

The registers are composed of fast-switching tape-wound cores having a read-regenerate or clear-write cycle of one microsecond. By functioning as fast-access storage for operands and results in either arithmetic operations or address indexing operations, they decrease the number of references to the slower main core storage and improve control of the arithmetic processes.

As many as 99 multipurpose registers may be included in the Computer. These are in addition to the various control and arithmetic registers that are used during the actual execution of an arithmetic instruction.

INDEX REGISTER WORD FORMAT

A UNIVAC-LARC index word contains 12 digits in the format shown in Figure 4.

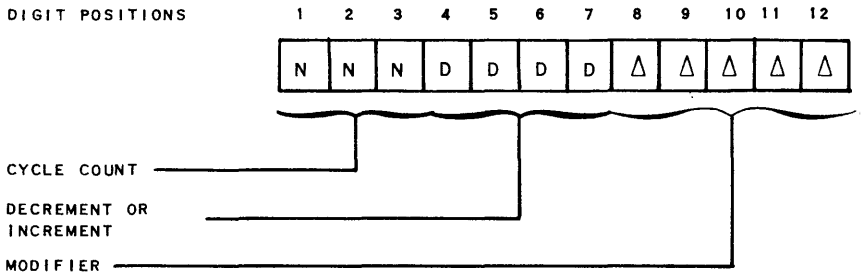


Figure 4. Index Word Format

Cycle Count

Digit positions one, two and three of an index register word contain the number of the times an iterative program loop is to be traversed. The number specified is reduced by one each time the program loop is traversed. When the count becomes zero, the iterative process is terminated.

Decrement or Increment

Before each program loop traversal, an increment or decrement is added or subtracted from the index word modifier (digits eight through 12). The increment or decrement number is contained in digit positions four through seven of the index register word.

The increment or decrement is a constant which indicates the amount by which the operand addresses of indexed instructions are to be modified during each program loop traversal relative to the previous loop traversal.

Modifier

The modifier, contained in digit positions eight through 12 of the index word, is automatically added to the m part of an instruction that addresses the index register in which the modifier is located.

EXECUTIVE COMMAND OF THE PROCESSOR

The code of the Computer does not include instructions for controlling input, output, and auxiliary storage operations directly. All such operations are handled by the Processor under executive command of the Computer. Consequently, the Computer is free to devote substantially all of its time to performing arithmetic operations. Input, output and editing commands may be summarized by the Computer in well-defined pseudo orders having adjustable parameters and issued to the Processor singly or in groups via the core storage.

The Computer program is required only to place the summary orders in the storage, alert the Processor to their presence, and check for their completion after a period of time has passed during which the summary orders are executed independently by the Processor.

The Processor may also be programmed to relieve the Computer program of the task of generating and issuing summary orders and, in fact, relieve it of all concern with input, output and drum operations. Computer time can thus be devoted exclusively to arithmetic and related logical operations. In any case, the computer programmer will be concerned, not with the details of the input, output, and drum operations, but with logistical problems of anticipating storage requirements, allocating storage, and directing the flow of data to and from the storage.

ERROR CHECKING

In many data-processing installations considerable computing time is wasted in detecting and correcting errors. To prevent the loss of valuable computer time, an error occurring in the UNIVAC-LARC System is detected automatically and, whenever possible, corrected without human intervention. When manual intervention is necessary, the general source of the error is detected and isolated from the system. The error is pin-pointed and corrected "off-line", thereby releasing the system for further computation.

BUILT-IN CHECKING CIRCUITRY

The Computer contains built-in checking circuits designed to detect all single-bit errors. The checking circuits are designed to detect an error and indicate the specific area of the Computer in which the error occurred. Twenty percent of the total circuitry in the UNIVAC-LARC System is devoted to redundant circuits and associated checking circuits. These circuits double the utility of the system by locating faults and by eliminating the need for programmed checks.

ERROR PROCEDURES

When an error is detected, control is transferred to an instruction in a specific storage location which is the beginning of an error routine. The routine determines the type of error committed and then initiates a print-out which assists the maintenance engineer or programmer in analyzing and correcting the error. The print-out might contain the following information;

1. The type of error (adder, index register, etc.);
2. The digit position at which the error occurred;
3. The time at which the error occurred;
4. The instruction that caused the error;
5. The storage address of the instruction that caused the error;
6. The contents of the accumulator register or registers involved, if any;
7. The contents of the index (B) register involved, if any; and
8. The operand involved.

More elaborate error routines can be designed which will isolate the error source still further and print out the designations of the specific printed circuit packages that are to be replaced. However, such routines might not be justified by the frequency of occurrence of the errors.

CONTINGENCY CHECKING

The Computer contains checking circuits for detecting overflow conditions within the arithmetic system and certain conditions reflecting mistakes in programming. If one of these conditions arises, it is handled in much the same way as a machine error in that the Computer automatically transfers control to an error routine. These built-in circuits continuously and automatically check for the following conditions:

1. *Floating Zero Result:* occurs on floating point add and subtract instructions when an arithmetic subtraction of two numbers with equal exponents produces a zero answer.
2. *Non-normalized Divisor:* occurs on floating point division instructions when the divisor has a zero in the most significant digit position (the digit position adjacent to the exponent).
3. *Exponent Overflow:* occurs on floating point add, subtract, multiply, and divide instructions when the addition, subtraction, multiplication, or division of two floating point numbers results in an exponent greater than 99.
4. *Exponent Underflow:* occurs on floating point add, subtract, multiply, and divide instructions when the addition, subtraction, multiplication, or division of two floating point numbers results in an exponent less than 00; or on fixed-to-floating point or floating-to-fixed point conversion instructions which would cause a loss of significant digits.
5. *Fixed Decimal Overflow:* occurs on single and double left shift instructions when at least one non-zero digit is shifted out of the register causing a loss of significant digits; or on fixed point add, subtract, multiply, and divide instructions when the result is greater than or equal to one in absolute value.

The Processor

The Processor is a stored-program two-address computer with many general-purpose characteristics. Its primary role in the UNIVAC-LARC System is to coordinate and control concurrent input, output and auxiliary drum storage operations under summary command of the Computer program.

FUNCTIONAL DESCRIPTION

The Processor picks up summary orders issued by the Computer, acknowledges their receipt, interprets them, supervises their execution, and informs the Computer of their completion. All these functions are accomplished under control of a fluid loop program which need not change for every program run on the Computer. A flexible Processor program for controlling input, output, and auxiliary storage was developed along with the UNIVAC-LARC System as the equipment was developed and tested. In fact, the program, in conjunction with the general-purpose computing abilities of the Processor, is an alternative to using a multitude of costly and inflexible built-in control equipment to perform a similar function.

An important advantage of the programmed-control approach is that the programmer is given the ability to modify the input, output and auxiliary storage control. As a programmer gains experience with the system, he may take advantage of advanced programming techniques to devise control programs for the Processor which will greatly improve and even change the performance characteristics of the Processor.

The Processor has sufficient speed and flexibility to handle the complete complement of input, output, and auxiliary storage devices in parallel, and to service both Computers in the expanded system. Its general-purpose characteristics enable the system to be expanded with ease and molded to a customer's requirements without conflicting with previously designed Computer programs.

When the Processor is not being used to the limit of its ability in controlling input, output, and auxiliary storage, it can relieve the Computer of various tasks, or it can perform sorting, merging, compiling, or other "side" routines concurrently with and entirely unrelated to a program being run on the Computer.

Logically, the Processor separates into three major sections which represent different levels of control. The three major sections are:

1. The Central Processor.
2. The Synchronizers.
3. The Dispatcher.

CENTRAL PROCESSOR

The Central Processor is the general-purpose computing section of the Processor. Compared to the Computer, it has less elaborate facilities for performing arithmetic operations. The arithmetic system of the Central Processor consists of a serial adder-comparator and two connecting 12-digit shift registers that are used for the temporary storage of operands. When an add instruction is executed, operands are shifted from the two registers into and through the adder a digit at a time. The result is shifted back into one of the registers, which also serves as an accumulator register. The bits and digits of a word are transferred between the registers and the main core storage completely in parallel.

INSTRUCTIONS

The Central Processor has an instruction code that is separate and distinct from that of the Computer. It contains a complement of general-purpose instructions, such as add, subtract, shift, and transfer, that are used in carrying out its primary editing, interpreting and supervisory functions, but which may also be used in executing a side program. The Central Processor does not, however, have instructions for multiplying and dividing since these instructions are not required in the editing and control routines which carry out its primary functions.

The Central Processor has the ability to set an "intervention" flip-flop in either Computer which will force the Computer to transfer control to a routine associated with the flip-flop. Normally, the transfer is programmed so that the Computer will automatically return after completing the routine to the point in its own program at which it was interrupted.

The Central Processor, although slower than the UNIVAC-LARC Computer, can perform in 16 microseconds an addition instruction which takes an operand from the storage, adds it to an operand in the accumulator register and returns the result to storage.

Basic Instruction Types

The majority of the Central Processor instructions are specialized instructions that are used to communicate with or control the error circuits, the input-output devices, the drums, the Synchronizers, and the Dispatcher. Most of these instructions are one of the three types listed below. Many can be addressed to any of several Synchronizers or other devices.

1. *Set Flip-Flop Instructions:* alert a Synchronizer or other device to perform a specific function such as connect or read 100 words.

2. *Transfer Instructions:* transfer control information between the Central Processor accumulator register and the Dispatcher or a Synchronizer. The control information might specify the mode in which a Synchronizer should operate or the first address of a storage area to which the Dispatcher should transfer data for a Synchronizer.

3. *Test Flip-Flop Instructions:* are actually conditional transfer instructions dependent on the state of the flip-flop tested. These instructions are used by the Central Processor to monitor and test the condition of a Synchronizer or other device ; for example, to test the availability of a Synchronizer or to test if a Synchronizer or other device has completed a previously ordered operation.

The above instructions are designed to provide the Central Processor with the ability to exercise flexible "real time" control over several operations being performed in parallel.

Instruction Word Format

A Central Processor instruction word contains 12 decimal digits.The format of an instruction word is shown in Figure 5 below.

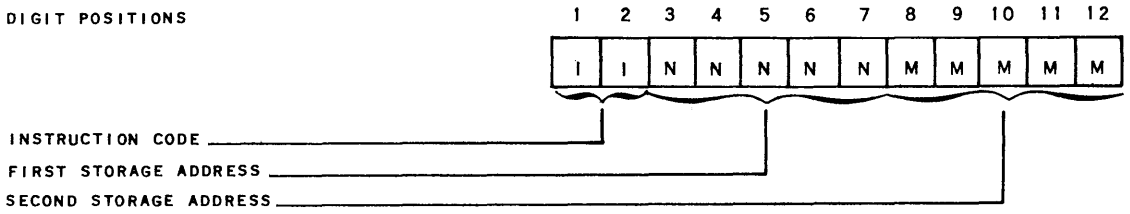


Figure 5. Processor Instruction Word Format

Instruction Code

Digit positions one and two of a Central Processor instruction word specify the operations to be executed by an instruction. An instruction code not in the Central Processor repertoireof instructions, when used, will cause the Central Processor to transfer control to an error routine.

First Storage Address

The first storage address, digit positions three through seven, specifies the storage address of an operand for single-operand-address instructions, or the storage address of the first operand for two-operand-address instructions. For other instructions, the first storage address of an instruction word is used to specify the number of shifts, (for shift instructions) or the address of a Synchronizer, storage drum, input-output unit, flip-flop circuit or display register.

Second Storage Address

Instruction word digit positions eight through 12 contain a second storage address. This address specifies the storage address for the result of an instruction, a second operand address for two-operand-address instructions, or a transfer-of-control address for transfer-of-control instructions.

TIME REFERENCE

The UNIVAC-LARC System is designed to change over to a new program without interruption. As computations are being performed on one problem, the next problem may be in the process of being loaded into the storage, while results from a previous problem are being printed. All of the above are made possible by the parallel operation of the various units of the system.

To aid in a changeover, a real-time reference is provided in the Central Processor. The timing reference may be used, for example, to determine when the time allotted for one program on the Computer is exhausted so that an automatic changeover may be made (without human intervention) to a new program. The timing source is a clock which continually alerts the Processor program to keep a running count of time. The Computer can order the Processor program to keep a check on the running time of a program and, after a specified period of time has passed, direct the Computer to a routine for effecting a changeover.

The Processor program may use the clock to time certain extra long logical operations, such as tape reversal operations on a tape unit or information displays on the operator console, thereby eliminating the need for costly fixed delay elements. Such a timing reference may be used for any number of other purposes; for example, to record the time at which errors or other events occur during the course of running programs. It is particularly useful in scheduling problems on the system and in solving problems in real time.

SYNCHRONIZERS

The Central Processor does not have time to control every step of the several input, output and drum operations being performed in parallel. Consequently, much of the detailed and specialized work of controlling these operations is performed by the Synchronizers.

A Synchronizer represents a modular grouping of logical circuits for controlling a particular reading or recording process. Its logical form is dependent to a great extent on the characteristics of the reading or recording device with which it is associated. Physically the Synchronizers are contained within the Processor cabinet. All of the Synchronizers of the expanded UNIVAC-LARC System may be housed within the cabinet.

FUNCTIONAL DESCRIPTION

The Synchronizers control the actual reading or recording process and the transition and the serial flow of information, digit by digit, between a buffer register and an input-output device or storage drum. In the process of transferring information, a Synchronizer may perform functions such as synchronizing input information with the internal timing of the system, checking and counting the information for errors, or translating the information in one way or another.

Whereas a single summary order from the Computer might call for the transfer of a block of several hundred or even thousands of words, a single instruction by the Central Processor alerts the Synchronizer to process a smaller block of words which is some increment of the block specified by the summary order. The Synchronizer is designed to process the smaller block automatically without direct intervention by the Central Processor. While one block of information is being processed, the Central Processor program may alert the Synchronizer to process the next block of information. The actual instruction that alerts the Synchronizer is executed by the Central Processor in four microseconds, whereas the operation initiated in the Synchronizer or other device by the instruction may take several milliseconds. In the meantime, the Central Processor is free to continue processing other summary orders.

COMMUNICATION WITH THE CENTRAL PROCESSOR

Whenever a Synchronizer, input-output device, or drum is ready to accept further instructions from the Central Processor program, it records this fact by setting a flip-flop. The Central Processor program determines whether or not a Synchronizer or other device requires attention by testing the flip-flop with a conditional transfer instruction. If it is set when tested, control is transferred to a routine which determines the action to take and instructs the device accordingly.

Rather than waste time testing each and every flip-flop to arrive at the specific flip-flop which is set, the Central Processor first performs a master test on all of the flip-flops and then a series of group tests. The testing is performed in an order of priority so that the flip-flops of the Synchronizers that require the most frequent attention are tested first. In general, the frequency at which a Synchronizer requires attention is a function of its data transfer rate. Consequently, the Drum Synchronizers which operate at the highest rate are tested first, then the Tape Synchronizers, and so on.

DISPATCHER

The Dispatcher is a central exchange which controls the transfer of data between the buffer registers of the Synchronizers and the main core storage. There are one to four one-word buffer registers for each Synchronizer. They are used to perform the serial-parallel conversions and to store data preparatory to transferring it to the main storage or to a drum or input-output device. Transfers between the buffer registers and the drums or input-output devices are controlled by the Synchronizers. The rate and order of flow is governed primarily by the characteristics of the particular device concerned.

Whenever a Synchronizer completes the processing and transfer of a word to or from a buffer register, it signals the Dispatcher to transfer the word to the main storage (if it is an input synchronizer) or to obtain a new word from storage (if it is an output synchronizer).

ERROR CHECKING

The Processor, like the Computer, contains extensive checking circuits designed to detect all single bit errors. An error in the Central Processor section of the Processor causes an immediate and automatic transfer of control to an error routine. The Central Processor has error test instructions which may be used in the error routine to determine the type and location of the failure.

Checking circuits in the Synchronizer section of the Processor indicate the type of error detected and the particular Synchronizer in which the error occured.

The checking circuits within the Processor are also designed to indicate whether an error originated within its own logical circuits or within the circuits of a storage or input-output unit.

Often, because of the use of solid-state circuitry, it is possible to exchange a faulty circuit with a reliable one with a minimum of time loss. The tape units, magnetic storage drums, and core storage units are all connected to the system through plugboards which simplify the substitution of one identical unit for another. These external devices are provided with test controls and other provisions for "off-line" testing which does not interrupt computing and processing.

Data Storage Systems

The UNIVAC-LARC System is equipped with both magnetic ferrite-core and magnetic drum storage systems, each of modular construction. In a completely expanded UNIVAC-LARC System, these data storage systems offer a combined data storage capacity of over 73 million decimal digits of information.

The magnetic ferrite-core storage of the UNIVAC-LARC is the main storage for both Computers, in an expanded system, and the Processor. It is the common link for Computer-Processor and Computer-Computer information exchange. The core storage system is also used as a flexible buffer storage for transferring data between the auxiliary storage (magnetic drum) and the input-output units.

The magnetic drum storage system serves as an auxiliary to the main core storage system. The drums are a low-cost, high-capacity repository for all data including input, intermediate processing results, output, and service routines.

MAGNETIC CORE STORAGE

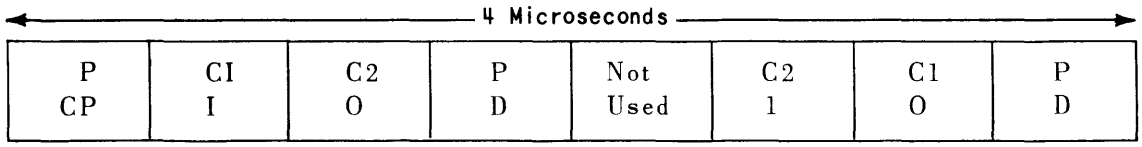
The core storage is divided into modular units each of which has a capacity of 2500 words of 12 decimal digits. Four storage units are contained in a cabinet. The storage units may be added to a system in units of four up to a maximum of 39 units (10 cabinets); the equivalent of 97,500 words. Each cabinet has its own power supply, clock-pulse generator, and heat exchangers. Because of a logical limitation on the number of storage addresses available for assignment, one cabinet in a completely expanded storage system of ten cabinets would contain only three 2500-word units.

Each storage unit contains the switching, timing, and amplifying circuits that are required for independent operation. The division of the storage into independent units permits simultaneous reference to storage: by the Computer, for obtaining instructions and for transferring operands; and by the Processor, for transfers involved in carrying out its program and for transferring data to or from the auxiliary storage or input-output. It also permits off-line maintenance to be performed on a single unit while the others are operating.

TIMING

A complete clear-write or read-regenerate cycle of the core storage actually takes approximately eight microseconds to complete. However, reading or clearing data from the cores may be overlapped and performed in parallel with the operations of selecting the cores and writing or regenerating the data. As a result, the storage cycle is, for all practical purposes, four microseconds. The allowable transfer rate to or from the storage is further increased by the fact that the storage units can operate independently and in parallel.

To keep interconnections within reasonable limits, the core storage units are connected to the Computers and the Processor by a transfer bus which is time shared to serve as the data transfer path to and from the storage for both the Computers and the Processor. The bus is time shared on the basis of a repetitive 4-microsecond time cycle which is broken down into eight ½-microsecond time intervals (time slots). During any time slot one word of data can be transmitted to the storage in parallel. The time slots are apportioned to the various connecting areas of the Computers and the Processor in the following order:



LEGEND:

P = Processor time slot.

CP = Central Processor; indicates the time slot on which the Central Processor section of the Processor transfers operands on instructions that are used in its program.

D = Dispatcher; indicates the time slots on which the Synchronizer Dispatcher section of the Processor transfers input-output or drum data for a Synchronizer.

C1 = Computer number 1.
C2 = Computer number 2.

I = Instruction; indicates the time slot on which a Computer obtains an instruction.

O = Operand; indicates the time slot on which a Computer transfers operands.

INTERLOCKS

The UNIVAC-LARC System is normally programmed to avoid simultaneous reference to the same storage unit by two or more sections of the system (the Computers, the Central Processor, or the Dispatcher).However, each storage unit is provided with interlocks to prevent conflicts and establish priorities. A storage unit is unavailable for four microseconds from the time it is addressed by a calling unit. During this time any other calling unit is prevented from gaining access to that storage unit.

Continual reference (once every four microseconds) to a storage unit by a Computer or the Central Processor could, if a system of priorities did not exist, lock out the Dispatcher indefinitely from access to the same storage unit. Because the Dispatcher must transfer data for the Synchronizers within a definite period of time in order to maintain a continual flow of input-output data, each storage unit is provided with a priority interlock which ensures access by the Dispatcher within four microseconds after it addresses the storage unit. Should the Dispatcher address a storage unit that is busy, the interlock prevents the Computers or the Central Processor from gaining access to that unit again until the Dispatcher has successfully completed its storage reference. Because the Central Processor must monitor within a definite period of time the real-time operations of the Synchronizers, it has the same type of storage priority over the Computers.

The Processor instruction repertoire contains write-interlock instructions to prevent either Computer from writing data into any designated storage unit. It also contains an instruction for removing the write interlock from any designated storage unit. These instructions are provided to prevent the accidental destruction by the Computer of data in the storage.

MAGNETIC DRUM STORAGE

Up to 24 magnetic drums may be included in a UNIVAC-LARC System. Each drum is capable of storing 250,000 words of 12 decimal digits. Up to three Read Synchronizer and two Write Synchronizer units can be added to the Processor for simultaneous control of as many as three reading and two writing operations on the drums concurrently with input-output operations. The Processor program can connect any drum to any Synchronizer. Two drums, operating alternately with a single Synchronizer, can transfer data at a continuous rate of 330,000 decimal digits per second.

The drum units are self-contained modules with individual test controls for off-line maintenance. They may be functionally interchanged by means of a plugboard.

PHYSICAL SPECIFICATIONS

Each drum is 27.6 inches long and 24.2 inches in diameter. The drum rotates at 880 rpm to attain a surface velocity of 1120 inches per second.

A complete 250,000 word drum is serviced by a single six-channel read-write head assembly which is held in a gimbal mounting and is floated on a thin film of air. The assembly is moved by the surface friction of the rotating drum. The "floating" head assembly enables the heads to record and read at a high density of 450 pulses per inch.

For protection against the effects of dirt and moisture, the drum,the head assembly, and the mechanism that positions the head assembly, are housed in an air-tight,dust-free enclosure. Largely due to the inherent simplicity of the floating head assembly, the drum storage is extremely reliable.

ORGANIZATION OF DATA

Each drum has 100 circumferential information bands. Each band is capable of storing 2500 computer words of 12 decimal digits; a capacity equal to that of one core storage unit. The bands are divided into 25 sectors of 100 words each, making it possible to begin reading or recording at any one of 25 access points around a band. One sector (100 words) is the smallest unit that can be read or recorded during any one reference to the drum.

A band consists of six tracks. The four information bits and parity check bit of a decimal digit are recorded in parallel on five of the tracks. Words and digits of a word are stored serially. The sixth track of a band is used to store serially a band number and an address for each sector.

Access to a particular band is gained by moving the single six-channel head assembly back or forth along the length of the drum. The six individual read-write heads are spaced in the head assembly at twice the track spacing on the drum. The six tracks of one band are always interspaced with the tracks of another. Two bands are interlaced by recording one band of an interlaced pair with the head assembly in one position and recording the other band of the pair with the head assembly shifted a distance equal to the track spacing. Interlacing the bands enables a high track density of 30 tracks to the inch to be achieved without the difficulties attendant in designing a head assembly with extremely close spacing between the individual heads.

The 100 bands of a drum are numbered in the following order:

00,99 01,98 02,96 . . . . . 47,52 48,51 49,50.

Where 00 and 99 are the numbers of the first pair of interlaced bands, 01 and 98 are the numbers of the next, and so on. To achieve minimum latency, data is normally organized in a systematic manner so that the processing of data begins at band 00 and proceeds through band 01, 02, 03, and so on. During each read or write operation, a complete band of data is processed after which the head assembly is stepped, in sequence, to the next band. After the data on band 49 is processed, the head assembly is shifted to band 50, the stepping mechanism is reversed, and the head assembly is stepped in the opposite direction through bands 51, 52, 53, etc. After a complete pass through the drum the head assembly is back to the starting point, thereby eliminating the equivalent of rewind time. Data can be organized on the drum in a less systematic manner and less than a full band can be read during each reference, although by so doing latency time would ordinarily be increased. The Computer can order the Processor to position the head assembly over any band and process any number of sectors from 1 to 25.

ACCESS TIME

Stepping the head assembly from one band of an interlaced pair to the equivalent band of the next pair requires 70 milliseconds. When the head assembly is continuously stepped without reading or writing, only 50 milliseconds are required for each step after the first. To reverse the direction of stepping requires 10 milliseconds. Shifting the head assembly from one band to the band with which it is interlaced requires 50 milliseconds. However, the shifting operation can be performed in parallel with a reversal.

Positioning of the head assembly is controlled by the Processor program which keeps a running account of the current position of the head assembly of each of the drums and moves the head assembly to any position ordered. The circuits in the Processor that control the head positioning are independent of the Drum Synchronizers. The head assembly on a drum can be positioned in parallel with a read or write operation being performed on any other drum.

A single summary order from the Computer can specify the transfer to or from sequential main storage locations of from one to 25 sectors of data on a band. If a complete band of 2500 words is to be transferred, reading or writing can begin as soon as one complete sector has been traversed with the drum connected to the Synchronizer. Therefore, from one to two sector intervals (from 2.7 to 5.4 milliseconds) may be required before access is obtained to a complete band. If a specific sector on a band is desired, up to a full drum revolution of latency time (68 milliseconds) may be required to gain access to it. However, any number of sectors on a band can be read or written during the time required for one drum revolution and one to two sector traversals.

The head assembly on any drum can be moved to the next band in sequence during the time required to read or write a band of data. By organizing the data in such a way that the reading and writing of bands alternate between two drums, the head movements can be executed in parallel with the reading and writing (while a band of data is being processed on one drum the head assembly on the other drum can be moved to the next band in the sequence). Using this technique, data can be transferred continuously at a rate of 2500 words every 83 milliseconds; the equivalent of 370,000 decimal digits per second. The 83 milliseconds required to transfer 2500 words includes:

1. The time required to pick up and interpret the summary order from the Computer.
2. The time required to connect the drum to the Synchronizer (assuming that the required drum and Synchronizer are available).
3. The time required to gain access to the first sector.
4. The time required to transfer the complete band of data to the main storage and notify the Computer of the completion of the transfer.

Input-Output Units

Input-output versatility of the UNIVAC-LARC System is gained through a variety of input-output units. To the basic UNIVAC-LARC System are added the required modular input-output devices to fit the individual needs of the user. The range between the basic and expanded UNIVAC-LARC Systems is sufficient to accomodate the immediate work load of the user and allow for future expansion as the work load increases.

The modular input-output units of the system include UNIVAC Uniservo II Magnetic Tape Units, UNIVAC High-Speed Printers, Punched-card Readers, and Electronic Page Recorders. Each provides a fast, distinct mode of input, output, or input/output.

MAGNETIC TAPE UNITS

High-speed input and output is provided in the UNIVAC-LARC System by Uniservo II Magnetic Tape Units. The tape units are used to introduce data into the system and to record output, either for long-term storage or for off-line conversion on an auxiliary device such as a High-Speed Printer.

COMPATIBILITY

Any magnetic tape prepared by the UNIVAC I and UNIVAC II System Central Computer or UNIVAC auxiliary equipment can be used by any UNIVAC-LARC magnetic tape unit. Conversely, any UNIVAC-LARC tape unit can prepare tapes for use by the UNIVAC I or UNIVAC II Central Computer or UNIVAC auxiliary equipment. Consequently, a fully compatible complement of off-line auxiliary equipment can be used with the UNIVAC-LARC System including the UNIVAC High-Speed Printer, Unityper II, Tape Verifier, Card-to-Tape Converter, Tape-to-Tape Converter, and Tape-to-Card Converter.

CONTROL

The UNIVAC-LARC System can accomodate up to 40 Uniservo II Tape Units. As many as four modular tape control units (Synchronizers) can be included in the Processor, each of which can control a reading or recording operation on any one of 10 tape units that can be connected to the Processor. Plugboards are provided which make it possible to substitute any tape unit for any other controlled by the same Synchronizer. The four Tape-Read-Write Synchronizers can perform in parallel with one another and in parallel with the Drum Synchronizers or other input-output Synchronizers in the system. While a reading or recording operation is being performed on one tape unit, the tapes on any one or all of the others can be rewinding.

CHECKING

A positioning checker can be provided as part of the Processor. The positioning checker may be connected by the Processor to any tape unit via its Synchronizer. It is used to perform a parity check and count of the characters recorded on tape or ensure that the recording was executed without error or to position a tape at a particular block of data, or to check-read and position the tape simultaneously. Although the positioning checker uses the read circuits of the Tape Synchronizer to which is connected, the same Synchronizer is free to control a concurrent write operation on another tape unit.

READ-WRITE SPECIFICATIONS

The tape units read or record on either plastic or metal tapes at a tape speed of 100 inches per second. Data is recorded at a density of 250 numeric or alpha-numeric characters to the inch for use on the UNIVAC-LARC or UNIVAC II Systems or at a lesser density for use on the UNIVAC I System or UNIVAC off-line auxiliary devices. Tapes having a wider range of pulse densities can be read, including tapes recorded by the Unityper I, at 20 pulses per inch. The length of a block of data on the tapes can be any multiple of ten 12-digit words. The Tape Synchronizers perform a parity check and count of the characters that are read or recorded in a 10-word block. The Processor program checks the number of 10-word blocks that are read or recorded. The tapes can be recorded in a forward direction or read in either a forward or backward direction. The data read from the tapes can be transferred to the main core storage or merely checked by the Processor program to locate a particular block of data or to ensure that the recorded data is reliable.

TAPE CODE TRANSLATION

Data recorded on tapes is in UNIVAC excess-three 7-bit code. Input and output data is translated by built-in translators. The Processor program can instruct the Tape Synchronizer to translate the UNIVAC 7-bit code that is read from the tape into either a 1-digit numeric or 2-digit alpha-numeric code that is used within the UNIVAC-LARC System. When output is being recorded on tape, the Synchronizer can be instructed to translate from either the 1-digit numeric or 2-digit alpha-numeric code to the UNIVAC 7-bit code.

READ-WRITE INTERLOCKS

A mechanical interlock is provided on each tape unit to prevent writing on a designated reel of tape. A rewind interlock is also provided on each tape unit which can be set at the discretion of the Processor program to prevent reading or writing on a rewound tape until the operator releases the tape unit from the interlocks.

A photoelectric cell on each tape unit detects unusable sections of tape indicated by holes punched through the center of the tape at intervals throughout the section. When an unusable section is detected, the reading or writing process is interrupted until the unusable section has passed the read-write heads. The tapes may be easily spliced and the spliced joint invalidated for reading or recording by punching spaced holes in the tape.

ACCESS TIME

Access time to the nearest block of data on the tape is 15 milliseconds. This includes the time required to connect the read-write heads and accelerate the tape. An additional 0.6 seconds is required if the tape direction is reversed. When a tape is in a rewound state 1.2 seconds is required to reach the first block of data on the tape.

ELECTRONIC PAGE RECORDER

For direct large-volume output of data in tabular or graphical form, an Electronic Page Recorder can be provided with the UNIVAC-LARC System. Output data may be represented by the Page Recorder in the form of a curve plot, a grid pattern, alpha-numeric characters, or a combination of all three, (a plotted curve with call-outs, titles, scales, grid patterns, etc.). The output is displayed on the face of a cathode ray rube and is recorded by means of a high-speed 35 mm camera controlled by the Processor program. For occasional monitoring of the output, a self-developing camera is provided.

OPERATING SPEEDS

The Page Recorder operates at an average character rate per film frame of approximately 15,000 characters per second. When used for graphing, it operates at average rates per frame of approximately 2,000 points per second or 1,000 grid lines per second. These output rates match internal Computer speeds and make it possible to produce a sufficient volume of timely and easily interpreted output data for efficient program debugging, program monitoring, or engineering and mathematical analysis.

CONTROL

Two identical, fast-interchange Page Recorders may be provided with the System. Each has a 35 mm and a self-developing camera. Both Recorders are controlled from a single Synchronizer in the Processor. Each is provided with an internal test program generator which may be used to simulate Processor instruction for purposes of off-line maintenance and adjustment. To achieve continuous output while the 35 mm camera film is advanced, data can be recorded alternately on the two printers. Should one Page Recorder become inoperative or exhaust its film supply, all of the output can be recorded on the other.

The shutter for the self-developing camera is controlled by the Processor program. The camera can produce either standard paper prints or positive transparencies that are suitable for projection and for easy overlay comparison of graphs. The operator can advance the film and develop a paper print in approximately one minute. A transparency may be developed in approximately two minutes.

MODES OF OPERATION

The format for recording numeric or alpha-numeric characters contains a maximum of 65 lines of 130 character positions each. Any one of 64 characters or symbols can be recorded. The Recorder Synchronizer can operate in either a numeric or alpha-numeric mode. In the numeric mode, a single digit in UNIVAC-LARC code is used to select a numeric character or one of five special symbols. In the alpha-numeric mode, two digits in UNIVAC-LARC code are used to select any one of 64 alpha-numeric characters or symbols. The Page Recorder Synchronizer can operate in an unedited mode, in which case all of the characters are recorded in a standard format, or in an edited mode, in which case the format is determined by digits within the output data itself.

Any one of the 64 characters or symbols can be selected by the Processor program for use in plotting a curve. The center of the plotting symbol can be directed to any position in a 1000 x 1000 mesh of discrete locations. The Recorder Synchronizer can operate in either of two plotting modes. In one mode, two sets of X and Y coordinates (2 points) are specified in a single word of output data. In the other plotting mode, X and Y coordinates are specified in two consecutive words of output data. The output data can be edited by a special routine in the Processor or Computer program. The Synchronizer can operate in two additional modes; one for plotting horizontal grid lines and the other for plotting vertical grid lines. In these two modes, a pair of abscissas or ordinates are specified in each output word for plotting respectively a vertical or horizontal grid line.

UNIVAC HIGH-SPEED PRINTER

Either one or two electro-mechanical High-Speed Printers and Printer Synchronizers can be connected into the System to produce direct, high-quality, multiple-copy records or results. The Printer can record either numeric or alpha-numeric data in a standard or a completely edited format. The paper can be fed in steps for single-line spacing or fast-fed for multiple-line spacing. The paper feed accepts paper from 4½ to 21 inches in width. The Printer has the following characteristics:

Printable characters	51
Lines per minute	600
Characters per line	120
Character positions per line	130
Characters per minute (maximum)	72,000
Characters per inch	10
Lines per inch	6

HIGH-SPEED CARD READER

An on-line, High-Speed Card Reader and a Card Reader Synchronizer can be provided as part of the UNIVAC-LARC System. Readers are available for processing 80 column punched-cards at speeds of up to 450 cards per minute.

Control Consoles

Two types of control consoles are provided with the UNIVAC-LARC System. One is the Operator Control Console; the other is the Engineer Control Console.

OPERATOR CONTROL CONSOLE

In a UNIVAC-LARC System containing one Computer, a single Operator Console is used to exercise complete operational control over both the Computer and the Processor. In a UNIVAC-LARC System containing two Computers, two identical Operator Consoles are used, one for each Computer. When separate problems are being run on the two Computers, the operators at both Consoles can communicate with and exercise control over the Processor without in any way interfering with one another.

KEYBOARD AND DISPLAY REGISTERS

A numeric keyboard is provided on each Operator Control Console. The keyboard is used to enter data into either a five-digit or 12-digit general-purpose display register in the Computer. The contents of both registers are displayed in decimal form on the Operator Control Console Panel. Both the Computer and Processor have access to the display registers by way of their accumulator registers and may be instructed to display data in the registers or pick up data entered into the registers from the keyboard. To prevent conflicts between the Computer and Processor in the use of the display registers, all displays are normally handled by the Processor program which times the duration of the display using the real time reference.

CONTROL PANEL

Operator direction of the Computer and Processor is exercised chiefly by means of manual intervention buttons provided on the control panel. There are five such buttons on each panel for the Computer and five for the Processor. Pressing a Computer manual intervention button causes the Computer to transfer control to a routine associated with the button. If necessary, provisions are made in the routine for re-entry into the main program when the routine is completed.

Although only five manual intervention buttons are provided for the Computer, the number of routines to which the operator may direct the Computer is not necessarily limited to five. For example, the data picked up from a display register may be interpreted by a manual intervention routine in such a way as to direct the Computer to any number of subroutines.

Pressing a Processor manual intervention button causes a transfer of control in the Processor to a routine associated with the button. Instead of forcing an immediate transfer, however, the button alerts the Processor to transfer control at the discretion of its program. The actual transfer may not be made immediately but may be delayed until the Processor has reached a point in its program at which it may enter the routine without interfering with other concurrent operations.

TYPEWRITER - PRINTER

An alpha-numeric Typewriter-Printer is provided on each Operator Control Console. The Printer is controlled through a Synchronizer in the Processor. It is used by the Processor program, or by the Computer program indirectly by way of summary order to the Processor program, to communicate with the operator. A print-out might consist of data relative to errors or contingencies that occur in a program or instructions to the operator, such as instructions for mounting tapes for a forthcoming program.

PAPER TAPE READER

A Paper Tape Reader is provided with the Printer on each Operator Control Console. It is used primarily during a start-up procedure as a fast means of initially loading the first part of the Processor program into main storage. When used for this purpose, data is read from the tape for transmittal to the main storage via the display registers. After sufficient data has been transferred into storage from the paper tape, the Processor program completes the loading from magnetic tape. The Paper Tape Reader may also be used to relieve the operator from typing data into the display registers from the keyboard while a problem is being run or as an optional method of loading data into the storage for the Computer. The Printer is also provided with a paper tape punch which may be used by the operator or the program to prepare punched paper tapes for the Reader.

ENGINEER CONTROL CONSOLE

The Engineer Control Console is physically separate from the Operator Control Console or Consoles. It contains an engineer control panel for the Processor and a separate panel for each Computer in the system. All of the controls and indicators on the Operator Control Console, including an operator control panel, a numeric keyboard, and an alpha-numeric printer with an associated paper tape punch and reader, are duplicated on the Engineer Control Console.

In a system containing two Computers, either one or two sets of operator controls and indicators can be provided. Should one set be provided, it can be manually connected to either Computer. A single Console Printer Synchronizer is provided in the Processor which can be connected by the Processor program to any of the four console printers in an expanded system. Normally, error analysis information and the like is routed to a printer at the Engineer Control Console and data on contingencies, instructions to the operator, and so forth are routed to the printer at the Operator Control Console.

COMPUTER CONTROL PANEL

The Computer Control Panel on the Engineer Control Console contains 60 neon lights which display *in binary form* the contents of the Computer 12-digit display register. Switches are provided on the engineer panel to operate the display register in either of three following modes:

Manual Display Mode: In the manual display mode, the engineer can set controls to select and sample data at various points within the Computer and transfer the data to the 12-digit display register where it can be observed in binary form on the panel. Data can be sampled at a specific pulse time and step of an instruction that is being executed. It may be obtained for display from the various registers within the arithmetic and control sections of the Computer, from the various data transfer paths including the main storage bus, and from various combinations of flip-flops.

Program Display Mode: In the program display mode, the engineer can select data for sampling at specific times and from specific points as in the manual display mode. However, the display will only be effected for instructions that are tagged with a "one" digit in the most significant digit position of the instruction word.

Fast Register Display Mode: In the fast register display mode, the engineer can select for display the contents of any of the fast registers within the Computer.

The display registers may also be used by the engineer, in conjunction with a type-in from the keyboard, to enter data into the main instruction register of the Computer, enter data into any main storage location, or display data from any storage location.

In addition to those associated with the display registers, the following controls and indicators are included on the Computer Control Panel:

1. Error and contingency indicator lights that indicate any error or contingency condition detected by the checking circuits of the Computer. The error indicator lights indicate the type of error detected and, for certain types of errors, the digit position at which the error occurred. An error option switch is provided on the panel. The switch has three positions labeled STOP, NORMAL, and IGNORE. When the switch is in the STOP position, the Computer stops if an error is detected. When the switch is in the NORMAL position, the Computer enters an error routine if an error is detected. When the switch is in the IGNORE position, the Computer ignores any error detected. A reset button is also provided with which the engineer may reset the error flip-flops. A similar contingency option switch and a reset button are provided on the panel for controlling contingency conditions.

2. Two neon pushbuttons are provided on the panel to control the gating in of various control signals that the engineer can manually introduce into the Computer for troubleshooting purposes by connecting signal input lines to terminals in the circuits.

3. A switch abnormal light which is lit if any switch on the Computer Control Panel is set in a position to interfere with the running of a normal program or to allow errors to go undetected.

4. A transfer switch which the engineer may use to force the Computer to either transfer control or not transfer control on conditional transfer of control instructions.

5. Buttons for clearing the Computer as a whole or selected parts of the Computer.

6. Retain buttons which can be used to retain the contents of the main instruction register, the control counter, or a fast register.

PROCESSOR CONTROL PANEL

The controls and indicators on the Processor Control Panel on the Engineer Control Console include:

1. Illuminated master power control buttons for applying power to the various units of the system. A set of 24 pushbuttons is provided to select the drums that are to be turned on. When the master drum-power control button is pressed, the selected drums are turned on in sequence.

2. Air-flow, power failure, and temperature indicators for the Processor, the Computers, each type of input-output device, and each main storage cabinet.

3. Start and stop pushbuttons.

4. Illuminated pushbuttons to control the mode in which the Processor operates. The Processor can operate in a continuous, one instruction, one step, arithmetic test stop, or input-output test stop mode or any of five breakpoint stop modes. With the test stop pushbuttons, the Processor can be made to stop on conditional transfer of control instructions (arithmetic tests, input-output tests, or breakpoint tests) and indicate whether a transfer of control is imminent. When the Processor stops, the engineer has the option of forcing the Processor to transfer control or forcing it to continue on the same sequence of instructions.

5. Clear buttons for clearing the Processor as a whole or selected parts of the Processor.

6. Retain buttons to prevent changing the contents of certain registers within the Processor.

7. Error indicators to display errors detected within the Central Processor, Dispatcher, and each of the Synchronizers. Separate error option switches are provided for the Central Processor and each of the Synchronizers.

8. A switch abnormal light which is lit if any switch on the Processor panel is set in a position to interfere with the running of a normal program or to allow errors to go undetected.

9. A master error-set pushbutton to set all of the Processor error flip-flops for the purpose of testing the error flip-flops and the indicators on the panel.

10. A gain control switch for each Tape Synchronizer enables the engineer to manually set the tape amplifier gain control of a Tape Synchronizer to high or low gain, or have the gain setting determined by the Processor program.

11. A sector-address write switch used in conjunction with a special Processor program to lay out the data bands on the magnetic drums when the drums are first installed into the system. If a bad spot (unusable recording area) should develop on a drum after it is installed, one or more bands can be repositioned so that the bad spot will lie in an area that is not used for recording.

12. A memory simulator consisting of a set of 60 switches used to manually insert a word of data into the Processor. A word set up on the switches can be directed to the main instruction register, the arithmetic registers and to the Synchronizer buffer registers.

13. Switches to run each of the Synchronizers.

14. A binary display of the main instruction register and various other registers, counters, and control flip-flops in the Processor.

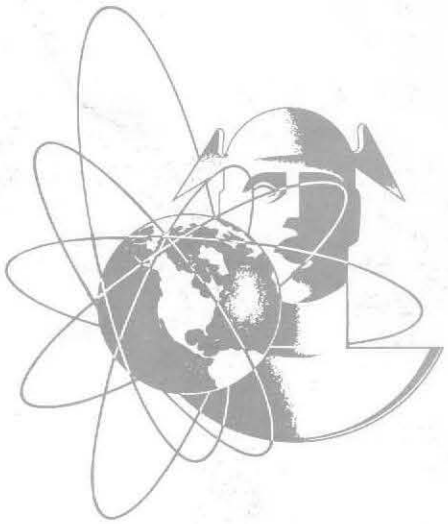
15. Display register controls which can be used to transfer the contents of the main Processor instruction register or either arithmetic register to a Computer display register for visual inspection, or to transfer the contents of a display register to the instruction and arithmetic registers. Data can be manually entered into the display register from the keyboard.

16. A type-out button which causes a type-out on a selected console printer of the contents of the Processor arithmetic registers.

17. A jam-signal button which is used to control the gating-in of various control signals that may be manually introduced into the Processor logical circuits for trouble shooting purposes.

18. An audio monitor that can be connected to either Computer or to the Processor. By changing pitch the audio signal gives an indication of the frequency of instruction execution.

19. A film monitor to indicate the status of the film in the 35-mm and self-developing cameras of the Electronic Page Recorder.



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