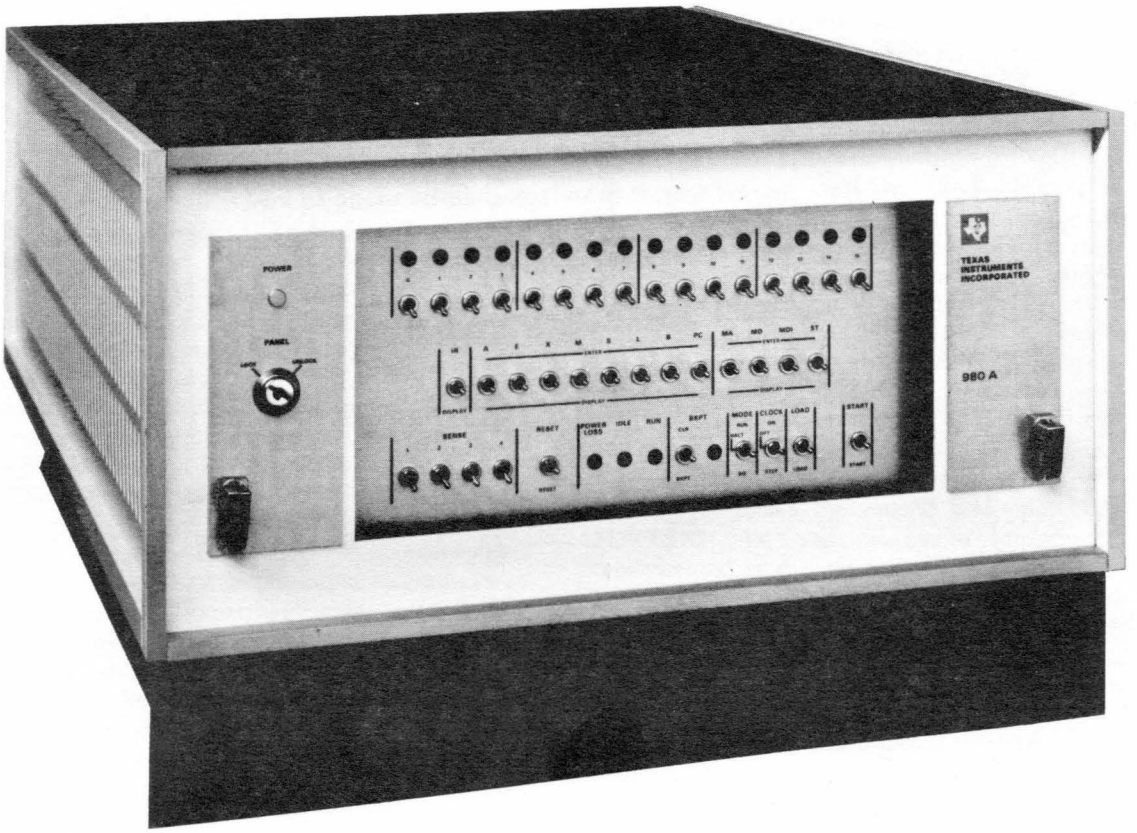
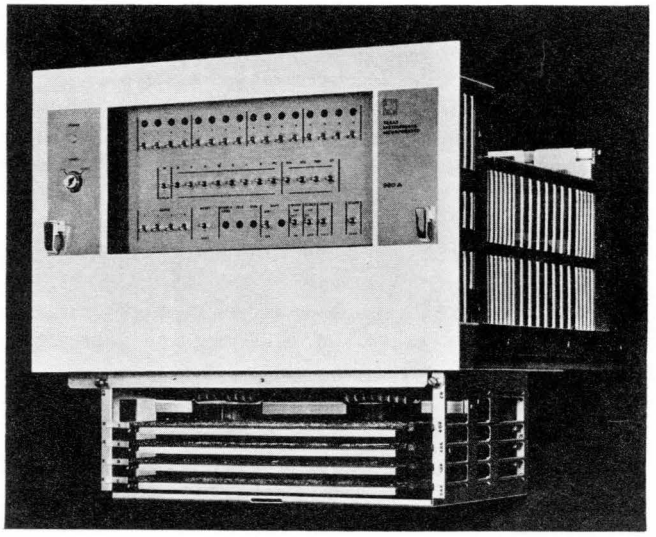
Texas Instruments
Model 980A Computer

System Characteristics





980A Processor
(Extended memory chassis front panel removed for viewing)

OVERVIEW

The latest in the 900 series of digital processors from Texas Instruments is the 980A general purpose computer. The 980A is designed not only to meet today's systems needs but the future's increased operating speeds and requirements. With performance characteristics exceeding those of many larger and higher-priced computers, the 980A is a fast and powerful 16-bit computer at a low unit price which includes an extensive list of hardware and software features, built-in and standard. By optimizing the use of hardware components common with the 960A industrial control computer, TI is able to provide the 980A general purpose computer at the cost of most stripped-down competitive models. Both computers are backed by TI's worldwide sales and service organizations.

The 980A is a general purpose arithmetic machine with many of the features incorporated as standard items which are usually considered as options or accessories to this class of computer. Bootstrap loader, multiply and divide, programmable memory protection, and power fail detection and auto restart are some of the hardware features included in the basic selling price. Combining these characteristics with an effective, I/O oriented executive-type monitor, establishes the 980A as a dramatically low-cost, high-performance general purpose processor.

The 980A uses MOS semiconductor memory elements. Up to 65K words can be directly addressed by the CPU. Sockets are provided and fully wired so that memory is field expandable in modules of 4K or 8K words up to 32K words directly within the CPU. Standard with the CPU is a power supply designed to support up to 65K words of memory. An additional 32K words of memory can be easily added to the system, external to the 32K basic CPU. Basic memory cycle time is 750 nanoseconds while instruction decode and control microsequencing executes in 250 nanoseconds. As the technology of manufacturing faster semiconductor memories is developed, these new products will be incorporated in the computer reducing the obsolesence factor and increasing its potential usefulness to the end user.

An optional, plug-in battery pack is available for the 980A which makes the semiconductor memory non-volatile. When a primary ac power failure occurs, it is detected immediately and the battery supply is switched to the memory, sustaining the memory's data contents. During power-down conditions, the battery is capable of maintaining 8K words of memory for four weeks at room temperature.

Although the 980A is a general purpose, I/O Bus structured computer, it shares many characteristics of the Model 960A computer. Where the 960A is designed primarily for interfacing with the control of external devices by efficient bit manipulation, the 980A incorporates hardware features and software support to allow bit/byte/word/or byte string manipulation. The difference between the two computers is established by the problems each is intended to solve. The 960A provides a cost-effective mechanism by virtue of its dual processor architecture and the Communications Register Unit (CRU) for interfacing and operating other machinery as a system. The 980A combines the arithmetic features, speed, and flexibility to provide a profitable solution to the class of jobs involving data processing and manipulation. TI supports both computers in a hierarchial and distributive multiprocessor configuration where this problem/solution differentiation is required. Provisions have been made in the 980A to extend this interface to special function hardware such as floating point arithmetic or special transforms by including an Auxiliary Processor Port in the CPU and implementing it with its own activation instruction.

To minimize the general user's programming costs, FORTRAN IV and a macro processor are fully implemented in the 980A. System Executives, available in both disc-resident and non-disc versions, allow rapid program generation as well as compile and execute capabilities. Programmable memory protect, used in conjunction with a privileged class of instructions accessible only to the System Executive, provides an operating environment which is unaffected by programmer errors.

Configuration Guide

The 980A is modular and can be configured in minimum form as a processor with 4K words of memory, a teletype for input/output, and three additional I/O ports for additional device controllers. A single 980A will support 65K words of random access semiconductor memory, up to

eight high-speed device controllers such as discs, magnetic tape units, and line printers on a direct memory access channel (DMAC), and up to 256 I/O Bus devices.

Both serial and parallel universal type interfaces are available for special or custom devices communicating via the I/O Bus. Four I/O ports with decoded interrupt, one DMAC port and one Auxiliary Processor port are implemented in the basic CPU. Any port may be expanded into multiple ports within the mainframe or in an external chassis. For example, the I/O Bus may be expanded internally to accommodate 13 device controllers with the addition of a connector plate and three special bus expander logic printed circuit boards. The same expander cards are used each time the I/O Bus is extended. The mainframe power supply is designed to provide all required operating voltages and currents for the CPU with the full 65K memory, any desired internal expansion feature, and also provide the user with regulated +5 Vdc power source for external use.

When external expansion of either DMAC or the I/O Bus is required, an independent chassis is available complete with power supplies. Each chassis may be factory wired to accommodate combinations of different device controllers, or unwired allowing custom wire-wrap interconnects. A maximum of 56 80-pin sockets can be mounted in each chassis.

Compatibility

The earlier generation, general purpose Model 980 is upward program-compatible with the new, Model 980A. The 980A has some instructions not in the 980's instruction set, thus software developed for the 980 will run on the 980A. The 980A is not program compatible with the 960A, but they are data compatible and use many of the same peripheral devices. A disc or magnetic tape may be recorded on one computer and read on another. DMAC controllers as well as devices are physically interchangeable. Both the 980A and 960A use some common hardware in the mainframe to the extent that power supplies and semiconductor memory modules may be interchanged.

A Cross-Assembler for the 960A is available for use on the 980A as well as a 360 Cross-Assembler for off-line assembly of 980A programs.

MAINFRAME

Architecture

The 980A is basically a 16-bit word oriented computer. The instruction set, however, allows direct manipulation of data in the form of bits, words or strings of bytes or words. Arithmetic operations can be performed in single-word or double-word precision. Hardware multiply and divide has been incorporated as a standard feature in the 980A central processor.

The 980A is designed for general purpose computer applications. Programmable memory protect has been incorporated allowing upper and lower limit boundaries to be established by the operating system. Privileged instructions have been implemented in the 980A so that the system supervisor is protected from interference by user programs and user programs are protected from each other. Attempts by users to access protected memory or change status are flagged as system violations and generate an internal interrupt.

Central Processor

The basic 980A processor is available from 4K to 65K of semiconductor memory in increments of 4K. Memory modules are available in either 4K or 8K configurations. The CPU can directly address memory to a maximum of 65K words. The CPU mainframe is wired to house 32K words internally with the remaining portion of incorporated memory housed in an external chassis; power for the external memory chassis is derived from the basic CPU.

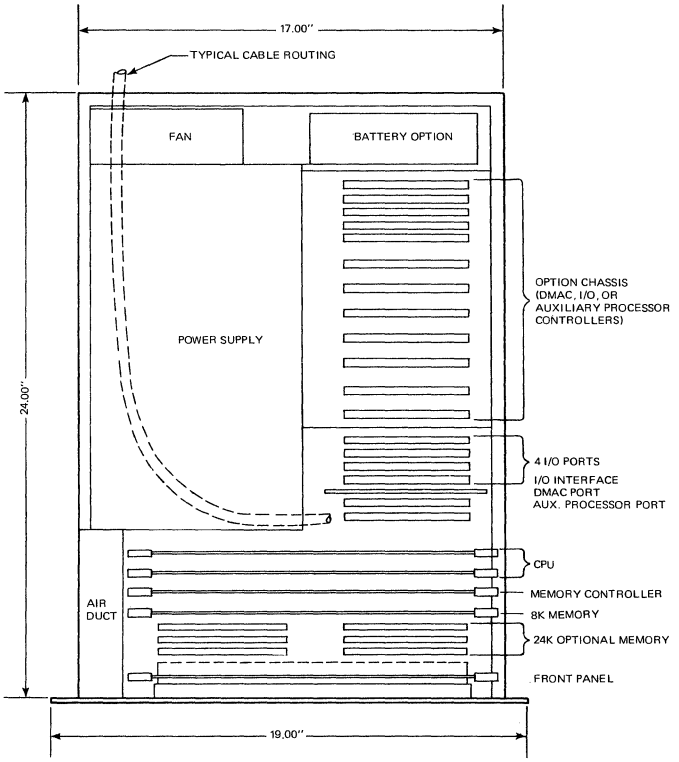
All processors include memory parity, programmable memory protect, privileged instructions, hardware program relocation, failure interrupt (auto restart with battery option), ROM bootstrap loader, multiply and divide, a control panel with key lock, one Auxiliary Processor (AP) port, one DMAC port, four I/O Bus ports with expanded interrupt, power supply, and rackmount chassis with slides.

A rear-mounted fan provides air circulation through the power supply and internal printed circuit boards. External cabling to the CPU is routed via cableways mounted over the fan assembly. Power and ground interconnections throughout the chassis are made via mother boards; signal interconnections are wire-wrap terminations. Space is available in the mainframe to mount an optional battery pack and a 12-connector internal expansion backplate. The battery provides refresh power to the semiconductor memory in the event of primary power failure. The internal expansion chassis is supplied unwired, wired for I/O Bus expansion, or wired for the inclusion of particular DMAC controllers or DMAC port expansion.

Table 1 lists the general characteristics of the 980A central processor, and Table 2 defines the operating and environmental specifications. Table 3 lists the physical characteristics.

Data Structure

Both data and instruction words in the 980A are 16 bits. Negative numbers are represented in the TWO's complement form with the most significant bit indicating the word sign. The range of integers represented in one



BASIC MODEL 980A MAINFRAME WITH OPTIONAL EXPANSION CHASSIS INSTALLED

980A Mechanical Configurations

16-bit word is from -2^{15} to $+2^{15}-1$. Basic arithmetic instructions use one-word operands; however, the extended instruction set provides some double-precision (2-word) arithmetic operations. Basic machine instructions may be one, two, or three words long. The operands for floating-point arithmetic subroutines consist of two words, 8-bit exponent and 24-bit mantissa, or three words with an 8-bit exponent and 32-bit mantissa.

Registers

The 980A incorporates eight directly addressable 16-bit registers. These registers with their normal functions and designations are as follows:

Register Number	Designation	Function
0	A	Primary Arithmetic Register
1	E	Secondary (extension) Arithmetic Register
2	X	Index Register
3	M	Maintenance Register
4	S	Storage Register
5	L	Link Register
6	B	Base Register
7	P	Program Counter

The processor status is contained in an additional 16-bit register identified as the Status Register. The Status Register is directly addressable under program control and together with the program counter constitutes the status block. The following status or control bits are indicated by the Status Register:

Bit	Function
0-1	Comparison indicators showing result of last magnitude comparison
2	Overflow indicator
3	Carry indicator showing arithmetic operation which resulted in overflow into sign bit
4	Enable/Disable Memory Protect
5	Memory Protect address violation
6	Privileged Instruction violation
7	Enable/disable I/O Bus interrupt
8	Enable/disable expanded interrupt
9	Enable/disable privileged instruction lower limit address bias
10	Pre/post index control
11	Enable/disable memory parity error interrupt
12	Enable/disable DMAC interrupt
14	Memory parity error indicator flag
15	Power failure indicator showing primary ac power failure is imminent.

Addressing

The 980A computer incorporates a Memory Protect/Privileged Instruction Feature (MP/PIF) for systems programming which prevents a user program from:

Changing the memory protection boundary address
Bring the computer to an idle
Branching into or accessing data in protected memory
Changing Status Register
Interfacing with system I/O operations.

The MP/PIF is controlled by two Status Register bits. When bit 4 is set (MP/PIF enabled), any attempt to address protected memory or use privileged instructions causes a system interrupt. Protected memory is defined by two Hardware Limit Registers implemented in the memory controller. Both upper and lower limit address registers are loaded under program control with the standard I/O instruction.

When Status Register bit 9 is set, the lower limit address bias is enabled and all subsequent memory accesses are dynamically biased by the current value in the lower limit address register. User programs are relocated automatically and executed as though they had never been moved. The two modes of MP/PIF operation can be used together or independently providing a powerful tool for the systems programmer.

Table 1. 980A Processor Characteristics

Characteristic	Description
Memory	
Type	MOS semiconductor
Word length	16 bits + parity
Cycle time/word	750 nanoseconds
Refresh rate	Every 67 microseconds (maximum memory speed reduced 1.2%)
Capacity (words)	
Minimum	4,096
Maximum	65,537
Increment size	4,096
Memory Protect	High and low address boundary protect alterable by System Executive.
ROM	Bootstrap loaders for 8 devices standard, switch initiated
Central Processor	
Number of working registers	8
Special register	Status - establishes working environment in CPU
Number of instructions	98
Fixed point arithmetic (TWO's complement)	Hardware
Add time (μsec)	1.75 (register to memory) 0.75 (immediate)
Multiply time (μsec)	6.25 (register to memory) 5.25 (immediate)
Divide time (μsec)	7.75 (register to memory) 6.75 (immediate)
Floating point arithmetic	Subroutine (hardware available 4th quarter 1972)
Addressing	15 modes including Immediate, Absolute, Index, Indirect, Displacement, and PC and Base Relative.
Special features	Direct address to bit level Privileged Instructions preventing branching into protected memory, halting CPU, changing status, or performing I/O.
Maximum number of I/O device controllers	256
Maximum number of DMAC device controllers	8 std. (64 max.)
Priority Interrupt System	
Levels	4, hardware, expandable to 64
I/O Channels	
Auxiliary Processor	1 port implemented
DMAC	1 port implemented, expandable to 8
I/O Bus	4 ports with interrupt bits implemented, expandable to 256.
Transfer rate (words/sec)	
DMAC	1M (device limited)
I/O Bus	130K
Microsequenced CPU control (ROM)	250-nanosecond cycle time

Table 2. 980A Operational And Environmental Specifications

Specification	Description
Temperature	
Operating	0°C to 50°C at sea level (derate upper limit 4°C for 50-Hz operation
Storage	-40°C to 70°C
Shock	
Operating	1G
Shipping	15G's to shipping container
Humidity	
Operating	0 to 95% RH
Storage	0 to 95% RH (non-condensing)
Altitude	0 to 10,000 feet (derate upper operating temperature limit 2°C/2500 ft)
Reliability	The calculated mean time between failure (MTBF) for the 980A with 4K words memory is 4000 hours. Calculations are based on MIL-HB-217A and represent a worst case number. Neither the confidence level or individual component failure rates have been adjusted to comprehend reduced interconnection failures due to multilayer PC board utilization, or the increased component reliability achieved by total system burn-in at maximum operation temperature for one week. These two mechanisms significantly increase the actual reliability. The established design goal for mean time to repair (MTTR) at the PC board replacement level is less than 10 minues.
AC line noise immunity	Dual, computer grade L-C line filters incorporated in each CPU power supply. Provides broad band noise suppression. Rejection specification dependent on noise characteristics.
Power failure detection	Standard power supply feature
Auto restart from power down	Incorporated in CPU but requires memory protect battery option to function

The following addressing modes are also available:

Hardware Addressing Modes	Instruction Length In Words
Immediate 8-bit	1
Immediate 16-bit	2
Immediate 32-bit	3
16-bit absolute address	2
16-bit absolute address ±15-bit index	2
Program counter ±7-bit displacement	1
Program counter ±15-bit index	1
Program counter ±7-bit displacement ±15-bit index	1
(Program counter ±7-bit displacement) indirect	1
(Program counter ±7-bit displacement ±15-bit index) indirect	1
(Program counter ±7-bit displacement) indirect ±15-bit index	1
Base register + 8-bit displacement	1
(Base register + 8-bit displacement) indirect	1
Base register + 8-bit displacement ±15-bit index	1
Each memory bit is directly addressable	

Table 3. 980A Physical Characteristics

Component	Part Number	Input Power	Power Available	Weight (lbs)	Shipping Weight (lbs)	Physical Size (inches)
980A CPU (8K memory)	960705-2	115Vac±10%,47-63Hz,450 watts max. (32K)		80	120	12-1/4Hx19Wx24D Shipping Container: 23Hx31Wx36D
External I/O or DMAC expansion chassis	216150-1	115Vac±10%,47-63Hz, 300 watts max.		70	100	10-1/4x19Wx24D
External memory expansion chassis	960707-2			15	25	5-1/4Hx19Wx10D (mechanically coupled to CPU)
Control panel*	960740					
CPU control (AU1)*	960754	+5V, 14A			8 (typ.)	Full size CPU PC boards
CPU control (AU2)*	960751				8 (typ.)	Full size CPU PC boards
Memory Controller*	960748	+5V, 4A			8 (typ.)	Full size CPU PC boards
8K-word Memory Module	226844-4	+5V, 1.5A			8 (typ.)	Full size CPU PC boards
I/O Interface card	960759	+5V, 0.5A			5 (typ.)	Single/Dbl Ended I/O PC boards
EIA Communication Module (half-dup)	217539		RS-232B		5 (typ.)	Single/Dbl Ended I/O PC boards
Digital I/O Module (16 In/Out)	961648-1		+5Vdc, 1A		5 (typ.)	Single/Dbl Ended I/O PC boards
DMAC Interface card	226772-1				5 (typ.)	Single/Dbl Ended I/O PC boards
Fixed Head Disc DMAC Controller	961751-17	+5V, 5A			12 (typ.)	
Moving Head Disc DMAC Controller	961752-1	+5V, 8A			12 (typ.)	
Line Printer DMAC Controller	217065-2	+5V, 1A			10 (typ.)	
Mag Tape DMAC Controller	217536-2	+5V, 6A			12 (typ.)	

Note: All weights are approximate and are dependent on PC board compliment.

*Included in basic CPU

Base relative addressing does not increase instruction execution time. Indexing increases execution time 250 nanoseconds, and indirect addressing adds 750 nanoseconds to the basic cycle time.

Machine Instructions.

Table 4 describes standard machine instructions grouped by instruction class as opposed to instruction function. Within any group, the descriptions are given in alphabetical order according to the mnemonic used by the programmer when coding in assembly language. These condensed instruction descriptions do not include conditions of overflow and carry indicators or format details. Machine execution times (in microseconds) are associated with each instruction.

Table 4. 980A Instruction Set

Register-Memory Instructions		Memory Referencing	Immediate Addressing
ADD	Add effective operand to contents of A register and leave sum in A register.	1.75	0.75
AND	Logically AND effective operand with contents of A register and leave result in A register.	1.75	0.75
BIX	Add one to X register and leave result in X register. BRANCH IF INCREMENTED INDEX is non-zero to effective address; otherwise, continue.	1.25	1.25
BRL	Load Link Register with contents of program counter, branch to effective address, and continue.	1.50	1.50
BRU	Branch unconditionally to effective address and continue.	1.25	1.00
CPA	Compare algebraically effective operand with A register.	1.75	0.75
CPL	Compare logically (16-bit unsigned number) effective operand with A register.	1.75	0.75
DAD	Add double-length operand in effective address and effective address plus one to the combined A and E registers.	2.75	1.0
DIV	Divide combined A and E registers by effective operand and leave quotient in A and remainder in E.	2.75 → 7.75	1.50 → 6.75
DLD	Load combined A and E registers with contents of effective address and effective address plus one.	2.75	1.0
DMT	Decrement operand by one; if zero, skip next instruction.	2.75	1.0
DSB	Subtract double-length effective operand from combined A and E registers.	2.75	1.0
DST	Store combined A and E registers in effective address and effective address plus one.	2.75	2.75
IMO	Increment effective operand by one.	2.75	2.75
IOR	Logically inclusive OR effective operand with A register, and leave results in A register.	1.75	0.75
LDA	Load register A with effective operand.	1.75	0.75
LDE	Load register E with effective operand.	1.75	0.75
LDM	Load register M with effective operand.	1.75	0.75

Table 4. 980A Instruction Set (Continued)

Register-Memory Instructions		Memory Referencing	Immediate Addressing
LDX	Load register X with effective operand.	1.75	0.75
MPY	Multiply effective operand by A register, and leave result in combined A and E registers.	2.25 → 6.25	1.25 → 5.25
STA	Store register A in effective address.	2.00	2.0
STE	Store register E in effective address.	2.00	2.0
STX	Store register X in effective address.	2.00	2.0
SUB	Subtract effective operand from A register and leave result in A register.	1.75	0.75

Register Shift Instructions		Execution Time
ALA	Shift A register left the number of bit positions indicated by immediate operand, and fill vacated bits with zeros.	All shift $0.75+\frac{\text{shift count}}{4}$
ALD	Shift combined A and E registers left the number of bits indicated by immediate operand, and fill vacated bits with zeros. (Omit register E bit 0 from the shift, and force the bit to agree with register A bit 0.)	
ARA	Shift A register right the number of bit positions indicated by immediate operand, and fill vacated bits with the sign bit.	
ARD	Shift combined A and E registers right the number of bits indicated by immediate operand, and fill vacated bits with the register A sign bit. (Omit register E bit 0 from the shift, and force it to agree with bit 0 of the A register.)	
CLD	Circularly left shift combined A and E registers the number of bits specified by immediate operand.	
CRA CRB CRE CRL CRM CRS CRX	Circularly right shift contents of the A,B,E,L,M,S, or X register by the number of bits specified by immediate operand.	
CRD	Circularly right shift combined A and E registers the number of bits specified by immediate operand.	
LLA	Logically left shift A register the number of bits specified by immediate operand, and fill vacated bits with zeros. (Differs from ALA by indicators set.)	
LLD	Logically left shift combined A and E registers the number of bits specified by immediate operand, and fill vacated bits with zeros.	
LRA	Logically right shift A register the number of bits specified by immediate operand, and fill vacated bits with zeros.	

Table 4. 980A Instruction Set (Continued)

Register Shift Instructions		Execution Time
LTO	Logically left shift A register per operand. If bit 0=1 during shift, store number shifted in X register.	All shift $1.0 + \frac{\text{shift count}}{4}$
LTZ	Logically left shift A register per operand. If bit 0=0 during shift, store number shifted in X register.	
RTO	Logically right shift A register per operand. If bit 15=1, set bit to 0 and store number shifted in X register.	
RTZ	Logically right shift A register per operand. If bit 15=0, set to 1 and store number shifted in X register.	

Register to Register Instructions		Execution Time
SR=Source Register	DR=Destination Register	1.25
RAD	Add the contents of SR to DR.	1.25
RAN	Logically AND SR to DR.	1.25
RCA	Algebraically compare SR to DR.	1.25
RCL	Logically compare SR to DR.	1.25
RCO	Replace DR with the TWO's complement of SR.	1.00
RDE	Subtract one from SR and place results in DR.	1.00
REO	Exclusive OR SR to DR.	1.25
REX	Exchange SR and DR.	1.50
RIN	Add one to SR and place result in DR.	1.00
RIV	Place ONE's complement of SR in DR.	1.00
RMO	Move SR to DR.	1.00
ROR	Logically inclusive OR SR to DR.	1.25
RSU	Subtract SR from DR	1.25

Register Skip Instructions		All execute in 1.0 μ sec
SEV	Skip the next instruction if register bit 15=0 (even).	
SMI	Skip the next instruction if register bit 0=1 (minus).	
SNO	Skip the next instruction if any bit in register=0.	
SNZ	Skip the next instruction if any bit in register=1.	
SOD	Skip the next instruction if register bit 15=1 (odd).	
SOO	Skip the next instruction if all register bits=1.	

Table 4. 980A Instruction Set (Continued)

Register Skip Instructions		All execute in 1.0 μsec
SPL	Skip the next instruction if register bit 0=0 (plus).	
SZE	Skip the next instruction if all register bits=0.	

Status Indicator Skip Instructions		All execute in 1.0 μsec
SEQ	Skip the next instruction if the last compare (CPA, CPL, RCA, or RCL) was =.	
SGE	Skip the next instruction if the last compare was $\geqslant$.	
SGT	Skip the next instruction if the last compare was $>$.	
SLE	Skip the next instruction if the last compare was $\leqslant$.	
SLT	Skip the next instruction if the last compare was $<$.	
SNC	Skip the next instruction if the carry indicator is not set.	
SNE	Skip the next instruction if the last compare was $\neq$.	
SNV	Skip the next instruction if the overflow indicator is not set.	
SOC	Skip the next instruction if the carry indicator is set.	
SOV	Skip the next instruction if the overflow indicator is set.	

Sense Switch Instructions		All execute in 1.0 μsec
SSE	Skip the next instruction if the indicated sense switches are set.	
SSN	Skip the next instruction if any indicated sense switch is not set.	

Multi-register Instructions		
LRF	Load registers A,E,X,M,S,L, and B from sequential memory locations starting at specified address.	
LSB	Load program counter with specified address and Status Register with specified address plus one, and branch.	
LSR	Same as LSB, with highest priority interrupt in priority interrupt option set to 0.	
SRF	Store registers A,E,X,M,S,L, and B into sequential memory locations starting at specified address.	
SSB	Store program counter and Status Register at specified address and address plus one, and branch to address plus two.	

Byte Manipulation Instructions		Execution Time
CLC	Logically compare one consecutive, specified byte string in memory to a second byte string in memory. The first byte-comparison-not-equal terminates the instruction, and the number of bytes left to be compared is stored in the X register.	5.0+2.25/byte

Table 4. 980A Instruction Set (Continued)

Byte Manipulation Instructions		Execution Time
MVC	Move a consecutive, specified byte string from one place in memory to another.	4.75+2.75/byte

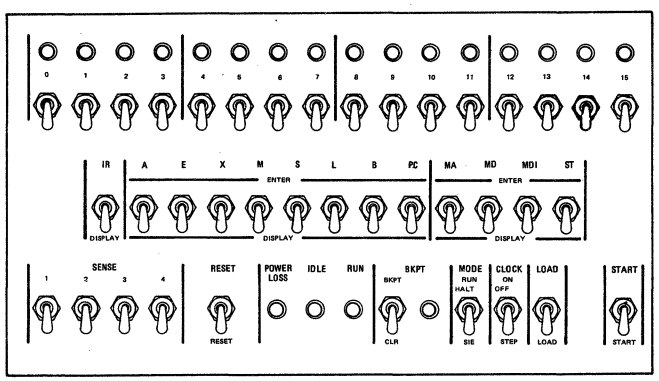
Memory/Register Bit Manipulation Instructions		Execution Time
SABO	Set a specified bit in register A to a one.	1.0
SABZ	Set a specified bit in register A to a zero.	1.0
SMBO	Set a specified bit in memory to a one.	3.25
SMBZ	Set a specified bit in memory to a zero.	3.25
TABO	Skip the next instruction if a specified bit in register A=1.	1.25
TABZ	Skip the next instruction if a specified bit in register A=0.	1.25
TMBO	Skip the next instruction if a specified bit in memory = 1.	2.75
TMBZ	Skip the next instruction if a specified bit in memory = 0.	2.75

Auxiliary Processor		
API	Automatically initiates transfer of information to device/ processor/CPU attached to auxiliary processor bus. (General purpose of special function.) This instruction is used to initiate execution of unique instruction sets implemented in special hardware.	AP controller dependent

Data Bus Input/Output Instructions		Execution Time
RDS	One word of data is moved from indicated external device into specified register or memory location.	3.00 → 4.75
WDS	One word of data is moved from a specified register or memory location to indicated peripheral device.	3.00 → 5.0

Direct Memory Access Channel Input/Output Instruction		Execution Time
ATI	Automatically transfer a buffer of data to or from a specific peripheral device.	2.5

Single Function Instructions		Execution Time
IDL	The computer idles until external interrupt or START switch	1.0
NRM	Shift combined A and E registers left until bit 0 of A register is different from bit 1, and fill vacated bits with zeros. Store the number of places shifted in X register. (Omit register E bit 0 from the shift, and force that bit to agree with register A bit 0.)	1.0 → 8.75



980A Console Control Panel

Console Control Panel

The operator's control panel is physically contained on a plug-in printed circuit board with operator access to switches and controls through a front panel cutout. Switch functions are performed by two or three position toggle switches and all control panel indicators are long-life (in excess of 10^5 hours) light emitting diodes (LED's). A key-operated LOCK/UNLOCK switch, located on the left of the control panel, disables switch control functions. An indicator lamp above the key switch indicates the application of primary ac power to the CPU. The power ON/OFF switch is located at the rear of the mainframe. Following is a brief description of the operating and control functions of the console.

Control	Function
DATA	16 switches and corresponding indicators used to enter or readout data
IR/DISPLAY	Initiates display of Instruction Register contents via the data display indicators
A through ST	Allows display or entry of data into selected working register. Note: MDI automatically increments memory address
SENSE 1-4	Four software accessed sense switches
RESET	Performs system reset function
POWER LOSS	Monitors battery level and indicates marginal battery power to maintain memory during ac power down condition
IDLE	Indicates the CPU has executed an idle instruction
RUN	Indicates the CPU is operating in the run mode
BKPT/CLR	Switch enable which compares data switches to memory address. Indicator lights up when comparison equal; if break point enabled, CPU halts
MODE	CPU mode control allowing run, stop, or single instruction execution conditions
CLOCK	Control allowing continuous, none, or single clock pulses to be generated
LOAD	Initiates auto load of 256 word ROM bootstrap into memory
START	Initiates RUN and SIE.

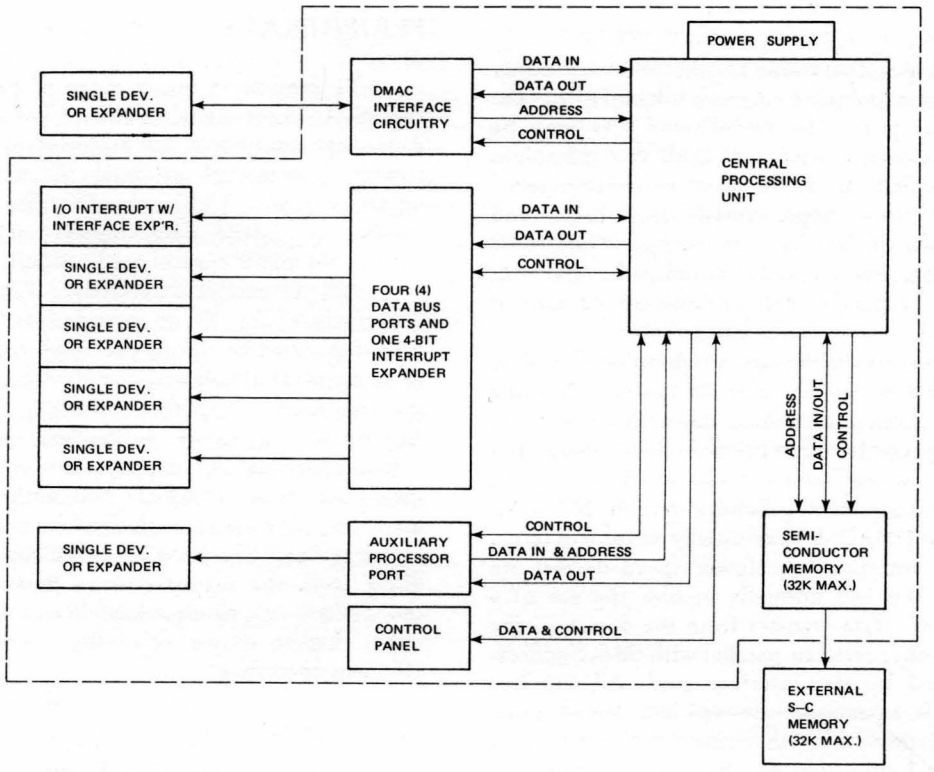
Interrupt Control

The 980A features a priority interrupt system that provides added program control of input/output operations, provides immediate response to abnormal conditions, and allows immediate recognition of special external conditions. The interrupt system has four levels of priority control as shown in Table 5.

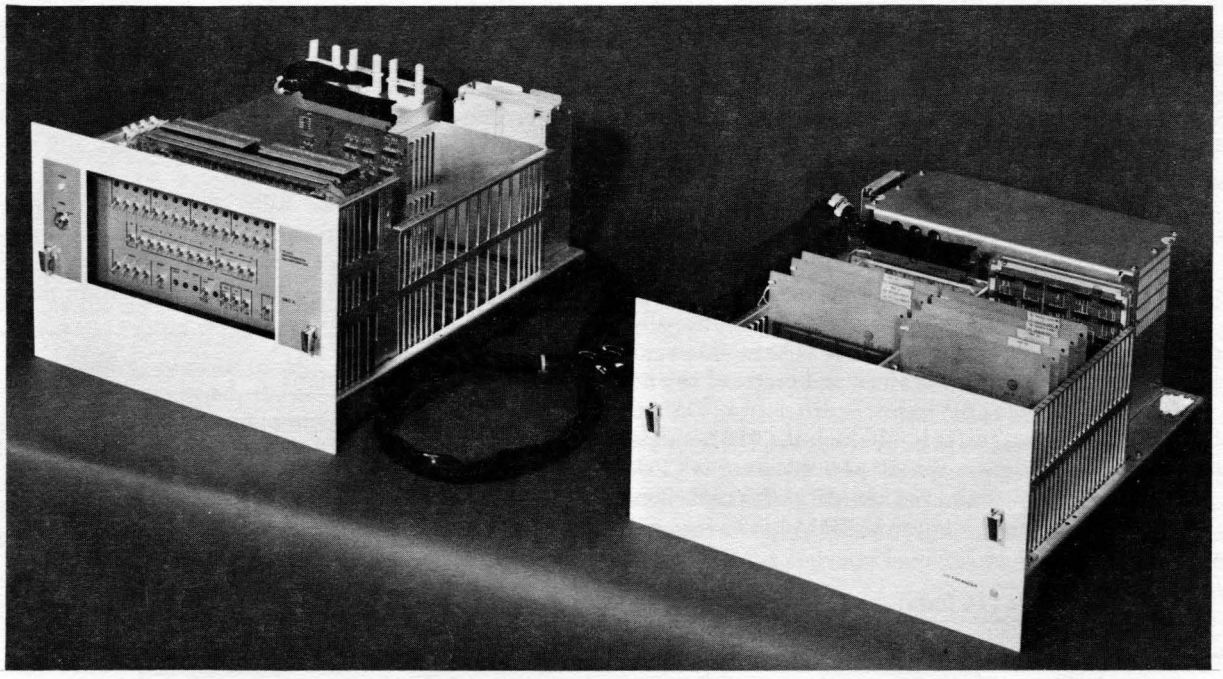
When an interrupt is recognized by the processor, the instruction at the trap address is executed; however, the program counter remains unchanged unless the instruction executed specifies a program counter change. If the instruction does not modify the program counter, the following instruction is executed from the normal program sequence. Interrupts are not recognized during the execution of the trap instruction and the following instruction. The internal interrupt cannot be disabled; however, the other interrupts can be masked by the control bit in the Status Register.

Table 5. 980A Interrupts and Priorities

Interrupt	Priority	Trap Address (Hexadecimal)	Remarks
Internal	1	0-2	Includes illegal op codes, PIF violation, memory parity error, power failure, and restart.
External priority	2	8-87	Optional expansion to 64 levels
DMAC	3	4	DMA device interrupt
I/O	4	6	I/O Bus interrupt



980A Basic I/O Configuration



980A With Expanded I/O and DMAC

I/O Control

Input and output operations for the 980A use either the I/O Bus, Direct Memory Access Channel, or the Auxiliary Processor port. The DMAC and I/O may be expanded with associated interrupts until the maximum configuration specified in Table 1 is reached. Special instructions have been implemented to initiate and supervise the transfer of data by each method. The DMAC and AP can operate at memory speeds, the I/O Bus transfers 16 lines of parallel data at a maximum rate of 130K words/second.

Controllers are available for all peripheral devices offered for the 980A. In the case of devices requiring high-speed DMAC communications, controllers take the form of multiple special function printed circuit boards and require specially wired connectors. Internal chassis expansion can accommodate generally one such DMAC controller; multiple DMAC devices usually require external chassis expansion. Interfaces to slower speed devices are made via the I/O Bus and normally involve the use of a single interface card. Data transfer from the device to the interface may be either serial or parallel with device address decoding performed by the Interface card. All I/O Bus devices interrupt via a common interrupt line. The program must test status to determine the cause of the interrupt. Interrupt decoding is provided on the I/O Bus expansion module to allow rapid identification of each interrupt.

Block transfers via the DMA channel are initiated by the Automatic Transfer Instruction (ATI) which selects the device and device function, and addresses an initialization list in memory. The DMAC controls the block transfer thereafter and transfers data words directly between the high-speed device and memory. Any change in the status of a DMAC device causes an interrupt to be generated. All devices connected to DMAC initiate an interrupt via the common DMAC interrupt line. The interrupt status bits for the eight DMAC ports are merged into a DMAC status word that is stored in memory at interrupt time. This allows quick access to the port causing the interrupt.

The Auxiliary Processor (AP) initiates communication via the API instruction. Memory access is then available to any AP controller. An optionally expandable hardware interrupt scheme where interrupt priority has been previously established and vectored can be used with AP controllers. AP transfers differ from DMAC transfers in that once a transfer is initiated, the 980A enters a wait state until such time as the AP port releases the CPU. Free access to memory is allowed the AP port controllers while operation is suspended; however, DMAC transfers will proceed as normal.

PERIPHERALS

TI provides a broad range of peripheral devices for the 980A. These include standard low-speed devices such as paper tape equipment and teleprinters and high-speed bulk storage devices such as fixed and moving-head discs and magnetic tapes. Universal I/O Bus interfaces for both parallel and serial data transfers are also available for custom computer control applications.

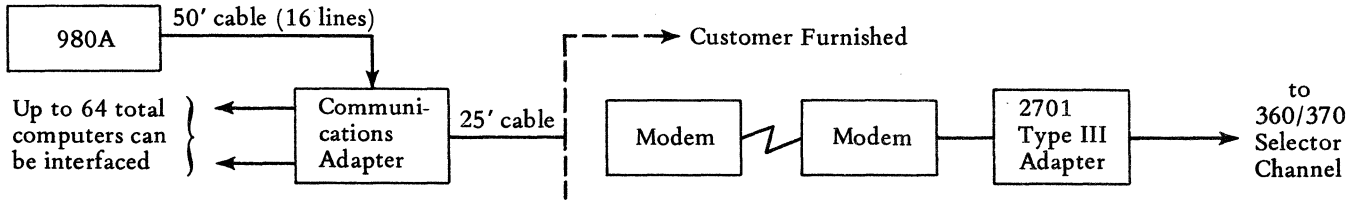
All peripherals described in Table 6, either directly manufactured by TI or provided as an OEM device, are fully supported by TI for the 980A computer. If purchased as an optional peripheral, each device will be furnished with the required computer interface and documentation. Appropriate hardware controllers, all required cabling, software drivers and support subroutines, and the device itself are fully checked out with the accompanying interfaces. Hardware maintenance contracts are available for all peripherals. Some TI specifications for OEM devices differ from the manufacturer's standard specification for the device; e.g., changes have been made to accommodate either higher device reliability, serviceability, or more effective operation.

Data Communications

Data communication devices, such as data sets and EIA compatible devices, interface the 980A through communication modules operating on the I/O Bus. Both half and full-duplex operating modes are available; however, the full-duplex module requires two I/O ports. Transmission rates available are 110, 300, 1200, and 2400 baud. The communication module provides asynchronous operation and includes character assembly/disassembly, insertion/deletion of start/stop bits and generates an interrupt when character transmission is received or completed. Bell Data Sets 103A or F and 202 C or D are directly interfaced and controlled by the module. The communication module fully complies with EIA Standard RS-232B or will interface devices requiring a standard 20-milliampere current loop. A ±15-volt regulator is required when operating the communication module with an EIA compatible device.

360/370 Communications

A 360/370 Communications Adapter (C/A) is available for the 980A. The C/A operates full-duplex to a customer furnished, self-clocking, synchronous modem (such as the Milgo 4400) operating at 2400 baud. A simplified block diagram of the network is shown as follows:



(continued on page 19)

Table 6. 980A Peripheral Devices

TI Part No.	Manufacturer	Description	Power Requirements	Size	Ship Weight
Teleprinters					
966330	TI Model 730	Virtually silent operation. Print rate-10, 15, or 30 cps switch selectable. MTBF < 2 failures/year any reason. Uses standard TTY DC interface (20 mA/60mA neutral). Full ASCII character set. Options-answerback memory and 5mA polar IF.	115Vac±10% 50-60 Hz 100 watts	18DX17WX16¼H	40
954783	TI Model 725	Portable version of 730 with built-in acoustic coupler and carrying case.	240 watts max.	19DX21WX6½H (integral carrying case)	40
965910	Teletype Corp. ASR-33/TBE	Uses standard EIA interface. Print rate-10 cps. Paper tape read/punch rate-10 cps.	115Vac±10% 60 Hz±3/4% 250 watts	Printer: 18DX22WX8.5H Stand: 8DX18WX24H	50 22
Paper Tape Equipment					
964569	Remex, Model 305	High-speed, heavy duty, fan-fold multilevel reader. Capstan drive, asynchronous read rate-300 cps. Tape travel L-R. Max. Temp. 50°C.	115Vac±15Vac 60 Hz 200 watts	8DX19WX7H (2½-in. protrusion)	42
964568	Remex, 3075	Combination fan-fold reader/punch asynchronous, stop-on-character. Punch-75 cps. Read up to 300 cps. Punches 0.003-0.0043 in. paper or mylar tape. Max. Temp. 55°C, 90%RH.	115Vac±10% 47-63 Hz 250 watts	12DX19WX10½H (2½-in. protrusion)	55
965943	Remex, 1075	Same specs. as reader/punch combination except punch only.	180 watts	Same as 3075	48
965946	Remex, 1300	Fan-fold, bidirectional, 300 cps tape reader. Stop-on-character. Sprocket drive.	115Vac±10% 47-420 Hz 80 watts	8DX19WX7H (2½-in. protrusion)	38

Table 6. 980A Peripheral Devices (Continued)

TI Part No.	Manufacturer	Description	Power Requirements	Size	Ship Weight
Punched Card Equipment					
966323	Data Products 8330	Asynchronous, photoelectric card reader-300 cpm. Input hopper capacity-600 cards. Internal cooling included. Max. Temp. 100°F, 90% RH. Table top mounted.	115Vac±10% 60 Hz±5% 120 watts	11½DX23WX13H	60
217185	Data Products SP 120	Card punch-100 cpm (full 80-column) or 160 column punches/second. Input hopper capacity-1000 cards. Internal 12-bit column buffer. Max. Temp. 85°F, 65% RH. Stand alone.	115Vac±10% 60 Hz±1% 300 watts	33DX37WX35H	570
Video Terminal					
957478	Hazeltine Model 2000	CRT display-12 in. (diagonal) screen 5 X 7 dot matrix/char., 64 alphameric char. 27 lines, 74 char/line. Full buffer 2K X 8 memory. Operates with std. EIA interface at 2400 baud, full duplex. Keyboard standard TTY design. Table top mount.	117Vac±10% 60 Hz±2Hz 350 watts	22DX19WX12½H	90
Line Printer					
964559	Printec, Model 100	100 cps impact liner printer, table/stand mount. Uses up to 6 part, fan-fold pin-feed paper. Print rate 132 column at 36 lpm; 80 column at 72 lpm. Full 64 character ASCII. Has vertical forms control.	115Vac±10% 60 Hz±1% 250 watts	18DX24WX11H	235
Analog-Digital Conversion					
964566	Computer Products RTP 7480/ 20/22	Wide range A/D converter. Fully addressable multiplexed input. Up to 16 (8 inputs/card, Hg-wetted or reed relays) cards housed in one rack. 13 programmable input ranges ±2.5 mV to ±10.24V. Output-15 bits, binary, 2's complement at 40 samples/sec; 13-bits output at 200 samples/sec. Z_{in} = 50	115Vac±10V 50-400Hz 100 watts max.	18DX19WX7H	25 (est.)

Table 6. 980A Peripheral Devices (Continued)

TI Part No.	Manufacturer	Description	Power Requirements	Size	Ship Weight
		megohm. Max. Temp. 60°C. Stability ±0.005%/°F. Common Mode 110 db with 1K source unbalanced. All channels differential input with guard (3-pole).			
965886	Computer Products RTP 7460/ 20/21	High-speed, high-level A/D converter. Input voltage ±4.096V or ±10.24V. Z_{in} = 10 megohm across 500pf. Aperature time - 200 μsec. Random access addressable to 4096 channels. Accuracy - 0.05% full scale. Output - 12-bit, 2's complement. Sample rate - to 20K samples/sec. Max. Temp. 60°C. Up to 16 (8-input) cards housed in rack. Up to 8 racks can be daisy-chained.	115Vac ±10% 50-400Hz 100 watts max.	18DX19WX7H	25 (est.)
964567	Computer Products RTP 7430/ 30	General purpose D/A converter. Rack houses up to 16 single-channel cards or other GP digital cards. Random addressing. 12-bit programming for ±5V, ±10V, or 4-20 mA output (select one when ordering), 2.5 mV resolution min. Uses D/A plug-in cards 7455/20/21/22.	115Vac±10V 47-63 Hz 330 watts	18DX19WX7H	25 (est.)
Line Printers		(NOTE: The following devices interface to 980A through DMAC.)			
217065	Data Products Model 2310	80 column, 356 lpm impact printer. 20 character input buffer. Full 64 character ASCII; size 0.1 in. X 6 lines/inch. Includes forms control. Indicators for: Paper Out, Over Temp., Over Speed, and PS Fail. Max. Temp. 43°C, 90% RH.	115Vac±10% 47-63Hz 330 watts	22DX23WX23H	220
Magnetic Disc Storage					
955157	Diablo Model 31	Uses 2315-type disc cartridge (15 in. diameter) with 24 sector marks. Capacity-1.14 M words (16-bit). Organization-406 tracks (2-sides), 88, 32-word sectors/track, 2200 bpi. Moving head operation, access time-15 msec (adjacent		18½DX19WX6½H	50

Table 6. 980A Peripheral Devices (Continued)

TI Part No.	Manufacturer	Description	Power Requirements	Size	Ship Weight
		tracks), 70 msec average, 135 msec for full 200 track movement. Bit transfer rate 1.56 MHz. Max. Temp. 90°F.			
		Power supply separate unit.	115Vac±10% 47-63Hz 300 watts	18DX19WX3½H	40
955158	Diablo Model 33	Dual moving head disc-one fixed cartridge, one removable. Same specs. as Model 31 except twice the word capacity.	400 watts	253/4DX19WX14H	106 40
961751	Digital Development Model 6000	Low capacity, high reliability (design for 8 year life), sealed He purged fixed head disc. min. capacity-57K words (16-bit)/ head group; can be stacked to 8 groups. Average access time-8.7 msec. Bit transfer rate-220Kc. Error rate 1 bit in 10^{13}. Max. Temp. 50°C, 95%RH. Shock-2G's. Vibration: 0-10Hz (0.005 in. excursion), 10-25Hz (0.002 in. ex.), 25-50Hz (0.001 in. ex.), 50Hz (0.005 in. ex.).	115Vac±10% 60Hz±3% 300 watts	22DX19WX15½H	140
961754	Digital Development Model 7311/ 7312	High capacity, fixed head disc. Design life-10 years. Helium pressurized unit. Max. Temp. 50°C, 95%RH. Same general specs. as 6000 except 688K words min. capacity, expandable in groups of 230K words to max. of 1.8M words.	400 watts	23DX18WX17½H	210
Magnetic Tape					
217536	TI Model 979	½ in., 9-track, IBM compatible format 800 bpi tape drive. Fixed speed of 37½ ips. All standard controls and features are included. 10½ reel. Daisy-chain 3 units/controller max. Max. Temp. 90°F, 80%RH.	115Vac±10% 47-63Hz 350 watts	12DX19WX24½H	165

NOTE: All peripheral devices available for operation at 230 Vac, 50Hz.

The C/A emulates the operation of an IBM 2848 Display Controller by assuming a 2260 address in the polling sequence. In the receive mode, the adapter acquires 10-bit characters from the modem in serial form, strips away the start/stop bits, and issues a character present interrupt. In the transmit mode, the converse operation is performed. Parity is checked on each character presented to the adapter as well as a longitudinal record check. Clocking is derived from the modem.

The software handler for the C/A can be linked into the basic System Executive and requires about 300 additional words of memory. Communication to the C/A is performed as if it were a system peripheral device of the 980A. The C/A incorporates a 500-word buffer per device thereby allowing semi-independent operation.

The C/A currently responds to two 2848 commands: Specific Poll and Write/Erase. The C/A is fully responsible for all line protocol (half-duplex), command decoding, and response to the 360/370. Future adaptations will include General Poll.

System interfaces are expandable in groups of four or eight 980A's.

Firmware Bootstrap Loaders

The 980A is equipped with firmware bootstraps in the form of plug-in 256 word read only memories. Bootstraps are included for the following devices: teletypewriter, magnetic tape, high-speed paper tape reader, fixed-head disc, moving-head disc, and the card reader. A firmware program is also included which writes idle instructions throughout memory. Bootstrap loading is initiated via the LOAD switch on the front panel.

Performance Assurance Tests

The performance assurance tests for the 980A include diagnostics for the CPU, memory, and supported peripheral devices. These tests are designed so that operating personnel can easily verify hardware integrity.

The memory and instruction tests exercise all parts of the central processing unit in accordance with the machine logic diagrams for the computer. These tests may be loaded and executed as stand-alone programs, (minimum 4K memory), or under control of the CPU test executive. Should a failure be identified, the trouble is pinpointed by the program and the operator is notified which instruction or memory location is inoperative.

Peripheral performance demonstration tests may be loaded as stand-alone programs to facilitate testing in a small system. Where possible, a peripheral test uses a logging typewriter to communicate the nature of any problems encountered, otherwise it is necessary to consult the program listing to determine how the device is failing. Tests are furnished for the following DMAC peripherals:

- Moving Head Disc
- Fixed Head Disc
- Magnetic Tape
- High Speed Line Printer

The Data Bus peripheral tests accommodate the following:

- ASR 33 Teletypewriter
- Silent 700* Data Terminal
- High Speed Paper Tape Reader and/or Punch
- Asynchronous Data Set (Bell 103A, 103F, 202C, or 202D)
- Serial-Buffer Line Printer
- CRT Terminal
- Data Module, parallel 16-bit in/out
- Card Reader and Punch
- Low Speed Line Printer

SOFTWARE

Texas Instruments furnishes, free of charge, a prepackaged software kit with each Model 980A Computer when the essential peripherals are also purchased from TI. Five standard kits are shown in the following configuration diagrams. Source for latest released configurations is available on IBM compatible 9-track magnetic tape for a nominal reproduction charge. Disc configurations will operate if either one or both of the disc units shown are present. The typewriter keyboard printer is used for operator communication. High-speed peripherals and disc units increase the utilization of the Model 980A Computer.

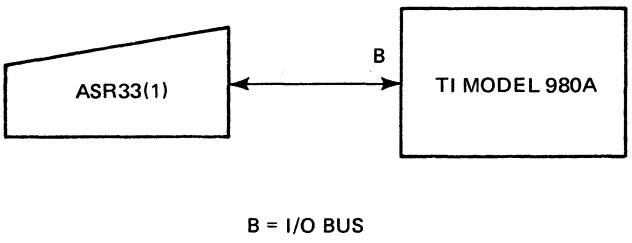
The operator can select the device to be used by a program before the program is run. Non-essential devices left out of a standard configuration will have no effect on the operation of a program unless the operator assigns an input or output to the missing peripheral.

Complete sets of Device Service Routines and Operator Communication Modules are included in the material furnished in the standard configuration. Modules for the Disc File Management Program are also furnished with a configuration 4 and 5 system. These modules may be recombined easily to form other configurations that are needed. This recombination is called system generation and may be performed by the purchaser using the Assembler and Link Editor furnished with any of the five standard configurations. System generation for non-standard configurations may also be purchased from TI.

*Trademark of Texas Instruments, Incorporated

980A CONFIGURATION 1

The Software Part Number for Configuration 1 is 963870.



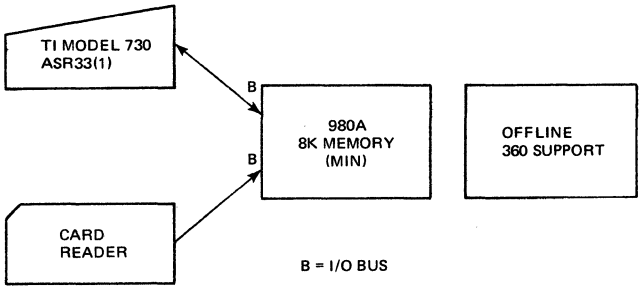
PAPER TAPE MEDIA
- ASR33 Loader
- EDIT
- SAP4
- FORTRAN IV Compiler (2)
- FORTRAN IV Library
- LINK4
- DEBUG
- Subroutine Library
- IOP-1 (3)
- Device Service Routine Library
- System Module Library

OTHER MATERIAL
- TI Model 980A CPU PAT
- TI Model 730/ASR33 PAT

Notes:
1. ASR33 must be equipped with Auto Reader and Auto Punch On/Off feature.
2. FORTRAN IV Compiler operates in 12K memory with IOP-1. A Class II IOP will operate the compiler in 8K memory.
3. IOP-1 is a Class III system with operator communication.

980A CONFIGURATION 2

The Software Part Number for Configuration 2 is 963871.



CARD MEDIA
- Card Loader
- EDIT
- SAPG
- LINKG
- DEBUG
- FORTRAN IV Compiler (2)
- FORTRAN IV Library
- Subroutine Library
- IOP-2
- Device Service Routine Library
- System Module Library

PAPER TAPE MEDIA
- Paper Tape Loader

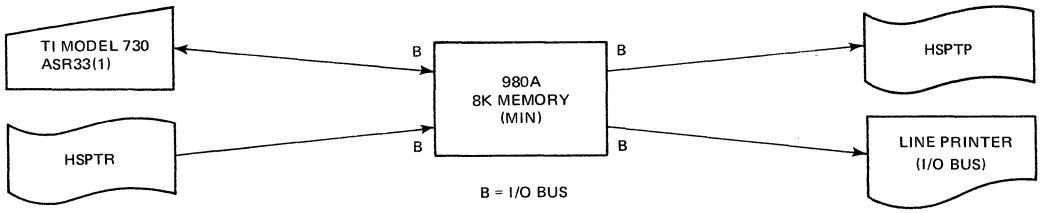
MANGETIC TAPE
- SAP980A/360 Source
- Link Edit Source

OTHER MATERIAL
- CPU PAT
- ASR33 PAT
- Card Reader PAT

Notes:
1. ASR33 must be equipped with Auto Reader and Auto Punch On/Off feature.
2. FORTRAN IV Compiler operates in 12K memory with IOP-2.
3. IOP-2 is a Class III system with op. comm.

980A CONFIGURATION 3

The Software Part Number for Configuration 3 is 963872.



PAPER TAPE MEDIA
- ASR33 Loader
- High-Speed Paper Tape Loader
- EDIT
- SAPG
- FORTRAN IV Compiler (2)
- FORTRAN IV Library

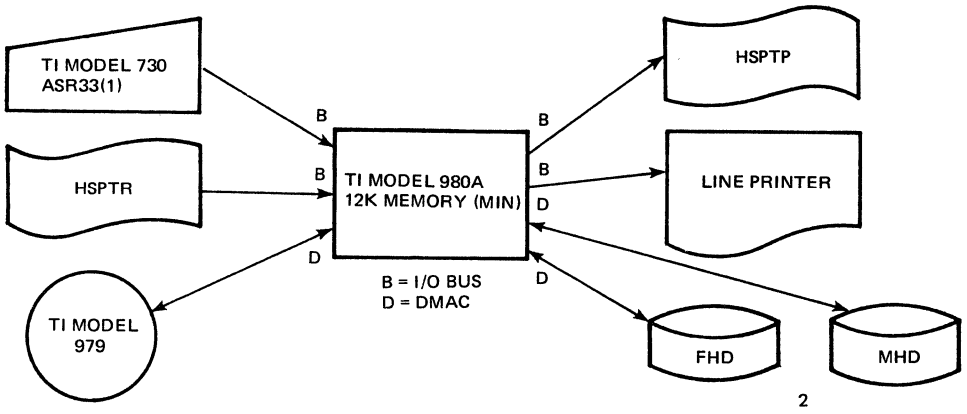
PAPER TAPE MEDIA (Continued)
- LINKG
- DEBUG
- Subroutine Library
- IOP-3
- Device Service Routine Library
- System Module Library

OTHER MATERIAL
- TI Model 980 CPU PAT
- TI Model 730/ASR33 PAT
- Paper Tape Reader PAT
- Paper Tape Punch PAT
- Line Printer PAT

Notes:
1. ASR33 must be equipped with Auto Reader and Auto Punch On/Off feature.
2. FORTRAN IV Compiler operates in 12K memory with IOP-3.
3. IOP-3 is a Class III system with operator communication.

980A CONFIGURATION 4

The Software Part Number for Configuration 4 is 963873.



PAPER TAPE MEDIA
- High Speed Paper Tape Loader
- EDIT
- SAPG
- FORTRAN IV Compiler
- FORTRAN IV Library
- LINKG
- DEBUG

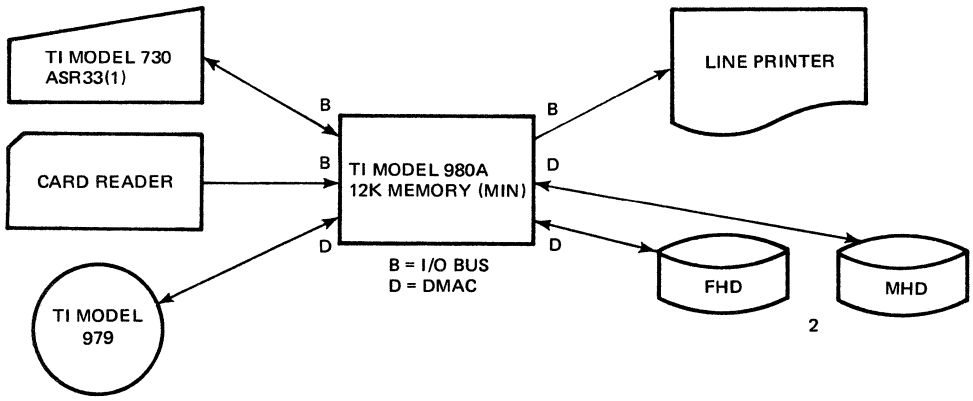
PAPER TAPE MEDIA (Continued)
- IOP-4
- Subroutine Library
- Device Service Routine Library
- System Module Library
- FMP Modules
- MHD System Boot
- FHD System Boot
- TILT Processor

OTHER MATERIAL
- Model 980A CPU PAT
- Model 730/ASR33 PAT
- Paper Tape Reader PAT
- Paper Tape Punch PAT
- Line Printer PAT
- Model 979 Magnetic Tape Pat
- FHD PAT
- MHD PAT

Notes:
1. ASR33 Must be equipped with Auto Reader and Auto Punch On/Off feature.
2. Either one or both disc units may be utilized.

980A CONFIGURATION 5

The Software Part Number for Configuration 5 is 963874.



CARD MEDIA
- Card Loader
- EDIT
- SAPG
- FORTRAN IV Compiler
- FORTRAN IV Library
- LINKG
- DEBUG

CARD MEDIA (Continued)
- Subroutine Library
- IOP-5
- Device Service Routine Library
- System Module Library
- FMP Modules
- MHD System Boot
- FHD System Boot
- TILT Processor

OTHER MATERIAL
- CPU PAT
- Model 730/ASR33 PAT
- Model 979 PAT
- Card Reader PAT
- Line Printer PAT
- FHD PAT
- MHD PAT

Notes:
1. ASR 33 must be equipped with Auto Reader and Auto Punch On/Off feature.
2. Either one or both disc units may be utilized.

Basic System Software

The basic software for the 980A provides simplified operation and control of the computer. It is composed of modular elements and provides a single program execution environment. The modules in the Basic System include:

- A system loader for installation of free-standing program.
- A Program/Machine Housekeeping subsystem furnishes power loss/restoration, memory protect/privileged instruction monitoring, lower limit address relocation protection, internal interrupt servicing, linkage to floating point math subroutines, manual loading, and control of program execution.
- An Input/Output subsystem connects logical unit with physical devices and performs I/O for all peripheral devices connected to the computer.
- An Operator Communication package for simple operator control of program loading, logical/physical unit assignment, program execution, and Disc File Space allocation.
- A Disc File Management subsystem which builds, identifies and maintains sequential files on one or more disc volumes.

These Basic System modules are used in combinations to provide four classes of operation. Basic Systems generally belong in one of the four classes depending on the peripheral devices selected by the user, the amount of memory in the system, and the complexity of the application.

Class I. The Class I system requires only a device for loading. Free standing programs are loaded and executed by the operator. The computer is operated from the front panel. Programs perform input/output directly via the data bus and Direct Memory Access Channel. Supervisor calls used in Class II, III and IV systems cannot be recognized or serviced. All interrupt servicing is the responsibility of the user program.

Class II. The Class II system also requires only a device for loading and is operated from the front panel (no operator communication package). The I/O assignments are preset, but they can be changed from the front panel. This class of executive routines comprehends MP/PIF, manages linkage to the floating point subroutines, decodes supervisor calls, and services internal interrupts. The Class II system also supports the operation of FORTRAN, the Link Editor, and other language processors as well as user generated programs. Input/Output is performed via logical units.

Class III. Class III includes an Operator Communication package which allows control from a teletypewriter or other input device instead of the front panel. On-line control of program execution and reassignment of I/O devices is standard. Input/Output programming is performed via logical units. The on-line message writer keeps the operator informed of detected peripheral malfunctions and program errors. All programs that will operate with a Class II system will operate in a Class III system.

Class IV. Class IV supports system operation with one or more discs. The system may reside on the disc. File Management provides for the creation, use, and deletion of sequential disc files on single or multiple fixed head discs or moving head discs with removable disc cartridges. Data and system control information can be stored in files on the disc and accessed by file name. Input/Output to all peripherals and to disc files is via logical units.

Table 7 outlines the memory requirements and special features for software systems supported by TI for the 980A.

Input/Output Methods

FORTRAN provides the easiest method of performing I/O. If formatted I/O is desired at the assembly language level, the FORTRAN library may be linked to any assembly language program to provide the user with another easy to use I/O facility.

For the user who wants to write stand-alone programs and handle all I/O and interrupts without assistance, a manual is furnished with step-by-step coded examples for every peripheral available on the 980A. The examples range from reading a character on the teletypewriter and waiting for operation complete to initializing the automatic transfer of a buffer of data to a disc. All commands are listed for each device as well as the meaning of the status returned when the operation is complete. A section is included on interrupts with suggestions for handling. Systems programming considerations are included.

System Classes II, III, and IV include the peripheral control and input/output management that enable the programmer to use the I/O devices connected to the 980A computer in a manner that is largely device independent. This is accomplished by coding a program that requests I/O for each program function from a specific logical unit. The logical unit is identified by a number; i.e., a Logical Unit Number (LUN). Before the program is executed, the operator assigns the LUN to a physical device. For example, the assembler is coded to accept input from LUN 5. Before the assembler is executed, the operator may give the command to "Assign LUN 5 to the card reader". In this example, the assembler will read the source program from the card reader. Program functions include:

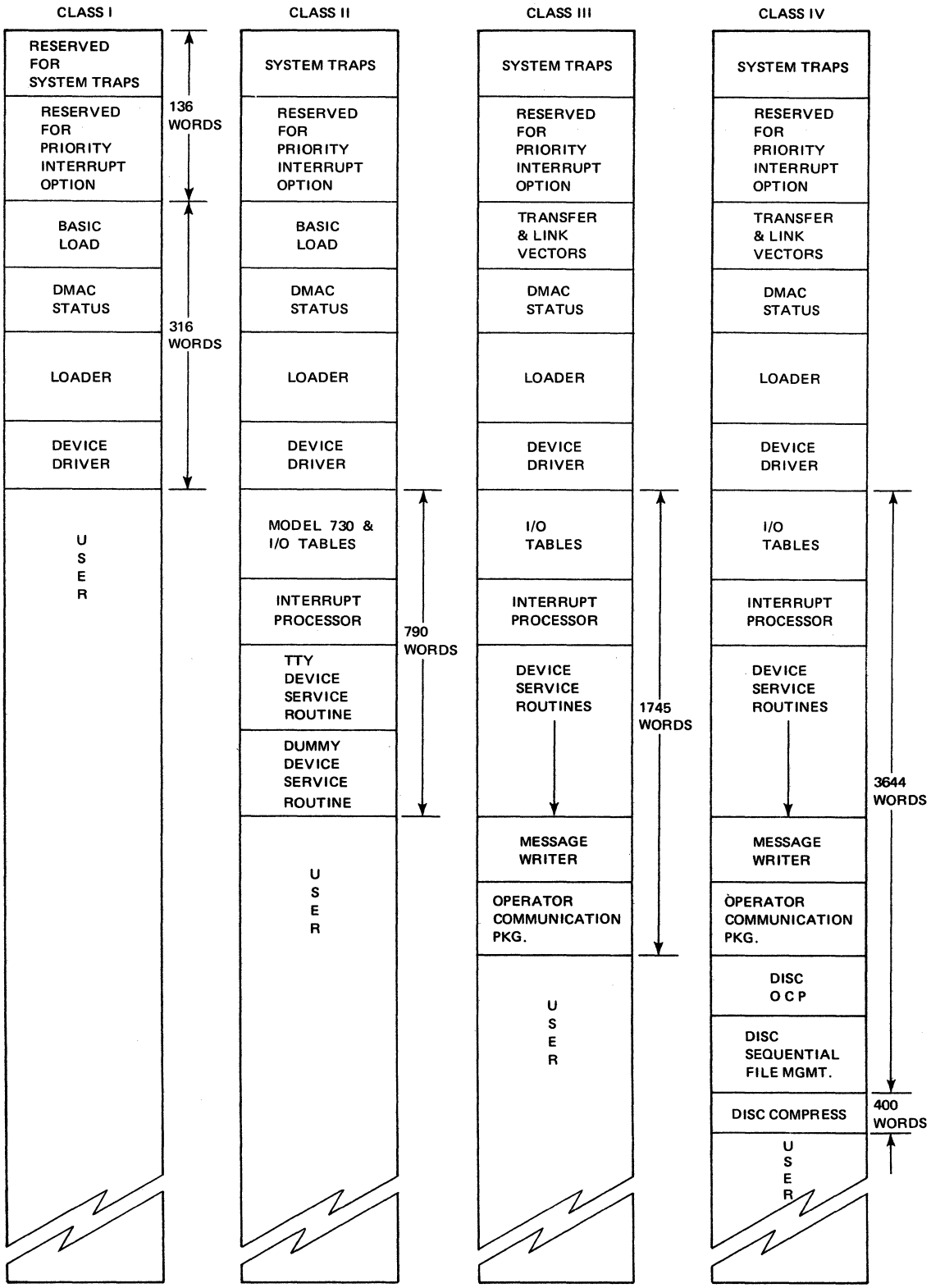
Read ASC II
Read Object
Write ASC II
Write Object
Rewind

(continued on page 25)

Table 7. 980A Software Systems

System Software	Memory Required	Comments	System Memory Required
Interrupt traps	136	Reserved memory	136
Loaders:			
730/ASR33	316	Only one required	
Card	342		
High-Speed PTR	313		
Disk	299		
Magnetic Tape	320		
System Executive:			
Class II	790	Includes ASR33	
Class III	1745	Includes ASR33	
Class IV	3644	Includes ASR33 and one disc controller	
Device Support:		(2)	
Keyboard (1)	191		
Card Reader	265		
Card Punch	445		
Magnetic Tape	185		
High Speed PTR	187		
High Speed PTP	189		
Line Printer	387		
Dummy	51		
		(Total peripherals added)	
Disc File Management	1780	Include 512 word buffer for blocked I/O	
Compress Disc Volume	400	(if required) Optional at sys. gen. time	
SAP4	2960		
SAPG	3581		
DEBUG	425		
EDIT	1594		
TILT	5158		
LINK EDIT	2600		
FORTRAN IV (pass 1)	6532		
(pass 2)	2563		
FEDIT	2957		
FLT 980	420		
		(Select largest desired program)	
		(Estimated working memory)	
		Total Memory Required	

Note: (1) Add 170 words for ASR33.
(2) Add 15 words of memory when a second device of any type is added.
(3) TI reserves the right to change program sizes in order to enhance program effectiveness.



Note: Memory sizes are approximate and subject to changes that result in improved software performance.

980A Basic System Support Executive Control Routines

Backspace
Forward Space
Open
Open, Rewind
Close
Close, Write EOF
Unload

Operator Communication

This package is included in the Class III and IV executive control routines. Its modular design allows any non-essential commands to be removed from the package thus saving memory. In the following commands, LUN is a hexadecimal logical unit number, PD is a physical device, TYPE specifies the file type, and EXTENT is the number of records in the file. The SKIPCS command allows a conditional skip of NN control statements. The //SWAPCS command takes future commands from a new device. Thus, a precanned command stream such as a FORTRAN compile and go sequence of commands can be stored on the disc and be subsequently switched to as required.

The available commands are:

```
//ASSIGN,LUN,PD,FILNAM.
//RELEASE,LUN.
//DEFINE,DISC,FILNAM,RECSZE,
      TYPE,EXTENT.
//DELETE,DISC,FILNAM.
//REWIND,LUN.
//SWAPCS,LUN.
//SKIPCS,NN.
//EXECUTE,PD,NAME.
//COMPRESS,PD,VOLUME.
```

Disc File Management Subsystem.

The Disc File Manager organizes each disc into 1 to 336 sequential files. The only limit to the size of a particular file is that it must reside on one disc cartridge or unit. The user specifies file name and size to the disc file manager; thereafter, the disc is addressed only by file name (no absolute addresses are allowed). All files in the Basic System are sequentially accessed on a record-to-record basis where each logical record is from 2 to 9984 characters of 8 bits each. The rewind, back space, and forward space commands only move a pointer with no data transferred. Individual programs may easily share data through the use of a common disc file.

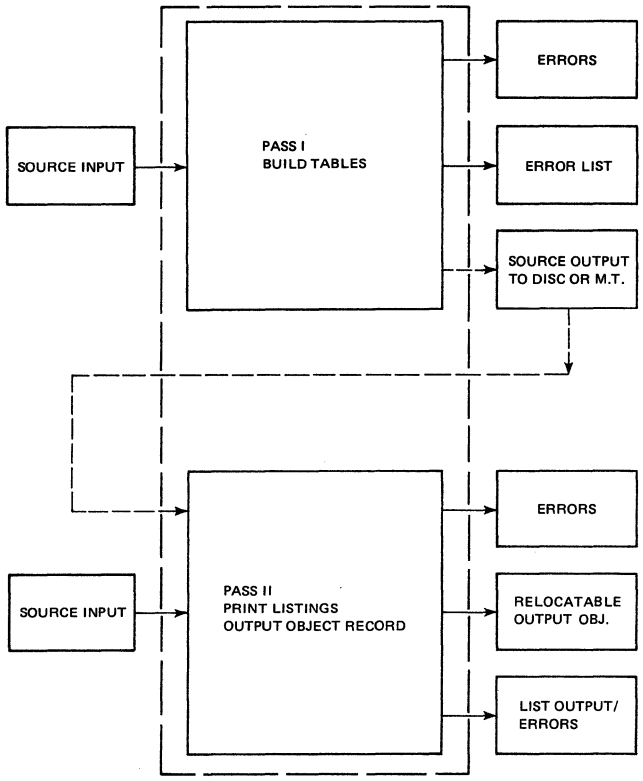
Each file uses a fixed-length number of sectors to transfer data to and from the disc. Since one disc sector holds 32 words (64 characters), five sectors contain 320 characters; and, four cards may be stored in five sectors at 80 characters per card. In this particular example the programmer may wish to specify blocking, and reduce the I/O time by reading from disc only once every four records. When blocking is specified, the Disc File Manager automatically blocks the file to reduce the number of disc accesses to a reasonable minimum. If unblocked files are specified, input/output is performed in one sector or multiples of one sector length records.

Language Processors And Support Programs

Assembler. A two-pass Symbolic Assembler Processor (SAP) is available for the 980A computer. The assembler uses storage media for enter-pass storage of the source if a rewindable device or disc file is available for this purpose. The following are significant assembler features:

- External references and definitions
- Expressions are allowed in any operand field.
- Relocatable or absolute object code
- Conditional assembly
- Common
- New operation codes may be defined for frequently used addressing modes or for system service requests.

Two variations of the Model 980A assembler are available. The variant for general use (SAPG) is operated in 8K memory with space remaining for more than 1000 symbols. The smaller variant (SAP4) operates in 4K memory with an ASR33 teletypewriter as the I/O device.



980A Assembler

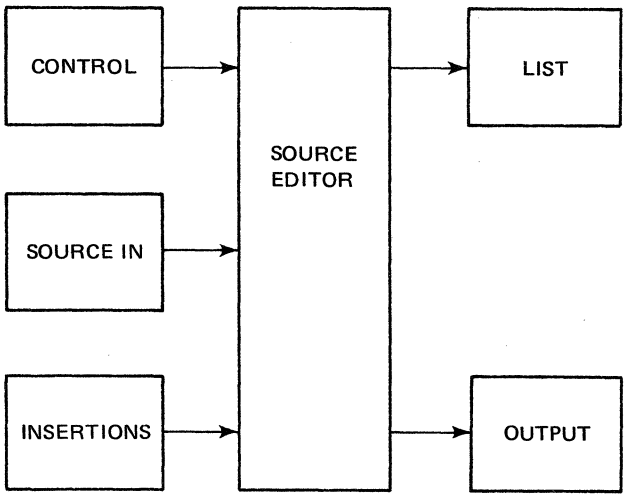
The assembler directives are as follows:

*BES	Block Ending Symbol
BRR	Base Register Reset
BRS	Base Register Set
BSS	Block Starting Symbol
BYTE	Generate Byte Address
*COMM	Common Storage Allocation
DATA	Generate Word Address or DATA
DEF	Define Entry Point
END	End of Source
EQU	Equate
FLAG	Bit Reference Address
*FRM	FORMAT
*HED	Heading
IDT	Identification
*IF	If (conditional assembly)
LIS	List
OPD	Operation Code Define
ORG	Orgin
PEJ	Page Eject
REF	External Reference
UNL	Unlist (stop listing)

*Provided in the SAPG assembler only.

A cross assembler is available for the IBM 360/40 (or larger) operating under either OS or DOS. The cross assembler is written in COBOL and requires approximately 100K bytes of memory. A cross assembler for the 960A computer also is available on the 980A.

Source Editor. The Source Editor allows instant editing and re-editing of program source material. It inserts, deletes, and replaces lines and characters as well as printing selected source lines for programmer verification. This program allows simplified update capability for all systems.



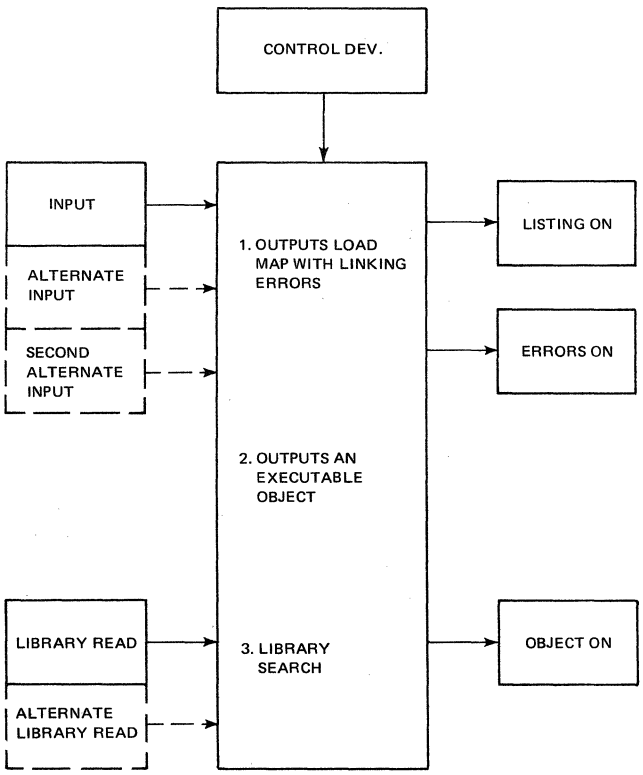
980A Source Editor

Link Editor. The one-pass Link Editor provides the capability of linking FORTRAN and/or assembly language programs into an executable object format. One level of overlay linking is provided. There are no practical limits on the number of overlays that can be linked. The main program at level zero may communicate with any overlay, but level one individual overlays may not communicate with each other directly.

If a library is furnished to the Link Editor, a library search is performed at the end of each overlay. The user may specify an optional library search at any node within any overlay. If the overlay option is not invoked, the Link Editor searches a library such as the FORTRAN library only once, and links only referenced library routines.

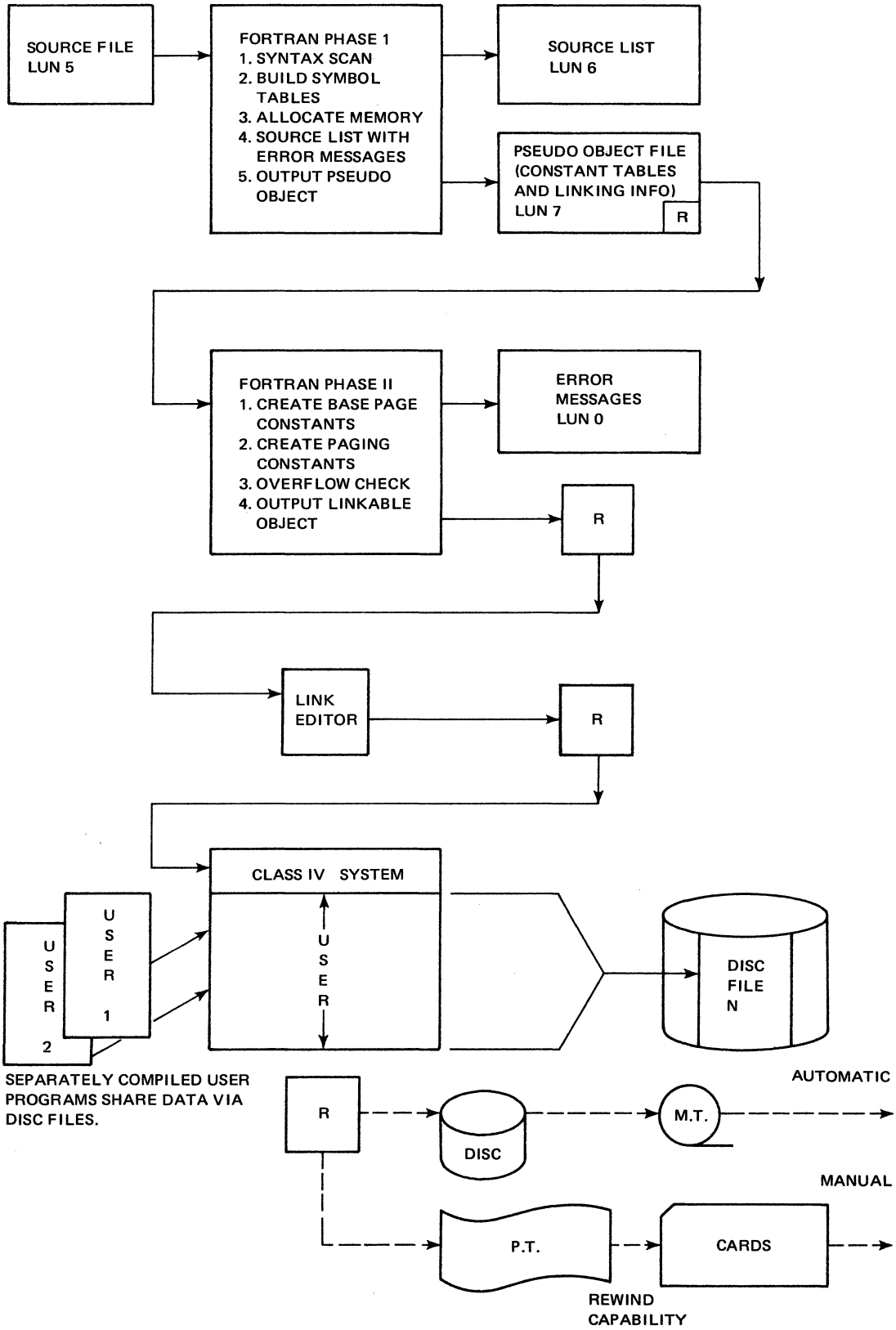
The Link Editor runs in 4K of memory or more, accepts input from a primary device and two optional secondary devices (thus programs on disc, magnetic tape, cards, etc. may be linked), and outputs a load map with linking errors. A cross 980A Link Editor which operates on the IBM System/360 also is available.

FORTRAN IV Compiler. The FORTRAN IV compiler furnished as standard software with the computer runs in 8K words of memory in Class II Systems* and



Link Editor

*Class III Systems require 12K, and 16K is recommended for Class IV Systems.



Basic System FORTRAN Execution

meets the specifications set forth by the American National Standards Institute in their publication number USAS X3.9-1966. Such compilers are commonly referred to as ANSI Standard FORTRAN or FORTRAN IV. The compiler exceeds FORTRAN IV as follows:

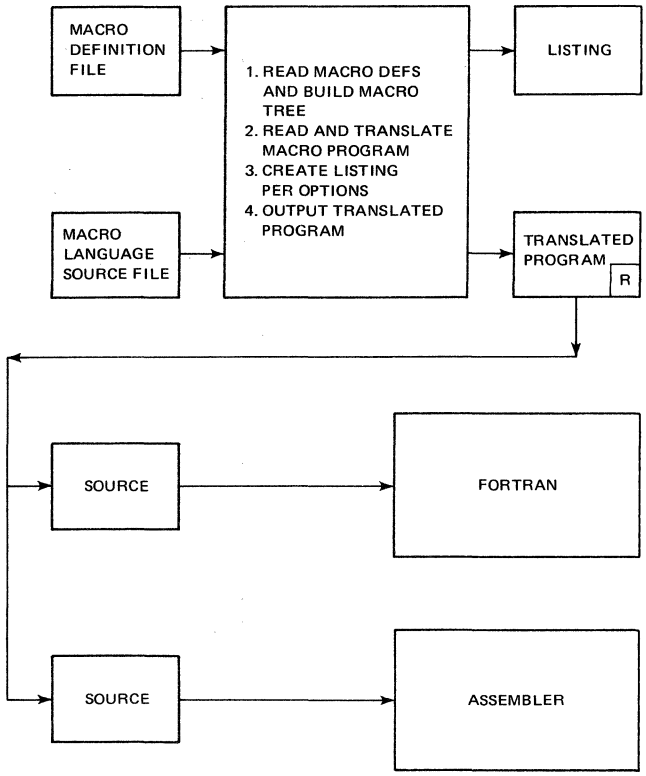
- Assembly language statements may be inserted at any point in a FORTRAN program.
- General integer expressions are allowed in subscripts, in the computed GO TO, as I/O unit designators, and as parameters of a DO statement.
- The capability to mix arithmetic types in expressions has been extended.
- DO parameters may be altered within a DO loop.
- Arrays may have any number of dimensions.
- The number of continuation lines allowed for a statement is limited only by the memory space available to the compiler.
- Identifiers may be any length, but only the first 6 characters are used.
- The format conversion facilities may be used without performing any I/O, thus the ASCII representation of a number may be obtained, or a conditional format read is possible.

This is a two-pass compiler which outputs an intermediate pseudo object of tables and linkage information. If rewindable storage media is available, the pseudo object does not have to be handled by the operator; otherwise, it must be manually input into pass 2 of the compiler.

TILT. Texas Instruments Language Translator (TILT) is a general purpose macro processor designed as a prepass to an assembler or compiler for language extension and language translation. TILT is a versatile tool which can be used by programmers and nonprogrammers alike to assist them in the efficient use of computer facilities. The language extension features of TILT enable programmers to define statements to the programming languages they use thus saving time and effort. Each implementation of TILT consists of a collection of statments or macro definitions. The user may add his own macro definitions to the furnished definition library; thus, TILT provides a dynamic environment for macro redefinition, language improvement, additions, etc. When a new function is required, a macro definition may be added to the library without disturbing existing language features. TILT versatility allows:

- Conditional assembly
- Created symbols
- Repetition over a list
- Definitions containing macro calls
- Parenthetical notation for compounding calls.

Debugging Aids. A DEBUG programming package is furnished for operation in the Class II, III or IV environment. Functions include program load, memory display and change, and software breakpoint.



980A TILT Macro Processor

File Copy/Merge. The generalized sequential file copy/merge program can be used to copy from file-to-file or to merge selected parts of two files into one file. Since the file/merge is performed on a record-by-record basis, any source program which is placed in a file may be easily copied or updated.

Subroutine Library. An extensive subroutine library is furnished for object form for use with programs written for FORTRAN IV assembly language. The FORTRAN Library contains subroutines for manipulation of integer, real, double precision, and complex data.

Subroutines are also available for conversion of:
Binary to decimal (integer and fraction)
Decimal to binary (integer and fraction)
Binary to hexadecimal (integer and fraction)
Hexadecimal to binary (integer and fraction).

SUPPORT

980A Documentation

With each 980A shipped, TI supplies a complete set of software documentation manuals. Included are manuals describing assembly language, FORTRAN, TILT, the basic system, source and link editors as well as the performance assurance tests and peripheral demonstration tests. Also

included with each system is a general systems description manual describing characteristics and installation procedures, and two manuals describing the theory of operation of the DMA, I/O and auxiliary processor channels. Each peripheral system device is documented with one manual outlining repair and maintenance of the device and a second describing the device controller, software handler, and performance assurance tests associated with the device. Additional hardware manuals are available at a nominal cost which completely describe the theory of operation, repair, and maintenance of the 980A CPU. Table 8 lists available manuals.

Table 8. 980A Hardware/Software Manuals

Title	Manual No.
Software Support Manuals	
Assembly Language Machine Instructions	961961-9730
Assembly Language Coding Conventions	961961-9732
Assembly Language Input/Output	961961-9734
FORTRAN Arithmetic and Control	961961-9740
FORTRAN Declarations and I/O	961961-9742
FORTRAN Library and IAL	961961-9744
Link Edit	961961-9714
Operating Systems Manual	961961-9710
IBM 360 Support Software	961961-9712
CPU Performance Assurance Tests	961971-9770
Peripheral Performance Demo Tests	961961-9772
Software Configuration Guide	961961-9790
Software Manual Index	961961-9792
TI Language Translator (TILT)	955382-9701
Hardware Maintenance Manuals	
Model 980A Auxiliary Processor and I/O Bus	960694-9701
System Description	960699-9701
Arithmetic Unit and Control Console	960699-9702
Memory, Memory Controller, DMAC	960699-9703
I/O, I/O Expansion, and I/O Controllers	960699-9704
Power Supply	960699-9705
Parts List and Assembly Drawings	960699-9706
Electrical Schematics	960699-9707
Load, Pin, and Wire Lists	960699-9708
Documentation Lists	960699-9709
DMAC Theory of Operation (2 volumes)	966312-9701
	966312-9702

Training

Texas Instruments maintains a fully staffed and supported training facility at its plant site in Houston, Texas. Classes are scheduled regularly in both software programming and hardware maintenance for 980A computer systems. The various courses consist of both classroom lectures and laboratory instruction. Students are provided with complete sets of appropriate manuals and other instructional documentation.

Purchasers or lessees of a computer system are allowed the enrollment of one person in any two courses. There is no charge for the training and it is provided with each system purchased up to a total of three systems. Fees for the enrollment of students not entitled to free training, as for all students, does not include any transportation, lodging, or meals.

Persons planning to take any of the programming courses should have a basic familiarity with computer programming in either a machine or compiler language. Persons taking the hardware maintenance courses should have a basic knowledge of digital logic and computer electronics.

The two or three courses making up the selected curriculum should be pursued serially and, for the convenience of the participants, will be scheduled for consecutive weeks. Information regarding class starting dates and student enrollment is available from any TI Field Sales Office. Each course lasts one week, Monday through Friday, 9 AM - 5 PM. Standard configurations of 980A computer systems are available to students for hands-on experience while attending the various classes.

The following is an outline of the training courses available for the 980A. In the general case, an experienced programmer should attend courses 9820-9830 while someone learning to program computers should enroll in course 9810-9820.

Course No. — Description

9810 — Introduction to the 980A – Architecture and Use
- Basic system hardware
- Machine language instructions
- Front panel use and operation
- Assembly language
- Practice problems and lab projects

9820 — Programming the 980A
- Review machine and assembly language
- Operation and use of Basic System Executive
- Directives and use of assembler
- I/O Support subroutines
- Source Editor and Debug aids
- Disc File Management
- Class problems and projects

9830 — Application of 980A
- Review assembler and assembly language
- Operator Communication subsystem
- Link Editor

Course No.	Description
	• FORTRAN IV – Use and subroutine support • Performance Assurance Test and Demo Tests
9850	Basic Hardware Maintenance • Assembly language programming • Front panel operation • I/O code sequences and interfaces • Documentation review • Performance Assurance Tests
9860	980A Hardware Maintenance • System configurations • Hardware theory of operation and logic • System generation • Performance Assurance Test and hands-on troubleshooting • Preventive maintenance

Special courses, video-taped class presentations, and courses conducted away from the Houston training center will be quoted on request.

Sales and Service Offices of Texas Instruments are located throughout the United States and in major countries overseas. Contact the Digital Systems Division, Texas Instruments Incorporated, P.O. Box 1444, Houston, Texas 77001, or call (713) 494-2168, for the location of the office nearest to you.

Texas Instruments reserves the right to make changes at any time to improve design and supply the best product possible.

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