MODEL 970
THEORY OF OPERATION

Section

4-1

Overview

The terminal is controlled by a Z80 microprocessor operating at a clock speed of 4.0Mhz. The Z80 can address all 64K memory and refreshes the dynamic RAM via the built in dynamic memory refresh counter during one M1 cycle.

4-2

Display Fundamentals

The SMC 9007 video processor/controller is the heart of the display unit. It has 14 address lines and can address up to 16k of video memory. The chip has a row-table addressing mode and each data row on the screen has its own starting address. A row table exists in memory which contains the starting address of each data row. For a screen with 26 data rows the row table will consist of 26 14 bit address each pointing to the first character position of its respective data row.

The controller is programmed to handle 26 rows by 80 or 132 columns. A Double Row Buffer (DRB) allows the buffer be loaded at a slower speed while the other buffer is displaying at screen painting speed. This is especially important in attribute assembly mode (hidden attribute). After the DRB is loaded the controller address lines are three stated for the remaining scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentages of total memory cycles available to the processor is approximately (10-2)/10 which equals to 80%.

During attribute assembly, the attribute data is latched into the controller during one clock cycle, both the character and its attribute is driven out and written into the row buffer (two 8 bit row buffers). This allows one to reserve 8 bits for font and 8 bits for attributes and each attribute only affects the character associated with it.

Smooth scrolling all or part of the screen (split screen) is accomplished by a scroll offset register and two programmable registers which define the start data row and the end data row of the smooth scroll operation. The offset register will force the scan line counter outputs of the controller to start at the programmed offset value rather than zero for the data row that starts the smooth scroll internal.

Row attributes such as double height double width or single height single width are programmed by the most significant 2 bits of the row address pointer in the row-table.

4-3

Communications

The keyboard is scanned and decoded by using a single chip microcomputer on the seperate keyboard PCB. Keyboard entry is transmitted to the processor serially at 9600 baud and received thru an SIO. Key codes are assigned using a PROM located on the keyboard PCB. The keyboard would interrupt the CPU for every character that is entered.

The modem interface is similar to the keyboard interface and also uses half a Z80-SIO tie to the interrupt line. The SIO is connected via a pair of line driver and receiver to a standard EIA RS-232 connector.

The printer also uses half a Z80-SIO serial interface with optional interrupt control on the interrupt line. The SIO is connected to an RS232 connector.

4-4

Character Generation

The character generator is 16k bytes of static RAM. The fonts are loaded from system RAM into the font RAM by the CPU. The characters are in a 6X8 matrix placed in a 8X10 cell with half-dot shift to achieve a 11X8 resolution. Bit 0 and 7 on the character font are used to control the half-dot shift.

4-5

Terminal Memory

2K bytes of CMOS RAM with memory power back up, are used to store the terminal`s set up parameters and the special function key codes.

The terminal has 16K RAM space for display memory which provides up to 2 pages in hidden attribute mode. The CRT controller constantly refreshes the display memory to the display screen.

The terminal can have up to 24K bytes of EPROM (2764) space for firmware program code space. The rest of the RAM space not used by the display RAM can be used for program data space.

4-6

Operating Clocks

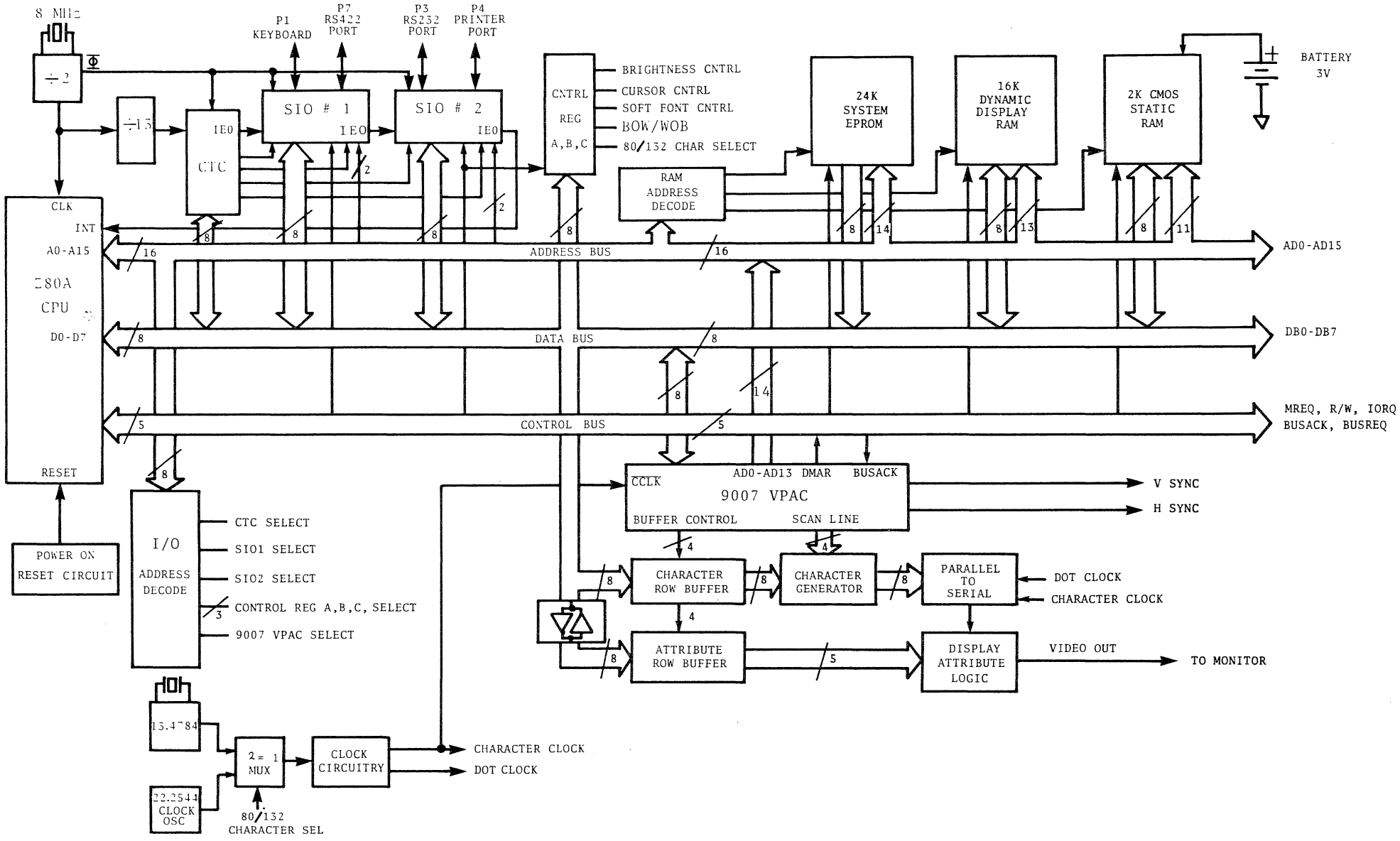
The Z80 CTC timing controller is used as a baud rate generator to generate the correct frequency clock for the 2 SIO channels. The baud rate on each channel is software programmable from 50 to 19.2K baud.

Interrupt Signals

The 970 CPU interrupt structure allows the peripheral device to identify the starting location of the interrupt service routine. This mode (mode 2) allows an indirect call to any memory location by a single 8 bit vector supplied by the peripheral. In this mode, the peripheral generating the interrupt places the vector onto the data bus in response to an interrupt acknowledge. The vector then becomes the least significant eight bits of the 16-bit indirect pointer.

The IEO and IEI lines of the peripheral devices are connected together in a daisy-chain fashion with the devices closest to the CPU having the lowest
priority.

Frame interrupt interrupts the CPU every 1/60 second or 1/50 second depending on line frequency setting. This can be used as the real time clock source. The CRT controller frame interrupt must be enabled in order to generate the frame interrupt. In response to this interrupt, the CPU jumps to location 66H.



970 FUNCTIONAL BLOCK DIAGRAM

TABLE 4-1

GENERAL SYSTEM MAP FOR MODEL 970

FFFFH	ADDITIONAL PROGRAM AREA (4K) CHARACTERS FOR SOFT FONT COMMUNICATION SERVICE ROUTINES COMMON ROUTINES
E000H	BY REPLACING THE 16K DRAM WITH 64K DRAM, THE ADDRESSES FROM 8000H TO FFFFH WILL REFER ONLY TO THE 32K OF DRAM
C000H	DRAM (16K) 8A61 DISPLAY AREA 8A60 STACK 8680 BUFFERS FOR HARDWARE INTERFACES 8180 PROTECT/FORMS MODE VARIABLES 8000 SET-UP VARIABLES
8000H	NON-VOLATILE RAM (2K) 7BBF PROGRAMMABLE FUNCTION KEYS 79F0 RESERVED FOR FUTURE USAGE 7800 SET-UP VARIABLES
7800H	BY REPLACING THE 2K NVRAM WITH AN 8K NVRAM THE ADDRESSES FROM 6000H TO 7FFFH WILL REFER TO THE 8K OF NVRAM
6000H	STANDARD PROGRAM AREA (24K) THREE 8K EPROMS OR ROMS
0000H	

TOSHIBA MOS MICROPROCESSORS

8-BIT SINGLE-CHIP MICROCOMPUTER

TMP8049P/8049P-6/8049PI-6
TMP8039P/8039P-6/8039PI-6

GENERAL DESCRIPTION

The TM8049P, from here on referred to as the TMP8049, is a single chip microcomputer fabricated in N-channel Silicon Gate MOS technology which provides internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 128 x 8 RAM data memory, 2K x 8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

The TMP8049 is particularly efficient as a controller. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic.

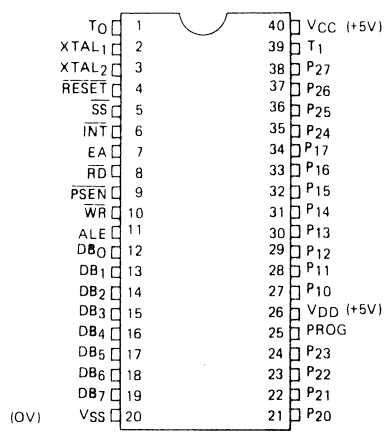
The TMP8039P is the equivalent of a TMP8049 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

The TMP8049P-6/TMP8039P-6 is a lower speed (6MHz) version of the TMP8049P/TMP8039P.

FEATURES

- Compatible with Intel's 8049
- 1.36 uS Instruction Cycle
- All instruction 1 or 2 cycles
- Over 90 instructions; 70% single byte
- Easy expandable memory and I/O
- 2K x 8 masked ROM
- 128 x 8 RAM
- 27 I/O lines
- Interval Timer/Event Counter
- Single level interrupt
- Single 5V supply

PIN CONNECTIONS (TOP View)



PIN NAMES AND PIN DESCRIPTION

VSS (Power Supply)
Circuit GND potential

VDD (Power Supply)
+5V during operation Low power standby pin for TMP8049 RAM.

VCC (Main Power Supply)
+5V during operation

PROG (Output)
Output strobe for the TMP8243P I/O expander.

P10-P17 (Input/Output) Port 1
8-bit quasi-bidirectional port (Internal Pullup ≅ 50KΩ).

P20-P27 (Input/Output) Port 2
8-bit quasi-bidirectional port (Internal Pullup ≅ 50KΩ).

P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB0-DB7 (Input/Output, Tri-State)
True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

T_0 (Input/Output)
Input pin testable using the conditional transfer instructions JTO and JNTO. T_0 can be designated as a clock output using ENTO CLK instruction. T_0 is also used during programming.

T_1 (Input)
Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

$\overline{INT}$ (Input)
External interrupt input. Initiates an interrupt if interrupt is enabled. Interupt is disabled after a reset. Also testable with conditional jump instruction.

(Active Low).

$\overline{RD}$ (Output)

Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

$\overline{WR}$ (Output)

Output strobe during a Bus write (Active Low) Used as a Write Strobe to External Data Memory.

$\overline{RESET}$ (Input)

Active Low signal which is used to initialize the Processor. Also used during Power down.

ALE (Output)

Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{PSEN}$ (Output)

Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{SS}$ (Input)

Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{SS}$ is low the CPU is placed into a wait state after it has completed the instruction being executed.

EA (Input)

External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High).

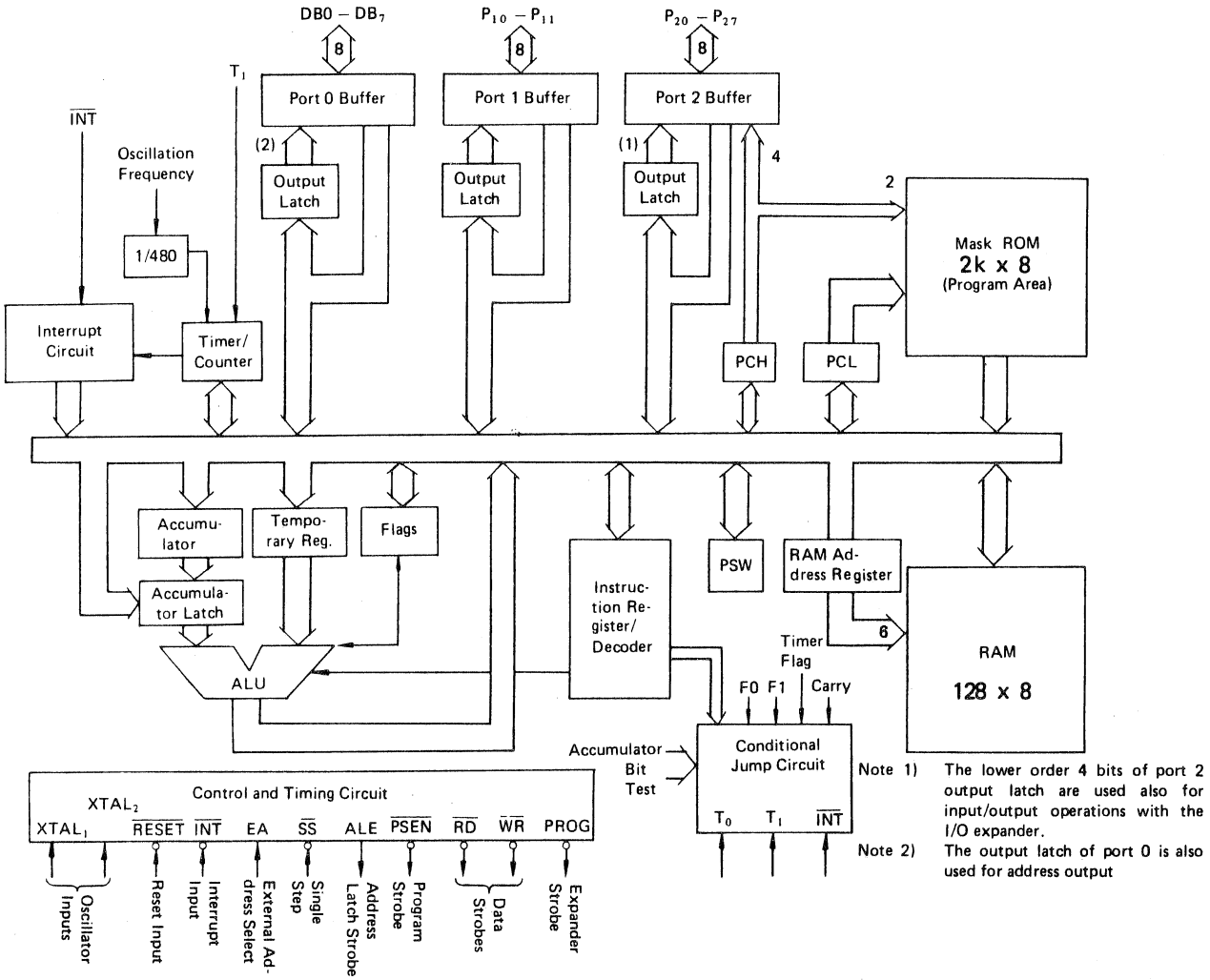
XTAL1 (Input)

One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)

Other side of crystal input.

BLOCK DIAGRAM



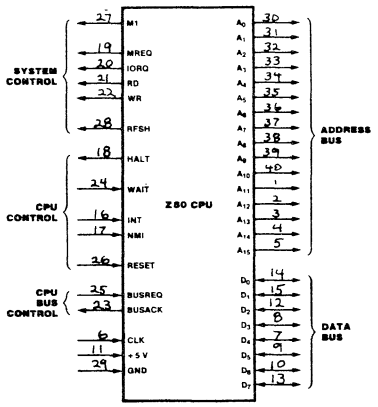
Note 1) The lower order 4 bits of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2) The output latch of port 0 is also used for address output

Zilog

Z8400
Z80® CPU Central Processing Unit

Features



Pin Descriptions

A_0-A_{15}. *Address Bus* (output, active High, 3-state). A_0–A_{15} form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

$\overline{BUSACK}$. *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ have entered their high-impedance states. The external circuitry can now control these lines.

$\overline{BUSREQ}$. *Bus Request* (input, active Low). Bus Request has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle. $\overline{BUSREQ}$ forces the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ to go to a high-impedance state so that other devices can control these lines. $\overline{BUSREQ}$ is normally wire-ORed and requires an external pullup for these applications. Extended $\overline{BUSREQ}$ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D_0-D_7. *Data Bus* (input/output, active High, 3-state). D_0–D_7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

$\overline{HALT}$. *Halt State* (output, active Low). $\overline{HALT}$ indicates that the CPU has executed a Halt instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

$\overline{INT}$. *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{INT}$ is normally wire-ORed and requires an external pullup for these applications.

$\overline{IORQ}$. *Input/Output Request* (output, active Low, 3-state). $\overline{IORQ}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. $\overline{IORQ}$ is also generated concurrently with $\overline{M1}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

$\overline{M1}$. *Machine Cycle One* (output, active Low). $\overline{M1}$, together with $\overline{MREQ}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{M1}$, together with $\overline{IORQ}$, indicates an interrupt acknowledge cycle.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{NMI}$. *Non-Maskable Interrupt* (input, active Low). $\overline{NMI}$ has a higher priority than $\overline{INT}$. $\overline{NMI}$ is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

$\overline{RD}$. *Memory Read* (output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{RESET}$. *Reset* (input, active Low). $\overline{RESET}$ initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that $\overline{RESET}$ must be active for a minimum of three full clock cycles before the reset operation is complete.

$\overline{RFSH}$. *Refresh* (output, active Low). $\overline{RFSH}$, together with $\overline{MREQ}$, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

$\overline{WAIT}$. *Wait* (input, active Low). $\overline{WAIT}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended $\overline{WAIT}$ periods can prevent the CPU from refreshing dynamic memory properly.

$\overline{WR}$. *Memory Write* (output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

Instruction Set

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the Z80 instruction set and shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. The *Z80 CPU Technical Manual* (03-0029-01) and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- ☐ 8-bit loads
- ☐ 16-bit loads
- ☐ Exchanges, block transfers, and searches
- ☐ 8-bit arithmetic and logic operations
- ☐ General-purpose arithmetic and CPU control
- ☐ 16-bit arithmetic operations
- ☐ Rotates and shifts
- ☐ Bit set, reset, and test operations
- ☐ Jumps
- ☐ Calls, returns, and restarts
- ☐ Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- ☐ Immediate
- ☐ Immediate extended
- ☐ Modified page zero
- ☐ Relative
- ☐ Extended
- ☐ Indexed
- ☐ Register
- ☐ Register indirect
- ☐ Implied
- ☐ Bit

8-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD r, r'	r ← r'	•	•	X	X	•	•	01 r r'		1	1	4	r, r' Reg.
LD r, n	r ← n	•	•	X	X	•	•	00 r 110 — n —		2	2	7	000 B 001 C
LD r, (HL)	r ← (HL)	•	•	X	X	•	•	01 r 110		1	2	7	010 D
LD r, (IX+d)	r ← (IX+d)	•	•	X	X	•	•	11 011 101 01 r 101 — d —	DD	3	5	19	011 E 100 H 101 L
LD r, (IY+d)	r ← (IY+d)	•	•	X	X	•	•	11 111 101 01 r 110 — d —	FD	3	5	19	111 A
LD (HL), r	(HL) ← r	•	•	X	X	•	•	01 110 r		1	2	7	
LD (IX+d), r	(IX+d) ← r	•	•	X	X	•	•	11 011 101 01 110 r — d —	DD	3	5	19	
LD (IY+d), r	(IY+d) ← r	•	•	X	X	•	•	11 111 101 01 110 r — d —	FD	3	5	19	
LD (HL), n	(HL) ← n	•	•	X	X	•	•	00 110 110 — n —	36	2	3	10	
LD (IX+d), n	(IX+d) ← n	•	•	X	X	•	•	11 011 101 00 110 110 — d — — n —	DD 36	4	5	19	
LD (IY+d), n	(IY+d) ← n	•	•	X	X	•	•	11 111 101 00 110 110 — d — — n —	FD 36	4	5	19	
LD A, (BC)	A ← (BC)	•	•	X	X	•	•	00 001 010	0A	1	2	7	
LD A, (DE)	A ← (DE)	•	•	X	X	•	•	00 011 010	1A	1	2	7	
LD A, (nn)	A ← (nn)	•	•	X	X	•	•	00 111 010 — n — — n —	3A	3	4	13	
LD (BC), A	(BC) ← A	•	•	X	X	•	•	00 000 010	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	X	•	•	00 010 010	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	X	•	•	00 110 010 — n — — n —	32	3	4	13	
LD A, I	A ← I	↕	↕	X	0	X	IFF	0 • 11 101 101 01 010 111	ED 57	2	2	9	
LD A, R	A ← R	↕	↕	X	0	X	IFF	0 • 11 101 101 01 011 111	ED 5F	2	2	9	
LD I, A	I ← A	•	•	X	•	X	•	• • 11 101 101 01 000 111	ED 47	2	2	9	
LD R, A	R ← A	•	•	X	•	X	•	• • 11 101 101 01 001 111	ED 4F	2	2	9	

NOTES: r, r' means any of the registers A, B, C, D, E, H, L.
IFF the content of the interrupt enable flip-flop, (IFF) is copied into the P/V flag.

For an explanation of flag notation and symbols for mnemonic tables, see Symbolic Notation section following tables.

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with whom the publisher is not associated."

16-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	•	•	X	•	X	•	•	•	00 dd0 001 ← n → ← n →	3	3	10	dd Pair 00 BC 01 DE 10 HL 11 SP
LD IX, nn	IX ← nn	•	•	X	•	X	•	•	•	11 011 101 DD 00 100 001 21 ← n → ← n →	4	4	14	
LD IY, nn	IY ← nn	•	•	X	•	X	•	•	•	11 111 101 FD 00 100 001 21 ← n → ← n →	4	4	14	
LD HL, (nn)	H ← (nn + 1) L ← (nn)	•	•	X	•	X	•	•	•	00 101 010 2A ← n → ← n →	3	5	16	
LD dd, (nn)	dd_H ← (nn + 1) dd_L ← (nn)	•	•	X	•	X	•	•	•	11 101 101 ED 01 dd1 011 ← n → ← n →	4	6	20	
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	•	•	X	•	X	•	•	•	11 011 101 DD 00 101 010 2A ← n → ← n →	4	6	20	
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	•	•	X	•	X	•	•	•	11 111 101 FD 00 101 010 2A ← n → ← n →	4	6	20	
LD (nn), HL	(nn + 1) ← H (nn) ← L	•	•	X	•	X	•	•	•	00 100 010 22 ← n → ← n →	3	5	16	
LD (nn), dd	(nn + 1) ← dd_H (nn) ← dd_L	•	•	X	•	X	•	•	•	11 101 101 ED 01 dd0 011 ← n → ← n →	4	6	20	
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	•	•	X	•	X	•	•	•	11 011 101 DD 00 100 010 22 ← n → ← n →	4	6	20	
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	•	•	X	•	X	•	•	•	11 111 101 FD 00 100 010 22 ← n → ← n →	4	6	20	
LD SP, HL	SP ← HL	•	•	X	•	X	•	•	•	11 111 001 F9	1	1	6	
LD SP, IX	SP ← IX	•	•	X	•	X	•	•	•	11 011 101 DD 11 111 001 F9	2	2	10	
LD SP, IY	SP ← IY	•	•	X	•	X	•	•	•	11 111 101 FD 11 111 001 F9	2	2	10	
PUSH qq	(SP − 2) ← qqL (SP − 1) ← qqH SP ← SP − 2	•	•	X	•	X	•	•	•	11 qq0 101	1	3	11	qq Pair 00 BC 01 DE 10 HL 11 AF
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H SP ← SP − 2	•	•	X	•	X	•	•	•	11 011 101 DD 11 100 101 E5	2	4	15	
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H SP ← SP − 2	•	•	X	•	X	•	•	•	11 111 101 FD 11 100 101 E5	2	4	15	
POP qq	qqH ← (SP + 1) qqL ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	•	11 qq0 001	1	3	10	
POP IX	IX_H ← (SP + 1) IX_L ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	•	11 011 101 DD 11 100 001 E1	2	4	14	
POP IY	IY_H ← (SP + 1) IY_L ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	•	11 111 101 FD 11 100 001 E1	2	4	14	

NOTES: dd is any of the register pairs BC, DE, HL, SP.
qq is any of the register pairs AF, BC, DE, HL.
$(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively.
e.g., BC_L = C, AF_H = A.

Exchange, Block Transfer, Block Search Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE ↔ HL	•	•	X	•	X	•	•	•	11 101 011 EB	1	1	4	
EX AF, AF'	AF ↔ AF'	•	•	X	•	X	•	•	•	00 001 000 08	1	1	4	
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	•	•	X	•	X	•	•	•	11 011 001 D9	1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	•	•	X	•	X	•	•	•	11 100 011 E3	1	5	19	
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	•	•	X	•	X	•	•	•	11 011 101 DD 11 100 011 E3	2	6	23	
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	•	•	X	•	X	•	•	•	11 111 101 FD 11 100 011 E3	2	6	23	
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	•	•	X	① 0	X	↕	0	•	11 101 101 ED 10 100 000 A0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	0	0	•	11 101 101 ED 10 110 000 B0	2 2	5 4	21 16	If BC ≠ 0 If BC = 0

NOTE: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.

Exchange, Block Transfer, Block Search Groups (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	•	•	X	① 0	X	↕	0	•	11 101 101 ED 10 101 000 A8	2	4	16	
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	① 0	0	•	11 101 101 ED 10 111 000 B8	2 2	5 4	21 16	If BC ≠ 0 If BC = 0
CPI	A − (HL) HL ← HL + 1 BC ← BC − 1	↕	② ↕	X	↕	X	① ↕	1	•	11 101 101 ED 10 100 001 A1	2	4	16	
CPIR	A − (HL) HL ← HL + 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	② ↕	X	↕	X	① ↕	1	•	11 101 101 ED 10 110 001 B1	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	↕	② ↕	X	↕	X	① ↕	1	•	11 101 101 ED 10 101 001 A9	2	4	16	
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	② ↕	X	↕	X	① ↕	1	•	11 101 101 ED 10 111 001 B9	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)

NOTES: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.
② Z flag is 1 if A = (HL), otherwise Z = 0.

8-Bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A + r	↕	↕	X	↕	X	V	0	↕	10 000 r	1	1	4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
ADD A, n	A ← A + n	↕	↕	X	↕	X	V	0	↕	11 000 110 ← n →	2	2	7	
ADD A, (HL)	A ← A + (HL)	↕	↕	X	↕	X	V	0	↕	10 000 110	1	2	7	
ADD A, (IX + d)	A ← A + (IX + d)	↕	↕	X	↕	X	V	0	↕	11 011 101 DD 10 000 110 ← d →	3	5	19	
ADD A, (IY + d)	A ← A + (IY + d)	↕	↕	X	↕	X	V	0	↕	11 111 101 FD 10 000 110 ← d →	3	5	19	
ADC A, s	A ← A + s + CY	↕	↕	X	↕	X	V	0	↕	001				s is any of r, n, (HL), (IX + d), (IY + d) as shown for ADD instruction. The indicated bits replace the 000 in the ADD set above.
SUB s	A ← A − s	↕	↕	X	↕	X	V	1	↕	010				
SBC A, s	A ← A − s − CY	↕	↕	X	↕	X	V	1	↕	011				
AND s	A ← A ∧ s	↕	↕	X	1	X	P	0	0	100				
OR s	A ← A ∨ s	↕	↕	X	0	X	P	0	0	110				
XOR s	A ← A ⊕ s	↕	↕	X	0	X	P	0	0	101				
CP s	A − s	↕	↕	X	↕	X	V	1	↕	111				
INC r	r ← r + 1	↕	↕	X	↕	X	V	0	•	00 r 100	1	1	4	
INC (HL)	(HL) ← (HL) + 1	↕	↕	X	↕	X	V	0	•	00 110 100	1	3	11	
INC (IX + d)	(IX + d) ← (IX + d) + 1	↕	↕	X	↕	X	V	0	•	11 011 101 DD 00 110 100 ← d →	3	6	23	
INC (IY + d)	(IY + d) ← (IY + d) + 1	↕	↕	X	↕	X	V	0	•	11 111 101 FD 00 110 100 ← d →	3	6	23	
DEC m	m ← m − 1	↕	↕	X	↕	X	V	1	•	101				m is any of r, (HL), (IX + d), (IY + d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

General-Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	Comments
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands.	↕	↕	X	X	P	•	↕ 00 100 111	27	1	1	4	Decimal adjust accumulator.
CPL	A ← $\overline{A}$	•	•	X	1	X	•	1 • 00 101 111	2F	1	1	4	Complement accumulator (one's complement).
NEG	A ← 0 − A	↕	↕	X	↕	V	1	↕ 11 101 101	ED	2	2	8	Negate acc. (two's complement).
								01 000 100	44				
CCF	CY ← $\overline{CY}$	•	•	X	X	•	0	↕ 00 111 111	3F	1	1	4	Complement carry flag.
SCF	CY ← 1	•	•	X	0	X	•	0 1 00 110 111	37	1	1	4	Set carry flag.
NOP	No operation	•	•	X	•	X	•	• • 00 000 000	00	1	1	4	
HALT	CPU halted	•	•	X	•	X	•	• • 01 110 110	76	1	1	4	
DI *	IFF ← 0	•	•	X	•	X	•	• • 11 110 011	F3	1	1	4	
EI *	IFF ← 1	•	•	X	•	X	•	• • 11 111 011	FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	• • 11 101 101	ED	2	2	8	
								01 000 110	46				
IM 1	Set interrupt mode 1	•	•	X	•	X	•	• • 11 101 101	ED	2	2	8	
								01 010 110	56				
IM 2	Set interrupt mode 2	•	•	X	•	X	•	• • 11 101 101	ED	2	2	8	
								01 011 110	5E				

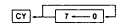
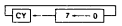
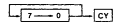
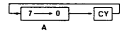
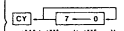
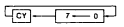
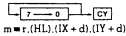
NOTES: IFF indicates the interrupt enable flip-flop.
CY indicates the carry flip flop.
* indicates interrupts are not sampled at the end of EI or DI.

16-Bit Arithmetic Group

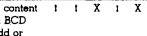
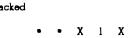
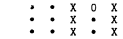
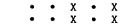
Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	Comments
ADD HL, ss	HL ← HL + ss	•	•	X	X	X	•	0 ↕ 00 ss1 001		1	3	11	ss Reg.: 00 BC, 01 DE, 10 HL, 11 SP
ADC HL, ss	HL ← HL + ss + CY	↕	↕	X	X	V	0	↕ 11 101 101	ED	2	4	15	
								01 ss1 010					
SBC HL, ss	HL ← HL − ss − CY	↕	↕	X	X	V	1	↕ 11 101 101	ED	2	4	15	
								01 ss0 010					
ADD IX, pp	IX ← IX + pp	•	•	X	X	X	•	0 ↕ 11 011 101	DD	2	4	15	pp Reg.: 00 BC, 01 DE, 10 IX, 11 SP
								00 pp1 001					
ADD IY, rr	IY ← IY + rr	•	•	X	X	X	•	0 ↕ 11 111 101	FD	2	4	15	rr Reg.: 00 BC, 01 DE, 10 IY, 11 SP
								00 rr1 001					
INC ss	ss ← ss + 1	•	•	X	•	X	•	• • 00 ss0 011		1	1	6	
INC IX	IX ← IX + 1	•	•	X	•	X	•	• • 11 011 101	DD	2	2	10	
								00 100 011	23				
INC IY	IY ← IY + 1	•	•	X	•	X	•	• • 11 111 101	FD	2	2	10	
								00 100 011	23				
DEC ss	ss ← ss − 1	•	•	X	•	X	•	• • 00 ss1 011		1	1	6	
DEC IX	IX ← IX − 1	•	•	X	•	X	•	• • 11 011 101	DD	2	2	10	
								00 101 011	2B				
DEC IY	IY ← IY − 1	•	•	X	•	X	•	• • 11 111 101	FD	2	2	10	
								00 101 011	2B				

NOTES: ss is any of the register pairs BC, DE, HL, SP
pp is any of the register pairs BC, DE, IX, SP
rr is any of the register pairs BC, DE, IY, SP

Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	Comments
RLCA		•	•	X	0	X	•	0 ↕ 00 000 111	07	1	1	4	Rotate left circular accumulator.
RLA		•	•	X	0	X	•	0 ↕ 00 010 111	17	1	1	4	Rotate left accumulator.
RRCA		•	•	X	0	X	•	0 ↕ 00 001 111	0F	1	1	4	Rotate right circular accumulator.
RRA		•	•	X	0	X	•	0 ↕ 00 011 111	1F	1	1	4	Rotate right accumulator.
RLC r		↕	↕	X	0	X	P	0 ↕ 11 001 011	CB	2	2	8	Rotate left circular register r.
								00 000 r					r Reg.: 000 B, 001 C, 010 D, 011 E, 100 H, 101 L, 111 A
RLC (HL)		↕	↕	X	0	X	P	0 ↕ 11 001 011	CB	2	4	15	
								00 000 110					
RLC (IX + d)	 r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0 ↕ 11 011 101	DD	4	6	23	
								11 001 011	CB				
								− d −					
								00 000 110					
RLC (IY + d)		↕	↕	X	0	X	P	0 ↕ 11 111 101	FD	4	6	23	
								11 001 011	CB				
								− d −					
								00 000 110					
RL m	 m = r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0 ↕ 010					Instruction format and states are as shown for RLC's. To form new opcode replace 000 of RLC's with shown code.
RRC m	 m = r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0 ↕ 001					

Rotate and Shift Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	Comments
RR m	 m = r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0 ↕ 011					
SLA m	 m = r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0 ↕ 100					
SRA m	m = r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0 ↕ 101					
SRL m	m = r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0 ↕ 111					
RLD		↕	↕	X	0	X	P	0 • 11 101 101	ED	2	5	18	Rotate digit left and right between the accumulator and location (HL).
								01 101 111	6F				
RRD		↕	↕	X	0	X	P	0 • 11 101 101	ED	2	5	18	The content of the upper half of the accumulator is unaffected.
								01 100 111	67				

Bit Set, Reset and Test Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	Comments
BIT b, r	Z ← $\overline{(r)_b}$	X	↕	X	1	X	X	0 • 11 001 011	CB	2	2	8	r Reg.: 000 B, 001 C, 010 D, 011 E, 100 H, 101 L, 111 A
								01 b r					b Bit Tested: 000 0, 001 1, 010 2, 011 3, 100 4, 101 5, 110 6, 111 7
BIT b, (HL)	Z ← $\overline{(HL)_b}$	X	↕	X	1	X	X	0 • 11 001 011	CB	2	3	12	
								01 b 110					
BIT b, (IX + d)$_b$	Z ← $\overline{(IX+d)_b}$	X	↕	X	1	X	X	0 • 11 011 101	DD	4	5	20	
								11 001 011	CB				
								− d −					
								01 b 110					
BIT b, (IY + d)$_b$	Z ← $\overline{(IY+d)_b}$	X	↕	X	1	X	X	0 • 11 111 101	FD	4	5	20	
								11 001 011	CB				
								− d −					
								01 b 110					
SET b, r	r_b ← 1	•	•	X	•	X	•	• • 11 001 011	CB	2	2	8	
								11 b r					
SET b, (HL)	$(HL)_b$ ← 1	•	•	X	•	X	•	• • 11 001 011	CB	2	4	15	
								11 b 110					
SET b, (IX + d)	$(IX+d)_b$ ← 1	•	•	X	•	X	•	• • 11 011 101	DD	4	6	23	
								11 001 011	CB				
								− d −					
								11 b 110					
SET b, (IY + d)	$(IY+d)_b$ ← 1	•	•	X	•	X	•	• • 11 111 101	FD	4	6	23	
								11 001 011	CB				
								− d −					
								11 b 110					
RES b, m	m_b ← 0 m = r, (HL), (IX + d), (IY + d)	•	•	X	•	X	•	• • 10					To form new opcode replace 11 of SET b, s with 10. Flags and time states for SET instruction.

NOTES: The notation m_b indicates bit b (0 to 7) of location m.

Jump Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	Comments
JP nn	PC ← nn	•	•	X	•	X	•	• • 11 000 011	C3	3	3	10	
								← n →					
								← n →					
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	• • 11 cc 010		3	3	10	cc Condition: 000 NZ non-zero, 001 Z zero, 010 NC non-carry, 011 C carry, 100 PO parity odd, 101 PE parity even, 110 P sign positive, 111 M sign negative
								← n →					
								← n →					
JR e	PC ← PC + e	•	•	X	•	X	•	• • 00 011 000	18	2	3	12	
								← e − 2 →					
JR C, e	If C = 0, continue	•	•	X	•	X	•	• • 00 111 000	38	2	2	7	If condition not met.
								← e − 2 →					
	If C = 1, PC ← PC + e									2	3	12	If condition is met.
JR NC, e	If C = 1, continue	•	•	X	•	X	•	• • 00 110 000	30	2	2	7	If condition not met.
								← e − 2 →					
	If C = 0, PC ← PC + e									2	3	12	If condition is met.
JP Z, e	If Z = 0 continue	•	•	X	•	X	•	• • 00 101 000	28	2	2	7	If condition not met.
								← e − 2 →					
	If Z = 1, PC ← PC + e									2	3	12	If condition is met.
JR NZ, e	If Z = 1, continue	•	•	X	•	X	•	• • 00 100 000	20	2	2	7	If condition not met.
								← e − 2 →					
	If Z = 0, PC ← PC + e									2	3	12	If condition is met.
JP (HL)	PC ← HL	•	•	X	•	X	•	• • 11 101 001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	• • 11 011 101	DD	2	2	8	
								11 101 001	E9				

Jump Group (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101 FD 11 101 001 E9	2	2	8	
DJNZ, e	B ← B − 1 If B = 0, continue If B ≠ 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 010 000 10 — e − 2 —	2 2	2 3	8 13	If B = 0. If B ≠ 0.

NOTES: e represents the extension in the relative addressing mode
e is a signed two's complement number in the range < − 126, 129 >
e − 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e

Call and Return Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	•	•	X	•	X	•	•	•	11 001 101 CD — n — — n —	3	5	17	
CALL cc, nn	If condition cc is false continue, otherwise same as CALL nn	•	•	X	•	X	•	•	•	11 cc 100 — n — — n —	3 3	3 5	10 17	If cc is false. If cc is true.
RET	PC_L ← (SP) PC_H ← (SP + 1)	•	•	X	•	X	•	•	•	11 001 001 C9	1	3	10	
RET cc	If condition cc is false continue, otherwise same as RET	•	•	X	•	X	•	•	•	11 cc 000	1 1	1 3	5 11	If cc is false. If cc is true.
RETI	Return from interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 001 101 4D	2	4	14	
RETN[1]	Return from non-maskable interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 000 101 45	2	4	14	
RST p	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0 PC_L ← p	•	•	X	•	X	•	•	•	11 t 111	1	3	11	

cc	Condition
000	NZ non-zero
001	Z zero
010	NC non-carry
011	C carry
100	PO parity odd
101	PE parity even
110	P sign positive
111	M sign negative

t	p
000	00H
001	08H
010	10H
011	18H
100	20H
101	28H
110	30H
111	38H

NOTE: [1]RETN loads IFF_2 → IFF_1

Input and Output Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A, (n)	A ← (n)	•	•	X	•	X	•	•	•	11 011 011 DB — n —	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
IN r, (C)	r ← (C) if r = 110 only the flags will be affected	↕	↕	X	↕	X	P	0	•	11 101 101 ED 01 r 000	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	X	↕ ①	X	X	X	X	1	•	11 101 101 ED 10 100 010 A2	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	1 ①	X	X	X	X	1	•	11 101 101 ED 10 110 010 B2	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
IND	(HL) ← (C) B ← B − 1 HL ← HL − 1	X	↕ ①	X	X	X	X	1	•	11 101 101 ED 10 101 010 AA	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 Repeat until B = 0	X	1 ①	X	X	X	X	1	•	11 101 101 ED 10 111 010 BA	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUT (n), A	(n) ← A	•	•	X	•	X	•	•	•	11 010 011 D3 — n —	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
OUT (C), r	(C) ← r	•	•	X	•	X	•	•	•	11 101 101 ED 01 r 001	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	X	↕ ①	X	X	X	X	1	•	11 101 101 ED 10 100 011 A3	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	1 ①	X	X	X	X	1	•	11 101 101 ED 10 110 011 B3	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	X	↕ ①	X	X	X	X	1	•	11 101 101 ED 10 101 011 AB	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}

NOTE: ① If the result of B − 1 is zero the Z flag is set, otherwise it is reset.

Input and Output Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 Repeat until B = 0	X	↕	X	X	X	1	•	11 101 101 ED 10 111 011	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to A_0 ~ A_7 B to A_8 ~ A_{15}

Summary of Flag Operation

Instruction	D_7 S	Z	H	P/V	N	D_0 C	Comments
ADD A, s; ADC A, s	↕	↕	X	↕	X	V	0	↕	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	↕	↕	X	↕	X	V	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	↕	↕	X	1	X	P	0	0	Logical operations.
OR s, XOR s	↕	↕	X	0	X	P	0	0	
INC s	↕	↕	X	↕	X	V	0	•	8-bit increment.
DEC s	↕	↕	X	↕	X	V	1	•	8-bit decrement.
ADD DD, ss	•	•	X	X	X	•	0	↕	16-bit add.
ADC HL, ss	↕	↕	X	X	X	V	0	↕	16-bit add with carry.
SBC HL, ss	↕	↕	X	X	X	V	1	↕	16-bit subtract with carry.
RLA, RLCA, RRA; RRCA	•	•	X	0	X	•	0	↕	Rotate accumulator.
RL m; RLC m, RR m; RRC m; SLA m; SRA m; SRL m	↕	↕	X	0	X	P	0	↕	Rotate and shift locations.
RLD; RRD	↕	↕	X	0	X	P	0	•	Rotate digit left and right.
DAA	↕	↕	X	↕	X	P	•	↕	Decimal adjust accumulator.
CPL	•	•	X	1	X	•	1	•	Complement accumulator.
SCF	•	•	X	0	X	•	0	1	Set carry.
CCF	•	•	X	X	X	•	0	↕	Complement carry.
IN r (C)	↕	↕	X	0	X	P	0	•	Input register indirect.
INI, IND, OUTI, OUTD	X	↕	X	X	X	X	1	•	Block input and output. Z = 0 if B ≠ 0 otherwise Z = 0.
INIR; INDR; OTIR, OTDR	X	1	X	X	X	X	1	•	
LDI; LDD	X	X	X	0	X	↕	0	•	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR; LDDR	X	X	X	0	X	0	0	•	
CPI; CPIR; CPD; CPDR	X	↕	X	X	X	↕	1	•	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I; LD A, R	↕	↕	X	0	X	IFF	0	•	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
BIT b, s	X	↕	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag.

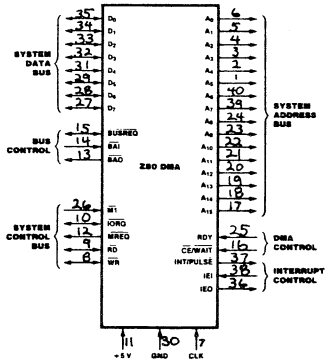
Symbolic Notation

Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.
Z	Zero flag. Z = 1 if the result of the operation is 0.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V = 1 if the result of the operation is even, P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow.
H	Half-carry flag. H = 1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N = 1 if the previous operation was a subtract.
H & N	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.

Symbol	Operation
↕	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range < 0, 255 >.
nn	16-bit value in range < 0, 65535 >.

Z8410
Z80® DMA Direct Memory Access Controller

Features



Pin Description

A_0-A_{15}. *System Address Bus* (output, 3-state). Addresses generated by the DMA are sent to both source and destination ports (main memory or I/O peripherals) on these lines.

$\overline{BAI}$. *Bus Acknowledge In* (input, active Low). Signals that the system buses have been released for DMA control. In multiple-DMA configurations, the $\overline{BAI}$ pin of the highest priority DMA is normally connected to the Bus Acknowledge pin of the CPU. Lower-priority DMAs have their $\overline{BAI}$ connected to the $\overline{BAO}$ of a higher-priority DMA.

$\overline{BAO}$. *Bus Acknowledge Out* (output, active Low). In a multiple-DMA configuration, this pin signals that no other higher-priority DMA has requested the system buses. $\overline{BAI}$ and $\overline{BAO}$ form a daisy chain for multiple-DMA priority resolution over bus control.

$\overline{BUSREQ}$. *Bus Request* (bidirectional, active Low, open drain). As an output, it sends requests for control of the system address bus, data bus and control bus to the CPU. As an input, when multiple DMAs are strung together in a priority daisy chain via $\overline{BAI}$ and $\overline{BAO}$, it senses when another DMA has requested the buses and causes this DMA to refrain from bus requesting until the other DMA is finished. Because it is a bidirectional pin, there cannot be any buffers between this DMA and any other DMA. It can, however, have a buffer between it and the CPU because it is unidirectional into the CPU. A pull-up resistor is connected to this pin.

$\overline{CE}$/$\overline{WAIT}$. *Chip Enable and Wait* (input, active Low). Normally this functions only as a $\overline{CE}$ line, but it can also be programmed to serve a $\overline{WAIT}$ function. As a $\overline{CE}$ line from the CPU, it becomes active when $\overline{WR}$ and $\overline{IORQ}$ are active and the I/O port address on the system address bus is the DMA's address, thereby allowing a transfer of control or command bytes from the CPU to the DMA. As a $\overline{WAIT}$ line from memory or I/O devices, after the DMA has received a bus-request acknowledge from the CPU, it causes wait states to be inserted in the DMA's operation cycles thereby slowing the DMA to a speed that matches the memory or I/O device.

CLK. *System Clock* (input). Standard Z-80 single-phase clock at 2.5 MHz (Z-80 DMA) or 4.0 MHz (Z-80A DMA). For slower system clocks, a TTL gate with a pullup resistor may be adequate to meet the timing and voltage level specification. For higher-speed systems, use a clock driver with an active pullup to meet the V_{IH} specification and risetime requirements. In all cases there should be a resistive pullup to the power supply of 10K ohms (max) to ensure proper power when the DMA is reset.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). Commands from the CPU, DMA status, and data from memory or I/O peripherals are transferred on these lines.

IEI. *Interrupt Enable In* (input, active High). This is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this DMA. Thus, this signal blocks lower-priority devices from interrupting while a higher-priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$/PULSE. *Interrupt Request* (output, active Low, open drain). This requests a CPU interrupt. The CPU acknowledges the interrupt by pulling its $\overline{IORQ}$ output Low during an $\overline{M1}$ cycle. It is typically connected to the $\overline{INT}$ pin of the CPU with a pullup resistor and tied to all other $\overline{INT}$ pins in the system. This pin can also be used to generate periodic pulses to an external device. It can be used this way only when the DMA is bus master (i.e., the CPU's $\overline{BUSREQ}$ and $\overline{BUSACK}$ lines are both Low and the CPU cannot see interrupts).

$\overline{IORQ}$. *Input/Output Request* (bidirectional, active Low, 3-state). As an input, this indicates that the lower half of the address bus holds a valid I/O port address for transfer of control or status bytes from or to the CPU, respectively; this DMA is the addressed port if its $\overline{CE}$ pin and its $\overline{WR}$ or $\overline{RD}$ pins are simultaneously active. As an output, after the DMA has taken control of the system buses, it indicates that the 8-bit or 16-bit address bus holds a valid port address for another I/O device involved in a DMA transfer of data. When $\overline{IORQ}$ and $\overline{M1}$ are both active simultaneously, an interrupt acknowledge is indicated.

$\overline{M1}$. *Machine Cycle One* (input, active Low). Indicates that the current CPU machine cycle is an instruction fetch. It is used by the DMA to decode the return-from-interrupt instruction (RETI) (ED-4D) sent by the CPU. During two-byte instruction fetches, $\overline{M1}$ is active as each opcode byte is fetched. An interrupt acknowledge is indicated when both $\overline{M1}$ and $\overline{IORQ}$ are active.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). This indicates that the address bus holds a valid address for a memory read or write operation. After the DMA has taken control of the system buses, it indicates a DMA transfer request from or to memory.

$\overline{RD}$. *Read* (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to read status bytes from the DMA's read registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled read from a memory or I/O port address.

RDY. *Ready* (input, programmable active Low or High). This is monitored by the DMA to determine when a peripheral device associated with a DMA port is ready for a read or write operation. Depending on the mode of DMA operation (Byte, Burst or Continuous), the RDY line indirectly controls DMA activity by causing the $\overline{BUSREQ}$ line to go Low or High.

$\overline{WR}$. *Write* (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to write control or command bytes to the DMA write registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled write to a memory or I/O port address.

Programming

The Z-80 DMA has two programmable fundamental states: (1) an enabled state, in which it can gain control of the system buses and direct the transfer of data between ports, and (2) a disabled state, in which it can initiate neither bus requests nor data transfers. When the DMA is powered up or reset by any means, it is automatically placed into the disabled state. Program commands can be written to it by the CPU in either state, but this automatically puts the DMA in the disabled state, which is maintained until an enable command is issued by the CPU. The CPU must program the DMA in advance of any data search or transfer by addressing it as an I/O port and sending a sequence of control bytes using an Output instruction (such as OTIR for the Z-80 CPU).

Writing. Control or command bytes are written into one or more of the Write Register groups (WR0-WR6) by first writing to the base register byte in that group. All groups have base registers and most groups have additional associated registers. The associated registers in a group are sequentially accessed by first writing a byte to the base register containing register-group identification and pointer bits (1's) to one or more of that base register's associated registers.

This is illustrated in Figure 8b. In this figure, the sequence in which associated registers within a group can be written to is shown by the vertical position of the associated registers. For example, if a byte written to the DMA contains the bits that identify WR0 (bits D0, D1 and D7), and also contains 1's in the bit positions that point to the associated "Port A Starting Address (low byte)" and "Port A Starting Address (high byte)," then the next two bytes written to the DMA will be stored in these two registers, in that order.

Reading. The Read Registers (RR0-RR6) are read by the CPU by addressing the DMA as an I/O port using an Input instruction (such as INIR for the Z-80 CPU). The readable bytes contain DMA status, byte-counter values, and port addresses since the last DMA reset. The registers are always read in a fixed sequence beginning with RR0 and ending with RR6. However, the register read in this sequence is determined by programming the Read Mask in WR6. The sequence of reading is initialized by writing an Initiate Read Sequence or Set Read Status command to WR6. After a Reset DMA, the sequence must be initialized with the Initiate Read Sequence command or a Read Status command. The sequence of reading all registers that are not excluded by the Read Mask register must be completed before a new Initiate Read Sequence or Read Status command.

Fixed-Address Programming. A special circumstance arises when programming a destination port to have a fixed address. The load command in WR6 only loads a fixed address to a port selected as the source, not to a port selected as the destination. Therefore, a fixed destination address must be loaded by temporarily declaring it a fixed-source address and subsequently declaring the true source as such, thereby implicitly making the other a destination.

The following example illustrates the steps in this procedure, assuming that transfers are to occur from a variable-address source (Port A) to a fixed-address destination (Port B):

1. Temporarily declare Port B as source in WR0.
2. Load Port B address in WR6.
3. Declare Port A as source in WR0.

Programming (Continued)

4. Load Port A address in WR6.
5. Enable DMA in WR6.

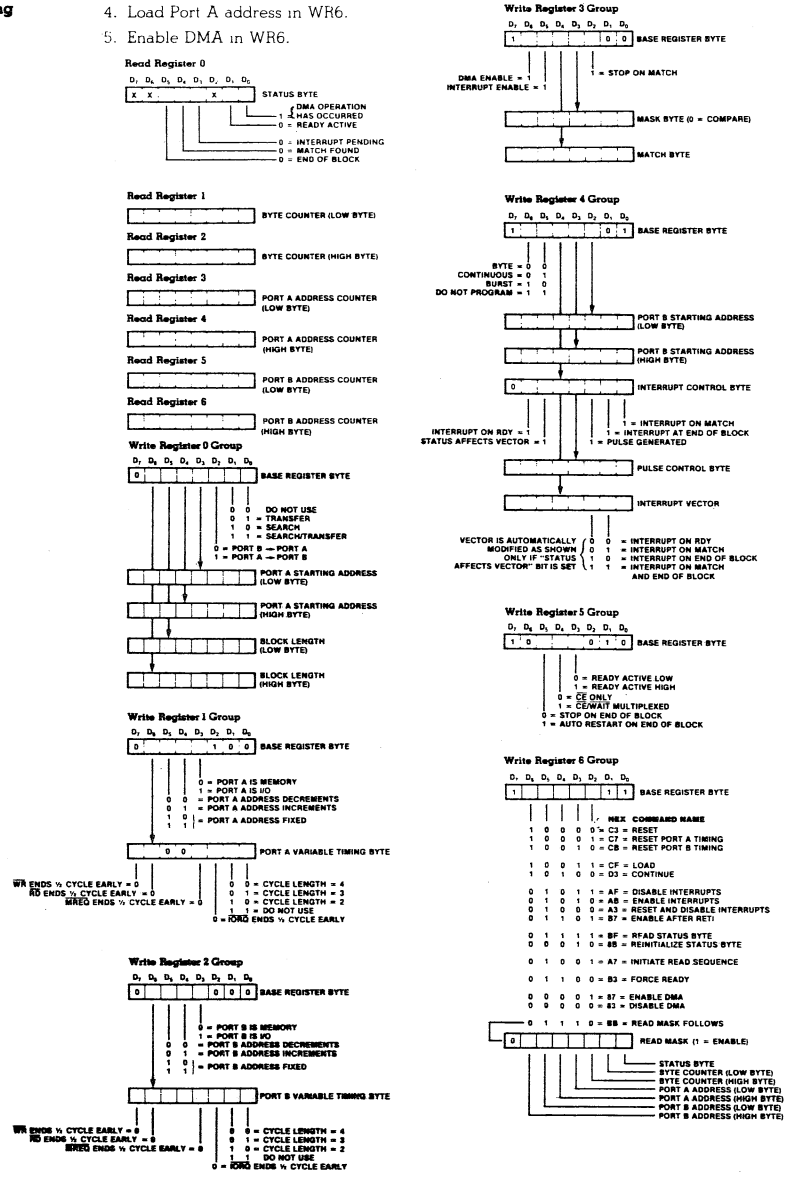
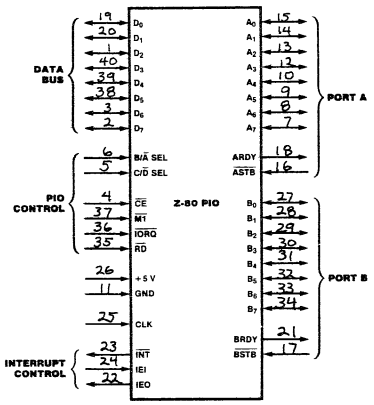


Figure 8b. Write Registers

Zilog

Z8420
Z80® PIO Parallel Input/Output Controller

Features



Pin Description

A_0-A_7. *Port A Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port A of the PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.

ARDY. *Register A Ready* (output, active High). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device.

Input Mode. This signal is active when the Port A input register is empty and ready to accept data from the peripheral device.

Bidirectional Mode. This signal is active when data is available in the Port A output register for transfer to the peripheral device. In this mode, data is not placed on the Port A data bus, unless $\overline{ASTB}$ is active.

Control Mode. This signal is disabled and forced to a Low state.

$\overline{ASTB}$. *Port A Strobe Pulse From Peripheral Device* (input, active Low). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO.

Input Mode. The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active.

Bidirectional Mode. When this signal is active, data from the Port A output register is gated onto the Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data.

Control Mode. The strobe is inhibited internally.

B_0-B_7. *Port B Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port B and a peripheral device. The Port B data bus can supply 1.5 mA at 1.5 V to drive Darlington transistors. B_0 is the least significant bit of the bus.

B/$\overline{A}$. *Port B Or A Select* (input, High = B). This pin defines which port is accessed during a data transfer between the CPU and the PIO. A Low on this pin selects Port A; a High selects Port B. Often address bit A_0 from the CPU is used for this selection function.

BRDY. *Register B Ready* (output, active High). This signal is similar to ARDY, except that in the Port A bidirectional mode this signal is High when the Port A input register is empty and ready to accept data from the peripheral device.

$\overline{BSTB}$. *Port B Strobe Pulse From Peripheral Device* (input, active Low). This signal is similar to $\overline{ASTB}$, except that in the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

C/$\overline{D}$. *Control Or Data Select* (input, High = C). This pin defines the type of data transfer to be performed between the CPU and the PIO. A High on this pin during a CPU write to the PIO causes the Z-80 data bus to be interpreted as a *command* for the port selected by the B/$\overline{A}$ Select line. A Low on this pin means that the Z-80 data bus is being used to transfer data between the CPU and the PIO. Often address bit A_1 from the CPU is used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally decoded from four I/O port numbers for Ports A and B, data, and control.

CLK. *System Clock* (input). The Z-80 PIO uses the standard single-phase Z-80 system clock.

D_0-D_7. *Z-80 CPU Data Bus* (bidirectional, 3-state). This bus is used to transfer all data and commands between the Z-80 CPU and the Z-80 PIO. D_0 is the least significant bit.

IEI. *Interrupt Enable In* (input, active High). This signal is used to form a priority-interrupt daisy chain when more than one interrupt-driven device is being used. A High level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

Pin Description (Continued)

IEO. *Interrupt Enable Out* (output, active High). The IEO signal is the other signal required to form a daisy chain priority scheme. It is High only if IEI is High and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When $\overline{INT}$ is active the Z-80 PIO is requesting an interrupt from the Z-80 CPU.

$\overline{IORQ}$. *Input/Output Request* (input from Z-80 CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{RD}$ to transfer commands and data between the Z-80 CPU and the Z-80 PIO. When $\overline{CE}$, $\overline{RD}$, and $\overline{IORQ}$ are active, the port addressed by B/$\overline{A}$ transfers data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not, the port addressed by B/$\overline{A}$ is written into from the CPU with either data or control information, as specified by C/$\overline{D}$. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt; the interrupting port automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. *Machine Cycle* (input from CPU, active Low). This signal is used as a sync pulse to control several internal PIO operations. When both the $\overline{M1}$ and $\overline{RD}$ signals are active, the Z-80 CPU is fetching an instruction from memory. Conversely, when both $\overline{M1}$ and $\overline{IORQ}$ are active, the CPU is acknowledging an interrupt. In addition, $\overline{M1}$ has two other functions within the Z-80 PIO: it synchronizes the PIO interrupt logic; when M1 occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal, the PIO is reset.

$\overline{RD}$. *Read Cycle Status* (input from Z-80 CPU, active Low). If $\overline{RD}$ is active, or an I/O operation is in progress, $\overline{RD}$ is used with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{IORQ}$ to transfer data from the Z-80 PIO to the Z-80 CPU.

Programming

Mode 0, 1, or 2. *(Byte Input, Output, or Bidirectional).* Programming a port for Mode 0, 1, or 2 requires two words per port. These words are:

A Mode Control Word. Selects the port operating mode (Figure 6). This word may be written any time.

An Interrupt Vector. The Z-80 PIO is designed for use with the Z-80 CPU in interrupt Mode 2 (Figure 7). When interrupts are enabled, the PIO must provide an interrupt vector.

Mode 3. *(Bit Input/Output).* Programming a port for Mode 3 operation requires a control word, a vector (if interrupts are enabled), and three additional words, described as follows:

I/O Register Control. When Mode 3 is selected, the mode control word must be followed by another control word that sets the I/O control register, which in turn defines which port lines are inputs and which are outputs (Figure 8).

Interrupt Control Word. In Mode 3, handshake is not used. Interrupts are generated as a logic function of the input signal levels. The interrupt control word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), and OR (if any one of the input bits changes to the active level, an interrupt is triggered). Bit D_6 sets the logic function, as shown in Figure 9. The active level of the input bits can be set either High or Low. The active level is controlled by Bit D_5.

Mask Control Word. This word sets the mask control register, allowing any unused bits to be masked off. If any bits are to be masked, then D_4 must be set. When D_4 is set, the next word written to the port must be a mask control word (Figure 10).

Interrupt Disable. There is one other control word which can be used to enable or disable a port interrupt. It can be used without changing the rest of the interrupt control word (Figure 11).

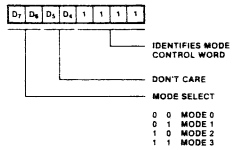


Figure 6. Mode Control Word

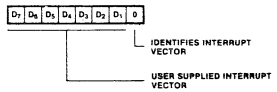


Figure 7. Interrupt Vector Word

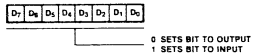


Figure 8. I/O Register Control Word

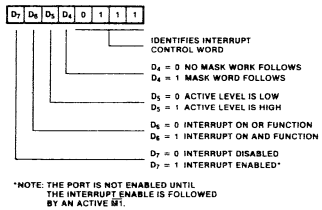


Figure 9. Interrupt Control Word

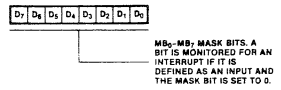


Figure 10. Mask Control Word

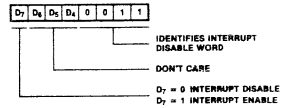
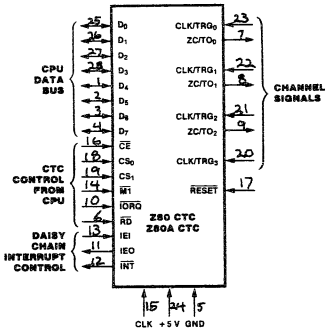


Figure 11. Interrupt Disable Word

Zilog

Z8430 Z80® CTC Counter/ Timer Circuit

Features



Pin Description

$\overline{CE}$. *Chip Enable* (input, active Low). When enabled the CTC accepts control words, interrupt vectors, or time constant data words from the data bus during an I/O write cycle; or transmits the contents of the down-counter to the CPU during an I/O read cycle. In most applications this signal is decoded from the eight least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter-timer channels.

CLK. *System Clock* (input). Standard single-phase Z-80 system clock.

CLK/TRG_0-CLK/TRG_3. *External Clock/Timer Trigger* (input, user-selectable active High or Low). Four pins corresponding to the four Z-80 CTC channels. In counter mode, every active edge on this pin decrements the down-counter. In timer mode, an active edge starts the timer.

CS_0-CS_1. *Channel Select* (inputs active High). Two-bit binary address code selects one of the four CTC channels for an I/O write or read (usually connected to A_0 and A_1).

D_0-D_7. *System Data Bus* (bidirectional, 3-state). Transfers all data and commands between the Z-80 CPU and the Z-80 CTC.

IEI. *Interrupt Enable In* (input, active High). A High indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z-80 CPU.

IEO. *Interrupt Enable Out* (output, active High). High only if IEI is High and the Z-80 CPU is not servicing an interrupt from any Z-80 CTC channel. IEO blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). Low when any Z-80 CTC channel that has been programmed to enable interrupts has a zero-count condition in its down-counter.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). Used with $\overline{CE}$ and $\overline{RD}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC. During a write cycle, $\overline{IORQ}$ and $\overline{CE}$ are active and $\overline{RD}$ inactive. The Z-80 CTC does not receive a specific write signal; rather, it internally generates its own from the inverse of an active $\overline{RD}$ signal. In a read cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ are active; the contents of the down-counter are read by the Z-80 CPU. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest priority interrupting channel places its interrupt vector on the Z-80 data bus.

$\overline{M1}$. *Machine Cycle One* (input from CPU, active Low). When $\overline{M1}$ and $\overline{IORQ}$ are active, the Z-80 CPU is acknowledging an interrupt. The Z-80 CTC then places an interrupt vector on the data bus if it has highest priority, and if a channel has requested an interrupt ($\overline{INT}$).

$\overline{RD}$. *Read Cycle Status* (input, active Low). Used in conjunction with $\overline{IORQ}$ and $\overline{CE}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC.

$\overline{RESET}$. *Reset* (input active Low). Terminates all down-counts and disables all interrupts by resetting the interrupt bits in all control registers; the ZC/TO and the Interrupt outputs go inactive; IEO reflects IEI; D_0-D_7 go to the high-impedance state.

ZC/TO_0-ZC/TO_2. *Zero Count/Timeout* (output, active High). Three ZC/TO pins corresponding to Z-80 CTC channels 2 through 0 (Channel 3 has no ZC/TO pin). In both counter and timer modes the output is an active High pulse when the down-counter decrements to zero.

Programming Each Z-80 CTC channel must be programmed prior to operation. Programming consists of writing two words to the I/O port that corresponds to the desired channel. The first word is a control word that selects the operating mode and other parameters; the second word is a time constant, which is a binary data word with a value from 1 to 256. A time constant word must be preceded by a channel control word.

After initialization, channels may be reprogrammed at any time. If updated control and time constant words are written to a channel during the count operation, the count continues to zero before the new time constant is loaded into the counter.

If the interrupt on any Z-80 CTC channel is enabled, the programming procedure should also include an interrupt vector. Only one vector is required for all four channels, because the interrupt logic automatically modifies the vector for the channel requesting service.

A control word is identified by a 1 in bit 0. A 0 in bit 2 indicates a time constant word is to follow. Interrupt vectors are always addressed to Channel 0, and identified by a 0 in bit 0.

Addressing. During programming, channels are addressed with the channel select pins CS_1 and CS_2. A 2-bit binary code selects the appropriate channel as shown in the following table.

Channel	CS_1	CS_0
0	0	0
1	0	1
2	1	0
3	1	1

Reset. The CTC has both hardware and software resets. The hardware reset terminates all down-counts and disables all CTC interrupts by resetting the interrupt bits in the control registers. In addition, the ZC/TO and Interrupt outputs go inactive, IEO reflects IEI, and D_0-D_7 go to the high-impedance state. All channels must be completely reprogrammed after a hardware reset.

The software reset is controlled by bit 1 in the channel control word. When a channel receives a software reset, it stops counting. When a software reset is used, the other bits in the control word also change the contents of the channel control register. After a software reset a new time constant word must be written to the same channel.

If the channel control word has both bits D_1 and D_2 set to 1, the addressed channel stops operating, pending a new time constant word. The channel is ready to resume after the new constant is programmed. In timer mode, if D_3 = 0, operation is triggered automatically when the time constant word is loaded.

Channel Control Word Programming. The channel control word is shown in Figure 5. It sets the modes and parameters described below.

Interrupt Enable. D_7 enables the interrupt, so that an interrupt output ($\overline{INT}$) is generated at zero count. Interrupts may be programmed in either mode and may be enabled or disabled at any time.

Operating Mode. D_6 selects either timer or counter mode.

Prescaler Factor. (Timer Mode Only). D_5 selects factor—either 16 or 256.

Trigger Slope. D_4 selects the active edge or slope of the CLK/TRG input pulses. Note that reprogramming the CLK/TRG slope during operation is equivalent to issuing an active edge. If the trigger slope is changed by a control word update while a channel is pending operation in timer mode, the result is the same as a CLK/TRG pulse and the timer starts. Similarly, if the channel is in counter mode, the counter decrements.

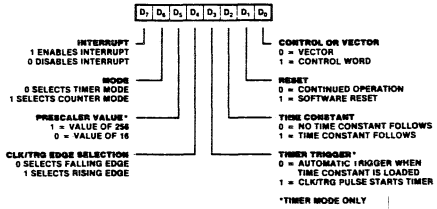


Figure 5. Channel Control Word

Programming (Continued)

Trigger Mode (Timer Mode Only). D_3 selects the trigger mode for timer operation. When D_3 is reset to 0, the timer is triggered automatically. The time constant word is programmed during an I/O write operation, which takes one machine cycle. At the end of the write operation there is a setup delay of one clock period. The timer starts automatically (decrements) on the rising edge of the second clock pulse (T_2) of the machine cycle following the write operation. Once started, the timer runs continuously. At zero count the timer reloads automatically and continues counting without interruption or delay, until stopped by a reset.

When D_3 is set to 1, the timer is triggered externally through the CLK/TRG input. The time constant word is programmed during an I/O write operation, which takes one machine cycle. The timer is ready for operation on the rising edge of the second clock pulse (T_2) of the following machine cycle. Note that the first timer decrement follows the active edge of the CLK/TRG pulse by a delay time of one clock cycle if a minimum setup time to the rising edge of clock is met. If this minimum is not met, the delay is extended by another clock period. Consequently, for immediate triggering, the CLK/TRG input must precede T_2 by one clock cycle plus its minimum setup time. If the minimum time is not met, the timer will start on the third clock cycle (T_3).

Once started the timer operates continuously, without interruption or delay, until stopped by a reset.

Time Constant to Follow. A 1 in D_2 indicates that the next word addressed to the selected channel is a time constant data word for the time constant register. The time constant word may be written at any time.

A 0 in D_2 indicates no time constant word is to follow. This is ordinarily used when the channel is already in operation and the new channel control word is an update. A channel will not operate without a time constant value. The only way to write a time constant value is to write a control word with D_2 set.

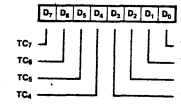


Figure 6. Time Constant Word

Software Reset. Setting D_1 to 1 causes a software reset, which is described in the Reset section.

Control Word. Setting D_0 to 1 identifies the word as a control word.

Time Constant Programming. Before a channel can start counting it must receive a time constant word from the CPU. During programming or reprogramming, a channel control word in which bit 2 is set must precede the time constant word to indicate that the next word is a time constant. The time constant word can be any value from 1 to 256 (Figure 6). Note that 00_{16} is interpreted as 256.

In timer mode, the time interval is controlled by three factors:

- The system clock period (ϕ)
- The prescaler factor (P), which multiplies the interval by either 16 or 256
- The time constant (T), which is programmed into the time constant register

Consequently, the time interval is the product of $\phi \times P \times T$. The minimum timer resolution is $16 \times \phi$ (4 μs with a 4 MHz clock). The maximum timer interval is $256 \times \phi \times 256$ (16.4 ms with a 4 MHz clock). For longer intervals timers may be cascaded.

Interrupt Vector Programming. If the Z-80 CTC has one or more interrupts enabled, it can supply interrupt vectors to the Z-80 CPU. To do so, the Z-80 CTC must be pre-programmed with the most-significant five bits of the interrupt vector. Programming consists of writing a vector word to the I/O port corresponding to the Z-80 CTC Channel 0. Note that D_0 of the vector word is always zero, to distinguish the vector from a channel control word. D_1 and D_2 are not used in programming the vector word. These bits are supplied by the interrupt logic to identify the channel requesting interrupt service with a unique interrupt vector (Figure 7). Channel 0 has the highest priority.

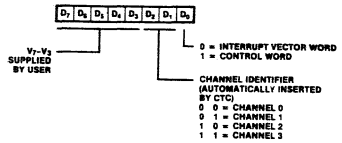
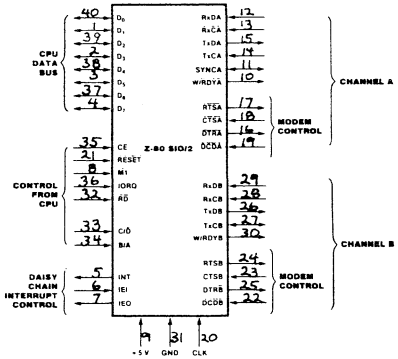


Figure 7. Interrupt Vector Word

Zilog

Z8440
Z80® SIO Serial Input/Output Controller

Features



Pin Description

Figures 1 through 6 illustrate the three pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- Z-80 SIO/2 lacks $\overline{SYNCB}$
- Z-80 SIO/1 lacks $\overline{DTRB}$
- Z-80 SIO/0 has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The first bonding option above (SIO/2) is the preferred version for most applications. The pin descriptions are as follows:

B/$\overline{A}$. *Channel A Or B Select* (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.

C/$\overline{D}$. *Control Or Data Select* (input, High selects Control). This input defines the type of information transfer performed between the CPU and the SIO. A High at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A Low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low level at this input enables the SIO to accept command or data input from the CPU during a write cycle or to transmit data to the CPU during a read cycle.

CLK. *System Clock* (input). The SIO uses the standard Z-80 System Clock to synchronize internal signals. This is a single-phase clock.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear To Send* (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). The system data bus transfers data and commands between the CPU and the Z-80 SIO. D_0 is the least significant bit.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffering does not guarantee a specific noise-level margin.

$\overline{DTRA}$, $\overline{DTRB}$. *Data Terminal Ready* (outputs, active Low). These outputs follow the state programmed into Z-80 SIO. They can also be programmed as general purpose outputs.

In the Z-80 SIO/1 bonding option, $\overline{DTRB}$ is omitted.

IEI. *Interrupt Enable In* (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When the SIO is requesting an interrupt, it pulls $\overline{INT}$ Low.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$ and $\overline{RD}$ to transfer commands and data between the CPU and the SIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$. If $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. *Machine Cycle* (input from Z-80 CPU, active Low). When $\overline{M1}$ is active and $\overline{RD}$ is also active, the Z-80 CPU is fetching an instruction from memory; when $\overline{M1}$ is active while $\overline{IORQ}$ is active, the SIO accepts $\overline{M1}$ and $\overline{IORQ}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z-80 CPU.

$\overline{RxCA}$, $\overline{RxCB}$. *Receiver Clocks* (inputs). Receive data is sampled on the rising edge of $\overline{RxC}$. The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).

In the Z-80 SIO/0 bonding option, $\overline{RxCB}$ is bonded together with $\overline{TxCB}$.

$\overline{RD}$. *Read Cycle Status* (input from CPU, active Low). If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with B/$\overline{A}$, $\overline{CE}$ and $\overline{IORQ}$ to transfer data from the SIO to the CPU.

RxDA, RxDB. *Receive Data* (inputs, active High). Serial data at TTL levels.

$\overline{RESET}$. *Reset* (input, active Low). A Low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.

$\overline{RTSA}$, $\overline{RTSB}$. *Request To Send* (outputs, active Low). When the RTS bit in Write Register 5 (Figure 14) is set, the $\overline{RTS}$ output goes Low. When the RTS bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{SYNCA}$, $\overline{SYNCB}$. *Synchronization* (inputs/outputs, active Low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 (Figure 13), but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven Low on the second rising edge of $\overline{RxC}$ after that rising edge of $\overline{RxC}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced Low, it should be kept Low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the Z-80 SIO/2 bonding option, $\overline{SYNCB}$ is omitted.

$\overline{TxCA}$, $\overline{TxCB}$. *Transmitter Clocks* (inputs). In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation.

In the Z-80 SIO/0 bonding option, $\overline{TxCB}$ is bonded together with $\overline{RxCB}$.

TxDA, TxDB. *Transmit Data* (outputs, active High). Serial data at TTL levels. TxD changes from the falling edge of $\overline{TxC}$.

$\overline{W}$/$\overline{RDYA}$, $\overline{W}$/$\overline{RDYB}$. *Wait/Ready A, Wait/Ready B* (outputs, open drain when programmed for Wait function, driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first; then the interrupt mode; and finally, receiver or transmitter enable.

Both channels contain registers that must be programmed via the system program prior to operation. The channel-select input (B/$\overline{A}$) and the control/data input (C/$\overline{D}$) are the command-structure addressing controls, and are normally controlled by the CPU address bus. Figures 15 and 16 illustrate the timing relationships for programming the write registers and transferring data and status.

Read Registers. The SIO contains three read registers for Channel B and two read registers for Channel A (RR0-RR2 in Figure 13) that can be read to obtain the status information; RR2 contains the internally-modifiable interrupt vector and is only in the Channel B register set. The status information includes error conditions, interrupt vector and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing a read instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occurred, all the appropriate error bits can be read from a single register (RR1).

Write Registers. The SIO contains eight write registers for Channel B and seven write registers for Channel A (WR0-WR7 in Figure 14) that are programmed separately to configure the functional personality of the channels; WR2 contains the interrupt vector for both channels and is only in the Channel B register set. With the exception of WR0, programming the write registers requires two bytes. The first byte is to WR0 and contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the SIO.

WR0 is a special case in that all of the basic commands can be written to it with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This implies that a channel reset must not be combined with the pointing to any register.

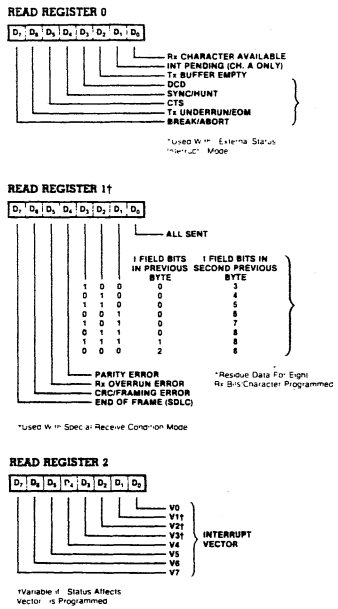


Figure 13. Read Register Bit Functions

Programming (Continued)

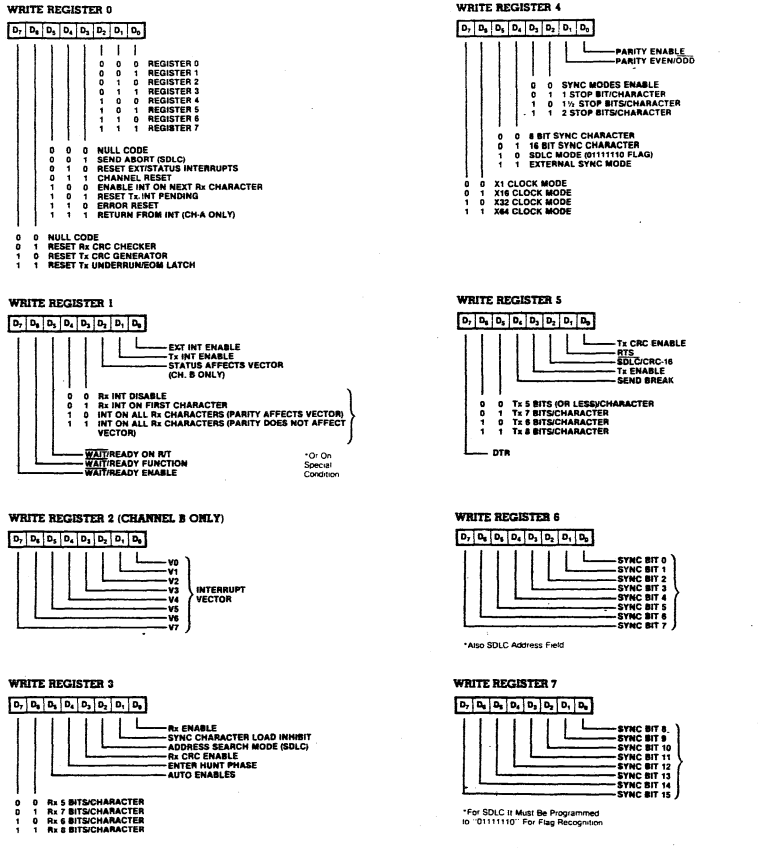


Figure 14. Write Register Bit Functions

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- ☐ Fully Programmable Display Format
  - Characters per Data Row (8-240)
  - Data Rows per Frame (2-256)
  - Raster Scans per Data Row (1-32)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (4-2048)
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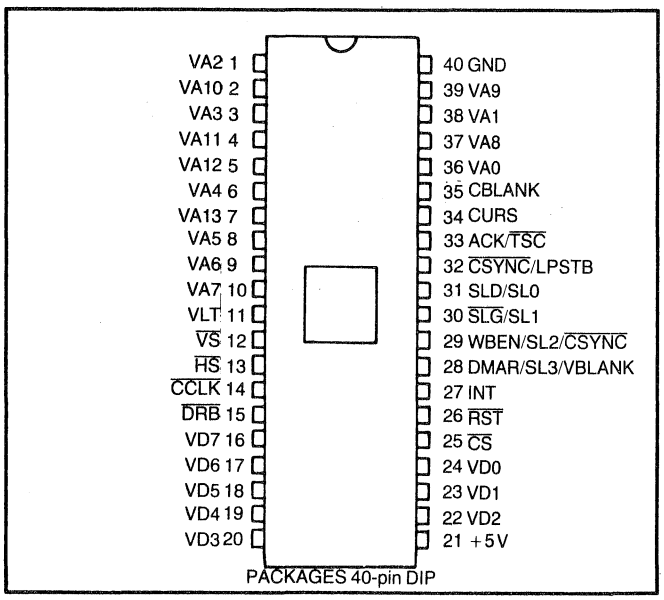
    — Vertical
  - Sync Width — Horizontal (1-128 Character Times)
    — Vertical (2-256 Scan Lines)
  - Back Porch — Horizontal
    — Vertical
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Composite Blanking
  - Cursor Coincidence
- ☐ Binary Addressing of Video Memory
- ☐ Row-Table Driven or Sequential Video Addressing Modes
- ☐ Programmable Status Row Position and Address Registers
- ☐ Bidirectional Partial or Full Page Smooth Scroll
- ☐ Attribute Assemble Mode
- ☐ Double Height Data Row Mode
- ☐ Double Width Data Row Mode
- ☐ Programmable DMA Burst Mode
- ☐ Configurable with a Variety of Memory Contention Arrangements
- ☐ Light Pen Register
- ☐ Cursor Horizontal and Vertical Position Registers
- ☐ Maskable Processor Interrupt Line
- ☐ Internal Status Register
- ☐ Three-state Video Memory Address Bus
- ☐ Partial or Full Page Blank Capability
- ☐ Two Interlace Modes: Enhanced Video and Alternate Scan Line

PIN CONFIGURATION



PACKAGES 40-pin DIP

- ☐ Ability to Delay Cursor and Blanking with respect to Active Video
- ☐ Programmable for Horizontal Split Screen Applications
- ☐ Graphics Compatible
- ☐ Ability to Externally Sync each Raster Line, each Field
- ☐ Single +5 Volt Power Supply
- ☐ TTL Compatible on All Inputs and Outputs
- ☐ VT-100 Compatible
- ☐ RS-170 Interlaced Composite Sync Available

GENERAL DESCRIPTION

The CRT 9007 VPAC™ is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC™ provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC™ works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006, a Double Row Buffer such as the CRT 9212, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC™ status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".

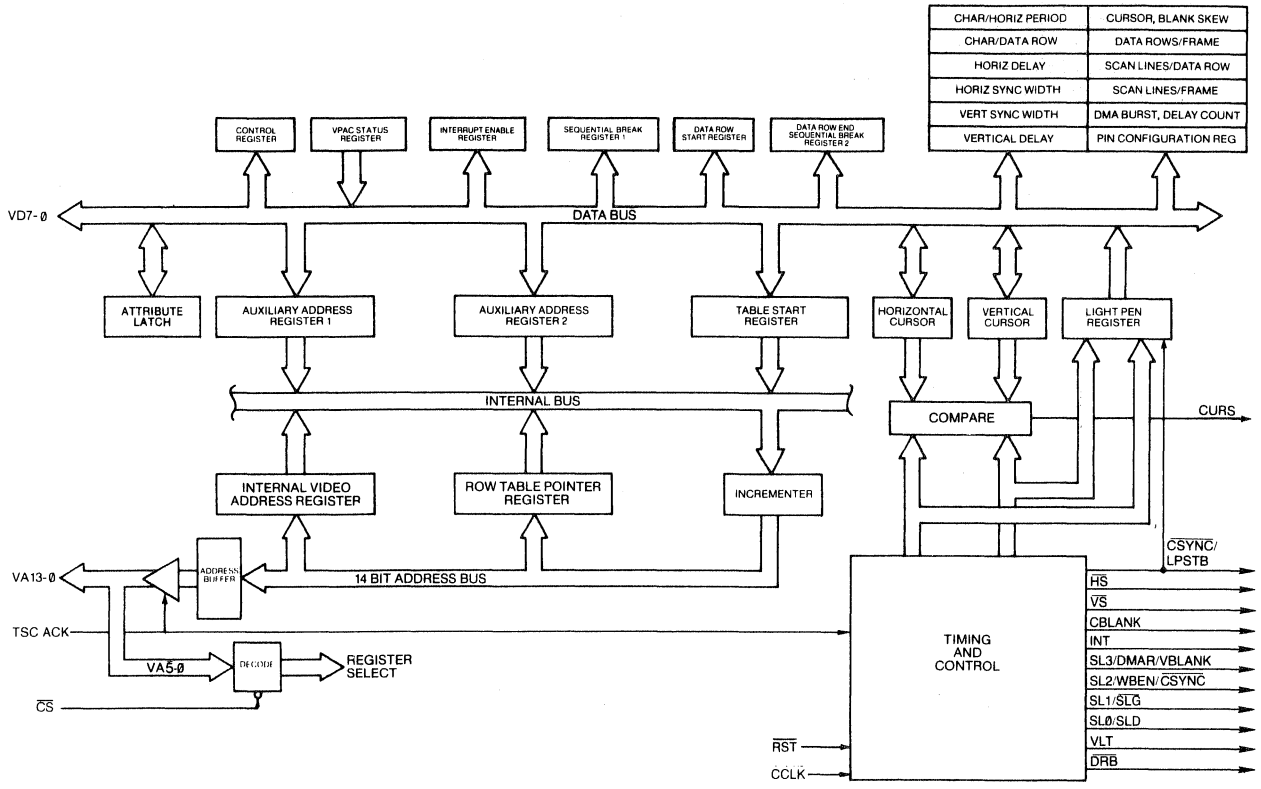


FIGURE 1: CRT 9007 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PROCESSOR INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
7, 5, 4, 2, 39, 37, 10, 9, 8, 6, 3, 1, 38, 36	Video Address 13-0	VA13-VA0	These 14 signals are the binary address presented to the video memory by the CRT 9007. The function depends on the particular CRT 9007 mode of operation. VA13-6 are outputs only. VA5-0 are bidirectional. —Double Row Buffer Configuration: VA13-0 are active outputs for the DMA operations and are in their high impedance state at all other times. —Single Row Buffer Configuration: VA13-0 are active outputs during the first scan line of each data row and are in their high impedance state at all other times. —Repetitive Memory Addressing Configuration: VA13-0 are active outputs at all times except during horizontal and vertical retrace at which time they are in their high impedance state. If row table addressing is used for either single row buffer or repetitive memory addressing modes, VA13-0 are active outputs during the horizontal retrace at each data row boundary to allow the CRT 9007 to retrieve the row table address. For processor read/write operations VA5-0 are inputs that select the appropriate internal register.
16, 17, 18, 19, 20, 22, 23, 24	Video Data 7-0	VD7-VD0	Bidirectional video data bus: during processor Read/write operations data is transferred via VD7-VD0 when chip strobe ($\overline{CS}$) is active. These lines are in their high impedance state when $\overline{CS}$ is inactive. During CRT 9007 DMA operations, data from video memory is input via VD7-VD0 when a new row table address is being retrieved or when the attribute latch is being updated in the attribute assemble mode. VD7-VD0 are outputs when the external row buffer is updated with a new attribute in the attribute assemble mode.
25	Chip strobe	$\overline{CS}$	Input; this signal when active low, allows the processor to read or write internal CRT 9007 registers. When reading from an internal CRT 9007 register, the chip strobe ($\overline{CS}$) enables the output drivers. When writing to an internal CRT 9007 register, the trailing edge of this signal latches the incoming data. Figure 2 shows all processor read/write timing.
26	Reset	$\overline{RST}$	Input; this active low signal puts the CRT 9007 into a known, inactive state and insures that the horizontal sync ($\overline{HS}$) output is inactive. Activating this input has the same effect as a RESET command. After initialization, a START command causes normal CRT 9007 operation. See processor addressable registers section, Register 16 for the reset state definition.
27	Interrupt	INT	Output; an interrupt to the processor from the CRT 9007 occurs when this signal is active high. The interrupt returns to its inactive low state when the status register is read.

DESCRIPTION OF PIN FUNCTIONS CONT'D

CRT INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
11	Visible Line Time	VLT	Output; this signal is active high during all visible scan lines and during the horizontal trace times at vertical retrace. This signal can be used to gate the character clock ($\overline{CCLK}$) when supplying data to a character generator from a single or double row buffer.
12	Vertical Sync	$\overline{VS}$	Open drain output; this signal determines the vertical position of displayed text by initiating a vertical retrace. Its position and pulse width are user programmable. The open drain allows the vertical frame rate to be synchronized to the line frequency when using monitors with DC coupled vertical amplifiers. If the $\overline{VS}$ output is pulled active low externally before the CRT 9007 itself initiates a vertical sync, the CRT 9007 will start its own vertical sync at the next leading edge of horizontal sync ($\overline{HS}$).
13	Horizontal Sync	$\overline{HS}$	Open drain output; this signal determines the horizontal position of displayed text by initiating a horizontal retrace. Its position and pulse width are user programmable. During hardware and software reset, this signal is inactive high. The open drain allows the horizontal scan rate to be synchronized to an external source. If the $\overline{HS}$ output is pulled low externally before the CRT 9007 itself initiates a horizontal sync, the CRT 9007 will start its own horizontal sync on the next character clock ($\overline{CCLK}$).
14	Character Clock	$\overline{CCLK}$	Input; this signal defines the character rate of the screen and is used by the CRT 9007 for all internal timing. A minimum high voltage of 4.3V must be maintained for proper chip operation.
15	Data Row Boundary	$\overline{DRB}$	Output; this signal is active low for one full scan line (from VLT trailing edge to VLT trailing edge) at the top scan line of each new data row. This signal can be used to swap buffers in the double row buffer mode. It indicates the particular horizontal retrace time that the CRT 9007 outputs addresses (VA13-VA0) for single row buffer operation.
34	Cursor	CURS	Output; this signal marks the cursor position on the screen as specified by the horizontal and vertical cursor registers. The signal is active for one character time at the particular character position for all scan lines within the data row. For double height or width characters, this signal is active for 2 consecutive $\overline{CCLK}$'s in every scan line within the data row. For double height characters, this signal can be programmed to be active at the proper position for 2 consecutive data rows. CURS is also used to signal either a double height or double width data row by becoming active during the horizontal retrace (CBLANK active) prior to a double height or double width scan line. The time of activation and deactivation is a function of the addressing mode, buffer configuration and the scan line number. See section of Double height/width for details.
35	Composite Blank	CBLANK	Output. This signal when active high, indicates that a retrace (either horizontal or vertical) will be performed. The signal remains active for the entire retrace interval as programmed. It is used to blank the video to a CRT.

USER SELECTABLE PINS: (see Tables 4 and 5)

PIN NO.	NAME	SYMBOL	FUNCTION
28, 29, 30, 31	Scan Line 3-Scan Line 0	SL3-SL0	Output; these 4 signals are the direct scan line counter outputs, in binary form, that indicate to the character generator the current scan line. These signals continue to be updated during the vertical retrace interval. SL3 and SLØ are the most and least significant bits respectively.
28	Direct Memory Access Request	DMAR	Output; this signal is the DMA request issued by the CRT 9007. It will only become active if the acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation.
28	Vertical Blank	VBLANK	Output; this signal is active high only during the vertical retrace period.
29	Write Buffer Enable	WBEN	Output; this active high signal is used to gate the clock feeding the write buffer in a double row buffer configuration.
29 or 32	Composite Sync	$\overline{CSYNC}$	Output; this signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and noninterlace formats. Figure 3 illustrates the $\overline{CSYNC}$ output in both interlaced and noninterlaced formats.
30	Scan Line Gate	$\overline{SLG}$	Output; this active low signal is used as a clock gate. It captures the correct 5 or 6 $\overline{CCLK}$'s and, in conjunction with $\overline{SLD}$ (pin 31), allows scan line information to be loaded serially into an external shift register.
31	Scan Line Data	$\overline{SLD}$	Output; this signal allows one to load an external shift register with the current scan line count. The count is presented least significant to most significant bit during the 5 or 6 $\overline{CCLK}$'s framed by $\overline{SLG}$. With this form of scan line representation, it is possible to define up to 32 scan lines per data row. The external shift register must be at least 5 bits in length. Even though 6 shifts can occur one should only use the 5 last bits shifted to define the scan line count. The extra shift occurs in interlace or double height character mode to allow the scan line count to be adjusted to its proper value. Figures 4 and 5 illustrate the serial scan line timing.
32	Light Pen Strobe	LPSTB	Input; this signal strobes the current row/column position into the light pen register at its positive transition.
33	Acknowledge	ACK	Input; this active high signal acknowledges a DMA request. It indicates that the processor bus has entered its high impedance state and the CRT 9007 may access video memory. It is not recommended to deactivate this signal during a CRT 9007 DMA cycle because the CRT 9007 will not shut down in a predictable amount of time.
33	Three State Control	$\overline{TSC}$	Input; this signal, when active low, places VA13-VAØ in their high impedance state.

Single Row Buffer Operation

The CRT 9007 configured with a CRT 9006 Single Row Buffer is shown in figure 6. The use of the CRT 9006 Single Row Buffer requires that the buffer be loaded at the video painting rate during the top scan line of each data row. However, after the CRT 9006 is loaded, the CRT 9007 address lines enter their high impedance state for the remaining N-1 scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentage of total memory cycles available to the processor is approximately [(N-1)/N] × 100 where N is the total number of scan lines per data row. For a typical system with 12 scan lines per data row this percentage is 92%. Figure 7 illustrates typical timing for the CRT 9007 used with the CRT 9006 Single Row Buffer.

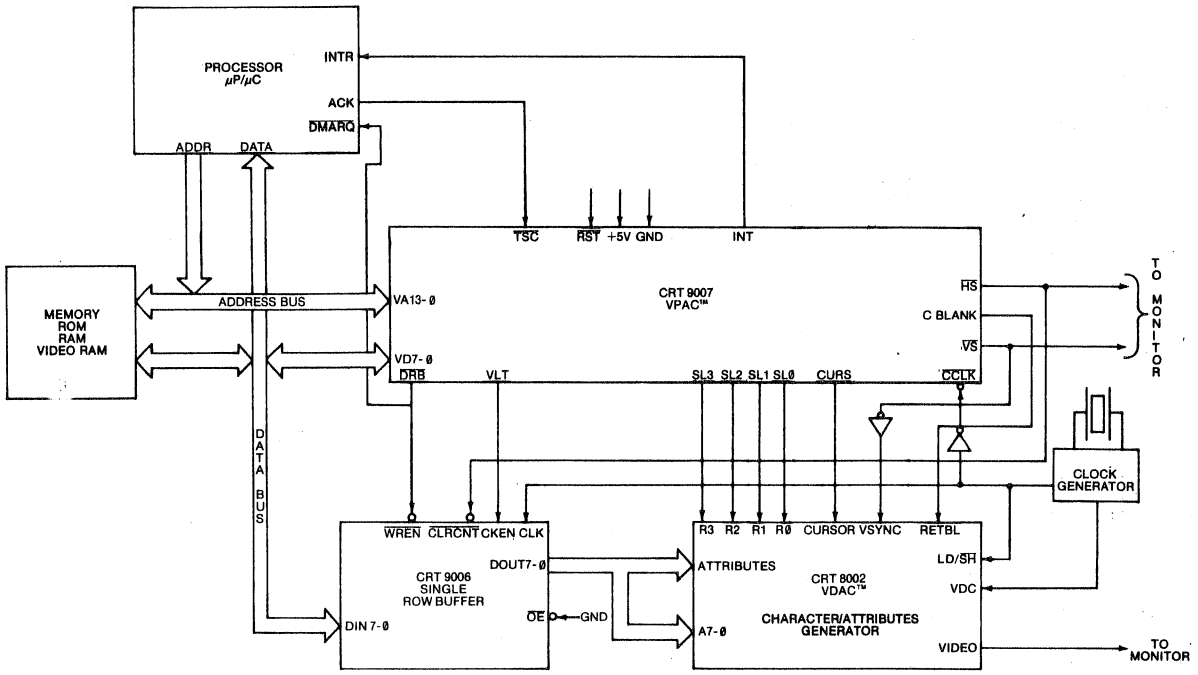


FIGURE 6: CRT 9007 CONFIGURATION WITH SINGLE ROW BUFFER

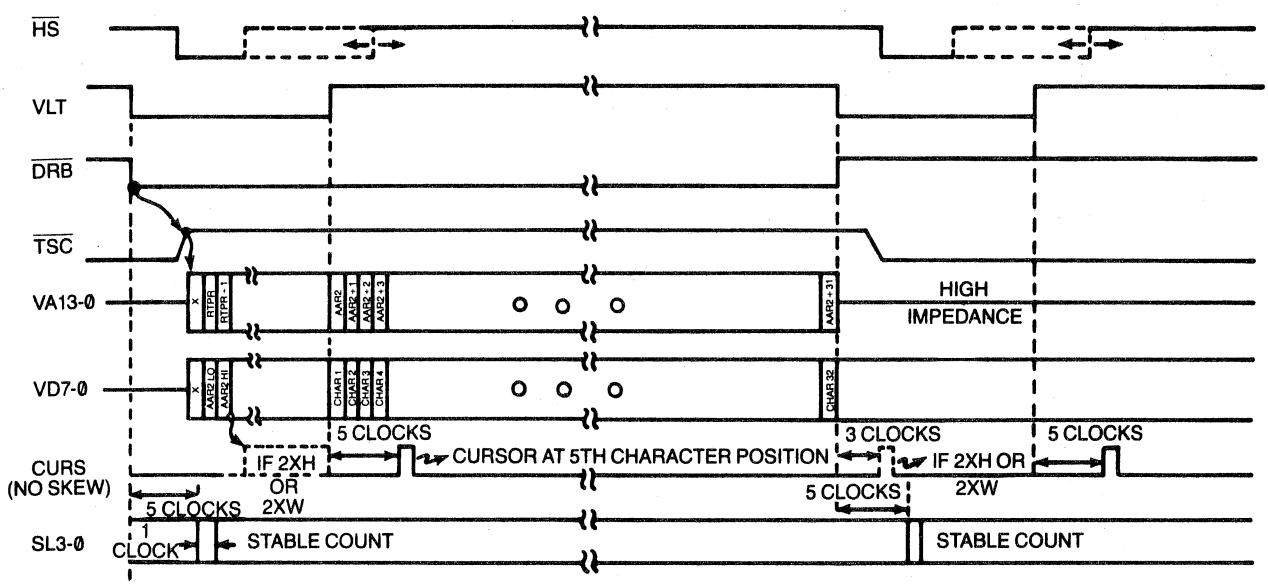


FIGURE 7: CRT 9007 SINGLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

Double Row Buffer Operation

Figure 8 shows the CRT 9007 used in conjunction with a CRT 9212 Double Row Buffer. The Double Row Buffer has a read buffer which is read at the painting rate of the CRT during each scan line in the data row. While the read buffer is being read and supplying data to the character generator for the current displayed data row, the write buffer is being loaded with the next data row to be displayed. This arrangement allows for relaxed write timing to the write buffer as it may be filled in the time it takes for N scan lines on the CRT to be painted where N is the number of scan lines per data row. Used in this configuration, the CRT 9007 takes advantage of the relaxed write buffer timing by stealing memory cycles from the processor to fill the write buffer (Direct memory access operation). The CRT 9007 sends the DMAR (DMA request) signal, awaits an ACK (acknowledge) signal and then drives out on VA13-VA0 the address at which the next video data resides. The CRT 9007 then activates the WBEN (write buffer enable) signal to write the data into the buffer. If for example there are 80 characters per data row, the CRT 9007 performs 80 DMA operations. The user has the ability to program the number of DMA cycles performed during each DMAR-ACK sequence, as well as the delay between each DMAR-ACK sequence, via the DMA CONTROL REGISTER (RA). If 8 DMA operations are performed for each ACK received, 10 such DMAR-ACK sequences must be performed to completely fill the write buffer. The programmed delay allows the user to evenly distribute the DMA operations so as not to hold up the processor for an excessive length of time. This feature also permits other DMA devices to be used and allows the processor to respond to real time events. In addition, the user has the ability to disable the CRT 9007 DMA mechanism. Figure 9 illustrates typical timing for the CRT 9007 used with the CRT 9212 Double Row Buffer.

Since the CRT 9212 Double Row Buffer has separate inputs for read and write clocks ($\overline{RCLK}$, $\overline{WCLK}$), it is possible to display proportional character widths (variable number of dots per character) by reading out the buffer at a character clock rate determined by the particular character. The writing of the buffer can be clocked from a different and constant character clock. Figure 10 illustrates the CRT 9007 used with two double row buffers and a CRT 9021 Video Attributes Controller chip to provide proportional character display.

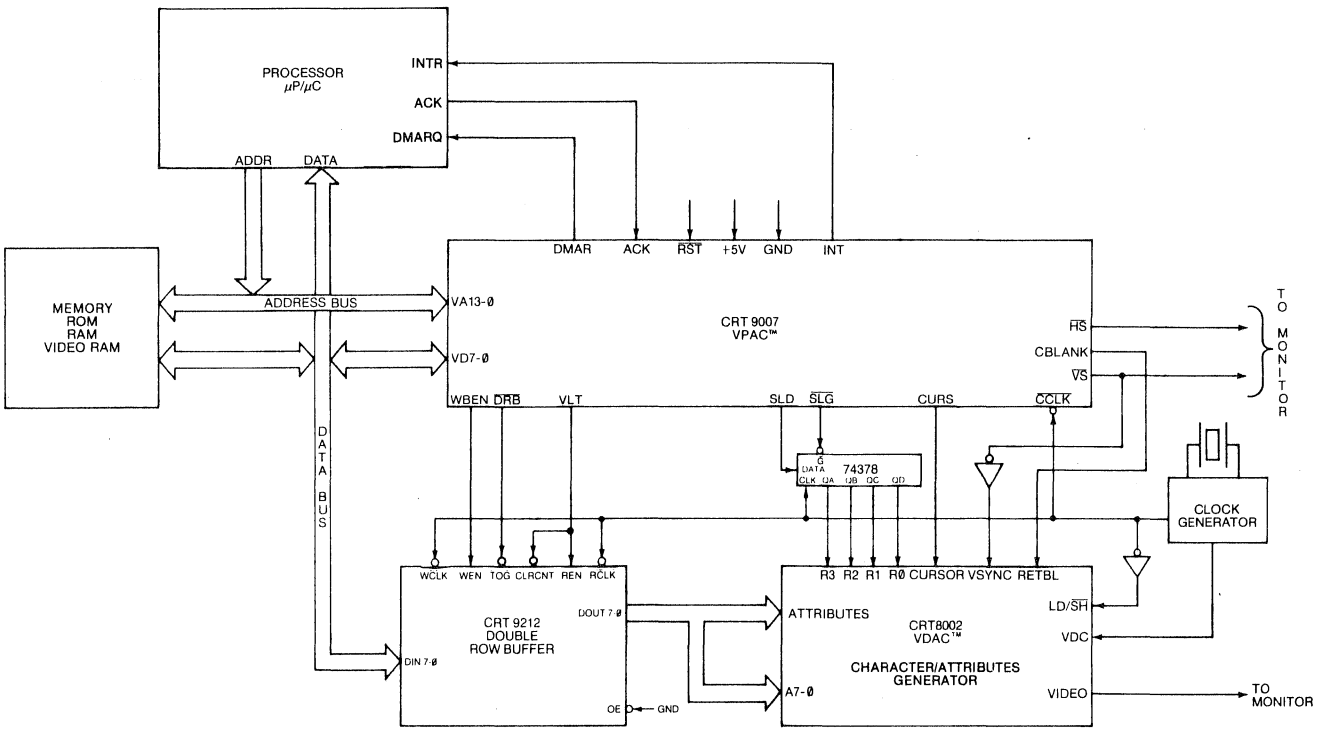


FIGURE 8: CRT 9007 CONFIGURATION WITH DOUBLE ROW BUFFER

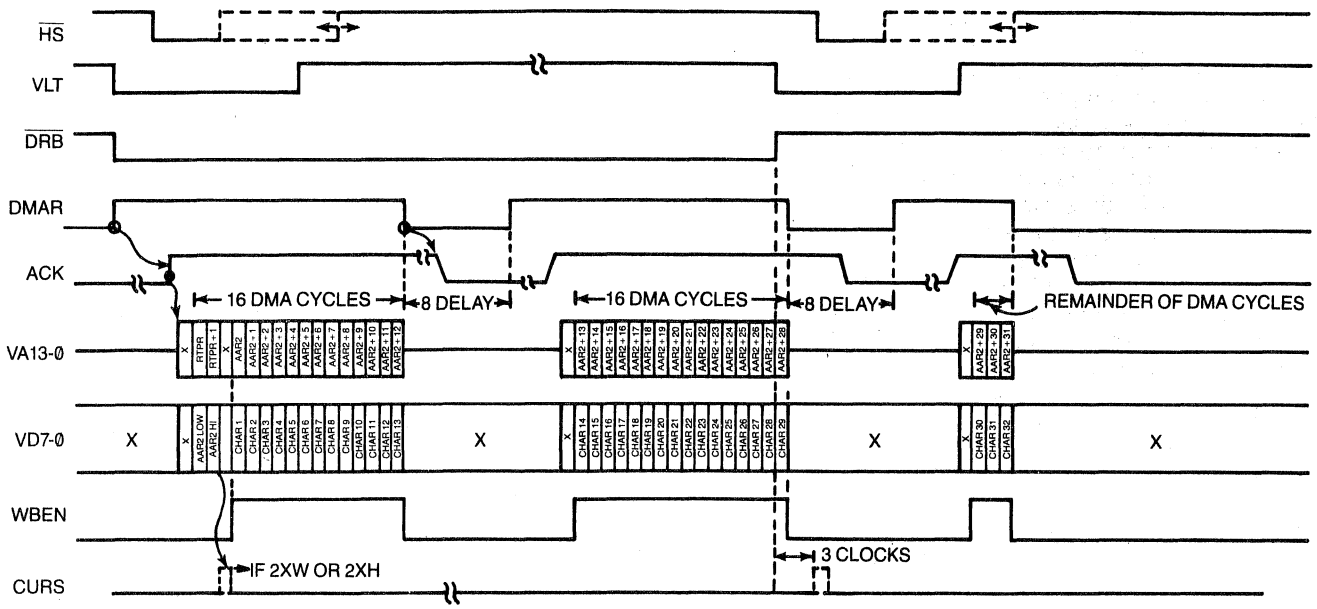


FIGURE 9: CRT 9007 DOUBLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

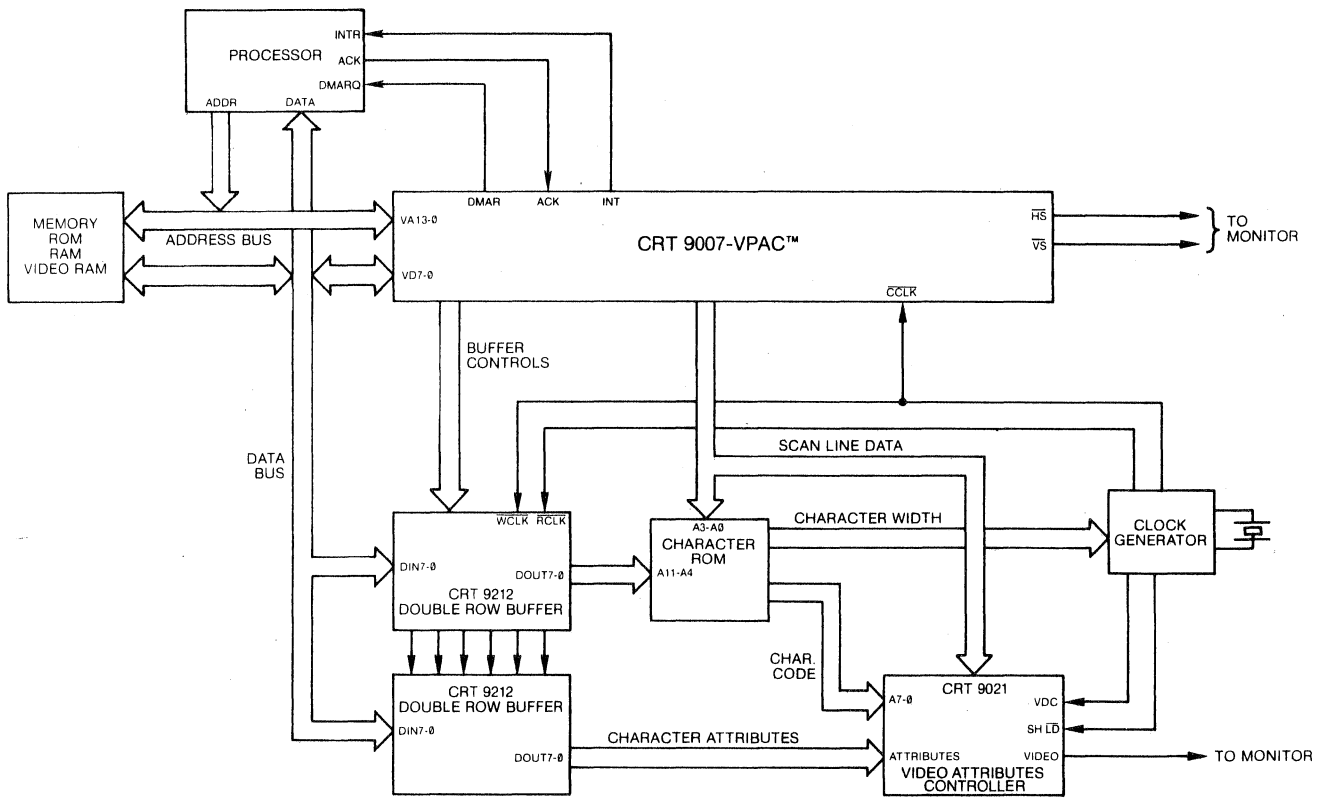


FIGURE 10: CRT 9007 CONFIGURATION FOR PROPORTIONAL CHARACTER DISPLAY

Repetitive Memory Addressing Operation

In this operation mode, the CRT 9007 will repeat the sequence of video addresses for every scan line of every data row. The CRT 9007 address bus will enter its high impedance state during all horizontal retrace intervals (except the retrace interval at a data row boundary if the CRT 9007 is configured in a row driven addressing mode). This arrangement allows for such low end contention schemes as retrace intervention (the processor is only allowed access to video memory during retrace intervals) and processor priority (the processor has an unlimited access to video memory). A high end contention scheme can be employed which uses a double speed memory such that in a single character period both the processor and the CRT 9007 are permitted access to video memory at predetermined time slots. Figure 11 illustrates the CRT 9007 configured with a double speed memory. Typical timing for this mode is illustrated in figure 12.

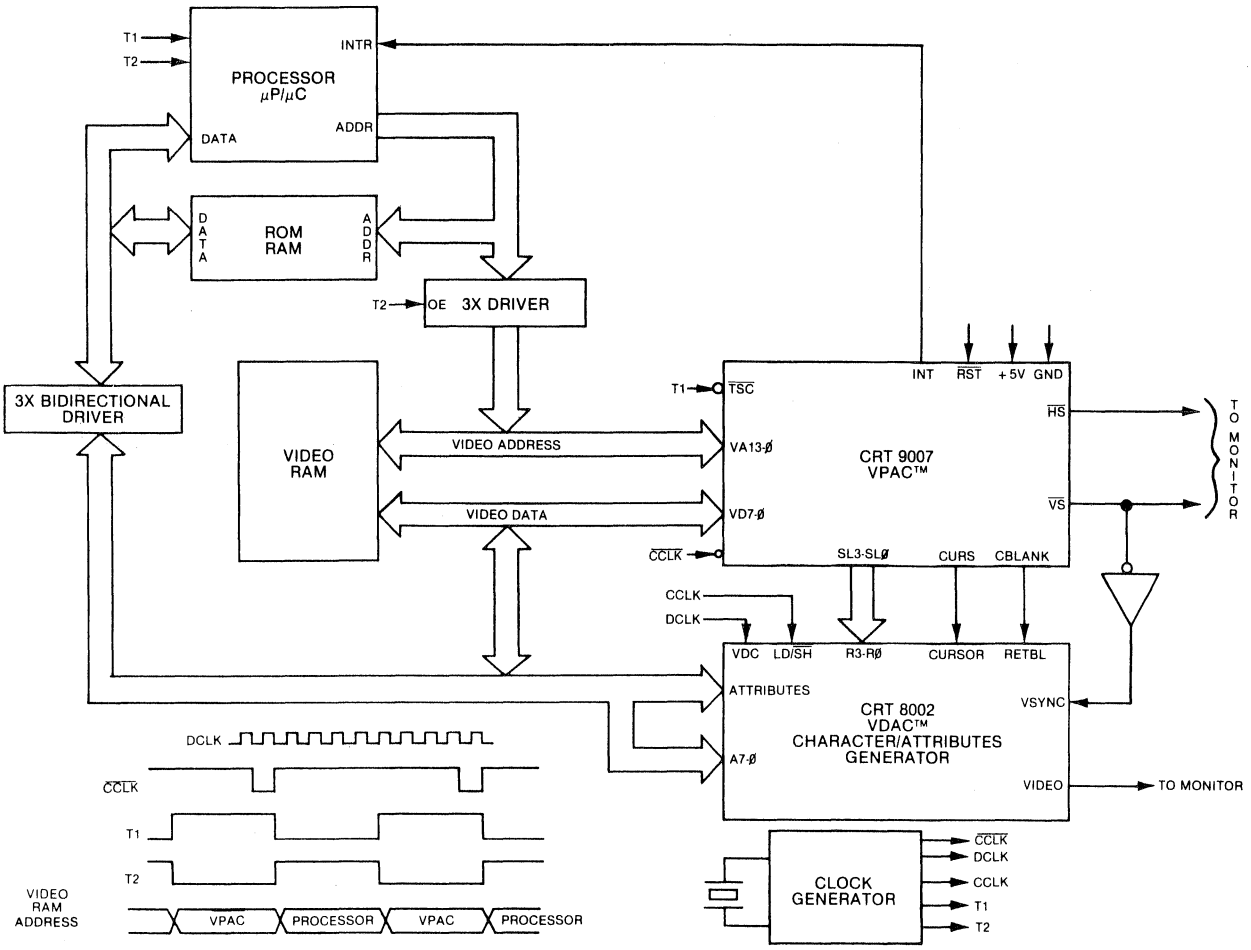


FIGURE 11: CRT 9007 CONFIGURATION WITH DOUBLE SPEED MEMORY

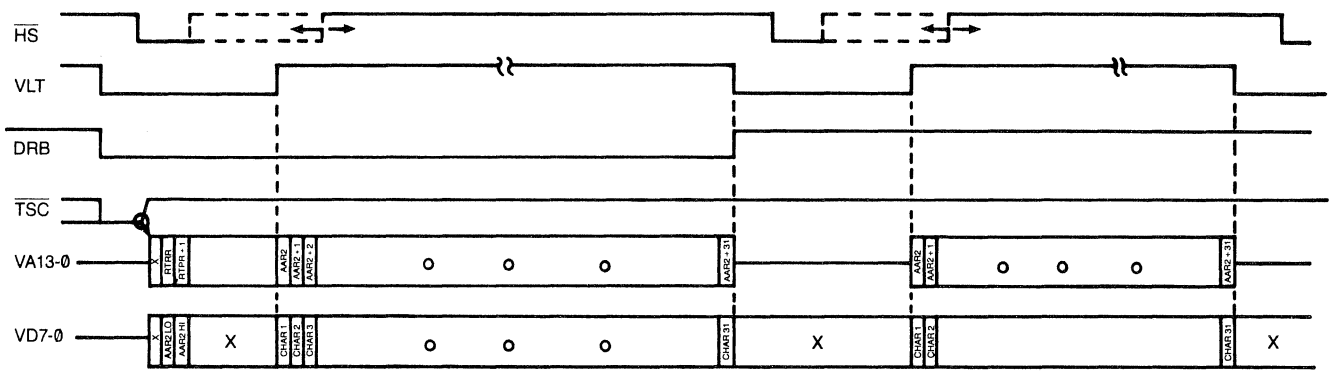


FIGURE 12: CRT 9007 REPETITIVE MEMORY ADDRESS TIMING (32 CHARACTERS PER DATA ROW)

Attribute Assemble Operation

This configuration allows the user to retain an 8 bit wide video memory in which attributes occupy memory locations but not positions on the CRT. This mode assumes that every other display position in video memory contains an attribute. During one clock cycle, attribute data is latched into the CRT 9007; during the next clock cycle a character location is addressed. The attribute data is driven out along with a WBEN signal allowing the character plus its associated attribute to be written simultaneously to two 8 bit double row buffers. Figure 13 illustrates the memory organization used for the Attribute Assemble mode. The first entry in each data row must begin with an attribute.

Figure 14 shows the CRT 9007 configured in the Attribute Assemble mode used with two CRT 9212 Double Row Buffers and 8, 16Kx1 dynamic RAMS. This mode, since it retains an 8 bit wide memory while providing all the advantages of a 16 bit wide memory, lends itself to some cost effective designs using dynamic RAMS. The CRT 9007 will refresh dynamic RAMS because twice the number of the programmed characters per data row are accessed sequentially for each data row.* Figure 15 illustrates typical timing of the CRT 9007 used in the Attribute Assemble mode.

Memory Address (typ)	Memory Data (8 bits)
0D00	Attribute 0
0D01	Character 0
0D02	Attribute 1
0D03	Character 1
0 0 0	0 0 0
2N	Attribute N
2N+1	Character N

Figure 13: Attribute Assemble Memory Organization

*Note: For 50 Hz operation there usually is about 3 milliseconds extra vertical blanking where refreshing might fail. In this situation the CRT 9007 can be programmed with about 5 more "dummy" data rows while extending the vertical blank signal. This allows the CRT 9007 to start addressing video memory much earlier within the vertical blanking interval and hence provide refresh to the dynamic RAMS. When displaying double height or double width data rows, only half as many sequential locations are accessed each data row and dynamic RAM refresh might fail.

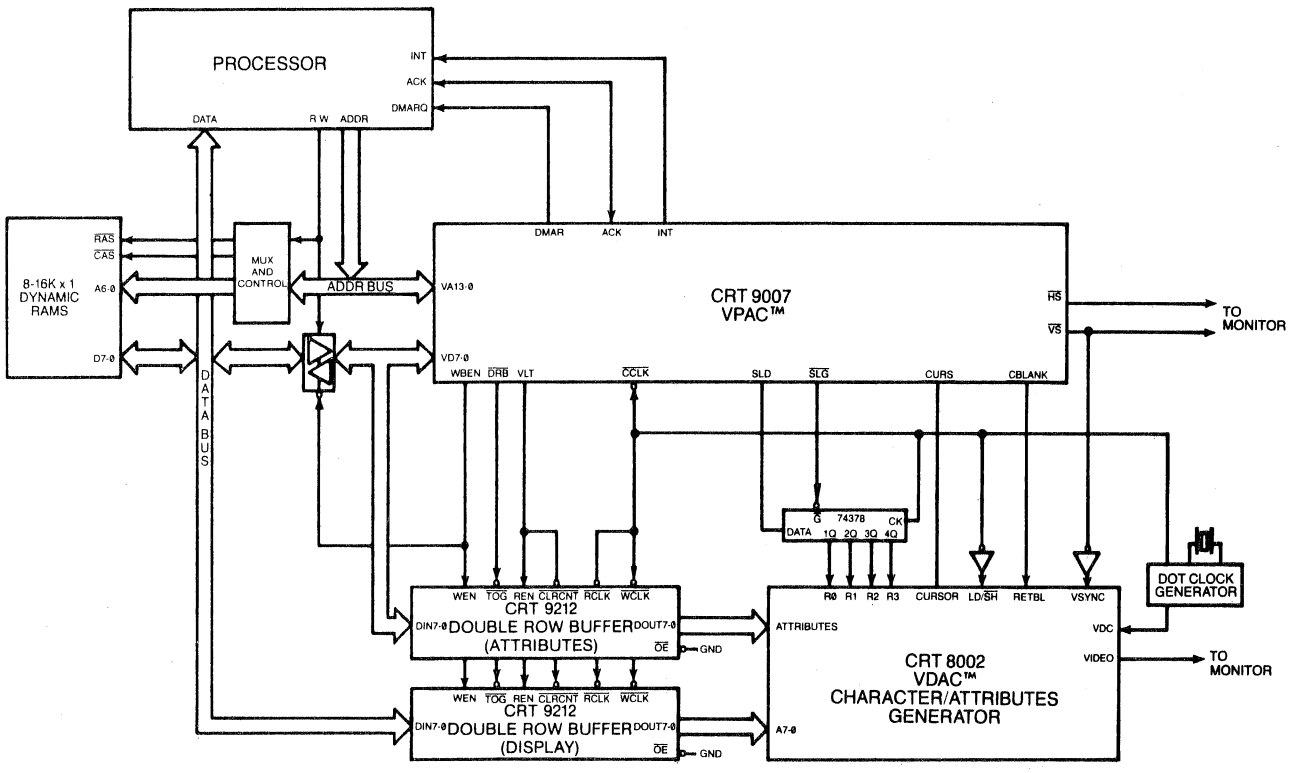
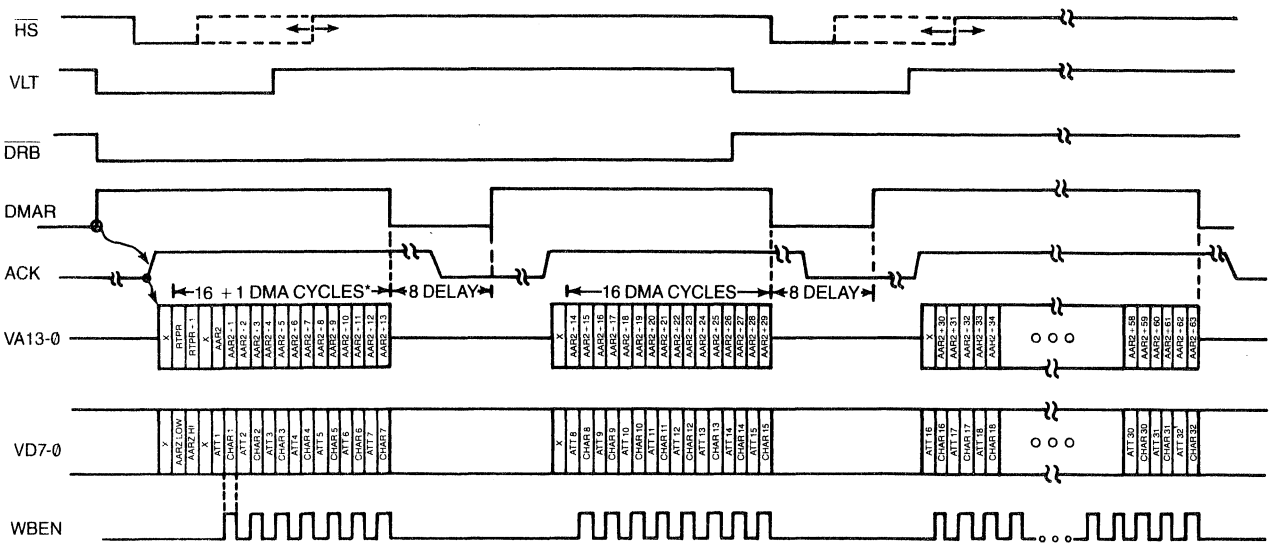


FIGURE 14: CRT 9007 CONFIGURATION FOR ATTRIBUTE ASSEMBLE MODE

Smooth Scroll Operation

Smooth scroll requires that all or a portion of the screen move up or down an integral number of scan lines at a time. 2 user programmable registers allow one to define the "start data row" and the "end data row" for the smooth scroll operation. A SMOOTH SCROLL OFFSET REGISTER (R17), when used in conjunction with a CRT 9007 vertically timed interrupt, allows the user to synchronize the update of the offset register to the vertical frame rate. The offset register causes the scan line counter outputs of the CRT 9007 to start at the programmed offset value rather than zero for the data row that starts the smooth scroll interval. To allow complete flexibility in smooth scroll direction and rate, one can update the offset register in the positive as well as negative direction and can also offset any number of scan lines each frame. Since a smooth scroll can momentarily result in a partial data row consisting of one scan line, the loading of the write buffer under DMA operations for the start and end data row of the smooth scroll operation is forced to occur in one scan line. This condition overrides the programmable DMA CONTROL REGISTER (RA).



*DMA cycles will always end at a character fetch

FIGURE 15: CRT 9007 ATTRIBUTE ASSEMBLE TIMING (32 CHARACTERS PER DATA ROW)

Row Table Addressing

In this addressing mode, each data row in video memory is designated by its own starting address. This provides greater flexibility with respect to screen operations than with other addressing schemes used by previous CRT controllers. The row table, which is a list of starting addresses for each data row, can be configured in one of 2 ways. The choice of row table format is highly dependent upon the particular application and the programmer's preference since each format allows full utilization of the CRT 9007 features.

Contiguous Row Table Format

In this format, the TABLE START REGISTER (RC and RD) points to the address where the row table begins. The contents of the first 2 locations define the starting address of the first data row. These 2 bytes define a 14 bit address where the first byte is the low order 8 bits and the second byte is the high order 6 bits. The 2 most significant bits of the second byte define double height/width characteristics to the current data row. The contents of the third and fourth locations define the address where the second data row begins. Figure 16 illustrates the contiguous row table organization in video memory.

Linked List Row Table Format

In this format the TABLE START REGISTER (RC and RD) points to the memory location which starts the entire addressing sequence into operation. The first byte read is the lower 8 bits and the second byte read is the upper 6 bits of the next data row's start address. The 2 most significant bits of the second byte define double height/width characteristics for the data row about to be read. The third, fourth, fifth, etc., bytes read are the first, second, third, etc., characters of the current data row. Figure 17 illustrates the linked list row table organization in video memory.

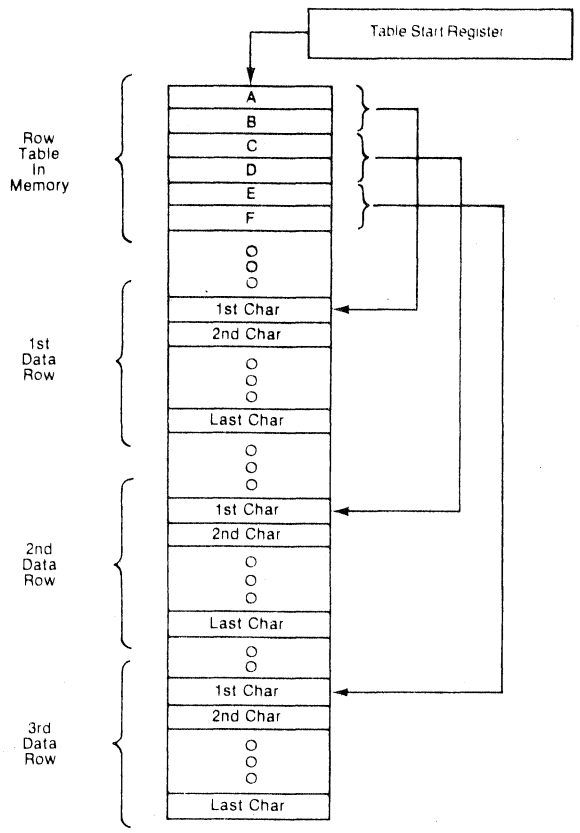


FIGURE 16: CONTIGUOUS ROW TABLE ADDRESS FORMAT

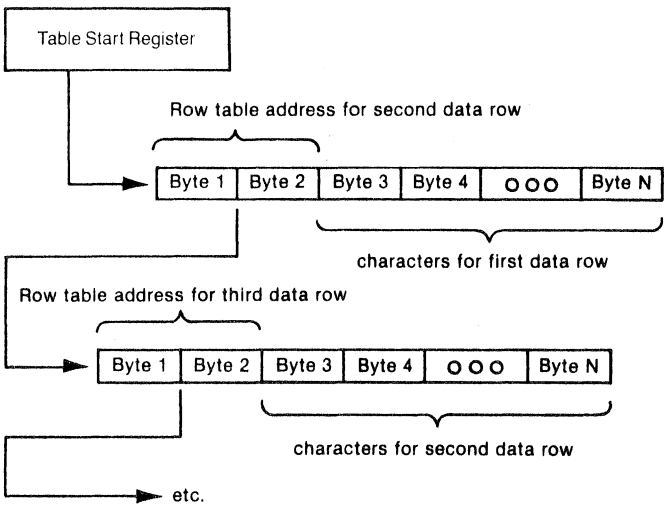


FIGURE 17: LINKED LIST ROW TABLE ADDRESS FORMAT

Sequential Addressing

In this addressing mode, characters on the display screen are located in successive memory locations. The TABLE START REGISTER (RC and RD) points to the address of the first character of the first data row on the screen. In this mode the TABLE START REGISTER does not point to the start of a table but the start of the screen. As each character is read by the CRT 9007 for display refresh, the internal video address register is incremented by one to access the next character.

For more versatile systems operation in the sequential addressing mode, SEQUENTIAL BREAK REGISTER 1 (R10) and SEQUENTIAL BREAK REGISTER 2 (R12) may be used to define the data rows at which two additional

sequential display areas begin. Note that DATA ROW END REGISTER (R12) is defined as SEQUENTIAL BREAK REGISTER 2 (R12) for the sequential addressing mode only. The starting addresses for these two additional display areas are defined by AUXILIARY ADDRESS REGISTER 1 (RE and RF) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14). When the raster begins painting a data row equal to the number programmed in one of the sequential break registers, the CRT 9007 addresses the video memory sequentially starting with the address specified by the corresponding auxiliary address register. Figure 18 illustrates a display with 80 characters per data row having sequential breaks at data rows 3 and 6.

Using the sequential addressing mode with 2 breaks, it is possible to roll a portion of the screen and keep the rest of the screen stable. Double height/width characteristics can be attached to the 2 sequentially addressed screens defined by SEQUENTIAL BREAK REGISTERS 1 and 2 by using the 2 most significant bits of AUXILIARY ADDRESS REGISTERS 1 and 2. See the description of these 2 registers for their bit definition.

TABLE START REGISTER = 1000
AUXILIARY ADDRESS REGISTER 1 = 2000
AUXILIARY ADDRESS REGISTER 2 = 0800
SEQUENTIAL BREAK REGISTER 1 = 3
SEQUENTIAL BREAK REGISTER 2 = 6

Data Row	Address range	
0	1000 to 104 F	
1	1050 to 109F	
2	10A0 to 10EF	
3	2000 to 204F	(Break 1)
4	2050 to 209F	
5	20A0 to 20EF	
6	0800 to 084F	(Break 2)
7	0850 to 089F	
8	08A0 to 08EF	
	O	
	O	
	O	

Figure 18: Sequential Addressing Example With Two Breaks

Double Height/Width Operation

When double height/width characters (2XH/2XW) are displayed, the following will occur:

1. the CRT 9007 will address half as many characters for each data row by incrementing its address every other character clock.
2. the high speed video shift register supplying serial video to the CRT must shift out dots at half frequency.
3. For double height, the scan line counter outputs (SL3-SL0 or $\overline{SLG}$, SLD) are incremented every other scan line.

The CRT 9007 is informed of the double height or double width display modes via the 2 most significant bits of the row table address or the 2 most significant bits of the AUXILIARY ADDRESS registers depending on the selected addressing mode. In any case, once the information is obtained by the CRT 9007, it must initiate the 3 tasks listed above. Tasks 1 and 3 are performed as appropriate and task 2 is performed using the CURS output of the CRT 9007 during CBLANK (horizontal retrace) to signal the external logic that a change in the dot shift frequency is required. The exact time of activation and deactivation of the CURS signal during horizontal retrace is a function of addressing mode, operation mode and actual scan line number to be painted. Tables 1 and 2 show the cursor activation and deactivation times as a function of the buffer configuration and addressing mode for the top scan line of a new data row. Tables 1 and 2 assume a cursor skew of zero. A cursor skew will effect the cursor position during trace as well as retrace time. For all subsequent scan lines, the CURS signal is activated 3 $\overline{CCLK}$'s after VLT trailing edge and stays active for exactly 1 CCLK assuming no cursor skew. When the cursor is placed on a double height or double width data row, it will become active for 2 $\overline{CCLK}$'s to allow the cursor to be displayed as double width. If the cursor position is programmed to reside in the top half of a double height data row, it may become active for all scan lines in both the current and next data row to allow the cursor to be displayed as double height.

For row driven addressing, a particular data row or pair of data rows can appear in one of the following ways as a function of the two most significant bits of the row table address (bits 15 and 14).

—Single height, single width (Row table address bits 15, 14 = 00). The CRT 9007 will display the particular data row as single height, single width.

—Single height, double width (Row table address bits 15, 14 = 01). The CRT 9007 will display the particular data row as single height double width by accessing half as many characters as appear in a single width data row. The CURS signal becomes active during horizontal retrace in the manner described previously.

—Double height, double width top half (Row table address bits 15, 14 = 10). In addition to providing the special timing associated with single height double width data rows, the scan line counter is started from zero and incremented every other scan line until N scan lines are painted (N is the number of scan lines per single height data row). In this way, new dot information appears every other scan line and the top half of the data row appears in N scan lines.

—Double Height, Double Width Bottom Half (Row table address bits 15, 14 = 11)—Same as Double Height, Double Width Top except the scan line counter is started from N/2 (or (N-1)/2 if N is odd), and incremented every other scan line until N scan lines are painted. In single row buffer operation, a double height bottom data row can never stand alone and is assumed to follow a double height top data row.

OPERATION MODE	ADDRESSING MODE	
	Row Driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Single row buffer	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Double row buffer	1 CCLK after high byte of row table read	1 CCLK after ACK leading edge

Table 1: Double Height/Width CURS activation for top scan line of new data row.

OPERATION MODE	ADDRESSING MODE	
	Row driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	at the leading edge of VLT	at the leading edge of VLT
Single row buffer	at the leading edge of VLT	at the leading edge of VLT
Double row buffer	1 CCLK after leading edge of CURS	1 CCLK after leading edge of CURS

Table 2: Double Height/Width CURS deactivation for top scan line of new data row.

PROCESSOR ADDRESSABLE REGISTERS

All CRT 9007 registers are selected by specifying the address on VA5-0 and asserting $\overline{CS}$. All 14 bit registers are written or read as two consecutive 8 bit registers addressed low byte first. Only the VERTICAL CURSOR REGISTER and the HORIZONTAL CURSOR REGISTER are read/write registers with 2 different addresses for read or write operations. The register address assigned to each register represents the actual address in hexadecimal form that must appear on VA5-0. Figure 2 illustrates all processor to CRT 9007 register timing. Tables 3a, 3b, and 3c summarize all register bits and provide register addresses.

HORIZONTAL TIMING REGISTERS

The following 4 registers define the horizontal timing parameters. Figure 19 relates the horizontal timing to these registers.

CHARACTERS PER HORIZONTAL PERIOD (R0)

This 8 bit write only register, programmed in units of character times, represents the total number of characters in the horizontal period (trace plus retrace time). This register is programmed with the binary number N where N is the total characters in the horizontal period. The horizontal period should not be programmed for less than 12 characters.

CHARACTERS PER DATA ROW (R1)

This 8 bit write only register, programmed in units of character times, represents the number of displayable characters during the horizontal trace interval. The difference R0 minus R1 represents the number of character times reserved for horizontal retrace. This register is programmed with the binary number (N-1) where N is the displayable characters per data row.

HORIZONTAL DELAY (R2)

This 8 bit write only register, programmed in units of character times, represents the time between the leading edge of horizontal sync and leading edge of VLT. This register is programmed with N where N represents the time of horizontal delay. By programming this time greater than the horizontal blank interval, one can obtain negative front porch (horizontal sync begins before the horizontal blank interval).

HORIZONTAL SYNC WIDTH (R3)

This 8 bit write only register defines the horizontal sync width in units of character times. The start of the sync pulse is defined by the HORIZONTAL DELAY REGISTER and the end is independent of the start of the active display time. This register is programmed with N where N is the horizontal sync width. However this register must be programmed less than or equal to [(A/2)-1] where A is the programmed contents of REGISTER Ø rounded to the smallest even integer.

VERTICAL TIMING REGISTERS

The following 5 registers define the vertical timing parameters. Figure 20 relates the vertical timing to these registers.

VERTICAL SYNC WIDTH (R4)

This 8 bit write only register defines the vertical sync width in units of horizontal periods. The start of this signal is defined by the delay register (R5) and the end is independent of the start of the active display time. This register is programmed with N where N is the vertical SYNC width.

VERTICAL DELAY (R5)

This 8 bit write only register, programmed in units of horizontal periods, represents the time between the leading edge of vertical sync and the leading edge of the first VLT after the vertical retrace interval. This register is programmed with (N-1) where N represents the time of the vertical delay.

VISIBLE DATA ROWS PER FRAME (R7)

This 8 bit write only register defines the number of data rows displayed on the screen. This register is programmed with (N-1) where N is the number of data rows displayed.

SCAN LINES PER DATA ROW (R8)

The 5 LSBs of this write only register define the number of scan lines per data row. These 5 bits are programmed with (N-1) where N is the number of scan lines per data row. When programming for scan lines per data row greater than 16, only the serial scan line pin option (SLD, $\overline{SLG}$) can be used.

SCAN LINES PER VERTICAL PERIOD (R8; R9)

Registers R9 and the 3 most significant bits of R8 define the number of scan lines for the entire frame. R8 contains the 3 most significant bits of the 11 bit programmed value and R9 contains the 8 least significant bits of the 11 bit programmed value. The 11 bits are programmed with N where N is the number of scan lines per frame. In the 2 interlace modes, the programmed value represents the number of scan lines per field.

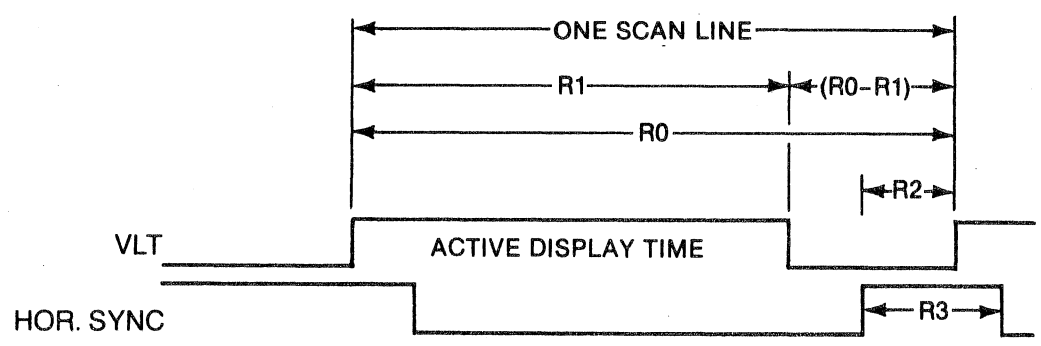


FIGURE 19: CRT 9007 HORIZONTAL TIMING

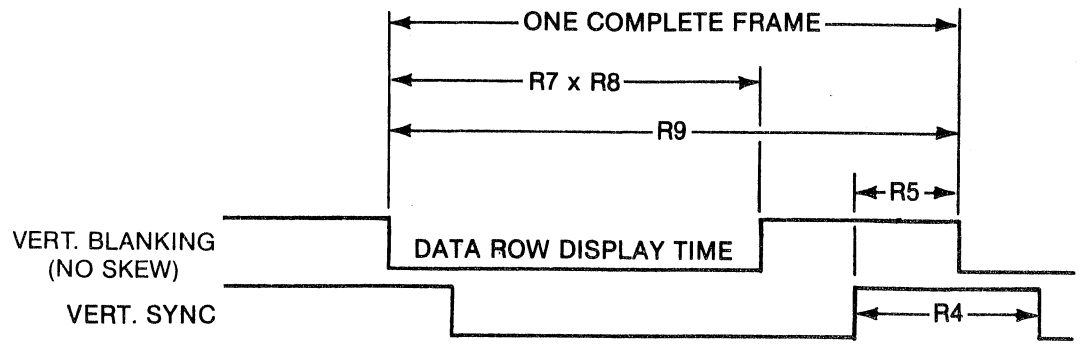


FIGURE 20: CRT 9007 VERTICAL TIMING

PIN CONFIGURATION/SKEW BITS REGISTER (R6)

This 8 bit write only register is used to select certain pin configurations and to skew (delay) the cursor and the blank signals independently with respect to the video signal sent to the monitor. The bits take on the following definition:

Bit 7, 6 (Pin Configuration)

These 2 bits, as illustrated in tables 4 and 5, define all pinout configurations as a function of double row buffer mode and non double row buffer mode. (The buffer mode is defined in the CONTROL REGISTER bits 3, 2, and 1.) The attribute assemble mode is assumed to be a double row buffer mode and obeys table 4.

Bits 5, 4, 3 (Cursor skew)

These three bits define the number of character clocks the cursor signal is skewed (delayed) from the VLT signal. The VLT signal is active for all characters within a data row and a non skewed cursor will always become active within the active VLT time at the designated position. The cursor can be skewed from 0 to 5 character clocks (Bits 5, 4 and 3 programmed from 000 to 101, bit 5 is the most significant bit; bit 3 is the least significant bit). For double height/width data rows, the cursor signal appearing during horizontal retrace is also skewed as programmed.

Bits 2, 1, 0 (Blank skew)

These three bits define the number of character clocks the horizontal blank component of the CBLANK signal is skewed (delayed) from the VLT signal. The edges of VLT will line up exactly with the edges of the horizontal component of the CBLANK signal if no skew is programmed. The CBLANK can be skewed from 0 to 5 character clocks (Bits 2, 1 and 0 programmed from 000 to 101, bit 2 is the most significant bit; bit 0 is the least significant bit).

REGISTER R6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	1	DMAR	WBEN	$\overline{SLG}$	SLD	$\overline{CSYNC}$	ACK
1	1	DMAR	WBEN	$\overline{SLG}$	SLD	LPSTB	ACK
0	0	NOT PERMITTED					
1	0	NOT PERMITTED					

Table 4: Pin configuration for double row buffer and attribute assemble modes.

REGISTER 6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	0	SL3	SL2	SL1	SL0	$\overline{CSYNC}$	TSC
1	0	SL3	$\overline{SL2}$	SL1	SL0	LPSTB	TSC
1	1	VBLANK	$\overline{CSYNC}$	$\overline{SLG}$	SLD	LPSTB	TSC
0	1	NOT PERMITTED					

Table 5: Pin configuration for Single Row Buffer and Repetitive Memory Addressing Modes.

DMA CONTROL REGISTER (RA)

This 8 bit write only register allows the user to set up a DMA burst count and delay as well as disable the DMA mechanism of the CRT 9007. The register bits have the following definition:

Bit 7 (DMA Disable)

A logic one will immediately force the CRT 9007 DMA request to the inactive level and the CRT 9007 address bus (VA13-VA0) will enter its high impedance state. After enabling the DMA mechanism by setting this bit to a logic zero, a start command must be issued (see START COMMAND, R15).

Bits 6, 5, 4 (DMA Burst Delay)

These 3 bits define the number of clock delays ($\overline{CCLK}$) between successive DMAR–ACK sequences. Bit 6 is the most and bit 4 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will delay for 4 (N + 1) clock cycles before initiating another DMA request. If 111 is programmed, however, this will result in a zero delay allowing all characters to be retrieved from video RAM in one DMA burst regardless of the value programmed for the DMA burst count.

Bits 3, 2, 1, 0 (DMA Burst Count)

These 4 bits define the number of DMA operations in one DMAR-ACK sequence. Bit 3 is the most and bit 0 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will produce 4 (N + 1) DMA cycles before relinquishing the bus. When programmed with 0000, the minimum DMA Burst will occur ($4 \times 1 = 4$) and when programmed with 1111 the maximum DMA Burst will occur ($4 \times 16 = 64$). When bits 6, 5, and 4 are programmed with 111, no DMA delay will occur and the Burst count will equal the number of programmed characters per data row as specified in R1. Refer to figures 9 and 15 which illustrate a DMA burst of 16 and a DMA delay of 8 for double row buffer and attribute assemble modes respectively. For single row buffer operation, no DMA delay is permitted and bits 6, 5, 4 must be programmed with 000.

CONTROL REGISTER (RB)

This 7 bit write only register controls certain frame operations as well as specifying the operation mode used. Internal to the CRT 9007, this register is double buffered. Changes in the register are reflected into the CRT 9007 at a particular time during vertical retrace. This allows the user to update the CONTROL REGISTER at any time without running the risk of destroying the frame or field currently being painted.

The bits take on the following definition:

Bit 6 (PB/$\overline{SS}$)

= 0; The smooth scroll mechanism is enabled permitting the SMOOTH SCROLL OFFSET REGISTER (R17) to be loaded in the scan line counter (SL3-0 or SLG, SLD signals) allowing for a scroll on the screen of a predetermined number of scan lines per frame or field. The starting and ending of the smooth scroll operation is defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

= 1; The page blank mechanism is enabled. The CBLANK signal is made active high for a continuous period of time starting and ending at the data row defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

Bits 5, 4 (Interlace)—these 2 bits define one of 3 displayed modes as illustrated in figure 21

= 00; Non interlaced display

= 10; Enhanced video interlace. This display mode will produce an interlaced frame with the same dot information painted in adjacent odd/even scan lines.

= 11; Normal video interlace. This display mode will produce an interlaced frame with odd scan lines of characters displayed in odd fields and even scan lines displayed in even fields. This mode can be used to allow the screen to show twice as many data rows at half the height since it effectively doubles the character density on the screen.

= 01; This combination is not permitted.

Bits 3, 2, 1 (Operation modes): These 3 bits define the various buffer configuration modes as follows:

= 000; (Repetitive memory addressing)—In this mode the address information (VA13-VA0) appears during every visible scan line and the address bus enters its high impedance state during all retrace intervals. When using a row driven addressing mode (linked list or contiguous), the address bus is in the high impedance state for all retrace intervals except the horizontal retrace interval prior to the top scan line of a new data row. This period can be distinguished from other retrace intervals because the $\overline{DRB}$ (data row boundary) signal is active.

= 001; (Double row buffer)—In this mode, the CRT 9007 will address a particular data row from video memory one data row prior to the time when it is displayed on the CRT. During vertical retrace, the first data row is retrieved and loaded into the double row buffer. At the next data row boundary (in this case at the end of vertical retrace), the first data row feeds the character generator while the second data row is retrieved from video memory. The address bus will enter its high impedance state in accordance with the DMA mechanism for address bus arbitration.

= 100; (Single row buffer)—In this mode, during the first scan line of each data row, the CRT 9007 will address video memory, load the buffer and feed the character generator at the painting rate of the CRT. If the CRT 9007 is used in a row driven addressing mode, it will drive the address bus during the retrace period prior to the first scan line of each data row in order to retrieve the row table address. It will automatically enter the high impedance state at the end of the first visible scan line of each data row. If the CRT 9007 is used in a sequential addressing mode, it will drive the address bus only during the visible line time of the first scan line of each data row.

= 111; (Attribute assemble)—In the attribute assemble mode, character data and attribute data are shared in consecutive alternating byte locations in memory. When the CRT 9007 reads an attribute byte, it loads it into its internal attribute latch. During the next memory access, a character byte is fetched. At this time the CRT 9007 isolates its bus from the main system bus and outputs the previously latched attribute. A WBEN signal is produced during every character byte fetch to allow the character and its associated attribute to be simultaneously latched into two double row buffers. This mode assumes that there exists twice as many byte locations as there are displayable character positions on the CRT. The first byte of every data row is assumed to be an attribute.

All other combinations of the CONTROL REGISTER bits 3, 2, 1 are not permitted.

Bit 0 ($\overline{2XC}$/1XC): This bit allows for either single or double height cursor display when the cursor is placed within a double height data row as follows:

= 1; (Single height cursor)—The CURS signal will appear during every scan line for single height data rows and will appear only during the top half or bottom half of a double height data row depending upon where the VERTICAL CURSOR REGISTER (R18, R38) defines the CURSOR data row.

= 0; (Double height cursor)—If the VERTICAL CURSOR REGISTER (R18, R38) places the cursor in the top half of a double height data row, the CURS signal will appear during every scan line of the top half (the current data row) and the bottom half (the next data row) of the double height data row. If the cursor is placed in the bottom half of a double height data row or if it is placed in a single height data row, the CURS signal will only appear during the one particular data row.

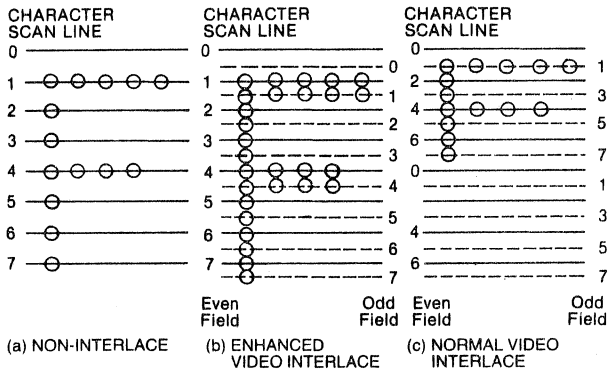


FIGURE 21: CRT 9007 INTERLACE MODES

TABLE START REGISTER (RC AND RD)

This 16 bit write only register contains a 14 bit address which is used in a variety of ways depending on the addressing mode chosen; the 2 remaining bits define the addressing mode. Register C contains the lower 8 bits of the 14 bit address. The 6 least significant bits of register D contain the upper 6 bits of the 14 bit address. The 2 most significant bits of register D define four addressing modes as follows:

Register D bits 7, 6:

= 00; (Sequential addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. One break is allowed in the sequential addressing scheme as defined by SEQUENTIAL BREAK REGISTER 1 (R10) and AUXILIARY ADDRESS REGISTER 1 (RE and RF).

= 01; (Sequential roll addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. SEQUENTIAL BREAK REGISTER 1 and AUXILIARY ADDRESS REGISTER 1 can be used to cause one sequential break as described in the sequential addressing mode. A second break in the sequential addressing can be defined by SEQUENTIAL BREAK REGISTER 2 (R12) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14) permitting up to 3 separate sequentially addressed screens to be painted.

= 10; (Contiguous row table mode)—The CRT 9007 will address video memory according to the contiguous row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define an address that points to the beginning of the contiguous row table.

= 11; (Linked list row table mode)—The CRT 9007 will address video memory according to the linked list row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define the address at which the second row table entry and the first data row reside.

AUXILIARY ADDRESS REGISTER 1 (RE and RF)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER F contain the upper order 6 bits of the 14 bit address and REGISTER E contains the 8 lower order bits of the 14 bit address. When the current data row equals the value programmed in SEQUENTIAL BREAK REGISTER 1 (R10) the remainder of the screen is addressed sequentially starting at the 14 bit address specified in this register. This sequential break overrides any row driven addressing mode used prior to the sequential break.

The 2 most significant bits of REGISTER F allow one to attach double height and/or double width characteristics to every data row in this sequentially addressed area in the following way:

For Double row buffer or attribute assemble mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; even data rows are double height double width top half odd data rows are double height double width bottom half

= 11; odd data rows are double height double width top half even data rows are double height double width bottom half

For Single row buffer or repetitive memory addressing mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; odd data rows are double height double width top half even data rows are double height double width bottom half

= 11; even data rows are double height double width top half
odd data rows are double height double width bottom half

SEQUENTIAL BREAK REGISTER 1 (R10)

This 8 bit write only register defines the data row number in which a new sequential video address begins as specified by AUXILIARY ADDRESS REGISTER 1 (RE and RF). To disable the use of this break, the register should be loaded with a data row count greater than the number of displayable data rows on the screen.

DATA ROW START REGISTER (R11)

This 8 bit write only register defines the first data row number at which a page blank or smooth scroll operation will begin. Bit 6 of the CONTROL REGISTER determines if a page blank or smooth scroll operation will occur.

DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12)

This 8 bit write only register has a dual function depending on the addressing mode used. For row driven addressing (contiguous or linked list as specified by the 2 most significant bits of the TABLE START REGISTER) this register defines the data row number which ends either a page blank or smooth scroll operation. The row numerically one less than the row defined by this register is the last data row on which the page blank or smooth scroll will occur. To use the page blank feature to blank a portion of the screen that includes the last displayed data row, this register must be programmed to zero. For sequential addressing, this register can cause a break in the sequential addressing at the data row number specified and a new sequential addressing sequence begins at the address contained in AUXILIARY ADDRESS REGISTER 2.

AUXILIARY ADDRESS REGISTER 2 (R13 and R14)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER 14 contain the upper order 6 bits of the 14 bit address and REGISTER 13 contains the 8 lower order bits of the 14 bit address. In the row driven addressing mode, this register is automatically loaded by the CRT 9007 with the current table address. The two most significant bits of REGISTER 14 specify one of four combinations of row attributes (for example double height

double width) on a row by row basis. Refer to the section entitled Double Height/Double Width operation for the meaning of these 2 bits. In the sequential addressing mode, this register can be loaded by the processor with a 14 bit address and a 2 bit row attributes field. The bit positions are identical for the row driven addressing mode. When the current data row equals the value programmed in DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12), the remainder of the screen is addressed sequentially starting at the location specified by the programmed 14 bit address. The 2 most significant bits of register 14 allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area. The bit definitions take on the same meaning as the 2 most significant bits of AUXILIARY ADDRESS REGISTER 1 and affect the display in an identical manner.

START COMMAND (R15)

After all vital screen parameters are loaded, a START command can be initiated by addressing this dummy register location within the CRT 9007. A START command must be issued after the DMA mechanism is enabled (DMA CONTROL REGISTER bit 7).

RESET COMMAND (R16)

The CRT 9007 can be reset via software by addressing this dummy location. Activation of the $\overline{RST}$ input pin or initiating this software command will effect the CRT 9007 in an identical manner. The reset state of the CRT 9007 is defined as follows:

CRT 9007 outputs	Reset state
VA13-0	High impedance
VD7-0	High impedance
$\overline{HS}$	High
VS	High
CBLANK	High
CUS	Low
$\overline{VLT}$	Low
DRB	High
INT	Low
Pin 28	Low
Pin 29	Low
Pin 30	Low
Pin 31	Low
Pin 32	Low

SMOOTH SCROLL OFFSET REGISTER (R17)

This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter output of the CRT 9007 to start at the programmed value rather than zero for the data row that starts the smooth scroll interval. The start is specified in the DATA ROW START REGISTER (R11). Typically, this register is updated every frame and it ranges from zero (no offset) to a maximum of the programmed scan lines per data row (maximum offset). For example, if 12 scan lines per data row are programmed (scan line 0 to scan line 11) an offset of zero will cause an unscrolled display. An offset of one will cause a display starting at scan line 1 and ending at scan line 11 (eleven scan lines total). An offset of eleven will cause a display starting at scan line eleven.

The next scan line will be zero, starting the subsequent data row. To allow smooth scroll of double height rows, the programmed range of the register is from zero to twice the programmed scan lines per data row. Whenever the offset register if greater than the programmed scan lines per data row, bit 7 of the register must be set to a logic 1 (offset overflow). It must be set to a logic zero at all other times. The 6 bit offset value occupies bits 6 through 1. Bit 0 must always be programmed with a logic zero. By setting the offset overflow (bit 7) to a logic 1, it is possible to have the bottom half of a double height data row stand alone in Single Row Buffer Mode by programming the scrolled data row as double height top half and loading R17 with the proper value.

VERTICAL CURSOR REGISTER (R18 or R38)

This 8 bit read/write register specifies the data row in which the cursor appears. To write into this register it is addressed as R18 and to read from this register it is addressed as R38.

HORIZONTAL CURSOR REGISTER (R19 or R39)

This 8 bit read/write register specifies the character position in which the cursor appears. To write into this register it is addressed as R19 and to read from this register it is addressed as R39.

It should be noted that the vertical and horizontal cursor is programmed in an X-Y format with respect to the screen and not dependant upon a particular location in video memory. The cursor will remain stationary during all scroll operations.

INTERRUPT ENABLE REGISTER (R1A)

This 3 bit write only register allows each of the three CRT 9007 interrupt conditions to be individually enabled or disabled according to the following definition:

Bit 6 (Vertical retrace interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when a vertical retrace (i.e., the start of the vertical blanking interval) begins.

Bit 5 (Light pen interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when the LIGHT PEN REGISTER (R3B, R3C) captures an X-Y coordinate. This interrupt, which occurs at the beginning of vertical retrace, reflects the occurrence of a LPSTB input on the frame or field just painted. This interrupt need not be enabled when other CRT 9007 interrupt conditions are enabled since the STATUS REGISTER (R3A) will flag the occurance of a light pen update and servicing can be done off of other interrupts.

Bit 0 (Frame timer)—This bit, when set to a logic one, allows the CRT 9007 to activate the INT signal once every frame or field at a time when a potential smooth scroll update may occur. In this way the user can use the frame timer interrupt as both a real time clock and can service smooth scroll updates and other frame oriented operations by using the appropriate status bits. This interrupt will occur after the last row table entry is read by the CRT 9007. In single row buffer operation, this will occur one data row before the start of vertical retrace. In double row buffer operation, this will occur two data rows before the start of vertical retrace.

STATUS REGISTER (R3A)

This 5 bit register flags the various conditions that can potentially cause an interrupt regardless of whether the corresponding condition is enabled for interrupt. In this way some or all of the conditions can be reported to the processor via the STATUS REGISTER. If some of the conditions are enabled for interrupt, the processor, in response to an interrupt, simply has to read the STATUS REGISTER to determine the cause of the interrupt. The bit definition of the STATUS REGISTER is as follows:

Bit 7 (Interrupt Pending)—This bit will set when any other status bit, having its corresponding interrupt enabled, experiences a 0 to 1 transition. In this manner, when the processor services a potential CRT 9007 interrupt, it only has to test the interrupt pending bit to determine if the CRT 9007 caused the interrupt. If it did, the individual bits can then be tested to determine the details of the CRT 9007 interrupt. Any noninterruptable status change (corresponding interrupt enable bit reset to a logic 0) will not be reflected in the interrupt pending bit and must be polled by

the processor in order to provide service. The interrupt pending bit is reset when the status register is read. All other bits except Light Pen Update are reset to a logic 0 at the end of the vertical retrace interval. The light pen update bit is reset to a logic 0 when the HORIZONTAL LIGHT PEN REGISTER is read.

Bit 6 (Vertical Retrace)—A logic 1 indicates that a vertical retrace interval has begun.

Bit 5 (Light Pen Update)—A logic 1 indicates that a new coordinate has been strobed into the LIGHT PEN REGISTER. It is reset to a logic zero when the HORIZONTAL LIGHT PEN REGISTER is read. The light pen coordinates may have to be modified via software depending on light pen characteristics.

Bit 2 (odd/even)—For a normal video interlaced display, this bit is a logic 1 when the field about be painted is an odd field and is a logic zero when the field about be painted is an even field.

Bit 0 (Frame timer occurred)—This bit becomes a logic 1 either one or two data rows before the start of vertical retrace. Since this bit is set when the CRT has finished reading the row table for the frame or field just painted, it permits row table manipulation to start at the earliest possible time.

VERTICAL LIGHT PEN REGISTER (R3B)

This 8 bit read only register contains the vertical coordinate captured at the time the CRT 9007 received a light pen strobe signal (LPSTB).

HORIZONTAL LIGHT PEN REGISTER (R3C)

This 8 bit read only register contains the horizontal coordinate captured at the time the CRT 9007 received a light pen strobe signal. When a coordinate is captured, the appropriate status bit is set and further transitions on LPSTB are ignored until this register is read. The reading of this register will reset the light pen status bit in the STATUS REGISTER. The captured coordinate may have to be modified in software to allow for light pen response.

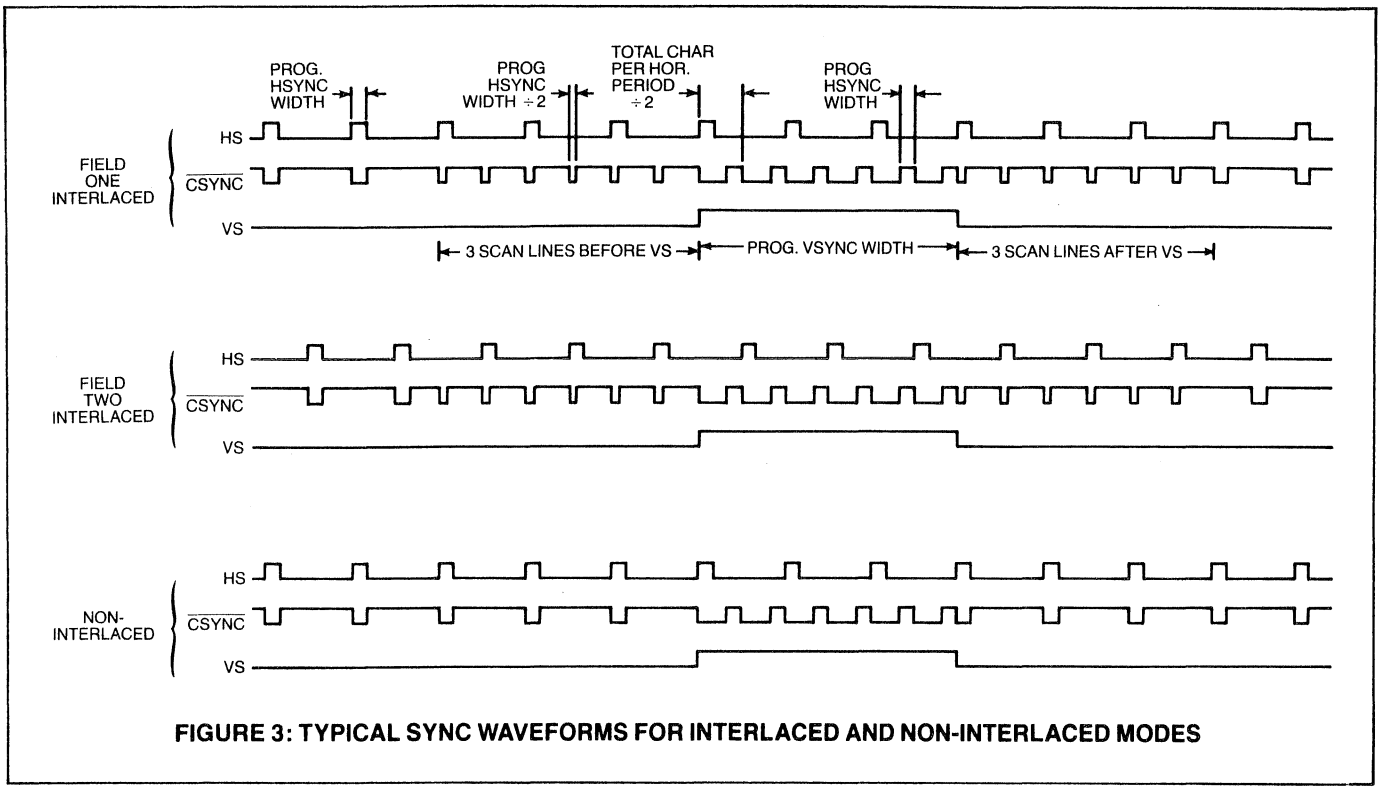


FIGURE 3: TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES

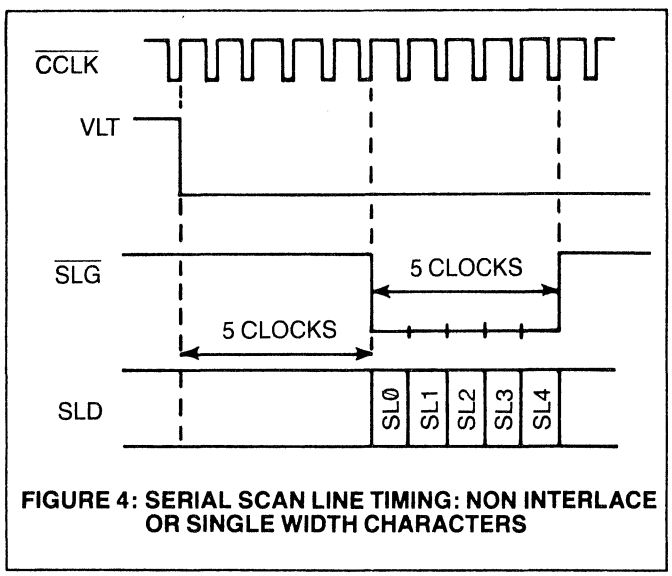


FIGURE 4: SERIAL SCAN LINE TIMING: NON INTERLACE OR SINGLE WIDTH CHARACTERS

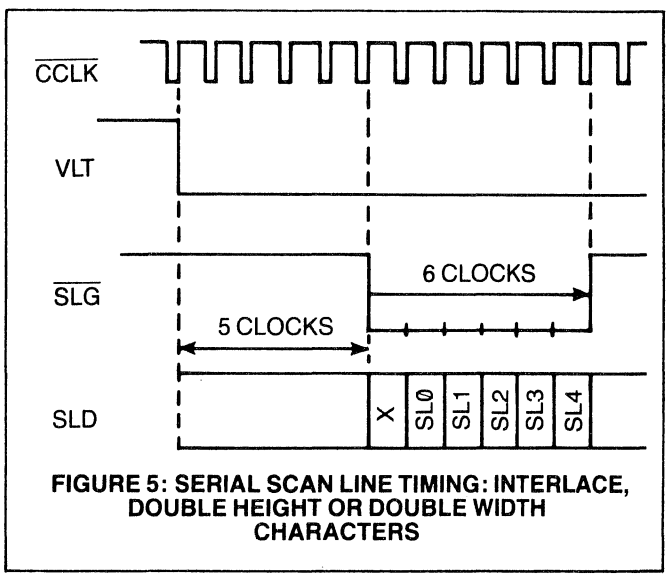


FIGURE 5: SERIAL SCAN LINE TIMING: INTERLACE, DOUBLE HEIGHT OR DOUBLE WIDTH CHARACTERS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0° to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+15V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH1}	High	2.0			V	all inputs except $\overline{CCLK}$
V_{IH2}	High	4.3			V	$\overline{CCLK}$ input
	Output voltage					
V_{OL}	Low			0.4	V	$I_{OL} = 1.6$ mA
V_{OH}	High	2.4			V	$I_{OH} = 40\mu A$
	Input leakage current					
I_{L1}				10	μA	$0 \leq V_{IN} \leq V_{CC}$; excluding $\overline{CCLK}$
I_{L2}				50	μA	$0 \leq V_{IN} \leq V_{CC}$; for $\overline{CCLK}$
	Input capacitance					
C_{IN1}			10		pF	all inputs except $\overline{CCLK}$
C_{IN2}			25		pF	$\overline{CCLK}$ input
	Power supply current					
I_{CC}			100		mA	

AC ELECTRICAL CHARACTERISTICS[3] $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Clock					
t_{CY}	clock period	250			ns	
t_{CKL}	clock low	23			ns	
t_{CKH}	clock high	203			ns	
t_{CKR}	clock rise time			10	ns	measured from 10% to 90% points
t_{CKF}	clock fall time			10	ns	measured from 90% to 10% points
	Output delay[1]					
t_{D1}				125	ns	
t_{D2}				125	ns	
t_{D3}				150	ns	
t_{D4}				150	ns	
t_{VA}				100	ns	measured to the 2.3V or 0.5V level on VA13-VA0
t_{DSL}				500	ns	
t_{D5}				185	ns	
t_{D6}				185	ns	
t_{DSY}				185	ns	
t_{VDS}		50			ns	valid for loading auxiliary address register 2 or the attribute latch
t_{VDH}		0			ns	
t_{VD0}				185	ns	$c_L = 50$pF
t_{SLG}				185	ns	
t_{SLD}				185	ns	
	Processor Read/write[2]					
t_{AS}		100			ns	
t_{AH}		0			ns	
t_{PW}		155			ns	
t_{PDS}		100			ns	
t_{PDH}		0			ns	
t_{PDA}				140	ns	
t_{PDH}		10		50	ns	
t_{IRR}				400	ns	
	Miscellaneous timing					
t_{ATS}				125	ns	measured from the 0.4V level of ACK or $\overline{TSC}$ falling edge
t_{RW}				$4t_{CY}$	ns	measured from the 0.4V level falling edge to 0.4V level rising edge

NOTE:
1. Timing measured from the 1.5V level of the rising edge of $\overline{CCLK}$ to the 2.4V (high) or 0.4V (low) voltage level of the output unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.

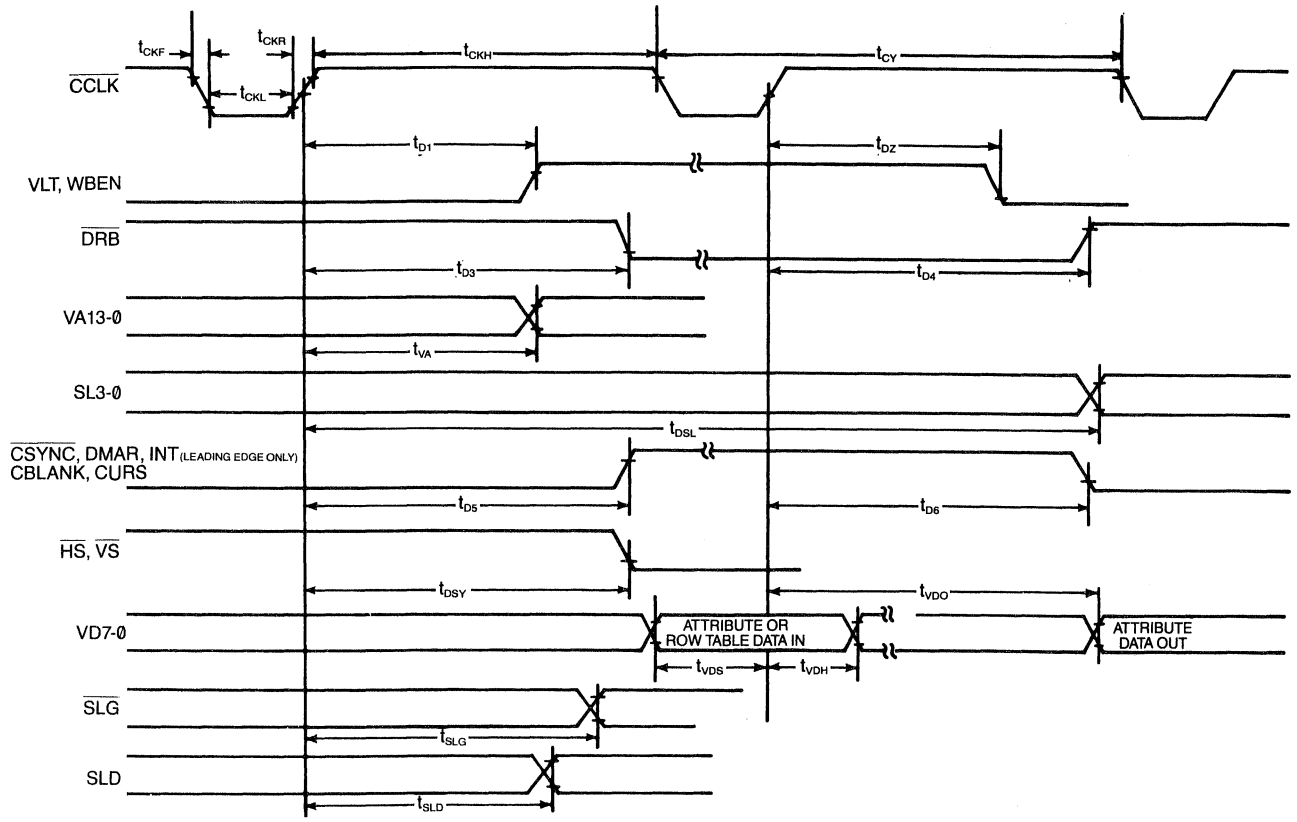


FIGURE 22: CRT 9007 TIMING PARAMETERS: OUTPUT SIGNALS

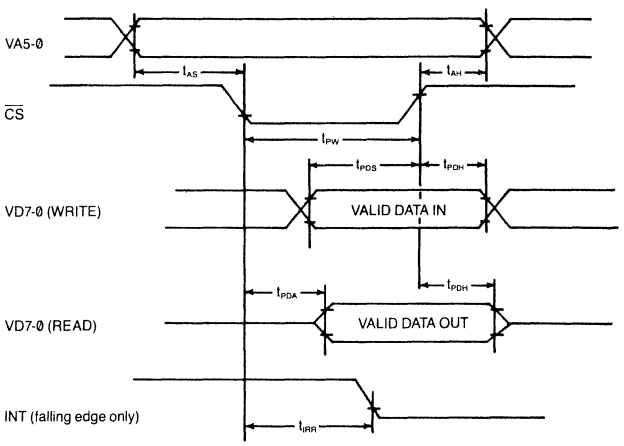
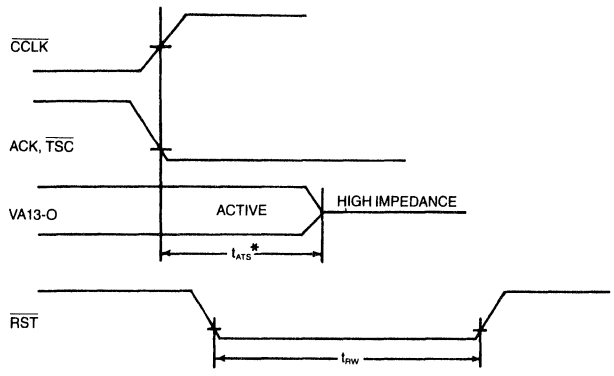


FIGURE 2: CRT 9007 PROCESSOR READ AND WRITE TIMING PARAMETERS



* t_{ATS} is controlled directly from ACK or $\overline{TSC}$ or from the particular $\overline{CCLK}$ that ends a DMA burst cycle.

FIGURE 23: CRT 9007 MISCELLANEOUS TIMING PARAMETERS

Register Type	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	0	0	0	0	MSB	CHARACTERS PER HORIZONTAL PERIOD						LSB	R0
WRITE	0	0	0	0	0	1	MSB	CHARACTERS PER DATA ROW						LSB	R1
WRITE	0	0	0	0	1	0	MSB	HORIZONTAL DELAY						LSB	R2
WRITE	0	0	0	0	1	1	MSB	HORIZONTAL SYNC WIDTH						LSB	R3
WRITE	0	0	0	1	0	0	MSB	VERTICAL SYNC WIDTH						LSB	R4
WRITE	0	0	0	1	0	1	MSB	VERTICAL DELAY						LSB	R5
WRITE	0	0	0	1	1	0	PIN CONFIG-URATION	CURSOR SKEW MSB			LSB	BLANK SKEW MSB		LSB	R6
WRITE	0	0	0	1	1	1	MSB	VISIBLE DATA ROWS PER FRAME						LSB	R7
WRITE	0	0	1	0	0	0	SCAN LINES/FRAME (B10))	(B8)	MSB	SCAN LINES PER DATA ROW				LSB	R8
WRITE	0	0	1	0	0	1	(B7)	SCAN LINES PER FRAME						LSB (B0)	R9

Table 3a: CRT 9007 Screen Format Registers

Register Type	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	1	0	1	0	DMA DIS-ABLE	DMA BURST DELAY MSBA		LSB	DMA BURST COUNT MSB			LSB	RA
WRITE	0	0	1	0	1	1	X	PB/$\overline{SS}$	INTERLACE MODES		OPERATION MODES			$\overline{2XC}$/1XC	RB
WRITE	0	0	1	1	0	0	MSB	TABLE START REGISTER (LS BYTE)						LSB	RC
WRITE	0	0	1	1	0	1	ADDRESS MODE	TABLE STRT REGISTER (MS BYTE) MSB						LSB	RD
WRITE	0	0	1	1	1	0	MSB	AUXILIARY ADDRESS REGISTER 1 (LS BYTE)						LSB	RE
WRITE	0	0	1	1	1	1	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 1 (MS BYTE) MSB						LSB	RF
WRITE	0	1	0	0	0	0	MSB	SEQUENTIAL BREAK REGISTER 1						LSB	R10
WRITE	0	1	0	0	0	1	MSB	DATA ROW START REGISTER						LSB	R11
WRITE	0	1	0	0	1	0	MSB	DATA ROW END/SEQUENTIAL BREAK REGISTER 2						LSB	R12
WRITE	0	1	0	0	1	1	MSB	AUXILIARY ADDRESS REGISTER 2 (LS BYTE)						LSB	R13
WRITE	0	1	0	1	0	0	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 2 (MS BYTE) MSB						LSB	R14

Table 3b: Control and Memory Address Registers

Register Type	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
READ OR WRITE	0	1	0	1	0	1	START COMMAND								R15
READ OR WRITE	0	1	0	1	1	0	RESET COMMAND								R16
WRITE	0	1	0	1	1	1	OFFSET OVER-FLOW	OFFSET VALUE MSB					LSB	0	R17
WRITE	0	1	1	0	0	0	MSB	VERTICAL CURSOR REGISTER (ROW COORD.)						LSB	R18 or R19
READ	1	1	1	0	0	0									
WRITE	0	1	1	0	0	1	MSB	HORIZONTAL CURSOR REGISTER (COL. COORD.)						LSB	R19 or R39
READ	1	1	1	0	0	1									
WRITE	0	1	1	0	1	0	X	VER-TICAL RE-TRACE	INTERRUPT ENABLE REGISTER LIGHT PEN	X	X	X	X	FRAME TIMER	R1A
READ	1	1	1	0	1	0	INT PEND-ING	VER-TICAL RE-TRACE	LIGHT PEN	STATUS REGISTER		ODD/ EVEN	X	FRAME TIMER	R3A
READ	1	1	1	0	1	1	MSB	VERTICAL LIGHT PEN REGISTER (ROW COORD.)						LSB	R3B
READ	1	1	1	1	0	0	MSB	HORIZONTAL LIGHT PEN REGISTER (COL. COORD.)						LSB	R3C

Table 3c: Cursor, Light Pen, Offset, and Status Registers

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STANDARD MICROSYSTEMS CORPORATION

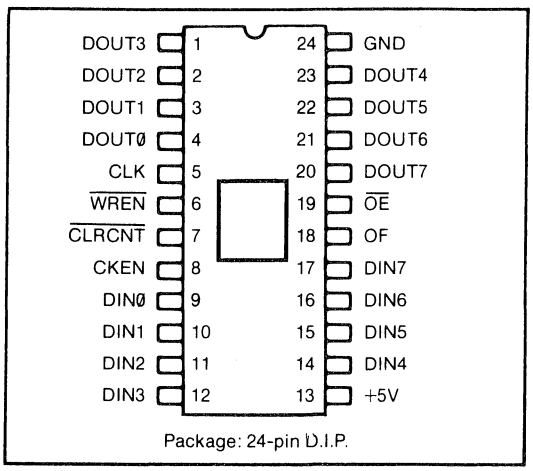
CRT 9006-135
CRT 9006-83
μPC FAMILY

Single Row Buffer
SRB

FEATURES:

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Provides 8 Bit Wide Variable Length Serial Memory
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row — ...64, 80, 132,... up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for Invisible Attributes or Character Widths of Greater than 8 Bits
- ☐ Three-State Outputs
- ☐ 4MHz Typical Read/Write Data Rate
- ☐ Static Operation
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 24 Pin Dual In Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible Inputs and Outputs
- ☐ Available in 135 Byte Maximum Length (CRT 9006-135) or 83 Byte Maximum Length (CRT 9006-83)

PIN CONFIGURATION



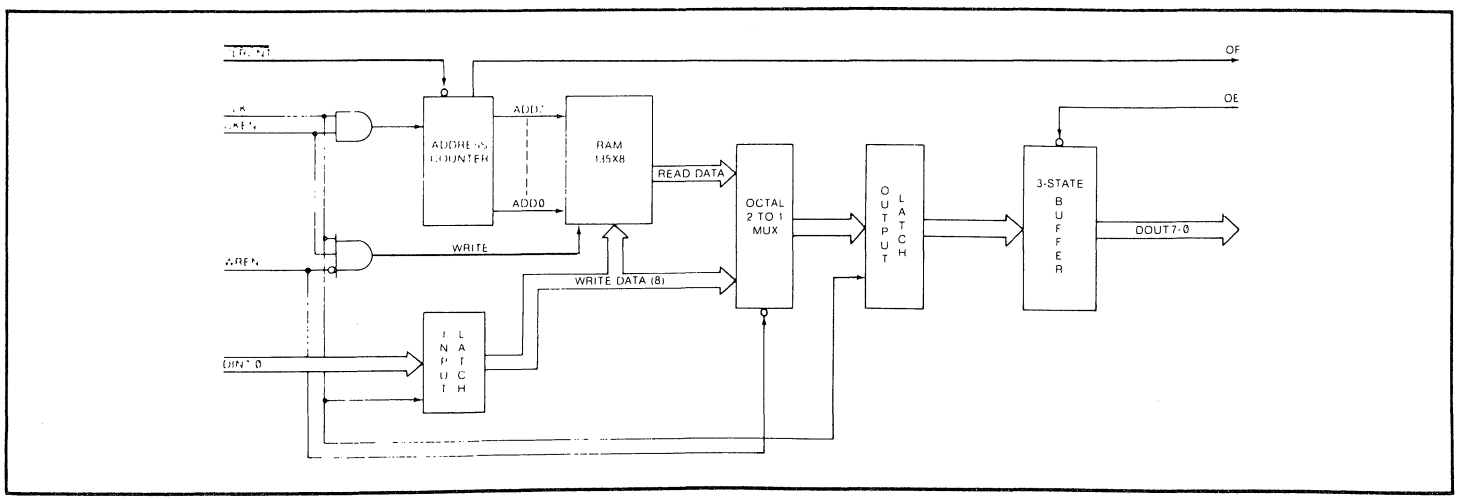
Package: 24-pin D.I.P.

APPLICATIONS:

- ☐ CRT Data Row Buffer
- ☐ Block-Oriented Buffer
- ☐ Printer Buffer
- ☐ Synchronous Communications Buffer
- ☐ Floppy Disk Sector Buffer

GENERAL DESCRIPTION

The SMC Single Row Buffer (SRB) provides a low cost solution to memory contention between the system processor and CRT controller in video display systems.
The SRB is a RAM-based buffer which is loaded with character data from system memory during the first scan line of each data row. While data is being written into the RAM it is also being output through the multiplexer onto the Data Ouput (DOUT) Lines. During subsequent scan lines in the data row, the system will disable Write Enable (WREN) and cause data to be read out from the internal RAM for CRT screen refresh, thereby releasing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row. The SRB enhances processor throughput and permits a flicker-free display of data.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-4	DATA OUTPUTS	DOUT3-DOUTØ	Data Outputs from the internal output latch.
5	CLOCK	CLK	Character clock. The negative-going edge of CLK clocks the latches. When CKEN (pin 8) is high, CLK will increment the address counter.
6	WRITE ENABLE	$\overline{\text{WREN}}$	When $\overline{\text{WREN}}$ is low, data from the input latch is transferred directly to the output latch and simultaneously written into sequential locations in the RAM.
7	CLEAR COUNTER	$\overline{\text{CLRCNT}}$	A negative transition on $\overline{\text{CLRCNT}}$ clears the RAM address counter. $\overline{\text{CLRCNT}}$ is normally asserted low near the beginning of each scan line.
8	CLOCK ENABLE	CKEN	When CKEN is high, CLK will clock the address counter. The combination of CKEN high and WREN low will allow the writing of data into the RAM.
9-12	DATA INPUTS	DINØ-DIN3	Data Inputs from system memory.
13	POWER SUPPLY	V_{CC}	+5 Volt supply.
14-17	DATA INPUTS	DIN4-DIN7	Data Inputs from system memory.
18	OVERFLOW FLAG	OF	This output goes high when the RAM address counter reaches its maximum count. If cascaded operation of multiple CRT 9006's is desired for more than 135 bytes, OF may be used to drive the CKEN input of the second row buffer chip.
19	OUTPUT ENABLE	$\overline{\text{OE}}$	When $\overline{\text{OE}}$ is low, the data outputs DOUTØ-DOUT7 are enabled. When $\overline{\text{OE}}$ is high, DOUTØ-DOUT7 present a high impedance state.
20-23	DATA OUTPUTS	DOUT7-DOUT4	Data Outputs from the internal output latch.
24	GROUND	GND	Ground.

OPERATION

For CRT operation, the Write Enable ($\overline{\text{WREN}}$) signal is made active for the duration of the top scan line of each data row. Clear Counter ($\overline{\text{CLRCNT}}$) typically occurs at the beginning of each scan line (HSYNC may be used as input to $\overline{\text{CLRCNT}}$). Data is continually clocked into the input latch by CLK. When Clock Enable (CKEN) occurs, the data in the input latch (Write Data) is written into the first location of RAM. At the negative-going edge of the next clock, the address counter is incremented, the next input data is latched into the input latch, and the new data is then written into the RAM. Loading the RAM continues until one clock after CKEN goes inactive or until the RAM has been fully loaded (135 bytes). While data is being written into the RAM, it is also being output through the multiplexer onto the Data Output (DOUT) lines. Each byte is loaded into the output latch one clock time later than it is written into the RAM. Output of the data during the first scan line permits the Video Display Controller (such as the CRT 8002) to display video on the first scan line. During subsequent scan lines in the data row, the system will disable Write Enable ($\overline{\text{WREN}}$) and cause data to be read out from the internal RAM, thereby freeing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row.

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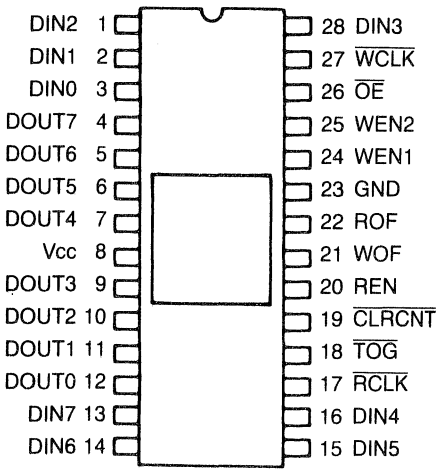
CRT 9212
μPC FAMILY

Double Row Buffer
DRB

FEATURES

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- ☐ Permits Display of One Data Row While Next Data Row is Being Loaded
- ☐ Data May be Written into Buffer at Less Than the Video Painting Rate
- ☐ Double Data Row Buffer Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

- ☐ Three-State Outputs
- ☐ Up to 4 MHz Read/Write Data Rate
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 28 Pin Dual-In-Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible

GENERAL DESCRIPTION

The CRT 9212 Double Row Buffer (DRB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The CRT 9212 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 9212 permits the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floppy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
3-0, 28, 16-13	Data inputs	DIN0-DIN7	DIN0-DIN7 are the data inputs from the system memory.
12-9, 7-4	Data outputs	DOUT0-DOUT7	DOUT0-DOUT7 are the data outputs from the CRT 9212 internal data output latch. Valid information will appear on DOUT0-DOUT7 two $\overline{RCLK}$ periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
17	Read Clock	$\overline{RCLK}$	$\overline{RCLK}$ increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge.
18	Toggle Signal	$\overline{TOG}$	$\overline{TOG}$ alternates the function of each buffer between read and write. $\overline{TOG}$ normally occurs at every data row boundary. Switching of the buffers occurs when both $\overline{TOG}$ and CLRCNT are low.
19	Clear Counter	$\overline{CLRCNT}$	Clear Counter clears the current "read" address counter at the next $\overline{RCLK}$ positive edge. $\overline{CLRCNT}$ is normally asserted low at the beginning of each horizontal retrace interval. $\overline{CLRCNT}$ clears the current "write" address counter when the $\overline{TOG}$ is active.
20	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when Read Clock is active.
21	Write Overflow	WOF	WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. See figure 4.
22	Read Overflow	ROF	The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of $\overline{RCLK}$ after ROF goes high. See figure 4.
24, 25	Write Enable	WEN1, WEN 2	WEN allows input data to be written into the selected "write" buffer during $\overline{WCLK}$ active. Both WEN1 and WEN 2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open.
26	Output Enable	$\overline{OE}$	When the $\overline{OE}$ input is low, the data outputs DOUT0-DOUT7 are enabled. When $\overline{OE}$ is high, DOUT0-DOUT7 present a high impedance state. $\overline{OE}$ has an internal pulldown resistor allowing it to assume a low if pin 26 is left open.
27	Write Clock	$\overline{WCLK}$	$\overline{WCLK}$ clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high.
8	Power Supply	V_{CC}	+5 Volt supply
23	Ground	GND	Ground

OPERATION

Figure 1 illustrates the internal architecture of the CRT 9212. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When both Write Enable (WEN1, WEN 2) signals go high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal ($\overline{TOG}$) will go low. When Clear Counter ($\overline{CLRCNT}$) goes low, the next Read Clock ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock ($\overline{RCLK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the CRT 9212 and the internal "read" address counter is cleared independent of the $\overline{CLRCNT}$ pulse width. The $\overline{CLRCNT}$ input may be tied to the REN input for proper operation.

Figures 2 and 3 illustrate the functional timing for reading and writing the CRT 9212. It is possible to cascade two or more CRT 9212's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 4 illustrates two CRT 9212's cascaded together.

The CRT 9212 is compatible with the CRT 9007 video processor and controller (VPAC™) and the CRT 8002 video display attributes controller (VDAC™). A typical video configuration employing the three parts is illustrated in figure 5.

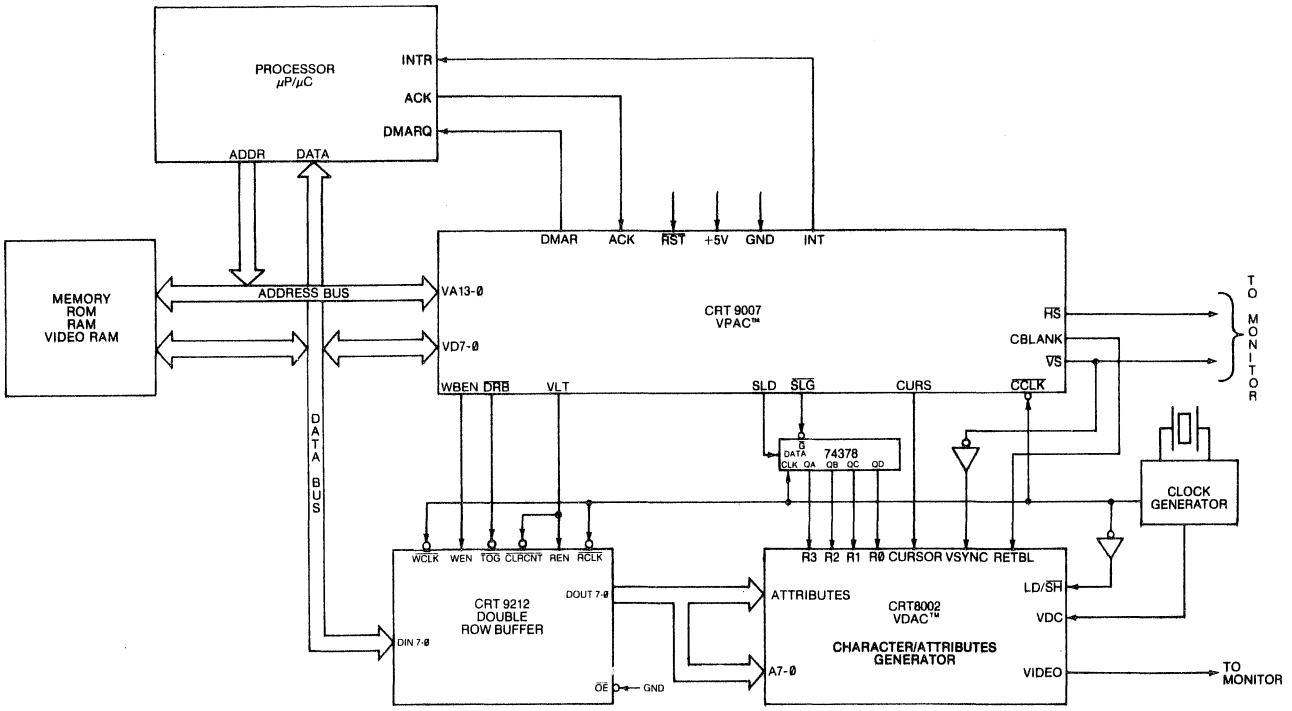


FIGURE 5: CRT 9212 CONFIGURED WITH THE CRT 9007 VPAC AND THE CRT 8002 VDAC™

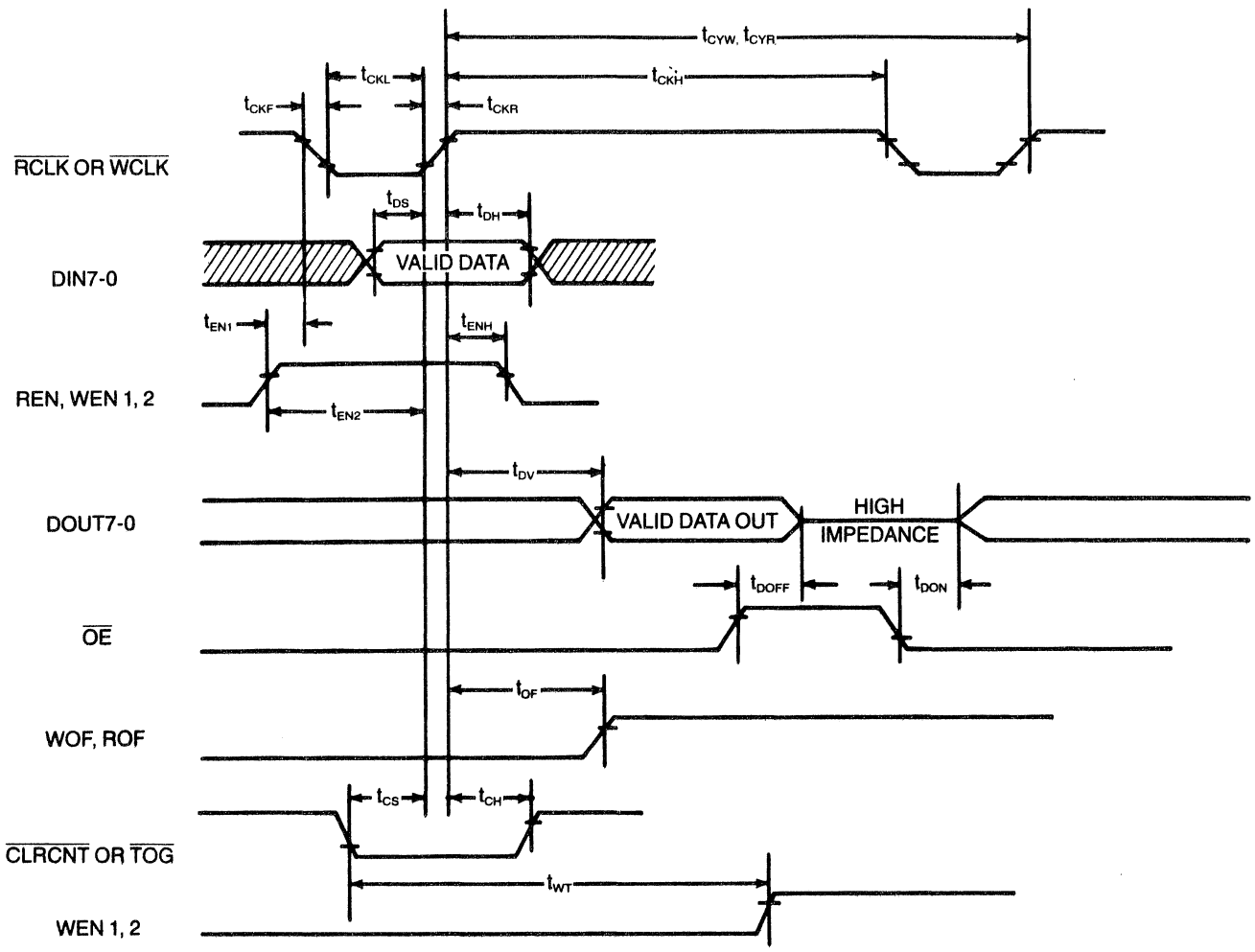


FIGURE 6: CRT 9212 I/O TIMING

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	PROTO REL		
	2	" "		
	3	" "		
	A	PROD REL PER ECO 0414		
	A1	PROD REL PER ECO 0443	9/1/82	
	B	PROD REL PER ECO 0459		
	C	" " ECO 0500	9/29/82	
	D	" " " 0548	11/12/82	

A1 DS8867 (OPTION)

A2 (OPTION)

A3 7414

A4 74LS145

A5 74LS145

A6 8049 8749

VR1 REGULATOR 78 M 05

RESET CLK A7 MC14040 QB GND

NOTES UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT.
2. ALL CAPACITOR ARE VALUED IN uF 50 VDC AND ARE 10%.

= KEY SWITCH

= NOT USED

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN			DWN HHUA 3-3-82	TeleVideo, Inc.
NEXT ASSY	USED ON				CHK	
2020900	—	ANG	2 PLC	3 PLC	ENGR	TITLE PCB SCHEMATIC 970 KYBD
					APPD	
		SCALE			APPD	
		MATERIAL			FINISH	SIZE D SHT 1 OF — DRAWING NO 2020800 REV D

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	PROTO REL		
	2	PROTO REL		
	3	"		
	A	PROD REL PER ECO 0584	11/16/82	Eric Chen
	A1	INCORP PER ECO 0640	12/27/82	Eric Chen
	A2	" " " 2011	1-7-83	Eric Chen
	B	" " " 2015	1-17-83	Eric Chen
	C	" " " 2041	3-3-83	Eric Chen
	D	CHANGE PER ECO 2121	3-8-83	Eric Chen

NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4W WATT. ± 5%.
2. ALL CAPACTORS ARE VALUED IN uF AND ARE 50 VDC ±20%.

PARTS LIST				
APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DRAWN	JOA 4-6-82
NEXT ASSY	USED ON	ANG ± PLCS ± PLC	CHK	
202100-2			ENGR	
			APPD	
			APPD	
			APPD	
		SCALE	FINISH	
		MATERIAL		

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 970 CONT BD

SIZE D | SHT 1 OF 10 | DRAWING NO. 202100 | REV T-2

202100

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		

REC 3
REC 2
SH 9 — REC Ø, REC 1
74LS08 A9
E37 27128
E35 E36 2764
+5V
R48 10K
SH 1 — AD 14, AD 13
E10 E11 E14 E15
+5V
E17 E16
E18 E19
CR7 IN756
+12V
Q9 2N2219A
R74
R73 220
R70 1K
+5V
CR4 IN914
CR5 IN914
B1 BATTERY
AD11 E21
E22
GND

A82 2764 27128
A87 2764, 27128
A99 2764, 27128
A105 MSM 5128 200

SH 1 — AD11, AD10, AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, ADØ, AD12
SH 1 — +5V MEMA
SH 1 — WR, DB 7, DB6, DB5, DB4, DB3, DB2, DB1, DBØ

SH 9 — OEØØ
SH 9 — OEØ1, OEØ2
SH 1 — BUSACK

A15 74LS374
A23 74LS374
A31 74LS 174
R29 4.7K 5V

A36 74LS02
A14 7406

SBØ4, SBØ3, SBØ2, SBØ1, SBIØ, NMDSFT, BLOCK/LINE CUR, TIME OUT BLANK
SH 9
SH 5
SH 6
SH 6

AD14, FNCTL, BOW/WOB, 80/132 CHAR, BI-DIR ENA, LRAM
SH 3,9
SH 10
SH 6
SH 4
SH 7
SH 4

CURSOR BLINK, BLINK CLK
SH 6

CONTROL REG A
CONTROL REG B
CONTROL REG C

P7-1 (OPT)
P7-8
SIG GND → P3-7
SIG GND → P4-7
P6-7
P6-8 (OPT)
P10-2 (OPT)
P10-12
PROT GND → P3-1
PROT GND → P4-1

B0000 C 001

PARTS LIST

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	OWN	HUTCHINSON
NEXT ASSY	USED ON	ANG ± PLC ± PLC ±	CHK	
		SCALE	ENGR	
		MATERIAL	APPD	
		FINISH	APPD	
			APPD	

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TITLE: PCB SCHEMATIC 970 CONT BD

SIZE D | DWG NO 20-1300 | REV J

SHEET NO 2021300 | SH 2 | REV 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		

WR
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
SH1

SH1,2
AD14
AD7
AD13
AD6
AD12
AD5
AD11
AD4
SH1
A90 74LS241

AD10
AD3
AD9
AD2
AD8
AD1
AD15
AD0
SH1
A97 74LS241

E7 64K
E5 16K
E6

+5V
RP64.7K
RP5 33Ω
RP6 4.7K
R69 33
R71 33
E25 64K
E30 16K
E27
E26 NC
E28 16K
E29 16K
E31
E32 64K
-5V
+12V

A94 4116
A101 4116
A106 4116
A111 4116
A95 4116
A102 4116
A107 4116
A112 4116
DI DO R/W A7/VCC A6 A5 A4 A3 A2 A1 A0 CAS RAS VDD VSS

A103 74LS244
1A3 2A3 1A1 2A2 1A4 2A4 2A1 1A2
1Y3 2Y3 1Y1 2Y2 1Y4 2Y4 1Y2 2Y1
G1 G2
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
SH1

SH1 RFSH
SH1 MI
SH1 MREQ
SH4 9KRD
SH1 BUSACK
SH4 CCLK
SH4 DMAR
SH1 MEMR
SH1 BUSACK
SH4 DCLK
SH4 QBCLK

A110 74LS04
A20 74LS00
A19 74LS10
A114 74LS51
A113 74LS74
A108 74LS74
A109 74LS08
A91 74LS32
R61 4.7K
R60 4.7K
+5V

MREQ SH1
AD15

BKC0025-001

PARTS LIST						
QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION			MATERIAL SPECIFICATION
APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN HHUR 4-22-82	TeleVideo, Inc.		
NEXT ASSY	USED ON	ANG ± PLC ± PLC	CHK			
			ENG	TITLE PCB SCHEMATIC 970 CONT BD		
		SCALE	APPD			
		MATERIAL	APPD			
		FINISH — 4	APPD	SIZE D	SHT 3 OF 10	DRAWING NO 2021300	REV J3

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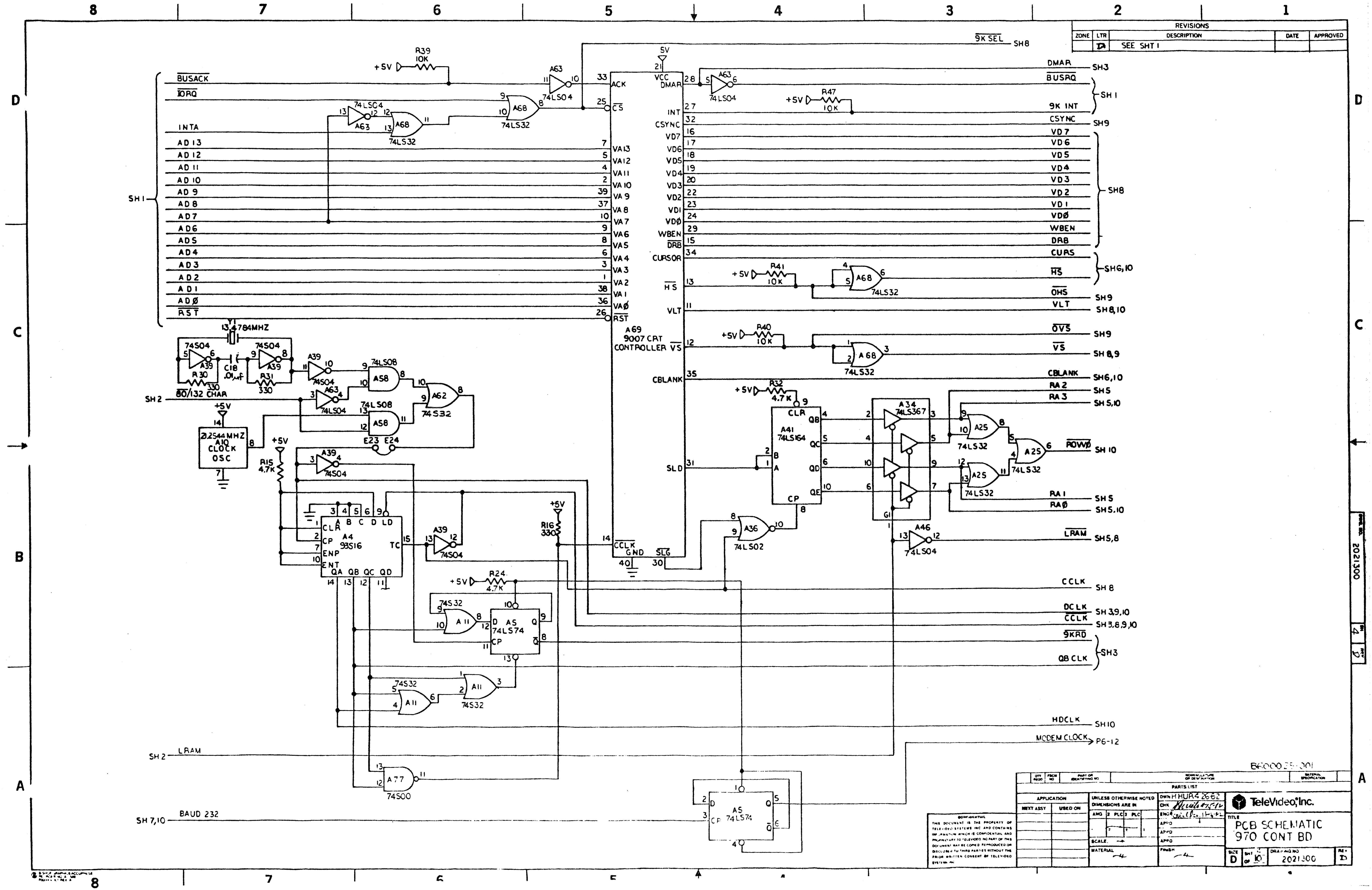
2021300 3 D


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
D SEE SHT 1
A69 9007 CRT CONTROLLER
A41 74LS164
A34 74LS367
A4 93S16
A10 21.2544 MHZ CLOCK OSC
13.4784MHZ
80/132 CHAR
BUSACK
IORQ
INTA
RST
9K SEL
DMAR
BUSRQ
9K INT
CSYNC
WBEN
DRB
CURS
OHS
VLT
OVS
VS
CBLANK
POWD
LRAM
CCLK
DCLK
9KRD
QB CLK
HDCLK
MODEM CLOCK
BAUD 232
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PCB SCHEMATIC
970 CONT BD
2021300
B4000 25-001
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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	ID	SEE SHT 1		

SH10 DCLKA
SH1 IOW
SH10 LAEN
SH10 CAD3
CHAD7
CHAD6
CHAD5
SH8 CHAD4
CHAD3
CHAD2
CHAD1
CHADØ
SH10 UPSEL
DB7
DB6
DB5
SH1 DB4
DB3
DB2
DB1
DBØ
SH9 FNØ1
SH4 RA0
RA1
RA2
RA3
SH9 FNØØ
SH10 CCLKA
DCLKA
SH9 FN Ø2
SH4 LRAM
SH10 HDINH
SH2 NHDSFT
SH6 DHDEN

A71 74LS32
A25 74LS32
A71 74LS32
A47 74LS32
A71 74LS32

E41 E42
+5V R44 4.7K
A76 74LS04
P/W
A56 6116/2716/2732
A40 74LS157
A64 74LS374
A33 74LS173
OE DEN
A65 74LS245
NBT245
G DIR
LREN

+5V R36 4.7K
A50 74-LS166
CLR QH SIN INH CLK LOAD
+5V R35 1K
A49 74S74
+5V R37 4.7K
A55 74LS163
ENP ENP QA QB QC LP
74LS08 A32
74LS08 A32
+5V R23 4.7K
A24 74LS74
A24 74LS74
A76 74LS04
74LS08 A66
74LS08 A66
A48 74S251
A46 74LS04
A46 74LS04
A47 74LS32
DOT SERIAL SH6
HDEN SH6

B60 0025-001

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± PLC ± PLC
SCALE
MATERIAL
FINISH

DWN HIBARGER-S2
CHK
ENG
APPD
APPD
APPD

TeleVideo, Inc.
TITLE PCB SCHEMATIC 970 CONT BD
SIZE D SHT 5 OF 10 DRAWING NO 2021300 REV I

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2021300 SHT 5 REV D

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		

SHT 10 CCLKA

SHT 5 HDEN

SHT 10 ROW BLANK
SHT 2 CURSOR BLINK
SHT 4 CURS

SHT 2 BLOCK/LINE CUR
SHT 10 ROW 9

SHT 4 CBLANK

SHT 4 HS

SHT 8 BLINK
SHT 2 BLINK CLK

SHT 8 BLANK

SHT 5 DOT SERIAL

SHT 8 UNDER LINE

SHT 8 REVERSE VIDEO
SHT 2 BOW/WOB
SHT 8 HALF INTENSITY
SHT 2 TIME OUT BLANK

A12, A12, A47 — 74LS08, 74LS08, 74LS32

A6 74LS374 (CP, D3, DØ, D6, D7, D5, D4, D2, D1, OE; Q3, QØ, Q6, Q7, Q5, Q4, Q2, Q1)

DHDEN SHT 5

DC BLANK SHT 10

A2 74LS04 → HS P2-1

A38, A38 — 74LS00
A47 — 74LS32
A46 — 74LS04
A38 — 74LS00
A39 — 74S04
A38 — 74LS00
A30, A30 — 74LS00
A22, A22 — 74LS86
DCURS

A7 — 74LS32
A22 — 74LS86
A14 — 7406
A14 — 7406
A14 — 7406
A14 — 7406

R17 270
R6 1K
R18 270
R19 330
R5 22 → +5V
C6 4.7uf 16V
VIDEO SHIELD GND → P2-3
R7 1K
R75 68 → VIDEO P2-4
VMIX SHT9

CR1 IN914
Q3 2N2219A

P5-5 → +12V
P5-4 → +5V
P5-1 → -5V
P5-3

C9 330PF 50V
C8 330PF 50V
C7 330PF 50V
C1 22uf 15V
C5 22uf 15V
C2,42-45 .1
VR1 LM 79L05 ACZ (-12V IN, OUT, GND)
C61,63,65 .1
C38-41, 46-52, 54, 56, 58-60, 62, 64, 66, 68-160 .1
C3 22uf 15V
C4,53,55,57 .1
C25 .1

B600025-001

PARTS LIST							
QTY ASSY	FSCM NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION				MATERIAL SPECIFICATION
APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN M.BELL	TeleVideo, Inc.			
NEXT ASSY	USED ON	ANG ± PLC ± PLC	CHK				
			ENGR	TITLE PCB SCHEMATIC 970 CONT BD			
		SCALE	MATERIAL	APPD	FINISH	SIZE D	DWG NO 2021300 REV E
						SHT 6 OF 10	

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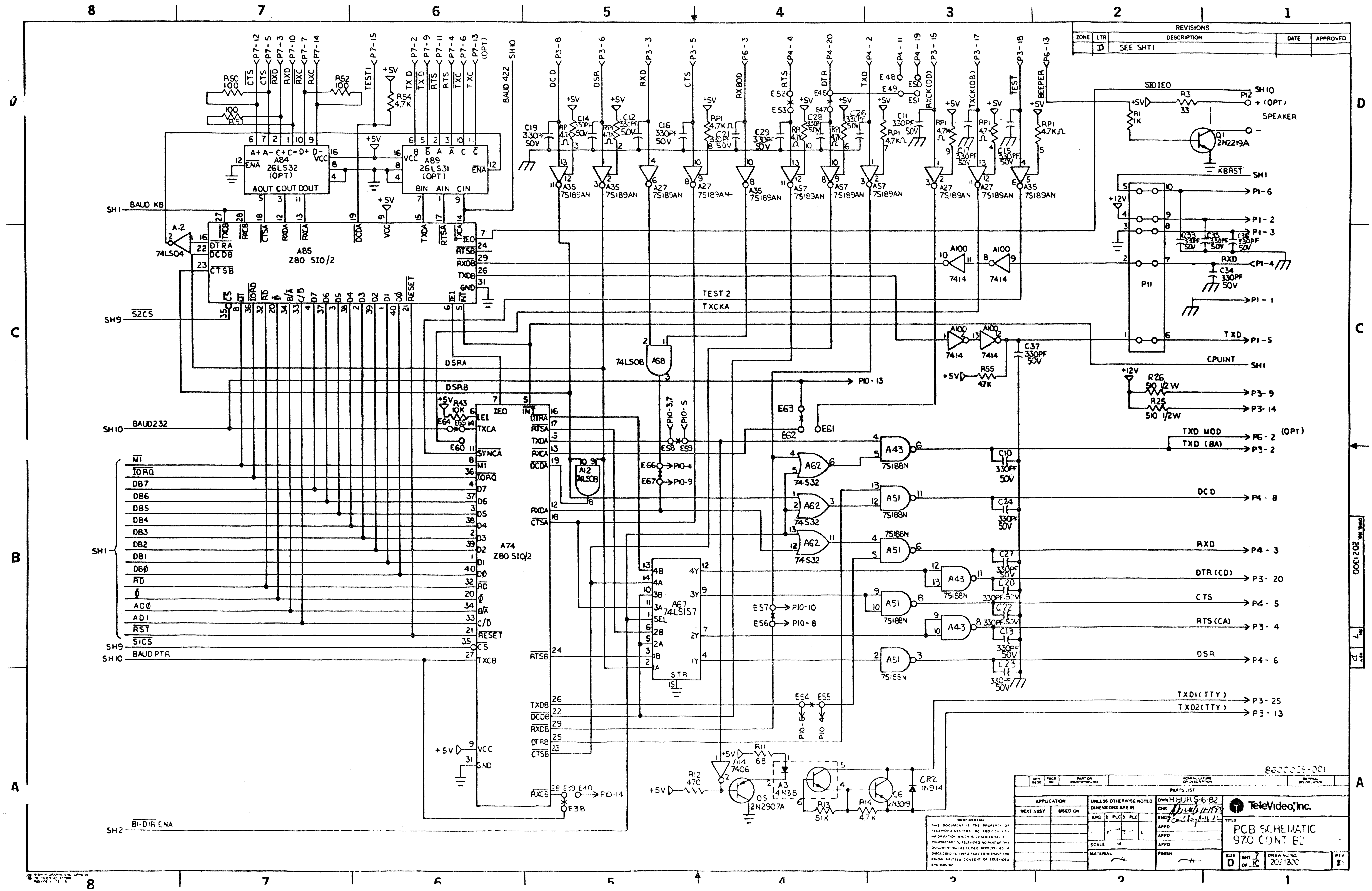
2021300 6 D


REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
SEE SHT1
A85
Z80 SIO/2
A74
Z80 SIO/2
A84
26LS32
(OPT)
A89
26LS31
(OPT)
A67
74LS157
A58
74LS08
A12
74LS08
A62
74S32
A43
75188N
A51
75188N
A100
7414
A35
75189AN
A27
75189AN
A57
75189AN
A14
7406
A3
4N38
Q1
2N2219A
Q5
2N2907A
Q6
2N3019
CR2
1N914
SPEAKER
KBRST
SIOIEO
TEST 2
TXCKA
DSRA
DSRB
CPUINT
BAUD KB
BAUD232
BAUD PTR
BAUD 422
BI-DIR ENA
TXD MOD
TXD (BA)
DCD
RXD
DTR (CD)
CTS
RTS (CA)
DSR
TXD1(TTY)
TXD2(TTY)
P11
B620025-001
PARTS LIST
APPLICATION
NEXT ASSY
USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
DWN H HUR 5-6-82
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TeleVideo, Inc.
TITLE
PCB SCHEMATIC
970 CONT BD
SIZE D
SHT 7 OF 10
DRAW NO 2021300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		

SH10 CCLKA

SH1 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBØ

SH4 LRAM VS CCLK — 74LS00 A30

SH1 BUSACK — SH4 WBEN — A81 74LS32

SH4 9KSEL — A58 74LS08

SH1 IOR — A63 74LS04

SH4 VD7 VD6 VD5 VD4 VD3 VD2 VD1 VDØ

A70 74LS245 N8T24SN — B7 B6 B5 B4 B3 B2 B1 BØ / A7 A6 A5 A4 A3 A2 A1 AØ

A54 9006-135 — CKEN OE DO7..DO0 DI7..DI0 WBEN CLK CLRCNT

A60 9006-135 — OE DO7..DO0 DI7..DI0 WBEN CKEN CLK

A53 9006-135 — CKEN CLRCNT OE DO7..DO0 DI7..DI0 WBEN CLK

A59 9006-135 — OE DO7..DO0 DI7..DI0 WBEN CKEN CLK CLRCNT

A61 74LS374 — D7..D0 CP OE Q7..Q0

A45 74LS374 — D7..D0 CP OE Q7..Q0

A37 74LS374 — D7..D0 CP OE Q7..Q0

CHAD7 CHAD6 CHAD5 CHAD4 CHAD3 CHAD2 CHAD1 CHADØ

CHAD7 CHAD6 CHAD5 — SH5,10

CHAD4 CHAD3 CHAD2 CHAD1 — SH5

CHADØ — SH 5,10

CKEN1

CLR1

OE1

CLR2

A7 74LS32

A28 74LS157 — 1A 2A 2B 1Y 2Y S G

HALF INTENSITY
UNDER LINE
REVERSE VIDEO
BLINK
BLANK
— SH6 — SH6,9

OE2

WBEN1

WBEN

OE1

A63 74LS04

VLT

+5V R34 4.7K

A52 74LS157 — S 1A 1B 2A 2B 3A 3B 4A 4B 1Y 2Y 3Y 4Y

A44 74LS109 — S J CK K R Q

A44 74LS109 — S J CK K R Q

CLRLD

SH4 CCLK VLT DRB

SH10 HCCLK

A36 74LS02

WBEN2

A46 74LS04

B-800035-001

PARTS LIST

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN: ANG ± PLC ± PLC

SCALE

MATERIAL

FINISH

DWN H.H.L. 4 28 82
CHK
ENG
APPD
APPD
APPD

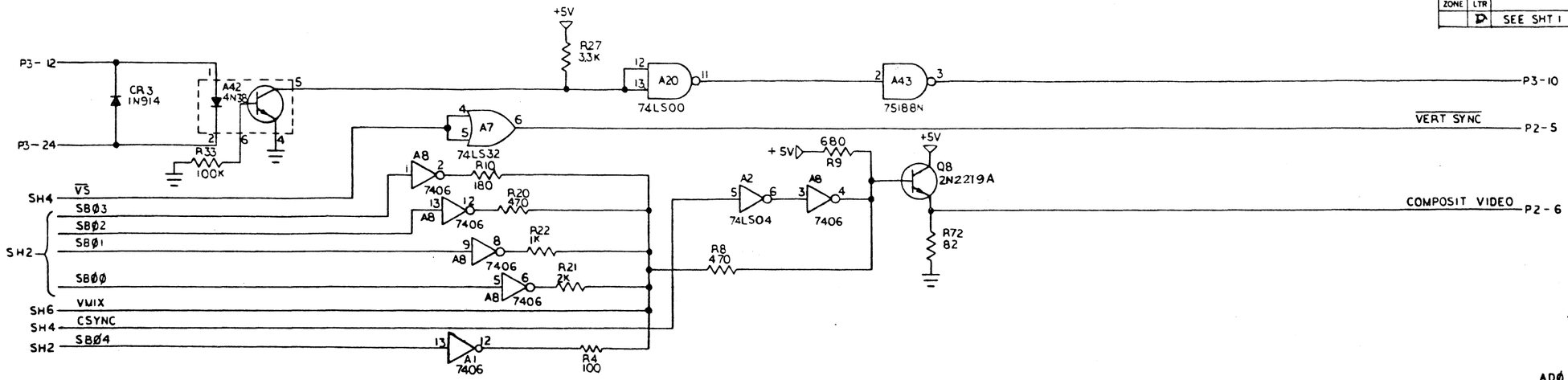
TeleVideo, Inc.

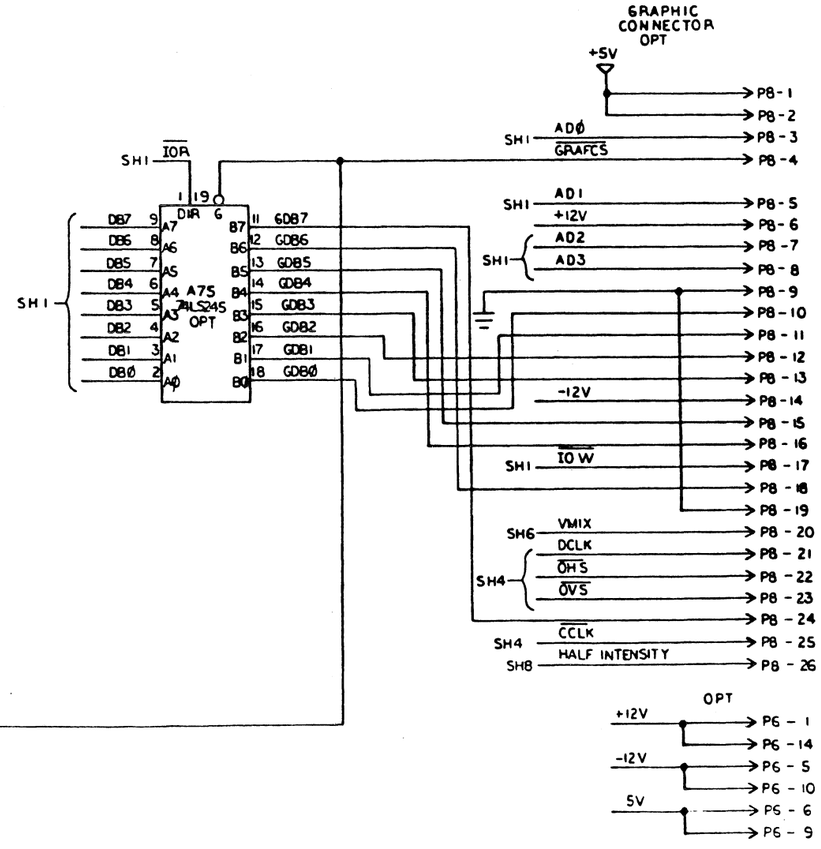
TITLE: PCB SCHEMATIC 970 CONT BD

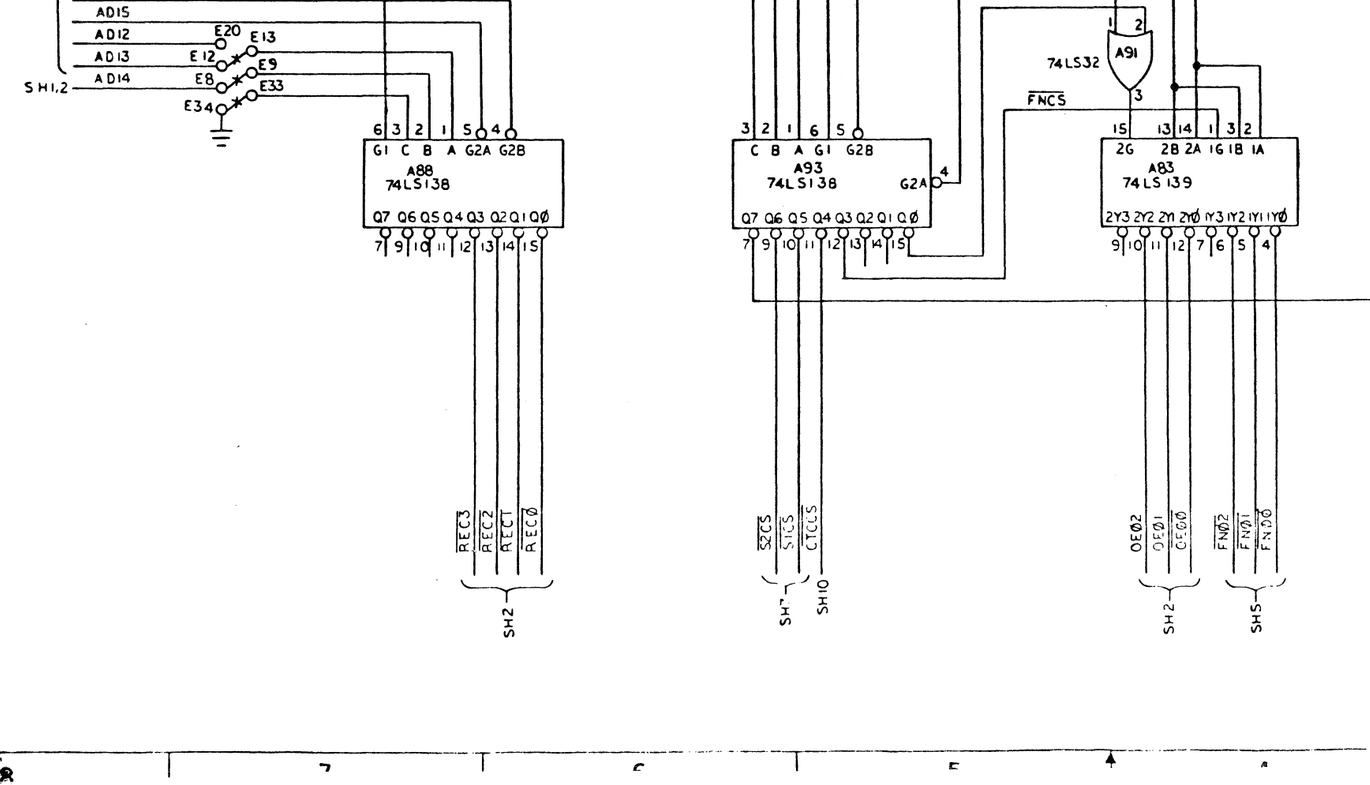
SIZE D | SHT 8 OF 10 | DRAWING NO 2021300 | REV D

2021300 8 D

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		







PARTS LIST					
QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL	

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN		
NEXT ASSY	USED ON	ANG ±	3 PLC ±	3 PLC ±
		SCALE		
		MATERIAL		

DWN	THURSTON 5-10-82	TeleVideo, Inc.
CHK		
ENGR		TITLE PCB SCHEMATIC 970 CONT BD
APPD		
APPD		
APPD		
FINISH		SIZE D / DRAWING NO 2021300 / REV D

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		

SH4 CCLK
+5V R45 4.7K
A72 74LS74 D CK Q Q
A71 74LS32
HS
SH4 DCLK
HDCLK
A76 74LS04
SH6 DCBLANK
5V R46 4.7K
A72 74LS74 CP R
A66 74LS08
A73 74LS112 J K CP S R Q Q
A66 74LS08
CURS
CBLANK
SH4 RA Ø
RA 3
ROW Ø
SH 8 CHAD Ø
74LS08 A26
CHAD 7
CHAD 6
SH 8 CHAD 5
SH 2 FNCTL
SH 7 SIOIEO
SH 4 VLT
A18 74LS04
A17 74LS32
ROW 9
A91 74LS32
BCLK
DB7
DB6
DB5
DB4
DB3
DB2
SH 1 DB1
DBØ
IORQ
RD
MI
A01
A00
SH 9 CT CS
SH 1 RST
A52 Z80 CTC
CS CS0 CS1 M1 RD IORQ Ø D0 D1 D2 D3 D4 D5 D6 D7 CLK/TRG0 CLK/TRG1 CLK/TRG2 CLK/TRG3 IEI
RESET
ZC/TOØ ZC/TO1 ZC/TO2 INT IEO
BAUD32 SH 7,4
BAUDPTR SH 7
BAUD22 SH 7
COUNT SH 1
HCCLK SH 8
A78 74S00
A77 74S00
CCLKA SH6,8
A78 74S00
A78 74S00
A77 74S00
A78 74S00
A117 74S04
DCLKA
DCLKA SH5
CAD3
A16 74LS157
A38 74LS00
A32 74LS08
ROW BLANK SH6
UP SEL SH5
ROW 9 SH6
A18 74LS04
HDINH SH 5
A17 74LS32

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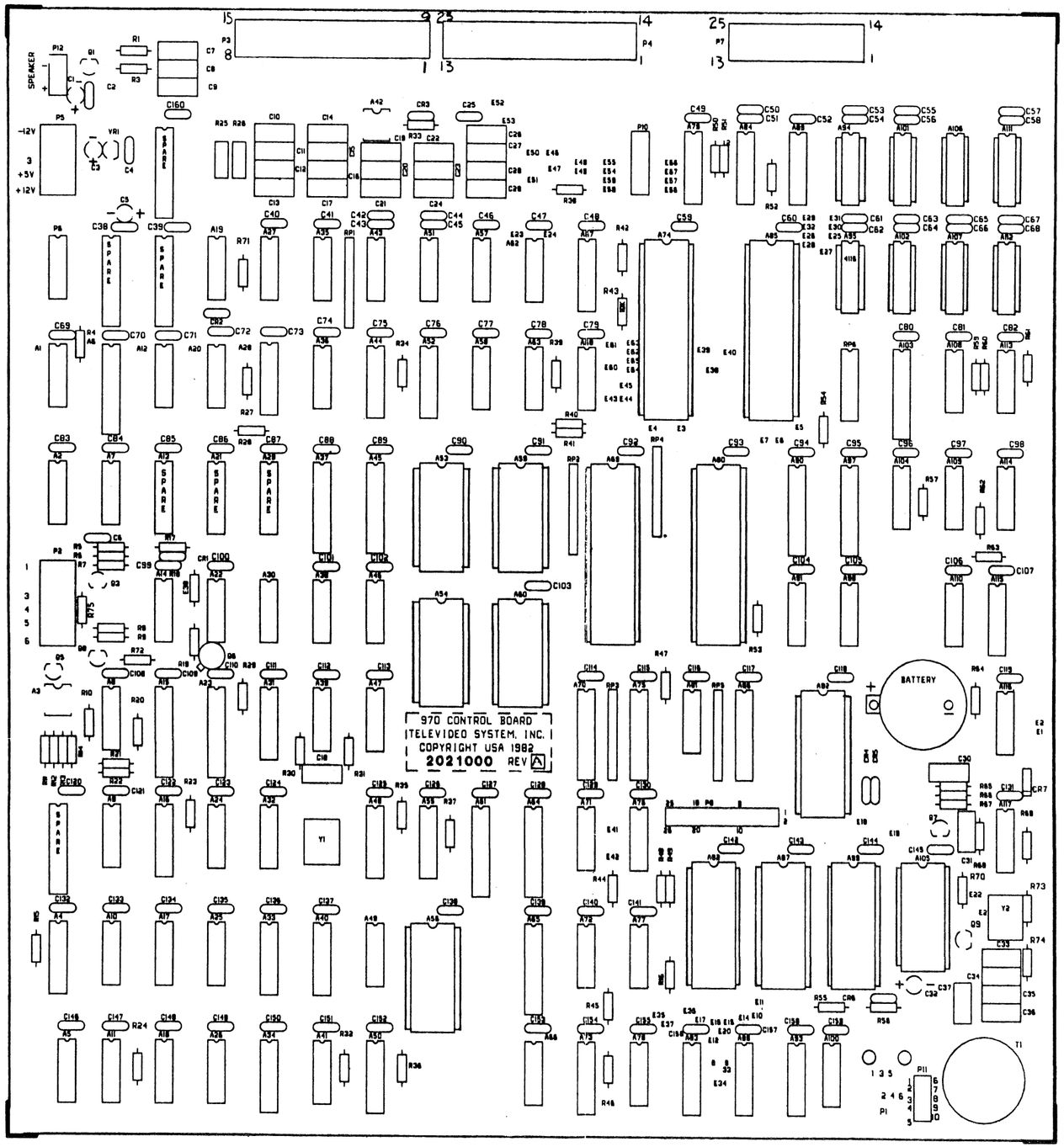
PARTS LIST					
QTY PER SET	PC BD NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION		REFERENCE DESIGNATION
APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H.HUR 5-10-82	TeleVideo, Inc.	
NEXT ASSY	USED ON	ANG ± PLC ± PLC	CHK	TITLE	
		SCALE	APPD	PCB SCHEMATIC 970 CONT BD	
		MATERIAL	FINISH	SIZE D	SHT 10
				DWG NO 2021300	REV I

202300 10 D



970
Control Board
Rev. A

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
2	4	4								C1,3,5,32	Cap Elec 22uf 15V 5%	2025700
3	1	1								C6	Cap Tant 4.7uf 16V 10%	2027500
4	26	26								C7-17,19-24,26-	Cap Cer 330pf 50V 20%	2029100
										29,33-37		
5	125	125								C2,4,25,38-160	Cap Cer .1uf 50V 20%	2030100
6	1	1								C30	Cap Mono 47pf 100V 5%	2029500
7	2	2								C18,31	Cap Mono .01uf 50V 10%	2028900
8												
9												
10	1	1								A80	IC Z80A CPU A	2051000
11	1	1								A92	IC Z80A CTC A	2050800
12	2	2								A74,85	IC Z80A SIO/2A	2050600
13	2	2								A44,79	IC 74LS109	2027000
14	1	1								A73	IC 74LS112	2138500
15	7	7								A5,24,72,104,108,	IC 74LS74	2026600
										113,116		
16	2	2								A39,117	IC 74S04	2024600
17	6	6								A2,18,46,63,76,	IC 74LS04	2024800
										110		

NOTES:

TITLE
PCB ASSY CONTROL BOARD 970

DATE
5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
18	1	1								A100	IC 7414	2035400
19	7	7								A9,12,26,32,58,	IC 74LS08	2025200
										66,109		
20	3	3								A20,30,38	IC 74LS00	2024200
21	9	8								A7,17,25,47,62,	IC 74LS32	2025800
										68,71,81,91		
22	2	2								A86,103	IC 74LS244	2044200
23	2	2								A36,98	IC 74LS02	2041600
24	2	2								A88,93	IC 74LS138	2041000
25	1	1								A83	IC 74LS139	2027200
26	7	7								A6,15,23,37,45,	IC 74LS374	2029000
										61,64		
27	1	1								A31	IC 74LS174	2028200
28	1	1								A114	IC 74LS51	2026200
29	2	2								A90,97	IC 74LS241	2042000
30	2	2								A55,115	IC 74LS163	2027600
31	1	1								A41	IC 74LS164	2048200
32	1	1								A34	IC 74LS367	2028600
33	2	2								A65,70	IC 74LS245, N8T245N	2036200

NOTES:

TITLE

PCB ASSY CONTROL BOARD 970

DATE

5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
34	1	1								A33	IC 74LS173	2028000
35	1	1								A48	IC 74S251	2138600
36	1	1								A49	IC 74S74	2026400
37	1	1								A50	IC 74LS166	2027800
38	1	1								A19	IC 74LS10	2025400
39	3	3								A1,8,14	IC 7406	2034800
40	1	1								A22	IC 74LS86	2026800
41	5	5								A16,28,40,52,67	IC 74LS157	2027400
42												
43												
44	2	2								A43,51	IC 75188N	2029200
45	3	3								A27,35,57	IC 75189AN	2029400
46	1	1								A56	IC EPROM US/UK CHAR GEN	8000139
47	1	1								A82	IC 970 EPROM FIRMWARE	8000100
48	1	1								A69	IC 9007 CRT CONTROLLER	2139900
49	4	4								A53,54,59,60	IC 9006-135 BUFFER CRT	2140000
											SGL ROW	
50	8	8								A94,95,101,102,	IC 4116 16K DYNAMIC RAM	2139200
										106,107,111,112	120 ns	

NOTES:

TITLE
PCB ASSY CONTROL BOARD 970

DATE
5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
51	1	1								A105	IC 2Kx8 6116 CMOS	2138700
											STATIC RAM	
52	2	2								A3,42	IC 4N38	2035000
53	1	1								A10	21.2544 MHZ CLOCK OSC	2138900
54	1	1								A4	IC 93S16PC	2040800
55	1	1								A11	IC 74S32	2038800
56	2	2								A77,78	IC 74S00	2024000
57	1	1								A87	IC 970 EPROM FIRMWARE	8000101
58	1	1								A99	IC 970 EPROM FIRMWARE	8000102
59												
60	1	1								Y2	Cry 8.0000 MHZ	2098603
61	1	1								Y1	Cry 13.4784 MHZ	2141400
62	6	6								XA53,54,56,59,60,	Socket 24P IC DIP	2098401
										105		
63	4	4								XA69,74,80,85	Socket 40P IC DIP	2098402
64	8	8								XA94,95,101,102,	Socket 16P IC DIP	2098405
										106,107,111,112		
65	4	4								XA82,87,92,99	Socket 28P IC DIP	2098404
66	2	2								P2,5	Plug 5P Str Waf	2098802

NOTES:

TITLE

PCB ASSY CONTROL BOARD 970

DATE

5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
67	2	2								P3,4	Conn 25P PCB Metal	2165300
											D-Sub Fem	
68	1	1								P1	Conn 6P RJ12 970 Logic	2141200
											Bd	
69												
70												
71												
72												
73												
74	1	1								VR1	Volt Reg 79L05AC	2126200
75	9	9								R39-43,47-49,56	Res C/F 10K Ohm 1/4W 5%	2034100
76	2	2								R27,28	Res C/F 3.3KOhm 1/4W 5%	2052700
77	1	1								R9	Res C/F 680 Ohm 1/4W 5%	2037100
78	2	2								R5,67	Res C/F 22 Ohm 1/4W 5%	2033500
79	3	3								R3,59,71	Res C/F 33 Ohm 1/4W 5%	2034500
80	1	1								R72	Res C/F 82 Ohm 1/4W 5%	2144000
81	2	2								R11,75	Res C/F 68 Ohm 1/4W 5%	2051100
82	4	4								R4,50-52	Res M/F 100 Ohm 1/4W 5%	2034900
83	2	2								R66,73	Res C/F 220 Ohm 1/4W 5%	2040300

NOTES:

TITLE

PCB ASSY CONTROL BOARD 970

DATE

5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
84	4	4								R16,19,30,31	Res C/F 330 Ohm 1/4W 5%	2051500
85	2	2								R17,18	Res C/F 270 Ohm 1/4W 5%	2051300
86	5	5								R8,12,20,68,69	Res C/F 470 Ohm 1/4W 5%	2051700
87	8	8								R1,6,7,22,35,65,	Res C/F 1K Ohm 1/4W 5%	2052100
										70,74		
88	1	1								R13	Res C/F 51K Ohm 1/4W 5%	2032300
89	1	1								R33	Res C/F 100K Ohm 1/4W	2032100
											5%	
90	22	22								R14,15,23,24,29,	Res C/F 4.7K Ohm 1/4W	2053100
										32,34,36-38,44-	5%	
										46,53-55,57,60-		
										64		
91	2	2								R25,26	Res C/F 510 Ohm 1/2W	2045100
											5%	
92	1	1								RP6	Res PK 33 Ohm 16 Pin	2041700
											DIP	
93	3	3								RP1,3,5	Res Pk 4.7K Ohm 10P	2041300
											SIP	
94	1	1								R10	Res C/F 180 Ohm 1/4W 5%	2053300

NOTES:

TITLE

PCB ASSY CONTROL BOARD 970

DATE

5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
95	1	1								R21	Res C/F 2K 1/4W 5%	2036900
96	2	2								RP2,4	Res PK 2.2K Ohm 10P	2230000
											SIP	
97	2	2								Q5,7	Trans 2N2907A	2045900
98	6	6								CR1-6	Diode 1N914	2047500
99	4	4								Q1,3,8,9	Trans 2N2219A	2045300
100	1	1								Q6	Trans 2N3019	2045700
111												
112												
113												
114												
115												
116												
117	1	1								CR7	Diode Zener 1N756 8.2V	2244500
118	1	1									Battery Holder	2195500
119	1	1								B1	Battery	2050001

NOTES:

TITLE PCB ASSY CONTROL BOARD 970

DATE 5-23-83

TeleVideo Systems, Inc.

VIDEO MONITOR/POWER SUPPLY SCHEMATICS AND PARTS LIST

TeleVideo Systems, Inc.
1170 Morse Ave., Sunnyvale, CA 94086
(408) 745-7760 TWX 910-338-7633 "TVI VIDEO"

VIDEO MONITOR

The Video Monitor is made up of two sections; the vertical amplifier and the horizontal amplifier. These amplifiers provide the voltages necessary to drive the CRT yoke, which deflects the electron beam across the CRT.

The electron beam which is generated by the CRT electron gun is swept across and down the screen to create what are called scan lines, which we discussed in character generation. The movement of the beam is driven by vertical and horizontal sweep rates which are both determined by the display circuitry on the logic board. The horizontal sweep is approximatly 16KHz and the vertical sweep is usually 60Hz for domestic and 50Hz for European applications.

The Horizontal sync pulses coming into the Video Monitor are inverted by transistor Q305 and then trigger IC301. In the precision timing mode of operation, the pulse width of IC301 is precisely controlled by R304, R306 and C312. The output Of IC301 is then coupled by Q303 and Q301 to drive transformer T301. The output of T301 is then amplified by Drive transistor Q302. This transistor drives both horizontal yoke windings, as well as the step-up transformer that produces the anode high voltage and the grid voltage for the CRT grid in the neck of the CRT. A new width coil is used for better Raster width control.

The Vertical sync. pulse's coming into the Video Monitor are converted to a sawtooth wave-form. When this is first done the sawtooth pulse is going from a negative leading edge to a positive falling edge, the pulse goes through transistor Q202 and is inverted to it's usable form. Now the pulse is going from a positive 2 volt leading edge to a negative - 2.5 volt falling edge. The timing here is critical because with in one sawtooth pulse there are 250 horizontal pulse's that will occur. This is the total number of horizontal scan lines on the CRT. The sawtooth pulse has to be proportional to all the previous pulse's or the timing will be wrong for the vertical sweep as well as the horizontal sweep. When the vertical sweep is negitive Q201 is conducting and C202 will be discharging. During the positive portion Q201 will cut off and allow C202 to charge. During the time that C202 is charging the electron beam will be scanning. The vertical sweep scans from top to the bottom, once the scan reaches the bottom of the page a (blank) occurs the video beam is turned off and it is retraced back to the top of the screen, this is the time when C202 is discharging. After the retrace the beam is once again turned on and begins it's scan routine. Adjusting SFR1 (vert. height) and SFR2 (vert. linearity) will change the rate of charge of C202 thus changing the slope of the sawtooth pulse.

POWER SUPPLY

Voltages are created and regulated as follows. A 24VAC voltage is rectified by Diode D105, 106, 107 and 108 resulting in a 31VDC output. This 31V is then filtered through C106 (3300MF/50V) and applied to five Volt switching regulator IC103. The output voltage of IC103 is filtered by L101 (200uH 5%) and C110 (2200MF/10V).

The raw 24VDC voltages for the positive and negative 12VDC are rectified by Diodes D101, 102, 103 and 104. The +24V is regulated by IC101 and Q101 for output voltage +12V. This is then filtered through C116. Negative 12V is stabilized by IC102 and filtered by C105.

A 79 volt AC waveform is applied to the halfwave rectifier D109 which is filtered by C115. the resulting 92VDC level is then regulated by a series voltage regulator. The stabilization network comprised of sensing and control elements, Q103 and Q102.

The 75VDC level goes to the Cathode of the CRT tube and spot killed quickly by D501 and C506 to protect burn out on the screen surface of when user turned off.

The high voltage needed to drive the CRT tube V501 are derived from the flyback transformer T302 on the Video Monitor.

TUBE SPECIFICATION

14 INCH 90 DEGREE, HIGH RESOLUTION

DISPLAY TUBE

340CXB 4N

The 340CXB4N is a 14 inch 90 degree high resolution, rectangular display tube primarily intended for use as a alpha-numerical and graphic display tube for computer peripheral devices. The tube is provided with banded type integral implosion protection (with mounting lugs). The tube features a low reflectance, high contrast screen.

ELECTRICAL DATA

Heating
Indirect by AC or DC:
Heater voltage. . . . . .12.0 volts
Heater current. . . . . 75 nA

Focusing Method. . . . . Electrostatic

Deflection Method. . . . . Magnetic

Deflection Angles (Approx.)
Diagonal. . . . . 90 degrees
Horizontal. . . . . 80 degrees
Vertical. . . . . 65 degrees

Anode voltage . . . . . 16,000 max. volts
9,000 min. volts

Using high voltage with this tube internal flash-overs may occur, which may cause damage to the cathode of the tube and to various circuit components on the video monitor board. Therefore it is necessary to provide protective circuits using spark-gaps etc. These should be connected as illustrated in figure #1 below.

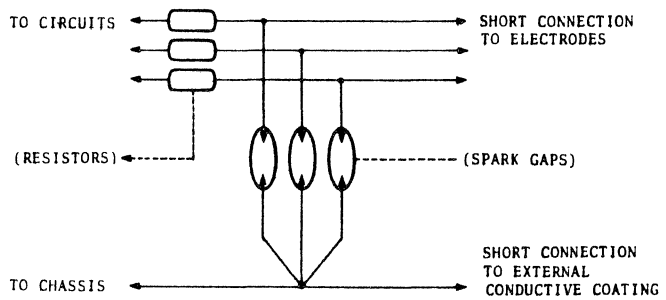


Figure 1.

No other connections between external conductive coating and chassis are permissible.

OPTICAL DATA

Faceplate	Filterglass
Anti-reflection treatment	Treated
Screen	Aluminized
Appearance	Low Reflective*

* The dark-colored screen, in combination with the filterglass, produces the low reflectivity (equivalent to a 20% light transmission filterglass) for easy-to-see display.

MECHANICAL DATA

Tube Dimensions:

Overall length	297.0 max. mm
Greatest dimensions of tube (excluding lugs)	
Diagonal	348.3 +/- 2.7 mm
Width	295.3 +/- 2.7 mm
Heigth	237.0 +/- 2.7 mm
Useful screen dimensions (projected)	
Diagonal	322.3 min. mm
Width	270.2 min. mm
Heigth	210.7 min. mm

Pin Position Alignment	Pin No 7 aligns approx. with anode contact.
Operating Position	Any
Weight (approx.)	3.5 kg
Implosion Protection	Tension band (with mounting lugs)

GENERAL CONSIDERATIONS:

1. Tube handling. Care should be taken not to scratch the tube.

2. Impact. The tubes should never be exposed to impacts of more than 30G during handling or transportation.

3. Grounding. The external conductive coating of the tube should be grounded with multiple contacts (e.g. a contact plate having many fingers.) Poor contact might cause local heating resulting in tube leakage.

WARNING

SHOCK HAZARD:

The high voltage at which the tube is operated may be very dangerous. Design of the equipment should include safeguards to prevent the user from coming in contact with the high voltage. Extreme care should be taken in the servicing or adjustment of any high voltage circuit.

Caution must be exercised during the replacement or servicing of the tube since a residual electrical charge is stored within the tube. Before handling the tube remove any undersible residual high voltage charge from the tube, by shorting the anode contact button to the frame of the terminal as illustrated in figure #2. Discharging the high voltage to isolated metal parts sucha as cabinets and control brackets may produce a shock hazard.

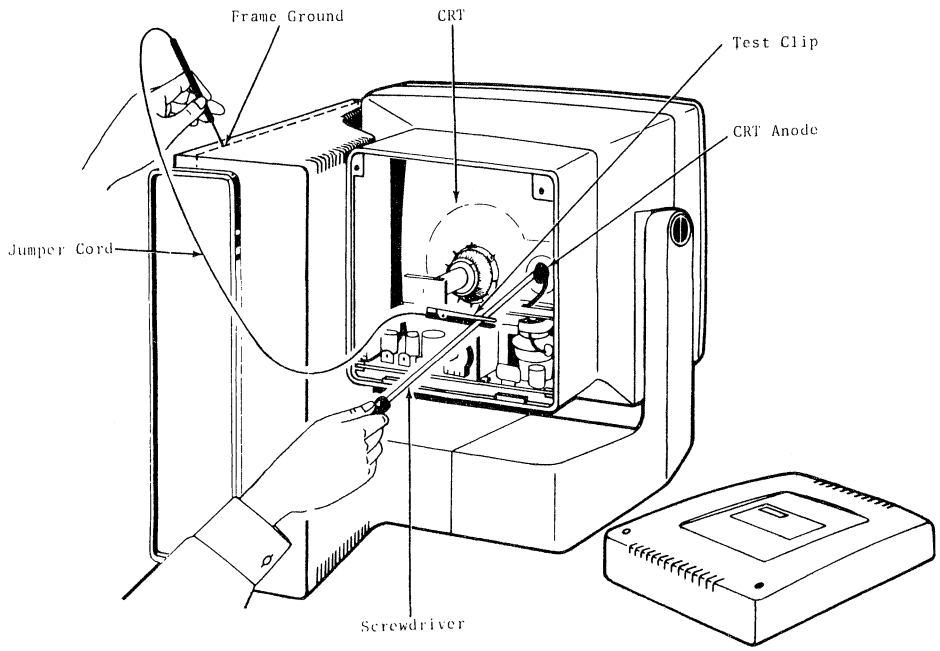
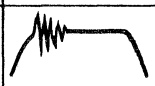
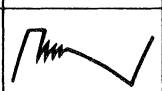
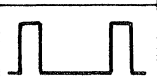
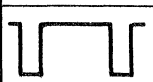
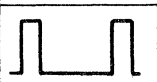
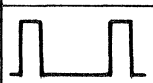


Figure 2.

TABLE 6-1
SIGNAL WAVEFORMS

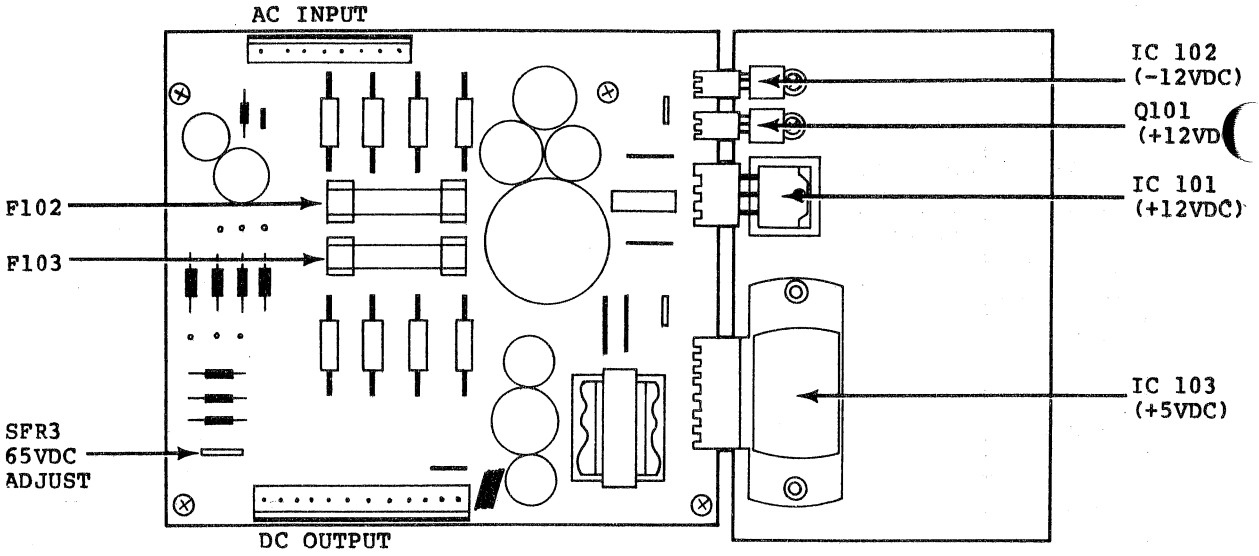
LOCATION	FUNCTION	DC	AC	BASE(IN)	DC	AC	COL.(OUT)	DC	AC	EMIT(GND)
IC101	REGULA-TION	22	1.0		12	0.0		0.0	0.0	
IC102	"	-22	0.0		-12	0.0		0.0	0.0	
IC013	"	28	1.0		5	0.0		0.0	0.0	
Q101	"	22	1.0		12	0.0		0.0	0.0	
Q102	"	65	0.0		100	1.0		65	0.0	
Q103	"	125	0.0		50	0.0		12	0.0	
Q201	VERT AMP	-0.8	3.0		-0.3	0.6		0.0	1.5	
Q202	"	0.2	0.5		3.5	8.0		0.0	0.0	
Q203	"	5.0	8.0		12	0.0		5.0	8.0	
Q204	"	4.0	8.0		0.0	0.0		4.0	8.0	
Q301	HORIZ AMP	-0.7	1.5		0.0	15		0.0	0.0	
Q302	"	-3.0	4.0		0.0	160		0.0	0.0	
Q303	"	2.2	1.5		3.0	1.5		0.8	3.5	
Q304	"	0.6	0.0		0.0	3.0		0.0	0.0	
Q305	"	-1.2	2.2		0.0	8.0		0.0	0.0	
Q501	VIDEO AMP	0.4	0.0		37	27		0.0	0.0	

ALL VOLTAGE MEASURES MADE WITH OSCILLOSCOPE

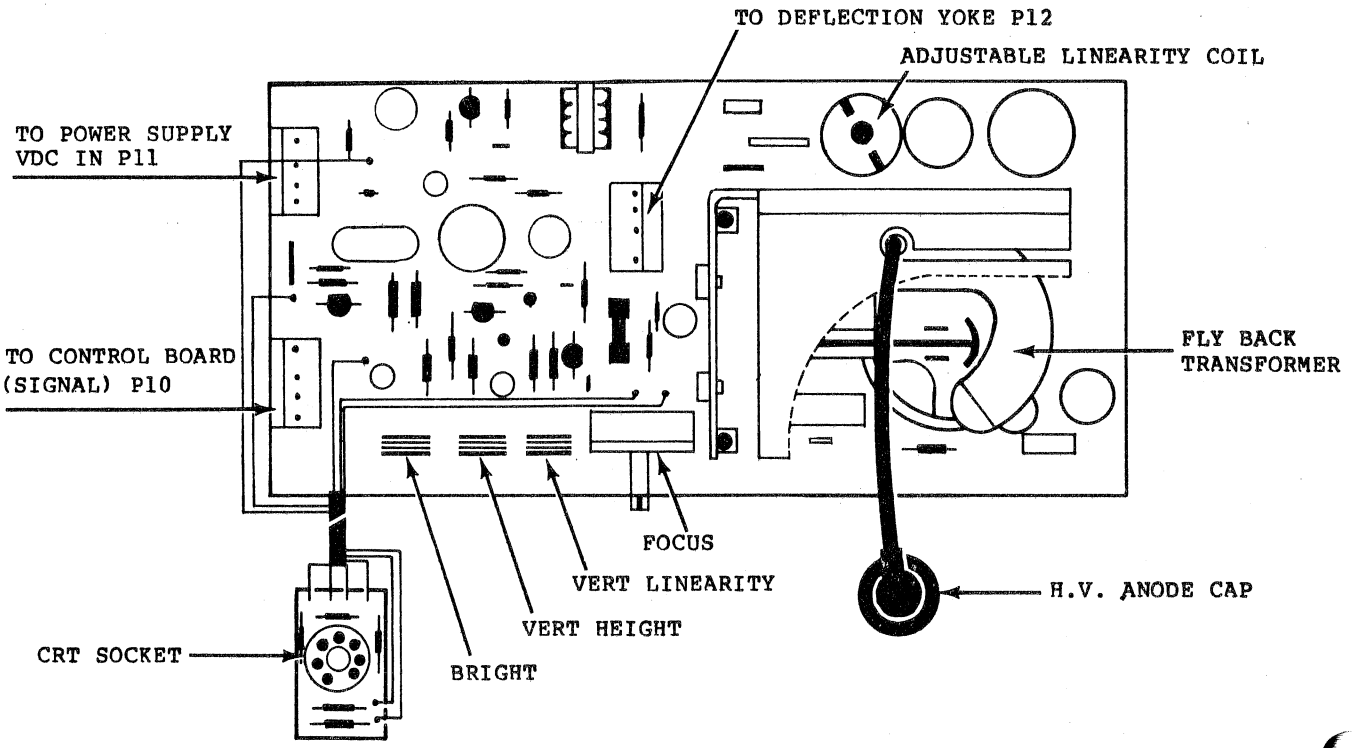
DC READING TAKEN OF SIGNAL BASELINE

AC READING TAKEN OF PEAK TO PEAK AMPLITUDE

NOTE: ANY RIPPLE MEASUREMENT LESS THAN ONE VOLT IS NOT ILLUSTRATED.



POWER SUPPLY



VIDEO MONITOR

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
		A	PROD RELEASE	2064	4/3/83	

VIDEO IN

P10

R201 2.7K
SFR1 100K
R202 100K
R203 2.2K
C201 10 16V
Q201 KTA1015
C202 4.7 25V
R204 0.6 2W
R205 2.7K
C203 22 / 16V
R206 820 1/2
SFR2 2KB
C204 4.7 / 25V
R207 6.8K
TH-201 1K
R208 4.7K
Q202 KTC1815
C205 100 10V
R209 47K
R210 330
Q203 2SC1173
C206 22 16V
D202
R211 150
R212 0.6 2W
C207 2200 10V
D201
R213 0.6 2W
C209 .001
Q204 2SA473

J12.3 V. YOKE
J12.1
J12.5
J12.4
R214 220 1/2W
C208 .047
KYS-00060 L601
H. YOKE
L301
L302
LINEARITY \ WIDTH COIL

R501 47
Q501 KTC 2229
C501 220P
R502 90
R505 47K
C505 22 / 100V
BRIGHT
JP7
R503 820 1/2W
SFR4 100K
R504 56K 1/2W
C503 .02
JP8
JP6
JP5
JP9
R506 220 1/2
R507 1.5K 1/2W
R508 10K 1/2W
S6 501 SPARK GAP
S6 502
S6 503
H3
H4
V501 340CXB31(N)
ANODE
VR2 2MB

D503 PLR 817
C504 0.1 800V
D502 PLR 817
C306 220/25V
C506 .47 100V
D501 1N914 OR KDS1553
C502 .1 / 100V
C306 NPHF 16 / 25V

D101-104 BY 251
F102 FUSE 3A / 125V
Q101 2SB595
R102 .4(WW)
IC101 3122P
C101 3300 35V
C102 3300 35V
C103 2.2 / 35V
C116 2200 16V
C104 2200 35V
IC 102 7912
C105 2.2 / 35V

D105-108 BY 251
F103 4A 125V
IC 103 SI-80506Z
L101 COIL 200UH
L102 COIL 1.4 UH
C106 3300
C107 .047
C108 .01
C109 .01
C111 3300 10V
C110 2200 10V
C112 0.1

D109 IN 4004
C113 .02
R103 4.7K
R104 4.7K
Q102 KTC 1627A
R105 30K
Q103 KTC 2229
R107 27K
SFR3 5K
R106 3.9K
D110 12V ZE
R108 2.7K
C115 100 / 160V
C114 22 / 160V

J1
J2
J3
K1
K2

R301 470
Q303 KTA 1015
C309 150 P
R302 5.6K
Q305 KTC1815
IC 301 555
R304 22K
C310 .01
D306 KDS 855A
R303 5.6K
R306 1.8K
R305 12K
C512 .015
C311 .01
R307 27K
R308 2.7K
C313 .039
Q304 KTC1815
C301 4.7 16V
Q301 KTC 200
D301 KDS 4448 OR 1N4448
C302 .01
H4 H3
HEATER
C308 1000 16V
C303 .0068 200V
C307 .039
Q302 2SC2233
D305 PFR852
D302 DS115A OR PFR852
C304 .035 400V
T301 HDT-19
T302 FBT KFS 120398E

SW102 POWER SELECT SWITCH
230V
115V
WHT
BLU
RED
BLK
R101 2.2M 1/2 W
F101 FUSE 1A 115V 0.5A 230V
SW101 POWER SWITCH
T101 POWER TRANS
GRN

NOTES:

1 ALL RESISTOR VALUES IN OHMS.

2 ALL CAPACITOR VALUES IN FARADS.

3 UNLESS OTHERWISE STATED, WORKING VOLTAGES OF CAPACITORS ARE 50 VOLTS.

4 THIS SCHEMATIC DIAGRAM COVERS BASIC OR REPRESENTATIVE CHASSIS ONLY. THERE MAY BE SOME COMPONENTS OT PARTIAL SCHEMATIC BETWEEN ACTUAL CHASSIS AND THE SCHEMATIC DIAGRAM.

1	Vpp 0.6	2	Vpp 8.0	3	Vpp 8.0	4	Vpp 15	5	Vpp 160

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED
DIMENSION — DECIMAL / INCH
X = ±
XX = ±
XXX = ±
ANGLES ±

CONTRACT NUMBER
DES. DATE 5/2/83
DR. DATE
CHK. DATE
ENGR. DATE 5/2/83
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
POWER SPLY VIDEO MON 970

SIZE	CODE IDENT		REV
D		3201200	A
SCALE		SHEET OF	

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
1									1	C503	Cap., Cer .02uF 50V	3018600
2									1	C309	Cap Cer 150pF 50V 10%	3013800
3									1	C501	Cap Cer 220pF 50V	2195900
4									1	C305	Cap Elec 220uF 25V	3012700
5									1	C306	Cap Elec 16uF 25V (non-	2280000
											P)	
6									1	C201	Cap Elec 10uF 16V 20%	2027300
7									2	C203,206	Cap Elec 22uF 15V 20%	3018900
8									1	C505	Cap Elec 22uF 100V	2196100
9									1	C205	Cap Elec 100uF 10V	2196000
10									1	C301	Cap Elec 4.7uF 16V	2196700
11									1	C207	Cap Elec 2200uF 10V	2196200
12									1	C308	Cap Elec 1000uF 16V	3018500
13									1	C303	Cap Mylar .0068uF 200V	2196800
											5%	
14									1	C209	Cap Mylar .001uF 50V	2196900
15									3	C302,310,311	Cap Mylar .01uF 50V	2197000
16												
17									1	C304	Cap Mylar .033uF 400V	3012600

NOTES:

TITLE 970 VIDEO MONITOR PARTS LIST

DATE 5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
18									1	C312	Cap Mylar .015uF 50V	3013900
											5%	
19									2	C307,313	Cap Mylar .039uF 50V	3014500
20									1	C502	Cap Mylar .1pF 100V	3016900
21									1	C506	Cap My.ar .47uF 100V	3018800
22									1	C208	Cap Mylar .047uF 50V	3016800
23									1	C504	Cap Mylar .1uF 800V	3018400
											10%	
24									2	C202,204	Cap Tant 4.7uF 25V 10%	3028400
25									1	L301	Coil Linearity 52MHz	3013400
26									1	L302	Coil Width 9MHz	3013500
27									2	D502,503	Diode PLR 817	3014700
28									2	D302,303	Diode PFR 852	3025100
29									1	D501	Diode 1N914	2047500
30									1	D301	Diode 1N4148 Switch	2048500
31									3	D201,202,306	Diode 1N920/KD8513A	2201800
32									1	IC301	IC NE555 Timer	2030200
33									1	VR2	Pot Focus 2M Ohm	2180100

NOTES:

TITLE

970 VIDEO MONITOR PARTS LIST

DATE

5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
34									1	SFR2	Pot Trim 2K Ohm Top-	2177800
											Adj Pcmt	
35									2	SFR1,4	Pot Trim 100K Ohm Top-	2177700
											Adj Pcmt	
36									1	R502	Res CF 90 Ohm 1/4W	2177600
37									1	R501	Res CF 47 Ohm 1/4W 5%	2037700
38									1	R211	Res CF 150 Ohm 1/4W 5%	2033900
39									2	R214,506	Res CF 220 Ohm 1/2W 5%	2186000
40									1	R210	Res CF 330 Ohm 1/4W 5%	2051500
41									1	R301	Res CF 470 Ohm 1/4W 5%	2051700
42									2	R206,503	Res CF 820 Ohm 1/2W 5%	2177000
43									1	R208	Res CF 4700 Ohm 1/4W 5%	2053100
44									3	R201,205,308	Res CF 2.7K Ohm 1/4W 5%	2038300
45									1	R203	Res CF 2.2K Ohm 1/4W 5%	2038700
46									1	R207	Res CF 6.8K Ohm 1/4W 5%	2039100
47									2	R507,509	Res CF 1.5K Ohm 1/2W 5%	2186300
48									1	R306	Res CF 1.8K 1/4W 5%	2052300
49									2	R302,303	Res CF 5.6K Ohm 1/4W 5%	3013600
50									1	R508	Res CF 10K Ohm 1/2W 5%	2186400

NOTES:

TITLE
970 VIDEO MONITOR PARTS LIST

DATE
5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
51									1	R305	Res CF 12K 1/4W 5%	3013700
52									1	R304	Res CF 22K Ohm 1/4W 5%	2036300
53									1	R307	Res CF 27K Ohm 1/4W 5%	2037300
54									2	R209,505	Res CF 47K Ohm 1/4W 5%	2033700
55									1	R504	Res CF 56K Ohm 1/2W 5%	3016500
56									1	R202	Res CF 100K Ohm 1/4W 5%	2032100
57									3	R204,212,213	Res WW 0.6 Ohm 2W	2177100
58									1	TH201	Thermistor OPC 1K Ohm	2180300
59									1	T302	Transformer Flyback	2269000
											12 VDC	
60									1	T301	TNFR Horiz DR HDT-19	2201200
61									3	Q202,305,304	Tran KTC 1815Y	3014600
62									2	Q303,201	Tran KTA 1015Y	3016700
63									1	Q204	Tran 2N6124/2SA473	2202100
64									1	Q203	Tran 2N6121/2SC1173	2199700
65									1	Q301	Tran KTC 200Y	3011700
66									1	Q501	Tran KTC 229Y	3011600
67									1	Q302	Tran KTC 2233	3011800

NOTES:

TITLE

970 VIDEO MONITOR PARTS LIST

DATE

5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
1									1	SW102	Switch Power Select	2097400
											DPDT	
2									1	SW101	Switch Power SPST	2097300
3									2	C108,109	Cap Cer .01uF 50V	3017800
4									1	C113	Cap Cer .02uF 50V	3018600
5									1	C112	Cap Cer .1uF 50V 10%	2030100
6									1	C115	Cap Elec 100uF 160V	2196300
7									1	C111	Cap Elec 3300uF 10V	3027600
8									1	C106	Cap Elec 3300uF 50V	3028100
9									1	C104	Cap Elec 2200uF 35V	3027500
10									2	C101,102	Cap Elec 3300uF 35V	2196500
11									1	C114	Cap Elec 22uF 160V	2196400
12									1	C110	Cap Elec 2200uF 10V	2196200
13									1	C116	Cap Elec 2200uF 16V	3016400
14									1	C107	Cap Mylar .047uF 50V	3016800
											10%	
15									2	C103,105	Cap Tant 2.2uF 35V	3027400
16									1	L102	Coil Air 1.4uH 5%	2268900

NOTES:

TITLE

970 POWER SUPPLY ASSEMBLY PARTS LIST

DATE

5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
17									1	L101	Coil Chock 200uH 5%	2268800
											Hi-Current	
18									8	D101-108	Diode BY251 3A 200V	3009800
19									1	D109	Diode 1N4004 MOT	2202200
20									1	D110	Diode 1N759A/RD12EB	2201600
											Zener	
21									1	F102	Fuse 3 Amp 125V 3AG	2193100
22									1	F103	Fuse 4 Amp 125V	3025300
23									1	SFR3	Pot Trim 5K Ohm Side	2177900
											Adj Pcmt A	
24									1	R107	Res CF 27K Ohm 1/4W 5%	2037300
25									1	R108	Res CF 2.7K Ohm 1/4W 5%	2038300
26									1	R106	Res CF 3.9K Ohm 1/4W 5%	2177400
27									1	R105	Res CF 30K Ohm 1/4W 5%	2039300
28									1	R102	Res WW .4 Ohm 2W 10%	3019500
29									2	R103,104	Res CF 4700 Ohm 1/4W 5%	2053100
30									1	Q101	Tran B595	3001600
31									1	Q102	Tran KTC1627/MPSA06	2046700
											NPN/SIL	

NOTES:

TITLE

970 POWER SUPPLY ASSEMBLY PARTS LIST

DATE

5-23-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
32									1	Q103	Tran Drv Pre 150V KTC	3011600
											TO-92L	
33									1	IC101	Volt Reg 3122P	3001700
34									1	IC102	Volt Reg 7912	3001800
35									1	IC103	Volt Reg SI-80506Z	2246400

NOTES:

TITLE

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