SYSTEMS CONCEPTS

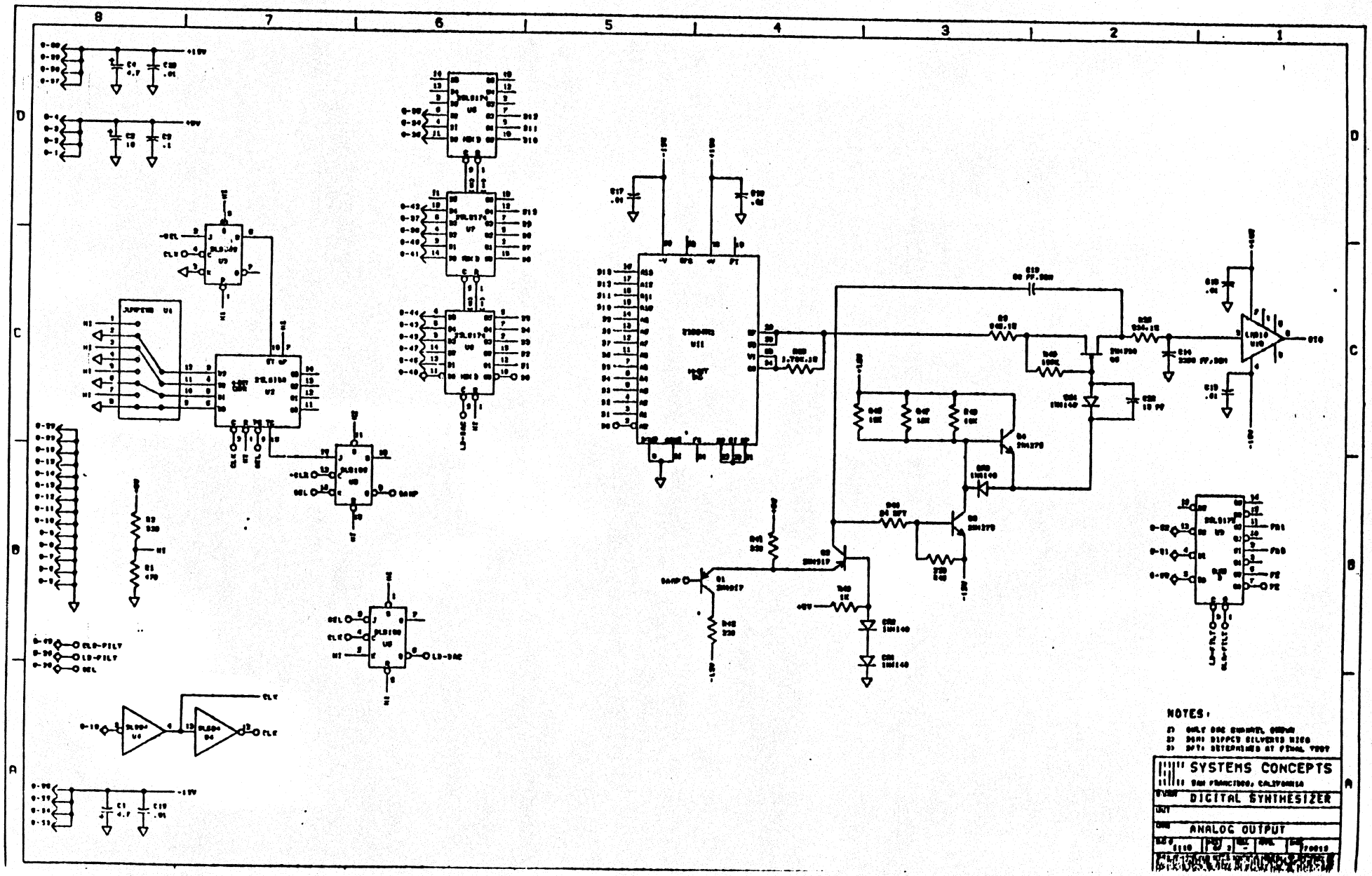
520 THIRD STREET SAN FRANCISCO, CALIFORNIA 94107

DIGITAL SYNTHESIZER
PRELIMINARY
ENGINEERING DRAWINGS
VOLUME 1

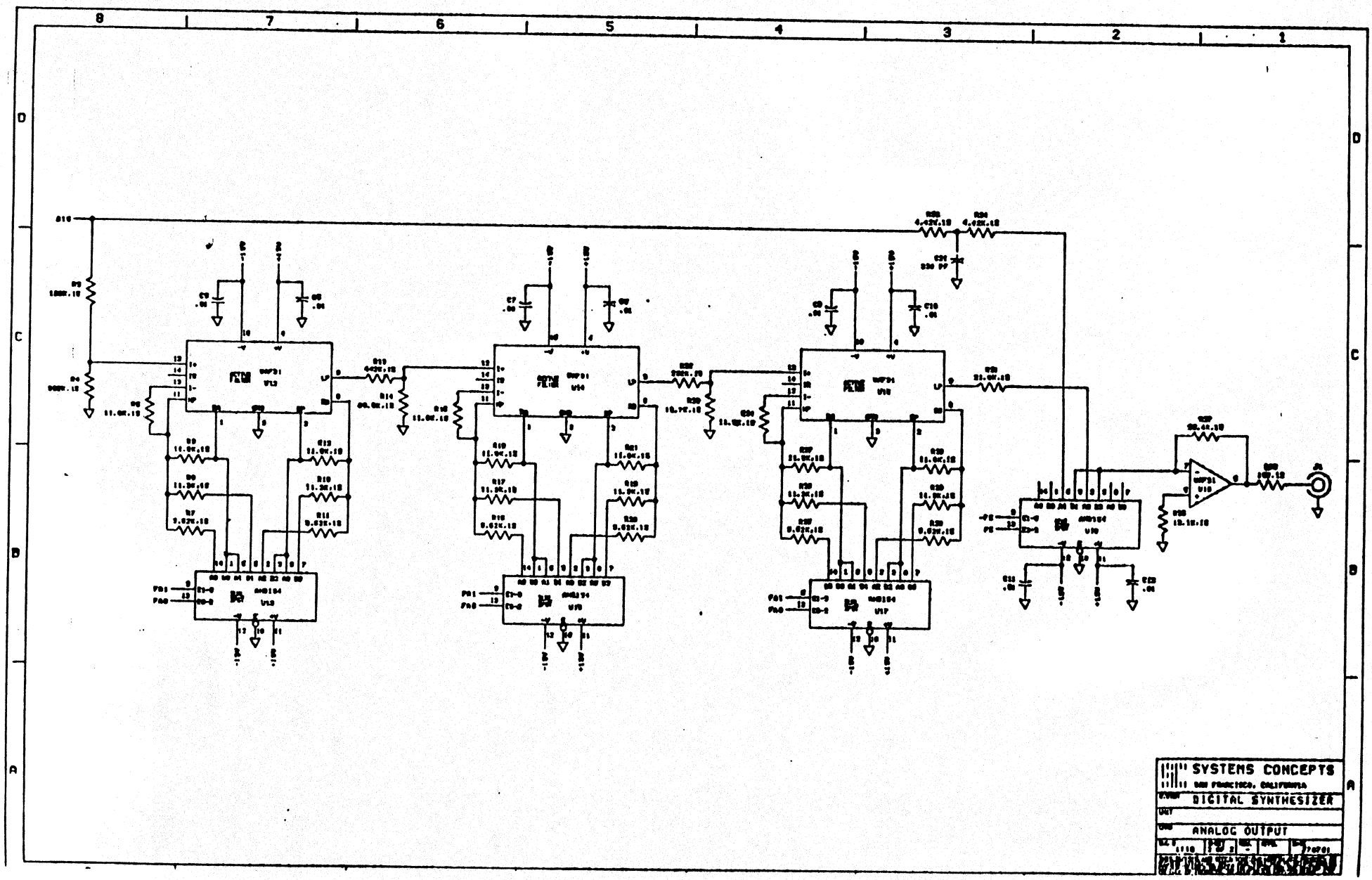
TELEPHONE: 415·442 1500 TWX: 910·372·6062

Exh. SC2

SFE; ANLOG1

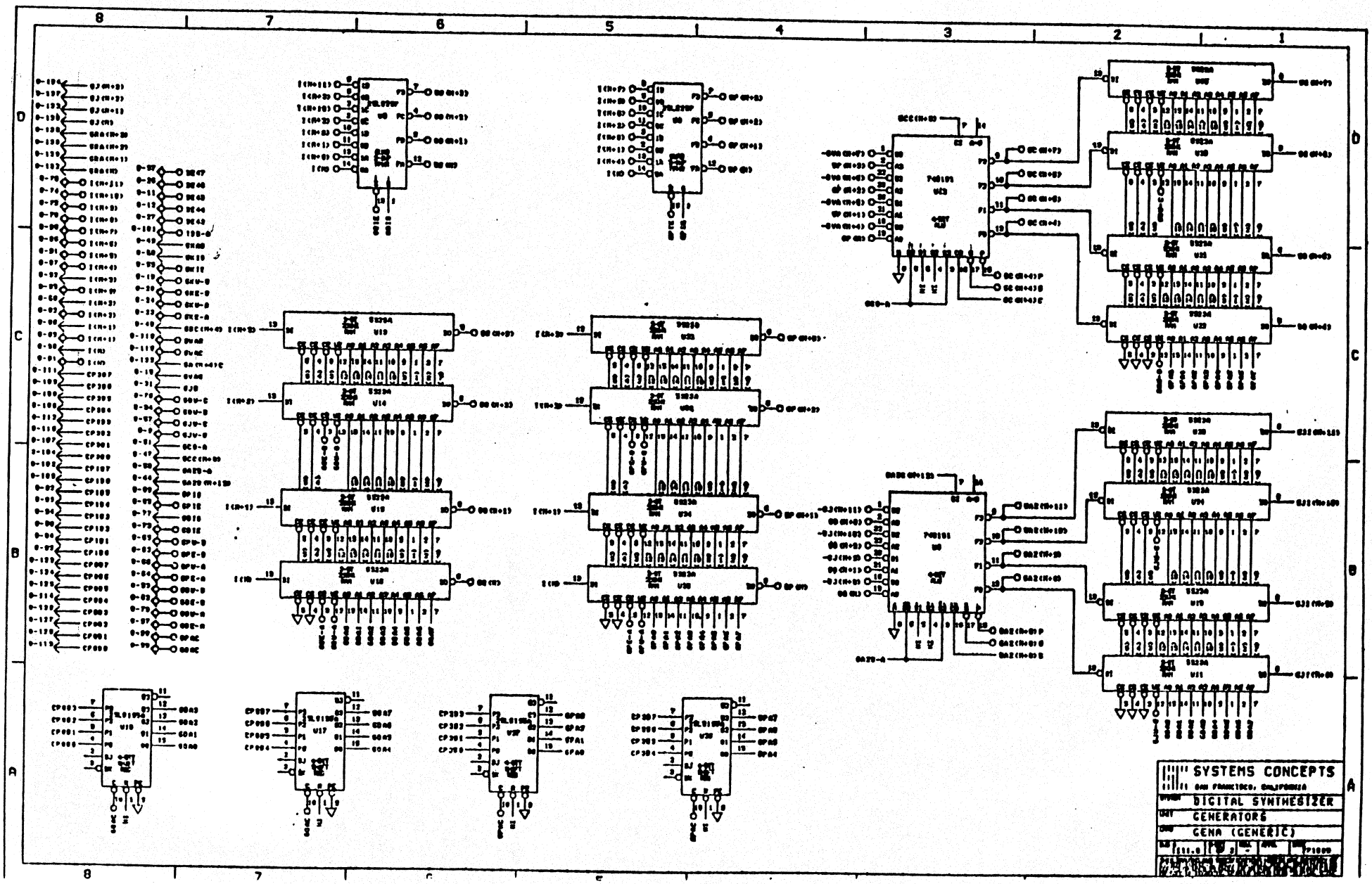

NOTES:
SYSTEMS CONCEPTS
DIGITAL SYNTHESIZER
ANALOG OUTPUT

SFE; ANLOG 2


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
ANALOG OUTPUT

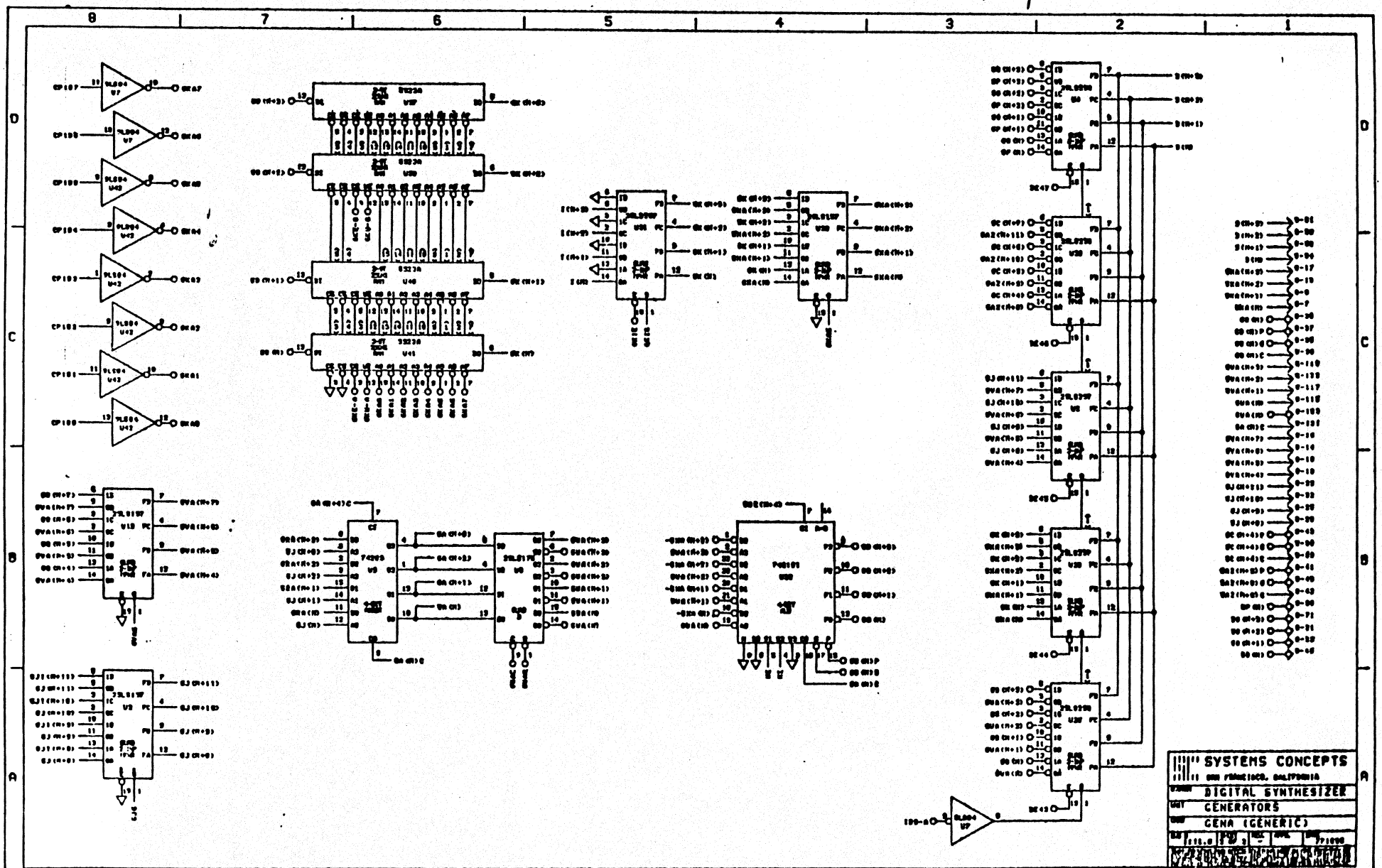
SWB;GENA1

PTF=1



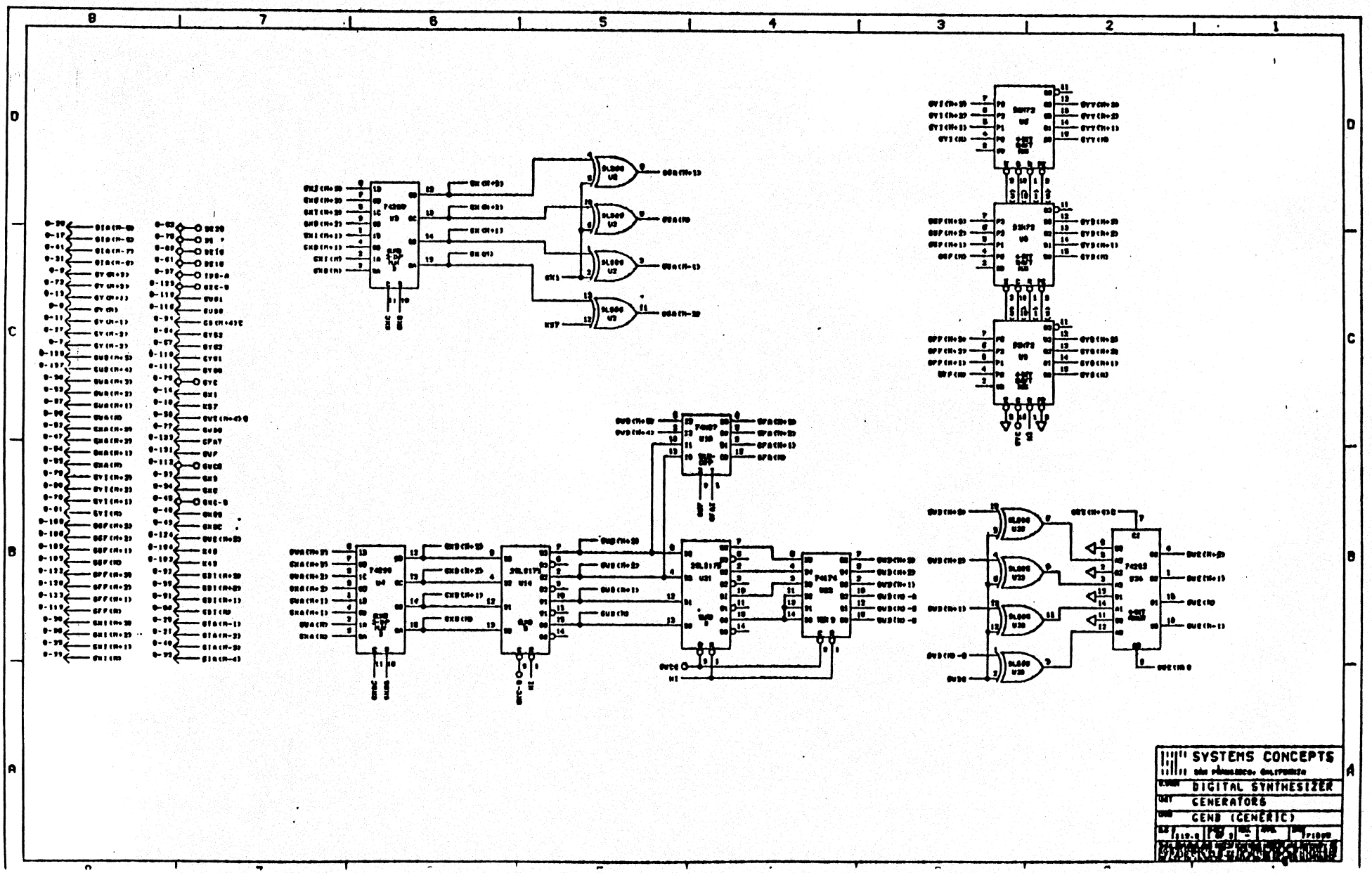
SWB; G ENA2

PTF=1



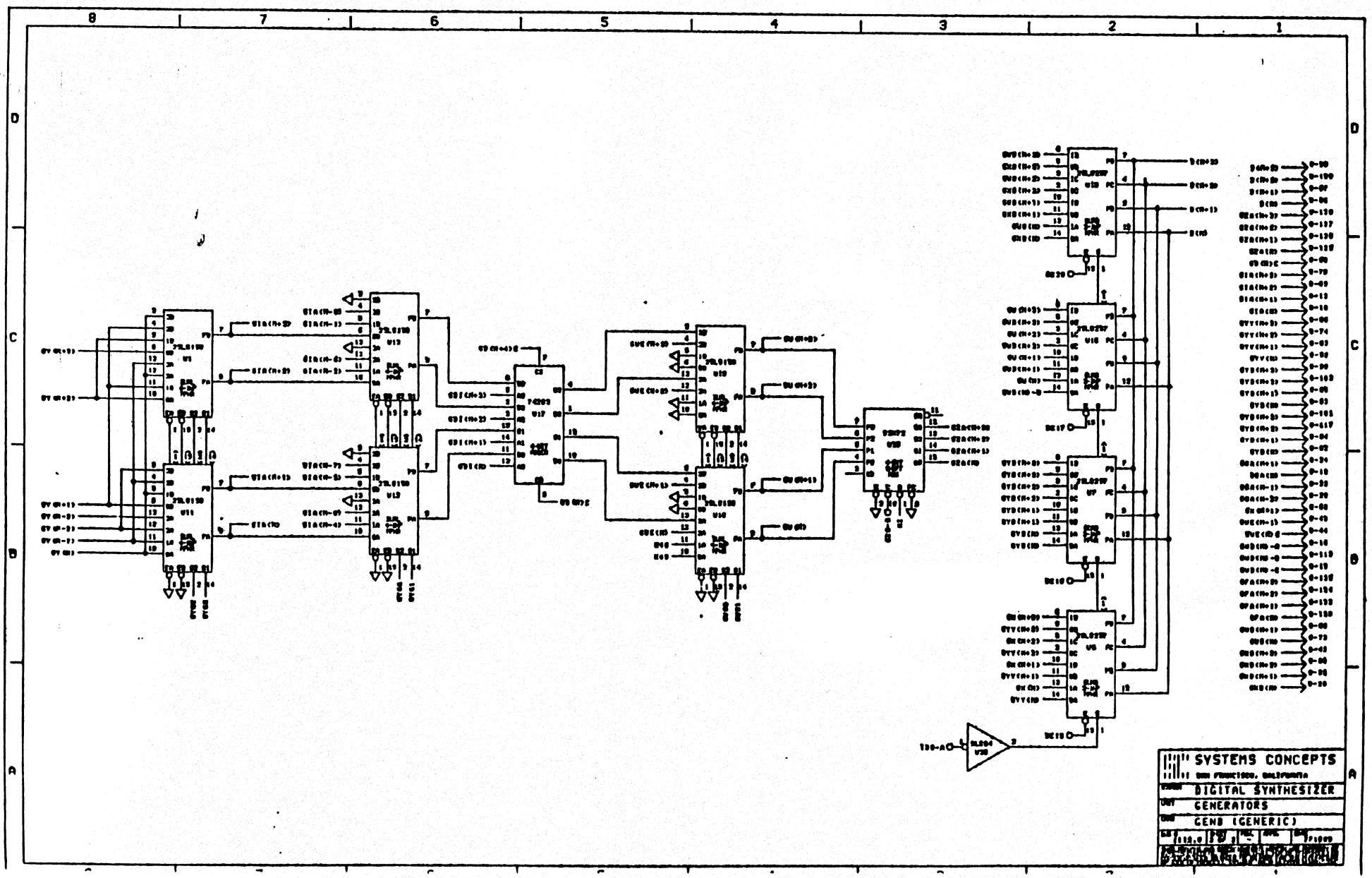
SWB; GENB1

PTF=1



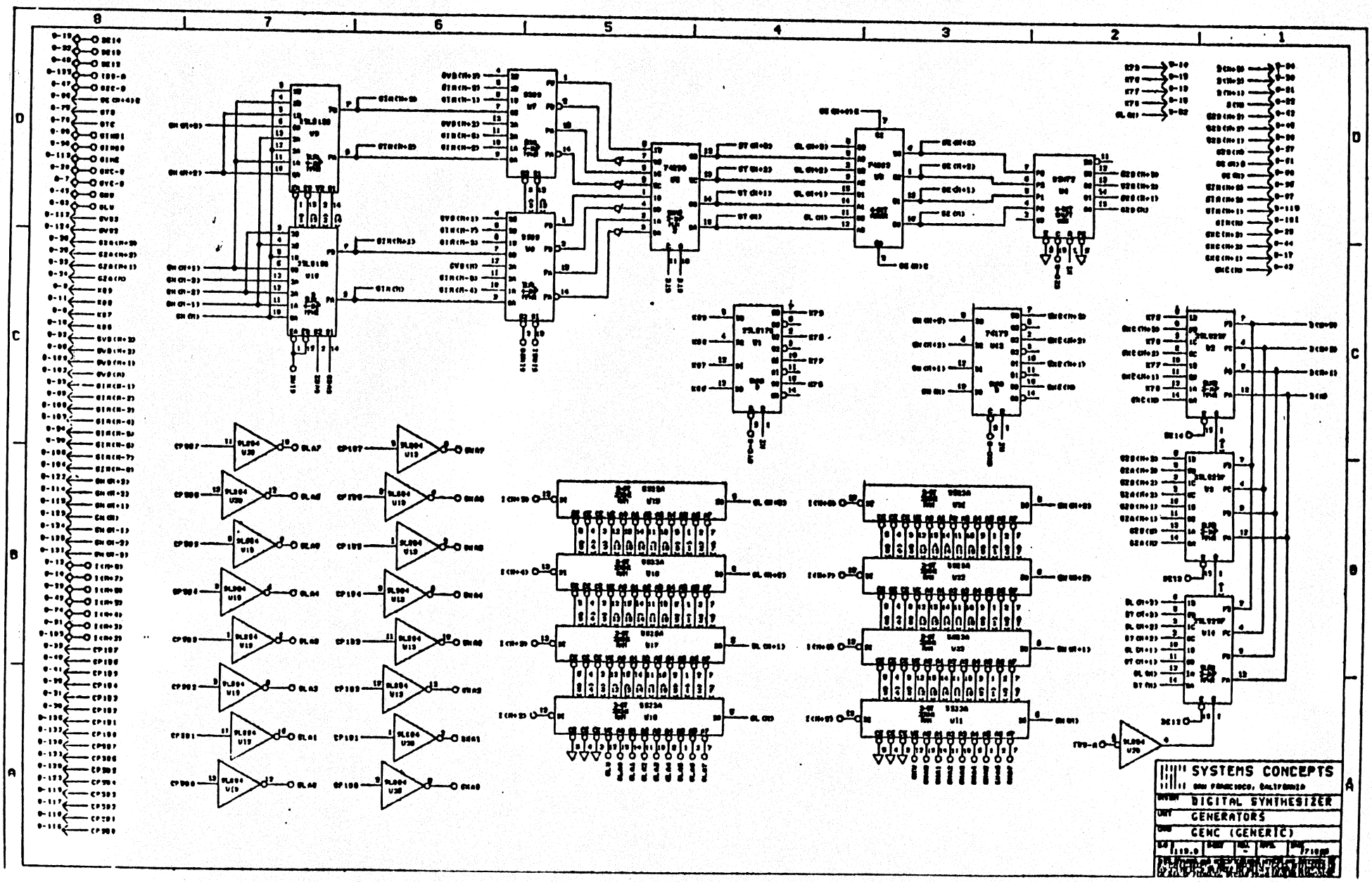
SNB; GENB?

PTF=2



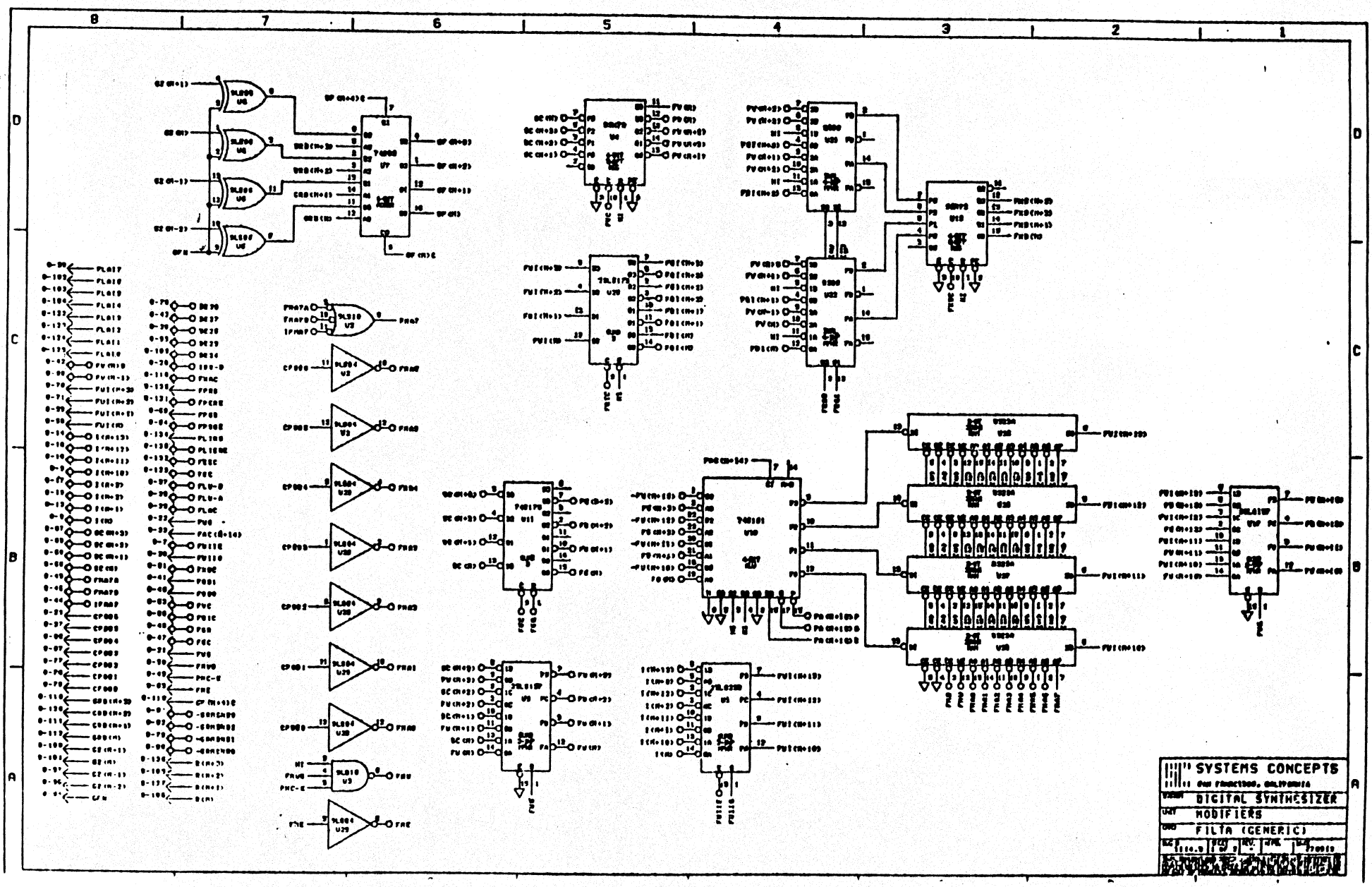
SFE; GENC

PTF=1



SFE; FILTA 1

PTF = 1



SFE;FILTA2

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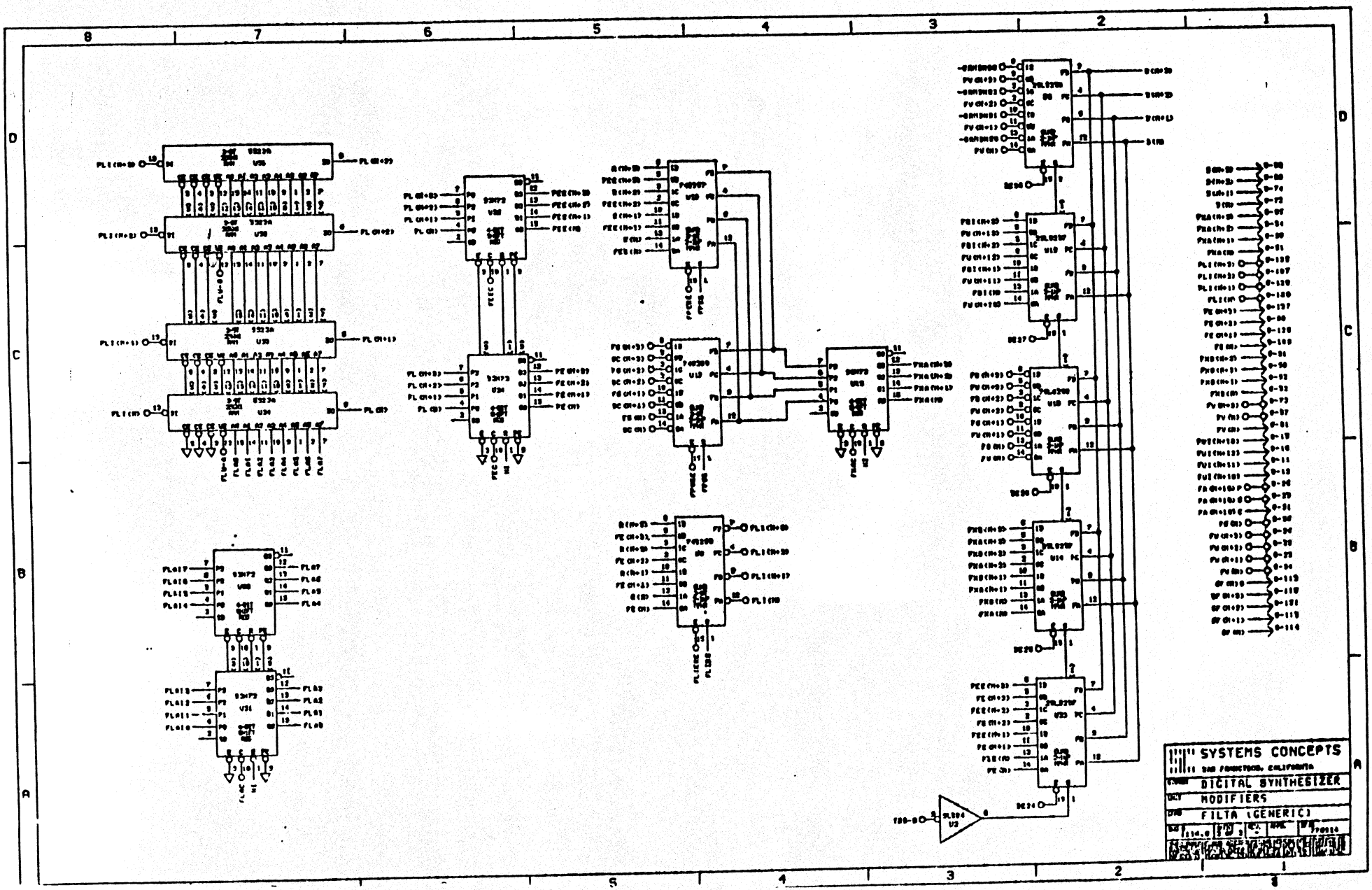
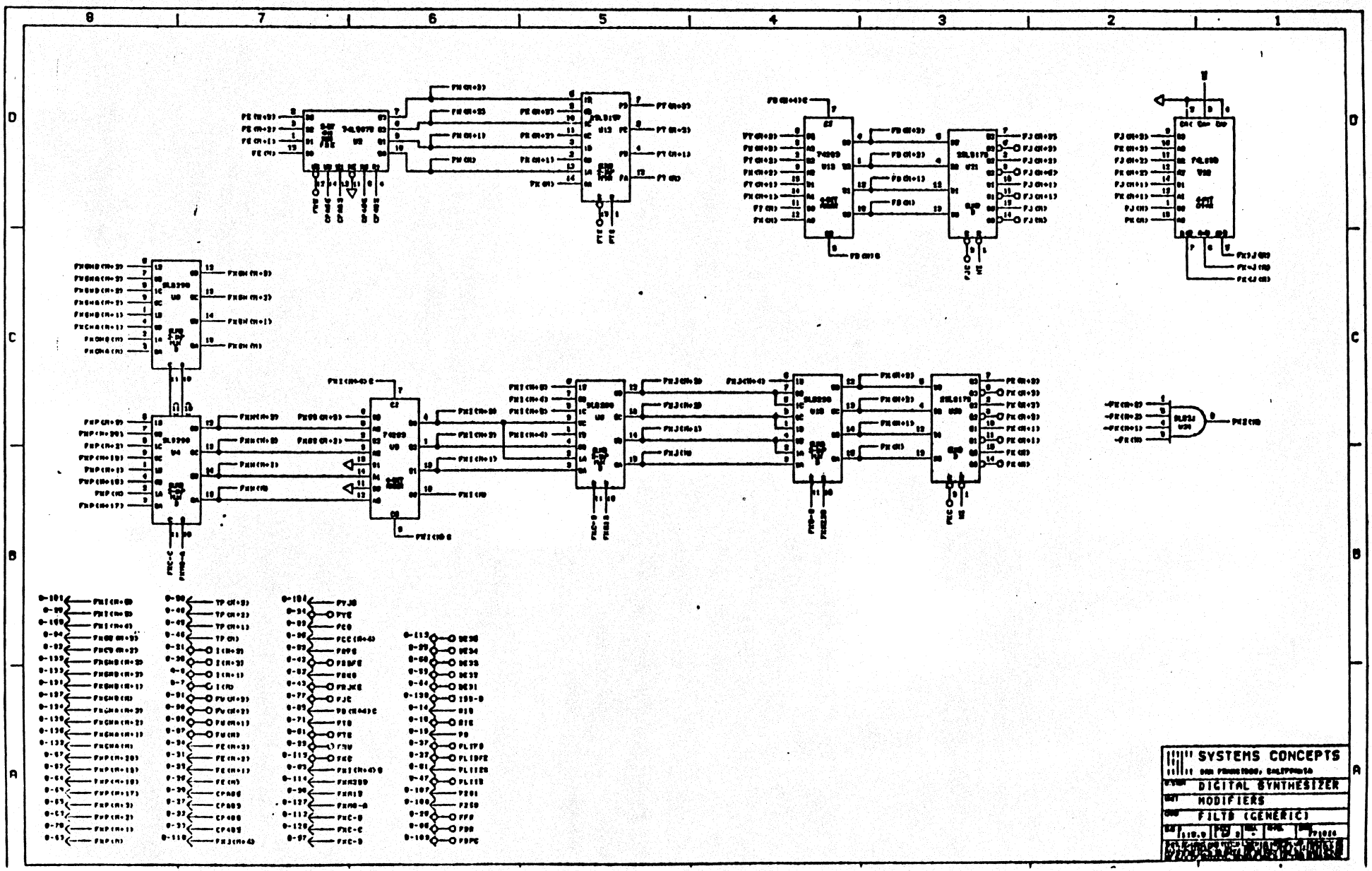


SFE; FILTB1
PTF=1



SFE; FILTB2

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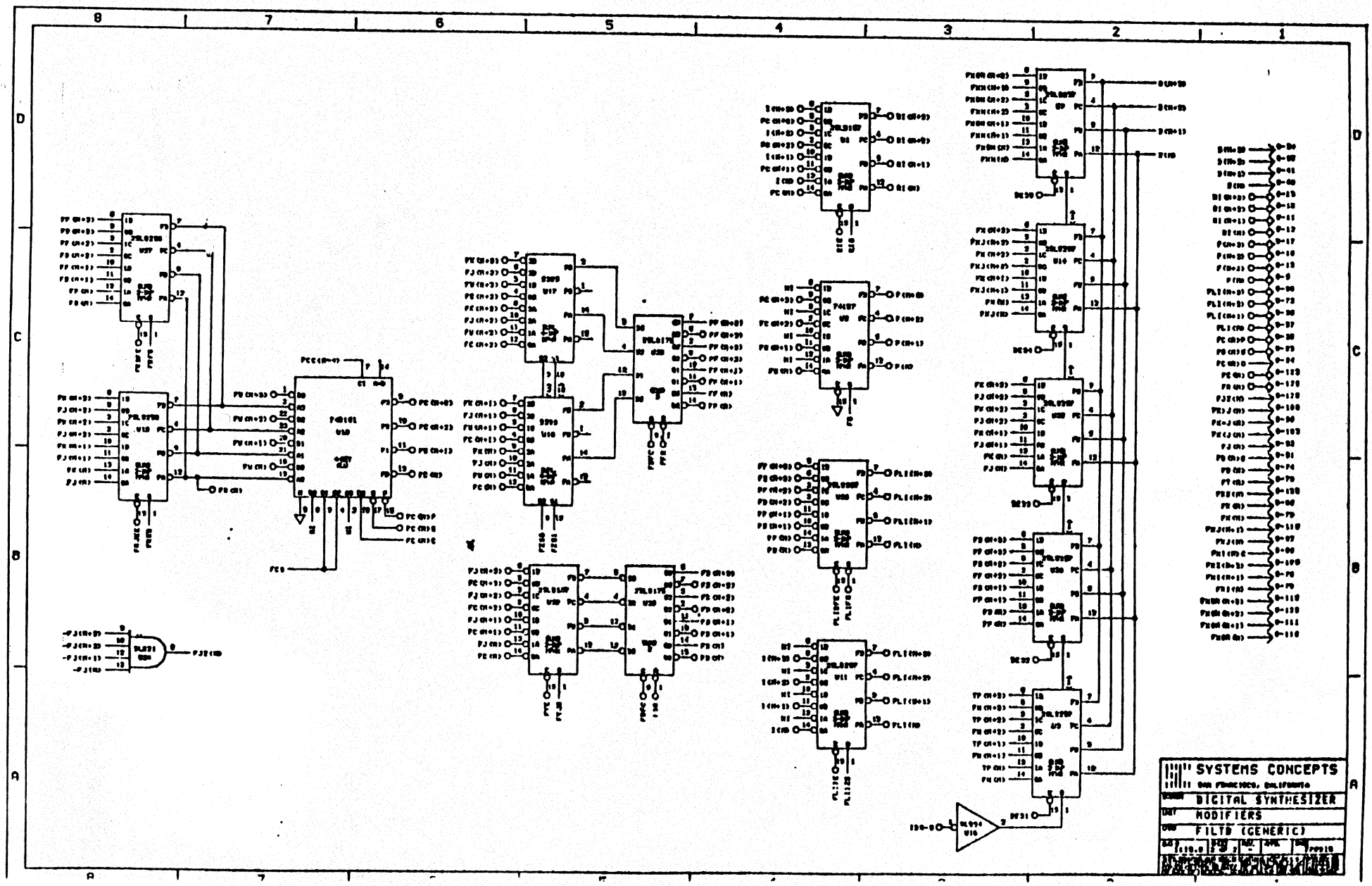
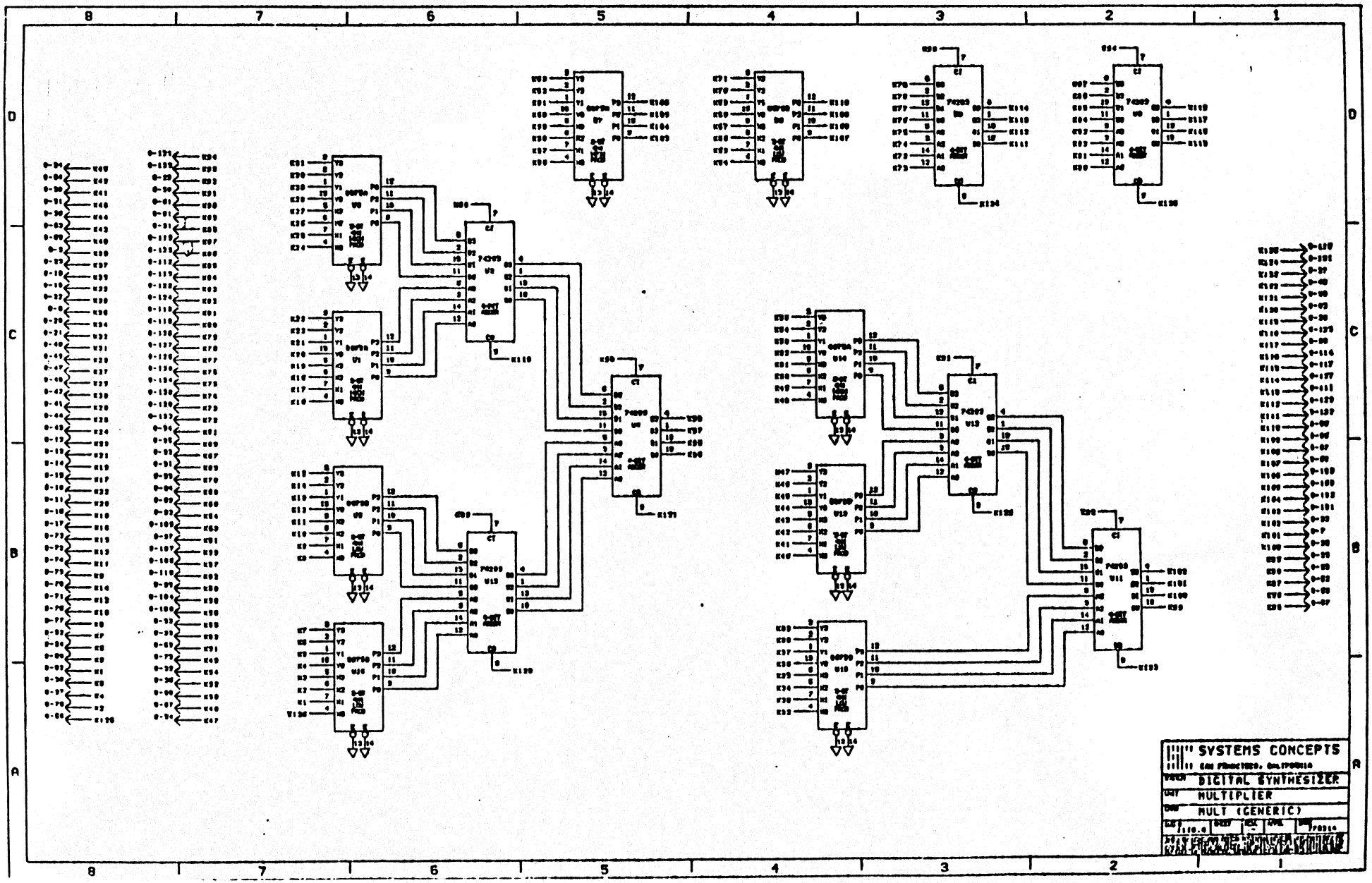


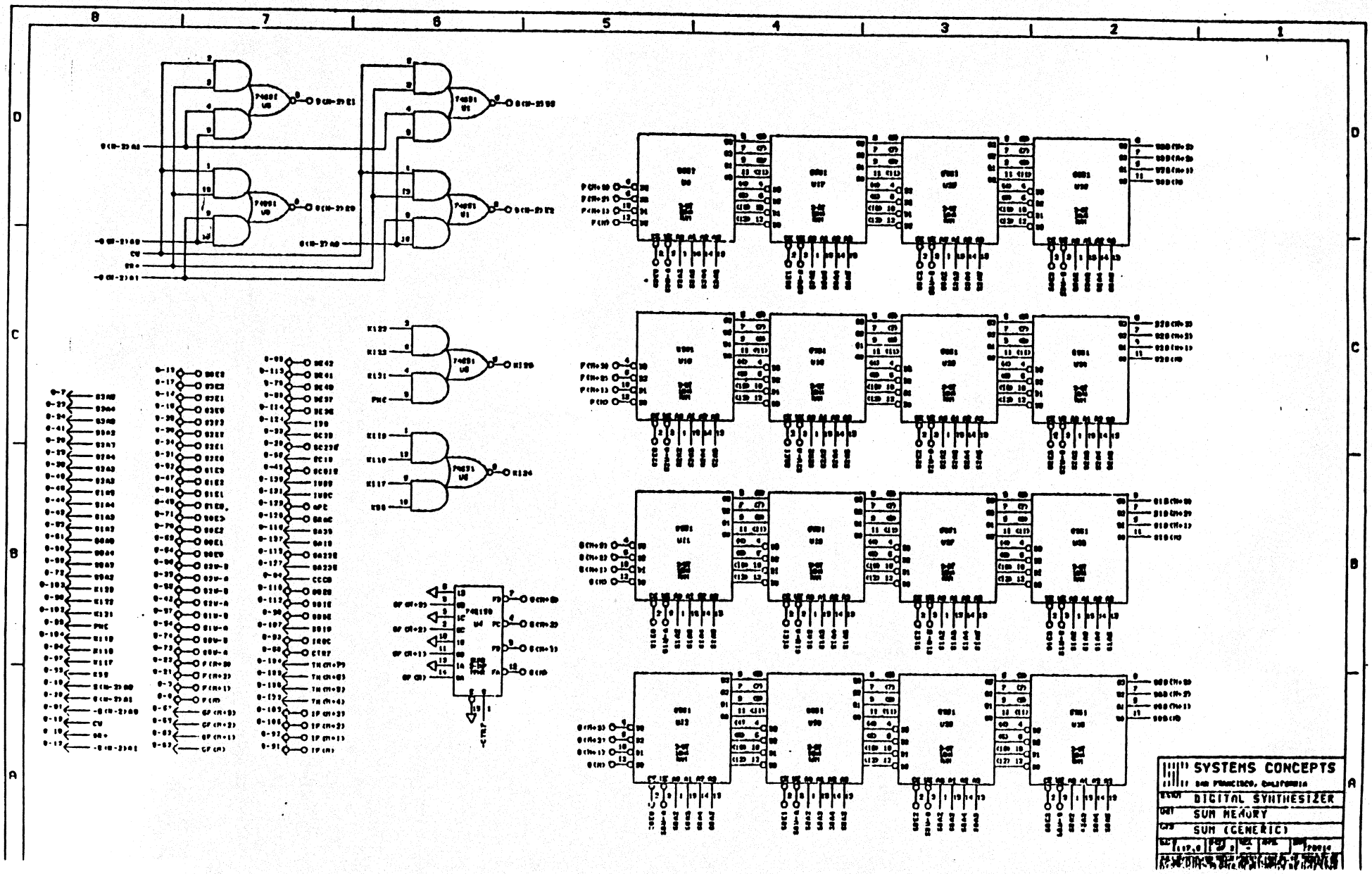
DM; MULT

PTF=1


SYSTEMS CONCEPTS
DIGITAL SYNTHESIZER
MULTIPLIER
MULT (GENERIC)

SFE;SUM 1

PTF=1



SFE;SUM2

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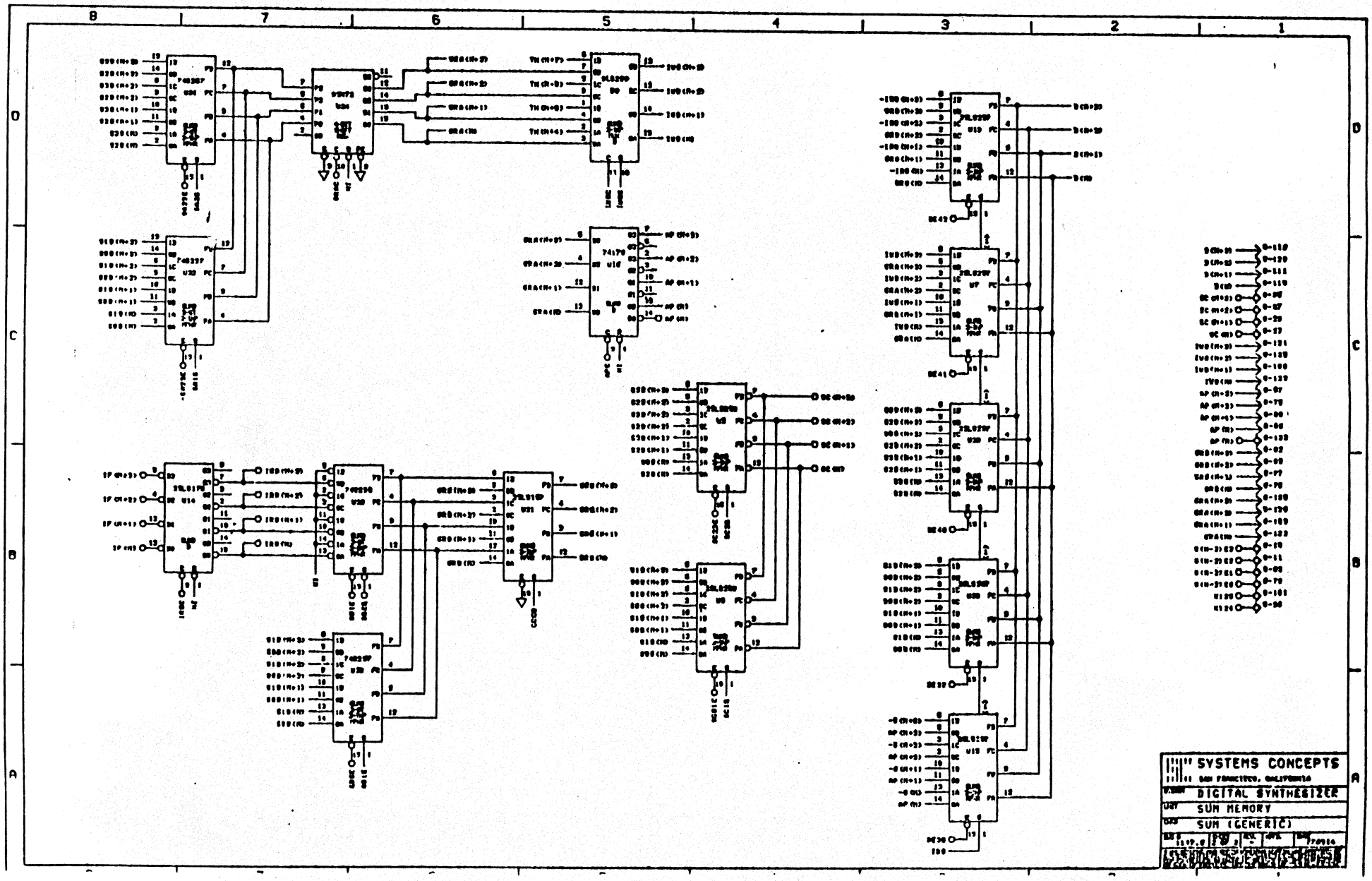
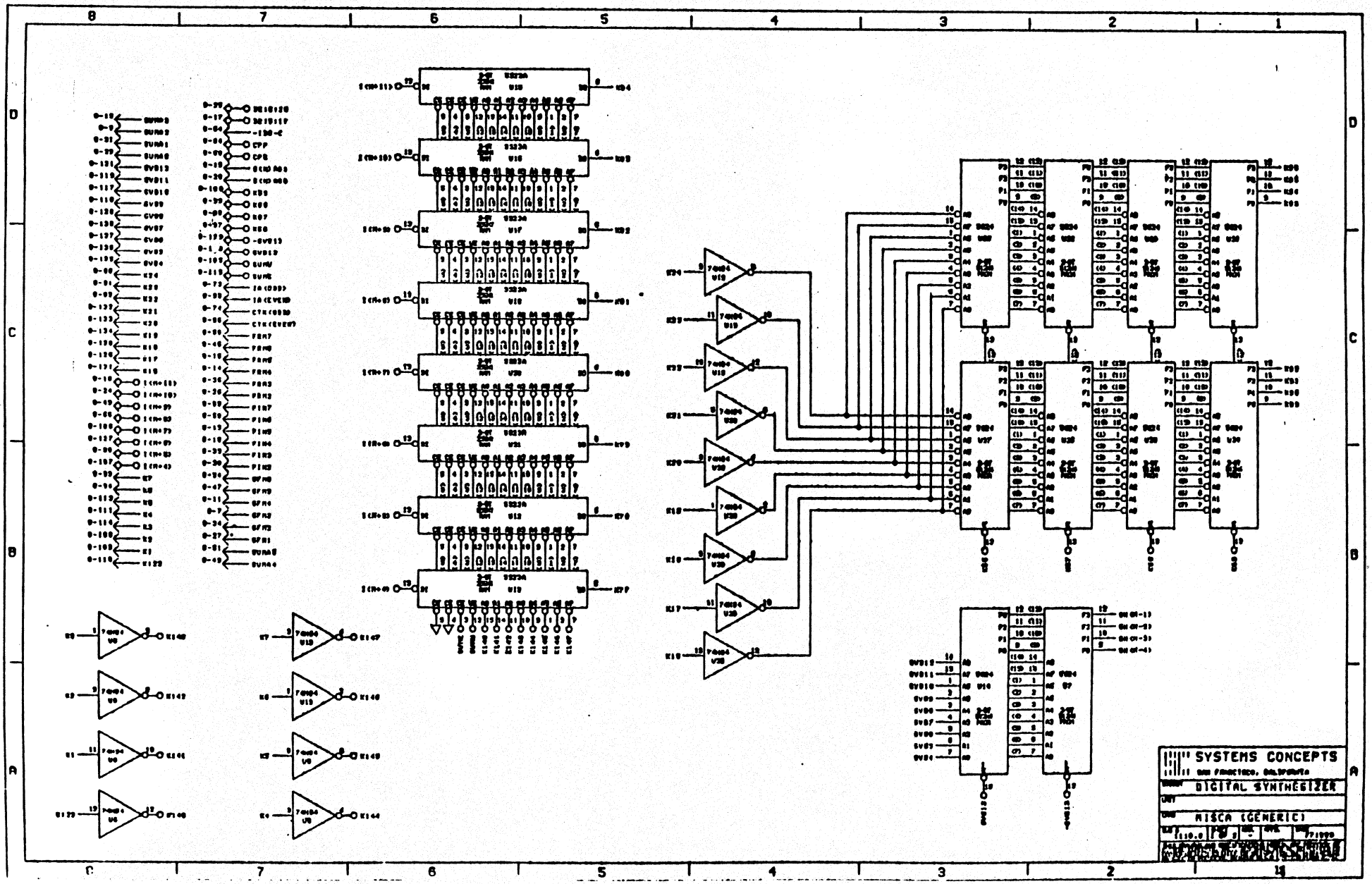


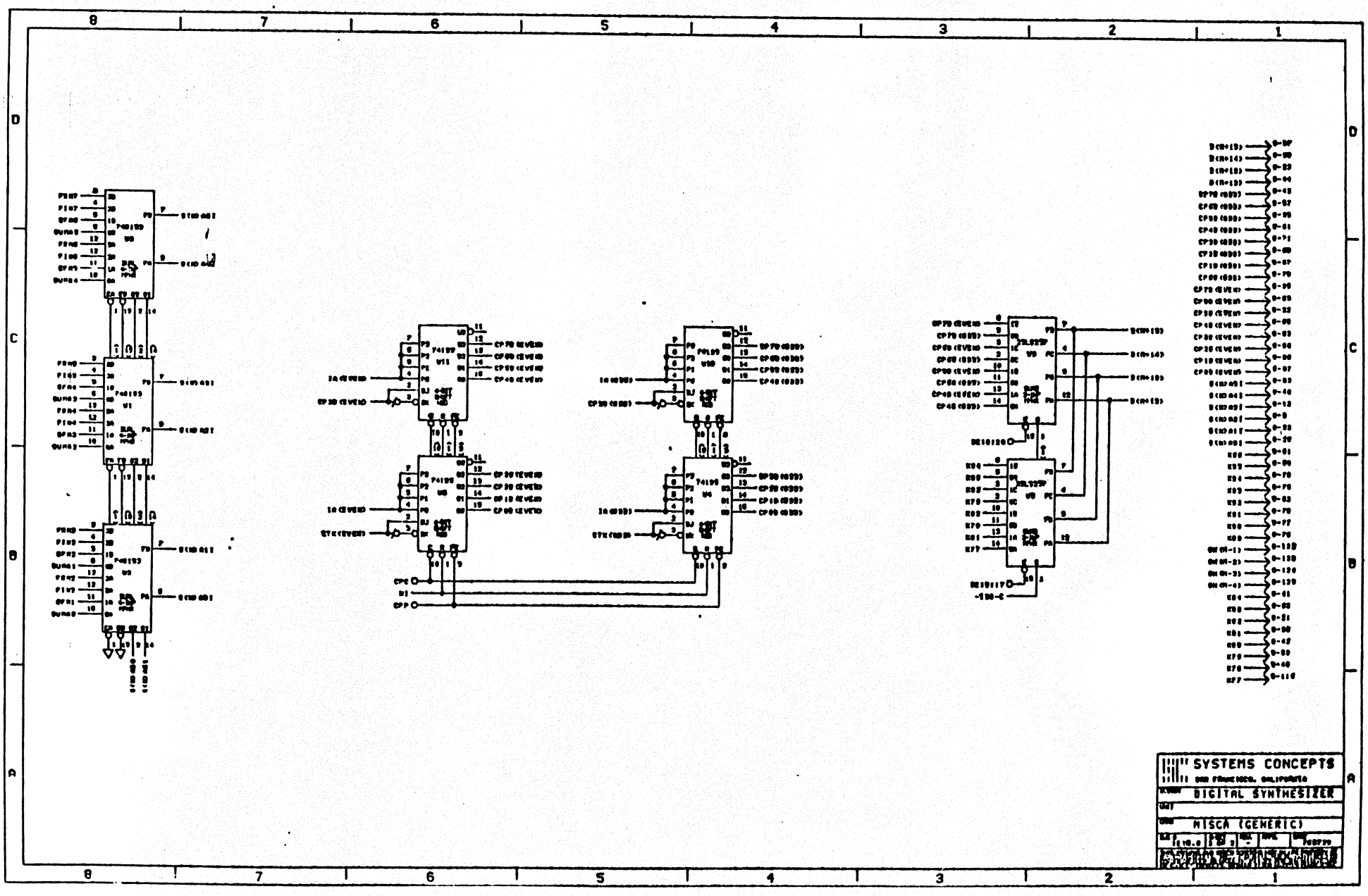
SRE; MISCA1

PTF=1



SRE; MISCA2

PTF=1



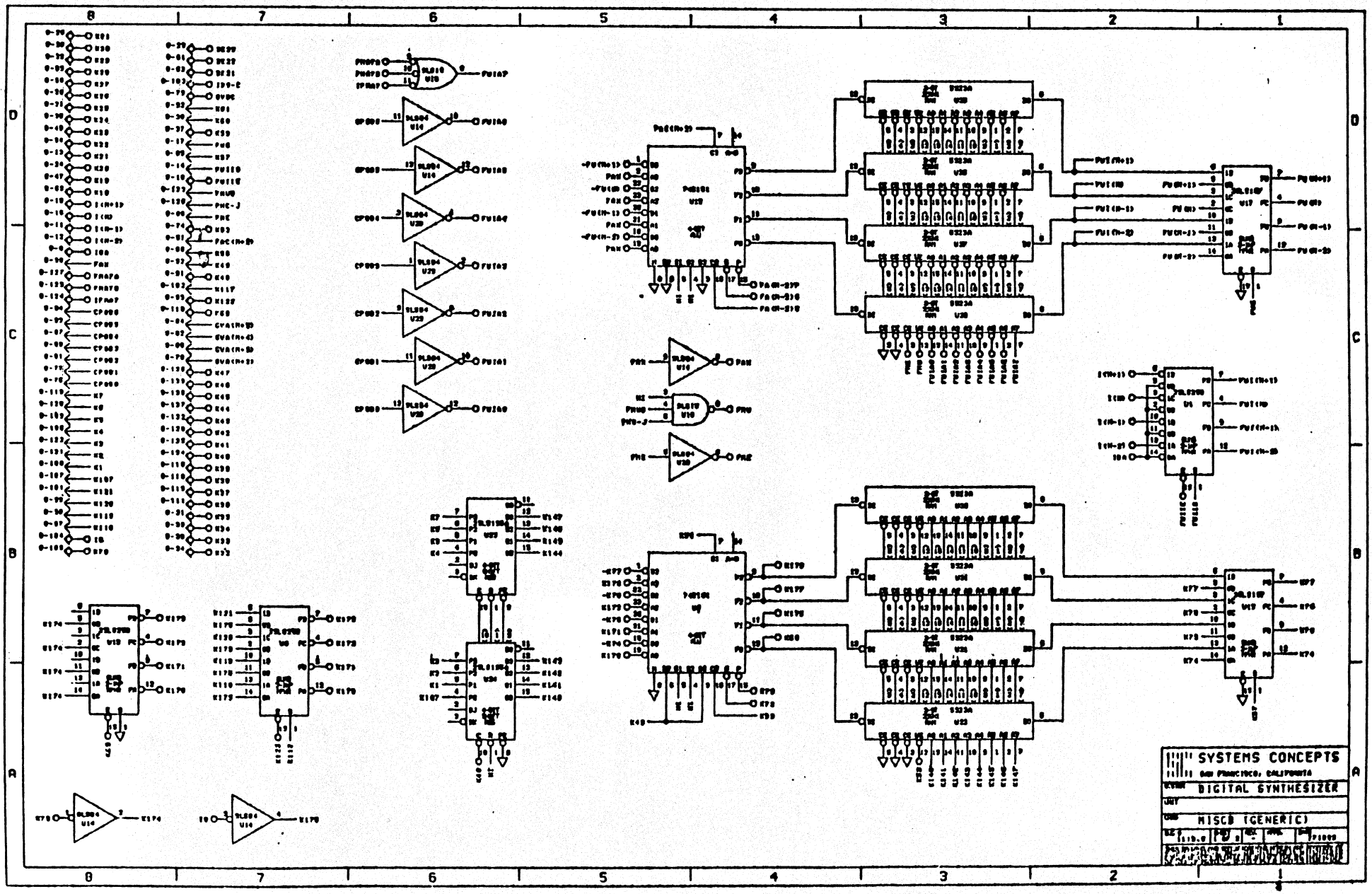
SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA

DIGITAL SYNTHESIZER

MISCA (GENERIC)

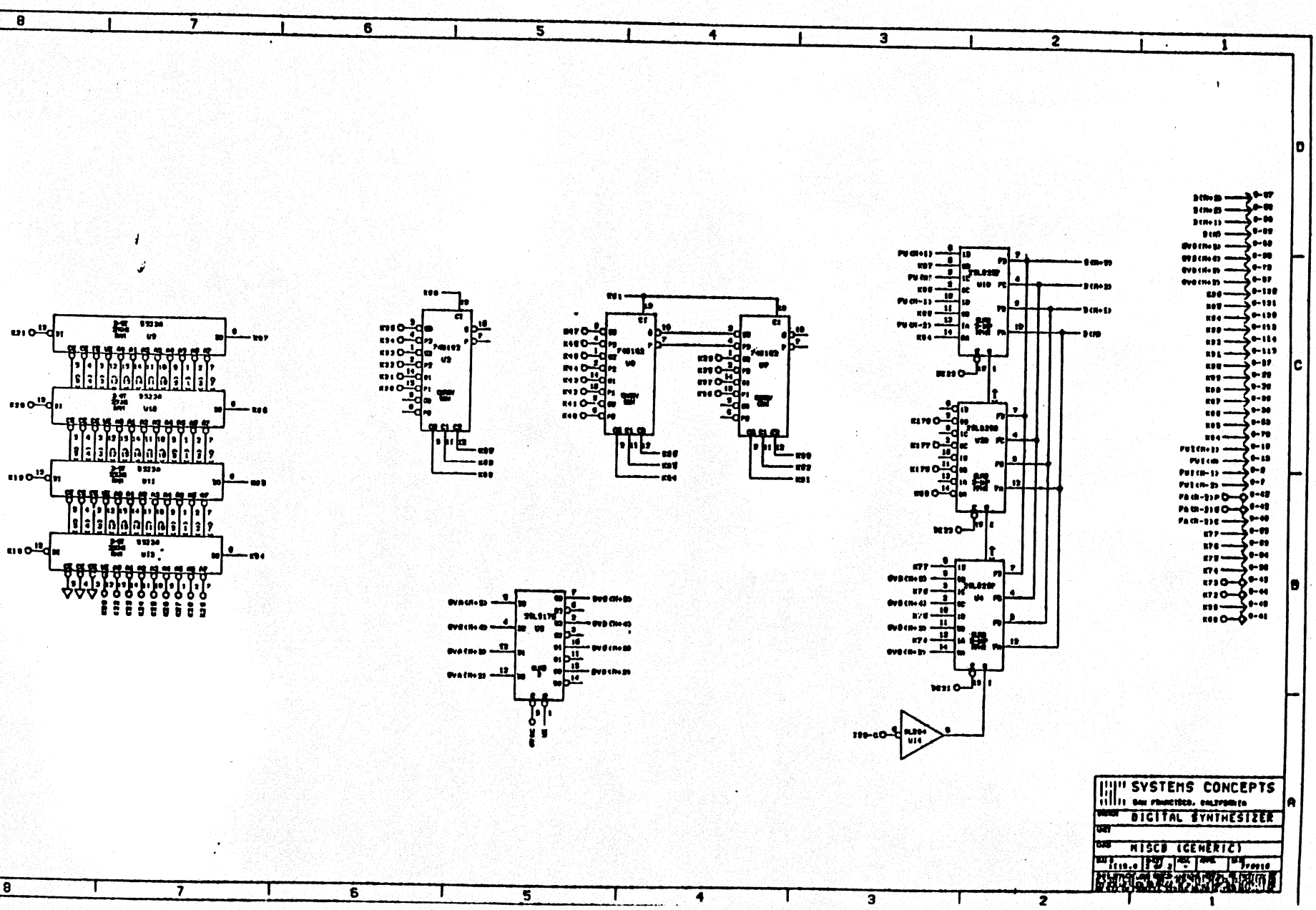
BG; MISCB1

PTF=1



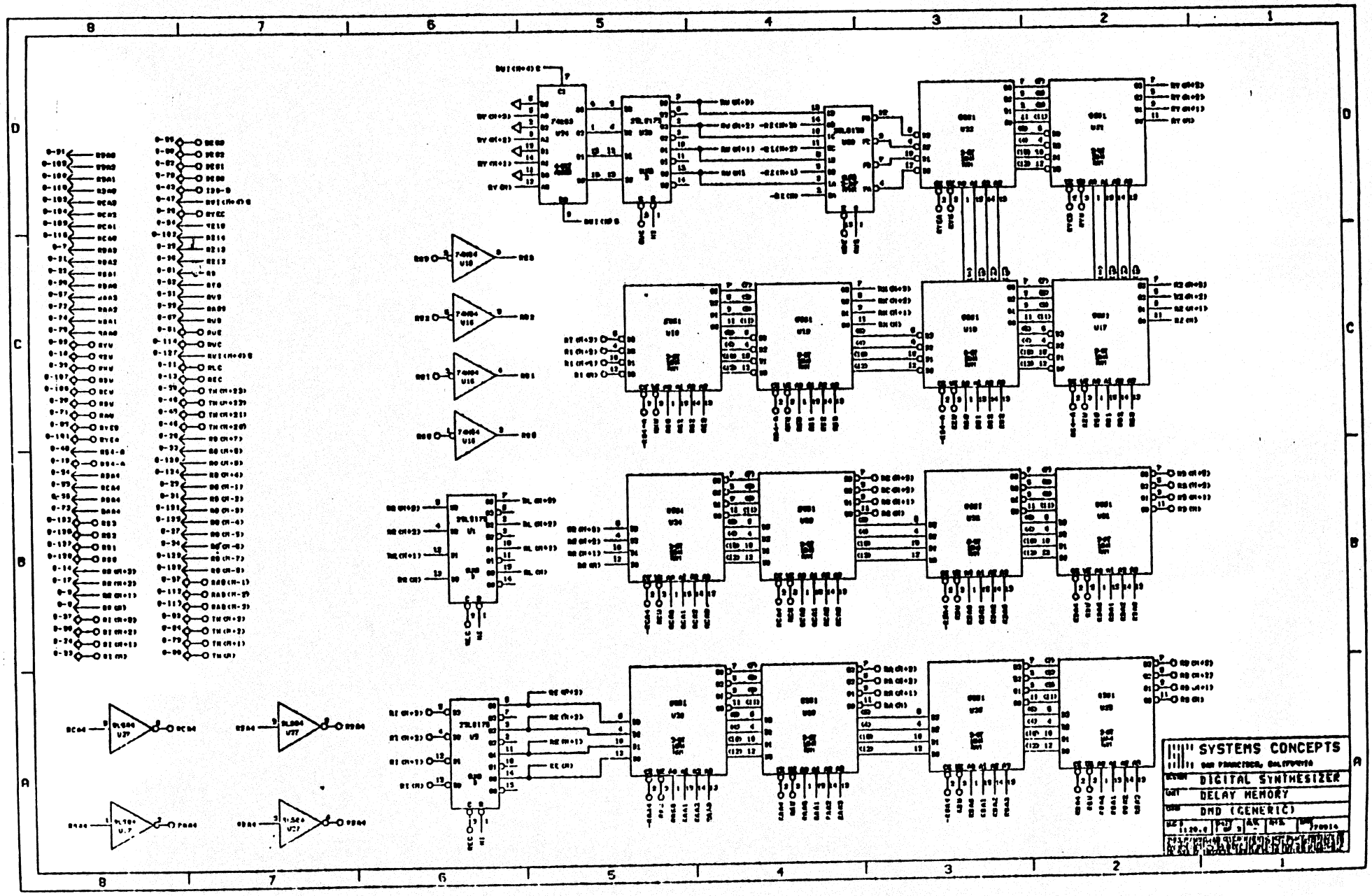
BG; MIS CB2

PTF=1



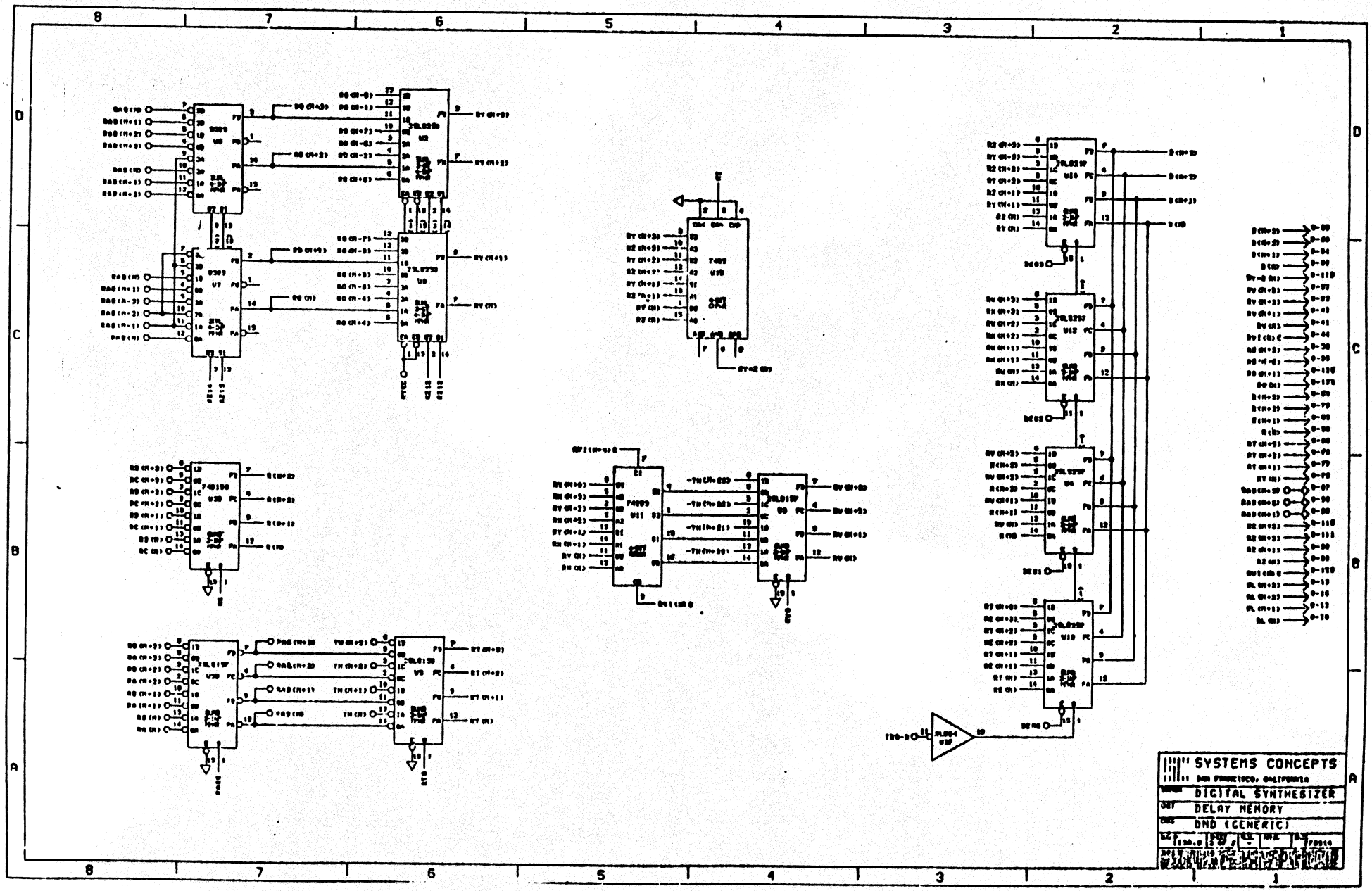
SWB: DMD1

PTF = 1



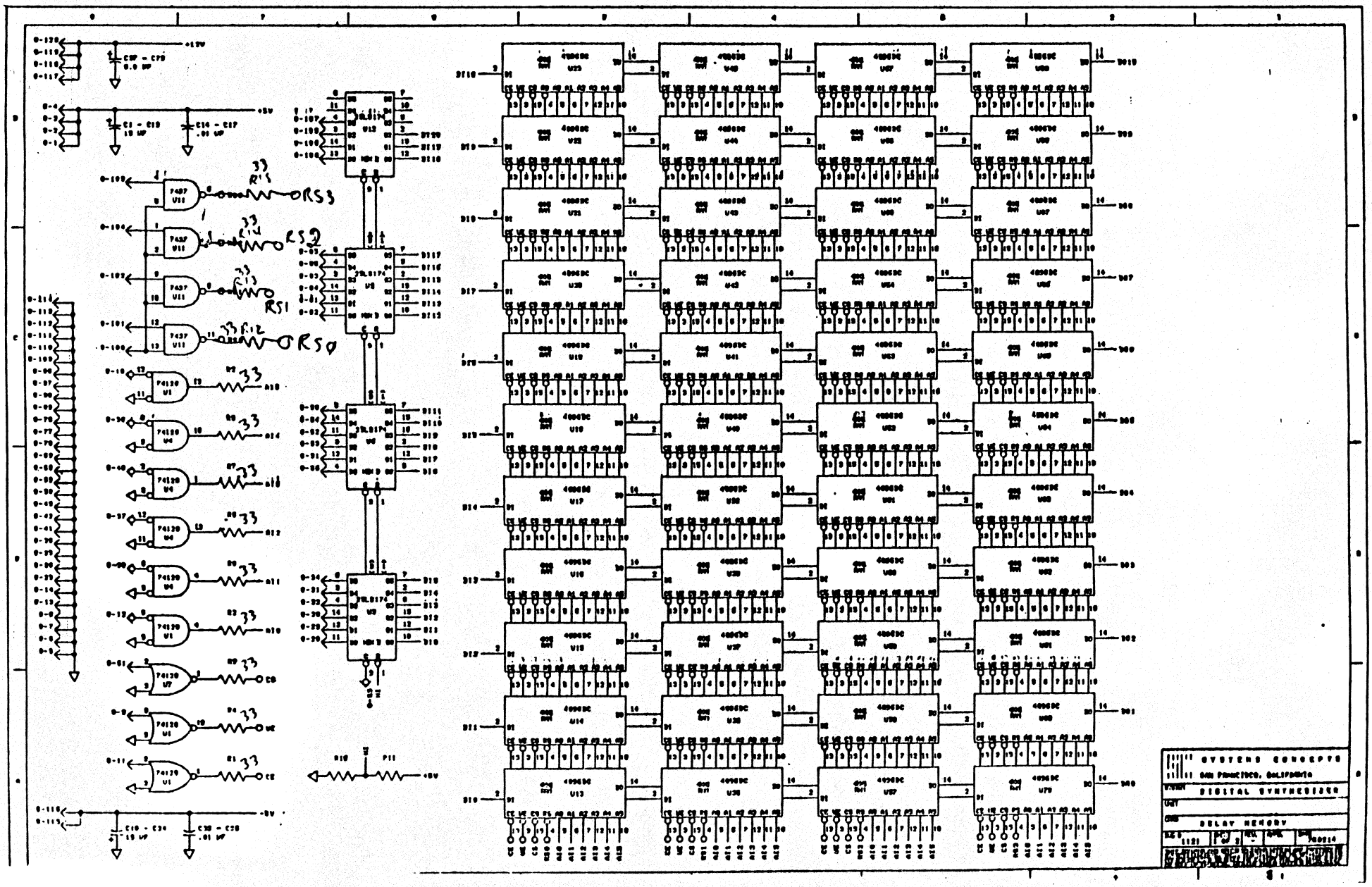
SWB; DMD2

PTF=1



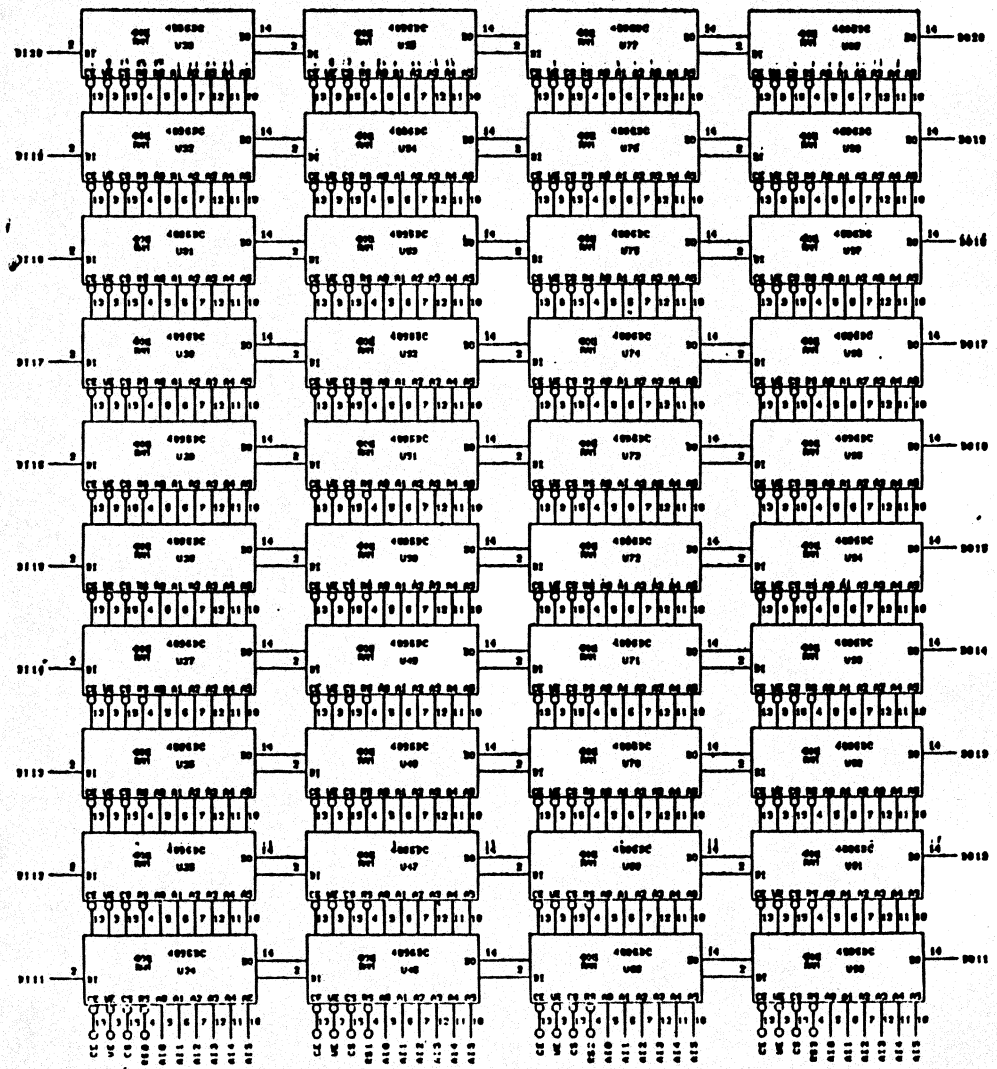
DXM; DEMRM 1

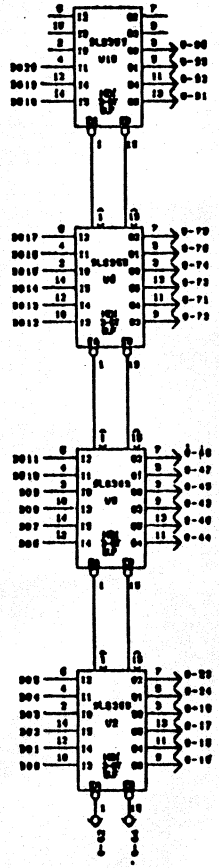
BIT 21 = Ø



DXM; DEMEM2

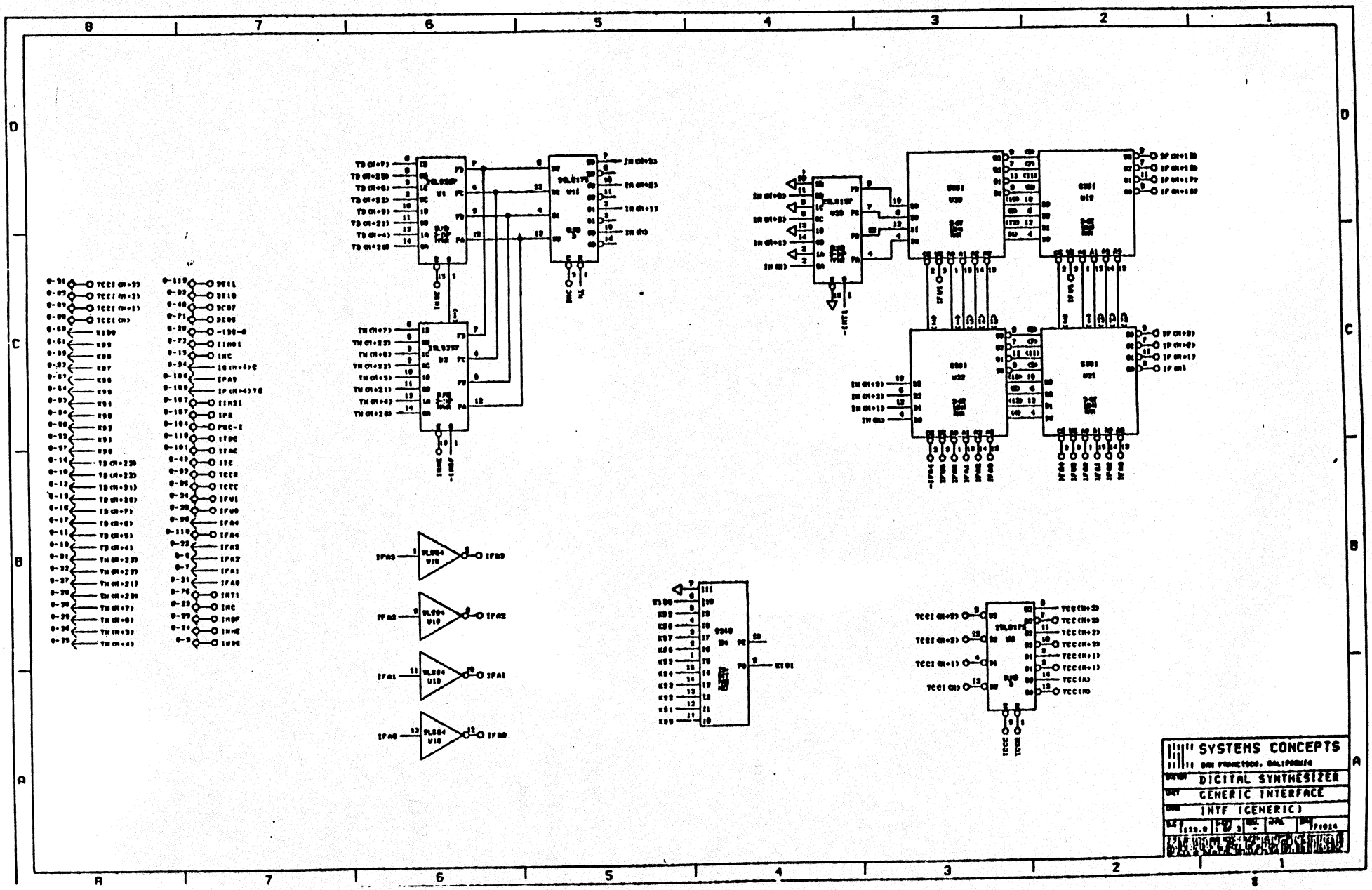
BIT 21 = Ø





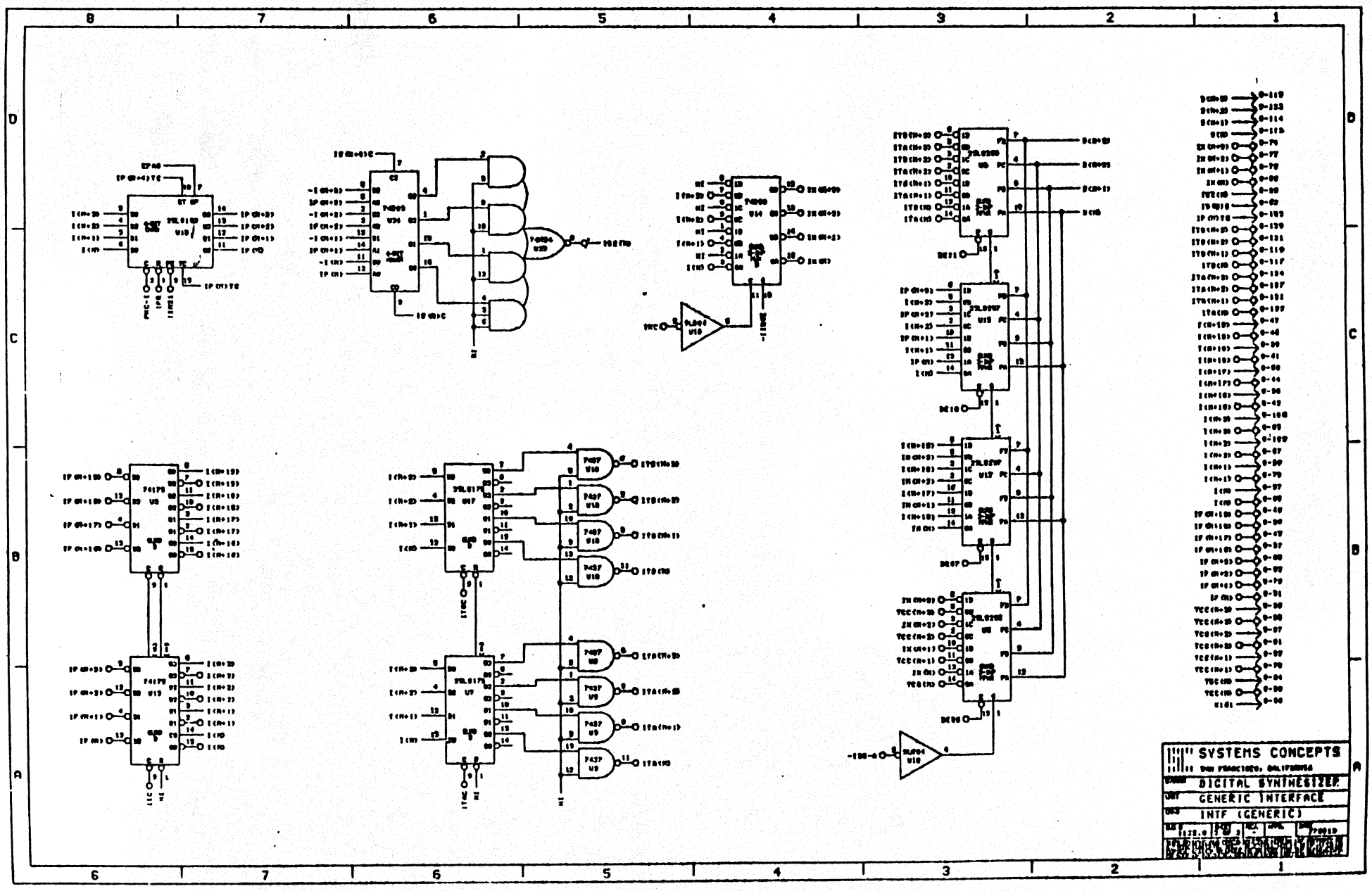
SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
SYSTEM DIGITAL SYNTHESIZER
UNIT
DWG DELAY MEMORY

DM; INTF1
PTF=1



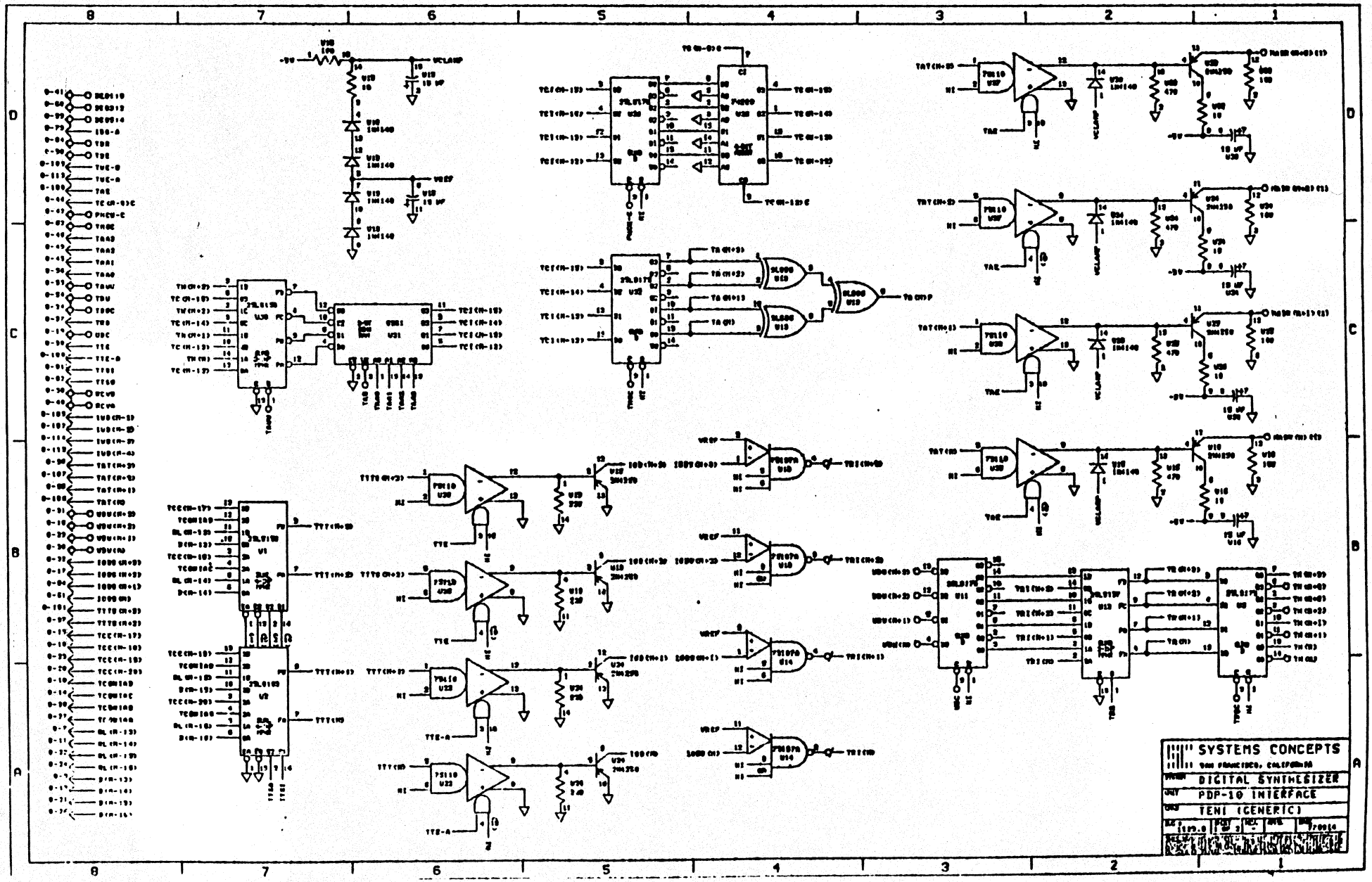
DM; INTF2

PTF=1



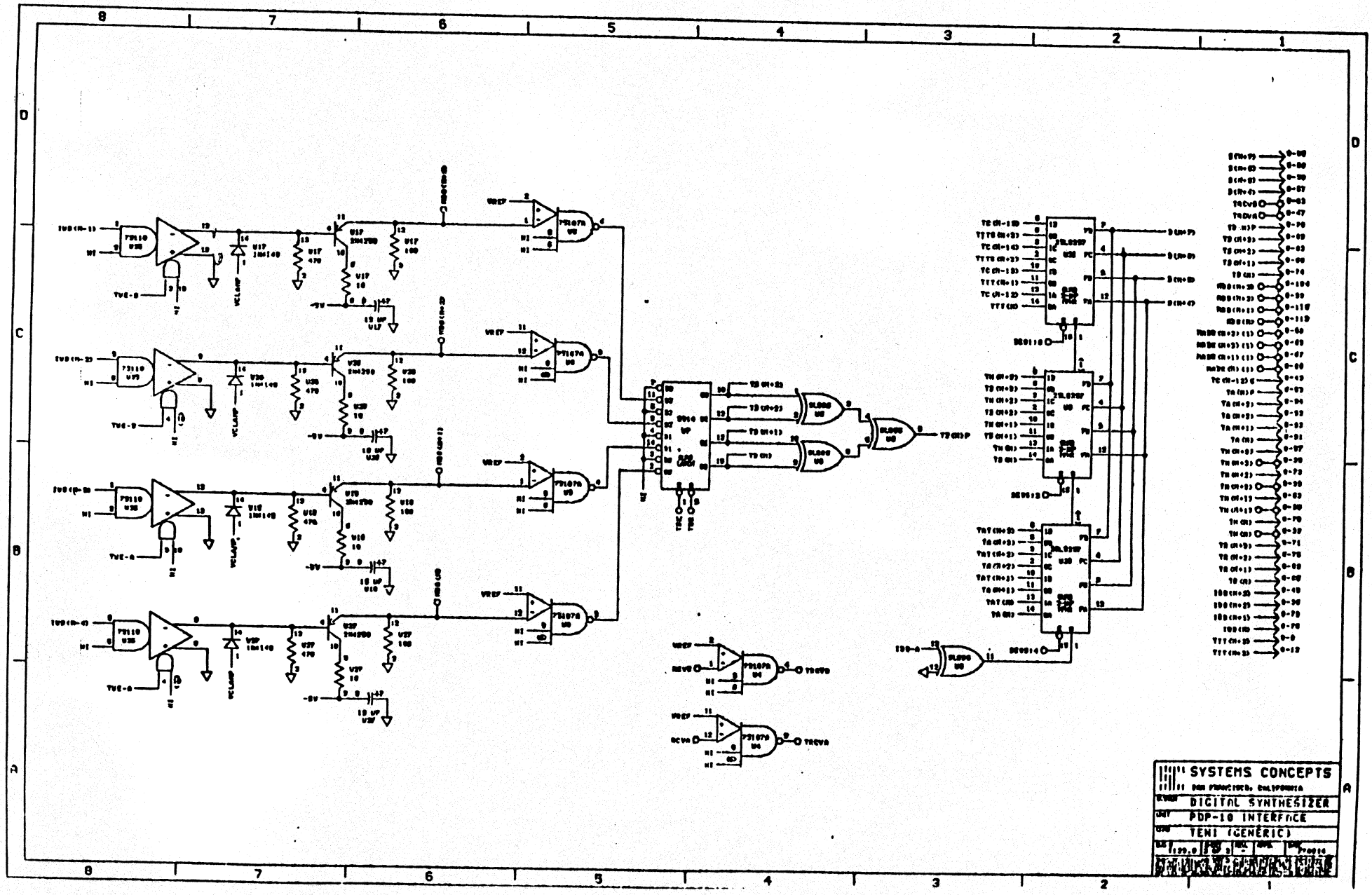
SWB, TENI

PTE=1

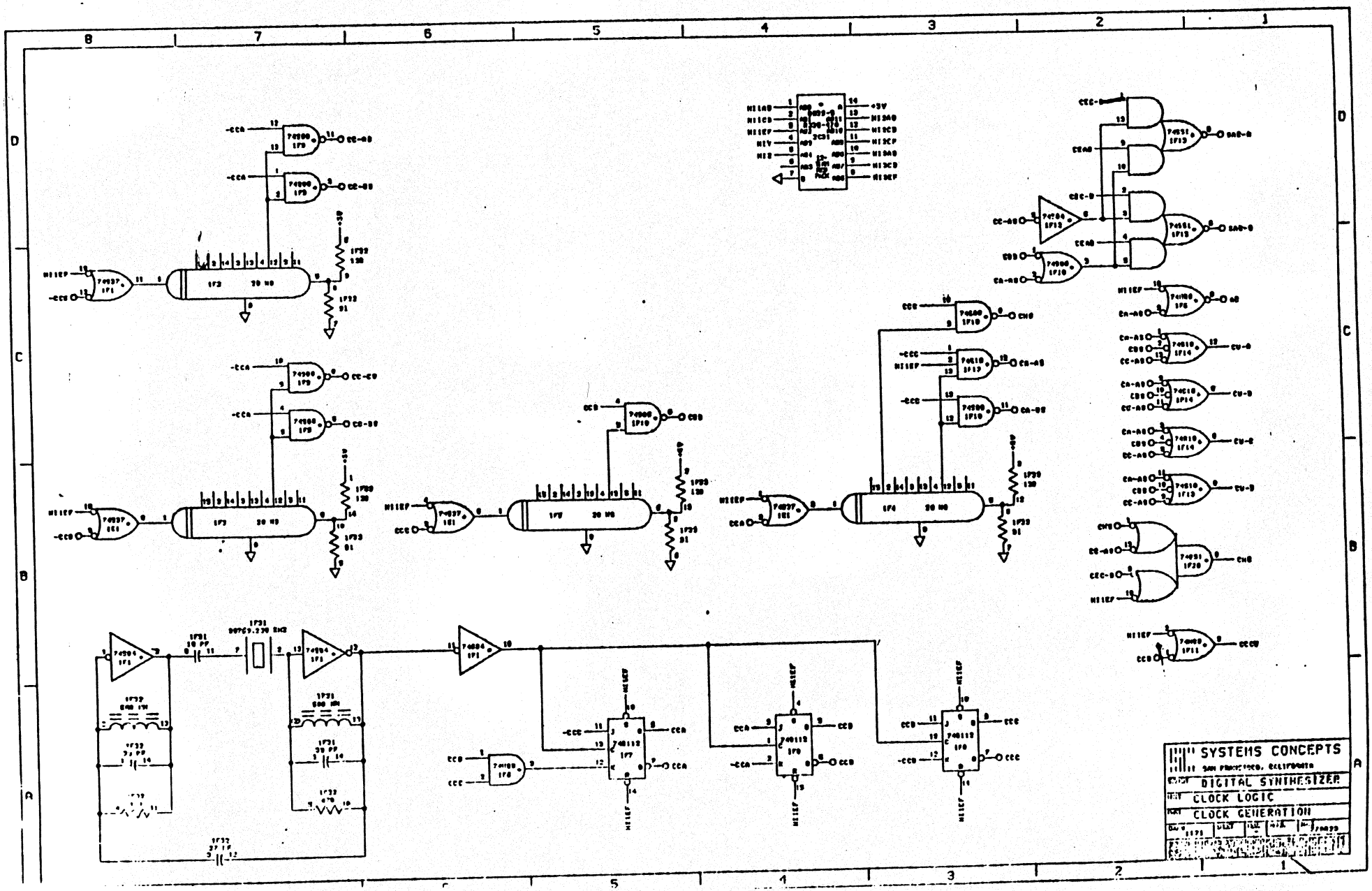


SWB, TENIL

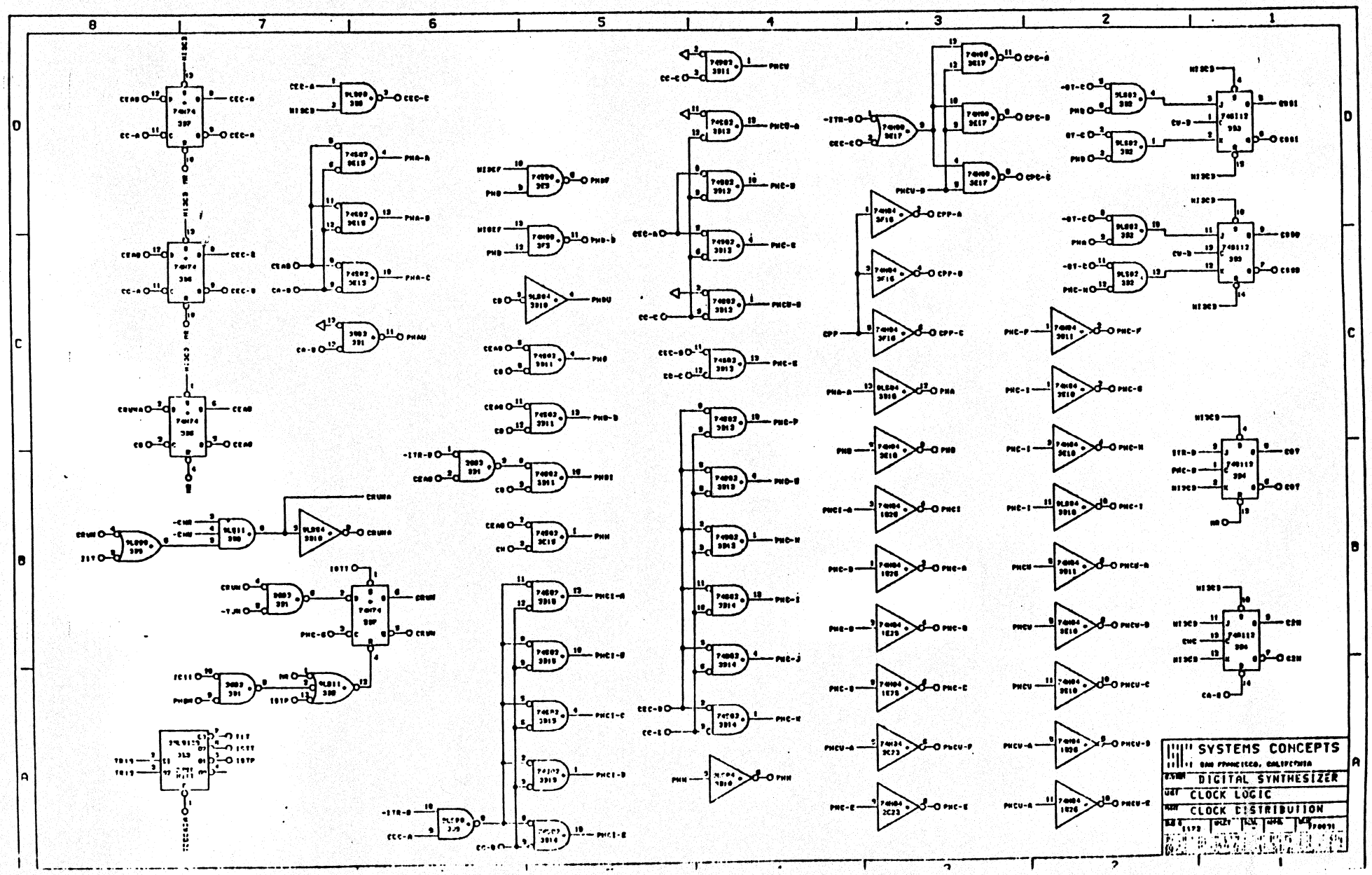
TTF=1



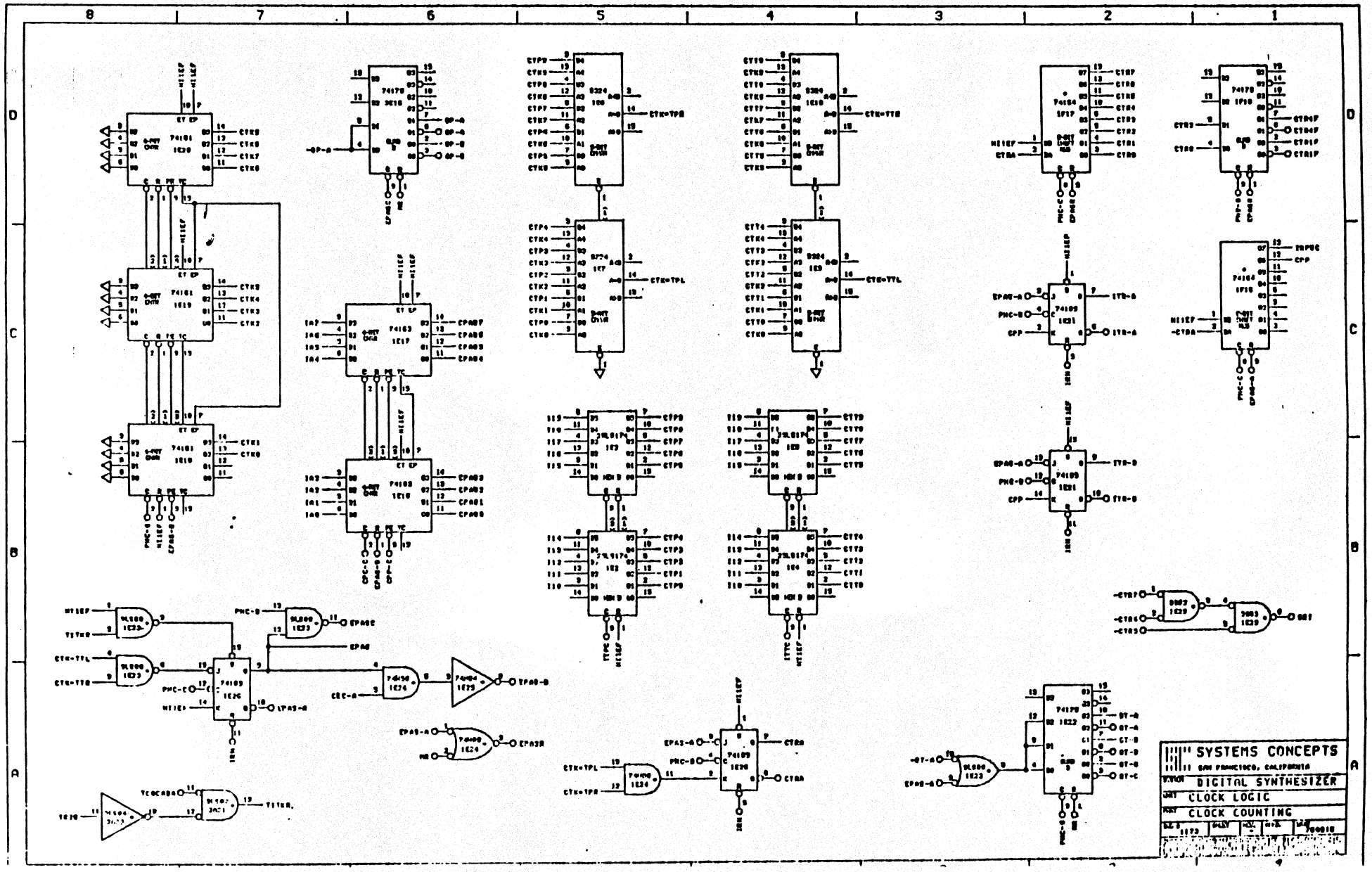
DXM; CLKGN


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
CLOCK LOGIC
CLOCK GENERATION

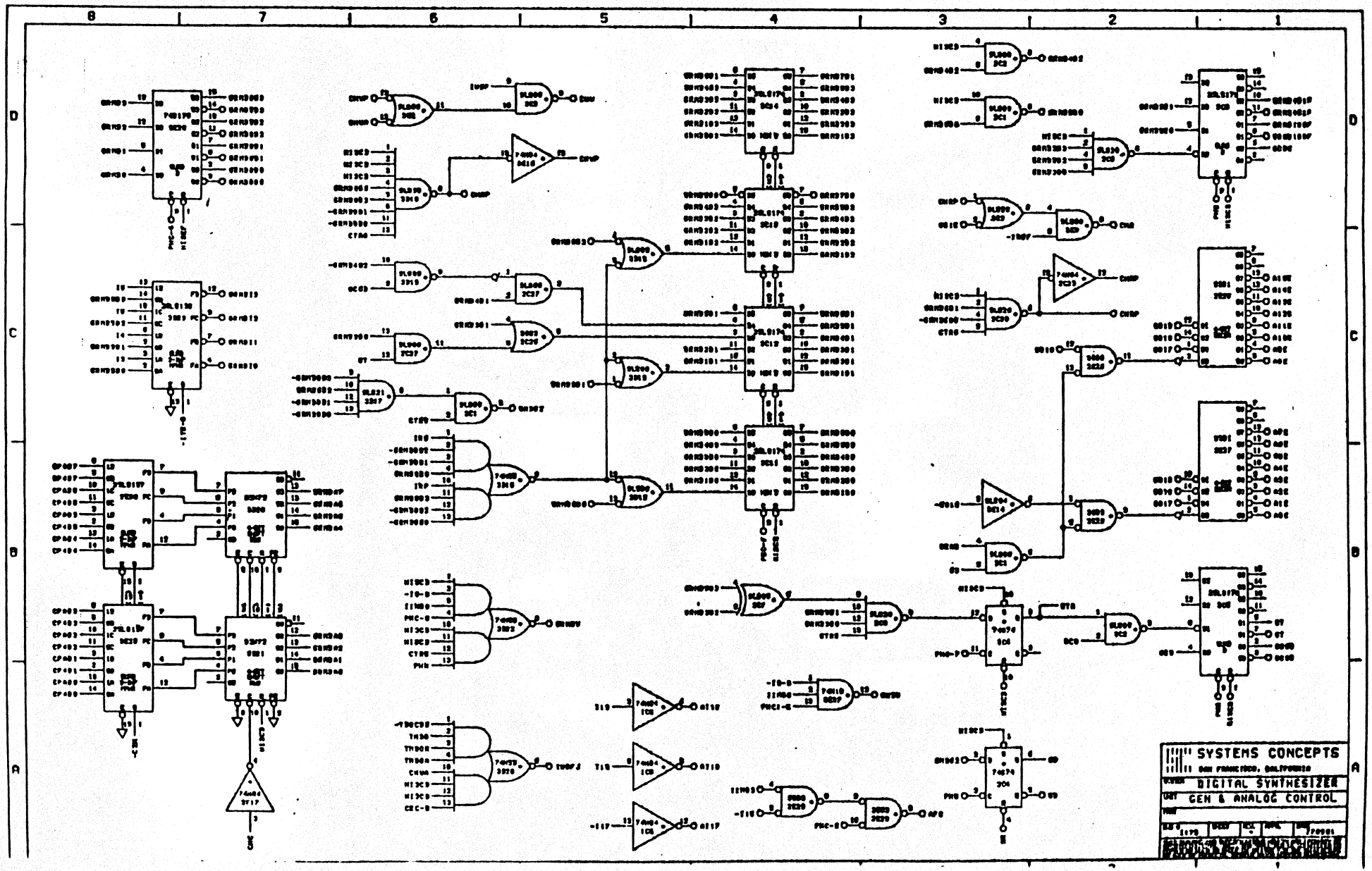
SRE; CLK(D)ST


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
CLOCK LOGIC
CLOCK DISTRIBUTION

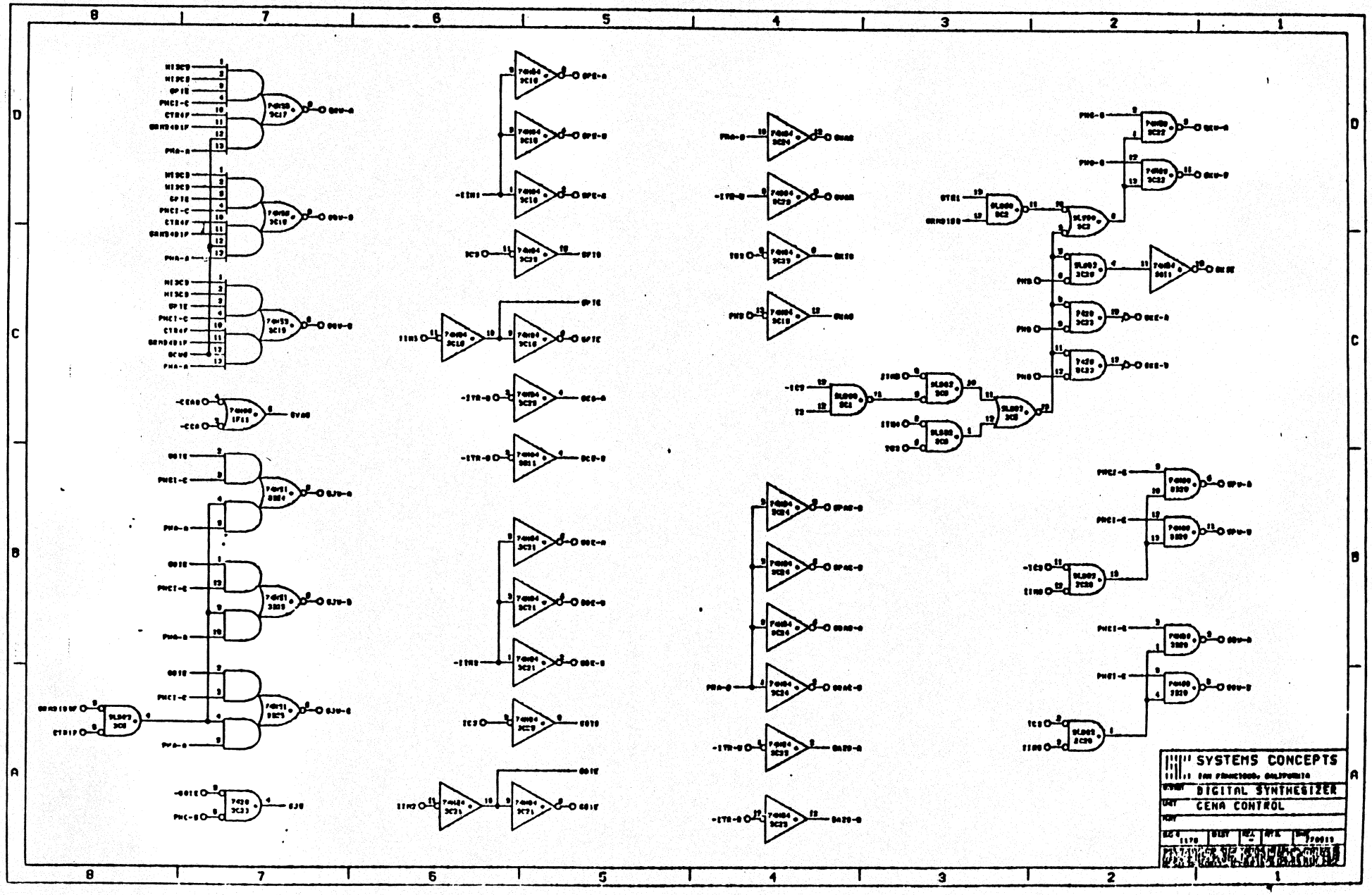
DXM; CLKCNT


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
CLOCK LOGIC
CLOCK COUNTING

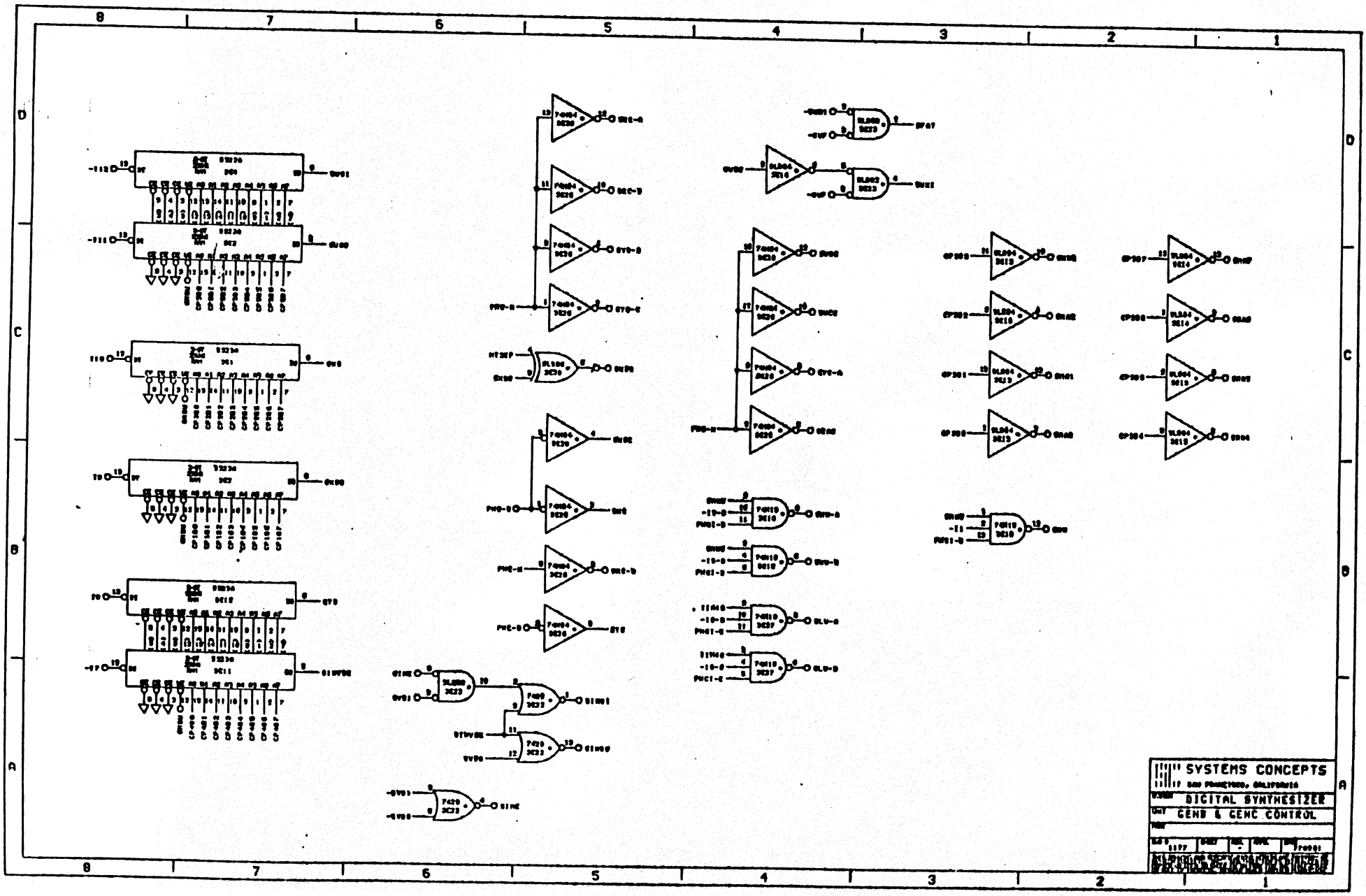
DXM, GENANC


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
GEN & ANALOG CONTROL

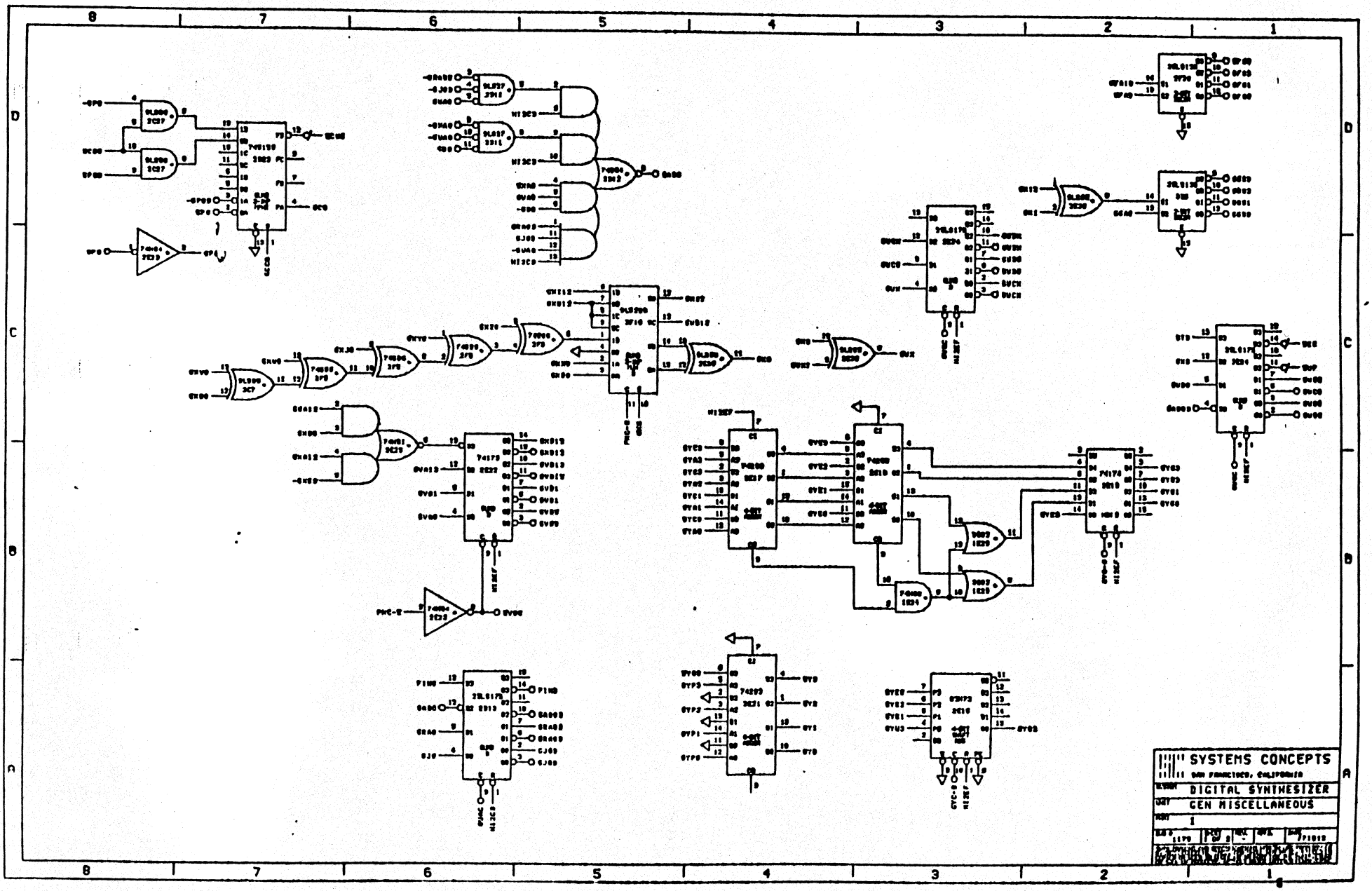
BG; GENAC



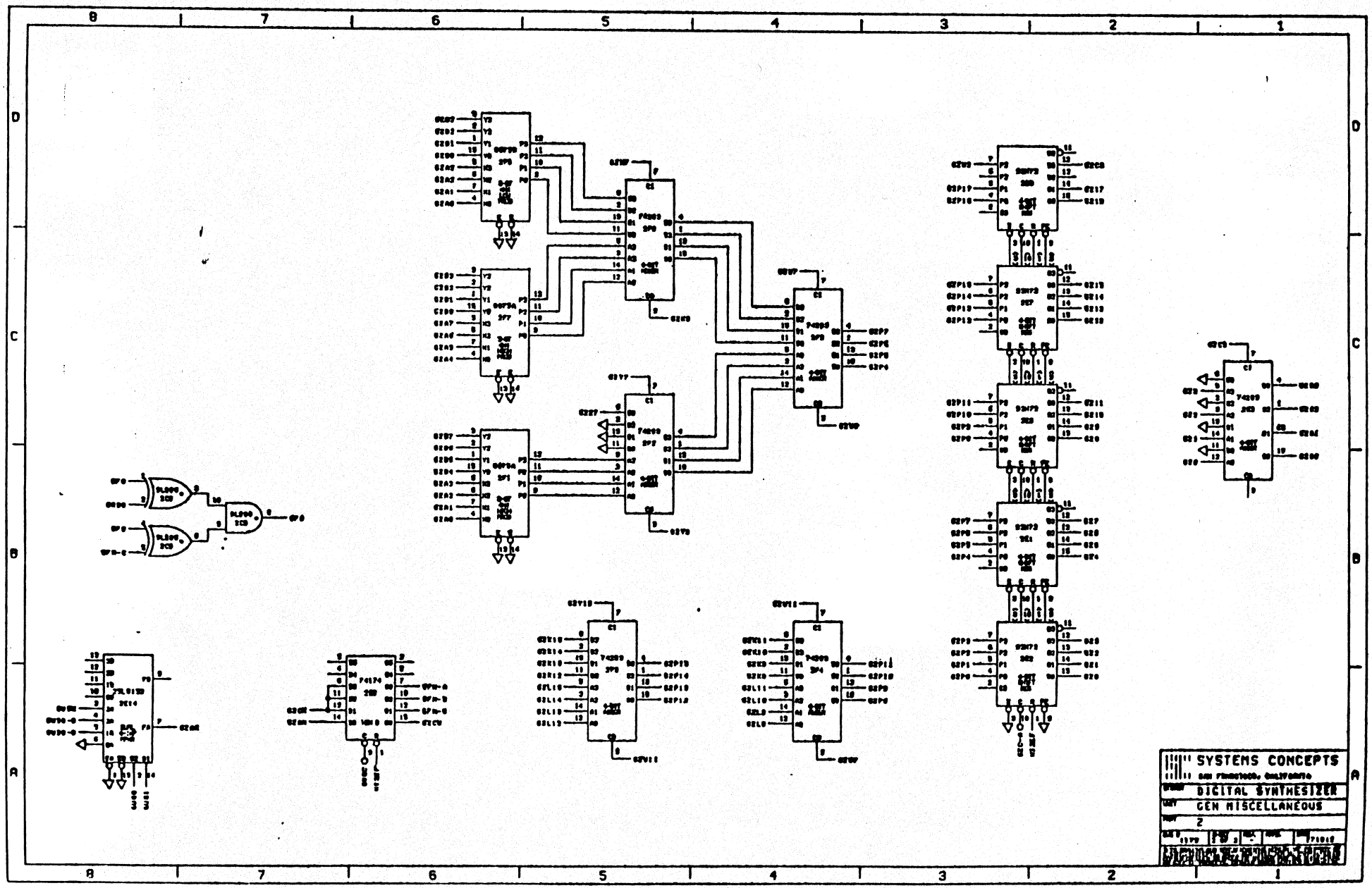
SRE ; GENBCC



SWB; GENM1


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
GEN MISCELLANEOUS

SWB; GENM2


SYSTEMS CONCEPTS
DIGITAL SYNTHESIZER
GEN MISCELLANEOUS
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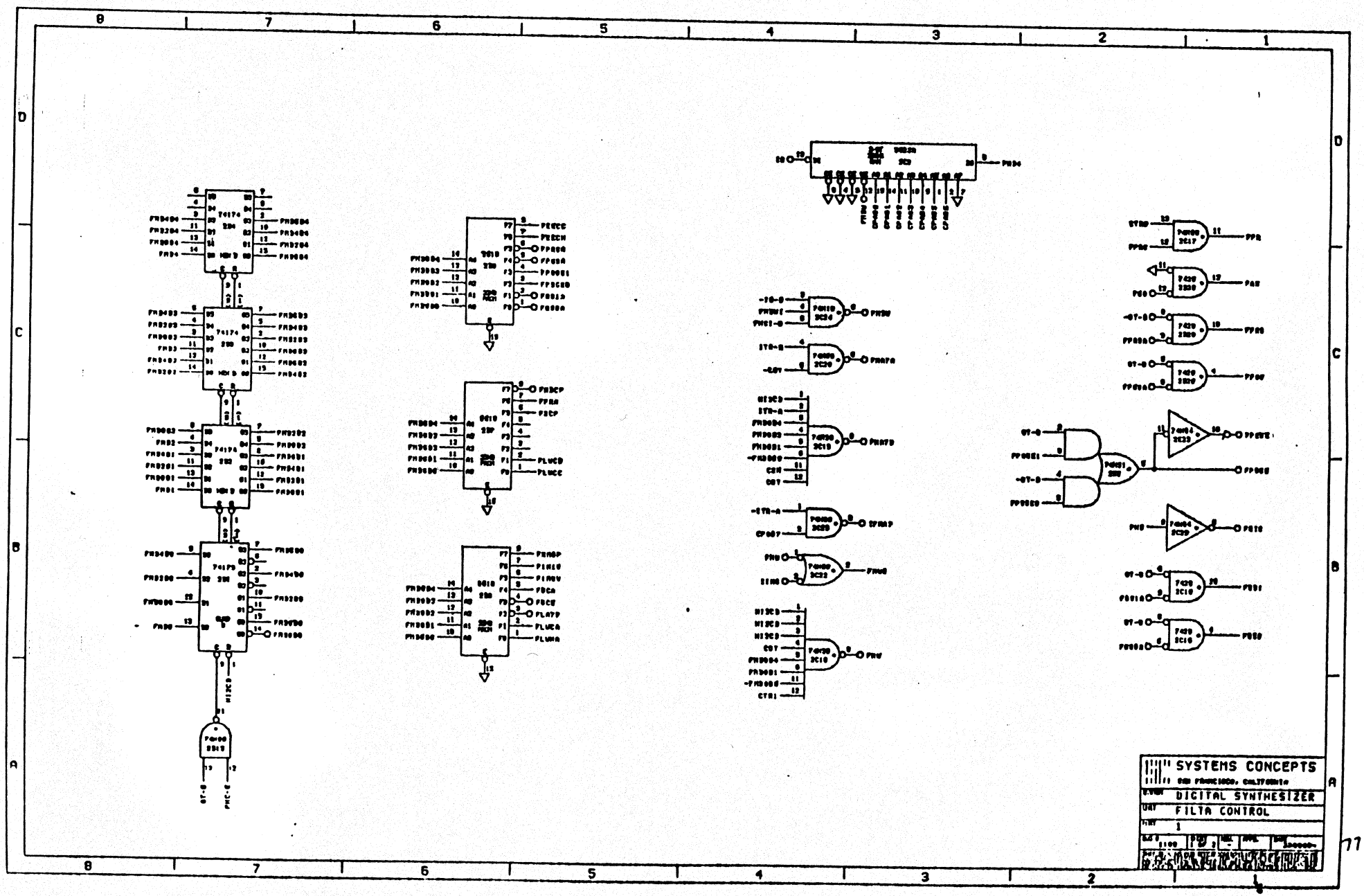
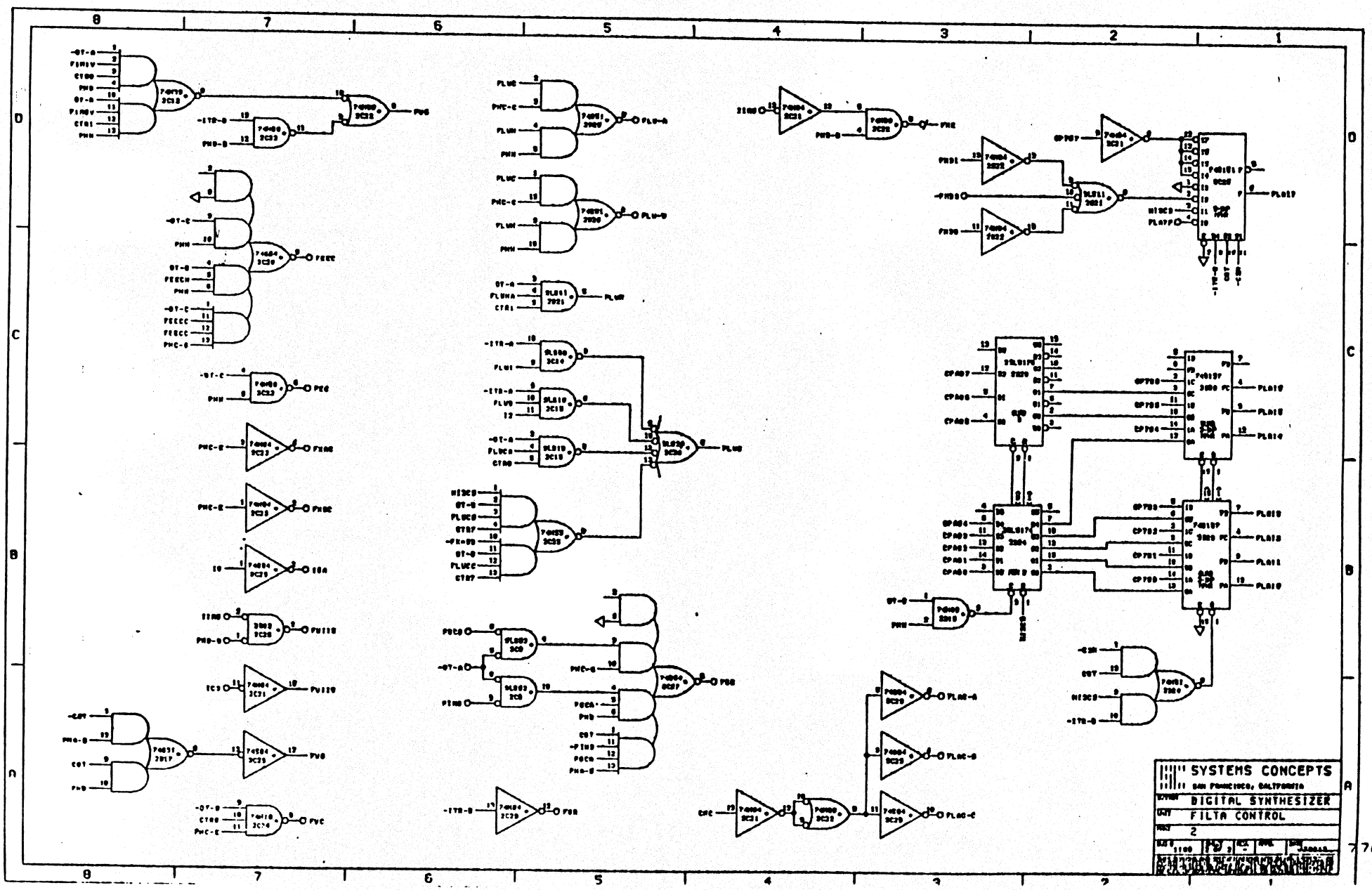
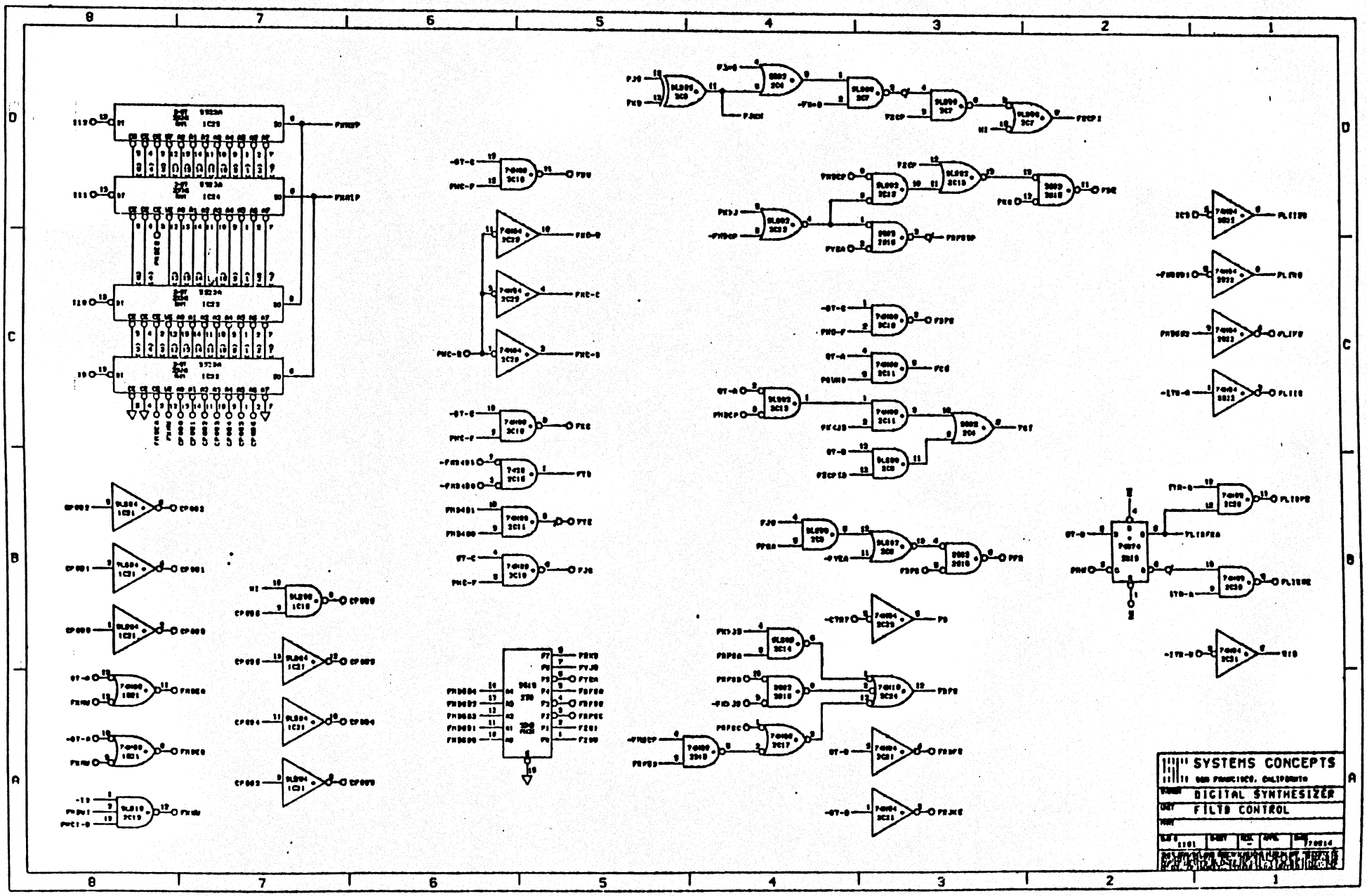
DXM; FILTAC1



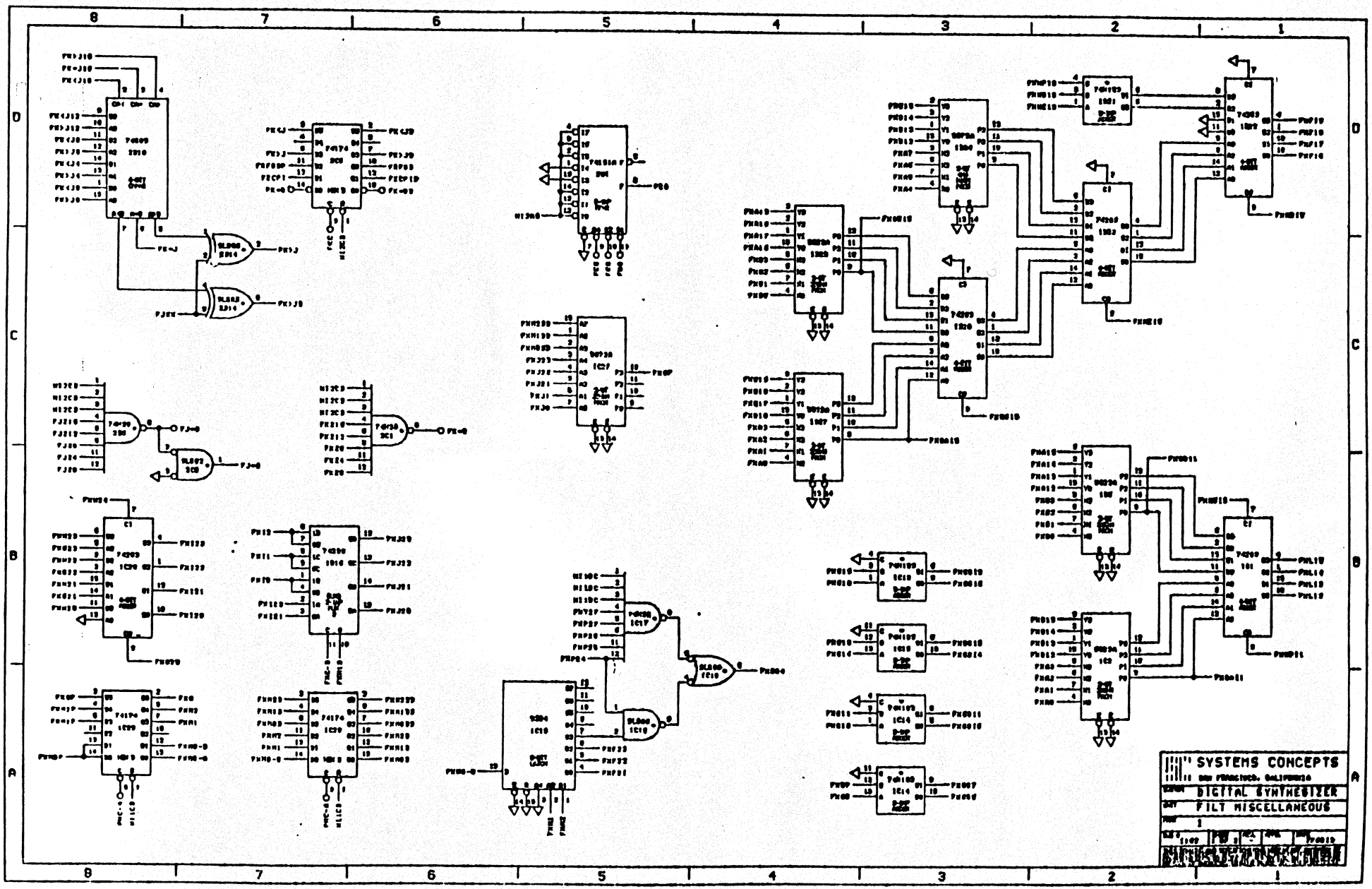
DXM; FLTAC2


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
FILTA CONTROL
2

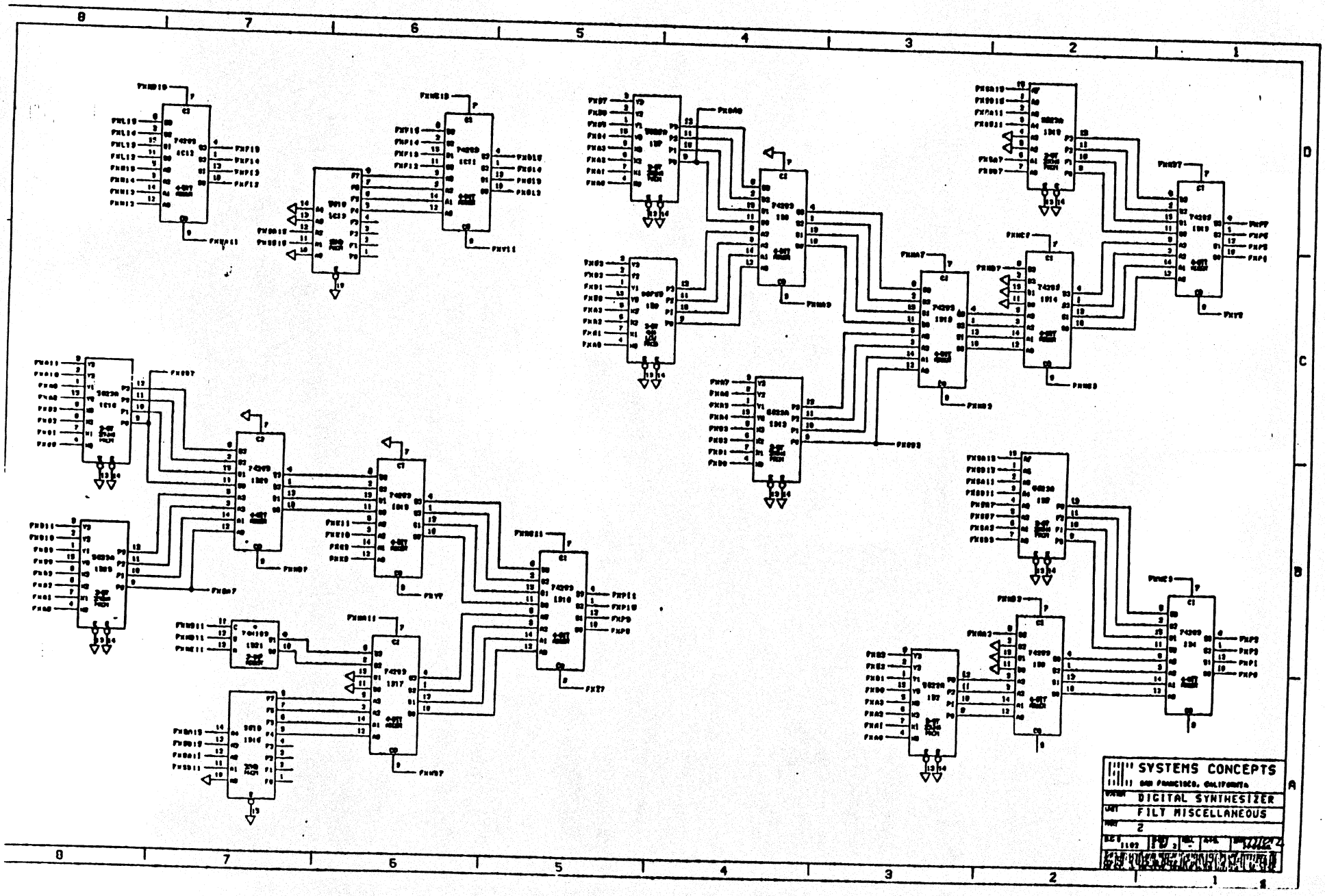
DXM; FILT BC


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
FILTB CONTROL

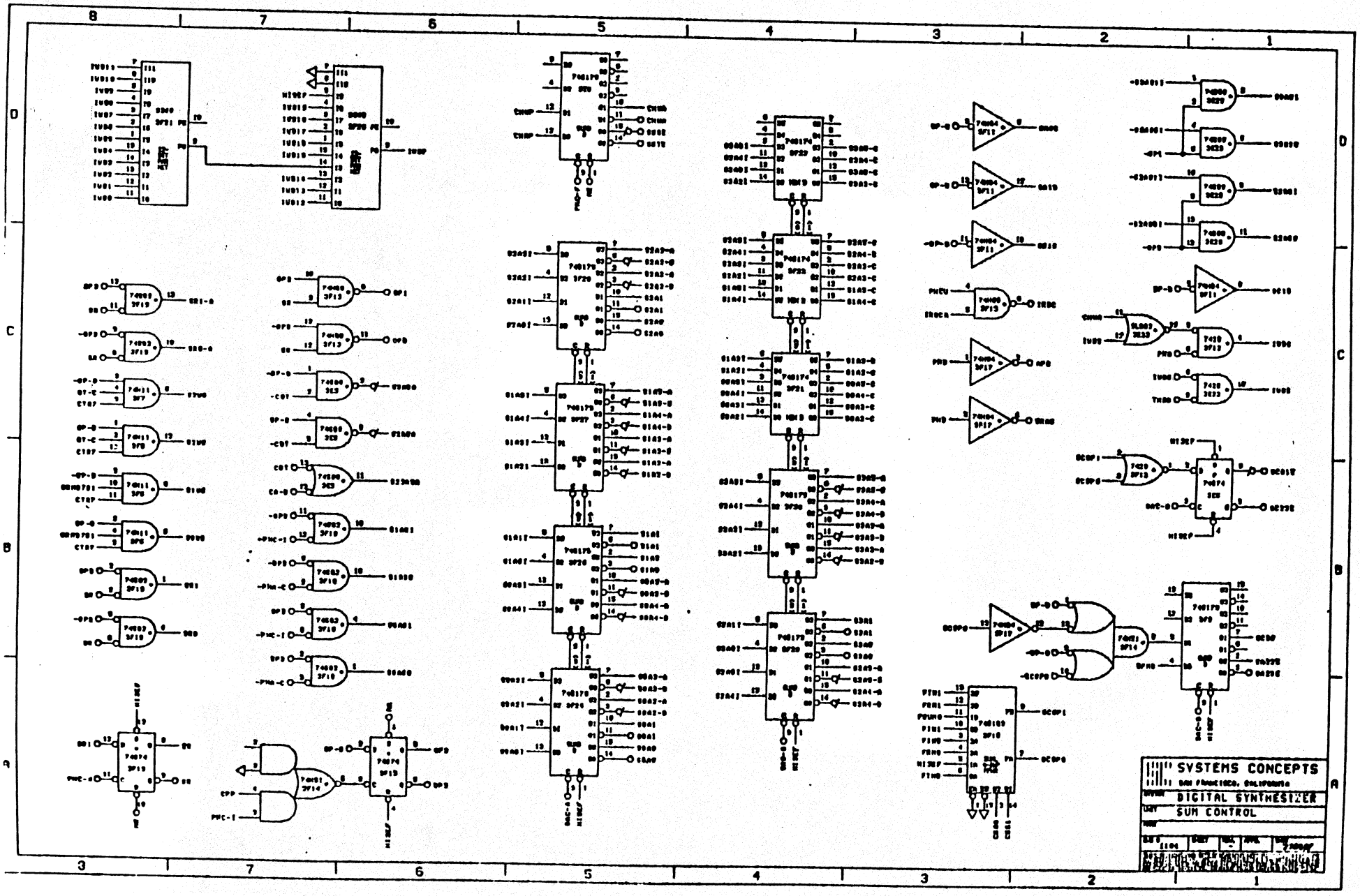
DXM;FILTM1


SYSTEMS CONCEPTS
DIGITAL SYNTHESIZER
FILT MISCELLANEOUS

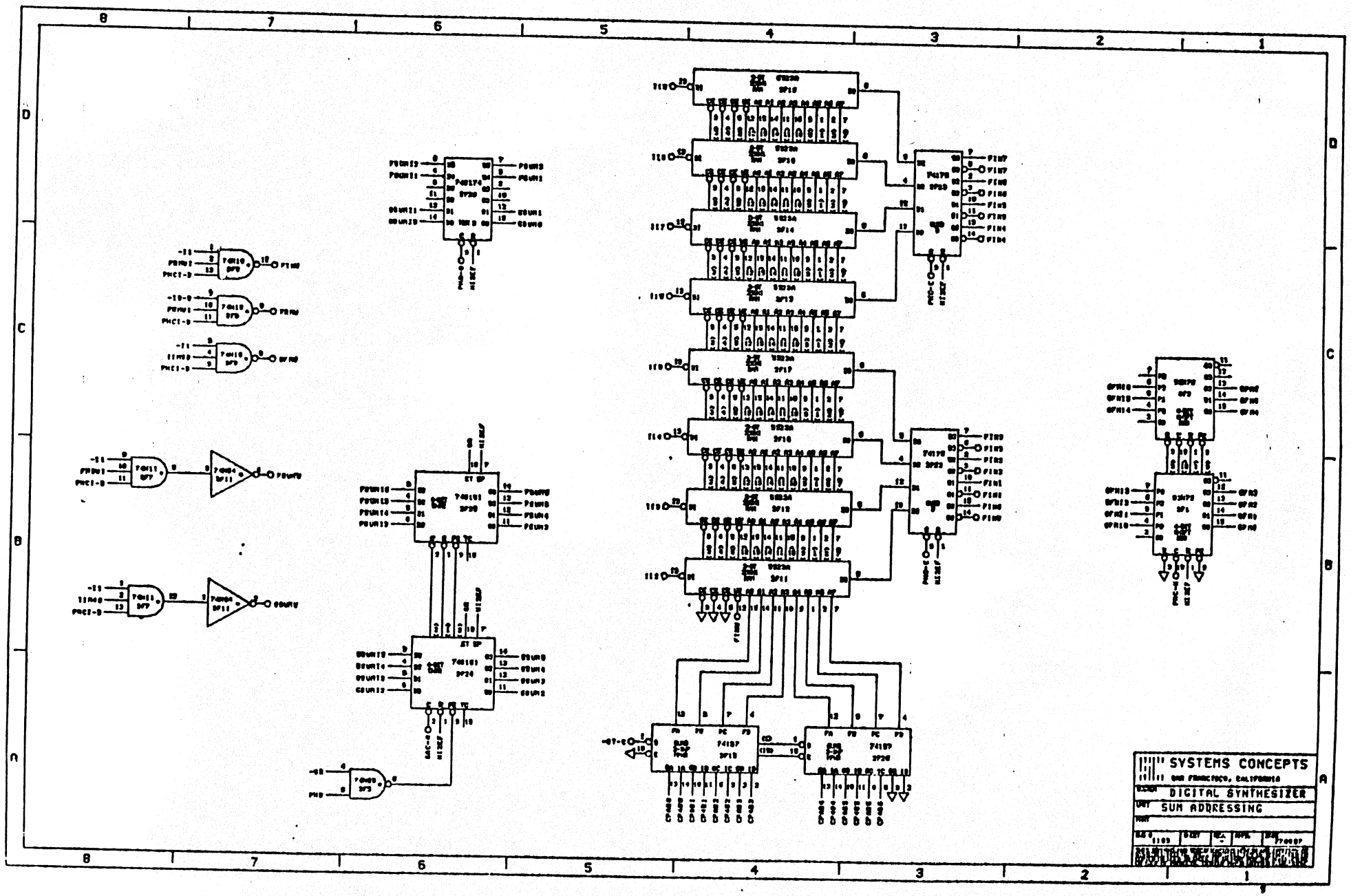
D:XM; FILT/M2


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
FILT MISCELLANEOUS
2

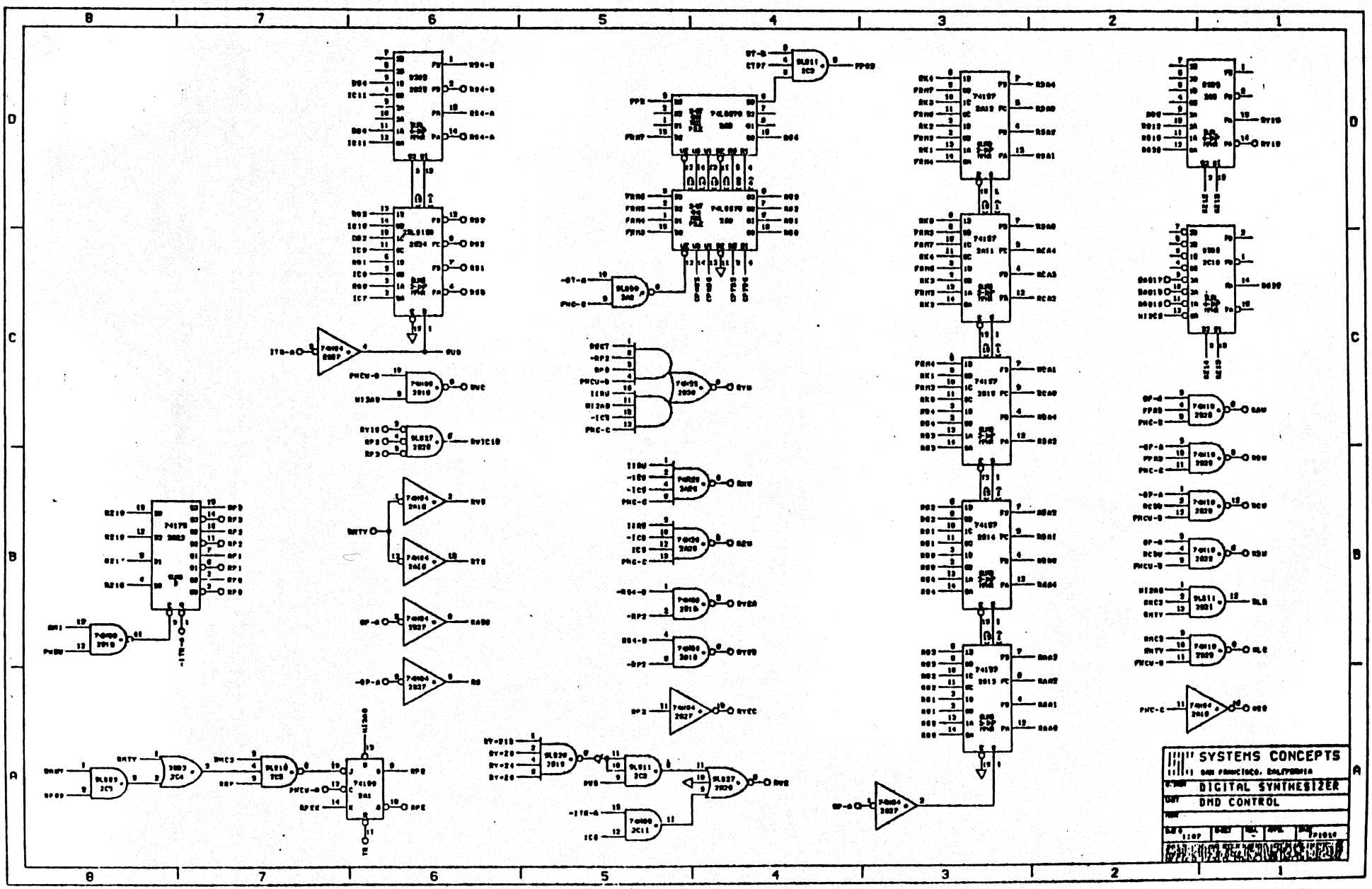
SWB; SUM C


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
SUM CONTROL

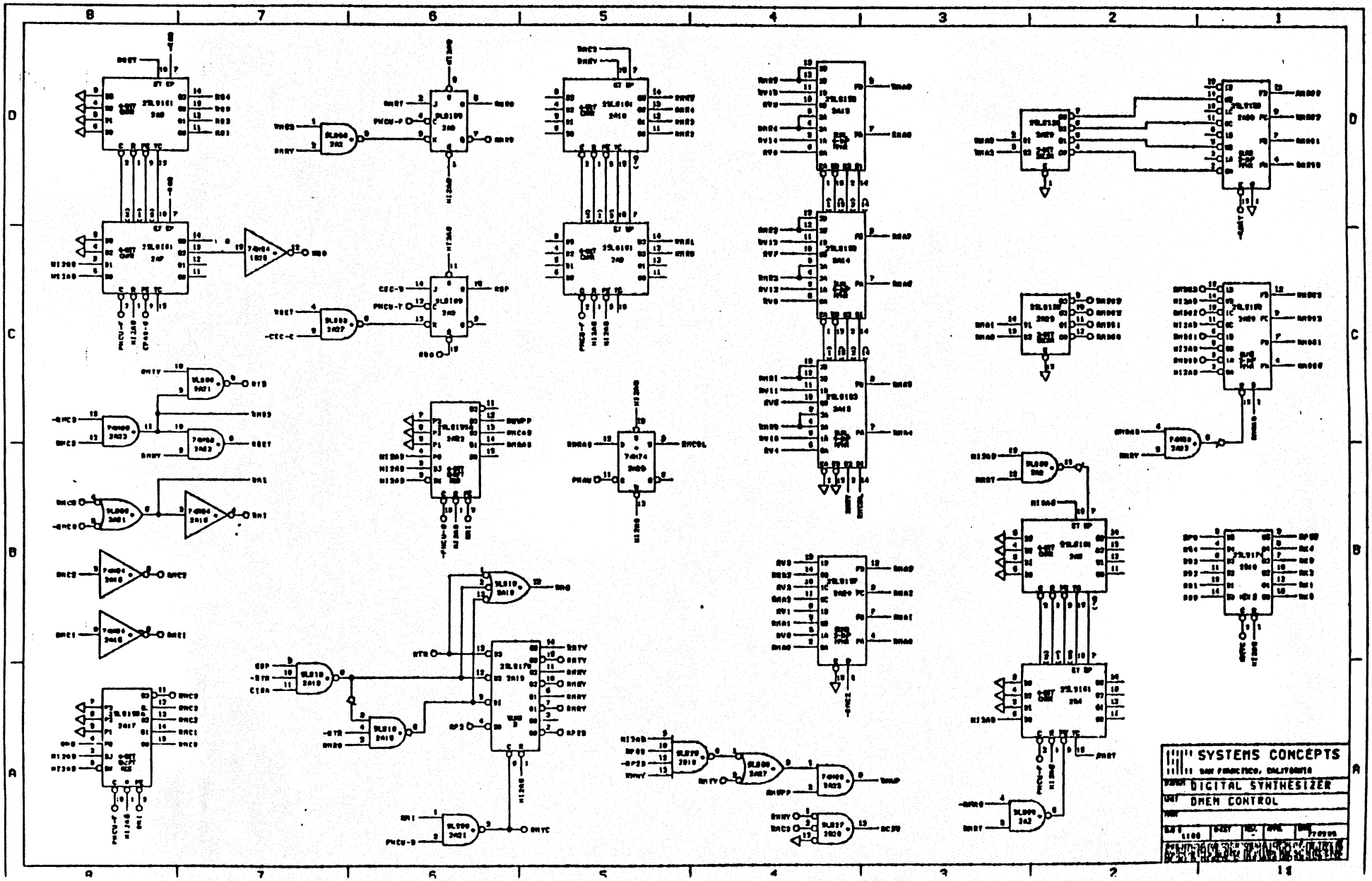
DXM;SUMADD


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
SUM ADDRESSING

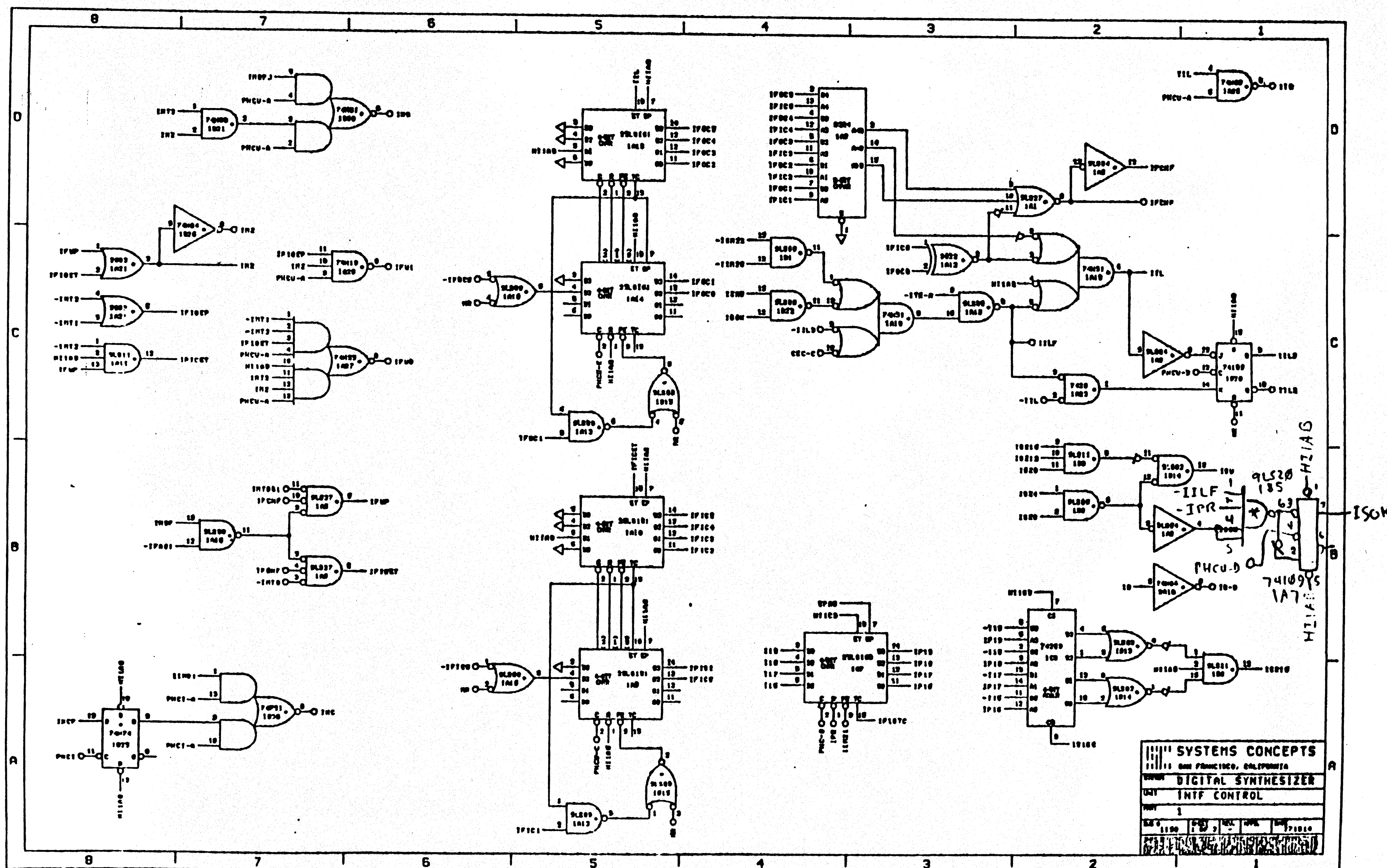
BG; DMDC


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
DMD CONTROL

SRE; DMEMC

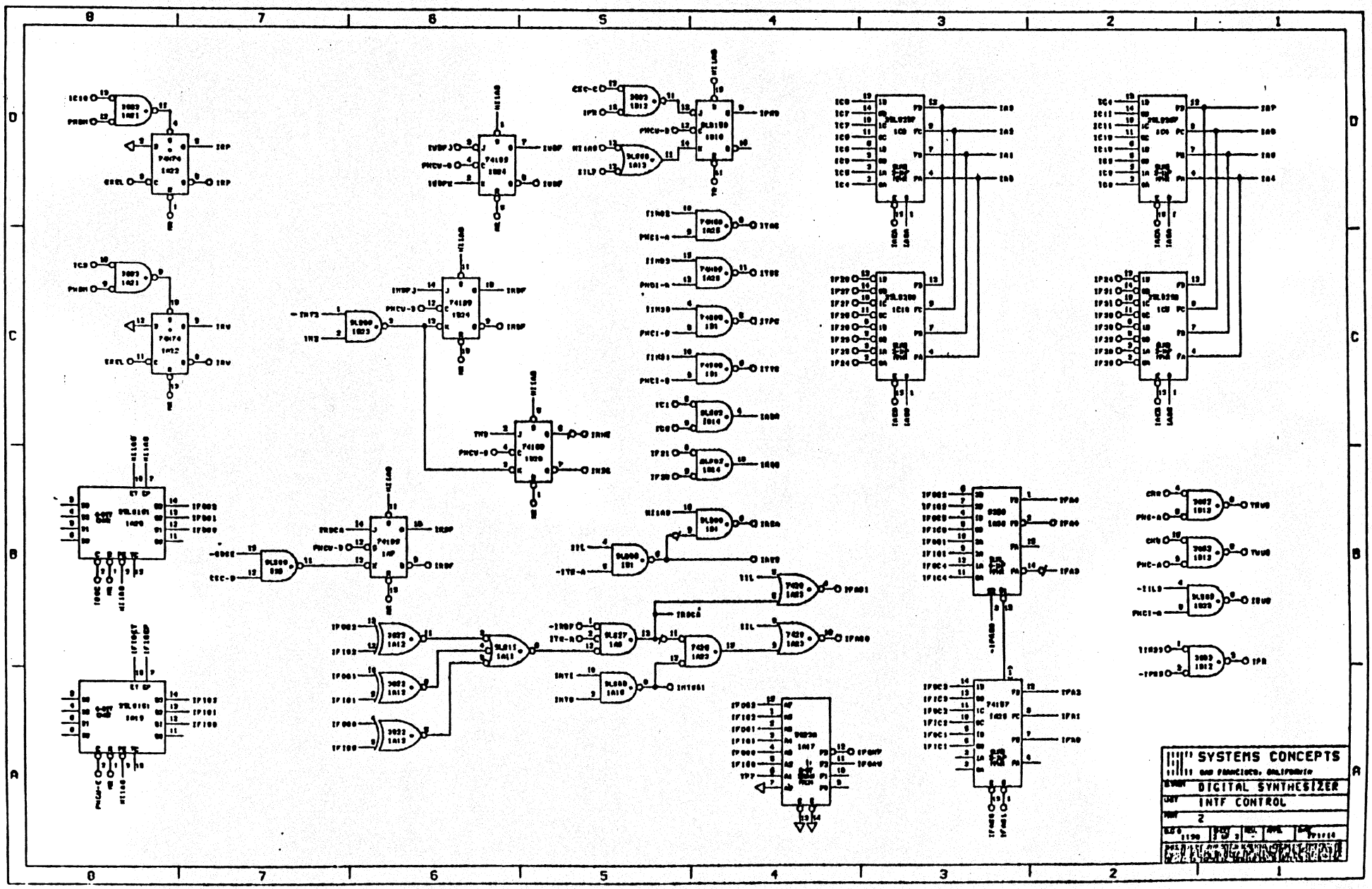

SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
DMEM CONTROL

SWB; INTFC1

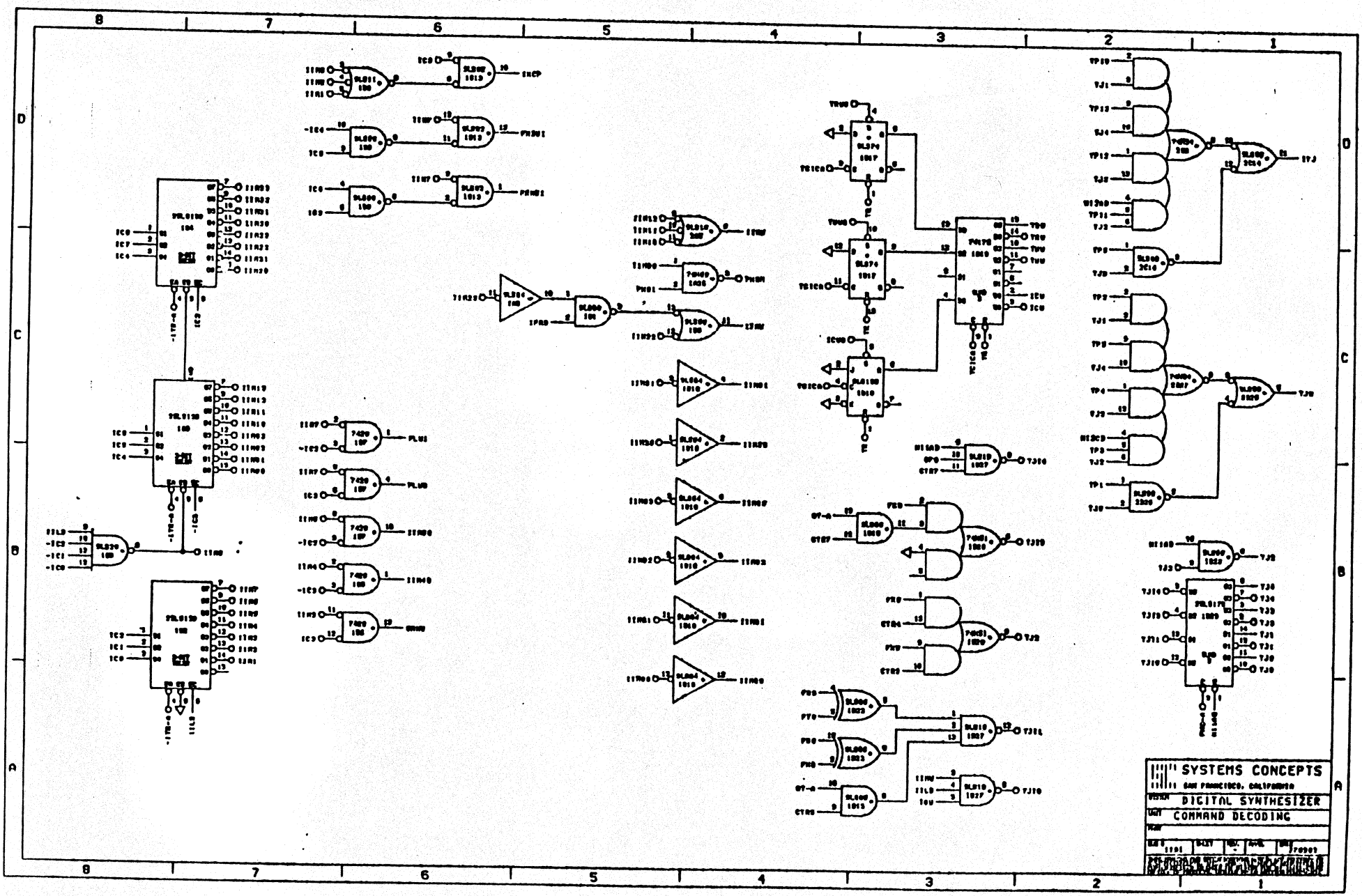


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
INTF CONTROL
-IILF
-IPR
91S20
1B5
PHCU-D
74109
1A7
HI1AG
ISOK

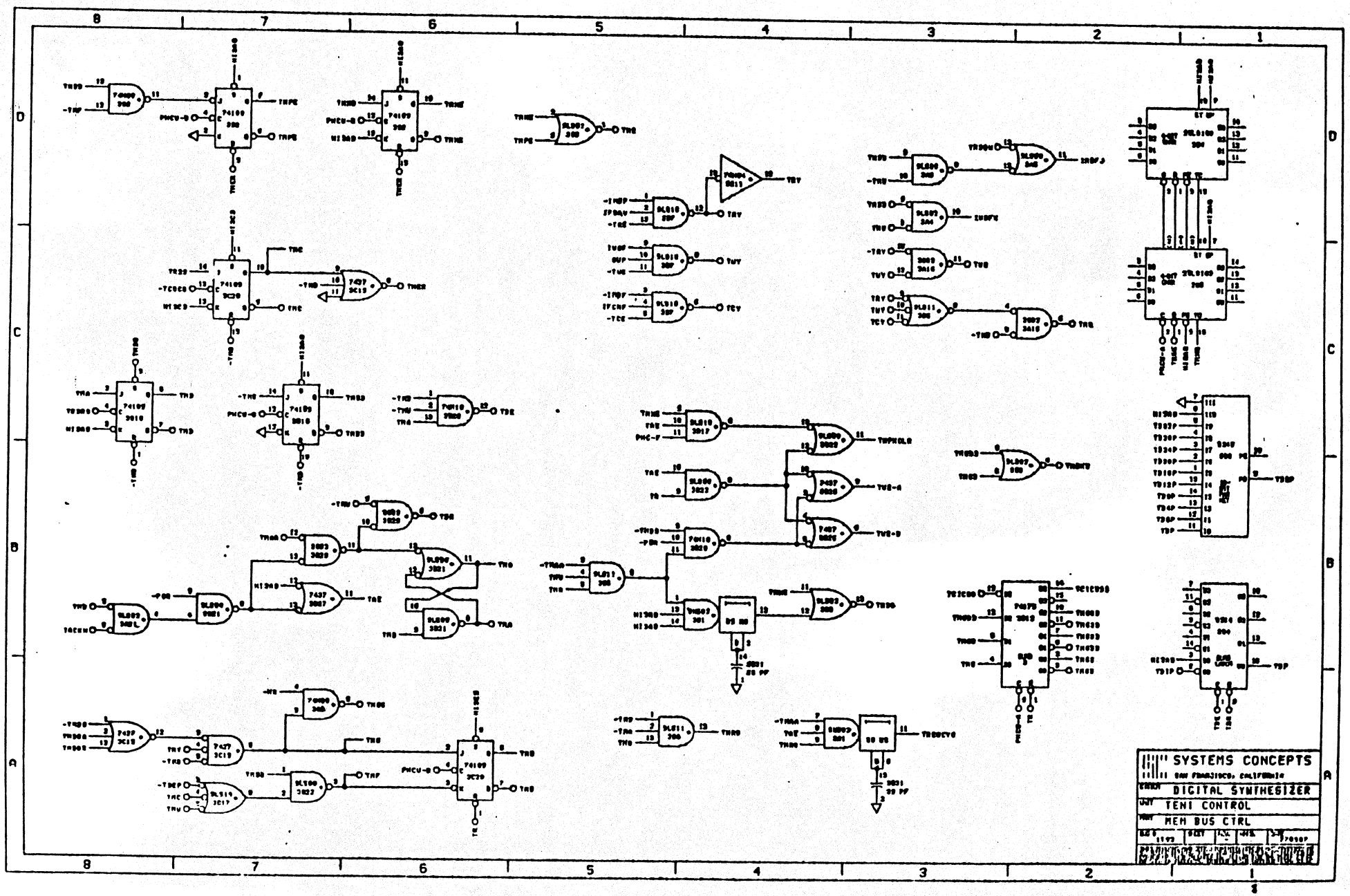
SWB; INTFC2


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
INTF CONTROL
2

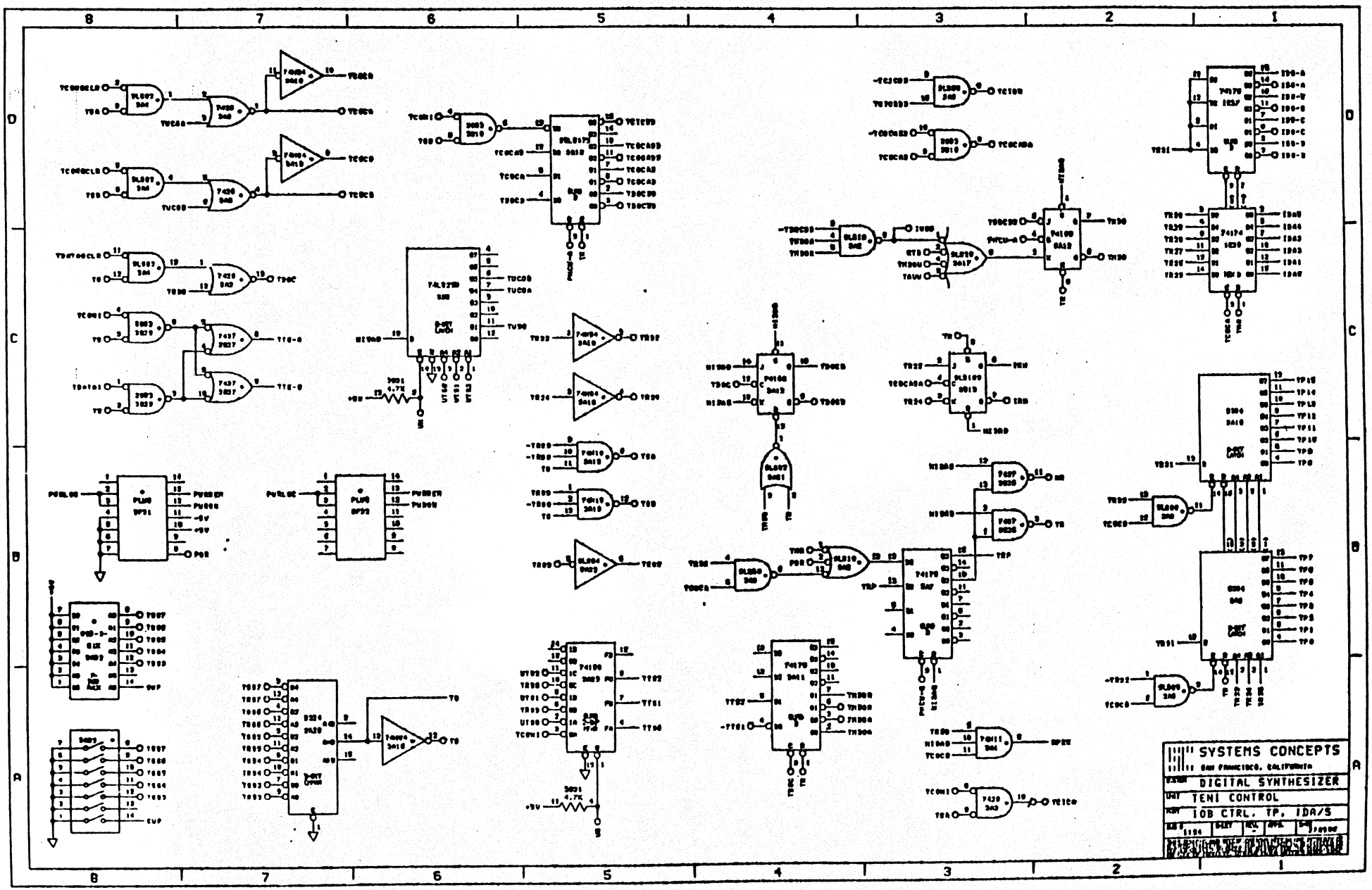
SWB; COMDEC


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
COMMAND DECODING

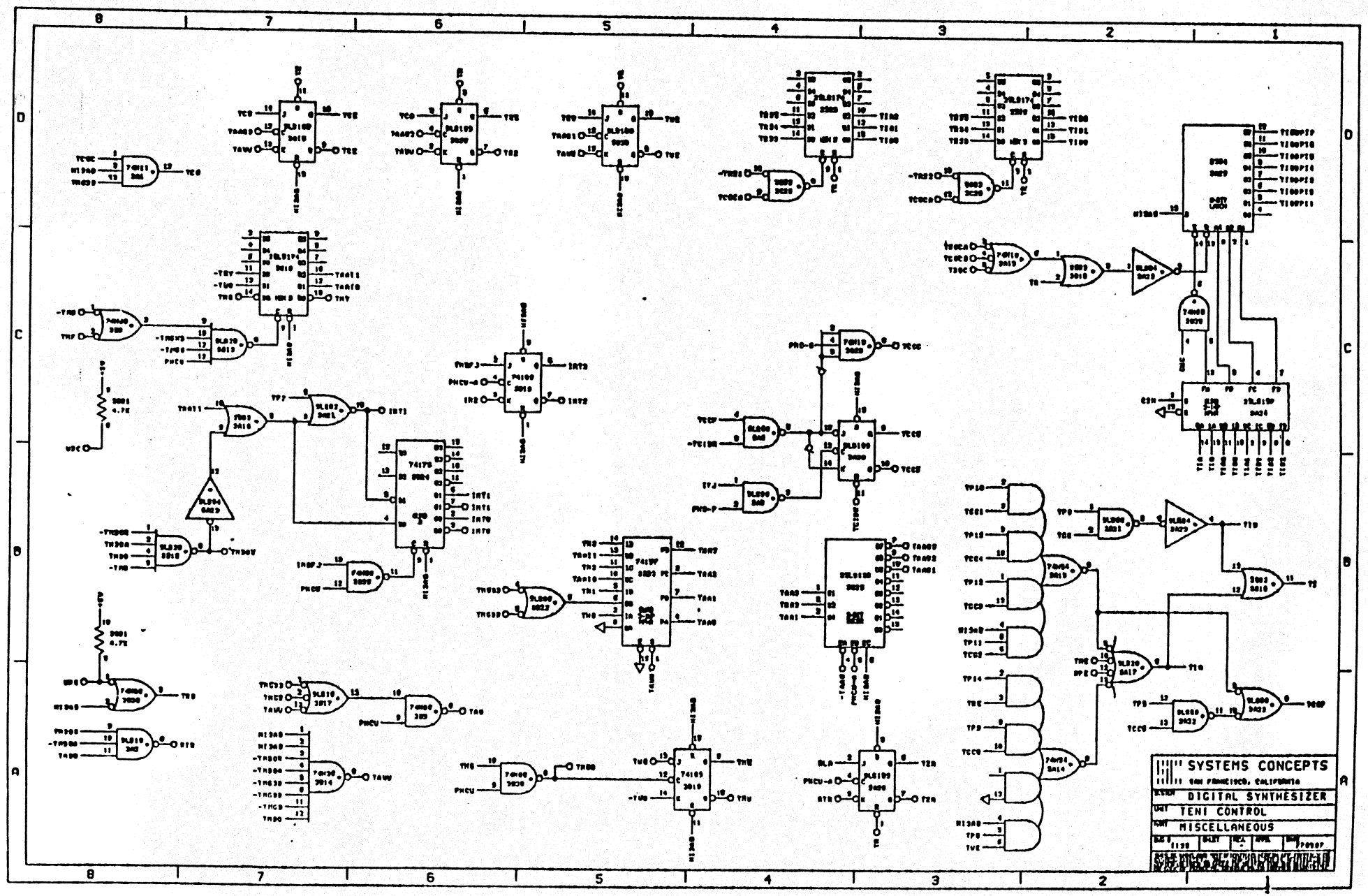
BG; MEMTBC


SYSTEMS CONCEPTS
San Francisco, California
DESIGN DIGITAL SYNTHESIZER
UNIT TENI CONTROL
PART MEM BUS CTRL

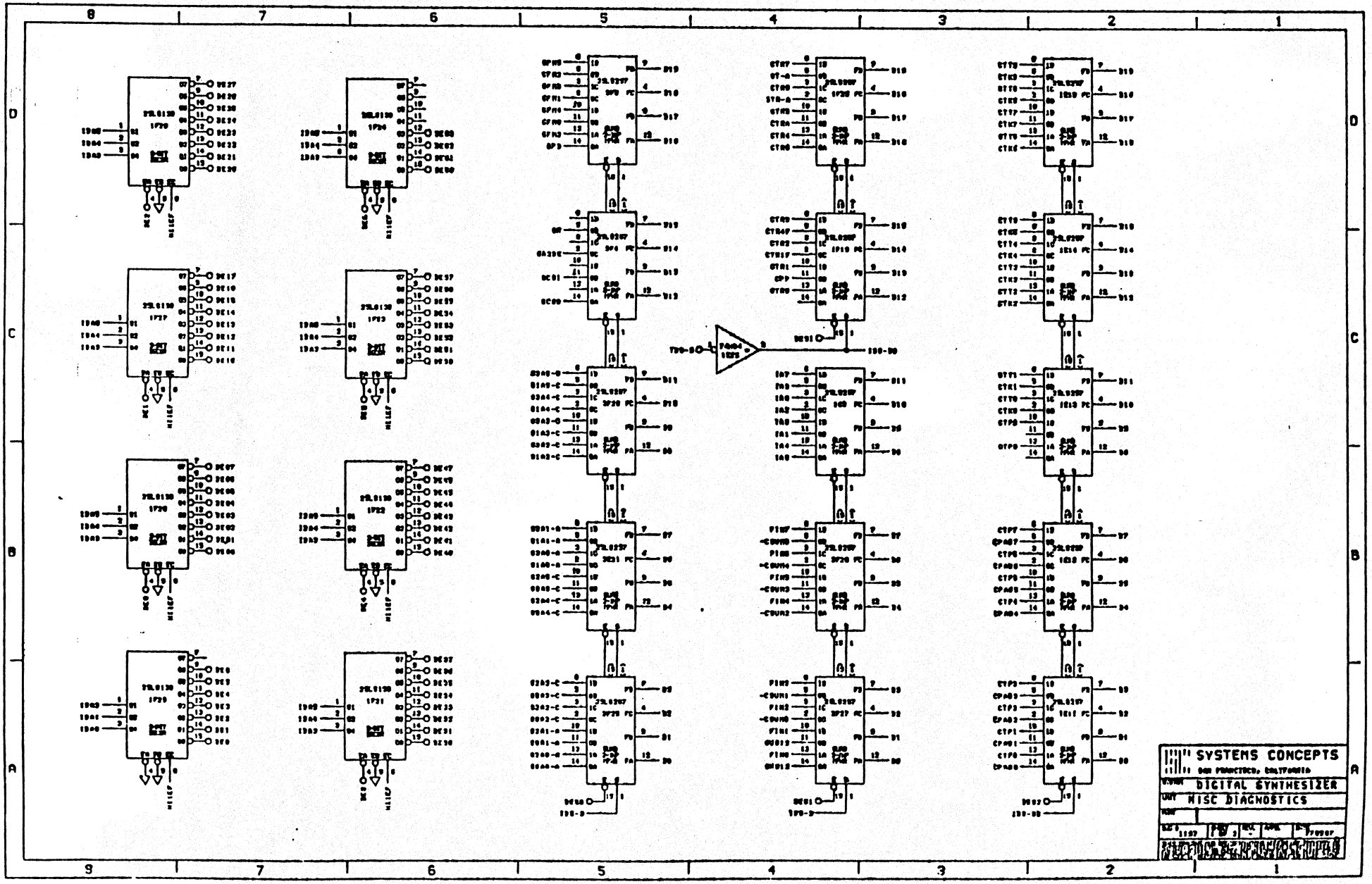
SWB; IOBC


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
TENI CONTROL
IOB CTRL. TP. IDA/S

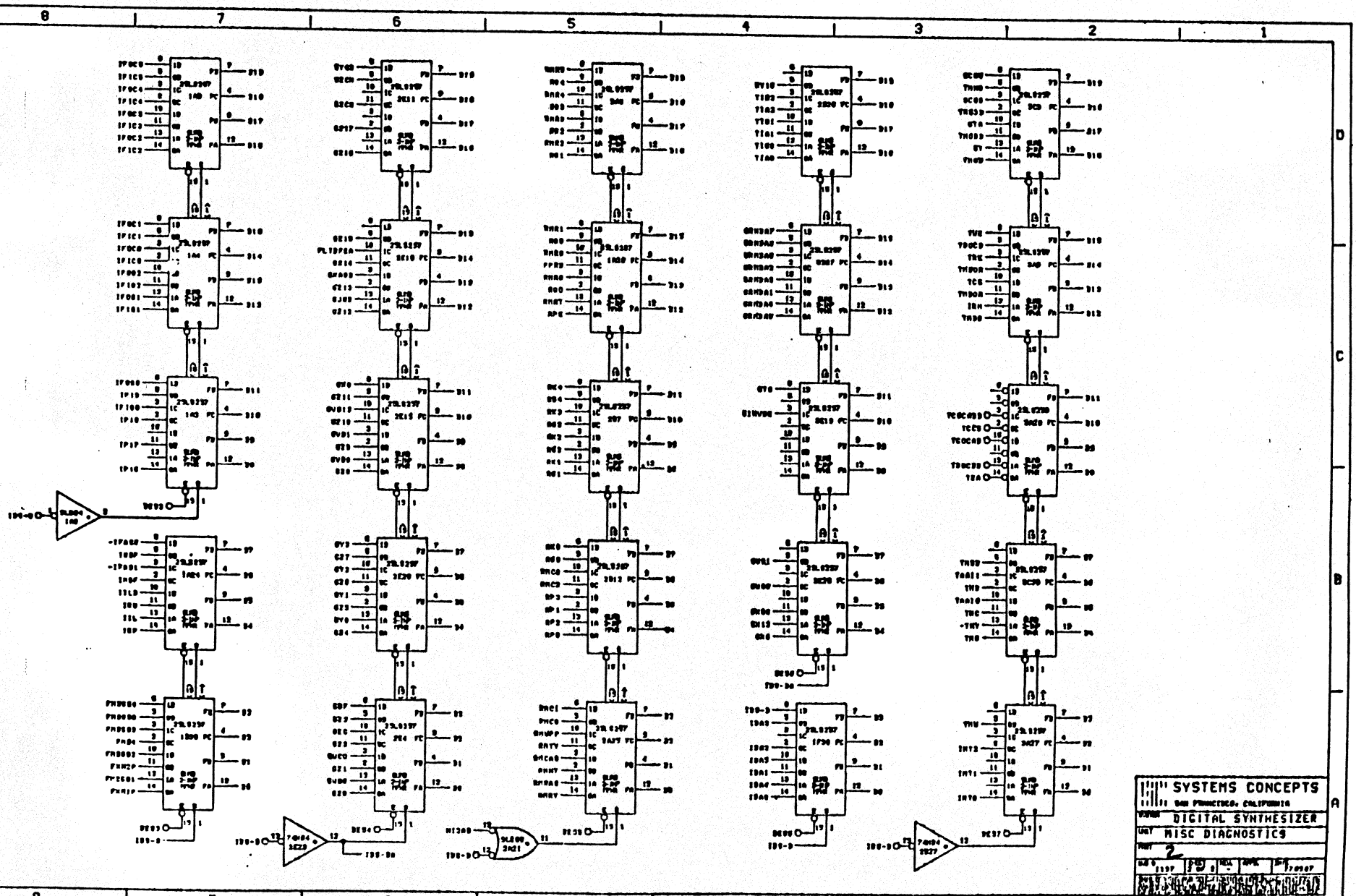
SRE;TMISC


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
TENI CONTROL
MISCELLANEOUS

DxM;MDIAG1

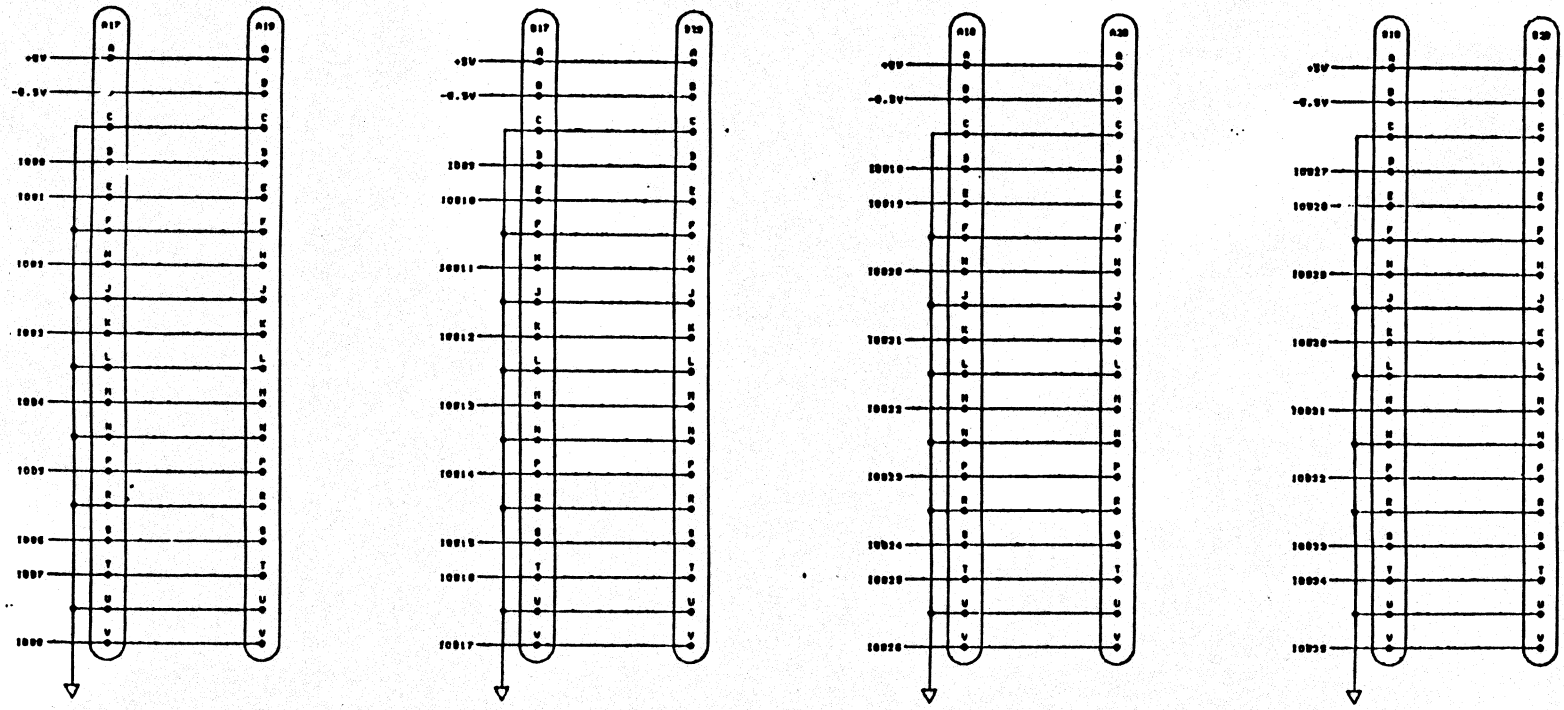

SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
MISC DIAGNOSTICS

DXM; MDIAG2



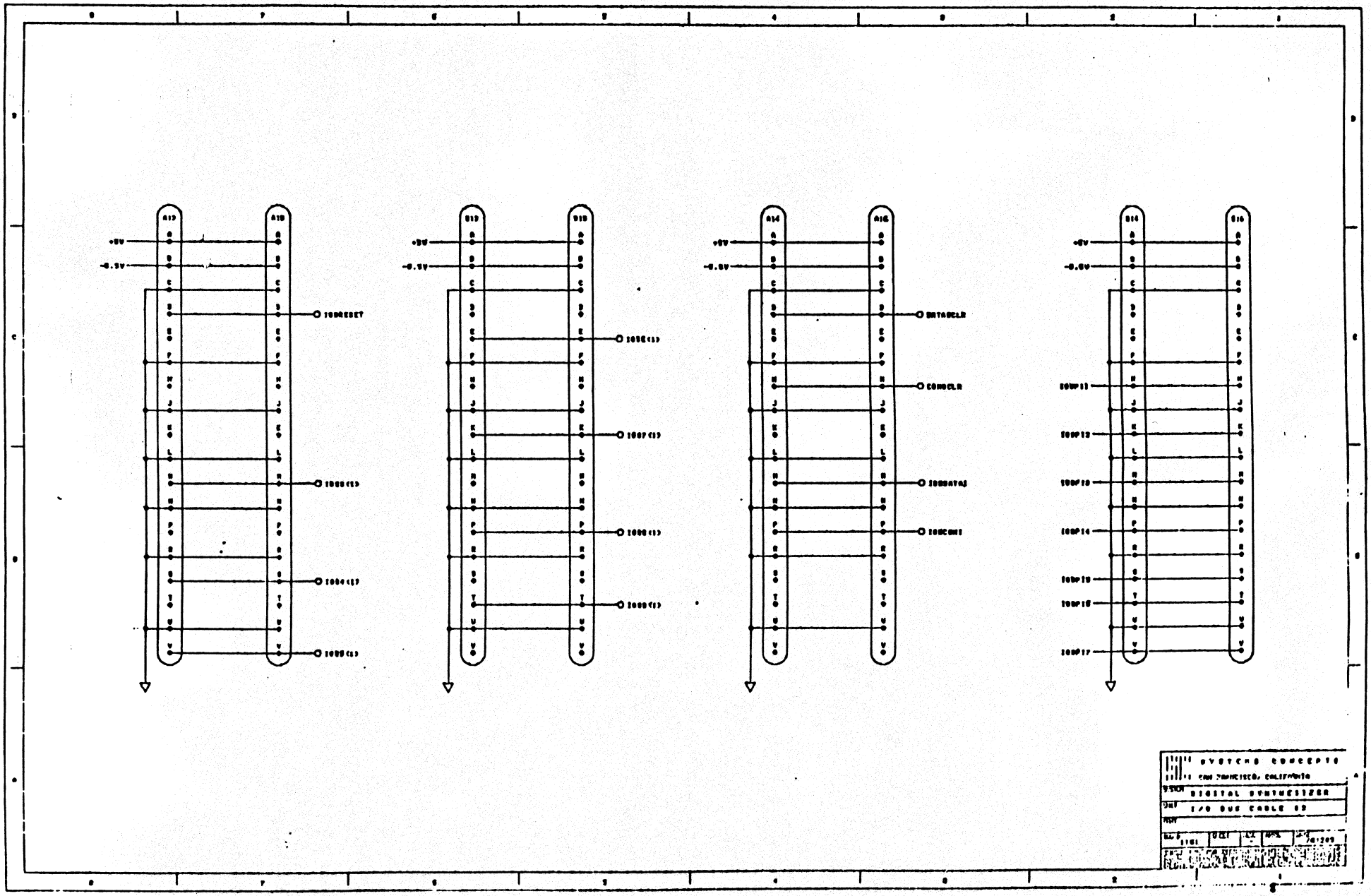
SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
MISC DIAGNOSTICS
PART 2

RLS. IOBCB1

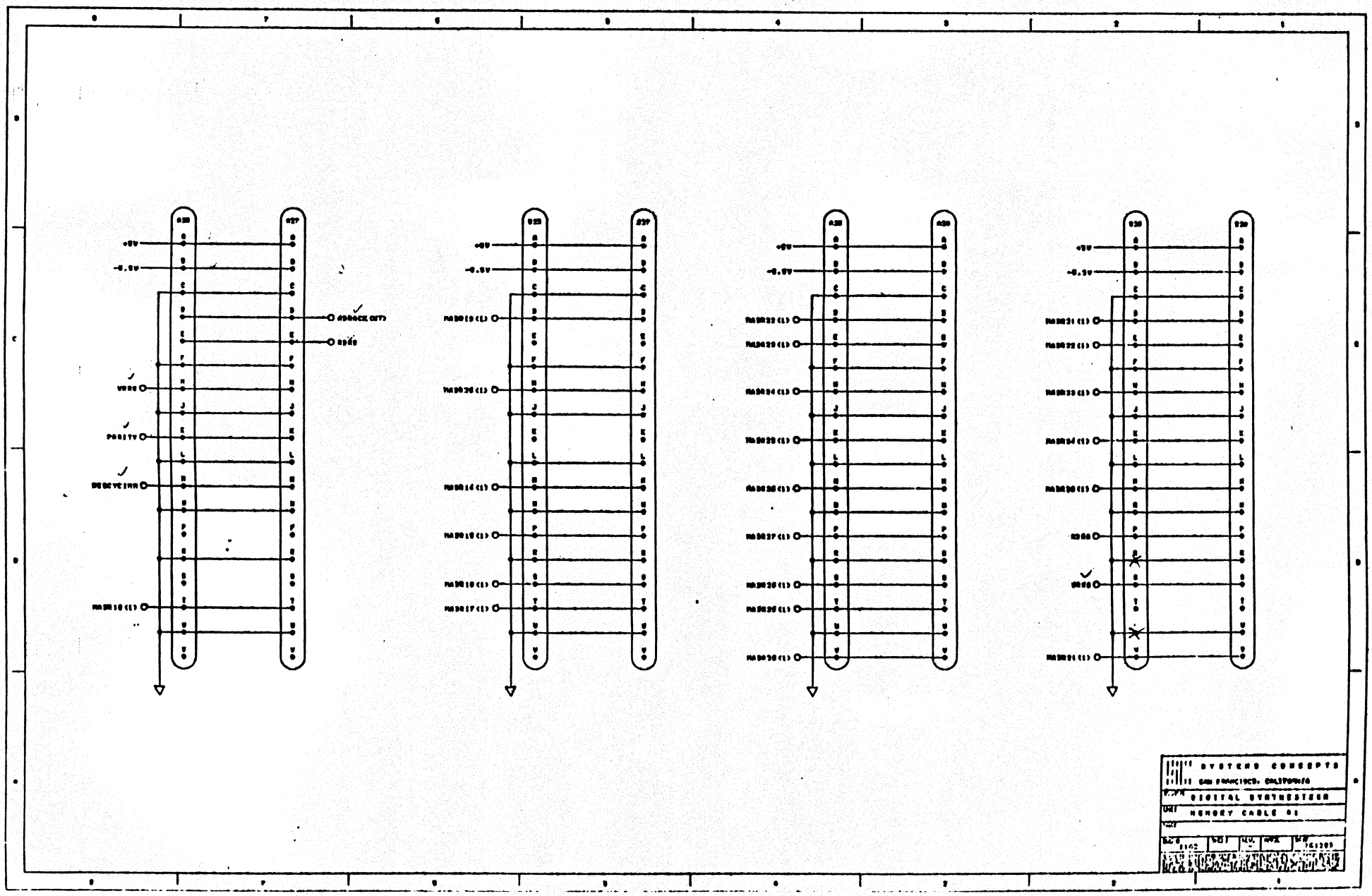


SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
I/O OUT CABLE 01

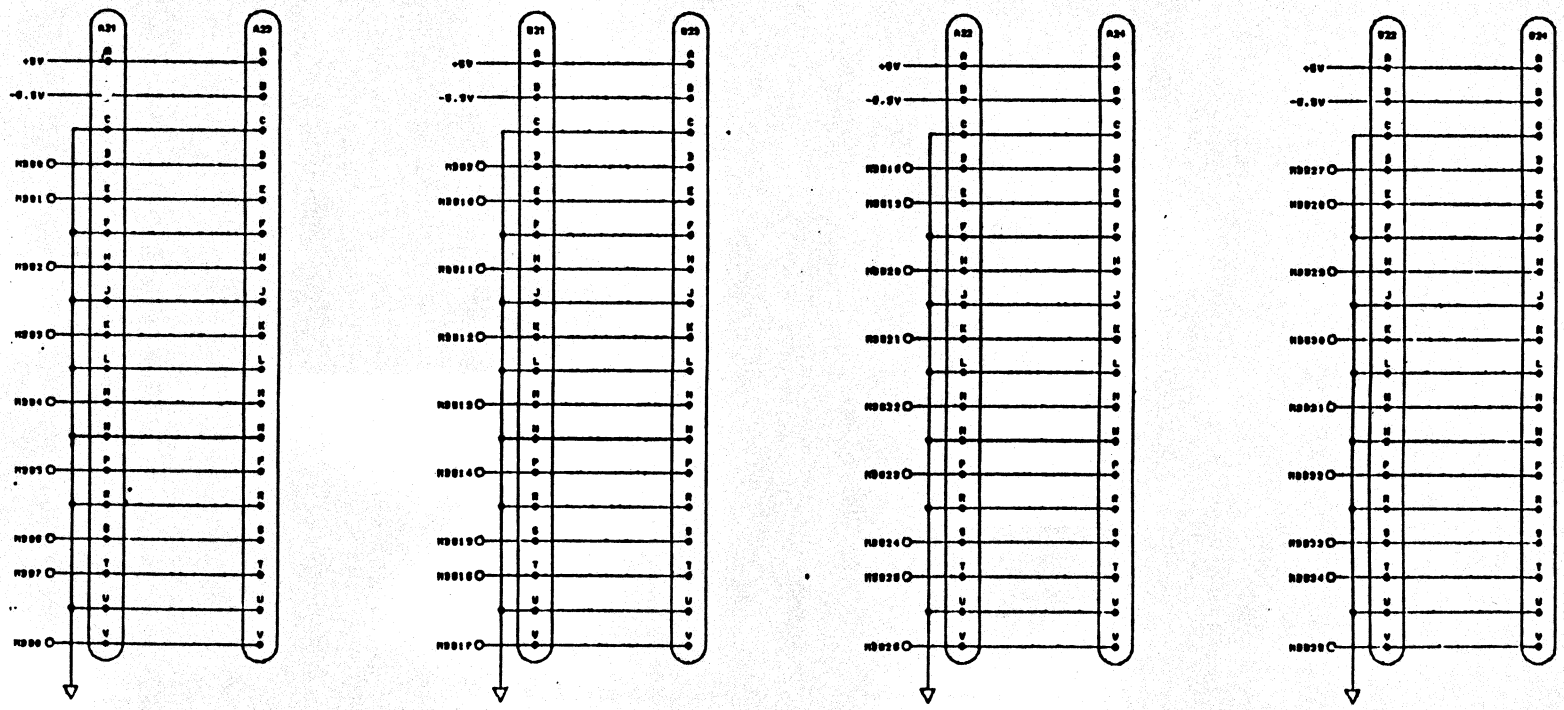
RLS; IOBC B2


+5V
-5.2V
IOBRESET
IOSE(1)
IOBDATA0
IOBCONI
IOBP11
IOBP12
IOBP13
IOBP14
IOBP15
IOBP16
IOBP17
SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
I/O BUS CABLE B2

R2S; MEMCB1

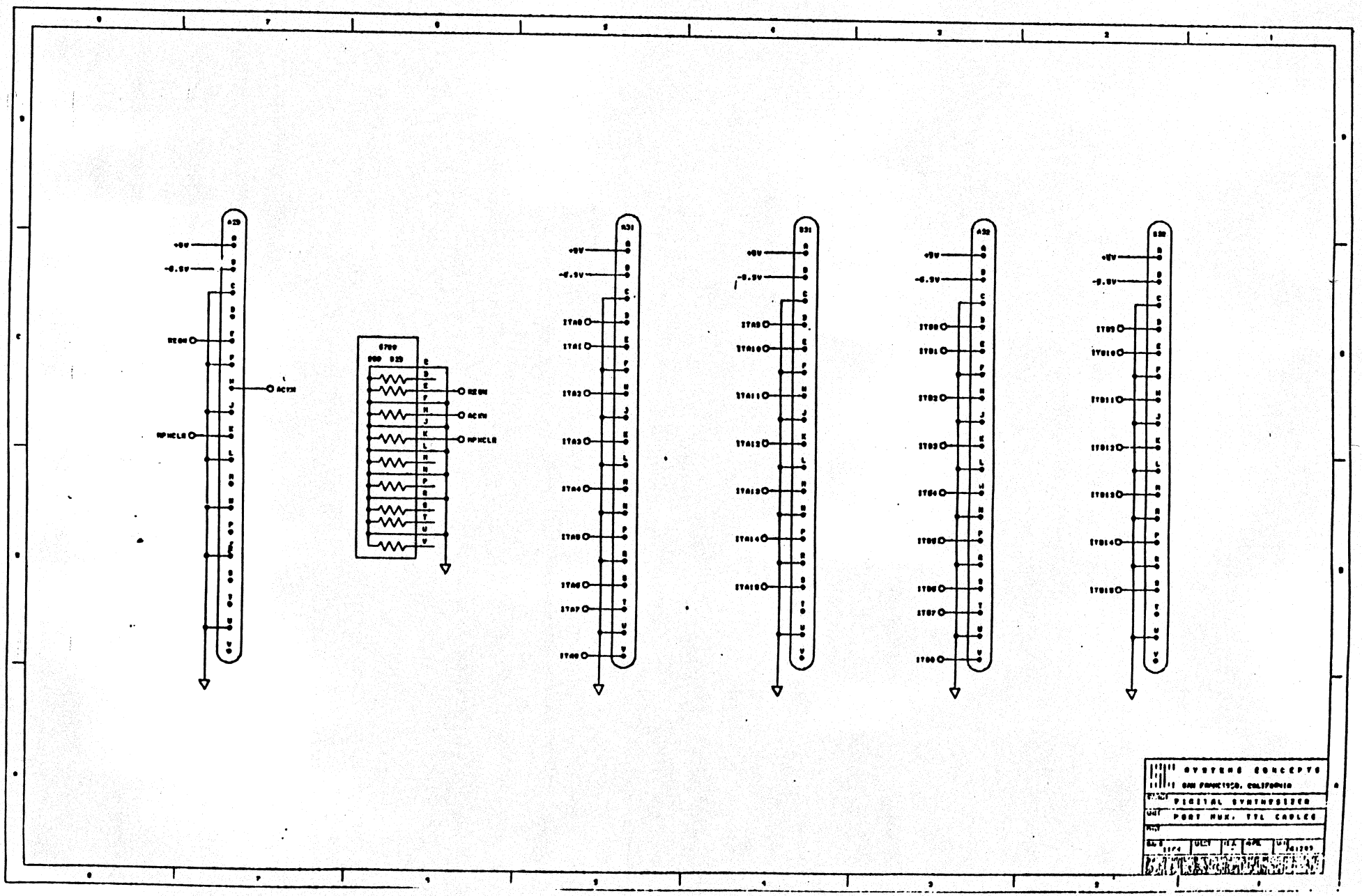

+5V
-5.2V
PARITY
SYSTEM CLOCK (1)
SPARE
SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
MEMORY CABLE 01

RLS; MEMCB2



SYSTEMS CONCEPTS
SAN FRANCISCO, CALIFORNIA
DIGITAL SYNTHESIZER
MEMORY CABLE #2

RLS; PMTCB


+5V
-5.2V
REGN
ACVN
RPHCLB
SYSTEMS CONCEPTS
PALO ALTO, CALIFORNIA
DIGITAL SYNTHESIZER
PORT MUX. TTL CABLES