

the

ATACC

COMPUTER

for Army Tactical Command and Control

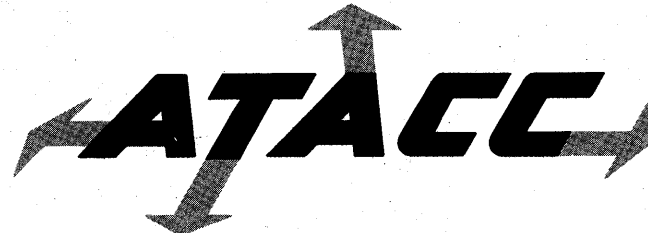
The ATACC Computer

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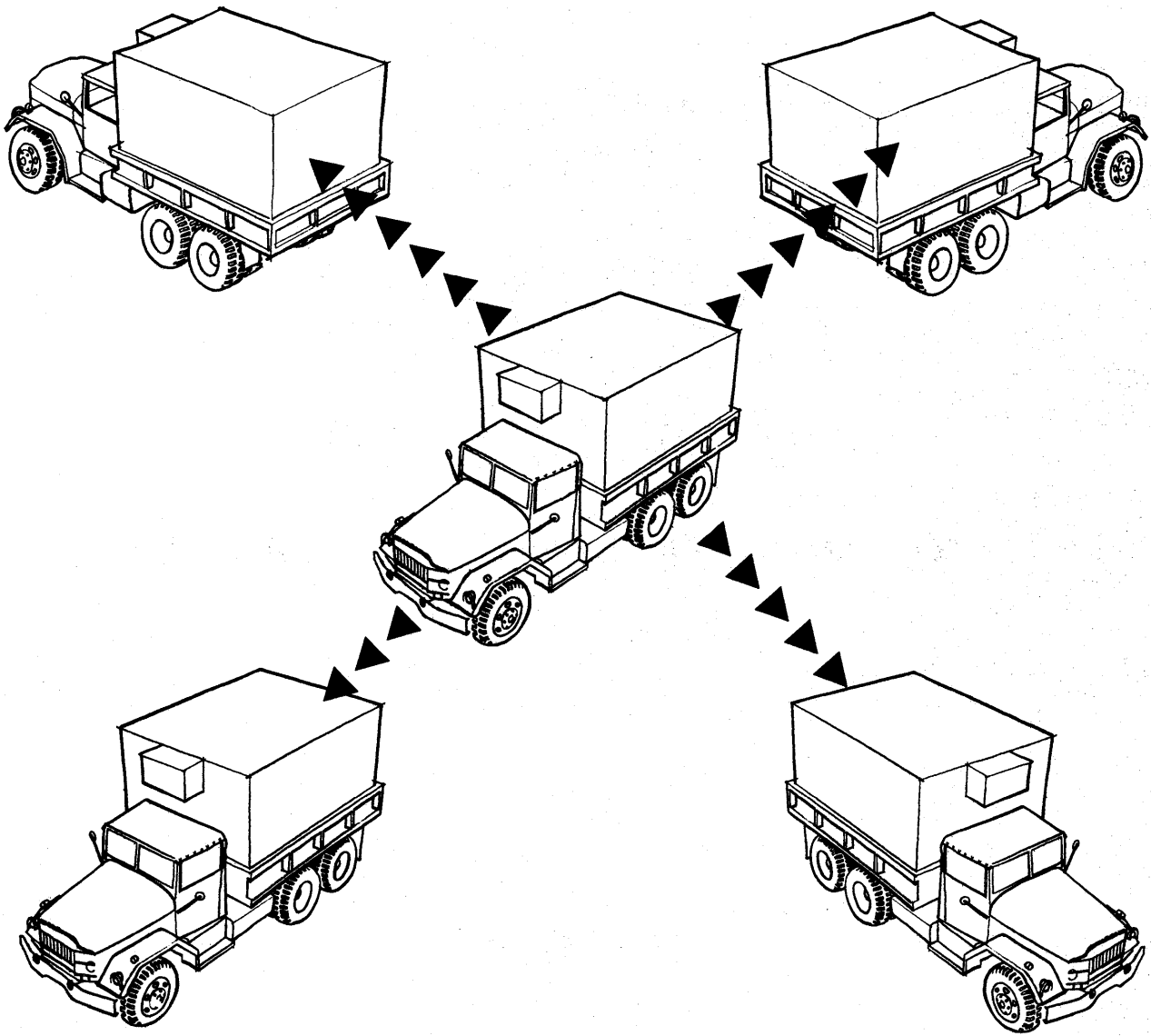
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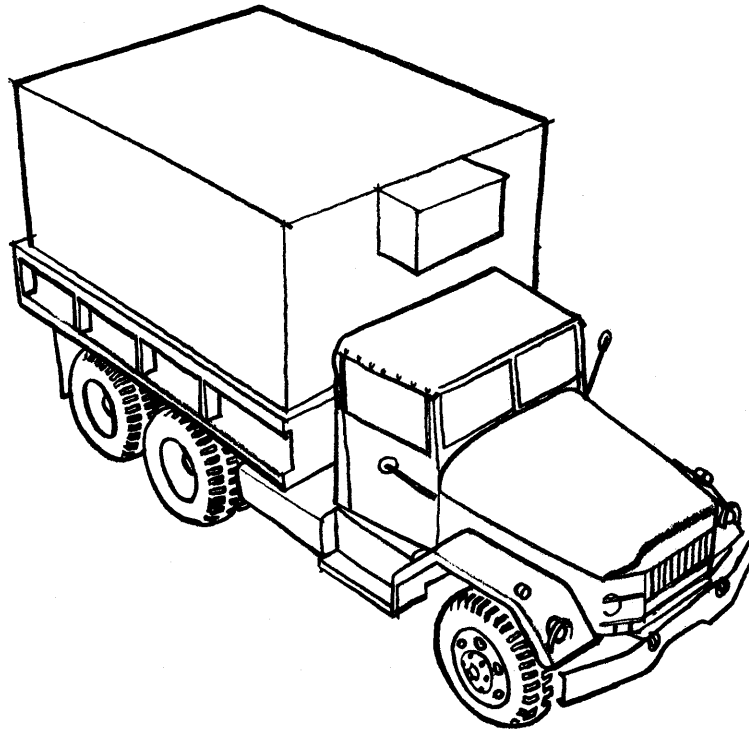


**FIELD ARMY ATACC-EXPANDED
TO HANDLE LARGE ADPS REQUIREMENTS**

the
ATACC
COMPUTER

FOR ARMY TACTICAL COMMAND & CONTROL

30 APRIL 1963



BATTALION ATACC
THE BASIC COMPUTER FOR SMALL ADPS REQUIREMENTS

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SECTION I

PRODUCT DESCRIPTION

1.1 GENERAL FEATURES

The ATACC Computer is a high-speed, general-purpose, modular, Fielddata-compatible data processing system. Designed and built to withstand the full range of military environmental conditions, the ATACC computer is ruggedized and transportable on one or more 2-1/2 ton trucks.

The ATACC has up-to-date, modern data processing capabilities, obtained by product improvement, incorporating and expanding the features of the AN/MYK-1(v) MOBIDIC computer, the Fielddata compatible fixed-plant 9400 computer, the AN/MPQ-32 transportable artillery locator computer, and other Fielddata developments.

As compared to the earlier MOBIDIC, the ATACC computer offers improvements in:

- PERFORMANCE** – The ATACC computer is an advanced programming tool providing continuous access to up to 128,000 words of memory, using an augmented Fielddata order code and greater simultaneity and control of input/output equipment.
- SPEED** – More rapid memory access and higher circuit speeds are utilized.
- SIZE & WEIGHT** – A smaller, lighter equipment results from repackaging and reductions in circuit complexity.
- TACTICAL USE** – Design of the ATACC computer started with the shelters which are the standard Army S-109 shelters, suitable for mounting on the back of 2-1/2 ton trucks. The shelters are "fitted" for the installation of a variety of computer units to permit the efficient application of the same Central Processor to problems which range from those at the Battalion echelon, where a single shelter can perform the entire data processing task, to those at the Field Army echelon, where a combination of three or more shelters may be required.

1.2 THE ATACC SHELTERS

The "fitted" shelters which house the ATACC data processing equipment are standard Army S-109 shelters which can be mounted on 2-1/2 ton trucks for cross-country transportation or air-lifted by a variety of aircraft, including helicopters. There are three shelter types, and one or more shelters, suitably equipped with modular inserts, can be used to serve all classes of military data processing functions.

1.2.1 Type 1, The Central Processor Shelter

This shelter, shown in Figure 1-1, contains the Main Frame, regardless of application. The Main Frame is made up of the Central Processor and Main Console, including a paper tape set; the ATACC Input/Output Converter; and a single core memory rack, holding either 16,000 or 32,000 words of storage. It is also fitted to accommodate additional racks of equipment. Depending on the particular application, these racks could be assembled in a variety of combinations including: a Communications Converter with 24 channels of AN/TYC-1 communication terminal equipment; additional core memory units, permitting the expansion of memory up to 128,000 words; militarized pneumatic magnetic tape transports; militarized card reader/punch units; a militarized rack-mounted line printer; or a random access memory disc file.

The shelter, in its basic form, contains all wiring and mounting fittings necessary for installing eight relay racks of equipment. This includes all air ducts, wiring ducts, cable terminations, and rack supports. The Main Frame consists of the equivalent of three relay racks. All of the other equipment listed above consists of single relay racks or double rack units, which are physically modular and mate with mounting supports. Wiring permanently fixed in the shelter consists of high-speed bus lines with cable terminations to tie directly to memory units; and high-speed input-output bus lines to tie to magnetic tape unit racks or random access memory racks; and low-speed bus lines to tie to card reader/punch or line printer racks.

External terminations on the Type 1 shelter provide for connection to power source and communications lines. In the minimum applications, these suffice to accommodate a complete working system. Additional terminations are provided in the basic shelter design so that both high-speed and low-speed bus

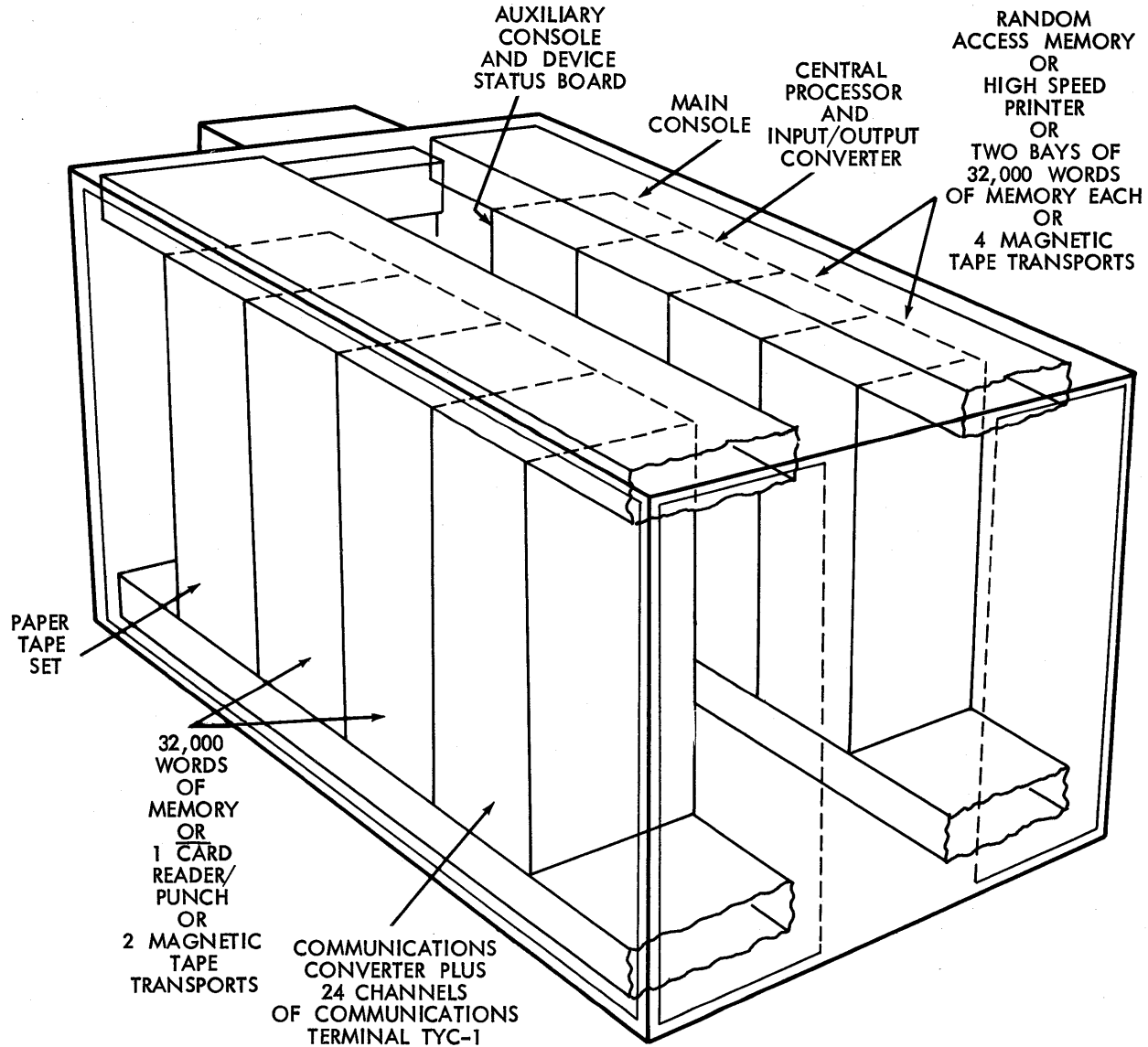


Figure 1-1. ATACC Central Processor Shelter (Type 1 Shelter)

lines can be run to other shelters, containing additional input/output devices. The cable connections are sufficient so that a total of four additional shelters can be connected to the Type 1 Central Processor shelter.

1. 2. 2 Type 2, High-Speed Input/Output Shelter

Figure 1-2 depicts this shelter, which conforms to the same basic shelter design as the Central Processor shelter. But, unlike the Type 1 shelter, this shelter is designed exclusively for high-speed input/output equipment and, therefore, contains wiring provisions for power and for a high-speed input/output bus system. Like the Type 1 shelter, this housing has provisions for eight standard racks of equipment. Two of the racks are set up for storage and have space for an auxiliary console, to facilitate operations from this shelter, and for the magnetic tape Direct Switching Units. The other six rack spaces may be allocated to up to three Random Access Memories or up to twelve Magnetic Tape Units, in a variety of combinations.

1. 2. 3 Type 3, Low-Speed Input/Output Shelter

The Type 3 shelter shown in Figure 1-3 is almost identical to the Type 2 shelter, except that it is fitted for use with low-speed input/output devices, and, therefore, contains a low-speed input/output bus line. Again provision is made for eight relay racks permitting the installation of up to six card reader/punch units or up to three line printers or some combination thereof. Two racks are again set aside for storage and an auxiliary console.

1. 2. 4 ATACC Computer Configurations

The modular principal which governs the assembly of shelters into a complete computer configuration can be seen in Table 1-1. The flexibility demonstrated in this table is such that a variety of input/output configurations could be assembled, varying from a minimal configuration utilizing only one shelter up to a greatly expanded configuration using as many as five shelters.

The versatility is shown in Figure 1-4. The top illustration shows an ATACC configuration suitable for use at lower echelons. The Main Frame is augmented by a suitable complement of input/output devices. In the case

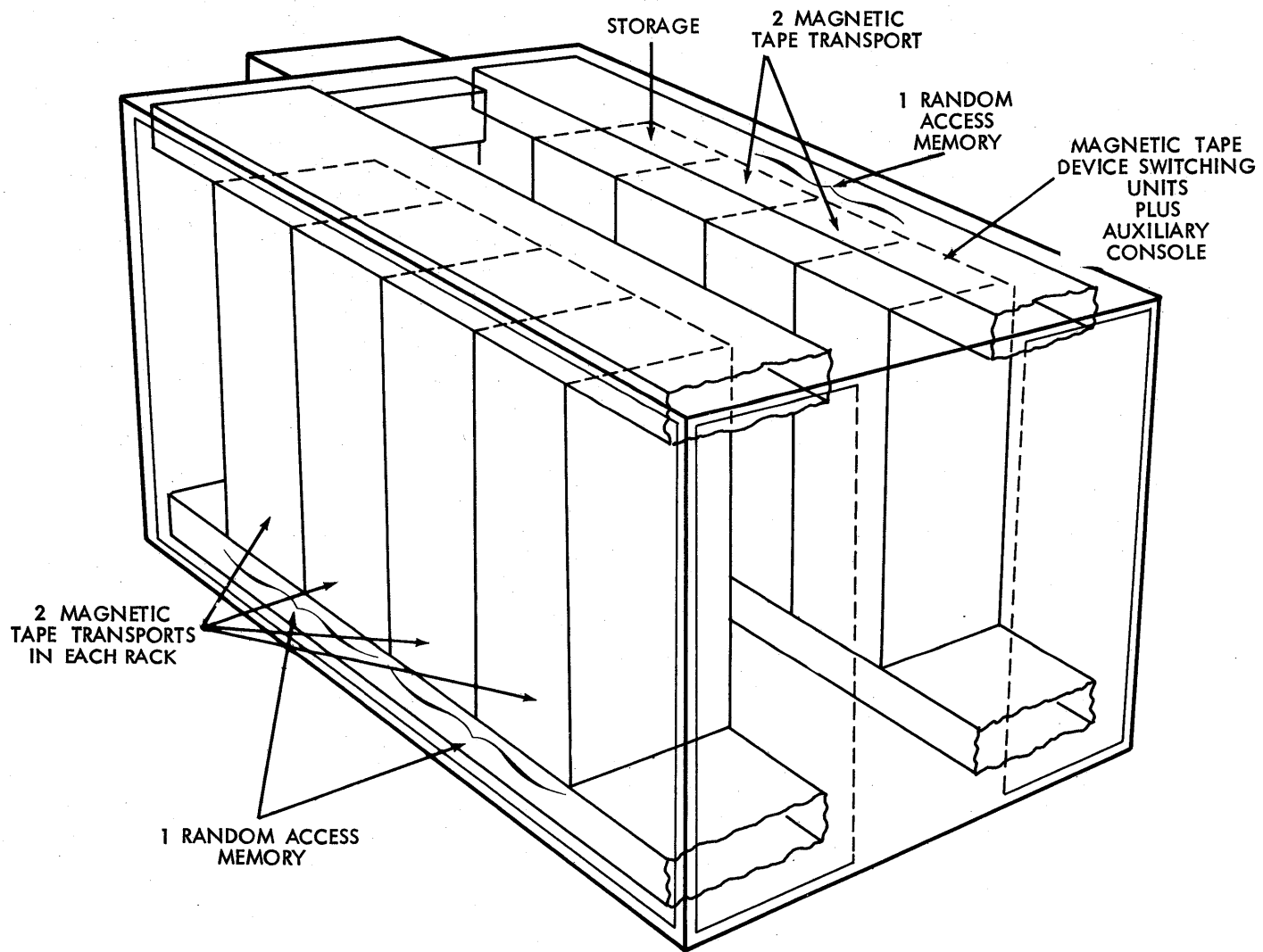


Figure 1-2. ATACC High-Speed Input-Output Device Shelter (Type 2 Shelter)

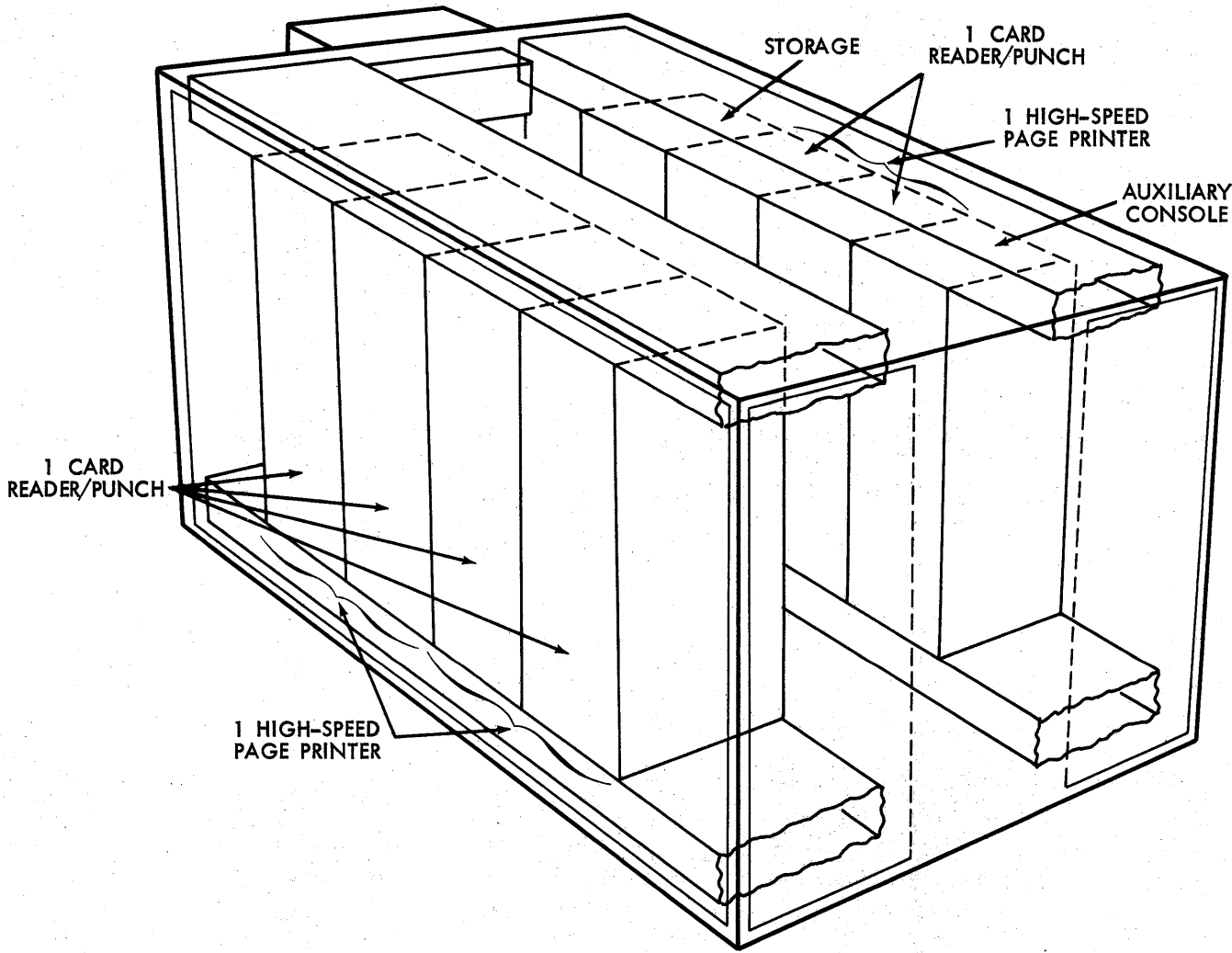
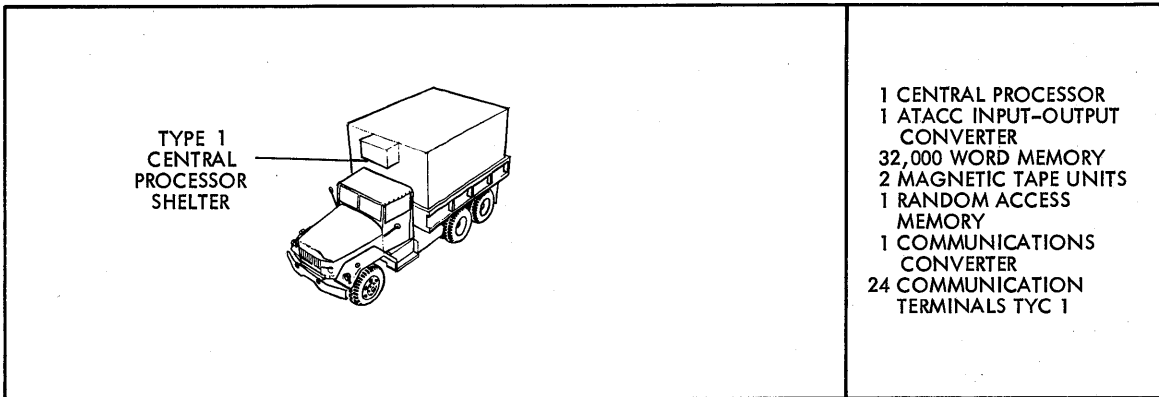
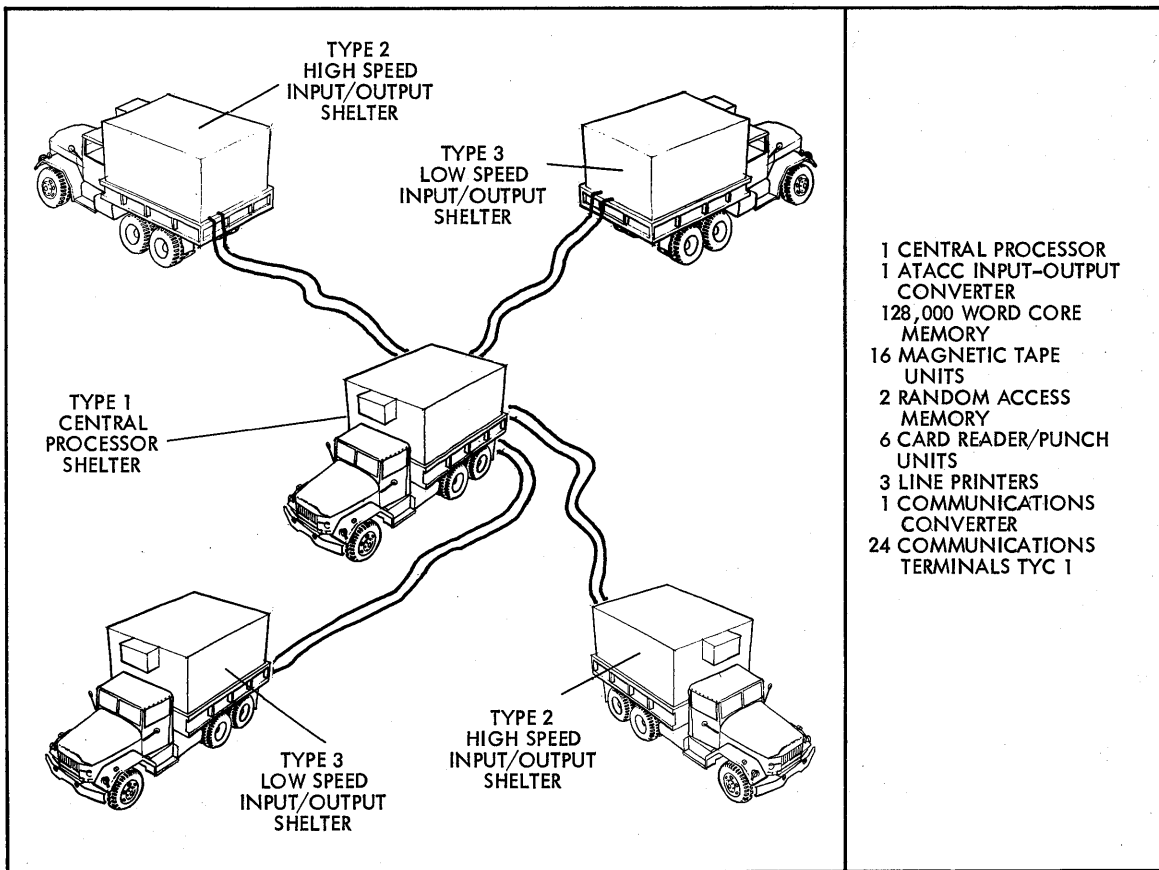


Figure 1-3. ATACC Low-Speed Input/Output Device Shelter (Type 3 Shelter)



A TYPICAL ATACC CONFIGURATION FOR BATTALION USE



A TYPICAL ATACC CONFIGURATION FOR FIELD ARMY USE

Figure 1-4. ATACC Configurations for Battalion and Field Army Use

TABLE 1-1. ATACC SHELTERS

Shelter Type	Function	Relay Rack Allocation							
		1	2	3	4	5	6	7	8
1	Central Processor Shelter	Console	Central Processor Plus ATACC In/Out Converter	Core Memory Unit 16,000 <u>or</u> 32,000 Words	Core Memory Unit 16,000 <u>or</u> 32,000 Words <u>or</u> 2 Mag Tape Units <u>or</u> 1 Card R/P	Core Memory Unit 16,000 <u>or</u> 32,000 Words <u>or</u> 2 Mag Tape Units <u>or</u> 1 Card R/P	Core Memory Unit 16,000 <u>or</u> 32,000 Words <u>or</u> 2 Mag Tape Units <u>or</u> 1 Card R/P	Communications Converter Plus 24 Channel TYC-1	Storage and Paper Tape Set
2	High Speed Input/Output Shelter	2 Mag Tape Units <u>or</u> 1 Random Access Memory	2 Mag Tape Units <u>or</u> 1 Random Access Memory	2 Mag Tape Units <u>or</u> 1 Random Access Memory	2 Mag Tape Units <u>or</u> 1 Random Access Memory	2 Mag Tape Units <u>or</u> 1 Random Access Memory	2 Mag Tape Units <u>or</u> 1 Random Access Memory	MTU Device Switching Units Plus Auxiliary Console Plus Storage	Storage
3	Low Speed Input/Output Shelter	1 Card R/P <u>or</u> 1 Line Printer	1 Card R/P <u>or</u> 1 Line Printer	1 Card R/P <u>or</u> 1 Line Printer	1 Card R/P <u>or</u> 1 Line Printer	1 Card R/P <u>or</u> 1 Line Printer	1 Card R/P <u>or</u> 1 Line Printer	Auxiliary Console Plus Storage	Storage

illustrated, this complement is two magnetic tape units and one random access memory file. The selection could just as well have been one of six magnetic tape units, or it could have consisted of two magnetic tape units and a line printer. Another possibility would be one card reader/punch and a line printer.

At the bottom of the page, the same Type 1 shelter forms the heart of a greatly expanded configuration suitable for Army-level use. Here the input/output devices are located in additional shelters and the core memory is implemented to the maximum capability of the Type 1 shelter, or 128,000 words.

The full input/output capability of the ATACC computer is sufficient to meet all Army needs. As shown, the attachment of two Type 2 shelters and two Type 3 shelters permits a configuration of sixteen magnetic tape units and two random access memory files. But because of the modularity, each group of four magnetic tape units is interchangeable with a random access memory file, so either six files or twenty-four magnetic tape units or any other combination of the two types of unit can be achieved. In a similar way, the two Type 3 shelters show a configuration of six card reader/punch units and three line printers, but again the inherent modularity of the design permits the interchange of each group of two card reader/punch units with one line printer. Thus, the figure shown could easily have been twelve card reader/punch units or six line printers or any combination of the two.

1.3 ATACC DATA PROCESSING UNITS

The individual units of the ATACC family will be described at the end of this document, but a brief description follows.

The ATACC Central Processor – The Central Processor is constructed of high density cordwood stick packages of the type developed for use in the AN/MPQ-32 computer. It occupies a single drawer, filling half of a standard 19-inch relay rack. It is capable of implementing the full Fieldata instruction code repertoire of up to 64 instructions at double the speed of MOBIDIC. By means of a compatibility switch, it can handle 28,000 words of memory and all existing MOBIDIC object, assembly, and compiler programs without modification, or new programs to take advantage of the new features, including up to 128,000 words of memory in the new configuration. It contains seven index registers, a real-time clock, an expanded program interrupt capability, and an increased capability for partial word or character operations.

The ATACC Core Memory—The memory has a repetitive random access time of two microseconds and is implemented in 16,000-word modules, each of which occupies one-half of a standard 19-inch relay rack. The memory is expandable in 16,000-word increments up to a logical maximum of 128,000 which words can be housed in the Central Processor shelter.

The ATACC Input/Output Converter—The converter is almost identical to the Central Processor in size, shape and basic construction. It contains provisions for both on-line and off-line input/output control. Utilizing advanced control features for simultaneous control of several input/output devices, it contains four separate input/output bus terminations, three for high-speed devices like magnetic tape units or random access memory disc files, and one for low-speed devices such as card units, line printers, or paper tape sets. The complete number of devices in any configuration (up to a maximum of 64) can be controlled from each bus line, with any four devices operating at once. A second Input/Output converter can be provided for exclusive off-line use.

The ATACC Console—The Console is improved and simplified as compared to its MOBIDIC predecessor and contains provisions for Arabic display of numeric data. Auxiliary control panels permit ease in simultaneous on-line and off-line operation and also facilitate control from the various shelters.

The ATACC Communications Converter—The converter contains provisions for real-time connection between the Central Processor and up to thirty-two communications channels. It is constructed of the same basic circuit packages as the other electronic equipment, and is housed together with twenty-four channels of TYC-1 communications terminal equipment in one relay rack.

The Magnetic Tape Transports (Model MT-452)—The transports are those developed by Sylvania under Signal Corps Contract No. DA36-039-sc-90832. Like all of the other equipment in the ATACC family, they are fully militarized. Two tape units with their common pneumatic air source mount in a single relay rack. This dual speed magnetic tape unit, cartridge-loaded, can operate at a normal data rate of 45,000 characters per second, utilizing a fourteen-channel data format which provides Hamming Code error correction. Packing density is 450 bits/inch and by means of a small field-change conversion kit, a low-speed operation of 300 characters per second can be achieved. Cartridge data capacity is over five million characters and start-stop time is three milliseconds.

The ATACC Random Access Memory—The disc file unit is housed complete with all electronics, including its Direct Switching Unit, in a dual relay rack. The memory is especially organized to store both data and programs, and has a storage capacity of over 18 million characters with an average access time of 8.6 milliseconds and a read/write rate of 105,000 characters per second.

The ATACC Card Reader/Punch—This unit is a rack-mounted card processing unit operating at rates in excess of 800 cards/minute read and 250 cards/minute punch. Fully militarized, it mounts, together with all electronics, including its Direct Switching Unit, in a single relay rack.

The ATACC Line Printer—The printer is a high-speed line-at-a-time page printer capable of speeds of 600 lines per minute and 120 characters per line. It mounts with all electronics, including its Direct Switching Unit, in a dual relay rack.

1.4 ATACC SUMMARY CHARACTERISTICS

The equipment described in the preceding sections have the following overall characteristics and specifications:

COMPUTER SPECIFICATIONS

Mode of Operation	Parallel
Internal Number System	Binary
Word Length	38 Bits
Timing	Synchronous
Arithmetic System	Fixed Point Magnitude and Sign
Indexing	7 Index Registers, 17 Bits each
Clock Rate	2 Megacycles

TYPICAL INSTRUCTION TIMES

Transfer Control	4 Microseconds
Clear and Add	8 Microseconds
Add	8 Microseconds
Subtract	8 Microseconds
Multiply	46 Microseconds
Divide	48 Microseconds

CORE MEMORY

Type	Coincident Current Magnetic Core
Repetitive Random Access Time	2 Microseconds
Storage Capacity	128,000 Words
Module Size	16,000 Words

INPUT/OUTPUT CAPABILITY

Combined on-line and off-line control	
Total Number of Channels	3 High-Speed, 1 Low-Speed
Maximum Number of Devices	63

INPUT/OUTPUT SPEEDS

Magnetic Tape	45,000 characters/second
Random Access Memory	105,000 characters/second
Disc File	
Card Reader/Punch:	
Read	800 cards/minute
Punch	250 cards/minute
Line Printer	600 lines/minute
	120 characters/line
Paper Tape Reader/Punch:	
Read	300 characters/second
Punch	100 characters/second

SECTION II

COMPUTER APPLICATION

2.1 FUNCTION

Strikingly similar data processing functions must be performed at all echelons of command in the present Army Command and Control Applications of fire support, intelligence, personnel and administration, and logistics. These functions are:

1. Simultaneously receive reports from many sources.
2. Update local files.
3. Transmit details or summaries to other echelons.
4. Receive both occasional and periodic queries from many sources.
5. Search local files.
6. Retransmit queries to other echelons.
7. Receive responses from other echelons.
8. Batch with local file responses.
9. Sequence and edit as directed by requestor.
10. Transmit for remote or local display.

To show these functions being performed repeatedly in various operations, a few examples will be helpful.

In a fire control application observers transmit reports to their battalion commander. These reports affect local files (ammunition, target assignment completion, etc.) and are also transmitted to division artillery fire direction, fire support coordination and/or survey information centers.

Intelligence queries are routed similarly. The command which is queried, must respond with data from its files and also transmit queries to other possible sources. The transmitted responses must be sequenced and output to the requestor by original command queried.

The personnel and administration application also requires transmission of updating messages to division, army and central personnel files as well as advising prospective commanders on reassignments, orders and personnel status.

In a typical logistics application, MILSTRIP requires that requisitions drawn on combat service support units be filled if possible, otherwise routed to field army support commands, and if necessary, further routed to oversea supply agencies.

2.2 SCALE

Army applications have a wide range of data urgency and volume at every command echelon.

For example:

Fire support requires reaction times ranging from a few seconds at Battalion level to a minute or more per report at Division level.

Stock control centers under MILSTRIP may have daily processing cycles but must handle tens of thousands of requisitions against hundreds of thousands of file items.

Personnel records tend to increase in volume at higher echelons for this data must be maintained on an individual basis. At the same time, records may be urgently required at an immediate command level, but only required for historical purposes at higher echelons.

2.2.1 Equipment Scale

The term "scale" has been applied to individual major units within configurations. Different computers in the same family may be designated as "small," "medium" and "large-scale" computers because they have different operating speeds and instruction sets.

However, experience has shown that decoding slightly fewer instructions or operating at slightly different rates has very little if any effect on cost. But, unless the designers always keep modularity as a design goal, the resulting units may become completely incompatible as units and systems. Often, different

computers in the same family cannot use the same programs even though the instructions have identical octal values, because the results are not the same. Memory locations of one computer may have special uses; another computer may use the same locations for general storage. Central Processors, memory modules, input/output converters, communication converters and some devices cannot be physically interchanged.

Incompatibility can be tolerated in a fixed-plant, commercial environment. Programmers can be re-instructed, programs may be altered leisurely, and compatibility black boxes can be designed and attached to make the equipment successfully simulate a different version. Incompatibility cannot be tolerated in a military environment. Combatant or support personnel do not have computer design engineering skills nor access to the special parts and equipment required. Equipment cannot be "off the air" with corresponding degradation in the state of the files. Programs cannot be changed leisurely. Furthermore, logistics commands can not be forced to carry different high value items whose performance differences cannot be economically justified.

The concept of "scale," applied to individual major units necessarily results in physical, procedural and data incompatibilities which cannot be tolerated in tactical environments nor even economically justified in non-tactical environments.

2.2.2 Configuration Scale

Scale can be meaningfully applied to equipment configurations—a computer with only paper tape equipment is "small scale," one with mass memory, several magnetic tapes and a variety of other peripheral equipment both on-line and off-line is logically called "large scale." For "scale," in this sense, classifies systems by the amount of work they can do in a given time—and time in Command and Control applications is related more to the number and types of input/output devices and storage units controllable than by the speed or repertoire of a Central Processor.

Since every Command and Control application requires simultaneous input and output and may require "off-line" processing as well, a multiple

simultaneous device controller allows complete freedom in device selection and operating mode to meet specific application requirements. Although there is little cost difference between a multiple, simultaneous device controller and a single device-at-a-time controller, there is a definite cost advantage in a multiple, simultaneous device controller over the cost of two or more Input-Output Controllers.

2.2.3 Equipment Conclusions

The above application summary indicates the need for a Control Processor, which is small and inexpensive enough for small scale applications, yet powerful enough for large scale applications. The ATACC computer specifications have been finalized with this in mind. The implementation of multiple input/output device control in a single input/output converter is another feature of the ATACC computer which enables efficient application to data processing problems at all echelons.

2.3 EQUIPMENT SELECTION

ATACC equipments have been designed to perform all the functions required, and to allow configurations to suit the wide scale of any applications. Either batch or in-line processing may be required for these applications. Selection of equipment for any one application or echelon involves determining the acceptable processing mode, file data quantity and response time.

2.3.1 Batch Processing

Batch processing is necessary when the primary mission of an echelon is evaluation over a relatively long period of time—monthly, quarterly, or annually. Configurations suitable for such work would use one or two core memory modules, ten to twelve tape units, two card readers and two to four printers. Magnetic tape provides the only unlimited file and program storage medium. The application programs would include "off-line" conversion of paper tape, cards or shipped magnetic tape input to a local standard magnetic tape format, extensive tape processing, and finally "off-line" conversion to printed reports, cards or paper tape.

2.3.2 In-Line Processing

In-line processing is required when an echelon is directly supporting a combat organization where "real-time" response is necessary. All the functions listed in paragraph 2.1 must be performed and overlapped, to minimize elapsed time for any individual input. For very fast response systems, all programs and data would be stored in two or more core memory modules; all communication converter channels would be used, and only two magnetic tape units for historical recording and program and data security would be required. Such a system would have a response cycle time of a few milliseconds. Intermediate speed response systems would replace core modules with several disc files. Slower real-time systems could then use a single disc file with two additional magnetic tapes for overflow or slower response files.

SECTION III

DESCRIPTION OF ATACC UNITS

3.1 BASIC COMPUTER SHELTER AND MAIN FRAME

The main computer shelter comes equipped with a Main Frame with alternatives for layout of the balance of the shelter. A typical installation is shown in Figure 3-1.

3.1.1 ATACC Main Frame

Figure 3-2 shows a block diagram of the ATACC Main Frame with the optional Communications Converter and Memories. The Central Processor (CP), Input/Output Converter (IOC) and Communications Converter (CC) share high speed buses for Memory Input/Output, Memory Addressing and Control. This gives all units direct access to memory, without interfering with the inner workings of each other.

3.1.1.1 Central Processor (CP)

Central Processor (Figure 3-3) is contained in a single slide-mounted drawer. Two such drawers, each housing approximately 1200 sticks can be mounted in one 19-inch relay rack. The power supplies are mounted externally. The total volume of the Central Processor is 5.95 cubic feet and the weight is 250 pounds. The overall dimensions, in inches, are approximately 8 wide by 23 deep by 56 high.

The Central Processor is the heart of the ATACC system, performing all arithmetic and logical operations, and initiating the transmission and reception of data from the Input/Output and Communications Converters. In addition, it contains the priority logic necessary to assign the memories to itself or to either of the two converters.

The ATACC Central Processor implements instructions of a modified Fielddata repertoire with up to 128,000 words of memory, or by means of a compatibility switch, can implement the standard MOBIDIC repertoire with up to 28,000 words. It is worthwhile to review the important features here. First, an

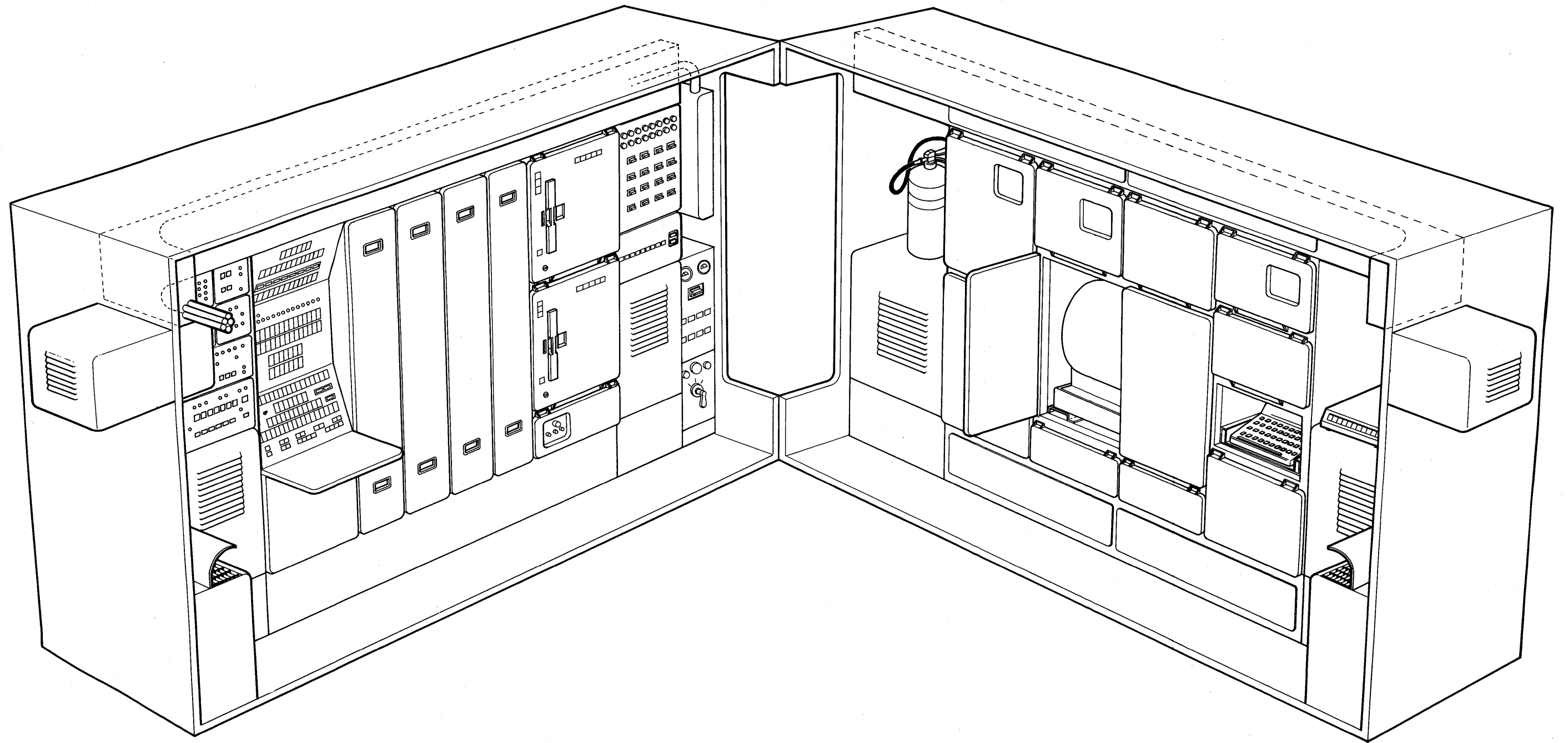


Figure 3-1. The Central Processor Shelter in an exploded view showing a typical configuration with 32,000 words of high-speed core memory, 2 magnetic tape transports, communications control for 24 channels, a random access memory disc file and a paper tape set.

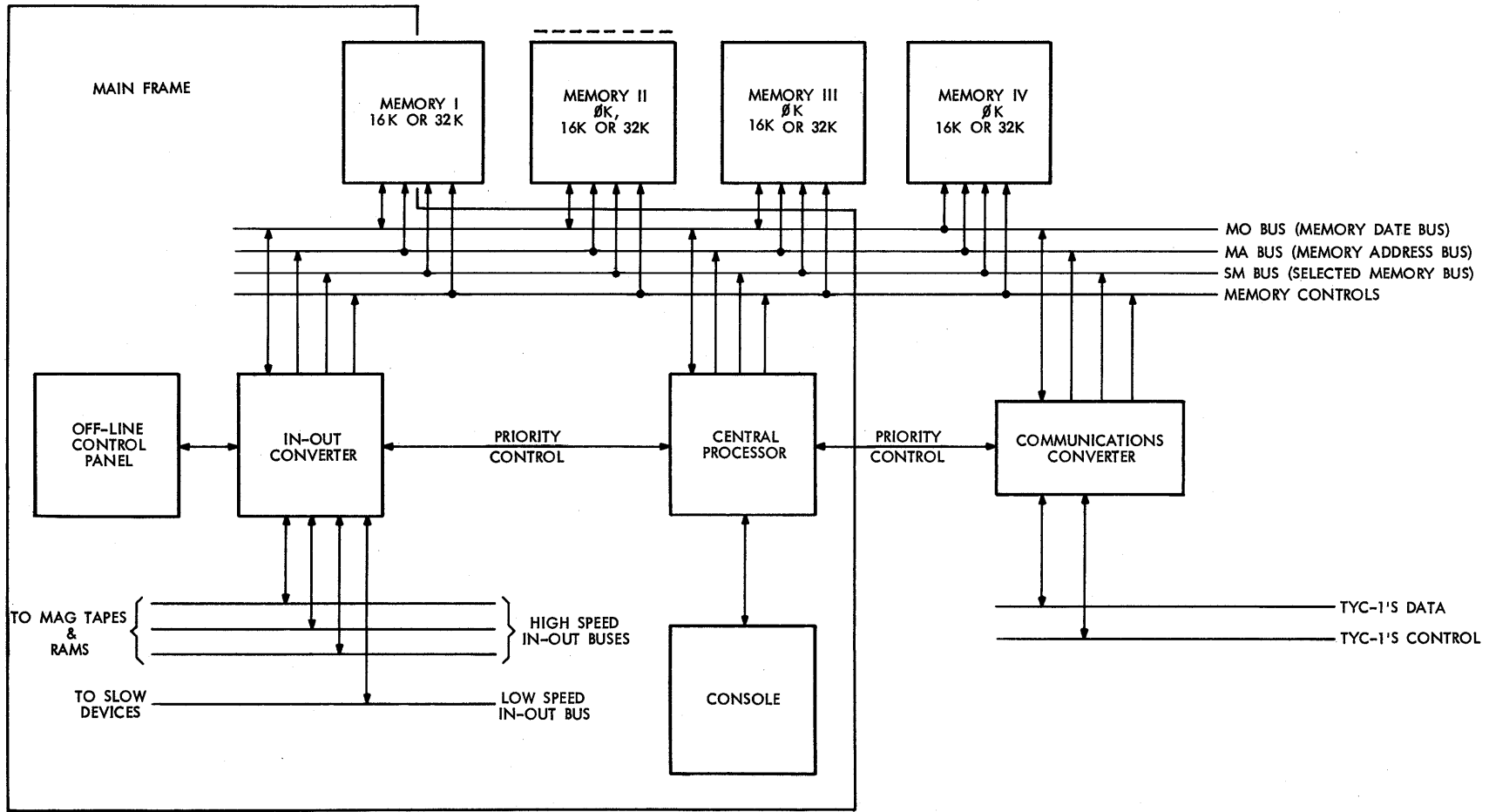


Figure 3-2. ATACC Computer Block Diagram (Main Frame and Communications Converter)

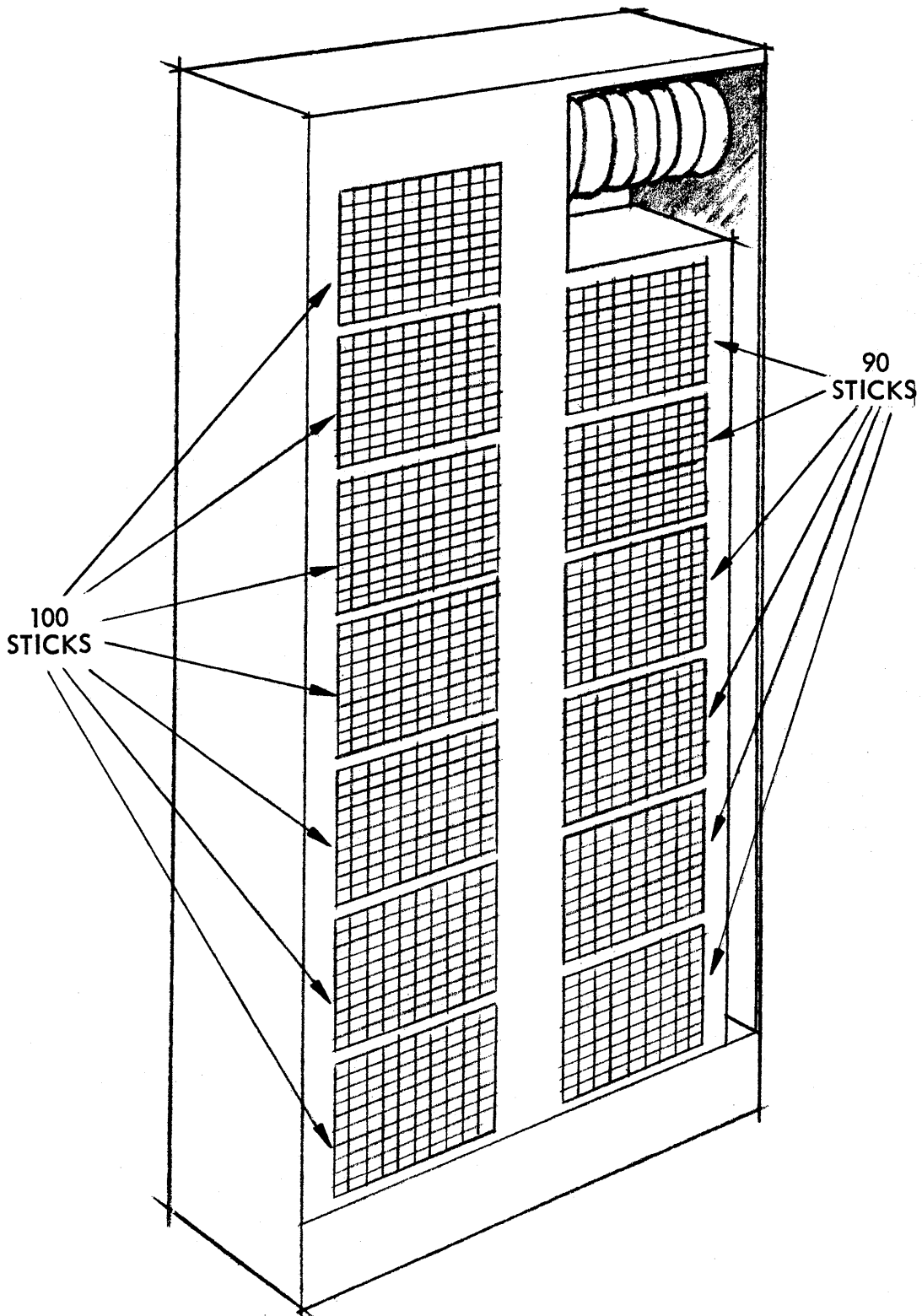


Figure 3-3. Central Processor Drawer

18 bit alpha field is used, which allows addressing up to 128,000 words of memory continuously with 17 bits, with the 18th bit used to indicate addressable registers. Second, Input/Output is handled through an order-sequence mode with the ATACC Input/Output Converter, rather than by direct Input/Output instructions. Third, a shift option is available with all arithmetic instructions. This has the effect of combining two instructions into one, with a saving of five percent in program memory locations. Another feature is a much more flexible program interrupt system, giving the program greater control over priorities.

The ATACC Central Processor represents a significant product improvement of MOBIDIC. It uses the same proven circuits, but is twice as fast, considerably smaller, and uses fewer components. The speed improvement is brought about by a faster clock and memory. The circuits have always been capable of speeds much greater than those encountered in MOBIDIC, but memory speed and long wiring have limited their application. Both the Sylvania 9400 and the AN/MPQ-32 Computer use the same circuits with a four microsecond memory, and the AN/MPQ-32 uses cordwood miniature packaging, identical in nature with that of ATACC, thus reducing wiring lengths.

3. 1. 1. 2 Input/Output Converter (IOC)

The ATACC Input/Output Converter is an autonomous processor which accepts input and output instructions from the CP or the Off-Line Control Panel, and controls device operation and data flow to and from memory. It performs all timing and synchronizing functions necessary to operate the devices, interrupting the Central Processor only upon completion of an operation or to gain access to the memory. The IOC is housed together with its power supplies in a single drawer, as shown in Figure 3-4. There are approximately 900 stick positions available in the drawer, of which about 800 are used. The power supplies are mounted on heat sinks directly on the air plenum, and are cooled by exhaust air from the sticks. The Central Processor and the Input/Output Converter occupy a single relay rack.

The ATACC Input/Output Converter represents a product improvement well suited to satisfy the Army's input/output and off-line requirements. Sylvania's examination of the Army's application requirements shows that applications as low as battalion level require at least two input/output channels, while

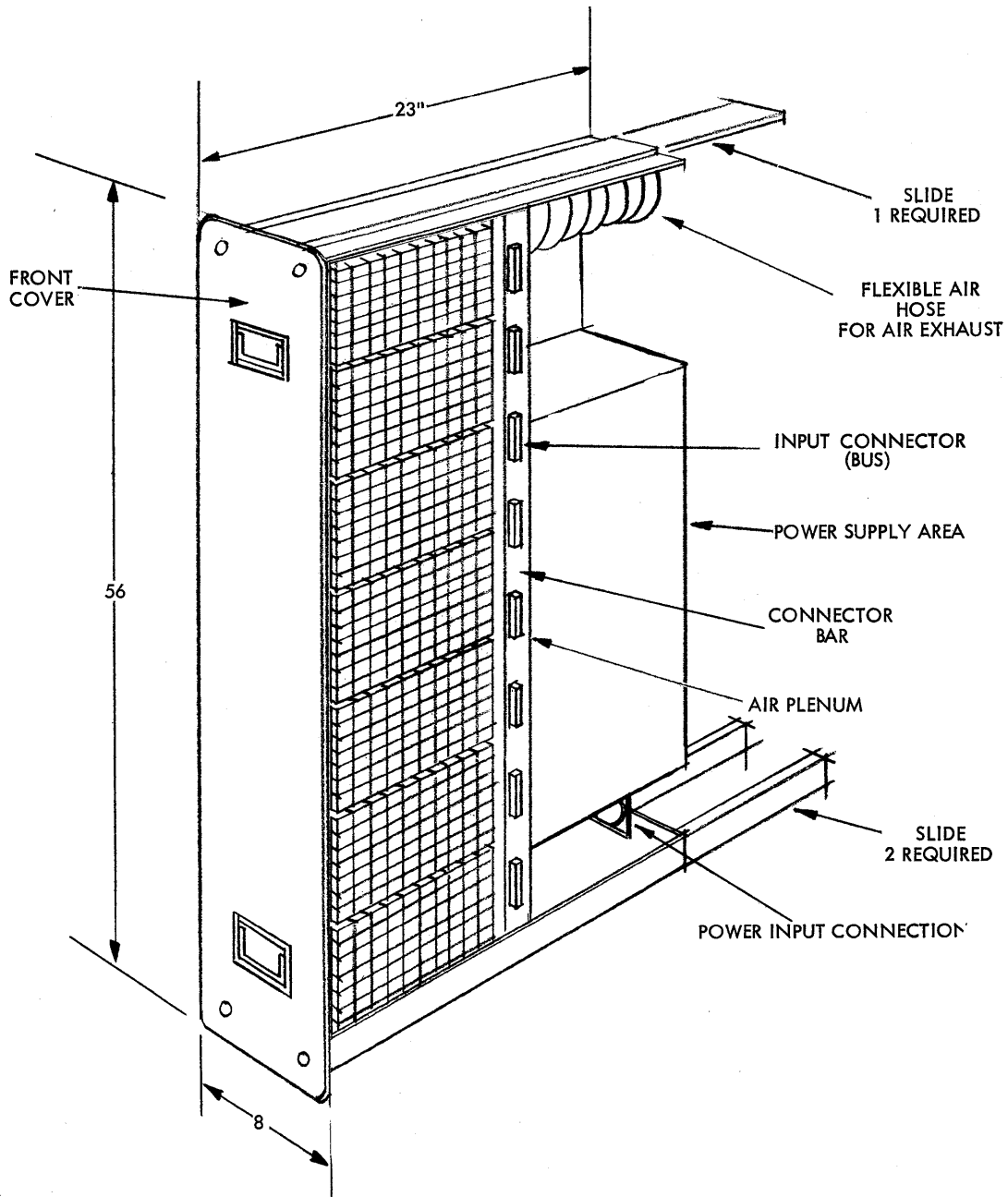


Figure 3-4. Input/Output Converter Drawer

those at army level require three high-speed and one multiplexed low-speed channels, with provisions for switching between on-line and off-line.

The ATACC IOC has the flexibility required at army level, but uses fewer components than two, single channel, MOBIDIC Input/Output Converters. Therefore, it is equally adaptable, without being unduly expensive, for battalion level applications.

This notable improvement of the Input/Output Converter has come about through Sylvania's experience in using MOBIDIC, and in subsequent computer designs. Through the use of high-speed core memory registers for instruction and device control word storage, transistor registers are eliminated, cutting the size drastically. This technique has been applied successfully on the AN/MPQ-32 computers. In addition, on the Sylvania 9400 computer, the capabilities of the input/output system were expanded by permitting the IOC to gain access to input/output orders which are stored sequentially in memory, a feature which is also included in the ATACC IOC.

One further improvement of the MOBIDIC input/output system is the separation of the four ATACC Input/Output channels into one low-speed channel, for paper tape, card equipment and printers; and three high-speed channels, for magnetic tapes and random access memories. On MOBIDIC, a device, no matter what its speed, demands a bus full time for the duration of an instruction, even though the actual data transmission takes a very small percentage of the instruction time. An example of this might be a paper tape punch instruction of sixty characters, which takes approximately one second to complete, in MOBIDIC although the data transmission for this instruction takes only 0.0006 seconds in a typical application.

The ATACC IOC takes advantage of the great disparity between instruction time and data transmission time by employing a lock-out technique on the slow-speed bus. (It should be noted here that the name "slow-speed" applies only to the devices attached to the bus, not to its data transmission capability). That is, a device is started and a character is sent (or received). The device then processes the character while other devices are serviced by the bus. When the first device signals that it is ready, the IOC dispatches another character. Thus several, slow-speed devices are operated simultaneously by the one bus.

In the case of the high-speed buses, no lock-out technique is necessary since the data rate capability of the bus and the device rate are more nearly matched. Complete lock-on is therefore provided for the magnetic tapes and random access memories.

With the three improvements noted above, the ATACC IOC is capable of operating three high-speed and up to five low-speed devices simultaneously, in any combination of on-line and off-line operation. Combined operation is made possible by an off-line console from which instructions may be entered and initiated.

The IOC will process such instructions intermixed with on-line instructions. To prevent an unauthorized off-line use of a device, a switch on each device-status panel reserves its associated device for on-line use.

3. 1. 1. 3 Core Memory

This memory is a 16,000-word, two microsecond coincident current core memory, complete with its own data and address registers. The memory is used to store data, instructions, as well as special buffer and control words for the two converters. In addition, this memory unit is able to count in certain fields of its Data Register. This feature is used as part of the Input/Output Control.

The basic memory is housed in a single drawer (Figure 3-5) containing 590 sticks and 28 printed circuit packages. This drawer is the same overall size as the CP and IOC drawers.

The printed circuit packages contain power transistors and their associated components which are too large for stick packages. The card is approximately 6-inches by 6-inches, with a wall connector and a test point block. Cards are housed in three bays and are cooled by air, from metered orifices on the side of the drawer, which passes down over the cards and is exhausted into the air plenum. The memory arrays are located relative to the sticks to minimize interconnecting wire lengths.

TYPE II

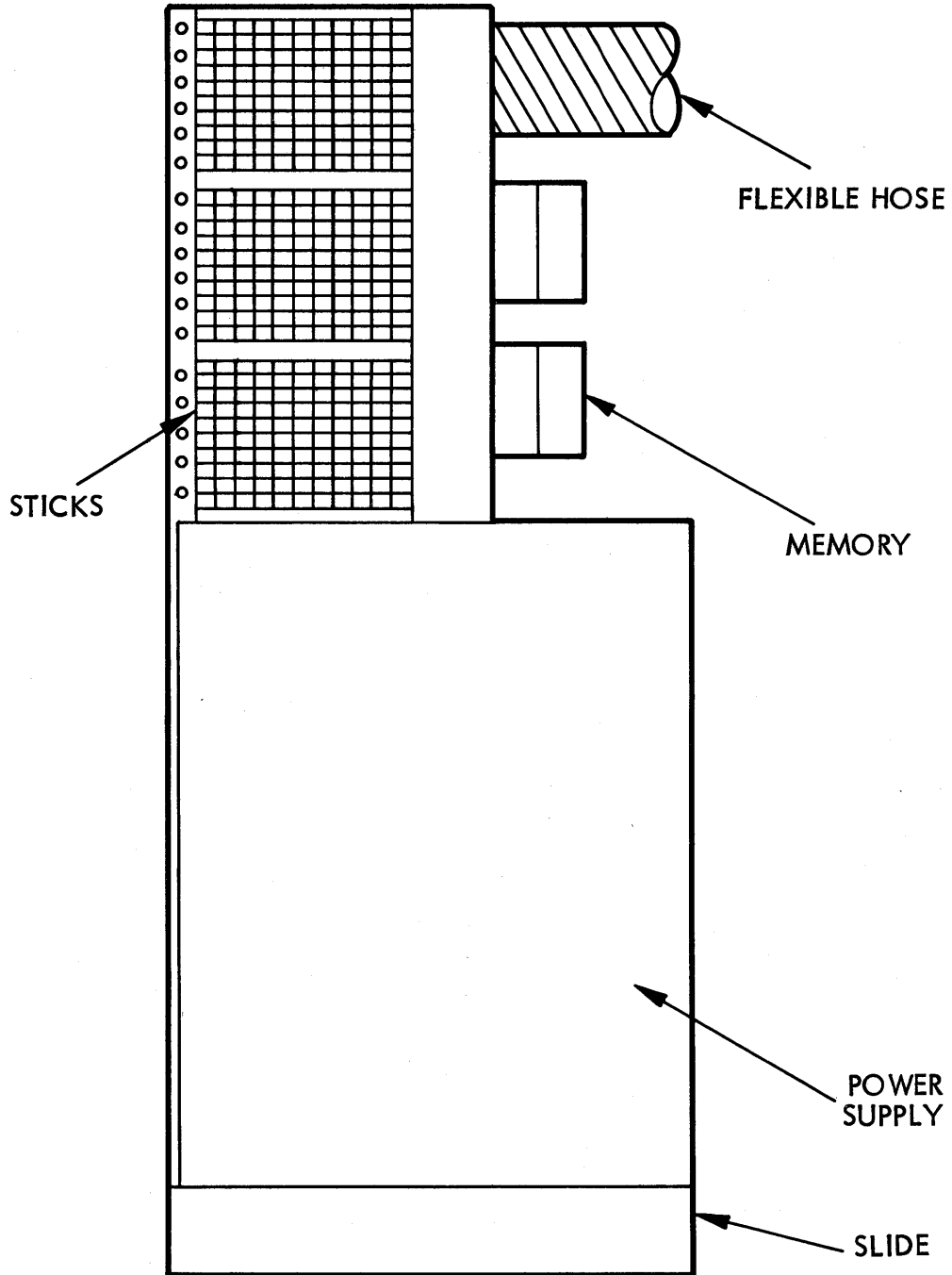


Figure 3-5. Basic 16,000 Word Memory Drawer

3. 1. 1. 4 Console

The console (Figure 3-6) occupies a single rack, and is operational center for the ATACC Computer. The rack contains all the switches and indicators required for efficient control of computer operation by operating and maintenance personnel.

The main controls and switch registers are located on a central panel. These include: the Address Switch Register, for selection of starting addresses or addresses for manual operation; the Word Switch Register, for entering data or instructions, Sense flip-flop switches and mode selection and initiation controls. Above the controls are operational displays, Nixie display registers for the Program Counter, the combined X, G and IR registers, and the MO Bus. The last display has a bank of register selection switches. The bottom of the rack contains power supplies for the Central Processor.

The console retains all of the desirable features of the MOBIDIC console, but packages them more compactly and presents them in a more easily comprehensible form. Human engineering principles have been applied in its layout.

In addition to the console, a number of other control panels are available for use in the ATACC system. These include an off-line control panel and auxiliary computer and off-line control panels. The off-line control panel is located in the CP shelter, adjacent to the console and is used to read-in and perform off-line peripheral device programs, simultaneous with computer operation, while the auxiliary panels are located in peripheral shelters.

3. 1. 2 Central Processor Shelter

Figure 3-1 depicts a cut-away view of the interior of the Central Processor shelter.

The console is located away from the shelter door, so that the operator will not be disturbed by personnel entering the shelter. The central processor power supply is mounted in the lower portion of the Console. The Central Processor and In-out Converter drawers, mounted beside the console, are placed together and adjacent to the console to reduce the lead length of the connections between them.

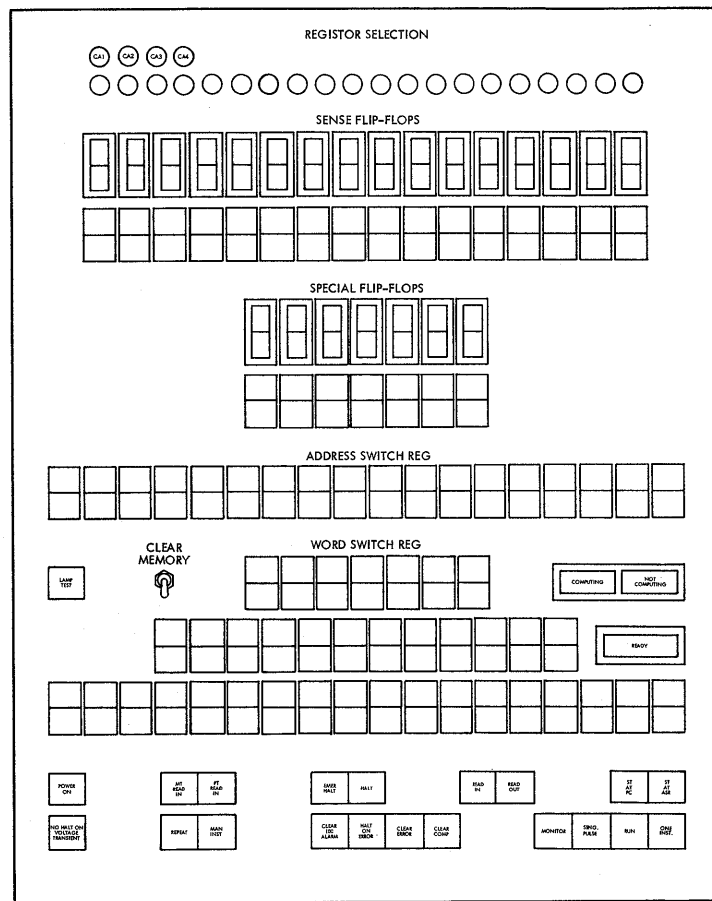
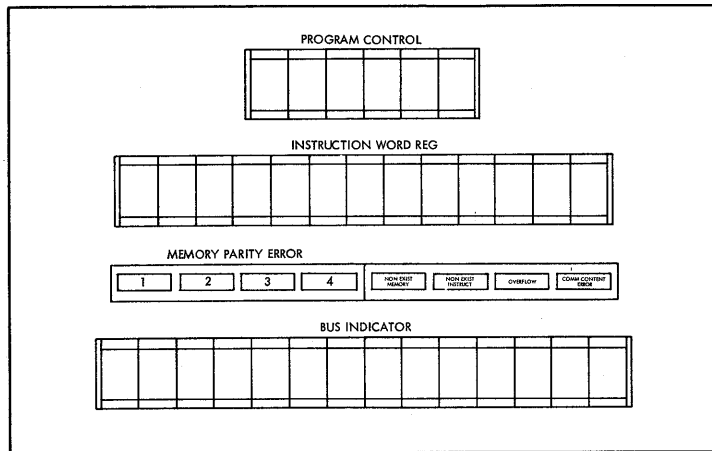


Figure 3-6. Console Panel

The Communications Converter and Communication Terminal Equipment are mounted adjacent to the shelter Digital Data Terminal input connector panel, also reducing the routing problem of the interconnecting cables.

The Paper Tape unit is located across the aisle from the Console, which places it in a convenient location for the operator.

The remaining locations contain terminations for all the memory buses, High-Speed In/Out Bus, Low-Speed Input Bus and Low-Speed Output Bus. A number of variations of memory, and low-speed and high-speed devices can be added to this basic installation to fill the five remaining equipment mounting locations.

A mounting member is provided in the space between the air intake and air exhaust duct adjacent to the Console. The Off-Line Control Panel and the Basic Shelter Device Panel are mounted in this space. Additional space is available on this structure to mount up to two High-Speed Shelter Device Status Panels and two Low-Speed Shelter Device Status Panels. These panels are added to the system as additional peripheral shelters are added, and are discussed in paragraph 3. 10.

Additional panel mounting space is provided next to the mounting area between the air intake and exhaust duct for the A-C Computer Control and Distribution Panel.

A Power Input Control Panel is located at the rear curbside wall. This panel contains the main circuit breaker for the shelter and the branch circuit breakers for the shelter equipment (air conditioner, heater, convenience outlets, lights, etc.). Mounted on a panel below the power input Control Panel are a 200-ampere rotary switch, phase sequence indicators and, a frequency meter, which allow the selection of one power line from two power sources. Power is distributed from this panel to the A-C Control and Distribution Panel and to four power receptacles mounted on the shelter rear wall. These four receptacles provide a power source for up to four additional device shelters.

The areas over the air intake duct adjacent to the Paper Tape Unit contain an intercommunications station and storage space. This places the station at the operator area. A fire extinguisher and storage space are also provided in the area over the air intake duct adjacent to the Communication Converter.

The inside of the door holds an auger type ground stake and a 25-foot ground cable. This door is also provided with a black-out curtain. The shelter floor provides storage space for two, 25-foot prime power cables.

Located on the external rear walls are the inter-shelter cable termination panels. The curbside wall contains a panel for two power connectors from two power sources and a ground stake lug, a panel for power distribution to four additional shelters, a panel for in/out buses and control connections for two High-Speed Device Shelters and a panel for In-Out Buses and Control connections for two Low-Speed Device Shelters. The roadside wall contains three panels each providing connections for four master stations and special four connector and binding posts for eight pair of telephone lines.

3. 1. 3 High-Speed Input/Output Shelter

The High-Speed Input/Output Shelter contains the same type of modifications as the basic shelter, but is simpler in the type of equipment which it may contain. Table 1-1 gave the alternatives available in this shelter.

Equipment mounting locations contain all prime power connections and High-Speed Bus outlets necessary to operate either magnetic tape units or random access memories. In addition to the devices, this shelter contains an Auxiliary Control Panel for both on-line and off-line operations, which will enable the operator, after having set up the main console, to initiate processing from the device shelter.

Intershelter cable termination panels are comprised of a panel provided with one prime power connector and ground stake lug, a panel provided with high-speed in/out bus terminations and a communications panel containing terminations for one intercommunication master station and eight pair of telephone lines.

Intershelter High-Speed Input/Output Cables, Control Cables and one prime power cable, are stored on the shelter floor while in transit.

3. 1. 4 Low-Speed Input/Output Shelter

This shelter is essentially the same as the High-Speed Shelter, with the exception of the devices mounted in it. Alternate equipment selections for this

shelter are also shown in Table 1-1. Auxiliary Control Panels are located in this shelter for the operator's convenience.

3.2 MEMORY SUPPLEMENT

The Memory Supplement provides a 16,000 word add-on capability to the basic memory. It shares the Data Register and the Address Register of the basic memory, replaces the power supply drawer of the basic memory, and contains power supplies adequate for the combined 32,000 words. The two together occupy a single rack. The Memory Supplement occupies a drawer, (Figure 3-7), similar to the basic memory, and is the same overall size; it contains 400 sticks, and 16 printed circuit cards. The method of cooling is identical to that of the Basic Memory.

3.3 COMMUNICATION CONVERTER

The Communication Converter fulfills a function very similar to the IOC. It is an autonomous processor which accepts input and output instructions from the CP and controls data flow to and from as many as 32 TYC-1, two-way data terminal equipments. All timing and synchronizing functions are performed by the Converter, and the CP is interrupted only for access to memory, or upon completion of an operation. Unlike the IOC, the Communication Converter is an optional piece of equipment.

The Communication Converter is housed in a slide-mounted drawer (Figure 3-8) containing approximately 200 sticks and power supplies, mounted on a hinged plate which allows access to the next wiring. The drawer is supported by two slides which will properly support the load and provide ease in inserting and withdrawing the drawer; both power supply and sticks are accessible when the drawer is open.

The Communication Converter is discussed fully in Appendix A.

TYPE I

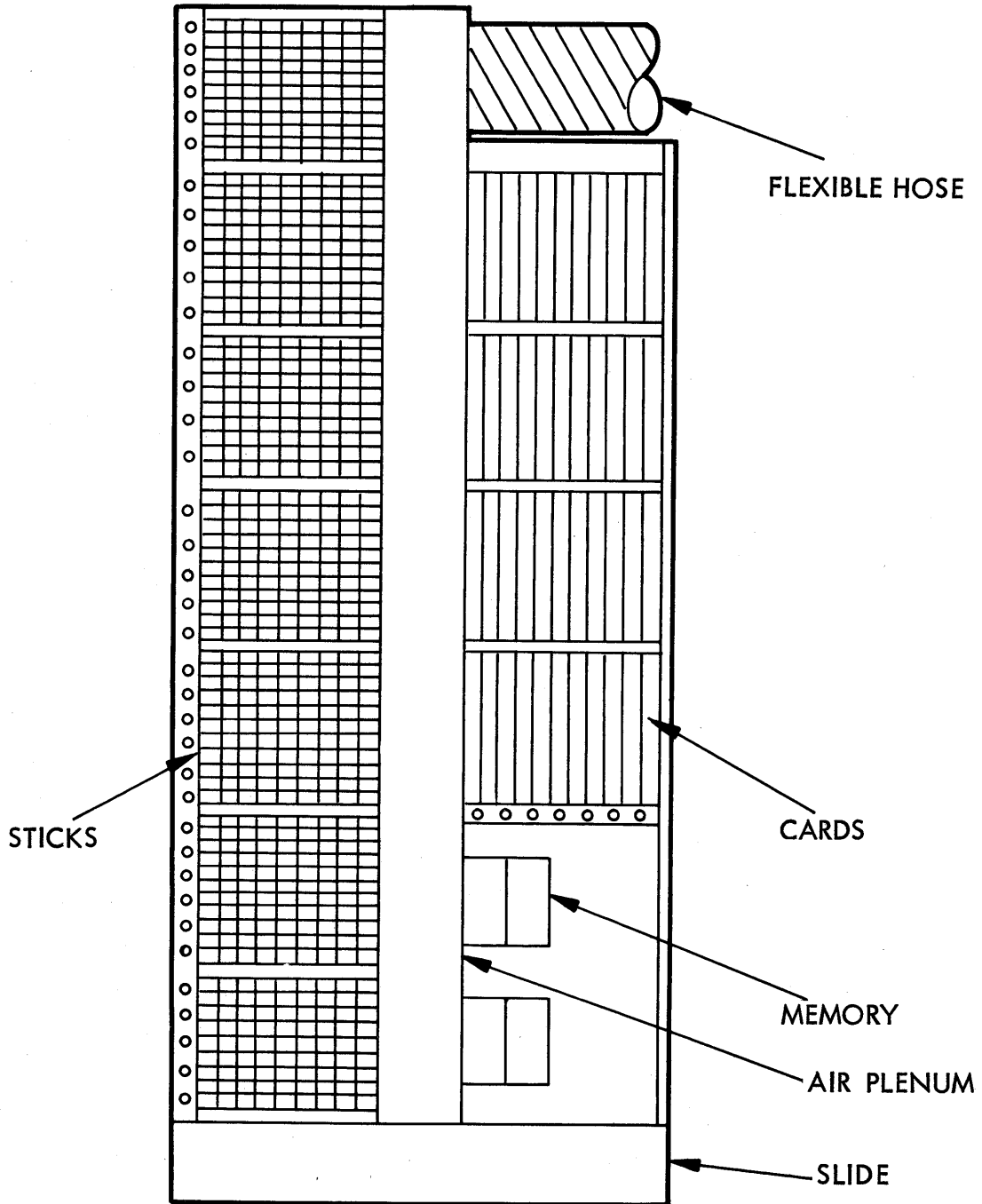


Figure 3-7. Memory Supplement Drawer

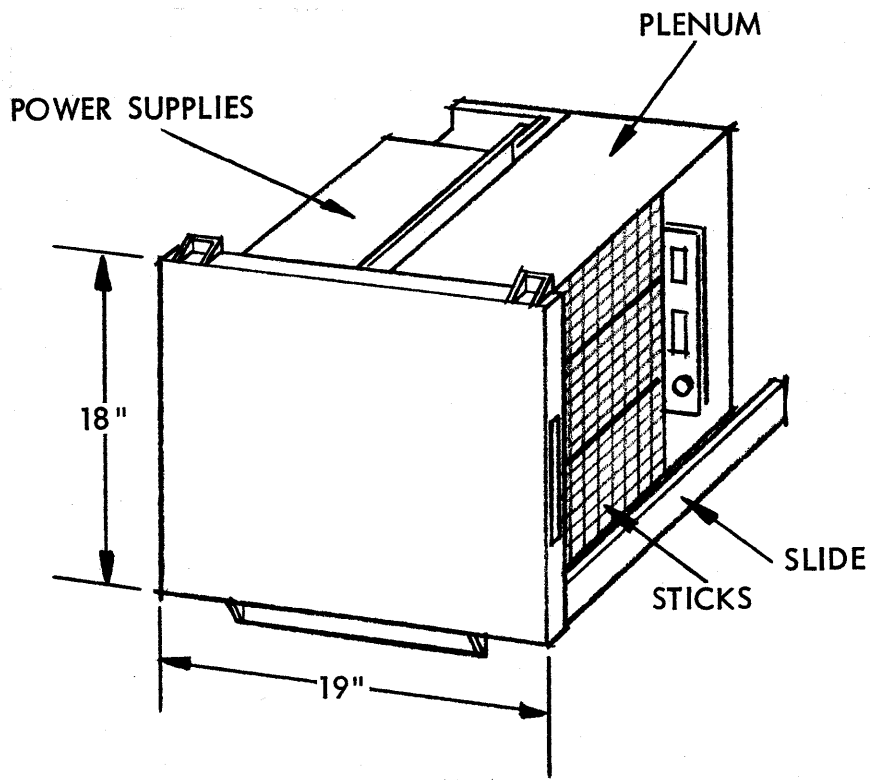


Figure 3-8. Communications Converter Drawer

3.4 MILITARIZED FIELDATA DIGITAL MAGNETIC TAPE TRANSPORT

3.4.1 General Characteristics

The Sylvania MT-452 is a compact, rugged, digital magnetic tape handler developed specifically for the Army Fieldata program and later generation military data processing systems. It meets all requirements of SCL-4310A. Its design stresses preservation of data and storage medium in military field environments through advanced techniques in systems logic and in the dynamics of tape guidance and control. The tape handler offers an unique combination of design features including fully automatic tape-cartridge loading and pneumatic tape drive, a proportional reel servo with applied fiber-optics, Sylvania 3-D stick electronics with Hamming Code error-correction logic and, for the first time in a single machine, data transfer rates for both computer and data terminal applications.

Magazine loading and automatic threading eliminates all human contact with the tape and thereby removes a principal cause of tape contamination. The operator-effort in loading, unloading, and threading is reduced to the removal of one cartridge and the easy insertion of another. The machine performs all associated functions automatically.

The pneumatic tape drive produces fast, positive control and maximum tape life. The unique drive characteristics prevent physical contact between the driver and the oxide surface of the tape. Tape wear is greatly reduced and particle-embossing, occurring in conventional machines when particles of dirt pass between the driver and the oxide surface of the tape, is eliminated.

The transport is completely self contained, except for the pneumatic compressor unit. A modular approach to the design of all sub-units assures ease of maintenance in the field.

Table 3-1 outlines the Sylvania Magnetic Tape Transport characteristics.

3.4.2 Tape Handling Function

The tape is friction-driven by the capstans. One capstan is used for each direction of tape travel. The manifolds provide air jets that "clamp" the tape

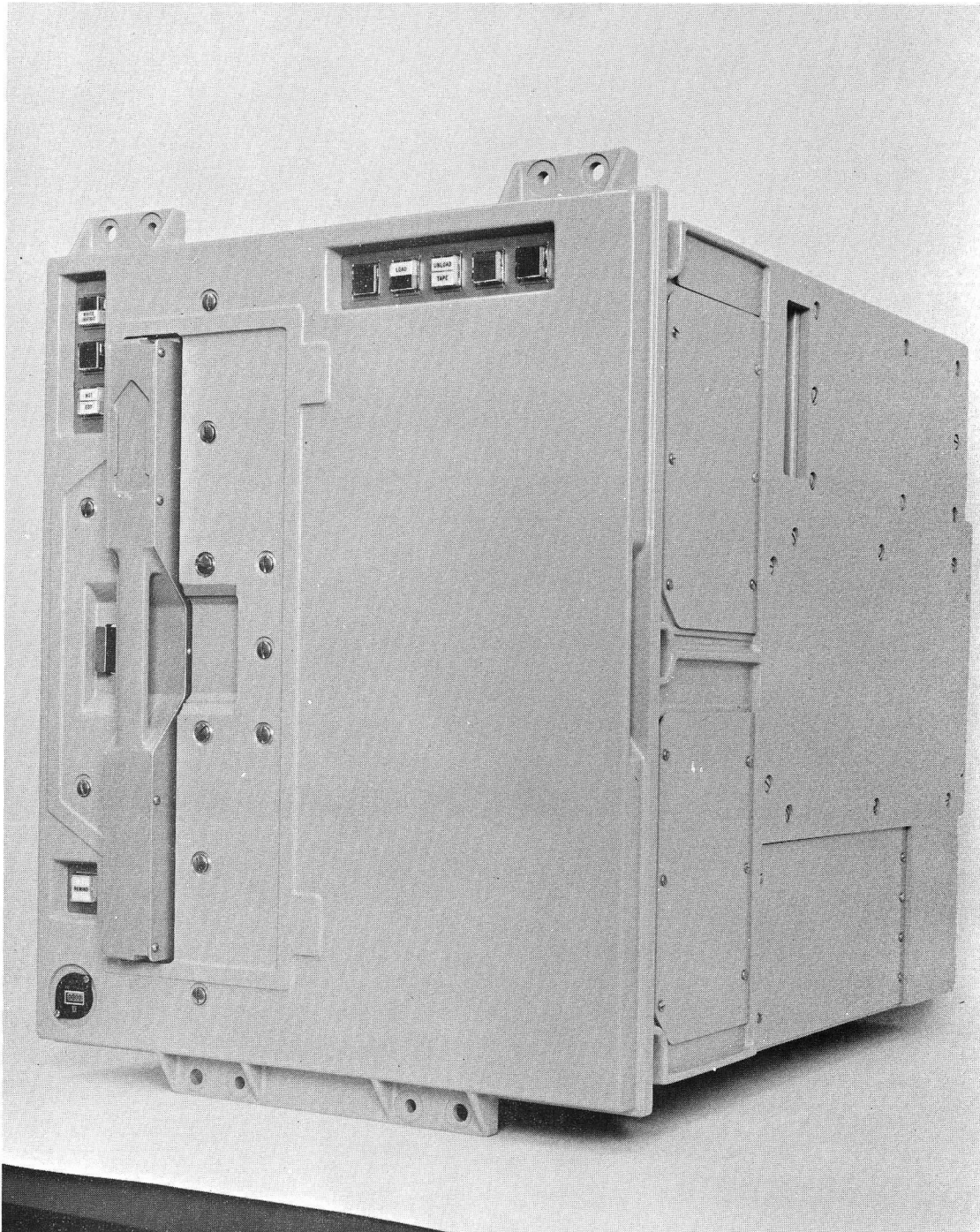


Figure 3-9. Military Magnetic Tape System

against the forward or reverse capstan on command from the computer or by manual control. The only mechanical contact with the oxide surface of the tape is at the point where it passes over the heads. The capstans are belt-driven, through an approximate three-to-one speed reduction, by the capstan motor.

The tape is protected from sudden stresses by use of a buffering tape loop between the capstans and the reels. These loops are contained and controlled in "buffer wells." A vacuum is maintained in the wells to keep the loop in a form that can be controlled (i.e., fully extended in the well as far as the tape slack between reel and capstan will allow).

The reel servo maintains the correct tape-loop length in the wells. The capstans operate at three different speeds to drive the tape:

- a. 100 inches per second, normal tape drive.
- b. 200 inches per second, high speed rewind.
- c. 2/3 inch per second, data-transmission applications.

In the first case, the capstan motor is driven from a stable-frequency, oscillator-amplifier power source. For rewind, the motor is switched to two pole operation (for twice normal speed operation) and is connected directly to the a-c prime power source. Low-speed drive is accomplished by replacing the usual capstan motor with a gearhead motor, a half-hour field change. This motor and the capstan power amplifier are enclosed in a servo loop for synchronization to the Kineplex transmission equipment.

3.4.3 Read-Write Subsystem

The system incorporates a 14-channel data format and all read and write circuitry, as well as the logic required for Hamming Code error correction. It operates at a normal data rate of 45,000 characters per second. A small field-change conversion kit is provided for data transmission at 300 characters per second.

The Read Electronics converts low-level bipolar signals representing ONE data bits to minus 3-volt RZ (return to zero) pulses while preventing high-amplitude noise voltages from causing spurious outputs. Other important functions

are the alignment of skewed characters, error detection, correction of single-bit errors, and the regeneration of parity.

The Write Electronics converts incoming RZ information to an NRZI (non-return to zero modified) form. Write Electronics also encodes the seven-message bits in such a way that single-bit transport errors can be corrected, double-bit errors can be detected, and the circuit makes an odd parity check to indicate an odd number of ONES in transmission.

3.4.4 Physical Packaging

The MT-452 Tape Transport is designed around four major aluminum castings, the front control panel, the main deck, the rear support and the package-mounting door. The main deck casting is fastened permanently, in a vertical plane, between the front panel and the rear support castings, approximately in the center of the unit. The package mounting door casting is hinged from the right vertical edge of the rear support and, when closed, fastens to the inside edge of the front panel. On its inner surface, the package mounting door carries all of the major electronic sub-assemblies: the D-C Power Supply, the Reel Servo System, the Machine Control, and Capstan Control cards and the Data Electronics 3-D stick nests. All cards and sticks are accessible for test or replacement through access openings in the outer wall of the door. In the same way, controls and test points for the D-C power supply are also accessible. This door need be opened only when it is necessary to gain access to rear card and stick wiring, to the major electronic sub-assemblies themselves, or to motors, mechanisms and other components mounted on the right side of the main deck casting. The transport may be operated with the package-mounting door open inasmuch as no electrical disconnects are involved.

The balance of the tape handling mechanisms, including the magnetic head and tape buffer wells, and some minor sub-assemblies are mounted on the left side of the desk or on the front panel and are readily available for maintenance. A secondary control panel, for maintenance only, is included on this side of the desk directly to the rear of the front panel.

The front panel has all controls necessary for normal manual operation of the transport as well as indicators to provide machine status information to the operator. The tape cartridge receptacle is sealed against dust, moisture and radio frequency interference by an interlocked door which remains closed except when a cartridge is to be replaced.

The tape transport is mounted on equipment slides and may be fully withdrawn from the supporting cabinet structure for service.

The packaging methods used in the tape handler have been selected for compatibility with the various levels of power dissipation. High-density 3-D sticks are used for the lower levels of power dissipation found in Data Electronics, the low-speed capstan frequency control logic and interface circuits.

In the low-to-medium power conversion sub-systems such as the machine control section, electronic-card packaging is used. This method allows reasonable packing density and ready access for monitoring circuit status. In this area where computer commands and status-sensing signals are converted to the medium power levels for control and actuation of electromechanical devices, more space is needed for wiring and the passage of cooling air.

In medium-to-high power conversion, such as D-C power supplies, and the servo systems, individual sub-system designs include plug-in replacement and heat-sink cooling.

TABLE 3-1. SYLVANIA MT-452 TAPE TRANSPORT SPECIFICATION

<u>Technical and Performance Data</u>	
<u>Tape Speeds</u>	
Normal Computer Operation	100 ips $\pm 1\%$
Data Terminal Operation	2/3 ips (Synchronized)
High-Speed Rewind	200 ips
<u>Start Time</u>	3 milliseconds (maximum)
<u>Start Distance</u>	0.125 \pm 0.035 inch
<u>Stop Time</u>	3 milliseconds (maximum)
<u>Stop Distance</u>	0.195 \pm 0.035 inch
<u>Tape (Ferrous oxide on polyester backing)</u>	

Width	1.000 ± 0.000 inches - 0.004
Thickness and Length	1200 feet, 1.5 mil. 1800 feet, 1.0 mil.

Tape Cartridge

Automatic Load Cycle	10 seconds
Automatic Unload Cycle	8 seconds

Data Storage

Number of Channels (Fielddata Code-Hamming & Clocks)	14
Bits per inch (per channel)	450
Recording Method	NRZI
Data Transfer Rates (write forward, read forward or reverse)	300 and 45,000 characters per second.
Data Reliability	Less than one error in 10^7 characters read.

Program Capability

Any cyclic program up to 60 cycles (240 commands per second)

Prime Power Requirement

115 volts ± 10%, single phase, 50 or 60 cps ± 5%
1.6 KVA

Physical Characteristics

Height: 21-1/4 inches, over front panel.
Width: 17-1/4 inches equipment widths 19 inches over panel.
Depth: 22-27/32, inches, from inside front panel. Panel projection 1-1/4 inches.
Weight: 340 lbs.

Environmental Specifications

The MT-452 Tape Transport has been designed in conformance with the environments described in Section 3.16 Service Conditions, SCL-4310A.

3.5 DUAL TAPE DEVICE SWITCHING UNIT

A Device Switching Unit (DSU) is an electronic switch which permits a peripheral device to operate from more than one source of data. In the case of the ATACC System, a Magnetic Tape Unit must work with any of the three of the high speed buses, on demand.

The Dual Tape DSU is Sylvania's answer to this need in the ATACC System. It contains sufficient electronics to control two magnetic tapes from each of three buses.

The Dual Tape DSU consists of 90 sticks, plus power supplies, housed in a single drawer. Six of these drawers, which will fit in a single rack, are sufficient to control 12 tapes, the maximum number which can be housed in a High-Speed Input/Output Shelter.

3.6 RANDOM ACCESS MEMORY

3.6.1 System Requirements

In recent years, information processing applications have steadily grown to require larger capacity on-line memory. The Army's logistics, fire support, intelligence and scientific requirements have kept pace with this demand for "mass storage." Logistics places heavy emphasis on "large capacity" while fire support implies "rapid access." Intelligence may require a combination of both. In the scientific field, the temporary storage of intermediate results and data tables dictates a rapid exchange of data with main memory. Recent multi-programming techniques make a large back-up store for high-speed reloads and dumps of internal memory very advantageous.

The addressing concept is a very important one from the system aspect. The internal core memory is composed of individual word locations and all addressing and transferring is done on a single word basis. If the mass storage device is also word addressable, it can directly image the main memory in content. This lends itself to programming simplicity and organization. It would also be desirable to provide for the transfer of blocks of words with single instructions to overcome the random access time and organize these blocks by sequential content. The resulting image presented by the device is simply a location with multi-million "pigeon-holes" for storing words in either binary or Fielddata format, with an extremely fast transfer time once the starting address has been reached.

The ideal location of this device is close to the core-memory since its functions are more similar to those of a memory than those of peripheral equipment. Peripheral equipment implies a conversion of internal data format to a more suitable human consumption format with the provision for permanently retaining this data at a physical location away from the computer proper. This definition imposes problems in a modular shelter type of configuration. Space near the computer proper is already occupied by main core memory, and if the data transfer rates are to be high, the length of the main transfer bus is definitely limited. For the present, connection through the input/output system with a reduction of transfer rate is the most feasible. However, a system containing one of these devices as a back-up for a smaller main memory may offer some very desirable characteristics.

3.6.2 Disc File Design

Figure 3-10 shows the disc file which has been selected for use in the ATACC computer. It was designed by the Burroughs Corporation Military Division, and has the following significant advantages:

- a. No head servo positioning system is required.
- b. Average random access time is 8.5 milliseconds.
- c. Storage capacity is over 22 million Fielddata characters.
- d. Single bit recording frequencies are as high as 3.0 megacycles, allowing a serial 75 kc word transfer rate, and ability to provide much higher rates if leads are paralleled.
- e. Packing density is over 36,000 bits per square inch for efficient magnetic media utilization.
- f. The file offers the ability to address and update individual words anywhere in the file.
- g. The disc file uses a proven principle of air-floated heads which allows head-to-disc separation increases to maintain a constant playback signal amplitude as the disc velocity increases.
- h. Temperature stability because of metal discs and individual clock tracks per disc side.
- i. True ready/strobe operation.
- j. Cobalt-nickel metal magnetic surface provides excellent wear and magnetic properties.

Table 3-2 shows the basic characteristics of this disc file.

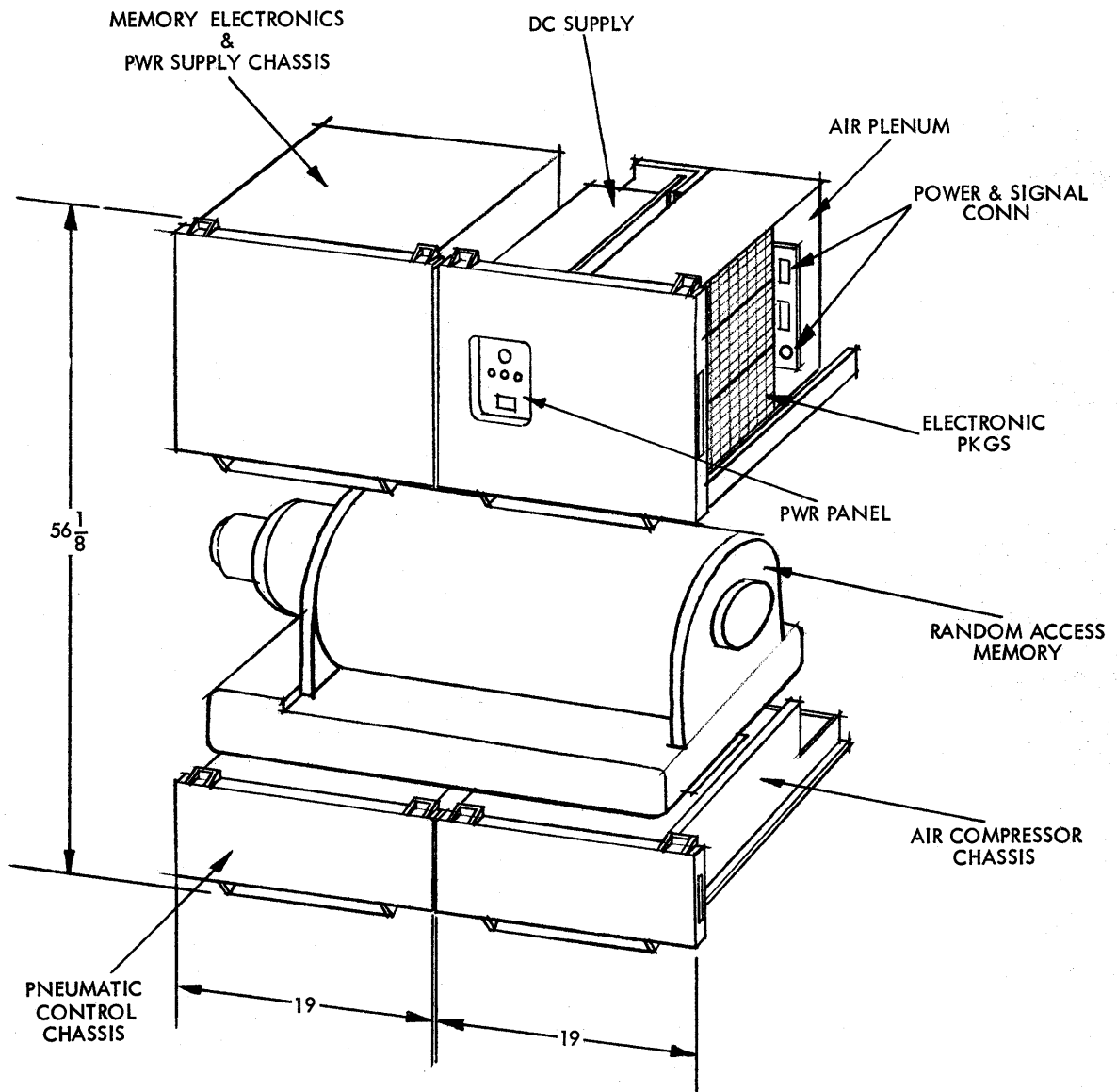


Figure 3-10. Militarized Random Access Memory

TABLE 3-2. TECHNICAL CHARACTERISTICS, DISC FILE

Head assemblies per disc side	13
Heads per assembly	13
Total heads per disc side	169
Data tracks required	156
Tracks available for clock or spares	13
Total head assemblies per file	260
Total tracks per file	3,380
Total data tracks required	3,072
Total spares	308
Total words/disc side	159,744
Total words/file	3,194,880
Total characters/file	22,274,160

3.6.3 Buffer Design

The buffer electronics is a Sylvania design which provides the necessary interface for converter operation. A simple word interlacing scheme allows the transfer rate to be reduced to a reasonable figure. A word transfer is provided so that time sharing by the converter will be more efficient. However, a character transfer can also be easily implemented without the addition of excessive electronics.

The formatting, address selection, disc control and error logic is performed by the buffer. A pure word addressing scheme is used. The word address continues to be updated until completion of an order. The format permits the recording of control words, with only a single bit per word used for this purpose. The control words can also be used for block formatting, allowing the reading of blocks, as well as words.

3.6.4 System Design

The disc file unit is completely operable through the input/output converter. A "write octal" order will initiate an address transfer to the disc buffer. A total of 22 bits of an internal memory word are necessary to specify the file starting address. The remaining 14 bits will be used for alarm and control conditions. If multiple words are received during the WOK order, the last word received will be the controlling address. A "read octal" order will initiate an address transfer from the disc buffer to the converter. This will provide information on the last word addressed plus full alarm information.

A converter "write" order will initiate data transfer to the file buffer. The buffer "ready" line must be sampled to determine if the full word transfer can take place. The ready line is set by the disc file buffer whenever the 40-bit data register is empty. Upon receipt of the ready signal the data word and a strobe signal will be sent to the file buffer. The converter will send the word as 36 bits of data, a sign bit, a control bit, and a parity bit. The control bit will signify that the word is a control word. This can be used to set up block formatting or other file organization.

The "read" function is initiated by a converter instruction. The disc buffer will search for the address contained in its address register. Upon reaching this address location the word will be serially shifted into its data register. When the data register is full, a ready signal is transmitted. The converter is now free to take this word. For a high efficiency transfer rate, the data register must be sampled within 44.4 microseconds for the worst-case inner field. If the time sampling limit is exceeded, the word may still be sampled at any time but the penalty is a full revolution time-loss before a ready is obtained for the next succeeding word. This mode of operation makes the disc unit a true ready/strobe device. It has the ability to communicate with the slowest asynchronous device without loss of data. It should be mentioned that the time period between words (66.7 microseconds) is a constant for the complete file; only the time period to shift, in a full 40-bit word, varies from field to field.

3.7 LINE PRINTER

The ATACC line printer shown in Figure 3-11 does not represent a new concept but is a proven device already in production. All of the mechanical features have been designed, tested and used under actual field conditions. Only minor modifications in packaging to adapt this printer for rack mounting in a shelter are required. The logic and circuits used have proven reliability in field use and are only repackaged to reduce over-all size and weight.

3.7.1 Printer Mechanical Description

Printer Sub-assembly—This is an integral unit consisting of a rigid framework housing the printing, paper feeding and ribbon drive mechanisms. The design follows the principle of fixed hammers operating in conjunction with a rotating drum containing the type font.

Yoke assembly—The yoke assembly houses the print wheel which is movable for ease and maintenance in cleaning.

Print wheel—The print wheel is a cylinder consisting of 120 individual segments, one for each group of 64 characters.

Pulse Generator—The pulse generator is used to provide the index and print wheel synchronizing pulses. It is attached to the end of the print wheel shaft and is of a magnetic reluctance type. Character time phasing is adjusted by the rotation of the position of the transducers.

Print Hammers—In operation, the print hammers impact the paper and inked ribbon against the appropriate character and column of the rotating print wheel. The print hammers are fired through the hammer-drive electronics at the proper time. The 120 print hammers, one for each column of type on the print wheel, are fabricated, assembled, serviced and replaced as individual modular units. The hammers are designed so that if the solenoids are energized, the hammers do not remain in contact with the print wheel. The hammers are mounted so that all adjustments can be easily made when the unit is withdrawn from the cabinet.

Paper feed—The paper feed tractors are of the pin-feed type. Upper and lower paper feed tractors are utilized for paper feeding and proper paper tension.

Line Spacing and Slew Rate—All horizontal line printing will be spaced at six lines to the inch or multiples thereof. Slew rate for continuous paper advance will be at the rate of approximately 25 inches per second.

Ribbon and Ribbon Feed—For maximum ribbon life, the ribbon is continuously moved across the printing station and is automatically reversed at the end of each traverse.

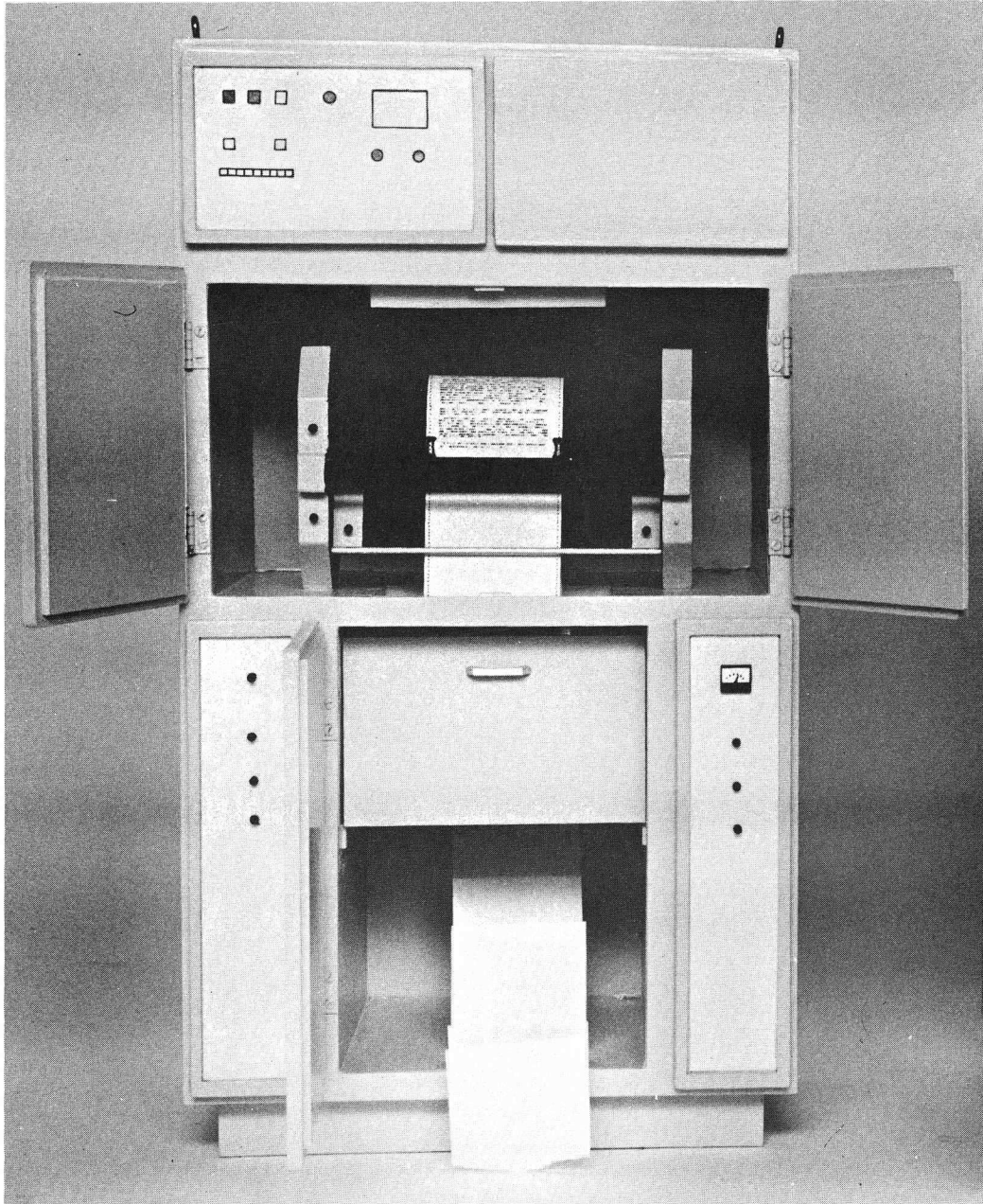


Figure 3-11. High Speed Page Printer

Printer Alarm Contacts—The firing circuits to drive the hammers, the pulse generator circuit to provide character timing, and the paper and ribbon advance circuits all utilize semi-conductors and will be packaged in pluggable modules.

Alarms—Included among the controls and alarms will be indicators to show when paper is not present as well as a low-paper indicator. The usual controls for power on/off and manual paper feed will also be included.

Table 3-3 details the printer performance characteristics. Figure 3-12 shows a sample printout (reduced photographically).

TABLE 3-3. PRINTER PERFORMANCE CHARACTERISTICS

1. Print Wheel Speed—900 rpm.
2. Type Font—Fielddata characters, 0.07 inches wide × 0.10 inches high.
3. Type pitch around the print wheel will be 64.
4. 120 characters per type line.
5. Horizontal spacing will be 0.1 inches between center lines of adjacent characters.
6. Vertical spacing will be 0.167 inches (6 lines per inch) between the mean horizontal character center lines of successive printed lines.
7. The rate of continuous paper slew will not be less than 25 inches per second.
8. Multiple part paper up to six total copies may be used.

3.7.2 Functional Description of the Line Printer and Line Printer Buffer

3.7.2.1 The Line Printer

The Shepard High-Speed Printer has no carriage as in the more conventional typewriters. Instead, there is one print hammer for each column of the page. The type face is on a drum which rotates at 900 rpm. Across one row of the drum are 120 "A"s, across the next row are 120 "B"s, etc., until, when we have gone around the entire periphery of the drum, all 64 characters have been found.

During the printing operation, the paper is positioned so that the line to be printed is opposite the print hammers. The drum rotates continuously.

As an example, let us assume that the row of "A"s on the drum is opposite the print hammers and it is desired to print "A"s on the 11th, 35th, and 97th columns of the line now being printed. If the 11th, 35th, and 97th hammer solenoids are impulsed, the hammer strikes the paper through the ribbon. The embossed "A"s on the print drum behind the paper are then transferred to the line of the page in columns 11, 35, and 97; then, the hammers return to rest while the drum continues to rotate. When the "B" row of the drum moves into position under the line of the page, the print hammers for the columns where "B"s are desired, if any, are then impulsed. This continues until all the characters on the periphery of the drum have passed under the print hammers; that is, until the drum has made one complete revolution. Of course, due to the finite travel time taken by the hammer to move from its rest position to the impact point, the actual impulsing must occur a finite time before the row of characters reaches the proper position.

In the Line Printer, 64 characters are provided around the periphery of the drum. One for each of the 64 possible Fielddata codes. Those codes which are not normally printing codes (for example, space, tabulate, etc.) were assigned special unique characters for use in the Verbatim Print-Out Mode, to be described later. The 64 characters are arranged in numerical order of their corresponding Fielddata code. Refer to Table 3-4.

A special track on the printing drum sends out sync pulses for each character position of the drum. By simply counting these pulses with an ordinary binary counter, the Fielddata code for the characters is obtained in the order in which they appear under the hammers. Another sync channel on the print drum sends out a pulse once per revolution to keep the drum and counter in synchronism.

When the drum has completed one complete revolution, the printing of the line is complete; and a signal may be sent to the printer to feed the paper. The paper will feed continuously while this signal is on. The printer will send out a pulse for every line fed, which also is sent to a counter so that the buffer may keep track of the vertical position of the paper. When the required number of

TABLE 3-4. THE 64 SIX-BIT FIELDATA CHARACTER CODES

The 64 six-bit Fieldata character codes are as follows. Where a code is not a printing character, its normal interpretation is given first, followed by the special character assigned to it for the Verbatim Print-Out Mode of operation.

000 000 Master space \mathcal{R}	100 010 +	101 101 !
000 001 No action, \mathcal{R}	100 011 <	101 110 ,
000 010 No action, \mathcal{R}	100 100 =	101 111 Stop, \oplus
000 011 Tabulate, \diamond	100 101 >	101 000 0
000 100 Carriage return, \mathcal{R}	100 110 _	to
000 101 Space, Δ	100 111 \$	111 001 9
000 110 A	101 000 *	111 010 ' ,
to	101 001 (111 011 ;
011 111 Z	101 010 "	111 100 /
100 000)	101 011 :	111 101 .
100 001 -	101 100 ?	111 110 \square
		111 111 No action, \leftarrow

line feeds has been completed, it may be stopped by simply terminating the signal from the buffer. A third signal will come from the printer until the paper has had time to come to a stop. This will be used by the buffer to inhibit the printing of the next line until the paper is at rest.

3.7.2.2 General Description of the Line Printer Buffer (See Figure 3-13 and Glossary)

The High-Speed Line Printer simultaneously prints on 120 columns of a line. Since the data to be printed comes from the In-Out Converter of the MOBIDIC system in the form of characters, of 6 bits each, buffering is needed. In addition, some of the characters are for control purposes, and some means must be provided to transform these into suitable control signals for the printer.

The High-Speed Line Printer, with its buffer unit, must be able to perform in various modes of operation. First, the so-called Programmed Line-Feed mode requires that the first character received for each line of print must be treated as a special Line-Feed Character. Before the line is printed, the printer must feed the number of lines denoted by the 6 bits of this character.

The second possible mode of operation is the Automatic Line-Feed mode, where all characters received are treated as printing or control characters. After the line is printed, a single or double line feed is always performed.

The third possible mode of operation is the Verbatim Print-Out Mode. Here, all characters received are printed, and none are treated as control characters. Since there is no possibility of a TAB, SPACE, or CARRIAGE RETURN code, the only format control possible is through the end-of-line receptacle on the TAB plugboard. Each line is followed by a double line feed.

SPACE and TAB codes will operate in the memory similarly to the way they do on an ordinary typewriter. Just as on a typewriter, the receipt of a TAB code causes the column selector counter (PA) to alter its selection to the next higher column previously chosen as a "tab" position. The choice of the tab positions must be made manually by an operator.

It is possible to select any 15 memory locations as tab positions. There are 120 TAB plugs, each wired to specify one of the memory locations from 2 to 120.

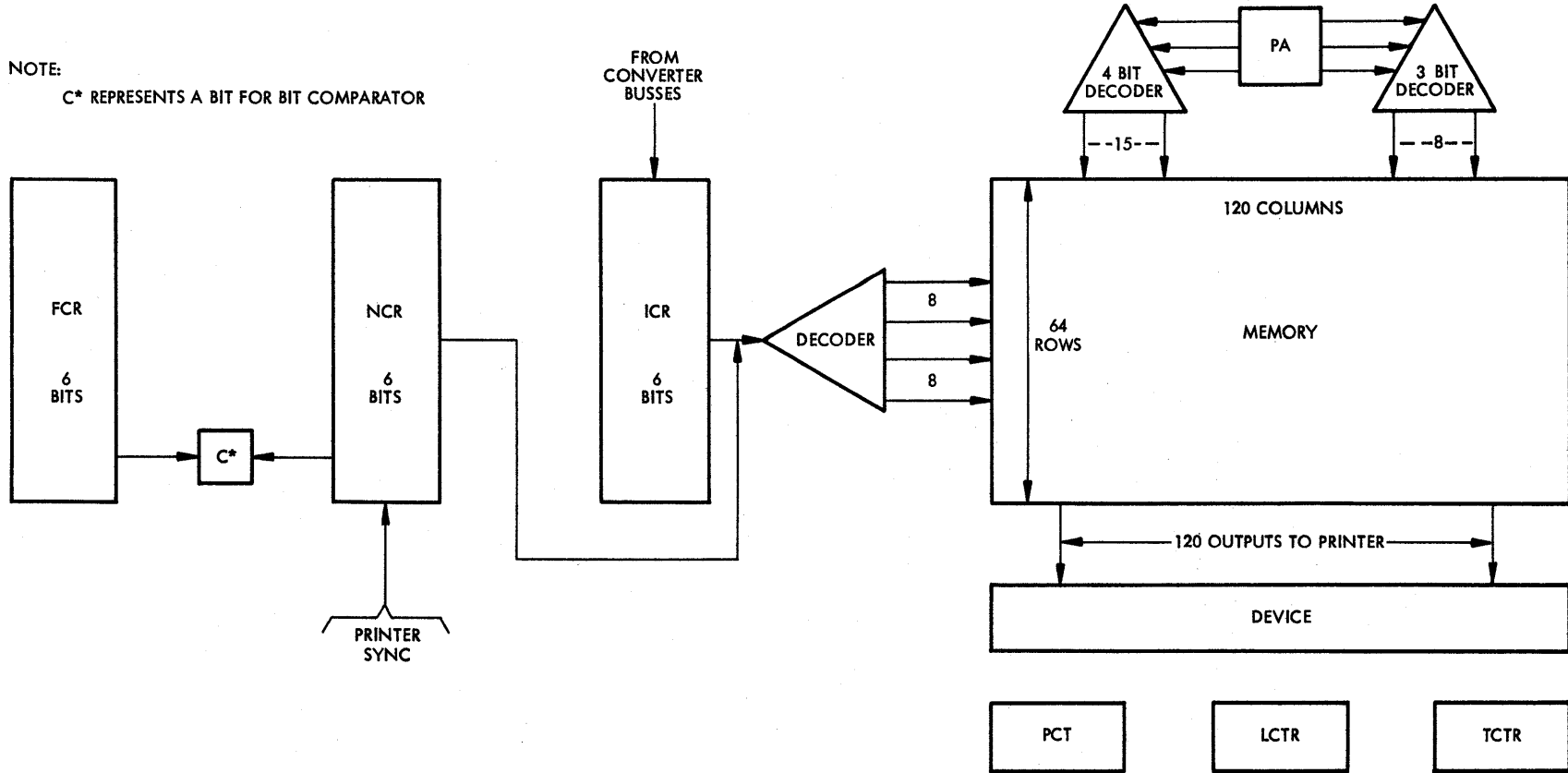


Figure 3-13. Block Diagram of Line Printer Buffer

Each plug has marked, on its back, the number corresponding to the memory location it represents. The plugs are inserted by the operator in fifteen receptacles of the TAB plugboard to indicate the columns to which the PA counter may be forced.

A sixteenth "end-of-line" receptacle is also provided; any TAB plug inserted in this receptacle will cause each line of characters to terminate at the column represented by this plug.

The reading in of data to the memory will be terminated by a CARRIAGE RETURN or a STOP code or by the end-of-line plug. Any one of these signals will stop the reading-in process and start the print-out and line-feed phases. The STOP code will also result in the printing operation being followed by a paper feed to the top of the next page.

Writing Print Drum Image into Memory

The six bits of the ICR register are decoded by an eight-by-eight matrix decoder into 64 outputs representing the 64 Fielddata alphanumeric and control characters. The address of each column is decoded from the memory address counter by a matrix. The output of the buffer matrix decoder in conjunction with the address of the column specified by the memory address counter (PA) selects one of the 64 positions in the first column of memory. Information is stored in the 120 columns by 64 rows of memory as a print drum image with one bit representing each character to be printed. As such, no more than one core can be selected in any column. The rows of the memory are ordered to coincide with the Fielddata code. The core selected in the first column corresponds to the first character of the first data word from the computer. Under control of the program counter, the ICR register is reloaded from the computer and the memory address counter is incremented by one.

The printer buffer repeats the above procedure until either the last column as specified by the End-of-Line control is written or a CARRIAGE RETURN or STOP code is sensed by the buffer, initiating a print cycle.

Selecting Next Character to be Printed

Once the memory is full, the buffer waits until the next character register is updated. Sensing the updating pulse, the buffer transfers the contents of the next character register into the first character register (FCR) to store the first character that is printed from memory.

In order to obtain maximum printing speed, the actual printout is started as soon as possible after the buffer memory is loaded. As a result, the print cycle can start with any character around the print drum. The code representing the first character printed must be retained in FCR while printing of the complete line takes place. When coincidence is detected between the contents of FCR and the next character to be printed, the print cycle is complete.

The first character printed can be any one of the 64 Fielddata characters. The output of the next character register is decoded by an eight-by-eight matrix into 64 outputs representing the 64 Fielddata alphanumeric and control characters. The space code does not produce a mark on the paper. The row in memory selected by the output of the matrix decoder is energized by a full read current producing a linear read-out from memory. Only those cores in the row previously switched in writing are again switched producing an output that is sensed by the sense amplifiers associated with each column. The sense amplifiers triggered trip the print hammers corresponding to the cores in the row switched, producing the required alphanumeric or control characters in up to one hundred and twenty positions. As the print drum rotates $1/64$ of a revolution, the next character register is incremented by one. The output of the next character register is decoded and the above process repeated.

Sensing End-of-Print Cycle

When there is a comparison between the next character register and the first character register, the print wheel has completed one revolution. The print buffer sensing the completion of the printing, causes the required paper advance to take place. The buffer is now able to process more data and sends the ready signal to the computer.

Memory Design

The print drum image memory, chosen for the buffer, differs from the more sophisticated character image memory in that, when reading out of memory to find a particular character, the memory is scanned only once rather than 120 times. At a print rate of 600 lines per minute, a character image memory is operating near the limit of its memory access cycle time, requiring critical circuit design. The print drum memory, as it is scanned only once per character imposes minimal requirements on the components and circuits thus providing the maximum in reliability. Although the same number of sense amplifiers is required for this system, their design is very simple; the memory readout is linear since full read current is driven through the memory and only a single core on any one vertical sense winding can switch. There is no disturbed zero output from other cores on the sense line and the next readout is approximately 800 microseconds later. This eliminates the problems of charge storage and common mode rejection within the sense amplifiers and also simplifies the temperature compensation of the memory.

The print drum image memory can also operate with printers capable of speeds much higher than 600 lines per minute, unlike the character memory that is operating near its limit.

In addition to these advantages, the print drum image memory is much easier to service than other designs. Failures in the more complex character storage memory systems are difficult to analyze, particularly because of the large number of operations the buffer must perform for each character. In contrast to this, the print drum image memory system is relatively slow and easy for the maintenance man to understand.

Printer and Buffer Off-Line Maintenance

An off-line checking feature is provided for the printer buffer and printer by the addition of two, 6-bit counters, and some additional control logic. This will permit the checking and maintenance of the printer buffer and printer off-line without having to use the computer. The self-check feature will produce a ripple pattern with each line of print containing all the

Fielddata characters and each succeeding line of print indexed one character. The first line of print will have 2 in column one while the second line will have a 2 in column one. Every 64th line would start with a 2 in column one. From past experience a ripple pattern of this type is most helpful in maintaining both the printer buffer and printer.

GLOSSARY

- Program Counter** — The Program Counter (PCT) controls the sequence of operation performed by the printer buffer.
- Next Character Register** — The Next Character Register (NCR) keeps track of which character is under the printer hammers. A sync. pulse, generated by the printer as each character is sensed approaching the print hammers, increments the NCR register by one.
- Memory Address Counter** — The Memory Address Counter (PA) holds the address of the next column in memory to be written when assembling a Print Drum image.
- First Character Register** — At the start of the print cycle, the first character is stored in the First Character Register (FCR). After each character is printed, the contents of NCR is incremented by one and compared with the contents of FCR. When a coincidence occurs, the print cycle has been completed.
- Information Character Register** — The Information Character Register (ICR) holds the six bit data word to be written into memory. The output of the six bits are decoded to select the one out of sixty four characters to be written into memory.
- Tab Counter** — The Tab Counter (TCTR) keeps track of which tab position is the next one to be used. Fifteen plugs on the control panel each indicate one of the 120 columns of memory. Initially, TCTR is set to zero and, therefore, selects the first of these plugs. Whatever code is wired into that plug is selected as the first tab position, and as long as it is active, a "Tab" code causes the insertion of this quantity into PA. The tab counter is then incremented by one, causing the selection of the next tab plug.
- Line Counter** — The Line Counter (LCTR) keeps track of how many lines have been fed from the top of the page. At the top of a page, LCTR contains a zero. A set of six toggle switches is preset to select the number of printed lines on a page. When coincidence is detected between the LCTR and this set of switches, it indicates that the bottom of the first page has been reached. The setting of the two page separation switches will cause the printer to line feed from one to four times more. At the end of this operation, the page is positioned and LCTR is cleared.

3.8 MILITARIZED CARD READER AND PUNCH UNIT

3.8.1 Card Processor Unit

The Card Processor is a card punch and reader combined in a single unit for computer applications in a military environment. The processor is designed for mounting in a standard 19-inch relay rack as shown in Figure 3-14. Its dimensions are $19\text{-}1/2 \times 32\text{-}1/2 \times 15\text{-}1/2$ inches. The input hopper, output stacker, reject pocket and control panel are all readily accessible from the front only.

The input hopper has a capacity of 2,000 cards. It stands vertically, is depressed into the front panel, and is pivoted as shown in the sketch to allow loading of cards.

As a card is picked from the hopper it moves to Ready Station No. 1 and is held in readiness for punching if a punch operation is called for. If the unit is to be used as a reader, Ready Station No. 1 is used as a preliminary Ready Station to fill Ready Station No. 2, which is positioned between the punch head and read brushes.

After Ready Station No. 1, the card progresses under the punch head. If it is being punched it is driven by the shuttle feed mechanism intermittently for punching. If the card is to be read, clutch-controlled rollers move it under the punch head at constant speed.

After passing under the punch head, the card is held in Ready Station No. 2 for reading. After Ready Station No. 2, the card is driven by clutch-controlled rollers into the read and re-read brushes. Reading and re-reading is performed by two rows of 80 sets of spring wire boards, one card row apart.

After reading, the card is deflected over a stacker drum and normally proceeds to the 2,000 card stacker, which stands horizontally underneath the unit. A large opening at the front of the processor allows easy access to the processed cards. If a card is rejected after passing over the stacking drum, a magnet-controlled gate puts it into a 100 card capacity reject pocket.

The processor is mounted on four full suspension slides. Maintenance, adjustments, inspection and clearing of card jams can easily be performed by sliding the processor out of the rack.

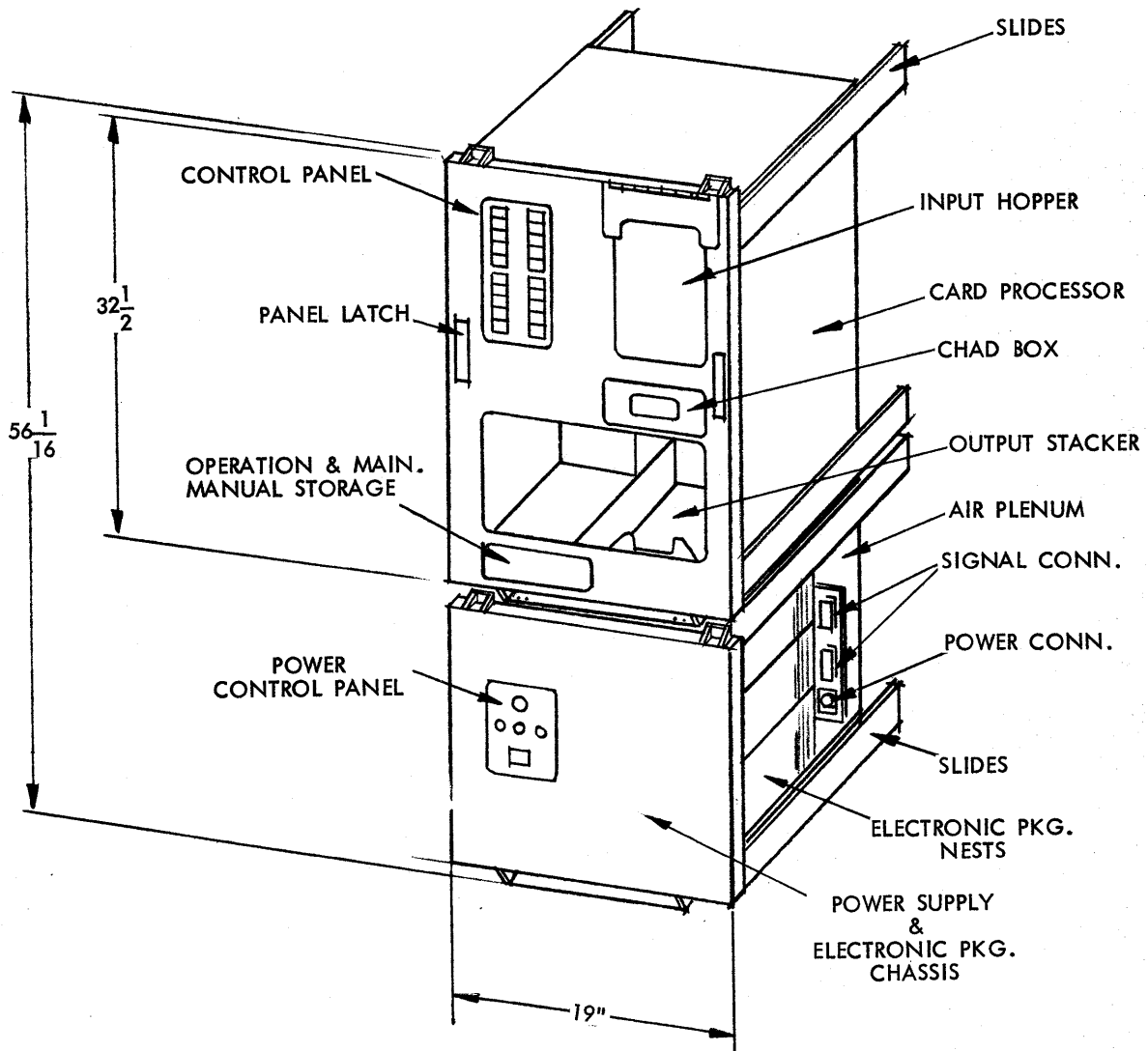


Figure 3-14. Militarized Card Reader/Punch Unit

The card unit has two basic modes of operation. They are read/re-read and punch/check read. When operated as a card reader, the unit can read and re-read cards at a rate of 800 cards per minute. When operated as a punch, it can punch and check-read cards at a rate of 250 cards per minute. When reading/re-reading or punching and read checking upon demand for every card, the rates are 650 and 232 respectively. The specifications for the card reader/punch are outlined in Table 3-5.

TABLE 3-5. CARD READER/PUNCH SPECIFICATIONS

<u>Specifications:</u>	
Input Hopper Capacity - 2,000 cards, with Hopper Empty Indicator	
Reject Pocket Capacity - 100 cards	
Output Stacker Capacity - 2,000 cards, Switch for Stacker "full"	
<u>Dimensions:</u>	
19-1/2 inches deep × 15-1/2 inches wide × 32-1/2 inches high	
Read/re-read - 813 cards per minute/650	
Punch/check - 250/232 cards per minute	
<u>Switches and Indicators Provided:</u>	
Switches	Card Read Mode
	Card Punch Mode
	Load
	Clear Buffer
	Power On
	Continuous Feed
Indicators	Power On
	Ready
	Punch Error
	Read Error
	Function Error
	Hopper Empty
	Stacker Full
	Reject Pocket Full
	Card Jam
	Card Misfeed
Head In Lock	

3.8.2 Card Buffer

The card buffer provides the control for the reading of cards at an 813 card per minute rate and the punching of cards at a 250 card per minute rate. The buffer is format compatible with the MOBIDIC Processing System. In addition, it has a built-in "echo" check for reading, and it transmits read-after-punch data to the central system for punch checking. If a read check error occurs, the error card will be rejected to a reject pocket from which point it can be recovered and again read. If a punch check error occurs, the error card will also be rejected to the reject pocket. The computer can then retransmit the data and the card will be repunched.

Read Operation

The buffer, upon receipt of a read command, initiates a read cycle. The first row of data is read into an 80-stage register (storage register No. 1) from read station No. 1. The data is sent to the converter on Fielddata character at a time with the buffer adding the control and parity bits. Upon completion of the transfer, the data in Register No. 1 is transferred to a second, 80-stage register (storage register No. 2) and storage register No. 1 is cleared. When the second row of the card is read into storage register No. 1, the previous row is under the brushes of read station No. 2 (read stations are one row apart). Wherever a logical "one" is read from the brushes of read station No. 2, the corresponding stage of register No. 2 is complemented. If the data read from the second read station is the same as that previously read at read station No. 1, storage register No. 2 will contain all "zeros." Storage register No. 2 is sampled and if all zero condition is absent, an error indication will be transmitted to the converter and the buffer halts. In addition, the error card is rejected to the reject pocket from which point it can be recovered and again read. If no error occurs, cards are continuously processed, reading one row and checking the previous row, until a halt command is received from the converter. The halt command stops the buffer in a state where it is ready to respond to another read order.

Punch Operation

Upon receipt of a punch order, the buffer initiates a punch cycle. Data is accepted from the converter, character by character until storage register No. 2 is filled. The data transfer is checked for parity, and if an error is detected, the

converter is signaled. Each time storage register No. 2 is filled, a row of the card is punched. As the first card is being punched, there is no card at the read after punch station (stations are one card apart). When punching the second card, the first card is simultaneously read at read station No. 1. The data from read station No. 1 is transferred into storage register No. 1 and then transmitted character by character to the converter for comparison. If an error is detected, a signal is sent to the buffer which rejects the card into the reject pocket. The data for that card is then retransmitted to the buffer and the card is repunched. Cards are processed in this manner until a halt order is detected. The halt order stops the buffer in a state where it is ready to respond to another punch order.

Device Alarms

When the card buffer or card transport is in a non-operating state, the converter will be signaled. Conditions contributing to this non-operating state include:

1. Ready stations not loaded
2. Machine set for reading and a punch order received
3. Machine set for punching and a read order received
4. Hopper empty
5. Stacker full
6. Reject pocket full
7. Card jam detected
8. Power failure

Control Panel

A control panel is located on the card buffer cabinet. The panel contains switches for applying power, loading cards, clearing the buffer, mode selection, and maintenance. Indicators are provided to display power and alarm status.

3.8.3 Card Reader and Punch Physical Design

The card equipment package will be a completely self-contained unit consisting of two chassis. The upper unit will be a row card processor transport and the lower unit a pull-out chassis containing d-c supplies and associated electronics. The total panel height of these two units will be 56-1/8 inches, with a maximum panel width of 19 inches and a maximum over-all depth of 23 inches

from the front mounting surface of the shelter housing. These units will also fit in a standard 17-3/4-inch opening.

Electronic Chassis

This chassis has mounted on its right hand side, three nests of electronic packages. This portion of the chassis is compatible to the standard computer logic drawers in concept. Air passages are at the front corner of the chassis and will be metered for proper cooling. The left hand side contains the necessary d-c supplies. These supplies will be mounted on a vertical panel running from front to rear of the chassis. This panel will be hinged at the rear to allow access to the wiring side of the electronic package nests. The power supply nests and the electronic package nests will each contain a fan for proper cooling.

This chassis will be supported by slides at each of the bottom corners and stabilized by a slide in the top center. The chassis will be permanently attached to a front panel which will contain power controls and be used to lock the chassis in place. This panel will have the physical shape of all other peripheral equipment panels and will be compatible with the row card processor panel. The chassis will have a standard 19-inch front panel, 20-1/2 inches high and will be 23 inches deep not including the front panel. The slides will allow accessibility to the chassis from all sides in its extended position.

3.9 MILITARIZED PAPER TAPE EQUIPMENT

Sylvania is proposing Kleinschmidt paper tape equipment with a fully compatible stick buffer unit. This equipment is rugged, reliable, and militarized, and provides low speed printer output. (See Figure 3-15.) A Fielddata Paper Tape Set previously delivered to the Signal Corps by Kleinschmidt, will be modified by substituting a Kleinschmidt Model 311 printer for the Smith Corona electric typewriter. The complete Paper Tape equipment consists of:

1. Reader: 300/40 characters per second
2. Punch: 40 characters per second
3. Kleinschmidt Model 311 printer:
40 characters per second, and built without large moving carriage
4. Control Unit

3.9.1 System Integration

The paper tape reader, paper tape punch and 311 printer will be operated and controlled over the converter slow speed I/O line. The control unit provided with the prototype paper tape set is no longer required. The Mod II Input/Output Converter is capable of performing all the necessary off-line operations, and an external control unit would only be redundant.

Sylvania's buffer will contain a single DSU for each device with a single Mod II system. The DSU will handle the addressing and ready/strobe logic and the gating for I/O transmission. The buffer will provide for full flexibility by allowing simultaneous operation of all three units. Code translation from Fielddata standard to Fielddata paper tape is not required by either the converter or the buffer, since each device is designed to perform this automatically. Full advantage of each device speed will be possible through Mod II IOC control since the converter can handle the asynchronous timing requirements. Normally, the reader will be operated in the stepping mode (40 characters per second) rather than free running (300 characters per second) mode, to prevent possible loss of characters. A buffer register will not be required even in the high-speed mode, but the converter must respond to a strobe within one millisecond to prevent

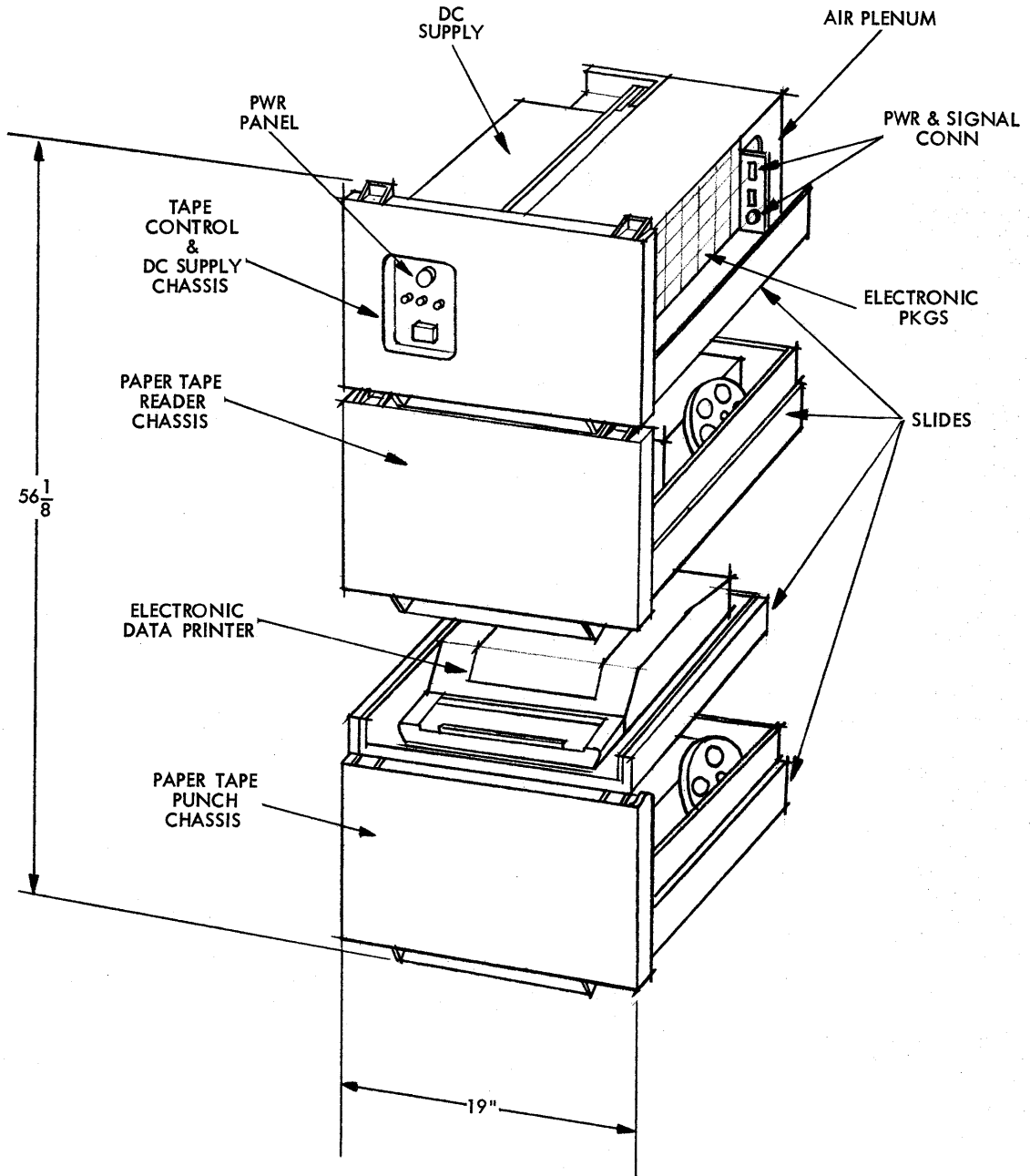


Figure 3-15. Militarized Paper Tape Equipment

loss of a character. The incremental mode is exceptionally well suited to the converter's time sharing operation. The high speed mode will be used for batch processing of large amounts of paper tape data, when paper tape time becomes a larger portion of the input/output processing.

3.9.2 Equipment Design

Paper Tape Reader

This device, already developed under Signal Corps contract is proposed essentially unchanged, with only product improvements resulting from previous testing. The device is Fielddata compatible and will therefore require little or no buffering. The reader senses paper tape containing Fielddata paper tape (even parity) code and transmits standard Fielddata (odd parity) code on eight parallel data lines. The reader employs reliable silicon solar cells and a standard light source, (12-volt automobile tail light bulb operating at 8 volts (any 12-volt military bulb is therefore acceptable). The bulb output is carried by a plexiglass light tube to the paper tape read station and activates the solar cells.

This reader can also handle 5, 6, 7 or 8 bit tape. It has two modes of operation: (1) "Stepped" at 40 characters/sec, and (2) "Free Running" at 300 characters/sec.

In the free running mode the device can stop on the next character if signaled within 100 microseconds after the strobe; it will not send this next character until the succeeding forward command. The unit is equipped with two 200 feet, five-inch diameter reels (supply and takeup) which store the tape during the reading operation. A toggle switch permits the tape to be rewound onto the take-up reel. A malfunction line indicates conditions which prevent the reading operation e.g., tape not loaded, tape broken or power off.

Paper Tape Punch

The punch operates in an incremental mode at 40 characters per second. It perforates paper tape with data received on 5, 6, 7 or 8 parallel wires, from the transmitting source. The electronic circuit of the punch translates the

received standard Fieldata (odd parity) code and perforates the tape with paper tape (even parity) code. The device has a 1000 foot, eight inch diameter supply reel and a 200 foot, five-inch diameter take-up reel. The punching operation is full ready/strobe and its speed is compatible with the reader. A punch operating at higher speeds is possible but Sylvania's previous experience has shown that it is better to decrease speed to obtain more reliable, maintenance-free performance. Both 100 characters per second, and 40 characters per second are slow speeds compared to the computer's capability, and with a multiplexing converter time is not lost on slow devices.

Medium Speed Printer

The model 311 data printer is used for both input and output. The input facility is intended primarily for off-line operation. Keyboard inputs can be punched on tape, cards or high speed line printer, thus providing the maximum in flexibility. The keyboard could also enable the operator to send information through the computer to the Communications Converter and thence out through the TYC units. The output features will enable the receipt of return messages.

The printer has no large moving carriage. It utilizes a 1600 rpm character drum mounted behind the paper. A pair of hammers travels across the front of an 80-column page and impact against the paper through a standard size typewriter ribbon at the correct time to produce the desired character in each column. The printer operates at an average rate of 40 characters per second, with the speed being dependent on successive character relationship. The minimum rate is 27 characters per second. This printer is capable of much higher operation with the installation of hammers for each column, if future requirements warrant. The printout is neat and legible and has a slightly raised appearance, since the type characters are directly behind the paper. An original and three tissue copies can be printed. Timing is provided by a pair of reluctance pickups which sense the position of the print drum and provide a continuous train of 64 character pulses and a single reset pulse for each drum revolution.

Buffer

The buffer unit contains, the three separate DSU's and some special control flip-flops applicable to the I/O bus multiplexing operation. The Mod II IOC will select a device by sending an address over the common bus lines. After the address information transients have settled (typically one microsecond), a select signal will be sent. All DSU's will then sample the address lines, but only the applicable device will connect to the data and control lines.

The reader buffer will contain a flip-flop to keep the forward line activated. The low speed/high speed switch on the reader will determine whether "stepped" or "free running" mode will be used. During the "free running" mode the tape will continue to move until the forward line is dropped. Each time the DSU is addressed the forward control line is sampled; if equal to "one" the flip-flop is set or remains set, if equal to "zero" the flip-flop is cleared and the reader halts.

The punch unit, being fully incremental, does not require a forward signal. It will process tape upon receipt of "strobe" pulses from the DSU, whenever power is on, and no malfunctions are reported.

The data printer and keyboard unit contains the necessary internal registers and thus requires no external buffer registers. The buffer must contain control flip-flops to select the printer or keyboard. The read or write line will determine the selection. The forward line will be flip-flop sampled as in the case of the reader for device start and stop control. A visual indicator is provided for keyboard input. This indicator, which is controlled from the ready signal, allows the operator to send a character. Attempts to send without the ready signal indicator, will cause a character drop indicator to light. The operator can thus synchronize his sending speed; it also enables the computer to not grant a ready signal if a line printer or TYC is overloaded and cannot accept more data.

3.10 PERIPHERAL DEVICE STATUS PANELS

Assigned to each peripheral device, but adjacent to the Main Console, in the Central Processor Shelter is a set of indicator lights and selection switches

to show the status of the associated device. These items are mounted on separate panels for each shelter in the system. That is the Central Processor Shelter will contain a panel for its own devices, as well as up to two panels for associated high-speed and two panels for low-speed shelters. The panels will contain the following items, which are necessary for all devices.

On-Line, Off-Line Selection Switch—This is a two position indicating switch to reserve the associated device for On-line operation. If it is in the On-line position and an attempt is made to use it from an off-line program or console, such use is prevented by the IOC.

Ready Indicator—This indicator shows that the device in question has however, no error conditions, and is ready to operate.

Selected Indicator—The device has been selected and is in operation.

In addition to the common items listed above, each device position which is capable of Magnetic Tape Operation also has the following indicators.

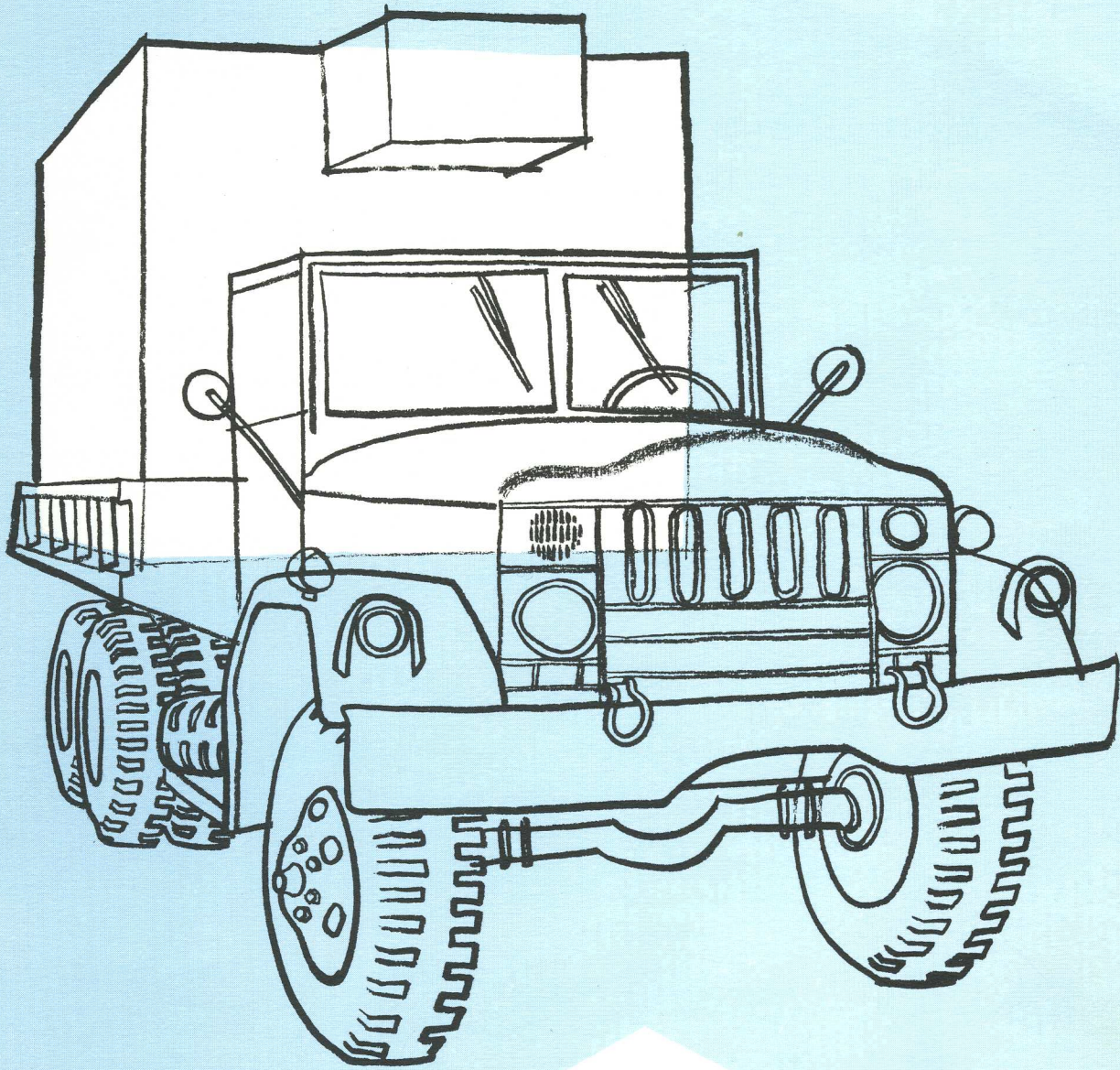
Rewind Indicator—The tape is being rewound.

Load Point Indicator—The tape is at its initial position after rewind.

Write Inhibit Indicator—The write unit of the tape in question is inhibited.

End of Tape Warning—The tape in question is within one block length of the end of tape.

APPENDICES



the

ATACC

COMPUTER

for Army Tactical Command and Control

APPENDICES

THE ATACC COMPUTER

FOR

ARMY TACTICAL COMMAND AND CONTROL

- A BLOCK DIAGRAMS AND TEXTS
- B BASIC CIRCUIT SELECTION AND ELECTRICAL PACKAGING
- C MECHANICAL DESIGN
- D ATACC RELIABILITY
- E PROGRAMMING

APPENDIX A
BLOCK DIAGRAMS AND TEXTS

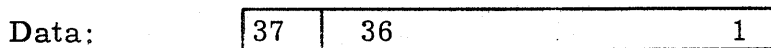
Appendix A consists of five parts, A. 1 through A. 5, each part gives further details of the unit which it treats.

Part A. 1 deals mainly with the Central Processor, giving its word structure, the order repertoire for the entire system and block diagram. Part A. 2 consists of a block diagram and theory of operation of the Input/Output Converter. Parts A. 3, A. 4, A. 5 treat the Memory, Console and Communications Converter respectively. The features of the system are discussed as though the "Compatibility Switch" is in the "ATACC" State, since its characteristics in the "MOBIDIC" position are well known.

A. 1 CENTRAL PROCESSOR

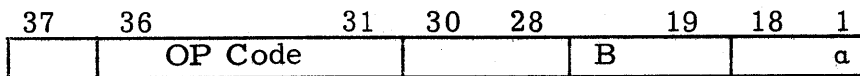
This section of the Appendix contains the ATACC Word Structures, Order Codes, a Register Block Diagram with description, and a brief discussion about a number of features of the ATACC Central Processor. Typical timing charts and diagrams complete the section.

A. 1. 1 ATACC CP Word Structures



Data words are interpreted as a binary point to the left of bit 36, plus a sign bit. (bit 37)

CP Instructions



In CP instructions, bits 1-18 specify a memory address (if bit 18 = 1, a refers to an addressable register), bits 31-36 specify an OP Code, while B and a are used for a variety of purposes.

Other word formats used for the purposes of the Input / Output Converter and the Communications Converter, are outlined in sections A. 2 and A. 5 respectively.

It should be pointed out here, however, that operation of the IOC is initiated by an SOS order, from the CP, giving the starting address of a series of IOC commands. Commands in that format are interpretable only by the IOC.

A. 1. 2 Overflow Control

An arithmetic overflow will set the Overflow Alarm flip-flop. This flip-flop can be reset by a SNR instruction, or by any CLA, CLS, CAM.

A. 1. 3 Trapping Mode

ATACC has no trapping mode.

That mode was designed to assist the programmer in debugging programs. The technique is now obsolete since programmed debugging aids have been developed which are much more flexible and useful.

A. 1. 4 Indexing

Prior to performing any indexable instruction, the address field is augmented by the contents of the index register specified by the gamma field of the instruction. If $\gamma = 0$, no augmenting takes place.

A. 1. 5 Program Interrupt

The ATACC Program Interrupt capabilities are more flexible and more easily used than those of MOBIDIC. Four basic interrupt causes are recognized by ATACC.

1. Malfunction of or improper order to Central Processor, communication converter or input/output converter.
2. Real time clock value equals or exceeds the real time clock compare register.
3. Communication Converter control character receipt, completion of input or output message.
4. Input/output converter control character receipt, completion of input or output order.

Each cause is assigned two fixed locations in memory and a two bit priority control register. Locations $(000000)_8$ through $(000007)_8$ are used. The even number addresses for subroutine entrance and the odd numbered for status information. The program initially loads each subroutine entrance location with a TRU to the appropriate subroutine, and loads the associated priority register to designate the assigned priority.

The priority bits have the following meaning:

- 00 Do not allow interrupt for this cause.
- 01 Allow interrupt unless a 10 or 11 interrupt is being processed.
- 10 Allow interrupt unless an 11 interrupt is being processed.
- 11 Allow interrupt for this cause.

When an interrupt is allowed to occur, the corresponding status word will contain the following:

- Bits 1-17 Program Ctr. at interrupt time
- 19-34 Address of IOC or CC control word
- 35-36 Error Indication
- 37 Previous interrupt Flag

The ATACC Priority Program Interrupt feature uniquely identifies each interrupt cause, conserving programming space and time, and is so designed to allow interrupts of higher priority while operating in a lower priority subroutine.

A. 1. 6 Memory Priority

A group of logic within the Central Processor establishes which units will have access to the memory next. Priorities are assigned in the following order:

- Priority Level 1: Program Interrupt or Interrupt Subroutine
- Level 2: Input/Output character
- Level 3: CP Normal Instructions

Within each of these levels, there are many sub-levels; for example, an input character takes priority over an output character.

A. 1. 7 Shift Option

Appendix E contains a discussion of still another feature of the ATACC CP, the Shift Option on arithmetic instructions.

A. 1. 8 Order Code and Sensable Flip-Flops

Table A-1 is a list of the ATACC Order Codes. Table A-2 is a list of Sensable Flip-flops.

A. 1. 9 Register Block Diagram

A register block diagram of the Central Processor is shown in Figure A-1. Its structure appears similar to that of MOBIDIC but closer inspection reveals a number of differences. The Add Logic has inputs from the Main Transfer Bus and the B Register, rather from A & B as in MOBIDIC. In addition, its outputs may be gated to AR as well as to A. This is the means by which the Add Logic is time shared.

For example, if an instruction has been read into B which calls for indexing, the appropriate index register is gated onto the bus, and the output of the Add Logic is read into AR. A second difference is that communications of data and addresses to the memory and over bus systems separate from the Main Transfer Bus. This permits the internal bus to be truly high speed, and operations internal to the CP may continue independently of the activities of the Input/Output and Communication Converters.

Other differences include the addition of three index registers, for a total of seven; lengthening of the index registers to 17 bits to span the entire field, and the addition of a real time clock, and real time clock compare registers in memory.

The function of each block in Figure A-1 is discussed briefly below.

TABLE A-1. SUMMARY OF ATACC OPERATION CODES

Instruction	a	A	Q	B	1^γ	$1^{\gamma+1}$	Notes	Time
ADB 24	$C(a) + \beta$	$C(a) + \beta$	$C(A)$	$A_{SN} = +; \beta \rightarrow B$ $A_{SN} = - \begin{cases} C(a) \geq \beta; C(a)' \rightarrow B, B_{SN} = A_{SN} \\ C(a) < \beta; 0 \rightarrow B \end{cases}$	$C(A)_{1-12}$		Cannot be indexed Overflow possible but not detected	$14\mu s$
ADD 12		$C(A) + C(a)$		$A_{SN} = A_{SN}; C(a) \rightarrow B$ $A_{SN} \neq A_{SN} \begin{cases} C(A) \geq C(a) ; C(a)' \rightarrow B, B_{SN} = A_{SN} \\ C(A) < C(a) ; 0 \rightarrow B \end{cases}$			Overflow is possible	$8\mu s$
ADM 13		$C(A) + C(a)$		$A_{SN} = +; C(a) \rightarrow B$ $A_{SN} = - \begin{cases} C(A) \geq C(a) ; C(a)' \rightarrow B, B_{SN} = A_{SN} \\ C(A) < C(a) ; 0 \rightarrow B \end{cases}$			Overflow is possible	$8\mu s$
CAM 11		$ C(a) $					Overflow is cleared	$8\mu s$
CLA 10		$C(a)$					Overflow is cleared	$8\mu s$
CLS 14		$C(a), A_{SN}' \rightarrow A_{SN}$					Overflow is cleared	$8\mu s$
CSM 15		$- C(a) $						$8\mu s$
CYL 35		A, Q cycled left amod 128 places					Signs included	$a < 8: 8\mu s$ $a > 8: 8 + \frac{a-8}{2}$
CYS 34		A cycled left amod 128 places					Sign not included	$a < 8: 8\mu s$ $a > 8: 8 + \frac{a-8}{2}$
DVD 22		Remainder	Quotient	$C(a)$			Overflow is possible	$48\mu s$
DVL 23		Remainder	Quotient	$C(a)$			Overflow is possible	$48\mu s$
HLT 00							Computer stops	$8\mu s$
LDX 53					β	α	Cannot be indexed	$8\mu s$
LGA 03		Logical Sum $C(a) + C(A)$		$C(a)$			Signs Included	$8\mu s$
LGM 02		Bit by bit Logical Product $C(A)C(a)$		$C(a)$			Signs Included	$8\mu s$

TABLE A-1. SUMMARY OF ATACC OPERATION CODES (Cont.)

Instruction	a	A	Q	B	I^γ	$I^{\gamma+1}$	Notes	Time
LGN 04		$C(a_{1-37})'$					(Sign included)	$8\mu s$
LOD 51				$C(a)$			$C(a) \rightarrow$ Addressable Register not in main memory	$10\mu s$
MLR 21		$C(A)C(a)$ High order bits rounded	$C(A)C(a)$ Low order	$Q_{36} = 0; C(a) \rightarrow B$ $Q_{36} = 1; 0 \rightarrow B$				$48\mu s$
MLY 20		$C(A)C(a)$ High order	$C(A)C(a)$ Low order	$C(a)$				$48\mu s$
MOV 52†			a on RPT-MOV only	$C(a)$			$C(a) \rightarrow \gamma\beta$ cannot be indexed	$12\mu s$
MSK 55	Bit by bit logic $Q_1 = 1; a_1 = A_1$ $Q_1 = 0; a_1 = a_1$			$C(A)$				$12\mu s$
NRM 37	Number of shifts $(x 2^{-36})_{36}$ $C(A) = 0; 36 \times 2^{-36}$	High order zeros shifted off; low order zeros inserted						-
RPA 54	$C(A_{1-15})'$ $C(a)_{1-15}$			$C(A)$				$10\mu s$
RPT 01							$a \rightarrow I^3$ $C(PC) + 2 \rightarrow PC$ $\beta \rightarrow I^4$	$8\mu s$
SBB 25	$C(a) - \beta$	$C(a) - \beta$	$C(A)$	$a_{SN} = + \begin{cases} C(a) \geq \beta; \beta' \rightarrow B, B_{SN} = a_{SN} \\ C(a) < \beta; 0 \rightarrow B \end{cases}$ $a_{SN} = -; \beta \rightarrow B$	$C(a) - \beta$		Overflow is possible but not detected.	$14\mu s$
SBM 17		$C(A) - C(a) $		$A_{SN} = -; C(a) \rightarrow B$ $A_{SN} = + \begin{cases} C(A) \geq C(a) ; C(a)' \rightarrow B, B_{SN} = a_{SN} \\ C(A) < C(a) ; 0 \rightarrow B \end{cases}$			Overflow is possible	$8\mu s$
SEN 05*				$TRA = 1; C(PC) \rightarrow B$			$C(\beta) = 1; a \rightarrow PC$ $C(\beta) = 0; C(PC) + 1 \rightarrow PC$	$8\mu s$
SHL 30		$C(A)$ Shifted left a mod 128					Sign not included Overflow is possible	$a < 8: 8\mu s$ $a > 8: 8 + \frac{2-3}{2}$
SHR 32		$C(A)$ Shifted right a mod 128					Sign not included	$a < 8: 8\mu s$ $a > 8: 8 + \frac{2-8}{2}$
SLL 31		$C(A, Q)$ Shifted left a mod 128					Signs not included Overflow is possible	$a < 8: 8\mu s$ $a > 8: 8 + \frac{2-8}{2}$

* Trapping is possible

† On this instruction β extended by the contents of the β extender register.

TABLE A-1. SUMMARY OF ATACC OPERATION CODES (Cont.)

Instruction	a	A	Q	B	1^{γ}	$1^{\gamma+1}$	Notes	Time
SNR 07*				TRA = 1; C(PC) → B			C(β) = 1; 0 → C(β), a → PC C(β) = 0; C(PC) + 1 → PC	8μs
SNS 06*				TRA = 1; C(PC) → B			C(β) = 0; 1 → C(β), a → PC C(β) = 1; C(PC) + 1 → PC	8μs
SRL 33		C(A, Q) Shifted right a mod 128 places					Signs not included	$\frac{a < 8: 8\mu s}{a > 8: 8 + \frac{a-8}{2}}$
STR 50	C(A)							8μs
SUB 16		C(A) - C(a)		$A_{SN'} = {}^a_{SN} \begin{cases} C(A) \geq C(a) : C(a)' \rightarrow B, B_{SN} = {}^a_{SN} \\ C(A) < C(a) : 0 \rightarrow B \\ A_{SN} \neq {}^a_{SN}' : C(a) \rightarrow B \end{cases}$			Overflow is possible	8μs
TRC 47			C(A)	a			C(A) < C(a); C(PC) + 1 → PC C(A) > C(a); C(PC) + 2 → PC C(A) = C(a); C(PC) + 3 → PC	12μs
TRL 41*				TRA = 1; C(PC) → B	β		C(PC) + 1 → PCS a → PC Cannot be Indexed	8μs
TRN 46*				TRA = 1; C(PC) → B			$A_{SN} = + ; C(PC) + 1 \rightarrow PC$ $A_{SN} = - ; a \rightarrow PC$	8μs
TRP 44*				TRA = 1; C(PC) → B			$A_{SN} = - ; C(PC) + 1 \rightarrow PC$ $A_{SN} = + ; a \rightarrow PC$	8μs
TRS 42*				TRA = 1; C(PC) → B			PCS → PC	8μs
TRU 40*				$\beta_{16} = 0, TRA = 1; C(PC) \rightarrow B$ Otherwise; B unchanged			$\beta_{16} = 0, TRA = 1; 0 \rightarrow PC$ Otherwise; a → PC	8μs
TRX 45*				TRA = 1; C(PC) → B TRA = 0; a → B	$C(1^{\gamma}) + \beta$ If $1^{\gamma+1} \neq 0$; Otherwise no change	$C(1^{\gamma+1}) - 1$ If $1^{\gamma+1} \neq 0$	$C(1^{\gamma+1}) \neq 0; a \rightarrow PC$ $C(1^{\gamma+1}) = 0; C(PC) + 1 \rightarrow PC$ Cannot be indexed	12μs
TRZ 45*				TRA = 1; C(PC) → B			$C \mid (A_{1-36}) \mid = 0; a \rightarrow PC$ $C \mid (A_{1-36}) \mid \neq 0; C(PC) + 1 \rightarrow PC$	

TABLE A-1. SUMMARY OF ATACC OPERATION CODES (Cont.)

Instruction	Operation	Notes
* WAN 74	Writes $k \pmod{2^9}$ words on IOD_j (Input Output Device). First word is at location a . Words record six bits at a time. If interpret sign flip-flop is set, the sign is treated as a six-bit character. If j is magnetic tape, block marks inserted before and after k words.	Six characters per word plus one character for sign.
* WOK 76	Three-bit octal digit is converted to six-bit equivalent and written on paper tape. Sign is always interpreted.	Cannot be used for magnetic tape. Thirteen Six-bit characters per word.
* ROK 72	Reads $k \pmod{2^9}$ words from IOD_j and stores in memory beginning at a . Treats thirteen six-bit characters as octal word and sign. If Stop code is read, order is terminated whether or not $k = 0$.	Cannot be used for magnetic tape.
* RAN 70	If j is magnetic tape unit, $k \pmod{2^8}$ words or blocks are read into memory beginning at location a . If $k_9 = 1$, k_{1-8} signify number of blocks; if $k_9 = 0$, k_{1-8} signify number of words. With paper tape, $ISN = 1$ gives continuous reading until a stop code is received or until $k_{1-9} = 0$; if $ISN = 0$ and $k_9 = 1$, reading will continue until a stop code is received; if $ISN = 0$ and $k_9 = 0$, only one character is read in.	Low order zeros inserted if full word is not used.
* SKP 66	Tape unit j skips forward $k \pmod{2^9}$ blocks.	Magnetic tape only.
* BSP 67	Tape unit j backspaces $k \pmod{2^9}$ blocks.	Magnetic tape only.
* RRV 71	Same as RAN except reads in opposite direction.	Magnetic tape only.
* RWD 77	Rewinds tape j .	Magnetic tape only.
* WWA 75	Searches for beginning block marks. Then writes $k \pmod{2^9}$ words starting at memory location a and puts block mark after $k \pmod{2^9}$ words.	If beginning block mark is not found, whole tape is searched.
SOS	The address field of this instruction defines the starting location of a set of input output commands.	

*The order codes given here are for MOBIDIC. A three bit order code is assigned for use with the IOC.

TABLE A-2. SENSABLE FLIP-FLOPS

Octal Address	Designation Code	Description	Can be set by Program	Can be reset by Program
0001 - 0077*	IOD	In-Out Device Busy Signals		
0100	OA	Overflow Alarm	X	X
0101	ROPI	Real Time Output Program	X	X
0102	ISN	Interpret Sign	X	X
0103	NHC	No Halt on In-Out Converter Error	X	X
0104	RPE	Real Time Parity Error		X
0110 - 0115	SFF1 - SFF6	General Sense Flip Flops	X	X
0116 - 0127	SFF7 - SFF16**	General Sense Flip Flops	X	X
0130, 0131	IOA ¹⁻²	In-Out Alarm Flip Flops In In-Out Converters No. 1 and No. 2		
0135	TPE	Tape Erase	X	X
0150	FCI	Functional Control Character Interrupt	X	X
0151 - 0152	FCC ¹⁻²	Read Functional Control Char- acter,	X	X
0155	ROSN	Real Time Output Interpret Sign	X	X
0156	RISN	Real Time Input Interpret Sign	X	X

TABLE A-2. SENSABLE FLIP-FLOPS (Cont.)

Octal Address	Designation Code	Description	Can be set by Program	Can be reset by Program
0160	SPI	Stop Program Interrupt	X	X
0161	ETI	End of Tape Interrupt (Allow End of File Signal to Interrupt)	X	X
0166	WEF	Write End of File	X	X
0167	WCC	Write Control Character	X	X
0170 - 0171	ETA ¹⁻²	End of Tape Alarm, Input-Output Converters No. 1 and No. 2	X	X
0174 - 0175	EOF ¹⁻²	End of File Alarm, Input-Output Converters No. 1 and No. 2	X	X

* These addresses correspond to the address of the In-Out Device being sensed. Busy Signals of In-Out Devices being sensed are not Flip Flops; they are voltage levels.

** Sense Flip Flops 7-16 are mechanized in all MOBIDICs other than B. In MOBIDIC B, these Flip Flops are simulated by routines contained in the reserved portion of the Magnetic Core Storage Unit.

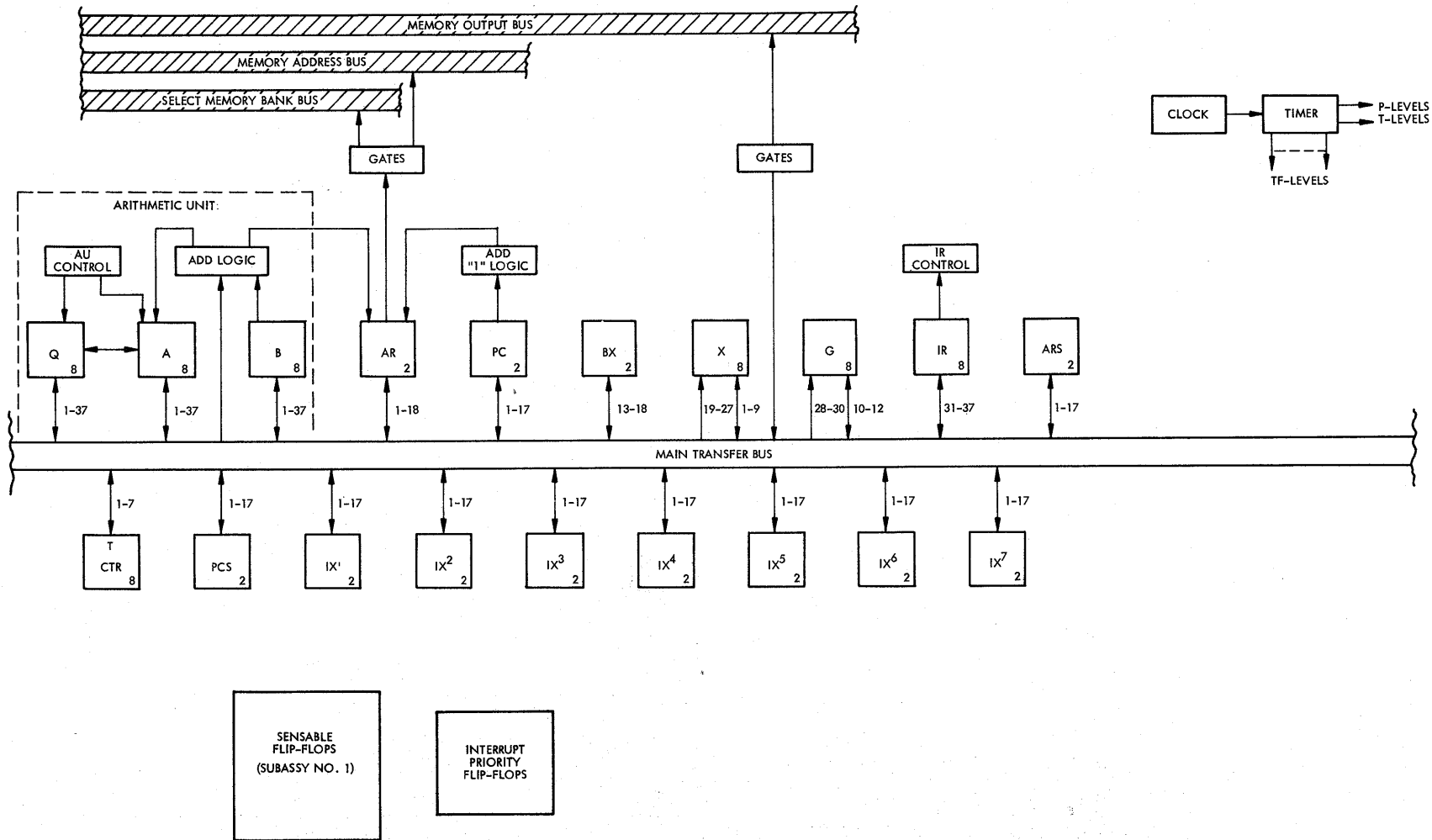


Figure A-1. Central Processor Register Block Diagram

Clock—The clock generates two-megacycle pulses that are applied to the timer.

Timer—The Timer accepts two-megacycle pulses from the clock and converts these through a commutating flip-flop to two square-wave outputs phased 180 degrees apart. These level outputs are distributed throughout the machine as the p and t timing levels. They are converted to p and t pulses before these signals are actually used in any of the pulse logic circuits. In addition to the p and t levels, the Timer generates sequential gating levels which identify the periods of a basic cycle.

Program Counter (PC)—The Program Counter (PC) is a 17-stage register that holds the address of the next instruction to be extracted from memory. Unless interrupted by a transfer, its contents will stop automatically through all of the memory cells in sequence.

T-Counter (T CTR)—The T-Counter is a 7-stage counter that is used as a shift control counter in shifting operations. It also serves for various other control purposes concerned with orders, such as multiply and divide, the implementation of which requires a counter.

Address Register (AR)—The AR provides temporary storage for the address specified by an instruction. This address is transferred to it from the B register via the adder-logic.

Should the instruction involve an index register, the contents of B are augmented by the contents of the specified index register in the transfer. Otherwise the address remains unchanged. The AR is also used as temporary storage in augmenting both Index Registers and the Program Counter.

X-Register (X)—The X-Register provides storage for the nine bits of the instruction word referred to as β . The specific use of β depends on the particular instruction being performed.

Index Registers (IX)—The Index Registers each have 17-bit capacity and are used to perform the following indexing operations:

1. They specify the number to be added to a programmed address to generate a relative address.

2. They specify the number of additional times that a particular programming routine is to be repeated.

Instruction Register—The Instruction Register is a 6-bit register which provides storage for the six operation code bits of the standard instruction word.

G-Register—The G-Register is a 3-bit register that provides storage for the γ bits until they are needed in the following memory cycle. The γ bits are used to address the Index Registers.

Control—The Control Section of the computer, under the influence of the outputs from the Decoder and the Timer, directs and controls the logical steps involved in the execution of the computer commands.

Arithmetic Unit—The Arithmetic Unit is composed of the A, B, and Q registers, the Add Logic plus the section marked AU-Control. The Arithmetic Unit is that section of the computer where the actual arithmetic and logical operations of the individual computer commands are implemented. The functions of the individual sections of the Arithmetic Unit are described below.

A-Register—The A-Register, or Accumulator, can be considered as the main register of the Arithmetic Unit. Most of the arithmetic or logical operations that the computer can perform involve either the existing contents of the A-Register or quantities which are entered in the A-Register before they are operated upon. In the four basic arithmetic operations, Add, Subtract, Multiply, and Divide, the Accumulator holds respectively, the sum, difference, product, and remainder resulting from the specified operation. At the beginning of the operations Add and Subtract, the A-Register holds the augend and minuend, respectively.

B-Register—The B-Register is an auxiliary register of the Arithmetic Unit that is generally used to hold one of the operands of an arithmetic operation. In the four basic arithmetic operations, Add, Subtract, Multiply, and Divide, the B-Register holds respectively the addend, subtrahend, multiplicand, and divisor.

Q-Register—The Q-Register is an auxiliary register of the Arithmetic Unit that finds its primary use in the operations Multiply and Divide. For these operations, the Q-Register holds the multiplier, low-order bits of a double-length product, low-order bits of a double-length dividend, and the quotient. It is also used as a

masking register for the "Mask" instruction. It can also be joined with the A-Register for double-length shift and cycle operations.

AU-Control—The section marked AU-Control contains the necessary logical circuits required to implement the arithmetic and logical operations that occur in the Arithmetic Unit.

Add Logic—The Add Logic is an adder network which forms the binary sum of the contents of the B Register and the data on the bus. Its outputs are gated either to A or AR.

Real Time Clock (RTC)—The RTC is a 17-bit binary number which is stored in a core memory location and is advanced automatically once per second from the One Second Source. Since it is a memory register, it is a fully addressable register.

Real Time Clock Compare Register (RCC)—The RCC is 17-bits in the other half of the core location assigned to the Real Time Clock which permits automatic interruption of a program at a preselected time. When the Compare Network shows that the RTC has attained the value stored in RCC, a program interrupt occurs.

Beta Extender (BX)—The BX Register is a six bit fully addressable register which augments the beta bits of a "Move" instruction. Since the "Move" order requires two full addresses of 18 bits, this register is necessary.

Add "1" Logic—This logic augments the contents of PC by 1 in transfer to the AR. The contents of AR are later transferred to PC. This advances the Program Counter.

Gates—Two sets of gates are used to correct the CP to the Memory Bus System. A bidirectional set allows the two way transfer between the Main Transfer Bus and the MO Bus. The other set gates the contents of AR onto the Memory Address Bus and the Select Memory Bus.

A. 1. 10 Time Charts

Figures A-2 through A-5 are typical time charts for CP operation.

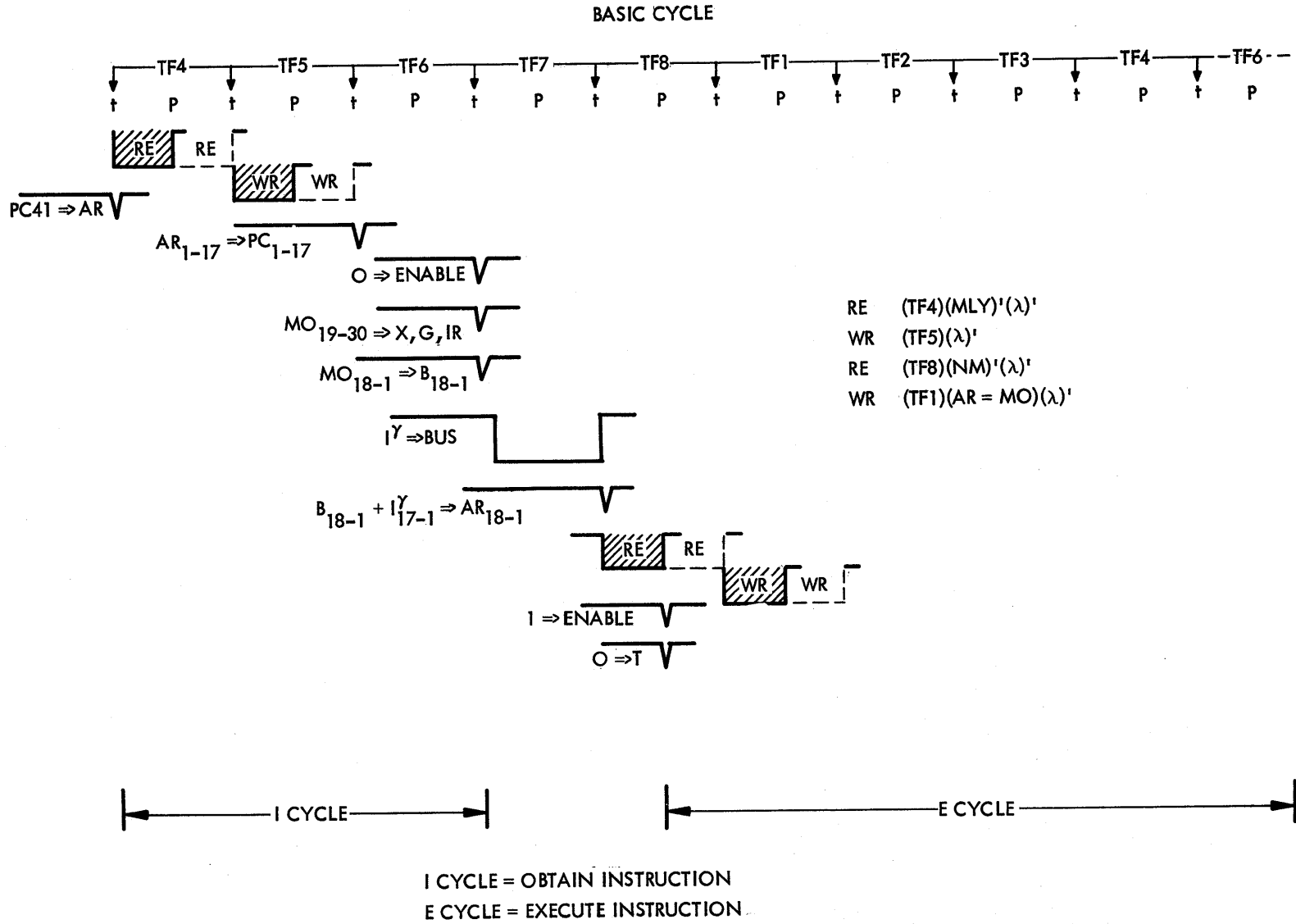


Figure A-2. Basic Timing Chart

ADD (BREG AND BUS)
 ASSUME SIGNS ARE DIFFERENT AND OF'

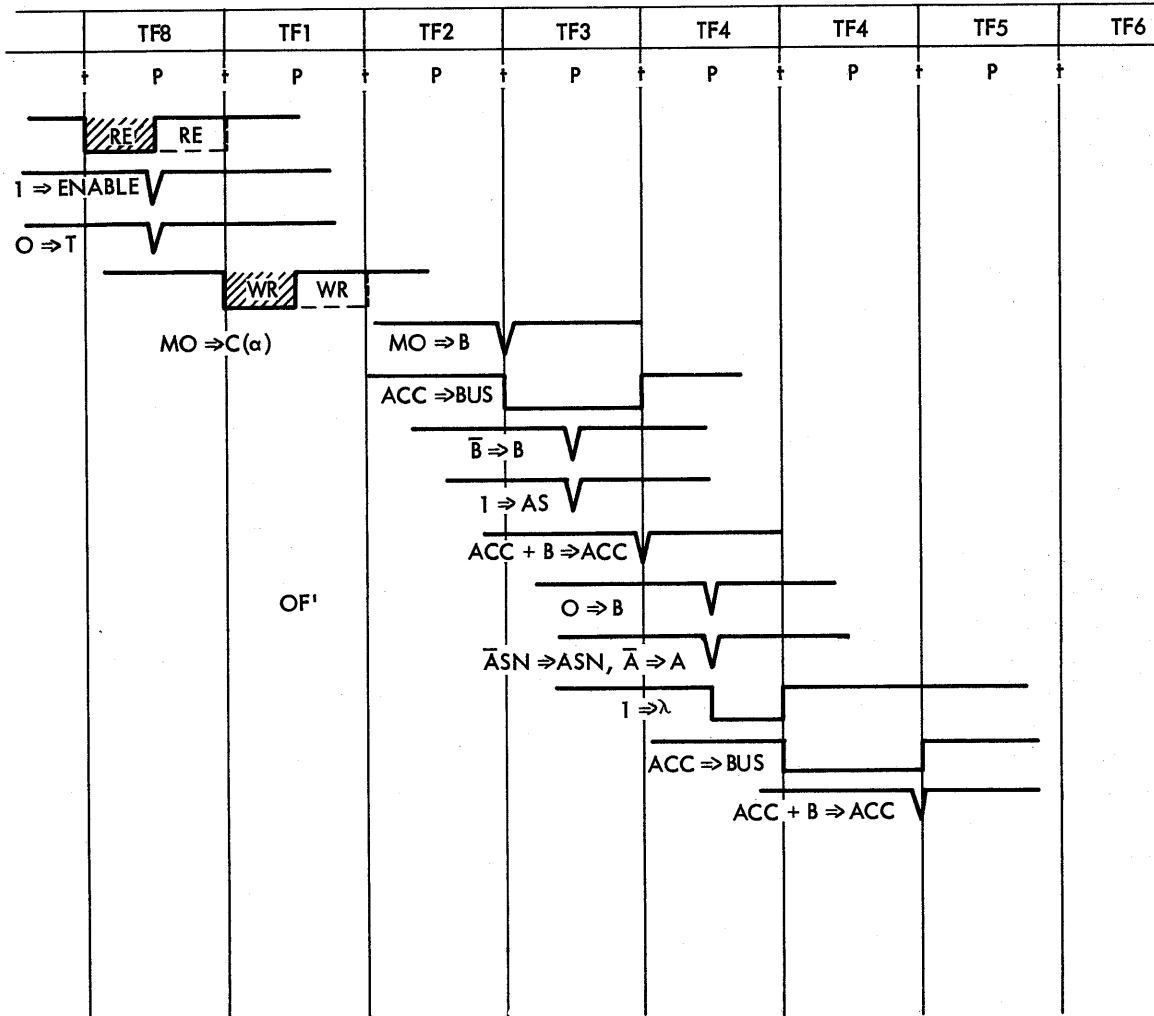


Figure A-3. "ADD" Timing Chart

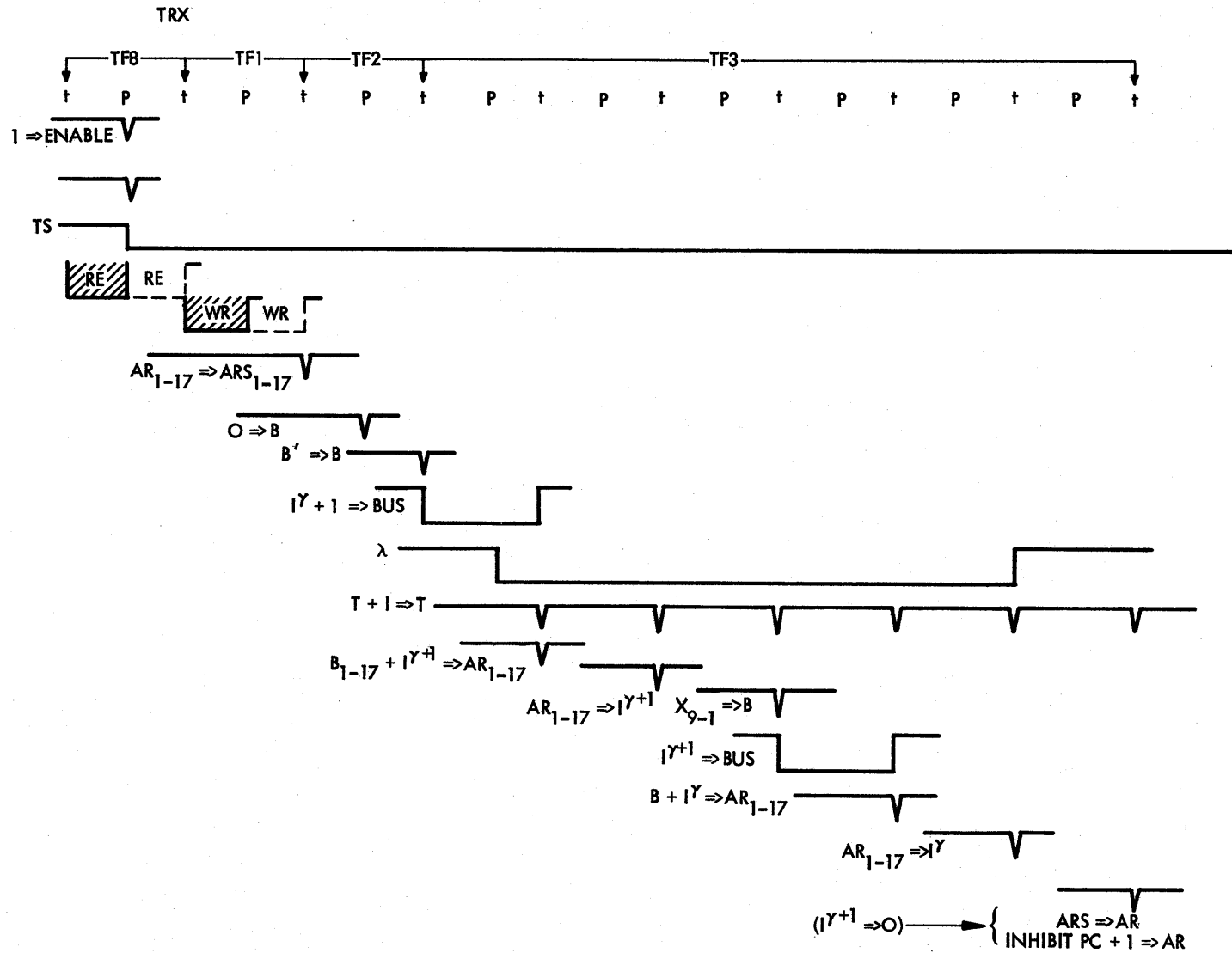


Figure A-4. "Transfer" Timing Chart

MOV - (RP')

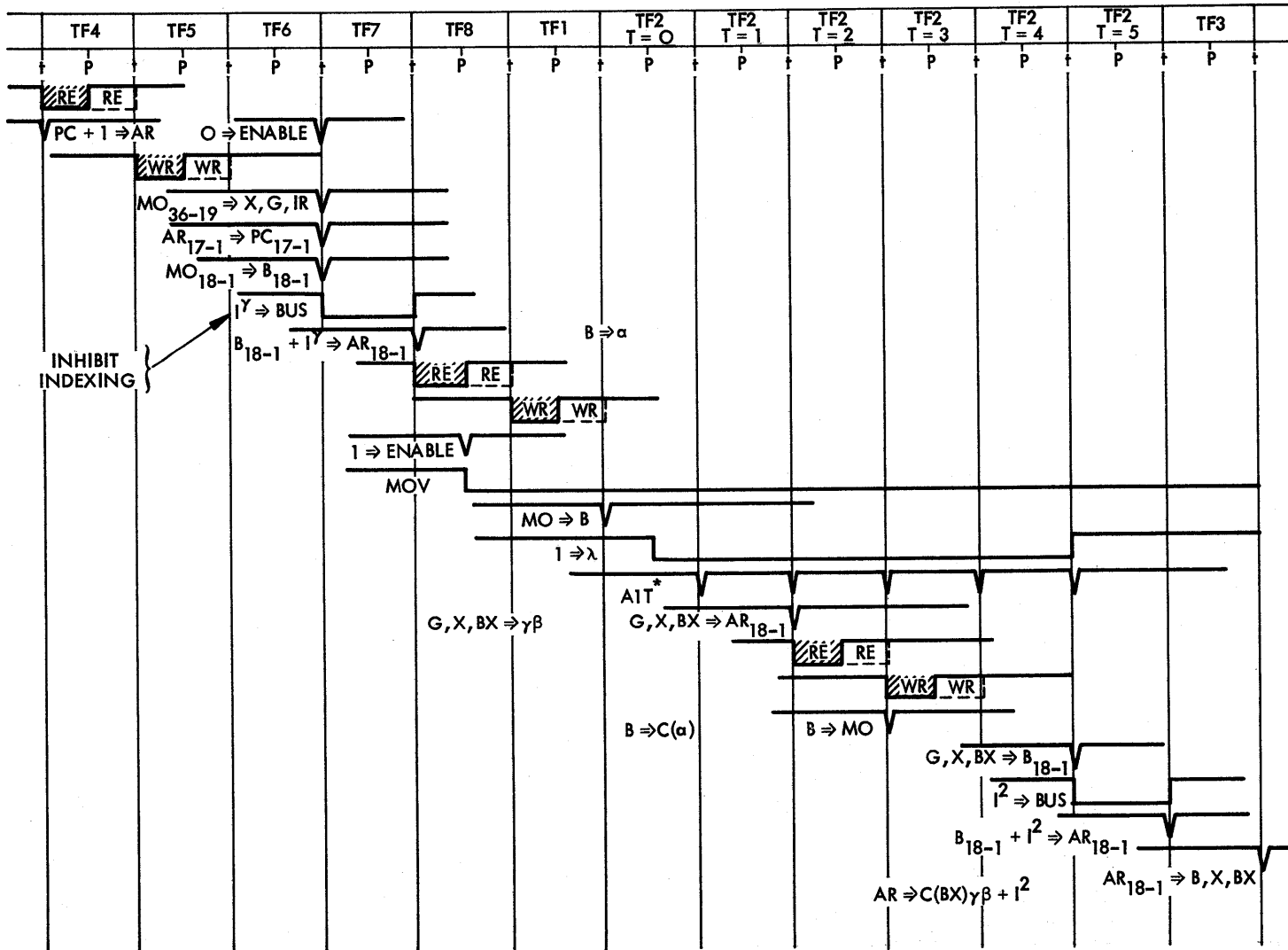


Figure A-5. "MOV" Timing Chart

A. 2 FUNCTIONAL DESCRIPTION OF ATACC INPUT/OUTPUT CONVERTER

The ATACC IOC is a data converter that controls device operation and data flow from one device to another. This is accomplished by assigning field locations in memory that serve to hold an I/O order for a particular device. These locations are called "control word locations" and they perform the same functions that were previously assigned to the CIS register of the MOBIDIC converter. By reserving a number of these control word locations, several devices can operate simultaneously, each controlled by its own instruction. On MOBIDIC, this would have required separate converters per device. But by performing identical functions in time sequence rather than by duplication of separate registers, simultaneous operation is economical in this embodiment of the ATACC IOC.

Operation is started by loading the in/out program and specifying an initial address where the program is to begin. The first instruction is examined and placed in the control word location for the device specified in the instruction. Once the control word is loaded, the device is started. Thereafter a system of busy bits is used whenever character transmission is required. When this happens, the appropriate control word is read-out of memory and interpreted in the IOC MO to discover the proper disposition of the character.

By assigning additional starting locations, several devices can be made to operate simultaneously. When several devices are in operation, busy bit processing acts as the traffic controller by selecting the device with the highest priority first.

Whenever the present instruction in the control word location is completed, the next order in the in/out program is read and placed in the proper control word location. Thus any device is controlled in a logical sequence of steps that is completely under program supervision.

Although orders are taken from sequential locations, provision is made for multiple entries and multiple branching so that, in effect, several independent programs are running concurrently. The action is similar to having many program counters operating at the same time. This also permits interlocking several independent programs in a more sophisticated arrangement. For example, if it is

necessary to punch cards and print two reports with different formats, all from the same magnetic tape data, individual programs for each device and format are linked together to provide this effect.

A. 2. 1 Internal Organization

The basic ingredients of any I/O system are instruction control, instruction storage, and data buffer storage.

Instruction performance is accomplished by control words that are stored in memory locations specifically assigned to a particular device. The various fields of the control words specify the following:

1. OP code—the operation that is to be performed (read, write, punch, print, etc.).
2. Address—This field specifies the memory locations of the ATACC IOC from which or into which data are to pass.
3. Word Count— This field specifies the number of words that are to be processed by this instruction.

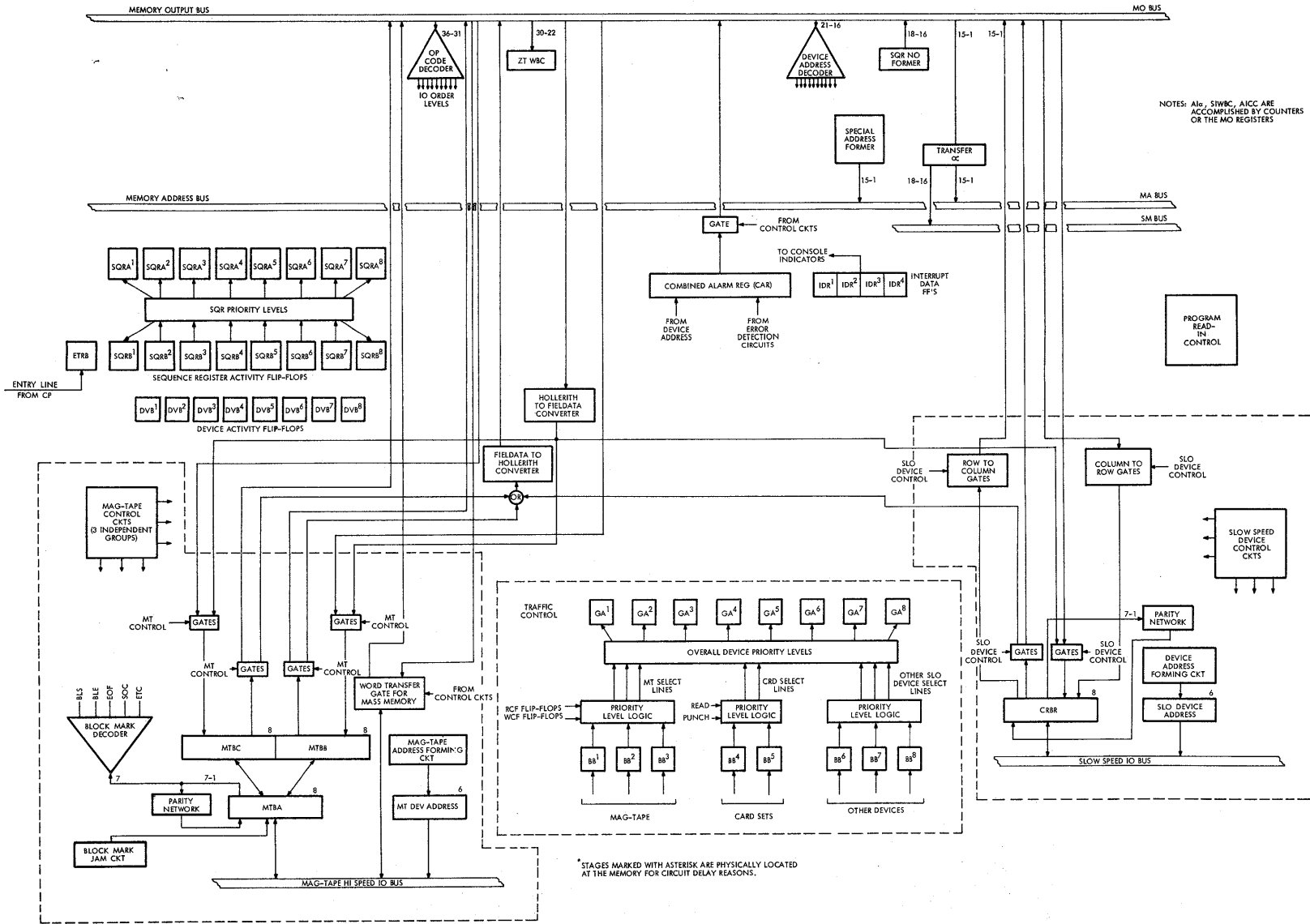
A. 2. 2 Input/Output Converter Operation

Figure A-6 is a block diagram of the IOC. A description of the block diagram and theory of operation follow.

Traffic Control Section—This section controls the selection of the device to be processed next by the ATACC IOC. It is composed of Busy Bit (BB) flip-flops, Go Ahead (GA) flip-flops and priority selection level logic.

Busy Bits—Associated with each device is an inverter type flip-flop which stores the fact that either a strobe level has been received from a device which is in process of reading (indicating that it is ready to transmit a character), or that the IOC has a character to transmit to a device and that devices' ready is raised.

Go Ahead Flip-Flops—Associated with each device is an inverter type flip-flop which, when set, indicates that that device has been selected for processing.



NOTES: AIC, SIWBC, AICC ARE ACCOMPLISHED BY COUNTERS OR THE MO REGISTERS

Figure A-6. ATACC Input/Output Converter System Block Diagram

Priority Level Logic – There are three groups of priority level logic which are designated by relative device speeds; Magnetic Tape, Card Reader-Punch, and other devices. Within each "speed" group the logic is implemented to select that device which is reading before a device which is writing. No more than one device select line from each group is raised.

Overall Device Priority Levels – The device select lines from each "speed" group are sampled and the device of the highest speed is selected by setting its corresponding "Go Ahead" Flip-Flop.

Magnetic Tape Section – This section controls the processing of magnetic tape information to and from up to three magnetic tape transports simultaneously. It contains three independent groups of logic, each of which contain the following stages:

MTBA, MTBB, MTBC – These three magnetic tape 8-bit character buffer registers are of the inverter flip-flop type (six data bits, plus control and parity bits to make up a fielddata character). Upon reading magnetic tape, characters from a transport enter MTBA and are alternately gated to MTBC and MTBB. When MTBC and MTBB are both filled the corresponding BB is set notifying the Traffic Control that the device is ready for processing. These character buffer registers have transfer in and out functions only. MTBA is also used in sensing or forming block marks and is the register in which parity is both checked and formed. Associated with MTBC and MTBB are transfer gates for a 12 bit transfer to and from Memory Buses of two characters into the memory location specified by a portion of the Device Control Word.

Hollerith/Fielddata Converters – Associated with processing of characters in the off-line mode of IOC operation are two code converters. These converters are used when transferring information from punch cards containing information punched in the Hollerith 12-bit code in column form to an output device where information is stored in Fielddata form and vice versa. Since the information will be stored in memory in Hollerith Code column form the punched card the H-F code converter is inserted in the transfer of data characters from the Memory Output Bus to the MTBC and MTBB character buffer registers or CRBR register while transmitting to an output device during off-line processing. The H-F code converter is inserted between the character buffers and the Memory Input Bus while receiving from an input device.

H-F Converter – During the H-F conversion operation each Hollerith character is presented to the converter which generates binary "ones" in appropriate positions as necessary to produce the equivalent Fielddata character with bit 7 always being a "one" since the characters are always data. The 8th bit is formed to produce overall odd parity in the character.

F-H Converter – During the F-H conversion the Fieldata character after having transferred up through the character buffers is presented to the inputs of the H-F code converter which generates "ones" in the appropriate bit positions as necessary to produce a Hollerith code character equivalent to the Fieldata coded character. The Hollerith character is then transferred to Memory via the Memory Input Bus to the location specified by a of the Device Control Word.

MT Device Address Register – A 6-bit flip-flop register of the inverter type used for holding the address of the selected magnetic tape transport during the Device Control Word processing cycle. The outputs of these flip-flops are connected to the MT input-output bus through Cable Drivers and bear the same meaning as Mod I IOC as far as the address "gating" the functions in the Device Switching Unit.

MT Address Forming Network – A special address forming network is required to place the correct device address in the above described flip-flop register inasmuch as a 6-bit device address will not be available as part of the IO instruction present during the Device Control Word processing cycle. That 6-bit portion of the instruction which previously held the device address will be used to designate Sequence Control Registers and Character Counts instead and a DVB activity flip-flop associated with each Device Control Word will be sensed and an appropriate 6-bit device address will be formed in the MT Address Forming Network.

Block Mark Decoder – The characters passing through MTBA are sensed for block mark configurations for purposes of MT Control timing while processing magnetic tape. A decoder is connected to the outputs of the flip-flops in the register for purposes of detecting Block Starts, Block Ends, End of File, Start of Control Block, and End of Control Block marks. These marks are decoded only when the 7th bit is a "zero".

Block Mark Jam – This circuit forms the above mentioned Block Marks and gates them into MTBA while writing magnetic tape. This is done at appropriate times at the beginning and end of blocks of data transfer, according to timing levels provided by Magnetic Tape Control, since block marks are not stored in memory.

Parity Network – The parity network samples bits 7 to 1 of the MTBA character buffer register and compares to the 8th bit of an input character to verify overall odd parity while receiving characters from the device. While transmitting a character to a device bits 7 to 1 are sampled and the 8th bit is set or reset to create overall odd parity.

Magnetic Tape Control Circuits – This section contains all of the pulse and level logic involved in the control of high-speed devices. The control circuits generate character and block-mark timing, and interblock timing during starting and stopping of the device, as well as generating device command levels which drive the IO Bus Lines.

Slow Speed Device Section – This section controls the processing of information for the relatively slow speed devices such as Card Reader-Punch Sets, Paper Tape Sets, Line Printer, Flexowriter, etc., and contains the following stages.

CRBR – A single 8-bit, inverter flip-flop register which performs a storage function for single characters communicating between memory and the slow speed devices. There are transfer gates to route characters from CRBR to the appropriate portions of the memory word specified by the character count via the Memory Input Bus while reading a device and likewise from portions of the Memory Output Bus to CRBR while writing.

Slow Device Address Register – A 6-bit inverter type flip-flop register which holds the address of the selected device and whose outputs perform the same gating functions in the DSU as with the Mod I IOC.

Slow Device Address Forming Network – Performs the same function as it does in the Magnetic Tape Section. A 6-bit device address is formed by this network as determined by the DVB flip-flop which is associated with the Device Control Word being used in the current processing cycle.

Parity Network – Identical to the one described for magnetic tape processing, for checking and forming parity.

Row-to-Column Gates – These gates route bits from CRBR register to the Memory Output Bus while reading cards which have been punched in Column Form. They provide for selective storing of bits into a memory word while the Memory Address is being incremented so that the final set of memory locations read into will contain information from the card in column form.

Column-to-Row Gates – The reverse process applies here in that as the memory address is being sequenced through locations in memory which contain card information in column form which is to be punched, selective readout is accomplished by these Column-to-Row Gates from the Memory Output Bus to CRBR to be sent to the card punch to be punched by Rows.

Slow Speed Device Control – This section contains all of the level and pulse logic associated with the control of slow speed devices, including Ready/Strobe circuitry for proper character timing, as well as error detection circuitry. All of the levels which drive the IO Bus Lines for starting, stopping and otherwise controlling the devices are generated here.

Flip-Flops Associated with Simulated Registers—All of the full word length registers associated with the control of the ATACC IOC are simulated in memory. These are the Device Control Word Registers (DCW), Sequence Control Registers (SQR) and Entry Register (ETR). There is a flip-flop or group of flip-flops assigned to each of these registers or group of registers which are used as activity and status indication to the control circuitry which makes decisions about the operation cycle to take place next.

Device Busy Flip-Flop (DVB)—Associated with each of the eight Device Control Word Locations in memory is a register-type flip-flop which is used to indicate that the device is in use. The DVB flip-flop is cleared when Word Block Counter portion of the In/Out order contained in that register has reached zero.

Sequence Control Register Flip-Flops—Associated with each one of the eight Sequence Control Registers in memory are two register-type flip-flops. One indicates that the register is in use (SQRB). The other (SQRA) indicates which one has been selected for the next operation, similar in use to the GA flip-flops in the Traffic Control Section.

Entry Flip-Flop (ETRB)—Assigned to the Entry Register (ETR) is a register-type flip-flop which is used to indicate that an IO order has been entered in ETR by the Central Processor.

Program Read-In Control—As part of the off-line operation it is necessary to have a Program Read-In feature in the ATACC IOC, independent of the Program Read-in from the Central Processor. This section contains all of the necessary circuitry to automatically read from cards and/or paper tape information regarding the device from which the program is read in, the starting memory location into which the program will be stored and an address where the program will be started upon completion of the Program Read-In operation.

Combined Alarm Register (CAR)—The Combined Alarm Register is composed of IO alarm flip-flops of the inverter type. They will include at least the following: DVA (Device Alarm), ISE (Interpret Sign Error), IPE (Input Parity Error), and a 6-bit address. If any one of the above type of errors is encountered during a character processing cycle the appropriate flip-flop is set, the device address is transferred into the register, and the register is stored into a reserved location in memory. An IDR (Interrupt Data Flip-Flop) flip-flop is set corresponding to which one of four reserved memory locations is used to store the error information.

Input-Output Instruction Logic—During the Device Control Word processing cycle the control word is contained in the MO register of the memory bank utilized by the ATACC IOC. Various stages exist between the three Memory Busses which sense parts of the IO order in the DCW and which modify parts of the DCW. The IO instruction logic consists of the following stages:

OP Code Decoder— This decoder is attached to the Memory Output Bus lines corresponding to the Op code bits to provide decoded levels corresponding to all the standard MOBIDIC IO instructions including the Start Order Sequence order. A few other instructions will be decoded for the IOC such as MOV and TRX.

Zero Test Word Block Counter (ZTWBC)—Decodes for the k-portion of the instruction word reaching zero indicating that the last character has been processed. This decoder is attached to bits 30-22 of the Memory Output Bus.

Subtract One Word Block Counter (S1WBC)—This circuit samples the k portion bits 30-22 of the DCW via the Memory Output Bus and transfers the contents minus one into the corresponding bits of the Memory Input Bus.

Character Counter (CC)—A four-bit binary counter consisting of register-type flip-flops is provided to store the number of characters which have been processed under the current Device Control Word. A part of the j-portion of the instruction word which is used for character counting is transferred via the Memory Output Bus into CC. Add-one logic is provided for updating the count. The result is gated onto the Memory Input Bus for insertion of the updated count into the Device Control Word.

Device Address Decoder—This decoder is attached to the Memory Output Busses corresponding to the j-portion of the IO instruction word for decoding the input-output device specified by the order.

Add One Alpha (A1 α)—The incrementing of the memory address portion of IO orders is accomplished by this circuit whose inputs are attached to the Memory Output Bus lines corresponding to α . The updated count is transferred onto the same lines of the Memory Input Bus.

Transfer Alpha—A network which accomplishes the transfer of the α -portion of the IO instruction from the Memory Output Bus (from the DCW contained in MO) to the Memory Address Bus for purposes of addressing data locations. It is also used to specify instruction locations in SOS orders.

Sequence Control Register Number Former—A network which forms the binary number corresponding to the SQRA flip-flop which is currently in the "one" state. The number is transferred into part of the j-portion of the IO order now in the MO register by way of the Memory Input Bus. This makes possible the return to the corresponding SOS order (in that SQR location) of which the current IO order is a part.

Special Address Former—A network which forms all of the addresses of the reserved locations in memory used by the ATACC IOC, including Entry Register (ETR), Sequence Control Registers (SQR), Device Control Words (DCW), and Interrupt Data Registers (IDR). The addresses are transferred onto the Memory Address Bus.

Parity Network—A full word-length network which samples 37 bit parity and forms the 38th bit to form overall odd parity in the word when forming parity or which compares the 37-bit parity against the 38th bit when checking parity during core memory access.

Physical placement of some of the above described stages in proximity to the MO register is necessary.

In the add one and subtract one carry chains in some instances there is only one microsecond in which to sample the outputs of the MO, modify the number and transfer the updated number back to the MO. This would present problems if done over the memory bus system. These stages which are part of the ATACC IOC but are located at the memory are indicated by notes on the System Block Diagram.

A. 2. 3 Internal Organization

The detailed operation of the ATACC IOC centers around the manipulation and interpretation of instructions and addresses, located in three areas of the memory.

1. The Device Control Words (DCW) Address $(000200-277)_8$ —
These are locations that hold the data address, word count, and OP code that are needed to control the data traffic to and from the device associated with the DCW.
2. The Sequence Control Register (SQR) $(000010-17)_8$ —These
Reserved locations of which there are eight in number, serve to hold the addresses from which the IO orders presently being performed were located. Their function is similar to that of program counters.

3. The Entry Register (ETR)—This memory location address, (000020)₈, is reserved as a temporary and initial repose for IO instructions or sequence commands that emanate from the main program.

Action is initiated whenever an "start order sequence" order is encountered during the execution of a program in the CP.

The following steps take place in the ATACC IOC:

1. The CP stores the sequence order in the Entry Register (ETR) and sets a flip-flop (ETRB).
2. If this is a sequence order, (SOS), select a free Sequence Register (SQR) and store the order in that location.
3. The address portion of a Sequence Order (SOS) specifies where in memory individual input/output instructions are stored sequentially, so that the ATACC IOC reads out of memory the contents of the location as specified by the address field of the Sequence Order.
4. The device address field of the instruction, thus, read out of memory, is examined to determine if the desired device is free.
 - a. If it is busy, a flip-flop is set and action indicated in (3) above is repeated at some other time.
 - b. If it is free, the instruction is stored in the DCW associated with that device.

In order to correlate the IO command with the proper SQR, a three-bit code, that defines the proper SQR is inserted in the device address field of the IO instruction. This does not create any ambiguity because the DCW location is related to a device, so that the address in the device field is no longer needed. The purpose for tagging the DCW with the SQR location is to provide continuity in the IO program. Thus, when the word count reduces to zero, signifying that the present IO command in the DCW is completed, reference to the appropriate SQR is made. The contents of the SQR contains the Order Sequence Instruction (SOS), the address of which (after being incremented) now specifies the location in memory where the next IO command is to be found. The actions described under part (3) above are now repeated.

The gross effect that these detailed operations produce is an IO system that can execute several independent IO programs, each initiated by a separate sequence order whenever it is sent to the entry register. Although the text above has described the events in the IOC when a sequence order is sent from the Main Program in the Central Processor, sequence commands can also be initiated and entered into the IOC through an off-line console; thus IO programs for Off-Line use can be entered in the memory and can be run concurrently with On-Line Programs by the IOC. In order that no conflicts occur, a single bit in all IO commands initiated by an Off-Line sequence order is coded so that only peripheral devices switched to Off-Line can be operated, and vice versa.

Thus, the IOC handles several devices simultaneously in complete harmony, each under control of an independent IO sequence that has been initiated, and will service the IO needs of either the main On-Line program or Off-Line operation.

IO Field Assignments

In order to retain the necessary control information such as address, device, SQR, character count, interpret sign, Hollerith conversion, and operation mode, the IOC assumes the following field definitions:

1. For the Order Sequence Instruction (SOS)

OP	-	a
----	---	---

(c) (b) (a)

- (a) The address field—eighteen bits in length defines the location in memory where a sequence of specific IO commands are locations.
- (b) Not used.
- (c) The OP code field—six bits in length defines the SOS instruction.

2. For the standard MOBIDIC IO instruction when used in the main program or when the MOBIDIC address field compatibility switch is set, the format is as follows:

OP	k	j	a
----	---	---	---

(d) (c) (b) (a)

- (a) The address field (a) – fifteen bits in length, defines the location in memory from which or into which data is to go.
- (b) The device address field (j) – six bits in length, defines the device that is to be used.
- (c) The word/block count (k) – nine bits in length, defines the number of words or blocks that are to be processed by this instruction.
- (d) The OP code field – six bits in length, defines the type of instruction (i. e. , read, write, etc.).

3. For IO control commands stored sequentially for use with the sequence order, the format is as follows:

OP	OFF	ax	k	j	a
----	-----	----	---	---	---

(f) (e) (d) (c) (b) (a)

- (a) The lower address field (a) – fifteen bits in length, defines the lower order address bits for the locations from which data is to be transferred.
- (b) Device address (j) – six bits in length, defines the device to be used.
- (c) Word/block count (k) – nine bits in length, defines the number of words or blocks to be processed.
- (d) Alpha extender (ax) – three bits in length, together with the a bits it forms a seventeen-bit memory address.
- (e) Off-Line Bit – one bit, that indicates that this command is a part of the off-line program, and may actuate the device when the device is set to off-line mode.

4. After internal manipulation by the IOC, the format of the individual DCW locations are modified to include SQR, Hollerith characters, and off-line control. The format internal to the DCW is as follows:

HF	OP	OFF	αx	k	cc	SQR	a
(h)	(g)	(f)	(e)	(d)	(c)	(b)	(a)

- (a) Address field (a)—same as in 3(a) above.
- (b) Sequence register field (SQR)—three bits in length, this field defines which SQR register contains the address from which subsequent IO commands are to be taken.
- (c) Character counter (cc)—three bits in length, this field is used to keep track of which character or characters of the data words are being processed. The SWR and CC fields of the DCW occupy the bit positions of the device address field. This is possible because the address of the device control word (DCW) is uniquely associated with the address of the device. Therefore the device address need not be carried as part of the DCW and those bits may be used for other purposes. (i. e. , SQR, and CC)
- (d) Word/block count (k)—same as in 3(c) above.
- (e) Alpha extender (αx)—same as in 3(d) above.
- (f) Off-Line Bit—same as 3(e) above.
- (g) OP code—same as 3(f) above.
- (h) Hollerith-Fielddata bit—the sign of the command is set if Hollerith-to-Fielddata conversion is required for off-line operation or vice versa.

A.3 BASIC MEMORY AND MEMORY SUPPLEMENT DESCRIPTION

Figure A-7 shows a block diagram of the Basic Memory and Memory Supplement Drawers. Both are two-microsecond coincident current core memories. Note that the Basic Memory Drawer has all controls and registers necessary to operate by itself, while the Memory Supplement can only operate in conjunction with the Basic Memory.

Considerable use is made in the memory design of transformers for driving and sensing. This technique results in savings in numbers of drivers and sense amplifiers. It also reduces to a minimum bias voltages on core stack windings, a source of corrosion difficulties in past memory designs.

While it is impossible to give a complete set of drive schematics without filling another volume, the following brief descriptions help to illustrate the techniques. The descriptions are for eight memory arrays of 4,000 words each.

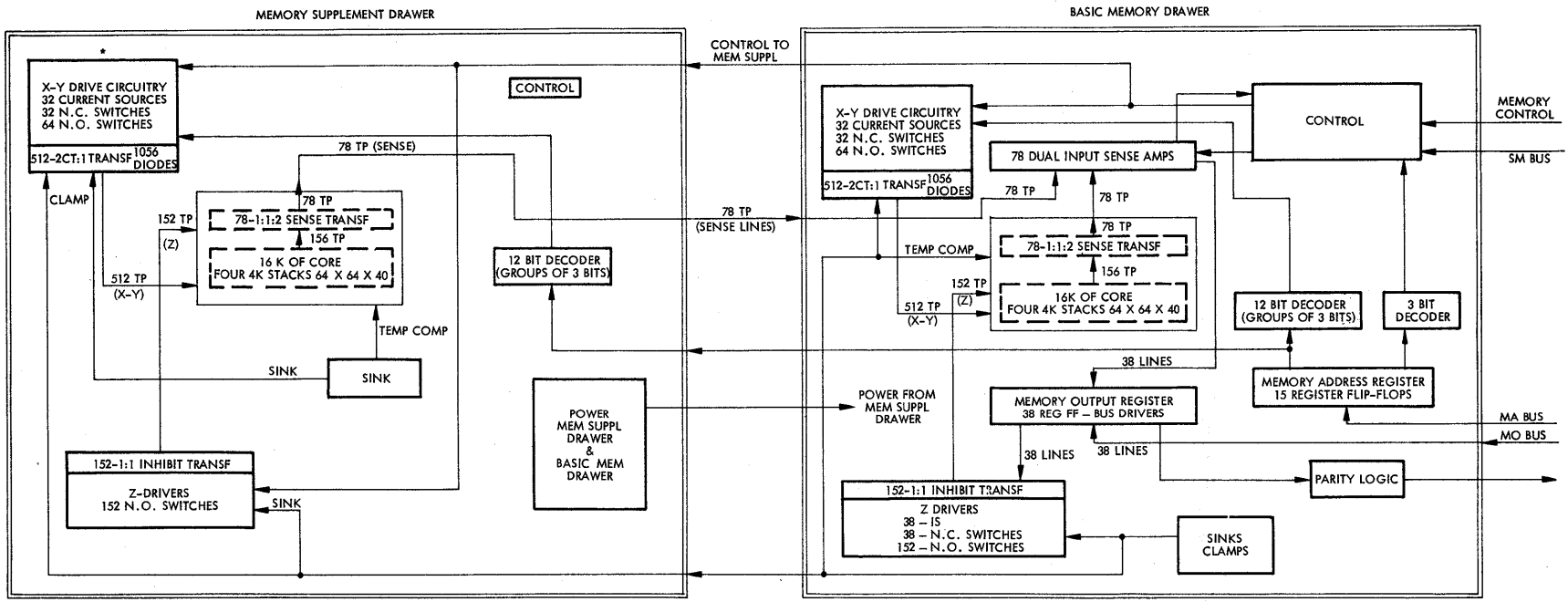
X-Y Drive—Each X and Y drive line of each stack has a single transformer, with a center tapped primary, for read and write drive. Figure A-8 shows a section of the drive line selection scheme for one coordinate of one stack. The sources and switches are shared between stacks in such a manner as to uniquely select one line of one stack.

Inhibit Drive—The inhibit line of each plane has a transformer for inhibit drive. Figure A-9 shows the connection of the transformers to a current source, normally-closed switch and normally-open switches.

Sense Amplifiers—Each sense line from each plane goes to the primary of a Sense Amplifier Input Transformer as shown in Figure A-10. Notice that the transformer inputs are selected in such a way that if one input is fully selected, the other input is not half-selected.

A.4 CONSOLE AND CONTROL PANELS

This section discusses the Operator's Console, the Off-line Control Panel and Auxiliary Control Panels for on-line and off-line uses. The Operator's Console Panel is shown in Figure A-11. The following displays and indicators are used on this panel.



* CT-CENTER TAP
TP-TWISTED PAIR

Figure A-7. Memory Block Diagram

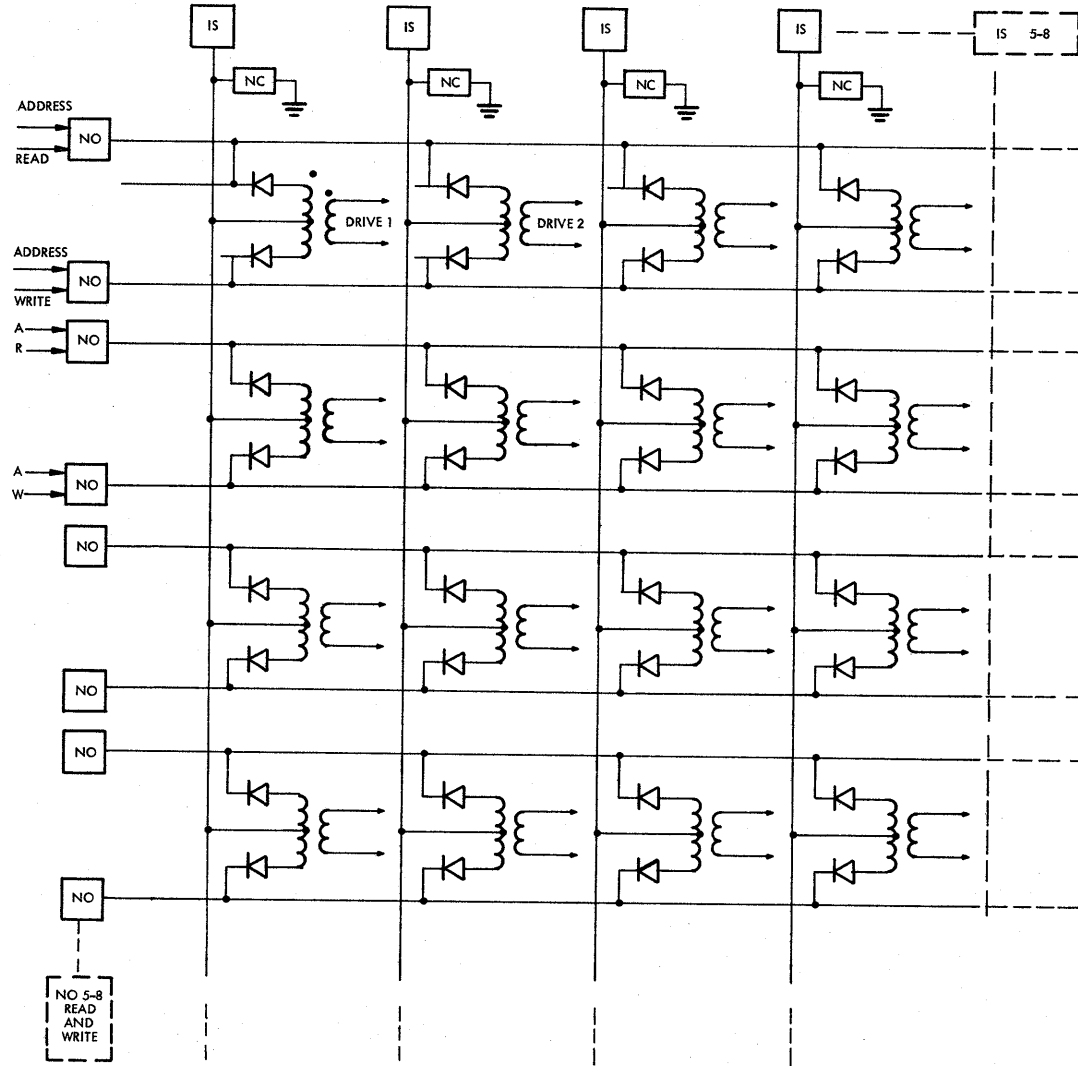


Figure A-8. Drive Line Selection Schematic

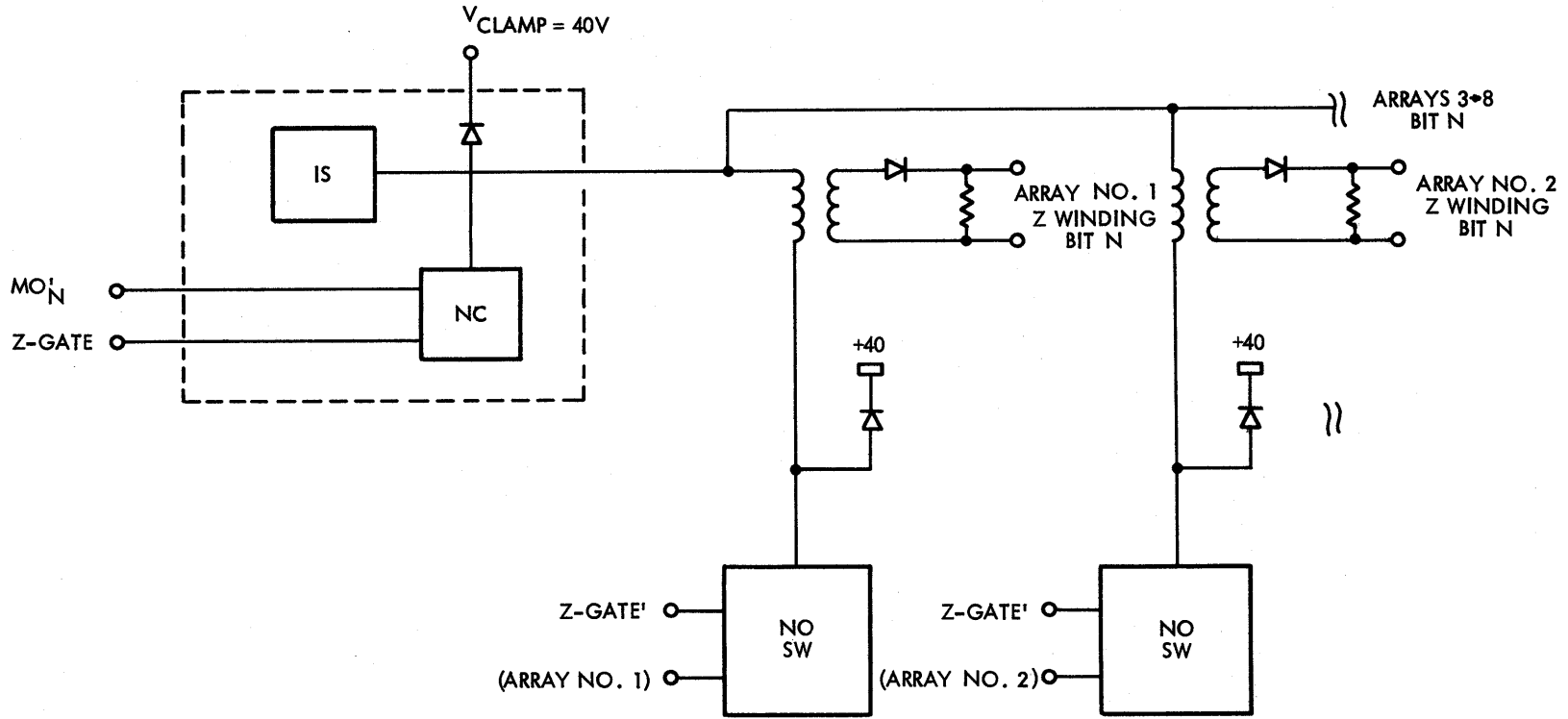


Figure A-9. Inhibit Drive Schematic

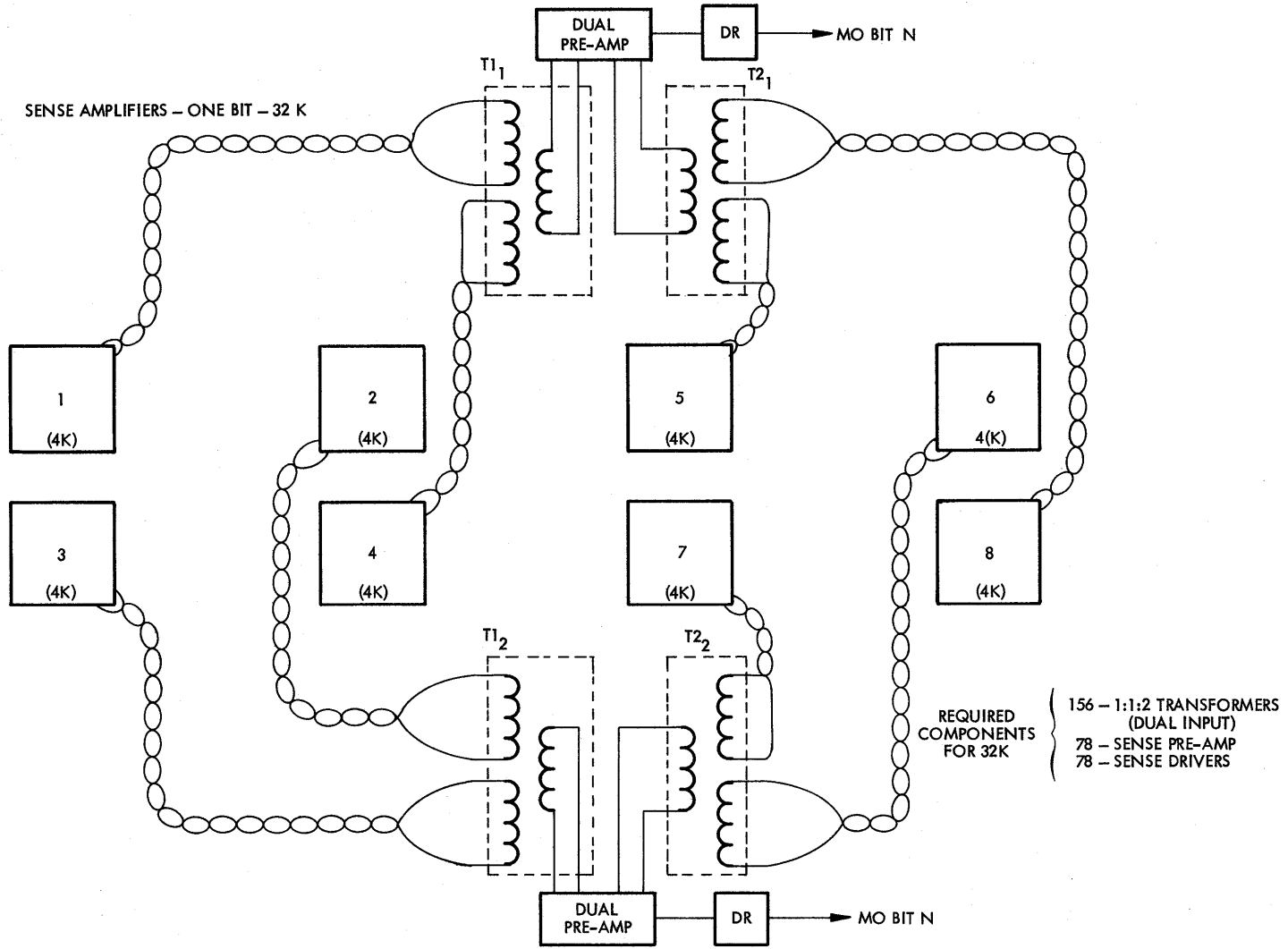


Figure A-10. Sense Amplifiers Schematic

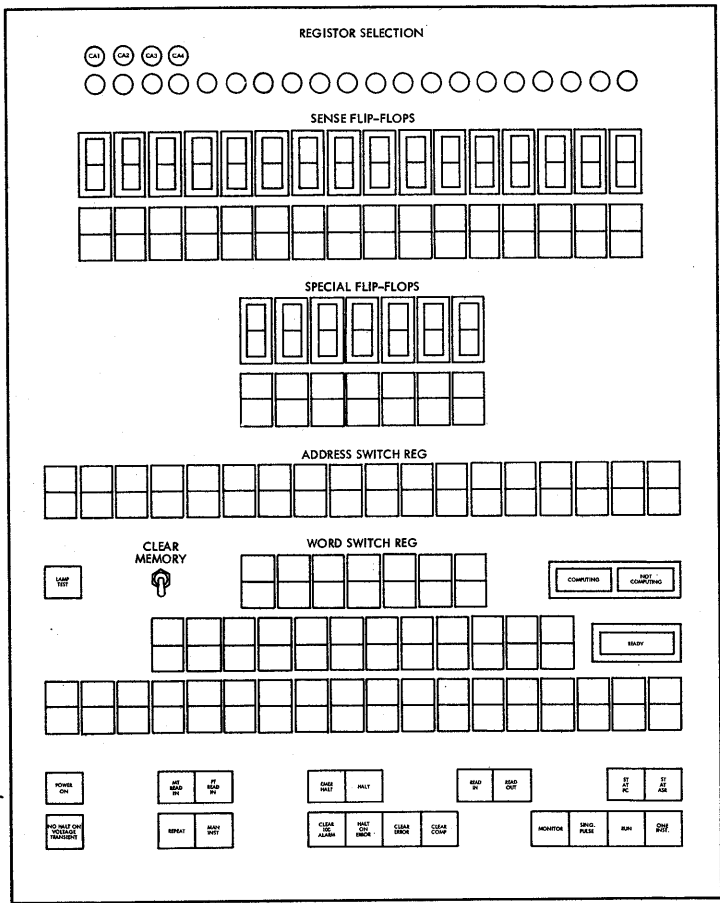
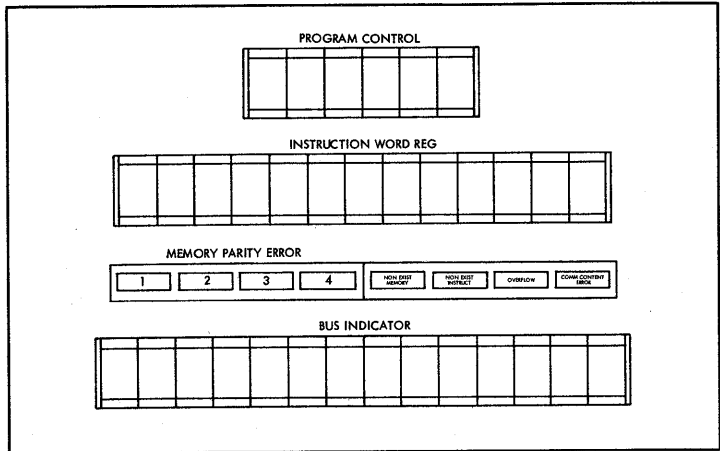


Figure A-11. Control Panel Drawing

A. 4. 1 Displays

A. 4. 1. 1 Nixie Tube Octal Displays

Each Nixie tube will be packaged in an assembly containing a binary coded decimal-to-octal converter circuit and drive circuits in addition to the tube. Each assembly is covered on the front panel by a bezel which contains a protective glass and a Polaroid filter to improve character legibility. The contents of the following registers will be displayed on Nixie tubes.

IWRL—The Instruction Word Register displays (made up of IR + G + X + AR) the last instruction performed by the computer. The thirty-seventh bit of the IWR is the sign bit. This is signified by a plus (+) or a (-). This register is displayed all of the time.

GXRL—The Alpha Extender Register displays the memory bank address of the last instruction performed by the computer. This register is displayed at all times.

PCL—The Program Counter displays the locations from which the next order will be taken. This register is displayed all of the time.

BIRL—The contents of the following eighteen registers can be displayed in the Bus Indicator Register:

- | | |
|--|---|
| 1. A Register (A) | 10. Index Register No. 7 (IX ₇) |
| 2. B Register (B) | 11. Memory Output (MO) |
| 3. Q Register (Q) | 12. Real-Time Clock Compare (RCC) |
| 4. Index Register No. 1 (IX ₁) | 13. Real-Time Clock (RTC) |
| 5. Index Register No. 2 (IX ₂) | 14. Program Counter Store (PCS) |
| 6. Index Register No. 3 (IX ₃) | 15. Converter Alarm Register 1 (CA ₁) |
| 7. Index Register No. 4 (IX ₄) | 16. Converter Alarm Register 2 (CA ₂) |
| 8. Index Register No. 5 (IX ₅) | 17. Converter Alarm Register 3 (CA ₃) |
| 9. Index Register No. 6 (IX ₆) | 18. Converter Alarm Register 4 (CA ₄) |

The register selection is provided by the Register Selection Switches located below the Bus Indicator Register. Each one of eighteen switches controls

one of the registers listed above. The Memory Output Registers can be used to monitor any word in memory after first transferring that word from memory to the appropriate Memory Output Register. This transfer can be achieved manually by means of the Address Switch Register and the Read-Out Switch. The sign, bit 37, is signified by a plus (+) or a minus (-) sign. Bit 38, the parity bit, is displayed by a zero (0) or one (1).

A. 4. 1. 2 Incandescent Displays

Computer Error and Alarm Conditions

NXIL—Non-Existent Instruction lamp on indicates the Operational Code portion of the Instruction Word being operated on has not been assigned and is non-existent.

NXML—Non-Existent Memory lamp on indicates the Program Counter and Alpha or Gamma Extender are addressing a non-existent memory.

OAL—Overflow Alarm lamp on indicates the Overflow Alarm flip-flop has been set.

MPEL—Memory Parity Error lamp on indicates even parity has been detected in the Memory Output Register.

CAL 1-4—One of the four Converter Alarm lamps illuminated indicates that a memory location reserved for storage of converter errors has been loaded. There is one memory location reserved for each of the four Converter Alarm lamps. The contents of the memory location can be displayed on the Bus Indicator Register by depressing the Register Selection Switch which is imprinted with the same name as the Converter Alarm lamp illuminated.

CCPEL—The Communications Converter Parity Error lamp on indicates even parity has been detected in the Communications Converter.

Power Status Indicator

RDYL—The Ready lamp on indicates the computer is ready for use. The computer is ready when the following conditions are achieved.

1. A-C power on.
2. D-C power on.

3. Peripheral power on.
4. No voltage transient has occurred when the Non-Halt-on-Voltage-Transient button is released. The Non-Halt-on-Transient button is an alternate action pushbutton.

When the button is locked in and a voltage transient occurs, the computer will not be halted and the Ready lamp will not be extinguished. When the Ready Indicator goes out, the console operator must look at the front of the a-c control enclosure to determine what condition must be corrected.

Computer Status Indicators

COMPL—The Computing Indicator which is tied to the prime side of the Halt flip-flop, illuminates when the machine is in a computing state.

COMPL—The Non-Computing Indicator is tied to the one side of the Halt flip-flop and indicates the compliment of COMPL above.

Sense and Special Flip-Flop Indicators

SFFL 1-16—There will be one indicator per Sense flip-flop. The indicator will be divided into two halves. Illumination of the upper half will indicate a set SFF and illumination of the bottom half a reset condition for the same SFF.

Special Flip-Flops—The following is a list of split indicators which are marked and illuminated the same as SFFL 1-16, above.

1. OFL — Overflow
2. ISL — Interpret Sign
3. DIPL — Disable Program Interrupt
4. ICL — Interpret Control
5. NHCL — Non-Halt On Converter Error
6. TPEL — Tape Erase
7. TML — Trapping Mode

Peripheral Device Status Panel Indicators

A Status Panel will be provided above the Console for indication of the following.

RDYL—The Ready lamp indicates when a device is ready for use. There is one of these lamps per peripheral device.

SELL – The Selected lamp indicates the device is being used. There is one of these lamps for each peripheral device.

RWDL – The Rewind lamp indicates the Magnetic Tape unit is rewinding. There is one of these lamps for each magnetic tape.

LDPL – The Load Point lamp indicates the Magnetic Tape Unit is at its initialized position after rewind. There is one of these lamps for each magnetic tape.

WLOL – The Write Lock-Out lamp indicates writing on the Magnetic Tape has been inhibited. There is one of these lamps for each magnetic tape.

EOTL – The End-of-Tape Warning lamp indicates the tape is within one block length of the end of tape. There is one of these lamps for each magnetic tape unit.

A. 4. 2 Controls

A. 4. 2. 1 Mode Controls

Run Switch – The Run Switch provides the gating levels necessary to operate the computer continuously after being started, until stopped by the program, the operator, or an error. The Run Switch releases the One Instruction and Single Pulse switches to provide the Run mode.

ONCW – The One Instruction switch generates the gating levels necessary to stop the computer after one instruction is completed.

SIPW – The Single Pulse switch generates the gating levels necessary to gate off the normal pulse distribution system and to provide a single pulse for each operation of an initiation control.

MONW – The Monitor switch generates levels which cause the computer to halt when the Address Switch Register equals the Program Counter.

A. 4. 2. 2 Initiating Controls

STW – The Start At Address Switch Register initiates a program sequence where the location of the first instruction is specified by the contents of the Address Switch Register.

COW—Start At Program Counter switch initiates an instruction sequence where the location of the first instruction is specified by the contents of the Program Counter.

CRDW—The Paper Tape Read In Switch causes a built-in read instruction to command the paper tape reader to read the first three words (Read, Sense, Transfer) from the tape into three reserved memory locations.

MTW—The Magnetic Tape Read In switch operates the same as CRDW above.

ROW—The Read Out switch initiates a read out operation which causes a memory location specified by the Address Switch Register to be read out into the Memory Output Register.

MIW—The Manual Instruction switch initiates the performing of the instruction in the Word Switch Register.

RIW—The Read In switch initiates a function which reads the contents of the Word Switch Register into a register or memory location specified by the Address Switch Register.

RPW—The Repeat Switch will cause the Central Processor Unit to repeatedly execute the instruction in the Instruction Register. The entire instruction is performed including memory access except for data transfer from memory to the Instruction Register.

A. 4. 2. 3 Special Purpose Controls

HAW—The Halt Switch is a manual method for stopping the computer. The switch performs a simulated halt instruction by setting the Halt flip-flop after completion of the current instruction except that all input/output instructions currently being executed are finished.

EHW—The Emergency Halt Switch halts the machine the same as HAW except when the computer is processing an input/output instruction. In this case the computer halts without completing the instruction and the Converter is cleared.

VTW—When the alternate action Voltage Transient Switch is in the released position, the computer will halt when an intolerable transient occurs on

the a-c power line. When the switch is locked in and a transient occurs, the computer will continue in its present mode and no action will be taken.

ACNW, ACFW—The a-c power-on/power-off alternate action switch causes the a-c Control Enclosure to connect a-c power to all units in all shelters when it is locked in.

LMPW—The momentary Lamp Test Switch when depressed lights all incandescent lamps on the Console and Peripheral Device Status Panel.

KEW—The alternate action Halt-On-Error Switch determines whether the Central Processor Unit halts or continues operation when an error condition occurs.

CLAW—The Clear Error momentary switch clears all flip-flop registers in the Central Processor Unit, In-Out Converter, and Communications Converter. This switch does not clear the simulated registers in memory.

CLRW—The Clear Computer momentary switch clears all flip-flop registers in the Central Processor Unit, In-Out Converter, and Communications Converter. This switch does not clear the simulated registers in memory.

CCAW—The Clear Converter Alarm switch clears all converter alarm flip-flops.

CMW—The Clear Memory switch provides a method for resetting to zero the contents of all memory locations.

RSW—The Register Selection buttons provide levels which result in the transferring of the contents of the eighteen registers to the Bus Indicator Register. A nine-tenth button is provided to release all other buttons and cause blanks to be displayed in the Bus Indicator Register.

Flip-Flop Controls—Manual controls and state indicators (for state indicators see Computer Status Indicators) for all sense and some of the error and control flip-flops are provided on the console. The manual control consists of a three-position switch which allows the operator three options. When the switches are up or down the flip-flops may be held in a set or reset condition. With the switch in the center position, the associated flip-flop is under program control. There are fifteen flip-flops controlled in this manner. Eight of these are Sense Flip-Flops and a list of the other seven can be found under Special Flip Flops, discussed in A.4.1.2 above.

A. 4. 2. 4 Switch Registers

WSR—A Word Switch Register consisting of 37 two-position switches is provided on the console. A word can be set up in the switches and can then be read into the register or memory specified by the Address Switch Register. Also an instruction specified in the WSR can be executed by means of the manual initiating controls (A. 4. 2. 2).

ASR—An Address Switch Register consisting of 18 two-position switches is provided on the console for addressing register and memory locations during Read-In and Read-Out operations.

A. 4. 3 Auxiliary Control Panel

An Auxiliary On-Line Control Panel is provided in each peripheral shelter for operating convenience. Halt, Emergency Halt, Start at PC, Start at ASR and Lamp Test switches, and Computing and Non-Computing indicators are provided.

A. 4. 4 The Off-Line Control Panel

An Off-Line Control Panel will be provided in the Central Processor Shelter. This panel will have the following controls and indicators:

A. 4. 4. 1 Controls

OASR—An Address Switch Register consisting of 18 two-position switches will be provided on the console for addressing register and memory locations during Read-In and Read-Out operations. This lever action switch has two positions—center and down.

OSTW—The momentary Start at ASR pushbutton initiates a program sequence where the location of the first instruction is specified by the contents of the Address Switch Register.

Read-In Switches

OCRDW—The Paper Tape Read-In momentary pushbutton causes a built in read instruction to command the paper tape reader to read the first three words (Read, Sense, Transfer) from tape into three reserved memory locations.

OCADW—The Card Read-In momentary pushbutton operates the same as the pushbutton above except the information is read from the Card Reader.

OROW—The Read-Out momentary pushbutton initiates a read instruction which causes a memory location or addressable register specified by the Address Switch Register to be read-out for displaying on the Bus Indicator Register.

OHAW—This momentary pushbutton titled Halt is a manual method for stopping the in-out instruction being performed.

A. 4. 4. 2 Indicators

OBIR—A Nixie tube octal display will be provided on this console to display the contents of any memory location or addressable register. The display can be achieved manually by means of the Address Switch Register and the Read-Out Switch. There will be fourteen of these Nixie tube displays. Twelve of these will be octal information displays, one will be a sign bit display and one will be a parity bit display. The sign bit will be signified by a plus (+) or a minus (-) and the parity bit by a one or a zero.

A. 4. 5 Auxiliary Off-Line Control Panel

An Auxiliary Control Panel for off-line purposes is located in each of the peripheral shelters. This panel has Start At ASR, Halt, Paper Tape Read-In and Card Read-In Switches.

A. 5 COMMUNICATIONS CONVERTER

The Communications Converter is a device which accepts input and output instructions from the CP via the MO Bus and controls data flow to and from up to 32 TYC-1 two-way data terminals. This is accomplished through control words stored in core memory.

Addresses $(00100)_8$ through $(00177)_8$ are fixed core locations assigned to the Communications Converter for control word and for incoming control character storage.

A. 5.1 Control Words

The structure of "Receiver" Control words is as follows:

37	36-34	33	32	31	30	-	22	21-19	18	17	-	1
----	-------	----	----	----	----	---	----	-------	----	----	---	---

- 1-17 Memory address at which to store data
- 18 Unused
- 19-21 Number of characters received this word
- 22-30 Number of words to be received
- 31 Interpret Sign
- 32 If this bit is a one, it indicates that a control character has been received
- 33 If this bit is a one, a parity error has been detected
- 34-36 Unused
- 37 Channel in use

The structure of the Transmit Control Word is as follows:

- 1-17 Address of memory location from which next character is to be transmitted
- 18 Unused
- 19-21 Number of characters remaining to be sent from current memory location
- 22-30 Number of words remaining to be sent
- 31 Interpret Sign
- 32 Transmit a single control character per word from bit positions 31-36 of each data word

	Ignore bits 19-21
33-36	Unused
37	Channel in use

A. 5. 2 Block Diagram

A block diagram of the Communications Converter is shown in Figure A-12. Below is a list of definitions which apply to this block diagram.

CW Register—Control Word Register—The control word is stored for interpretation and updating.

SAR—Strobe Active Register —A strobe from a receiver channel will place a one in the appropriate bit position of this register to indicate that a strobe pulse has been received in that channel.

TAR—Transmitter Active Register—A one is placed in the appropriate bit position by the LOD order to indicate that the transmitter channel is to be used.

RCTR—A counter which polls the SAR to determine which receiver is active.

TCTR—A counter which polls the TAR to determine which transmitter should be used.

TARC, SARC—Devices which sample to SAR and TAR for "All 0's" condition.

STATUS—The main control register of the CC. The status register controls sequencing of the receive and transmit operations.

A. 5. 3 Communications Converter Operation

A. 5. 3. 1 Receiving

1. An incoming character activates the STROBE signal, placing a one in the appropriate bit position of SAR
2. SARC detects that SAR is no longer "All 0's" and informs STATUS
3. STATUS activates RCTR, which polls the SAR until it finds a non-zero bit

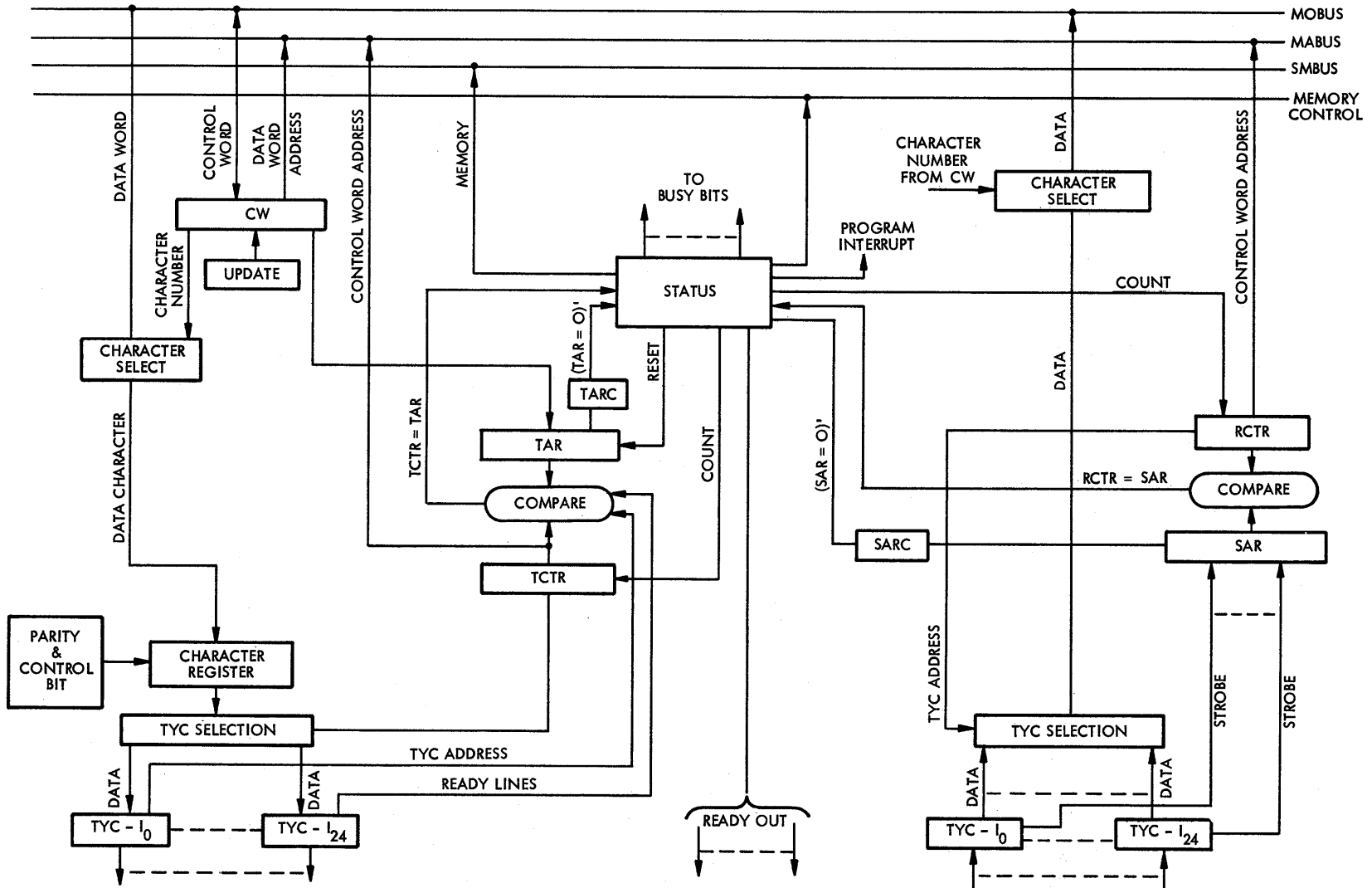


Figure A-12. Communications Converter Block Diagram

4. When a non-zero bit is detected, STATUS sets the "busy bit" requesting the memory. When the memory is available, the contents of RCTR are placed on Mem In-Out Bus, and the proper control word is addressed.
5. Central Memory, using contents of MA bus, gets appropriate control word and puts it on MO Bus.
6. STATUS gates contents of MO bus into CW register; bit of SAR is reset to 0.
7. Control word is updated and modified if necessary to indicate control character or parity error, and returned to memory.
8. If incoming character was a data character, the address in the control word is used to fetch word from memory, mask in the new character with parity bit and control bit involved, and restore word to memory.

A. 5. 3. 2 Transmitting

1. A LOD instruction causes the appropriate bit of TAR to be set to a one.
2. TARC senses that TAR is no longer "All 0's" and reports to STATUS.
3. STATUS starts TCTR polling TAR until it finds a non-zero bit.
4. When the non-zero bit is detected, STATUS sets the "busy bit" requesting the memory. When the memory is available, it places the contents of TCTR on MA Bus.
5. Memory, using this information, fetches the control word and places it on MO bus.
6. STATUS gates contents of MO bus into CW register, and bit of TAR is reset to 0.
7. Control word is updated and returned to memory.
8. Using control word information, the memory sends data word to CC.
9. STATUS selects appropriate character, according to CW, and after tacking on parity and control bit, sends character to the proper TYC transmitter.

A. 5. 3. 3 Sequencing (Interrupt is Required)

The Communications Converter will generate an interrupt under the following conditions:

- a. Completion of a transmission (bits 30-22 of control word "All 0's")
- b. Receipt of completed message (bits 30-22 of control word "All 0's")
- c. Receipt by CC of a control character

APPENDIX B

BASIC CIRCUIT SELECTION AND ELECTRICAL PACKAGING

B. 1 CIRCUIT SELECTION

B. 1. 1 General Background

The ATACC computer is a product improvement version of MOBIDIC, but in establishing its design, a careful study was undertaken to determine whether or not the same type of basic circuit used in MOBIDIC was suitable for incorporation into a computer to be used in the late 1960's and early 1970's. This study has proven that the basic, transistor-logic, germanium circuitry remains superior to its alternatives on grounds of:

- Lower semiconductor count
- Increased reliability and better proof of reliability
- Lower heat dissipation per circuit stage
- Lower sensitivity to nuclear radiation
- Lower present cost
- Fewer design changes

B. 1. 2 Possible Alternatives

Based on the current state-of-the-art, two types of circuit design deserved consideration for the ATACC application. First is the all-transistor inverter logic used in MOBIDIC and second is the transistor-diode type using silicon semiconductors. Both circuit types have been used extensively at Sylvania; both have a proven record of reliability; and a good argument could be generated in favor of either type. The specific outstanding experience with MOBIDIC circuit performance clearly justifies the retention of this circuit design for the ATACC computer.

B. 1. 2. 1 Various Characteristics; Semiconductor Count and Costs

The major advantages to transistor-diode logic might appear to be a reduction in the number of transistors and the use of silicon devices. Silicon semiconductors might seem desirable because of their availability in smaller cans

suitable for various forms of microminiaturization; their higher junction temperature, presumably reducing the requirements for artificial cooling under high temperature operation; and the prospect that future silicon device costs will become equal to or less than the present cost of germanium transistors. In actual fact, the advantages of transistor-diode logic are less meaningful than might be claimed. It is true that this approach permits the reduction of the total number of transistors, but the reduction is far outweighed by the addition of a requirement for diodes. Thus, the MOBIDIC Central Processor, as it now stands, uses 14,000 transistors and no diodes in its present transistor logic form. A transistor-diode version would use 8,000 transistors and 24,000 diodes. Therefore, the net increase of semiconductor devices is extremely large. In going from 14,000 semiconductors to 32,000 semiconductors, we have an increase by a factor of more than two to one. Even more important, a reliability analysis indicates that in this case, based on the component counts and general industry experience, the mean-time-between-failure for the MOBIDIC transistor logic will be considerably longer than for the transistor-diode alternative. Since MOBIDIC circuitry has already demonstrated actual reliability almost ten times that of such analyses, the shift to transistor-diode logic is even more questionable. The ATACC Central Processor, using MOBIDIC logic, will contain only about 10,000 transistors and no diodes. Furthermore, the cost advantage of the germanium transistors is present and real, while the future costs of silicon semiconductor devices is subject to many economic factors which cannot be controlled and which may vary unpredictably. When germanium transistors were originally selected for MOBIDIC in 1957, the cost was about \$8.00 per transistor. This cost has steadily diminished to a present amount of \$1.25. Continued use of the same transistor gives the Army the opportunity to take advantage of the gradual reduction which has developed. Shifting to a silicon transistor may mean tripling the initial semiconductor cost, in the hope that future costs will again follow the same downward trend. However, future costs of the transistor used in MOBIDIC can be predicted more accurately than the future costs of the silicon transistors and diodes, and so, in another way, the MOBIDIC circuitry approach offers reduced risk for application to ATACC.

B. 1. 2. 2 Junction-Temperature Differences

The apparent advantage of silicon semiconductors, due to their higher junction temperature tolerance, is of primary significance in establishing the manufacturing process for modules, since processes involving curing or baking are more appropriate. Therefore these semiconductors are more suitable to the various types of microminiaturization approaches. The difference in junction temperatures is much less important when it comes to usage in ground equipment; in both cases, however, the combination of environmental extremes and internal dissipation calls for a moderate amount of cooling air to remain within the temperature limits.

B. 1. 2. 3 Higher Temperature Disadvantages

Silicon transistors can tolerate a junction temperature considerably higher than germanium, typically 150°C versus 90°C for germanium. However, Sylvania and other electronics companies have produced a long list of equipment using germanium transistors which have performed well in the rigid military environment. In digital data circuits, power consumption is very low as compared, for example, to servo amplifier circuits, and properly designed circuits need never approach the critical junction temperature of the semiconductor. The type of circuitry used in MOBIDIC was later repackaged in miniature form for AN/USD-7 and AN/MPQ-32, where exhaustive environmental tests showed that the circuit junction temperatures remained below 68°C , even at the high temperature test extremes. The inherently higher collector-emitter saturation voltage and base-emitter voltage of silicon transistors cause dissipation in the transistor, some three to five times greater than that of the germanium transistor used in MOBIDIC and ATACC. These higher transistor voltage ratings necessitate the use of a higher d-c voltage in the power supply in order to obtain satisfactory logic levels. Thus both the d-c dissipation and the transient power dissipation in the transistor are increased. The end result is that the junction temperatures rise to values higher than those in germanium transistors; ultimately, the same cooling requirements are encountered and no improvement is obtained.

B. 1. 3 Nuclear Radiation Damage

Furthermore, an important disadvantage of silicon semiconductors is their much greater sensitivity to nuclear radiation. This might be of great significance in the present application, since a distant atomic attack might disable the computer at a critical time even though the equipment is far out of blast range.

B. 1. 3. 1 Selected Type Less Vulnerable

Should the area near the ATACC computer be subjected to nuclear radiation resulting from either artillery- or aircraft-launched nuclear explosives, the equipment design should be such that, if the shelters survive the physical damage from blast and heat waves, the computer should not fail due to permanent damage resulting from the radiation effects. Sylvania has determined that the proper selection of electronic components can give an improvement of the first magnitude in the computer's resistance to radiation. In particular, the semiconductors are among the most vulnerable components. As shown below, the germanium PNP transistor that Sylvania has selected to use for the ATACC computer is far more resistant to radiation damage than are NPN silicon transistors.

B. 1. 3. 2 Confirmation from Other Sources

Studies conducted by many organizations, including Boeing, Litton, and Philco Corporation, all agree approximately on the desirable properties of transistors. This discussion limits itself to fast transistors best suited for switching purposes in a digital computer.

B. 1. 3. 3 Characteristics of Preferred Type

To be most resistant to nuclear radiation, a transistor should have:

PNP construction

germanium

a narrow base width

low resistivity, graded base region

thin inter-electrode region

B. 1. 3. 4 Radiation Effect on Beta Value

The 2N393, which is used in the ATACC computer, satisfies every one of the requirements listed except that the base region is not a graded region. However, the resistivity of the base region (0.1 ohm-centimeter) is extremely low. For purposes of comparison, we have considered the case of a 10 kiloton bomb. If the ATACC computer were located 2,000 yards away from the point of explosion, both the personnel and the structure can be expected to survive both blast and nuclear effects. Some permanent damage would be done to the circuit characteristics, no matter what transistors had been selected. In the case of silicon transistors, like the 2N1115 NPN silicon grown-junction transistor, the radiation flux would permanently reduce the value of Beta to a point less than 25 percent of its normal value, thereby completely destroying the usefulness of the computer. Under similar conditions, the germanium transistors of the class used in the ATACC computer would suffer a much smaller degradation. The value of Beta would remain about 75 percent of its normal, and the derating rules used in circuit design would permit the computer to continue satisfactory operation.

B. 1. 4 Proven Performance of Selected Type

The major advantage of the transistor logic germanium circuitry is its proven performance. Probably no other digital computer circuitry has seen more use in militarized equipment under the observation and control of Army personnel than the MOBIDIC basic circuits. MOBIDIC A has been in operation and test at Fort Monmouth for over three years; MOBIDIC B has been operating part of the Army's ARTOC for two years; MOBIDIC 7A has been operational with the 7th Army in Europe for over a year on a three-shift basis; MOBIDIC C has been in use by the Army at Fort Huachuca for one year; and MOBIDIC D is now undergoing installation by the Army in Europe after more than a year of operation in the Sylvania plant. The identical circuitry has been operational with a two megacycle clock pulse in the 9400 computer, one of which is installed at the Pentagon for the Army's OACSI, while a second is in continuous operation at Sylvania's Needham plant and has often been used by the Army. The same circuit design is embodied in the computer portions of the Army's MPQ-32 artillery-locating equipment, as well as in the USD-7, an airborne surveillance computer;

the PARADE computer for use in an Army anti-missile system; and the IT&T 465L computer. The same type of circuitry has been widely used by organizations other than Sylvania, most notably in the BASICPAC computer and the TX-0 and TX-2 computers of Lincoln Laboratories.

B. 1. 4. 1 Reliability

However, popularity is at best only a partial guide. As a matter of fact, the transistor logic type's performance has been remarkably good. In MOBIDIC, circuit reliability has far exceeded expectations and design requirements. The electronic (that is, transistor) portions of MOBIDIC have been essentially trouble-free in MOBIDIC 7A wherever operational status has been achieved under military field conditions. On those rare occasions when trouble has developed in the electronic portions of MOBIDIC 7A, it has usually been traced to the plugs that hold the packages in place or to the cables and connectors running between cabinets, and only rarely to the circuitry itself. (See also Appendix D to this proposal, discussing reliability more fully.)

B. 1. 5 Miniaturization

It is noteworthy that the MPQ-32 computer was miniaturized and uses the same packaging technique as the ATACC computer. As a result of this miniaturization, an improvement in speed performance has been noted. Table B-1 presents quantitative data to substantiate the improvement in the performance of the original MOBIDIC circuitry as Sylvania gained experience and was able to go to more dense packaging and, therefore, shorter "back wiring".

B. 1. 5. 1 Less Obvious Advantages of Dense Packaging

With denser packaging, a decrease was achieved in the stray inductances, capacitances, (producing delay and ringing) and mutual inductances (producing crosstalk) associated with circuit interconnections. The actual reduction in circuit delays, as shown in the table, was from one-third to one-half; the decrease from the original condition was from better than one-half to one-fifth. In addition, the shorter interconnections required fewer power-consuming terminating resistors, thus reducing the power level of the computer.

B. 1. 5. 2 Circuit Speed and Noise Level

An interesting conclusion is that the limiting factor in the speed of the MOBIDIC circuits was not the transistor, but the interconnections. Also, the noise level had gone down. The MPQ-32 interconnections have been so improved that contemplated operation of the circuits at twice the original MOBIDIC speed is justified and even conservative in the ATACC computer, which uses the same packaging design as the MPQ-32 computer.

TABLE B-1. COMPARISON OF CIRCUIT DELAYS

Circuit	Original Delay Limit (Nanoseconds)	Typical Delays Measured on Original MOBIDIC Breadboard (Nanoseconds)	Typical Delays Measured on MPQ -32 Computer (Nanoseconds)
Inverter	100	34	18
Emitter Follower	40	<10	<10
Register Driver	150	62	40
Half Register Driver	-	-	35
Gated Pulse Driver	150	61	25
Flip-Flop (complementing)	250	215	115
Flip-Flop (inverter)	-	-	40

B. 1. 6 Adaptability of Existing MOBIDIC Design

Another advantage of the MOBIDIC circuitry is the fact that the existing MOBIDIC block diagram design can be used, exactly as is, in most of the ATACC computer. Again, advantage can be taken of proven performance, but more than that, the tedious task of transforming the logical design from transistor logic to transistor-diode logic can be avoided. This task is not a large nor a challenging

one, but would require time and engineering manpower; to the Army, this can only mean unnecessary cost and the risk that elsewhere the schedule must be compressed if the established delivery dates are to be met. If this transformation were done within Sylvania by engineers who have worked previously on MOBIDIC and under the control of a management team supporting MOBIDIC, it would be relatively certain that such a task would be completed in a straightforward way. However, if the transformation were performed by another engineering organization under a different management, there is a real likelihood that the engineers assigned to this task will be tempted to indulge their technical virtuosity and add internal innovations to the design. This would greatly increase the risk of cost and schedule performance, as well as the risk that the end result will fail to meet existing requirements without additional debugging and retrofit during the test and initial usage phases.

B. 1. 7 Comparable Characteristics

The comparison between MOBIDIC transistor-logic circuitry and silicon transistor-diode circuitry may, therefore, be summarized as follows and as shown in Table B-2:

MOBIDIC Transistor Logic

1. Total semiconductor component count is less than one-third that of the alternative.
2. Semiconductor device cost advantage is present and real.
3. Semiconductor junction temperature limit is lower, and circuit dissipation is also lower.
4. Circuit design is fully proven in performance, in large systems.
5. Existing logic design may be used.
6. Germanium semiconductors are less sensitive to nuclear radiation.

Silicon Transistor-Diode Logic

1. Transistor count is not much more than half that of MOBIDIC logic.

TABLE B-2. COMPARISON BETWEEN MOBIDIC TRANSISTOR LOGIC (MTL) AND TRANSISTOR-DIODE LOGIC (TDL) CIRCUITRY

Item	MOBIDIC Transistor Logic (MTL)	Transistor-Diode Logic (TDL)	Advantage	Net Advantage
1. Semiconductor Count				
Transistors	More	Fewer	TDL	
Diodes	None	Many	MTL	
TOTAL	Fewer	More		MTL
2. Reliability				
Based on Component Count	Higher	Lower		MTL
3. Semiconductor Type				
Junction Temperature	Germanium	Silicon		
Heat Dissipation per Stage	Lower	Higher	TDL	
Sensitivity to Nuclear Radiation	Lower	Higher	MTL	
Size of Transistor	Larger	Smaller	TDL	
Cost Advantage	Present, Real	Future, Potential	MTL	
TOTAL				MTL
4. Equipment Design Implications				
Circuit Design Proof	Performance in Field	Testing Only	MTL	
Logical Design Changes	Less Required	Complete Revision Needed	MTL	
TOTAL				MTL

2. There is promise of a cost advantage in future production.
3. Semiconductor junction temperature limit is higher, and circuit dissipation is twice as high.
4. Circuit design is promising, based on test results but not on extensive performance data.
5. Complete transformation of logic design is required.
6. Silicon semiconductors are more sensitive to nuclear radiation.

B. 1. 7. 1 Comparison in Detail

Comparison reveals that the choice is between an existing proven, satisfactory solution and a prospective, semi-proven, slightly better solution. It is concluded that the present real advantages of the MOBIDIC circuits are so strong that those circuits have been selected for use in the ATACC computer, since the objectives of early delivery and minimum cost are paramount; silicon transistor-diode circuitry could be justified only if long-range objectives of size and economy warrant a delay in reaching earlier scheduled milestones.

B. 2 ELECTRICAL PACKAGING

B. 2. 1 General

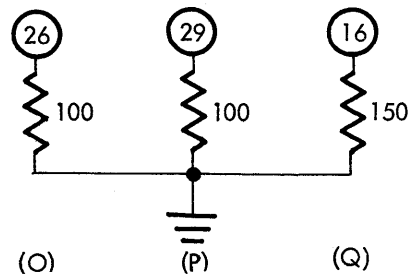
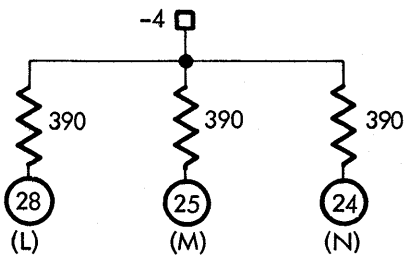
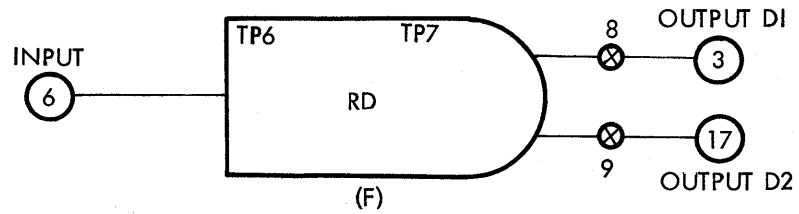
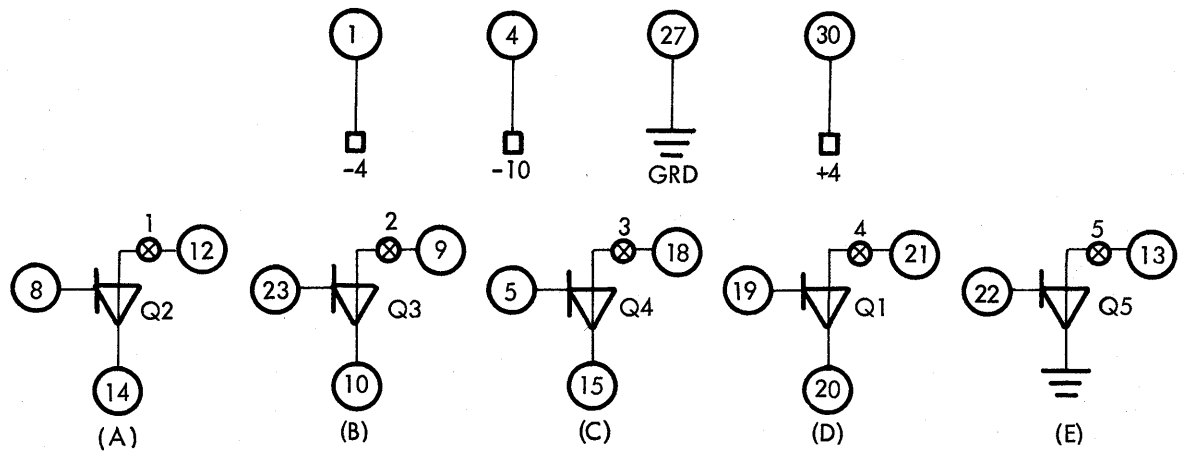
The module stick package represents a happy compromise between all of the counterforces which must be considered in choosing a basic pluggable package. It contains sufficient components so that not all interconnections have to be done on the back panel, yet is not so large that each package is a special type for a single application. In addition, its small size and high density permits the packaging of a large number of circuits in a given backpanel area. This reduces wiring length, with stray capacitance, so that a given circuit may be used at a rate more compatible with its own capability. (See also Appendix D to this proposal for stick reliability and testing.)

B. 2. 2 Reliability and Adaptation

The stick, together with its associated items and techniques, (such as the plated receptacle block, solderless wire connectors, established tooling and assembly techniques) has proven an unqualified success on the AN/MPQ-32 computer. In that computer, only 22 electrical types of packages were necessary. In the ATACC System approximately 40 types are necessary, due to the variety of peripheral devices offered.

B. 2. 3 Illustrations

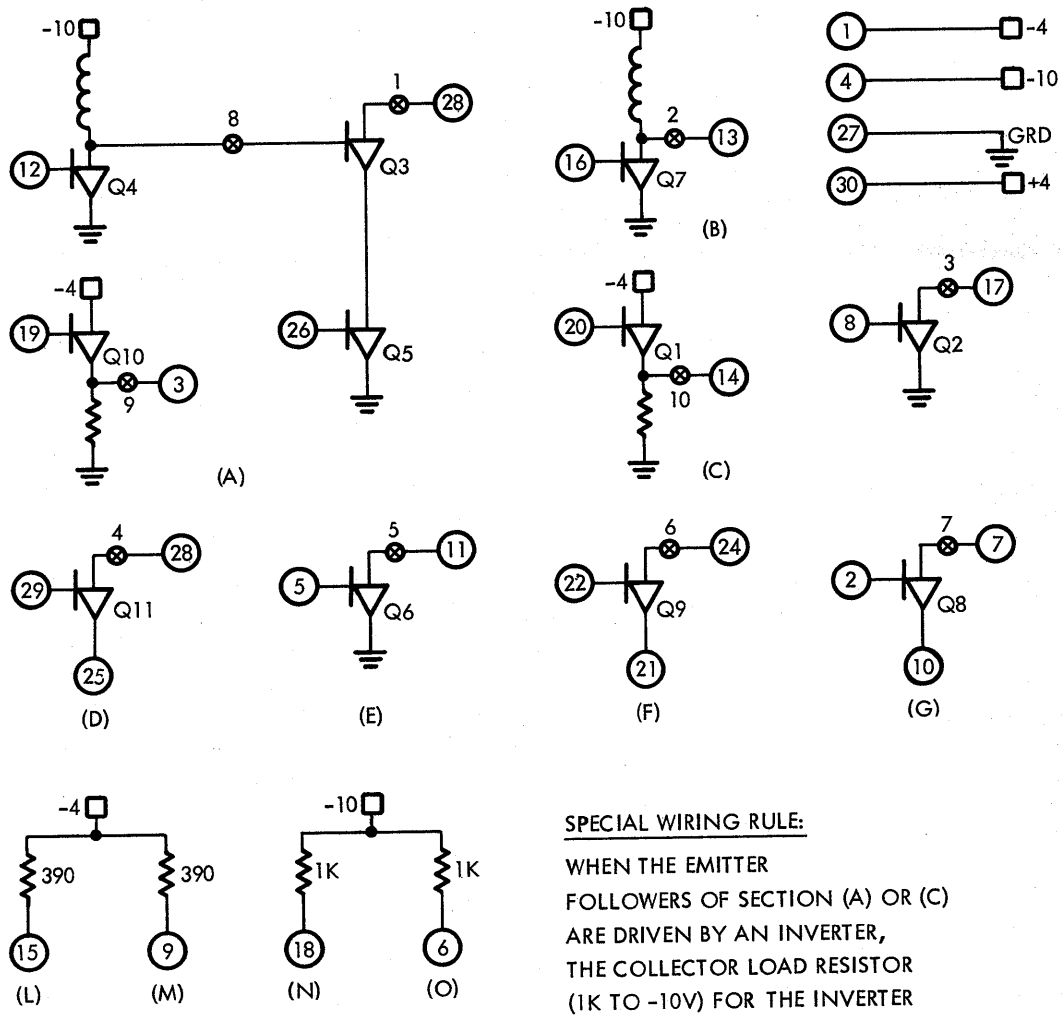
Figures B-1 through B-11 show logical drawings for some typical sticks.



KEY:

- ⑤ ... CONNECTOR PIN AND NUMBER
- ⊗ ... TEST PIN
- ... VOLTAGE SOURCE

Figure B-1. Type 101 Register Driver



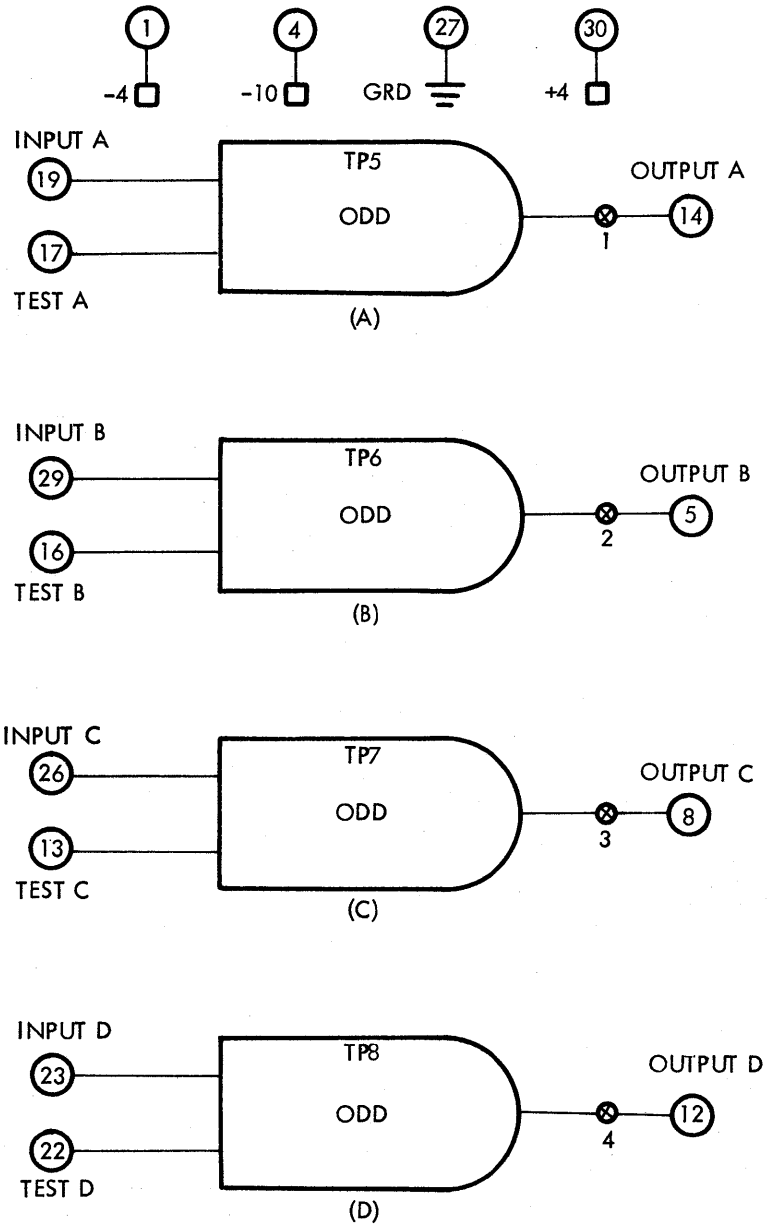
SPECIAL WIRING RULE:
 WHEN THE EMITTER FOLLOWERS OF SECTION (A) OR (C) ARE DRIVEN BY AN INVERTER, THE COLLECTOR LOAD RESISTOR (1K TO -10V) FOR THE INVERTER MUST BE LOCATED IN THIS STICK. (SECTIONS (N) OR (O)).

KEY:
 (5) CONNECTOR PIN AND NUMBER
 ⊗ TEST PIN
 □ VOLTAGE SOURCE

Figure B-2. Type 102 GPD Gating and Ringing Circuits

DRIVER TYPE	STICKS USED		WIRING CONNECTIONS		DRIVER CONFIGURATION
	NO.	SEC.	CONNECT	TO	
REGISTER DRIVER	101	F	STICK 101, PIN 7	GROUND	
PULSE DRIVER (1)	101	F	STICK 101, PIN 2	STICK 102, PIN 23 -4 VOLTS	
	102	A	STICK 102, PIN 26		
PULSE DRIVER (2)	101	F	STICK 101, PIN 7	GROUND STICK 102, PIN 13	
	102	B	STICK 101, PIN 11		
GATED PULSE DRIVER (1 GATE)	101	F	STICK 101, PIN 2	STICK 102, PIN 23 STICK 102, PIN 26	
	102	A	STICK 102, PIN 3		
GATED PULSE DRIVER (1 GATE)	101	F	STICK 101, PIN 7	STICK 102, PIN 17 STICK 102, PIN 13 STICK 102, PIN 8	
	102	B	STICK 101, PIN 11		
	102	C	STICK 102, PIN 14		
GATED PULSE DRIVER (2 GATES)	101 102 102 102	F A B C	STICK 101, PIN 2 STICK 101, PIN 7 STICK 101, PIN 11 STICK 102, PIN 3 STICK 102, PIN 14	STICK 102, PIN 23 STICK 102, PIN 17 STICK 102, PIN 13 STICK 102, PIN 26 STICK 102, PIN 8	

Figure B-3. Type 101 and 102 Wiring

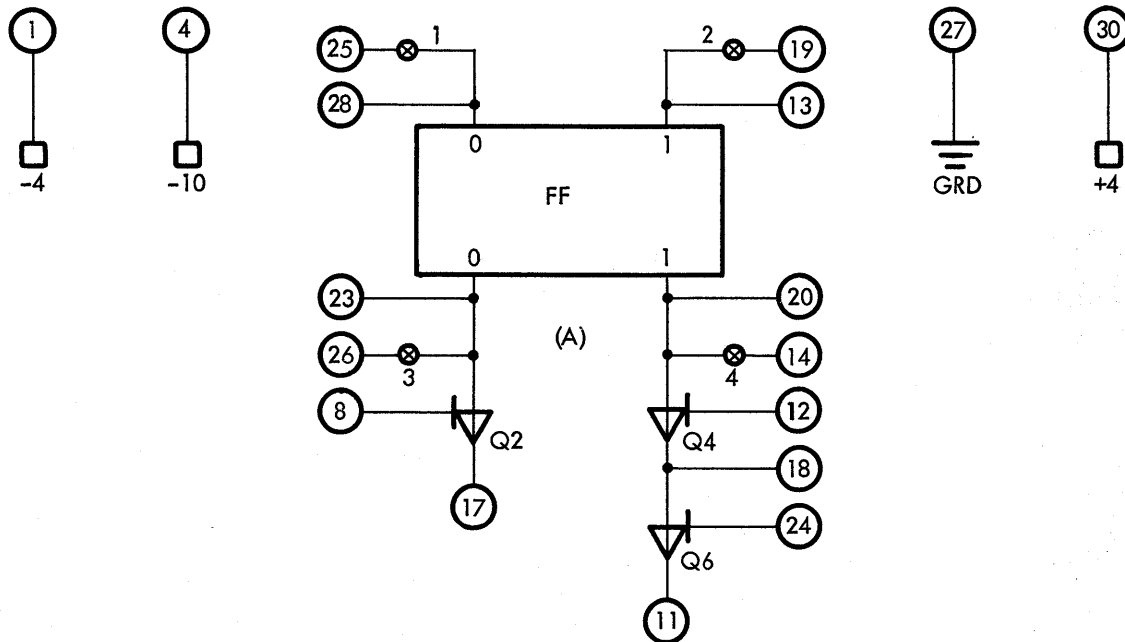


KEY:

⑤... CONNECTOR PIN AND NUMBER

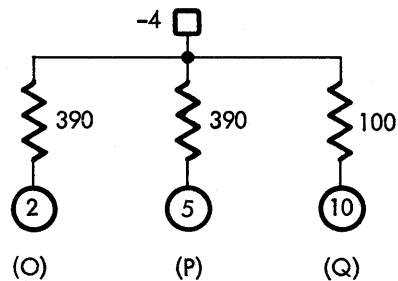
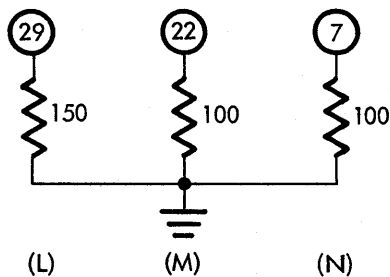
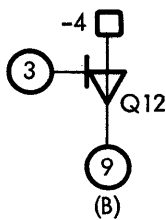
⊕... TEST PIN

Figure B-4. Type 301 Output Device Drivers



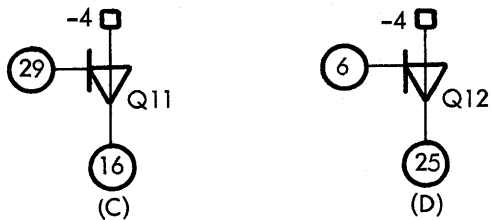
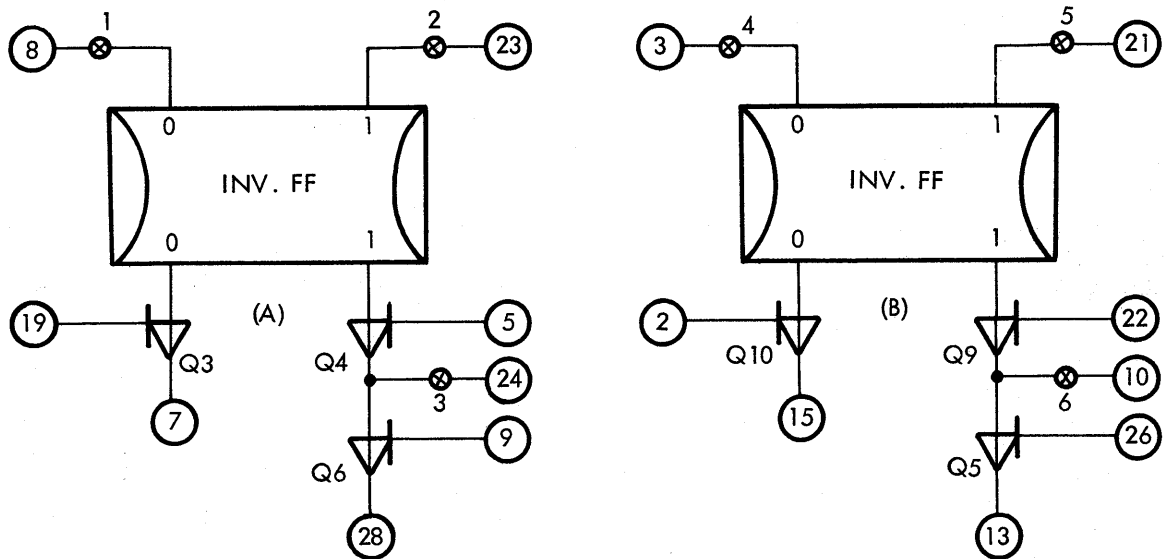
SPECIAL WIRING RULE:

THE EMITTER FOLLOWER OF SECTION (B) CAN ONLY BE EMPLOYED WITH THE OUTPUTS OF THIS PACKAGE, OR WHEN DRIVEN BY ANOTHER EMITTER FOLLOWER OR CASCODE CIRCUIT.



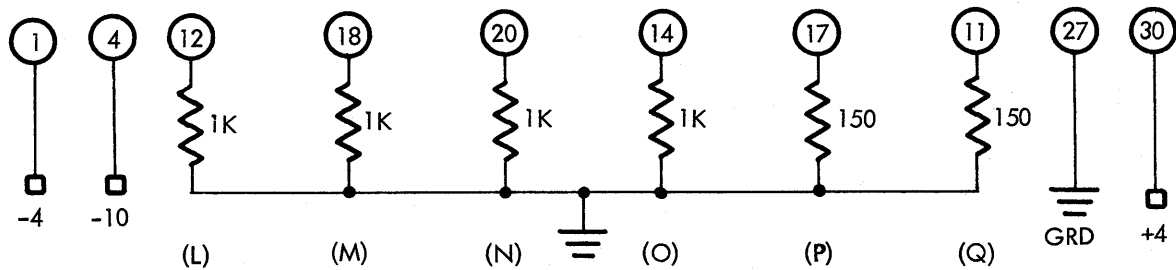
- KEY:
- ⑤ CONNECTOR PIN AND NUMBER
 - ⊗ TEST PIN
 - VOLTAGE SOURCE

Figure B-5. Type 501 Register Flip-Flops



NOTE:

SEE SHEET 2 OF 2 FOR
SPECIAL WIRING RULES.



KEY:

- ⑤...CONNECTOR PIN AND NUMBER
- ...TEST PIN
- ...VOLTAGE SOURCE

Figure B-6. Type 502 Inverter Flip-Flops

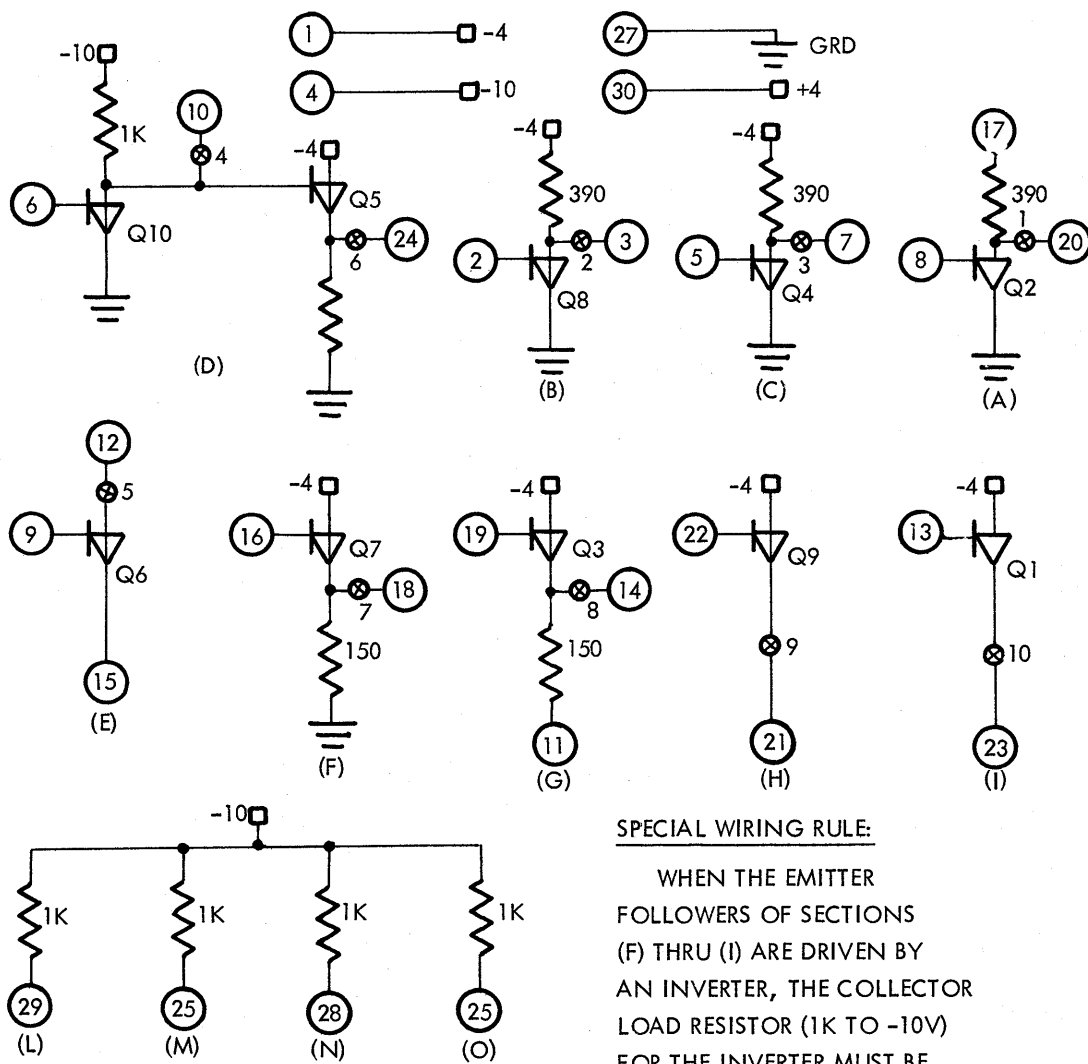
RULE No.	TYPE OF OUTPUT	RULE	LOADING RESISTOR
1	NOT USED	NONE	1K TO GRD
2	SINGLE EMITTER FOLLOWER	EMITTER FOLLOWER MUST BE LOCATED IN THE SAME STICK AS THE INVERTER FLIP-FLOP.	NONE
3	EMITTER FOLLOWERS IN PARALLEL	ONE EMITTER FOLLOWER MUST BE LOCATED IN THE SAME STICK AS THE INVERTER FLIP-FLOP; THE OTHERS MAY BE EXTERNAL TO THE STICK.	NONE
4	EMITTER FOLLOWERS PLUS INVERTER	USE RULE No. 3.	NONE
5	INVERTERS	NONE	1K TO GRD

*THESE RULES APPLY TO EITHER OUTPUT OF THE INVERTER FLIP-FLOPS.

SPECIAL WIRING RULE:

THE EMITTER FOLLOWERS OF SECTION (C) AND (D) CAN ONLY BE EMPLOYED WITH THE OUTPUTS OF THIS STICK OR WHEN DRIVEN BY ANOTHER EMITTER FOLLOWER IN A CASCODE CIRCUIT.

Figure B-7. Type 502 Wiring



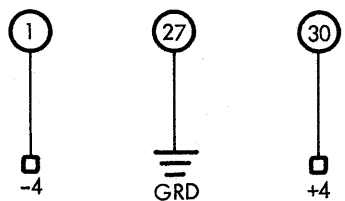
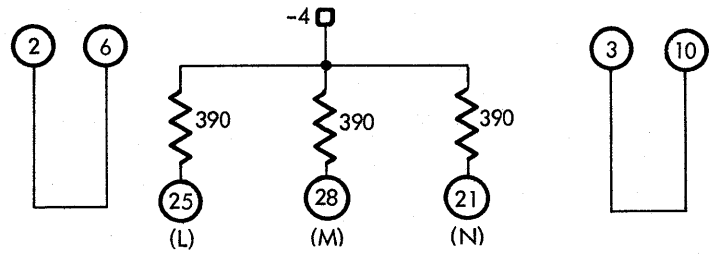
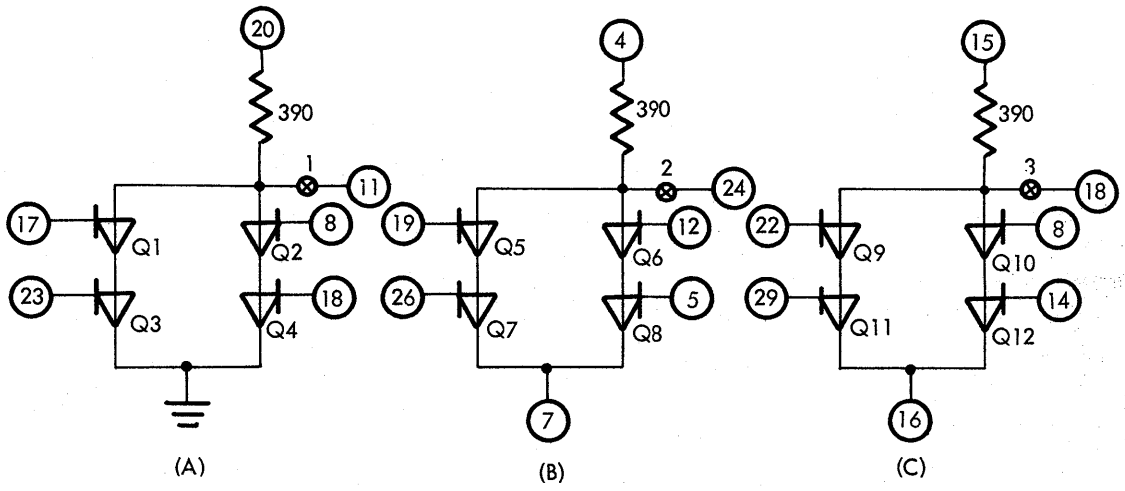
SPECIAL WIRING RULE:

WHEN THE EMITTER FOLLOWERS OF SECTIONS (F) THRU (I) ARE DRIVEN BY AN INVERTER, THE COLLECTOR LOAD RESISTOR (1K TO -10V) FOR THE INVERTER MUST BE LOCATED IN THIS STICK.

KEY:

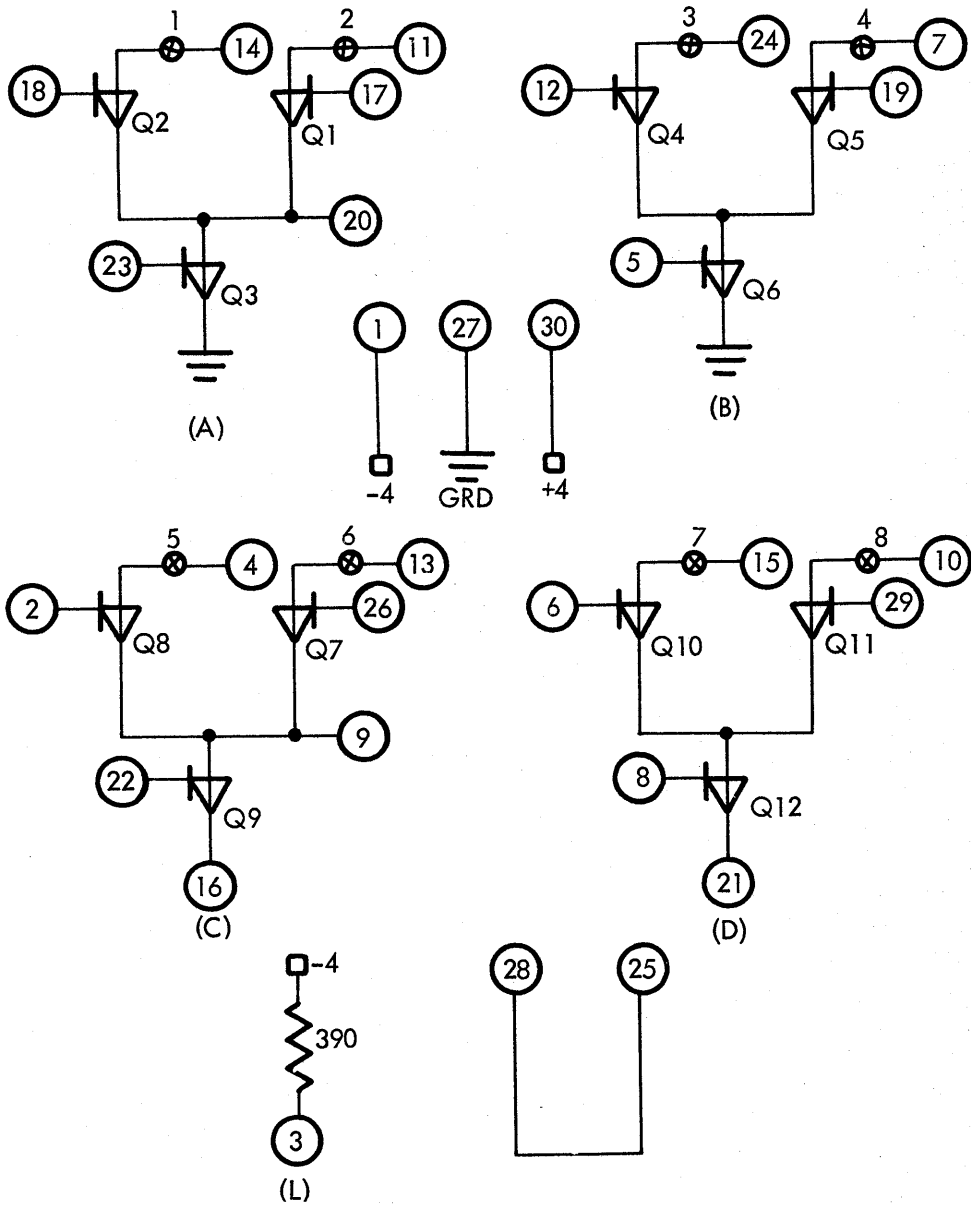
- ⑤ ... CONNECTOR PIN AND NUMBER
- ⊕ ... TEST PIN
- ... VOLTAGE SOURCE

Figure B-8. Type 801 Logic 1



KEY:
 (5) ...CONNECTOR PIN
 ⊗ ...TEST PIN
 □ ...VOLTAGE SOURCE

Figure B-9. Type 803 Logic 3



KEY:

- ⊙ ... CONNECTOR PIN
- ⊗ ... TEST PIN
- ... VOLTAGE SOURCE

Figure B-10. Type 805 Logic 5

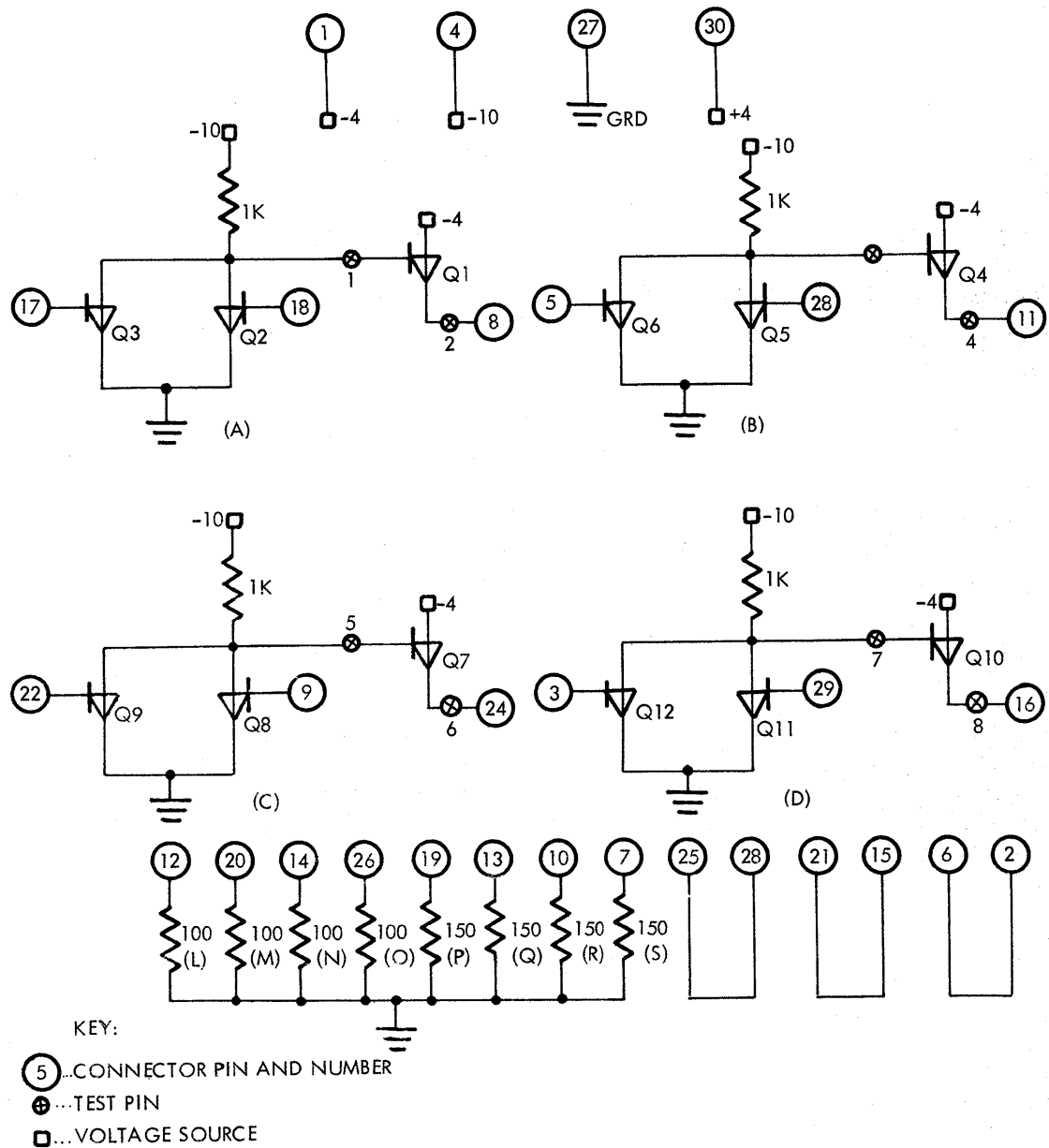


Figure B-11. Type 808 Bus Drivers

APPENDIX C

MECHANICAL DESIGN

C. 1 STICK PHYSICAL DESIGN

C. 1. 1 General

The mechanical design of ATACC equipment and associated electronics employs a miniaturized, three dimensional (stick), electronic plug-in package. Stick packaging was selected because of its extreme density of standard military approved components, maximum reliability, resistance to severe environments, minimum cost, size and weight. Extensive scrutiny and evaluation under value engineering programs have resulted in this optimum design. Stick packages have been produced and tested by two Sylvania manufacturing facilities for use in the AN/MPQ-32 Radar Set Computer (Figure C-1) and in a Military Magnetic Tape Transport System currently under development.

C. 1. 2 Advantages

A comparison of the three major parameters based on the same transistor count in the present MOBIDIC flat board packaging (Figure C-2) and the stick shows that the stick is approximately:

- 45 percent lighter in weight
- 92.5 percent smaller in volume
- 2/3 of the cost

The entire system has approximately 40 stick types compared to 375 package types and 75 element types used on MOBIDIC. This reduction of package types greatly reduces the quantity and types of spare parts required. In addition, over twice the number of test points are available per transistor on the sticks permitting easier probing of the system in testing. The use of high density stick packaging considerably reduces the average length of logic interconnections, thereby increasing circuit speed and decreasing crosstalk.

A significant point to note is that even with the tremendous reduction in volume and weight, standard military approved components and manufacturing

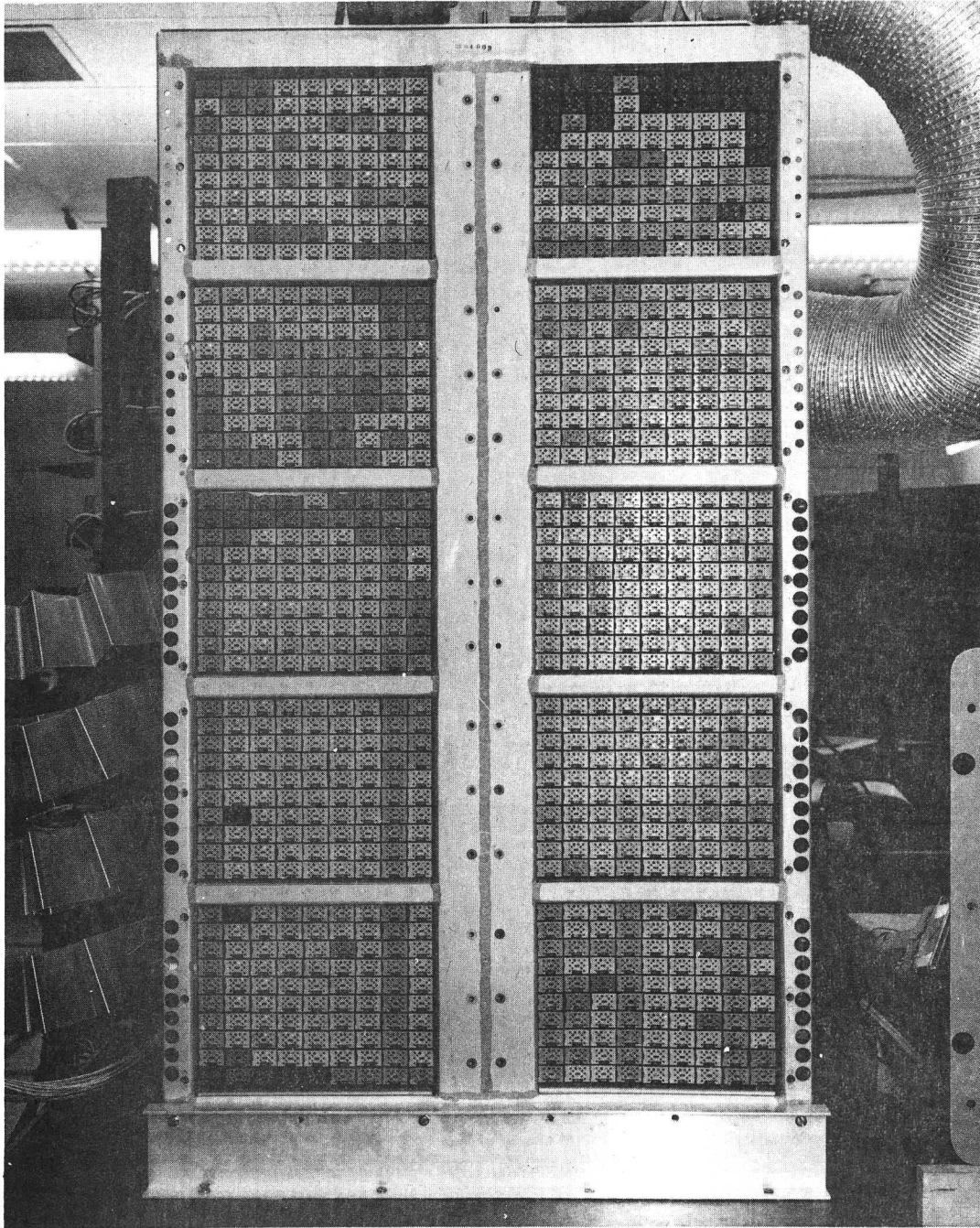


Figure C-1. AN/MPQ-32 Central Processor Sticks

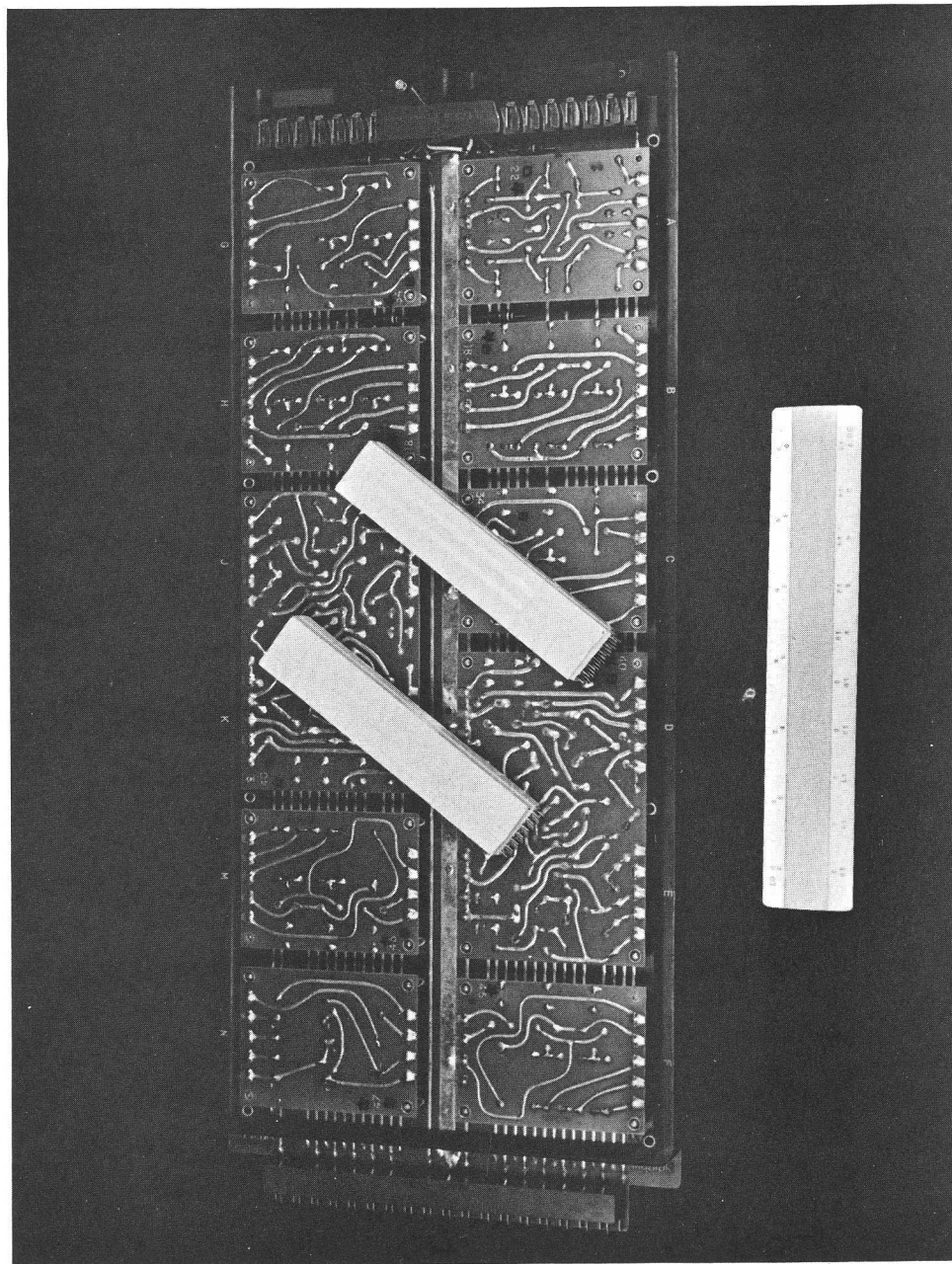


Figure C-2. Illustration Showing Comparative Size of MOBIDIC Board and 3-D Stick

techniques are still used. Other advantages found in the use of the stick element is the fact that the inherent design allows the sticks to be butted together without loss of space due to mounting. This leads to a component density of 50,000 standard components per cubic foot. The use of replaceable transistors is another feature of the stick.

Stick packaging was originally designed and developed for the militarized tactical digital computer AN/MPQ-32. A major objective was to obtain a high density package at minimum cost that was capable of being manufactured using reliable, conventional methods and standard military approved components for field army equipment.

C. 1. 3 Physical Characteristics

The dimensions of the stick (Figures C-3 and C-4) are four inches long by nine inches wide by 0.62 inch high with a volume of 2.23 cubic inches and an average weight of 2.11 ounces. The test point block, Figure C-5, has a stick type number and an extraction slot for removing the stick from the cabinet.

On the two ends are a 30-pin connector and a 10-pin test point block. A recess along the transistor mounting surface forms an air plenum for the cooling air to pass over the transistor cases when the sticks are vertically stacked (Figure C-6). The logic package can accommodate as many as 75 standard components, including 12 transistors. In special applications, such as the magnetic tape units, even more dense packaging is achieved.

The left and right sides of the stick have a tongue and groove configuration (refer to Figure C-5) to interlock adjacent horizontal sticks. In the structure, groups of stick packages are pre-stressed in compression to form rigid sections. The basic stacking for this computer is 10 high and 13 across resulting in a block assembly of 130 sticks.

The internal structure of the package (Figure C-3) has axial lead components positioned between printed circuit boards in a sandwich-like fashion. Since the narrow width of a single printed circuit board is not sufficient to make all the connections required, additional boards are stacked in parallel.

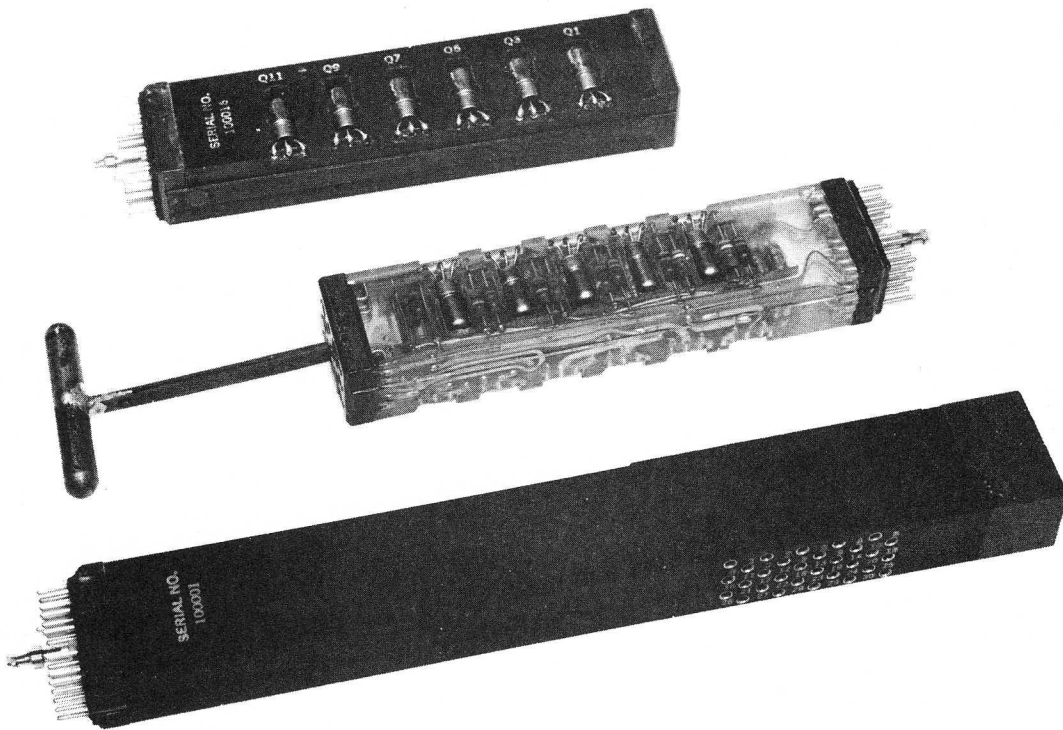


Figure C-3. Electronic Circuit Stick Types

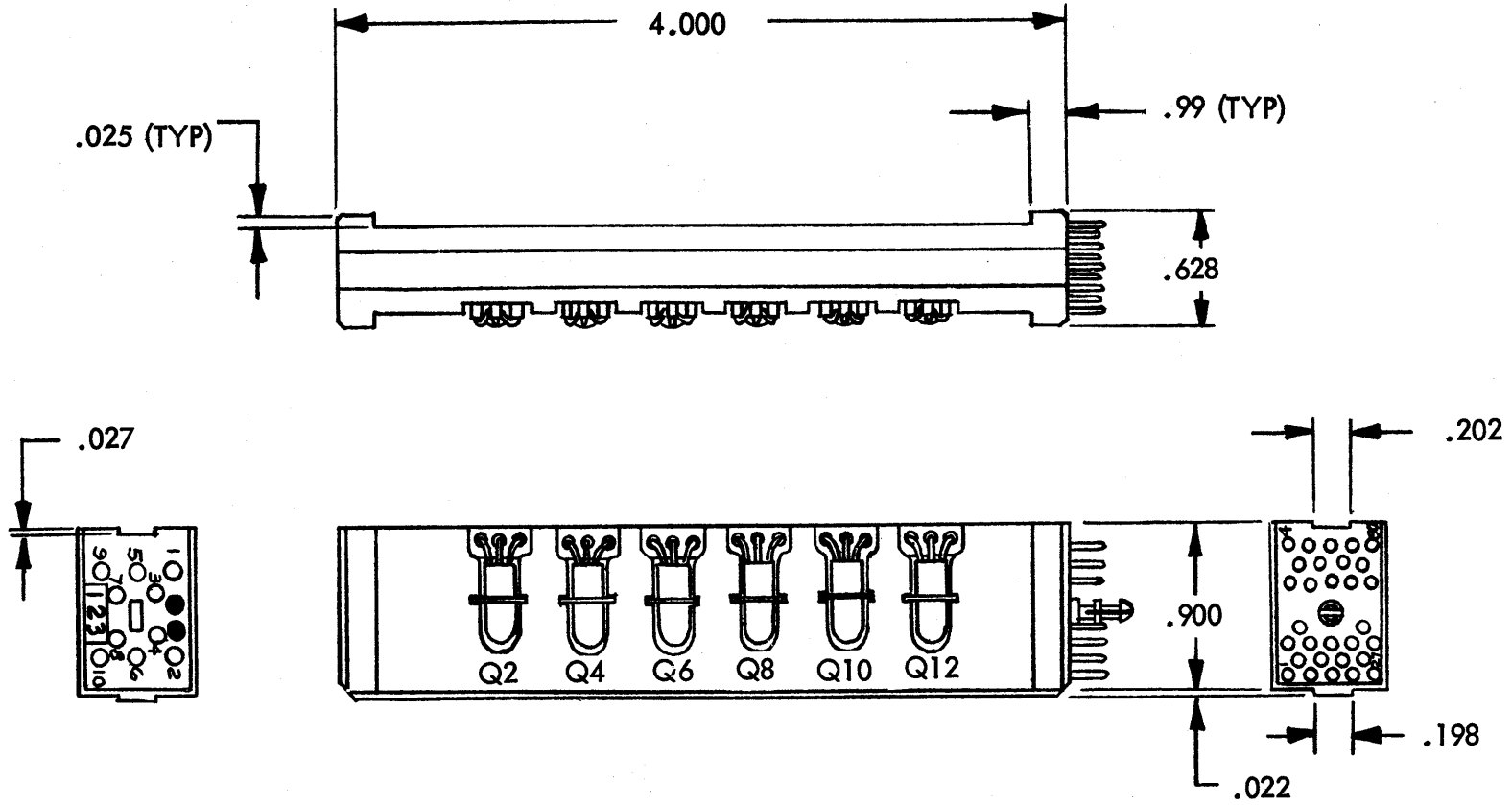


Figure C-4. Electronic Circuit Stick Dimensions

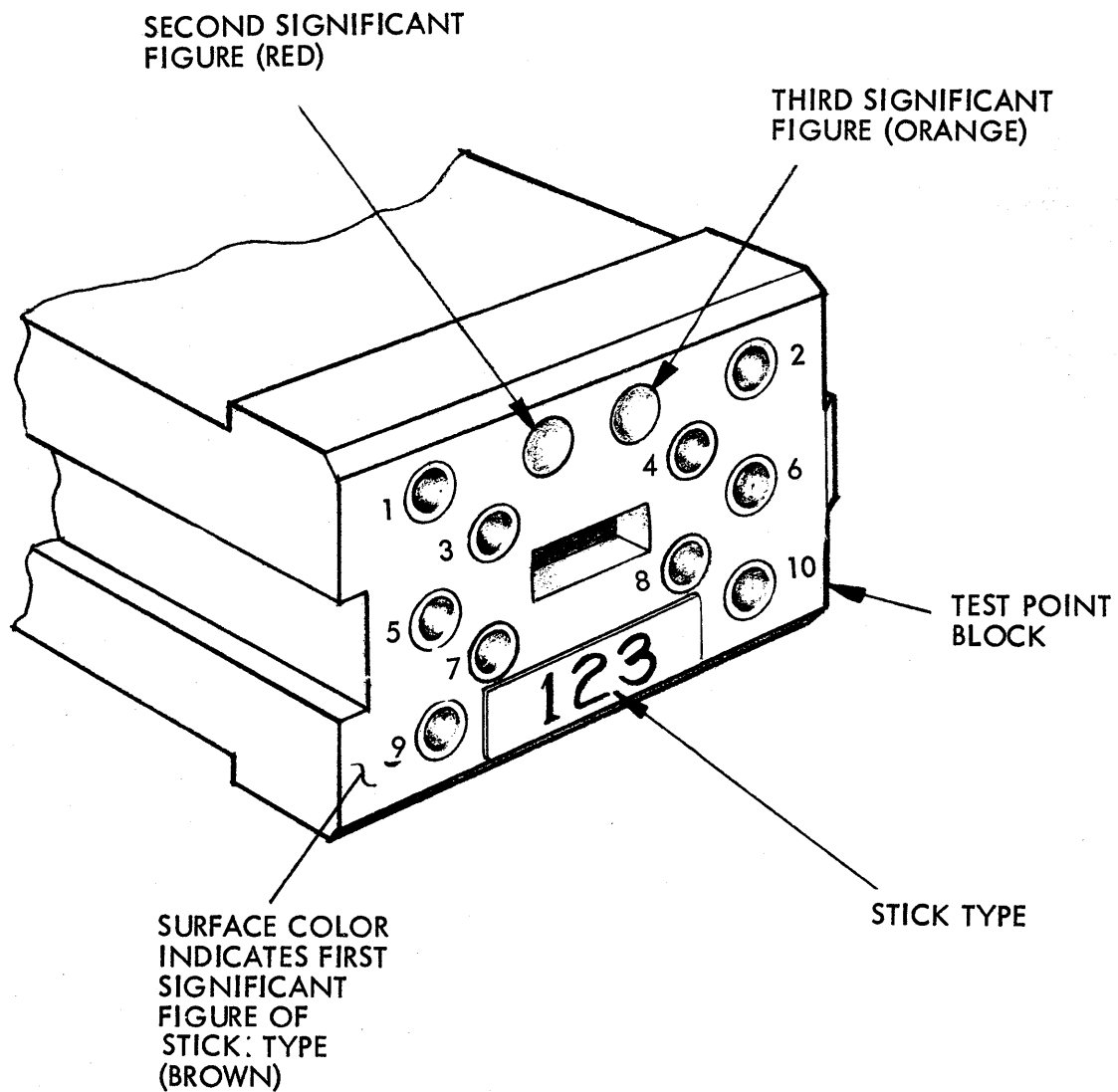


Figure C-5. Test Point Blocks

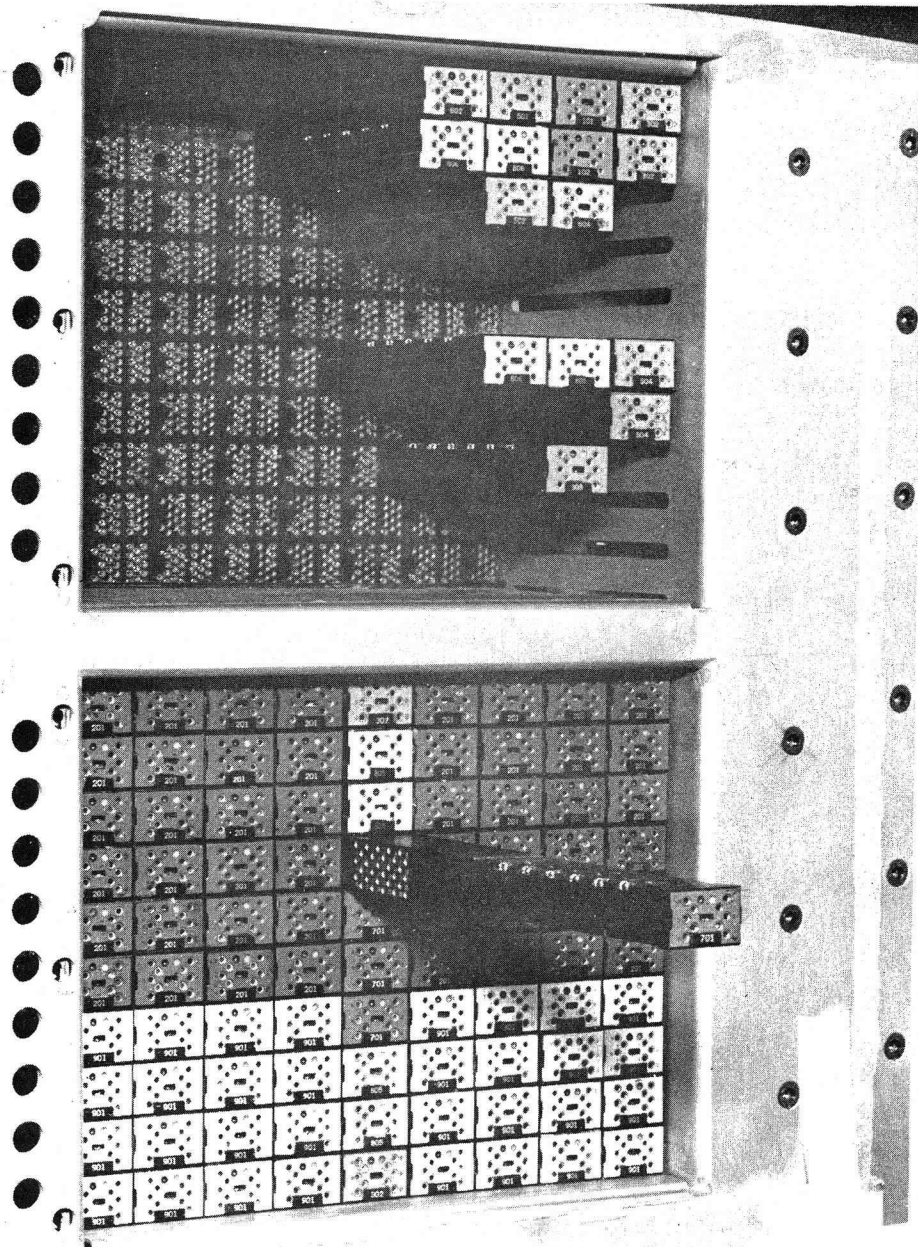


Figure C-6. Electronic Circuit Sticks (Vertical Stacking)

Before encapsulation of the assembly, it is performance-tested with a special transistor mounting fixture. Encapsulation of the stick is then done before the transistors are mounted. The transistors are placed into cavities molded in the sides and a final test is run.

The transistors are mounted externally for three basic reasons:

1. Transistors are not subjected to thermal stresses encountered in potting.
2. The transistor case is directly exposed to the cooling air for heat transfer.
3. Transistor replacement is possible in event of failure.

C. 1. 4 Environmental Test Performance

The stick has been built and successfully tested to the following environmental conditions:

Vibration to 500 cps

Shock to 10g's

Temperature

Operating : -25° F to +125° F

Storage : -80° F to +160° F

Humidity to 95 percent

A typical test report is shown below:

Vibration:

<u>Cycles/sec</u>	<u>Amplitude</u>	<u>Result</u>
10-55	0. 016DA (2. 5G Max)	No visible resonance
10-100	0. 016DA (8. 2G Max)	No visible resonance
10-55	0. 031DA (4. 8G Max)	No visible resonance
55-200	0. 0049DA (10G)	No visible resonance
200-500	0. 0004DA (5G)	No visible resonance

Moisture resistance per Method 106A of MIL-STD-202B for 95 hours: no visible evidence of physical degradation. To date, 10,000 sticks have been successfully fabricated at two Sylvania locations—Needham, Massachusetts and Muncy, Pennsylvania.

C. 2 CABINET PHYSICAL DESIGN

C. 2. 1 Electronics Drawer

Figure C-7 depicts a typical drawer used for housing the electronics. The slide-mounted drawer is 23 inches deep; the height and width of the drawers vary depending on the complexity of the circuits. The drawer is ruggedly constructed of welded aluminum. The forward portion contains up to seven nests, one upon the other, each with the capability of accepting 130 sticks for a maximum of 910 sticks. If there is a requirement for additional sticks, they may be added by removing power supplies.

An air plenum along one side of the nests serves to maintain the proper operating temperature of the electronics. Both air plenum and the nests are constructed as part of the drawer. The power supplies and/or other electronic modules, at the rear of the unit, are mounted directly to the air plenum. This system minimizes the air requirements in that the exhausted air from the sticks is used in cooling the power supplies in addition to minimizing the air resistance due to intermediate mounting pieces.

Cooling air is balanced by varying the size orifice holes along the forward portion of the nests. Air drawn into these orifices is directed across the sticks into the air plenum and transmitted into the system air ducts by means of a flexible hose. Additional metering is accomplished by varying the air intake into the drawers. Sufficient air will be supplied to maintain the transistor case temperature at a maximum of 140° F. Approximately 28 cfm of air will be required per module of 130 sticks.

C. 2. 2 Drawer Mounting

The unit is mounted on three slides. Two slides located on the bottom of the drawer support the required load and the third slide contributes stability necessary for optimum ruggedness. Based on tests performed on the AN/MPQ-32 drawers, this solid design eliminates the necessity of shock absorbers. The placement of nests in the forward position of the drawer results in the necessity of only partial opening of the drawer for testing and/or trouble-shooting. When the drawer is partially opened, the bulk of interdrawer wiring is exposed for

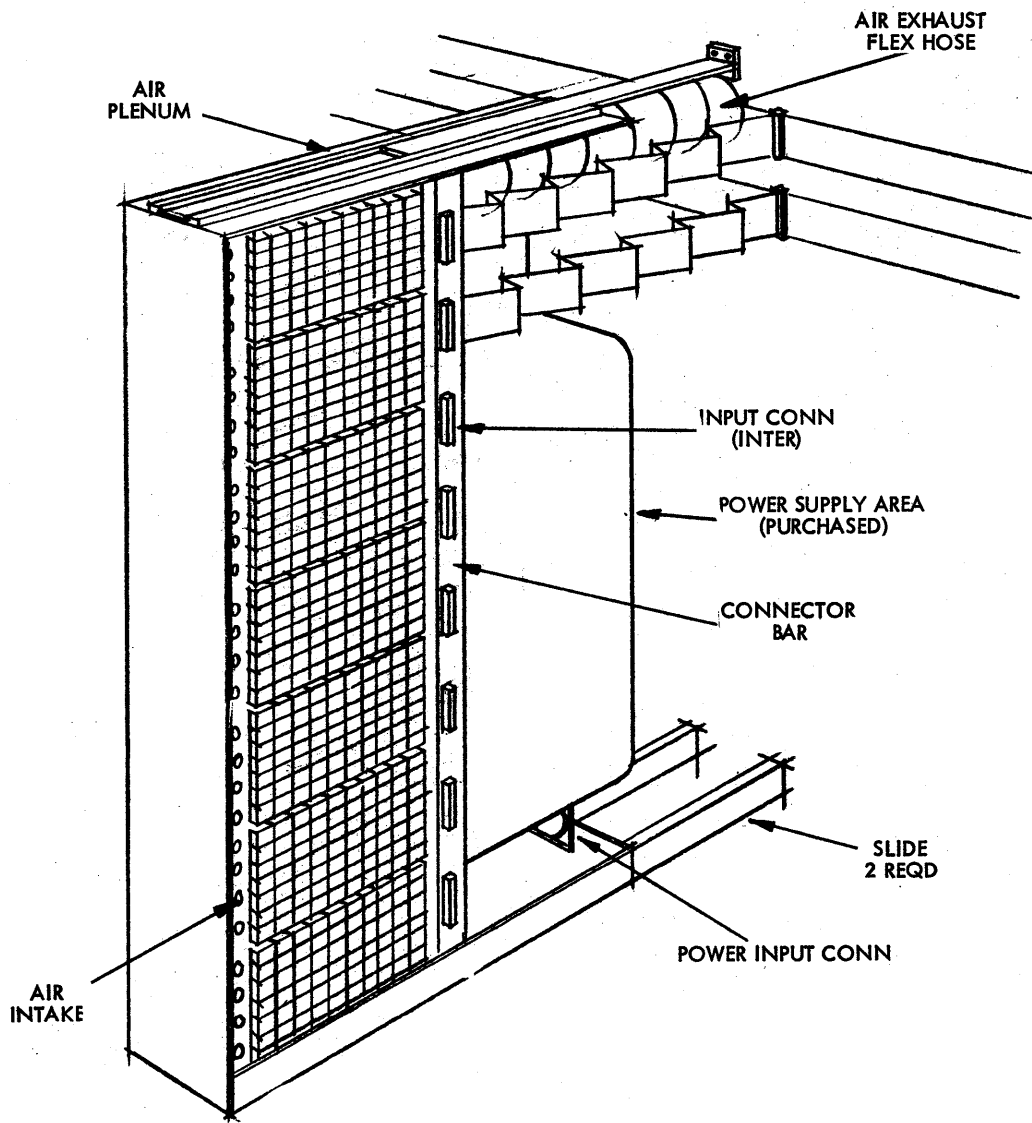


Figure C-7. Typical Drawer Layout (Detailed)

maintainability. This advantage allows minimum use of personnel area for maintenance. The drawers will be mounted onto structural members bolted in place between two ducts. The cooling air will be exhausted into the upper duct and air intake will be from the lower duct. Two drawers will fit into a standard 19 inch rack opening.

Crimped poke-in contacts are used in the female connector with rear insertion and front extraction. The crimped terminations achieve a high reliability and the rear insertion and front extraction result in simplified maintenance. Point-to-point wiring is used in the nest areas. In production quantities, this area is adaptable to multi-layer printed wiring which would lower assembly costs and increase reliability even further.

Ground noise is suppressed through a unique method developed by Sylvania. The strip female connector used to mate with the stick is assembled to a ground plane. These connectors are molded of diallyl phythalate conforming to MIL-M-14. They are then plated with copper, followed by gold, on the sides and back for continuity. Thirteen connectors are then mounted to a ground plane that constitutes one module. The ground plane is fabricated of aluminum gold-plated over copper. It must be noted that the gold-on-gold contact by assembly of the connectors to the ground plane ensures no ground loop; this is further ensured by a common bus soldered to each turret lug on the female connector. This frame is then assembled to a chromate-film finished aluminum frame that has a low electrical resistance.

A front plate on the drawer contains handles for ease in withdrawing the unit and any indicators or switches needed. The plate is supplied with RFI gaskets to prevent any RFI leak.

C. 2. 3 Drawer Connectors

The connectors located along the air plenum as shown in Figure C-7 are readily accessible when the drawer is opened. Flexible cables which fold like an accordion will be utilized in interconnecting the drawers to a bus mounted along the walls of the shelter. The flex-cables achieve an inexpensive, space-saving technique of interconnecting.

C.3 SHELTER PHYSICAL DESIGN

Sylvania has considerable experience in installing signal equipment in vans and shelters. This experience was acquired on the many different van installations of the various MOBIDIC systems, the Random Access Memory installation in shop trucks delivered on the MOBIDIC B System and in the AN/MPQ-32 Radar System Control Shelter. Sylvania is aware of the Signal Corps shelter installation requirements and is prepared to meet these requirements in the ATACC Computer.

C.3.1 Shelter Modifications

The shelter design and layout has been considered in keeping with the building block product line. A typical shelter modification, shown in Figure C-8, shows the shelter divided into two areas: Personnel area and equipment area. The equipment area is located along both side walls of the shelter for the entire length of the shelter and extends out 23 inches from the shelter wall. The remaining space is the personnel area.

The equipment area contains computer equipment cooling system, cable ducts, equipment mounting structure, computer power wiring and control, and computer bussing. The personnel area contains convenience outlets and other items for operator use, lighting, and heater and air conditioner for operator's comfort.

The computer equipment cooling system is comprised of an air intake duct, an exhaust duct and blowers. The intake duct is located along the side walls at the floor of the shelter. Air enters the intake duct through filtered openings located on the side walls of the shelter. The openings are located high enough on the shelter wall to clear the body of a standard 2-1/2-ton truck. Registers on the ends of the duct are provided for shelter air to the computer equipment during cold weather operation or in the event of air conditioner failure. They also provide an air path for exhausting ventilation air which can be admitted through the shelter doorway.

The equipment cooling exhaust ducts are located along the side walls of the shelter at the ceiling. Centrifugal blowers installed at both ends of these

ducts provide 1000 cfm of air each at four inches of water head. The blower is arranged so that it can discharge through the side walls of the shelter or discharge back into the shelter for cold weather operation. Adjustable openings are provided in both ducts at each equipment mounting area, so that air balancing in each of these areas can be accomplished easily. An area along the length of each duct is sectioned off from the air duct for a hinged cable duct which is accessible from the personnel area. The cable area in the exhaust duct is used for signal distribution cables while the cable area in the intake duct is used for power distribution cables.

C. 3. 2 Equipment Mounting Area

The equipment mounting area is the space between the air intake and exhaust ducts, and measures approximately 56 inches high by 23 inches deep. This area can be divided by modular structural members which are bolted to the reinforced intake and exhaust plenums. The members can be located on a pitch to provide any combination of 17-3/4 (19-inch panel) or 37-1/8 inch (38-3/8 inch panel) wide clear openings up to the equivalent of four 19-inch panel openings per shelter wall as shown in Figure C-8. Simple sheet metal skins are provided between the front and rear structural supports to provide an air baffle for each opening. This arrangement has made the equipment mounting completely modular.

An AC power control and distribution panel is provided on the curbside wall by the door. This panel contains power distribution and control for the computer equipment. Power is distributed from this panel through cables in the power cable duct to each equipment mounting area.

Each shelter contains all of the computer buses that are associated with the equipment for the shelter type. The Central Processor shelter contains the Main Frame buses, High Speed Input/Output Buses, and the Low-Speed Input/Output Buses. The High Speed Input/Output Shelter contains the High Speed Input/Output Buses and the Low Speed Device Shelter contains the Low Speed Input/Output Buses. All buses will be made of flexible printed wiring cable mounted along the shelter walls. At each equipment mounting area a receptacle is provided to allow the installation of any piece of computer equipment into any mounting area.

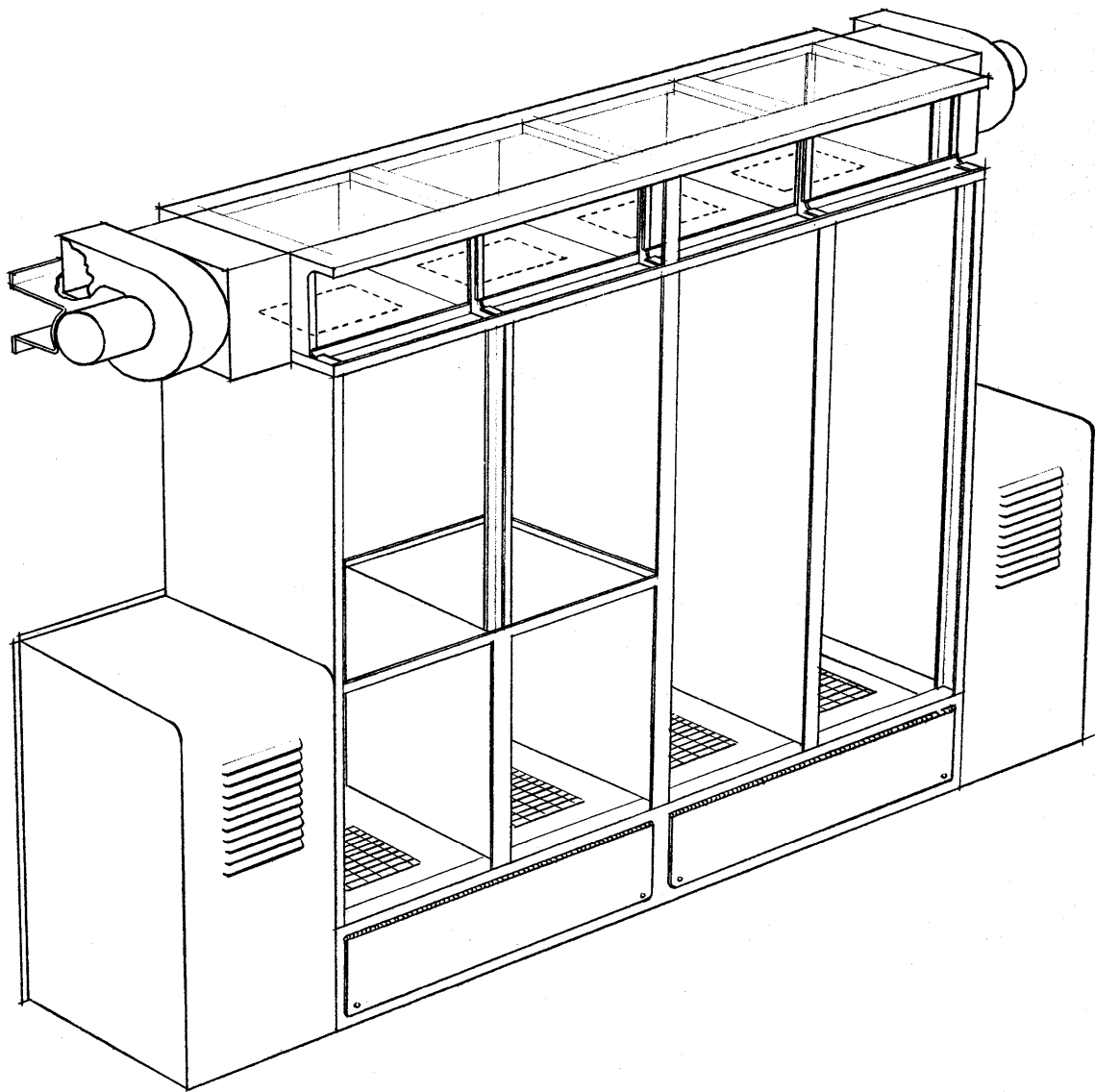


Figure C-8. Typical Shelter Modification

Interconnections between the computer equipment modules and the system buses are made through printed wiring jumper cables which fold in accordion fashion. This same type cable will be used to interconnect the various computer equipment modules, and will be routed between the units through the signal cable duct. The use of flexible printed cable in this application provides an inexpensive, reliable, light-weight, small size cable.

The shelter input connector panels are located in the rear wall of the shelter. Weather proof connectors are mounted on panels through the shelter wall. All of the shelter types will contain the following connector panels:

A power input panel will be provided on the curbside rear wall. The panel will contain a power input receptacle and a ground stake lug.

A communication panel will be provided on the roadside rear wall. This panel will contain four "Spiral-Four" Connectors, eight Binding Posts and an intercom receptacle.

In addition to the above connector panels, the Central Processor shelter will contain a Communication Terminal Equipment Panel with facilities for 24 channels of input and output connections located on the roadside rear wall; Two High Speed Device Panels with facilities for three input/output buses and control and display connectors; and two Low Speed Device Panels with facilities for one input bus, one output bus and control and display connections. The Device Shelters will contain one bus input panel for those buses required within the shelter.

C. 3. 3 Personnel Area

The personnel area is approximately 30 inches wide running the length of the shelter. The area will be illuminated with fluorescent lights, but incandescent lights will be provided for emergency use and as partial illumination during cold weather operation.

A 60,000 BTU/hr. gasoline heater per MIL-H-11511 will be mounted to the floor at the front wall. (The dry bulb temperature corresponding to the maximum (ET) effective temperature of 71° F at 75 percent relative humidity for Winter operation is given in the "A. S. H. A. E. Comfort Chart for still air, 15 to 25 feet per minute as 73° F. D. B. Using this figure for the maximum personnel

heating differential, $\Delta T = 73^{\circ} F - (-65^{\circ} F) = 138^{\circ} F$; and using a "K" factor of 0.40 BTU/Hour/ $^{\circ} F/Sq. Ft.$) The total heating loss is 31,390 BTU/Hour which can be easily supplied by the 60,000 BTU heater.

A 9,000 BTU/Hour air conditioner per MIL-A-14372 will be mounted on the forward wall. The worst case tropical conditions at 0° latitude is an ambient temperature of $125^{\circ} F$. The internal temperature should be $80^{\circ} F \pm 2^{\circ} F$ (ET) at 75 percent R.H., which corresponds to a dry bulb temperature of $84^{\circ} F$ on the A.S.H.A.E. Comfort Chart. Using a "K" factor of 0.40 BTU/Hour/ $^{\circ} F/Sq. Ft.$, the heat load of two people and a solar heat load for the personnel area roof, the total heat loss of 8,920 BTU/hour which under worst conditions described, can be adequately handled by the 9,000 BTU/hour air conditioner.

Additional equipment provided will include a blackout curtain at the back door, a 10-pound carbon dioxide type fire extinguisher, a ground stake and ground cable, and an intercom.

Intervan shelter cables will be provided with each shelter. These cables will be molded neoprene jacketed cable 300 feet long with weather proof connectors at each end. Cable strain relief grips will be provided at each connector end. The cable set provided with each shelter will enable that shelter to be tied to the Computer Shelter and to the Prime Power Distribution Box.

All air openings through the shelter wall will be provided with water-tight, hinged covers. All other openings will be fitted with water-tight panels to maintain air tightness of the original shelter.

APPENDIX D

ATACC RELIABILITY

D.1 GENERAL

This appendix constitutes a reliability analysis of the Fielddata Computer and the Digital Magnetic Tape Transport. The inherent reliability of any equipment is highly dependent on factors applied during the design stage. Sylvania's reliability organization is well staffed to support the design groups in optimizing system reliability within performance, cost, and schedule objectives.

D.2 RELIABILITY OBJECTIVE, IN DETAIL

Sylvania's reliability objective, consistent with the scope of MIL-STD-441, states that the Fielddata computing system shall provide, as a minimum, an MTBF of 100 hours which must be met with a 90 percent confidence level, while the Digital Magnetic Tape Transport shall have an MTBF of 160 hours, similarly met with a 90 percent confidence level. The equipment must also be capable of operation on a 24-hour basis with no more than 15 minutes' maintenance every other day, excluding head cleaning, plus a six-hour maintenance period per 30 days of operation.

D.2.1 Availability; Ratio of Uptime to Total Operating Time

For most ground electronic systems where repair is feasible, an appropriate measure of system capability is an availability numeric. This can be defined as the ratio of system uptime to total operating time. From the above requirements, where downtime periods are specific, it seems more appropriate to consider these downtime periods as occurring randomly in time, provided that the accumulated downtime does not exceed that specified. With this interpretation, it is determined that out of a total of 720 hours the equipment must be up for 710.25 hours, thus giving an availability requirement of 98.6 percent.

D. 2. 2 Overall System Reliability

Sylvania's approach was to analyze the equipments and shelters separately. Once it is known what equipments make up a system, the mathematical methods contained herein can be utilized to determine the overall system reliability. The reliability program outlined below is designed to show how the inherent reliability of the proposed equipment is estimated, optimized, and verified.

D. 3 AVAILABILITY METHODOLOGY

Taking for example a one-unit subsystem having a constant failure rate, λ , and a constant repair rate, μ , an expression is required which defines instantaneous availability at any time, t ; i. e., the probability that at any instant of time the system will be operating satisfactorily. Given this, one can determine interval availability or total uptime from the relationship

$$A = \frac{1}{T} \int_0^T P_O(t) dt \quad (1)$$

where

T = total time period of interval

$P_O(t)$ = instantaneous availability

Let $P_O(t)$ be the probability that the system is up at any instant of time, and $P_F(t)$ the probability of its being down at any time. Therefore, $P_O(t) + P_F(t) = 1$ and $P_O(0) = 1$. The system can only be in one of the two possible states at any time, t ; accordingly, the difference equations satisfying these conditions can be written:

$$P_O(t + \Delta t) = P_O(t)(1 - \lambda\Delta t) + P_F(t)\mu\Delta t \quad (2)$$

$$P_F(t + \Delta t) = P_O(t)\lambda\Delta t + P_F(t)(1 - \mu\Delta t) \quad (3)$$

Rearranging terms, dividing through by Δt , and taking the limit as $\Delta t \rightarrow 0$ result in the following differential equations:

$$P_O'(t) = -(\lambda + \mu)P_O(t) + \mu \quad (4)$$

$$P_F'(t) = -(\lambda + \mu)P_F(t) + \lambda \quad (5)$$

From one of the initial conditions, i. e., $P_O(0) = 1$, it can be shown that:

$$P_O(t) = \frac{\mu + \lambda e^{-(\lambda+\mu)t}}{\lambda + \mu} \quad (6)$$

and

$$P_F(t) = \frac{\lambda - \lambda e^{-(\lambda+\mu)t}}{\lambda + \mu} \quad (7)$$

Since the probability of the system being up for a time period T is desired, this is obtained as follows:

$$A = \frac{1}{T} \int_0^T \frac{\mu + \lambda e^{-(\lambda+\mu)t}}{\lambda + \mu} dt = \frac{\mu}{\lambda + \mu} + \frac{\lambda}{T(\lambda + \mu)^2} - \frac{\lambda e^{-(\lambda+\mu)T}}{T(\lambda + \mu)^2} \quad (8)$$

As T becomes large, the above relationship reduces to so-called steady state availability or:

$$A = \frac{\mu}{\lambda + \mu} \quad (9)$$

For a system which requires all subsystems to be operable for satisfactory performance, total system availability is given by:

$$A_S = \prod_{i=1}^n \frac{\mu_i}{\lambda_i + \mu_i} \quad (10)$$

where

μ_i = repair rate of i^{th} subsystem

λ_i = failure rate of i^{th} subsystem

D. 4 ANALYSIS OF FIELDATA COMPUTER

Figure D-1 shows a reliability block diagram of the Fieldata Computer and the estimated failure rates, λ , in percent per thousand hours. For this analysis, all functional units are considered to be operating in series when all system functional capabilities are required, so that a failure of any one unit causes unsatisfactory performance of the system.

For n units in series, the system probability of survival is given by

$$P_S(t) = P_1(t) \cdot P_2(t) \cdot P_3(t) \cdot P_4(t) \cdots P_n(t) = \prod_{i=1}^n P_i(t) \quad (11)$$

where all $P_i(t)$'s in the system are exponential, Equation 11 becomes:

$$P_S(t) = e^{-\lambda_1 t} \cdot e^{-\lambda_2 t} \cdot e^{-\lambda_3 t} \cdots e^{-\lambda_n t} \quad (12)$$

$$P_S(t) = e^{-(\lambda_1 + \lambda_2 + \lambda_3 \cdots \lambda_n)t} \quad (13)$$

$$P_S(t) = e^{-\sum_{i=1}^n \lambda_i t} \quad (14)$$

and the MTBF (m) is given by:

$$m = \int_0^{\infty} e^{-\sum_{i=1}^n \lambda_i t} dt = \frac{1}{\lambda_1 + \lambda_2 + \lambda_3 \cdots \lambda_n} \quad (15)$$

where λ is expressed in failures per hour.

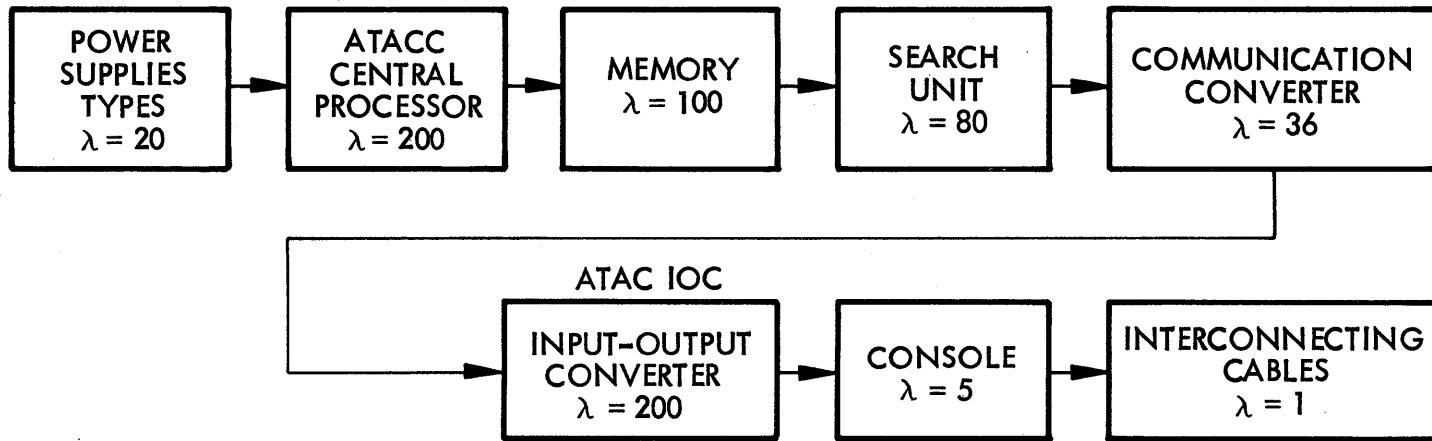


Figure D-1. Reliability Block Diagram of Fielddata Computer

From the series system in Figure D-1 and Equation 15, the estimated MTBF of the total ATACC Computer System is significantly better than 120 hours.

D. 5 RELIABILITY STUDY OF MOBIDIC LOGIC CIRCUITRY

To provide sufficient assurance that the MOBIDIC circuitry has achieved a high degree of reliability, a study was conducted on the central processor because it is accepted as typifying pure MOBIDIC logic. Data on MOBIDIC 7A was selected due to the large amount of useful reliability information obtained under fully operational field conditions. Such information supplies more suitable reliability data for evaluation of system performance in that it contains no bias which might be present in controlled laboratory testing. Many demands are imposed on a system in the field which cannot easily be duplicated or anticipated in the laboratory. It is usually prohibitive to accumulate enough running time during laboratory testing to make statistically valid statements as regards system reliability, because of time, cost, and number-in-sample constraints. However, data from a fully operational system in the field is not limited by those constraints.

D. 5.1 Data Used in Study

Because of limitations in resources for collecting and evaluating field data, two periods were chosen as displaying representative system reliability data of the MOBIDIC 7A. These were periods for which the data was available in complete form, encompassing the six months of initial installation just after arrival in Europe and the most recent four months during which the equipment was fully operational.

TABLE D-1. MOBIDIC CENTRAL PROCESSOR LOGIC (7A)

Time Interval	Cumulative Operating Time	No. of Failures
1 Feb 61 - 31 July 61 (initial installation)	3700	3
14 Sept 62 - 15 Jan 63 (fully operational)	2600	1

Number of modules in Central Processor - 4300
 Total Component Elements - 70,000
 (The MOBIDIC module contains about 17 component elements.)

TABLE D-2. MOBIDIC LOGIC CIRCUITRY RELIABILITY

Type	No. of Modules Tested	Test Conditions	Element Component Hours	Analysis of Test Results				
				No. of Failures	Module MTBF 60% Confidence	Module MTBF 90% Confidence	F/R 60% Confidence %/1000 hr.	F/R 90% Confidence %/1000 hr.
MOBIDIC Central Processor	4300	Actual Field Conditions	441×10^6	4	1,302,404	846,563	0.068	0.118

D. 5. 2 Equation for Availability of Central Processor

The availability of the Central Processor during the time intervals used is given by:

$$A = \frac{MTBF}{MTBF + MTTR} \quad (16)$$

The following tabulation indicates that the availability of the Central Processor improved as the system tended toward fully operational status.

TABLE D-3. MOBIDIC CENTRAL PROCESSOR AVAILABILITY

Central Processor	Cumulative Operating Time (hrs)	No. of Failures	MTBF (hrs)	MTTR (hrs)	Availability
1 Feb 61–31 July 61	3700	3	1233	0.5	0.9996
14 Sept 62–15 Jan 63	2600	1	2600	0.5	0.9998

The demonstrated reliability of MOBIDIC logic circuits is based on many cumulative hours of operating time under actual field conditions, a superlative factor for determining system reliability.

D. 5. 3 Reliability of "Cordwood" Packaging Technique

Sylvania has at present two parallel reliability test programs in progress for determining the reliability of the "Cordwood" logic packaging technique.

D. 5. 3. 1 Room Temperature Test on MPQ-32

One test involves the MPQ-32 1A Computer, which contains 1,370 module sticks being operated at room temperature. Since the start of the formal test, the computer has accumulated some 200 hours of operating time with a single

failure. This represents a total of 274,000 stick-hours with only one stick failure. Although the results look promising, it is still too early to make statistically valid statements about the stick failure rate.

D.5.3.2 Smaller System Tested Under Environmental Stresses

A combination reliability environmental test is also in progress, which involves a small system of 59 sticks placed in an environmental chamber and subjected to the cycle shown in Figure D-2.

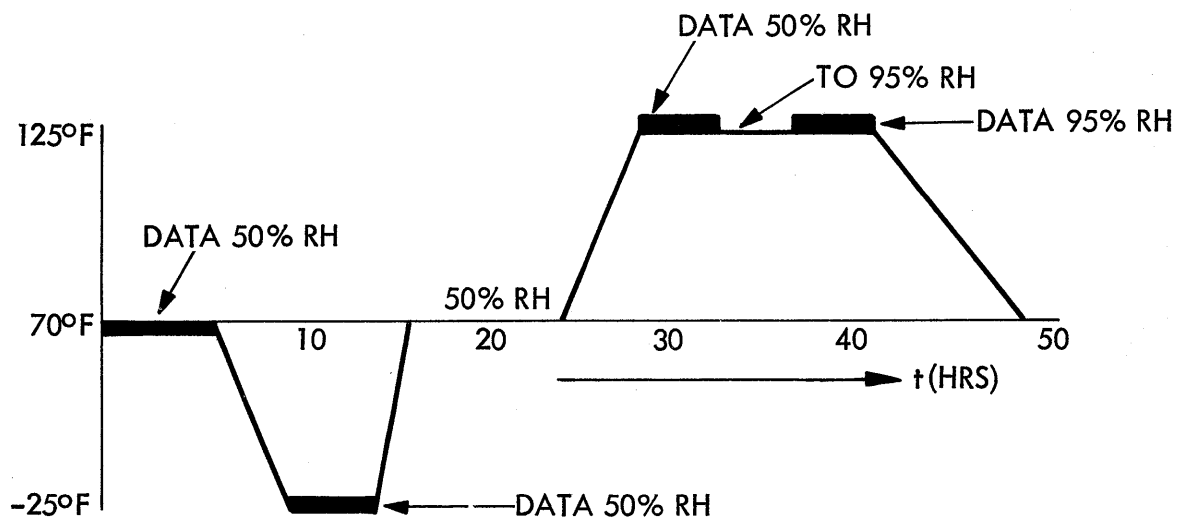


Figure D-2. Environmental Cycle, Stick Test

D.5.3.3 Technique Employed and Result Obtained

At the time of data taking, a series of key waveforms are monitored to detect malfunctions. To date, the sticks have accumulated about 400 hours of test time with only two failures, representing a total of 23,600 stick-hours with two stick failures. It should be noted that the environmental test cycle is subjecting the sticks to a range of severe environments periodically every 48 hours.

D. 5. 3. 4 Planned Test Period and Data Available

Both of these reliability tests will continue for at least 720 hours, and log books maintained on them are available for inspection and verification at all times.

D. 6 ANALYSIS OF DIGITAL MAGNETIC TAPE TRANSPORT

Sylvania has, developed and currently operational, a Militarized Digital Magnetic Tape Transport which does not employ redundancy. If, however, during Phase I of the present program a particular area of the system demonstrates a high failure frequency, and if it is deemed necessary that this portion of the equipment have a high probability of being up at any time, then redundancy techniques for increasing subsystem MTBF will be generated.

D. 6. 1 Reliability Figures for Tape Transport

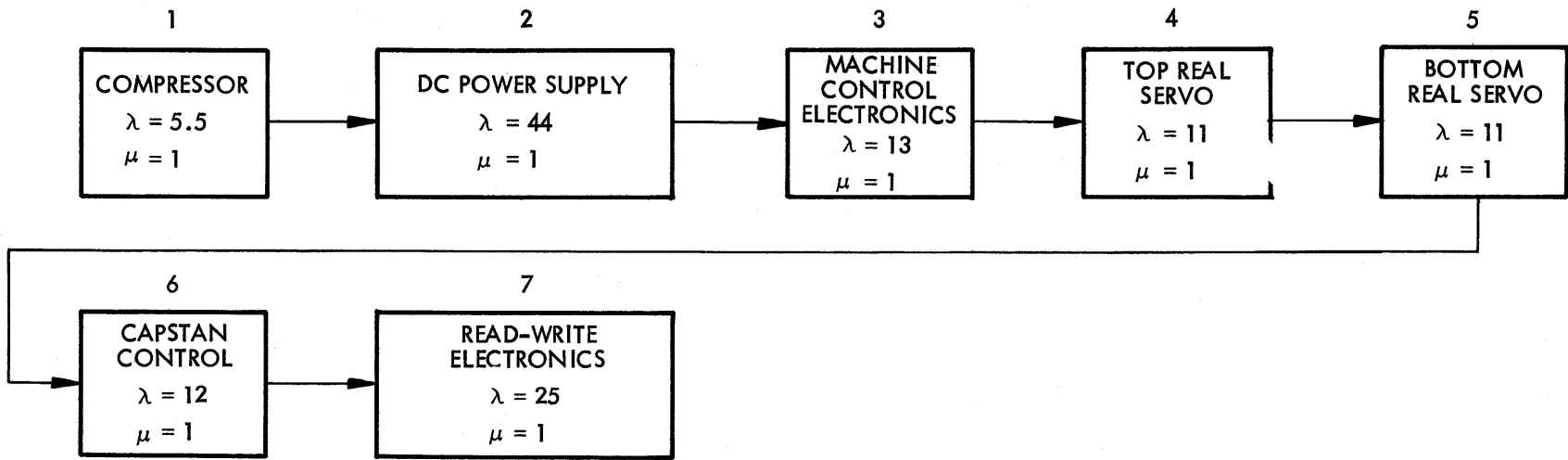
Figure D-3 shows a simplified reliability block diagram of the Digital Magnetic Tape Transport and the estimated failure rates and repair rates. The same assumption made in the analysis of the Fielddata Computer regarding series operation is made in this analysis also. System availability from Figure D-3, utilizing Equation 10 is given by:

$$A_S = \prod_{i=1}^7 \frac{\mu_i}{\lambda_i + \mu_i} \quad (17)$$

$$A_S = 0.99919$$

The MTBF from Equation 15 is:

$$m = \frac{1}{\sum_{i=1}^7 \lambda_i} = 1226 \text{ hours} \quad (18)$$



NOTE: ALL FUNCTIONAL BLOCKS OPERATING IN SERIES; λ's EXPRESSED IN PERCENT PER THOUSAND HOURS AND μ's IN REPAIRS PER HOUR.

Figure D-3. Reliability Block Diagram of Digital Magnetic Tape Transport

D.7 MAINTENANCE ANALYSIS FOR CERTAIN REPLACEMENT TIMES

There are various components in any large system which must be periodically replaced to maintain the system at some specified reliability level. Normally, such components undergo some form of wearout distribution function. That is, the failure rate for that component is essentially zero for a given period of time, and rapidly increases once wearout has set in. Such items include motors, gears, bearings and other mechanical devices, found primarily in the I/O devices.

D.7.1 MTTF for Affected Items

The MTTF (mean-time-to-first-failure) must be determined for these items, given that replacement occurs sometime before their mean lifetimes expire. During the program, a complete analysis will be undertaken to evaluate the life distributions for such components used in the various equipments. It will then be possible to plan replacement time periods for these components.

D.7.2 Mathematical Evaluation of the Problem

To illustrate the mathematical approach in the evaluation of such problems, the following analysis is presented. Graphically, the problem is presented in Figure D-4, involving a component whose failure density function is Gaussian with mean μ ; replacements are planned at time periods T where $T < \mu$. The approach is developed for a general distribution function and then extended to that shown in Figure D-4 and illustrated for a specific problem.

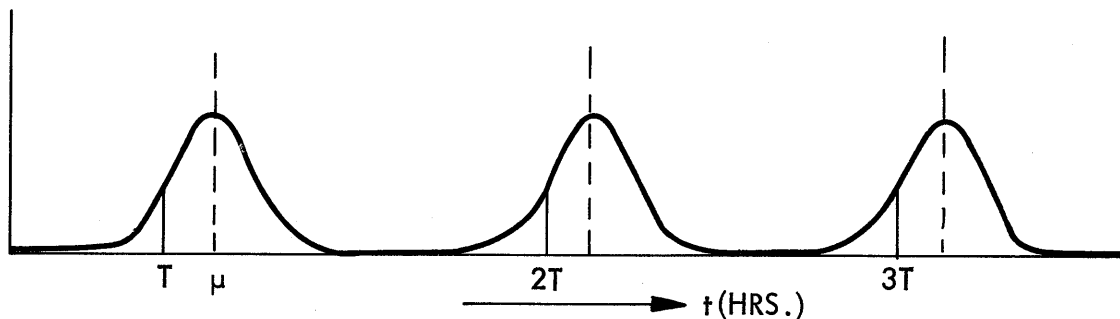


Figure D-4. Failure Density Function

D. 7. 2. 1 Analytical Method Applied

This calls for an analytical expression relating MTTF as a function of a component's failure density function and the time replacement periods, T. The reliability, R(t), for specific intervals is given below:

$$R(t) = 1 - F(t) \quad 0 \leq t \leq T \quad (19)$$

$$R(t) = [1 - F(T)][1 - F(t - T)] \quad T \leq t \leq 2T \quad (20)$$

$$R(t) = [1 - F(T)]^2 [1 - F(t - 2T)] \quad 2T \leq t \leq 3T \quad (21)$$

$$R(t) = [1 - F(T)]^N [1 - F(t - NT)] \quad NT \leq t \leq (N + 1)T \quad (22)$$

R(t) in the N + 1 interval is thus the probability that the component has not failed in N interval times the probability that it survives to t in the N + 1 interval. It is also known that:

$$R(t) = \begin{cases} 1 & \text{for } t = 0 \\ 0 & \text{for } t = \infty \end{cases} \quad (23)$$

Examination of these relationships will verify that the constraints do hold. By definition:

$$MTTF = - \int_0^{\infty} dR(t)t \, dt = \int_0^{\infty} R(t)dt \quad (24)$$

Therefore, from Equation 22:

$$\text{MTTF} = \sum_{N=0}^{\infty} \int_{NT}^{(N+1)T} [1 - F(T)]^N [1 - F(t - NT)] dt \quad (25)$$

$$= \sum_{N=0}^{\infty} [1 - F(T)]^N \int_0^T [1 - F(\tau)] d\tau \quad (26)$$

where

$$\tau = (t - NT)$$

$$d\tau = dt$$

The limits of integration have been changed accordingly. Notable also is:

$$\sum_{N=0}^{\infty} [1 - F(T)]^N = \frac{1}{1 - [1 - F(T)]} = \frac{1}{F(T)} \quad (27)$$

Therefore Equation 26 becomes

$$\text{MTTF} = \frac{1}{F(T)} \int_0^T R(\tau) d\tau = \frac{1}{F(T)} \int_0^T [1 - F(\tau)] d\tau \quad (28)$$

It can be shown that Equation 28 reduces to

$$\text{MTTF} = \frac{1}{F(T)} \left\{ T - TF(T) + \int_0^T \tau f(\tau) d\tau \right\} \quad (29)$$

This is the general expression of any distribution function for MTTF with planned replacement periods of time T.

For the failure densities shown in Figure D-4:

$$f(\tau) = \frac{1}{\sigma \sqrt{2\pi}} e^{-\frac{(T-\mu)^2}{2\sigma^2}} \quad (30)$$

Substituting into Equation 29 gives

$$\text{MTTF} = \frac{T[1 - F(T)]}{F(T)} + \frac{1}{F(T)\sigma\sqrt{2\pi}} \int_0^T e^{-\frac{(t-\mu)^2}{2\sigma^2}} \cdot t \, dt \quad (31)$$

It can be shown by a rather complex integration that Equation 31 reduces to

$$\text{MTTF} = \frac{T[1 - F(T)]}{F(T)} + \mu + \frac{\sigma}{F(T)\sqrt{2\pi}} \left\{ e^{-\frac{\mu^2}{2\sigma^2}} - e^{-\frac{(T-\mu)^2}{2\sigma^2}} \right\} \quad (32)$$

This is the general expression for a Gaussian failure distribution function. To illustrate this, a component is chosen whose mean life $\mu = 1000$ hours, $\sigma = 100$, and $T = 872$ hours. For this example $F(T) = 0.1$.

D. 7. 2. 2 Determination of MTTF

Substituting these values into Equation 32 results in a MTTF of approximately 8500 hours.

D. 7. 3 Future Application of Mathematical Approach

It is interesting to note that this approach adapts readily to an optimization problem which will be explored during the program.

APPENDIX E

PROGRAMMING

E.1 EXERCISE ROUTINES

E.1.1 General

The primary purpose of the exercise routines is to operate all the circuitry in the data processing system to provide assurance that the system meets operational specifications. As such, the fault detection capability, in addition to being concerned with faulty components in the system, must also consider the possibility that errors in the logic design and wiring may exist. For this reason, the diagnostic capabilities of the exercise routines are limited and, to a large degree, depend on the ability of the engineers or maintenance personnel using the programs. The exercise routine is designed using a gradual build-up of hardware testing from the minimum machine to the entire system in a logically ordered sequence.

The main criteria in the design and implementation of the exercise routines are those judged necessary to allow the most successful performance in meeting the requirements of the following two tasks.

1. In-house Checkout—Proving the logic design of the system and detecting "Bugs" that may have developed during the manufacturing process is important in this area (i.e., faulty components or miswiring). To accomplish this task, some troubleshooting aids are required: for instance, the test program must indicate the test case that is failing and the contents of data registers that may be significant for the particular test case. In addition, some means must be provided for locking the computer, in a specific test case, so that an oscilloscope may be used for troubleshooting.
2. Acceptance Tests—To perform this task, the exercise routines must demonstrate that the entire computer system is capable of performing to specifications. Special programming considerations required for this application include the ability to continuously loop the programs for relatively long periods of time and provide permanent records of the test results.

E.1.2 Test Routines

The following program units satisfy the requirements outlined above.

1. Central Processor Exercise
2. Core Memory Exercise
3. Input-Output Exercise

E. 1. 2. 1 Central Processor Exercise Program

All functions of the Central Processor are thoroughly exercised in this program unit. Included in this category are the following:

- a. Instructions—Each instruction, except for those directly related to Input-Output operations, is executed to insure its correct operation under all specified conditions.
- b. Registers—All registers, internal to the Central Processor are tested to insure data handling capabilities. Any unique register operations such as arithmetic, shifting, incrementing or decrementing are also included.
- c. Flip-Flops—All programmable flip-flops are exercised to insure proper operation and control transfer relative to sensing, setting and resetting.
- d. Program Interrupts—Any program interrupts unique to the Central Processor including trapping mode operations are tested.
- e. Console and Errors—These tests insure the correct operation of all manual controls and indicators on the operator's console that can be controlled or interrogated by the internal program. Error conditions are purposely generated, where possible, to check built-in hardware detection circuitry in both the Halt on Error and No-Halt on Error modes. Due to the stop and go nature of these tests and the operator intervention required, a manual control is provided to allow these tests to be by-passed so that all the automatic testing of the remainder of the Central Processor may be cycled continuously.

The following control options are provided through simple manual switches at the operator's console.

1. Halt on Error
2. Print Errors
3. Cycle tests continuously
4. Load in next test program from Magnetic Tape or paper tape

5. By-pass halt tests

6. Cycle in a specific test case.

E.1.2.2 Core Memory Exercise Program

This program unit exercises all memory locations for proper operation using the following test patterns.

- a. Test all "ones"
- b. Test all "zeros"
- c. Test alternating ones and zeros and complement
- d. Test Address sequencing to insure every address may be accessed.
- e. Test Ripple one—Each bit position is tested for storing a "one" when the remaining positions are "zero"
- f. Test Ripple zero—Each bit position is tested for storing a "zero" when the remaining positions are "ones"

In addition to the test patterns described above, provisions are made to allow entering any desired test pattern through the Word Switch Register keys at the console.

The following control options are available through simple manual controls at the operator's console.

1. Halt on Error
2. Print Errors
3. Compile Errors for an edited printout at the end of the test
4. Cycle tests continuously
5. Select a specific test pattern
6. Select a specific test location
7. Select a test pattern from the Word Switch Register
8. Select the number of memory modules (16K per module) to be tested
9. Load in next test programs from magnetic tape or paper tape

E. 1. 2. 3 Input-Output Exercise Programs

The purpose of these programs is to execute a comprehensive test of all the input-output circuitry. This task is subdivided into two main programs:

1. Input-Output Converter (Mod II) and related peripheral equipment.
2. Communications Converter and related peripheral equipment (AN/TYC-1).

In both of these programs, the following control options are provided through simple manual controls at the operator's console.

1. Indicate errors by halting
2. Indicate errors by printing
3. Cycle program continuously
4. Repeat a single test routine continuously
5. Select the I/O devices to be tested. (Any number and combination of devices within the limits of the program described below and the system capacity.)
6. Load in the next program from magnetic tape or paper tape.

I/O Converter (Mod II) and Related Peripheral Equipment

The general approach used by this program is to first exercise as much converter circuitry as possible with very limited use of the actual I/O devices, then to use the converter to perform exhaustive tests on the I/O devices themselves. Once the converter and units have been thoroughly exercised, the program then exercises system operations by demonstrating capabilities such as simultaneous operations and program interrupts. The general subdivision of tests within the program is as follows:

1. Basic I/O Converter Tests—This test is concerned with exercising circuitry in the I/O Converter that may be checked with one I/O device. Included here are checks of the I/O control flip-flops, memory accessing by the converter, converter handling of the I/O control word, and simple operations involved in controlling an I/O device.

2. Paper Tape and Typewriter Tests—This sub-unit includes tests of the paper tape punch, paper tape reader and typewriter. The paper tape punch is exercised by generating a test paper tape using all data character configurations and modes of operation. The generated tape is then used as input to a check of the paper tape reader. Here again, all modes of operation are used (octal, interprets sign, non-interpret sign, single character, etc.) in reading the tape. Error conditions in interpret sign and reading octal when Fieldata characters are on tape are programmed into this test. To provide the ability to test the reader without depending on the punch a test paper tape is provided.

The typewriter is exercised by printing all possible characters available and using all controls, such as Tab and carriage return. This test requires visual observation of the printed format and content to detect errors.

3. Magnetic Tape Drive Tests—This test demonstrates the ability of the magnetic tape units to write and read all data configurations, write and read using worst-case data patterns, and to be controlled for all motions (start, stop, forward, reverse) required in magnetic tape operations. Start-stop operations are checked ranging from a sequence of extremely short blocks to long blocks of data. During the course of this test all modes of operation programmable on magnetic tape are exercised.
4. Card Reader and Card Punch Tests—The testing of this equipment is accomplished in a manner similar to that used for checking paper tape. The card punch is checked by generating a deck of punched cards using all controls and worst-case data configurations to check alignment. This deck is then used as input to the card reader tests where the validity of the punching and the capabilities of the reader are checked simultaneously. A correct test deck is provided in the event it is desired to test the reader as a separate unit independent of the punching unit.
5. Printer Tests—This unit is exercised by generating a printed output using all possible characters, all print positions, and all control functions unique to the printer. The test includes printing a single character per line and a ripple printout. Visual observations of the printed format and content is required to detect errors.
6. Random Access Storage—This section of the program demonstrates the capability of the Random access storage device to operate within specifications. Tests that are included are:
 - a. Worst-case data patterns
 - b. Word addressing functions (the capability to randomly access words)

- c. Random access timing tests
 - d. The ability to record, read, and check all word locations (Bad spot test)
7. Simultaneous Operations—This test routine system tests the devices that have been previously unit tested in that the capabilities of the Mod II I/O converter in performing simultaneous operations is demonstrated. Assuming the operator has designated a sufficient number of I/O devices to create full load conditions, the program sets up conditions to test the system at full capacity in the Input/Output processing area. Also included in this test is the capability of the I/O converter to assume the role of an off-line control unit while continuing its functions in one-line I/O processing.
 8. Program Interrupts—During this routine all program interrupts are tested for proper operation.

Communications Converter and Related Peripheral Equipments

The function of this program is to thoroughly exercise the Communications Converter and the AN/TYC-1 digital data transmitter and receiver. To accomplish this task, a test switch is provided to allow looping the output of the AN/TYC-1 back into the input to provide a means of having the equipment automatically check itself. The test plan is divided into three main areas:

1. Converter Test—This portion of the test is mainly concerned with converter functions such as control word handling and control flip-flops.
2. AN/TYC-1 Unit Tests—This portion of the program checks each selected AN/TYC-1 as a unit. All data patterns and transmission frequencies are included.
3. Simultaneous Operations—The function of this test section is to demonstrate system capabilities by operating the available devices simultaneously. Control provisions allow for testing the maximum system capacity in this manner.

E. 2 DIAGNOSTIC PROGRAM SYSTEM

E. 2. 1 Overall Test Plan

In order to provide a consistent approach to troubleshooting malfunctions in the Data Processing system, three levels of activity are dictated. (See Figure E-1.) The first level consists of manual and semi-automatic procedures during which the operator plays an important role in initiating actions and visually observing results. The second level, which would be the normal starting point in troubleshooting procedures, consists of a preliminary diagnostic routine designed to test basic operations and simple use of the core memory. Successful completion of the preliminary diagnostic routine automatically initiates the main Central Processor test routine at level 3 where all diagnosis is performed automatically. Should an error be detected at the second level, the program will either

1. Perform diagnosis of the malfunction (for instance a memory failure that does not affect the area occupied by the preliminary diagnostic).
2. Indicate that the malfunction seriously impairs the ability of the preliminary test to perform any diagnosis with reasonable assurance and that the manual or semi-automatic procedures at the first level must be resorted to.

The design of the diagnostic routines is based on the following assumptions.

1. The system has been completely operational at some point prior to testing so that no logical errors exist.
2. The malfunction under diagnosis is a steady-state failure. (Intermittent and transient failures will require the use of marginal checking to aggravate the error condition.)
3. In the case of more than one failing component in the system at any one time, it is assumed the first detected and isolated malfunction will be repaired before subsequent diagnosis can be considered valid.

E. 2. 2 Description of the Levels of Diagnostic Analysis

E. 2. 2. 1 First Level Diagnostic Procedure

Manual Test Procedure

The purpose of these procedures is to provide a systematic approach to troubleshooting when the central computer is completely inoperative. The type

2ND LEVEL

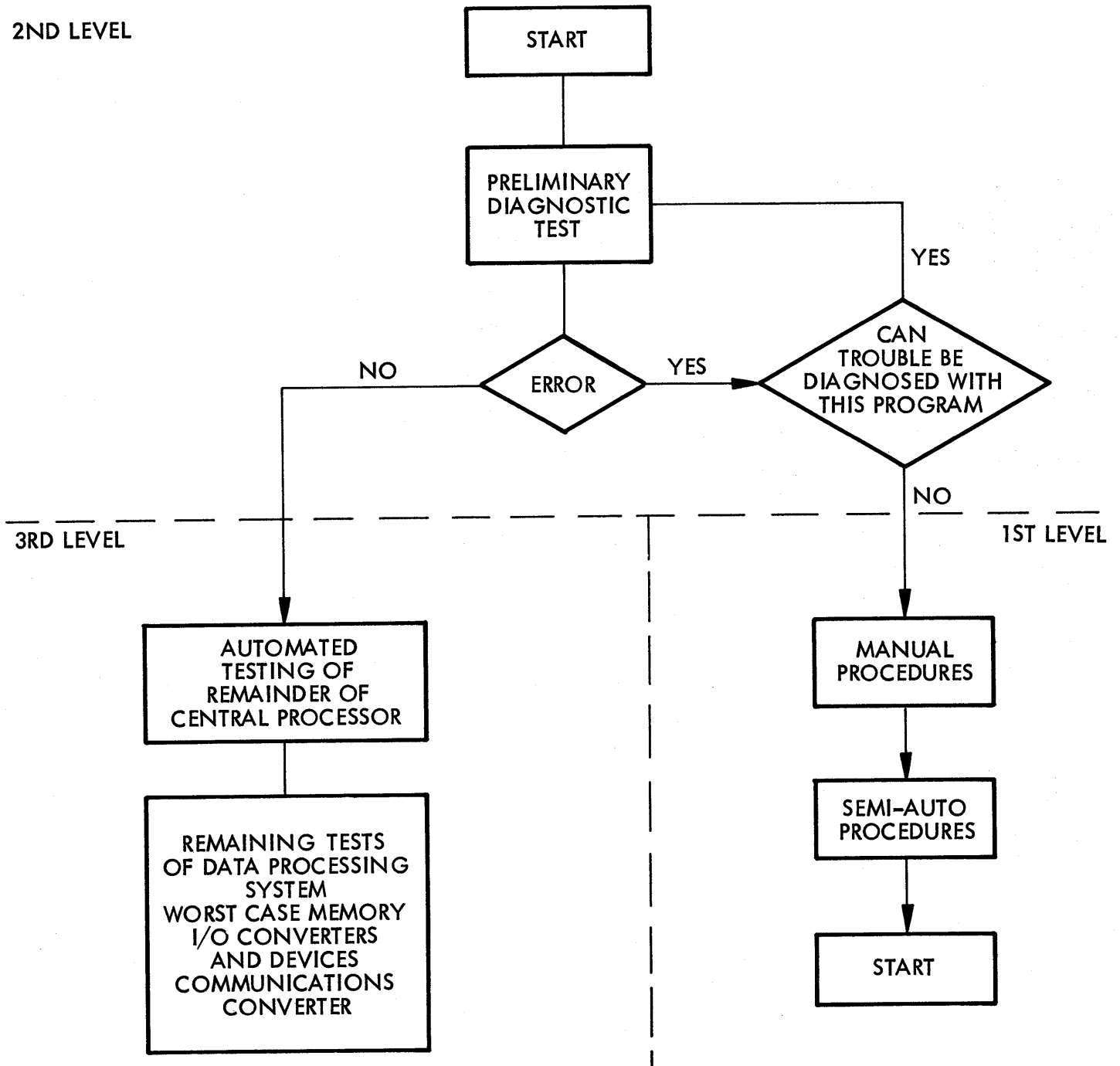


Figure E-1. Levels of Activity Used in Troubleshooting Data Processing System

of participation required by the operator will be simple manual executions and observations. The procedures will be prepared in the form of a manual outlining 1) the action to be taken, 2) what to observe, 3) what the results should be, and 4) the action to be taken if indications are abnormal. The step-by-step format is designed to the level of detail required to make its use simple for a relatively unskilled operator.

Examples of the type of action required by the operator are:

1. Manually displaying critical registers for "hot" bits
2. Repetitive depressions of the Start at Program Counter button and observing proper incrementing of the program counter
3. Checking Power Supply indicators
4. Simple manual Read-in/Read-out operations through the operator's console.

Semi-Automatic Test Procedures

The purpose of these procedures is to provide an intermediate step between strictly manual operations and fully automated diagnosis. This test section fits into the overall scheme of systems testing by providing diagnostic capabilities in the following machine areas.

1. The minimum input circuitry required to load a program into memory
2. The minimum memory area required to store the preliminary diagnostic routine
3. Some basic instruction requirements

During this test, the operator is still required to initiate certain actions and observe results. However, at this level his participation will be limited to operator controls to initiate the loading of a sequence of very short programs, ranging from 1 to 10 instructions, from paper tape and observing the operational results through console displays. The approach described here is based on the fact that a failure symptom, especially in this basic machine area, can be more easily defined and recognized before it has had a chance to compound itself to a point where the failure symptoms become ambiguous.

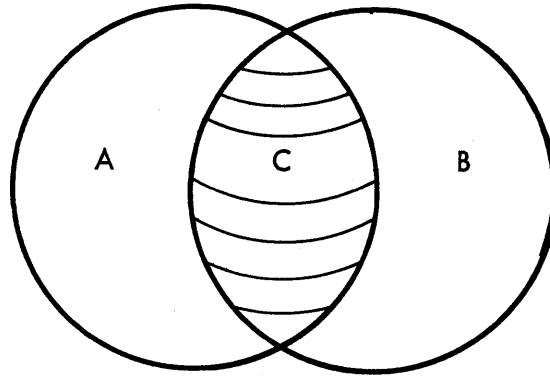
As in this case of the manual procedures, the operator is only required to follow a detailed step-by-step set of procedures outlined in a manual. The manual, in addition to specifying the actions and results to be observed, will also indicate the circuitry under test and the probable cause of failure when the proper indications are not present.

E. 2. 2. 2 Second Level Diagnostic Test--(Preliminary Diagnostic Routine)

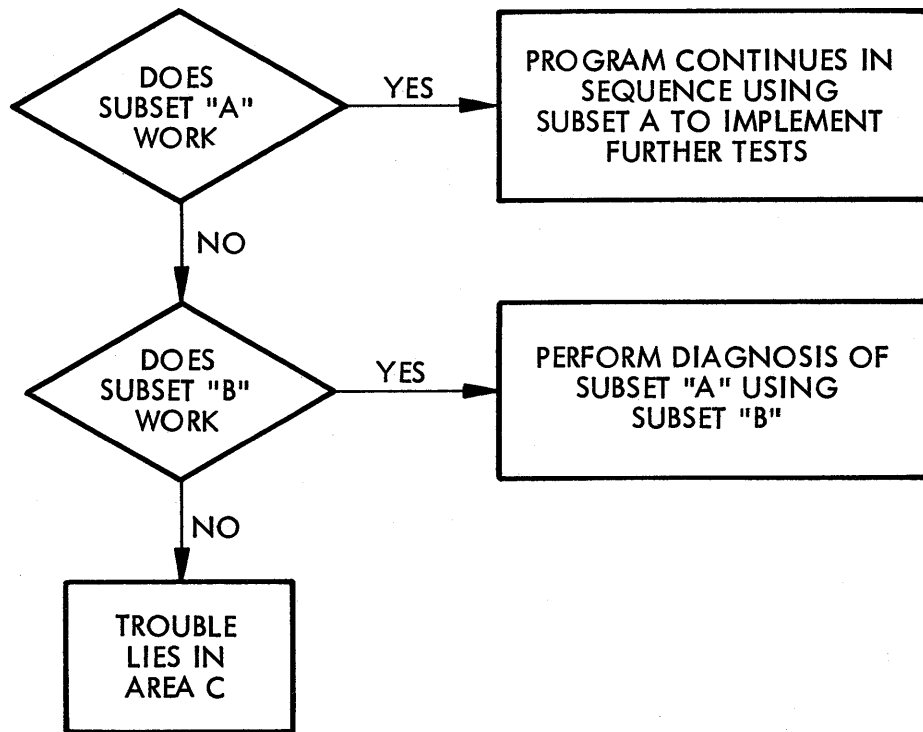
At this level, fully automatic testing is attempted for the first time in the form of a preliminary diagnostic test routine. As previously stated, this level would be the normal starting point in the diagnostic procedure used for troubleshooting under field conditions. If the program runs successfully it will automatically initiate a comprehensive test of the remainder of the Central Processor at level 3. In the event of failure at this level the program will either perform diagnosis on the malfunction, if it is capable, or indicate, to the operator that the nature of the failure is so basic that diagnosis must be performed at the first level. The program will indicate the proper action to be taken by the operator by simple typewriter output, if possible, or information displayed on the console which may be cross-referenced to a maintenance manual provided for this purpose.

Initially, the preliminary diagnostic routine will attempt to prove a subset of control processor instructions required to implement testing of the remaining core memory locations and the remaining Central Processor instructions. This is accomplished by taking advantage of the inter-relationship of the various instructions in terms of common circuitry. The concept used is illustrated graphically in Figure E-2.

The "A" area represents a subset of computer commands complete enough to implement some basic test routines, (minimum of one data moving command and one conditional transfer command). The area of circle A represents the area of actual computer hardware used by instruction subset "A". Area "B" represents another subset of computer commands, selected to have as little as possible in common with "A" but also capable of performing some basic test routines. The area of "B" represents the hardware required by instruction subset "B".



(a)



(b)

Figure E-2. Graphical Representation of Interrelationships of Instructions in Terms of Common Circuitry

The area "C" represents the area of hardware common to both subsets. Analysis of hardware then proceeds as shown by the flow chart of Figure E-2b.

Once the program has determined a "basic set" of Central Processor instructions may be relied on, a test of the remaining core memory locations is executed. (The size, in terms of instructions, of the preliminary diagnostic will be kept to a minimum.) Each memory location is tested for its ability to hold ones and zeros and for proper addressing. The addressing function is tested by initializing each location with a unique constant (its own address) and then checking to insure that no locations have been modified due to failures in the address selection circuitry. Diagnostic analysis of memory failures is based on the inherent symmetry in the design of a core memory device.

Successful completion of the diagnostic tests at this level will automatically initialize a comprehensive test of the remaining Central Processor instructions.

E. 2. 2. 3 Third Level Diagnostic Tests

This level of diagnostic testing encompasses the major portion of the hardware in the data processing system. The size of the equipment and the testing techniques best suited to the different machine areas requires that the programming task be subdivided in the following manner.

1. Comprehensive Central Processor Test
2. Comprehensive Memory Test (worst-case data patterns)
3. Comprehensive Input/Output Test (including associated peripheral device)
4. Communications Converter Test (including associated equipments)

Comprehensive Central Processor Test

This program assumes that the preliminary diagnostic routine has been executed successfully. The design of the Central Processor diagnostic takes full advantage of the inter-relationship of the various computer commands in terms of micro-instructions, arithmetic registers, and data registers common to more than one instruction. Test modules are designed to thoroughly exercise all functions of each instruction. These modules are then arranged in a logical order so

that diagnosis starts with the basic computer developed by the preliminary diagnostic routine and continues the development of the Central Processor as each module introduces new hardware to be tested. The decision making process involved in the diagnosis takes into account the operations that were properly executed, prior to the detection of an error and the additional information that must be assessed after the error has occurred. For example, an investigation of the mechanization equations for a Fielddata type of computer reveals that the LGN (Logical Negate) command is identical to the CLA (Clear and Add) command in performing the functions of accessing memory and gating the data into the A-register. What makes LGN unique is the complementing function in the A-register after the data has been brought in. Therefore, it is necessary that the CLA command be tested prior to the LGN so that a failure in the LGN can be isolated to the logic completely unique to LGN. At this point however, additional information to further isolate the failure may be analyzed by the program. For instance, is the failure in a single register position, indicating that complementing logic unique to that register position is failing, or are all positions failing, indicating the malfunction is in the complementing control logic? To proceed further, this same complementing logic, in part, is also used by the ADD (different signs) and SUB (like signs) commands so that diagnostic decisions in these areas must in turn consider the operation of the LGN command.

The discussion above should serve to illustrate how inter-related the various commands within the Central Processor complex are and how these relationships are analyzed in the construction of a consistent diagnostic approach.

In this manner, the program will attempt to isolate any failure, to a point where the program can specify the general logic under test, pertinent data relative to the failure and the probable trouble source in terms of replaceable elements. Where the inherent logic of the system inhibits diagnosis to a small enough area, the general circuitry under test will be specified. Normally, communications will be made through printed output although provisions will be made for interpreting error halts from console displays and making reference to a maintenance manual when printing is undesirable or impossible. This manual will also provide assistance in interpreting the printed output of the program.

Flexibility in the use of the program is provided through simple manual controls (Sense Switches) at the operator's console. The following options will be available:

- a. Indicate errors by printing
- b. Indicate errors by halting
- c. Ignore errors
- d. Repeat entire program (life test)
- e. Repeat a specific test module
- f. Indicate errors immediately (at time of occurrence)
- g. Compile errors for an edited printout at the completion of the program

Comprehensive Memory Diagnostic (Worst-Case Patterns)

This program assumes that the Comprehensive Central Processor diagnostic is operating correctly so that the computer instruction repertoire is available for diagnosis and testing.

The preliminary diagnostic routine was concerned with the ability to store data properly and to address all locations correctly in memory, while this diagnostic assumes these functions are operating correctly and is concerned with the affects of marginal conditions that may be revealed when the memory is subjected to worst-case patterns.

Through the manipulation of the background pattern in the memory array, each location is subjected to variations of the following tests.

1. Cause bit pick-up or turn "zeros" to "ones." This is accomplished by initializing a background pattern such that the half-select noise generated on the sense winding when the location is selected will be maximized in one direction and tend to appear as a "one" signal to the sense amplifier.
2. Cause bit drop-out or change "ones" to "zeros." In this case, the background pattern is initialized so that the half-select noise on the sense winding is maximized in a direction that will produce a signal opposing the signal produced by the "one" in the selected test location. This opposing signal tends to cancel out the "one" and appears as a "zero" to the sense amplifier.

Error diagnosis in the memory system is based on the fact that a failing component in a coincident-current memory will produce a predictable pattern of failures because of the inherent symmetry in the design of the device. The technique employed by this diagnostic involves compiling all the errors during a test and presenting them in a format designed to make these characteristic patterns easily recognized and referenced to a maintenance manual where the failing component will be listed.

The following options will be built into the program with control provided through simple manual operations at the operator's console.

1. Indicate errors by printing
2. Indicate errors by halting
3. Ignore errors
4. Repeat the program continuously
5. Select a specific test routine
6. Select a specific memory location for testing
7. Select a specific data pattern for testing
8. Select the amount of memory to be tested (provisions for testing any number of arrays from the minimum system to the maximum system)
9. Indicate errors immediately (at time of detection)
10. Compile errors and edit for a condensed printout of the end of the test

Comprehensive Input/Output Test (Mod II)

This problem assumes that the Central Processor and Memory have been thoroughly tested in all areas not directly related to I/O operations. From this point the diagnostic program gradually develops the I/O system in logically sequential steps designed to isolate failures as much as possible. Initially, interface between the Central Processor, Memory and I/O Converter is tested. During this phase, any reference to an I/O device is made only when necessary to analyze operations at these interfaces and the effects on the I/O device itself are ignored. Analysis is largely concentrated in the following areas.

1. Proper operation of control flip-flops related to I/O operations
2. Transfer of these controls from the Central Processor to the I/O converter
3. Correct operation in accessing and updating I/O control words in memory
4. Proper operation in accessing data words in memory

After these basic functions have been tested, the computer proceeds to a unit test of the I/O devices where the main interface of concern is that between the converter and I/O device through the device switching units. In general, the procedure used in the unit tests of the I/O devices is to first use simple write and/or read sequences with basic use of all the commands and controls. Once basic control is established, vigorous testing of the I/O device itself to fully test mechanical operations and electronic circuitry follows. The final phase of the test procedure involves using these unit-tested devices in a system sense, by operating the circuitry necessary to allow simultaneous I/O processing.

Diagnosis of malfunctions in the I/O area is based on this building block approach plus the fact that considerable circuitry within the converter is common to more than one I/O device. Interpretation of failure symptoms is provided through program printout of errors and reference to a maintenance manual which will indicate the location of the failing element or procedures to aid in further isolation. The general goal is to first isolate the malfunction to the unit level and then to diagnose within the unit itself. In the case of the I/O converter considerable diagnosis can be performed, due to its direct connections with the Central Processor and the core memory in addition to the fact that a variety of I/O devices can be utilized in the fault-isolation procedure. The different I/O devices themselves each require unique procedures but, in general, the diagnostic attempts to distinguish faults resulting because of malfunctions in data handling from faults due to errors in the I/O device control hardware. For example, in the testing of magnetic tape, the analysis, on the part of the program, will be capable of distinguishing between a repetitive failure occurring on each character (because read or write circuitry in one channel is failing) from a failure produced by the fact that tape is positioned incorrectly (because a motion control was malfunctioning). Elimination or inclusion of the I/O converter as the trouble source

is accomplished by examining the results of an identical test sequence on another magnetic tape. In general, the coincidence of identical malfunctions in more than one I/O device will be considered highly improbable for purposes of diagnostic analysis performed by the program and further outlined in a supplementary maintenance manual.

Control options, through simple manual controls at the operator's console are provided as follows:

- a. Halt on error
- b. Print on error
- c. Ignore errors
- d. Cycle the complete program continuously
- e. Repeat a specific test routine
- f. Indicate data errors immediately
- g. Compile data errors for an edited printout at the end of a test routine
- h. Select the devices to be tested (any number of combinations within the limits of a maximum system configuration)

The following is a list of the I/O devices tested by this program with a brief summary of test procedures.

The paper tape and typewriter tests – The paper tape punch circuitry is checked in generating a paper tape that is in turn used as a test input for the paper tape reader. For purposes of fault isolation, a test paper tape known to be correct must be available at all times. The typewriter is tested using a specified printed output. Abnormal indications detected through visual observations are then interpreted by a supplementary maintenance manual.

Magnetic tape drive tests – The tape unit is tested in all modes of operation. Tests included:

- a. Simple data handling
- b. Worst-case patterns to cover the extremes of the recording frequency
- c. Worst-case start-stop tests

Card Reader/Punch tests—The procedures for this test are similar to those used in the paper tape reader/punch tests. The actual test routines will differ because of the different control circuitry and data patterns required by the equipment.

Printer tests—This equipment is tested by generating a printed output with a specific format and content. Abnormal results must be detected visually and interpreted with the use of a supplementary maintenance manual.

Random Access Storage—Special considerations for this test are

- a. Decoders for determining word address, track address and zone
- b. Individual Read and Write heads
- c. Random access timing tests
- d. Worst-case data patterns

E. 2. 2. 4 Communications Converter Test

This program also assumes the Central Processor and core memory have been thoroughly tested. The program locates and diagnoses malfunctions in the communications converter and the AN/TYC-1 digital data transmitters and receivers. To facilitate this test procedure a special test switch is provided to loop the transmitter output back into the receiver so that testing is completely under program control.

In the diagnostic analysis, the philosophy is similar to that used for the I/O converter. Initially the program checks all control functions that may be interrogated by the Central Processor without using the AN/TYC-1. Once these basic functions have been proven, I/O operations are brought into play only insofar as necessary to supplement further testing of the converter in the areas involving accessing and updating control words from memory, transfer of controls between Central Processor and converter, and memory access for data. The behavior of the AN/TYC-1 devices at this phase of testing is ignored because many of the converter functions may be tested even though the device may be failing.

The next step in the test process involves unit-testing the AN/TYC-1 devices and includes

- a. Proper handling of all data configurations
- b. Worst-case data patterns
- c. Testing transmission at all data rates
- d. Testing operation in all possible modes

The final phase of the procedure involves testing the circuitry necessary to allow simultaneous operations at maximum specified system capacity. As in the case of the I/O converter fault isolation, the program initially attempts isolation to the unit level followed by fault isolation within the unit. The interpretation of failure symptoms is provided through program printout and reference to a supplementary maintenance manual that will indicate the location of the failing element or procedures to aid in further isolation.

The following control options will be made available through simple manual operations at the operator's console.

- a. Indicate errors by halting
- b. Indicate errors by printing
- c. Ignore errors
- d. Repeat the entire program continuously
- e. Repeat a specific test routine
- f. Indicate data errors immediately
- g. Compile data errors for an edited printout at the end of a test routine
- h. Select the number of AN/TYC-1 devices to be tested (capabilities will provide to include the maximum system capacity)

E. 3 ATACC COMPUTER SHIFT OPTION

E. 3. 1 Summary

A shift option, in the presently unused beta bits of Fielddata instructions, improves instruction performance. Instruction execution time on bit, character or partial word fields will be decreased by 10 percent to 33 percent, and memory space correspondingly reduced. Total instruction memory requirements will be reduced by at least 4 percent. The modification is compatible with existing programs; it will definitely enhance the ATACC capability for searching and editing.

This option would use bits 16 through 27 for a secondary shift instruction. It would apply to all instructions except control transfers or instructions where these bits are now used. The shift would occur after the primary instruction had been executed. The bits would have the following meanings:

Bits 27	Direction of shift (left or right)
26	Registers (Accumulator, or accumulator or Q register)
25-19	Number of places

E. 3. 2 Fielddata Instructions

The Fielddata instructions were adapted from the TX-2 in 1956. These instructions had been proved to be general purpose, though it was impossible at that time to foresee how adapted they were to Field Army programs.

Since then, it has been recognized that considerable space and time is required to do typical bit, character, or partial-word field editing or comparing. Any attempt to improve these operations on a basis of "what instructions would help" however, opens a Pandora's box of "wouldn't it be nice to have an instruction that does....". Therefore, early in 1962 Sylvania set out to determine the suitability of the Fielddata instructions for existing Army and Sylvania programs, and investigate additions or modifications to the instruction set that would meet the following criteria.

1. Economically justifiable
2. Reduce execution time of common instruction sequences
3. Reduce memory space by requiring fewer instructions for these sequences
4. Be completely compatible with existing Fieldata programs and library routines

E. 3.3 Analysis Program and Results

The most frequently used instructions occupy only 24 or 27 bits of the 36-bit word. Coupling two instructions into one word, would meet criteria 2, 3, and 4 cited above. Experienced programmers could qualitatively justify five uses. These were shifting, comparing, transferring control, skipping, and indirect addressing. The best qualitative judgment indicated that a secondary shift instruction (operating exactly like the present shifts) would both reduce access time and conserve space in bit, character or partial word operations. The other uses were soon eliminated because they were quite different in principle from the Fieldata instructions or could affect only a few instructions.

A quantitative analysis was then made which required determining two facts: how often are shifts actually used in programs and what instructions precede shifts. Five programs were analyzed by a special Sylvania 9400 computer program; a Seventh Army program was manually analyzed by the original programmer.

Instruction counts showed that shifts take about 4% of all instructions. (See Table E-1) The percentage was quite constant across the various programs except for a run which operated solely on whole word fields. The 3.7 percent for the Seventh Army Demand Analysis run would be increased to 4.1 percent if the programmer had straight-line coded rather than used subroutines with tie-in through 179 TRL's. Table E-2 shows the occurrences of each instruction in this program.

Next, shifts were counted in commonly used data handling subroutines. Table E-3 shows that space savings (and time savings if not input-output limited)

TABLE E-1. PROGRAM INSTRUCTION COUNTS				
Program Name	Description	Instructions		
		Total	Shifts	Shift %
Pre-Ops	Hollerith→Fielddata conversion; Input editing formating and conversion to tape.	461	19	4.1
Audit	Verifies consistency of information, size and content of fields.	549	27	4.9
File Maintenance	Maintenance file of contracts and schedules by task and project.	811	38	4.7
Main	Matrix manipulation of whole-word fields.	1,099	28	2.5
FORTTRAN	FORTTRAN assembly program.	5,633	274	4.9
7A Demand Analysis	Determine demands by depot and part for setting re-order quantities (does not include IO).	1,693	63	3.7
	TOTAL	10,246	449	4.4

TABLE E-2. INSTRUCTION OCCURRENCES
SEVENTH ARMY DEMAND ANALYSIS (Excluding I/O Routines)

Load			Move		
CAM	2		MOV	347	
CLA	189		LOD	80	
CLM	5				427
CLS	1				
LGA	4				
LGM	66				
		267			
Arith			Control		
ADD	59		SEN	12	
DVL	4		SNR	34	
MER	6		SNS	18	
MLY	3		TRC	14	
SBM	2		TRL	179	
SUB	50		TRN	8	
		124	TRP	15	
			TRS	9	
			TRU	142	
			TRX	7	
			TRX	65	
					503
Shift			Misc		
SHL	12		ADB	11	
SHR	25		HLT	57	
SLL	20		LDX	4	
SRL	6		RPA	9	
		63	RPT	53	
			SBB	5	
			NOP	34	
					173
Store			TOTAL		
MSK	61				1,693
STR	75				
		136			

TABLE E-3. SUBROUTINE INSTRUCTION COUNTS				
Subroutine Name		Instructions		
		Total	Shifts	Shift %
HFC-3	Hollerith to Fielddata Conversion	110	11*	10.0
F → B	Fielddata to Binary	19	3*	15.8
B → F	Binary to Fielddata	10	1*	10.0
Field Edit	Edit a partial word field (CIA, Shift, LDQ, MSK)	4	1	25.0
Field Access	Load accumulator and position partial word field (CLA, LOM, SHR)	3	1	33.0

*The shift % measures total space, not total time. In these routines, the shifts are in a main loop and are executed once or twice for every bit; most of the other instructions are executed only once for every word or once for entrance and exit.

in repeated data handling loops could range from 10 percent to 33 percent. Both the field access and edit subroutines are used in most Seventh Army programs.

Instruction precedence matrices were constructed for each program. These showed the number of times each instruction was followed by the same instruction or some other instruction. A summarized precedence matrix for the Seventh Army program is shown in Table E-4. The instructions were summarized by the types shown in Table E-2.

These matrices showed that nearly all of the shift instructions were preceded by instructions with available beta bits. Though 16 of the 63 shifts were "preceded" by control instructions, the shifts could have preceded the control instructions without affecting the program. Similarly, the seven shifts following move type instructions (LOD and MOV—neither having available beta bits) could have been done as a secondary option in an instruction preceding the move type. Though both MOV and LOD can affect the accumulator or Q register, the sequence LOD, SLL could have been avoided by preshifting the data prior to loading.

Because a secondary shift command can not be indexed, we manually examined every shift in the Seventh Army program and 50 shifts in the other programs. No shifts in the Seventh Army program were indexed; only two of the 50 were indexed, and both could have been recoded in fewer instructions without indexing.

TABLE E-4. INSTRUCTION SEQUENCE OCCURRENCES
SEVENTH ARMY DEMAND ANALYSIS (EXCLUDING I/O ROUTINES)

		This Instruction Type:							
		Load	Arith	Shift	Store	Move	Control	Misc	Total
Is followed by this Instruction Type:	Load	12	4	16	74	40	105	16	267
	Arith	60	21	11	10	1	13	8	124
	Shift	31	4	5	-	7	16	-	63
	Store	81	29	11	2	3	3	7	136
	Move	9	3	11	9	244	87	64	427
	Control	55	55	6	36	128	190	33	503
	Misc	19	8	3	5	4	89	45	173
	TOTAL	267	124	63	136	427	503	173	1,693

E.4 SEARCH UNIT

E.4.1 Summary

Sylvania concludes that a search unit should not be a major unit in the ATACC product line since present search unit designs:

1. Cannot process either intelligence or non-intelligence files now in use.
2. Increase elapsed processing time.
3. Require more main memory than Central Processor searching.
4. Do not "free" the computer to do related processing.

E.4.2 Application

Search units are intended to reduce Central Processor time in searching files by accepting search criteria from a Central Processor, then independently monitoring the data transfer from file device to main memory.

The following quotation illustrates the need for a search capability in the intelligence system:

Retrieval of data from the system will be initiated by a query or SRI (Standing Request for Information) from an intelligence element. . . A request for data designated as an SRI must specify the duration of time it is to be active. . . The computer queried will respond immediately with data from its files. Simultaneously, it will transmit the query to the other computers in the system which will respond with data from their files. When responses from all computers have been received, the computer initially queried will output a second reply to the requester, incorporating the data from the first reply with the subsequently received data. Data in both replies will be sequenced as specified by the requester. . .

SRI's will be maintained in each computer for the duration of time specified to be matched against incoming data.¹

¹"Objectives and Specifications of the Intelligence System", USCONARC, 16 January 1961.

E.4.3 Design

"The purpose of the search unit is to relieve the computer of the time consuming operations involved in searching through large files of data for a small portion of that data... Thus, the search unit will perform tests to determine desirability of a piece of data read from an I/O device while the computer is free to perform arithmetic or a data processing operation which may be completely unrelated to the search."²

The Informer main memory has 30 preassigned locations for search criteria. Each criteria word has a logical relation, equation term connector and one or two characters for literal comparison with the data. These words are transferred to the search unit when a search is started. The program selects the device holding the file. An IOC starts the device and accepts the input characters for transfer to main memory. The search unit monitors the input characters. In the "valid record" mode, the search unit allows data transfer to memory until it knows the current record cannot satisfy the search. In the "valid block" mode, the entire block is transferred to memory.

E.4.4 Conclusions

1. The Search Unit cannot handle either intelligence or non-intelligence files now in use.

The search unit can only compare on one or two, 6-bit character fields. OACSI uses both a variable number of bits to a character, and a variable number of characters per field. OSCA and 7A, both use fields whose length ranges from 1 to 36 (or more) bits. The search unit also cannot handle two types of commonly used records: multilevel, repetition variable or both. A file of multilevel records has headers and trailers to several levels. A repetition variable record has one or more untagged fields which may occur a variable number of times.

2. The Search Unit increases elapsed processing time.

The elapsed time to search a file must be at least the total time to read the file. For example, a file has

²IBM Informer Final Design Plan

270,000 records of 100 characters each on either magnetic tape or disc. At 45,000 char/sec one search will take approximately 10 minutes. If another query is received 2 minutes after the first, there is no practical way with a search unit to merge the second query with the first. Instead, the first search must be completed before the second can be started, bringing the total time to 20 minutes. A Central Processor program can perform multiple searches and can avoid re-searching. The program would do the first query for 2 minutes. It would then do both the first and second until end of file. Then it would do the second query for the 2 minutes worth of file it had missed, for a total time of only 12 minutes.

3. The Search Unit requires more main memory than Central Processor searching.

Whether a search unit or the Central Processor is used, there must be an equal amount of main memory for valid item storage. A search unit cannot match standing requests for information against incoming data records without a program to file the SRI's on a disc or tape and turning the incoming data records into the search unit criteria format. The alternative of filing the incoming records, then successively loading the search unit with all the SRI's would require starting, reading, stopping and backspacing an incoming data record as many times as there were SRI's. This procedure would take excessive time. Thus a search unit needs two programs; one to turn a query into the search unit format and the second to turn an incoming data record into a search unit format. A Central Processor program needs only a few program switches and a single program to decide whether to pass many queries against one record, one query against many records, or many queries against many records. An extension of the same program could pass a new query against previous queries to avoid a file search entirely if the new query were logically included within previous unsatisfied queries.

4. A Search Unit does not "free" the computer to do related processing.

A search unit precludes Central Processor access to the file being searched. Thus while the search is going on, it is not possible to enter new transactions or change the file contents even though a matching entry may be read into Central Processor memory during the search.

It is possible to do unrelated processing since the search instruction execution is done by the search unit. However, if the most critical fields of a record are tested first (impossible to do with a search unit program) most invalid records can be rejected within five to ten Fielddata instructions. Both the number and execution time of testing instructions would be reduced by the shift option of the ATACC Central Processor.