POLY-88 MICROCOMPUTER SYSTEM
VOLUME I: ASSEMBLY, TEST, AND THEORY OF HARDWARE

Construction NOTE: omit R6 on
All SLAVE Chassis.

POLYMORPHIC SYSTEMS
737 South Kellogg Avenue
Goleta, CA 93017

PLEASE NOTE

Several erratta sheets are included at the end of this manual. Be sure to read the erratta pertaining to volume I before beginning any assembly.

TABLE OF CONTENTS

POLY 88 Microcomputer System Manual
VOLUME I: Assembly, Test, and Theory of Hardware

This volume explains how to assemble and test the POLY 88, a complete microcomputer system that interfaces with an ASCII keyboard and video monitor. It also explains how the hardware works. Volume II discusses system software, and offers hands-on experience with the system.

The assembly and test portion of this volume is intended for those who have unassembled kits. If your POLY 88 is assembled, turn directly to Section A.5, system checkout. That section concerns inserting assembled circuit cards into the chassis and checking for correct operation. Those with assembled systems will find the remainder of this volume interesting mainly as a source of reference.

A. Assembly and Test

1. Check all components for inclusion.

The POLY 88 microcomputer system in unassembled form consists of three packages containing the components for the three sub-assemblies, plus a two-volume manual. The three sub-assemblies are:

a. backplane, cabinet, and power supply.
b. central processor sub-assembly.
c. video terminal interface.

Following are complete parts lists. Check each sub-assembly for inclusion of all components. If any component is missing, see the enclosed warranty.

a. Backplane, cabinet, and power supply.

Backplane and power supply components are packed inside the cabinet. Lift off the cabinet and verify that packed inside it are:

check

( ) backplane circuit board

( ) two boxes of components

The cube-shaped box contains the transformer. The other box contains all the miscellaneous components for the backplane and power supply. They are:

check

( ) 1 line cord

( ) 1 17,000 μF capacitor (15V)

( ) 1 2,000 μF capacitor (50V)

( ) 1 1,000 μF capacitor (50V)

( ) 2 100-pin edge connectors

( ) 1 lighted reset button

( ) 1 lighted power switch

( ) 1 fuseholder with hex nut

( ) 2 plastic slotted card guides

( ) 1 strain relief

( ) 1 3-lug terminal strip

( ) 2 6-amp power diodes (60S05)

( ) 4 1-amp power diodes (IN4003)

( ) 1 330-ohm ½ W resistor

( ) 1 0.1 μF ceramic disc capacitor @16V

( ) 2 100-ohm ¼ W resistors

( ) 2 2200-ohm ¼ W resistors

( ) 1 1000-ohm ¼ W resistor

( ) 1 470-ohm ¼ W resistor

( ) 1 2N5449 transistor

( ) 1 1N4148 diode

( ) 6 hexagonal metal standoffs

( ) 2 0.01 μF ceramic disc capacitors @1KV

(✓) 2 Card guide brackets (one front and one back)
(✓) 4 10-32 screws, lockwashers, and nuts
(✓) 24 6-32 X ¼" screws
(✓) 4 6-32 X ½ screws
(✓) 8 6-32 nuts and starwashers
(✓) 4 rubber feet
( ) 2 flat plastic insulators (or plastic backing on brackets)
(✓) 2 pairs of Molex connectors with assorted pins
(✓) Green, orange, and blue wire (26")
(✓) 1 length of shrink tubing
(✓) 8 small forked standoffs
(✓) 1 2 Amp fuse
(✓) solder
(✓) black wire (6")
( ) Additional edge connectors, if ordered, plus additional 4-40 screws, nuts, and fiber washers, are also in this box.

b. Processor board

Processor and video board components are packed in the remaining two boxes. The processor board box contains clear plastic bags. One bag contains the processor circuit board. The others, numbered starting with Ø, contain the components to be mounted on the board. Check each bag to see if all components are included.

BAG Ø: INTEGRATED CIRCUITS (38 in all)

check
(✓) 1 C8080A central processing unit
(✓) 1 8224 clock generator
( ) 1 C2708 Monitor read-only memory
(✓) 4 AM91L11APC 256 X 4 random-access memories (or type 2111's)
(✓) 6 N8T97B bus drivers
(✓) 3 74LS109
(✓) 2 74LS138
(✓) 2 74LS174
(✓) 2 74LS257
(✓) 2 74LS32

( ) 1 74LS08
( ) 1 74LS132
( ) 1 7425
( ) 1 7407
( ) 1 74148
( ) 1 74LS00
( ) 1 74LS02
( ) 1 74LS04
( ) 1 74LS13
( ) 1 40 pin socket
( ) 3 24 pin socket

BAG #1: HARDWARE

CHECK
( ) 2 6107B-14 Thermalloy heatsinks
( ) 1 6051B Thermalloy heatsink
( ) 1 mica insulator
( ) 3 6-32 X 3/8" screws
( ) 3 #6 star washers
( ) 4 6-32 hex nuts
( ) 1 #6 fiber washer
( ) 1 6-32 X 3/8" nylon screw
( ) 1 LM309K or LM340K-5.0
( ) 1 MC78M12PC
( ) 1 MC79M05PC

BAG #2: DISCRETE COMPONENTS

CHECK
( ) 2 2,200-ohm resistors
( ) 3 1,000-ohm resistors
( ) 1 4,700-ohm resistor
( ) 8 10,000-ohm resistors
( ) 1 470 pF ceramic disc capacitor
( ) 6 10 μF tantalum capacitors

( ) 1 33 μF tantalum capacitor
( ) 1 39 pF ceramic disc capacitor
( ) 31 0.1 μF ceramic disc capacitors
( ) 2 IN4148 diodes
( ) 1 16.5888 MHZ crystal
( ) 5" teflon sleeving
( ) 6" bare wire

The following bags contain components for options that may or may not have been ordered.

BAG #3: SOCKET KIT

check
( ) 4 18-pin sockets
( ) 17 16-pin sockets
( ) 12 14-pin sockets

BAG #4: RECEIVER/TRANSMITTER PACKAGE

( ) 1 MM5307 programmable baud-rate generators
( ) 1 8251 universal synchronous/asynchronous receiver/ transmitter with socket
( ) 1 74LS08
( ) 2 14 pin sockets
( ) 1 1N4148 diode
( ) 1 79L12 regulator
( ) 1 10 μF tantalum capacitor
( ) 2 .1 μF ceramic disc capacitors

c. Video board

The last box contains bags of components for the video terminal interface. One unnumbered bag contains the circuit board. Check the others for completeness.

BAG #0: INTERGRATED CIRCUITS

check

( ) 1 SN7407N
( ) 2 SN7415ON
( ) 3 SN74367N or DM8097N
( ) 2 SN74393N
( ) 2 SN74LSOON
( ) 1 SN74LSO2N
( ) 1 SN74LS2ON
( ) 2 SN74LS74N
( ) 1 SN74LS123N
( ) 2 SN74LS132N
( ) 1 SN74LS138N
( ) 1 SN74LS139N
( ) 1 SN74LS153N
( ) 5 SN74LS157N
( ) 3 SN74LS161N
( ) 1 SN74LS273N
( ) 1 SN74S124N
( ) 1 SN74S412N or P8212
( ) 1 MCM6571A or MCM6574 or MCM6576
( ) 4 AM91L11APC D2111AL-4
( ) 1 DM8131N
( ) 1 N8274B

BAG #1: DISCRETE COMPONENTS

check

( ) 1 Capacitor-Silver Mica 22pf @ 150v CD15ED220J03
( ) 1 Capacitor-Silver Mica 39pf @ 150v CD15ED390K03
( ) 6 Capacitor Tantalum 10mf @ 25v T362B106M025AS(Kemet)
( ) 1 100pf ± 10% Ceramic Disc
( ) 1 Capacitor Ceramic .0047 @ 25v
~~( ) 1 Capacitor Ceramic 470pf~~
( ) 1 Regulator LM323K
( ) 1 MC78L12CP
( ) 2 Trimpot 10K ohm 72WR10K
( ) 1 Resistor 82ohm ¼w
( ) 1 Resistor 100 ohm ¼w
( ) 2 Resistor 220 ohm ¼w
( ) 1 Resistor 470 ohm ¼w
( ) 4 Resistor 1000 ohm ¼w
( ) 1 Resistor 3300 ohm ¼w 10%
( ) 2 Resistor 4700 ohm ¼w
( ) 1 Transistor 2N5449
( ) 1 DIODE

BAG #2: HARDWARE, ETC.

check

( ) 30 Capacitor Ceramic .1mf @ 16v UK16-104
( ) 1 Heat sink 6051
( ) 14 Resistor 2200 ohm ¼w
( ) 1 Bag Hardware

VIDEO HARDWARE (SHIPPED IN BAG #2)

check		
( )	2	6-32 x 3/8" pan head screws
( )	2	#6 Hex nut (small pattern)
( )	2	#6 Lockwasher
( )	1	12" #24 bare wire
( )	1	6" Teflon sleeving
( )	1	15 feet solder

BAG #3: MEMORY OPTION

check		
( )	4	Capacitor Ceramic .1mf @ 16v
( )	4	AM91L11APC

BAG #4: SOCKET SET

check		
(✓)	2	Male Receptacle 22-05-2021
(✓)	1	Female Connector 08-50-0114
(✓)	1	Plug Housing Molex 22-01-2021
(✓)	11	Socket-14 pin Low Profile
(✓)	18	Socket-16 pin Low Profile
(✓)	8	Socket-18 pin Low Profile
(✓)	1	Socket-20 pin Low Profile
(✓)	4	Socket-24 pin Low Profile
(✓)	1	14 pin sidewiping
(✓)	1	CTS20607 14 pin Dip Slide Switch
(✓)	1	Coaxial Cable, 1 Foot

BAG #5: POLY 88 ACCESSORIES

check		
( )	2	MALE PC RECEPTACLE 22-05-2021
( )	1	FEMALE CONNECTOR 08-50-0114
( )	1	HARDWARE FOR AMP 206584-1, 205817-1
( )	1	CONNECTOR AMP 206584-1
( )	1	REAR MTG PHONO PLUG
( )	1	RIBBON CABLE 3M 06/06/65-15
( )	1	PC BOARD-PARALLEL
( )	1	BAG HARDWARE
( )		COAXIAL CABLE 1 FOOT

SUPPLEMENTAL HARDWARE (SHIPPED IN BAG #5)

check		
( )	2	4.40 x 3/8" Pan Head Screws
( )	2	2.40 Hex nuts
( )	2	#4 Star Washers
( )	1	6.32 x 3/8" Pan Head Screws
( )	1	6.32 Hex nuts
( )	1	#6 Star Washers
( )	1	1" shrink tubing

2. Assemble cabinet, backplane, and power supply

The first step in building the POLY 88 is assembling the backplane, starting with the discrete electronic components (smallest through largest), then card guides, then sockets. The transformer is then assembled into the chassis, and the backplane mounted and connected.

a. Assemble backplane. Refer to figure A-1 to see where the components go on the board. When installing discrete components, solder on the back of the board and trim leads.

(✓) 1. Install standoffs for four 1-amp power diodes, with forks up. (for D3 through D6 -- see fig. A-1.) Clip off extra pin below board.
NOTE: The extra holes with diode symbol nearest the center are not used.

(✓) 2. Install 1A diodes (1N4003) onto standoffs (D3 through D6) oriented as indicated by the arrow on the board. The banded end of the diode points in the direction the arrow is pointing.

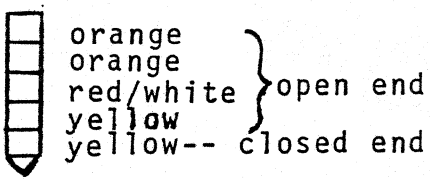
(✓) 3. Install both 6-amp power diodes in place (D1-D2). These two diodes alone provide full-wave rectification with the center-tapped transformer. (60S05)

(✓) 4. Install two 2,200-ohm resistors R1 and R2. (red-red-red)
(✓) 5. Install the 330-ohm ½ W resistor R3. (orange-orange-brown)
(✓) 6. Install one 100-ohm ¼ W resistor R4. (brn-blk-brn)
(✓) 7. Install the other 100-ohm ¼W resistor R5.
(✓) 8. Install the 1N4148 diode D7.
(✓) 9. Install the ceramic disc capacitor C4. (.1 μF)
(✓) 10. Install the 1,000-ohm resistor R6 at the other end of the board (brn-blk-red)
(✓) 11. Install the 470-ohm resistor R7. (ylw-viol-brn)
(✓) 12. Install the 2N5449 transistor Q1 oriented as shown.
(✓) 13. Install the 1,000 μF electrolytic capacitor C2 oriented with its positive end in the direction indicated on the board.

(✓) 14. Install the 2,000 μF electrolytic capacitor C1, oriented with its positive end in the direction indicated on the board.
(✓) 15. Using the screws supplied on the capacitors, attach the 17,000 μF electrolytic capacitor C3. (Noting the polarity)
(✓) 16. Attach plastic card guides to metal card-guide supports, using 6-32 screws and nuts. (Nuts on inside.)
(✓) 17. Mount card guides as shown. Use short 6-32 screws and six metal standoffs. These are protected from the circuit board by plastic insulators.
(✓) 18. Attach two 100-pin edge connectors (or up to five as desired) into connector areas J1 and J5 as shown. Making sure that the connector does not bow the backplane, solder all 100 pins on each connector. Be careful not make solder bridges.
(✓) 19. Solder male halves of Molex connectors into each end of board as shown on page 10.
(✓) 20. Install a wire jumper on front of board as shown. (R8)

The backplane is now complete.

b. Assemble chassis.
Do not solder until instructed to do so.
(✓) 1. Install 4 rubber feet to chassis undersides, using 4 #6-32 x 3/8 screws, nuts, and lockwashers.
(✓) 2. Install fuseholder on rear of chassis, with perpendicular tab pointing down.
(✓) 3. Tin the line cord wires and trim the exposed ends to about 3/8".
(✓) 4. Install through rear of chassis using the strain relief provided, allowing about 2 inches of the heavy outside insulation inside beyond the strain relief. Pliers or a strain relief tool will be necessary, due to the tight fit.
(✓) 5. Attach the black wire from the line cord to the end of the fuseholder and solder in place.
(✓) 6. Take the transformer and cut the secondary wires (yellow, orange, red, white) to 7 inches, then strip about 3/8" and tin.



(✓) 7. Attach and solder the 5 larger molex pins to secondary wires, making sure the one with the closed tip goes on one of the yellow wires, and the red and white wires are together on one pin. Use needle pliers to crimp pins and solder to insure good connections.

(✓) 8. Insert molex pins in the connector as shown above.

(✓) 9. Cut the blue and black primary wires down to 5 inches and the red and brown wires to 8½ inches, strip to about 3/8 inch, and tin.

(✓) 10. The remaining 2 wires (green, gray) must be kept from shorting to anything else. Cut one of these wires to about 3 inches and the other to 2 3/4 inches, place a 1 inch length of shrink tubing on the two wires so that ¼ inch extends past the end of the longer wire. Shrink the tubing by using a match; pinch the end of the warm tubing to seal the wire inside.
CAUTION: Do not burn the tubing by allowing the flame to touch it.

(✓) 11. Install rocker power switch in front of chassis with the 2 closer contacts at the top.

(✓) 12. Take the 3 20 inch lengths of wire, strip to about 3/8 inch and tin (both ends). Then twist the 3 wires together, leaving 1½ inch loose at each end.

(✓) 13. Attach and solder these 3 wires to the power switch from the bottom up. The order should be green-bottom, orange middle, and blue-top.

( ) 14. Take the 3 lug terminal strip and attach green wire from line cord to the grounded lug on terminal strip and the white wire to another lug. To make later connections to terminal strip lugs easier, it is helpful to attach the line cord wires to the lug rivets on the bakelite strip rather than on the ends of the lugs. If you do this, solder the line cord

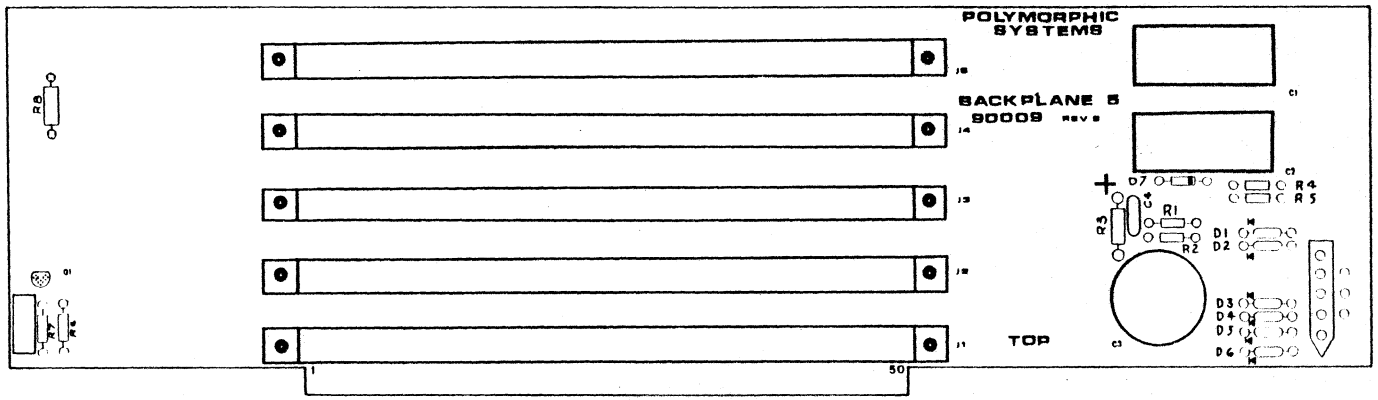

POLYMORPHIC
SYSTEMS
BACKPLANE 5
90009 Rev B
J5
J4
J3
J2
J1
TOP
1
50
R1
R2
R3
R4
R5
R6
D1
D2
D3
D4
D5
D6
D7
C1
C2
C3
Q1

FIGURE A1

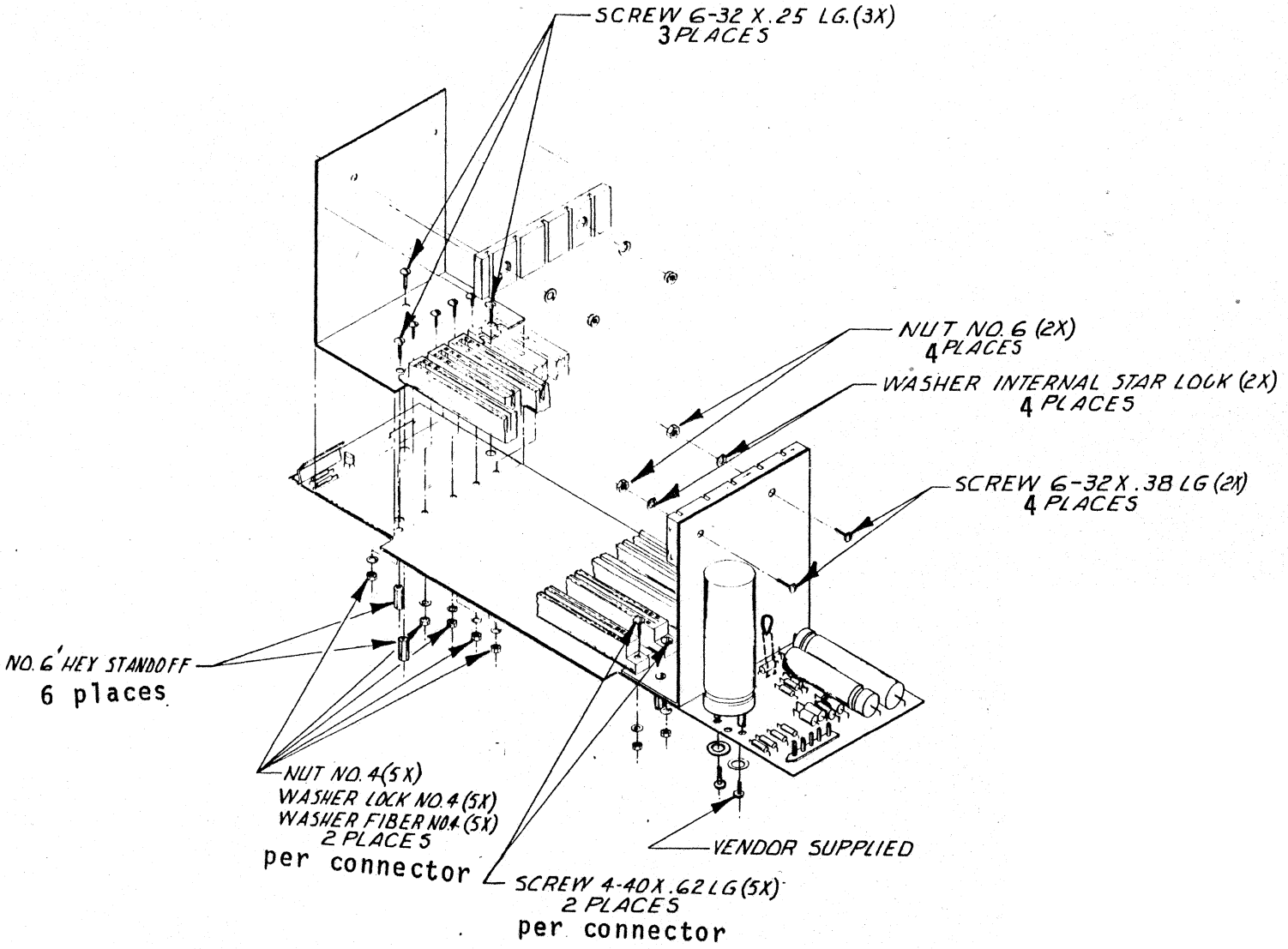

SCREW 6-32 X .25 LG. (3X)
3 PLACES
NUT NO. 6 (2X)
4 PLACES
WASHER INTERNAL STAR LOCK (2X)
4 PLACES
SCREW 6-32 X .38 LG (2X)
4 PLACES
NO. 6 HEX STANDOFF
6 places
NUT NO. 4 (5X)
WASHER LOCK NO. 4 (5X)
WASHER FIBER NO. 4 (5X)
2 PLACES
per connector
VENDOR SUPPLIED
SCREW 4-40 X .62 LG (5X)
2 PLACES
per connector

Fig. A-2

wires in place now. This terminal strip will be attached to the foot of the transformer as shown on the next page.

(✓) 15. Attach 1 of the .01 μF disc capacitors from the side lug of the fuseholder to the terminal strip lug with the green wire attached.

(✓) 16. Attach the blue wire from the power switch on the front of the chassis to the side lug on the fuseholder, and solder at this point.

(✓) 17. Attach the green wire from the power switch to the same terminal strip lug to which you already attached the white line cord wire.

(✓) 18. Attach and solder the remaining .01 μF capacitor between the lug used in step 17 and the grounded lug of the terminal strip and solder the lug with the two caps.

(✓) 19. Placing the transformer beside the chassis, but without yet installing it, attach its blue and black primary wires to the term lug with the white line cord wire and solder.

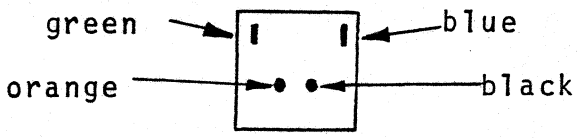
(✓) 20. Take the transformer and turn it so the secondary wires are on the same side as the terminal strip and attach it into place in the rear of chassis, being very careful not to pinch any wires under it. The terminal strip should be installed on one foot of the transformer above the fuseholder.

(✓) 21. Attach the orange wire from the power switch and remaining red and brown primary wires from the transformer to the remaining empty lug on the terminal strip and solder. These are the only connections to this lug.

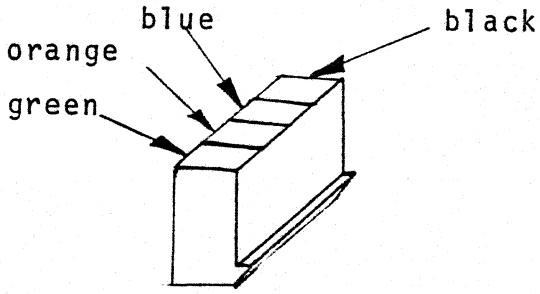
(✓) 22. Solder all connections to the terminal strip now.

(✓) 23. Take the 4½ inch long wires (orange, black, green, blue), strip and tin both ends to about 3/8 inch, and crimp the 4 smaller molex pins to one end. Solder again to insure good connections.

(✓) 24. Trim off about half of the two thin wire pins in the center of the reset button. Attach and solder the 4 wires to the button as shown:



(✓) 25. Insert molex pins into the small female molex connector as shown:

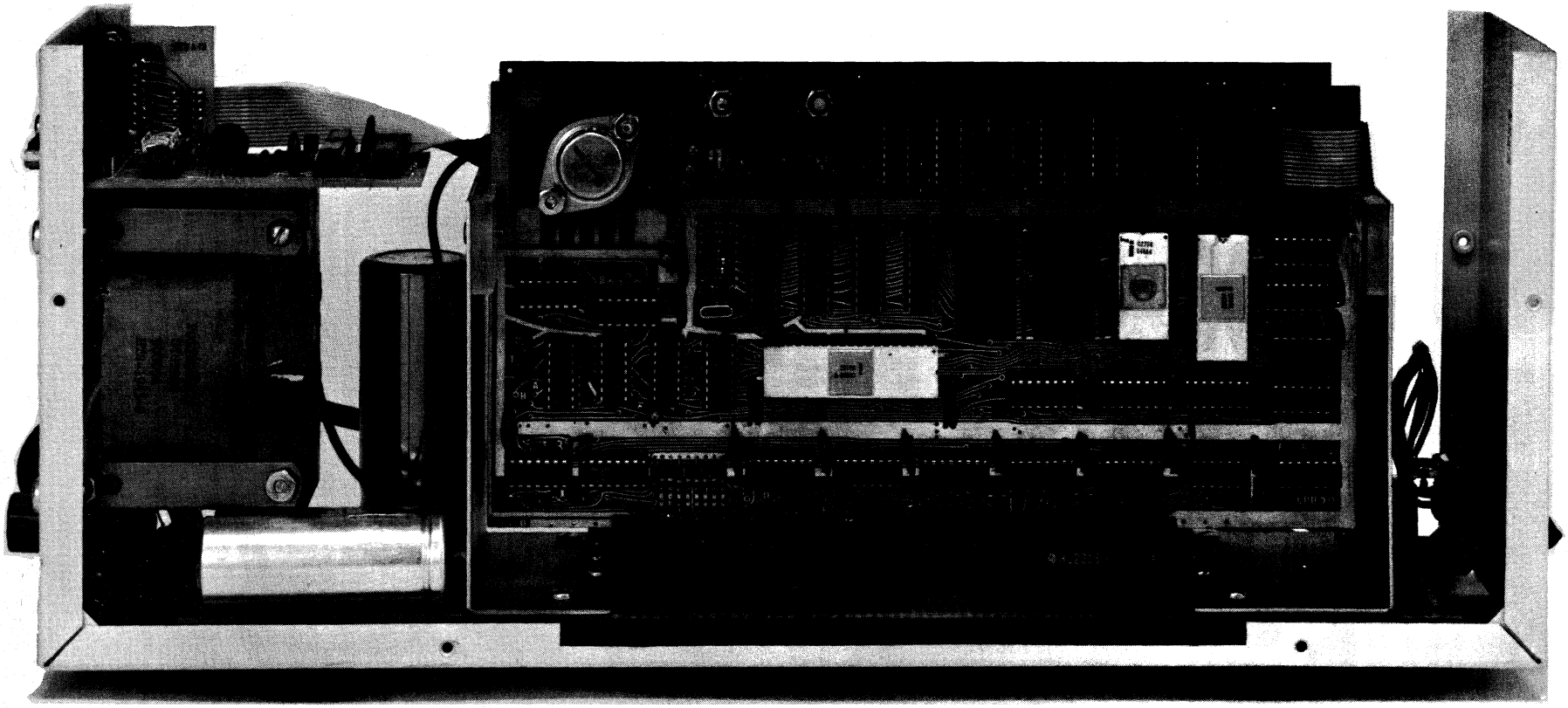


(✓) 26. Insert connector through square hole on front panel and draw the wires through. With the green and blue wires at the top, snap the switch firmly in place.

(✓) 27. Assemble backplane into chassis by sliding the end with the two horizontal filter capacitors under the transformer, align the hexagonal standoffs with the six holes in the bottom of the chassis. Fasten the backplane in place with six #6-32 screws, making sure not to pinch the wires running to the power switch.

(✓) 28. Connect the backplane to the transformer and the reset switch by mating the molex connector at each end of the backplane.

The cabinet, backplane, and power supply assembly is now complete.



c. Test backplane and power supply.

If you have a small voltemeter, you can now check the backplane and power supply. Plug in the chassis and "smoke test" it. If anything is obviously wrong, don't go any further till you've eliminated the problem.

Next, turn the cabinet so that the transformer is on your left. Along the edge of the backplane circuit board nearest you is a row of finger-like pads. These are the pads you would solder a connector to, in order to mate this chassis to another. They also make a convenient voltage check point. At each end of this row you will find a pad much wider than the others. The one on the right is ground; attach the ground lead of the voltmeter to this point, being careful not to include the adjacent pad. (The ground pad is available on both upper and lower surfaces of the board.)

CAUTION!

The pad on the left end of the board is next to a minus-voltage pad on the upper surface of the board and a plus-voltage pad on the lower surface. If the upper surface of the board is shorted to the lower, serious damage will result. Do not clip your volt-meter lead to this end of the board. Instead, probe carefully at the indicated pads.

The pad on the left end should read between +8 and +10 VDC. The pad just to its right on the upper surface of the board should have -18 to -22 VDC. The pad on the lower surface next to the large end pad should have +18 to +22 VDC.

3. Assemble Processor Board

The central processor circuit card consists of the Intel 8080A that provides all central processing, plus the devices that support the central processor: random-access and read-only memory, plus optional serial port if ordered.

Orient the board as shown in figure A-3.

a. Install components required for voltage regulation.

1. The following ICs are not dual in-line packages. Each of these ICs has a heat sink.

Check	IC#	Part #	Function
(✓)	32	7805 or LM309 or LM340K-5.0	5V regulator
(✓)	33	78M12	12V regulator
NOTE:	Install IC 34 with mica wafer and non-conductive screw.		
(✓)	34	79M05	-5V regulator
(✓)	44	79L12	-12V regulator*

*Include with Serial Option only

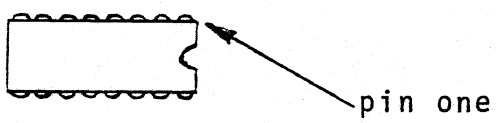
2. Install the following capacitors.

CHECK	CAP. #		TYPE
(✓)	20	10	μF tantalum
(✓)	21	0.1	μF ceramic disc
(✓)	32 through 35	10	μF tantalum
(✓)	36 and 37	0.1	μF ceramic disc
(✓)	38	10	μF tantalum

3. Now you can test voltage regulation. (✓) Check pin 28 of IC 14 (CPU) for 12V± 0.6 V. (✓) Check pin 20 for 5V ± 0.25 V. (✓) Check pin 11 for -5V ± 0.25 V. If proper voltages are not present, check the installed components and the solder points. Check continuity between IC 43 (78 M05) and ground (outer trace); if resistance does not exceed 1,000 ohms, check the insulation on this IC. The metal tab should be insulated by the nylon screw and mica washer.

b. Install integrated circuits. Begin by installing the integrated circuits themselves, OR the optional sockets if you bought them.

If you bought the socket option, install and solder in place all sockets by referring to figure A-3 and the list of componenets below. DO NOT install the integrated circuits at this time; install them after completing Step C below. Verify the location of each socket by checking the number of pins. Verify that the orientation is correct by noting the "pin one" location on the figure.



If you did not buy the socket option, install and solder into place all the integrated circuits by referring to the figure and list as above, verifying location and orientation as above.

	CHECK	IC#	TYPE	#PINS	FUNCTION
	( )	1	74LS13	14	Quad NOR gate
	( )	2	74148	16	Decoder
	( )	3 through 8	8197	16	Bus driver
	( )	9	7407	14	Hex buffer
	( )	10	74LS109	16	
	( )	11	74LS02	14	
	( )	12	74LS04	14	Hex inverter
	( )	13	8224	16	Clock generator
	( )	14	Socket	40	Socket for CPU
	( )	15 and 16	74LS257	~~14~~ 16	
	( )	17	74LS174	~~14~~ 16	
	( )	19	~~7425~~ 74LS08	14	
	( )	20	74LS132	16	
	( )	21 through 24	91L11	18	256X4 RAM
	( )	25 through 27	Sockets	24	Sockets for ROM
→ *	( )	28	Socket	28	Socket for USART
	( )	18	7425	14	
*	( )	29	MM 5307	~~16~~ 14	Baud rate generator
	( )	30	74LS174	16	
*	( )	31	74LS08	14	
	( )	35 and 36	74LS138	16	
	( )	37	74LS32	14	Quad NOR gate
	( )	38	74LS109	16	
	( )	39	74LS32	14	Quad NOR gate
	( )	40	74LS00	14	Quad NAND gate
	( )	41	74LS109	16	
→ *	( )	42 and 43	Sockets	14	Sockets for serial post

c. Install discrete components.
Install all resistors, starting at the lower left corner of the board.

✓* Included with Serial option only.

CHECK	#	TYPE
(✓)	1 through 11	2,200-ohm (red-red-red)
(✓)	12	4,700-ohm (ylw-viol-red)
(✓)	13 ~~through~~ ~~17~~ +22 +23	2,200-ohm
(✓)	14 +21	1,000-ohm (brn-blk-red)
(✓)	15 Thru 17	2,200-ohm
(✓)	~~20~~ 18	1,000-ohm
(✓)	19 through 20	2,200-ohm
(✓)	24 through 31	10,000-ohm (brn-blk-orng)
(✓)	32 through 36	2,200-ohm

Install all capacitors, starting at the lower left corner.

CHECK	#	TYPE
(✓)	1 through 7	0.1 µF ceramic disc
(✓)	8	470 pF ceramic disc
(✓)	9 through 13	0.1 µF ceramic disc
(✓)	14	33 µF tantalum
(✓)	15 through 18	0.1 µF ceramic disc
(✓)	19	39 pF ceramic disc
(✓)	22 through 31	0.1 µF ceramic disc C25, C30*
(✓)	39 through 42	0.1 µF ceramic disc
(✓)	43	10 pF tantalum*

Install all diodes. The end of the diode with the colored band points in the same direction as the arrow etched on the board.

CHECK	#	TYPE
(✓)	1 and 2	1N4148
(✓)	3	1N4148*

If you bought the socket option, you can now check voltage regulation without endangering your chips. Install the board into any chassis edge connector (it will not go in wrong), then turn on the power and use a small voltmeter to verify +5V, +12V, -5V and -12V

(✓)	X1	Install 16.5888 MHz crystal

* Included with Serial option only.

Install jumper using telfon tubing from point labeled "F" near pin 21 on the edge connector to the corresponding point "F" below IC 8.

If the power supply checks out, install all ICs now. If power supply is not correct, fix it (check for solder bridges, mis-oriented components, etc.) before installing chips.

The CPU board is now complete.

4. Assemble Video Board

Install DIP sockets:

Orient the PC board so that the gold plated contact of the bus connector is facing you and the large foil area is at the upper right. This is the TOP of the board.

According to assembly diagram, check-off list, and designation on board, install sockets on top of the PC board.

Install IC sockets

Check	Location	Component
(✓)	IC 1,2	16 pin sockets
(✓)	IC 3, 4, 5	14 pin sockets
(✓)	IC 6	16 pin socket
(✓)	IC 7	14 pin socket
(✓)	IC 8, 9, 10, 11, 12, 13	16 pin sockets
(✓)	IC 14, 15, 16	14 pin sockets
(✓)	IC 17, 18, 19, 20	16 pin sockets
(✓)	IC 21 through 28	18 pin sockets
(✓)	IC-29	16 " "
(✓)	IC 30, 31, 32	14 pin sockets
(✓)	IC 33, 34, 35, 36	16 pin sockets
(✓)	IC 37, 38, 39	24 pin sockets
(✓)	IC 40	20 pin sockets
(✓)	IC 41	24 pin sockets
(✓)	IC 42	14 pin socket
(✓)	SWITCH	DIP Switch
(✓)	J 1	14 pin sidewipe socket (keyboard)

Install resistors

Check	Number	Description	Color
(✓)	R1	470 ohm	YEL-Vio-~~Brn~~ Brn
(✓)	R2 - R10	2200 ohm	red-red-red
(✓)	R11	1000 ohm	brown-black-red
(✓)	R12	2200 ohm	red-red-red
(✓)	R13	1000 ohm	brown-black-red
→ ( )	R14	customer provided option for keyboard (see page 28)	
(✓)	R15	2200 ohm	red-red-red
(✓)	R16	4700 ohm	yellow-violet-red
(✓)	R17	2200 ohm	~~brown-black-red~~ Red-Red-Red
(✓)	R18	4700 ohm	yellow-violet-red
(✓)	R19	100 ohm	brown-black-brown
(✓)	R20	220 ohm	red-red-brown
(✓)	R21	220 ohm	red-red-brown
(✓)	R22	82 ohm	grey-red-black
(✓)	R23	2200 ohm	red-red-red
(✓)	R24, ~~25~~, 26	1000 ohm	brown-black-red
(✓)	R25	3300 Ω	ORANGE-ORANGE-Red

Install diodes: BEWARE OF POLARITY

Check	Number	Description
(✓)	D1	1N5225
→ ( )	D2	vacant (customer provided keyboard regulator) For Neg KBd sply

Install transistor Q-1 2N5449 flat side toward top of board

Step completed.(✓)

Install capacitors

Check	Number	Description
(✓)	C1,2	0.1 $_{u}$F Ceramic Disc Cap
(✓)	C3	100 pF ceramic disc
(✓)	C4 through C23	0.1 $_{u}$F ceramic disc

Check	Number	Description
(✓)	C24	10_uF 25V tantalum (note polarity)
(✓)	C25, 26	0.1_uF ceramic disc
(✓)	C27	10_uF tantalum
( )	C28 option, customer provided	0.1_uF ceramic disc (suggested)
( )	C29 option, customer provided	10_uF 25V tantalum (suggested)
(✓)	C30	0.1_uF ceramic disc
(✓)	C31	10_uF tantalum
(✓)	C32	0.1_uF ceramic disc
(✓)	C33	10_uF tantalum
(✓)	C34	39pf
(✓)	C35	22pf
(✓)	C36	$.0047_u$F ceramic disc
(✓)	C37	0.1_uF ceramic disc
(✓)	C38	10_uF tantalum - Note: positive toward bus connector
(✓)	C39,40,41	0.1_uF ceramic disc
(✓)	C42	10_uF tantalum
(✓)	C43,44,45,46	0.1_uF ceramic disc

Install potentiometers:

Install 10K ohm pots at R27 and R28. Screw adjustments must be toward outside of board to be of practical value. Step completed (✓).

Install Male output connector at Video out location.
Note that the unit closely matches the diagram printed on the Video board.
Step completed (✓).

Install voltage regulators

At IC 43 install 12V regulator 78L12 (✓) check.

At IC 44 install LM323 and heat sink assembly. Pleace the heat sink over the large foil area so that all four holes line up. Then place regulator

over the heat sink. Secure with 6-32 hardware. Solder underside after securing heat sink. Check (✓).

4.a Smoke Test

At this point your VTI board is completed except for installation of IC's.

Before installing the IC's the board should be "smoke tested". Connect your VTI to appropriate power supply and observe carefully. Any unusual odor or sign of smoke indicates an error that must be remedied before you proceed.

4.b Install integrated circuits

Check			PINS	FUNCTION
(✓)	IC 1	74LS161	16	Binary counter
(✓)	IC 2	74LS161	16	Binary counter
(✓)	IC 3	74LS02	14	Quad 2-input NOR gate
(✓)	IC 4	74LS74	14	Dual D flip-flop
(✓)	IC 5	74LS132	14	Quad 2-input NAND gate
(✓)	IC 6	DM8131	16	6 input comparator
(✓)	IC 7	74LS00	14	Quad 2-input NAND gate
(✓)	IC 8	74LS153	16	Dual 4-input multiplexor
(✓)	IC 9	8097	16	Hex tri-state buffer
(✓)	IC10	8097	16	Hex tri-state buffer
(✓)	IC11	8097	16	Hex tri-state buffer
(✓)	IC12	74LS138	16	3 to 8 decoder
(✓)	IC13	74LS161	16	Binary counter
(✓)	IC14	74LS20	14	Dual 4-input NAND gate
(✓)	IC15	74393	14	Dual 4 bit binary counter
74393 (✓)	IC16	(74383)?	14	Dual 4 bit binary counter
(✓)	IC17	74LS157	16	Quad 2-input multiplexor
(✓)	IC18	74LS157	16	Quad 2-input multiplexor
(✓)	IC19	74LS157	16	Quad 2-input multiplexor
(✓)	IC20	74LS139	16	Dual 2 to 4 line decoder

Check			PINS	FUNCTION
( )	IC21	91L11	18	256X4 bit static memory
( )	IC22	91L11	18	256X4 bit static memory
( )	IC23	91L11 memory option	18	256X4 bit static memory
( )	IC24	91L11 memory option	18	256X4 bit static memory
( )	IC25	91L11 memory option	18	256X4 bit static memory
( )	IC26	91L11 memory option	18	256X4 bit static memory
( )	IC27	91L11	18	256X4 bit static memory
( )	IC28	91L11	18	256X4 bit static memory
( )	IC29	74S124	16	Dual gated voltage contrid osc.
( )	IC30	74LS00	14	Quad 2-input NAND gate
( )	IC31	7407	14	Hex open-collector buffer
( )	IC32	74LS74	14	Dual D flip-flop
( )	IC33	74LS157	16	Quad 2-input miltiplexor
( )	IC34	74123	16	monostable multivibrator
( )	IC35	N8274	16	Ten bit shift register
( )	IC36	74LS157	16	Quad 2-input miltiplexor
( )	IC37	MCM6571A	24	Character generator
( )	IC38	74150	24	16-input multiplexor
( )	IC39	74150	24	16-input multiplexor
( )	IC40	74273*	20	8 bit register
( )	IC41	74S412 or 8212	24	8 bit latch
( )	IC42	74LS132	14	Quad 2-input NAND gate

4. c Option Selection

Though the VTI is an integral part of the POLY 88 system, it is compatble with other systems. We have therefore, included a number of additional jumper option areas which do not apply to POLY 88 owners.

These are Jumper areas 1, 2, 3, 5 and 6.

*The polarity may be ambiguous; the oblong groove indicates the device orientation.

JMP1 changes the divide ratio from the system clock to produce scan rates which are more appropriate when using different system clock rates.

JMP2 selects the vectored interrupt priority for the keyboard input. The VTI is already wired for interrupt priority 2.

JMP3 and JMP6 are similar to JMP1 in that they adjust the scan rates when used with different clocks.

JMP5 allows use of an on-board clock.

4.d Select Character line length option.

Your board is configured for a 64 character line. If you require the 32 character line cut the trace on the back of the board between the middle pad of JMP4 and the pad designated 64 at JMP4. If you do not require the 32 character line, do nothing.

4.e Address location:

The VTI interacts through the S-100 bus as a block of memory and input port for keyboard. The memory block, (½ or 1 K bytes, depending on option) can be located at any address from Ø through 63 K in 1 K increments. (Software writter for this product will usually locate it at hexadecimal address F800).

Location is determined by comparing the six most significant bits of the memory address with six jumper selected bits. Reducing circuit complexity, the memory block also determines the address of the input port. The six most

significant bits of the input port address must match the six switch or jumper selected bits. The two least significant bits are not compared for input address therefore, their state is arbitrary.

The address selection switch area is located at the lower left hand corner of the board near IC6.

Each of the six most significant bits of the address is resistor tied to + 5V, so that they are normally in binary state 1. Any or all of them may be grounded to cause a situation of binary state Ø. A DIP switch is provided for selectable jumpering. Typically, the address line on the right is grounded to the pads at left, producing a logical zero. The five switches nearest bus connector should be in the off position. The remaining two switches should be on, setting the board at F8ØØH. 63488D

4.3 Interface TV monitor or TV receiver:

At this point, your unit should operate if connected via coaxial cable to either video monitor or slightly modified receiver. (For the Hitachi line, an inexpensive TV receiver modification kit is available through PolyMorphic Systems).

If the prompt character does not appear on "power up", horizontal frequency adjustments, found on the back of the video unit, may be required.

Because of rigid FCC regulations, the circuit has been designed for direct connection to the video input circuit of the video amplifier, which is located between the last video IF stage and the video output circuit.

When the circuit is broken at video amplifier input, a DC bias circuit for the stage will probably be necessary, since in most cases it is supplied from the video IF amplifier. The optimum interface circuit will vary, but frequently a capacitive coupling to a resistive bias circuit is adequate.

The coupling capacitor is typically a 1-5$_u$F tantalum, oriented with the positive side connected to the video input amplifier.

IMPORTANT: Check to see that the chassis of your TV is isolated by a transformer from the 110 VAC line. If the chassis is not so isolated, but rather a polarized plug has been used on the line cord, FATAL INJURY COULD RESULT from possible electrical shock. If you must use this type of set, either isolate it with a transformer or isolate the video signal with an opto-isolator between the video terminal interface and the video input connection to the TV set. Under no circumstances should the polarized plug be trusted to maintain the isolation from the line voltage.

4.4 Connect keyboard

At the upper right hand corner of the video terminal interface board is the keyboard input port. This port provides a latched 8 bit parallel input capability which completely interfaces with many ASCII keyboards. Keyboards usually indicate a keystrike to the computer via a strobe line, in addition to the eight parallel input lines. The signal on this line changes state -- from high to low or from low to high -- to indicate a keystrike. Hookup varies according to whether the strobe on your keyboard is "positive going" (rising in voltage to indicate keystrike) or "negative going" (dropping to indicate keystrike).

4.4.1 Connector configuration

The parallel input from the keyboard is designed to come in over a ribbon cable terminated by a DIP MALE CONNECTOR. This plugs into the 14 pin DIP socket at the upper right hand corner of the board. The 8 parallel input lines are connected to pins 1 through 8 of this socket, (J-1) with 1 being the least significant bit. Pin 9 carries the "positive going" or "negative going," strobe. Pins 10, 11, and 12 are grounded.

Pin 13 is the output from the optional (*) negative voltage regulator. Pin 14 carries +5 volts as the primary supply for most keyboards. JMP8 allows 8 volts unregulated power at Pin 14 if desired. Be sure to cut the trace connecting 5 volts if you require this option. A jumper is inserted from the middle pad of JMP8 to the pad nearest the regulator within the area designated JMP8.

WARNING: FAILURE TO CUT THE TRACE SUPPLYING 5 VOLTS WHILE ATTEMPTING TO JUMPER IN 8 VOLTS WILL DESTROY EVERY COMPONENT ON THE BOARD AND VOID THE WARRANTY!

4.4.2 Keypress strobe

When the processor accesses the video terminal interface with an input instruction, the state of the keyboard input latch is transferred to the accumulator. Proper use of the keyboard requires that the processor must establish two conditions before using the input data. It must indicate that

1) a key has been pressed, and

2) this particular key depression has not been previously serviced.

These functions are accomplished by making the keypress strobe information available to the processor.

The keypress strobe line is an additional keyboard output line parallel with the data lines. This line signals each depression by a pulse. This test-function informs the processor that the necessary input conditions are met. The pulse:

1) interrupts the processor by setting an interrupt service latch contained on the input buffer,

(*) Used when the keyboard requires a negative supply. The user should select and obtain the components suited to his keyboard.

or 2) the interrupt request latch is available on data bit Ø of the status port; the keyboard strobe is available on data bit 7.

Attaching the strobe line of your keyboard to a VOM determine whether it is normally low (below .8V) or normally high (above 2.5V). If low, the jumper is already properly configured.

If high, cut the minus trace from center pad of JMP-7 and jumper from center pad to + labled pad.

i. optional voltage regulator

Provision has been made for the optional negative voltage regulator required by a number of keyboards. The pads and traces for this voltage supply are located adjacent to the keyboard input socket, just above the IC23. The supply regulates the -16V line by means of a resistor and zener diode stabilized by two capacitors. The four components are R14, C29, C28 and D2. The choice of resistor and zener values depends on the voltage and current requirements of the keyboard.

5. System checkout.

Install all boards and "smoke test" them. If something is obviously wrong, solve it before proceeding.

To test the POLY 88 system, you will want to hook it up to the video monitor.

In addition to a video monitor, you will need a simple logic probe with pulse detector. If you do not have one, buy one or build one using the circuit enclosed. If you cannot use a logic probe, do not attempt detailed checkout.

You will also need the VTVM or VOM you used earlier. A magnifying glass will also be helpful.

If the system does not operate properly, first eliminate the most common problems:

( ) 1. Check all components on all boards for proper location and orientation. In particular, check the tantalum capacitor orientation carefully.

( ) 2. Check all boards to make sure there are no solder bridges.

( ) 3. Check that all jumpers are in place, and that they are correct for either the 32 or 64 character option, whichever you ordered.

( ) 4. Check all boards to make sure tha all IC pins are correctly inserted -- not folded under or broken off, etc.

( ) 5. Check the jumpers or DIP switch on the video board for proper address selection.

If these problems are eliminated and the system still does not run properly, check the CPU board, using the logic probe pulse detector, to ensure that the clock signal from IC13 is available on pin 49 of the edge connector.*

If there is no clock signal, check for solder bridges and incorrect component placement and orientation on the CPU board. Check IC13 and IC8 (bus driver, 8197) using the list of chip pinouts at the end of this volume. Pins 10 and 11 of IC12 should have +2 to +8V. Use a VTVM for this test if your logic probe will not accept these levels. A malfunction at this point will usually produce a constant 0V or 10V. If you now have a clock pulse on pin 49 of IC13, and you still have system malfunctions, proceed to Video Board checkout, immediately below. If you still do not have a clock pulse, go directly to CPU Board checkout.

a. Video Board Checkout

If you have a clock signal, hook up the video monitor and power up. You should get a clear screen with the cursor in upper left hand corner.

The video board consists in essence of three areas: Sync, Data Bus, and Character Generation-Video.

If you have a coherent, stable, but useless display, the problem is most likely in Data Bus.

* Pin 49 is the second pin from the right on the top of the board (49th from left).

If you have no display, the problem is most likely in Character Generation-Video.

One problem that affects all three areas is the output buffer, so begin by checking pinouts on:

( ) IC 31 (output buffer, 7407).

Next, perform the relevant steps below.

Data Bus

( ) Check all RAMs, ICs 21 through 28 (91L11 or 2111).

( ) Check all RAM pins for proper insertion

( ) Check for solder bridges on RAMs and in the bus driver area.

Character Generation-Video

( ) Check the dot clock chip, IC 29(74S124).
If you have a display, you can check IC29 by decreasing the display width by adjusting potentiometer R27. If the display changes, the dot clock chip is probably defective.

( ) Check the shift register, IC 35 (8274).

If you have done all the above, and still have system malfunctions, continue with detailed checkout below. If a synchronized array of characters cannot be achieved by adjustments of sync controls on the CRT (or TV), check first for the more obvious and frequently encountered problems. Most typical will be such items as:

1. Loose connections to system or to display.
2. Improper interfacing to display's video input (biasing, etc.).
3. Omission or improper installation of components on the board (reversed diode or chip orientation).
4. Soldering problems of unsoldered contact or solder-bridge shorts.
5. Omitted or wrongly selected jumper patterns (line length, address selection, etc.).

The discussion below follows one of many possible logically sequenced procedures to localize problems and is written for those without access to an oscilloscope.

Start with a good visual inspection of connections and of the

board itself. Progress through checks on the power supply busses and video output to electrical test patterns of the signals on the board. In using the electrical test patterns, work from end results backwards towards those parts of the circuit which contribute to the end results. For example: if the proper raster sync signals are doing their job, all further measurements concerning these circuits involved can be omitted in favor of checking contributions to character presentation.

a.1 Power mains

a.1.1. If visual inspection looks good, see if the power mains are proper. There should be +5.0 ± 0.2 VDC on the VCC bus. Convenient clip lead points include:

A. Ground reference: the metallized board area under the voltage regulator heat sink at the top right is a good one. The board has been designed with a blank area on the reverse side so that the other jaw of a clip cannot short any signals there. (Watch out for this at other locations, especially along the top of the board.)

B. 5 volt bus: the bottom lead of resistor R12. A voltage below tolerance here may indicate either a heavy current load from a misconnection or a reverse-oriented IC or that your power main feeding the board has less than 7 volts available.

Zero volts at this point probably indicates missing power to the board (a cold regulator) or a dead short on the board in which case the regulator will be very hot to touch. (Don't panic. You will be amazed at its recuperative capability when the short is cleared.)

C. VDD bus for the character generating ROM IC36(6571-4). Measure +12V± 10% at the junction of R20/C29.

D. VBB bus for IC37: Measure -3V ± 10% at the left hand lead of D1. (This is the only negative voltage.)

a.1.2 If power bus shorts are suspected, ohmmeter verification involves considerations of the polarity of the test leads. The

board will not suffer from checks where the ohmmeter leads apply the polarity expected from the power supply and an open circuit voltage not exceeding the power supply value. The non-linearity of the load prevents us from predicting what an unknown ohmmeter will read on a normal board, but readings below an ohm mean that you should look for a short or an inverted IC. Reverse polarity from ohmmeter leads can be damaging unless the current is limited to low values. Most series-connected 50 micro-amp movement VOM's are safe when only the 1.5 volt battery is used on the scale selected.

a.2 Signal tracing

Unsolder the right end of the 100 ohm R1 (junction with pins 2, 4, 6, of IC31---- 7407) and attach a clip lead to the free end of the resistor for use as a scope probe. (Keeping a wire in the hole for the right end of R18 makes an easy way to remake the "normal" connection with the clip lead.)

DC voltages would normally read 1.6 V at this junction, but, when open, the clip lead will read about 4.5 and the IC31(7407) pins less than 0.1 V. This produces DC levels at the 2N5449 emitter of about 2V normally (average of normal waveform) and near 4V with an open test lead. 27% of these values should be found on the cable to the CRT. (If you have D.C. coupled into your CRT video, check that your design is proper for these values.)

Those users owning oscilloscopes probably have sufficient technical background to interpret the following discussion into equivalent scope presentations. This discussion assumes that the only signal tracing display available is the TV or CRT intended for computer display use. Therefore, the first checks are that the output stage is functioning and that its responses are visible on the CRT. If NOGO on these, check your cable and CRT. input arrangement.

a.2.1 video interface

Grounding the probe lead should pull the output emitter down to around a volt, and opening it should give a rise to around 4v. This transition should couple through the AC coupling to your CRT and be apparent as momentary brightening as the lead opens.

a.2.2 localizing on the video path

If logic levels applied to the clip lead are modulating the display brightness, but you are having to troubleshoot, let us consider what is missing. If, in the "normal" connection (i.e: lead clipped to where R19 should be soldered), there is an array of bright and dark spots on the display, chances are that video is being generated and that you will be chasing sync or blanking troubles. With only video coming through, most CRTs will at least partially sync on the video itself, and patient tinkering with the sync controls on the display and the two pots on the video board should give at least some torn-up version of what is trying to be a display. If you have sophisticated your power-up sequence to program a blank display, either alter the sequence until troubles are cured or remove programming to the board. Random states in the board RAM at power-up will produce some interpretable static pattern. But maintain the system clock connection. Horizontal sync is derived from that clock. (The board is testable with nothing more than proper power supplies and a clock for inputs.)

No video pattern? Let us see if it is shifting out of the register IC35-6(8274) (pin 6 of IC35). Got it? Then the path through IC31 is not passing it. Check for it at the input pin 9 and output pin 8 of IC31. Following the path should reveal a gap in signal passage that is correctable. This is the concept of signal tracing that will be assumed throughout the remaining discussion.

No video shifting out of IC35-6? Well, is there data on the

input pins to be loaded for shifting - or a load signal to load it - or a dot clocking to shift it out?

First the dot clock on IC35-9(8274): This should show as a raster full of tiny white dots. Depending on the setting of the "width" pot, there should be from 100 or so to almost 900 on each raster sweep, but several factors influence this. Sync and blanking, if they are working, keep many dots out of the visible area. Also, the bankwidth of this setup may not permit you to discern dots at the higher frequency settings of the dot clock. Best to view this at the minimum frequency (ccw) setting of the "width" pot (pot at top left). Do not bother counting dots. Their presence is all that is necessary to show register shift clocking input. Since this signal is negative true, a brighter presentation may be found at the inverted form on IC30-8(74LS00). Absence of sync should not prevent this display from being recognizable.

EOC (end-of-character) loading signals on IC35-7 should show as dark (negative true) vertical bars every tenth dot (except for a portion of the screen where horizontal blanking normally disables the dot clock). Their presence proves the dot clock (and dot counter) whether we check IC35-9(8274) or not. The number of bars visible is variable by the dot clock frequency ("width" pot) and by the "pos" pot control of sweep blanking. Although the blanking path is broken by lifting R19, the composite sync path is not. Therefore, if a strong sync is at work, some of the display, such as the area unbroken by vertical bars, may be sync'd into times not visible on the screen. This point about sync must be borne in mind as you check many of the waveforms - particularly in the sync path itself.

Assuming that shift (dot) clocking and its subcount, EOC load clocking, are available, is there video data on the input pins to be loaded? Each of pins 1 through 5 and 11 through 14 should show a screen pattern of white and dark states as wide as the

distance between the vertical bars seen on pins carrying the EOC or shift loading pulses. So too should input and output pins of the MUX's IC33 and IC36(74LS157). Also the outputs ROM IC37 (6571) and the graphics generators IC38 and IC39(74150).

The patterns associated with outputs from IC38 and IC39(74150) have a right to change every 5 sweeps. At the IC39(74273) inputs to the display generators IC37, 38, & 39, (6571) however, the sweep patterns should not change more frequently than every fifteenth sweep. These last patterns show what the memory is requesting for each character position of ten dots by fifteen sweeps. Counting these dimensions is generally not necessary. Merely noting that the fineness of detail is less at the input to generators than at the output is usually sufficient for trouble locallizing. Subcounting is discussed under 3.2.3 and 3.2.5.

The screen pattern for any significant bit input to the generators should be traceable back through corresponding pins of the sampling latch IC40(74273) to the same significant bit of the internal data bus. But remember, the nth character in memory is held in the latch until an EOC pulse strobes the latch and increments the memory address. If sync and clocking are at work to keep the display pattern straightened up, any lack of correspondence of the patterns up the path can be discerned. Without sync, it may take both a photographic memory and a lot of luck -- but the chances are that you would not be needing that level of detailed trouble-shooting without sync, anyway.

In like fashion, grounding pin one of IC33(7LS157) forces MUX's IC33 and IC36(74157) to select only graphic symbols from IC38 and IC39(74150). This change is most apparent with a sync'd display, but some shift should usually be discernible in the pattern for any shift register input pin. The degree of change will depend on how frequently the MSB is a one in the RAM. Correspondingly, the display probe on IC33-1(74157) will show

which memory locations contain graphics or non-graphics characters. An MSB in memory is inverted in the latch to select graphics.

a.2.3 localizing on the EOC (end of character) path

If you had dot clock input to shift register IC35-9(8274) but no stobe (IC35-7) to load the register, you will want to check back to where the EOC is generated by counting every tenth dot in IC14. In fact, failure of IC30(74LS00) or other problems can permit it to count by other than ten, with some weird results in displays. Clock dots are discernible at the input IC13-2. Slowing the dot clock (CCW on the "width" pot) makes these countable by eye. A piece of paper on the screen or a millimeter scale may help. Sync helps here but should not be necessary to array the pattern of dots into vertical bars. IC13-14(74161) has half as many vertical bars but of double width. Pin 13 has narrow vertical white bars equal to twice the width of the bars on pin 14. The total pattern of pin 13 is repetitions of black, white, black, white, white vertical bars. The last two whites show as a double width white as the carry preloads a 6 into this 4 bit binary counter. This preload makes it produce a carry every tenth dot. If pin 13 looks right, chances are that all the rest is okay.

The tenth dot carry on IC13-15 is the EOC (end of character) signal. It should appear at the input to the symbol counter IC16-13. An inverse (negative true) of this pattern should be found as loading signals n latch IC40-11(74273) and shift register IC35-9. Of course, if there is no dot clock, none of this paragraph is working properly. On the other hand, presence of dots anywhere does not leave much room for problems in the dot clock.

a.2.4 localizing on the dot clock path

If either the shift register or the dot counter is getting dots, you are in for some detail checks of solder bridges to ground, a single NAND gate in IC30(74LS00), or some such, because the

clock is present at the other end of these places. If neither is present (and of course no EOC signals), then look for dots at the clock IC29-7(74S124). Using a voltmeter, check its "width" pot for the ability to vary IC29-2 from zero to 5 volts. Check also for the enabling portion of the horizontal blanking signal on IC29-6. This may be hard to see as a broad vertical bar in the presence of strong horizontal sync, but if desyncing gives you a torn version of it, it is probably okay. A voltmeter reading on IC29-6 of 5 VDC would be a continuous disable signal. Under proper conditions, the average of the horizontal blanking waveform reads typically 0.9 to 2.3 VDC on a meter at IC29-6. The value is under control of the "pos" pot which varies the time delay (and thus the average DC value) of the blanking monostable.

a.2.5 localizing on the horizontal blanking path

Under the most ideal conditions of sync and blanking, events occurring during flyback, retrace, or blanking should not be visible. Note that opening R19 does not open the composite sync path at IC31-10(7407). Therefore, sync, if operating, will reach the CRT sync circuits - regardless of what is done with the probe lead. Remember, even without sync working, most CRT's or TV;s will find in many of the test signals something repetitious enough to sync on. There is usually a way to view sync-hidden signals by misadjusting the horizontal hold control of the CRT to force a "tear" in the picture. Then if the sweep rate is calibrated in time units, the signal can be measured in the torn portion. An example of this is horizontal blanking. Forcing a torn but stable pattern reveals a dark space in each sweep when looking at IC29-6 (74S124). Varying the "pos" pot changes the width of the space.

Typical values from stop to stop on the pot are about 10 or 20 microseconds (see section 3.3.1 on time calibration) but, if you can change it, it is working. Perhaps easier to see is its

inverse - a logic high on IC34-5(74123). For this, you should not have to force the tear. Horizontal blanking that is high logic will appear as a bright vertical bar at one or both sides depending on where the CRT is syncing. For most IC's, if Q is working, $\overline{Q}$ probably is also. Take the easiest way down the locallizing path first and back up to the harder ones only when necessary.

No horizontal blanking? How about the horizontal sync which triggers the IC34 monostable multi-vibrator to stretch the sync into a wider blanking? The carry out of counter IC1-15(74161) should have its inverse on IC34-9(74123). This is a 4½ microsecond pulse every 58½ microseconds.

Actual horizontal sync is the same width, but 4½ microseconds later, and can be seen on IC3-13(74LS02). Its inverse is on IC3-1 but is also mixed with vertical sync. Observation of a once-per-sweep, narrow vertical bar is probably sufficient to eliminate further details up this path, but if things are not clearing up, you may want to calibrate time as in a.3.1.

If these are NOGO, is the system clock on edge pin 49 and is it reaching IC2-1(74161)?

You can use your piece of paper or plastic millimeter scale to ratio the distance between leading edges of the bars. However, if the vertical bar pattern on IC2-14 is repetitions of black, white, black, white, black, white, black, white, white, then the binary 7 is apparently preloading on every carry and division is probably okay. (Compare this with the discussion of the dot counter in a.2.3.)

Counting bars will only tell you how many of the 58½ microseconds

per sweep are visible on your CRT and usually does not contribute to trouble analysis.

IC2-2 has an inverted form of IC1-15 showing a dark bar every 4½ microseconds, but division by 13 is difficult to ratio unless you have a rare CRT that has a horizontal width control that permits shrinking the picture sufficiently to see both ends of the sweep. But then - if any of IC2-11(74LS138), IC2-13(74161), IC2-15, or IC3-13(74LS138) have an observable once-per-sweep bar, horizontal sync seems to be doing its job.

a.2.6 sweep and symbol related counter patterns:

Verification of sweep counter test patterns is difficult in the absence of horizontal sync. Since the sweep counter is counting the carries from the same counter that generates horizontal sync, the presence of one signal without the other would indicate that the integrity of any missing path should be reestablished before proceeding. The clocking input IC15-1 (74393) is a once-per-sweep pulse which may not be in the visible portion of the sweep unless a tear is forced in the horizontal hold. All other patterns are stretched by the sweep into horizontal bar patterns with the exception of the reset IC15-2. The reset is like the clock on IC15-1 except a) it occurs every 15th sweep; b) it is a 4½ microsecond darkening instead of a brightening; and c) it occurs 4½ microseconds later (to the right) on the screen. It is therefore probably visible only under torn conditions.

Correct patterns for pins 3, 4, 5, and 6 of IC15 can be inferred from the timing diagrams. A quick check of proper operations and counting by fifteen can be made on pin 4. The pattern for IC16-3 is: every other pair of sweeps is white (2nd, 4th, and 6th pairs) followed by the single white 15th sweep during which the counter is reset. Symbol lines are perhaps better defined by the double black sweeps visible on IC15-13. These occur

because of the adjacency of the first and last sweeps, which are both dark, while all even numbered sweeps including those during retrace are bright.

As further subcounting is done in the line counter, IC15-11 shows every other line (group of 15 sweeps) as dark or bright. Forcing a tear in the horizontal sync can permit staggering the gap caused in each sweep. This can permit an alternate form of checking division by 15 (sweeps per line) in the sweep counter.

The MSB in the line count is white in the bottom half of the display. After the bottom bright trace of IC15-8, IC2-9 shows the bright inverse of 8 sweeps of vertical blanking at the bottom of the screen and the later sweeps normally hidden by the vertical blanking at the top of the screen.

Patterns for the symbol counter IC16(74394) can be directly inferred from the theory discussion and the pin outs of the 74393. The EOC pulses described in a.2.3 are seen as a vertical bar per symbol space on IC16-13. Successive divisions by 2 on pins 11, 10, 9, 8, 3, 4, and (if 64 symbol option, pin 5) are seen as fewer, wider bars. Reset will appear on pins 12 and 2 as it does at IC34-5 (Refer to Section a.2.5.)

The functions of IC12(74138) and IC34(74123) are not directly observable in the presence of sync. If no sync at all is reaching the raster, normal operation of IC34-13 can be noted as small (on the order of 30 nanoseconds)specks scattered in regular fashion throughout the raster. If sync is working, operation may be inferred by noting rapid regular jumping of vertical sync when IC34-1 is held to ground.

The combination of IC34b and IC12 can be checked by grounding pins 4 and 5 of IC3. Under this condition, the normal output connection to the display will show repetitions of seven darkened sweeps of vertical blank followed by thirty visible sweeps of retrace allowance. Also, placement of the test clip on IC12-12

will show continuous repetitions of seven dark sweeps, eight white sweeps, seven dark, fifteen white.

The outputs of the symbol and line counters should show obvious ÷ 2 relationships for ascending orders of bits. These patterns should be traceable through the MUX's IC's 17, 18, and 19(74157) and decoder IC11 to the associated RAM address input pins.

Normal events on the dot blank flip-flops IC32-2, 4, 5, and 8 (74LS74) produce vertical bars on a once per sweep basis. Position and width of the bars is variable by both "pos" and "width" pots. The waveform average of these waveforms read on a DC meter will also vary under control of these pots. If sync prevents visual observation of these pulses, DC voltage variations by the pots can be taken as proof that the variable width dot blank is reaching the right places.

a.3 Diagnostic aids

Viewing the display in normal conditions gives information on where to start troubleshooting. A blank screen directs attention to sections 3.2.1 through 3.2.5, which look for dynamically changing patterns originating in a sequentially scanned memory, being translated in the ROM's and being shifted out of the register. In the process, dot clocking and EOC signals are investigated as necessary.

A dynamic but useless display in normal conditions, on the other hand, directs attention to the subcounters and decoders which control memory address, the blanking of the display borders, and the orderliness of symbol element display.

Thoughtfully examining the display can give valuable clues for trouble locallizing. Torn-up symbols logically relate to the sweep counter and its derivatives in the line counter and vertical blanking. Wrong symbol displays indicate a need to also verify dynamic signal paths between symbol and line counters,

or the ability to load memory properly. Since many of these are interrelated in unpredictable syndromes, it is impractical to anticipate all combinations here. Problems relating to data exchanges between the memory and/or keyboard and the system CPU are not peculiar to the video display and should be approached in whatever is your standard method for handling problems with memory or peripherals.

a.3.1 time calibration

In verifying the timing diagrams related to horizontal sweep rates, the 4½ microsecond wide bars on IC1-14(74161) give a quick idea of how much of the timing diagram will show on your TV. A 50 microsecond block is indicated on most of the timing diagrams, but a typical TV might show five white and give black bars on IC1-14 for a total display of 45 microseconds. Remember also that horizontal sync may permissibly vary widely, so that your picture may start at a different point in comparison to the arbitrary marks on the diagrams.

Calibration of the vertical dimension or vertical sweep time base is perhaps easiest by looking at IC15-3(74393). The leading edges (measuring top to bottom) of the groups of white sweeps are 15 sweeps or 877 microseconds apart. A 16 line (240 sweep) visible raster is 14.04 milliseconds, and vertical sync recurs every 277 sweeps or 16.205 milliseconds.

Occasionally, an integrated circuit is itself defective. You can sometimes determine this by swapping ICs from one location on the board to another -- i.e., ICs that are used in more than one location (like memory). If you find that you were supplied with a defective chip, it will be replaced free (see the warranty information sheet included herein).

b. Central Processor Checkout

A malfunctioning central processor may not produce enough behavior to allow testing. For that reason, the following checkout procedure is limited. Checkout beyond the limits of this discussion should be performed by someone with a thorough knowledge of data processing electronics.

Begin by checking the data bus, pins 3 through 10 on IC14 (CPU), and the address bus, pins 25 through 27 and 29 through 40, for shorts to each other, to the power supply, or to ground.

Put your logic probe on pin 12 of the CPU chip. Logic should be low. Push RESET; logic should go high while RESET is held down. If the logic is otherwise, check IC13, the RESET button wiring, and the 33 μF capacitor. Check also for cold solder joints along the path from pin 75 of the bus to pin 2 of IC13.

Signal is high when RESET is held down, check ICs 17 and 30 (74LS174) and IC38 (74LS109) to see that the POC-signal is low. It should go high when RESET is released.

When you push RESET, the screen should clear and a prompt character appear in the upper left corner. If this does not happen, the CPU chip is not running. Check for a "reading" signal on pin 23 of the CPU chip. The signal should be high. If it is not, check ICs 13, 40(74LSØØ) and 1 (74LS13).

Now check for a sync signal on pin 19 on the CPU chip. There should be a pulse. If there isn't, hold down RESET and check to see if the signal is low on this pin; releasing RESET should cause momentary or continuous pulsing. If you are not getting the desired sync signal, check the board again for solder bridges with a magnifying glass. If the sync signal cannot be obtained, further checkout will require a high-quality oscilloscope and considerable experience.

If you do have a sync signal, check pin 9 of IC17(74LS174) for

pulses. If the sync signal isn't getting through to that point, check ICs 17, 13, 41(74LS109), and 12 (74LS04). If there is a pulse on pin 9 of IC17, but the system still does not work, further checkout will require a high-quality oscilloscope and considerable electronics experience. At this point, if you are not able to continue checkout on your own, you should talk to a knowledgeable friend or fellow club member, to the personnel at the store where you bought your system, or to the manufacturer.

b. Schematic Diagram

The schematic in the appendix gives a more detailed view of the central processor board circuitry. To get full use of the following discussion of the schematic, it is necessary to have some familiarity with the Intel 8080A CPU chip. We recommend reading the Intel Microprocessor User's Manual, chapter 1.

Power Supply

There are four voltages on the board: +12, -12, +5, and -5. The power supply section consists of ICs 32, 33, 34, and 44, and the associated capacitors.

CPU

Clock signal generation is provided by IC 13, running at 16.588 MHZ. That oscillation is divided by nine and used to form a two-phase clock, ø (Greek phi) 1 and ø 2 on the schematic. (The 8080 requires two phases.) These clocks time all processing.

Ready and reset signals are synchronized to the clocks in IC 13. The ready signal to IC 13 is generated by ICs 1 and 40.

If (BGNT+ and XRDY+ and PRDY+) or ONBD- are active, then a ready signal is generated.

A reset signal is produced when pin 75 of the backplane goes low. On application of power, this line is held low momentarily by the 33 F capacitor and the 4.7K resistor.

The reset signal labeled POC (power on clear) on the schematic, generated by IC 13, resets the CPU, IC 14, status latch IC 12, and baud rate port IC 30. It also resets a part of the single step log, IC 38, and the USART, IC 28. This signal also goes out to the backplane for use by other boards.

During the T1 cycle (see Intel manual), the system strobe signal SSTB is generated by IC 13. This signal is used by the status latch to latch the CPU status for the duration of the memory cycle that follows.

The output of the status latch is used directly on the CPU board; it is also buffered by ICs 7 and 8 and goes on to the backplane. Both phases of the clock signal are also buffered in ICs 7 and 8 and sent to the backplane.

Clock phase ø1 is converted to TTL levels by the diode and the 2.2K resistor.

SYNC, DBIN (data bus in), and WR (write) strobes are buffered in IC 3 and also connect to the bus.

Data Paths

The CPU data bus is connected to the on-board ROMs amd RAMs, ICs 21 through 27, the USART, IC 28, and the baud rate generator port, IC 30. The data bus is also connected to ICs 5, 6, and 7, which are buffers leading to the data out bus on the backplane.

Data in from the backplane comes through ICs 15 and 16, two input multiplexors. Other multiplexor input comes from IC 2, the priority encoder. This IC encodes eight interrupts into eight restart instructions, RST Ø through RST 7.

Address Decoding

The CPU address bus is connected to ICs 21 through 27 (RAMs and ROMs), and to the address bus on the backplane through ICs 3 through 6, tri-state buffers. The lower eight bits of the address bus are connected to RAMs ICs 21 through 24. The upper four address bits are connected to IC 35, which generates signal ONBD- when all four bits are low. This determines whether on-board or off-board memory is accessed. If off-board memory is being accessed, ONBD is not active. If it is not active, there is no ready signal to the CPU till BGNT and XRDY and PRDY are active. If they are not active, the CPU waits till it can get access to the bus and till the device it is addressing is ready. Access to the bus is determined by BGNT (bus grant); XRDY and PRDY indicate that the addressed device is ready.

For accessing on-board memory, address decoder IC 36 is enabled via a connection to the EØ input (enable Ø) except when in an interrupt acknowledge cycle, in which case E1, connected to INTA+ (interrupt acknowledge), will be high, which inhibits IC 36.

Decoder IC 36 decodes the next two lower address lines, A1Ø and A11, along with the signal indicating whether we are in a memory cycle or an input-output cycle. The I/O select signal is generated by IC 37, which ORs together input and output status signals from the status latch.

The decoder generates eight output signals. Three of them select one of three on-board ROMs; these signals are ANDed with DBIN in IC 39 and applied to chip selects on ICs 25, 26, and 27. These three signals, MSØ, MS1, and MS2 correspond to address Ø through BFF hex. The fourth memory select signal, MS3, enables on-board RAMs, ICs 21 through 24, for addresses cØØ through FFF hex. (CPU)

Further address decoding is provided by IC2, which is connected to A8. The remaining four signals, PSØ through PS3, select on-board I/O ports. PS Ø selects IC 28, the USART. Address decoding also is provided by AØ, connected to pin 12 of IC 28. The USART is located at addresses Ø through 3. Addresses 4 through 7, PS1, select the baud rate port, IC 30. Addresses 8 through B hex select the real-time clock, which uses ICs 20, 10, and 37. PS3, at addresses C through F hex, selects the single-step logic, which uses ICs 37, 38, 40, and 41.

Serial I/O Port

Circuitry for the optional serial input-output port consists of the USART IC 28, baud rate generator IC 29, baud rate port IC 30, buffer IC 31, and NOR gate IC 18. The clock signal for the USART is generated from ø2 of the system clock by division by two in IC 38 and further division in IC 29; the division ratio is selected by the data held in output port IC 30. The

resulting frequency goes to the USART and through the buffer in IC 31 out to the serial I/O device, which connects to one of the 14-pin sockets on the CPU board.

The USART converts serial data to parallel form and puts it on the data bus for the CPU, or takes parallel data from the CPU and converts in to serial form.

The NOR gate, IC 18, ties the USART to the vectored interrupt system.

Real-Time Clock

The real-time clock is derived from a 60HZ rectified sine wave present on the backplane. The sine wave is converted to a square wave in the Schmiddt trigger, IC 20, and toggles the flip-flop IC 10 on each positive-going transition. Output of IC 10 jumper pad A may be tied to the vectored interrupt system. IC 10 may be reset by writing to output port 8. This generates PS2- and WR-, which are ANDed together in IC 37 and used to reset the flip-flop.

Single-Step Logic

Single-step logic provides for causing an interrupt two instruction cycles after the logic has been enabled. Single-step logic is enabled by issuing an OUT C hex through OUT F hex instruction. PS3 and WR- are ANDed together in IC 37 and used to reset flip-flop IC 38. This causes $\overline{Q}$ output to go high, enabling IC 41. Input to the first section of IC 41 consists of clock signal SSTB- and a signal off the bus, D5. If SSTB- occurs while D6 is high, then the left-hand flip-flop of IC 41 will toggle, causing $\overline{Q}$ to go low. The next occurrence will cause $\overline{Q}$ to go high, creating a positive edge on the clock input to the right-hand flip-flop of IC 41. This will cause IC 41 to be set, generating an interrupt. During the interrupt acknowledge cycle, INTA+ will be true. This signal is applied to the J input of IC 38. This flip-flop is clocked by DBIN-. On the rising edge

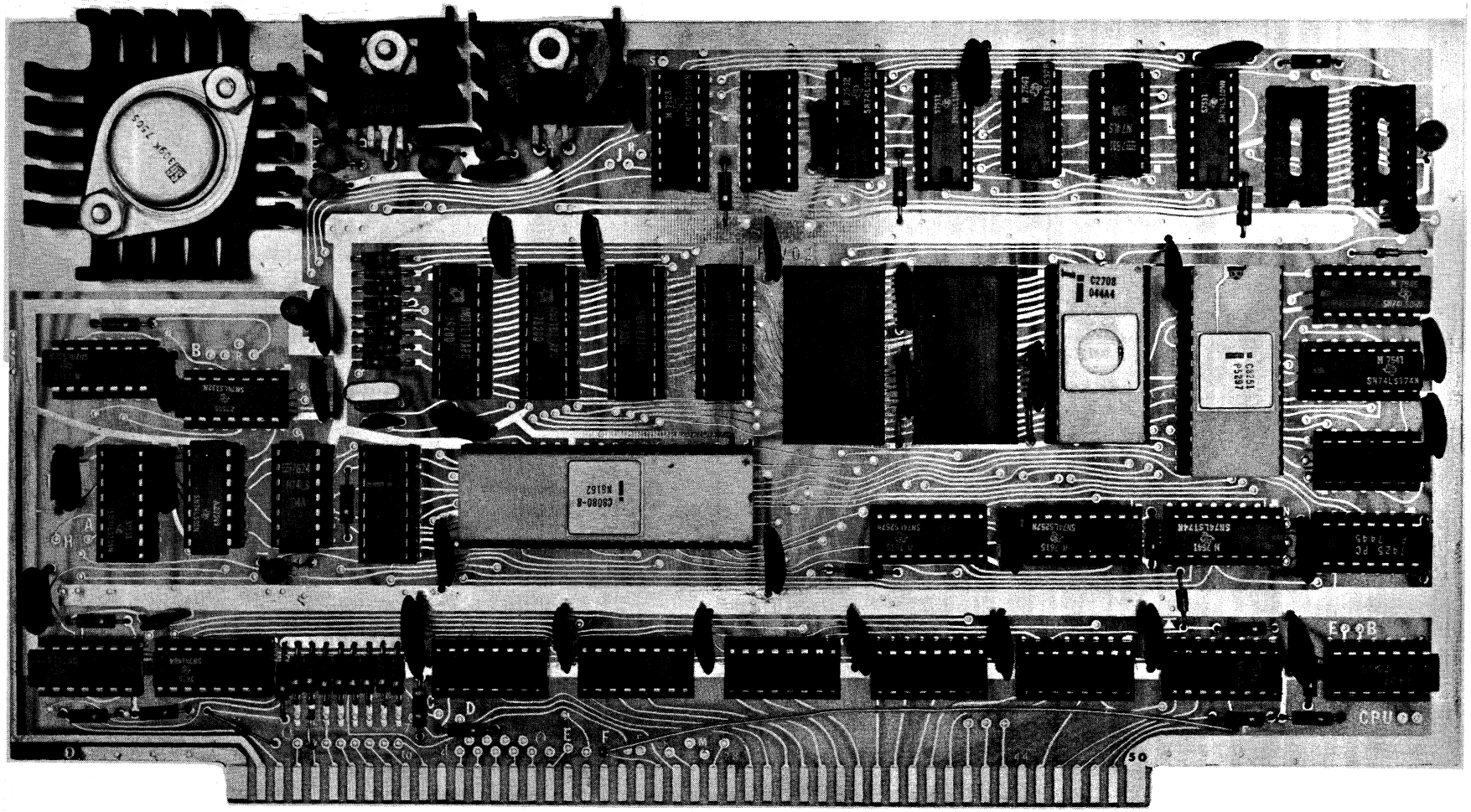
of DBIN-, and if J is high (at the end of the interrupt acknowledge cycle), IC 38 will be set, causing $\overline{Q}$ to return low, which in turn resets IC 41, which in its turn clears the interrupt.

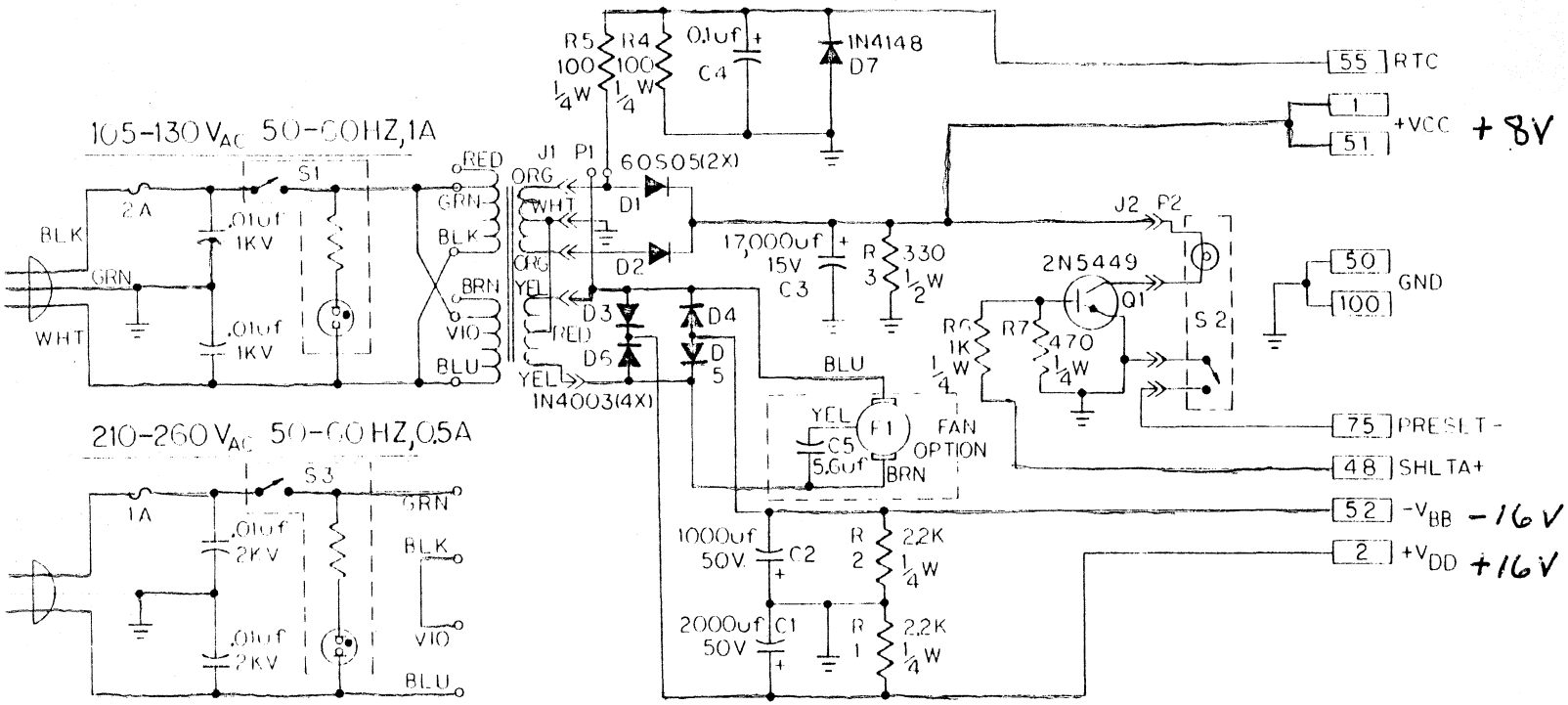
While IC 38 is reset, other interrupts are inhibited. In order to inhibit interrupts, the $\overline{Q}$ output of IC 38 is tied to the $\overline{\text{enable}}$ of IC 2, the priority encoder. The interrupts from this encoder and the interrupt logic are ORed together in IC 40 and applied to the interrupt input on the CPU.

Bus Request Logic

Bus request logic uses ICs 10, 20, 19, 11, and 12. To generate a bus request, ONBD- must be high. ONBD- is ANDed with SSTB+, pin 4 of IC 12, in IC 20, and is used to set the flip-flop, pin 11 of IC 10. This causes $\overline{Q}$, pin 9 of IC 10, to go low, generating a bus request. The bus request is cleared at the end of the memory cycle when WR- goes high (if a write cycle) or when DBIN- goes high (if a read cycle). These two signals are ANDed together in IC 19 and applied to the clock input of IC 10, causing a Ø to be read into IC 10, which causes $\overline{Q}$ to go high. IC 10 may also be reset by POC+ or HLTA+. These two are ORed together in IC 11 and applied to pin 15 of IC 10.

APPENDICES


CPU



NOTES:

1. FOR HIGH LINE VOLTAGE OR IN SMALL SYSTEMS USE RED AND BRN TAPS INSTEAD OF GRN AND VIO, RESPECTIVELY.
2. ALL RESITANCE VALUES ARE IN OHMS.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN DAVID FORRESTER	10/19/76
CHECKED	

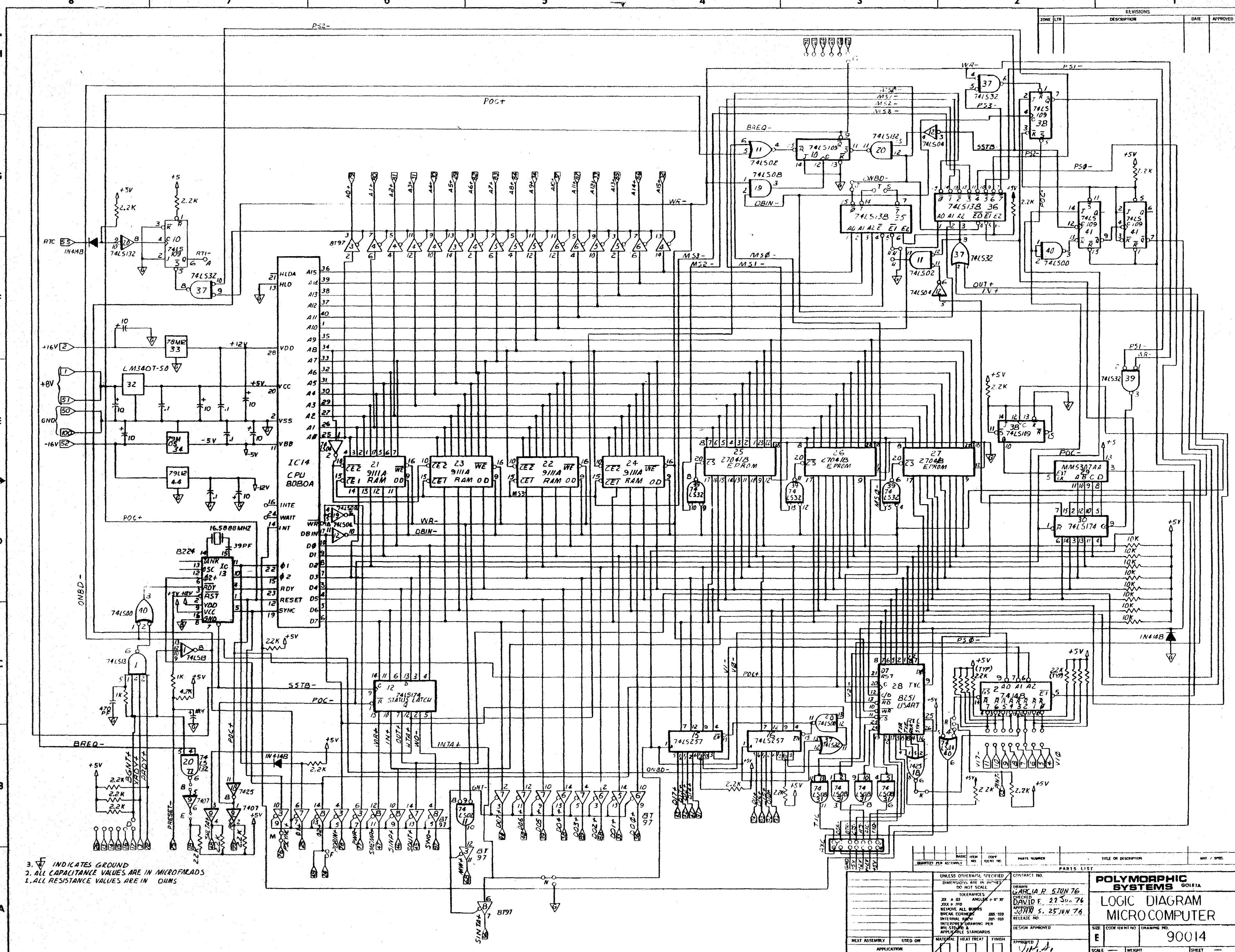
NEXT ASSY | USED ON

APPLICATION

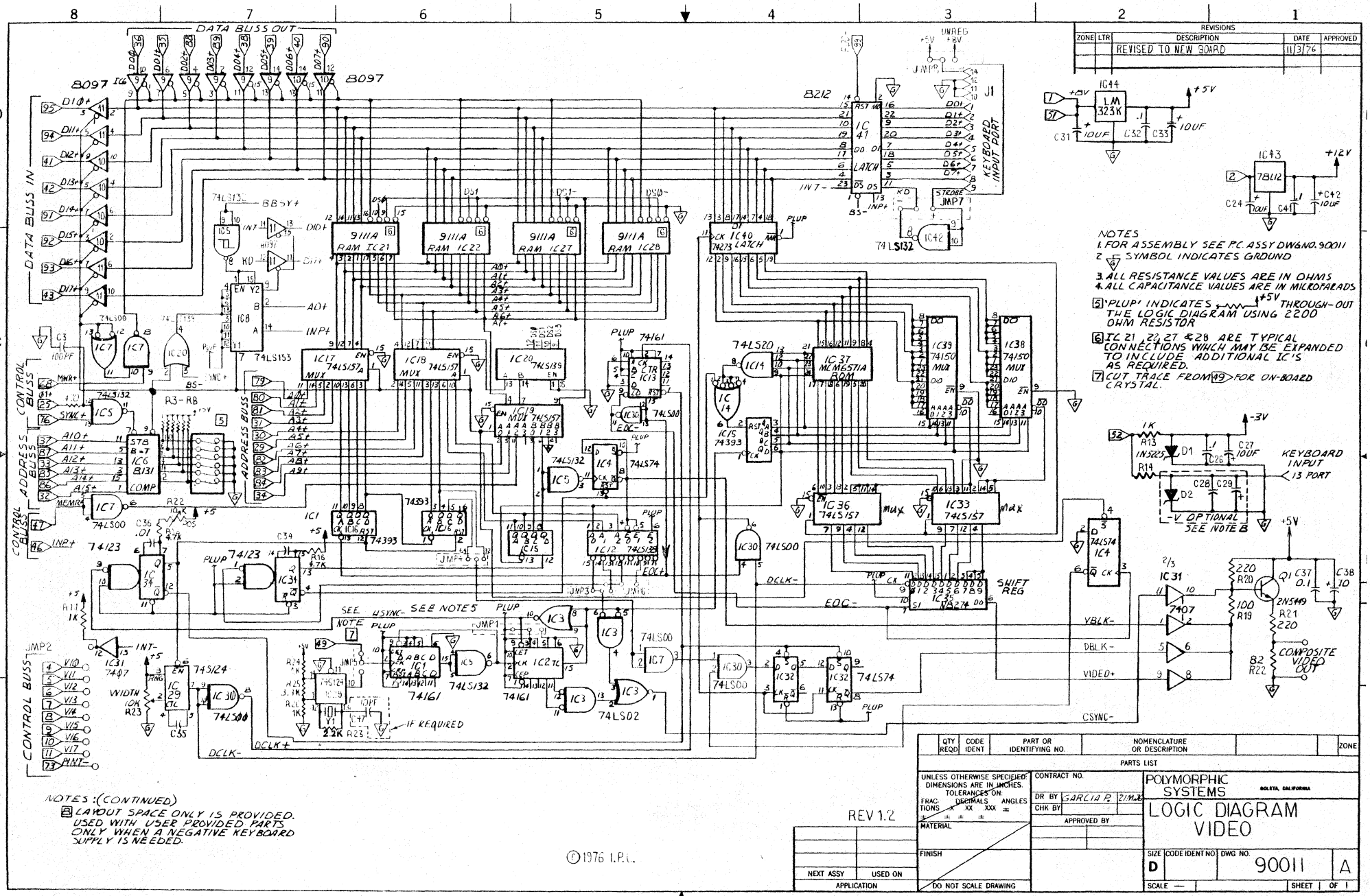
SCHEMATIC DIAGRAM POLY-88 POWER SUPPLY

SIZE	CODE IDENT NO.	DRAWING NO.
C		90021

SCALE | SHEET / OF /


3. INDICATES GROUND
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS
1. ALL RESISTANCE VALUES ARE IN OHMS
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DO NOT SCALE
TOLERANCES
REMOVE ALL BURRS
BREAK CORNERS
INTERNAL RADII
INTERPRET DRAWING PER MIL-STD-100 & APPLICABLE STANDARDS
NEXT ASSEMBLY
USED ON
APPLICATION
MATERIAL
HEAT TREAT
FINISH
CONTRACT NO.
DRAWN GARCIA R. 5 JUN 76
CHECKED DAVID F. 23 JUN 76
APPROVED JOHN S. 25 JUN 76
RELEASE NO.
DESIGN APPROVED
POLYMORPHIC SYSTEMS GOLETA
LOGIC DIAGRAM
MICRO COMPUTER
SIZE E
DRAWING NO. 90014
SCALE
WEIGHT
SHEET

Circuit Description
Vol. I Pg. 45



NOTES
1. FOR ASSEMBLY SEE PC ASSY DWG NO. 90011
2. ⏚ SYMBOL INDICATES GROUND
3. ALL RESISTANCE VALUES ARE IN OHMS
4. ALL CAPACITANCE VALUES ARE IN MICROFARADS
5. 'PLUP' INDICATES +5V THROUGH-OUT THE LOGIC DIAGRAM USING 2200 OHM RESISTOR
6. IC 21, 22, 27 & 28 ARE TYPICAL CONNECTIONS WHICH MAY BE EXPANDED TO INCLUDE ADDITIONAL IC'S AS REQUIRED.
7. CUT TRACE FROM (19) FOR ON-BOARD CRYSTAL.

NOTES: (CONTINUED)
8. LAYOUT SPACE ONLY IS PROVIDED. USED WITH USER PROVIDED PARTS ONLY WHEN A NEGATIVE KEYBOARD SUPPLY IS NEEDED.

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		REVISED TO NEW BOARD	11/3/76	

REV 1.2

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING

CONTRACT NO.
DR BY GARCIA P 2/1/77
CHK BY
APPROVED BY

POLYMORPHIC SYSTEMS GOLETA, CALIFORNIA

LOGIC DIAGRAM
VIDEO

SIZE D | CODE IDENT NO. | DWG NO. 90011 | A
SCALE — | SHEET 1 OF 1

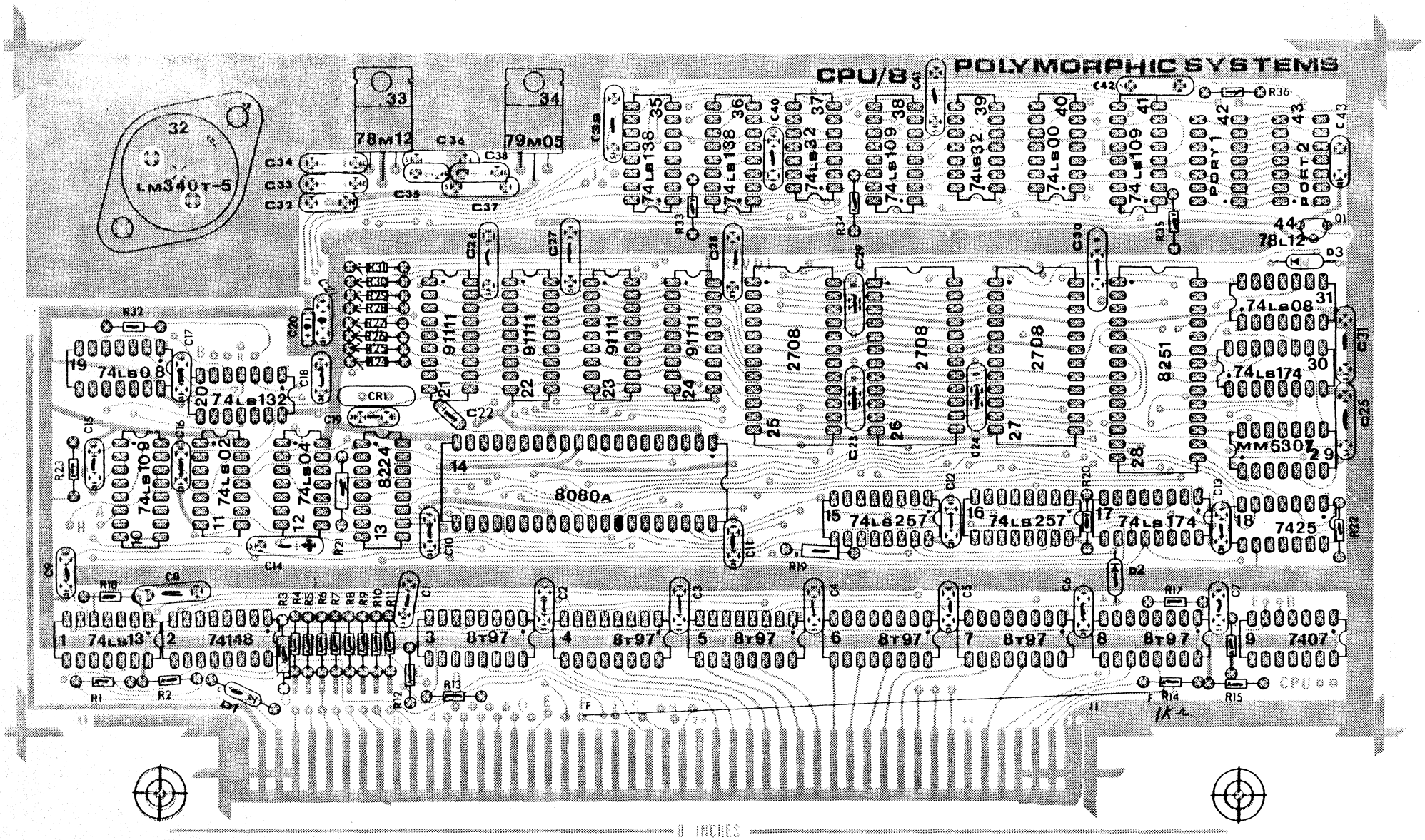
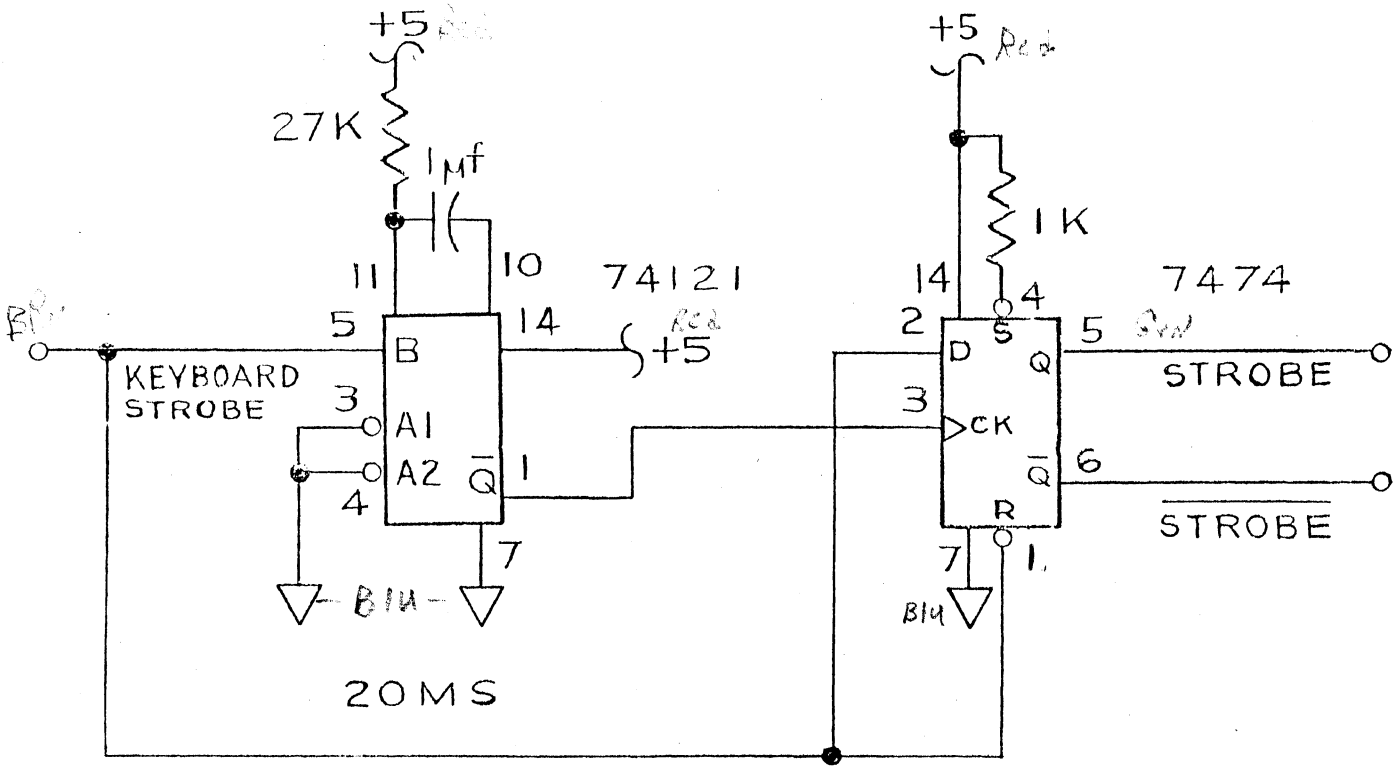

CPU/8
POLYMORPHIC SYSTEMS
LM340T-5
78M12
79M05
74LS138
74LS32
74LS109
74LS00
74LS08
74LS174
74LS132
74LS109
74LS02
74LS04
74LS257
74LS257
74LS174
74148
8T97
7407
2708
8251
8224
8080A
78L12
MM5307
7425
PORT 1
PORT 2
8 INCHES

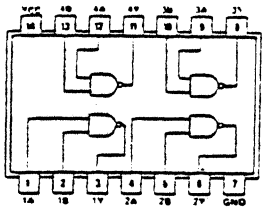
figure A-3

TTY33-53B

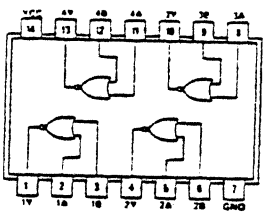
SHOULD STROBE DEBOUNCE BE NECESSARY THE FOLLOWING SIMPLE CIRCUIT IS RECOMMENDED AS AN INTERFACE.



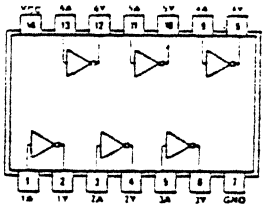
DATA LINE AND SPECIAL FUNCTION KEY INTERFACE SHOULD BE TTL OR EQUIVALENT COMPATIBLE, HAVING AN INPUT LOW VOLTAGE OF 0.0 TO 0.8V AND AND INPUT HIGH VOLTAGE OF 2.0 TO V_{CC}.



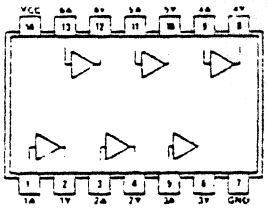
SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)



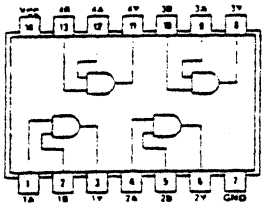
SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



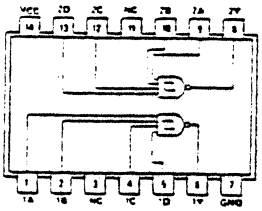
SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)



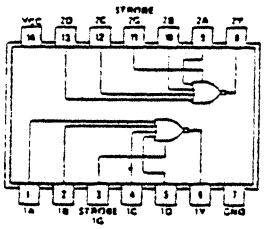
SN5407/SN7407(J, N, W)



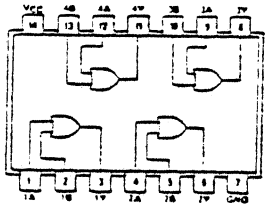
SN5408/SN7408(J, N, W)
SN54LS08/SN74LS08(J, N, W)



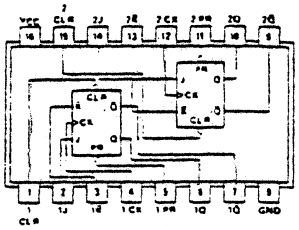
SN5413/SN7413(J, N, W)



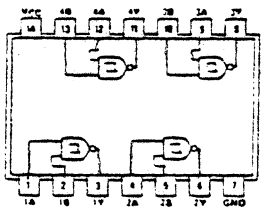
SN5425/SN7425 (J, N, W)



SN5432/SN7432(J, N, W)
SN54LS32/SN74LS32(J, N, W)

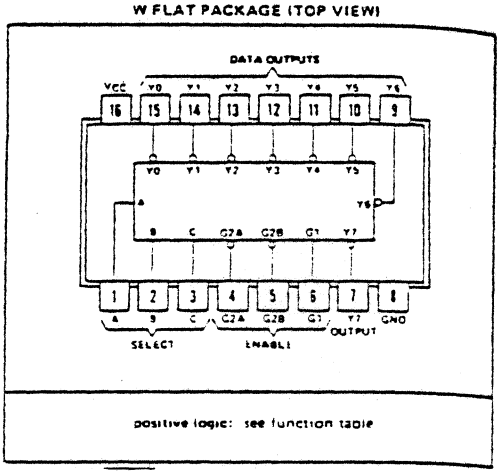


SN54109/SN74109(J, N, W)
SN54LS109/SN74LS109(J, N, W)

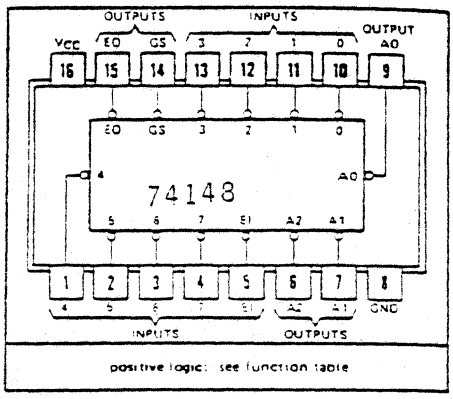


SN54132/SN74132(J, N, W)
SN54S132/SN74S132(J, N, W)

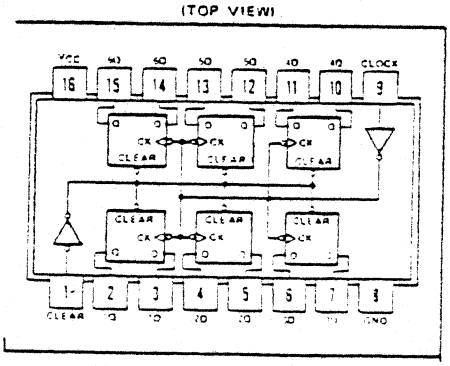
'LS138, 'S138
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



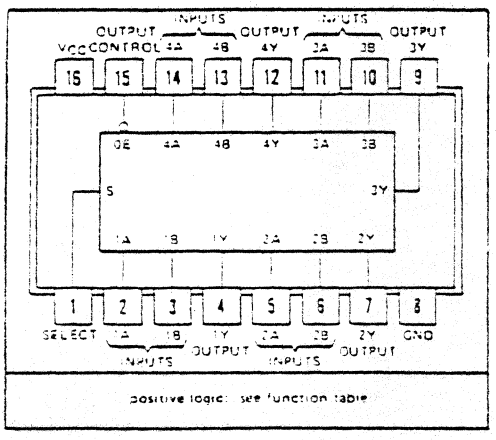
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

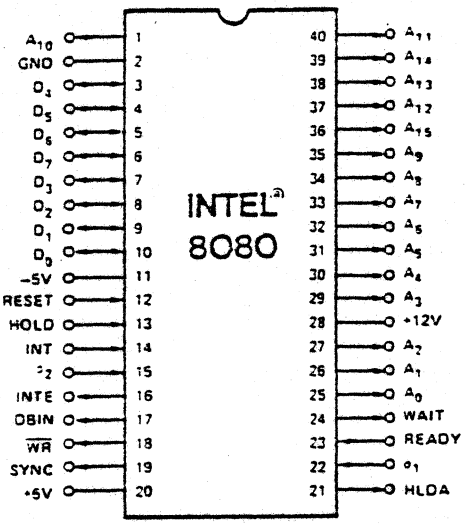


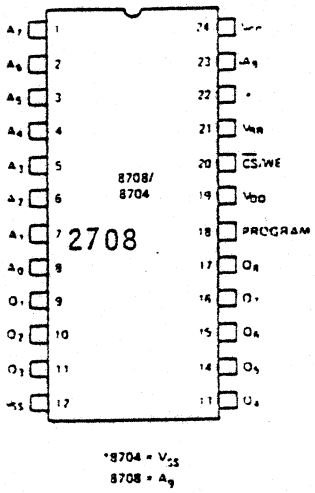
SN54S174 J OR W PACKAGE
'174, 'LS174, SN74S174 J, N, OR W PACKAGE
(TOP VIEW)

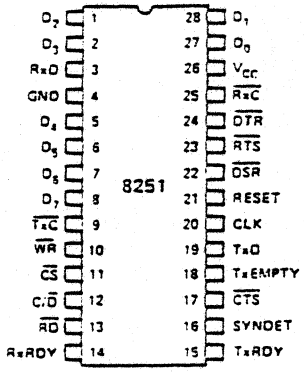


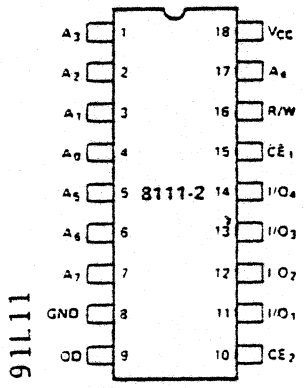
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)
SN54S257, SN74S257

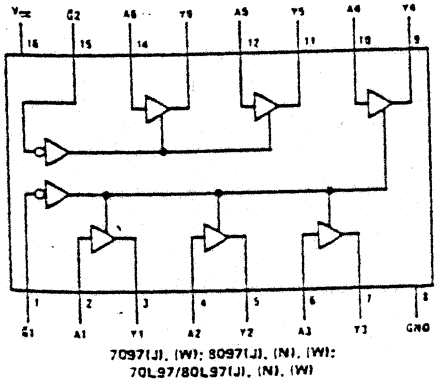




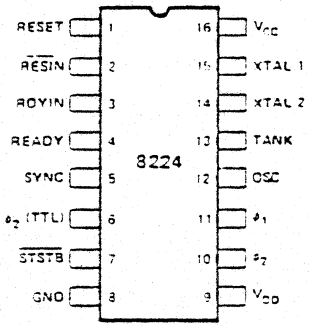




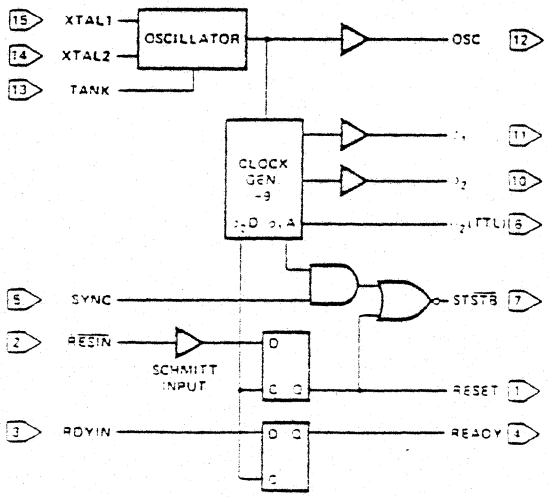




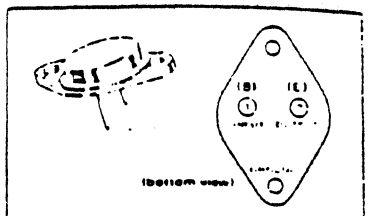
PIN CONFIGURATION



BLOCK DIAGRAM



POSITIVE
VOLTAGE REGULATOR
MONOLITHIC SILICON
INTEGRATED CIRCUIT



K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 Type)

CASE 199-04
(P Suffix)

CASE 79-02
TO-39
(G Suffix)

POSITIVE, 500 mA – MC78M00 Series

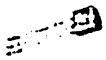
Family Characteristics
0 to +125°C Junction Temperature
I_O – 500 mA (Max)
V_O – ±5% of nominal voltage for all line and load condition limits

Nominal V_O	V_I (dc) Min	V_I (dc) Max	Device Type
5 V	7 V	35 V	MC78M05C
6 V	8 V	35 V	MC78M06C
8 V	10.5 V	35 V	MC78M08C
12 V	14.5 V	35 V	MC78M12C
15 V	17.5 V	35 V	MC78M15C
18 V	21 V	35 V	MC78M18C
24 V	27 V	40 V	MC78M24C

NEGATIVE, 100 mA – MC79L00 Series

Family Characteristics
0 to +175°C Junction Temperature
I_O – 100 mA (Max)
V_O – ±10% of nominal voltage for all line and load condition limits

Nominal V_O	V_I (dc) Min	V_I (dc) Max	Device Type
3 V	5 V	30 V	MC79L03C
5 V	7 V	30 V	MC79L05C
12 V	14.5 V	35 V	MC79L12C
15 V	17.5 V	35 V	MC79L15C
18 V	21 V	35 V	MC79L18C
24 V	27 V	40 V	MC79L24C



*CASE 29-02
TO-92
(P Suffix)

CASE 79-02
TO-39
(G Suffix)

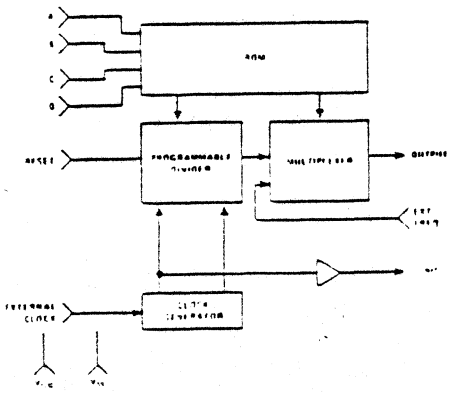
CASE 199-04
(P Suffix)

CASE 11
(K Suffix)

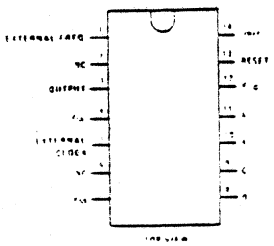
NEGATIVE, 1.5 A – MC7900 Series

Family Characteristics
0 to +125°C Junction Temperature
I_O – 1.5 A (Max)
V_O – ±5% of nominal voltage for all line and load condition limits

Nominal V_O	V_I (dc) Min	V_I (dc) Max	Device Type
2 V	7.2 V	35 V	MC7902C
5 V	7 V	35 V	MC7905C
5.2 V	7 V	35 V	MC7905.2C
6 V	8 V	35 V	MC7906C
8 V	10.5 V	35 V	MC7908C
12 V	14.5 V	35 V	MC7912C
15 V	17.5 V	35 V	MC7915C
18 V	21 V	35 V	MC7918C
24 V	27 V	40 V	MC7924C



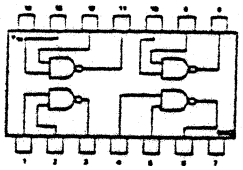
Dual In-Line Package



Order Number MM5307 AA/D
See Package 2
Order Number MM5307 AA/N
See Package 14

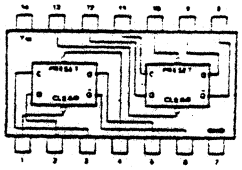
A,F PACKAGE

7400

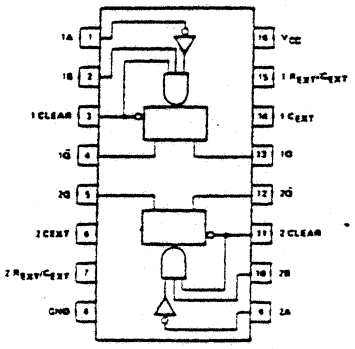


A,F PACKAGE

7474

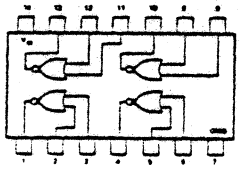


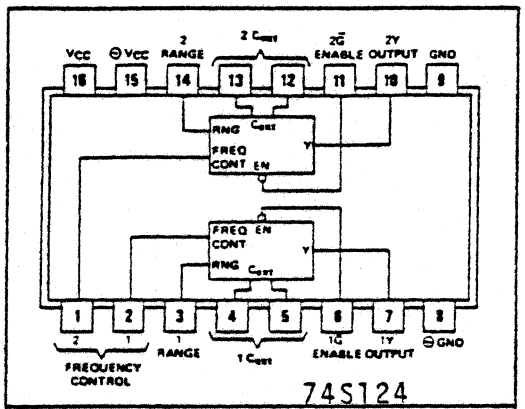
74123



A,F PACKAGE

7402

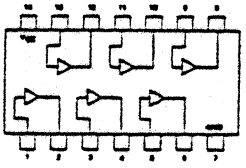




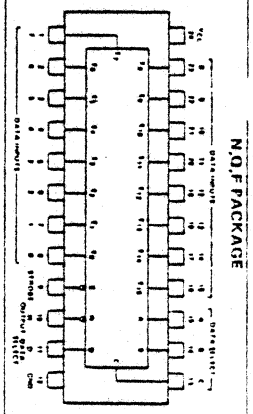
positive logic: While the enable input is low, the output is enabled. While the enable input is high, the output is high.

A,F PACKAGE

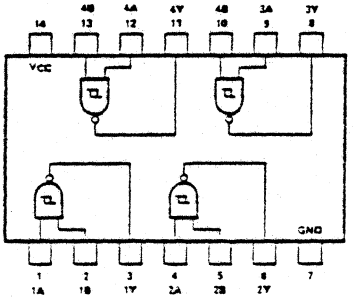
7407



74150



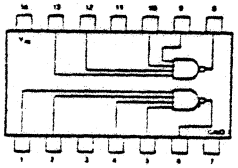
SS4132, N74132



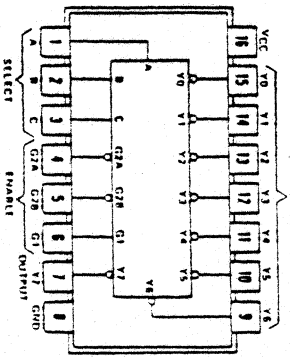
POSITIVE LOGIC: $Y=\overline{AB}$

A,F PACKAGE

7420

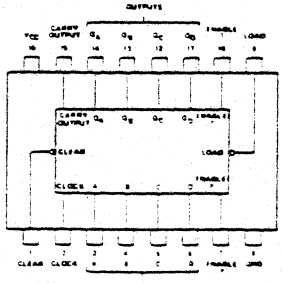


74LS138



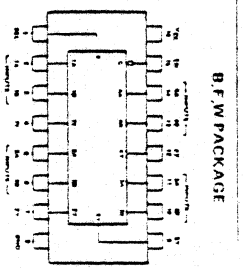
positive logic: see function table

B,F,W PACKAGE

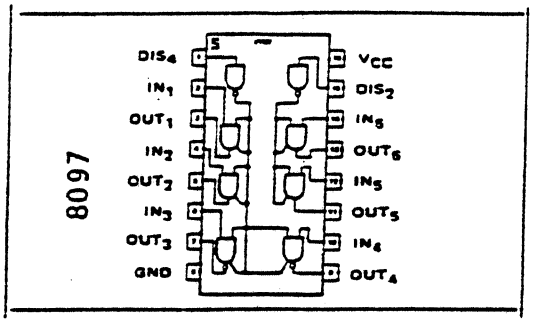


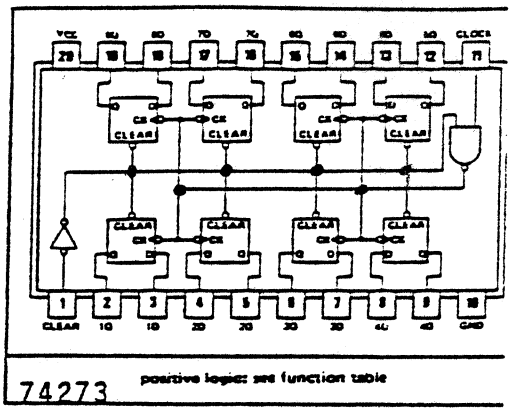
74161

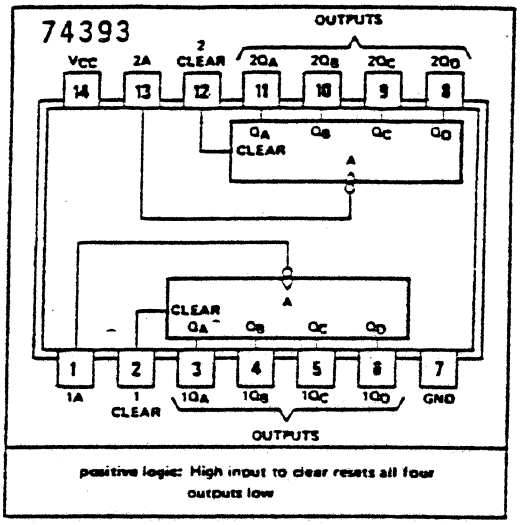
74157

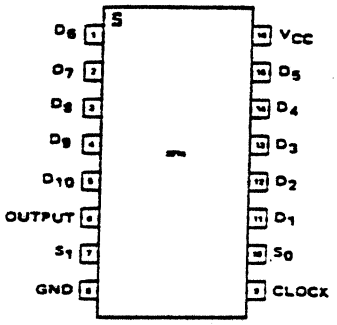


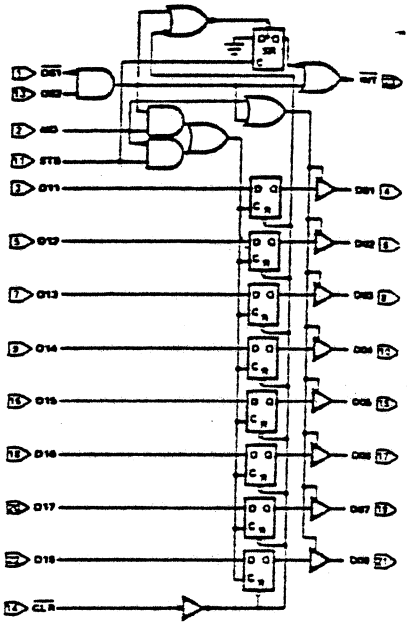
APPENDIX B: Chip pinouts

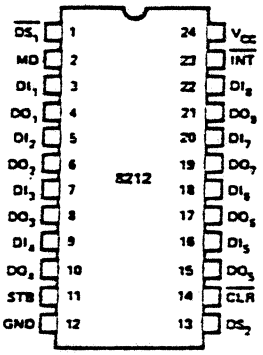


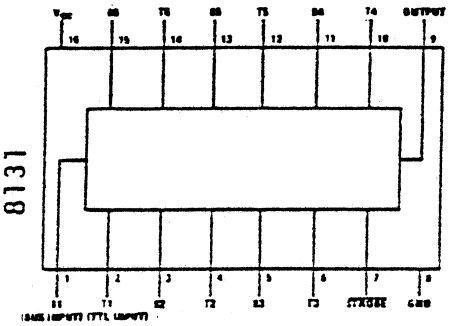




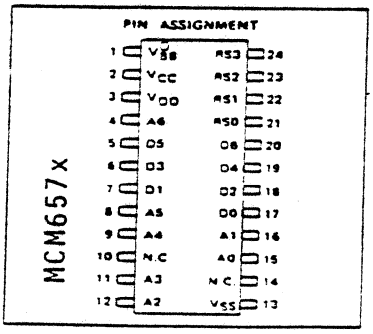


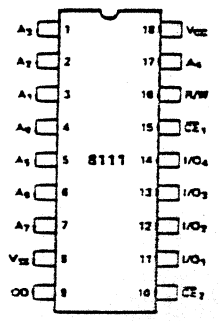




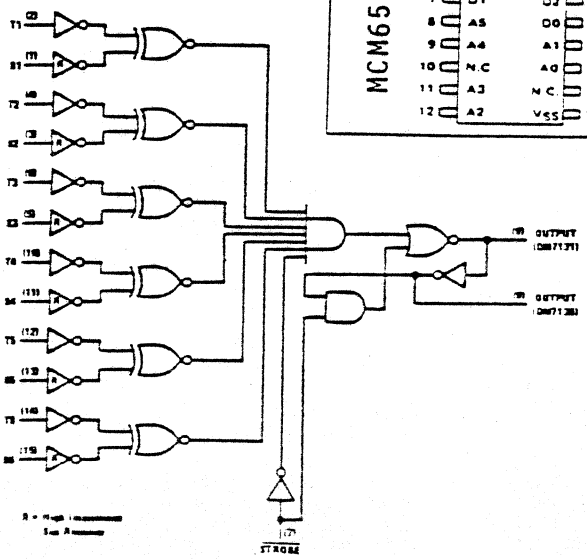


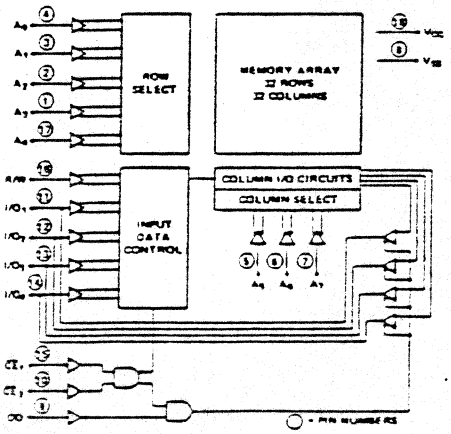
7131(J), (W); 8131(J), (N), (W);
7136(J), (W); 8136(J), (N), (W)

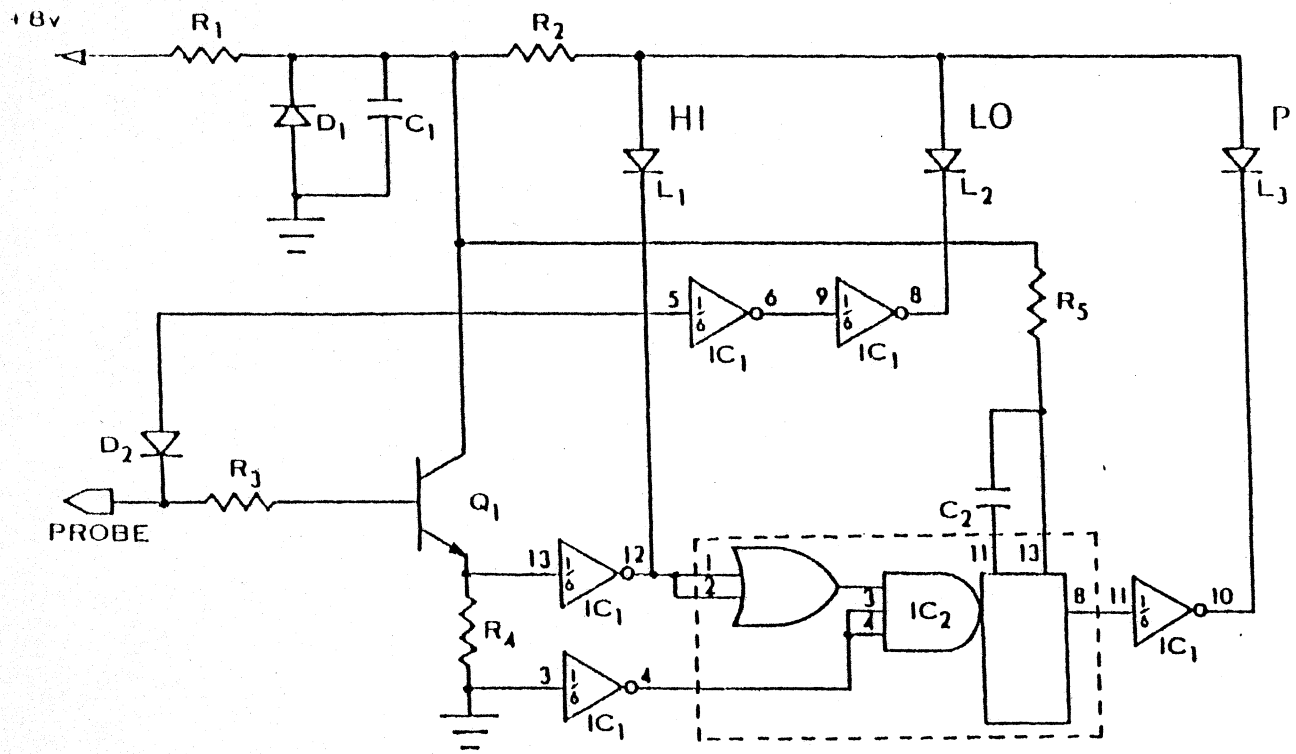




Logic Diagram







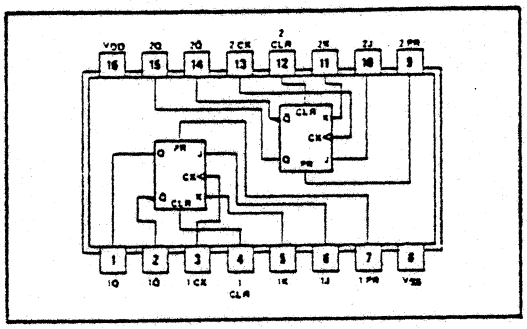
C1,C2 - 39μF 10 volt capacitor
D1 - 5.1 volt zener diode
D2 - 1N914 or 1N4148 diode
IC1 - 7404 hex inverter
IC2 - 9601 retriggerable one-shot
L1 - red LED
L2 - green LED
L3 - yellow LED
Q1 - 2N4401 transistor
R1 - 68 ohm ¼ watt resistor
R2 - 270 ohm ¼ watt resistor
R3 - 10K ohm ¼ watt resistor
R4 - 1K ohm ¼ watt resistor
R5 - 30K ohm ¼ watt resistor

TEST PROBE SCHEMATIC

CHIP PINOUTS

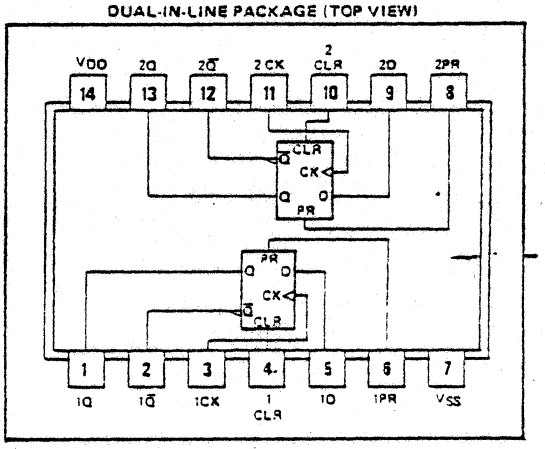
TF4027A, TP4027A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

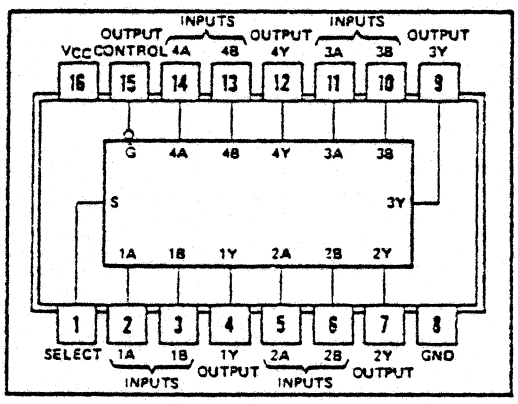


TF4013A, TP4013A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

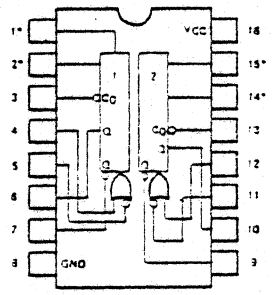


SN54LS257, SN54S257 . . . J OR W PACKAGE
SN74LS257, SN74S257 . . . J OR N PACKAGE
(TOP VIEW)

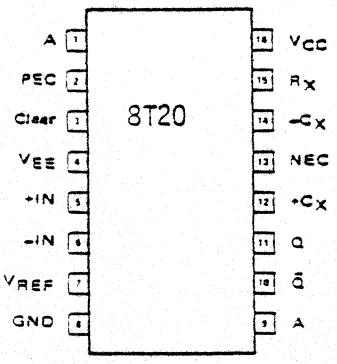


CONNECTION DIAGRAMS
DIP (TOP VIEW)

96L02

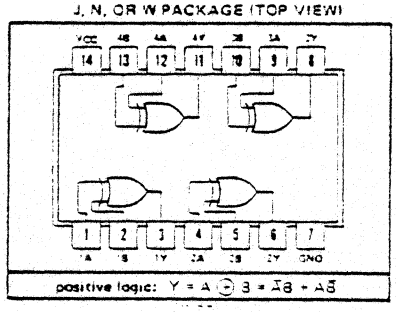


*Pins for external timing.



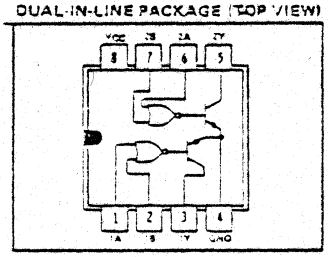
SN74LS86

J, N, OR W PACKAGE (TOP VIEW)



SN754538

DUAL-IN-LINE PACKAGE (TOP VIEW)



1. On Page 4, Bag #2 should have 24 2,200 ohm resistors and 3 1,000 ohm resistors.

2. Figure A-2 is not labeled. It is located between pages 9 and 10.

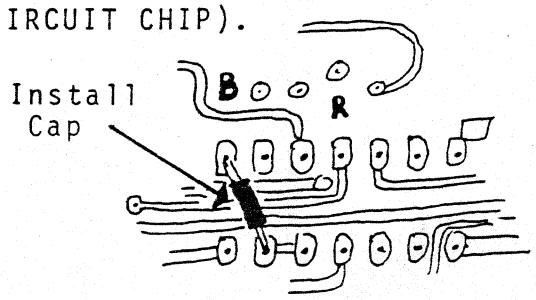
3. On page 16, IC 19 is listed as a 7425, and IC 18 is not listed. Actually, IC 19 is a 74LS08 and IC 18 is the 7425.

4. On Page 17, the resistor list should read as follows:

( )	1 through 11	2,200-ohm
( )	12	4,700-ohm
( )	13	2,200-ohm
( )	14	1,000-ohm
( )	15 through 17	2,200-ohm
( )	18	1,000-ohm
( )	19 through 20	2,200-ohm
( )	21	1,000-ohm
( )	22 through 23	2,200-ohm
( )	24 through 31	10,000-ohm
( )	32 through 36	2,200-ohm

5. R14 on the CPU board schematic is incorrectly designated 2.2K -- it should be 1K.

6. The real time clock (RTC) runs too fast on some POLY 88's. To eliminate this problem, install a 0.1µF ceramic disc capacitor from pin 9 to pin 7 on IC20 (74LS132) of the CPU board. Keep the leads short in length to avoid shorting them to other circuitry. Install the capacitor on the rear of the board (DO NOT SOLDER THE CAPACITOR DIRECTLY TO THE INTEGRATED CIRCUIT CHIP).



7. Connection hardware has been provided for keyboard input and video output. The recommended connector configuration for the keyboard is as follows:

Cannon Jack	Dual-in-line socket
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10 - 13	No connection
14 - 22	ground (10, 11, 12)
23	13
25	14

9. For Rev. 1.2 VTI only: One Page 20, there are two errors. The color code for R17 (2200 ohm) should be red-red-red. R25 should be a 3300 ohm resistor with a color code or orange-orange-red.

10. The stripe down the side of a color coded tantalum capacitor indicates the positive lead.

11. On page 6, there should <u>not</u> be a 470pf ceramic capacitor in Bag #1.