DIGITAL COMPUTER
NEWSLETTER

OFFICE OF NAVAL RESEARCH · MATHEMATICAL SCIENCES DIVISION

TABLE OF CONTENTS

Issue I

Eniac

When the Eniac was moved to Aberdeen, provision was made for the installation of two new panels. One of these, the converter, has been in operation about six months. This has made possible the expansion of the proposed sixty order code to the ninety-odd orders presently available. The introduction of the code has been accompanied by a great increase in operating efficiency. How much of this is due to the code and how much to other changes introduced at the same time is not known. The second additional panel is the register. This is a high-speed mercury memory unit, which will increase the internal number storage capacity of the Eniac from 20 to 120 ten-digit numbers. It has been built at the Moore School, University of Pennsylvania, and is being given its preliminary testing there. A new code is nearing completion which will utilize the register and greatly increase the speed of operation as compared with the present code, probably by a factor of about three. Subsidiary equipment necessary to implement this code is being built at Aberdeen. The code will probably be introduced as soon as the register is installed and tested.

Edvac

The construction of the Edvac at the Moore School has been completed. Its testing is to be done partly there and partly after moving it to Aberdeen. It operates on a megacycle pulse rate as compared to 100 kilocycles for the Eniac. Because of its serial operation, however, the overall speed is about the same. It has an internal memory of the mercury tank type with a capacity of 1024 words where each word may be the binary equivalent of a 12 digit number or an order in a four-address code. The four addresses give the

locations in the memory of two numbers to be operated on, the location where the result is to go, and the location of the next order to be executed. The external memory is on magnetic tape. All arithmetic operations are performed in duplicate on two separate arithmetic organs and the machine is halted if these fail to agree.

Ordvac

The Ordnance Department is negotiating a contract with the University of Illinois for a machine to be called the Ordvac. Design data for components of the Ordvac will be drawn from the results of the research and development work being carried out by the Institute for Advanced Study, which is under Army Ordnance contract supported by the Air Force, ONR and A. E. C.

Institute for Advanced Study Computer

At the present time the principal emphasis of the group at the Institute for Advanced Study is on the arithmetic and memory organs of the machine under development there. The arithmetic organ will contain three so-called shifting registers, an adder and gates for going into and out of the adder. Life tests have been proceeding for some time on the shifting registers, and they seem to perform satisfactorily. The adder was recently installed and given an initial test. On the basis of this test it would seem that with safety factors an addition time will be of the order of 10 microseconds. As soon as the gate chasses mentioned above are completed the arithmetic organ will be operated at a high duty cycle as an adder.

In addition to following the RCA development of the Selectron the group at the Institute is carrying out a program to modify somewhat the circuits used by F. C. Williams in his electrostatic storage tube. The latest version by the Institute group of this memory tube is now being built, and continuing tests will be made within the next several months.

The Binac

Some time ago, the Eckert-Mauchly Computer Corporation finished construction of two Binary Computers, known as BINACS, each having an acoustic delay line memory of 512 words of 30 binary digits each. Very rigorous tests of all circuits have been made so that experience with these computers would be available for use in completing the final design of the UNIVAC System. Various mathematical routines have been run without error, many of them for extended periods, as a part of the BINAC testing program. Mathematical and circuit checks are continuing.

At the Convention of the Institute of Radio Engineers, March 8, in New York, Mr. Eckert, Mr. Lukoff and Mr. Smoliar presented a summary of their work on a "Dynamically Regenerated Electrostatic Memory for Computers." This memory uses a standard electrostatic deflection oscilloscope tube already being manufactured. A small model of this memory has already been tested and a larger one is now being prepared for test.

The Eckert-Mauchly Computer Corporation has moved its offices and library to 3747 Ridge Avenue, Philadelphia, where it will have expanded facilities.

Raytheon Computer

An ONR Computer, intended for use in one of the activities of the National Applied Mathematics Laboratories of the National Bureau of Standards, has been ordered by the Bureau from the Raytheon Manufacturing Company. Interesting features of the design are (a) the inclusion of extensive checking facilities and (b) the provision for an acoustic memory that can be expanded to 4096 words (numbers or instructions). As delivered, the computer will have a memory of 1024 words, but additional blocks of 1024 words each can be added as desired without revision of the computer circuits. Multiplication time is expected to be of the order of 1000 micro-seconds, including access times to the high speed memory. Raytheon has done considerable component research on the acoustic memory, the magnetic tape auxiliary memory, and the arithmetic unit.

National Bureau of Standards Interim Computer

The complexity of the large computer just discussed makes its construction a long-range project. However, by scaling down certain features of the machine, such as the high speed memory, it would be possible to assemble within a much shorter period a computer capable of solving many of the less complicated problems that continually arise in scientific work. In an effort to provide useful interim equipment the Bureau has undertaken the construction of a modest serial type machine operating at a repetition rate of 1 mega-cycle per second. The memory unit will consist of acoustic delay lines similar to those used in the EDVAC. The interim computer will have 500 words of memory, with provisions for later expansion to 1,000 words. The control will be limited to about seven commands, which have been selected to be logically sufficient to perform any ordinary sequence of computations. The input and output for the machine will initially consist of punched paper tape, with arrangements for later replacement by magnetic recording media. The block diagrams of the machine system are essentially complete and much of the circuitry has been determined. Extensive use is being made of pulse transformer techniques to achieve A-C coupling throughout the machine. Nearly all of the switching functions will be accomplished by crystal diode circuits. A number of prototype circuits have been assembled and all have functioned reliably in tests that have been carried out on them. It is expected to have the minimum version of the Interim Computer assembled by the end of the year. This computer is being built at the Washington Laboratory.

Institute for Numerical Analysis Computer

A computing machine is being designed and built by Dr. Huskey of the National Bureau of Standards at the Institute for Numerical Analysis in

cooperation with the niversity of California, Los geles. According to present plans, an electrostatic memory of about 1000 words will be employed.

A laboratory set-up has been completed to investigate the storage method proposed by Dr. Williams, Manchester University, England, and extensive tests have been made. Overall design of the computer and component research is well underway.

Mark III

According to the present construction schedule, Mark III should be finished some time during the month of June. Since testing will, no doubt, uncover a number of alterations, the completion date is estimated as some time prior to the first of the coming year.

At the IRE National Convention, Dr. Aiken stated that the computer would have the facility for storing 4000 orders (sequencing instructions) on a magnetic drum. As an aid to maintenance, thirty types of basic circuits have been incorporated into plug-in units with color coding for easy identification.

Objectives of the design include (1) reliability, (2) checking, (3) meeting the requirements of the mathematician and (4) simplification of coding.

Whirlwind I

The Whirlwind I arithmetic element and arithmetic control have been installed and operated satisfactorily on all machine orders. Test equipment was used to simulate central control. Timing sequences have been verified at both push button and 2 megacycle pulse rates. The central control is designed and is now being constructed and tested. Storage tubes are operating experimentally and should be installed toward the end of 1949. Plans are now being laid for beginning computer applications research in 1950.