NOVAL 32 KBYTE MEMORY CARD

(ASSEMBLY NO. 860-0042)

WARRANTY

NOVAL 32 KBYTE MEMORY CARD

Three months warranty is to be assumed by the Dealer/ Distributor. NOVAL Inc. will sell memory chips to the warrantor at $5.00 per chip. If the card cannot be repaired by replacing chips, NOVAL Inc. will assume warranty repair responsibilities during the first three months after delivery to the Dealer. For this purpose the card should be mailed back to NOVAL Inc. at NOVAL's expense.

IMPORTANT

The NOVAL 32K memory board as shipped is strapped to occupy the second, third, fourth and fifth 8K blocks of a 64K system (Hex addresses 2000-9FFF). Information on modifying these assignments is included in the manual. Make sure you have the card configured properly before plugging into a system.

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ADVANCE INFORMATION (Preliminary)

The NOVAL 32K memory board provides 32 KBytes of dynamic memory on an S-100 compatible PC board. Principle features include low power operation (typically less than one static 8K memory board), foolproof refresh operation (invisible to 8080 CPU. maintained during wait states, halt, long interrupt responses), and low cost. Every board is factory assembled and tested, and all ICs are socketed for each service. Memory timing is fully synchronous, eliminating adjustments.

JUMPER OPTIONS

The board as shipped from the factory has jumpers in the following positions:

1. E4 to E6. This selects the MK4115-41 8K RAM part. In the event that it is desired to use MK4115-40 parts, the jumper would be removed and a jumper would be connected between E5 and E6. ALL 32 MEMORY PARTS (U1-U32) MUST BE OF THE SAME TYPE (Either -40 or -41).

2. E1 to E3. This derives the memory write signal from the two S-100 signals SOUT (pin 45) and WR (pin 77). Onboard logic inverts both of these signals and NANDS them to provide the memory write strobe, which is routed to the jumper pad E3. Pad E1 is connected to the memory Read/Write line.

2. E1 to E3. (Continued) Pad E2 is the S-100 MWRITE signal. This jumper option is provided because some early S-100 machines put the the gate which derives the MWRITE signal on the front panel. Since not all systems can be guaranteed to have a front panel, it is always safer to derive the memory write signal. Since the derived strobe signal is not fed back into the bus, the E1 to E3 jumper has no detrimental effect on system operation. If you have an overwhelming reason to use the MWRITE strobe directly (pin 68) then change the jumper to E1-E2.

3. B1
B2
B3
B4

These pads (upper right corner of PCB) control the paging of the memory board. Slightly to the right and down from these pads are eight pads labelled 0 through 7. These correspond to the eight possible starting addresses in the system, according to the following table:

Pad	Memory Addresses (Hex)
0	0000-1FFF
1	2000-3FFF
2	4000-5FFF
3	6000-7FFF
4	8000-9FFF
5	A000-BFFF
6	C000-DFFF
7	E000-FFFF

3. (Continued)

The B1-B4 pads select banks 1 through 4 of the memory array, each bank being 8K of memory. B1 corresponds to U1 thru U8; B2 is U9 - U16; B3 is U17 - U24; B4 is U25 - U32. As shipped from the factory, the board is strapped to occupy the 32K from 2000 to 9FFF (HEX). To disable any 8K bank, it is only necessary to remove the appropriate "B" jumper. This electrically removes an 8K bank from the system, so if desired an 8K bank may be disabled without physically removing the RAM parts from their sockets.

The above information indicates that the memory board is actually four independent memory sections, each section being strappable to any 8K boundary. An example will clarify this point. Suppose your system has RAM at 0000-1FFF, and at 8000-BFFF. To fill the 8K gaps from 2000 through 7FFF, connect one B jumper to "1", another to "2", and another to "3". This implements 24K from 2000 through 7FFF. The remaining 8K can be unused (the remaining B jumper unconnected), or strapped for a higher 8K block (above BFFF).

Notice that the B numbers are arbitrary. It makes no difference in the above example which B pads (1-4) are used for each jumper.

Also, removing the B jumper for any 8K bank disables the S-100 bus drivers for that bank, so a plugged-in but disabled bank of 8 RAMS does not interfere with proper bus operation.

SYSTEM COMPATIBILITY

The NOVAL RAM card should run in any 2 MHz S-100 system. Proper operation of the card depends on the following bus signals:

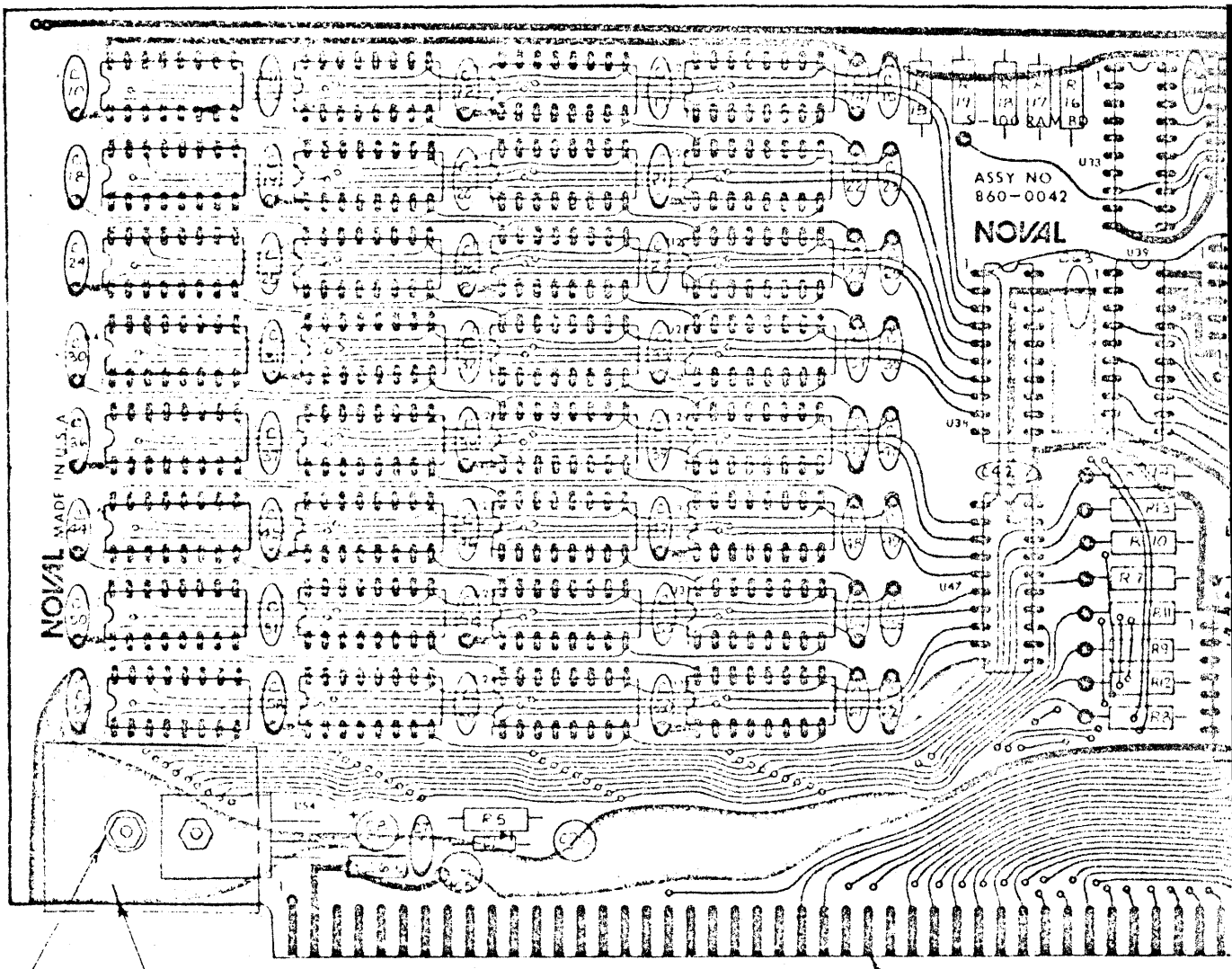
- ø1 (pin 25)
- ø2 (pin 24)
- PSYNC (pin 76)
- SOUT (pin 45)
- WR' (pin 77)
- MEMR (pin 47)
- Data input bus (8 lines)
- Data output bus (8 lines)
- Address bus (16 lines).

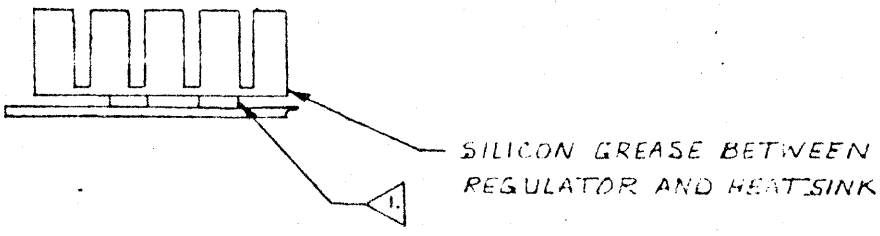
Any CPU card which uses the 8224 clock generator for timing generation should work without a hitch. Also, any CPU card which derives its own 8080 timing (which must meet the 8080 spec), will work. A possible exception in compatibility is an S-100 CPU card which uses a processor other than the 8080 (or 8080A).

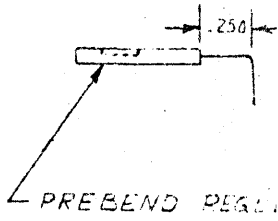
The reason for this is that the S-100 bus is defined for specific 8080 signals, and any other processor design must emulate these signals to insure S-100 compatibility. To take a specific example, the Z80 CPU has no sync signal, uses a single phase

SYSTEM COMPATIBILITY (Continued)

clock, and times its input and output operations slightly differently from the 8080. The degree of compatibility with the NOVAL memory board depends on the accuracy with which the Z80 CPU board designer synthesized the 8080 control signals (specifically ø1, ø2 and SYNC) to feed to the bus.

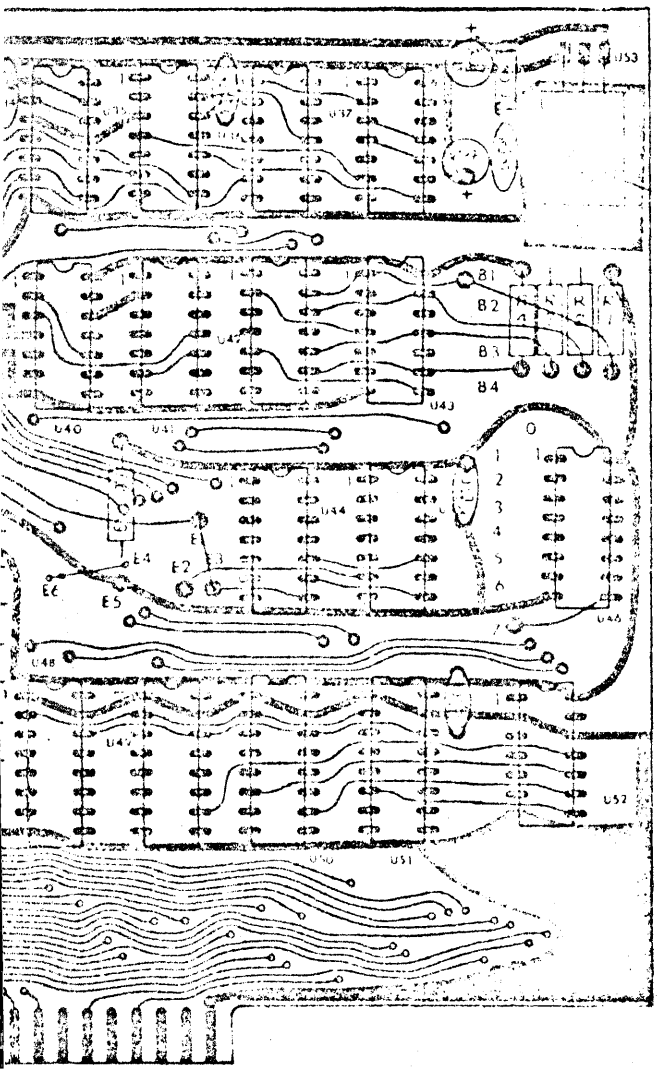






1. INSTALL INSULATED JUMPERS AT E4-E6 AND E1-E3
2. NO. 4 WASHER (2) BETWEEN BOARD AND ITEM 33

NOTES: UNLESS OTHERWISE SPECIFIED



4-40 SCREW TYP. 3 PLS.
4-40 NUT TYP. 3 PLS.
SILICON GREASE BETWEEN
BOARD AND REGULATOR

SEE DETACHED PARTS LIST

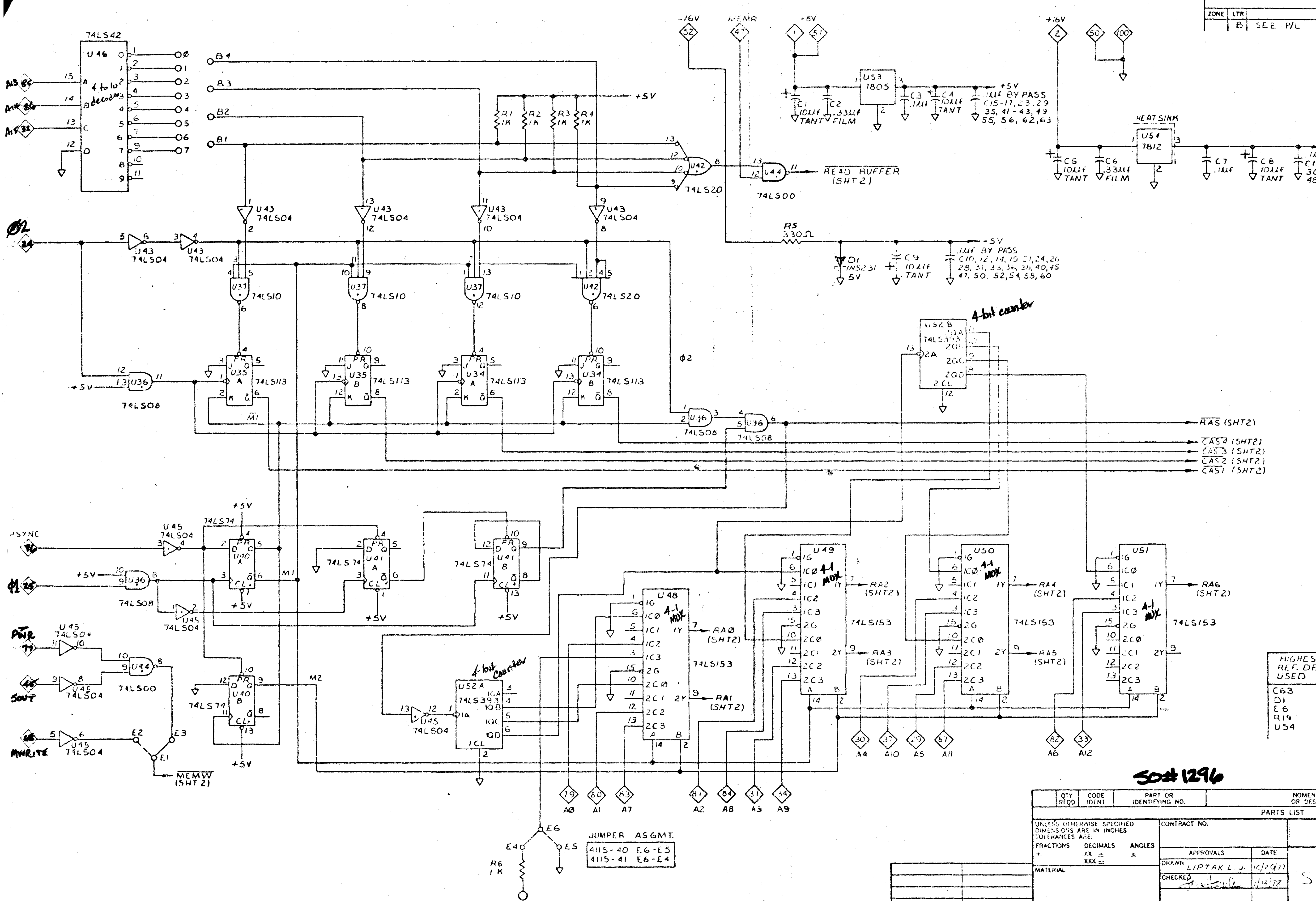
...ULATORS

NOVAL San Diego, Calif.

ASSEMBLY
S-100 RAM BOARD

D 810-0042

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
	B	SEE P/L	



SO# 1296

INTEGRATED CIRCUITS				
REF. DES.	PART NO	VCC	GND	UNUSED
U44	74LS00	[illegible]	7	[illegible]
U43, 45	74LS04	[illegible]	7	
U36	74LS08	[illegible]	7	
U37	74LS10	[illegible]	7	
U42	74LS20	[illegible]	7	8
U46	74LS42	[illegible]	[illegible]	
U40, 41	74LS74	[illegible]	7	
U34, 35	74LS113	4	7	
U48 - U51	74LS153	[illegible]	[illegible]	
U33, 38, 39, 47	74LS244	[illegible]	[illegible]	
U52	74LS393	4	7	
U1 - 32	MK4115-41	SEE CKTS		

HIGHEST REF. DES. USED
C63
D1
E6
R19
U54

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

CONTRACT NO.

APPROVALS	DATE
DRAWN LIPTAK L. J.	11/29/77
CHECKED [signature]	1/13/78

NOVAL San Diego, California

SCHEMATIC S-100 RAM BOARD

SIZE D | CODE IDENT NO | DRAWING NO. 860-0042

SCALE NONE | SHEET 1 OF 1

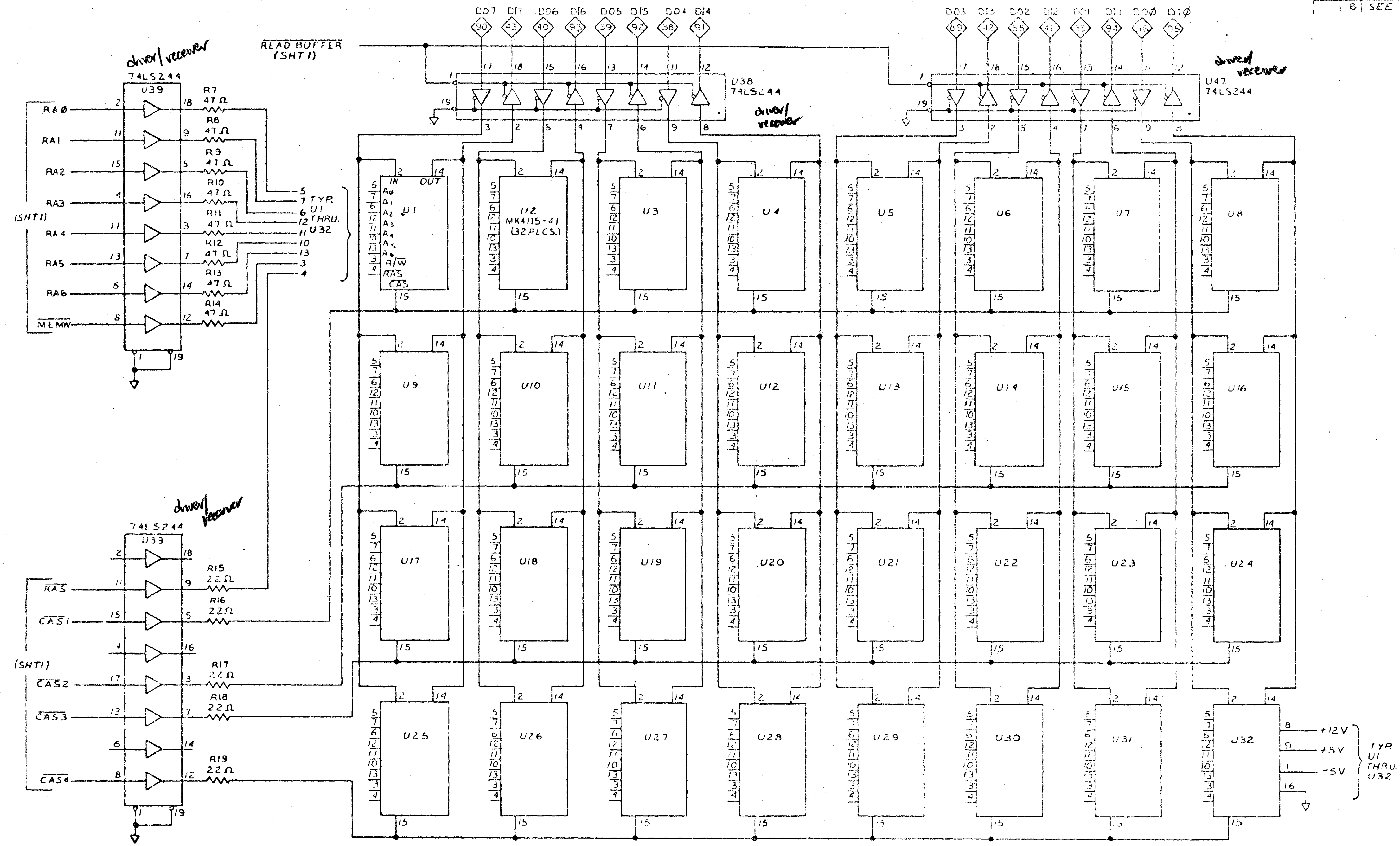
NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS 1/2W 5%
2. CAPACITANCE VALUES ARE IN MICROFARADS

Revisions: B SEE P/L



Soc# 1296

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES

CONTRACT NO.

MATERIAL

FINISH

DRAWN LIPTAK

CHECKED

NEXT ASSY / USED ON / APPLICATION

DO NOT SCALE DRAWING

NOVAL San Diego, California

SCHEMATIC S-100 RAM BOARD

SIZE D CODE IDENT NO. DRAWING NO. 860-0042

SCALE NONE

NOTES: UNLESS OTHERWISE SPECIFIED