

NP37 A02

LOGIC DIAGRAM

MACHINE LIST FOR NP37-A02

SER NO- 0141 MACHINE REV-
 OPTION- NONE, SSW HDA- FRT, TFH, NONE
 CTRY- CUST-

PAGE NO	FIG NO	SHEET REV	PARTS NO	PCB REVISION		TITLE	REMARKS
				(ACTUAL)	(LOL)		
0 -		0				GUIDANCE OF LOGIC DIA	
CZ-1	NC-21441	1				DC PWR-CTRL B/B INTERFACE	
-2,3	"	1		-		RELAY BOX	
-4	"	1		-		DC PWR SUPPLY A	
-5	"	1	NP441	B		OP PANEL	
CX-1 - 8	NC-21445	0		-		CTRL INTERFACE	
CU-1 - 4	NC-29430	0	NP430	B		CTLI-1B	SSW only
CT-1 - 5	NC-29431	0	NP431	C		CTLI-2B	SSW only
CR-1 - 4	NC-28430	0	NP430	B		CTLI-1A	
CQ-1 - 5	NC-28431	0	NP431	C		CTLI-2A	
CN-1 - 5	NC-28432	0	NP432	B		MPU-1	
CM-1 - 5	NC-28433	0	NP433	A		MPU-2	
CL-1 - 4	NC-28434	0	NP434	A		MPU-3	
CL-1 - 4	NC-28484	0	NP484			X CALL	
CJ-1 - 4	NC-28435	0	NP435	B		DEVI	
CH-1 - 5	NC-28436	0	NP436	B		REG	
CG-1 - 7	NC-28437	0	NP437	B		ECC	
CF-1 - 5	NC-28438	0	NP438	A		SERDES-1	
CE-1 - 5	NC-28439	0	NP439	C		SERDES-2	
CD-1 - 5	NC-28440	1	NP440	D		VFO	
CC-1 - 5	NC-28481	0	NP481	A		XCALL-2	
CB-1 - 5	NC-28479	0	NP479	A		XCALL-1	
CA-1,2	NC-21446	0				DEVICE INTERFACE	
Z-1,2		2				DC PWR SUPPLY B	
-3,4	NC-20408	2	NP408	C		POWER AMP	
-5	NC-20419	0	NP419	A		OP PANEL	
-6 - 9		0				HDA INTERFACE A,B	
X-1 - 3		0				DRIVE INTERFACE	
A-1 - 9	NC-21410	4	NP410	F		INTERFACE	
A-1 - 10	NC-20460	3	NP460	C		INTERFACE - A	XCL only
B-1 - 6	NC-20469	3	NP469	C		INTERFACE - C	XCL only
C-1 - 6	NC-20411	6	NP411	E		HAR/CAR A	
D-1 - 10	NC-22462	1	NP462	G		SRV VEL A	
E-1 - 7	NC-20463	2	NP463	B		SRV POS A	
F-1 - 6	NC-22414	2	NP414	H		R/W CTRL A	
J-1 - 9	NC-20425/	11	NP425/	K		RD DTCT	

PAGE NO	FIG NO	SHEET REV	PARTS NO	PCB REVISION		TITLE	REMARKS
				(ACTUAL)	(LOL)		
K-1 - 6	NC-23414	2	NP414	H		R/W CTRL B	
L-1 - 7	NC-21463	2	NP463	B		SRV POS B	
M-1 - 10	NC-23462	1	NP462	G		SRV VEL B	
N-1 - 6	NC-21411	6	NP411	E		HAR/CAR B	

REV No.	DATE	DRAWN	APPD

GUIDANCE OF LOGIC DIAGRAM.

(1) PACKAGE LOCATION.

CONTROL BACK BOARD PACKAGE LOCATION

CX CW CV CU CT CS CR CQ CP CN CM CL CK CJ CH CG CF CE CD CC CB CA

NP445 (CTL-1A)	NP445 (CTL-1B) ^{SSW only}
NP430 (CTLI-1B)	SSW only
NP431 (CTLI-2B)	SSW only
NP430 (CTLI-1A)	
NP431 (CTLI-2A)	
NP432 (MPU-1)	
NP433 (MPU-2)	
NP434 (MPU-3)	J203
NP435 (DEV)	
NP436 (REG)	J202
NP437 (ECC)	
NP438 (SERDES-1)	
NP439 (SERDES-2)	
NP440 (VFO)	
NP446 (DEV-1)	

O1

O2

NPL-NM-31028

DRIVE BACK BOARD PACKAGE LOCATION

N M L K J H G F E D C B A

NP411 (HAR/CAR B)	
NP462 (SRV VEL B)	
NP463 (SRV POS B)	
NP414 (R/W CTRL B)	
NP425 (RD DTCT)	
HDA B	HDA A
NP414 (R/W CTRL A)	
NP463 (SRV POS A)	
NP462 (SRV VEL A)	
NP411 (HAR/CAR A)	
NP469 (INTERFACE C)	XCALL only J307
NP 410 (INTERFACE)	(for BASIC)
NP 460 (INTERFACE A)	(for XCALL)
	J311 J303
	J312 J304

O1

O2

NPL-NM-31177 REV.0

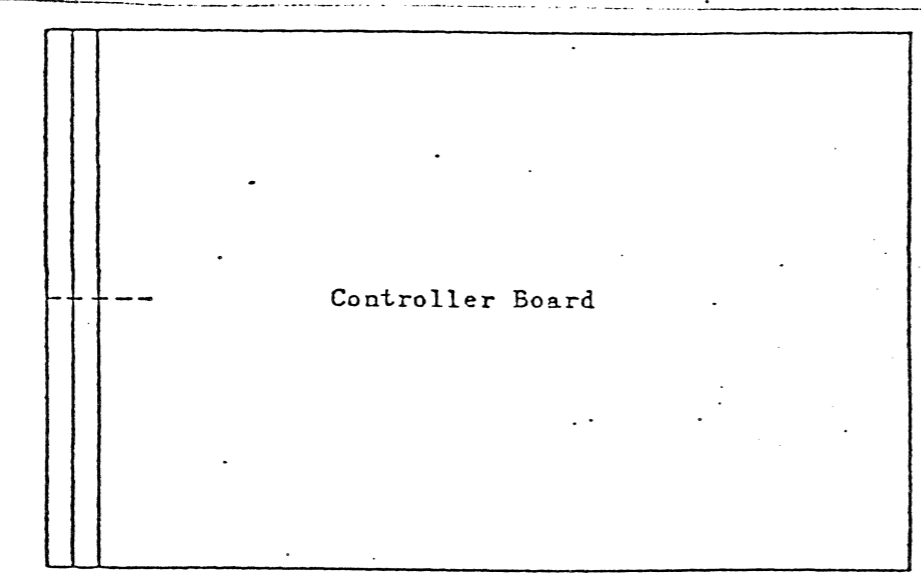
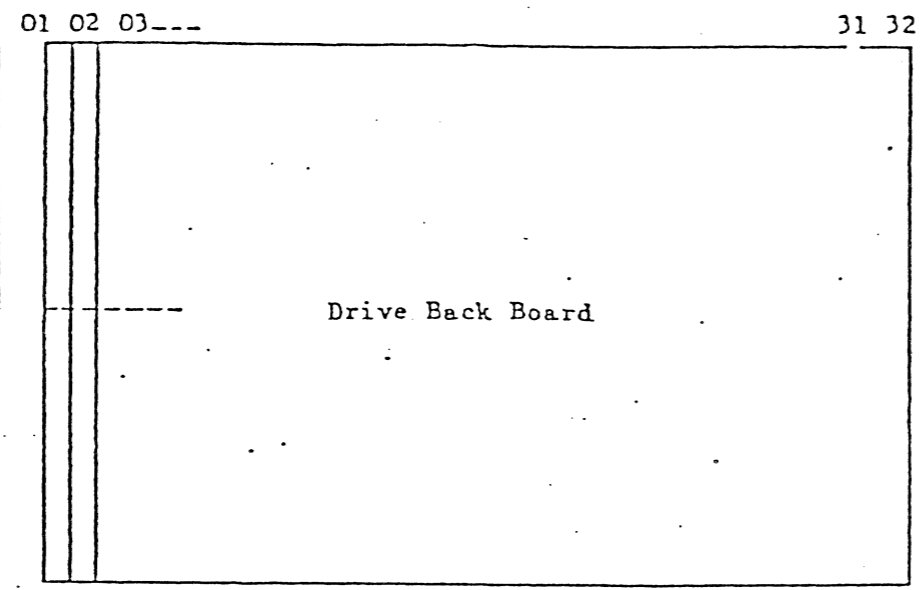
Notes:

- (1) The upper diagram shows the drive back board and the lower diagram shows the controller back board, both viewed from the package insertion side.
- (2) The card mounted in A and B positions indicates the twin size card while the card mounted in either A or B position indicates the single size card.
- (3) In these diagrams NP XXX "package" denotes package name, and the card with letters "EDGE" shows the edge card of each interface.

P/N REV	TITLE GUIDANCE OF LOGIC DIAGRAM	SHEET 1 / 4	DRAWN	
		REV 0	CHECK	
	DRAWING NO		APPD	
			Nippon Peripherals Limited	

REV No.	DATE	DRAWN	APPD

(2) Back Board Card Pin Location



This diagram is viewed from the wiring side.

Single card Twin card
 ↓ ↓
 01 02

CARD PIN LOCATION
 SINGLE CARD TWIN CARD

01	02	101	102
03	04	103	104
05	06	105	106
07	08	107	108
09	10	109	110
11	12	111	112
13	14	113	114
15	16	115	116
17	18	117	118
19	20	119	120
21	22	121	122
23	24	123	124
25	26	125	126
27	28	127	128
29	30	129	130
31	32	131	132
33	34	133	134
35	36	135	136
37	38	137	138
39	40	139	140
41	42	141	142
43	44	143	144
45	46	145	146
47	48	147	148
49	50	149	150
51	52	151	152
53	54	153	154
55	56	155	156
57	58	157	158
59	60	159	160
61	62	161	162
63	64	163	164
65	66	165	166
67	68	167	168

01	02	201	202
03	04	203	204
05	06	205	206
07	08	207	208
09	10	209	210
11	12	211	212
13	14	213	214
15	16	215	216
17	18	217	218
19	20	219	220
21	22	221	222
23	24	223	224
25	26	225	226
27	28	227	228
29	30	229	230
31	32	231	232
33	34	233	234
35	36	235	236
37	38	237	238
39	40	239	240
41	42	241	242
43	44	243	244
45	46	245	246
47	48	247	248
49	50	249	250
51	52	251	252
53	54	253	254
55	56	255	256
57	58	257	258
59	60	259	260
61	62	261	262
63	64	263	264
65	66	265	266
67	68	267	268

Note:

- (1) The number of signal pins is 68 in a single card and 136 in a twin card. Of these pins 24 pins are used for power supply (+5V, GND) and the special power supply pin is assigned among 112 effective signal pins.

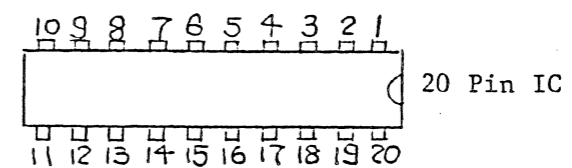
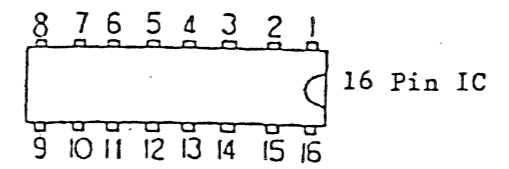
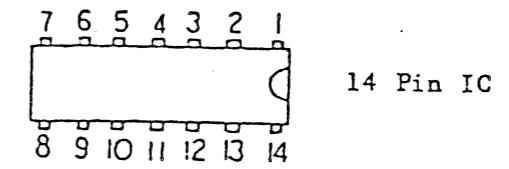
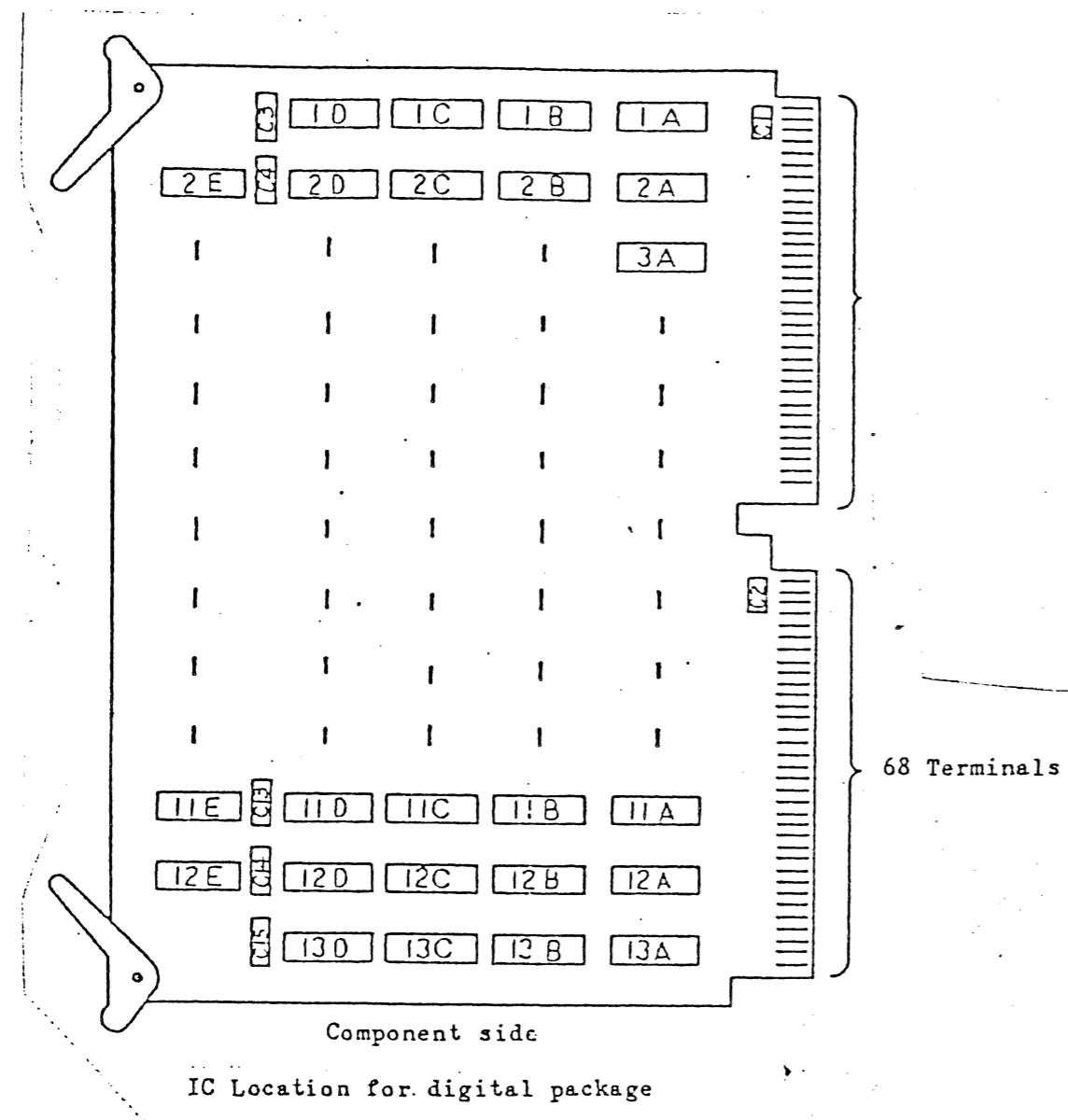
P/N REV	TITLE	SHEET 2 / 4	DRAWN	
	GUIDANCE OF LOGIC DIA	REV	CHECK	
	DRAWING NO	Nippon Peripherals Limited		

REV No.	DATE	DRAWN	APPD

(3) IC Location

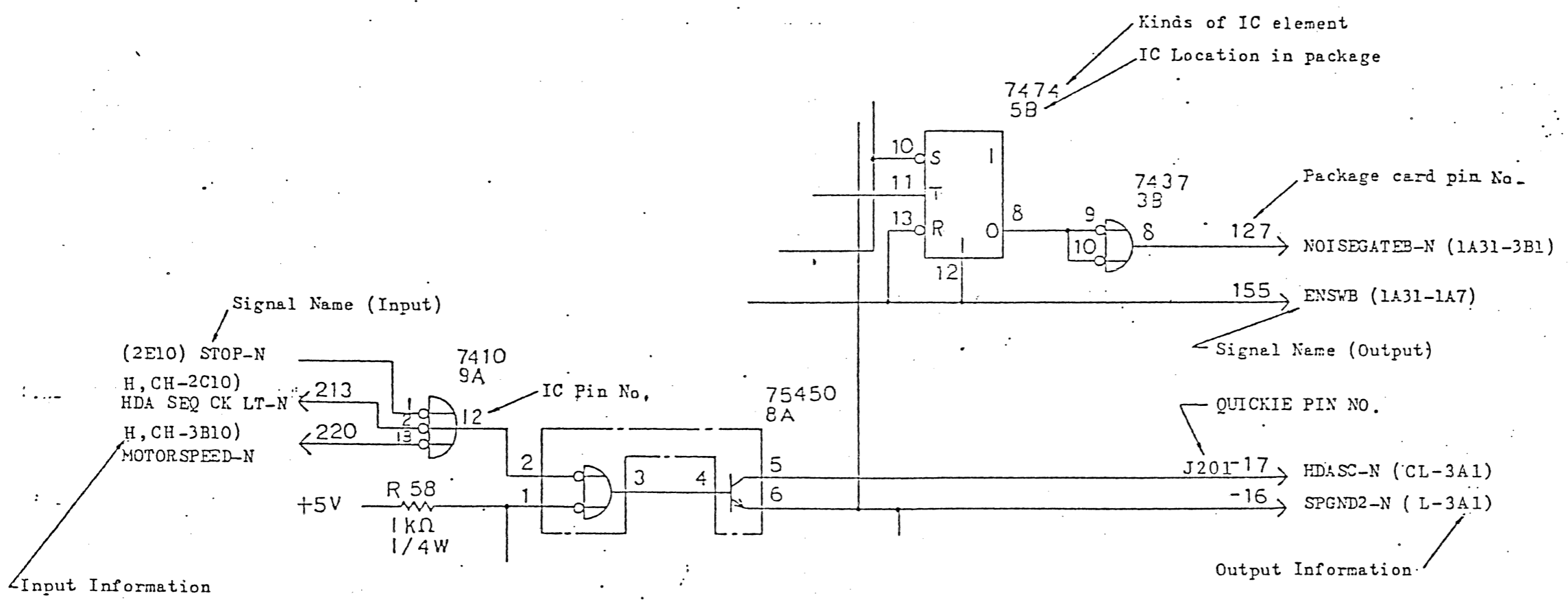
Note:

- (1) The IC location applies to digital packages.
- (2) Numbering of DIL Type IC Pins is as follows. (Top View)



P/N REV	TITLE GUIDANCE OF LOGIC DIA	SHEET 3 / 4	DRAWN	
		REV	CHECK	
	DRAWING NO		APPD	
			Nippon Peripherals Limited	

(4) Guidance of Logic Dia



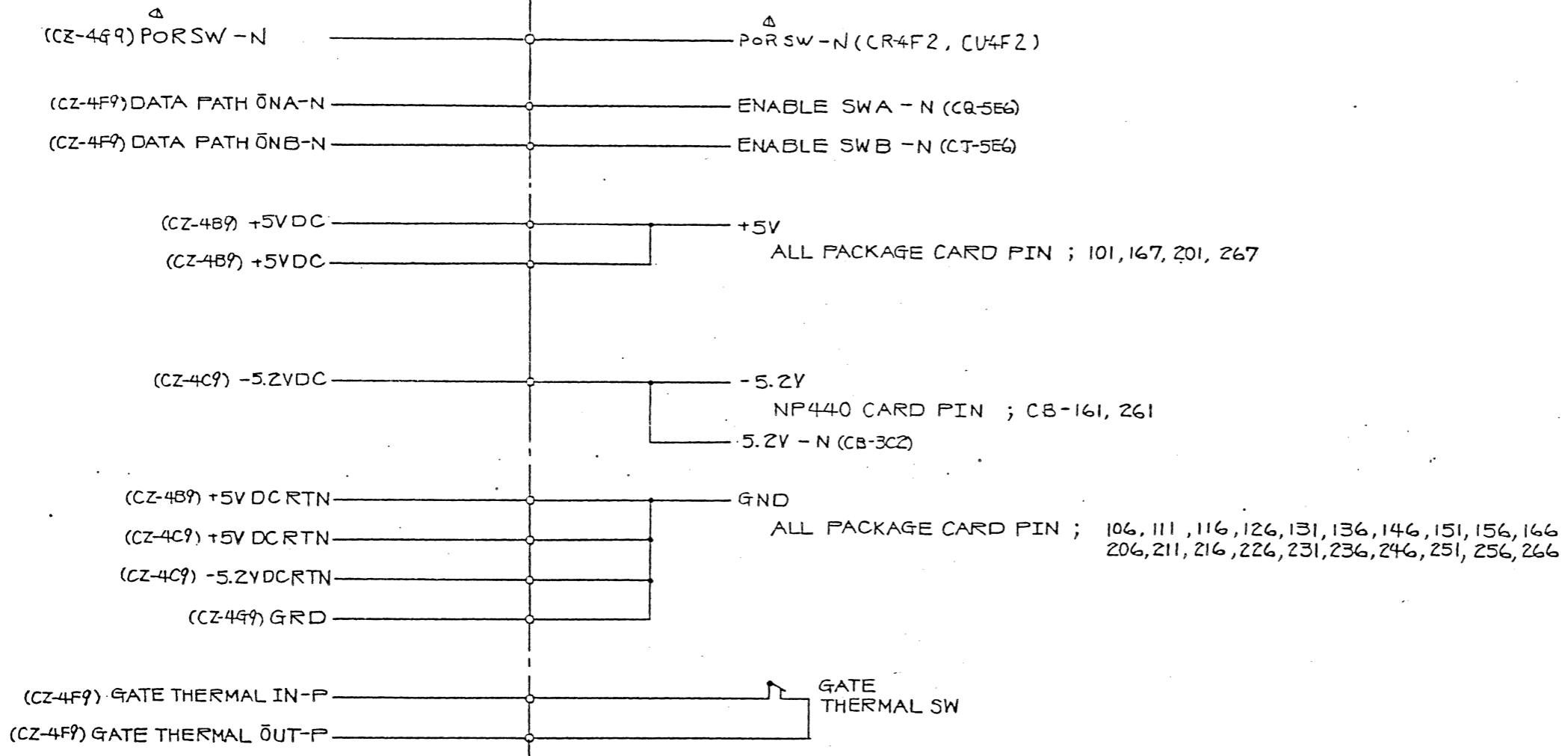
H, CH: Package Location and Source Gate Page No. in Logic Dia.
 3B10: Source Gate Location

L-3, CE-3: Cable Connection Dia Page No.
 A1: Sink Terminal Location

P/N REV	TITLE	SHEET 4 / 4	DRAWN
	GUIDANCE OF LOGIC DIA	REV 0	CHECK APPD
DRAWING NO		Nippon Peripherals Limited	

D.C. POWER SUPPLY

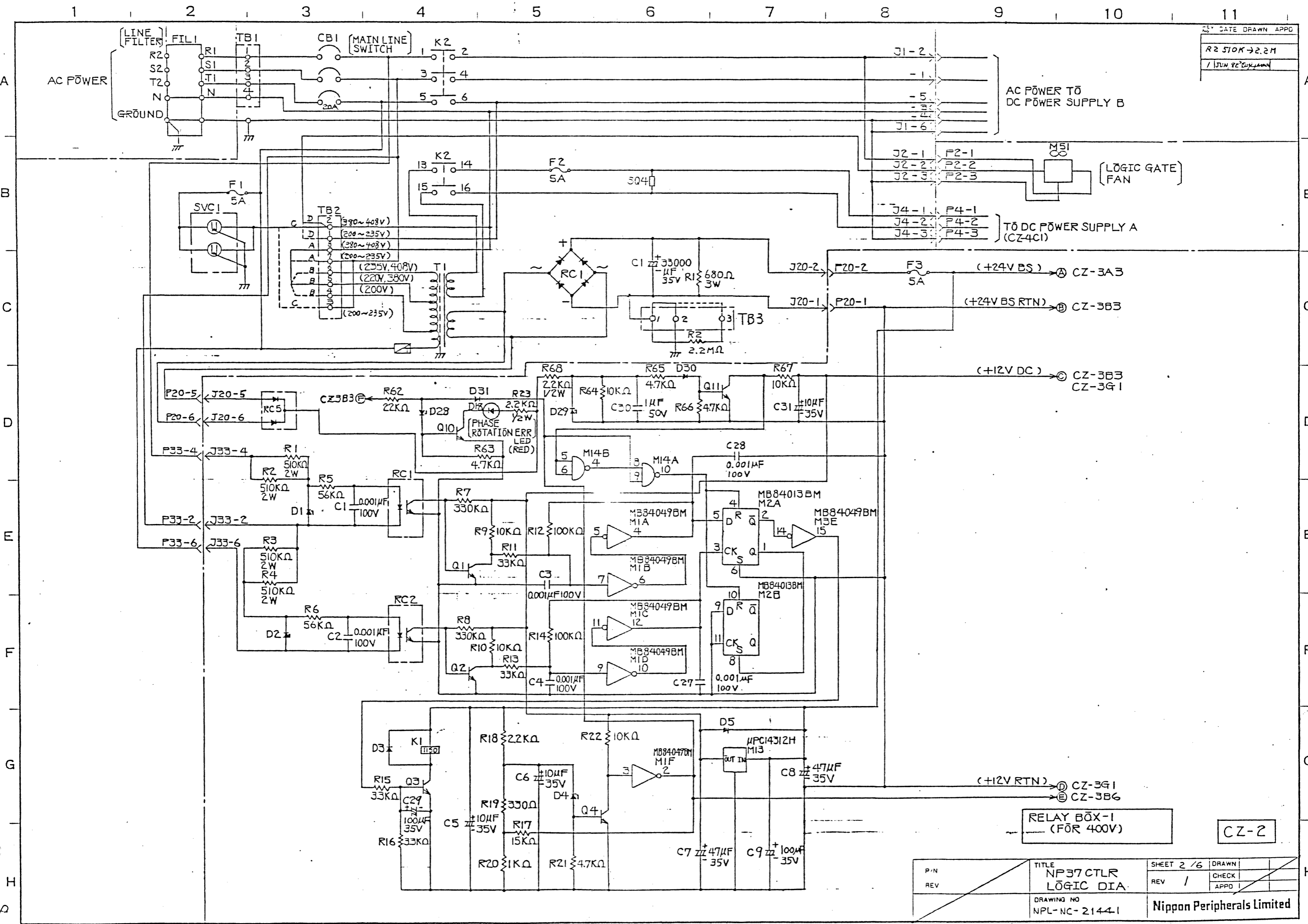
CONTROLLER BACK BOARD



D.C. POWER SUPPLY-CTLR
 BACK BOARD INTERFACE

CZ-1

P/N REV	TITLE NP377 CTLR LOGIC DIA	SHEET 1 / 6	DRAWN A.D.G. 82.2.2
	DRAWING NO NPL-NC-21441	REV	CHECK A.O.G. 82.2.2 APPD K.J.M. 82.6.15
Nippon Peripherals Limited			

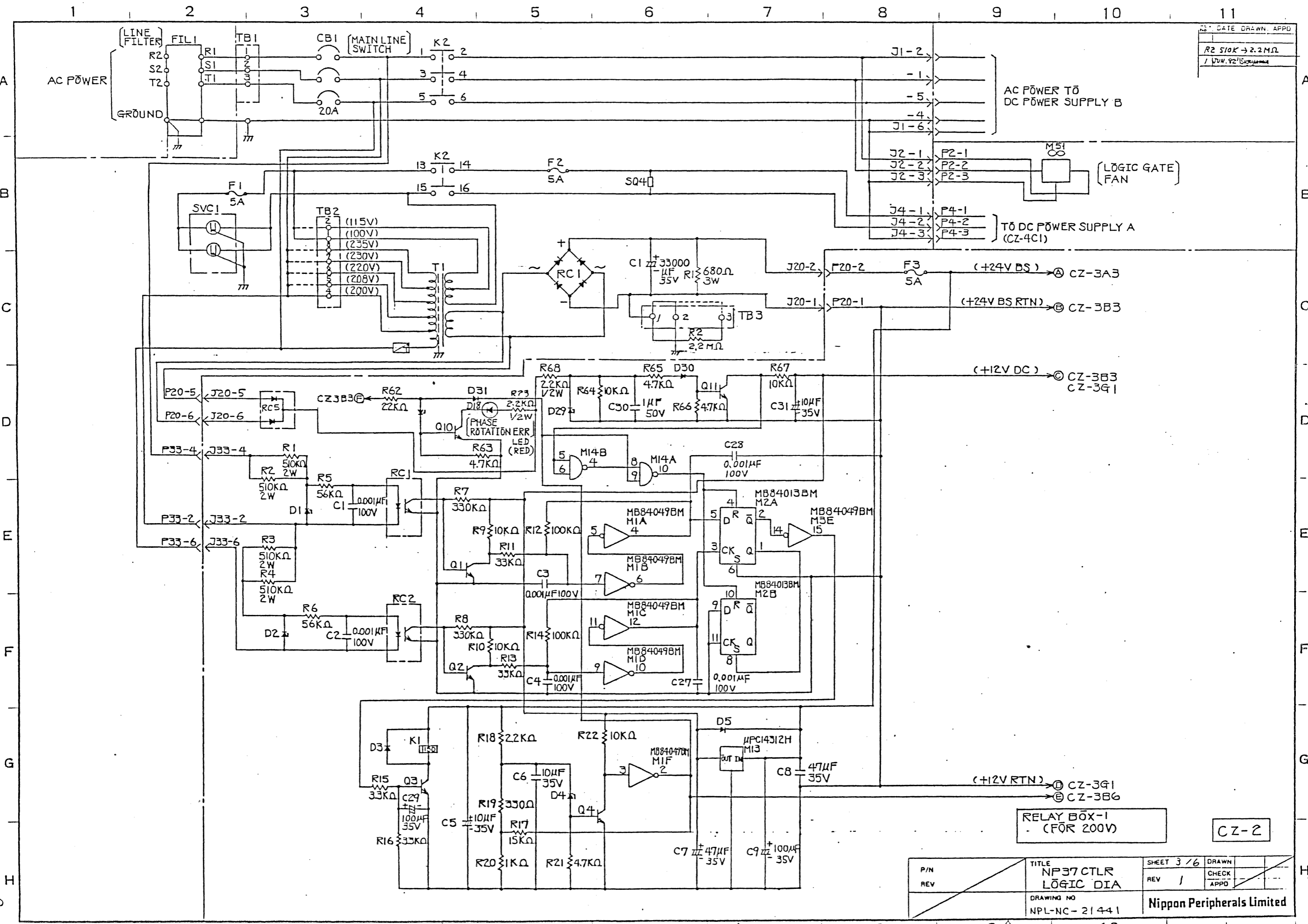


REV DATE DRAWN APPD
 R2 510K → 2.2M
 1 JUN 92 S. KAWANO

RELAY BOX-1
 (FOR 400V)

CZ-2

P/N	TITLE	SHEET 2 / 6	DRAWN
REV	NP37 CTRL LOGIC DIA.	REV 1	CHECK
	DRAWING NO		APPD
	NPL-NC-2144-1		
		Nippon Peripherals Limited	



DATE DRAWN. APPD
 R2 510K -> 2.2MΩ
 1/20/74. P2/15/15/15/15

AC POWER TO
 DC POWER SUPPLY B

(LOGIC GATE)
 FAN

TO DC POWER SUPPLY A
 (CZ-4C1)

(+24V DS) -> CZ-3A3

(+24V BS RTN) -> CZ-3B3

(+12V DC) -> CZ-3B3
 CZ-3G1

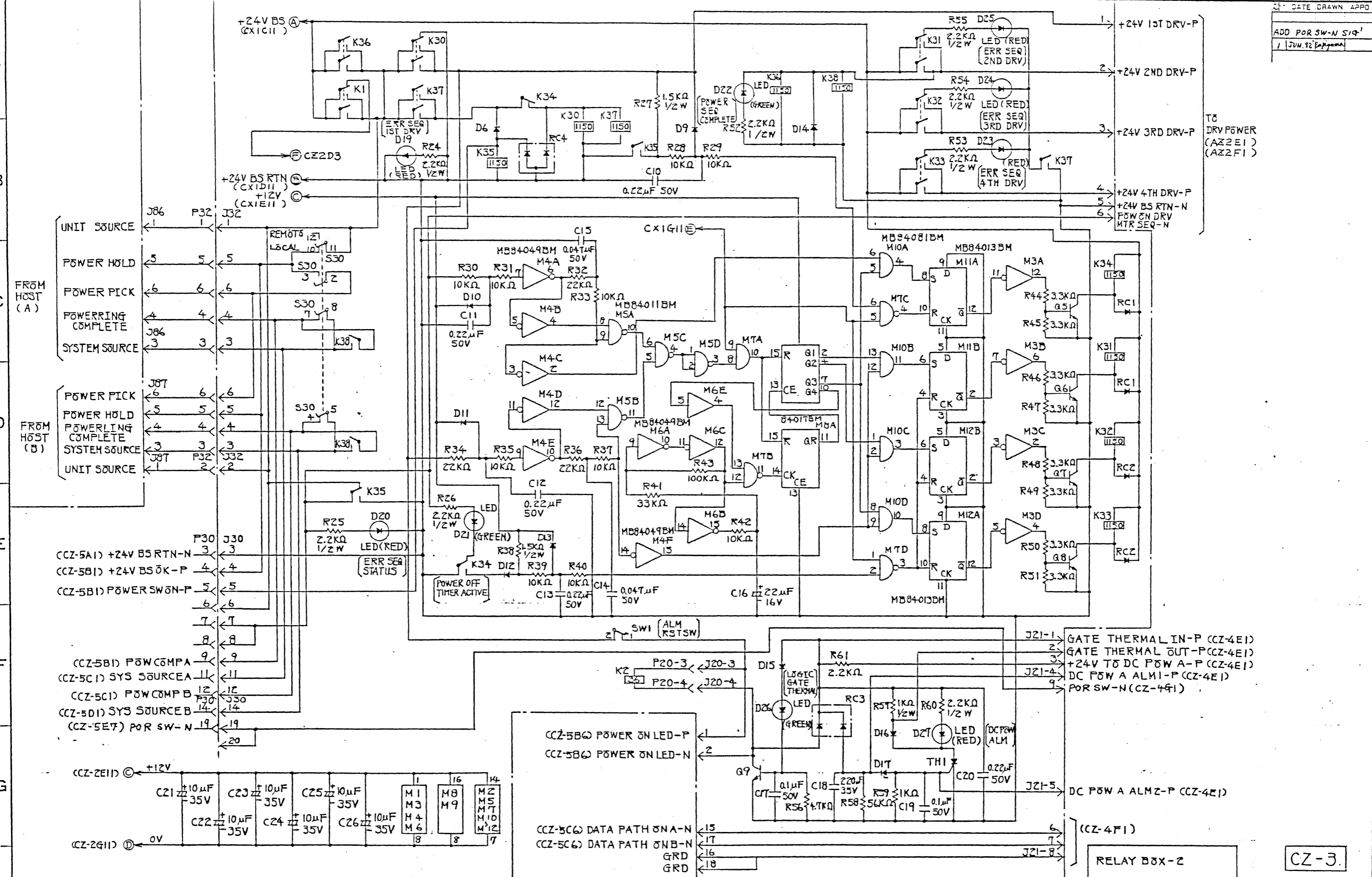
(+12V RTN) -> CZ-3G1
 CZ-3B6

RELAY BOX-1
 (FOR 200V)

CZ-2

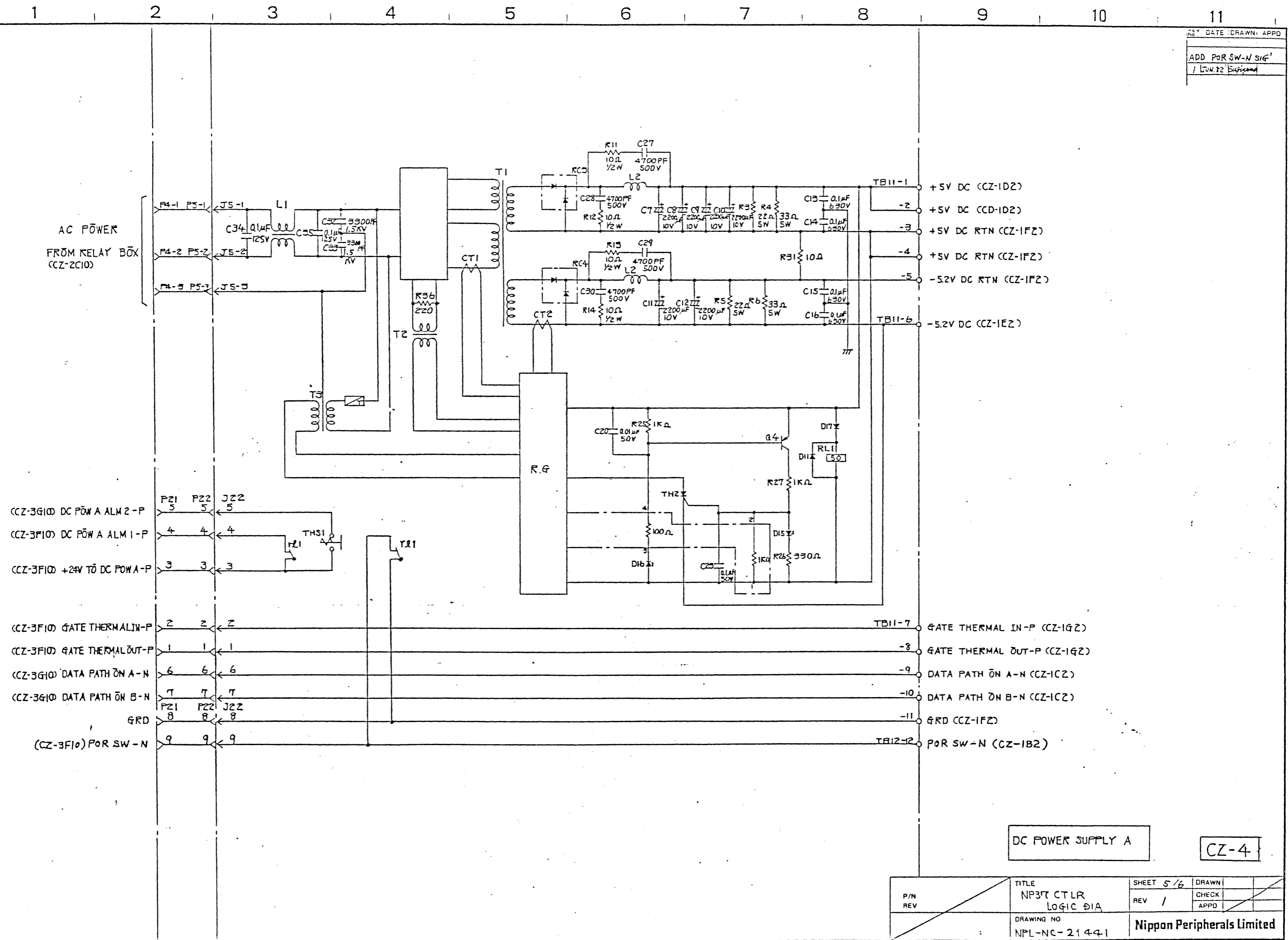
P/N	REV	TITLE	SHEET	DRAWN
		NP37 CTRL LOGIC DIA	3 / 6	
		DRAWING NO	REV	CHECK
		NPL-NC-21441	1	APPO
Nippon Peripherals Limited				

DATE DRAWN APPD
 ADD FOR SW-N SIG
 1 JUN 82 [Signature]



P/N	REV	TITLE	SHEET	DRAWN
		NP37 CTLR	4/6	
		LOGIC DIA	REV	CHECK
			1	APPD
DRAWING NO		Nippon Peripherals Limited		
NPL-NC-21441				

REV DATE DRAWN APPD
 ADD POR SW-N SIG'
 / LUN 12 *Signature*



AC POWER
 FROM RELAY BOX
 (CCZ-2C10)

CCZ-3G10 DC POW A ALM 2-P
 CCZ-3F10 DC POW A ALM 1-P
 CCZ-3F10 +24V TO DC POW A-P
 CCZ-3F10 GATE THERMAL IN-P
 CCZ-3F10 GATE THERMAL OUT-P
 CCZ-3G10 DATA PATH ON A-N
 CCZ-3G10 DATA PATH ON B-N
 GRD
 (CCZ-3F10) POR SW-N

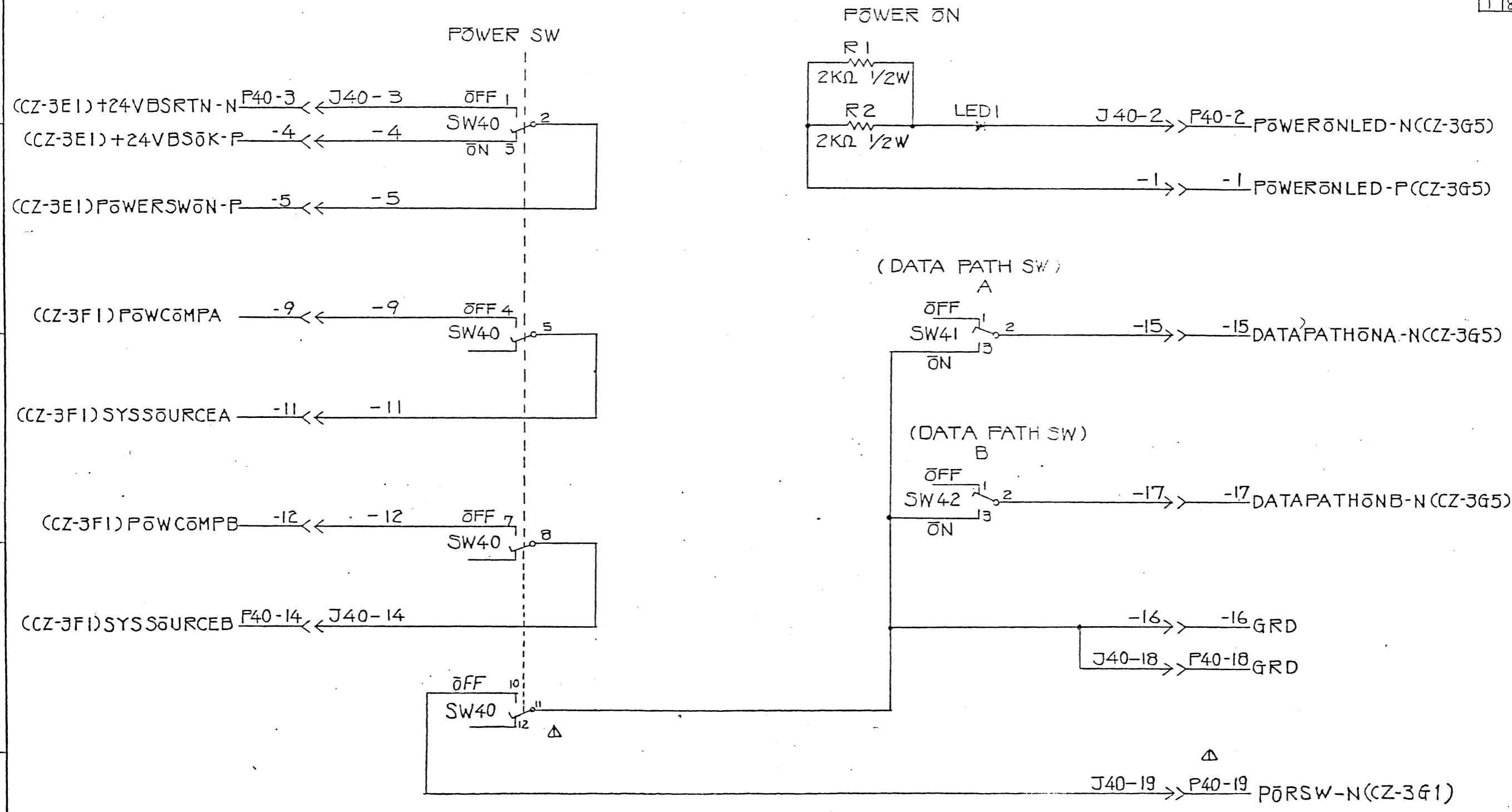
TB11-1 +5V DC (CZ-1D2)
 -2 +5V DC (CD-1D2)
 -3 +5V DC RTN (CZ-1F2)
 -4 +5V DC RTN (CZ-1F2)
 -5 -5.2V DC RTN (CZ-1F2)
 TB11-6 -5.2V DC (CZ-1E2)
 TB11-7 GATE THERMAL IN-P (CZ-1G2)
 -8 GATE THERMAL OUT-P (CZ-1G2)
 -9 DATA PATH ON A-N (CZ-1C2)
 -10 DATA PATH ON B-N (CZ-1C2)
 -11 GRD (CZ-1F2)
 TB12-1 POR SW-N (CZ-1B2)

DC POWER SUPPLY A

CZ-4

P/N REV	TITLE NP37 CTLR LOGIC DIA	SHEET 5/6	DRAWN
	DRAWING NO NPL-NC-21441	REV 1	CHECK APPO
Nippon Peripherals Limited			

REV No.	DATE	DRAWN	APPD
Addition			
PORSW - N			
1	82.5.8	Haruta	



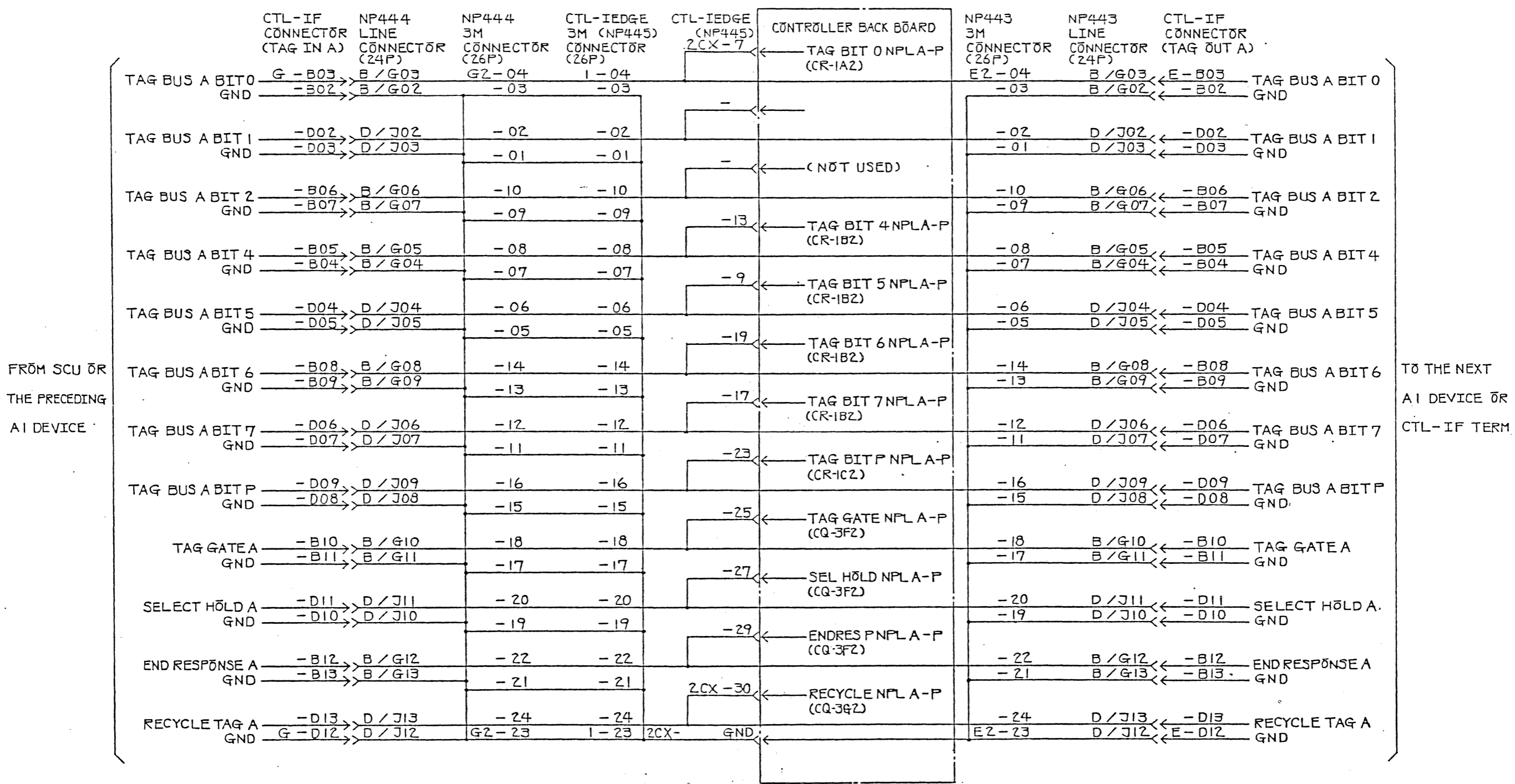
NP441 (CTRL OPERATOR PANEL)

CZ-5

P/N REV	TITLE NP37 CTRL LOGIC DIA	SHEET 6/6	DRAWN	
		REV 1	CHECK	
DRAWING NO NPL-NC-21441		Nippon Peripherals Limited		

A
B
C
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H

A
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H

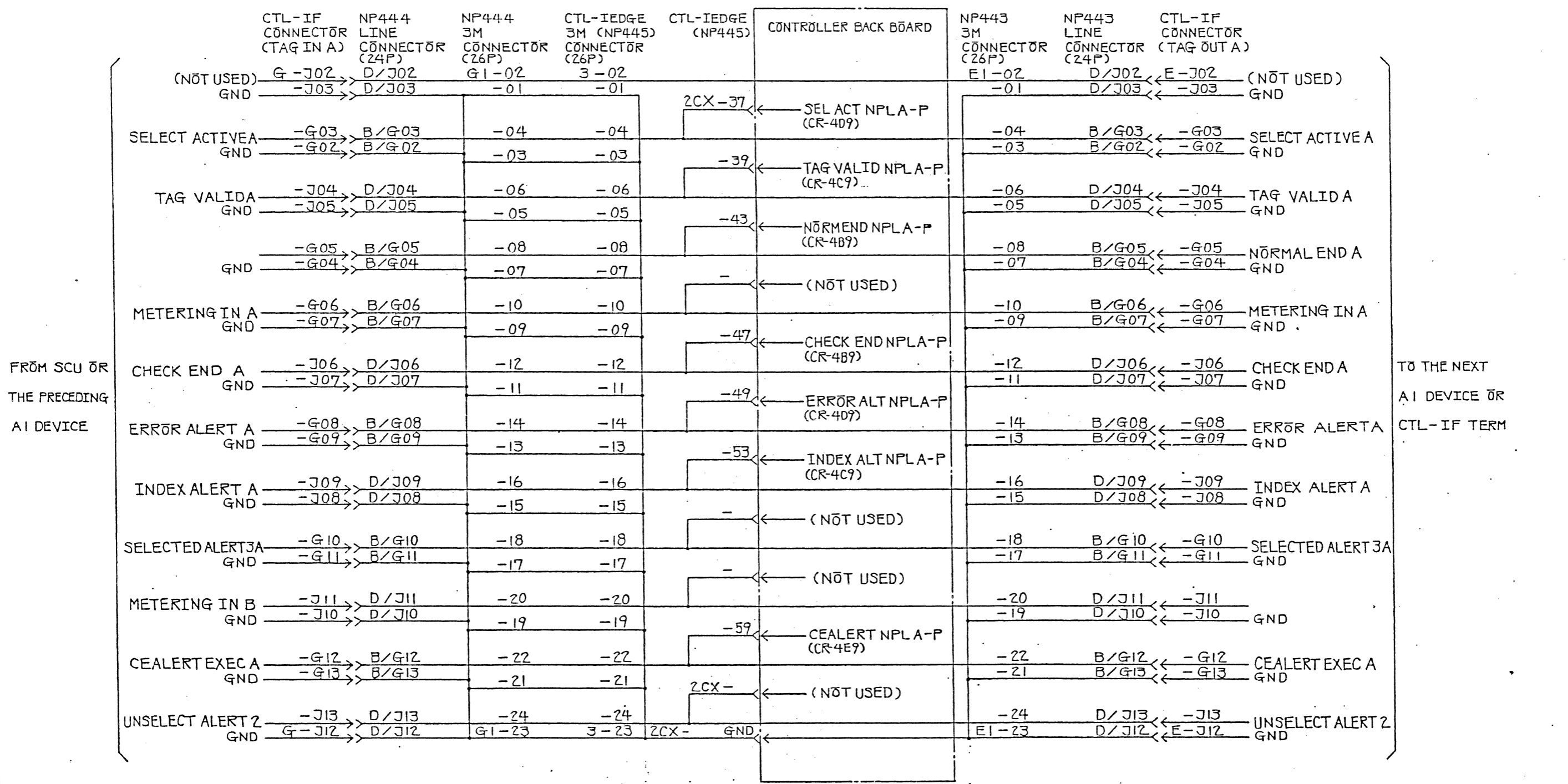


FROM SCU OR THE PRECEDING AI DEVICE

TO THE NEXT AI DEVICE OR CTL-IF TERM

(CTL INTERFACE A1) CX-1

P/M	TITLE	SHEET 1 / 8	DRAWN A0610182.2.2
REV	NP37 CTLR LOGIC DIA	REV 0	CHECK APPD
CTL INTERFACE		DRAWING NO NPL-NC-21445	Nippon Peripherals Limited

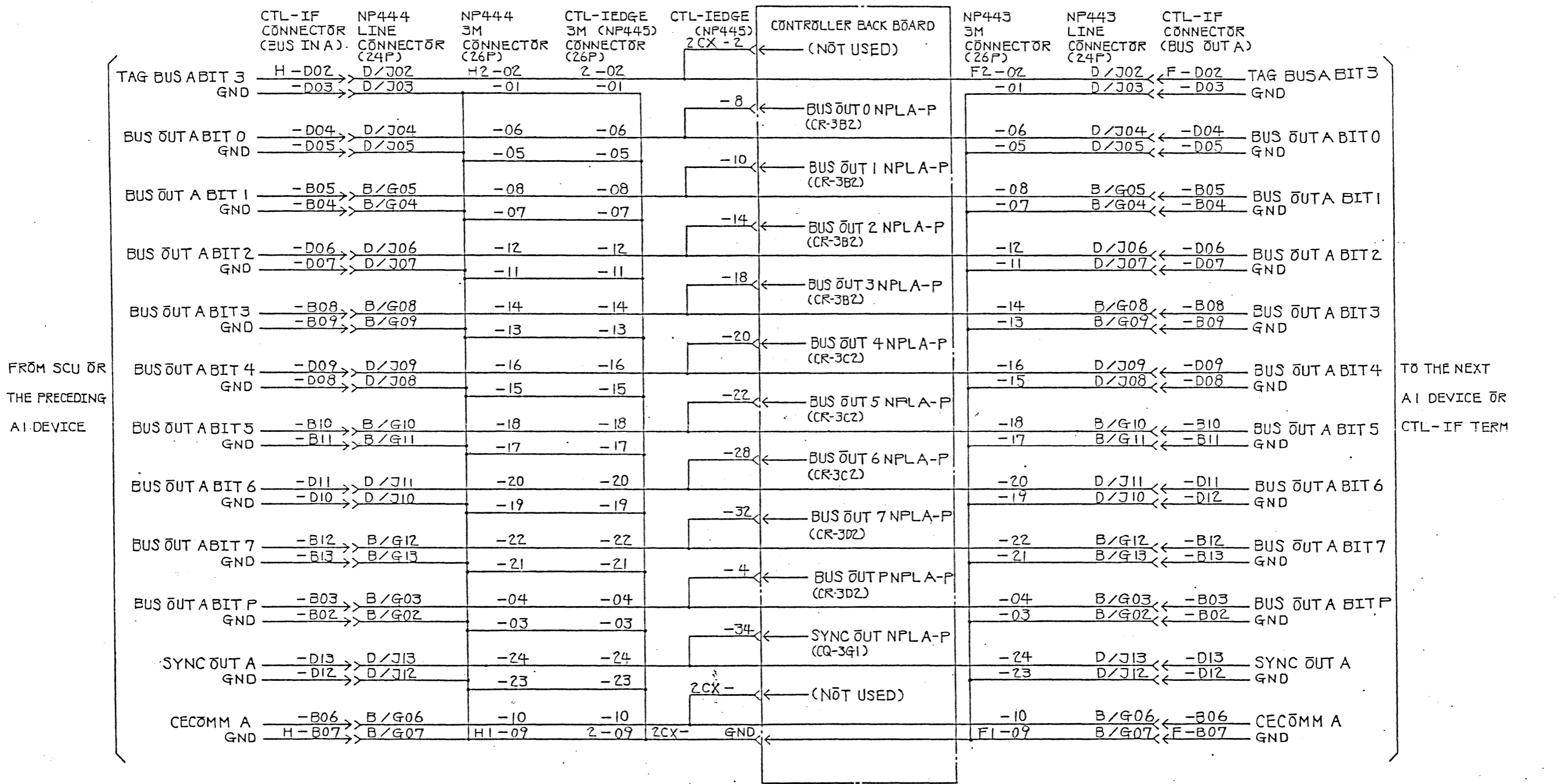


FRÖM SCU ÖR
THE PRECEDING
AI DEVICE

TÖ THE NEXT
AI DEVICE ÖR
CTL-IF TERM

(CTL INTERFACE A2) CX-2

P/N	TITLE	SHEET 2 / 8	DRAWN
REV	NP37 CTLR LOGIC DIA	REV 0	CHECK
	DRAWING NO		APPD
	NPL-NC-21445	Nippon Peripherals Limited	



FROM SCU OR THE PRECEDING AI DEVICE

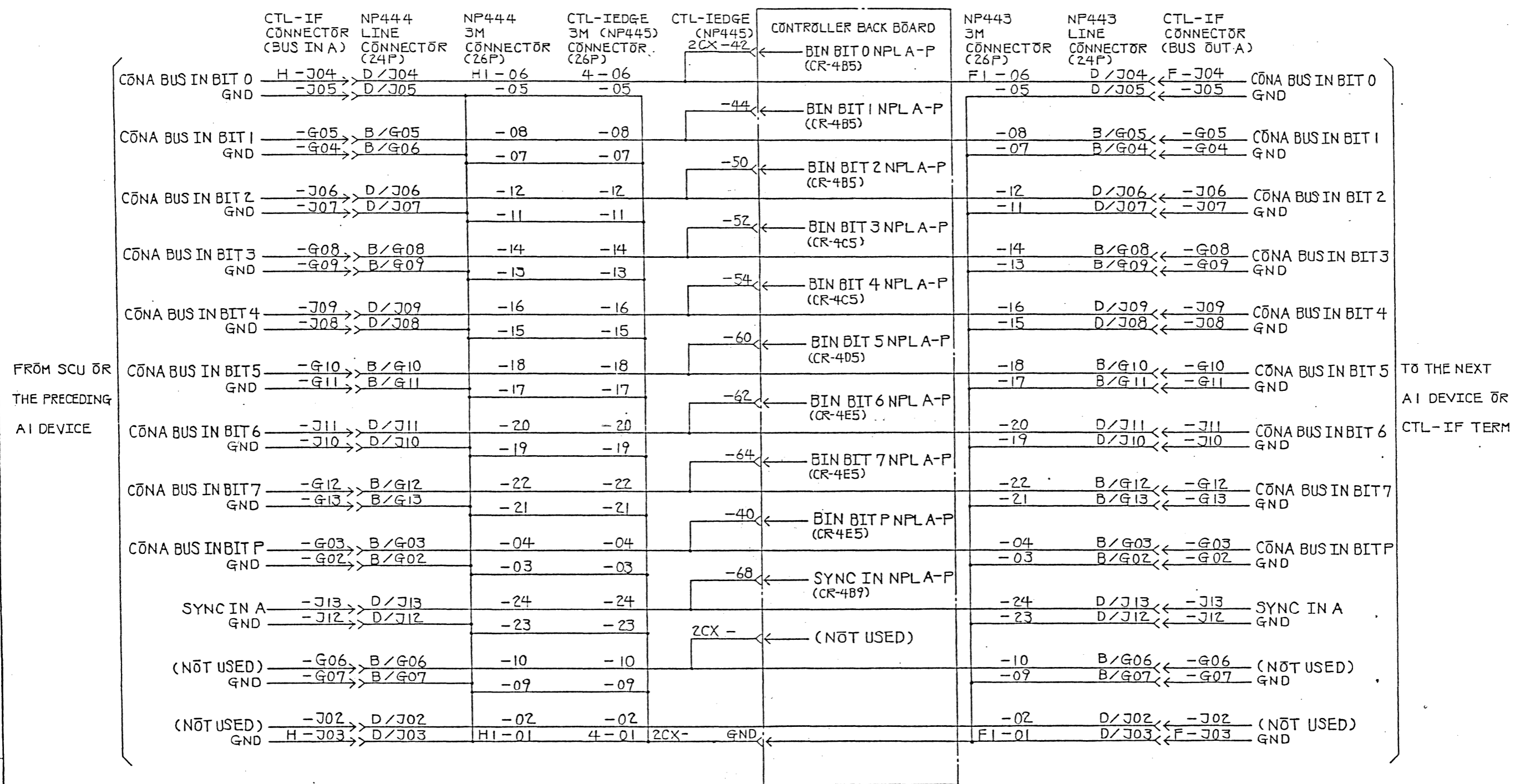
TO THE NEXT AI DEVICE OR CTL-IF TERM

(CTL INTERFACE A3) CX-3

P/N	TITLE	SHEET 3 / 8	DRAWN
REV	NP37 CTLR LOGIC DIA	REV 0	CHECK
	DRAWING NO		APPD
	NPL-NC-21445	Nippon Peripherals Limited	

A
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H

A
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H



(CTL INTERFACE A4) CX-4

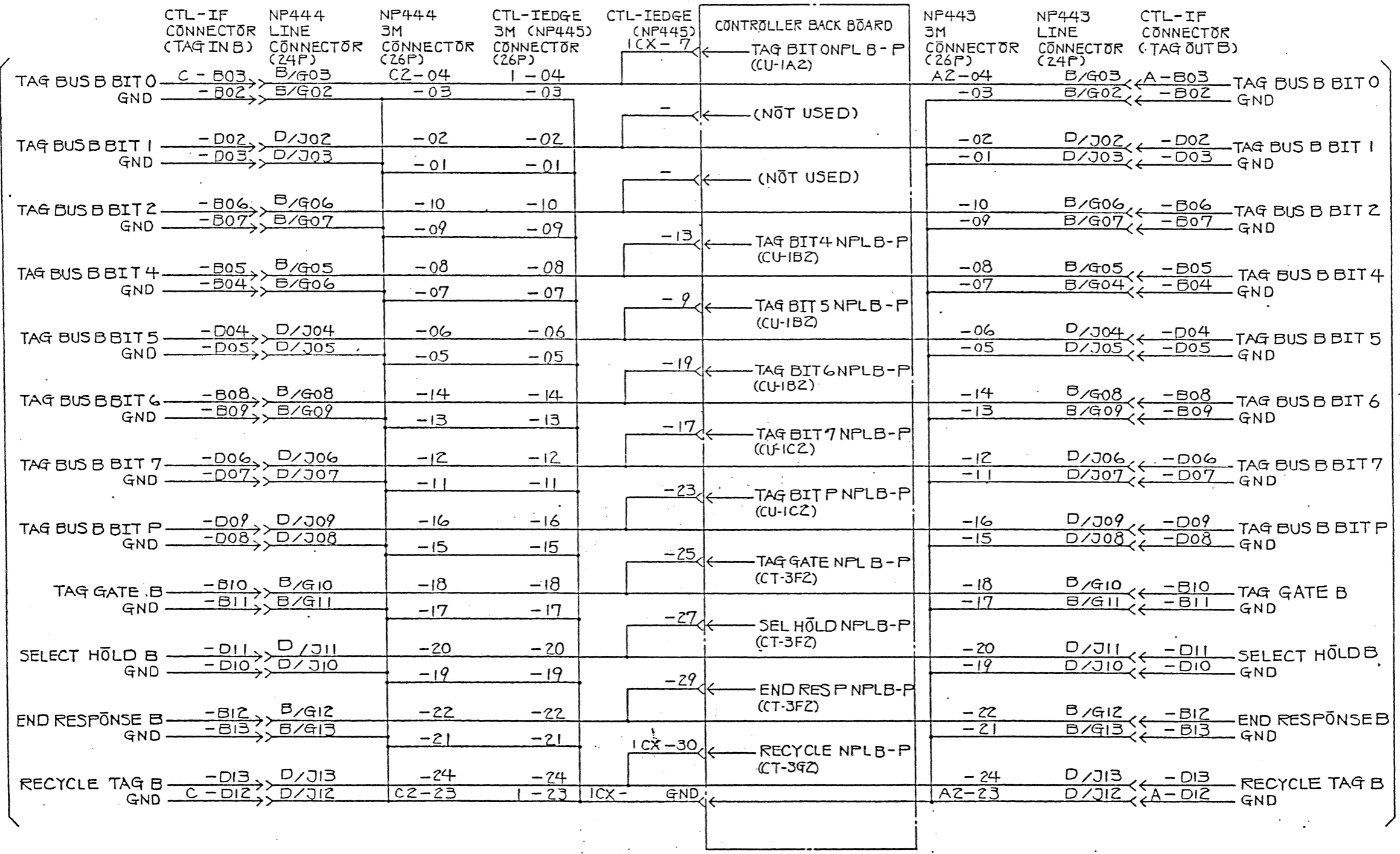
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	DRAWING NO NPL-NC-21445	REV 0	CHECK APPO
Nippon Peripherals Limited			

A
B
C
D
E
F
G
H

A
B
C
D
E
F
G
H

FROM SCU OR
THE PRECEDING
AI DEVICE

TO THE NEXT
AI DEVICE OR
CTL-IF TERM



(CTL INTERFACE B1)

CX-5

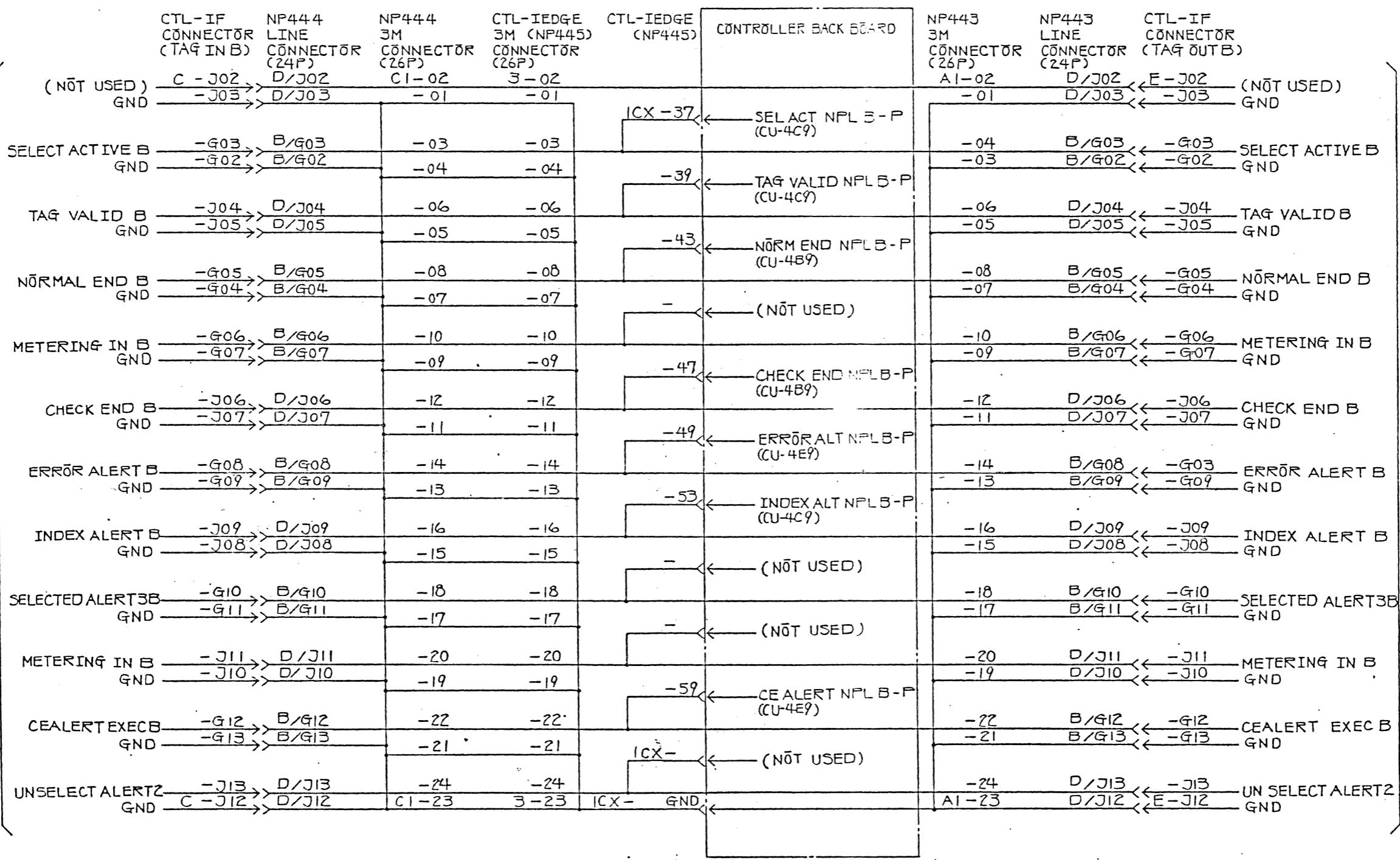
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	DRAWING NO NPL-NC-21445	REV 0	CHECK APPD
Nippon Peripherals Limited			

A
B
C
D
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G
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A
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C
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H

FRÖM SCU ÖR
THE PRECEDING
AI DEVICE

TÖ THE NEXT
AI DEVICE ÖR
CTL-IF TERM



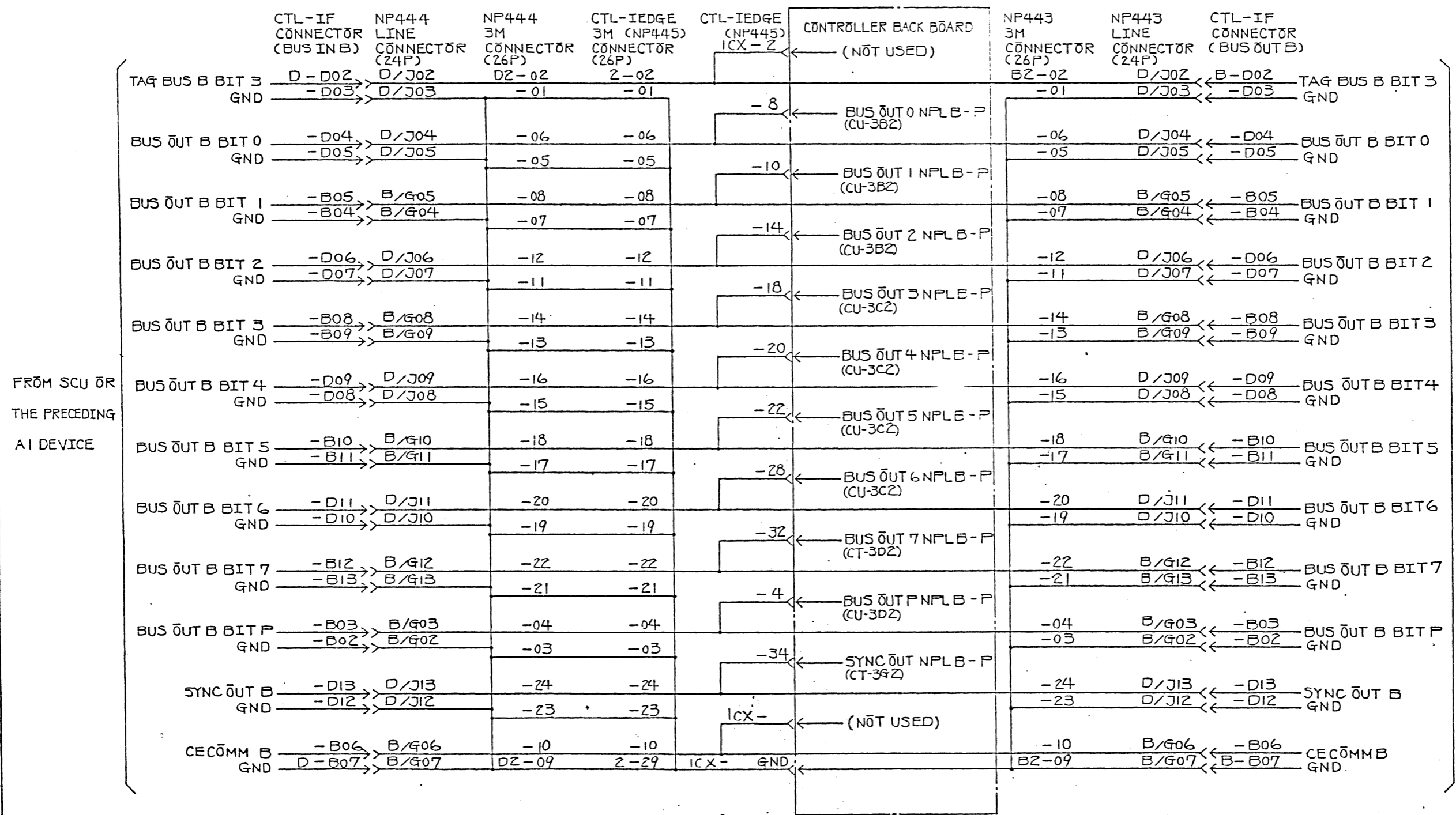
(CTL INTERFACE B 2)

CX-6

P/N	TITLE	SHEET 6/8	DRAWN
REV	NP37CTLR LOGIC DIA	REV 0-	CHECK
	DRAWING NO		APPD
	NPL-NC-21445	Nippon Peripherals Limited	

A
B
C
D
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F
G
H

A
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E
F
G
H



TO THE NEXT
AI DEVICE OR
CTL-IF TERM

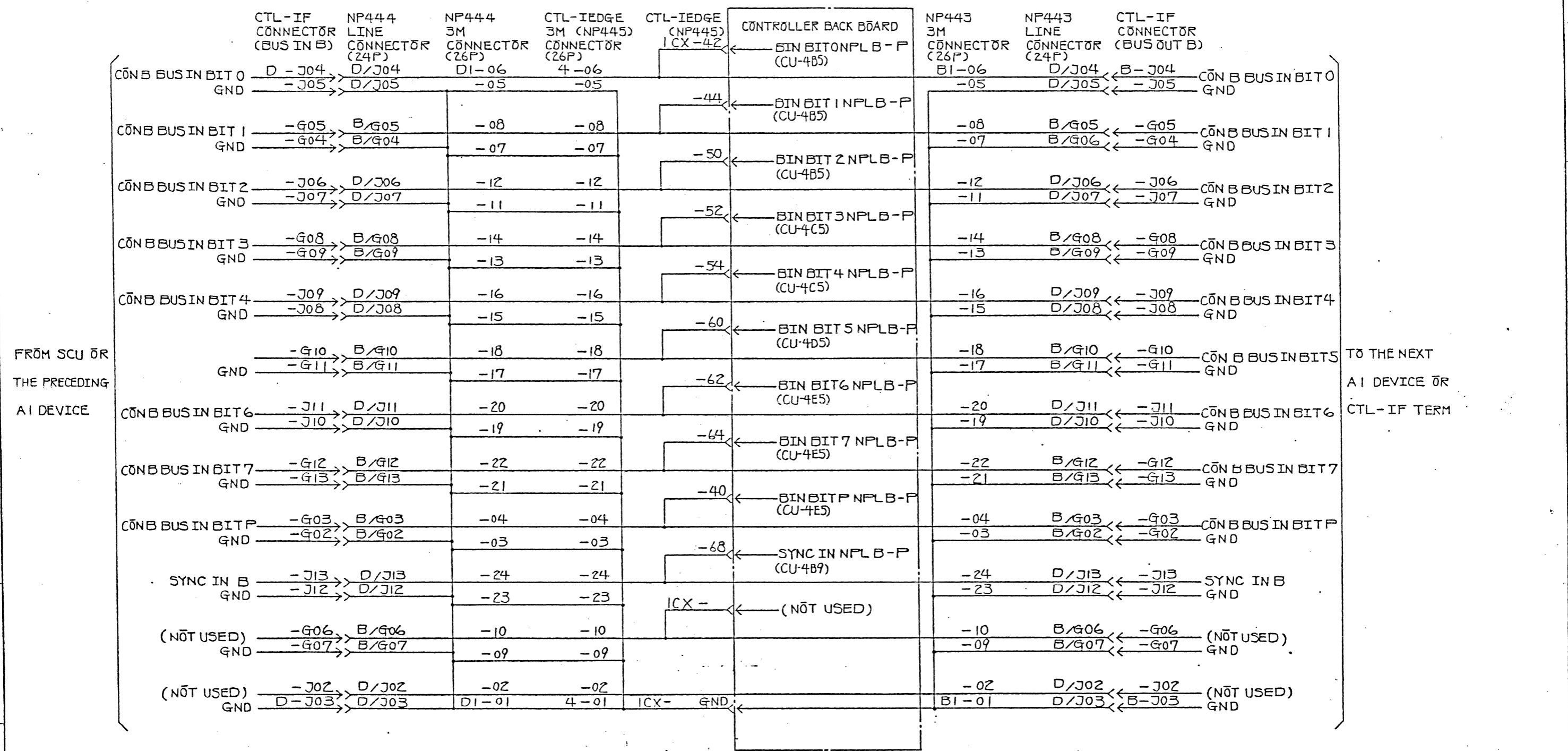
(CTL INTERFACE B3)

CX-7

P/N	TITLE	SHEET 7 / 8	DRAWN
REV	NP37 CTLR LOGIC DIA	REV 0	CHECK
DRAWING NO		Nippon Peripherals Limited	
NPL-NC-21445			

A
B
C
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F
G
H

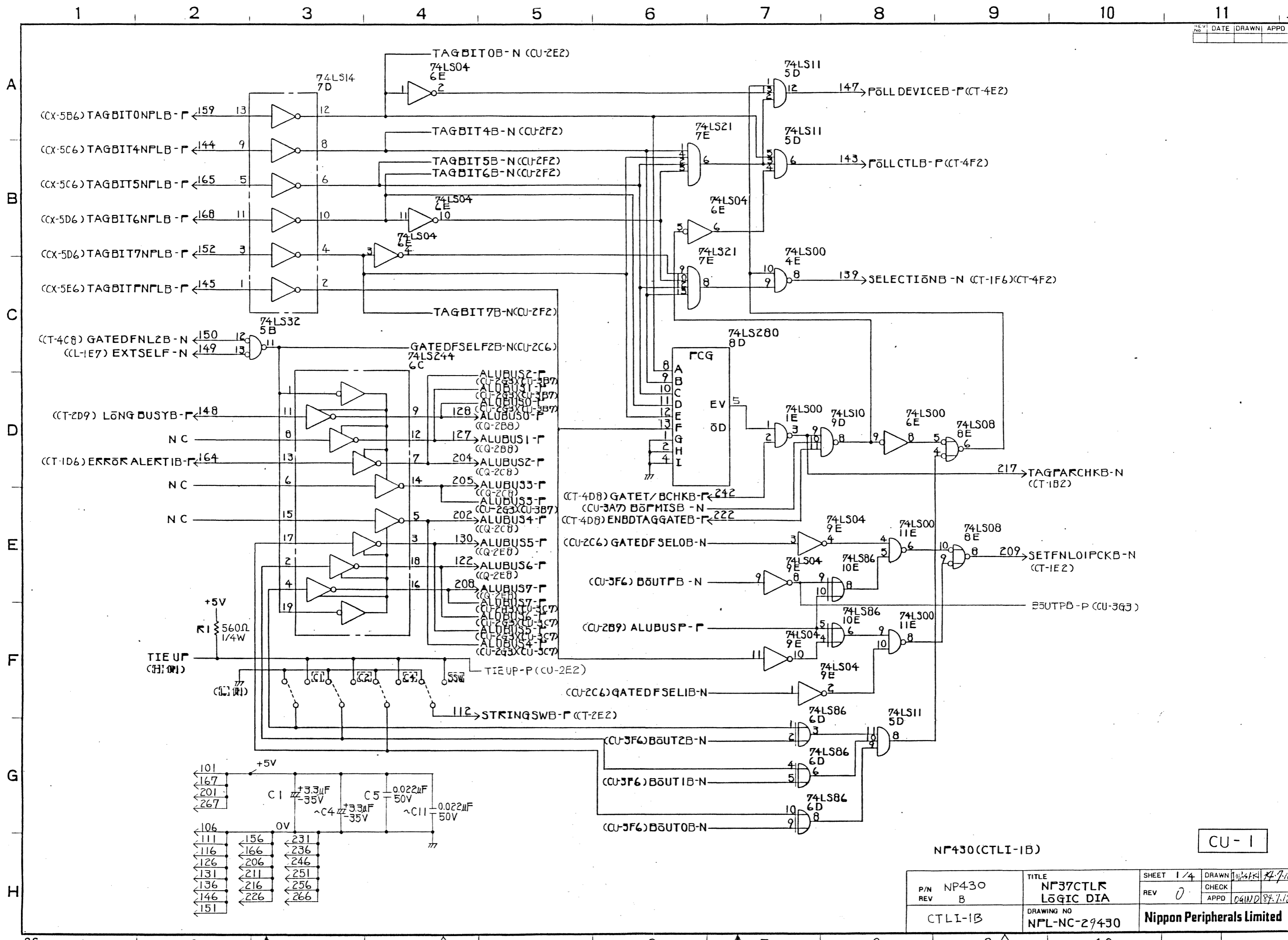
A
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C
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G
H



(CTL INTERFACE B4) CX-8

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 8 / 8	DRAWN
		REV. 0	CHECK
DRAWING NO NPL-NC-21445		Nippon Peripherals Limited	

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TIE UP (H101)

+5V

R1 560Ω 1/4W

C1 3.3μF 35V

C4 3.3μF 35V

C5 0.022μF 50V

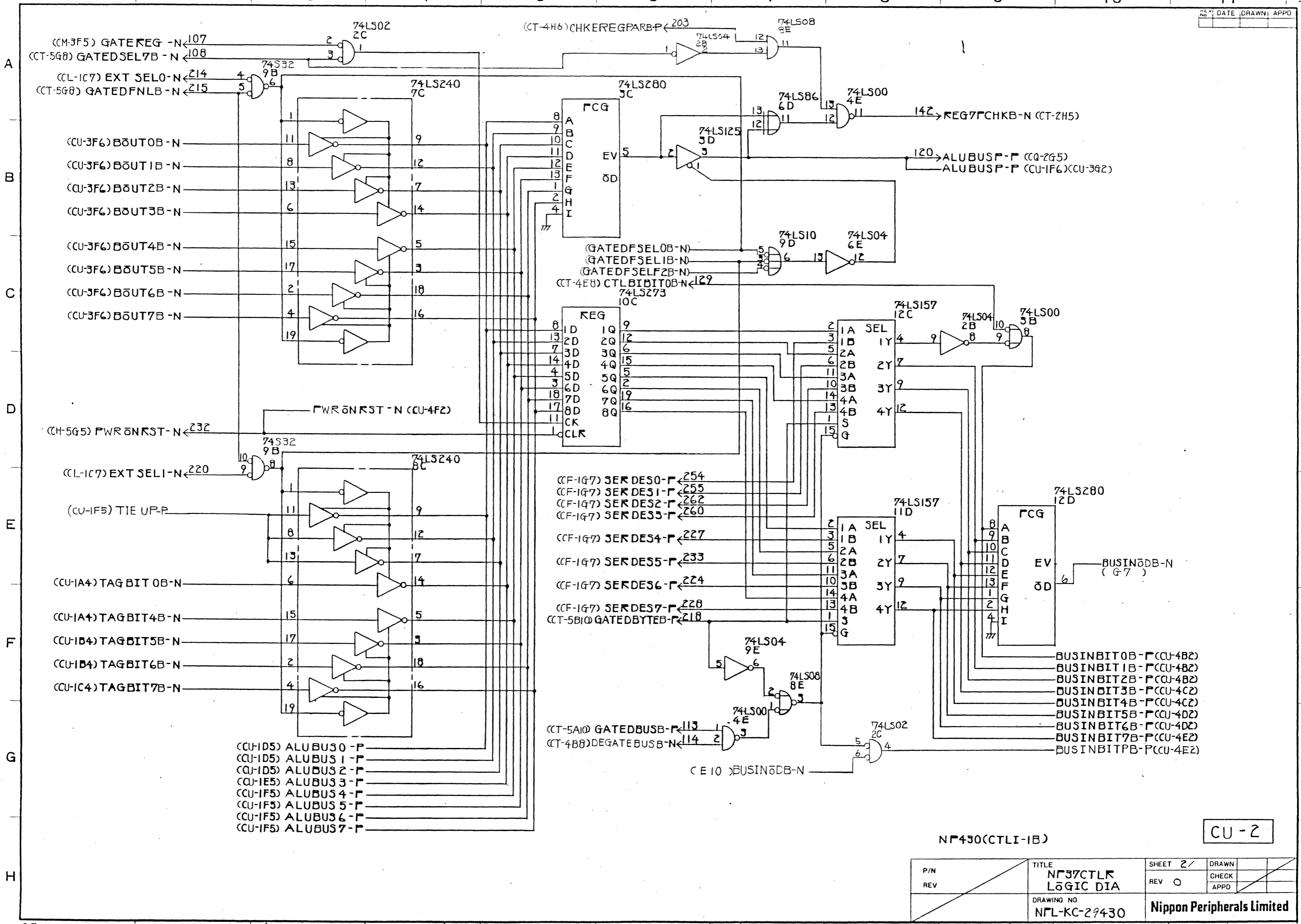
55W

101	156	231
167	166	236
201	206	246
267	211	251
106	216	256
111	226	266
116		
126		
131		
136		
146		
151		

NP430 (CTLI-1B)

P/N NP430	TITLE NP37CTLR LOGIC DIA	SHEET 1/4	DRAWN [Signature]
REV B	DRAWING NO NPL-NC-29430	REV 0	CHECK [Signature]
CTLI-1B		APPD [Signature]	

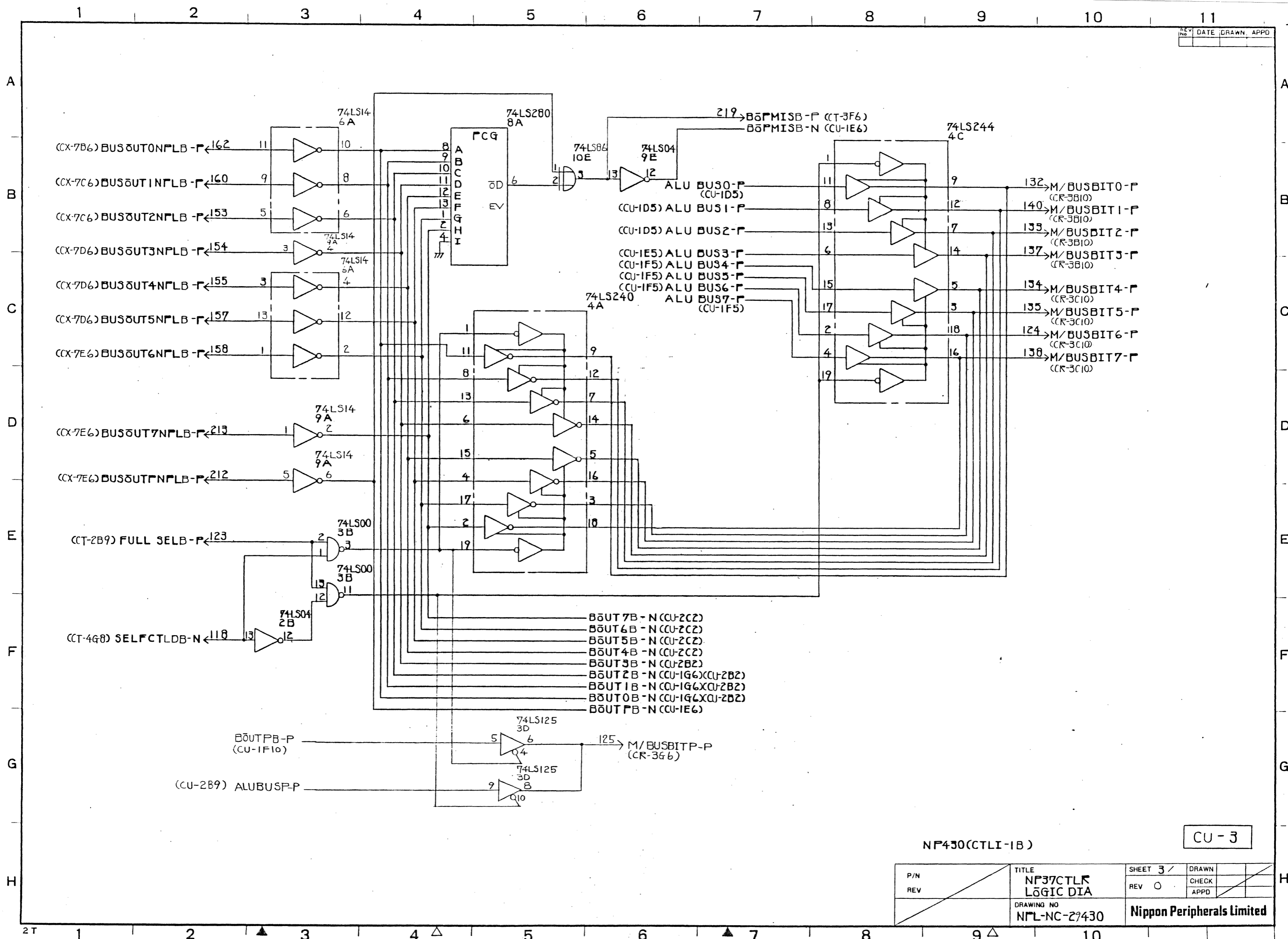
Nippon Peripherals Limited



NF430(CTLI-1B)

CU-2

P/N	REV	TITLE	SHEET 2/	DRAWN	CHECK	APPD
		NF37CTLR LOGIC DIA	REV 0			
DRAWING NO			NPL-KC-29430			
			Nippon Peripherals Limited			



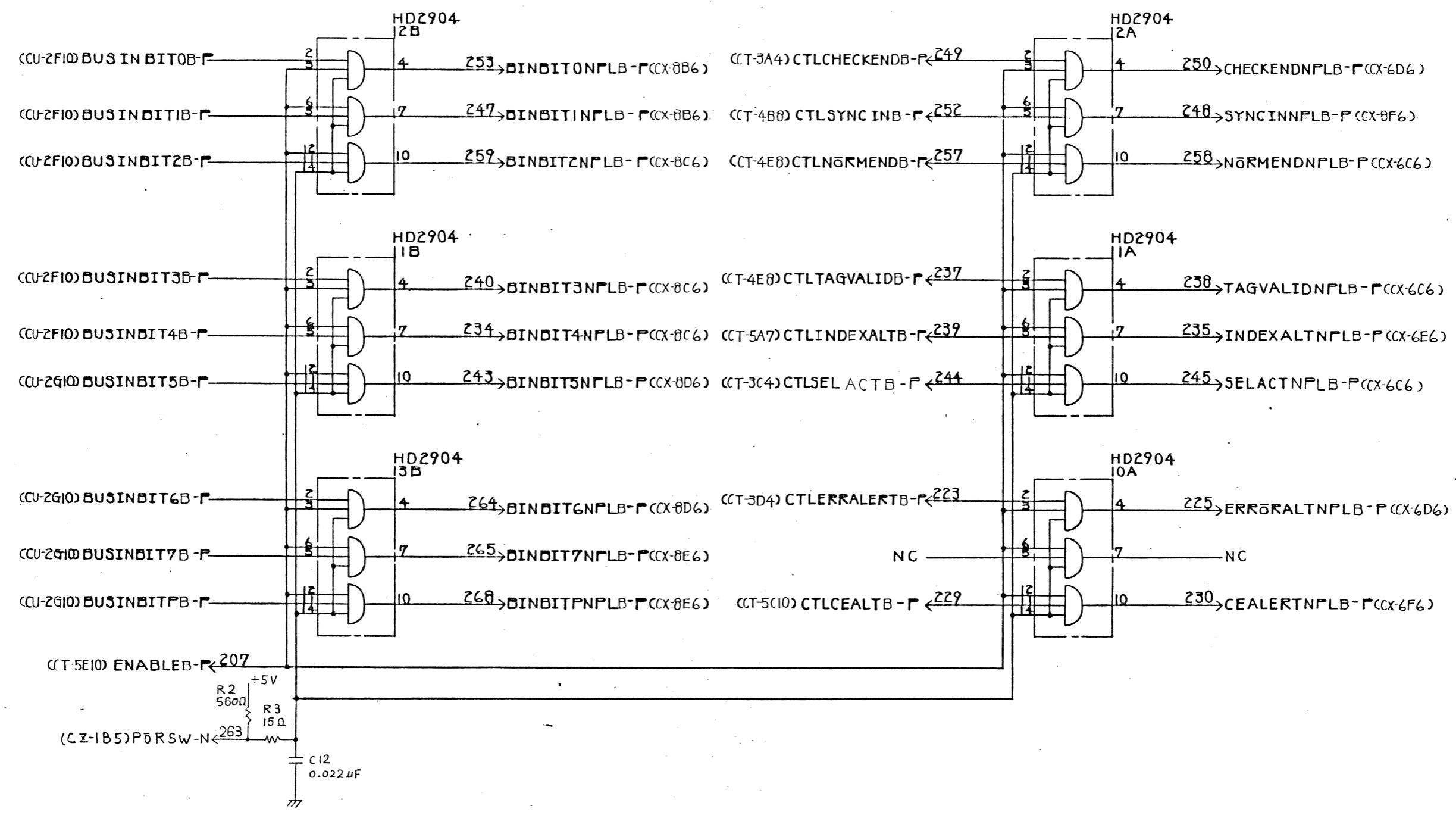
NP430(CTLI-1B)

CU-3

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 3 /	DRAWN
	DRAWING NO NFL-NC-29430	REV 0	CHECK APPD
		Nippon Peripherals Limited	

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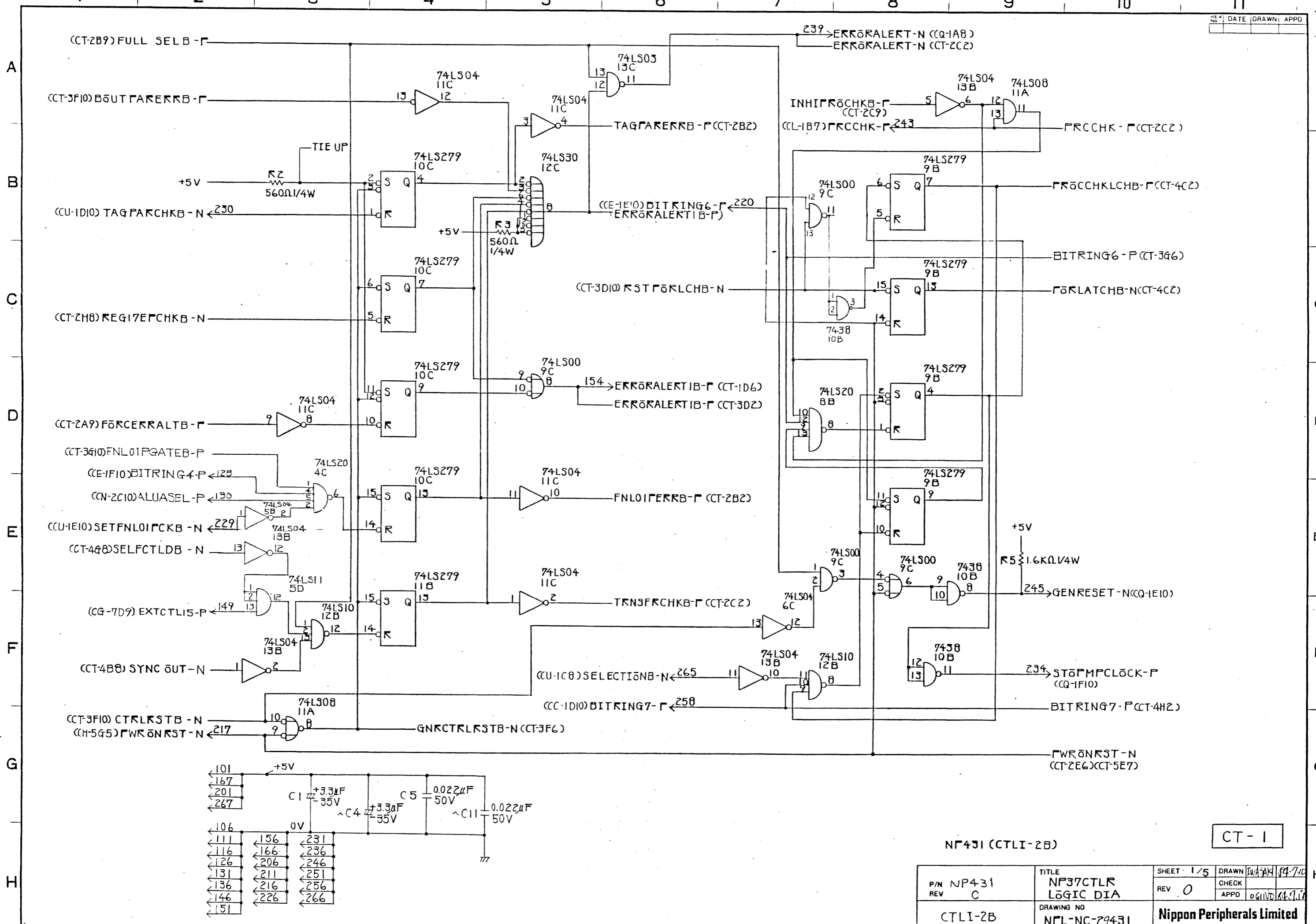
REV	DATE	DRAWN	APPD



NF430(CTLI-1B)

CU-4

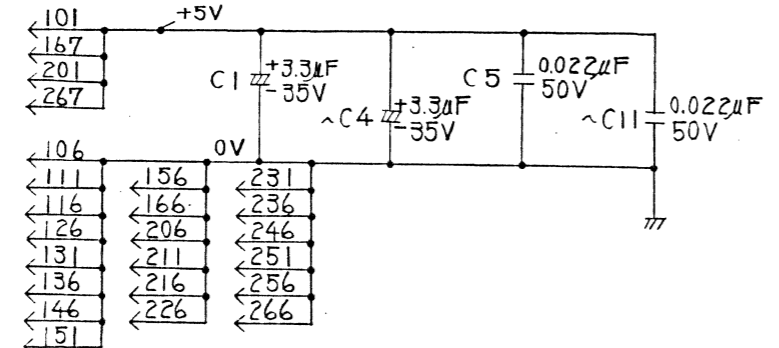
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	DRAWING NO NPL-NC-29430	REV 0	CHECK APPD
Nippon Peripherals Limited			



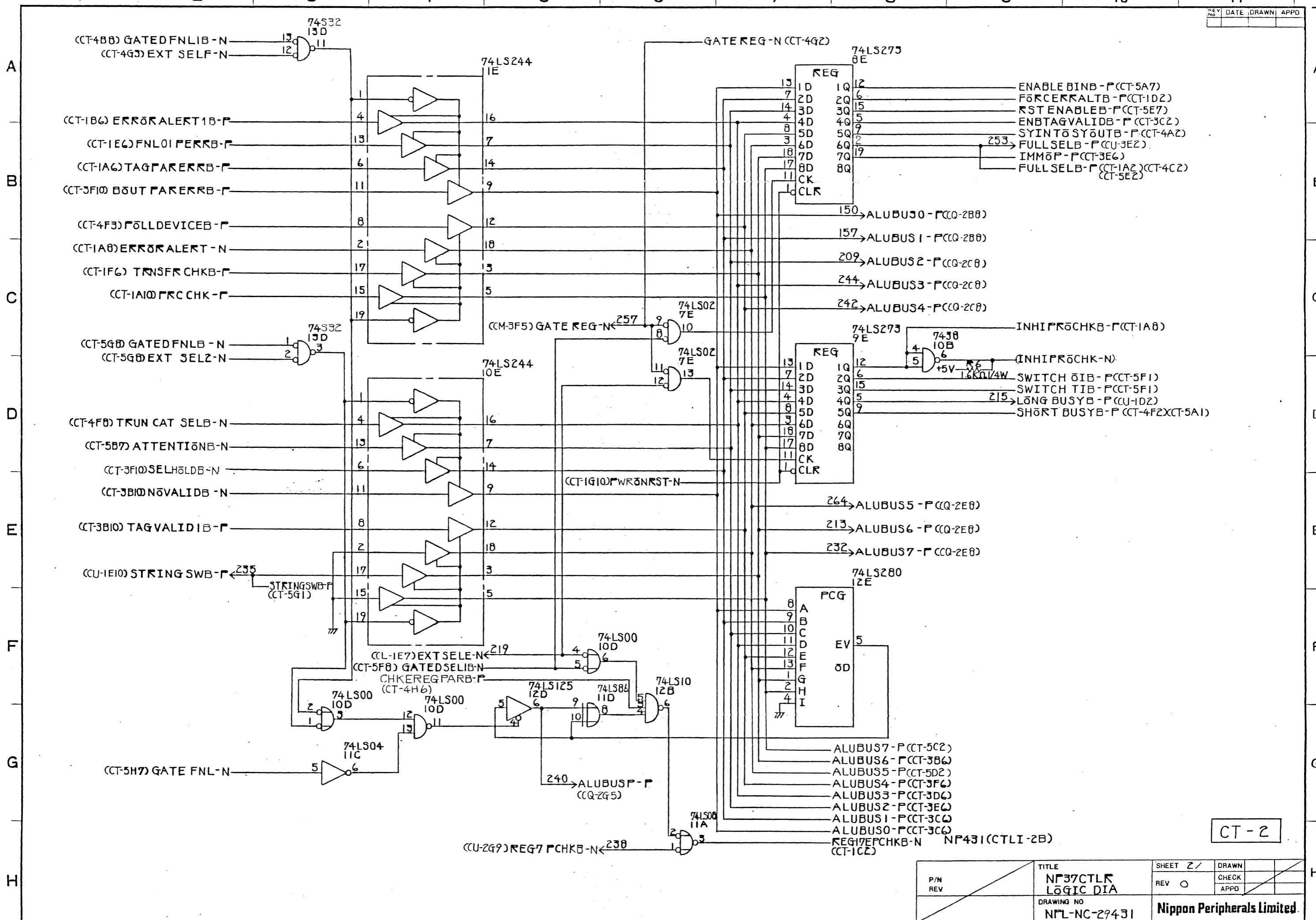
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NP431 (CTLI-2B)

CT-1

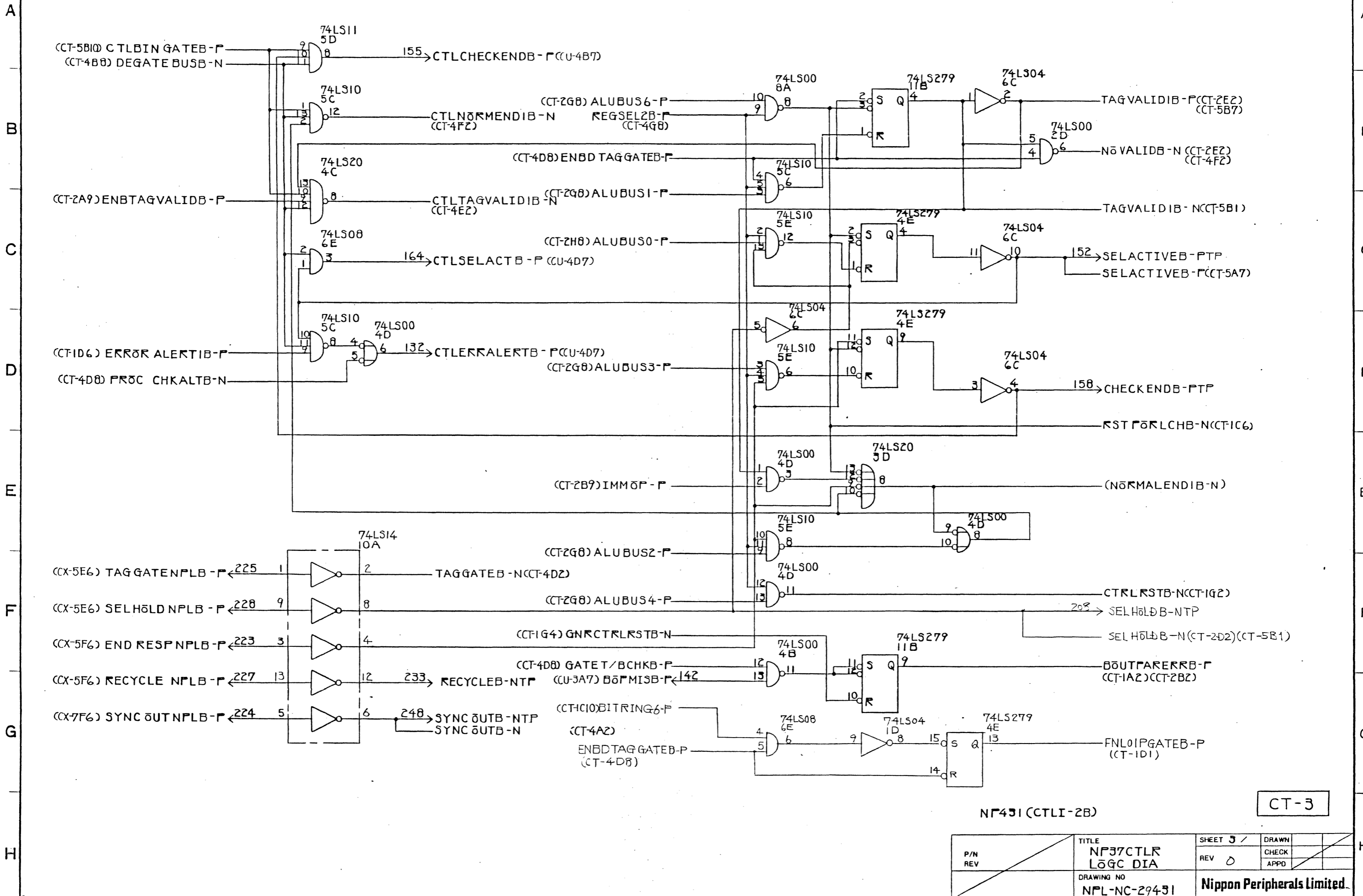


P/N REV	NP431 C	TITLE	NP37CTLR LOGIC DIA	SHEET	1/5	DRAWN	DAWAH	84-7/0
REV	0	CHECK		APPD		OGINO	14.9.84	
CTLI-2B		DRAWING NO NFL-NC-29431		Nippon Peripherals Limited				



CT-2

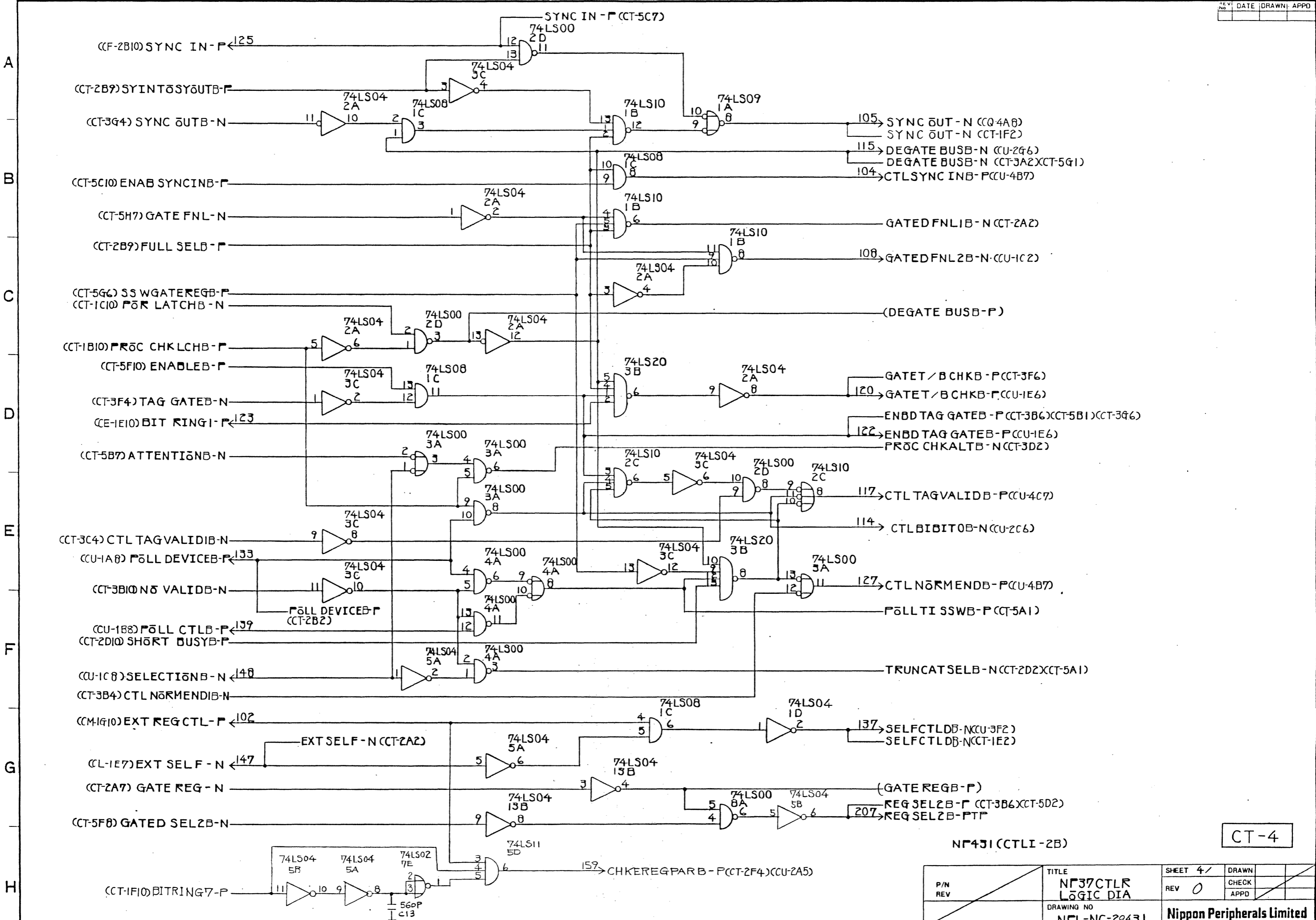
P/N REV	TITLE NIP37CTLR LOGIC DIA	SHEET 2 /	DRAWN
	DRAWING NO NPL-NC-29431	REV 0	CHECK
Nippon Peripherals Limited		APPD	



NPL-NC-294-31 (CTLI-2B)

CT-3

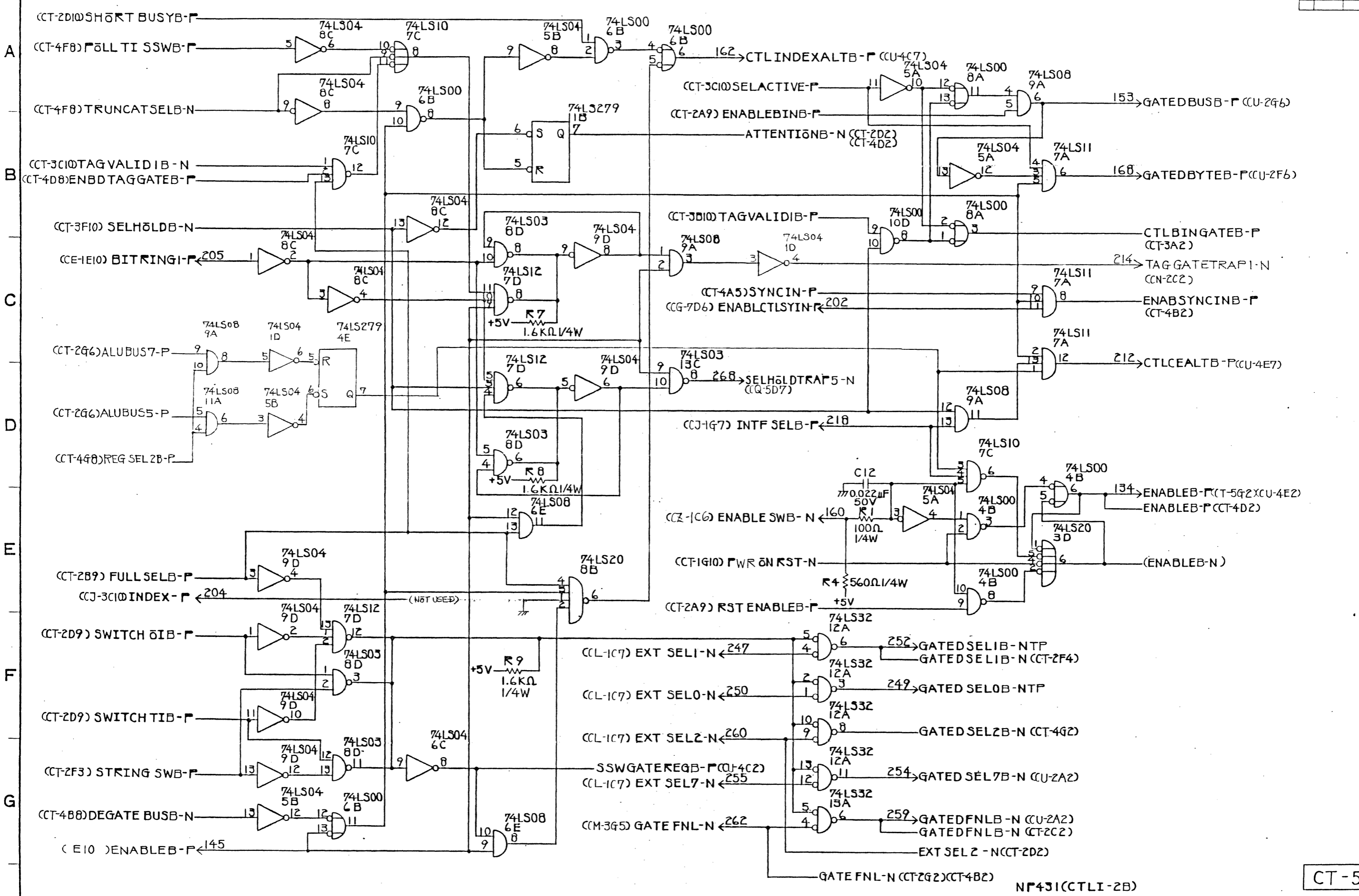
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		Nippon Peripherals Limited	



CT-4

NF431 (CTLI-2B)

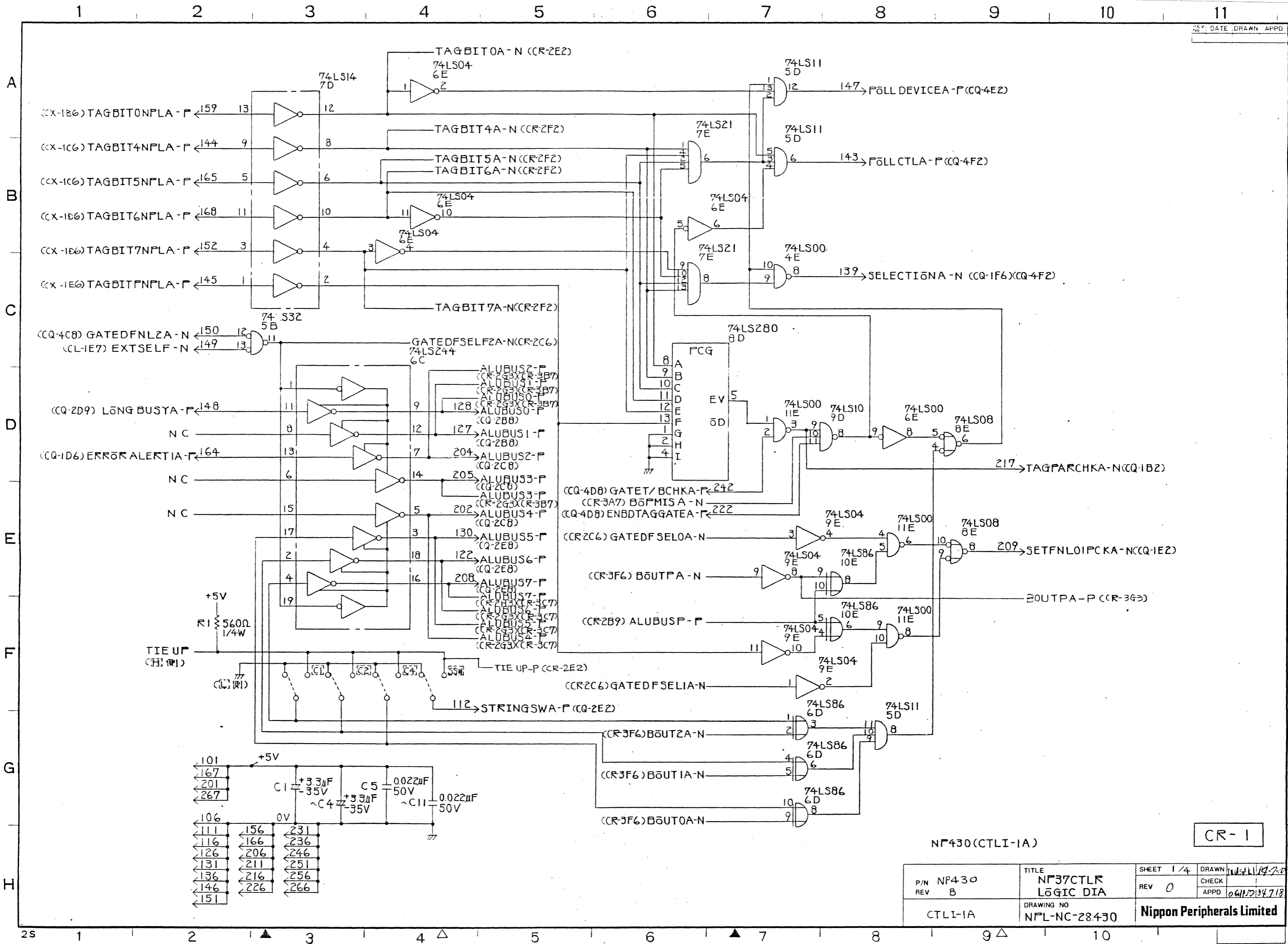
P/N REV	TITLE	SHEET 4/	DRAWN
	NF37CTLR LOGIC DIA	REV 0	CHECK
DRAWING NO NFL-NC-29431		APPD	
Nippon Peripherals Limited			



CT-5

P/N REV		TITLE NP37CTLR LOGIC DIA	SHEET 5/5	DRAWN	
		DRAWING NO NPL-NC-29431	REV 0	CHECK	
		Nippon Peripherals Limited			

69

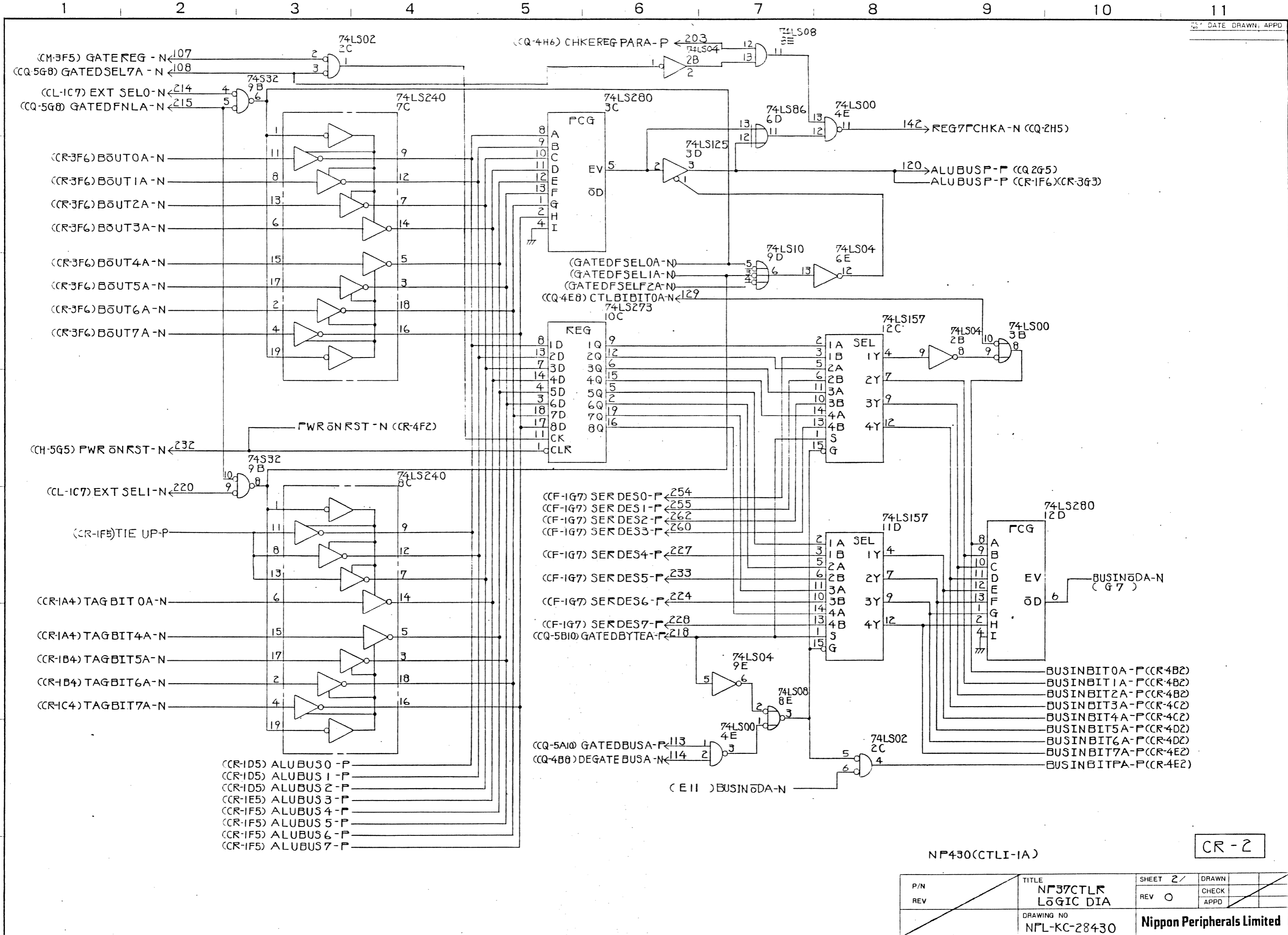


NP430(CTLI-1A)

CR-1

P/N NP430	TITLE NP37CTLR LOGIC DIA	SHEET 1/4	DRAWN 11/11/74
REV B		REV 0	CHECK
CTLI-1A	DRAWING NO NFL-NC-28430	APPD 06/12/74	
Nippon Peripherals Limited			

30

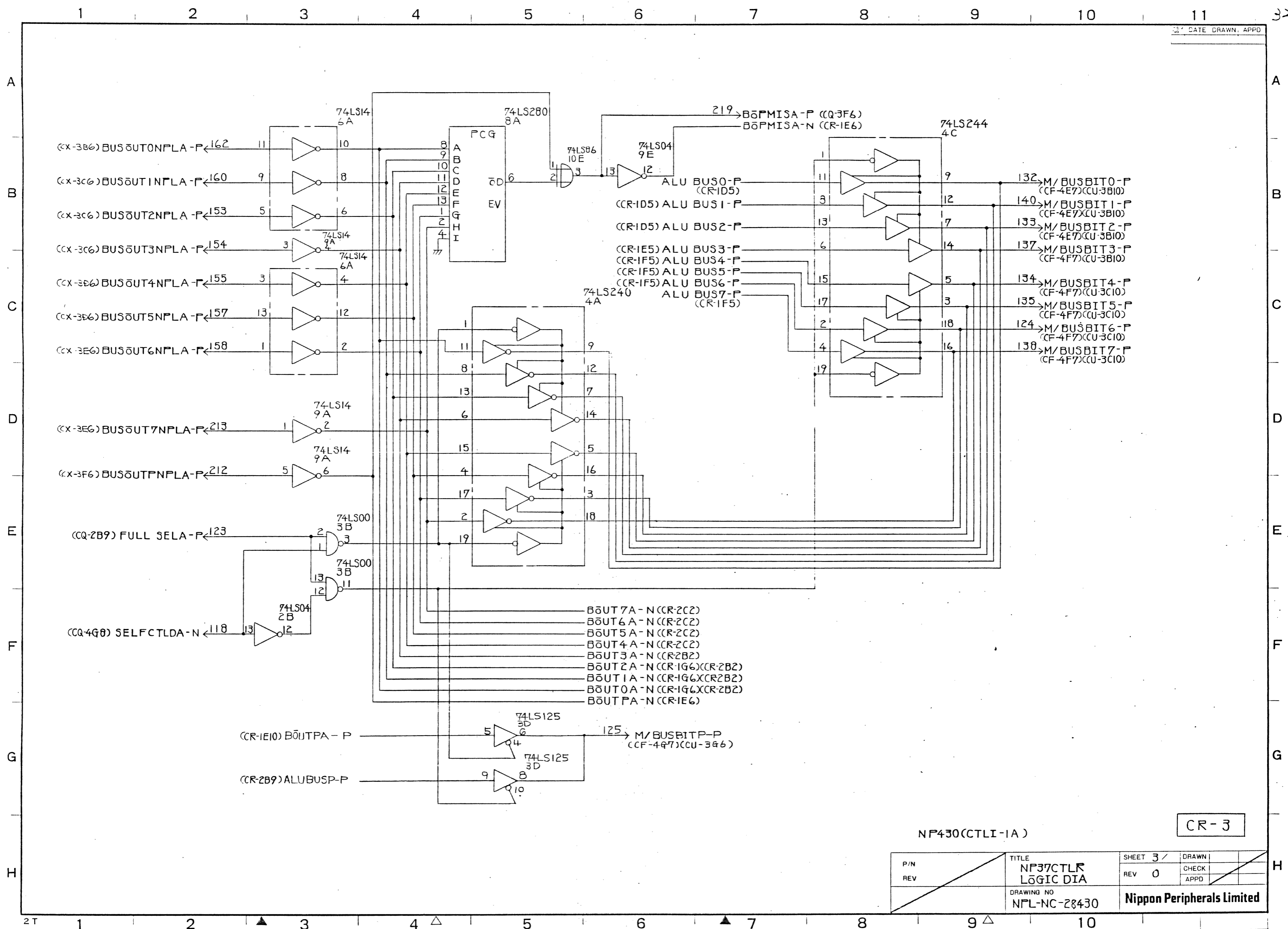


NPL430(CTLI-1A)

CR-2

P/N	REV	TITLE	SHEET 2/	DRAWN	CHECK	APPD
		NPL37CTLR LOGIC DIA	REV 0			
DRAWING NO			NPL-KC-28430			
			Nippon Peripherals Limited			

16

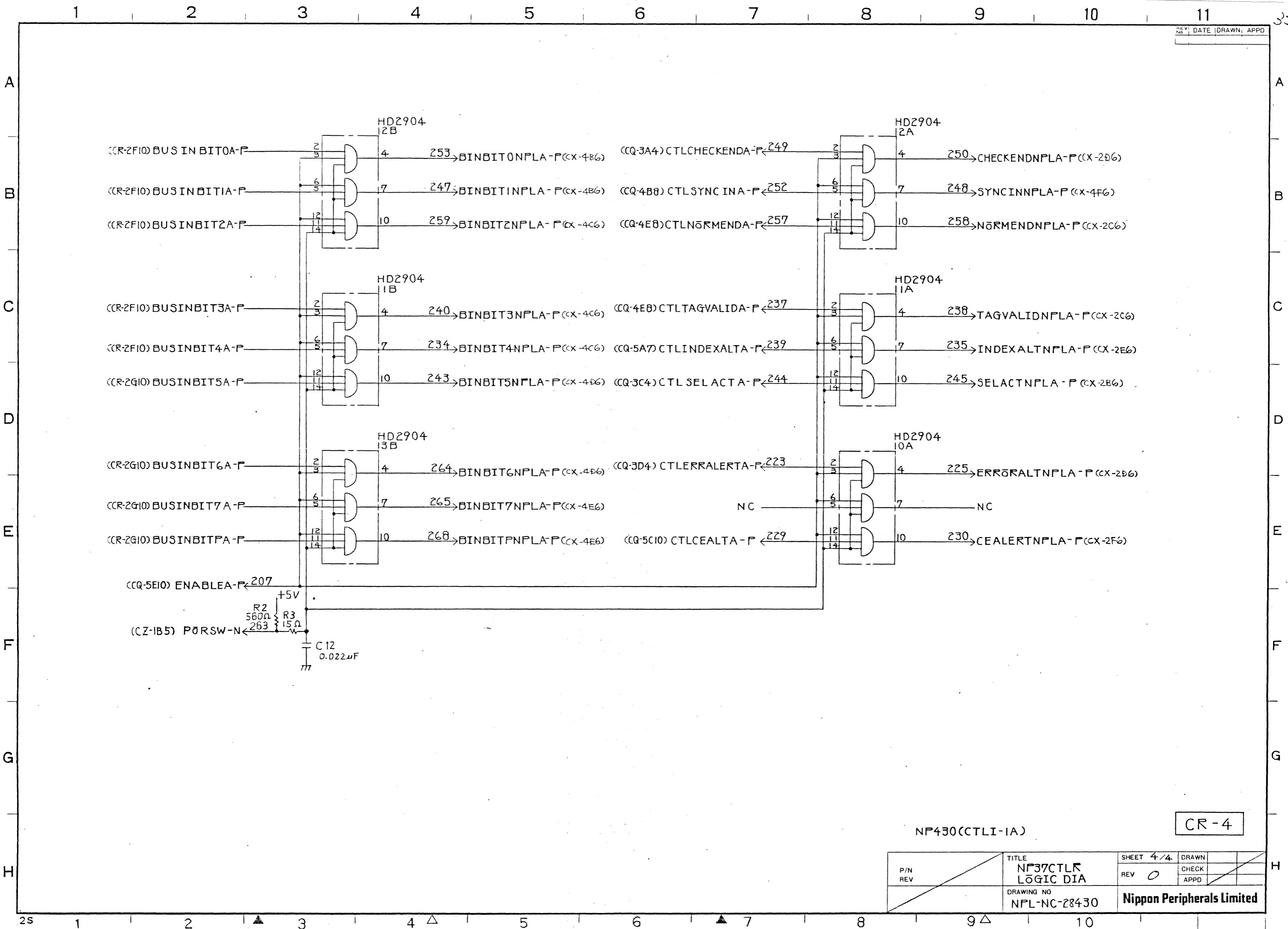


CR-3

NP430(CTLI-1A)

P/N	TITLE	SHEET 3 /	DRAWN
REV	NP37CTLR LOGIC DIA	REV 0	CHECK
	DRAWING NO		APPD
	NPL-NC-28430	Nippon Peripherals Limited	

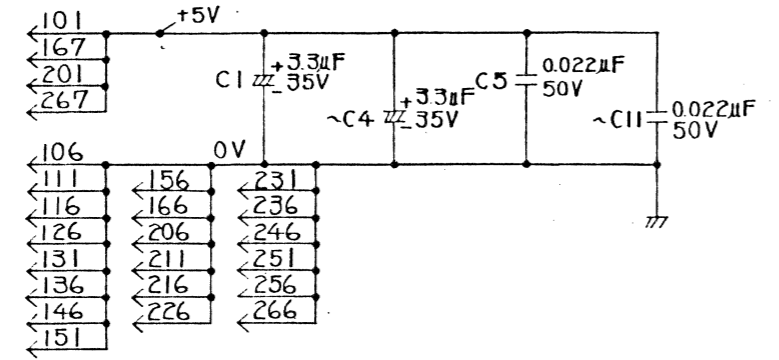
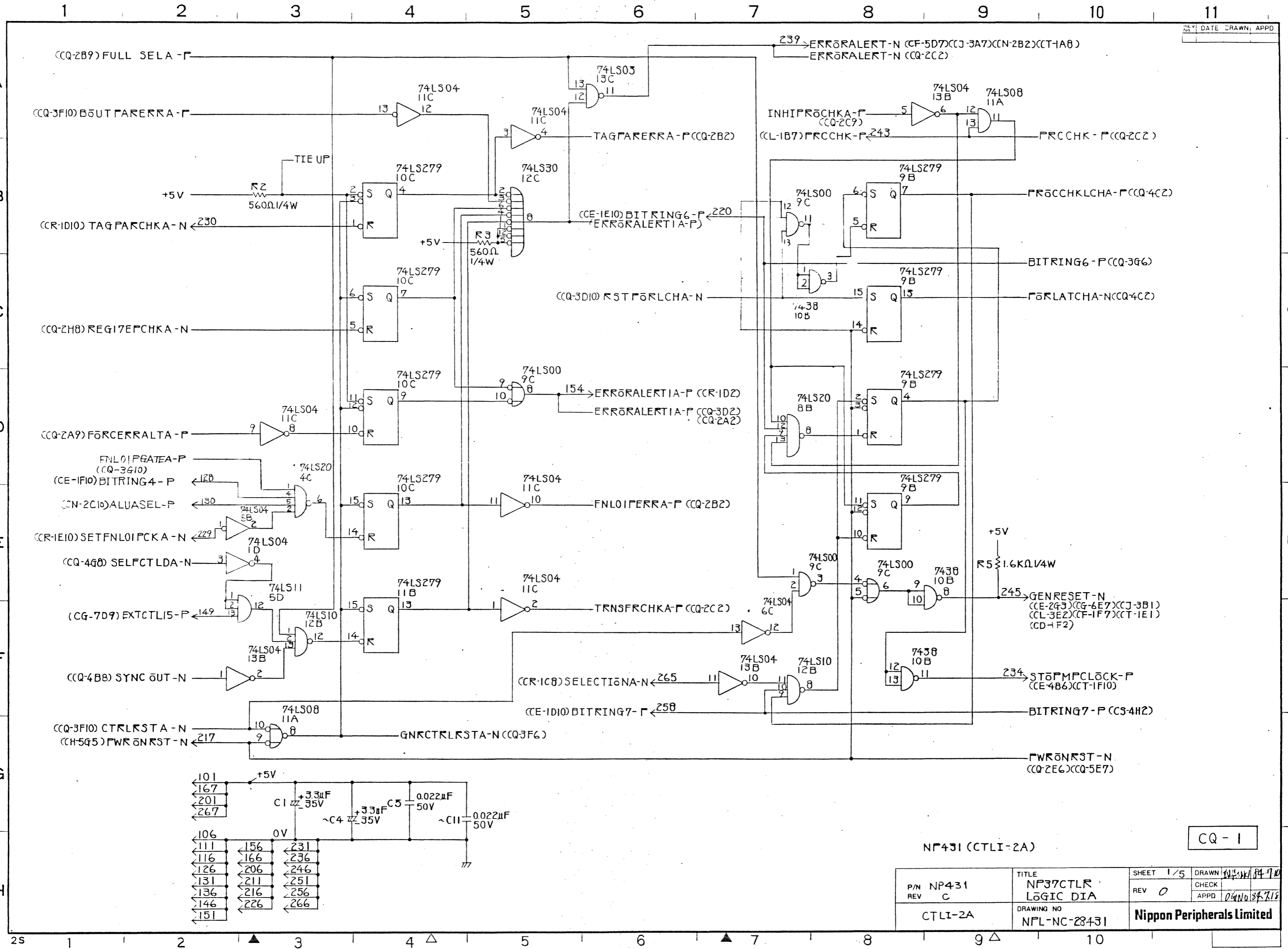
32



NF430(CTLI-1A)

CR-4

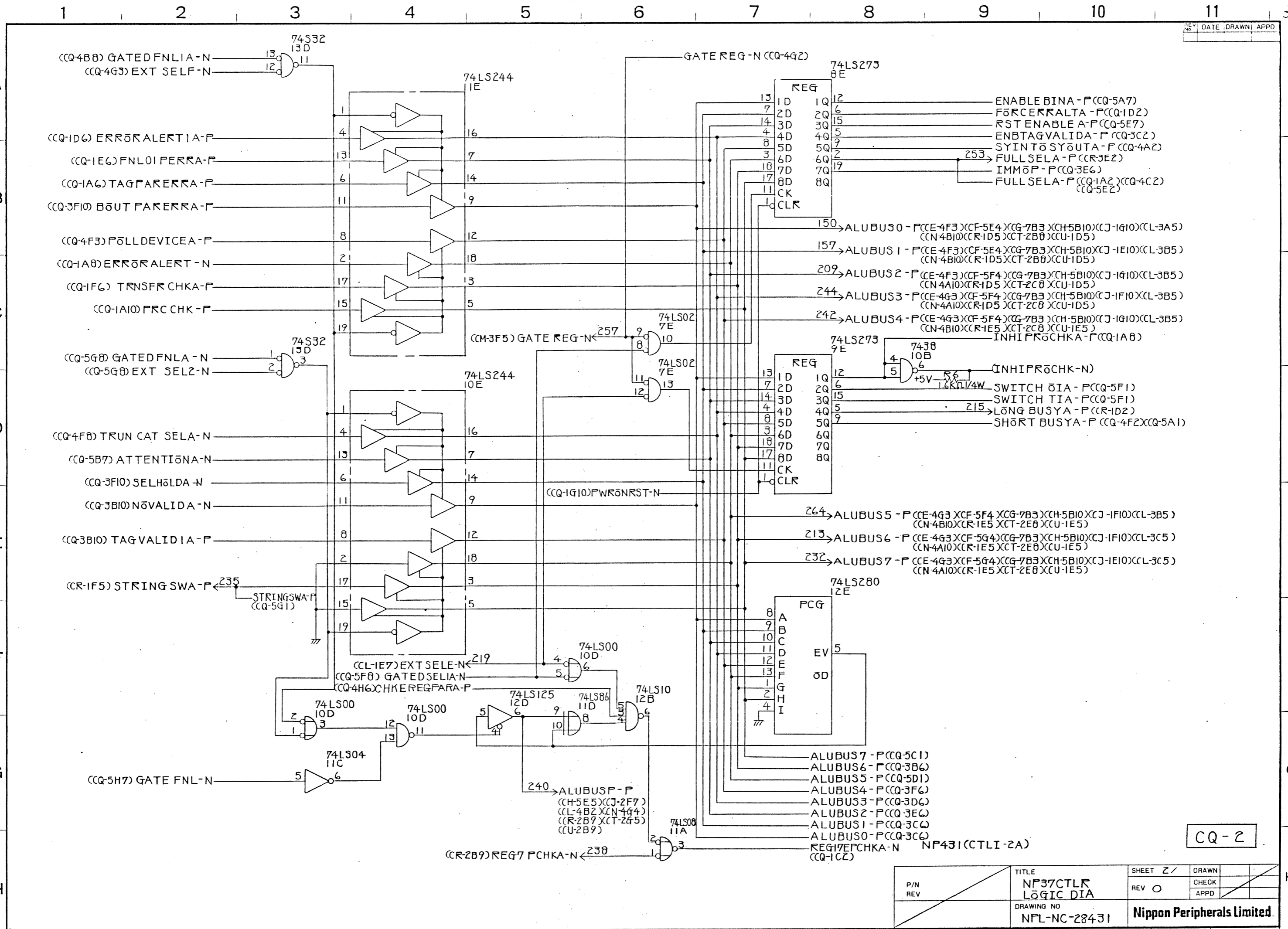
P/N REV	TITLE	SHEET 4/4	DRAWN
	NF37CTLR LOGIC DIA	REV 0	CHECK
DRAWING NO NFL-NC-28430		APPD	
Nippon Peripherals Limited			



NP431 (CTLI-2A)

CQ-1

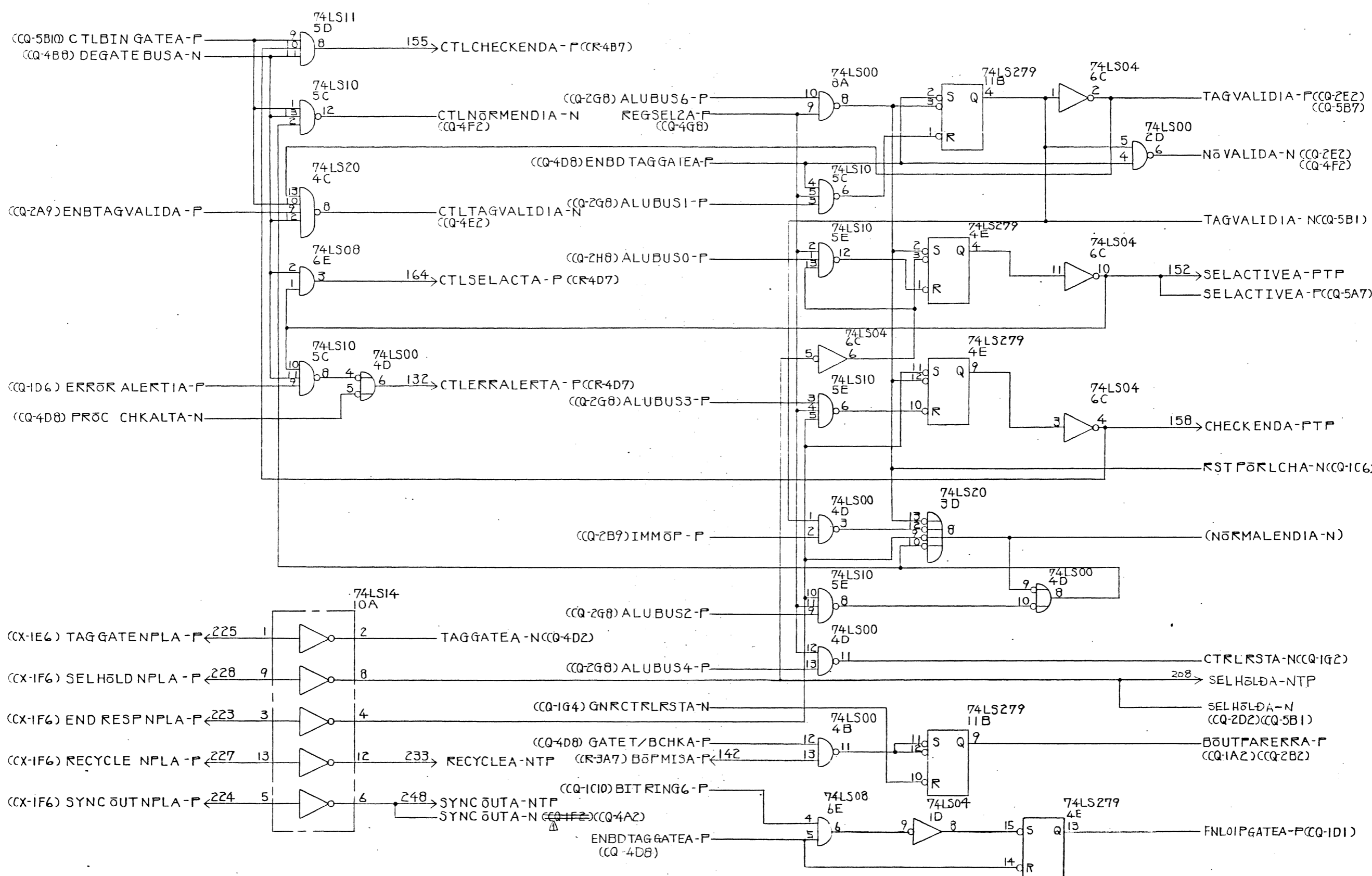
P/N NP431 REV C	TITLE NP37CTLR LOGIC DIA	SHEET 1/5 REV 0	DRAWN CHECK APPD
CTLI-2A	DRAWING NO NPL-NC-28431	Nippon Peripherals Limited	



CQ-2

P/N REV	TITLE NF37CTLR LOGIC DIA	SHEET 2/	DRAWN
	DRAWING NO NFL-NC-28431	REV 0	CHECK APPD
		Nippon Peripherals Limited.	

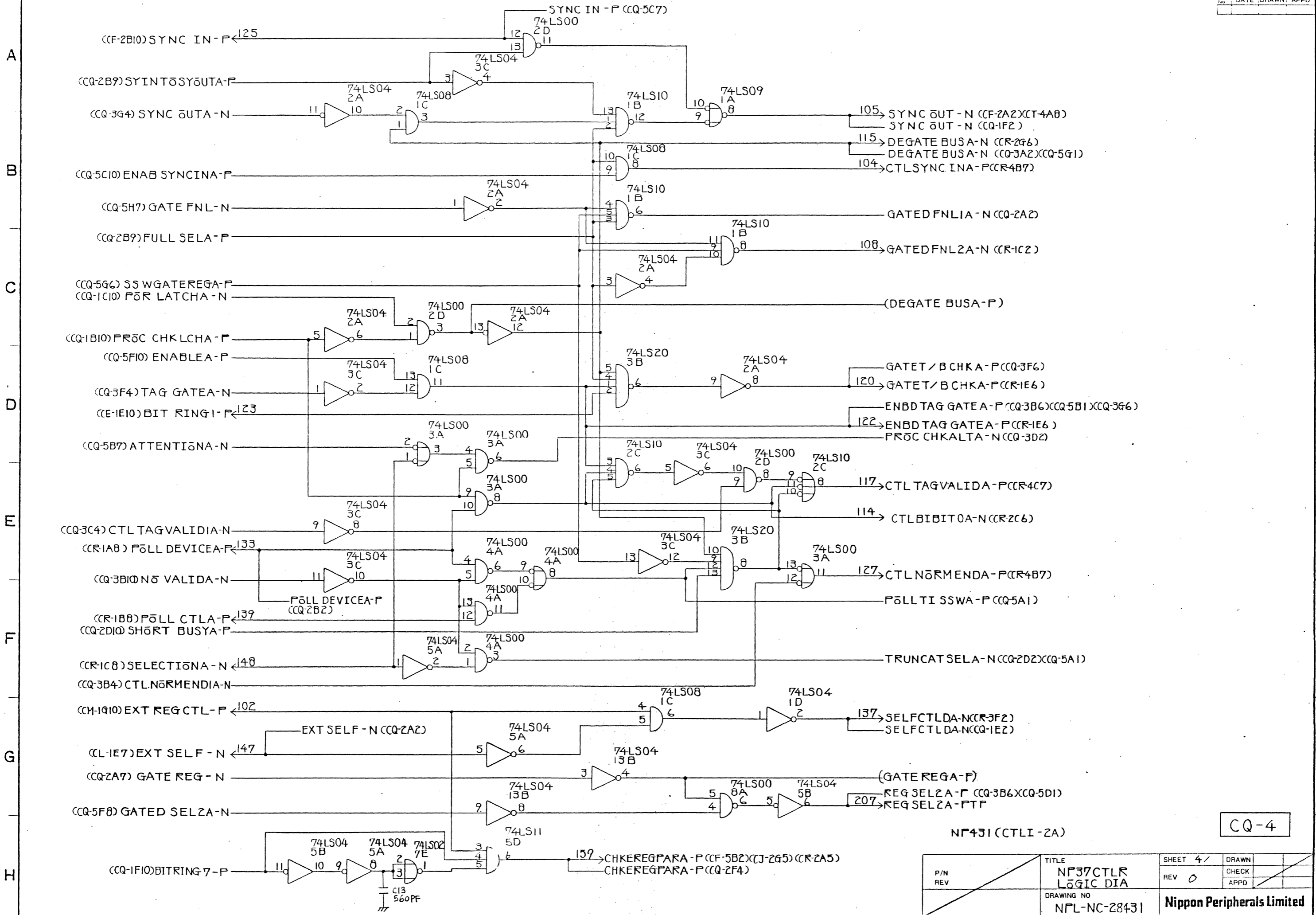
35



NP431 (CTLI-2A)

CQ-3

P/N REV	TITLE	SHEET 3 /	DRAWN
	NP37CTLR LOGC DIA	REV 0	CHECK
DRAWING NO		APPD	
NPL-NC-28431		Nippon Peripherals Limited.	

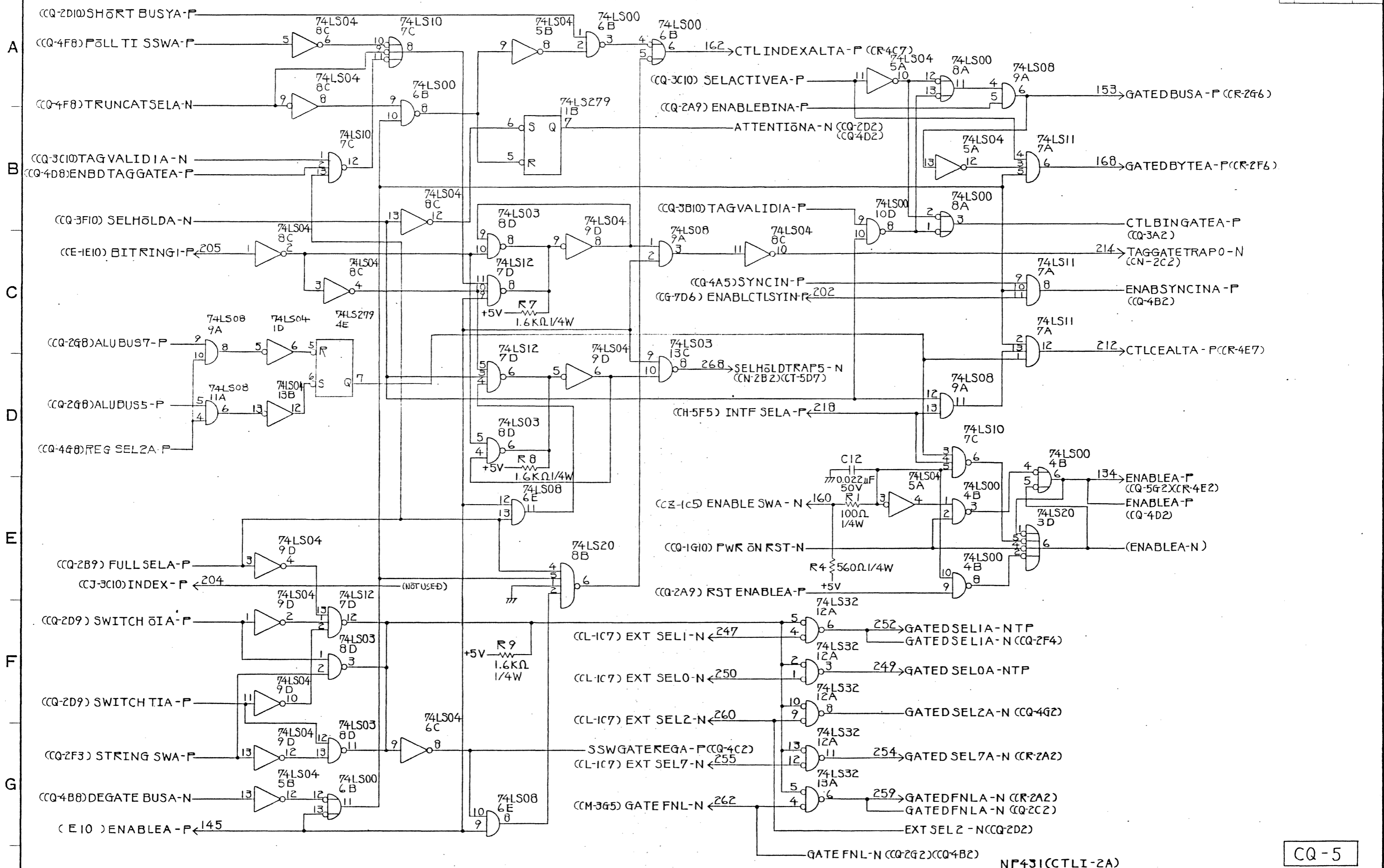


NIP431 (CTLI-2A)

CQ-4

P/N REV	TITLE NIP37CTLR LOGIC DIA	SHEET 4/	DRAWN
		REV 0	CHECK
DRAWING NO NFL-NC-28431		Nippon Peripherals Limited	

37

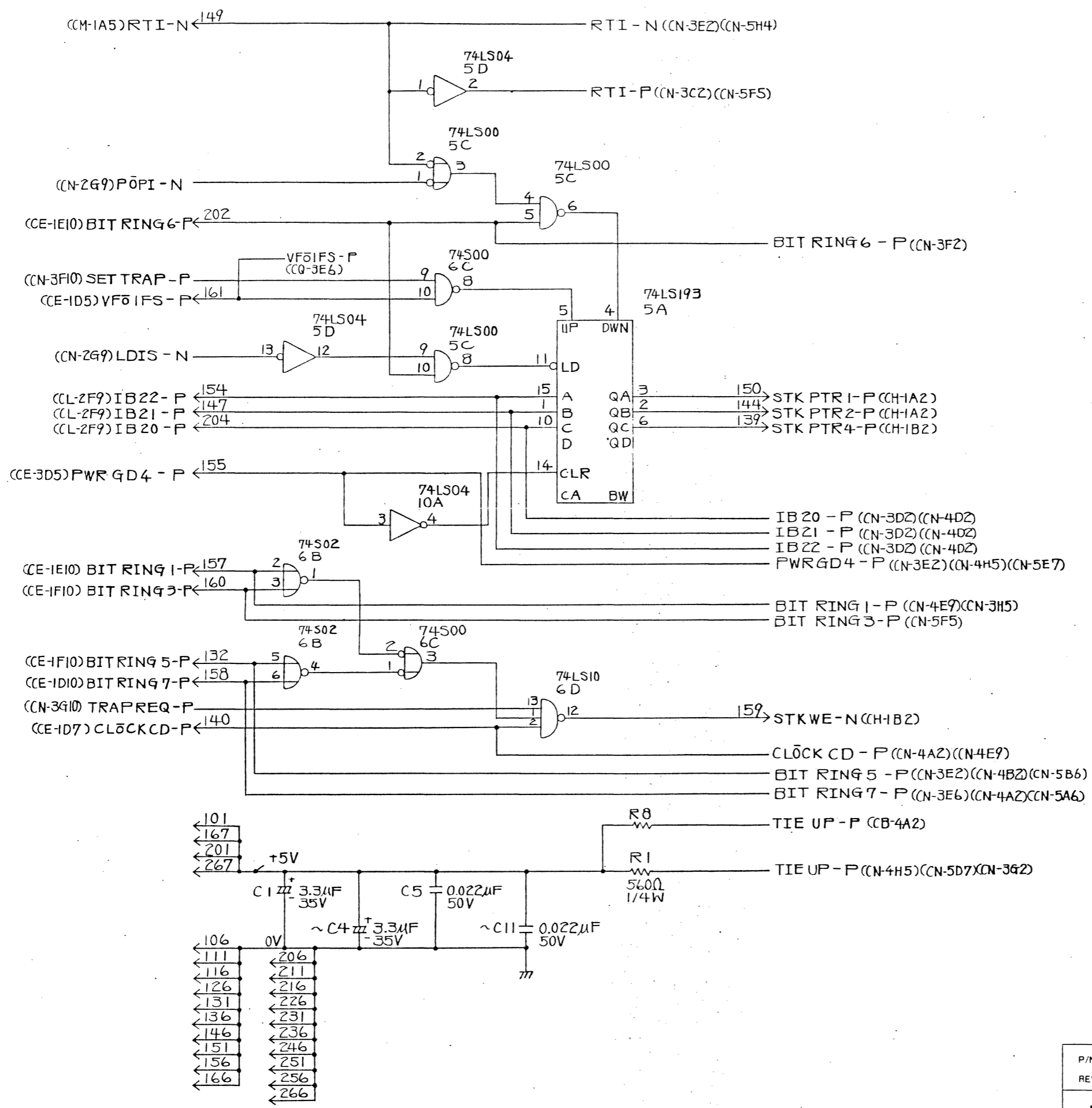


NP431 (CTLI-2A)

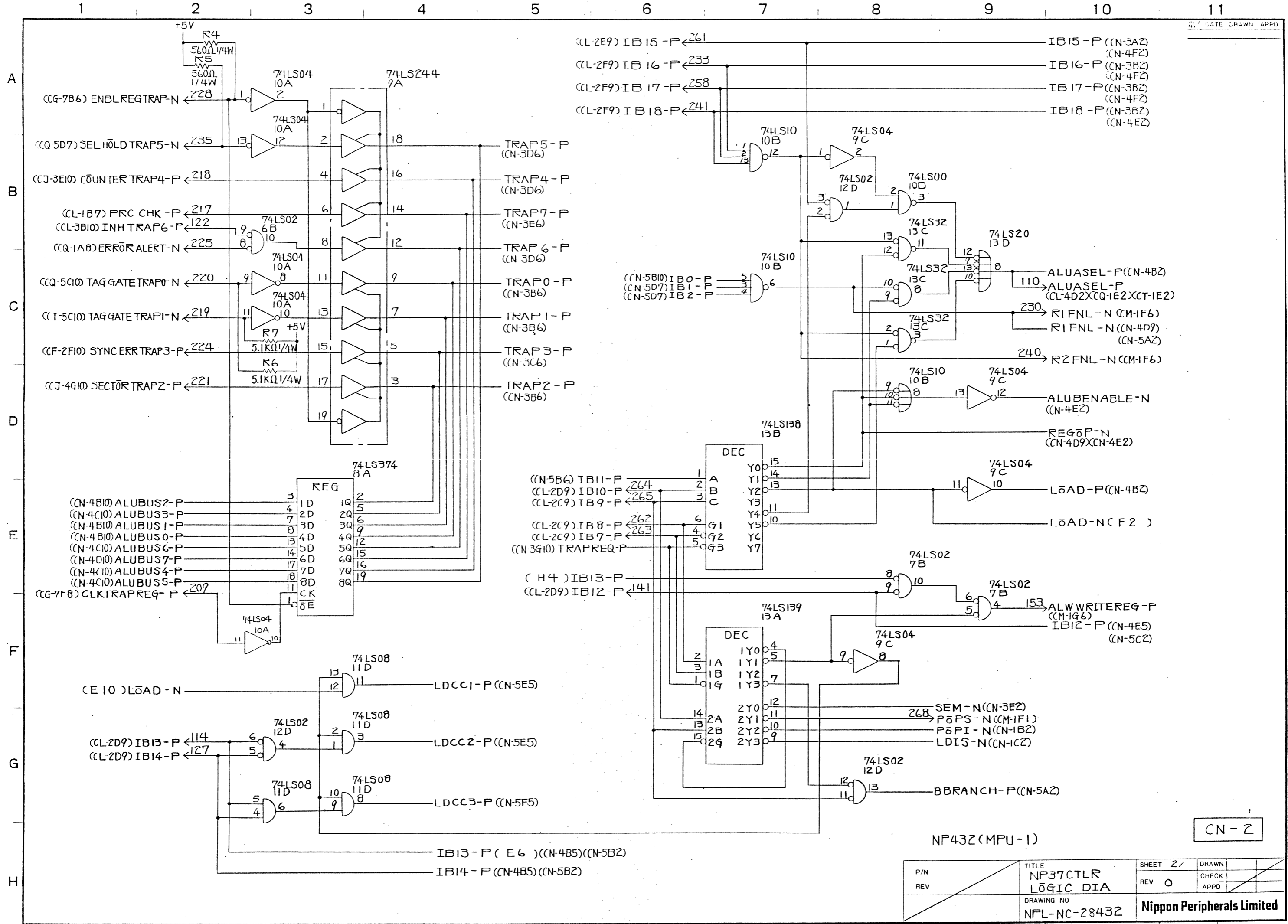
CQ-5

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 5 / 5	DRAWN	
		REV 0	CHECK	
DRAWING NO NPL-NC-28431		Nippon Peripherals Limited		

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NP432(MPU-1)		CN-1	
P/N NP432	TITLE NP37CTLR	SHEET 1/5	DRAWN A.G.M. 82.1.28
REV B	LÖGIC DIA	REV 0	CHECK APPD K.HASHI 82.1.28
MPU-1	DRAWING NO NPL-NC-28432	Nippon Peripherals Limited	



NP432(MPU-1)

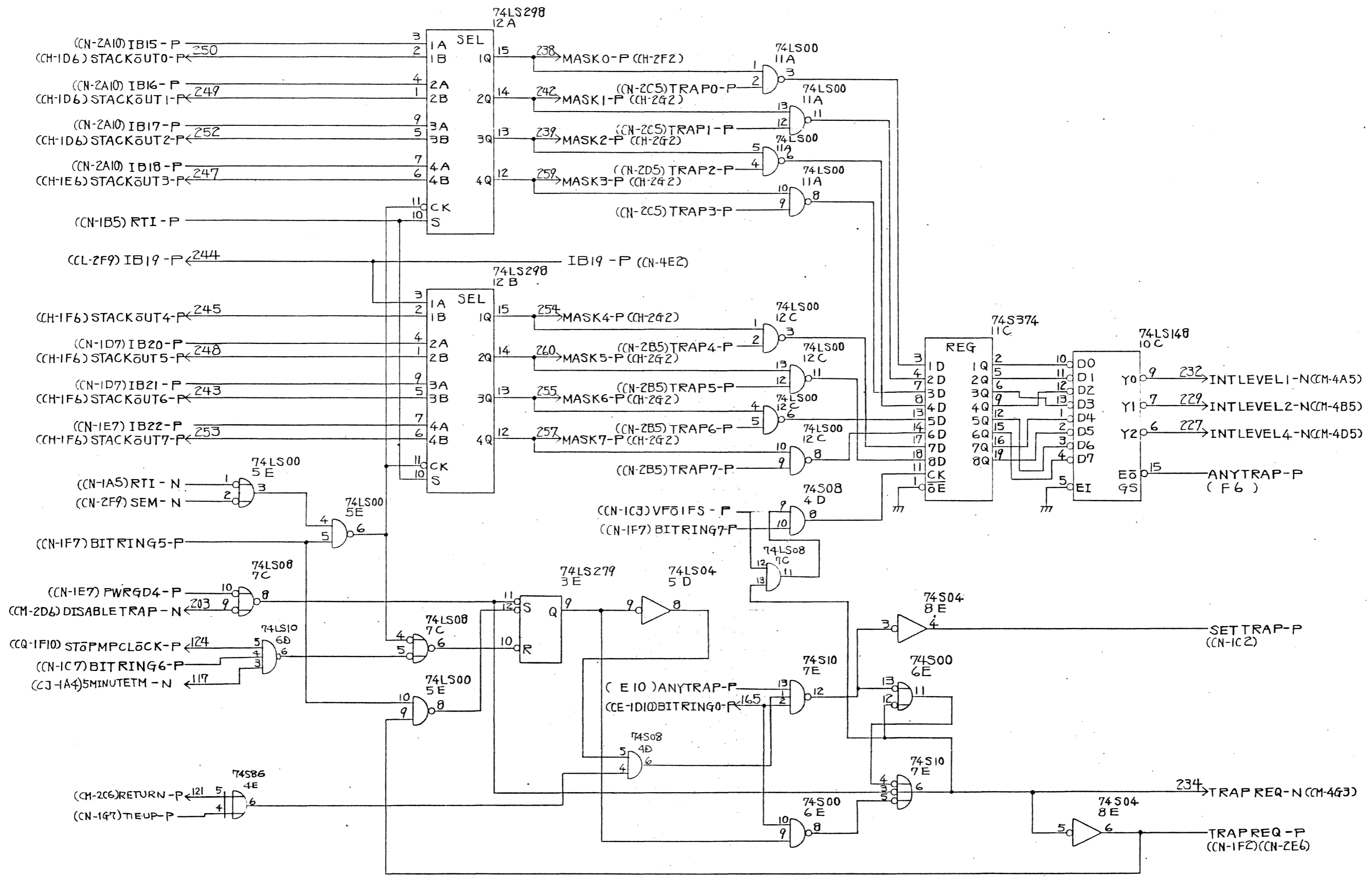
CN-2

P/N REV	TITLE NP370TLR LOGIC DIA	SHEET 2/	DRAWN
		REV 0	CHECK
DRAWING NO NPL-NC-28432		Nippon Peripherals Limited	

047

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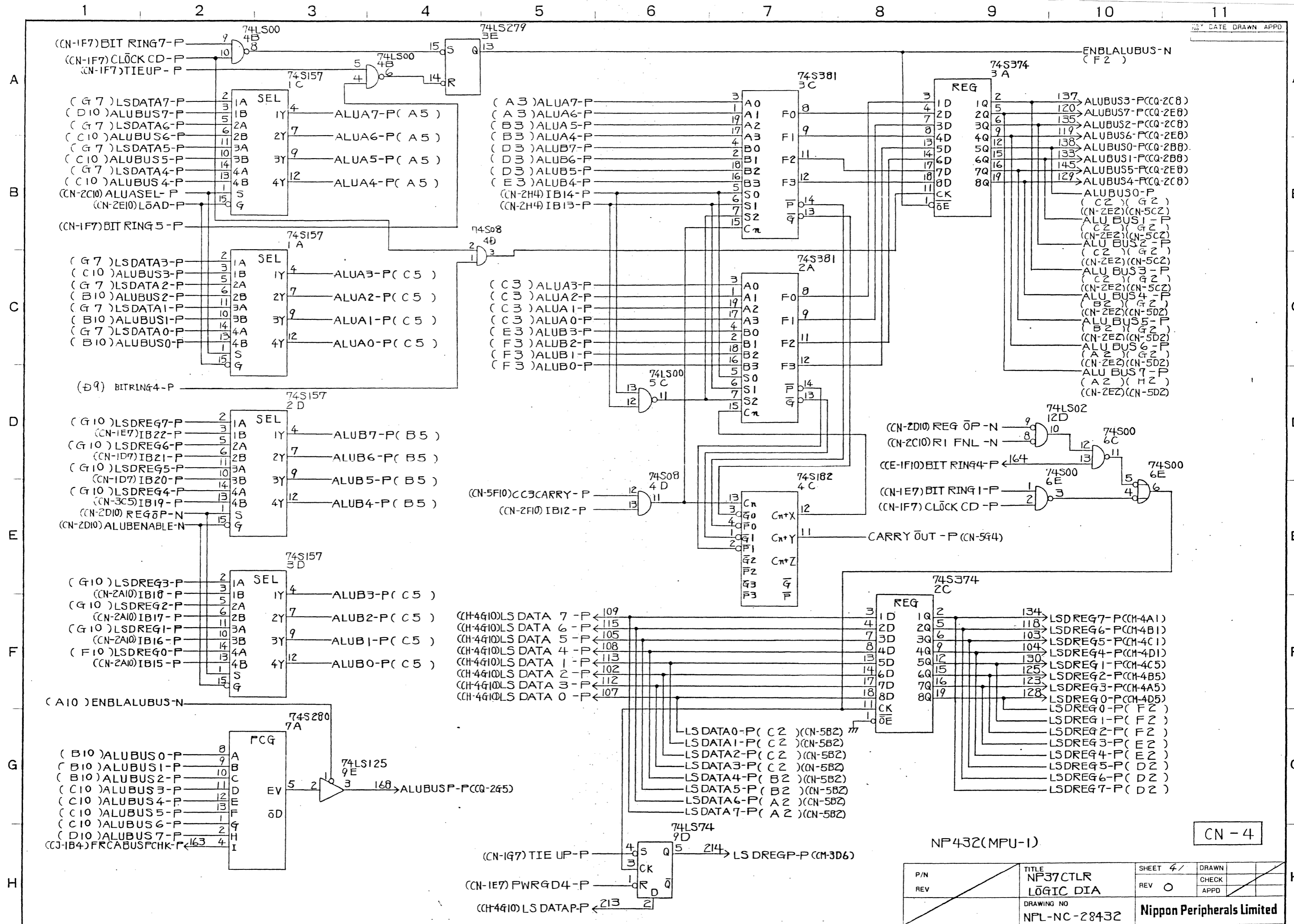
A
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NP432(MFU-1)

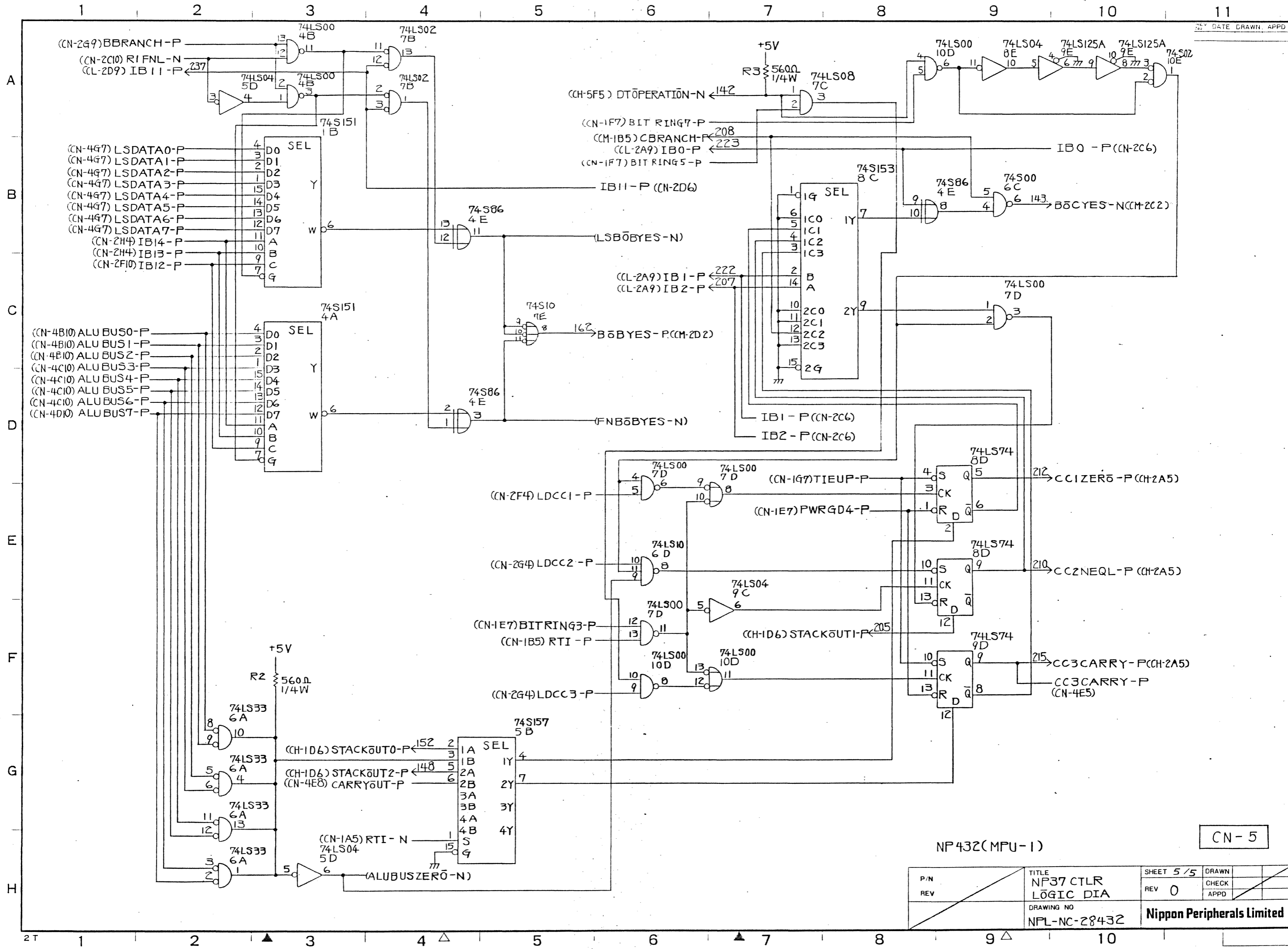
CN-3

P/N	REV	TITLE	SHEET 3/	DRAWN
		NP37CTLR	REV 0	CHECK
		LOGIC DIA	APPD	
DRAWING NO		Nippon Peripherals Limited		
NPL-NC-28432				



CN-4

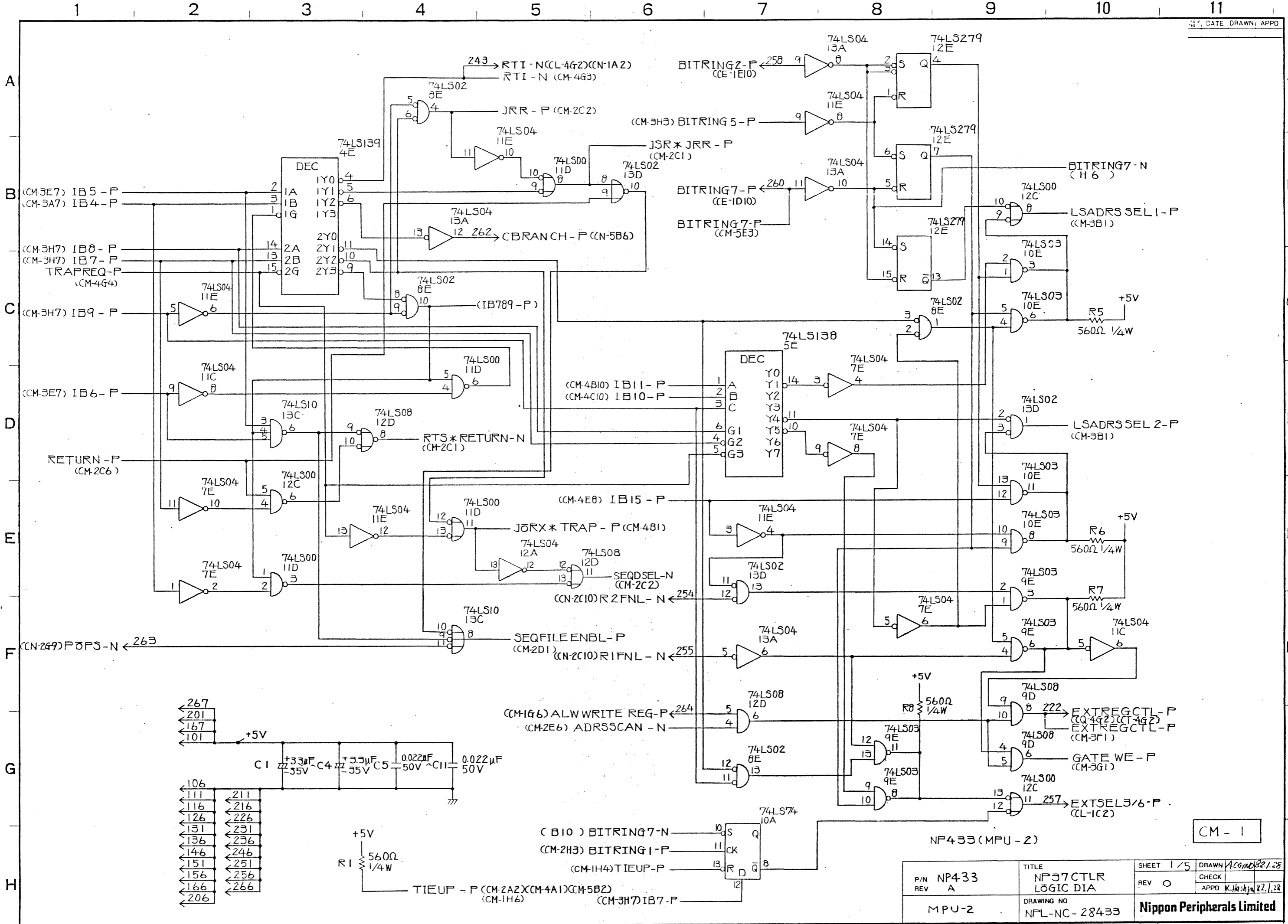
P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 4/	DRAWN
	DRAWING NO NPL-NC-28432	REV 0	CHECK APPD
Nippon Peripherals Limited			



P/N		TITLE NP37 CTLR LOGIC DIA	SHEET 5/5	DRAWN
REV			REV 0	CHECK
DRAWING NO		NPL-NC-28432	Nippon Peripherals Limited	

CN-5

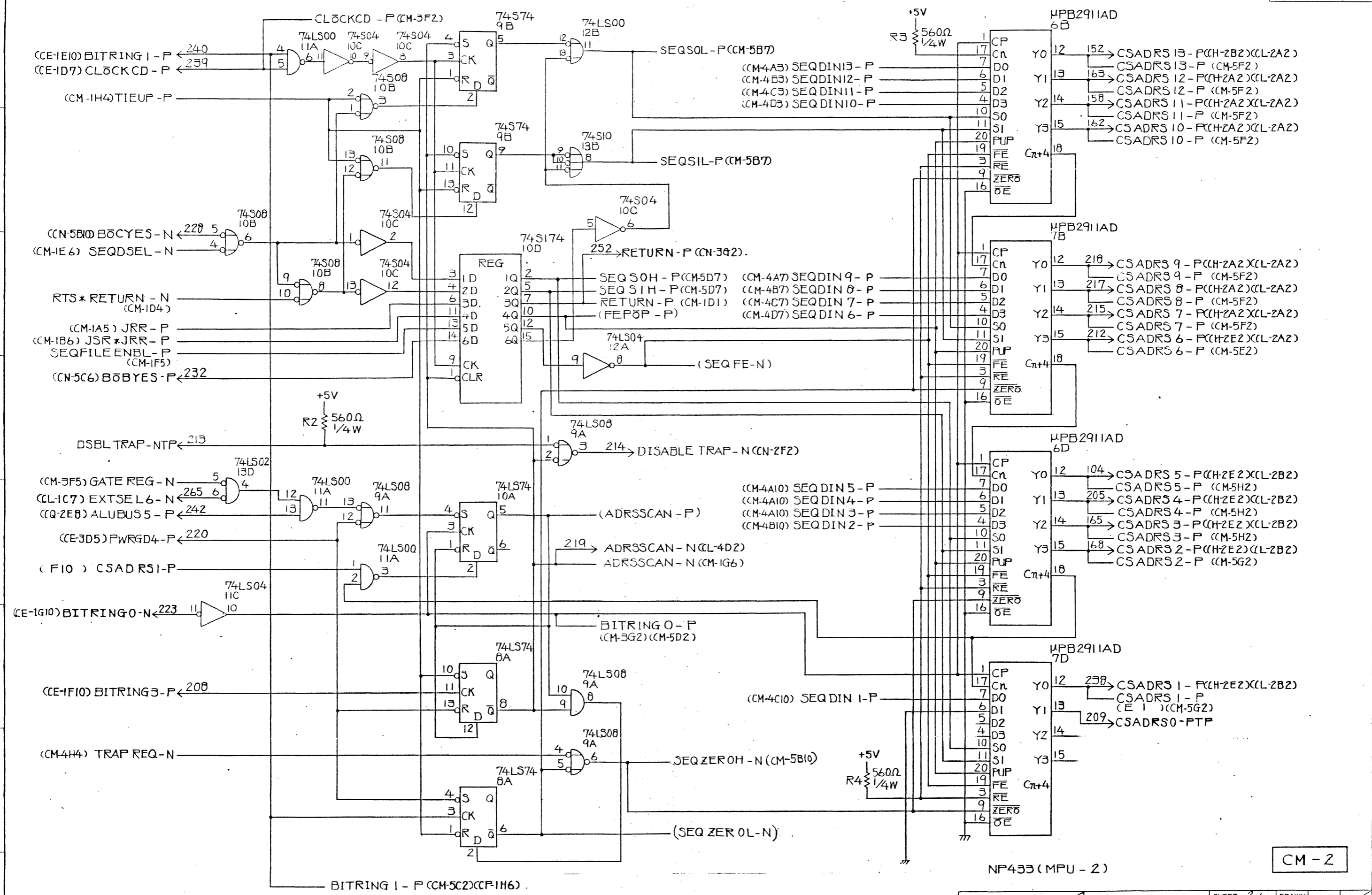
NP432(MPU-1)



267	106
201	111
167	116
101	126
	131
	136
	146
	151
	156
	166
	206
	211
	216
	226
	231
	236
	246
	251
	256
	266

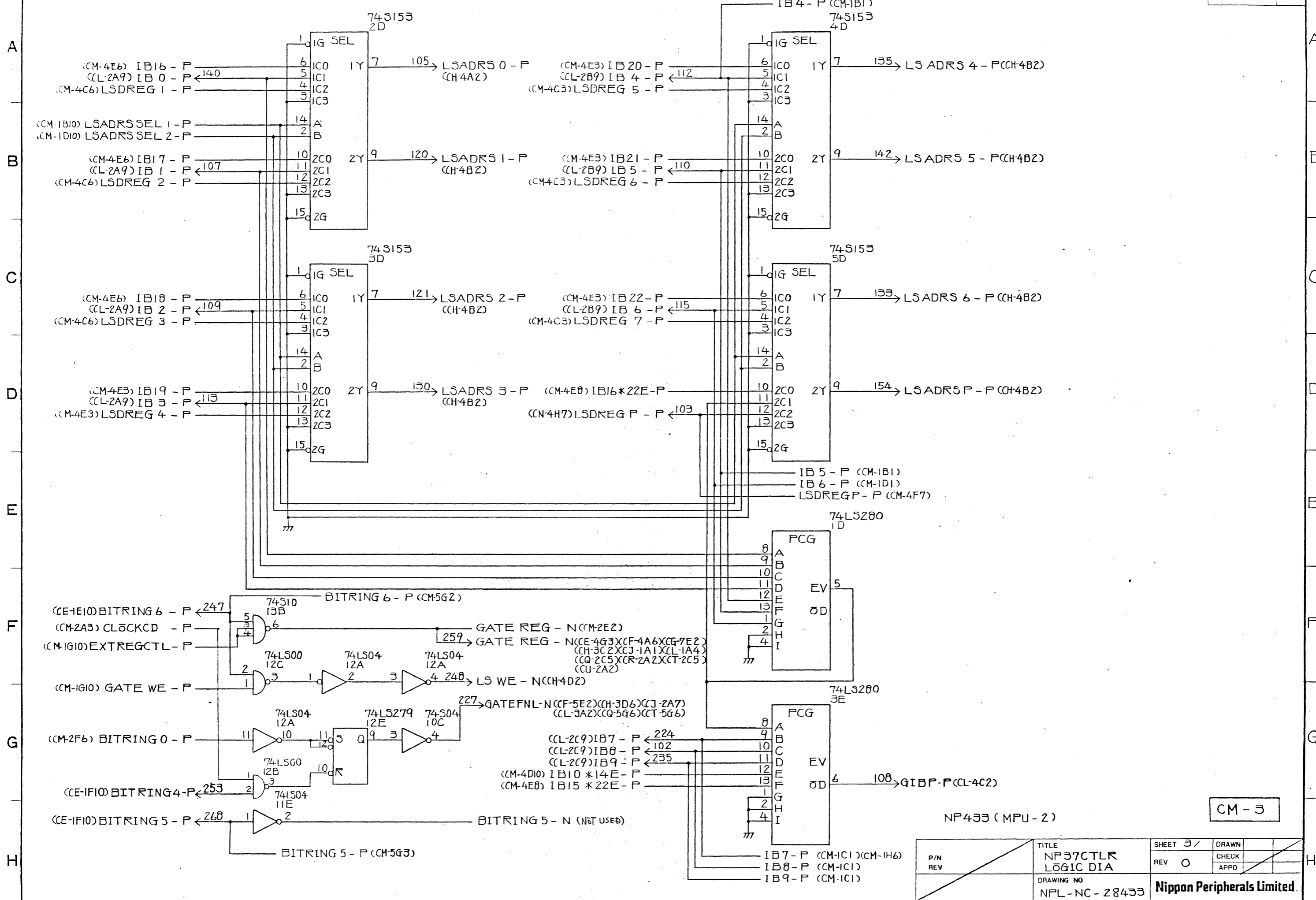
P/N NP433	TITLE NP57CTLR LOGIC DIA	SHEET 1/5	DRAWN ACGM/22.28
REV A	DRAWING NO NPL-NC-28433	REV 0	CHECK APPD K.Hishin 22.28
MPU-2	Nippon Peripherals Limited		

CM-1



CM-2

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 2/	DRAWN	
		REV 0	CHECK	
DRAWING NO NPL-NC-28433		Nippon Peripherals Limited		

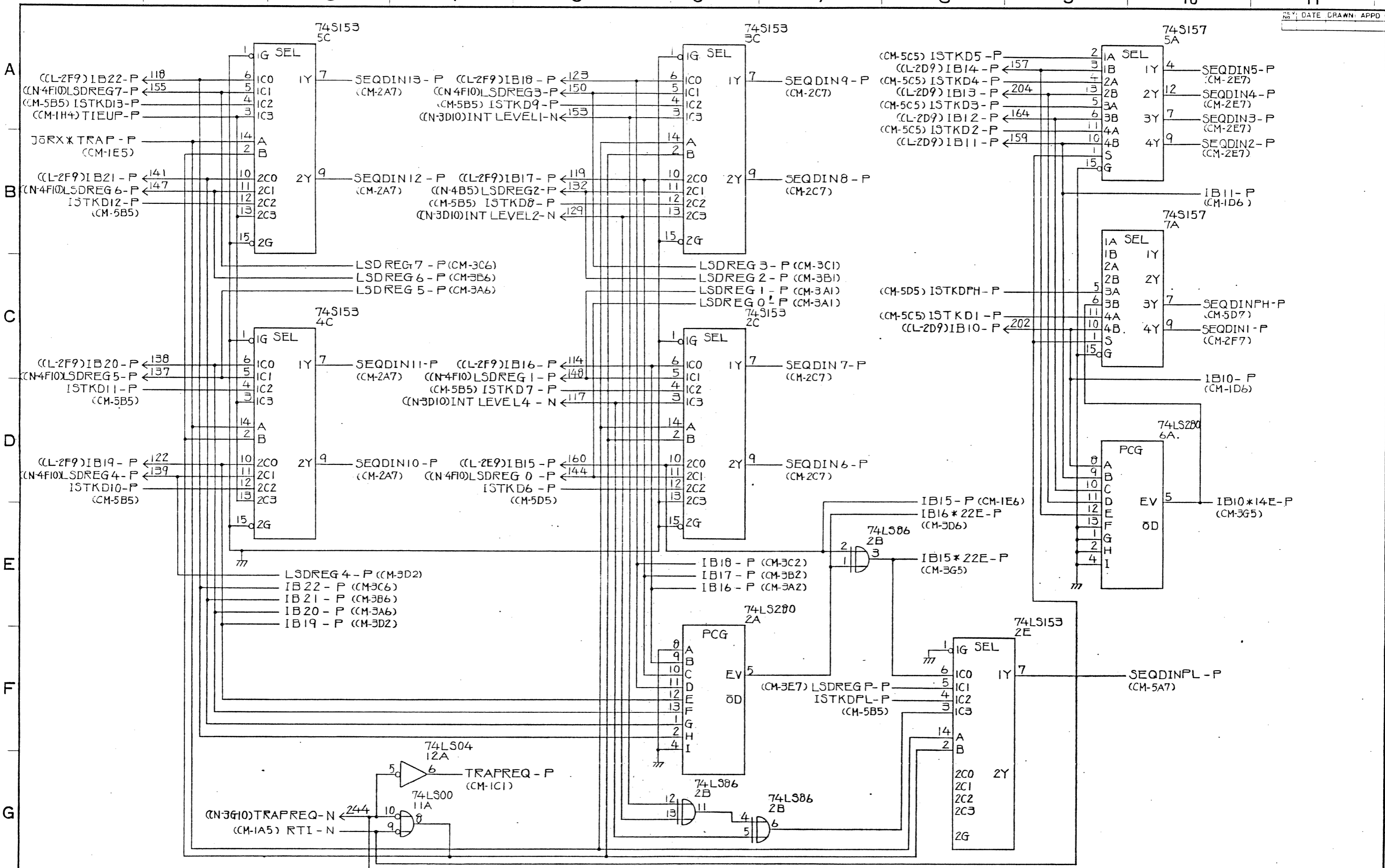


CM-3

NP433 (MPU-2)

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 3/	DRAWN
		REV 0	CHECK APPD
DRAWING NO NPL-NC-28433		Nippon Peripherals Limited	

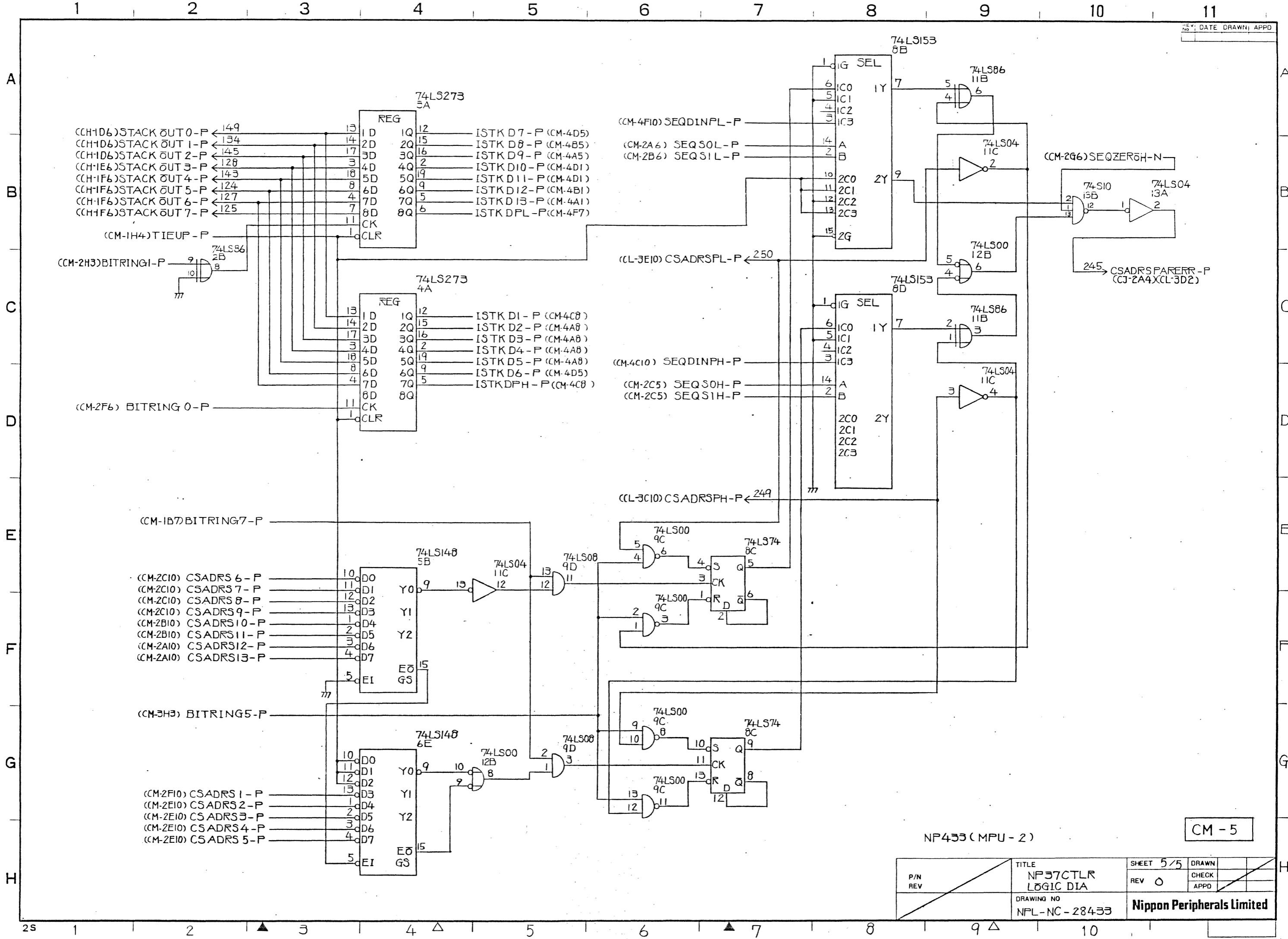
9-7



NP433 (MPU - 2)

CM - 4

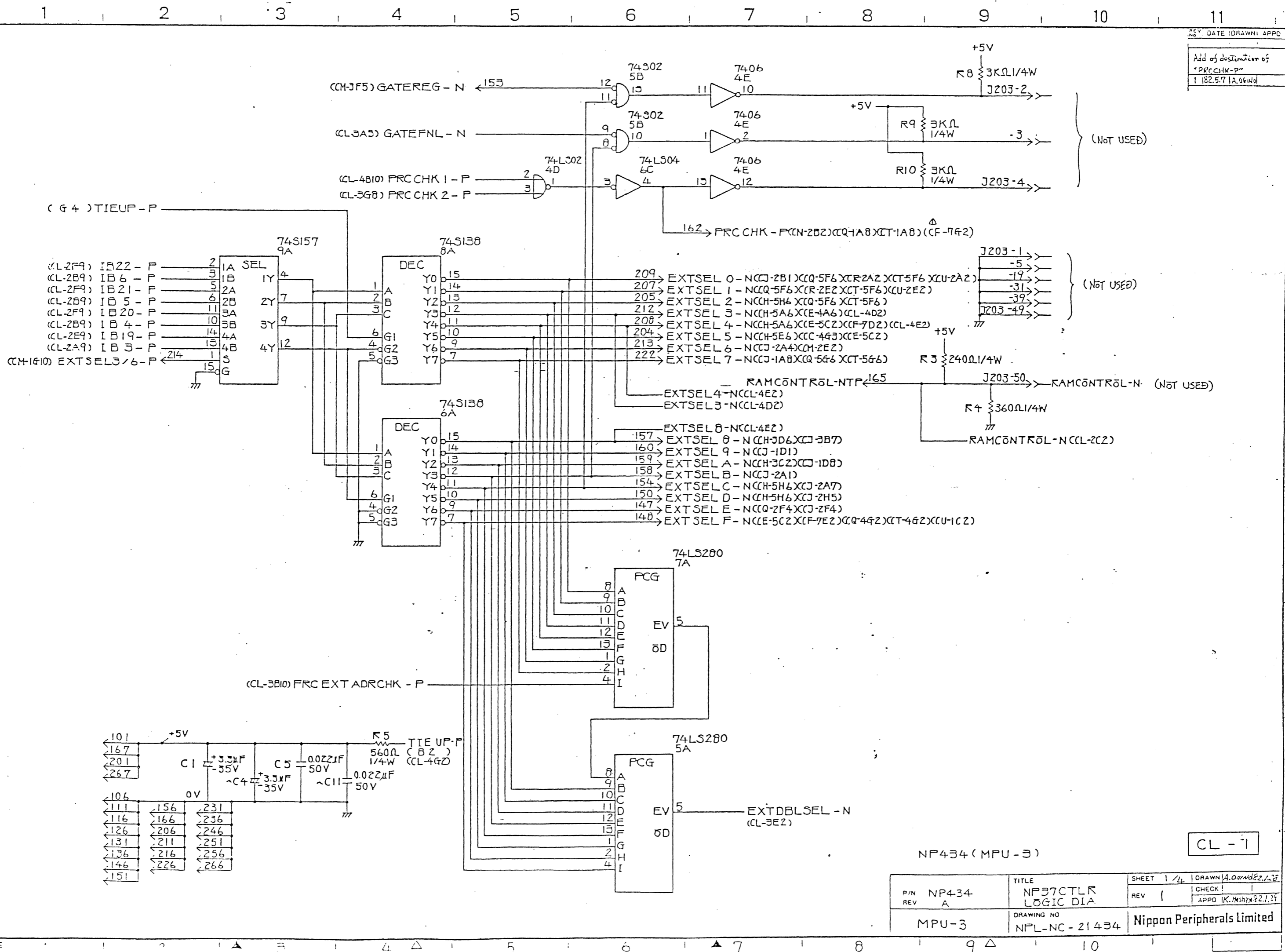
P/N REV	TITLE	SHEET 4/	DRAWN
	NP37CLR LOGIC DIA	REV 0	CHECK
	DRAWING NO	APPD	
NPL-NC-28433		Nippon Peripherals Limited	



NP433 (MPU-2)

CM-5

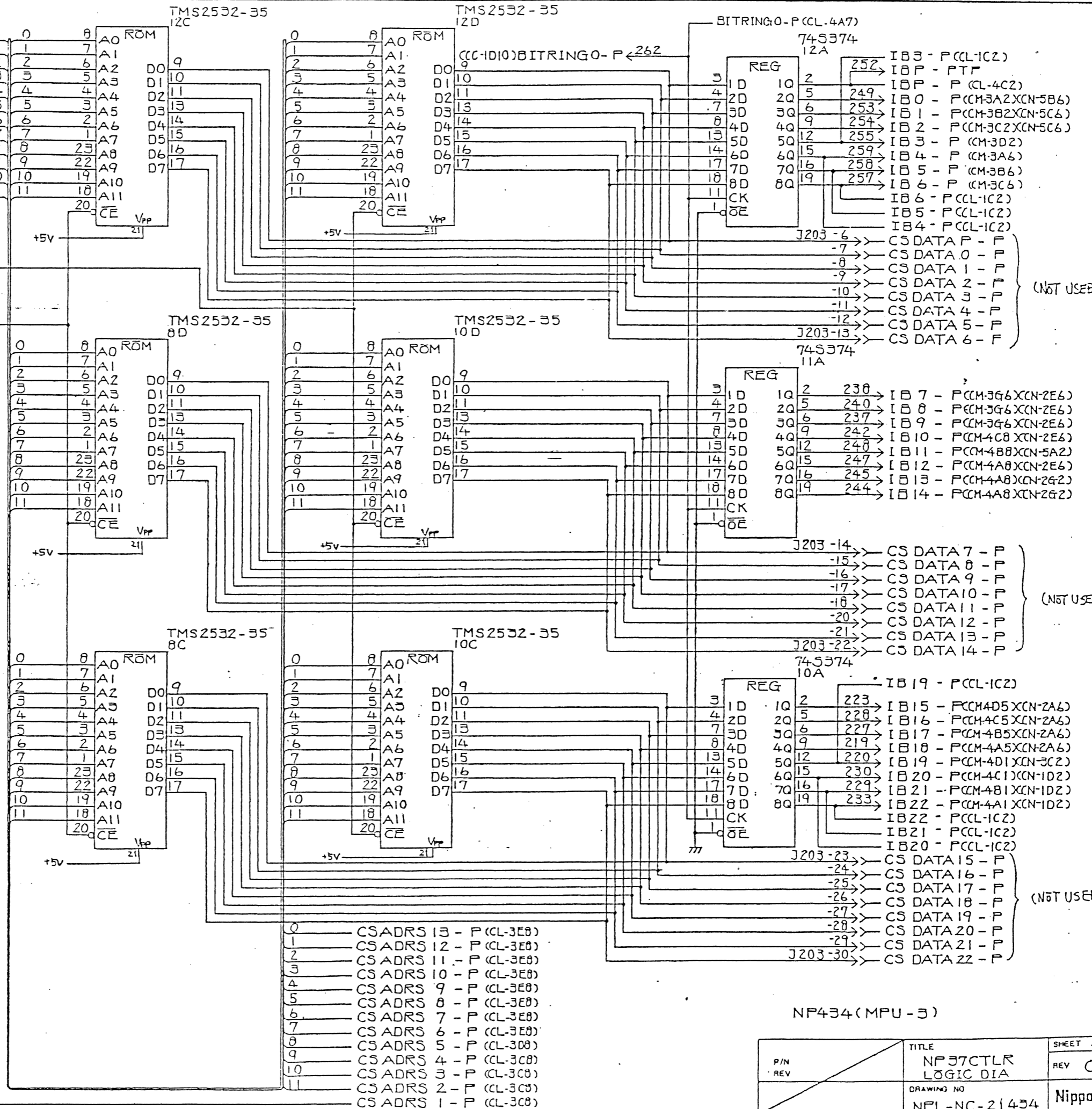
P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 5/5	DRAWN
	DRAWING NO NPL-NC-28433	REV 0	CHECK APPD
		Nippon Peripherals Limited	



MPU-3		DRAWING NO NPL-NC-21434		Nippon Peripherals Limited	
P/N REV	NP434 A	TITLE NP37CTLR LOGIC DIA	SHEET 1/4	DRAWN JA.06Wol	APPD JK.Hshjx22.1.34

CL-1

(CM-2A10)CSADRS13 - P ← 218
 (CM-2A10)CSADRS12 - P ← 217
 (CM-2A10)CSADRS11 - P ← 232
 (CM-2B10)CSADRS10 - P ← 202
 (CM-2C10)CSADRS9 - P ← 224
 (CM-2C10)CSADRS8 - P ← 250
 (CM-2C10)CSADRS7 - P ← 260
 (CM-2C10)CSADRS6 - P ← 235
 (CM-2E10)CSADRS5 - P ← 264
 (CM-2E10)CSADRS4 - P ← 215
 (CM-2E10)CSADRS3 - P ← 265
 (CM-2E10)CSADRS2 - P ← 268
 (CM-2F10)CSADRS1 - P ← 225



RAMCONTROL-N (CL-109)

0 CSADRS13 - P (CL-3E8)
 1 CSADRS12 - P (CL-3E8)
 2 CSADRS11 - P (CL-3E8)
 3 CSADRS10 - P (CL-3E8)
 4 CSADRS9 - P (CL-3E8)
 5 CSADRS8 - P (CL-3E8)
 6 CSADRS7 - P (CL-3E8)
 7 CSADRS6 - P (CL-3E8)
 8 CSADRS5 - P (CL-3D8)
 9 CSADRS4 - P (CL-3C8)
 10 CSADRS3 - P (CL-3C8)
 11 CSADRS2 - P (CL-3C8)
 CSADRS1 - P (CL-3C8)

NF434(MPU-3)

CL-2

P/N REV	TITLE	SHEET 2 /	DRAWN
	NF37CTLR LOGIC DIA	REV 0	CHECK
DRAWING NO		APPRO	
NFL-NC-21434		Nippon Peripherals Limited	

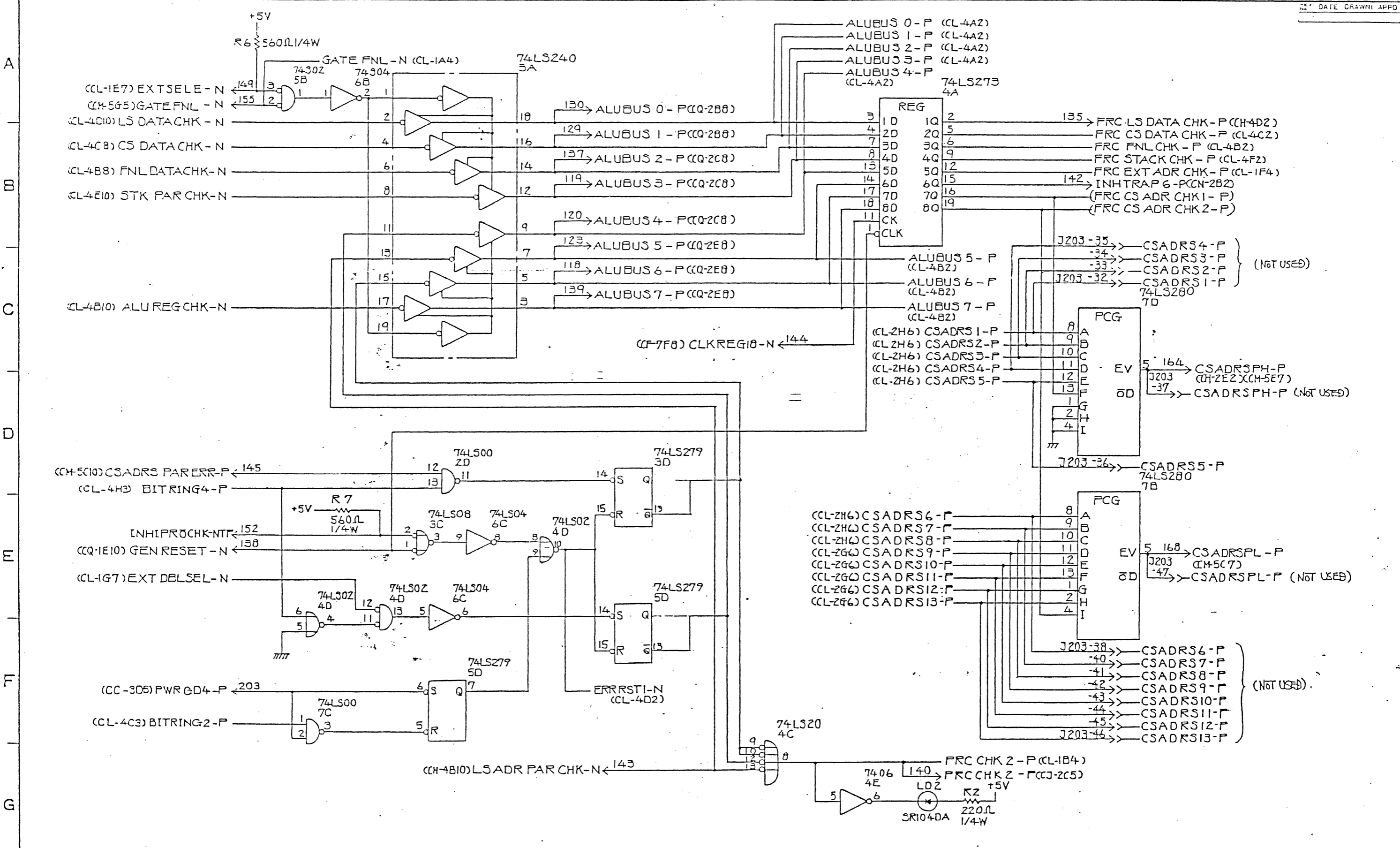
(NOT USED)

(NOT USED)

(NOT USED)

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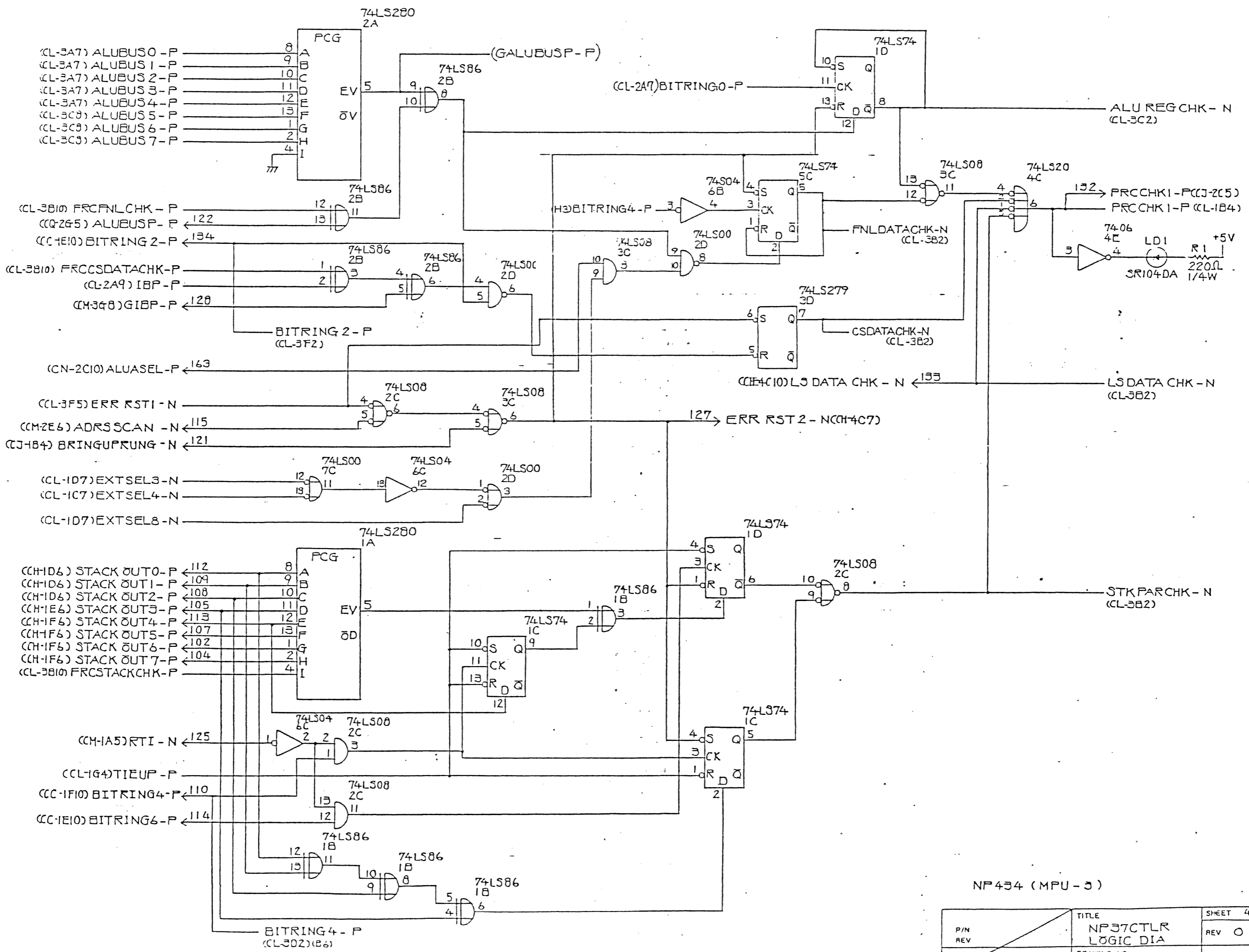
CL-3

NP434 (MPU-3)

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 3/	DRAWN
		REV 0	CHECK
DRAWING NO NPL-NC-21434		APPO	
		Nippon Peripherals Limited	

1 2 3 4 5 6 7 8 9 10 11

A B C D E F G H

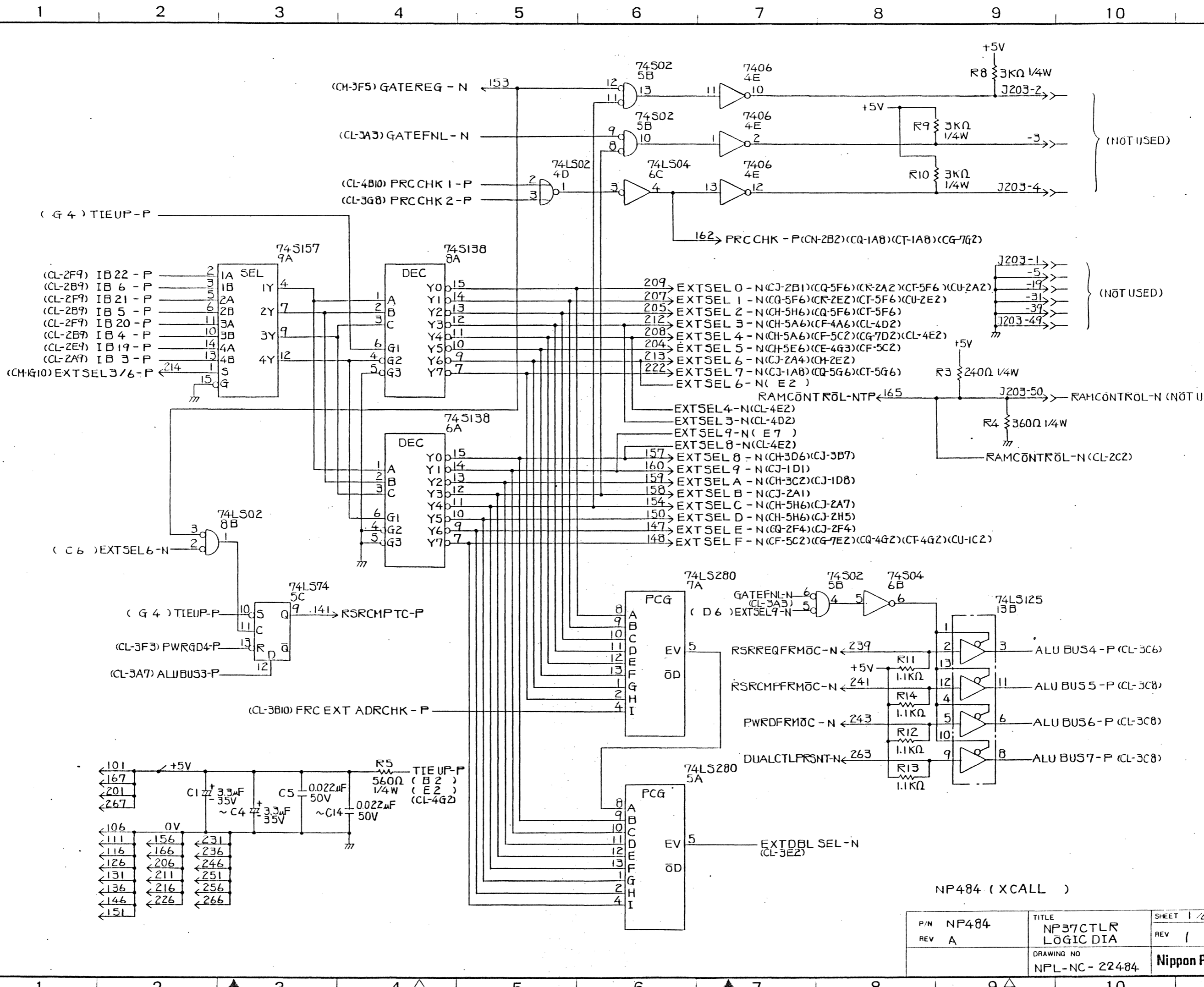


NP434 (MPU-3)

CL-4

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 4/4	DRAWN
		REV 0	CHECK
DRAWING NO NFL-NC-21434		Nippon Peripherals Limited.	

25 1 2 3 4 5 6 7 8 9 10



(NOT USED)

(NOT USED)

RAMCONTROL-N (NOT USED)

CL-1

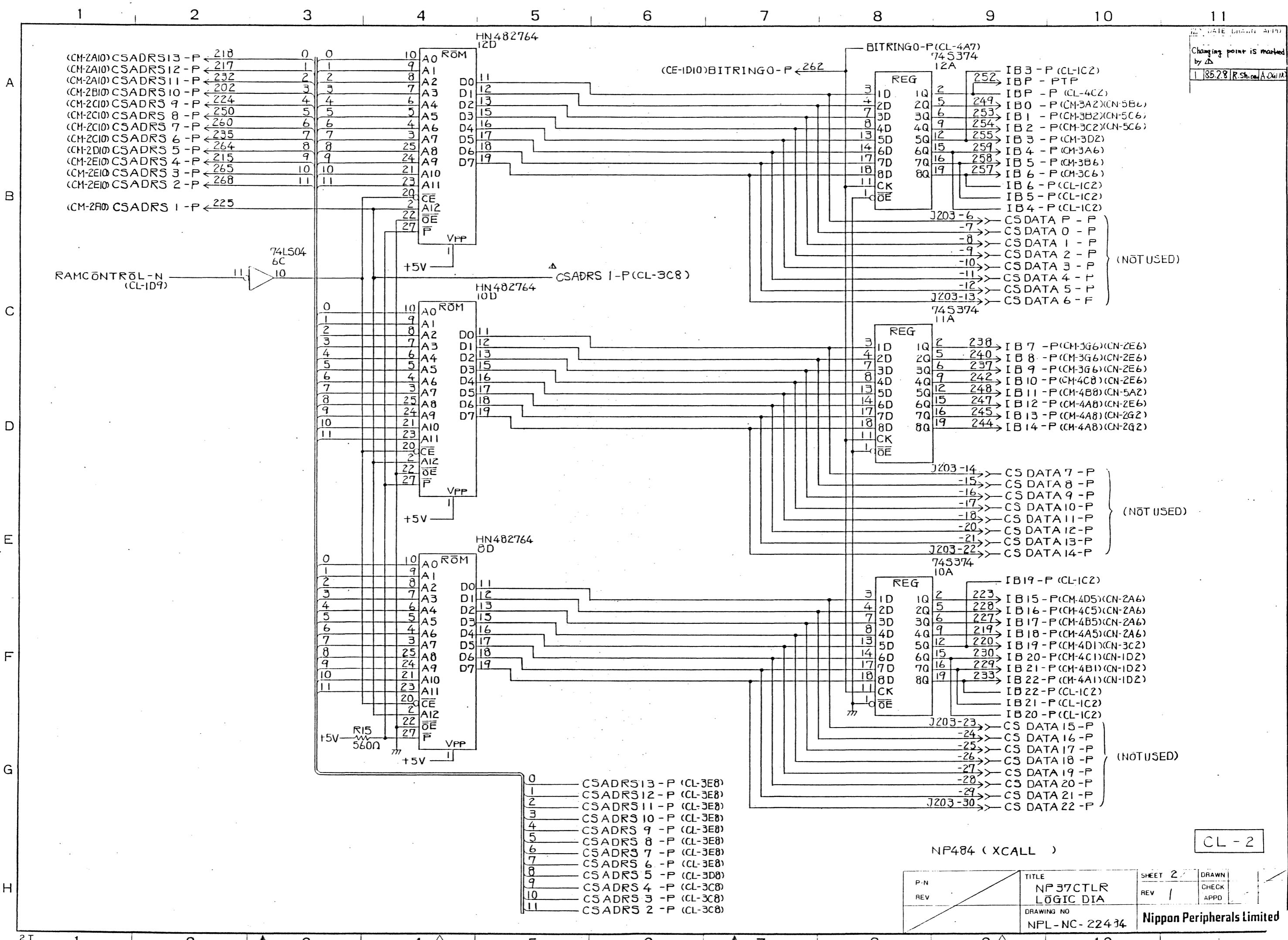
NP484 (XCALL)

P/N	NP484	TITLE	NP37CTLR LOGIC DIA	SHEET	1/4	DRAWN	Shino	69.11.26
REV	A	CHECK	APPD	REV	1	CHECK	Shino	70.11.27
DRAWING NO			NPL-NC-22484			Nippon Peripherals Limited		

67

2T

DATE: 1985.2.8
 Changing point is marked by Δ
 185.28 R.Shimada A.Ohira



- 0 CSADRS13 -P (CL-3E8)
- 1 CSADRS12 -P (CL-3E8)
- 2 CSADRS11 -P (CL-3E8)
- 3 CSADRS10 -P (CL-3E8)
- 4 CSADRS9 -P (CL-3E8)
- 5 CSADRS8 -P (CL-3E8)
- 6 CSADRS7 -P (CL-3E8)
- 7 CSADRS6 -P (CL-3E8)
- 8 CSADRS5 -P (CL-3D8)
- 9 CSADRS4 -P (CL-3C8)
- 10 CSADRS3 -P (CL-3C8)
- 11 CSADRS2 -P (CL-3C8)

NP484 (XCALL)

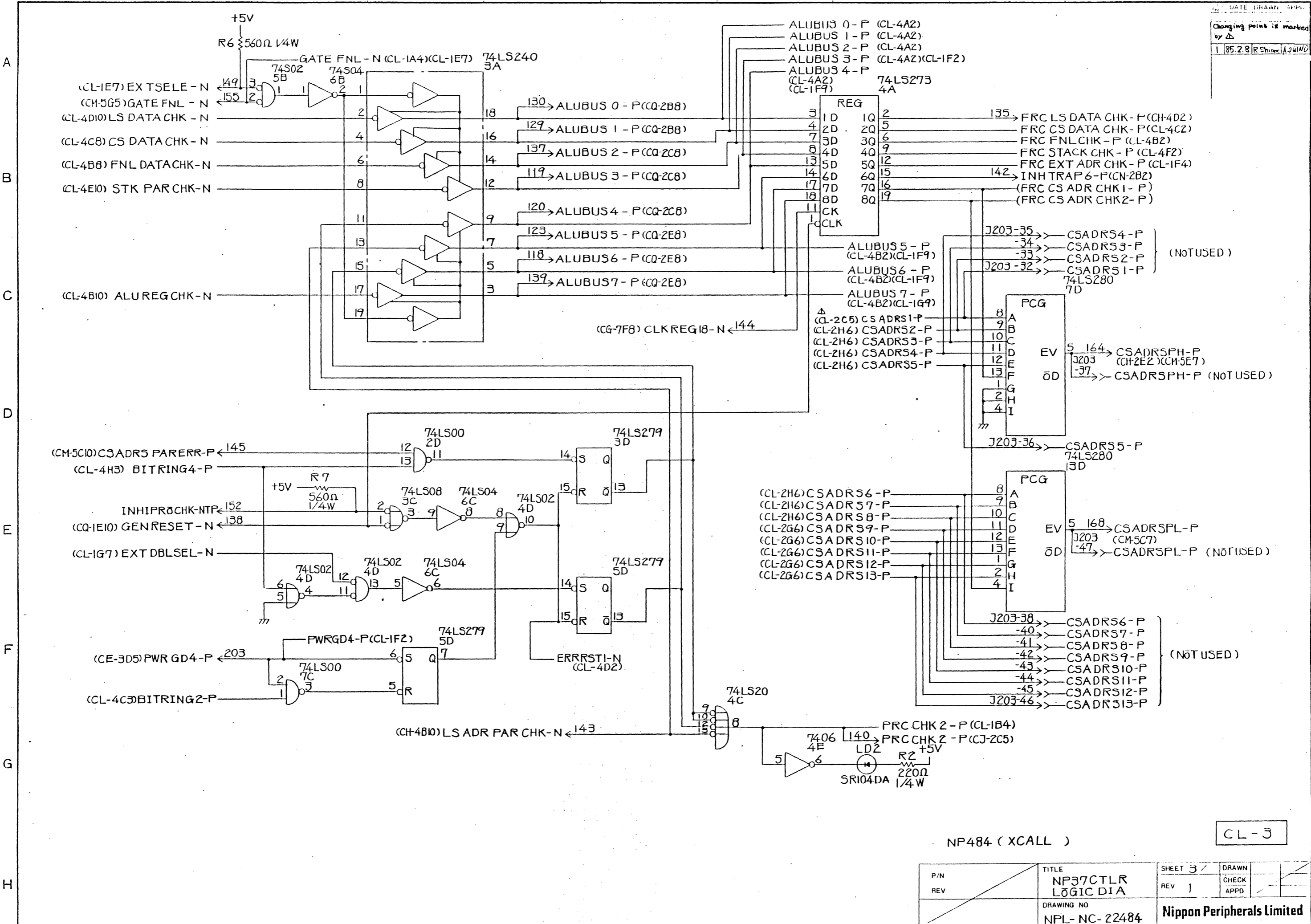
CL-2

P-N	TITLE	SHEET 2	DRAWN
REV	NP37CTLR LOGIC DIA	REV 1	CHECK APPD
DRAWING NO		Nippon Peripherals Limited	
NPL-NC-22434			

50

2T

DATE DRAWN: APPD
Changing points if marked by Δ
1 85.2.8 R.Sharma A.0410



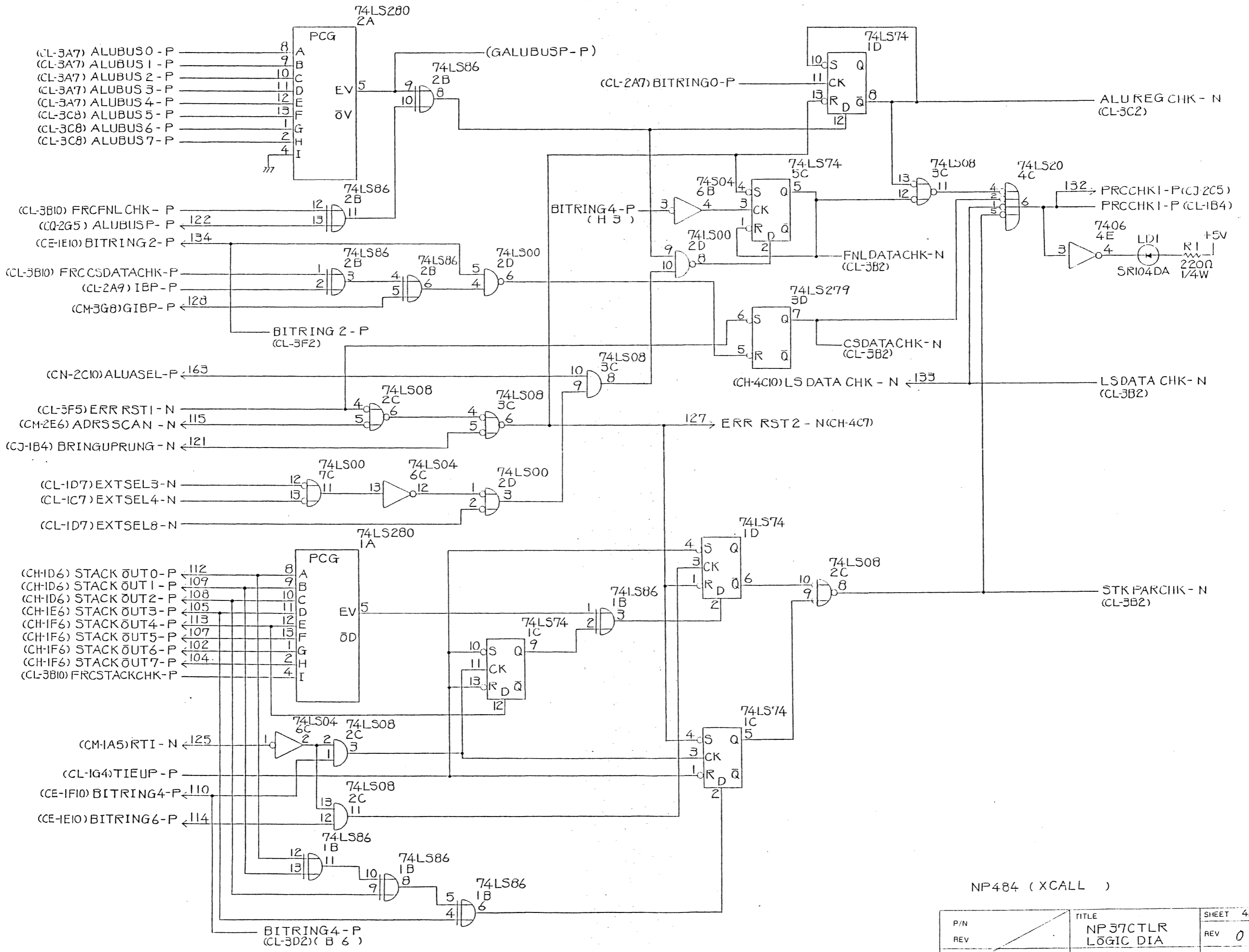
NP484 (XCALL)

CL-3

P/N	REV	TITLE	SHEET	DRAWN
		NP37CTLR L0GIC DIA	3 /	
		DRAWING NO	REV	CHECK
		NPL-NC-22484	1	APPD
Nippon Peripherals Limited				

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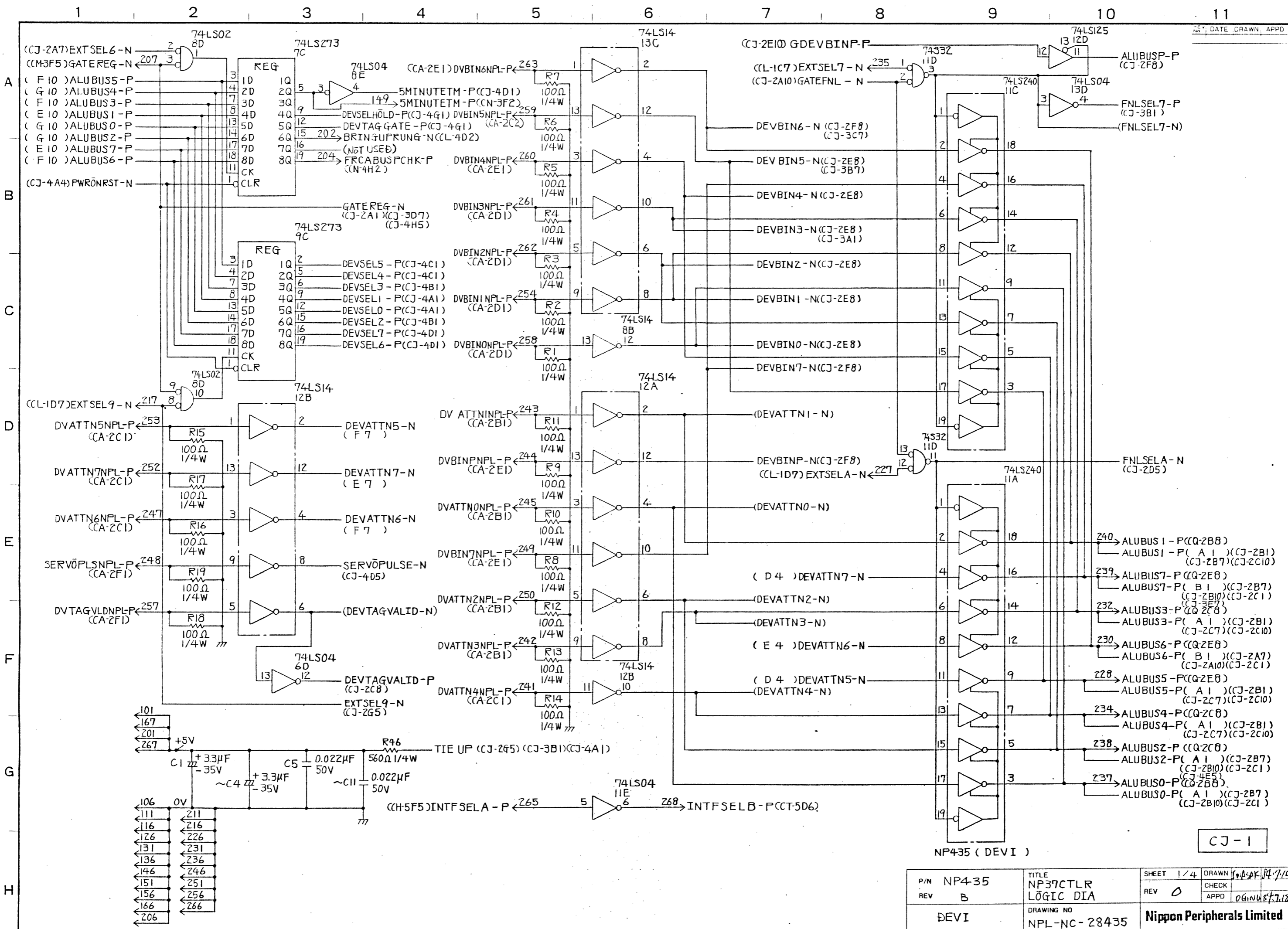


CL-4

NP484 (XCALL)

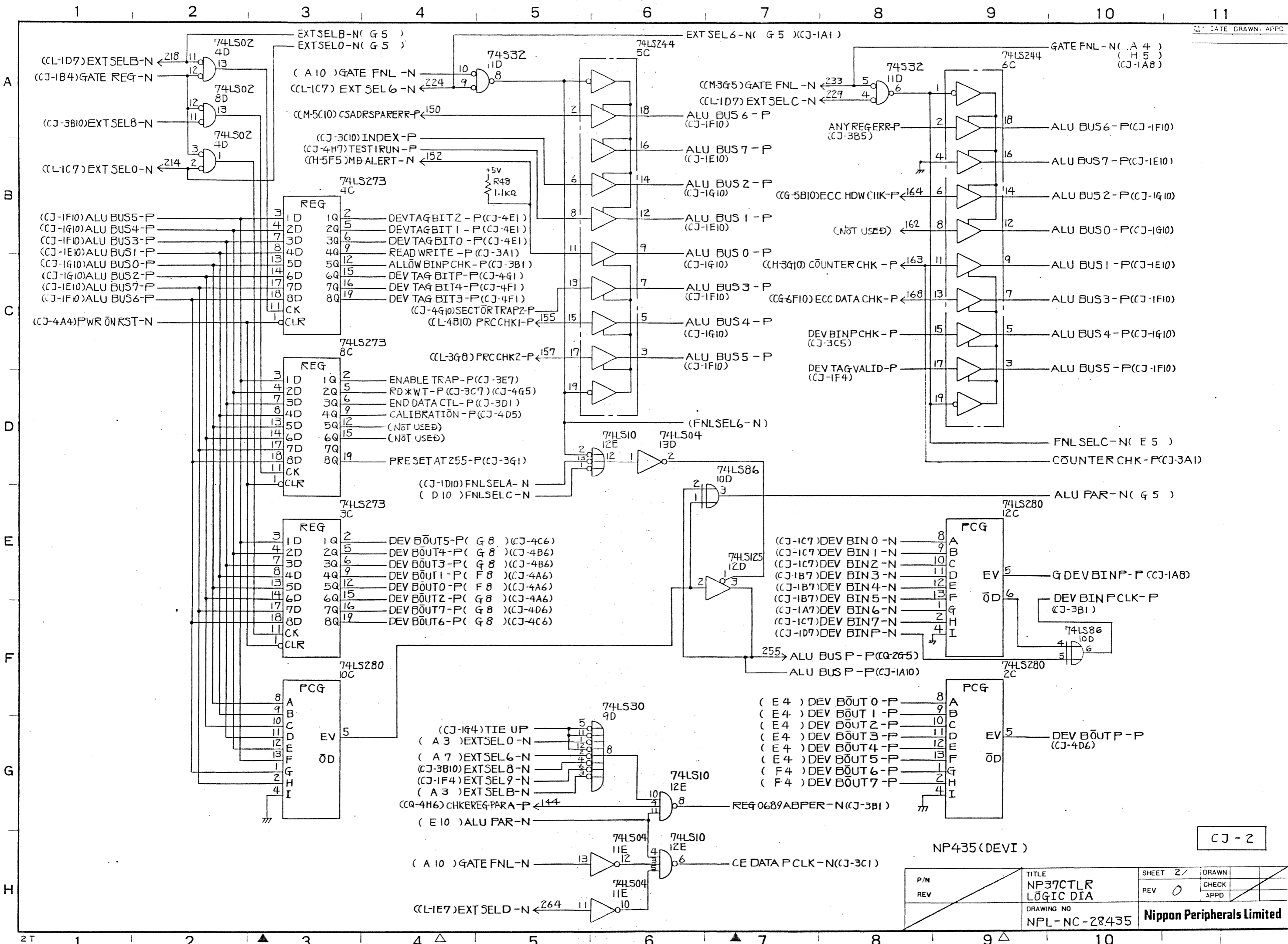
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		NP37CTLR LOGIC DIA	4/4	
		DRAWING NO	REV	CHECK
		NPL-NC-22484	0	APPD
Nippon Peripherals Limited				

2T 1 2 3 4 5 6 7 8 9 10



CJ-1

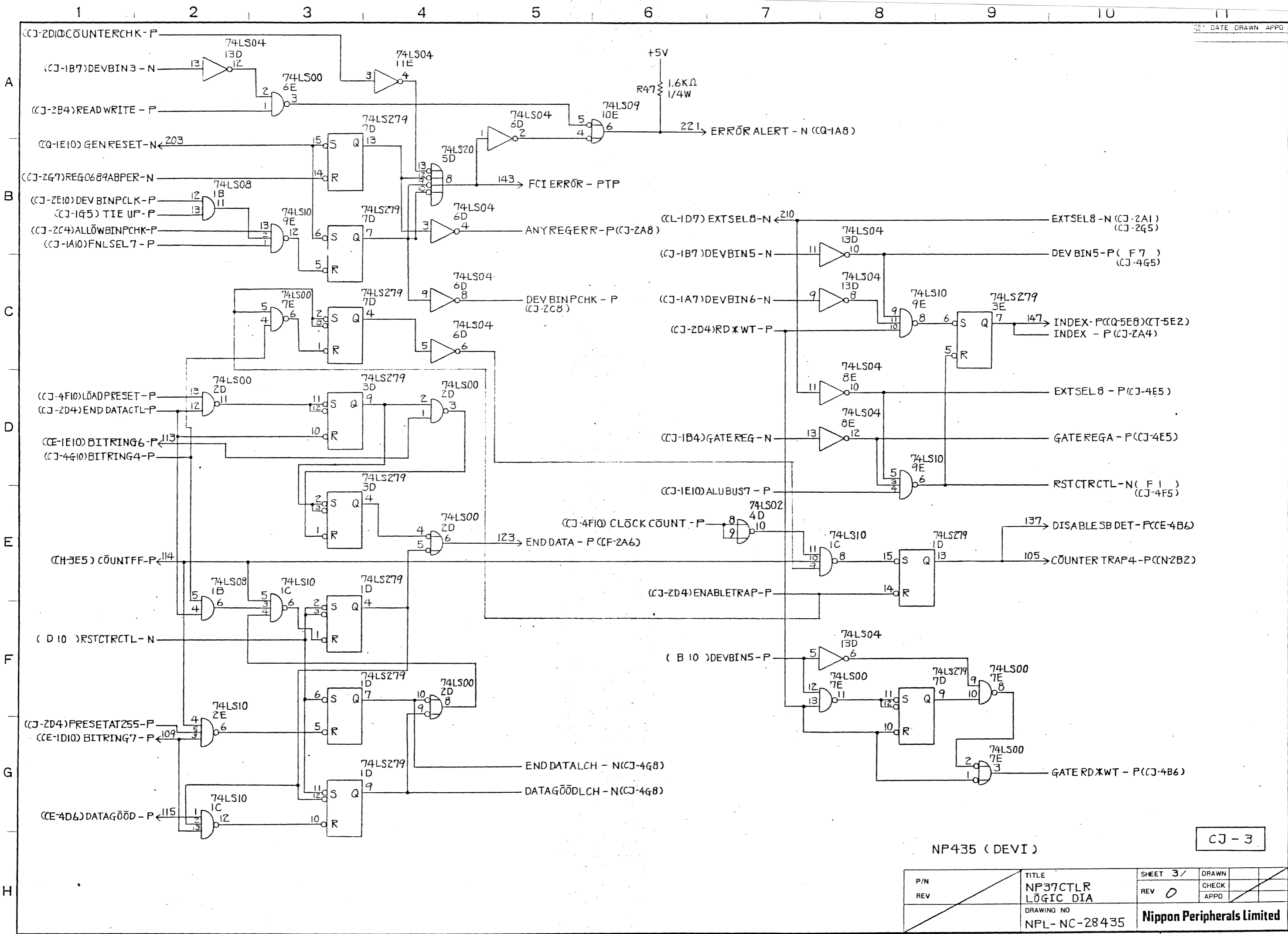
P/N	NP435	TITLE	NP37CTLR LOGIC DIA	SHEET	1/4	DRAWN	10.10.71
REV	B	CHECK		REV	0	APPD	06.10.71
DEVI		DRAWING NO	NPL-NC-28435	Nippon Peripherals Limited			



CJ-2

P/N		TITLE NP37CTLR LOGIC DIA DRAWING NO NPL-NC-28435	SHEET 2/	DRAWN
REV			REV 0	CHECK APPD
		Nippon Peripherals Limited		

54

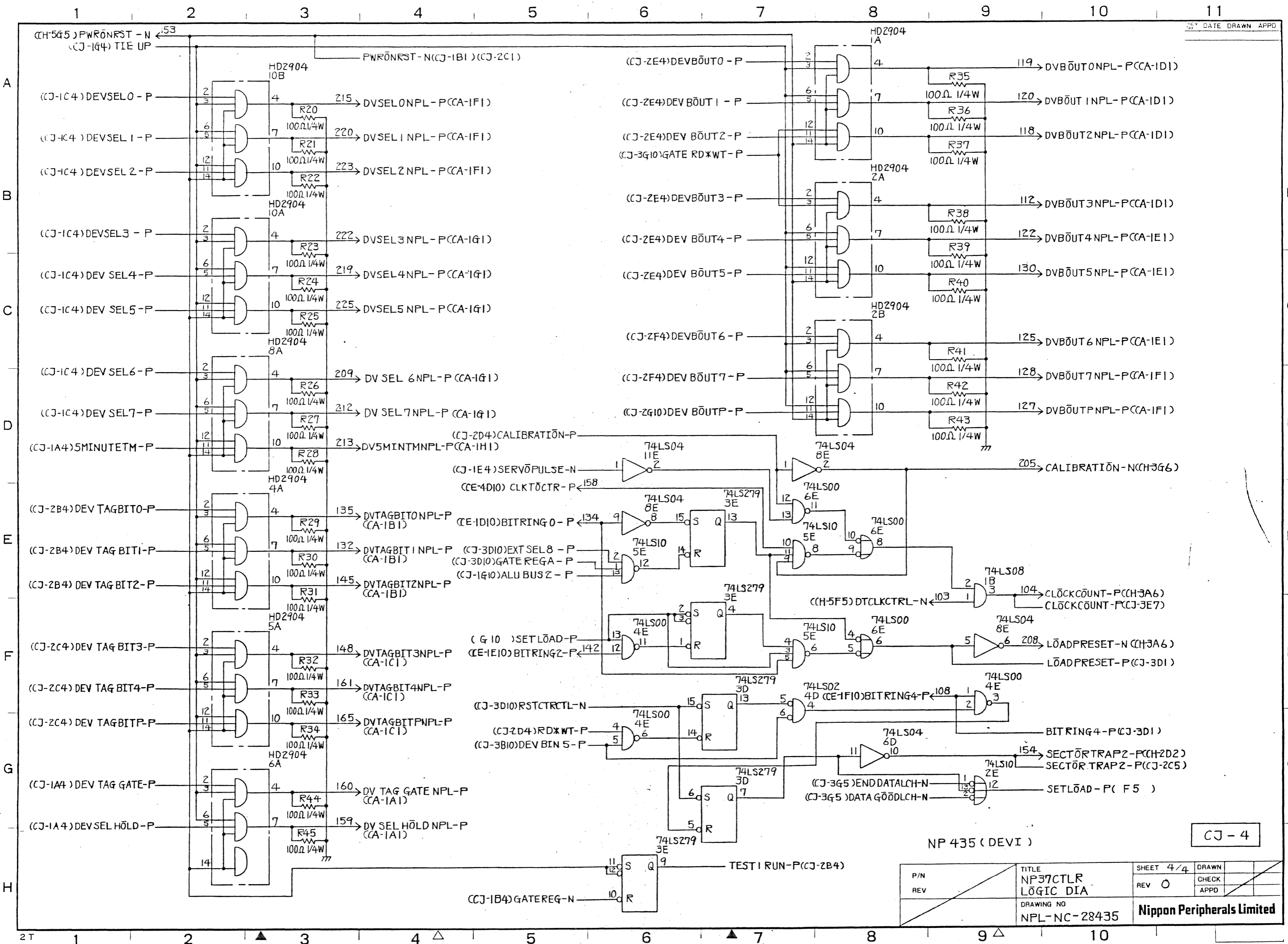


NP435 (DEVI)

CJ-3

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 3/	DRAWN	
		REV 0	CHECK	
DRAWING NO NPL-NC-28435		Nippon Peripherals Limited		

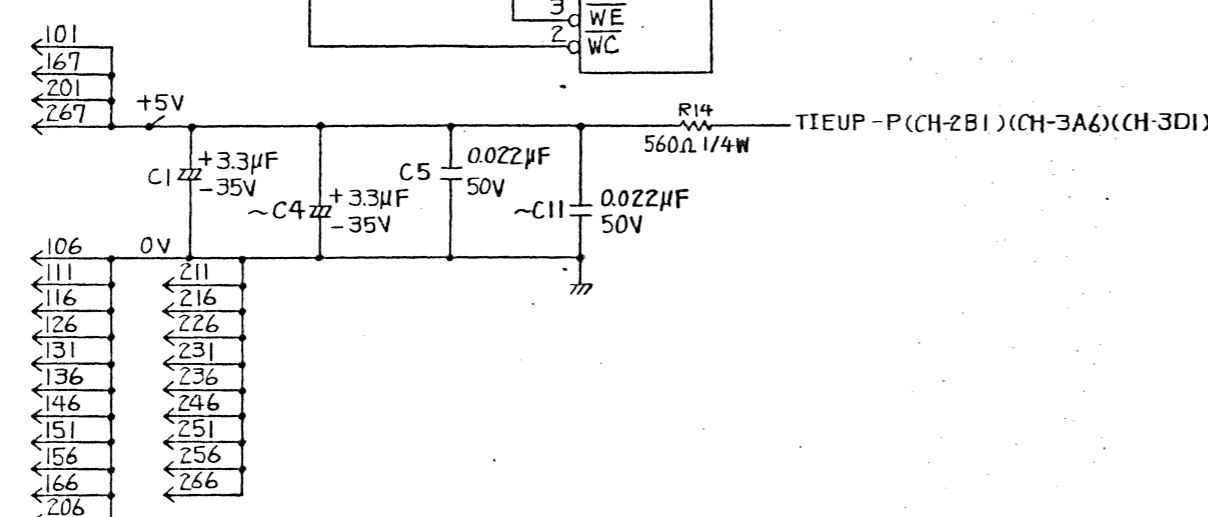
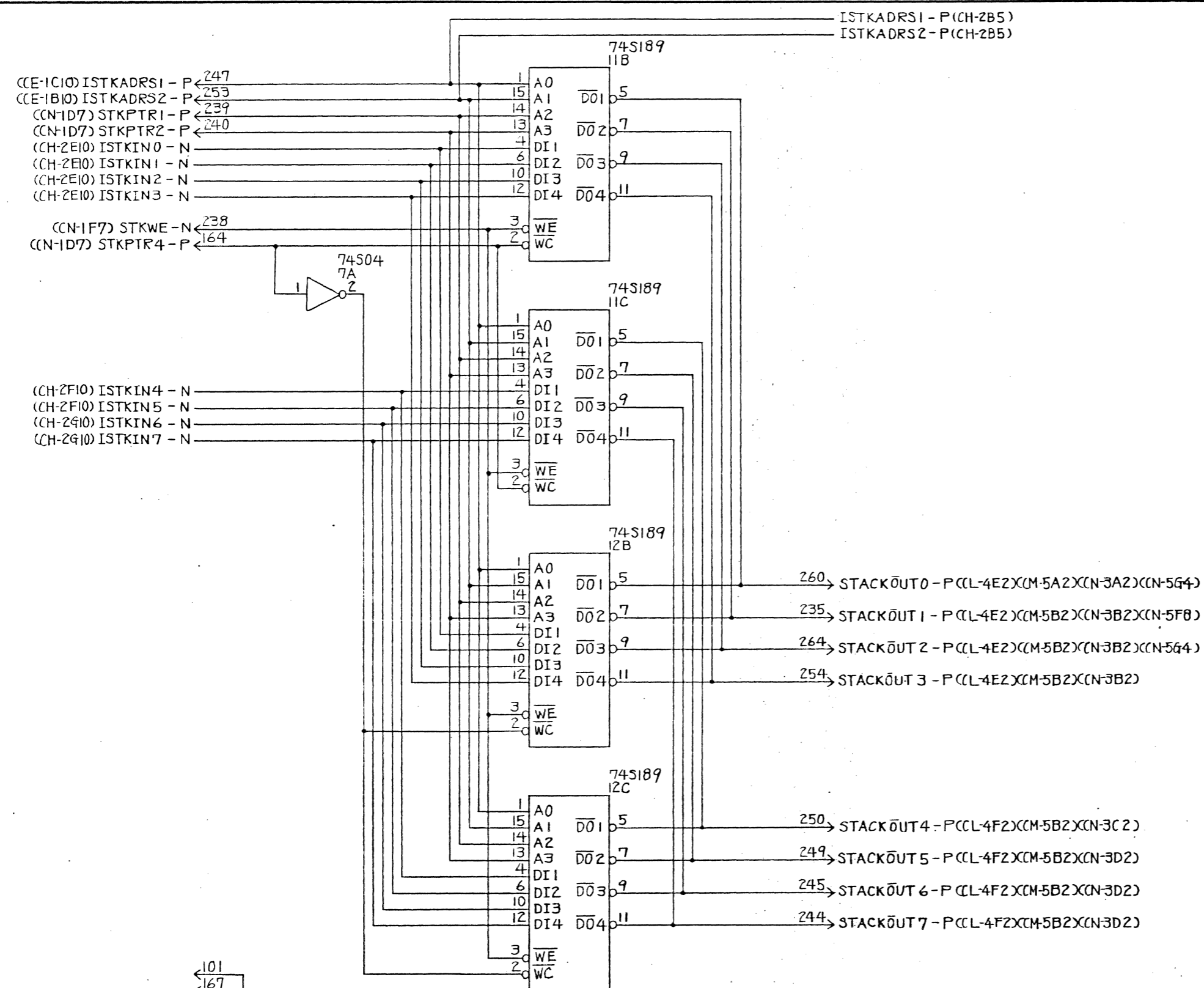
55



56

CJ-4

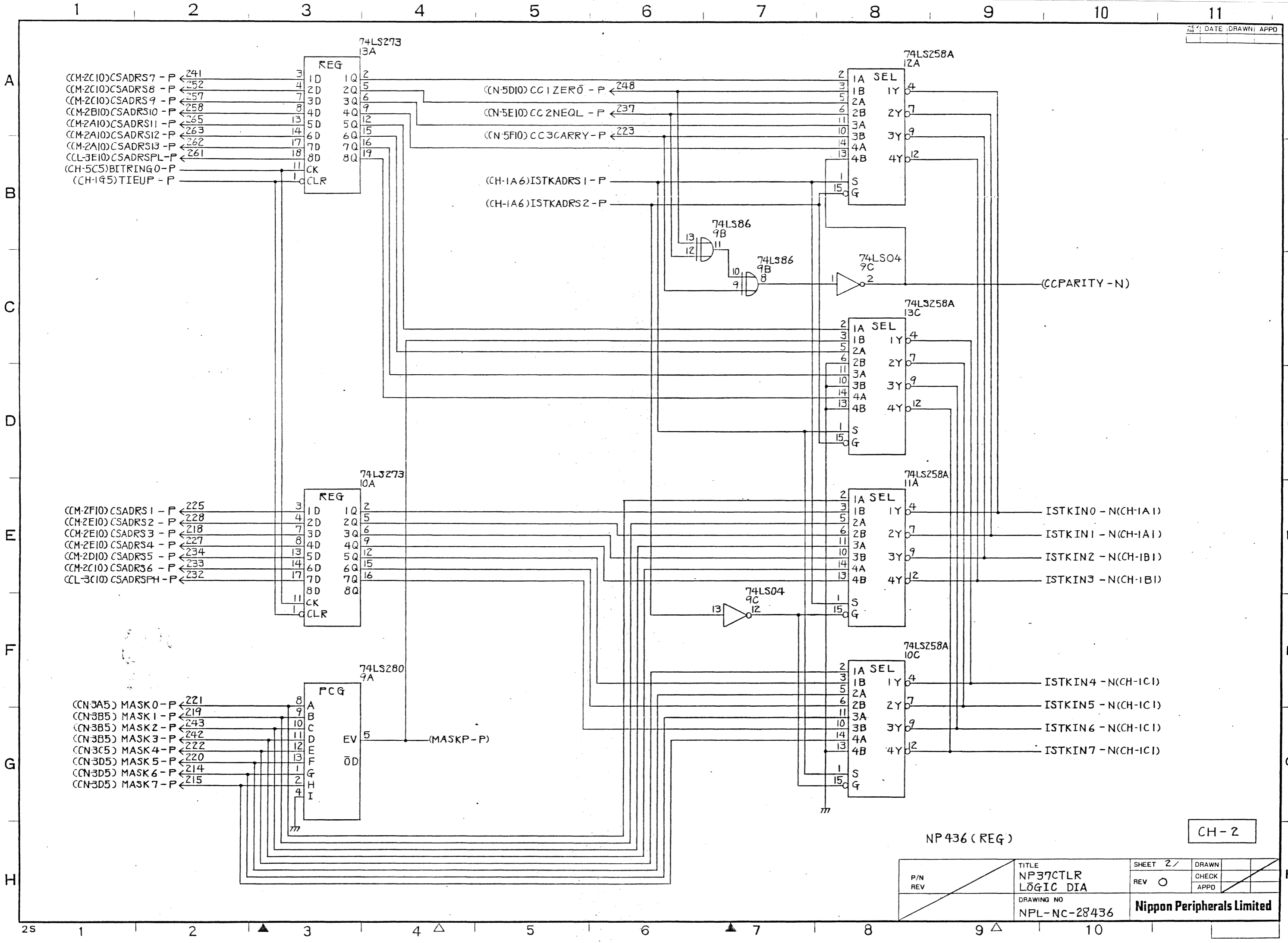
P/N	REV	TITLE NP37CTLR LOGIC DIA	SHEET 4/4	DRAWN	
			REV 0	CHECK	
DRAWING NO NPL-NC-28435			Nippon Peripherals Limited		



NP436 (REG)

CH-1

P/N NP436	TITLE NP37CTLR LOGIC DIA	SHEET 1/5	DRAWN A.06/1.0 82.1.28
REV B		REV 0	CHECK APPD K.H. 82.1.29
REG	DRAWING NO NPL-NC-28436	Nippon Peripherals Limited	

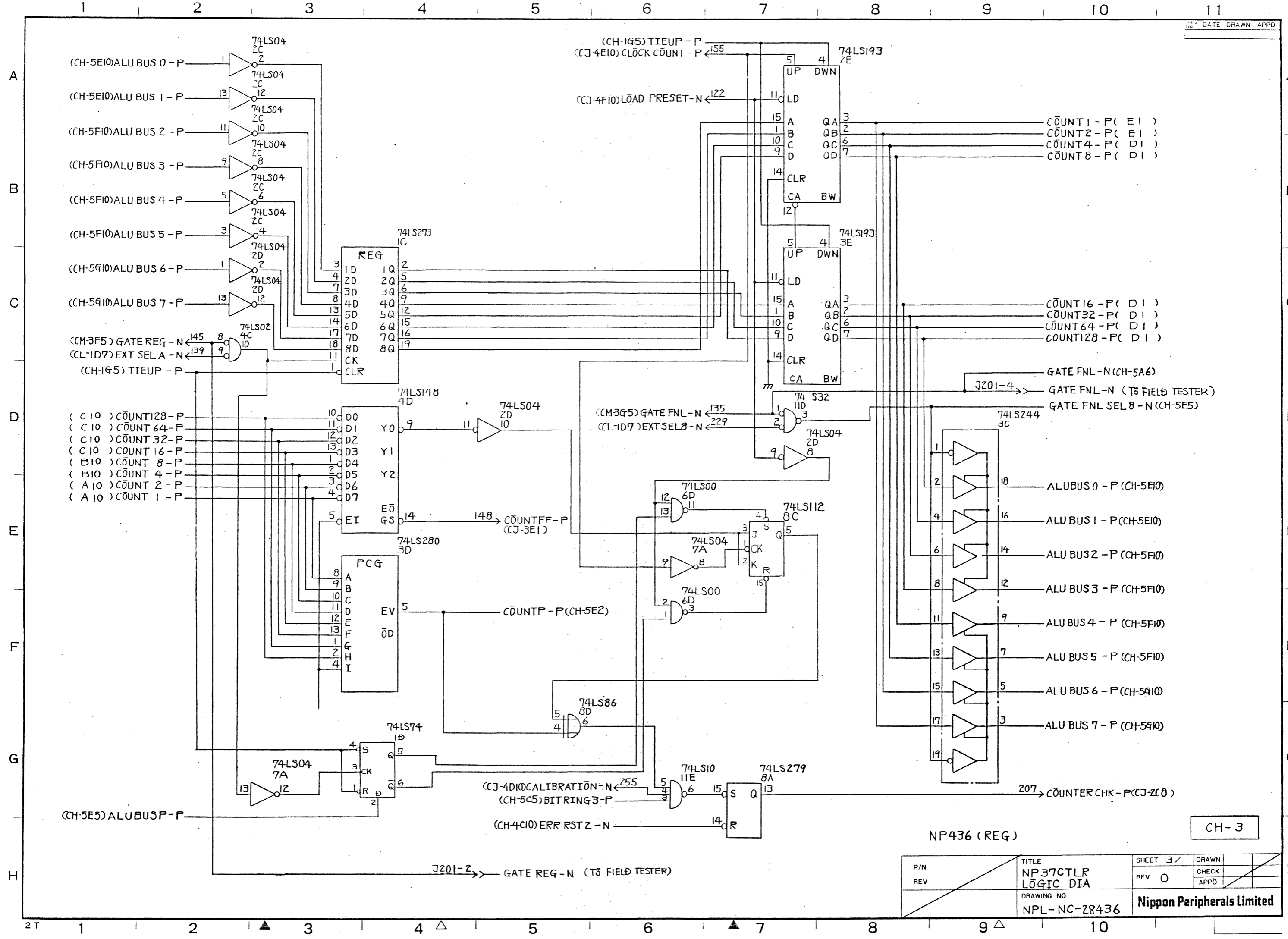


NP436 (REG)

CH-2

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 2/	DRAWN
	DRAWING NO NPL-NC-28436	REV 0	CHECK APPD
		Nippon Peripherals Limited	

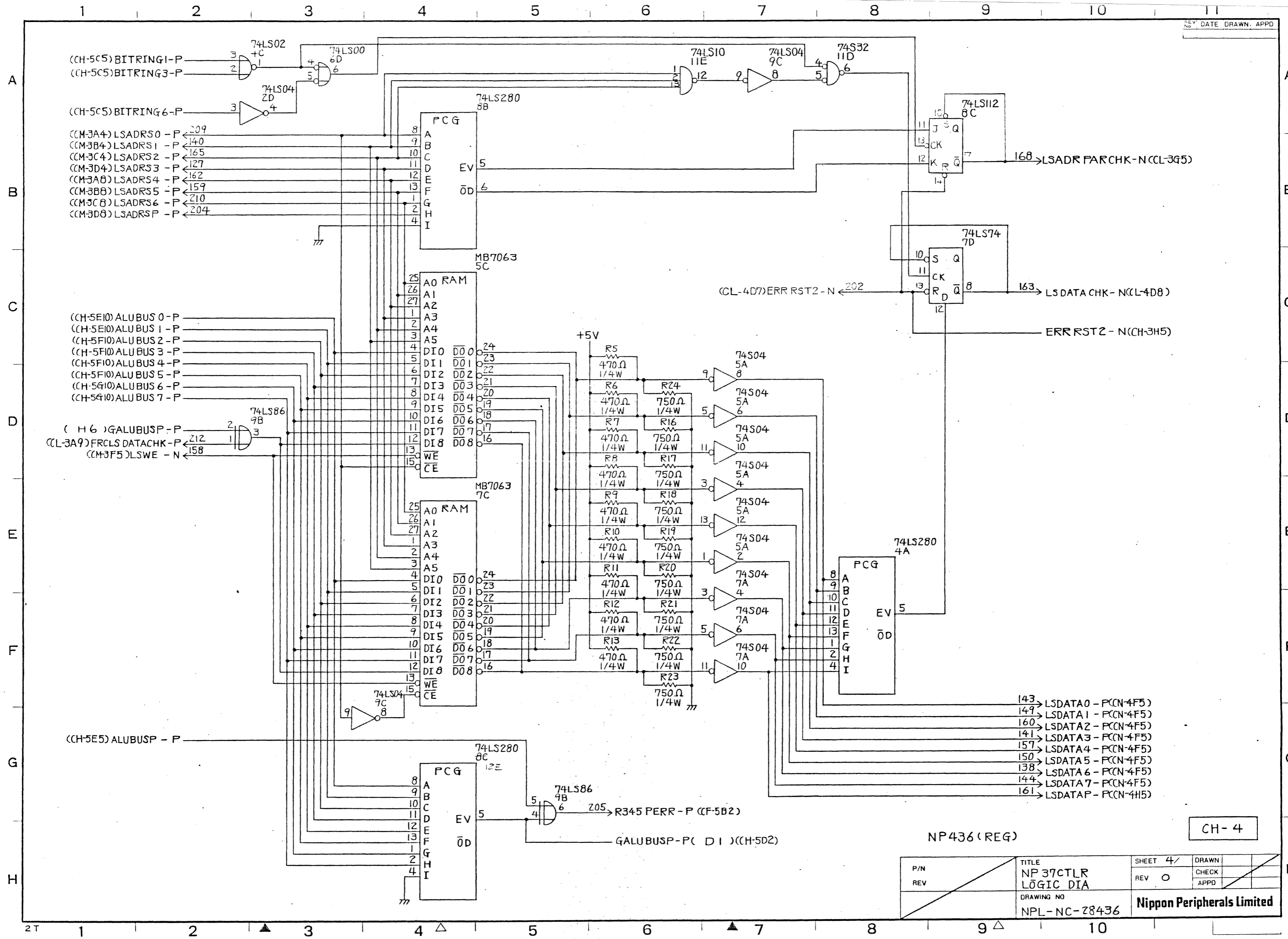
58



59

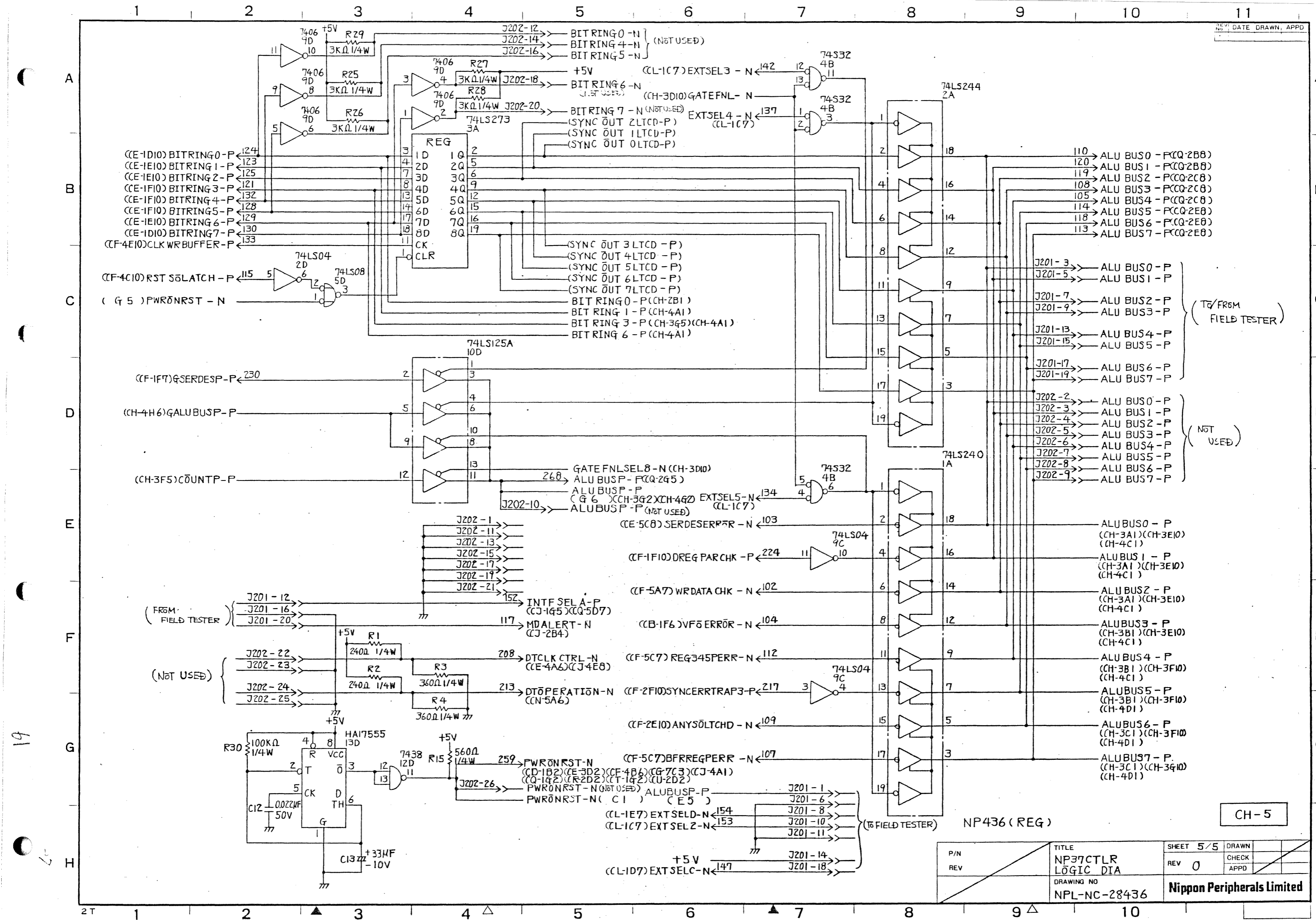
CH-3

P/N	REV	TITLE	SHEET 3 /	DRAWN
		NP37CTLR LOGIC DIA	REV 0	CHECK
		DRAWING NO	APPD	
		NPL-NC-28436	Nippon Peripherals Limited	



NP436 (REG)		CH-4	
P/N	TITLE	SHEET 4/	DRAWN
REV	NP 37CTLR LOGIC DIA	REV 0	CHECK
	DRAWING NO		APPD
	NPL-NC-28436	Nippon Peripherals Limited	

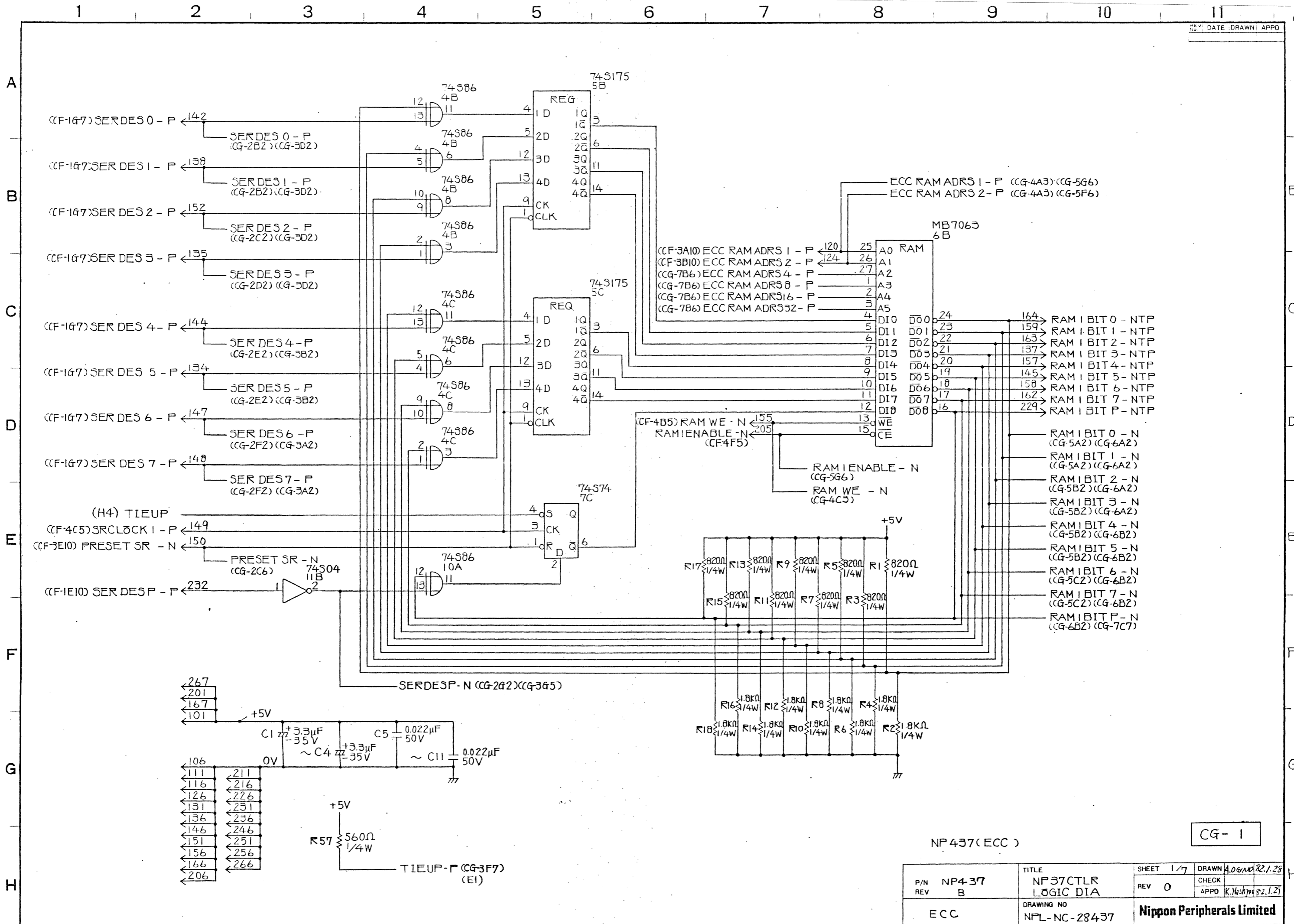
09
95



CH-5

P/N REV	TITLE	SHEET 5/5	DRAWN
	NP37CTLR LOGIC DIA	REV 0	CHECK
DRAWING NO NPL-NC-28436		APPD	
		Nippon Peripherals Limited	

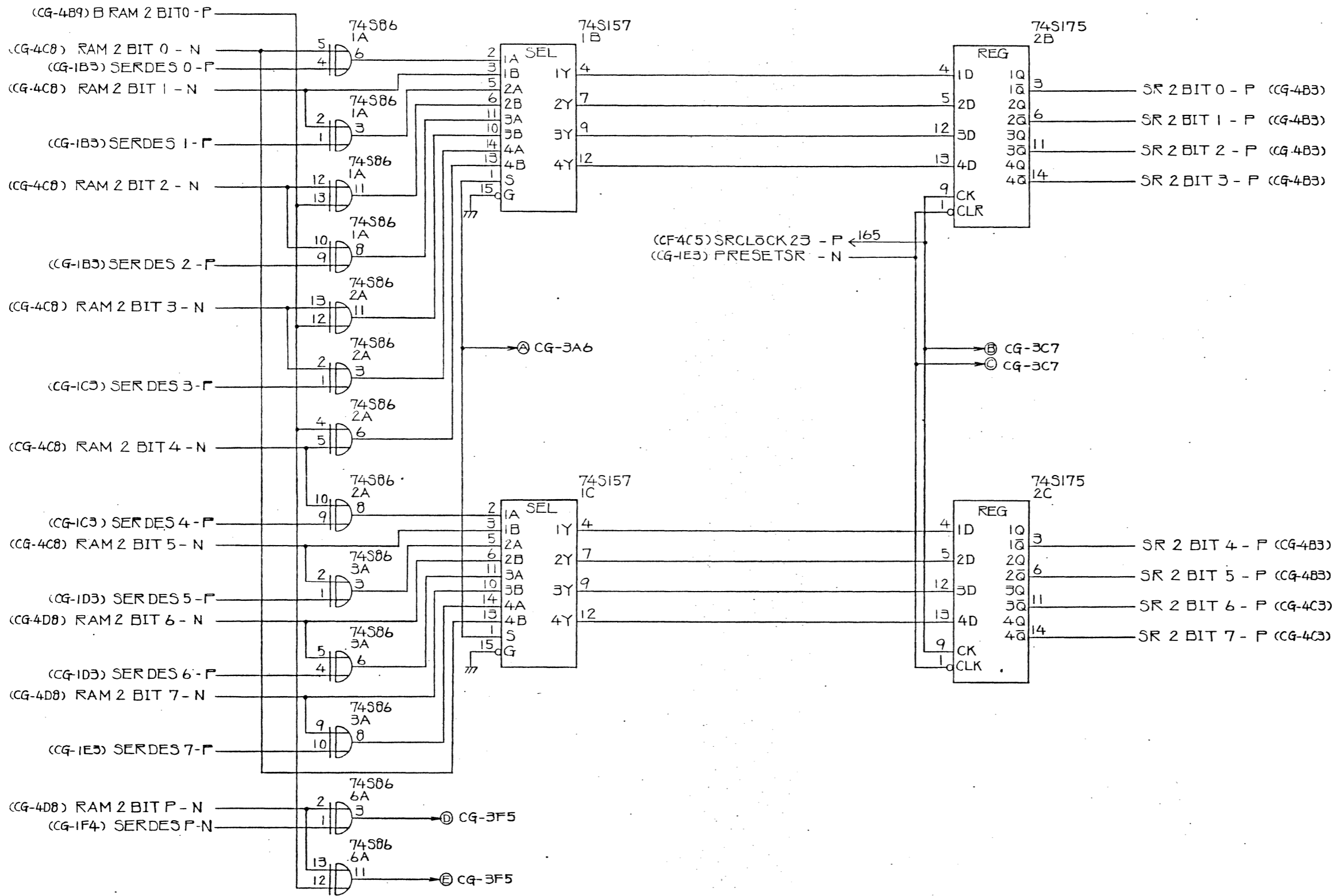
19



CG-1

P/N NP437		TITLE NP37CTLR		SHEET 1/7		DRAWN A. Ogino 22.1.28	
REV B		LOGIC DIA		REV 0		CHECK	
ECC		DRAWING NO NPL-NC-28437		APPD K. Hashim 22.1.27		Nippon Peripherals Limited	

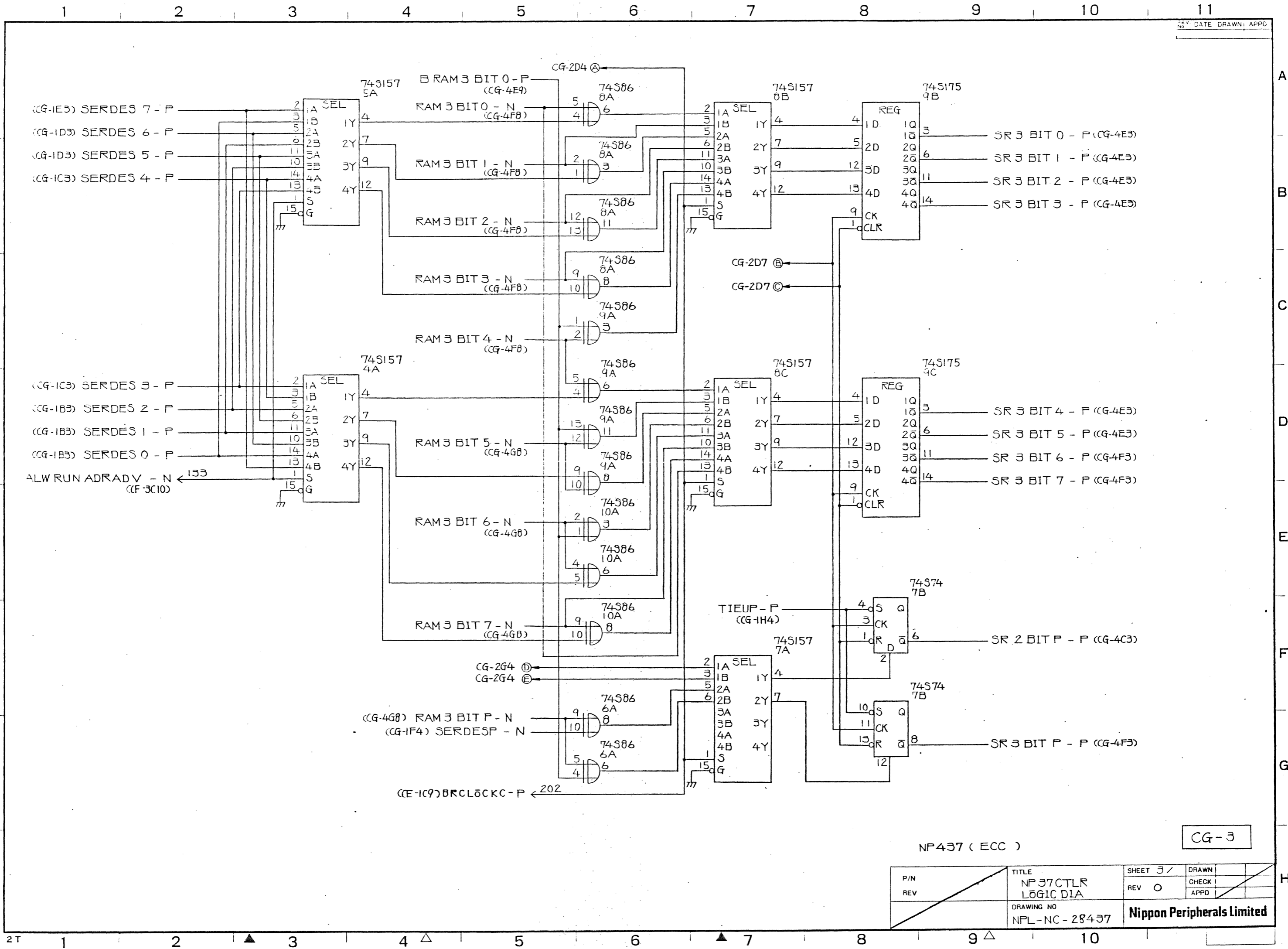
62



NP437 (ECC)

CG-2

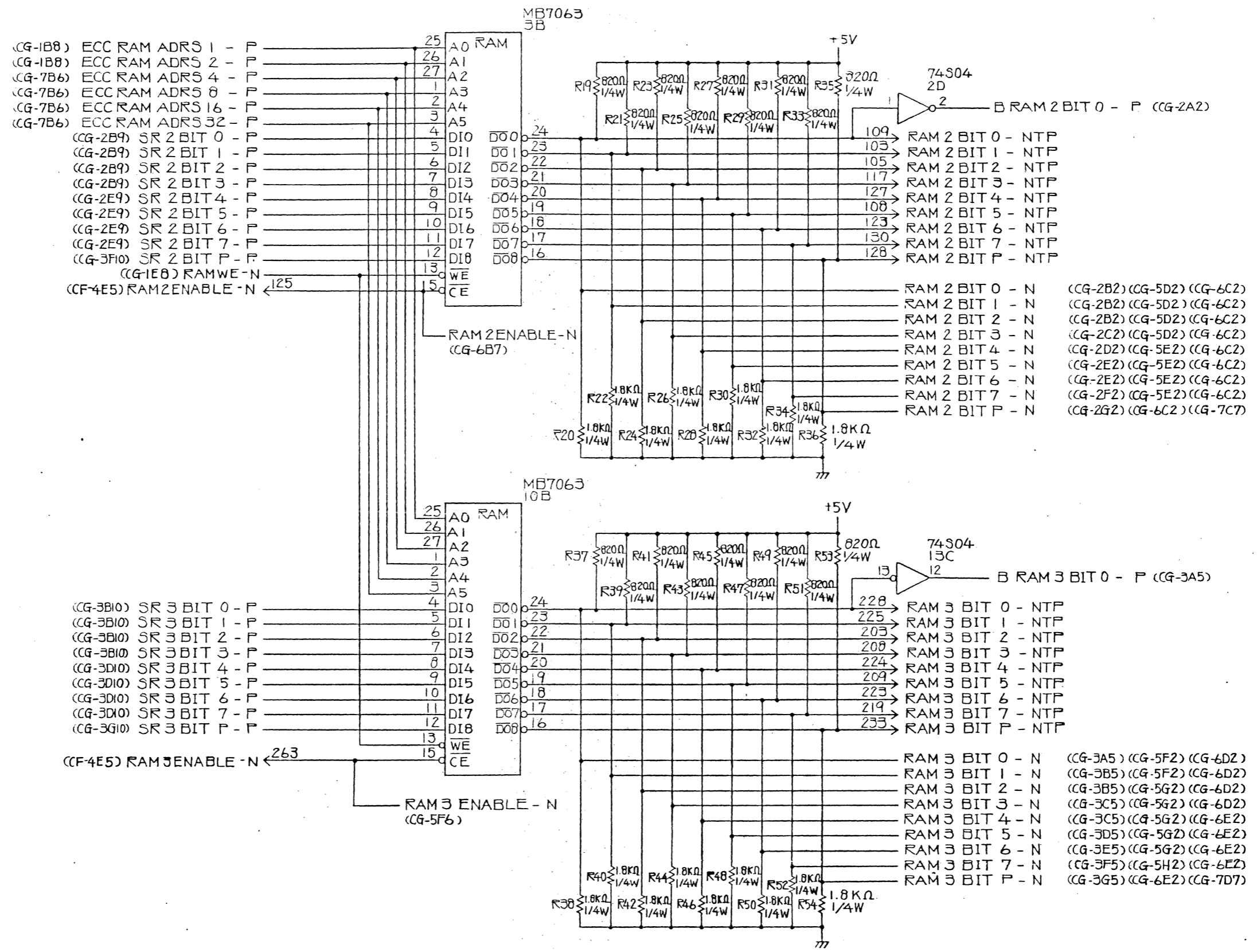
P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 2/ REV 0	DRAWN CHECK APPD
	DRAWING NO NPL-NC-28437	Nippon Peripherals Limited	



NP437 (ECC)

CG-3

P/N REV	TITLE	SHEET 3 /	DRAWN
	NP37CTLR LOGIC DIA	REV 0	CHECK
DRAWING NO NPL-NC-28437		Nippon Peripherals Limited	

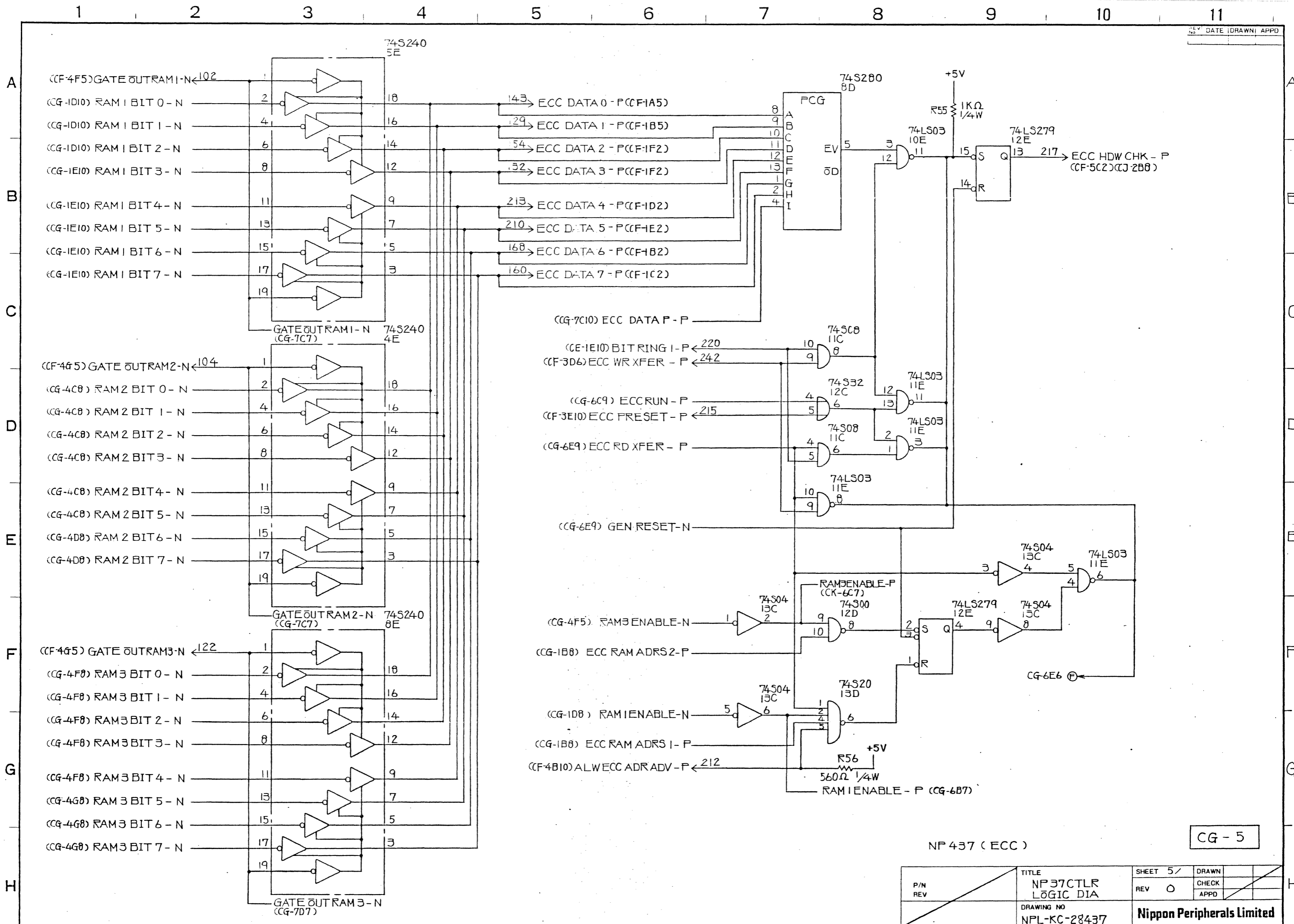


NF437 (ECC)

CG-4

P/N REV	TITLE NF37CTLR LOGIC DIA	SHEET 4/	DRAWN
	DRAWING NO NFL-NC-28437	REV 0	CHECK APPD
		Nippon Peripherals Limited	

65



NP 437 (ECC)

CG-5

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 5/	DRAWN	
		REV 0	CHECK	
DRAWING NO NPL-KC-28437		Nippon Peripherals Limited		

99

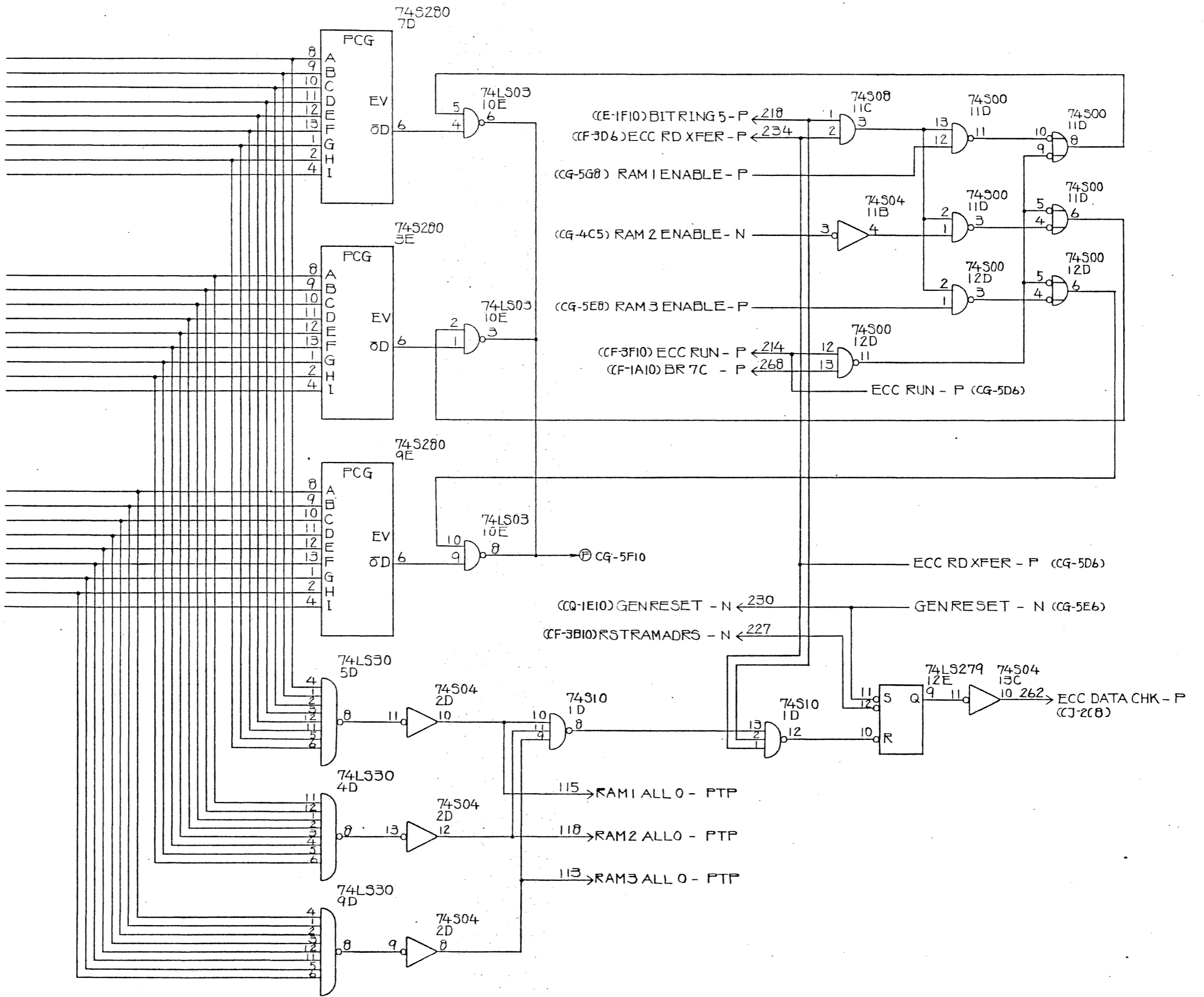
1 2 3 4 5 6 7 8 9 10 11

A
B
C
D
E
F
G
H

(CG-1D10) RAM 1 BIT 0 - N
 (CG-1D10) RAM 1 BIT 1 - N
 (CG-1D10) RAM 1 BIT 2 - N
 (CG-1E10) RAM 1 BIT 3 - N
 (CG-1E10) RAM 1 BIT 4 - N
 (CG-1E10) RAM 1 BIT 5 - N
 (CG-1E10) RAM 1 BIT 6 - N
 (CG-1E10) RAM 1 BIT 7 - N
 (CG-1F10) RAM 1 BIT P - N

(CG-4C8) RAM 2 BIT 0 - N
 (CG-4C8) RAM 2 BIT 1 - N
 (CG-4C8) RAM 2 BIT 2 - N
 (CG-4C8) RAM 2 BIT 3 - N
 (CG-4C8) RAM 2 BIT 4 - N
 (CG-4C8) RAM 2 BIT 5 - N
 (CG-4D8) RAM 2 BIT 6 - N
 (CG-4D8) RAM 2 BIT 7 - N
 (CG-4D8) RAM 2 BIT P - N

(CG-4F8) RAM 3 BIT 0 - N
 (CG-4F8) RAM 3 BIT 1 - N
 (CG-4F8) RAM 3 BIT 2 - N
 (CG-4F8) RAM 3 BIT 3 - N
 (CG-4F8) RAM 3 BIT 4 - N
 (CG-4G8) RAM 3 BIT 5 - N
 (CG-4G8) RAM 3 BIT 6 - N
 (CG-4G8) RAM 3 BIT 7 - N
 (CG-4G8) RAM 3 BIT P - N

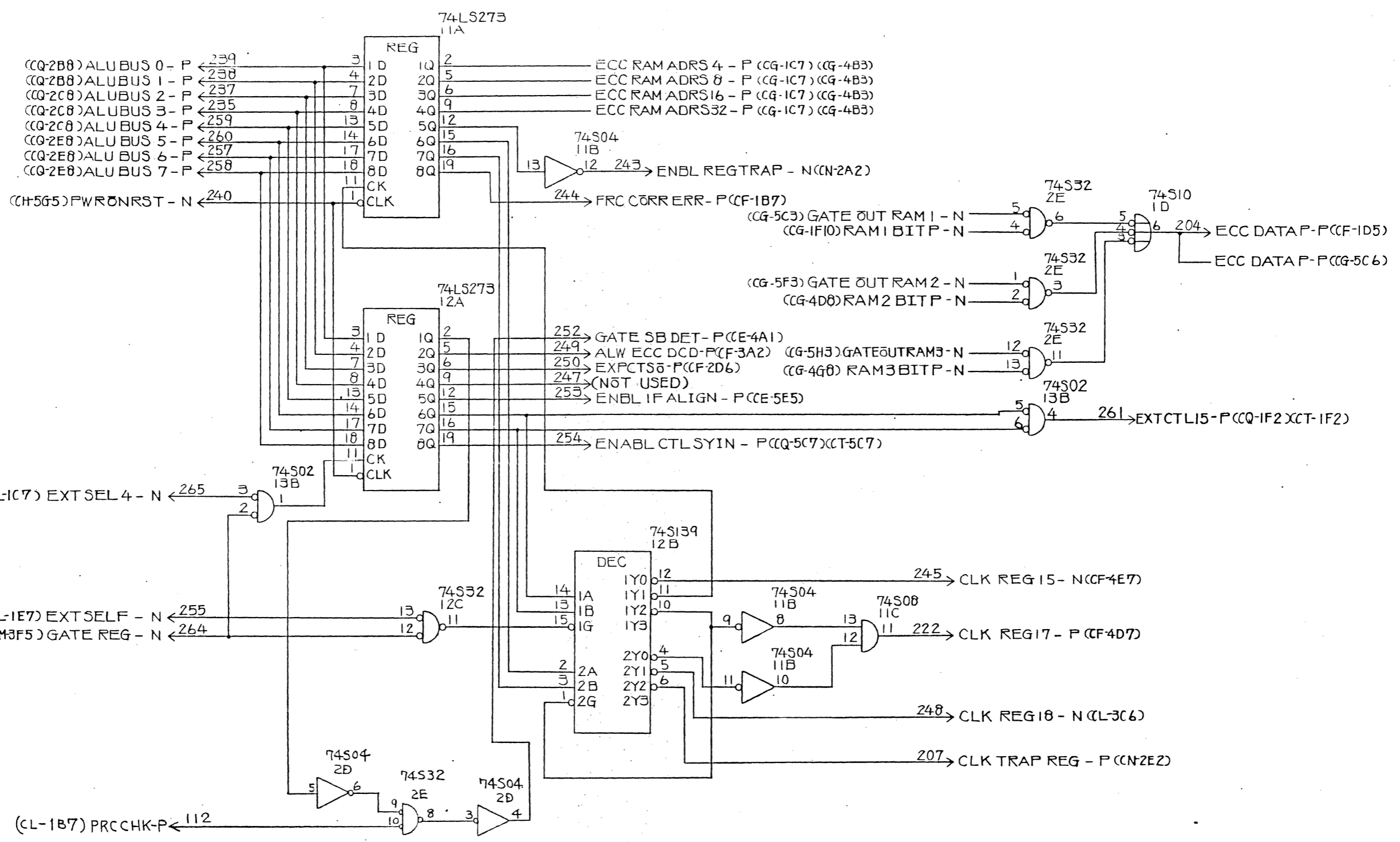


NP437 (ECC)

CG-6

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 6/ REV 0	DRAWN CHECK APPD
	DRAWING NO NPL-NC-28437	Nippon Peripherals Limited	

25 1 2 3 4 5 6 7 8 9 10

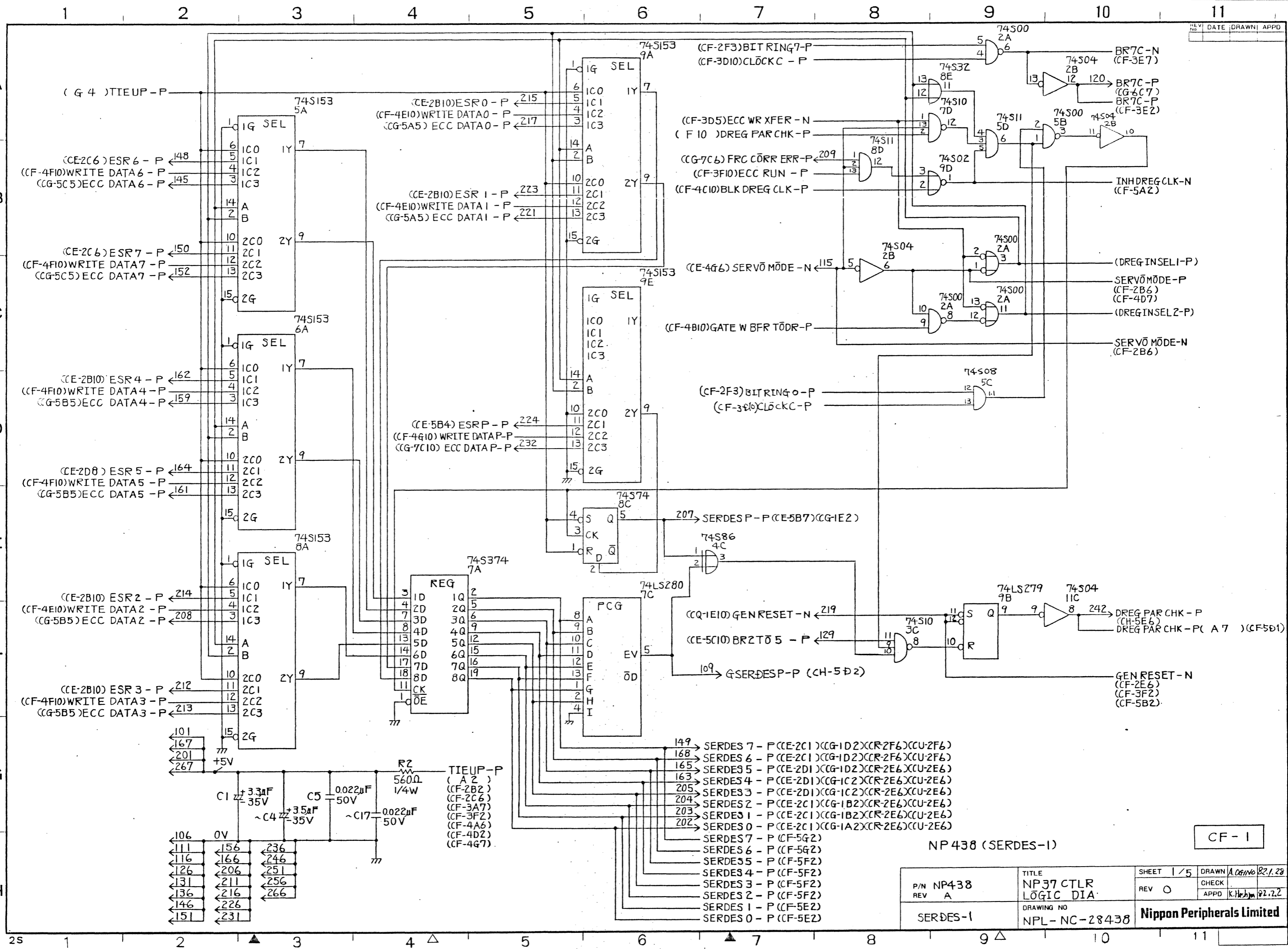


NP437 (ECC)

CG-7

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 7/7	DRAWN
	DRAWING NO NPL-NC-28437	REV 0	CHECK APPD
		Nippon Peripherals Limited	

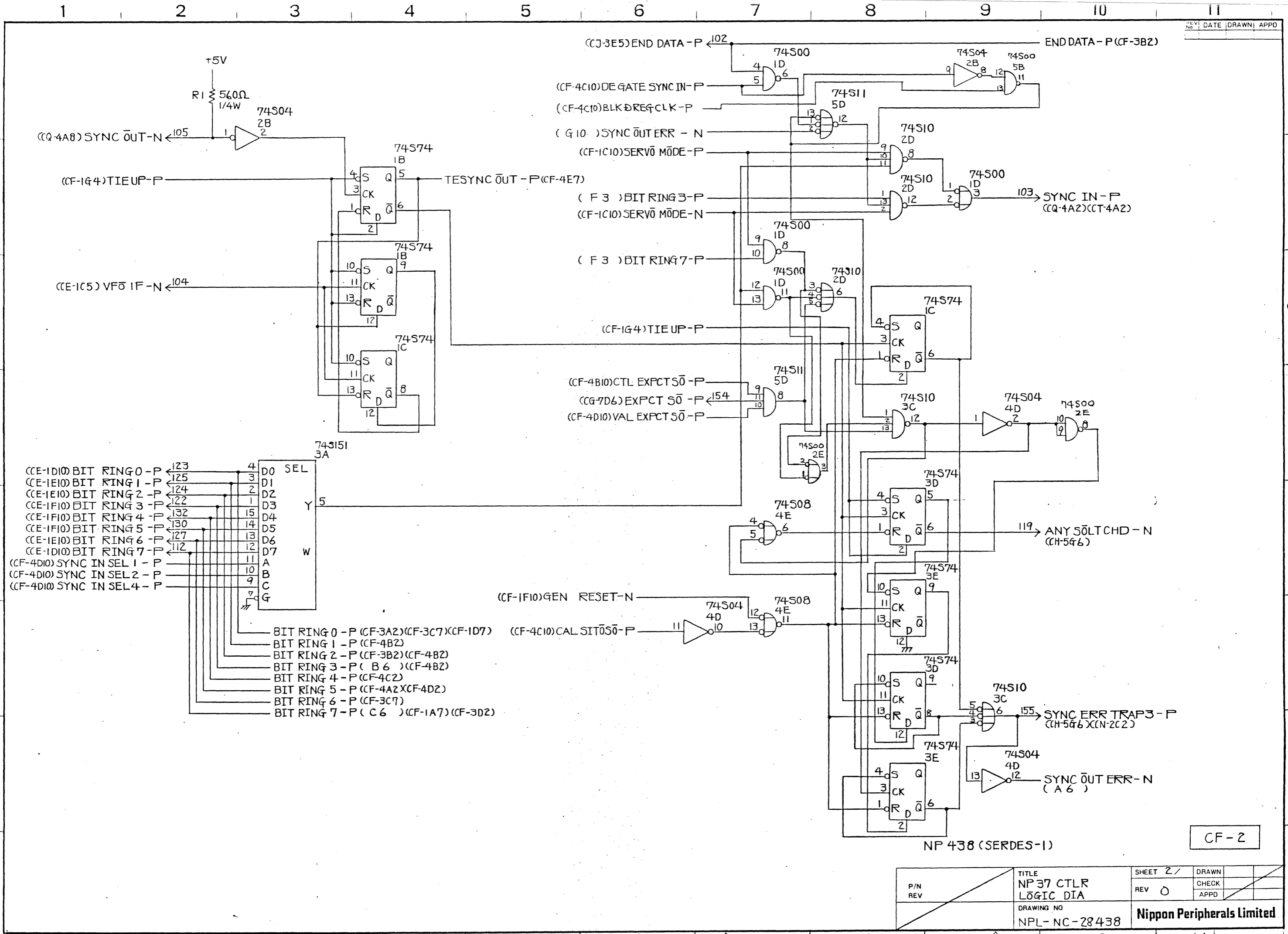
89



NP438 (SERDES-1)

CF-1

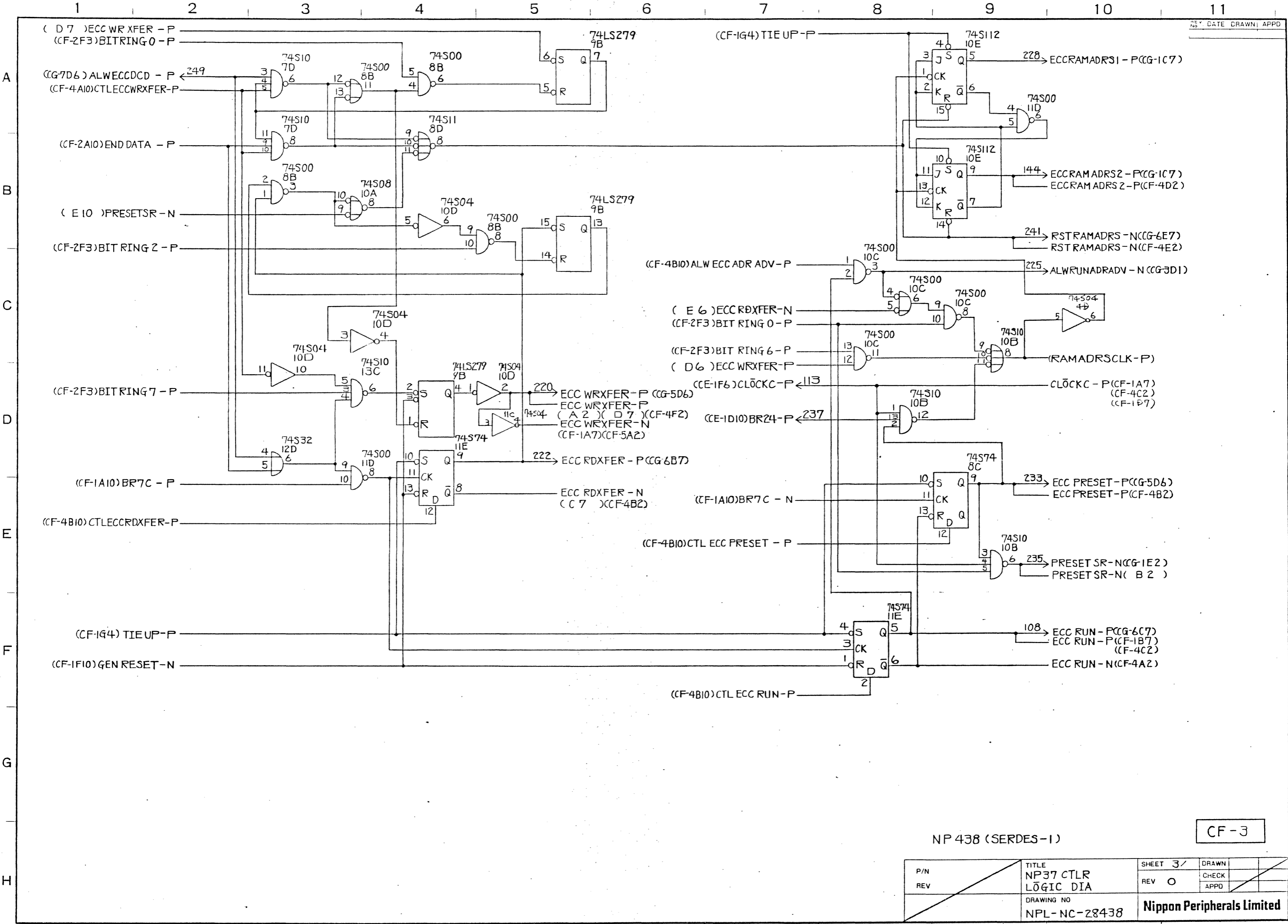
P/N NP438	TITLE NP37 CTRLR LOGIC DIA	SHEET 1/5	DRAWN A. G. No. 22.1.28
REV A		CHECK	APPD K. H. No. 22.2.2
SERDES-1	DRAWING NO NPL-NC-28438	Nippon Peripherals Limited	



CF-2

NP 438 (SERDES-1)

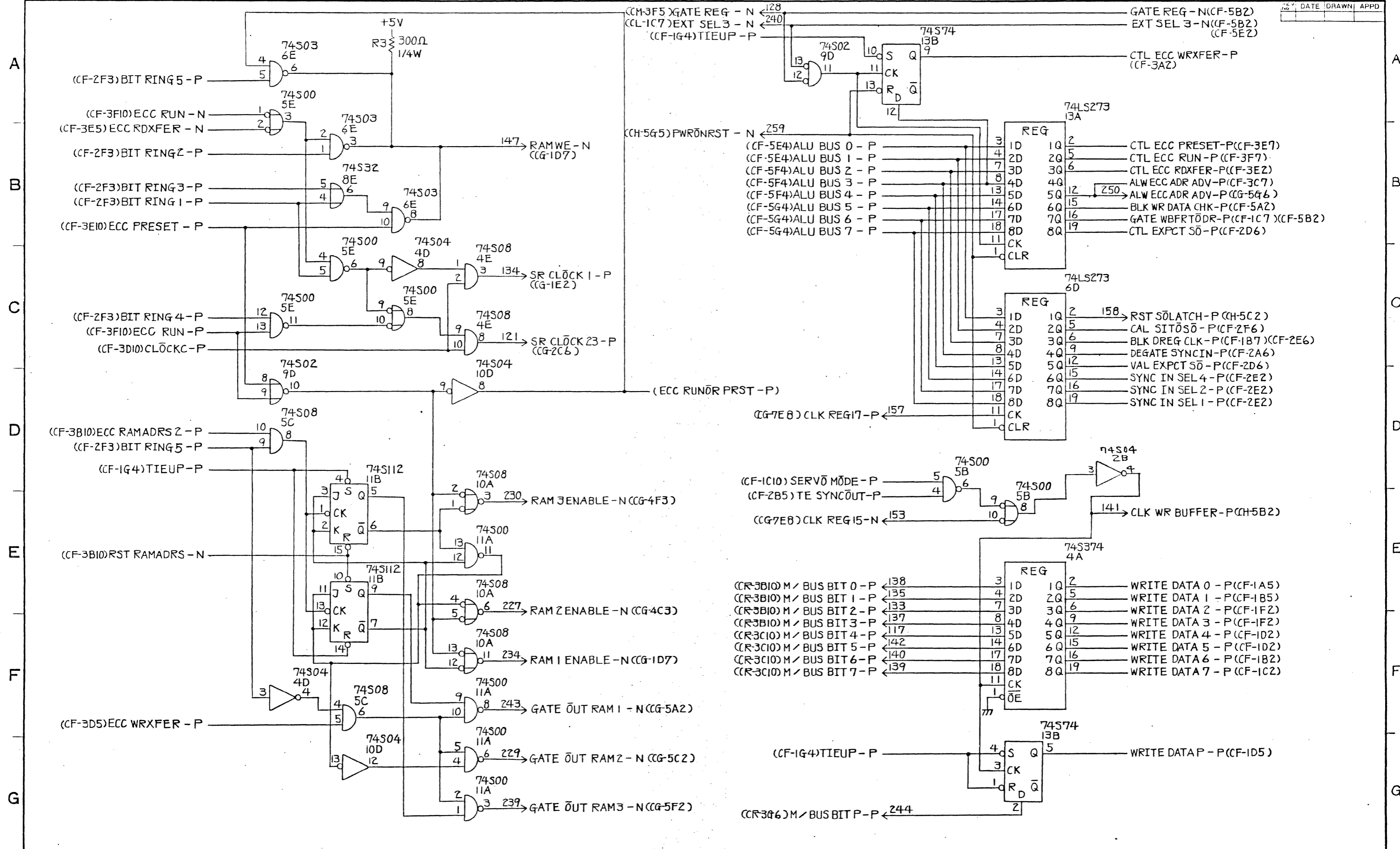
P/N REV	TITLE NP 37 CTLR LOGIC DIA	SHEET 2 /	DRAWN
	DRAWING NO NPL-NC-28438	REV 0	CHECK
Nippon Peripherals Limited		APPD	



NP 438 (SERDES-1)

CF-3

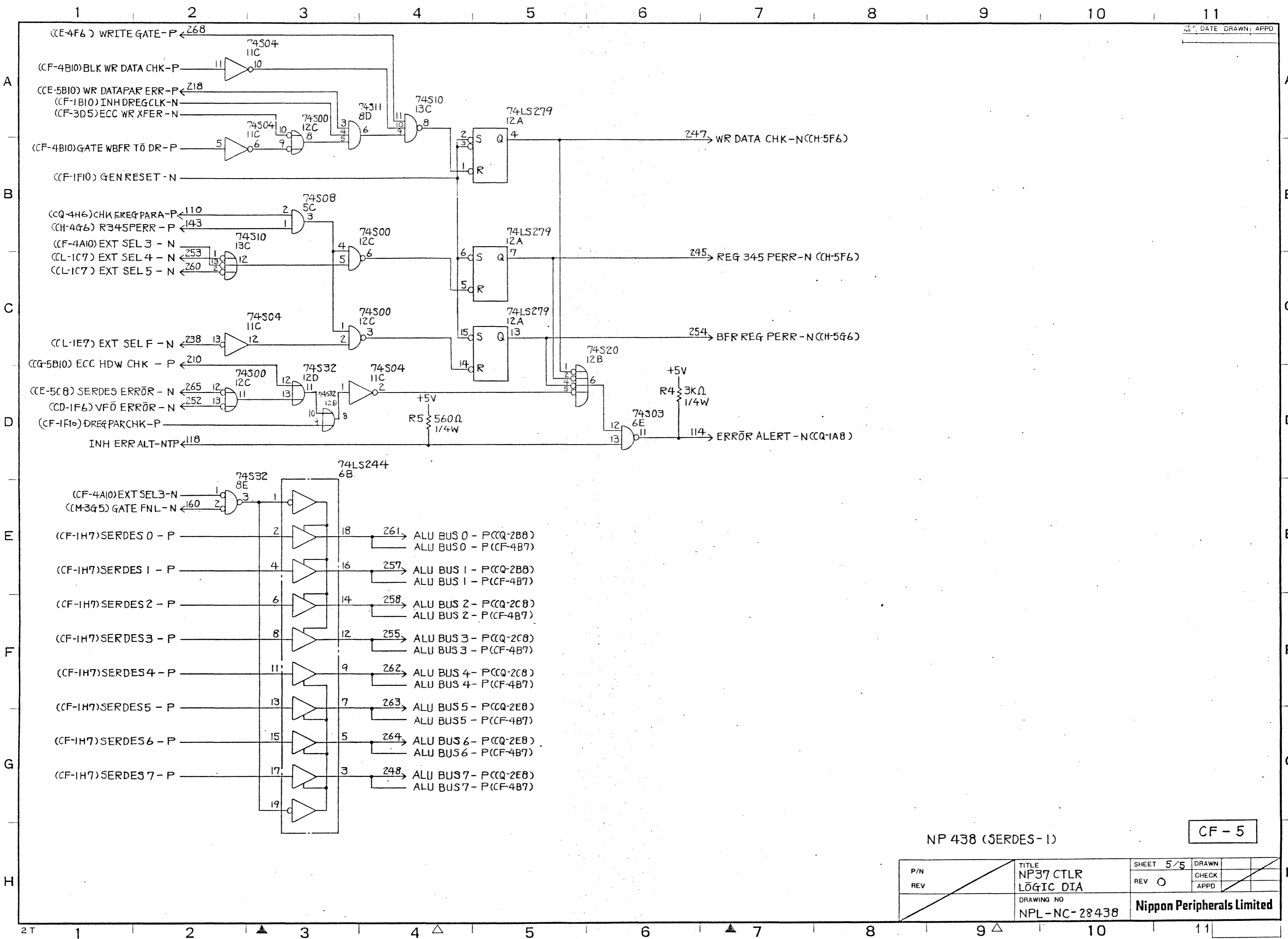
P/N REV	TITLE NP37 CTLR LOGIC DIA	SHEET 3/	DRAWN
		REV 0	CHECK
DRAWING NO NPL-NC-28438		APPD	
		Nippon Peripherals Limited	



NP 438 (SERDES-1)

CF-4

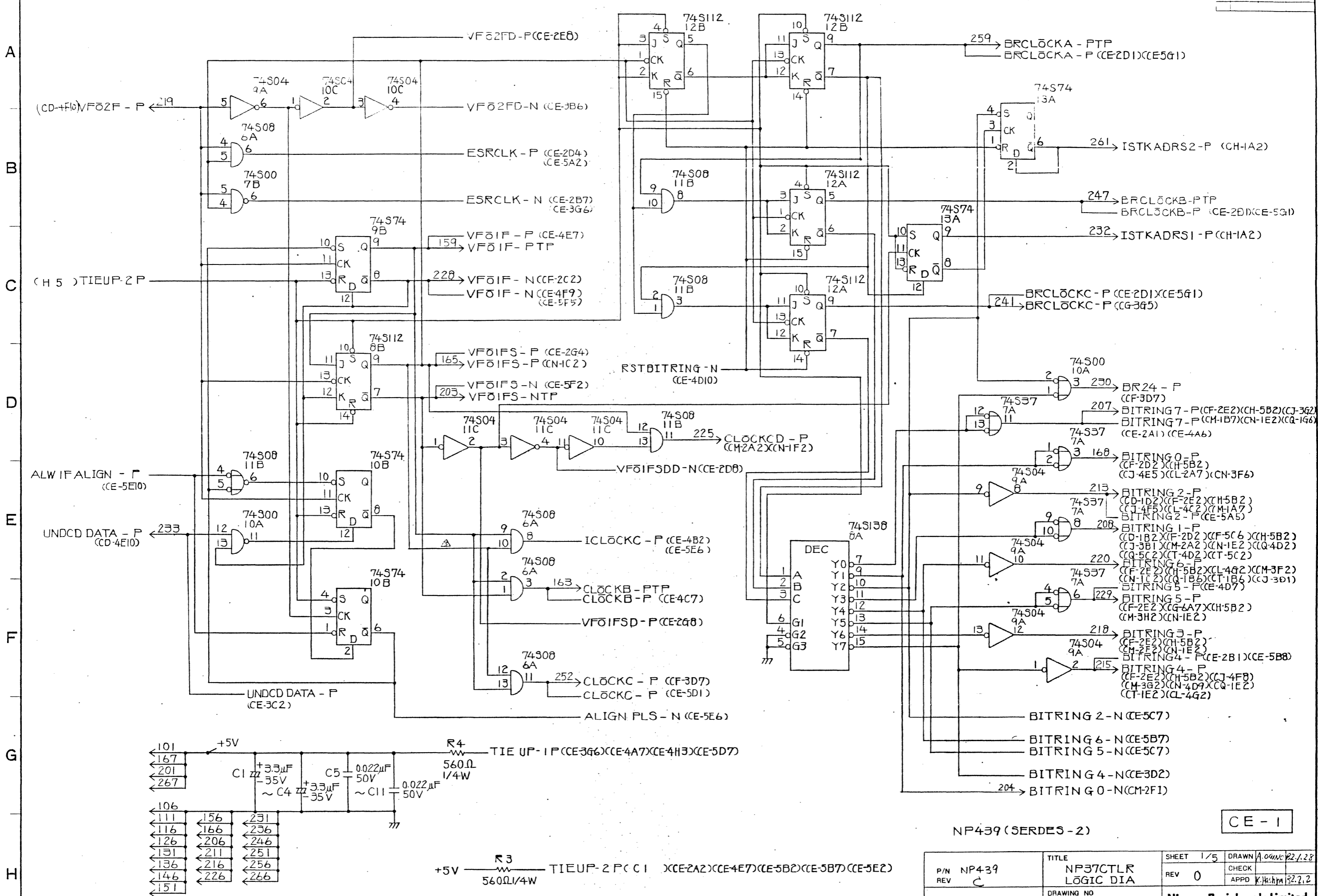
P/N REV	TITLE NP 37 CTR LOGIC DIA	SHEET 4/	DRAWN	
		REV 0	CHECK	
DRAWING NO NPL-NC-28438		Nippon Peripherals Limited		



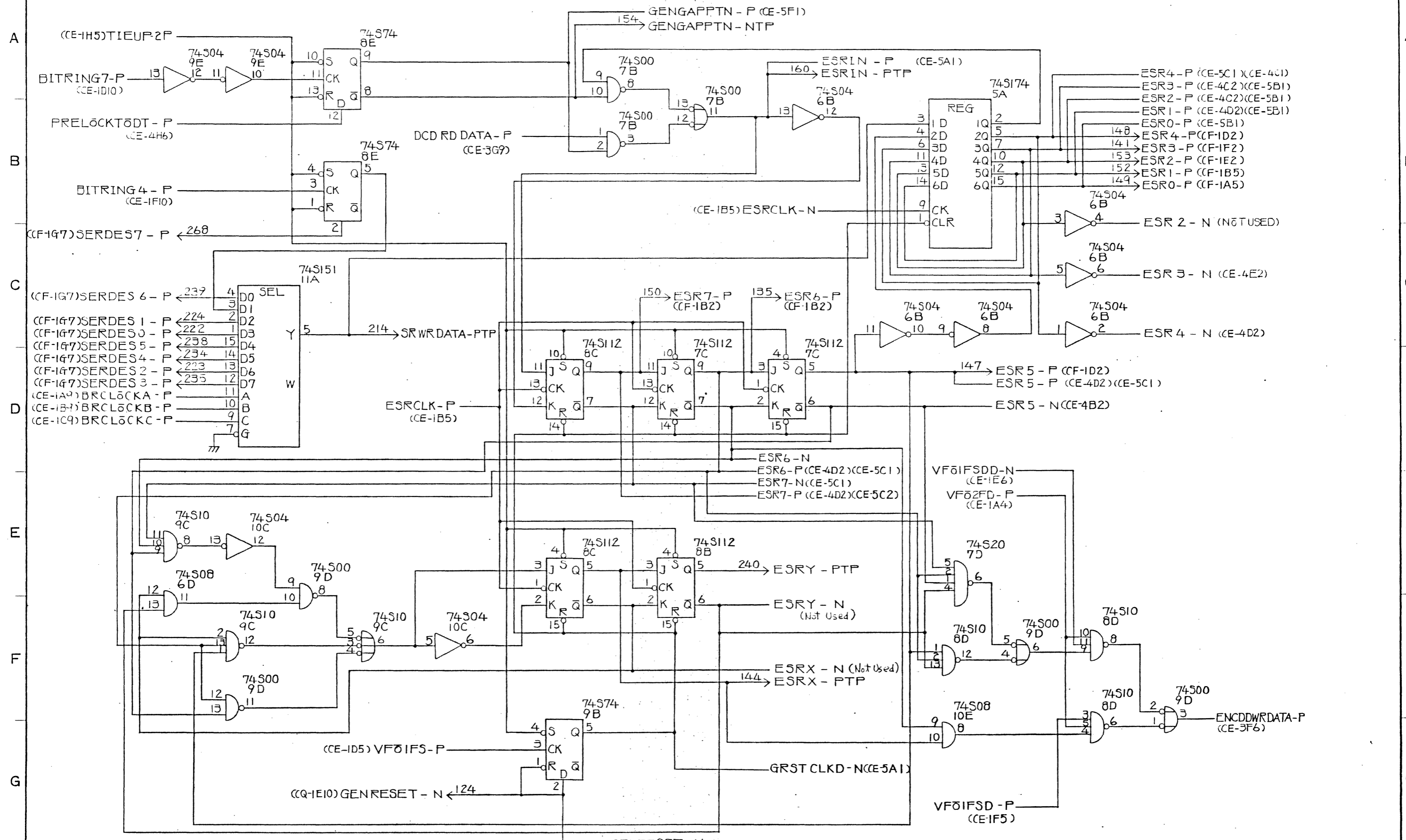
NP 438 (SERDES-1)

CF-5

P/N REV	TITLE NP37 CTLR LOGIC DIA	SHEET 5/5	DRAWN	
		REV 0	CHECK	
DRAWING NO NPL-NC-28438		Nippon Peripherals Limited		



NP439 (SERDES-2)		CE-1	
P/N NP439	TITLE NP37CTLR LOGIC DIA	SHEET 1/5	DRAWN A.ogmc 22.1.28
REV C		REV 0	CHECK
SERDES-2	DRAWING NO NPL-NC-28439	APPD K.Hshpa 32.2.2	
Nippon Peripherals Limited			



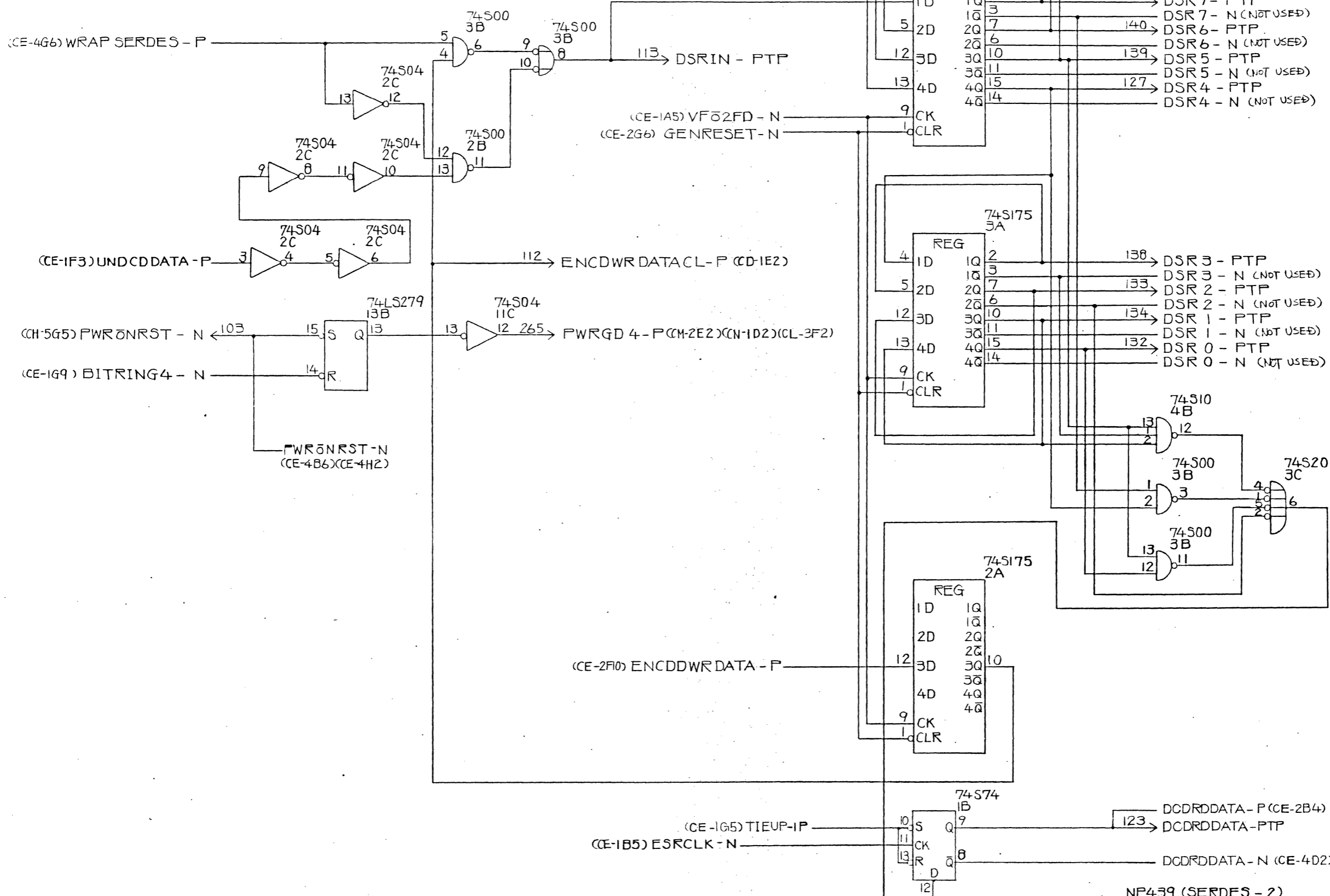
NP439 (SERDES-2)

CE - 2

P/N	REV	TITLE NP37CTLR LOGIC DIA	SHEET 2 /	DRAWN	
			REV 0	CHECK	
		DRAWING NO NPL-NC-28439	Nippon Peripherals Limited		

75

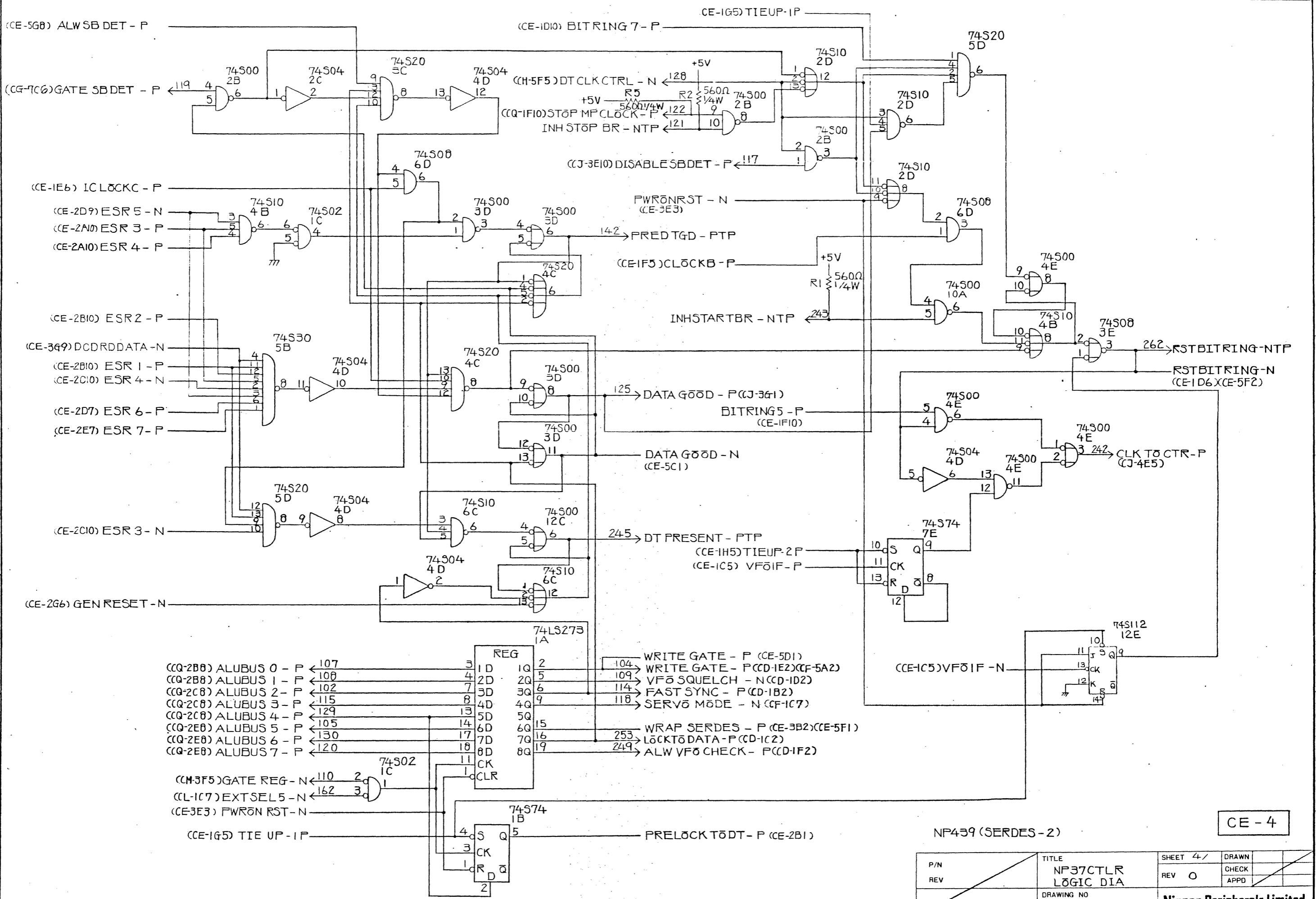
H



CE - 3

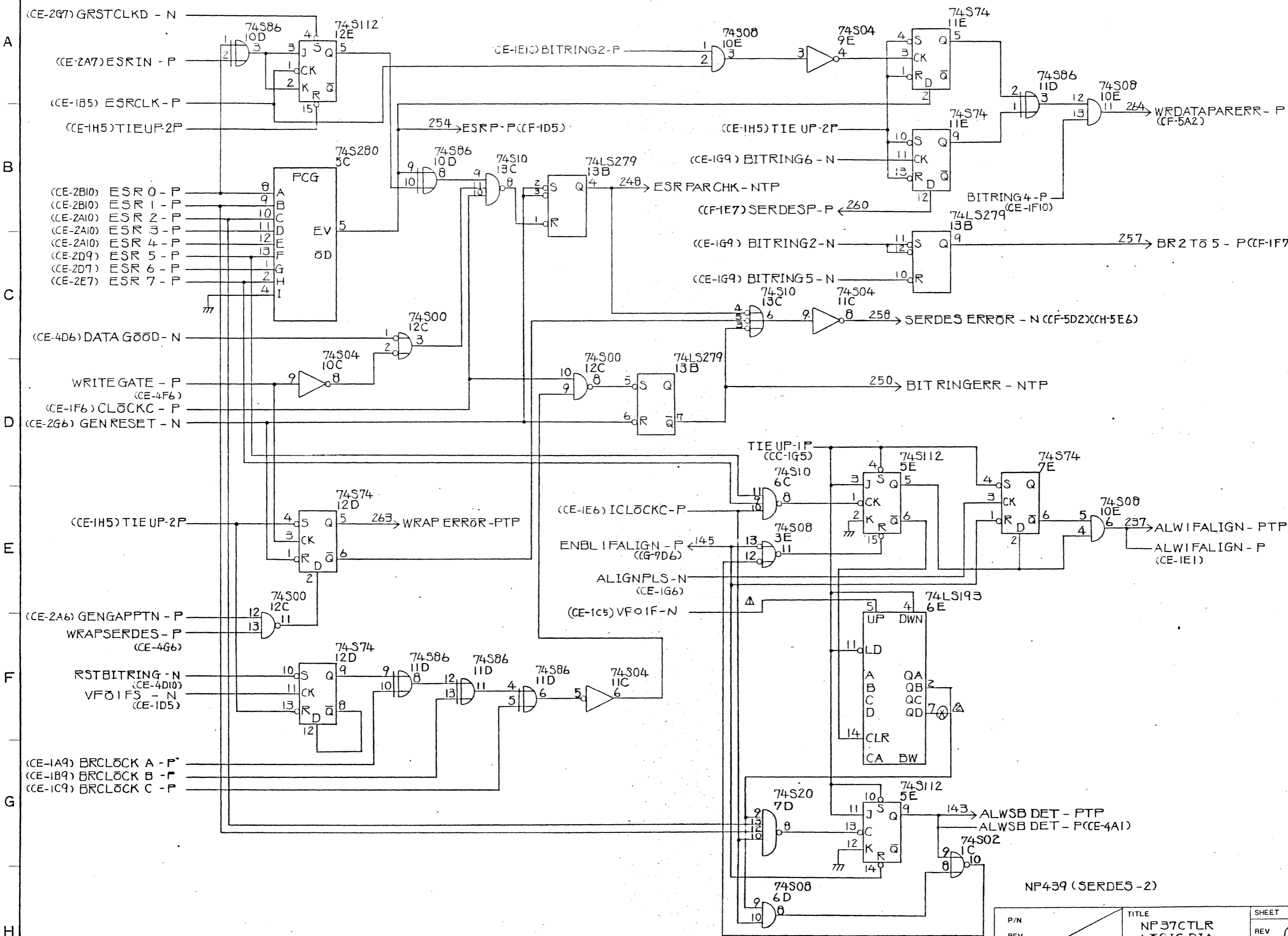
P/N	REV	TITLE	SHEET 3/	DRAWN
		NP37CTLR LOGIC DIA	REV 0	CHECK
		DRAWING NO	APPD	
		NPL - NC - 28439	Nippon Peripherals Limited	

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CE - 4

P/N		TITLE NP37CTLR LÖGIC DIA	SHEET 4/	DRAWN
REV			REV 0	CHECK
DRAWING NO NFL-NC-28439		Nippon Peripherals Limited		



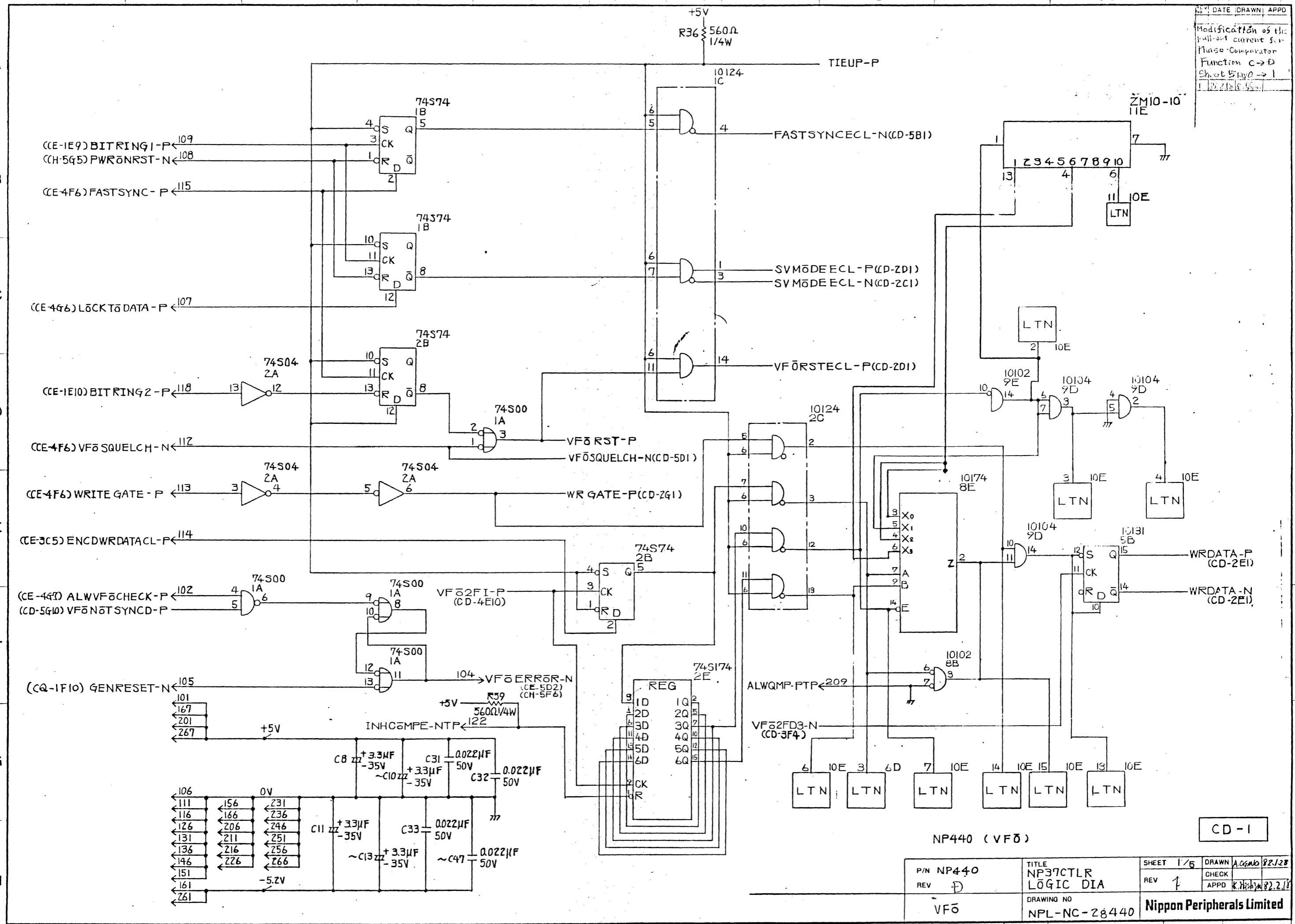
NP439 (SERDES-2)

CE - 5

P/N	REV	TITLE	SHEET	DRAWN
		NP37CTLR LOGIC DIA	5/5	
		DRAWING NO	REV	CHECK
		NPL-NC-28439	0	APPD
Nippon Peripherals Limited				

78

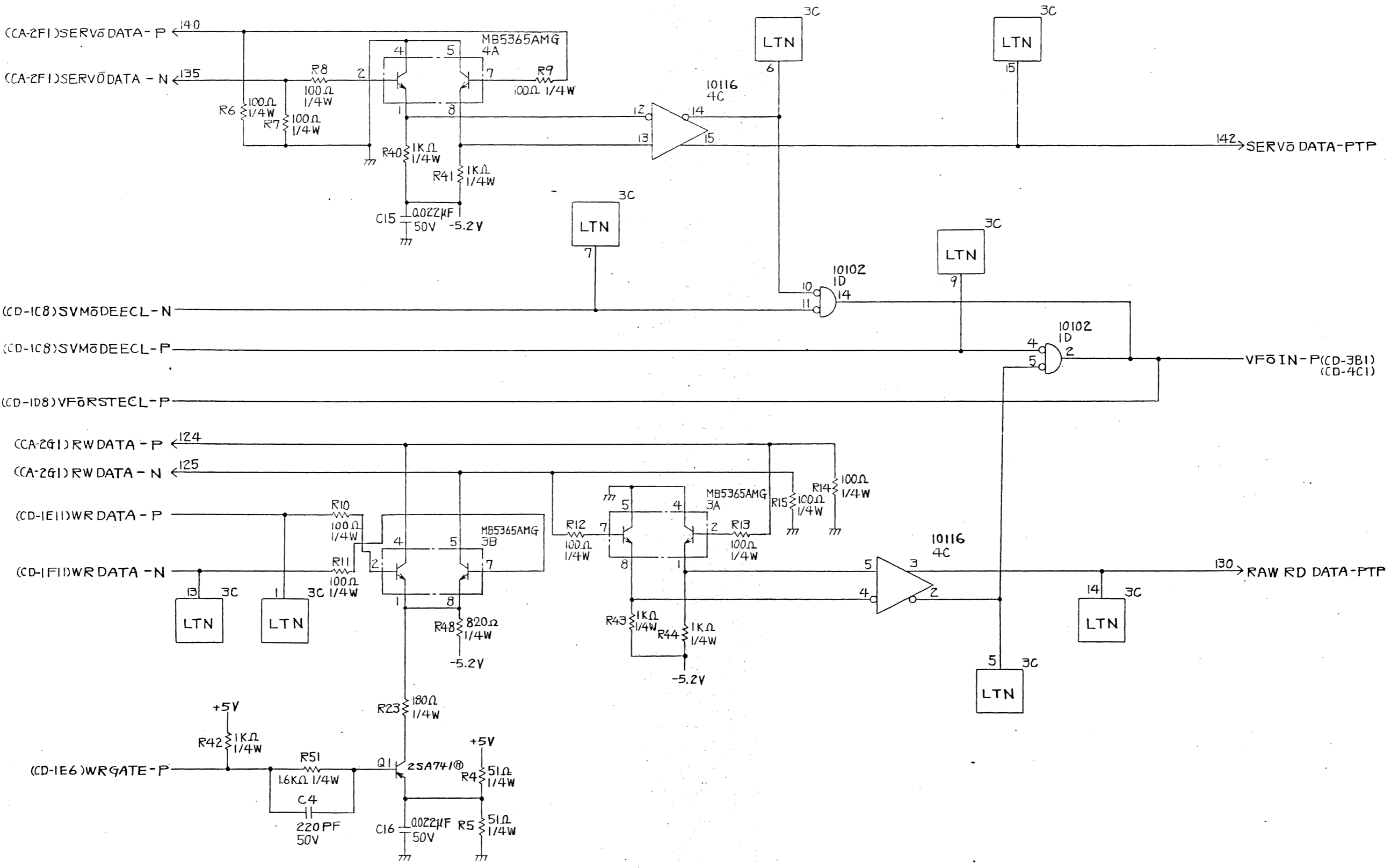
DATE [DRAWN] APPD
 Modification of the
 full-on current for
 Phase-Comparator
 Function C→D
 Sheet 5/300 → 1
 1/22/82



P/N NP440	TITLE NP37CTLR LOGIC DIA	SHEET 1/5	DRAWN A. Ogino 82/28
REV D	DRAWING NO NPL-NC-28440	CHECK	APPD K. Nishimura 82/28
VF0		Nippon Peripherals Limited	

64

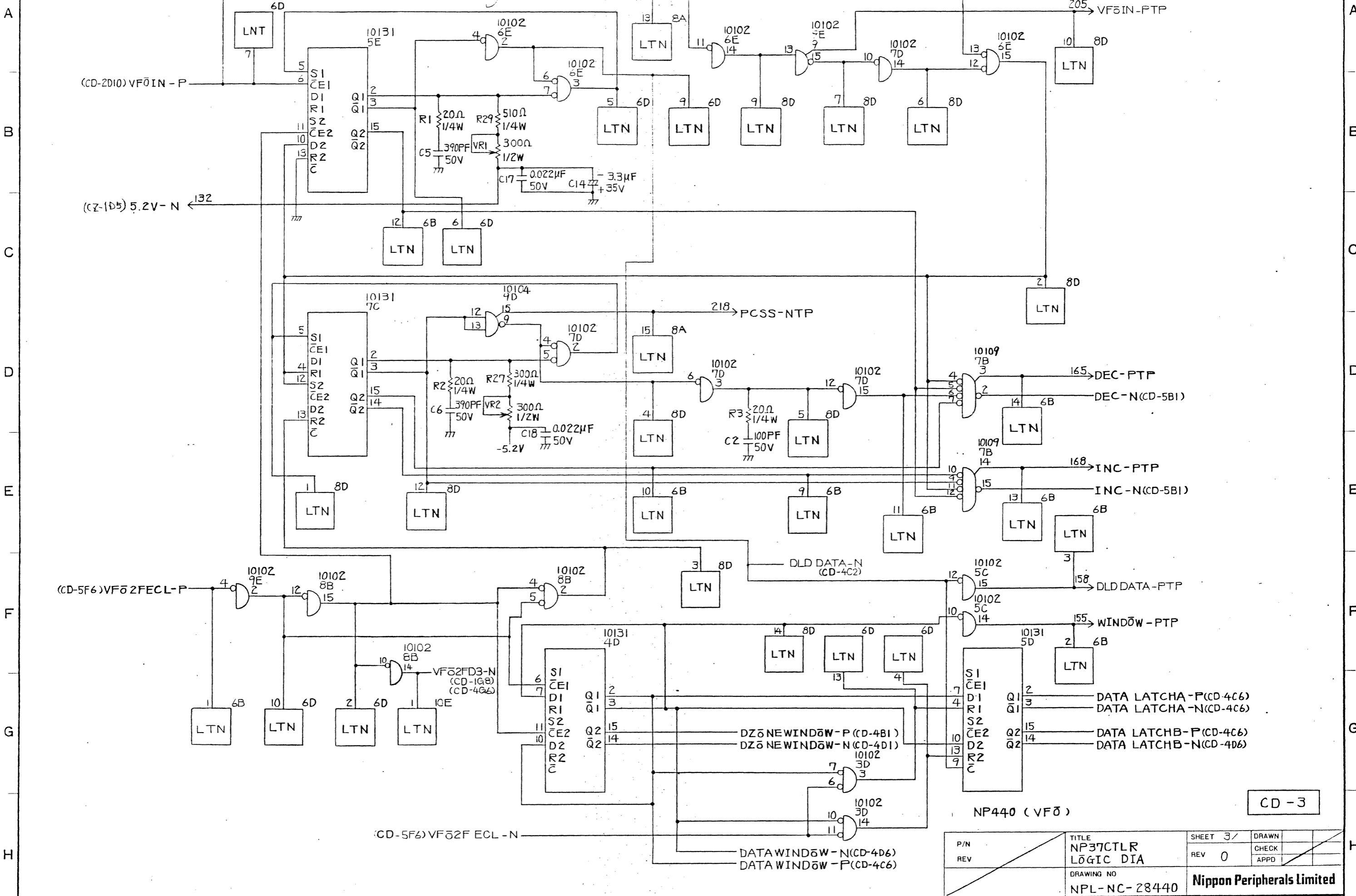
A
B
C
D
E
F
G
H



NP440 (VF0)

CD-2

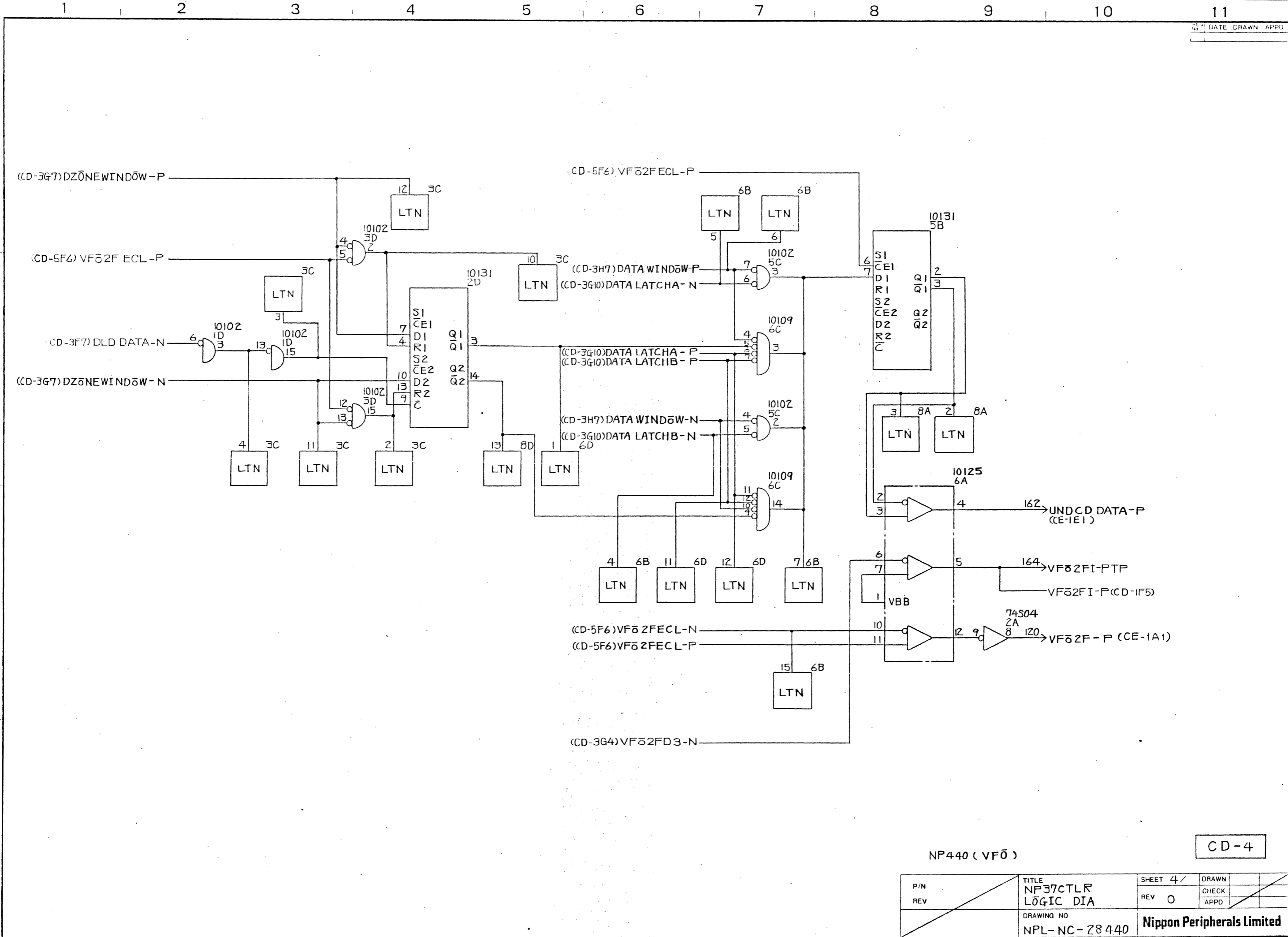
P/N	TITLE	SHEET 2/	DRAWN
REV	NP37CTLR LOGIC DIA	REV 0	CHECK
	DRAWING NO		APPD
	NPL-NC-28440	Nippon Peripherals Limited	



CD-3

P/N	REV	TITLE	SHEET	DRAWN
		NP37CLR LOGIC DIA	3/	
		DRAWING NO	REV	CHECK
		NPL-NC-28440	0	APPD
			Nippon Peripherals Limited	

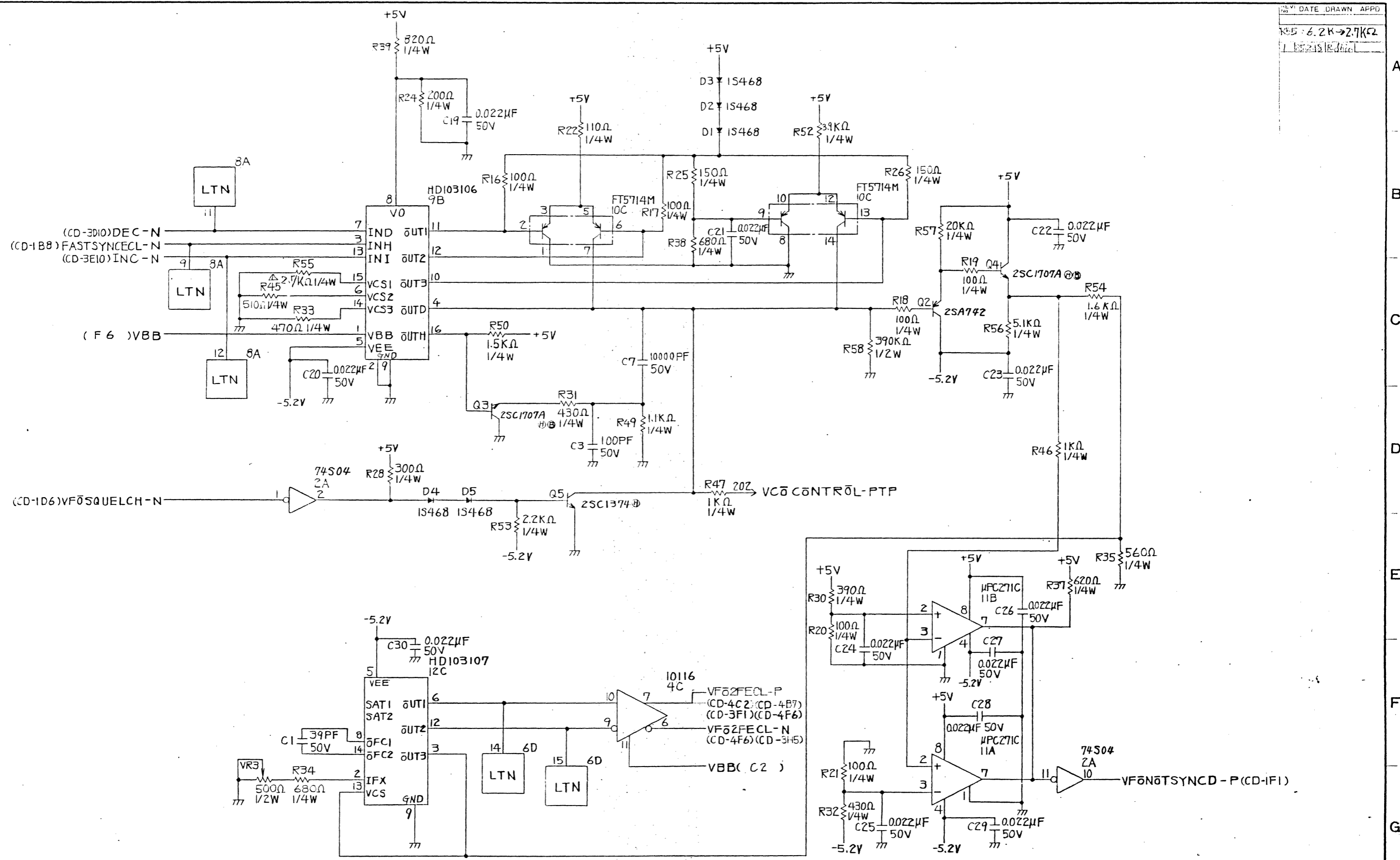
18



NP440 (VF0)

CD-4

P/N	TITLE NP37CTLR LOGIC DIA	SHEET 4/	DRAWN
REV		REV 0	CHECK APPD
DRAWING NO NPL-NC-28440		Nippon Peripherals Limited	

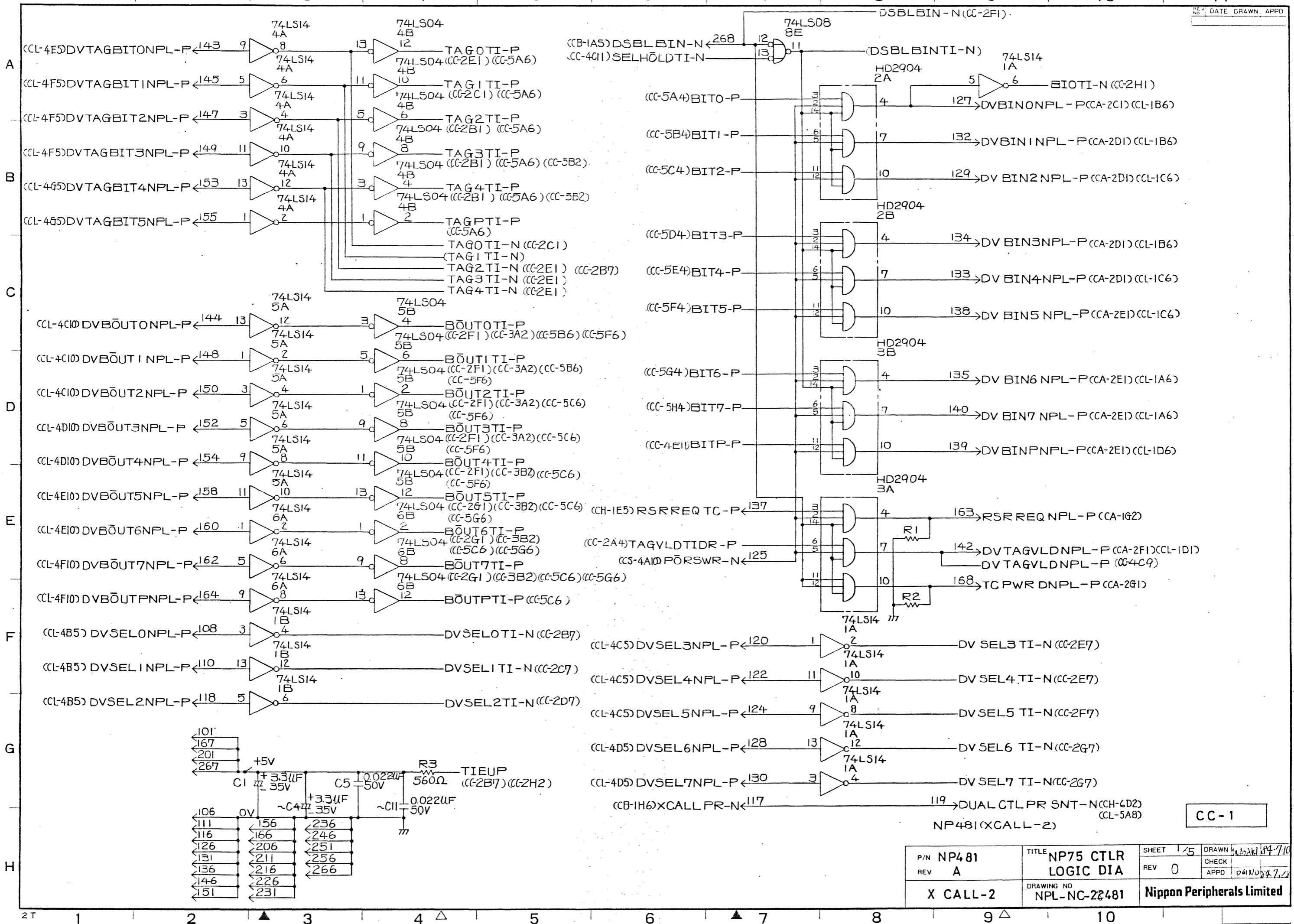


NP440 (VF0)

CD-5

P/N REV	TITLE NP37CTLR LOGIC DIA	SHEET 5/5	DRAWN
	DRAWING NO NPL-NC-28440	REV 1	CHECK APPD
		Nippon Peripherals Limited	

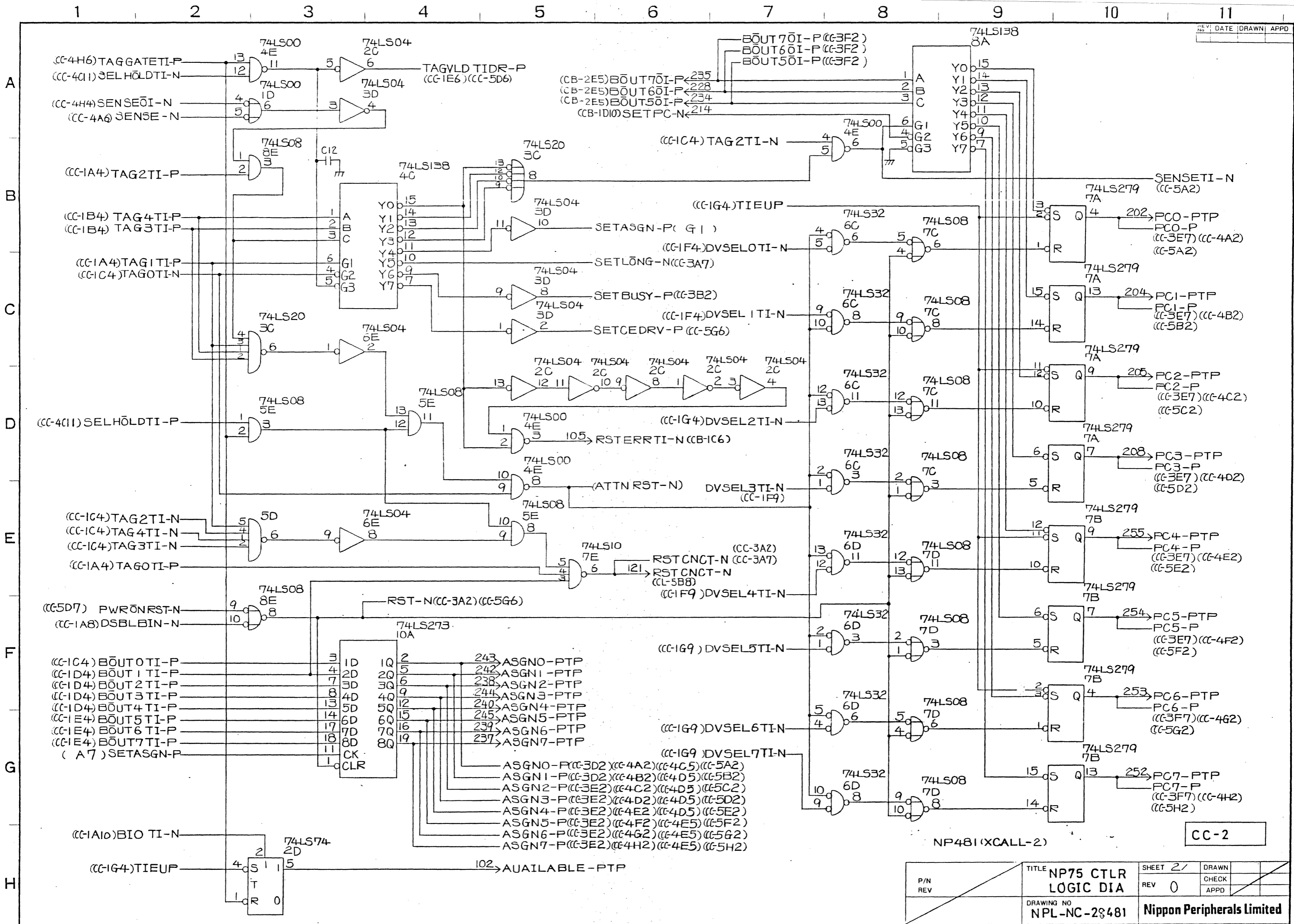
83-1



83-2

CC-1

P/N NP481	TITLE NP75 CTLR LOGIC DIA	SHEET 1/5	DRAWN K. TAKI 84-7/10
REV A		REV 0	CHECK
X CALL-2	DRAWING NO NPL-NC-28481	APPD. DANISHI 84.7.11	
			Nippon Peripherals Limited



83-3

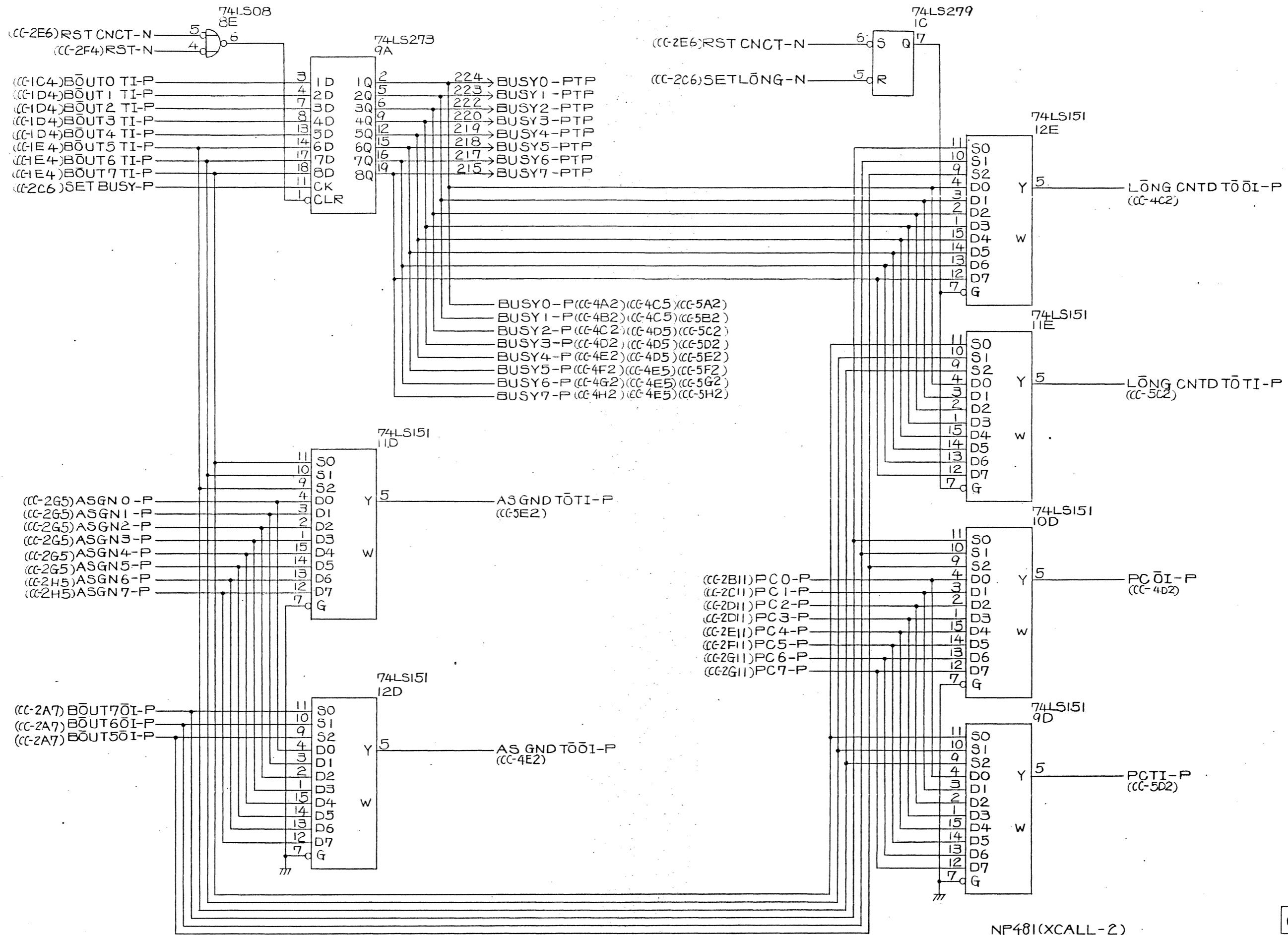
CC-2

NP481 (XCALL-2)

P/N REV	TITLE	SHEET 2/	DRAWN
	NP75 CTLR LOGIC DIA	REV 0	CHECK
DRAWING NO NPL-NC-28481		Nippon Peripherals Limited	

A
B
C
D
E
F
G
H

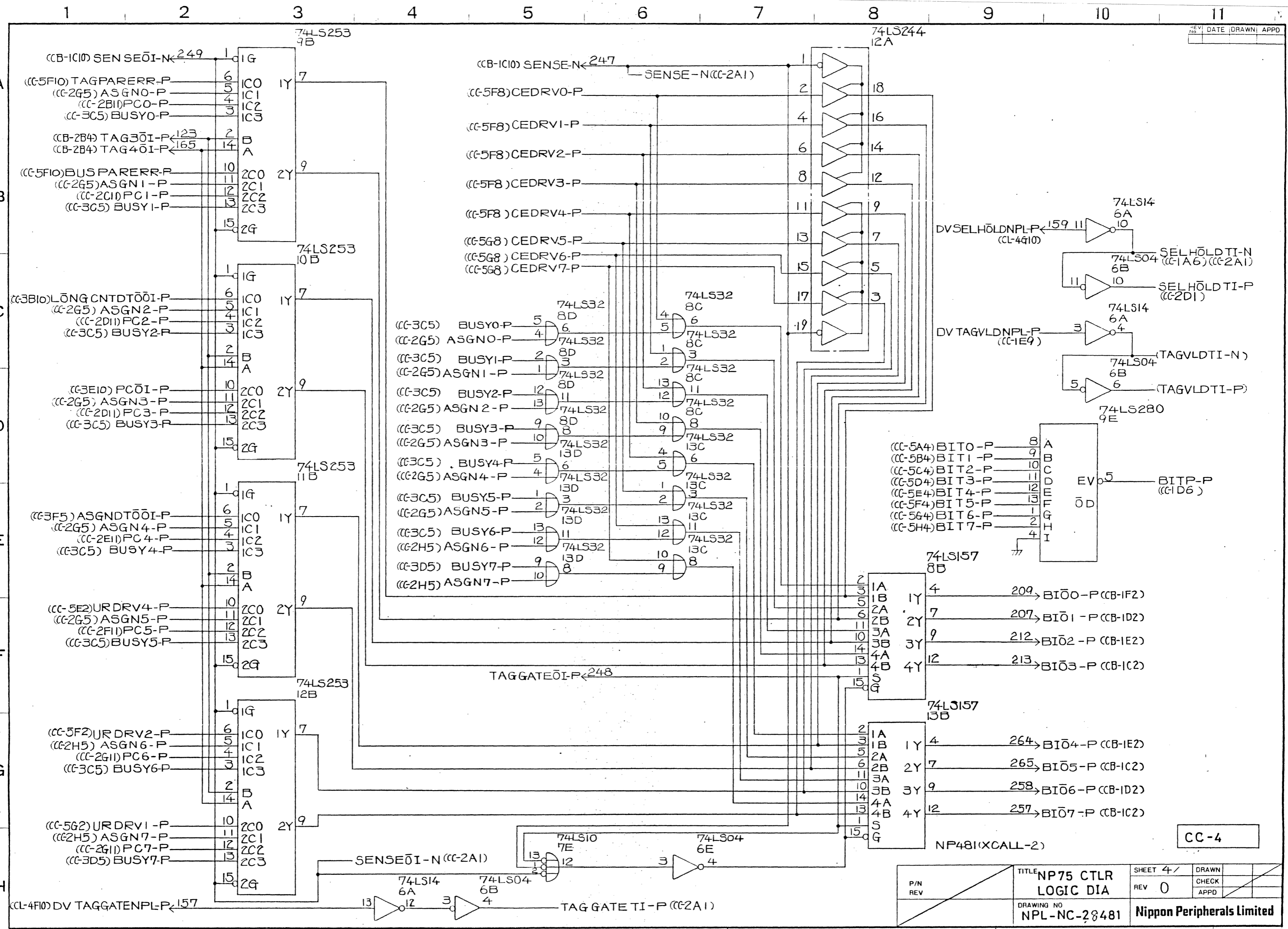
83-4



NP481(XCALL-2)

CC-3

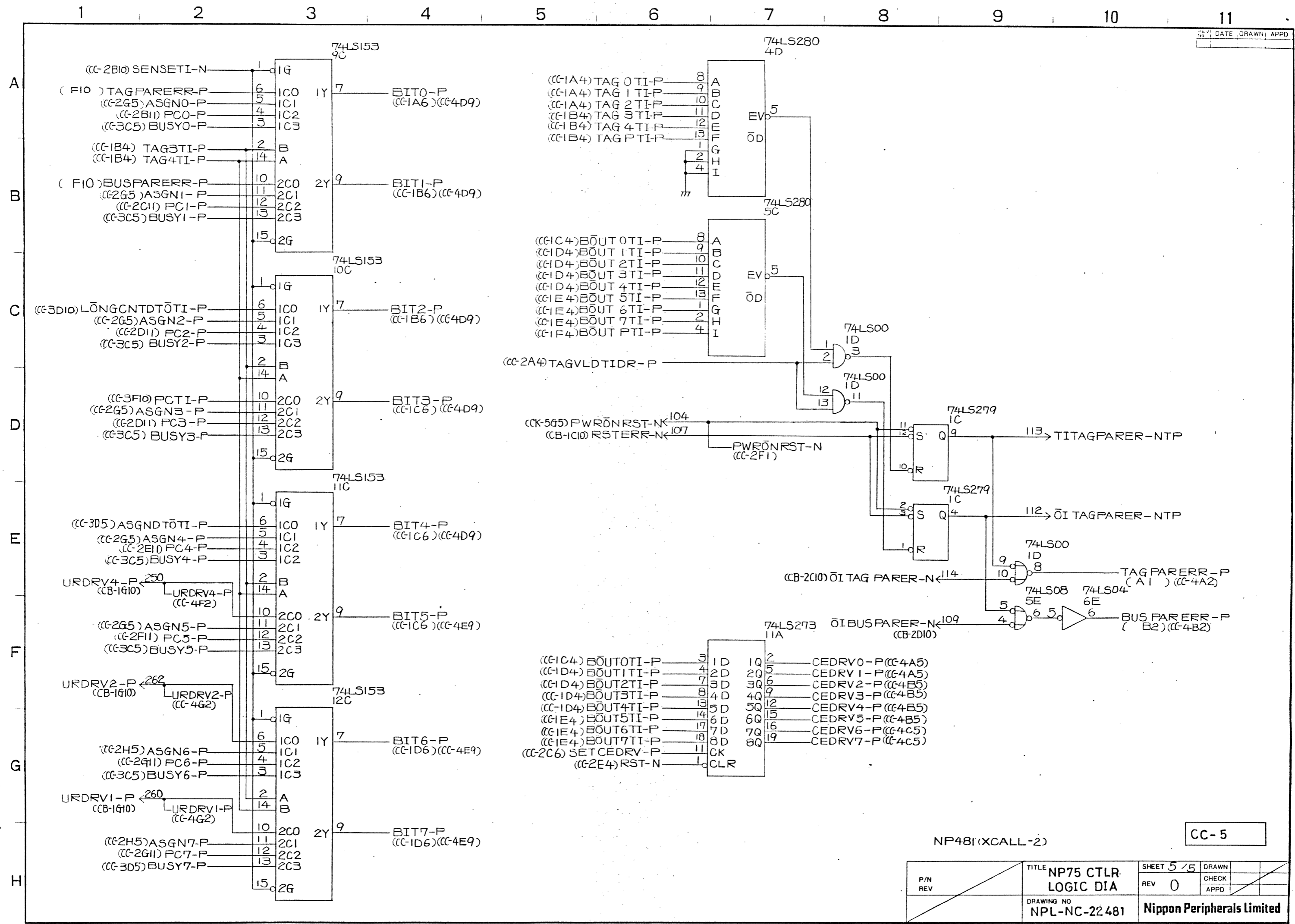
P/N REV	TITLE NP75 CTLR LOGIC DIA	SHEET 3 /	DRAWN
	DRAWING NO NPL-NC-28481	REV 0	CHECK APPD
Nippon Peripherals Limited			



83-5

CC-4

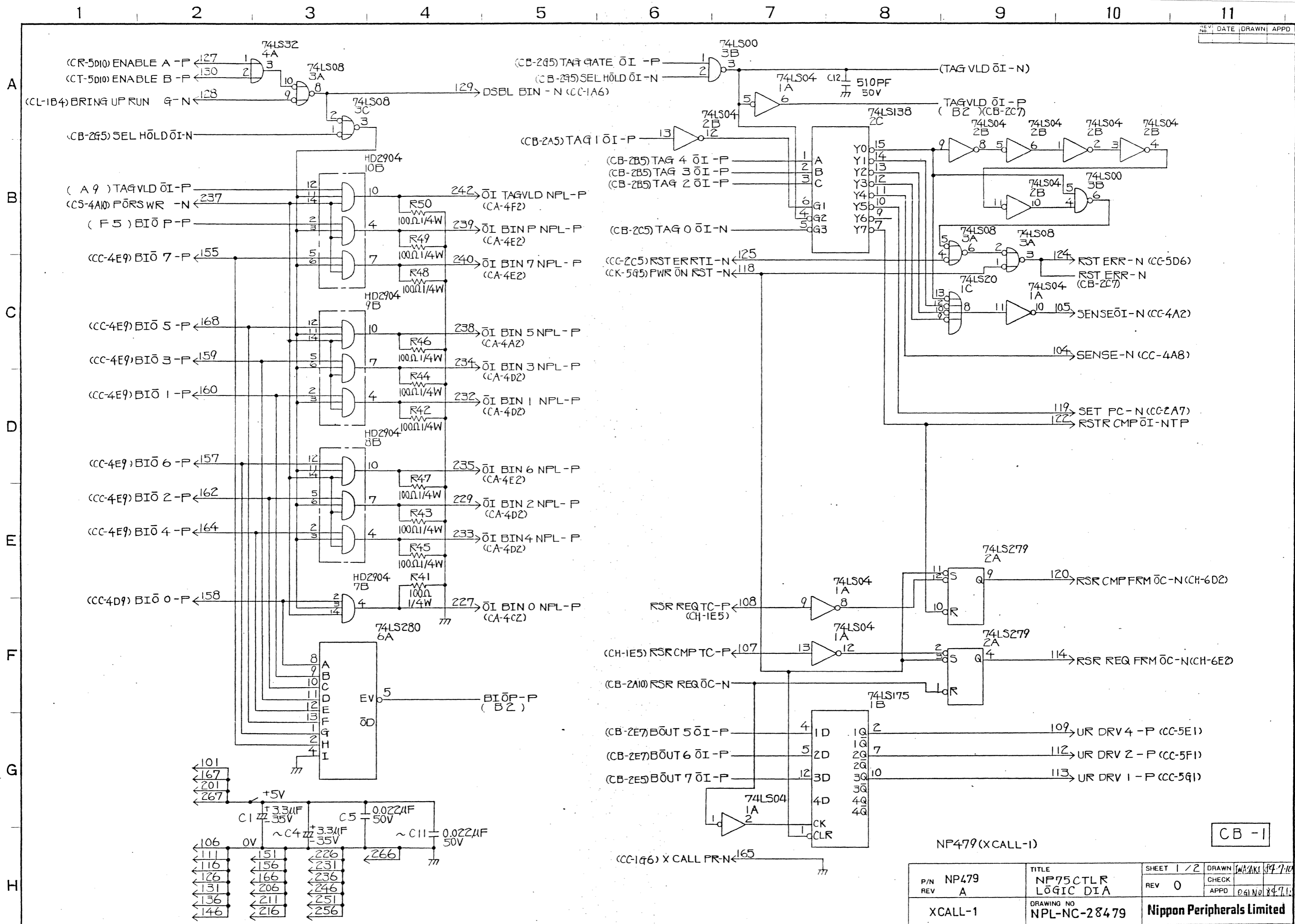
P/N REV	TITLE	SHEET 4/	DRAWN
	NP75 CTLR LOGIC DIA	REV 0	CHECK
DRAWING NO NPL-NC-28481		Nippon Peripherals Limited	



NP481(XCALL-2)

CC-5

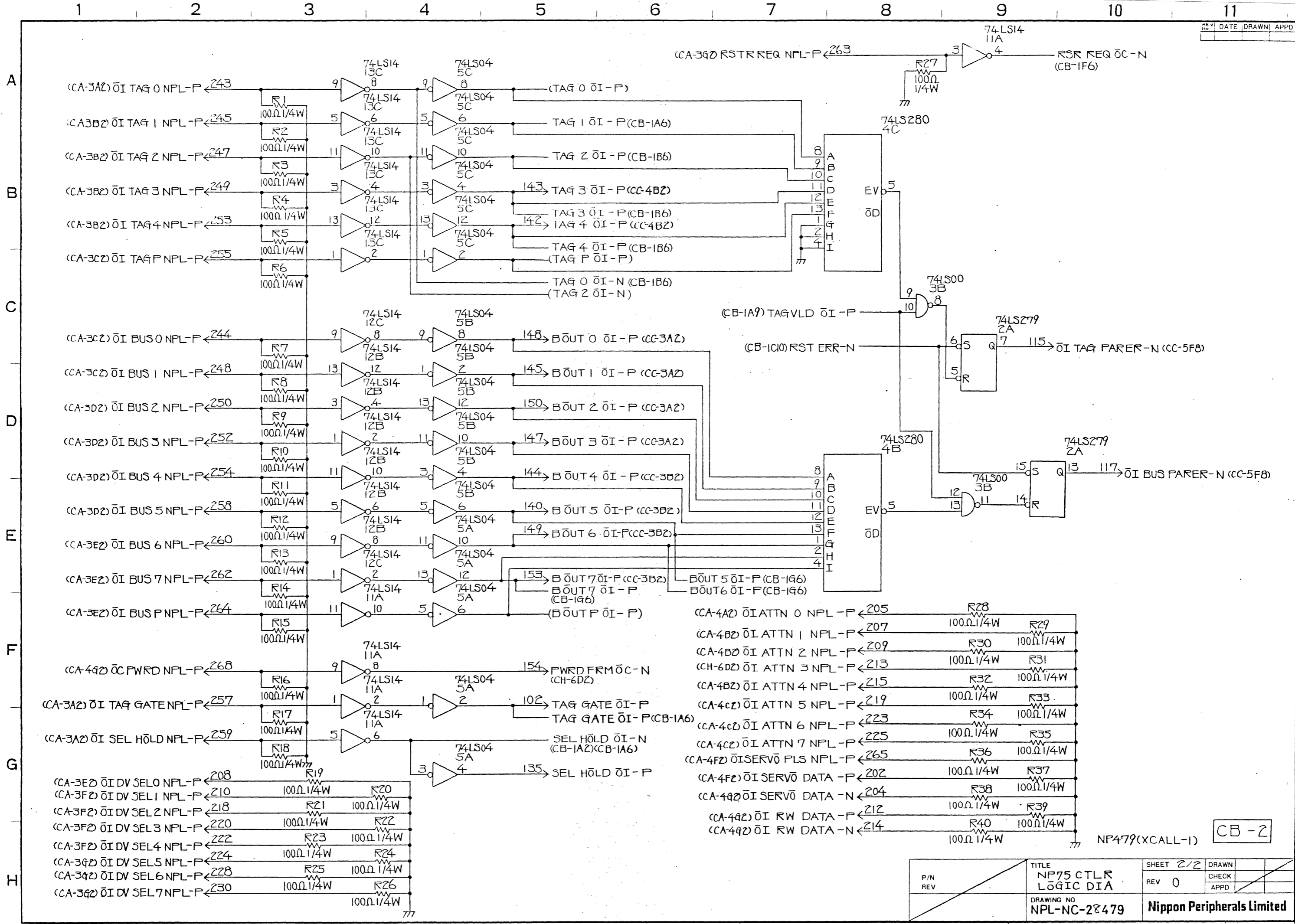
P/N REV	TITLE	SHEET	DRAWN
	NP75 CTLR LOGIC DIA	5 / 5	
DRAWING NO NPL-NC-22481	REV	CHECK	APPD
	0		
Nippon Peripherals Limited			



CB-1

P/N	NP479	TITLE	NP75CTLR LOGIC DIA	SHEET	1 / 2	DRAWN	WAKI 84-7-10
REV	A	CHECK		REV	0	APPD	OGI 84-7-10
XCALL-1		DRAWING NO	NPL-NC-28479	Nippon Peripherals Limited			

83-7

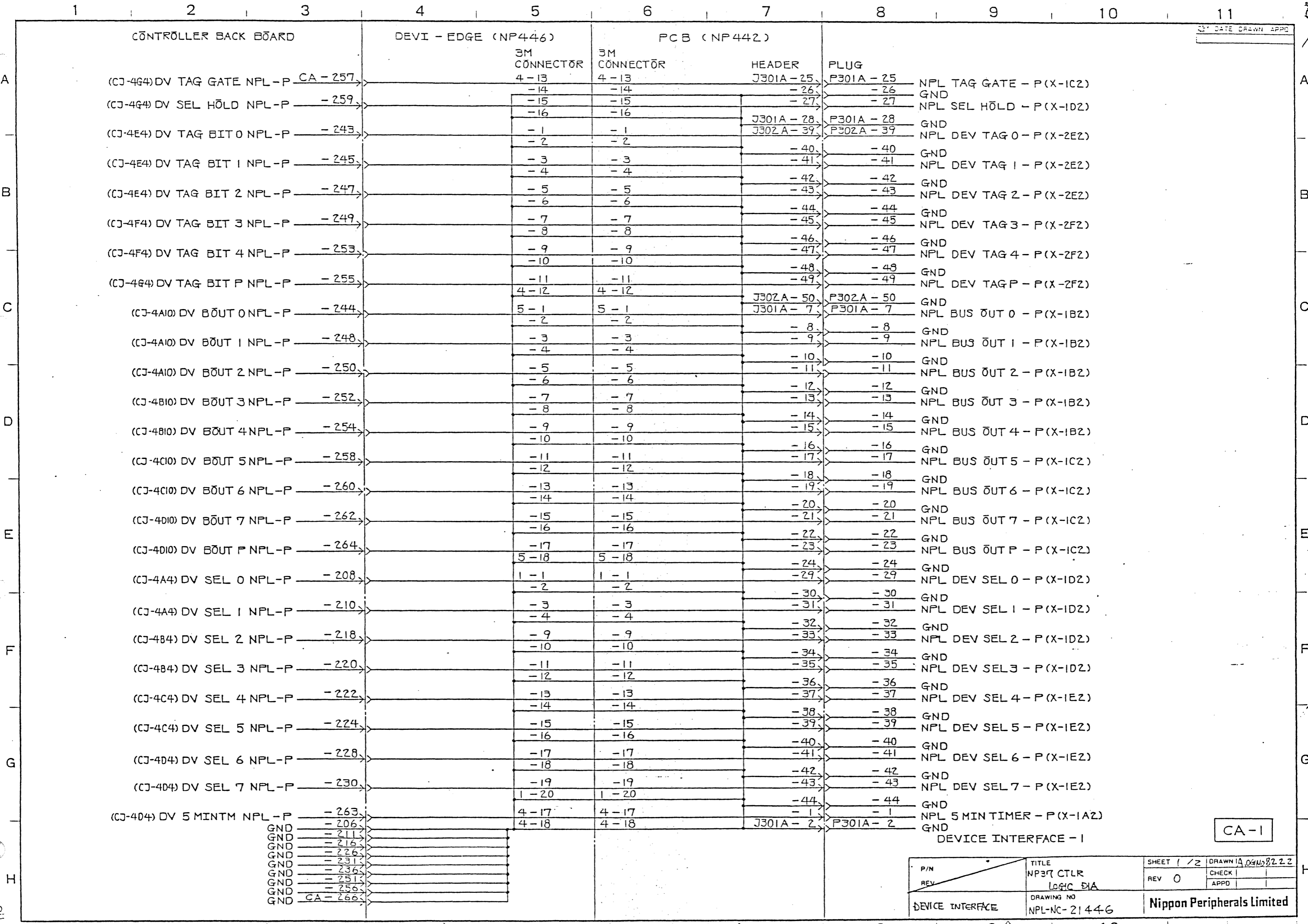


83-88

CB-2

NP479(XCALL-1)

P/N REV	TITLE NP75 CTLR LOGIC DIA DRAWING NO NPL-NC-28479	SHEET 2/2	DRAWN	
		REV 0	CHECK	
		Nippon Peripherals Limited		



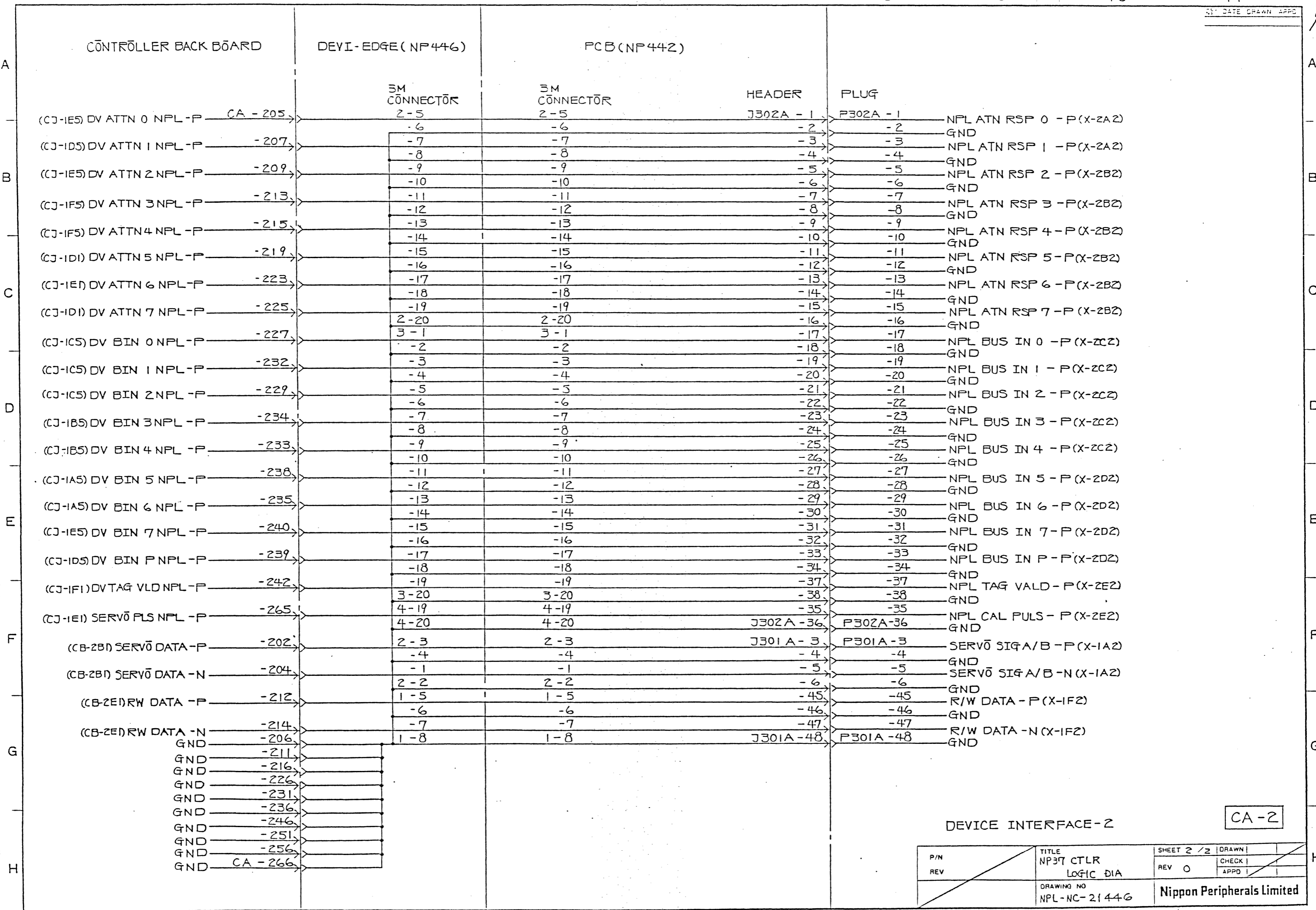
DATE DRAWN APPD

90

CA-1

P/N REV	TITLE NP37 CTRL LOGIC DIA	SHEET 1 / 2	DRAWN IA 06/02/22
	DEVICE INTERFACE	DRAWING NO NPL-NC-21446	REV 0 CHECK APPD
		Nippon Peripherals Limited	

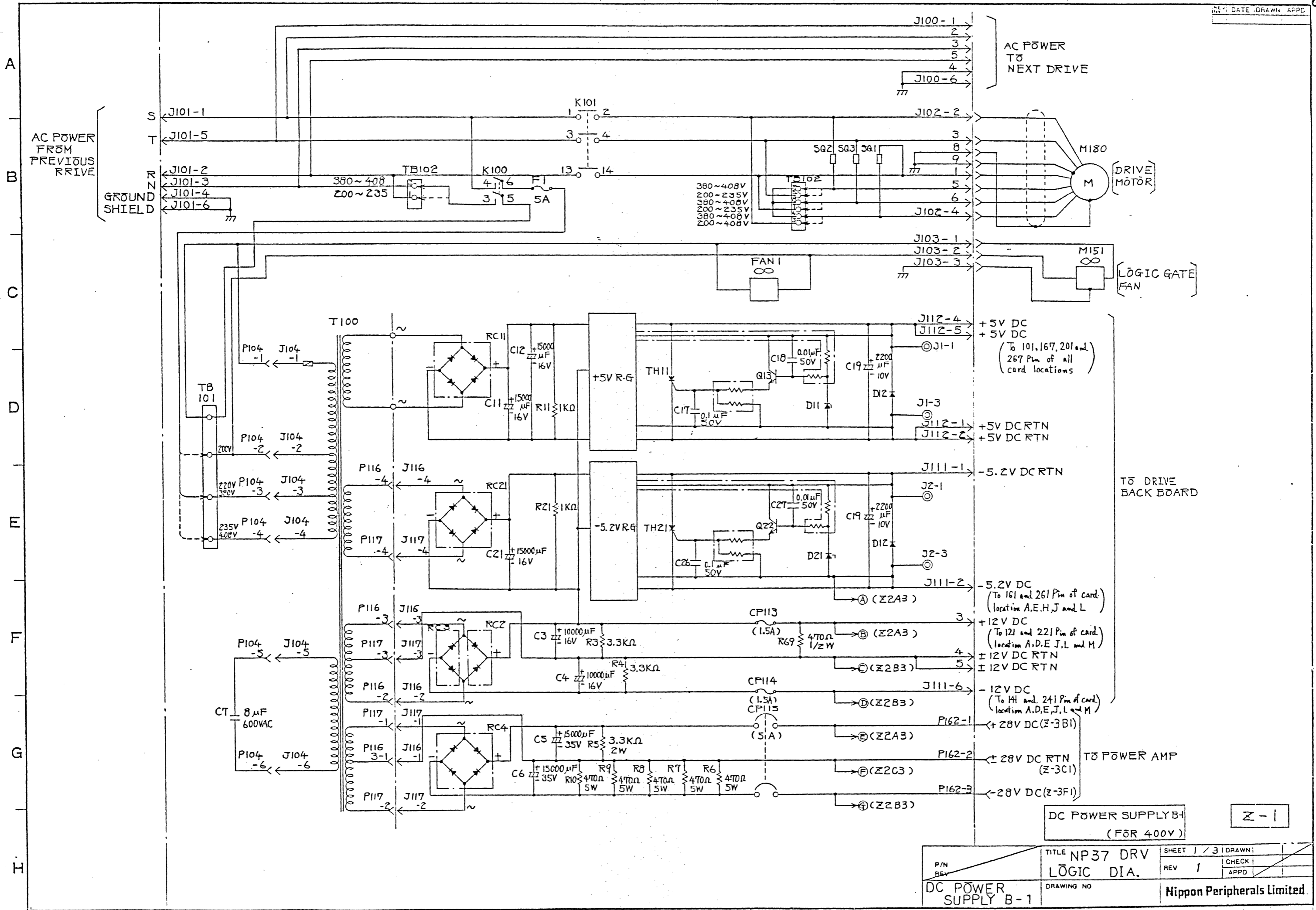
DEVICE INTERFACE - I



DEVICE INTERFACE - 2

CA-2

P/N	TITLE	SHEET 2 / 2	DRAWN
REV	NP37 CTLR	REV 0	CHECK
	LOGIC DIA		APPD
	DRAWING NO	Nippon Peripherals Limited	
	NPL-NC-21446		



AC POWER TO NEXT DRIVE

AC POWER FROM PREVIOUS DRIVE

GROUND SHIELD

M180 (DRIVE MOTOR)

M151 (LOGIC GATE FAN)

+5V DC
+5V DC
(To 101, 167, 201 and 267 Pin of all card locations)

+5V DC RTN
+5V DC RTN

TO DRIVE BACK BOARD

-5.2V DC RTN

-5.2V DC
(To 161 and 261 Pin of card location A, E, H, J and L)

+12V DC
(To 121 and 221 Pin of card location A, D, E, J, L and M)

±12V DC RTN
±12V DC RTN

-12V DC
(To 141 and 241 Pin of card location A, D, E, J, L and M)

+28V DC (Z-3B1)

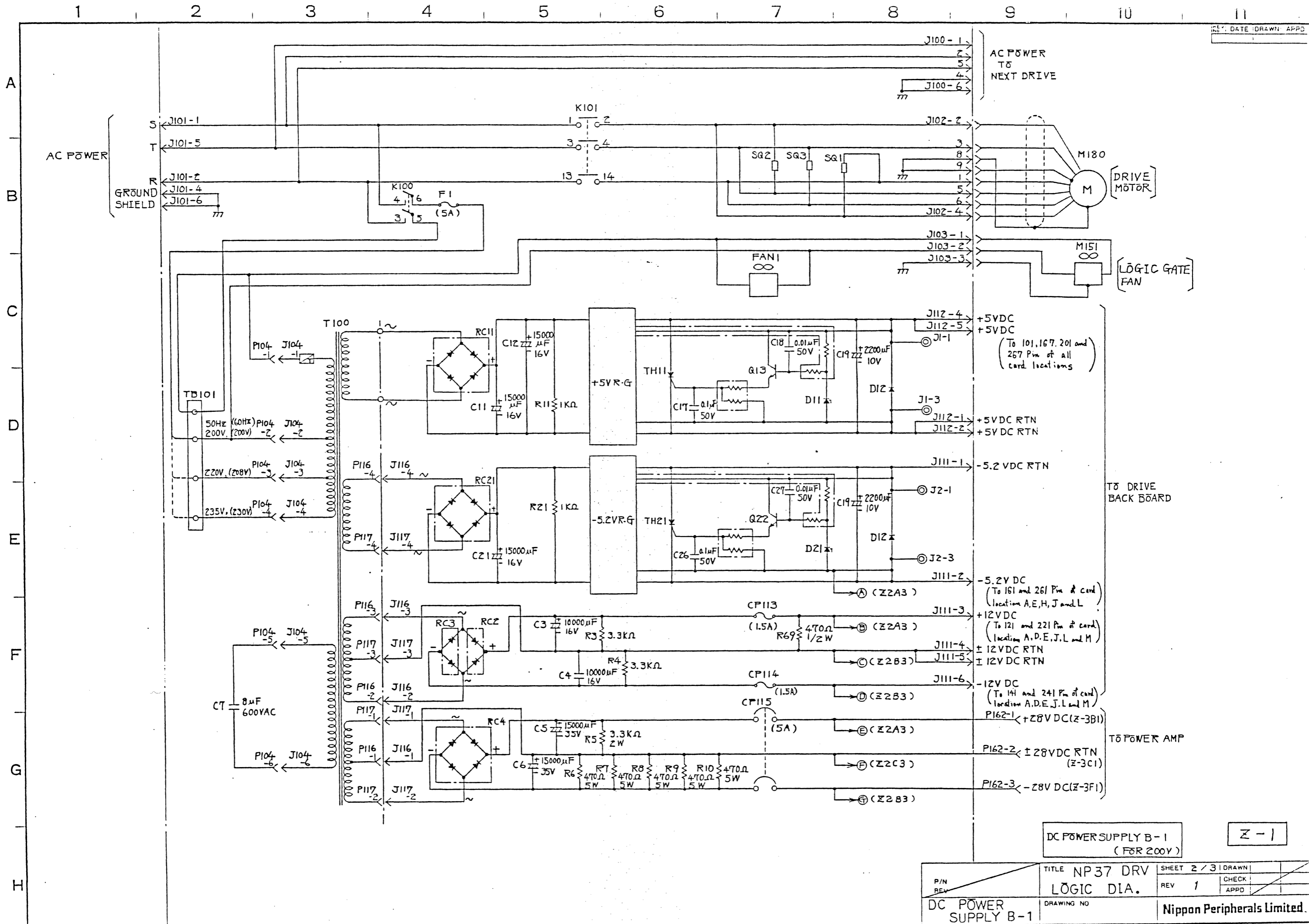
TO POWER AMP (Z-3C1)

±28V DC RTN (Z-3C1)
±28V DC (Z-3F1)

DC POWER SUPPLY B-1 (FOR 400V)

Z-1

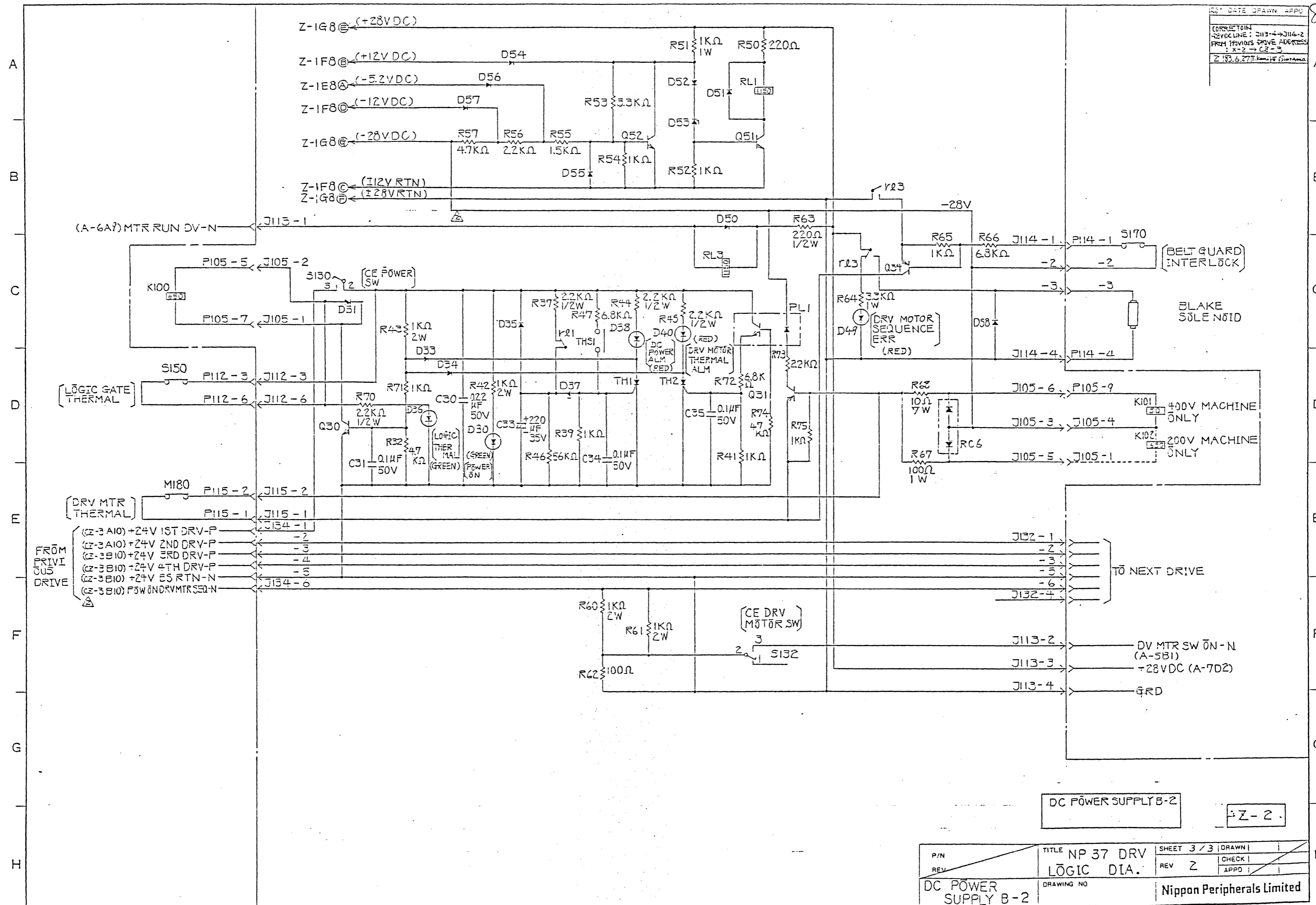
P/N REV	TITLE NP37 DRV LOGIC DIA.	SHEET 1 / 3 DRAWN	CHECK
	DRAWING NO	REV 1	APPD
DC POWER SUPPLY B-1		Nippon Peripherals Limited.	



DC POWER SUPPLY B-1 (FOR 200V) Z-1

P/N REV	TITLE	SHEET	DRAWN
	DC POWER SUPPLY B-1	2 / 3	
DRAWING NO	REV	CHECK	APPD
		1	
Nippon Peripherals Limited			

DATE DRAWN APPD
 CORRECTION
 -REV LINE: J113-4 → J114-2
 FROM PREVIOUS DRIVE ADDRESS
 : X-2 → CZ-3
 Z 193.6.27T. Kunita (Dietama)



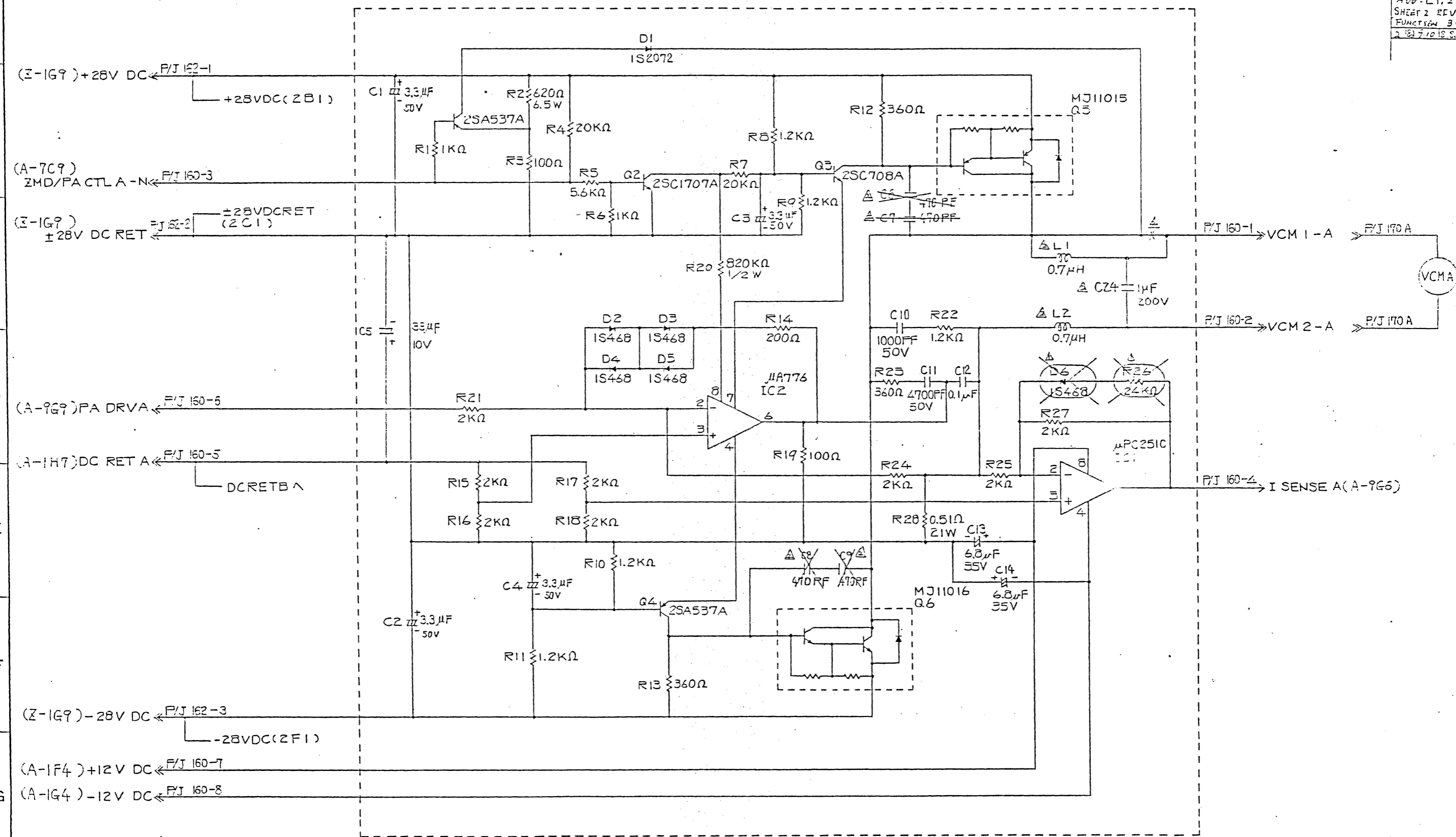
DC POWER SUPPLY B-2

Z-2

P/N	TITLE NP 37 DRV	SHEET 3 / 3	DRAWN
REV	LOGIC DIA.	REV 2	CHECK
DC POWER SUPPLY B-2	DRAWING NO	Nippon Peripherals Limited	

2T 1 2 3 4 5 6 7 8 9 10

DATE	DRWN.	APPD.
1982.5.19		
D6, R26 REMOVE		
1 182.5.19		
REMOVE: C6~9		
ADD: L1, 2 C24		
SHEET 2 REV1 → 2		
FUNCTION 3 → C		
2 182.7.10 IS		



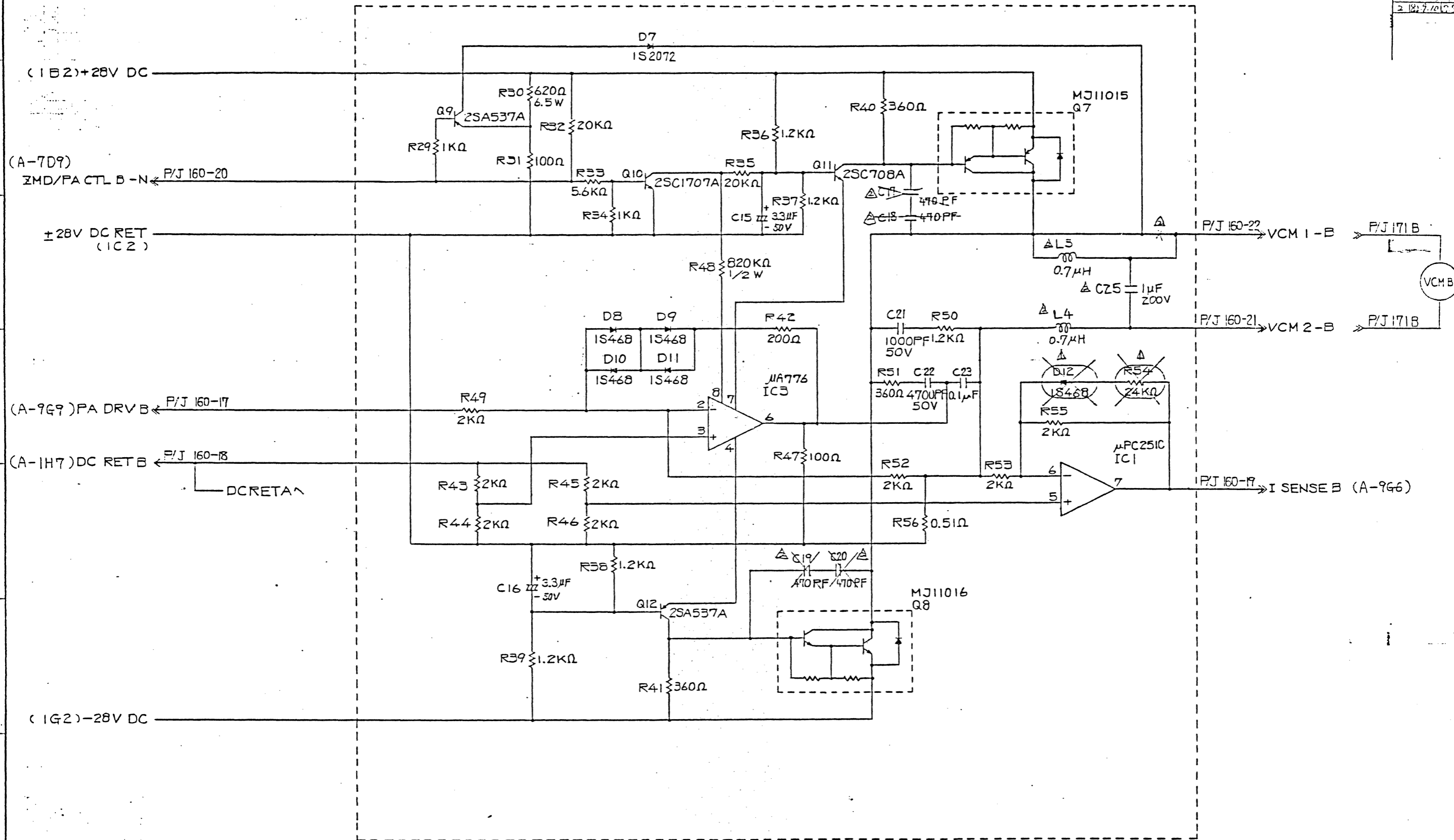
注. 指定なき抵抗はすべて1/4Wとする.

Z-3

NP 408 (PWR AMP)

P/N NP 408	TITLE NP408 CIRCUIT_DIA.	SHEET 1/2	DRAWN 1982.5.19
REV C		REV 2	CHECK 1982.5.19
PWR AMP	DRAWING NO NFL-NC-20408	APPD 1982.5.21	
		Nippon Peripherals Limited	

REV	DATE	DRAWN	APPO
1	82.5.19	kanjiya	
D12, R54 REMOVE			
REMOVED: C17, 20			
ADD: L3.4 C25			
2 82.7.012			



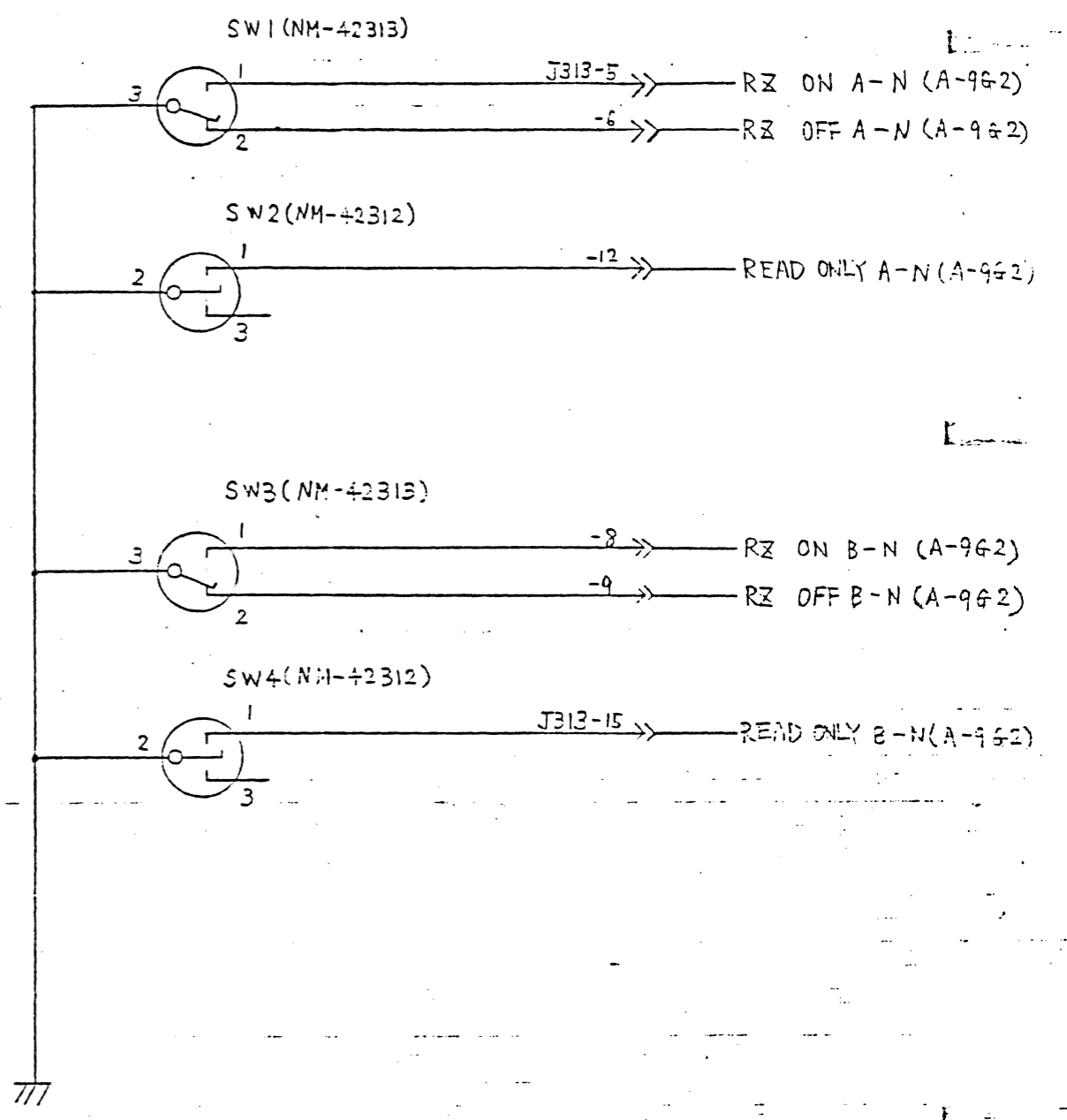
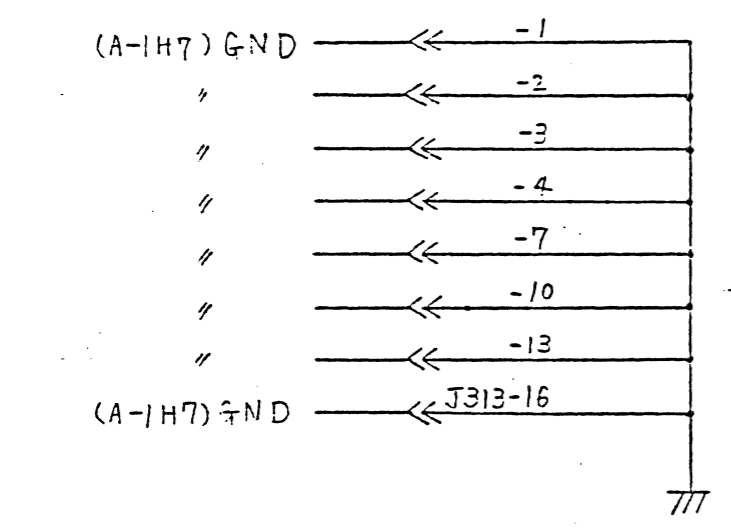
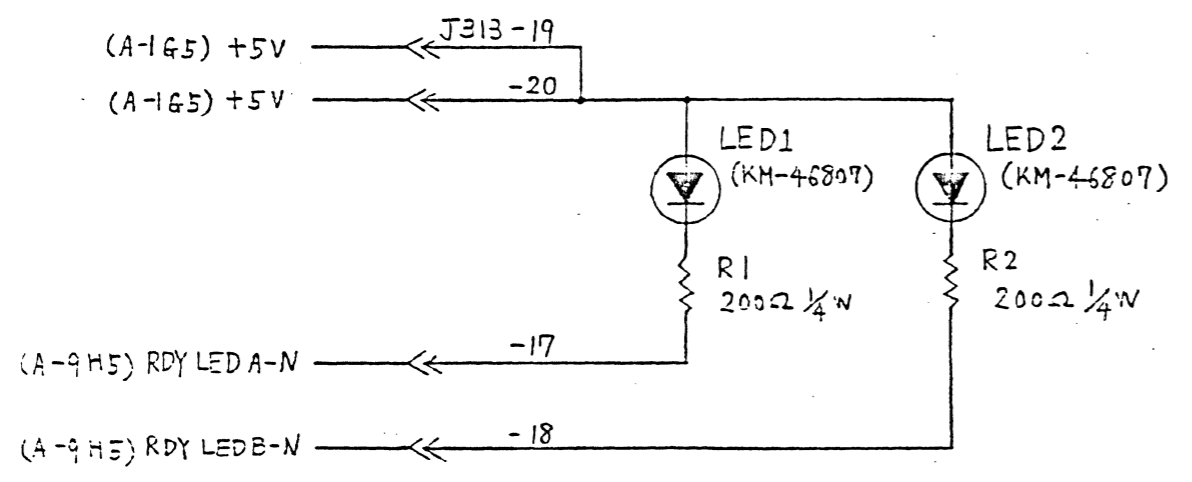
NP 408 (PWR AMP)

Z-4

P/N	TITLE	SHEET 2/2	DRAWN
REV	NP 408 CIRCUIT DIA.	REV 2	CHECK
	DRAWING NO		APPO
	NPL-NC-20408	Nippon Peripherals Limited	

1 2 3 4 5 6 7 8 9 10 11 91

A
B
C
D
E
F
G
H

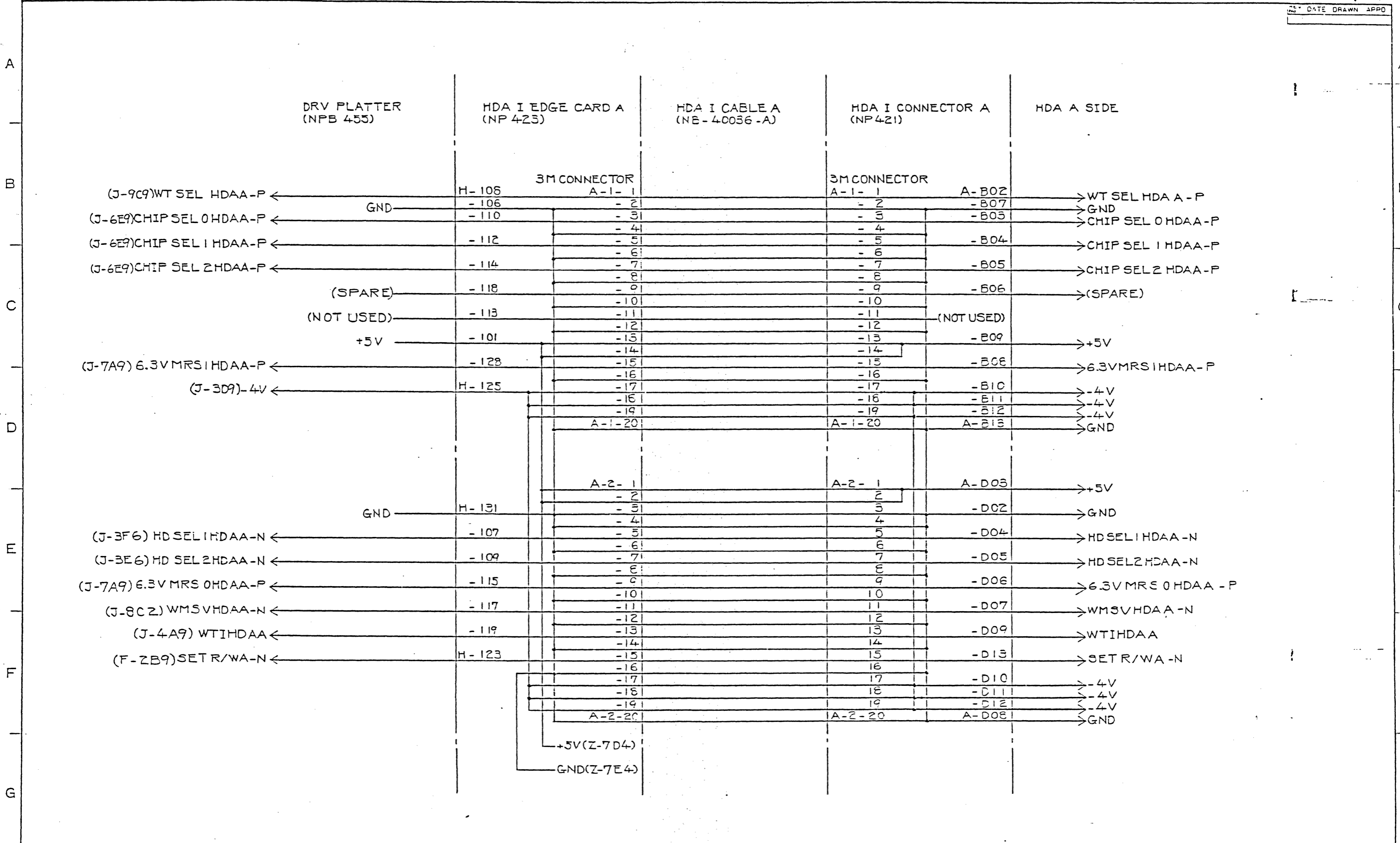


3-5

NP419 (DRIVE OPERATOR PANEL)

P/N NP 419	TITLE NP 37 DRV LOGIC - DIA.	SHEET 1/1	DRAWN
REV 0		REV 0	CHECK I APPD
DRIVE OPERATOR PANEL	DRAWING NO NPL-NC-20419	Nippon Peripherals Limited	

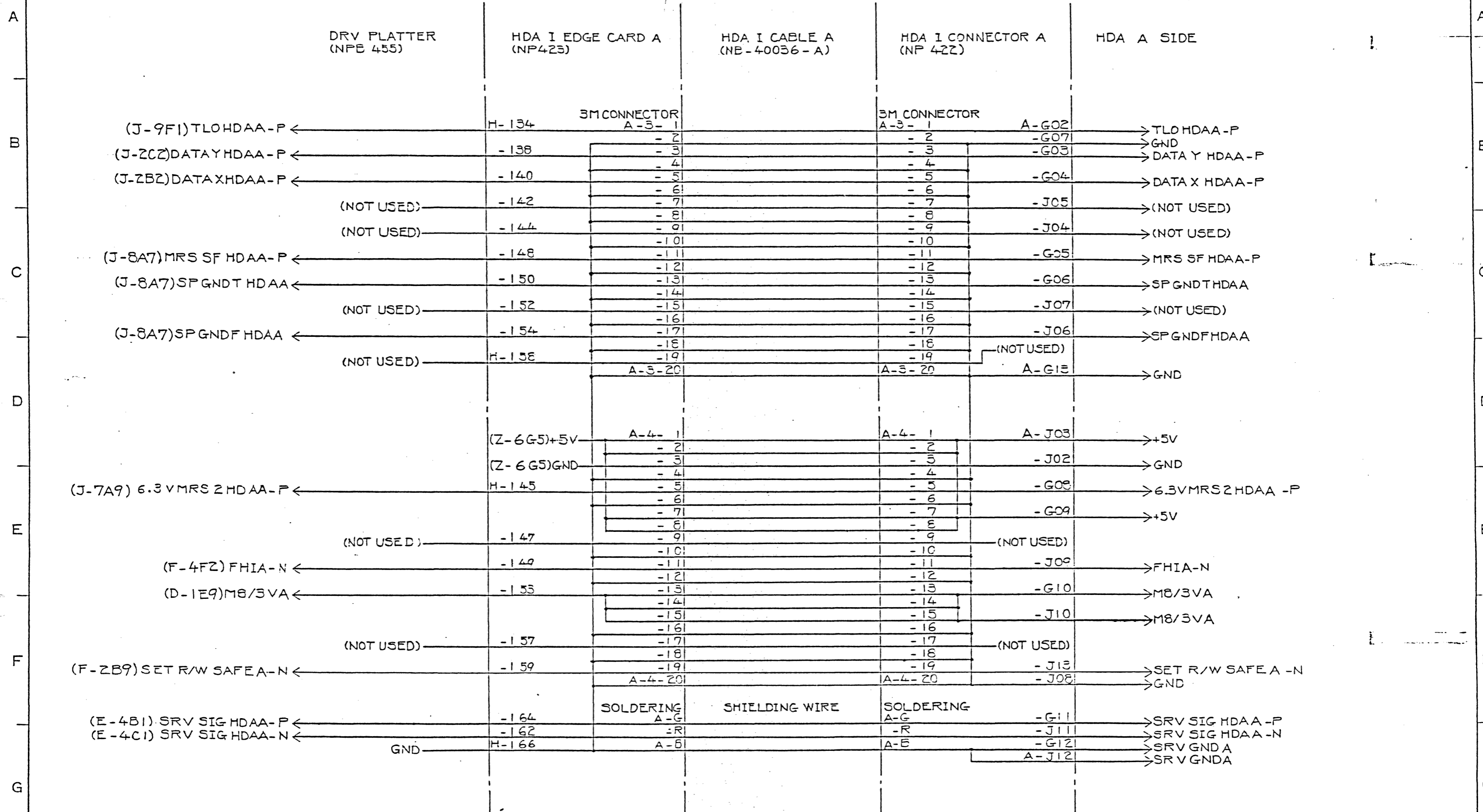
1 2 3 4 5 6 7 8 9 10



HDA INTERFACE A

Z-6

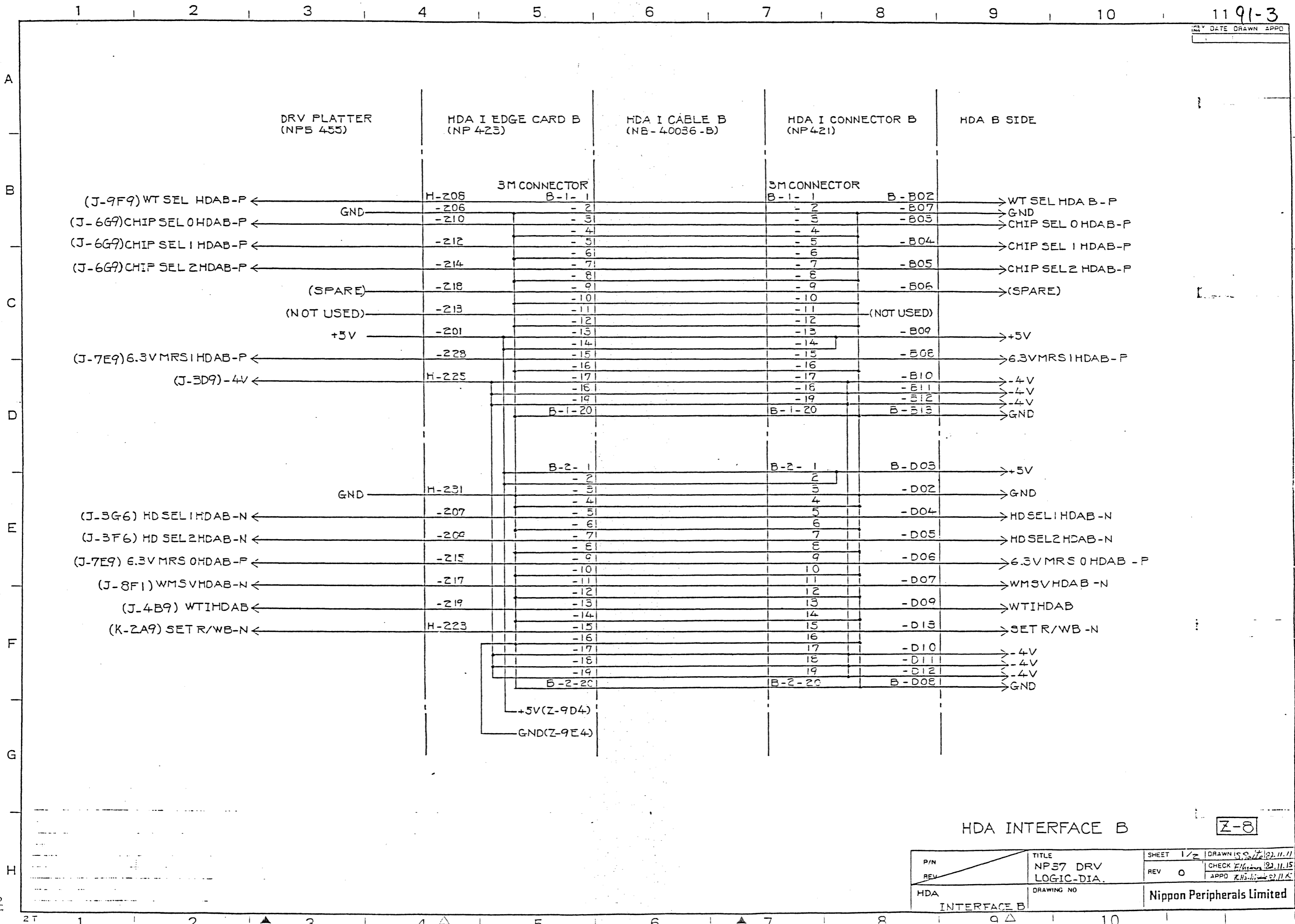
P/N	TITLE	SHEET	1/2	DRAWN	S. Saito 82.11.11
REV	NP37 DRV LOGIC-DIA.	REV	0	CHECK	F. Nishida 82.11.15
HDA	DRAWING NO	APPD	K. Nishida 82.11.16	Nippon Peripherals Limited	
INTERFACE A					



HDA INTERFACE A

Z-7

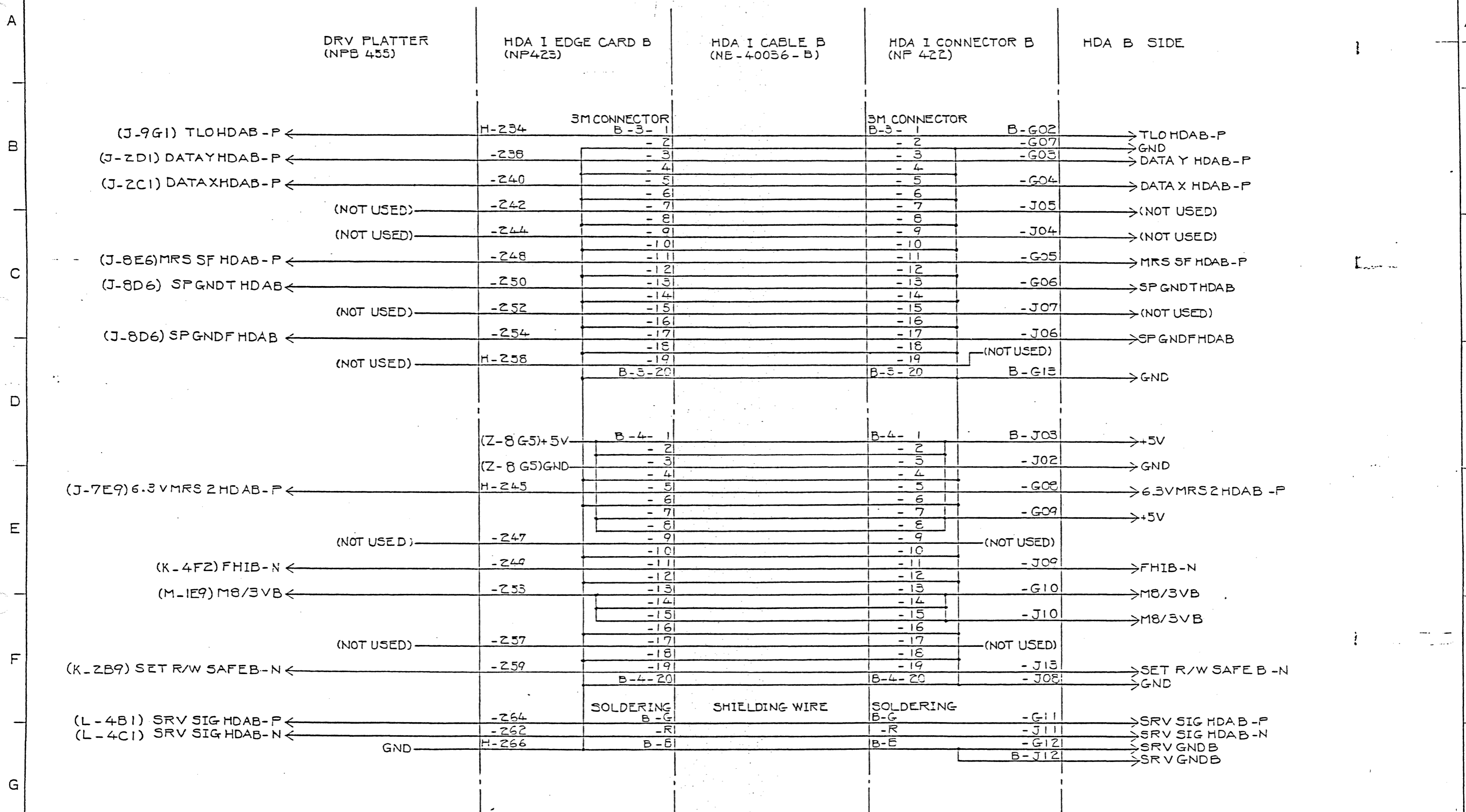
P/N REV	TITLE NP 37 DRV LOGIC-DIA.	SHEET 2/2	DRAWN
		REV 0	CHECK
HDA INTERFACE A		DRAWING NO	
		Nippon Peripherals Limited	



HDA INTERFACE B

Z-8

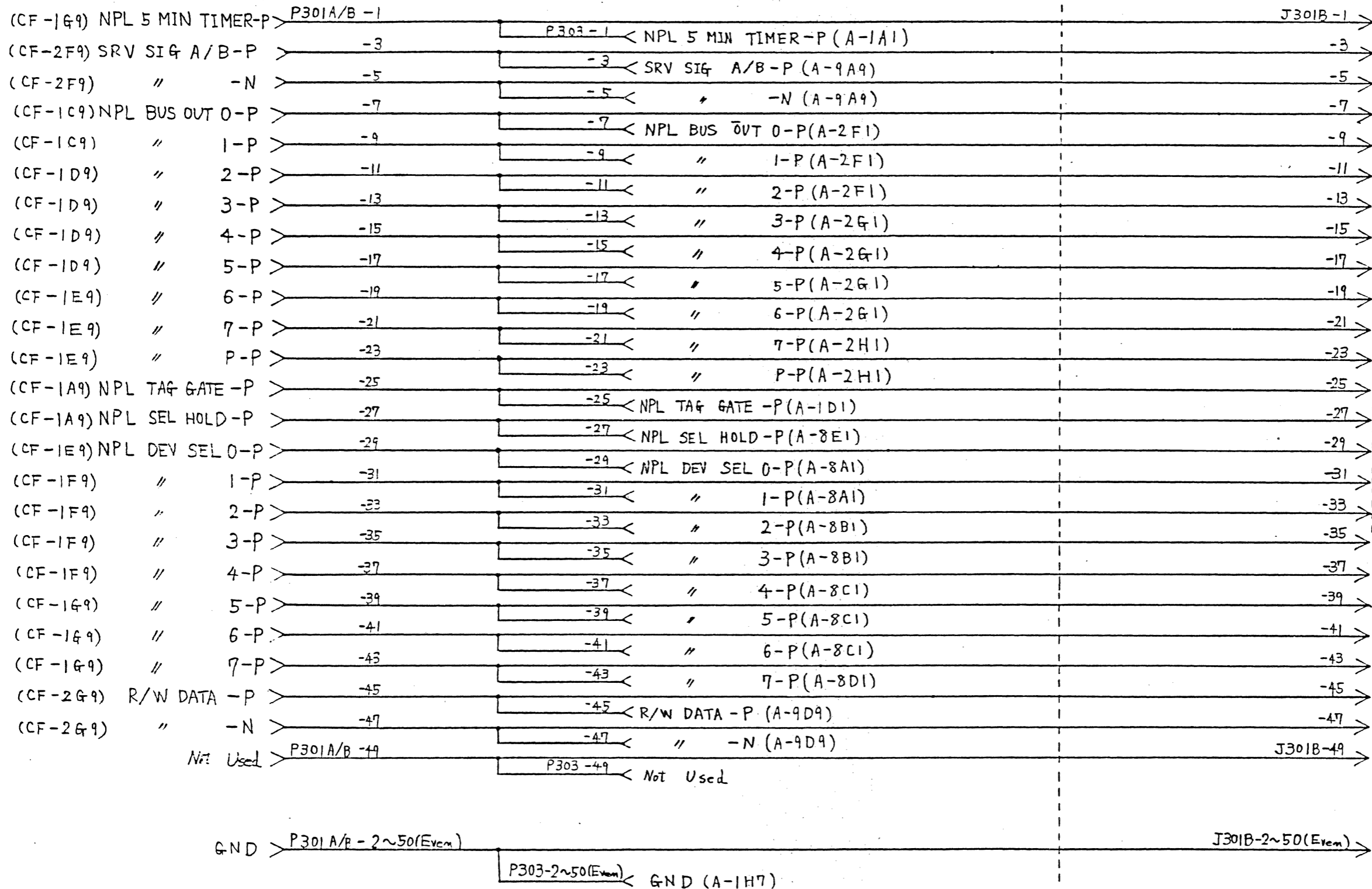
P/N	TITLE	SHEET	DRAWN
REV	NP37 DRV LOGIC-DIA.	1/2	12.11.11
HDA	DRAWING NO	REV	APPD
INTERFACE B		0	12.11.15
		Nippon Peripherals Limited	



HDA INTERFACE B Z-9

P/N	TITLE	SHEET	Z/Z	DRAWN
REV	NP 37 DRV LOGIC-DIA.	REV	0	CHECK
HDA INTERFACE B	DRAWING NO	Nippon Peripherals Limited		

NP420



These signals are transmitted to next drive by connecting P301 of next drive to J301 on PCB NP420.

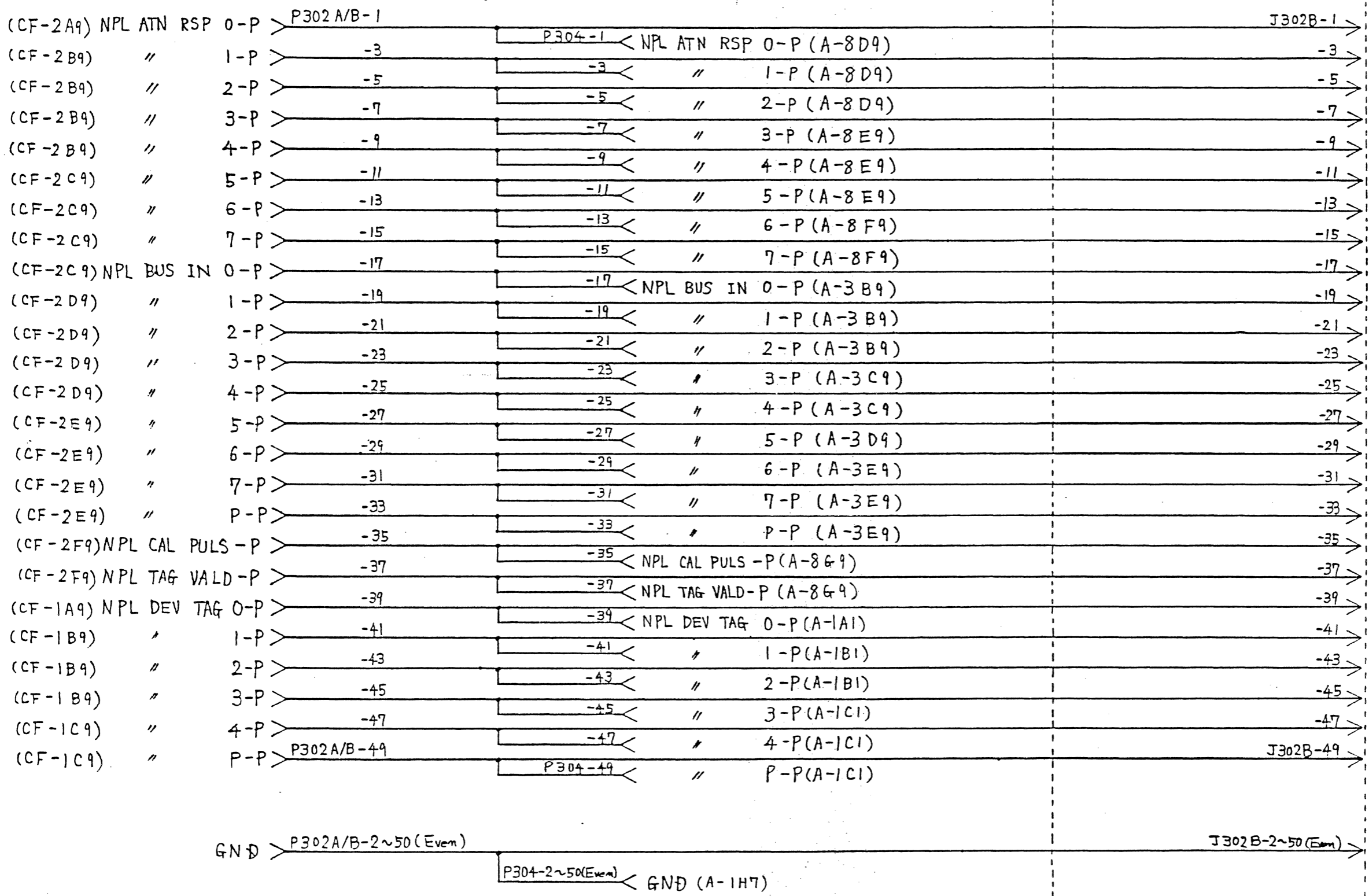
On last drive of the string, DVI terminator NP4-16 (cf X-3) must be installed to J301 instead of P301.

DRIVE INTERFACE 1

X-1

P/N	TITLE	SHEET 1/3	DRAWN
REV	NP37 DRV LOGIC DIA.	REV 0	CHECK APPD
DRIVE INTERFACE 1		DRAWING NO	
Nippon Peripherals Limited			

NP420



These signals are transmitted to next drive by connecting P302 of next drive to J302 on PCB NP420.

On last drive of the string, DVI terminator NP416 (cf X-3) must be installed to J302 instead of P302.

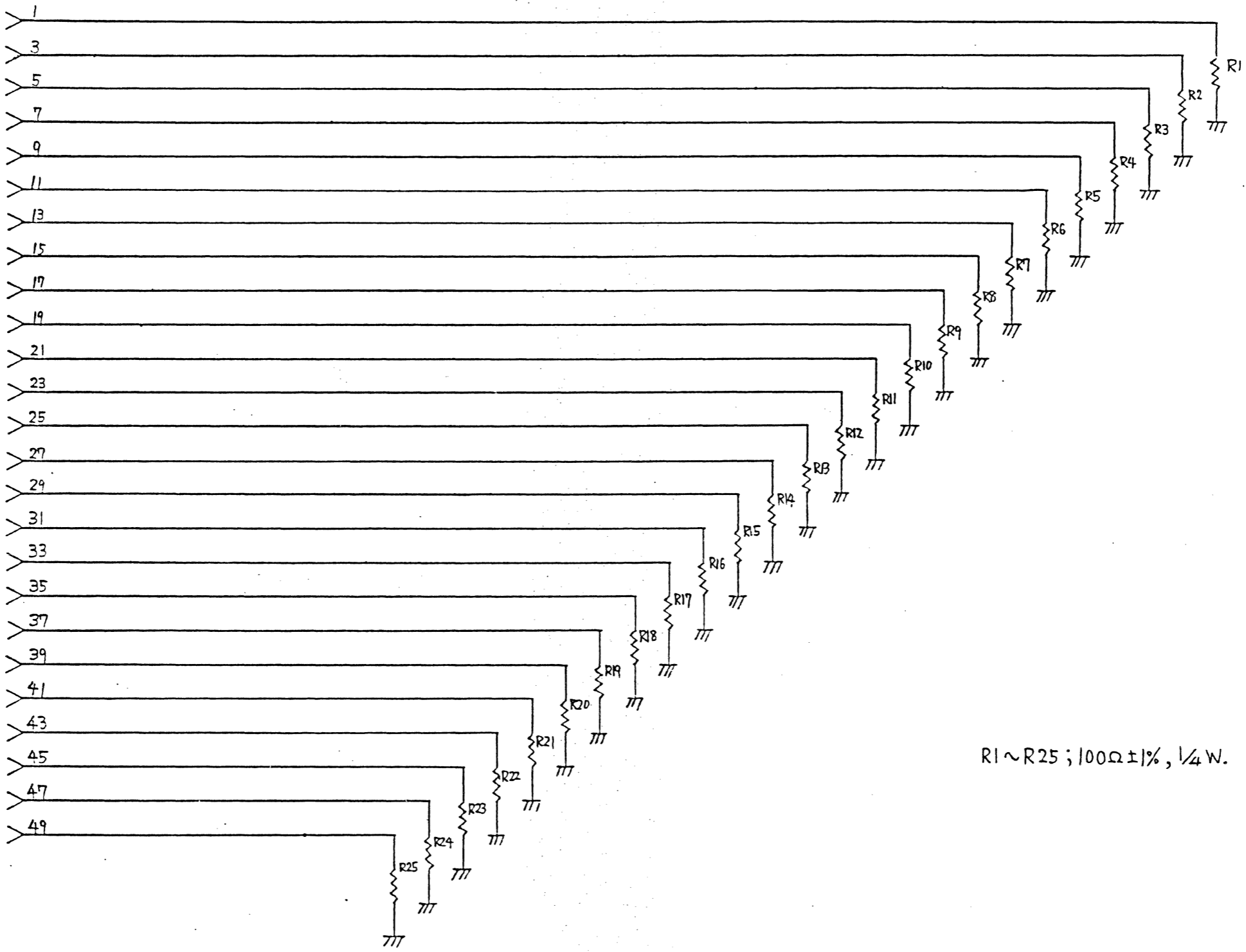
DRIVE INTERFACE 2.

X-2

P/N	TITLE	SHEET 2/3	DRAWN
REV	NP37 DRV LOGIC DIA.	REV 0	CHECK
DRIVE INTERFACE 2	DRAWING NO	Nippon Peripherals Limited	

A
B
C
D
E
F
G
H

A
B
C
D
E
F
G
H



R1~R25; 100Ω±1%, 1/4 W.

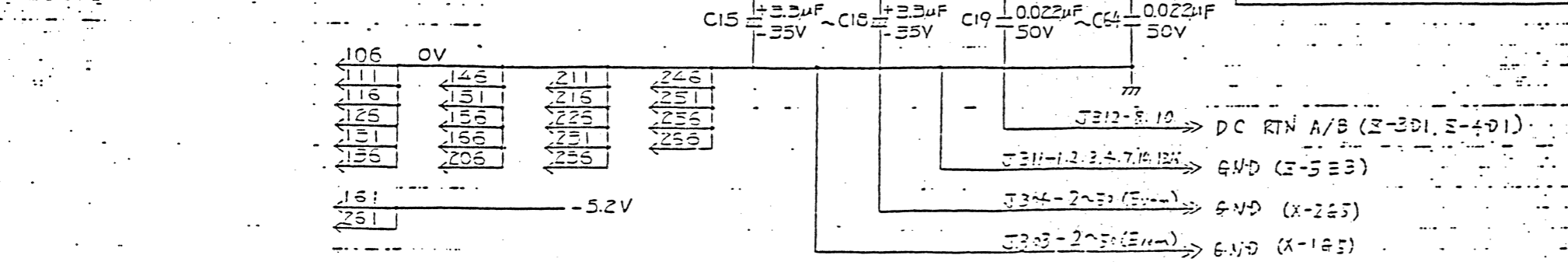
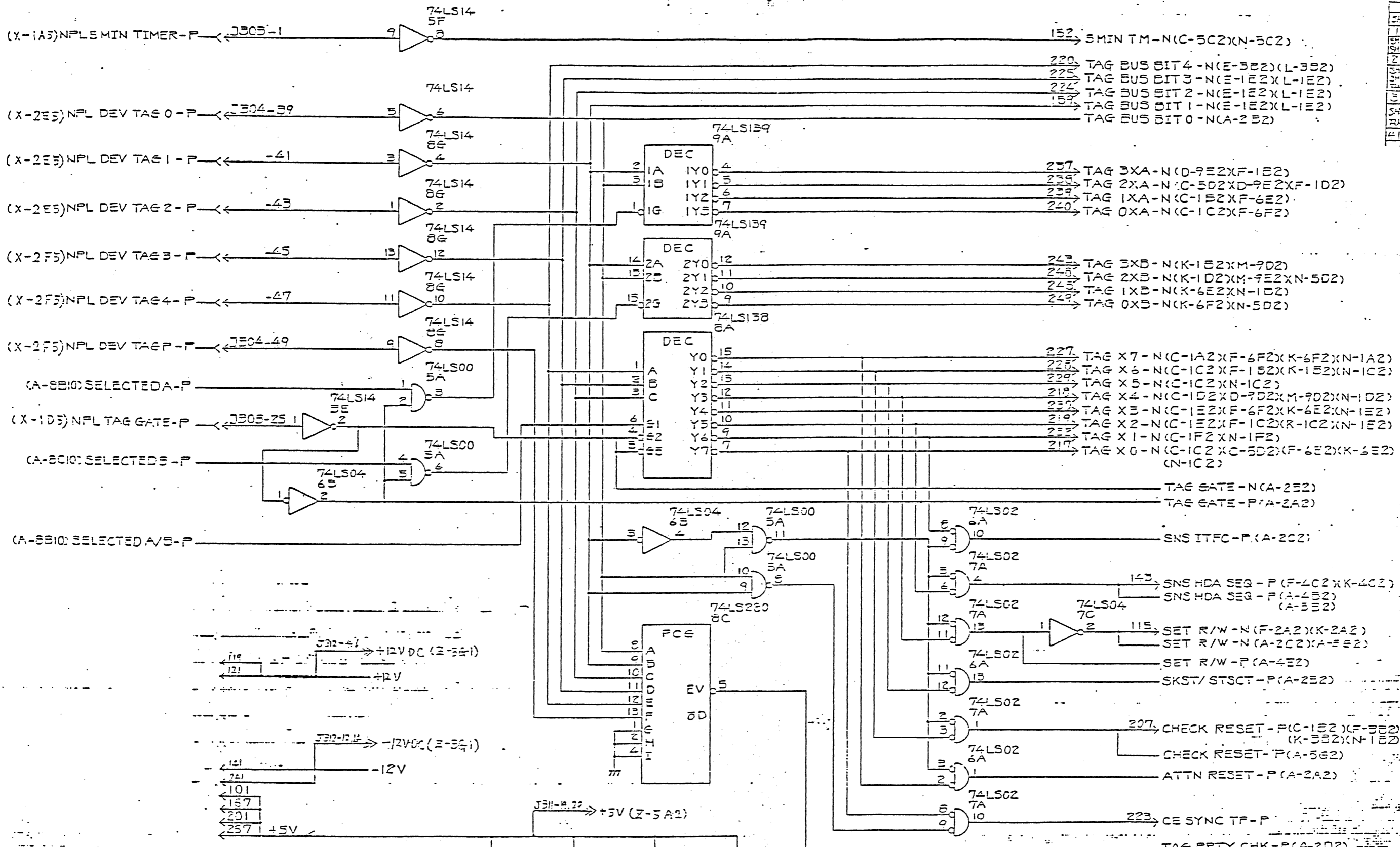
X-3

NP416 (DVI Terminator)

P/N	NP 416	TITLE	NP37 DRV LOGIC DIA.	SHEET	3/3	DRAWN	
REV		REV		APPD			
DVI Terminator			DRAWING NO	Nippon Peripherals Limited			

26

DATE DRAWN	2008
SHEET	7
REV	0
REV	1
REV	2
REV	3
REV	4
REV	5
REV	6
REV	7
REV	8
REV	9
REV	10
REV	11
REV	12
REV	13
REV	14
REV	15
REV	16
REV	17
REV	18
REV	19
REV	20
REV	21
REV	22
REV	23
REV	24
REV	25
REV	26
REV	27
REV	28
REV	29
REV	30
REV	31
REV	32
REV	33
REV	34
REV	35
REV	36
REV	37
REV	38
REV	39
REV	40
REV	41
REV	42
REV	43
REV	44
REV	45
REV	46
REV	47
REV	48
REV	49
REV	50



P/N NP 410
REV F

TITLE
NF 37 DRV
LOGIC DIA.

SHEET 1/2
REV 4

DRAWING NO
NPL-NC-21410

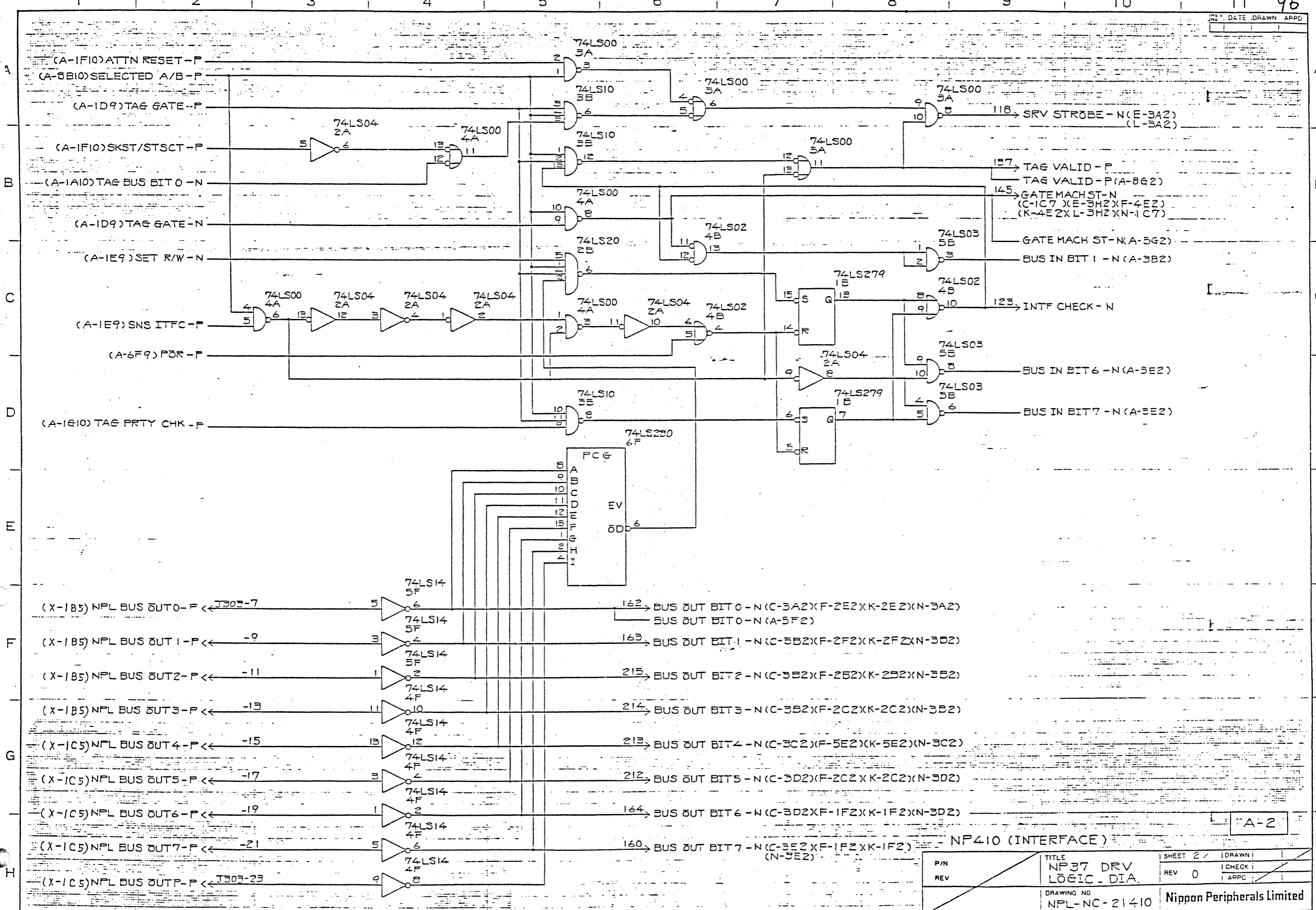
INTERFACE

APPD

CHECKED

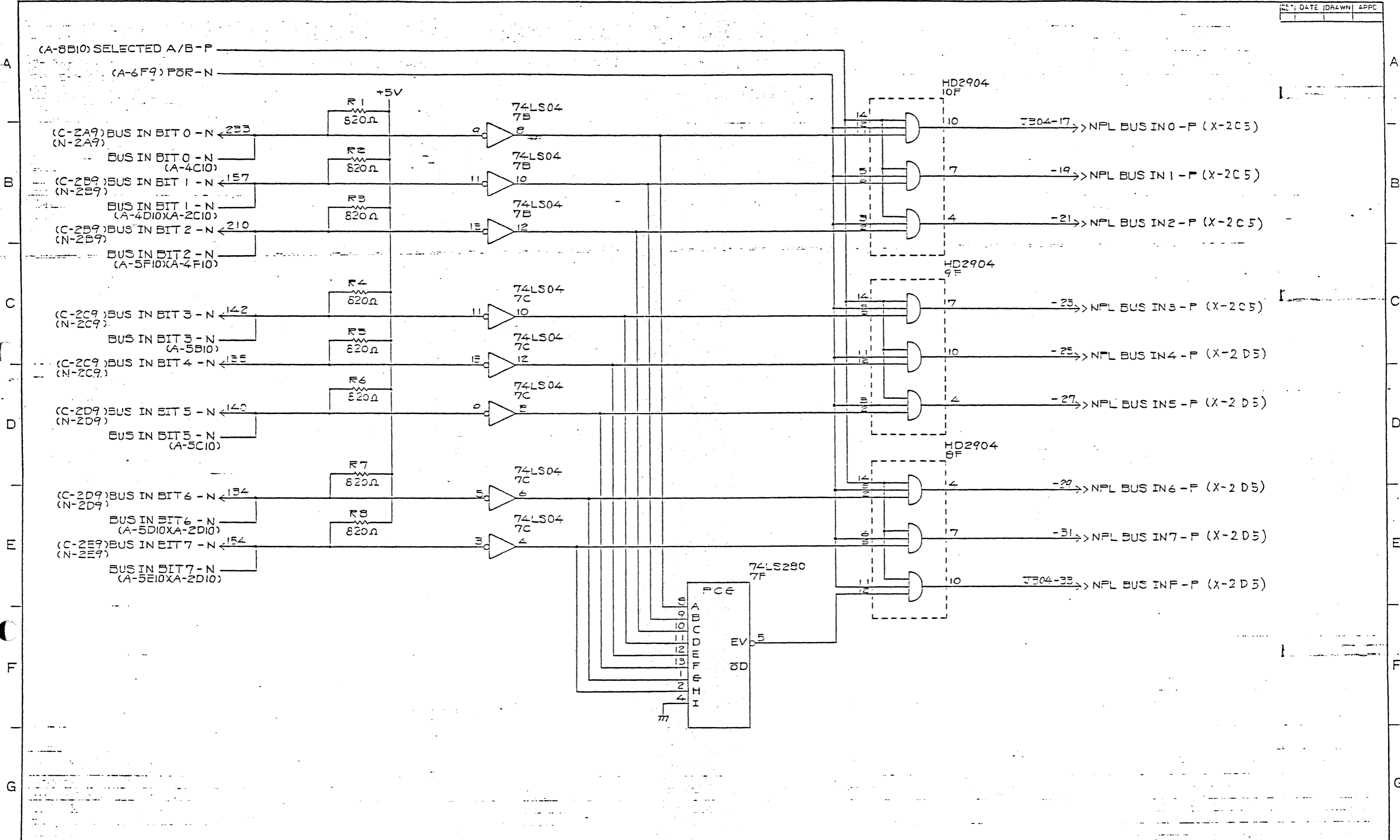
DATE

Nippon Peripherals Limited
NC-21410



A-2

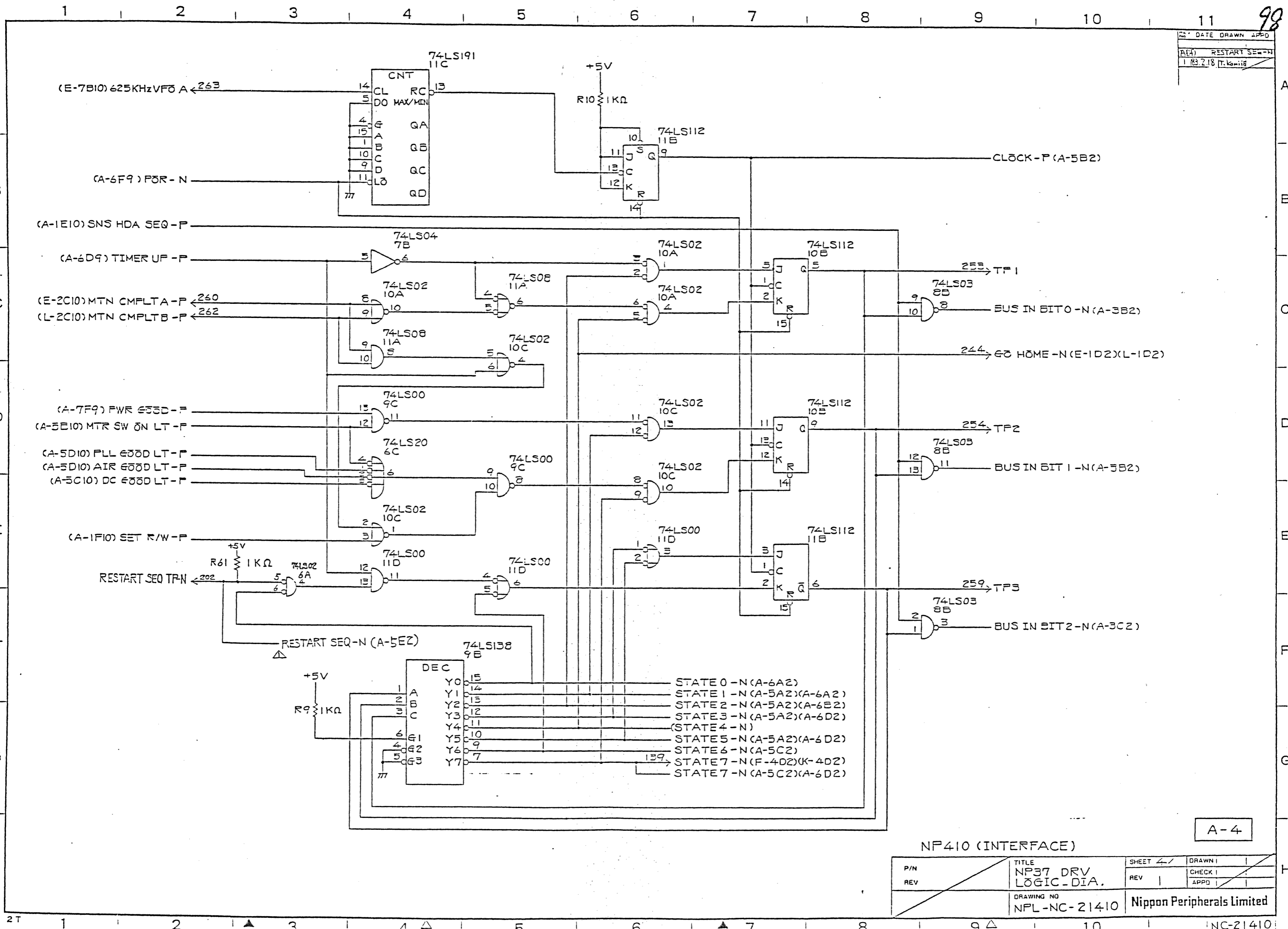
P/N REV	TITLE NP37 DRV LOGIC - DIA.	SHEET 2 / 1	DRAWN
	DRAWING NO NPL-NC-21410	REV 0	CHECK APPD
NP410 (INTERFACE)		Nippon Peripherals Limited	



A-3

NP410 (INTERFACE)

P/N	REV	TITLE	SHEET 5 /	DRAWN
		NP37 DRV LOGIC DIA.	REV 0	CHECK
DRAWING NO		Nippon Peripherals Limited		
NPL-NC-21410				



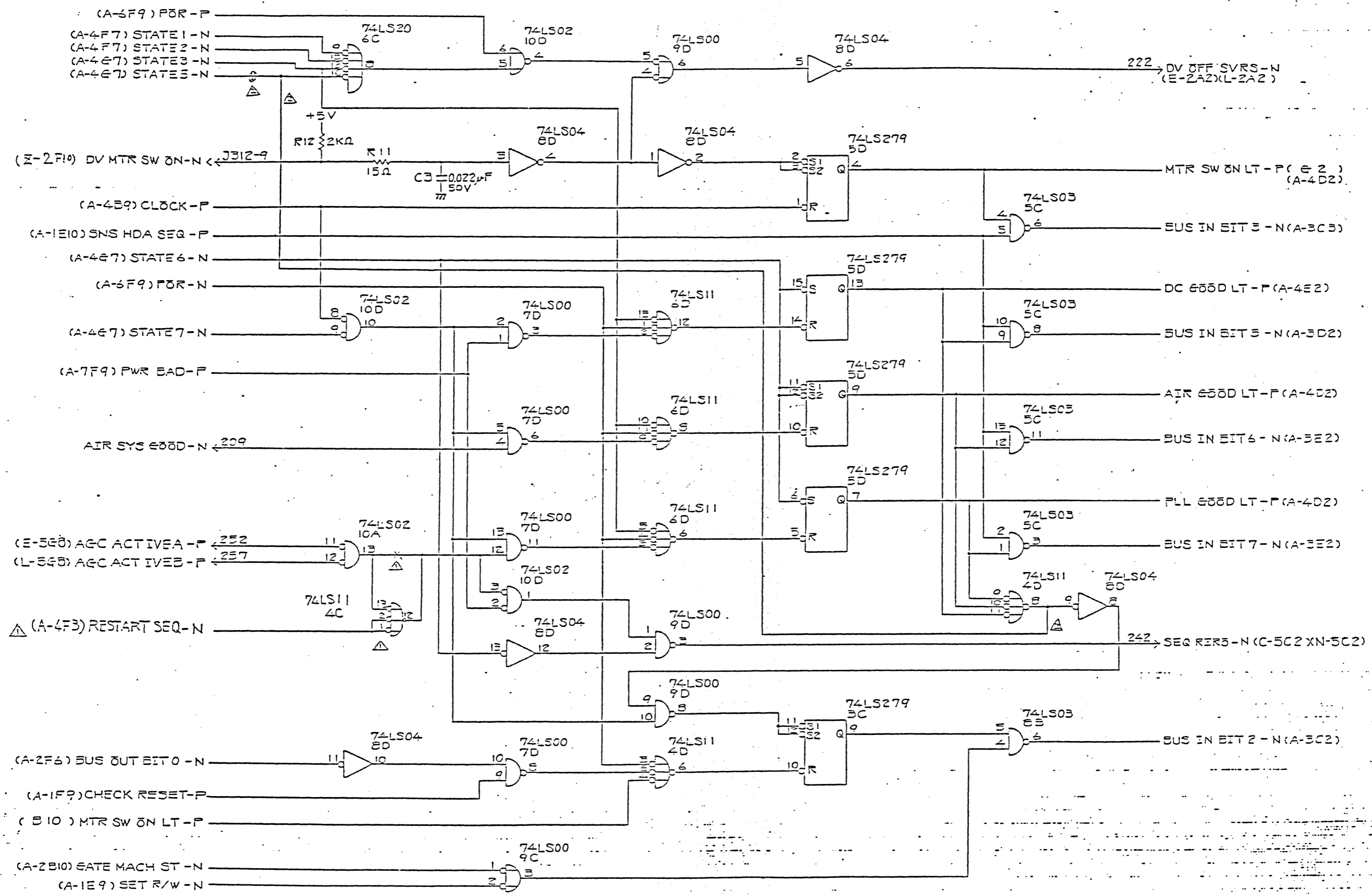
NP410 (INTERFACE)

A-4

P/N	TITLE	SHEET 4/	DRAWN I
REV	NP37 DRV LOGIC-DIA.	REV 1	CHECK I
	DRAWING NO	APPD I	
	NPL-NC-21410		Nippon Peripherals Limited

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ISSY DATE	DRAWN	APPD
CHANGE AGC ACTIVE		
1 18 21 17 17 17 17		
CHANGE DV OFF SV		
RS-N		
2 18 13 05 17 17		

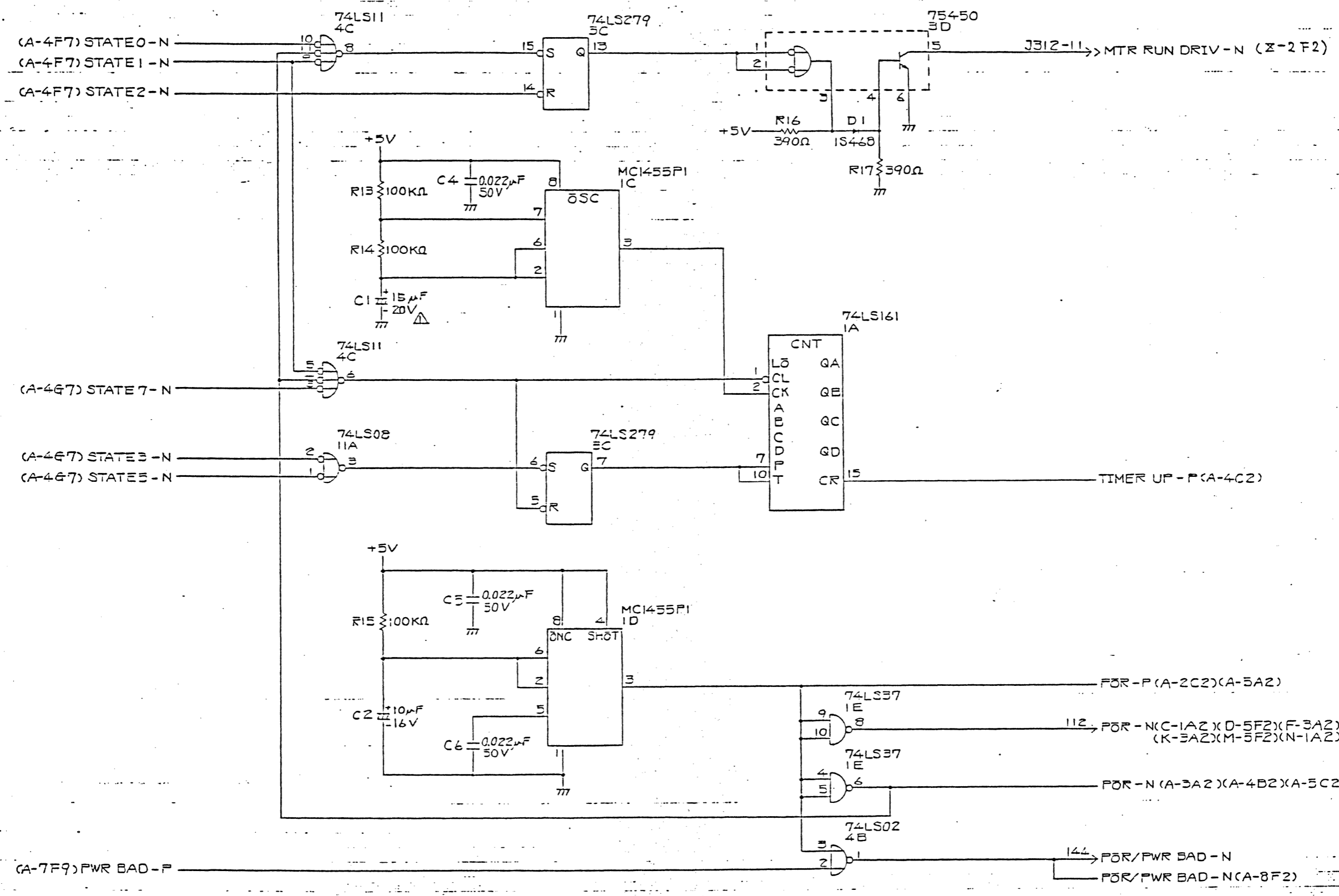


A-5

NP410 (INTERFACE)

P/N	TITLE	SHEET 5 /	DRAWN
REV	NP37 DRV LOGIC DIA.	REV Z	CHECK
	DRAWING NO	Nippon Peripherals Limited	
	NPL-NC-21410		

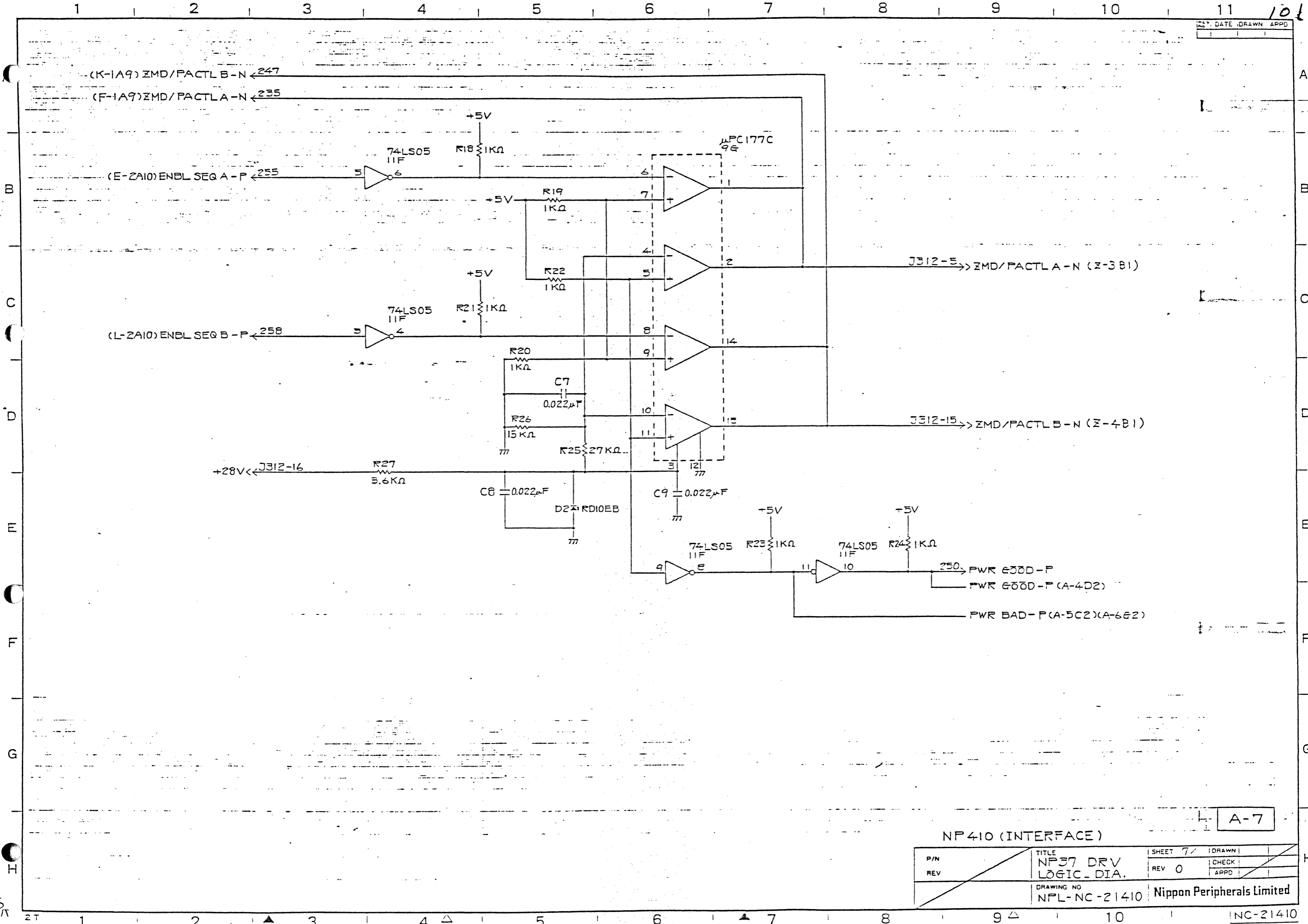
NO.	DATE	DRAWN	APPRO
CHANGE			
CT: 47μF	→	10μF	
10V	→	16V	
183.2018			



A-6

NP410 (INTERFACE)

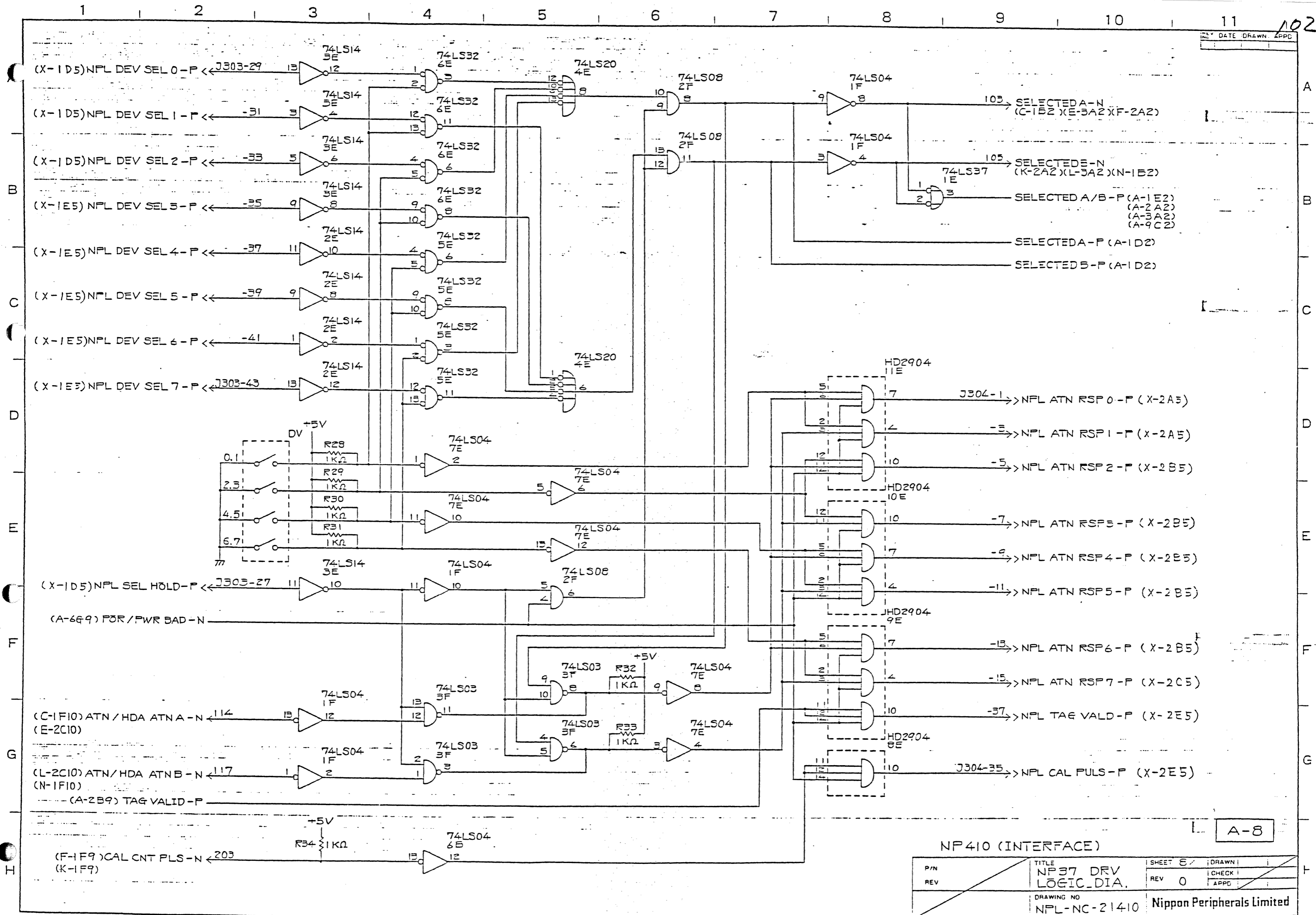
P/N	REV	TITLE	SHEET 6 /	DRAWN
		NP37 DRV LOGIC-DIA.	REV 1	CHECK
DRAWING NO		Nippon Peripherals Limited		APPRO
NPL-NC-21410				



A-7

NP 410 (INTERFACE)

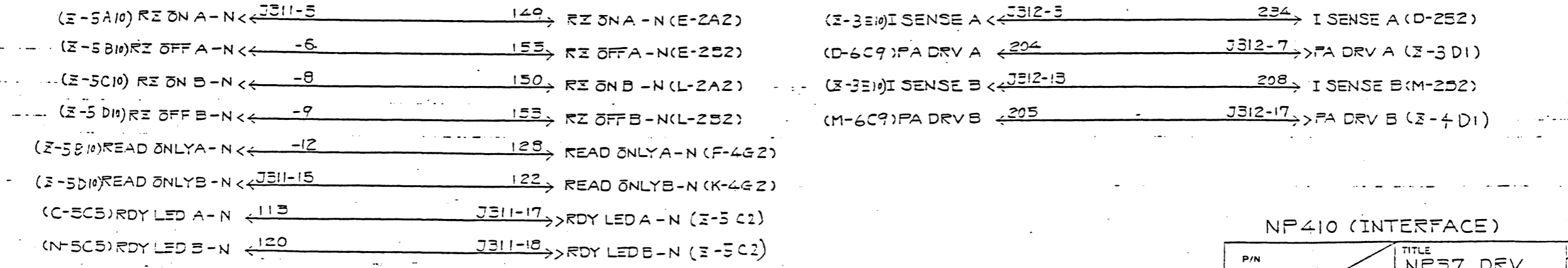
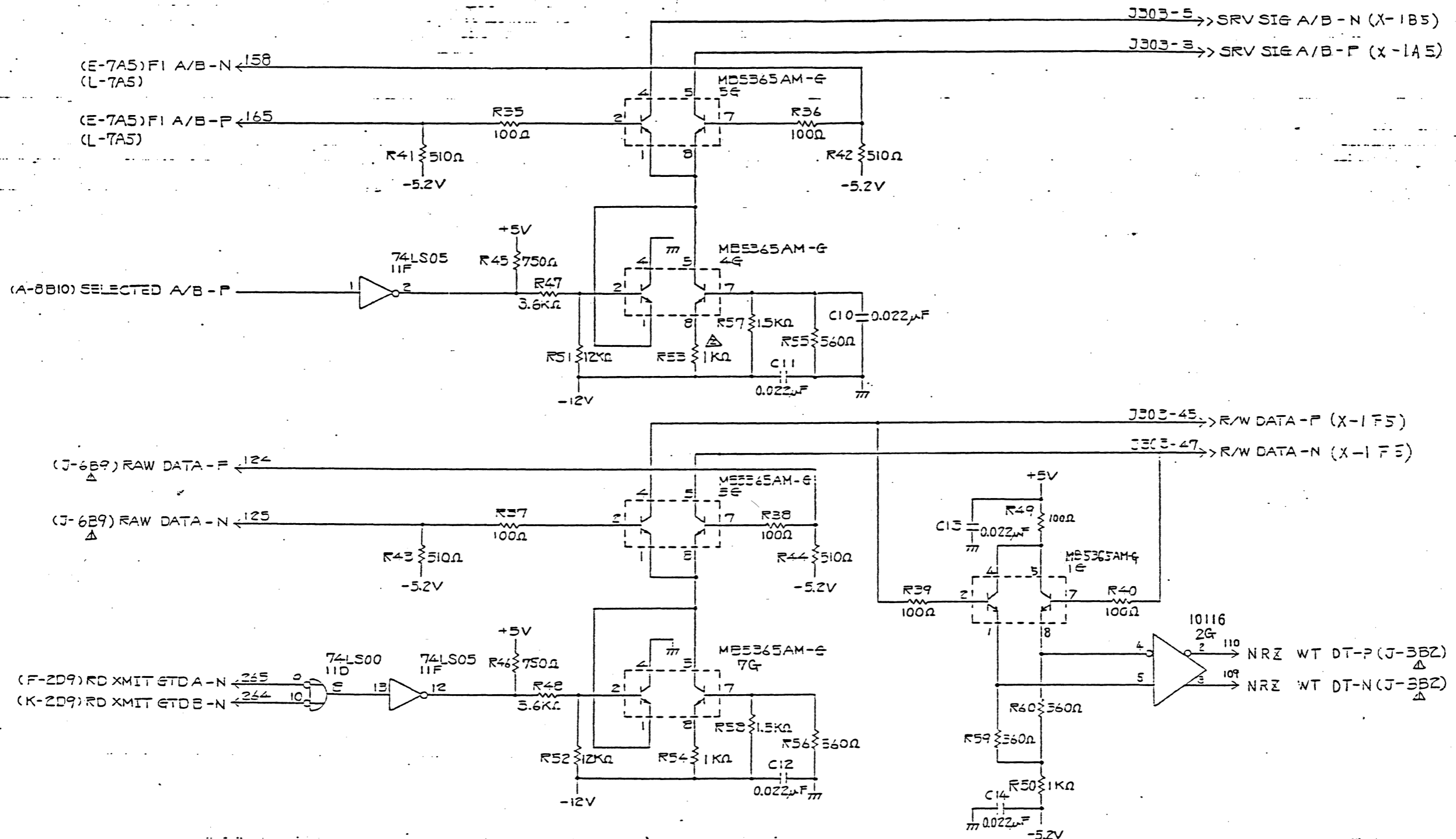
P/N	TITLE	SHEET 7	DRAWN
REV	NP37 DRV LOGIC-DIA.	REV 0	CHECK
DRAWING NO		APPD	
NPL-NC-21410		Nippon Peripherals Limited	



NP410 (INTERFACE)

A-8

P/N	TITLE	SHEET	DRAWN
REV	NP37 DRV LOGIC DIA.	0	CHECK
DRAWING NO		Nippon Peripherals Limited	
NPL-NC-21410			

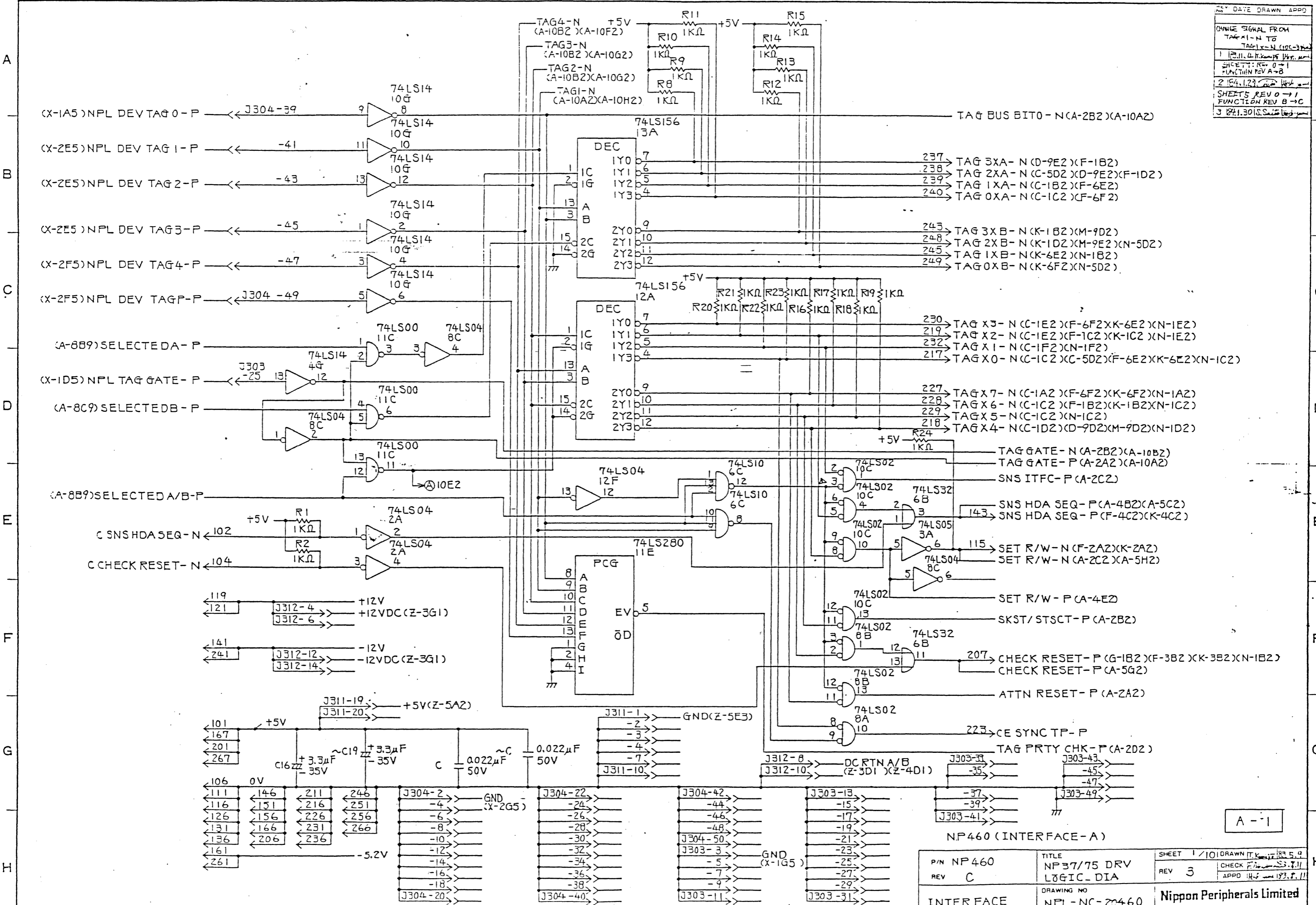


NP410 (INTERFACE)

P/N	TITLE	SHEET 9/9 (DRAWN)
REV	NP37 DRV LOGIC - DIA.	REV 2 (CHECK)
	DRAWING NO	APPD
	NPL-NC-21410	Nippon Peripherals Limited

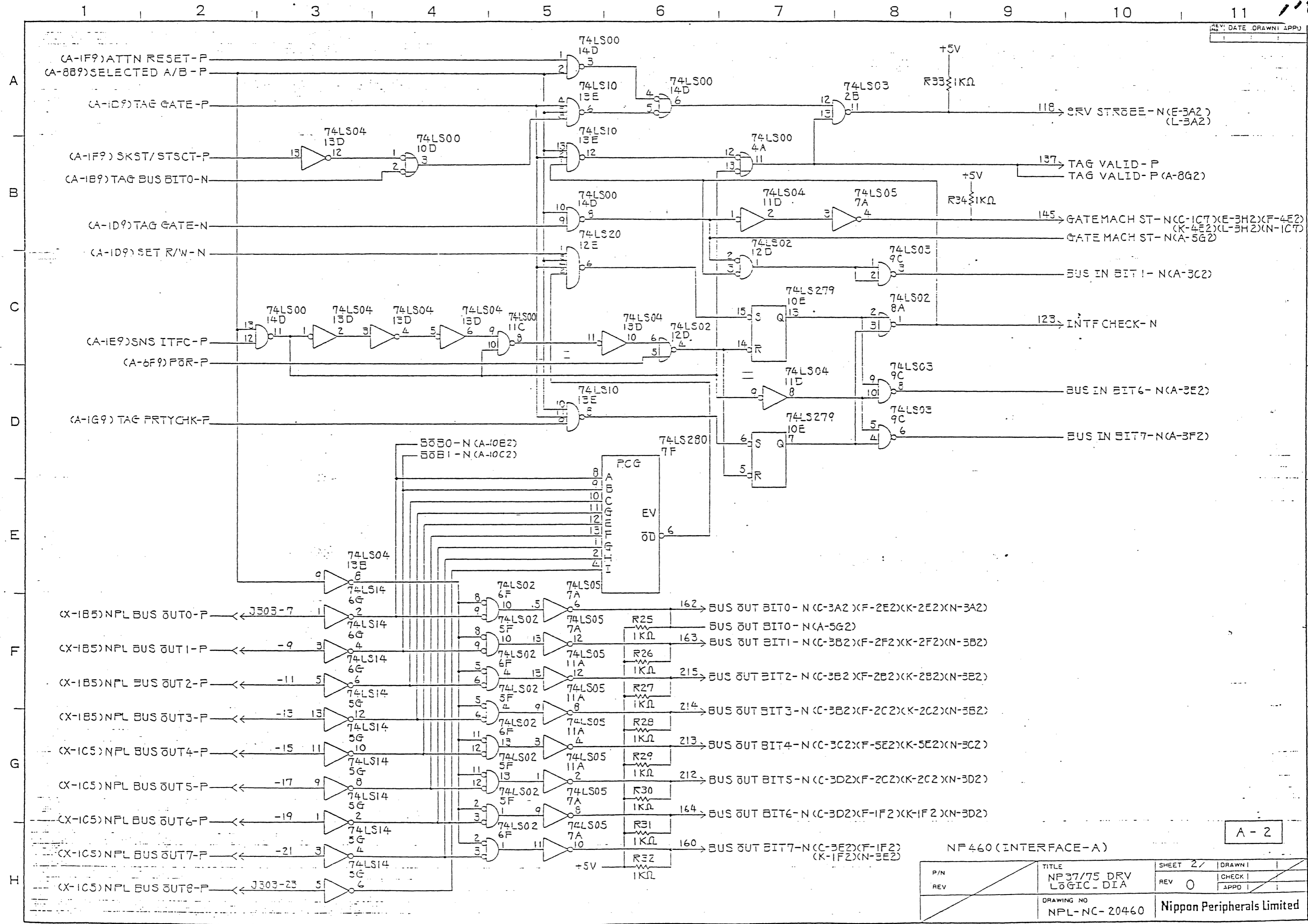
A-9

DATE DRAWN	APPRO
CHANGE SIGNAL FROM TAG X1-N TO TAG X-N (100-300)	
1 2 11.4.73 (100-300)	
SHEETS REV 0 -> 1	
FUNCTION REV A -> B	
2 15.4.73 (100-300)	
SHEETS REV 0 -> 1	
FUNCTION REV B -> C	
3 18.1.80 (100-300)	



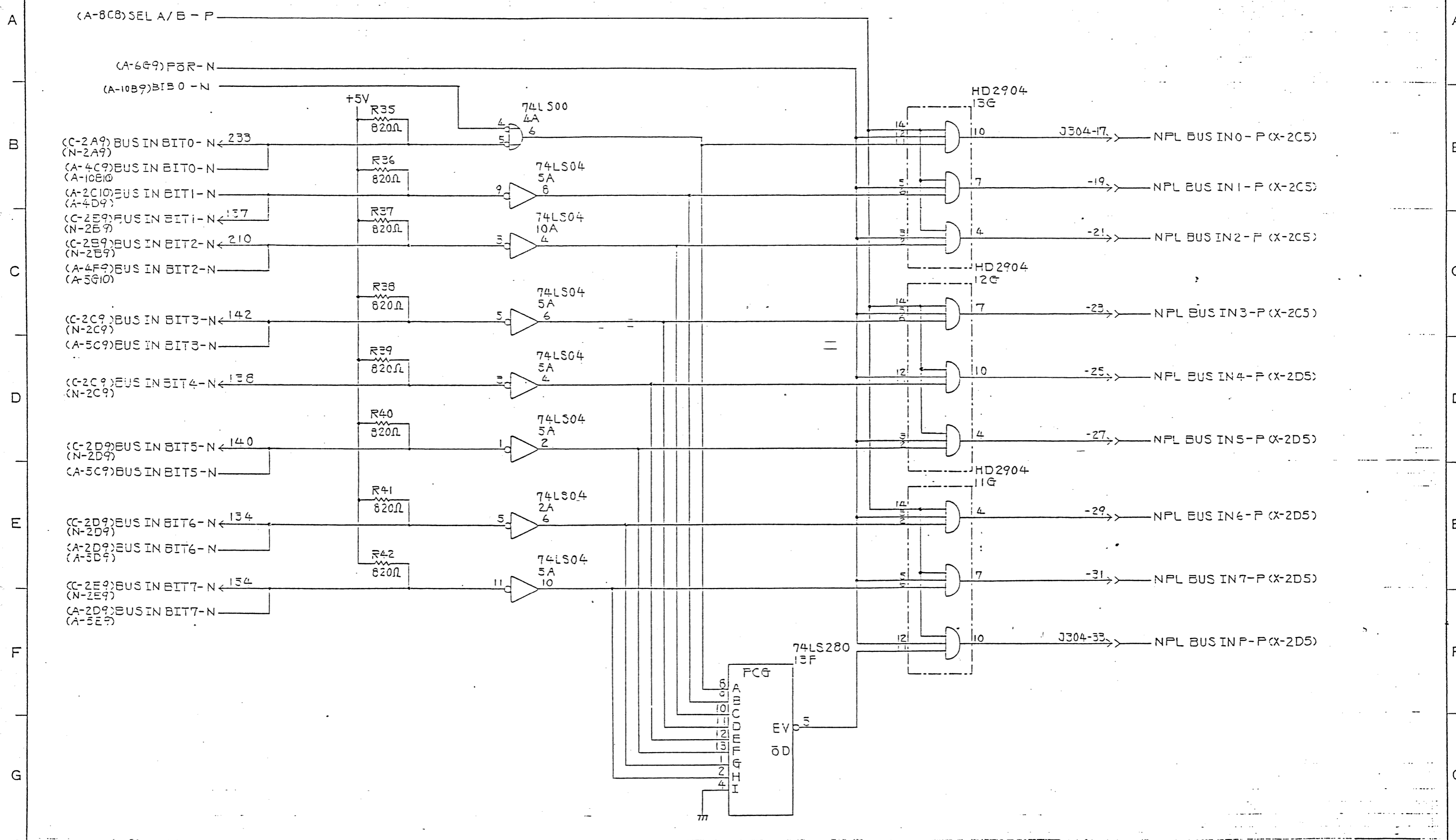
P/N NP 460	TITLE NP37/75 DRV LOGIC-DIA	SHEET 1/10	DRAWN BY 183.5.9
REV C	INTERFACE	REV 3	CHECK BY S3.7.11
DRAWING NO NPL-NC-20460		APPRO 18.1.80	
Nippon Peripherals Limited		INC-20460	

A - 1



NF 460 (INTERFACE-A)

P/N	REV	TITLE	SHEET 2 /	DRAWN
		NF 37/75 DRV LOGIC-DIA	REV 0	CHECK
DRAWING NO		Nippon Peripherals Limited		
NPL-NC-20460				

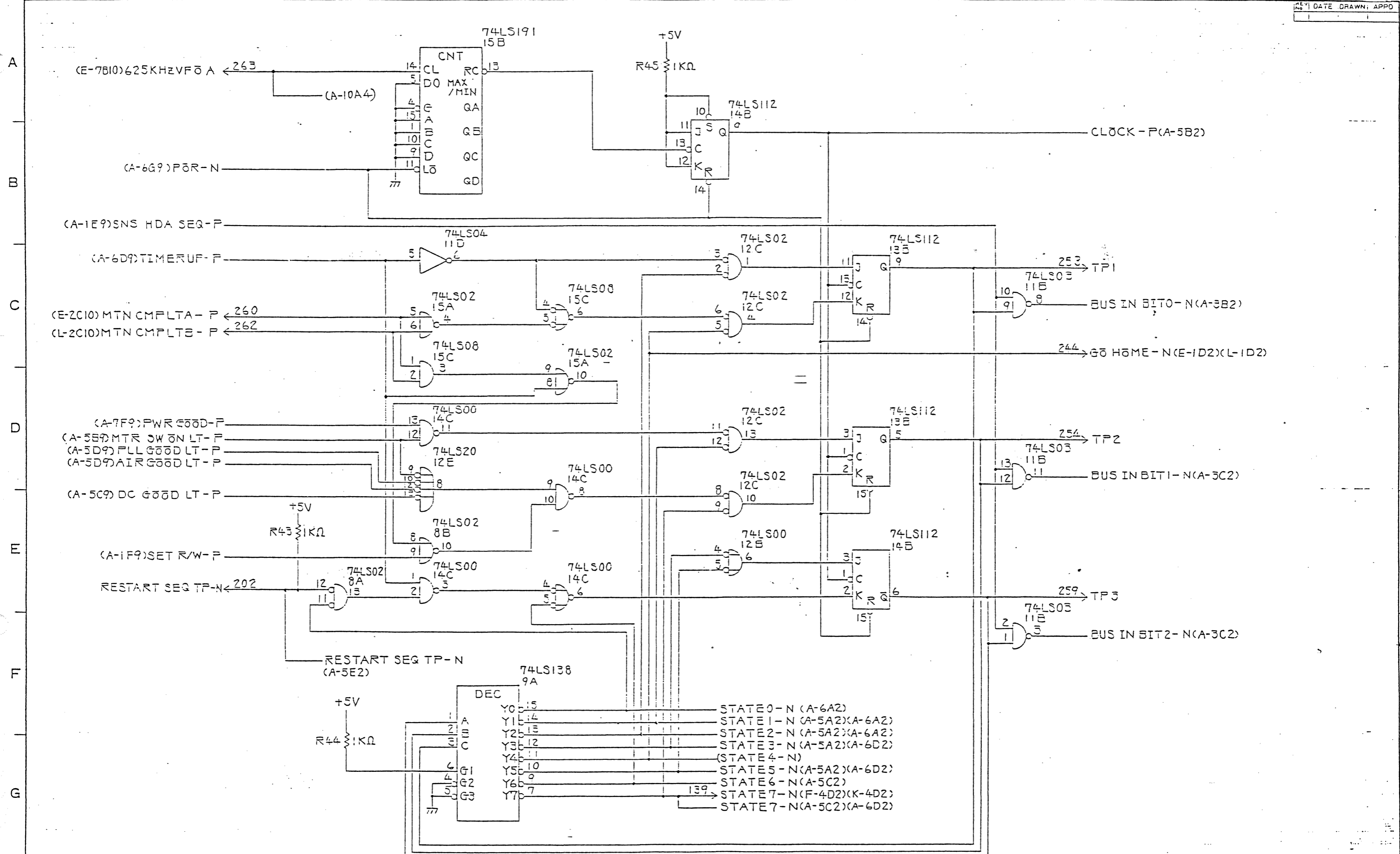


A-3

NF 460 (INTERFACE-A)

P/N	TITLE	SHEET 3 /	DRAWN
REV	NP37/75 DRV LOGIC DIA	REV 0	CHECK
DRAWING NO NPL-NC-20460		APPD	
Nippon Peripherals Limited			

H

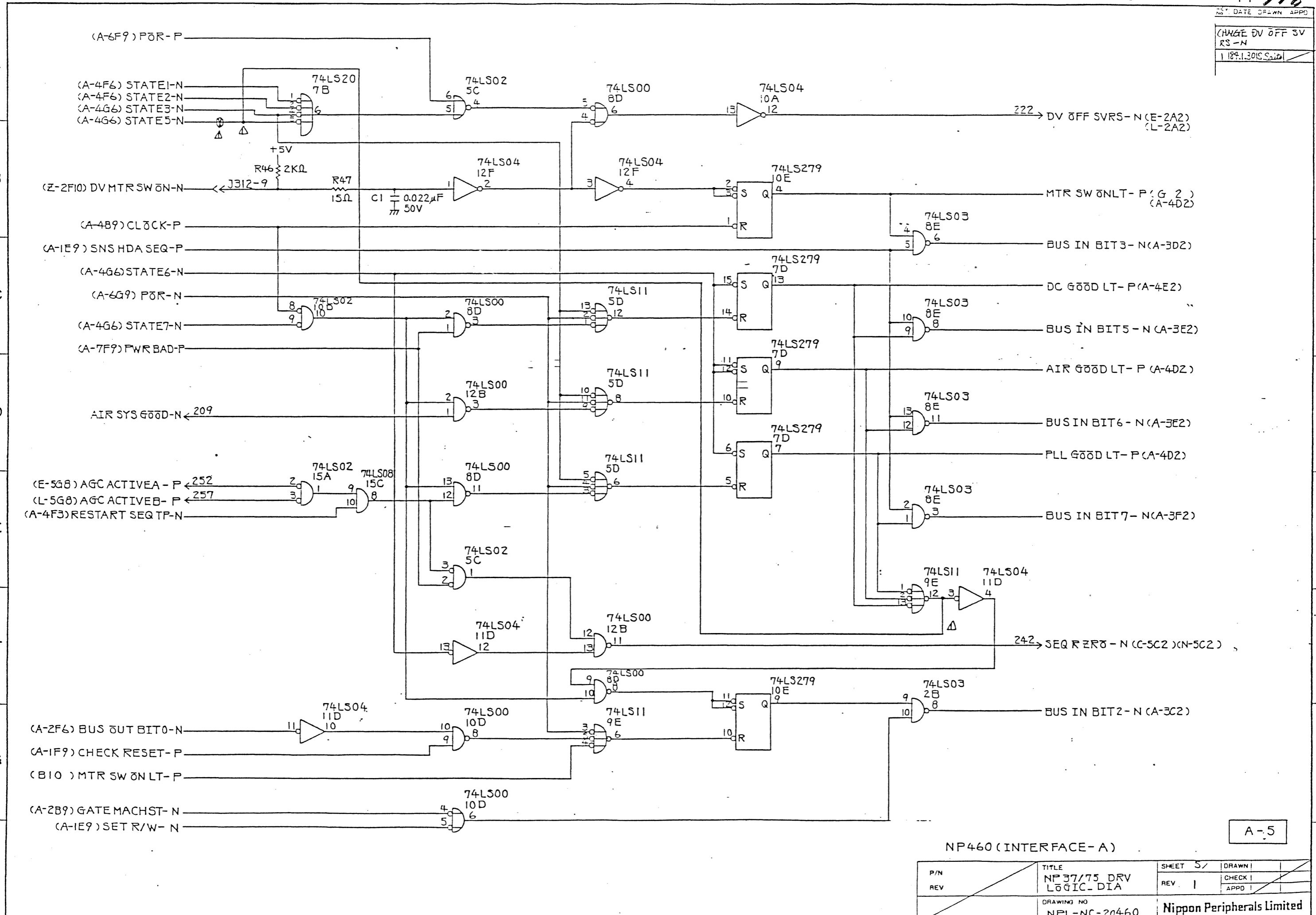


A-4

NF 460 (INTERFACE - A)

P/N	TITLE	SHEET 4/	DRAWN
REV	NP37/75 DRV LOGIC - DIA	REV 0	CHECK
DRAWING NO		Nippon Peripherals Limited	
NPL-NC-20460			

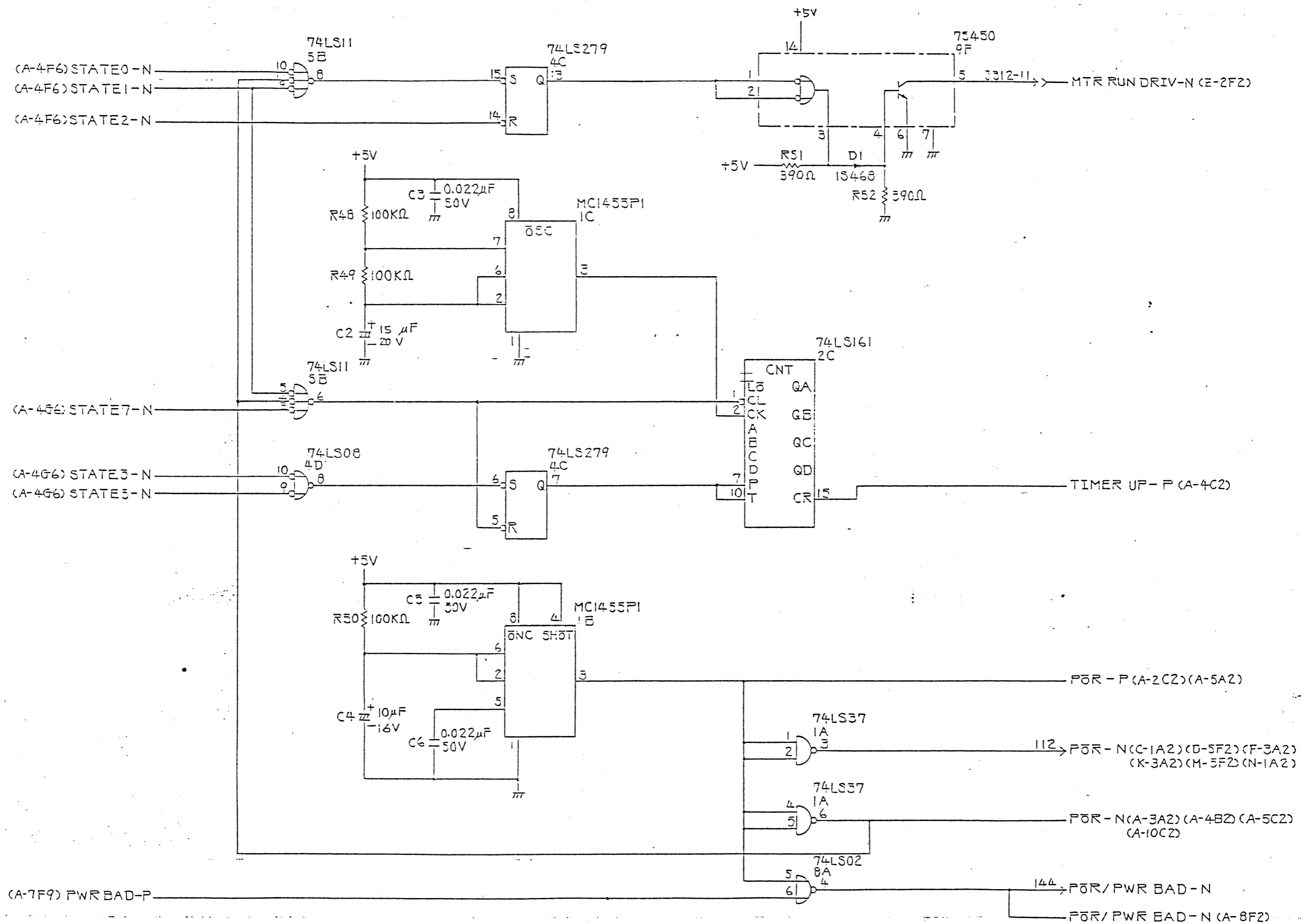
DATE OF DRAWN APPD
 CHANGE DV OFF SV
 RS-N
 1 189.1.3015 Saito



NP460 (INTERFACE-A)

P/N	TITLE	SHEET 5/	DRAWN
REV	NP 37/75 DRV LOGIC-DIA	REV 1	CHECK
	DRAWING NO		APPD
	NPL-NC-20460	Nippon Peripherals Limited	

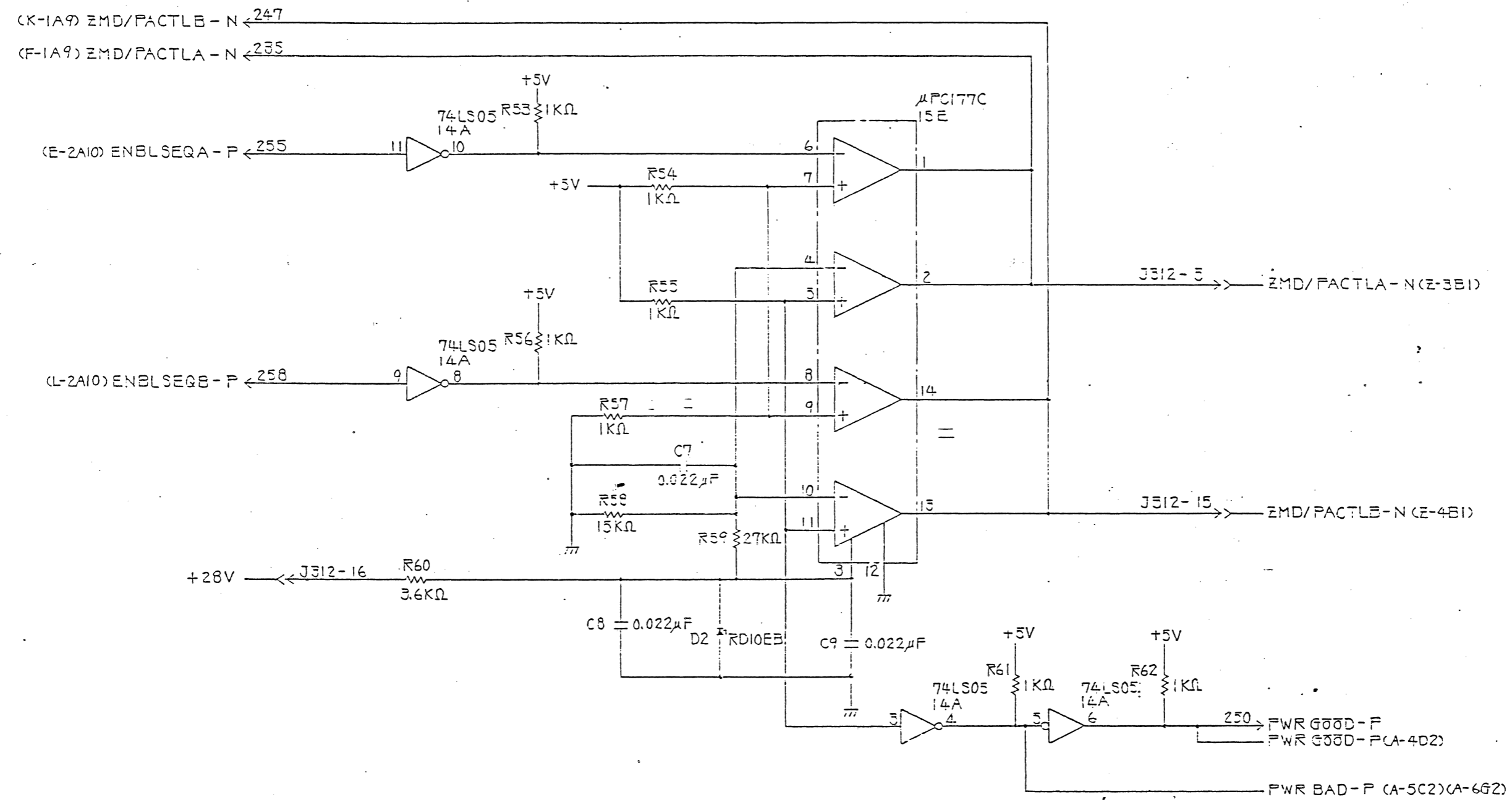
A-5



A-6

NP460 (INTERFACE-A)

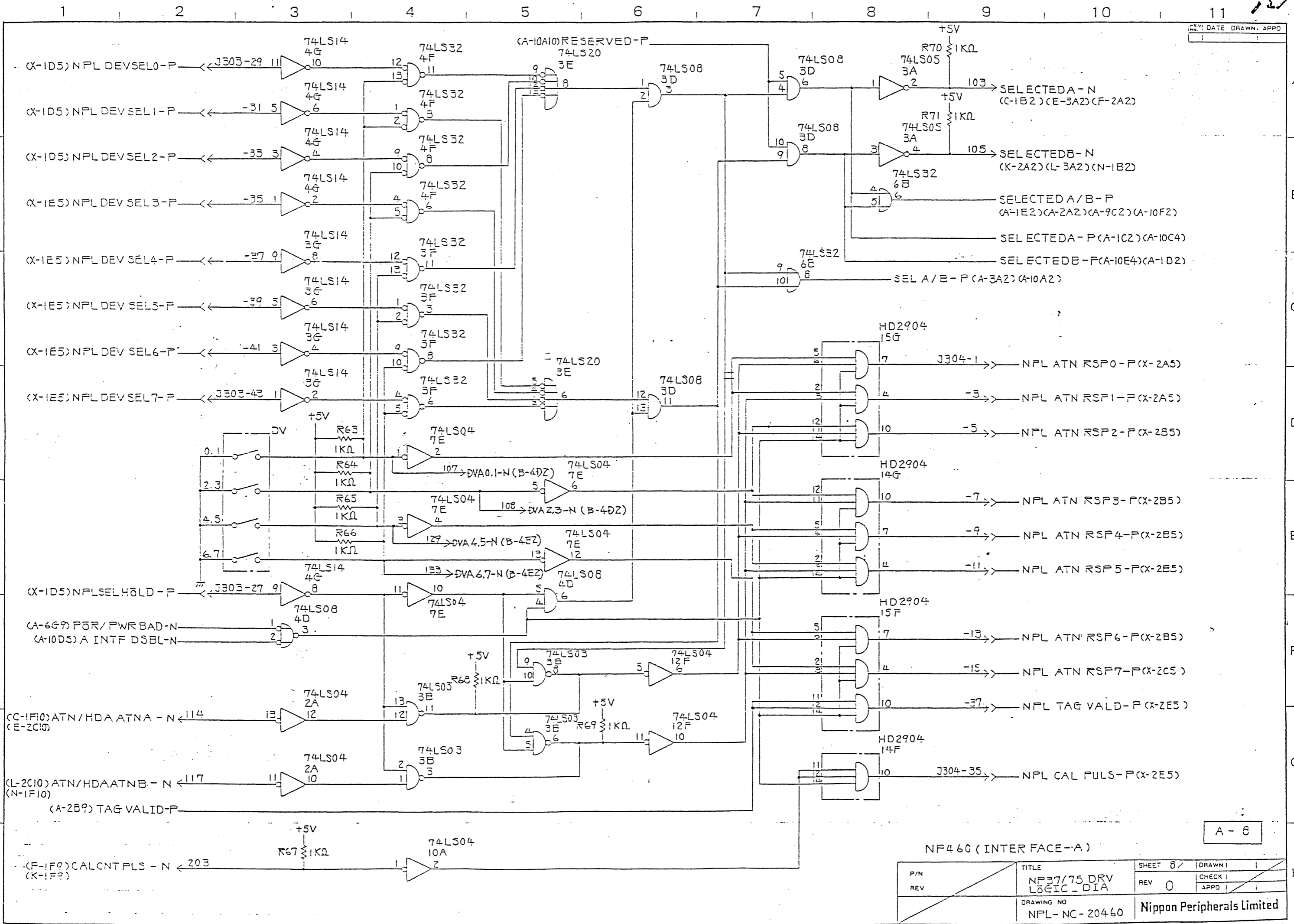
P/N	TITLE	SHEET 6/	DRAWN
REV	NP 37/75 DRV LOGIC-DIA	REV 0	CHECK
DRAWING NO		Nippon Peripherals Limited	
NPL-NC-20460		APPD	



A-7

NP460 (INTERFACE-A)

P/N REV	TITLE NP37/75 DRV LOGIC DIA	SHEET 7 /	DRAWN
		REV 0	CHECK
DRAWING NO NPL-NC-20460		Nippon Peripherals Limited	



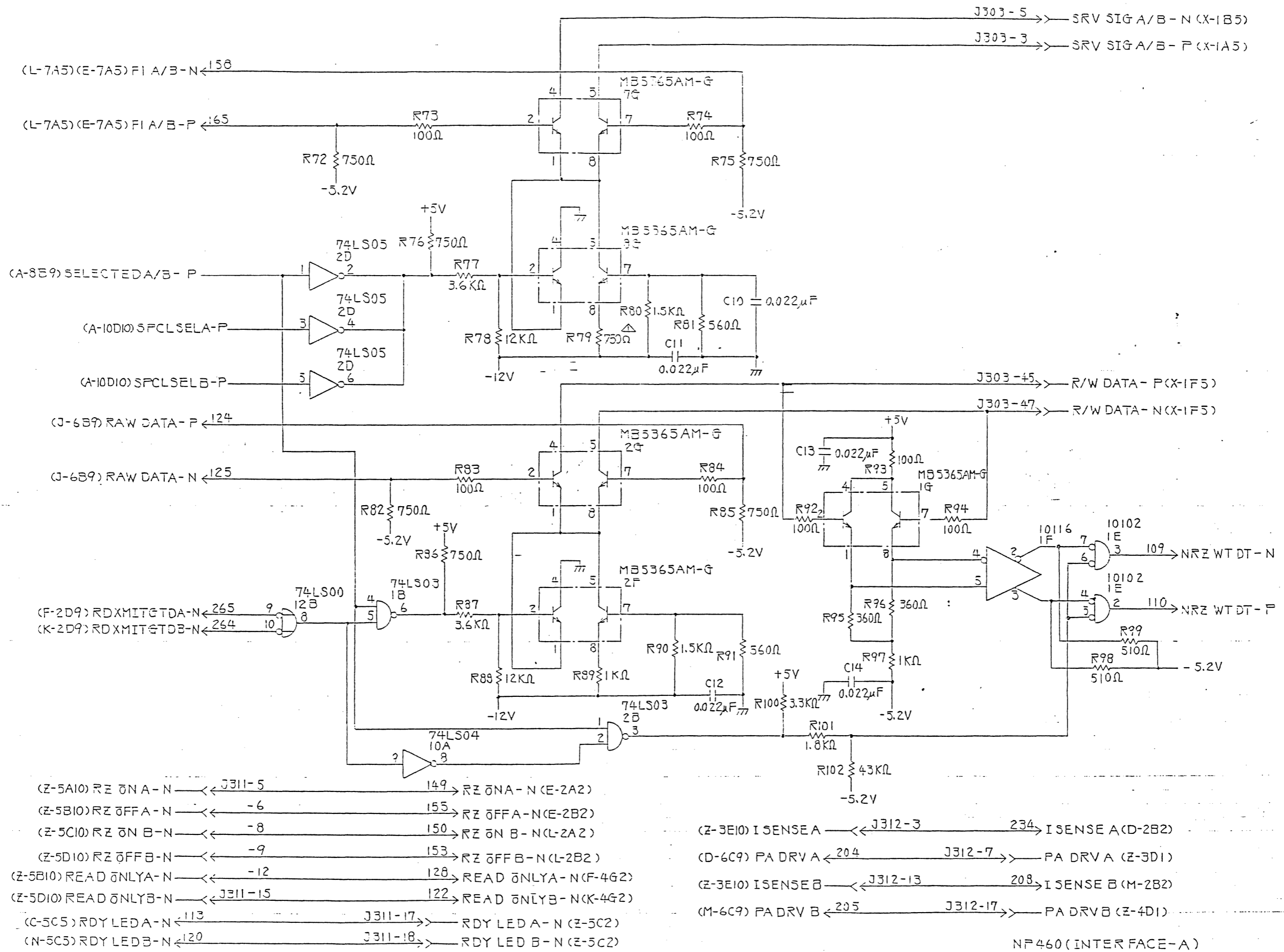
REV	DATE	DRAWN	APPD

A-8

NF460 (INTERFACE-A)

P/N	TITLE	SHEET 8	DRAWN
REV	NP37/75 DRV LOGIC-DIA	REV 0	CHECK I
DRAWING NO		APPD	
NPL-NC-20460		Nippon Peripherals Limited	

DATE DRAWN	APPD
CHANGES	REV
1 KR → 750R	
1 15/11/75	



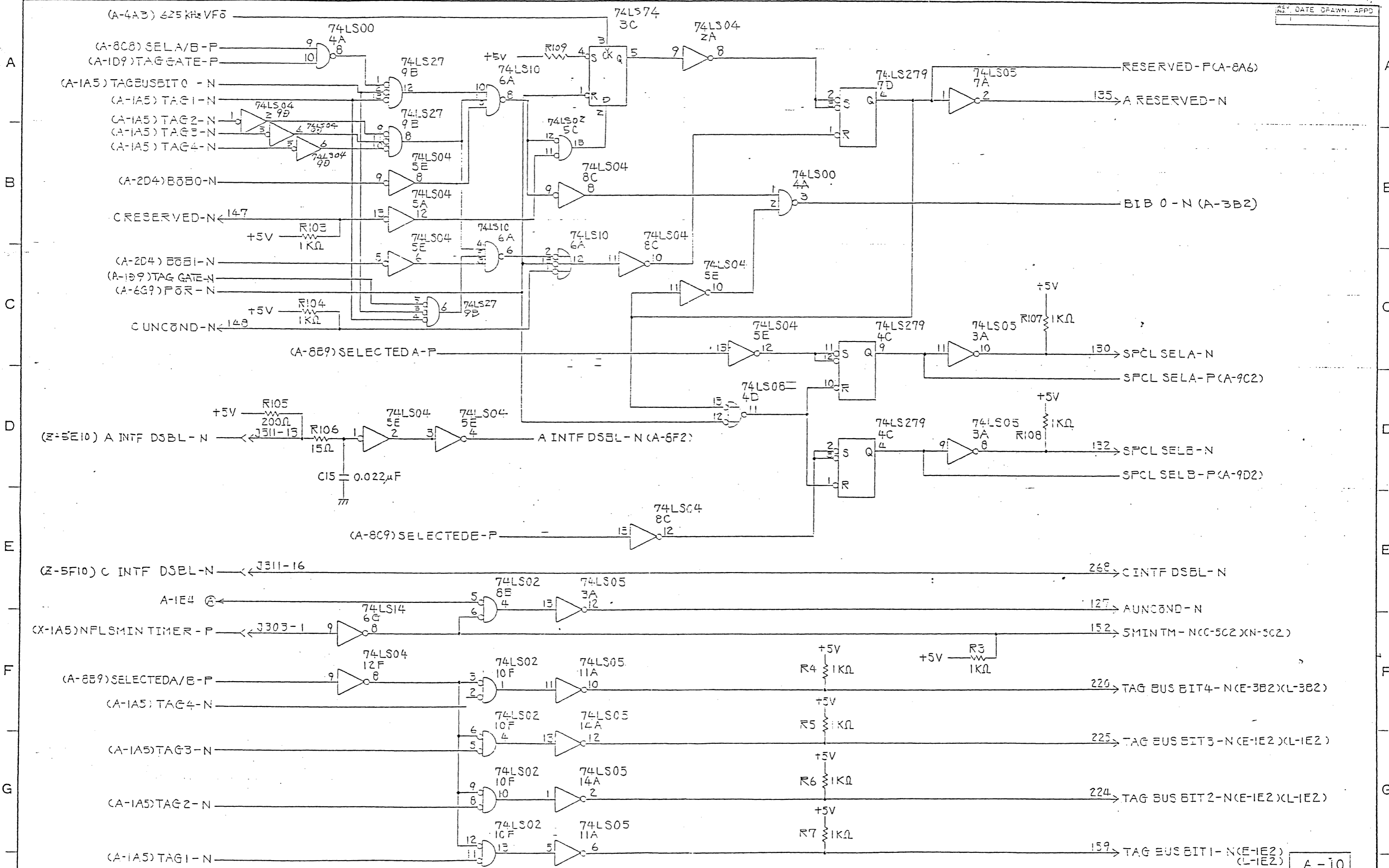
- (Z-5A10) RZ ON A - N ← J311-5 → 149 → RZ ON A - N (E-2A2)
- (Z-5B10) RZ OFF A - N ← -6 → 155 → RZ OFF A - N (E-2B2)
- (Z-5C10) RZ ON B - N ← -8 → 150 → RZ ON B - N (L-2A2)
- (Z-5D10) RZ OFF B - N ← -9 → 153 → RZ OFF B - N (L-2B2)
- (Z-5B10) READ ONLY A - N ← -12 → 128 → READ ONLY A - N (F-4G2)
- (Z-5D10) READ ONLY B - N ← J311-15 → 122 → READ ONLY B - N (K-4G2)
- (C-5C5) RDY LED A - N ← 113 → J311-17 → RDY LED A - N (Z-5C2)
- (N-5C5) RDY LED B - N ← 120 → J311-18 → RDY LED B - N (Z-5C2)

- (Z-3E10) I SENSE A ← J312-3 → 234 → I SENSE A (D-2B2)
- (D-6C9) PA DRV A ← 204 → J312-7 → PA DRV A (Z-3D1)
- (Z-3E10) I SENSE B ← J312-13 → 208 → I SENSE B (M-2B2)
- (M-6C9) PA DRV B ← 205 → J312-17 → PA DRV B (Z-4D1)

NP460 (INTERFACE-A)

A - 9

P/N	REV	TITLE	SHEET	DRAWN
		NP37/75 DRV LOGIC-DIA.	9/	
		DRAWING NO	CHECK	
		NFL-NC-20460	APPD	
			Nippon Peripherals Limited	

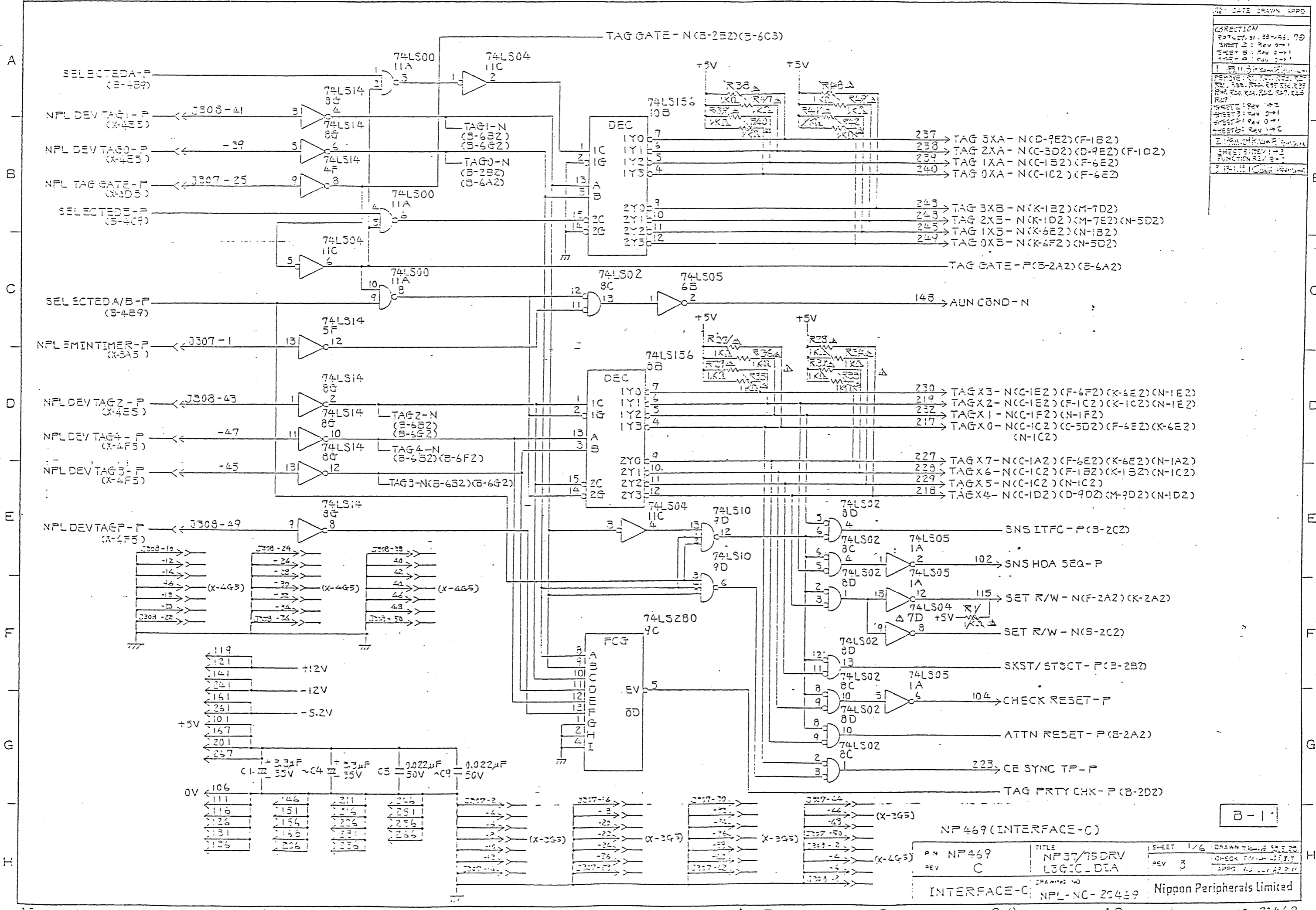


NP460 (INTERFACE-A)

A-10

P/N	REV	TITLE	SHEET 10/10	DRAWN
		NP37/75 DRV LOGIC DIA	REV C	CHECK
DRAWING NO		Nippon Peripherals Limited		
NPL-NC-20460				

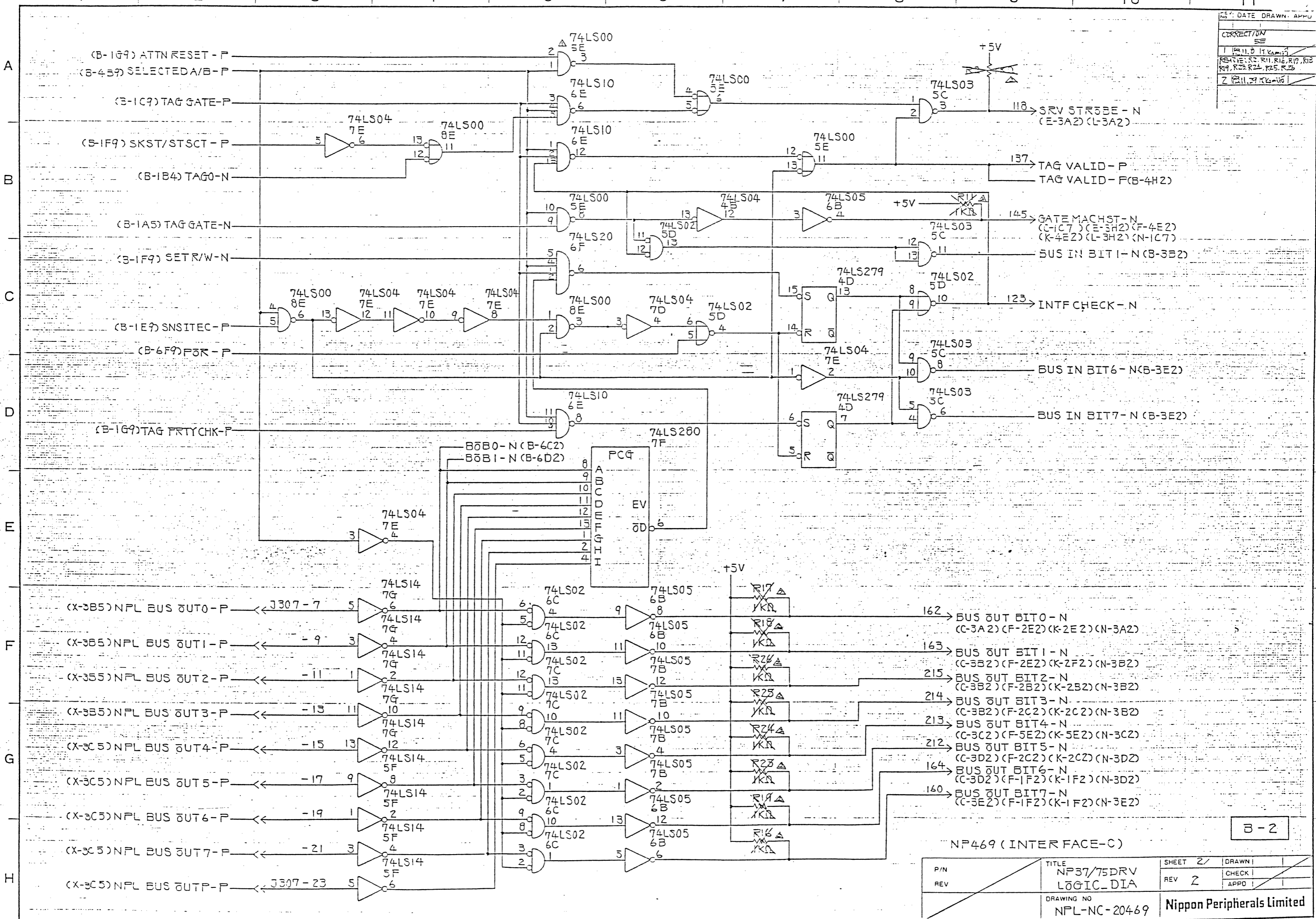
DATE DRAWN	APPD
CORRECTION	
REV 01: 21.03.79	
SHEET 2: Rev 01	
SHEET 3: Rev 01	
SHEET 4: Rev 01	
SHEET 5: Rev 01	
SHEET 6: Rev 01	
SHEET 7: Rev 01	
SHEET 8: Rev 01	
SHEET 9: Rev 01	
SHEET 10: Rev 01	
SHEET 11: Rev 01	
SHEET 12: Rev 01	
SHEET 13: Rev 01	
SHEET 14: Rev 01	
SHEET 15: Rev 01	
SHEET 16: Rev 01	
SHEET 17: Rev 01	
SHEET 18: Rev 01	
SHEET 19: Rev 01	
SHEET 20: Rev 01	



NP 469 (INTERFACE-C)	
P/N NP 469	TITLE NP 37/75 DRV LOGIC DIA
REV C	SHEET 1/6 DRAWN BY: S.S. 20469
INTERFACE-C	APPD: S.S. 20469
Nippon Peripherals Limited	

8-1

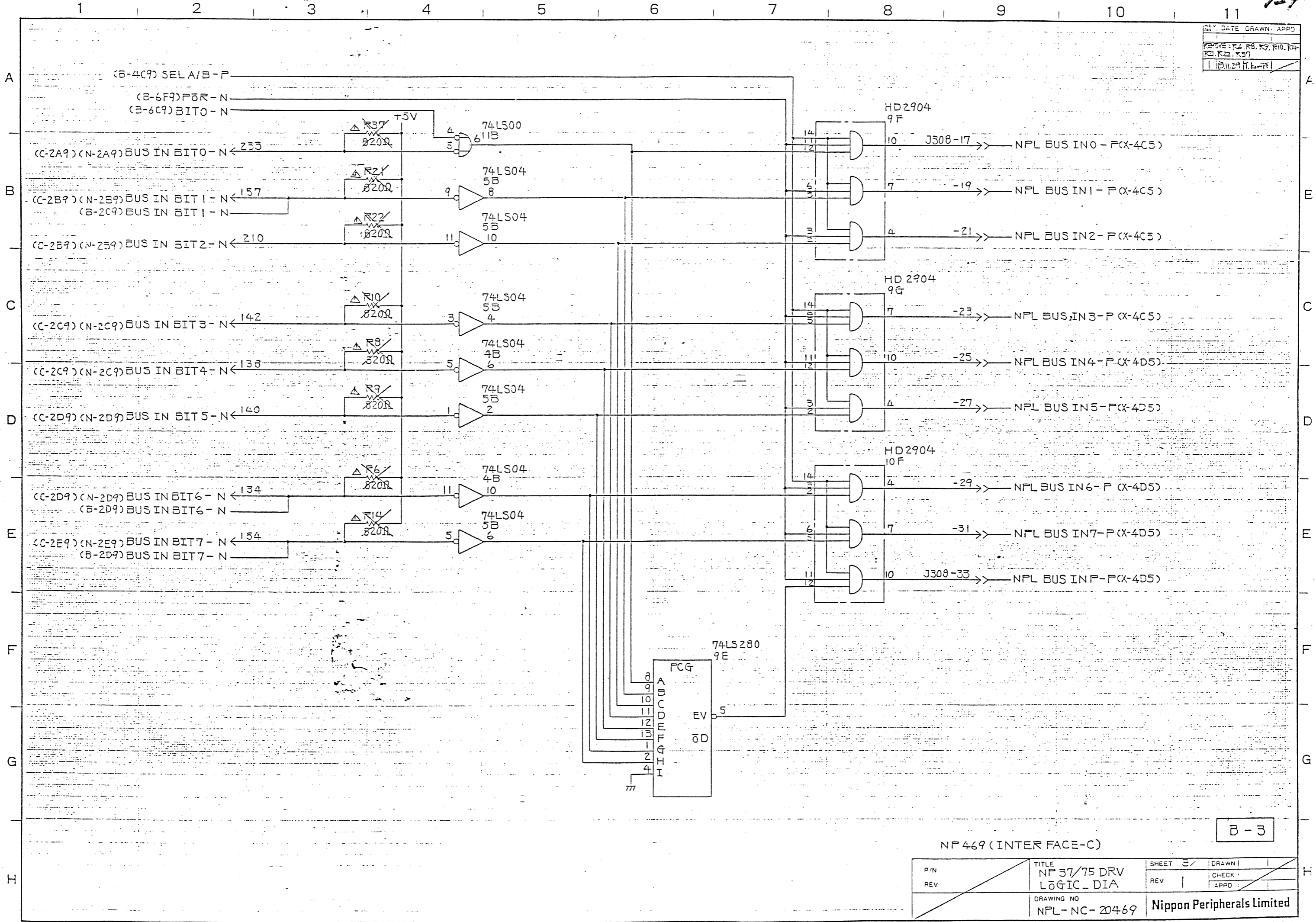
DATE	DRAWN	APPRO
CORRECTION		
1. 19.11.81 H. Kamada		
RS41E, R21, R16, R10, R18, R19, R23, R24, R25, R26		
2. 22.11.81 K. Kamada		



B-2

NP469 (INTERFACE-C)

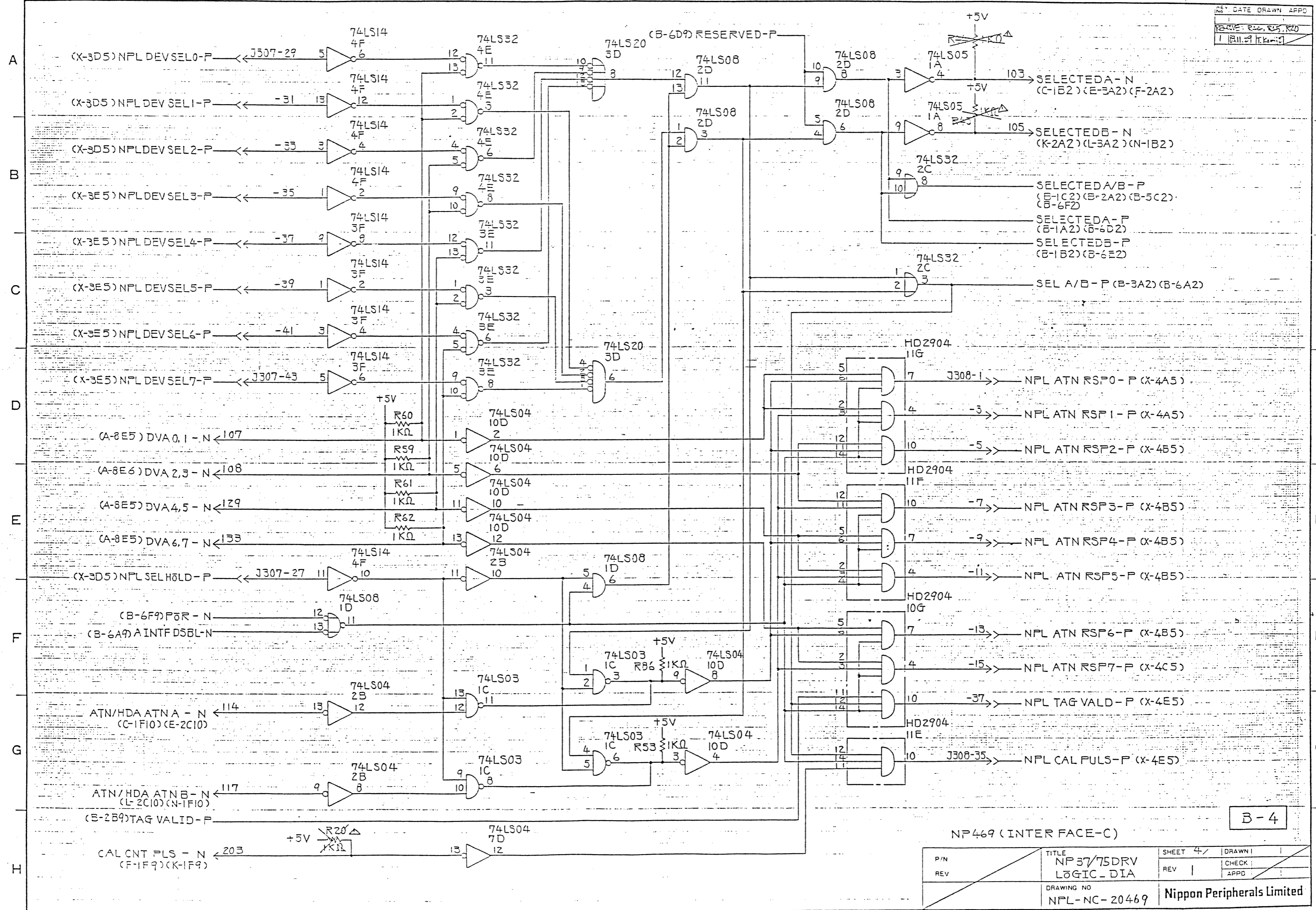
P/N	TITLE	SHEET 2/	DRAWN I
REV	NP37/75DRV LOGIC DIA	REV 2	CHECK I
DRAWING NO NPL-NC-20469		APPRO I	
Nippon Peripherals Limited			



B-3

NP 469 (INTER FACE-C)

P/N REV	TITLE NP 37/75 DRV LOGIC DIA	SHEET 5 / DRAWN
	DRAWING NO NPL-NC-20469	REV CHECK APPD
Nippon Peripherals Limited		

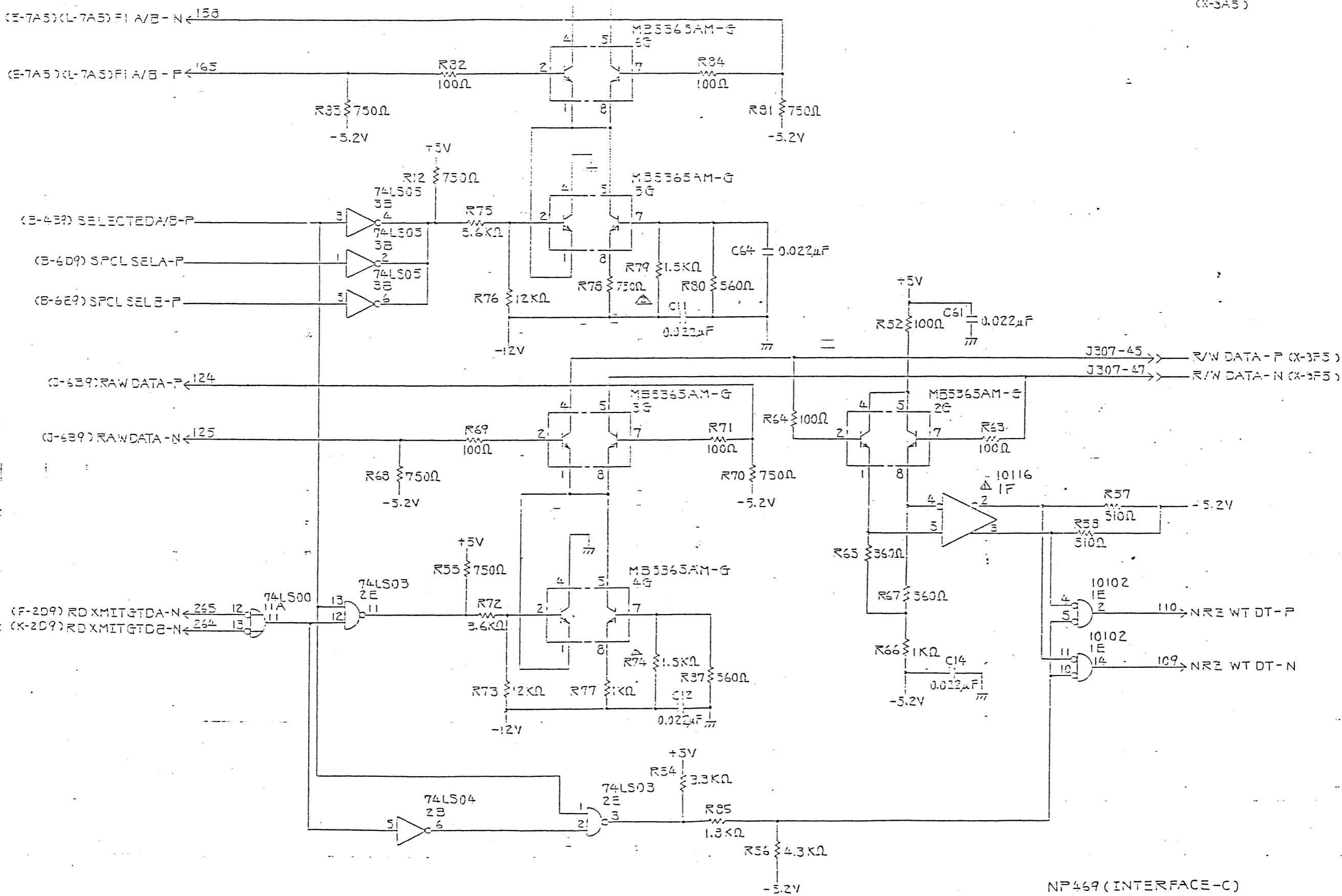


B-4

NP 469 (INTERFACE-C)

P/N	REV	TITLE	SHEET	DRAWN
		NP 37/75DRV LOGIC-DIA	4/	
		DRAWING NO	CHECK	APPD
		NPL-NC-20469		
Nippon Peripherals Limited				

NO.	DATE	DRAWN	APPRO
CORRECTION			
REV. 1F			
1. 15.10.75			
CHANGE R73			
1K → 250Ω			
2. 15.10.75			

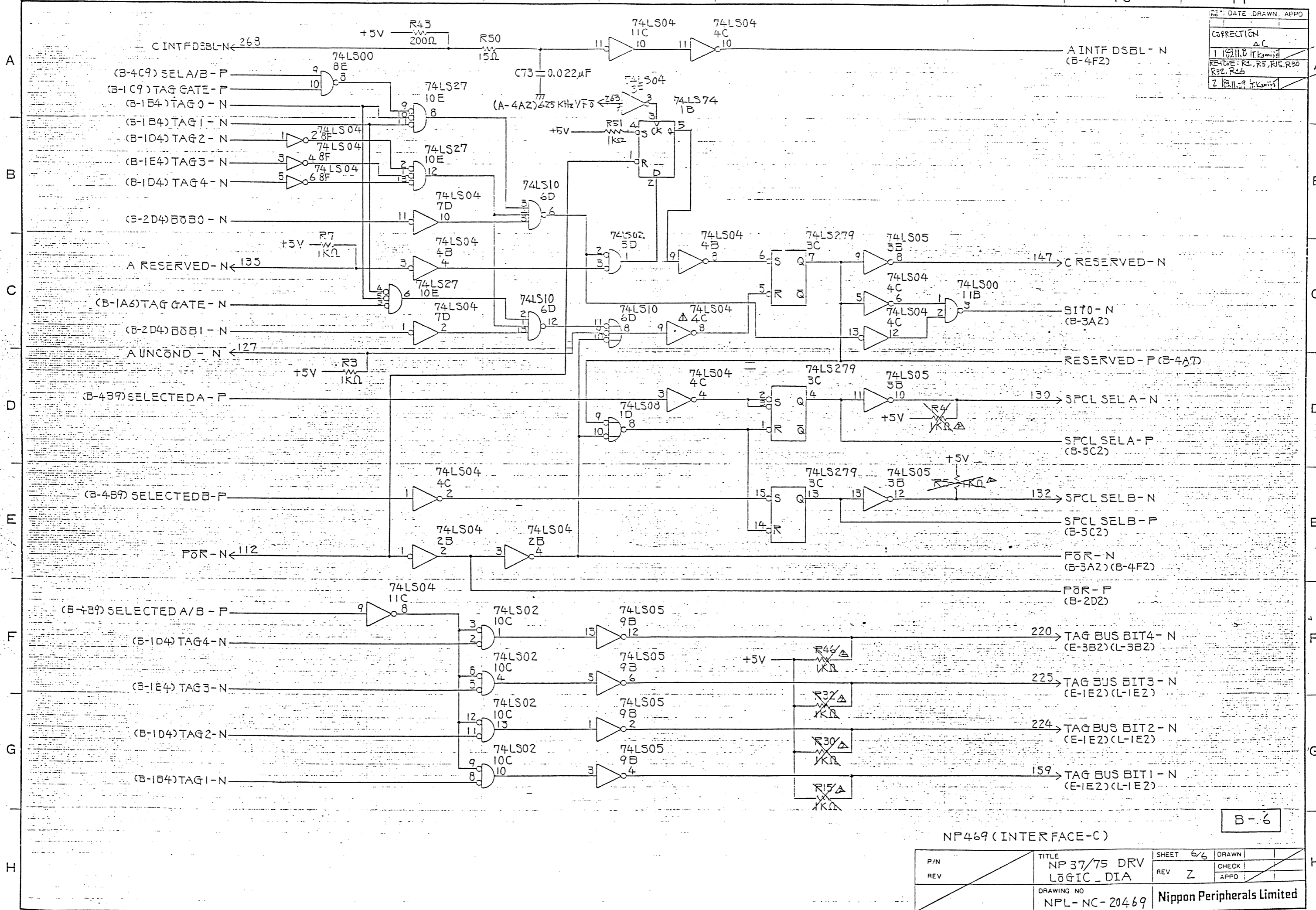


NP469 (INTERFACE-C)

5-5

PIN	TITLE	SHEET 5 / DRAWN
REV	NP37/75DRV LOGIC-DIA	REV 2 CHECK 1
DRAWING NO		APPRO
NPL-NC-20469		Nippon Peripherals Limited

NO.	DATE	DRAWN	APPO
CORRECTION			
1 1981.06 11 Kojima			
RELATIVE: R4, R5, R15, R20			
R22, R26			
Z Call. 29 Kojima			



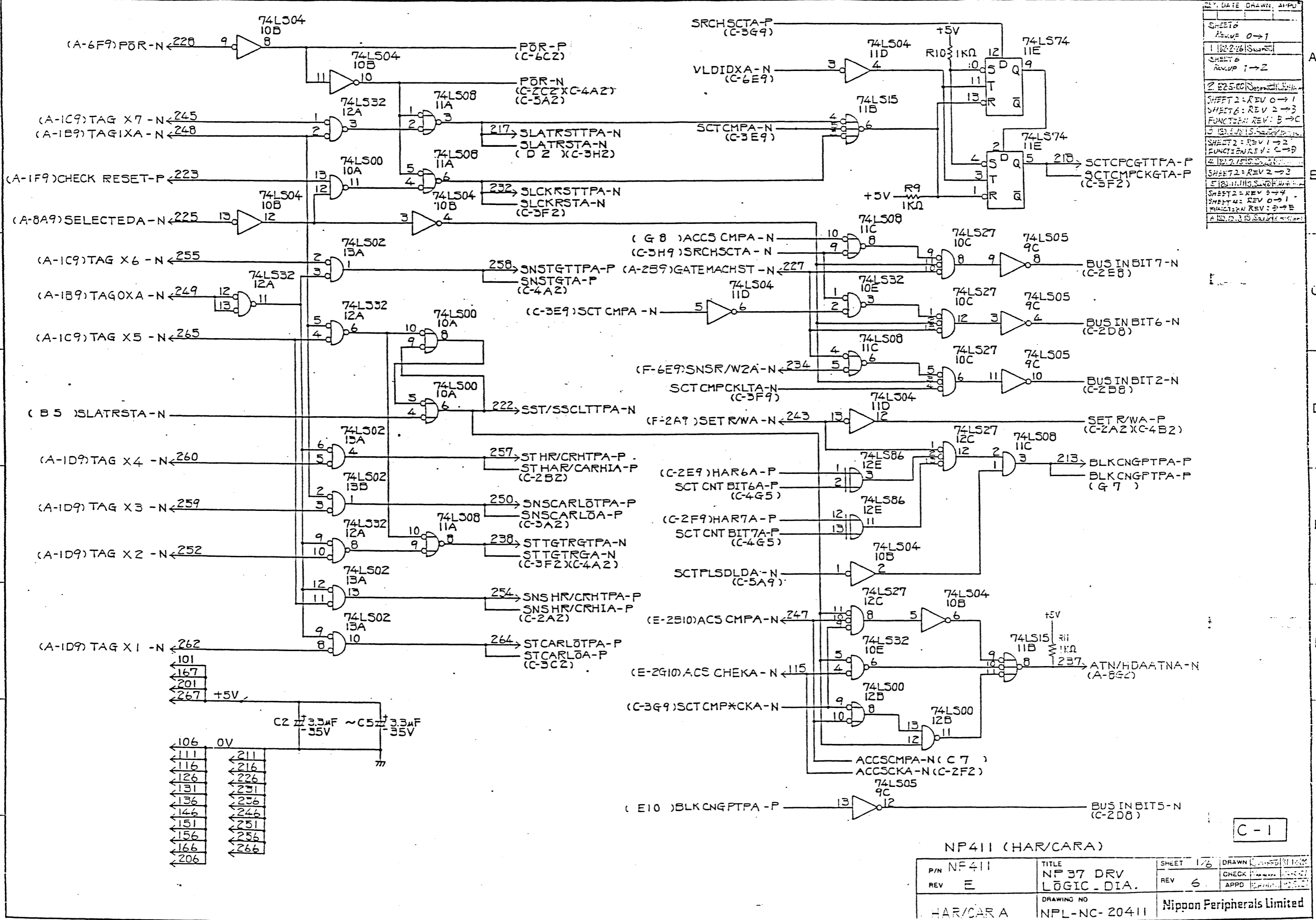
B-6

NP469 (INTERFACE-C)

P/N	TITLE	SHEET	6/6	DRAWN	
REV	NP 37/75 DRV LOGIC_DIA	REV	Z	CHECK	
DRAWING NO		Nippon Peripherals Limited			
NPL-NC-20469					

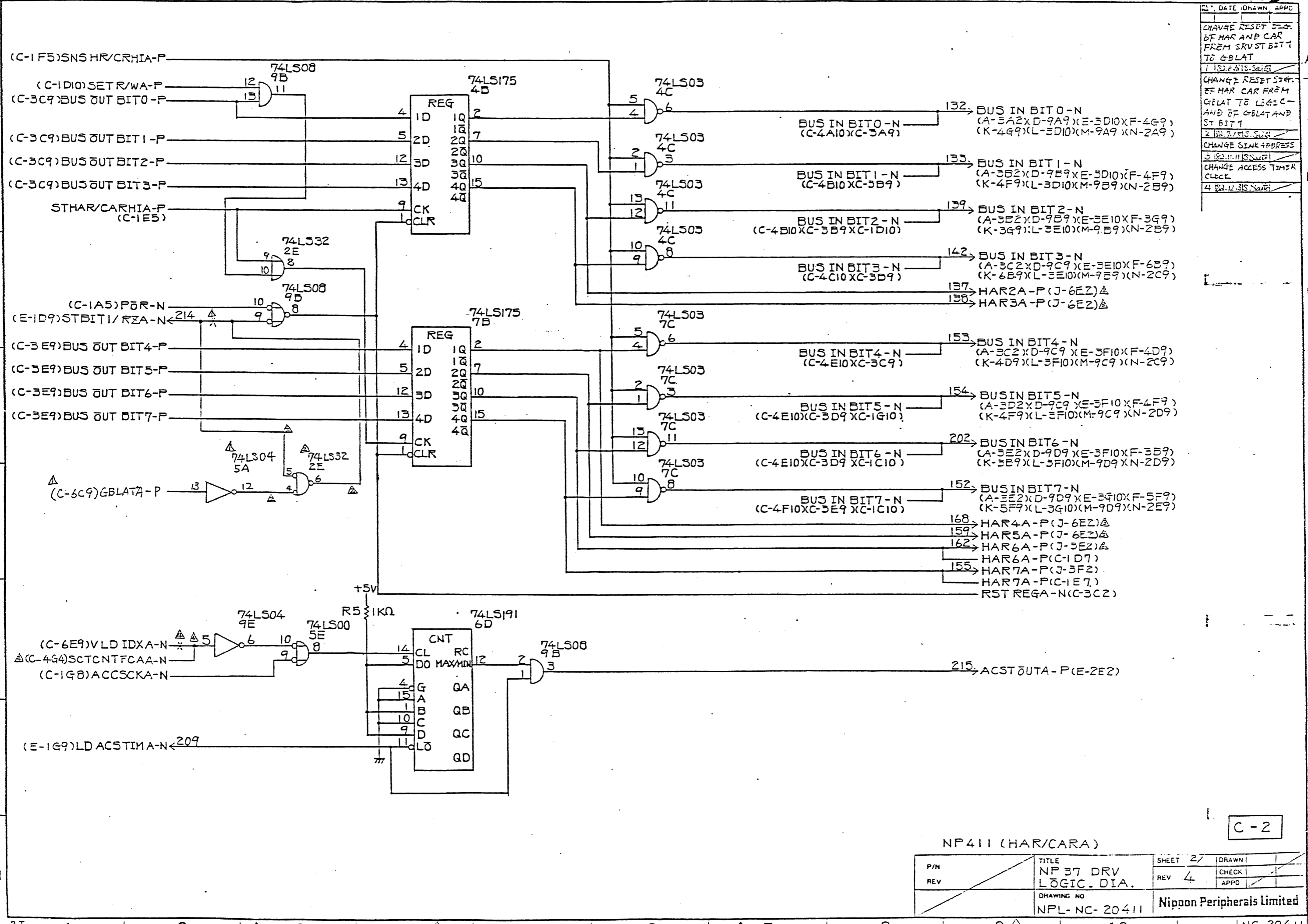
NC-20469

REV.	DATE	DRAWN	APPD.
SHEET 6			
Rev. 0 → 1			
SHEET 6			
Rev. 1 → 2			
2. 22.5.80			
SHEET 2: REV. 0 → 1			
SHEET 6: REV. 2 → 3			
FUNCTION: REV. B → C			
3. 18.2.85			
SHEET 2: REV. 1 → 2			
FUNCTION: REV. C → D			
4. 12.2.85			
SHEET 2: REV. 2 → 3			
5. 11.11.85			
SHEET 4: REV. 0 → 1			
FUNCTION: REV. D → E			
6. REV. 3.15.86			



NP411 (HAR/CARA)			
P/N	NF411	TITLE	NP 37 DRV LOGIC-DIA.
REV	E	SHEET	1/6
DRAWING NO		REV	6
HAR/CARA		APPD	
NPL-NC-20411		DRAWN	
Nippon Peripherals Limited		DATE	

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REV	DATE	DRAWN	APPC
1	12.2.85	Saito	
2	12.7.85	Saito	
3	12.11.85	Saito	
4	12.12.85	Saito	

CHANGE RESET STG. OF HAR AND CAR FROM SRVST BIT 1 TO GBLAT

CHANGE RESET STG. OF HAR CAR FROM GBLAT TO LOGIC AND OF GBLAT AND ST BIT 1

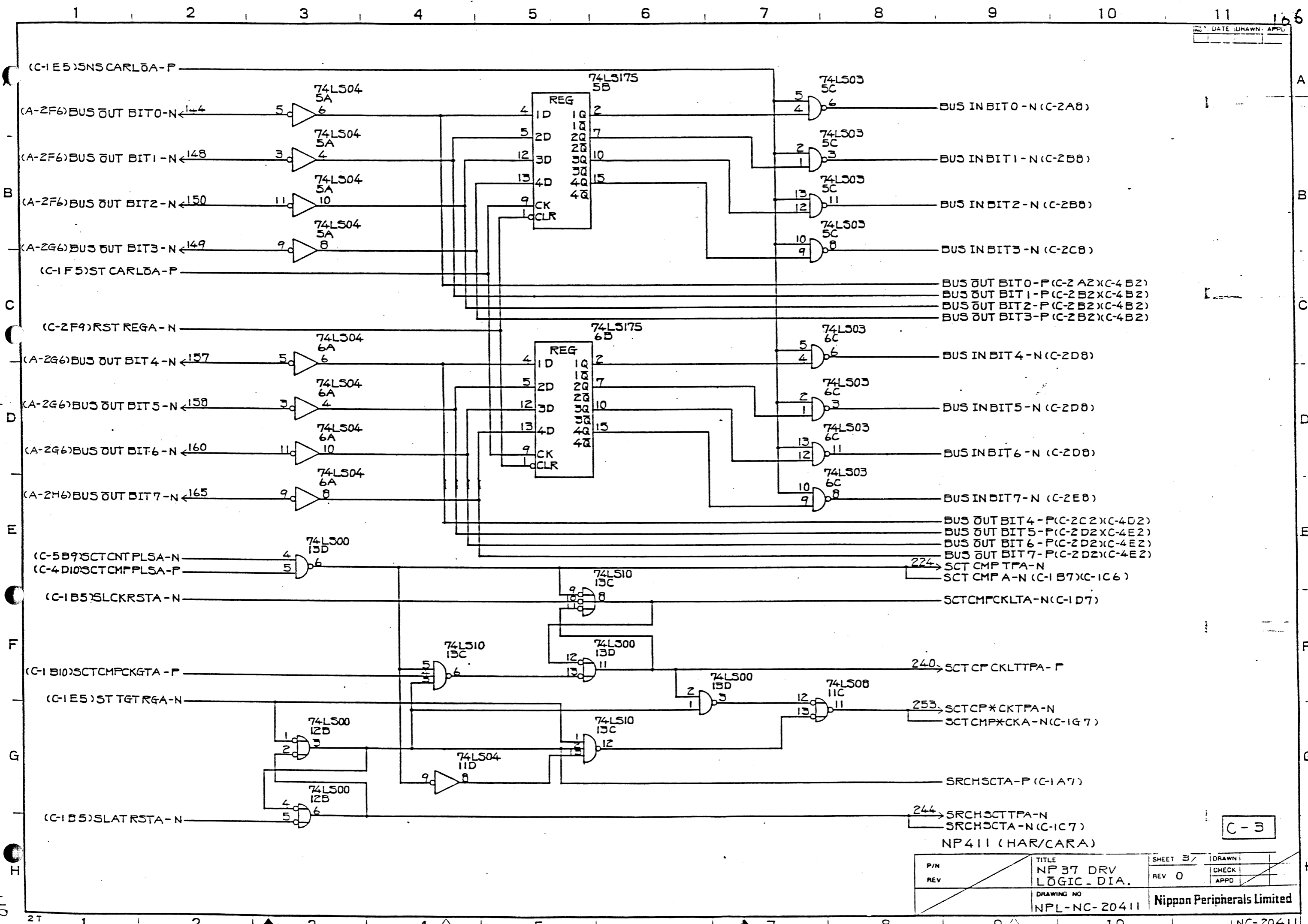
CHANGE SINK ADDRESS

CHANGE ACCESS TIMER CLOCK

C-2

NP411 (HAR/CARA)

P/N	TITLE	SHEET 2	DRAWN
REV	NP 37 DRV LOGIC DIA.	REV 4	CHECK
	DRAWING NO		APPC
	NPL-NC-20411	Nippon Peripherals Limited	

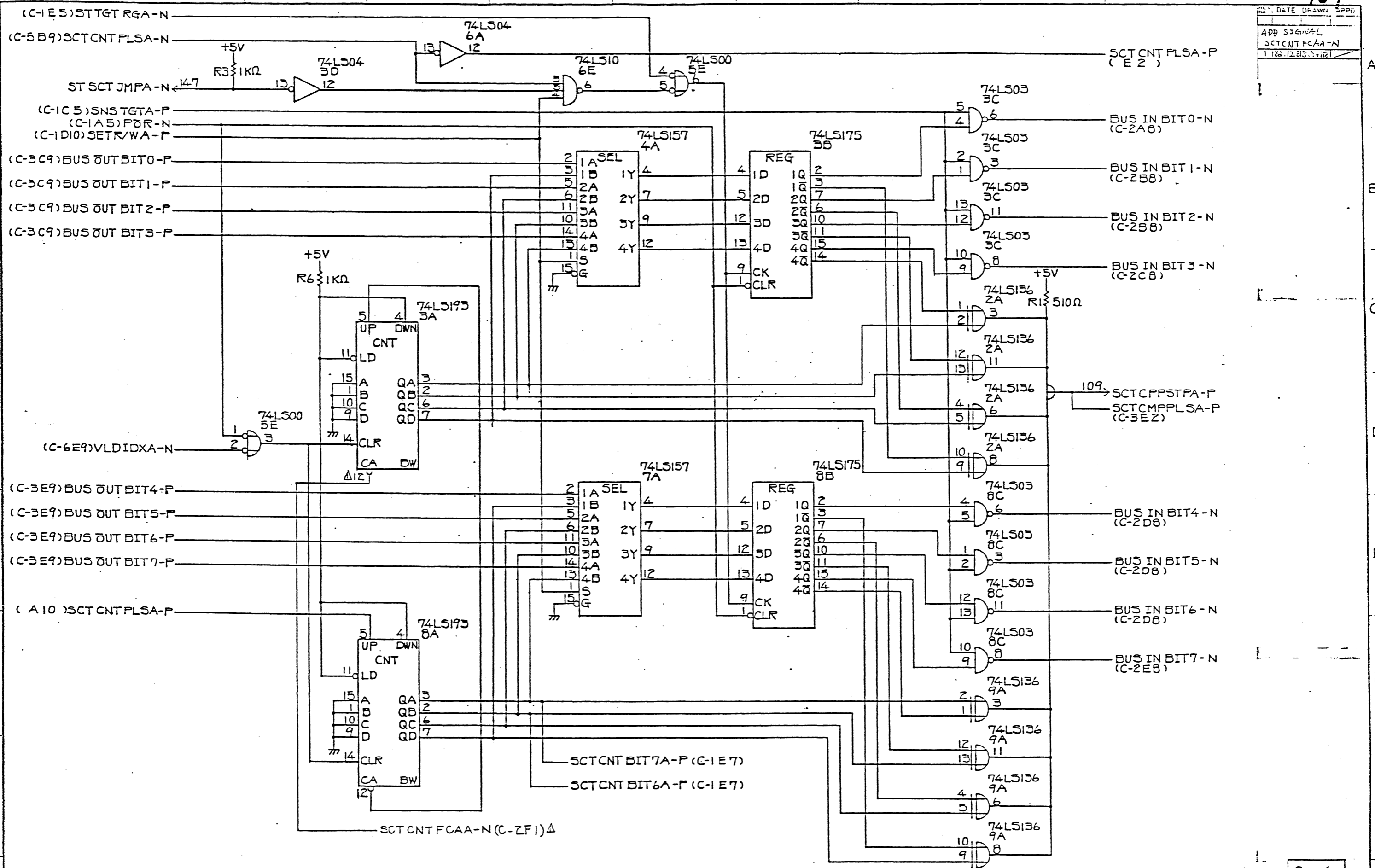


C-3

P/N	TITLE	SHEET 3/	DRAWN
REV	NP 37 DRV LOGIC-DIA.	REV 0	CHECK
	DRAWING NO		APPD
	NPL-NC-20411	Nippon Peripherals Limited	

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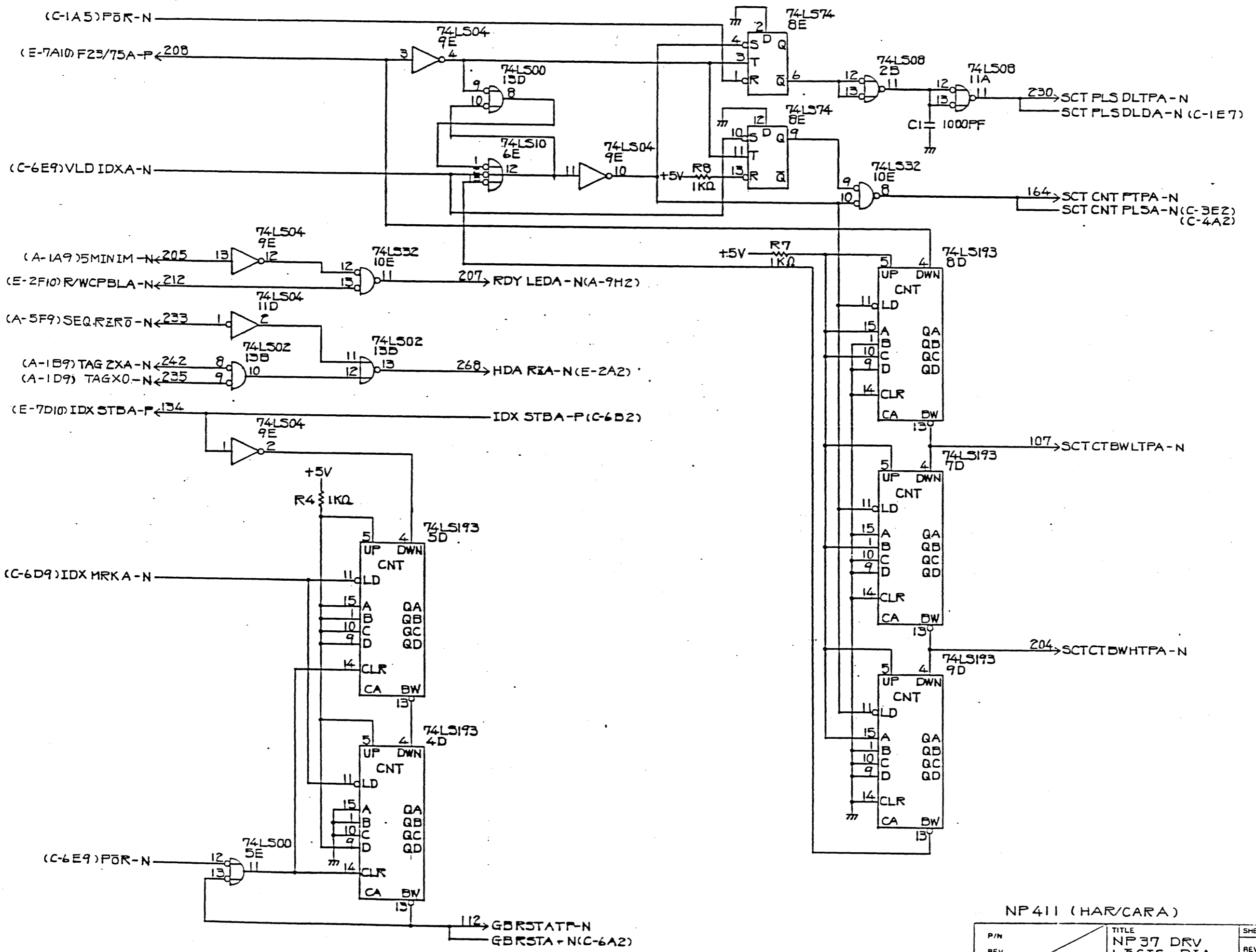
DATE	DRAWN	APPD
ADD SIGNAL	SCTCNT FCAA-N	
1 188.12.83.5.1281		



C-4

NP 411 (HAR/CARA)

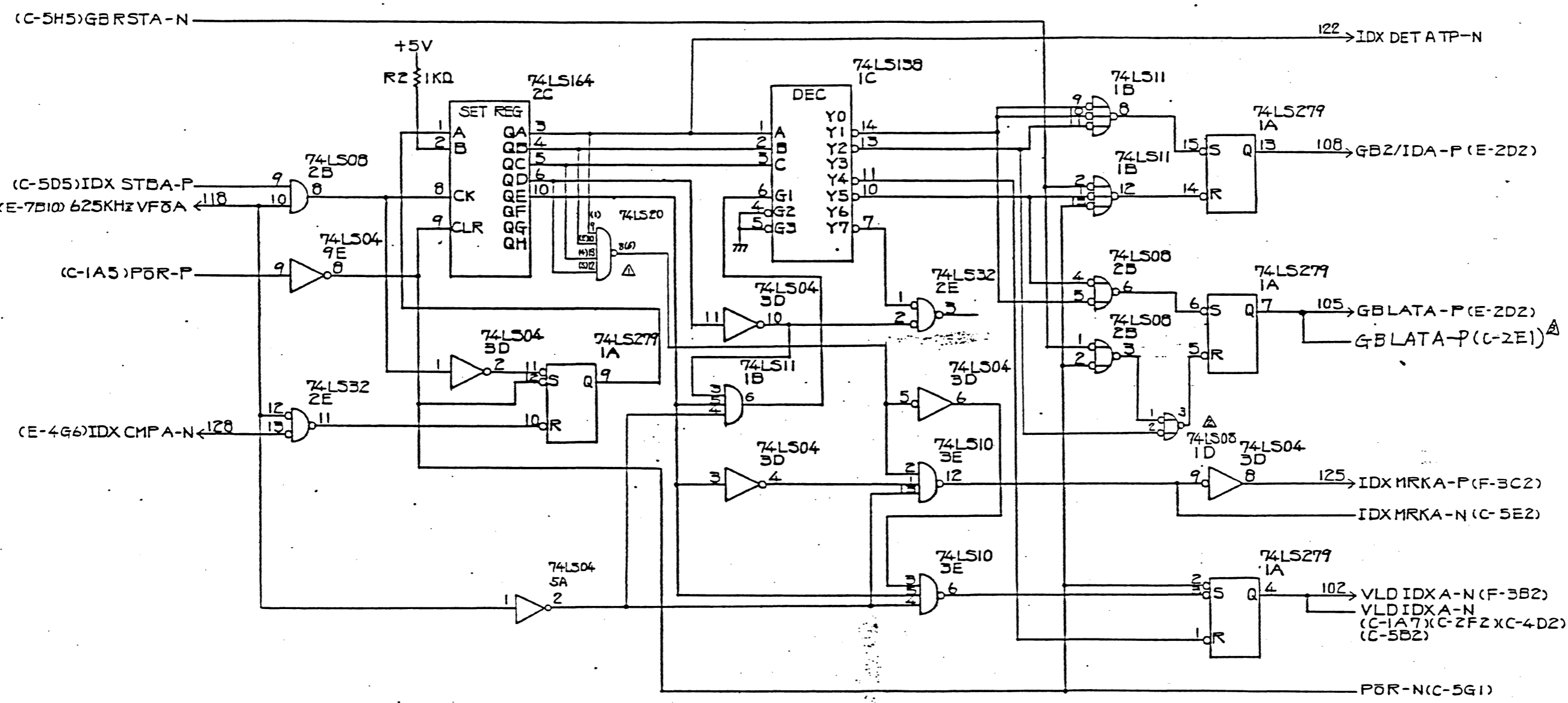
P/N	REV	TITLE NP 37 DRV LOGIC - DIA.	SHEET 4/	DRAWN
			REV 1	CHECK
DRAWING NO NPL-NC-20411		Nippon Peripherals Limited		



C-5

NP411 (HAR/CARA)

P/N	TITLE	SHEET 5/	DRAWN
REV	NP37 DRV LOGIC DIA.	REV 0	CHECK
	DRAWING NO		APPD
	NPL-NC-20411	Nippon Peripherals Limited	



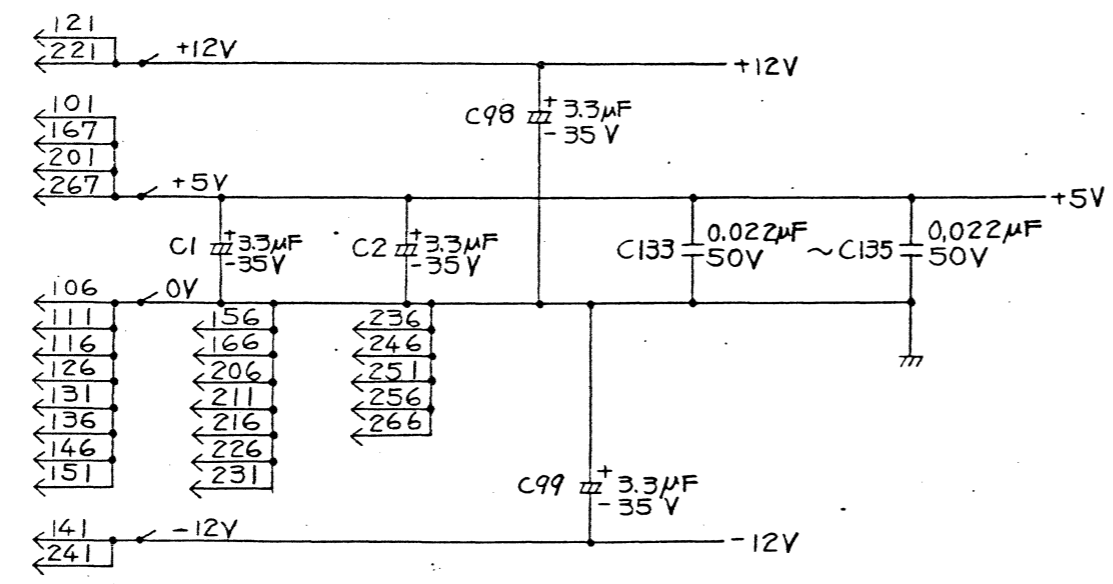
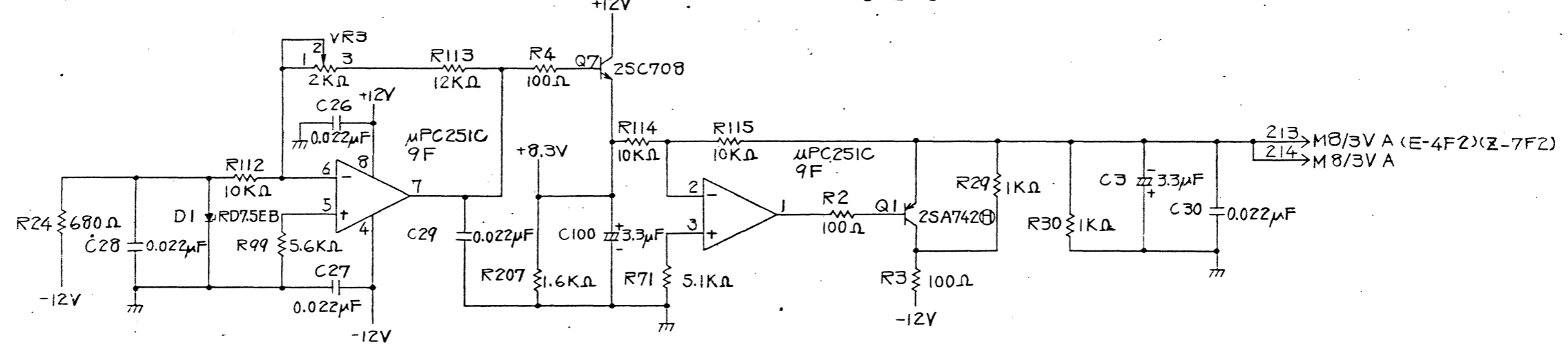
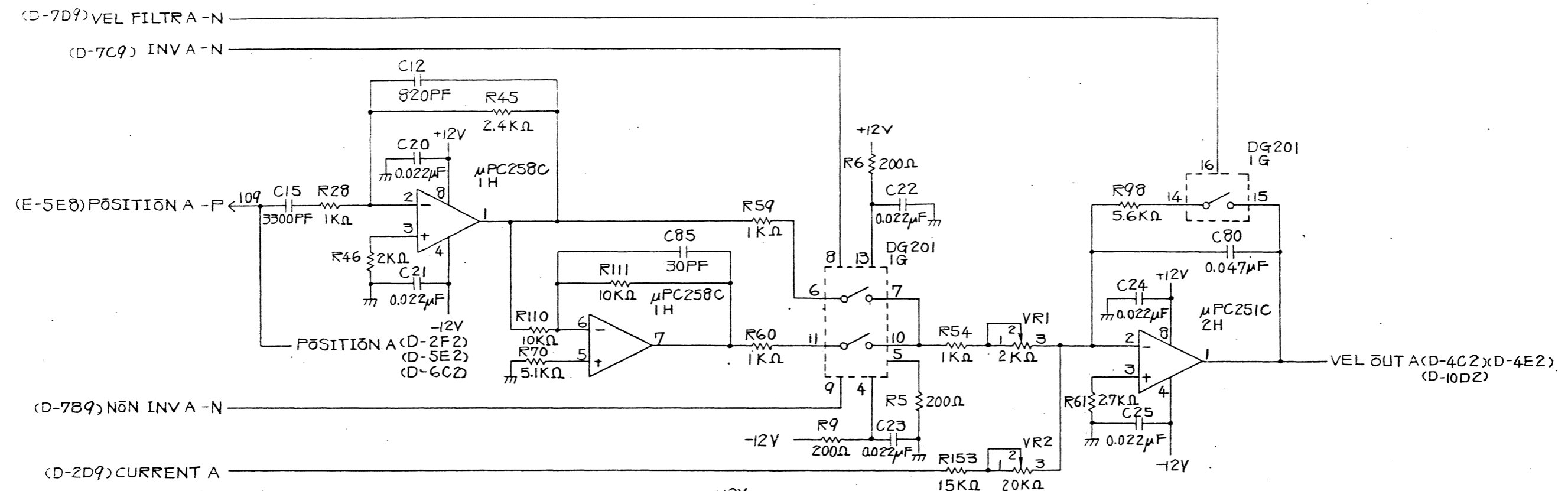
DATE	DRAWN	APPD
For PB Assy		
NPL-NY-4041 00-0		
74LS20 → 4E 1.2.4.5.6		
From NPL-NY-4041 01-1~		
74LS20 → 2D 3.9.10.11.13		
1 182.2.26		
Circuit		
74LS08	74LS279	
2B-3	1A-5	
Connect		
74LS08	74LS08	
2B-3	1B-1	
74LS138	74LS08	
1C-13	1B-2	
74LS08	74LS279	
1B-3	1A-5	
2 182.5.20		
APP SIGN K ADDRESS		
OF GBLAT		
3 182.6.15		

C-6

NP 411 (HAR/CARA)

P/N	TITLE	SHEET	DRAWN
REV	NF 37 DRV LOGIC - DIA.	66	
	DRAWING NO	REV	CHECK
	NPL-NC-20411	3	APPD
		Nippon Peripherals Limited	

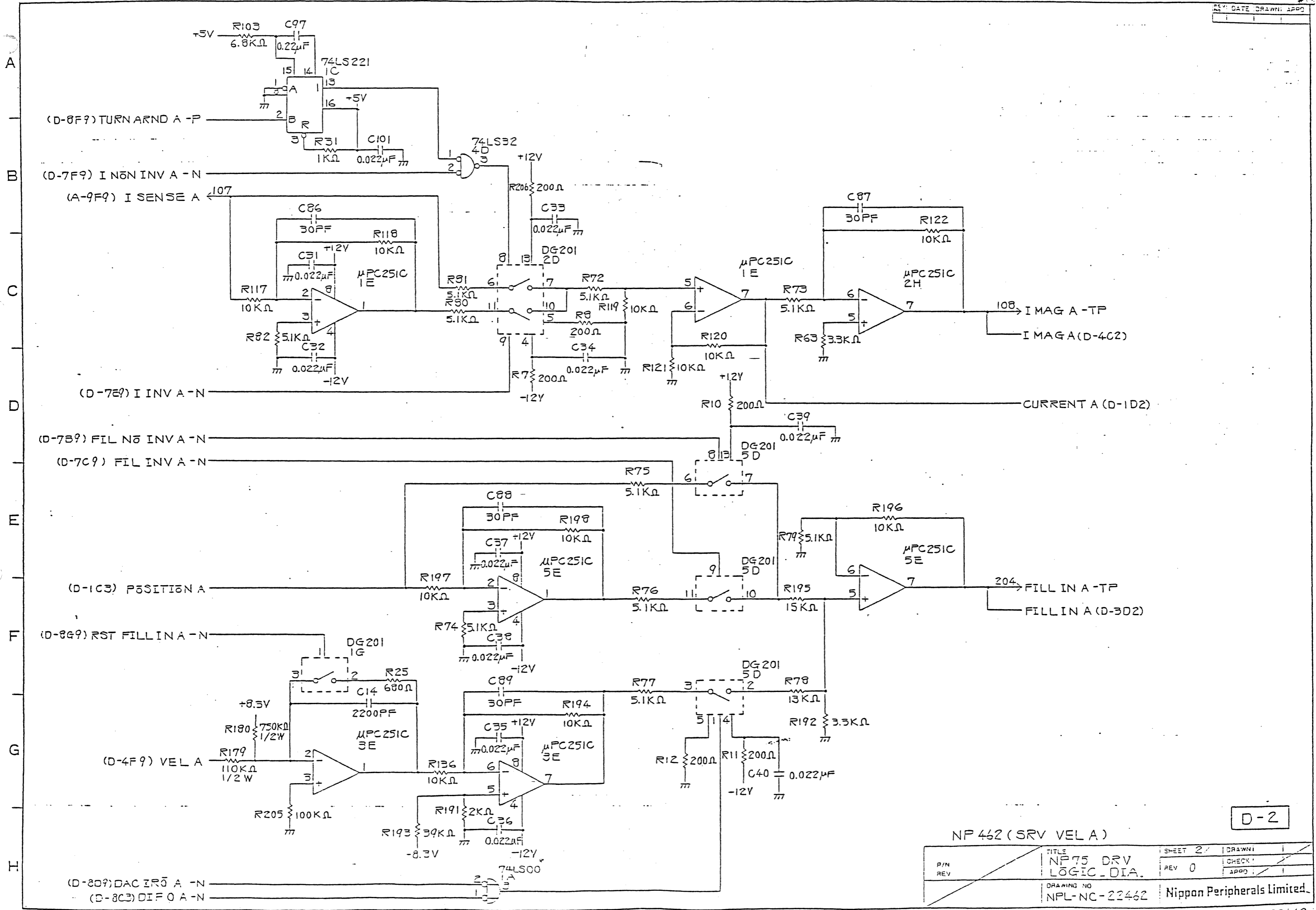
113



D-1

NP 462 (SRV VEL A)

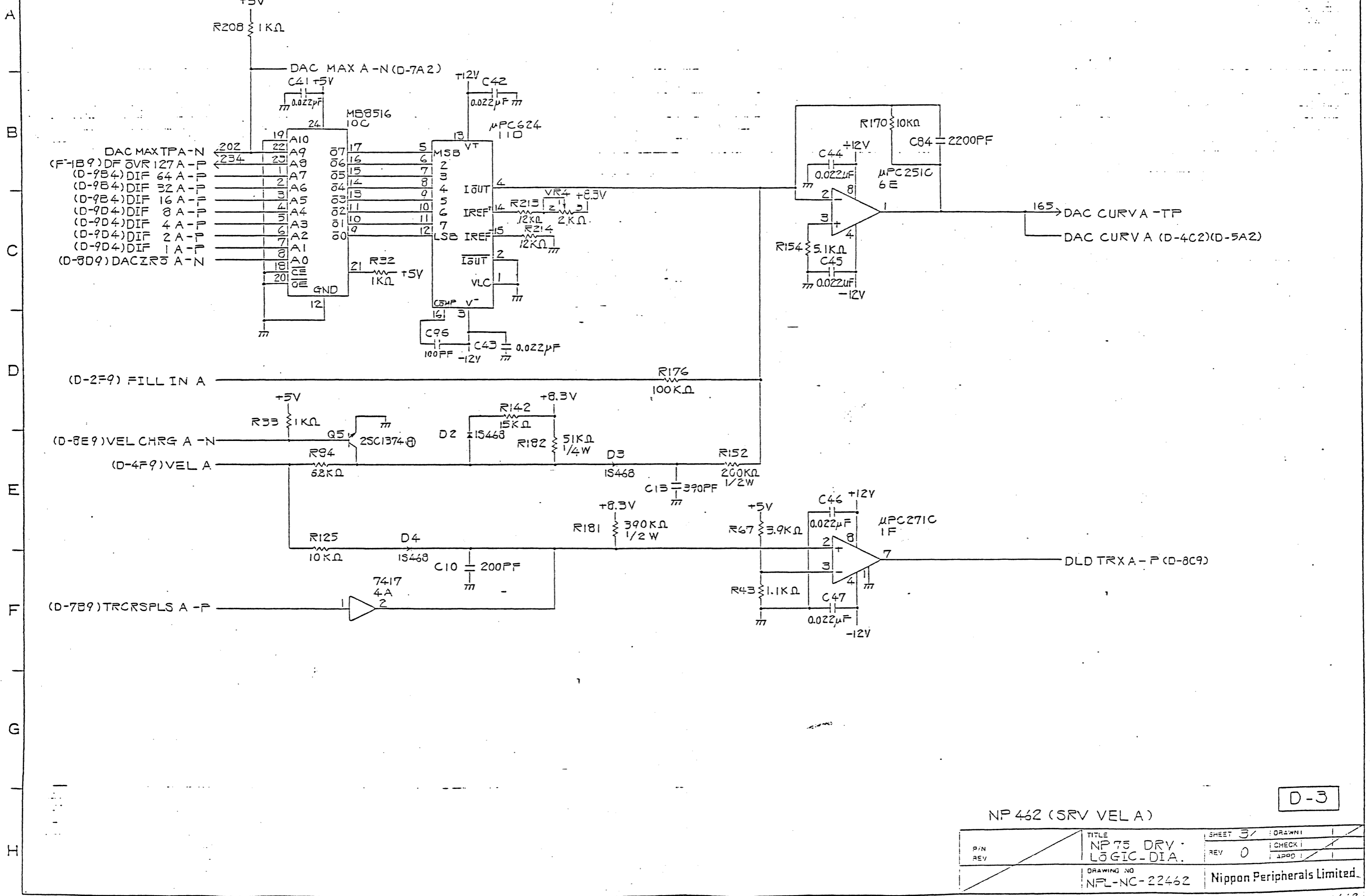
NP 462	TITLE NP 75 DRV LOGIC-DIA.	SHEET 1/10	DRAWN T.S. 9.5
P/N REV G		REV D	CHECK APPD agi 108 9.5
SRV VEL A	DRAWING NO NPL-NC-22462	Nippon Peripherals Limited	



D-2

NP 462 (SRV VEL A)

P/N REV	TITLE NP 75 DRV LOGIC - DIA.	SHEET 2 /	DRAWN
	DRAWING NO NPL-NC-22462	REV 0	CHECK
Nippon Peripherals Limited.		APPD	

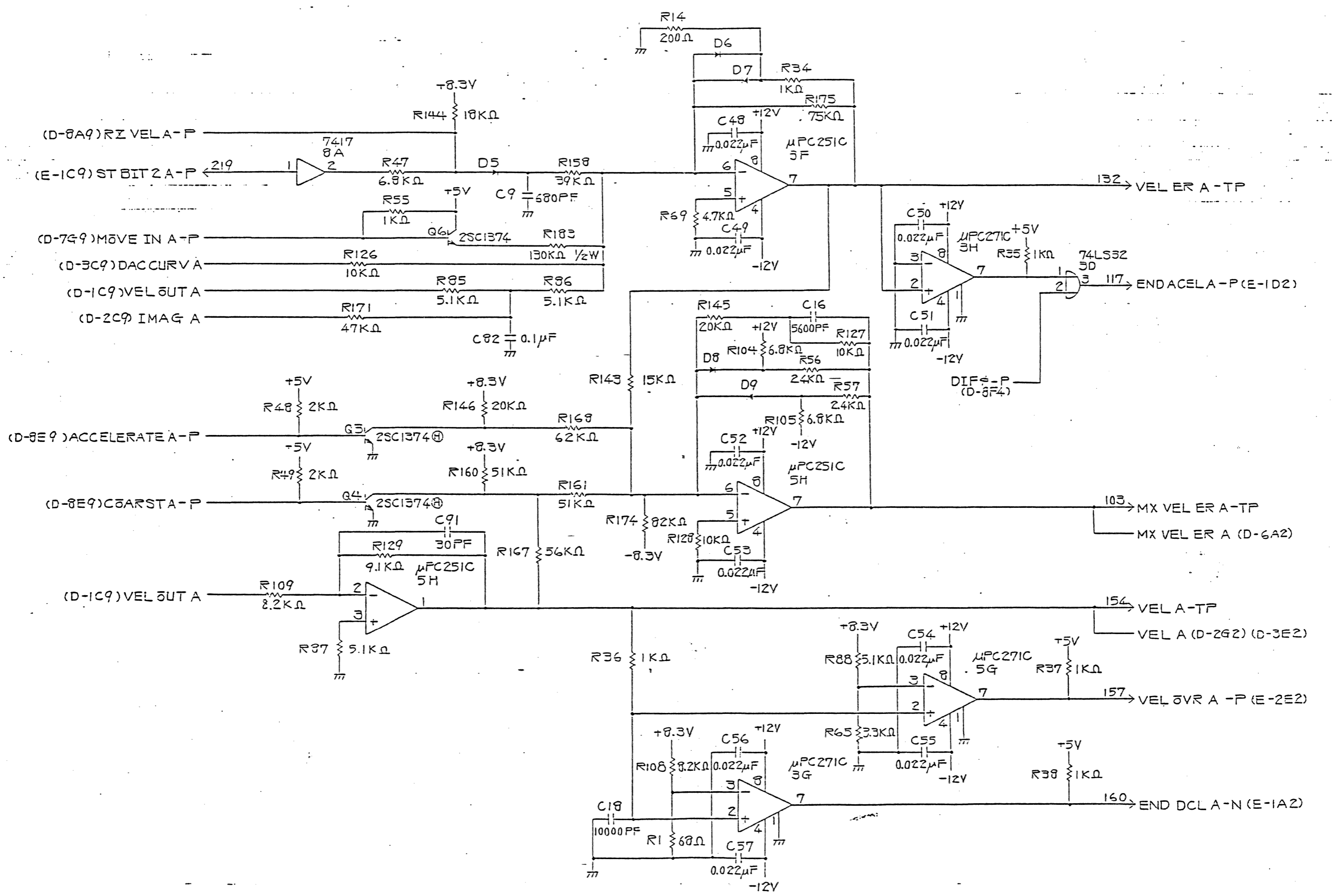


D-3

NP 462 (SRV VEL A)

P/N	TITLE	SHEET 3 /	DRAWN
REV	NP 75 DRY - LOGIC-DIA.	REV 0	CHECK
DRAWING NO		Nippon Peripherals Limited.	
NFL-NC-22462		NC-22462	

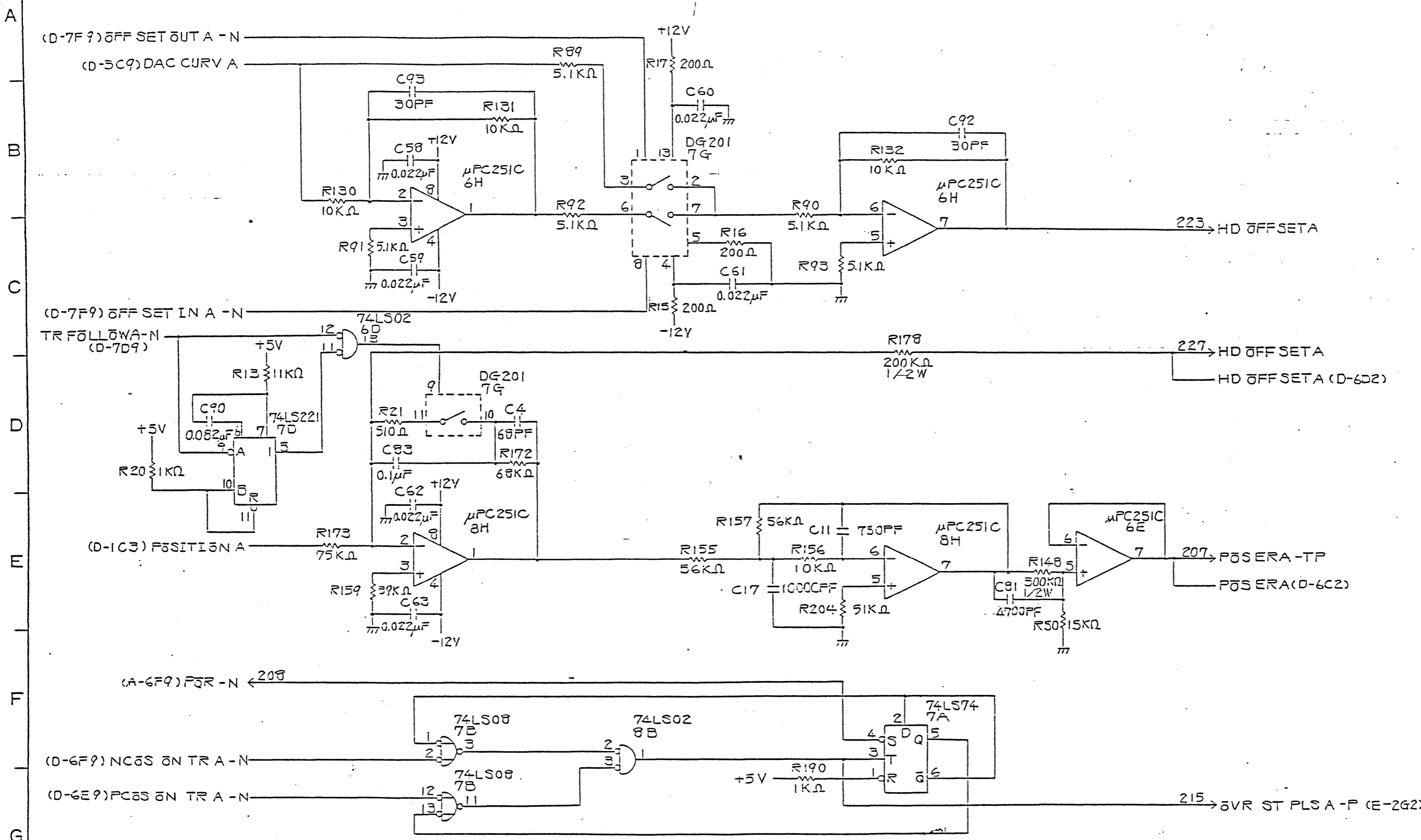
A
B
C
D
E
F
G
H



D-4

NP462 (SRV VEL A)

P/N REV	TITLE NP 75 DRV. LOGIC DIA.	SHEET 4	DRAWN
	DRAWING NO NPL-NC-22462	REV 0	CHECK APPD
Nippon Peripherals Limited.			

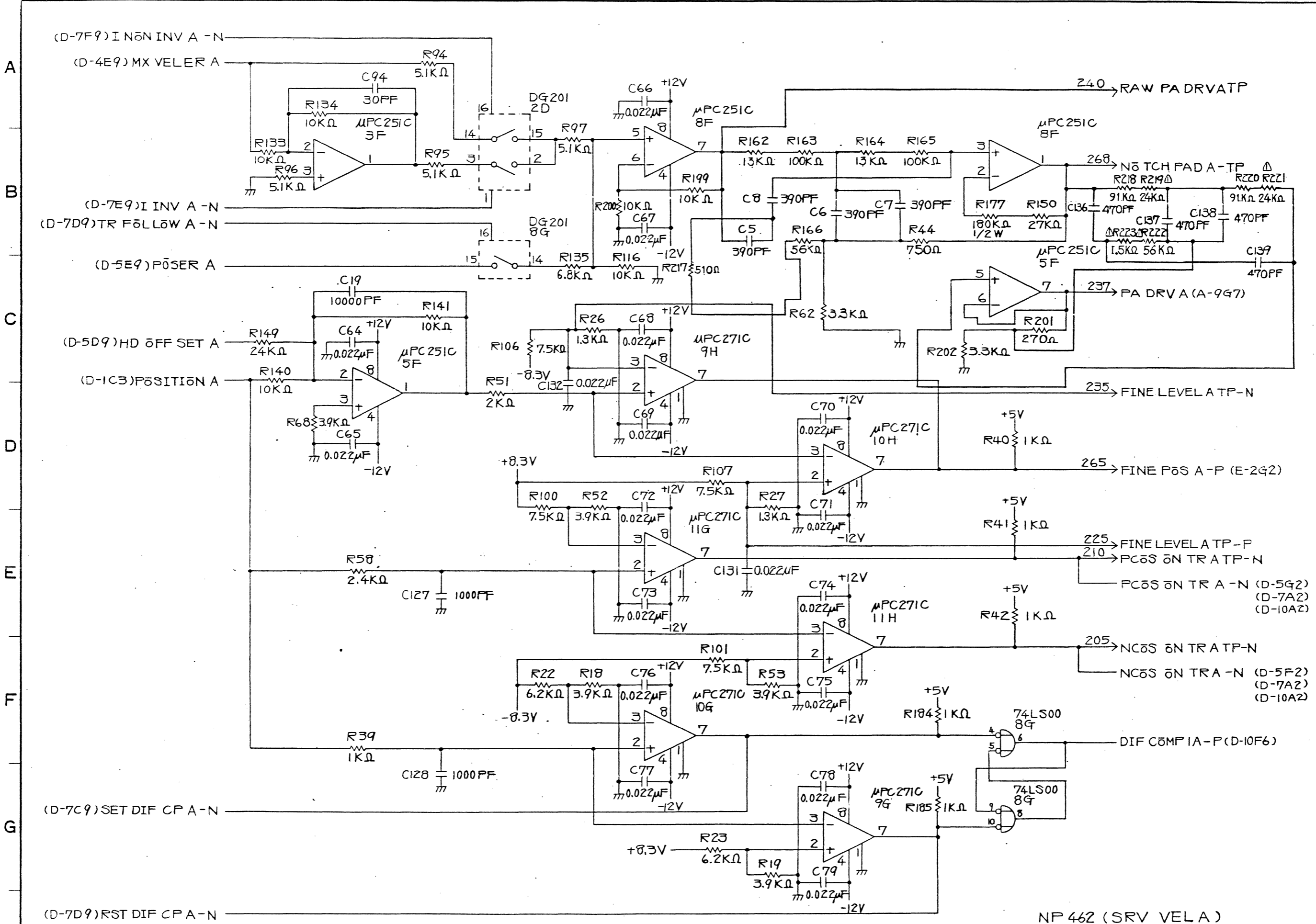


D-5

NP 462 (SRV VEL A)

P/N	REV	TITLE	SHEET	DRAWN
		NP 75 DRV LOGIC-DIA.	5 /	
		DRAWING NO	CHECK	APPD
		NPL-NC-22462	2	
Nippon Peripherals Limited.				

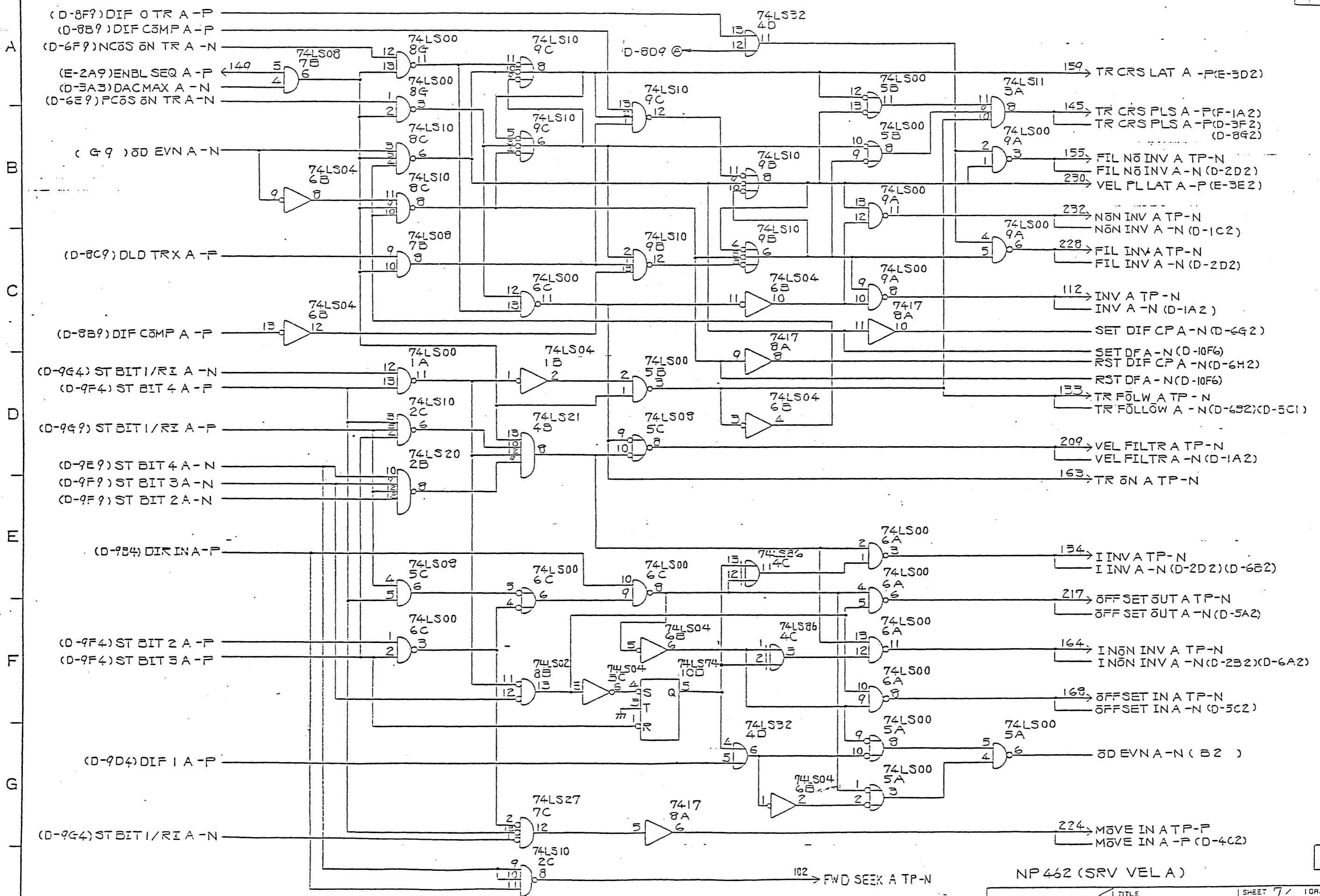
DATE DRAWN APPD
 R219, 221: 56KΩ → 24KΩ
 R222: 68KΩ → 56KΩ
 R223: 5.6KΩ → 1.5KΩ
 1 85-2-24



NP 462 (SRV VEL A)

D-6

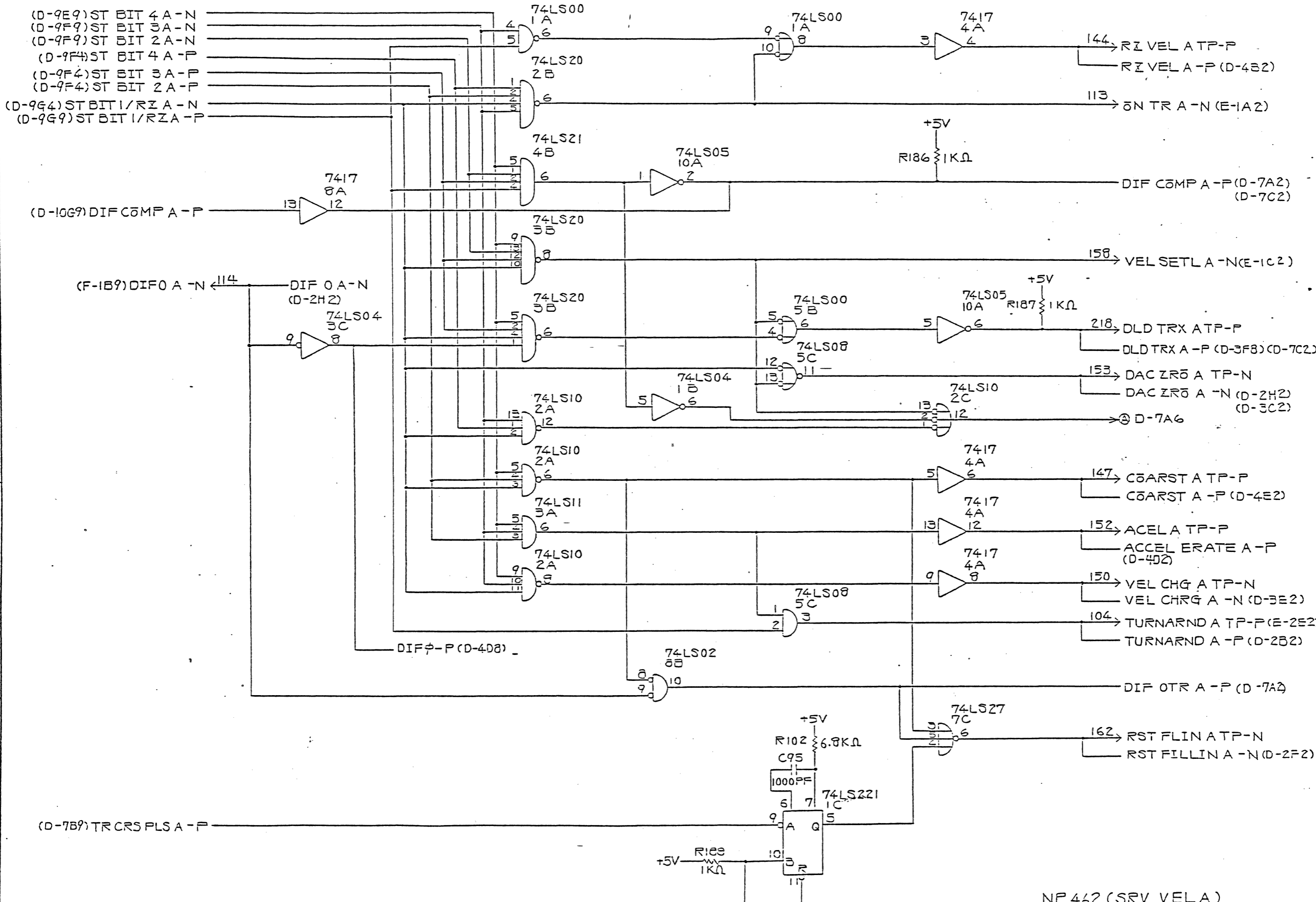
P/N REV	TITLE NP 75 DRV LOGIC-DIA.	SHEET 6 /	DRAWN
	DRAWING NO NPL-NC-22462	REV 1	CHECK APPD
Nippon Peripherals Limited			



D-7

NP 462 (SRV VEL A)

P/N	REV	TITLE	SHEET	DRAWN
		NP 75 DRV LOGIC DIA.	7 /	
		DRAWING NO	REV	CHECK
		NPL-NC-22462	0	APPROV
Nippon Peripherals Limited.				

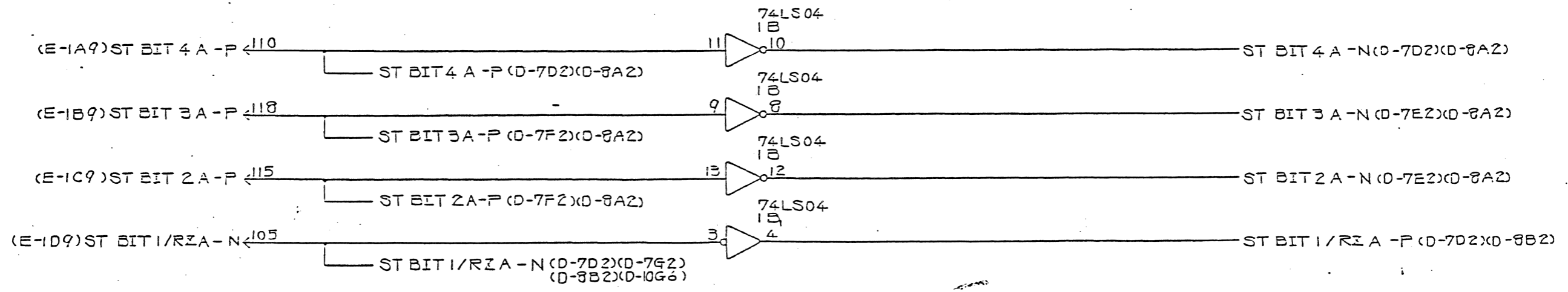
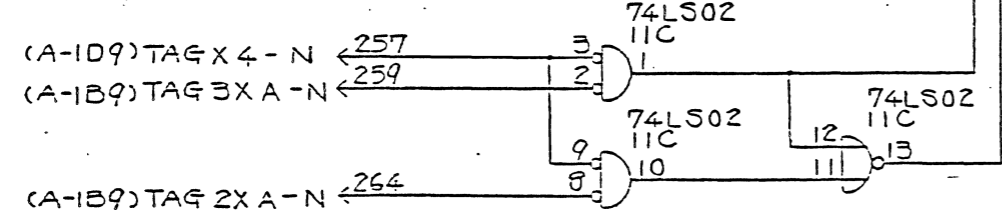
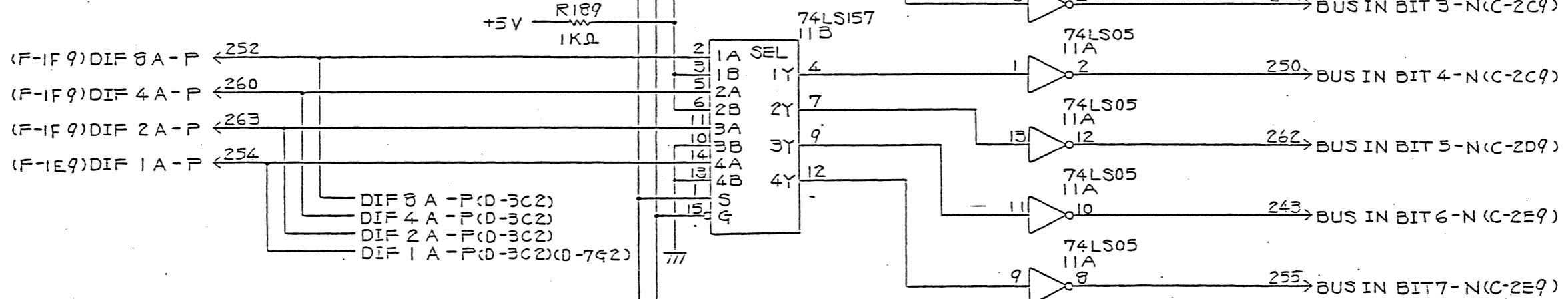
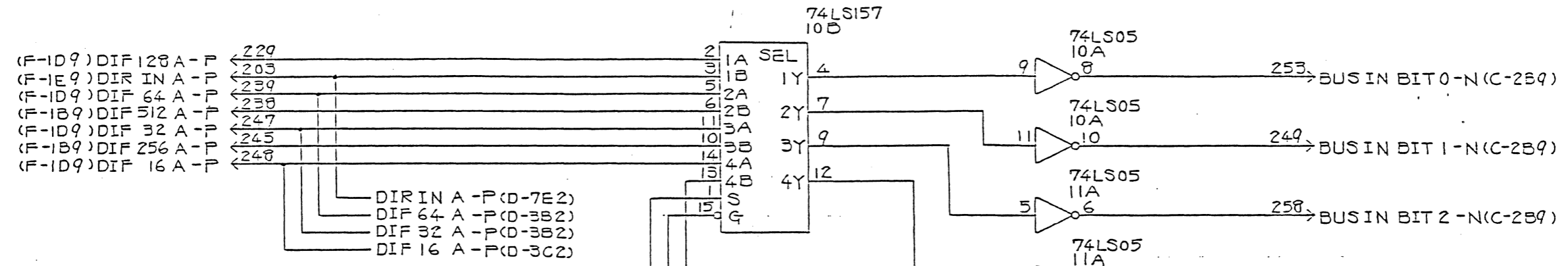


NP 462 (SRV VELA)

D-8

P/N	TITLE	SHEET 5/	DRAWN
REV	NP 75 DRV LOGIC-DIA.	REV 0	CHECK
DRAWING NO		1990	
NPL-NC-22462		Nippon Peripherals Limited	

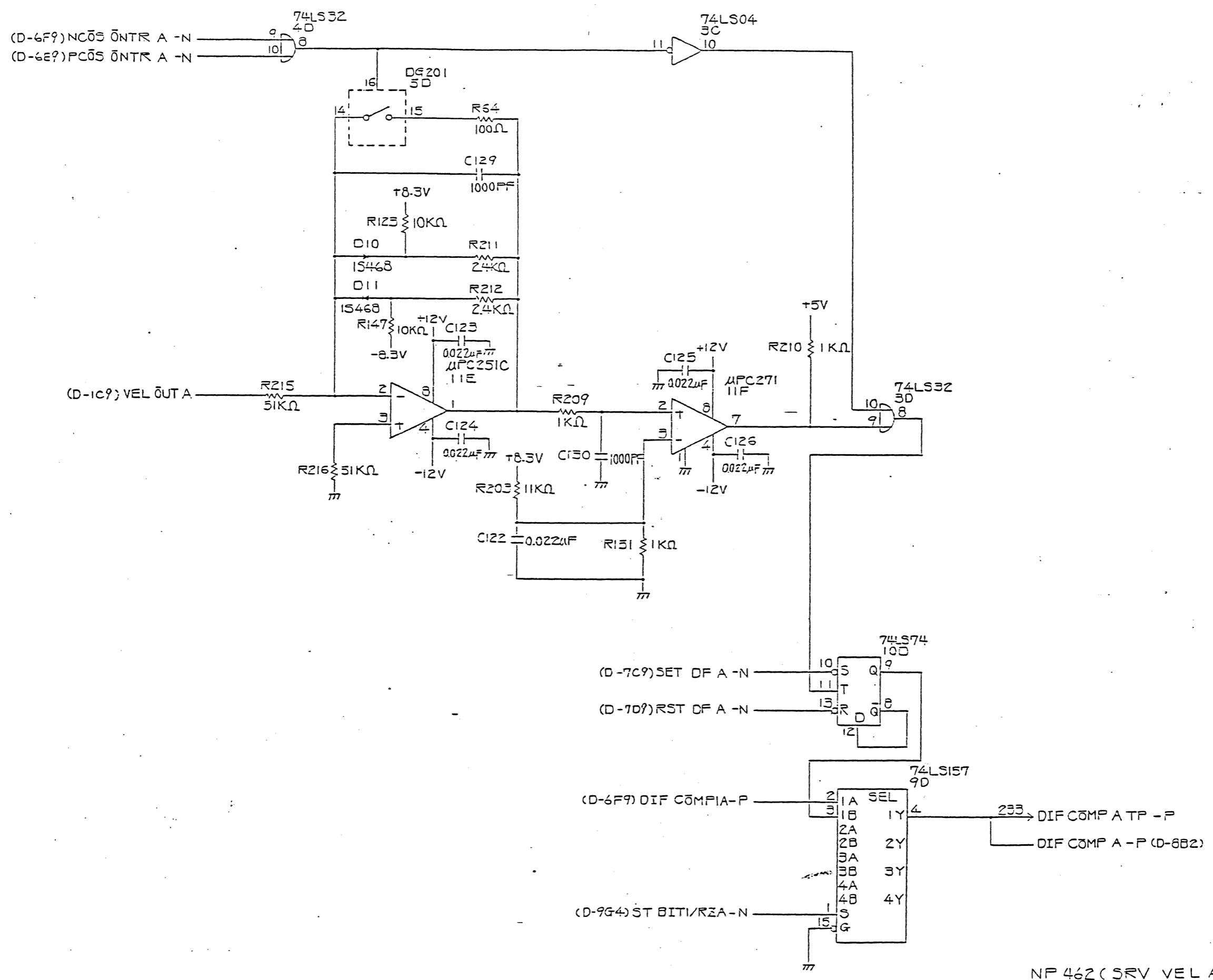
A
B
C
D
E
F
G
H



NP462 (SRV VEL A)

D-9

P/N REV	TITLE NP75 DRV. LOGIC-DIA.	SHEET 9 / 10 DRAWN	CHECK
	DRAWING NO NPL-NC-22462	REV 0	APPD
Nippon Peripherals Limited			

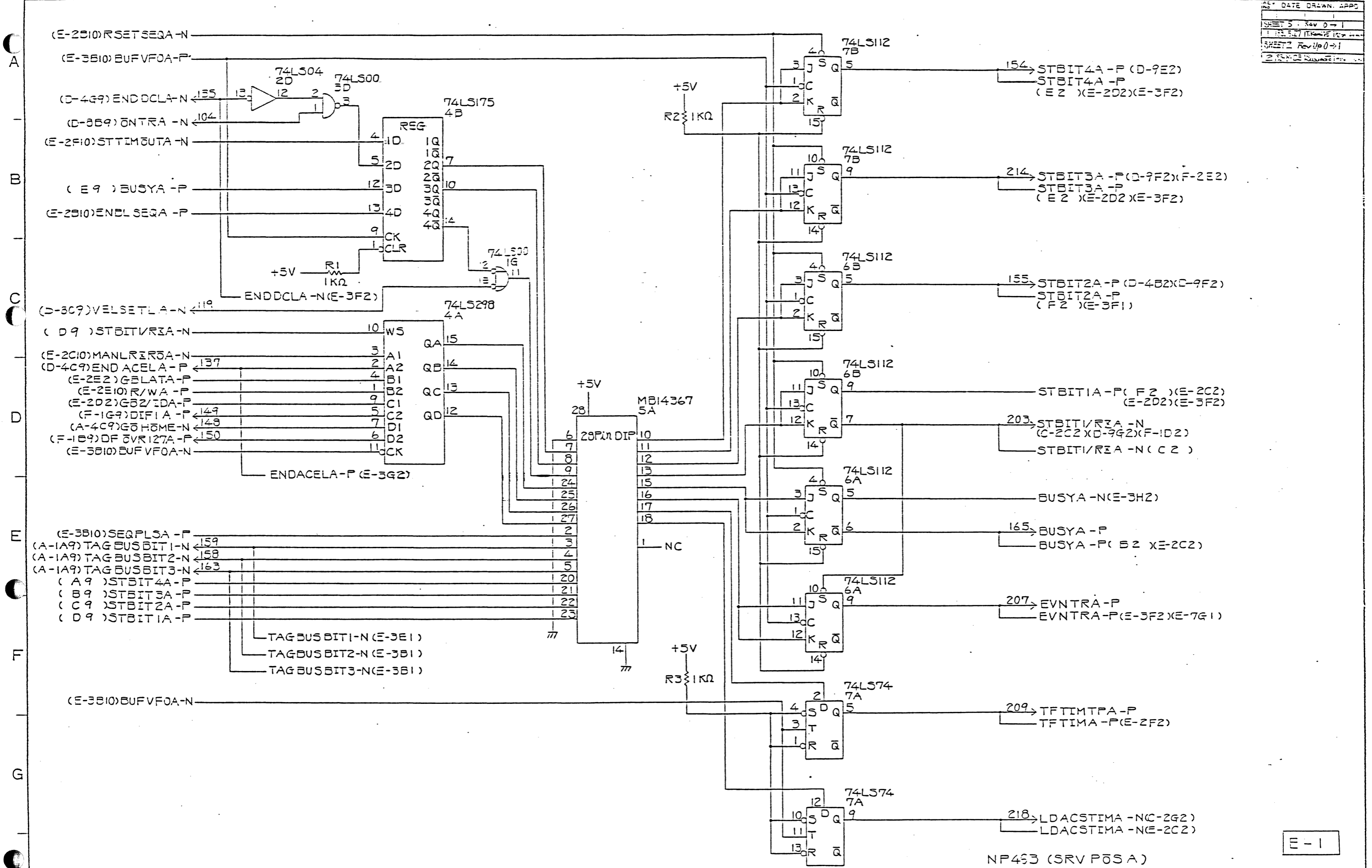


D-10

NP 462 (SRV VEL A)

P/N	TITLE	SHEET 10 / 10	DRAWN
REV	NP 75 DRV LOGIC - DIA.	REV 0	CHECK
	DRAWING NO	Nippon Peripherals Limited	
	NPL-NC -22462		

DATE	DRAWN	APPD
SHEET 5	Rev 0	1
SHEET 2	Rev Up 0	1



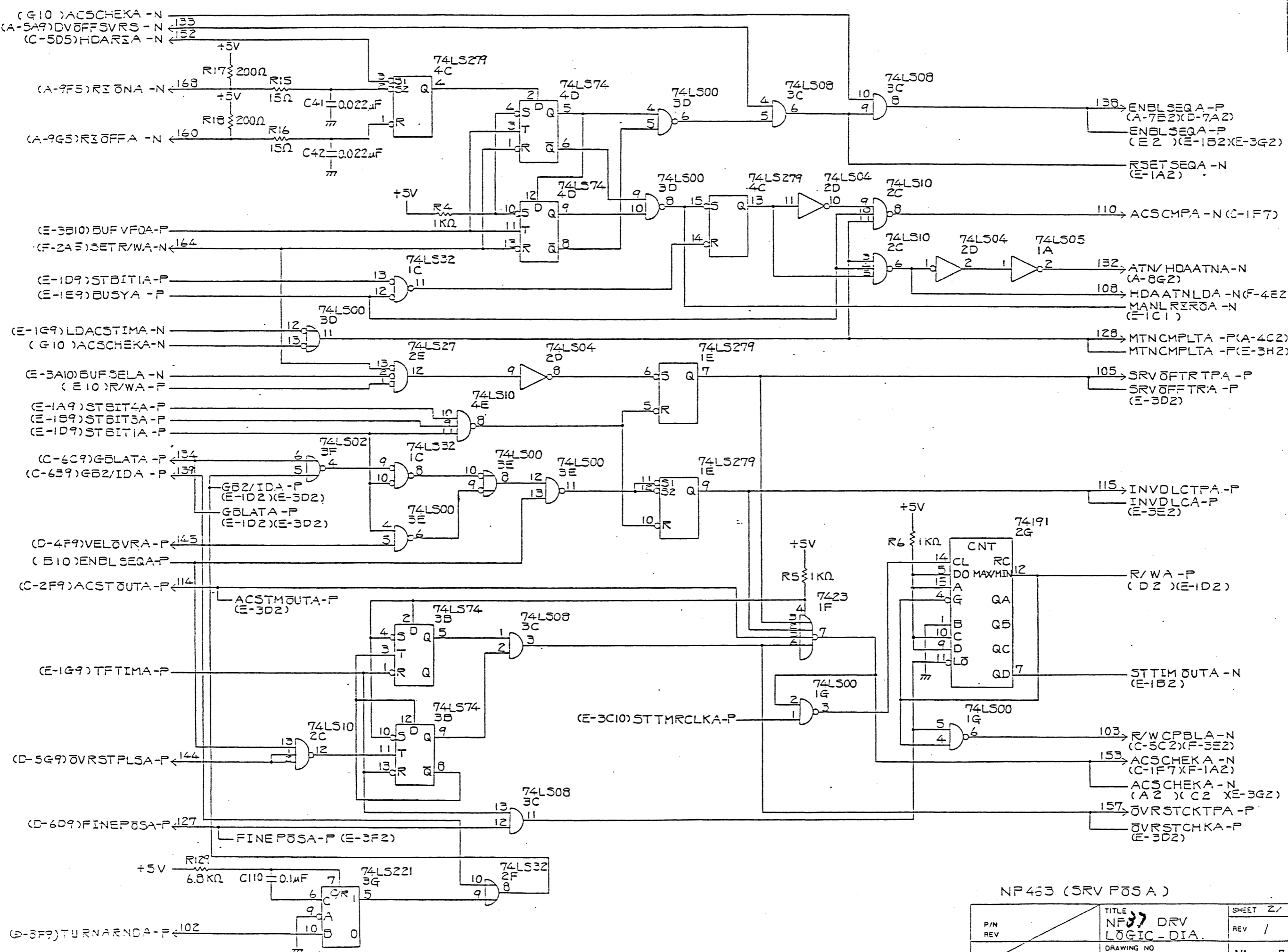
注. 指定なき抵抗はすべて1/4Wとする.

E-1

NP453 (SRV P05A)

P/N	REV	TITLE	SHEET	DATE	DRAWN	APPD
NP453	B	NP-37 DRV LOGIC-DIA.	1/1	1982.05.16
SRV P05A		DRAWING NO	REV	CHECK	APPD	
		NPL-NC-20453	2	1982.05.16
Nippon Peripherals Limited						

REV	DATE	DRAWN	APPD
25	7/81	1	
Paper 6 → 3H			
1/15/22/22/80			

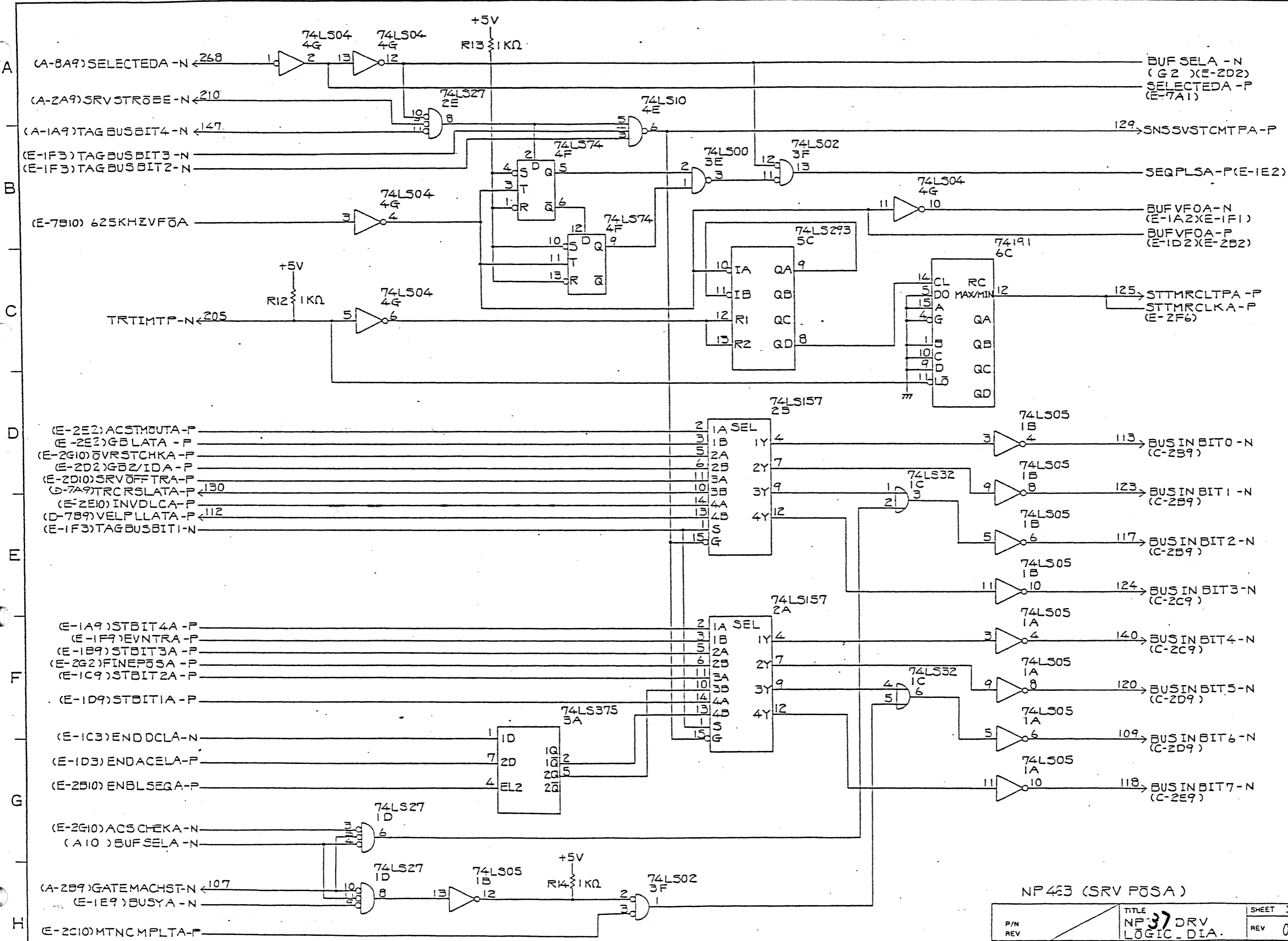


NP463 (SRV PDS A)

P/N REV	TITLE	SHEET 2 / 10 DRAWN
	DRV LOGIC-DIA.	CHECK
	DRAWING NO	APPD
NPL-NC-20463		Nippon Peripherals Limited

E-2

125

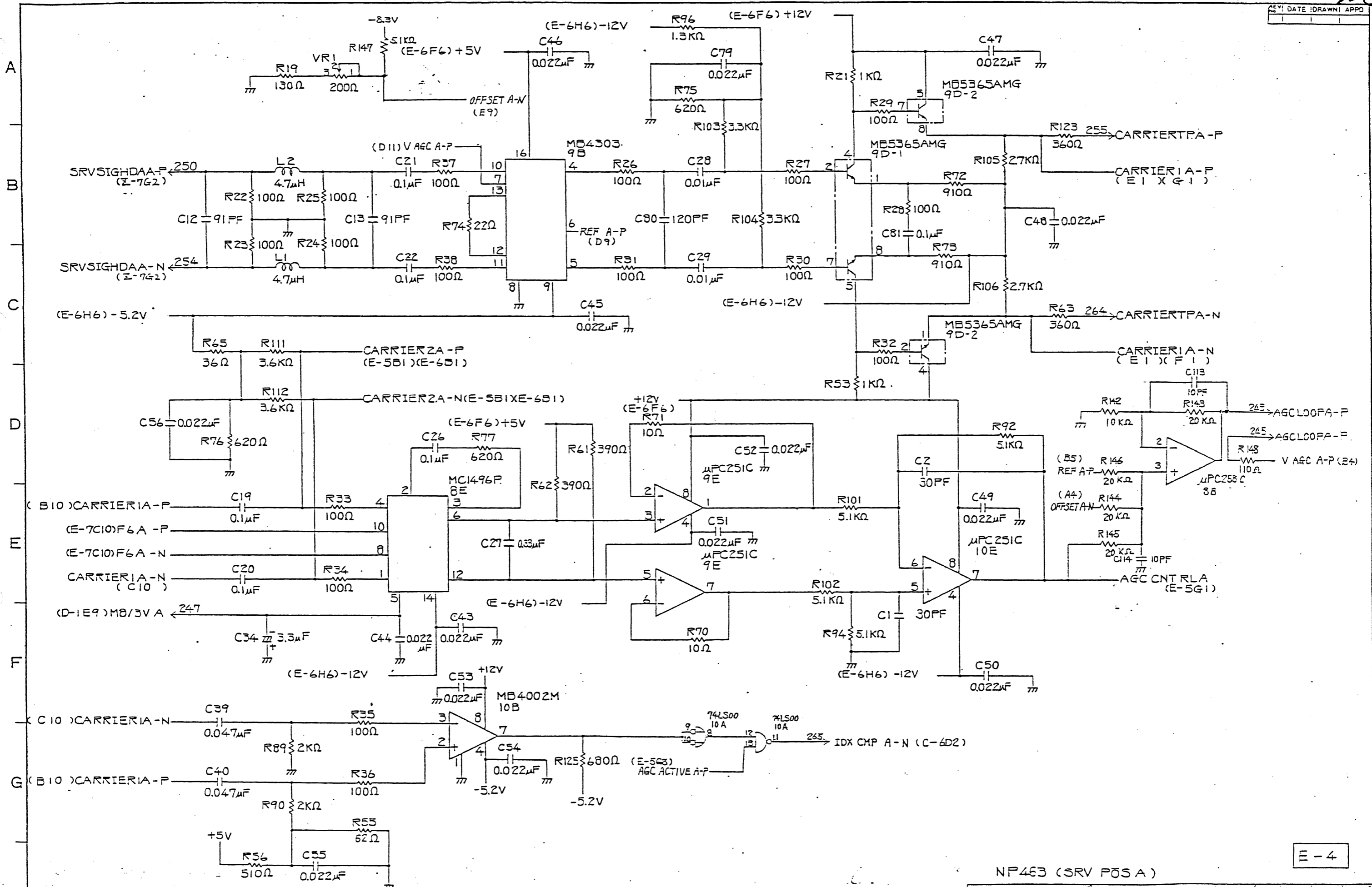


E-3

NP 463 (SRV P05A)

P/N REV	TITLE NP 37 DRV LOGIC DIA.	SHEET 3/ REV 0	DRAWN	CHECK
	DRAWING NO NPL-NC-20463	APPD		
Nippon Peripherals Limited				

126



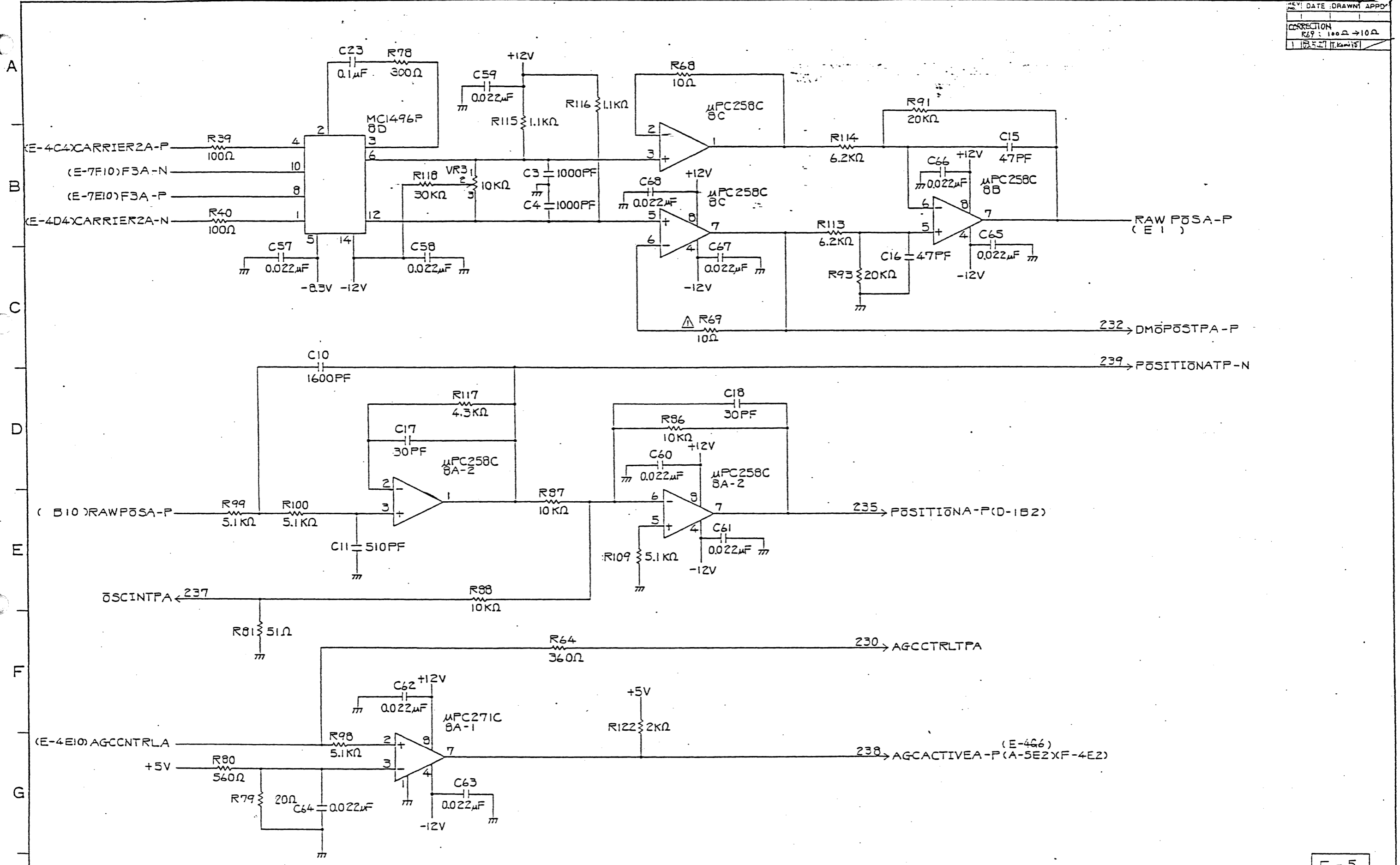
E-4

NF463 (SRV POS A)

P/N REV	TITLE NF 463 DRV LOGIC-DIA.	SHEET 4/	DRAWN
	DRAWING NO NPL-NC-20463	REV 0	CHECK I APPD
Nippon Peripherals Limited			

127

REV	DATE	DRAWN	APPD
CORRECTION	R69: 100Ω → 10Ω		
	1 19 5 27		

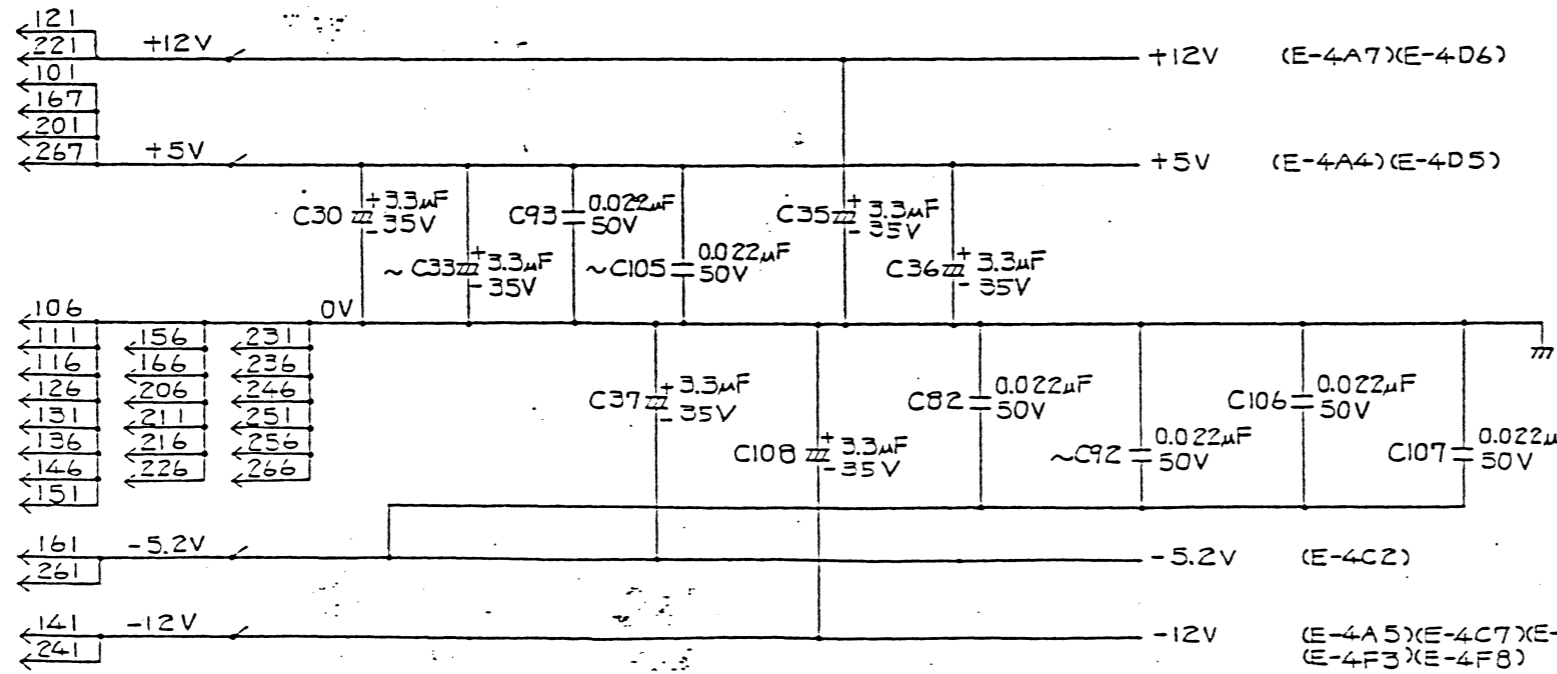
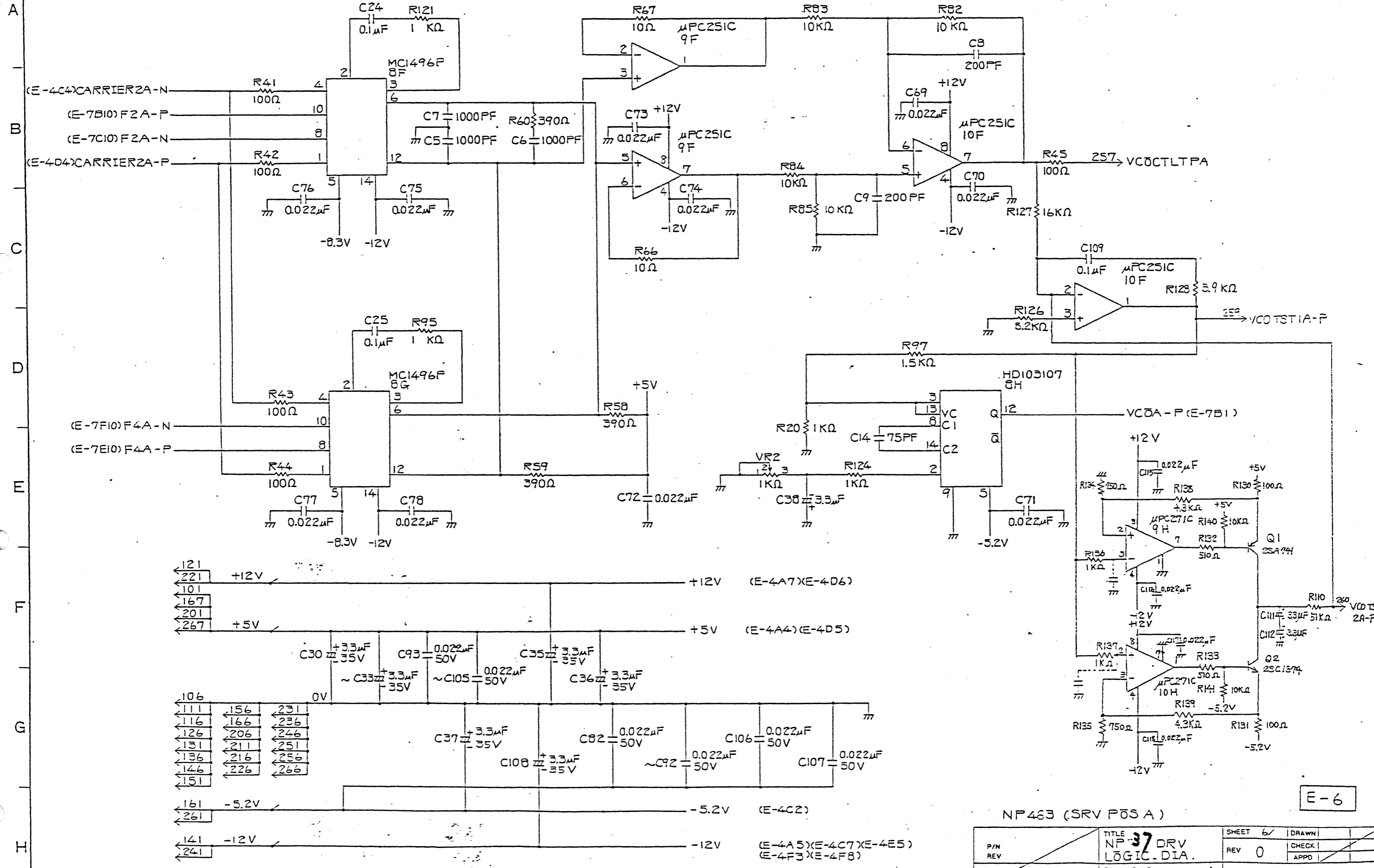


E-5

NP.463 (SRV P0S A)

P/N REV	TITLE NP 37 DRV LOGIC_DIA.	SHEET 5 /	DRAWN
	DRAWING NO NPL-NC-20463	REV 1	CHECK APPD
Nippon Peripherals Limited			

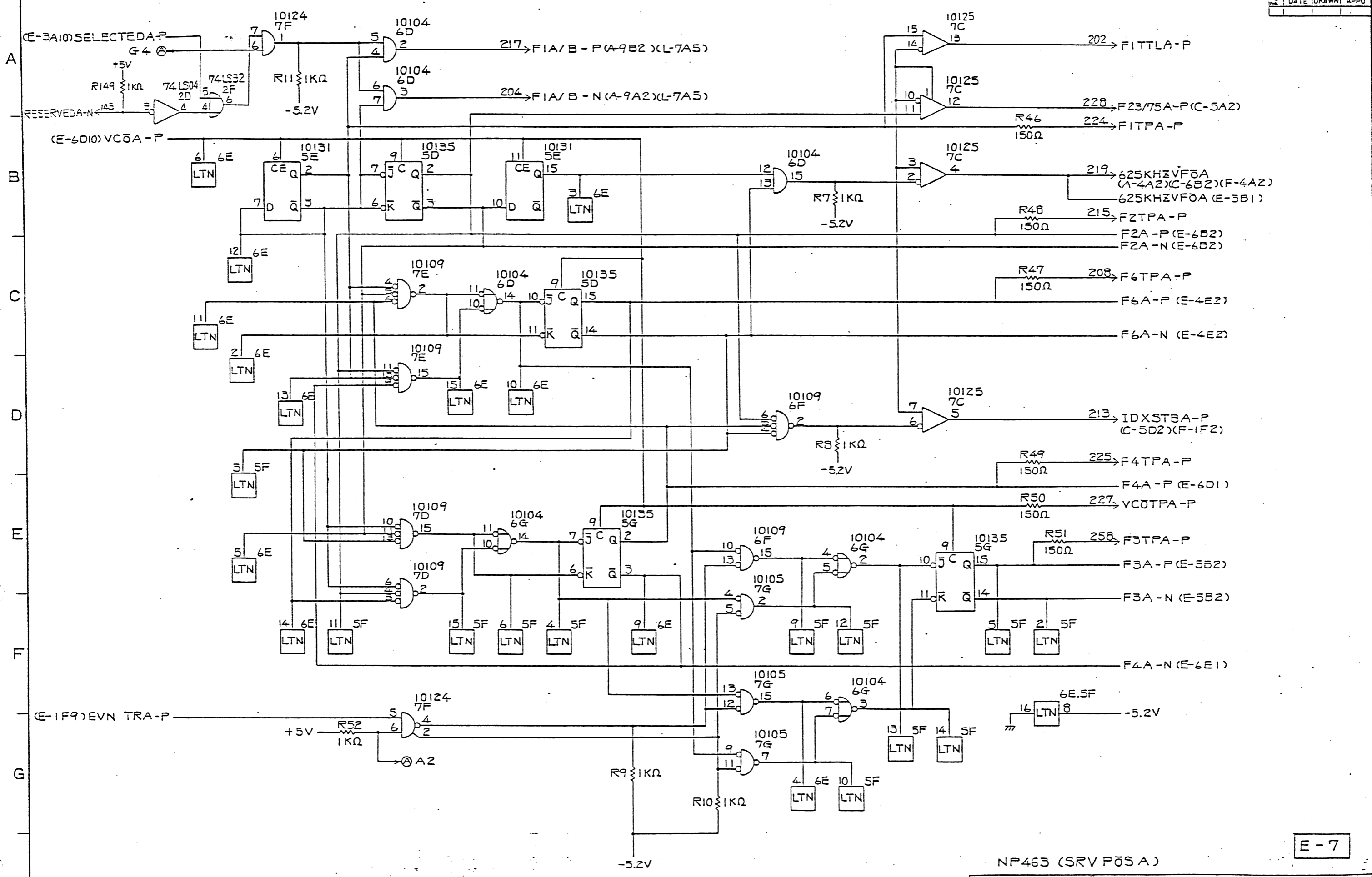
128



NF463 (SRV P05 A)

E-6

P/N REV	TITLE	SHEET	DRAWN
	NP-37 DRV LOGIC-DIA.	6/	
DRAWING NO	REV	CHECK	APPD
	NPL-NC-20463	0	
Nippon Peripherals Limited			

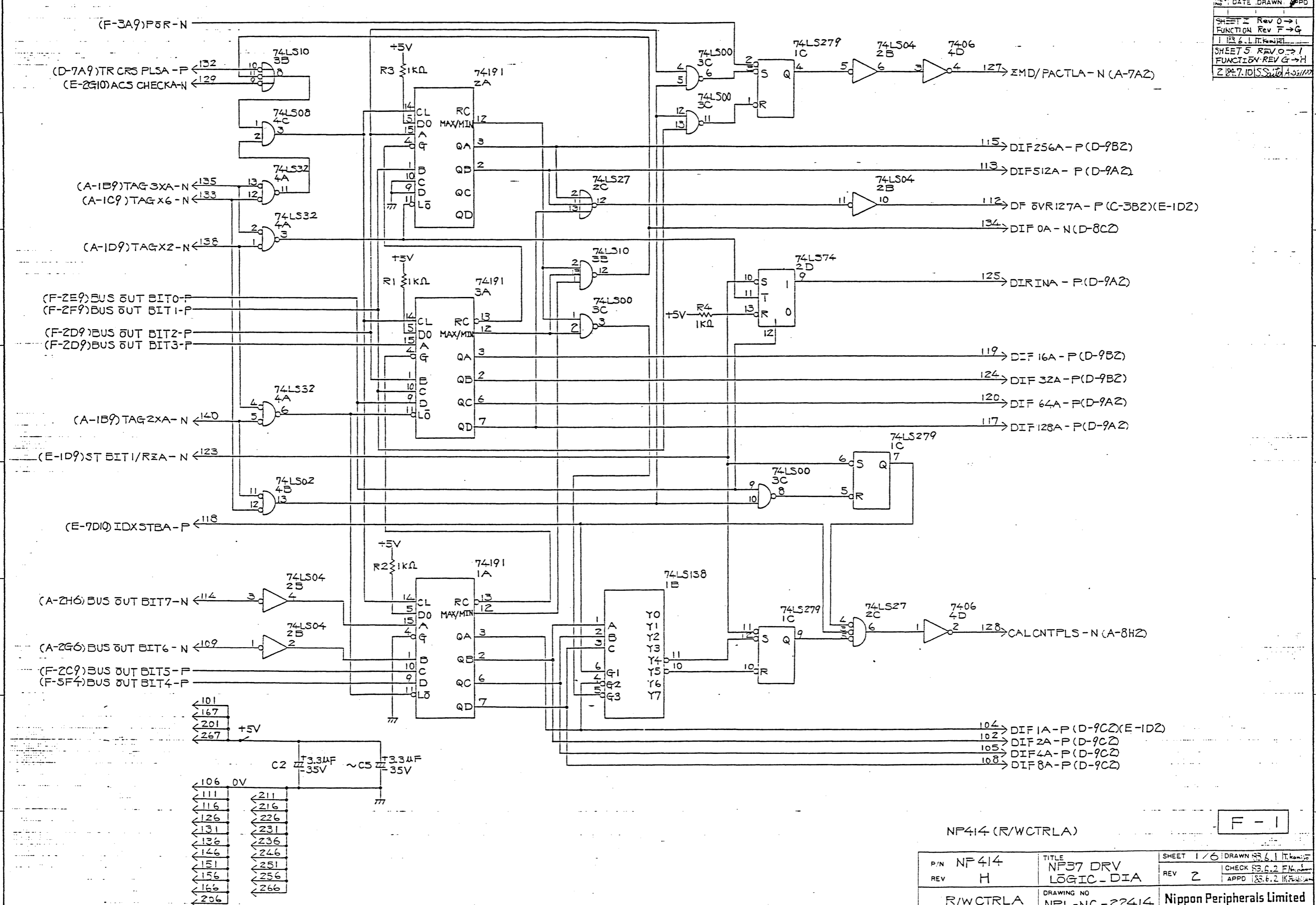


E-7

NP463 (SRV POS A)

P/N REV	TITLE	SHEET 7/7	DRAWN
	NF 37 DRV LOGIC-DIA.	REV 0	CHECK
	DRAWING NO	APPD	
NPL-NC-20463		Nippon Peripherals Limited	

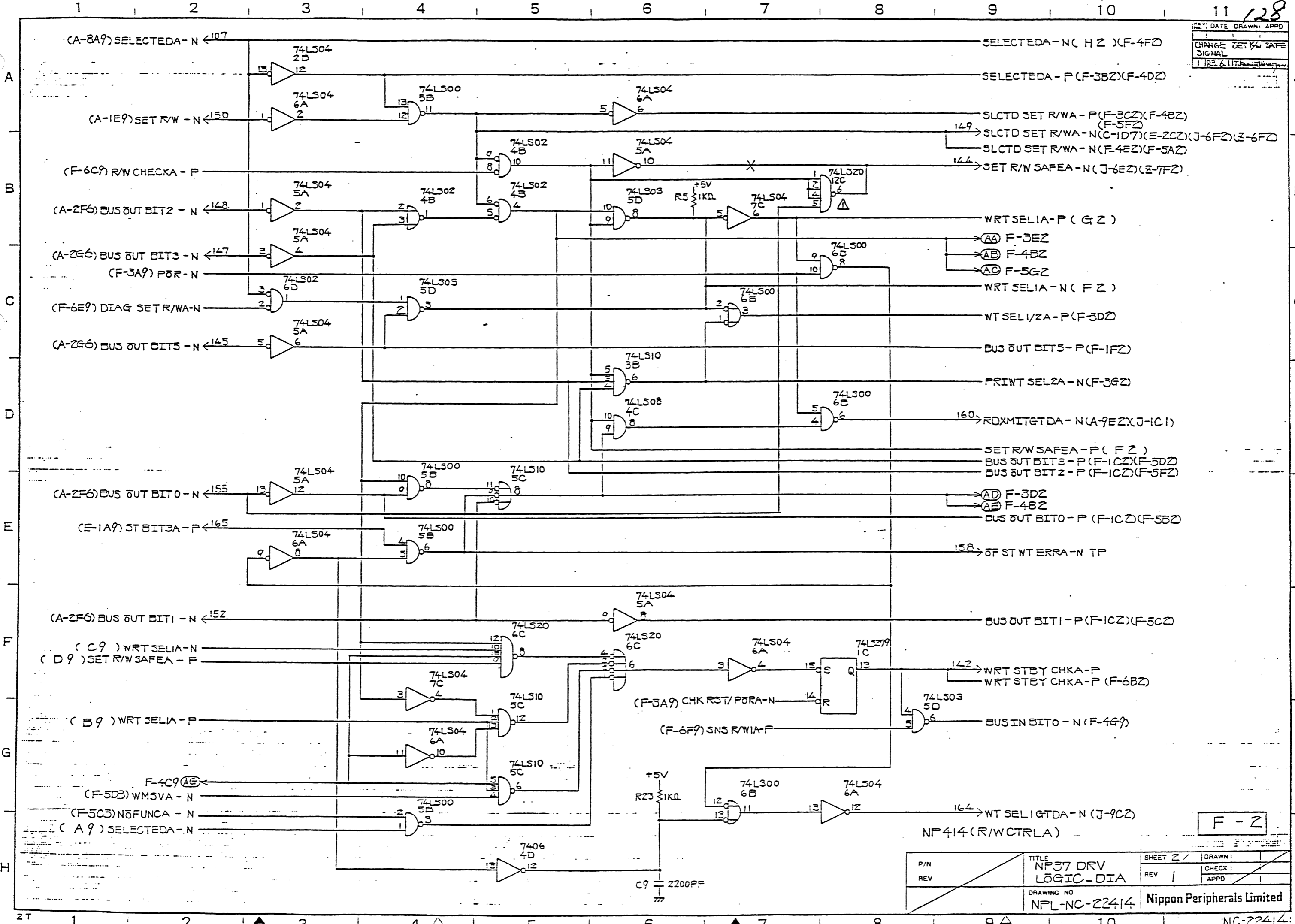
REV	DATE	DRAWN	APPD
SHEET	Rev 0 → 1	FUNCTION	Rev F → G
1 13 6.1 ITK			
SHEET 5 REV 0 → 1			
FUNCTION REV G → H			
Z 13.7.10 ISSUED A 05/11/97			



NP414 (R/WCTRLA)

F-1

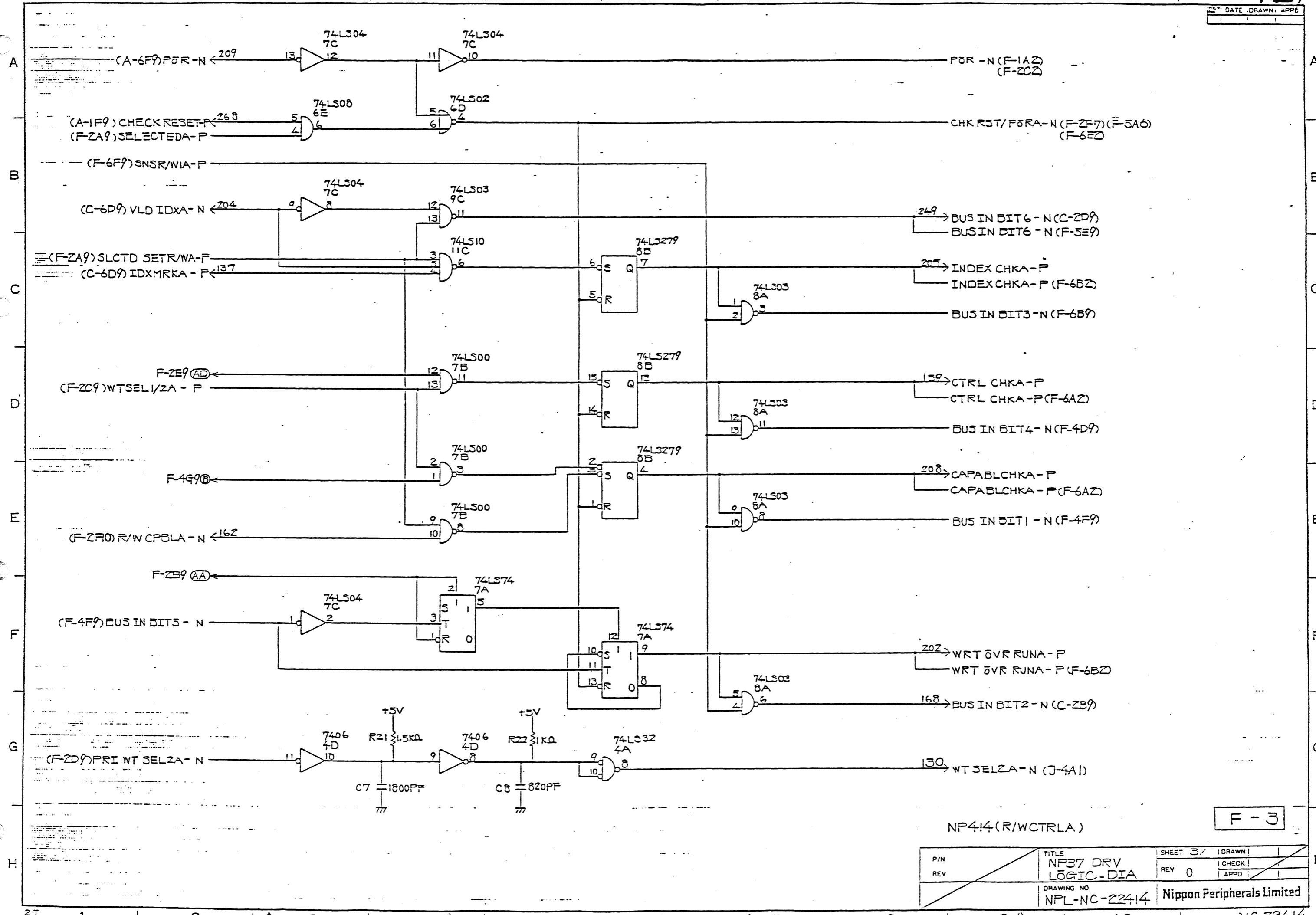
P/N	NP 414	TITLE	NP37 DRV LOGIC-DIA	SHEET	1 / 6	DRAWN	6.1 ITK
REV	H	CHECK	83.6.2 F.K.	REV	2	APPD	83.6.2 K.F.
R/WCTRLA		DRAWING NO NPL-NC-22414		Nippon Peripherals Limited			



F-2

P/N		TITLE		SHEET 2 /		DRAWN	
REV		NP37 DRV LOGIC-DIA		REV 1		CHECK	
		DRAWING NO		APPD			
		NPL-NC-22414				Nippon Peripherals Limited	

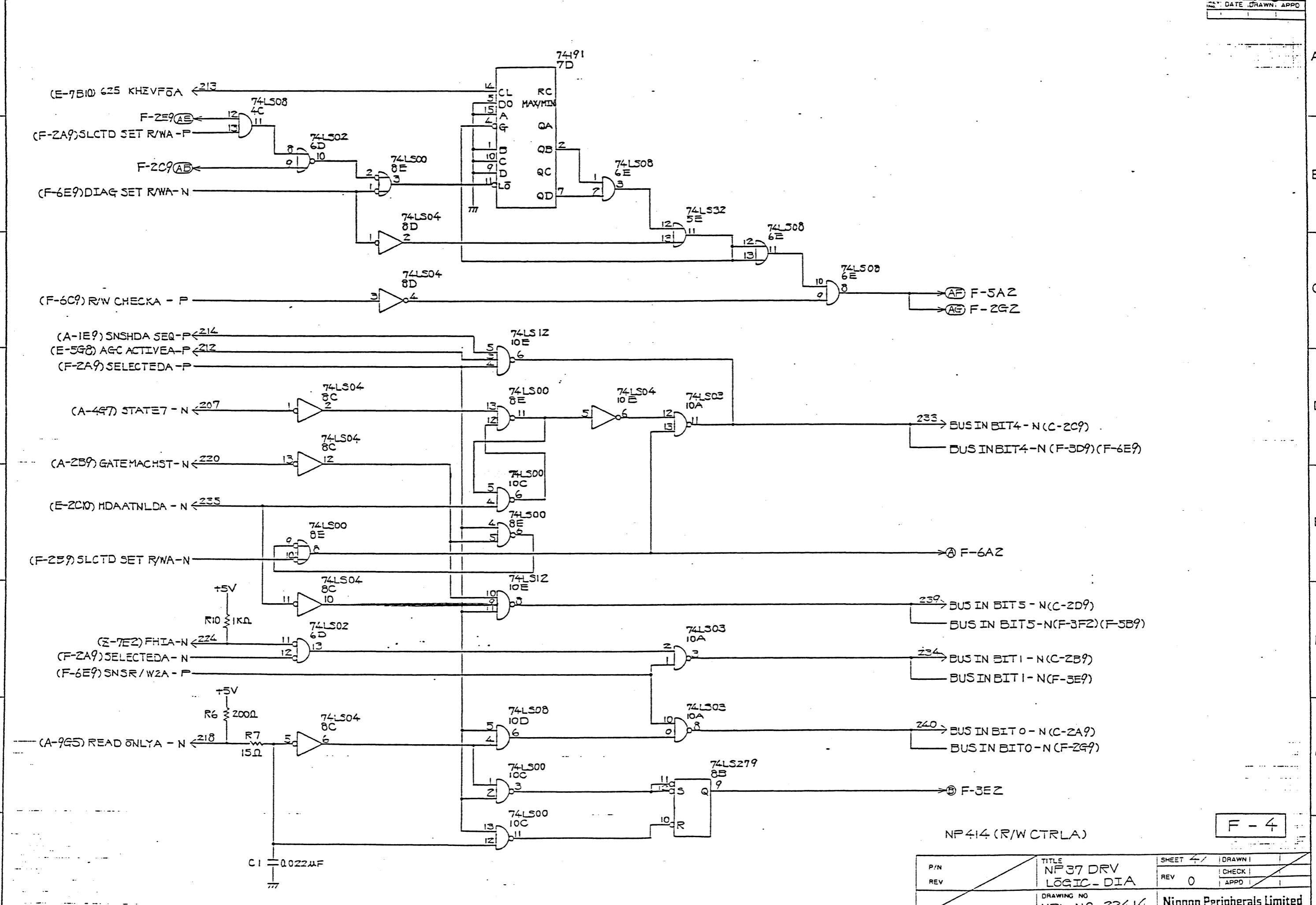
132



NP414 (R/WCTRLA)

F-3

P/N	TITLE	SHEET 3 / 3	DRAWN
REV	NP37 DRV LOGIC-DIA	REV 0	CHECK
DRAWING NO		NPL-NC-22414	
		Nippon Peripherals Limited	

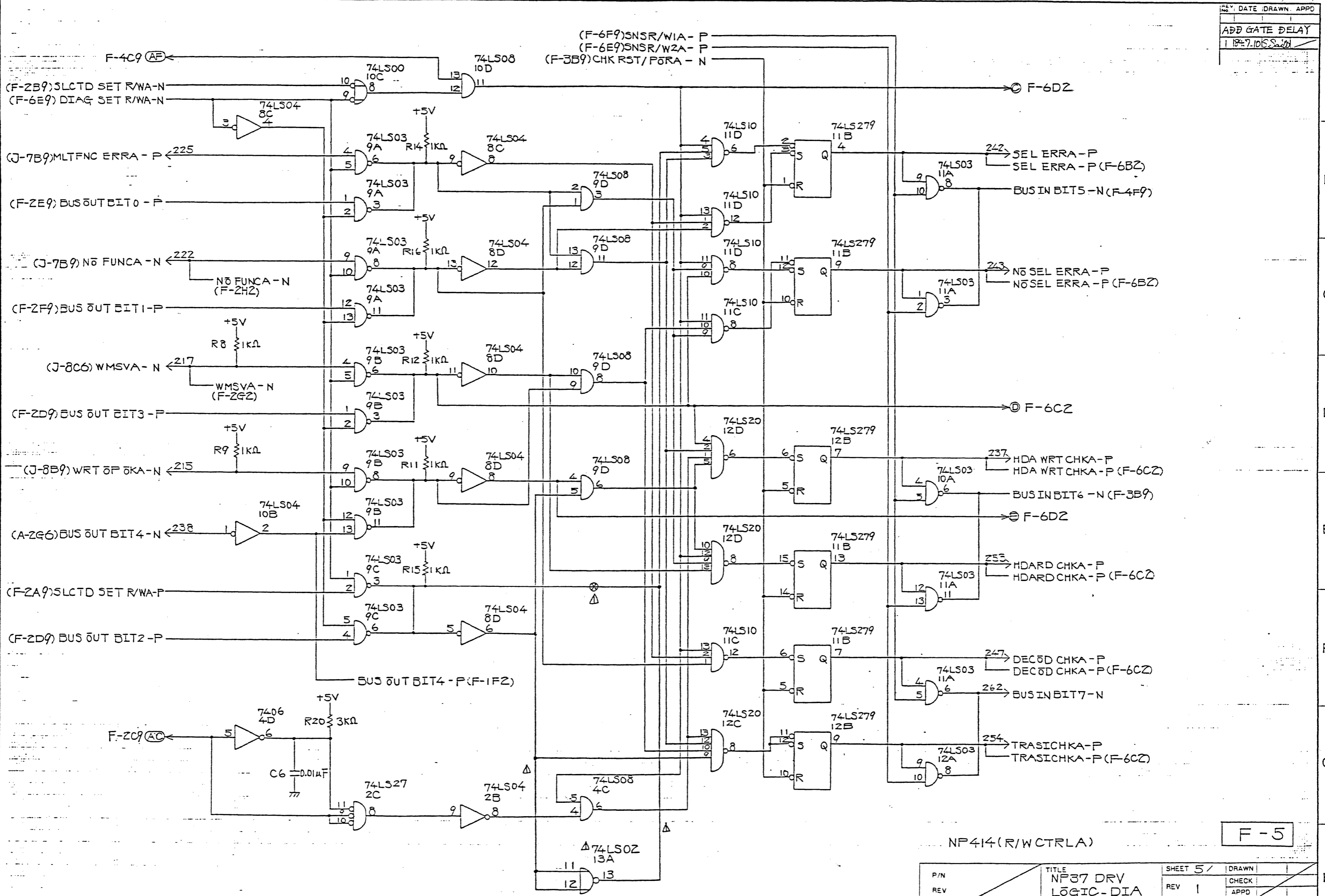


NP414 (R/W CTRLA)

F-4

P/N	TITLE	SHEET 4 /	DRAWN
REV	NF37 DRV LOGIC-DIA	REV 0	CHECK
	DRAWING NO	NPL-NC-22414	APPD
			Nippon Peripherals Limited

REV	DATE	DRAWN	APPD
ADD GATE DELAY			
18.7.106 S. J. J.			

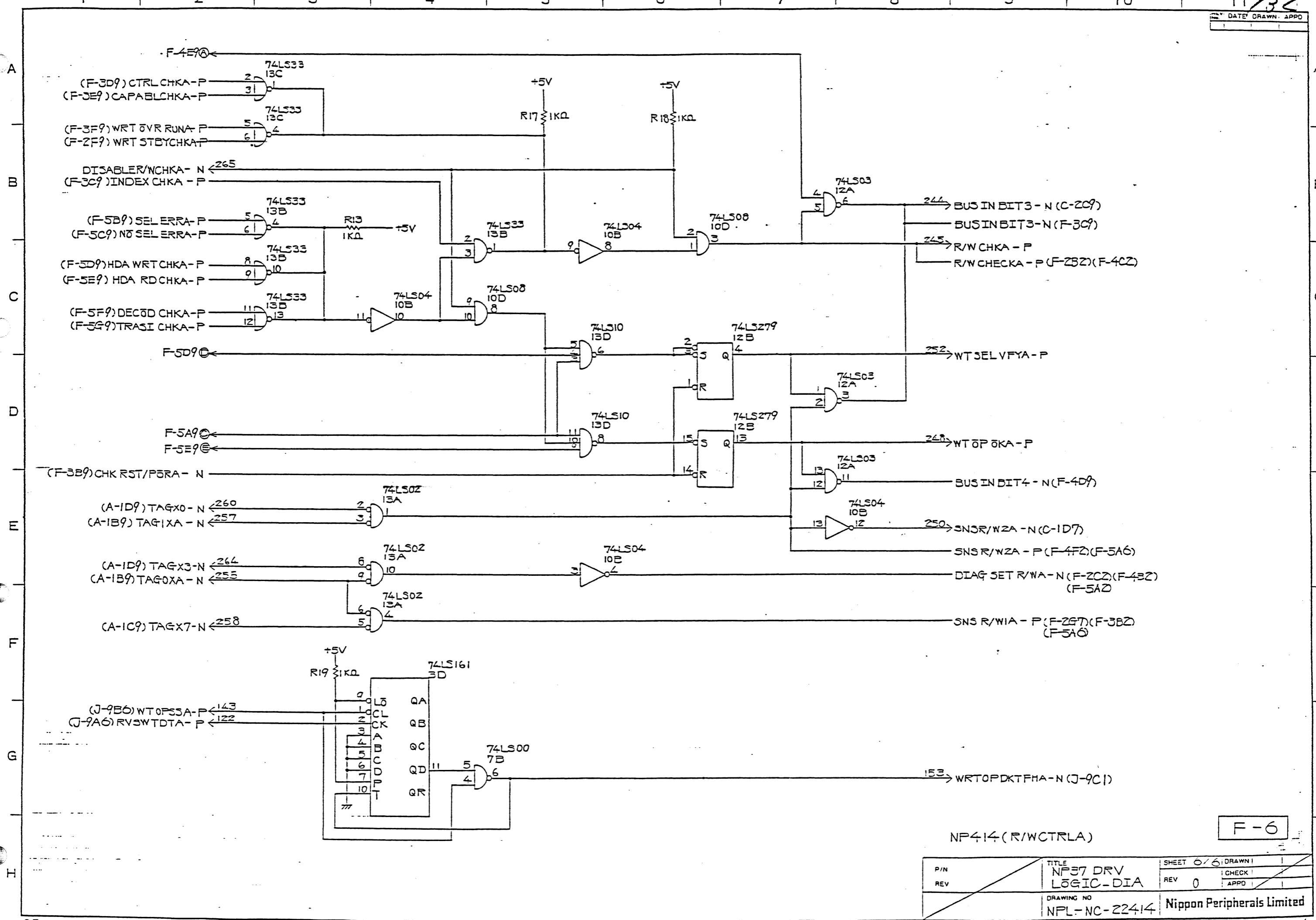


NP414 (R/W CTRLA)

F-5

P/N	TITLE	SHEET 5 /	DRAWN
REV	NF37 DRV LOGIC-DIA	REV 1	CHECK
DRAWING NO NPL-NC-22414		APPD	
		Nippon Peripherals Limited	

NC 22414

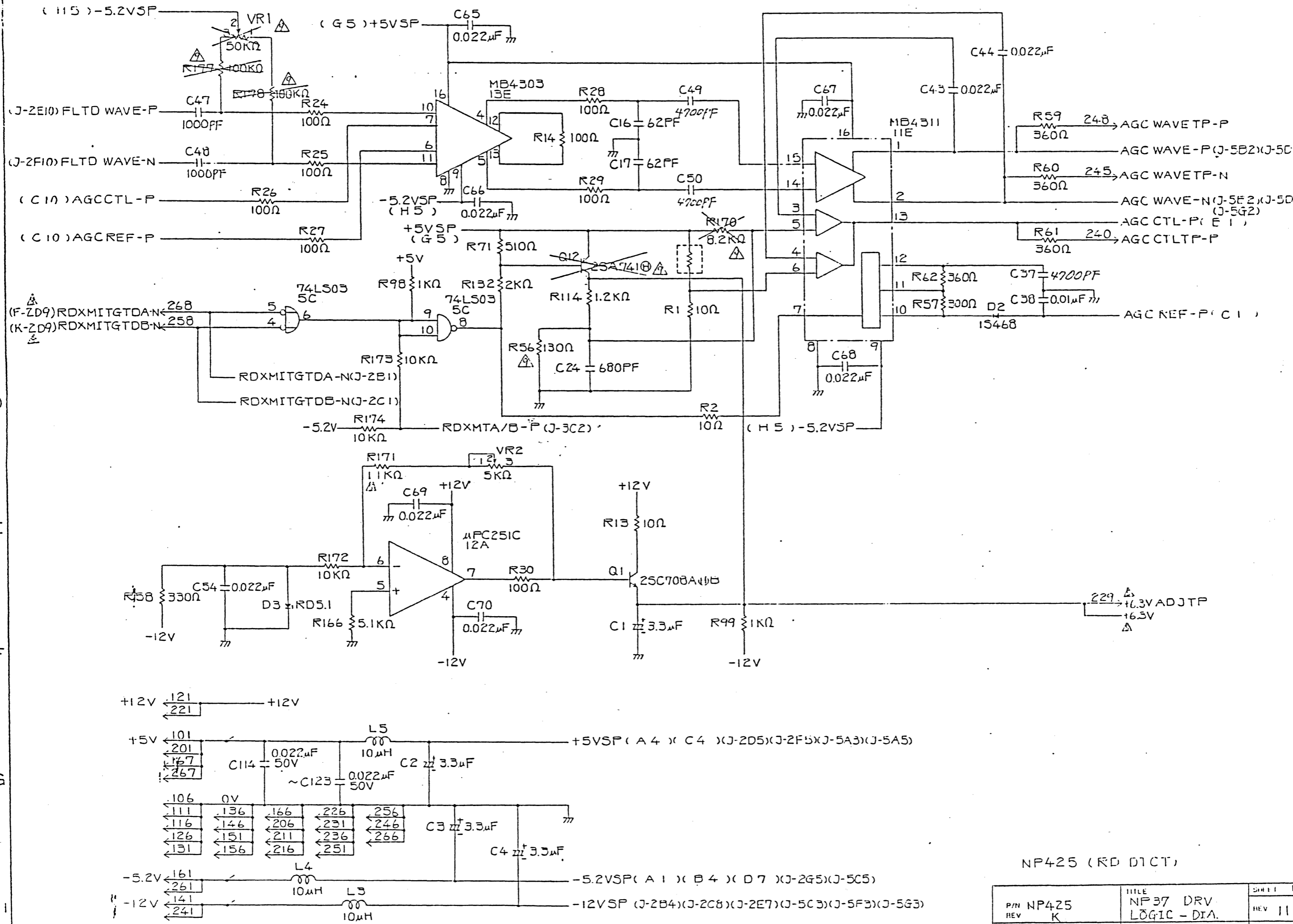


NP414 (R/WCTRLA)

F-6

P/N	TITLE	SHEET	DRAWN
REV	NF37 DRV LOGIC-DIA	6/6	
		REV	CHECK
		0	APPD
DRAWING NO		Nippon Peripherals Limited	
NPL-NC-22414			

136



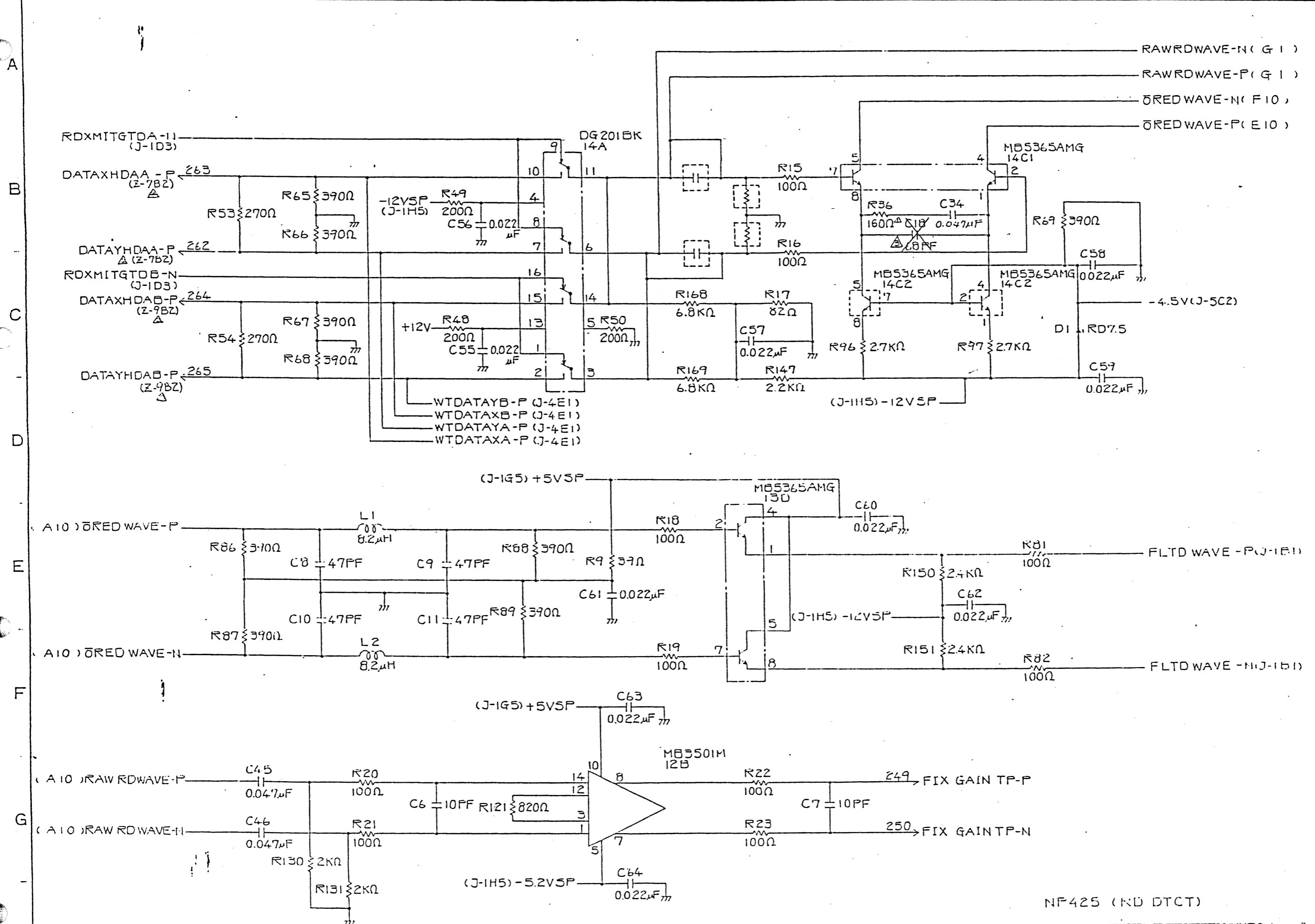
REV 1	11/16/73	J.S.
REV 2	1/10/74	J.S.
REV 3	2/15/74	J.S.
REV 4	3/15/74	J.S.
REV 5	4/15/74	J.S.
REV 6	5/15/74	J.S.
REV 7	6/15/74	J.S.
REV 8	7/15/74	J.S.
REV 9	8/15/74	J.S.
REV 10	9/15/74	J.S.
REV 11	10/15/74	J.S.
REV 12	11/15/74	J.S.
REV 13	12/15/74	J.S.
REV 14	1/15/75	J.S.
REV 15	2/15/75	J.S.
REV 16	3/15/75	J.S.
REV 17	4/15/75	J.S.
REV 18	5/15/75	J.S.
REV 19	6/15/75	J.S.
REV 20	7/15/75	J.S.
REV 21	8/15/75	J.S.
REV 22	9/15/75	J.S.
REV 23	10/15/75	J.S.
REV 24	11/15/75	J.S.
REV 25	12/15/75	J.S.
REV 26	1/15/76	J.S.
REV 27	2/15/76	J.S.
REV 28	3/15/76	J.S.
REV 29	4/15/76	J.S.
REV 30	5/15/76	J.S.
REV 31	6/15/76	J.S.
REV 32	7/15/76	J.S.
REV 33	8/15/76	J.S.
REV 34	9/15/76	J.S.
REV 35	10/15/76	J.S.
REV 36	11/15/76	J.S.
REV 37	12/15/76	J.S.
REV 38	1/15/77	J.S.
REV 39	2/15/77	J.S.
REV 40	3/15/77	J.S.
REV 41	4/15/77	J.S.
REV 42	5/15/77	J.S.
REV 43	6/15/77	J.S.
REV 44	7/15/77	J.S.
REV 45	8/15/77	J.S.
REV 46	9/15/77	J.S.
REV 47	10/15/77	J.S.
REV 48	11/15/77	J.S.
REV 49	12/15/77	J.S.
REV 50	1/15/78	J.S.
REV 51	2/15/78	J.S.
REV 52	3/15/78	J.S.
REV 53	4/15/78	J.S.
REV 54	5/15/78	J.S.
REV 55	6/15/78	J.S.
REV 56	7/15/78	J.S.
REV 57	8/15/78	J.S.
REV 58	9/15/78	J.S.
REV 59	10/15/78	J.S.
REV 60	11/15/78	J.S.
REV 61	12/15/78	J.S.
REV 62	1/15/79	J.S.
REV 63	2/15/79	J.S.
REV 64	3/15/79	J.S.
REV 65	4/15/79	J.S.
REV 66	5/15/79	J.S.
REV 67	6/15/79	J.S.
REV 68	7/15/79	J.S.
REV 69	8/15/79	J.S.
REV 70	9/15/79	J.S.
REV 71	10/15/79	J.S.
REV 72	11/15/79	J.S.
REV 73	12/15/79	J.S.
REV 74	1/15/80	J.S.
REV 75	2/15/80	J.S.
REV 76	3/15/80	J.S.
REV 77	4/15/80	J.S.
REV 78	5/15/80	J.S.
REV 79	6/15/80	J.S.
REV 80	7/15/80	J.S.
REV 81	8/15/80	J.S.
REV 82	9/15/80	J.S.
REV 83	10/15/80	J.S.
REV 84	11/15/80	J.S.
REV 85	12/15/80	J.S.
REV 86	1/15/81	J.S.
REV 87	2/15/81	J.S.
REV 88	3/15/81	J.S.
REV 89	4/15/81	J.S.
REV 90	5/15/81	J.S.
REV 91	6/15/81	J.S.
REV 92	7/15/81	J.S.
REV 93	8/15/81	J.S.
REV 94	9/15/81	J.S.
REV 95	10/15/81	J.S.
REV 96	11/15/81	J.S.
REV 97	12/15/81	J.S.
REV 98	1/15/82	J.S.
REV 99	2/15/82	J.S.
REV 100	3/15/82	J.S.

NP425 (RD DTCT)

J-1

P/N NP425	TITLE NP37 DRV LOGIC - DIA.	SHEET 14	DRAWN S.S.	82.6.9
REV K		REV 11	CHKD F. Aburata	82.6.9
RD DTCT	DRAWING NO NPL-NC-20425	Nippon Peripherals Limited		

DATE	DRAWN	APPD
CORRECTION		
K 31: 10022 → 16022		
1 10.11.85 S.H.		
APC HDA IF		
2 10.11.85 S.H.		
REMOVE C18: 68PF		
3 14.11.85 S.H.		



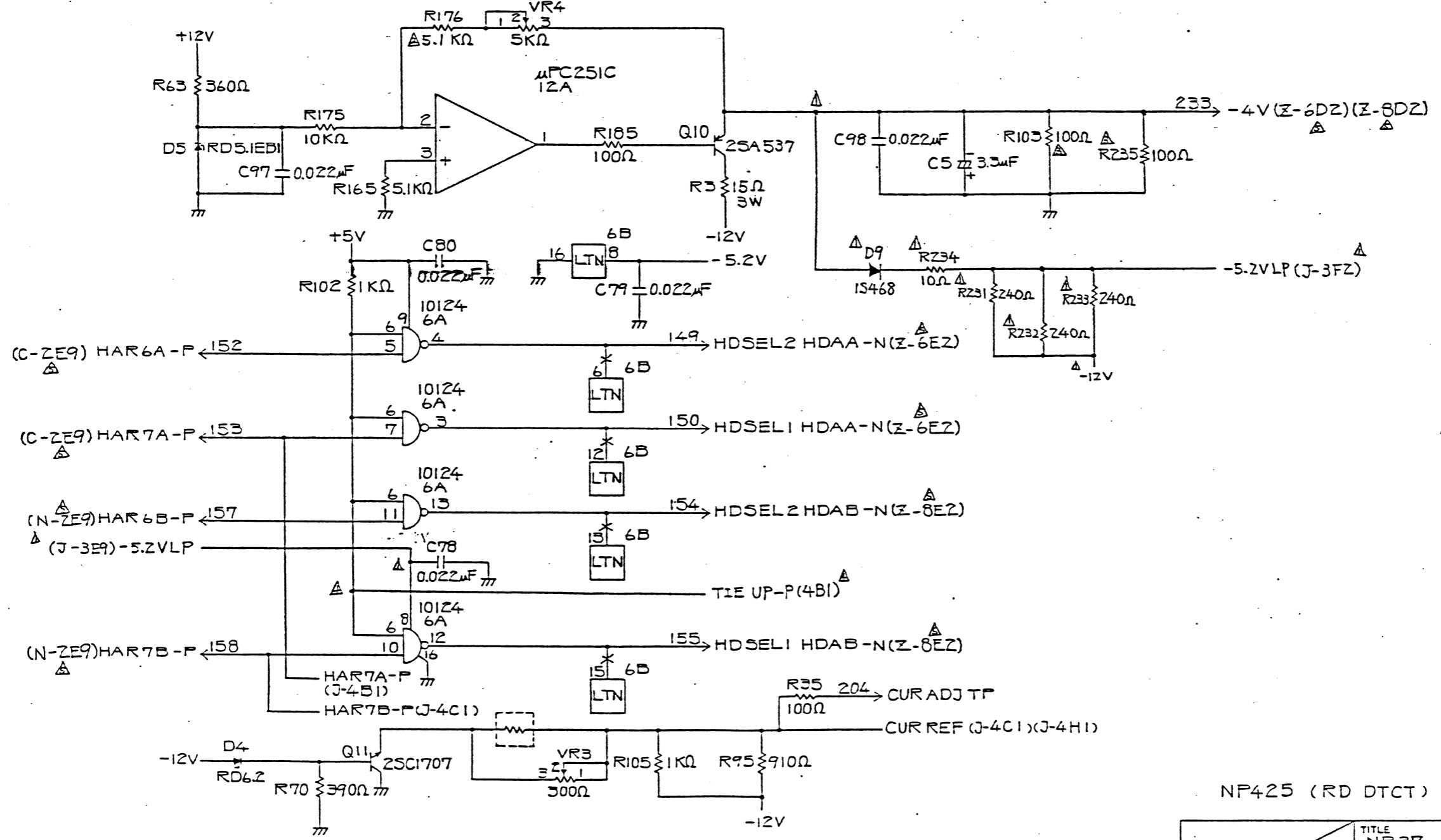
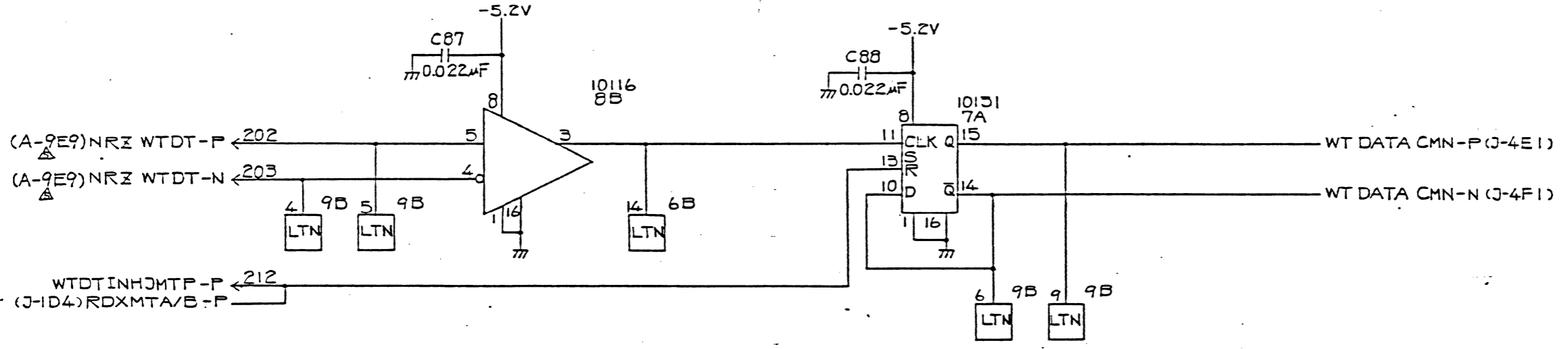
NF425 (NO DTCT)

J-2

P/N	REV	TITLE	SHEET	DRAWN
		NP37 DRV	2	
		LOGIC -DIA	REV	CHECK
			3	APPD
DRAWING NO		Nippon Peripherals Limited		
NPL-NC-20425				

138

DATE	DRAWN	APPD
CHANGE VEE OF 6A		
FROM -4V TO -5.2VLP		
1 R22.61E. Saito		
CORRECTION OF H25 DWG		
R176: 5K Ω \rightarrow 5.1K Ω		
= 142.7.51E. Saito		
R103: 1K Ω \rightarrow 100 Ω		
APP R 235 = 100 Ω		
3 182.7.151E. Saito		
APP: TIE UP-P		
4 182.7.151E. Saito		
APP: 5.2VLP ADDRESS		
5 182.11.11E. Saito		

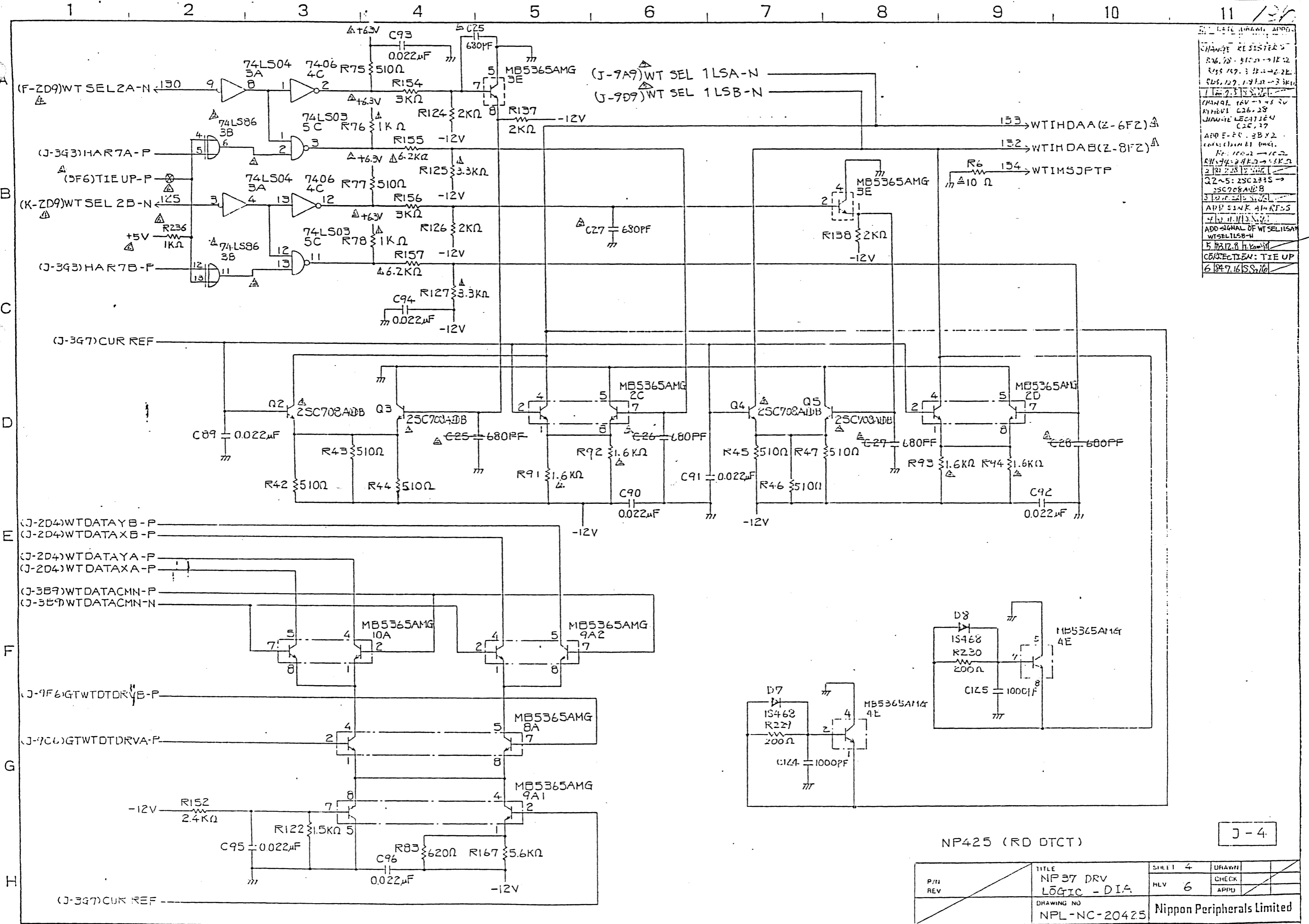


NP425 (RD DTCT)

J-3

P/N	REV	TITLE	SHEET	DRAWN
		NP37 DRV	5/	
		LOGIC DIA.	REV	CHECK
			5.	APPD
DRAWING NO		Nippon Peripherals Limited		
NPL-NC-20425				

139

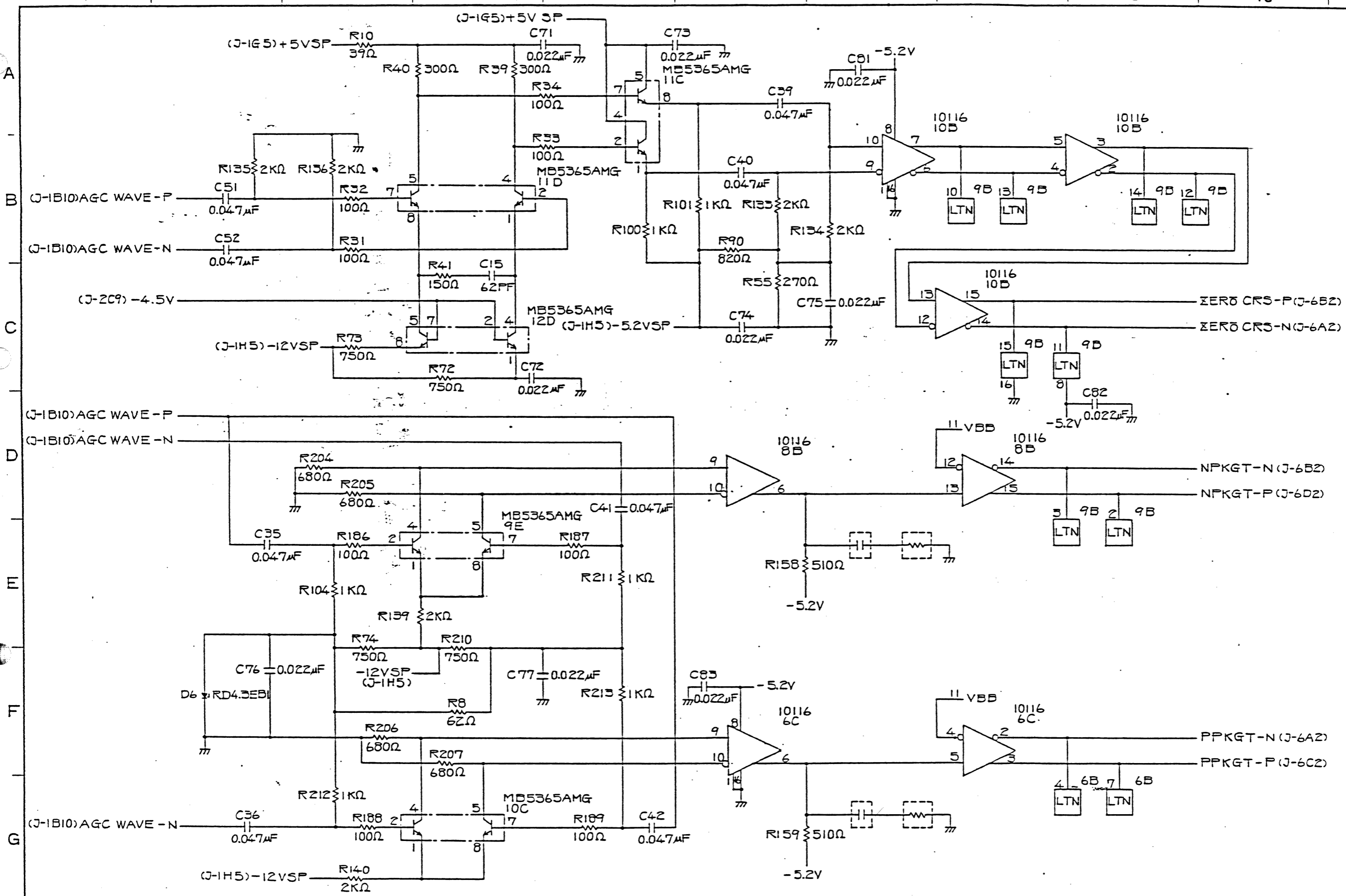


CHANGE RESISTORS
 R76, 78, 510Ω → 1KΩ
 R55, 159, 3.3KΩ → 2KΩ
 R25, 127, 1.5KΩ → 3.3KΩ
 CHANGE CAPS
 C26, 28
 CHANGE RESISTORS
 C26, 28
 ADD SIGNAL OF WTSEL15A
 WTSEL15B-N
 CORRECTION: TIE UP
 6/84/9.16/SS/160

NP425 (RD DTCT)

J-4

P/N REV	TITLE NP37 DRV LOGIC - DIA.	SHEET 4	DRAWN
		HLV 6	CHECK APPD
DRAWING NO NPL-NC-20425		Nippon Peripherals Limited	

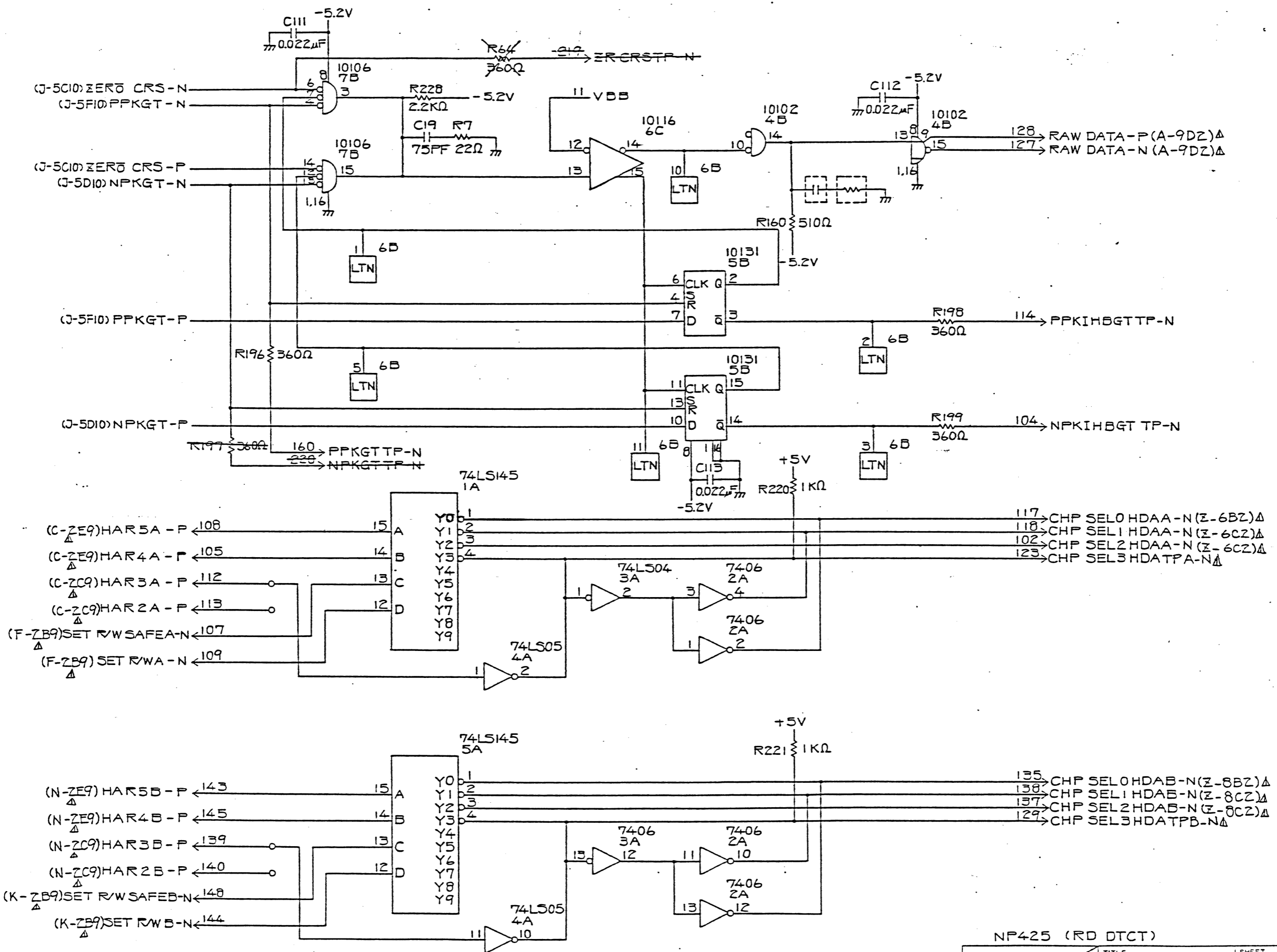


NP425 (RD DTCT)

J-5

P/N REV	TITLE NP37 DRV LOGIC -DIA.	SHEET 5	DRAWN
	DRAWING NO NPL-NC-20425	REV 0	CHECK APPJ
Nippon Peripherals Limited			

DATE	DRAWN	APPD
APPD SINK ADDRESS		
18.11.16.5.2		

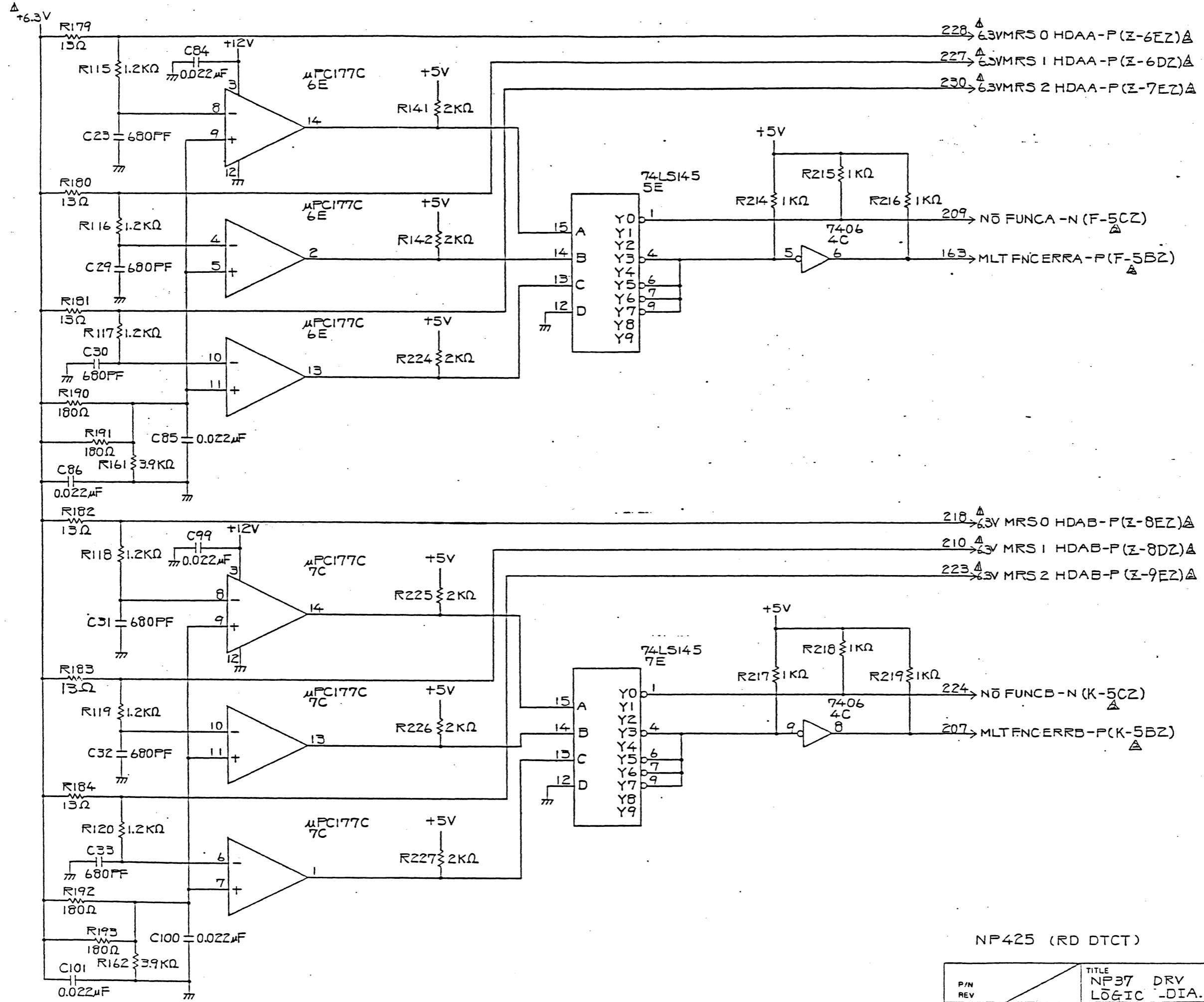


J-6

NP425 (RD DTCT)		TITLE	SHEET 6/	DRAWN
P/N	REV	NP37 DRY LOGIC -DIA.	REV 1	CHECK
DRAWING NO		Nippon Peripherals Limited		
NPL-NC-20425				

142

DATE	DRAWN	APPD
CHANGE: 6V → 6.3V		
1 12.12.15.50		
APP SWK ADDRESS		
2 12.11.15.50		



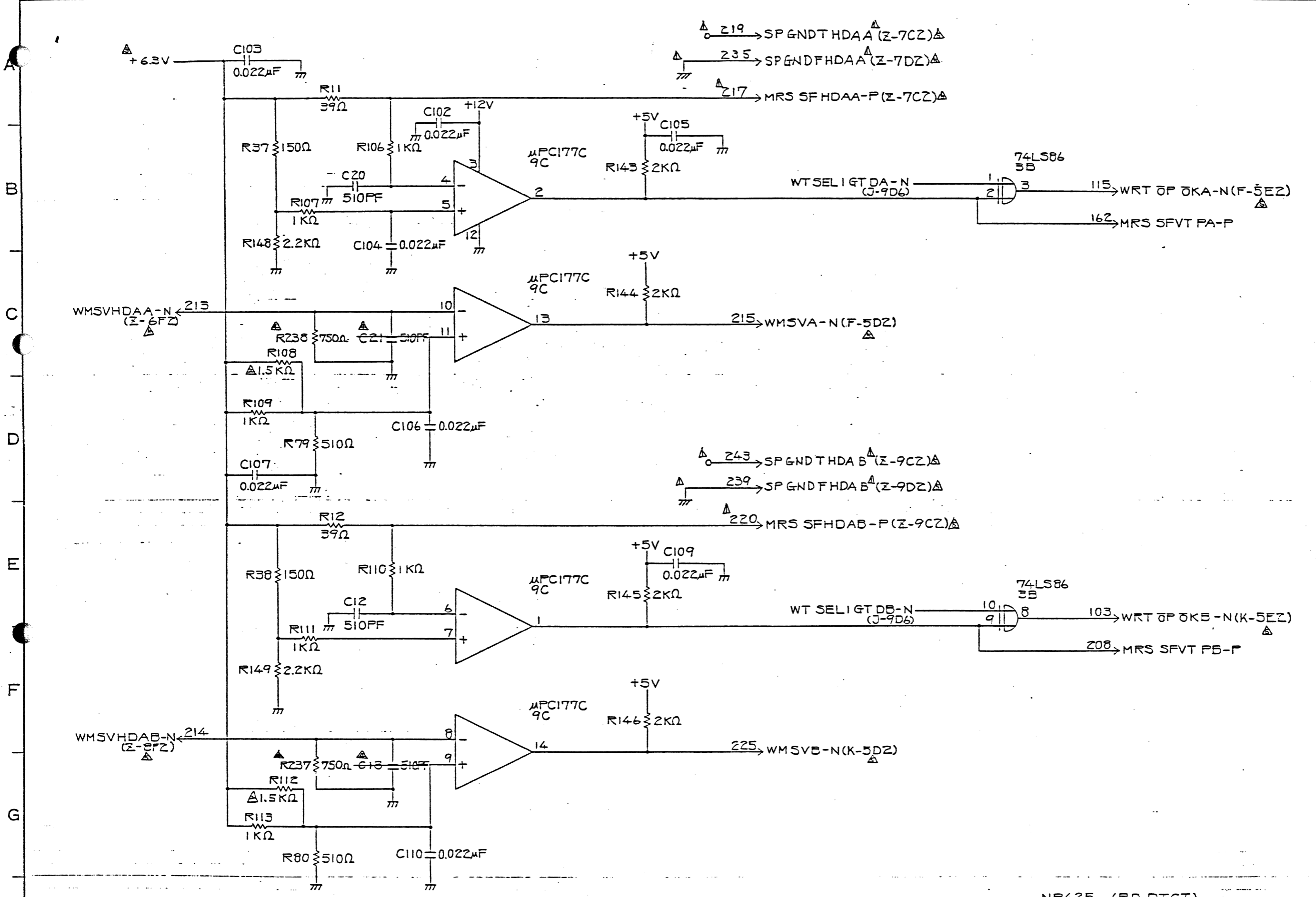
NP425 (RD DTCT)

J-7

P/N REV	TITLE NP37 DRV LOGIC -DIA.	SHEET 7/	DRAWN
	DRAWING NO NPL-NC-20425	REV 2	CHECK APPD
Nippon Peripherals Limited			

143

DATE: DRAWN: APPD:
 CHANGE OUTPUT
 P/N OF MRS
 SFHDA LINE
 165 → 217
 205 → 220
 ADD SP GND ON
 PIN 219, 235, 243
 239
 1 182.4.15. Saiki
 CHANGE RESISTORS
 R108, 112 = 1KΩ → 1.5KΩ
 2 182.7.515. Saiki
 CHANGE: +6V → +6.3V
 3 182.7.515. Saiki
 REMOVE: C15, C16: STOPF.
 ADD: R237, 238: 250Ω
 4 182.7.515. Saiki
 ADD SINK ADDRESS
 5 182.11.15. Saiki

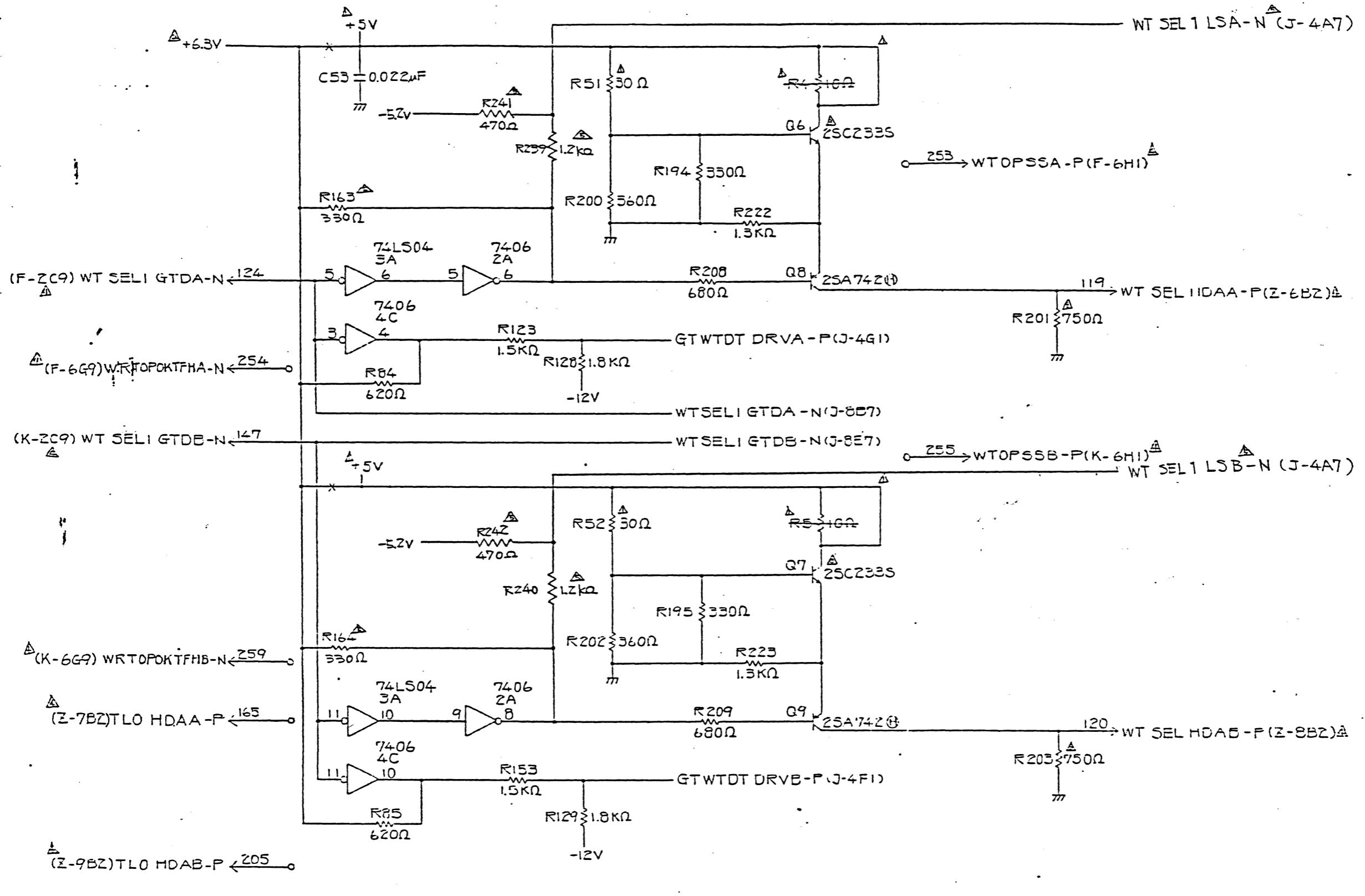


NF425 (RD DTCT)

J-8

P/N REV	TITLE NF37 DRV LOGIC -DIA.	SHEET 8	DRAWN
	DRAWING NO NFL-NC-20425	REV 5	CHECK APPO
Nippon Peripherals Limited			

DATE: _____ DRAWN: _____
 REMOVE R4, 5
 CHANGE R51, 52
 FROM 100Ω TO 300Ω
 CHANGE VCC OF WT
 SEL1 SELT SOURCE
 FROM 1.8V TO 1.5V
 CHANGE: 1.6V → 1.5V
 CHANGE: 1.2K → 1.5K
 CHANGE
 Q6, 7: 2SC2335
 2SC2335
 R194: 330Ω → 300Ω
 R222: 1.3K → 1.5K
 APP SINK ADDRESS
 11: 1111 1111
 CHANGE R163, 164
 330Ω → 300Ω
 MOUNT R239, 240
 1.2K
 R241, 242
 470Ω
 ADD SIGNAL WTSEL1LSA-N
 WTSEL1LSB-N
 5.0V



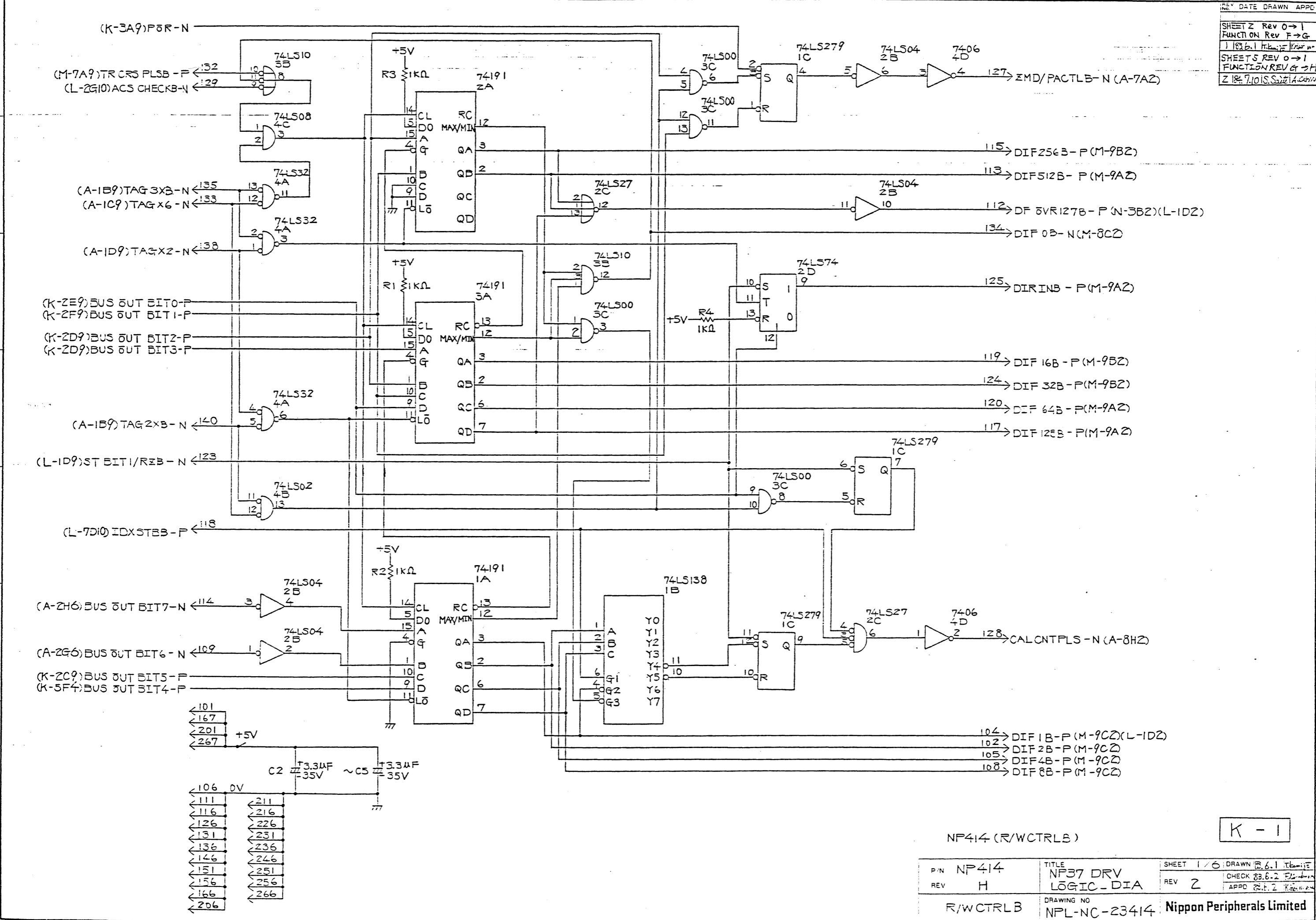
NP425 (RD DTCT)

J-9

P/N REV	TITLE NF37 DRV LOGIC -DIA.	SHEET 9.9	DRAWN
	DRAWING NO NPL-NC-20425	REV 5	CHECK APTD
Nippon Peripherals Limited			

145

REV	DATE	DRAWN	APPD
SHEET 2	Rev 0 → 1	FUNCTION	Rev F → G
1	18.1	18.1	18.1
SHEETS	REV 0 → 1	FUNCTION	REV G → H
2	18.1	18.1	18.1



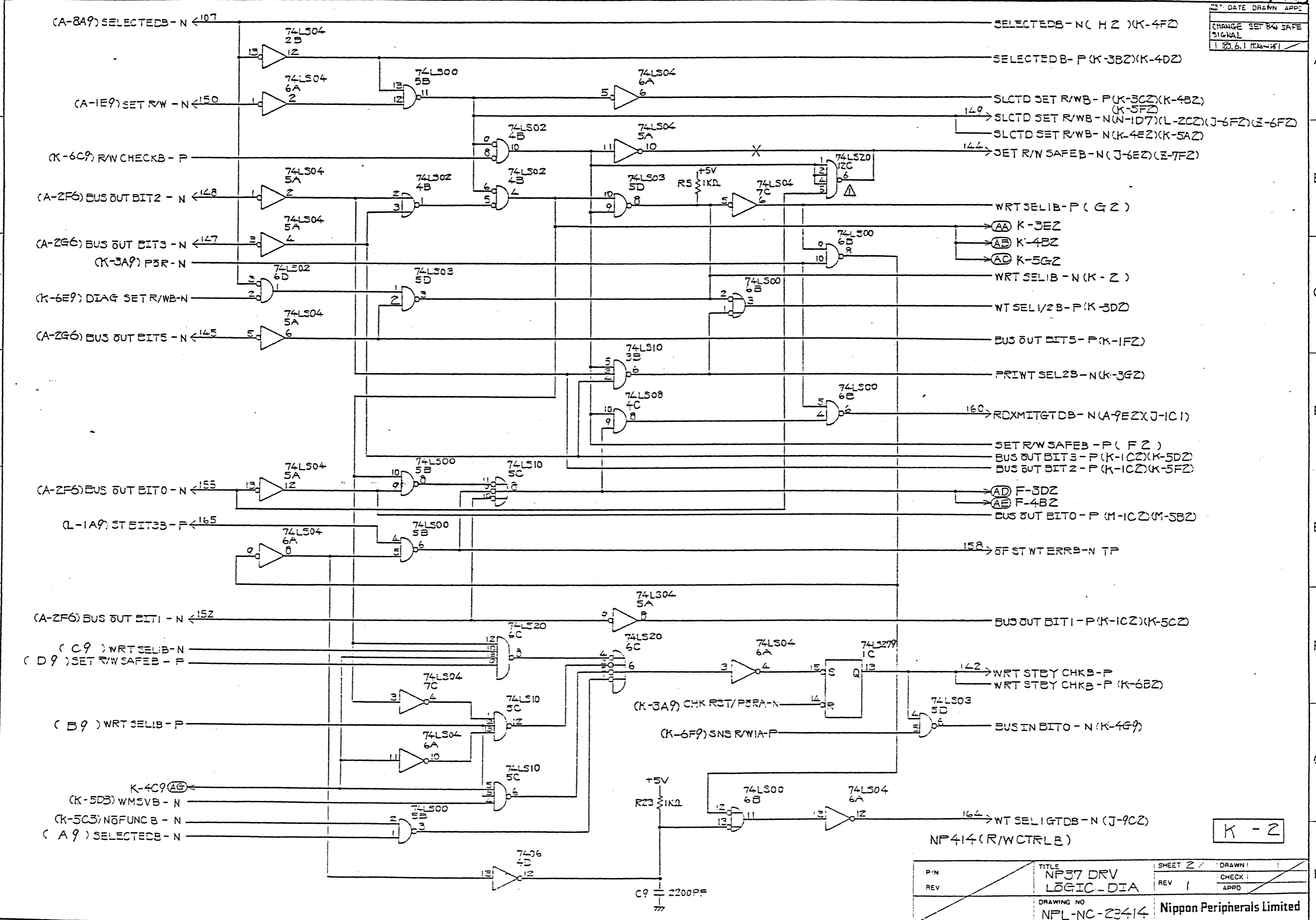
1148

NP414 (R/WCTRLB)

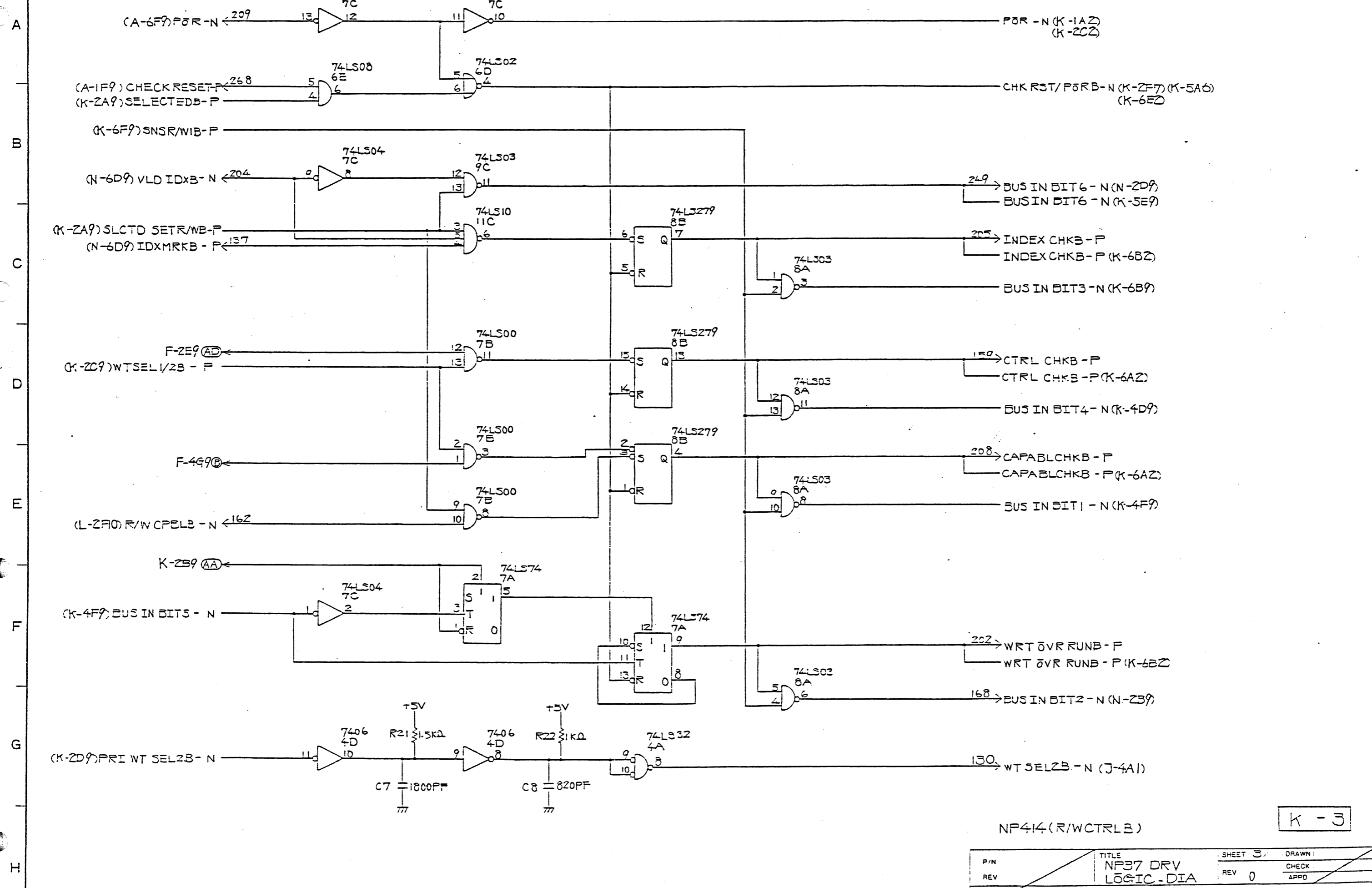
K-1

P/N	NP414	TITLE	NP37 DRV LOGIC-DIA	SHEET	1/6	DRAWN	6.1	TEAM
REV	H	REV	2	CHECK	83.6.2	APPD	83.6.2	TEAM
R/WCTRLB		DRAWING NO		NPL-NC-23414		Nippon Peripherals Limited		

REV. DATE DRAWN APPE
CHANGE SET R/W SAFE SIGNAL
1 23.6.1 (K-2)



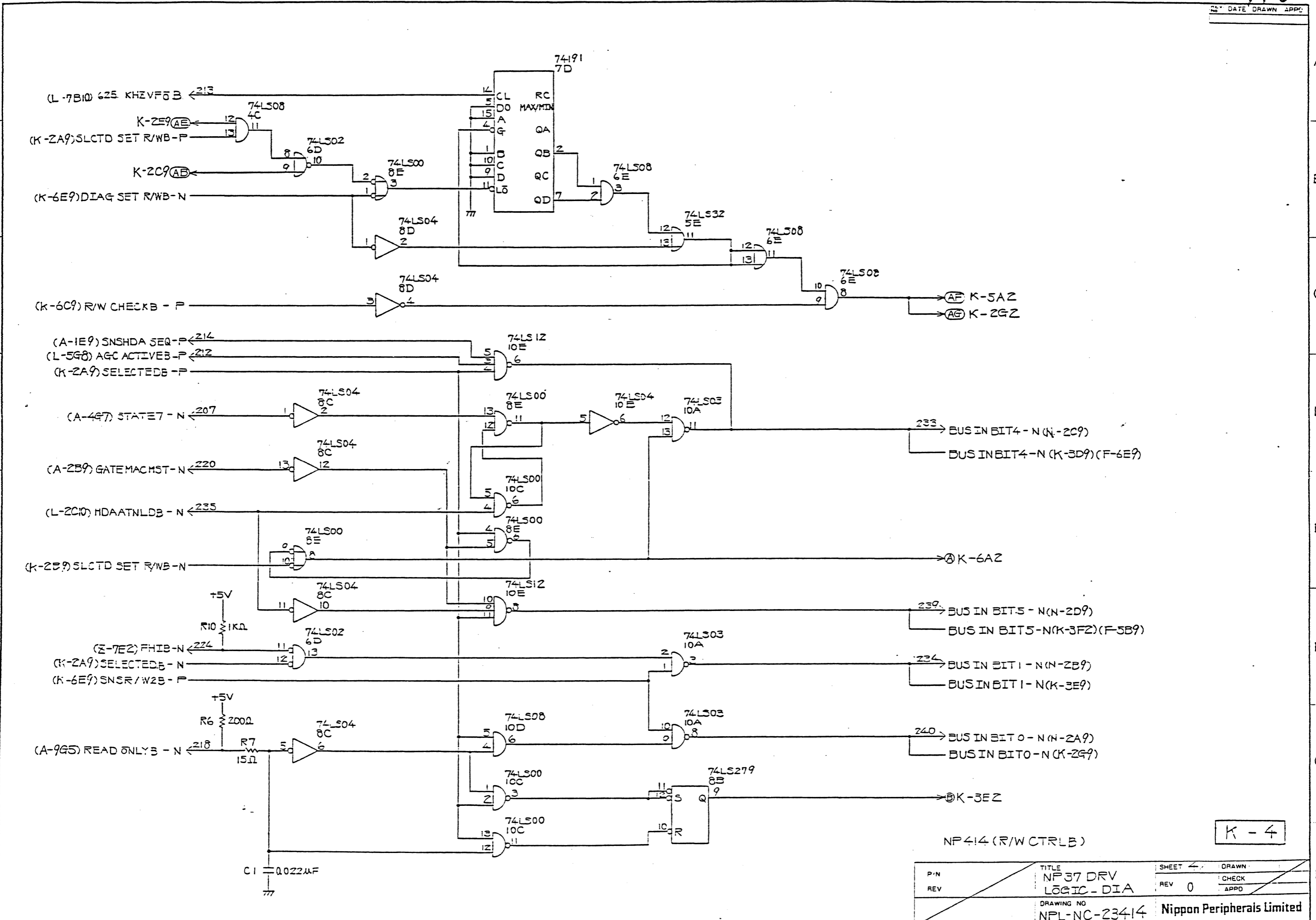
P/N	TITLE	SHEET 2 /	DRAWN
REV	NP37 DRV LOGIC-DIA	REV 1	CHECK I
	DRAWING NO		APPD
	NPL-NC-23414	Nippon Peripherals Limited	



NP414 (R/WCTRLB)

K-3

P/N	TITLE	SHEET 3	DRAWN
REV	NF37 DRV LOGIC-DIA	REV 0	CHECK
DRAWING NO		APPD	
NPL-NC-23414		Nippon Peripherals Limited	

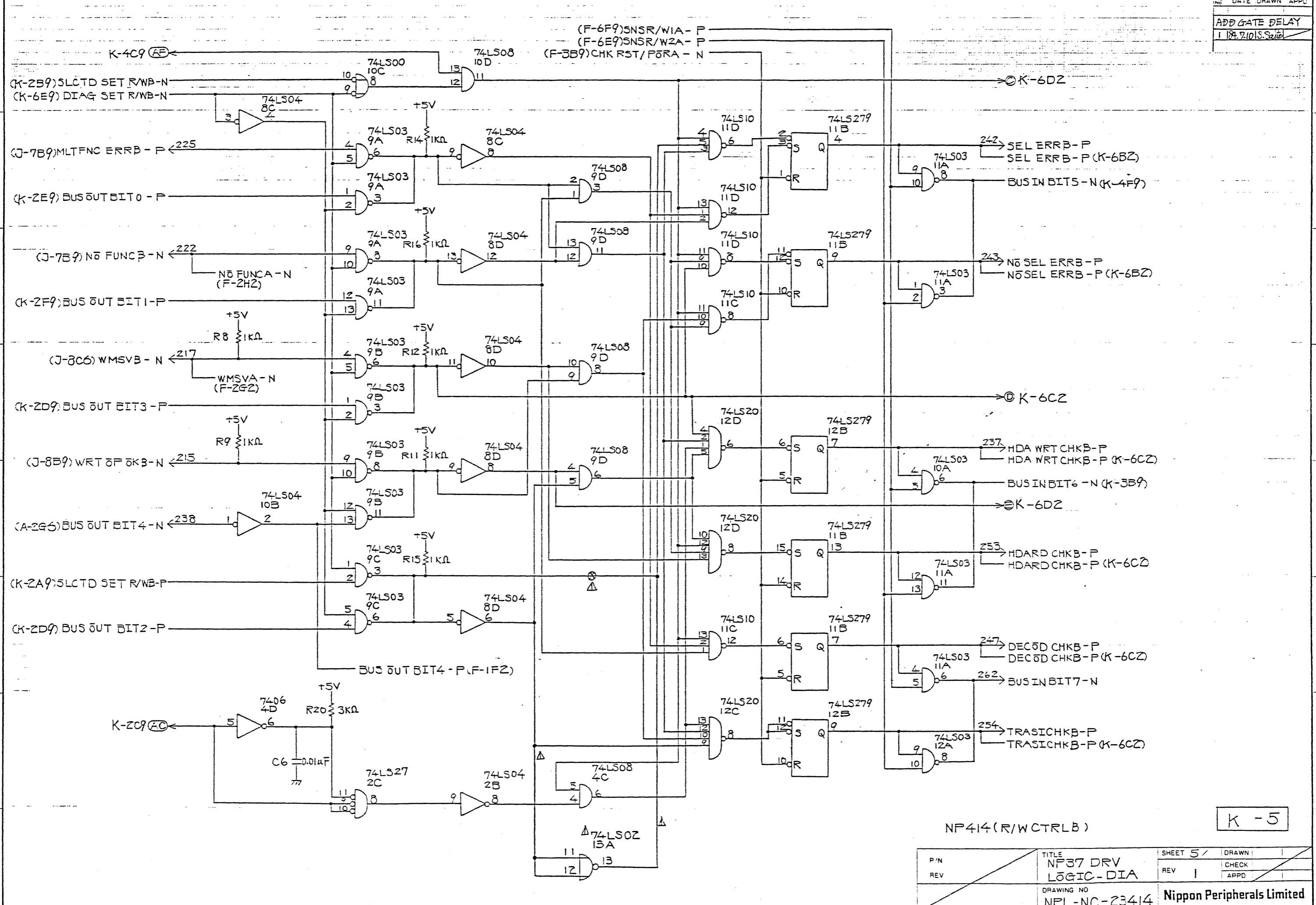


K-4

NP414 (R/W CTRL B)

P/N	TITLE	SHEET	DRAWN
REV	NF37 DRV LOGIC - DIA	REV 0	CHECK
DRAWING NO		APPD	
NPL-NC-23414		Nippon Peripherals Limited	

REV	DATE	DRAWN	APPD
ADD GATE DELAY			
1 17.10.15. Saito			

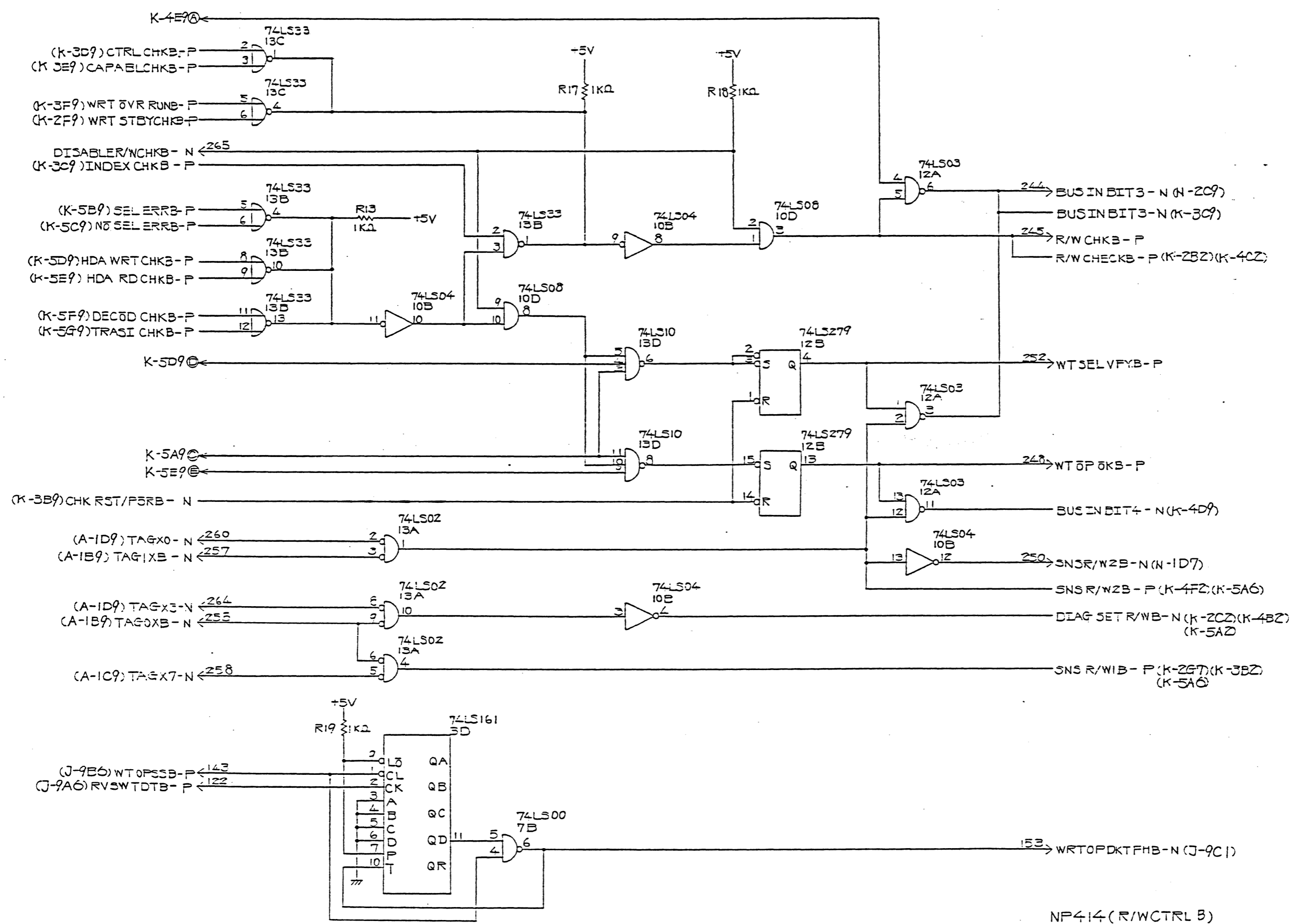


K-5

NP414 (R/W CTRL B)

P/N	TITLE	SHEET 5 /	DRAWN
REV	NP37 DRV LOGIC-DIA	REV 1	CHECK
DRAWING NO		APPD	
NPL-NC-23414		Nippon Peripherals Limited	

150



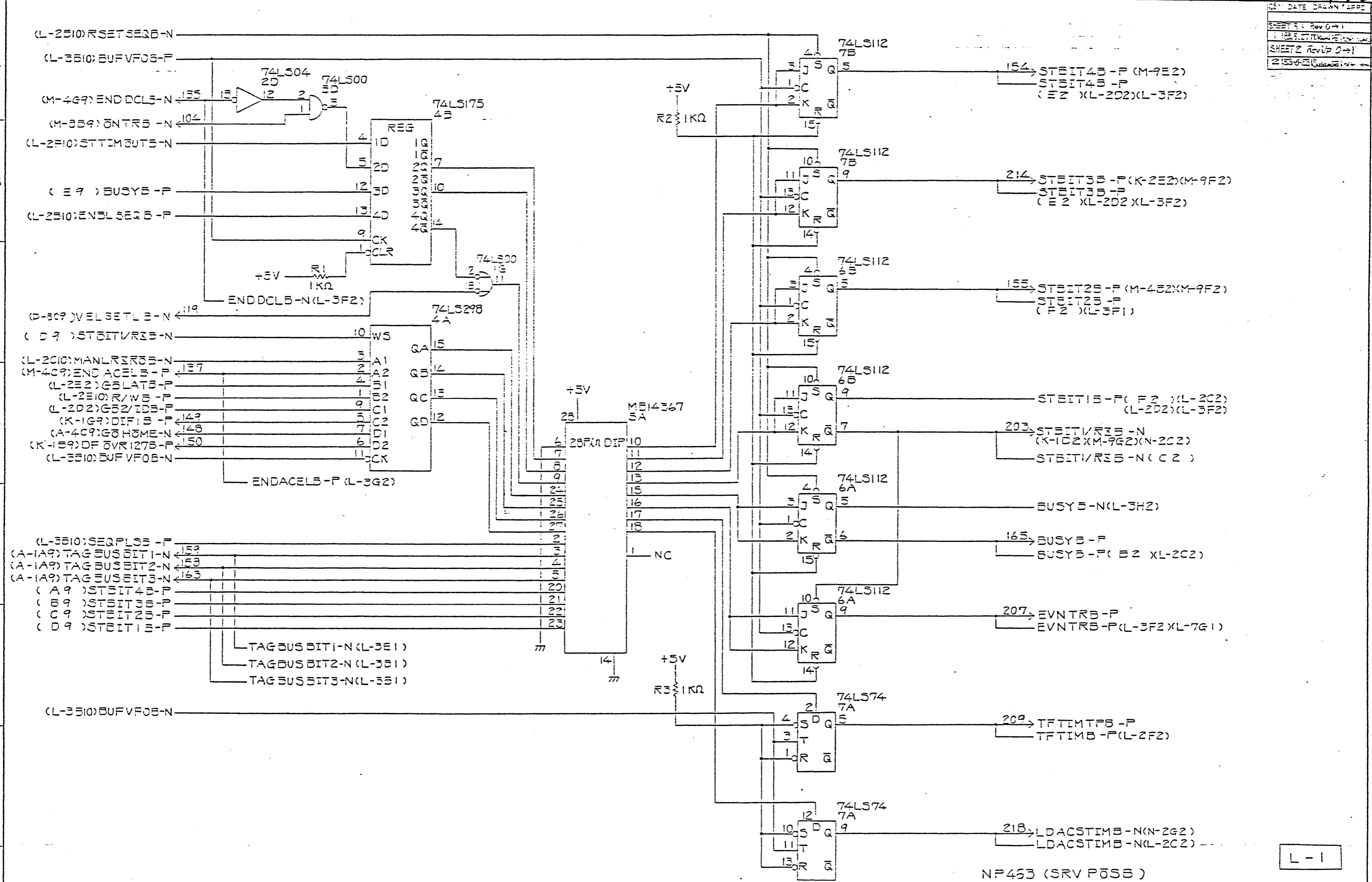
NP414 (R/WCTRL B)

K-6

P/N	TITLE	SHEET 6/6	DRAWN
REV	NP37 DRV LOGIC-DIA	REV 0	CHECK APPR
DRAWING NO NPL-NC-23414		Nippon Peripherals Limited	

151

DATE	DRAWN	APPD
SHEET 5	Rev 0-1	
SHEET 2	Rev 0-1	



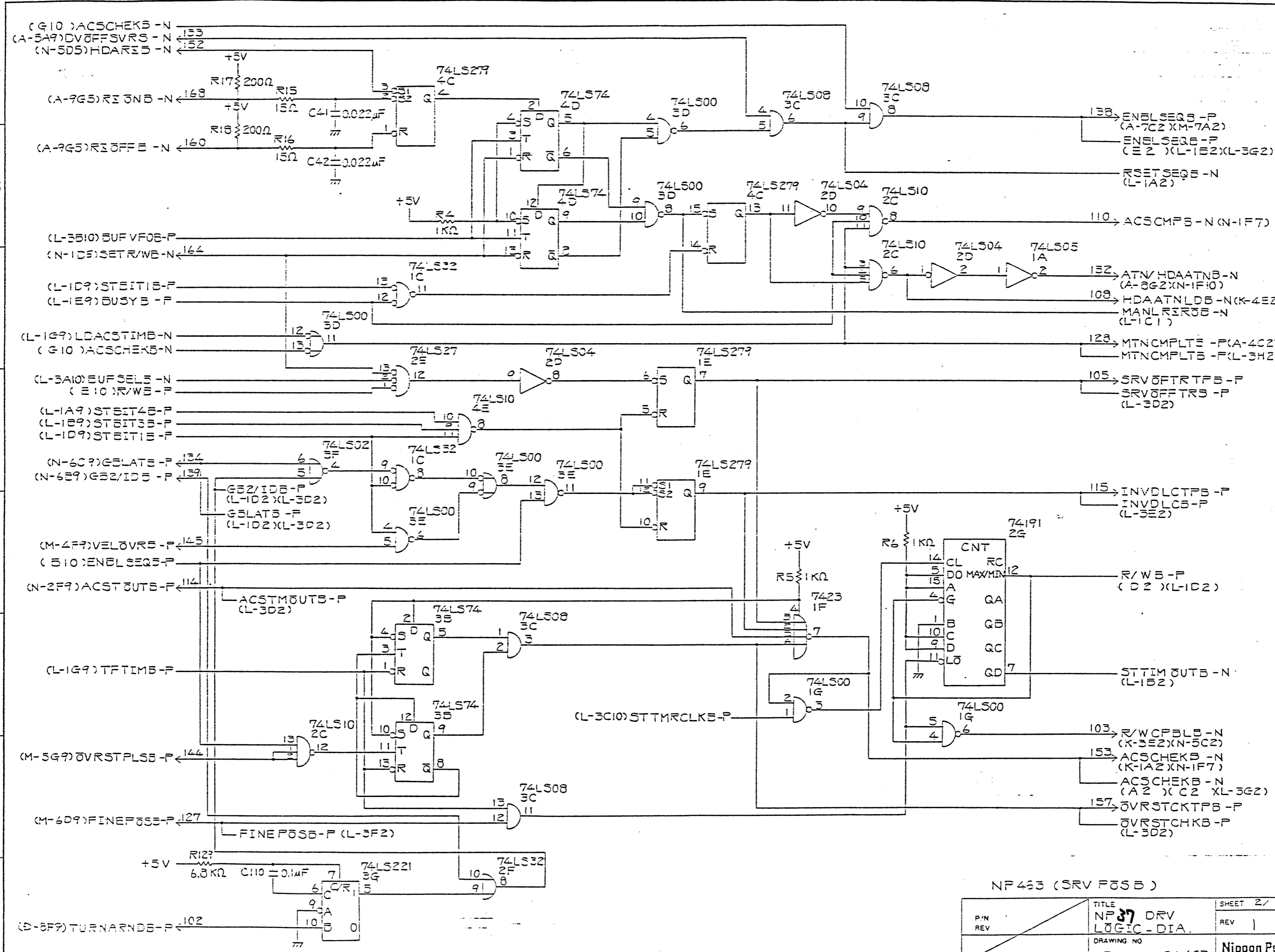
注: 指定なき抵抗はすべて1/2Wとする。

L-1

NP453 (SRV P05B)		SHEET 5 of 10 DRAWN: k... 93.5.16	
P/N	REV	TITLE	CHECK
NP 453	B	NP 37 DRV LOGIC DIA.	93.5.16
SRV P05B		DRAWING NO	APPD
		NPL-NC-21463	
		Nippon Peripherals Limited	

152

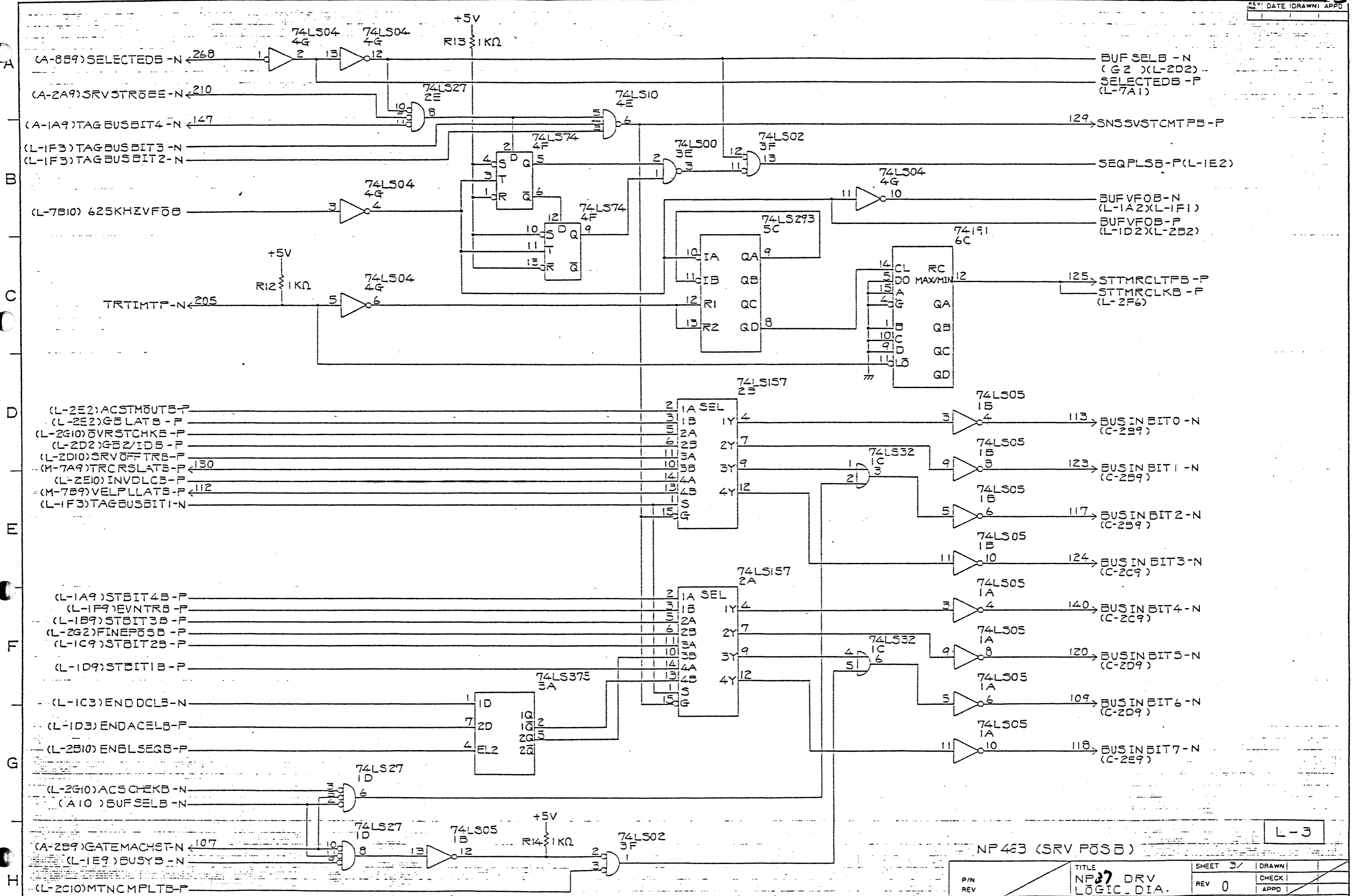
DATE DRAWN	APPD
23 7491	
Reset 6 → 5H	
1 183-8-23	



L-2

NP463 (SRV F05B)

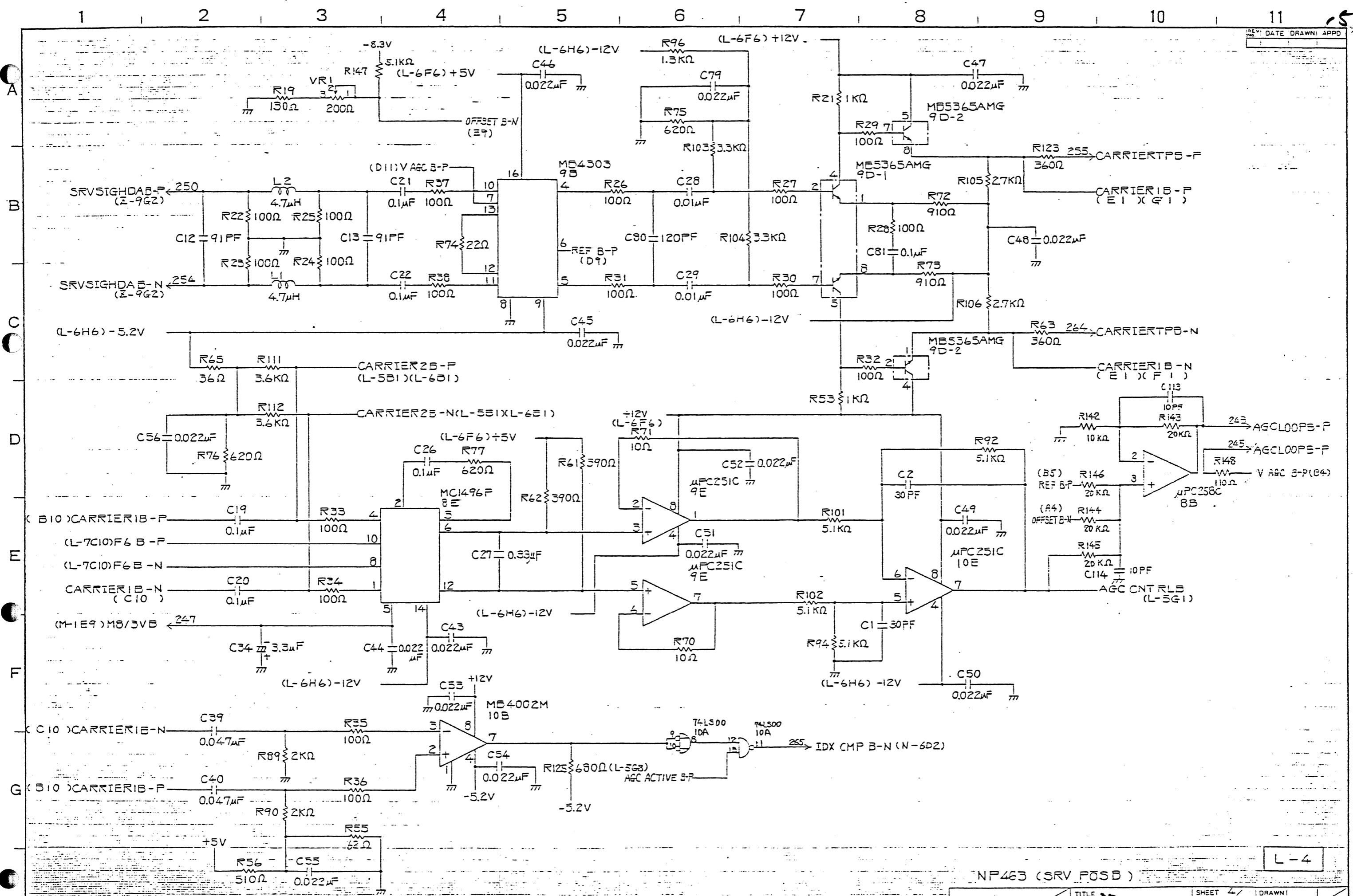
P/N REV	TITLE NP 37 DRV LOGIC-DIA.	SHEET 2/	DRAWN
		REV 1	CHECK
DRAWING NO NPL-NC-21463		Nippon Peripherals Limited	



NP 463 (SRV POSB)

L-3

P/N REV	TITLE NP 463 DRV LOGIC DIA.	SHEET 3/	DRAWN
	DRAWING NO NPL-NC-21463	REV 0	CHECK APPD
Nippon Peripherals Limited			

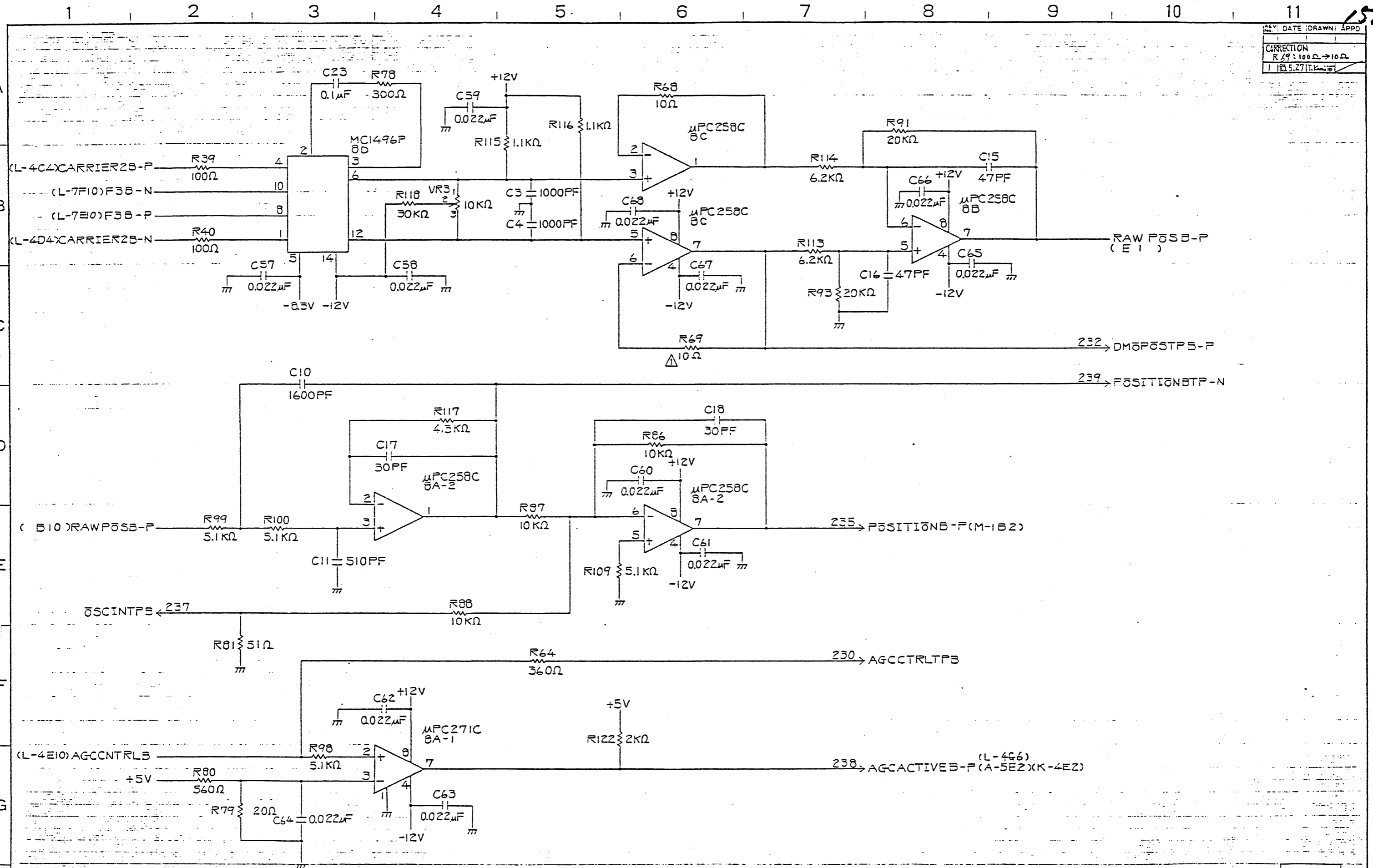


L-4

NF463 (SRV F05B)

P/N REV	TITLE NF37 DRV LOGIC-DIA.	SHEET 4/	DRAWN
	DRAWING NO NPL-NC-21463	REV 0	CHECK APPD
Nippon Peripherals Limited			

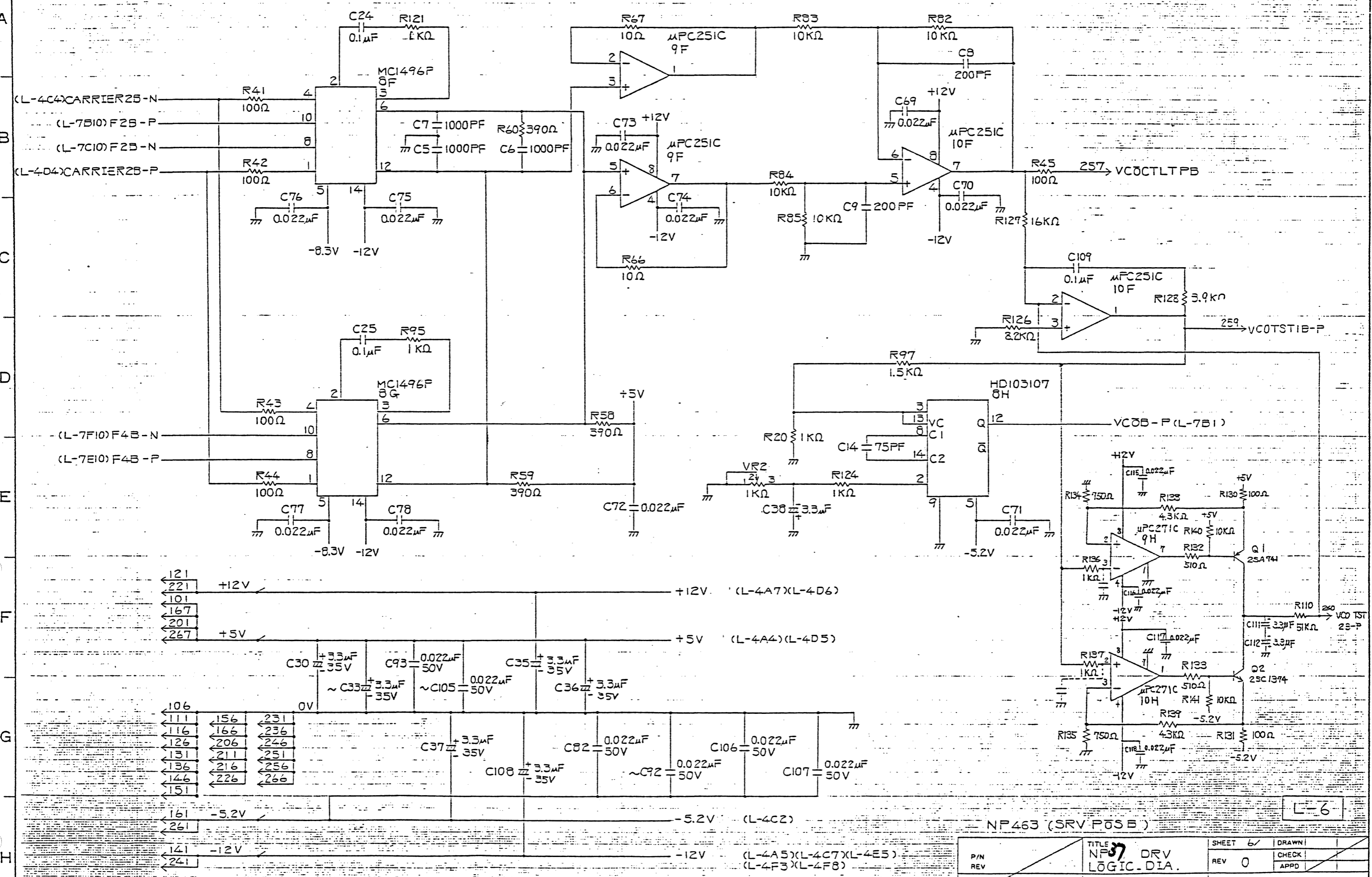
REV.	DATE	DRAWN	APPD
CORRECTION			
R19: 100Ω → 10Ω			
I 18.5.27.12			



L-5

NP463 (SRV POSB)

P/N REV	TITLE NP37 DRV LOGIC DIA.	SHEET 5/ REV 1	DRAWN CHECK APPD
	DRAWING NO NPL-NC-21463	Nippon Peripherals Limited	

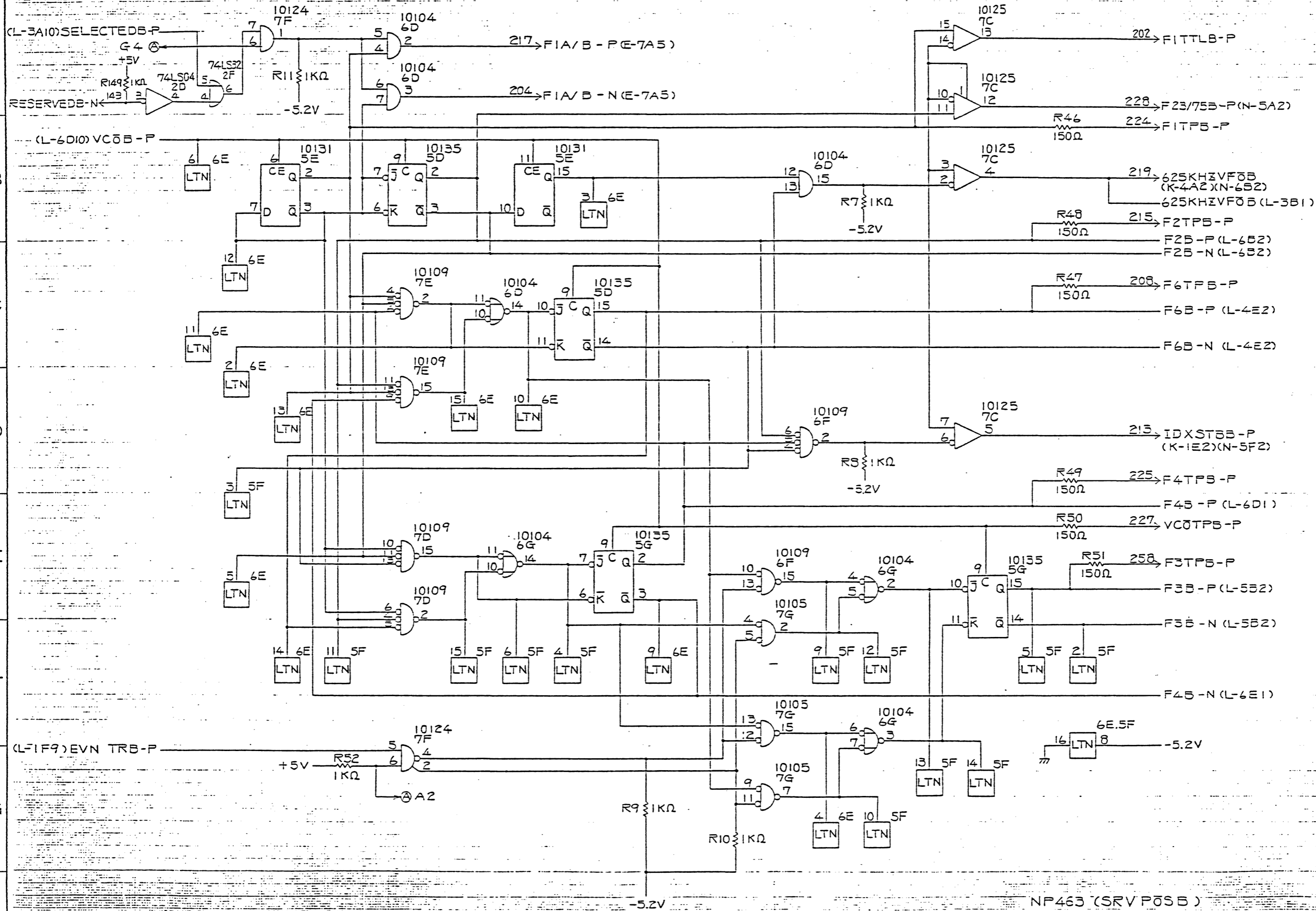


121 +12V
 221 +12V (L-4A7)(L-4D6)
 101 +12V
 167 +12V
 201 +12V
 267 +5V
 +5V (L-4A4)(L-4D5)
 0V
 106 0V
 111 0V
 116 0V
 126 0V
 131 0V
 136 0V
 146 0V
 151 0V
 161 -5.2V
 261 -5.2V (L-4C2)
 141 -12V
 241 -12V (L-4A5)(L-4C7)(L-4E5)
 (L-4F3)(L-4F8)

NP463 (SRV P05B)

L-6

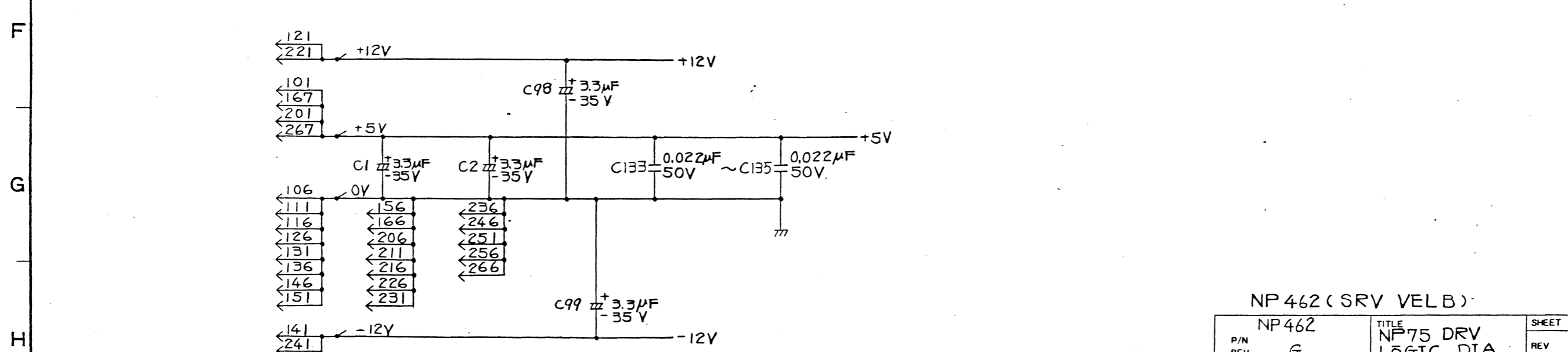
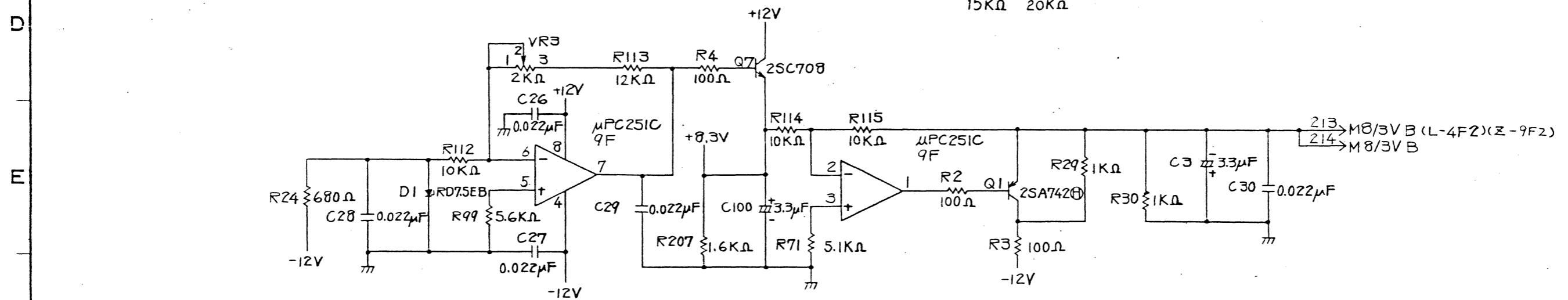
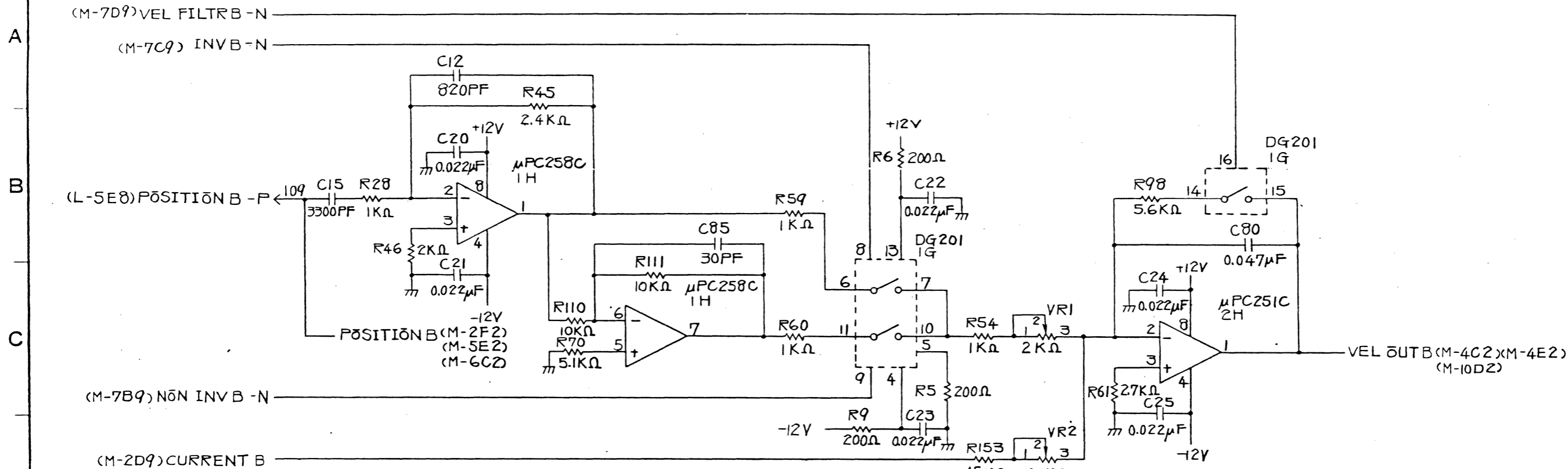
P/N REV	TITLE NF37 DRV LOGIC-DIA.	SHEET 6 /	DRAWN
	DRAWING NO NPL-NC-21463	REV 0	CHECK APPD
Nippon Peripherals Limited			



L-7

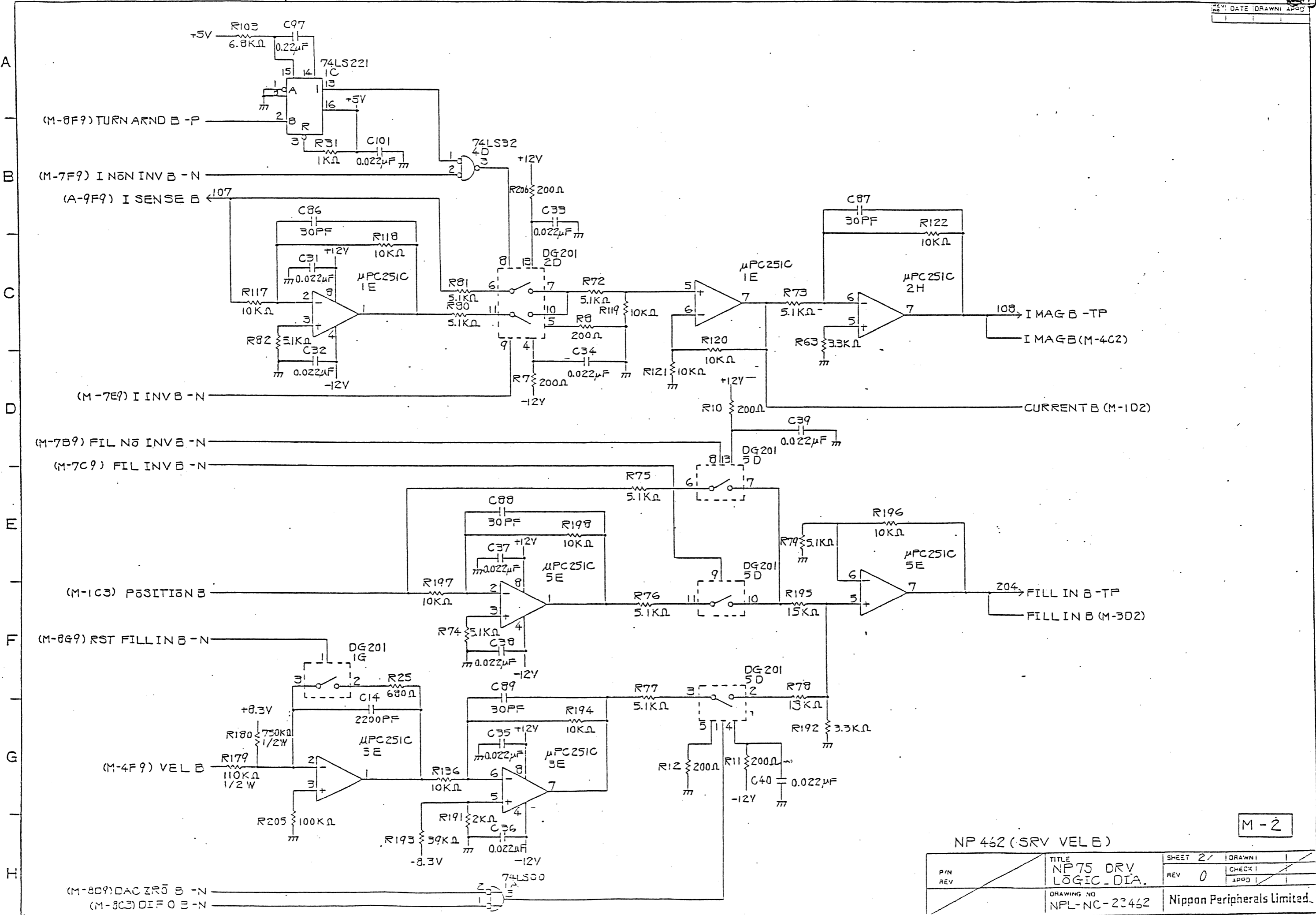
NP463 (SRV P05B)

P/N REV	TITLE NP 37 DRV LOGIC-DIA.	SHEET 7/7	DRAWN
		REV 0	CHECK APPD
DRAWING NO NPL-NC-21463		Nippon Peripherals Limited	



M-1

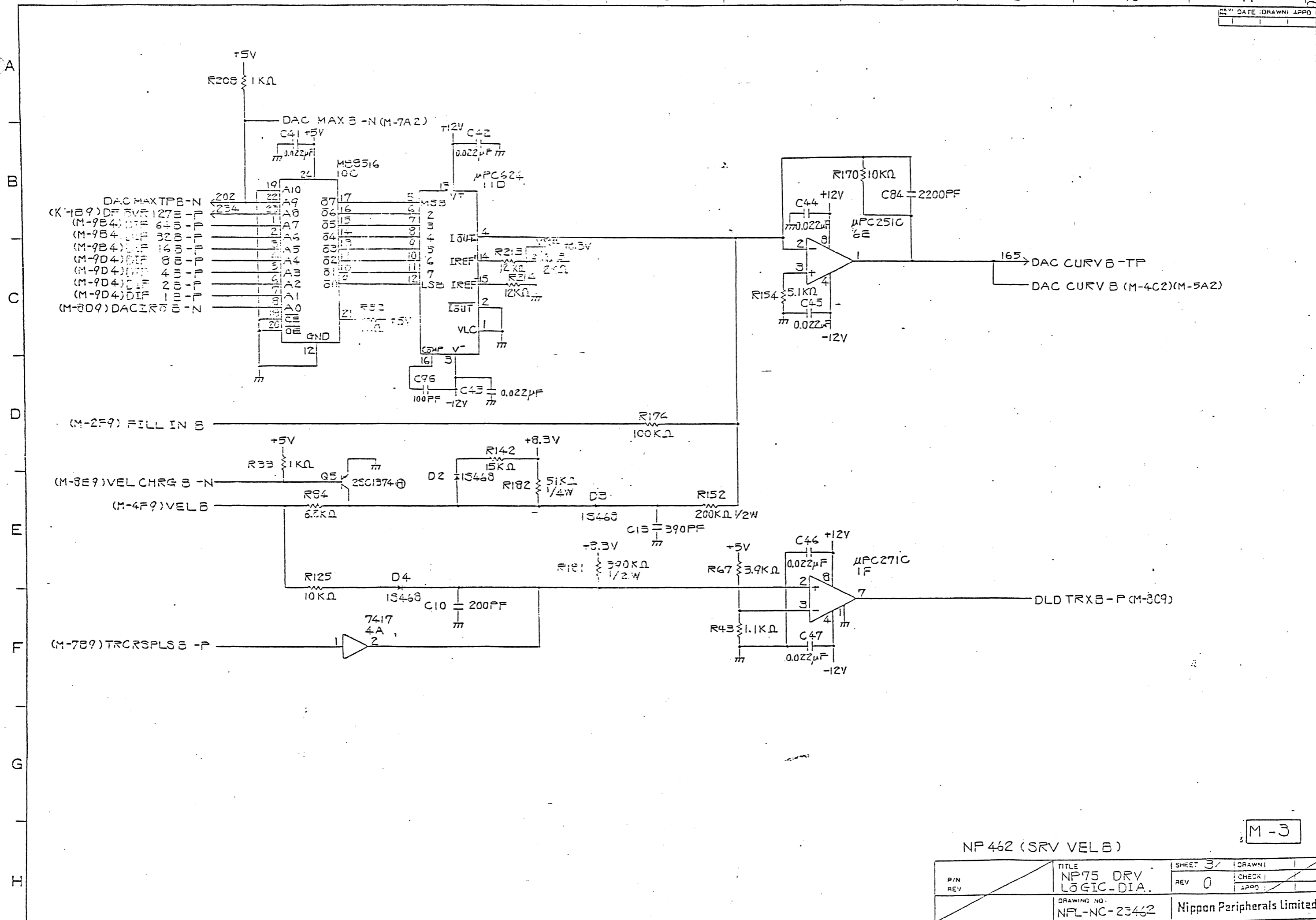
NP462 (SRV VEL B)		TITLE		SHEET 1/10		DRAWN T.S.	
P/N	NP462	NP75 DRV LOGIC-DIA.		REV	1	CHECK	
REV	G	DRAWING NO		APPD	OGINO 89.5		
SRV VEL B		NPL-NC-23462		Nippon Peripherals Limited			



M-2

NP 462 (SRV VEL B)

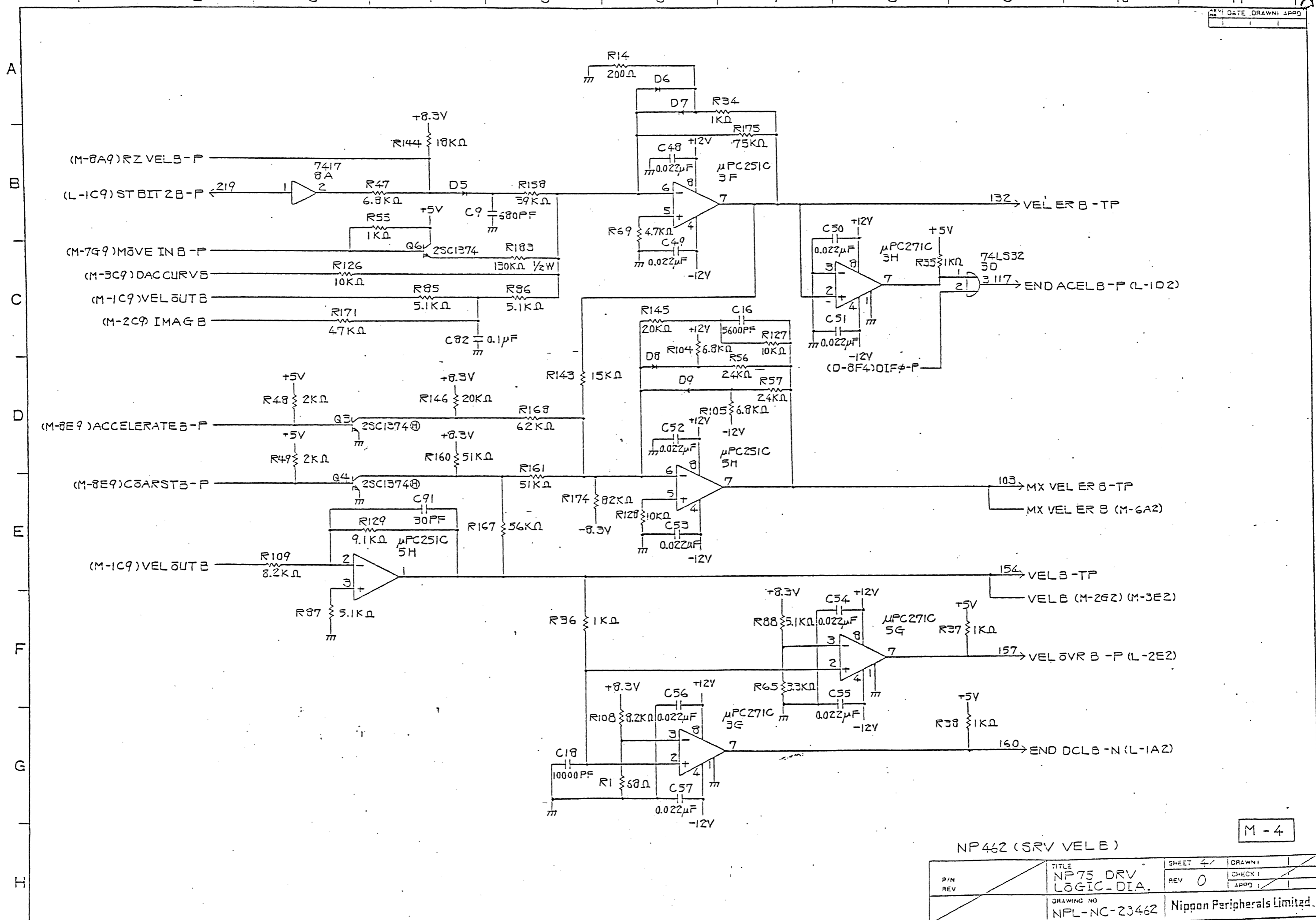
P/N REV	TITLE NP75 DRV LOGIC-DIA.	SHEET 2 / REV 0	DRAWN CHECK APPD
DRAWING NO NPL-NC-23462		Nippon Peripherals Limited.	



M-3

NP 462 (SRV VEL B)

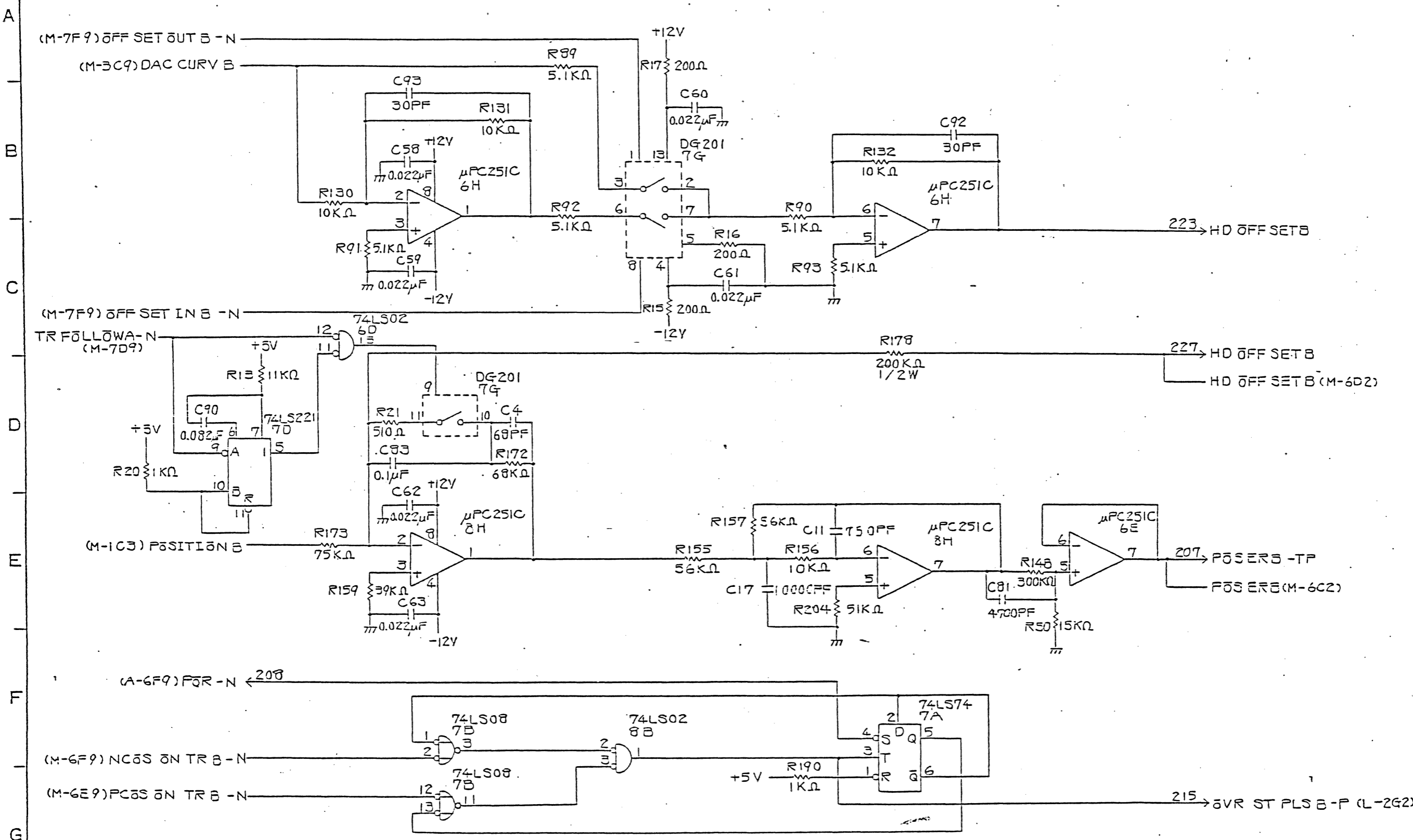
P/N REV	TITLE NP75 DRV LOGIC-DIA.	SHEET 3 /	DRAWN
		REV 0	CHECK
DRAWING NO. NFL-NC-23462		Nippon Peripherals Limited.	



M-4

NP462 (SRV VEL B)

P/N	REV	TITLE	SHEET	DRAWN
		NP75 DRV LOGIC-DIA.	4	
		DRAWING NO	REV	CHECK
		NPL-NC-23462	0	
Nippon Peripherals Limited				

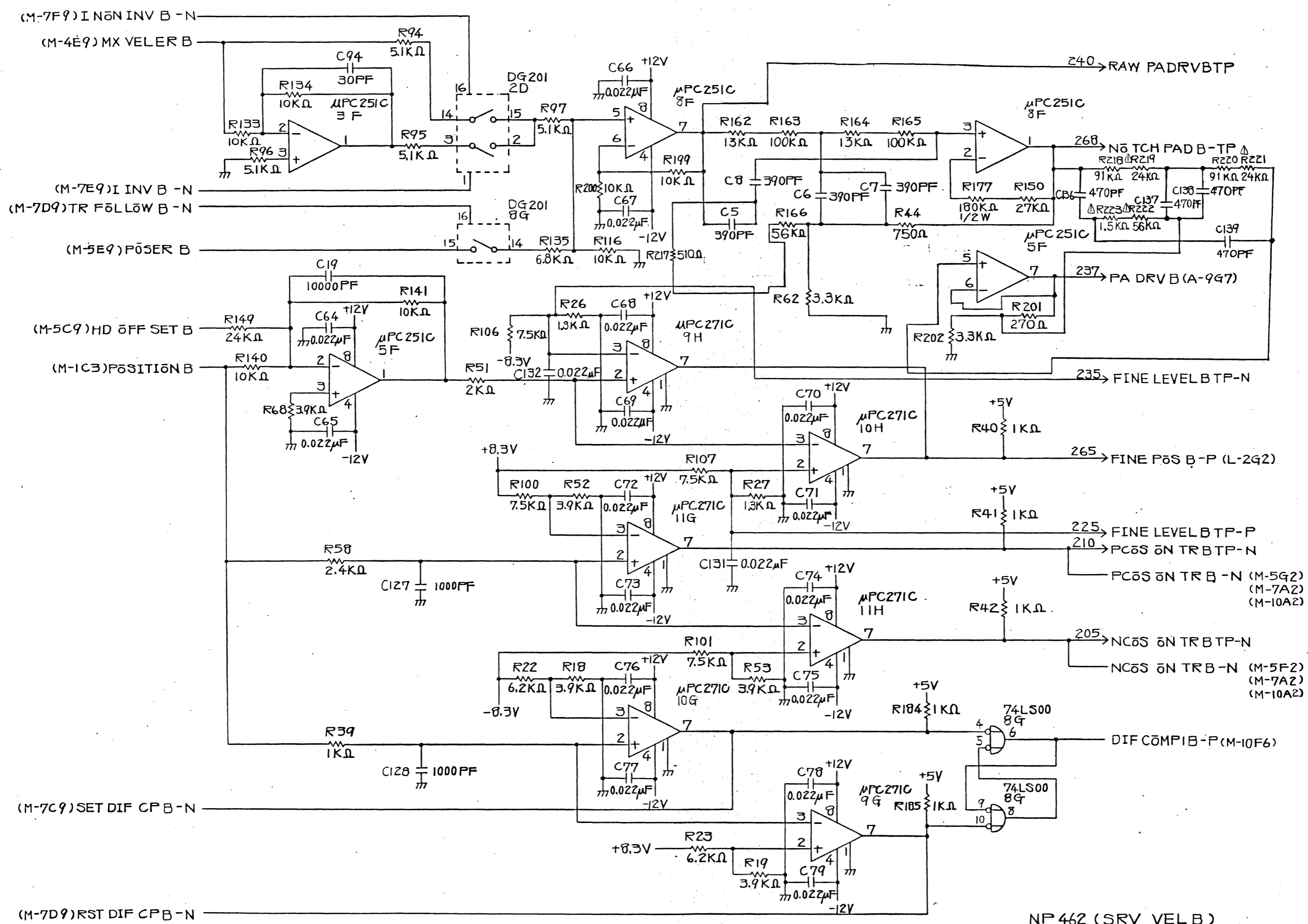


M-5

NP 462 (SRV VEL 6)

P/N REV	TITLE NP75 DRV LOGIC-DIA.	SHEET 5 /	DRAWN
	DRAWING NO NPL-NC-23462	REV 0	CHECK / APPD /
Nippon Peripherals Limited			

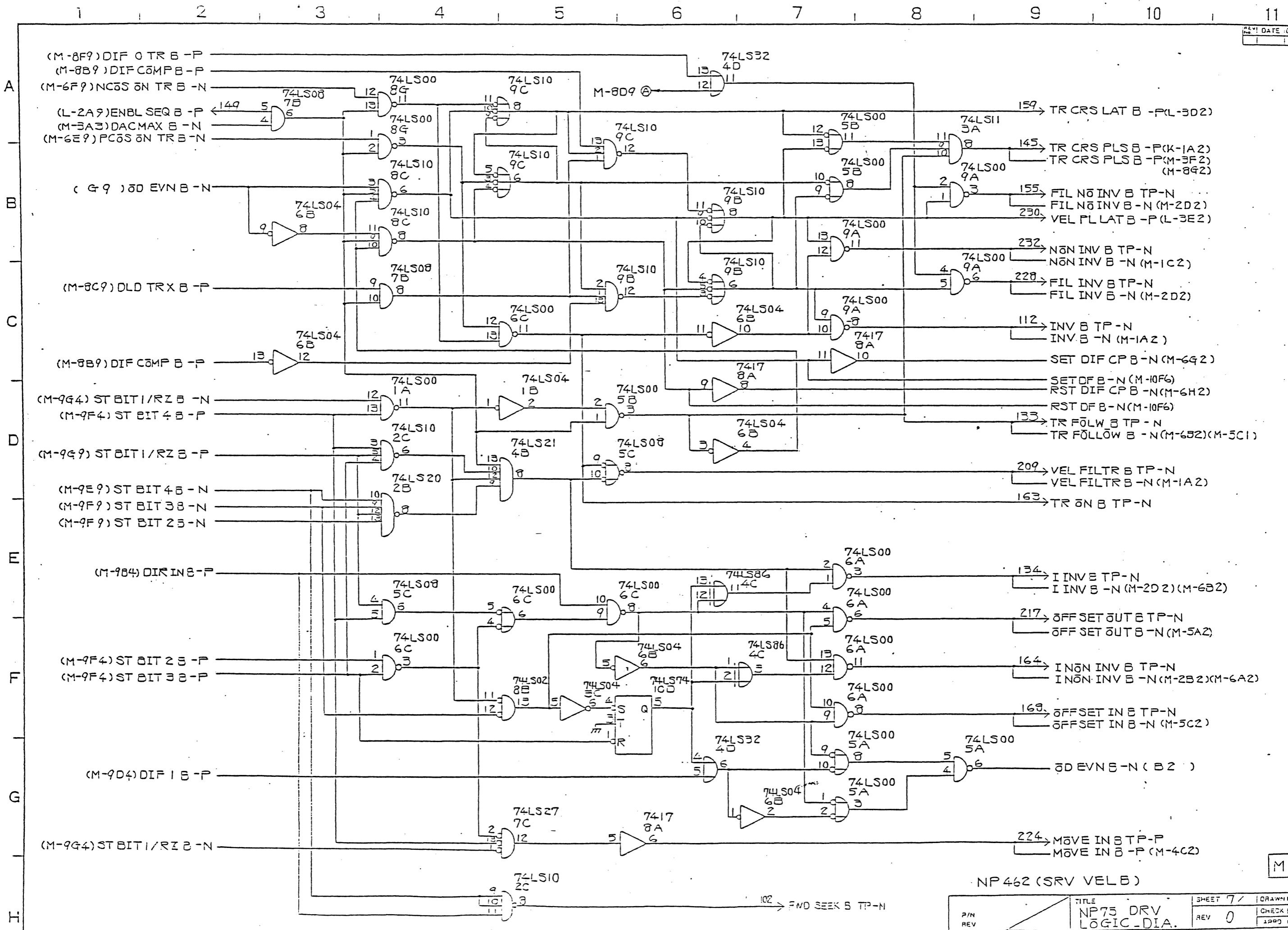
REV No.	DATE	DRAWN	APPD
R219, 221 : 56KΩ → 24KΩ			
R222 : 68KΩ → 56KΩ			
R223 : 5.6KΩ → 1.5KΩ			
1 85-2285			



M-6

NP 462 (SRV VEL B)

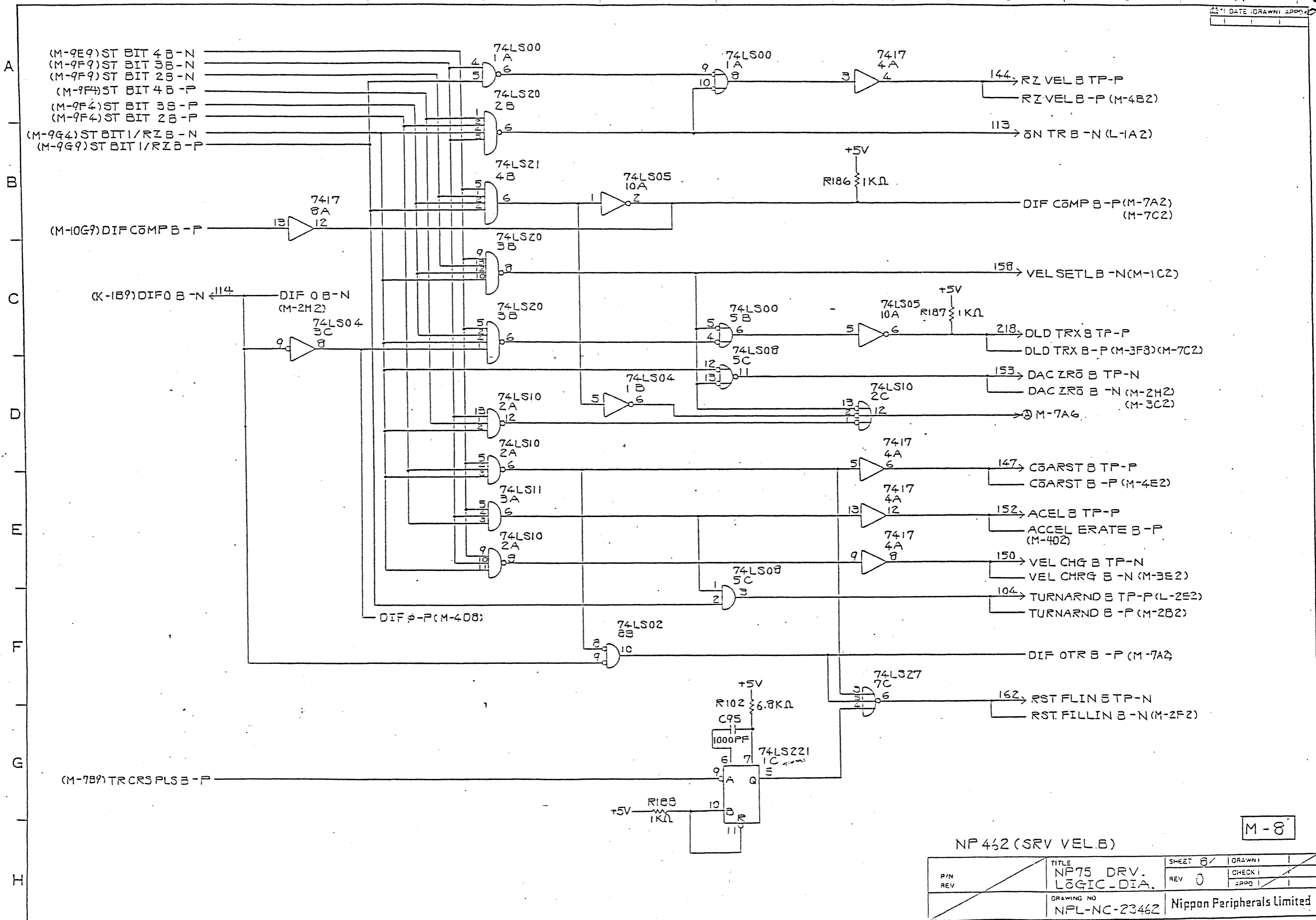
P/N	REV	TITLE	SHEET	DRAWN
		NP75 DRV LÖGIC-DIA.	6/	
		DRAWING NO	REV	CHECK
		NPL-NC-23462		APPD
Nippon Peripherals Limited				



NP 462 (SRV VEL B)

M-7

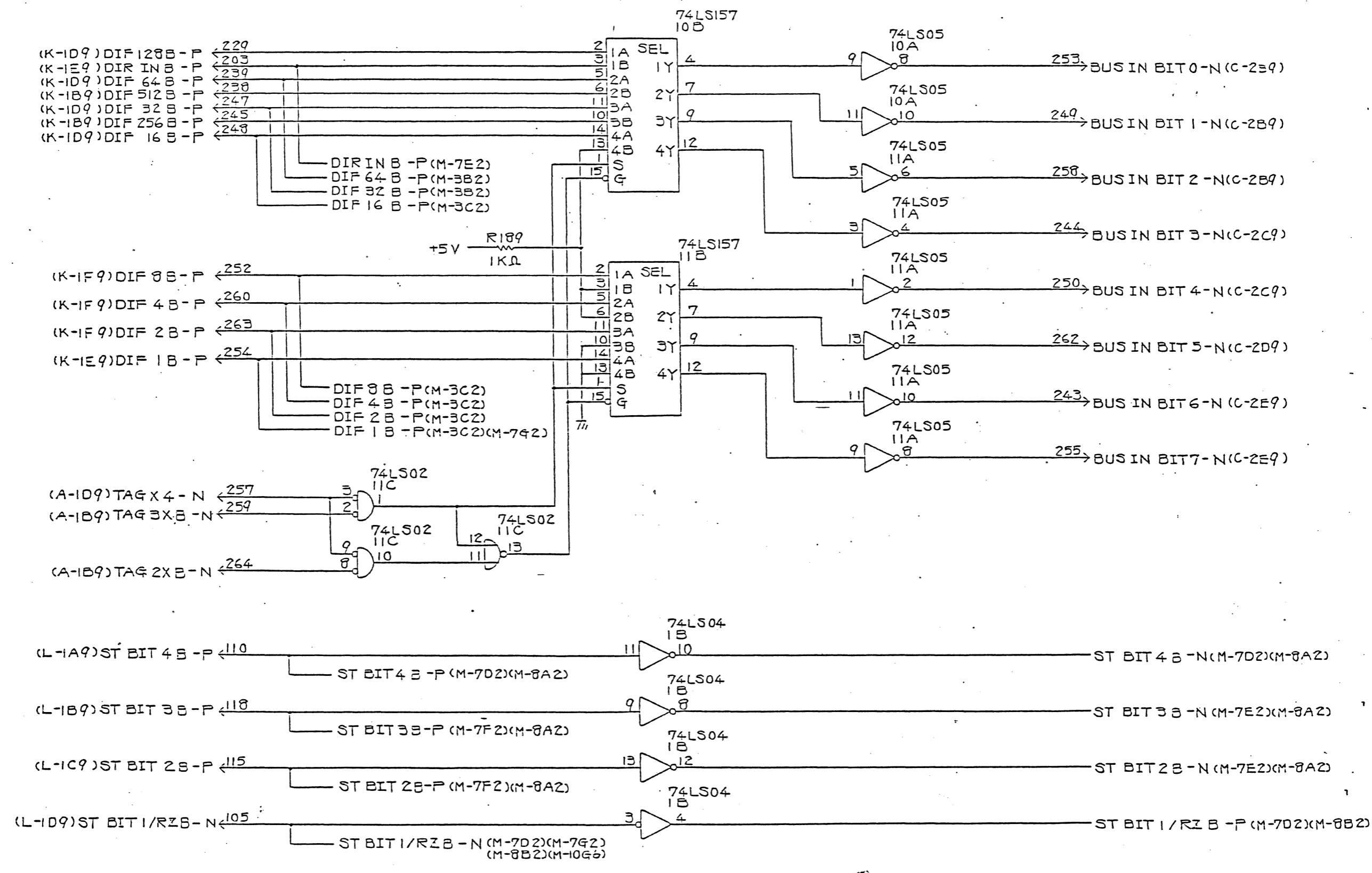
P/N REV	TITLE	SHEET 7 /	DRAWN
	NP75 DRV LOGIC-DIA.	REV 0	CHECKED
DRAWING NO		Nippon Peripherals Limited.	
NPL-NC-23462			



M-8

NP 452 (SRV VEL.B)

P/N REV	TITLE NP75 DRV. LOGIC-DIA.	SHEET 8 /	DRAWN
	DRAWING NO NPL-NC-23462	REV 0	CHECK
Nippon Peripherals Limited			



M-9

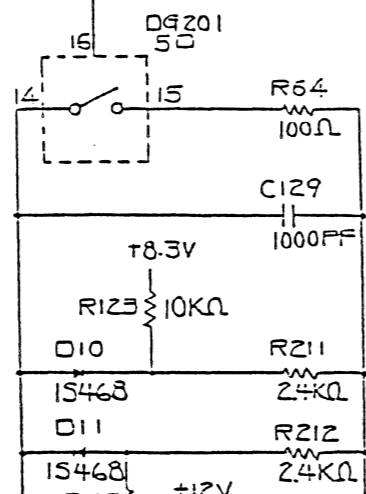
NP462 (SRV VEL B)

P/N REV	TITLE NP75 DRV LOGIC-DIA.	SHEET 9/	DRAWN
	DRAWING NO NPL-NC-23462	REV 0	CHECK I APPD
Nippon Peripherals Limited			

(M-6F9) NCOS ONTR B -N
 (M-6E9) PCOS ONTR B -N

74LS32
 4D
 8

74LS04
 3C
 10



(M-1C9) VEL OUT B

R215
 51KΩ

+12V
 C123
 0.022μF
 μPC251C
 11E

-8.3V

+12V
 C125
 0.022μF
 μPC271
 11F

-12V

C122 = 0.022μF
 R151 1KΩ

+5V

R210 1KΩ

74LS32
 3D
 8

(M-7C9) SET DF B -N

(M-7D9) RST DF B -N

74LS74
 10D
 9

(M-6F9) DIF COMP B -P

(M-9G4) ST BIT I/R B -N

74LS157
 9D
 4

233 → DIF COMP B TP -P
 DIF COMP B -P (M-8B2)

NP 462 (SRV VEL B)

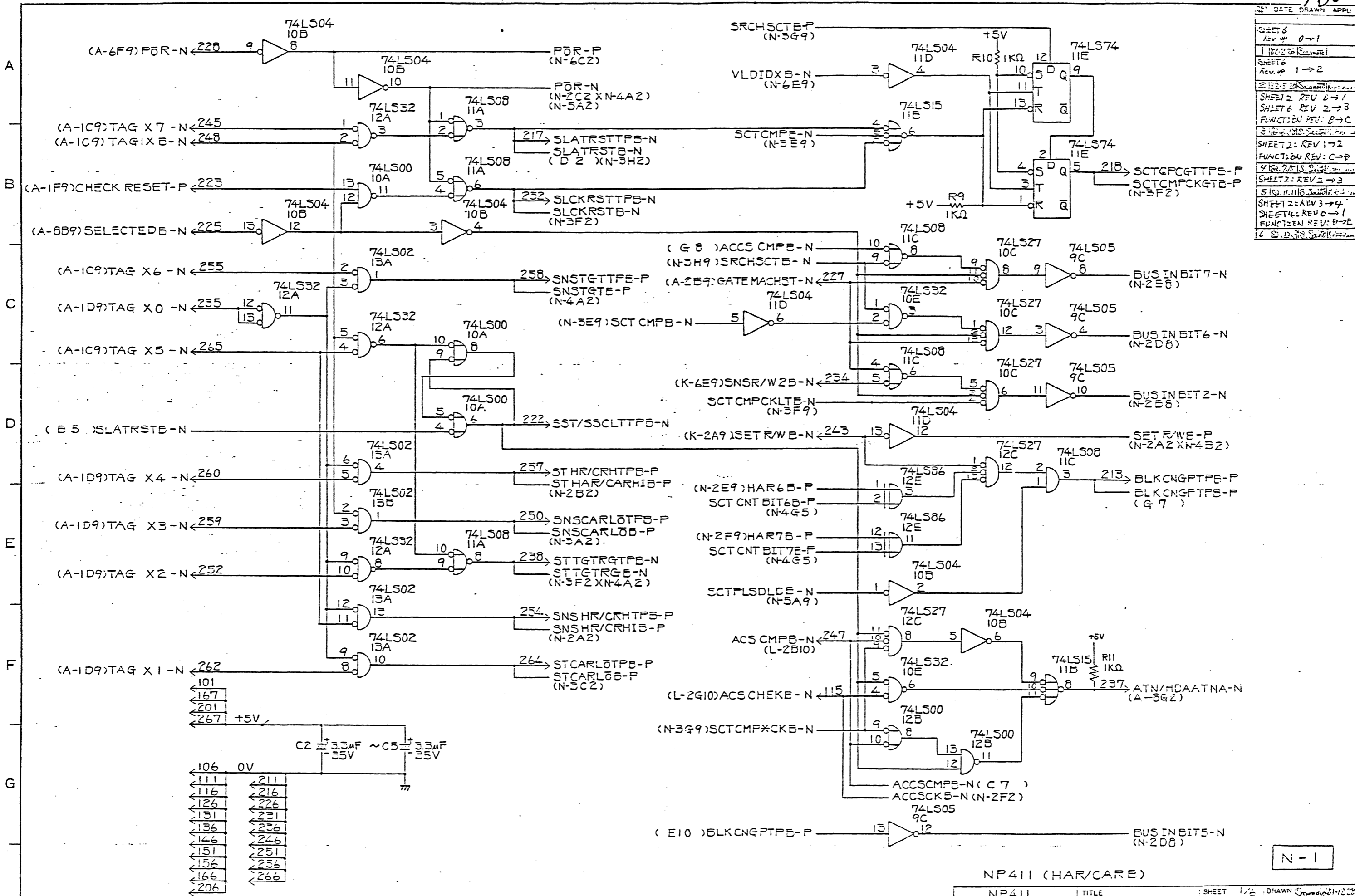
M-10

P/N	TITLE	SHEET 10 / 10	DRAWN
REV	NP75 DRV. LOGIC-DIA.	REV 0	CHECK
	DRAWING NO	Nippon Peripherals Limited	
	NPL-NC-23462	APPRO	

NC-23462

11/65

DATE DRAWN	APPL
SHEET 6	REV UP 0 → 1
SHEET 6	REV UP 1 → 2
SHEET 2: REV 0 → 1	
SHEET 6: REV 2 → 3	
FUNCTION REV: B → C	
SHEET 2: REV 1 → 2	
FUNCTION REV: C → D	
SHEET 2: REV 2 → 3	
SHEET 2: REV 3 → 4	
SHEET 4: REV 0 → 1	
FUNCTION REV: D → E	
6	



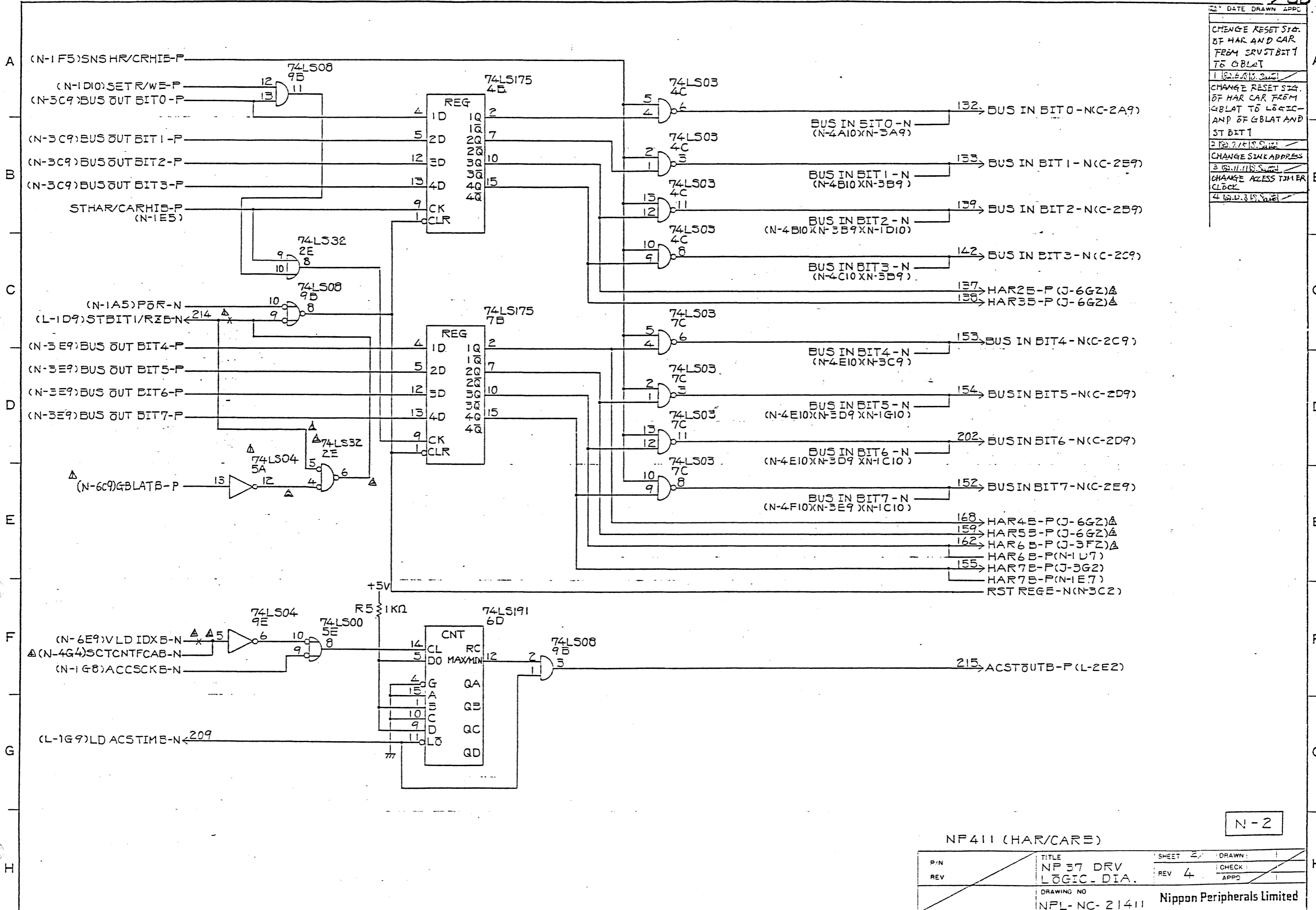
106	0V
111	211
116	216
126	226
131	231
136	236
146	246
151	251
156	256
166	266
206	

NP411 (HAR/CARE)		SHEET 1/2	DRAWN
P/N NP411	TITLE NP 37 DRV LOGIC - DIA.	REV 6	CHECK
REV E	DRAWING NO NFL-NC-21411	APPRO	
HAR/CARB		Nippon Peripherals Limited	

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N-1

REV	DATE	DRAWN	APPR
1	12.10.77		
2	2.11.78		
3	11.11.78		
4	12.11.78		



CHANGE RESET SIG. OF HAR AND CAR FROM SRVST BIT 1 TO GBLAT

CHANGE RESET SIG. OF HAR CAR FROM GBLAT TO LOGIC-AND OF GBLAT AND ST BIT 1

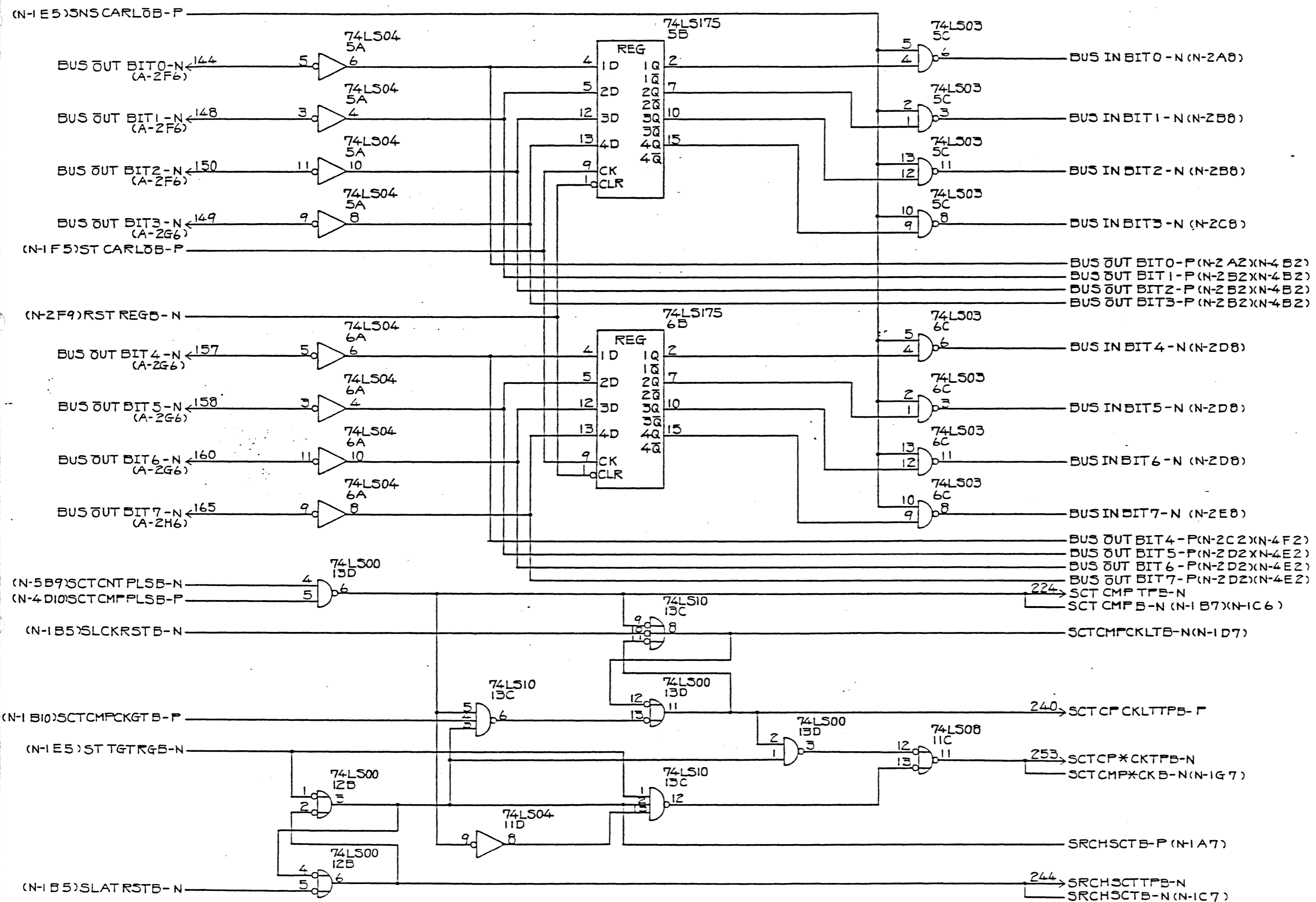
CHANGE SINK ADDRESS

CHANGE ACCESS TIMER CLOCK

N-2

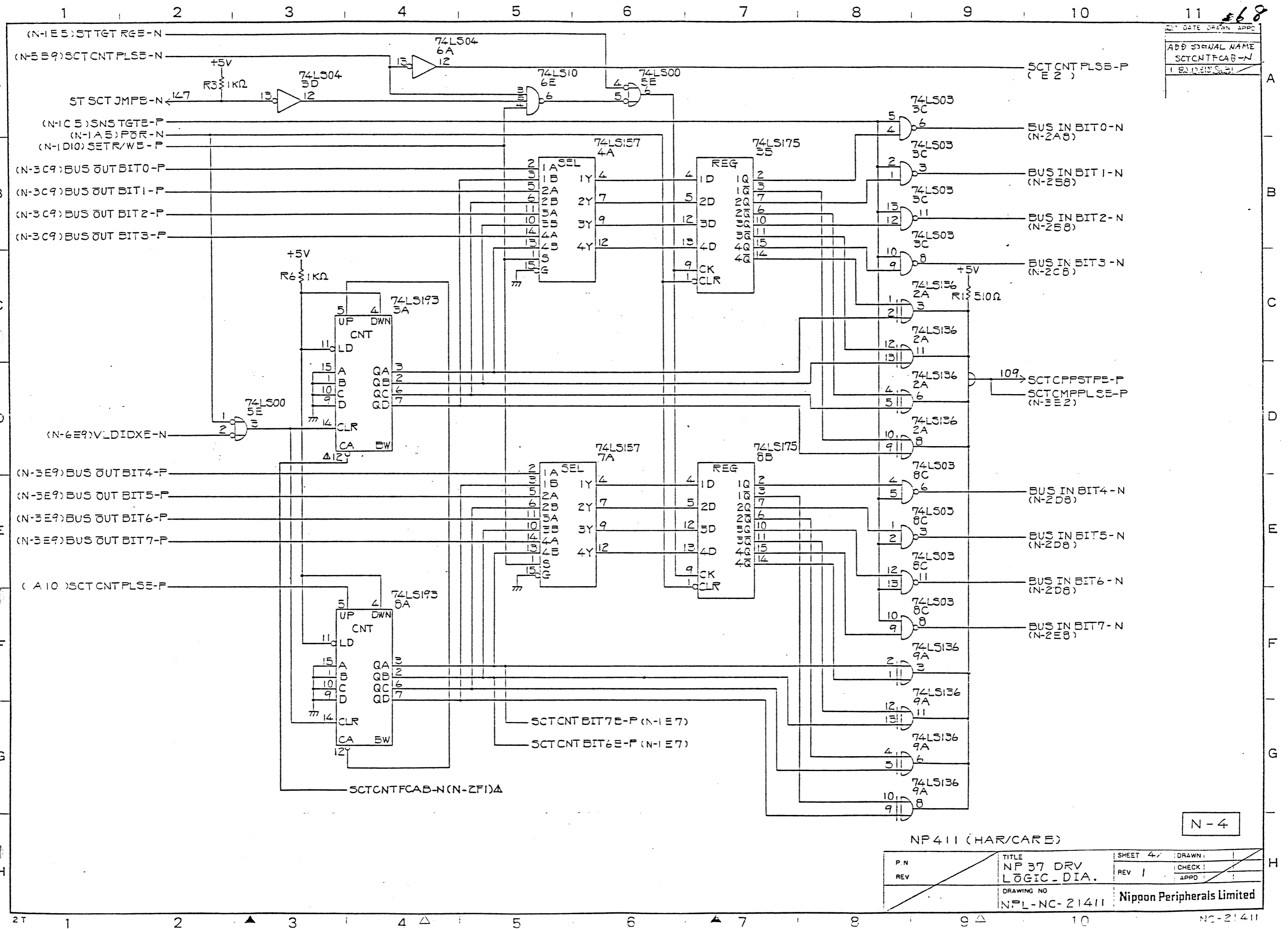
NF411 (HAR/CAR)

P/N	TITLE	SHEET	DRAWN
REV	NP 37 DRV LOGIC-DIA.	4	CHECK
DRAWING NO		APPD	
NFL-NC-21411		Nippon Peripherals Limited	



N-3

P/N	TITLE	SHEET 3 /	DRAWN
REV	NP 37 DRV LOGIC DIA.	REV 0	CHECK
	DRAWING NO		APPD
	NPL-NC-21411	Nippon Peripherals Limited	



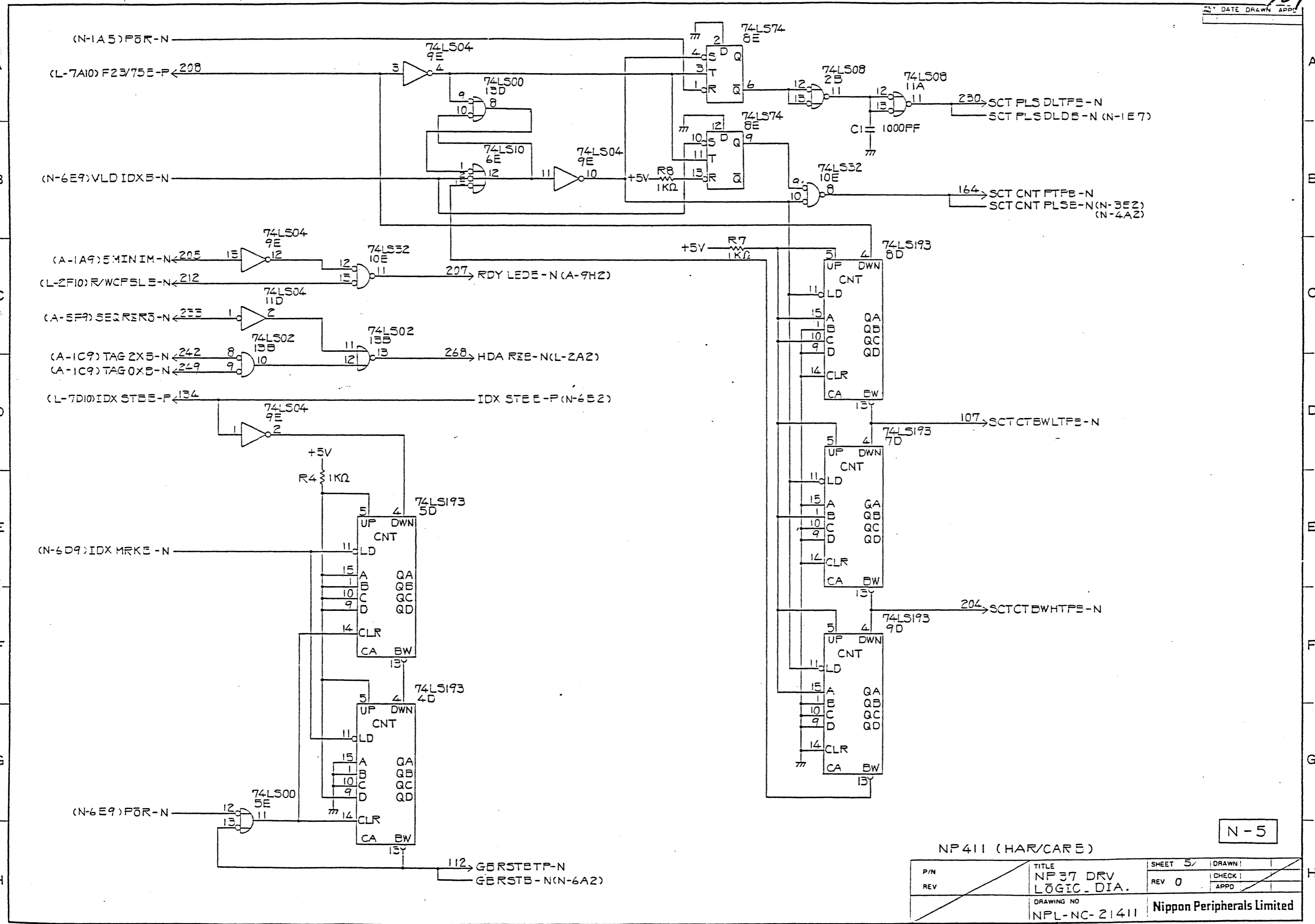
REV	DATE	DRAWN	APPD
ADD	SIGNAL NAME	SCTCNTFCAB-N	
1	ENCLOSURE		

N-4

NP411 (HAR/CAR)		TITLE		SHEET 4/		DRAWN	
P.N	REV	NP 37 DRV LOGIC-DIA.		REV	1	CHECK	
DRAWING NO		N.P.L-NC-21411		APPD		Nippon Peripherals Limited	

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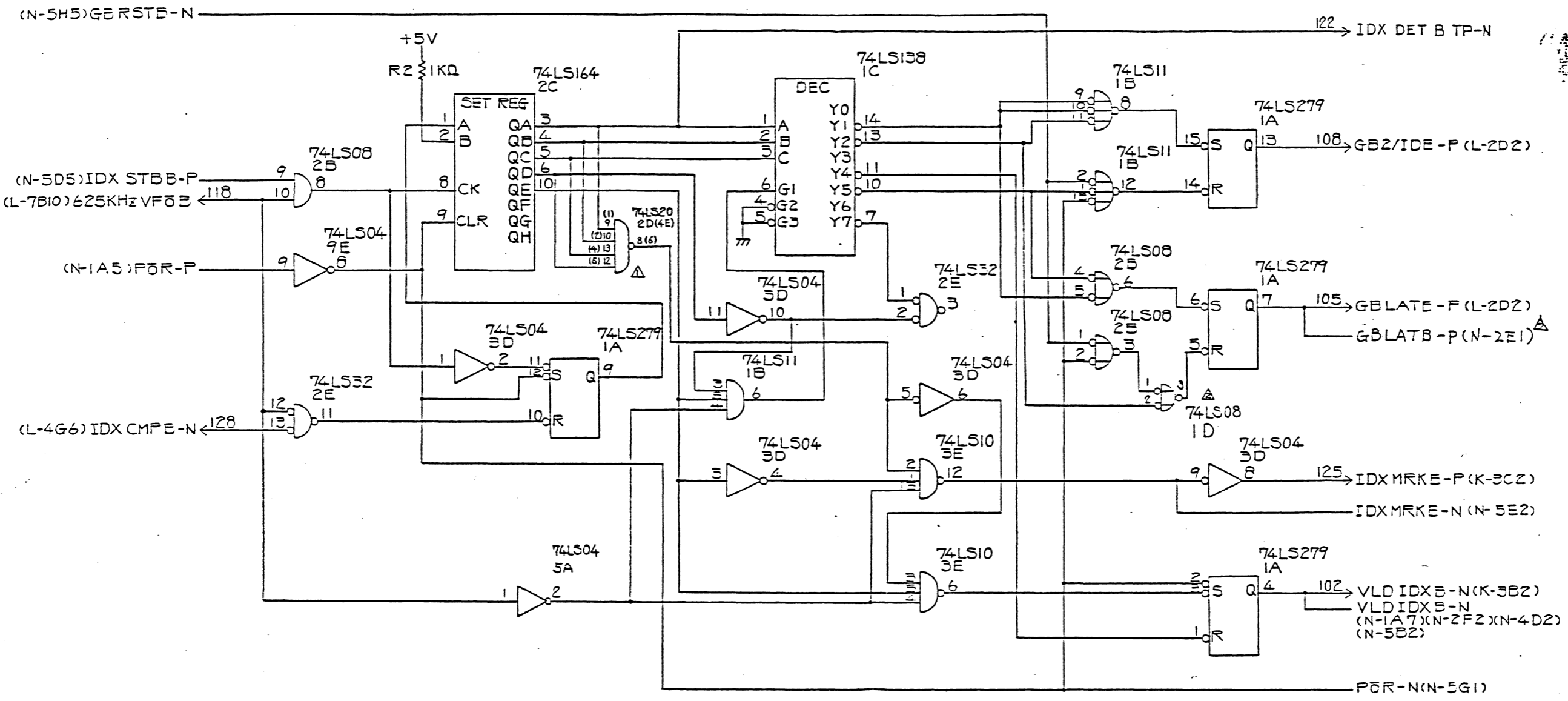
H



N-5

NP411 (HAR/CARE)		SHEET 5 / DRAWN	
TITLE NP37 DRV LOGIC-DIA.		REV 0	CHECK
DRAWING NO NPL-NC-21411		Nippon Peripherals Limited	

DATE DRAWN APP	
REV 3	
74LS08 → 2D 11.0.12.3	
74LS20 → 4E 1.2.4.5.6	
74LS138 → 1C	
74LS164 → 2C	
74LS279 → 1A, 2A, 3A, 4A, 5A, 6A, 7A, 8A, 9A, 10A, 11A, 12A, 13A, 14A, 15A, 16A, 17A, 18A, 19A, 20A, 21A, 22A, 23A, 24A, 25A, 26A, 27A, 28A, 29A, 30A, 31A, 32A, 33A, 34A, 35A, 36A, 37A, 38A, 39A, 40A, 41A, 42A, 43A, 44A, 45A, 46A, 47A, 48A, 49A, 50A, 51A, 52A, 53A, 54A, 55A, 56A, 57A, 58A, 59A, 60A, 61A, 62A, 63A, 64A, 65A, 66A, 67A, 68A, 69A, 70A, 71A, 72A, 73A, 74A, 75A, 76A, 77A, 78A, 79A, 80A, 81A, 82A, 83A, 84A, 85A, 86A, 87A, 88A, 89A, 90A, 91A, 92A, 93A, 94A, 95A, 96A, 97A, 98A, 99A, 100A	
ADD SINK ADDRESS OF GB LAT	
3 18.6.81 S. S. S.	



N-6

NF411 (HAR/CARB)		SHEET 6/6	DRAWN
P/N	TITLE	REV 3	CHECK
REV	NP 37 DRV LOGIC-DIA.	APPD	
DRAWING NO		Nippon Peripherals Limited	
NPL-NC-21411			