SuperRam™

User's Manuel

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SUPERAM

INTRODUCTION

The ECONORAM* was one of the first low cost fully buffered S-100 memory boards on the market. It made its appearance as the venerable 2102 1K memory chip made its way down the learning curve into high production. Today, the 2114 is at that same point on the volume/learning curve. It is natural then that a low density, low cost, fully buffered 16K static memory board based on the 2114 should be offered by the designer of the original ECONORAM. This time the name is SupeRam! The 2114 memory chip promises to be an even higher volume part than the 2102. This means the SupeRam memory boards will be faster, lower in power consumption, and (hopefully) cheaper with each passing of a milestone on the learning curve of the 2114 1Kx4 memory chip.

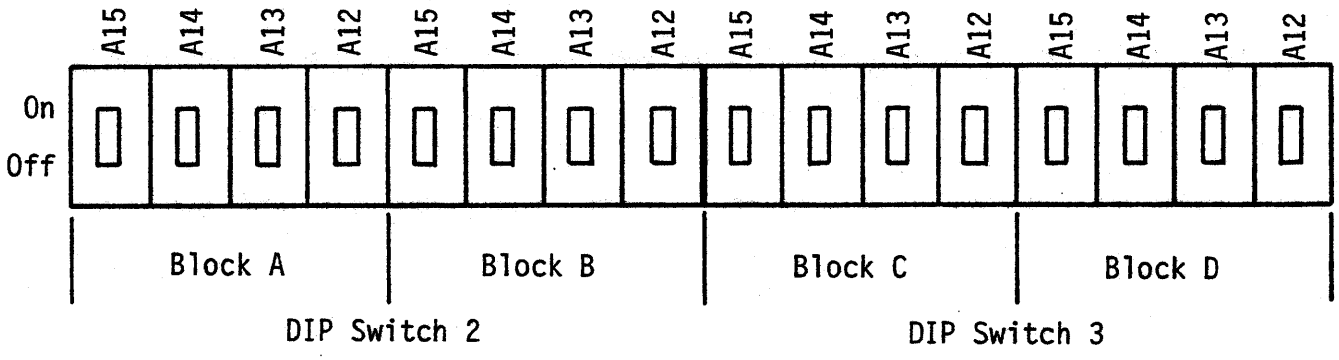
*Trademark of Godbout Electronics.

OPERATING INSTRUCTIONS

> Whenever the SupeRam memory is plugged into or removed from the host computer, it is important that the power is off.

ADDRESSING

At the top of the circuit board are three eight-position DIP switches. The right two determine the addressing of the memory. (See illustration below for DIP switches 2 and 3. DIP switch 1 will be discussed later.)



In the 64K bytes of address space of the S-100 buss, there are sixteen blocks of 4K segments. The positions of the four switches above Blocks A through D determine which 4K segment of the address space the 4K blocks of the SupeRam will occupy. For example, if the switches above Block A are all on (up), Block A will occupy locations 000:000 through 17:377 octal or 0000 FFF hex. If the switches above Block B are on (15 through 13) and off (12), Block B will occupy memory locations 20:000 through 37:377 octal or 1000 through 1FFF hex.

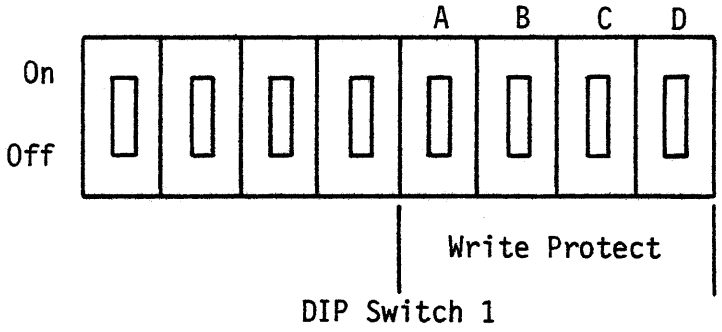
Above each switch is an address bit that the switch corresponds to. Block positions are formed by making a hex digit pattern with each group of four switches. These hex digits represent the starting address of the block associated with the switches (when followed by three hex zeros). Following is a table of switch positions and corresponding starting addresses.

Starting Address		A	A	A	A	Corres-ponding	Corresponding Binary
Hex	Octal	15	14	13	12	Hex Digit	Number
0000	000:000	up	up	up	up	0	0000
1000	020:000	up	up	up	down	1	0001
2000	040:000	up	up	down	up	2	0010
3000	060:000	up	up	down	down	3	0011
4000	100:000	up	down	up	up	4	0100
5000	120:000	up	down	up	down	5	0101
6000	140:000	up	down	down	up	6	0110
7000	160:000	up	down	down	down	7	0111
8000	200:000	down	up	up	up	8	1000
9000	220:000	down	up	up	down	9	1001
A000	240:000	down	up	down	up	A	1010
B000	260:000	down	up	down	down	B	1011
C000	300:000	down	down	up	up	C	1100
D000	320:000	down	down	down	up	D	1101
E000	340:000	down	down	down	up	E	1110
F000	360:000	down	down	down	down	F	1111

Note: up = on; down = off.

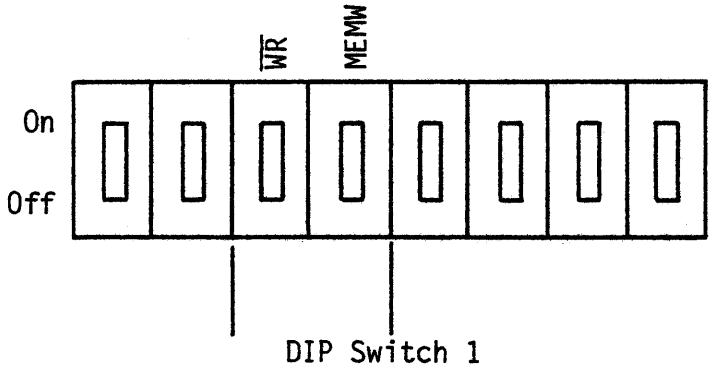
The 74S287 PROM which is responsible for doing board selection and chip selection has been programmed in such a way that if any two (or more) of the groups of switches address the same block of memory, those two (or more) blocks will disappear from the address space of the S-100 buss. For instance, if all four blocks on the board had their address selection switches on (i.e., all starting at location zero), the board would never be selected and the host computer would behave as if the memory board was not plugged into the chassis.

WRITE PROTECTION LOGIC



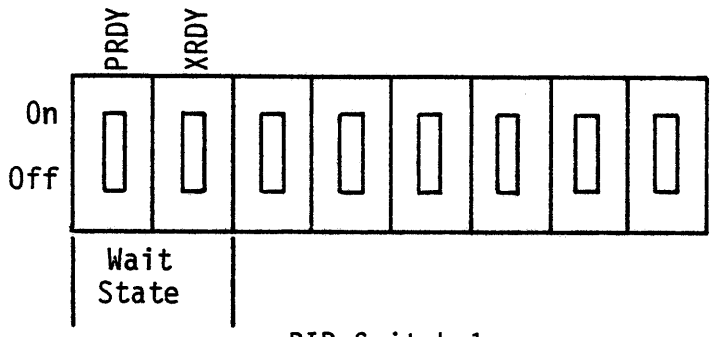
The right most four switches of DIP switch #1 are devoted to write protection for the four blocks A, B, C and D. If the switch below A is on, block A is write proted. When this switch is on (up), it is impossible for the CPU to alter any of the 4096 memory locations spanned by Block A. When this switch is off (down), the processor can write into the memory locations of Block A. A similar set of circumstances holds for the switches below B, C and D. These switches have been arranged in the same order as the address selection switches (A to the left, D to the right) to help minimize errors when these switches are manipulated.

$\overline{WR}$ and MWRITE SELECTION



Some CPU boards do not generate the signal MWRITE which represents the "memory write" strobe function. The original Altair generated MWRITE on the front panel and not on the CPU board. Several other vendors of CPU boards copied this design and so, when this type of CPU is plugged into an S-100 buss board, very likely MWRITE will be absent. If this is the case, the switch below $\overline{WR}$ should be "on" while the switch below MEMW should be "off". If the signal MWRITE is indeed generated by the CPU board in the host computer, the switch below MEMW should be "on" while the switch below $\overline{WR}$ should be "off". At no time should both switches be on.

WAIT STATE



DIP Switch 1

The memory chips included with SupeRam have a guaranteed access time of at least 450 ns over the entire 0-70° C temperature range. At 25° C (room temperature), the typical 2114 in this kit has access times between 175 and 250 ns. Although not guaranteed to run at 4 Mhz over the entire 0-70° C temperature range, the majority of the SupeRam kits currently being shipped will confortably run at 4 Mhz.

If the host computer is running at 4 Mhz and the SupeRam does not function reliably at this speed, one of the two wait switches should be turned on (up) to produce one wait state of 250 ns. Some mainframes pre-empt PRDY (most notably the Altair front panel). If this is the case, the switch above XRDY should be turned on. Other mainframes pre-empt XRDY (the IMSAI front panel). If the host processor does indeed actively drive XRDY at all times, the switch above PRDY should be turned on.

MEMORY DIAGNOSTIC

The memory test described below was designed by Phil Meads of William Brobeck Associates to exercise the most sensitive circuitry of the memory chips -- the address buffers. The test starts from the middle and works its way outward alternately to the top and bottom of memory. This type of test inverts the address lines more often than sequential ones. This continual inversion process punishes and eventually breaks down weak or faulty address buffers in the device.

USING THE TEST

The test itself must be placed in an area which is different than the location of the board(s) to be tested. The test starts on a page boundary to make the task of relocating the binary code easier.

There are two parameters in the test to be set by the user:

(1) The number of 4K blocks to be tested -- keep in mind that there are four 4K blocks per board. This constant is called BLKCNT and is located at the eleventh byte of the test.

(2) The starting page number of the lowest 4K block to be tested is called PAGENO and is located at the ninth byte of the test.

When testing more than one 4K block of memory, be sure that they occupy contiguous memory.

The page number of the position of the test itself must be entered wherever a $(YYY)_8$ or $(YY)_{16}$ occurs in the test listing. This is necessary because JMP and CALL need both the page number and the location within the page to execute correctly.

The only other thing to remember when loading the test is that it must be placed at the starting address of a page.

Start the test at the first instruction. Once started, the test will run continuously unless an error is detected. If the test encounters an error, all the data pertinent to this error is stored in the last ten locations of the test. After storing this data, the test comes to a dynamic halt at the label STALL. The test may be restarted by stopping the computer and restarting it at the POP PSW instruction following JMP STALL. The user may also restart the test from the beginning. If errors indicate the board is malfunctioning, return it as soon as possible for warranty service.

MEMORY TEST PROGRAM FOR 4K NMOS RAMS
(Octal)

```
YYY  000 061 175 YYY     START  LXI   SP,STACK   INITIALIZE STACK POINTER
     003 001 000 000            LXI   B,0        INITIALIZE CYCLE COUNT
     006 305            NEWCYL  PUSH  B          UPDATE CYCLE COUNT
     007 006 100                MVI   B,PAGENO   STARTING ADDR OF TEST MEM
     011 016 002                MVI   C,BLKCNT   # OF 4K BLOCKS TO TEST
     013 041 377 007    LOOP    LXI   H,7:377Q   HALF SIZE OF MEMORY -1
     016 170                    MOV   A,B
     017 204                    ADD   H          CALCULATE MIDDLE
     020 147                    MOV   H,A          OF CURRENT BLOCK
     021 345                    PUSH  H          SAVE INITIAL ADDRESS
     022 315 114 YYY    WRITE   CALL  TWORD      GET TEST WORD
     025 167                    MOV   M,A        STORE
     026 315 123 YYY            CALL  COMP       COMPLEMENT ADDRESS
     031 315 114 YYY            CALL  TWORD      GET TEST WORD
     034 167                    MOV   M,A        STORE
     035 315 134 YYY            CALL  INCR       COMPLEMENT & DECREMENT
     040 302 022 YYY            JNZ   WRITE        ADDRESS
     043 341                    POP   H          RECOVER INITIAL ADDRESS

YYY  044 315 114 YYY     READ    CALL  TWORD      GET TEST WORD
     047 256                    XRA   M          COMPARE
     050 304 145 YYY            CNZ   ERROR
     053 315 123 YYY            CALL  COMP       COMPLEMENT ADDRESS
     056 315 114 YYY            CALL  TWORD      GET TEST WORD
     061 256                    XRA   M          COMPARE
     062 304 145 YYY            CNZ   ERROR
     065 315 134 YYY            CALL  INCR       COMPLEMENT & DECREMENT
     070 302 044 YYY            JNZ   READ         ADDRESS

YYY  073 076 020                MVI   A,20Q     ADVANCE
     075 200                    ADD   B            THE
     076 107                    MOV   B,A          BLOCK
     077 015                    DCR   C          DECREMENT BLOCK COUNT
     100 302 013 YYY            JNZ   LOOP
     103 173                    MOV   A,E        CALCULATE NEW
     104 306 207                ADI   135          BASE FOR
     106 137                    MOV   E,A          TEST WORD
     107 301                    POP   B
     110 003                    INX   B          INCREMENT CYCLE COUNT
     111 303 006 YYY            JMP   NEWCYL

     114 175            TWORD   MOV   A,L        GET LOWER BYTE OF ADDRESS
     115 007                    RLC              ROTATE
     116 207                    ADD   A          SHIFT
     117 204                    ADD   H          ADD HIGHER BYTE OF ADDR
     120 203                    ADD   E          ADD BASE
     121 127                    MOV   D,A        SAVE TEST WORD
     122 311                    RET
```

```
YYY  123  174          COMP   MOV   A,H     COMPLEMENT THE UPPER
     124  356 017             XRI   17Q       BYTE ADDRESS
     126  147                 MOV   H,A       WITH RESPECT TO MEM SIZE
     127  175                 MOV   A,L     COMPLEMENT THE LOWER
     130  356 377             XRI   377Q      BYTE OF THE
     132  157                 MOV   L,A       ADDRESS
     133  311                 RET

YYY  134  315 123 YYY  INCR   CALL  COMP    RESTORE ADDR TO NORMAL SIZE
     137  053                 DCX   H       DECREMENT
     140  300                 RNZ           TEST IF LOWER BYTE ZERO
     141  170                 MOV   A,B     TEST UPPER BYTE EQUAL
     142  075                 DCR   A         TO BLOCK
     143  274                 CMP   H         BOUNDARY
     144  311                 RET

YYY  145  345          ERROR  PUSH  H       SAVE ERROR ADDRESS
     146  305                 PUSH  B       SAVE CURRENT BLOCK
     147  325                 PUSH  D       SAVE TEST WORD
     150  365                 PUSH  PSW     SAVE ERROR BITS
     151  303 151 YYY  STALL  JMP   STALL   DYNAMIC HALT
     154  361                 POP   PSW     RESTORE
     155  321                 POP   D         THE
     156  301                 POP   B         STATE OF
     157  341                 POP   H         THE CPU
     160  311                 RET

YYY  161  000          TABLE  DB    0       FLAGS
     162  000                 DB    0       ACC - ONES ARE ERROR BITS
     163  000                 DB    0       E - CURRENT RANDOM OFFSET
     164  000                 DB    0       D - CURRENT TEST WORD
     165  000                 DB    0       C - CURRENT BLOCK COUNT
     166  000                 DB    0       B - CURRENT BLOCK PAGE
     167  000 000             DW    0       HL - ERROR ADDRESS
     171  000 000             DW    0       RETURN ADDRESS
     173  000 000             DW    0       CYCLE COUNT
     175  000 000        STACK DW    0
```

MEMORY TEST PROGRAM FOR 4K NMOS RAMS
(Hex)

```
YY  00   31 7D YY      START  LXI   SP,STACK
    03   01 00 00             LXI   B,0
    06   C5           NEWCYL PUSH  B
    07   06 40                MVI   B,PAGENO
    09   0E 02                MVI   C,BLKCNT
    0B   21 FF 07      LOOP   LXI   H,7:377Q
    0E   78                   MOV   A,B
    0F   84                   ADD   H
    10   67                   MOV   H,A
    11   E5                   PUSH  H
    12   CD 4C YY      WRITE  CALL  TWORD
    15   77                   MOV   M,A
    16   CD 53 YY             CALL  COMP
    19   CD 4C YY             CALL  TWORD
    1C   77                   MOV   M,A
    1D   CD 5C YY             CALL  INCR
    20   C2 12 YY             JNZ   WRITE
    23   E1                   POP   H

YY  24   CD 4C YY      READ   CALL  TWORD
    27   AE                   XRA   M
    28   C4 65 YY             CNZ   ERROR
    2B   CD 53 YY             CALL  COMP
    2E   CD 4C YY             CALL  TWORD
    31   AE                   XRA   M
    32   C4 65 YY             CNZ   ERROR
    35   CD 5C YY             CALL  INCR
    38   C2 24 YY             JNZ   READ

YY  3B   3E 10                MVI   A,20Q
    3D   80                   ADD   B
    3E   47                   MOV   B,A
    3F   0D                   DCR   C
    40   C2 0B YY             JNZ   LOOP
    43   7B                   MOV   A,E
    44   C6 87                ADI   135
    46   5F                   MOV   E,A
    47   C1                   POP   B
    48   03                   INX   B
    49   C3 06 YY             JMP   NEWCYL

YY  4C   7D           TWORD  MOV   A,L
    4D   07                   RLC
    4E   87                   ADD   A
    4F   84                   ADD   H
    50   83                   ADD   E
    51   57                   MOV   D,A
    52   C9                   RET
```

```
YY  53   7C          COMP   MOV    A,H
    54   EE 0F               XRI    17Q
    56   67                  MOV    H,A
    57   7D                  MOV    A,L
    58   EE FF               XRI    377Q
    5A   6F                  MOV    L,A
    5B   C9                  RET

YY  5C   CD 53 YY    INCR   CALL   COMP
    5F   2B                  DCX    H
    60   C0                  RNZ
    61   78                  MOV    A,B
    62   3D                  DCR    A
    63   BC                  CMP    H
    64   C9                  RET

YY  65   E5          ERROR  PUSH   H
    66   C5                  PUSH   B
    67   D5                  PUSH   D
    68   F5                  PUSH   PSW
    69   C3 69 YY    STALL  JMP    STALL
    6C   F1                  POP    PSW
    6D   D1                  POP    D
    6E   C1                  POP    B
    6F   E1                  POP    H
    70   C9                  RET

YY  71   00          TABLE  DB     0        FLAGS
    72   00                  DB     0        ACC - ONES ARE ERROR BITS
    73   00                  DB     0        E - CURRENT RANDOM OFFSET
    74   00                  DB     0        D - CURRENT TEST WORD
    75   00                  DB     0        C - BLOCKS LEFT TO TEST
    76   00                  DB     0        B - CURRENT BLOCK PAGE
    77   00 00               DW     0        HL - ERROR ADDRESS
    79   00 00               DW     0        RETURN ADDRESS
    7B   00 00               DW     0        CYCLE COUNT
    7D   00 00          STACK  DW     0
```

PARTS LIST

○	1	8" x 10" glossy photo
○	1	5" x 10" printed circuit board
○	3	SIP resistor packs
○	23	by-pass capacitors*
○	5	39 µfd tantulum capacitors
○	4	14-pin low-profile sockets
○	4	16-pin low-profile sockets
○	32	18-pin low-profile sockets
○	2	20-pin low-profile sockets
○	1	24-pin low-profile socket
○	3	8-position DIP switches
○	4	heat sinks
○	4	6-32 x 5/16 machine screws
○	4	6-32 hex machine screws
○	1	74LS154/74154 1 of 16 decoder
○	2	74LS240/74LS241/74LS244 octal tristate** buffer
○	4	74LS266 quad exclusive nor gates
○	1	74S287/82S129/6301 4x256 PROM
○	1	74S288/82S123/6331 8x32 PROM
○	1	74368 hex tristate** inverting buffer
○	1	74LS368 hex tristate** inverting buffer
○	32	2114 4 x 1K static PROMs
○	4	7805/340.5 monolithic 5 volt regulators

*by-pass capacitors will vary in value between .01 µfd and .1 µfd.

**tristate is a trademark of National Semiconductor.

ASSEMBLY INSTRUCTIONS

DO NOT INSTALL OR SOLDER ANY PARTS UNTIL YOU HAVE READ THESE INSTRUCTIONS SEVERAL TIMES AND HAVE FULLY DIGESTED THE INFORMATION!

CAUTION - DO NOT SOLDER OR CLIP COMPONENT LEADS WITHOUT USING SAFETY GLASSES!

INSPECTION

Use the parts list to make sure that there are no missing items in your kit. Please notify us of any shortages. Be sure to check for missing parts before you start assembling.

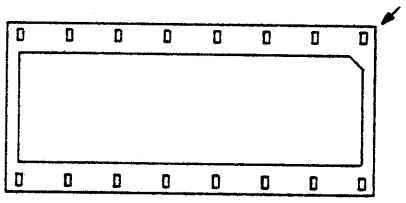
SOCKETS

A socket is furnished for every integrated circuit. It is important that you use the sockets; otherwise, a defective part will be extremely difficult to replace.

NO REPAIR OR SERVICE WILL BE PERFORMED ON A CIRCUIT BOARD WHICH HAS HAD INTEGRATED CIRCUITS SOLDERED TO IT.

PARTS ORIENTATION

In all references throughout the instructions, the convention used is that the gold edge connector is the bottom of the board. Orientation identification is molded into the plastic of the sockets either with numbers or in the manner illustrated below.



This orientation mark or an embossed "1" identifies where pin #1 of the integrated circuit is to be positioned when inserted into the socket. The sockets should be inserted in the board so that the orientation mark is in the upper right hand corner.

ASSEMBLY INSTRUCTIONS

The tantulum capacitors should be oriented so that the red strip or positive mark is to the left when the part is inserted in the board. The three DIP switches at the top of the board should be positioned so that switch #1 is to the left.

The SIP resistor packs have an orientation dot at one end. The pin associated with this dot is the common point of the nine resistors in this package and must be to the right when the parts are soldered to the board.

SOLDERING AND SOLDER IRONS

The most desirable soldering iron for complex electronic kits is a constant temperature soldering iron with an element regulated at 650° F. The tip should be fine so that it can be brought in intimate contact with the pads of the circuit board. Both Unger and Weller have excellent products which fit the above requirements.

There are three important soldering requirements for building this kit:

1. Do not use an iron that is too cold (less than 600° F) or too hot (more than 750°).

2. Do not apply the iron to a pad for extended periods.

3. Do not apply excessive amounts of solder.

The proper procedure for soldering components to the circuit board is as follows:

1. Bring the iron in contact with both the component lead and the pad.

2. Apply a small amount of solder at the point where the iron, component lead, and pad all make contact.

3. After the initial application of solder has been accomplished with the solder flowing to the pad and component lead, the heat of the iron will have transferred to both the pad and the lead. Apply a small amount of additional solder to cover the joint between the pad and the lead. DO NOT PILE SOLDER ON THE JOINT! EXCESSIVE HEAT AND SOLDER CAUSE PADS AND LEADS TO LIFT FROM THE CIRCUIT BOARD. EXCESSIVE SOLDER IS THE PRIMARY CAUSE FOR BOARD SHORTS AND BRIDGED CONNECTIONS.

PARTS INSTALLATION

Install:

_____ Sockets 1B-8B, 1C-8C, 1D-8D, 1E-8E, 18-pin low-profile. Pin #1 to upper right.

_____ Sockets 1F, 2F, 2H, 8H, 16-pin low-profile sockets. Pin #1 to upper right.

_____ Sockets 3F, 4F, 3H, 4H, 14-pin low-profile sockets. Pin #1 to upper right.

_____ Sockets 5F, 5H, 20-pin low profile. Pine #1 to upper right.

_____ Socket 7H, 24-pin low-profile. Pin #1 to upper right.

_____ C1-C5, 39 µfd tantulum capacitors. Orientation mark to the left. .6" wide.

_____ SIPS 1, 3, 4. Single-in-line resistor packs. Orientation dot to the right.

_____ By-pass capacitors (23) as shown on the silk screen legend on the circuit board.

_____ DIP switches 1, 2 and 3. Switch #1 of each DIP is to the left.

_____ 7805/LM340.5 5-volt regulators (4) by bending the leads, inserting and hand tightening the nut and bolt through the regulator, heat sink, and circuit board. Solder the leads. If heat sink grease is available, apply a thin film between the board, heat sink and regulator before soldering the leads. Finally, tighten the nut.

POWER SUPPLY/VOLTAGE REGULATOR CHECK OUT

Voltage requirements: (reference to ground - pins 50 and 100)

Pins 1 and 51: not less than 7 volts approx. 2000 ma
not more than 10 volts

Before installing any of the integrated circuits, apply power to pins 1 and 51 as specified above. Power can come from external supplies or from a host computer. After applying power, perform the following measurements:

(1)	1F pin 16	+5 volts
(2)	2H pin 16	+5 volts
(3)	3H pin 4	+5 volts
(4)	4H pin 14	+5 volts
(5)	5H pin 20	+5 volts
(6)	7H pin 24	+5 volts
(7)	8H pin 16	+5 volts

If the voltage at any of the check points differs by more than 5% of the required value, return the board for warranty/repair trouble-shooting.

POWER-UP CHECK OUT

Install the integrated circuits as per the layout sheet. Be very careful not to bend pins of the ICs under the package. Often a pin which is bent under an IC appears to be inserted in the socket. REMEMBER: BENT PINS ARE THE MOST COMMON REASON FOR A MALFUNCTIONING BOARD!

After the parts have been installed, repeat the seven voltage measurements specified in the previous section. If the test points differ from the required values, the board should be returned. Under no circumstance should sockets be removed from the board. Such abuse may void the warranty under which repair and service is performed.

SYSTEM CHECK OUT

Select four different bank positions for the four blocks of memory on the board. Make sure that the write protect switches are all off. Select PWR or MWRITE (switches number 3 and 4 of DIP switch #1) as appropriate for the host computer. Finally, qualify XRDY or PRDY if the host computer is running at 4 Mhz (switches number 1 and 2 of DIP switch #1). Normally, both switch #1 and #2 of DIP switch #1 should be off. Next, plug the board into

an empty slot of the main frame and apply power. Examine several locations in each of the four different blocks and verify that all zeros and all ones can be written into and read from each of the four 1K sub-blocks of each 4K block.

Finally, a memory test (either the one included in this manual or one of your own chosing) should be run for several hours over the entire 16K. After completion of these steps, the memory is ready for use in your mainframe.

PRINCIPLES OF OPERATION

ADDRESS SELECTION

Sixteen address switches are set up to select memory as four independently addressable blocks of 4K bytes each. The first four address switches of DIP switch #2 set memory address for the first 4K block and the second four switches set memory address for the second 4K block; the first four switches of DIP switch #3 set memory address for the third 4K block and the second four switches set memory address for the fourth 4K block.

Each address switch is connected to an open-collector exclusive NOR gate and pull-up resistor so that if the switch is closed, less than .6 volts pass, producing a logical Ø. If the switch is open, more than 2.4 volts pass, producing a logical 1. The logical values of the voltages passing through each address line and its switch line are compared, determining the signal sent to the select line: if both the address line and the switch line equal logical 1 or both equal logical Ø, that selecting signal is high, but if they do not equal each other, that selecting signal is low. When each pair in each set of four lines match, producing a high signal (whether through matching at logical Ø or logical 1) the corresponding 4K block of memory is selected; if the pairs of lines do not match (for example, if three pairs produce a high signal but one produces a low signal) the memory block is not selected.

Truth Table of the 74LS266 Open Collector Exclusive NOR Gate

Input	Input	Output
0	0	Off
0	1	On
1	0	On
1	1	Off

These select lines enter PROM 74S287/82S131/6301, effectively a 4 to 2 encoder, which ultimately selects the memory boards and chips to be used. It combines the select signals with five other bus signals as discussed below. Provided that $\overline{\text{PHANTOM}}$ is high while SOUT, SINP, and SINP are low, $\overline{\text{BD ENBL}}$ will be low. When $\overline{\text{BD ENBL}}$ is low, $\overline{\text{STB BUFFER}}$ goes low if PDBIN goes high and vice versa. $\overline{\text{STB BUFFER}}$ acts to enable the 74LS240/241/244 input data buffers to transfer data from the memory to the CPU. (If $\overline{\text{PHANTOM}}$ is low, all other signals will be ignored and addressing is not enabled. If either SINP or SOUT is high, an input or input instruction is occurring and the address lines are ignored. If PDBIN is low, signals are moving from the CPU to the memory board. If SINTA is low, the unit will work as memory; if it is high, other signals will be ignored.)

Pin 9 of the 74S287/6301 PROM will be referred to as BLOCK SELECT I (BS I) and Pin 10 as BLOCK SELECT II (BS II). If SELECT A is the only high select line, both the BSI and BS II lines will equal logical Ø; if SELECT B is the only high select line, BS I line will equal logical Ø and BS II line will equal logical 1; if SELECT C is the only high select line, BS I line will equal logical 1 while BS II line will equal logical Ø; if SELECT D is the only high select line, both BS I and BS II lines will equal logical 1. If two or more select lines are high, $\overline{\text{STB BUFFER}}$ and $\overline{\text{BD ENBL}}$ signals will remain high and no block will be selected.

In addition to these BS I and II lines entering decoder chip 74154 are two address lines, A1Ø and A11. These four lines, governed by the $\overline{\text{BD ENBL}}$ signal, select two of thirty-two chips, each pair of chips containing 1K by 8 bits (1K bytes) of memory. If $\overline{\text{BD ENBL}}$ is high, all chip selects are high and no chips are selected. If $\overline{\text{BD ENBL}}$ is low, one chip pair is selected by matching the logical values of the two BLOCK SELECT lines and the two address lines as shown in the following table:

A1Ø	A11	BS I	BS II	Selected Pair
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	15

Each chip contains ten address lines, four (bidirectional) input/output data lines, a 5 volt power supply, a ground, and a write line (low for writing and high for reading). Additionally, memory chips and buffers are tri-state and when enabled can transmit a high signal to turn the data buffers on or a low signal to turn the data buffers off, or they can transmit no signal (completely off).

WRITE OPERATION

Four write-protect switch lines enter PROM 74S288, each switch governing one 4K block of memory. Additionally, the $\overline{\text{PWR}}$ line carries signals from the CPU (or, in some computers, the $\overline{\text{PWR}}$, front panel write, and low SOUT combine to produce a MWRITE signal) to enable writing. During a write operation, PDBIN is low, and $\overline{\text{PWR}}$ is low and/or MWRITE is high. Signals enter the PROM and when combined with signals from write-protect switches in the unprotected mode emit a write enable signal.

READ OPERATION

To read, PDBIN is high, and $\overline{\text{PWR}}$ is high and/or MWRITE is low. When an address is selected (see "Address Selection"), the $\overline{\text{STB BUFFER}}$ enables the output buffers of the selected board which then buffer data from the selected chip through the input data buss lines.

WAIT STATE

To allow guaranteed operation at 4 Mhz with standard speed 2114 parts, two switches of DIP Switch 1 are set aside to invert PSYNC through the 74368 tri-state buffer to conditionally drive either XRDY or PRDY low to produce one wait state during a memory cycle which addresses the board.

OCTAL BUFFERS

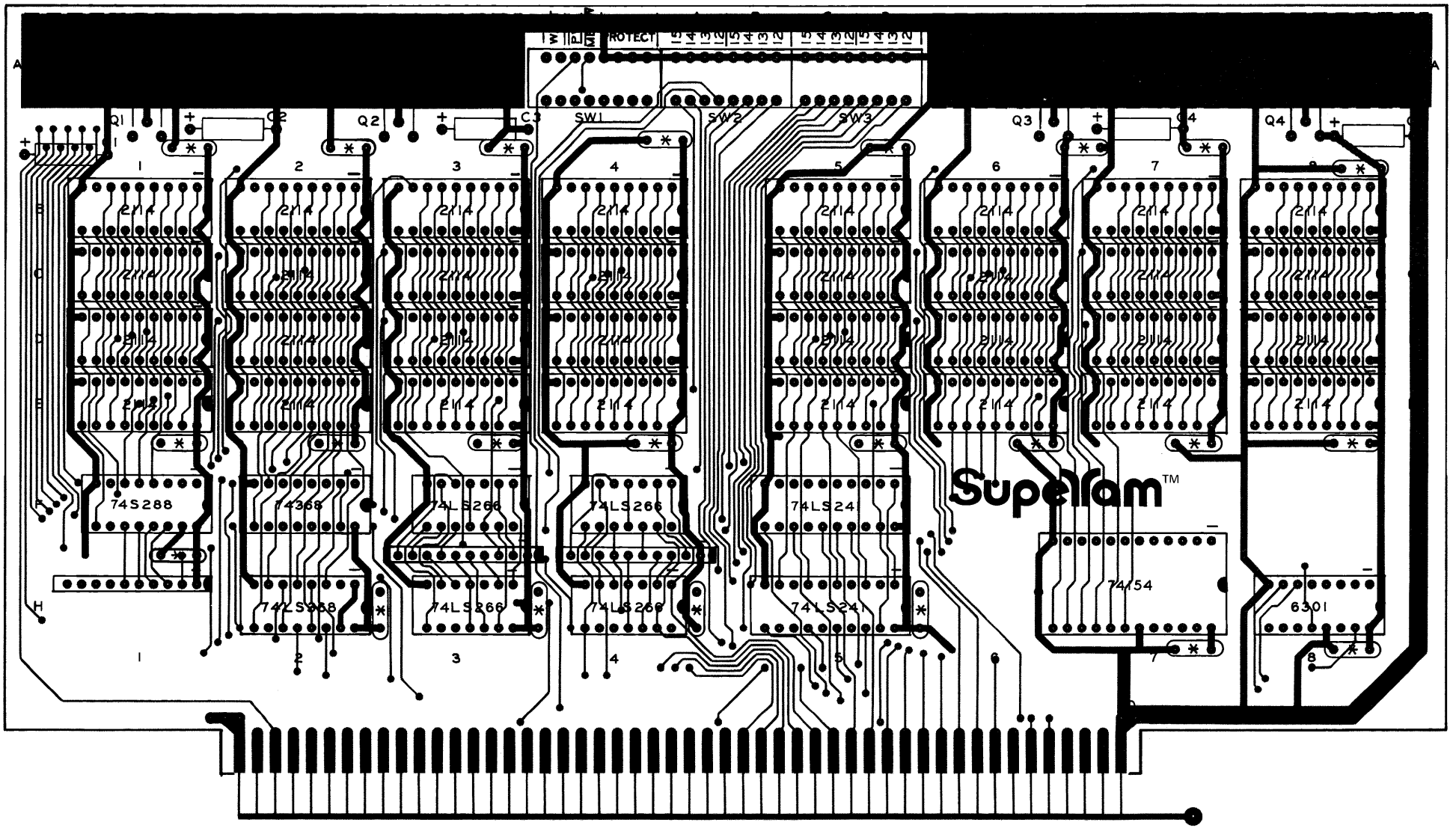
For writing and reading, data buffers containing eight input and output lines are used. These buffers may or may not invert signals, but in SupeRam the buffers are paired so that signals are consistently inverted or not inverted and the 74S288 PROM can be programmed to set enabling at a low or high value.

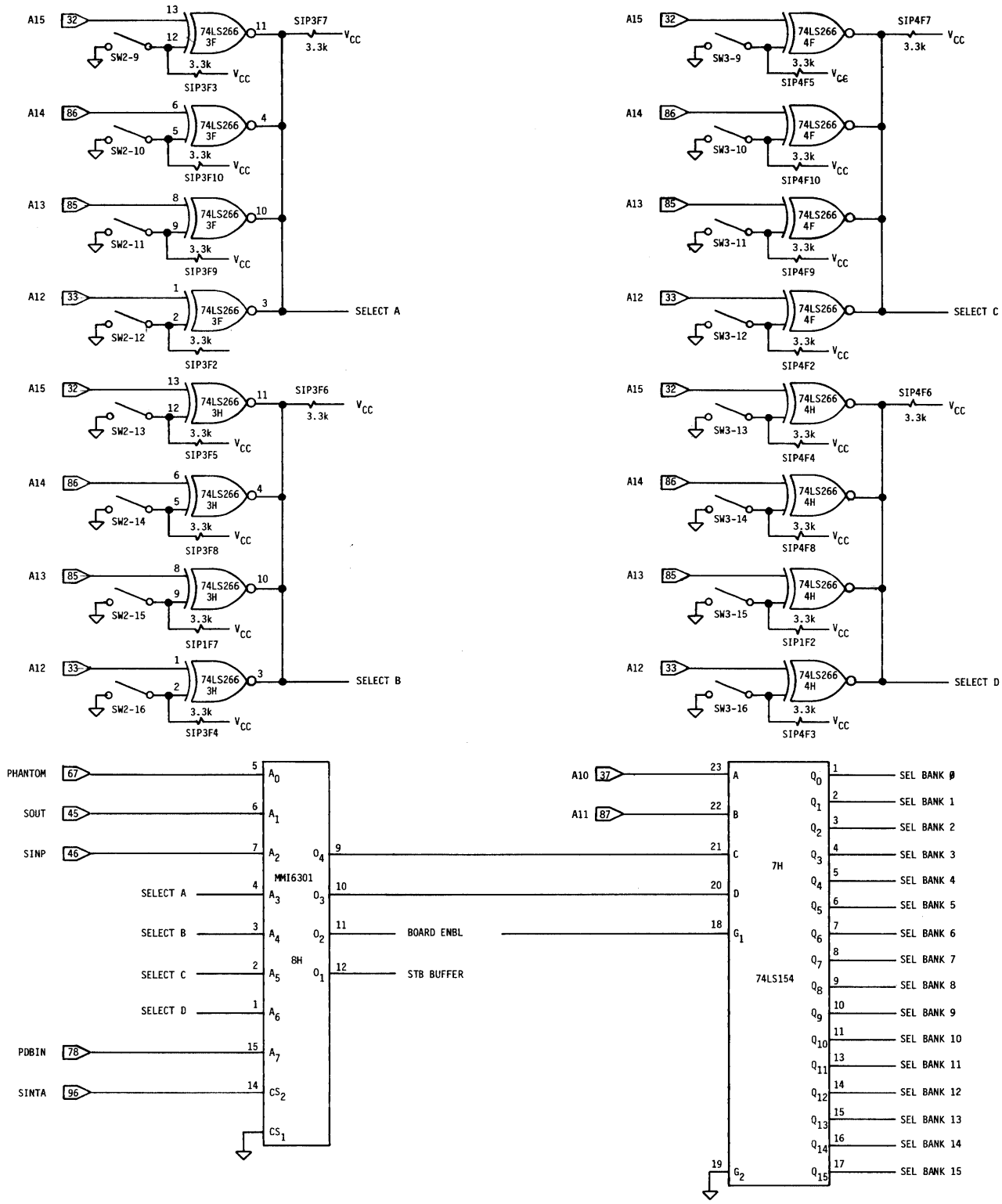
WARRANTY

Parts are warranted to be free from defects in material and workmanship. Defective parts returned postpaid will be exchanged free of charge. SupeRams purchased in kit form are warranted for six months from date of invoice; SupeRams purchased as assembled units are warranted for one year from invoice date. Malfunctioning units will be repaired, tested, and returned with a minimal charge for postage/handling if in the opinion of Morrow's Micro-Stuff or Thinker Toys care has been exercised in their assembly and/or use. Warranty is void if on inspection by Morrow's or Thinker Toys it is found that the product has been subject to improper assembly or abuse. Charges will be assessed accordingly for repair parts and labor if the unit is determined to be repairable. Repair fees will not exceed $25.00 unless prior approval has been obtained from purchaser.

The foregoing warranty is in lieu of all other warranties expressed or implied and in any event is limited to product repair or replacement.

Please note: a registration card is enclosed with each Thinker Toy product; please return to record your warranty.


WRITE PROTECT
SW1
SW2
SW3
Q1
Q2
Q3
Q4
C3
2114
74S288
74368
74LS266
74LS24
74LS241
74154
6301
SuperRam™



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