MORROW DESIGNS

USER'S MANUAL

16K MEMORY MASTER ™

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User's Manual

16K MEMORY MASTER™

INTRODUCTION

The Thinker Toys 16K Memory Master™ is George Morrow's first entry into the field of bank select S-100 memories. Using the popular 2114 static RAM memory array with access time guaranteed to run at 4MHZ, the Memory Master is compatible with most popular S-100 bank select software. This versatile board can be switched to become selected or deselected in response to any bit of any I/O port; to come up active or inactive on power-on/reset; and to honor or ignore PHANTOM. Once selected, Memory Master is configured as four independently addressable and write protectable 4K blocks, with addressing allowed at the beginning of any 4K boundary.

In addition to all this, the 16K Memory Master has a unique and powerful feature: it can be disabled in 16 individual 1K segments. Thus even those who have no need for bank selection as such can use the Memory Master to "plaster up" otherwise hard to fill gaps in their system RAM. It's now a snap to configure, say, a 61 or 63K system, without interfering with ROM up top; or to side-step little islands of firmware floating around in mid-memory, which cause less resourceful RAM boards to flounder.

Of course, the 16K Memory Master also offers the reliability and economy that come with all Morrow designs, as well as service that is unmatched in the industry-- it's another Thinker Toys product you can bank on.

OPERATING INSTRUCTIONS

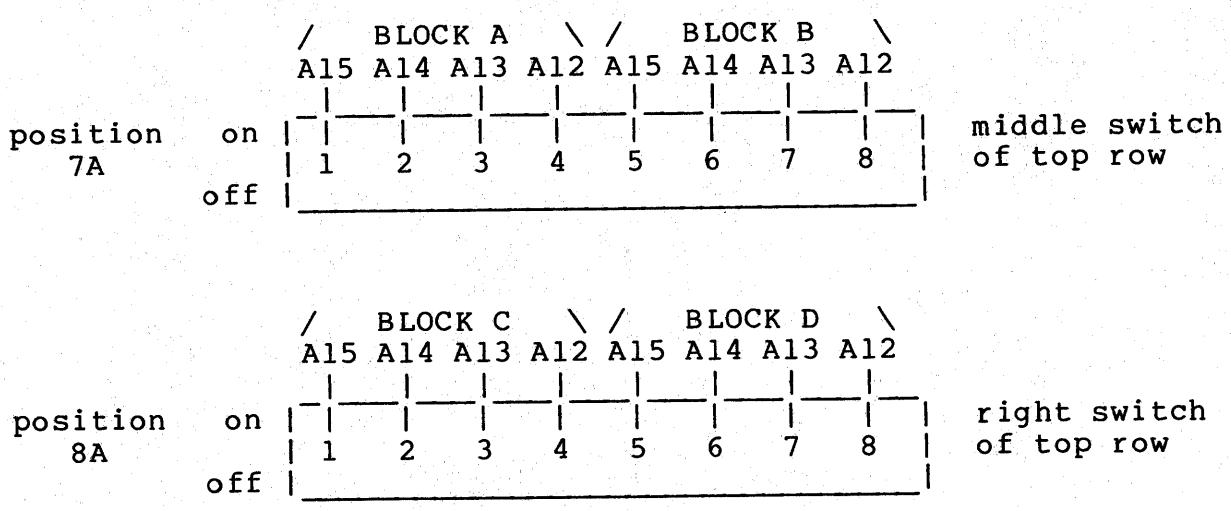
IMPORTANT NOTE: TO AVOID ELECTRICAL DAMAGE TO YOUR MEMORY MASTER BOARD, TURN OFF THE POWER IN YOUR COMPUTER BEFORE INSTALLING OR REMOVING THE BOARD.

MEMORY ADDRESSING

The 16K Memory Master is configured as 4 blocks of 4K bytes each. Each of the 4K blocks can be addressed on a 4K boundary. Thus, a block may begin at 0000H, 1000H, 2000H and so forth up to F000H. The addressing need not be consecutive and may even overlap.

DIP switches 7A and 8A on the top of the circuit board are the address selection switches. Each paddle of these switches either grounds (when set to "on") or pulls high (when set to "off") one input of a 74LS266 Exclusive Nor gate. The other input is one of the four address lines A12 to A15, buffered and inverted by 74LS04's. Sets of four of these 74LS266 equality gates will select their respective 4K memory block if and only if S-100 address lines A12 to A15 correspond exactly to the setting of the appropriate DIP switch. Thus, if the four paddles of the DIP switch controlling block "A" are all set to "off", or high, then the inverted address lines 12 to 15 must also be high (meaning that the actual address lines are low), in order to select block "A". In this case, selection will only occur when memory between 0000H and 03FFH is being addressed.

The diagram below depicts memory selection switches 7A and 8A and shows the correspondence between the paddles and the four 4K blocks of memory which they govern.



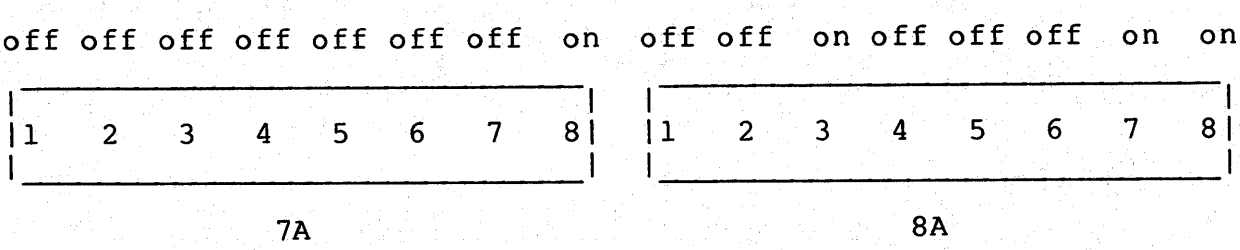
MEMORY ADDRESSING TABLE

The following table shows the relationship between the switch settings of the four addressing paddles controlling a 4K memory block and the starting address of that 4K block. The table applies equally to block A, B, C, or D.

Starting Address		A15	A14	A13	A12	Corresponding	
Hex	Octal					Hex Digit	Binary #
0000	000:000	off	off	off	off	0	0000
1000	020:000	off	off	off	on	1	0001
2000	040:000	off	off	on	off	2	0010
3000	060:000	off	off	on	on	3	0011
4000	100:000	off	on	off	off	4	0100
5000	120:000	off	on	off	on	5	0101
6000	140:000	off	on	on	off	6	0110
7000	160:000	off	on	on	on	7	0111
8000	200:000	on	off	off	off	8	1000
9000	220:000	on	off	off	on	9	1001
A000	240:000	on	off	on	off	A	1010
B000	260:000	on	off	on	on	B	1011
C000	300:000	on	on	off	off	C	1100
D000	320:000	on	on	off	on	D	1101
E000	340:000	on	on	on	off	E	1110
F000	360:000	on	on	on	on	F	1111

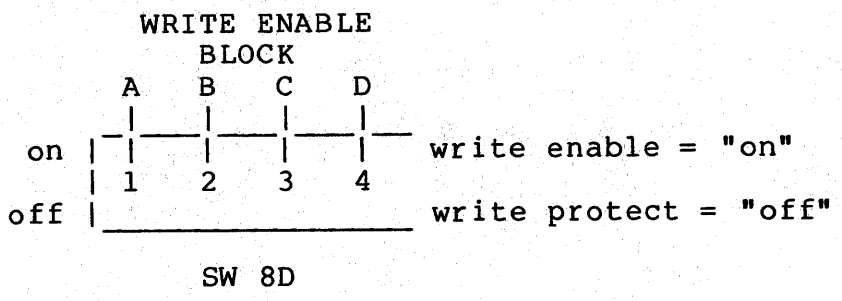
Memory Addressing

As an example of addressing the the Memory Master board, the following switch positions will set the board to the first 16K of memory, starting with Block A at 0000:



WRITE PROTECTION

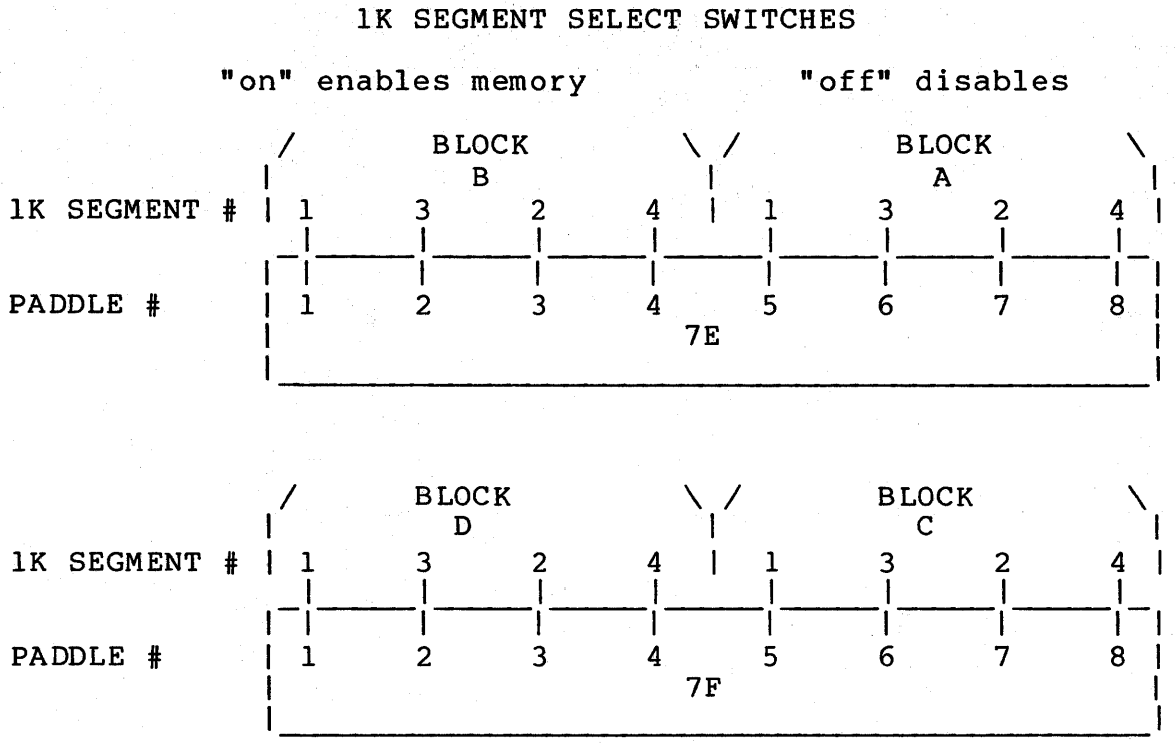
The first four paddles of DIP Switch 8D are the Write Enable switches controlling the four 4K blocks of memory on the Memory Master board. The CPU can write into a 4K block of memory when the paddle associated with that block is in the "on" position. If the paddle is in the "off" position the entire block is protected and cannot be altered. The figure below shows the relationship between paddle position and memory block.



1K MEMORY SEGMENT ENABLE

Individual 1K segments of memory may be enabled or disabled by setting the appropriate paddles on DIP switches 7E and 7F. Each paddle controls a unique 1K segment. The "on" position enables a segment, the "off" position disables it. When a 1K segment is disabled, the memory space to which it is addressed becomes free. Another device on the bus may address RAM or ROM in the same space without posing any conflict. The RAM chips themselves which make up the disabled segment may be removed.

The figure below shows which 1K segment of which 4K block of RAM is controlled by each paddle on DIP switches 7E and 7F. The 4K blocks are labeled A, B, C, or D; the 1K segments within each block are labeled 1, 2, 3, or 4.



Thus, to disable the 3rd 1K segment of Block "C", for example, paddle 6 of DIP Switch 7F should be placed in the "off" position.

The table below lists, in ascending order, the 64 1K segments and their relative positions within a 4K block of memory.

1K Memory Segment Enable

1K SEGMENT TABLE

REL POS	OCTAL INTERVAL	HEX INTERVAL	REL POS	OCTAL INTERVAL	HEX INTERVAL
1	000:000-003:377	0000-03FF	1	200:000-203:377	8000-83FF
2	004:000-007:377	0400-07FF	2	204:000-207:377	8400-87FF
3	010:000-013:377	0800-0BFF	3	210:000-213:377	8800-8BFF
4	014:000-017:377	0C00-0FFF	4	214:000-217:377	8C00-8FFF
1	020:000-023:377	1000-13FF	1	220:000-223:377	9000-93FF
2	024:000-027:377	1400-17FF	2	224:000-227:377	9400-97FF
3	030:000-033:377	1800-1BFF	3	230:000-233:377	9800-9BFF
4	034:000-037:377	1C00-1FFF	4	234:000-237:377	9C00-9FFF
1	040:000-043:377	2000-23FF	1	240:377-243:377	A000-A3FF
2	044:000-047:377	2400-27FF	2	244:000-247:377	A400-A7FF
3	050:000-053:377	2800-2BFF	3	250:000-253:377	A800-ABFF
4	054:000-057:377	2C00-2FFF	4	254:000-257:377	AC00-AFFF
1	060:000-063:377	3000-33FF	1	260:000-263:377	B000-B3FF
2	064:000-067:377	3400-37FF	2	264:000-267:377	B400-B7FF
3	070:000-073:377	3800-3BFF	3	270:000-273:377	B800-BBFF
4	074:000-077:377	3C00-3FFF	4	274:000-277:377	BC00-BFFF
1	100:000-103:377	4000-43FF	1	300:000-303:377	C000-C3FF
2	104:000-107:377	4400-47FF	2	304:000-307:377	C400-C7FF
3	110:000-113:377	4800-4BFF	3	310:000-313:377	C800-CBFF
4	114:000-117:377	4C00-4FFF	4	314:000-317:377	CC00-CFFF
1	120:000-123:377	5000-53FF	1	320:000-323:377	D000-D3FF
2	124:000-127:377	5400-57FF	2	324:000-327:377	D400-D7FF
3	130:000-133:377	5800-5BFF	3	330:000-333:377	D800-DBFF
4	134:000-137:377	5C00-5FFF	4	334:000-337:377	DC00-DFFF
1	140:000-143:377	6000-63FF	1	340:000-343:377	E000-E3FF
2	144:000-147:377	6400-67FF	2	344:000-347:377	E400-E7FF
3	150:000-153:377	6800-6BFF	3	350:000-353:377	E800-EBFF
4	154:000-157:377	6C00-6FFF	4	354:000-357:377	EC00-EFFF
1	160:000-163:377	7000-73FF	1	360:000-363:377	F000-F3FF
2	164:000-167:377	7400-77FF	2	364:000-367:377	F400-F7FF
3	170:000-173:377	7800-7BFF	3	370:000-373:377	F800-FBFF
4	174:000-177:377	7C00-7FFF	4	374:000-377:377	FC00-FFFF

As an example of using the above table, suppose one has an S-100 main frame with a Thinker Toys Disk Jockey 2D double density controller board with on-board ROM and RAM occupying memory space from E000H to E7FFH (340:000Q - 347:377Q). With a 16K Memory Master board addressed as the last 16K of memory with Blocks A through D addressed consecutively, the table indicates that Block C should have its first two 1K segments disabled which means that paddles 5 and 7 of switch 7F should be in the "off" position to make room in memory for the controller board. Of course, if one of the 2114 RAM chips on the disk controller board should go bad, one of the displaced RAM chips on the Memory Master board could be used to replace it (see "RAM IC LOCATION CHART" for how to locate the physical RAM chips of a givin segment).

RAM IC LOCATION CHART

The chart below can help locate the physical position on the Memory Master board of a RAM IC known only by its relative address. By relative address is meant the RAM's position in a given 4K block of memory. The low order byte of the second 1K segment of Block C, for example, is indicated on the chart by "C-2 lo". The letters outside and to the left of the RAM grid are the same as appear on the silk screened legend on the Memory Master board. These letters apply to the horizontal row location of chips within the RAM array only-- IC's to the right of this array are identified as to row by the silk screened letters on the extreme right side of the Memory Master board. Note that these two sets of letters do not correspond. Vertical columns are, on the other hand, identified by a single common set of numbers running accross both the top and bottom of the circuit board.

RAM IC LOCATION CHART

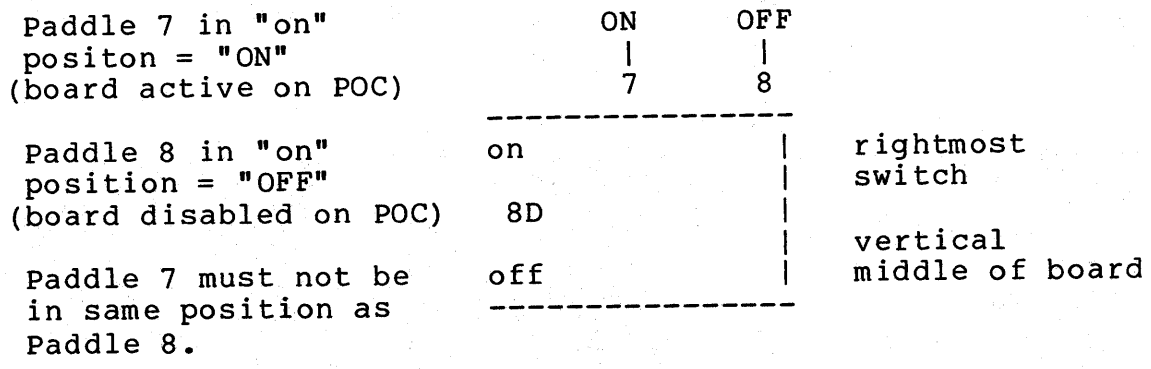
	1		2		3		4	
	lo	hi			lo	hi		
A	A-1				B-1			
	lo	hi			lo	hi		
B	A-3				B-3			
	lo	hi			lo	hi		
C	A-2				B-2			
	lo	hi			lo	hi		
D	A-4				B-4			
	lo	hi			lo	hi		
E	C-1				D-1			
	lo	hi			lo	hi		
F	C-3				D-3			
	lo	hi			lo	hi		
G	C-2				D-2			
	lo	hi			lo	hi		
H	C-4				D-4			

COMING UP ENABLED OR DISABLED ON POWER-ON-CLEAR/RESET

Paddles 7 and 8 of DIP switch 8D control whether the Memory Master will come up active or inactive on Power-On-Clear/Reset. Paddle 7 is the "ON" switch, and paddle 8 is the "OFF" switch. "ON" in this case means that the board will be active on Power-On-Clear/Reset (hereafter called simply POC); "OFF" means the board will come up inactive on POC. For the "ON" option, set paddle 7 to the "on" position, and paddle 8 to the "off" position. For the "OFF" option, set paddle 7 to the "off" position and paddle 8 to the "on" position. In no case should paddles 7 and 8 of DIP switch 8D be set to the same position.

The figure below depicts the "ON" and "OFF" switches of DIP switch 8D.

"ON"/"OFF" OPTION SWITCH



BOARD SELECT BY I/O ADDRESS-- BANK SELECTION

The purpose of "Bank Selection" is to allow more memory in a system than the CPU can normally address. This is accomplished by assigning a board not only a memory address somewhere within the 64K range of addressable memory, but also an I/O port number between Ø and 255. Thus two boards can share the same memory address, yet have a different I/O address. If a system software scheme takes care to disable one board (by outputting an appropriate byte to the board's I/O port number) before enabling another board (again by outputting the proper byte to its port number), many memory boards can occupy the same memory space without causing any conflict.

With the Memory Master board, two assigments must be made for each board in order to operate under a bank select scheme. First, an I/O port number must be decided upon; and second, a bit within that port must be chosen to act as a switch to enable the board or disable it when a byte is written to the I/O port in question. If, for example, a board is assigned I/O port number 4ØH, and further assigned data bit Ø of that port, then the board will be activated by an OUT 4ØH CPU instruction if the CPU's accumulator has bit Ø set. Conversely , the same board will be disabled by an OUT 4ØH instruction if bit Ø of the accumulator is cleared at the time the instruction is executed. In either case the board will remain selected or deselected until anoter OUT 4ØH instruction changes its state or until a Power-On-Clear or Reset takes place. POC will select or deselect the board according to the setting of paddles 7 and 8 on DIP switch 8D, as described above.

Dip Switch 6A, the leftmost switch on the Memory Master board, controls the selection of the I/O port number to which the board is assigned. Paddles 1 through 8 on this switch may be thought of as representing the 8 address bits of the I/O port, with paddle 1 representing bit 7, paddle 2 bit 6, and so on through paddle 8 representing bit Ø. This is depicted below.

I/O PORT ADDRESSING--SWITCH 6A

	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR Ø
	|	|	|	|	|	|	|	|
Paddle	1	2	3	4	5	6	7	8

A paddle in the "off" position can be taken as a cleared bit, while a paddle in the "on" position sets the bit. Thus, turning all the paddles on switch 6A to the "off" position addresses the Memory Master board to I/O port Ø. Turning all the switches "on" addresses the board to device 255 (FF Hex or 377 Octal). To set the board to, say, 4ØH, the following setting should be used:

Bank Selection--I/O Port Address

Example-- Setting Memory Master to I/O Port 40H

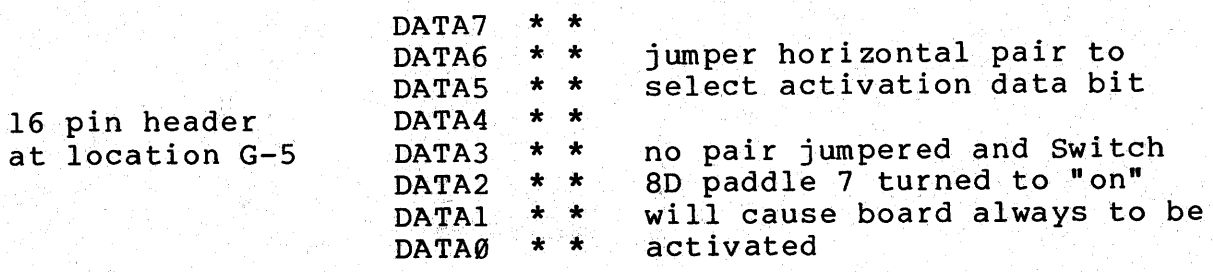
Paddle	1	2	3	4	5	6	7	8
	off	on	off	off	off	off	off	off

BOARD SELECTION BY BIT

Once the I/O port number of the Memory Master board has been determined, there remains the selection of the data bit which will activate or de-activate the board during OUT instructions to the proper port.

The sixteen pin header at location G-5 on the circuit board, just by the lower right corner of the RAM array, is used to assign the board selection data bit. The silk screened legend names the bottom pair of pins "DATAØ" and the top pair "7". By jumpering one of the horizontal pairs of pins with the slide-on jumper included with the Memory Master board, the user can select the corresponding bit to activate or de-activate the board. The 16 pin header G-5 is shown below with all pairs numbered.

DATA BIT JUMPER SELECTION



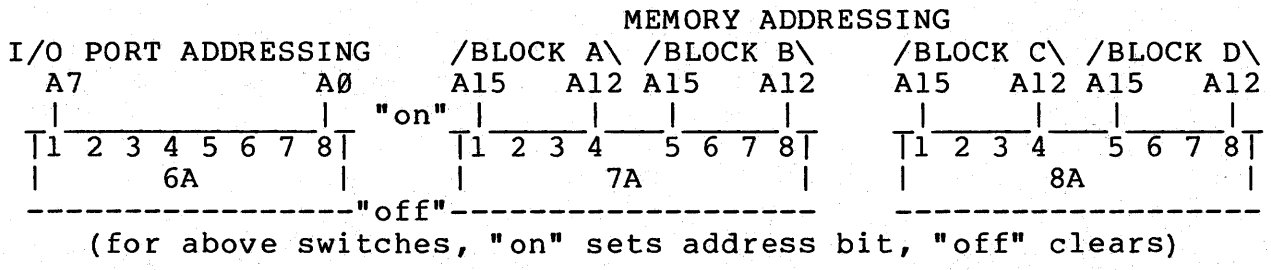
As an example, with the lowest pair of pins jumpered, and the board addressed as I/O port 40H, any OUT 40H instruction with data bit Ø set will activate the board, while any OUT 40H instruction with data bit Ø cleared will de-activate the board. In other words, an OUT 40H with, say, a 71H in the accumulator will select, while an OUT 40H with a 72H will de-select.

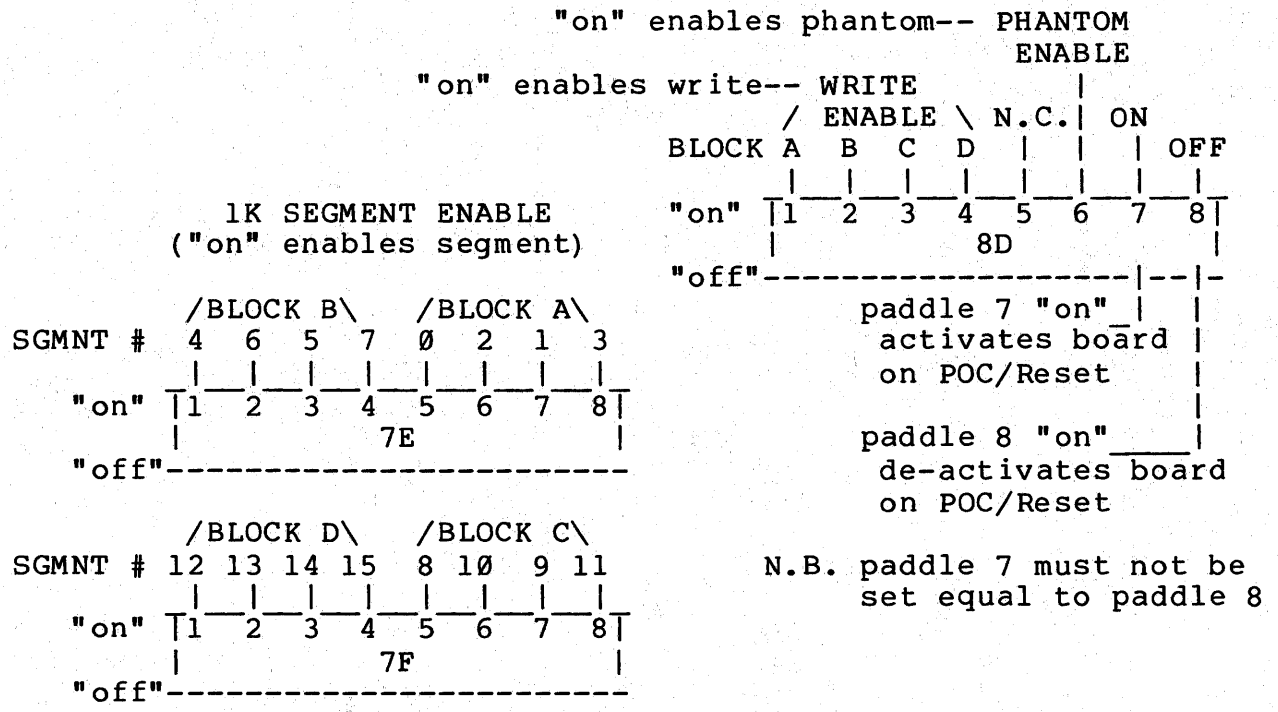
The fact that any bit can used as the board select/de-select bit means that it is possible to have 256 (the number of possible I/O ports) times 8 (the number of possible data bits) 16K Memory Master boards in a system at one time without presenting an addressing conflict. This should be sufficient for most applications. Note that, as indicated in the above illustration, the Memory Master can be used as a conventional 16K memory board which pays no attention to any I/O commands. Simply do NOT jumper any pair of pins on the header at G-5, set DIP Switch 8D paddle 7 to "on" and set Switch 8D paddle 8 to "off". This will cause the board to come up selected and prevent any bit from de-selecting it, regardless of I/O port addressing.

PHANTOM ENABLE

Paddle 6 of DIP Switch 8D is the Phantom Enable switch. If this switch is in the "on" position, the Memory Master board will become de-activated when PHANTOM, line 67 of the S-100 bus, is asserted (brought low). When paddle 6 is in the "off" position, the Memory Master will not respond to the PHANTOM line.

SUMMARY OF SWITCH SETTINGS AND FUNCTIONS





16K MEMORY MASTER PARTS LIST

[ ]	1	5" x 1Ø" printed circuit board	
[ ]	6	3.3K SIP resistor packs	
[ ]	25	Disk by-pass capacitors-- may vary in value from .Ø1 to .1 microfarads depending on current supplies.	
[ ]	6	1.8 microfarad tantalum capacitors	
[ ]	6	8 position DIP switches	
[ ]	3	Heat sinks	
[ ]	3	78Ø5 positive 5 volt regulators	
[ ]	3	Machine nuts and screws	
[ ]	1	16 pin DIP header	
[ ]	1	Slide-on jumper	
[ ]	16	14-pin low profile IC sockets	
[ ]	4	16-pin "	
[ ]	32	18-pin "	
[ ]	1	24-pin "	
[ ]	1	74LSØØ quad 2-input NAND gate	9D
[ ]	1	74LSØ2 quad 2-input NOR gate	9C
[ ]	3	74LSØ4 hex inverter	5C,6D,7D
[ ]	2	743Ø/LS3Ø 8-input NAND gate	6E,6F
[ ]	2	74LS32 quad 2-input OR gate	9B,9E
[ ]	1	74LS74 dual D-type flip flop	9G
[ ]	1	74154/74LS154 1 of 16 decoder	8F
[ ]	6	74LS266 quad Exclusive Nor gate	6B,6C,7B,7C,8B,8C
[ ]	3	74LS367 hex tri-state buffers	6G,7G,8G
[ ]	32	2114 4 x 1K static RAMS	1A through 4H
[ ]	1	6331 8 x 32 PROM	8E

WARNING! IMPROPER ASSEMBLY OF THIS KIT WILL VOID THE WARRANTY. READ THESE INSTRUCTIONS CAREFULLY BEFORE ATTEMPTING TO CONSTRUCT THIS KIT

INVENTORY

Make sure that all parts listed in the Parts List have been included. Notify Thinker Toys immediately if any are missing. Also, quickly return all extra parts.

USE SOCKETS

Sockets are provided for every IC on the 16K Memory Master.

NO REPAIR WORK WILL BE ATTEMPTED ON ANY RETURNED BOARD WITH ANY IC SOLDERED DIRECTLY TO THE CARD

ORIENTATION

When this manual refers to the bottom of the circuit board it means the edge with the gold S-100 edge connectors. Right and left assume a view from the component side of the board which has the silk screened parts legend.

All IC sockets will either have their pins numbered or have a 45 degree angle across the corner of pin one. On the 16K Memory Master, all sockets and all IC's have pin 1 closest to the bottom left corner of the board.

The 1.8 microfarad capacitors are polarized. This capacitor's positive lead is identified by a circular "tit" where it enters the body of the housing. The silk screen identifies the positive lead of these axial parts with a "+" sign. The by-pass caps, identified on the silk screened legend by an asterisk "*" enclosed by an oval, are not polarized.

The six DIP switch arrays are to be positioned so that the letters and numbers stamped on them are right side up-- i.e., their paddles run from left to right, 1 to 8.

The SIP resistor packs, historically prone to being inserted backwards, should have their white dot nearest the white dot on their respective legends. This turns out to be up for the two

3.3k Ohm packs in the center of the board, and to the left for the 3.3K Ohm packs just below the three DIP switches at the top of the board.

EXAMINE THE BOARD

Visually examine the circuit board for any trace opens or shorts. A concentrated five minute scrutiny will uncover most trace defects. Several hours of scattered, unconcentrated scrutiny generally won't reveal anything. Take special care that no shorts or opens exist on those areas of the circuit board that will be covered by IC sockets. Ohm out any suspicious looking traces for either shorts or discontinuity as appropriate. Return immediately any bare board found to be flawed. Such boards will be replaced under warranty.

SOLDERING AND SOLDER IRONS

The most desirable soldering tool for complex electronic kits is a constant temperature iron with an element regulated at 650 degrees F. The tip should be fine so that it can be brought into close contact with the pads of the circuit board. Such irons are available from Weller and Unger and should be part of any electronics shop.

There are three important soldering requirements for building this kit:

1. Do not use an iron that is too cold (less than 600 degrees F) or too hot (more than 750 degrees F).
2. Do not hold the iron against a pad for more than about six seconds.
3. Do not apply excessive amounts of solder.

The recommended procedure for soldering components to the circuit board is as follows:

1. Bring the iron in contact with BOTH the component lead AND the pad.
2. Apply a SMALL amount of solder at the point where the iron, component lead, and pad ALL make contact.
3. After the initial application of solder has been accomplished with the solder flowing to the pad and component lead, the heat of the iron will have transferred to BOTH the pad AND lead. Apply a small amount of additional solder to cover the joint between the pad and the lead. DO NOT PILE SOLDER ON THE JOINT! EXCESSIVE HEAT AND SOLDER CAUSE PADS AND LEADS TO LIFT FROM THE CIRCUIT BOARD. EXCESSIVE SOLDER IS THE PRIMARY CAUSE FOR BOARD SHORTS AND BRIDGED CONNECTIONS.

PROTECT YOUR EYES WHEN YOU CLIP COMPONENT LEADS AFTER SOLDERING

[ ] Install and solder the 24 pin socket first, then the 18, 16, and 14 pin sockets in that order. By installing the sockets in this order, a smaller sized socket will never be placed in a larger sized position.

[ ] Install and solder the SIP resistor pack arrays. The top packs should have their white dots to the left while the center packs will have their white orientation dots closer to the top of the circuit board.

[ ] Install and solder the 6 axial lead 1.8 microfarad capicators. These have their "+" leads towards the bottom of the circuit board. Clip the excess leads from the parts.

[ ] Install and solder the six DIP switch arrays. Switch 1 of each DIP should be positioned toward the top left corner.

[ ] Install, solder, and clip the leads of the 25 by-pass capacitors whose positions are identified by an oval with an asterisk "*" in the middle.

[ ] Bend the leads of the three 78Ø5 regulators and insert them in the circuit board. Place a separate, finned heat sink between the regulator and the board, work a screw from the back of the board through the board, heat sink, and regulator and hand tighten into the nut on top of the regulator. Solder the leads and adjust the wings of the separate heat sink and, finally, tighten the screw.

[ ] Install and solder the 16 pin DIP header just by the lower right corner of the RAM array-- at location 5G. Make sure that the shorter pins pass through the circuit board.

CLEAN AND EXAMINE THE BOARD

Use flux cleaner to remove solder rosin residue. Examine the circuit board carefully for shorts, solder bridges, or missed pins.

HOW TO FIND WHERE TO PLACE PARTS

For parts placement, please see the silk screened legend on the printed circuit board and the 8" x 1Ø" photograph. IC's may vary from those marked on the silk screened legend if they are listed as alternate IC's (following a slash) in the Parts List.

DO NOT INSERT ANY IC'S IN THEIR SOCKETS AT THIS TIME

Before inserting any IC in its socket perform the following check-out procedure:

1. Re-check the back of the board for solder shorts and bridged connections and for pins of IC sockets that have not been soldered. These unsoldered pins can cause aggravating intermittant probems if overlooked.

2. Re-check components for orientation and make sure all components to be soldered have been soldered.

3. With an ohm meter, check for shorts between the regulated 5 volts and ground. (Regulator output pins are on the right side of the regulator.) Check for shorts between S-100 pin 1 or 51 (+8v) and ground. S-100 pins 50 and 100 are ground.

4. Place the board WITHOUT IC's into an empty system bus slot and power up. In case of smoke, power down immediately and investigate.

5. With a VOM or scope, check the regulators for +5V. Check for Vcc and ground on all IC sockets. If everything is OK, power down and proceed to the next step.

IC INSERTION

If an IC insertion tool is not available, IC leads should be straightened a ROW at a time, not by the individual PIN. The edge of a straight sided table is an excellent device for this operation. Hold the IC by the plastic case, place one row of legs against a flat surface and push very slightly. Repeat with the opposite row. Continue this procedure until the legs of the IC can be inserted with minimum effort into its socket.

When inserting an IC into its socket, take care that you DO NOT BEND THE IC'S LEGS UNDERNEATH ITS PLASTIC PACK. This is an extremely common error and can escape even a fairly careful visual inspection.

If IC pins become bent under during insertion, use a long nose pliers to straighten them and try again. When removing an IC from its socket, use an IC remover, an IC test clip (another must for any electronics shop) or a miniature screw driver. DO NOT ATTEMPT TO REMOVE AN IC WITH YOUR FINGERS. You will bleed on severely bent pins.

PARTS INSTALLATION

Once all IC's have been inserted, re-check for bent pins. Then check twice for proper orientation. Upside down IC's are generally destroyed upon power up.

IF FOR ANY REASON IT BECOMES NECESSARY TO REMOVE A COMPONENT WHICH HAS BEEN SOLDERED TO THE CIRCUIT BOARD, CLIP ALL LEADS BEFORE REMOVING. THIS WILL REDUCE THE CHANCE OF LIFTING PADS OFF TRACES.

POWER UP

If all previous checks have been performed, you are ready to put power to your fully populated board. In an empty system with power off, insert the Memory Master and power up. If the board smokes, power down and investigate. If not, measure the regulated voltages again.

If any voltages have been lost since powering up the bare board, power down and check for upside down IC's. Isolate the possible faulty chip or chips by powering down, removing a section of IC's, and powering up again. Continue this sequence until the faulty IC or IC's are found.

BE SURE NEVER TO INSERT OR REMOVE A BOARD WITH POWER ON! THIS MAY DAMAGE THE BOARD

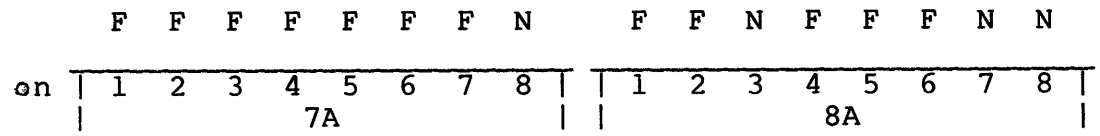
This completes the initial check-out of your Memory Master.

STATIC TEST

Set Up

In order to check-out the operation of the 16K Memory Master board, first configure the board to function as a simple 16K memory addressed as the first 16K of RAM, that is, from 0000H - 3FFFH. This can be accomplished through the following switch settings:

- Set Memory Addressing switches 7A and 8A as below--



where "F" = off and "N" = on. This represents 0000H - 3FFFH.

- Set board to ON (to appear active on POC/Reset) by turning paddle 7 of DIP switch 8D to "on" and paddle 8 of 8D to "off".

- Set board to enable write operations by placing paddles 1, 2, 3 and 4 of DIP switch 8D all "on".

- Set board to ignore PHANTOM by placing paddle 6 of switch 8D "off".

- Set board to I/O port 40H (100:000Q) by setting paddle 2 of DIP switch 6A to "on", and setting the remaining 7 paddles of switch 6A to "off".

- Do not place the slide-on jumper anywhere on the 16 pin DIP header.

- Enable every 1K segment by setting all paddles of DIP switches 7E and 7F to "on".

TEST 1: Memory Addressing and Write Protection

In a system with no memory occupying the first 16K and with power turned OFF, place the Memory Master board with paddles configured as indicated above. Power up.

With a front panel or monitor, (the front panel MUST generate the S-100 status signal SWO during memory deposits) examine location 0000H. Write 00 in this location, and re-examine it to be sure that it now contains a 00. Now deposit FFH (377Q) in this location and read it back. Set paddle 1 of DIP switch 8D to "off", and attempt to change the FF in location 0000 to any other number-- you should not be able to write into this location. Set 8D paddle 1 back to "on". Make sure you can now write to 0000.

TEST 2: 1K Segment Disable

Deposit a ØØ in location ØØØØ again. Set paddle 5 of DIP switch 7E to "off". Re-examine location ØØØØ. It should read FF and you should not be able to change this data. Set paddle 5 of 7E back to "on" and make sure that you can again deposit data into ØØØØ.

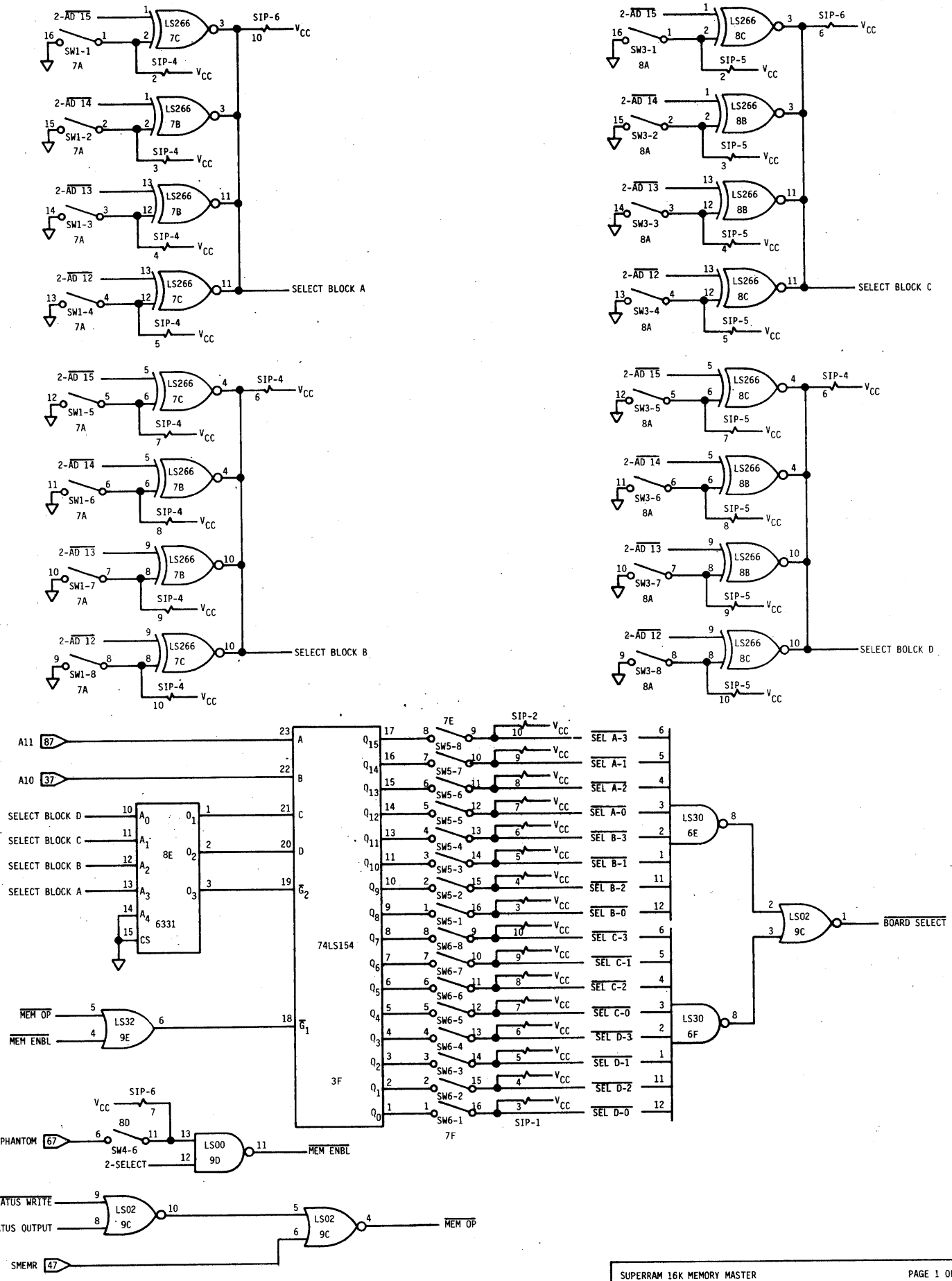
TEST 3: Bank Selection

Place the slide-on jumper across the two pins labeled "DATAØ" on the 16 pin DIP header at location G-5. With a Ø in the CPU's accumulator, execute an OUT 4ØH command. You should now have lost access to the Memory Master board. Now execute an OUT 4ØH command with a 1 in the CPU's accumulator. The Memory Master should now be re-enabled.

TEST 4: POC/Reset-- ON/OFF

With a jumper still across "DATAØ" of the 16 pin header, make sure that you can access the board. Reset the system and verify that you can still access the board. Now set paddle 7 of DIP switch 8D to "off" and paddle 8 of 8D to "on". Reset the system. The Memory Master board should now be disabled. Execute an OUT 4Ø instruction with a 1 in the CPU's acumulator. This should re-activate the Memory Master.

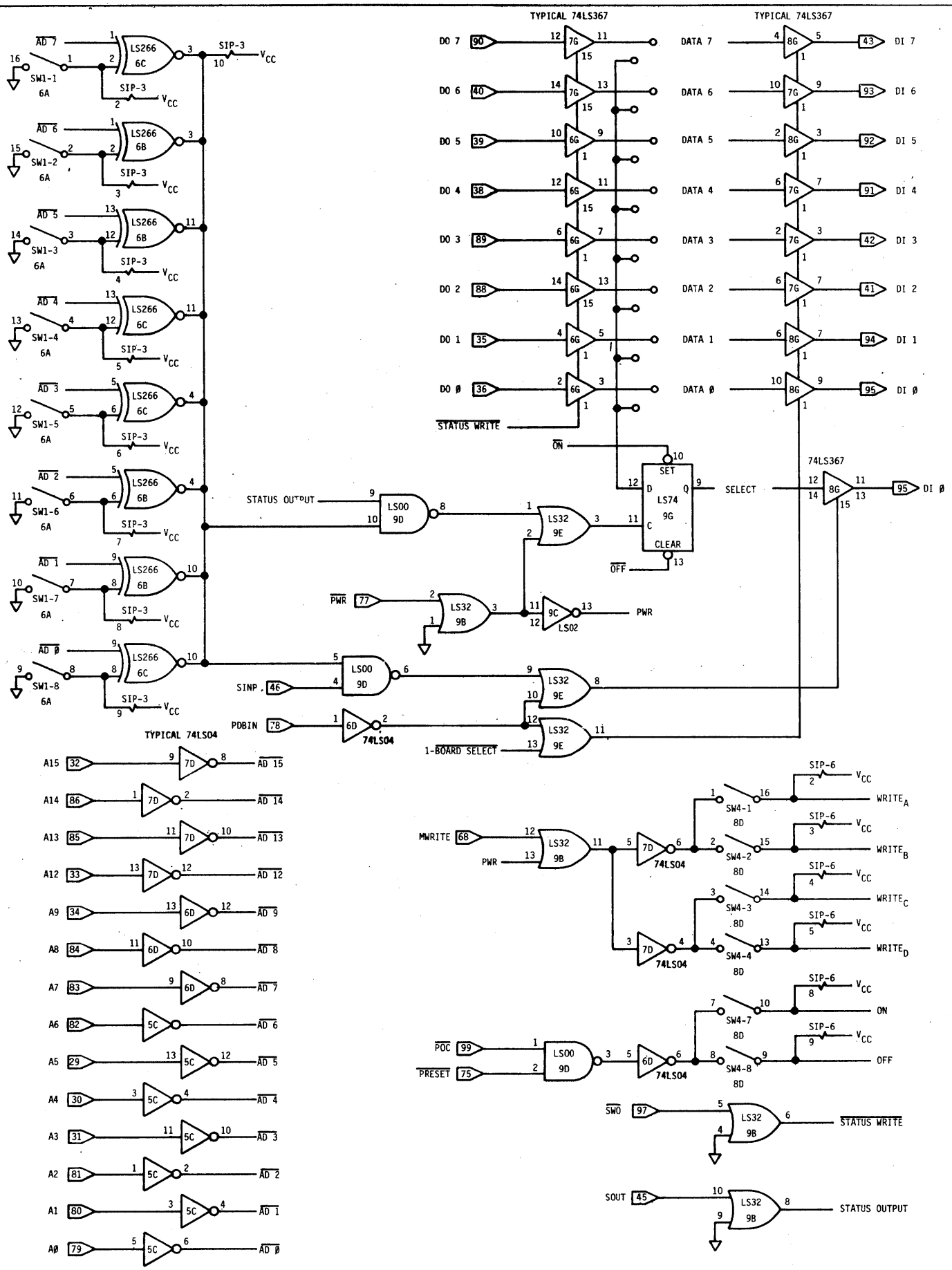
This completes the static system test. The following pages contain a full fledged memory diagnostic.



SUPERRAM 16K MEMORY MASTER

PAGE 1 OF 3

BOARD SELECT LOGIC & BANK SELECT LOGIC



SUPERRAM 16K MEMORY MASTER

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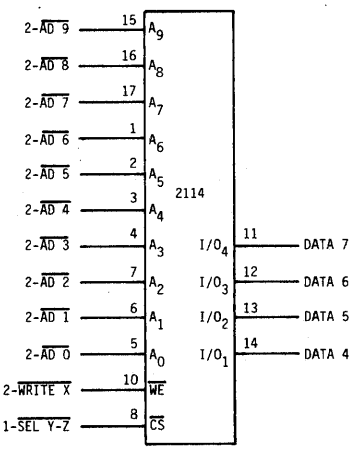
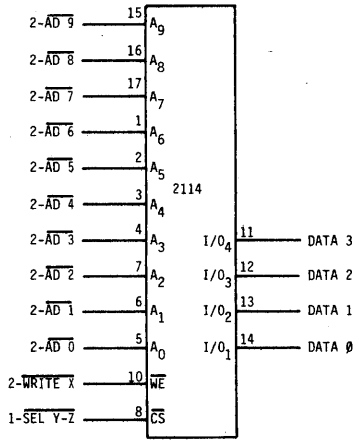
I/O SELECTION, DATA & ADDRESS BUFFERS

	LOW DATA 1	HIGH DATA 2	LOW DATA 3	HIGH DATA 4	
A	SECTION A BLOCK 0	SECTION A BLOCK 0	SECTION B BLOCK 0	SECTION B BLOCK 0	A
B	SECTION A BLOCK 2	SECTION A BLOCK 2	SECTION B BLOCK 2	SECTION B BLOCK 2	B
C	SECTION A BLOCK 1	SECTION A BLOCK 1	SECTION B BLOCK 1	SECTION B BLOCK 1	C
D	SECTION A BLOCK 3	SECTION A BLOCK 3	SECTION B BLOCK 3	SECTION B BLOCK 3	D
E	SECTION C BLOCK 0	SECTION C BLOCK 0	SECTION D BLOCK 0	SECTION D BLOCK 0	E
F	SECTION C BLOCK 2	SECTION C BLOCK 2	SECTION D BLOCK 2	SECTION D BLOCK 2	F
G	SECTION C BLOCK 1	SECTION C BLOCK 1	SECTION D BLOCK 1	SECTION D BLOCK 1	G
H	SECTION C BLOCK 3	SECTION C BLOCK 3	SECTION D BLOCK 3	SECTION D BLOCK 3	H





SEL A-0, SEL A-1, SEL A-2, SEL A-3 GO WITH WRITE A
SEL B-0, SEL B-1, SEL B-2, SEL B-3 GO WITH WRITE B
SEL C-0, SEL C-1, SEL C-2, SEL B-3 GO WITH WRITE C
SEL D-0, SEL D-1, SEL D-2, SEL D-3 GO WITH WRITE D

MEMORY ARRAY LAYOUT AND TYPICAL BLOCK OF THE ARRAY