IBM Field Engineering

Manual of Instruction

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Z22-2798-1

Solid Logic Technology

Component Circuits

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Manual of Instruction

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Solid Logic Technology

Component Circuits

Preface

This manual describes Solid Logic Technology (SLT) circuits and their relation to Automated Logic Diagrams (ALD's). It is to be used in conjunction with the Field Engineering Manual of Instruction *SLT Packaging,* Form Z22-2800

The major sections of this book are:

Symbology and Definitions, which illustrates and defines the ALD logic block.

Automated Logic Diagrams (ALD's), which explains ALD terminology and layout.

SLT Circuits, which shows the basic parameters of SLT circuits. The basic SLT circuit is the AND-OR-inverter. The section contains a brief circuit description and schematic of the general SLT circuits.

Card Layout, which explains the SLT card, the card ALD sheet, assembly drawing, and schematic.

Circuit Numbers, which is a list of circuit numbers, including representative examples of different types of circuits.

Modules, which shows the schematic of the modules in part-number order.

This manual, Form Z22-2798-1, is a major revision which obsoletes the former edition, Form Z22-2798-0. The circuit descriptions are rearranged; the circuit number list is updated; and the examples are changed to represent both the circuit descriptions and the modules. The cross-referencing between sections is increased and the index expanded.

Revisions to text are indicated by a vertical line to the left of the change; revised illustrations are denoted by the symbol • to the left of the caption.

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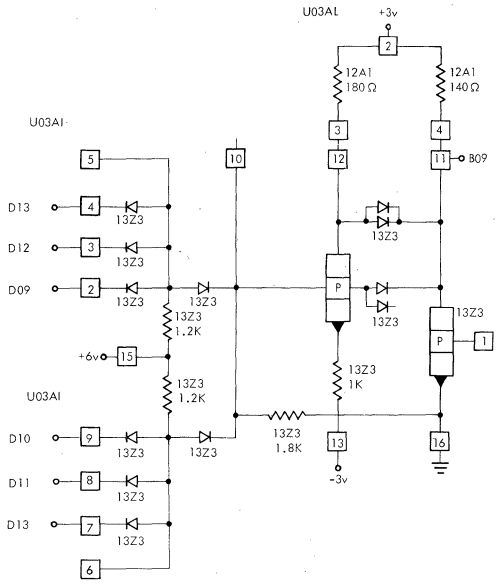
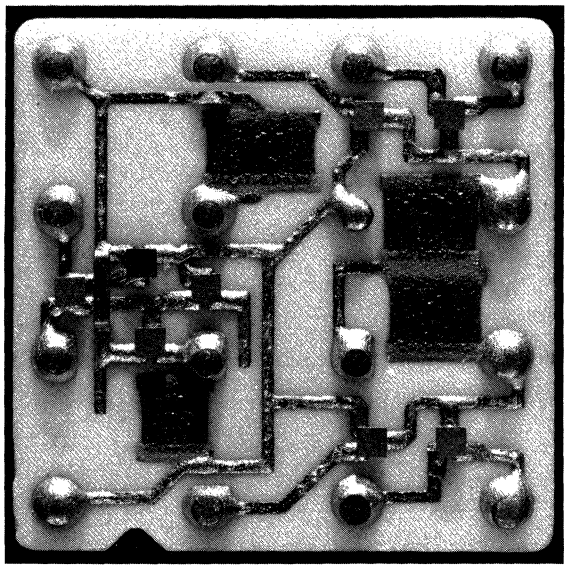
Contents

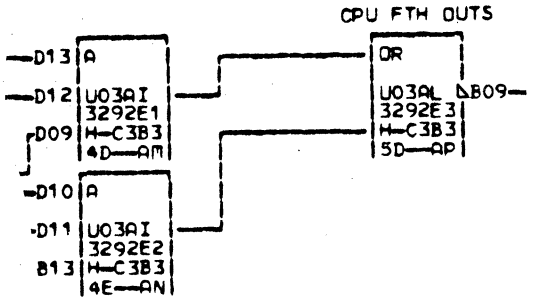
Illustrations

Abbreviations

A	AND
A	AND Circuit
A-2, A-3	Threshold
ACT	AC Trigger
AI	AND-Inverter
AIT	AND-Inverter-Terminate
ALD	Automated Logic Diagram
AOI	AND-OR-Inverter
AOPI	AND-OR-Power-Inverter
AOPX	AND-OR-Power-Extender
AOX	AND-OR-Extender
API	AND-Power-Inverter
AR	Amplifier
Array	Array
C	Capacitor
CABL	Cable
CD	Core Driver
Chan	Channel
Cl	Cell
Clk	Clock
CR	Diode
CS	Current Switch
Ctrl	Control
Ctr	Counter
CV	Converter
D	Driver
DCI	Direct Coupled Inverter
DL	Delay Line
DLD	Delay Line Driver
Dly	Delay
ENTR	Entrance from Machine Type
EVEN	Even Count
EXIT	Exit to Machine Type
FDD	Four Dual Diodes
FF	Flip Flop
FFL	Flip Flop Latch
FL	Flip Flop Latch or Flip Latch
FTX	Four Transistors
FUSE	Fuse
HD	Magnetic Head Driver
HP	High Power
HPD	High Power Driver
HS	High Speed
I	Inverter
ICN	Indicator Coupling Network
ID	Indicator Driver
IDL	Indicator Driver Lamp
II	Isolating Inverter
Ind	Indicator
JACK	Jack
JMPR	Jumper
L	Inductor
Ld	Loaded
Lim	Limiter
Lp	Loop
LS	Low Speed
LSA	Line Sensing Amplifier
LTN	Line Terminating Network
Mach	Machine
MD	Magnet Driver
Mem	Memory
Mpx	Multiplex
MS	Medium Speed
N	Inverter
NL	No Load
ODD	Odd Count
OE	Exclusive OR
OI	OR-Inverter
OIT	OR-Inverter-Terminate
OR	OR
OR	OR Circuit
Osc	Oscillator
PB	Push Button
PH	Polarity Hold
Pwr	Power
R	Resistor
R-C	Resistor-Capacitor
Rcvr	Receiver
Rd	Read
Reg	Register
Rly	Relay
RW	Read-Write
Sel	Select
Ser	Serial
SERV	Service
SERV	Service Voltage
SLT	Solid Logic Technology
SPD	Sample Pulse Driver
SPEC	Special
SS	Singleshot
SSL	Singleshot Low-Speed
SSA	Singleshot Medium-Speed
ST	Schmitt Trigger
SW	Switch
T	Terminate
TD	Time Delay
Tgr	Trigger
THRM	Thermal Switch
TLD	Transmission Line Driver
TLR	Transmission Line Receiver
TLT	Transmission Line Terminator
Tx	Transistor
V	Voltage Amplifier
Var	Variable
XOI	Exclusive-OR-Inverter
XOR	Exclusive-OR
XORL	Exclusive-OR Latch
Xtl	Crystal
Z	Impedance







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- **Solid Logic Technology (SLT) is the technology of current IBM systems.**
- **Chip, module, card, board, and gate are the physical building blocks.**
- **Circuit speeds demand computer use for figuring wire lengths.**

Solid Logic Technoogy (SLT) is the newest technology applied to the design of IBM products. SLT uses microminiaturization techniques in the production of devices for high-speed computers.

In SLT, the modules and other electronic components are mounted on cards. The cards plug into 8½ x 12½ inch boards. The boards are cabled into gates. The gates are cabled together to form the machine or system.

The basic semiconductors are the dual diode and the transistor chip. These chips are about the size of a grain of salt. The chips, along with screened resistors and interconnections, are packaged in ½-inch square modules. The modules have 12 or 16 pins for connections to a card.

The module and other electronic components are designed into circuits that have three operating speeds: 700 nanoseconds (slow speed), 30 nanoseconds (medium speed), and 5-10 nanoseconds (high speed).

Design automation has developed several programs for SLT. One of these programs, called Automated Logic Diagrams (ALD's), is the computer-generated logic of the machine or system. Another computer program designs the printed wiring of the boards for optimum operation.

As machines operate at faster speeds, wire lengths between components become a design problem. Electrons travel at about 186,300 miles per second, which equals 11.8 inches per nanosecond. If we assume 1 nanosecond of delay for approximately each foot (11.8 inches) of wiring, we see that the wiring paths for circuits in the 5-10 nanosecond range of operation become critical. The design automation program calculates wiring paths on the card and board so that wire lengths and circuit paths are minimal.

Physical Description

The smallest physical component is the dual diode or the transistor chip, each of which is 0.025-inch square A chip is mounted on a substrate along with other chips, screened resistors, and the printed wiring. The substrate and its components are encapsulated to form a ½-inch square module. Modules and molded R-C components are mounted on pluggable cards. The cards have a printed land (wiring) pattern and, generally, a voltage-ground plane. Card sizes are such that 6, 12, 24, 36 or more modules may be mounted on each card. The cards may plug into one or two sockets, depending upon the particular type of card.

In summary, physical size from the smallest to the largest is: chip to module to card to board to gate to frame to machine.

Physical Design of Circuits

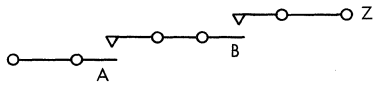
The physical building blocks of SLT are modules, cards, boards, and gates. The physical building blocks of electronic circuits (the function block found on the ALD page) are the modules and the printed land pattern of the card. The modules are designed so that they may be used separately or in combinations with other modules or separate components. Circuits are designed to use parts of modules in combinations with other modules or parts of modules and/or components. For example, Figure 54 shows that the medium speed singleshot is made up of: one-half of a FDD, R-1 of an R-pack, one-half of a II module, one-half of a DCI module, and a timing capacitor. All these separate parts are tied together by the printed land pattern of the card.

Symbology and Definitions

- **The standard SLT symbol for logic is the rectangular block.**
- **All blocks must have a defined function.**
- **Standard functions are: A, OR, N, A-(n), OE, AR, ODD, EVEN, FF, FL, PH, SS, ST, CV, TD, CS, OSC, SPEC.**
- **Components have defined functions: relays, switches, resistors, capacitors, transformers, etc.**

SLT component circuits are represented by a standard set of symbols. A symbol only conveys information; the symbol is not the information itself but merely a representation of it. However, a standard set of symbols allows us to represent the wiring of a computer, no matter how complex or large, with a logic diagram. A logic diagram (ALD) is a representation of logical elements and their interconnections.

The basic SLT component circuit is an AND, an OR, or an inverter. An AND circuit is a circuit that has an output when all inputs are satisfied. A simple analogy is a relay circuit representing an AND circuit:

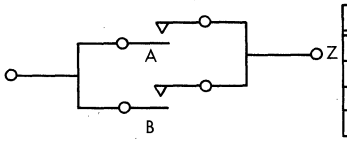


When A is satisfied (the normally open point is closed) *and* when B is satisified, then, and only then, is an output present at point Z. If 0 is the value for an unsatisfied point, and 1 is the value for a satisfied point, the function of the AND circuit may be expressed in a truth table:

Z = AB

A	B	Z
1	1	1
1	0	0
0	1	0
0	0	0

An OR circuit, by definition, has an output if any input is present. It can be represented by the relay circuit and its truth table as follows:

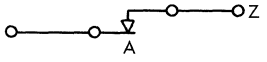


Z = A + B

A	B	Z
1	1	1
1	0	1
0	1	1
0	0	0

With this OR circuit, there is an output at Z if either point A is satisfied, *or* if point B is satisfied, *or* if both A and B are satisfied.

An inverter, as the name implies, is a circuit that has an output when the input is not satisfied, and no output when the input is satisfied. An analogy of the relay circuit and truth table follows:

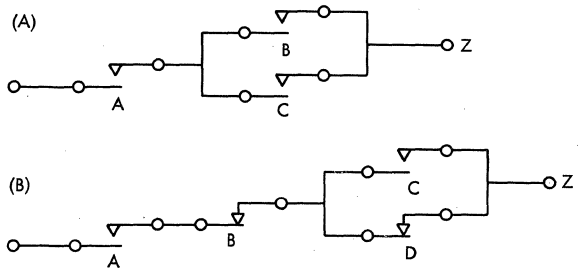


$Z = \overline{A}$

A	Z
1	0
0	1

With this circuit, there is an output at point Z when A is not satisfied – expressed as (not A or $\overline{A}$); there is no output from point Z when A is satisfied.

These concepts can be thought of as logical functions: AND, OR, and inverter. Logical functions may be combined to provide such complex circuits as shown in Figure 1.



Z = A (B + C)

A	B	C	Z
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

$Z = A\overline{B}\ (C+\overline{D})$

A	B	C	D	Z
1	1	1	1	0
1	1	1	0	0
1	1	0	1	0
1	1	0	0	0
1	0	1	1	1
1	0	1	0	1
1	0	0	1	0
1	0	0	0	1
0	1	1	1	0
0	1	1	0	0
0	1	0	1	0
0	1	0	0	0
0	0	1	1	0
0	0	1	0	0
0	0	0	1	0
0	0	0	0	0

•Figure 1. Relay Circuits Combining Two or More Logical Functions

NOTE: In truth tables:
1 means a satisfied input or output
0 means an unsatisfied input or output
+ means or
• (or no symbol) means and
$\overline{X}$ means not X

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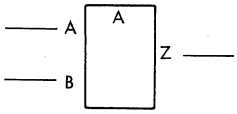
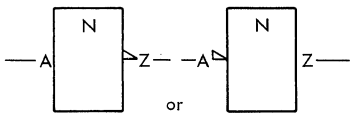
Once the rules for writing symbols have been established, logical functions may thereafter be expressed in symbols. ALD's use the rectangular block as the basic symbol for a circuit:



The function of a circuit is placed inside the block at the top. The foregoing example represents an AND circuit. The function symbols, of the three circuits discussed are: A for the AND circuit; OR for the OR circuit; and, N for the inverter circuit. Other symbols and their definitions will be discussed later. An inverter circuit is represented below.



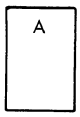
Point A is the input; Z is the output, or output line.

The wedge (◺) at an input or output indicates that the line must be at the least positive potential when the function of the block is satisfied. Blocks with different functions may be connected together to perform a logical operation. Figure 2 shows blocks connected together and the resultant truth tables. For example, as shown in Figure 2F, there is a plus (+) output at Z when either A and B are plus (+), or C and D are plus (+).

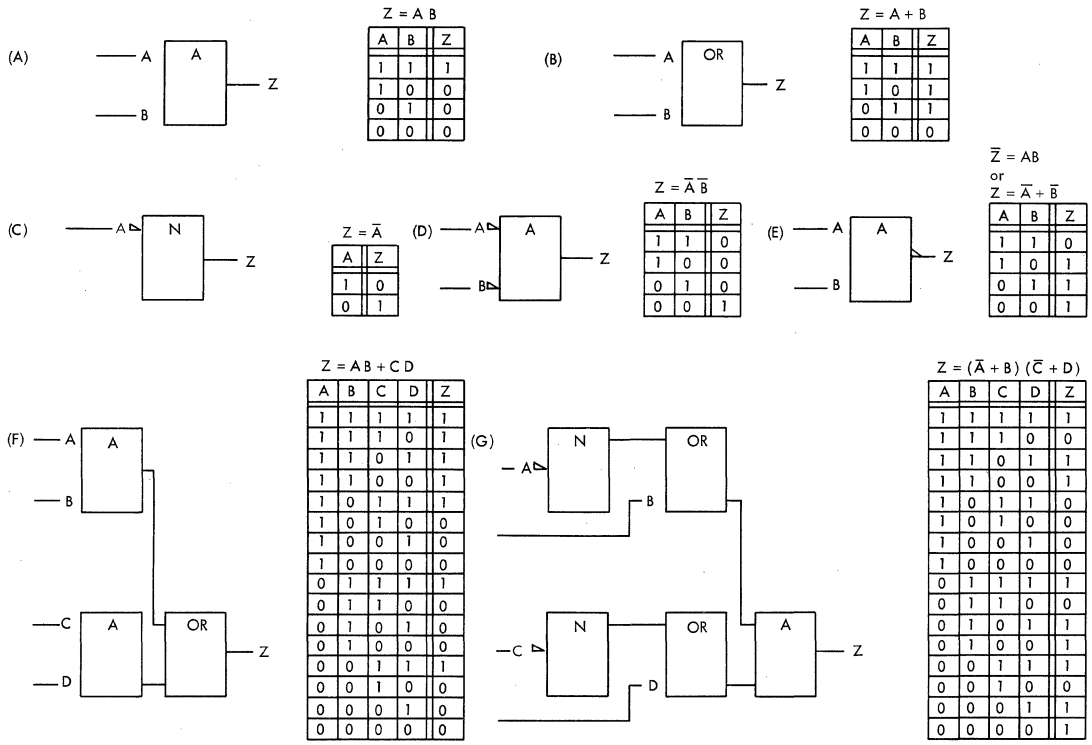
Standard Logic Blocks

AND

The output of the AND block is at its indicated polarity only when all of its inputs are at their indicated polarities. Note, the letter(s) in the block is the symbol of the function. In this case, A is the symbol for the function AND.



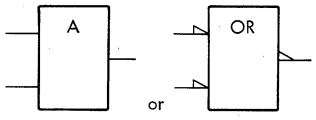
Circuit Description: Figures 27-49
Example: Figures 76 and 79



•Figure 2. Symbols and Truth Tables for Electronic Circuits

Positive AND (Negative OR)

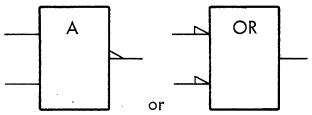
The output of the positive AND is in its more positive condition only when all the inputs are in their more positive condition.



Example: Figure 76

Positive AND Inverter

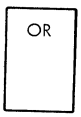
The output of the positive AND inverter is in its more negative condition only when all of the inputs are in their more positive condition.



Example: Figure 79

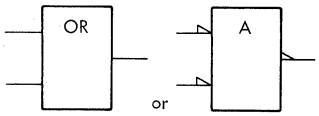
OR

The output of the OR block is at its indicated polarity only when one or more of its inputs are at their indicated polarity.



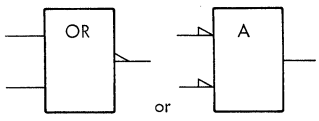
Positive OR (Negative AND)

The output of the positive OR is in its more positive condition only when one or more of the inputs are in their more positive condition.



Positive OR Inverter

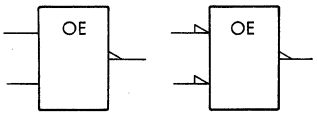
The output of the positive OR inverter is in its more negative condition when one or more of the inputs are in their more positive condition.



Example: Figure 77

Exclusive OR

The output of an exclusive OR will be at its indicated polarity when one and only one of its inputs is at the indicated polarity.



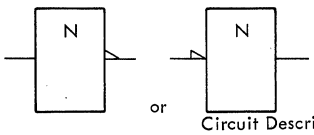
Ckt Desc: Figure 50

Example: Figure 78

The following examples describe types of inverter, amplifier, threshold, ODD, and EVEN functions.

Inverter

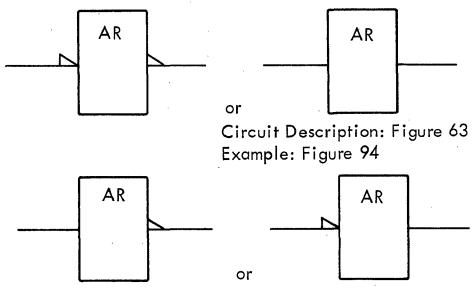
The output of the inverter is of opposite potential to the input.



Circuit Description: Figure 58
Example: Figure 81

Amplifier

The amplifier provides adequate driving energy and an appropriate impedance match to other blocks. The amplifier output is at its indicated polarity only when the input is at its indicated polarity. An amplifier can have no more than one logic input. An amplifier having input or output of other than standard logic signal voltage will have distinctive labeling at the block.



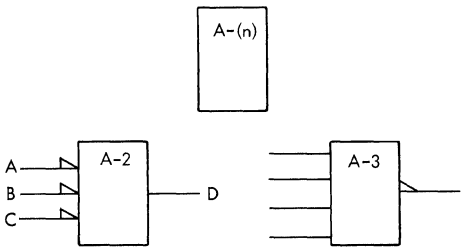
Circuit Description: Figure 63
Example: Figure 94

Threshold

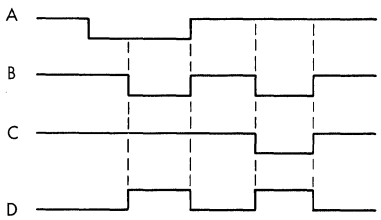
The output of the threshold is at its indicated polarity when and only when the number of inputs (at their indicated polarity) reaches or exceeds the number specified in the function symbol. The threshold symbol is also used when an input has greater weight than 1 in the determination of the threshold. In this case the input is titled with a number denoting the particular weighting factor. "Weight," as used here, denotes a value that is relative to the other inputs. For example, if two inputs are weighted at 2 each and six others are weighted at 1 each, and the symbol is A-4, the output is up if: both 2-weighted inputs are up; or four 1-weighted inputs are up; or if one 2-weighted input and two 1-weighted inputs are up.

The A-(n) symbol (shown in the accompanying illustration) will have at least three inputs. The num-

ber specified in the function symbol will not be 1, or equal to the number of inputs, or their total weighted value.



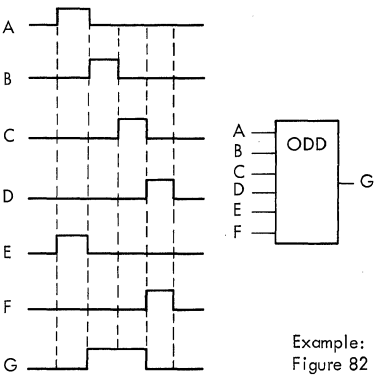
Example: (A-2)



ODD Count

The output of odd count (ODD) is at its indicated polarity when, and only when, an odd number (1, 3, 5, 7, etc.) of inputs are at their indicated polarity.

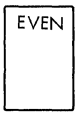
NOTE: An ODD may be shown as an even count (EVEN) through proper change in polarity indication, and vice versa. There is a simular relationship in the AND and OR circuits.



Example: Figure 82

Even Count

The output of even count is at its indicated polarity when and only when an even number (0, 2, 4, 6, etc.) of inputs are at their indicated polarity.



As noted earlier an EVEN may be shown as an ODD through proper change in polarity indication, and vice versa. This change may be compared to the AND and OR circuit.

Flip Flop

The flip flop has two stable states. One of these is called the 1 state or set state; the other is the 0 state or clear state. The flip flop block normally has two outputs, a 1 output and a 0 output. In the ALD's a line from the upper part of the block represents the 1 output and a line from the lower part of the block represents the 0 output.

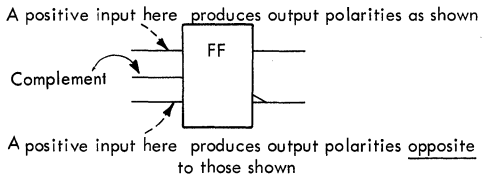
The flip flop is in the 1 state when the 1 output (the upper output on the ALD) is at its indicated polarity. Regardless of a flip flop's inputs, its 1 output and 0 output in the stable state are always opposite in polarity.

A signal of indicated polarity sent to the line opposite the 1 output causes the outputs of the block to assume their indicated polarities.

A signal of indicated polarity sent to the line opposite the 0 output causes the outputs to assume polarities opposite to those indicated.

A signal of indicated polarity sent to a line centered between the two lines already mentioned, or sent to both the set and clear inputs simultaneously, changes the state of the flip flop (complement the flip flop).

The polarities shown at the inputs and outputs of a flip flop of a particular circuit type are unchanging parts of the symbol itself.



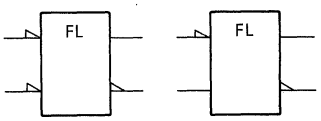
Circuit Description: Figure 52
Example: Figure 103

Flip Flop Latch or Flip Latch

The definition of the flip flop latch or the flip latch is the same as that given for a flip flop except that simultaneous signals of the indicated polarity at the 1 input and the 0 input will cause both the 1 output and the 0 output to go to either the negative polarity or the positive polarity for the duration of that input signal.

NOTE: A simultaneous set and reset is not a normal operation. If, however, simultaneous set and reset did

happen, the design of the circuit would determine which polarity both outputs would have.

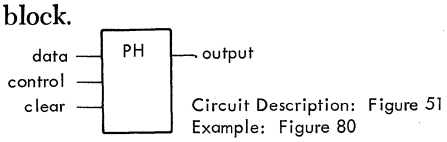


The complement input is not used with the flip-latch block.

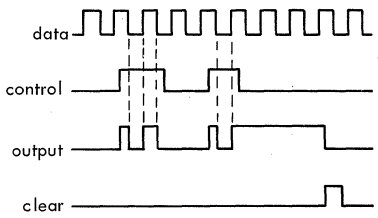
Polarity Hold

The output of this block it at the indicated polarity whenever the data line is at its indicated polarity and the control line is at its polarity. When, at a particular moment in time, the control input goes to the polarity opposite to that indicated, the output remains at whatever polarity it possesses at that moment. The PH block may have a clear input. If so, when the clear polarity is at its indicated polarity, the output will be opposite of its indicated polarity.

The output line is located towards the top of the block. The data line is opposite the output line. The control line is centered on the input side of the block. The clear line is located towards the bottom of the block.

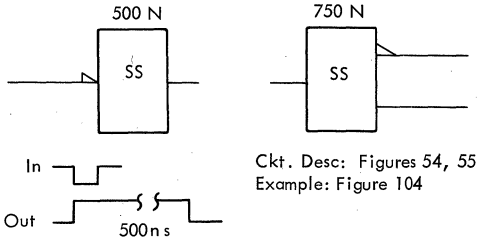


Circuit Description: Figure 51
Example: Figure 80



Singleshot

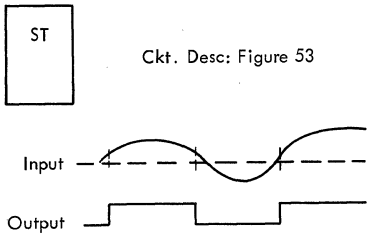
The output of the singleshot changes temporarily to the indicated polarity when it receives an input signal of the indicated polarity. The output remains in this quasi-stable state for a time characteristic of the particular block. The singleshot always has the time duration shown in the title area of the block. If a singleshot has more than one output not of the same duration, the block will be labeled or a reference note on the page will relate pin numbers to time durations.



Ckt. Desc: Figures 54, 55
Example: Figure 104

Schmitt Trigger

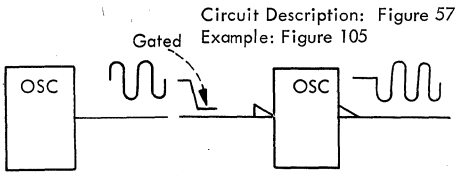
The output of the Schmitt trigger goes to its indicated polarity whenever the input crosses the threshold in the direction of the indicated polarity. The output remains at this indicated polarity until the input signal crosses the threshold in the opposite direction.



Ckt. Desc: Figure 53

Oscillator

The oscillator produces a uniform, repetive continuous output, or produces an output only when the input signal is at the indicated polarity.



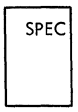
Circuit Description: Figure 57
Example: Figure 105

Special Blocks

Two conditions must exist for a block to be designated as special:

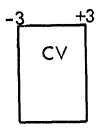
1. The function is not covered by any single block symbol.
2. The function cannot be expressed in terms of an interconnected set of individual block symbols.

The function of a special block is described by the wording on the ALD, located either at the block or in a comment area referenced by a note in the title area of the block.



Converter

The converter block provides the necessary conversion or translation between two types of logic, i.e., voltage mode to current mode, voltage to voltage, etc. An indication of input and output voltage levels, or line types, is shown in the block title area of the block.



Example: Figure 92

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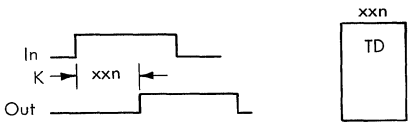
Time Delay

The time delay block delays a signal without intentional distortion of the signal. The time delay symbol must always be accompanied by the time delay.



Circuit Description: Figure 61

Time delays having a delay time for the leading edge of the output that is different from the time delay for the trailing edge shall be identified by the placement of an L for leading and a T for trailing immediately prior to the separate delay times in the block area. The input polarity at the block must be that associated with the "leading" edge of the output.

Limiter

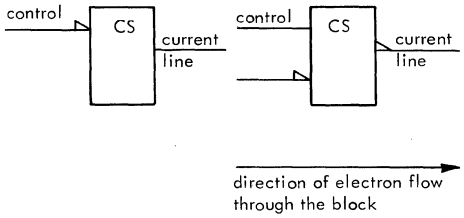
The limiter block sets one or both extremes of a waveform to a predetermined level without intentional distortion of the remaining waveform.

Example: Figure 106

Current Switch

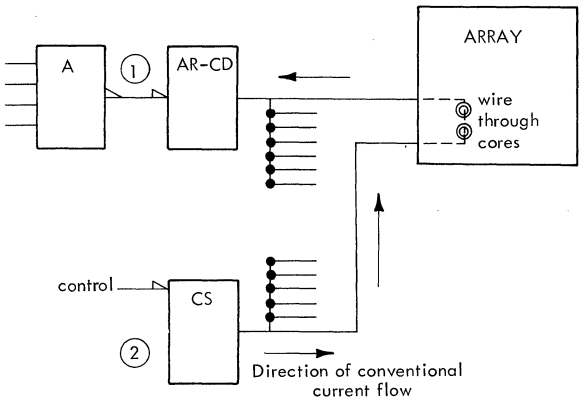
Under some circumstances it is difficult to describe the logic operations of AND'ing and OR'ing in the standard block symbols because of the use of series control of current flow, e.g., handling the drive currents in a magnetic core array. At times the purpose of a circuit is to allow a flow of current (either in or out) under logic voltage control. When this condition exists, the circuit cannot cause the current to flow solely through electrical action at its own logic input. Because of the series flow of this current through other controlling circuits, the circuit may be given the function label CS (current switch).

The control input of the CS is placed towards the top of the block. Sending a signal of indicated polarity to this input allows (not necessarily causes) the flow of current through the block in the direction indicated by the polarity symbol located at the output side of the block (on the current line). A negative polarity symbol, for example, indicates electron flow away from the output side. A line opposite the output line is assumed to be the same current line, separated by the circuitry of the CS. The polarity indication for this line is the same as that of the corresponding output line.



Example: Figure 101

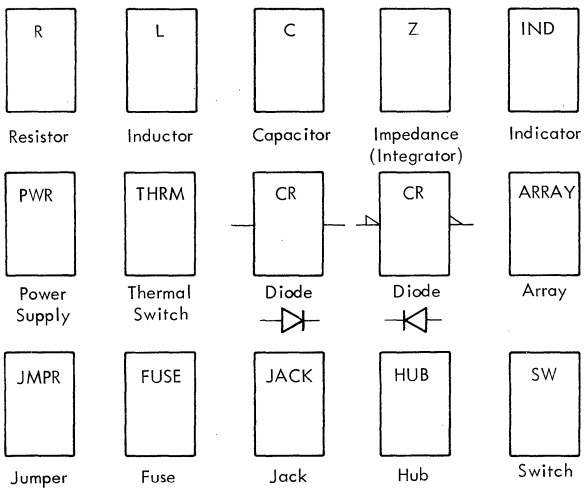
The accompanying illustration shows the use of the current switch in the control of a series flow of current through more than one circuit. A negative signal at (1) causes current to flow in the array, provided the control signal is negative at (2).



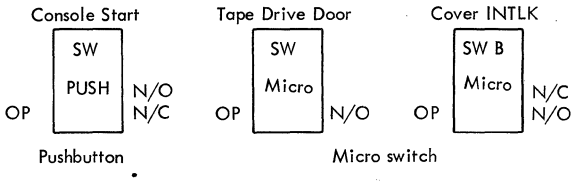
Component and Auxiliary Blocks

Many types of components may be mounted on an SLT card. The following examples are typical (but not all-inclusive) of these components.

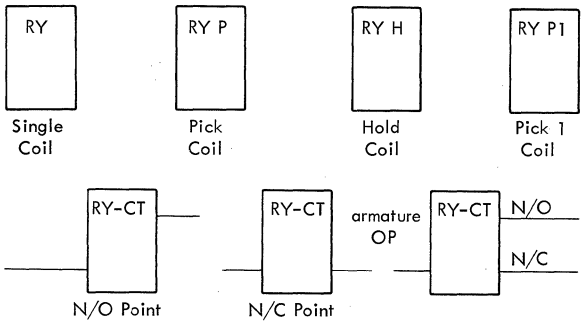
Component Blocks



Switch Blocks



Relay Coil and Contact Blocks



Note: 1. One set of contact points will be shown in each block.
2. This symbology refers to relays mounted on cards.

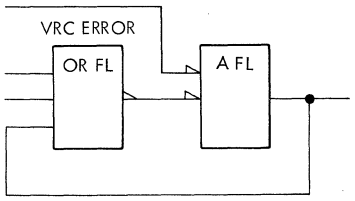
Example: Figures 113, 114

Multiple Block Configurations

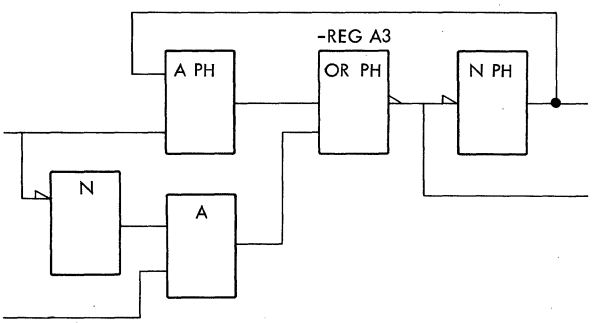
Bi-Stable Circuits

The flip flop, flip latch, or the polarity hold circuits (see examples A, B, C, D) may be designed with AND-OR blocks instead of a single circuit. When these bi-stable circuits are shown in multiple block form, one of the blocks will be an OR block placed towards the top (or left) in the block arrangement containing the cross-coupled parts. The title of the arrangement is placed above this OR block.

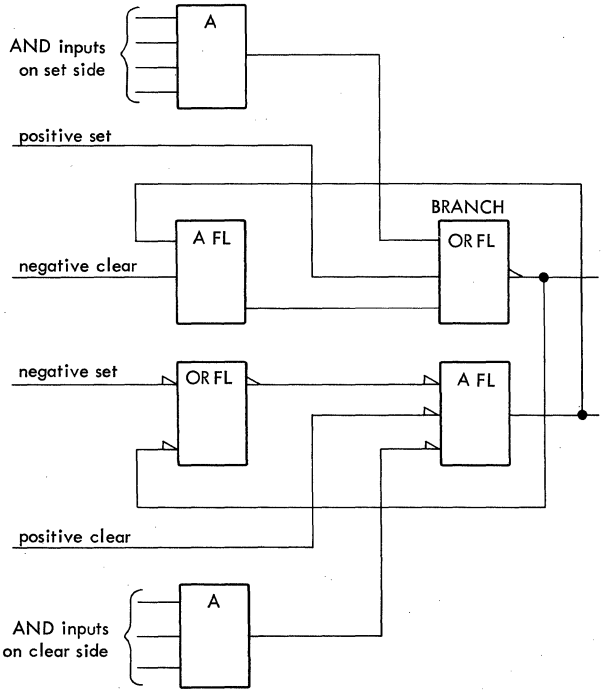
When AND-OR blocks are arranged to perform the function of a flip latch, flip flop, or polarity hold, the symbol FL, FF, or PH is added to the AND-OR function symbol in the top of every block making up the cross-coupled arrangement. An exception to this arrangement occurs when the AND-OR block is part of a DOT AND or DOT OR. (See discussion on DOT functions that follows.)



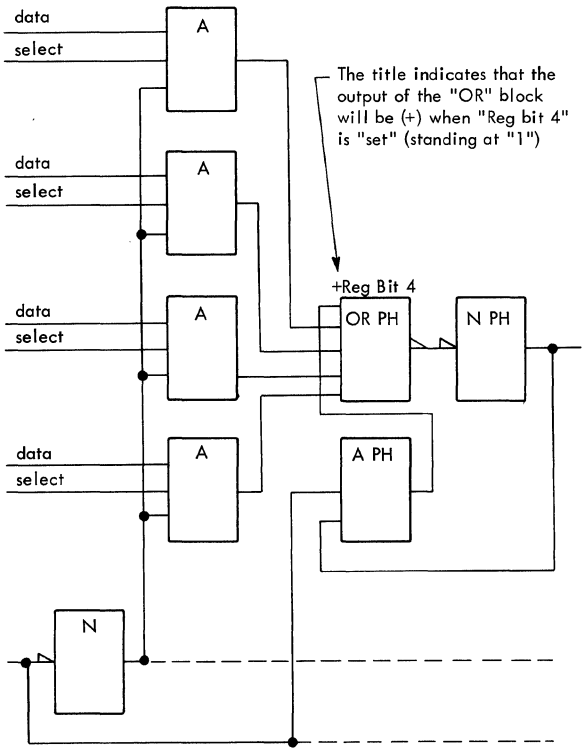
Example A



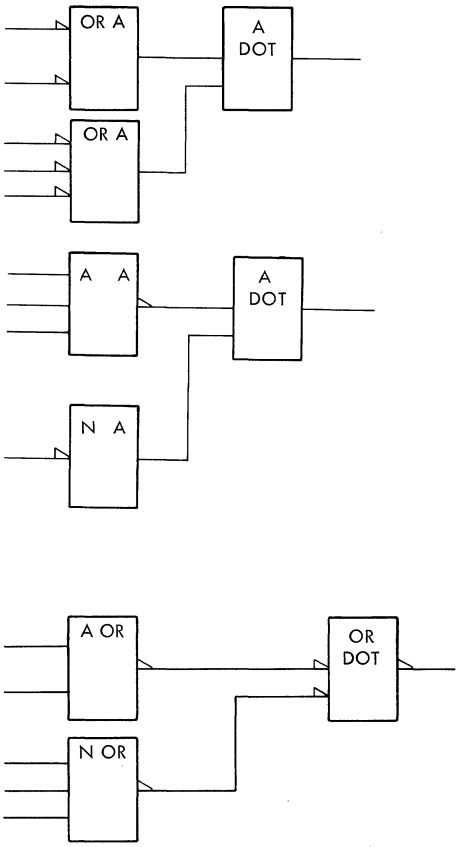
Example B



Example C



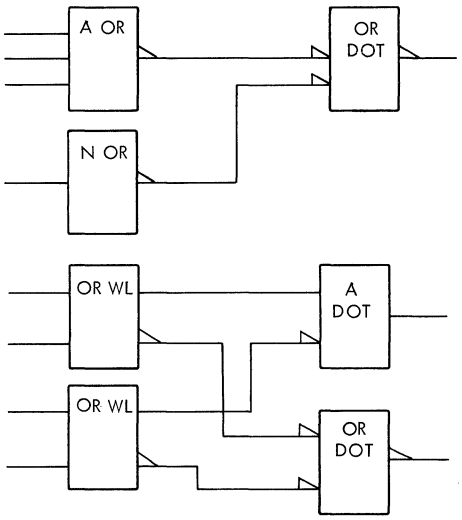
Example D



DOT OR, DOT AND

Basic blocks whose outputs are connected externally to perform an AND or OR operation (DOT AND, DOT OR) are identified by an additional A or OR placed in the block to the right of the primary block function symbol. In the ALD's a block labeled OR DOT or A DOT is used to form the junction of the lines being joined.

When the output of a block enters into both a DOT OR and a DOT AND, the letters WL (for wired logic) are placed to the right of the primary block function symbol.



Suffixes to the Block Function Symbol

The suffix is information added to the block function to clarify the logic usage. Some of the suffixes are:

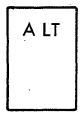
LT	Transmission line terminator
LD	Transmission line driver
ID	Indicator driver
CD	Core driver
HD	Magnetic head driver
MD	Magnet driver
V	Voltage amplifier
DF	Differential amplifier

FF, FL, PH — Used for emphasis of storage type blocks when these blocks are in multiple block form.

OR, A, WL — Used in the identification of blocks whose outputs are connected in the DOT OR or DOT AND arrangement; these suffixes take precedence over all others. When the DOT AND or DOT OR takes precedence over a suffix, the suffix is placed in the title area of the block.

P, H, CT — Used with the RY (relay) blocks to indicate coil and contacts.

Some possible uses of the suffix are:



AND circuit being used as a transmission line terminator

Amplifier used as a magnet driver

Amplifier used as a core driver

OR circuit used as an indicator driver

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- **ALD's are computer generated.**
- **ALD's for all SLT machines use the same symbols and page format.**

Computer-automated design helps engineers check designs and connect individual circuit sections involving literally hundreds of thousands of electrical connections, components, cables, and other items. The computer maintains an interim magnetic tape record of circuits as they are developed and produces the final tape used in an automatic system to make new circuit patterns.

In SLT, the design automation program is used to:

1. Print the ALD's.
2. Document on magnetic tape the logical design of computers, determining the layout of printed boards and cards.
3. Assist the engineer to simulate logical designs and verify circuit loading before the designs are committed to manufacture.
4. Assist the engineer in assigning the logical elements to boards and cards and in locating printed wiring on boards.
5. Compute cable length requirements for different interconnections.
6. Provide a monitoring service to help enginneering and manufacturing groups coordinate their activities.

The SLT design automation program accepts various forms of information from design engineers and processes it into machine logic. Design automation gives the engineer the option of using the computer to package a logic design or to check manual packaging. In addition, it allows him to treat a portion of a system as a unit for simulation, packaging, or design modification.

Simulation and circuit load checking programs verify logic designs recorded on a logic master tape. Packaging programs, which pertain to card selection, card-to-board assignments, pin locations, and card placement, assist in mapping logic circuits into the circuit cards. The computer also aids integration of cable design and installation data with cable manufacturing data.

After the computer determines the connections and designs the board wiring, it records the printed connections on a master tape. This tape is later used to generate other tapes containing circuit board design data.

The basic document produced by design automation is the Automated Logic Diagram (ALD), a computer-drawn schematic representation of machine functions. The ALD for Solid Logic Technology is a 11 x 17 inch sheet. See Figures 3 and 4.

On an ALD, circuits are represented by rectangular blocks, which symbolize logical functions. They are connected by printed lines, which symbolize electrical connections. Inputs enter the circuits on the left; outputs leave at the right. Most of the page is used for the representation of logic; page identification and supplemental information appear at the bottom of the sheet.

Page Number

The page number is located in three places on the sheet. The page number in Figure 3 is KH142. In this illustration the page number is in the upper right-hand corner, as well as in both the lower right and the lower left corners.

Logic pages are numbered according to a coded prefix consisting of two alphabetic letters, representing the major and the minor characters. The general scheme of the coding is shown in Figure 5.

For example, the coding for the A register is RA. "R" is the major character; it means register. "A" is the minor character, designating the particular register. Another example is KR101, which means control (K), check triggers (R), page 101.

Figure 5 is processor oriented. Slight variations appear both in the processor pages and in the I/O pages.

Machine Version

A version page shows wiring and cards that are not on the basic machine. This wiring must be added to that used by the basic machine. This is in direct contrast to the additive card code, in which the wiring is part of the basic machine, and only cards are added to make the feature operative. An example of a version page is those pages that added the cards and wiring for floating point.

A version page is made up of all basic page blocks which are unchanged in the version design plus additional blocks (version blocks) needed to change the basic page into a version page. A version number is printed at the top of each version block to differentiate it from a basic block.

The machine version number appears below the page number; for a basic (standard) machine this number is 000. A version page assigned by Design automation has a number other than 000.

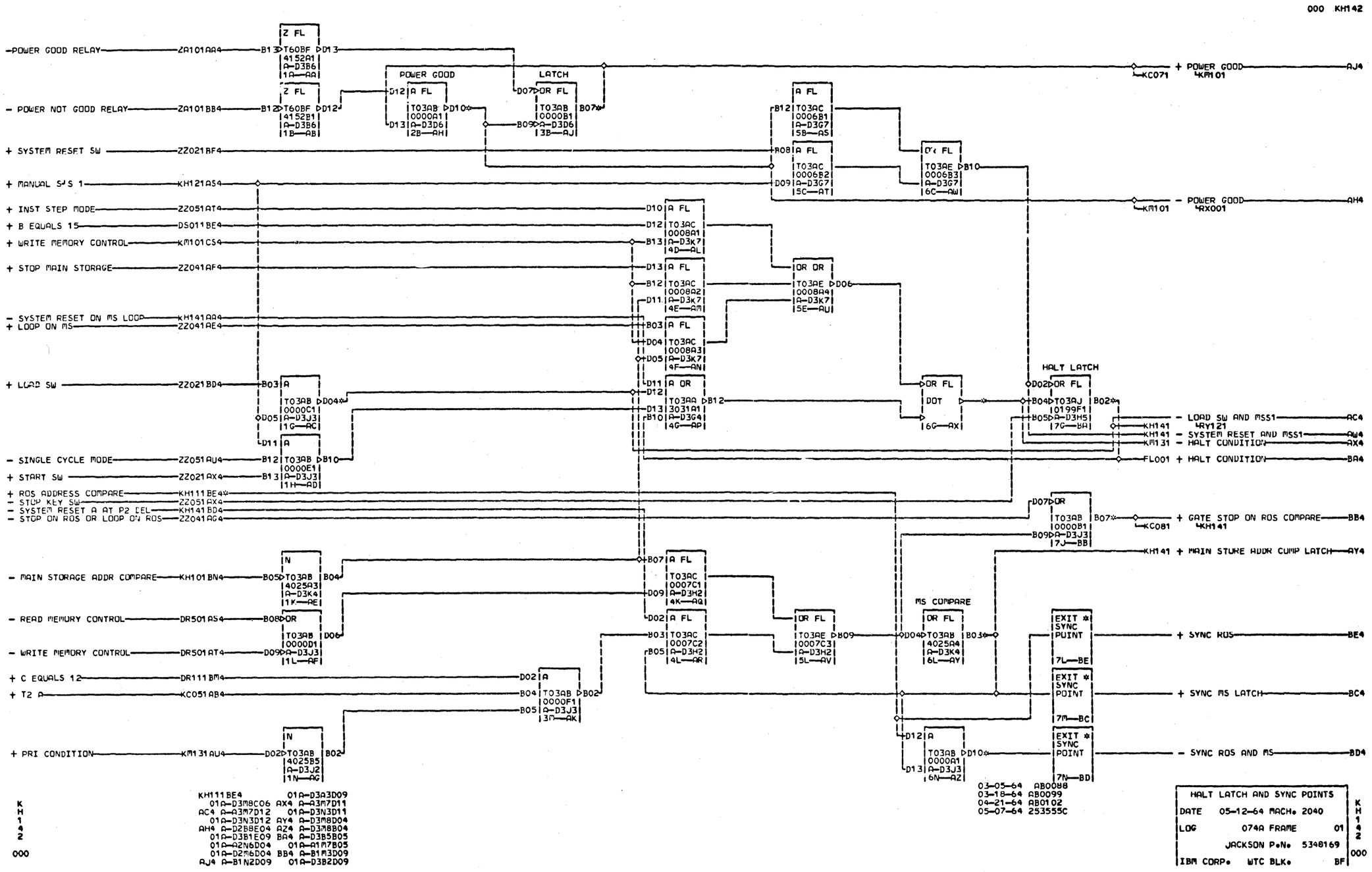
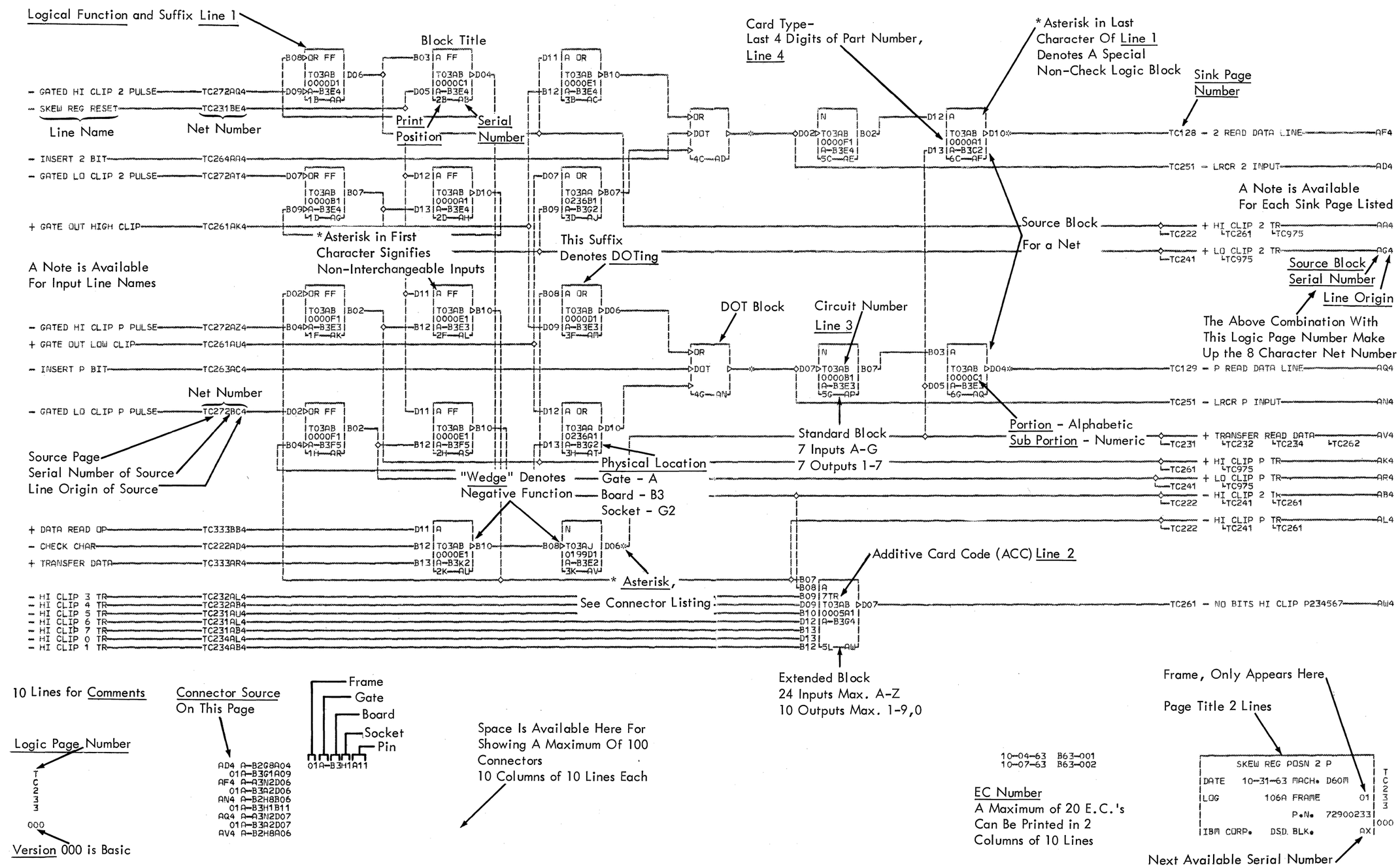


Figure 3. The Automated Logic Diagram (ALD)



•Figure 4. ALD Page Annotated

I.	Adders	
	1. Addressing Adder	AA-AB
	2. IC Incrementer	AC-AD
	3. Exponent Adder	AE-AF
	4. Main Adder	AM-AQ
	5. Serial Adder	AS
	6. VFL and DEC Adder	AV-AW
II.	Decoders	
	1. Op Decoders	DN
	2. FLP and Gen. Decoder	DP
	3. Addressing and Pre FTH	DA
	4. Trap Decode	DB
	5. Reg Decode	DG
	6. ROM Decode	DR-DS
III.	Counters	
	1. Instruction Ctrs	CA-CB
	2. Local Store Address Ctr	CC-CD
	3. Misc. Ctr	CE-CZ
IV.	Busing (Excluding Memory Bus)	BA-BZ
V.	Registers	
	1. A Reg	RA
	2. B Reg (BOP REG, Mod 70)	RB
	3. D Reg	RD
	4. E Reg (PSW for Mod 70)	RE
	5. F Reg (I/O Reg, Mod 70)	RF
	6. G Reg (Gen Purpose, Mod 70)	RG
	7. H Reg	RH
	8. J Reg	RJ
	9. K Reg	RK
	10. L Reg	RL
	11. M Reg	RM
	12. N Reg (Op Code Reg, Mod 70)	RN
	13. P Reg (FLT Pt Reg, Mod 70)	RP
	14. Q Reg (FLT Pt Reg, Mod 70)	RQ
	15. R Reg (Reg Bus Latch, Mod 70)	RR
	16. S Reg (Shift Ctr & Exp in, Mod 70)	RS
	17. T Reg	RT
	18. U Reg	RU
	19. V Reg	RV
	20. W Reg	RW
	21. X Reg	RX
	22. VFL and Decoder Reg, Mod 70	RY
	23. Direct Data Reg	RZ
VI.	Main Storage Registers and Controls in CPU (Includes SDR Registers, Storage Buses, SAR, SBI "OR", M and N Regs in Mod 30)	MA-MC
VII.	Controls	
	1. Advance or Seq Cntls	KA
	2. Branch and IC Cntls	KB
	3. Clock Cntls	KC
	4. I Exec (Mod 70) I Fetch & Exec (Mod 60)	KD
	5. Chan Cntrls	KE
	6. Fix Seq Cntls	KF
	7. Gen Reg Cntls	KG
	8. FLT Cntls	KH
	9. ROS Cntls	KK
	10. Local Store Cntls	KL
	11. Priority and Interrupt Cntls	KM
	12. I/O Instr Cntls	KN
	13. VFL Cntls	KP
	14. VFL Cntls	KQ
	15. Check Triggers	KR
	16. Status Triggers	KS
	17. VFL Cntls & Decimal Cntls	KY
	18. Any Misc. Cntls such as FP	KT-KU
	19. Fixed Pt, Storage Protect, Real Time clk, Status Cntls	KW-KZ
VIII.	Consoles	PA-PE,PJ-PZ
	1052 Console Adapter	PF,PG,PH
IX.	Local Store	LS-LT
X.	TROS	EA-EC
XI.	CROS	ED-EF
XII.	Spec. Features	XA-XZ
XIII.	Hardware Oriented Pages	ZA-ZZ
XIV.	I/O Channels	
	Multiplex Channel	FA-FZ
	Selector Channel #1	GA-GZ
	Selector Channel #2	HA-HZ
	Direct Data	JA-JZ
XV.	ROS Flow charts	QA-QZ
XVI.	Power Supplies	YA-YZ

Figure 5. Definitions of Page Number Prefixes

Title Block

The title block is printed in the lower right corner of the page. As Figure 6 shows, information can be found at three places in the block:

1. At the top
   a. The page title ("LS Address Register J Bits 0 Through 3" in Figure 6).
2. On the left side
   a. Date of processing by design automation (05-12-64).
   b. Log number (or computer run), "074A," assigned by design automation.
   c. The corporate division, WTC (World Trade Corporation).
3. On the right side
   a. Machine type, "2040." This may be a pseudo number or it may be the machine number followed by a suffix. The suffix differentiates between models or features of the machine number.
   b. Frame, "01"; within the machine, may be 01 to 63.
   c. Part number of the page, "5348221."
   d. Block DF is, in terms of design automation, the next available block serial number available for for use on that page.

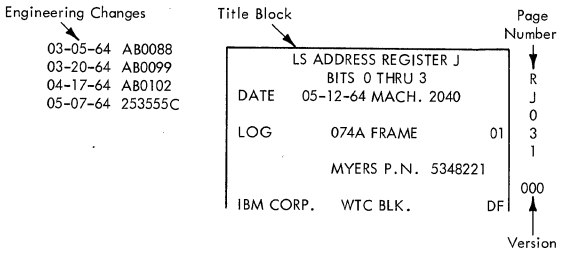


Figure 6. Example of Title Block, Page Number and Version, and Engineering Changes

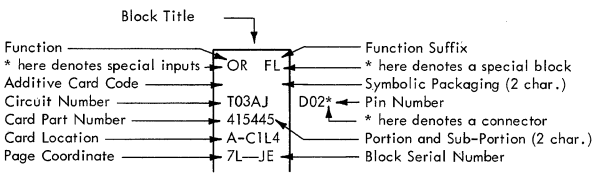


Figure 7. The ALD Logic Block

Logic Block

Logic blocks shown in Figure 7 are positioned on the page in a matrix seven columns wide and 13 rows high. The columns are numbered 1-7. Rows are lettered A-N, excluding I.

A logic block is six increments wide by seven increments high; it may be lengthened downward to a maximum of 24 increments. The block may have one to seven input and/or output lines on the basic block; one to 24 input and/or one to 10 output lines on the extended block.

Information Inside the Block

Line 1

The logical function being performed by the circuit represented appears on line 1; for example A, OR, N, FF, etc. An asterisk (*) preceding the logical function symbol means to design automation that the input line positions are placed in a certain arrangement.

The suffix, preceded by a space and following the function, is additional information describing the function. The suffix is used to indicate DOT functions such as A OR, OR A, N OR, OR WL; to indicate the blocks in a multi-block configuration of bi-stable circuits such as A FF, OR FF, A PH, OR PH, N PH; and to indicate additional information in special component blocks such as RY CT, RY P, A LT. (See "Symbology and Definitions.")

An asterisk (*) following the suffix and/or in position six indicates a special block that does not follow the rules of design automation. Some of the special blocks are exit and entry, service-voltage logic, switch, and jack blocks, as well as discrete components such as capacitors, resistors, etc.

Line 2

The additive card code (special machine feature) appears here in the first four characters, for example, 7TR (seven-track tape feature). Additive card codes identify those logic blocks which pertain to a special class of machine features in which the feature can be installed by plugging in the feature cards.

The last two characters of line 2 contain the symbolic package designation. The use of these two characters allows design automation to generate the ALD's, to position the card on the board, and to generate the wiring (printed or discrete) on the board. Blocks with the same characters in the symbolic package field will be placed on the same board by the card partitioning program used by design automation.

NOTE: Blocks with different symbolic packages may be packaged on the same board.

Line 3

The circuit number (Figure 8) appears on line 3 except when design automation generates a pseudo block for a DOT function. In this case DOT appears on line three. A DOT block is a tie point for the output of two or more circuits feeding one circuit.

The circuit number is the coded name given to a particular circuit. The number is defined in Figure 8 and discussed in greater detail later. It will be used to

understand the logic and to identify particular components on the SLT card.

SRETL - Screened Resistor Etched Transistor Logic

Logic General Form - XYYZZ

X Defined

S - SRETL General
T - 30 ns
U - 5-10 ns
V - 700 ns
O - Analog

YY Defined

03 - Logic Blocks
05 - Voltage Translate Circuits
06 - Transmission Line Drivers and Receivers
07 - Sense Amplifiers
10 - Inverting Drivers less than 50 ma
11 - Non-Invert Driver less than 50 ma
15 - Power Driver more than 50 ma
16 - Magnetic Head and Core Driver
20 - Triggers
21 - Singleshots
22 - Oscillators
25 - Regulators, Clamps, Clippers, and Limiters
32 - Gates
40 - Specials
45 - Delay Circuits
55 - Indicator Circuits
60 - Integrators and Filters
61 - Components
63 - Reed Relays
65 - Functional Card
66 - Field Replacement Card

ZZ Defined - The Unique Card

Note: Appendix lists all circuit numbers.

Figure 8. Circuit Number Code

Line 4

The last four digits of the card part number appear here. The first three numbers, 580, are the same for all cards and are not recorded.

The last two characters on line 4 represent the portion and sub-portion. A portion represents an independent section of a card. A section may be represented by one or more logic blocks, each of which has a sub-portion number. The portion character is of the form A, B, ... Z, excluding I, O, and R. ALD blocks which are interconnected on a card are in the same portion. Every block in a portion has a unique sub-portion number. These sub-portion numbers are assigned in the sequence 1, 2, ... 9, A, B, ... Z (excluding I, O, and R).

Exception: When a circuit with an unloaded collector and an associated load resistor packaged on the same card are used together, the block designating the load resistor has the same portion as the unloaded circuit, and the sub-portion character is R.

Line 5

The card location is placed at line 5 as follows:

1. Character one is the gate (A-Z) followed by a dash.
2. Characters three and four are the board location, one alphabetic and one numeric.
3. Characters five and six are the card location, one alphabetic and one numeric.

Line 6

The print location in positions 1 and 2 of line 6 are the grid co-ordinates of the block on the ALD page, for example, 1B, 3F. The serial number of the logic block appears in positions 5 and 6, and is expressed in alphabetic characters. Serial numbers begin with AA and proceed in a sequential order (AA, AB, AC, ... ZZ). Serial numbers AA through RZ refer to the basic system group, and numbers SA through ZZ, to the special engineering group.

An Engineering Change (EC) may add logic blocks in which case the sequence of double alphabetic characters would be continued. An EC may move a block to another print location, but the serial number for that block will stay the same. If an EC eliminates a block, that serial number will not appear again on that page. The block serial number is an integral part of the net number. (See the "Glossary.")

Information Outside the Block

Title and Version Number

When logic blocks have been assigned a title, the title appears over the block. The version number appears in the title area for all version blocks.

Pin Numbers

Pin numbers are in line with the input or output line. They are the actual numbers of the base pins of the card.

Asterisk (*) On an Input or Output Line

An asterisk (*) on an input or output line denotes a connection that leaves the board. The routing is found at the bottom of the ALD page, keyed with the serial number of the block and the output line number, e.g., AQ4.

Information on the Side of the Block

Wedges

The wedge (◺) is a small triangle at the point where a signal line joins a logic block. The wedge indicates that the active state of this line (the state which satis-

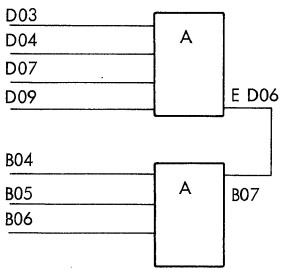
fies the function of the block to produce an output line of the state indicated) is at the least positive potential with respect to the most positive potential shown by the signal line without a wedge.

A wedge is placed in the edge of the block in line with an input or output line. When the block or circuit is performing its function, the wedge indicates the most negative (least positive) DC voltage that will be found on the line.

NOTE: Signal lines are operated at one of two voltages, an up level and a down level. Because SLT circuits operate at different speeds and at different pulse levels (0.0v to +12.0v; +0.9v to 3.0v, etc.), the line level designated by the wedge must be described as the most negative (least positive); the absence of the wedge is the most positive (least negative) level of the line.

E in the Side

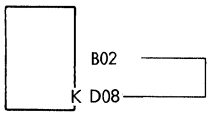
An E is placed in the side of the block whose inputs are being extended. An example is a circuit that is used to add inputs to another AND or OR circuit; the connection from this second circuit to the first is made at other than a normal input or output of the first circuit. A connection of this kind is shown without polarity and is labeled E (for extender).



K in the Side

Non-logical outputs of different blocks are not tied together by DOT blocks. Instead, a K is put in the edge of the block in line with each (except one) of the outputs connected together. The one exception is the output used to determine the net number.

Output (or input) lines on the same block may be tied together. In this case the net number will be the position without the K in the edge of the block.

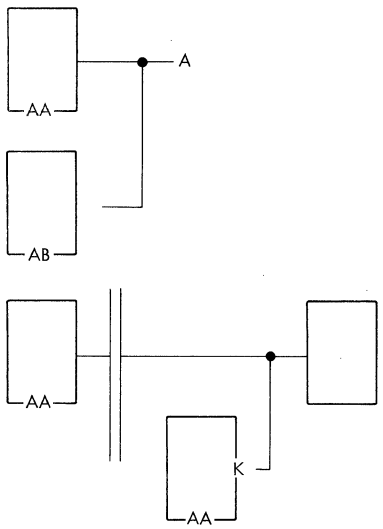


Example: the timing capacitor of a SS

Nonlogical outputs on different blocks may be tied together when:

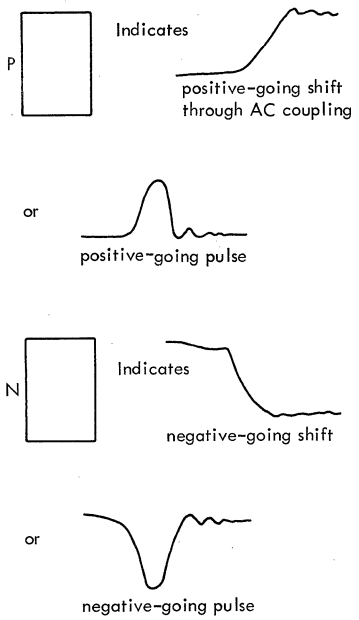
1. All the outputs tied together appear on the same page. The net number then includes the line origin of one of the outputs from one block. The commoned outputs are differentiated from the source by a K in the edge of the box position.

2. All of the outputs tied together are not on the same page. In a situation of this kind the outputs tied together on one page show an output to the right side of that page. The outputs in the same net on other pages return to the left of their respective pages and are referenced to the first page in the normal manner. The net number includes the line origin of one of the commoned outputs of the first page. In the edge of all the other blocks having outputs in the same net, a K appears in line with each commoned output.



P or N in the Side

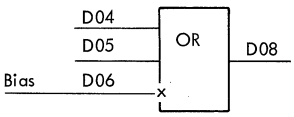
When a capacitive input to a block is designated, a P or N in the side of the block indicates the polarity of the shift necessary to satisfy the function of the block.



Example: Figure 98

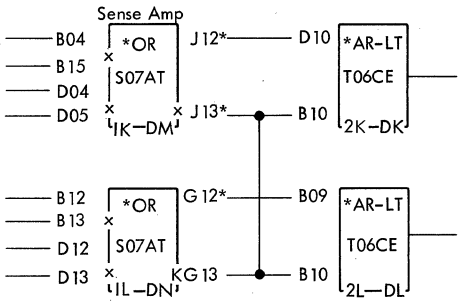
X in the Side

Non-logic connections to a logic block have an X in the side at the place where the polarity indicator (wedge) is normally placed. This non-logic input or output can be a bias line. In the accompanying illustration D06x is a non-logic connection to the two-way OR block.



Example: Figure 97

The following example shows the use of the X in the edge of the block. There is an X on the lines labeled D05 and J13, showing that these lines are the same. (It is really one ground line that is common to several blocks and completes the ground circuit in these blocks.) At location 1L, lines D13 and G13 are similar to lines D05 and J13 except that there is a K at G13 because a net may have only one source. (Other input lines to a net are designed with the K.)



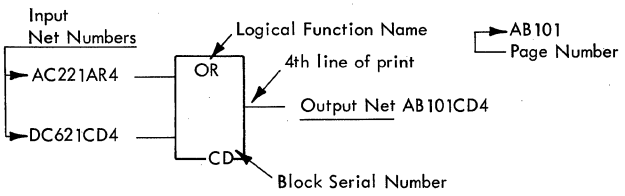
Line Names

Input Line

Each input line (Figure 4) entering an ALD page has a net number and a line name.

The net number is composed of the source page, the serial number of the source block, and the line origin of the source block. For example, KH141AT4 means that this line came from page KH141, from the block whose serial number at AT on that page, and from the fourth line position on the block. When an input line comes from more than one particular unit, such as one of many types of I/O units, or from more than one memory, a pseudo-net number will be put on the ALD net number position. These pseudo-net numbers will generally be in sequence on a page starting at 000.

A net is a set of signal points (a source and sinks) which are electrically interconnected. Generally the source point refers to the output pin of the driving block, and the sink points refer to the input pins at the driven blocks. The net identification is used to indicate which points (pins) belong to a given network.



The line name is generally a description of the line function and is signed plus (+) or minus (−), depending upon the active condition of the line at that point. If most of the lines in the box are plus (+), the sign may not appear unless it is minus (−).

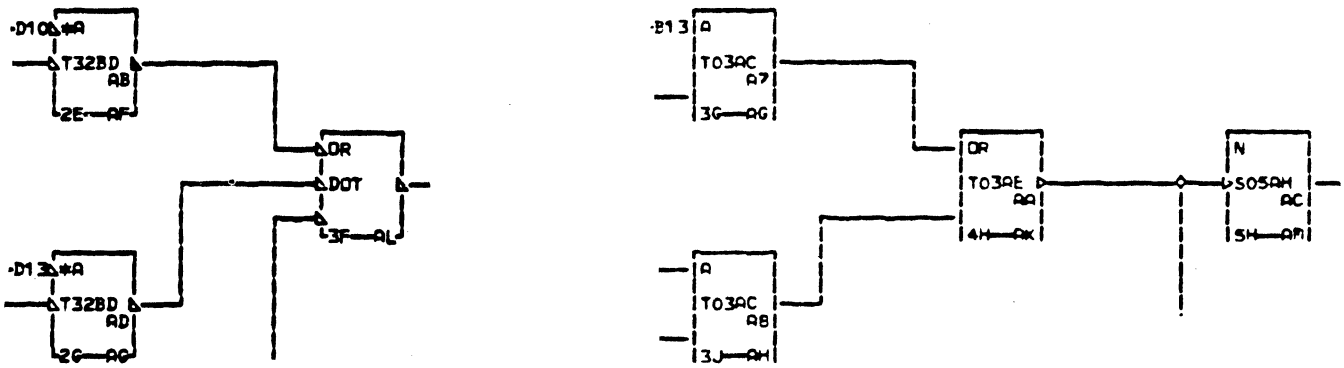


Figure 9. AND, OR, Inverter

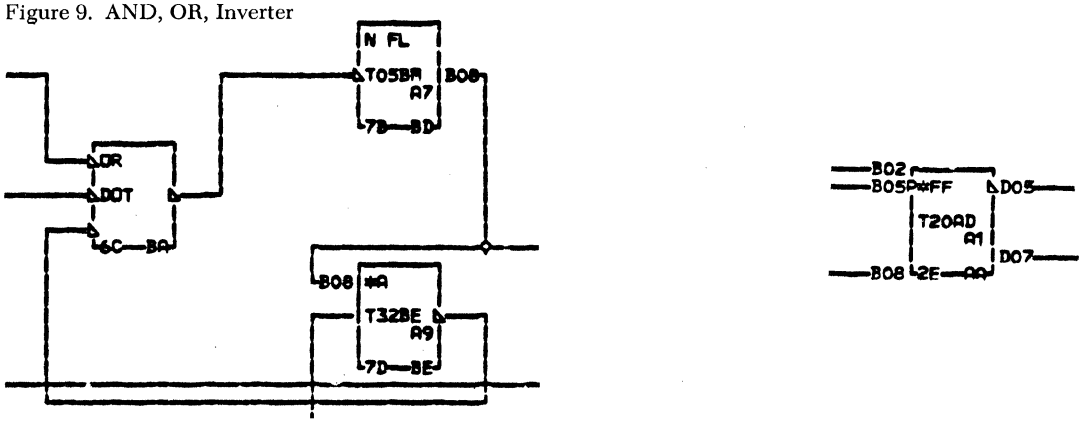


Figure 10. Flip Flop and Flip Latch

Output Line

On each output line (Figure 4) leaving the ALD page, the sink page number (where the line is going), the line name (with the sign of the active state of the line), and the line origin are printed.

The line origin is composed of the serial number of the last logic block before the line name and the number of the printing line of that block.

Whenever the output line branches to several pages, the other "to" pages are listed below the sink page number.

In Figure 4, the top output line is "TC128 -2 Read Data Line AF4." The sink page number is TC128 (the page where the line is going); the active state of the line is minus (−) and a description of the line would be "2 Read Data Line"; the source point is the logic block whose serial number is AF, and the line leaves the block at position 4.

Logic Circuit Blocks

AND, OR, and Inverter Circuits

The basic logic blocks (Figure 9) are the AND (A), OR (OR), and the inverter (N). Almost all other circuits can be built from a combination of these basic circuits. Specifically:

AND circuits (either diodes or transistors) have the designated output when all inputs are at the designated level.

OR circuits (either diodes or transistors) have the designated output when one input is at the designated level.

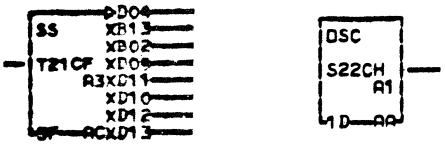
Inverters change the line from one level to the other as designated. (The inverter is really an AND circuit with one input.)

Bi-Stable Circuits

The basic SLT logical storage blocks (Figure 10) are the flip flop (FF), the flip latch (FL), and the polarity hold (PH). Each may be a single circuit or a combination of individual AND, OR, and inverter circuits.

Singleshot and Oscillator Circuits

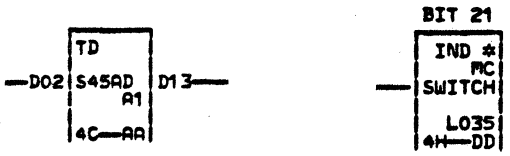
The basic timed storage block (Figure 11) is the singleshot. The oscillator produces crystal-controlled timing pulses.



•Figure 11. Singleshot and Oscillator

Driver Terminator Circuits

A need for varied circuits exists in all machines. Some of these circuits are (Figure 12): indicator and relay drivers, line terminators, converters, and integrators.



•Figure 12. Miscellaneous Circuits

Combination Circuits

Circuits may be combined to provide a particular need or function. These combinations may be:

Exclusive OR

The output of an exclusive OR (OE) (Figure 13) is at its indicated polarity when one and only one of its inputs is at its indicated polarity.

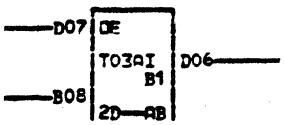


Figure 13. Exclusive OR

Threshold (A-2, A-3, A-(n))

The output of the threshold (Figure 14) is at its indicated polarity when and only when the number of its inputs which are at their indicated polarity reaches or exceeds the number specified in the function symbol. The A-(n) symbol has at least three inputs. The number specified in the symbol may not be 1, nor may it be equal to the number of inputs or their total weighted value.

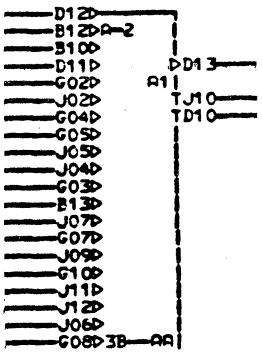
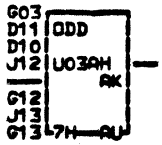


Figure 14. Threshold Circuit (A-2)

Odd Count

The output of odd count (Figure 15) is at its indicated polarity when and only when an odd number of its inputs are at their indicated polarity.



•Figure 15. Odd Count

Even Count

The output of even count (Figure 16) is at its indicated polarity when and only when an even number of its inputs are at their indicated polarity.

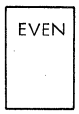


Figure 16. Even Count

Special Circuits

Under certain conditions a block will have a "special" designation. These conditions, both of which must exist, are:

1. The function is not covered by any single block symbol.
2. The function cannot be expressed in terms of an interconnected set of individual block symbols.

The functions of a special block are described on the ALD page, either at the logic block or in the comment area with a reference note in the title area of the block.

Pseudo Blocks

DOT Blocks

The DOT block (Figure 17) is a pseudo block that is used whenever a functional DOT is performed. It is necessary because a net can have only one source. The DOT block has the function, DOT, a print position, and a serial number.

Figure 17. Dot Blocks

The DOT block by definition is the block used on logic pages to show the DOT OR and DOT AND functions. This function is physically accomplished by tying two signals together at a pin. In this manner one logical net may be combined with other logical nets by means of a DOT block to show a single combined physical net.

A net is a complex of nodes (normally pins or connectors on a logic page) that are all common electrically. A node is one end of a circuit that is a point of a net, e.g., a pin on a card, a connector on a board or panel. A source is the beginning of a net from which the signals flow. A sink is the end or ends of a net to which signals flow.

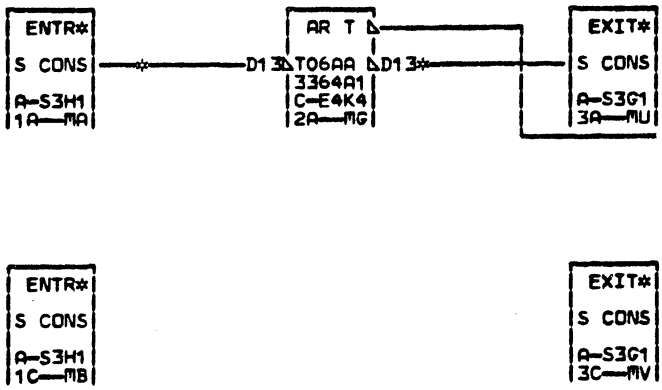
Entry and Exit Blocks

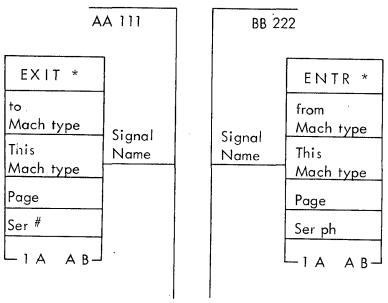
Entry and exit blocks (Figure 18) can be used to show cross-referencing from one machine to another or when a line crosses a machine type. The information may be associated with the line name or it may be shown in a pseudo block. These pseudo blocks are identified by an asterisk in the sixth position of line 1. The machine type from which or to which the line is coming is on line 2. The machine type where the logic block is located is on line 3. The page of the other end of the line is shown on line 4. Line 5 is the serial number of the block on the other end of the line. The print location and serial number of the logic block are shown in line 6.

Service-Voltage Logic Blocks

The four-character mnemonic code (SERV) identifies one type of the pseudo block. An asterisk (*) in the first character of line 1 indicates that the inputs are in particular positions; the asterisk (*) in the last character of line 1 indicates that the block is special. Line 3 identifies the voltage. Line 5 locates the card socket. The logic block pin numbers identify which pins are wired for the particular voltage.

A SERV logic block (Figure 19) indicates that a voltage is wired into a connector area by printed wiring.

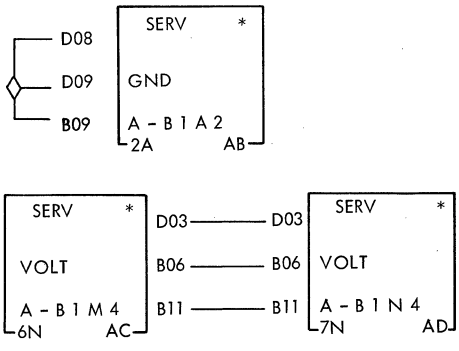




•Figure 18. Entry and Exit Blocks

NOTE: No voltages are present in each outside column (A and N) of card sockets on the board.

Normally the sockets in columns A and N of the board are used for cable connectors. When these sockets are used for cards, service voltages are brought to these sockets by printed wiring. This arrangement is shown with the SERV special block (Figure 19). When a half cable connector plugs into columns A or N on the printed board, additional ground wires are shown on the ALD's in the lower half of the socket. A board is not normally wired this way. Normally, on a given board all blocks that are used for service voltages appear on the same ALD page(s).



•Figure 19. Service-Voltage Logic Blocks

Cable Logic Blocks

Two logic blocks (Figure 20) are used to define each cable: one logic blocks shows the "from" location; the other logic blocks shows the "to" location. Line 1 contains CABL* for regular cables (both intergate and intragate) and XOVR* for crossover cables.

Basic data in the block provide cable block identification: location of the end points, cable assembly part number, location suffix (half cable can be plugged into top or bottom section, or left or right section of the connector socket), intergate sequence numbers, and orientation of intergate cable.

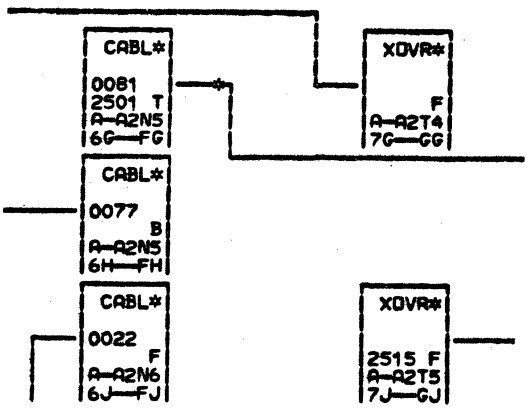
The code used in Figure 20 is:

NNNN	last four numbers of the cable assembly drawing appear only on the "from" block. The first three numbers (580) are understood as relating to the part number.
P	socket portion used, i.e., T for top, B for bottom, F (or blank) for full; this will appear as a location suffix.
QQQQ	installation sequence number (required in both blocks of the intergate cable).
GGBBSS	gate, board, and socket for the respective end of the cable.
Z	L or R indicates left or right for the direction this cable takes in leaving the board specified in the "from" block. (Assume a position facing the card side of the board.)

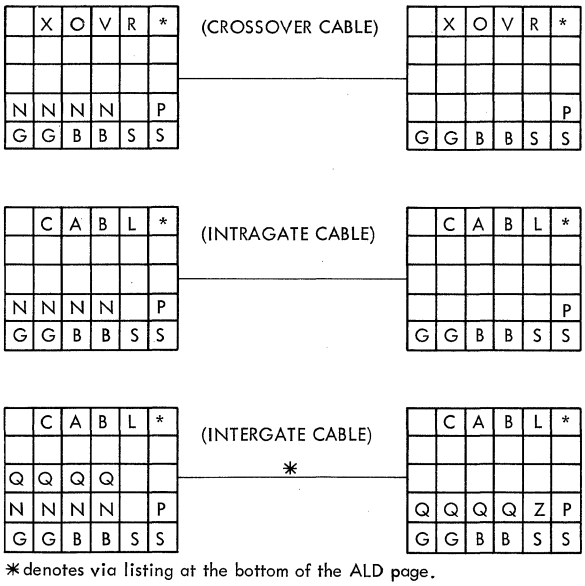
Cable blocks will have "from" and "to" orientations similar to the orientations of the particular cable assembly reference drawings.

Line 2 may contain an additive card code, but it is not required.

Installation Sequence: Intergate cables are divided into groups; each group contains all of the cables connecting a particular pair of logic or I/O gates. The group number is the first number of the code QQQQ. It defines the cabling sequence required for gate pairs. The number may be 1 through 9. Other numbers of the code QQQQ are the installation order of the cables in the group, with the lower numbers being installed first, advancing in order to the higher numbers.



Cable Block Formats



*denotes via listing at the bottom of the ALD page.

•Figure 20. Cable Logic Blocks

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Via Points: The point at which the intergate cable leaves the gate is designated as a via and the point at which it enters the "to" gate is designated as a via.

Via coordinates identify channel intersections as well as identify segments of the vertical channel. Within the channel intersection and within the vertical segments, channel coordinates are specified. It is at these coordinates that the cable is folded and the lengths are specified.

The via points are shown in order from one end of the cable to the other. The format of routing vias is in the form FFG-VVCC---; FF designates frame, G- designates gate, VV designates via coordinate, CC designates channel coordinate, and --- (three dashes) fill out the 11 characters. An example is O1A-C2D5---.

Cable Routing: The routing of the cable is given by via and channel coordinates (Figure 21). These coordinates will be identified by the asterisk (*) on the line between the to and from block. The asterisk (*) references the connector field at the bottom of the (cable) ALD logic page.

The general form of the via designation is:

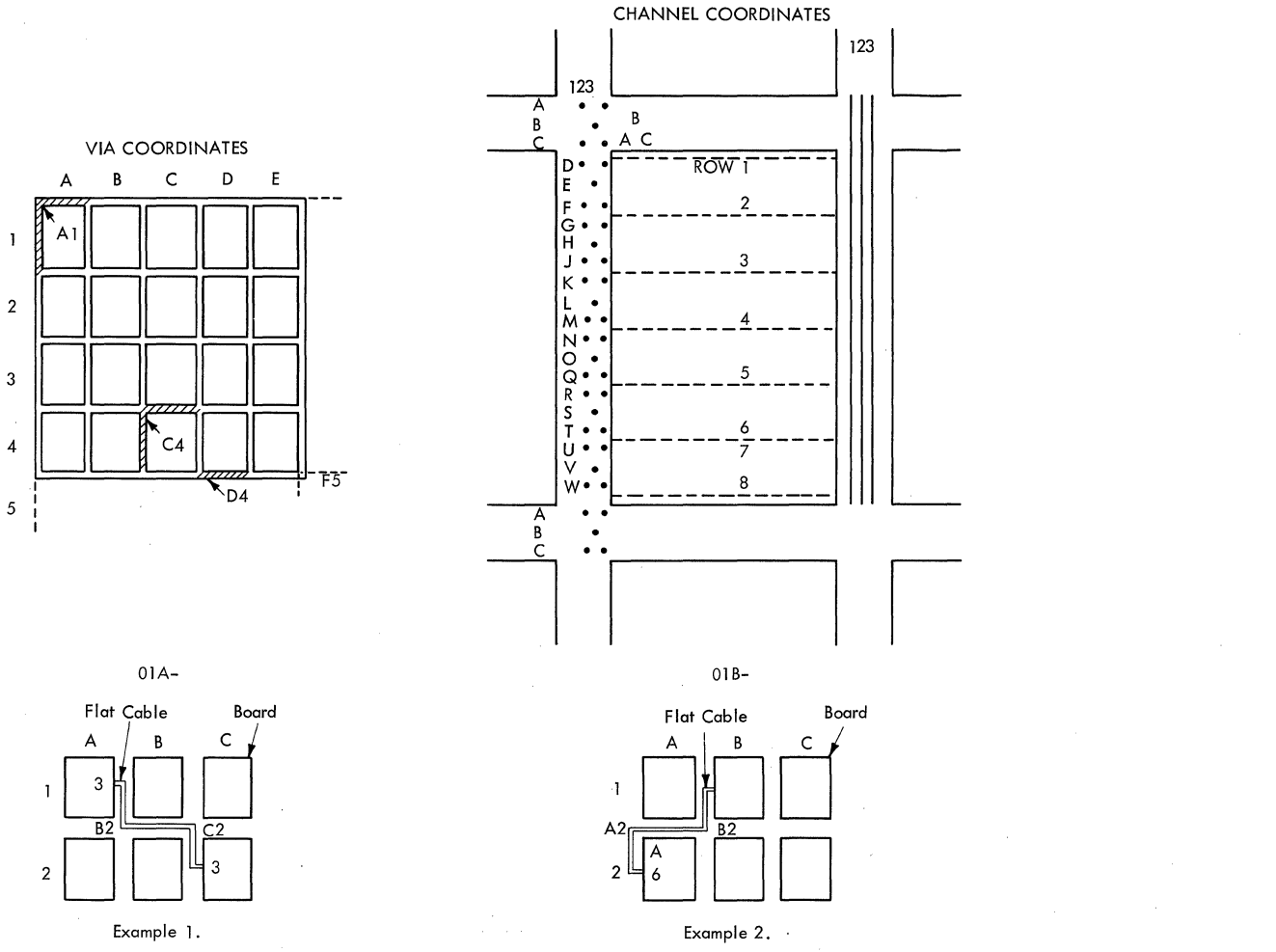
01	A-	C2	D5	- - -
		Via	Channel	Not
Frame	Gate	Coordinate	Coordinate	Used

The general form of a logic connector is:

01	A-	D3	B2	D09
Frame	Gate	Board	Socket	Pin

Example 1 in Figure 21 shows a six pack cable on gate A in frame 01 between board A1 socket N3 and board C2 socket A3. In this example the connector listing is:

```
01A-A1N3      (appears in CABL* block)
01A-A1N3      Identification
01A-B1H2---
01A-B2B2---   Cable Vias
01A-C2B2---
01A-C2H2---
01A-C2A3      (appears in second CABL* block)
```



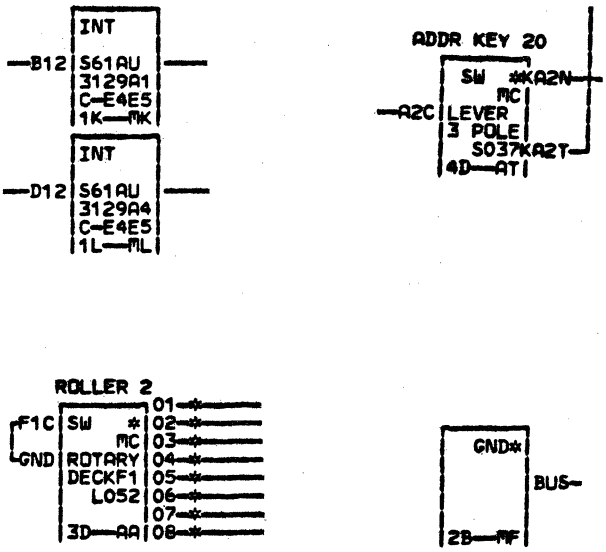
•Figure 21. Cable Routing

Example 2 in Figure 21 shows a split pack cable on gate B in frame 01 between board B1, top half of the socket A4, and board A2, bottom half of socket A6. In this example the connector listing is:

```
01B-B1A4T      (in CABL* block)
01B-B1K1---
01B-B2C1---    Cable Vias
01B-A2C3---
01B-A2T3---
01B-A2A6B      (in CABL* block)
```

Component and Auxiliary Logic Blocks

Special components such as switches, relays, fuses, resistors, capacitors, R-C networks, thermals, and indicators are shown on the ALD's. An asterisk (*) in the last position of the function line indicates a special block. Examples of component logic blocks are shown in Figure 22. See "Symbology and Definitions."



•Figure 22. Component Logic Blocks

Engineering Changes

To the left of the title block, 20 engineering change levels, with dates, may be listed in two columns of 10 each. For example Figure 3 shows EC 25355C on 05-07-64.

Comments

Comments are found at the bottom left of the page. There may be up to 10 lines of comments.

Connector Listing

Connectors (Figure 4) are listed at the bottom center of the page. There is space to list 100 connectors. The general form of a logic connector is:

O1	A-	D3	B2	D09
Frame	Gate	Board	Socket	Pin

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- **The basic SLT circuit is the AND-OR-Inverter (AOI).**
- **Circuit Speeds are: 700 ns, 30 ns, and 5-10 ns.**
- **Voltage levels are: 0.0v to +3, +12v.**
- **Logic may be diode, transistor, or a combination.**
- **A logic block may use different circuits for each of the three speeds.**

A transistor circuit can be understood by knowing the logic relation of the inputs to the outputs, or by knowing the power dissipation of components and the relation of loading and input transition times to circuit delays.

This manual is written for those who service, rather than design, machines using SLT circuits. For this reason circuit information is restricted to:

1. Relation of circuit inputs to circuit outputs.
2. How the circuit converts input signals to output signals.
3. Important input and output requirements.

The manual describes only those SLT circuits that are most widely used. Less widely used circuits are described in FE manuals covering specific machines.

Circuit Speeds

Presently there are three circuit speeds, depending upon the semiconductor (diode and/or transistor) and its switching speed. Switching speeds are in the order of 10, 30, and 700 nanoseconds for each logical block.

Circuit Voltages

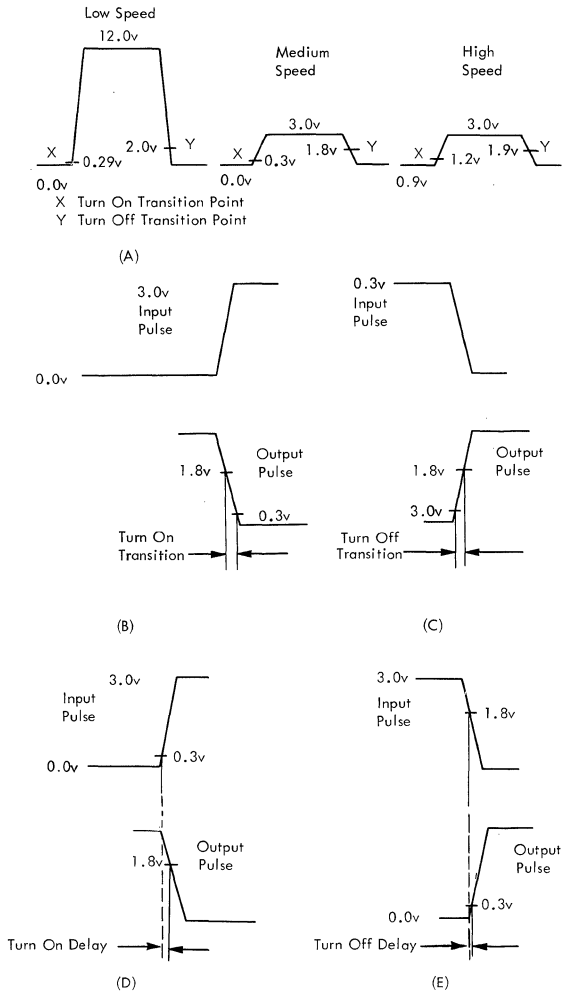
Approximate voltage levels for each of the three speeds of circuits are:

10 ns circuit:	+0.9v, most negative; +3.0v, most positive.
30 ns circuit:	+0.0v, most negative; +3.0v, most positive.
700 ns circuit:	+0.0v, most negative; +12.0v, most positive.

Transitions

Transition (Figure 23A) is the time a transistor output takes to switch from one logic state to the other. The voltage levels at which the transitions are measured for the different families are:

FAMILY	TRANSITION POINTS
5-10 ns, high speed	+1.2v & 1.9v
30 ns, medium speed	+0.3v & 1.8v
700 ns, low speed	+0.29 & 2.0v



•Figure 23. Transitions and Circuit Measurements

Switching times include turn-on transition, turn-off transition, turn-on delay, and turn-off delay. The different transition times are turn-on-transition, and turn-off transition. These values are basically the same for each of the circuit families. The major difference is that the transition points and voltage levels vary for each family.

Turn-on transition (Figure 23B) is the switching time from an off state to an on state. Turn-on transition is measured on the output waveform from a specified value in the nonconducting state, to a specified value in the conducting state.

Turn-off transition (Figure 23C) is the switching time from an on state to an off state. Turn-off transi-

tion is measured on the output waveform from a specified value in the conducting state to a specified value in a nonconducting state.

Turn-on delay (Figure 23D) or *turn-off delay* (Figure 23E) is the time the circuit takes to change its output state due to a change in the state of the input. Switching time is measured from a point where the input waveform has reached a specified value to a point where the output waveform has reached a specified value.

Basic Circuits

The basic circuit of SLT is the AOI (AND-OR-inverter) (Figures 28, 29, and 37). The AOI is comprised of an AND gate, an OR circuit, and an inverter. These three circuits comprise most of the design circuits for the computer.

The Diode AND Gate

The AND gate is a diode AND circuit (Figure 24A). An AND circuit may be considered a plus AND or a minus OR. The logical operation of these circuits requires:

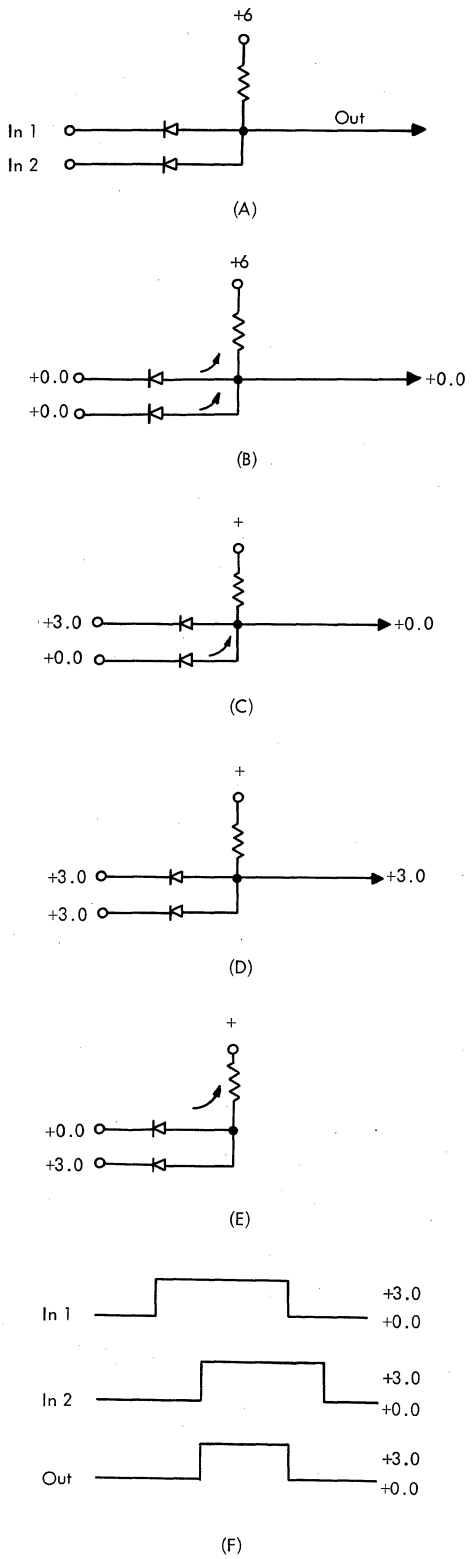
+AND circuit: must have all plus inputs for a plus output.
−OR circuit: has a minus output if any input is minus.

The two circuits are identical; only the logical usage is different. The +AND circuit insures that both inputs are up before the output comes up; the −OR circuit has a minus output as long as any input is down. In this simplified description, the example specifies two diodes. The same descriptions, however, applies to (n) diodes. If both inputs are minus, the polarity is correct, and both diodes will conduct (Figure 24B). The resultant current flow through R causes a voltage drop to maintain a minus voltage output. Because of the forward resistance of the diodes, the output voltage will be approximately that of the input voltage.

If input 1 change instantaneously to a positive voltage, diode 1 is cut off because the cathode is more positive than the anode (Figure 24C). Diode 2, with a minus voltage on its cathode, maintains conduction and the output voltage remains unchanged (minus).

When input 2 also changes to a positive voltage, diode 2 is cut off (Figure 24D). When the output voltage reaches +3.0v, the diodes go back into conduction. When input 1 falls to +0.0v, diode 1 conducts harder, and diode 2 is cut off (Figure 24E). The output follows the input down to +0.0v. When input 2 falls to +0.0v, diode 2 goes back into conduction to help to maintain the +0.0v output.

In summary, the output voltage of a positive AND circuit approximately equals the most negative input voltage. This statement applies regardless of the number of inputs.



•Figure 24. The AND Gate

The Diode OR Circuit

Circuit configurations (Figure 25A) for the +OR and the −AND circuits are identical. Logical operation of these two circuits requires:

+OR circuit: gives a plus output, if an input is plus.
−AND circuit: requires all minus inputs for a minus output.

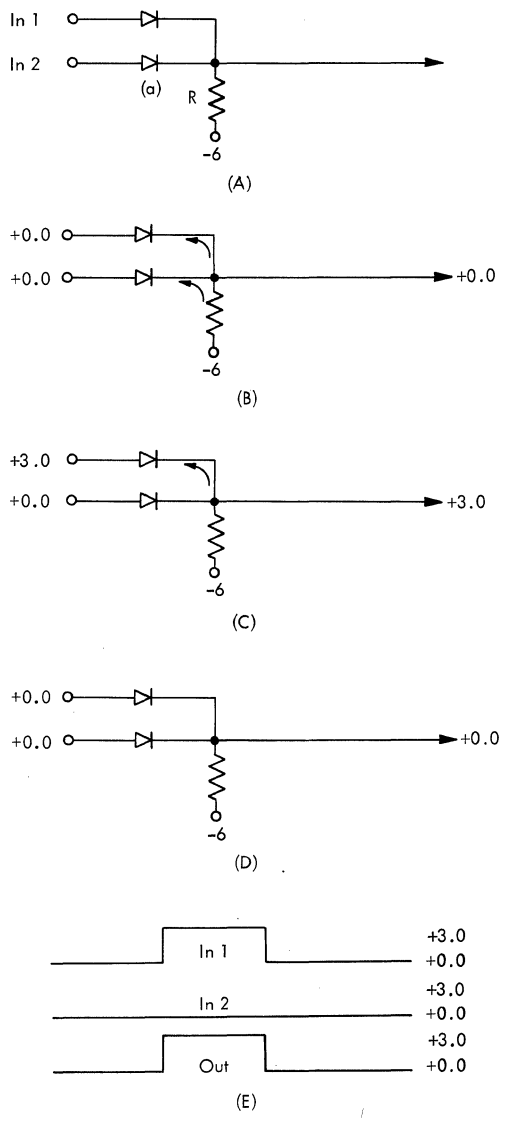
Therefore, the +OR circuit differs from the +AND circuit because the OR circuit needs only one input up to bring the output up.

(In this simplified description the example specifies two diodes but the description applies as well to (n) diodes.) The operation is as follows. If both inputs are at the most negative level, the polarity is correct so that both diodes will conduct (Figure 25B). The voltage drop across the load resistor (R) sets the output level.

If either input diode rises to the most positive level, that diode conducts harder (Figure 25C). The other diode then cuts off and the output follows the input rising to the most positive level of input voltage. Normally only one input to an OR circuit comes up at a time.

When the input that was up drops, the input diode is cut off (Figure 25D). The input diode conducts again when the output voltage reaches a point slightly more plus than the most negative input level.

In summary, the output voltage of a positive OR circuit approximately equals the most positive input voltage.



•Figure 25. The OR Circuit

The Inverter

In SLT circuits the transistor provides inversion. The inverter used in SLT applications is the grounded emitter transistor of the NPN (P base) type.

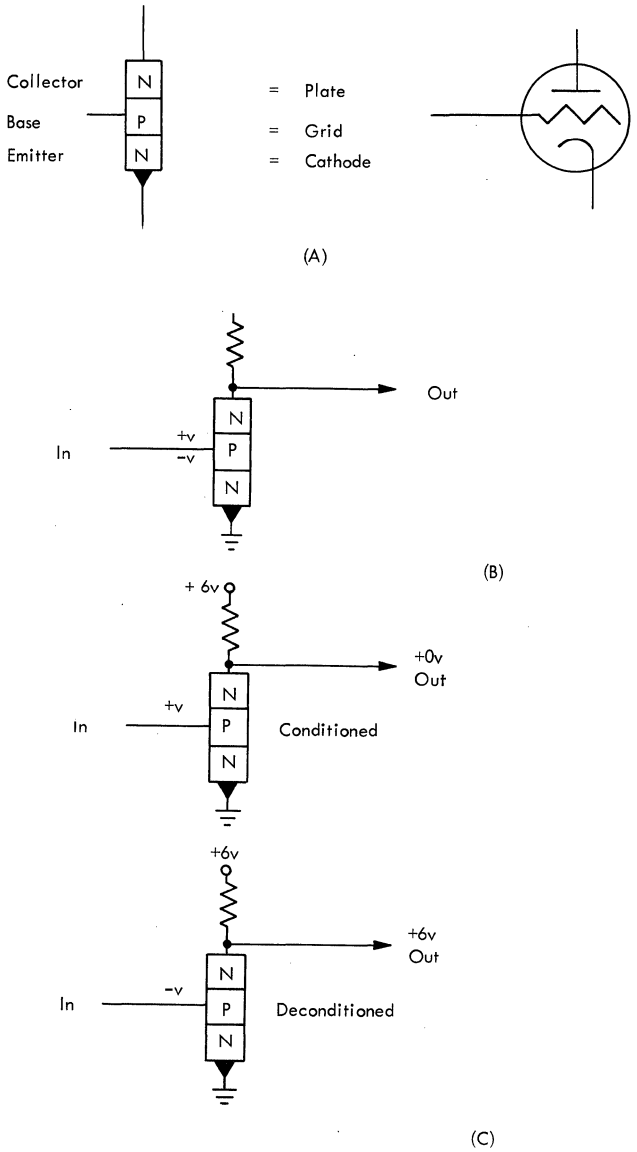


Figure 26. The Inverter

The voltages applied to the elements of a transistor are the basis for controlling the transistor's conduction. Figure 26A compares conduction for a transistor and a tube. Transistor conduction, as defined here, is current which flows through the collector or emitter circuit.

Bias is the term given to the control potential in both transistor and tube applications. Bias voltage is the DC voltage difference in potential between the base (grid) and the emitter (cathode). Bias voltage is the controlling factor in transistor conduction.

To determine conduction control, consider the emitter voltage held at a constant ground level; then apply the input voltage to the base (Figure 26B).
To control the conduction of the transistor, the base voltage must be capable of level either above or below the emitter voltage.

The following rules cover conduction:

1. An NPN (P base) transistor will conduct if its base is more positive than its emitter.
2. A PNP (N base) transistor will conduct if its base is more negative than its emitter.

In tube theory if the dynamic resistance between the cathode and plate is decreased by the grid voltage, current will flow in the plate circuit. This rule is also true in transistors: the bias potential decreases the dynamic resistance between the emitter and collector so that current will flow through the transistor. Otherwise, the bias potential will increase the dynamic resistance of the transistor so that little or no current will flow. This direction of bias potential is called either "forward bias," which causes conduction, or "reverse bias," which cuts off conduction.

The property of displaying a large or a small resistance is the primary consideration in analyzing basic transistor (and tube) circuits.

The following rules govern resistance:

1. A conducting (or "conditioned") transistor presents small resistance to current flow.
2. A cut-off (or "deconditioned") transistor presents a large resistance to current flow.

Even though direction of current flow through a transistor is rel ely unimportant in analyzing a circuit, remember that: (1) Current (electron) flows from emitter to collector in a NPN transistor; and (2) Current flows from collector to emitter in a PNP transistor. Remember also that even though current flows against the direction of the arrowhead indicating the emitter (Figure 26C), current always flows from negative to positive, so that:

1. The collector of an NPN must be returned to a more positive voltage than it emitter.
2. The collector of a PNP must be returned to a more negative voltage than its emitter.

Operating Characteristics

There is approximately a 0.6v drop across a conducting diode. A conducting diode will have +0.6v on the anode, if it has ground (0.0v) on the cathode.

A transistor with a grounded emitter will be cut off with 0.3v at the base. An input voltage above 0.3v will start a transistor into conduction. With 0.8v at the base, the transistor will be conducting at saturation.

The translate diode (Figures 28, 29, diode 5, i.e., the diode between the AND gate and the transistor acting as an OR diode) suppresses noise and provides uniform voltage at the base of the transistor. The voltages are 0.3v for cut off and 0.8v for saturation.

Circuit Descriptions

AND-OR-Inverter Circuits

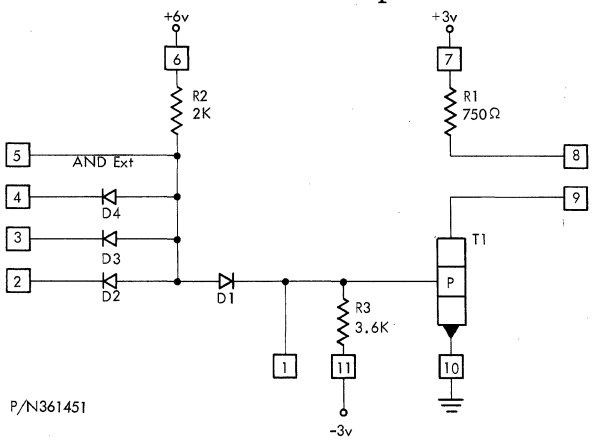
The AND-OR-inverter circuit is used in many ways. The most frequent uses are described here.

Note that there are differences in the same circuit when it operates at different speeds; i.e., the AOI, medium-speed (Figure 29), and the AOI_{10}, high-speed (Figure 37).

AND Inverter (AI)

The AI (Figure 27) consists of a diode positive AND circuit followed by a saturating transistor inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 is available for extending the fan-in to the AND by connecting it to common-anode diodes from an FDD or AOX module. Pins 8 and 9 are connected on the card for most applications. However, when collectors are dotted, only one collector resistor is needed for the common collector connection. If more collector resistors are connected, the fan-out is reduced accordingly.

The output, pin 9, fans out to a maximum of five AI loads for medium-speed circuits and to a maximum of seven AI/AOI loads for slow-speed circuits.



•Figure 27. AND-Inverter, Medium-Speed (AI)

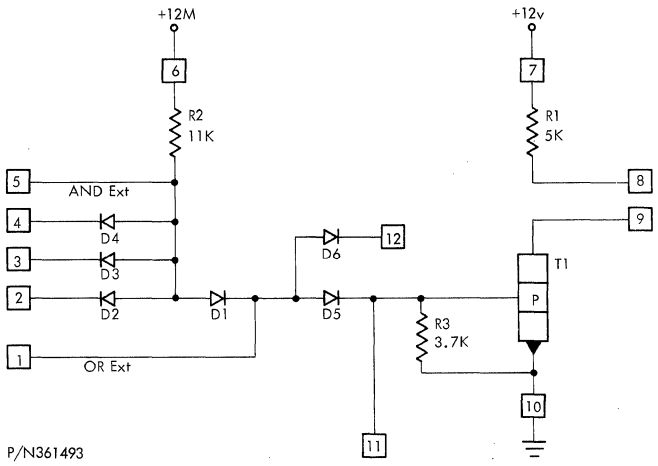
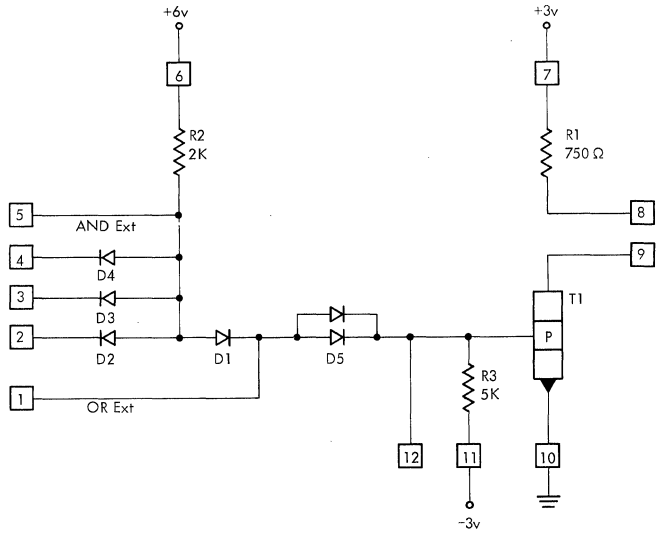


Figure 28. AND-OR-Inverter, Low-Speed (AOI)



•Figure 29. AND-OR-Inverter, Medium-Speed (AOI)

AND-OR Inverter (AOI)

The AOI module (Figures 28 and 29) consist of a three-way diode positive AND function and one diode for an OR function, followed by a saturating transistor inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 extends the fan-in to the AND by connecting it to the common-anode diodes of the FDD module. Pin 1 can extend the OR fan-in from the OR diode of the AOX (or AOX_2) module. The maximum OR fan-in is five.

The output pins, 8 and 9, are connected on the card for most applications. However, when collectors are dotted, only one collector resistor may be connected to retain the specified fan-out capability. The AOI can drive a maximum of five AOI circuits (medium-speed) or seven AI/AOI circuits (low-speed).

AND-OR-Extender (AOX)

The AOX module (Figures 30 thru 34) has two identical extender circuits on one substrate. The extender circuits are used with the AI, AOI, API, and ACT to increase the input capabilities of these circuits. Each extender circuit can:

1. Increase the AND fan-in of the AI and AOI by four.
2. Increase the OR fan-in of the AOI by one while simultaneously increasing and AND fan-in by three.
3. Increase the number of AC gates on one side of one AC trigger (ACT) by three.
4. Provide one DC set input for the ACT.
5. Increase the AND fan-in of the API by four; this requires two extender circuits.

AND-Power-Inverter (API)

The API module (Figure 35) is used as a power inverter with input logic capability. It serves the same logic function as the AI module and can drive more loads than the AI. The API module consists of a three-way

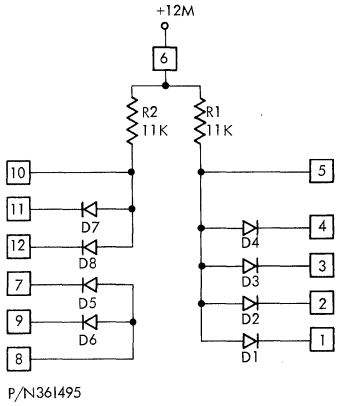


Figure 30. AND-OR-Extender, Low-Speed (AOX_1)

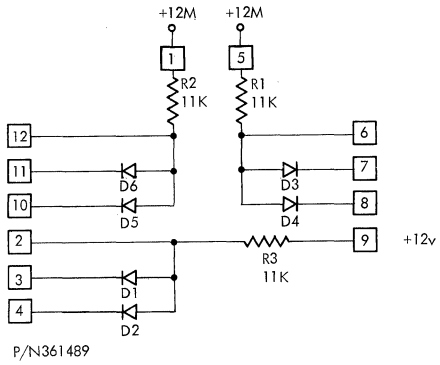


Figure 31. AND-OR-Extender, Low-Speed (AOX_2)

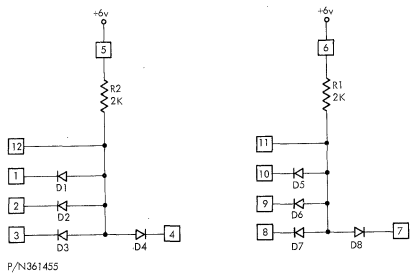


Figure 32. AND-OR-Extender, Medium-Speed (AOX)

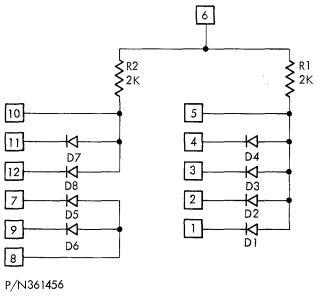


Figure 33. AND-OR-Extender, Medium-Speed (AOX$_B$)

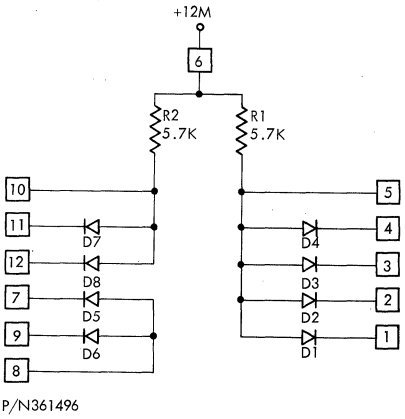
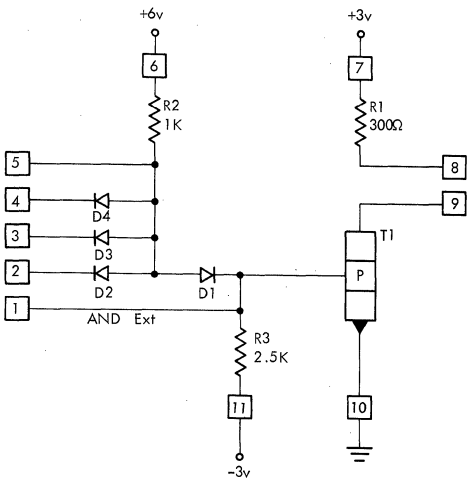


Figure 34. AND-OR-Power-Extender, Low-Speed (AOPX-1)

diode positive AND circuit followed by a saturating transistor power inverter. Pins 2, 3, and 4 are the AND inputs. (Pin 5 is not used to extend the AND circuit. Pin 1 and a special hook-up of AOX's are used.)

Pins 8 and 9 are connected on the card for most applications. However, when the collectors are dotted, only one collector resistor can be connected to retain the specified fan-out capability.



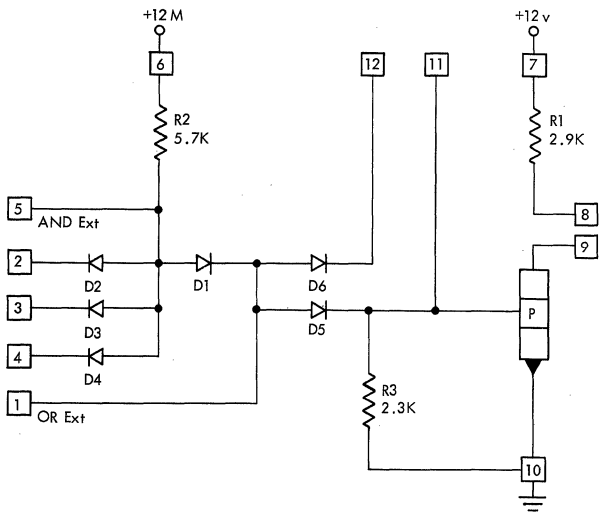
•Figure 35. AND-Power-Inverter, Medium-Speed (API)

The API can drive a maximum of 14 AI/AOI, or equivalent, loads.

AND-OR-Power-Inverter (AOPI)

The AOPI module (Figure 36) consists of a three-way positive AND function and one diode for an OR function, followed by a saturating transistor power inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 extends the AND fan-in by connection to the common-anode diodes of the FDD module. Pin 1 can extend the OR fan-in by connection to the OR diode of the AOPX$_1$ module. The maximum OR fan-in is five. The output pins, 8 and 9, are connected on the card for most applications. However, when collectors are dotted, only one collector resistor may be connected to retain the specified fan-out capability.

The AOPI can drive a maximum of 14 AI/AOI, or equivalent, loads.



•Figure 36. AND-OR-Power-Inverter, Low-Speed (AOPI)

AND-OR-Inverter (AOI$_{10}$)

The AOI$_{10}$ is the basic circuit of a logic family consisting of the AOI$_{10}$, AOI$_{10}$T, and line terminator circuits. Both the AOI$_{10}$ and AOI$_{10}$T are logic circuits with maximum fan-in of five OR inputs and five AND inputs per OR input. The AOI$_{10}$ differs from the AOI$_{10}$T only in input and delay characteristics. The AOI$_{10}$ has better delay characteristics, while the AOI$_{10}$T has a greater positive going-noise rejection level. The AOI$_{10}$ is used when block-to-block wiring lengths do not exceed 12 inches. The AOI$_{10}$T is used when long line lengths or certain logical situations require a greater positive-going noise rejection level.

The output characteristics of the AOI$_{10}$ and AOI$_{10}$T circuits are identical. Both circuits have maximum fan-outs of 10 AOI$_{10}$ and/or AOI$_{10}$T circuits. Either circuit can drive a 93-ohm transmission line terminated by an

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LTN or LSA. Outputs of both the AOI_{10} and/or $AOI_{10}T$ can be wired together to perform a negative OR function.

The AOI_{10} circuit uses the 12-pin AOI_{10} module (Figure 37) or the 16-pin $AOI_{10}B$ module (Figure 38). The 12-pin AOI_{10} module has one OR gate containing three positive AND diode inputs. The 16-pin $AOI_{10}B$ module contains a two-way OR gate with each OR gate having three positive AND diode inputs. Each module has an OR-extender pin and an AND-extender pin.

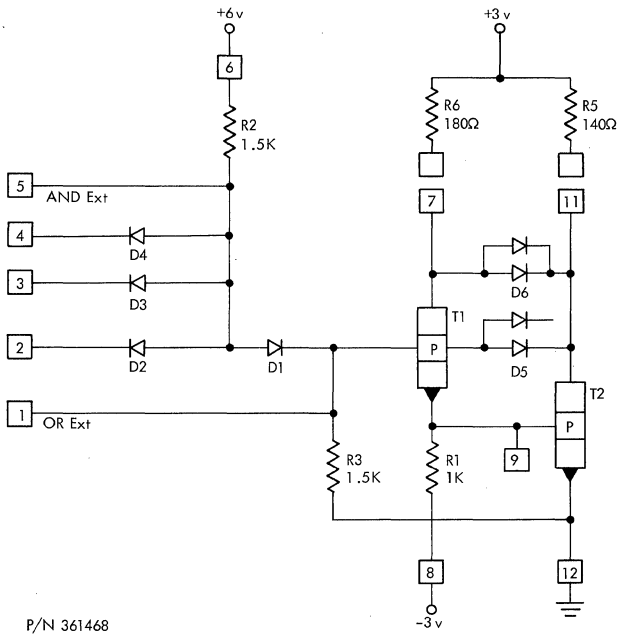
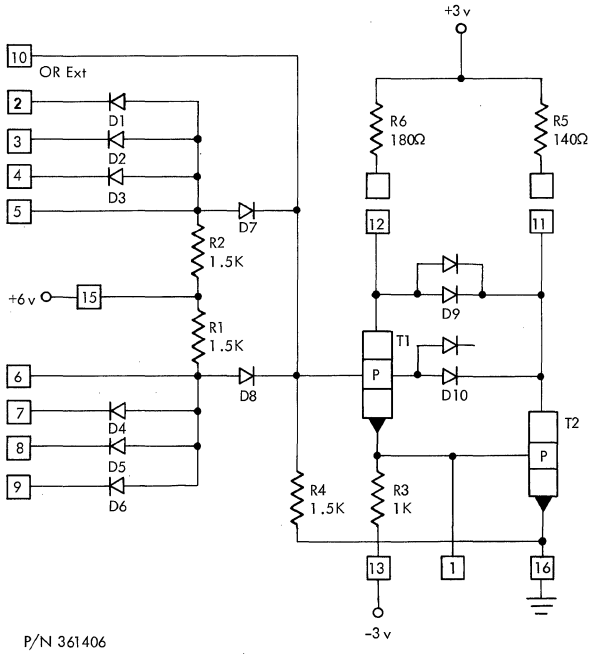


Figure 37. AND-OR-Inverter, High-Speed (AOI_{10})



•Figure 38. AND-OR-Inverter, High-Speed ($AOI_{10}B$)

The AOX_{10} module (Figure 39) is used to extend the OR function of the AOI_{10} circuit. The FDD_{10} module (Figure 41) is used to extend the AND function of the AOI_{10} circuit. In addition, the diodes on the AOX_{10} (Figure 39) and $AOX_{10}T$ (Figure 40) modules may be used to extend the AND function.

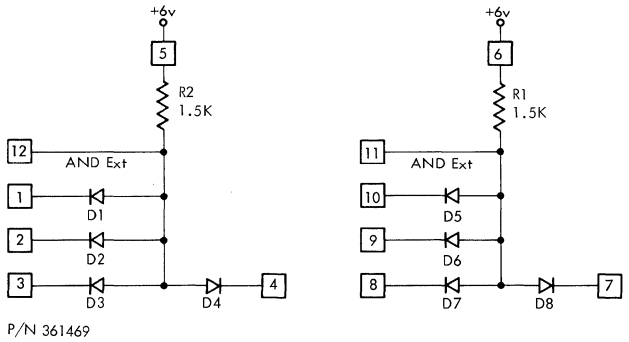


Figure 39. AND-OR-Extender, High-Speed (AOX_{10})

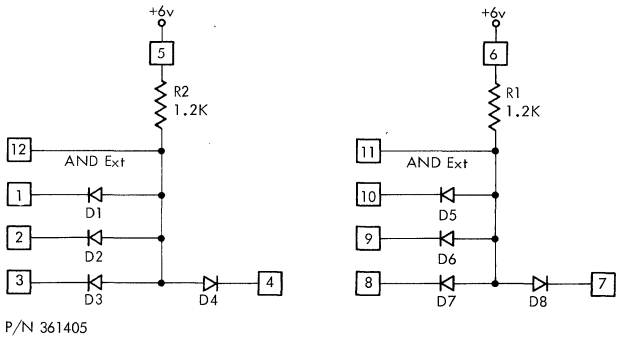


Figure 40. AND-OR-Extender, High-Speed ($AOX_{10}T$)

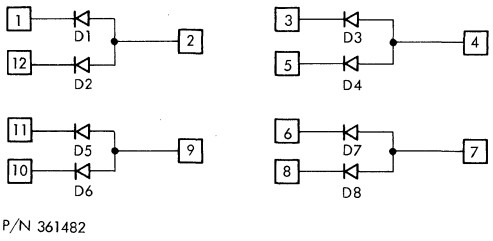
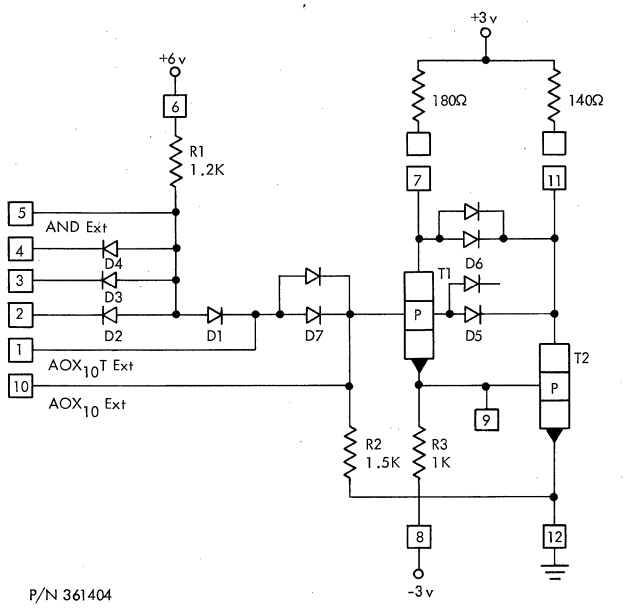


Figure 41. Four Double Diodes, High-Speed (FDD)

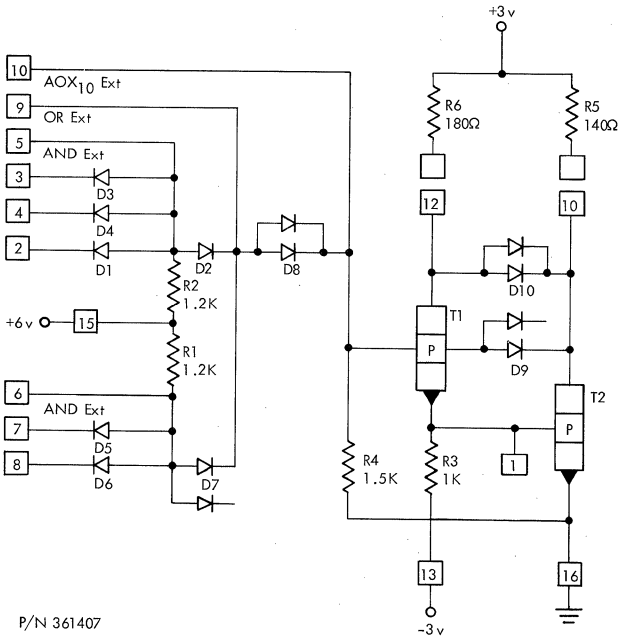
AND-OR-Inverter ($AOI_{10}T$)

The $AOI_{10}T$ circuit provides the same system function as the AOI_{10} circuit, except that an additional diode level shift is incorporated to give the circuit additional immunity to positive noise pulses. It may be used in line terminator applications and other system locations requiring greater immunity to positive noise than the AOI_{10} circuits provides.

The $AOI_{10}T$ circuit uses either the 12-pin $AOI_{10}T$ (Figure 42) module or the 16-pin $AOI_{10}BT$ module (Figure 43) plus an external resistor package containing the collector resistors R5 and R6.



•Figure 42. AND-OR-Inverter-Terminate, High-Speed ($AOI_{10}T$)



•Figure 43. AND-OR-Inverter, High-Speed ($AOI_{10}BT$)

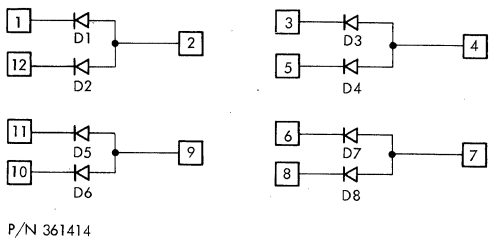
The $AOI_{10}T$ module consists of a three-input positive AND diode gate, followed by a single OR diode, a level shifting diode pair, and a non-saturating inverter amplifier. The basic three-way AND function can be extended by connecting the diodes of the FDD_{10} module to the AND extend input (pin 5) of the $AOI_{10}T$ module. The AOX_{10} (Figure 39) or $AOX_{10}T$ (Figure 40) modules may be used for the same purpose if pins 5 and 6 are not connected to +6v. The trivial one-way OR function of the $AOI_{10}T$ module may be extended by connecting the $AOI_{10}T$ module to pin 1 of the $AOI_{10}T$ module. The OR function can also be extended by connecting an AOX_{10} module to pin 10. However, in this case the level shift diode pair is by-passed. Therefore, the input legs so involved do not have the extra noise immunity.

The $AOI_{10}BT$ module is identical to the $AOI_{10}T$ except that an extra AND/OR leg is provided to make it a two-way OR as compared to a trivial one-way OR for the $AOI_{10}T$. Also the AND gate on this extra leg is only two-way, compared with three-way for the other leg as on the $AOI_{10}T$. The basic AND/OR capability may be extended in the same manner as the $AOI_{10}T$.

The fan-in for the AND and OR functions is limited to five each. Fan-out is limited to 10. Circuit outputs may be wired together.

AND-OR-Inverter (AOI_{11})

The AOI_{11} circuits are similar to the AOI_{10} circuits. They differ in speed and in some component values. The circuits that make up the AOI_{11} circuits are: FDD_{11} (Figure 44), AOI_{11} (Figure 45), $AOI_{11}B$ (Figure 46), $AOI_{11}T$ (Figure 47), $AOI_{11}BT$ (Figure 48), and AOX_{11} (Figure 49).



•Figure 44. Four Double Diodes (FDD_{11})

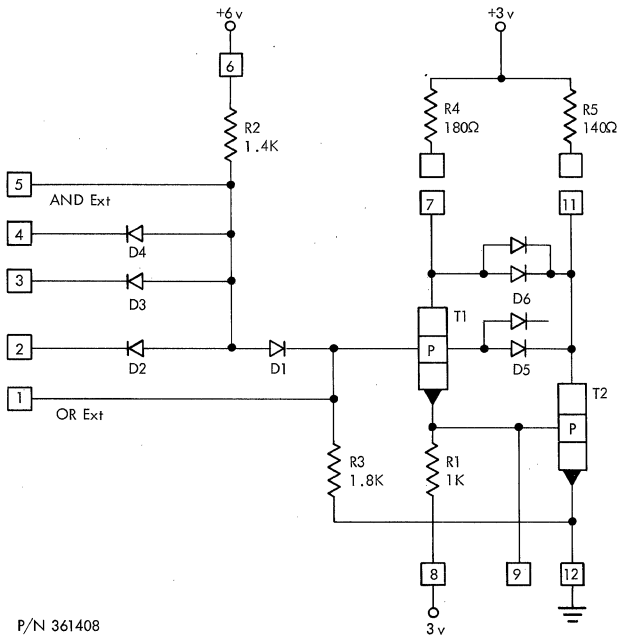
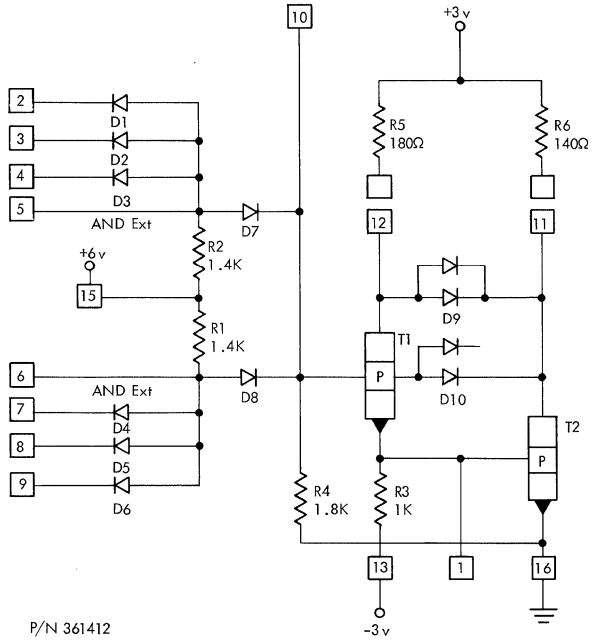


Figure 45. AND-OR-Inverter, High-Speed (AOI_{11})



•Figure 46. AND-OR-Inverter (Two-Way OR), High-Speed ($AOI_{11}B$)

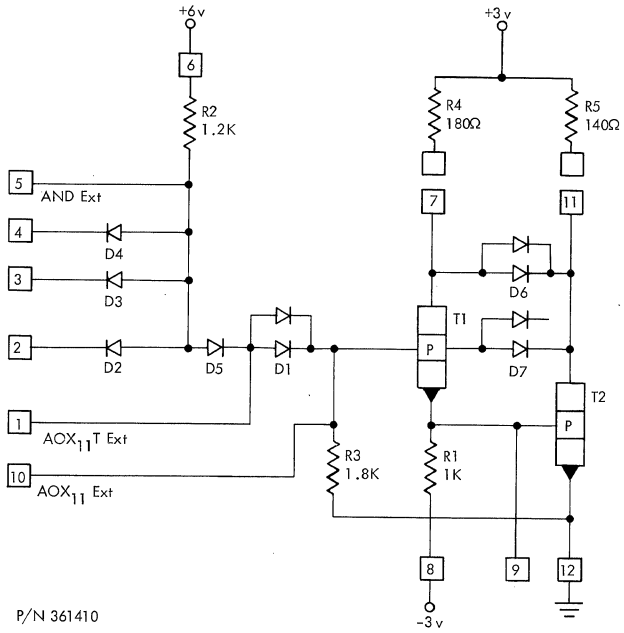


Figure 47. AND-OR-Inverter-Terminate, High-Speed ($AOI_{11}T$)

Exclusive OR Circuits

Exclusive OR (XOR)

This circuit (Figure 50) performs the exclusive OR of the signals applied to pins 6 and 3 when pins 6 and 1 are tied together. When the inputs are both up or both down, the output is at a potential of less than 0.30v. When the inputs are not identical (i.e., one up and one down), the output is between 2.0v and 3.0v, depending on the loads.

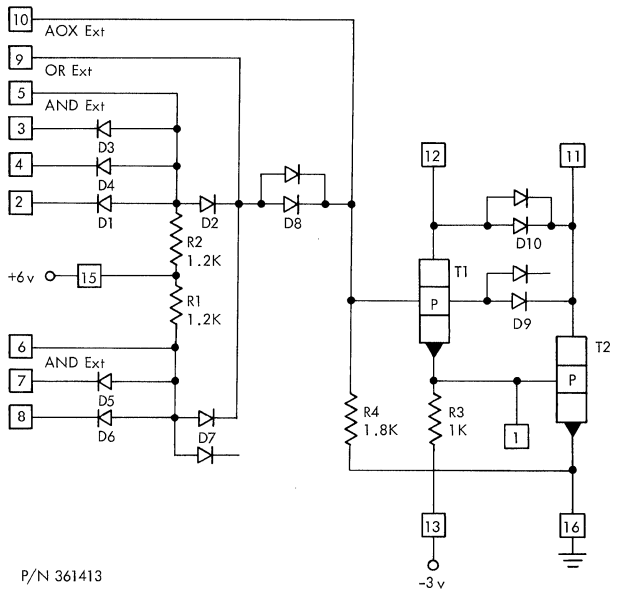


Figure 48. AND-OR-Inverter, High-Speed ($AOI_{11}BT$)

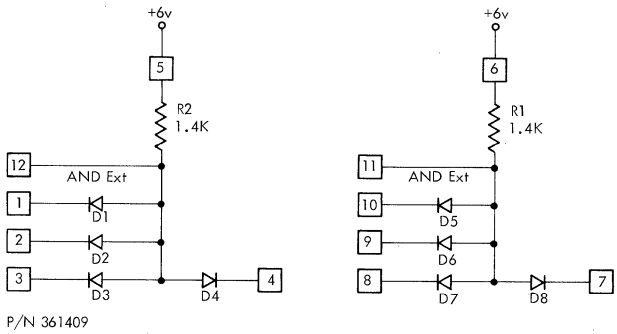
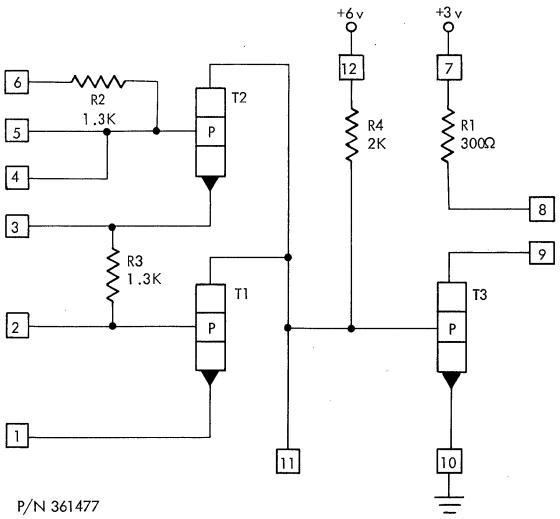


Figure 49. AND-OR-Extender, High-Speed (AOX_{11})



•Figure 50. Exclusive OR, Medium-Speed (XOR)

The XOR module will not perform the exclusive OR latch function. The XOR-L module is the exclusive OR latch.

Exclusive OR Latch (XOR-Latch)

The XOR latch (Figure 51) has a single bi-stable output that can be changed by proper sequencing of the control and data inputs. The inputs can be used in either sequence 1 or sequence 2.

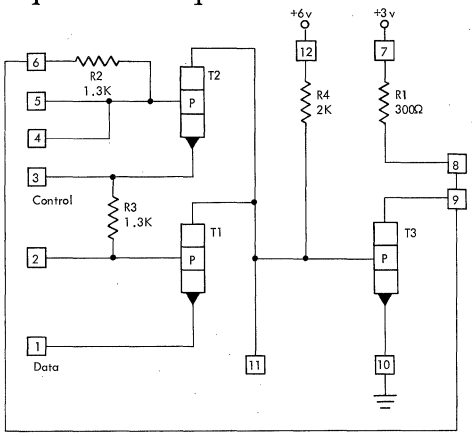


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Figure 51. Exclusive OR Latch, Medium-Speed (XORL)

Sequence 1:

a. Data Line Up — With the rise of the clock pulse the output is set to the 0 state. All further changes in the control line will not affect the state of the latch.

b. Data Line Down — With the rise of the clock pulse the output is set to the 1 state. All further changes in the control line will not affect the latch state.

Sequence 2:

a. Data Line Up — With the fall of the clock pulse the output is held in the 0 state.

b. Data Line Down — With the fall of the clock pulse the output is held in the 1 state. In either sequence 1 or 2, the control is normally down.

After the fall of the control line, changes in the data line will not affect the latch state.

Bi-Stable Circuits

Flip Flop (FFL)

The FFL (Figure 52) consists of two cross-coupled AI modules, an R-C pack, and an R-pack. The AI's are fed at the cathode of D6 through a 175 pf capacitor from the negative going transition of an AC set pulse at the AC input. During the negative transition, currents from the AND resistor of the ON transistor and 30K bias resistor are directed into the collector of the AC set driver. This forces the ON transistor off. As a result the other transistor will turn on.

Each side of FFL has two DC set/reset inputs available, which can be driven from any low-speed logic block.

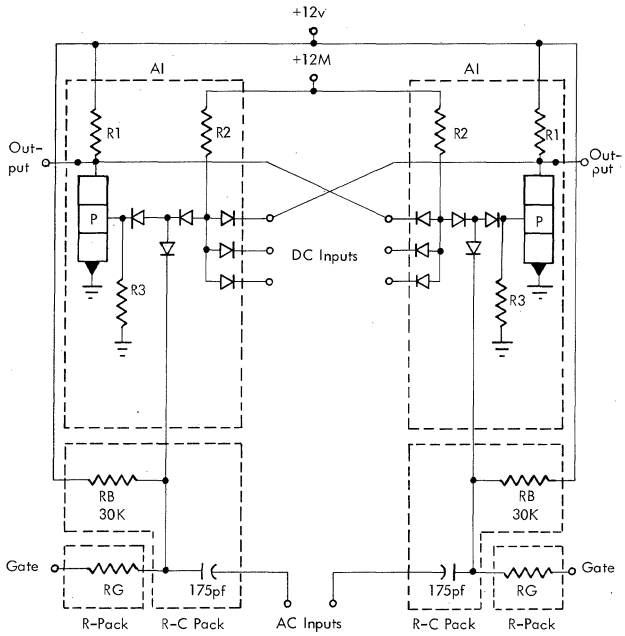

Figure 52. Flip Flop (FF)

Collector resistors of AI's must not be programmed. Two AI's, an R-C pack, and an R-pack all must be mounted on the same card.

AC Trigger (ACT)

The AC trigger (ACT) (Figure 53) consists of two AI modules, one AOX module, and a four-capacitor C-pack. Additional components may be added to increase flexibility.

The cross-coupled inverters are fed at their respective bases either from the up level of a DC set

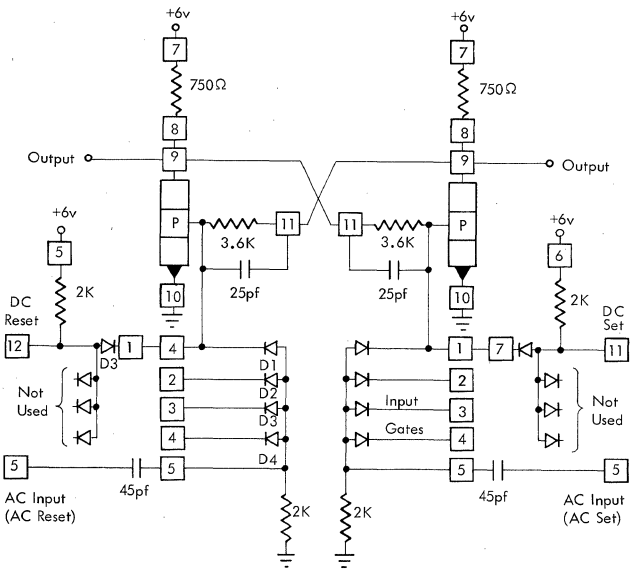

Figure 53. AC Trigger (ACT)

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pulse (at a DC set or DC reset input), or from the positive-going edge of an AC set pulse (at the AC inputs).

The current from an AC set pulse is directed either into the base of a transistor in the cross-coupled latch or is by-passed through a gate diode determined by the voltage at the cathode of this diode. If the cathodes of the three gate diodes associated with a common AC input are at an "up level" (+3 volts), current from the AC input starts trigger switching by turning the transistor, connected to this gate network, from off to on. If the cathode of any gate diode is tied to a saturated collector (0.3v), the AC input current for the gate is sent to the gate diode through the saturated collector to ground, preventing trigger switching.

The DC set inputs (11) and (12) can be driven from any 30 ns logic block. It is impossible to program collector resistors as in other 30 ns circuits. Maximum fan-in on each side of the trigger is:

AC inputs	2
Input Gates available for use with each AC input	3
DC input	1

Singleshot and Oscillator Circuits

Singleshot (SSA)

The SSA (Figure 54) uses one half of a II module, one half of a DCI module, one half of an FDD module, a trim pot, and a timing capacitor. The II module provides a transistor and two resistors; the DCI module gives powering at the output of the singleshot. The output pulse is controlled by the 10K trim pot and the timing capacitor. For a given timing capacitor, the range of the output pulse width is fixed. A continuous variation is obtained by the trim pot.

The SSA serves the same function as a delay-line singleshot, but in addition, it gives longer and continuously variable pulse widths. The input to the SSA must be a down-going pulse of width 30 ns or larger. On triggering, the output level drops from +3v to about +0.3v and stays at this level for the preset duration before returning to the +3v level again. Before the next trigger pulse is received a minimum time must be allowed for the timing capcitor to charge through R1, or a trigger pulse received during the recharging period of the capacitor will result in an output pulse of incorrect width. The collector of T1 may be inhibited with the collector of another logic block in the DOT OR configuration.

Singleshot (SSL)

Variable Singleshot: The singleshot (Figure 55) consists of one AOX$_1$ module, one II module, one trim pot and one capacitor. D2, D3, D4 are AND fan-in's. The fan-in can be extended by using FDD or AOX modules.

An up-going pulse triggers the singleshot. It has two complementary outputs with output 2 in phase with the input. The output pulse width is controlled by the

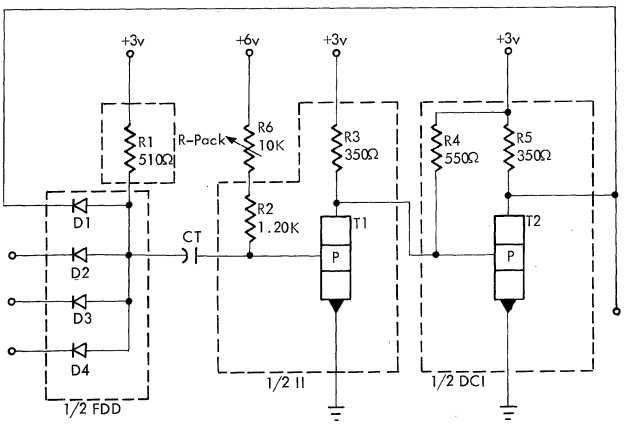


Figure 54. Singleshot, Medium-Speed (SSA)

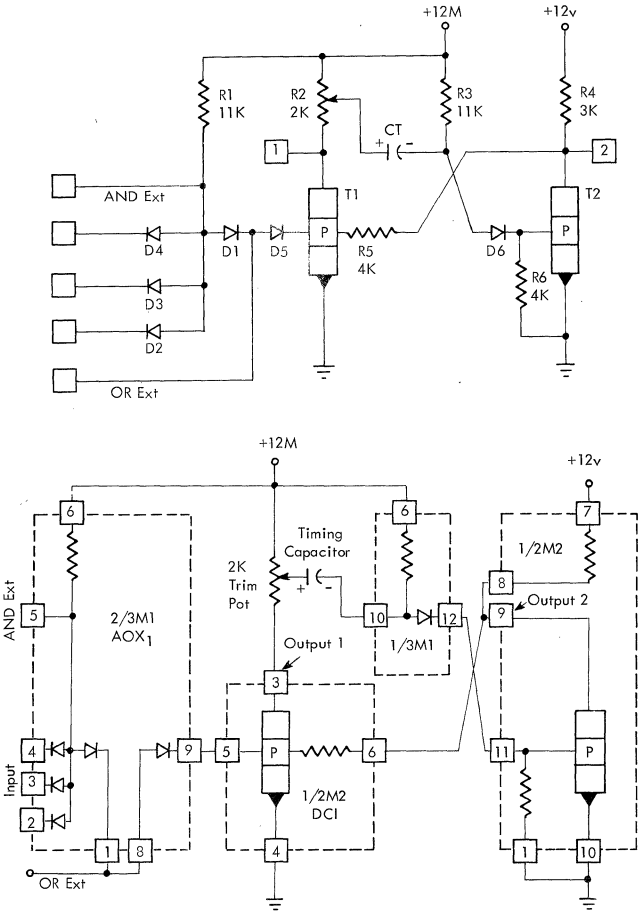


Figure 55. Singleshot, Low-Speed (SSL)

2K trim pot and the timing capacitor. For a given timing capacitor the range of the output pulse width is fixed (Figure 68). A continuous variation can be obtained by adjusting the trim pot.

Capacitor	Output Pulse Width
0.00068 uf	0.99 - 5.1 us
0.0018 uf	3.4 - 13.5 us
0.0047 uf	9 - 35 us
0.012 uf	23 - 90 us
0.033 uf	62 - 248 us
0.082 uf	153 - 615 us
0.22 uf	410 - 1,650 us
0.56 uf	1.1 - 4.2 ms
1.5 uf	2.8 - 11 ms
3.9 uf	7.3 - 29 ms
10 uf	19 - 75 ms
27 uf	50 - 200 ms

Figure 56. SSL Timing Capacitors

Between the end of the output pulse and the start of next trigger, a minimum time (recovery time is equal to or greater than the desired output pulse width) must be allowed for the timing capacitor to be fully charged, or a "premature" triggering will result in an incorrect output pulse width.

NOTE: Output 1 is a negative-going pulse and output 2 is a positive-going pulse. The singleshot cannot drive a DCI or II. Output 1 cannot be used if the input pulse width is longer than the desired output pulse width.

Fixed Singleshot: An R-C module combines with one AOX_1 module and one II module to form a singleshot with fixed pulse width of 2.8 μs or 5.6μs $\pm$30 percent. The module contains two resistors and one capacitor. The interconnections between modules remain as in the preceding description except that an R-C module replaces the 2K trim pot and the timing capacitor.

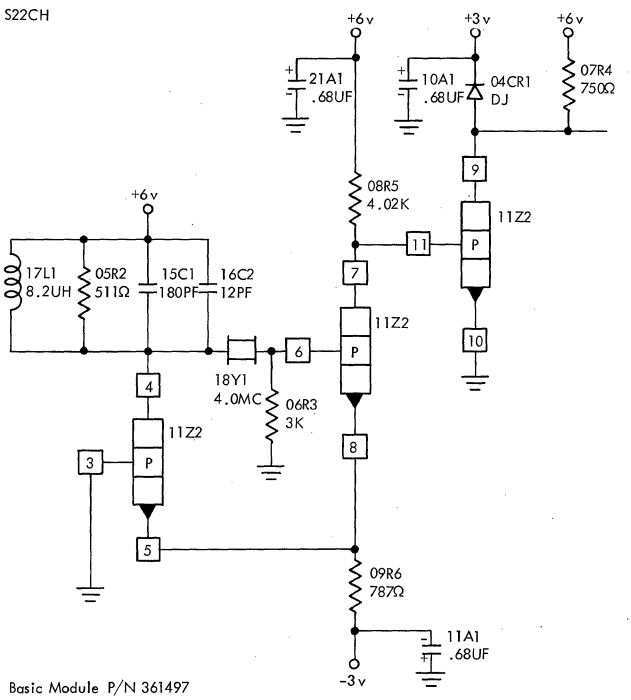
Oscillator

The free-running crystal oscillator (Figure 57) serves as a pulse generator. The oscillator produces pulses or voltage variations of a definite frequency, e.g., 4.0 mc. The circuit consists of a basic switching circuit whose output is determined by the quartz crystal. The crystal vibrates at 4.0 mc and develops a sinusoidal voltage that is amplified and clipped to produce the square wave output of the oscillator. The inductively tuned tank circuit provides regenerative feedback to sustain the crystal oscillations.

Inverter Circuits

Isolating Inverter

The II module (Figure 58) consists of two isolating inverters. This is one way of connecting direct coupled inverters with the advantage of allowing the driver to have full fan-out like the II. However, because of the current-limiting resistor in the base, the II fan-out capability is only seven AI/AOI, or equivalent, loads.



•Figure 57. Crystal Oscillator

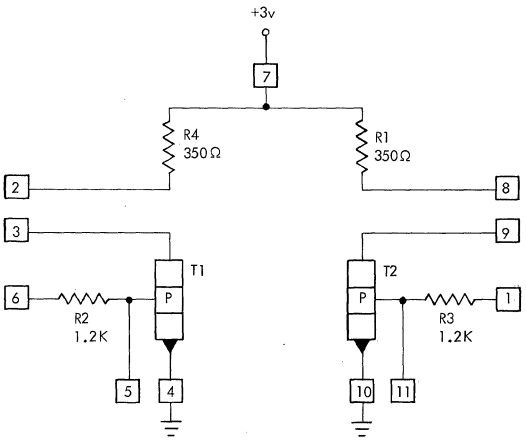


Figure 58. Isolating Inverter, Medium-Speed (II)

Pins 1 and 6 are the input, and 2, 3, and 8, 9 the output pins. Pins 2, 3 and 8, 9 are connected on the card for most applications. When the collectors are dotted, only one collector load register is connected to retain the specified fan-out capability.

Direct Coupled Inverter (DCI)

The DCI module (Figure 59) contains two separate direct coupled inverters. These inverters are designed to provide a fast, economical way of extending the

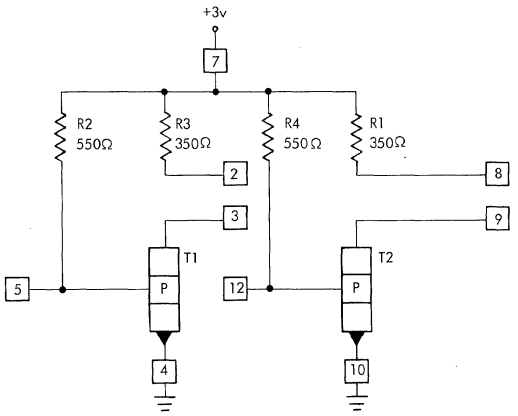


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Figure 59. Direct Coupled Inverter, Medium-Speed (DCI)

fan-out of an AI or AOI module approximately three times. The lead between the AI or AOI output pin 9 and the DCI input pin 5 or 12 must be kept as short as possible to realize the speed capability of this circuit.

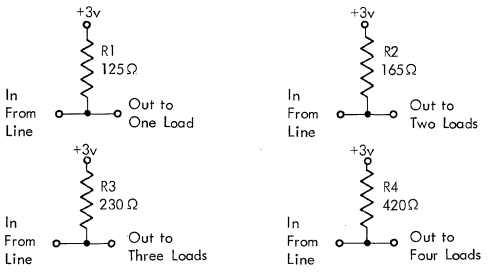
The collector resistor must be connected on the driving AI or AOI to provide the necessary base current drive to the DCI. The DCI collector resistor has been left programmable but must be connected on the card for the intended use of this module. Connect pin 2 to 3 and 8 to 9.

The circuit will not drive long transmission lines because of fast output transitions, unless the lines are terminated.

Transmission Line Circuits

Line Terminator Circuits (AOI_{10} Circuit Family)

The line terminating network (LTN) circuit (Figure 60) consists of a single terminating resistor (four different values: 125, 165, 230, or 420 ohms, depending upon the load) connected at the end of the line and returned to +3 volts. The resistors are discrete components placed immediately at the end of the line with one to four AOI_{10} circuits. Essentially, the LTN allows the line to be terminated in a logic block without the insertion of an active buffering circuit.



R1, R2, R3, R4 are on RC Modules

•Figure 60. Line Terminating Network (LTN)

The line sensing amplifier (LSA) line termination consists of a resistor network at the end of the line and one to ten LSA circuits placed at the end of the line or distributed along the line. Each LSA may drive only one AOI_{10} circuit.

The transmission lines are SLT printed wire, SLT flat cable, or commercial coax. All have approximately a 93-ohm characteristic impedance.

Delay Circuit (DLY)

Variable Delay Circuit: The delay circuit (Figure 61) consists of one AOX_1 module, one II module, one potentiometer, and one capacitor. It has a fan-in of one and fan-out of five AI's. The circuit functions as an inverter with worst case turn-off delay of 520 ns and variable turn-on delay, ranging from 1.9 μs to 220 ms, controlled by the 2K potentiometer and the timing capacitor. For a given timing capacitor, the range of the turn-on delay is fixed (Figure 62). A continuous variation can be obtained by adjusting the potentiometer. After the circuit is turned off, a minimum time must be allowed for the timing capacitor to charge up fully before it can be turned on. Otherwise, incorrect turn-on delay will result.

Fixed Delay Circuit: An R-C module combines with one AOX_1 module and one II module to form a delay circuit with a fixed turn-on delay of 2.8 μs or 5.6 μs ±30 percent.

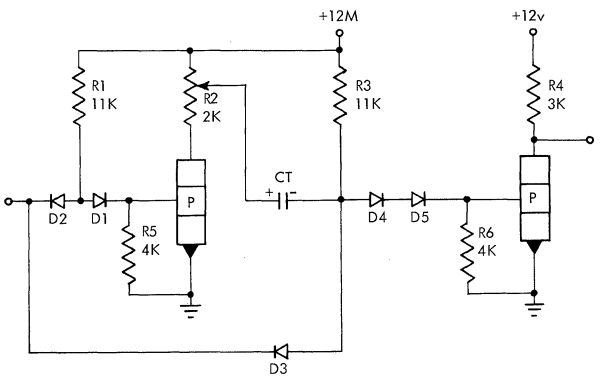


Figure 61. Delay Circuit (DLY)

Capacitor		Turn-On Delay			
0.00068	uf	1.4	-	5.5	usec
0.0018	uf	4.5	-	14.6	usec
0.0047	uf	12	-	38	usec
0.012	uf	30	-	97	usec
0.033	uf	83	-	260	usec
0.082	uf	205	-	660	usec
0.22	uf	550	-	1,780	usec
0.56	uf	1.4	-	4.5	ms
1.5	uf	3.7	-	12	ms
3.9	uf	9.7	-	31	ms
10	uf	25	-	81	ms
27	uf	67	-	220	ms

•Figure 62. Timing Capacitors (DLY)

The module contains two resistors and one capacitor. The interconnections between modules remain as shown except that an R-C module replaces the 2K trim pot and the timing capacitor.

Line Sensing Amplifier (LSA)

When it is necessary to tap a transmission line at two or more locations, the tapped connections must present a high impedance to the transmission line to prevent reflections. The LSA (Figure 63) is the medium and high-speed circuit used for this purpose.

The terminating resistor (RT) is external to the module. (RT is connected only on the LSA at the receiving end of the transmission line. There can be only one RT connection per transmission line. It is always located at the receiving end of the transmission line.)

In Figure 63 resistor R4 is used to obtain emitter follower stability. Transistor T2 does not saturate. Therefore, the LSA presents an impedance of approximately h_{FE} (static forward current transfer ratio) times R4 to the transmission line. In the selection of R4, the following must be considered:

1. h_{FE}R4 must be >> the characteristic impedance of the line.
2. The voltage drop across R4 (when the input to the LSA is down), because of the worst case off diode current from the connecting AI logic block, cannot exceed 0.495v for an AI and 1.01v for an AOI.

When the input signal of the LSA is up, T2 conducts with an emitter-base voltage drop of approximately 0.6 to 0.7v. At this time, the input diode of the connecting logic block is back biased so that the LSA presents a minimum impedance of 6000 ohms to the transmission line. When the input to the LSA is down, T2 is turned off. Thus, the LSA presents an infinite impedance to the transmission line.

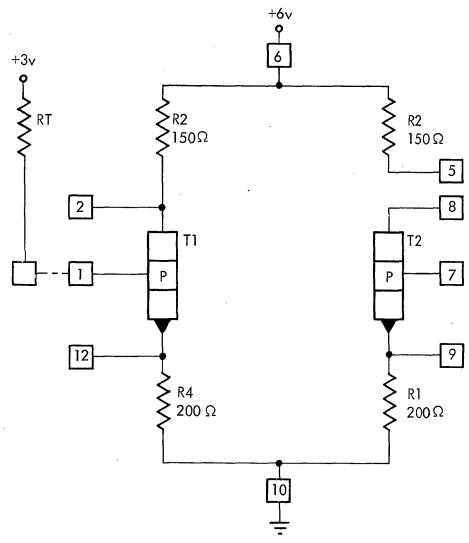
With T2 off, the diode current from the driven logic block flows into R4. The voltage level, developed by this diode's current into R4, cannot exceed 0.495v for an AI and 1.01v for an AOI. As the LSA's input begins to rise, the voltage level at the emitter of the LSA does not change until the base of the LSA becomes 0.6 to 0.7v, more positive than the emitter. This V_{eb} drop is maintained as the base's input voltage continues to rise. The driven block does not turn on until the emitter of the LSA has passed the 0.7v level. When the LSA's input is up and begins to fall, the driven block does not turn off until the emitter of the LSA is at the level of 0.912 volts for the AI and 1.652 volts for the AOI. The pulse widths at the emitter of the LSA must be at least 40 ns in order to obtain unity gain. All other diode inputs of the driven block may be used in their normal manner.

Transmission Line Receiver (TLR)

The transmission line receiver (TLR) (Figure 64) is used with the interface driver. Up to eight receivers and eight drivers may be placed on any one transmission line.

The circuit operates as follows: the input transistor (isolating transistor), T1, is heavily saturated. T2, a current amplifying transistor, is on regardless of the input line level. When the input is up, T3, another current amplifying transistor, is on, and the output from T3 is down. When the input is down, T3 is cut off, and the output from the TLR is up. When the power is turned off on the TLR, it presents a high input im-

TLR



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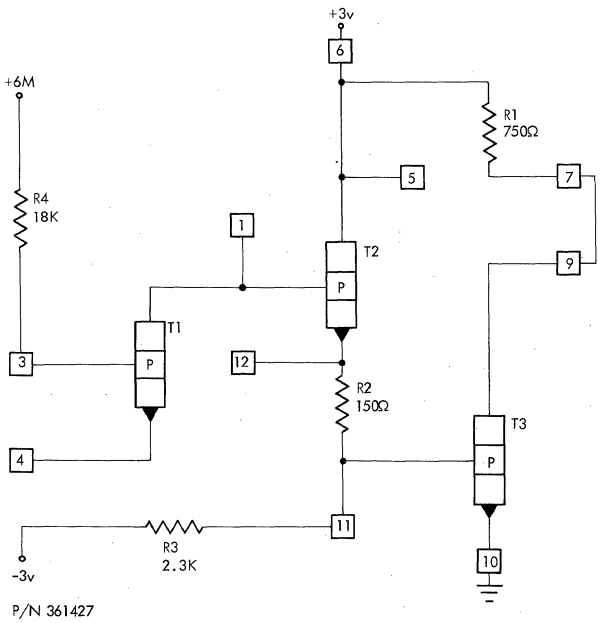
•Figure 63. Line Sensing Amplifier (LSA)



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•Figure 64. Transmission Line Receiver (TLR)

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pedance which will not load down the driver; the other drivers and TLR's on the transmission line operate normally.

Delay Line, Driver and Terminator (DLD)

The DLD (Figure 65) consists of an API driver, a programmable delay line, a line terminating network (LTN), and an AOI output stage. It yields an output transition pulse which is the same as the input transition pulse delayed in time.

The API line driver accepts the LTN current plus the AOI drive current, a total of 29 ma. The API collector resistor is not used.

The programmable delay lines offer delays of 5-500 ns maximum in 5 ns increments, or four separate 5-125 ns maximum delay lines used individually. The LTN with the ON input impedance of the AOI matches the characteristic impedance of the delay line (93 ohms). The AOI with the LTN acts as a terminator and as an output stage.

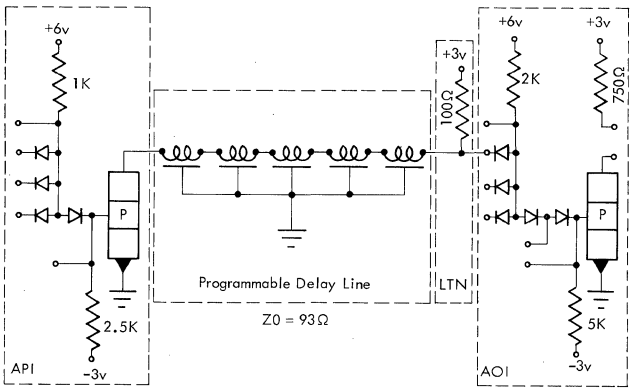

Figure 65. Delay Line Driver and Terminator (DLD)

Direct Coupled Inverter (DCI) and Transmission Line Driver (TLD)

The DCI module (Figure 66) contains two separate direct coupled inverters. The inverters are designed to provide a fast, economical way of extending the fan-out of an AI or AOI module approximately four times.

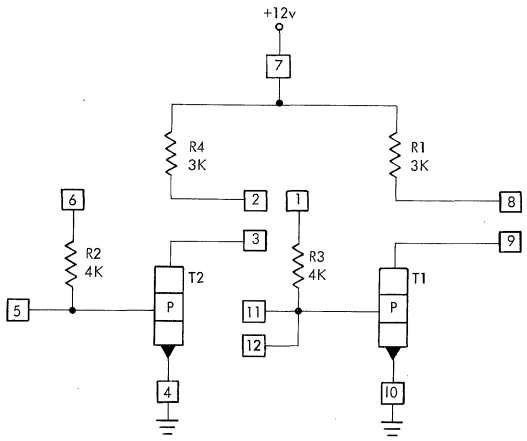

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Figure 66. Direct Coupled Inverter, Low-Speed (DCI)

A DCI stage, when driven by API/AOPI, serves as a 56 ma transmission line driver (TLD).

The collector resistor must be connected on the driver to provide the necessary DCI or TLD base current.

The collector load resistor of the DCI/TLD is programmable. For most applications module pins 2 and 3 or 8 and 9 are connected on the card.

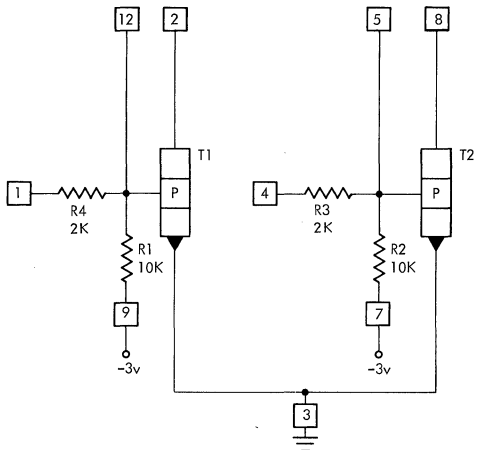
NOTE: Except for external connectives, this module is identical to II (isolating inverter).

Indicator Driver Circuits

Indicator Driver (ID)

The indicator shows evidence of the output state of the driving circuit. For the up-level indicator, lamp L1 is on only when the driving circuit is at an up level. For the down-level indicator, lamp L2 is on only when the driving circuit is at a down level.

Because of the high (2K) input impedance, neither circuit loads down the driver (Figure 67) when it is used singularly. As a general rule, no two indicators will be driven from the same driver. However, the driver may drive the regular AND logic blocks plus an ID.



P/N 361480

•Figure 67. Indicator Driver, High-Speed (ID)

40 ma Switch (Indicator Driver) (ID_2)

The 40-ma switch (Figure 68) is a driver capable of accepting 40 ma at its output. It is used in slow-speed applications such as an indicator driver.

The ID_2 may be driven by high-, medium-, or low-speed circuits. Its driver may drive the regular AND blocks and the ID_2 block. It can not be driven from an LSA.

Indicator Driver (IDL)

An II stage (a saturating transistor) (Figure 69) serves as a driver for both the up- and down-level indicators (bulbs).

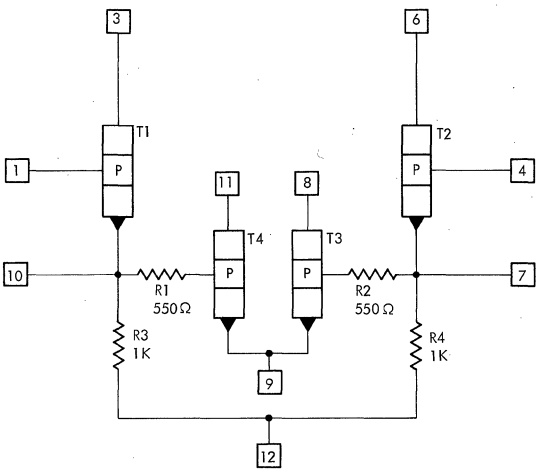


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Figure 68. Indicator Driver, 40 ma (ID)

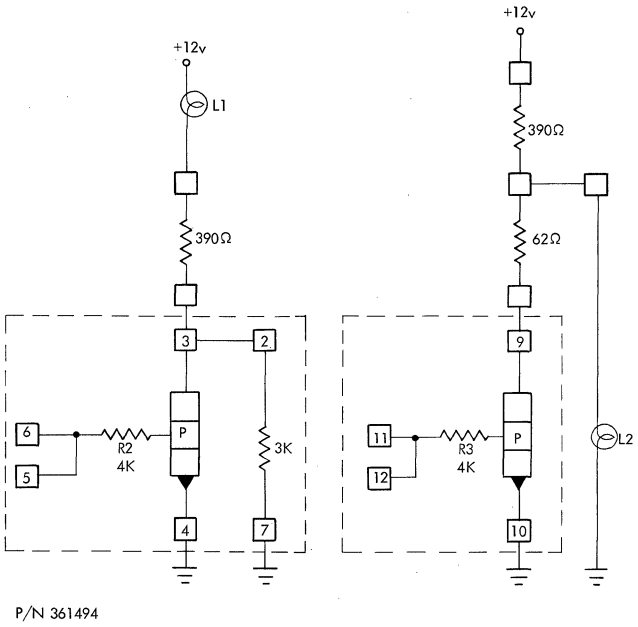

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Figure 69. Indicator Driver (IDL)

The bulb, when lit, indicates the state of the input level. The up-level indicator requires a 1, and the down-level indicator a 0 at the input to turn the light on.

Because of the high input impedance of the II, the driver can drive its full load plus the indicator driver (ID).

The indicator driver, besides driving either of the indicators, can drive also an API/AOPI load for latch-back (transient noise indication).

Using one II/DCI module, two R-packs, and two bulbs, these combinations are possible:

1. Two up-level indicators
2. Two down-level indicators
3. One up- and one down-level indicator.

Special Conditions

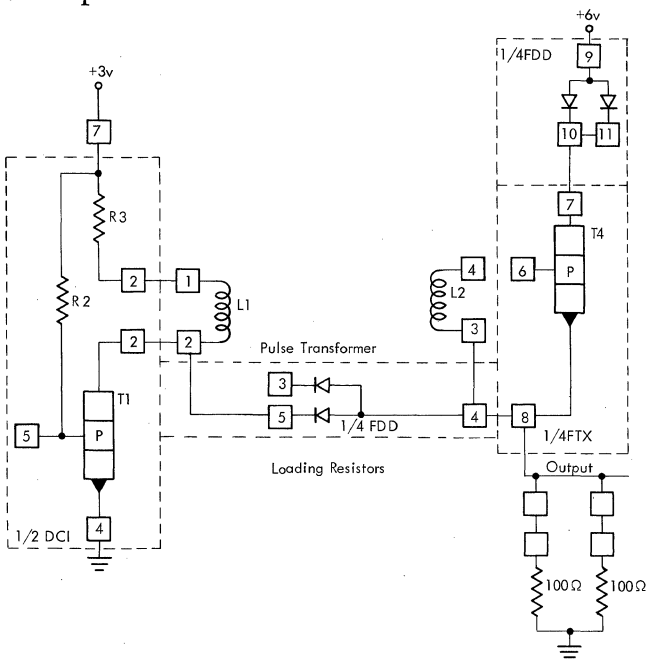
1. The indicator driver(s) must not be used as a link in a logic chain.
2. The indicator driver(s) cannot drive an II or DCI.
3. The indicator driver(s) can drive, besides the bulb and its network, an additional AI/AOI or API/AOPI load only for latch-back purposes.

Driver Circuits

Sample Pulse Driver (SPD)

The SPD (Figure 70) consists of one half of a DCI, one half of an FDD, one quarter of an FTX, and a pulse transformer. The input to the SPD can be an AI, AOI, or API minus the collector resistor. When the input is at the up level, T1 is turned on and current is built up in the primary inductance L1 with a time constant of L1/R1. During the time that T1 is on, T2 remains off. When the input is at the down-level, T1 switches off. The current in the primary inductance falls at a rate of di_1/dt, which turns on T2 by the mutual coupling in the transformer. When T2 is turned on, a large current is delivered to the load.

The diodes at the collector of T2 limit the voltage swing, while the diodes between the collector of T1 and the emitter of T2 are used for the off current from the AC inputs. The SPD must drive at least 16 AC inputs on two separate lines of no more than 10 inches each when the output of the SPD has no load resistor. When only two AC inputs are used, the output of the SPD must be terminated with a 50-ohm resistor. The SPD can drive 20 AC inputs when the output is not terminated. The output of the SPD is an emitter follower, and the impedance reflected back to the emitter decreases



•Figure 70. Sample Pulse Driver, Medium-Speed (SPD)

as the number of AC inputs increases. The current available to the load increases when the emitter follower recognizes the low impedance load. Therefore, the output of the SPD can be readily loaded by a 100-ohm or 50-ohm resistor depending on the fan-out.

High Power Driver (HPD)

The HPD (Figure 71) is a high current driver made by connecting the two inverters in parallel on a specially selected DCI module. The HPD can be driven by an AI or an AOI if the collector resistor on the driving block is returned to +6v. The HPD will be mounted in the adjacent module position.

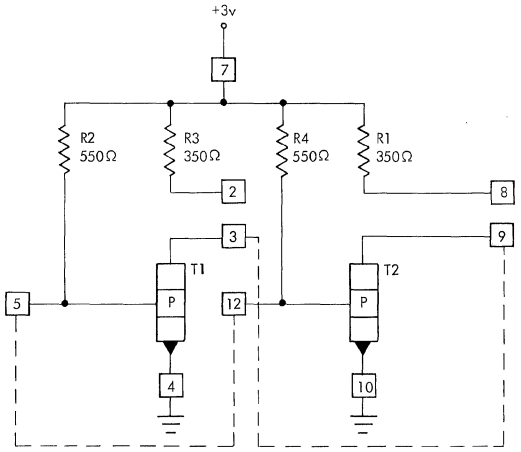


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Figure 71. High Power Driver (HPD)

The API−3v will also drive the HPD with normal power supplies.

The HPD may be used to drive a large number of loads (36 AI or 28 AOI), or it may drive long transmission lines. The HPD may not be used to drive both LSA's and regular loads simultaneously. It cannot drive long lines when it is driving a high fan-out of AI, etc., because of the reflections on the unterminated transmission lines.

NOTES: 1. This is not a standard application of the DCI module. The HPD is a selected DCI that has closely matched transistors to allow paralled operation of the two inverters.

2. The collector current can become 80 ma for the most unbalanced transistor pair.

3. The HPD module may not be used as a DCI.

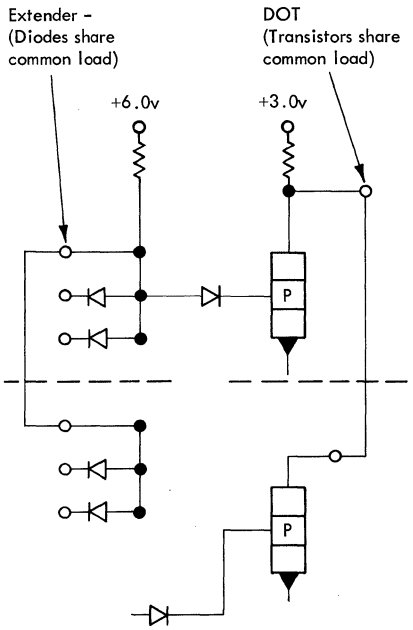
Extender and DOT Functions

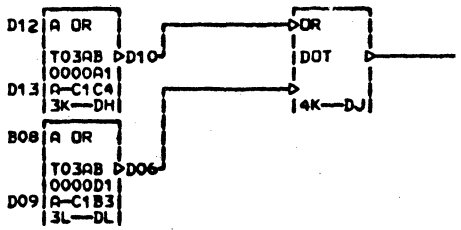
AND circuits and OR circuits may be connected together to produce a single output.

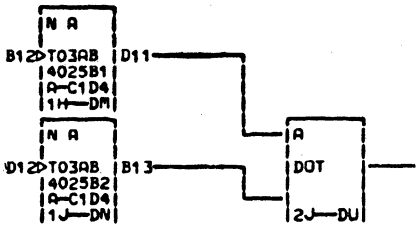
When the circuit of the AND or OR block is diode logic, one logic block is connected to the other by an extender (E). The extender is in effect a method of adding diodes to the input of a circuit. The symbol E is only used on the ALD's when the connection is made between two cards.

When the output of the AND or OR block comes from a transistor (vs. a diode), the logic blocks are connected with the DOT block (Figures 72 and 73). The DOT block is simply wiring connecting the outputs of two or more transistors.

The function of the DOT block depends upon the desired logical use of the shared transistors. Generally, the AND DOT is a +A; the OR DOT is a −OR.







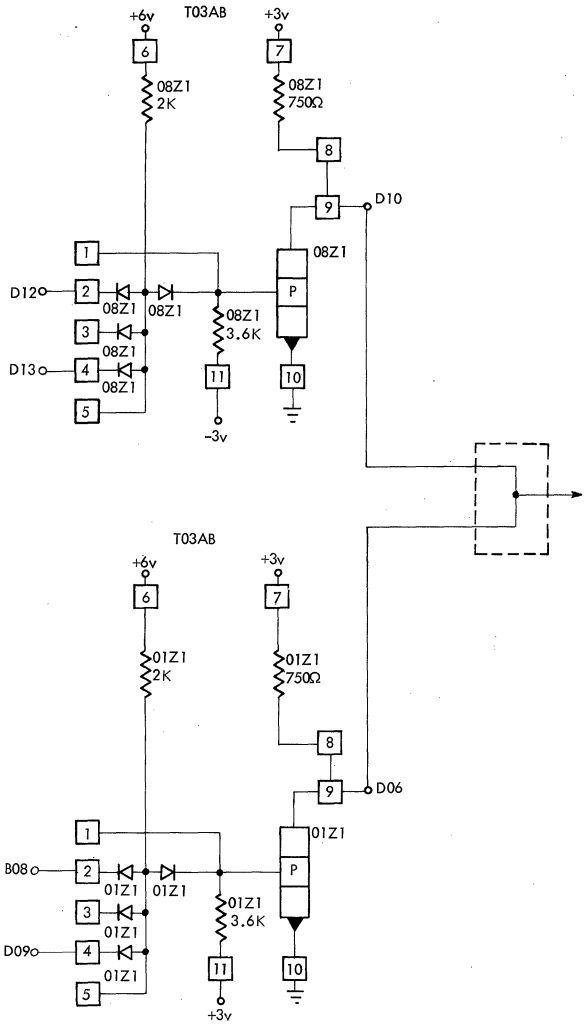


Figure 72. The OR DOT Block

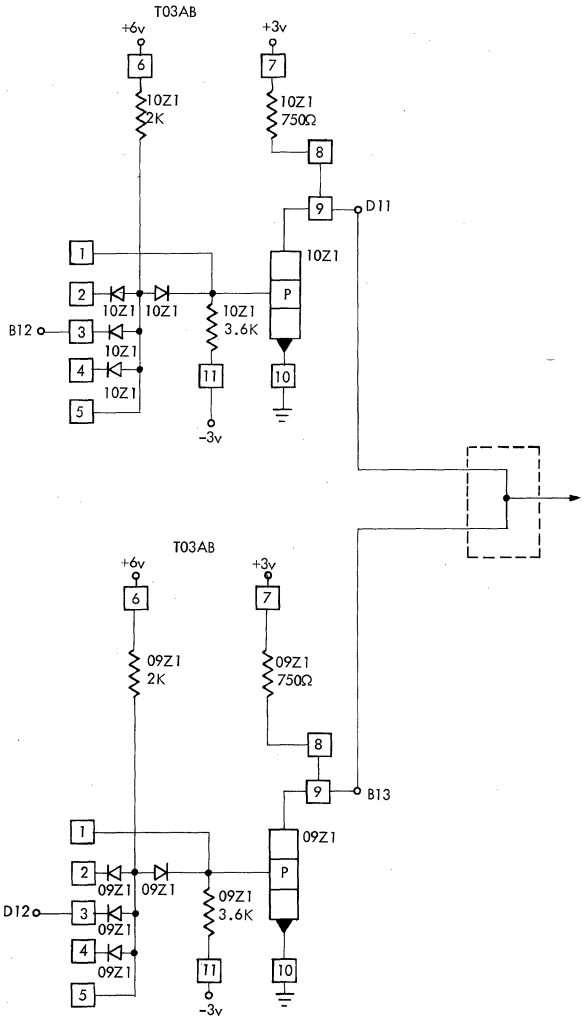


Figure 73. The AND DOT Block

- Card ALD sheet shows ALD logic blocks.
- Assembly drawing sheet shows physical placement of components on card.
- Schematic sheet shows circuit diagram of electronic components.

The card layout is defined as the card ALD sheet, the assembly drawing sheet, and the schematic sheet. These sheets (Figure 74) are a three-way representation of the actual SLT card.

There is at least one page for each type of sheet but one page only for the assembly drawing. The circuit complexity, the circuit speeds, functional versus logical card packaging, and the size of the card are some of the factors determining whether a card will have more than one page of card ALD sheets and/or schematic sheets.

Card ALD Sheet

The card ALD sheet (Figure 74, sheet 1) is similar to a regular ALD logic sheet. The part number (P/N) appears at three corners of the sheet. The part number consists of four digits and a suffix. A 580 always is understood to precede the four digits, as it is in the ALD logic block. The suffix consists of the number of the card ALD sheet. The engineering change level (EC) appears to the left of the title block.

Logic Block

The logic block is similar to the ALD logic block, except that specific machine information is left out. Line 1 gives the function of the block; an asterisk (*) is placed before the function name if the input line position is significant. Line 3 designates the circuit number. Line 4 describes the portion and subportion of the block. Line 6 indicates the block position and the serial number of the block of the card ALD. In some cases the engineering specification of the circuit is placed above the block; for example, the OR block at location 2B of Figure 74, sheet 1, is labeled 890972. The pin numbers of the card, if they exist for the block, are placed on the input and output lines of the logic block.

As in regular ALD logic blocks, wedges (◺) denote the line levels to satisfy the function of the block.

Card Characterization

The lower left-hand corner contains information concerning the card size, the voltage pins, and the card characterization code. Five card sizes are in general use: 1-6, 1-12, 2-6, 2-24, and 2-36, where the first digit (1 or 2) designates the number of the socket the card fits into, and the next digit or digits (6, 12, 24, or 36) designate the number of standard module positions on the card.

The voltage pin information indicates where and what actual voltages are present on the card.

The card characterization code tells the general voltage and the logical use of the card. The code has a voltage code (T, V, U, S, L, or O) and a use code, which consists of the number portion of the circuit number. See Figure 8 for the use code interpretation.

The voltage codes are:

T requires a +3, −3v, or +6v power supply or any combination.
V requires *only* a +12v power supply.
U requires a +3, −3v, or +6v power supply or any combination and specifically associated with the 5 ns family.
S requires either a combination of the voltages listed for U or may be used in category.
L are the SMS circuits associated with the SMALL family.
O are the nondigital circuits associated with analog families.

For example, T03 (Figure 74, sheet 1) means the card uses a combination of +3v, −3v, or +6v (T) and has logic circuits (03).

Input Lines

Input lines are identified in two ways: (1) by the pin number of the card, and (2) by a net number. An example of a pin number of a card is D05.

The net number may be a number assigned by design automation, such as 001 or 002. On the other hand, it may be a net number of the type used when there are multiple card ALD sheets; the number 41681AB4, for example, means the line originates from the block located on part number 5804168, page 1, with serial number AB, fourth line.

Output Lines

Output lines are identified by the source block and line origin and by a net number. The source block and line origin (example: AA5) is the same as that shown on the ALD page.

The net number is either the card pin number or a combination of the card pin number and the page number to which the line goes. An example of the card pin number is J10. If the line goes to page 41682, the combination is 41682J10.

Assembly Drawing

The assembly drawing sheet (Figure 74, sheet 2) contains two parts: (1) on the left portion of the page, a graphic representation of the components on the card and (2) on the right side of the page, a chart listing the part numbers.

This sheet has the part number in the upper right and lower left corners, a title block in the lower right corner, the EC record in the upper right portion of the sheet, and a chart of the voltages and their respective pins near the part number chart.

The part number chart (Figure 74, sheet 2) consists of a listing of the component parts used on the card. Each different component is listed with part number, description or value, quantity used on the card, and a code that is used on the schematic sheet and the assembly drawing sheet. The module code is A for an RC module and Z for an SLT module.

The graphic representation numbers each component, modular and discrete, from top to bottom and from right to left.

Schematic Sheet

The schematic sheet (Figure 74, sheet 3) has the schematic of the circuits, along with the card part number, a regular title block, and an EC block. The schematic has the actual components (such as resistors, transistors, diodes, and capacitors) of the ALD logic block (by circuit numbers). The components are keyed to the assembly drawing by a location code.

Each ALD logic block in the ALD's reference an SLT card by part number. Each particular ALD logic block has card pin numbers and a circuit number. The same ALD block is found on the card ALD sheet of the card layout and also on the schematic sheet with the same card pin numbers and circuit number.

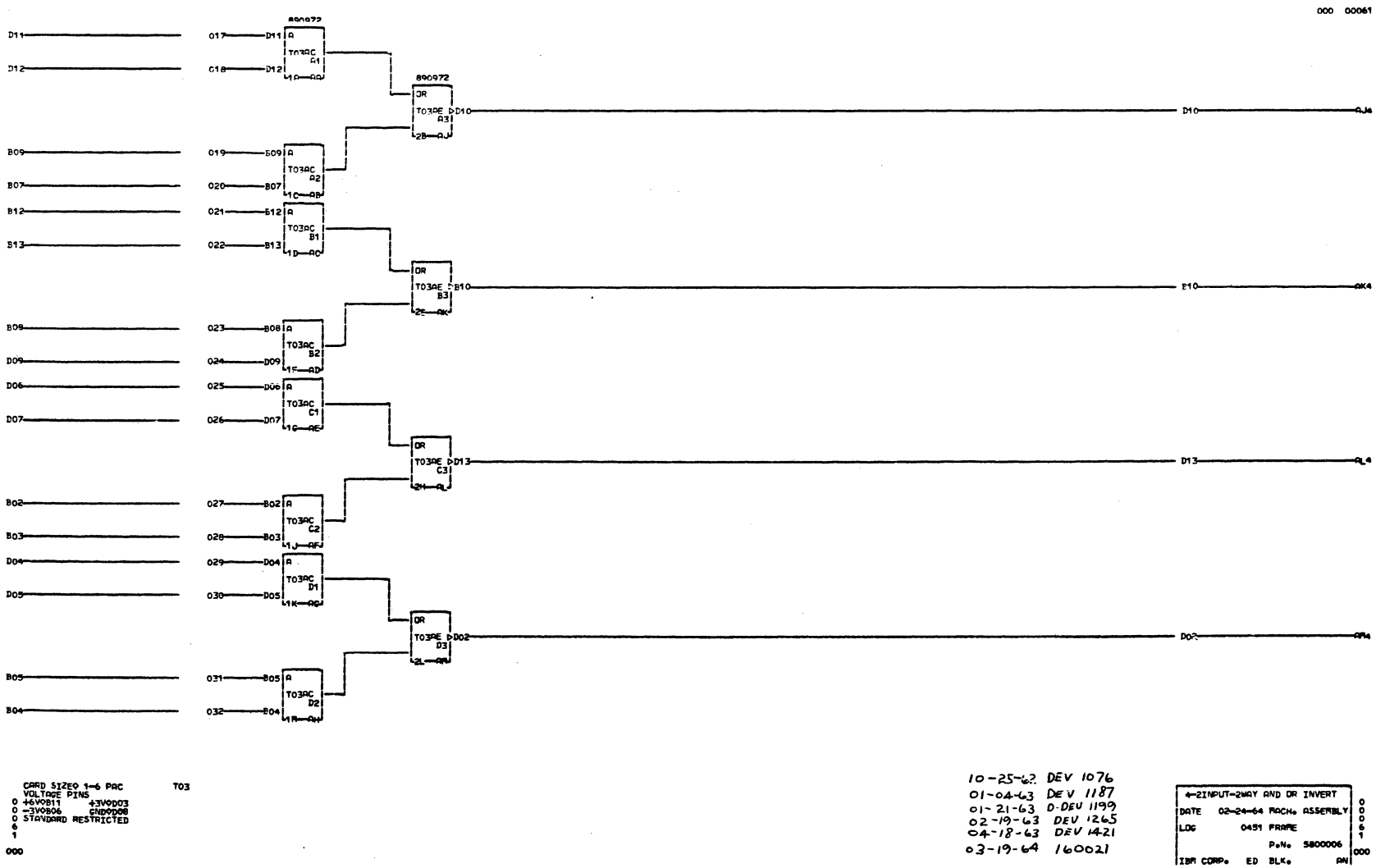
The circuit number on the schematic sheet identifies its components. The identification of each component is its physical location on the card as shown on the assembly drawing sheet, Figure 74, sheet 2.

The complexity of the card may require more than one sheet of schematics. Sometimes each sheet (Figure 74) is complete as far as the individual circuits are concerned, that is, there are no electrical connections between circuits on the card. However, if the circuits are electrically connected, the schematic is interconnected on more than one sheet.

A Particular Example

Let us examine a particular logic line by using Figure 74. The logic line labeled D11 is the top line of sheet 1. This line has a net number, assigned by design automation, of 017. This line enters the card on card pin D11. This line in its more positive condition will condition one leg of the AND circuit T03AC. Sheet 3 shows that the logic line entering the card at D11 is connected to pin 3 of a module. Numbers with squares around them (□) refer to pins of a module. Pin 3 of the module is connected to the cathode of the diode labeled 5Z1. The diode 5Z1 is one of two legs of the circuit T03AC. Circuits are usually labeled with their circuits numbers on the schematic sheet.

The part number chart on sheet 2 shows that the Z1 is part number 361453. The complete schematic of this module may be found in the last section of this manual. The 5 of the 5Z1 designation of the diode locates the module as the fifth component on the card when counting top to bottom and right to left. Looking at the chart, we find module 5Z1 located in the upper left part of the card.



•Figure 74. Regular Card Layout (Sheet 1 of 3)

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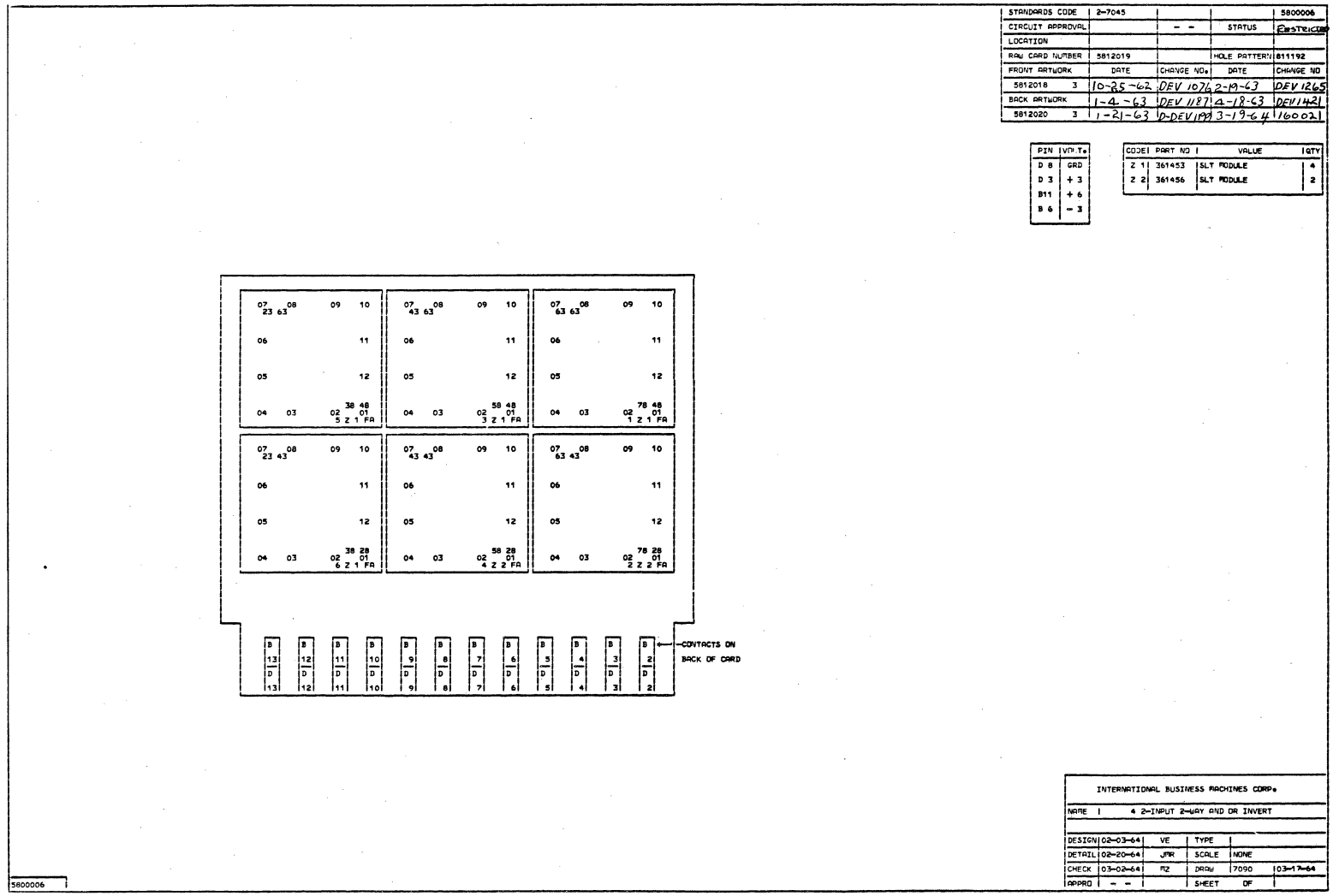

Figure 74. Regular Card Layout (Sheet 2 of 3)

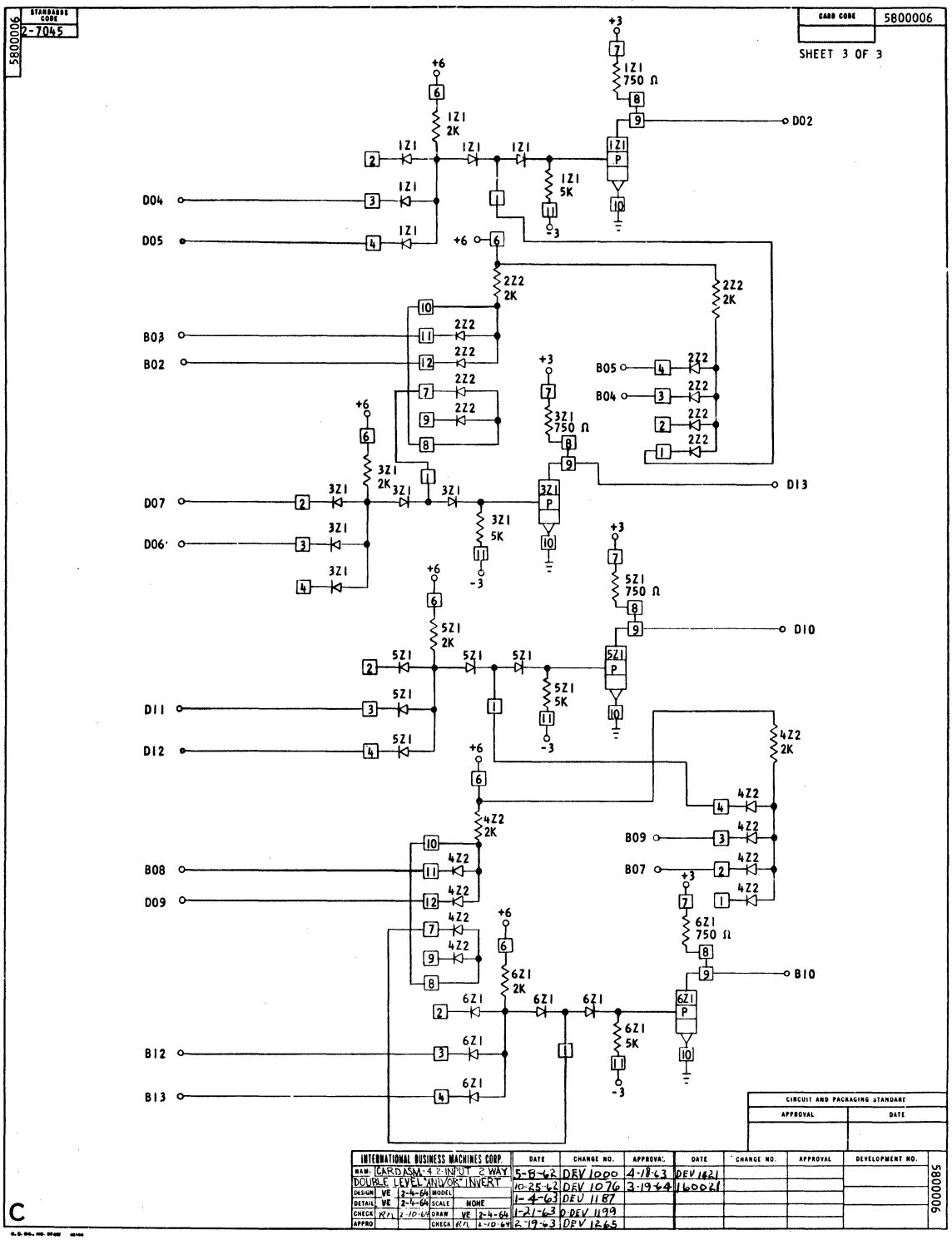

Figure 74. Regular Card Layout (Sheet 3 of 3)

Circuit Numbers

Circuit numbers are the common denominator between ALD's and the card layout. The understanding of circuit numbers is one step in the understanding of a particular system or unit.

All circuit numbers used in systems or units are listed in the "Appendix." Figure 75 is a sample of the list. The first column of the listing is the circuit number; the second column is a word description of that particular circuit number. In the item "T03AJ AND-PWR INVERT 300 OHM LOAD" for example:

T means the circuit speed is in the 30 ns range;
03 means that it is a logical circuit;
AJ is the unique circuit;
AND-PWR INVERT 300 OHM LOAD means the circuit is an API with the 300 ohm load resistor connected.

Figures 76 to 114 are representative examples of circuit numbers as actually used on the card layout. The ALD block is also shown. Note that module pin numbers and connections within the card are shown in a square with the number within. Card pin numbers are shown as a circle with the card pin number adjacent.

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LOGIC GENERAL FORM - XYYZZ

X DEFINED

S - SRETL GENERAL
T - 30 NS
U - 5-10 NS
V - 700 NS
O - ANALOG

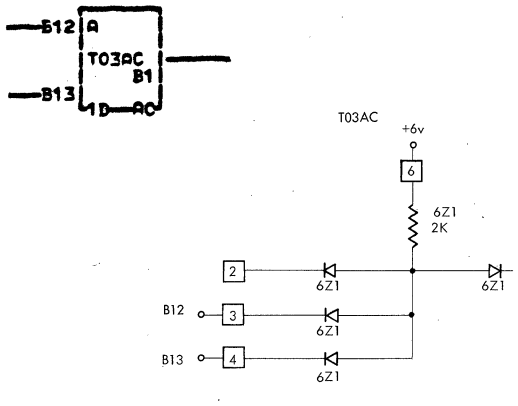
YY DEFINED

3 - LOGIC BLOCKS.
5 - VOLTAGE TRANSLATE CIRCUITS
6 - TRANSMISSION LINE DRIVERS AND RECEIVERS
7 - SENSE AMPLIFIERS
10 - INVERTING DRIVERS LESS THAN 50 MA
11 - NON-INVERT DRIVER LESS THAN 50 MA
15 - POWER DRIVER MORE THAN 50 MA
16 - MAGNETIC HEAD AND CORE DRIVER
20 - TRIGGERS
21 - SINGLESHOTS
22 - OSCILLATORS
25 - REGULATORS, CLAMPS, CLIPPERS, AND LIMITERS
32 - GATES
40 - SPECIALS
45 - DELAY CIRCUITS
55 - INDICATOR CIRCUITS
60 - INTEGRATORS AND FILTERS
61 - COMPONENTS
63 - REED RELAYS
65 - FUNCTIONAL CARD
66 - FIELD REPLACEMENT CARD

ZZ DEFINED - THE UNIQUE CIRCUIT

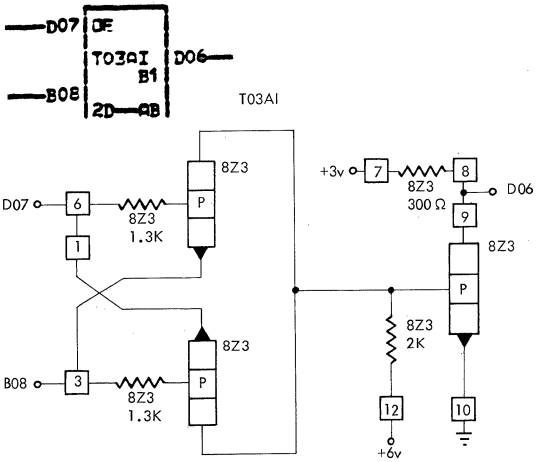
CIRCUIT NUMBER	TITLE	CIRCUIT NUMBER	TITLE
T03AJ	AND-PWR INVERT 300 OHM LOAD	T05AL	TRANSLATE BLOCK
T03AK	EXCLUSIVE OR LATCH	T05AM	WRITE DRIVER CHECK
T03AL	8 WAY EXCLUSIVE OR	T05AO	45 MA TRANSMISSION LINE DRIVER
T03AM	4 WAY EXCLUSIVE OR	T05AP	INTERLOCK CIRCUIT TERMINATOR
T03AN	7 WAY API-NO LOAD	T05AQ	INVERTER

•Figure 75. An Example of the Circuit Number Listing



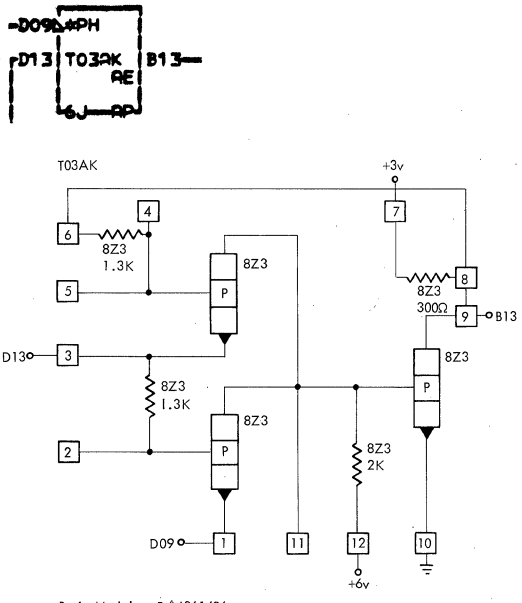
Basic Module may be P/N 361453, 361455, 361456, 361459

Figure 76. T03AC, AND



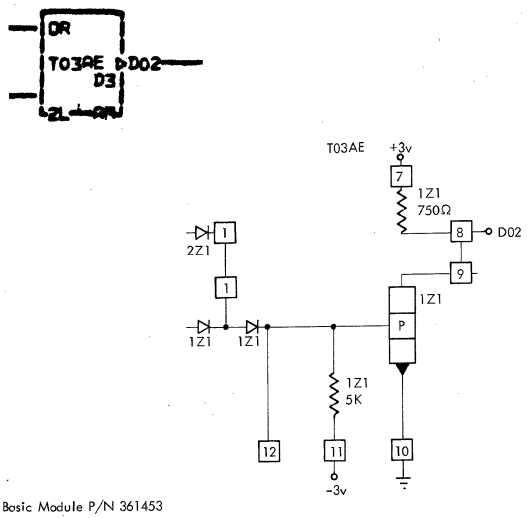
Basic Module - P/N 361477

Figure 78. T03AI, Exclusive OR



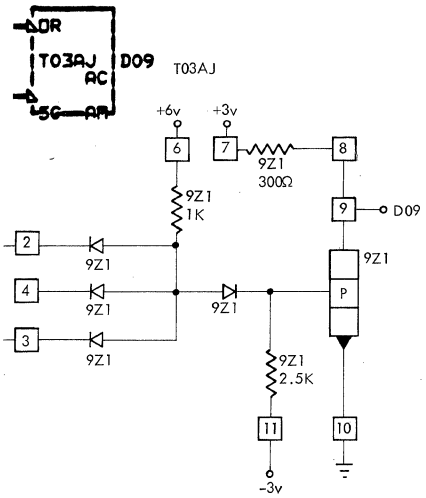
Basic Module - P/N361486

Figure 80. T03AK, Exclusive OR Latch



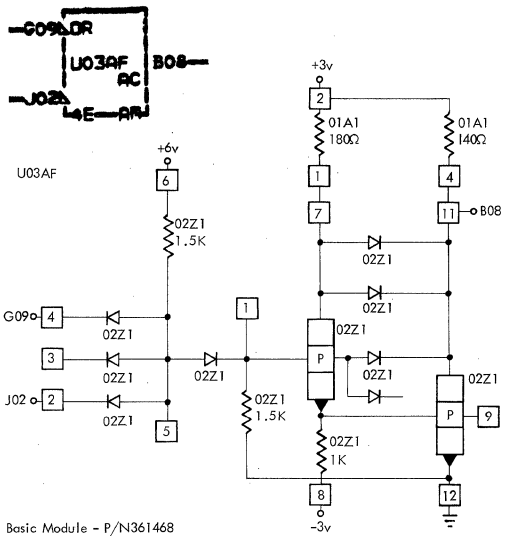
Basic Module P/N 361453

Figure 77. T03AE, OR-Inverter Loaded



Basic Module - P/N361473

Figure 79. T03AJ, AND-Power-Inverter Loaded



Basic Module - P/N361468

Figure 81. U03AF, AND-Inverter with Load

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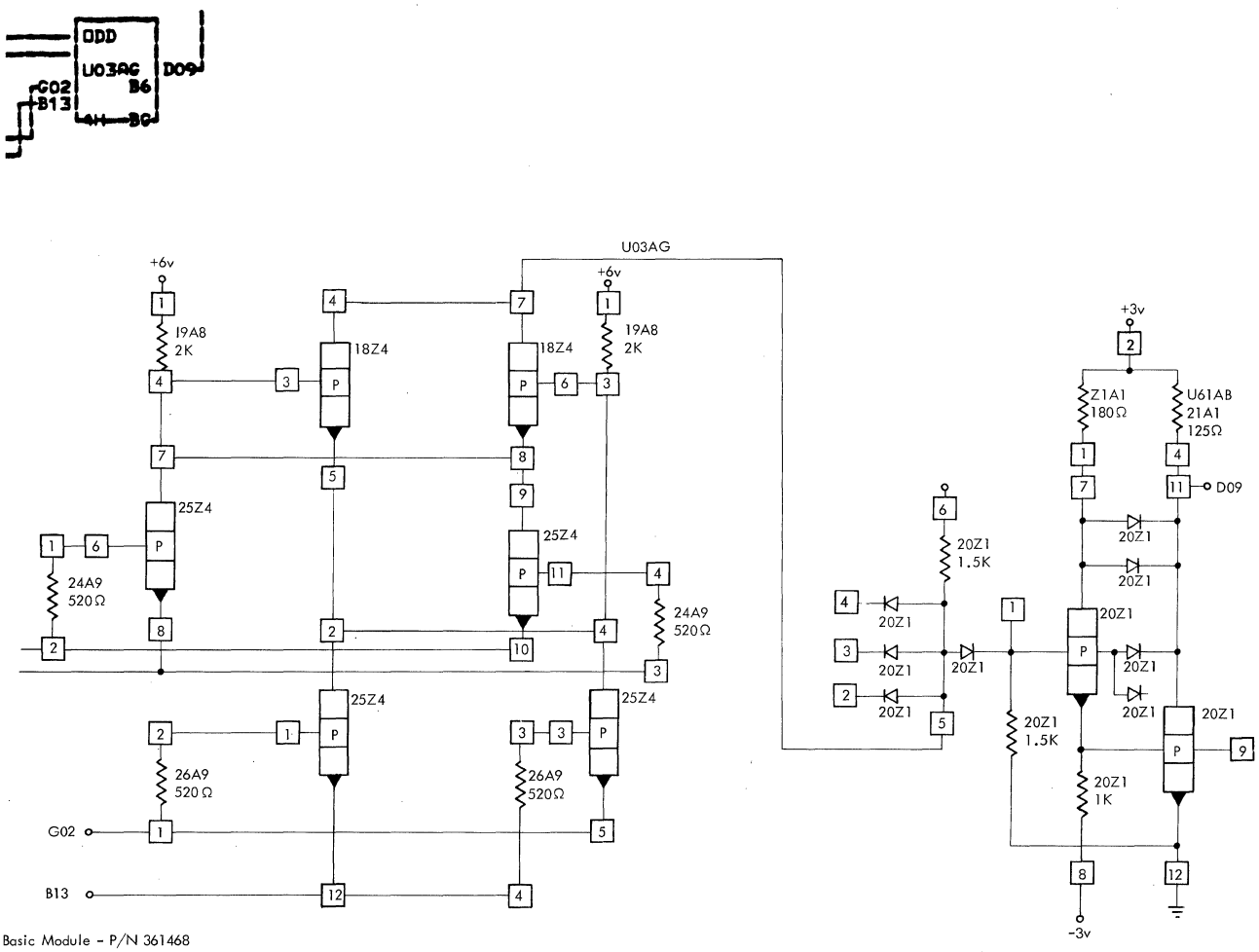
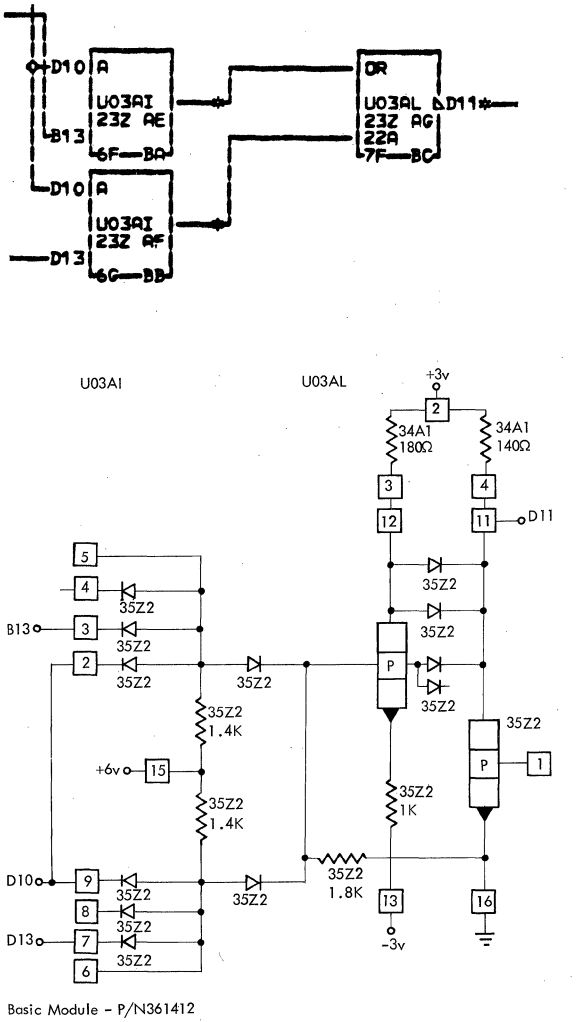
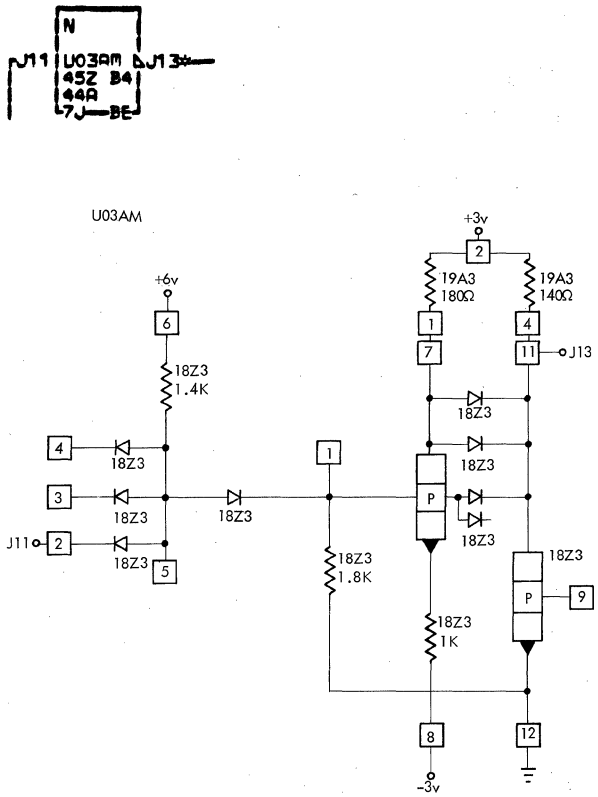


•Figure 82. U03AG, Four-Way Exclusive OR (ODD)



Basic Module - P/N361412

•Figure 83. U03AI, AND
U03AL, OR-Inverter with Load



Basic Module - P/N361408

•Figure 84. U03AM, AND-Inverter with Load

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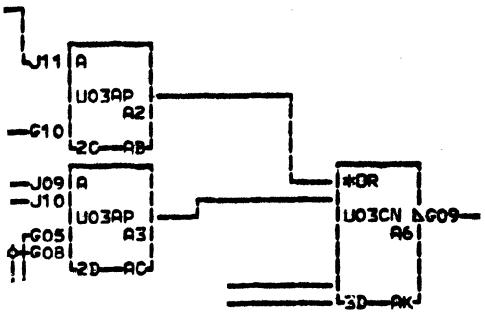
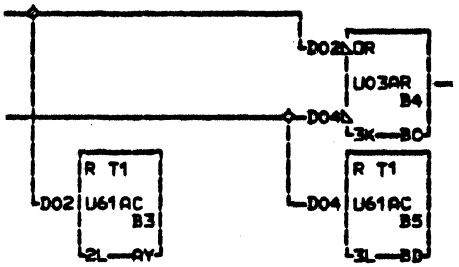
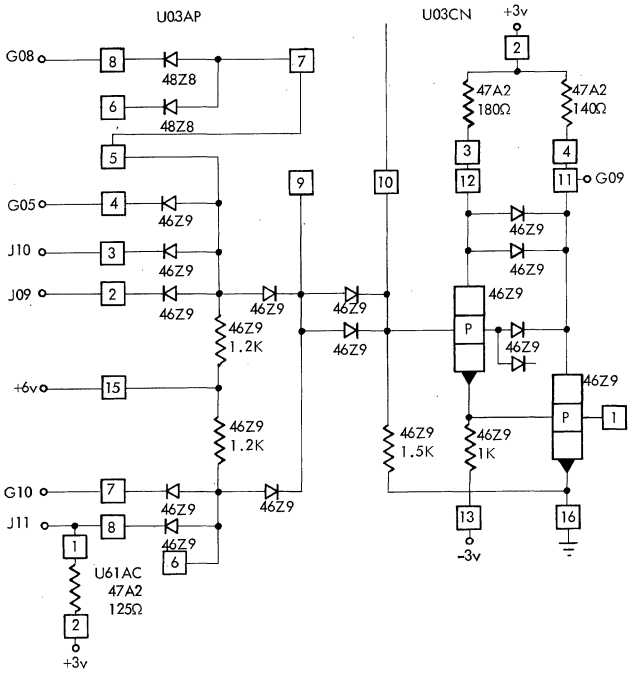
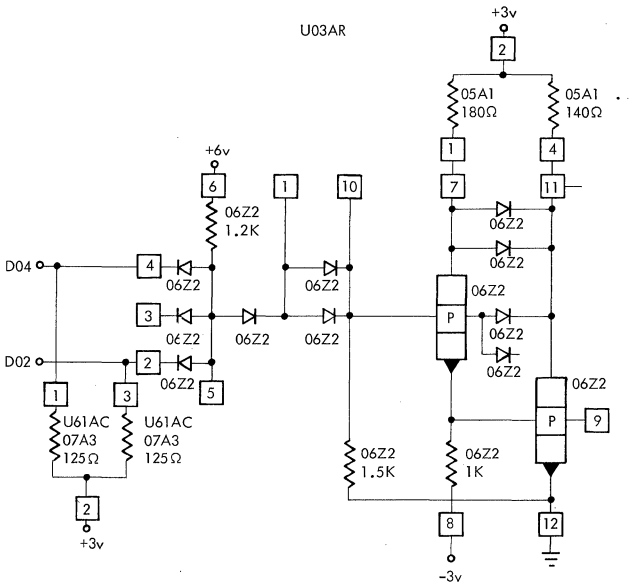






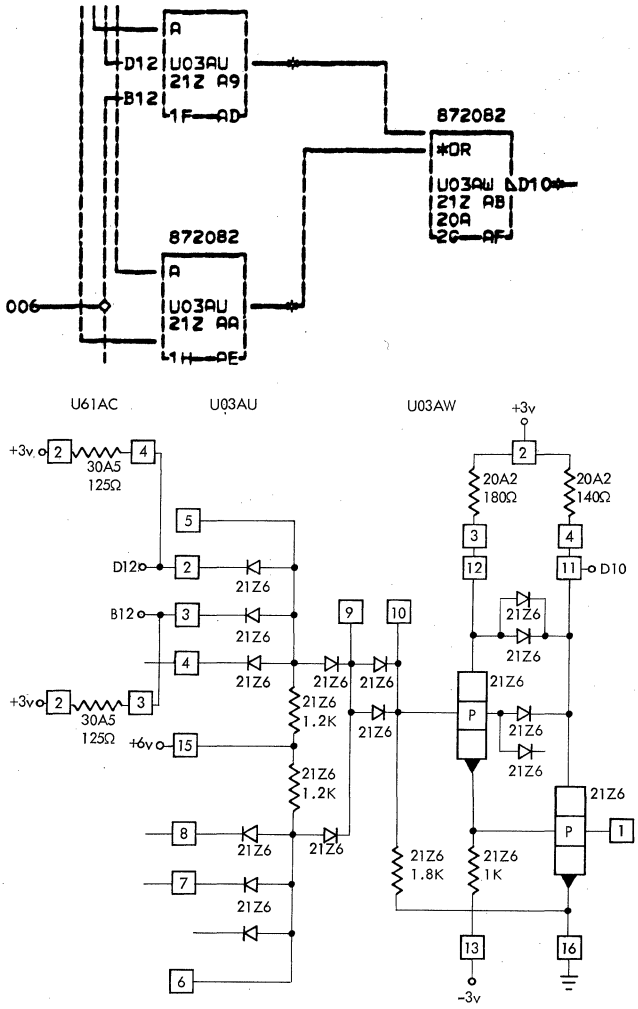
Basic Module - P/N361407

•Figure 85. U03AP, AND Network to 1.2K
U03CN, OR-Inverter-Terminate with Load

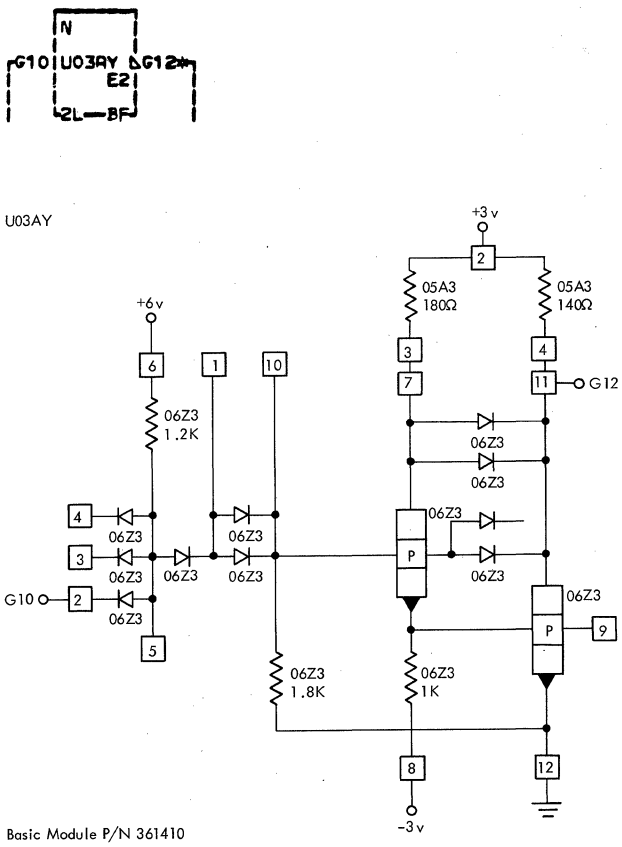


Basic Module - P/N 361404

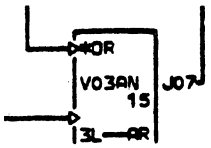
•Figure 86. U03AR, AND-Inverter-Terminate with Load

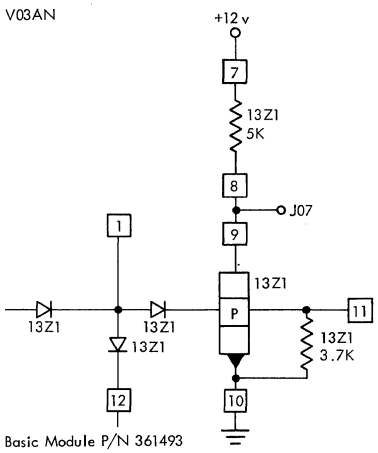


•Figure 87. U03AU, AND-Terminate
U03AW, OR-Terminate Inverter with Load
U61AC, 125 Ohm to +3v

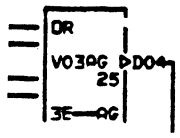


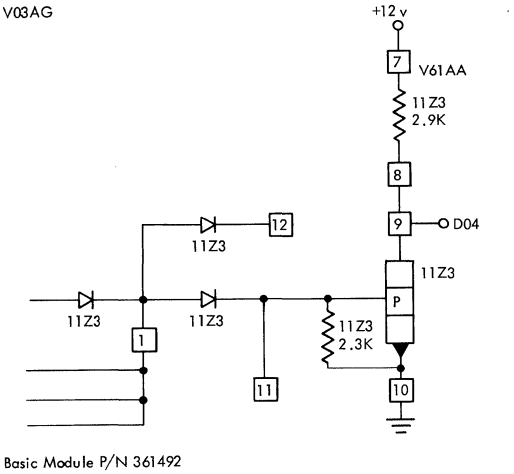
•Figure 88. U03AY, AND-Inverter-Terminate with Load



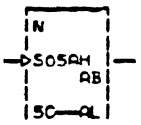


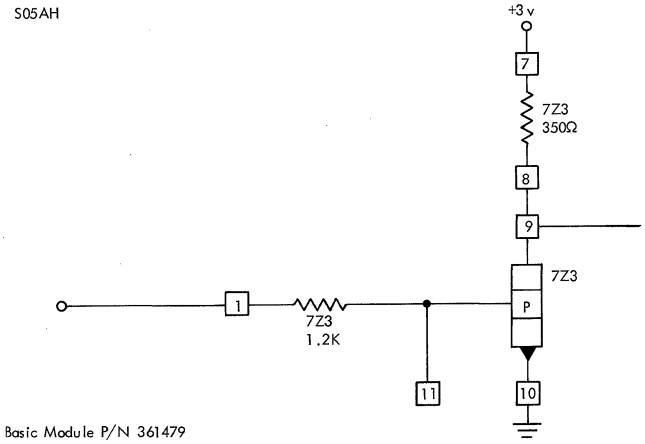
•Figure 89. V03AN, OR-Inverter for Low-Speed Flip Flop



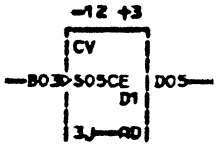


•Figure 90. V03AG, OR-Power-Inverter 2.9K Load





•Figure 91. S05AH, Isolating Inverter



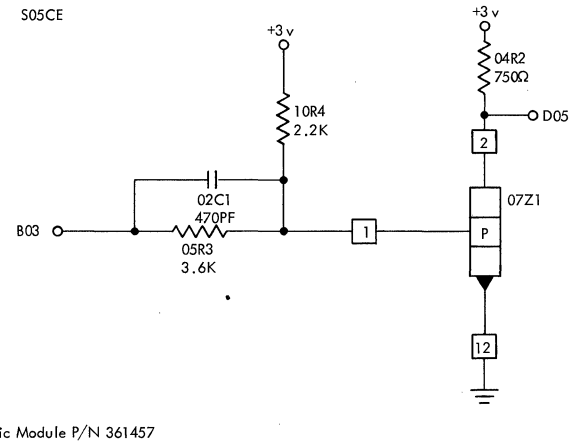
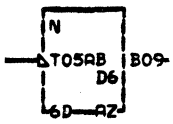
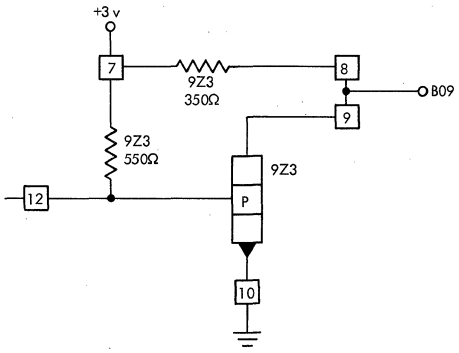


Figure 92. S05CE, S to SLT Level Converter

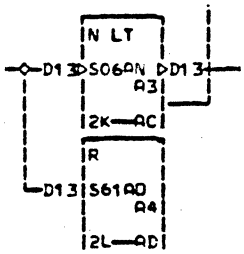


T05AB

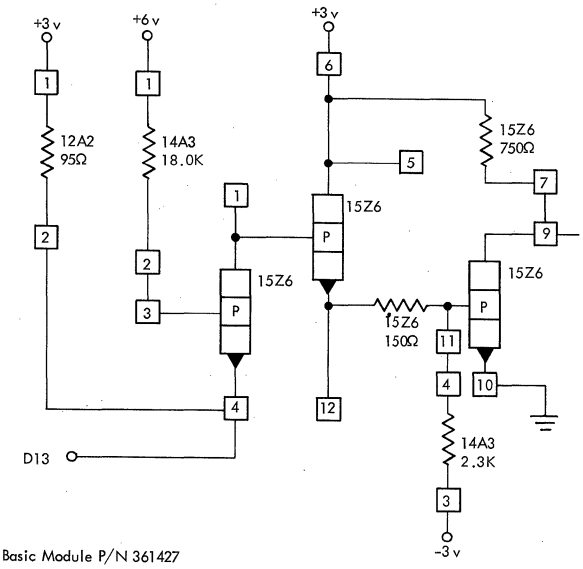


Basic Module P/N 361454

Figure 93. T05AB, Inverter Direct Coupled – 350 Ohm load

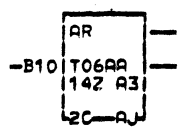


S06AN

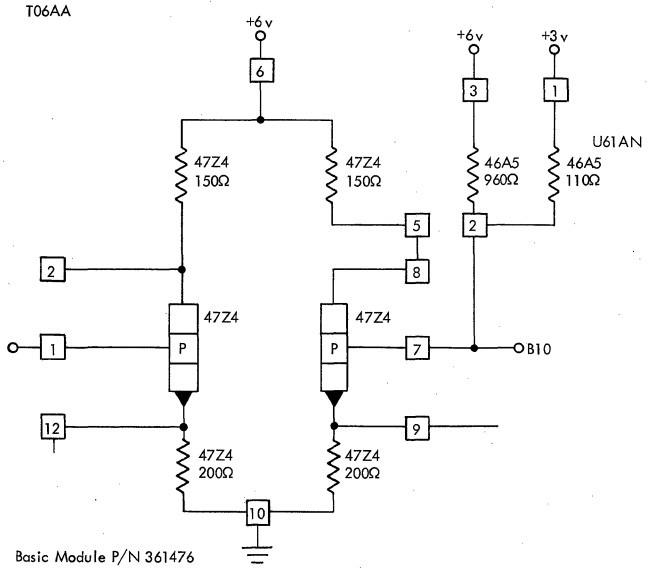


Basic Module P/N 361427

•Figure 95. S06AN, Transmission Line Receiver with Load

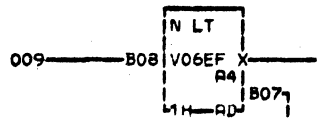


T06AA

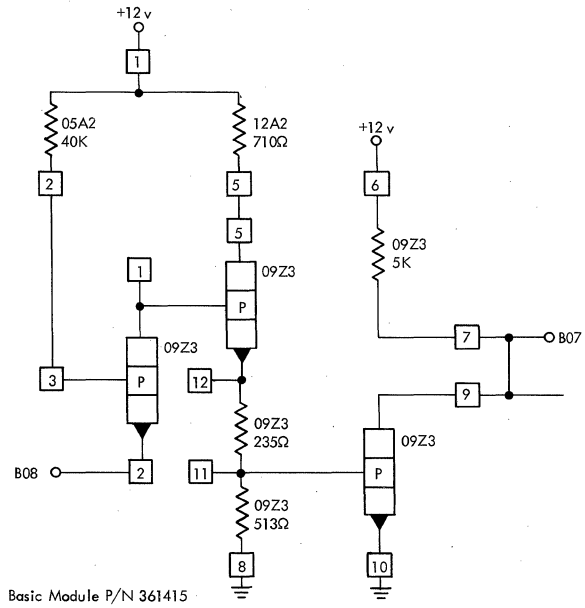


Basic Module P/N 361476

Figure 94. T06AA, Line Sensing Amplifier U61AN, LSA Resistor Network

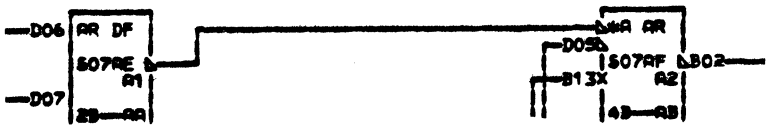


V06EF



Basic Module P/N 361415

Figure 96. V06EF, NPL Line Receiver – 5K Load



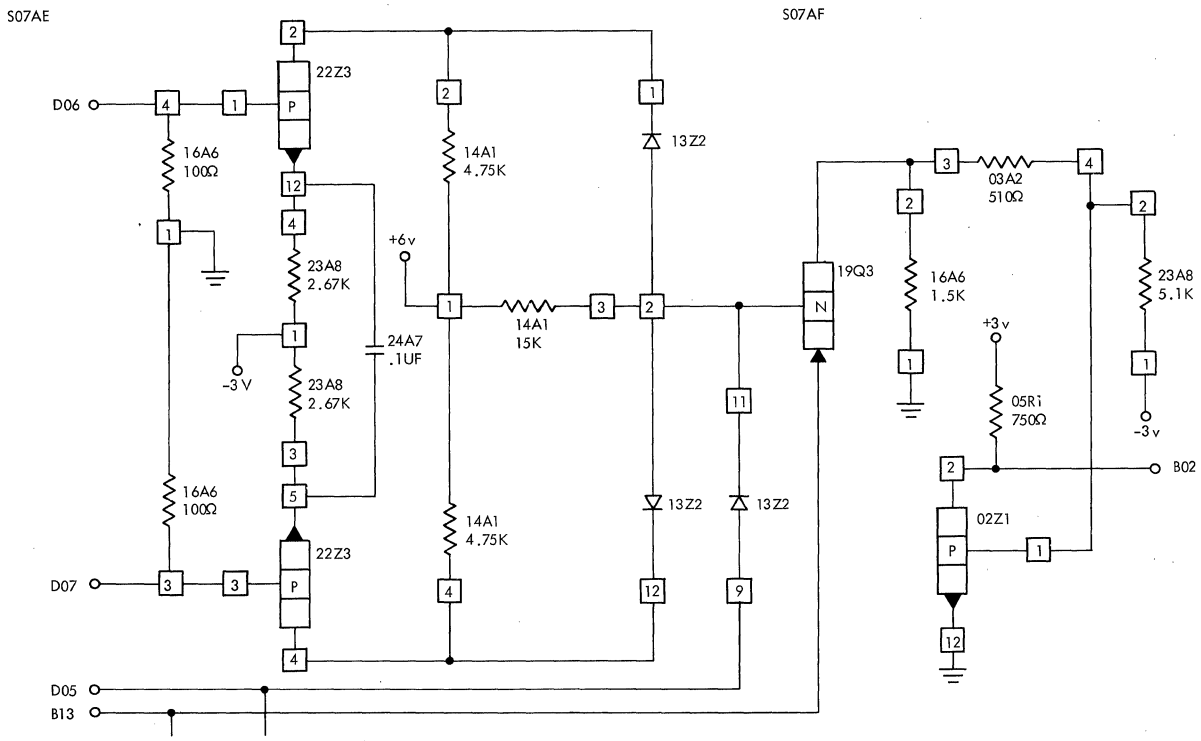


Figure 97. S07AE, Sense Amplifier 2 Part B
S07AF, Sense Amplifier 2 Part A

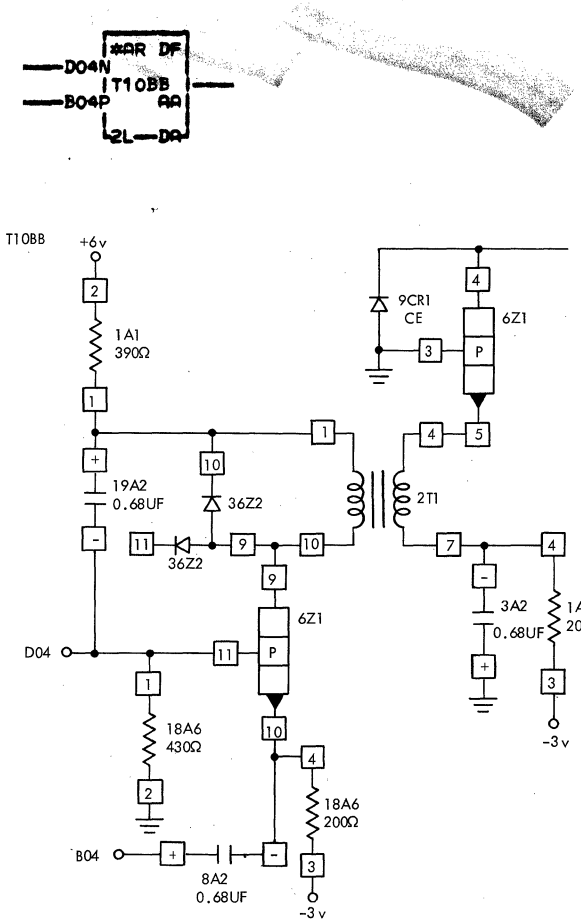
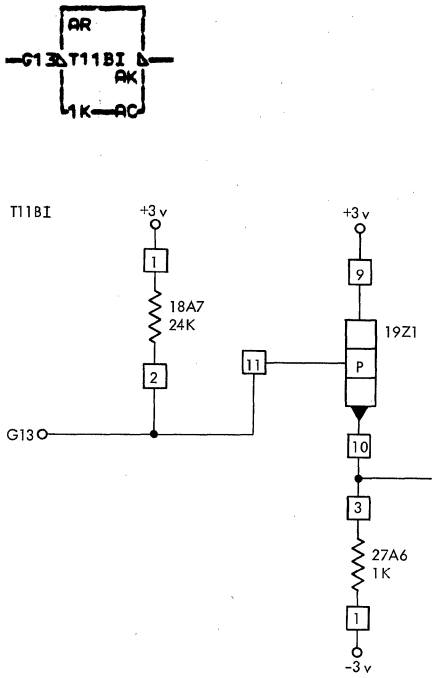


Figure 98. T10BB, Sense Amplifier



•Figure 99. T11BI, Emitter Follower

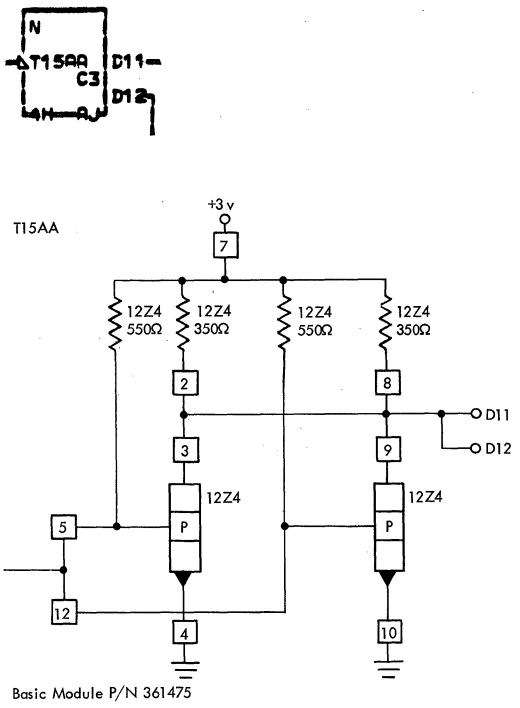


Figure 100. T15AA, High Power Driver – 175 Ohm Load

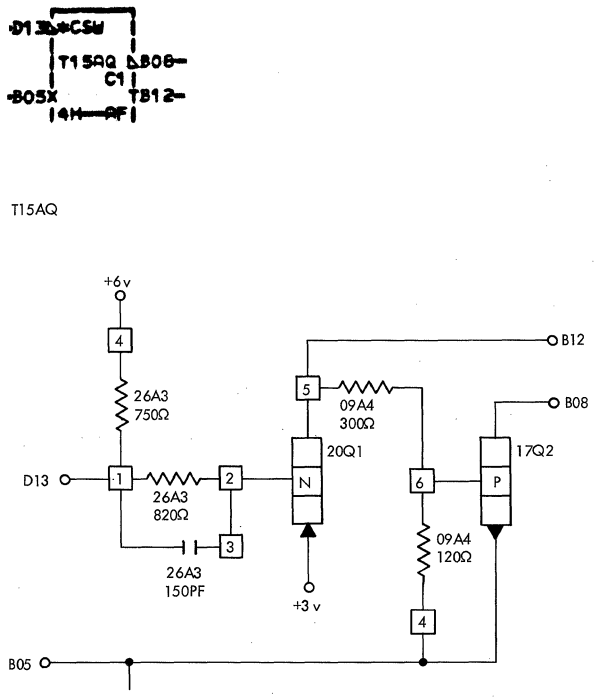
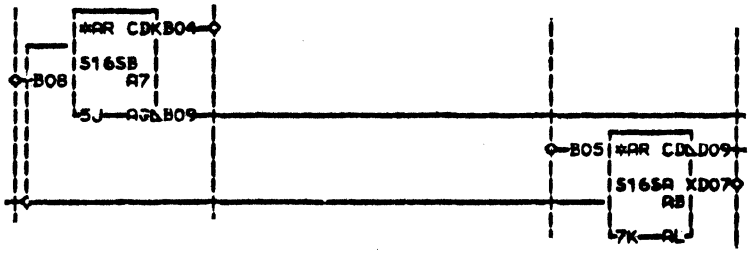


Figure 101. T15AQ, XY Gate OR Inhibit Driver



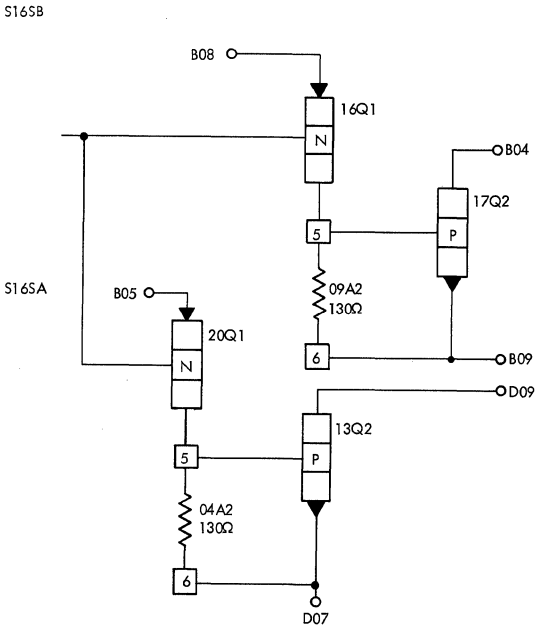


Figure 102. S16SA, XY Gate
S16SB, XY Driver

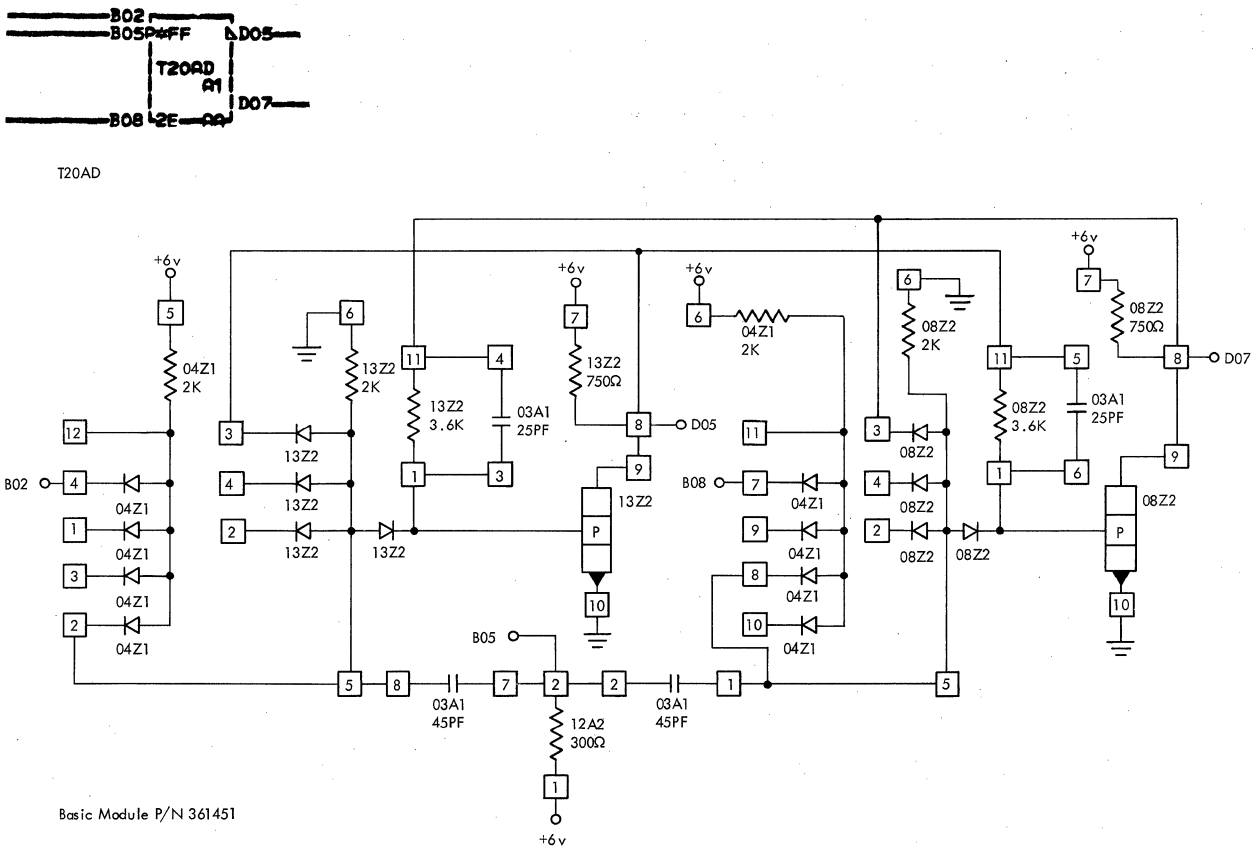
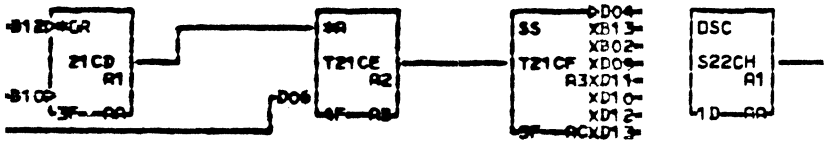
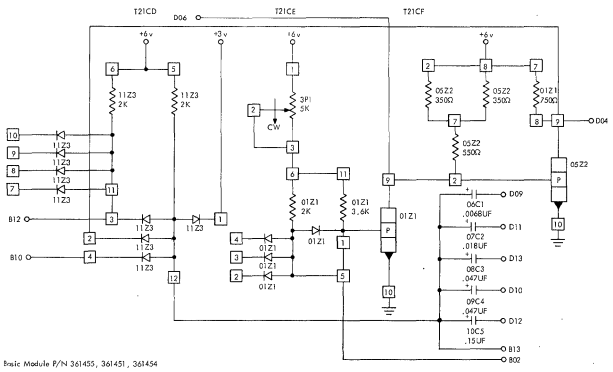


Figure 103. T20AD, AC Trigger Number 2





•Figure 104. T21CF, Variable Singleshot

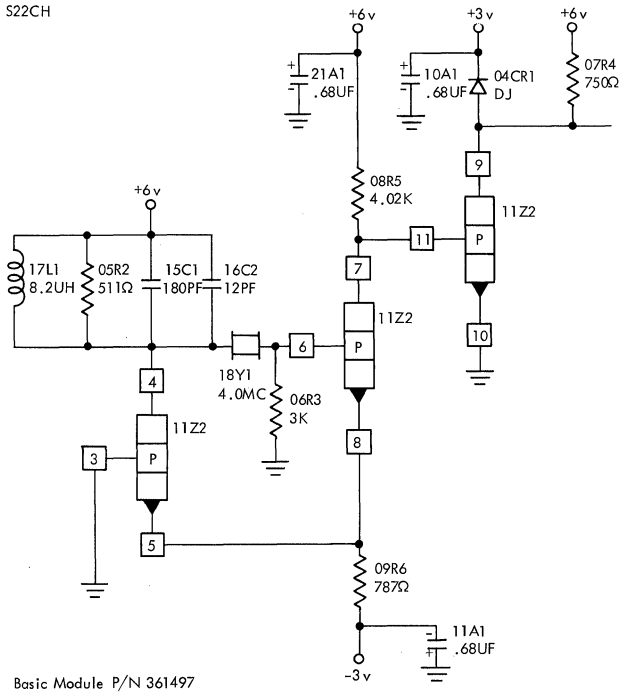


Figure 105. S22CH, 4.0 mc Crystal Oscillator

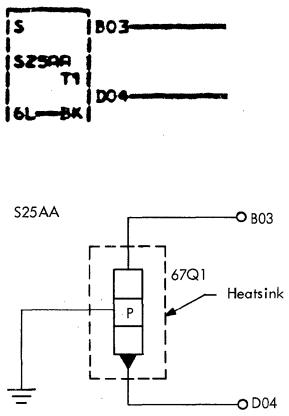
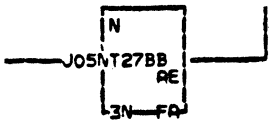
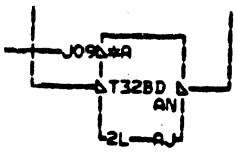
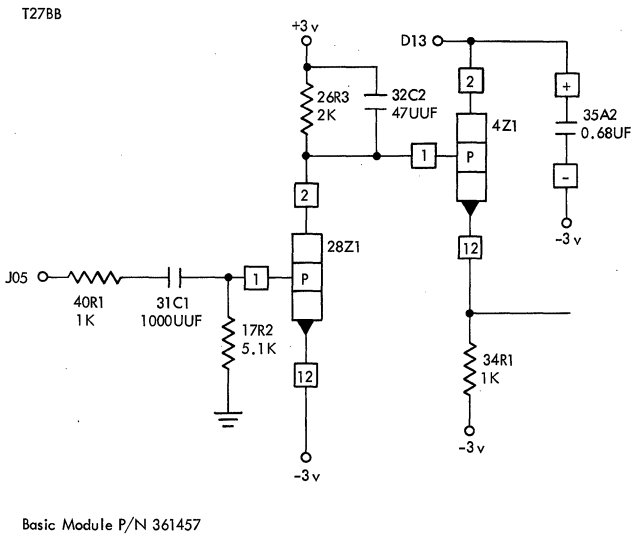


Figure 106. S25AA, Z Clamp

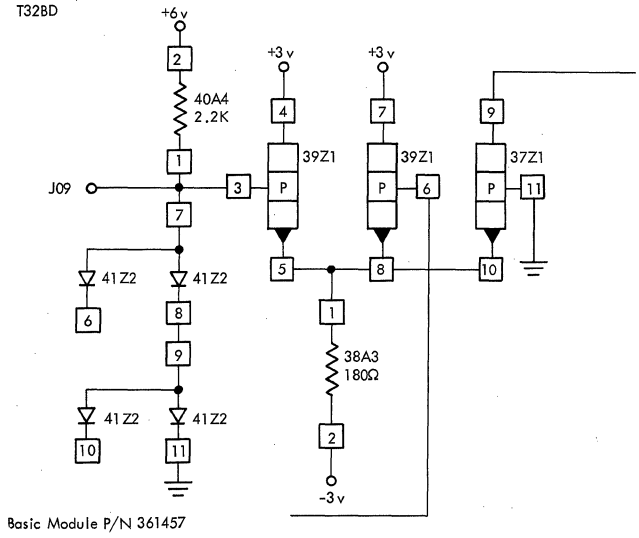






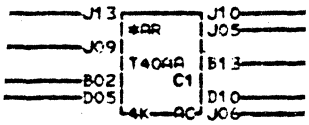
Basic Module P/N 361457

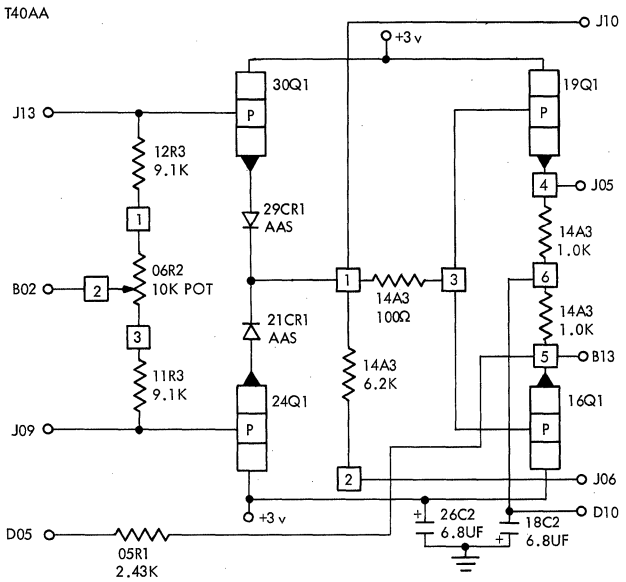
Figure 107. T27BB, Sense Clamp Power Amplifier



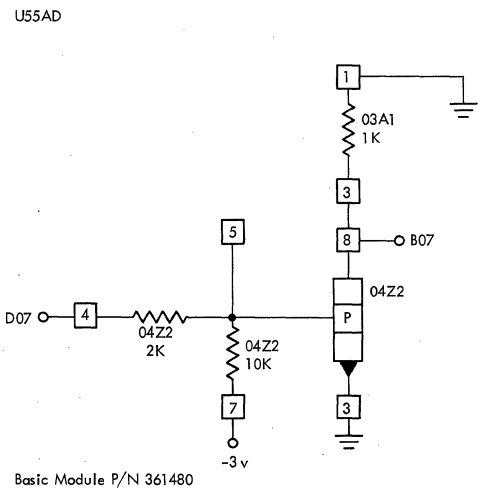
Basic Module P/N 361457

•Figure 108. T32BD, Threshold Gate



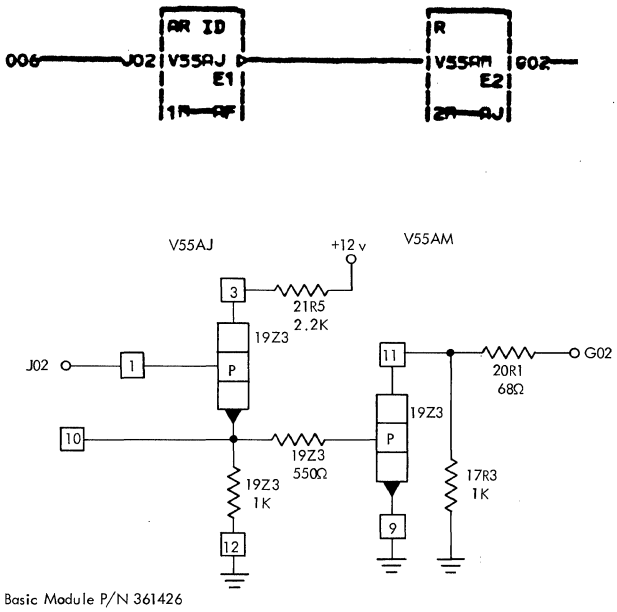


•Figure 109. T40AA, NPL Final Amplifier Rectifier and Channel Separator



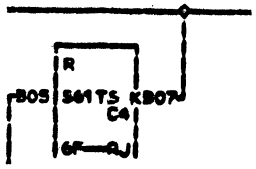
Basic Module P/N 361480

•Figure 110. U55AD, 15 ma Switch ID – 1K Load

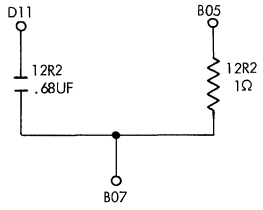


Basic Module P/N 361426

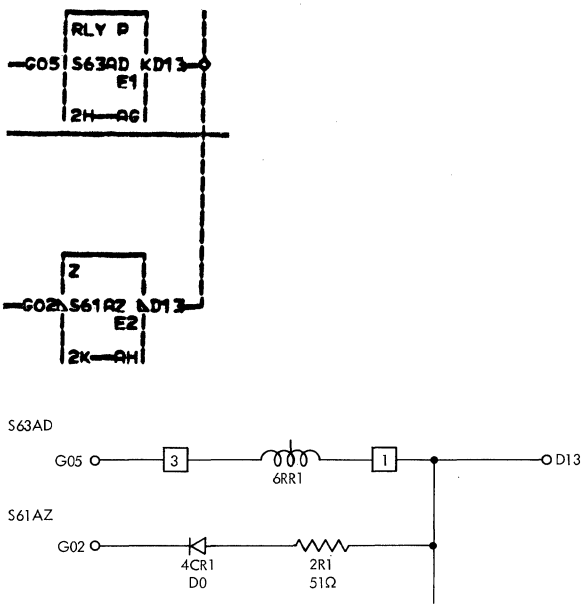
Figure 111. V55AJ, 700 ns-40 ma Indicator Driver Unloaded
V55AM, Resistor for V55AK



S61TS

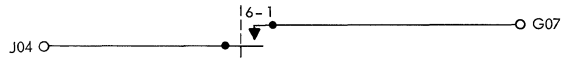


•Figure 112. S61TS, Resistor – 1 Ohm



•Figure 113. S63AD, Coil Six-Pole Reed Relay
S61AZ, Reed Relay Suppression

S63AE



•Figure 114. S63AE, Relay Point Reed

Modules

Several types and speeds of modules are used in SLT circuits. Figures 116 through 157 show the circuit configuration with pin numbers of the modules used. For ease in cross-referencing, we have listed the modules in Figure 115 by part number and by name.

MODULES BY PART NUMBER AND TYPE

361404	AOI10T	HS
361405	AOX10T	HS
361406	AOI10B	HS
361407	AOI10BT	HS
361408	AOI11	HS
361409	AOX11	HS
361410	AOI11T	HS
361412	AOI11B	HS
361413	AOI11BT	HS
361414	FDD11	HS
361415	TLR	LS
361426	ID	
361427	TLR	
361429	FTX	MS
361430	FTX	
361433	FTX	
361451	AI	MS
361453	AOI	MS
361454	DCI	MS
361455	AOX	MS
361456	AOXB	MS
361457	FTX	MS
361459	FDD	MS
361468	AOI10	HS
361469	AOX10	HS
361473	API	MS
361475	HPD	MS
361476	LSA	
361477	XOR	MS
361479	II	MS
361480	ID	
361482	FDD	HS
361483	FDD	MS
361486	XORL	MS
361489	AOX2	LS
361492	AOPI	LS
361493	AOI	LS
361494	DCI	LS
361495	AOX1	LS
361496	AOPX-1	LS
361497	FTX	LS
361499	FDD	LS

MODULES BY NAME

361451	AI	MS
361453	AOI	MS
361493	AOI	LS
361468	AOI10	HS
361406	AOI10B	HS
361407	AOI10BT	HS
361404	AOI10T	HS
361408	AOI11	HS
361412	AOI11B	HS
361413	AOI11BT	HS
361410	AOI11T	HS
361492	AOPI	LS
361496	AOPX-1	LS
361455	AOX	MS
361495	AOX1	LS
361469	AOX10	HS
361405	AOX10T	HS
361409	AOX11	HS
361456	AOXB	MS
361489	AOX2	LS
361473	API	MS
361454	DCI	MS
361494	DCI	LS
361459	FDD	MS
361482	FDD	HS
361483	FDD	MS
361499	FDD	LS
361414	FDD11	HS
361429	FTX	MS
361430	FTX	
361433	FTX	
361457	FTX	MS
361497	FTX	LS
361475	HPD	MS
361426	ID	
361480	ID	
361479	II	MS
361476	LSA	
361415	TLR	LS
361427	TLR	
361477	XOR	MS
361486	XORL	MS

•Figure 115. Modules

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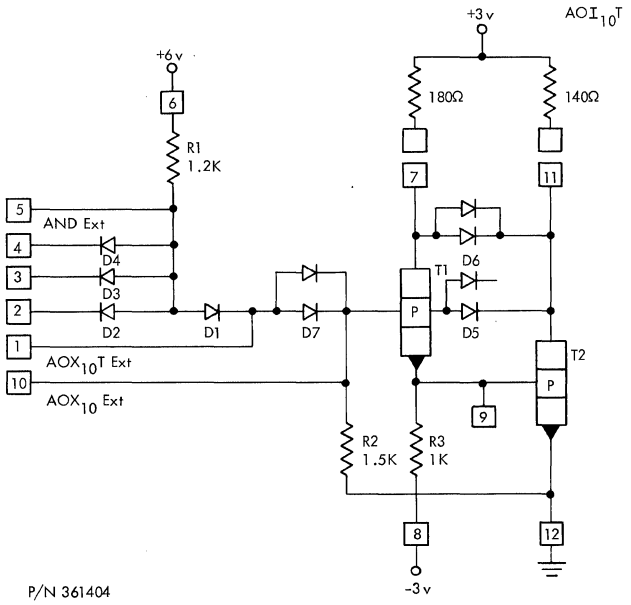

Figure 116. ($AOI_{10}T$) AND-OR-Inverter-Terminate, High-Speed

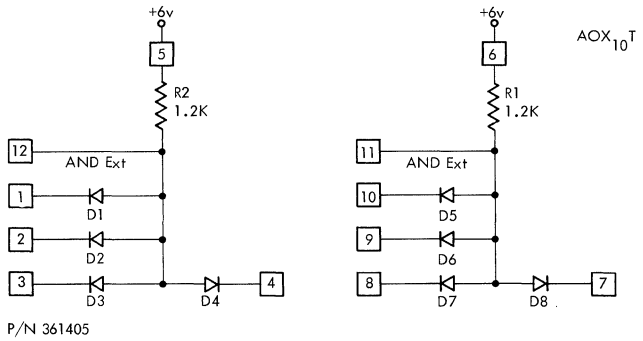

Figure 117. ($AOX_{10}T$) AND-OR-Extender-Terminate, High-Speed

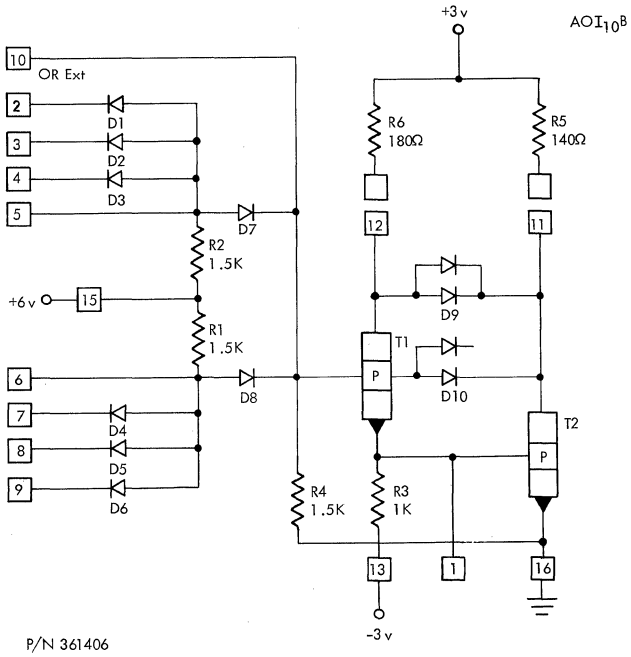

Figure 118. ($AOI_{10}B$) AND-OR-Inverter, High-Speed

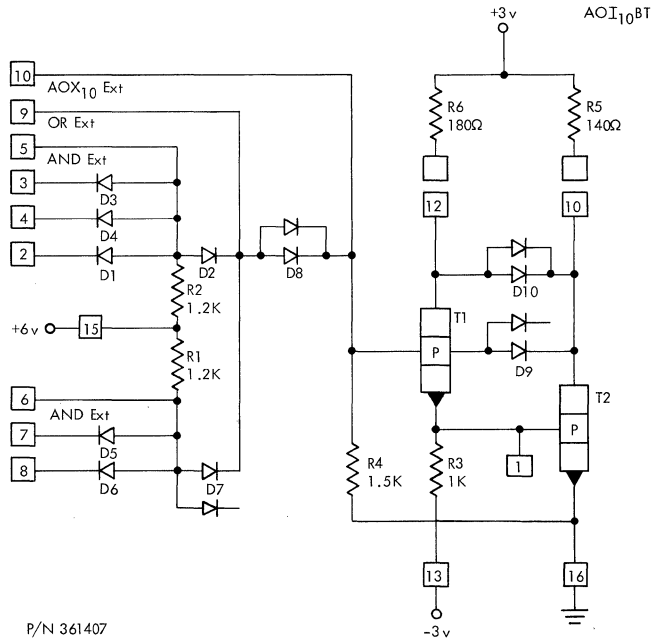

Figure 119. ($AOI_{10}BT$) AND-OR-Inverter-Terminate, High-Speed

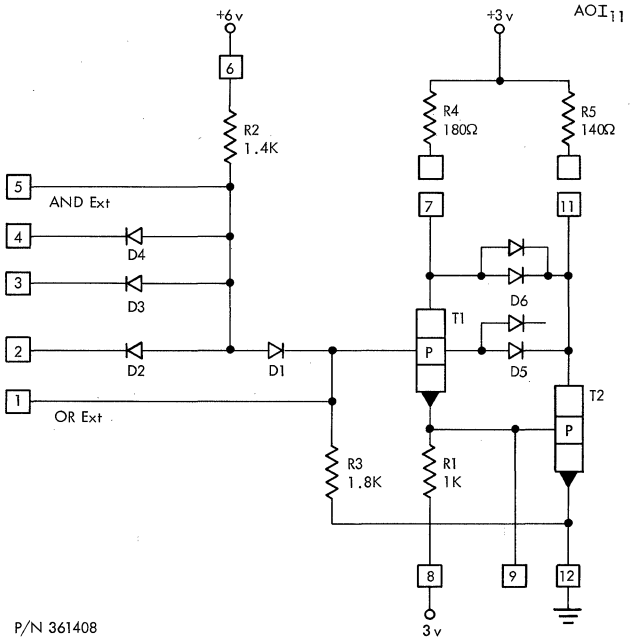

Figure 120. (AOI_{11}) AND-OR-Inverter, High-Speed

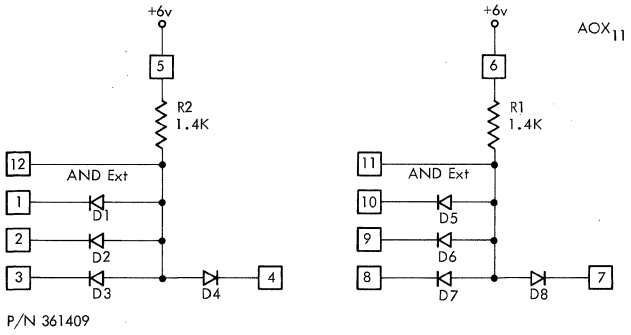

Figure 121. (AOX_{11}) AND-OR-Extender, High-Speed

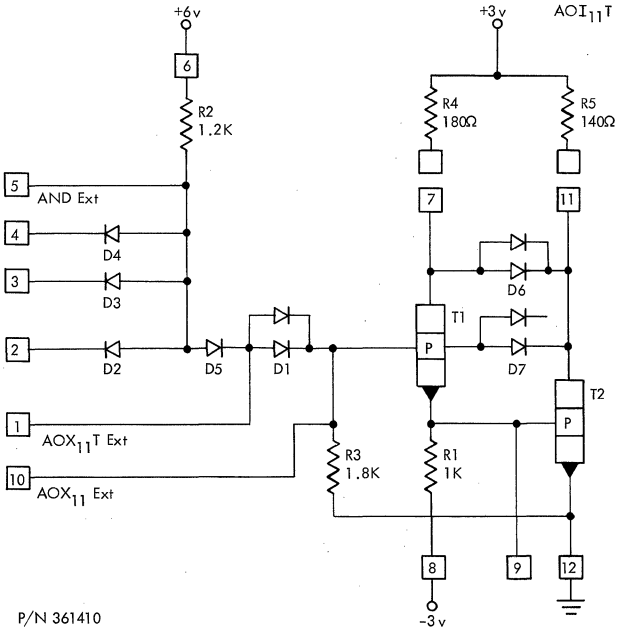

Figure 122. ($AOI_{11}T$) AND-OR-Inverter-Terminate, High-Speed

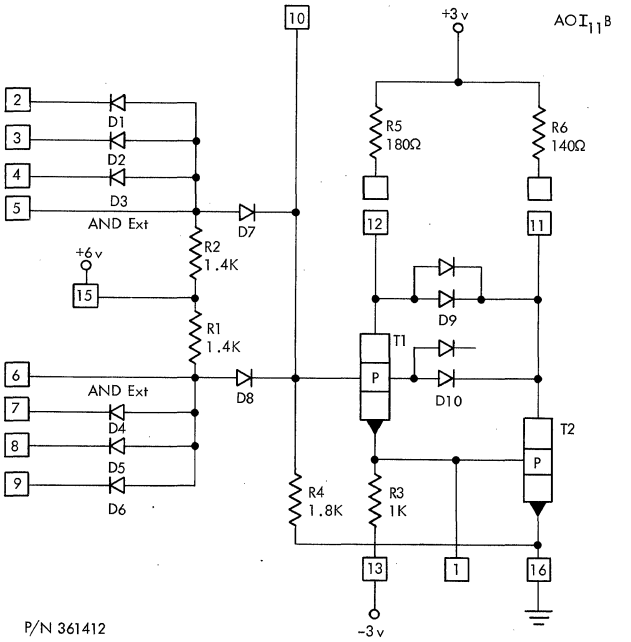

Figure 123. ($AOI_{11}B$) AND-OR-Inverter (Two-Way OR), High-Speed

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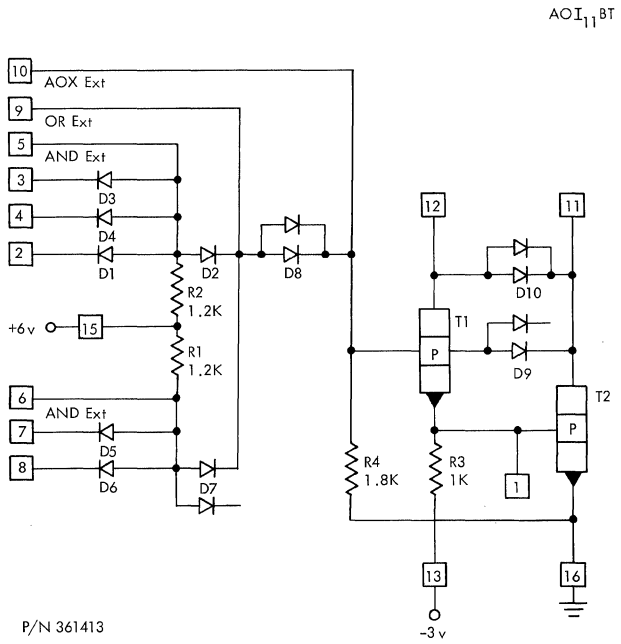


Figure 124. ($AOI_{11}BT$) AND-OR-Inverter, High-Speed

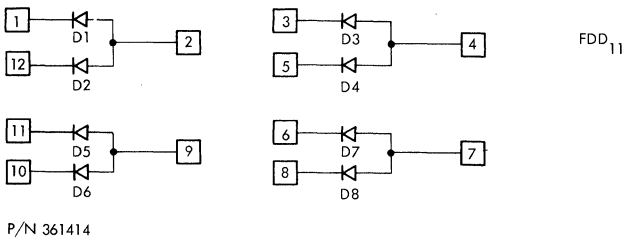
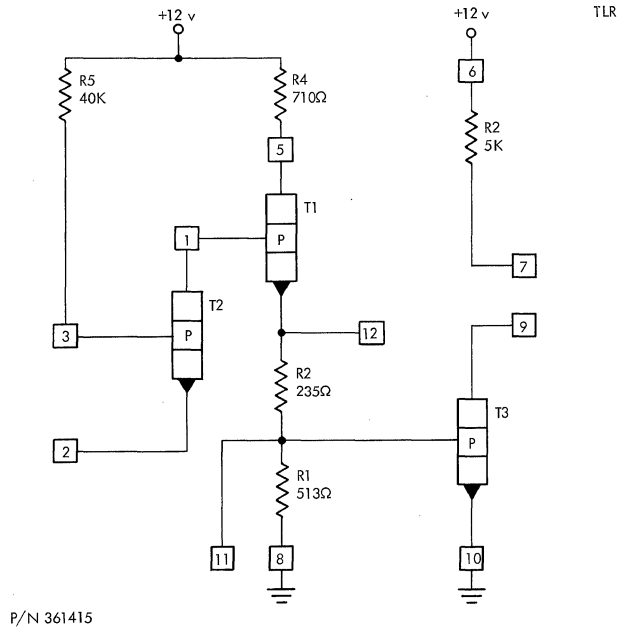


Figure 125. (FDD_{11}) Four Double Diodes, High-Speed



•Figure 126. (TLR) Transmission Line Receiver, Low-Speed

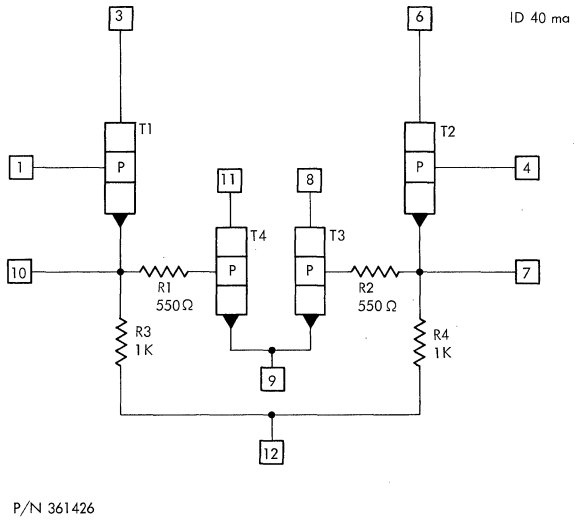
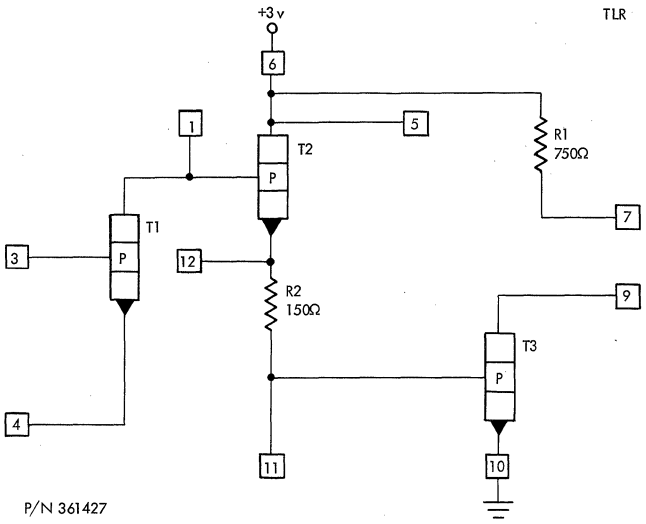


Figure 127. (ID) Indicator Driver, 40 ma



•Figure 128. (TLR) Transmission Line Receiver

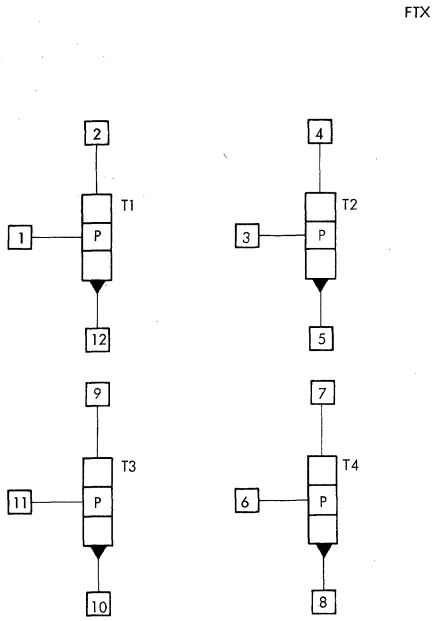


Figure 129. (FTX) Four Transistors 12v, Medium-Speed

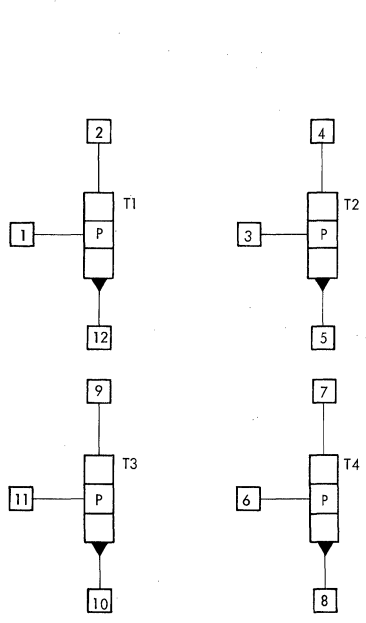


Figure 130. (FTX) Four Transistors

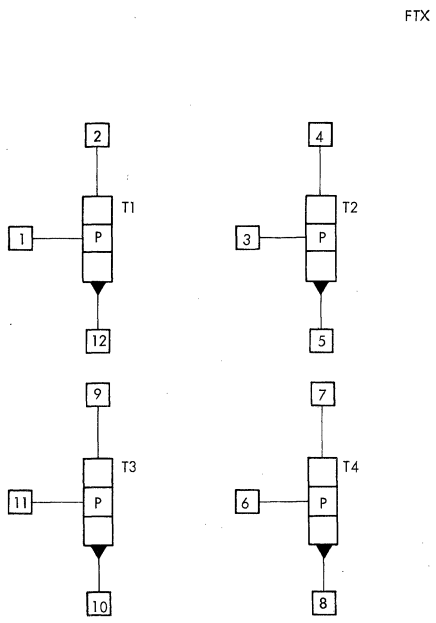


Figure 131. (FTX) Four Transistors

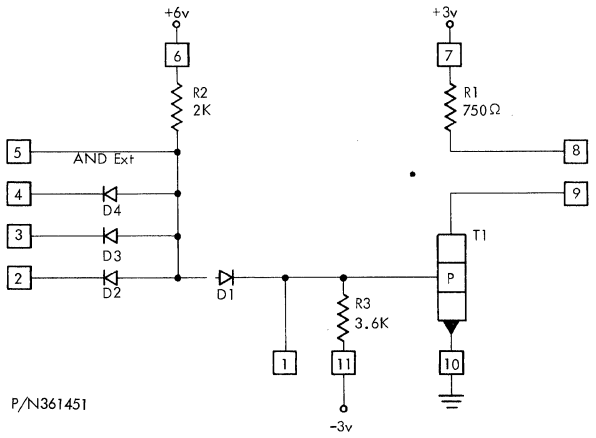
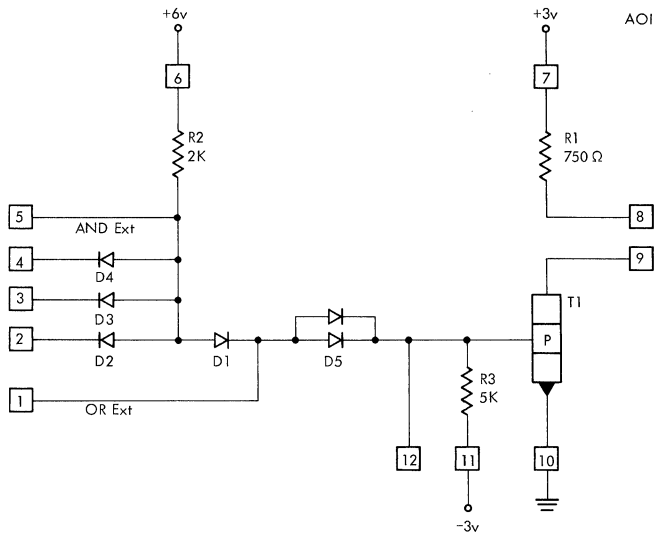


Figure 132. (AI) AND-Inverter, Medium-Speed



•Figure 133. (AOI) AND-OR-Inverter, Medium-Speed

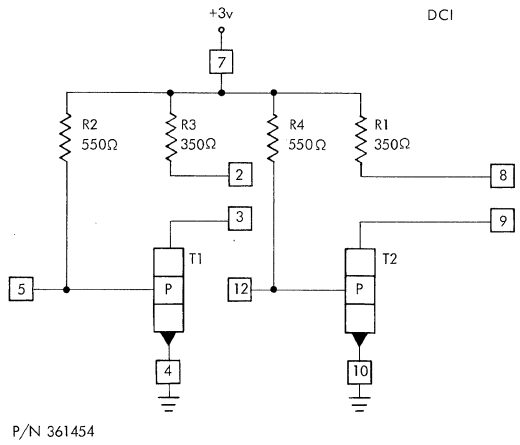


Figure 134. (DCI) Direct Coupled Inverter, Medium-Speed

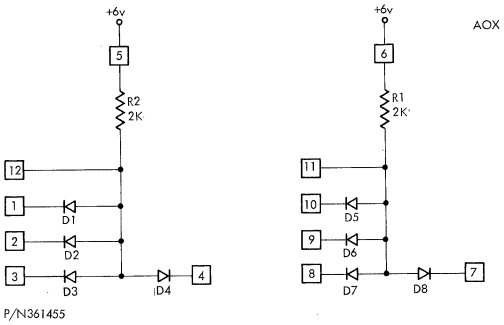


Figure 135. (AOX) AND-OR-Extender, Medium-Speed

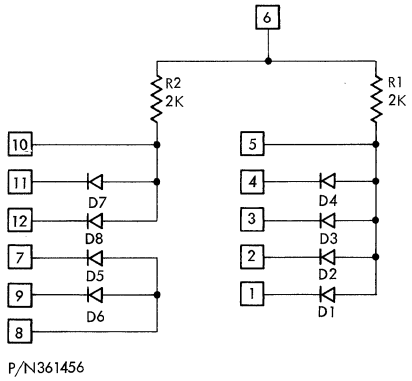


Figure 136. (AOX_B) AND-OR-Extender, Medium-Speed

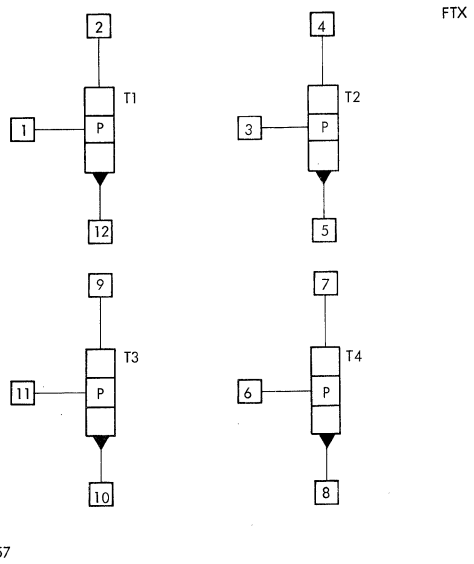


Figure 137. (FTX) Four Transistors 9v, Medium-Speed

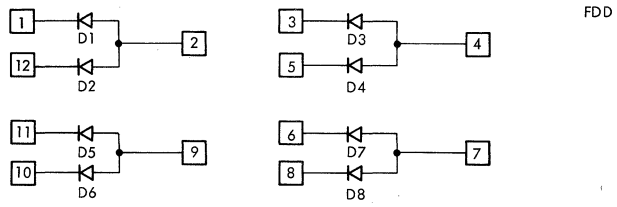


Figure 138. (FDD) Four Double Diodes, Medium-Speed

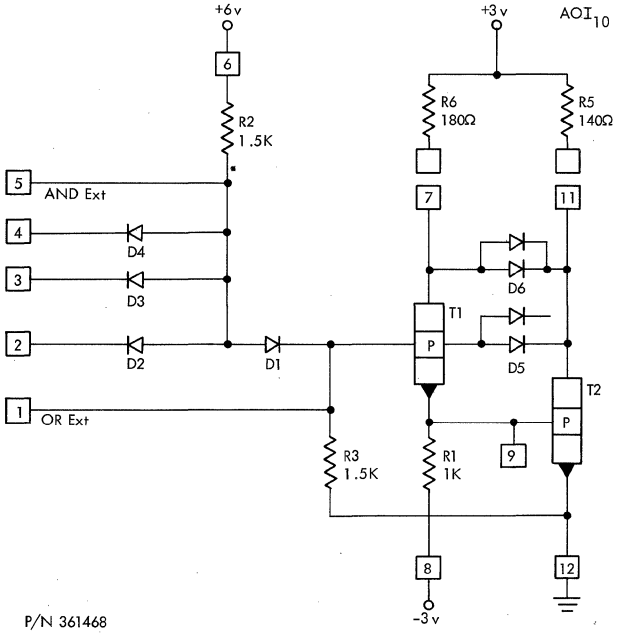


Figure 139. (AOI_{10}) AND-OR-Inverter, High-Speed

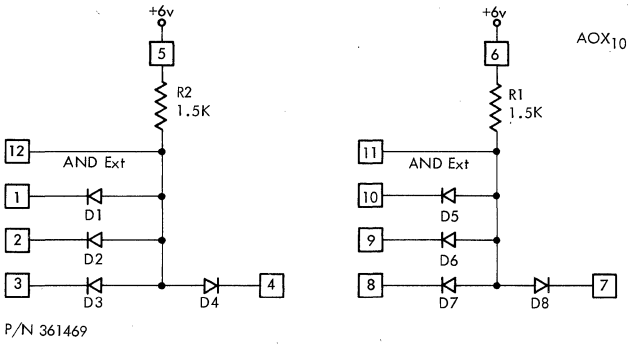


Figure 140. (AOX_{10}) AND-OR-Extender, High-Speed

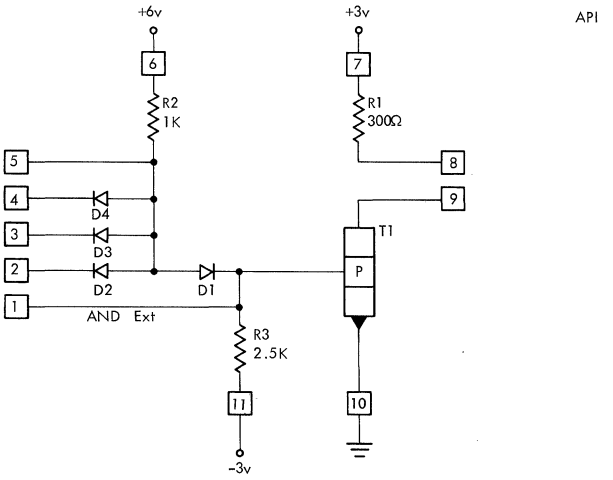


Figure 141. (API) (3v) AND-Power-Inverter, Medium-Speed

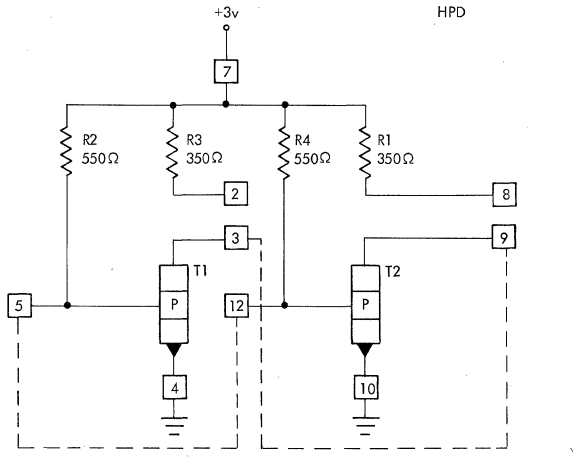
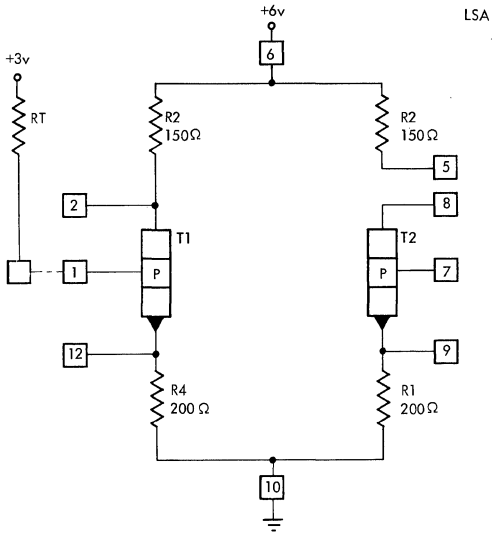
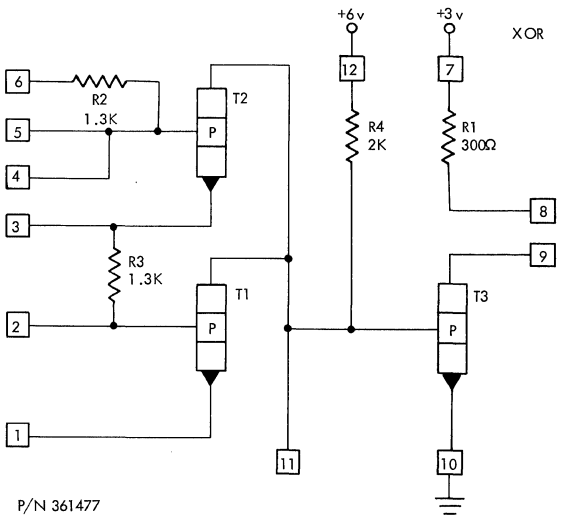


Figure 142. (HPD) High Power Driver



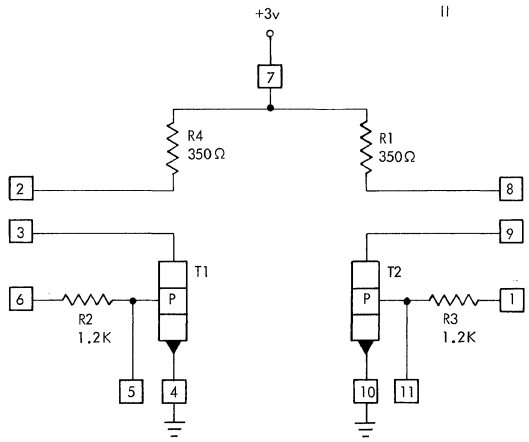
P/N 361476

Figure 143. (LSA) Line Sense Amplifier



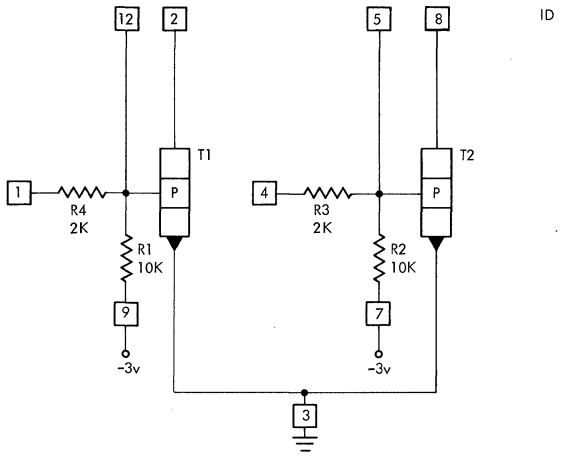
P/N 361477

Figure 144. (XOR) Exclusive OR, Medium-Speed



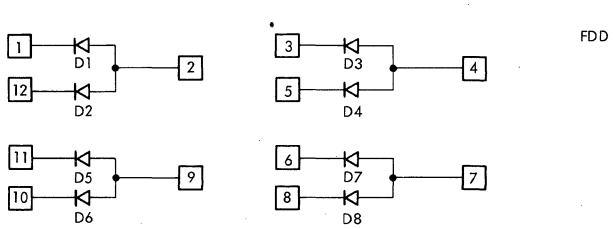
P/N 361479

Figure 145. (II) Isolating Inverter, Medium-Speed



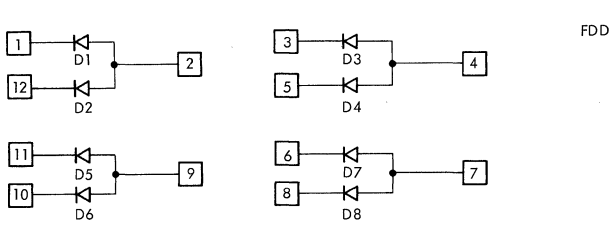
P/N 361480

Figure 146. (ID) Indicator Driver



P/N 361482

Figure 147. (FDD) Four Double Diodes, High-Speed



P/N 361483

Figure 148. (FDD) Four Double Diodes (General Purpose), Medium-Speed

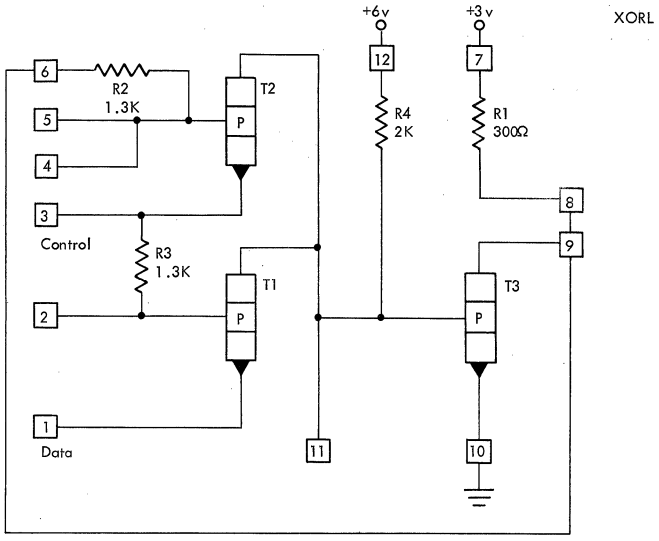
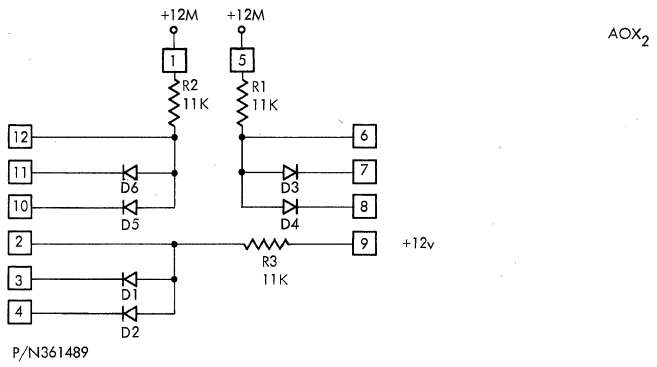
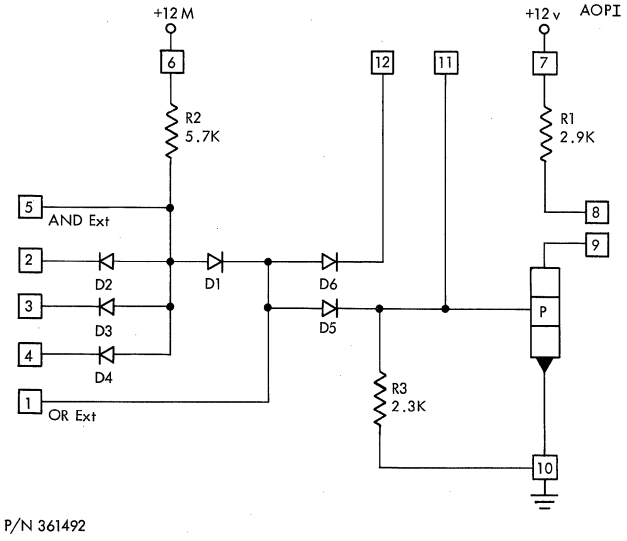


Figure 149. (XORL) Exclusive OR Latch, Medium-Speed



•Figure 150. (AOX_2) AND-OR-Extender, Low-Speed



•Figure 151. (AOPI) AND-OR-Power-Inverter, Low-Speed

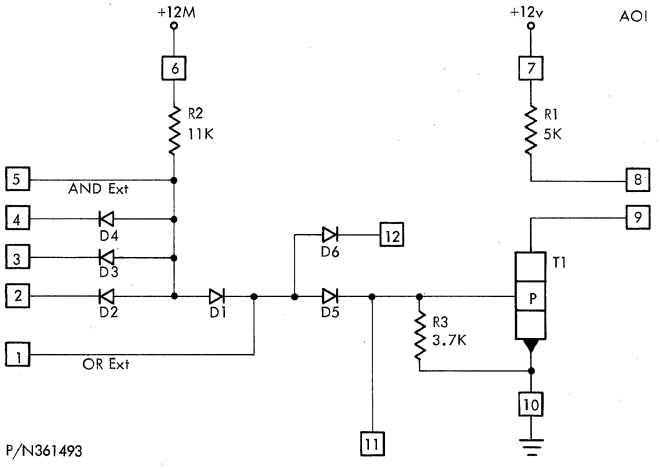
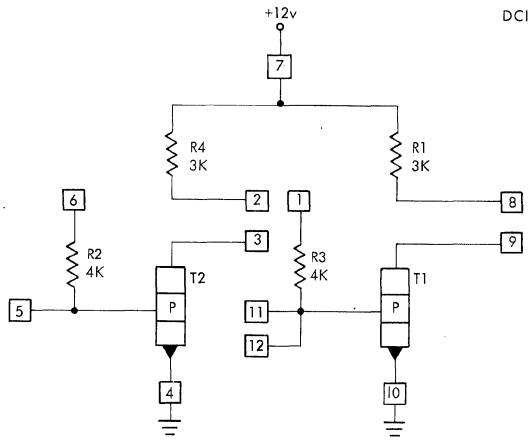
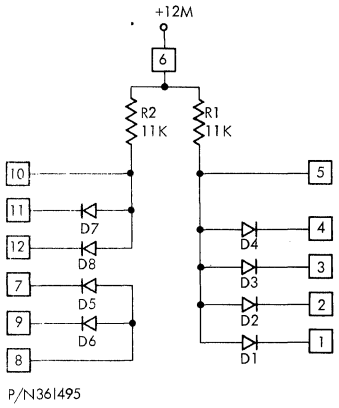


Figure 152. (AOI) AND-OR-Inverter, Low-Speed



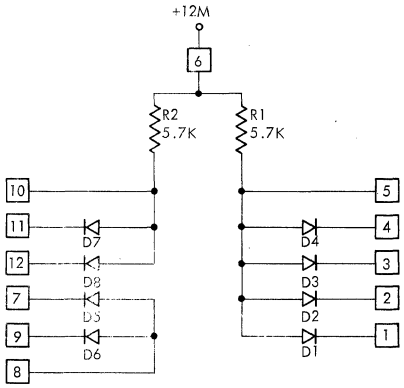
P/N 361494

Figure 153. (DCI) Direct Coupled Inverter, Low-Speed



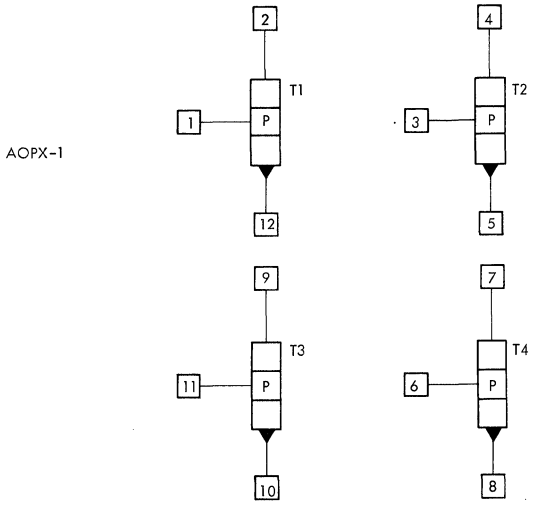
P/N361495

Figure 154. (AOX_1) AND-OR-Extender, Low-Speed



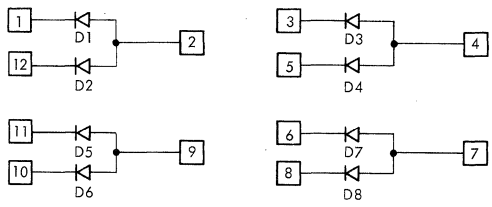
P/N361496

Figure 155. ($AOPX_1$) AND-OR-Power-Extender



P/N 361497

Figure 156. (FTX) Four Amplifier and Saturating Transistors, Low-Speed



P/N 361499

Figure 157. (FDD) Four Double Diodes

Glossary

Basic refers to the standard design of the machine; it includes optional features (MFI's) if drawn as part of the standard logic page. "Basic" is in contrast to "Version."

Circuit Number consists of five alphameric characters of the form ANNAA, which uniquely define a particular basic circuit.

Design Automation refers to the programs that prepare and print the ALD's. They consist of four major stages of processing: logic master tape, simulation, packaging and checking, and physical master tape. The outputs consist of documents to aid engineering in the development of computers, release documents (ALD's), and tapes for manufacturing.

DOT Block is an ALD block used on ALD logic pages to show DOT AND and DOT OR functions, which are physically accomplished by tying two signals together at a pin. Thus, one logical net on the ALD is combined with other logical nets by the DOT block to produce one combined physical net.

NOTE: One DOT block does not connect to another DOT block.

Grouping refers to the associating of certain circuit configurations prior to partitioning. Circuits represented on the ALD's by more than one block but always found on the same card are said to be in the same group.

Logic Master Tape (LMT) is the machine language record in logic page order. Each time a portion of this machine record is altered, logic pages containing the changes are produced for the engineer.

Net is a complex of modes, normally pins or connectors on the ALD, all common electrically.

Net Number consists of the source block page number, block serial number, and output line position of the source block. It consists of eight alphameric characters of the form AANNNAAB (A-alphabetic, N-numeric, B-either alphabetic or numeric).

Node is one circuit end point of a net (such as a pin on a card or a connector on a board).

Packaging and Checking refers to a series of programs that aid the engineer in the physical packaging of the logic and check data that is manually inserted on the pages.

Partitioning refers to that part of the design automation program that breaks up logic into cards and assigns the cards to boards.

Physical Master Tape (PMT) is a machine language record of the physical aspects of the design. It is arranged in physical sequence. Its purpose is (1) to retain in a convenient form the physical data from LMT, as well as the physical data from the PMT (wiring data primarily), (2) to retain the physical design at a fixed level while the logical design is undergoing change, and (3) to extract information from the tapes at the request of the engineer or other users.

Pins are the male parts of the connection between card and board or between cable connector and board.

Portion refers to those circuits on a card that are connected together by printed wiring.

Signal Name is the title (may be blank) that gives meaning to a logical net; each net has only one signal name.

Simulation refers to programs that allow the engineer to exercise the logic dynamically before the machine is packaged.

Sink is the end or ends of a net to which signals flow.

Source is the beginning of a net from which signals flow.

Symbolic Package is two characters to be used by design automation in the partitioning and placement programs. Blocks with the same characters in the symbolic package field are placed on the same board by the card partitioning program.

NOTE: Blocks with different symbolic packages may be packaged on the same board.

Version is a term used by design automation and indicates the particular manner in which logic records are kept for certain features; a feature is a version of its records and is kept as an add-delete (by block) to the basic records.

NOTE: "Version" gives automatic or implied updating of the feature by the basic, since an added basic block is, in effect, in the version.

Version Page is the ALD page made up of all blocks on the basic page which appear unchanged in the version design, plus additional version blocks needed to change the basic page into the version page.

Via Hole is the plated-through hole which may or may not contain a pin; it is used to make contact between conducting layers of the board. It is not a node.

CIRCUIT NUMBER LISTING

CIRCUIT NUMBER CODE

LOGIC GENERAL FORM - XYYZZ

X DEFINED

S - SRETL GENERAL
T - 30 NS
U - 5-10 NS
V - 700 NS
0 - ANALOG

YY DEFINED

3 - LOGIC BLOCKS
5 - VOLTAGE TRANSLATE CIRCUITS
6 - TRANSMISSION LINE DRIVERS AND RECEIVERS
7 - SENSE AMPLIFIERS
10 - INVERTING DRIVERS LESS THAN 50 MA
11 - NON-INVERT DRIVER LESS THAN 50 MA
15 - POWER DRIVER MORE THAN 50 MA
16 - MAGNETIC HEAD AND CORE DRIVER
20 - TRIGGERS
21 - SINGLESHOTS
22 - OSCILLATORS
25 - REGULATORS, CLAMPS, CLIPPERS, AND LIMITERS
32 - GATES
40 - SPECIALS
45 - DELAY CIRCUITS
55 - INDICATOR CIRCUITS
60 - INTEGRATORS AND FILTERS
61 - COMPONENTS
63 - REED RELAYS
65 - FUNCTIONAL CARD
66 - FIELD REPLACEMENT CARD

ZZ DEFINED - THE UNIQUE CIRCUIT

CIRCUIT NUMBER	TITLE
017AE	EMITTER FOLLOWER
018AC	LOW COST VOLTAGE DISCRIMINATOR
018AD	PRECISION OPERATIONAL AMPLIFIER
018AE	PRECISION-VOLTAGE DISCRIMINATOR
018AF	HI GAIN AMPLIFIER
018AG	UNITY GAIN AMPLIFIER
018EA	LOW COST OPERATIONAL AMPLIFIER
018EG	VOLTAGE SWITCH
023EA	Z CUBED 1
025AB	ZOT CLAMP
025AC	HGA BUFFERS
031AB	VOLTAGE SWITCH
031EA	VOLTAGE SWITCH
032EA	CRF II
032EB	CRF III
032EC	CRF IV
061EA	G.C. II
061EB	RESISTORS-ANALOG
061EC	G.C. III
061ED	G.C. V
061EE	G.C. IV
061EF	G.C. I
061EG	G.C. VI
061EH	G.C. VII
061EJ	G.C. VIII
061EK	CRF I
061EM	INTEGRATOR-COMP
061EN	SWEEP PACK III
061EP	SWEEP PACK IV
062EB	CIRCLE FORMATION
062EC	CIRCLE FORMATION III
Q61AA	JUMPER BLOCK
S03AG	MULTIPLEX INTERFACE DRIVER-M4
S03AH	SELECT SAFETY
S03AI	AND-DOUBLE GATE
S03AJ	AND-HARPER GATE
S03AW	SPECIAL RECEIVER 750 OHM LOAD
S03SA	NEGATIVE OR DIODES
S03SC	CURRENT CONTROL AND EMITTER LOAD
S03SD	RESISTOR OR
S03SE	HIGH VOLTAGE AND
S03SF	AC AND
S03SG	AC AND
S03SJ	BINARY OUTPUT
S03SK	AC SET AND RESET
S03SL	MINUS AND
S03SM	NEGATIVE AND
S03SN	DUAL DIODE OR
S03SO	DUAL DIODE AND
S03SP	NON SYMETRICAL OR
S03SQ	AND-DOUBLE GATE
S05AB	U TO T CONVERTER
S05AC	L TO U CONVERTER
S05AE	MULTIPLEX INTERFACE RECEIVER
S05AG	SLT STANDARD INTERFACE DRIVER
S05AH	ISOLATING INVERTER
S05AJ	HI-GAIN AMPLIFIER
S05AK	UNITY GAIN AMPLIFIER
S05AM	FINAL AMPLIFIER
S05AO	DELAY LINE TERMINATOR
S05AR	MULTIPLEX INTERFACE DRIVER
S05AS	ISOLATING INVERTER NO LOAD
S05AT	U TO L CONVERTER
S05AU	T TO L CONVERTER
S05AW	5NS TO 30NS INTERFACE
S05AZ	INTERFACE TRANSMITTER
S05CA	INPUT AMPLIFIER DISC SPEED DETECTO
S05CB	OUTPUT AMPLIFIER DISC SPEED DETECT
S05CD	50 OHM CABLE DRIVER CIRCUIT
S05CE	S TO SLT LEVEL CONVERTER
S05CF	CABLE TERMINATOR CIRCUIT
S05CH	CONVERTER
S05CI	CLAMPING TERMATOR
S05CJ	TRANSMISSION LINE RECEIVER WITH GA
S05CM	SLT +3V TO +5V CONVERTER
S05EB	NAND SLT CONVERTER
S05EC	SLT NAND CONVERTER
S05SA	ISOLATING INVERTER WITH DELAY
S05SB	CONVERTER
S05SC	LEVEL CONVERTER
S06AB	INHIBIT TIMER
S06AC	MULTIPLEX INTERFACE DRIVER
S06AE	FIX STROBE EF
S06AK	TRANSMISSION LINE RECEIVER
S06AN	TRANSMISSION LINE RECEIVER W LD

CIRCUIT NUMBER	TITLE
S06AS	LOOP 2.0MC RD BUS TERM
S06AT	EMITTER FOLLOWER C13
S06AV	RESISTOR TERMINATORS 100 OHM
S06EA	NPL TERMINATION
S06SA	LINE DRIVER
S06SC	DATA LINE RECEIVER
S06SD	MULTIPLEX LINE DRIVER
S06SE	MULTIPLEX LINE DRIVER 3
S07AA	PREAMPLIFIER
S07AC	SENSE AMPLIFIER 1 PART A
S07AD	SENSE AMPLIFIER 1 PART B
S07AE	SENSE AMPLIFIER 2 PART A
S07AF	SENSE AMPLIFIER 2 PART B
S07AQ	PHOTOCELL AMPLIFIER
S07AS	SENSE AMPLIFIER
S07AT	SENSE AMP C13
S07CF	SYNC SENSE AMP
S07EA	PUNCH DETECTOR
S07ED	PREAMPLIFIER
S07EE	PREAMPLIFIER OUTPUT
S07LA	PHOTO TRANSISTOR SENSE AMPLIFIER
S07LB	PHOTO TRANSISTOR EF
S07SF	PRE-AMPLIFIER
S07SI	CYLINDER PULSE PRE-AMP
S07SJ	PREAMPLIFIER
S07SK	LOW LEVEL SOLAR CELL AMP
S07SL	READ AMPLIFIER
S07SM	PUNCH CHECK AMPLIFIER
S07SN	WRITE ERASE CURRENT DETECT
S07SO	PREAMPLIFIER
S07SP	DIFF-LIN AMP
S07SQ	HEAD DE-SELECT CKT
S07SS	INDEX PRIMARY AMP
S07SU	CYLINDER PREAMP
S07SV	DETENT PREAMP
S07SW	INDEX PREAMP
S07SX	READ AMPLIFIER 2
S07SZ	CE TEST AMP
S07TA	AMPLIFIER AND FILTER
S07TB	AMP-DIFFERENTIATOR
S07TE	PRE AMPLIFIER
S07TF	TACH BUFFER AND FILTER
S07TG	POWER AMPLIFIER
S10AF	25MA RELAY DRIVER
S10AG	LOOP 2.0MC VFO CLAMP DRIVER
S10AH	37MA RELAY DRIVER
S10SB	GATE CONTROL
S10SC	INVERTER WITH LOAD
S10SE	AI WITH LOAD
S10SH	EMITTER AMPLIFIER
S10SI	INVERTER WITH LOAD
S10SJ	INVERTER POWER
S10SK	INVERTER UNLOADED
S10SL	INVERTER
S10SM	INVERTER CLAMP
S10SN	INVERTER
S10SO	INVERTER
S10SP	POWER INVERTER
S10SQ	INVERTER
S11AE	EMITTER FOLLOWER
S11AG	DELAY LINE DRIVER
S11AL	DATA CONCENTRATOR RDU
S11AM	OSCILLATOR AMP
S11EA	DELAY LINE DRIVER
S11SA	EMITTER FOLLOWER - V.C.
S11SB	EMITTER FOLLOWER HEAD LOAD
S15AE	1.3 AMP DRIVER
S15AG	DRIVE FOR 1.3AMP DRIVER
S15AH	100 MA HAMMER DRIVER
S15AI	Y-SELECT

CIRCUIT NUMBER	TITLE
S15AK	300MA DRIVER
S15AQ	PROLAY DRIVER
S15AR	RELAY DRIVER
S15AW	1.7A SOLENOID DRIVER
S15AZ	DATA CONCENTRATOR 2 RDM
S15CA	650 MA SOLENOID DRIVER
S15EB	400 MA DRIVER
S15EC	DRIVER FOR 2.2 A DRIVER
S15ED	DRIVER FOR 2.2 A DRIVER
S15EF	2.2 A DRIVER
S15EJ	R/W DRIVER
S15LA	CLUTCH DRIVER
S15LB	BRAKE DRIVER
S15LC	48V 0.1AMP RELAY DRIVER
S15SA	INHIBIT DRIVER
S15SF	STROBE DRIVER
S15SG	DRIVER GATE CONTROL
S15SH	1AMP 8MS SOLENOID DRIVER
S15SL	1 AMP PNP DRIVER
S15SM	1 AMP NPN DRIVER
S15SN	2.5 AMP DRIVER 1
S15SO	.5 AMP NPN DRIVER
S15SP	2.5 AMP DRIVER 2
S15SQ	HIGH CURRENT SWITCH I
S15ST	INHIBIT DRIVER
S15SV	WRITE DRIVER INVERTER
S15SX	POWER TRANSISTOR
S15SY	POWER TRANSISTOR 257
S15SZ	POWER INVERTER HEAD LOAD
S16AE	Z DRIVER
S16AG	TITLE R/W DRIVER
S16AH	CORE DRIVER-INHIBIT
S16AI	X-Y CORE DRIVER
S16AJ	CURRENT SWITCH-CORE
S16AK	SWITCH DRIVER
S16AL	WRITE DRIVER
S16AT	DIFFERENTIATOR
S16AU	AC COUPLED AMPLIFIER
S16CH	READ AMP FILTER
S16CJ	STROBE DRIVER SP4
S16CK	SINGLE SHOT CONTROL
S16CL	ARRAY DRIVER C13
S16CM	WRITE DRIVER
S16EA	Z-DRIVER
S16EB	TERMINATOR GATE
S16EC	INHIBIT TIMER
S16SA	X-Y DRIVER
S16SB	X-Y DRIVER
S16SC	ERASE DRIVER
S16SD	WRITE DRIVER
S16SE	WRITE CURRENT SOURCE
S16SG	WRITE HEAD SELECT
S20SA	TRIGGER
S21AA	50-60 PULSE PER SECOND
S21AF	PULSE FORMER SINGLE SHOT
S21AI	VAR. FREQ. SINGLE SHOT
S21SB	MAGNETIC CB SHAPER
S21SC	PRECISION TIMER
S21SD	2 SECOND TIMER
S21SE	SINGLE SHOT 60NS
S21SF	SINGLE SHOT 165 USEC
S21SG	SINGLE SHOT 800 USEC
S22AA	4 MC OSCILLATOR
S22AE	5KC XTAL OSCILLATOR
S22AK	500KC XTAL OSCILLATOR
S22AL	720KC XTAL OSCILLATOR
S22AS	500KC GATED OSCILLATOR
S22AT	700KC GATED OSCILLATOR
S22AZ	5 WAY PLO
S22CH	4 MC XTAL OSCILLATOR

CIRCUIT NUMBER	TITLE
S22CI	1.36 MC CRYSTAL OSC
S22CJ	1.496 MC CRYSTAL OSC
S22CK	3.2648KC XTAL OSCILLATOR
S22CL	4.004KC XTAL OSCILLATOR
S22CM	4.84KC XTAL OSCILLATOR
S22CN	5.0063KC XTAL OSCILLATOR
S22CO	SLT 5.9176KC XTAL OSCILLATOR
S22CP	1460 MCS OSCILLATOR
S22CU	CRYSTAL OSCILLATOR
S22CV	4.0 MC CRYSTAL OSCILLATOR
S22CW	3.3KC XTAL OSCILLATOR
S22CX	4.4KC XTAL OSCILLATOR
S22DE	2.0 K.C CRYSTAL OSCILLATOR
S22LA	4.26 KC XTAL OSCILLATOR
S22LB	5.824 KC XTAL OSCILLATOR
S22LC	3.64 KC XTAL OSCILLATOR
S22LE	6.4 KC XTAL OSCILLATOR
S22LF	4.8 KC XTAL OSCILLATOR
S22LG	7.04 KC XTAL OSCILLATOR
S22LH	9.6 KC XTAL OSCILLATOR
S22SA	185 KC OSCILLATOR
S22SC	400 CPS OSCILLATOR
S25AA	Z CLAMP
S25AB	GATE CLAMP
S25AC	REFERENCE VOLTAGE
S25AD	REFERENCE VOLTAGE
S25AE	RW DRIVER CLAMP
S25AF	LOOP 2.0MC AMP-LIMITER
S25AH	9V REGULATOR
S25AI	REGULATOR 9V
S25AJ	13V CLAMP
S25AK	VOLTAGE REGULATOR C13
S25AL	VOLTAGE REGULATOR
S25AM	VOLTAGE CLAMP +0.125 V DC
S25AT	CLAMP DIODES +3V
S25CF	SINGLE SHOT REF
S25EA	VOLTAGE DIVIDER
S25EC	+12 CCROS DRIVER SUPPLY
S25EB	CAPACITOR COUPLING NETWORK
S25EE	DIODE
S25EF	R/W DRIVER CLAMP
S25LA	POSITIVE TRANSITION DETECTOR
S25SA	VOLTAGE SET FOR SAR
S25SB	REFERENCE TEMPERATURE LEVEL
S25SD	DRIVER CONTROL
S25SE	DIODE CLAMP
S25SF	CURRENT SOURCE
S25SG	POWER REGULATOR 20V
S25SH	VOLTAGE REFERENCE 50 MV
S25SI	VOLTAGE REFERENCE 5 V
S25SL	VOLTAGE REGULATOR
S25SM	POWER REGULATOR 60V
S25SN	LEVEL SETTER
S25SO	OVER DRIVEN AMPLIFIER
S25SP	VOLTAGE REGULATION 36 OHM
S25SQ	RECTIFIER
S32AB	GATE
S32AC	TERMINATOR GATE
S32AE	GATE
S32AF	LOOP 2.0MC LWR GATE
S32AG	LOOP 2.0MC LINEAR GATE
S32EB	GATE TRANSISTORS WITH CLAMP
S32EC	GATE TRANSISTORS WITH CLAMP
S40AB	SECTOR SWITCH
S40AC	SPEED DETECTOR
S40AD	INDEX GENERATOR
S40AG	LOOP 2.0MC REF CLOCK GEN
S40AJ	LOOP 2.0MC PEAK PULSER
S40AM	LOOP 2.0MC SQUELCH DRIVER
S40AO	FREQUENCY DETECTOR DISC SPEED DET

CIRCUIT NUMBER	TITLE
S40EA	SWITCH NETWORK
S40EB	TEMP SENSING NETWORK
S40SA	POWER SUPPLY 28V
S40SB	POWER SUPPLY 28V
S40SD	SENSE LEVEL VOLTAGE
S40SE	REF VOLTAGE
S40SF	+4V SPECIAL VOLTAGE
S40SH	LEVEL SETTING
S40SI	POWER SUPPLY SAFETY
S40SJ	NULL BIAS
S40SK	VARIABLE CURRENT SOURCE
S40SL	DC SAFETY
S40SM	AC SAFETY
S40SO	VOLTAGE TO FREQUENCY CONVERTER
S40SP	LEVEL INDICATOR MINUS
S40SQ	LEVEL INDICATOR PLUS
S40SR	DETECTOR AMPLIFIER
S40SS	SINGLE BRK FUNC GENERATOR
S40ST	FAIL SAFE BLOCKING VALVE DET
S40SV	REFERENCE VOLTAGE
S40SW	ZERO S DETECTOR
S40SX	GAP SENSOR
S40SY	DETECTOR
S40SZ	RAMP GENERATOR
S40TA	CAP SENSOR
S40TB	TEST REFERENCE CIRCUIT
S40TE	0.45 AMP DRIVER
S40TF	BALANCE NETWORK
S40TG	LEVEL DETECTOR
S40TH	VOICE COIL AMPLIFIER
S40TL	DETECTOR CIRCUIT
S40TM	WRITE SELECT
S40TN	A C UNSAFE
S40TO	VOLT TO HIGH FREQ CONV
S40TP	ZERO S DETECTOR (0.438 MBS)
S40TQ	GAP SENSOR (0.438 MBS)
S40TR	DETECTOR 0.438MBS
S40TS	RAMP GENERATOR 0.438MBS
S40TW	WRITE SAFETY LATCH
S40TX	SCHMIDT TRIGGER
S40TY	TRANSDUCER DETECTOR
S40TZ	LEVEL DETECTOR
S45AB	5 TO 25 NS DELAY LINE
S45AC	TAPPED DELAY LINE
S45AD	5-125NS DELAY LINE
S45AE	DELAY LINE TERMINATOR W/O-L
S45AH	ELAPSED TIME METER DISPLAY
S45AK	DELAY LINE 0-125
S45AN	VARIABLE DELAY .2 SEC TO 2.0 SEC
S45EA	350 NS DELAY LINE
S45EB	3 TO 8.6 SECOND TIME OUT
S45EC	VARIABLE TIME DELAY 5-125NS
S45SB	500NS DELAY LINE
S45SC	DELAY LINE 1MS
S45SD	DELAY 90 SEC
S55AA	40 MA INDICATOR DRIVER
S55AD	15 MA INDICATOR NETWORK
S55AH	LAMP DRIVER-ID 2
S55EA	40 MA LAMP RESISTOR NETWORK
S55EB	40 MA INDICATOR DRIVER
S55EG	SCR SIGNAL ENTRY RESISTOR
S55EH	SCR INDICATOR DRIVER
S55SB	40 MA INDICATOR NETWORK
S55SC	250 MA DRIVER
S55SD	LAMP DRIVER
S60AB	CAM INTEGRATOR
S60AC	CAPACITOR NETWORK
S60AH	SINGLE SHOT FILTER
S60AR	INTEGRATOR
S60BA	JUMPER CARD

CIRCUIT NUMBER	TITLE
S60EA	FILTER 25 KC
S60EC	TUNGSTEN CONTACT NETWORK
S60FE	DRIVER FILTER
S60SA	RESISTOR EMITTER LOAD
S60SB	COMPENSATION NETWORK
S60SC	DISK SPEED DETECTOR
S60SD	DECOUPLING CAPACITORS
S60SE	VELOCITY INTEGRATOR
S60SF	LINE FILTER
S60SG	FILTER
S60SH	INTEGRATOR 07 PERCENT SPEED
S60SI	INTEGRATOR LESS THAN 98 PERCENT SP
S61AD	MULTIPLEX TERMINATING NETWORK
S61AF	JUMPER
S61AJ	STANDARD INTERFACE TERMINATOR
S61AM	DISCRETE CAPACITOR
S61AN	2.7K RESISTOR 1/4 W
S61AO	TRANSMISSION LINE RECEIVER
S61AP	TYPE 6V DIODE
S61AR	TERMINATING RESISTOR-100 OHM
S61AU	INTEGRATOR
S61AX	39K RESISTOR
S61AY	PLUGGABLE SWITCH
S61AZ	REED RELAY SUPPRESSION
S61BE	JUMPER
S61BG	200 OHM RESISTOR TO +3V
S61CA	220 OHM RESISTOR
S61CC	TYPE DD DIODE CLAMP
S61CG	THERMISTOR
S61CH	POTENTIOMETER
S61CM	DEC CAPACITOR +3V
S61CN	DEC CAPACITOR -3V
S61CO	DEC CAPACITOR +66V
S61CP	DECOUPLING CAPACITOR TO +12V
S61CQ	DEC CAPACITOR -12V
S61CR	ISOLATING RESISTOR-1D2
S61CS	200 OHM RESISTOR TO +6V
S61CT	DELAY CAPACITOR
S61CU	SPECIAL DN LVL IND RESISTOR
S61CW	TYPE AM DIODE TO -12V
S61CX	22 MEG OHM RESISTOR
S61CY	THERMOSWITCH
S61CZ	330 OHM RESISTOR
S61DA	AC INPUT
S61DB	36 OHM RESISTOR
S61DC	TERMINATOR C13
S61DD	5 UF CAPACITOR NP
S61DE	10 UF COUPLING CAPACITOR
S61DF	2.0 KC CRYSTAL
S61DG	DECOUPLING CAPACITOR TO GROUND
S61DH	1.0 UH CHOKE
S61DI	ALS DIODE
S61DJ	CAPACITOR 680PF 5 PER CENT
S61DK	3K RESISTOR
S61DL	MAGNETIC HEAD
S61DM	SOLAR CELL
S61DN	.1UFD DELAY CAPACITOR
S61DQ	AM DIODE
S61DR	RESISTOR 200 OHM
S61DT	CAPACITOR .02UF
S61DW	6.8UFD DECOUPLING CAPACITOR
S61DX	LOAD RESISTOR 95 OHM
S61EA	CAPACITORS I
S61EB	CAPACITORS II
S61EE	PLUGGABLE JUMPERS
S61EK	LOAD RESISTOR -52 OHM
S61EM	100 OHM RESISTOR LOAD TO GND
S61EQ	1 K RESITOR TO -3V
S61IG	95 OHM TERMINATING RESISTOR TO GRD
S61II	DEC CAPACITOR +12V

CIRCUIT NUMBER	TITLE
S61LA	1K RESISTOR
S61SO	DIODE MATRIX
S61SA	VERNIER RESISTANCE
S61SC	RESISTOR 14.3 OHM
S61SE	5.1 OHM RESISTOR
S61SF	10 OHM RESISTOR
S61SG	POWER SEQUENCE BLOCK
S61SH	EMITTER LOAD
S61SI	DIODE SUPPRESSION
S61SJ	18 OHM RESISTOR
S61SK	COMMON BAR JUMPER
S61SL	READ-WRITE SELECTION MATRIX
S61SM	PROGRAM CAP HUB
S61SP	DIODE MATRIX
S61SQ	36 OHM 1 WATT RESISTOR
S61SR	DIODE SUPPRESSION
S61ST	RESISTOR 2.49K
S61SU	TRACK DIVIDER 2
S61SW	RESISTOR SAFETY
S61SX	CURRENT FEEDING
S61SZ	RESISTOR 21 OHM
S61TA	AC TERMINATOR
S61TB	DEOUPLING CAPACITOR
S61TC	DIODE MATRIX
S61TD	VOLTAGE REGULATOR
S61TE	1.8K RESISTOR
S61TF	RESISTOR-100 OHM
S61TG	2.4K RESISTOR
S61TH	RESISTOR 1100 OHM 1/2W
S61TJ	RESISTOR - 1.5K 1/2W 5 PER CENT
S61TK	2K RESISTOR
S61TL	HEAD PLUG-13RK
S61TM	RESISTOR 220 OHM
S61TN	RESISTOR 62 OHM
S61TO	RESISTOR 130 OHM
S61TP	RESISTOR 2 OHM
S61TQ	DIODE CLAMP
S61TR	RESISTOR 25 OHM
S61TS	RESISTOR 1 OHM
S61TT	RESISTOR 825 OHM
S61TU	DIODE SUPPRESSION
S61TV	RESISTOR 1K
S61UF	DIODE AAS
S63AA	4-POSITION REED RELAY
S63AB	6-POSITION REED RLY
S63AC	COIL 1-POLE REED RELAY
S63AD	COIL 6- POLE REED RELAY
S63AE	RELAY POINT REED
S63AK	REED RELAY COIL OR 2N/O 2N/C ASSM
S63AL	REED RELAY 2N/O 2N/C
S63AM	REED RELAY HOLD WINDING
S63AN	REED RELAY PICK WINDING
S63AQ	6 N/O P AND H REED RELAY
S63AS	4 N/O P AND H REED RELAY
S63AU	1 POSITION REED RELAY
S63AW	TELEGRAPH RELAY - RECEIVE
S63AY	TELEGRAPH RELAY - TRANSMIT
S63EA	REED POINT-NORMALLY OPEN
S63EB	REED POINT-NORMALLY CLOSED
S63EC	REED RELAY ASSM 2N/O 2N/C
S63ED	REED RELAY ASSM 6V
S63EF	6V COIL FOR REED RELAY
S63EG	REED POINT-NORMALLY OPEN
S63EH	REED POINT-NORMALLY CLOSED
S63SA	COIL-2 POLE REED RELAY
S63SB	COIL 2-POLE REED RELAY
S63SC	COIL 2-POLE REED RELAY
S63SD	48V REED RELAY COIL
S63SE	2 POINT - REED - RELAY
S63SF	4 POINT - REED - RELAY

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CIRCUIT NUMBER	TITLE
S63SG	1-POINT REED RELAY
S63SH	4 POINT RELAY
T03AA	AND INVERT NO LOAD
T03AB	AND INVERT-750 OHM LOAD
T03AC	AND
T03AC	AND
T03AD	OR INVERT-NO LOAD
T03AE	OR INVERT-750 OHM LOAD
T03AF	AND POWER INVERT NO LOAD
T03AI	EXCLUSIVE OR W/LOAD
T03AJ	AND-PWR INVERT 300 OHM LOAD
T03AK	EXCLUSIVE OR LATCH
T03AL	8 WAY EXCLUSIVE OR
T03AM	4 WAY EXCLUSIVE OR
T03AN	7 WAY API-NO LOAD
T03AO	7 WAY API-300 OHM LOAD
T03AP	EXCLUSIVE OR-NO LOAD
T03AQ	AND FOR MULTIPLEX INTERFACE DRIVE
T03AR	MULTIPLEX INTERFACE DRIVE
T03AS	AND-1K
T03AX	AND EXT MULTIPLEX INTERFACE DR
T03BF	MINUS OR INVERT UNLOADED
T03BN	GATE
T03BO	MINUS OR INVERT LOADED
T03BP	DECODER
T03BQ	SENSE LATCH AND
T03BR	SENSE STROBE AND
T03BS	SENSE AMPL AND
T03BT	EXTENDED API WITHOUT LOAD
T03BV	EXTENDED API
T03BW	EXTENDED API 270 OHM +6
T03BX	SELECTOR
T03BY	GATE DECODER
T03CC	Y-SELECT LOGIC
T03CD	Y-SELECT 2
T03CE	AND GATE
T03CG	AND FOR SENSE AMP LCM
T03CI	POSITIVE OR DIODES
T03CK	TITLE WRITE DRIVER
T03CO	MULTIPLEX RECEIVER
T03CP	OR-INVERT
T03EF	AND FOR API
T03EH	OR INVERT NO LOAD
T03EI	OR INVERT WITH LOAD COMBINED LOGIC
T03EL	AND-OR INVERT NO LOAD
T03EM	AND-OR INVERT WITH LOAD
T03EN	AND-FOR AI
T03JB	SENSE AMPLIFIER AND
T03JC	AND - LATCH CONTROL
T03JD	AND
T03JE	AND
T03JF	OR
T03SA	AND
T03SF	OR INVERTER
T03SG	AND INVERTER
T03SH	OR DIODES
T03SI	AND INVERTER WITH LOAD
T03SJ	API WITH LOAD
T03SK	SPECIAL OR CIRCUIT
T03SL	AND INVERT
T03SN	POSITIVE AND WITH DELAY
T03SV	REPLACED BY T03SI
T03TB	POSANDEL
T03TC	AOI WITH EXTEND
T03TD	MINUS AND
T03TE	AND EMITTER FOLLOWER
T03TG	DIODE OR
T03TH	STEP MODE OR
T03TI	STEP MODE AND
T03TJ	SEPARATE COMPONENT AI

CIRCUIT NUMBER	TITLE
T03TK	READ SELECT
T03TL	OR INVERTER
T03TM	INVERTER
T03VA	AOI-GROUPING-NO LOAD
T03VB	AOI-GROUPING-W/LOAD
T03VC	MULTIPLEX DRIVER GROUPING-NO LOAD
T05AA	INVERT DIRECT CPLD NO LOAD
T05AB	INVERTER DIRECT CPLD.-350 OHM LOAD
T05AF	NPL FINAL AMP HI + LO ACCEPT DRIVE
T05AJ	TERMINATING EIA TO SLT CONVERTER
T05AL	TRANSLATE BLOCK
T05AM	WRITE DRIVER CHECK
T05AO	45 MA TRANSMISSION LINE DRIVER
T05AP	INTERLOCK CIRCUIT TERMINATOR
T05AQ	INVERTER
T05BG	DELAY LINE DRIVER
T05BI	DRIVER STROBE
T05BJ	LAMP TEST CCT FOR DLID
T05BK	GATE
T05BM	LATCH STAGE I
T05BN	INVERTER
T05BO	GATE INVERT
T05EA	FINAL AMPLIFIER
T05SA	FORMAT X-READ SELECT
T05SB	DATA X-READ SELECT
T05SC	DIRECT COUPLED INVERTER
T05SD	ISOLATING INVERTER DISCRETE
T05SE	CONVERTER
T05SG	MAGNETIC CB SHAPER
T06AA	LINE SENSE AMP LSA
T06AE	CORE-DRIVER
T06AG	MULTIPLEX LINE TERMINATOR
T06AH	MULTIPLEX INTERFACE DRIVER
T06AI	SLT TO E1A CONVERT LINE DRIVER
T06AJ	DIRECT COUPLED INVERTER DRIVER
T06AL	STD INTERFACE LINE DRIVER
T06AM	GATED LINE INTRFC TERM
T06AN	STD INTERFACE LINE TERMINATOR
T06AR	HIGH POWER DRIVER - 100 OHM LOAD
T06AY	PHASE DETECTOR
T06AZ	LINE TERMINATOR AND GATE
T06BC	LINE SENSING AMPLIFIER
T06BD	DELAY LINE SENSING AMPLIFIER
T06CE	SENSE AMP TERM C13
T06CF	EMITTER FOLLOWER C13
T06CG	LINE REPEATER
T06CH	LINE TERMINATOR AND GATE II
T06CI	MULTIPLEX LINE DRIVER
T06CJ	LINE DRIVER
T07AD	NPL FINAL AMP PEAK DETECTOR
T07AG	C9 SENSE LATCH 2
T07AH	C9 SENSE AMP 1
T07AI	SENSE AMPLIFIER
T07AJ	PRE AMPLIFIER AND FILTER
T07AK	FILTER
T07AS	SENSE AMPLIFIER REFERENCE FLYERLCM
T07AT	NPL FINAL AMP INPUT TERM
T07AZ	MAGNETIC HEAD SENSE AMPLIFIER
T07BB	PARAPHASE AMP
T07BC	SENSE AMPLIFIER
T07BD	CCROS RHO SENSE AMPLIFIER
T07BE	CR SENSE AMPLIFIER
T07CA	PROBE AMPLIFIER
T07CB	PROBE AMPLIFIER
T07CF	SENSE AMP
T07CH	SENSE AMPLIFIER
T07CK	SENSE AMPLIFIER
T07CM	MOTION INTEGRATOR II
T07CN	DETECTOR AMPLIFIER 2
T07SA	SUMMING AMP INPUT

CIRCUIT NUMBER	TITLE
T07SB	FUNCTION GENERATOR INPUT
T07SC	LOW LEVEL POSITION AMP
T07SD	LOW LEVEL VELOCITY AMP
T07SG	FUNCTION GENERATOR OUTPUT
T07SH	INNER FUNCTION GENERATOR
T07SI	VELOCITY ARRIVAL BUFFER
T07SJ	TACHOMETER BUFFER AND FILTER
T07SK	COMPLEX ZERO INPUT
T07SL	POSITION ARRIVAL BUFFER
T07SM	CLASS A POWER AMPLIFIER
T07SN	2 SECOND CIRCUIT INPUT
T07SP	SOLAR CELL AMPLIFIER
T07SQ	CYLINDER DETECTOR CIRCUIT
T07SR	INDEX DETECTOR CIRCUIT
T07SS	READ AMPLIFIER 1
T07ST	WRITE AMPLIFIER 1
T07SU	BLOCKING VALVE DET INPUT
T07SW	DETENT DETECTOR CIRCUIT
T07SX	PUNCH CHECK AMPLIFIER
T10BB	SENSE AMPLIFIER
T10BC	DRIVER SUPPLY
T10BE	FORCE CARD PRINT INVERTER
T10BF	LATCH RESET DRIVER 1
T10BG	INVERTER DRIVER
T10BH	GATED INVERTED DRIVER
T10BI	LATCH RESET DRIVER 2
T10EA	HARPER GATE DRIVER
T10SA	CURRENT CONTROL
T10SC	AMPLIFIER-STROBE DRIVER
T10SF	TRIGGER DRIVER
T10SI	INVERTER
T10SL	INVERTER
T10SN	INVERTER-CLAMPED
T10SP	INTEGRATOR SWITCH
T10SQ	INVERTER SPEC
T10SR	ISOLATING INV WITH FILTER
T10SS	HIGH POWER INVERTER
T11AB	SA GATE DRIVER
T11BH	SENSE STROBE FOLLOWER
T11BI	EMITTER FOLLOWER
T11BJ	DRIVER
T11BK	RESET DRIVER
T11BL	GATE DRIVER
T11BO	SENSE AMP STROBE DRIVER
T11BP	EMITTER FOLLOWER
T11BQ	EMITTER FOLLOWER
T11BR	EMITTER FOLLOWER
T11BS	EMITTER FOLLOWER
T11BT	EMITTER FOLLOWER
T11BU	EMITTER FOLLOWER
T11BW	EMITTER FOLLOWER
T11EA	STROBE DRIVER
T11EC	CCROS DECODE DRIVER
T11ED	CCROS EMITTER GATE
T11EE	CCROSS GATED DRIVER
T11SA	AND EMITTER FOLLOWER
T15AA	HIGH POWER DRIVER - 175 OHM LOAD
T15AE	HIGH POWER DRIVER-NO LOAD
T15AJ	SOLENOID DRIVER, 1.5A
T15AM	1 POLE REED RELAY DR
T15AN	REED RELAY DRIVER
T15AO	STROBE DRIVER
T15AQ	XY GATE OR INHIBIT DRIVER
T15AT	4 AMP DRIVER NPL
T15AY	HIGH POWER DRIVE-COMBINED LOGIC
T15AZ	434 MA RELAY DRIVER
T15BC	GATE STROBE
T15BD	UP LEVEL INDICATOR DRIVER
T15BE	SENSE STROBE DRIVER
T15BF	DRIVER SUPPLY AMP

CIRCUIT NUMBER	TITLE
T15BG P	DRIVER SUPPLY OUTPUT
T15BH P	SENSE STROBE DRIVER 2
T15BI P	DRIVER SUPPLY AMP 2
T15BJ E	DRIVER DECODER
T15BK P	HIGH POWER INVERT
T15EF P	SONIC LINE DRIVER
T15SH P	BOOTSTRAP AMPLIFIER
T15SJ P	INVERTER
T15SK P	HIGH POWER
T15SL P	450 MA DRIVER
T15SN P	2.5 AMP DRIVER
T16AF P	S9-WRITE DRIVER
T16AH P	S9-READ DRIVER
T16AI P	A WORD GATE LCM
T16AJ P	SWITCH GATE
T16AK P	A GROUP AND DRIVER
T16AL P	WORD GATE
T16AM E	B SWITCH GATE-LCM
T16AN P	A B GROUP AND LCM
T16AO E	A WORD DRIVER
T16AP P	A GROUP AND CONVERTER LCM
T16AQ P	A GROUP PULSE GEN LCS
T16AT P	WRITE DRIVER
T16AU P	WRITE SAFETY
T16AY E	STROBE DRIVER LCM
T16BB T	DOWN LEVEL INDICATOR DRIVER
T16BC P	CLOCK LINE DRIVER
T16CA P	A GROUP DRIVER- LCS
T16CB E	A WD GATE DRIVER LOAD RESISTOR LCM
T16CC E	B WD GATE DRIVER LOAD RESISTOR LCM
T16CF P	A SWITCH GATE DRIVER- LCM
T16CG P	B SWITCH GATE DRIVER LCM
T16CH P	A WORD GATE DRIVER-LCS
T16CI P	B WORD GATE DRIVER-LCM
T16CJ P	STRIP HIGH DETECTOR
T16CK E	HEAD PRE-AMP
T16CL E	A SHUNT CLIPPER LCM
T16CN E	A COMPENSATION AMPLIFIER LCM
T16CO E	B COMPENSATION AMPLIFIER
T16CT P	BIT GATE CONVERTER LCM
T16CU P	B GROUP AND DRIVER- LCS
T16CW P	B GROUP DRIVER LCS
T16CX P	B GROUP AND CONVERTER LCS
T16CY E	BIT DRIVER
T16CZ P	BIT DRIVER LCM
T16DA P	A EMITTER CLAMP- LCM
T16DB P	B EMITTER CLAMP
T16DC P	A REFERENCE CLAMP LCM
T16DD E	B REFERENCE CLAMP
T16DE E	B WORD DRIVER LCM
T16DG P	S-9 BIT DRIVER
T16DK P	INVERTER FOR C E F
T16DL P	COMP EMITTER FOLLOWER
T16DN E	CURRENT DRIVER
T16DO E	TIMING SWITCH A
T16DP E	A CURRENT GATE
T16DQ E	B CURRENT GATE
T16DR E	VFC DENSITY SWITCHES
T16DS E	WRITE CURRENT CONTROL
T16DT P	SP4 BIT DRIVER
T16DU P	SP4 WRITE DRIVER
T16DW E	LCS BUFFER AND READ BIT RESISTOR
T16DY E	LCS DETECTOR
T16DZ E	LCS FINAL AMPLIFIER
T16IA E	LCS AMPLIFIER INVERTER
T16IB E	LCM BIT GATE PULL DOWN
T16IC E	TIMING SWITCH B
T16SA P	PHOTO TRANSISTOR AMPLIFIER
T20AB B	400 KC TRIGGER
T20AD T	AC TRIGGER NO. 2

CIRCUIT NUMBER	TITLE
T20AE	HARPER GATE
T20AF	HARPER GATE
T20AG	INTEGRATOR-STROBE
T20AH	S9-LATCH
T20AI	LOGIC TRIGGER
T20AM	AC TRIGGER
T20AR	GATED AC TRIGGER
T20AT	GATED AC TRIGGER
T20AW	GATED AC TRIGGER 2
T20BB	CCROSS SENSE LATCH
T20BC	SPECIAL LATCH
T20BD	SPECIAL LATCH
T20EB	400 KC TRIGGER
T20SA	WRITE TRIGGER
T20SC	MULTIPLE INPUT TRIGGER
T20SD	WRITE TRIGGER
T20SE	TRIGGER 2.1
T21AH	NPL FINAL AMP PULSE SHAPER + DR
T21AN	LEADING EDGE TIME DELAY
T21AP	B GROUP PULSE GENERATOR PNP-LCS
T21AR	HALF PERIOD GEN
T21AW	SINGLE SHOT-VARIABLE
T21AZ	VARIABLE SINGLE SHOT
T21CC	VARIABLE SINGLE SHOT
T21CF	VARIABLE SINGLE SHOT
T21CH	SINGLE SHOT-FIXED
T21CI	SINGLE SHOT 410 NS-NF
T21CK	250 NS SINGLE SHOT
T21CM	FIXED SINGLE SHOT 1
T21CN	PRECISE SINGLE SHOT ADJ
T21CT	VARIABLE SINGLE SHOT
T21CU	HALF PERIOD GEN II
T21CW	SINGLE SHOT SSB(VAR) 78NS-68.5US
T21SC	SINGLE SHOT 1400 NS
T21SD	SINGLE SHOT 185 NS
T21SE	SINGLE SHOT WITH DELAY
T21SH	500 NS SINGLE SHOT
T21SJ	7MS SINGLE SHOT
T21SK	SINGLE SHOT 600 MS
T21SL	300MS SINGLE SHOT
T21SS	SINGLE SHOT
T21ST	SINGLE SHOT 1
T21SU	SINGLE SHOT 2
T21SV	1060 NS SINGLE SHOT
T21SW	300 NS SINGLE SHOT
T21SX	1100 NS SINGLE SHOT
T21SY	VARIABLE SINGLE SHOT
T21TA	110 NS SINGLE SHOT
T21TB	VARIABLE-SINGLE-SHOT
T21TC	2 MS SINGLE SHOT
T21TD	10 MS SINGLE SHOT
T21TE	800NS SS
T21TG	15 MS SS
T21TJ	100 NS SINGLE SHOT
T21TK	500 NS SINGLE SHOT
T22AB	2KC OSCILLATOR
T22AC	20KC OSCILLATOR
T22AF	1.667 MC CRYSTAL OSCILLATOR
T22AH	2.4MC XTAL OSC
T22BC	CLOCK OSCILLATOR 3.2 MC/S
T22BD	170 KC/S OSCILLATOR
T22EA	2.0MC CRYSTAL OSCILLATOR
T22EB	3 PER CENT 117.2 CPS OSCILLATOR
T22SB	2 MC OSCILLATOR
T22SC	4 MC CRYSTAL OSCILLATOR
T22SD	CLOCK 1.44 MC
T22SE	2.5MC XTAL OSCILLATOR
T22SG	GATED MULTIVIBRATOR
T25AA	NPL FINAL AMP LOW ACCEPT CLIP
T25AB	NPL FINAL AMP HI ACCEPT CLIP

CIRCUIT NUMBER	TITLE
T25AD	REGULATOR 28.5V
T25AG	SENSE LEVEL SET
T25AH	VOLTAGE REFERENCE
T25AL	AB GROUND CLAMP- LCM
T25AM	BASE CLAMP C13
T25BB	SENSE CLAMP PWR AMPL
T25BC	SENSE CLAMP
T25BD	+3V CLAMP
T25BE	SENSE CLAMP PWR AMP
T25BF	SENSE CLAMP PWR AMP
T25BG	OVER VOLTAGE LIMITER
T25EE	SIGNAL DETECTOR
T25EF	GATE CLAMP
T25EH	DELAY LINE DETECTOR
T25SB	CURRENT CONTROL
T25SC	CURRENT CONTROL
T25SD	OFFSET VOLTAGE
T26AA	NPL FINAL AMP LO ACCEPT CLIP
T26AB	NPL FINAL AMP HI ACCEPT CLIP
T27BB	SENSE CLAMP POWER AMP
T27BC	SENSE CLAMP
T27BD	+3 V CLAMP
T30BC	PUNCH MAGNET DRIVER GROUPING
T31BB	TROM GATE GROUPING
T31BC	CHANGE OVER SWITCH
T31BD	3-WAY CHANGE OVER
T31BE	LAMP TEST SWITCH
T32AF	NPL FINAL AMP GATE
T32AH	CORE-GATE
T32BA	LINE RECEIVER GROUPING
T32BD	THRESHOLD GATE
T32BE	LATCH STAGE II
T32BF	GATE
T32EB	TRIGGER GATE
T32SA	ARRIVAL DETECTOR
T32SC	RESISTOR-CAPACITOR AND GATE
T32SF	HOME DRIVE AND
T32SG	INTEGRATOR RESET
T32SH	CE RUN
T32SI	DETENT DRIVER
T40AA	NPL FINAL AMP RECT + CHAN SEP
T40AB	NPL FINAL AMP 9V ZENER SUPPLY
T40AE	LIMIT AMPLIFIER
T40AF	INDEX PULSE AMPLIFIER
T40AG	FORMAT SELECT
T40AH	8 POSITION CLOCK
T40AI	6 POSITION COUNTER
T40AJ	DIFFERENTIAL AMP FOR SENSE AMP LCM
T40AK	VFC PULSER
T40AL	VARIABLE FREQUENCY CLOCK
T40AN	VARIABLE CURRENT SOURCE
T40AP	SA GATE GENERATOR
T40AR	VARIABLE FREQUENCY CLOCK 2
T40BB	BUFFERED SENSE LATCH
T40SA	CONSTANT CURRENT LAMP SUPPLY
T40SB	CURRENT SOURCE
T40SC	SUMMING AMP CURRENT SOURCE
T40SD	WRITE BYPASS
T40SE	DIFFERENTIATOR
T40SG	POWER SUPPLY SAFETY +6 V
T40SH	BLOCKING VALVE DET. OUTPUT
T40SI	SINGLE SHOT 750 USEC
T40SJ	CURRENT CONTROL
T40SK	SENSE LEVEL
T40SL	REFERENCE VOLTAGE
T45AC	125 NS DELAY LINE
T45AF	15 SECOND DELAY
T45AG	250 NSEC TAPPED DELAY LINE
T45AH	500 NSEC DELAY LINE TAPPED
T45AL	MOTOR DELAY CIRCUIT

CIRCUIT NUMBER	TITLE
T45BB	VARIABLE DELAY LINE
T45BC	CLOCK DELAY
T45EC	200 NS DELAY CIRCUIT
T45ED	350 NS DELAY LINE
T45LC	RC DELAY CIRCUIT 250 NS
T45LD	RC DELAY CIRCUIT 440 NS
T45LE	RC DELAY CIRCUIT 160 NS
T45LG	RC DELAY CIRCUIT 2.1 S
T45LH	RC DELAY CIRCUIT 500 MS
T45LI	RC DELAY CIRCUIT 176 MS
T45SA	DELAY FILE READY
T55AA	INDICATOR COUPLING NETWORK
T55AB	ICN-LAMP
T55AC	INDICATOR LAMP-3V
T55AD	15MA SWTCH ID NO LOAD
T55AH	40 MA IND DRIVER UNLOADED
T55AI	40 MA INDICATOR DRIVER
T55AM	15 MA INDICATOR DRIVER
T55AN	15 MA INDICATOR WITH NETWORK
T55BB	INDICATOR
T60AA	50V DECOUPLING NETWORK
T60AB	20V DECOUPLING NETWORK
T60AI	+48V INTEGRATOR
T60AJ	20V INTEGRATOR
T60BF	SWITCH INTEGRATING NETWORK
T60SA	AC WRITE CURRENT INT
T60SE	INTERGRATOR
T61AA	750 OHM LOAD RESISTOR
T61AB	750 OHM LOAD RESISTOR
T61AC	350 OHM LOAD RESISTOR TO +3V
T61AD	LINE TERMINATOR NETWORK
T61AG	BIT GATE CONVERTR LOAD RESISTR LCM
T61AJ	300 OHM LOAD RESISTOR TO +3V
T61AK	750 OHM RESISTOR
T61AM	630 OHM LOAD RESISTOR
T61AN	LOAD RESISTOR-2322
T61AO	NPL FINAL AMP INPUT TERMINATOR
T61AP	100 OHM TERMINATING RESISTOR
T61AW	100UH INDUCTOR TO -3V
T61AX	160 OHM RESISTOR TO +3V
T61BD	DRIVER DAMPING NETWORK
T61BE	DRIVER COLLECTOR LOAD
T61BF	DRIVER EMITTER LOAD
T61BG	130 OHM TO +3V
T61BI	RESISTOR COMB
T61BJ	DELAY LINE TERMINATOR
T61BK	RESISTOR 759 OHM TO -3V
T61BL	100 OHM TO +3V
T61BM	220 OHM TO +3V
T61BN	300 OHM TO +3V
T61BO	RESISTOR 300 OHM TO -3V
T61BP	RESISTOR 1.8K TO -3V
T61BR	180 OHM RESISTOR TO +3V
T61BS	SELECTOR DECOUPLING NETWORK
T61BT	DRIVER COLLECTOR LOAD
T61BU	DECOUPLING NETWORK A
T61BV	DECOUPLING NETWORK B
T61BW	+12V MARGINAL POWER SUPPLY
T61BX	110 OHM TO +3V
T61BY	180 OHM TO +3V
T61BZ	120 OHM TO +3V
T61CC	430 OHM TO +6M
T61CF	FDD DIODE
T61CG	TYPE DD DIODE
T61CH	TYPE DE DIODE
T61CK	RESISTOR-CHOKE
T61CL	175 OHM TO +3V
T61CN	BIASING NETWORK
T61CR	WRITE BIT RESISTOR-LCM
T61CS	TYPE DO DIODE

CIRCUIT NUMBER	TITLE
T61CV	TYPE DE DIODE
T61CW	HPD LOAD RESISTOR
T61CY	1.175K LOAD RESISTOR
T61CZ	2K POTENTIOMETER
T61DA	750 OHM TO +3V
T61DC	100 OHM LINE TERMINATOR TO +3V
T61DD	MAGNETIC HEAD DIFFERENTIATOR
T61DE	BIT GATE DIODE LCM
T61DF	RESISTOR 38.3 OHM
T61DG	BIT GATE CONVERTER LOAD RESISTOR
T61EA	600 OHM RESISTOR LOAD TO +6V
T61EE	164 OHMS TO -3V
T61EF	820 OHM RESISTOR TO +6V
T61JB	680 OHM TO +6V
T61JD	240 OHM TO -3V
T61JE	+ 6V DECOUPLING NETWORK
T61SB	DETENT LEVEL SETTER
T61SC	CYLINDER A.C. LEVEL SETTER
T61SD	INDEX LEVEL SETTER
T61SE	51 OHM RESISTOR TO -3V
T61SJ	R.C. FILTER
T61SN	130 OHM RESISTOR TO +6V
T61SQ	BIASING NETWORK
T61SS	SINGLE STEP DIFFERENTIATOR
T61ST	RESISTOR 2K
T63AA	COIL FOR 6 CONTACT REED RELAY
T63AB	POINTS FOR 6 CONTACT RR
T63AC	6 CONTACT REED RELAY
T66AA	NPL FINAL AMP PULSE SHAPE AND DR
U03AA	AND
U03AD	AND INVERT WITHOUT LOAD
U03AE	OR INVERT WITH LOAD
U03AF	AND INVERT WITH LOAD
U03AG	4 WAY EXCLUSIVE OR
U03AH	8 WAY EXCLUSIVE OR
U03AI	AND
U03AJ	OR INVERT NO LOAD
U03AK	AND INVERT NO LOAD
U03AL	OR INVERT WITH LOAD
U03AM	AND INVERT WITH LOAD
U03AN	4 WAY EXCLUSIVE OR
U03AO	8 WAY EXCLUSIVE OR - WITH LOAD
U03AP	AND NETWORK TO 1.2K
U03AQ	AND INVERT TERM WITHOUT LOAD
U03AR	AND INVERT TERM WITH LOAD
U03AS	OR INVERT TERM NO LOAD
U03AT	OR INVERT TERM WITH LOAD
U03AU	AND TERMINATE
U03AV	OR TERM INV NO LOAD
U03AW	OR TERM INV WITH LOAD
U03AX	AND INV TERM NO LOAD
U03AY	AND INV TERM WITH LOAD
U03AZ	OR TERM INV NO LOAD
U03CA	OR TERM INV WITH LOAD
U03CD	MEM DRVR GATE AND
U03CE	MEM DRVR GATE OR
U03CF	MEMORY DRIVER GATE
U03CG	MEM DRVR GATE GROUPING
U03CI	AOI GROUPING NO LOAD
U03CJ	AOI TERMINATOR GROUPING-W/LOAD
U03CM	OR INVERT TERM NO LOAD
U03CN	OR INVERT TERM WITH LOAD
U03CQ	AND INVERT-200 OHM LOAD
U03CT	OR INVERT TERM NO LOAD
U03CU	OR INVERT TERM WITH LOAD
U03CV	OR CIRCUIT MEM GATE
U03CW	MEMORY DRIVER GATE GROUPING
U03VC	AOI GROUPING-NO LOAD
U03VD	AOI GROUPING WITH LOAD
U03VE	AOI GROUPING NO LOAD

CIRCUIT NUMBER	TITLE
U03VF	AOI GROUPING WITH LOAD
U03VG	AOI NO LOAD GROUPING
U03VI	OR INVERT WITH LOAD M-40
U06AA	LSA HIGH SPEED
U07AH	RRE-AMP GATE DRIVER-IOLI
U07AI	M-4 SENSE PRE-AMPLIFIER
U07AL	SENSE DETECTOR- M-10
U07AM	M-4 SENSE AMPLIFIER OR INVERT WITH
U07AN	M-10 PREAMPLIFIER
U07AP	M4 SENSE DETECTOR II
U07AQ	M-10 STROBE DRIVER
U16AL	M-10 BIT DRIVER B
U20AB	GATED AC TRIGGER
U22AA	8.0MC CRYSTAL OSCILLATOR
U22AB	10.0 MC CRYSTAL OSCILLATOR
U32AA	WORD GATE
U40AG	MATRIX SWITCH INPUT-2362
U40AH	MATRIX SWITCH BIAS-2362
U40AI	MATRIX OUTPUT-2362
U40AJ	DETECTOR STROBE 2362
U45AE	DELAY LINE-TAPPED
U55AA	15MA SWITCH ID
U55AD	15 MA SWITCH ID 1K LOAD
U61AB	140 OHM RESISTOR TO +3V
U61AC	125 OHM TO +3V
U61AD	420 OHM TO +3V
U61AE	165 OHM TO +3V
U61AF	230 OHM TO +3V
U61AG	180 OHM TO +3V
U61AN	LSA RESISTOR NETWORK
U61AO	3/4 AMP FUSE TO +30V
U61AP	LINE TERMINATING NETWORK
U61AQ	DELAY LINE DRIVER TERMINATOR
U61AR	DELAY LINE TERMINATOR
U61AU	M-10 SENSE TERMINATION RES
U61AV	M-10 MATRIX READ-WRITE RESISTOR TE
U61AW	M-10 MATRIX GATE TERMINATION RESIS
V03AA	AND FOR A1/A01
V03AF	OR POWER INVERT NO LOAD
V03AL	AND EXTEND
V03AN	OR-INVERT FOR LO SPEED FLIP FLOP
V03AO	AND
V03AR	AND EXTENDER
V03AT	OPI NO LOAD
V03AU	OPI 2.9K LOAD
V03AV	OR INVERT NO LOAD
V03AW	OR INVERT 5K LOAD
V03AX	AND EXTEND FOR API-AOPI
V03AZ	PARITY CHECK NO.1
V03CA	PARITY CHECK NO.2
V03EA	OR
V03EB	AND INVERT NO LOAD
V03EC	AND INVERT 5K LOAD
V03EJ	AND OR GROUPING
V03SD	150 KC AC TRIGGER-INPUT NET
V03SG	DIODE
V03SH	OR-DIODES
V03SI	40 MS SINGLE SHOT
V03SJ	40 MS SINGLE SHOT
V03SK	TRIGGER AC GATE
V03VE	AND-OR-SS GROUPING
V03VF	AND-OR-SS GROUPING
V03VG	AND-OR-SS GROUPING
V03VH	AND-OR-SS GROUPING
V03VI	AND-OR-SS GROUPING
V03VJ	AND-OR-SS GROUPING
V03VK	AND-OR-SS GROUPING
V03VL	AND-OR-SS GROUPING
V03VM	AND-OR-SS GROUPING
V03VN	AND-OR-SS GROUPING

CIRCUIT NUMBER	TITLE
V03VO	AND-OR-SS GROUPING
V03VP	AND-OR-SS GROUPING
V05AE	II NO LOAD
V05EA	HIGH SPEED INVERTER NO LOAD
V05EB	HIGH SPEED CONVERTER 700NS W/L
V05EJ	DCI-II-TLD NO LOAD
V05EK	DCI-II-TLD 3K LOAD
V06AE	EIA TERMINATOR
V06AF	EIA DRIVER
V06EE	NPL LINE RECEIVER NO LOAD
V06SA	LINE TERMINATOR
V07AE	D C HOLE DETECTOR
V07AG	A C MARK DETECTOR
V07EB	SENSE AMPLIFIER
V07EC	P.D.S AMPLIFIER
V10SB	INVERTER
V11AA	SIGNAL EMITTER FOLLOWER
V15AA	280MA DRIVER
V15AC	REED RELAY DRIVER
V15AD	MAGNET DRIVER
V15AE	TRIGGER DRIVER INVERT
V15AI	MAGNET DRIVER 2
V15EC	100 MA HAMMER DRIVER LATCH
V15ED	350 MA RELAY DRIVER
V15EH	407 MA DRIVER
V15SA	RELAY DRIVER 200 MA
V15SB	RELAY DRIVER 100 MA
V20AA	LOW SPEED FLIP-FLOP
V20AB	MG TRIG-700
V20SB	150 KC AC TRIGGER
V20SD	500 KC TRIGGER
V21AL	4.0 USEC FIXED OR DR SINGLE SHOT
V21AT	45 M S SINGLE SHOT
V21AU	AND S S GROUPING
V21AX	100 MSEC SINGLE SHOT
V21AY	AND S S GROUPING
V21AZ	OR VAR SS .99US-200MS
V21CA	OR VARIABLE SINGLE SHOT
V21CB	MSEC SINGLE SHOT
V21CC	AND - SS GROUPING
V21CE	0.5 MS FIXED SINGLE SHOT
V21EA	750 MS SINGLE SHOT
V21EB	2.9 OR 5.6 USEC SINGLE SHOT
V21EC	1.3 US NON-LATCHING SINGLE SHOT
V21EE	AND SS GROUPING
V21EF	1.3 US NON-LATCHING S/S LOAD-3K
V21EP	AND SS GROUP FOR FIXED 750 MS
V21EQ	VARIABLE SINGLE SHOT
V21ER	VAR SS 5.0-20MS
V21SB	67 MS SINGLE SHOT
V21SC	3.1 MS SINGLE SHOT
V21SD	40 MS SINGLE SHOT
V21SE	50 US SINGLE SHOT
V21SF	1.6 USEC DELAY CIRCUIT
V22AA	CONTROL MULTIVIBRATOR
V22AC	5(100 CPS OSCILLATOR
V22EG	360 KC OSCILLATOR XTAL
V22EH	1.6 MC OSCILLATOR XTAL
V22EI	100 KC XTAL OSCILLATOR
V22EJ	1.44 MC XTAL OSCILLATOR
V22EL	720 KC XTAL OSCILLATOR
V22EM	128 KC XTAL OSCILLATOR
V22EN	200 KC XTAL OSCILLATOR
V22ET	15.059KC XTAL OSC
V22SB	.5 PERCENT 269 CPS OSCILLATOR
V22SC	0.5 PER CENT 1200 CPS OSCILLATOR
V40AA	A C CLOCK DETECTOR
V45AA	4.5-14.6 USEC DELAY CIRCUIT
V45AB	12-38 US DELAY CIRCUIT
V45AC	30-97 US DELAY CIRCUIT

CIRCUIT NUMBER	TITLE
V45AG	4.4-17 MS DELAY CIRCUIT
V45AH	16-63 MS DELAY CIRCUIT
V45AI	59-220 MS DELAY CIRCUIT
V45AJ	2.0 USEC FIXED DELAY CIRCUIT
V45AK	4.0 USEC FIXED DELAY CIRCUIT
V45AL	INVERTER FOR DELAY CIRCUITS
V45AM	4.5-14.6 USEC DELAY GROUPING
V45AN	12-38 USEC DELAY GROUPING
V45AO	30-97 USEC DELAY GROUPING
V45AP	2.0US FIXED DELAY GROUPING
V45AQ	4.0US FIXED DELAY GROUPING
V45AR	205-660US DELAY GROUPING
V45AS	1.4-4.5US DELAY GROUPING
V45AT	67-220MS DELAY GROUPING
V45AU	9.7-31 MSEC DELAY GROUPING
V45AV	25-81 MSEC DELAY GROUPING
V45AW	550-178 USEC DELAY GROUPING
V45AX	1.7-5.5 USEC DELAY CIRCUIT
V45AY	1.7-5.5 USEC DELAY GROUPING
V45AZ	83-260 USEC DELAY CIRCUIT
V45CA	83-260 US DELAY GROUPING
V45CC	3.7-12 MS DELAY GROUPING
V45CD	1 SEC TIMER
V45CF	1.7 US-220MS DELAY CKT
V45CG	200 MS DELAY
V45CH	140 MS FIXED DELAY CKT
V45CJ	30 MS FIXED DELAY CKT
V45EA	1.7 2.9 OR 3.4 US DELAY CKT
V45EB	VARIABLE DELAY CIRCUIT
V45EF	FAST RECOV 1.8US DELAY CKT

CIRCUIT NUMBER	TITLE
V45EH	DELAY CIRCUIT
V45SA	75 SEC TIME OUT
V55AB	INDICATOR DRIVER
V55AE	RESISTOR INDICATOR UP LEVEL
V55AF	INDICATOR-UPLEVEL RESISTOR
V55AG	RESISTOR DOWN LEVEL INDICATOR
V55AJ	700 NS 40 MA IND DRIVER UNLOADED
V55AK	UP LEVEL INDICATOR LAMP
V55AL	UP LEVEL INDICATOR LAMP
V55AM	RESISTOR FOR V55AK
V55AN	UP LEVEL RESISTOR INDICATOR
V55AO	HP INDICATOR DRIVER
V55AP	LP INDICATOR DRIVER
V55EA	40 MA LAMP RES NW COMB LOGIC
V60AA	INTEGRATOR CKT
V60AB	INTEGRATOR-G
V60AC	INTEGRATOR-S
V60AD	INTEGRATOR-L
V60AE	12 VOLT INTEGRATOR
V60AF	48 VOLT INTEGRATOR
V60ED	CARRIAGE TAPE INTEGRATOR
V60EE	DECOUPLING NETWORK
V61AA	2.9K LOAD RESISTOR
V61AC	3K LOAD RESISTOR
V61AD	3K RESISTOR TO +48V
V61AE	4.5 V DIVIDER
V61AF	RESISTOR 1.5K
V61EA	LOAD RESISTOR 270 OHM
V61ED	390 OHM 1 WATT RESISTOR TO +12V
V61EF	VOLTAGE REFERENCE NETWORK

Index

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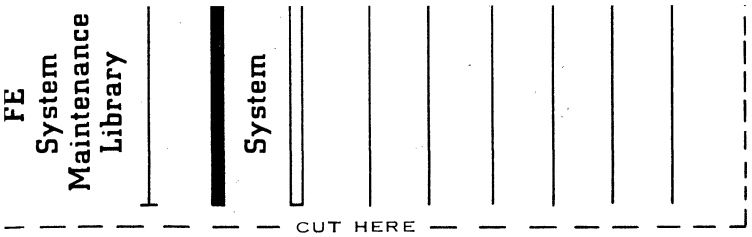

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