IBM

Field Engineering Education
Student Self-Study Course

# Monolithic System Technology
# Packaging and Documentation

## PREFACE

This publication is primarily intended for FE Education students enrolled in the Monolithic System Technology Packaging and Documentation Course 50070.

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## Preliminary Edition

THIS PUBLICATION IS IN A PRELIMINARY STATE OF DEVELOPMENT. ANY CORRECTION OR SUGGESTIONS THAT YOU CAN OFFER FOR THE FORMAL PUBLICATION WILL BE APPRECIATED.

CONTENTS

## GENERAL INFORMATION

### LEGEND

| | |
|---|---|
| ALD | Automated Logic Diagram |
| AR-DF | Differential Amplifier |
| ASLT | Advanced Solid Logic Technology |
| C | Control |
| CD | Controlled Data |
| Com | Common |
| DCD | Decoder |
| FEESSC | Field Engineering Education Student Self-Study Course |
| FF | Flip Flop |
| FETOM | Field Engineering Theory of Operations Manual |
| FL | Flip Latch |
| FLB | Functional Logic Block |
| GI | Gate In |
| GO | Gate Out |
| I/O | Input/Output |
| MST | Monolithic System Technology |
| PH | Polarity Hold |
| Reg | Register |
| SCM | Supplementary Course Material |
| Sel | Selector |
| SLD | Solid Logic Dense |
| SLT | Solid Logic Technology |
| SS | Singleshot |
| SSC | Student Self-Study Course |

### MATERIAL REQUIRED

The FSS monitor or your branch office self-study administrator will provide you with the materials necessary to complete this course.

## SESSION 1 - INTRODUCTION

This session requires approximately .5 hour to complete.

MST is introduced, described, and compared to current technologies. Comparisons between SLT and MST are made with the emphasis on similarities. Begin by reading the objectives and self-evaluation questions. Next answer the questions at the terminal. After all answers are entered, you will be given assignments where needed.

Objective: Upon completion of this topic, the student, using the maintenance documentation, should be able to:

1. List the basic packaging scheme:
   a. Module-on-card
   b. Card-on-board
   c. Board-on-gate
   d. Gate-on-frame
   e. Frame-on-machine
2. Define the acronym MST.
3. List the number and type of MST families.
4. Define the maintenance philosophy.
5. List the cooling method used for each MST family.

### PRE-POST TEST QUESTIONS

Enter your answers via the FSS terminal.

1. Arrange the following list in the correct ascending order for the MST packaging scheme: (answer questions with letter only - no spaces or shifts)

   a. Gate-on-frame
   b. Module-on-card
   c. Card-on-board
   d. Frame-on-machine
   e. Board-on-gate

2. MST stands for _____.

3. There are _____ families of MST and they are _____, _____ and _____.

4. The MST maintenance philosophy includes: (choose one)

   a. Module replacement
   b. Gate replacement
   c. Card replacement
   d. Frame replacement

5. Match the following families with the method used in cooling: (Enter the numeric characters only)

| | | | |
|---|---|---|---|
| _____ | a. | MST-1 | 1. Liquid cooled air |
| _____ | b. | MST-2 | 2. Forced ambient air |
| _____ | c. | MST-4 | 3. Normal room ventilation |
| | | | 4. Convection |

ASSIGNMENT

The assignments during this course are objective oriented. Assignment 1 will be material necessary to satisfy objective 1, etc. Where there is more than one assignment for a given objective, the assignment number (objective number) will be suffixed with an a, b, c, etc.

The assignments for this session are as follows:

1-1. Read assignment 1-1.
1-2. Read Assignment 1-2 (this page)
1-3. Read assignment 1-3 (page 3)
1-4. Read Assignment 1-4 (page 3)
1-5. Read Assignment 1-5 (page 3)

The assignments given in this section of the FEESSC are objective oriented and are numbered to the session and objective. For example, 1-1 would be an assignment for Session 1, objective 1. 1-1b would be assignment 2 for objective 1 within Session 1.

1-1. There are many similarities between MST and SLT. The first obvious one is the packaging scheme - modules are used to contain circuits. The modules are mounted on cards which in turn plug into boards. The boards make up gates which are grouped as frames. The boards, gates, and frames are interconnected by cables.

The prime reason for the development of MST is the increased need for faster speeds and higher performance. MST provides higher circuit reliability along with decreased circuit cost when compared with SLT.

1-2. MST is an abbreviation for Monolithic System Technology. It is IBMs newest method of designing and building products. MST is a progressive step of SLT/SLD to ASLT to MST.

The term monolithic relates to the method used to fabricate circuit components within the structure of a single material by successive etching and deposition of doped materials.

1-3. Monolithic System Technology consists of three circuit families - MST-1, MST-2, and MST-4. The three families differ in circuit speed, module, and card packaging density. The various computer systems will use one or more of these circuit families within its framework. However, one family will usually predominate. For example, the Model 85 uses MST-4.

1-4. The maintenance philosophy for MST type equipment is card swapping or card replacement. Card swapping is the location of the same card in another part of the system and exchanging it with the suspected card. The error symptoms should change, indicating that the suspected card is indeed failing. Card swapping has proved to be a very successful troubleshooting tool. The card replacement technique is required where there are no redundant part numbers of the suspected card within the system.

However, the replacement cost per card for MST is much higher than for SLT because of the higher circuit density. For example, an MST card can have up to 20 circuits within one module.

Module replacement is not included in the maintenance philosophy. Cards with faulty modules will be returned to the plant for repair.

1-5. The method used for cooling in SLT was forced ambient air. The progression to ASLT, because of additional heat dissipation, required a more efficient and effective heat dissipation, hence the use of liquid cooling.

In MST, the cooling method is dictated by the circuit family type. MST-1 and MST-2 use forced ambient air whereas MST-4 uses liquid cooled air. You will find that throughout our discussion that MST-1 more closely compares with SLT than MST-2 or MST-4.

SESSION 2 - PACKAGING AND PHYSICAL LOCATIONS

This session requires approximately 1.0 hour to complete.

In this session the physical characteristics of the technology are described. The location of all relevant components and points on components within a gate are defined.

The various coordinate schemes which are used to locate components is taught. This includes module pins and card coordinates since scoping at these points may be required when servicing MST equipment.

Objective: Upon completion of this topic, the student, using the maintenance documentation, should be able to:

1. Locate any card on an MST gate.
2. Identify any card pin number on an MST card.
3. List the number of signal, voltage, and ground planes that exist for each of the MST board types.
4. Define the following terms:
   a. I/O pin.
   b. Logic pin.
   c. I/O logic pin.
5. Locate any pin on a module.
6. Locate any pin location on an MST board.

PRE-POST TEST QUESTIONS

1. Refer to Frame 14 (A15).

   When entering, please enter the three numbers corresponding to the blanks indicated.

2. An MST-4 card (four wide) has tab pins labeled:

| Alphabetically | Numerically |
|---|---|
| _____ and _____ | _____ through _____ |
| _____ and _____ | _____ through _____ |
| _____ and _____ | _____ through _____ |
| _____ and _____ | _____ through _____ |

   To answer this question - fill in the blanks and then enter the characters and numerals on the terminal - no spaces, words or shifts please.

   Enter reading from left to right, top to bottom.

3. How many signal, voltage, and ground planes are there on each of the MST:

| Boards | Signal | Voltage | Ground |
|---|---|---|---|
| MST-1 | _____ | _____ | _____ |
| MST-2 (single) | _____ | _____ | _____ |
| MST-2 (double) | _____ | _____ | _____ |
| MST-4 | _____ | _____ | _____ |

Enter a total of 12 numbers on the terminal. No spaces or shifts please.

Enter the filled in blanks left to right, top to bottom.

4. Match the following:

| | | | |
|---|---|---|---|
| _____ a. | I/O pin. | 1. | Board pins used for communication to the logic contained on a card. |
| _____ b. | Logic pin. | 2. | Board pins used for both communication to card logic and communication off the board via a cable. |
| _____ c. | I/O logic pin. | 3. | Board pins used for communication off the board via a cable. |

Enter the number characters only.

5. Refer to Frame 15 (A16).

You are looking at a module from the pin side so that the orientation code indicator is in the lower right-hand corner.

Answer this question by filling in the numbered location that corresponds to the following list of pins:

| | |
|---|---|
| A03 _____ | D04 _____ |
| D01 _____ | B02 _____ |

Answer by entering numbers from left to right, top to bottom.

6. Refer to Frame 16 (B02)

There are 3 darkened squares denoting board pin locations. Please enter, in any order the socket and pin number.

For example, enter C2D13

Please do not enter spaces or shifts.

ASSIGNMENT

Assignments given in the Field Engineering Theory of Operations Manual (FETOM) are chapter and title heading oriented. The table of contents will assist you in locating any references I will make.

2-1. The MST card location scheme consists of seven intermixed letters and numbers eg, 02AC1D2. The first two digits - 02 - equal the frame number. The next letter indicates the gate within that indicated frame. The next two digits - C1 - equal the column and row of the board. The D2 equals the column and row location of the card on that board. Refer to the FETOM under the heading MST Boards in Chapter 1. There are about seven board grids shown in the MST Boards section. The number scheme is the same for each, so that anyone will do.

NOTE: The grid shows the board looking at the card side and not the probe side.

## SESSION 3 - LOGIC BLOCKS

This session requires approximately 1.5 hours to complete.

The logic blocks unique to MST are defined. A good deal of SLT experience and knowledge is assumed in this session. A review of the Logic Blocks session in the SLT Packaging and Documentation course may be helpful.

Objective: Upon completion of this topic, the student, using the maintenance documentation, should be able to:

1. Recognize and define the following terms and symbols:
   a. Storage element
   b. Common section
   c. Data section
   d. Gate-in
   e. Gate-out
   f. Sel
   g. Reg
   h. DCD
   i. AR-DF
   j. Com
   k. M and only M
2. Given input levels, determine the output levels of a logic block with any of the above logic symbols.

### PRE-POST TEST QUESTIONS

1. Match the following list of logic symbols with the descriptions of how they operate:

| Description | | Logic Symbols | |
|---|---|---|---|
| _____ a. | A device whose output stands at its indicated polarity, when and only when the specified number of inputs stand at their indicated polarity. | 1. | Storage element |
| _____ b. | A block that consists of two or more unit logic functions with common lines, such as gates, which does not fit the description of Reg or Sel. | 2. | Sel |
| _____ c. | Operates similar to an exclusive OR. In addition to ORing, it also amplifies. | 3. | Reg |
| _____ d. | A logic block in which inputs and outputs are assigned numeric numbers. | 4. | DCD |
| _____ e. | A logic block, consisting of a group of associated storage elements with common lines, such as reset, control, etc. | 5. | AR-DF |
| _____ f. | Consists of two or more ANDs or ORs shown as input and/or output gates. | 6. | Com |
| | | 7. | M and only M |
| | | 8. | SS |

Enter the numeric characters only.

2. Refer to Frames 17 through 19, location B3 through B5. Each frame has two logic blocks drawn with at least one output line. To the right of each logic block is a timing chart with each input line indicated. The output line is indicated below the input line with three alternatives. Choose the number which most correctly indicates the output waveform.

   When entering your answer on the terminal, you should enter all six answers at one time, eg, 1 1 2 2 3 3.

ASSIGNMENT

3-1. This assignment defines a functional logic symbology for high density digital circuitry. It defines a dependency notation system (gating) that provides for common controls to large portions of circuitry.

Objectives

To provide a more comprehensive functional diagram by replacing large groupings of interconnected basic logic (ANDs, ORs, inverters) by one symbol. To provide more direct information for maintenance by making the important probe points stand out. To reduce system page count.

Applicability

This document is applicable to new Field Engineering Automated Logic Diagrams (FE ALDs), and to all hand-generated diagrams for new machines.

General

The symbology presented in the following paragraphs may be used on any level of diagrams requiring a logic symbol provided that the circuits are packaged in logical groupings consistent with this standard. It is imperative that the boundary of the symbol used does not encompass any connection points required at that diagram level. For example, the register described in this standard would not be feasible for card package logic which must provide module pins, unless it were contained in one module, but should be used for system logic which only requires that card pins be shown.

Non-Exhaustive

The figures in this assignment are examples only of particular combinations that illustrate a typical symbol. There is no intent to be exhaustive.

Storage Element

A group of circuit elements or basic logic functions interconnected to perform the storage function. The storage element is a device that has two stable states, which are referred to as the one or set state and the zero or reset state. The outputs shall be shown with polarity indicating the one state. The storage element has seven possible basic inputs that affect the state of the device as indicated in the definitions given below. Any number of inputs may be used and in combinations dependent upon the design of the device. See Figure 3.1.

| | |
|---|---|
| Input S<br>Set | When at its indicated polarity, the storage element will be set and the outputs will be at the polarity shown, and the storage element will remain in the one state until reset. |
| Input R<br>Reset | When at its indicated polarity, the storage element will be reset and the outputs will be at the opposite polarity to that shown, and the storage element will remain in the zero state until set. |
| Application | Application of R and S depends on one or the other being active, but not both. When both the R and S inputs are simultaneously brought to their indicated polarity, the polarity the outputs will assume is dependent on the circuitry, not on the logic function. |
| Input J<br>Set/Complement | When at its indicated polarity, the storage element will be set, and the outputs will be at the polarity shown, and the storage element will remain in the one state until reset. |
| Input K<br>Reset/Complement | When at its indicated polarity, the storage element will be reset, and the outputs will be at the opposite polarity to that shown, and the storage element will remain in the zero state until set. |

| | |
|---|---|
| Application | Simultaneous application of the indicated polarity to both J and K will cause the storage element to complement. If the storage element was in the one state, it will change to the zero state and vice versa. |
| Input T Complement | When at its indicated polarity, it causes the storage element to complement. If the storage element was in the one state, it will change to the zero state and vice versa. |
| Input C Control | When at its indicated polarity, it will enable the controlled line to set or reset the storage element. |
| Input CD Controlled Data | When the control input (C) is at its indicated polarity, the controlled data (CD) input will, when at its indicated polarity, set the storage element and the outputs will be at the polarity shown, when at the opposite polarity to that indicated, the storage element will be reset and the outputs will be at a polarity opposite to that shown. When the control input (C) is at a polarity opposite to that shown, the controlled data input (CD) has no affect on the state of the storage element. When the control input (C) goes from its indicated polarity to the polarity opposite that indicated, the storage element will remain in the state it had at that instant. If the storage element was in the one state, it will remain in that state and vice versa. |

Treatment of Ambiguous Inputs

A notation will be added to the output(s) of a storage element to indicate the polarity of the outputs during the simultaneous application of ambiguous inputs. Ambiguous inputs are defined as inputs S and R. An S or R will be placed under the appropriate output(s) to indicate the condition of the output(s) with respect to the state of the storage element. An S indicates that the output will be at the polarity indicated and an R indicates that the output will be at a polarity opposite to that indicated. See Figure 3.2. There are other possible combinations not shown which cannot be defined.

Figure 3.1

Storage Elements MST

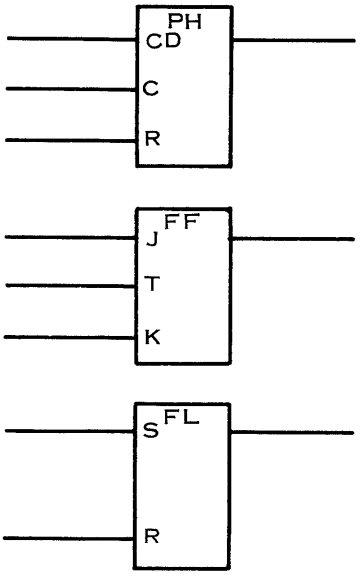
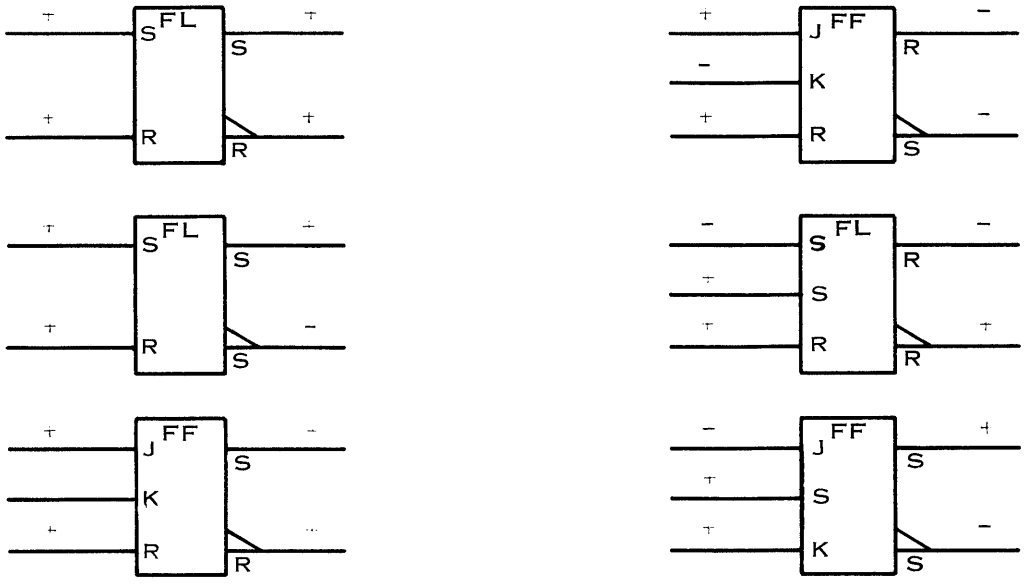



Figure 3.2

Indications of Outputs During Simultaneous Application of Ambiguous Inputs



Symbol

This symbol shall consist of two sections and the functional designation. See Figure 3.3.

Data Section

The bottom section is a group of vertically stacked (butted) functional elements. The height of each logic element may vary with the number of inputs and the amount of data to be placed in each; the width, as required for maximum data content shall be the same for all elements. The individual logic positions may be separated by lines.

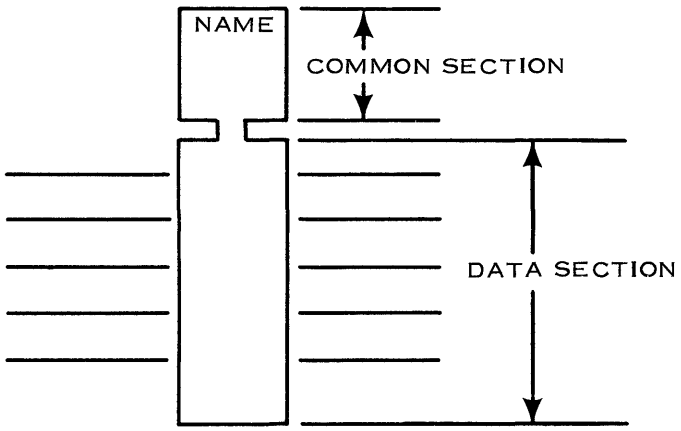
Common Section

The top section for common lines is located at the top of the block and separated from the bottom functional element by a narrow neck. The neck may vary in length consistent with diagram needs. The height of the common section shall depend upon the number of inputs, its width shall be the same as the attached logic elements. There shall be no outputs from the common section.

Name

The common section shall have the block's name on its first internal line.

Figure 3.3



## Gating

This notation can be considered to be a method of representing the AND function without the use of the AND logic symbol. Its use simplifies the representation of high density packaged logic.

### Rules for Gating

Each gated line shall be identified with the same numeral used to identify its related gating line. The numeral shall be placed opposite the line just within the logic block. The gating lines shall be numbered 1, 2, etc, except when used with DCD, then they shall be lettered A, B, etc.

NOTE: Each gate shall have a unique number (letter).

Gating lines, in addition to being numbered, shall be identified by a letter preceding the numeral; the letter shall be consistent with the following:

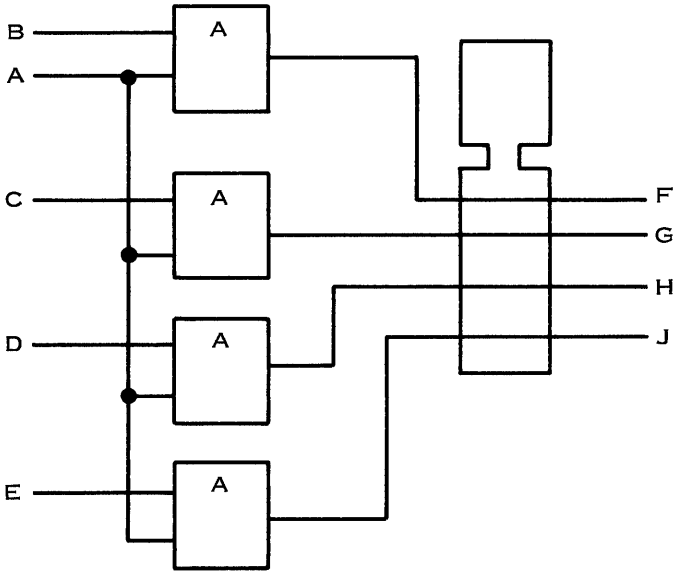
1. When a gating line has gated lines, as inputs, or inputs and outputs, it shall be identified by the letter "G." (Gate)
2. When a gating line has as gated lines only outputs, it shall be identified by the letters "GO." (Gate out)

### Definition

| | |
|---|---|
| Gate In (G) | (A.) When at its indicated polarity, it will permit its gated line to enter its condition into the FLB. A gated line at its indicated polarity will enter an active condition into the FLB and vice versa.<br><br>(B.) When at a polarity opposite to that indicated, it will prohibit its gated line from entering its condition into the FLB.<br><br>See Figure 3.4. |
| Gate Out (GO) | (A.) When at its indicated polarity, the condition of the FLB can be gated out. An active FLB position will produce a polarity on the output line of the polarity indicated and vice versa.<br><br>(B.) When at a polarity opposite to that indicated, the condition of the FLB cannot be gated out. The output line will always be at a polarity opposite to that indicated.<br><br>See Figure 3.5. |

Figure 3.3

Without Gating Notation




Using Gating Notation

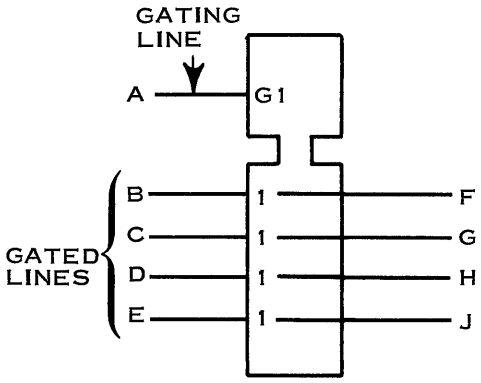
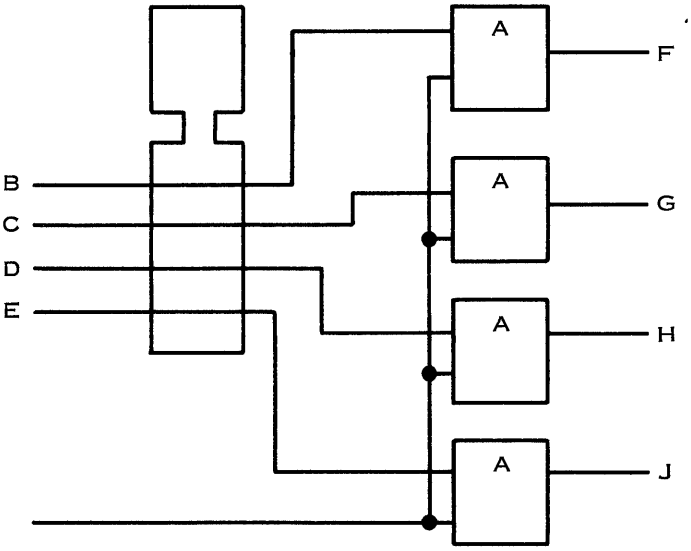
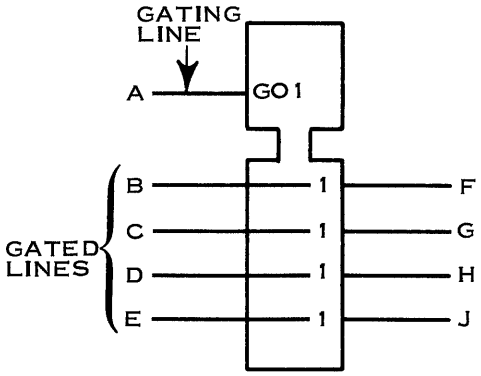



Figure 3.4



Selector (Sel)

The selector is a functional logic block that consists of:

1. Two or more ORs having input and/or output gating (see Figure 3.5), or
2. Two or more ANDs shown as input and/or output gates (see Figure 3.6), or
3. A combination of 1 and 2.

Common Section

Contains gating lines common to one or more logic elements, which shall be identified as described in paragraph on Rules for Gating.

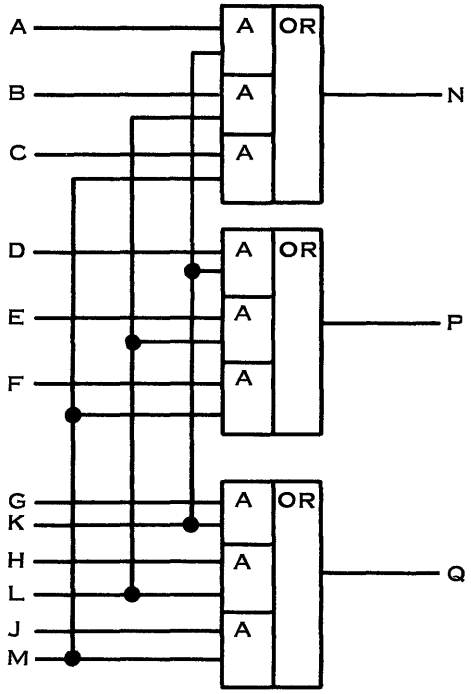
Data Section

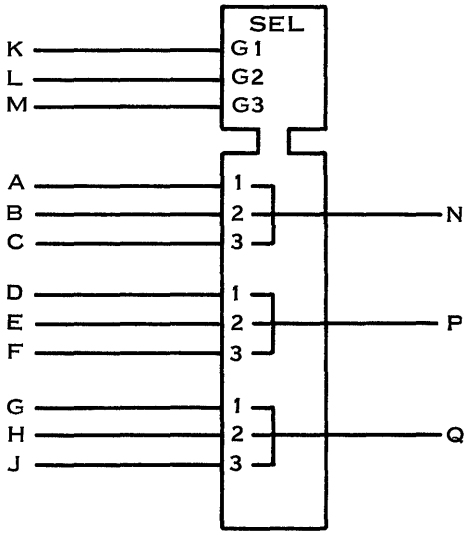
The inputs and/or outputs shall be grouped and shall be interconnected with lines and connecting symbol (◇). The connecting symbol denotes an OR function when used to connect input lines. See Figure 3.5.

Name

The common section shall have the name Sel.

Figure 3.5



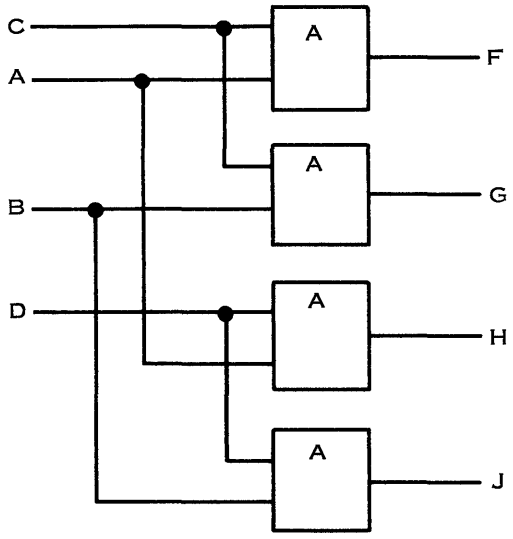



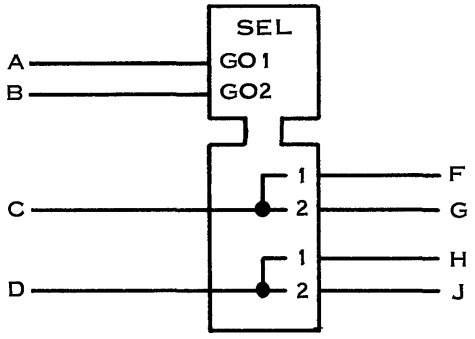

TRUTH TABLE

| K | L | M | A | B | C | N |
|---|---|---|---|---|---|---|
| + | X | X | + | X | X | + |
| X | + | X | X | + | X | + |
| X | X | + | X | X | + | + |
| + | + | + | - | - | - | - |
| - | - | - | + | + | + | - |

X = EITHER + OR -

Figure 3.6




TRUTH TABLE

| A | B | C | F | G |
|---|---|---|---|---|
| + | - | + | + | - |
| - | + | + | - | + |
| - | - | + | - | - |
| + | + | - | - | - |

Register (Reg)

A register is a functional logic block consisting of a group of associated storage elements with common lines, such as reset (R), control (C), etc. Common gates may also be included. (See Figures 3.7 and 3.8.)

Common Section

Contains lines common to one or more logic elements, which shall be identified as described under Gating and under storage elements.

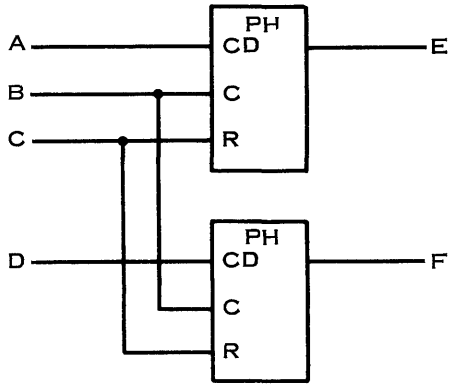
Data Section

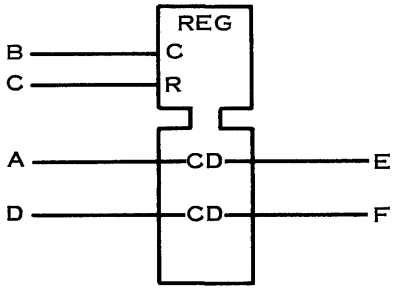
The inputs and/or outputs shall be grouped and shall be interconnected with lines and connecting symbol.

Name

The common section shall have the name Reg.

Figure 3.7



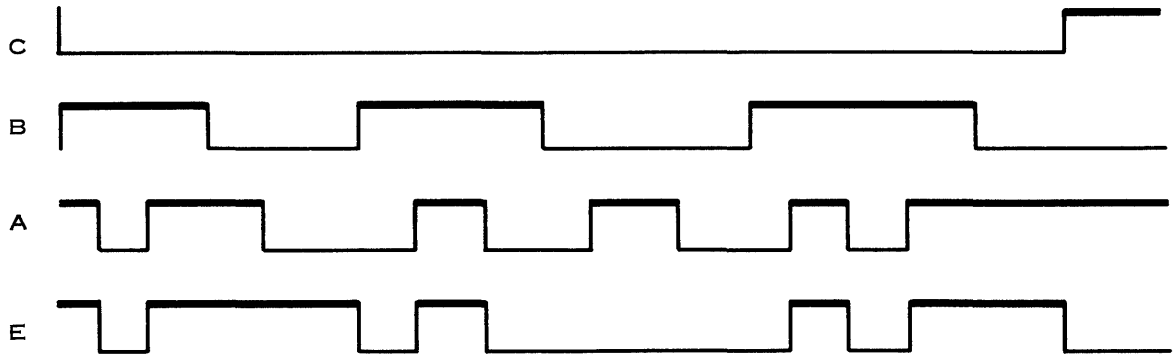
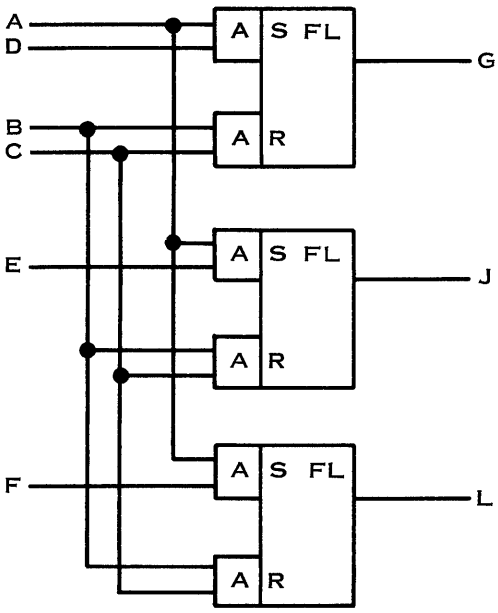
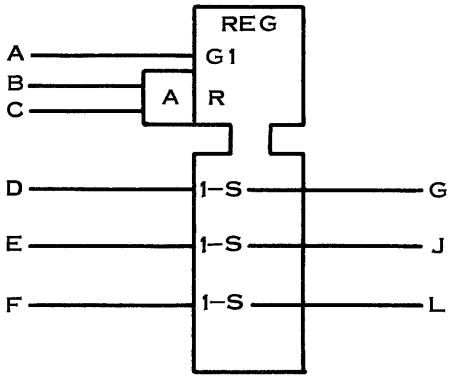



Figure 3.8



Decoder (DCD)

A functional logic block in which inputs and outputs are assigned numeric values. An output line is active when and only when its value (number) is equal to the sum of the values of all active input lines.

NOTE: At any given time, there is only one sum. If all input lines are inactive, the sum is zero.

Common Section

When gating is used, the gating line and gated line shall be cross-related by labeling with a letter, rather than a numeral. These common lines shall be drawn to the common section. See Figure 3.10. The common section is not used if there are no common lines. See Figure 3.9.

Data Section

The inputs to a DCD block shall be numbered 1, 2, 4, 8, 16, etc (from top to bottom). The outputs shall be numbered to reflect the sum of the active inputs required for each DCD output.

Name

The common section (when used) shall have the name DCD; when the common section is not used, the data section shall have the name DCD.

Figure 3.9

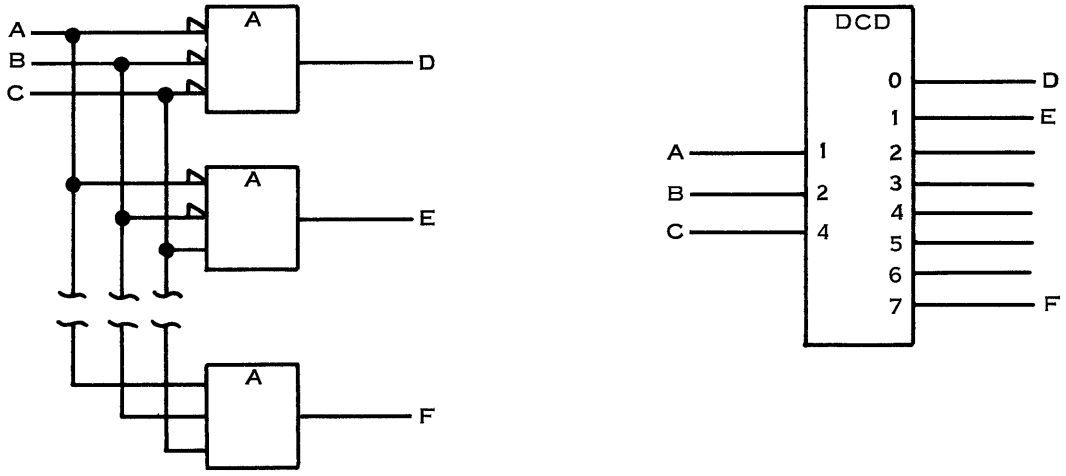
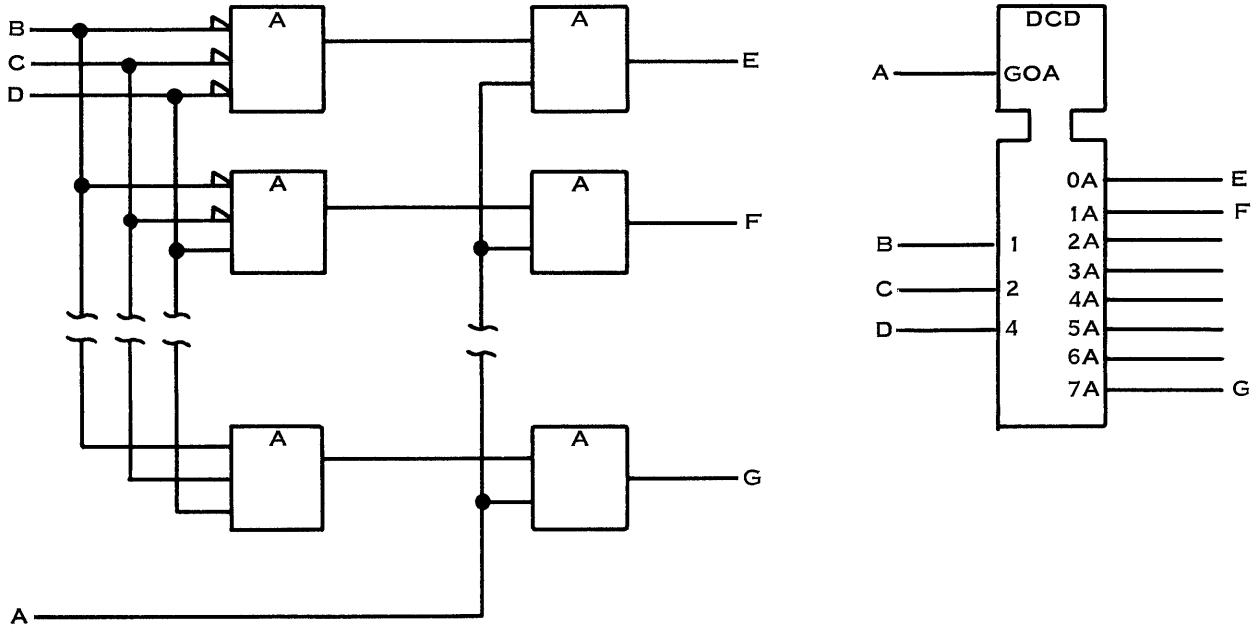



Figure 3.10



## Common (Com)

The common block is a functional logic block that consists of two or more unit logic functions with common lines, such as gates, which does not fit the description of Reg or Sel. (See Figures 3.11 and 3.12.)

### Common Section

The common lines are drawn to the common section of the logic block, and if they perform the gating function are as described under Gating; otherwise, they are defined as performing the logic function of the individual positions.

### Data Section

This section contains the individual unit logic blocks and their functions. The individual unit logic positions are separated by lines.

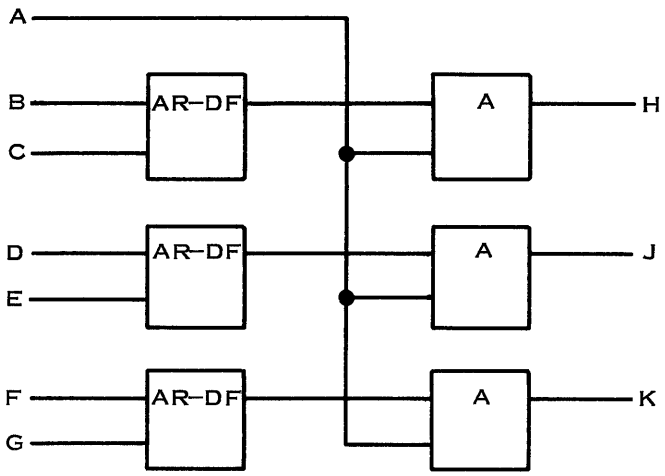
### Name

The common section shall have the name Com.

### AR-DF (Refer to frame B04)

This block represents a differential amplifier which produces an output that corresponds to the signed difference in voltage of the two input signals. Another way of saying this is that it operates like an exclusive OR. It is sometimes shown with a third input which is a gate out (GO). In the referenced frame, choice 2 shows the output of line D.

Figure 3.11




TRUTH TABLE

| A | B | C | H |
|---|---|---|---|
| - | X | X | - |
| + | + | - | + |
| + | - | + | + |

X = EITHER + OR -

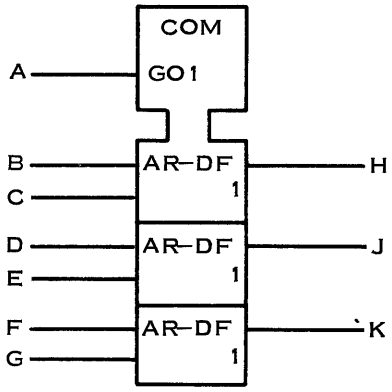
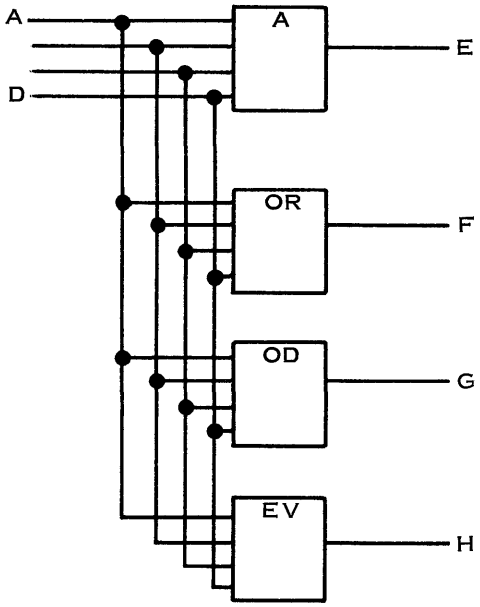
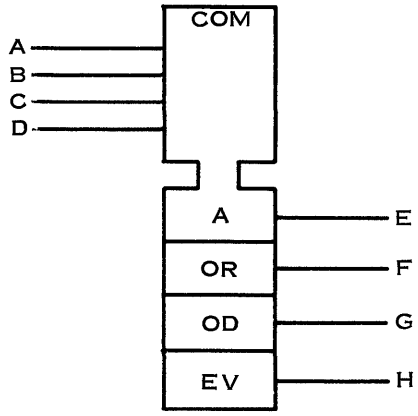


Figure 3.12




TRUTH TABLE

| A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|
| + | + | + | + | + | + | - | + |
| + | + | + | - | - | + | + | - |
| + | + | - | + | - | + | + | - |
| + | + | - | - | - | + | - | + |
| + | - | + | + | - | + | + | - |
| + | - | + | - | - | + | - | + |
| + | - | - | + | - | + | - | + |
| + | - | - | - | - | + | + | - |
| - | + | + | + | - | + | + | - |
| - | - | + | + | - | + | - | + |
| - | + | - | + | - | + | - | + |
| - | + | + | - | - | + | - | + |
| - | - | - | + | - | + | + | - |
| - | + | - | - | - | + | + | - |
| - | - | + | - | - | + | + | - |
| - | - | - | - | - | - | - | + |

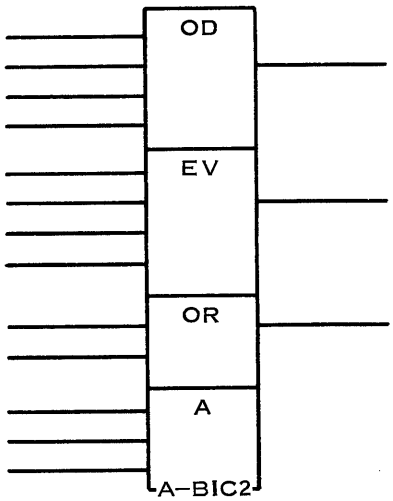



NOTE: OD = ODD
EV = EVEN

Vertical Stacked Blocks

Logic functions that have a common location, within the same replaceable unit, may be butted together to form a vertical stack. Each logic function will retain its own identity. The common location will not be repeated in each logic block, but will appear only once in the last print position of the bottom most block.

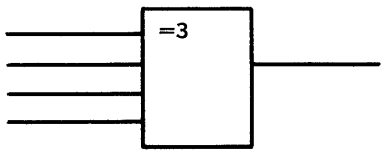
Figure 3.13




M and Only M

A device whose output stands at its indicated polarity, when and only when the specified number of inputs stand at their indicated polarity. The functional symbol to be marked in the block shall consist of the equals sign (=) followed by the numeral for the specific m-number of inputs. The =m symbol shall not be used to replace a single AND function.

Figure 3.14



Notations Beneath Output Line

Additional information shall be placed below each output of a block as explained in the following paragraphs.

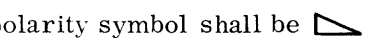
Loading

On outputs which have a probe point, the symbol L will be used to indicate internal load. External loads will be assumed if the symbol is not indicated. A loaded output is defined here as one which will react to its inputs in the absence of any external connection to the output. See Figures 3.15 and 3.16.

Dotting

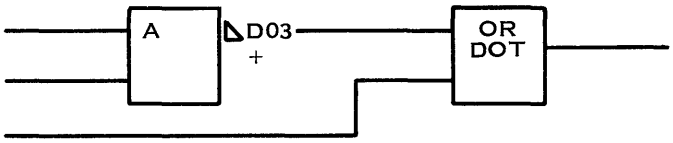
Where wired logic is employed, each output of a logic block which is affected by a dot shall have a symbol which indicates the polarity to which that output may be forced by the dot.

The positive polarity symbol shall be +.

The negative polarity symbol shall be 

See Figures 3.15 and 3.16.

Figure 3.15



SESSION 4 - FE ALDs

This session requires approximately 1.5 hours to complete.

The most significant difference between SLT and MST FE ALDs is found in the technique of Direct Addressing which facilitates the tracing of logic on an FE ALD page.

Objective: Upon completion of this topic, the student, using the maintenance documentation, should be able to:

1. Locate any logic blocks on an FE ALD page, using its block serial number and determine:
   a. Input pin numbers.
   b. Output pin numbers.
   c. Gate and card location for that block.
   d. Logic function of that block.
2. Trace any input or output line on an FE ALD page to its destination or from its origin. The FE ALD page will use the direct addressing scheme.
3. Locate the following FE ALD page facts:
   a. Input/output line net numbers.
   b. Input/output line name.
   c. FE ALD page number.
   d. Output page number.
   e. Asterisk in a logic block output line.

PRE-POST TEST QUESTIONS

1. Refer to Frame 23 (B10).

   Frame 23 shows an FE ALD page for MST using the direct addressing scheme of line tracing.

   Choose the correct statement for the following questions (enter a, b, c, or d).

   The question concerns the first block down in column 5.

   a. Block serial = BD, output pin = 502, block logic = AND, block location = 01BB2K2.
   b. Block serial = BD, output pin = 502, block logic = AND, block location = 02BB2K2.
   c. Block serial = BD, output pin = G13, block logic = AND, block location = 01BB2K2.
   d. Block serial = BD, output pin = G13, block logic = AR, block location = 02BB2K2.

2. Refer to Frame 23 (B10).

This question has twelve parts. When answering via the terminal, please enter one answer at a time. Please use no spaces, shifts, or other punctuation. I suggest you fill in the blanks and enter from there.

a. Locate input line labeled -EARLY BITS 21-25 EVEN. The page number that this line came from is _____.
b. This line goes to a total of _____ locations on this page. (numeric answer)
c. The input line number is _____.
d. The block serial number of column 1 location is _____.
e. The input pin number is _____.
f. The output line number is _____.
g. The logic function of the next logic block is _____.
h. Assuming that this block is satisfied, the output line number that will be active is numbered _____.
i. The column 4 output location logic block (upper one) serial number is _____.
j. The output line number of this block is _____.
k. The logic of the column 5 logic block is _____.
l. The output line of this block leaves this board at socket location _____. (Answer with board socket location only.)

3. Refer to Frame 23 (B10).

This question has six parts. When answering via the terminal, please enter one answer at a time. Please use no spaces, shifts, or other punctuation. I suggest you fill in all blanks and then enter from the paper.

a. Locate output line labeled +SS FIELD DECODE ERROR. The line number is _____.
b. This line goes to a total of _____ pages when it leaves ED131.
c. Continue tracing this line back toward the input side. The line comes from column _____.
d. The function of the block is _____.
e. Assume the upper line of this block was active. The pin location is _____.
f. The input line comes from page number _____.

ASSIGNMENT

4-1. Refer to Frame 23 (B10). Use Frame 23 as you follow the following description. Frame 23 shows a FE ALD page using the direct addressing scheme for tracing the logic displayed. Locate the EV logic block which is the third logic block down in the first logic block column.

Each logic block is broken down into a number of print line positions. The EV logic block you are looking at has a total of five print line positions and they are counted from top to bottom.

The layout for the EV is:

Print position 1 = AG (block serial number)
Print position 2 = 52TD10 or 137
Print position 3 = 2TD09
Print position 4 = 12TB10
Print position 5 = B-B2K2

Let us examine each print line. The first print line contains the block serial number. In this particular case, it is AG. Each logic block on an FE ALD page contains a block serial number for location purposes. There is no particular sequence to the block serial numbering scheme. They are scattered throughout the page in a random fashion. The logic block serial numbers are listed alphabetically at the bottom of the page and will assist us in tracing output lines. We will cover this aspect later on in the course.

Print line 2 contains five pieces of information in this particular block. First, it has the number 52. The 52 is called a line number and will later assist us in tracing a line throughout the page. Whereas the old method was to label each line with a name, we will now label them with numbers.

The second item of information is T. This is voltage level information and indicates the acceptable up and down levels for this particular input pin.

The third item is D10 which is the input pin number.

The fourth item is the logic of this block which is an EV.

The next item of information is 137 which is the line number for the output pin for this EV block.

The last print line contains B-B2K2 which is the gate, board, and card location for the card that this EV circuit is mounted on (note the frame number for this card is located in the lower right-hand corner of the FE ALD page).

4-2. Direct addressing is a method of block to block communication without using lines.

The page can be divided in up to seven columns. The left most column contains the input information and the right most column contains the output information. In the columns between are the logic blocks. The columns are separated by vertical lines and may have a line of asterisks. The line of asterisks represents information that goes to the output column. The vertical lines correspond to the logic block columns 1-5, line one for column 1, line 2 for column 2, etc.

All input and output lines of a block are labeled with numbers. The input lines coming from the input information column with one or two digit numbers; all other input and output lines with three digit numbers. The first digit representing the logic block column, column 1 with a one, column 2 with a two, etc, the second and third digit represent the vertical print position. The page has ninety vertical print positions so line 140 will appear in column 1 approximately half way down the page, line 280 will be in column 2 near the bottom of the page, etc.

To become familiar with direct addressing, a line will be followed from input to output.

Refer to Frame 23 (B10).

Step 1

Input line 12, labeled -early ROSDR bit 22 SS bit 1, is found on the left side of the page, the second line down.

Line 12 shows a two in vertical line 1. This means that it goes to column 1, two times. In column 1, line 12 feeds a sel block and an EV block. The EV block has two other lines feeding it. They are line numbers 52 and 2 Any input pin to a logic block which does not have a pin number indicated means that pin cannot be scoped.

Step 2

The output of the EV block line 137 goes to column 2 one time. In column 2 line 137 goes to an AND block serial AH. The other line feeding the AND block comes from line labeled 72.

Step 3

The output of the OR line number 237 goes to column 4 two places. If you trace this line through either the EV or OD blocks in column 4, you will eventually wind up with line number 402 or 444 in column 5 feeding the OR block serial number BD.

Step 4

The output pin is labeled G13*502, which means the output pin number is G13 and the asterisk indicates that additional information concerning this line is available at the bottom of this FEALD page.

Step 5

The output line of block serial number BD goes two places on this page. It goes to the output column (last line) and is labeled +SS Field Decode Error.

The * means that this line leaves this board. To find the connector socket and pin used to leave this board, refer to the information at the bottom of this FEALD page.

The block serial numbers start with AA6 and run through BD2. The 2 after the BD indicates the output pin that is found on print line position 2 for the BD block. Following BD is B-B2H1B13, which means that the line leaves this board at board B2 socket H1 pin B13.

This completes tracing a line from input to output.

With direct addressing, it is just as easy to trace a line from output to input.

Step 1

Locate line number 328 in the output information column. The line is labeled -SS FIELD EQU OF EXOFF.

Step 2

The next step in locating where this line comes from is to analyze the line number itself (328). The three indicates the column; the 28 gives the print location in that column. Number 28 is approximately one-third of the way down column 3.

Step 3

Locate line 328 in column 3 at the output of the SEL serial number AA. The SEL has a number of inputs. Assume that we were interested in the upper input line number 204.

Step 4

Locate line 204 in column 2, 4 print positions down from top. It is an output pin of a DCD serial block BA. Line 204 represents the one output of the DCD. To get this output pin 1 of the inputs must be satisfied. Let's look for the line number 106 which is the input pin.

Step 5

A line number of 106 tells us that this line comes from the column one. Line 106 is located 6 print positions down in column one and is the output of a SEL block serial AE.

Step 6

The input pin required to satisfy the output of 106 is B10 line number 12. Line number must be from the input information column because it is a 2 digit line number. Line number 12 is labeled - Early ROSDR Bit 22 SS Bit 1.

This completes tracing a line from output to input.

4-3. Refer to Frame 23 (B10).

Locate line number 330 in the output information column. The line is labeled -SS FIELD EQU OD BSOE. The information at the end of the line reads GN6 which is not pertinent to our discussion.

The information under the label reads ED241 and RZ102. The ED241 and RZ102 are the page numbers to which this line goes.

Locate line 330 in column 3. It is one of the output pins of a SEL block. The output pin number is B07. Note the asterisk on the line which indicates that the line leaves this board. The succeeding pins to which this line goes are indicated at the bottom of this FEALD page.

The SEL block serial is AA. The output pin B07 is output print position 8. Locate the AA8 at the bottom of the page.

Following the AA8 is B-B2J6C02 which means that the line goes from B-B2K2B07 (location of SEL block) to B-B2J6C02 (from bottom of page) to B-B3C1A11 (from bottom of page).

## SESSION 5 - SMALL CARD DOCUMENTATION

This session requires approximately .5 hour to complete.

Card ALDs and supporting documentation is developed in this session. The requirements to scope at the card level is necessitated primarily by the relatively few numbers of scopeable pins per logic contained on a card.

Objective: Upon completion of this topic, the student, using the maintenance documentation, should be able to:

1. Locate the following things on a small card ALD:
   a. Card part number
   b. The part number of any module
   c. The logic of any block
   d. Any module pin number
   e. Input/output pin numbers
2. Locate any part on a card, using the small card ALD reference grid.

PRE-POST TEST QUESTIONS

1. Refer to Frame 24 (B12).

   The number of input tab pins indicated on ALD page 3963-1 is:

   a. 8
   b. 3
   c. 1

2. Refer to Frame 24 (B12).

   Choose the correct statement:

   The block located at 4L on ALD page 3963-1 indicates the following facts:

   a. Part number of the card is 2541833. The block logic is 2 ANDs ORed together. The module represented by this block is located at coordinates M28.
   b. Part number of the module is 2541833. The block logic is 2 ANDs ORed together. The module represented by this block is located at coordinates M28.
   c. Part number of the module is 25418330. The block is 2 ORs ANDed together. The module represented by this block is located at coordinates M28.

3. Refer to Frame 24 (B12).

The part number of the card represented is:

a. 5856181
b. 2541833
c. Cannot be determined by the ALD page.

4. Refer to Frame 24 (B12).

(True/False) The block located at 4L has four input pins numbered D03, D02, A03, etc. The pin numbers represent card pin numbers.

5. Refer to Frame 25 (B14).

The module represented in the upper left-hand corner is located by which of the following indicators?

a. 2541846
b. AC
c. T23

ASSIGNMENT

5-1. All MST systems will include ALDs for each card in the system. Frame 24 (B12) is a sample copy of a small card ALD page.

The page number is indicated outside the description block in the lower right-hand corner. The page number of this page is 3963-1. The -1 indicates that it is the first page of this group. The information within the square is self-explanatory except for the part number (PN). The part number is the part number of the MST card that is represented by this and other pages in the group. In our example, the part number of this MST card is 5856181.

The input lines enter the left side of the page and the output lines leave the right side of the page. Let's examine the input lines first. Refer to Frame 24 (B12). The top input line is labeled -MUP CTR BUS BIT P and the label is followed by 39639AD4. The first 5 digits (3963-9) is the page number from which this line came.

This is the first page of the group and the line originated on the ninth page of the group. The next three digits are AD4 and they equal the net number of this particular line. Note that this line is an internal wiring on the card and is not connected to one of the tab pins on the card.

The third line up on Frame 24 is labeled -IO MODE CHO-5 A CYCLE. Note that this line does not include the eight digits that the first line did, indicating that this line does not originate on this card but instead, originates off the card. If you follow the line to the right about an inch, you will note three digits (001). The three digits denote the fact that this line is connected to a tab pin on the card. The tab pin number to which this line is connected is listed in the margin information at the bottom of the page.

Refer to the bottom of Frame 24. To the left of the bit information is listed the number 001, etc. Beneath 001 is the number M10 B10. The first three digits (M10) denotes the pin number on the card to which the line labeled -IO MODE CHO-5 ACYCE is connected. The B10 indicates technical information concerning this line and should not concern you.

Note that in addition to the number 001, there are three more groups of characters (AT2), (AU2), and (AV2). These characters refer to output line information. Find the output line characters labeled -YIC INPUT P BIT (it is the first line down on the right side of the page). If you follow the line out, you will notice the character AT2 and they can be found at the bottom of the page along with the input pin indicator. The AT2 line indicates that this line is connected to card tab pin number S05.

Let's discuss the individual characters within each block as shown on Frame 24. Locate the first block down on the left side of the page. It has a AOR on the first line within the block. The AOR indicates the logic of the block as being a circuit which operates as an AND circuit ORed (the pin C04, is a module pin, not card tab pin).

The next two lines within the block (C1 and ALA00) are not significant for our explanation so skip down to 18300H. The 1830 is the last four numbers of the part number for this module. The full part number for this module is 2541830 and I will show you how we get the 254 a little later in the course.

Move down to the next line which reads T19-A. The -A is of no significance to us, but the T19 shows the location information for locating this specific module on the card. The next step in the course will show the use of the card component locating grid and how the T19 will locate the module physically for us.

The last line on the block shows the characters 1B-AA. The 1B locates the logic block on this page. The AA on this line can also be disregarded as it does not contain information pertinent to our discussion.

5-2 Refer to Frame 25 (B14). Frame 25 shows the component location scheme for an MST card. The upper left-hand corner gives the card part number and the EC level of the card.

The left and right margins of the page show A 0-4 through a minus sign - 92. The numbers 4 through 92 are print line positions for this two high card. Actually the print line starts with 1 even though they show the first number as 4.

The top and bottom margins show two rows of numbers (4-108 and 01-27). The 4-108 again are print line positions and the 01-27 are location indicators.

To locate a specific module on a card, you refer to the location indicator on the small card ALD page (it was the fifth print line down on the logic block). The location indicator uses numbers like T23-A (the 'A' is not relevent). The T23 is the location code for the module in the upper left corner of Frame 25 (B14).

The module is located by using the alphabetic characters in the verticle rows and crossing them to the location numbers in the horizontal rows. Look at the block located at T23 on Frame 25 (B14). The top line of print for this module shows a part number of 2541846. The A01* indicates that the pin underneath that indicator is pin A01 for that module. The AC in the left hand corner is not used for our discussion.

## SESSION 6 - MAINTENANCE TECHNIQUES AND SERVICE AIDS

This session requires approximately .5 hour to complete.

In this section of the course we will investigate the type of reference documentation available to the CE which can be considered to be technology - oriented and related to the troubleshooting process.

Objective: Upon completion of this topic, the student, using the maintenance documentation, should be able to:

1. Determine if a duplicate of a suspected card with a given part number resides elsewhere in the system/machine. If so, determine its physical location.
2. Define the following acronyms:
   a. MPUL
   b. LPUL
   c. LNDL
   d. MNDL
3. Identify the proper scope probes and tips to be used for each type MST board and card.

PRE-POST TEST QUESTIONS

1. Assume you have determined that a card at location 02AC3E2 (P/N 5853323) is failing and you want to swap it with a card in the machine, which of the following locations contains the same card P/N:

   a. C2
   b. D2
   c. P2
   d. E2

   Refer to Frame 26 (B15).

2. Match the following MST families with their respective MPUL and MNDL:

| MPUL and MNDL | Families |
|---|---|
| _____ a. 0.570 - 1.000 | 1. MST-1 |
| _____ b. -0.613 - 2.383 | 2. MST-2 |
| _____ c. 0.675 - 1.260 | 3. MST-4 |

   Fill in the blanks and then enter the number and letter.
   For example, 3a, 1b, etc.

3. Match the following scope probe part numbers with their respective MST family:

| | | | | |
|---|---|---|---|---|
| _____ | a. | MST-1 | 1. | 453163 |
| _____ | b. | MST-2 | 2. | 453446 |
| _____ | c. | MST-4 | 3. | 453888 |

Enter numeric characters only.

4. Match the following abbreviation with definition:

| | Definition | | Abbreviation | |
|---|---|---|---|---|
| _____ | a. | Most positive up level. | 1. | MNDL |
| _____ | b. | Least positive up level. | 2. | MPUL |
| _____ | c. | Least negative down level. | 3. | LNDL |
| _____ | d. | Most negative down level. | 4. | LPUL |

Fill in the blanks. Enter 1a, 3b, etc.

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