dsp Technology Inc.

TRAQ

Reference Manual

48500 Kato Road Fremont, CA 94566 tel:510-657-~~7576~~ 7555 fax:510-657-7576

Proprietary Statement

Notice is hereby given that all data contained in, revealed by, or shown on this document, whether a drawing or other writing, is proprietary and belongs to DSP TECHNOLOGY INC., Fremont, California. It is furnished and received in confidence solely for information purposes or procurement of the product to which it relates. Neither the document nor any information/data contained in it shall be used for any other purpose or duplicated or disclosed in whole or in part to anyone else without the prior written authorization of DSP TECHNOLOGY INC. in each instance. If such written authorization be given by DSPT, any disclosure or revelation by the recipient to anyone else shall be accompanied by a written statement incorporating the language and contents of this legend.

TABLE OF CONTENTS

SECTION 1
TRAQ SYSTEM

System Description

DSP Technology's TRAQ system is a modular product which acquires analog or digital data from multiple input channels and stores the information in local memory at rates up to 8 million data samples per second. Modular memory and analog digitizing (or digital interface) units allow easy system field expansion or reconfiguration.

Each TRAQ system is defined by one controller (4012 A or P; 4032 A or P), at least one memory module (5003, 5004, 5200..5032) and at least one digitizer module or input channel (2812, 2824, 2814, 2860...).

Data transferred from the digitizer modules to memory is initiated by a clock pulse which the controller generates from an internal crystal or an external signal. There are actually two selectable internal clocks (CLK1, CLK2) which can be controlled by the user. This allows selected portions of the data to be sampled at different rates. There are many instances where some portions of the data which has higher frequency components needs to be sampled at faster rates. The 4012/4032 will accept an external control signal which causes the unit to switch between the two clock frequencies. There is also available a mode which enables the controller to switch to the second frequency after detecting a "stop trigger." When the controller is sampling with the second clock (CLK2) the 16th bit of the data (MSB) can be set to a binary one. This allows the user to differentiate data sampled at the two clock rates.

> **NOTE**
>
> This option can be defeated by a jumper strap if the 16th bit is used by the digitizer unit. (See Section 10.)

Once the digitizer units receive the clock pulse (conversion command) all analog data is sampled simultaneously and digital data is stored in local digitizer buffer memories. Analog data is captured by sample & hold circuits which hold the signals constant as the analog to digital converters (ADCs) operate. Each sample & hold feeds directly into its own ADC. At the end of the conversion cycle, a signal is sent back to the controller

signaling that data is ready for readout. The controller then sequentially reads data for all required channels. The user can select the Number Of Channels (NOC) that are actively converting. As NOC is decreased the controller will allocate more memory storage for the active channels. Data is transferred sequentially as 16-bit words to the controller at a 8 Megasample/second rate. The controller double buffers the digitizer data, forming a 32-bit word which is stored in memory. When sampling is started the first data sample is stored at address zero of the memory and subsequent data at the next incremental memory location. After the memory is filled , new data is written over the previous data starting at address zero. This continues in a "round robin" fashion until a "stop trigger" is received. The "stop trigger" is either an external TTL signal, a front panel switch, or a computer command. This trigger initiates the "post trigger" sampling sequence which determines how much data is recorded before the trigger versus after the trigger. If "PTS" is set to "8/8" then all data is post trigger and sampling will stop once the entire memory is filled one more time.(i.e.,. if the memory size/channel is 32 K samples; another 32 K samples of data is recorded). If "PTS" = "0/8" then recording stops immediately and all the data was recorded before the time of the trigger. The controller allows the user not only to select the amount of memory per data channel, but also to divide this memory in 1/8th segments of post and pre-trigger data. The controller keeps track of where the earliest recorded sample resides in memory. All data read, or displayed starts from this sample.

After recording is complete the controller will display the data (through a digital-to-analog converter) or read it out to the computer. Data can be read starting at any 1024 block in the record. Also data readout can terminate at any point in the record and immediately go to another channel for readout.

TRAQ Controllers

The system controller is in command of all data acquisition. It communicates with the computer or user (through front panel controls) to determine the required sampling rate, pre/post trigger information, number of active data channels, memory allocation, data display and data readout. All control settings can be saved in a non-volatile memory to be restored on power-up. Communication with the computer is via the CAMAC bus; however, all data acquisition is passed through two private busses. Data from the input units is sequentially passed to the controller and then out to memory. The data is sequentially retrieved by the controller for display and readout.

The controller also executes a set of diagnostic routines on command or power up. These routines will usually catch and isolate any fatal system problem.

There are presently four controllers available for the TRAQ system:

Controller	TRAQ Memory Limitations	Comments
4012A	16 MegaSamples total; 4 MegaSamples/Channel	Standard Controller
4012P	16 MegaSamples total; 4 MegaSamples/Channel	Data retention on power down. (Requires battery backed-up TRAQ memory modules)
4032A	256 MegaSamples total; 256 MegaSamples/Channel	Standard Controller
4032P	256 MegaSamples total; 256 MegaSamples/Channel	Data retention on power down. (Requires battery backed-up TRAQ memory modules)

The 4012P/4032P units are used in environments where data retention upon loss of power is critical and they have extra control signals to protect acquired data. The 4012P has an optional reserved memory section for calibration data. These controllers are used with 5204 memory modules (internal batteries) or 5008 Bs, 5432 Bs (using external batteries).

TRAQ Memories

The amount of data storage in a TRAQ system depends on the selected controller and memory module.

Model	Memory Size (MegaSamples)	Max Modules/System	Comments
5004B	1	8	4012 or 4032 Controller
5005	2	4	4012 or 4032 Controller
5006	4	4	4012 or 4032 Controller
5007	6	1	4012 or 4032 Controller
5008	8	4	4012 or 4032 Controller
5408	8	8	4032 Controller
5416	16	8	4032 Controller
5424	24	8	4032 Controller

5432	32	8	4032 Controller
5204	0.5	8	4012 or 4032 Controller; Internal Battery Retention

🕮 NOTE

5005..5008 and 5408..5432 are also available in B version for external battery backup.

All memory modules on a system should be of the same type. If modules are mixed, consult the factory for configuration information.

Analog-To-Digital Converters

A variety of analog to digital conversion units are currently available for the TRAQ system. A maximum of 256 digitizer channels can be run on one system but the total throughput rate cannot exceed 8 million samples per second. The total throughput is calculated as the product of the number of active digitizer channels times the sampling rate.

Presently the following units are available:

Model	Number of Channels/Module	Maximum Conversion Rate/Channel	Resolution
2812	8	100 KiloSamples/Sec	12
2814	4	100 KiloSamples/Sec	14
2824	1	2 MegaSamples/Sec	12
2840	4	1 MegaSamples/Sec	14
2860	4	1 MegaSamples/Sec	12

Digital-to-Digital Converters

Two modules, 2932 and 2904, are available for inputting digital information. The 2904 is used to record encoder signals from rotating devices and is not covered in this manual (see 2904 manual). The 2932 is a general purpose digital input module which will record two 16-bit TTL channels (32-bits) into TRAQ simultaneously with ADC data from the analog-to-digital channels. It also contains spare wire wrap socket space and a CAMAC interface for user customization.

Typical TRAQ Configurations

Controller	Memory	Allowable Memory Sizes	Max Number of ADC channels	
			2812	2860
4012 A/P	5004B	1 to 8 Meg	80	8
4032 A/P	5432	32 to 256 Meg	80	8

NOTE

This assumes that each channel of the

2812 is sampling at 100 kHz

2860 is sampling at 1 MHz

TRAQ Current and Power Requirements

Model	Current (amps)				Power (avg.)
	+6	-6	+24	-24	(Watts)
Controllers					
4012 (A/P)	4.0	0.05	0.05	0.05	27
4032 (A/P)	4.0		0.05	0.05	27
Memories					
5004B	2.5				15
5005	1.25				7.5
5006	1.5				9
5007	1.75				10.5
5008	2.0				12
5408	1.25				7.5
5416	1.5				9
5424	1.75				10.5
5432	2.25				13.5
Digitizers					
2812	1.5	0.55	0.150	0.150	20
2814	1.3		0.150	0.250	18
2824	1.0	0.70	0.100	0.100	15
2840	1.0		0.600	0.600	35
2860	1.7		0.250	0.270	20
2932	1.0				6
2904	2.0				12

TRAQ Installation

The minimum system configuration consists of one signal conversion channel (ADC), one controller, and 1 Megasample of memory. A CAMAC crate is also required and usually a crate controller to allow the TRAQ system to communicate with a computer. (Only one crate controller is required for each CAMAC crate).

System Interconnections

1) The memory modules are connected to the controller via a 50 pin flat cable. This cable plugs into the front panel TRAQBUS connectors. The memory modules usually reside to the left of the controller in the crate. This keeps the flat cable from interfering with the other controller signal cables. TRAQ systems are delivered with flat cables built for the system configuration ordered. If the system configuration is not specified, the cables will correspond to an equal distribution of ADC modules and memories.

2) During power-up diagnostics the controller will determine how much memory is on the bus. There must be at least 1024K words. The diagnostic routines will fail at the MEM1 test if no memory is found. Memory modules must have their I.D. switches set so that one module has ID=0, another ID=1, etc., (see Section 11, Memory Modules).

3) The modules can be located in any order in the crate relative to the controller. The 50-pin flat cable connector should be as short as possible to reduce bus noise and crosstalk. Refer to the memory module sections and the diagnostic section of this manual for further information regarding memory configurations.

4) The digitizer modules are connected to the controller through a 40 pin flat cable at the rear of the modules. This cable is also built for the system configuration originally ordered. The digitizer modules are usually installed to the right of the controller in the crate. The first digitizer module must have its ID. switch set to zero, the second to one, etc. The modules can be located in any order relative to the 4012/4032. For DSP digitizers (ex: 2812 ,8 channel ADC), channel 1 will correspond to channel 1 of the module with ID. switch set to zero; channel 9 will correspond to channel 1 of the module with ID. switch set to 1, etc.

5) After installing the units in the crate and connecting the two flat cable connectors, turn on the crate power. The controller will now sequence through a set of

diagnostics. If any problem is found the controller will display a "FAIL" message at the current diagnostic. Refer to the diagnostic part of the controller section.

🕮 NOTE

The controller is not able to check the connection to the digitizer units. This can be checked by setting NOC to the maximum number of channels and CLK1 to the maximum conversion rate. Depress the "start" sampling switch and check that the "CVT" and "SEL" LEDs on the digitizer modules are on. Also the "DACY" LEDs on the memory modules should be on. If more than one memory module is present the "SEL" LEDs should be blinking on/off at a rate dependent on the sampling speed. If this fails check the cable interconnection between the controller and the digitizers.

6) A failed digitizer or memory can usually be determined without removing the interconnection cable. To locate a failed memory just change the ID to a number out of the contiguous memory address range (and the other memory IDs to fill in for the removed module), and repower the system.

☑ EXAMPLE

Consider a four module memory system where the third module is suspected to have failed:

Module Number	ID Before	ID After
1	0	0
2	1	1
3	2	15
4	3	2

When the system is re-powered the controller will find only 3 modules in the system (the controller assumes that an empty address space means the end of the memory chain). If the system is now functional, module 3 has failed.

The digitizers can be checked in the same fashion except that it is not necessary to re-power the system. A failed digitizer can also be isolated by changing NOC. This will reduce the number of active channels and not address the modules with higher IDs.

7) When using the TRAQ system for transient recording there are several parameters that must be set carefully:

a) NOC (number of active ADC channels) must be equal to or less than the number of actual digitizer channels. The 4012/4032 expects a "handshake" signal from each channel when transferring data and if no channel is present the controller will wait indefinitely for the handshake.

b) CLK1 or CLK2 must not be greater than the maximum conversion speed of the channels or else erroneous data will be recorded. Also, the user must be careful not to select a combination of NOC and CLK1, CLK2 which exceeds the maximum TRAQBUS speed of 8 megasamples/second. For instance,

CLK1 (FREQUENCY) <= 8 MHz/NOC

CLK2 (FREQUENCY) <= 8 MHz/NOC

☑ EXAMPLE

Using 50 active channels of 2812 modules, each channel converting at 100 kHz gives:

(50 channels) x (100 KHz) = 5000 kilo samples/second
(5 megasamples/second)

which therefore does not exceed the maximum bus rate.

c) Since the controller accommodates a large amount of memory/channel the user should be careful that "stop triggers" are not generated before sufficient

samples have been recorded or old and new data will be intermixed. This is especially true when PTS =0 (all pre trigger information).

☑ EXAMPLE

Consider using one active channel at 1 MHz (NOC=1, CLK1 = 1 MHz) and one megaword of memory. With these parameters it requires one second to sample all of memory. If PTS=0 and the "stop trigger" is received 1/2 second after sampling begins the last 1/2 of memory is never written into and will contain old data. If PTS=8/8 there is no problem as all the data (and all of memory) will be recorded after the "stop trigger" arrives.

SECTION 2
MODEL 4012 AND MODEL 4032 TRAQ CONTROLLERS OPERATIONAL DESCRIPTION

General Description

The DSP models 4012(A and P) and 4032 (A and P) TRAQ system controllers direct the flow of data between signal conversion units such as analog to digital converters (ADCs), scalers, etc. and memory storage units (Models 5004B, 5008). Up to 256 signal conversion channels can be controlled by one controller with a maximum TRAQBUS transfer rate of 8 million samples per second. Up to 16 megasamples of 16 bit data can be stored using a 4012 Controller and 256 megasamples using a 4032.

As the number of active channels are decreased the controller will allocate more memory to each channel. Also the controller allows the user to increase the number of active channels (NOC) in increments of two (except for NOC=1), i.e. NOC can be 1, 2, 4, 6, 8, 10..256. The memory size (record size) allocated to each channel is set by the controller and depends on the number of active channels and the total memory size. The user may select record sizes from the maximum memory/channel allowed down to 1024 samples. Once data acquisition is initiated the memory is written into continuously until a "**stop trigger**" is received which causes the controller to stop sampling after the correct number of post trigger samples have been recorded. The number of post-trigger samples is set in increments of 1/8 of the record size (0, 1/8, 2/8....8/8). The "**stop trigger**" is either an external TTL signal, front panel switch, or computer command.

After completion of sampling, data is either displayed (through a digital-to-analog converter) or read to the computer. The controller has an internal 12 bit digital-to-analog converter which allows the user to view a reconstructed analog waveform on an oscilloscope. A trigger is also provided to synchronize the display. Data is displayed or read starting at the earliest sample recorded. The user can select which channel to display or read. The controller displays all of the recorded data; however, data can be read by the computer starting at any 1K (1024) block.

Signal conversion units are DSP units such as Models 2812 and 2824. Two clock frequencies are available to accommodate switchable sampling rates and are controlled by either:

1) An external control signal "**CLK SWI**" which activates the first clock (CLK1) when the signal is at TTL low and the second clock (CLK2) when "**CLK SWI**" is TTL high.

2) The "**TRIG**" signal which causes the controller to start counting down the preset number of post-trigger samples. In this mode all pre-trigger samples are recorded using CLK1 and all post-trigger samples using CLK2.

The controller can also be clocked using an external user supplied signal. The sampling clock is available to synchronize other controllers.

All controller parameters can be set from front panel switches and through CAMAC from a computer. These parameters can be stored in nonvolatile memory and automatically reloaded on power-up. Also on power-up, the controller sequences through a series of diagnostics and notifies the user if a problem is detected (see DIAGNOSTIC section).

Models 4012P/4032P

The 4012P and 4032 P are special versions of the 4012A and 4032A. The systems differ from the standard units in that:

1) There is a "**LOCKOUT**" signal which can force the controllers to always be in the **LOCAL** control mode and lockout the remote computer.

2) There are two signals which if received in the correct order will start the controller digitizing:

a) "**MASTER ARM**"

b) "**MASTER ENABLED**"

3) The controllers record the memory address of the first sample digitized in a non-volatile memory chip. After power-up this address is restored and data can be displayed/read from the battery backed-up memory modules.

4) The 5204 memory modules used in these systems have an input signal "**WRITE LOCK**" which prohibits the controllers from overwriting the memories.

An additional calibration data block is available only for the 4012:

A 128K sample section of memory can be reserved for calibration data. If enabled, the 4012 will display a total memory size which is 128K less than on the TRAQBUS as this memory is reserved for calibration data only. When the unit is in the acquisition calibration mode, "ACQ CAL", data is digitized as usual, however, after recording is complete the last 2048 samples of data for each channel are transferred to the reserved memory section (approximately 1/2 second is required to transfer data for each channel). The only time data is ever written into the reserved memory section is during this transfer time. The acquisition mode "ACQ DATA" is the standard mode. Data can be read from both the calibration and data sections of memory depending which acquisition mode is enabled. This feature requires a minimum memory size of 256K samples and can be enabled or disabled from the front panel (MCAL function) or by the computer.

The 4012P and 4032P users must be sure that "4012 P" (or "4032 P") has been saved in the non-volatile RAM. On power-up the unit checks this control setting and aborts the memory diagnostics if "4012 P" is set, otherwise the data will be rewritten. The firmware also checks for a valid control setting; detection of an invalid control word forces a default setting to the "4012 A" mode but no memory diagnostics.

Model 4012 and Model 4032 Differences

The 4032 is an upgraded version of the 4012 and is able to read/write larger memory sizes. The 4012 is limited to 16 megasamples of storage while the 4032 is able to address 256 megasamples. The only functional differences are in the CAMAC control commands. **(See Programming the Control Registers Section).**

System Diagnostics

Whenever the controller's microprocessor is reset, either by the front panel reset button or a CAMAC Z (or C) command a series of diagnostic tests are performed. Failure to pass any of these test indicates the system is not functional **(refer to Diagnostic Test section).**

SECTION 3
FRONT PANEL INDICATORS AND CONTROLS

Alphanumeric LED Indicators

The controller has two alphanumeric LED displays which are controlled by two corresponding rotary switches. The **function** switch selects a control to be set and the **value** switch selects the control parameter to be used. As the **value** switch is incremented/decremented the new values are used by the internal processor to set control registers. Once sampling is initiated the values are locked-in and changing the switch values will only affect the next recording. If the controller is in remote mode only the local/remote control and the display channel can be changed. When the controller is initialized by a CAMAC clear (Z or C) or the front panel reset a series of diagnostic tests are performed (see diagnostic section). If any of these tests fail, a "**FAIL**" message will be displayed on the value LED with the corresponding test on the function LED. Failure to complete these tests indicates that the unit is not functional.

Function	Value	Description
ACQ	DATA	The unit is enabled to take data in the standard recording mode.
	CAL	The unit is enabled to take data for calibration recording. After calibration is complete the last 2048 samples for each channel are transferred to the reserved calibration memory.**(4012 only)**
CLKC	NONE	Both internal clocks(CLK1 & CLK2) and the external clock input are disabled.
	EXT	The external clock input is enabled and the internal clocks, CLK1 & CLK2, are disabled.
	INT	The internal clocks (CLK1 & CLK2) are enabled and the external clock input is disabled.
CKSW	NONE	Switching between CLK1 and CLK2 is disabled.
	FTRG	CLK1 is enabled when the SWI front panel input is TTL low. CLK2 is enabled when SWI is TTL high. **NOTE** **CLK1 is the normal sampling clock. When CLK2 is active the 16th bit of the data is set to 1.**
	STRG	CLK2 is enabled after receipt of a stop trigger. (All post-trigger samples are taken with CLK2)

CLK1	5 MHz-10 Hz	Selects the sampling frequency for CLK1 **NOTE** **Do not select a sampling speed greater than the maximum ADC conversion rate.**
CLK2	5 MHz-10 Hz	Selects the sampling frequency for CLK2 **NOTES** **1) Do not select a sampling speed greater than the maximum ADC conversion rate.** **2) Whenever CLK2 is active the 16th bit (MSB) of the data is set to 1. (see DATA FORMAT section)**

Function	Value	Description
DISP	1..NOC	Displays recorded data from the selected channel through the "Display Out" front panel connector to an attached oscilloscope. NOC (number of active channels) is selected by the NOC control. The display is active only after sampling is complete and if there is no CAMAC readout. All data is displayed except when NOC = 1 which displays every other data sample.
INCR	1,10,100,1000	Selects the increment/decrement value used by MSCH.

MSCH	1..	Displays the memory/channel (record size) in 1k blocks. Changing the value switch will increment or decrement the memory/channel by the amount selected in INCR. The minimum memory/channel is 1024 samples and the maximum is determined by the following algorithm: MSCH(MAX) = INTEGER(MSTO/NOC) NOC = NUMBER OF ACTIVE CHANNELS MSTO = TOTAL MEMORY SIZE **☑ EXAMPLE** MSTO = 256k : NOC = 6 MSCH = INT(256k/6) = 42k **🕮 NOTE** The Total Memory Size (MSTO) Is Determined During The Power-Up Test Sequence.
MSTO	Not Adjustable	Displays the total memory size (1k blocks) which is determined during the power-up diagnostic test sequence. **🕮 NOTE** The 4012P will display 128K less memory for MSTO than actually present if enabled for calibration memory ("MCAL YES") since 128K is the required memory to store the calibration data.

Function	Value	Description
MODE	LOCL	Front panel controls are enabled and computer control is locked-out.
	RMOT	Computer control is enabled and front panel controls are locked-out. **NOTE** The computer can override the LOCL control and change to RMOT. Also the front panel can override RMOT and change to LOCL. The display control can be set in RMOT mode.
4012 or 4032	A	Sets control firmware to run 4012A or 4032A code.
	P	Sets control firmware to run 4012P or 4032P code.
MCAL	NO	All TRAQ memory is used for data acquisition. (required for 4032 & 4032P units)
	YES	A 128K data block is reserved for calibration data. **NOTE** Only available for 4012 units.

NOC	1,2,4,6.. 256	Sets the number of active ADC channels. NOC can be set from one to the total number of available ADC channels. **NOTE** Do not set NOC greater than the total number of available ADC channels.
PREV	xxxx	Displays the current revision level of the microprocessor firmware. This message is only displayed after power-up diagnostics are completed.
PTS	0/8,1/8.. 8/8	Sets the number of post-trigger samples in 1/8 intervals. 0/8 : all data is recorded before the trigger. 1/8 : 1/8 of the data is recorded after the trigger , 7/8 before. 4/8 : 1/2 of the data will be recorded after the stop trigger; 1/2 before the trigger 8/8: all of the channel's data will be recorded after the stop trigger.

SAVE	[blank] or DONE	Saves the control parameters in the non- volatile RAM memory. Turning the value switch one position forward or backwards causes the control parameters to be stored and the message "DONE" to be displayed. On power-up the unit will use these settings for the control registers. If on power-up the non-volatile RAM containing the control settings has incorrect settings, the Controller will default to the following control values: ACQ : DAT CLKC : INT CKSW : NONE CLK1 : 100 KHz CLK2 : 100 KHz MSCH : Full record size 4012 : A MCAL : NO MODE : LOCAL NOC : 1 PTS : 8/8

Front Panel LED Indicators

N	Momentary LED. On for approximately 1/2 sec when the Controller is addressed by the CAMAC dataway.
MST	Not Used

LOC	On when the controller is in local mode off when in remote mode.
CVT	On when the controller is recording data.

Front Panel Switch Controls

START/ STOP	Two position momentary switch. The "**START**" position starts sampling, and the "**STOP**" position generates a stop trigger (equivalent to the front panel trigger input). The controller will initiate or reinstate sampling any time "**START**" sampling is depressed. After "**STOP**" sampling is depressed, no further stop triggers will be acknowledged (until sampling is restarted.) **NOTE** This switch is not active in the remote mode.
RST	Resets the microprocessor and initiates the power-up diagnostic sequences.

Front Panel Signals

(The following signals use LEMO, single pin, coax connectors)

DISPLAY OUT	Analog output, approximately ±10 Volts max into 1 Kohm minimum. Displays a reconstructed 12 bit waveform of the recorded data. ADC data is shifted by 2 LSBS (divided by 4) before displaying. Data from 14-bit converters only displays the upper 12 bits; data from 12 bit converters displays only the upper 10 bits. The full scale display ranges for these ADCs are: 1) 14 bit converters: +10V = ADC +full scale. -10V = ADC -full scale. 2) 12 bit converters : +2.5V = ADC +full scale. -2.5V = ADC -full scale. The channel to be displayed is controlled by the front panel switches or CAMAC. At the beginning of each sweep there is approximately a 100 µsec. dead time during which no data is displayed. When there is only one active channel (NOC=1) every other data point is displayed. For all other cases all of the data is displayed.
SYNCH	TTL signal out, into 1 Kohm minimum. The positive edge is synchronized to the beginning of the display sweep.
TRIG	Stop trigger which initiates post-trigger sampling, positive edge sensitive. After receipt of the first positive edge all further transitions are ignored until sampling is re-initiated. Optically isolated, protected to ± 300 Volts, requires approximately 1 ma. of current at 3 Volts to activate.

CLK IN	External clock which initiates sampling of all active ADC channels, positive edge sensitive, TTL, 1 Kohm impedance. The clock frequency may change arbitrarily but the user must insure glitch free transitions.
CLK OUT	TTL signal at the same frequency as the selected clock frequency (internal or external). Will drive one 50 ohm load.
CLK SWI	TTL signal which causes the sampling rate to change from CLK1 to CLK2 if enabled. 1 Kohm impedance, TTL low enables CLK1, TTL high enables CLK2.
BUS REG	Not Used

Model 4012P and Model 4032P Rear Panel Signals

(The following signals use LEMO, single pin, coax connectors)

ARM	Optically isolated, TTL signal, protected to ± 300 Volts. A high TTL level must be detected by the controller followed by **MASTER ENABLE** before digitizing will be initiated. There should be at least a 100 µsec. time delay between assertion of MASTER ARM and **MASTER ENABLE**. Requires approximately 1 mA to activate at 3 Volts.
MASTER ENABLE	Optically isolated, TTL signal, protected to ± 300 Volts. A high TTL level must be detected after assertion of MASTER ARM before digitizing will be initiated. Requires approximately 1 mA to activate at 3 Volts.
MASTER LOCKOUT	Optically isolated, TTL signal, protected to ±300 Volts. A low TTL (or absence of) signal forces the controller into the local control mode. A high TTL level allows the remote control level to be activated. Requires approximately 1 mA to activate at 3 Volts.

Front and Rear Panel Flat Cable Bus Connectors

TRAQBUS	50-pin connector, TTL signals. 32 bits of multiplexed data/address and 12 control signals. Transfers data from the TRAQ controller to memory modules or slave controllers.
ADCBUS	Rear panel, 40 pin, connector, TTL levels. Transfers data from signal conversion units to the TRAQ controller.

SECTION 4
PROGRAMMING THE 4012/4032 CONTROL REGISTERS

CAMAC Control

The following list describes the response of the 4012/4032 to the CAMAC dataway commands. All commands require N(station number) and return X=1 and Q=1 unless stated.

F(0)*A(0)	Read data from the requested command register (see READING the 4012 CONTROL REGISTERS).
F(2)*A(0)	Read data for the selected channel number. Each F(2)*A(0) command reads one data sample and increments TRAQ memory to read the next sample. Data transfer rates up to the maximum CAMAC rates. Before data readout can proceed the correct CAMAC commands must be issued.
F(3)*A(0)	Read module ID. ("4012" or "4032")
F(8)*A(0)	Returns Q=1 if the internal LAM is on, regardless if the LAM was enabled by F(26)*A(0) or not.
F(9)*A(0)	Start sampling. (Only in remote control mode). There is, approximately, a 500 µsec delay from receipt of the F(9)*A(0) command to the actual start of sampling.
F(10)*A(0)	Reset LAM Turns the internal and external(CAMAC dataway) LAM off.
F(17)*A(0)	Selects a command register for reading/writing.(see WRITING the 4012 CONTROL REGISTERS, this section).
F(24)*A(0)	Disables the LAM (look-at-me) signal from the CAMAC dataway. However the internal status can be monitored by the F(8)*A(0) command (Q=1 returned if the internal LAM is on).

F(25)*A(0)	Stop sampling (equivalent to then front panel" stop trigger"). **NOTE** The controller will respond to this command in both local and remote control modes.
F(26)*A(0)	Enables the internal LAM (look-at-me) signal onto the CAMAC dataway.
Z/C	Initializes the controller, resets the microprocessor, and starts power-up diagnostics. **NOTE** The controller will respond to this command in both local and remote control modes.
LAM	LAM, look-at-me is generated when sampling is complete and when data is ready for readout (if in remote mode.)

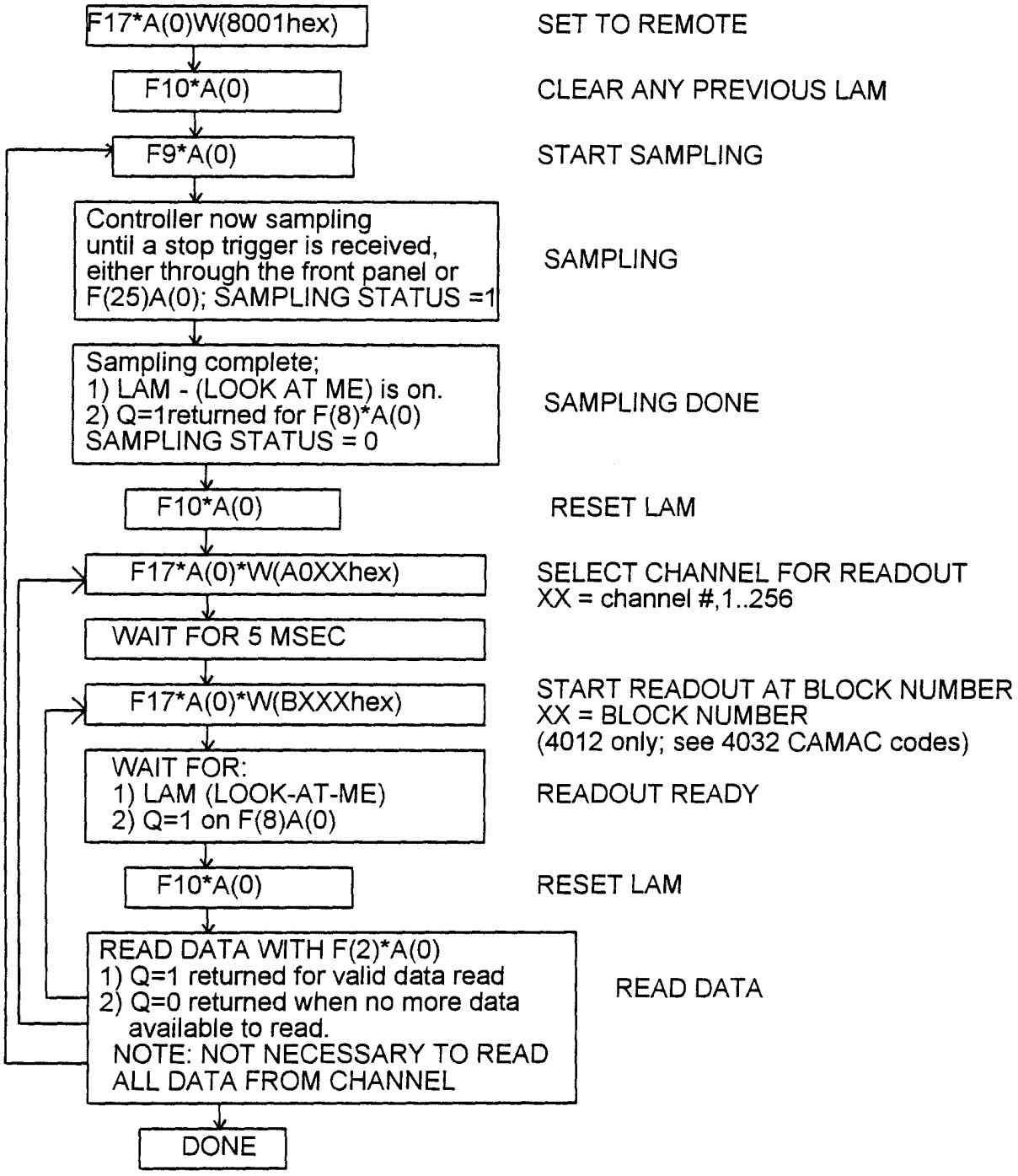
Control registers are programmed using the F(17)*A(0) command and W16-W1 CAMAC write lines. The W16-W13 lines address the control registers and W12-W1 contain the data to be loaded.

If the 4012/4032 controller is in the local control mode, only the local/remote (see 8 below) register can be changed. After commanding the unit to the remote mode all registers can be changed. As new values are programmed into the controller, the new values/functions are displayed on the front panel LEDs.

Since all command registers are read/written through the microprocessor there is a response time of approximately several hundred microseconds. The controller will respond with a Q=1 on F17*A(0) [F(0)*A(0)] if the unit is ready to accept (read) the command (data), otherwise a Q=0 is generated. When reading the control registers, which requires F(17)*A(0) to be followed by F(0)*A(0), both commands must be executed before the next F(17)*A(0) can be generated. It is recommended that a minimum of 500

μsec delay be inserted between all commands which address the 4012 control registers. This applies for F (17), F(0), and F(9) commands.

Controlling Sampling and Data Readout From CAMAC



SECTION 5
WRITING COMMON 4012/4032 CONTROL REGISTERS

F(17)*A(0)*[(W16..W13 = Command) **(W12..W1** = Data)]

> **NOTE**
> COMMAND = upper 4 write bits (W16..W13) in hex
>
> DATA = lower 12 write bits (W12..W1) in decimal

Function	Command	Data	Description
SET NUMBER OF ACTIVE CHANNELS	1	1 , 2, 4,... 256	1=1 active ch. 2=2 active ch. : 256= 256 active ch. **NOTE** Do not program more active channels than the total number of ADC channels, otherwise the controller will always be waiting for a "conversion complete" signal from the erroneous channels

SET NUMBER OF POST-TRIGGER FRACTION SAMPLES	2	0,1,2,...8	0 = No post-trigger samples -sampling , stops immediately after receipt of the "stop trigger". 1 = 1/8 of the channels memory is sampled after receipt of "stop trigger" 2 = 2/8 of the channels memory is 3 = 3/8. ... 8 = all data is recorded after receipt of "stop trigger"

SET CLK1 FREQUENCY	4	0,1,...17	0 = 5 MHz 1 = 2 MHz 2 = 1 MHz 3 = 500 Khz 4 = 200 Khz 5 = 100 Khz 6 = 50 Khz 7 = 20 Khz 8 = 10 Khz 9 = 5 Khz 10 = 2 Khz 11 = 1 KHz 12 = 500 Hz 13 = 200 Hz 14 = 100 Hz: 15 = 50 Hz 16 = 20 Hz 17 = 10 Hz **NOTES** 1. If using FTRG and FTRIG is TTL high or a "stop trg" has been detected using STRG then CLK2 will be active. 2. Do not set CLK1 frequencies higher than the maximum conversion rate of the ADC modules.

SET CLK2 FREQUENCY	5	0,1,..17	Same as CLK1 **NOTES** 1. The W16 data bit is set to 1 (if enabled) for data sampled when CLK2 is active- see DATA FORMAT section 2. Do not set CLK2 frequencies higher than the maximum conversion rate of the ADC modules or the maximum transfer rate of the bus
SET CLOCK SWITCHING CONTROL	6	0,1,2	0 = No switching from clock 1 to clock 2 1 = Switch from clock 1 to clock 2 when front panel input signal "CLK SWI" is high [FTRG] 2 = Switch from clock 1 to clock 2 when "STOP TRG" received [STRG]
SET CLOCK CONTROL	7	0,1,2	0 = Both external and internal clocks are disabled. 1 = External clock (front panel input signal) is enabled; internal clocks are disabled. 2 = Internal clocks are enabled and the external clock input is disabled.

SET LOCAL REMOTE CONTROL	8	0,1	0 = Set to local control mode 1 = Set to remote control mode **📖 NOTE** If the controller is in the local control mode the computer may override and set to remote mode. This is required in order to set any other control registers or read data. Also, the LOCAL/REMOTE can be changed from the front panel
SET THE D/A OUTPUT DISPLAY CHANNEL	9	1, 2, 3, 4,5, ... 256	[Data(decimal):] 1 = display channel 1 2 = display channel 2 ... 256 = display channel 256 Displays data from the selected channel, **(see "DISPLAY OUT," SIGNALS section).** **📖 NOTE** Do not program a display channel greater then the number of active channels. If the controller is in the data readout mode then the display can be reactivated by reading out the last block of data in a channel until Q=0 is returned on the 1025th read cycle.

SELECT A CHANNEL FOR READOUT 1,2,3,4,5...256	A	1, 2, 3, 4,5, ... 256, 512... 514	[Data(decimal):] 1 : Select channel 1 for readout 2 : Select channel 2 for readout . 256 : Select channel 256 for readout 512 : DATA STREAMOUT 513 : DATA STREAMOUT WITH AUTO RESTART 514 : MEMORY DUMP **NOTE** This command must be executed at least once before data readout can begin. It is not necessary to re-issue the command if the channel readout number is not changed. Do not program a channel number greater than the active number of channels.

Data Streamout

If the channel number = 512 then the controller will immediately enter the data streamout mode. Data is ready to read approximately 1.5 msec after issuing the command. This mode is useful for users who wish to read all TRAQ data without the overhead of setting up each channel and starting address (app. 3 msec). This mode reads data out in the following the following sequence:

Channel(NOC), Sample(1)

Channel(NOC-1), Sample(1)

.

.

Channel(1), Sample(1)

Channel(NOC), Sample(2)

Channel(NOC-1), Sample(2)

.

Channel(1), Sample(2),

etc.

Data Streamout with Auto-restart

This mode allows the controller to continuously sample/read/sample... data. After the controller is commanded into this mode it will automatically enter the data readout mode after sampling is complete. The data is read in the same format as above. After the last data sample + 1 is read the Controller will automatically restart sampling. This mode is enabled until the channel readout number is changed from 513.

Data Dump: The entire memory is readout starting at address 0.

SET MODE 1 REGISTER	C	1,2,4,... 128	1 = ACQUISITION MODE = DATA 2 = ACQUISITION MODE = CALIBRATE (4012P only) 4 = ARM UNIT (P units only) 8 = STOP SAMPLING 16 = RUN 4012A CODE 32 = RUN 4012P CODE 64 = ENABLE CALIBRATION MEMORY 128= DISABLE CALIBRATION MEMORY (64,128 only for 4012P)

🕮 NOTES

Acquisition mode = data is the standard transient capture mode and is the default on power-up.

Acquisition mode = calibrate will transfer 2k samples/ channel to the reserved memory after data is acquired.

Arm is the computer equivalent of the front panel MASTER ARM and must be (if in remote mode) before the Controller will accept the F(9) command start digitizing.

Stop Sampling - This command will cause the controller to stop sampling immediately; executing the following:

a) The internal or external clock is immediately stopped.

b) The controller waits approximately 100 μsec after disabling the clocks to allow all ADC converters to finish converting data.

c) The number of post-trigger samples is read by the controller.

If there have been no post-trigger samples (no stop trigger) then the earliest sample digitized is assumed to reside at the beginning of memory. The total number of samples converted is equal to the memory address of the last sample stored.

🕮 NOTE

This will not be true if the memory address counters have wrapped around one time. It is advisable to use the forced stop mode only in all post-trigger mode. The user should be sure that a trigger is received before issuing this command.

If a stop trigger was received the total number of samples converted is equal to the number of programmed pre-trigger samples plus the number of post-trigger samples actually converted.

a) The number of samples converted is stored in registers for readout. (see W=16, W=17 under READING THE CONTROL REGISTERS)

b) If no post-trigger samples were recorded then a flag bit is stored to notify the user that no stop trigger was received. (see W=14 under READING THE CONTROL REGISTERS)

Run 4012A (4032A) code assumes the unit is a 4012A controller, 4012P a 4012P controller.

Enable/disable calibration memory reserves a 128K memory block for the calibration data.

SECTION 6
MODEL 4012 CONTROL REGISTERS ONLY

Function	Command	Data	Description
SET MEMORY/ CHANNEL	3	1...4095	Set memory/channel in 1024K sample increments. The minimum memory/channel is 1K and the maximum is determined by the number of active channels(NOC) and the total memory size or 4095 increments (4,193,280 samples/channel). Maximum memory/channel = NOC * integer(MSTO/NOC) where: NOC = NUMBER OF ACTIVE CHANNELS (1,2,4,6...256) MSTO = TOTAL MEMORY SIZE (128K,256,...) MSTO is determined during the power-up diagnostic sequence. The 4012 will default to the maximum memory/channel for any value out of bounds.

START DATA READOUT ADDRESS	B	1...4095	[Data(decimal):] 0= Start readout at earliest sample digitized 1 = " " " " " +1024 2 = " " " " " +2048 . N-1 " " " the last 1K memory block (N= MEMORY/CHANNEL ,1K BLOCKS; N(max) = 4095 blocks (sample 4,193,280).

🕮 NOTE

The 4012 will not respond to this command unless the unit is both in the remote mode and sampling is complete. Data readout will start approximately 500 μsec. after receipt of this command. A LAM will be generated when data is ready for readout.

The LAM should be reset ,F(10)*A(0), before readout begins. A Q=1 on F(2)*A(0) will be generated for valid read data. A Q=0 on F(2)*A(0) will be generated after all data from the selected channel has been read. Also, the 4012 will be in the display mode (front panel "DISPLAY OUT" active) until this command is received and will return to the display mode after the last 1K block of data has been read from the channel. It is not necessary to read all data from the channel before reading another channel or skipping to some other 1K data block.

SAVE CONTROL REGISTERS	D	0	All control settings are saved in the non-volatile memory and used as control parameters on power-up. The 4012 contains a non-volatile memory chip. The chip will retain the control parameters indefinitely but has a limited number of SAVE cycles (approximately 1000).
RESTORE CONTROL REGISTERS	E	0	Restores the control settings using the values stored in non-volatile memory. This is done automatically on power-up.
INITIATE POWER-UP DIAGNOSTIC TESTS	F	0	Allow approximately 3 seconds to execute. This test will reset the system (same as power-up). If using the 4012P firmware mode (see **SET MODE REGISTER (12)**) this test will NOT exercise TRAQ memories which would write overwrite data.

SECTION 7
4032 CONTROL REGISTERS ONLY

SET MEMORY/ CHANNEL LOWER	3	1...4095	Set lower 12 bits of the total Memory/Channel.
SET MEMORY/ CHANNEL UPPER	D	1...4095	Set upper 12 bits of the total Memory/Channel.

To set the 4032's MEMORY/CHANNEL requires using both:

a) **SET MEMORY/CHANNEL LOWER**

b) **SET MEMORY/CHANNEL UPPER**

SET MEMORY/CHANNEL UPPER and **SET MEMORY/CHANNEL LOWER** combine to form the full MEMORY/CHANNEL (1k blocks) .

1) Use **SET MEMORY/CHANNEL UPPER** to set the upper 12 bits of MEMORY/CHANNEL

2) Use **SET MEMORY/CHANNEL** to set the lower 12 bits of MEMORY/CHANNEL

🕮 NOTE

SET MEMORY/CHANNEL UPPER must always be programmed first and always followed by **SET MEMORY/CHANNEL LOWER**

☑ EXAMPLE

Set MEMORY/CHANNEL to 8,389,632 Samples/Channel

1) 8,389,632/1024 = 8193 (hex 2001) blocks of 1024 samples

2) Int[8193/4096] = 2 (Data for **SET MEMORY/CHANNEL UPPER**)

3) 8193-2*4096 = 1(Data for **SET MEMORY/CHANNEL LOWER**)

🕮 NOTE

Maximum memory/channel = NOC * integer(MSTO/NOC) where:

NOC = NUMBER OF ACTIVE CHANNELS (1,2,4,6...256)

MSTO = TOTAL MEMORY SIZE (128K,256,...)

MSTO is determined during the power-up diagnostic sequence. The 4032 will default to the maximum memory/channel for any value out of bounds.

START DATA READOUT ADDRESS LOWER	B	1.. 4095	Set lower 12 bits of the data channel readout block.
START DATA READOUT ADDRESS UPPER	E	1.. 4095	Set upper 12 bits of the data channel readout block.

To set the starting readout block number requires using both the

a) START DATA READOUT ADDRESS LOWER

b) START DATA READOUT ADDRESS UPPER

START DATA READOUT ADDRESS UPPER and **START DATA READOUT ADDRESS LOWER** combine to form the full start of data readout address (1k blocks) .

1) Use **START DATA READOUT ADDRESS UPPER** to set the upper 12 bits of the start address.

2) Use **START DATA READOUT ADDRESS LOWER** to set the lower 12 bits of start address.

🕮 NOTE

START DATA READOUT ADDRESS UPPER must always be programmed first and always followed by **START DATA READOUT ADDRESS LOWER.**

☑ EXAMPLE

Set start of readout to sample 8,389,632..

1) 8,389,632/1024 = 8193 (hex 2001) blocks of 1024 samples

2) Int[8193/4096] = 2 (Data for **START DATA READOUT ADDRESS UPPER**)

3) 8193-2*4096 = 1(Data for **START DATA READOUT ADDRESS LOWER**)

🕮 NOTE

The 4032 will not respond to this command unless the unit is both in the remote mode and sampling is complete. Data readout will start approximately 500 μsec. after receipt of this command. A LAM will be generated when data is ready for readout.

The LAM should be reset ,F(10)*A(0) before readout begins. A Q=1 on F(2)*A(0) will be generated for valid read data. A Q=0 on F(2)*A(0) will be generated after all data from the selected channel has been read. Also, the 4012 will be in the display mode (front panel "DISPLAY OUT" active) until this command is received and will return to the display mode after the last 1K block of data has been read from the channel. It is not necessary to read all data from the channel before reading another channel or skipping to some other 1K data block.

SET MODE 2 REGISTER	F	1,2,3	1 = SAVE CONTROL REGISTERS 2 = RESTORE CONTROL REGISTERS 3 = INITIATE POWER-UP DIAGNOSTIC TESTS

SAVE CONTROL REGISTERS: All control settings are saved in the non-volatile memory and used as control parameters on power-up. The 4012 contains a non-volatile memory chip. The chip will retain the control parameters indefinitely but has a limited number of SAVE cycles (approximately 1000).

RESTORE CONTROL REGISTERS: Restores the control settings using the values stored in non-volatile memory. This is done automatically on power-up.

INITIATE POWER-UP DIAGNOSTIC TEST: Allow approximately 3 seconds or more to execute. This test will reset the system (same as power-up). If using the 4012P firmware mode (see **SET MODE REGISTER (12)**) this test will NOT exercise TRAQ memories which would write overwrite data.

SECTION 8
READING THE 4012/4032 CONTROL REGISTERS

F(0)*A(0)*R(R16..R1)

Control registers can be read at any time, either in remote or local control mode. The registers are read using a two step command process:

1) Address the register with F(17)*A(0)*W(register address) which causes the TRAQ processor to fetch the register data.

2) Read the register data with F(0)*A(0)*R(register data).

If the TRAQ controller is available to accept the F(17)*A(0) command, a Q=1 will be returned. The data to be read will be available within 500 μsec and should be read by the F(0)*A(0) command within 1 sec after F(17)*A(0). The controller will not respond for one second to any other CAMAC command while waiting for F(0)*A(0) to read the control register.

🕮 NOTE

In the table below:

W corresponds to the **W** data (decimal) in the F17 command: F(17)A(0)**W(W16-W1)**

R corresponds to the **R** data (decimal) in the F0 command: F(0)A(0)**R(R16-R1)**

CMD corresponds to the previous sections **COMMAND** value (hex).

Description	W	R	CMD
READ NUMBER OF ACTIVE SIGNAL CHANNELS	1	1,2..256	1
READ POST-TRIGGER SAMPLES	2	0,1,2..8	2
READ CLOCK 1 FREQUENCY	4	0,1,2,,17	4
READ CLOCK 2 FREQUENCY	5	0,1,2,,17	5
READ CLOCK CONTROL	6	0,1,2	6
READ CLOCK SWITCH. REG.	7	0,1,2	7
READ LOCAL/REMOTE STATUS	8	0,1	8
READ DISPLAY CHANNEL	9	1,2,,256	9
READ DATA CHANNEL TO BE READ	10	1,2..256	A
RESERVED	13		

READ STATUS	14							
	READ(R8-R1) (BINARY)							
Description	8	7	6	5	4	3	2	1
4012 NOT sampling	x	x	x	x	x	x	x	**0**
4012 sampling	x	x	x	x	x	x	x	**1**
Data acquisition mode	x	x	x	x	x	x	**0**	x
Calibration acquisition mode	x	x	x	x	x	x	**1**	x
4012P/4032P not master armed	x	x	x	x	x	**0**	x	x

4012P/4032P master armed	x	x	x	x	x	**1**	x	x
4012P/4032P not master enabled	x	x	x	x	**0**	x	x	x
4012P/4032P master armed enabled	x	x	x	x	**1**	x	x	x
Stop trigger received before EOC	x	x	x	**0**	x	x	x	x
Stop trigger not received before EOC	x	x	x	**1**	x	x	x	x
4012 (4032) not triggered	x	x	**0**	x	x	x	x	x
4012 (4032) triggered	x	x	**1**	x	x	x	x	x
4012P (or 4032P) code running	x	**0**	x	x	x	x	x	x
4012A (or 4032) code running	x	**1**	x	x	x	x	x	x
Calibration memory not enabled	**0**	x	x	x	x	x	x	x
Calibration memory enabled	**1**	x	x	x	x	x	x	x

🕮 NOTE

1) The 4012 will turn the LAM on when sampling is complete in the remote mode.

2) In calibration mode the 4012 will store 2k/samples per channel in the reserved calibration section of memory after data acquisition.

3) Stop trigger received before EOC: This status flag should be monitored when using the Stop Sampling Command. (See 12 under Writing the 4012 CONTROL REGISTERS.)

Reserved	15
Read Number of Samples Converted, Lower Word R16-R1	16
Read Number of Samples Converted, Upper Word R16-R1	17

Read the total number of samples converted. This command is used when sampling has been forced to stop (see **WRITING CONTROL REGISTERS).** Returns the TOTAL number of samples converted:

TOTAL samples converted = NOC * samples

therefore if 1000 samples have been taken and Number Of Channels = 6 then the total samples converted is 6000.

TOTAL samples converted = 65536 * (UPPER WORD) + LOWER WORD

NOTE

TOTAL samples converted can be greater than (record length * NOC) if no stop - trigger was received and the samples converted are greater than the record length.

Reserved	15
Read Number of Samples Converted, Lower Word R16-R1	16
Read Number of Samples Converted, Upper Word R16-R1	17

Read the total number of samples converted. This command is used when sampling has been forced to stop (see **WRITING CONTROL REGISTERS**). Returns the TOTAL number of samples converted:

TOTAL samples converted = NOC * samples

therefore if 1000 samples have been taken and Number Of Channels = 6 then the total samples converted is 6000.

TOTAL samples converted = 65536 * (UPPER WORD) + LOWER WORD

NOTE

TOTAL samples converted can be greater than (record length * NOC) if no stop - trigger was received and the samples converted are greater than the record length.

Model 4012 Only

Read Memory/Channel (1k Blocks)	3	1,2..	3
Read Start ADDR OF DATA (1k Blocks)	11	1..4095	B
Read TRAQ Total Memory Size	12	128=128K 256=256K, etc.	C

Model 4032 Only

(UPM) Upper Read Memory/Channel	18		D
(LPM) Lower Read Memory/Channel	19		

NOTE

Total Memory/Channel (1k blocks) = 65536*UPM+LPM

(TTMSU) : Read Total TRAQ Memory Size Upper	20		
(TTMSL) : Read Total TRAQ Memory Size Lower	21		

NOTE

Total TRAQ Memory Size (1k blocks) = 65536*TTMSU+TTMSL

(SADU): Read Start Addr of Data Upper	22		E
(SADL): Read Start Addr of Data Lower	23		B

🕮 NOTE

Start Address for Data Readout (1k blocks) =

65536*SADU+SADL

SECTION 9
DIAGNOSTICS

During the power-up sequence the TRAQ microprocessor runs a series of diagnostic tests. Failure to pass these tests implies the system is not functional. If a test does not pass a message will be displayed on the **"value"** LED display while the **"function"** LED displays the **TEST** being performed. For most of the test, the controller will continually loop through the failed test to facilitate oscilloscope probing of the failed circuitry. To restart the testing sequence hit the reset button or issue CAMAC Z (or C) commands. The tests are performed sequentially as listed below.

NOTE

In the following discussions the 4012-01 board is on the left side (as viewed from the front) and the 4012-02 (processor board) is the board on the right. The 4012-03 is the front panel board. Also, 4012P units do not use the MEM2 and MEM4 tests as stored data would be erased after power-up.

Value LED:	**Function LED:**
No Display	
Test Description:	
Either the 4012-02 board has no +6V power, the 4012-03 is not connected to the 4012-02, or there is some failure on the 4012-02 (such as a bad PROM, RAM, etc.) that is inhibiting the processor from initializing.	
Check:	
Check 4012-02 and 4012-03 connections, 4012-02 fuses. Or generate repetitive CAMAC Z(or C) cycles and probe the T.I. 9995 address/data lines for correct logic states. Immediately after reset, the processor will access the RAM memory (starting at location A000, hex) - check for memory access signals.	

Value LED:	Function LED:
RAM	Fail

Test Description:

The processor writes an alternating 1010... and 0101... pattern into the onboard static RAM and attempts to read it back.

Check:

The processor writes an alternating 1010... and 0101... pattern into the onboard static RAM and attempts to read it back.

Value LED:	Function LED:
INTP	Fail

Test Description:

The processor sets-up the 9519 interrupt control chip, fires interrupt #7 (internally) and checks the 9519's interrupt status register for interrupt #7.

Check:

Failure implies either a bad 9519 IC or bad connections to the chip. Since a message is being displayed, the processor and associated bus circuitry are probably O.K. Probe pin 1 of 1L (9519) for chip select. Also, check for wr(write) and rd(read).

Value LED:	Function LED:
L646	Fail

Test Description:

This is the first test that checks board interconnections, the state of the 4012-01 board and the TRAQBUS. The processor loads a pattern (AAAA 5555, hex) into the LS646s (6H-9H) on the 4012-01 board and then reads the pattern back.

Check:

1) Remove the cable from the 50 pin TRAQBUS connector and restart the test. If the test passes, the problem is either a bad TRAQBUS cable or a bad memory module which is generating data on the bus when not addressed.

2) Check all fuses on the 4012-01 board and the interconnection cable between the 4012-01 and 4012-02

3) If the test still fails, this indicates a component failure on the 4012-01 or 4012-02 board. The 4012-01 has three data busses:

   4) A 32-bit data bus (IB31-IB0); main data bus

   5) A 16-bit data bus (MD15-MD0); CAMAC data bus

   6) A 8-bit data bus (PD7-PD0); μ-processor data bus

Communication between the microprocessor the IB bus is through the CAMAC MD bus; i.e., μ-processor - CAMAC - data bus

After data bytes are latched into the LS646 B latches they are transferred to the A latches and then read back through the same data paths. Any problems on the TRAQBUS will show up during the LS646 B to A transfer. To check the data in the LS646 latches, trigger a scope on pin 9H(1), the signal which transfers the data in the latches. Check 6H(4 to 11),7H(4-11),etc. for the AAAA 5555 pattern. Failure of the pattern at this point implies either bad signal levels on the PD, MD, or IB bus, defective ICs or bad enable, latch signals to the data path chips.

Value LED:	Function LED:
LPTS	Fail

Test Description:

Loads a 32-bit pattern (AAAA 5555, hex) into the 32-bit PTS counter and reads the pattern back.

Check:

Since the "L646" test passed the data bus, connections between the 4012-01 and 4012-02 board are OK. Also, the IB, MD, and PD bus are OK. The transfer of data bytes to/from the microprocessor is the same as the "L646" test except data is latched into the PTS counters, not the LS646s. Data is transferred to internal 8-bit latches by strobing the LO-DMA-CNT line. Data is then read when RD-PTS-CNT line goes low (4 times to read 4 bytes).

Value LED:	Function LED:
ADDR	Fail

Test Description:

Loads a 32-bit test pattern (AAAA 5555) into the 32-bit address counter. This counter can auto-skip address in increments of 1 to 255 under hardware control only. It is used to readout the data for display or CAMAC.

Check:

The previous tests have checked the IB and other data busses. Therefore, any problems are probably associated with internal chip problems.

Value LED:	Function LED:
ADIN	Fail

Test Description:

Loads a 1 into the address counters, increments the address counters 8 times and reads the resulting address back. Then repeats the test starting at address FF (hex), FFFF (hex) and FF FFFF (hex)..

Check:

Failure of this test usually implies a problem with the address auto-incrementer.

Value LED:	Function LED:
ADAU	Fail

Test Description:

Loads zero into the address counters, 128 into the auto-skip register and checks for correct auto-incrementing of the address counters after generating address strobes. The test is performed 32 times (addresses 0 to 4096, in increments of 128). The addresses are read and checked after each of the 32 address strobes.

Check:

Since test "ADDR" has passed, this test should only fail due to a faulty auto-increment register or faulty overflow logic from counters.

Value LED:	Function LED:
ADOV	Fail

Test Description:

Loads FFFF FFFE (hex) into the address counters, increments two times and checks for overflow reset (address =0). The address overflow counter is used to reset the memory modules' internal address counters to zero after the end of memory has been reached during writing or reading. This counter is incremented each time counter (counts in 64K increments) and reaches its terminal count when the memory space is exhausted. The overflow triggers a 50 nsec. reset pulse, which resets the controller and memory module internal address counters. On the first address cycle the addresses increment to FF FFFF, hex, and the next address cycle causes the overflow to reset the address counters and reload.

Check:

Since the address counters have passed the three previous tests, any problems should be associated failed ICs.

Value LED:	Function LED:
PTIN	Fail
Test Description:	
Loads a 1 into the PTS counters, increments the counters 8 times and reads back the data. Repeats the same test starting with an initial count of FF, FFFF, and FF FFFF (hex).	
Check:	
Since the "LPTS" test passed this test should only fail due failed ICs.	

Value LED:	Function LED:
PTOV	Fail
Test Description:	
Loads FFFF FFFE (hex) into the PTS counters, increments one time and checks for interrupt #3 on. When the PTS counters. reach the terminal count of FFFF FFFF(hex), the DMARCO goes low which in turn generates interrupt #3 to the 4012-02 board.	
Check:	
Since the PTS counters have passed the "LPTS" and "PTIN" tests the only problems should be due to faulty overflow circuitry.	

Value LED:	Function LED:
MEM1	Fail
Test Description:	

This is the first test for the memory modules. At this point all of the 4012-01 diagnostics have passed. This test performs the following functions:

1) Determines how much memory is on the TRAQ bus.

Checks that interrupt #6 in generated when the memory module returns the DARDY signal.

The 4012 assumes that there is at least 128K words of memory on the bus and will fail the test if no memory module responds with a DARDY, when address FFFF (hex)is addressed. The modules are organized as 32-bit words and each module's internal address counters range from FFFF-0000, hex. This is equivalent to 64 K, 32-bit words or 128K of 16-bits words. The test proceeds as:

1) Address 0000 FFFF is loaded into the memory modules.

2) A data cycle (DACYC) is generated.

3) The processor looks for interrupt #6 on.

If interrupt #6 is not on after the first DACYC, the test fails as either no memory is present or there are logic problems.

If interrupt #6 is on, the address is incremented by 64K (i.e. to 1 FFFF, hex) and loaded into the memory module, which generates a DACYC. This continues unless a DARDY is not returned signifying no more memory is present.

Check:

Check the I.D. switches on the memory modules. One of the units must have I.D.= 0. Also check the TRAQ bus cable. If the test still fails, set another module on the bus to I.D.= 0 (set the original modules' I.D. = 7) and rerun the test. If the test now passes, the original module was faulty. If the test still fails, probe the DARDY signal on the 4012, sheet 2. DARDY is an open collector signal so if any module is faulty, the line could be held down.

Value LED:	Function LED:
MEM2	Fail

Test Description:

This test writes the address of the first word in each 32 bit, 64k memory block on the TRAQ bus, i.e. the word at location 0000 is loaded with 0000 and then checked. The word at address 1 0000 (hex) is loaded with 1 0000 and then checked, etc. This is a very rough memory test to quickly see if there are any gross memory failures. This test will usually pickup any bad memory chips that are totally failing.

Check:

Check which memory module has it SEL LED on. This is where the failure is occurring. Probe the data lines (synchronizing with DARDY to locate the bad memory chip).

Value LED:	Function LED:
MEM4	0,1,2,....

Test Description:

This is the final diagnostic test and tests all the memory on the TRAQ bus in 1k block increments. Data is written into memory using the address counters in the 4012-01. A 1 MHz clock is used to write the data. After the memory block is written, the processor reads and checks every 64th memory location. If the test fails, the processor will remain in a loop writing/reading at the block that failed. The value displayed on the LEDs is the block being tested.

Check:

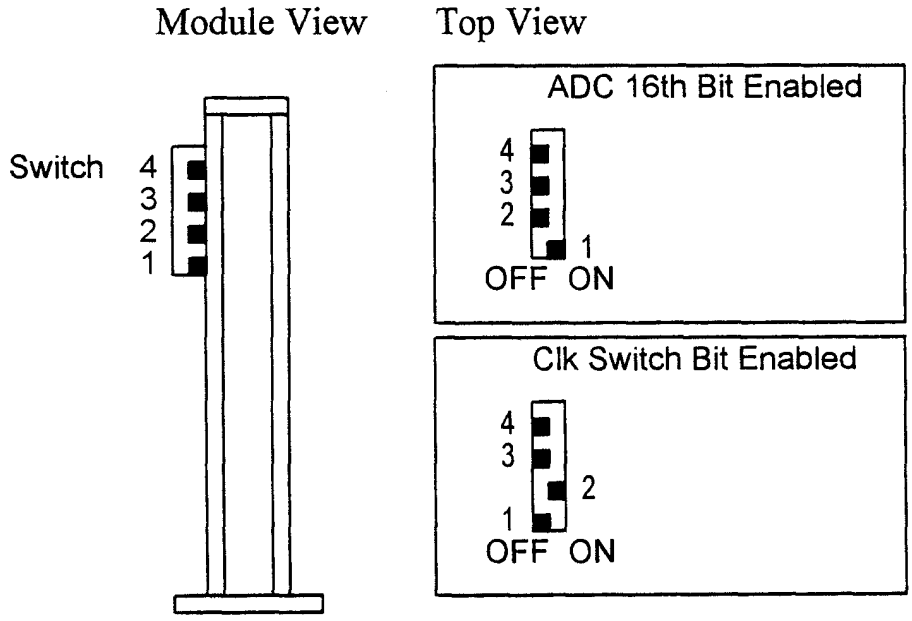
Check that the 1 MHz clock is working. If no clock is present, check the clock circuitry on the 4012-02 board. Otherwise, check the module for faulty logic or a bad memory locations.

SECTION 10
SWITCH OPTIONS

CLK2 16th Bit Set

The 4012/4032 is normally delivered with the 16th data bit set to the CLK2 status detect line. Whenever CLK2 is active the 16th bit of the data will be set to one (1). This option can be defeated by changing the switch settings on the 4012-01 board. This switch is accessible at the top of the module, left side.

This allows the 16th data bit from the signal channels to be stored in memory.



Installation of TRAQ Firmware

Firmware for the 4012/4032 is programmed into two 64k EPROMs which can be field upgraded by installing new EPROM chips into the control board. Occasionally DSP may send out new revisions of this software. To install the new EPROMs place the unit on a table with the front panel facing you and:

1) Remove the back panel and open the unit (it may be necessary to remove the right side panel).

2) Remove the 28-pin integrated circuits in sockets E1 and E2 which are located at the top of the right side printed circuit board. The I.C. will have a revision number on it such as REV 1.10. Be sure to note the orientation which has pin 1 facing the rear of the module.

3) Install the new EPROMs in the same sockets with the same orientation.

4) Close the unit and remount the rear panel.

5) Install the unit in the crate and turn the power on. After diagnostics are complete the new revision number should be displayed.

6) If the unit does not power-up properly check for bent pins or incorrect installation of the EPROMs.

SECTION 11
SERIES 5000
MEMORY MODULES

General Description

Models 5004,...5432 and up are high density memory modules which store data from the TRAQ 4012/4032 controllers.

Memory in the units is organized as 32-bit words. The units can write/read data at a maximum rate of 8.0 Megasamples/second (a sample is a 16 bit data word). The maximum number of modules on the bus is limited to 8 or the maximum allowed memory size (16 Megasamples for 4012 controllers; or 256 Megasamples for 4032 controllers). All communication with the memory module is through the front panel TRAQBUS connector; the CAMAC connector supplies power only. The TRAQBUS is a multiplexed address/data bus with the ability to write/read data up to 8.0 Megasamples/second. The memory consists of dynamic RAMS with on board refresh control or static rams (Model 5200 only).

Front Panel Indicators and Controls

LED Indicators

ADCY	Momentary LED. Indicates that an address cycle has been generated.
DACY	Momentary LED. Indicates that a data cycle has been generated.
RFCY	Momentary LED. Indicates that memory refresh cycles are being generated.
RFEN	Indicates that refresh cycles are enabled **NOTE** RFCY & RFEN should be on when the module is not connected to the TRAQBUS

WRITE	Indicates that the module is enabled for writing data to memory (when the LED is on) or reading to the Controller (when the LED is off).
SEL	Indicates that the module is selected for reading/writing. Only one memory module is selected at a time
ID3-ID0	Indicates the position of the module ID switches.
WRITE LOCK	Indicates that the memory cannot be over-written. (5200 series only)

Module ID Switches

ID3,ID2,ID1,ID0:

🕮 NOTES

1) Some 500x module have only 2 or 3 ID switches

2) The following discussion assumes:

   a) Only one type of memory module used (for example - multiple 5004 modules); consult the factory for ID switch settings if you need to mix different types of modules (example - 5005 and 5004).

   b) Memory modules are installed immediately to the left of the controller.

Four switches which set the module identification number. The ID LEDs are on when the switch is in the "on" position. Up to 8 memory modules can be installed on the TRAQBUS and these switches determine which module will be "module 0," "module 1," etc. The ID switches must be set so that one module has ID zero, one module ID one, (up to the number of installed modules -1).

ID	ID3	ID2	ID1	ID0	Use this setting for module:
0	off	off	off	off	Module directly to left of controller
1	off	off	off	on	2nd memory module to left of controller
2	off	off	on	off	3rd memory module to left of controller
3	off	off	on	on	4th memory module to left of controller
4	off	on	off	off	5th memory module to left of controller
5	off	on	off	on	6th memory module to left of controller
6	off	on	on	off	7th memory module to left of controller
7	off	on	on	on	8th memory module to left of controller
8	on	off	off	off	**NOTE** **Following ID's are used when mixing different memory model types (consult factory)**
9	on	off	off	on	
10	on	off	on	off	
11	on	off	on	on	
12	on	on	off	off	
13	on	on	off	on	
14	on	on	on	off	
15	on	on	on	on	

Anytime modules are added to the TRAQ system or ID numbers changed, the controller should be reset or re-powered to initiate diagnostics.

Input Signal (5200 Series Only)

Write Lock

TTL signal, LEMO type input connector, internally pulled-up to 5 Volts by a 10 Kohm resistor. Whenever the Write Lock input signal (WLIS) is driven to a TTL low, the memory cannot be overwritten with new data. When power is applied to the module an internal signal generates a write lock. As the controller starts its power-up diagnostics it will reset the internal write lock unless the WLIS signal is present. The presence of the WLIS will always prohibit overwriting the memory.

SECTION 12
TRAQ DIGITIZER MODULES

TRAQ data acquisition is performed by modular Analog-to-Digital Converters (ADCs). These modules include the 8 channel, (100 KHz DSP 2812), 4 channel (1 MHz DSP2860) and others. Multiple modules may be connected to form a multichannel (256 maximum) system. Features common to all DSP data acquisition modules are:

1) High Resolution

2) Simultaneous Sampling

3) Fully Independent Channels

4) Modularity

Each channel is fully independent, incorporating an individual fully differential amplifier, track and hold, and ADC. This allows any or all channels to be used simultaneously at a constant data acquisition rate.

TRAQ Digitizer Module Specifications

Model	2812	2814	2840	2860	2824
Sampling Rate (KiloSamples/Sec)	100	100	1000	1000	2000
Number of Channels	8	4	4	4	1
Maximum Channels/Controller at maximum Sampling Rate	80	80	8	8	4
Resolution (bits)	12	14	14	12	12
Input Voltage Range (Volts)	± 5	± 10	± 10	± 5	± 5
Input Impedance (ohm)	100K	100K	100K	100K	100K
Bandwidth (0.5dB)(Hz)	50K	50K	500K	500K	500K
Bandwidth (3dB)(Hz)	100K	100K	1M	1M	1M
CMRR (dc-100 Hz)dB	80	80	94	72	80
CMVR (Volts)	±12	±12	±20	±12	±12
Input Protection (dc) (Volts)	±50	±50	±100	±50	±50
DC Gain Error (%)	±0.1	±0.1	±0.1	±0.1	±0.1
DC Offset Error (% of FS)	±0.1	±0.1	±0.1	±0.1	±0.1
Integral Non-Linearity (LSB)	±0.5	±0.5	±0.5	±0.5	±0.5
Differential Non-Linearity (LSB)	1	1	1.5	1	1
Aperture Delay (Nsec)	<15	<15	<15	<15	<15
Channel-Channel Time Skew	<100	<100	<100	<100	<100

Temperature Range

Operational: 10 - 55°
Storage: -5 - 85°

Front Panel Description

LED Indicators

ADCY	Momentary LED. Indicates that an address cycle has been generated.
CVT	Indicates module is performing analog to digital conversions. The indicator will appear to be continuously on for sampling rates greater than 10 samples per second.
SEL	Indicates module is currently selected for data transfer from the internal data buffer. The indicator will appear to be continuously on for rates greater than 10 samples per second.
ID3-ID0	Indicates module identification number (module address) as determined by MODULE ID switches.

Module ID Switches

Four switches which set the module identification number. The ID LEDs are on when the switch is in the "on" position. Up to 16 ADC modules can be installed on the ADCBUS and these switches determine which module will be "module 0," "module 1," etc. The ID switches must be set so that one module has ID zero, one module ID one, (up to the number of installed modules -1).

Data Acquisition module IDs must be set according to the following rules:

1)

Module ID Switch Settings:					**Channel Numbers:**				
ID	**ID3**	**ID2**	**ID1**	**ID0**	**2812**	**2814**	**2840**	**2860**	**2824**
0	0	0	0	0	1-8	1-4	1-4	1-4	1
1	0	0	0	1	8-16	5-8	5-8	5-8	2
2	0	0	1	0	17-24	9-12	9-12	9-12	3
15	1	1	1	1	120-128	60-64	60-64	60-64	16

2) A module with an ID = 0 must be present in the system.

3) Module IDs must be contiguous (i.e., no gaps in channel numbers are allowed).

4) Module IDs must be unique (i.e., no modules with identical channel numbers are allowed).

NOTE

The physical placement of modules on the TRAQ bus is not restricted.

Input Signal Connectors

Differential input signal connectors mate with:

LEMO - F0.302 NYL U/3.7 or equivalent.

Bipolar/Unipolar Input Option

All digitizer modules are delivered and calibrated in the bipolar input mode. Some modules have internal jumpers for unipolar mode.

NOTE

Internal jumpers are not computer readable.

Model	2812	2814	2840	2860	2824
BIPOLAR MAX VOLTAGE	+4.998	9.9988	9.9988	+4.998	+4.998
BIPOLAR MIN VOLTAGE	-5.000	-10.000	-10.000	-5.000	-5.000
BIPOLAR ADC ZERO CODE	2048	8192	8192	2048	2048
UNIPOLAR MAX VOLTAGE	+9.998			+9.998	+9.998
UNIPOLAR MIN VOLTAGE	0.0			0.0	0.0
UNIPOLAR ADC ZERO CODE	0			0	0

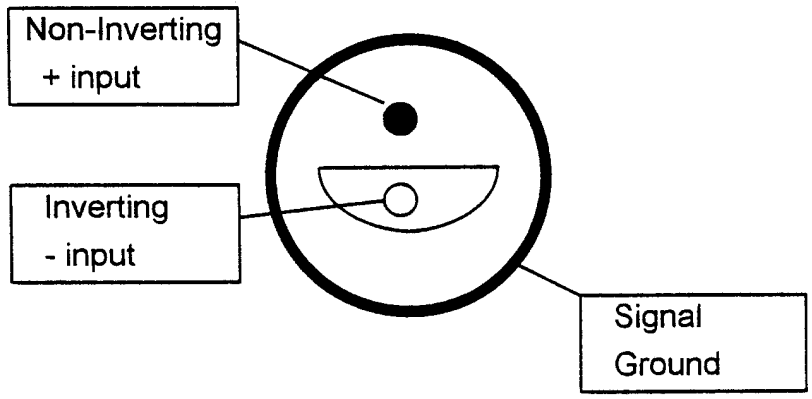
Independent mode selection is available for each channel. Selection is made via jumpers within the module. Refer to the MODULE INFORMATION section of the manual for their locations.

Input Signal Connection

Each ADC channel has a high impedance, wide bandwidth differential amplifier input.

Connector compatibility:

LEMO RA0.302NYL dual pin connector mates with LEMO F0.302NYLU/3.7



The 2812M is a special version of the 2812 with a multipin cable input which is compatible with the 1008 amplifiers; this module uses an AMP 204731-1 w/ 205172-8 Female Pins which mates with AMP 204744-1 w/ 203816-3. The pin-out for this connector is:

CHANNEL	+IN	-IN	SIG GND
1	1A	2A	1B
2	1C	2C	2B
3	4A	5A	4B
4	4C	5C	5B
5	8A	9A	8B
6	8C	9C	9B
7	11A	12A	11B
8	11C	12C	12B

Signal Conditioning

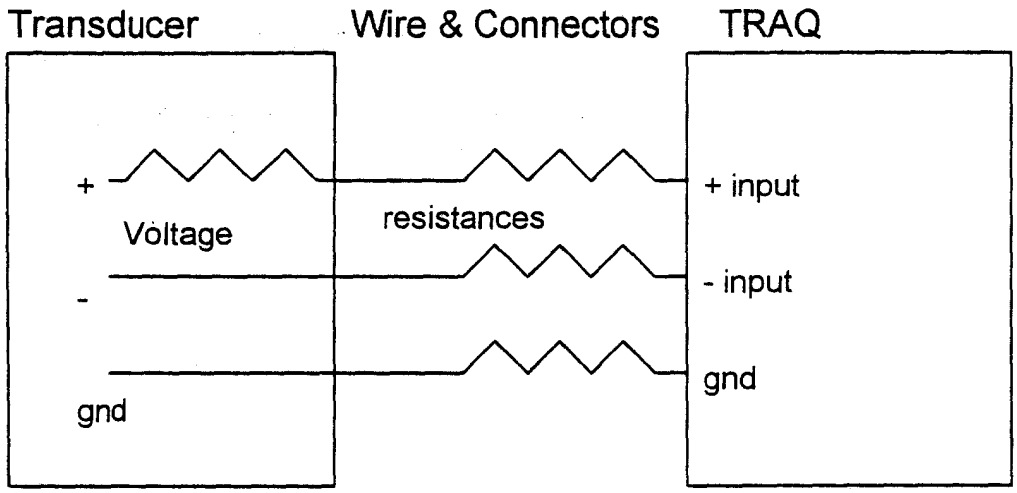
In order to maintain signal quality and, therefore, digitizer accuracy, certain signal conditioning procedures must be observed when connecting the TRAQ system to a signal source.

1) Use differential connections for analog signals. If the source is single ended, connect one side of the differential pair to the source ground.

2) Use twisted pair shielded cables.

3) Shield all analog signals to minimize inter-channel coupling and noise pickup. Ground all shields at a single, common ground to avoid ground loops.

4) Use low impedance sources, cabling, and connections. The DSP ADCs can resolve a milliVolt Voltage changes. The signal source impedance, as measured at the TRAQ channel input, must be less than 200 Ohms in order to maintain system accuracy.



SECTION 13
DATA ACQUISITION MODULE SPECIFIC INFORMATION

The following sections describe in detail each of the TRAQ Data Acquisition modules. This includes information on selecting available options and calibration procedures.

Model 2812 12 bit / 100 kHz / 8 Channel ADC

Bipolar/Unipolar Signal Input Options

1) To select BIPOLAR input option remove jumper labeled "UNI" next to R21 component at desired channel.

2) To select UNIPOLAR option, install jumper at position labeled "UNI" next to R21 component at desired channel.

NOTES

1) Make sure R19 is 10 Kohms at the desired channel. On some early units R19 was 51.1 Kohms.

2) Signal input is connected to inverting channel input. Ground is connected to non-inverting channel input .

Bipolar Calibration and Alignment

Each channel of the DSP 2812 has an individual set of calibration adjustments. Access to the offset, gain, and common mode rejection trims is achieved by removing the left-hand side cover. Drawing 2812A-01-AD indicates the location of each channel and the adjustments for each.

1) Set channel to bipolar mode.

2) Set digitizer sampling clock to 100 KHz.

3) Connect +ve channel input to gnd.
Connect -ve channel input to gnd

4) Digitize and average over 10 data samples.
Adjust R21 for averaged reading of 2048.

5) Connect +ve channel input to gnd.
Connect -ve channel input to +4.900 Volt reference.

6) Digitize and average over 10 data samples.
Adjust R22 for averaged reading of 41.

7) Connect +ve channel input to +4.900 Volt reference.
Connect -ve channel input to +4.900 Volt reference.

8) Digitize and average over 10 data samples.
Adjust R25 for averaged reading of 2048.

Unipolar Calibration and Alignment

1) Perform BIPOLAR MODE calibration first.

2) Set channel to unipolar mode.

3) Set digitizer sampling clock to 100 KHz.

4) Connect -ve channel input to +5.000 Volt reference.
Connect +ve channel input to gnd.

5) Digitize and average over 10 data samples.
Adjust R21 for averaged reading of 2048.

Common Mode Rejection

1) Set channel to bipolar mode.

2) Connect +ve channel input to 10 v pk-pk 25 KHz sinewave.

3) Digitize and display reconstructed data.
Adjust R25 for minimum amplitude display.

Model 2814 14 bit / 100 kHz / 4 Channel ADC

Bipolar Calibration and Alignment

1) Set digitizer sampling clock to 100 kHz.

2) Connect both inputs of the unit under test to system ground. Adjust R19 until the digital data from the unit under test reads 8188 (decimal).

3) Connect the non-inverting input of the unit under test to the precision DC source. Set the source output Voltage to 9.990 Volts. Adjust R18 until the digital data from the unit under test reads 16302.

Model 2840 14 bit / 1 mHz / 4 Channel ADC

Bipolar Calibration and Alignment

1) Set digitizer sampling clock to 100 kHz.

2) Connect both inputs of the unit under test to system ground. Adjust

Channel 1 R51

Channel 2 R69

Channel 3 R14

Channel 4 R32

until the digital data from the unit under test reads 8188 (decimal).

3) Connect the non inverting input of the unit under test to the precision DC source. Set the source output Voltage to 9.990 Volts. Adjust

Channel 1 R53

Channel 2 R21

Channel 3 R16

Channel 4 R34

until the digital data from the unit under test reads 16302.

Model 2824 12 bit / 2 mHz / 1 Channel ADC

Access to the DSP 2824 gain, offset, and common-mode rejection adjustments is achieved by removing the left hand side cover. Drawing 2824-01-AD indicates the locations of these adjustments.

Bipolar Calibration and Alignment

1) Connect both inputs of the unit under test to system ground. Adjust R30 until the digital data from the unit under test reads 2048 (decimal).

2) Connect the non-inverting input of the unit under test to the precision DC source. Set the source output voltage to 4.974 Volts. Adjust R9 until the digital data from the unit under test reads 4085.

3) Repeat step 1. If no adjustment is necessary, continue to step 4; otherwise repeat steps 1 and 2 until there is no change when step 1 is repeated.

4) Connect both inputs of the unit under test to the precision voltage source. Adjust R10 until the digital data from the unit under test reads 2048.

Unipolar Calibration and Alignment

1) Select BIPOLAR MODE* and perform BIPOLAR MODE calibration.

2) Select UNIPOLAR MODE*.

3) Connect both non-inverting and inverting inputs to ground. Adjust R30 until a digital reading of between 0 and 1 is recorded.

> **NOTE**
>
> See sheet 1 of 2824 schematic for selecting UNIPOLAR or BIPOLAR MODES.

Model 2860 12 Bit / 1mHz / 4 Channel ADC

Bipolar/Unipolar Signal Input Options

Bipolar

Install jumper at position labeled "BI" for the desired channel(s). (factory setting)

Unipolar

Install jumper at position labeled "UNI" for the desired channel(s).

Calibration and Alignment

Each channel of the DSP 2860 has an individual set of calibration adjustments. Access to the offset, gain, and common mode rejection trims is achieved by removing the left hand side cover. Drawing 2860-01-AD indicates the location of each channel and the adjustments for each.

Bipolar Mode Calibration

1) Set channel to bipolar mode according to the previous section

2) Set digitizer sampling clock to 1MHz.

3) Connect 0.000 Volt reference to + input of channel.

Connect 0.000 Volt reference to - input of channel.

4) Adjust R12 (Offset) so that the digitized readout from the Controller (averaged over 10 samples) reads 2047.5 (± 0.5).

5) Connect +4.900 Volts reference to + input of channel.

Connect 0.000 Volts reference to - input of channel.

6) Digitize and average over 10 data samples.

Adjust R27 (+Gain) for averaged reading of 4054 (±0.5).

7) Connect +4.900 Volt reference to + input of channel.

Connect +4.900 Volt reference to - input of channel.

8) Digitize and average over 10 data samples.

Adjust R34 (-Gain) for averaged reading of 2047.5 (±0.5).

APPENDICES

ORDERING INFORMATION AND WARRANTY

Ordering

When ordering, please specify the complete Model Number along with any options, product description, and quantity. Orders may be placed by written order, telephone, TWX/Telex or FAX. Telephone orders must be confirmed in writing. All orders are subject to the approval of DSP Technology's Credit Department which is indicated by confirming sales order issued by the Company. The minimum order is one hundred ($100) dollars, excluding transportation charges.

Customers should send their orders to:

DSP Technology Inc.
Order Processing Department
48500 Kato Road
Fremont, CA 94538
Telephone: (415) 657-7555
Telex: 283608
FAX: 415-657-7576

Pricing

Published prices cover standard packing only and do not include shipping, insurance, taxes, or any customs charges. All prices are subject to change without notice. All prices are F.O.B. Fremont, California. Please contact factory for volume discounts.

Payment Terms

Unless otherwise indicated, terms of payment for domestic orders, except for turn-key module/system, are net thirty (30) days from date of shipment. Terms of payment for turn-key systems are 40% of the written contracted price submitted with the purchase order, 40% due net 30 days after shipment, 20% due net 30 days after acceptance of the system at the customer's facility (which must be completed within 30 days after shipment). A turn-key system is defined as customized hardware and software combination for which performance specifications are written that communicate how the system will perform for a specific application. Terms for orders outside the U.S. are cash in advance or irrevocable letter of credit, unless other terms have been previously arranged.

All orders placed with DSP Technology are binding and are subject to a cancellation charge of twenty five (25) percent of the selling price if cancelled.

Shipping

Domestic shipments are made by UPS, air freight, or truck. Shipping charges for UPS services are prepaid and charges added to the invoice, while other shipping methods are on a freight-collect basis. Overseas shipments are made by air freight.

Claims for shipping damages must be reported and confirmed in writing to the delivering carrier no later than fifteen (15) days after date of receipt. Claims for shortages of material must be made to DSP Technology within thirty (30) days after receipt of shipment.

Returns

DSP Technology must be notified before any product is returned for any reason. The Customer Service Department must

issue a Returned Material Authorization (RMA) number before any product can be accepted for credit, exchange or repair.

All returns for credit or exchange are subject to DSP Technology's approval and will incur a restocking charge of twenty five (25) percent, as well as any incoming transportation charges or other fees incurred by DSP Technology Inc.

Other Services

Contact DSP Technology for details regarding the following services: On-site consultation, Service contracts, System integration, and Installation.

PRODUCT WARRANTY[1]

DSP TECHNOLOGY ("DSPT") warrants its products to be free from defects in material and workmanship and to meet DSPT's performance specifications. The warranty period which begins from the date of shipment to the buyer, is 90 days for ODAS products and one year for all other products. The warranty is limited by the paragraphs below.

Return to Factory

If a buyer discovers a defect in a DSPT product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSPT's Fremont factory, where DSPT will, at its option, either repair or replace the product. This remedy applies if DSPT receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSPT of the defect before returning the product.

Cost of Repairs or Replacement

Buyer must prepay freight charges to DSPT. DSPT will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement of during warranty period.

Transferable Warranties

In addition to the foregoing warranty, DSPT also provides the buyer the transferable warranty, if any, provided to DSPT by the manufacturers of other products such as terminals and disk systems supplied by DSPT as part of a total system.

Limitation

The foregoing constitutes DSPT's entire warranty, expressed, implied, and/or statutory (except as to title), ad to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential.

---

[1]Excludes Software and ODAS Products

Other than as expressly provided in this document, no warranties expressed or implied, including any warranty of merchantability of fitness for a particular purpose are made. No employee, representative, or agent or seller has any authority expressed or implied to alter or supplement the terms of this warranty.

SCHEMATICS

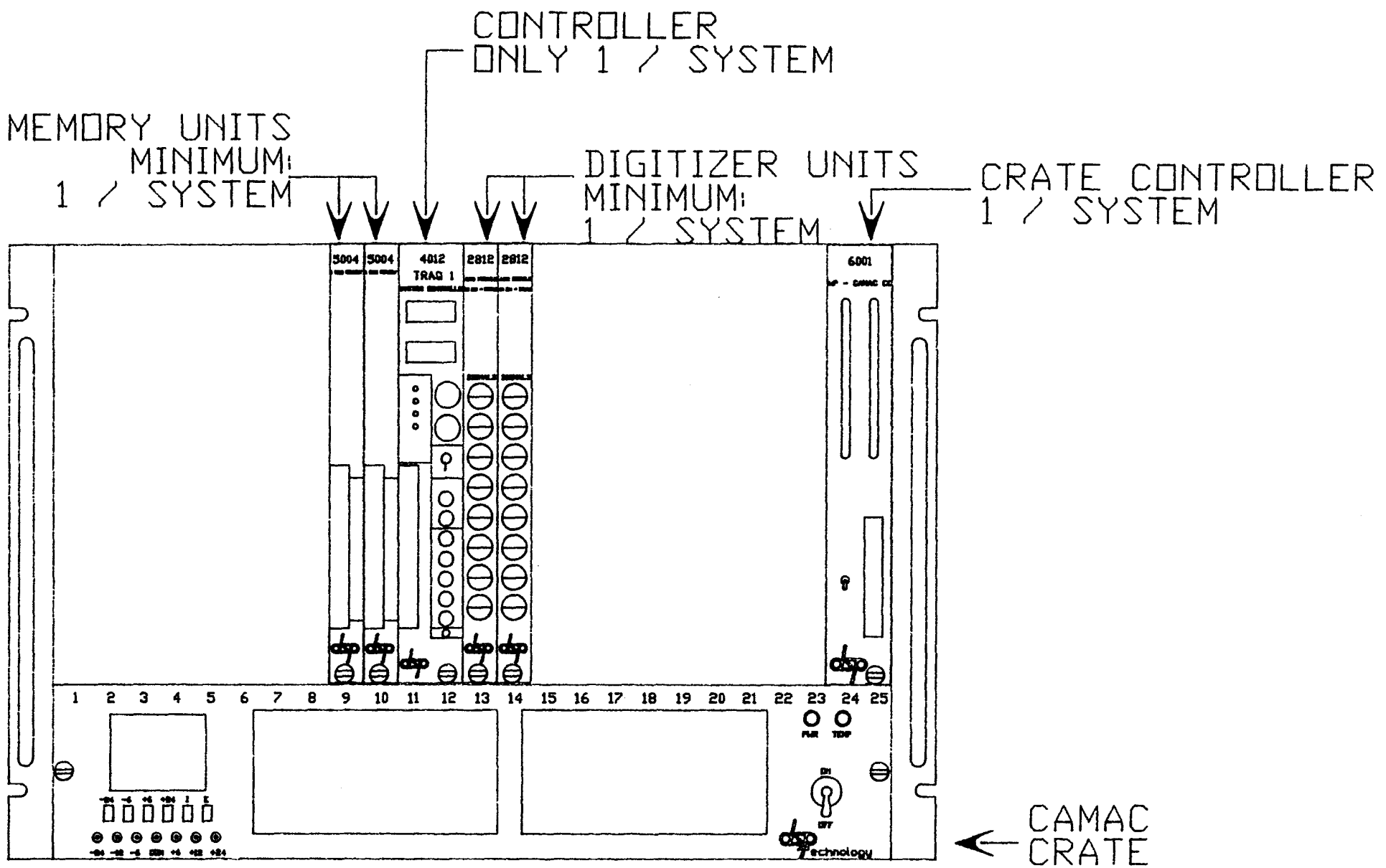


DIAGRAM 1
TRAQ CONFIGURATION DRAWING

40 PIN DAISY CHAINED CONNECTOR
CONNECTS TO:
REAR OF 4012 CONTROLLER
& REAR OF EACH DIGITIZER MODULE

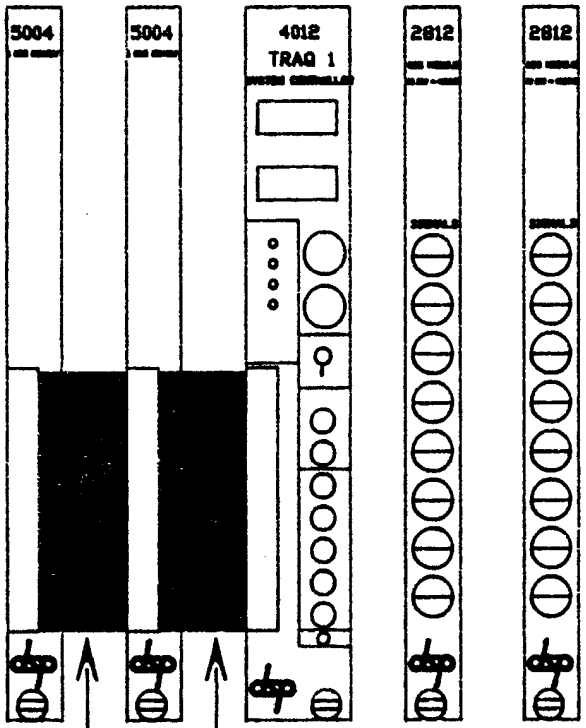


DIAGRAM 2
TRAQ
SYSTEM
INTERCONNECT

50 PIN DAISY CHAINED CONNECTOR
CONNECTS FROM 4012 CONTROLLER
TO EACH MEMORY MODULE

SYMBOLS.

CAMAC EDGE CONNECTOR

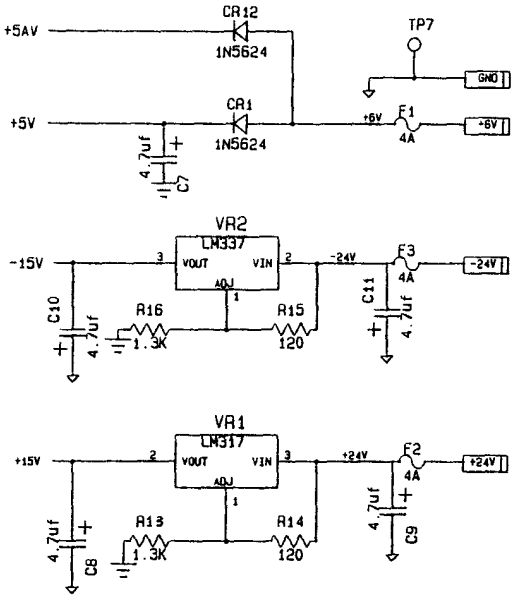
CONNECTOR (TO OUTSIDE WORLD)

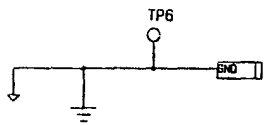
CONTINUE ON SAME SHEET

CONTINUE ON DIFFERENT SHEET

UNUSED PIN

JUMPERS





NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ⏚ DENOTES DIGITAL GROUND.
2. ⏚ DENOTES ANALOG GROUND.
3. ALL CAPACITORS ARE IN uf.
4. ALL RESISTORS ARE 5% 1/4WATT AND OHMS.
5. "*" DENOTES FACTORY OPTIONAL LOAD.

STANDARD JUMPERS	OPTIONAL JUMPERS LOADED AT TEST
"TRAQ II"	"TRAQ I"
"BI" (8 PLCS)	E1-E2, E3-E4, E5-E6 } ON LAST UNIT IN SYSTEM

REV	DESCRIPTION	BY	DATE
B	ECO1004-1009	JC	6/90
A	PROD. RELEASE		12/86

REVISIONS

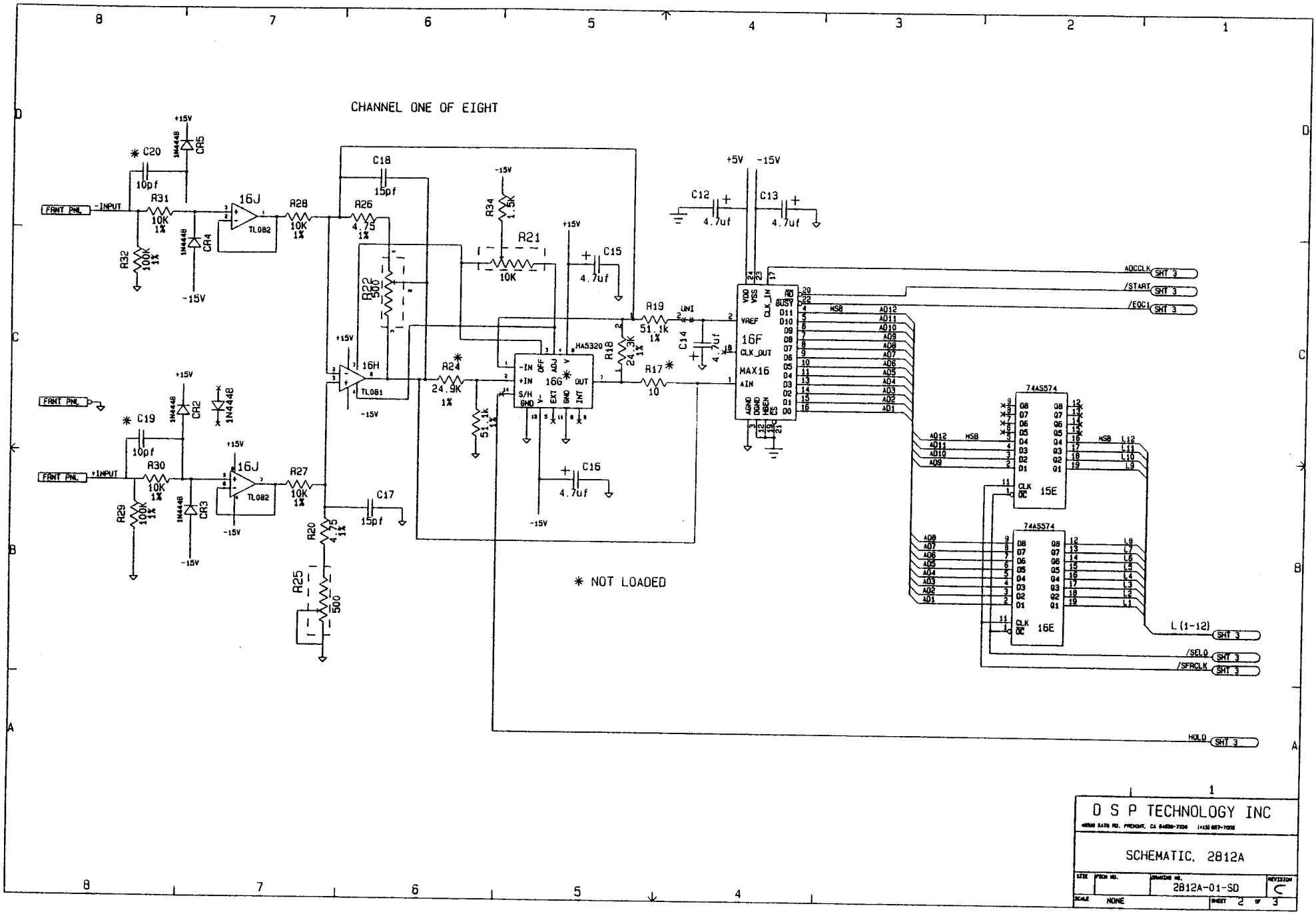
SIGNATURES	DATE
DESIGNED	
DRAWN N. PERALTA	12/85
CHECKED	
APPROVED	
ISSUED	

D S P TECHNOLOGY INC

SCHEMATIC, 2812A

SIZE | FSCM NO. | DRAWING NO. A-2812A-01-SD | REVISION C

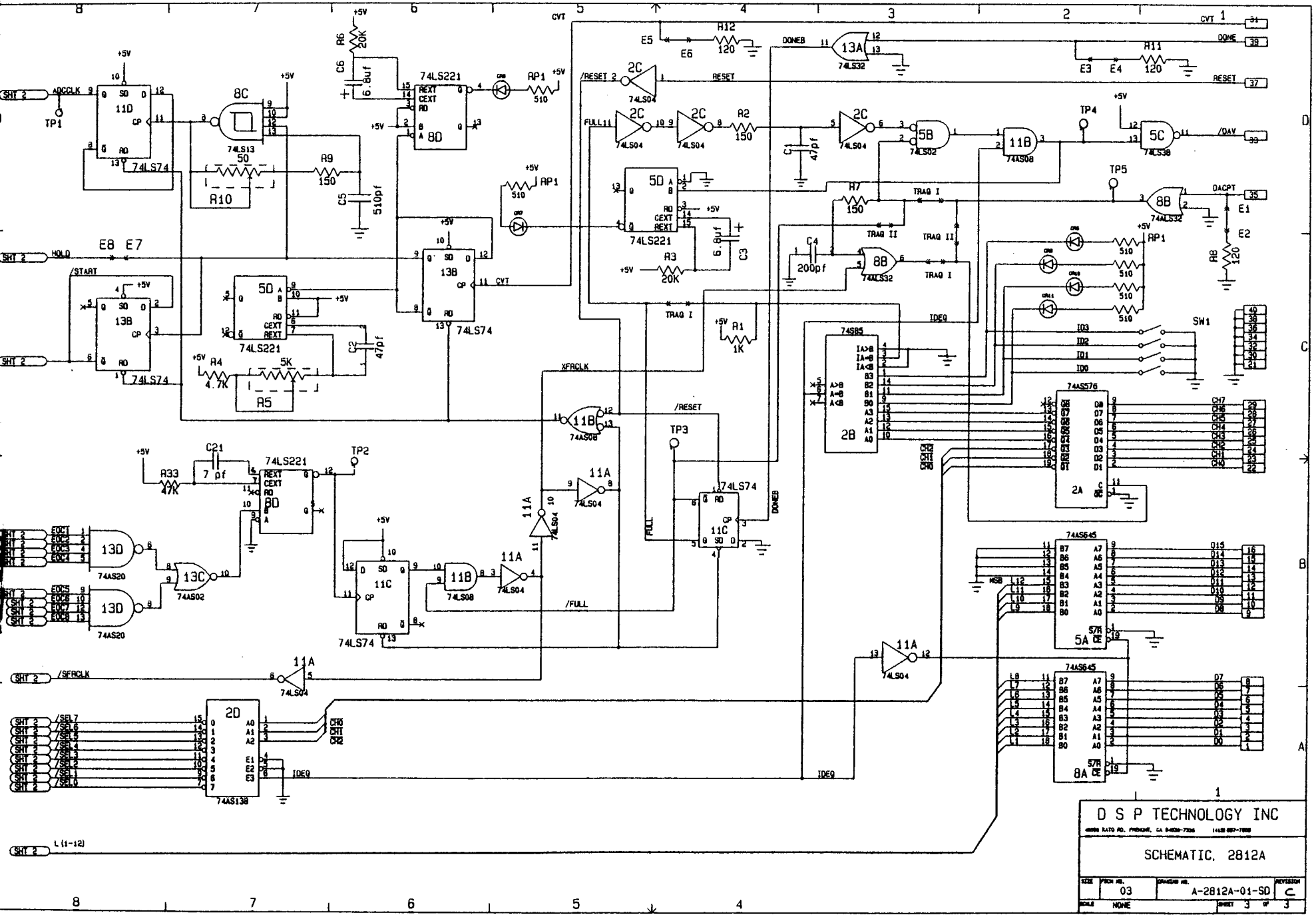
SCALE NONE | SHEET 1 OF 3

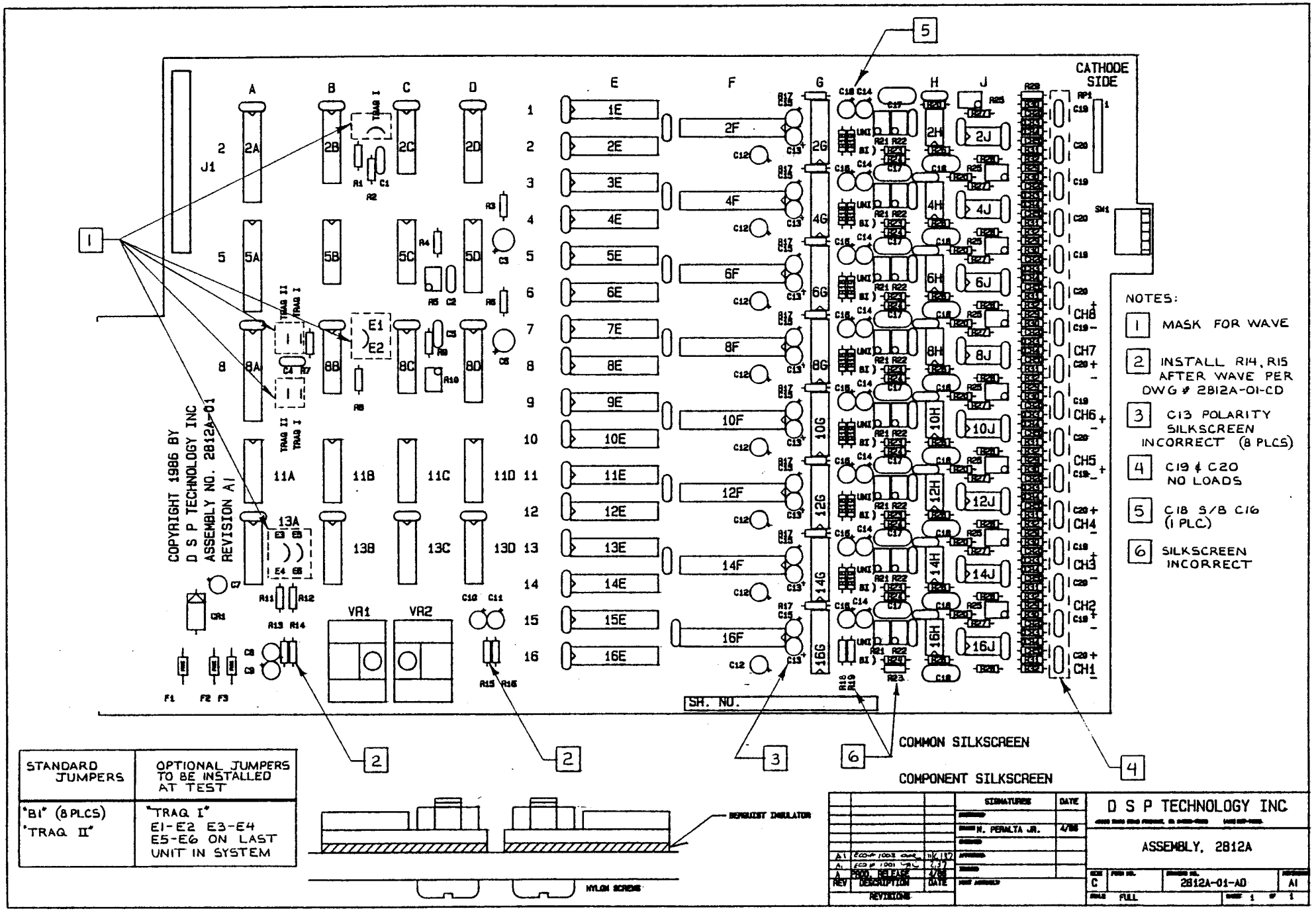


D S P TECHNOLOGY INC

SCHEMATIC, 2812A

SIZE	FSCM NO.	DRAWING NO.	REVISION
		2812A-01-SD	C
SCALE NONE		SHEET 2 OF 3	


D S P TECHNOLOGY INC
SCHEMATIC, 2812A
A-2812A-01-SD
03
NONE
74LS74
74LS221
74LS04
74LS02
74LS08
74LS32
74AS20
74AS02
74AS08
74AS32
74LS138
74S85
74AS576
74AS645
74LS13
74LS38
74ALS32
CVT
DONEB
RESET
/RESET
FULL
/FULL
XFRCLK
/SFRCLK
IDEQ
TRAQ I
TRAQ II
/START
/DAV
DACPT
ADCCLK
+5V
TP1
TP2
TP3
TP4
TP5
SW1
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
A1
A2
C1
C2
C3
C4
C5
C6
C21
AP1
E1
E2
E3
E4
E5
E6
E7
E8



STANDARD JUMPERS	OPTIONAL JUMPERS TO BE INSTALLED AT TEST
"B1" (8 PLCS) "TRAQ II"	"TRAQ I" E1-E2 E3-E4 E5-E6 ON LAST UNIT IN SYSTEM

REV	DESCRIPTION	DATE
A1	ECO # 1003	4/86
A	ECO # 1001 RELEASE	4/86

REVISIONS

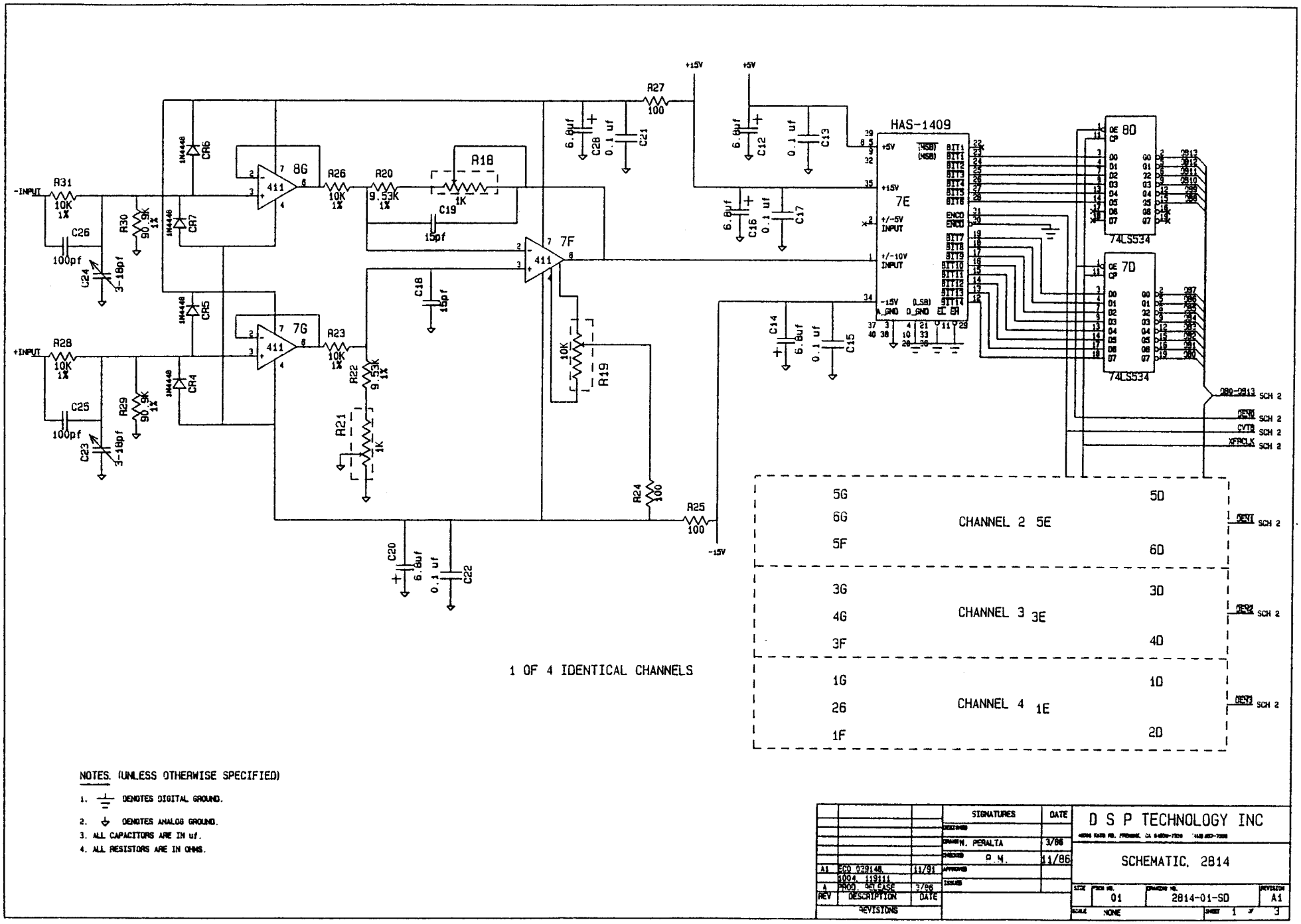
SIGNATURES	DATE
N. PERALTA JR.	4/86

D S P TECHNOLOGY INC

ASSEMBLY, 2812A

SIZE	FSCM NO.	DRAWING NO.	REV
C		2812A-01-A0	A1

SCALE FULL SHEET 1 OF 1



1 OF 4 IDENTICAL CHANNELS

NOTES. (UNLESS OTHERWISE SPECIFIED)

1. ⏚ DENOTES DIGITAL GROUND.
2. ⏚ DENOTES ANALOG GROUND.
3. ALL CAPACITORS ARE IN uf.
4. ALL RESISTORS ARE IN OHMS.

REV	DESCRIPTION	DATE
A1	ECO 02914B, 1004, 11911	11/91
A	PROD. RELEASE	3/88

REVISIONS

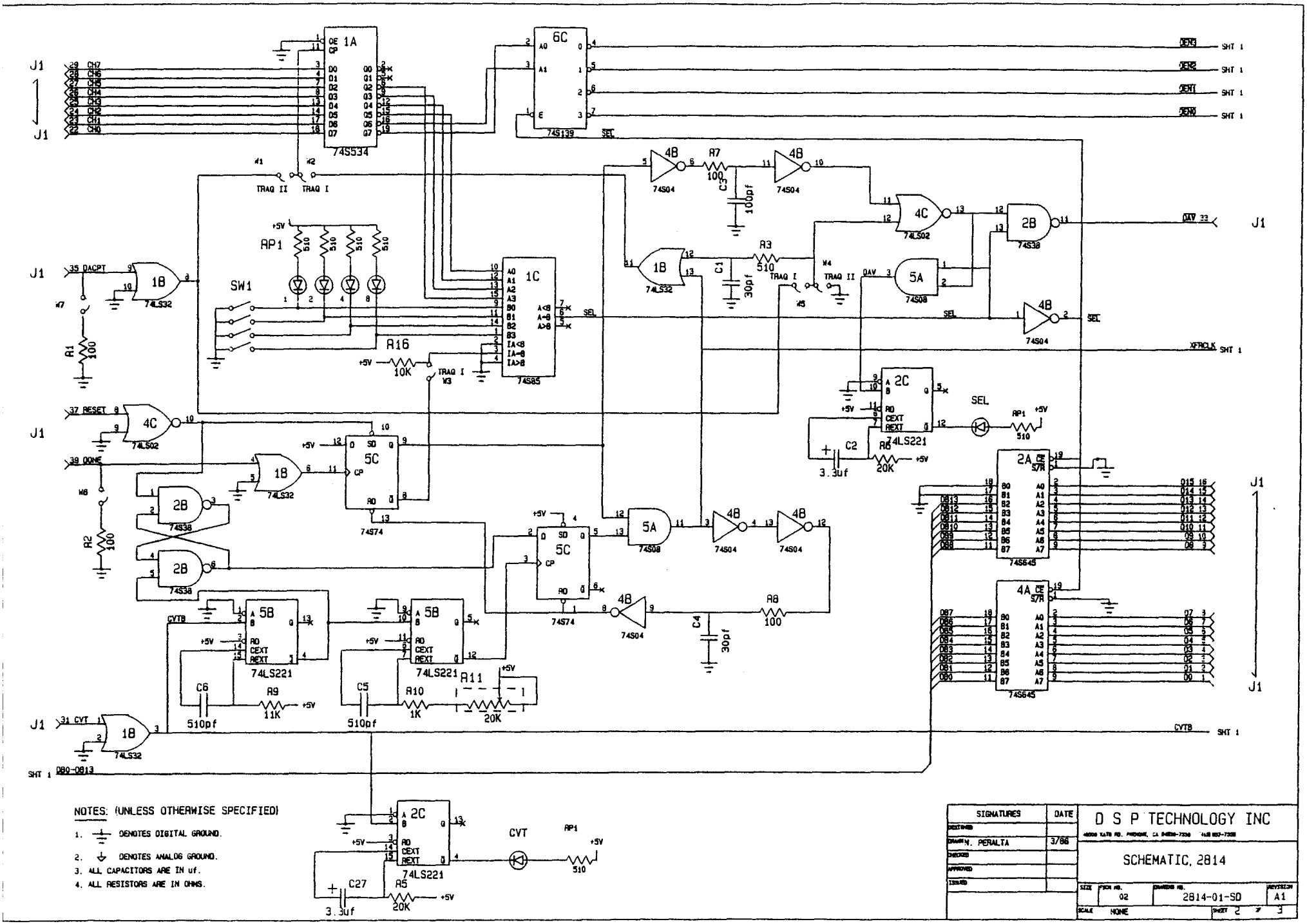
SIGNATURES	DATE
DRAWN N. PERALTA	3/88
CHECKED P.M.	11/88
APPROVED	
ISSUED	

D S P TECHNOLOGY INC

SCHEMATIC, 2814

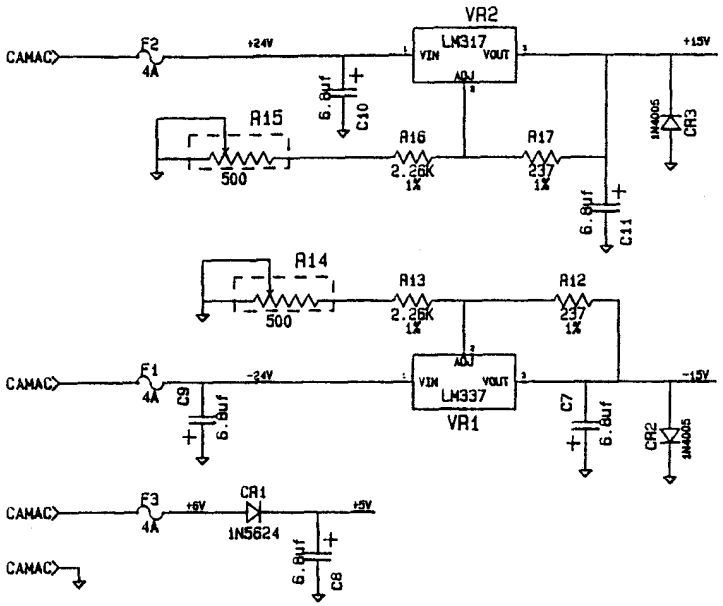
SIZE A | FSCM NO. 01 | DRAWING NO. 2814-01-SD | REVISION A1

SCALE NONE | SHEET 1 OF 3

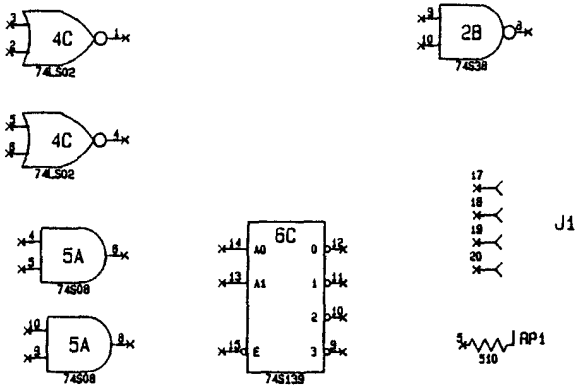

74S534
74S139
74S85
74S574
74LS221
74LS32
74S04
74S08
74S38
74LS02
74S645
TRAQ II
TRAQ I
SEL
XFRCLK
CVTB
DAV 33
SHT 1
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. DENOTES DIGITAL GROUND.
2. DENOTES ANALOG GROUND.
3. ALL CAPACITORS ARE IN uf.
4. ALL RESISTORS ARE IN OHMS.
SIGNATURES
DATE
N. PERALTA
3/86
D S P TECHNOLOGY INC
SCHEMATIC, 2814
2814-01-SD
A1
NONE

TRAQ I (ONE CARD PER SYSTEM ONLY)
W2, W3, W5, W6, W7

TRAQ II OPT A
W1, W4 INSTALLED



SPARES



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ⏚ DENOTES DIGITAL GROUND.
2. ⏚ DENOTES ANALOG GROUND.
3. ALL CAPACITORS ARE IN uf.
4. ALL RESISTORS ARE IN OHMS.

SIGNATURES	DATE
DESIGNED	
DRAWN N. PERALTA	3/86
CHECKED	
APPROVED	
ISSUED	

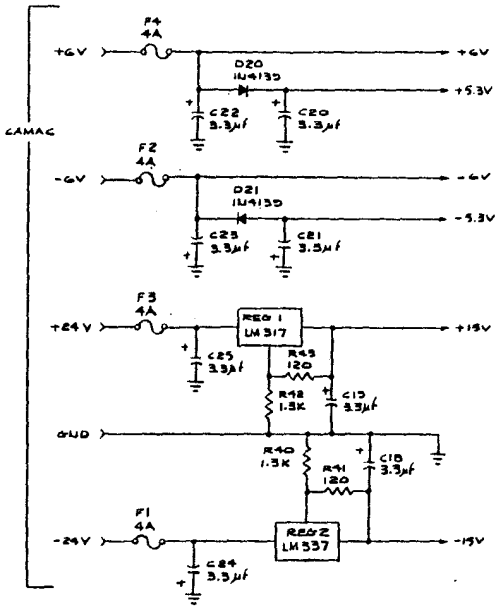
D S P TECHNOLOGY INC

SCHEMATIC, 2814

SIZE	DWG NO.	REVISION
	2814-01-SD	A1

SCALE NONE SHEET 3 OF 3

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	C	ECO 1009	3-21-86	
	D	ECO 1018	10-22-86	
	D1	ECO 1019, 1015, ADDED COVER SHT	11-2-88	JMC
	D	ECO 1017, 1018, 1019	6-1-90	JWC
	D	ECO 035138, 035145	2-21-92	JWC



NOTES: OPTIONS

1. FOR 2824 OPTION "A"
   a. R57 = 0 Ω (JUMPER)
   b. C14 IS NOT LOADED
   c. INSTALL TRACE JUMPERS.

2. FOR 2824
   a. R57 = 510 Ω
   b. C14 = 100 pF
   c. INSTALL THE FOLLOWING JUMPERS.

      TRACE
      E4 - E5 (ONLY ON ONE UNIT IN THE SYSTEM)
      E6 - E7 (ONLY ON ONE UNIT IN THE SYSTEM)

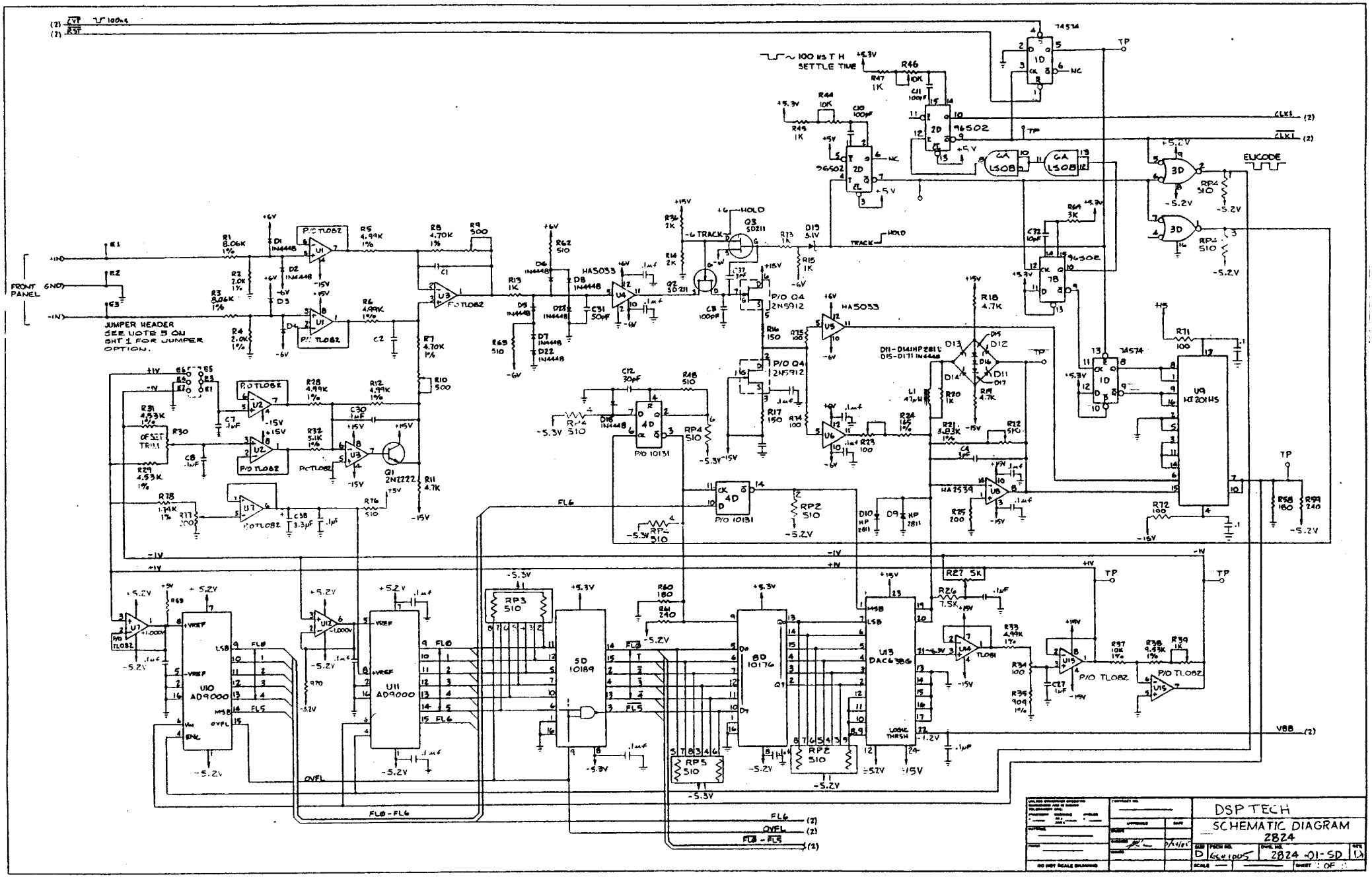
3. FULL SCALE INPUT OPTIONS:
   REFER TO COMPONENT SIDE OF PCB AT GROUP OF JUMPER SOCKETS MARKED "J1" NEAR FRONT PANEL.
   a. UNIPOLAR (-):

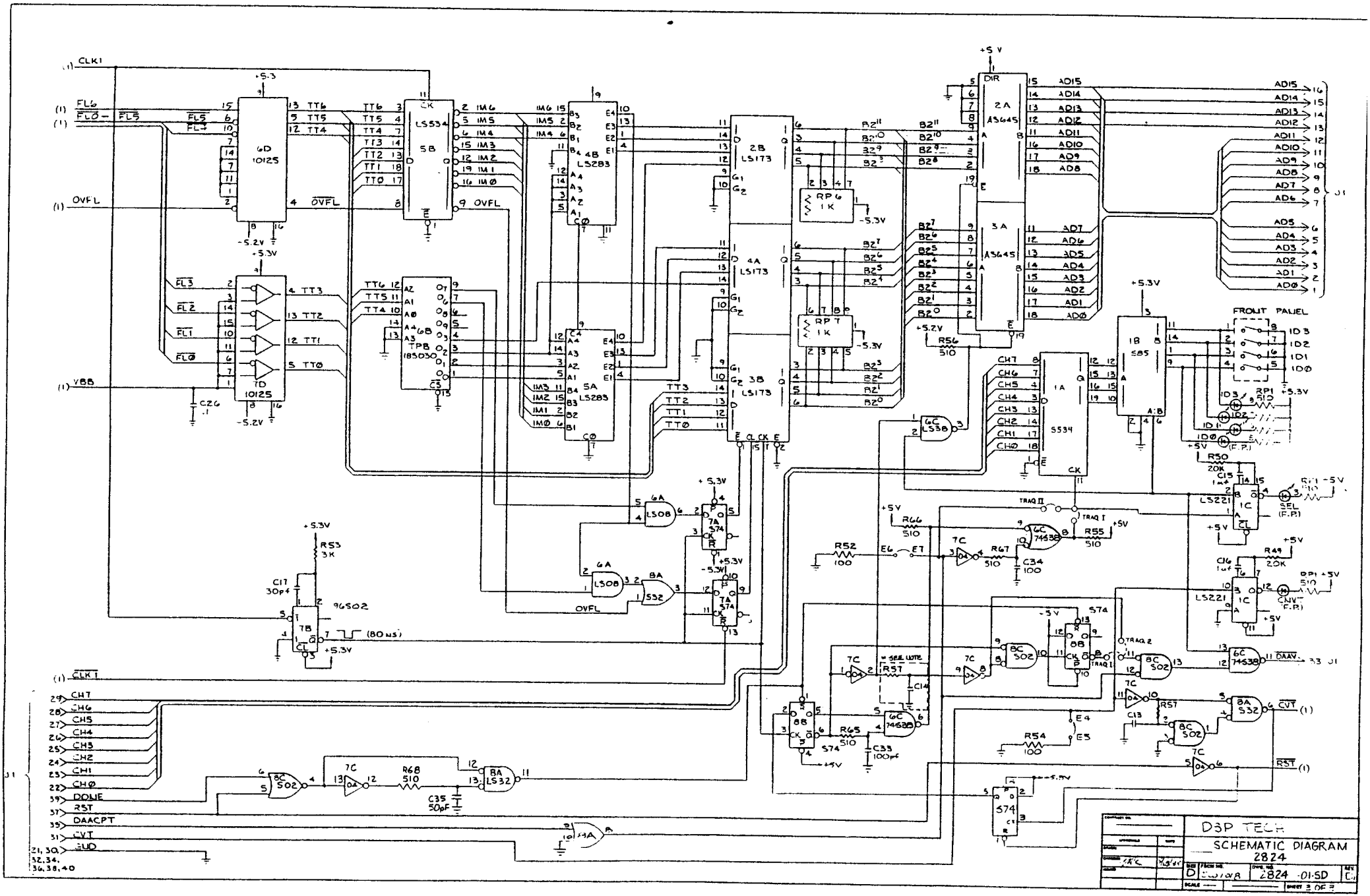
   b. BIPOLAR:

   c. UNIPOLAR (+):

PARTS LIST					
QTY	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION	

CONTRACT NO.		DSP TECHNOLOGY	
APPROVALS	DATE	SCHEMATIC DIAGRAM 2824	
DRAWN JWC	12/2/88		
CHECKED			
ISSUED			
NEXT ASSY	USED ON		
APPLICATION	DO NOT SCALE DRAWING	SIZE D	DWG NO. 2824-01-SD REV D1
		SCALE	SHEET 1 OF 3

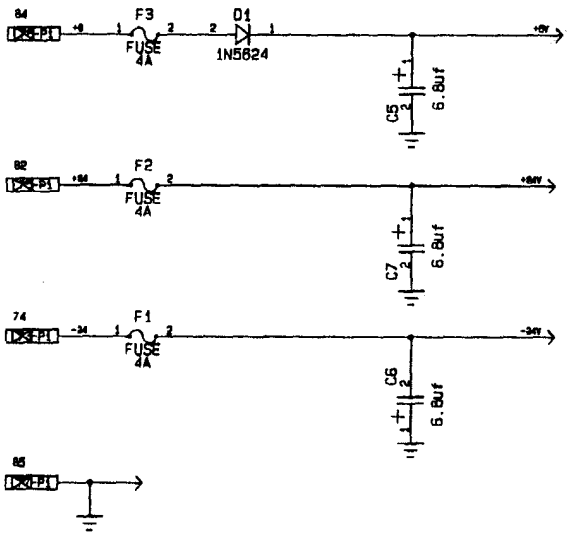

DSP TECH
SCHEMATIC DIAGRAM
2824
2824-01-SD
FRONT PANEL
JUMPER HEADER
SEE NOTE 3 ON SHT 1 FOR JUMPER OPTION.
SETTLE TIME
TRACK
HOLD
ELCODE
OFFSET TRIM
U10 AD9000
U11 AD9000
U13 DAC6386
OVFL
FL0 - FL6


DSP TECH
SCHEMATIC DIAGRAM
2824
D
2824-01-SD
SHEET 3 OF 3
CLK1
OVFL
YBB
FL6
FL5
FL4
FL3
FL2
FL1
FL0
6D 10125
7D 10125
LS534
5B
4B LS283
5A LS283
2B LS173
4A LS173
3B LS173
TPB 18S030
96S02
(80 NS)
2A AS645
3A AS645
1A S534
1B S85
FRONT PANEL
ID3
ID2
ID1
ID0
(F.P.)
SEL (F.P.)
CNV (F.P.)
LS221
LS08
LS32
74S38
74S74
TRAQ I
TRAQ II
TRAQ 2
DAAV
CVT
RST
DONE
DAACPT
CVT
GND
CH7
CH6
CH5
CH4
CH3
CH2
CH1
CH0
J1
21, 30, 32, 34, 36, 38, 40

SYMBOLS:

- CAMAC EDGE CONNECTOR
- EXTERNAL CONNECTOR
- CONTINUE ON SAME SHEET
- CONTINUE ON DIFFERENT SHEET
- UNUSED PIN
- JUMPERS

REVISIONS						
ECO#	REV	BY	DATE	DESCRIPTION	APPRV	DATE



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.

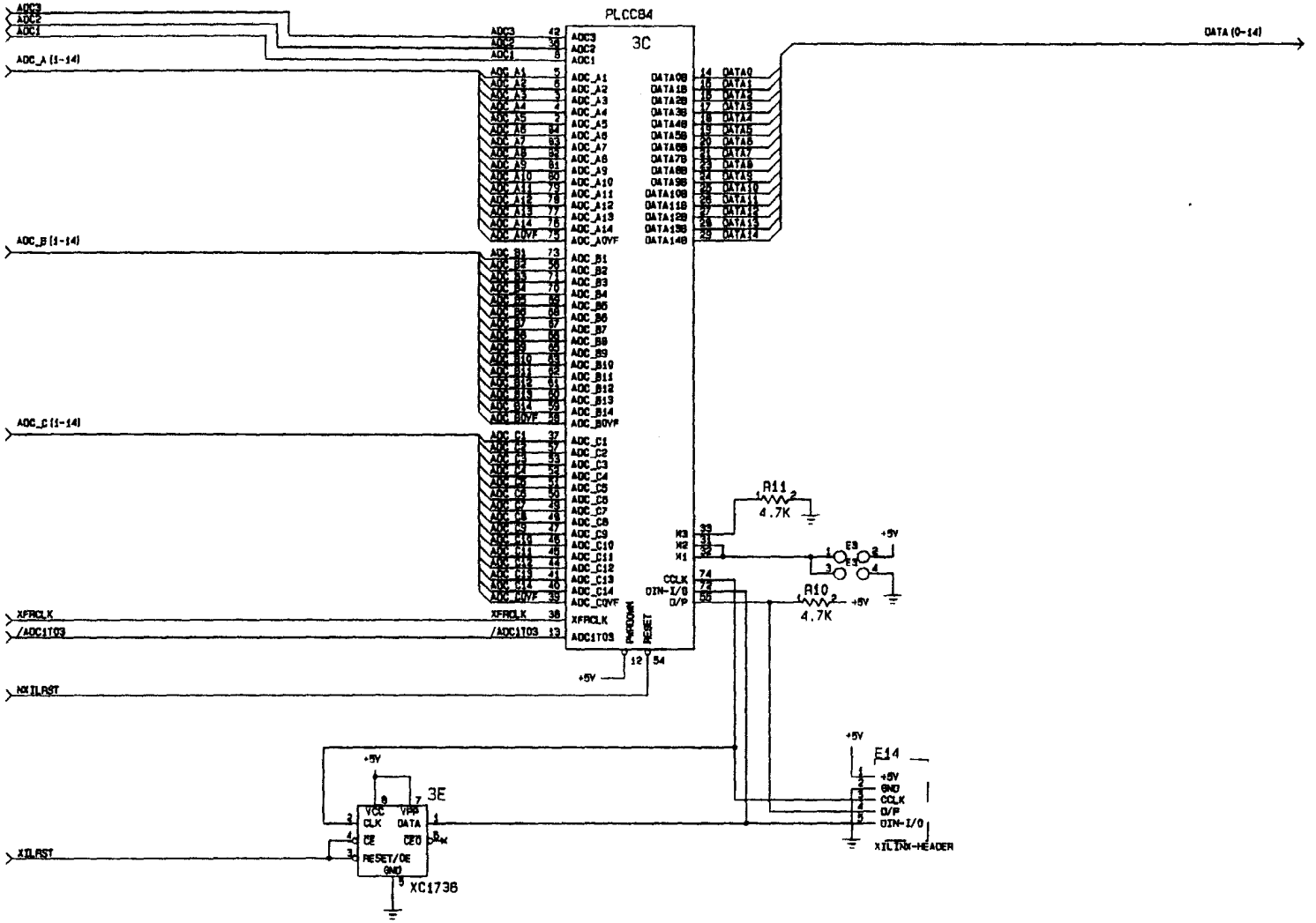
SIGNATURES	DATE
N. PERALTA	9/92

D.S.P. TECHNOLOGY INC
44080 KATO ROAD, FREMONT, CA 94538 (510) 657-7255

SCHEMATIC, 2840
POWER

SIZE	FSCM NO.	DRAWING NO.	REVISION
B		A-2840-01-SD	2

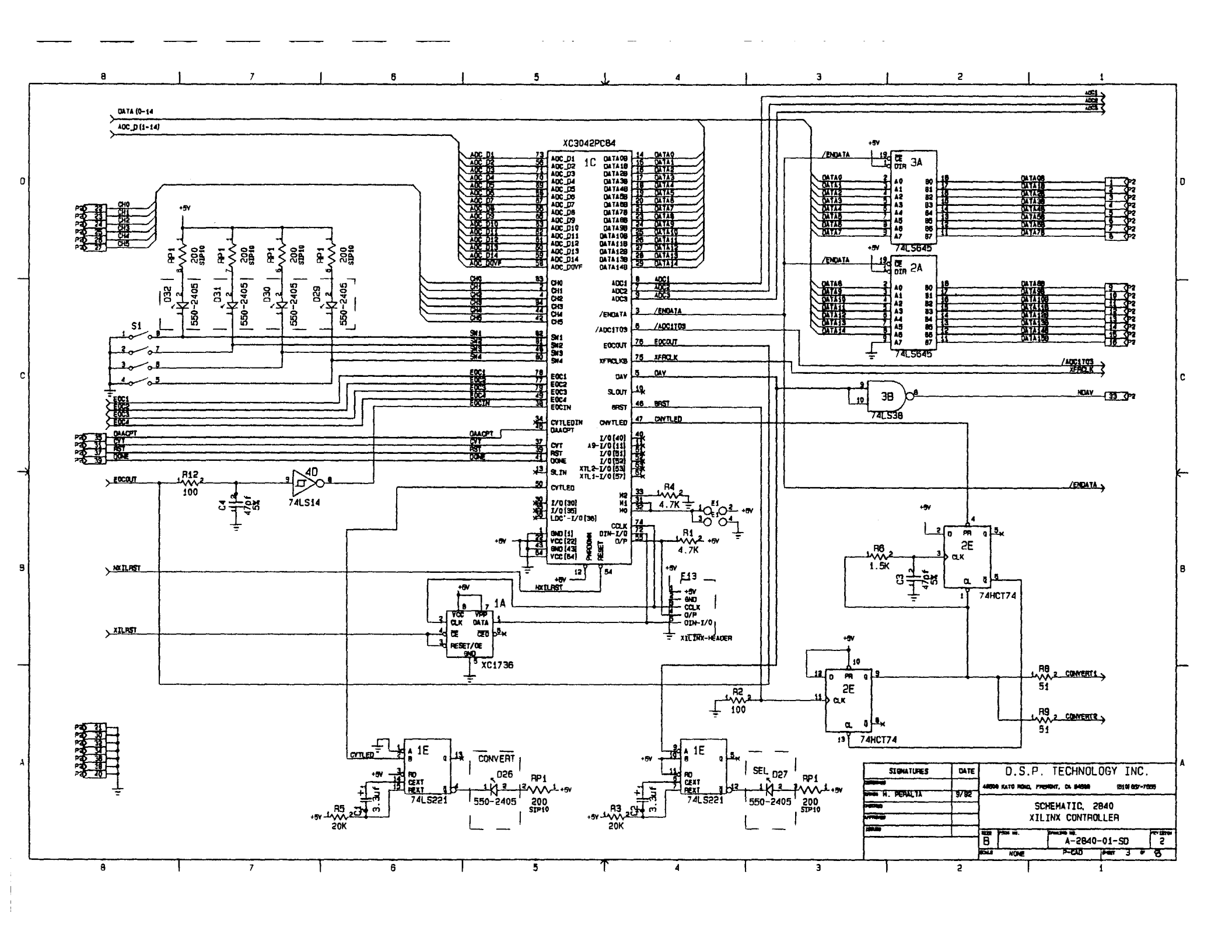
SCALE NONE P-CAD SHEET 1 OF 8

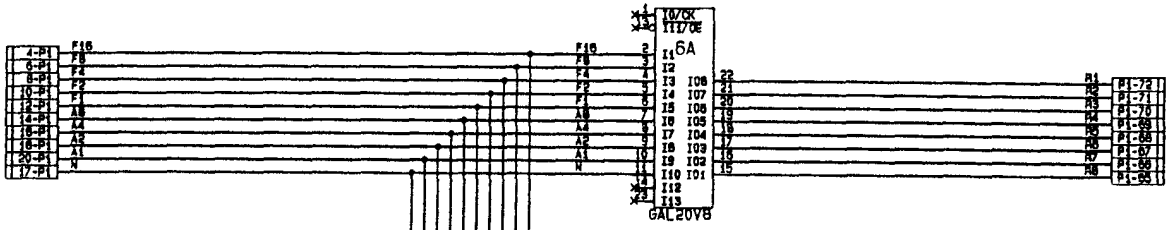


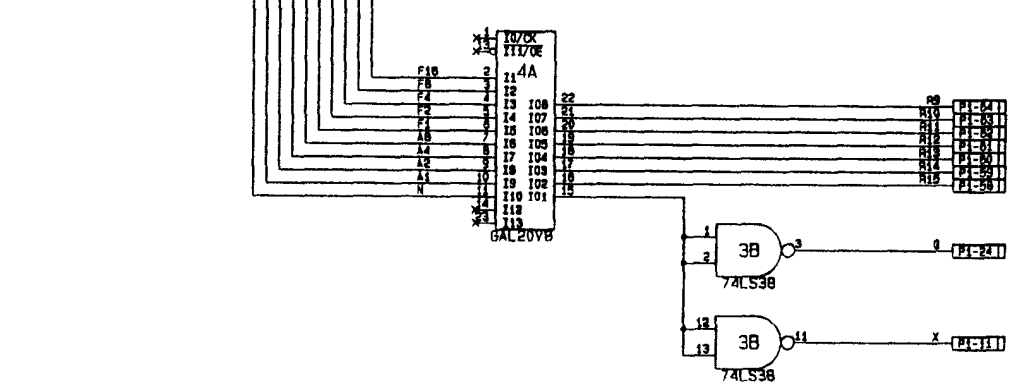
SIGNATURES	DATE
DRAWN N. PERALTA	9/92
CHECKED	
APPROVED	
ISSUED	

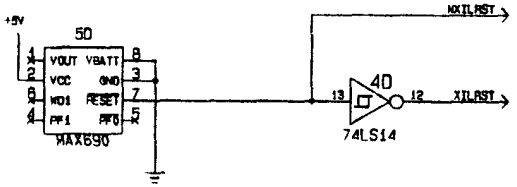
SCHEMATIC, 2840
XILINX BUS DRIBER

SIZE	FSCM NO.	DRAWING NO.	REV DATE
B		A-2840-01-SD	2
SCALE NONE		P-CAD	SHEET 2 OF 3


XC3042PC84
74LS645
74LS38
74HCT74
74LS14
74LS221
XC1736
XILINX-HEADER
550-2405
SCHEMATIC, 2840
XILINX CONTROLLER
D.S.P. TECHNOLOGY INC.
A-2840-01-SD
9/92







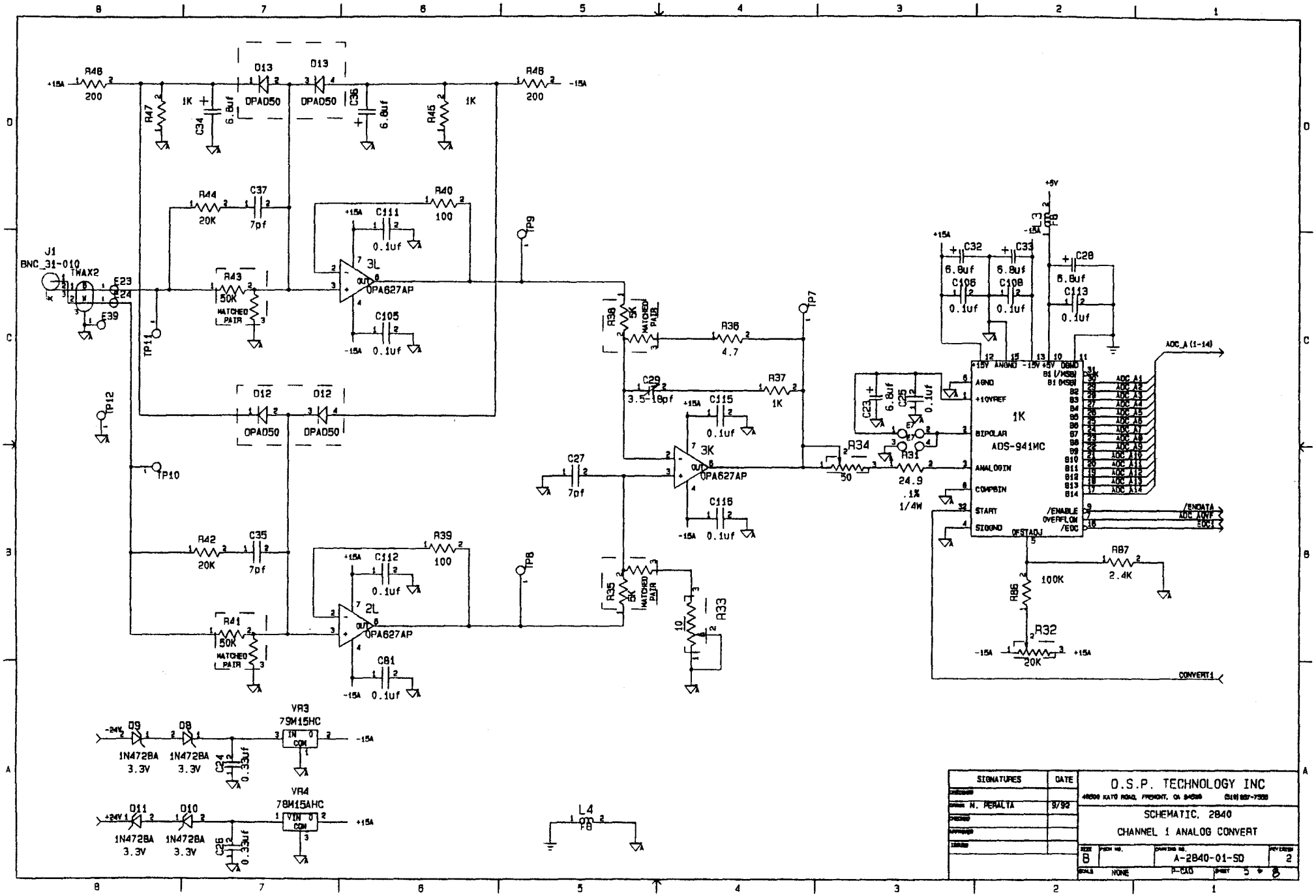
SIGNATURES	DATE
N. PERALTA	9/92

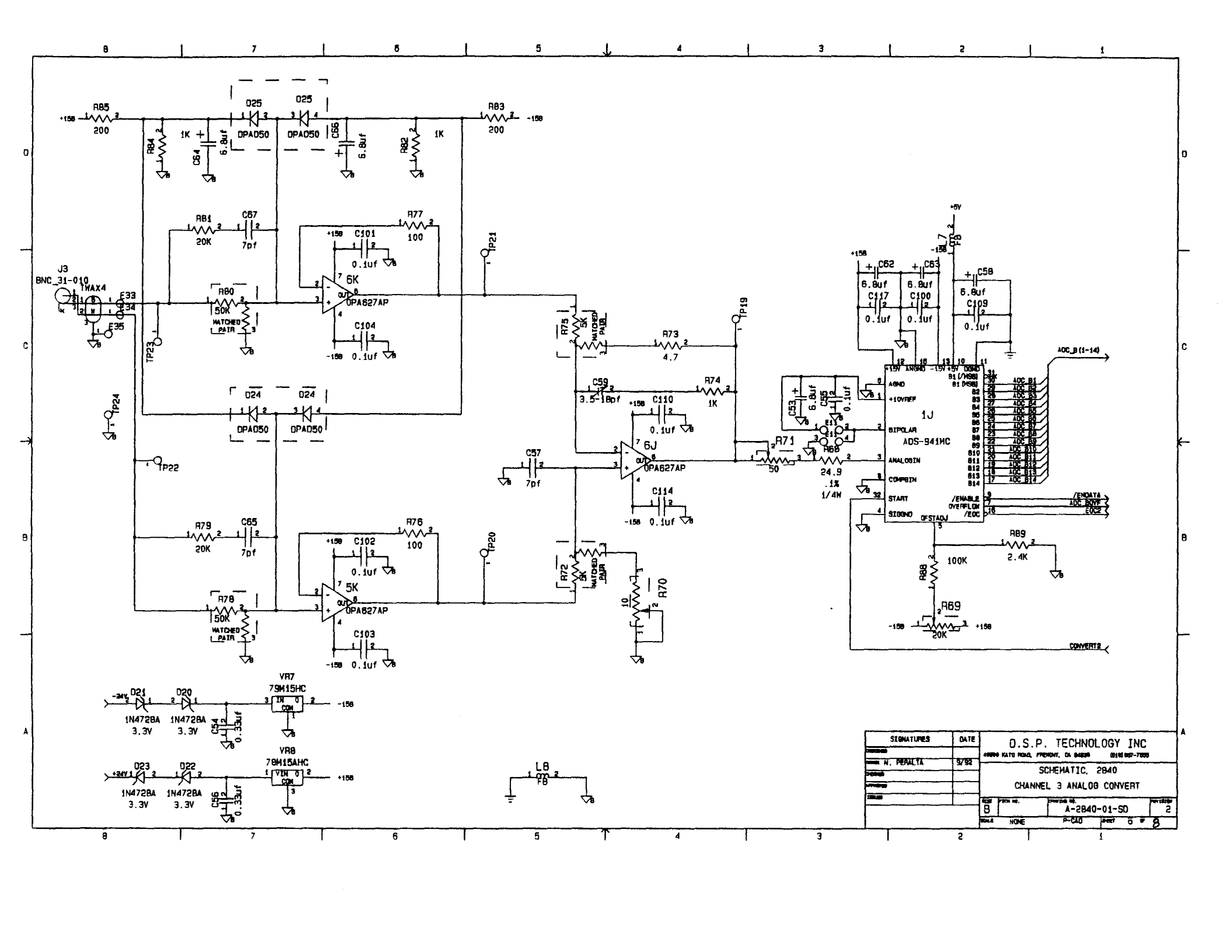
D.S.P. TECHNOLOGY INC

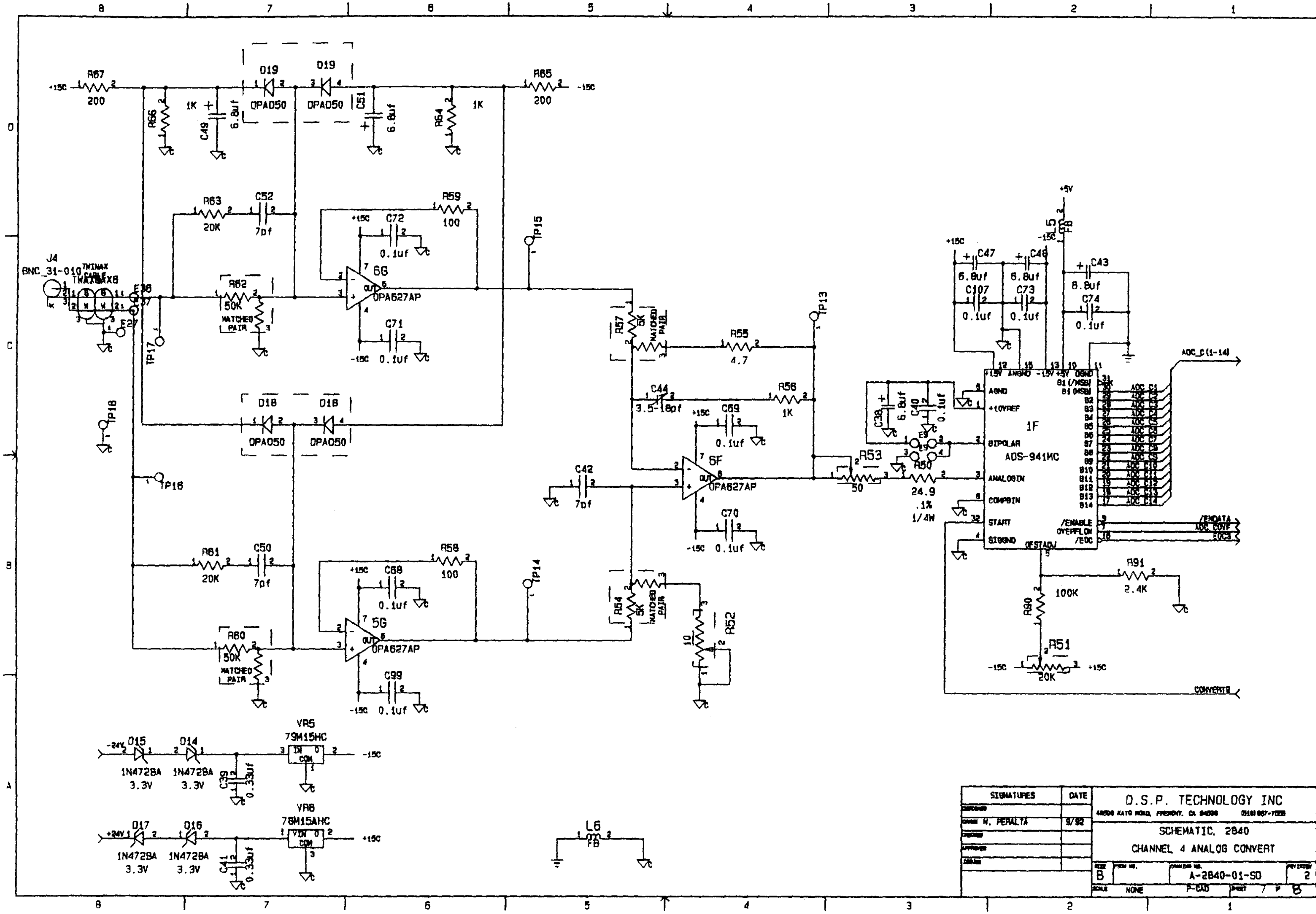
SCHEMATIC, 2840
CAMAC

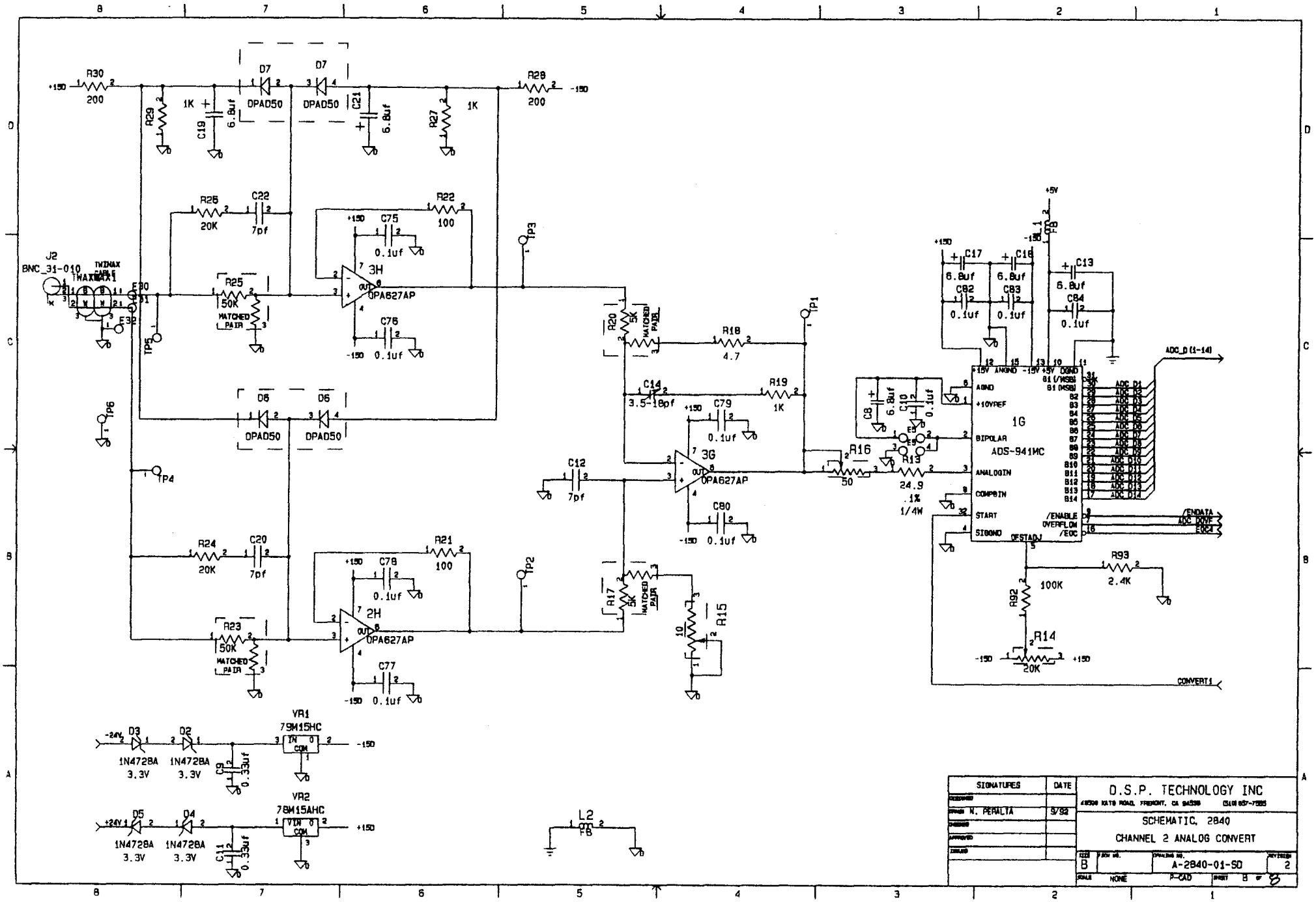
SIZE	DRAWING NO.	REV
B	A-2840-01-5D	2

SCALE NONE P-CAD SHEET 4 OF 8


R48
200
D13
D13
OPA050
OPA050
R47
1K
C34
6.8uf
C35
6.8uf
R45
1K
R48
200
R44
20K
C37
7pf
R40
100
C111
0.1uf
J1
BNC_31-010
TMAX2
E23
E24
E39
R43
50K
MATCHED PAIR
3L
OPA627AP
C105
0.1uf
TP11
TP9
R38
5K
MATCHED PAIR
R36
4.7
C29
3.5-18pf
R37
1K
C115
0.1uf
TP12
D12
D12
OPA050
OPA050
TP10
3K
OPA627AP
C27
7pf
C116
0.1uf
R42
20K
C35
7pf
R39
100
C112
0.1uf
R41
50K
MATCHED PAIR
2L
OPA627AP
C81
0.1uf
TP8
R35
5K
MATCHED PAIR
R33
10
R34
50
R31
24.9
.1%
1/4W
C23
6.8uf
C25
0.1uf
+5V
C32
6.8uf
C33
6.8uf
C106
0.1uf
C108
0.1uf
C28
6.8uf
C113
0.1uf
ADC_A (1-14)
1K
BIPOLAR
ADS-941MC
AGND
+10VREF
ANALOGIN
COMPBIN
START
SIGGND
OFSTADJ
/ENABLE
OVERFLOW
/EOC
/ENDATA
ADC_OVF
EOC1
R87
2.4K
100K
R86
R32
20K
CONVERT1
VR3
79M15HC
D9
D8
1N4728A
3.3V
1N4728A
3.3V
C24
0.33uf
-15A
VR4
78M15AHC
D11
D10
1N4728A
3.3V
1N4728A
3.3V
C26
0.33uf
+15A
L4
FB
SIGNATURES
DATE
N. PERALTA
9/92
O.S.P. TECHNOLOGY INC
SCHEMATIC, 2840
CHANNEL 1 ANALOG CONVERT
SIZE
B
DRAWING NO.
A-2840-01-SD
REV
2
SCALE
NONE
P-CAD
SHEET
5 of 8


R85
200
D25
D25
OPA050
OPA050
R83
200
R84
1K
C64
6.8uf
C66
6.8uf
R82
1K
R81
20K
C67
7pf
R77
100
C101
0.1uf
6K
OPA627AP
C104
0.1uf
J3
BNC_31-010
TMAX4
E33
E34
E35
R80
50K
MATCHED PAIR
TP23
TP21
TP24
D24
D24
OPA050
OPA050
TP22
R79
20K
C65
7pf
R76
100
C102
0.1uf
5K
OPA627AP
C103
0.1uf
R78
50K
MATCHED PAIR
TP20
R75
5K
MATCHED PAIR
R73
4.7
TP19
C59
3.5-18pf
R74
1K
C110
0.1uf
6J
OPA627AP
C114
0.1uf
C57
7pf
R72
5K
MATCHED PAIR
R70
10
R71
50
R68
24.9
.1%
1/4W
C53
6.8uf
C55
0.1uf
1J
ADS-941MC
AGND
+10VREF
BIPOLAR
ANALOGIN
COMPBIN
START
SIGGND
OFSTADJ
AOC_B (1-14)
/ENDATA
ADC_BOVF
EOC2
CONVERT2
C62
6.8uf
C63
6.8uf
C58
6.8uf
C117
0.1uf
C100
0.1uf
C109
0.1uf
R89
2.4K
100K
R88
R69
20K
VR7
79M15HC
D21
D20
1N4728A
3.3V
1N4728A
3.3V
C54
0.33uf
VR8
78M15AHC
D23
D22
1N4728A
3.3V
1N4728A
3.3V
C56
0.33uf
L8
FB
SIGNATURES
DATE
N. PERALTA
9/92
D.S.P. TECHNOLOGY INC
SCHEMATIC, 2840
CHANNEL 3 ANALOG CONVERT
A-2840-01-SD
2
NONE
P-CAD


D.S.P. TECHNOLOGY INC
SCHEMATIC, 2840
CHANNEL 4 ANALOG CONVERT
SIGNATURES
DATE
N. PERALTA
9/92
A-2840-01-SD
B
NONE
P-CAD
J4
BNC_31-010
TP17
TP18
TP16
TP15
TP14
TP13
R67
200
R65
200
R66
R64
1K
C49
C51
6.8uf
D19
D18
OPA050
R63
20K
C52
7pf
R59
100
C72
C71
0.1uf
+15C
-15C
6G
5G
OPA627AP
R62
R60
50K
MATCHED PAIR
R61
20K
C50
7pf
R58
100
C68
C99
0.1uf
R57
R54
5K
R55
4.7
C44
3.5-18pf
R56
1K
C69
C70
0.1uf
6F
OPA627AP
C42
7pf
R52
10
R53
50
R50
24.9
.1%
1/4W
1F
ADS-941MC
C38
C40
6.8uf
0.1uf
C47
C48
C43
C107
C73
C74
L5
FB
+5V
ADC_C(1-14)
/ENDATA
ADC CONV
EOC3
CONVERT2
R91
2.4K
R90
100K
R51
20K
VR5
79M15HC
VR6
78M15AHC
D15
D14
D17
D16
1N4728A
3.3V
C39
C41
0.33uf
-24V
+24V
L6
FB


R30
200
+15V
D7
D7
OPAD50
OPAD50
C21
6.8uf
R29
1K
C19
6.8uf
R27
1K
R28
200
-15V
R26
20K
C22
7pf
R22
100
C75
0.1uf
3H
OPA627AP
C76
0.1uf
J2
BNC_31-010
TWINAX CABLE
R25
50K
MATCHED PAIR
TP5
TP3
R20
5K
MATCHED PAIR
R18
4.7
TP1
C14
3.5-18pf
R19
1K
C79
0.1uf
D6
D6
OPAD50
OPAD50
TP6
TP4
C12
7pf
3G
OPA627AP
C80
0.1uf
R16
50
R13
24.9
.1%
1/4W
C17
6.8uf
C18
6.8uf
C82
0.1uf
C83
0.1uf
C13
6.8uf
C84
0.1uf
C8
6.8uf
C10
0.1uf
1G
ADS-941MC
BIPOLAR
ANALOGIN
COMPBIN
START
SIGGND
+10VREF
AGND
+15V
-15V
+5V
DGND
/ENABLE
OVERFLOW
/EOC
ADC_D (1-14)
/ENDATA
ADC OVF
EOC1
CONVERT1
R24
20K
C20
7pf
R21
100
C78
0.1uf
2H
OPA627AP
C77
0.1uf
R23
50K
MATCHED PAIR
R17
5K
MATCHED PAIR
R15
10
R92
100K
R93
2.4K
R14
20K
VR1
79M15HC
VR2
78M15AHC
D3
D2
D5
D4
1N4728A
3.3V
C9
0.33uf
C11
0.33uf
L2
FB
SIGNATURES
DATE
N. PERALTA
9/92
D.S.P. TECHNOLOGY INC
SCHEMATIC, 2840
CHANNEL 2 ANALOG CONVERT
A-2840-01-SD
B
NONE
P-CAD

SYMBOLS:

- CAMAC EDGE CONNECTOR
- EXTERNAL CONNECTOR
- —( ) CONTINUE ON SAME SHEET
- CONTINUE ON DIFFERENT SHEET
- UNUSED PIN
- JUMPERS

STANDARD CONFIGURATION

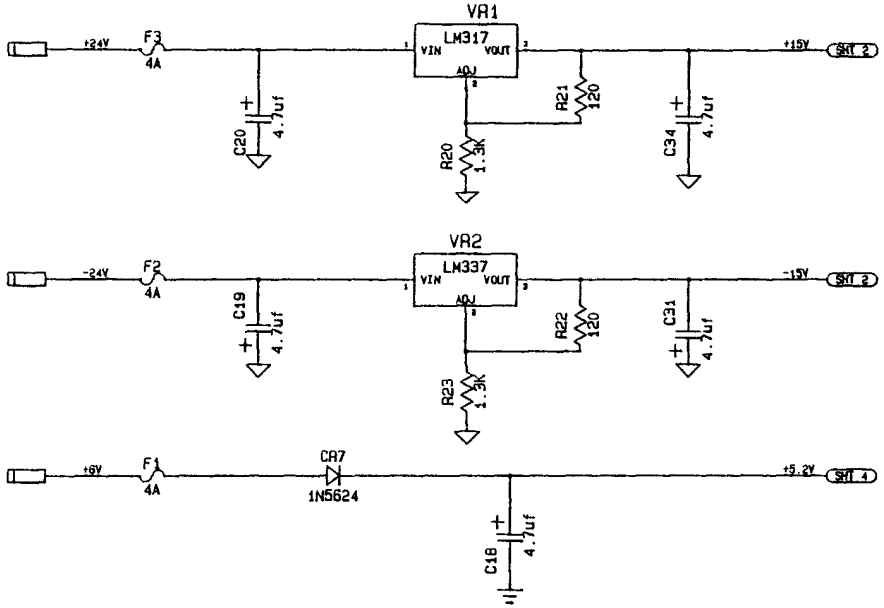
MODE	INSTALL
BIPOLAR	B1' (4 PLACES)
4012A	TRAQ II (2 PLACES)
10VFS	E7 - E8 (4 PLACES) E9 - E10 (4 PLACES)

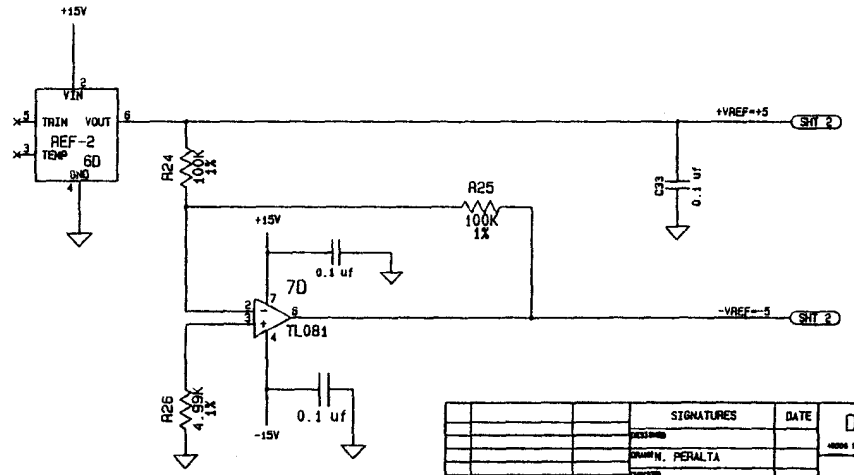
OPTIONAL CONFIGURATION

MODE	INSTALL
UNIPOLAR	UNI (4 PLACES)
20VFS	E7 - E8, E9 - E10 } NOT INSTALLED
4012	TRAQ I (3 PLACES) E1 - E2, E3 - E4, E5 - E6 } ONLY ON ONE UNIT IN THE SYSTEM

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE IN OHMS.
3. ⏚ DENOTES ANALOG GROUND
4. ⏚ DENOTES DIGITAL GROUND
5. * NOT USED





REV	DESCRIPTION	DATE
	PROD RELEASE	
C	ECO 1006	2/9/89
C	ECO 1005	11/15/88
B	ECO'S 1001-1004	

REVISIONS

SIGNATURES

DRAWN N. PERALTA

DATE

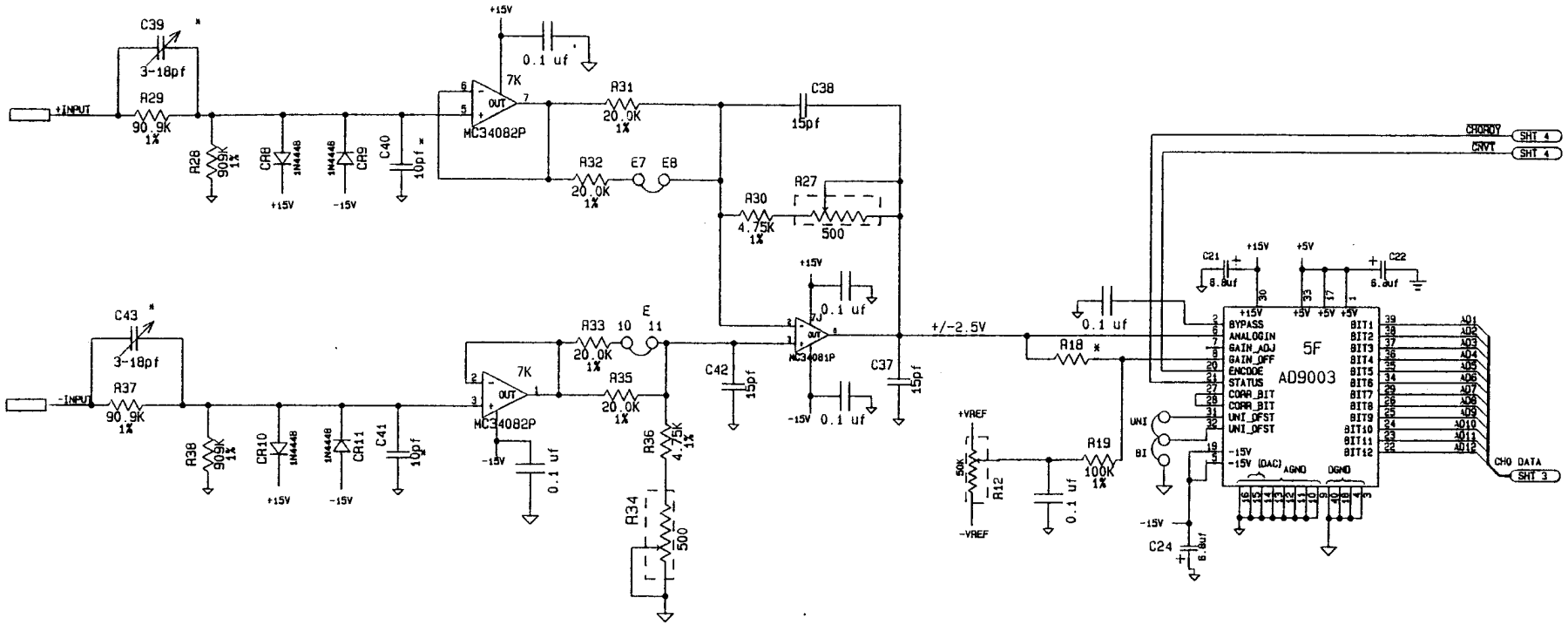
D S P TECHNOLOGY INC

SCHEMATIC, 2860

1MHZ/12 BIT/4 CHANNEL TRAQ ADC

SIZE: D | DSN NO.: 01 | DRAWING NO.: 2860-01-SD | REVISION: C

SCALE: NONE | SHEET 1 OF 4



1 OF 4 IDENTICAL CHANNELS

REV	DESCRIPTION	DATE
C	ECO 1005	11/16/88

REVISIONS

SIGNATURES	DATE
DESIGNED	
DRAWN N. PERALTA JR.	
CHECKED	
APPROVED	
ISSUED	

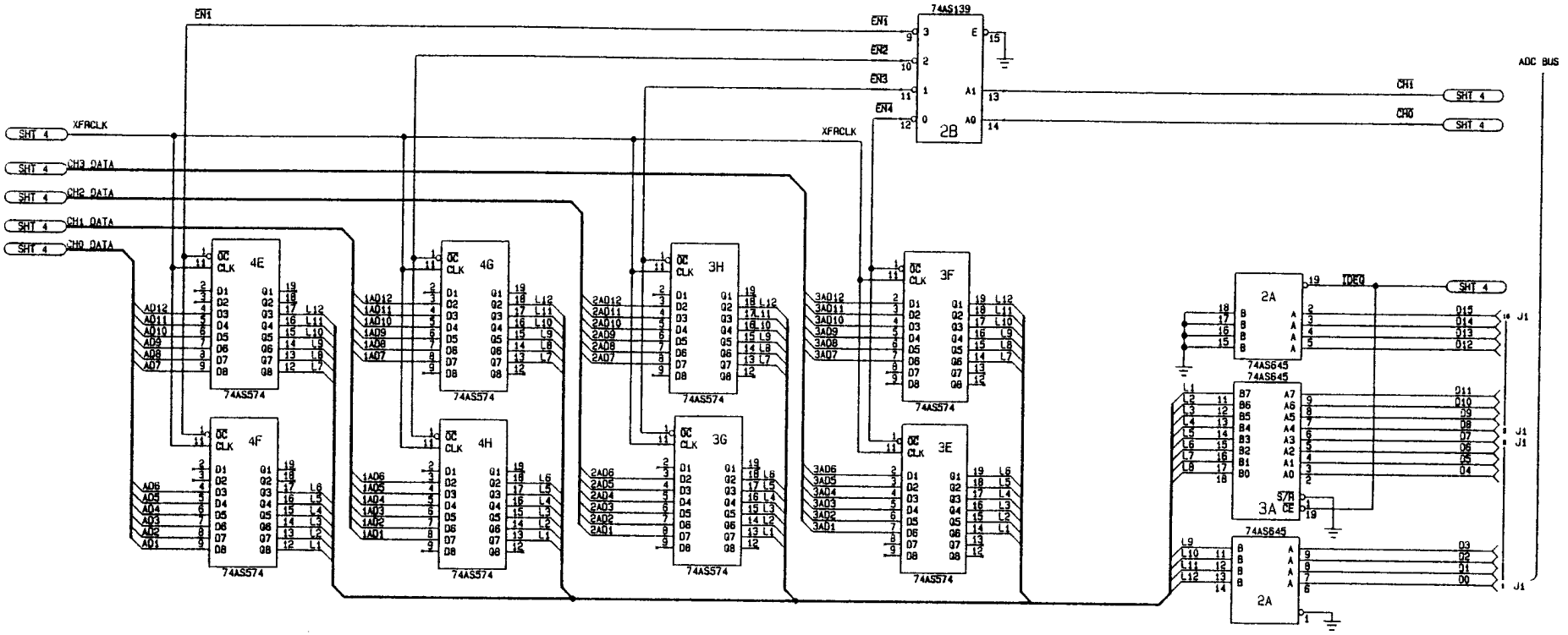
D S P TECHNOLOGY INC

SCHEMATIC, 2860

1MHZ/12 BIT/4 CHANNEL TRAQ ADC

SIZE	FSCM NO.	DRAWING NO.	REVISION
		2860-01-SD	C

SCALE NONE SHEET 2 OF 4



REV	DESCRIPTION	DATE
C	ECO 1004	11/16/88

REVISIONS

SIGNATURES	DATE
DESIGNED	
DRAWN N. PERALTA JR.	9-24
CHECKED	
APPROVED	
ISSUED	

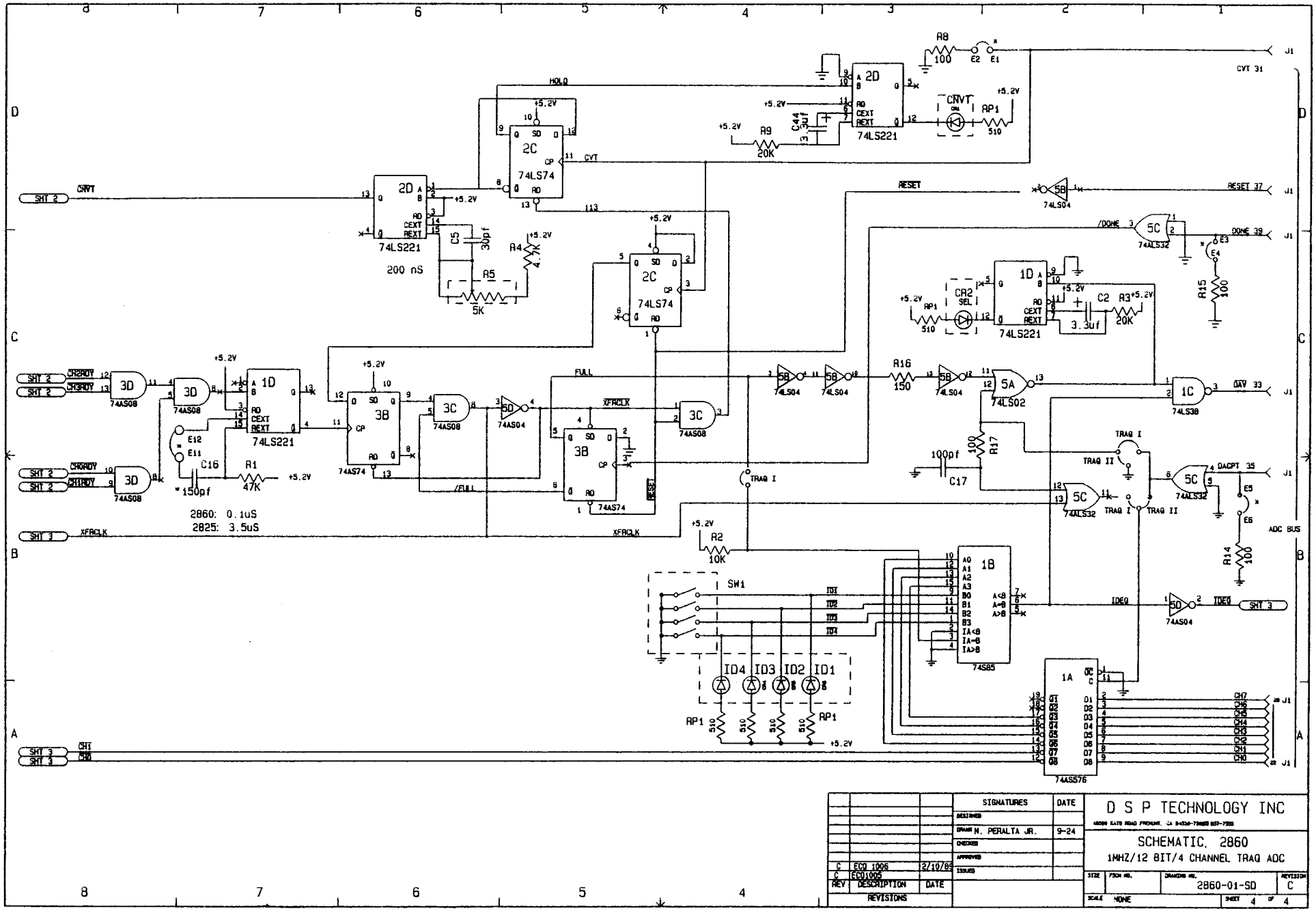
D S P TECHNOLOGY INC

SCHEMATIC, 2860

1MHZ/12 BIT/4 CHANNEL TRAQ ADC

SIZE	FSCM NO.	DRAWING NO.	REVISION
		2860-01-SD	C

SCALE NONE SHEET 3 OF 4



REV	DESCRIPTION	DATE
C	ECO 1006	2/10/86
C	ECO1005	

REVISIONS

SIGNATURES	DATE
DESIGNED	
DRAWN N. PERALTA JR.	9-24
CHECKED	
APPROVED	
ISSUED	

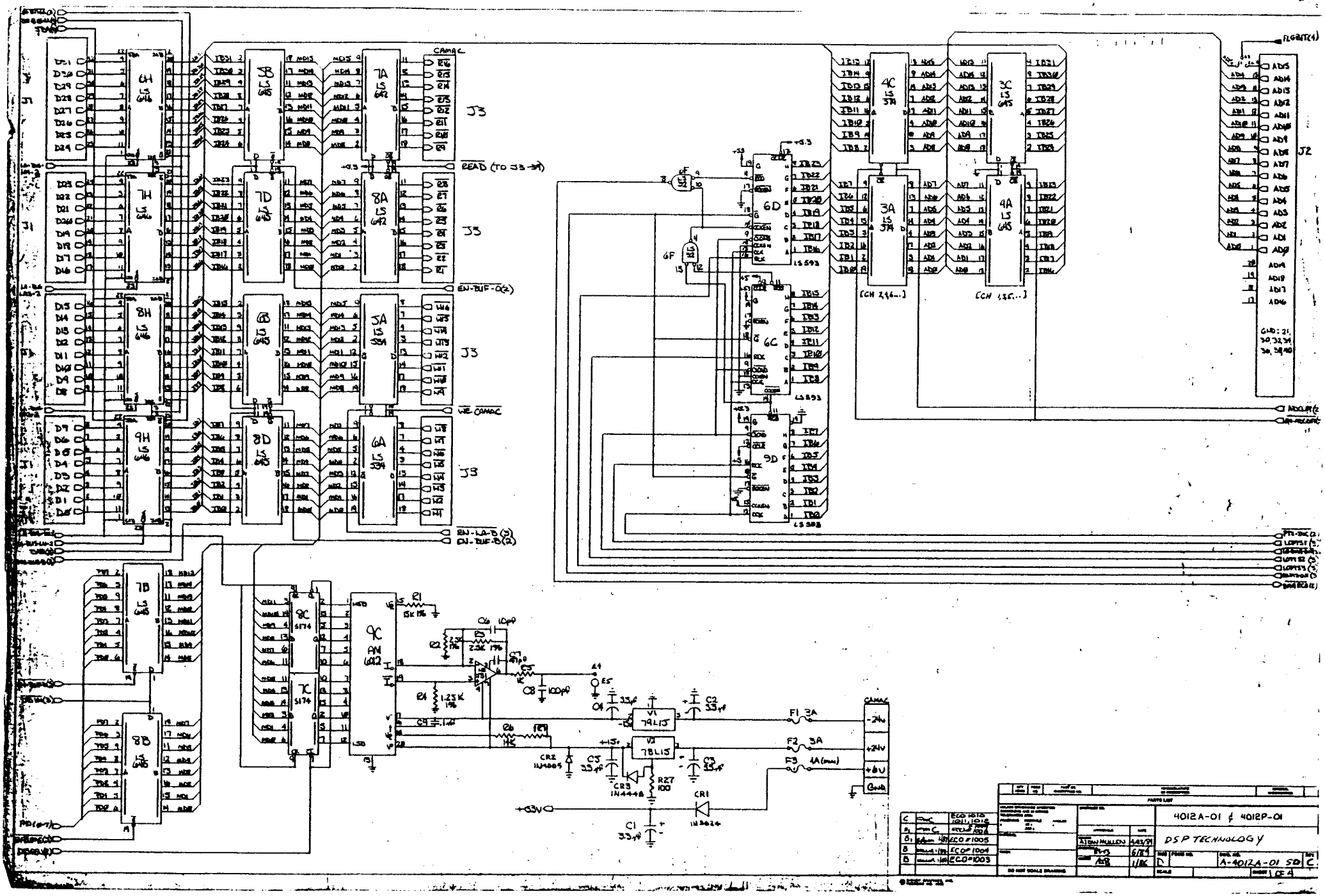
D S P TECHNOLOGY INC

SCHEMATIC, 2860

1MHZ/12 BIT/4 CHANNEL TRAQ ADC

SIZE	FSCM NO.	DRAWING NO.	REVISION
		2860-01-SD	C

SCALE NONE SHEET 4 OF 4



C		ECO 1012	
B		ECO 1010	
A		ECO 1005	
0		ECO 1004	
D		ECO 1003	

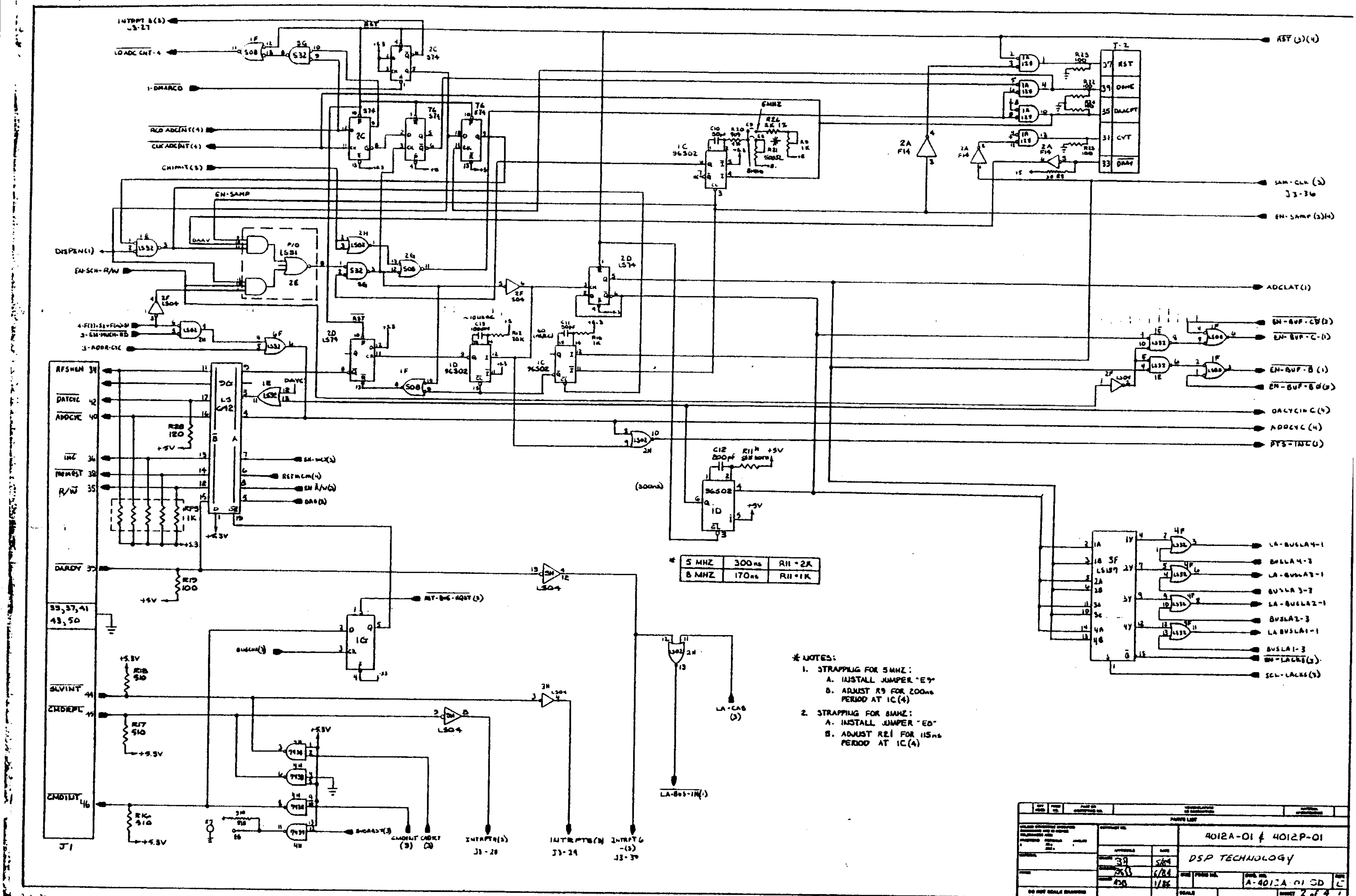
4012A-01 & 4012P-01

DSP TECHNOLOGY

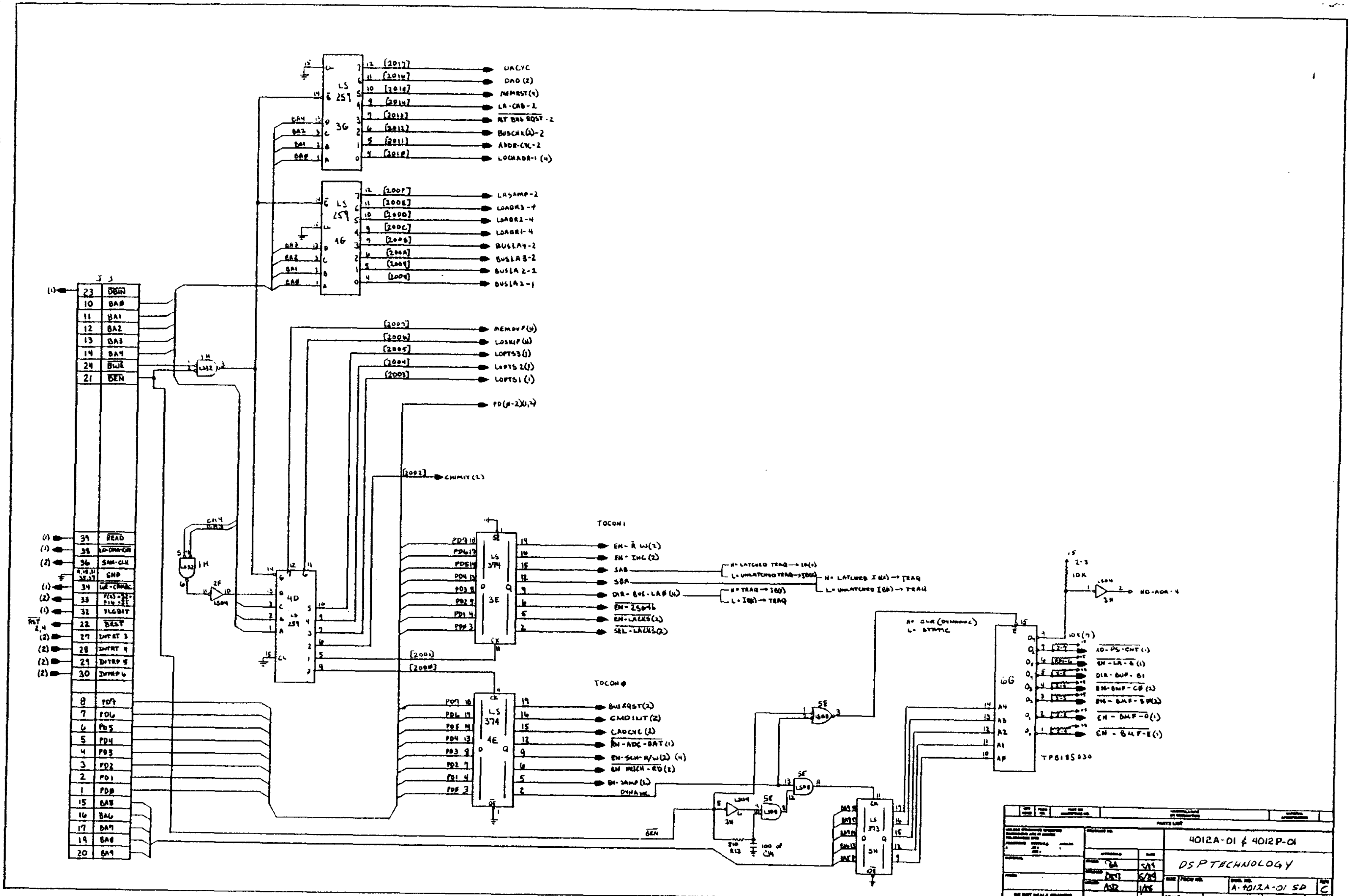
A-4012A-01 SD C

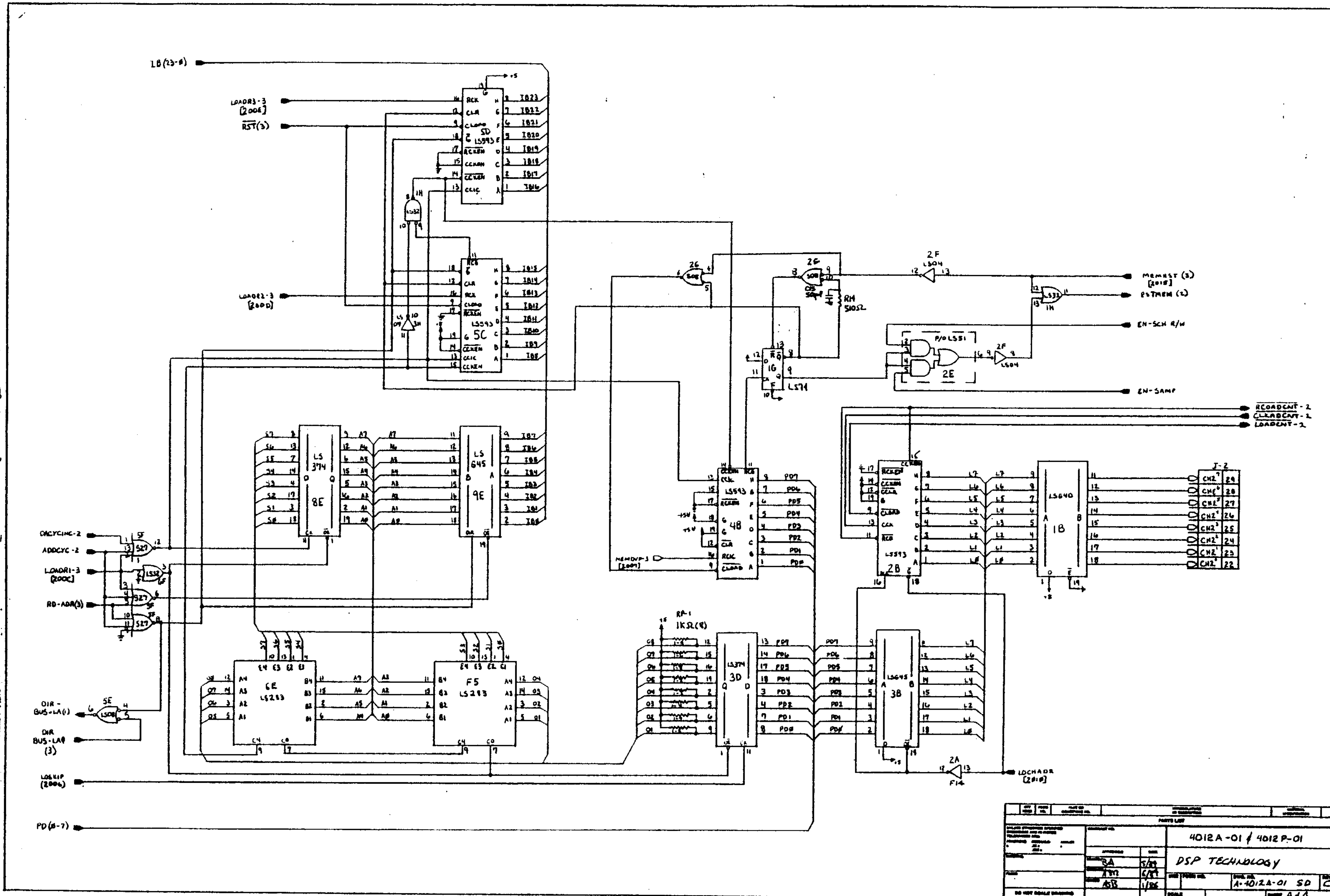
SCALE

SHEET OF 4

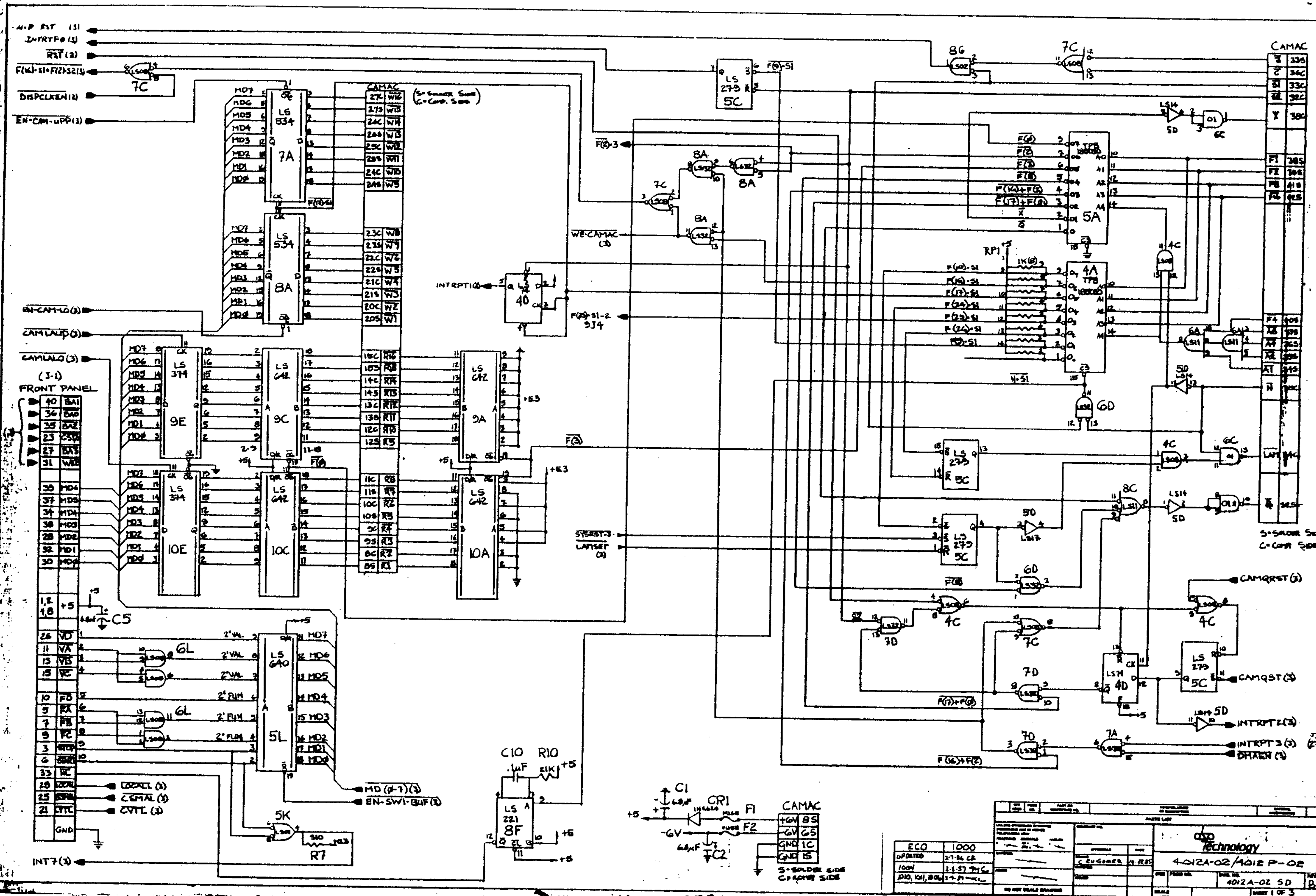


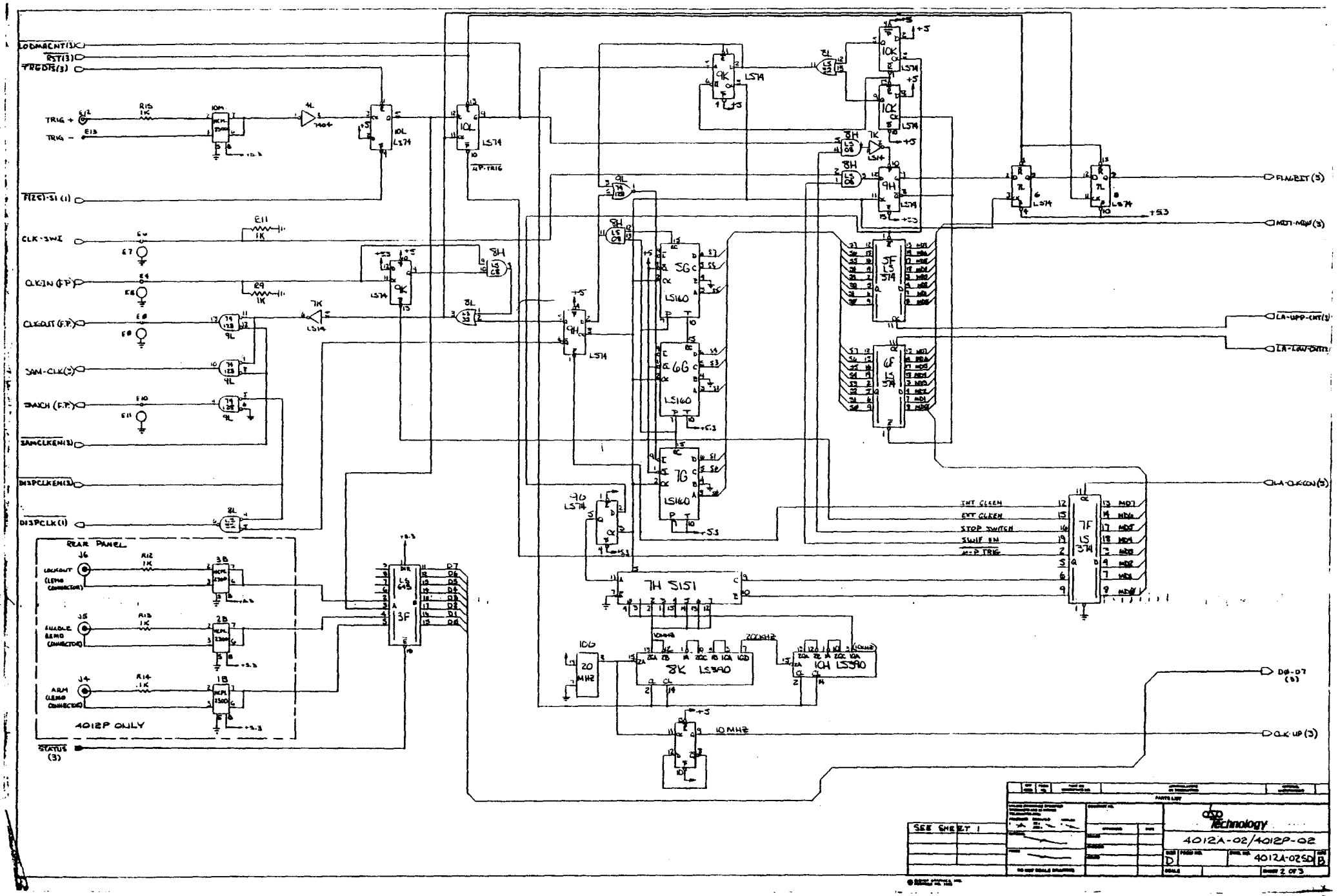
INTRPT 3(3) J3-27
LOAD ADC CNT-4
1-DMARCQ
RLD ADC CNT(4)
CLK ADC CNT(4)
CHIMIT(3)
EN-SAMP
DISPEN(1)
EN-SCH-R/W
3-ADDR-CYC
RFSHEN
DATCYC
ADDCYC
INC
MEMRST
R/W
DARDY
33, 37, 41 43, 50
SLVINT
CMDIEPL
CMDINT
J1
+5V
RST (3)(4)
SAM-CLK (3) J3-36
EN-SAMP (3)(4)
ADCLAT(1)
EN-BUF-CB(3)
EN-BUF-C-(1)
EN-BUF-B(1)
EN-BUF-B d(3)
DACYCINC(4)
ADDCYC(4)
PTS-INC(1)
LA-BUSLA4-1
BUSLA4-3
LA-BUSLA3-1
BUSLA3-3
LA-BUSLA2-1
BUSLA2-3
LA-BUSLA1-1
BUSLA1-3
EN-LACHS(3)
SCL-LACHS(3)
LA-CAS (3)
LA-BUS-IN(1)
INTRPT6(3) J3-29
INTRPT6 -(3) J3-37
RST-BUS-RQST(3)
BUSCHK(3)
EN-INC(3)
RSTMEM(4)
EN R/W(3)
DAS(3)
J-2
RST
DONE
DMACPT
CVT
DMAV
96S02
LS74
LS157
6MHZ
(300ns)
| 5 MHZ | 300ns | R11 = 2K |
| 8 MHZ | 170ns | R11 = 1K |
* NOTES:
1. STRAPPING FOR 5MHZ:
A. INSTALL JUMPER "E9"
B. ADJUST R9 FOR 200ns PERIOD AT 1C(4)
2. STRAPPING FOR 8MHZ:
A. INSTALL JUMPER "E8"
B. ADJUST R21 FOR 115ns PERIOD AT 1C(4)
4012A-01 & 4012P-01
DSP TECHNOLOGY
A-4012A-01 SD
C
SHEET 2 of 4

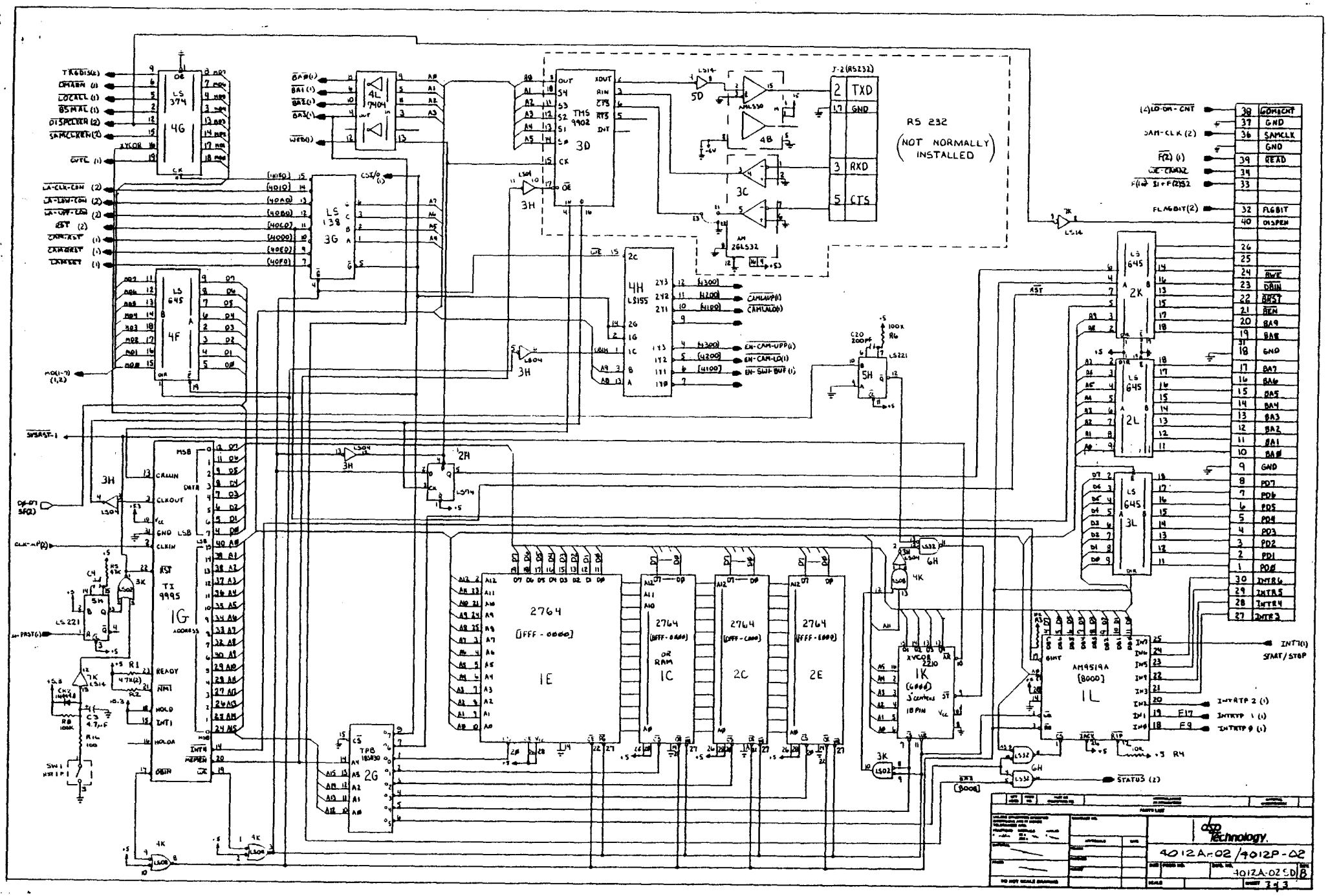

UACYC
DAO (2)
MEMRST(4)
LA-CAB-2
RT BUS RQST-2
BUSCHK(Ø)-2
ADDR-CK-2
LOCKADR-1 (4)
LASAMP-2
LOADR3-4
LOADR2-4
LOADR1-4
BUSLA4-2
BUSLA3-2
BUSLA2-2
BUSLA2-1
MEMOVF(4)
LOSKIP(4)
LOPTS3(1)
LOPTS2(1)
LOPTS1(1)
CHIMIT(2)
LS 257
3G
4G
4D
LS 374
3E
4E
LS 373
5H
6G
TPB18S030
J3
DBIN
BWE
BEN
READ
SAM-CLK
GND
FLGBIT
RST
INTRT 3
INTRT 4
INTRP 5
INTRP 6
TOCON1
TOCON0
EN-R W(2)
EN-INC(2)
SAB
SBA
DIR-BUS-LAB(4)
EN-25646
EN-LACKS(2)
SEL-LACKS(2)
BUSRQST(2)
CMDINT(2)
CADCYC(2)
EN-ADC-DAT(1)
EN-SCH-R/W(2) (4)
EN MUCH-RD(2)
EN-SAMP(1)
DYNAMIC
H= LATCHED TRAQ
L= UNLATCHED TRAQ
H= CLR (DYNAMIC)
L= STATIC
10K
AD-ADR-4
AD-PS-CNT(1)
EN-LA-B(1)
DIR-BUF-B1
EN-BUF-CB(2)
EN-BUF-D
EN-BUF-O(1)
EN-BUF-E(1)
4012A-01 & 4012P-01
DSP TECHNOLOGY
A-4012A-01 SD
C
DO NOT SCALE DRAWING
PARTS LIST

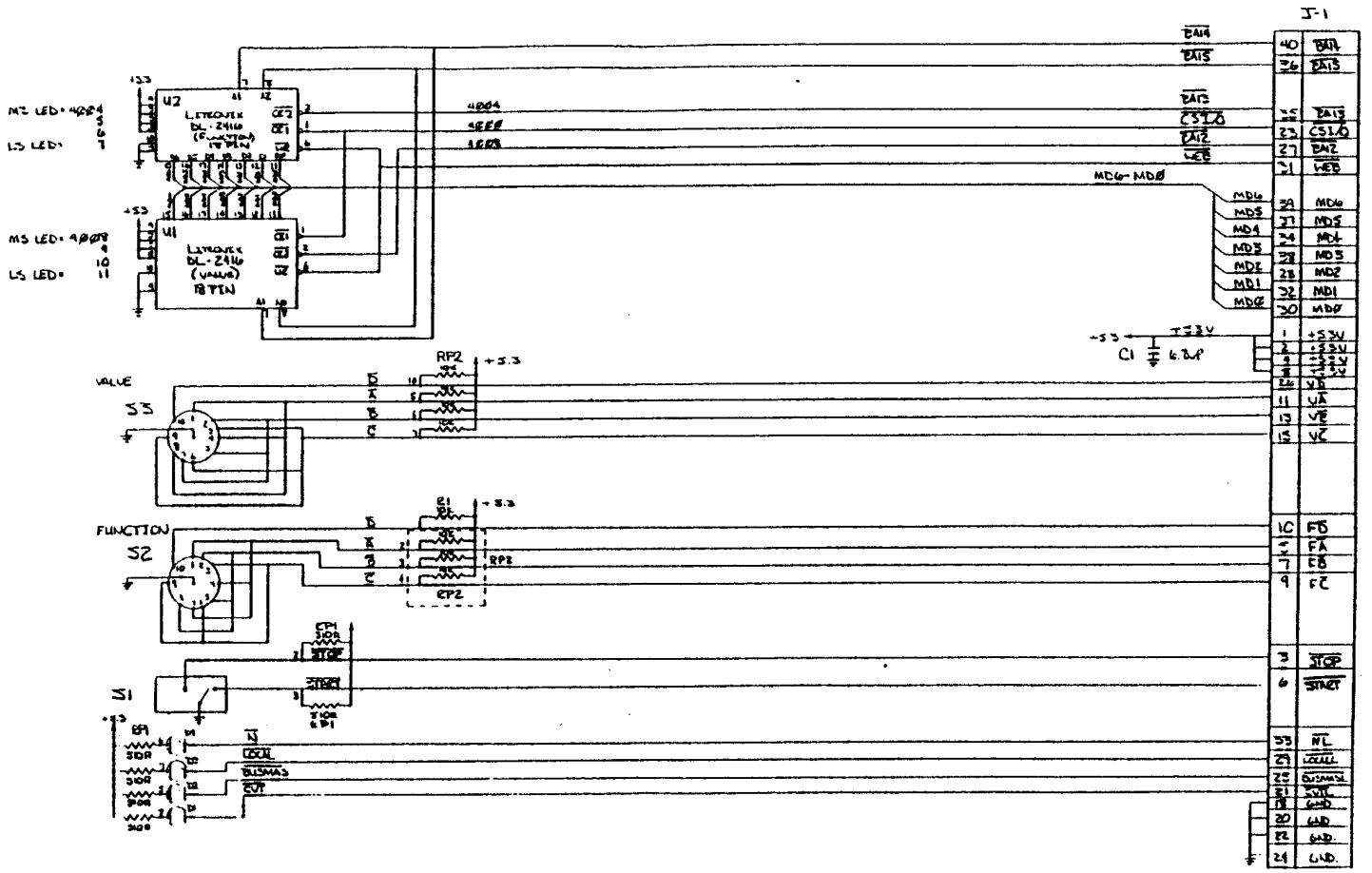


IB(23-0)
LOADR3-3 [2006]
RST(3)
LOADR2-3 [200D]
LS593 5D
LS593 5C
IB23 IB22 IB21 IB20 IB19 IB18 IB17 IB16
IB15 IB14 IB13 IB12 IB11 IB10 IB9 IB8
IB7 IB6 IB5 IB4 IB3 IB2 IB1 IB0
LS374 8E
LS645 9E
A7 A6 A5 A4 A3 A2 A1 A0
LS283 6E
LS283 F5
DACYCINC-2
ADDCYC-2
LOADR1-3 [200C]
RD-ADR(3)
DIR-BUS-LA(1)
DIR BUS-LA0 (3)
LOSKIP (2006)
PD(0-7)
MEMRST (3) [2015]
RSTMEM (2)
EN-SCH R/W
EN-SAMP
RLOADCNT-2
CLRADCNT-2
LOADCNT-2
MEMDVP-3 [2007]
LS593 4B
LS593 2B
LS640 1B
LS374 3D
LS645 3B
LS74 1G
P/O LS51 2E
RP-1 1KΩ(8)
PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0
L7 L6 L5 L4 L3 L2 L1 L0
J-2
CH2 29 28 27 26 25 24 23 22
LDCHADR [2010]
2A F14
2F LS04
2G
1H
4012A-01 / 4012P-01
DSP TECHNOLOGY
A-4012A-01 SD
C


CAMAC
FRONT PANEL
(J-1)
Technology
4012A-02/4012P-02
4012A-02 SD
SHEET 1 OF 3
ECO
1000
UPDATED
S=SOLDER SIDE
C=COMP. SIDE
INT7(3)
CAMQRST(3)
CAMQST(3)
INTRPT2(3)
INTRPT3(3)
DMAEN(3)
WE-CAMAC (3)
INTRPT1(3)
SYSRST-3
LAMSET (3)
MD(Ø-7)(3)
EN-SW1-BUF(3)
LOCALL (3)
CSMAL (3)
CVTL (3)
DISPCLKEN(1)
EN-CAM-uPP(3)
EN-CAM-LO(3)
CAMLAUP(3)
CAMLALO(3)
C1
CR1
F1
F2
C5
C10
R10
R7
RP1


LOADMCNT(3)
RST(3)
TRIG(3)
TRIG +
TRIG −
FIFO1-S1 (1)
CLK-SWI
CLK-IN (F.P.)
CLKOUT (F.P.)
SAM-CLK(3)
SWCH (F.P.)
SAMCLKEN(3)
DISPCLKEN(3)
DISPCLK(1)
REAR PANEL
4012P ONLY
STATUS (3)
FLAGBIT(3)
MUX-MUX(3)
LA-UPP-CNT(3)
LA-LOW-CNT(3)
LA-CLKCON(3)
INT CLKEN
EXT CLKEN
STOP SWITCH
SWIP EN
M-P TRIG
D0-D7 (3)
CLK UP(3)
10MHZ
20MHZ
SEE SHEET 1
Technology
4012A-02/4012P-02
4012A-02SD
SHEET 2 OF 3


RS 232
(NOT NORMALLY INSTALLED)
J-2 (RS232)
2 TXD
7 GND
3 RXD
5 CTS
TMS 9902
AM 26LS32
AM 26LS31
2764
(0FFF - 0000)
1E
2764
(BFFF - 8000)
OR RAM
1C
2764
(DFFF - C000)
2C
2764
(FFFF - E000)
2E
TI 9995
1G
2K
2L
3L
1K
AM9519A
(8000)
1L
4012A-02/4012P-02
4012A-02 SD
cxp technology.

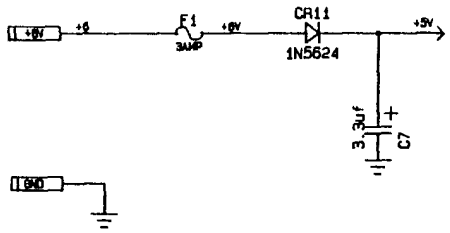


		DSP Technology	
		4012-03	
		4012-03-SD	A

SYMBOLS:

- CAMAC EDGE CONNECTOR
- EXTERNAL CONNECTOR
- —( ) CONTINUE ON SAME SHEET
- CONTINUE ON DIFFERENT SHEET
- UNUSED PIN
- JUMPERS

5004A		5003A	
E2 - E3	(512K)	E1 - E2	(256K)
E4 - E5		E3 - E4	
E6 - E7		E5 - E6	
E8 - E9		E7 - E8	
		4T[9] - GND	



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.

REV	DESCRIPTION	DATE
C	ECO 010212 005004	2/92
A	PROD RELEASE	

REVISIONS

SIGNATURES		DATE
DESIGNED	N. PERALTA	9/86
DRAWN	J.CHURCH	6/92
CHECKED		
APPROVED		
ISSUED		

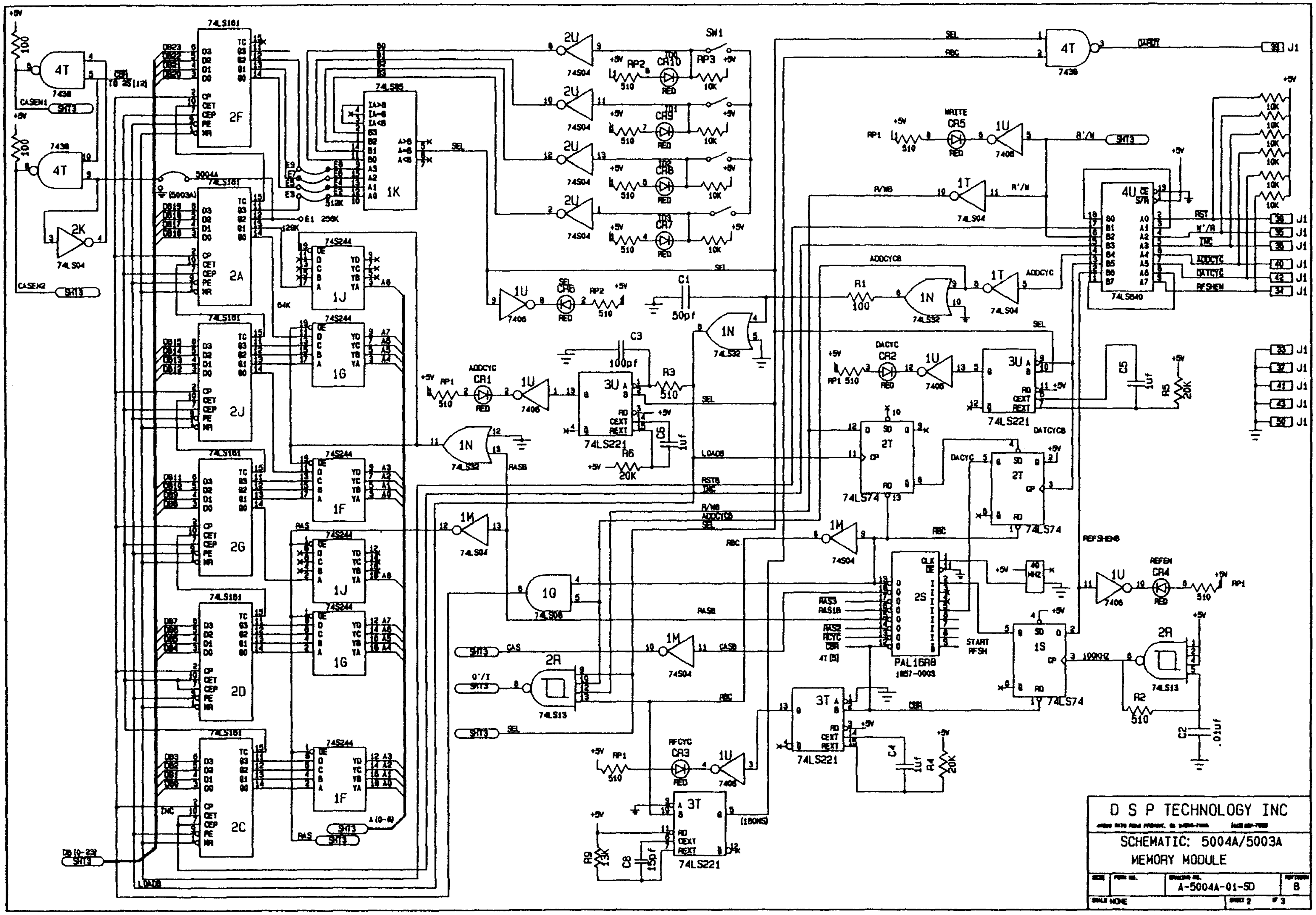
D S P TECHNOLOGY INC

SCHEMATIC: 5004A/5003A
POWER

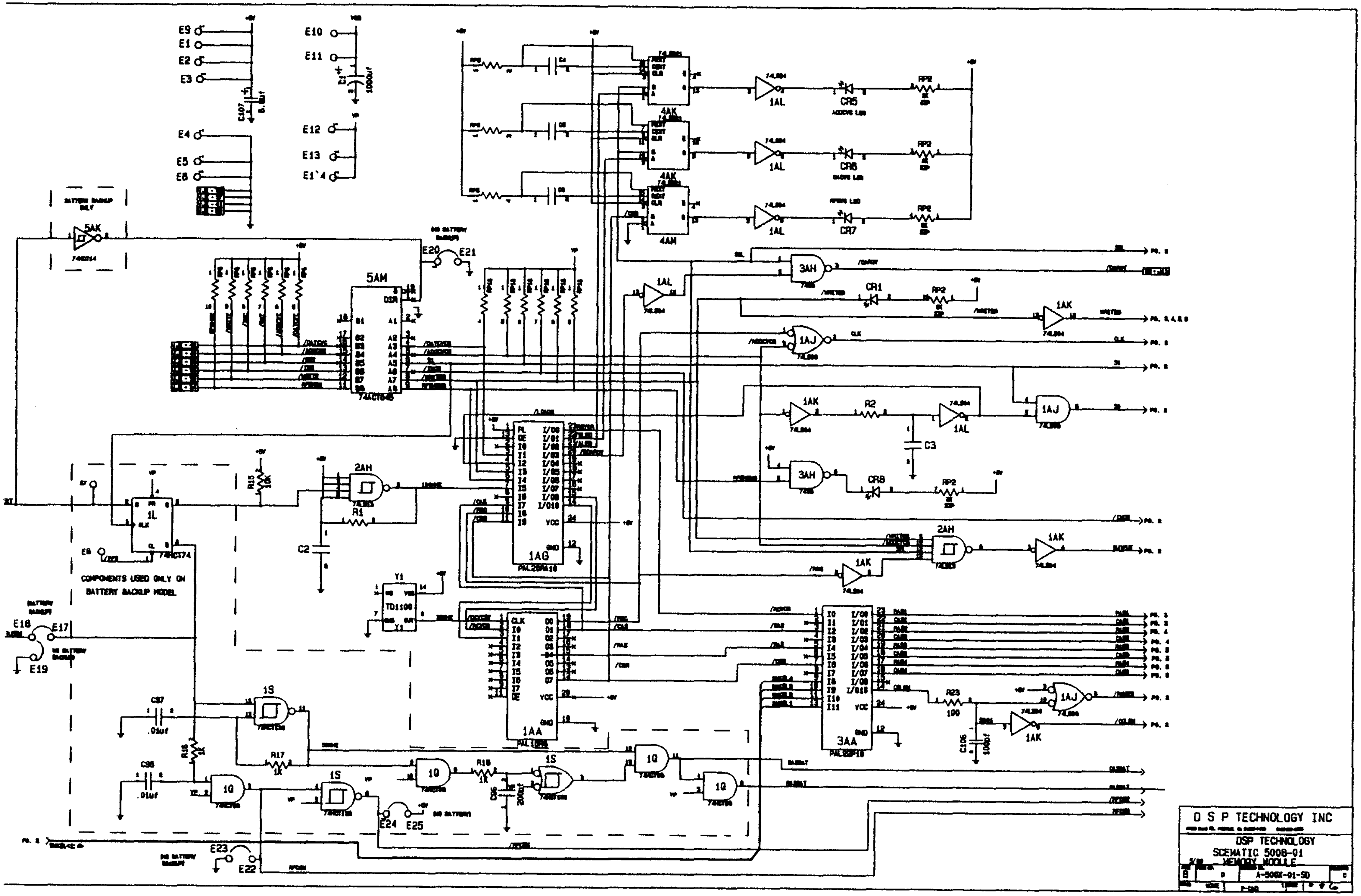
SIZE	DWG NO.	REVISION
B	A-5004A-01-SD	C

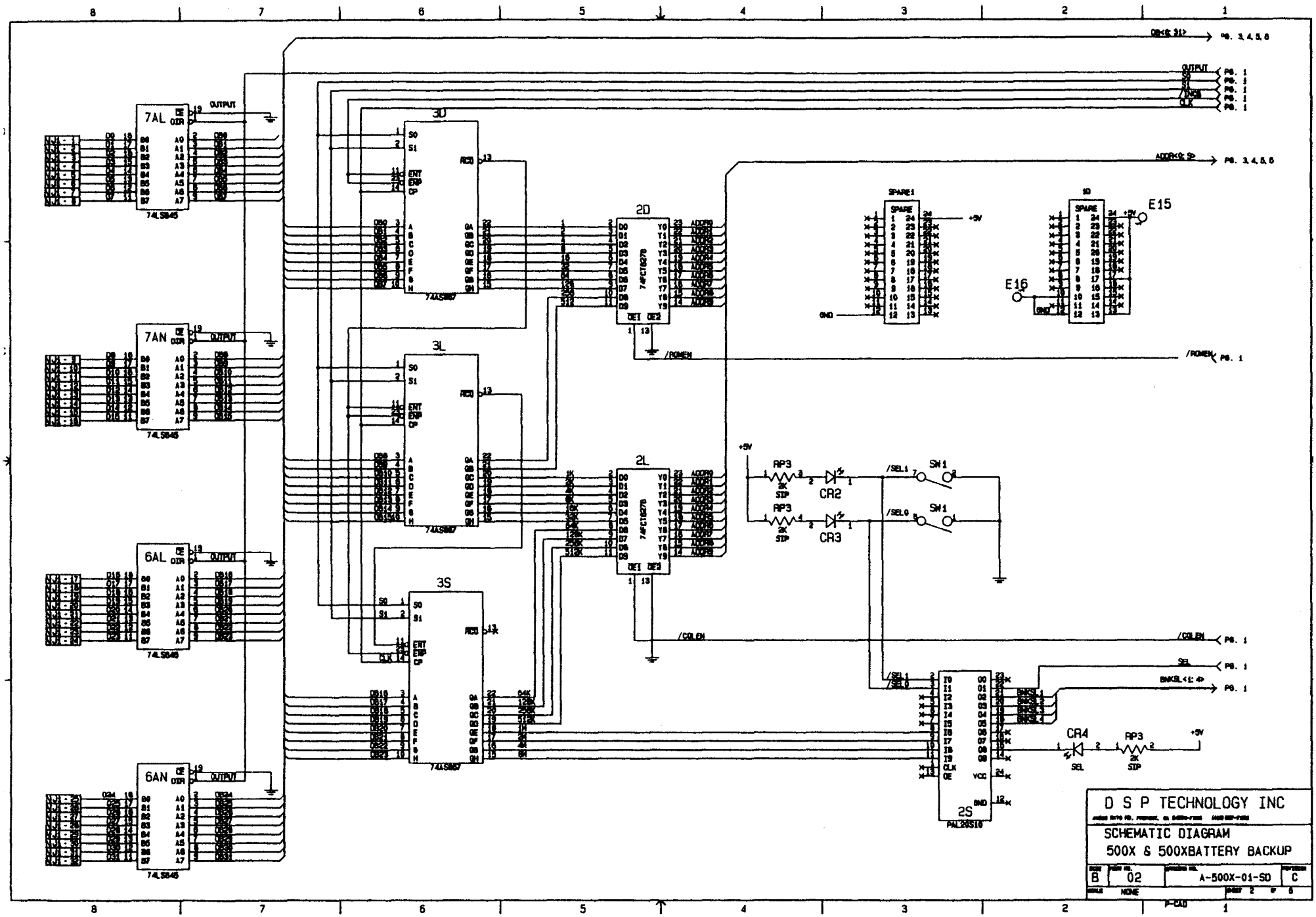
SCALE NONE SHEET 1 OF 3

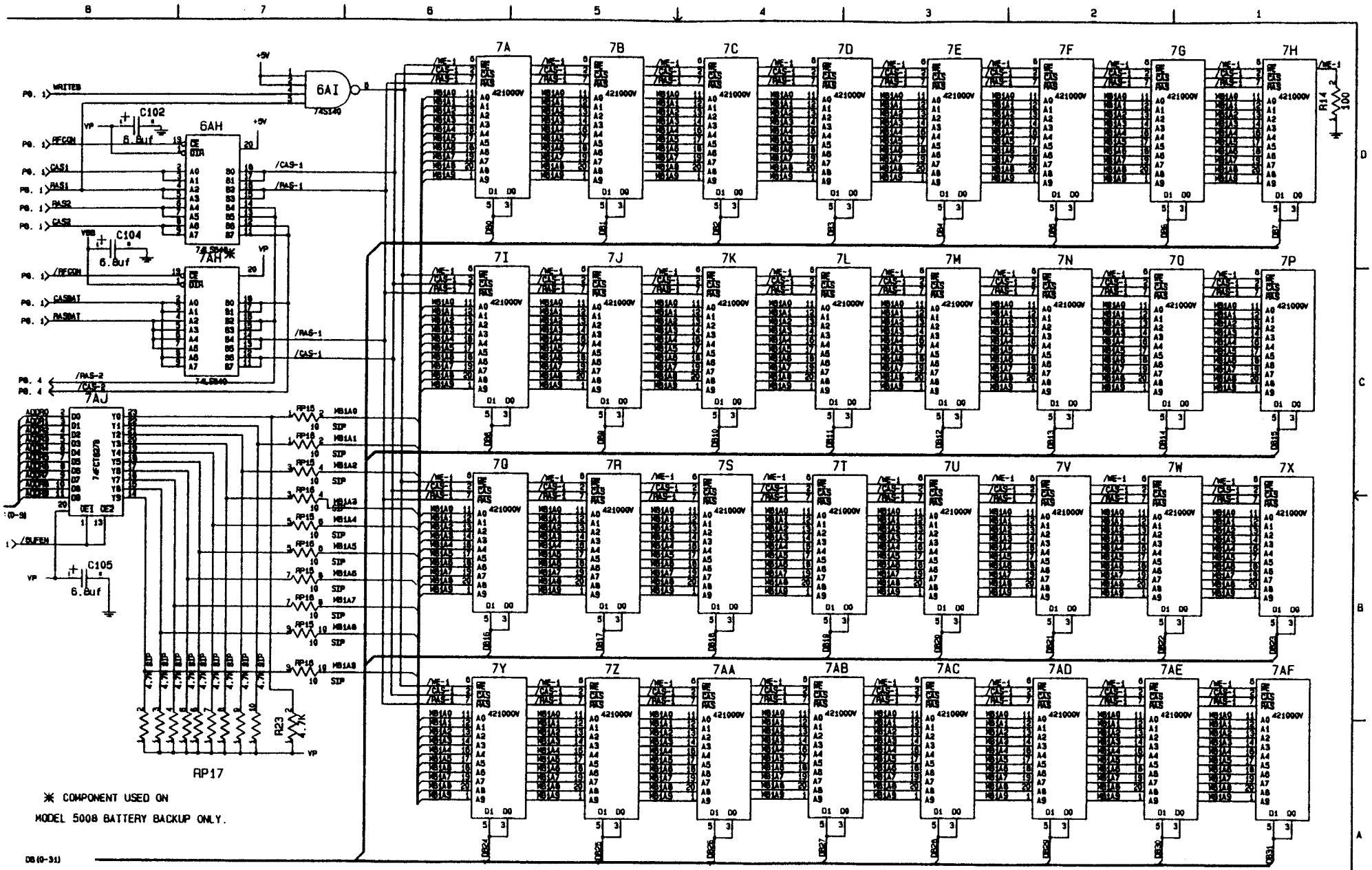
P-CAD


D S P TECHNOLOGY INC
SCHEMATIC: 5004A/5003A
MEMORY MODULE
A-5004A-01-SD
B
NONE
SHEET 2 OF 3

D S P TECHNOLOGY INC
SCHEMATIC: 5004A\5003A
MEMORY MODULE
A-5004A-01 SD
C
MCM6256
74S140
74LS245
AM2966


D S P TECHNOLOGY INC
DSP TECHNOLOGY
SCEMATIC 5008-01
MEMORY MODULE
COMPONENTS USED ONLY ON
BATTERY BACKUP MODEL


7AL
7AN
6AL
6AN
74LS645
OUTPUT
3D
3L
3S
74AS867
2D
2L
74FCT827B
2S
PALCE16S10
SPARE1
SPARE
E15
E16
+5V
GND
RP3
2K
SIP
CR2
CR3
CR4
SW1
/SEL1
/SEL0
SEL
/ROMEN
/COLEN
ADDR<0:3>
DB<0:31>
P8. 1
P8. 3,4,5,6
D S P TECHNOLOGY INC
SCHEMATIC DIAGRAM
500X & 500XBATTERY BACKUP
A-500X-01-SD
B
02
C
NONE
P-CAD



MEMORY BLOCK 1

USED ON MODELS:

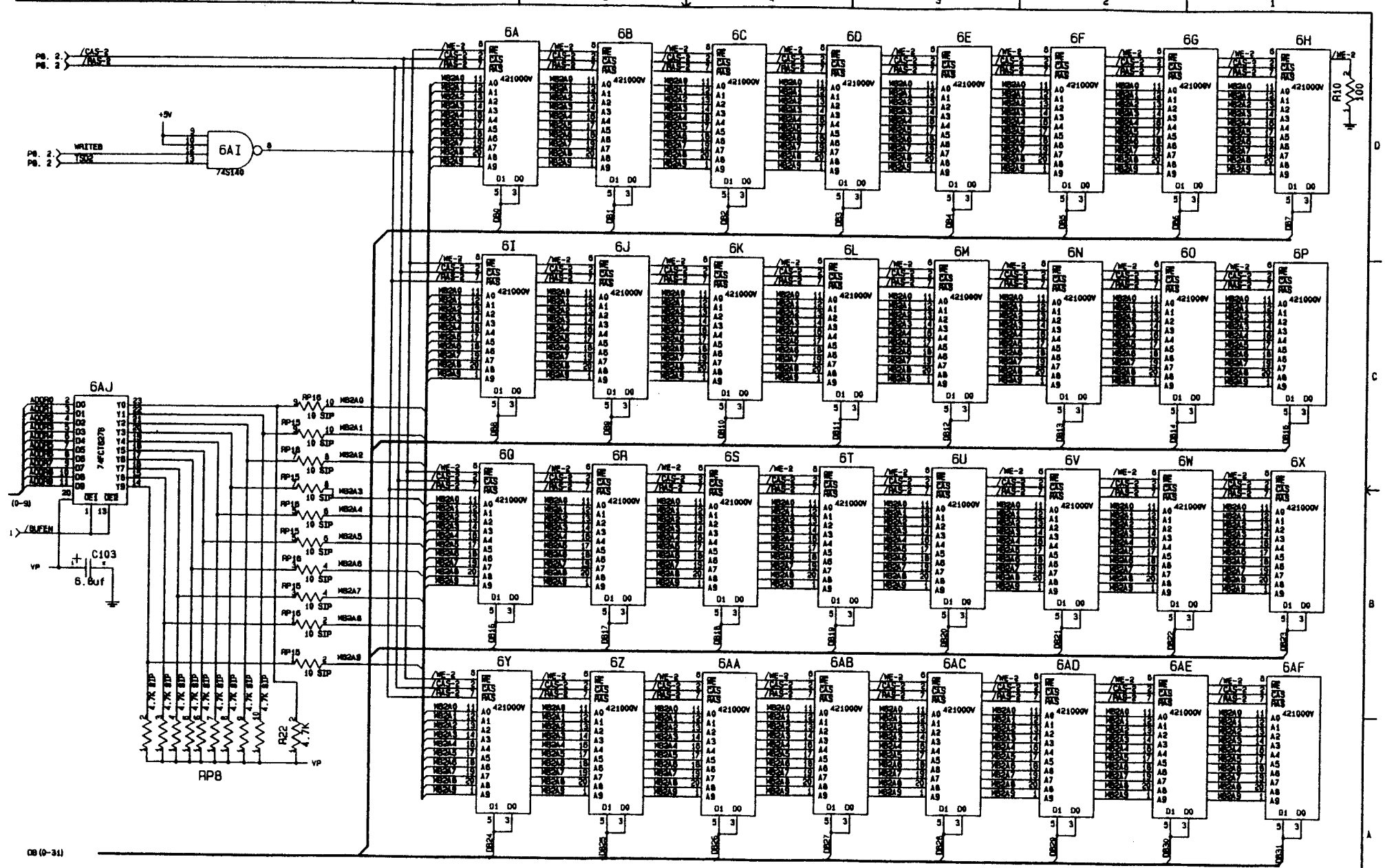
5005	5005BB
5006	5006BB
5007	5007BB
5008	5008BB

D S P TECHNOLOGY INC

MEMORY BLOCK 1 5008-01

B | 5/88 | A-500X-01-SD | C

NONE | SHEET 3 OF 6



MEMORY BLOCK 2

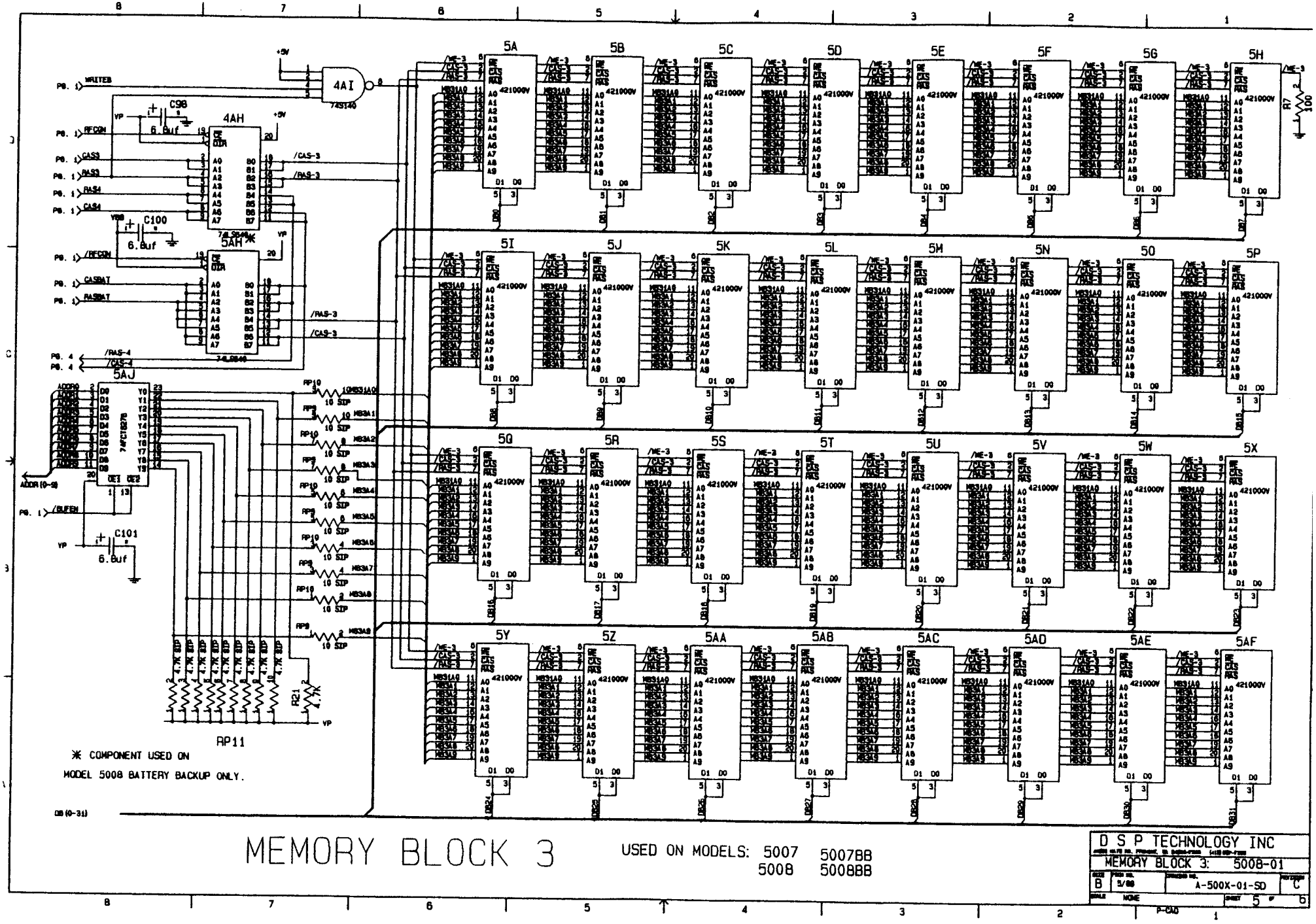
USED ON MODELS: 5006 5006BB
5007 5007BB
5008 5008BB

D S P TECHNOLOGY INC

MEMORY BLOCK 2: 5008-01

SIZE	DRAWING NO.	REVISION
B	A-500X-01-SD	C
SCALE: NONE	SHEET 4 OF 6	

P-CAD



* COMPONENT USED ON
MODEL 5008 BATTERY BACKUP ONLY.

MEMORY BLOCK 3

USED ON MODELS: 5007 5007BB
5008 5008BB

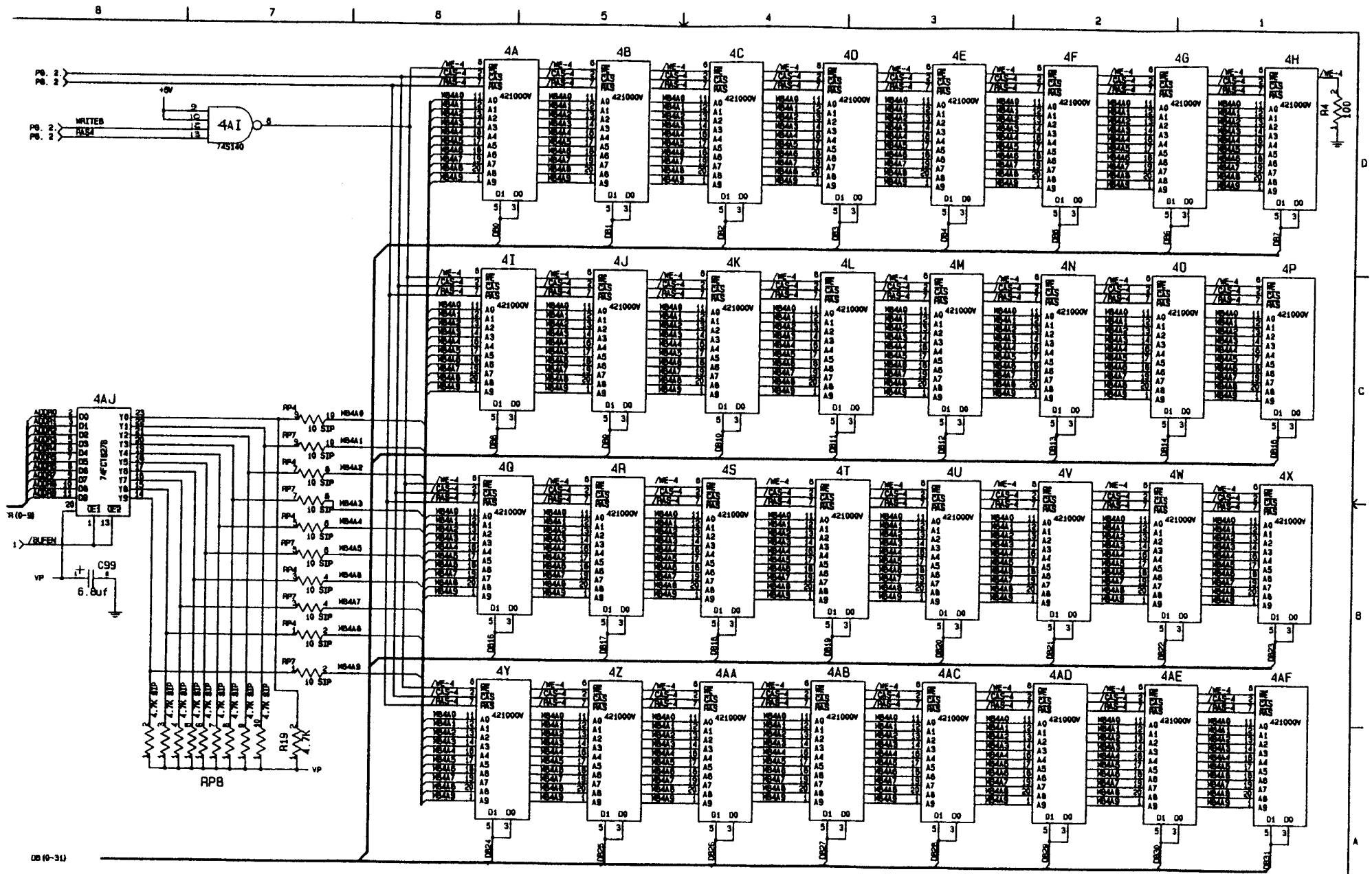
D S P TECHNOLOGY INC

MEMORY BLOCK 3: 5008-01

SIZE	DWG NO.	REV
B	A-500X-01-SD	C

SCALE: NONE SHEET 5 OF 6

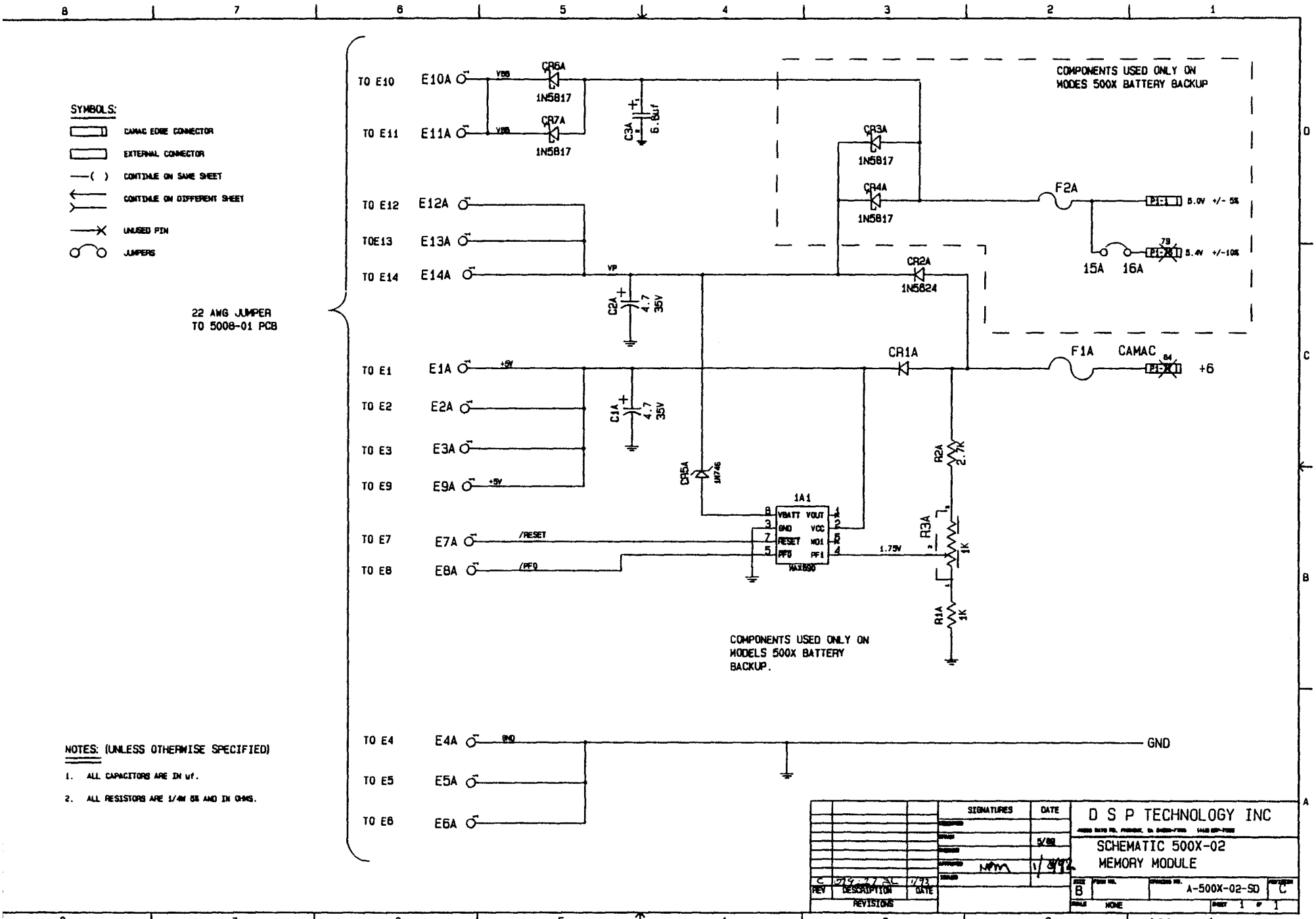
P-CAD

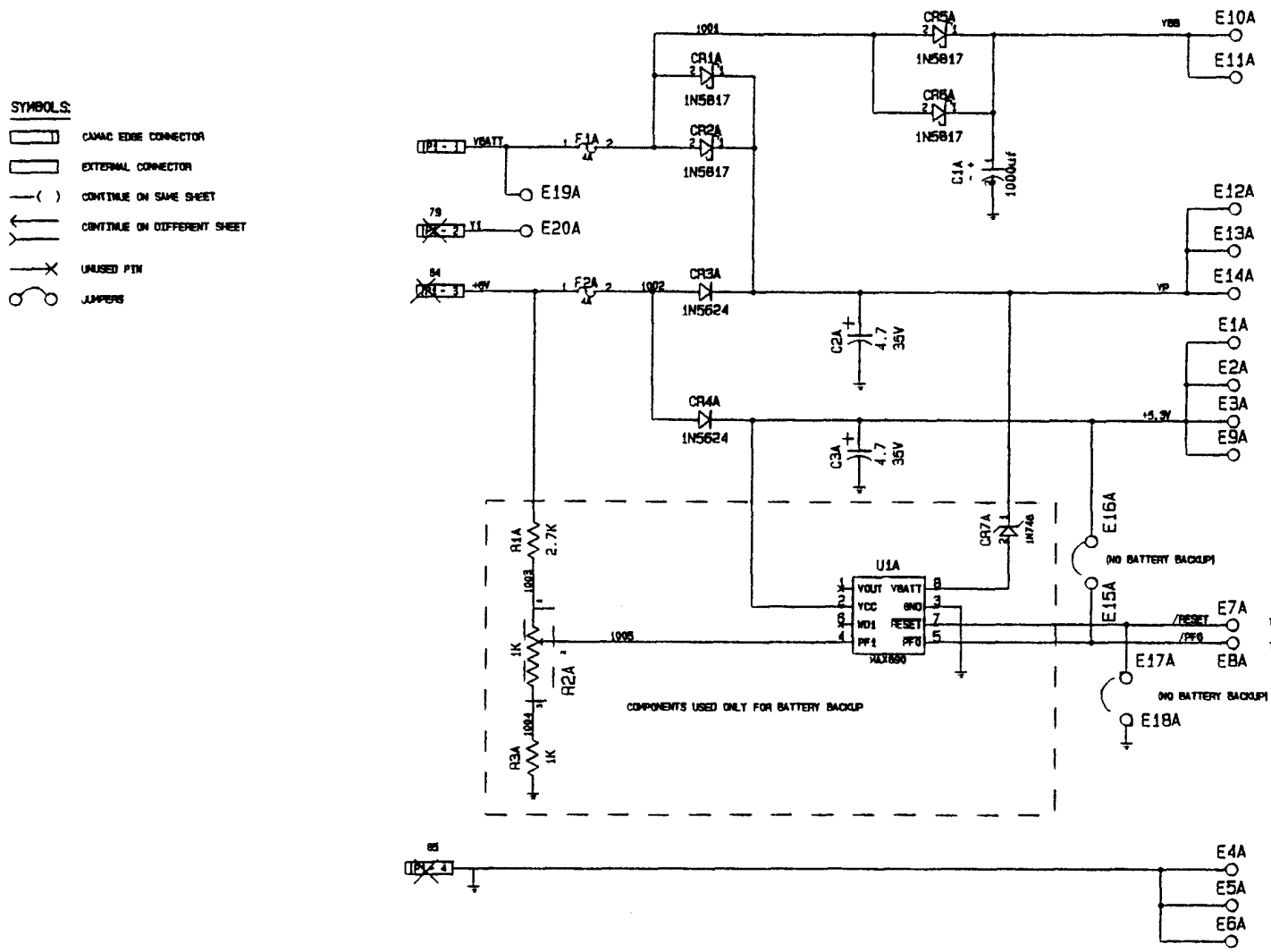


MEMORY BLOCK 4

USED ON MODELS: 5008 & 5008BB

D S P TECHNOLOGY INC		
MEMORY BLOCK 4: 5008-01		
B	5/89	A-500X-01-SD
SCALE: NONE		SHEET 6 OF 6
P-CAD		


SYMBOLS:
CAMAC EDGE CONNECTOR
EXTERNAL CONNECTOR
CONTINUE ON SAME SHEET
CONTINUE ON DIFFERENT SHEET
UNUSED PIN
JUMPERS
22 AWG JUMPER
TO 5008-01 PCB
TO E10
E10A
TO E11
E11A
TO E12
E12A
TOE13
E13A
TO E14
E14A
TO E1
E1A
TO E2
E2A
TO E3
E3A
TO E9
E9A
TO E7
E7A
TO E8
E8A
TO E4
E4A
TO E5
E5A
TO E6
E6A
CR6A
1N5817
CR7A
1N5817
C3A
6.8uf
CR3A
1N5817
CR4A
1N5817
F2A
P1-1
5.0V +/- 5%
P1-2
5.4V +/-10%
15A
16A
CR2A
1N5824
C2A
4.7
35V
CR1A
F1A
CAMAC
+6
C1A
4.7
35V
CR5A
1A1
VBATT
VOUT
GND
VCC
RESET
MR1
PFO
PFI
MAX690
/RESET
/PFO
1.75V
R2A
2.7K
R3A
1K
R1A
1K
COMPONENTS USED ONLY ON MODELS 500X BATTERY BACKUP.
GND
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.
SIGNATURES
DATE
D S P TECHNOLOGY INC
SCHEMATIC 500X-02
MEMORY MODULE
A-500X-02-SD
REVISIONS
DESCRIPTION
DATE
P-CAD



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.

REV	DESCRIPTION	DATE
1	PRODUCTION RELEASE	6/19/92

REVISIONS

	SIGNATURES	DATE
	J.CHURCH	6/19/92

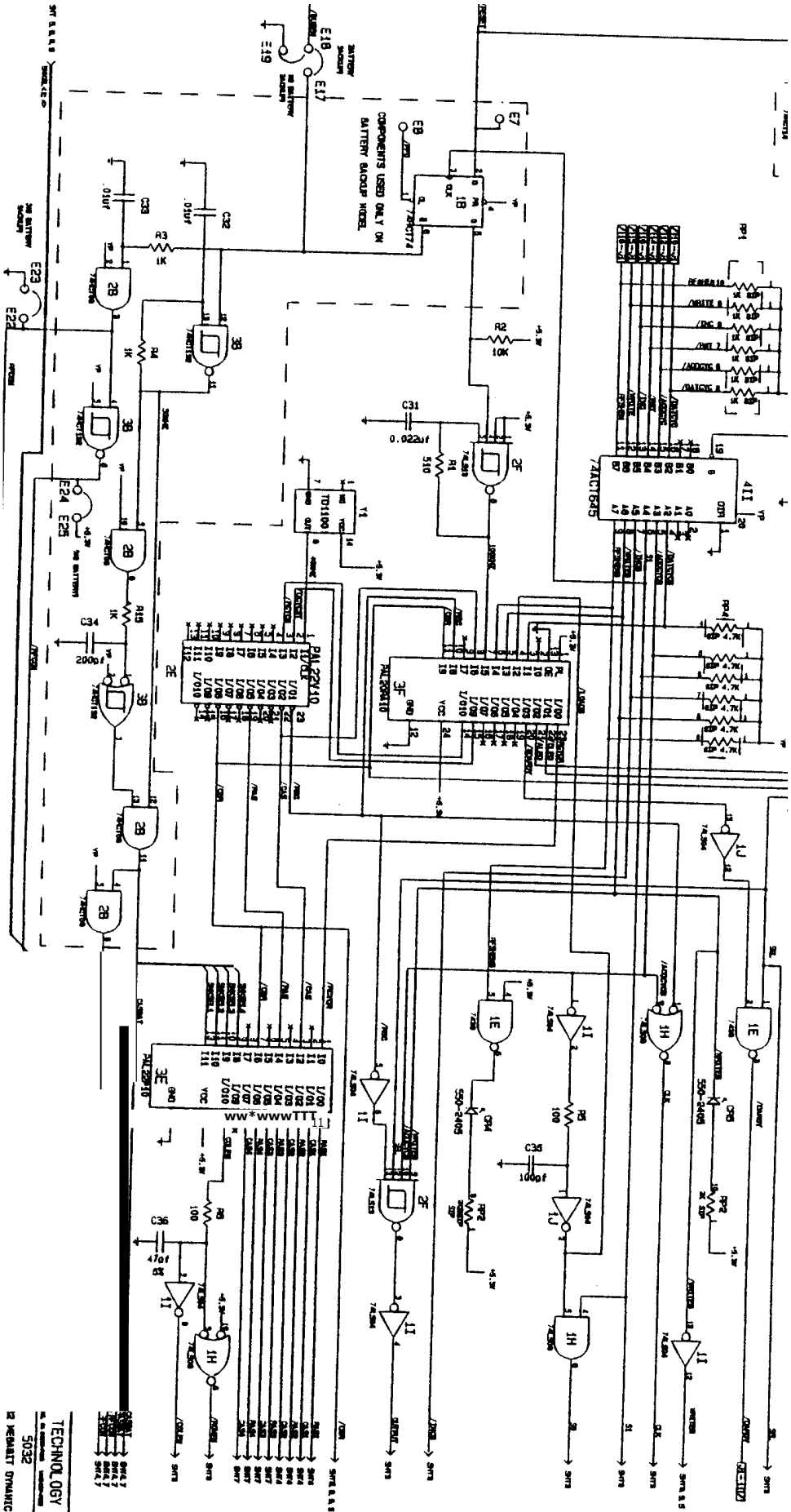
D S P TECHNOLOGY INC

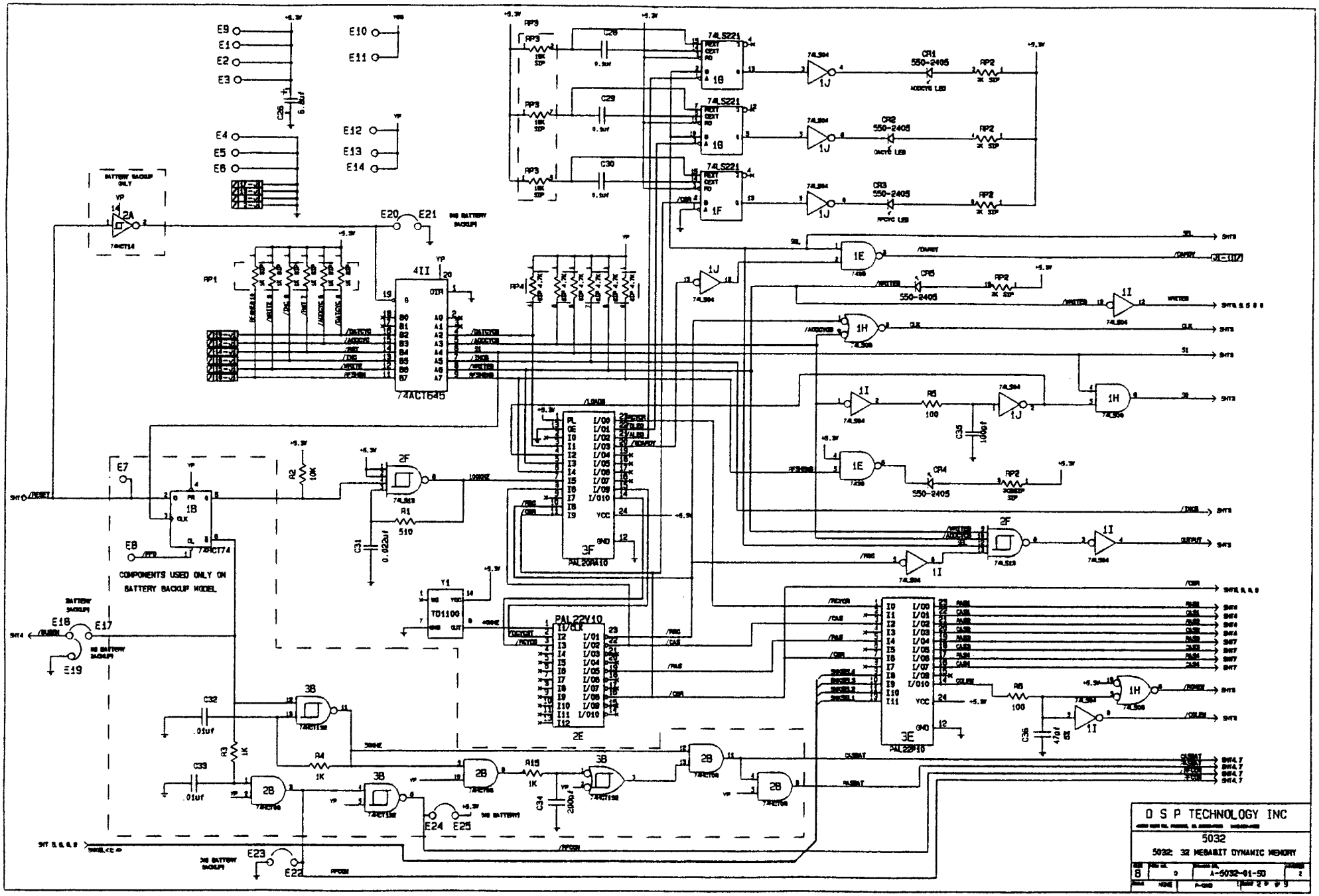
5032
32 MEGABIT DYNAMIC MEMORY
POWER SUPPLY/BATTERY BACKUP

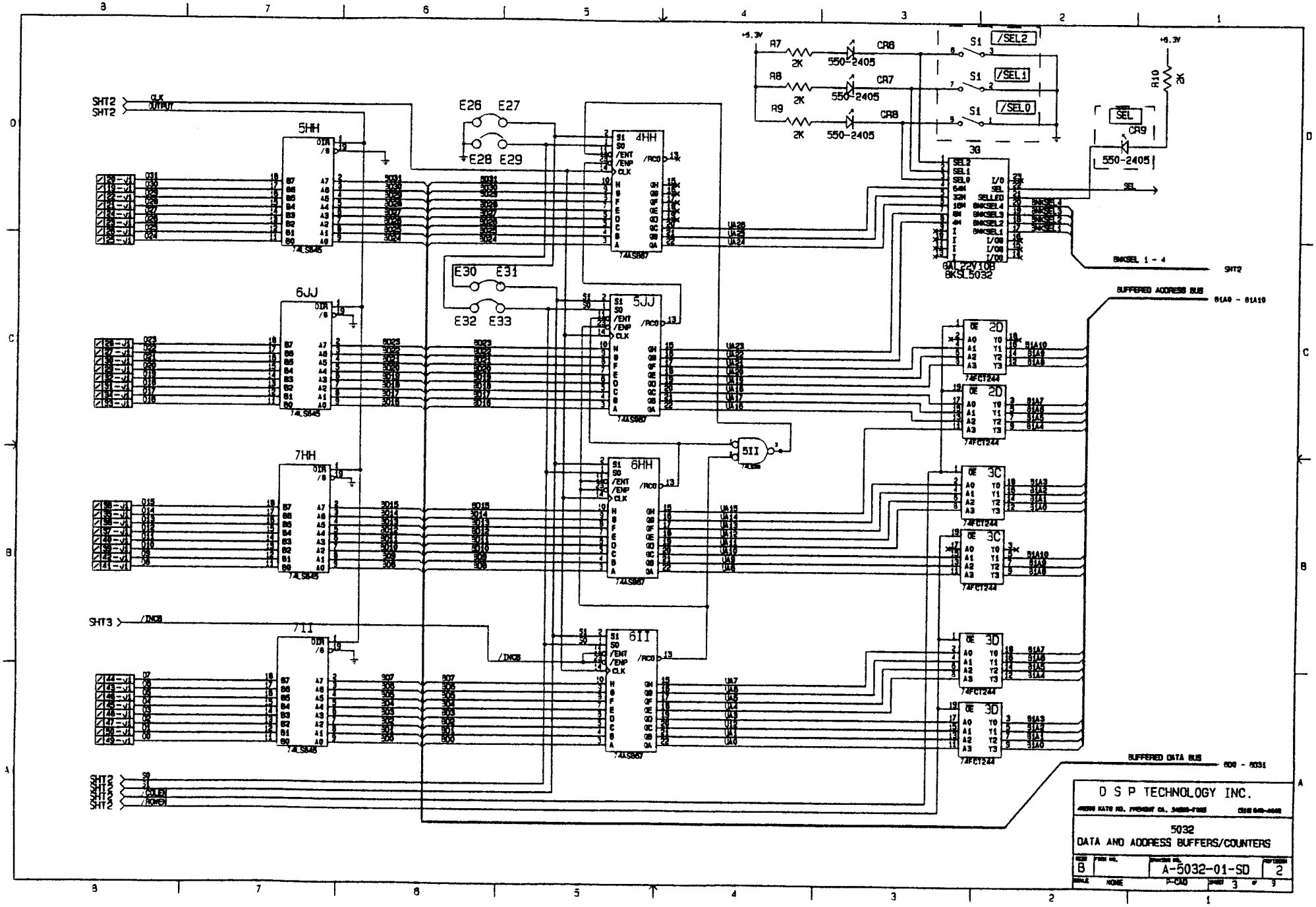
SIZE	DRAWING NO.	REV
B	5032-01-SD	2

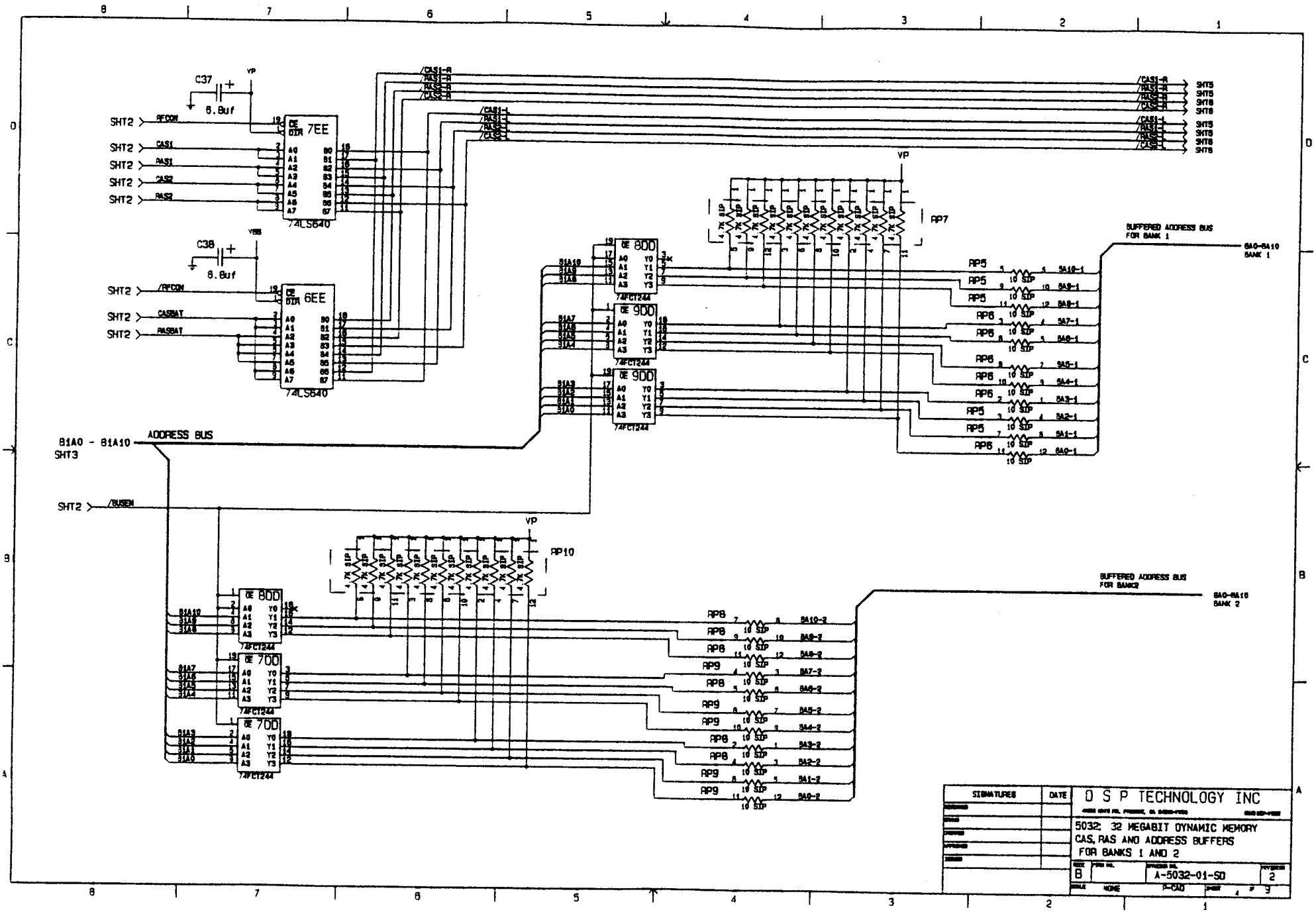
SCALE: NONE SHEET 1 OF 9

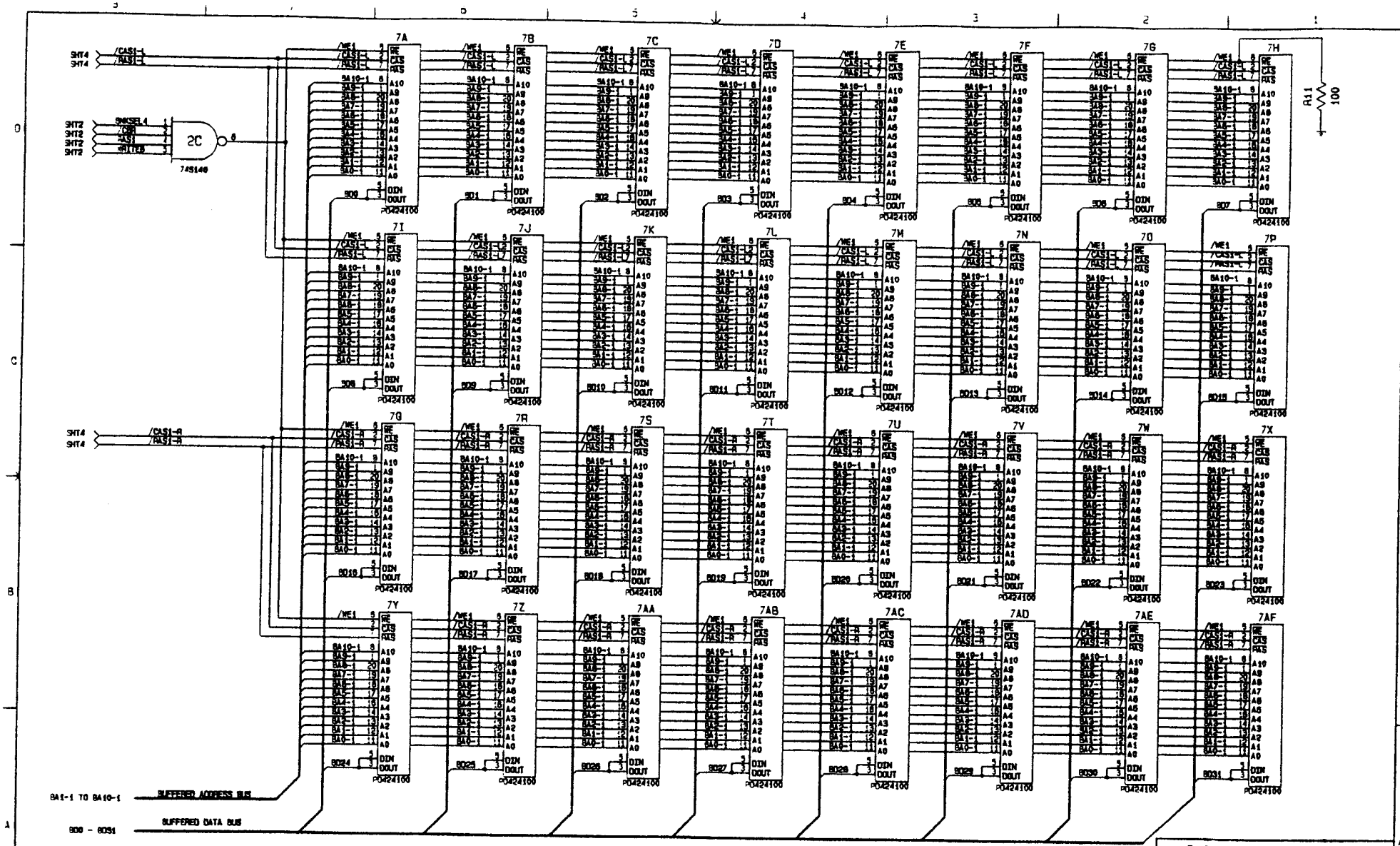
P-CAD

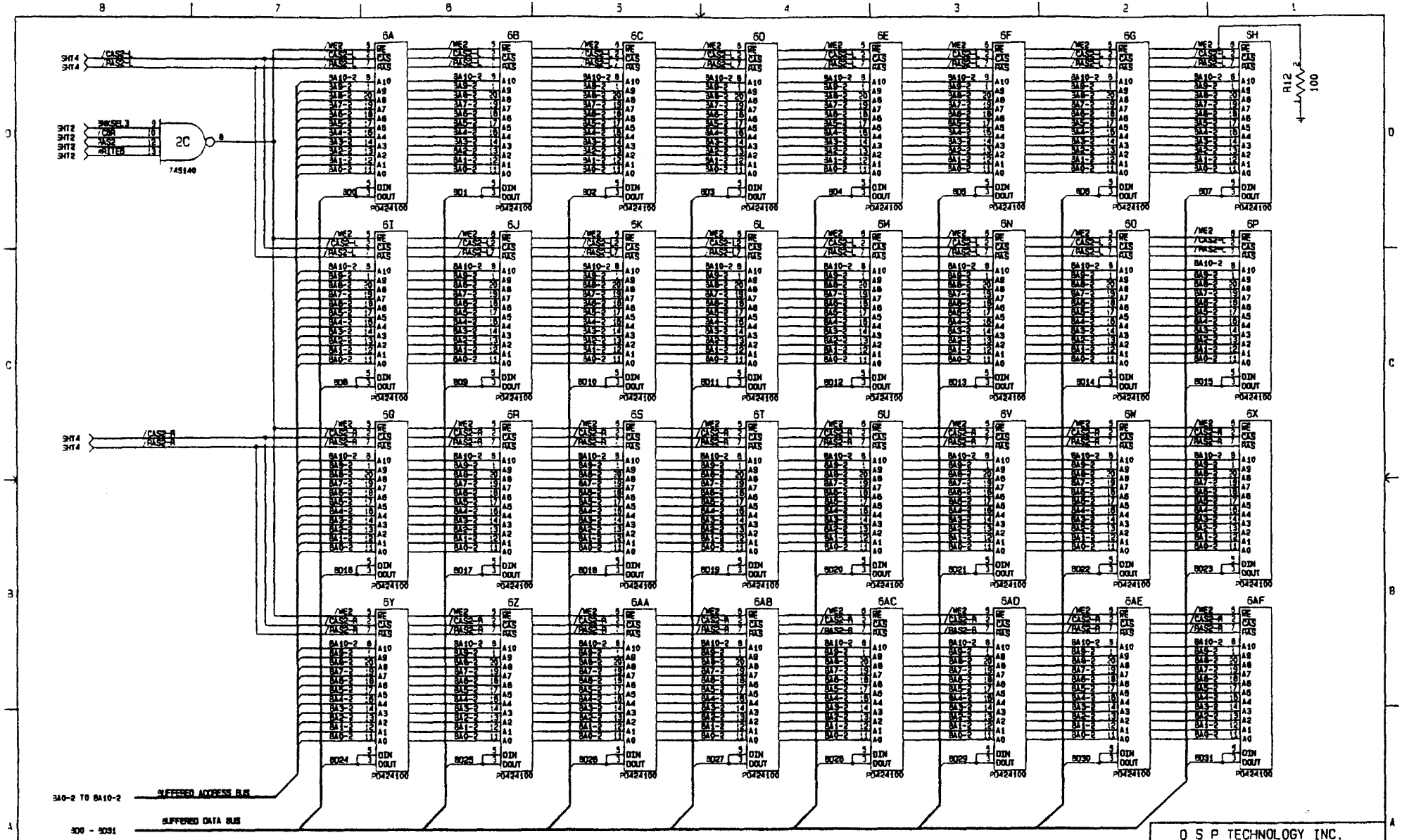

COMPONENTS USED ONLY ON BATTERY BACKUP MODEL
74ACT845
PAL22V10
PAL20R8
TECHNOLOGY INC
5032
32 MEGABIT DYNAMIC MEMORY


D S P TECHNOLOGY INC
5032
5032: 32 MEGABIT DYNAMIC MEMORY
A-5032-01-SD
74AC1645
PAL20RA10
PAL22V10
74ACT74
74ALS221
74ALS04
74ALS08
74ALS32
74ACT138
74ACT86
COMPONENTS USED ONLY ON BATTERY BACKUP MODEL


D S P TECHNOLOGY INC.
5032
DATA AND ADDRESS BUFFERS/COUNTERS
A-5032-01-SD
BUFFERED ADDRESS BUS
BUFFERED DATA BUS
/SEL2
/SEL1
/SEL0
SEL
BMCSEL 1 - 4
5HH
6JJ
7HH
7II
4HH
5JJ
6HH
6II
5II
3G
2D
3C
3D
74ALS645
74ALS867
74FCT244
GAL22V10B
8KSL5032


C37
6.8uf
VP
SHT2 /RFCON
SHT2 CAS1
SHT2 RAS1
SHT2 CAS2
SHT2 RAS2
OE DIR 7EE
74LS640
C38
6.8uf
VSS
SHT2 /RFCON
SHT2 CASBAT
SHT2 RASBAT
OE DIR 6EE
74LS640
/CAS1-R
/RAS1-R
/CAS2-R
/RAS2-R
/CAS1-L
/RAS1-L
/CAS2-L
/RAS2-L
SHT5
SHT6
B1A0 - B1A10
ADDRESS BUS
SHT3
SHT2 /BUSEN
OE 800
OE 900
OE 700
74FCT244
RP7
RP10
RP5
RP6
RP8
RP9
10 SIP
BUFFERED ADDRESS BUS FOR BANK 1
BA0-BA10 BANK 1
BUFFERED ADDRESS BUS FOR BANK2
BA0-BA10 BANK 2
SIGNATURES
DATE
D S P TECHNOLOGY INC
5032: 32 MEGABIT DYNAMIC MEMORY
CAS, RAS AND ADDRESS BUFFERS
FOR BANKS 1 AND 2
A-5032-01-SD
SIZE B
REV 2
SCALE NONE
SHEET 4 OF 9


SHT4 /CAS1-L
SHT4 /RAS1-L
SHT2
SHT2
SHT2
SHT2
2C
74S140
R11
100
7A
7B
7C
7D
7E
7F
7G
7H
7I
7J
7K
7L
7M
7N
7O
7P
7Q
7R
7S
7T
7U
7V
7W
7X
7Y
7Z
7AA
7AB
7AC
7AD
7AE
7AF
SHT4 /CAS1-R
SHT4 /RAS1-R
BA1-1 TO BA10-1
BUFFERED ADDRESS BUS
D00 - D031
BUFFERED DATA BUS
4M X 32 BIT MEMORY BANK
(ONE OF 4)
NOTE: ALL 424100S RUN OFF VP SUPPLY LINE
O S P TECHNOLOGY INC.
5032: 32 MEGABIT DYNAMIC MEMORY
4M X 32 BIT MEMORY: BANK 1
5032-01-SD
2
5 of 9



4M X 32 BIT MEMORY BANK

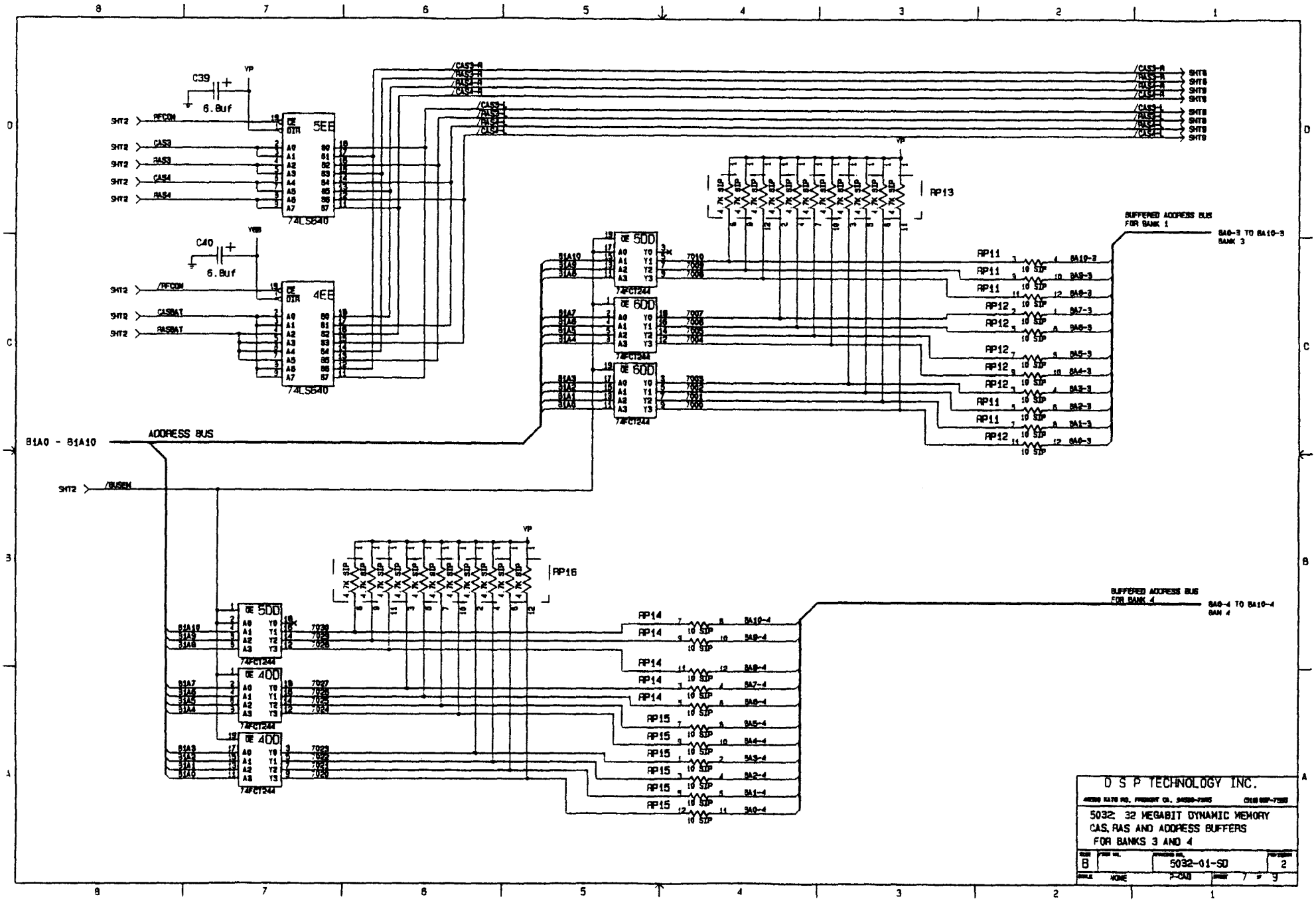
(TWO OF FOUR)

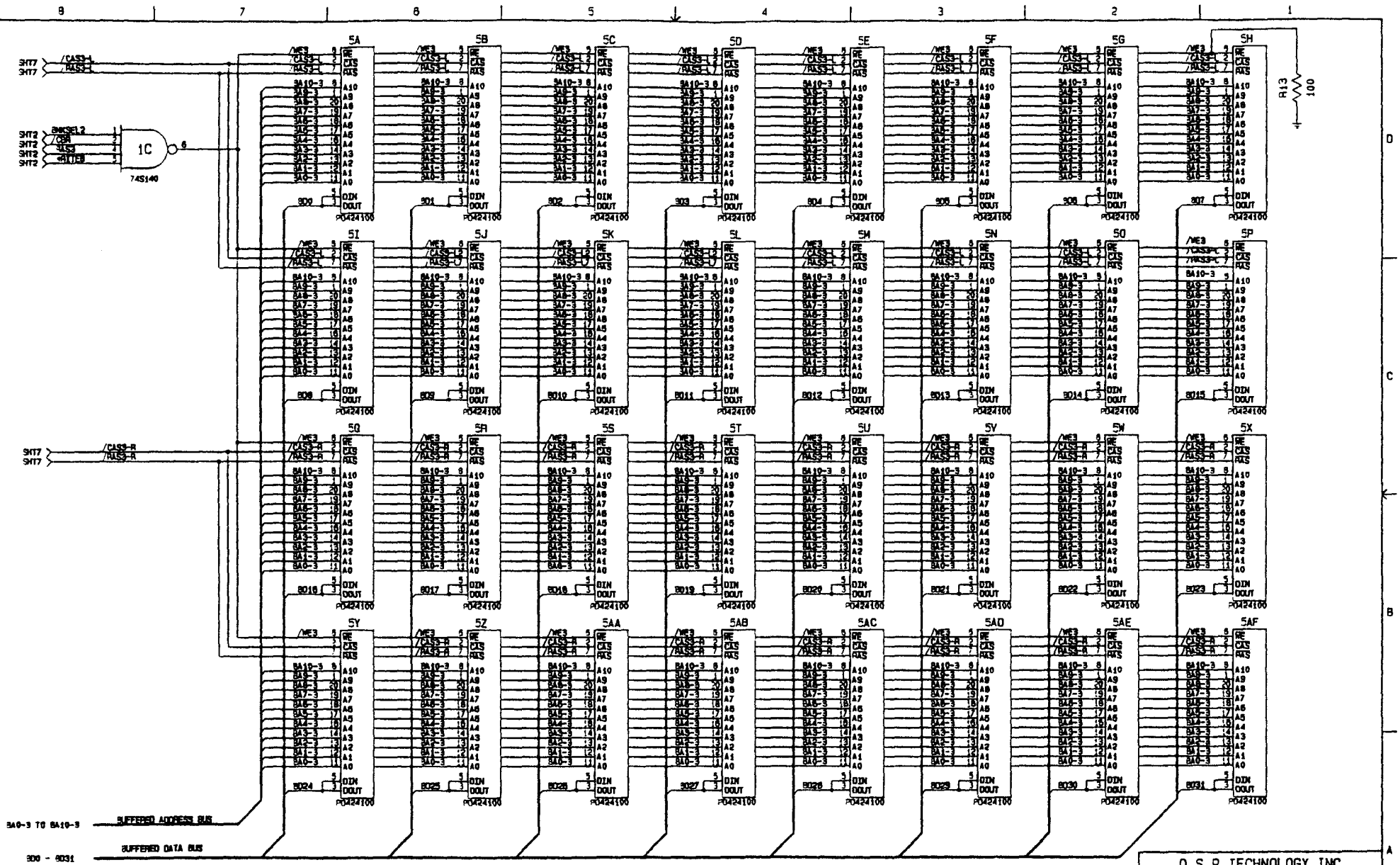
NOTE: ALL 424100S RUN OFF VP SUPPLY LINE

O S P TECHNOLOGY INC.

5032: 32 MEGABIT DYNAMIC MEMORY
4M X 32 BIT MEMORY: BANK 2

SIZE	FSCM NO.	DRAWING NO.	REVISION
B		5032-01-SD	2
SCALE: NONE		A-CAD	SHEET 5 OF 9


C39
6.8uf
VP
SHT2
/RFCON
/CAS3
/RAS3
/CAS4
/RAS4
5EE
74LS640
C40
6.8uf
VBB
/RFCON
/CASBAT
/RASBAT
4EE
74LS640
/CAS3-A
/RAS3-A
/CAS4-A
/CAS3-1
/RAS3-1
/CAS4-1
SHT8
SHT9
RP13
RP16
OE 500
OE 600
OE 400
74FCT244
B1A0 - B1A10
ADDRESS BUS
/BUSEN
BUFFERED ADDRESS BUS FOR BANK 1
BA0-3 TO BA10-3 BANK 3
BUFFERED ADDRESS BUS FOR BANK 4
BA0-4 TO BA10-4 BANK 4
RP11
RP12
RP14
RP15
10 SIP
D S P TECHNOLOGY INC.
5032: 32 MEGABIT DYNAMIC MEMORY
CAS, RAS AND ADDRESS BUFFERS
FOR BANKS 3 AND 4
5032-01-SD
2
NONE
P-CAD



4M X 32 BIT MEMORY BANK

(3 OF 4)

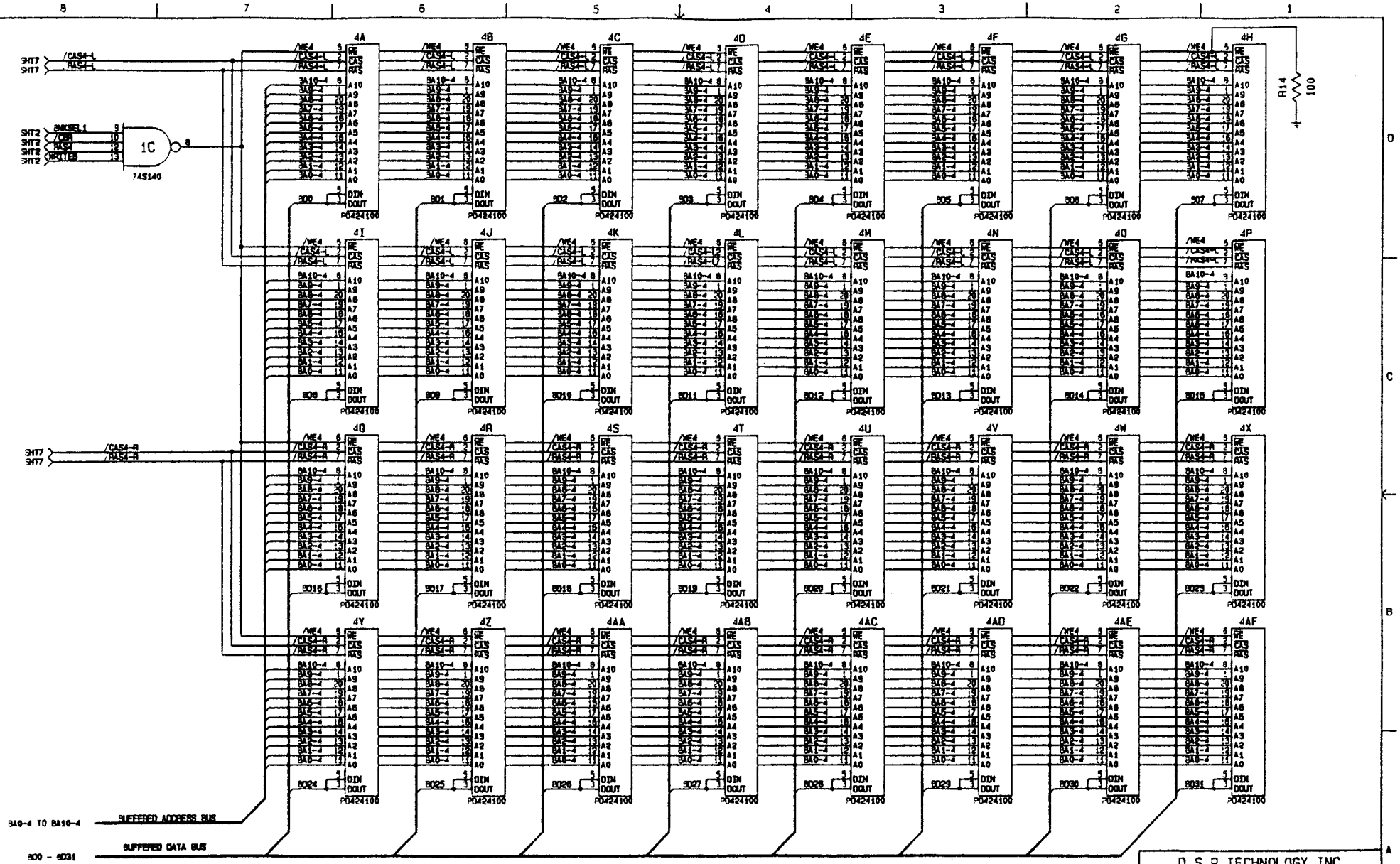
NOTE: ALL 424100S RUN OFF VP SUPPLY LINE

O S P TECHNOLOGY INC.

5032: 32 MEGABIT DYNAMIC MEMORY
4M X 32 BIT MEMORY: BANK 3

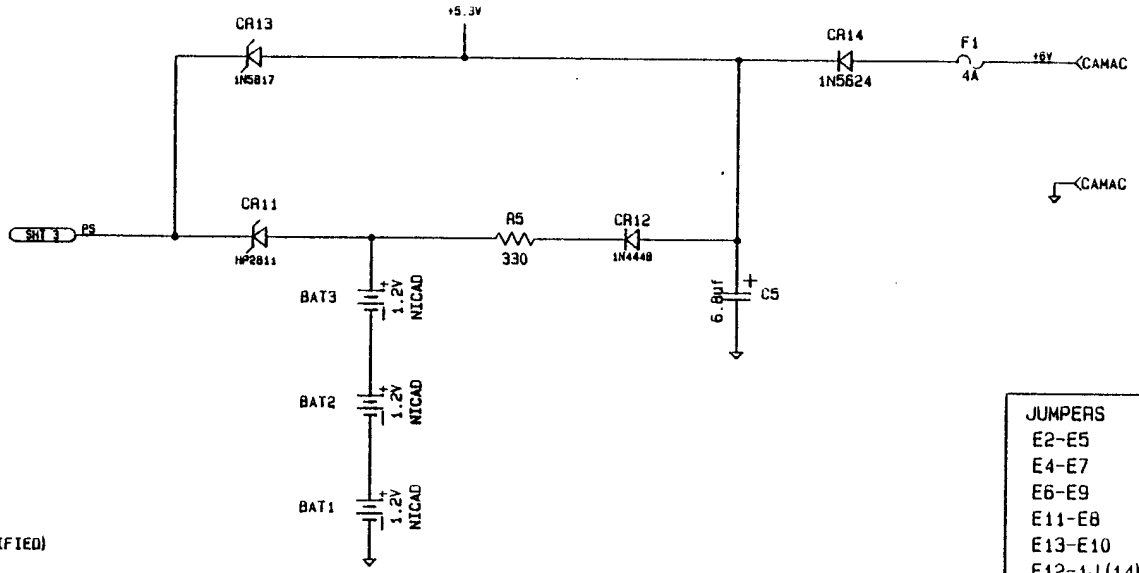
SIZE	DWG NO.	REV
B	5032-01-SD	2

SCALE NONE — CAD — SHEET 8 OF 9


4M X 32 BIT MEMORY BANK
(4 OF 4)
NOTE: ALL 424100S RUN OFF VP SUPPLY LINE
BA0-4 TO BA10-4
BUFFERED ADDRESS BUS
D00 - D031
BUFFERED DATA BUS
74S140
R14
100
O S P TECHNOLOGY INC.
5032: 32 MEGABIT DYNAMIC MEMORY
4M X 32 BIT MEMORY: BANK 4
A-5032-01-SD
A-CAD

SYMBOLS.

- CAMAC EDGE CONNECTOR
- EXTERNAL CONNECTOR
- —( ) CONTINUE ON SAME SHEET
- CONTINUE ON DIFFERENT SHEET
- UNUSED PIN
- JUMPERS



JUMPERS
E2-E5
E4-E7
E6-E9
E11-E8
E13-E10
E12-1J(14)
E14-1J(13)

NOTES. (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE IN OHMS.

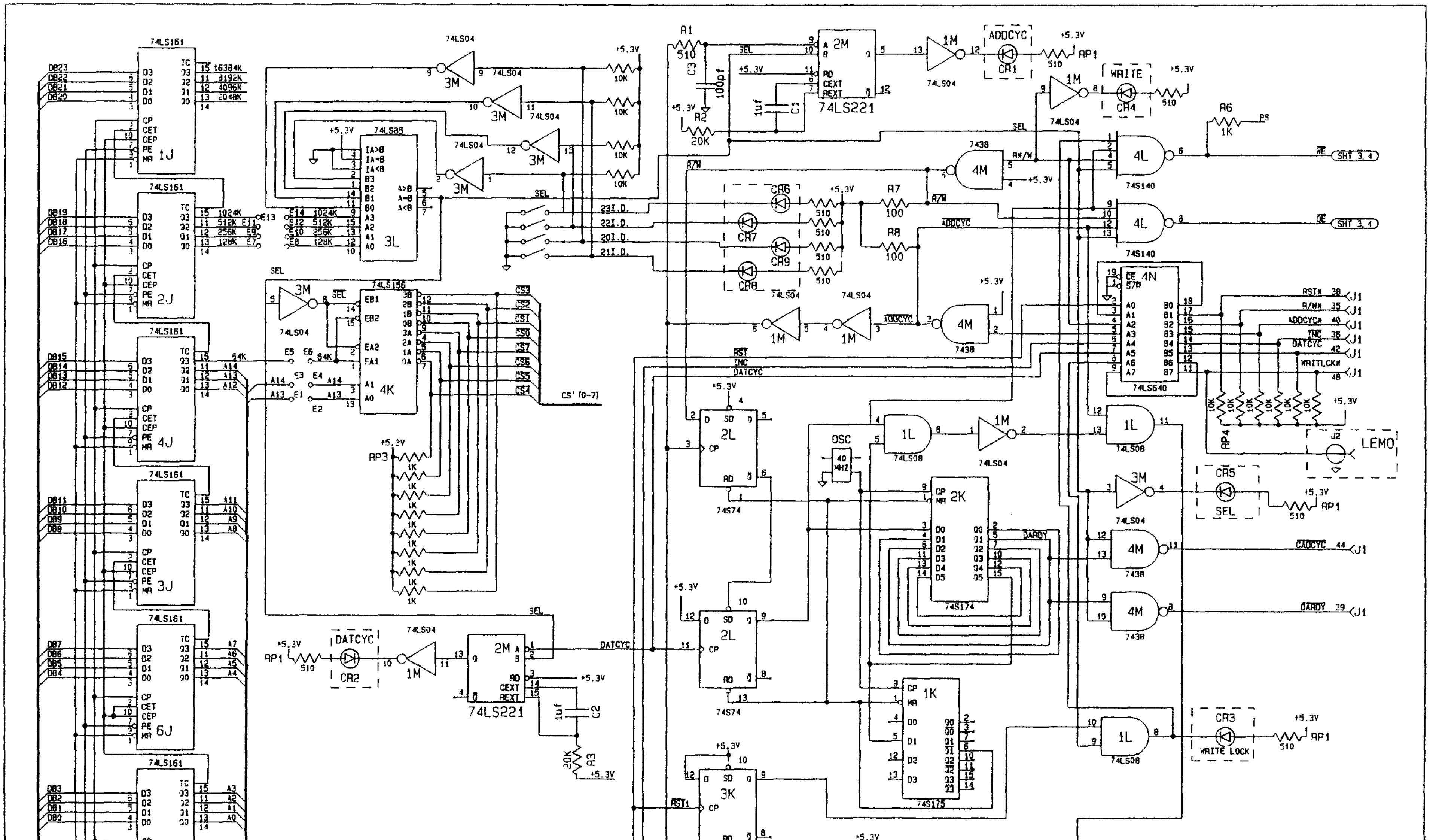
REVISIONS			
REV	PROD RELEASE DESCRIPTION	DATE	

SIGNATURES		DATE
DESIGNED		
DRAWN	N. PERALTA	
CHECKED		
APPROVED		
ISSUED		

D S P TECHNOLOGY INC

SCHEMATIC, 5204: 512K MEMORY POWER SUPPLY

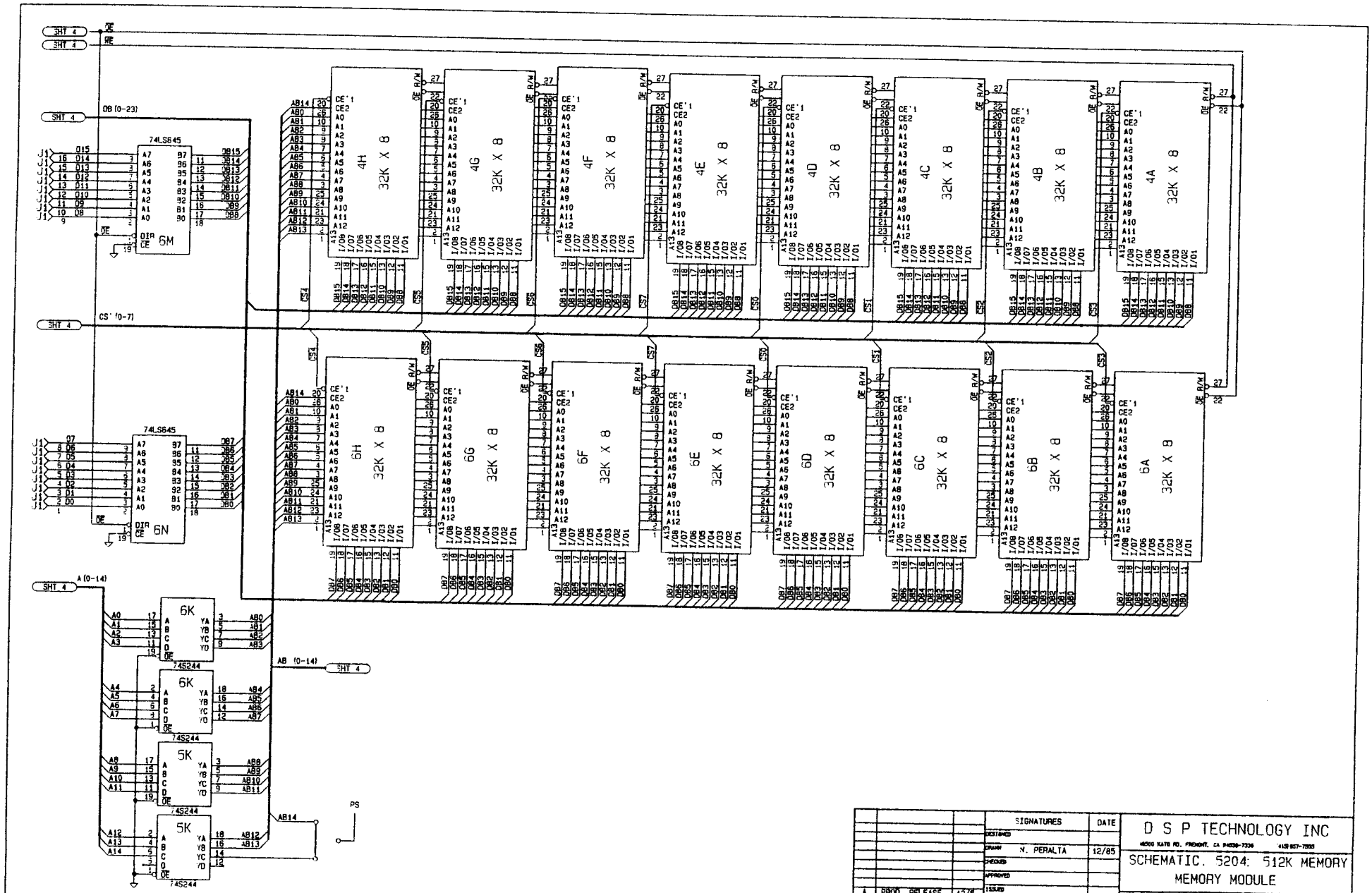
SIZE	FSCM NO.	DRAWING NO.	REVISION
D1		1-5204-01 SD	A
SCALE NONE		SHEET 1 OF 4	

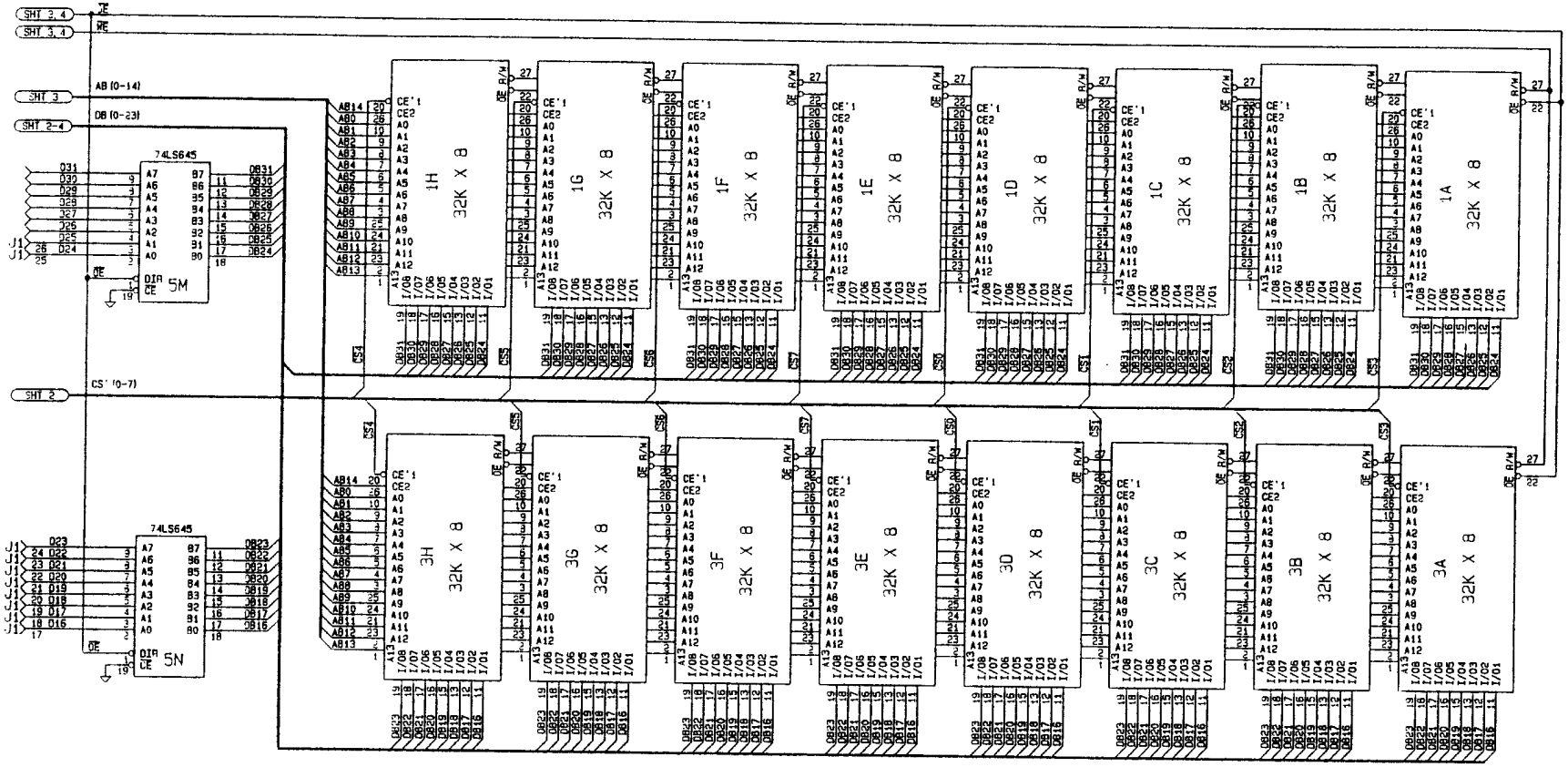


D S P TECHNOLOGY INC

SCHEMATIC, 5202: 512K MEMORY
TTL LOGIC

SIZE C | DRAWING NO. A-5204-01 SD | REVISION A
SCALE NONE | SHEET 2 OF 4


SHT 4
OE
WE
DB (0-23)
CS* (0-7)
A (0-14)
AB (0-14)
PS
74LS645
6M
6N
4H
4G
4F
4E
4D
4C
4B
4A
6H
6G
6F
6E
6D
6C
6B
6A
32K X 8
6K
5K
74S244
SIGNATURES
DESIGNED
DRAWN N. PERALTA 12/85
CHECKED
APPROVED
ISSUED
REVISIONS
A PROD. RELEASE 12/4
REV DESCRIPTION DATE
D S P TECHNOLOGY INC
SCHEMATIC. 5204: 512K MEMORY
MEMORY MODULE
SIZE C
DRAWING NO. A-5204-01 SD
REVISION A
SCALE NONE
SHEET 3 OF 4



REVISIONS		
REV	DESCRIPTION	DATE
A	PROD. RELEASE	12/5

SIGNATURES		DATE
DESIGNED		
DRAWN	N. PERALTA	12/85
CHECKED		
APPROVED		
ISSUED		

D S P TECHNOLOGY INC

SCHEMATIC. 5204: 512K MEMORY

MEMORY MODULE

SIZE	FSCM NO.	DRAWING NO.	REVISION
C	04	A-5204-01 SD	A

SCALE NONE SHEET 4 OF 4

INDEX