EK-VS200-PS-PRE

VAXstation I Service Guide

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PREFACE

INTRODUCTION TO THE GUIDE

This guide contains system configuration and maintenance information and procedures. All the information in this guide has been abstracted from the VAXstation I Technical Manual, EK-VS200-TM. For more detailed descriptions and explanations, refer to that manual.

CHAPTER:

1 **SYSTEM CONFIGURATION** -- Brifely describes switches, jumpers, and backplane configuration. For more information see Chapter 2 in the VAXstation I Technical Manual, EK-VS200-TM.

2 **PROGRAMMING INFORMATION** -- This chapter describes the 32 I/O page locations that are used for the exchange of control and status information between the CPU nad the VCB01. For more information see Chapter 4 in the VAXstation I Technical Manual, EK-VS200-TM.

3 **MAINTENANCE** -- Describes diagnostic procedures. For more information see Chapter 5 in the VAXstation I Technical Manual, EK-VS200-TM.

4 **REPLACEMENT** -- Gives step-by-step procedures for removing and replacing system components. This chapter is nearly identical to Chapter 6 in the VAXstation I Technical Manual, EK-VS200-TM.

RELATED DOCUMENTS

VAXstation I Owner's Manual	EK-VS200-OM
VAXstation I Technical Manual	EK-VS200-TM
MicroVAX I CPU Technical Description	EK-KD32A-TD
MicroVAX I Owner's Manual	EK-KD32A-OM
MicroVAX Handbook	EB-25156-47
RQDX1 Controller User's Guide	EK-RQDX1-UG
RX50-D-4 Dual Flexible Disk Drive Manual	EK-LEP01-OM
RD52 Fixed Disk Drive	[TBS]
DEQNA User's Guide	EK-DEQNA-UG
DZV11 Asynchronous Multiplexer Technical Manual	EK-DZV11-TM
MSV11-QA Memory [TBS]	[TBS]
Microcomputer Interfaces Handbook	EB-20175-20
Print Set	MP-02005-01

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CONVENTIONS

The following table defines the conventions used throughout this guide.

CONVENTION	MEANING
<mm:nn>	Read as "mm through nn"; indicates a bit field or a set of lines or signals. For example, A<17:00> is the mnemonic for Unibus Address Lines A17 through A00.
DS> RUN EHXVS<RETURN>	Terminal dialogue. Prompts and system typeouts are shown in normal type. User responses are shown in boldface type. <RETURN> is described below.
<RETURN>	The boldface symbol of a label enclosed by angle brackets represents a key (usually a control or special character key) on the keyboard (in this case, the RETURN key). (Draft document only. The convention is different for final documentation -- see DEC STD 165.)
abbreviations	Abbreviations used in this manual are in accordance with DEC STD 015, 3 February 1983.

NOTE -- contains general information.
CAUTION -- contains information to prevent damage to equipment.
WARNING -- contains information to prevent personal injury.

CHAPTER 1

SYSTEM CONFIGURATION

This chapter brifely describes switches, jumpers, and backplane configuration. For more information see Chapter 2 in the VAXstation I Technical Manual, EK-VS200-TM.

1.1 BACKPLANE

Figure 1-1 shows an example backplane installation for a system configured with all the option modules listed in Table 1-1. Figure 1-2 shows grant continuity chaining and interrupt acknowledge priority. With regard to the backplane, the following should be observed:

- The M7136 MCT (memory controller) module is installed in slot 1.
- The M7135-YA DAP (data path) module is installed in slot 2.
- Memory modules are installed adjacent to the M7135-YA; that is, starting with slot 3.
- It is recommended that the DEQNA be installed ahead of (that is, in the lower-numbered slot) the VCB01.
- The DEQNA is a dual-height module and requires a G7272 Grant Continuity card in the A or C position of the same slot. As Figure 1-1 shows, the DEQNA occupies the A/B position and the G7272 occupies the C position. (Figure 1-2, below, shows the Grant path).
- The RQDX1 Disk Controller is installed in the last active slot in the backplane. For example, in a base

system with no options, the VCB01 would occupy slot 4 and the RQDX1 would occupy slot 5.

Table 1-1: System Components and Options

BASE SYSTEM	
KD32-AB	MicroVAX I CPU (includes):
	M7135-YA DAP (Data Path) Module
	M7136 MCT (Memory Controller) Module
MSV11-QA	1 MB Memory Module
RQDX1	Disk Controller
RD52	28 MB Fixed-disk Drive
RX50	400 kB Diskette Drive
VCB01	Video Graphics Controller Module
VR100	48 cm (19 in) Video Monitor
LK201-CA	Keyboard
VS10X	Mouse
OPTIONS	
MSV11-QA	1 MB Memory Module
DEQNA	Ethernet Controller
DZV11	4-line Asynchronous Multiplexer
LA50 or	Printer
LA100	Printer
[TBD]	Graphics Tablet
[TBS]	Tilt/swivel Base for Monitor

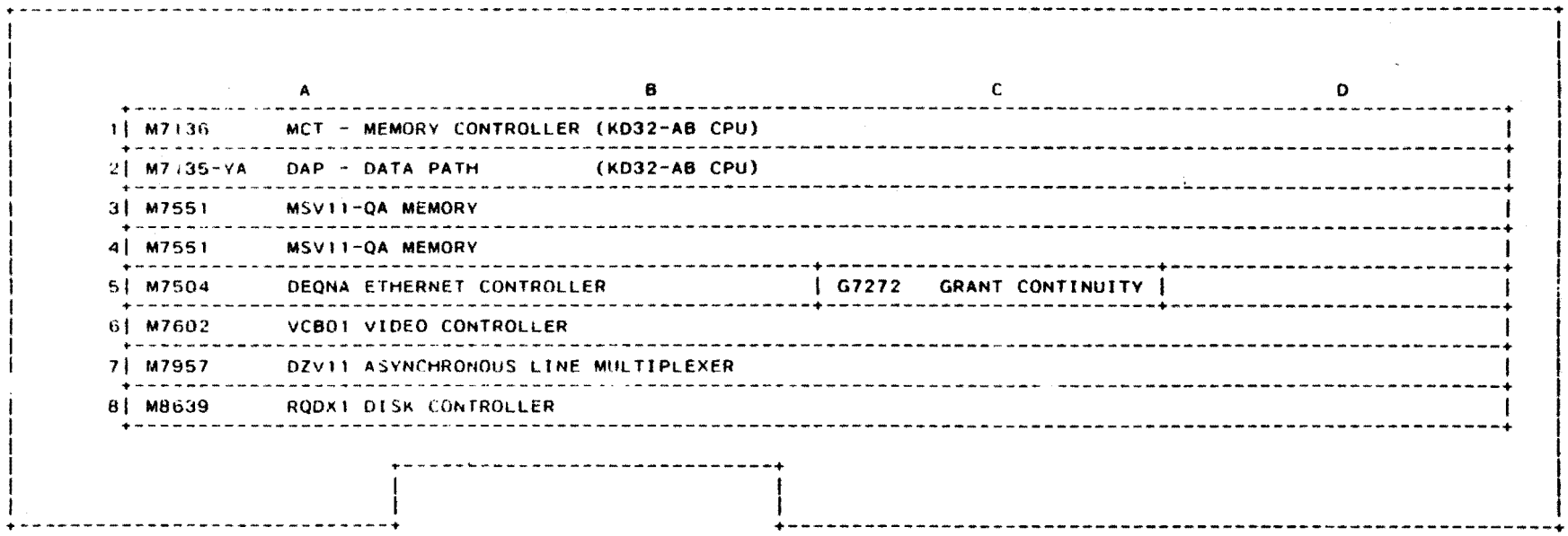


Figure 1-1: Backplane Configuration Example

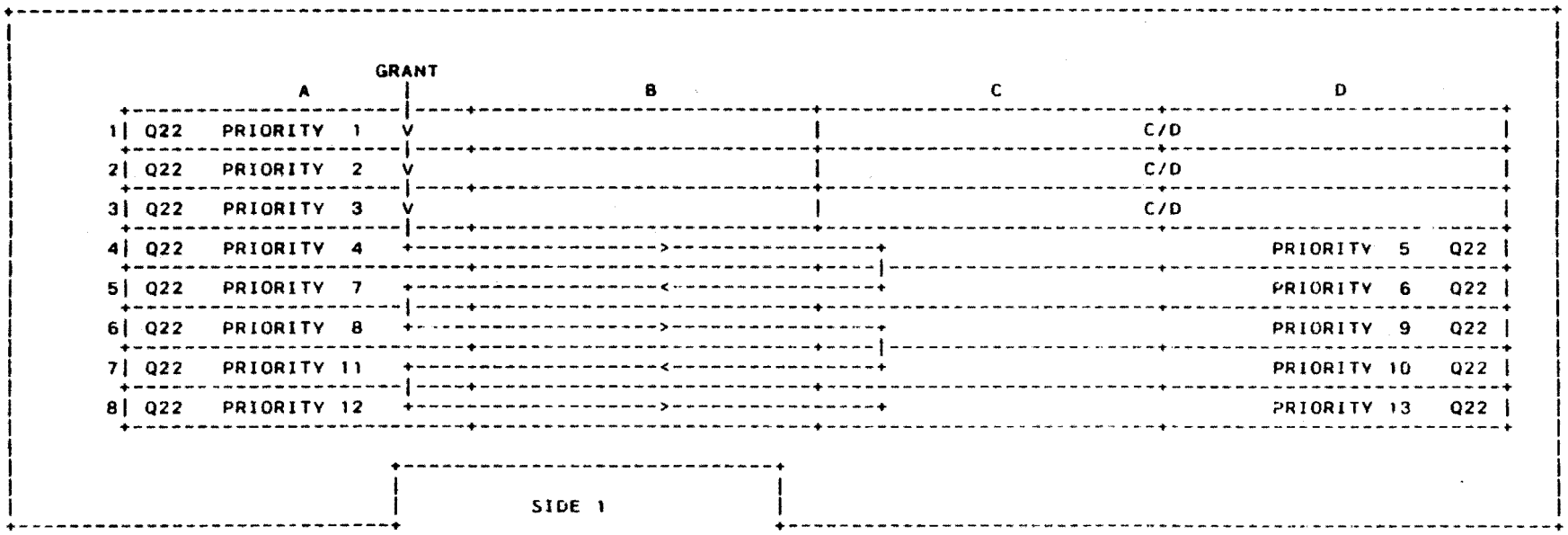


Figure 1-2: H9278-A Backplane

1.2 KD32-AB CPU

The KD32-AB CPU comprises two quad-height modules: the M7135-YA DAP (data path) module, and the M7136 MCT (memory controller) module. For more information on the KD32-AB, see the MicroVAX I CPU Technical Description, EK-KD32A-TD.

1.2.1 M7135-YA DAP

The DAP module (Part Number M7135-YA) is connected to the MCT with a ribbon cable.

1.2.1.1 Switches - As Figure 1-3 shows, the DAP contains two sets of eight DIP switches and a single jumper. The SID register switches are used by manufacturing and should not be changed. Table 1-2 lists the Option switch functions and the normal setting for the VAXstation 1.

The three LEDs display a binary error code that matches the error code displayed in the segmented-LED display on the CPU insert mounted in the Patch and Filter Panel assembly.

1.2.1.2 Microverify Jumper - This jumper determines the test mode for Microverify. The jumper is factory-set to **single-pass** mode (as shown in Figure 1-3). In the alternate jumper positon, **multiple-loop** mode, DAP Option Switch 2 (Table 1-2) **must** be in the OFF (VT100 compatible) position (also see the NOTE -- VT100 Mode, below).

NOTE - VT100 Mode

> If DAP Option switch 2 is set to the OFF position, a VT100 can be connected to the terminal SLU and used as the console terminal.

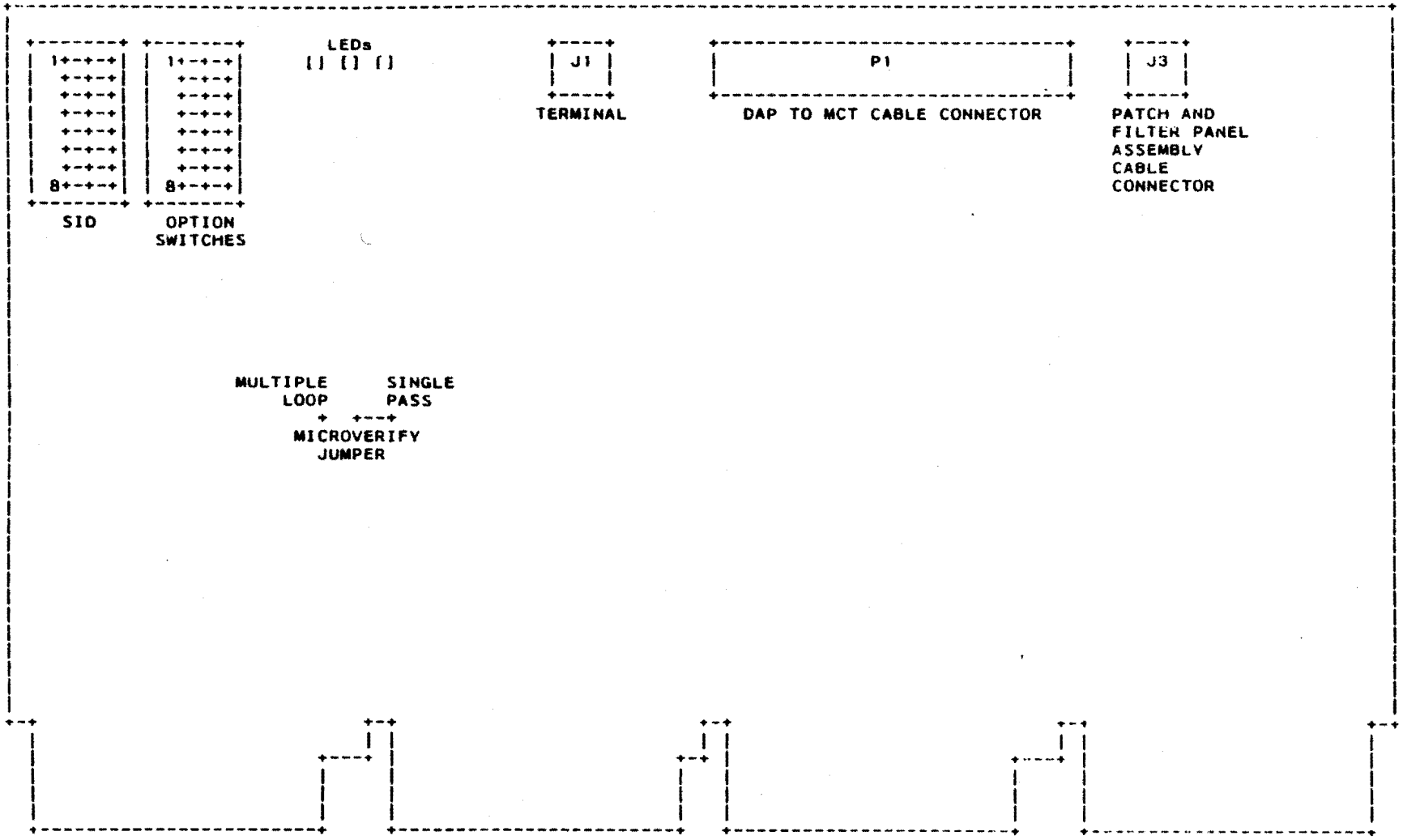


Figure 1-3: M7135-YA DAP Switches and Jumper

Table 1-2: DAP Option Switches

SWITCH	NORMAL SETTING	FUNCTION
8 7	OFF OFF	BAUD RATE SELECT -- specify the data transfer baud rate between the CPU and console terminal. 8 / 7 OFF / OFF = 9600 OFF / ON = 19200 ON / OFF = 300 ON / ON = 1200
6	OFF	(reserved)
5	OFF	BREAK DETECT ENABLE -- determines whether a break condition on the SLU causes a halt: OFF = <BREAK> key disabled ON = <BREAK> key enabled
4 3	OFF OFF	RECOVERY ACTION -- determine attempted CPU functions during Power-on: 4 / 3 OFF / OFF = warm start or boot or halt OFF / ON = boot or halt ON / OFF = warm start or halt ON / ON = halt
2	ON	CONSOLE TERMINAL TYPE -- identifies the type of console terminal connected to the system: OFF = VT100 compatible (see NOTE -- VT100 Mode, above) ON = Graphics terminal
1	OFF	BOOTSTRAP SEARCH ORDER -- determines which devices are searched when the system is bootstrapped: OFF = All devices searched ON = Disk/diskette drives not searched

1.2.2 M7136 MCT Module

The MCT module (Part Number M7136) contains no user-configurable components, and is connected to the DAP with a ribbon cable.

1.3 MSV11-QA MEMORY

The MSV11-QA Memory switches and jumpers are described in Figure 1-4 and Tables 1-3, 1-4 and 1-5.

1.3.1 Switches

As Figure 1-4 shows, the MSV11 has two sets of six DIP switches. These are the memory's starting and ending address switches, and select the address on 128 kB boundaries (Table 1-3).

VAXstation I configuration guidelines are:

- For all switches: 1 = OFF and 0 = ON.
- SW1 positon 6 is not used.
- If the MSV11-QA is the only memory or the first memory installed (in other words, the memory installed in backplane slot 3):
  - the STARTING ADDRESS must be 00000.
  - the ENDING ADDRESS must be 1024 kB.
- If the MSV11-QA is the second memory:
  - the STARTING ADDRESS must be 1024 kB (the same as the first memory's ending address).
  - the ENDING ADDRESS must be 2048 kB.

  The VAXstation I supports only one or two MSV11-QA memories, and they must be configured as stated above and shown in the following examples. Any other configuration is invalid and not supported.

	STARTING ADDRESS						ENDING ADDRESS				
	SW1						SW2				
	5	4	3	2	1	6	5	4	3	2	1
ONE MSV11-QA	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	ON	ON
	00000						1024 kB				

Example 1-1: One MSV11-QA Starting Address Selection

	STARTING ADDRESS						ENDING ADDRESS				
	SW1						SW2				
	5	4	3	2	1	6	5	4	3	2	1
FIRST MSV11-QA	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	ON	ON
	00000						1024 kB				
SECOND MSV11-QA	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	ON	ON
	1024 kB						2048 kB				

Example 1-2: Two MSV11-QA Starting Address Selection

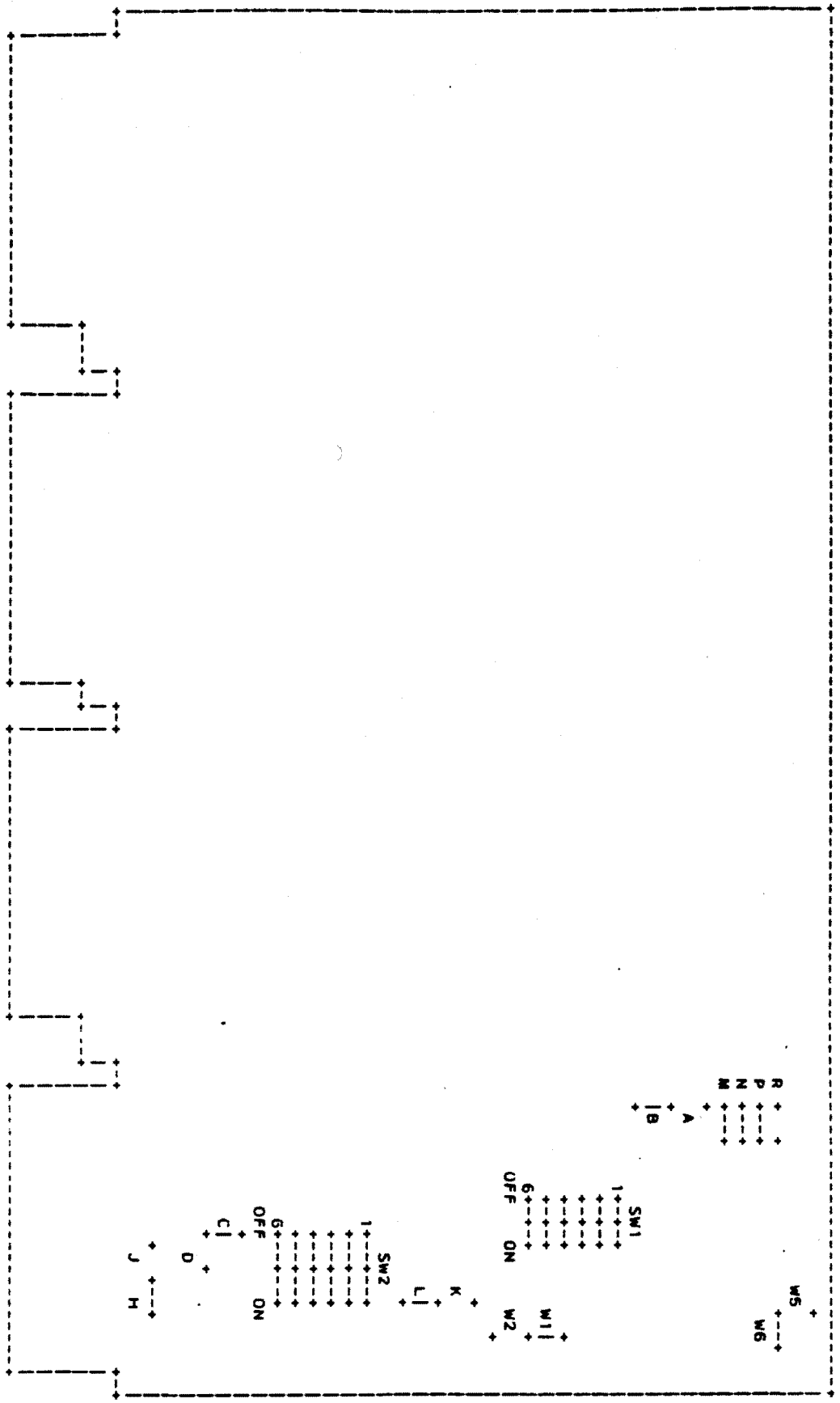


Figure 1-4: MSV11-QA Jumpers and Switches

Table 1-3: MSV11-QA Switches

	BDAL:	21	20	19	18	17		21	20	19	18	17
		STARTING ADDRESS						ENDING ADDRESS				
		SW1 POSITION						SW2 POSITION				
	(kB)	5	4	3	2	1	6	5	4	3	2	1
	4096							0	0	0	0	0
	3968	0	0	0	0	1	1	0	0	0	0	1
	3840	0	0	0	1	0	1	0	0	0	1	0
	3712	0	0	0	1	1	1	0	0	0	1	1
	3584	0	0	1	0	0	1	0	0	1	0	0
	3456	0	0	1	0	1	1	0	0	1	0	1
	3328	0	1	1	1	0	1	0	0	1	1	0
	3200	0	0	1	1	1	1	0	0	1	1	1
	3072	0	1	0	0	0	1	0	1	0	0	0
	2944	0	1	0	0	1	1	0	1	0	0	1
	2816	0	1	0	1	0	1	0	1	0	1	0
	2688	0	1	0	1	1	1	0	1	0	1	1
	2560	0	1	1	0	0	1	0	1	1	0	0
	2432	0	1	1	0	1	1	0	1	1	0	1
	2304	0	1	1	1	0	1	0	1	1	1	0
	2176	0	1	1	1	1	1	1	1	1	1	1
*	2048	1	0	0	0	0	1	1	0	0	0	0
	1920	1	0	0	0	1	1	1	0	0	0	1
	1792	1	0	0	1	0	1	1	0	0	1	0
	1664	1	0	0	1	1	1	1	0	0	1	1
	1536	1	0	1	0	0	1	1	0	1	0	0
	1308	1	0	1	0	1	1	1	0	1	0	1
	1280	1	0	1	1	0	1	1	0	1	1	0
	1152	1	0	1	1	1	1	1	0	1	1	1
*	1024	1	1	0	0	0	1	1	1	0	0	0
	896	1	1	0	0	1	1	1	1	0	0	1
	768	1	1	0	1	0	1	1	1	0	1	0
	640	1	1	0	1	1	1	1	1	0	1	1
	512	1	1	1	0	0	1	1	1	1	0	0
	384	1	1	1	0	1	1	1	1	1	0	1
	256	1	1	1	1	0	1	1	1	1	1	0
	128	1	1	1	1	1	1	1	1	1	1	1
*	0	0	0	0	0	0	0					

* VAXstation I addresses

0 = ON 1 = OFF

1.3.2 Jumpers

As Figure 1-4 shows, the MSV11-QA has 6 sets of jumpers. The CSR Address jumpers (Table 1-4) are a set of 4 jumpers. In the VAXstation I, the first (or only) MSV11-QA CSR address is set to 17772100, and the second MSV11-QA CSR address is set to 17772102. Because the VAXstation I supports only one or two MSV11-QAs, the jumpers should not be set to any other positions.

Table 1-4: MSV11-QA CSR Address Jumpers

	BDAL:	21	05	04	03	02	01	00
		1111111111010001	0	x	x	x	x	0
	OCTAL:	1 7 7 7 2 1		X			X	
		ADDRESS		JUMPER M	JUMPER N	JUMPER P	JUMPER R	
*	FIRST	17772100		IN	IN	IN	IN	
*	SECOND	17772102		IN	IN	IN	OUT	
		17772104		IN	IN	OUT	IN	
		17772106		IN	IN	OUT	OUT	
		17772110		IN	OUT	IN	IN	
		17772112		IN	OUT	IN	OUT	
		17772114		IN	OUT	OUT	IN	
		17772116		IN	OUT	OUT	OUT	
		17772120		OUT	IN	IN	IN	
		17772122		OUT	IN	IN	OUT	
		17772124		OUT	IN	OUT	IN	
		17772126		OUT	IN	OUT	OUT	
		17772130		OUT	OUT	IN	IN	
		17772132		OUT	OUT	IN	OUT	
		17772134		OUT	OUT	OUT	IN	
		17772136		OUT	OUT	OUT	OUT	

* VAXstation I MSV11-QA CSR addresses

The remaining sets (Table 1-5) consist of 5 pairs of jumpers, each pair having a common pin. The VAXstation 1 settings are indicated with an asterisk (*).

Table 1-5: MSV11-QA Jumper Pairs

FUNCTION	SELECTION	JUMPER	STATUS	
MEMORY TYPE	**CSR PARITY**	**A**	**OUT**	*
		B	IN	
	NON-PARITY	A	IN	
		B	OUT	
PARITY ERROR ENABLE	**ENABLE**	**H**	**IN**	*
		J	OUT	
	DISABLE	H	OUT	
		J	IN	
CSR MEMORY TYPE	**22 bit CSR**	**K**	**OUT**	*
		L	IN	
	18 bit CSR	K	IN	
		L	OUT	
I/O PAGE SIZE	**4 k WORD**	**C**	**IN**	*
		D	OUT	
	2 k WORD	C	OUT	
		D	IN	
BLOCK MODE	**ENABLE**	**W1**	**IN**	*
		W2	OUT	
	DISABLE	W1	OUT	
		W2	IN	
WRITE WRONG PARITY	**FROM CSR**	**W5**	**OUT**	*
		W6	IN	
	FROM BDAL<16>	W5	IN	
		W6	OUT	

* VAXstation I position

For more information on the MSV11-QA memory, see the MSV11-QA [TBS], [TBS].

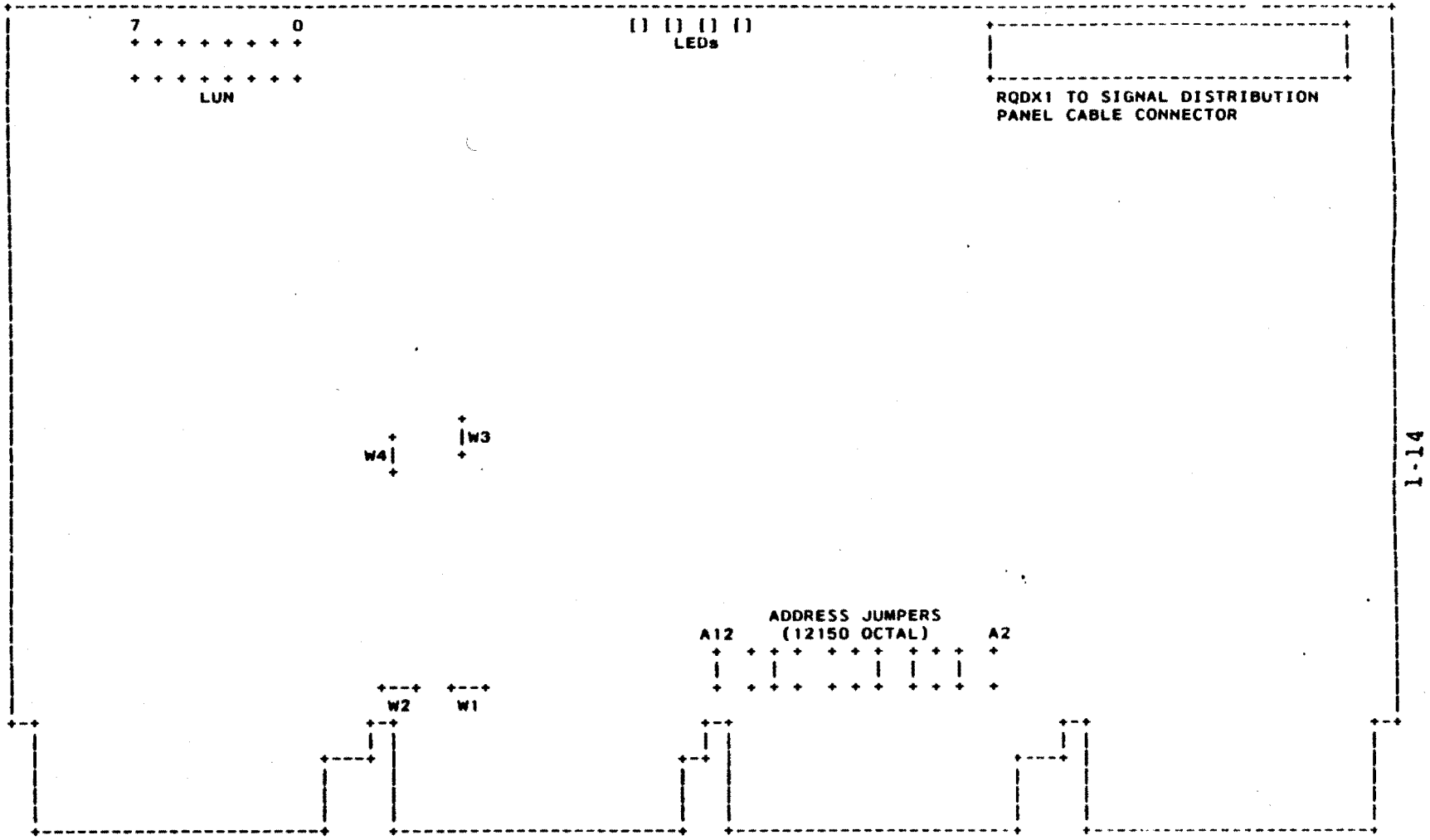


Figure 1-5: RQDX1 Jumpers

1.4 MASS STORAGE

The VAXstation I Mass Storage subsystem includes the RQDX1 Controller (Part Number M8639), RX50 Diskette Drive, and RD52 Fixed-disk Drive.

1.4.1 RQDX1 Controller

1.4.1.1 Jumpers - Figure 1-5 shows the three sets of RQDX1 jumpers in their factory-set configuration. W1 through W4 are for manufacturing use only. The LUN is set to LUN 0; that is jumpers LUN7 through LUN0 are all out. The device address is set to 772150 (octal); that is jumpers A12, A10, A6, A5, and A3 are in (see Table 1-6).

Table 1-6: RQDX1 Device Address Select

BDAL:	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
						DEVICE ADDRESS SELECT												
JUMPER A:						12	11	10	9	8	7	6	5	4	3	2		
	1	1	1	1	1	1	0	1	0	0	0	1	1	0	1	0	0	0
OCTAL:	7			7		2			1			5			0			

For more information on the RQDX1, see the RQDX1 User's Guide, EK-RQDX1-UG.

1.4.2 RX50 Diskette Drive

The RX50 is connected to the Mass Storage Cable Distribution Panel with one cable (Part Number 17-00285-02), and to the power supply with another cable (Part Number 70-20435-1K). This second cable also connects the RD52 to the power supply.

1.4.3 RD52 Fixed-disk Drive

The RD52 is connected to the Mass Storage Cable Distribution Panel with two cables (Part Numbers 17-00282 and 17-00286), and to the power supply with another cable (Part Number 70-20435-1K). This third cable also connects the RX50 to the power supply.

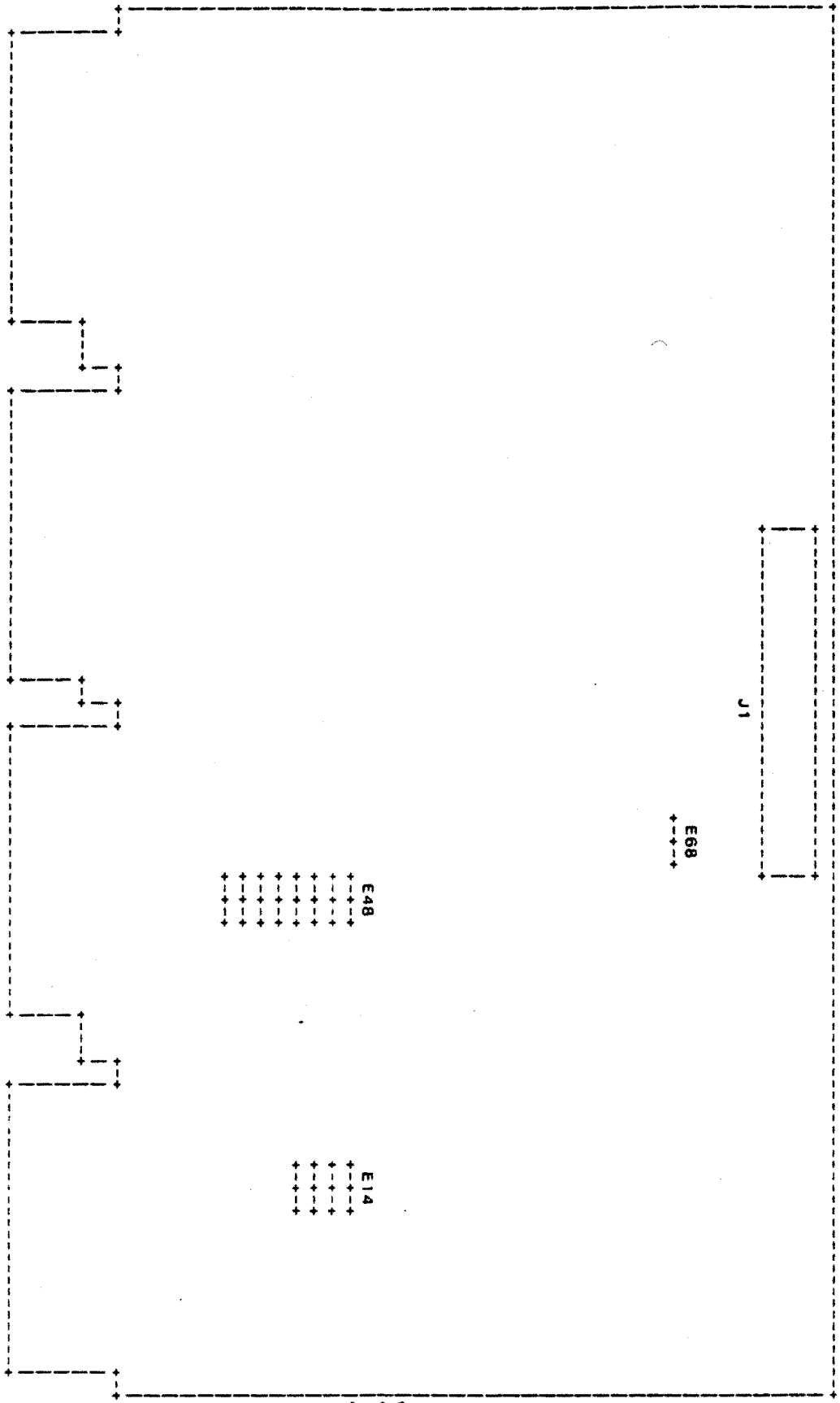


Figure 1-6: VCB01 Switches

1.5 VCB01 VIDEO CONTROLLER

The VCB01 is shown in Figure 1-6.

1.5.1 Switches

The VCB01 switches select:

- The MSA (Memory Starting Address)
- The CSR (Control and Status Register) base address
- Display density

1.5.1.1 Memory Starting Address (MSA) - Switches 1 through 4 of switch-pack E14 select the starting address for the 256 kB block of MicroVAX physical memory where the VCB01 resides. Table 1-7 shows the switch settings (**0 = ON** and **1 = OFF**).

Table 1-7: VCB01 MSA Selection

	BDAL:	21	20	19	18	
	E14:	S1	S2	S3	S4	
	(kB)					
*	3840	1	1	1	1	
	3584	1	1	1	0	
	3328	1	1	0	1	
	3072	1	1	0	0	
	2816	1	0	1	1	
	2560	1	0	1	0	
	2304	1	0	0	1	
	2048	1	0	0	0	
	1792	0	1	1	1	
	1536	0	1	1	0	
	1280	0	1	0	1	
	1024	0	1	0	0	
	768	0	0	1	1	
	512	0	0	1	0	
	256	0	0	0	1	1 = OFF
	0	0	0	0	0	0 = ON

* VAXstation I setting

The video memory always resides in the topmost 256 kB of the 4 MB MicroVAX physical address space. Therefore, all the MSA switches

are set to OFF; that is, BDAL<21:18> select the 256 kB block starting at 3840 k.

1.5.1.2 **CSR Base Address** - As Table 1-8 shows, BDAL<17:13> are all 1s (ones), giving an address range of 7600xx through 7777xx (octal). Switches 1 through 7 of switch-pack E48 correspond to BDAL<12:06>, and select the CSR base address (that is, the I/O registers base address). BDAL<05:01> select one of the 32 registers; and BDAL<00> is byte select and MBZ (must be zero). Currently, in the VAXstation I, E48 switches S7:S1 are set to 172 (octal). This makes BDAL<17:00> = 7772xx (octal; 3FExx, hex).

Table 1-8: CSR Base Address Select

	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BDAL:	(HARD WIRED)					CSR BASE ADDRESS							CSR SELECT					
E48:						S7	S6	S5	S4	S3	S2	S1						
	1	1	1	1	1	1	1	1	1	0	1	0	x	x	x	x	x	0
OCTAL:	7			7			7			2			X			X		

1.5.1.3 **Display Density** - Switch E68 and switch S8 of switch-pack E48 select either a full-page or half-page monitor (Table 1-9). The VR100 is a full-page monitor and E68 is ON (position C2); E48 S8 is OFF.

Table 1-9: Display Density Selection

	FULL-PAGE MONITOR	HALF-PAGE MONITOR
E68	ON (C2)	OFF (C1)
E48 S8	OFF	ON
DIAGNOL	48 cm (19 in)	38 cm (15 in)
PIXELS	829 k	384 k

1.6 OPERATOR I/O DEVICES

1.6.1 VR100 Video Monitor

The VR100 monitor (Part Number VR100-AA) has only two external controls, contrast and brightness (Figure 1-7). Alignment controls and adjustments are contained within the enclosure, and described in Chapter 3. The functions of the four LEDs are also described in Chapter 3.

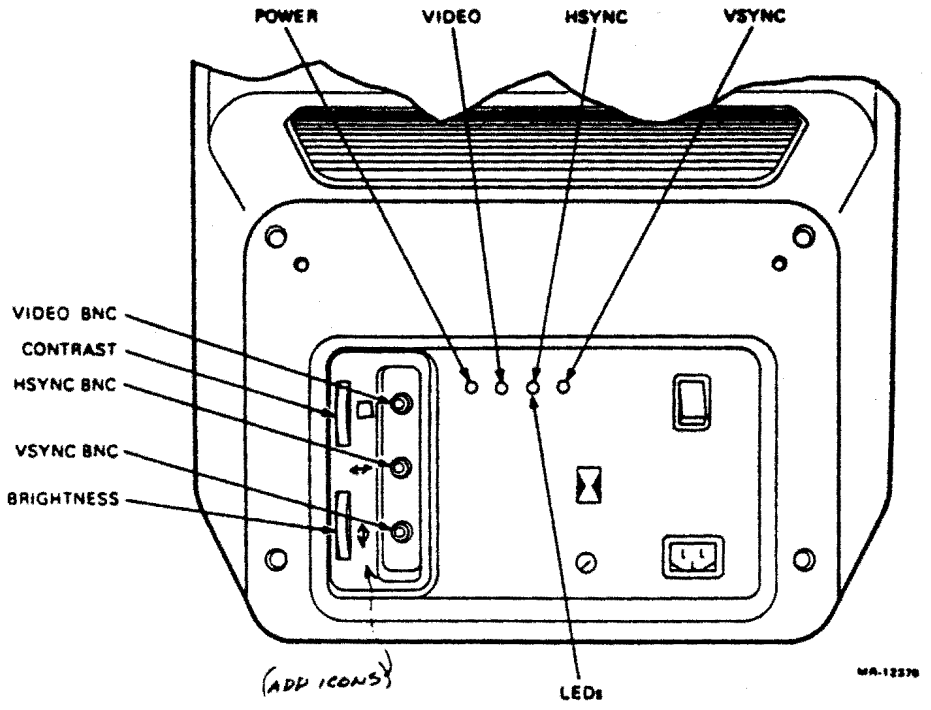


Figure 1-7: VR100 Monitor Rear Panel

The monitor is connected to the Patch and Filter Panel Assembly with the video cable (Part Number BC18T-10). At the VR100 end of this cable, the VIDEO, HSYNC, and VSYNC coaxial leads are connected to match the icons molded in the cable and the VR100 enclosure. The lead from the keyboard also plugs into the VR100 end of this cable.

1.6.2 LK201 Keyboard

The keyboard Part Number is LK201-CA. The keyboard lead is terminated in a 4-pin modular connector that plugs into the monitor end of the video cable (Part Number BC18T-10).

1.6.3 VS10X Mouse

The hand-held mouse (Part Number 30-20038-01) is connected to the Patch and Filter Panel Assembly with a 3.7 m (12 ft) 10-conductor cable.

1.6.4 LA50 And LA100 Printers

Either an LA50 or an LA100 can be connected to the CPU insert in the Patch and Filter Panel Assembly with a single cable (Part Number BC22D-10).

1.7 OPTION MODULES

1.7.1 DEQNA Ethernet Controller

The DEQNA (Figure 1-8) module (Part Number M7504) communicates with the Ethernet through an H4000 Ethernet Transceiver and Cable Tap. A Transceiver Cable connects the H4000 to the DEQNA insert in the Patch and Filter Panel Assembly.

NOTE - G7272 Required

In the VAXstation 1, it is recommended that the dual-height DEQNA be installed between the last quad-height MSV11-QA and the quad-height VCB01 (see section 2.1). Therefore, a G7272 Grant Continuity card must be installed in the A or C connector position of the same slot as the DEQNA.

1.7.1.1 Jumpers - Figure 1-8 shows the three DEQNA jumpers:

W1 This jumper identifies the first or second DEQNA in the system. Factory connected to pin 1 as shown, it identifies the first (and only, in the VAXstation 1) DEQNA. It is normally installed.

W2 This jumper controls the Hold-off Timer. It is normally removed.

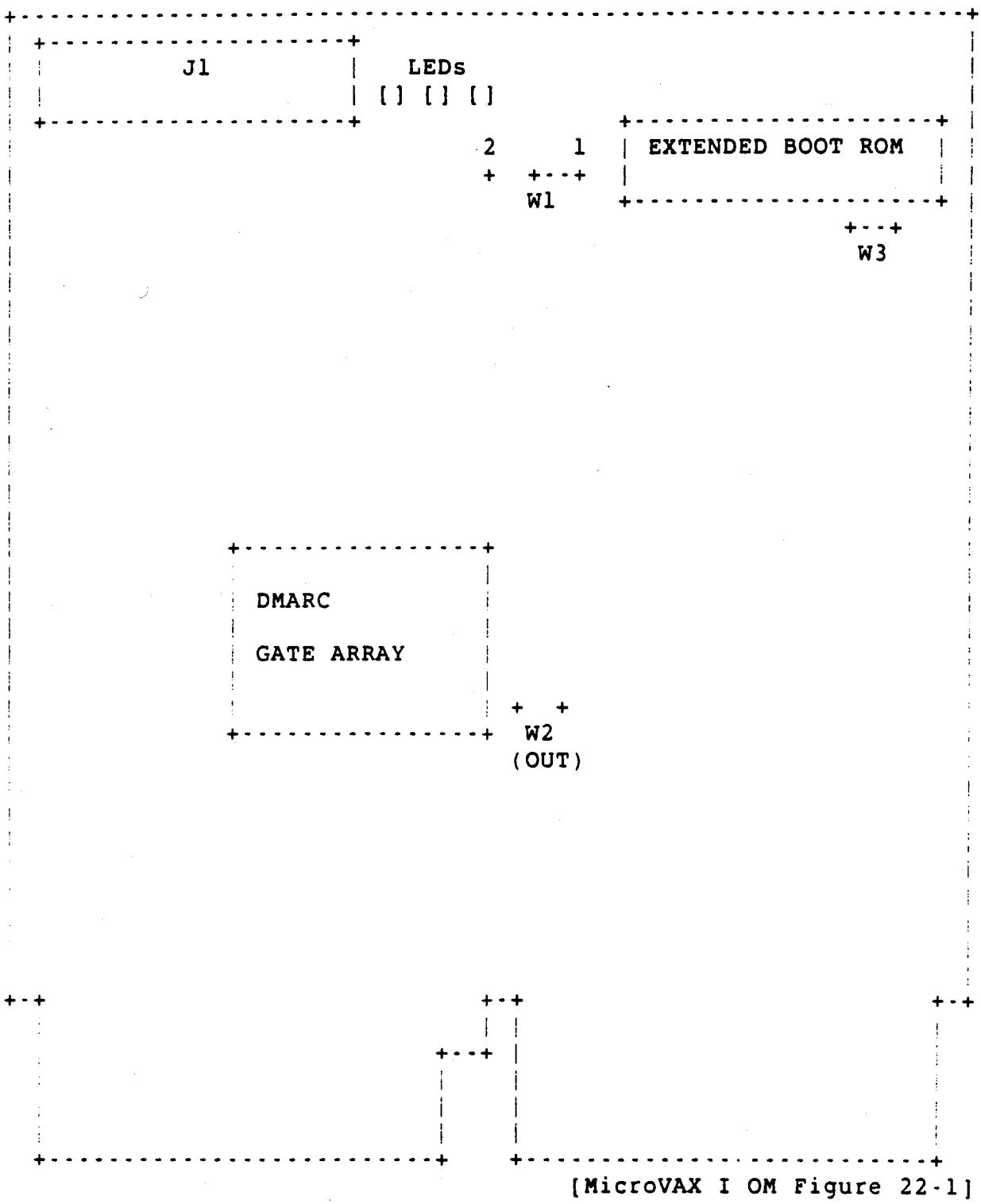


Figure 1-8: DEQNA Jumpers

W3 This jumper controls the Sanity Timer. It is normally installed.

Factory set as shown, W2 and W3 are correct for most applications. For more information see the DEQNA User's Guide EK-DEQNA-UG.

1.7.2 DZV11 Asynchronous Line Multiplexer

The DZV11 (Part Number M7957) includes the module, an insert for the Patch and Filter Panel Assembly, and a cable between the two.

1.7.2.1 Switches And Jumpers - As shown in Figure 1-9, the DZV11 contains a set of 10 and a set of 8 DIP switches, and 16 jumpers. The switches select the device starting address (Table 1-10) and floating vector (Table 1-11). The jumpers (Table 1-12) configure the module for various applications; factory set as shown, they are correct for most applications.

The address switches are factory set to address 760100 (all OFF except S7):

Table 1-10: DZV11 Address Switches

BDAL:	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
						DEVICE ADDRESS SELECT												
SWITCH																		
S:						1	2	3	4	5	6	7	8	9	10			
A:						12	11	10	9	8	7	6	5	4	3			
	1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0
OCTAL:	7			6		0			1			0				0		

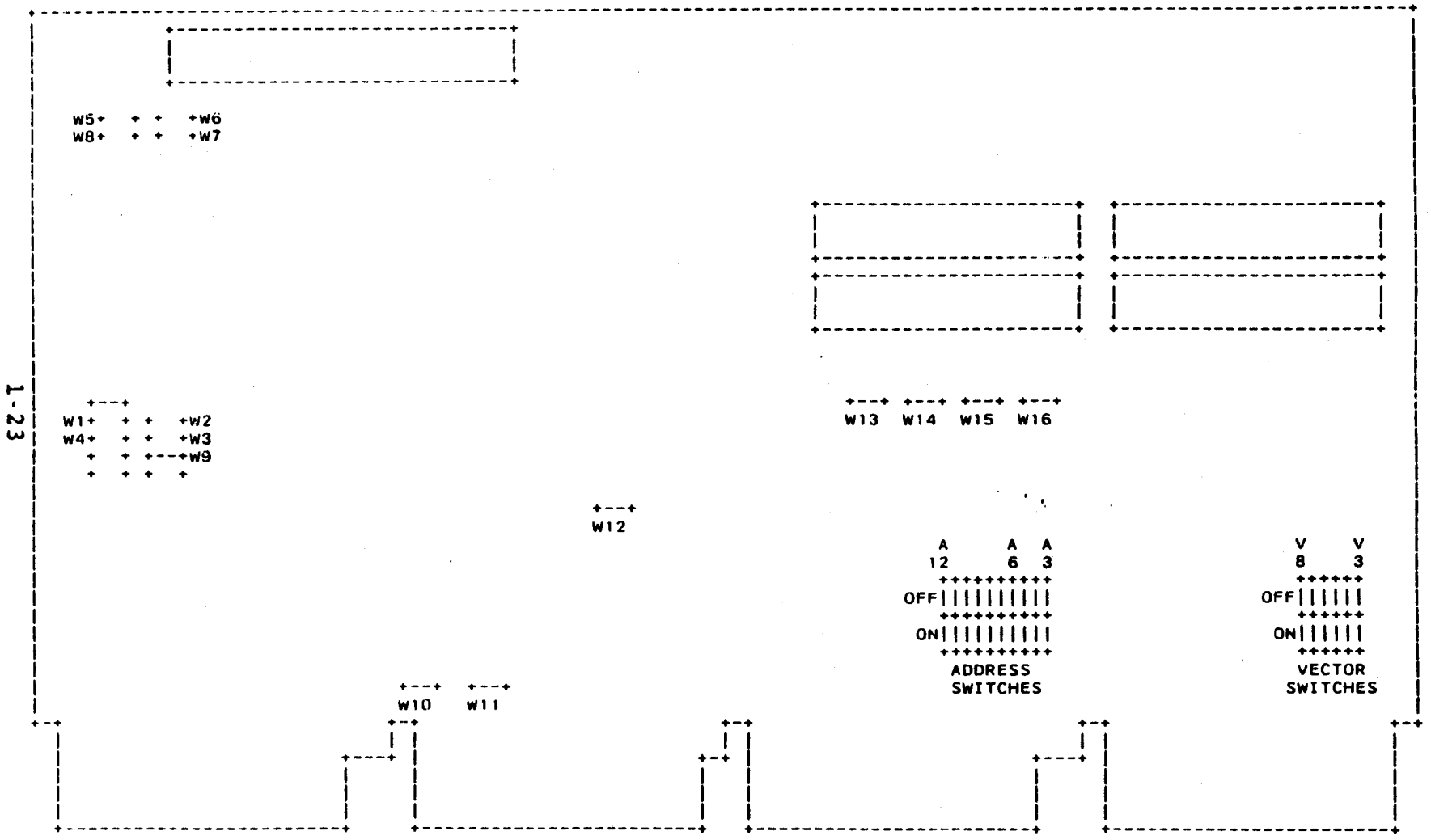


Figure 1-9: DZV11 Switches and Jumpers

The vector switches are factory set to vector **310: S1, S4, and S5 OFF; S2, S3, and S6 ON.** Switches S7 and S8 are not used:

Table 1-11: DZV11 Vector Switches

BDAL:	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
										VECTOR SELECT								
SWITCH																		
S:										1	2	3	4	5	6	7	8	
V:										8	7	6	5	4	3			
										0	1	1	0	0	1	0	0	0
OCTAL:										3			1			0		

Table 1-12: DZV11 Jumpers

JUMPER	STATUS	NOTE	FUNCTION
W1	REMOVED		W1:W4 connect DTR (data terminal ready to RTS (request to send)
W2	REMOVED		
W3	REMOVED		
W4	REMOVED		
W5	REMOVED		W5:W8 connect FB (forced busy) to RTS
W6	REMOVED		
W7	REMOVED		
W8	REMOVED		
W9	INSTALLED	1	W9:W16 connect bus signals
W10	INSTALLED	2	
W11	INSTALLED	2	
W12	INSTALLED	1	
W13	INSTALLED	1	
W14	INSTALLED	1	
W15	INSTALLED	1	
W16	INSTALLED	1	

NOTES: 1. Removed only for manufacturing tests. Should not be removed in the field.
2. Removed if the module is installed in C/D interconnect slot.

For more information, see the DZV11 Asynchronous Multiplexer Technical Manual, EK-DZV11-TM.

CHAPTER 2

PROGRAMMING INFORMATION

This chapter briefly describes the programmable functions of the VCB01; that is, the functions that can be specified and/or examined by software. For more information see Chapter 4 in the VAXstation I Technical Manual, EK-VS200-TM.

2.1 VCB01 REGISTERS

Control and Status information is exchanged between the VCB01 and the CPU through 32 16-bit locations in the I/O Page. These locations are listed in Table 2-1 and described below.

NOTE - Bit Descriptions

Many of the bit descriptions in the following tables include a value in parenthesis; for example: (1 = chip armed). This usually indicates the initialized value of the bit.

Table 2-1: VCB01 Registers

ADDRESS*	NAME
BASE	CSR -- Control and Status Register
BASE+2	Cursor X Position
BASE+4	Mouse Position Register
BASE+6	(spare)
BASE+8	CRTC Address Pointer Register
BASE+10	CRTC Data Register
BASE+12	ICDR -- Interrupt Controller Data Register
BASE+14	ICSR -- Interrupt Controller Command/Status Register
BASE+16	(spare)
through	
BASE+31	(spare)
BASE+32	UART Mode Registers 1A and 2A
BASE+34	UART Status/Clock Select Register A
BASE+36	UART Command Register A
BASE+38	UART Transmit/Receive Buffer A
BASE+40	(spare)
BASE+42	UART Interrupt Status/Mask Register
BASE+44	(spare)
BASE+46	(spare)
BASE+48	UART Mode Registers 1B and 2B
BASE+50	UART Status/Clock Select Register B
BASE+52	UART Command Register B
BASE+54	UART Transmit/Receive Buffer B
BASE+56	(spare)
through	
BASE+62	(spare)

* BASE = The CSR Base Address

2.1.1 Control And Status Register

The CSR bits are described in Figure 2-1 and Table 2-2. Note that following a Q22-bus BINIT, bits <06:02> are cleared (= 0).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
nu	BR3	BR2	BR1	BR0	MSC	MSB	MSA	CUR	IEN	TST	VRB	FNC	VID	nu	MOD

ADDRESS = CSR BASE

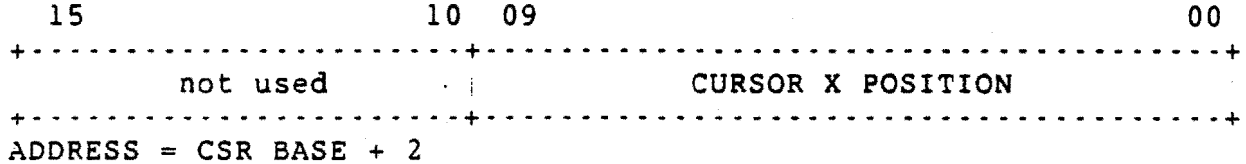
Figure 2-1: CSR Format

Table 2-2: CSR Bits

BITS	ACCESS	DESCRIPTION
<15>		(spare - not used)
<14:11>	READ	Memory bank switch 0:3 (MSA switch E14 S1:S4)
<10:09>	READ	Mouse switch C:A (0 = closed)
<07>	READ	Cursor active (1 = cursor on)
<06>	RD/WR	Interrupt Enable (1 = enabled)
<05>	RD/WR	Test Bit (used with loop-back connector)
<04>	RD/WR	Enable video read-back (1 = enabled)
<03>	RD/WR	Cursor function (1 = OR, 0 = AND)
<02>	RD/WR	Enable video output (1 = enabled)
<01>		(spare - not used)
<00>	READ	19 in / 15 in mode (1 = 19 in)

2.1.2 Cursor X Position

This location contains the horizontal position of the top left corner of the 16 X 16 (pixel) cursor image. The value is in pixels and must not allow the cursor to be positioned beyond the maximum X pixel. That is, the maximum value is 943 (959 - 16) for a VR100 monitor, and 783 (799 - 16) for a 38 cm (15 in) monitor.



ADDRESS = CSR BASE + 2

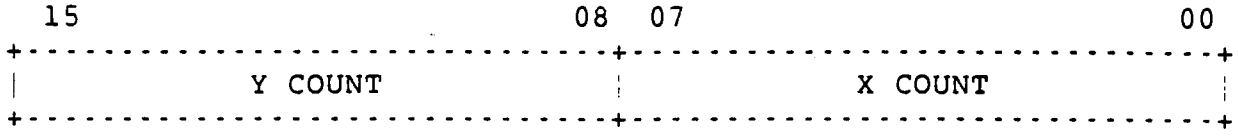
Figure 2-2: Cursor X Position Format

Table 2-3: Cursor X Position Bits

BITS	ACCESS	DESCRIPTION
<15:10>		(not used)
<09:00>	WRITE	Cursor X position in pixels.

2.1.3 Mouse Position Register

This register contains mouse X and Y position values. The values are counted up or down, in proportion to the direction and amount of mouse movement.



ADDRESS = CSR BASE + 4

Figure 2-3: Mouse Position Register Format

Table 2-4: Mouse Position Register Bits

BITS	ACCESS	DESCRIPTION
<15:08>	READ	Mouse Y position count.
<07:00>	READ	Mouse X position count.

2.1.4 CRTC Registers

2.1.4.1 CRTC Address Register Pointer - This register points to the one of 17 internal CRTC registers (Table 2-6), that is to receive the data contained in the CRTC Data Register (described below). It also contains three status bits (Figure 2-4 and Table 2-5).

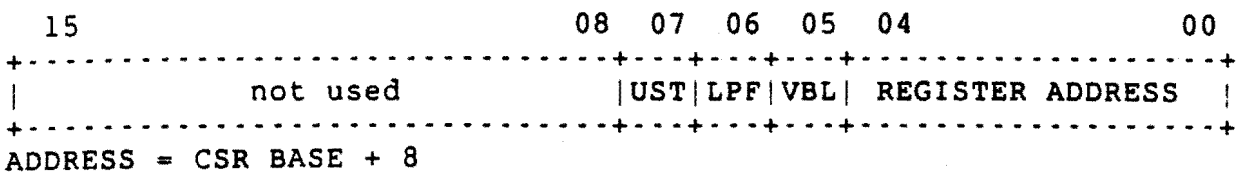


Figure 2-4: CRTC Address Register Pointer Format

Table 2-5: CRTC Address Register Pointer Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
<07>	READ	Update strobe (not used)
<06>	READ	Light pen register full (1 = full)
<05>	READ	Vertical blank (1 = Vblank time)
<04:00>	WRITE	CRTC internal register address (Table 2-6)

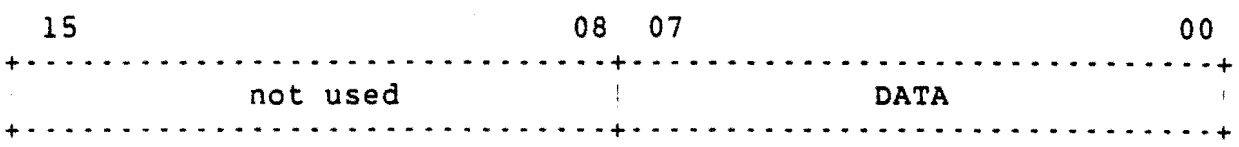
Table 2-6: CRTC Internal Registers

REG	NAME	DESCRIPTION
00	Horizontal Total	The total number of character times in a line, minus 1.
01	Horizontal Displayed	The total number of displayed characters in a line.
02	Hsync Positon	Defines the number of character times until Hsync (horizontal sync).
03	Hsync/Vsync Widths	Four bits each are used to define the Hsync pulse width and the Vsync (vertical sync) pulse width.
04	Vertical Total	Total number of character rows on the screen, minus 1.
05	Vertical Total Adjust	The number of scan lines to complete the screen.
06	Vertical Displayed	The number of character rows displayed.
07	Vsync Position	Number of character rows until Vsync.

Table 2-5: CRTC Internal Registers (continued)

REG	NAME	DESCRIPTION
08	Mode	Controls addressing, interlace, and cursor.
09	Maximum Scan Line	The number of scan lines in a character row, minus 1.
10	Cursor Scan Start	Defines the scan line at which the cursor starts.
11	Cursor Scan End	Defines where the cursor ends.
12	Start Address High	Defines the RAM location where video refresh begins.
13	Start Address Low	
14	Cursor Address High	Defines the cursor position in RAM.
15	Cursor Address Low	
16	Light Pen Position High	Contains the position of the light pen.
17	Light Pen Position Low	

2.1.4.2 CRTC Data Register - This register contains the eight bits of data to be loaded into the internal CRTC register addressed by bits <04:00> of the CRTC Address Pointer Register (above).



ADDRESS = CSR BASE + 10

Figure 2-5: CRTC Data Register Format

Table 2-7: CRTC Data Register Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
<07:08>	RD/WR	CRTC internal register data

2.1.5 Interrupt Controller Registers

2.1.5.1 ICDR - The Interrupt Controller Data Register contains the data for/from the internal Interrupt Controller register addressed by the last Preselect command (see ICSR, below).

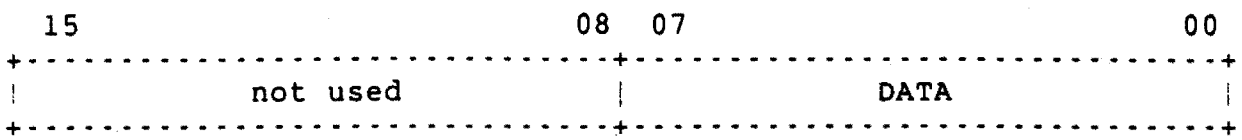


Figure 2-6: ICDR Format

Table 2-8: ICDR Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
<07:08>	RD/WR	Interrupt Controller internal register data

2.1.5.2 ICSR - The internal Interrupt Controller registers are accessed through the ICDR (above) and the ICSR (Interrupt Controller Command/Status Register). The ICSR is a command register on write operations and a status register on read operations.

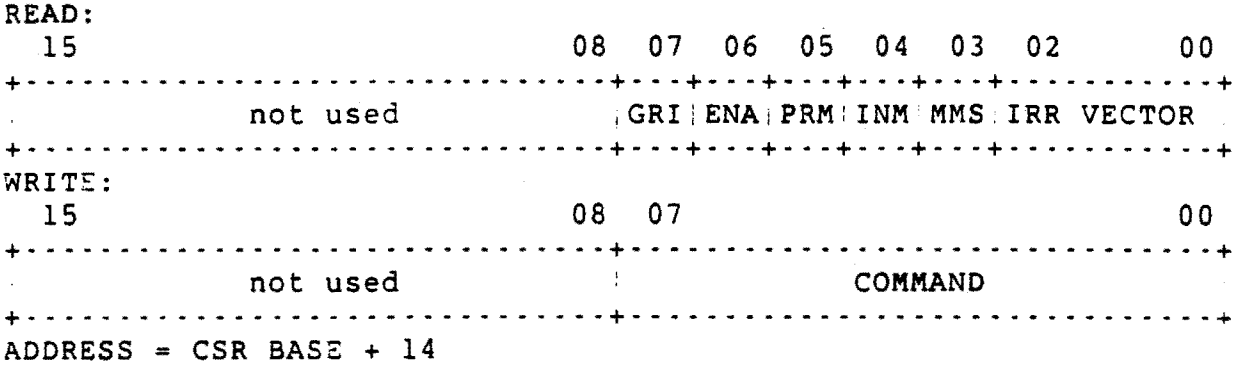


Figure 2-7: ICSR Format

Table 2-9: ICSR Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
<07>	READ	Group interrupt (1 = interrupt pending). Vector is in bits <02:00>.
<06>	READ	Enable (1 = chip enabled).
<05>	READ	Priority mode (1 = rotating, 0 = fixed).
<04>	READ	Interrupt mode (1 = polled, 0 = interrupt).
<03>	READ	Master mask (1 = chip armed).
<02:00>	READ	Binary vector of the highest unmasked bit in the IRR (Interrupt Controller Interrupt Response Register). Valid only when bit <07> is set.
<07:00>	WRITE	Command (see Table 2-10).

Table 2-10: ICSR Commands

ICSR* <07:00>	COMMAND	DESCRIPTION
00000000	RESET	Sets the IMR (Interrupt Mask Register) to all ones. Clears to zeros, the IRR (Interrupt Response Register), ISR (Interrupt Service Register), ACR (Auto Clear Register), and Mode Register. Response Memory and byte count registers are not affected.
00010xxx	CLEAR IRR AND IMR	Clears all bits in the IRR and IMR.
00010BBB	CLEAR ONE IRR AND IMR BIT	Clears both the IRR bit and the IMR bit specified in <02:00>.
00110xxx	SET IMR	Sets all IMR bits to ones.
00111BBB	SET ONE IMR BIT	Sets the IMR bit specified in <02:00>.
01000xxx	CLEAR IRR	Clears all IRR bits to zeros.
01001BBB	CLEAR ONE IRR BIT	Clears the IRR bit specified in <02:00>.
0110xxxx	CLEAR HIGHEST PRIORITY ISR BIT	Clears the highest priority bit set in the ISR.
01110xxx	CLEAR ISR	Clears all ISR bits to zeros.
01111BBB	CLEAR ONE ISR BIT	Clears the ISR bit specified in <02:00>.
100MMMMM	LOAD MODE BITS M4:M0	Sets the five low-order bits of the Mode Register to the value in <04:00>.

Table 2-10: ICSR Commands (continued)

ICSR* <07:00>	COMMAND	DESCRIPTION
1010MMNN	CONTROL MODE BITS M7:M5	Sets Mode Register bits 6 and 5 to the value in <06:05>. Mode Register bit 7 is set according to <01:00>, as follows: 01 00 Bit 7 -- -- --------- 0 0 Unchanged 0 1 Set 1 0 Cleared 0 0 (illegal)
1011xxxx	PRESELECT IMR FOR WRITING	All future write operations to the ICDR load the data into the IMR.
1100xxxx	PRESELECT ACR FOR WRITING	All future write operations to the ICDR load the data into the ACR.
11100LLL	PRESELECT RESPONSE MEMORY FOR WRITING	All future write operations to the ICDR load the data into the Response Memory at the interrupt request level location specified in <02:00>.

* x = 1 or 0 (doesn't matter)

2.1.5.3 **IRR** - The 8-bit Interrupt Request Register stores pending interrupt requests. An IRR bit is set when the corresponding interrrupt request line is asserted; and automatically cleared when the request is acknowledged. The IRR bits can be read, set, and cleared through the ICSR and ICDR. RESET clears the IRR.

2.1.5.4 **IMR** - The 8-bit Interrupt Mask Register is used to enable (bit cleared) or disable (bit set) the corresponding interrupt request lines. A set IMR bit does not disable the IRR bit, and the request will remain pending until the IMR bit is cleared. Only unmasked interrupts generate the Group Interrupt output. All IMR bits are set by RESET.

2.1.5.5 ISR - The 8-bit Interrupt Service Register stores the acknowledge status of interrupt requests. When an interrupt is acknowledged, the controller selects the highest priority pending request, clears its IRR bit, and sets its ISR bit. ISR bits can be automatically cleared at the end of the acknowledge cycle or on specific command. The ISR can be read throught the ICSR and ICDR. RESET clears the IRR.

2.1.5.6 ACR - The 8-bit Auto Clear Register specifies the clearing mode for the ISR. A set ACR bit specifies the corresponding ISR bit will be automatically cleared at the end of the acknowledge cycle; and a cleared ACR bit means that the corresponding ISR bit must be cleared by the CPU through the ICSR and ICDR. The ACR can be read through the ICSR and ICDR. RESET clears the ACR.

2.1.5.7 Mode - The 8-bit Interrupt Controller Mode Register controls many controller options. The Mode register is loaded through the ICSR and ICDR. It cannot be read. Bits 00, 02, and 07 are available to the ICSR on read operations. RESET clears the Mode register. The bits are described in Table 2-11.

Table 2-11: Interrupt Controller Mode Register Bits

BITS	DESCRIPTION
07	MM -- Master Mask. Enables (set) and disables (cleared) group interrupts to the CPU.
06:05	RP1:RP0 -- Repister Preselect. Select the internal register to be read when the CPU reads the ICDR: RP1 RP0 Register 0 0 ISR 0 1 IMR 1 0 IRR 1 1 ACR
04	REQP -- Interrupt Request Polarity. Determines interrupt request transition direction for setting IRR bits. Set = LOW to HIGH, cleared = HIGH to LOW. (Should always be cleared.)
03	GIP -- Group Interrupt (GINT) Polarity. When set, GINT is asserted HIGH; when cleared, GINT is asserted LOW. (Should always be cleared.)

Table 2-11: IMR Bits (continued)

BITS	DESCRIPTION
02	IM -- Interrupt Mode. When set, **polled mode** is selected, and group interrupt disabled. The controller will not interrupt the CPU. To respond determine if there are any pending interrupts, the CPU must read the ICSR. When cleared, **interrupt mode** is selected, and group interrupt functions normally.
01	VS -- Vector Selection. When cleared, each interrupt will generate its own vector (contained in Response Memory). When set, all interrupts generate the same vector (request level 0 vector).
00	PM -- Priority Mode. When cleared (**fixed priority**), level 0 interrupt requests are the highest priority, level 7 the lowest. When set (**rotating priority**), the last interrupt level serviced becomes the lowest priority level.

2.1.6 UART Registers

2.1.6.1 Mode Registers 1A And 2A - These UART registers are accessed by two successive references to the same I/O address.

1A:

15 ... 08	07	06	05	04	03	02	01	00
not used	RRC	RIS	ERM	PAR	MOD	PAT	B/CHAR	

2A:

15 ... 08	07	06	05	04	03 ... 00
not used	CH MODE	TRC	CET	STOP BIT	LENGTH

ADDRESS = CSR BASE + 32

Figure 2-8: Mode Registers 1A and 2A Format

Table 2-12: Mode Registers 1A and 2A Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
1A:		
<07>	RD/WR	Rx (receive) RTS (request to send) control (1 = no).
<06>	RD/WR	Rx interrupt select (1 = FIFO full).
<05>	RD/WR	Error mode (1 = block).
<04:03>	RD/WR	Parity mode (10 = no parity).
<02>	RD/WR	Parity type (1 = odd).
<01:00>	RD/WR	Bits per character (11 = 8).
2A:		
<07:06>	RD/WR	Channel mode (00 = normal).
<05>	RD/WR	Tx (transmit) RTS control (1 = no).
<04>	RD/WR	CTS (clear-to-send) enable Tx (1 = no).
<03:00>	RD/WR	Stop bit length (0111 = 1 bit).

2.1.6.2 Mode Registers 1B And 2B - (ADDRESS = CSR BASE + 48) See Mode Registers 1A and 2A

2.1.6.3 Status/Clock Select Register A - This register returns UART status information on a read, and selects the Transmit and Receive baud rates on a write.

READ:

15 ... 08	07	06	05	04	03	02	01	00
not used	RXB	FER	PER	OER	TXE	TXR	FFL	RXR

WRITE:

15 ... 08	07 ... 04	03 ... 00
not used	RX CLOCK SELECT	TX CLOCK SELECT

ADDRESS = CSR BASE + 34

Figure 2-9: Status/Clock Select Register A Format

Table 2-13: Status/Clock Select Register A Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
<07>	READ	Received break (1 = yes).
<06>	READ	Framing error (1 = yes).
<05>	READ	Parity error (1 = yes).
<04>	READ	Overrun error (1 = yes).
<03>	READ	Transmitter empty (1 = yes).
<02>	READ	Transmitter ready (1 = yes).
<01>	READ	FIFO full (1 = yes).
<00>	READ	Receiver ready (1 = yes).
<07:04>	WRITE	Receiver clock select (1001 = 4800 baud).
<03:00>	WRITE	Transmitter clock select (1001 = 4800 baud).

2.1.6.4 Status/Clock Select Register B - (ADDRESS = CSR BASE + 50) See Status/Clock Select Register A

2.1.6.5 Command Register A - All the bits in this UART register are write access only.

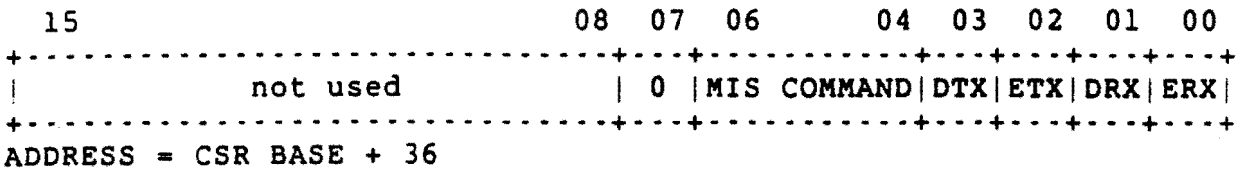


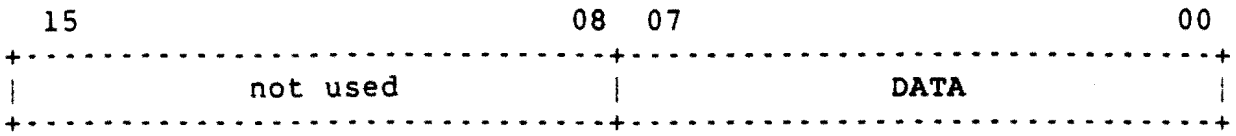
Figure 2-10: Command Register A Format

Table 2-14: Command Register A Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
<07>	WRITE	(spare - must be zero).
<06:04>	WRITE	Miscellaneous commands: 000 NOP (no operation) 001 Reset mode register pointer. Causes the Mode Register pointer to point to register 1. 010 Reset receiver 011 Reset transmitter 100 Reset error status. Clears error status bits <07:04> in Status/Clock Select Register. 101 Reset channel A break-change interrupt. Clears Interrupt Status/Mask Register bit <02>. 110 Start break 111 Stop break
<03>	WRITE	Disable Transmitter (1 = yes).
<02>	WRITE	Enable Transmitter (1 = yes).
<02>	WRITE	Disable Receiver (1 = yes).
<00>	WRITE	Enable Receiver (1 = yes).

2.1.6.6 Command Register B - (ADDRESS = CSR BASE + 52) See Command Register A

2.1.6.7 Transmit/Receive Buffer A -



ADDRESS = CSR BASE + 38

Figure 2-11: Transmit/Receive Buffer A Format

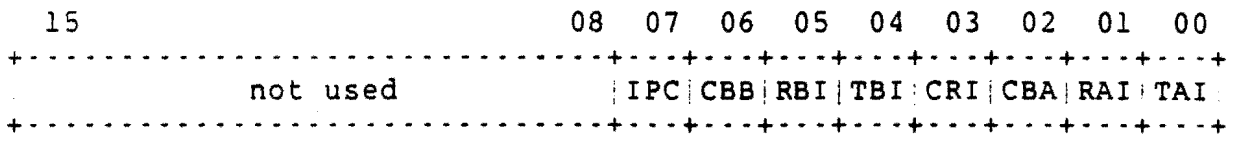
Table 2-15: Transmit/Receive Buffer A Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
<07:00>	READ	Receive data.
<07:00>	WRITE	Transmit data.

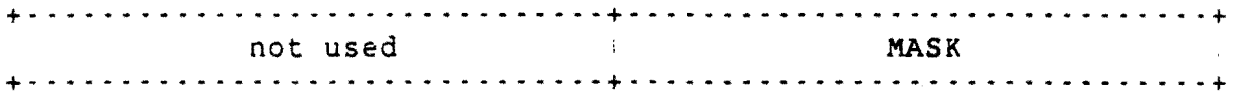
2.1.6.8 Transmit/Receive Buffer B - (ADDRESS = CSR BASE + 54) See Transmit/Receive Buffer A

2.1.6.9 Interrupt Status/Mask Register - This register transfers interrupt status on a read. On a write, set bits enable the UART interrupt request associated with the corresponding status bit.

READ:



WRITE:



ADDRESS = CSR BASE + 42

Figure 2-12: Interrupt Status/Mask Register Format

Table 2-16: Interrupt Status/Mask Register Bits

BITS	ACCESS	DESCRIPTION
<15:08>		(not used)
<07>	READ	Input port change (1 = yes).
<06>	READ	Change in break B (1 = yes).
<05>	READ	Receiver ready/FIFO full B (1 = yes).
<04>	READ	Transmitter ready B (1 = yes).
<03>	READ	Counter ready (1 = yes).
<02>	READ	Change in break A (1 = yes).
<01>	READ	Receiver ready/FIFO full A (1 = yes).
<00>	READ	Transmitter ready A (1 = yes).
<07:00>	WRITE	Bit-for-bit mask to enable interrupt request asscociated with the above status bits (00000010 = enable Receiver Ready interrupt on channel A).

CHAPTER 3

MAINTENANCE

This chapter briefly describes maintenance features, diagnostic procedures, and monitor alignment. A troubleshooting flow (Table 3-11) is included at the end of the chapter. For more information see Chapter 5 in the VAXstation I Technical Manual, EK-VS200-TM.

3.1 MICROVERIFY

Microverify is automatically executed at power-up, and in response to the console-mode TEST command.

CAUTION - Console Mode

> Before entering console mode, all open files should be closed, and all open accounts logged-off the system. The console interface is described in Appendix A of the VAXstation I Owner's Manual, EK-VS200-OM.

Microverify normally runs in single-pass mode, but can be configured to run in multiple-loop mode (see Chapter 1, subsection 1.2.1.2)

In single-pass mode, the result of Microverify execution is reported on the monitor screen as follows:

MICROVERIFY STARTED

(approximately five seconds later:)

MICROVERIFY PASSED

(or)

MICROVERIFY FAILED

When Microverify, including the VCB01 self-tests, is successfully completed and bootstrap is initiated, the keyboard bell sounds.

3.1.1 Microverify Error Reporting

If the MICROVERIFY FAILED response is displayed, the system returns to console mode, and the >>> console prompt is displayed on the screen. Failures are reported in the seven-segment LED located on the CPU insert in the Patch and Filter Panel assembly (and in the LEDs on the M7135-YA DAP module). A blinking code indicates a VCB01 self-test failure. The failure codes are listed in Table 3-1.

Table 3-1: Microverify Error Codes

CODE	DESCRIPTION/ACTION
7	Microverify failed before completing the DAP microsequencer test. Error on DAP module.
6	M7135-YA DAP error.
5	M7136 MCT error.

Table 3-1: Microverify Error Codes (continued)

CODE	DESCRIPTION/ACTION
4	Undertermined error in DAP/MCT interface. Could be DAP, MCT, or interconnect cable.
3	Memory error. Run CPU (EHKAA) and memory (EHXMS) diagnostics.
2	Boot device was not found. Check RQDX1 controller.
1	Unable to boot from selected device (media/drive fault).
.	(period) Primary bootstrap successful. Control passed to secondary bootstrap.
BLINKING 7 BLINKING 6	Scan line map test failed if either blinking 7 or blinking 6 is displayed. Replace the VCB01.
BLINKING 5	Keyboard power-up self-test failed. Check keyboard cable and BC18T-10 video cable connections, or replace the keyboard, or replace the VCB01.
BLINKING 4	DUART polled loop-back test failed. Replace the VCB01.
BLINKING 3	Bitmap memory test failed. Replace the VCB01.
BLINKING 2	Register probe test failed: a) Make sure the VCB01 is in the correct backplane slot (see Chapter 2, subsection 2.1). b) Make sure the MSA is set to 3840 k. VCB01 switch pack E14, S1:S4 all OFF. c) Replace VCB01.

Table 3-1: Microverify Error Codes (continued)

CODE	DESCRIPTION/ACTION
BLINKING 1	Failed CSR test: a) Make sure that the CSR base address is 177200. VCB01 switch pack E48: S1 S2 S3 S4 S5 S6 S7 ON ON ON ON OFF ON OFF b) Replace VCB01.

3.1.2 Monitor Display Errors

In addition to displaying diagnostic failure reports, the monitor display itself may indicate errors, as described in Table 3-2.

Table 3-2: Monitor Display Errors

DISPLAY	DESCRIPTION/ACTION
HALF-PAGE	Check VCB01 switches E68 and E48 S8.
IMPROPER SYNC	Check VCB01 switches E68 and E48 S8. E68 = OFF E48 S8 = ON

3.2 STANDALONE DIAGNOSTICS

The standalone diagnostic comprise:

- Macroverify (EHKMV)
- CPU Diagnostic (EHKAA)
- Memory Diagnostic (EHXMS)

The three diagnostics are contained on one diskette, labeled

"MICROVAX DIAGNOSTICS 1 of 3," and are run with the system in console mode.

3.2.1 Macroverify

Macroverify (EHKMV) is normally run to verify system installation, and run before any other diagnostics to isolate faults. Running Macroverify does not destroy disk data.

3.2.1.1 Running Macroverify - Figure 3-1 is an example of a Macroverify run report. To run Macroverify:

1. Close any open files and log-out any open accounts.
2. Turn system power OFF.
3. Disconnect external cables from the DZV11 patch panel (if any).
4. Turn monitor power ON.
5. Turn system power ON.
6. Enter console mode (press the HALT button twice).
7. Insert a blank diskette in drive 2.
8. Insert the MICROVAX DIAGNOSTICS 1 of 3 diskette in drive 1.
9. In response to the >>> console prompt type:

   >>> B DUA1<RETURN>

```
>>> B DUA1
ATTEMPTING BOOTSTRAP


Macroverify V1.7


This MicroVAX is at microcode revision level 5, hardware revision
level 1, and includes support for F_FLOAT and D_FLOAT data types.

Testing          Time to Test (Mins.)   Comments

Memory           0:50                   TEST SUCCEEDED (1.0 MB)
Disk unit DUA0   0:20                   TEST SUCCEEDED (RD52)
Disk unit DUA1   0:20                   TEST SUCCEEDED (RX50)
Disk unit DUA2   0:20                   TEST SUCCEEDED (RX50)
DLVJ1            0:40                   DEVICE DLVJ1 WITH CSR 776500 NOT FOUND.
                                        NO TESTING PERFORMED.
DZV11            0:40                   TEST SUCCEEDED
DEQNA            0:10                   TEST SUCCEEDED (Address=AA-00-03-01-10)
VCB01            0:10                   TEST SUCCEEDED

Macroverify test completed.

Press RETURN key to enter console command mode.
```

Figure 3-1: Macroverify Run Report

Verify that the reported memory size (1 MB in Figure 3-1) is the size of memory installed in the system. If not, run the Memory Diagnostic (EHXMS, described below).

Macroverify tests each device to see if it responds to its assigned Q2-bus address. If the device does not respond, no testing is done and Macroverify outputs the device name, CSR address, and vector address (see DLVJ1 in Figure 3-1). The vector address is not output for devices with floating vectors (such as the DLVJ1 and DEQNA). Verify that devices not found are not installed.

For devices that do respond, the test result is reported as either TEST SUCCEEDED or TEST FAILED. If a given test time exceeds the minutes indicated in *Time to Test (Mins.)* (that is, SUCCEEDED or FAILED status is not reported), assume the device

failed. A complete Macroverify run takes approximately four minutes. If a device fails Macroverify testing, run the specific device diagnostic.

3.2.1.2 Macroverify Error Messages - The diagnostic reports operator and hardware errors in the *Comments* column (Figure 3-1). The following list gives some examples and corrective action.

MESSAGE: Please verify that the cable from the DEQNA module to the DEQNA patch panel assembly is correctly connected. Please verify that the fuse at the DEQNA patch panel assembly has not blown.
ACTION: Check cable connection and fuse.

MESSAGE: This unit either has no media or has been disabled. Please correct and rerun this diagnostic.
ACTION: Make sure the Fixed Disk Ready pushbutton (on the system control panel) is in the out position (glowing green) and that the diskettes are correctly inserted. Re-run Macroverify.

MESSAGE: This disk is not hardware formatted. Please format the disk, or, if this is a diskette, please use another diskette with correct hardware format and rerun this diagnostic.
ACTION: Fixed-disk -- run the disk subsystem diagnostic.
Diskette -- Insert the correct diskette and re-run Macroverify.

MESSAGE: This disk is write protected. Please enable writing on the disk and rerun this diagnostic. NOTE: Testing will not destroy disk data.
ACTION: Fixed-disk -- put the Fixed Disk Write Protect and Ready push buttons (on the system control panel) in the out position (Write Protect does not glow, Ready glows green).
Diskette -- Remove the write protect tab from the diskette or replace the diskette with one that has the write protect tab removed. Insert the diskette (the Removable Disk Write Protect indicator(s) should be off). Re-run Macroverify.

3.2.2 CPU Diagnostic

This diagnostic (EHKAA) is run when a CPU fault is indicated by Microverify or Macroverify failing, intermittent system problems, or failure to bootstrap correctly.

3.2.2.1 **Running The CPU Diagnostic** - Figure 3-2 is an example of a CPU diagnostic run report. To run the diagnostic:

1. Insert the MICROVAX DIAGNOSTICS 1 of 3 diskette in drive 1.

2. In response to the >>> console prompt enter:

   >>> B/100 DUA1<RETURN>

3. Enter the CPU diagnostic file name when the Bootfile: prompt appears:

   Bootfile: **[SYS0.SYSMAINT]EHKAA.EXE<RETURN>**

The test will start running, and report every 10 passes (approximately 20 seconds) as shown in Figure 3-2. It will continue to run until an error is detected, or until it is stopped (press HALT pushbutton twice).

```
-----------------------------------------------------------------

     EHKAA V1.13 CPU Test


     EHKAA V1.13 pass number 10 done!
     EHKAA V1.13 pass number 20 done!
     EHKAA V1.13 pass number 30 done!
     EHKAA V1.13 pass number 40 done!
     EHKAA V1.13 pass number 50 done!
     EHKAA V1.13 pass number 60 done!

-----------------------------------------------------------------
```

Figure 3-2: CPU Diagnostic Run Report

3.2.2.2 **CPU Diagnostic Error Reporting** - If the diagnostic detects an error, it executes a HALT instruction, and outputs an error message in the format:

```
---------------------------------------------------------------

    ???Error Test n subtest n problem

    problem description

    No expected/received data
          (or)
    Expected - nnnnnnnn
    Received - nnnnnnnn

---------------------------------------------------------------
```

Figure 3-3: CPU Diagnostic Error Message Format

If the CPU fails, replace the DAP module and re-run the diagnostic. If the CPU fails again, replace the MCT module. (Also see the Troubleshooting Flow, Table 3-11.)

3.2.3 Memory Diagnostic

The Memory diagnostic (EHXMS) is run to isolate a failing memory module when the operating system detects memory errors or when intermittent program failures indicate possible memory problems. The tests are described in Table 3-3.

Before running the Memory diagnostic, the CPU diagnostic should be run to verify CPU operation.

Table 3-3: Memory Diagnostic Tests

TEST	DESCRIPTION
1	CSR FUNCTION TEST -- Determines the number of CSRs present and that they set and clear correctly when the Q22-bus is initilaized.
2	MEMORY CONFIGURATION TEST -- Verifies the size of memory, memory contiguity, and the CSR/memory correlation.
3	MEMORY ADDRESS TEST PART 1 -- Memory addresses are written and verified, one longword at a time.
4	MEMORY ADDRESS TEST PART 2 -- Two's complement memory addresses are written and verified, one word at a time.

Table 3-3: Memory Diagnostic Tests (continued)

TEST	DESCRIPTION
5	MEMORY ADDRESS TEST PART 3 -- The 16 kB bank number is written and verified, one byte at a time.
6	MEMORY ADDRESS TEST PART 4 -- The two's complement 16 kB bank number is written and verified, one byte at a time.
7	WORST CASE NOISE TEST -- A series of stuck-at-0, stuck-at-1, and worst-case word parity patterns are written and verified, one word at a time.
8	MEMORY PARITY TEST -- Forced bad parity, together with a set of worst-case patterns, is written into each byte in memory. This test is executed only if the parity option is enabled, by entering an ENABLE PARITY command.
9	DATIO TEST -- Uses the Q22-bus DATIO function to write memory data, one word at a time.
10	DATIOB TEST -- Uses the Q22-bus DATIOB function to write memory data, one byte at a time.
11	INSTRUCTION EXECUTION TEST -- Executes a series of simple instruction sequences, from locations throughout memory.
12	MARCHING ONES AND ZEROS TEST -- Exercises each 16 kB memory bank by writing and reading several passes of alternating bytes of ones and zeros. Memory refresh and quadword memory references are also checked.

3.2.3.1 Running The Memory Diagnostic - The diagnostic control keys, commands, and options are described in Tables 3-4, 3-5, and 3-6.

Table 3-4: Memory Diagnostic Control Keys

KEY	DESCRIPTION
<DELETE>	Backspaces one character and deletes it. The deleted character is displayed, preceded and followed by a backslash (\).
<CTRL>U	Deletes and ignores the current line of text.
<CTRL>R	Reprints the current line of text with deleted characters and backslashes omitted.

Table 3-5: Memory Diagnostic Commands

COMMAND	DESCRITPION
HELP	Provides information about the commands.
ENABLE	Selects a command option.
DISABLE	Disables a command option.
MEMORY SIZE n	Specifies the amount of installed memory.
START n	Starts the test(s).
VIEW	Shows the status of command options.

Table 3-6: Memory Diagnostic Command Options

OPTION	DESCRIPTION
BELL	Sounds keyboard bell upon error detection. E*
ERRORS	Prints error messages upon error detection. E*
HALT	Halts the test upon error detection. E*
LOOP	Loops on test upon error detection. D*
MAP	Outputs a memory map. E*
PARITY	Enables Test 11 execution. E*
RELOCATION	Causes the diagnostic to relocate itself in memory during testing. E*
TRACE	Prints status after each test. D*

E* Default enabled.
D* Default disabled.

To run the diagnostic:

1. Insert the MICROVAX DIAGNOSTICS 1 of 3 diskette in drive 1.

2. In response to the >>> console prompt enter:

   >>> B/100 DUA1<RETURN>

3. Enter the CPU diagnostic file name when the Bootfile: prompt appears:

   Bootfile: **[SYS0.SYSMAINT]EHXMS.EXE<RETURN>**

   A header message with the diagnostic version number, and the EHXMS> prompt, will appear on the screen. Testing is continued by typing commands in response to the prompt.

4. To display status after each test, enter:

   EHXMS> **ENABLE TRACE<RETURN>**

5. Enter the memory size (in kilobytes), for example:

   EHXMS> **MEMORY SIZE 1024<RETURN>**

6. To run all the memory tests, enter:

   EHXMS> **START<RETURN>**

   There are 12 memory tests (Table 3-3). To run a particular test, enter:

   EHXMS> **START n<RETURN>**

   where n is the number of the test.

7. To get descriptions of the diagnostic commands, options, and syntax, use the HELP command:

   EHXMS> **HELP<RETURN>**

   The command options are enabled and diabled with the ENABLE and DISABLE commands. For example:

   EHXMS> **ENABLE PARITY<RETURN>**

   enables (and is required) to run the Memory Parity Test (Test 8).

   The status of the options, and the specified memory size can be displayed with the VIEW command:

```
----------------------------------------------------------

EHXMS> VIEW<RETURN>

Options status: BELL = ENABLED, ERRORS = ENABLED,
HALT = ENABLED, LOOP = DISABLED,
MAP = ENABLED, PARITY = ENABLED,
RELOCATION = ENABLED, TRACE = DISABLED

Memory size = 1024 kB

----------------------------------------------------------
```

Figure 3-4: Memory Diagnostic EHXMS View Command

8. The diagnostic will loop through the specified test(s) until stopped. To stop testing and return to the prompt, enter <CTRL>C. To exit the diagnostic press the HALT pushbutton (on the system control panel).

3.2.3.2 Memory Diagnostic Error Reporting - The diagnostic will print error messages in two formats, one for operator error (Figure 3-5) and the other fo: memory errors detected by tests (Figure 3-6).

```
------------------------------------------------------------

    EHXMS - message text

------------------------------------------------------------
```

Figure 3-5: Memory Diagnostic Operator Error Format

```
------------------------------------------------------------

    EHXMS - Error durnig test n, subtest n

    testname, subtestname

    message text

------------------------------------------------------------
```

Figure 3-6: Memory Diagnostic Memory Error Format

3.3 VDS DIAGNOSTICS

The VDS diagnostics are contained on two diskettes, as follows:

Diskette:	MICROVAX DIAGNOSTICS 2 of 3	MICROVAX DIAGNOSTICS 3 of 3
	(EHXRQ) Storage Subsystem	(EHXVS) VCB01
	(EHXDZ) DZV11	
	(EHXQN) DEQNA	

Table 3-7 is a summary of the VDS commands needed to run the diagnostics. The diagnostics are booted from console mode.

CAUTION - Console Mode

Before entering console mode, all open files should be closed, and all open accounts logged-off the system. The console interface is described in Appendix A of the VAXstation I Owner's Manual, EK-VS200-OM.

Table 3-7: VDS Command Summary

COMMAND/ QUALIFIER	DESCRIPTION
ATTACH	Defines the device to be tested, and path to the device, in the following order: 1. device type 2. link type 3. device name 4. CSR base address (octal) 5. vector address (octal) Note that every item in the list may not apply to a particular device.
DEATTACH	Used to correct ATTACH command mistakes.
HELP EHXnn	Displays information about the diagnostic, where nn identifies the specific diagnostic mnemonic.
RUN EHXnn	Loads and starts the diagnostic. (Sometimes used in place of the LOAD and START commands.)
LOAD EHXnn	Copies the diagnostic into system memory for execution.
START EHXnn	Executes the diagnostic.

Table 3-7: VDS Command Summary (continued)

COMMAND/ QUALIFIER	DESCRIPTION
/PASSES=n	Where n is the number of times the diagnostic will be run.
/SECTION=name	Where name is the specific test or section of the diagnostic selected for execution.
SET EVENT FLAG n	Where n specifies a specific test condition.
SELECT	Identifies the UUT (unit under test).

3.3.1 VCB01 Diagnostic (EHXVS)

The diagnostic comprises 14 tests/routines (described in Table 3-8). The tests are structured in nine sections; four of which are selectable (Table 3-9).

The monitor screen should be observed while the tests are running, to verify correct operation. More specifically, Tests 12, 13, and 14 require visual verification.

Error messages are displayed in standard VDS format. When there is no apparent output or activity for certain tests, the keyboard WAIT LED is turned-on, to indicate that the software is running.

Table 3-8: VCB01 Diagnostic Tests

TEST	DESCRIPTION
1	REGISTER PROBE TEST -- Performs an access test on the VCB01 I/O registers residing on the Q22-bus. The test is checking for bus time-outs resulting from the register probe.
2	BITMAP MEMORY TEST -- Performs byte, word, and longword read/write operations on the 512 kB on-board memory. Memory addressing, time-outs, and invalid memory responses are checked. using alternating ones-and-zeros data patterns.

Table 3-8: VCB01 Diagnostic Tests (continued)

TEST	DESCRIPTION
3	INTERRUPT CONTROLLER R/W -- Tests the internal functions of the Interrupt Controller chip, with interrupts turned-off at the CSR and the Interrupt Controller. (Because interrupts are turned-off, the Interrupt Controller response memory is not tested.)
4	INTERRUPT CONTROLLER INTERRUPT TEST -- An Interrupt Controller internal test, including response memory, with interrupts enabled, using fixed and rotating interrupts.
5	DUART REGISTER R/W TEST -- Tests all the internal read/write registers in UARTs A and B, using all-ones, all-zeros, and alternating ones-and-zeros data patterns.
6	DUART LOOPBACK TEST -- Using the chip's internal loopback facilities, verifies that both UARTs can transmit data at all baud rates. The patch panel and cables can be tested if an external loopback connector is used and the appropriate event flag is set.
7	DUART INTERRUPT DRIVEN LOOPBACK TEST -- Using the Interrupt Controller to drive the software, this test verifies that data can be transmitted through the DUART. The patch panel and cables will be tested if an external loopback connector is used; otherwise, only the internal loopback path will be tested.
8	CURSOR TEST -- Tests the CRTC and the Cursor RAM. Using the video readback path, the following functions are checked for valid responses: o cursor positioning o cursor RAM o cursor-generated interrupts o cursor enable/disable
9	SCAN LINE MAP TEST -- Tests each word in the Scan Line Map RAM. Data patterns are written into the RAM and verified using the video readback path.

Table 3-8: VCB01 Diagnostic Tests (continued)

TEST	DESCRIPTION
10	MOUSE COUNTER TEST -- Using exetrnal loopback connectors, the CSR, and UART B, this test forces the mouse X/Y counters to count up and down.
11	MEMORY REFRESH TEST -- Verifies the operation of the VCB01's memory refresh circuitry.
12	ODD/EVEN PIXEL GENERATOR -- Verifies the video shift registers (requires visual verification). Odd pixels should be displayed on the top-half of the screen and even pixels on the bottom-half. If half or all of the screen is blank, then a problem exists in either or both shift registers.
13	MOUSE AND KEYBOARD INTERACTIVE TEST -- Displays the pointer icon, and a test pattern comprising a square in each corner of the screen. The test also initializes the keyboard. The icon should reflect mouse movement, and a check is made to see if the returned mouse coordinates compare to the coordinates of the squares displayed on the screen. Any combination of depressed mouse buttons should display the equivalent octal code, and the code for any depressed keyboard key should be displayed.
14	ALIGNMENT PATTERN GENERATOR -- Displays the monitor alignment pattern.

Table 3-9: VCB01 Diagnostic Sections

SECTIONS	TESTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	SELECTABLE
MEMORY	X	X							X		X	X			
INTERRUPT			X	X			X			X					
DUART					X	X	X								
CURSOR								X							
MOUSE									X						
REFRESH											X				X
DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X			X
OPERATOR													X		X
ALIGN														X	X

The selectable sections (Table 3-9) are:

- DEFAULT -- This section, comprising tests 1 through 12, is run when no other section is selected. One pass takes approximately two minutes.

- REFRESH -- This section runs Test 11. If event flag 2 is set, a prompt asks for the number of seconds the test is to run, otherwise, the test runs for 20 seconds.

- OPERATOR -- This section runs Test 13. To exit the test, press either the leftmost mouse button or the keyboard <CTRL> key three consecutive times.

- ALIGN -- This section runs the alignment pattern generatot (Test 14). Pressing <CTRL>C exits the pattern and returns to the DS> prompt.

3.3.1.1 **Running The VCB01 Diagnostic** - To run the diagnostic:

1. Press the HALT pushbutton twice, to enter console mode.

CAUTION - Console Mode

Before entering console mode, all open files should be closed, and all open accounts logged-off the system. The console interface is described in Appendix A of the VAXstation I Owner's Manual, EK-VS200-OM.

2. Load the MICROVAX DIAGNOSTICS 2 of 3 diskette in drive 1.

3. Enter:

```
>>> B/10 DUA1<RETURN>
```

The VDS header should be displayed, with the DS> prompt.

4. Load the MICROVAX DIAGNOSTICS 3 of 3 diskette in drive 2.

5. Enter:

```
DS> ATTACH RX50 DUA DUA2<RETURN>
DS> SET LOAD DUA2:[SYS0.SYSMAINT]<RETURN>
DS> LOAD EHXVS<RETURN>
DS> ATTACH VCB01 HUB VCB0 777200 100<RETURN>
DS> SELECT VCB0<RETURN>
```

6. If the screen display appears to be missing pixels, the run time for the Refresh Test (Test 11) can be increased by setting event flag 2:

```
DS> SET EV 2<RETURN>
```

and responding to the number of seconds prompt with a value between 0 and 327679. Running the test for a few minutes (that is, between 150 and 300 seconds) is usually enough.

If the screen display appears to be normal, omit this step.

7. If the VCB01 is not the console device, event flag 5 must be set:

   DS> SET EV 5<RETURN>

8. Run the diagnostic, by entering:

   DS> START<RETURN>

   The diagnostic will execute the DEFAULT section.

   To run a different section, use the /SECTION qualifier, for example:

   DS> START/SECTION=ALIGN<RETURN>

   will run the alignment pattern generator (Test 14).

9. To abort testing and return to the DS> prompt, type **<CTRL>C**. To exit the test normally after completion, enter:

   DS> EXIT<RETURN>

3.3.1.2 VCB01 Diagnostic Error Messages -

[TBC...]

3.4 MONITOR LED INDICATORS

The monitor is equipped with four LEDs, located and labeled as shown in Figure 1-7. All the LEDs normally glow. With the exception of the POWER LED, a turned-off LED means that the associated signal is not present. Table 3-10 specifies the LEDs, their operation, and associated FRU.

Table 3-10: Monitor LED Description

LABEL	FRU	OPERATION
POWER	[a]	The LED is switched OFF when the Power Supply output voltage drops below its failure threshold.
VIDEO	[b]	The LED is switched OFF when the Video signal drops below its failure threshold. *
HSYNC	[b]	The LED is switched OFF when the Horizontal Sync signal drops below its failure threshold.
VSYNC	[b]	The LED is switched OFF when the Vertical Sync signal drops below its failure threshold.

[a] Power Supply

[b] Most probable failed-FRU first:

1 VCB01 Module
2 Monitor Video Module
3 Video Cable BC18T-10

* When most of the screen is black (that is, only one or two lines of text are displayed) the VIDEO LED may appear to be OFF (due to low average-video-pulse input). To verify, run the VCB01 diagnostic ALIGN section (subsection 3.3.1.1). If the LED remains OFF, replace the Video module. If the LED turns ON, there is no failure.

3.5 MONITOR ADJUSTMENT PROCEDURES

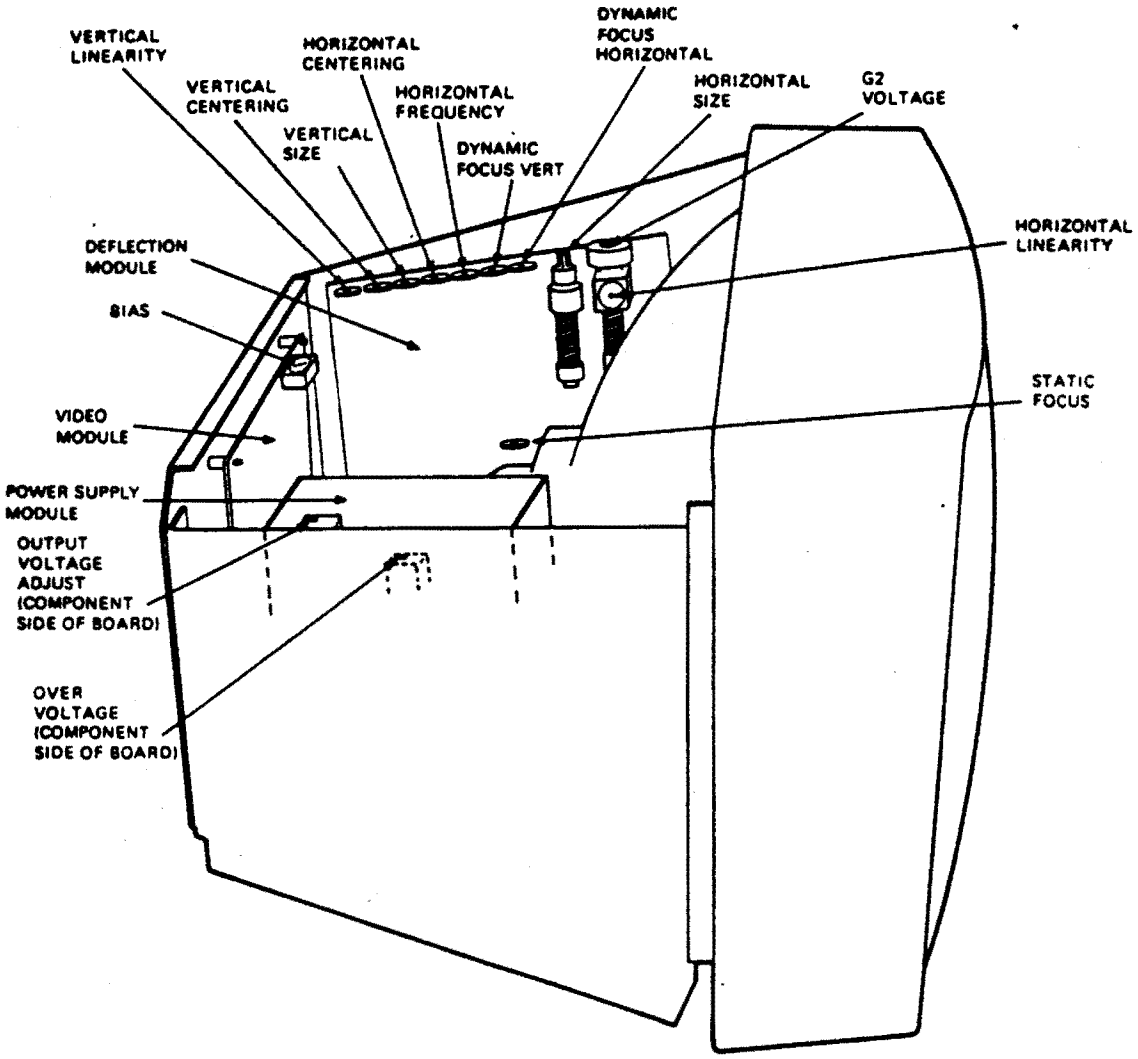


Figure 3-7: Monitor Internal Controls

3.5.1 Power Supply

1. Connect a digital voltmeter across the Power Supply output: positive test lead to the red output lead; negative test lead to ground.

2. Adjust the OUTPUT VOLTAGE control (R14) for an output of +52 Vdc +/- 0.1 Vdc.

CAUTION - Overvoltage Adjustment

DO NOT adjust the OVERVOLTAGE ADJUSTMENT control (R21). It is preset at the factory.

3.5.2 Video Module

1. Remove the video input cable from the rear panel BNC connector.
2. Set the BIAS control (R609) fully clockwise.
3. Turn up the BRIGHTNESS control (rear panel) until the raster is visible on the screen.
4. Turn BIAS control counter-clockwise until the raster brightness starts to increase. Leave at this setting.
5. Reconnect the video input cable.

3.5.3 Deflection Module

3.5.3.1 Cutoff Preset (G2 Voltage) -

1. Remove the video input cable from the rear panel BNC connector.
2. Set the BRIGHTNESS control (rear panel) to its midrange, or to the point where the raster becomes visible.
3. Adjust the CUTOFF PRESET control (R434) to the point where the raster disappears.
4. Reconnect the video input cable.

3.5.3.2 Horizontal Frequency -

1. Run the VCB01 diagnostic and select the ALIGN section (subsection 3.3.1.1):

   a. Enter console mode.
   b. Load the MICROVAX DIAGNOSTICS 2 of 3 diskette in drive 1.
   c. Enter:

      >>> B/10 DUA1<RETURN>

   d. Load the MICROVAX DIAGNOSTICS 3 of 3 diskette in drive 2.

e. Enter:

```
DS> ATTACH RX50 DUA DUA2<RETURN>
DS> SET LOAD DUA2:[SYS0.SYSMAINT]<RETURN>
DS> LOAD EHXVS<RETURN>
DS> ATTACH VCB01 HUB VCB0 777200 100<RETURN>
DS> SELECT VCB0<RETURN>
DS> START/SECTION=ALIGN<RETURN>
```

2. Turn the HORIZONTAL FREQUENCY control (R211) clockwise and counter-clockwise, noting the points where the image loses synchronization. There can be none, one, or two points of sync loss:

   a. If there is no loss of synchronization, set the HORIZONTAL FREQUENCY control to its midrange.
   b. If there is one point, set the HORIZONTAL FREQUENCY control midway between the sync loss point and the end of its range.
   c. If there are two points, set the HORIZONTAL FREQUENCY control midway between the two points.

3.5.3.3 Contrast -

1. Run the VCB01 diagnostic and select the ALIGN section (see subsection 3.3.1.1 or Horizontal Frequency adjustment, above).
2. Using the rear panel CONTRAST control, increase contrast until the horizontal crosshatch lines at the right start to distort.
3. Decrease contrast to the point where the crosshatch is not distorted and there has been a noticeable decrease in intensity.

3.5.3.4 Horizontal Size -

1. Run the VCB01 diagnostic and select the ALIGN section (see subsection 3.3.1.1 or Horizontal Frequency adjustment, above).
2. Using an alignment tool adjust the HORIZONTAL SIZE control until the image is set to a width of: 368.3 +/- 3 mm (14.5 in).

3.5.3.5 Horizontal Centering -

1. Run the VCB01 diagnostic and select the ALIGN section (see subsection 3.3.1.1 or Horizontal Frequency adjustment, above).
2. Measure and record the distance between the center left edge of the test pattern and the monitor bezel.
3. Measure and record the distance between the center right edge of the test pattern and the monitor bezel.
4. Compare the measurements of steps 2 and 3. If the difference between the two measurements is greater than 5 mm, adjust the HORIZONTAL CENTERING control until the difference is less than 5 mm.

3.5.3.6 Vertical Height -

1. Run the VCB01 diagnostic and select the ALIGN section (see subsection 3.3.1.1 or Horizontal Frequency adjustment, above).
2. Adjust the VERTICAL SIZE control until the image is set to a height of: 283.5 +/- 3 mm (11.16 in).

3.5.3.7 Vertical Centering -

1. Run the VCB01 diagnostic and select the ALIGN section (see subsection 3.3.1.1 or Horizontal Frequency adjustment, above).
2. Measure and record the distance between the center top edge of the test pattern and the monitor bezel.
3. Measure and record the distance between the center bottom edge of the test pattern and the monitor bezel.
4. Compare the two measurements of steps 2 and 3. If the difference between the two measurements is greater than 5 mm, adjust the VERTICAL CENTERING control until the difference is less than 5 mm.

3.5.3.8 Horizontal And Vertical Linearity -

1. Run the VCB01 diagnostic and select the ALIGN section (see subsection 3.3.1.1 or Horizontal Frequency adjustment, above).
2. Check that all vertical lines in the test pattern are equidistant across the screen.
3. If not, adjust the VERTICAL LINEARITY control (R318) until the vertical lines are equidistant.

NOTE

Exact equidistance may not be possible. In that case, adjust for the best possible pattern.

4. Check that all horizontal lines of the test pattern are equidistant across the screen.
5. If not, adjust the HORIZONTAL LINEARITY control (L232) until all horizontal lines are equidistant (see the note above).
6. Recheck the horizontal and vertical size, and horizontal and vertical centering. There will be some interaction between these adjustments -- readjust if necessary.

3.5.3.9 Static And Dynamic Focus -

1. Run the VCB01 diagnostic and select the ALIGN section (see subsection 3.3.1.1 or Horizontal Frequency adjustment, above).
2. Adjust the STATIC FOCUS control (R431) for a sharp image at the screen center. Individual pixels should be distinguishable.
3. Adjust the HORIZONTAL DYNAMIC FOCUS control (R418) for a sharp image at the right and left edges of the screen.
4. Adjust the VERTICAL DYNAMIC FOCUS control (R416) for a sharp image at the top and bottom of the screen edges.
5. Visually check the entire image for center, horizontal, and vertical focus quality. If necessary, repeat steps 2, 3, and 4.

3.6 TROUBLESHOOTING FLOW

The following notes apply to the Troubleshooting Flow (Table 3-11):

- The answer to any procedure decision is either the next line, or a branch to another step
- The => ("arrow") is read as: "go to step."

For example:

STEP	PROCEDURE/DECISION	BRANCH
START	Turn system power ON.	
	Does the system bootstrap?	N => 1
	Is the system operating reliably?	N => 20
	DONE	

If the answer to: "Does the system bootstrap?" is no (N), branch to step 1 (N => 1); if yes (Y), take the next line: "Is the system operating reliably?" If that answer is no, branch to step 20 (N => 20); if yes, you are done.

- Microverify error numbers displayed in the CPU patch panel segmented-LED display, are valid only when the CPU is in console Halt mode (the >>> console prompt is displayed on the monitor screen).

Table 3-11: Troubleshooting Flow

STEP	PROCEDURE/DECISION	BRANCH
START	Turn system power ON.	
	Does system bootstrap?	N => 1
	Is the system operating reliably?	N => 20
	DONE	
1	Is DC OK LED ON?	N => 2
	"MICROVERIFY STARTED" displayed on monitor?	N => 8
	Garbled or no monitor display?	Y => 10
	Error number in Microverify LED display?	Y => 14
	Error message dispalyed on monitor?	Y => 19
		N => 20
2	Is AC power switch lighted?	N => 3
	Both fans turning?	N => 4
	Turn power OFF.	
	Remove all modules except CPU.	
	Turn power ON.	
	Is DC OK LED ON?	N => 5
	a) Turn power OFF.	
	b) Re-install one module in backplane.	
	c) Turn power ON.	
	d) Is DC OK LED ON?	N => 6
	Repeat a), b), c) until d) = NO	
3	Check: AC wall receptacle	
	AC power cord	
	AC circuit breaker	
	Power-on switch	
	AC power switch	
4	Possibly power supply and/or fan.	
	Replace fan; or	
	Replace H7864 power supply.	
	Return to START	
5	Replace H7864 power supply.	
	Return to START	
6	Replace failed module.	
	Is DC OK LED ON?	N => 7
	Return to START	

Table 3-11: Troubleshooting Flow (continued)

STEP	PROCEDURE/DECISION	BRANCH
7	Power supply +5 Vdc and +12 Vdc outputs OK?	N => 5
	Possibly faulty LED or cable. Replace DC OK LED; or Replace Front Control Panel cable. Return to START	
8	Microverify LED display = 6 or 7?	N => 7 or 10
	HALT light ON?	N => 9
	Press HALT button (to release it). Return to START	
9	Replace DAP. If error still present, replace MCT. Return to START	
10	VCB01 Display Density switches set OK?	Y => 11
	Set: E68 = ON E48 S8 = OFF	
	Return to START	
11	Run VCB01 diagnostic. VCB01 passes diagnostic.	Y => 12
	Replace VCB01 Return to START	
12	Possibly faulty cable. Replace BC18T-10 video cable. Problem resolved?	N => 13
	Return to START	
13	Possibly monitor problem. Repair/replace monitor. Return to START	
14	LED = 6 or 7?	Y => 8
	LED = 5?	Y => 15
	LED = 4?	Y => 16
	LED = 3?	Y => 17
		N => 19

Table 3-11: Troubleshooting Flow (continued)

STEP	PROCEDURE/DECISION	BRANCH
15	Replace MCT Return to START	
16	Check DAP to MCT interconnect cable seating. If seated OK: replace DAP; then MCT; then cable. Return to START	
17	Can deposit/examine any memory location? Error message on monitor?	N => 18 Y => 19 N => 20
18	Possibly MCT or memory. Replace MCT; then first MSV11-QA. Return to START	
19	LED = 2 or 1? Is one of following error messages true? DEVICE IS NOT PRESENT DEVICE IS OFFLINE NO VALID ROM IMAGE FOUND BOOT DEVICE I/O ERROR FAILED TO INITIALIZE BOOT DEVICE NO RESPONSE FROM LOAD SERVER MEMORY INITIALIZATION ERROR Do all the following check OK? Named valid boot device? Bootable media is in boot device? Fixed-disk is ready? Boot device installation is OK? System configuration is correct? Grant continuity is OK? Switch and jumper settings are correct? Cable connections are OK? Correct configuration and re-boot. Return to START	N => 20 N => 24 Y => 22

Table 3-11: Troubleshooting Flow (continued)

STEP	PROCEDURE/DECISION	BRANCH
20	Boot diagnostic diskette. Will Macroverify or other diagnostics load?	N => 27
	Load and Run Macroverify. Did Macroverify find failed FRU?	N => 21
	Replace FRU. Return to START	
21	Run applicable device diagnostic. Replace FRU. Return to START	
22	Will any (other) device boot?	N => 23
	Replace boot unit, then RQDX1. Return to START	
23	Possible interrupt or Q22-bus fault. Replace DAP for interrupt fault. Replace MCT or backplane for Q22-bus fault. Return to START	
24	Is following error message true?	Y => 27
	UNEXPECTED SCB EXCEPTION OR MACHINE CHECK	
	Is one of following error messages true?	N => 2?
	NO VALID BOOT DEVICE IS PRESENT IN THE CONFIGURATION NONE OF THE BOOTABLE DEVICES CONTAIN A PROGRAM IMAGE PROGRAM IMAGE NOT FOUND INVALID BOOT DEVICE FILE STRUCTURE PROGRAM IMAGE FILE NOT CONTIGUOUS FILE CHECKSUM ERROR BAD FILE STRUCTURE HEADER BAD VOLUME DIRECTORY INVALID PROGRAM IMAGE FORMAT PREMATURE END OF FILE UNEXPECTED EXCEPTION AFTER STARTING PROGRAM IMAGE	
	Suspect media. Try to boot from another media. Return to START	

Table 3-11: Troubleshooting Flow (continued)

STEP	PROCEDURE/DECISION	BRANCH
25	Is following error message true? INVALID FILENAME Re-enter correct filename. Return to START	N => 26
26	Is following error message true? PROGRAM IMAGE DOES NOT FIT IN AVAILABLE MEMORY More physical memory is required for this boot. Return to START	N => 27
27	FATAL SYSTEM ERROR. Possible multiple failures. The following sequence is recommended: a) Reduce system to minimum configuration: o CPU o MSV11-QA (1) o RQDX1 o RX50 o VCB01 b) Follow troubleshooting flow from START. c) Replace failed unit. d) Re-install other FRUs, one-at-a-time. e) Verify each re-installed unit, by repeating steps b) through d).	

CHAPTER 4

REPLACEMENT

This chapter lists the procedures for removing and replacing failed FRUs in a desk-top system. With the exception of cover removal, the same procedures apply to floor-stand and rack-mounted systems. Table 4-1, at the end of this chapter, is a list of replacement part numbers.

4.1 BACKPLANE MODULES

The general procedure for removing/replacing modules plugged into the backplane is the same for all modules.

4.1.1 Module Removal

1. Turn-off system and monitor power.
2. Remove the system ac power cord from the wall receptacle.

3. Remove the system unit rear cover, by grasping each end and pulling the cover toward you (Figure 4-1).

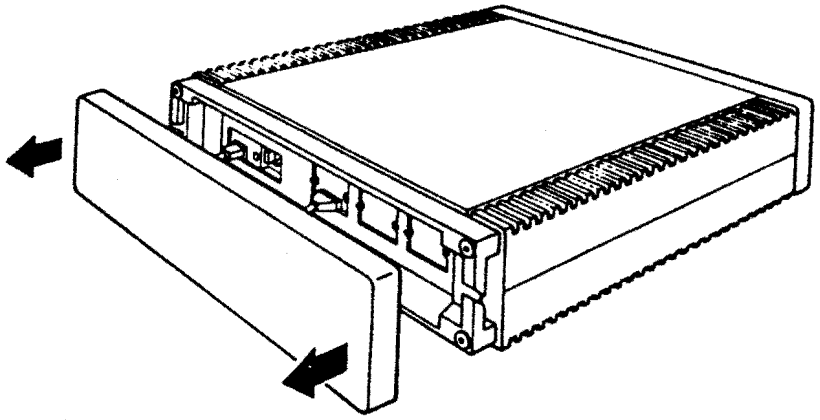


Figure 4-1: Rear Cover Removal

4. Note the position of any external cables connected to the Patch and Filter Panel assembly. Remove the cables (Figure 4-2).

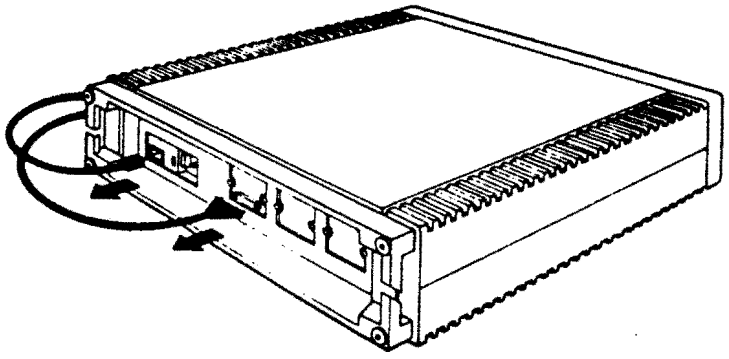


Figure 4-2: Rear Cable Removal

5. Loosen the two captive screws on the left end of the Patch and Filter Panel assembly, and swing it open (Figure 4-3).

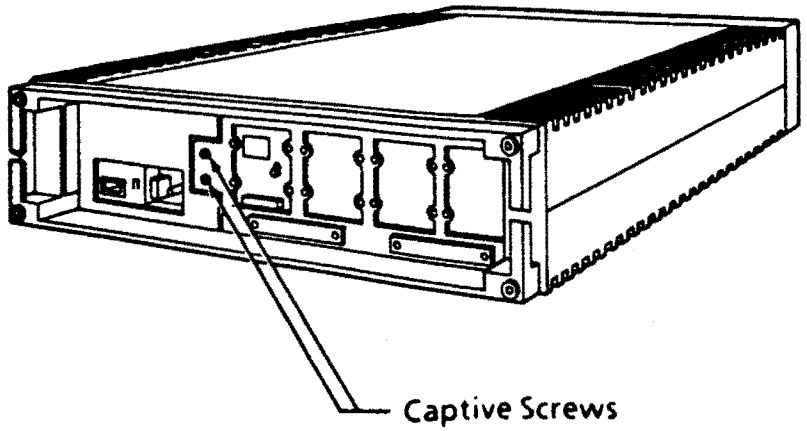


Figure 4-3: Patch and Filter Panel Assembly Access

6. Note the location of the module to be replaced, and the position of any cables connected to the module.

7. Disconnect any cables connected to the module (Figure 4-4). Note: the module may first have to be partially withdrawn, before the cable(s) can be removed.

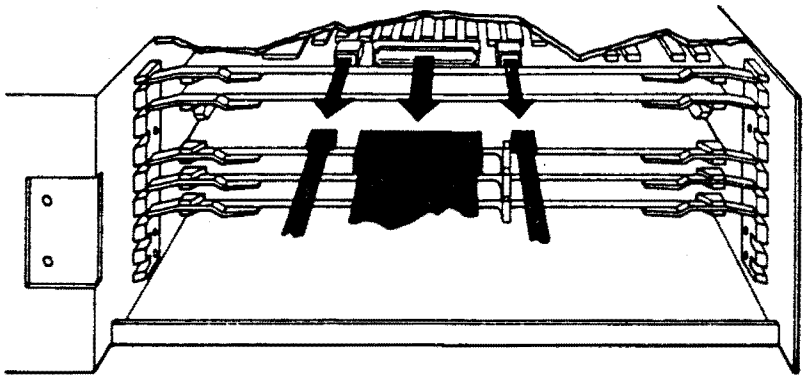


Figure 4-4: Module Cable Removal

8. Pull the levers at each end of the module to release it, and carefully pull the module toward you (Figure 4-5).

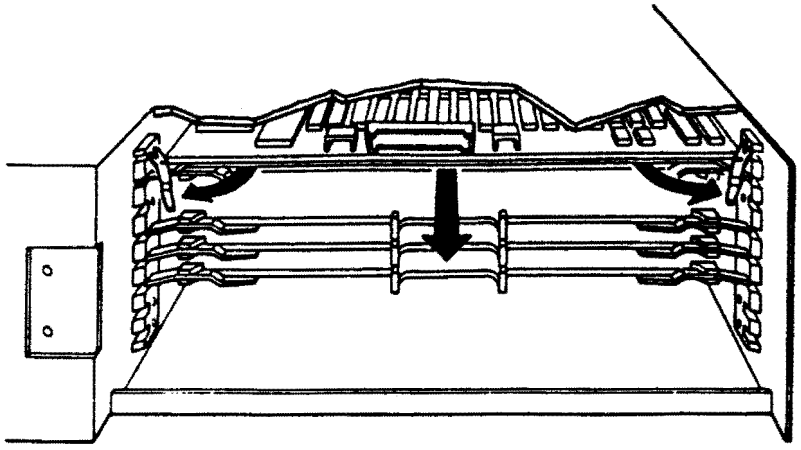


Figure 4-5: Module Removal

9. Note the settings of any switches and jumpers on the removed module.

4.1.2 Module Replacement

1. Normally, switches and jumpers on the replacement module should be set to the same position as those on the removed module. (Also see Chapter 1.)

2. Make sure the locking levers at each end of the module are in the released position.

3. Slide the module partially into the slot, and reconnect any cables removed from the old module (Figure 4-6).

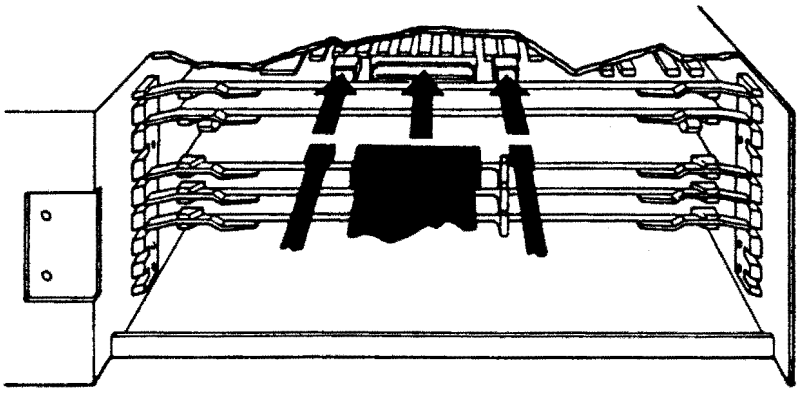


Figure 4-6: Module Cable Replacement

4. Slide the module into the slot until firmly seated, and close the locking levers (Figure 4-7).

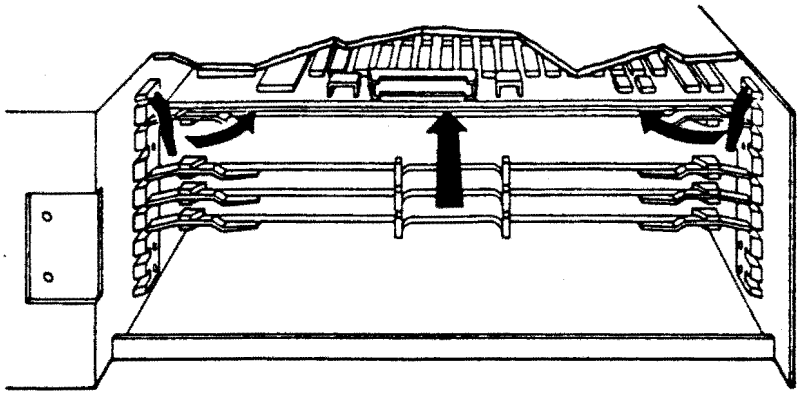


Figure 4-7: Module Replacement

5. Close the Patch and Filter Panel assembly, and refasten the two captive screws.

6. Reconnect any removed cables to the Patch and Filter Panel assembly.

7. Replace the rear cover.

8. Turn-on system and monitor power. Microverify should run.

9. Run Macroverify.

4.2 STORAGE SUBSYSTEM

This procedure describes removal/replacement of the RD52 and RX50 drives.

4.2.1 Access

1. Turn-off system and monitor power.

2. Remove the system ac power cord from the wall receptacle.

3. Remove the system unit rear cover, by grasping each end and pulling the cover toward you (Figure 4-1).

4. Remove the system unit front cover, by grasping each end and pulling the cover toward you (Figure 4-8).

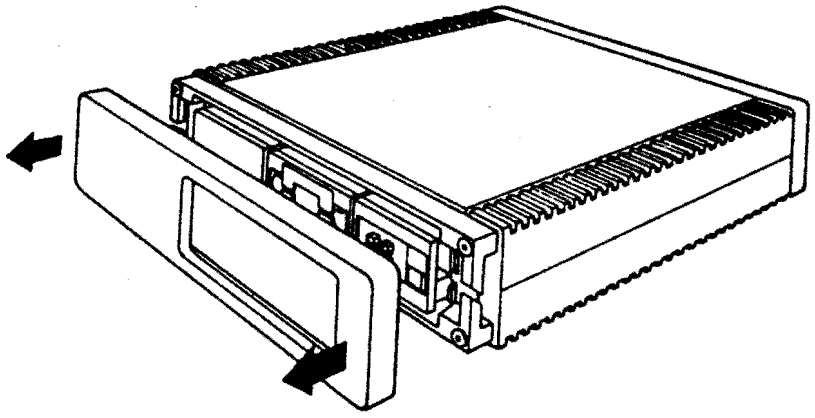


Figure 4-8: Front Cover Removal

5. Remove the front chassis retaining bracket by removing the screws that secure it to the enclosure (Figure 4-9).

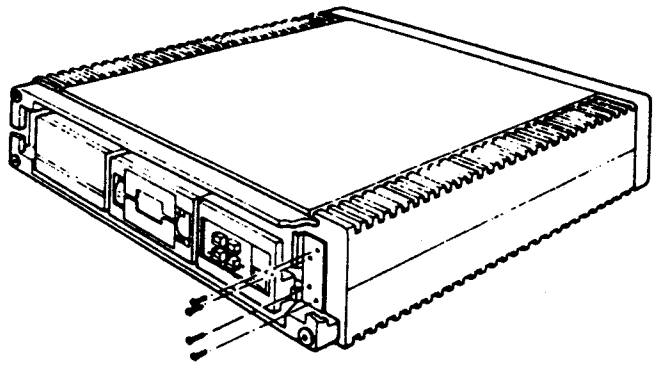


Figure 4-9: Front Bracket Removal

6. Make sure there is enough slack in the cables connected to the back of the system unit, and slide the system unit out of the enclosure until restrained by the stopper on the chassis.

7. Remove the storage subsystem cover (Figure 4-10).

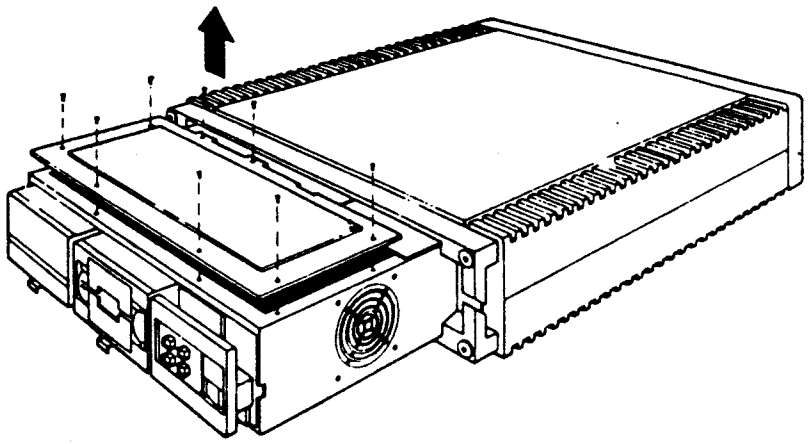


Figure 4-10: Storage Subsystem Cover Removal

4.2.2 RD52 Removal

CAUTION - RD52

Use extreme care when handling the RD52 drive. It will be damaged by sudden physical shocks (such as dropping it on a hard surface). A shipping case is required to protect the drive in transit.

CAUTION - Head Positoner Flag

When handling the drive, do not hold the front, right-hand side of the drive; doing so will cause the head positioner flag to rotate (Figure 4-11).

1. Push down the release tab, and slide the drive forward to access the cables at the rear of the drive (Figure 4-11).

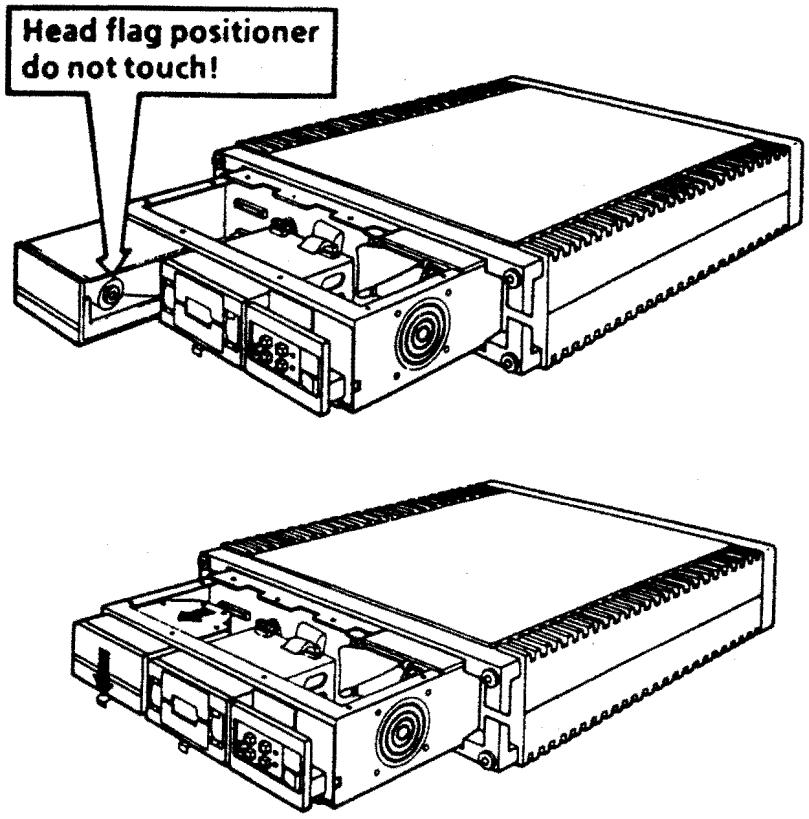


Figure 4-11: RD52 Cable Access

2. Disconnect the dc power and two signal cables from the drive (Figure 4-12).

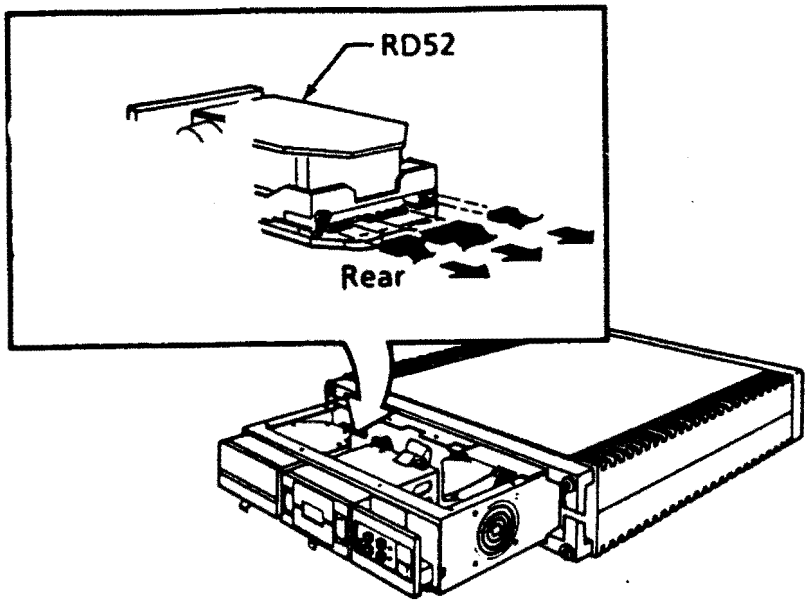


Figure 4-12: RD52 Cable Removal

3. Remove the drive from the chassis by sliding it forward. Observe the previous head positioner flag caution (Figure 4-11).

4. Replace the red plastic cover on the head positioning arm (Figure 4-13). (This cover should have reen removed and taped to the top of the drive during installation.)

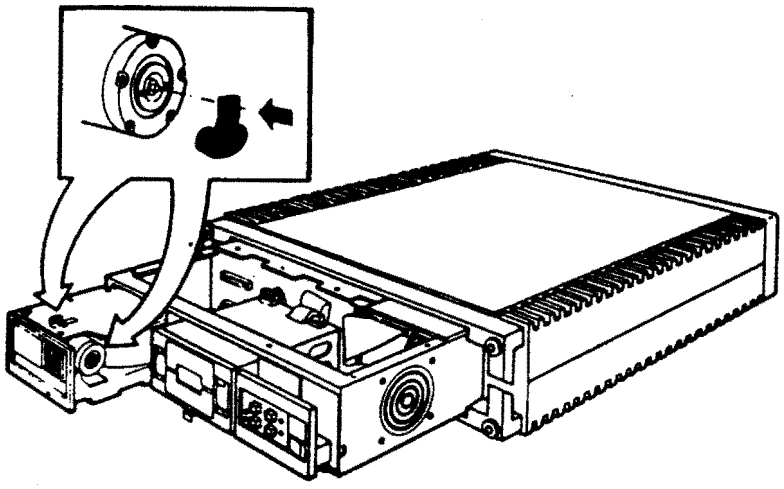


Figure 4-13: RD52 Head Positioning Arm Cover Replacement

5. Pack the removed drive in its special shipping case (Figure 4-14).

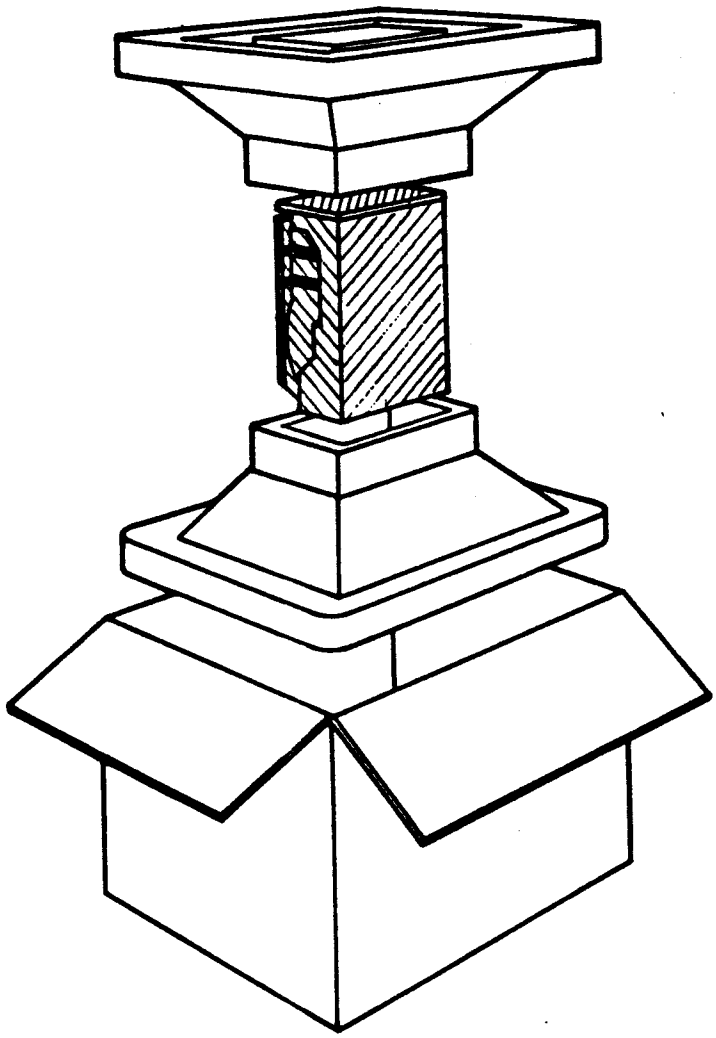


Figure 4-14: RD52 Shipping Container

4.2.3 RD52 Replacement

1. Unpack the replacement drive.

2. Set the DIP switches as shown in Figure 4-15.

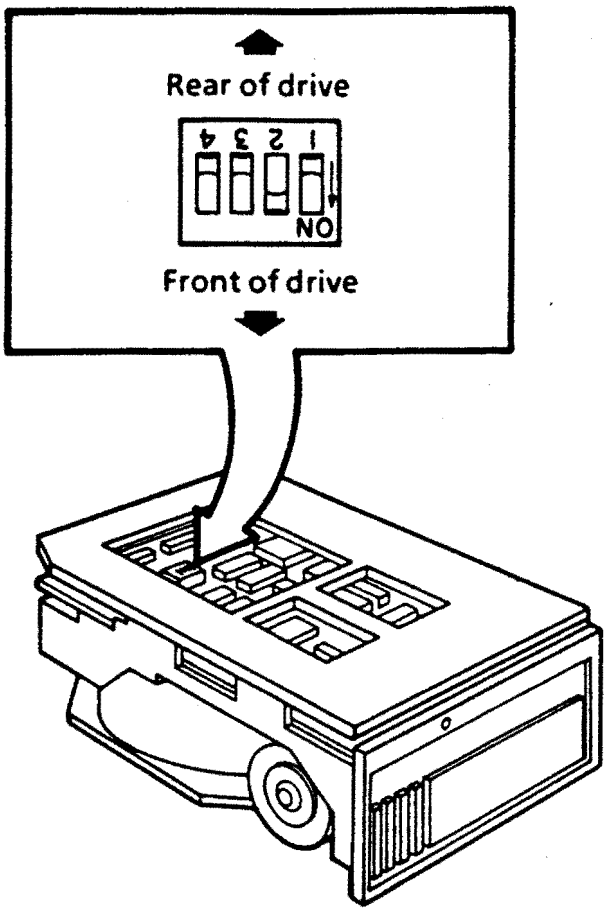


Figure 4-15: RD52 DIP Switches

3. Remove the red plastic cover on the head positioning arm and tape it to the top of the drive (Figure 4-16).

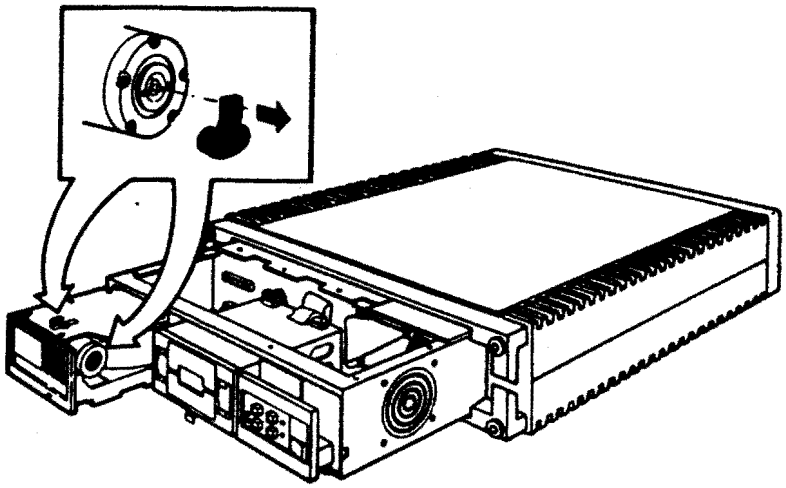


Figure 4-16: RD52 Head Positioning Arm Cover Removal

4. Slide the drive most of the way into the chassis, leaving enough room to reconnect the cables (Figure 4-17). Push on the front corners of the drive. Observe the head positioner flag caution.

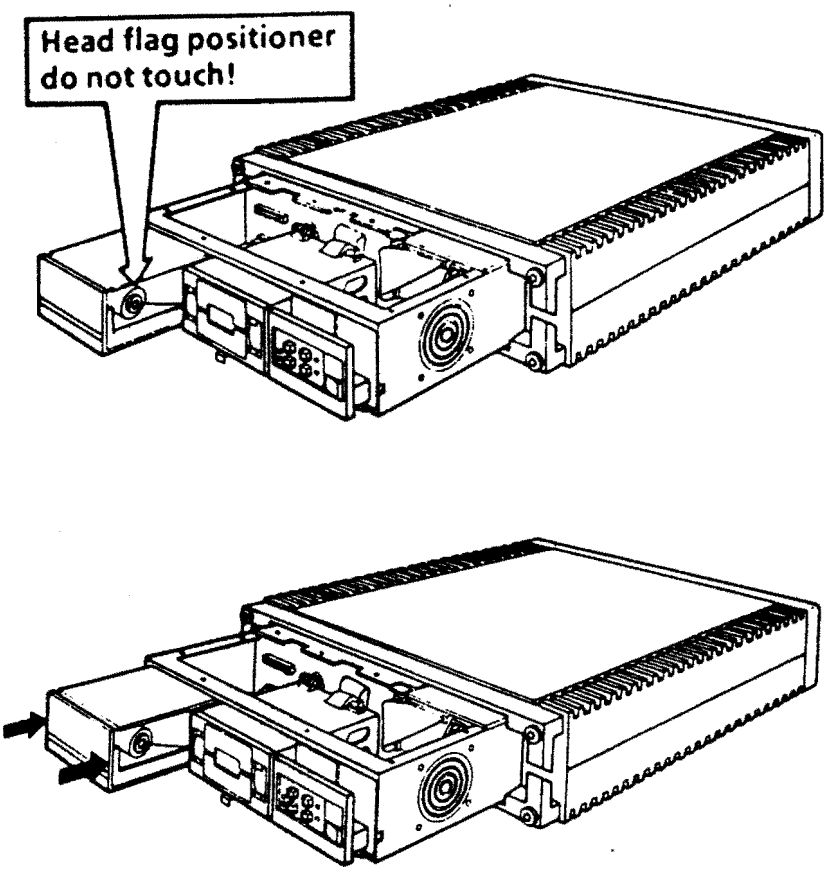


Figure 4-17: RD52 Insertion

5. Connect the dc power and two signal cables (Figure 4-18). Push the drive into the chassis until it latches.

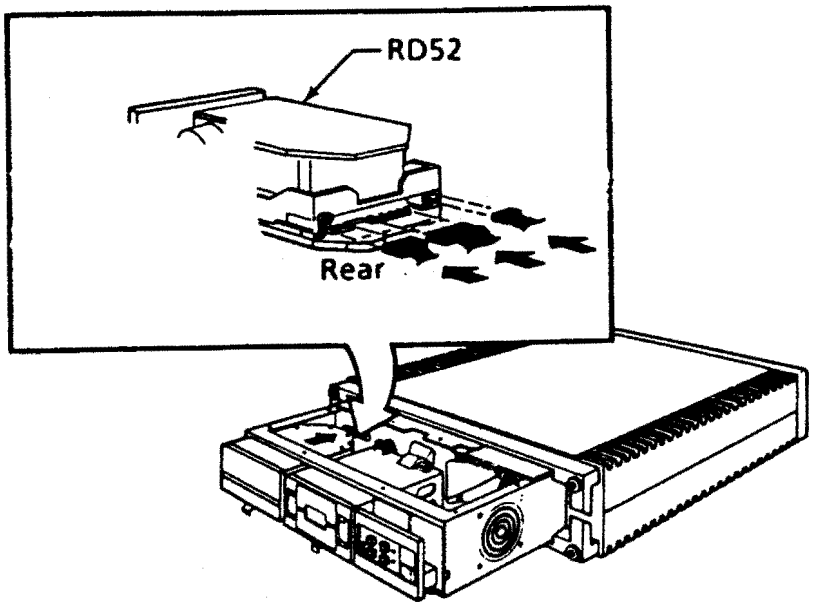


Figure 4-18: RD52 Cable Connection

6. Replace the storage subsystem cover.
7. Push the system unit all the way into the enclosure.
8. Replace the front chassis retaining bracket.
9. Replace the front cover.
10. Reformat the disk (see Chapter 8 in the VAXstation I Owner's Manual, EK-VS200-OM).
11. Turn-on system and monitor power. Microverify should run.
12. Run Macroverify.

4.2.4 RX50 Removal

1. Slide the drive forward to access the cables at the rear of the drive, and disconnect the dc power cable and signal cable (Figure 4-19).

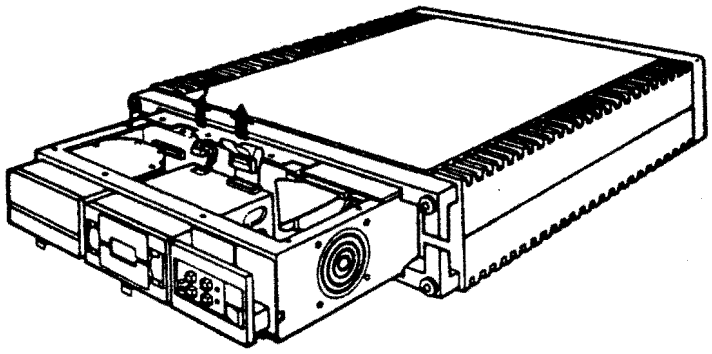


Figure 4-19: RX50 Cable Access

2. Push down the release tab, and slide the drive forward and out (Figure 4-20).

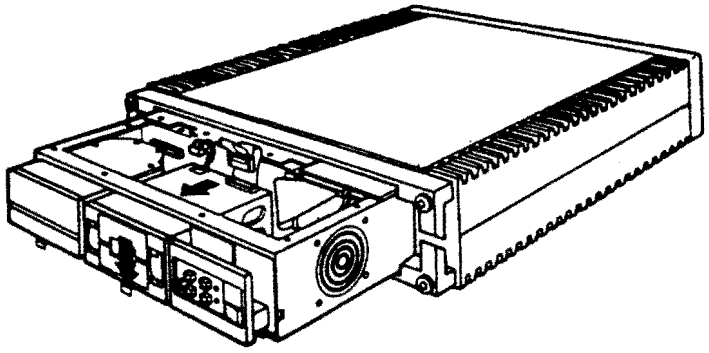


Figure 4-20: RX50 Removal

4.2.5 RX50 Replacement

1. Slide the drive into the chassis to reconnect the dc power and signal cables (Figure 4-21).

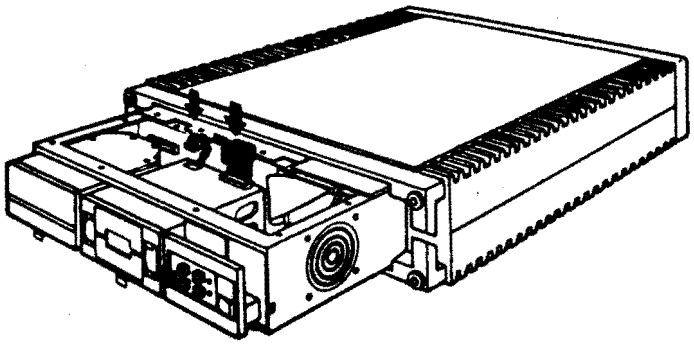


Figure 4-21: RX50 Cable Connection

2. Push the drive all the way into the chassis.
3. Replace the storage subsystem cover.
4. Push the system unit all the way into the enclosure.
5. Replace the front chassis retaining bracket.
6. Replace the front cover.
7. Turn-on system and monitor power. Microverify should run.
8. Run Macroverify.

4.3 POWER SUPPLY

The power supply is not adjustable and does not contain any FRUs; it is an FRU.

4.3.1 Power Supply Removal

1. Turn-off system and monitor power.
2. Remove the system ac power cord from the wall receptacle.
3. Remove the system unit front cover and rear cover. Grasp each end of the cover and pull the cover toward you (Figures 4-1 and 4-8).
4. Note the position of any external cables connected to the Patch and Filter Panel assembly. Remove the cables (Figure 4-2).
5. Remove the rear chassis retaining bracket on the rear, left side of the system unit.
6. Slide the system unit out of the enclosure.
7. Remove the storage subsystem cover (Figure 4-10).
8. Loosen the two captive screws on the Patch and Filter Panel assembly (Figure 4-3).

9. From the front of the power supply, disconnect (Figure 4-22):

   a. J7 -- 6-pin, keyed, locking ac power connector.
   b. J8 -- 9-pin mass storage power connector.
   c. J9 -- 18-pin backplane power connector.
   d. J10 -- 4-pin, in-line, keyed, locking fan power connector.

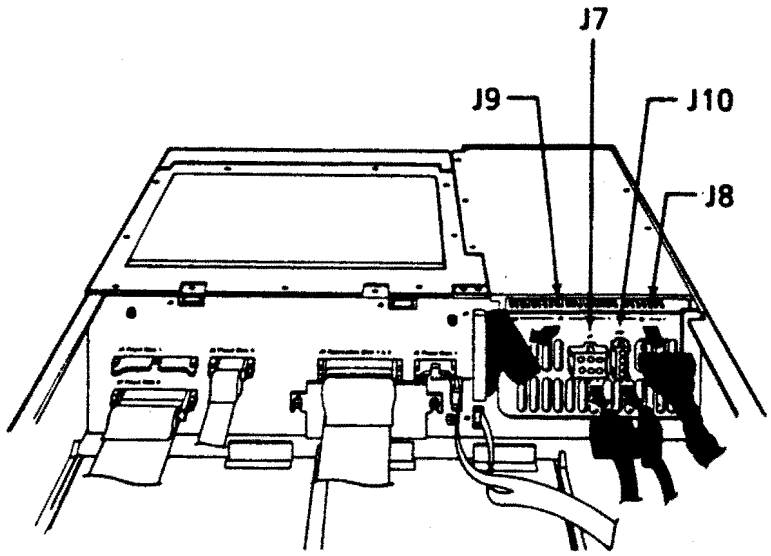


Figure 4-22: Power Supply Cable Removal

10. Remove the five screws that hold the power supply to the chassis.

11. Carefully lift the power supply and rest it on the cover of the backplane modules.

12. Disconnect the rear cooling fan power connector.

4.3.2 Power Supply Replacement

1. Rest the power supply on the cover of the backplane modules, and reconnect the rear cooling fan power connector.

CAUTION - Fan Power

The polarized, dc power connector to the cooling fan must be installed with the curve of the connector matching the curve of the fan housing, for correct fan rotation (Figure 4-23).

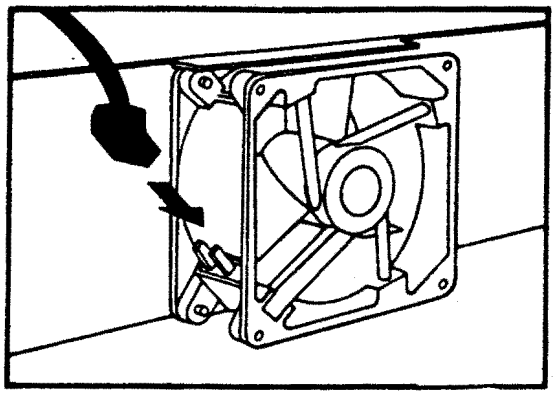


Figure 4-23: Fan Power Connector

2. Place the power supply in positon, making sure that the rear fan power cable is routed over the top of the fan.

3. Insert the five power supply hold-down screws.

4. On the front of the power supply, reconnect (Figure 4-22):

   a. J7 -- 6-pin, keyed connector.
   b. J8 -- 9-pin connector.
   c. J9 -- 18-pin connector.
   d. J10 -- 4-pin, keyed connector.

5. Refasten the Patch and Filter Panel assembly captive screws.

6. Replace the storage subsystem cover.

7. Make sure that the voltage selector switch is set for local requirements.

8. Slide the system unit into the enclosure.

9. Install the rear chassis retaining bracket.

10. Reconnect any removed cables to the Patch and Filter Panel assembly.

11. Replace the front and rear covers.

12. Turn-on system and monitor power. Microverify should run.

13. Run Macroverify.

4.4 BACKPLANE AND SIGNAL DISTRIBUTION PANEL

4.4.1 Backplane Removal

1. Turn-off system and monitor power.

2. Remove the system ac power cord from the wall receptacle.

3. Remove the system unit front cover and rear cover. Grasp each end of the cover and pull the cover toward you (Figures 4-1 and 4-8).

4. Note the position of any external cables connected to the Patch and Filter Panel assembly. Remove the cables.

5. Remove the rear chassis retaining bracket on the rear, left side of the system unit.

6. Slide the system unit out of the enclosure.

7. Remove the storage subsystem cover (Figure 4-10).

8. Remove the backplane modules cover.

9. Loosen the two captive screws on the Patch and Filter Panel assembly and swing it open (Figure 4-3).

10. Remove the backplane modules as described in subsection 4.1.1, steps 6, 7, and 8.

11. Without disconnecting the cables from the drives, remove the disk drives, following the procedures described in subsection 4.2.2, steps 1 and 3, and subsection 4.2.4, steps 1 and 2. The drive cables are disconnected from the backplane (Figure 4-24):

    a. J6 -- RX50 signal cable
    b. J2 -- RD52 signal cable
    c. J7 -- RD52 signal cable

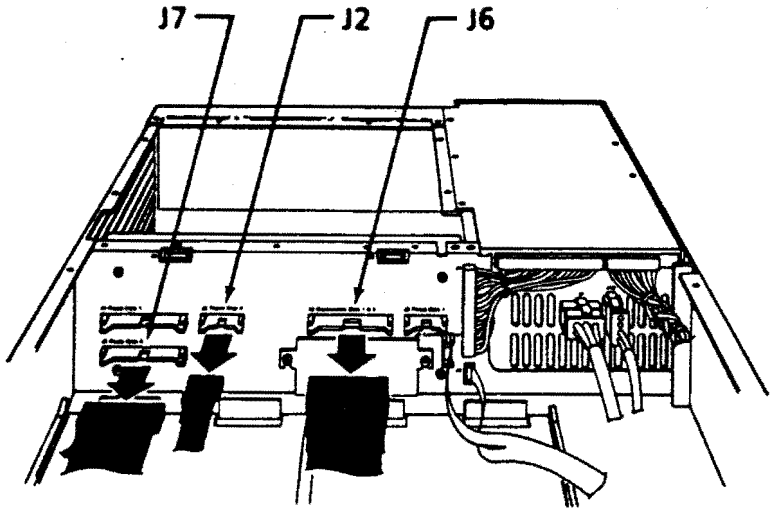


Figure 4-24: Drive Cable Backplane Connectors

12. Remove the following cables (Figure 4-25):

    a. J1 -- Power supply cable
    b. J2 -- 10-pin connector
    c. J4 -- 10-pin connector

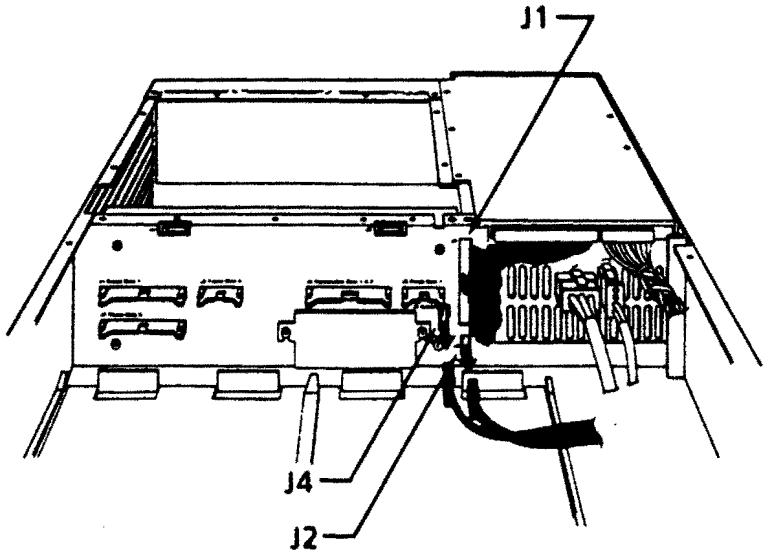


Figure 4-25: Other Backplane Cable Connectors

13. To remove the Q22-bus cable connected to the signal distribution panel, loosen the two screws holding the cover and lide the cover off. Remove the cable (Figure 4-26).

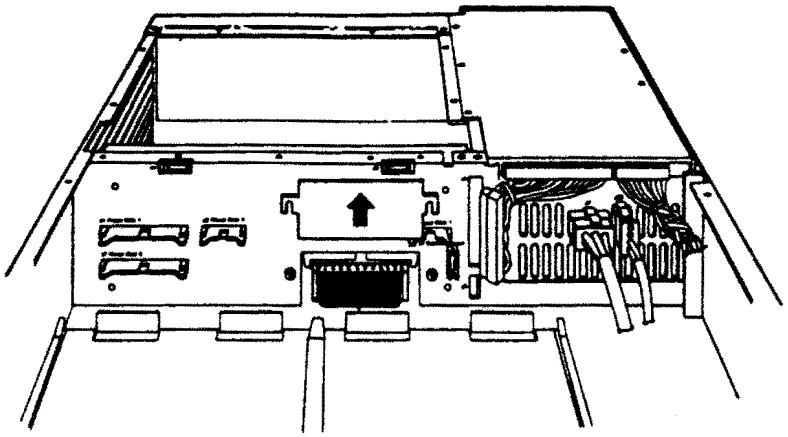


Figure 4-26: Q22-bus Cable Backplane Connector

14. Remove the four screws holding the backplane assembly to the chassis.

15. Pivot the C/D interconnect side of the backplane 45 degrees (toward the Patch and Filter Panel assembly). Remove the backplane assembly from the chassis by lifting it straight up.

16. Remove the signal distribution panel from the backplane by removing four screws.

4.4.2 Backplane Replacement

1. Install the signal distribution panel on the backplane with four screws.

2. Install the backplane assembly with four screws.

3. Reconnect the Q22-bus cable (Figure 4-26) and install the cover.

4. Reconnect (Figure 4-25):

   a. J1 -- Power supply cable
   b. J2 -- 10-pin connector
   c. J4 -- 10-pin connector

5. Replace the disk drives as described in subsection 4.2.3, steps 3 and 5, and subsection 4.2.5, steps 1 and 2.

6. Making sure that the connectors (Figure 4-24) are properly aligned, reconnect:

   a. J6 -- RX50 signal cable
   b. J2 -- RD52 signal cable
   c. J7 -- RD52 signal cable

7. Re-install the backplane modules as described in subsection 4.1.2, steps 2, 3, and 4.

8. Refasten the Patch and Filter Panel assembly captive screws.

9. Replace the backplane modules cover.

10. Replace the storage subsystem cover.

11. Slide the system unit into the enclosure.

12. Install the rear chassis retaining bracket.

13. Reconnect any removed cables to the Patch and Filter Panel assembly.

14. Replace the front and rear covers.

15. Turn-on system and monitor power. Microverify should run.

16. Run Macroverify.

4.5 COOLING FANS

4.5.1 Rear Fan Removal

1. Turn-off system and monitor power.
2. Remove the system ac power cord from the wall receptacle.
3. Remove the system unit front cover and rear cover. Grasp each end of the cover and pull the cover toward you (Figures 4-1 and 4-8).
4. Note the position of any external cables connected to the Patch and Filter Panel assembly. Remove the cables (Figure 4-2).
5. Remove the rear chassis retaining bracket on the rear, left side of the system unit.
6. Slide the system unit out of the enclosure.
7. Remove the power supply as described in subsection 4.3.1, steps 7 through 12.
8. Remove the four screws and spacers holding the fan to the chassis; lift the fan and guard from the chassis.

4.5.2 Rear Fan Replacement

1. Place the four fan mounting screws in the chassis holes.

2. Place the guard over the screws, with the circular wires of the guard against the chassis (Figure 4-27).

3. Place the four spacers over the screws.

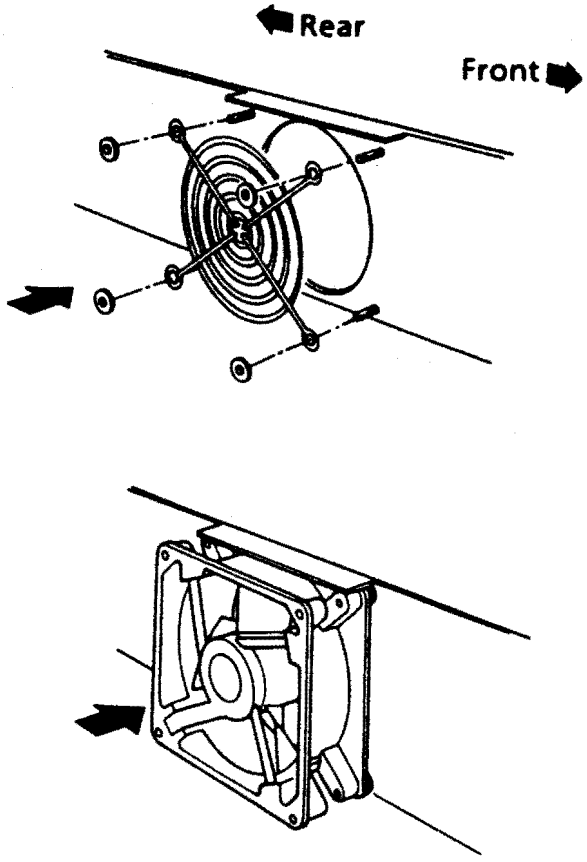


Figure 4-27: Rear Fan Installation

4. Fasten the screws to the fan. The fan must be placed such that airflow is away from the power supply.

5. Reconnect the rear cooling fan power connector.

CAUTION - Fan Power

The polarized, dc power connector to the cooling fan must be installed with the curve of the connector matching the curve of the fan housing, for correct fan rotation (Figure 4-23).

6. Replace the power supply as described in subsection 4.3.2, steps 2 through 7.

7. Slide the system unit into the enclosure.

8. Install the rear chassis retaining bracket.

9. Reconnect any removed cables to the Patch and Filter Panel assembly.

10. Replace the front and rear covers.

11. Turn-on system and monitor power. Microverify should run.

12. Run Macroverify.

4.5.3 Front Fan Removal

1. Turn-off system and monitor power.

2. Remove the system ac power cord from the wall receptacle.

3. Remove the system unit front cover, by grasping each end and pulling the cover toward you (Figure 4-8).

4. Remove the front chassis retaining bracket by removing the screws that secure it to the enclosure.

5. Make sure there is enough slack in the cables connected to the back of the system unit, and slide the system unit out of the enclosure until restrained by the stopper on the chassis.

6. Remove the storage subsystem cover (Figure 4-10).

7. Remove the RX50 as described in subsection 4.2.4, steps 1 and 2.

8. Disconnect the power cord from J10 (Figure 4-28).

9. Remove the four screws and spacers holding the fan to the chassis; lift the fan and guards from the chassis.

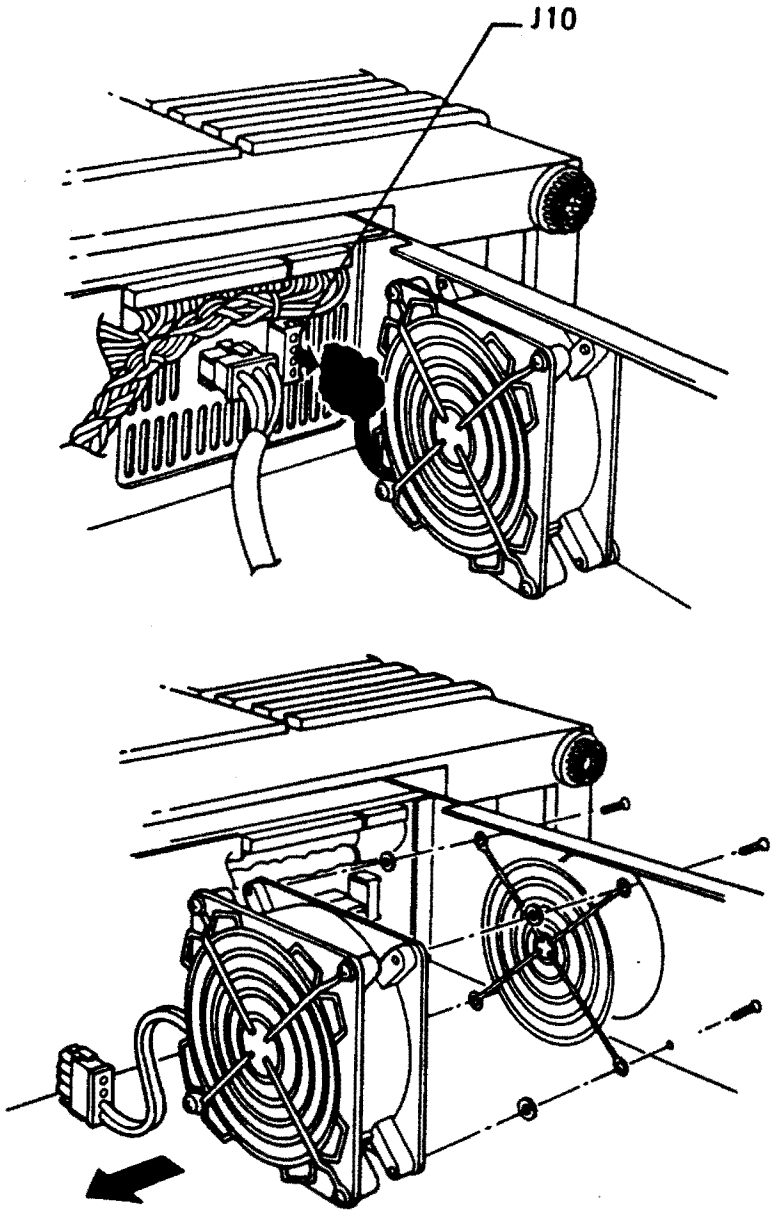


Figure 4-28: Front Fan Removal

4.5.4 Front Fan Replacement

1. Remove the power cable and fan guard from the intake side of the removed fan and fit them to the replacement fan.

CAUTION - Fan Power

The polarized, dc power connector to the cooling fan must be installed with the curve of the connector matching the curve of the fan housing, for correct fan rotation (Figure 4-23).

2. Place the four fan mounting screws in the chassis holes.
3. Place the guard over the screws, with the circular wires of the guard against the chassis (Figure 4-29).
4. Place the four spacers over the screws.

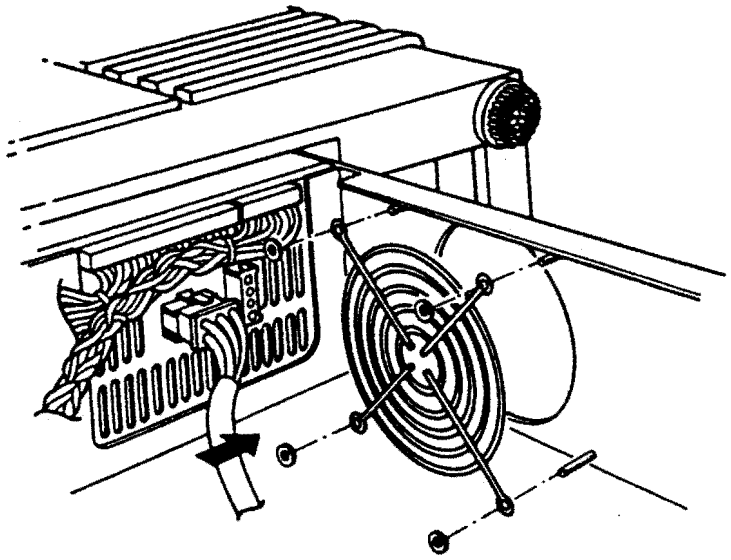


Figure 4-29: Front Fan Installation

5. Fasten the screws to the fan. The fan must be placed such that airflow is away from the power supply.
6. Reconnect the fan power cable to J10.

7. Install the RX50 drive as described in subsection 4.2.5, steps 1 and 2.

8. Replace the storage subsystem cover.

9. Slide the system unit into the enclosure.

10. Install the front chassis retaining bracket.

11. Replace the front cover.

12. Turn-on system and monitor power. Microverify should run.

13. Run Macroverify.

4.6 PATCH AND FILTER PANEL

4.6.1 Insert Removal

1. Turn-off system and monitor power.

2. Remove the system ac power cord from the wall receptacle.

3. Remove the system unit rear cover, by grasping each end and pulling the cover toward you (Figure 4-1).

4. Note the position of any external cables connected to the Patch and Filter Panel assembly. Remove the cables.

5. Loosen the two captive screws on the left end of the Patch and Filter Panel assembly, and swing it open (Figure 4-3).

6. Note the position of any internal cables connected to the Patch and Filter Panel assembly insert. Remove the cables.

7. Remove the four screws holding the insert to the Patch and Filter Panel assembly. Remove the insert.

4.6.2 Insert Installation

1. Using four screws, fasten the insert to the Patch and Filter Panel assembly.
2. Connect the internal cables to the insert.
3. Refasten the Patch and Filter Panel assembly captive screws.
4. Reconnect any removed cables to the Patch and Filter Panel assembly.
5. Replace the rear cover.
6. Turn-on system and monitor power. Microverify should run.
7. Run Macroverify.

4.7 FRONT CONTROL PANEL

4.7.1 Control Panel Removal

1. Turn-off system and monitor power.
2. Remove the system ac power cord from the wall receptacle.
3. Remove the system unit front cover. Grasp each end of the cover and pull the cover toward you (Figure 4-8).
4. Remove the four screws from the front of the control panel assembly.

5. Remove the connector from the control panel printed circuit board (Figure 4-30).

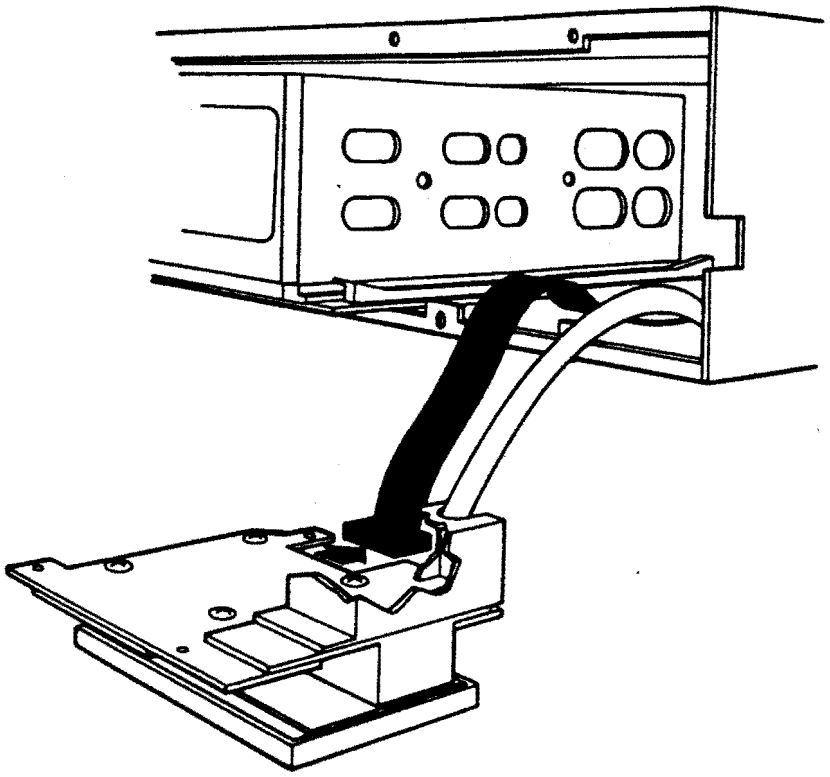


Figure 4-30: Front Control Panel Removal

6. Remove the four screws that hold the control panel assembly together (Figure 4-31).

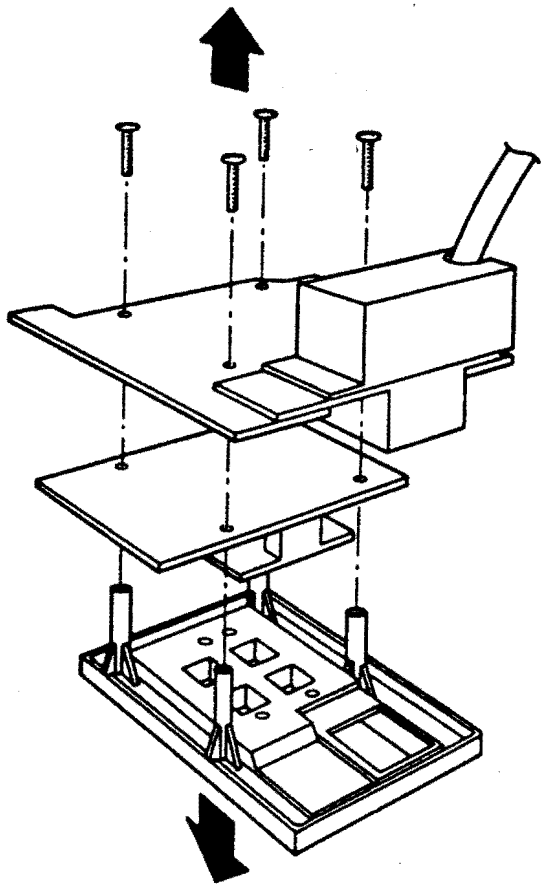


Figure 4-31: Front Control Panel Disassembly

4.7.2 Control Panel Replacement

1. Using the LEDs to correctly position the assembly, refasten the four screws that hold the assembly together.
2. Reconnect the control panel cable.
3. Remount the panel with four screws.
4. Replace the front cover.

5. Turn-on system and monitor power. Microverify should run.

6. Run Macroverify.

4.8 MONITOR

4.8.1 Monitor Cover Removal

1. Place the monitor on its CRT face on a level work surface.

WARNING - CRT Face

The integral CRT bezel is designed to keep the CRT face above the work surface; however, the work surface under the CRT face should be clear of any debris. In addition, it is recommended that rough work surfaces be covered to prevent any unnecessary scratches on the bezel.

2. To remove the tilt-swivel base from the monitor cover, remove the four mounting feet from the monitor. The mounting feet are finger tight.
3. Remove the four philips-head screws from the rear of the cover.
4. Lift the cover off the monitor compartment.

4.8.2 EMI Screen

WARNING - CRT Neck

With the EMI screen removed, the neck of the CRT is exposed and can be broken. Be very careful when removing modules or passing tools over the monitor compartment.

1. With the cover removed, place the monitor in its normal viewing position.
2. Loosen the six screen hold-down screws.
3. Remove the EMI screen.

4. When installing the screen, be sure that each slot of the screen flange is under its associated hold-down screw.
5. Tighten the hold-down screws.

4.8.3 Monitor Power Supply

1. Remove the two connectors on the Power Supply assembly.
2. Loosen the four philips-head mounting screws (right side panel, viewed from rear).
3. Remove the assembly by working the mounting screws through the elongated mounting holes.
4. To install the assembly, reverse the previous steps.

4.8.4 Deflection Module

1. Remove the four module connectors.
2. Loosen the four philips-head module mounting screws (left side panel, viewed from rear).
3. Remove the module by working the mounting screws through their elongated mounting holes.
4. To install the module, reverse the previous steps.

4.8.5 Video Module

1. Remove the four module connectors.
2. Loosen the four philips-head mounting screws on the rear panel.
3. Remove the module by working the mounting screws through their elongated mounting holes.

CAUTION

Be careful not to entangle any module component on the CRT cable, or bend/break the LEDs of the module assembly.

4. To install the module, reverse the previous steps, observing the previous caution.

4.8.6 CRT Cable

1. Remove the CRT cable connector from the Video Module.
2. Slide the quick-disconnect spade and pin of the cable from the Video Module.
3. Slide the quick-disconnect spade from the grounding lug.
4. Disconnect the CRT socket and remove the cable from the compartment.
5. To install the cable, reverse the previous steps.

4.8.7 Monitor Cover Replacement

1. Place the monitor on its CRT face.

WARNING - CRT Face

The integral CRT bezel is designed to keep the CRT face above the work surface; however, the work surface under the CRT face should be clear of any debris. In addition, it is recommended that rough work surfaces be covered to prevent any unnecessary scratches on the bezel.

2. Place the cover over the compartment; be sure that the cover edge fits into the CRT bezel assembly.
3. Insert and tighten the four philips-head mounting screws on the rear of the cover.
4. Hold the tilt-swivel base, with the lever pointed down, against the monitor bottom.
5. Align the base and monitor mounting holes, and replace and tighten the monitor feet.
6. Place the monitor in its normal viewing position.

Table 4-1: Part Numbers

DESCRIPTION		PART NUMBER
KD32-AB	Module, Data Path	M7135-YA
	Module, Memory Controller	M7136
	F11 MMU	21-15542-01
	Cable, LED and Baud Rate	BC22K-1C
	Cable, DAP - MCT	70-18448-00
	Cable, Patch Panel	70-11411-1C
	Insert, Patch Panel	70-21150-01
MSV11-QA	Module, 1 MB Memory	M7551-AA
RQDX1	Module, Disk Controller	M8639
	Cable, RD/RX Data	BC06L-1C
RD52	Drive, 30 MB Winchester	RD52
	Cable, Data - 20 Conductor	17-00282
	Cable, Data - 34 Conductor	17-00286
RX50	Drive, Diskette	RX50-AA
	Cable, Data	17-00285-02
RD/RX	Cable, Power	70-20435-1K
VCB01	Module, Video Controller	M7602
	Cable, Monitor/Keyboard (Video)	BC18T-10
	Insert, Patch Panel	70-21495-01
VR100	Monitor	VR100-AA
	Power Supply	29-24782
	Board, Video	29-24783
	Board, Deflection	29-24784
	Assembly, CRT Socket	29-24785
	Assembly, Control Bracket	29-24789
	Cable, Video - Deflection	29-24786
	Cable, Power Supply - Video	29-24787
	Cable, Power Supply - Deflection	29-24788
	Alignment Wrench	29-23190
	Alignment Ruler	29-24868

Table 4-1: Part Numbers (continued)

DESCRIPTION		PART NUMBER
H7864	Power Supply	30-21794-01
	Fan, 12 Vdc	12-17556-01
H9278-A	Backplane Assembly	70-19986
Keyboard		LK201-CA
Mouse		30-20038-01
Jumper	Two-position	12-18783
DEQNA	Module, Ethernet Controller	M7504
	Cable, Patch Panel	[TBS]
	Insert, Patch Panel	[TBS]
H4000	Transceiver	[TBS]
	Cable, Transceiver	[TBS]
DZV11	Module, Async. Line Multiplexer	M7957
	Cable, Patch Panel	[TBS]
	Insert, Patch Panel	[TBS]
LA50	Printer	[TBS]
LA100	Printer	[TBS]
	Cable, Printer - SLU	BC22D-10

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