DEC-14-HGZB-D

pdp14

MAINTENANCE MANUAL

digital equipment corporation · maynard. massachusetts

1st Edition March, 1970
2nd Edition July, 1972

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INTRODUCTION

This manual contains instructions and drawings for maintaining the PDP-14 Programmable Controller manufactured by Digital Equipment Corporation, Maynard, Massachusetts. The manual is organized into four chapters for various levels of maintenance personnel.

Chapter 1 provides a brief description and specifications for the PDP-14 and is designed to give the reader a first level introduction to the system.

Chapter 2 presents the first level maintenance philosophy and procedures to be used by maintenance personnel assigned to the machine. The techniques described are those of module swapping which, when systematically performed, will correct most problems.

Chapters 3 and 4 are intended to be used by highly trained and qualified maintenance personnel. Chapter 3 explains the theory of operation and Chapter 4 outlines techniques to be used for fault isolation on a particular module.

REFERENCES

For additional information concerning the PDP-14, the PDP-14/L, or system-related equipment, refer to the following DEC publications:

PDP-14 Reference Card
PDP-14 User's Manual
Control Handbook
Small Computer Handbook

SOFTWARE DOCUMENTATION

The following diagnostic documentation is also provided by DEC:

TEST-14, MAINDEC-14-D7AB-D: This document contains the program listing for TEST-14 plus instructions for using the diagnostic program and interpreting its results. TEST-14 performs a comprehensive test of the PDP-14 Processor, Input Boxes, and Output Boxes.

TEST-14/L, MAINDEC-14-D7LA-D-(D): Same as TEST-14 except for PDP-14/L.

ABE-14, MAINDEC-14-D8AB-D: This document contains the program listing and instructions for loading, running, and interpreting the results of ABE-14. ABE-14 is a diagnostic program for testing PDP-14 and PDP-14/L Accessory Boxes.

VER-14, MAINDEC-14-D1AB-D: This document contains the program listing and instructions for using VER-14. VER-14 is a program that verifies the contents and operation of a Read-Only Memory (ROM).

LOAD-14, DEC-14-LZPB-D: This document contains the program listing and instructions for LOAD-14. LOAD-14 is used to enter a ROM program into the computer memory for verification by VER-14.

ROL-14, DEC-14-MWZC-PB: This document contains the program listing and instructions for using the ROL-14 program. ROL-14 is an interrogation and control program that can be used with an on-line system for diagnostic tests.

MAINTENANCE PHILOSOPHY

This manual contains two levels of maintenance instructions. The first level, designated **User Maintenance**, is presented in Chapter 2 and is intended primarily for end user maintenance personnel. However, it should also be used as the first level of maintenance for DEC Field Service personnel. This level of maintenance assumes the user is familiar with industrial control systems and basic electrical repair techniques but may not be familiar with programmable controllers.

There are two primary divisions of user maintenance; one for fault isolation using module substitution techniques and a second for using computer diagnostics. In either case, only module replacement is recommended; repair of the modules should only be attempted by qualified personnel.

Detailed Maintenance is the second level of maintenance and is intended only for DEC Field Service personnel or user personnel thoroughly trained in electronic repair (and soiid-state digital repair techniques). This level is intended primarily for module repair and is presented in Chapter 4.

CHAPTER 1
GENERAL INFORMATION

1.1 GENERAL

This chapter defines the purpose of the PDP-14 Controller, lists typical system applications, and describes the major elements of the controller. A summary of equipment specifications is also included at the end of the chapter.

1.2 SYSTEM DESCRIPTION

1.2.1 Purpose and Use

The PDP-14 Controller replaces conventional relay control systems in virtually all types of industrial applications requiring high-reliability control operations. Typical uses include the PDP-14 as the controller for:

- Transfer and assembly lines
- Machine tool systems
- Packaging and materials handling systems
- Chemical mixing systems
- Elevator control systems

The PDP-14 can control any operation or process sequence that comprises discrete steps and involves on/off status inputs and on/off control outputs. The controller can be used in a stand-alone application or can be used with a computer in a monitoring application or an interactive application.

1.2.2 Stand-Alone Applications

When used in a stand-alone or independent application (Figure 1-1), the PDP-14 controls the machine or process system operating sequence using a program in its Read-Only Memory (ROM). This program establishes the control relationships between status inputs and control outputs. Status inputs are provided as on/off inputs from machine system pushbutton switches, limit switches, etc. The program continually tests the status inputs (and outputs) and, based upon the results, advances the control sequence by turning outputs (to solenoids, motor starters, etc.) on or off.

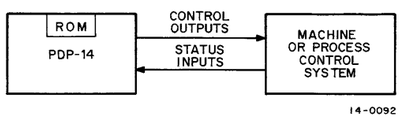


Figure 1-1 Stand-Alone Application

In a stand-alone application, the PDP-14 can accept up to 256 status inputs and can control up to 255 outputs.

1.2.3 Monitoring Applications

The PDP-14 can be connected to a small, general purpose computer such as the PDP-8/E for monitoring (Figure 1-2). The PDP-14 still performs control functions as described in Paragraph 1.2.2; however, it also reports status information to the PDP-8/E. The PDP-8/E analyzes this data to determine if the machine is working properly and/or stores production information (e.g., piece counts, cycle times, scheduled tool changes, etc.).

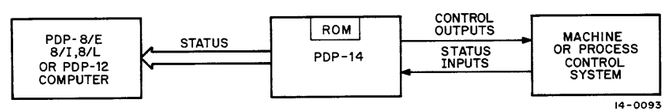


Figure 1-2 Monitored Application

In other applications, the PDP-14 does not control machine operation (this function is provided by relays or other control systems). Instead, the PDP-14 acts as an interface for the computer and tests inputs from the machine in an order defined by a ROM program (or by the computer) and provides the test results to the computer. Since the PDP-14 does not control any outputs in this application, it can be configured to accept up to 512 discrete status inputs.

1.2.4 Interactive Applications

The PDP-14 can also be used with a small, general purpose computer in an interactive application (Figure 1-3). In this application, the PDP-14 can provide the fundamental control for the machine and return status information to the computer. The computer can then direct the control in the PDP-14 based upon the status information provided by the PDP-14 or upon other information available to the computer (such as analog signals from a measuring device).

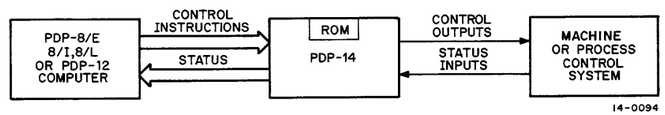


Figure 1-3 Interactive Application

1.2.5 Operating Concepts

The controller directs the machine or process system sequence by solving input/output relationships, using a program (a method or procedure for solving a problem) stored in its memory. Basically, this program defines what outputs are to be turned on or off (and in what order or sequence) and what combinations of inputs (and outputs) are to effect an output. In other words, the controller controls the machine or process system sequence by solving input/output equations.

The controller cannot directly react to an input (or output) change of state (on-to-off or off-to-on). Therefore, it must test the pertinent inputs (and outputs) many times a second and it must define the pertinent state of the test. With each test, the controller must decide whether to turn an output on or off before continuing the testing procedure. Following a valid test decision, the controller turns the output on or off, then continues testing.

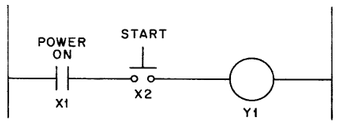
The above operations are all performed as discrete steps of a program. The smallest part of a program is called an instruction. The instruction is stored in a discrete memory location called an address. It defines a single step or action to be performed. The controller uses three basic types of instructions: Test, Decision, and Operate. A Test instruction defines the input (or output) to be tested and the applicable state (on or off). A Decision instruction links the Test instructions with other Test instructions or with the Operate instructions. That is, for a valid decision, either an Operate instruction can be performed to turn an output on or off, or another Test instruction can be performed.

The basic logic operators (AND and OR) for solving input/output equations are inherent in the arrangement of the Test, Decision, and Operate instructions. The following example defines one way the controller might solve an input/output equation.

Assume a machine motion requires two inputs; for example, POWER ON and START. If POWER ON is represented as X1 (input 1), START as X2 (input 2), and the machine motion as Y1 (output 1), then:

Y1 = X1 * X2, where * signifies both inputs are needed concurrently; i.e., a logical AND function.

The "ladder diagram" for the above example is shown at the right.



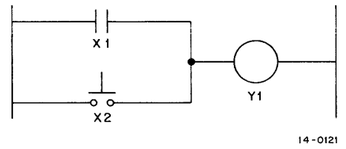
For solution of this equation, the controller could test input X1 for an on condition. It could then examine the test result with a Decision instruction. If X1 is off, there is no need to test input X2; therefore, the controller can continue the program by testing other equations. Input X1 would then be tested again on the next complete cycle through memory. If, however, X1 is on, the Decision instruction could link the program to a Test instruction for X2. This Test instruction could then be followed with another Decision instruction. If X2 is off, the controller returns to other testing. If X2 is on, however, the program is linked to an Operate instruction that turns on output Y to cause machine motion.

NOTE
Inputs are always identified with the letter X; outputs are always identified with the letter Y.

A logical OR function could be represented as follows:

Y1 = X1 + X2, where + signifies that either input (or both) can activate an output; i.e., a logical OR function.

The "ladder diagram" for the above example is shown at the right.



For solution of this equation, both inputs need be tested only if the one checked first is off. Each Test instruction could be linked to an Operate instruction (using a Decision instruction) if either input is on.

The PDP-14 Controller has the capabilities for checking inputs (or outputs) for either an on or off state. In addition, there are other instructions to control sequences. Therefore, the control programs can be written in a number of ways.

To summarize, a typical PDP-14 control program is made up of a series of instructions that are stored in a Read-Only Memory (ROM). These instructions can be arranged in groups as shown in Figure 1-4. Each group of instructions solves a Boolean equation by testing specific PDP-14 inputs and outputs and, at the end of the test, turns an output either on or off.

The final instruction in the program is an unconditional jump instruction. This instruction returns the PDP-14 to the first instruction in the program and the program execution cycle is repeated. Thus, the PDP-14 control program consists of a closed loop of instructions which are executed every 15 to 60 milliseconds (the actual execution time is dependent on the number of instructions in the program).

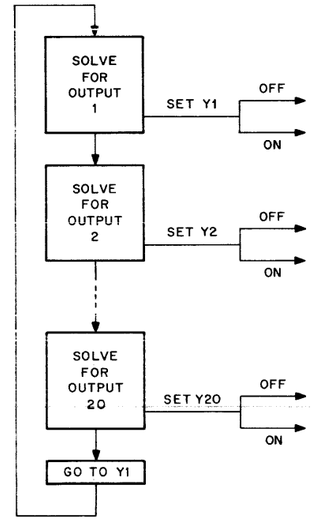


Figure 1-4 PDP-14 Program Execution Cycle

1.3 EQUIPMENT DESCRIPTION

1.3.1 General

A PDP-14 Controller comprises the four major assemblies that are identified in Figure 1-5. Figure 1-6 depicts the functional relationships of the major assemblies that are described in subsequent paragraphs.

In a typical control application, the PDP-14 Controller consists of a Control Unit, a Read-Only Memory (ROM), Input (I), Output (O), and Accessory (A) Boxes. The Control Unit is fundamentally the heart of the controller. It directs and coordinates the overall operation from manual control inputs, the stored program, input (or output) test results, or information supplied by a computer. The ROM stores the program for evaluating status inputs and controlling a machine or process system. An I Box converts machine or process system inputs into signals usable by the controller. Similarly, O Boxes convert controller outputs into signals usable by the machine or process system. Accessory (A) Boxes provide timer functions, storage functions during normal operation, and special storage functions during power-off conditions.

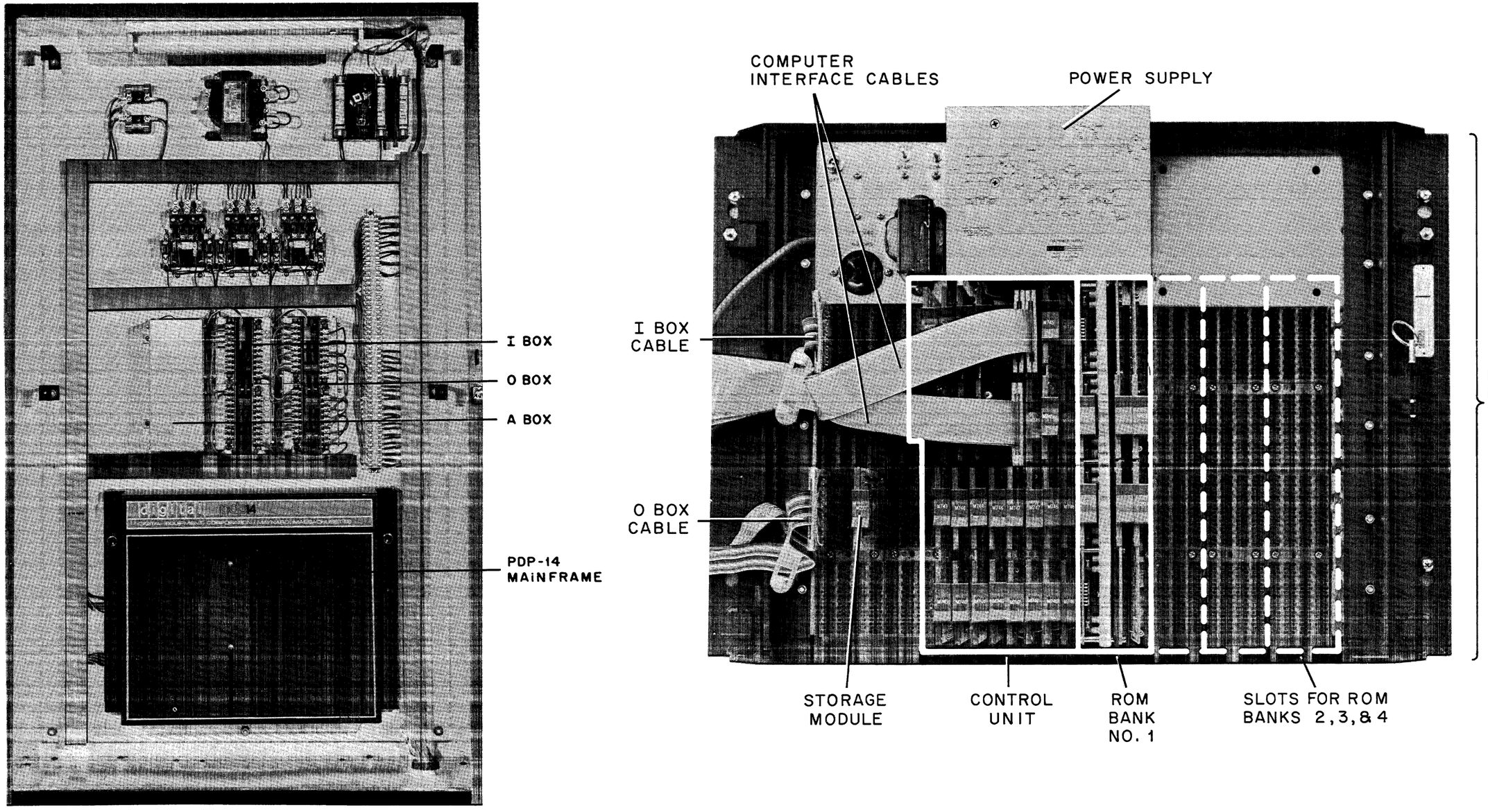


Figure 1-5 Typical PDP-14 Control System

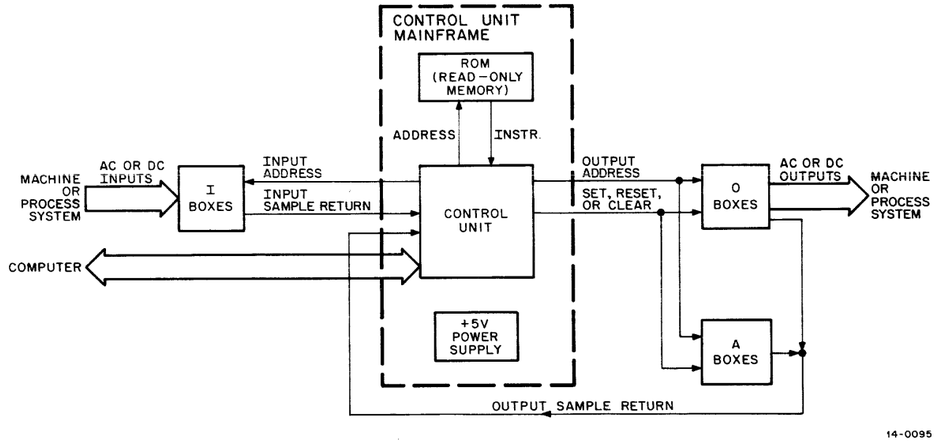


Figure 1-6 PDP-14 Control System

1.3.2 Control Unit Mainframe

The control unit mainframe consists of a heavy steel frame that is hinged to a mounting base frame (Figure 1-5). The mainframe contains a low-voltage power supply (or supplies), module sockets for Control Unit and Read-Only Memory (ROM) logic, and module sockets for Input (I) Box, Output (O) Box, and Accessory (A) Box connectors.

1.3.2.1 **Power Supply Filter Assembly** – This assembly contains an input power terminal strip, a utility receptacle, an ON/OFF switch, and a 2A line fuse. The assembly also contains two manual control switches. The START/STOP switch, as the name implies, starts or stops the controller's timing circuits. The CONTINUE switch allows the controller to resume operation at the point it was stopped. In contrast, a start operation causes the program to begin at its initial step. These manual switches are not used during normal operation or troubleshooting.

1.3.2.2 **Power Supply** – The +5V power supply provides the operating potential for logic circuit operation. The supply operates from a 105 to 125 Vac (or 210 to 250 Vac), 47 to 500 Hz source. It provides a nominal +5 Vdc at 7A. The power supply is short-circuit proof and provides over-load protection for logic circuits.

Two power supplies are required for controller configurations having load currents in excess of 7A. These supplies are connected in parallel as shown in Figure 1-7.

1.3.2.3 **Read-Only Memory** – The PDP-14 Memory stores a program that defines the machine system operating sequence. The memory is termed "read-only" because it cannot be altered electrically (i.e., written on).

A machine program consists of many discrete steps called instructions. Each instruction is stored in a discrete ROM location called an address and is retrieved (fetched) from memory by Control Unit action. When executed by the Control Unit, an instruction causes the controller to perform a single action such as testing an input or turning on an output.

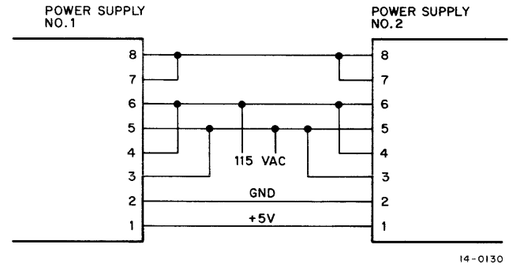


Figure 1-7 Power Supply Connections

The ROM is a passive device; i.e., it provides an instruction only when requested by the Control Unit. In its maximum configuration, the ROM provides the capability for storing up to 4096 instructions; therefore the Control Unit must be capable of addressing 4096 locations.

The ROM is not interchangeable with ROM units used in other PDP-14 control systems. It is functionally equivalent to the interconnections in a relay control system, and as such, is specifically programmed (wired) for each application.

1.3.2.4 **Control Unit** – The Control Unit directs the operation of the controller based upon manual inputs, program instructions, test results, or information provided by a computer. It interfaces with the ROM, all I, O, and A Boxes, and the computer.

The Control Unit begins operation by initializing the controller (placing its circuits in a state for starting operation). Next, it addresses the first ROM location and fetches an instruction. The Control Unit interprets (decodes) then performs (executes) the instruction.

Instruction execution can entail testing an input or output, making a decision, or turning an output on or off. After executing an instruction, the Control Unit repeats the cycle by fetching another instruction.

For a Test Input instruction, the Control Unit addresses the input circuit. The input circuit responds by providing the on/off state of the input to the Control Unit on the input sample return line. The Control Unit temporarily stores this information. It then fetches another instruction to evaluate the input.

An identical operation is performed for a Test Output instruction. For an Operate instruction, however, the Control Unit also specifies the function to be performed; i.e., whether an output is to be turned on (SET) or off (RESET), or whether all outputs are to be turned off (CLEARED).

1.3.3 I Boxes

An I Box accepts on/off status inputs from the machine or process system and converts them into logic levels usable by the controller. Each I Box is capable of accepting up to 32 ac or dc inputs (but not both). Up to eight I Boxes can be used in a typical control application for a total of 256 inputs. Machine inputs are connected to screw terminals on the front of I Box modules. Control cables (one from each I Box) connect the I Boxes with the Control Unit.

A Test Input instruction defines the input to be tested and the state (on or off). When the controller executes one of these instructions, the Control Unit sends an input address (for selecting one of 32 inputs) to the I Boxes

and selects one of eight possible I Boxes. The selected I Box, in turn, decodes the address and selects two input circuits. Information from the selected input circuits is then provided on two sample return lines and the PDP-14 Control Unit must determine which sample return is valid.

1.3.4 O Boxes

An O Box converts controller logic levels into outputs used by machine or process system load circuits (such as indicators, solenoids, motor starters, etc.). Up to sixteen outputs can be handled by one O Box. These outputs can be either ac or dc (but not both). Up to sixteen O Boxes can be used in an application for a total of 255 outputs (the last output address, 256, is reserved for a special function). Output connections are provided by screw terminals on the output modules. Control cables (one from each O Box) connect the O Boxes to the Control Unit.

An output can be turned on or off or tested for an on or off state by the program instructions. These instructions define the output and the function to be executed. When the controller executes one of these instructions, the Control Unit addresses the output and defines the function. An output is turned on by a SET function and remains on until turned off by a RESET or CLEAR function. For testing of an output, the Control Unit simply addresses the output. In return, the O Box provides the state of the addressed output to the Control Unit on the output sample return line.

1.3.5 A Boxes

An A Box is a special purpose assembly that provides timer, retentive memory, and storage functions. An A Box requires one O Box cable slot in the mainframe and thus precludes the use of 16 output drivers. The A Box uses the same addressing logic and instructions as the O Box.

Up to 16 timer (or delay) circuits can be used in an A Box. The circuits are packaged two per board. Each timer circuit can provide a delay interval from 0.01 seconds to approximately 3 minutes. Each timer has an associated storage register (flip-flop) that is turned on (SET) or off (RESET) by program instructions. When set, this flip-flop starts the delay interval. After the timeout interval, the timer is considered on with respect to testing. A timer must be turned off (RESET) before it can be used again. A program instruction or an initialize operation resets the associated flip-flop to implement this action.

A retentive memory is a device that retains its state during power shutdown, power-off, or power-up conditions. Its principal use is to record a critical action or event and to retain the state corresponding to the event even though power is lost. Thus, its output can be used as a reference point when power is restored.

Two types of retentive memory modules are available. The K274 module provides two retentive memories (with indicator lights). The retentive memories are addressed in the same manner as outputs. Up to 16 retentive memories can be accommodated in one A Box by using K274 modules. The K272 module provides one retentive memory and only uses the even-numbered addresses on the right side of the A Box. Therefore, up to four retentive memories can be accommodated in an A Box by using K272 modules.

Each retentive memory has an associated control flip-flop. Each memory is turned on (SET) or off (RESET) by program instructions and is unaffected by an initialize operation.

Unused timer or retentive memory module slots can be used for storage outputs. A storage module is inserted in the vacant slots to connect the output of two storage register flip-flops to the output sample return line.

1.3.6 Storage Module

Storage functions can be provided by elements in the Control Unit as well as the A Box. A storage module can be installed in the Control Unit O Box connector slots. It provides 16 storage outputs but precludes the use of 16 "real" outputs. The storage module is addressed in the same manner as "real" outputs.

1.3.7 Operating Summary

A Test instruction defines whether an input or output is to be tested, the state (on or off) to be checked, and which input or output (address). For a Test Input instruction, the Control Unit provides the input address selection code to the I Boxes. The state of the applicable input is then provided to the Control Unit on the input sample return line. The Control Unit temporarily stores this state, then fetches another instruction from the ROM.

A Test Input instruction can be followed by a Decision instruction. This instruction compares the test result with a programmed state (on or off). Based upon the comparison, the program can branch to: 1) turn an output on; 2) turn an output off; or 3) continue testing. This branching defines the next ROM address.

Following the above action, the Control Unit fetches the next instruction from the specified ROM address and decodes the instruction. An Operate instruction defines the output function and the output address. For an Operate instruction, the Control Unit provides the output address selection code to the O and A Boxes. It also specifies a turn-on (SET) or turn-off (RESET) function. If a "real" output is specified, an output is provided to the machine or process system.

As the above operation continues, only pertinent portions of the ROM program are used (as determined by program branching). When the end of a ROM cycle is reached, the operation recycles. If no input (or output) states have changed since the last test, the program will follow the same memory path. If, however, input or output conditions have changed, program branching will cause a different path through the ROM, thereby changing the output states.

As mentioned previously, A Boxes permit the use of timers, retentive memories, or storage elements. Outputs provided by these elements do not directly control system outputs and are not considered "real" outputs. Accessory (A) Boxes use the same instruction and address selection scheme as O Boxes.

1.4 SPECIFICATIONS

Overall System

Number of Inputs:	Up to 256 (eight I Boxes with 32 inputs each). Further expansion in units of 32 is possible up to a maximum of 512 inputs by decreasing output capability accordingly.
Type of Inputs:	ac or dc
Number of Outputs:	Up to 255 (sixteen O Boxes with sixteen outputs each; output address 256 is reserved for clearing all outputs).
Type of Outputs:	ac or dc
Average Instruction Execution Time:	20 μs ± 20%
ROM Capacity:	1024 to 4096 12-bit instruction words in increments of 1024 words.

*Average ROM Program Execution Times for Program Usage:	**1K**	**2K**	**3K**	**4K**
	15 ms	30 ms	45 ms	60 ms

Environmental:

Operating Temperature	0° to 70°C (32° to 160°F) at controller; 0° to 55°C (32° to 130°F) ambient (outside enclosure).
Relative Humidity	10 to 85%
Vibration	1.25 g's (maximum); 0 to 100 Hz (sinusoidal) in each of three normal axes.
Other	Designed for NEMA 12 enclosure.

Power Requirements:

Voltage	105 to 125 Vac or 210 to 250 Vac
Frequency	47 to 500 Hz
Wattage	86W (average power dissipation for maximum system using ac inputs and outputs)

BX14-DA Input (I) Box

Number of Inputs:	32 (with indicators)
Input Voltage and Loading:	115 Vac @ 1.5 VA
Input Threshold:	100 Vac (minimum)
Response:	16 to 32 ms for K578A usage; 8 ms (minimum) for K578B usage.

BX14-SA Input (I) Box

Number of Inputs:	32 (with LED indicators)
Input Voltage and Loading:	115 Vac @ 1.5 VA
Input Threshold:	80 Vac (minimum)
Response:	8 to 12 ms

BX14-DD Input (I) Box

Number of Inputs:	32 (with indicators)
Input Voltage Range:	10 to 55 Vdc (above 55 Vdc with external series resistor at 50 ohms per volt)
Input Voltage and Current (typical):	12 Vdc @ 10 mA 24 Vdc @ 10 or 30 mA 48 Vdc @ 20 mA
Response Time:	2 ms excluding contact bounce
Bounce Rejection:	will reject up to a 3-ms bounce

*Based upon a 20-μs instruction execution time and 75% usage of program instructions.

BY14-DA Output (O) Box

Number of Outputs:	16 (with indicators)
Output Voltage and Drive:	115 Vac; 500 VA (maximum) per output or a distributed maximum of 1000 VA per 1/4 O Box.

BY14-DD Output (O) Box

Number of Outputs:	16 (with indicators)
Output Voltage:	10 to 250 Vdc (dc switched to ground)
Output Current:	1A (maximum) for each circuit
Output Saturation Voltage:	2.5V (maximum)

BA14 Accessory (A) Box

*Number of Retentive Memories:	16 maximum using the K274 module (2 memories per module) 4 maximum using the K272 module (1 memory per module)
*Number of Timers:	16 maximum (2 timers per K302 module)
Timer Intervals:	0.01 to 30 sec (standard). Up to 4 min, 45 sec with additional resistance.
*Storage Outputs:	16 maximum (2 outputs per K022 module)

BF14-M Storage Module

Storage Outputs:	16 non-active outputs. Plugs into PDP-14 mainframe in place of an ac or dc Output Box.

*One A Box can accommodate various combinations of up to eight retentive memory, timer, and storage modules (Figure 2-4).

CHAPTER 2
USER MAINTENANCE

2.1 GENERAL

This chapter contains instructions that enable user personnel to maintain the PDP-14 Controller; they are also intended as the first level of maintenance for field service personnel. The chapter has three primary divisions:

a. Maintenance Information – 1) defines the maintenance philosophy; 2) briefly describes the controller units and functional relationships; and 3) lists the recommended test equipment and spares.
b. Fault Isolation and Repair Without A Computer – provides the recommended approach and procedures for isolating and repairing the PDP-14.
c. Fault Isolation and Repair With A Computer – provides the procedure for using computer diagnostics and for repair of the PDP-14.

2.2 MAINTENANCE INFORMATION

2.2.1 Maintenance Philosophy

The PDP-14 requires no periodic maintenance or adjustments and, therefore, no scheduled downtime. From a maintenance standpoint, it is operated continually until a system malfunction occurs.

For the user, the recommended level of repair is module replacement. If the PDP-14 cannot be fixed by module replacement, replace the next larger assembly or contact your DEC Field Service representative. Module repair should only be attempted by personnel thoroughly trained in electronics and digital repair techniques.

2.2.2 Controller Description

2.2.2.1 ROM – A ROM (Read-Only Memory) stores the program instructions for implementing a machine or process system sequence. A ROM can be comprised of up to four banks as shown in Figure 2-1. Each ROM bank consists of three modules, two of which (the G922 and G923) form one plug-in assembly. Each bank can store up to 1024 12-bit instructions. The functions provided by each module are described below:

a. ***G924 ROM Selection*** – This module selects the instructions stored in the ROM as specified by the control unit. This module also contains the timing circuits for controlling ROM operation. For an address selection, the Control Unit enables one memory bank and provides a 10-bit address and a timing pulse to start the operation. The G924 module receives seven of these address bits and selects one of 128 braid wires. The three remaining bits select one out of eight rows of sense amplifiers on the G922-G923 assembly. After a short interval allotted for circuit settling, the G924 module pulses the selected group of sense amplifiers to load an instruction in its output buffer. It then notifies the Control Unit that the memory cycle is complete.

b. ***G922 ROM Braid and G923 Sense Amplifier*** – The G922 module contains a pattern or braid of 128 wires. Each wire is routed either through or around 96 (8 sets of 12) Ferrite-core transformers to form the binary content of eight 12-bit instructions. (If the wire is routed through the transformer, it results in a logical 1 for the pertinent bit when the wire is pulsed; if the wire is routed around, it results in a logical 0 bit). The braid arrangement is functionally equivalent to the wiring in a conventional control system; i.e., it forms a list of permanently wired instructions that define the control operation. Once the braid is formed, it is encapsulated for immunity to accidental change. The module is then attached to the G923 module to form one plug-in assembly.

The G923 module decodes three bits of address to select one of eight groups of sense amplifiers. Each group consists of 12 sense amplifiers or one for each bit in an instruction. This selection (in conjunction with that of the G924) selects one 12-bit instruction out of 1024 possible instructions (128 wires x 8 instructions per wire). The selected instruction is made available to the Control Unit when the G924 module notifies the Control Unit that an instruction cycle is completed.

NOTE
The information content of each G922 module is unique; therefore, do not substitute this plug-in assembly.

2.2.2.2 Control Unit – As mentioned previously, the Control Unit is fundamentally the heart of the PDP-14 Controller. It consists of a number of modules with perhaps the most complex interrelationships of the system. Figure 2-1 shows the Control Unit modules and includes a brief title that defines their function. Note that the maximum configuration is shown; a number of the modules (and connectors) are required only if the controller interfaces with a computer. A brief functional description of the modules follows:

a. ***M742 Switch and Power Control*** – This module:

1) Senses power-up and power-down conditions, initializes the system, and starts system timing.
2) Interfaces with the START/STOP and CONTINUE switches to provide manual control.
3) Detects timing failures and holds the system in an initialize state.
4) Decodes two bits of the memory address to enable one out of four possible ROM banks.
5) Provides control (and three bits) for Test and Display instructions used for computer monitoring.

b. ***M741 Major States and Timing*** – This module provides the timing relationships and control signals for:

1) Fetching of instructions
2) Decoding of instructions
3) Execution of instructions
4) Sampling and storing input or output test results

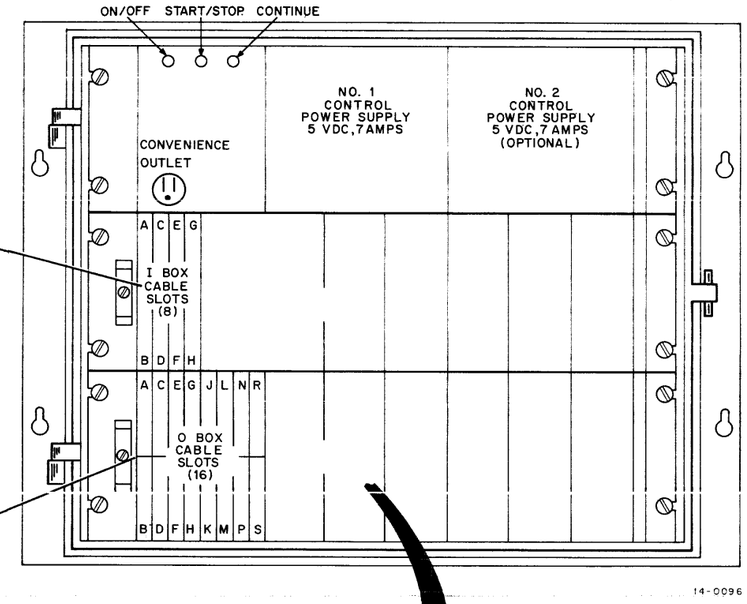
c. ***M747 Program Counter 1 (PC1)*** – Two M747 modules comprise PC1. This register addresses the ROM to fetch an instruction. It is an incrementing type register; i.e., its count can be incremented by one.

d. ***M746 Memory Buffer (MB) Register*** – Two M746 modules comprise the MB Register. This register temporarily stores instructions provided by the ROM or computer.

e. ***M746 Instruction Register (IR)*** – Two M746 modules comprise the IR. This register accepts the instructions from the MB Register and stores them for decoding and execution.

I Box Cable Slot	System Address (Octal)
A	0–37
B	40–77
C	100–137
D	140–177
E	200–237
F	240–277
G	300–337
H	340–377

O Box Cable Slot	System Address (Octal)	O Box Cable Slot	System Address (Octal)
A	0–17	J	200–217
B	20–37	K	220–237
C	40–57	L	240–257
D	60–77	M	260–277
E	100–117	N	300–317
F	120–137	P	320–337
G	140–157	R	340–357
H	160–177	S	360–377



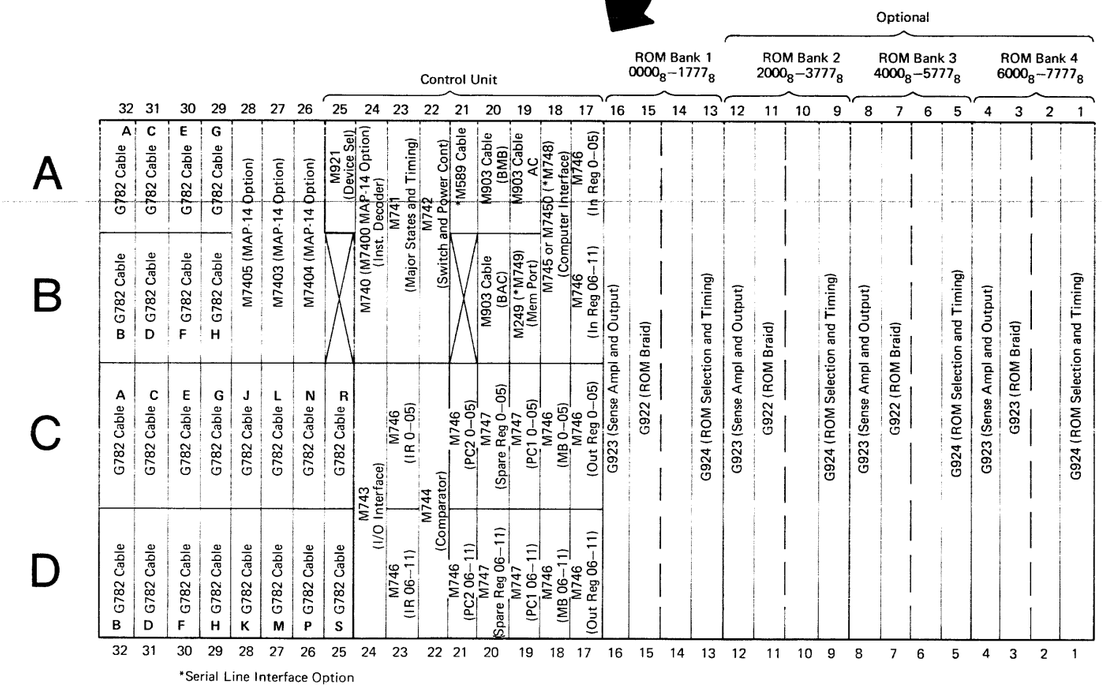


Figure 2-1 PDP-14 Mainframe Showing Module Locations

Notes:

1. Maximum configuration shown.
2. The following modules are used only with a computer application:

Module		Slot
M249	Memory Port	B19
M745	Computer Interface	AB18
M746	Input Register	A17, B17
	Output Register	C17, D17
M921	Device Selector	A25

3. Storage Module M232 can be used in any O Box cable slot to provide up to 16 storage outputs.

f. ***M740 (or M7400) Instruction Decoder*** – This module examines each instruction and provides unique control signals for instruction execution. (The M7400 module must be used with MAP-14.) This module decodes parts of the instruction to:

1) Define the type and specific instruction to be executed
2) Select the source register for internal transfers
3) Select the destination register for internal transfers

g. ***M743 I/O Interface*** – This module interfaces the Control Unit with the I, O, and A Boxes. It provides the input or output circuit address and designates the required function for outputs. It also compares the test result with the program-expected result and provides this comparison result to the M741 module.

h. ***M746 Program Counter 2 (PC2)*** – Two M746 modules comprise PC2. This register is used only for program subroutines. It stores the program return address for subroutines.

i. ***M747 Spare Register*** – Two M747 modules comprise the Spare Register. This register is not normally included in the PDP-14 and is not required. If included, this register is used as a utility register.

j. ***M745 Computer Interface*** – This module interprets computer input/output transfer (IOT) instructions and synchronizes controller operations with the computer.

k. ***M746 Input Register*** – Two M746 modules comprise the Input Register. The register is only used for computer operations. The register accepts and buffers 12-bit data from the computer for internal register transfer instructions.

l. ***M746 Output Register*** – Two M746 modules comprise the Output Register. The principal use for this register is to return test results to a computer.

m. ***M921 Device Selector*** – This module is only used for computer operations. It establishes a device code for the PDP-14 Controller so that the computer can communicate with the controller.

n. ***M249 (or M106) Memory Port*** – This module is only used for computer operations. The register accepts and buffers 12-bit instructions from the computer and provides them to the MB register for execution. The M249 Memory Port must be used with the PDP-8/E computer. PDP-14s used with the PDP-8/I or PDP-8/L computer may also use the M106 Memory Port in place of M249 if the proper ECO is installed.

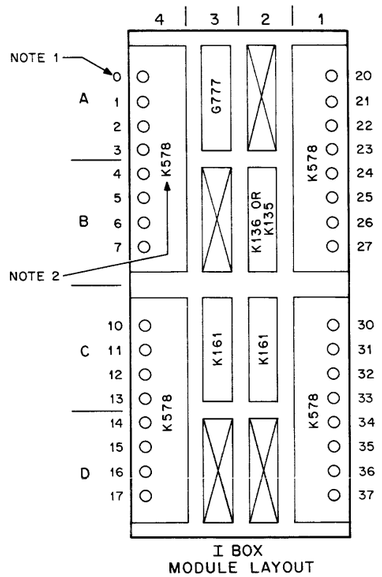
2.2.2.3 I Boxes BX14-DA and BX14-DD – As mentioned previously, each I Box provides the capability for handling 32 status inputs. These inputs can be either ac or dc (but not both). For ac inputs, a system uses I Box BX14-DA. For dc inputs, a system uses I Box BX14-DD. These I Boxes differ only in the input converter module used. Figure 2-2 depicts the module layout for an I Box and the hierarchy of modules as related to fault isolation. The modules are described in subsequent paragraphs.

a. ***K578 AC Input Converter*** – This module accepts up to eight ac inputs and converts them into logic levels. Inputs are connected to a terminal strip on the front of the module. A neon indicator is provided for each input; this indicator lights when 115 Vac is present at the input.

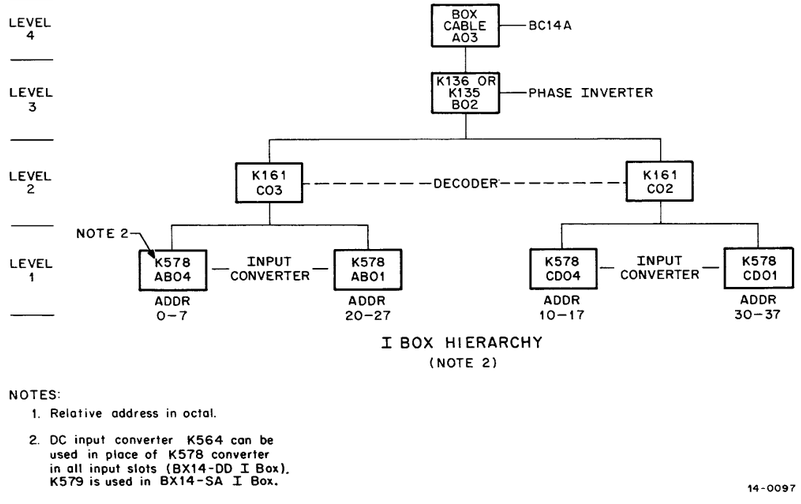
b. ***K564 DC Input Converter*** – This module accepts up to eight dc inputs and converts them into logic levels. This module accepts inputs having a range from 10 to 55 Vdc (or above 55 Vdc with an external series resistor at 50 ohms per volt). Inputs are connected to a terminal strip on the front of the module. A light-emitting diode (LED) is provided for each input. This indicator lights when voltage is present at the input terminal.

c. ***K161 Decoder*** – This module is used in the addressing (or selection) of inputs. It decodes three bits of address from the Control Unit to select one of the eight input circuits on a K578 or K564 Input Converter.

d. ***K136 (or K135) Inverter*** – This module contains four independent inverter circuits used in the addressing of input circuits and in input test return circuits. Each inverter circuit performs a logical NOT function.



I BOX
MODULE LAYOUT



I BOX HIERARCHY
(NOTE 2)

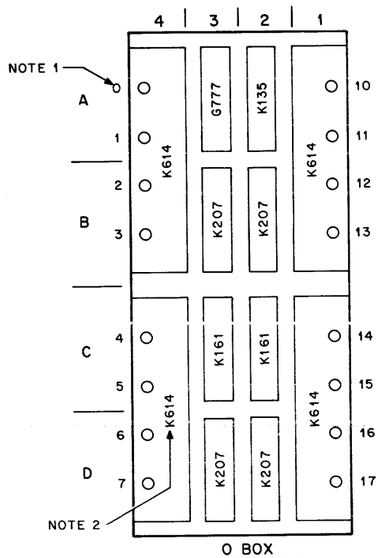
NOTES:
1. Relative address in octal.
2. DC input converter K564 can be used in place of K578 converter in all input slots (BX14-DD I Box). K579 is used in BX14-SA I Box.

14-0097

Figure 2-2 I Box Layout and Hierarchy

2.2.2.4 O Boxes BY14-DA and BY14-DD – Each O Box contains 16 independent output circuits that drive machine or process system devices. The outputs can be either ac or dc (but not both) depending upon system usage. A BY14-DA O Box provides ac outputs; a BY14-DD O Box provides dc outputs. These boxes differ only in the output driver modules used.

Figure 2-3 depicts the module layout for an O Box and the hierarchy of modules as related to fault isolations. The modules are briefly described in the following paragraphs.



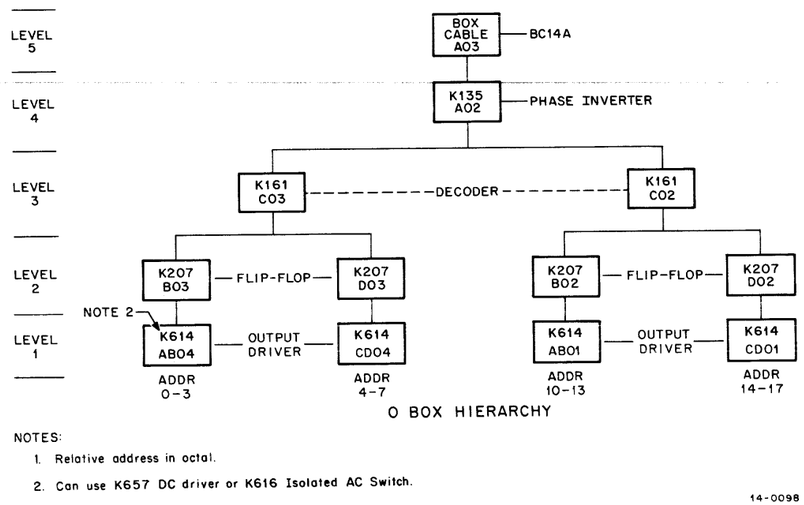


Figure 2-3 O Box Layout and Hierarchy

a. ***K614 Isolated AC Switch*** – Four of these modules can be used in a BY14-DA O Box. Each module contains four independent ac driver circuits. Each circuit is independently rated at 500 VA, however, the collective total power rating for a module is 1000 VA. Each circuit is equipped with a neon indicator. This indicator lights when 115 Vac is being provided to the load.

b. ***K657 DC Driver*** – Four of these modules can be used in a BY14-DD O Box. Each module contains four dc driver circuits. Each circuit can be used to switch a dc load (having a source voltage from 10 to 250 Vdc) to ground. Each driver circuit is rated at 1A (maximum). Each output has an LED that indicates when the output path is completed.

c. ***K207 Flip-Flop*** – This module contains four storage registers (flip-flop circuits) that control the output circuit on a K614 or K657 module. When turned on (SET) by a program instruction, a flip-flop causes the output circuit path to be completed. The flip-flop remains in this state until turned off (RESET) by a program instruction or an initialize operation. The state of the K207 flip-flop is tested by the control program to determine if an output is on or off.

d. ***K161 Decoder*** – This module is used in the addressing (or selection) of outputs. It decodes three bits of address from the Control Unit for selection of one of eight flip-flop circuits contained in two K207 modules.

e. ***K135 Inverter*** – This module contains four independent inverter circuits used in the addressing of output circuits and in the output test return circuits. Each inverter circuit performs a logical NOT function.

2.2.2.5 A Box – An A Box can be used to provide timer (delay), retentive memory (event storage during power-off states), or normal storage functions. Each A Box requires one O Box cable slot. In most instances, A Boxes are assigned an upper system address to differentiate from "real" outputs. An A Box can be configured in a number of ways. Figure 2-4 depicts the module location and hierarchy for an A Box. A brief description of the modules is provided in subsequent paragraphs. (For additional details concerning A Box functions and relationships, refer to Chapter 1).

a. ***K302 Timer*** – A K302 Timer module contains two timer circuits. Each circuit is capable of providing standard delay intervals from 0.01 to 30 seconds. With the additional resistance, a timer can also provide delay intervals up to 4 minutes, 45 seconds. A timer circuit is addressed in the same manner as O Box modules, except the sample return is generated on this module and not on the K207. Up to eight K302 Timer modules (16 timer circuits) can be accommodated in one A Box.

b. ***K272 Retentive Memory*** – A retentive memory retains its state during power off and is unaffected by an initialize operation. Up to four K272 Retentive Memory modules can be used in an A Box, each providing one retentive memory circuit. These modules are addressed in the same manner as "real" outputs but only even-numbered relative addresses on the right-hand side of the A Box can be used.

c. ***K274 Retentive Memory*** – This module functions in the same manner as the K272 module, but contains two retentive memory circuits per board. Up to eight K274 modules can be accommodated in one A Box to provide a total of 16 retentive memory circuits.

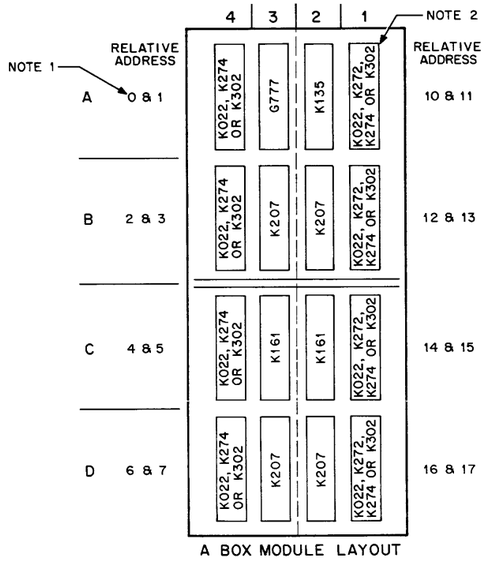
d. ***K022 Storage Module*** – This module can be inserted in the unused timer or retentive memory slot to provide two storage outputs. The module connects the outputs from two K207 flip-flops to the output test return circuits in an A Box. The storage outputs provided by the K022 use the relative addresses of the module slot.

e. ***K207 Flip-Flops*** – This module contains four flip-flops. Each flip-flop can be independently set and reset or all can be collectively reset. Each flip-flop can control one timer or one retentive memory or can be used with a K022 Storage module to provide one storage output. Unlike the O Box, the sample return in an A Box is not generated from this module.

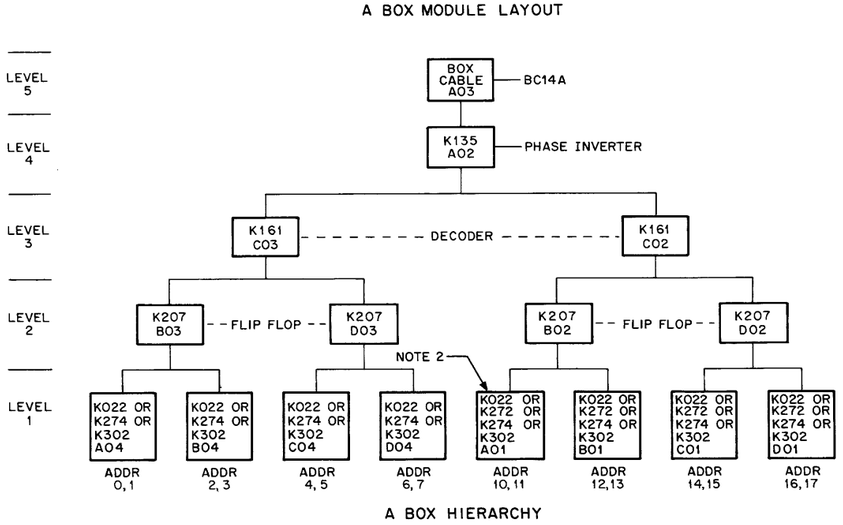
f. ***K161 Decoder*** – This module is used in the addressing of A Box circuits. It decodes three bits of address from the Control Unit to select one of eight K207 flip-flops.

(continued on next page)

g. ***K135 Inverter*** – This module contains four independent inverter circuits used in the addressing of A Box circuits. Each inverter circuit performs a logical NOT function.



A BOX MODULE LAYOUT



A BOX HIERARCHY

NOTES:
1. Relative address in octal
2. K272 retentive memory contains one memory and uses only even numbered relative addresses. K274 retentive memory contains two memories and uses both addresses.

14-0099

Figure 2-4 A Box Layout and Hierarchy

2.2.3 Recommended Test Equipment

A VOM (such as Simpson, Model 260 or Triplett, Model 630NA) is recommended for user maintenance. An oscilloscope (such as Tektronix, Model 453) is considered optional.

2.2.4 Recommended Spare Parts

Table 2-1 lists the recommended spare parts by major units. Table 2-2 lists the spare parts recommended for a typical PDP-14 configuration.

Table 2-1
Recommended Spare Parts by Major Units

CONTROL UNIT SPARES

M740	Instruction Decoder	one for every three control units
M741	Major States and Timing	
M742	Switch and Power Control	
M743	I/O Interface	
M744	Comparator	
M746	Bus Register	
M747	Incrementing Bus Register	
BC14A-15	I/O Cable	

COMPUTER INTERFACE SPARES

M249	Memory Port	one for every three computer interfaces
M745	Computer Interface	
M746	Bus Register	
M921	Device Selector	

MEMORY SPARES

G923	ROM Sense Amplifier	one for every four ROMs
G924	ROM Selection and Timing	

FUSES

Littelfuse 5A type 276005 for K614 Isolated AC Switch

INPUT (I) BOX SPARES

K136	Inverter	one for every two boxes
K161	Binary-To-Octal Decoc	
K564	DC Input Converter	
or	or	
K578/K579	AC Input Converter	

OUTPUT (O) BOX SPARES

K135	Inverter	one for every two boxes
K161	Binary-To-Octal Decoder	
K207	Flip-Flop	
K614/K616	Isolated AC Switch	
or	or	
K657	DC Driver	

ACCESSORY (A) BOX SPARES

K135	Inverter	one for every two boxes
K161	Binary-To-Octal Decoder	
K207	Flip-Flop	
K302	Timer	
K022	A Box Storage Module	
K272	Retentive Memory	
or	or	
K274	Retentive Memory	

2.3 FAULT ISOLATION WITHOUT A COMPUTER

2.3.1 General Approach

Fault isolation of a machine system malfunction can be analogous to isolating faults in the automobile. That is, the same general principles apply. First, we try to analyze the fault in major categories; whether the entire system is inoperative or, if it works, what part works and what part does not work.

Table 2-2
Spare Parts Recommended for a Typical Configuration

Configuration	Recommended Spares Quantity	Spare
One PDP-14 Control Unit	1	BC14A-15 I/O Cable
One Computer Interface	1	G923 ROM Sense Amplifier
Two 1K ROMs	1	G924 ROM Selection and Timing
Four I Boxes	1	K022 A Box Storage Module
Four O Boxes	5	K135 Inverters
One A Box	5	K161 Binary-To-Octal Decoders
Two Storage Modules	3	K207 Flip-Flops
	1	K274 Retentive Memory
	1	K302 Timer
	2	K578 or K579 AC Input Converters (or K564 DC Input Converters)
	2	K614 or K616 Isolated AC Switches (or K657 DC Drivers)
	1	M232 Storage Module (BF14-M)
	1	M249 Memory Port
	1	M740 Instruction Decoder
	1	M741 Major States and Timing
	1	M742 Switch and Power Control
	1	M743 I/O Interface
	1	M744 Comparator
	1	M745 Computer Interface
	2	M746 Bus Registers
	1	M747 Incrementing Bus Register
	1	M921 Device Selector

For example, if someone told you that your car won't run, you'd probably begin by finding out if the starting system will turn over the engine. If it did not, you'd probably suspect the starting system (battery, starter motor, solenoid, etc.). From this point, you can continue the investigation or begin substitution of components. If, however, the engine can be rotated but fails to start, you'd suspect a different set of components (possibly the carburetor, distributor, etc.) and would begin isolation from this point.

The same principles apply to the machine system you are troubleshooting. First, you must have a good understanding of what the machine does and in what order it does it. Next, you must analyze the failure in major categories. Is it a complete failure? If yes, you should literally begin at the power source of the controller. If no, examine the equipment and equipment sequence for additional symptoms or clues.

Since each machine or process system sequence is unique, the information provided in this chapter can only be considered as guidelines to systematic troubleshooting.

Figure 2-5 illustrates the basic steps of user maintenance described below.

Step 1. Determine what functions the machine or process system will and will not perform. In some instances, the malfunction may be readily apparent from the lack of a machine motion (or action) or from control panel status.

Step 2. Use the information from Step 1 to begin fault isolation. In general terms, the PDP-14 Controller output(s) for the applicable malfunction is checked first. This approach will generally isolate the machine or process system load circuits. If the PDP-14 is not providing the output, the machine status inputs (for this output) must be checked. This approach generally isolates the PDP-14 from the machine system input circuits.

Step 3. Locate and replace the machine components (switch, solenoid, etc.) or the PDP-14 malfunctioning module. (For maintenance purposes, the machine system includes all input and output wiring to and from the machine system.)

Step 4. Verify that the system operates normally after the repair.

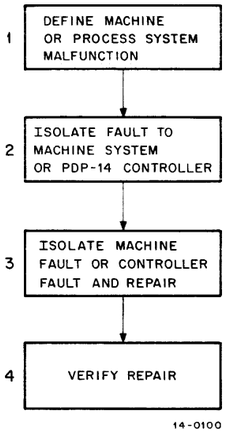


Figure 2-5
User Maintenance Steps

2.3.2 Input and Output Organization

As mentioned previously, the PDP-14 program establishes the relationships between inputs denoting machine status and controller outputs denoting machine action. Before this program can be written, however, the input and output relationships must be defined. Then, the inputs and outputs must be assigned to I and O circuits.

In the traditional relay control system, control relationships are often established using ladder diagrams and symbolic equations. Both are also useful tools in defining control relationships for PDP-14 Controller applications.

Figure 2-6 shows an example of a ladder diagram, symbolic equation usage, and the Boolean equivalent. It also illustrates the usage of Input and Output Assignment Tables and defines the logical operators and the input and output designations for controller use.

The A part of Figure 2-6 illustrates a logical AND function and the B part illustrates a logical AND-OR function with grouping of combinations using parentheses. Parentheses are used to eliminate ambiguity in the relationships. The B part also defines the use of a NOT operator.

After input and output relationships have been established, each PDP-14 output and input is assigned a terminal number. The symbolic equation, its Boolean equivalent, and the device(s) involved are then entered into Input or Output Assignment Tables such as those illustrated in Figure 2-6.

2.3.3 Input and Output Assignment Tables

Input/output relationships (and the devices providing the status or using the output) are usually defined in Input and Output Assignment Tables. From a fault isolation standpoint, the information in these tables is very useful. Therefore, a brief description of their content and typical use follows.

(Continued on page 2-9)

INPUT ASSIGNMENT TABLE

Prog No.	Input Device	Notes	I Box Terminal
X0	POWER Control Relay CR1		A1
X1	START pushbutton PB1		A2
X2	SLOW switch LS2		A3
X3	FORWARD Motor Starter M2	From NC contacts of FORWARD Motor Starter	A4

OUTPUT ASSIGNMENT TABLE

Output Device Identification	Output Control Equation X = Input, Y = Output, + = OR, * = AND, / = NOT	Prog No.	O Box Terminal
RESTART Sol. SOLA	SOLA = CR1 * PB1 Y0 = X0 * X1	Y0	A1
SLOW light 2LT	2 LT = (SOLA * LS2) + / M2 Y1 = (Y0 * Y2) + X3	Y1	A2

LADDER DIAGRAMS EQUATIONS

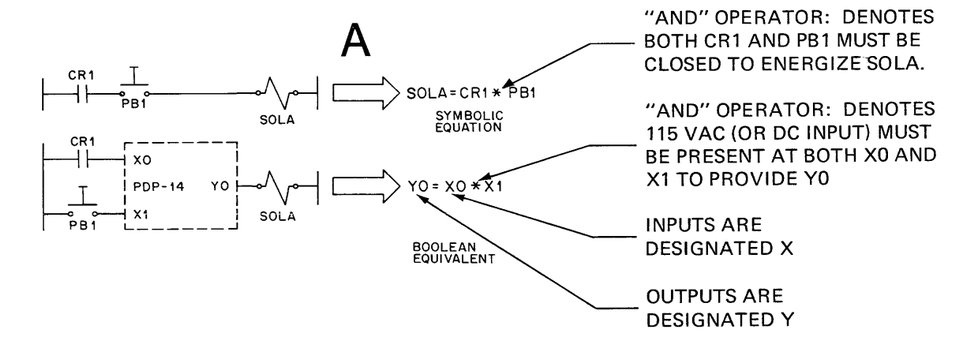


Figure 2-6 Input/Output Relationships

EXAMPLE 1: ASSUME THAT YØ=XØ*X1 (SOLA=CR1*PB1) AND THAT YØ IS OFF.

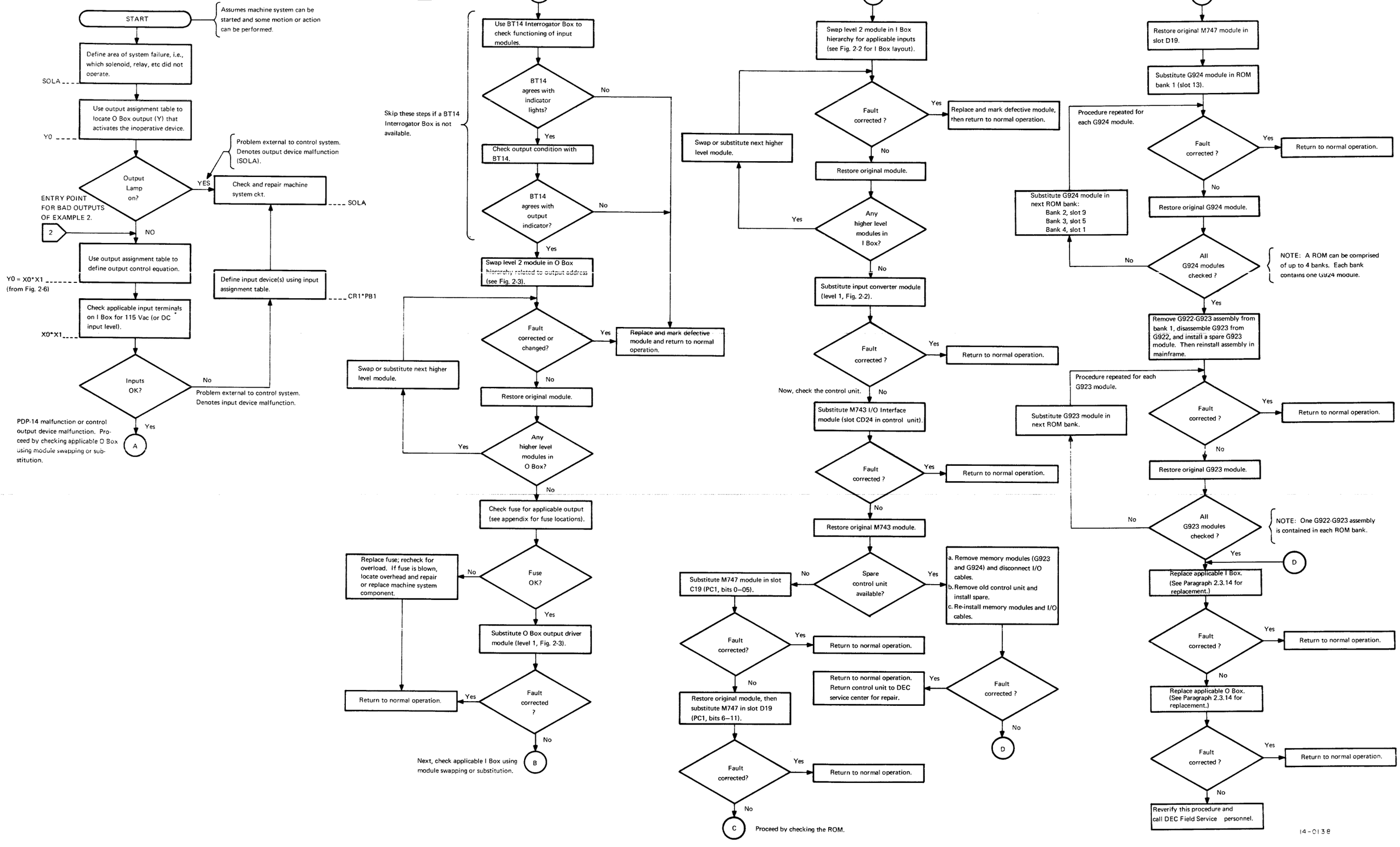


Figure 2-7 Decision Diagram, Fault Isolation Example Number 1

An Output Assignment Table usually identifies the device being controlled, the symbolic and Boolean equations for the output, and a PDP-14 terminal number for the output. Terminal numbers are generally assigned using the system address (in octal) for the output circuit. These terminal numbers range from 0 to 377, excluding numbers containing the digits 8 or 9. Generally, non-real outputs (storage, timer, or retentive memory outputs) are assigned the upper-most program numbers.

An Input Assignment Table generally defines the input device supplying the status input plus any pertinent notes related to system functions. Input tables can be arranged by terminal number order as shown in Figure 2-6. Terminal numbers for inputs can be from 0 to 377, excluding numbers containing the digits 8 or 9.

2.3.4 Fault Isolation Example Number 1

Figure 2-7 is a decision diagram that illustrates the recommended methods of fault isolation. The example assumes the RUN indicator (Figure 2-6) is off, yet some machine action or motion can be performed (the system can be started or is not locked in an initialize condition). Note that malfunctions external to the controller can be readily identified and that in the worst case condition, the decision diagram must be followed to the end (or near the end). The decision diagram is presented in general terms so that it is generally applicable to all output equations. The decision diagram has two entry points other than START. These points are used when more complex equations are encountered as illustrated in Fault Isolation Example Number 2. Use of steps involving the BT14 Interrogator Box are optional, but are strongly recommended if a BT14 is available.

2.3.5 Fault Isolation Example Number 2

Figure 2-8 is a decision diagram that indicates how more complex equations should be handled. Note that the general approach is to determine if an alternate mode works. Note also that if the fault is isolated to the controller, the isolation is continued using Figure 2-7.

2.3.6 Fault Isolation For Equations Involving Timer Functions

In general, timer malfunctions can be readily detected by observing system symptoms. A timer malfunction manifests itself by the lack of an interval between two machine or process system events or the second event never occurs.

Timer malfunctions are isolated in a manner similar to that of active outputs, except that there are no indicators to define whether the timer is working. In addition, each timer module is unique from a substitution standpoint; i.e., its components are set up to provide a unique time interval. In addition, substitution is compounded because each timer module contains two timer circuits.

The general approach for equations involving timers is to check all other parts of the equation first, using the methods described in Paragraphs 2.3.4 and 2.3.5. If the fault is isolated to the timer term of an equation, use the method illustrated in Figure 2-9 to isolate the fault. As can be observed, all modules involved in the selection are changed first, since timer substitution is difficult because each timer is unique and possibly affects two circuits.

NOTE

When substituting or replacing a timer module, always match timing capacitor usage; i.e., clip the same capacitor leads as on the old module (see Figure 2-10 for timing capacitor location). For gross adjustment of the timer interval, refer to Paragraph 4.5.2.

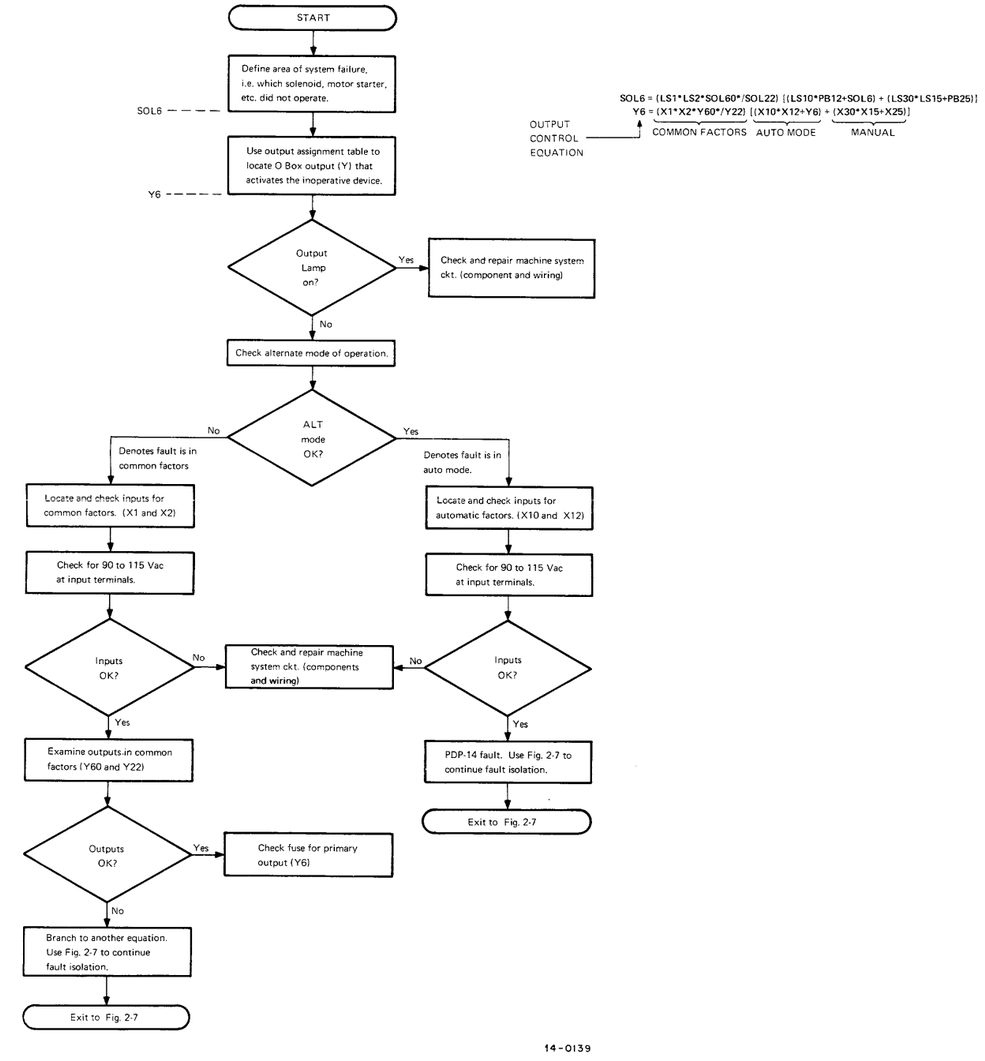
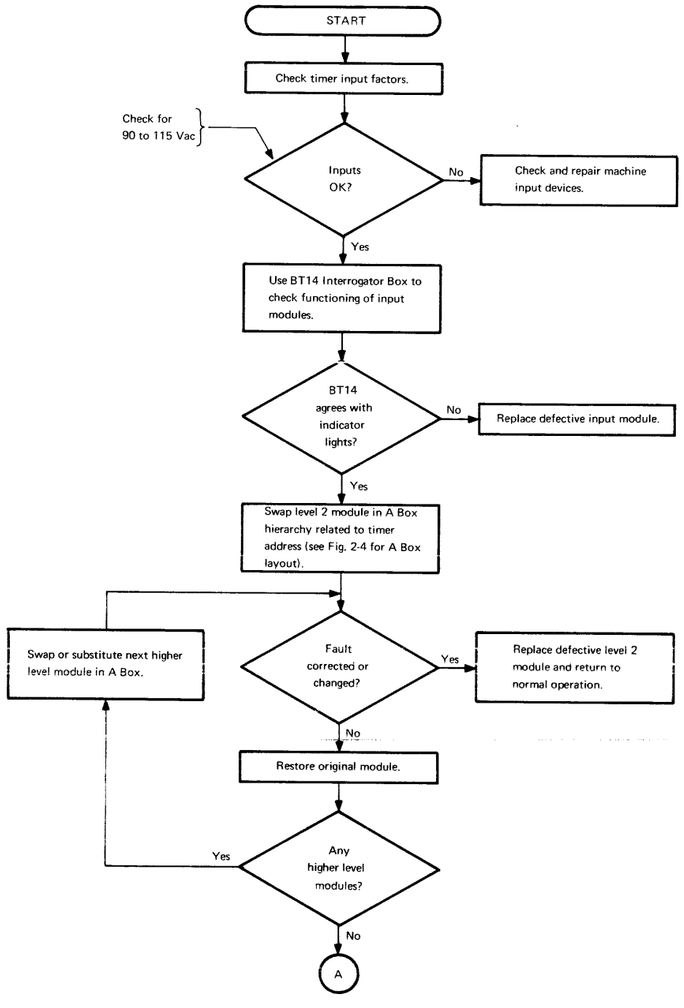


Figure 2-8 Decision Diagram, Fault Isolation Example Number 2

2.3.7 Fault Isolation For Equations Involving Retentive Memory Factors

When a retentive memory is suspected of being defective, replace the retentive memory module first. If the fault is not corrected, restore original module, then continue isolation using Figure 2-7. The K274 Retentive Memory module is easily isolated since an LED indicator is used to display the status of each circuit. K272 and K274 modules have switches to clear the retentive memory. This switch should be in the center position for proper operation.



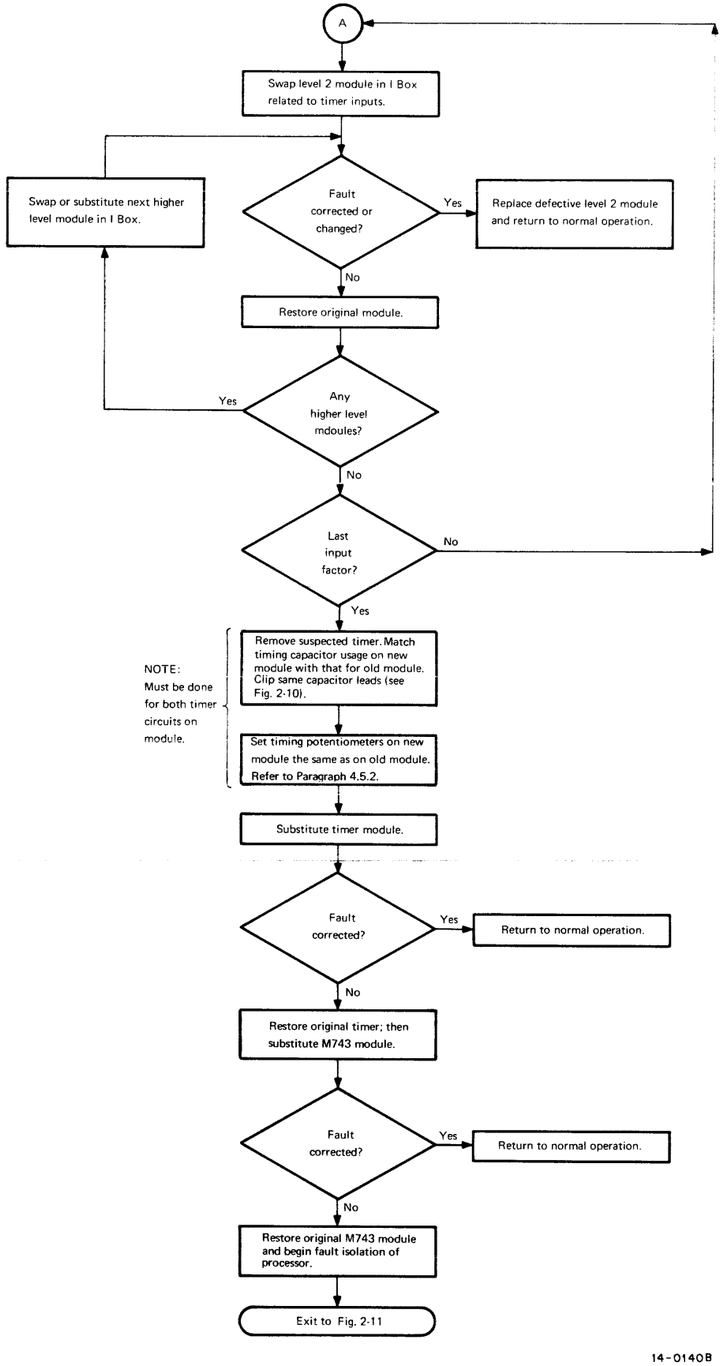


Figure 2-9 Decision Diagram, Fault Isolation for Equations Involving Timer Functions

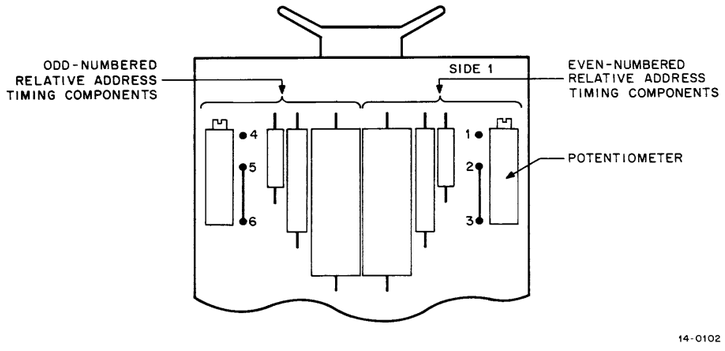


Figure 2-10 K302 Timer Components

2.3.8 Fault Isolation For Equations Involving A Box Storage Functions

When a K022 Storage module is suspected of being defective, replace the K022 module first. If the fault is not corrected, restore original module and continue fault isolation using the procedure in Figure 2-7. Use of the BT14 Interrogator Box will allow the state of the storage bit to be determined.

2.3.9 Fault Isolation For Major System Failure

If the system cannot be started or is locked in an initialize condition, the fault is probably in an area common to all logic functions. For example, the low-voltage power supply, the power-up and power-down sequence, or controller timing should be suspected. When a problem of this nature is encountered, use a systematic isolation method such as that illustrated in Figure 2-11.

2.3.10 Troubleshooting Hints and Kinks

a. ***Intermittent Problems*** – For intermittent problems, always check the common earth ground between the machine or process system and controller. A #6 copper wire (or larger) should be used for the common ground. Also check common ground between the processor and the I, O, and A Boxes.

b. ***Power Supply Foldback*** – To detect a power supply foldback problem, disconnect the load, then return to full load while observing output voltage for a 0.1V or greater change. If output voltage change is greater than 0.1V, replace power supply.

2.3.11 Module Substitution and Replacement Notes

a. ***K578 AC Input Converter*** – When replacing a K578, Rev. B, always use a Rev. B or greater, because of the speed of the input converter.

b. ***M744 Comparator*** – If TEST-14 denotes a faulty M744 module, continue troubleshooting unless the controller is performing SKE or SKZ functions. The M744 module does not normally affect control operation.

c. ***Modules for PDP-8/E Interface*** – An M745, Rev. E is required with M249 usage.

d. ***K302 Timer Module*** – When substituting or replacing a K302 Timer module, use the old module as a guide and clip out the same capacitor(s) on the new module. This must be done for both circuits if both are used. For gross adjustment of the time delay, refer to Paragraph 4.5.2.

2.3.12 Mainframe Replacement

When replacing the mainframe, be sure it is operational before putting it on-line. Do not swap the processor modules. Remove 110 Vac power from the entire system before starting. Then carefully mark all cables and ROM sections *before* removing them. Make sure the same number of power supplies are installed on the new mainframe as were present on the mainframe being removed. Finally, recheck *all* memories and cables after they are plugged into the new processor before applying power.

2.3.13 Power Supply Replacement

When replacing power supplies, be sure the jumpers between the two supplies are properly installed before applying power (if two power supplies are used).

2.3.14 I, O, and A Box Replacement

When replacing I, O, and A Boxes, be sure *all* power to the system is *off*. Attempting to change I, O, and A Boxes with the power on can result in serious damage to the system. Make sure the correct input and output modules (ac or dc) are used in the replacement box.

2.3.15 A Box Replacement

When replacing A Boxes, make sure the correct modules are installed in each slot (timers, retentive memories, and storage modules). Remember the timers must be individually adjusted for the proper timing. See Paragraph 4.5.2 or use a computer.

2.4 FAULT ISOLATION WITH A COMPUTER

2.4.1 Fault Isolation Approach

Four diagnostic test tapes are provided to aid in fault isolation. In general, three of the test tapes (TEST-14, VER-14, and ABE-14) are used for major or complete failures. The fourth test tape (ROL-14) provides an on-line interrogation feature to examine inputs and outputs. The ROL-14 tape is generally used for other than major or complete failures.

Figure 2-12 shows the recommended types of tests and the general dependency of the tests. Note that three tests can be performed using TEST-14. The first test, in general terms, checks the power control functions, major states and timing, computer interface, and all the other Control Unit functions except I/O interface and I/O timing. The second test (TEST-14 with one storage module) checks the I/O interface and I/O timing. The third test involving TEST-14, checks O Box functions with the O Box 115 Vac (or dc) source disconnected.

The VER-14 test checks the operation and contents of the ROM against a ROM tape entry in the computer that defines what the ROM should contain. Both sequential and random addressing are used.

The ABE-14 test checks the timer, storage, and retentive memory functions performed by A Box circuits. Thus, in the case of a major or complete failure, the system is tested from basic Control Unit functions through all output functions.

The ROL-14 test enables interrogation of inputs and outputs using the teleprinter. Thus, ROL-14 is generally used to evaluate malfunctions other than those considered a major or complete failure. In other words, ROL-14 is used when the machine or process system functions normally with only an isolated failure or failures.

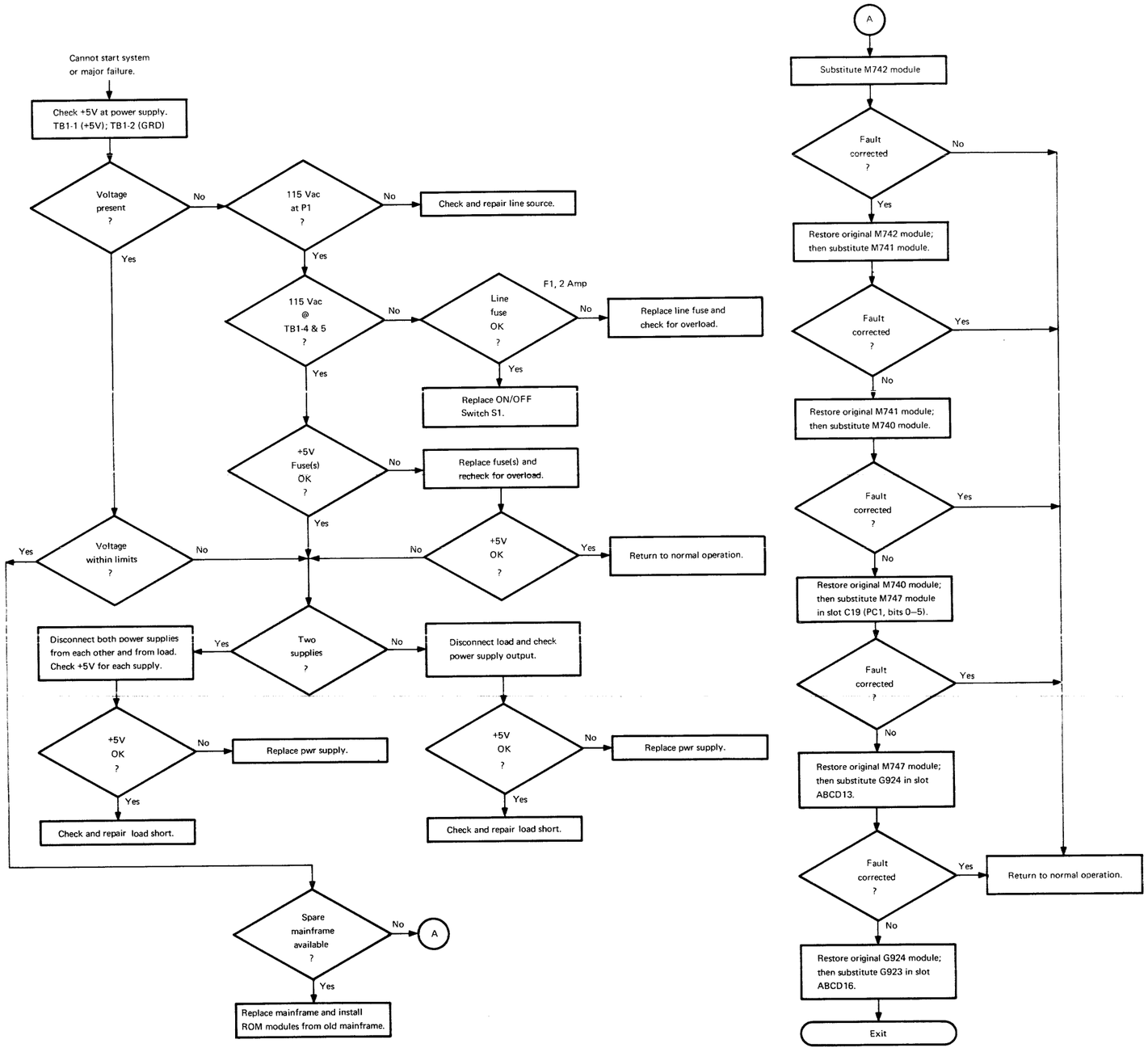


Figure 2-11 Decision Diagram, Fault Isolation for Major System Failure

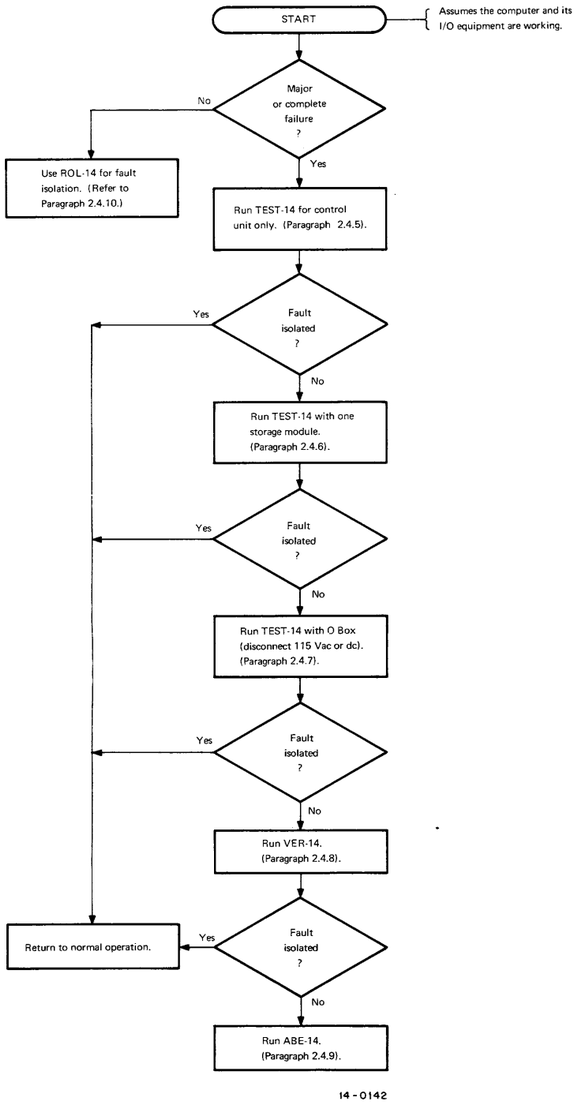


Figure 2-12 Diagnostic Test Usage

2.4.2 Connecting a Computer

A computer can be used for fault isolation of a controller used in a stand-alone application. However, since the computer is not an integral part of the system, interface modules must be installed and the computer must be connected to the PDP-14.

The following modules are required for the computer interface:

Module		Slot
*M249 Memory Port		B19
M745 Computer Interface		AB18
M746	Input Register	A17 and B17
	Output Register	C17 and D17
M921 Device Selector		A25

*An M106 module may be used in place of the M249 in any configuration except the PDP-8/E or PDP-8/M.

The M921 module selects the device code of the controller. It must have the device A portion wired to provide a device code of 16_8 or 17_8 (corresponding to BMB03 through 05 and 06 through 08 respectively). Figure 2-13 shows these connections. Figure 2-14 shows the cabling for the PDP-14-to-computer interface.

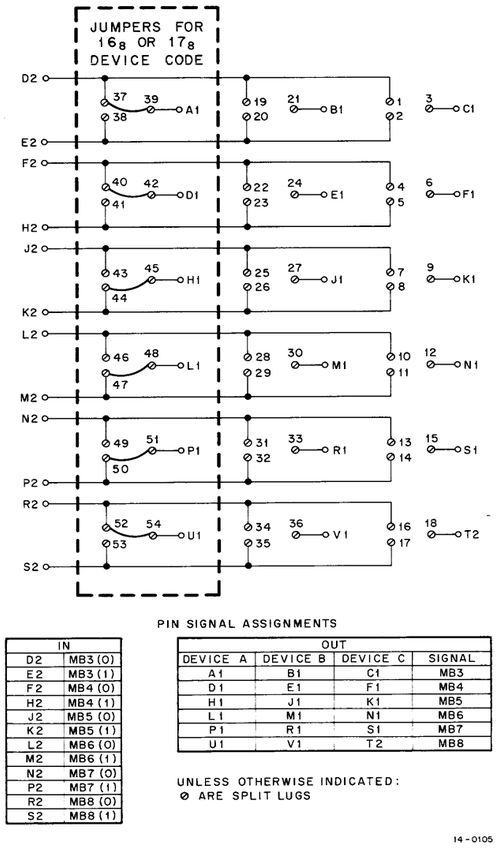
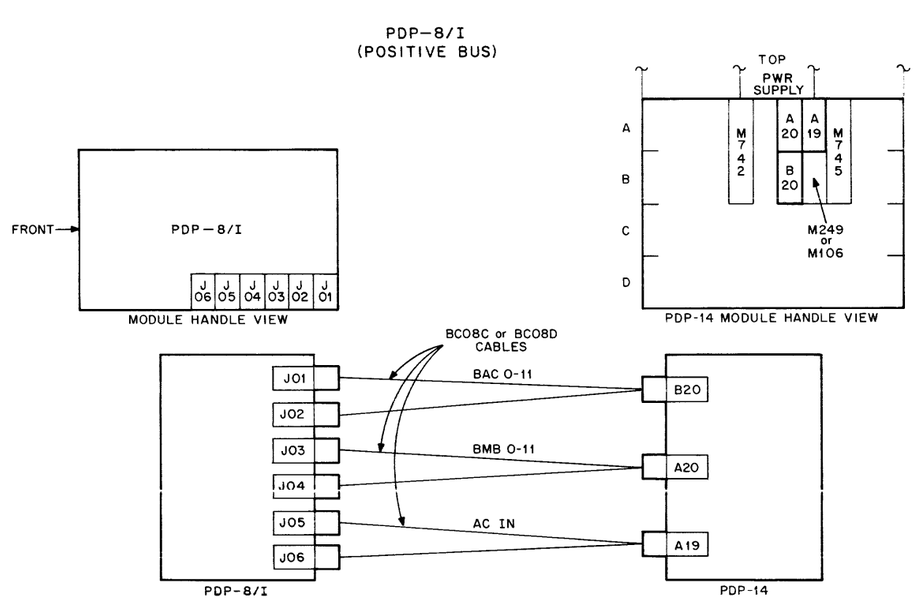
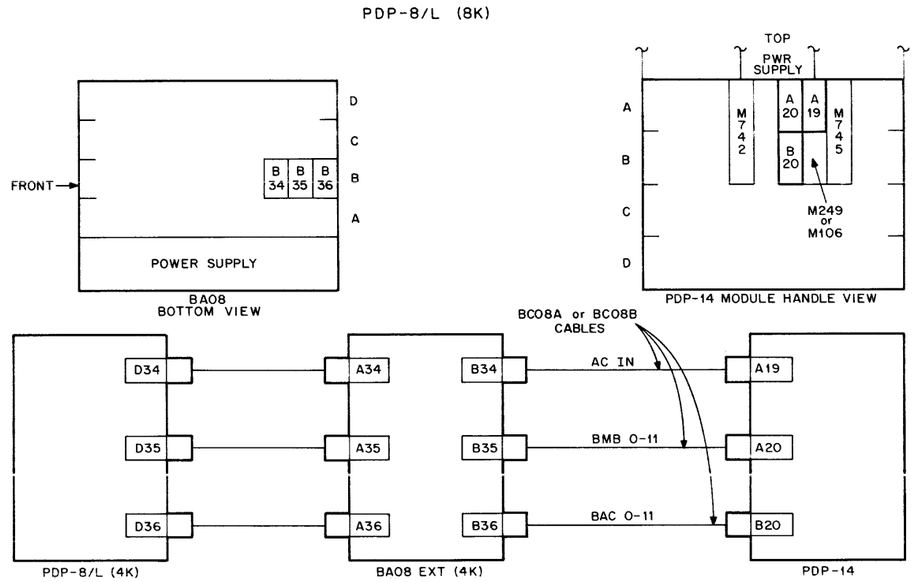
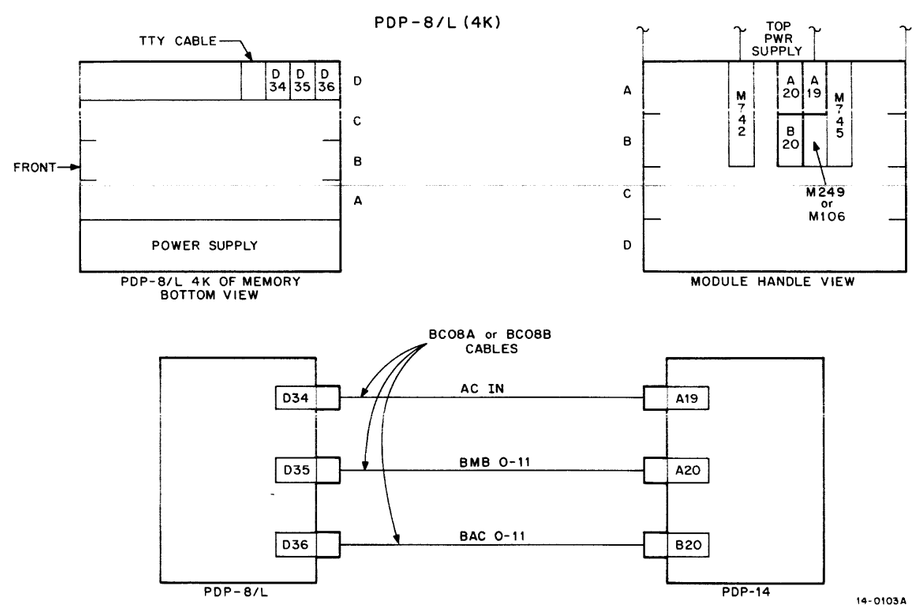


Figure 2-13 M921 Connections for a Device Code of 16_8 or 17_8







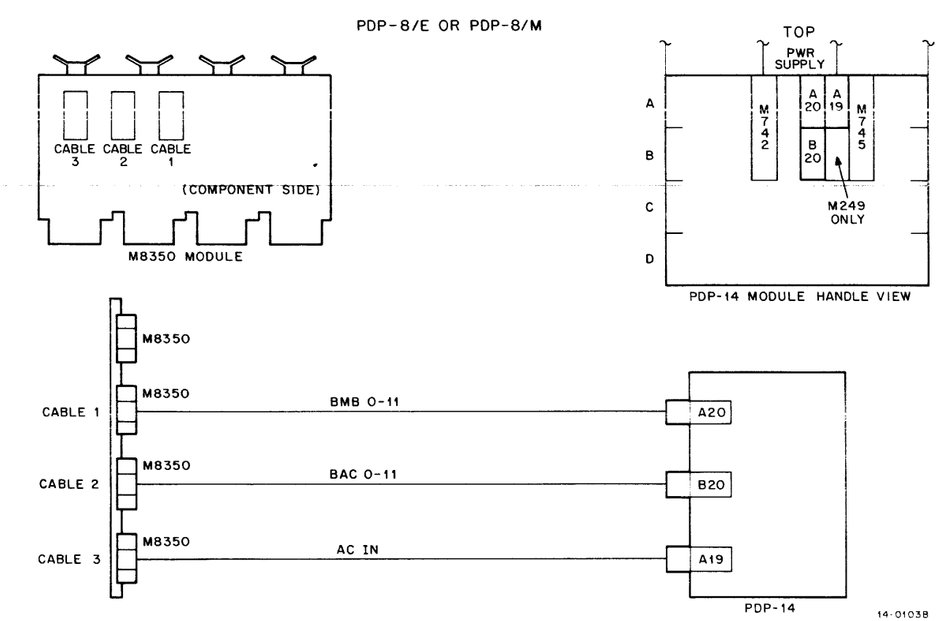
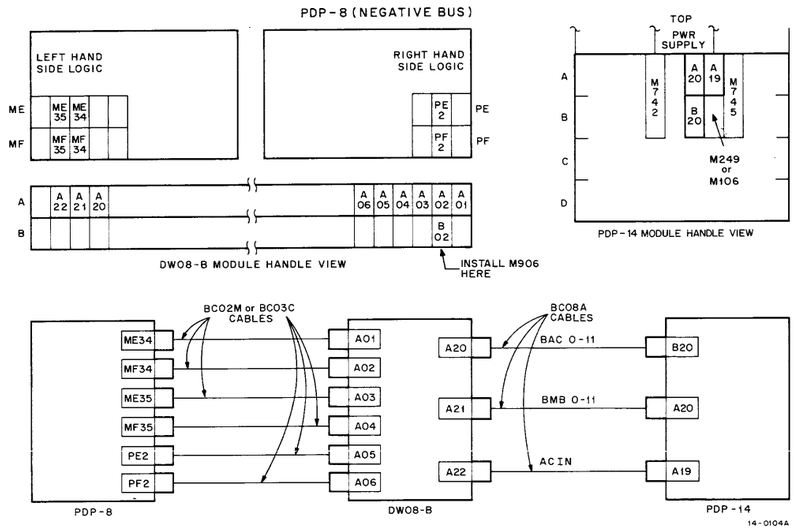
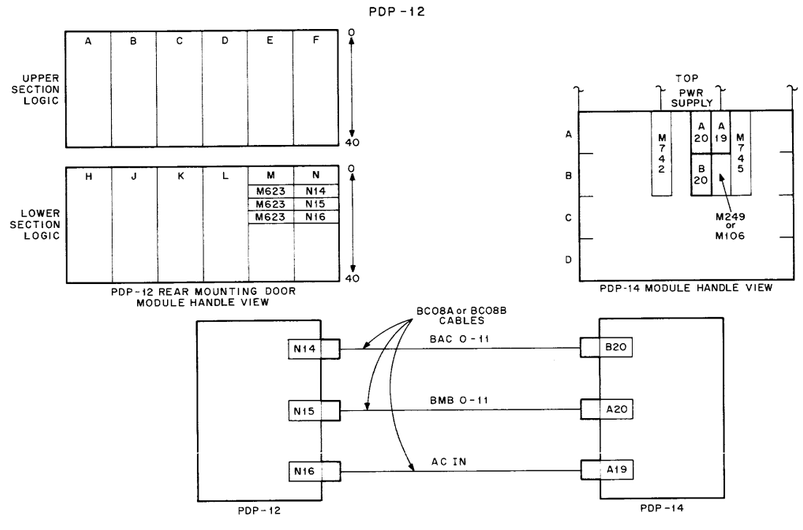
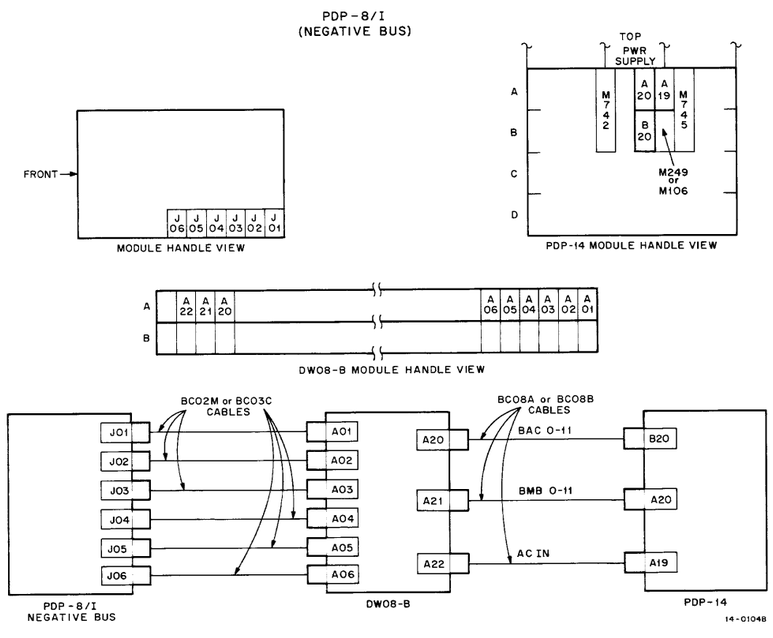


Figure 2-14 PDP-14 Cabling (Sheet 1 of 2)







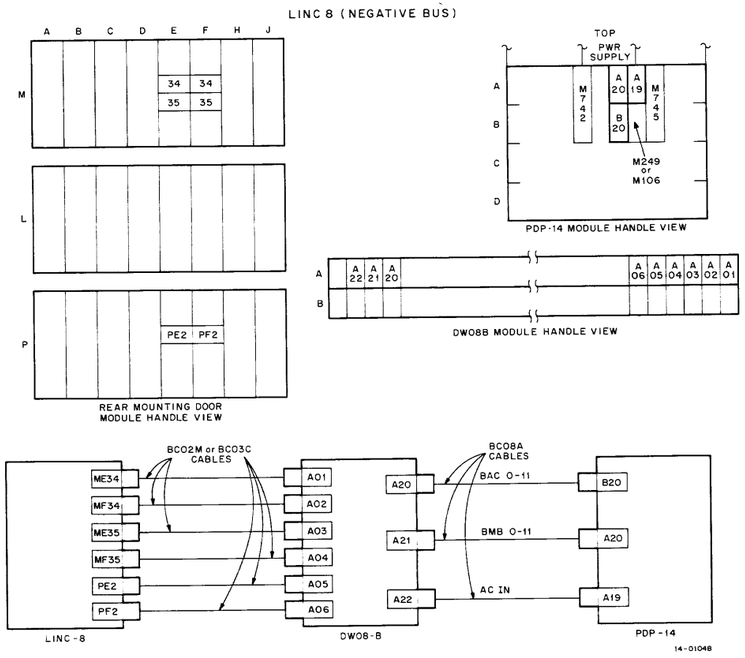


Figure 2-14 PDP-14 Cabling (Sheet 2 of 2)

2.4.3 Loading of Binary (BIN) Loader Tape (DEC-08-LBAA-PM)

Toggle in the Read-In Mode (RIM) Loader for the low-speed paper-tape reader (33 ASR Teletype® or equivalent) or the high-speed paper-tape reader (PC04, PC05, PR-8/I or equivalent) as applicable:

1. Turn on computer.
2. Set up starting address 111 111 101 110 (octal 7756) in the computer's switch register (SR), then press LOAD ADDR switch*. (Refer to Chapter 10 of the *PDP-14 User's Manual* for a description of the computer's front panel and the octal numbering system.)
3. Set first instruction in SR for low- or high-speed reader (as applicable) using the information in Table 2-3. Then depress DEP key.

Table 2-3
RIM Loader

Low-Speed Reader			High-Speed Reader		
Address	Instruction		Address	Instruction	
7756	110 000 011 010	(6032_8)	7756	110 000 001 100	(6014_8)
7757	110 000 011 001	(6031)	7757	110 000 001 001	(6011)
7760	101 011 101 111	(5357)	7760	101 011 101 111	(5357)
7761	110 000 011 110	(6036)	7761	110 000 001 110	(6016)
7762	111 001 000 110	(7106)	7762	111 001 000 110	(7106)
7763	111 000 000 110	(7006)	7763	111 000 000 110	(7006)
7764	111 101 001 000	(7510)	7764	111 101 001 000	(7510)
7765	101 011 101 111	(5357)	7765	101 011 111 100	(5374)
7766	111 000 000 110	(7006)	7766	111 000 000 110	(7006)
7767	110 000 011 001	(6031)	7767	110 000 001 001	(6011)
7770	101 011 110 111	(5367)	7770	101 011 110 111	(5367)
7771	110 000 011 100	(6034)	7771	110 000 001 110	(6016)
7772	111 100 010 000	(7420)	7772	111 100 010 000	(7420)
7773	011 111 111 110	(3776)	7773	011 111 111 110	(3776)
7774	011 011 111 110	(3376)	7774	011 011 111 110	(3376)
7775	101 011 101 110	(5356)	7775	101 011 101 111	(5357)

4. Repeat Step 3 for each remaining instruction.
5. To verify RIM was loaded correctly:
   a. Set SR to 7756_8
   b. Depress LOAD ADDR
   c. Depress EXAM
   d. Compare MB contents with the first instruction in Table 2-3. (For PDP-8/E, set selector switch to MD position.)
   e. Repeat Steps c and d for remaining instructions.
6. If an instruction was loaded incorrectly, set SR to the address of the instruction then press LOAD ADDR. Next, set SR for "correct instruction content," then depress DEP.
7. After verifying RIM is correctly loaded, set SR to 7756_8, then depress LOAD ADDR.
8. Insert Binary (BIN) Loader tape in applicable paper-tape reader.
9. Turn on reader and depress START.
10. If tape stops before completion, restart tape at beginning.
11. After binary tape is loaded, depress STOP, turn off reader and remove tape.

®Teletype is a registered trademark of Teletype Corporation.
*PDP-8/I – If top of SR switch is out, the bit is a binary 1; otherwise it is a binary 0.
PDP-8/L or PDP-8/E – If SR switch is up, the bit is a binary 1; otherwise it is a binary 0.

2.4.4 Loading of Diagnostic Tapes

The following procedures can be used to load all diagnostic tapes (TEST-14, VER-14, LOAD-14, ABE-14, or ROL-14):

1. Turn on computer and depress STOP key.
2. To address the Binary (BIN) Loader program, set 7777_8 into SR. The correct switch configuration for this number is:
   111 111 111 111
3. Press LOAD ADDR key.
4. Load diagnostic tape into applicable paper-tape reader.
5. For high-speed reader, set SR0 to 0. For low-speed reader, leave SR0 set to 1.
6. With reader on, depress START key.
7. When tape stops, verify that the computer's accumulator (AC) contains all 0s (all AC indicators off). This condition denotes that the tape was loaded correctly. If AC contains all 0s, remove tape and turn off reader. If not, reattempt loading. If error still occurs, the tape is bad, the equipment is malfunctioning, or the Binary Loader is not properly loaded.

2.4.5 Control Unit Fault Isolation Using TEST-14

Test Summary – This test checks all the functions performed by the Control Unit except those performed for the I/O interface. It includes testing of the computer interface, timing, register transfers, etc.

Requirements and Limitations – This test requires only that the computer be operating properly.

Test Setup – The following procedures ready the PDP-14 and the computer for testing. If the computer is an integral part of the system and the BIN Loader is maintained in the computer's memory, this part can usually be skipped. To set up the equipment:

1. If necessary, connect the PDP-14 to the computer using the instructions in Paragraph 2.4.2.
2. If necessary, toggle in RIM Loader and load the binary tape loader using the instructions in Paragraph 2.4.3.
3. If necessary, load TEST-14 diagnostic tape using the instructions in Paragraph 2.4.4.

Procedures – To run TEST-14:

1. If necessary, turn on computer, teleprinter, and PDP-14.
2. Depress computer STOP key.
3. Address TEST-14 program by setting SR to 0200_8, then press LOAD ADDR key. The switch settings for 0200_8 are:
   000 010 000 000

(continued on next page)

4. Define the test operation by setting the SR as follows. If Control Unit C20 and D20 module slots are empty, set SR to:

0 1 2	3 4 5	6 7 8	9 10 11
0 0 0	0 0 0	1 0 0	0 0 0

If C20 and D20 contain modules, set SR to:

000 000 000 000

The program responds to SR bits 0 through 6 as follows:

SR	Selection	Action
0	1	Loop on Current Test
	0	Don't Loop
1	1	Don't Halt on Error
	0	Halt on Error
2	1	Don't Print Errors
	0	Print Errors
3	1	Long Test
	0	Short Test
4	1	Repeat All Tests
	0	Stop at End of Tests
6	1	Spare Register Not Plugged In
	0	Spare Register is Plugged In

5. Press START key on computer. The program responds by typing:

HOW MANY I BOXES?

6. Respond to this query by typing the number 0, then press the carriage return (RETURN) key.

7. The program then types:

HOW MANY O BOXES?

Respond by typing the number 0, then press the RETURN key.

8. The program then types:

HOW MANY HALF S BOXES?

Respond to this query by typing the number 0, then press the RETURN key.

9. The program then begins testing the PDP-14 Control Unit. If the Control Unit is operating correctly, the program types the following in 1.5 to 2 minutes:

PASS 1 COMPLETE

10. If the Control Unit is malfunctioning, the program types an error statement as explained in Step 14.

11. If the program types:

PDP-14 STOPPED

then substitute M741 (module slot AB23) and M742 (module slot AB22).

12. If necessary, restart test program and re-run tests. To do this without redefining the configuration, set SR to 0201_8, then press LOAD ADDR key. The program resumes testing without configuration queries.

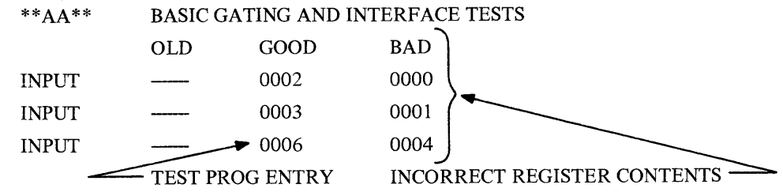
13. If the program types:

PDP-14 HUNG

or computer RUN light goes off, check if 5 Vdc is present at the PDP-14 backplane. Then substitute M741 (module slot AB23) and re-run test by setting SR to 0201_8 and depressing LOAD ADDR key. If this action does not correct fault, re-install original M741 and substitute M745 (module slot AB18). Then re-run test.

14. If the computer detects other malfunctions, it types a 2-letter code (flanked by asterisks) followed by a brief description of the test or defining the failing error condition. This code identifies the module or modules that should be substituted to remedy the malfunction. Table 2-4 lists the error codes, the respective module slots, and the type of module. Where more than one module is listed, substitute first module then re-run test. If this action does not correct fault, restore original module then substitute second module listed and re-run test. Continue this practice until all listed modules have been tried.

15. If the computer detects a register error, the error printout can be as follows:



In the example shown above, the error designator is AA. The operator can go to the module-call table (Table 2-4) and look up AA, or he can analyze the rest of the message. The tests being performed involve some of the basic gating of the PDP-14 and the PDP-8E/8I/8L-to-PDP-14 interface module. The failing register was the Input Register (or possibly the Output Register, as it is impossible to tell at this point in the testing scheme). Since the old contents of the register are not important, there is no entry in that column. The GOOD Column lists the data entered by the test program. The BAD Column lists the incorrect register contents. Analysis of the typeouts indicate a problem with the gating of bit 10.

GOOD Column					BAD Column				
Octal	Binary Equivalent				Octal	Binary Equivalent			
BIT→	0 1 2	3 4 5	6 7 8	9 10 11	BIT→	0 1 2	3 4 5	6 7 8	9 10 11
0002	0 0 0	0 0 0	0 0 0	0 1 0	0000	0 0 0	0 0 0	0 0 0	0 0 0
0003	0 0 0	0 0 0	0 0 0	0 1 1	0001	0 0 0	0 0 0	0 0 0	0 0 1
0006	0 0 0	0 0 0	0 0 0	1 1 0	0004	0 0 0	0 0 0	0 0 0	1 0 0
					Bit 10 does not compare				

16. It is possible that more than one register can be affected in a test. In the example shown below, gating between the Spare Register and PC1 was being tested. Since the data in the Spare Register was destroyed, both registers contained the wrong numbers when the test was completed. The number following the error code is the PDP-14 instruction.

AO	INSTRUCTION		
	0334	(JMR)	TEST
	OLD	GOOD	BAD
SPARE	3642	3642	3600
PC1	0000	3643	3600

(continued on next page)

17. If more information is desired about a malfunction after an error stop, depress computer CONTINUE key. The test then continues until another error stop or the test is completed. If a series of error diagnostics is desired, set SR=1 (continue after error).

18. If no failure has been located with the above program tests, continue testing by performing storage module test, Paragraph 2.4.6.

Table 2-4
Test Program Error Code/Module Location Cross Reference

Error Code Typed	Module Location/ (Type)	Module Function
AA	AB18 (M745)	Computer Interface
	B19 (M106, M249)	Memory Port
	A17 (M746)	Input Reg, 0–05
	B17 (M746)	Input Reg, 06–11
	C17 (M746)	Output Reg, 0–05
	D17 (M746)	Output Reg, 06–11
	C18 (M746)	Memory Buf, 0–05
	D18 (M746)	Memory Buf, 06–11
	AB23 (M741)	Major States and Timing
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AB	C19 (M747)	Program Counter 1, 0–05
	D19 (M747)	Program Counter 1, 06–11
	C18 (M746)	Memory Buf, 0–05
	D18 (M746)	Memory Buf, 06–11
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AC	C21 (M746)	Program Counter 2, 0–05
	D21 (M746)	Program Counter 2, 06–11
	C18 (M746)	Memory Buf, 0–05
	D18 (M746)	Memory Buf, 06–11
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AD	C20 (M747)	Spare Reg, 0–05
	D20 (M747)	Spare Reg, 06–11
	C18 (M746)	Memory Buf, 0–05
	D18 (M746)	Memory Buf, 06–11
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AE	Same as **AB**	—
AF	Same as **AD**	—
AG	Same as **AB**	—
AH	Same as **AD**	—
AI	AB18 (M745)	Computer Interface
	B19 (M106, M249)	Memory Port
	AB23 (M741)	Major States and Timing
	C19 (M747)	Program Counter 1, 0–05
	D19 (M747)	Program Counter 1, 06–11
	C18 (M746)	Memory Buf, 0–05
	D18 (M746)	Memory Buf, 06–11
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AJ	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AK	Same as **AJ**	—
AL	Same as **AJ**	—
AM	Same as **AJ**	—
AN	Same as **AJ**	—
AO	Same as **AJ**	—
AP	Same as **AJ**	—
AQ	Same as **AJ**	—
AR	AB23 (M741)	Major States and Timing
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AS	AB23 (M741)	Major States and Timing
	CD22 (M744)	Comparator
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AT	Same as **AJ**	—
AU	Same as **AJ**	—

Table 2-4 (Cont)
Test Program Error Code/Module Location Cross Reference

Error Code Typed	Module Location/ (Type)	Module Function
AV	Same as **AJ**	—
AW	CD22 (M744)	Comparator
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
AX	Same as **AJ**	—
AY	Same as **AJ**	—
AZ	Same as **AJ**	—
BA	Same as **AJ**	—
BB	Same as **AJ**	—
BC	Same as **AJ**	—
BD	Same as **AJ**	—
BE	Same as **AJ**	—
BF	Same as **AJ**	—
BG	Same as **AJ**	—
BH	CD24 (M743)	I/O Interface
	AB22 (M742)	Switch and Pwr Control
	AB23 (M741)	Major States and Timing
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
BI	Same as **BH**	—
BJ	CD24 (M743)	I/O Interface
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
BK	Same as **BJ**	—
BL	Same as **BH**	—
BM	AB22 (M742)	Switch and Pwr Control
	CD24 (M743)	I/O Interface
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
BN	Same as **BH**	—
BO	AB23 (M741)	Major States and Timing
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
BP	Same as **BO**	—
BQ	Same as **BH**	—
BR	Same as **BO**	—
BS	Same as **BH**	—
BT	Same as **BO**	—
BU	Same as **BO**	—
BV	Same as **BJ**	—
BW	Same as **BO**	—
BX	Same as **BH**	—
BY	Same as **BH**	—
BZ	Same as **BJ**	—
CA	Same as **BJ**	—
CB	Same as **BH**	—
CC	Same as **BH**	—
CD	AB18 (M745)	Computer Interface
	B19 (M106, M249)	Memory Port
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11
CE	C19 (M747)	Program Counter 1, 0–05
	D19 (M747)	Program Counter 1, 06–11
	AB22 (M742)	Switch and Pwr Control
	AB24 (M740)	Instruction Decoder
	C23 (M746)	Instruction Reg, 0–05
	D23 (M746)	Instruction Reg, 06–11

2.4.6 Control Unit I/O Interface Fault Isolation Using TEST-14

Test Summary – This test checks the I/O interface and I/O timing functions for the Control Unit.

Requirements and Limitations – This test requires that the Control Unit be able to pass the tests in Paragraph 2.4.5. In addition, an M232 Storage module is a necessary item for this test.

Test Setup – The following steps ready the PDP-14 and the computer for testing:

1. If necessary, connect the PDP-14 to the computer using the instructions in Paragraph 2.4.2.
2. If necessary, toggle in RIM Loader and load binary tape loader using the instructions in Paragraph 2.4.3.
3. If necessary, load the TEST-14 diagnostic tape using the instructions in Paragraph 2.4.4.
4. Tag all I, O, and A Box cables at Control Unit end, then disconnect all I, O, and A Box cables at Control Unit end.
5. Insert an M232 Storage module in module slot C32 (the first O Box cable slot).

Procedure – To run TEST-14:

1. If necessary, turn on computer, teleprinter, and PDP-14.
2. Depress computer STOP key.
3. To address the TEST-14 program, set SR to 0200_8, then press the LOAD ADDR key.
4. To define the test operation, set the SR as follows. If Control Unit module slots C20 and D20 are empty, set SR to:

   000 000 100 000

   If C20 and D20 contain modules, set SR to:

   000 000 000 000

   The program responds to SR bits 0 through 6 as follows:

SR	Selection	Action
0	1	Loop on Current Test
	0	Don't Loop
1	1	Don't Halt on Error
	0	Halt on Error
2	1	Don't Print Errors
	0	Print Errors
3	1	Long Test
	0	Short Test
4	1	Repeat All Tests
	0	Stop at End of Tests
6	1	Spare Register Not Plugged In
	0	Spare Register is Plugged In

5. Press START key on the computer. The program responds by typing:

   HOW MANY I BOXES?

6. Answer this query by typing the number 0, then press the carriage return (RETURN) key.
7. Computer then types:

   HOW MANY O BOXES?

   Respond by typing the number 0, then press the RETURN key.
8. Computer then types:

   HOW MANY HALF S BOXES?

   Respond to this query by typing the number 1, then press the RETURN key.
9. The program automatically begins testing the Control Unit and the I/O interface. If they are both operating correctly, the computer types the following in approximately two minutes:

   PASS 1 COMPLETE
10. If the I/O interface is malfunctioning, the computer types out an error message such as:

    BH SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0000
    BH SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0001
    BH SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0002
    BH SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0003

    The above example indicates a problem in the I/O interface of the PDP-14. The operator can refer to the module-call table (Table 2-4) for error BH after reading this message, or he can further analyze the message.
11. When testing is complete, turn off the PDP-14, remove M232 Storage module, and reconnect I/O cables. If necessary, continue fault isolation using the procedures in Paragraph 2.4.7.

2.4.7 Output Fault Isolation Using TEST-14

Test Summary – This test is performed only if a fault prevails but cannot be located with the tests in Paragraphs 2.4.5 and 2.4.6. This text exercises all O Box functions except the output drivers.

Requirements and Limitations – This test requires that the O Box 115 Vac (or dc output voltage) be disconnected to prevent equipment damage.

Test Setup – The following steps ready the PDP-14 and the computer for testing:

1. If necessary, connect the PDP-14 to the computer using the instructions in Paragraph 2.4.2.
2. If necessary, toggle in RIM Loader and load the binary tape loader using the instructions in Paragraph 2.4.3.
3. If necessary, load TEST-14 into the computer using the instructions in Paragraph 2.4.4.
4. Turn off and disconnect 115 Vac (or dc) for output drivers.
5. Tag all I, O, and A Box cables at Control Unit end, then disconnect all I and A Box cables at Control Unit end.
6. Insert all O Box cables and M232 modules in the first O Box cable slots of the Control Unit.

Procedures – To run TEST-14:

1. If necessary turn on computer, teleprinter, and PDP-14.
2. Depress computer STOP key.
3. To address the TEST-14, set SR to 0200_8, then press LOAD ADDR key.

(continued on next page)

4. Select the desired operation for the test using SR0 through SR6 as follows:

SR	Set As	Action
0	1	Loop on Current Test
	0	Don't Loop
1	1	Don't Halt on Error
	0	Halt on Error
2	1	Don't Print Errors
	0	Print Errors
3	1	Long Test
	0	Short Test
4	1	Repeat All Tests
	0	Stop at End of Tests
6	1	Spare Register Not Plugged In
	0	Spare Register is Plugged In

5. Press computer START key. The program responds by typing:

   HOW MANY I BOXES?

6. Respond to this query by typing the number 0, then press the RETURN key.

7. The program then types:

   HOW MANY O BOXES?

   Respond to this query by typing the number 0, then press RETURN key.

8. The program then types:

   HOW MANY HALF S BOXES?

   Respond to this query by typing the total number of O Boxes and M232 Storage modules in use, then press the RETURN key.

9. The program then begins testing the PDP-14. If the Control Unit, I/O interface and O Boxes are operating correctly, the program types the following message in one to two minutes:

   PASS 1 COMPLETE

10. If an O Box is malfunctioning, the program types out an error message such as:

    BH SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0000
    BH SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0001
    BH SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0002
    BH SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0003

11. The above example denotes a problem in either the O Box or the I/O interface. However, since the I/O interface has already been checked, the fault must be in the O Box.

12. Substitute the O Box modules related to the malfunction beginning with the level 2 module first (see Figure 2-3 for O Box hierarchy).

13. If this action does not correct fault, restore original module, then substitute next higher level. If this action does not correct fault, continue with next higher level.

14. If all higher level items have been substituted and the fault is still not corrected, turn off 115 Vac (or dc source) to O Box and substitute output driver related to fault.

15. If all modules have been substituted without correction of fault, substitute O Box.

2.4.8 ROM Fault Isolation Using VER-14 (MAINDEC-14-D1AB-D)

Test Summary – This diagnostic test compares the contents of the ROM with information that defines what the ROM should contain. Sequential address tests are performed first, then random address tests are implemented to verify ROM operation and content. The diagnostic program provides error halts and error messages in the same manner as for TEST-14.

A user-furnished paper tape defines what instructions the ROM should contain. This tape is normally generated during initial programming and is updated to reflect any ROM changes. The content of this tape is entered into the computer's memory using a LOAD-14 tape; i.e., the user enters LOAD-14 into memory and uses this program to enter the user's ROM tape. The information content of the ROM tape is always unique; therefore, verify that the tape is the correct one for the ROM you are checking.

Requirements and Limitations – This test requires that the Control Unit be able to run TEST-14 (exçluding input/output tests).

Test Setup – The following procedures ready the PDP-14 and the computer for testing:

1. If necessary, connect the PDP-14 to the computer using the instructions in Paragraph 2.4.2.
2. If necessary, toggle in RIM Loader and load binary tape loader using the instructions in Paragraph 2.4.3.
3. To enter LOAD-14 tape:
   a. Turn on computer and depress STOP key.
   b. To address the BIN loader program set SR to 7777_8.
   c. Press LOAD ADDR key.
   d. Place LOAD-14 tape in applicable paper-tape reader.
   e. For high-speed reader, set SR0 to 0. For low-speed reader, leave SR0 set to 1.
   f. With reader on, depress START key.
   g. When tape stops, verify that the computer's accumulator (AC) contains all 0s, then remove tape.
4. To enter ROM tape:
   a. Address LOAD-14 tape by setting SR to 7400_8 and depressing LOAD ADDR.
   b. Select the applicable paper-tape reader. For high-speed reader, set SR0 to 0. For low-speed reader, leave SR0 set to 1.
   c. Load tape into applicable reader, then depress START.
   d. When tape loading is complete, remove tape and turn off reader.

Procedure – To load and use VER-14, proceed as follows:

1. Load VER-14 using the instructions in Paragraph 2.4.4.
2. Address VER-14 by setting SR to 6000_8, then depressing LOAD ADDR.
3. Select the memory bank to be tested using the following:

SR0	SR1	BANK
0	0	First Bank
0	1	Second Bank
1	0	Third Bank
1	1	Fourth Bank

(continued on next page)

4. Set SR10 and SR11 to 0. (See following for the program operation selected)

SR10	
1	Loop on Data Error
0	Don't Loop on Data Error
SR11	
1	Don't halt on Data Error
0	Halt on Data Error

5. Turn off PDP-14, then power up PDP-14 while holding START/STOP switch at STOP.
6. Depress computer START key.
7. Depress PDP-14 START/STOP switch to START. The program now begins testing.
8. If the ROM content and operation are correct, the program rings the teleprinter bell after each program pass.
9. If the ROM content or operation is incorrect, the program types out an error message, then halts.
10. Error messages can be for either the sequential or random address tests as shown below:

SEQUENTIAL ADDRESS TEST

ADDR	GOOD	BAD
0470	2457	0000
0471	2031	0000
0472	1075	0000
0473	1657	0000
0474	5477	0000
0475	3056	0000
0476	0344	0000
0477	3456	0000

See Note 2 Below

RANDOM ADDRESS TEST

ADDR	GOOD	BAD
0061	2425	0425
0071	3177	1177
0101	**2061**	0061
0111	**3561**	2561
0121	**7015**	5015
0131	**3172**	1172
0141	**2525**	0525
0171	**2617**	0617
6261	**2225**	0225

See **Note 3 Below**

NOTES

1. The first column defines the address, the second (GOOD) denotes the program entry, and the third (BAD) the result read for the program entry.
2. In the sequential address test, addresses 0470–0477 are bad. This could be caused by an open wire (number 47 in this example) on the G922 module or by an open transistor on the G924 module.
3. In the random address test, bit 1 is being dropped. This could be caused either by a transformer on the G923 module or by the integrated circuit associated with that transformer.

2.4.9 Accessory Box Fault Isolation Using ABE-14 (MAINDEC-14-D8AB-D)

Test Summary – This diagnostic checks the timer and retentive memory functions performed by A Box circuits. Each A Box must be checked individually. The content of an A Box is defined during the test so that the program can perform a timer or retentive memory test. For each timer, the program types out its delay interval. Each retentive memory is checked for a power-down and power-up sequence. Upon successful completion of the test, the teleprinter bell rings. Error messages and error stops are provided for malfunctions.

Requirements and Limitations – This test requires that the Control Unit is able to successfully complete its portion of TEST-14.

Test Setup – The following procedures ready the PDP-14 and the computer for testing:

1. If necessary, connect the PDP-14 to the computer using the instructions in Paragraph 2.4.2.
2. If necessary, toggle in RIM Loader and then load binary tape loader using the instructions in Paragraph 2.4.3.
3. If necessary, load ABE-14 tape using the instructions in Paragraph 2.4.4.

Procedure – To test an Accessory Box using ABE-14:

1. Turn on computer, teleprinter, and PDP-14.

NOTE

Reset all retentive memories before beginning test. Ensure K272 memories are not latched (switch is in center position) and that A Box (with K272 modules) is in upright position.

2. To address ABE-14 program, depress computer STOP key. Set SR to 0200_8, then depress LOAD ADDR key.
3. Select program operation using the following (usually, the SR is set to 0000_8):

SR	Set As	Action
0	1	Loop on Current Test
	0	Don't Loop
1	1	Don't Halt on Error
	0	Halt on Error
2	1	Don't Print Errors
	0	Print Errors
3	1	Repeat Timing of Current Output (allows timer adjustment)
	0	Don't Repeat Timing of Current Output

4. Depress computer START key. Program then types:

   A BOX IS CONNECTED TO SLOT

5. Respond to this statement by typing the connector slot letter for the A Box. (Refer to Figure 2-1 for connector slot designations and locations.)
6. The program then types:

   IDENTIFY THE HARDWARE ASSOCIATED WITH EACH ADDRESS BY TYPING
   T FOR TIMER, M FOR RETENTIVE MEMORY, ALL ELSE EMPTY
   0000

7. Using Figure 2-4 as a guide for relative addresses, type:

   T if module slot A04 contains a K302 or K022
   M if module slot A04 contains a K274 or K272
   0 if module slot A04 is empty

NOTE

K272 Retentive Memory modules have only one memory circuit and use only the even numbered relative address for a module slot. For a K272 module, answer "0" for the second (odd-numbered) address. K274 modules have two memory circuits and use both relative addresses.

(continued on next page)

8. Program replies by typing:

   0001

9. Respond by typing T, M, or 0 for relative address 0001.

10. Continue until the A Box configuration is defined. After the reply for address 0017_8, the program is automatically run.

11. For each address having a correctly operating timer, the program checks the timer interval and types it on the teleprinter. An example follows:

    OUTPUT 0000 SET ON IN ABOUT 00000010 MILLISECONDS
    OUTPUT 0001 SET ON IN ABOUT 00004980 MILLISECONDS
    OUTPUT 0006 SET ON IN ABOUT 00000203 MILLISECONDS
    OUTPUT 0007 SET ON IN ABOUT 00032513 MILLISECONDS

12. For each address containing a faulty timer, retentive memory, or storage module, the program types an error message such as the one that follows. Refer to Table 2-5 for modules to be substituted for error codes.

    CH TIME OUT ERROR, OUTPUT 0000

    NOTES

    1. For additional information on the fault, depress computer CONTINUE key.
    2. ABE-14 currently tests timers up to a maximum of 61 seconds. The following locations can be changed once ABE-14 is loaded to extend the timing capability of ABE-14.

Location	Change To	Was
0060	7665	7761
0626	1363	1046
0763	0113	0000

13. For each address containing a correctly operating K022 module, the program denotes the output was set on immediately. An example follows.

    OUTPUT 0010 SET ON IN ABOUT 00000000 MILLISECONDS
    OUTPUT 0011 SET ON IN ABOUT 00000000 MILLISECONDS

14. For each address containing a correctly operating memory circuit, the program types a message such as:

    OUTPUT 0010 SET ON IN ABOUT 00000000 MILLISECONDS
    OUTPUT 0011 SET ON IN ABOUT 00000000 MILLISECONDS
    OUTPUT 0012 SET ON IN ABOUT 00000000 MILLISECONDS
    OUTPUT 0013 SET ON IN ABOUT 00000000 MILLISECONDS

15. After successfully completing this phase, the program tests each retentive memory for retaining its on state through a power-down, power-off, and power-up sequence. For this test, it types:

    POWER DOWN THE PDP-14, THEN POWER IT UP AGAIN, DEPRESS PDP-8 CONTINUE

16. This test is repeated to determine if each retentive memory retains its off state. Hence, the above message is repeated.

17. If a retentive memory malfunctions, the program types an error message such as the following. Table 2-5 defines the A Box modules to be substituted for the error codes.

    POWER DOWN THE PDP-14, THEN POWER IT UP AGAIN, DEPRESS PDP-8 CONTINUE
    CG ONE LOST IN POWER SHUTDOWN BY RM0013

18. The teleprinter bell rings when the A Box test is complete.

Table 2-5
Accessory Box Module/ABE-14 Error Code Cross Reference

ABE-14 Error Code	Accessory Box Module Type
BL **BN** **BQ** **BX** **BY** **CB**	K207, K161, K135
CF **CG**	K302
CH	K272, K274, K022, K302, K207, K161, K135

2.4.10 Fault Isolation Using ROL-14

Test Summary – This program is an on-line program that allows the user to interrogate inputs and outputs, set outputs on or off, and store and type out data entered into the PDP-14 Output Register. The ROL-14 program can be implemented while the PDP-14 is idle or is running a computer or a ROM program. When the PDP-14 is idle, ROL-14 can be used to read a tape from either the high- or low-speed reader.

The following commands and features are available while the PDP-14 is idle or is running a ROM or computer program:

IX, IY	Interrogate a single input (IX) or output (IY) and type its state (0 or 1).
YN, YF	Set a single output on (YN) or off (YF) (Enabled only when SR switch 0 is set on).
C	Clear all outputs, and stop ROL-14 execution of the control program if currently in progress.
SR0 = 1	Enable YN and YF commands.
SR10 = 1	Store and type any numbers loaded into the Output Register.
SR10 = 0	Don't store any further values but type any currently stored.
SR11 = 1	Clear the storage buffer and stop typing Output Register values.

The following commands and features are available while the PDP-14 is *not* running a program:

Sn	Start program at location n.
R	Read a binary tape on the low-speed reader.
RH	Read a binary tape on the high-speed reader.

Test Requirements and Limitations – This test requires that the controller be able to perform at least some of the I/O functions; i.e., the controller does not have a major or complete failure.

The buffer area that stores output words can overlap (and destroy) the Binary Loader; therefore, it is necessary to reload the Binary Loader after using ROL-14 or else relocate the Binary Loader.

The YN and YF commands are enabled only when SR0 is set to 1. This feature provides added protection against unwanted outputs being accidently turned on or off.

Test Setup – The following procedures ready the PDP-14 and computer for using ROL-14:

1. If necessary, connect the PDP-14 to the computer using the instructions in Paragraph 2.4.2.
2. If necessary, toggle in RIM Loader and load the binary (BIN) tape loader using the instructions in Paragraph 2.4.3.
3. If necessary, load ROL-14 using the instructions in Paragraph 2.4.5.

Procedures – To use ROL-14:

1. If necessary, turn on computer, teleprinter, and PDP-14.
2. To address ROL-14, depress computer STOP key, set SR to 7000_8, then depress LOAD ADDR key.
3. Set up SR for the desired program operation using the information in Paragraph 2.4.4.
4. Depress START key. The program is now available for testing.
5. To interrogate an output, type IY followed by the octal address of the output. Then depress the carriage RETURN key. The program responds by typing the state of the output. For an off state, the program types a 0; for an on state, the program types a 1.
6. To interrogate an input, type IX followed by the octal address of the output. Then depress the carriage RETURN key. The program responds by typing the input state (0 for off or 1 for on).
7. To set an output on or off, set SR0 to 1, then type YN (for on) or YF (for off) followed by the octal address of the output. Then depress the carriage RETURN key.

CHAPTER 3
THEORY OF OPERATION

3.1 GENERAL

This chapter contains theory of operation for the PDP-14 Controller in two primary levels: a block diagram level and a detailed level.

3.2 SYSTEM RELATIONSHIPS

3.2.1 Operating Configurations and Modes

The primary operating configurations (or applications) for the controller are described in Chapter 1. To reiterate, a stand-alone application does not normally interface with a computer. A PDP-14 Controller used in a stand-alone application therefore only operates in the internal mode (all instructions provided by the ROM).

A monitoring or a monitoring and control application entails the use of a computer. A controller used in a monitoring or a monitoring and control application can operate in the internal mode (with interrupt operation) or the external mode.

The interrupt operation is basically a cycle-steal operation in which the ROM program is interrupted so that the controller can execute one computer-supplied instruction. After this instruction is executed, the ROM program automatically resumes at the point it left off. The principal use of this operation is to provide test results to the computer on an as-needed basis and to change the operating mode to external.

In the external mode, the computer provides the instructions. To enter the external mode, the computer must request a PDP-14 interrupt and then issue an instruction to enter the external mode. In the external mode, the ROM program is suspended and the computer provides all program instructions. To return to ROM (or internal) operation, the computer must issue an instruction to leave the external mode.

3.2.2 Control Unit Block Diagram Description

3.2.2.1 General – Figure 3-1 shows the major registers, control elements, and interfaces that constitute the Control Unit. For description purposes, mode switching is represented as a double-pole, double-throw, switch. When this switch is placed to the INT position, the Control Unit provides the ROM with a timing input and an address. Thus, the Control Unit fetches instructions from the ROM. When momentarily placed to EXT, an interrupt operation is active. The Control Unit receives one instruction from the computer, then resumes operation with the ROM (switch returns to INT). When placed to EXT and held there, the Control Unit receives its instructions from the computer.

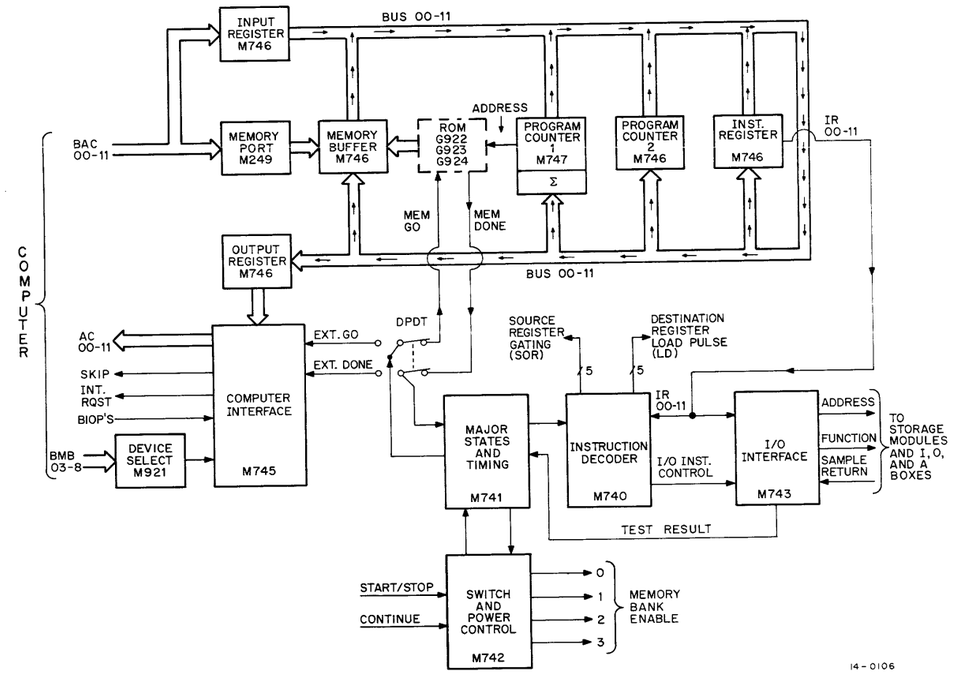


Figure 3-1 PDP-14 Control Unit, Block Diagram

3.2.2.2 Bus Arrangement and Internal Transfers – A 12-bit data transfer bus, designated BUS 00–11, handles the majority of internal transfers. This bus interconnects the major registers shown in Figure 3-1. The inputs of each register are directly connected to BUS 00–11. The outputs, however, are connected to the bus by gating structures on the respective registers. Thus, for a transfer between registers, one register is specified as the source

register and another as the destination. The source register receives an output gating pulse while the destination register receives a load pulse. The contents of a register placed on the bus then can transfer back to the same register by specifying it both as the source and destination. This type of transfer is used for incrementing (or decrementing) of counters. (The decrementing capability is not presently used.) All register transfers are jam-transfers.

3.2.2.3 **Registers** – Table 3-1 lists the Control Unit registers, their source and destination codes, and their major use. The least significant octal digit of a register transfer instruction defines the destination register. The more significant octal digit defines the source register.

Table 3-1
PDP-14 Major Registers

Register	Source Code	Destination Code	Major Use
Dummy (No Register)	$000 = 0_8$	None	Implied register. Can be used for transfer of all 1s into a register.
Instruction Register (IR)	$001 = 1_8$	$001 = 1_8$	Stores the instruction for decoding and execution.
Memory Buffer (MB)	$010 = 2_8$	$010 = 2_8$	Temporary storage for instruction fetched from ROM or entered from computer via Memory Port.
Spare Register (Optional)	$011 = 3_8$	$011 = 3_8$	Utility register; not normally used.
Program Counter 1 (PC1)	$100 = 4_8$	$100 = 4_8$	Stores the address for the next ROM instruction. It is an incrementing-type register used as a counter.
Program Counter 2 (PC2)	$101 = 5_8$	$101 = 5_8$	Stores the return address for a subroutine.
Input Register	$110 = 6_8$	None	Input buffer for data transfer from computer. Its major use is for loading of PC1 or PC2 from the computer.
Output Register	None	$110 = 6_8$	Output buffer for data transfer to the computer.

3.2.2.4 **I/O Interface** – This element, as the name implies, interfaces storage modules and I, O, and A Boxes with the Control Unit. As part of this function, the I/O interface receives IR inputs (specifying the I/O address) and control inputs (denoting the type of instruction) from the instruction decoder. From these inputs, it selects the input or output circuit and initiates the desired function. For Operate instructions, this interface simply specifies the function (SET, RESET, or CLEAR). For Test instructions, the I/O interface also compares the test state with the program-defined state. The result is then temporarily stored for evaluation by a Decision instruction.

3.2.2.5 **Computer Interface** – This functional area interfaces the PDP-14 with a computer I/O bus for programmed data transfers. It has the capabilities for operating with a computer's skip chain or with its program interrupt facility. As part of this interface function, the interface interprets computer input/output transfer (IOT) instructions, selects the operating mode (internal or external), and synchronizes controller operations with the computer for input and output transfers. The interface also provides the capabilities for interrupting ROM operation on a cycle-steal basis so that one computer instruction can be implemented. Data from the computer's accumulator is provided to the MB Register via the Memory Port logic or to BUS 00–11 via the Input Register (Figure 3-1). The interface provides the control for these functions. It also controls the gating of Output Register data to the computer's accumulator.

3.2.2.6 **Control** – The Control Unit uses three major control sections as shown in Figure 3-1. The switch and power control area senses power-up and power-down conditions and initializes the system. For power-up conditions, it also starts Control Unit timing. This control area also interfaces with the START/STOP and CONTINUE switches for manual control functions.

The major states and timing control area provides the basic timing for fetching and executing instructions. It establishes the major states of FETCH and EXECUTE, intermediate time states (TS), and I/O timing. This functional area also contains logic for storing test results and evaluating these results with Decision instructions.

The instruction decoder is the third major control area. It, as the name indicates, decodes the instructions and provides the discrete control signals for executing them. In addition to these control signals, the decoder generates the source gating and destination load strobes for internal transfers.

3.2.3 ROM Block Diagram Description

The ROM is organized in 1024 (1K) word increments called banks. Up to four banks can be used for a total word capacity of 4096. Each bank is a complete functional entity; i.e., it contains all the necessary circuits to retrieve instructions. A bank is selected by the two most significant bits (MSBs) of PC1. These bits are decoded by the switch and power control module (M742). This module then selects the applicable bank. The remaining 10 bits of PC1 select one of 1024 locations within the bank.

The ROM operates asynchronously with the Control Unit. For retrieval of an instruction, the Control Unit addresses the ROM and provides a MEM GO pulse. The ROM, in turn, selects the location and transfers the content of the location in an internal output buffer. The outputs of this buffer then set corresponding bits of the MB Register. Concurrently, the ROM provides a MEM DONE timing output. This pulse denotes the instruction access cycle is complete and signifies an instruction is available. The instruction remains in the MB Register until it is cleared at the start of another instruction access. To access one instruction requires about 450 to 500 nanoseconds, however, this can vary from bank to bank without detriment to system operation since asynchronous timing is used.

3.2.4 I Box Block Diagram Description

For Test and Operate instructions, the I/O interface decodes the IR bits and asserts one of eight package select lines. Each package select line is connected to one I Box and two O Box cable slots. When asserted, the package select line selects one I Box and two O Boxes (or else a combination of O Box, A Box, or storage modules). For selection of circuits within the boxes, the I/O interface provides a 4-bit address selection code. This selection code is provided to all I Box and O Box cable slots.

Figure 3-2 shows the functional relationships of the major elements in an I Box. For selection of the I Box, the package select line is asserted and the 4-bit selection code is provided. The MSB of this code and the package select input are combined to enable one of two binary-to-octal decoders to respond to the three remaining selection code bits. Each decoder selects two input circuits concurrently. If the MSB is asserted, a decoder selects one input circuit in octal group 10 through 17 and one in 30 through 37. If the MSB is not asserted, the second decoder selects one input in octal group 0 through 7 and one in 20 through 27. With this arrangement, two sample return lines are required and the I/O interface must determine which line is to be sampled. For an on input, the selected circuit asserts the sample return line.

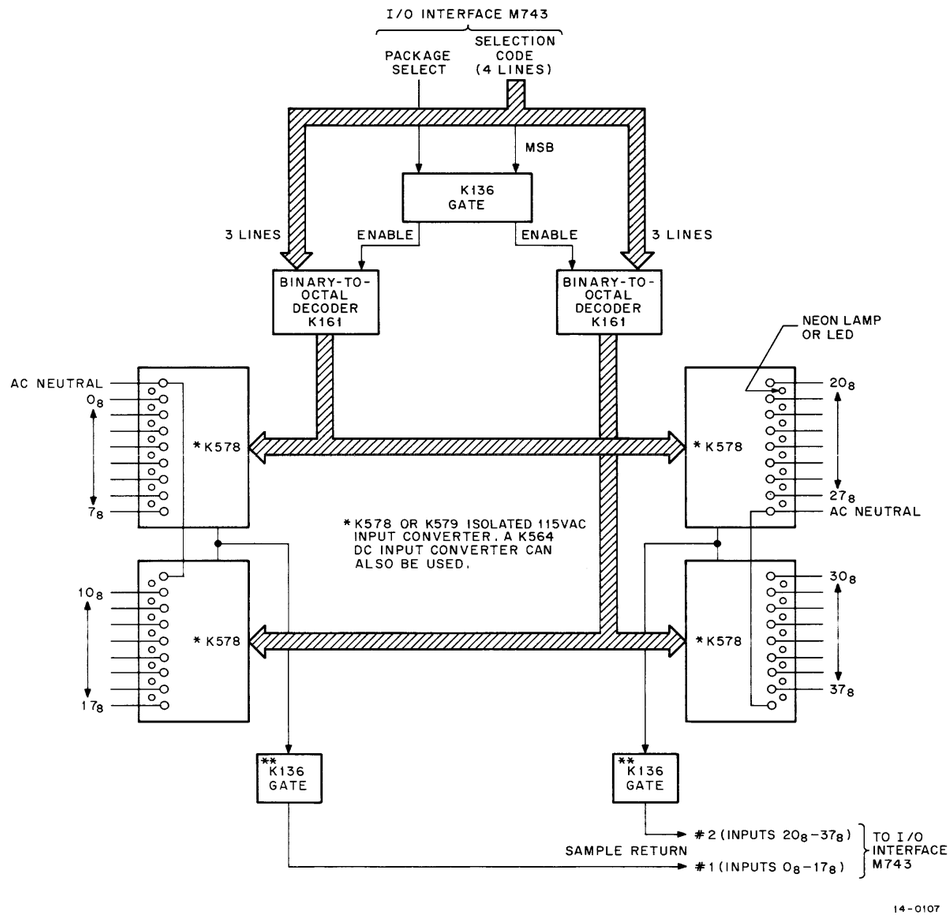


Figure 3-2 I Box Block Diagram

3.2.5 O Box Block Diagram Description

The same circuit selection methods are used for O Boxes as for I Boxes. There is one minor difference, however. Since each O Box (or equivalent) has sixteen outputs and up to sixteen O Boxes can be used, the same number of selection combinations are required for outputs as inputs. However, each asserted package select line selects two O Boxes concurrently. With this arrangement and a 4-bit selection code (common to all O Boxes), two output circuits (one in each of two boxes) are addressed concurrently. Again, two sample return lines are required and the I/O interface must interpret the result for Test instructions. In addition, two sets of function lines (SET and RESET) are required for Operate instructions.

Figure 3-3 shows the functional relationships of the O Box. For a turn on (Operate) instruction, the I/O interface supplies a 4-bit selection code, a package select, and enable set signal. The MSB of the selection code and the package select enable one decoder circuit. The respective decoder, in turn, decodes the remaining three bits of the selection code and selects one of eight flip-flops to perform the designated function. For a turn on function, the respective flip-flop is set to turn on an output. It remains set until reset by an ENABLE RESET or CLEAR (reset for all output flip-flops). With the flip-flop on, the output driver is turned on.

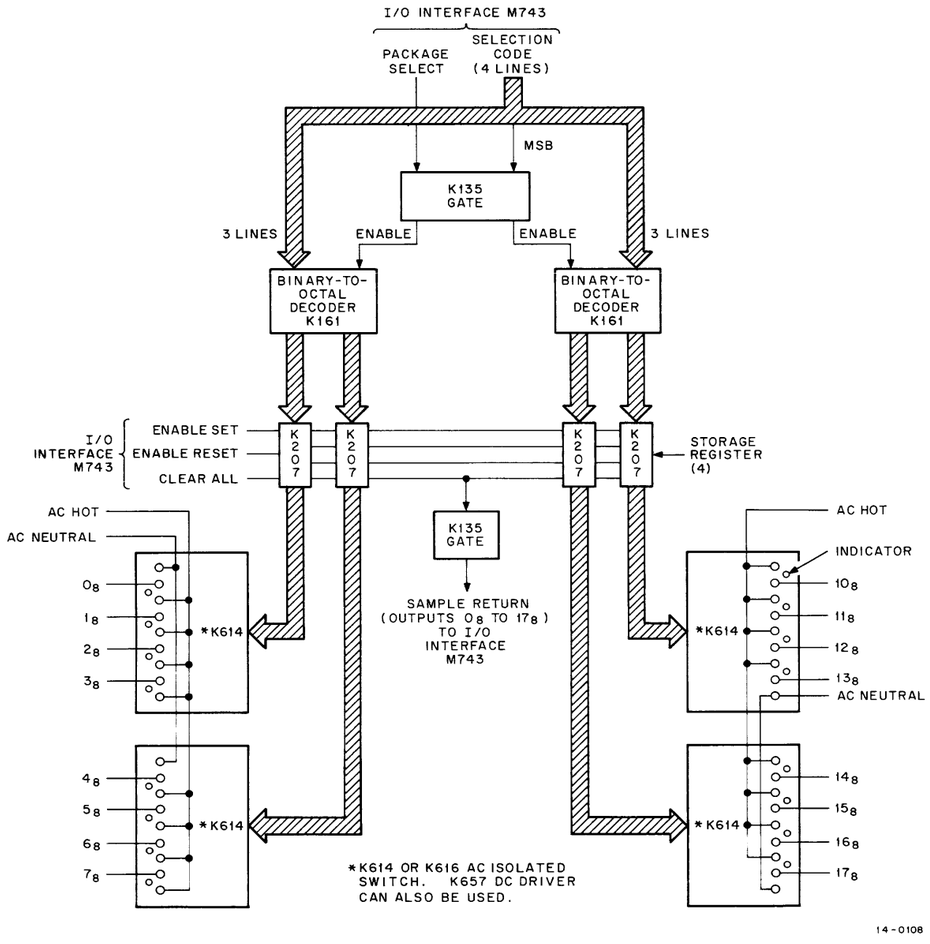


Figure 3-3 O Box Block Diagram

For a Test instruction, the output circuit is addressed in the manner described above. However, the I/O interface does not assert a function line. The address selection simply gates the state of the selected flip-flop to a sample

return line. This line is common to the gated outputs of all 16 flip-flops in a box. The sample return output is provided to the I/O interface for interpretation.

3.2.6 A Box Description

The A Box addressing and function (SET or RESET) structures are identical to those described for the O Box. The A Box, however, is used for special circuits such as timers, retentive memory, or storage elements. Figure 3-4 shows the functional relationships of the A Box.

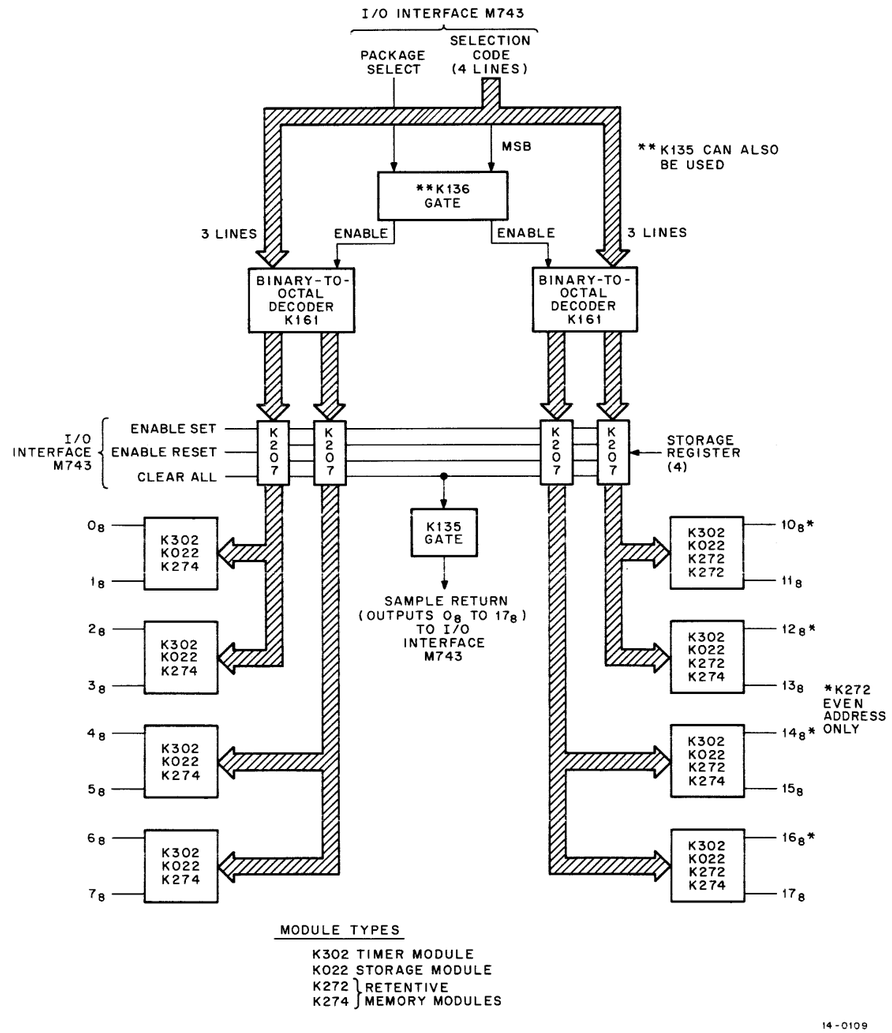


Figure 3-4 A Box Block Diagram

Up to 16 timer circuits can be used. Each circuit can provide a delay interval from approximately 0.01 seconds up to 4 minutes and 45 seconds. A delay interval is started when the flip-flop associated with the timer is set. The timer is not considered on, however, until its delay interval has expired.

Up to 16 retentive memories can be provided in one A Box by using K274 Retentive Memory modules. Each module provides two memory circuits and precludes the use of two timers (or two storage circuits). Each memory circuit has an indicator to denote its state (on or off) and a switch to clear (turn off) the memory.

Up to four retentive memories can be provided in one A Box by using K272 Retentive Memory modules. Each module contains only one memory circuit and precludes the use of two timers (or two storage circuits). Although a K272 module consumes the space normally allotted for two addresses, it can only be addressed by the even-numbered relative addresses for the A Box. Each K272 memory circuit has a switch to clear the memory.

Testing of A Box outputs differs from that of O Boxes. Instead of testing the output state of the control flip-flop (as is done for O Boxes), an A Box test samples the output of the actual output circuit; e.g., the output of a timer or retentive memory.

Unused A Box output slots can be used for storage outputs by using a K022 Storage module. Each module contains two diode gating circuits. Each circuit gates the output of one control flip-flop to the sample return line when selected by the addressing circuits.

3.3 INSTRUCTION SET

3.3.1 General

The PDP-14 Controller uses two basic sets of instructions; one for internal mode (ROM) operation and one for external mode operation. The external mode set includes all of the internal mode instructions plus instructions that control external mode operations. In addition to these instructions, the PDP-14 must recognize and execute input/output transfer (IOT) instructions from the computer.

3.3.2 Internal Mode Instruction Set

3.3.2.1 General – The internal mode instruction set can be divided into five basic classes directly related to the functions performed. These classes are:

a. ***Test*** – Sample input or output state (on or off).

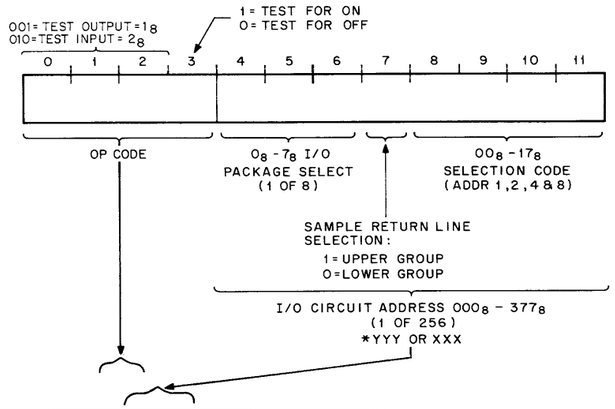
b. ***Decision*** – Jump (or branch) if input or output is in the state defined by the instruction.

c. ***Operate*** – Set output on or off.

d. ***Monitoring*** – These instructions test an input or output and place the test result and other pertinent information in an Output Register for transfer to the computer.

e. ***Housekeeping*** – These instructions, in general, provide the basic address links for performing a program efficiently. These instructions include register transfer and subroutine operations.

3.3.2.2 Test Instructions – Figure 3-5 shows the format of Test instructions. It also lists the symbolic and octal codes and briefly describes the function of each Test instruction. Note that inputs are designated X and outputs are designated Y and that each can be tested for an on or off condition. Also note that test results are held in a common TEST flip-flop used for all input and output testing.



Symbolic Code	Octal Code	Description
TYF	1 0 0 0 + Y Y Y*	Test output for OFF; set TEST flip-flop if output is OFF.
TYN	1 4 0 0 + Y Y Y	Test output for ON; set TEST flip-flop if output is ON.
TXF	2 0 0 0 + X X X*	Test input for OFF; set TEST flip-flop if input is OFF.
TXN	2 4 0 0 + X X X	Test input for ON; set TEST flip-flop if input is ON.

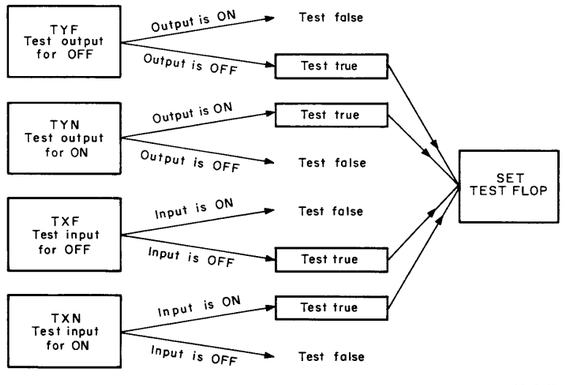
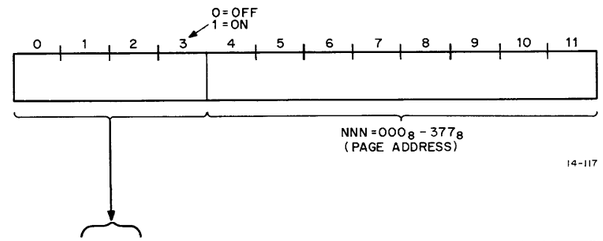
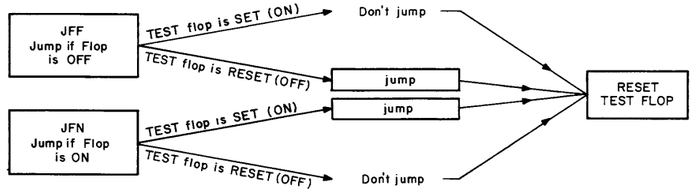


Figure 3-5 Test Instructions

3.3.2.3 Decision Instructions – Two basic Decision instructions are used. Figure 3-6 shows the format of Decision (conditional jump) instructions and defines their codes and function. As mentioned previously, these instructions link the Test instructions with Operate or other Test instructions. Note that the TEST flip-flop can be tested for either an on (SET) or off (RESET) state. Observe also that it is reset (if set) after it is tested, regardless of the test result.



Symbolic Code	Octal Code	Function
JFF	5 0 0 0 + N N N (377 max)	If TEST flip-flop is OFF, jump to location specified by NNN (NNN→PC1); if TEST flip-flop is ON, then clear TEST flip-flop (0→TEST flip-flop).
JFN	5 4 0 0 + N N N (377 max)	If TEST flip-flop is ON, jump to location specified by NNN and reset TEST flip-flop (NNN→PC, 0→TEST FLAG). If TEST flip-flop is OFF, continue with next instruction.

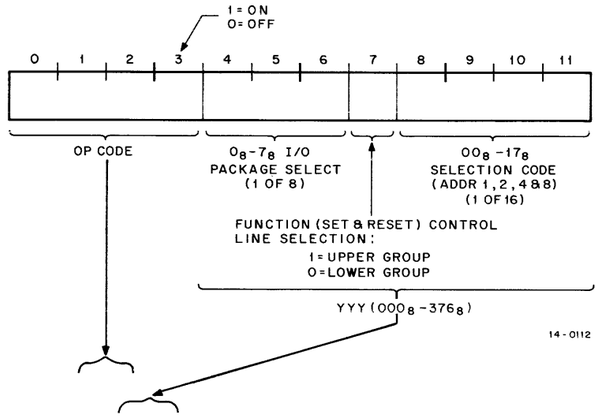


NOTE: All other PDP-14 instructions have *no effect* upon the TEST flip-flop.

14-0116

Figure 3-6 Decision Instructions

3.3.2.4 Operate Instructions – Three basic Operate instructions are used. Figure 3-7 depicts the format of Operate instructions and defines their codes and functions. Note that an output can be turned on or off. Observe that the upper-most output address is used for a clear-all-outputs function, and therefore cannot address a "real" output.



Symbolic Code	Octal Code	Description
SYF	3 0 0 0 + Y Y Y	Set output OFF (interrupt output circuit, clear retentive memory or storage, or turn off timer).
SYN	3 4 0 0 + Y Y Y	Set output ON (complete output circuit, set retentive memory or storage, or start delay timer).
CLR	3 3 7 7	Clear all outputs.

Figure 3-7 Operate Instructions

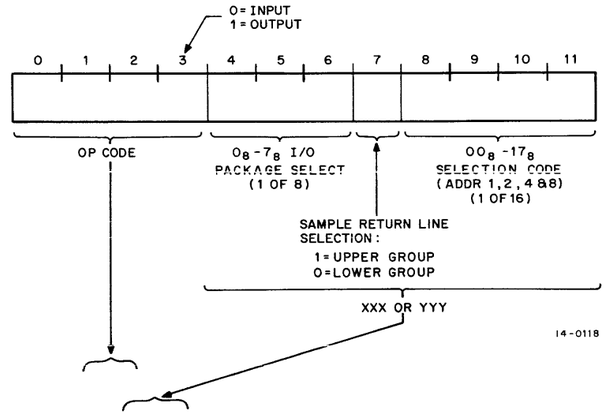
3.3.2.5 Monitoring Instructions – There are two basic Monitoring instructions. Figure 3-8 illustrates the format of these instructions and their associated output words. Observe that each display defines which input or output, whether it is an input or output, the state (on or off) of input or output, and the state of the TEST flip-flop.

3.3.2.6 Housekeeping Instructions – The PDP-14 Controller uses up to nine basic Housekeeping (transfer and minor arithmetic) instructions. Figure 3-9 shows the format of these instructions and defines their content. Note that bits 4 and 5 define the type of operation. (Although a transfer and decrement capability is provided, it is not presently used.) Observe also that bits 6 through 8 define the source register and bits 9 through 11 define the destination register. Further, observe that a skip operation is implemented by transferring the content of PC1 to the transfer bus, incrementing this value, and loading the result back into PC1 (corresponding to a code of 0344_8).

There are two 2-word jump instructions (JMP and JMS) and one 2-word transfer instruction. For jump instructions, the content of the location (NNNN) following the jump instruction defines the jump address. Since this address consists of 12 bits, it can specify any location within a 4096-word ROM; i.e., an unconditional jump can address any memory location. Figure 3-9 also defines the bit structure of the second word for a jump instruction. Similarly, for the 2-word transfer instruction (TRM), the content of the location following the TRM is provided to the Output Register. There are no restrictions on the content of the TRM word.

3.3.3 IOT Instructions

As mentioned previously, the PDP-14 must recognize and execute IOT instructions to communicate with a PDP-8 family computer or PDP-12 computer. Figure 3-10 depicts the format of IOT instructions and defines their use.



Symbolic Code	Octal Code	Description
TXD	7 0 0 0 + X X X	Test Input and Display (test input and place TXD word in Output Register).
TYD	7 4 0 0 + Y Y Y	Test Output and Display (test output and place TYD word in Output Register).

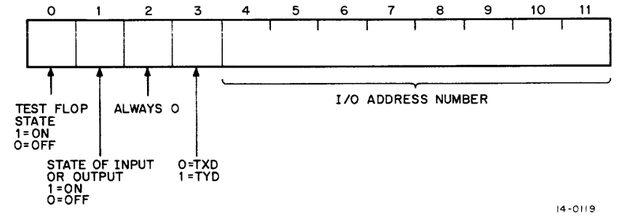
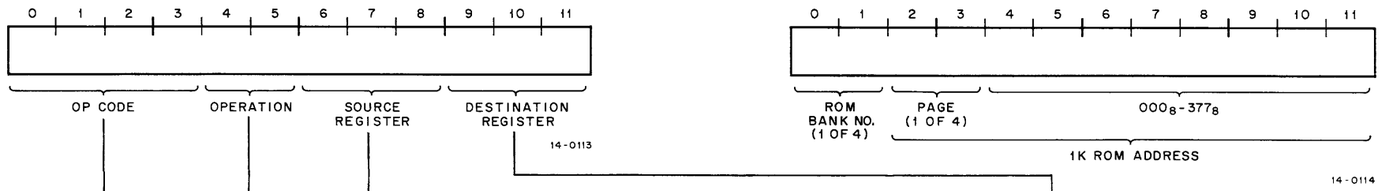


Figure 3-8 TXD and TYD Instructions and Display Words



FORMAT OF SECOND WORD FOR UNCONDITIONAL JUMP INSTRUCTIONS (JMP or JMS)

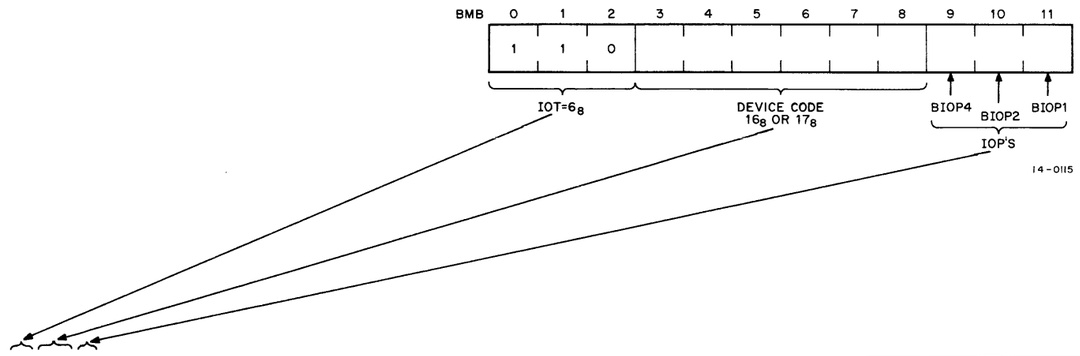
4	5	Operation
0	0	Transfer
0	1	Transfer & Decrement
1	0	Transfer
1	1	Transfer & Increment

Octal	Register
0	Dummy
1	IR
2	Mem Buf
3	Spare Reg
4	PC1
5	PC2
6	Input Reg
7	Not Used

Octal	Register
0	Not Used
1	IR
2	Mem Buf
3	Spare Reg
4	PC1
5	PC2
6	Output Reg
7	Not Used

Symbolic Code	Octal Code	Function
NOP	0 0 0 0	No operation.
SKP	0 3 4 4	Skip next location, PC1+1→PC1.
JMP	4 2 2 4 N N N N	Unconditional jump to location NNNN (2nd word of 2-word instruction in Memory Buffer), MB→PC1.
JMS	4 6 4 5 N N N N	Jump to subroutine at location NNNN (2nd word of 2-word instruction) PC1→PC2, then NNNN→PC1.
JMR	0 3 5 4	Jump return from subroutine (PC2→PC1, PC1+1→PC1).
TRM	4 2 2 6 N N N N	Transfer next memory word to Output Register (PC1+1→PC1, MB→Output Register).
TRR	0 2 X Y	Transfer Register X to Register Y; where X equals Source Register and Y equals Destination Register.
SKZ	6 3 N 4	Skip next location if Register N is equal to zero; if Reg N = 0, PC1+1→PC1.
SKE	6 7 N 4	Skip next location if Register N is equal to contents of PC2. If Reg N = PC2, then PC1+1→PC1.
HALT	0 0 0 7	Halt the PDP-14 Control Unit.

Figure 3-9 Housekeeping Instructions



Symbolic Code	Octal Code	Description
GNI	6 1 6 5	Generate Interrupt – This instruction sets INTERRUPT REQUEST FLAG in the PDP-14, clears EXT FLAG, and transfers BAC00–11 to MB Register upon completion of present PDP-14 instruction. PC1 is not incremented. EXT FLAG is set upon completion and control returns to the ROM. **NOTE** **A GNI can be used with the PDP-14 external mode to provide a memory readout capability for diagnostic purposes. That is, if the GNI provides a TRM, the content of the ROM location specified by PC1 is transferred to the Output Register for examination by the computer.**
LDE	6 1 6 4	Load and Execute – This instruction loads MB Register from BAC00–11 and clears the EXT FLAG. Following this action, the controller transfers the instruction to the IR, increments PC1, then executes the instruction. After execution, the EXT FLAG is set to denote the controller is ready for another action.
CEF	6 1 6 7	Clear EXT FLAG. Used for External operation.
CLF	6 1 7 2	Clear OUTPUT FLAG – The controller sets this flag when data is entered into the Output Register. This instruction also returns an AC CLEAR to the computer. Thus, this instruction can be used as a preparatory instruction for Output Register transfers to the computer.

Symbolic Code	Octal Code	Description
LIR	6 1 6 2	Load Input Register – This instruction loads the information from BAC00–11 into the Input Register. The principle use for this transfer path is for placing an address in PC1 or PC2.
ROR	6 1 7 6	Read Output Register – This instruction gates the contents of the Output Register to AC00–11. It also clears the output flag.
SEF	6 1 6 1	Skip On EXT FLAG – This instruction samples the EXT FLAG. If set, a SKIP pulse is returned to the computer. As a result, the computer skips the next instruction.
SOF	6 1 7 1	Skip On OUTPUT FLAG – This instruction samples the OUTPUT FLAG. If set, a SKIP pulse is returned to the computer to cause it to skip the next instruction.
STF	6 1 7 3	Skip On TEST FLAG – This instruction samples the TEST flip-flop. If set, a SKIP pulse is returned to the computer to cause it to skip the next instruction.
SCR	6 1 7 5	Skip on Controller Running – This instruction samples the RUN flip-flop. If set, a SKIP pulse is returned to the computer to cause it to skip the next instruction.

Figure 3-10 IOT Instructions

3.3.4 External Mode Instructions

In addition to the internal mode operating instructions, the controller can also perform six external mode instructions. These instructions are used for mode control and related operations. The format for external instructions is the same as that for internal mode Housekeeping instructions (Figure 3-9). Table 3-2 describes the function of each external mode instruction.

Table 3-2
External Mode Instructions

Symbolic Code	Octal Code	Description
EEM	0600	Enter External Mode – This instruction sets the EXT MODE flip-flop so that the controller operates with the computer. A generate interrupt (GNI) instruction loads the EEM instruction into the MB Register from the computer's accumulator during the FETCH cycle. During the EXECUTE cycle, the EXT MODE flip-flop is set. Next, the EXT FLAG is set to notify the computer that the PDP-14 is ready for another instruction.
EES	0645	Enter External Mode and Subroutine – This instruction performs the same functions as the EEM instruction and it prepares the controller for a subroutine jump; i.e., the contents of PC1 (next ROM address) is stored in PC2 for return from the subroutine.
LEM	0400	Leave External Mode – This instruction returns the controller to the internal operating mode by resetting the EXT MODE flip-flop. The controller resumes the ROM program at the address specified by PC1.
LER	0454	Leave External Mode and Return From Subroutine – This instruction resets the EXT MODE flip-flop and transfers the contents of PC2 to PC1 so that the ROM program can resume at the place it was interrupted.
TRM	4226 NNNN	Transfer Memory to Output Register – This instruction transfers the contents of the next memory location to the Output Register (via the MB Register) for transfer to the computer.
TRS	4225 NNNN	Transfer Register and Store – This instruction transfers the contents of the next ROM address to PC2 via the MB Register. Since PC2 stores the program return address for subroutines, this instruction can be used to change the return address during the subroutine.

3.4 INSTRUCTION FLOW

3.4.1 General

Drawing D-FD-PDP-14-0-6 (Appendix B) depicts the flow of all instructions. For external mode operation, the machine follows the path labeled EXT MODE (1). Similarly, for a single instruction interrupt, the machine follows the path labeled INTERRUPT (1). For internal or ROM operation, the machine follows the third or unlabeled path; unlabeled lines can also be common to other modes.

The flow diagram consists of two major cycles; FETCH and EXECUTE. During the FETCH cycle, the Control Unit retrieves an instruction from memory (ROM operation) or accepts an instruction from the computer (EXT MODE or INTERRUPT). During the EXECUTE cycle, the Control Unit decodes and executes the instruction. Following this action, the Control Unit can continue operation by obtaining another instruction (either from the ROM or the external computer) or can halt operation if a halt instruction is decoded.

The timing states for the FETCH and EXECUTE cycles are denoted at the left edge of drawing D-FD-PDP-14-0-6. Note that the FETCH cycle is invariable and that it consists of an interval for START cycle, PAUSE, time states 1 and 2 (TS1 and TS2), and END CYCLE. Note also that only part of the EXECUTE cycle uses PAUSE (specifically 2-word instruction such as JMP or TRM).

3.4.2 FETCH Cycle for Internal Mode

When the PDP-14 is operated in the internal mode, instructions are fetched from the ROM. The flow diagram (D-FD-PDP-14-0-6) FETCH cycle shows the major events for this function. First, a START CYCLE pulse initiates a MEM GO pulse. This pulse clears the MB Register (to prepare it for receiving the ROM instruction) and starts memory timing. A short interval is required for the access as denoted in the flow diagram. Upon completion of the access, the ROM transfers the instruction to the MB Register (this is a direct-set operation and requires no gating or load strobe) and generates a MEM DONE pulse.

The MEM DONE pulse advances the timing to TS1 from the PAUSE state. The end of TS1 causes the transfer of the instruction in the MB to the IR. The Control Unit then advances to TS2 and at the end of this time state PC1 is incremented. Next, the Control Unit generates an END CYCLE pulse which sets up the EXECUTE cycle.

3.4.3 FETCH Cycle for Interrupt Mode

For interrupt mode operation, the computer provides a GNI IOT instruction. This instruction sets the INTERRUPT flip-flop, and when synchronization is achieved (next END CYCLE pulse), the Control Unit begins a FETCH cycle for interrupt operation. With the START CYCLE pulse, the MB Register is cleared and the contents of the computer's accumulator are transferred to the MB Register. Following this action, the Control Unit generates an EXT DONE. From this point on, the interrupt mode differs from the internal mode only in that PC1 is not incremented. Thus, after execution of the current instruction, the program returns to the point where it was interrupted, unless the GNI instruction was used to provide an EEM or EES instruction.

When several GNI instructions are provided by the computer in rapid succession, the PDP-14 will process at least one ROM instruction between every GNI, unless one of the GNI instructions forces the PDP-14 into the external mode.

3.4.4 FETCH Cycle for External Mode Operation

The FETCH cycle for external mode operation begins with the clearing of the MB Register. Concurrently, the Control Unit sets the EXT FLAG to signify to the computer that it is ready for another operation. When the computer senses this condition, it places an instruction in its accumulator and issues an LDE (6164_8) IOT instruction. This instruction clears the EXT FLAG and loads the accumulator word in the MB Register. From this point, an EXT DONE pulse is generated and the remaining part of the FETCH cycle is the same as for internal mode operation.

3.4.5 EXECUTE Cycle

The major events for instruction execution are also shown on D-FD-PDP-14-0-6. The events are generally self-explanatory; however, a couple of explanations are necessary. Note that 2-word instructions (JMP + JMS) require another memory access (either from ROM or external computer). Also observe that I/O instructions do not require the discrete time states (PAUSE, TS1 and TS2). Note also that controller operation is halted at the end of an EXECUTE cycle if the RUN flip-flop is reset; otherwise, a FETCH cycle is started.

3.5 LOGIC AND CIRCUIT DESCRIPTION

3.5.1 General

The major logic functions and circuits are described in subsequent paragraphs. The description, in general, references drawings in Appendix B, however, simplified diagrams are provided where necessary. For a definition of signals, refer to the signal glossary in Appendix A.

3.5.2 Initialization

The PDP-14 is initialized: 1) during a power-up sequence; 2) when the START/STOP switch is depressed to START while the RUN flip-flop is cleared; 3) when a timing error is detected for internal mode operation; and 4) when power is removed (power shutdown or power failure). In general terms, the initialize operation resets all control flip-flops and clears the MB, PC1, PC2, and the IR. In addition, an I/O CLEAR pulse generated from the INITIALIZE output, clears all output, storage, and accessory flip-flops except the retentive memories. The INITIALIZE signal sets the FETCH flip-flop and, since PC1 is cleared, the processor begins a FETCH cycle at memory location 0.

Drawing D-BS-PDP-14-0-3 shows the functional relationships of the power control logic and drawing C-CS-M742-0-1 depicts the circuits that generate the INITIALIZE outputs. Transistor Q1 and associated RC networks (drawing C-CS-M742-0-1) function as a power-up sensor and delay circuit; its output is ORed with the output of the power shutdown circuits. Transistors Q3 and Q4 form an emitter-coupled differential pair that senses a power shutdown. Transistors Q5 and Q6 function as inverter drivers for the power shutdown circuit. Transistors Q7 and Q8 form a Schmitt trigger for switch filtering with a driver stage (Q9). These stages are used for manual control functions (START and CONTINUE) and power-up functions.

During power up, the +5V potential reaches a usable value in approximately 16 milliseconds (corresponding to approximately one ac input cycle) after power is switched on. During this interval, and for approximately 50 to 90 milliseconds after, Q1 is forward-biased by the charging of C9. As a result, the SHUTDOWN L signal resets the RUN flip-flop, and causes INITIALIZE L, INITIALIZE H, CLR PC1 H, and CLR MB H outputs as shown in Figure 3-11.

During power up, C14 begins charging to +5V (Node A, Figure 3-11). Approximately 200 milliseconds later, the voltage at Node A exceeds the threshold of Schmitt trigger Q7 and Q8. With Q7 and Q8 on, Q9 switches on and triggers START EXT pulse generator E2. This stage, in turn, sets the RUN flip-flop and clears the STOP flip-flop with a 200-nanoseconds ground-asserted pulse. The START EXT L output also starts Control Unit timing by triggering a start delay stage in the M741 module. With this action, the Control Unit begins a FETCH cycle at memory location 0 (PC1 = 0000).

During power shutdown (or a power failure), the machine system is shut down in a predictable manner by returning the PDP-14 to an initialized state. For detection of power shutdown or a power drop, the base of Q3 is referenced to +2.8V while the base of Q4 is referenced to approximately +2.5V. With this arrangement, Q4 is conducting while Q3 is off during normal operation. When the +5V source drops to approximately +4.6V, however, Q3 conducts hard and Q4 is cutoff. (The bias for this action is maintained by C11 so that the process continues until the +5V drops to an unusable value, nominally in about 200 nanoseconds.) With Q4 off, Q5 switches off and Q6 switches on. With Q6 on, the system is initialized and the RUN flip-flop is reset (Figure 3-11).

The machine system is also initialized when the START/STOP switch is depressed to START (provided the RUN flip-flop is cleared). For this function, the START switch provides a ground level during switch closure. As a result of this level, diode D3 completes a discharge path for C14. With C14 discharged below the threshold of Schmitt trigger Q7 and Q8, Q9 switches off. With Q9 off, E9 generates an initialize output. (The system can be held in the initialize state by holding the START switch depressed.) When the START switch is released, the initialized output is discontinued, and C14 begins charging again. Approximately 200 milliseconds later, the threshold of Q7 and Q8 is exceeded and E2 generates a START EXT L pulse to set the RUN flip-flop and to start processor timing.

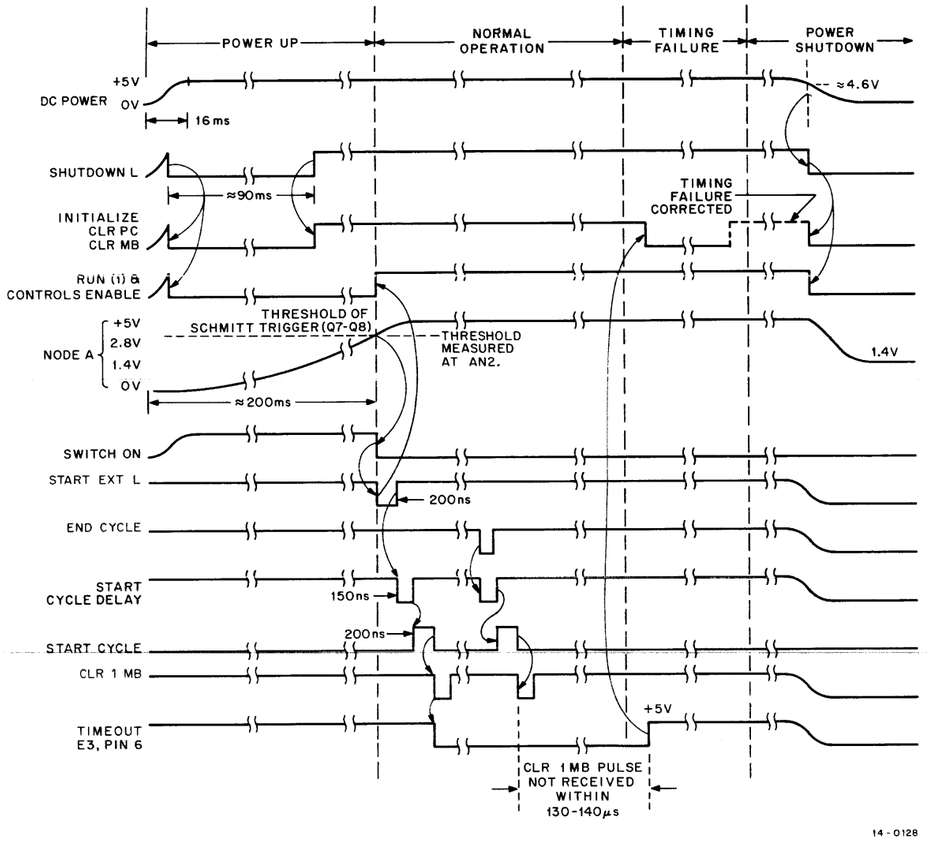


Figure 3-11 Power Control Timing

Detection of a timing malfunction for internal (ROM) mode operation also initializes the system. An integrating monostable multivibrator (designated E3 on circuit schematic) detects a timing malfunction. This stage is qualified by a RUN input denoting the RUN flip-flop is set. A CLR 1 MB L triggers stage E3 following the setting of the RUN flip-flop. As a result, E3 generates a ground-level output. If the stage does not receive another CLR 1 MB pulse within 130 to 140 microseconds, it reverts to its stable state (+5V at pin 6). As a result, the system is held in the initialized state until the timing malfunction is cleared and the system is restarted.

3.5.3 Manual Controls

The PDP-14 uses three manual controls: an ON/OFF switch; a spring-loaded, center-off START/STOP switch; and a spring-loaded CONTINUE switch. The ON/OFF switch controls primary power to the power supply as shown in drawing C-CS-7006314-0-1. When this switch is placed to the ON position, the PDP-14 automatically begins its control sequence as described in the previous paragraphs. The PDP-14 control sequence continues until a HALT instruction is executed, the START/STOP switch is depressed to STOP, a timing malfunction is detected, or power is removed.

Drawing D-BS-PDP-14-0-3 shows the functional relationships of the START/STOP and CONTINUE switches with the M742 module. The STOP position of the START/STOP switch momentarily grounds an input to the M742 module. This input directly resets the STOP flip-flop. With the STOP flip-flop reset, the RUN flip-flop is reset at the end of the current instruction cycle.

With the RUN flip-flop reset, the M742 provides a ground-asserted CONTROL ENABLE level to the START position of the START/STOP switch and to the CONTINUE switch. Thus, when either switch is closed, a ground-asserted pulse is returned to the M742 module. This input discharges C14 in the RC delay network of Schmitt trigger Q7 and Q8 (drawing C-CS-M742-0-1).

With C14 discharged below the turn off of Q7 and Q8, Q9 provides a positive-asserted output. This output is gated with START H to initialize the system during the interval the START switch is closed. As long as the START/STOP switch is held in the START position, the system is held in an initialized state.

When the START switch is released, C14 must again charge to the turn-on threshold of Q7. This action provides a 200-millisecond delay interval to eliminate switch bounce. After 200 milliseconds, Q9 provides an output transition to ground. As a result, pulse generator E2 starts the controller timing and sets the RUN flip-flop.

3.5.4 Major States and Timing

3.5.4.1 General – The logic circuits that comprise this functional area are shown in block schematic form on D-BS-PDP-14-0-3, Sheet 1. These logic circuits are contained on an M741 module and are detailed on D-CS-M741-0-1. Figure 3-12 shows the pertinent timing relationships for the logic.

3.5.4.2 FETCH Cycle – During initialization, the FETCH/EXECUTE flip-flop is set to the FETCH state. At the end of an initialize function, the power control provides a START EXT pulse. This pulse triggers a delay and pulser stage. Since these circuits are somewhat unique and are also used in other control areas, the circuit is described in detail in subsequent paragraphs before continuing with the FETCH cycle.

Figure 3-13 depicts the circuit schematic, logic equivalent, and timing relationships for a delay stage and a pulser stage. The circuit shown is used for start delay timing and START pulse generation; however, it is representative of other delay and pulser circuits in the Control Unit.

A start delay of approximately 150 nanoseconds is established by RC network C17–R31 and the turn-on threshold of E17. At end of the delay, this circuit triggers the pulser circuit to generate a 200-nanosecond START pulse (Figure 3-13).

In a quiescent state, C17 is charged to +5V, the charge across C12 is equalized at approximately +0.7V and the pulser output (Node E) is a logical 0. With the negative transition of the START EXT L pulse, transistor Q9 switches on and C17 discharges to approximately 0V. With both inputs to E17 a logical 0, E17 switches off and C12 rapidly charges to the difference between the base voltage of Q6 and +5V.

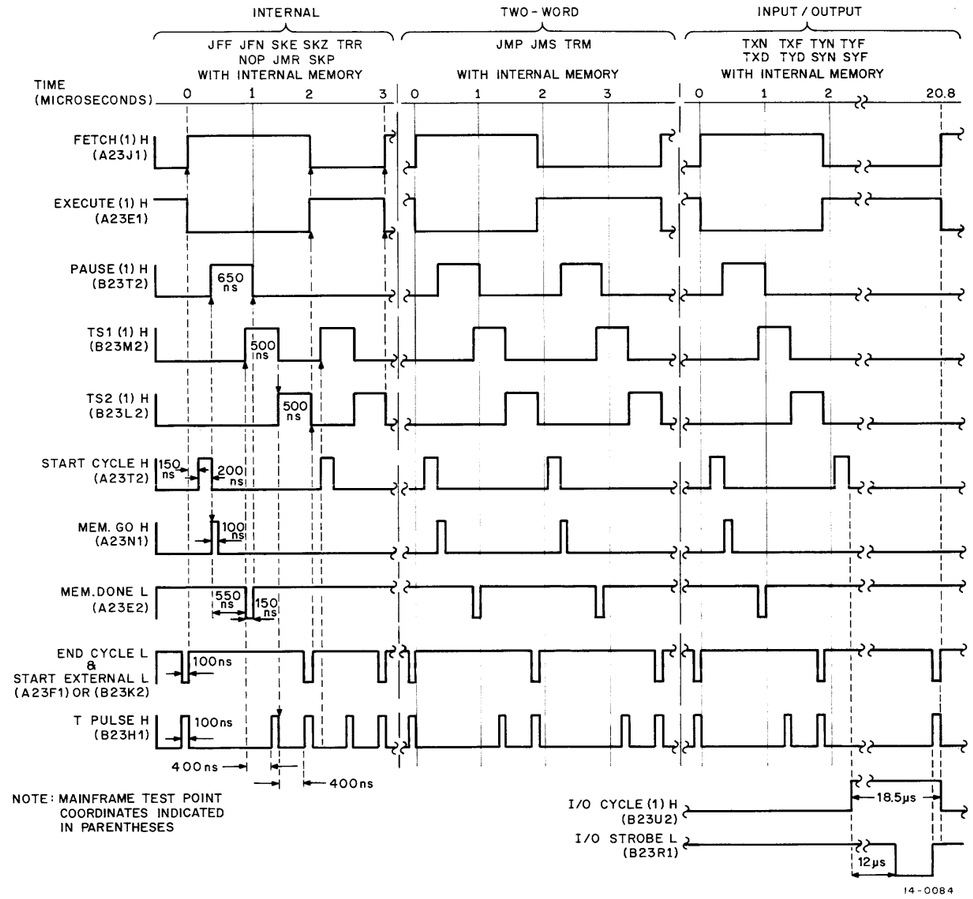


Figure 3-12 Control Logic Timing

The positive transition of the START EXT L initiates the delay action. This transition causes E16 to switch Q9 off. With Q9 off, C17 begins charging toward +5V. After an interval of 150 nanoseconds, the voltage across C17 exceeds the turn-on threshold (≈2V) of E17.

The turn-on of E17 places Node C at approximately +0.7V and C12 couples the -5V charge to the base of Q6. Since the base of Q6 is driven negative, Q6 switches off and remains off until C12 discharges through R23. The interval required for this action is approximately 200 nanoseconds; thus, Q6 generates a 200-nanoseconds positive pulse. This START CYCLE pulse begins the major state timing.

The trailing edge of the START cycle pulse sets the PAUSE flip-flop as shown in Figure 3-12. Setting the PAUSE flip-flop triggers a 100-nanoseconds pulser circuit. This circuit and associated gating generate a CLR MB L and a MEM GO H pulse.

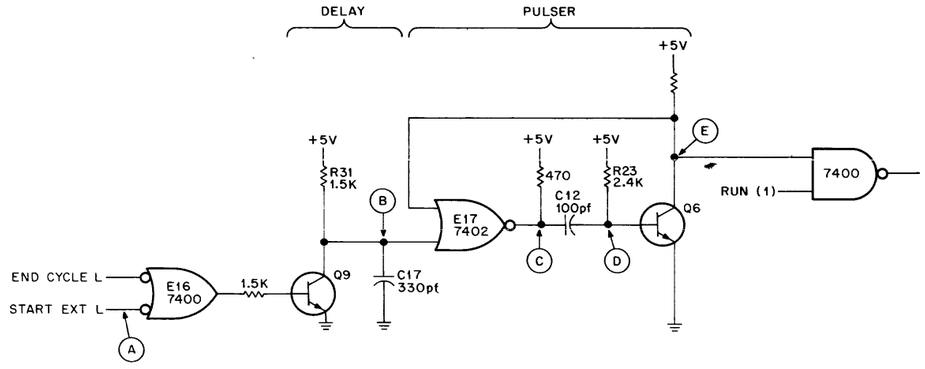


Figure 3-13 Delay and Pulser Operation

The MEM GO H pulse starts a ROM cycle (refer to Paragraph 3.5.6.3 for details of memory timing). Upon completion of this cycle (approximately 450 to 550 nanoseconds later), the ROM returns a MEM DONE L pulse (Figure 3-12). The leading edge of this pulse initiates TS1 during which the instruction is transferred to the IR. The trailing edge of MEM DONE resets the PAUSE flip-flop. Time state 1 has a duration of approximately 500 nanoseconds. Two pulser circuits determine this interval. These pulser circuits are connected in tandem with the 400-nanosecond pulser first. The trailing edge of its output pulse triggers the 100-nanosecond pulser.

The trailing edge of the resulting pulse (T PULSE) resets the TS1 flip-flop and sets the TS2 flip-flop. During TS2, PC1 is incremented. No further action occurs during TS2. The interval for TS2 is also 500 nanoseconds (this interval is established by the same pulser circuits as TS1). At the end of TS2, a T PULSE is ANDed with TS2 to generate an END CYCLE L pulse. This pulse resets the FETCH/EXECUTE flip-flop to begin an EXECUTE cycle.

3.5.4.3 EXECUTE Cycle – The END CYCLE L pulse also triggers the START CYCLE timing to begin the execution cycle. The decoding of an instruction op code begins when the instruction is transferred to the IR. This information is not acted upon, however, until at least the beginning of the EXECUTE cycle. The operations and timing for the EXECUTE cycle are instruction dependent. These relationships can perhaps best be understood using the instruction flow diagram (D-FD-PDP-14-0-6) and major state timing (Figure 3-12).

If the instruction is a NOP, JFN, JFF, SKE, SKZ, or a TRR instruction, the TS1 flip-flop is set by the START CYCLE H pulse. If the instruction is a JFN, JFF, SKE, or SKZ instruction, the related decision is executed during TS1 and the result is received either in the JF-OK flip-flop (for JFN or JFF) or the SKIP OK (for SKE or SKZ). For register-to-register transfer (TRR) instructions, the transfer is implemented during TS1. For a NOP instruction no action is performed during TS1. At the end of TS1, the timing advances to TS2. During this state, PC1 is updated for the Decision instructions (JFN, JFF, SKE, and SKZ). At the end of TS2, the END CYCLE L pulse initiates another FETCH cycle by complementing the FETCH flip-flop and initiating a start cycle delay.

If the decoded instruction is a 2-word instruction (JMP, JMS, or TRM), then the START CYCLE H pulse sets the PAUSE flip-flop. This action results in another ROM access. During TS1, the control transfers the second word of the JMP or TRM to the register designated by the JMP, JMS, or TRM instruction. Then, the control advances to TS2. During TS2, the PC1 is updated if required. For a JMS instruction, PC1 receives the contents of the MB Register. For a JMP instruction, the JMP address (entered into PC1 during TS1) is incremented. Following TS2, the control again generates an END CYCLE L pulse to begin another FETCH cycle or halt.

If the decoded instruction is an I/O instruction (TXF, TXN, TYF, TYN, SYF, SYN, TXD, or TYD), the START CYCLE H pulse sets the I/O CYCLE flip-flop at the beginning of the EXECUTE cycle. This action starts a 12-microsecond (approximate) delay to allow for selection of the input or output circuit. At the end of this delay interval, the control generates a 6.5-microsecond (approximate) strobe. This strobe clocks the SET and RESET functions for SYN and SYF instructions. At the end of this pulse, the T PULSE circuit is triggered to produce another END PULSE. This pulse strobes the sample return line for Test instructions and also loads the Output Register for Test and Display instructions.

3.5.5 Major Registers

3.5.5.1 General – Drawing D-BS-PDP-14-0-4 shows the major registers comprising the basic Control Unit. Drawing D-BS-DA14-L-3 shows the major registers added for a computer interface. Each register is updated by a jam-transfer that occurs on the trailing edge of the load pulse.

3.5.5.2 Program Counter 1 (PC1) – This 12-bit register stores the address of the next ROM instruction. This register can be cleared. It can also be loaded from a BUS 00–11 source register or a direct input. This register contains a summation and carry structure at its input that enables it to be incremented (or decremented) by 1. (At present, the decrementing capability is not used.) To increment a count, the contents of PC1 are gated to BUS 00–11 by SOR–PC1 0–3 and SOR–PC1 4–11 gating levels from the instruction decoder. The instruction decoder also provides an INCREMENT input which enables the summation structure. The decoder also provides an LD PC1 strobe. This strobe, derived from a 100-nanosecond T PULSE, loads and increments PC1. The content of PC1 directly drives the ROM selection circuits and can be gated to BUS 00–11 for transfer to another register.

3.5.5.3 Program Counter 2 (PC2) – This 12-bit register stores the program return address from subroutines. Program Counter 2 receives this address from PC1 when a jump-to-subroutine instruction is executed. This transfer is implemented via BUS 00–11. When the subroutine is completed, PC2 provides this address to PC1 so that the program can resume at the correct address. Again the transfer is implemented via BUS 00–11. Unlike PC1, this program counter cannot be incremented (or decremented).

3.5.5.4 Memory Buffer – This 12-bit register accepts instructions from the ROM, the computer Memory Port, or from the PDP-14 transfer bus (BUS 00–11). Instructions from the ROM or the computer Memory Port are provided to the direct-set inputs (MBS 00–11) of the MB Register and therefore require no load strobe. However, the register must be cleared before loading it via the direct-set inputs. Data can also be loaded from a BUS 00–11 source register. For this jam-transfer, the control provides a 100-nanosecond LD MB pulse. The contents of the MB Register can also be transferred to BUS 00–11 by SOR–MB (0–3) and SOR–MB (4–11) pulses.

3.5.5.5 Instruction Register (IR) – This 12-bit register stores the instructions for decoding and execution. Instructions from the ROM (or a computer) are transferred to the IR from the MB Register via BUS 00–11. A LOAD IR strobe (in conjunction with an SOR–MB gating pulse) performs this transfer. The IR content is made directly available to the instruction decoder until updated by the next jam-transfer. The content of IR can be gated to BUS 00–11 by a SOR–IR gating pulse from the source register decoder in the M740 module.

3.5.5.6 Input Register – This 12-bit register is only used for computer interface functions. Its principal use is to load PC1 or PC2 from BUS 00–11. For this input transfer, the computer interface provides an LD INPUT pulse. This pulse is derived from BIOP timing as a result of an IOT instruction. For an output transfer, the instruction decoder provides a SOR–INPUT gating pulse that places the contents of the Input Register on BUS 00–11.

3.5.5.7 Output Register – This 12-bit register is used only for computer interface functions. It is loaded from a BUS 00–11 source register (principally the IR or MB Register) by an LD OUTPUT strobe. The Output Register does not utilize its integral output gating structure. Instead, a gating structure on the computer interface module (M745) transfers the Output Register contents to the computer's bus. The computer interface module also provides the transfer strobe for this function.

3.5.5.8 Memory Port Buffer – The Memory Port contains a 12-bit register that buffers inputs from the BAC 00–11 lines and provides outputs that direct-set the MB Register. The principal use of this register is to supply computer instructions via the MB Register path. The computer interface module (M745) generates the strobe for loading this register. This strobe is derived from the computer bus timing. The computer interface also generates the output gating strobe for this register.

3.5.6 ROM Circuits

3.5.6.1 General – A ROM bank consists of three primary divisions: 1) a G924 ROM Selection and Timing module; 2) a G922 ROM Braid module; and 3) a G923 Sense Amplifier module. The general relationships of these divisions are described in Paragraph 2.2.2.1; D-BS-MR-14-0-2 shows the module interconnections. Module circuit details are shown in D-CS-G924-0-1, C-CS-G922-0-1, and D-CS-G923-0-1, respectively.

As mentioned previously, the ROM consists of up to four 1024-word banks for a total storage capacity of 4096 12-bit instructions. Also, each bank is an operating entity. For a 1K ROM, this bank must be installed in the module slots for bank 1 (Figure 2-1). If other banks are used, they must be inserted in consecutive bank slots or the ROM will not respond correctly and the PDP-14 timing will stop.

If all banks are removed, a timing loop in the major states and timing module is completed to effectively bypass ROM timing. With this arrangement, the Control Unit continuously executes NOP instructions.

Figure 3-14 depicts the functional circuits for a ROM bank and is used for the ensuing discussion.

3.5.6.2 Address Selection – A ROM address is specified by PC1. The two MSBs (PC1 00 and PC1 01) select the ROM bank. These bits are decoded by a structure in the M742 power control module as shown in Figure 3-14. This decoder then selects the applicable bank with one of four discrete ENABLE MEM signals. An ENABLE MEM signal, when asserted, gates MEM GO to the respective bank timing chain.

The next seven MSBs of PC1 (PC1 02 through PC1 08) select one of 128 braid wires. For this function, a 4-bit decoder structure decodes PC1 02 through 05 to select one of sixteen matrix transistor rows. A second decoder circuit decodes PC1 06 through 08 to select one of eight current switch columns. This latter action is not performed, however, until the respective decoder is pulsed.

Each of the 128 braid wires is routed through or around 96 Ferrite-core transformers to form eight binary instructions. If the wire passes through a transformer, a logical 1 is generated for the corresponding bit when the braid wire is pulsed by the address selection circuits. If the wire passes around the transformer, a logical 0 is generated for the bit. Only one of the eight binary instructions formed by the braid routing is selected at a time. For this selection, PC1 09 through 11 select one of eight groups of 12 sense amplifiers (Figure 3-14).

3.5.6.3 Timing Circuits – For selection and pulsing of a braid wire, the gated MEM GO pulse triggers the read pulse generator (Figure 3-15). This stage, in turn, produces a 350-nanosecond pulse that enables the current switch decoder to complete the selection matrix by selecting one of eight lines. As an end result, one of 128 braid wires is pulsed. The gated MEM GO also triggers a 150-nanosecond strobe delay pulser in the timing chain. The delay interval provided by this stage permits switching transients to settle before strobing the output. The trailing edge of the delay pulse triggers a strobe pulse generator. The 150-nanosecond pulse generated by the stage pulses the outputs of a word decoder to select 12 of 96 sense amplifiers. (This action is described in detail in Paragraph 3.5.6.4.)

The trailing edge of the 150-nanosecond strobe pulse also triggers a MEM DONE pulser. This stage, in turn, produces a 150-nanosecond pulse which informs the Control Unit that the memory cycle is complete and an instruction is available.

3.5.6.4 Data Sense Circuits – Figure 3-14 illustrates the general arrangement of the sense circuits. As indicated, there are 96 Ferrite-core transformers associated with the braid. These transformers (and their related sense amplifiers) are arranged to provide eight 12-bit instructions for each braid wire pulsed. However, only one instruction is selected at a time. PC1 09 through 11 select the instruction by strobing only one of the eight groups of sense amplifiers.

Figure 3-16 illustrates the method used to obtain one bit of an instruction and provide it to the MB Register. To reiterate, if a braid wire passes through the transformer, a pulse is induced in the sense winding when the braid wire is pulsed. If the braid wire is routed around the transformer, no pulse is generated when the braid is pulsed. The sense amplifier for the stage is strobed after switching transients have settled. If the drive wire for the bit passes through the transformer, the sense amplifier output is ground-asserted. As a result, the latch circuit for the bit is set and, in turn, direct-sets a corresponding stage of the MB Register. The latch is cleared when the PAUSE input returns to ground. This action readies it for another cycle.

NOTES:
(1) ROM TRANSFORMER SENSE WINDINGS ON G923 BOARD.
DRIVE WIRES (PROGRAM) ON G922 BOARD.
(2) SAME AS READ PULSE GENERATOR ONESHOT.

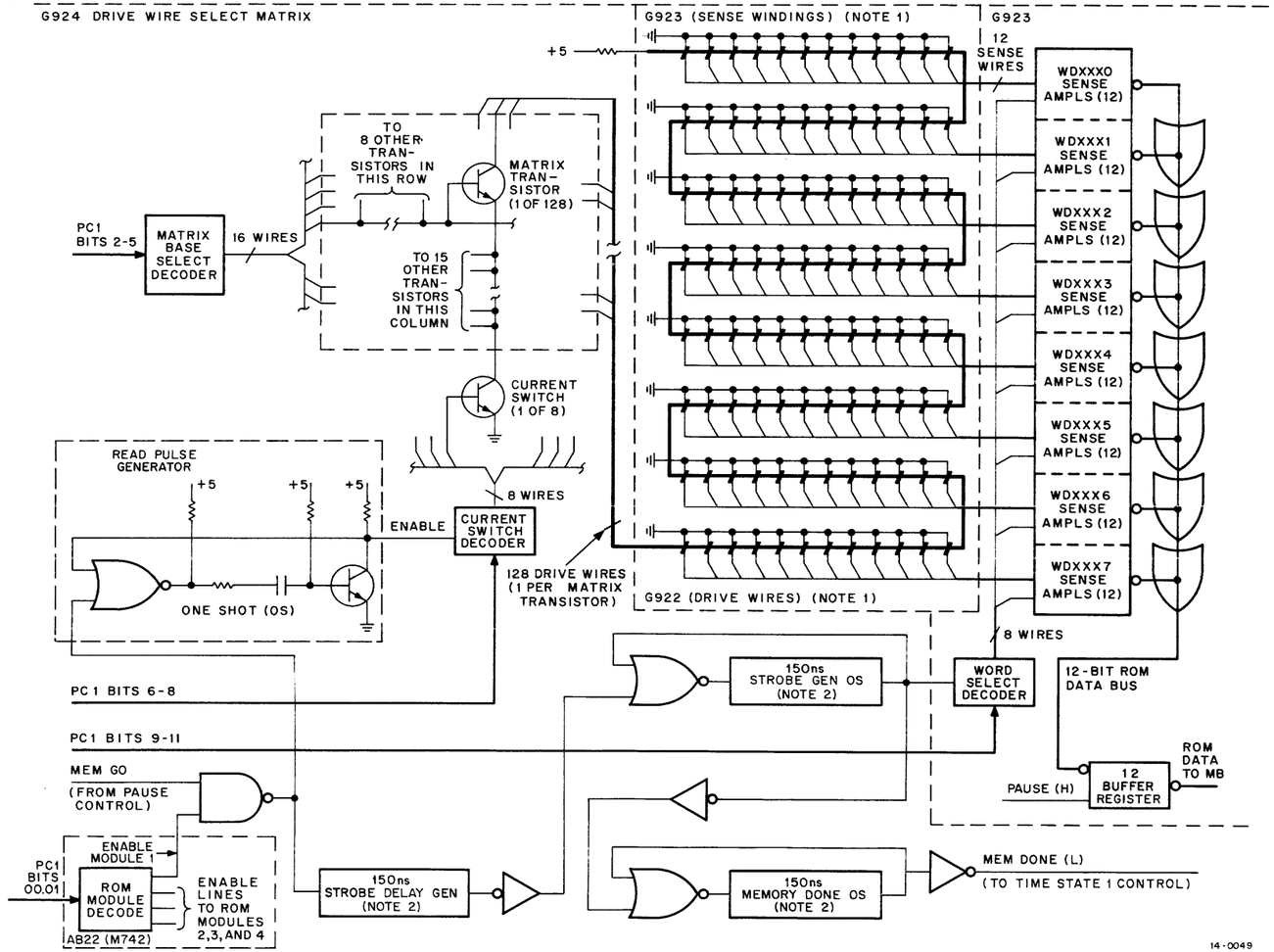
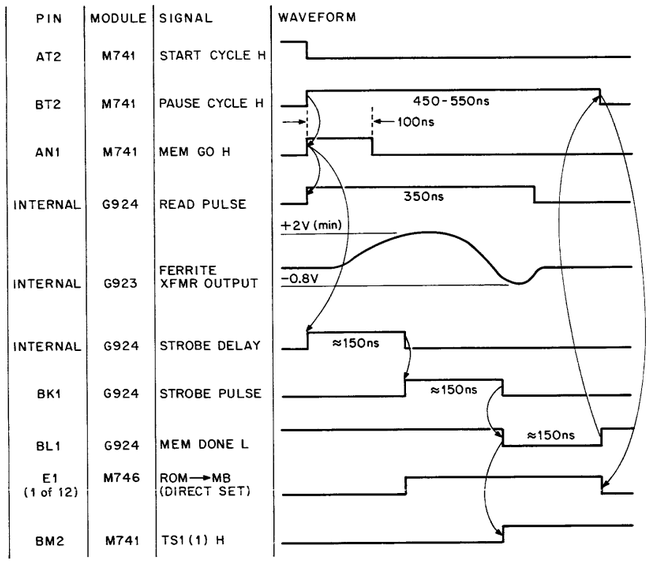


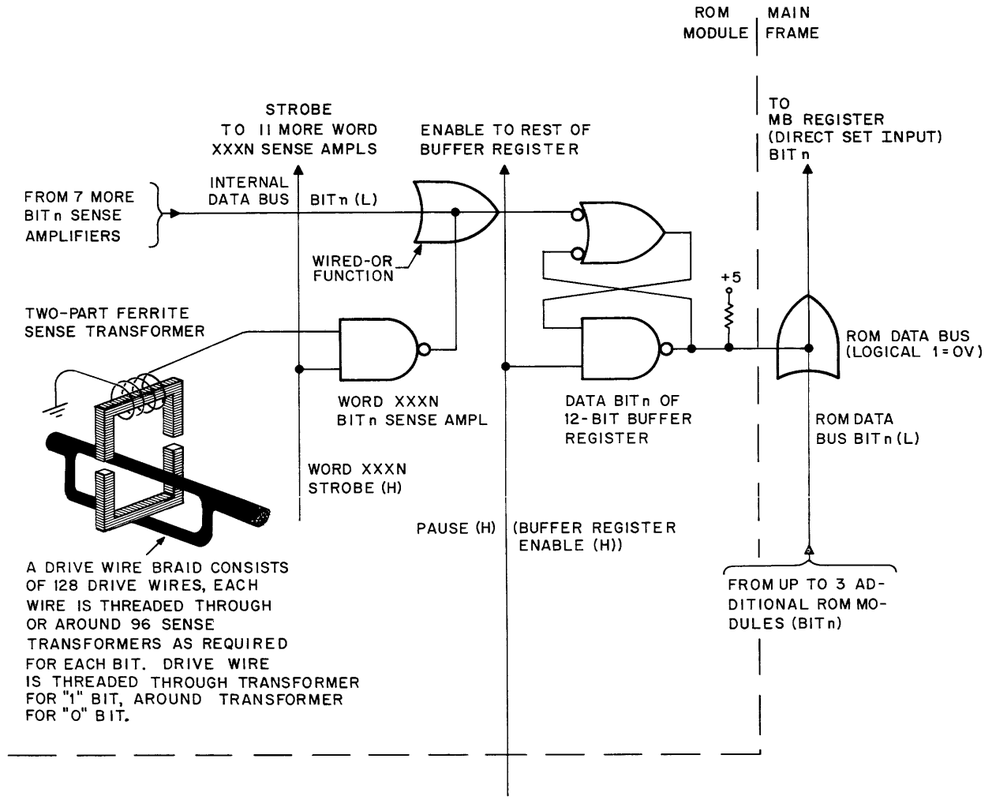
Figure 3-14 ROM Functional Diagram



NOTE:
Test points accessible from wiring side of mainframe are shown for ROM no. 1, other waveforms must be observed on G923 module of ROM assembly.

14-0052

Figure 3-15 ROM Timing Relationships



14-0053

Figure 3-16 ROM Data Sense Circuits, Simplified Logic Diagram

3.5.7 Instruction Decoding and Register Control

The M740 module decodes the instructions and generates the discrete control signals for executing the instructions. The decoding operation is performed in four basic parts and involves four decoder circuits as shown in D-BS-PDP-14-0-3 (Sheet 1). Drawing D-CS-M740-0-1 shows the logic circuits for the functional areas.

The op code (IR 00–03) is decoded by a block labeled INSTRUCTION DECODER. This operation begins when the instruction is transferred to the IR (at TS1 of the FETCH cycle). Thus, discrete control signals defining the instruction overlap the FETCH and EXECUTE cycles.

An operate decoder deciphers IR 04 and 05 to define minor arithmetic operations associated with transfers (increment or decrement). Figure 3-9 lists the codes and functions associated with these bits. A 500-nanosecond pulse, occurring at TS1 of the EXECUTE cycle, strobes this decoder to synchronize the applicable operation with the transfer.

The source register decoder decodes IR 06 through IR 08 of instructions involving transfers (TRR, EEM, LEM, JMP, JMS, SKE, and SKZ instructions) to generate source gating strobes. A 500-nanosecond pulse, derived from TS1 and EXECUTE conditions, clocks this operation. Figure 3-9 defines the source codes for the registers.

The destination register decoder, as the name implies, decodes IR 09 through IR 11 to generate pertinent load pulses for the registers. Timing for this decoder is provided by TS1 and EXECUTE conditions; thus, the decoder output is active for only 500 nanoseconds.

A 100-nanosecond T PULSE input clocks the load pulse operation. Since the decoder output is only active during TS1 of an EXECUTE cycle, a single load pulse is generated at the end of TS1 (corresponding to the end of the source gating strobe).

Source and destination strobes are also generated for conditions within the Control Unit. For example, SOR–MB (0–3) and SOR–MB (4–11) output gating strobes and an LD–IR must be provided during TS1 of a FETCH cycle to update the IR. Similarly, to increment PC1 at TS1 of a FETCH cycle, SOR–PC1 0–3 and LD–PC1 load strobe must be generated. To prevent the incrementing of PC1 during an interrupt operation, INT SYNC 0 qualifies the generation of the LD–PC1 strobe.

3.5.8 I/O Interface Circuits

3.5.8.1 General – As mentioned previously, the I/O interface circuits select the I/O package and address the circuits within the package. For a Test instruction, these circuits also compare the state of the input or output with the state specified by the Test instruction and provide the comparison result to the TEST flip-flop. For

Operate instructions, these interface circuits select the output circuit and define the function to be performed (SET, RESET, or CLEAR).

The general relationships of the I/O interface circuits are shown in D-BS-PDP-14-0-5. This drawing also defines the input and output addresses associated with a PACKAGE SELECT (PS) line and the output function lines. Drawing D-CS-M743-0-1 shows the logic and circuit details for the I/O interface.

3.5.8.2 Input Tests – Figure 3-17 illustrates the circuits used for testing inputs. For discussion purposes, a specific input address is used. However, circuit operation is the same for all other input addresses.

For an example of circuit operation, assume the IR contains a TXN instruction for input address 7 (octal 2407). With this instruction in the IR, the instruction decoder asserts the I/O instruction line (TXF, TXN, TYF, TYN, SYF, SYN, TXD, or TYD). As a result, the I/O package decoder circuit decodes IR 04 through 06 and asserts PACKAGE SELECT 1. Concurrently, the I/O interface address gating asserts ADDR 1, 2, and 4, and negates ADDR 8.

The PACKAGE SELECT 1 output is ANDed with the MSB (and its complement) of the address bits to enable one of two circuit decoders within the I Box. For the example, the K161 decoder for addresses $0_8 - 7_8$ and $20_8 - 27_8$ is selected since ADDR 8 is a logical 0. This octal decoder, in turn, decodes the ADDR 1, 2, and 4 lines and positive-asserts output line 7. As shown in Figure 3-17, output line 7 selects the gating circuits for two input converters, one for address 7_8 and one for address 27_8. Assume at this point that the inputs for addresses 7 and 27 are on. With this condition, the converters for these addresses provide +5V (logical 1) outputs. Since the decoder gating strobe is also positive, the output diodes are forward-biased and both sample return lines are asserted.

The sample return lines are gated with IR 07 (and its complement) to select the pertinent line. This method has the same net effect as choosing one input out of 32 and using one sample return line. For the example, IR 07 is a logical 0 so the state of X RET 0 is selected. This result is then qualified by control signals denoting that a test input instruction is active (TXN, TXY, or TXD). Immediately following this gating, the state of the input is compared with IR 03. This bit defines whether the input is to be tested for an on or off state. For the example, IR 03 is a logical 1 (denoting an on test) and, since the input is on, results in TEST TRUE H being positive-asserted. This output sets the TEST flip-flop. This action occurs at the end of the EXECUTE cycle. The TEST flip-flop provides one input to the jump comparator where it is used in a Decision (JFF or JFN) instruction. This function is described in Paragraph 3.5.9. The TEST flip-flop remains set until reset by a JFF or JFN instruction. This action occurs at the end of the EXECUTE cycle for these instructions.

If the input for address 7 was off, however, and was tested for on, the TEST TRUE signal is not asserted and the TEST flip-flop is not set. Similarly, if the input for address 7 was on and was tested for off, the TEST TRUE signal is not asserted and the TEST flip-flop is not set. If, however, the address 7 input is off and is tested for off, TEST TRUE is asserted and the TEST flip-flop is set.

3.5.8.3 Output Tests – Output testing is identical to that for inputs except for the arrangement of the addressing circuits. The same number of addressing combinations are required. However, each I/O PACKAGE SELECT line selects two O Boxes instead of one. With this arrangement, two circuits are selected for each basic address. These circuits, however, are in different O Boxes. Again, two sample return lines are used and IR 07 selects the correct line.

3.5.8.4 Output Functions – The same addressing scheme is used for output functions. The I/O interface, however, must also assert a function line. Drawing D-BS-PDP-14-0-5 shows, in block form, the circuits that control the function lines. There are two lines (E SET 0 and 1) for a SET function, two for RESET (E RSET 0 and 1), and one for a CLEAR. This arrangement is required because the addressing scheme addresses two circuits concurrently. Bit 03 of the IR determines whether a set or reset function is implemented. (If IR 03 is a logical 1, a SET function is performed; if not, a RESET function is performed.) Similarly, IR 07 selects the group line. If IR 07 is a logical 1, the upper group is selected (either E SET 1 or E RSET 1). If not, E SET 0 or E RSET 0 is selected.

3.5.9 Conditional Jump Circuits

Figure 3-17 also shows the jump comparator and JF-OK flip-flop. These circuits are used with Decision (conditional jump) instructions.

The jump comparator logic is enabled during TS1 of the EXECUTE cycle for a JFN or JFF instruction. It compares the state of the TEST flip-flop with a bit (IR 03) defining the jump conditions and sets the JF-OK flip-flop if a favorable comparison results. Note that after the TEST flip-flop is tested, it is reset (if set) regardless of the test result.

There are two comparison conditions which set the JF-OK flip-flop. First, if the TEST flip-flop is set and IR 03 is a logical 1 (denoting a JFN instruction), the JF-OK flip-flop is set. Second, if the TEST flip-flop is reset and IR 03 is a logical 0 (as for a JFF instruction), then the JF-OK flip-flop is set. All other comparison conditions have no effect on the JF-OK flip-flop.

The JF-OK flip-flop is clocked by a 100-nanosecond T pulse occurring at the end of TS1 in the EXECUTE cycle. The state of this flip-flop is then used to initiate a transfer during TS2. This transfer establishes the jump address.

A conditional jump can be implemented only on the same ROM page (256 locations) because bits 0 through 3 of a JFF or a JFN must be used to define the instruction, thus leaving only bits 4–11 to define the jump address. In addition, there are no facilities for updating PC1 0–3 concurrently. Thus, the bank bits (defined by PC 00 and 01) and page bits (defined by PC1 02 and 03) can only specify the same ROM bank and page.

The jump address is established by loading MB 04–11 and PC1 00–03 into PC1. This action is performed during TS2 of the EXECUTE cycle as illustrated in D-FD-PDP-14-0-6. For this transfer, the instruction decoder generates concurrent SOR–PC1 0–3 and SOR–MB (4–11) gating strobes. This action places the address on BUS 00–11. The address is loaded into PC1 by a 100-nanosecond LD–PC1 pulse occurring at the end of TS2. As a net result, the next instruction is accessed at the jump address.

The JF-OK flip-flop is also cleared concurrently with the address transfer. The qualifying signal for this action is TS1 returning to a logical 0 state.

3.5.10 Computer Interface

3.5.10.1 General – The computer interface contains the circuits for operating the PDP-14 with a computer's I/O bus for programmed data transfers. The circuits involved in this function are housed on an M745 Interface Control module and an M249 Memory Port Register module for the PDP-8/E. (An M106 Memory Port Register is used with the PDP-8/I and PDP-8/L, but will not operate with the PDP-8/E. The M249 will work with the PDP-8/L, PDP-8/I, or PDP-8/E with the appropriate ECO, 14-0039, installed in the PDP-14.)

Drawing D-BS-DA14-I-2 shows, in block diagram form, the major functional areas for a negative I/O bus interface such as for a PDP-8/I computer. Drawing D-BS-DA14-L-2 shows the equivalent for a positive I/O bus such as for a PDP-8/L computer.

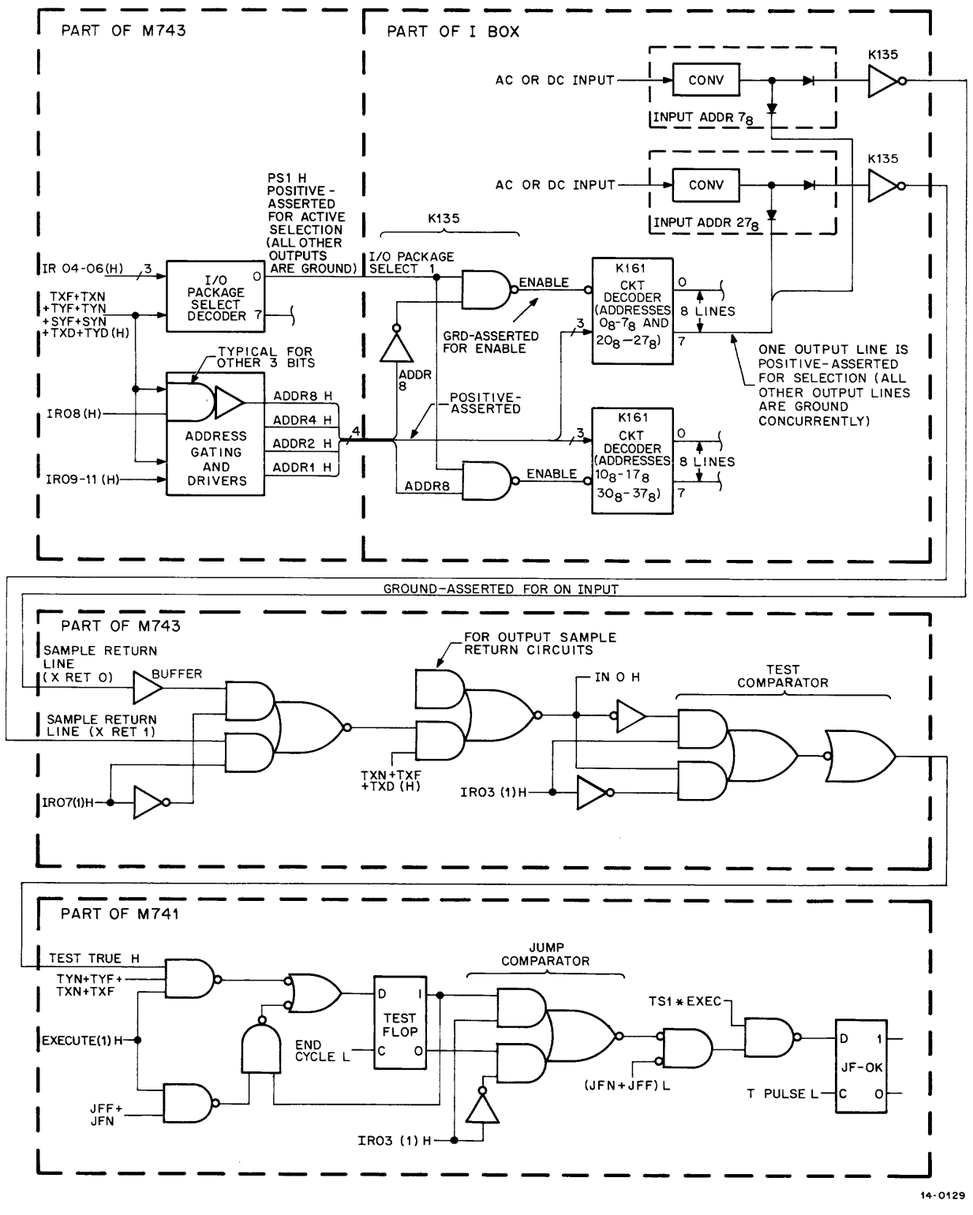


Figure 3-17 Input Test Functional Diagram

The interface control module decodes the device code provided by the computer and executes the transfer instructions. As part of this overall function it: 1) selects the operating mode; 2) selects and synchronizes an interrupt operation; 3) generates input load strobes for accepting BAC inputs; 4) interfaces PDP-14 flags with the computer's skip chain and program interrupt request bus; and 5) performs output gating for transfers to the computer.

The Memory Port Register, in contrast, simply buffers instructions transferred from the computer. It gates the instructions to the PDP-14 internal bus under control of the interface control logic.

3.5.10.2 Device Selector Logic – The IOT device selector (and subdevice) circuits are similar to those used by other I/O bus peripherals. The controller, however, recognizes two device codes (namely 16_8 and 17_8) on BMB 03 through 08. It also decodes BMB 09 through 11 (subdevice code) to perform the IOT operations. With this arrangement, up to 14 IOT instructions could be recognized; however, only 10 IOT instructions are implemented (Figure 3-10).

The BMB 03 through 07 inputs are provided in complement pairs. An M921 connects the pertinent lines to a device selector gate in the M745 module. This selector gate recognizes the basic device code of 16_8 or 17_8. Its output is then ANDed with BMB 08 to determine whether the code is 16_8 or 17_8.

Timing for the IOT operation is provided by the BIOP1, 2, and 4 pulses. Like other peripherals, the controller uses these pulses to establish transfer relationships. And like that for other peripherals, BIOP1 timing is used for the sampling of flags for the skip bus; BIOP2 timing is used for the clearing of flags and for the generation of an AC clear; and BIOP4 performs input loading, output gating, and clearing of specific flags.

3.5.10.3 Skip Bus – There are four controller status conditions that can be interrogated by computer IOT instructions. These IOT instructions and conditions are:

Instruction	Condition
SCR(6175_8)	RUN (1) – This condition denotes the controller is operating; i.e., it is not in a power-off or stop state (SCR = SKIP ON INITIALIZE).
SEF(6161_8)	EXT FLAG (1) – This condition denotes an interrupt transfer operation has been completed.
STF(6173_8)	TEST FLOP (1) – This condition denotes the I/O condition checked for was true.
SOF(6171_8)	OUTPUT FLAG (1) – This condition signifies the controller has information in the Output Register for transfer to the computer.

If the condition interrogated is true, the interface control returns a skip pulse to the computer. A BIOP1 pulse establishes the timing for the skip pulse. The skip pulse causes the computer to skip the next sequential memory location.

3.5.10.4 Interrupt Operation – A GNI (6165_8) instruction initiates an interrupt operation. During this operation, the controller interrupts ROM access and accepts an instruction from the computer. The controller subsequently executes the computer-supplied instruction, then resumes operation with the ROM at the next sequential address.

Since a GNI instruction can be issued any time during a FETCH or EXECUTE cycle, the interrupt operation must be synchronized with controller operation. Thus, there are two flip-flops associated with an interrupt. The first, designated INTERRUPT, stores a bit denoting that a GNI instruction has been issued while the controller is operating in the internal mode (EXT MODE 0). The second flip-flop, designated INTERRUPT (INT) SYNC, signifies a point in the Control Unit cycle has been reached where the interrupt can be implemented. This flip-flop establishes interrupt timing paths and also prevents PC1 from being incremented during the interrupt operation. Thus, the ROM program resumes at the next sequential address.

An interrupt operation starts when the computer issues a GNI instruction. As a result of this IOT instruction, the interface control generates an IOT 165 (LD INTER) pulse. The leading edge of this pulse loads the content of the computer's accumulator into the Memory Port Buffer Register. The leading edge also sets the EXT FLAG to denote the interface is busy (Figure 3-18). The trailing edge of the IOT 165 pulse clocks the INTERRUPT flip-flop. If the controller is operating in the internal mode, the INTERRUPT flip-flop is set to permit the controller to acquire synchronization. (If the controller is already in the external mode, the synchronization function is not required.)

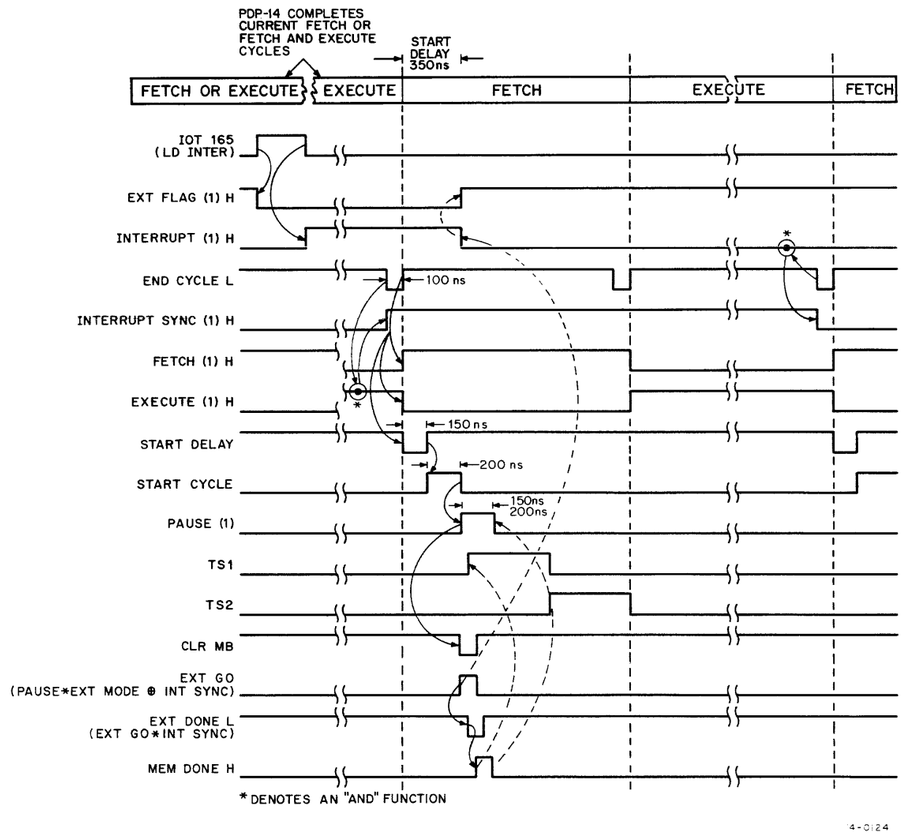


Figure 3-18 PDP-14 Interrupt Mode Timing

The controller then awaits the completion of an EXECUTE cycle. Thus, if the GNI instruction is issued during a controller FETCH cycle, the controller completes the current FETCH cycle and an EXECUTE cycle. If, however, the GNI is received during an EXECUTE cycle, the interface control waits for the completion of the current EXECUTE cycle. Timing for this aspect is provided by the END CYCLE pulse. The leading edge of this pulse sets the INT SYNC flip-flop. The trailing edge initiates START DELAY timing and sets the FETCH/EXECUTE flip-flop to the FETCH state as illustrated in Figure 3-18.

After the normal 350-nanosecond start delay, the PAUSE flip-flop is set. With the setting of the PAUSE flip-flop, the control clears the MB Register to ready it for receiving information from the Memory Port Buffer. Next, the instruction decoder logic generates an SOR–MEMPORT gating pulse. This pulse transfers the content of the Memory Port Buffer to the MB Register. Concurrently, the controller generates an EXT GO pulse which clears the EXT FLAG and INTERRUPT flip-flops to prepare the control for ending the interrupt. This event does not occur, however, until the end of the EXECUTE cycle. The EXT GO pulse, after a small propagation delay, generates an EXT DONE pulse. This pulse, in turn, produces a MEM DONE pulse. The leading edge of the MEM DONE pulse initiates TS1. The trailing edge loads the contents of the MB Register into the IR. The trailing edge also resets the PAUSE flip-flop so that the timing can advance. The remaining portion of the FETCH cycle is the same as for normal operation except that the INST SYNC flip-flop prevents the incrementing of PC1 during this FETCH cycle. As an end result, the next instruction is accessed from the next sequential memory location.

During the EXECUTE cycle, the controller executes the instruction in the IR. At the end of the EXECUTE cycle, the controller clears the INT SYNC flip-flop to allow the next access from the ROM. The GNI can be used to enter or leave the external mode as described below. The GNI instruction can also be used in the external mode to provide computer-supplied instructions without incrementing PC1.

3.5.10.5 External Mode Operation – The external mode enables the PDP-14 to stop the execution of its ROM program and accept and execute instructions supplied via the Memory Port. For selection of the external mode, the computer places an EEM (0600_8) instruction in its accumulator, then issues a GNI instruction. During the FETCH cycle for the GNI, the applicable instruction is transferred to the IR. During the EXECUTE cycle for the GNI, the controller decodes the IR content and sets the EXT MODE flip-flop. It also implements the register transfer for the EES instruction. To leave the external mode, the computer supplies an LEM (0400_8) instruction. These instructions can be provided by a GNI or LDE instruction; the LDE instruction increments PC1 while a GNI does not.

Drawing D-FD-PDP-14-0-6 shows the overall functions performed for EEM and LEM instructions. For an EEM instruction, the EXT MODE flip-flop is set during TS1 of the EXECUTE cycle. For an EES instruction, the EXT MODE flip-flop is set and a register transfer is implemented during TS1. That is, the contents of PC1 are transferred to PC2 to ready the controller for a subroutine jump.

At the beginning of the next fetch, the external mode control clears the MB Register and asserts the EXT FLAG. It then waits for the computer to provide its next instruction. The computer, upon sensing the EXT FLAG condition, can supply another instruction using a GNI (if PC1 is not to be incremented) or an LDE (if PC1 is to be incremented). Upon receipt of one of these IOTs, the controller clears the EXT FLAG (to denote the interface is busy), then transfers the content of BAC 0–11 to the MB Register via the Memory Port Buffer. After this function is complete, the controller generates an EXT DONE pulse. This pulse advances the timing from PAUSE to TS1. During TS1, the MB Register content is transferred to the IR. During TS2 of an LDE, PC1 is incremented.

To leave the external mode and return to ROM operation, the computer provides an LEM or LER instruction. A GNI or an LDE IOT instruction can be used to transfer the mode control instructions. During the FETCH cycle, the LEM or LER is placed in the IR. During the EXECUTE cycle, the EXT MODE flip-flop is reset and

for LER instructions a register transfer is implemented. This transfer returns the content of PC2 (the subroutine return address) to PC1 so that ROM operation can resume at the correct memory location.

3.6 I, O, AND A BOX CIRCUIT DESCRIPTION

3.6.1 Input Circuits

3.6.1.1 AC Input Converter – Each K578 module contains eight identical converter circuits. Each circuit (Figure 3-19) consists of a full-wave rectifier (and filter) that converts a 115-Vac input to +5 Vdc. A neon indicator is included at the input to denote the presence of an ac input. A diode output gate connects the logic signal to a signal return line. The operation of the K579 module is essentially the same as the K578. The K579 contains light-emitting diodes (LEDs) instead of neon lights and a Schmitt trigger for contact-bounce filtering. The K579 is used only in the BX14-SA input box.

3.6.1.2 DC Input Converter – Each K564 module contains eight identical dc converter circuits. Figure 3-19 also shows the circuit elements for a dc converter.

The dc converter consists of a transistor input switch, an RC filter, a Schmitt trigger, and an output gate. A light-emitting diode (LED), in series with the dc input line, denotes the presence of an input.

The converter can accept inputs having a range from 10 to 55 Vdc (or with an external resistor, inputs from 55 to 130 Vdc). For input voltages greater than 24 Vdc, a jumper clamps the base of the input switch to ground. This jumper collectively controls all input switches in the module. With this jumper connected, the input switch remains off, and inserts a 1.5K resistor in the input voltage divider. For input voltages from 10 to 24 Vdc, the jumper is disconnected and the input switch shunts the 1.5K resistor.

The input filter removes input transients (such as may be caused by switch bounce) to prevent erroneous triggering of the Schmitt trigger. The circuit has a response time of 2 milliseconds.

An overvoltage clamp protects the filter and the Schmitt trigger from excessive input voltages.

The Schmitt trigger has an upper (or turn-on threshold) of +2.7 to 3 Vdc and a lower (or turn-off threshold) of 1.5 Vdc or less. Thus, with a dc voltage of +10 Vdc or greater at the input terminal, the Schmitt trigger latches in the on state and provides a positive asserted output. This output remains positive until the input drops below the lower threshold of the circuit.

3.6.2 Output Circuits

3.6.2.1 Isolated AC Switch – Each K614 or K616 module contains four identical ac output circuits and one common master oscillator. Each output circuit consists of a diode AND gate (for positive inputs), a 2-MHz gated (or slave) oscillator, and a Triac output switching circuit as shown in Figure 3-20.

The active switching device for an output is the Triac. In an off state, this device provides a high impedance (essentially an open circuit) to the load. For turn on, this device requires a negative dc gate voltage. Two oscillators are used to develop this gate voltage as described below.

The master oscillator operates at a natural frequency of approximately 5 kHz. Its output is a non-symmetrical waveform with a positive pulse equal to approximately 10 percent of the duty cycle. The master oscillator output is gated to the slave oscillator by setting the K207 flip-flop. With this action, the master oscillator's positive pulses gate "on" the slave oscillator. The slave oscillator operates at a natural frequency of approximately 2 MHz. Thus, its output is a burst of 2-MHz pulses occurring at a 5-kHz rate.

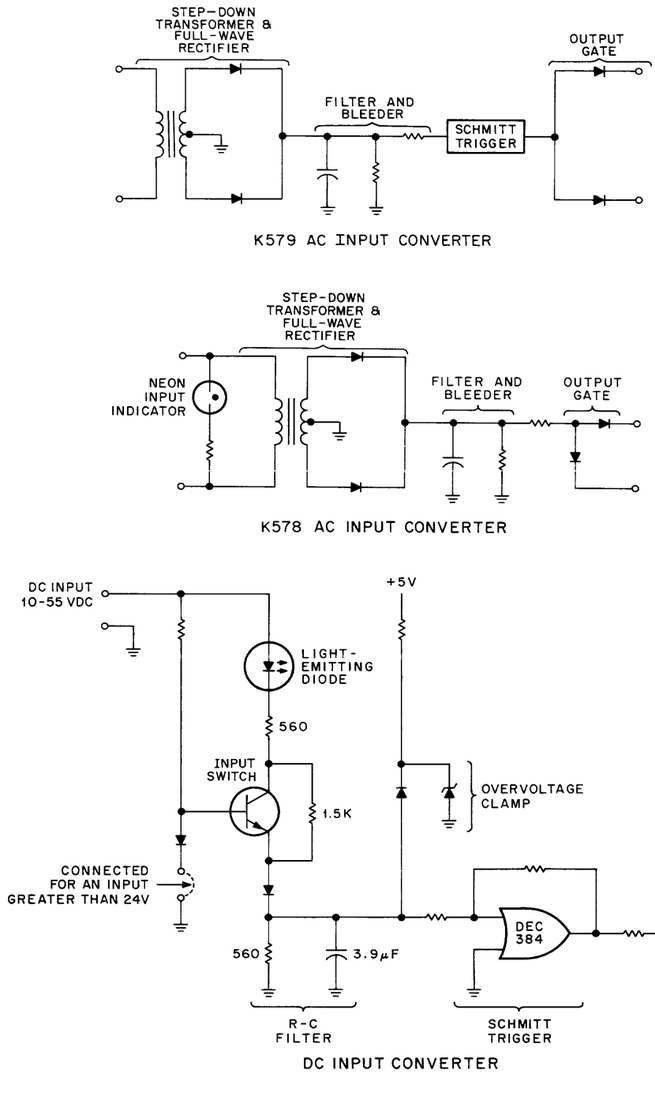


Figure 3-19 Input Converter Circuits

The slave oscillator drives a Ferrite-core isolation transformer. The high-energy pulses coupled to the secondary of this transformer are rectified and filtered. The resulting negative dc level (a nominal 2 to 4 dc) is used to switch on the Triac. When on, the Triac provides a low-impedance path between the ac input and the load terminal. A neon indicator denotes the output is present.

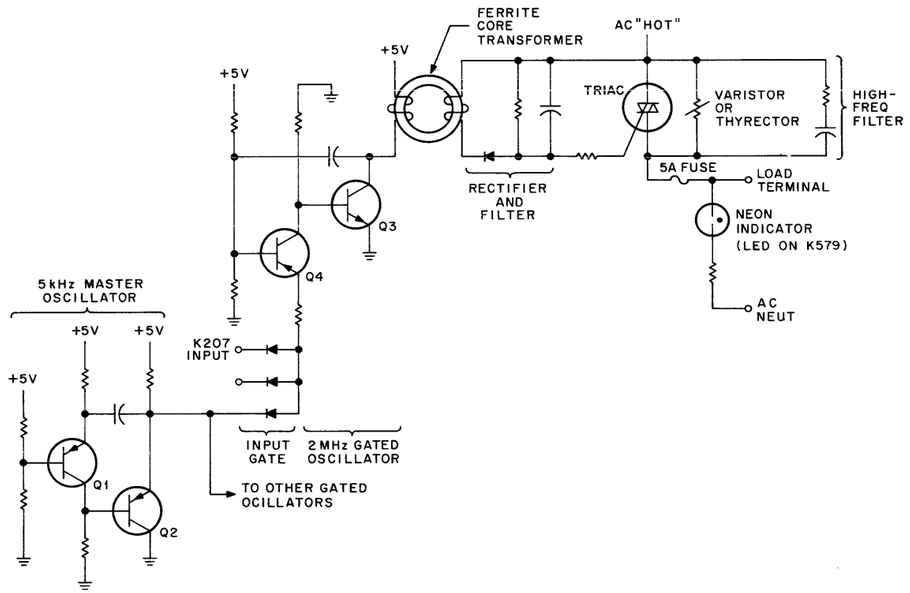


Figure 3-20 AC Isolated Switch

The Triac is switched off by eliminating the gate potential. For this function, the external control flip-flop is switched off. This action disables the slave oscillator input gate. The Triac does not switch off, however, until zero current is drawn by the load.

The Triac circuit has a number of protective features. A 5A fuse protects the Triac from excessive load current and a Varistor (or Thyrector) protects it from high-voltage transients. In addition, a high-frequency filter shunts the device. This filter prevents accidental turn on by high-frequency pulses.

3.6.2.2 **DC Output Driver** – Each K657 module contains four identical dc driver circuits. Each circuit consists of an input gate, a buffer, and a Darlington-pair output switch as shown in Figure 3-21. As denoted, the output stages only switch a load to ground. Each circuit uses an LED to denote that its output is on. A diode clamp is also provided to protect the output stages from inductive transients. This diode is normally connected between the switched output and the positive source and can be clipped out if not needed.

3.6.3 Accessory Box Circuits

3.6.3.1 **Timer Circuits** – Each K302 Timer module contains two independent timer circuits. Each circuit provides standard time delay ranges. These ranges are established by selecting capacitor values for an RC network. A potentiometer, that is also part of the network, enables vernier adjustments within the selected delay range. The selectable delay ranges are as follows:

a. Range 0.01 to 0.3 seconds – The 22 μF and 220 μF capacitors are disconnected from the RC network.
b. Range 0.1 to 3.0 seconds – The 220 μF capacitor is disconnected from the RC network.
c. Range 1.0 to 30 seconds – All three capacitors are connected in the RC network.
d. Range up to 4 minutes, 45 seconds – Capacitance is added to the RC network in place of the jumper.

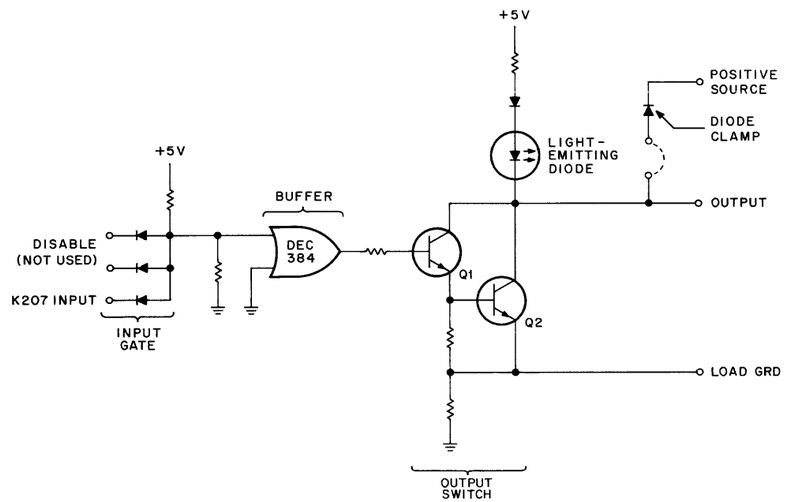
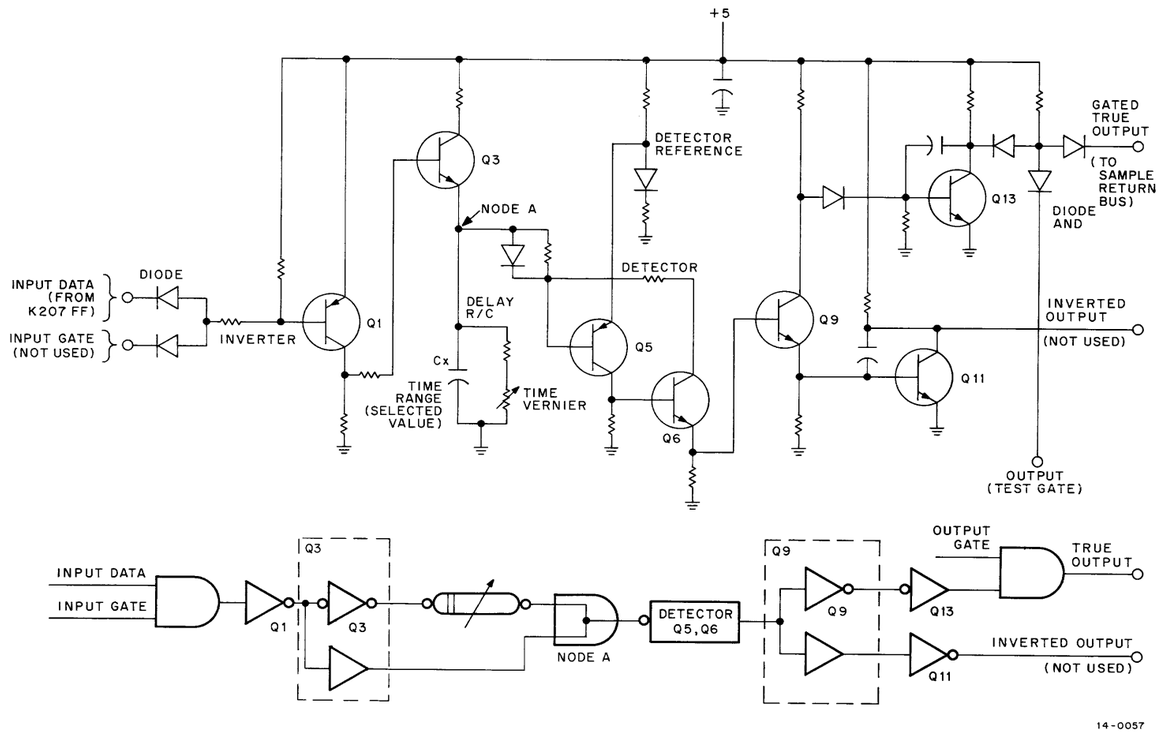


Figure 3-21 DC Driver

Figure 3-22 is a schematic and simplified diagram of a timer circuit. The timer circuit is controlled by a K207 flip-flop input to the diode input gate. With the flip-flop reset, Q1 is on, Q3 is on, and C_x is charged to approximately +5V. With Node A at approximately +5V, Q5 is off, Q6 is off, Q9 is off, and Q13 is on. As a result, the timer output is at ground level.

The delay interval is started when the flip-flop is set. With this action, the positive input to the diode gate switches Q1 off, which, in turn, turns off Q3. With Q3 off, C_x begins to discharge through the resistance of the RC network. Transistor Q5 remains off until the voltage at Node A decreases below the emitter reference of Q5. The time required to reach the turn-on threshold of Q5 is the delay interval for the timer. When Q5 begins to conduct, it turns on Q6. Regenerative feedback (provided by the feedback resistor between the collector of Q6 and the base of Q5) causes Q5 and Q6 to rapidly saturate. The emitter current of Q6 is now provided by the base-emitter junction of Q5. With Q6 on, Q9 turns on and switches Q13 off and Q11 on. The end result is that Q13 provides a logical 1 to the sample return. This output denotes the timer is on.

The timer flip-flop must remain set until the timer completes its timeout. If not, Q3 turns on when the flip-flop is set and ends the delay function. In addition, if the inputs that qualify a timer for turn-on are part of the timer turn-off equation, then they too must remain true during timeout. Figure 3-23 illustrates the timing relationships for these features. The timer flip-flop must be reset (and C_x must again be fully charged) before the timer can be used again.



14-0057

Figure 3-22 Timer Module, Time Delay Circuit, Simplified Schematic Diagram and Equivalent Logic Diagram

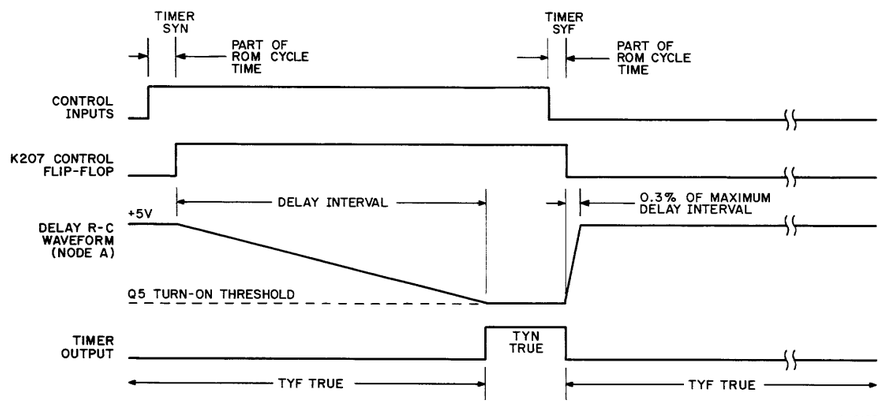


Figure 3-23 Timer Relationships

3.6.3.2 K274 Retentive Memory – During normal operation of the K274, a flip-flop is set by a combination of SET and ENABLE signals for the appropriate memory. It is then reset by RESET and ENABLE for the same flip-flop. The reed relay simply follows the operation of the flip-flop.

The sample return for the PDP-14 is sampled from the flip-flop and not the reed relay; hence, the system does not have to wait on the propagation time of the relay. This means much faster response from the retentive memory than would be possible using the relay contacts.

The relay state is sampled during INITIALIZE H to re-establish the state of the flip-flop before the power failure. Otherwise, the relay only follows the flip-flop. When INITIALIZE H is generated by the PDP-14, it removes power from the relay coils permitting the flip-flop to stabilize before the relay coils are energized when INITIALIZE H is removed.

The LEDs on the K274 module light when the memory is set. The memory can be manually reset by actuating S1. Moving S1 up will clear the upper memory (even addresses) and moving it down will clear the lower memory (odd addresses).

CHAPTER 4
DETAILED MAINTENANCE

4.1 GENERAL

The information presented in this chapter is more in the form of performance standards and measurement procedures rather than adjustment data. However, pertinent adjustment information is included wherever appropriate. In those areas where it is not included, it is assumed the individual servicing the equipment is adequately trained to perform the test, interpret the results, and if necessary, substitute components.

4.2 LEVEL OF MAINTENANCE

The PDP-14 user is encouraged to maintain his controller by judiciously replacing modules thought to be defective with known good modules as described in Chapter 2. This is recommended for two reasons: 1) it is the fastest way to repair the controller; and 2) it requires less training for the maintenance personnel at the site. Time does not permit most users to find specific problems within a module and defective modules can be returned to DEC for repair at a modest charge.

4.2.1 Personnel Intended to Use This Chapter

This chapter contains information intended to aid the well qualified maintenance individual in isolating faults within a module or modular unit. Maintenance at this level should be attempted only by persons thoroughly familiar with Chapters 1, 2, and 3 of this manual and with digital troubleshooting and maintenance techniques.

4.2.2 Relationship to Other Chapters

It is important to re-emphasize that Chapter 2 is intended for the user and the troubleshooting techniques described there would be carried out by the user's electricians. The user might wish to train a few technicians to perform the level of maintenance detailed in this chapter but only after the technicians are thoroughly familiar with the contents of Chapter 3. It is further assumed that the procedures described in Chapter 2 have been thoroughly explored before proceeding with the tests described here.

4.3 TOOLS AND TEST EQUIPMENT

Table 4-1 lists the tools and test equipment recommended for maintenance of the PDP-14. Use of lesser quality instruments is not recommended, as it may seriously affect the reliability of the measurements and lead to false conclusions.

Table 4-1
Recommended Tools and Test Equipment

Item	Model	Manufacturer	Use
VOM	630NA	Triplett	Voltage measurement
Oscilloscope	453	Tektronix	Voltage and waveform measurement
Module Extender	W982	DEC	Access to single-height modules
Module Extender	W984	DEC	Access to double-height modules
Soldering Iron	PU-1	Weller	Module repair
Solder Remover	Standard	Soldapullt	Solder sucker for parts removal
I/O Interrogator	BT14	DEC	Checking input and output conditions
Computer	PDP-8	DEC	Diagnostic

4.4 SYSTEM CHECKOUT

4.4.1 Power Voltage Checks

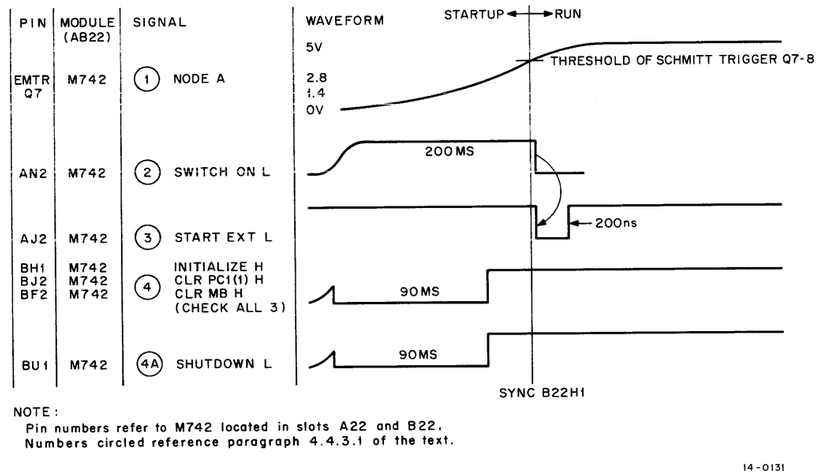
The PDP-14 power supply is designed for a nominal +5 Vdc output. This voltage, measured at terminals 1 and 2 of TB1, should be 5.15V when the PDP-14 is first started with no load. After warm-up the voltage may drop to no less than 4.90V under full load (7A). Should the voltage be incorrect, make the appropriate adjustment on the power supply printed circuit card.

4.4.2 Power Supply Ripple Check

Use a Tektronix Model 453 or equivalent oscilloscope to check the ripple content of the power supply at terminals 1 and 2 of TB1. The ripple should not exceed 10 mV peak-to-peak under full load.

4.4.3 Power-up Sequence and Manual Controls

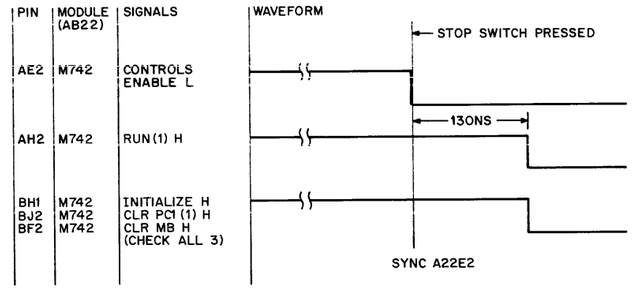
4.4.3.1 Power-up Sequence – The following checks are made on the M742 module located in slots A22 and B22. Each check is performed by turning the power off and then making the appropriate test as power is turned back on. Synchronize oscilloscope on B22H1 for all tests. The waveforms illustrated in Figure 4-1 correspond to the following step numbers.



NOTE:
Pin numbers refer to M742 located in slots A22 and B22.
Numbers circled reference paragraph 4.4.3.1 of the text.

14-0131

Figure 4-1 Startup Timing



NOTES:
1. Pin numbers refer to M742 located in slots A22 and B22.
2. Refer to text paragraph 4.4.3.2 and fig. 4-1 for restart checks.

14-0132

Figure 4-2 Manual Controls Check

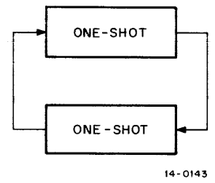
1. Check charging of C14 at the emitter Q7. It should reach the threshold (2.8V) of Q7, Q8 Schmitt trigger in about 200 milliseconds.
2. Check the output of Schmitt trigger Q7, Q8, and Q9. The output at pin AN2 (SWITCH ON L) should drop, then go high for about 200 milliseconds after power is turned on and finally return low.
3. Check that the 200-nanosecond START EXT L pulse is generated at AJ2 by the high-to-low transition of the collector of Q9. This pulse is used to start the PDP-14 timing.
4. Check INITIALIZE H (BH1), CLR PC1 H (BJ2), and CLR MB H (BF2) to ensure they go high for 90 milliseconds after power on. Also check SHUTDOWN L which generates these pulses (BU1).
5. Check INITIALIZE L (BK2) to ensure it goes low for 90 milliseconds after power up. INITIALIZE H is the inverted signal of INITIALIZE L.

4.4.3.2 Manual Controls Check – All of the following tests reference components and pins on the M742 module located in slots A22 and B22. Synchronize the oscilloscope on A22E2 for the following checks. The waveforms illustrated in Figure 4-2 correspond to the following step numbers.

1. Check operation of the STOP switch by depressing it and check RUN (1) H (AH2) to ensure it goes low.
2. Check CONTROLS ENABLE (AE2) and RUN (1) H (AH2) with the processor stopped to make sure it is at 0V. This line enables the START and CONTINUE switches only when the controller is stopped.
3. Before pressing CONTINUE check to make sure INITIALIZE H (BH1), CLR PC1 H (BJ2), and CLR MB H (BF2) have all gone high and INITIALIZE L (BK2) has dropped low. This check ensures that the timing failure detect E3 is functioning properly.
4. Pressing either START or CONTINUE causes the processor to resume timing. The sequence is the same as the power-up sequence described in Paragraph 4.4.3.1 and Figure 4-1 when the switch is released.

4.4.4 Processor Timing Checks

4.4.4.1 General – The PDP-14 is an asynchronous processor; it does not use a common clock and hence each timing component is largely independent of all others. All of the timing in the PDP-14 is accomplished by one-shot multivibrators with the last one-shot in the system triggering the first one to start the next cycle. Note in Figure 4-3 that a free-running multivibrator can be built using two one-shots.



14-0143

Figure 4-3
Free-Running Multivibrator

The on time and off time of a one-shot can be independently controlled. This concept is utilized in the PDP-14 to permit the timing of each part of the system to be optimized. The concept can be further expanded by cascading as many one-shots as are necessary to generate the required number of timing pulses. The length of each pulse is independent of all others.

The PDP-14 System is easy to troubleshoot since a pulse can be injected and then traced as it is propagated through the system. In the PDP-14, depressing START or CONTINUE injects a pulse that starts the timing. The pulse that starts the timing is the START EXT L pulse which can be measured at pin AJ2 of the M742 module. This pulse appears once each time the START or CONTINUE switch is released, provided the controller was halted before activating the START or CONTINUE switch. Figures 4-4 and 4-5 define the timing chain sequence.

4.4.4.2 Processor Timing Assumptions – The following paragraphs assume that the controller switches to a RUN state each time it sees START EXT L. The START EXT L pulse is generated each time the START or CONTINUE switches are pressed and then released. The RUN state is defined by the following conditions:

Signal	State	M742 Pin
INITIALIZE H	Low	BH2
INITIALIZE L	High	BK2
CLR PC1 H	Low	BJ2
CLR MB H	Low	BF2
SHUTDOWN L	High	BU1
CONTROLS ENABLE L	High	AE2
SWITCH ON H	Low	AN2
RUN (1) H	High	AH2

NOTE: Logical High = 3.0 to 5.0V
Logical Low = 0.0 to 0.7V

4.4.4.3 Detailed Timing Analysis (FETCH Cycle) – The following tests are made on the M741 module located in slots A23 and B23. The step numbers refer to numbered waveforms on Figure 4-4. Before proceeding with these tests it is desirable to remove the ROMs (ROM timing is covered in Paragraph 4.4.5). The controller timing will function without the memory. If removing the memory from a PDP-14 which will not run causes the controller to start, the problem is in the memory timing. If the controller still does not run, proceed with the following steps.

The steps are presented with Figure 4-4 to assist the reader in utilizing this type of timing chart for troubleshooting purposes. The procedure for utilizing Figures 4-5, 4-6, and 4-7 is the same and therefore only a general discussion of these timing charts is included.

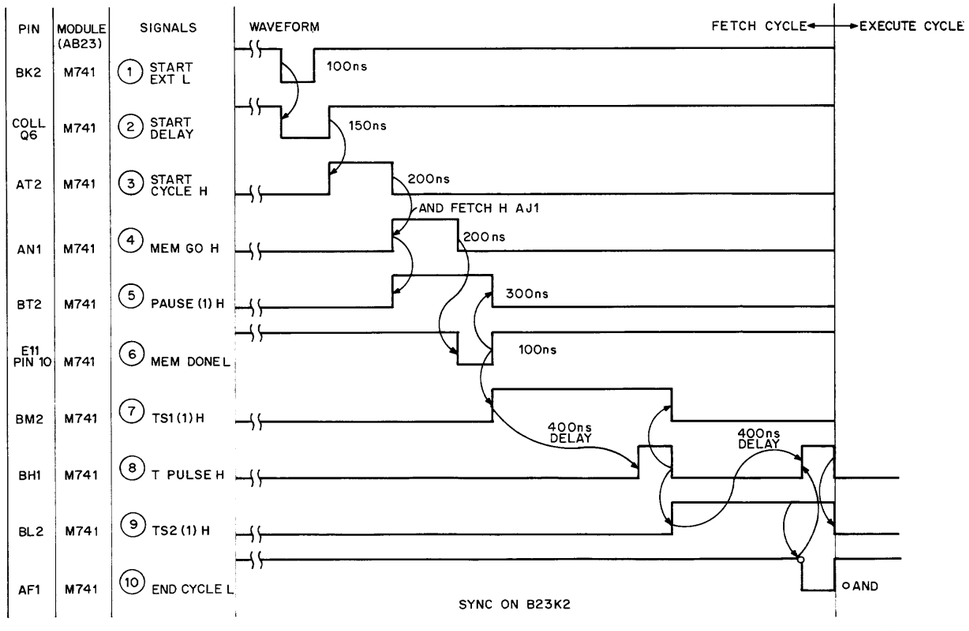


Figure 4-4 FETCH Cycle Timing Analysis (Paragraph 4.4.4.3)

1. Processor timing is initiated by the presence of a pulse at BK2 (START EXT L) that is generated on the M742 module during power up or when the START switch or CONTINUE switch is pressed. If processor timing will not run, it is necessary to inject this pulse by pressing the START or CONTINUE switch. The propagation of the pulses is traced as outlined in the remaining steps.

2. The leading edge of START EXT L triggers the START DELAY which is a 150-nanosecond pulse. The START DELAY pulse can be measured at the collector of Q6 and is 200 nanoseconds in duration.

3. The trailing edge of START DELAY triggers START CYCLE H which lasts 200 nanoseconds and is measured at pin AT2.

4. If FETCH H (pin AJ1) is high, the trailing edge of START CYCLE triggers MEM GO (pin AN1) which is a 200-nanosecond pulse.

5. The leading edge of MEM GO causes PAUSE (1) H (pin BT2) to go high. It is later reset by MEM DONE.

6. With the memory removed, the trailing edge of MEM GO triggers MEM DONE (pin 10 of IC E11, ETCH REV C). This is a 150-nanosecond pulse.

7. The trailing edge of MEM DONE (100 nanoseconds) resets PAUSE (1) H (pin BT2) and initiates TS1 (1) H (pin BM2).

8. The leading edge of TS1 (1) H starts a 400-nanosecond one-shot consisting of E17 and Q8. The output of this timer can be seen at the collector of Q8 as a 400-nanosecond pulse. The falling edge of the one-shot output (collector of Q8) triggers T PULSE (pin BH1) which has a duration of 100 nanoseconds.

9. The trailing edge of T PULSE H (pin BH1) ends TS1 (pin BM2) and initiates TS2 (pin BL2).

10. The leading edge of TS2 starts another 400-nanosecond one-shot consisting of E15 and Q4. The output of this one-shot can be measured at the collector of Q4. The trailing edge of the one-shot then generates another T PULSE H (pin BH1). When both T PULSE H (pin BH1) and TS2 are present, then END CYCLE (pin AF1) is generated.

11. The trailing edge of T PULSE resets TS2 (pin BL2) and END CYCLE (pin AF1) and initiates a START CYCLE (collector of Q6) for the EXECUTE cycle.

4.4.4.4 Detailed Timing Analysis (EXECUTE Cycle: JFF, JFN, SKE, SKZ, TRR, NOP, JMR, and SKP Instructions) – The internal EXECUTE cycle is initiated by the END CYCLE pulse generated at the completion of the FETCH cycle. Before trying to troubleshoot this section, be sure the processor is attempting to execute one of the instructions noted in the paragraph heading. If the memory has been removed and the PDP-8 is not connected, the controller will be executing NOPs and this is the best place to start.

Other instructions can be traced in the same manner using the oscilloscope loop procedure outlined in Paragraph 4.4.8.

Figure 4-5 is the timing diagram for the internal EXECUTE cycle. The troubleshooting procedure is the same as the procedure outlined in Paragraph 4.4.4.3. If the processor will not run, it is necessary to depress the START or CONTINUE switch and then trace the propagation of the pulses through the system.

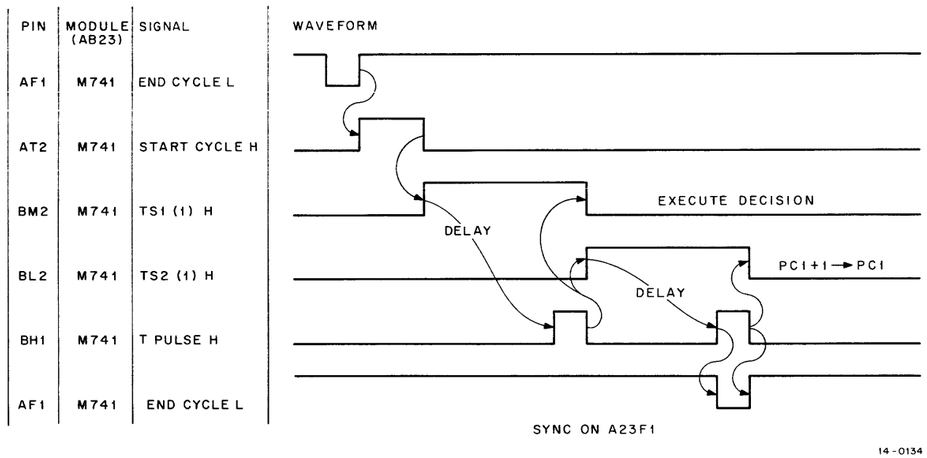


Figure 4-5 Internal Execution (JFF, JFN, SKE, SKZ, TRR, NOP, JMR, and SKP)
(Paragraph 4.4.4.4)

The following actions occur during TS1 and TS2:

TS1

a. No action if the instruction is a NOP.
b. A decision is made and the result of the decision is stored in the JF-OK or SK-OK flip-flop.
c. The register transfer is made if a TRR instruction is being executed.
d. PC1 is updated if the instruction is a JMR or SKP instruction.

TS2

PC1 is updated by adding 1 (i.e., PC1 + 1 → PC1).

4.4.4.5 Detailed Timing Analysis (Two-word EXECUTE Cycle: JMP, JMS, and TRM Instructions) – The 2-word EXECUTE cycle requires an additional access to memory to obtain the data word. This type of instruction is therefore identical to the FETCH cycle, except that the MB is transferred to the register specified by the previous instruction instead of the word being decoded by the IR and then being executed. Therefore, the procedure described in Paragraph 4.4.4.3 can be followed. The timing diagram for the 2-word EXECUTE cycle is shown in Figure 4-6.

4.4.4.6 Detailed Timing Analysis (I/O Execution: TXD, TYD, SYF, SYN, TXF, TXN, TYF, and TYN) – Figure 4-7 shows the I/O cycle beginning with the END CYCLE pulse generated at the end of the FETCH cycle. The I/O cycle is very long to permit gates in the K-Series modules to settle. Therefore, the I/O CYCLE (1) H (pin BU2) is 16 to 18.5 microseconds and I/O STROBE L (pin BR1) is 6.5 microseconds. During the I/O cycle the address to the I/O Box is asserted. The test data is then strobed back to the processor and is stored in the TEST flip-flop by END CYCLE if the tested condition is met. The I/O STROBE is used to turn outputs on or off if the instruction is an SYN or SYF.

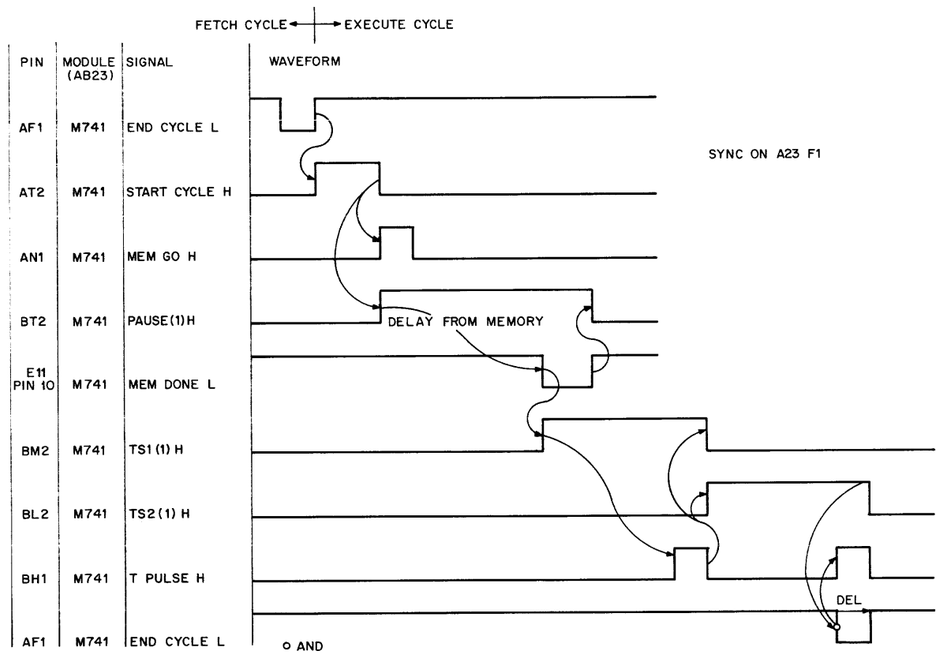


Figure 4-6 Two-Word Instruction Execution (JMS, JMP, and TRM)
(Paragraph 4.4.4.5)

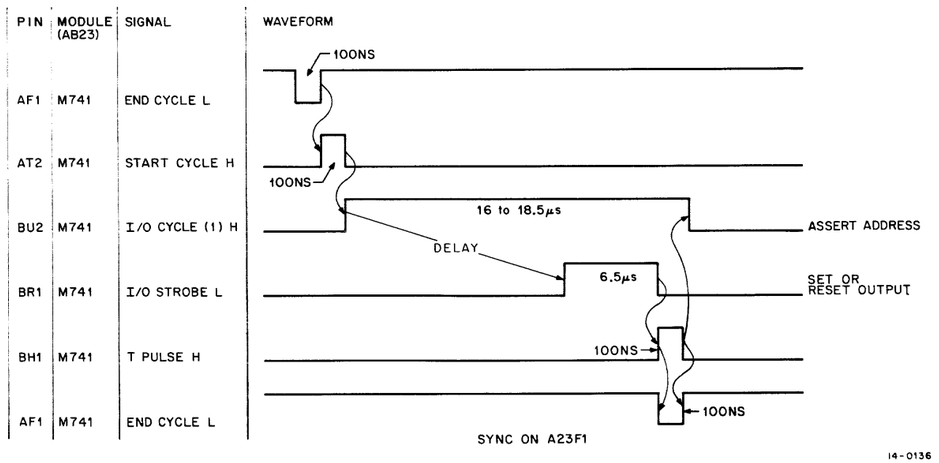


Figure 4-7 I/O Execution Cycle (TXN, TXF, TYN, TYF, TXD, TYD, SYN, and SYF)
(Paragraph 4.4.4.6)

4.4.5 Memory Timing Checks

Figure 4-8 shows the timing relationships in the memory. Memory timing is initiated by MEM GO (pin AL1) and PAUSE (1) H (pin AL2) on the G924 ROM Selection board located in slots A13, B13, C13, and D13 for the first 1K of memory.

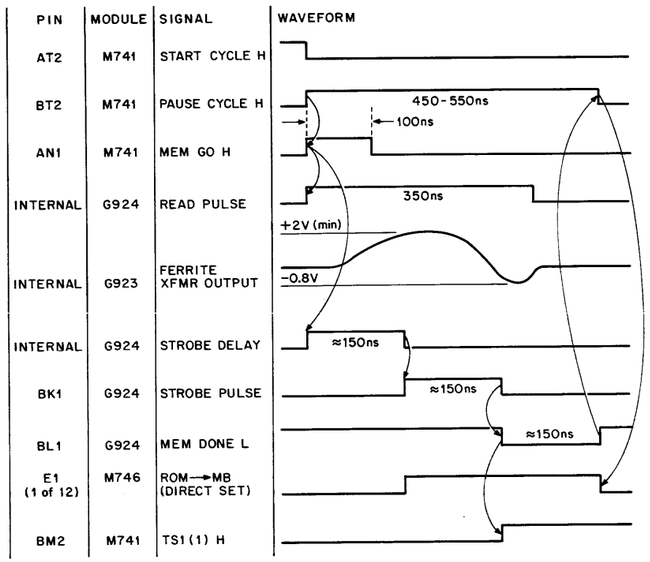


Figure 4-8 Memory Timing Checks (Paragraph 4.4.5)

The output of the Ferrite transformers is connected directly to a gate which is selected by STROBE 1 through STROBE 8. The output of this gate is then connected to a SET-RESET flip-flop which is set by the STROBE PULSE and is cleared at the end of PAUSE.

The data from the memory output is applied to the direct-set inputs of the memory buffer. The data is present at the memory output for about 300 nanoseconds.

It is important to note that the processor timing as discussed in the previous paragraphs must be operating properly before the memory timing can be checked. The step-by-step procedure that is used to check the memory is of the same type as the procedure used to check the rest of the processor.

4.4.6 I/O Timing Checks and Notes

The I/O process is initiated by a START CYCLE H pulse which sets I/O CYCLE (1) H as shown in Figure 4-9. During I/O CYCLE (1) H the appropriate input or output is selected and the K-Series logic in the Input or Output Box is given time to settle. If an SYN or SYF instruction is decoded, the appropriate output is set on or off during I/O STROBE L. If a Test instruction (TXN, TXF, TYN, TYF) is decoded, nothing happens until END CYCLE when the results are strobed into the TEST flip-flop. If the test is true, the TEST flip-flop is set; if the test is not true, the condition of the TEST flip-flop remains the same.

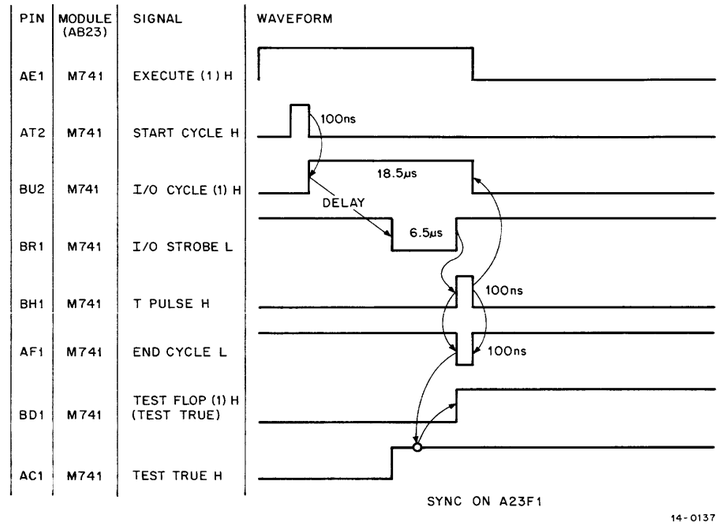


Figure 4-9 I/O Timing Checks (Paragraph 4.4.6)

The address and sample return lines are connected to all boxes and the package select line to only one box. Therefore, consider the following points when troubleshooting the I/O system on the PDP-14:

a. If 50 percent of the test instructions are yielding false results, the sample return lines should be checked for an open or short circuit condition.

b. If a given input in every Input Box or a given output in alternate Output Boxes yields false results, the address lines from the M743 module should be checked.

c. If one entire Input or Output Box is inoperable, check the package select lines.

d. If only one input or output malfunctions, check the modules in the I or O Box.

4.4.7 Computer Interface Check

The DA14 Computer Interface between the PDP-8 family computer and the PDP-14 can be used for a variety of applications. The most common use of the interface is during startup of the PDP-14 to develop and test the program which the ROM will eventually contain. The second mode of operation permits the PDP-8 to monitor functions being performed by the PDP-14 or to use the PDP-8 to analyze analog data and then have the PDP-14 execute the decision. In either event, the hardware is the same.

Figure 4-10 illustrates the basic relationship between the PDP-8 and the PDP-14.

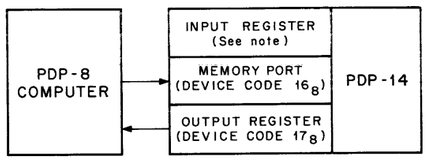


Figure 4-10 PDP-8/PDP-14 Interface

Using the DA14 Computer Interface, the PDP-8 can transfer instructions to the Memory Port or determine events in the PDP-14 by reading the Output Register.

There are three registers which permit the PDP-14 to communicate with the PDP-8. The most frequently used register is the Memory Port. When instructions are entered into the PDP-14 via the Memory Port, the PDP-14 operates exactly as though the information is coming from its Read-Only Memory. The second register is the Output Register which displays information about inputs and outputs as directed by the PDP-14. The results of tests on inputs and outputs are displayed in the Output Register.

The third register is the Input Register. The Input Register will not be discussed in this chapter because it is used at very few installations and is not available in late model machines wired for MAP-14.

Many of the problems which appear to be PDP-14 problems may be due to a PDP-8 I/O bus problem, skip and interrupt bus problem, or cable problem. However, before any troubleshooting can begin, the PDP-14 timing must be operating. This can most easily be determined by checking INITIALIZE on pin B23H1 of the M741 module.

With the PDP-14 running, run TEST-14 which will check the entire PDP-14 Processor and the computer interface. The following tests should only be used if TEST-14 prints PDP-14 HUNG or PDP-14 STOPPED and it is known that the PDP-14 is actually running, or the PDP-14 is not executing instructions properly as received from the PDP-8. The PDP-14 is running if INITIALIZE H (pin B22H1) is low.

The short patch presented in Table 4-2 performs the functions listed below. It should be used in conjunction with Figure 3-18 and the associated test.

a. Generate a PDP-14 interrupt.
b. Place the PDP-14 in external mode.
c. Transfer all 1s from the PDP-8 through the Memory Port to the Output Register and back to the PDP-8 through the Output Register.
d. Return the PDP-14 to internal mode.
e. Halt the PDP-8 with all 1s in the AC.

By replacing HLT with NOP the computer will loop and any of the BAC, BMB, or skip and interrupt lines on the PDP-8 can be checked. The following items can then be easily scoped to check if they are operating properly.

a. Interrupt flip-flop on M745.
b. External mode flip-flop on M745.
c. BMB lines should all be 1s at one time.
d. BAC lines should all be 1s at one time.
e. The skip and interrupt buses on the PDP-8 can be checked.
f. The Output Register should contain all 1s after one pass.
g. The AC should contain all 1s after the computer stops.

Table 4-2
Short Patch for Computer Interface Checkout

```
7600  7300  START,  CLA CLL          /CLEAR AC & LINK
7601  1222          TAD EEM          /GET EEM
7602  6165          GNI              /INTERRUPT PDP-14
7603  6161          SEF              /WAIT FOR COMPLETION
7604  5203          JMP .-1
7605  1224          TAD K4226        /LOAD TRM
7606  6164          LDE
7607  6161          SEF
7610  5207          JMP .-1
7611  7240          CLA CMA          /AC=7777
7612  6164          LDE              /LOAD PDP-14 MEMORY PORT
7613  6161          SEF              /WAIT FOR EXTERNAL FLAG
7614  5213          JMP .-1
7615  1223          TAD LEM          /LEAVE EXTERNAL MODE
7616  6164          LDE
7617  6176          ROR              /GET OUTPUT REGISTER TO AC
7620  7402          HLT              /HALT WITH 7777 IN AC
7621  5200          JMP START        /DO AGAIN
7622  0600  EEM,     0600
7623  0400  LEM,     0400
7624        K4226,   4226
```

If any of the above conditions are not met, then a thorough investigation of the problem must be undertaken. Remember that PDP-8 diagnostics may not necessarily find problems related to the I/O bus. This test should be repeated after replacing the CMA with a NOP which will cause conditions c, d, f, and g to be all 0s instead of all 1s. Figure 3-18 may be of assistance in determining the timing of the interface.

4.4.7.1 Running Standard DEC Software on the Serial-Line Interface – All DEC standard software for program development and diagnostic purposes, including patches contained in this manual, can be run on the serial-line interface. In order to do this, it is necessary to set up the Channel Status Register using the following short program:

Location	Contents	Comment
7600	7604	LAS
7601	0206	AND K17
7602	6143	LCSR
7603	7602	HLT CLA
7604	5605	JMP I ± 1
7605	0200	200
7606	17	K17, 17

To use this program, proceed as follows:

1. Load the desired program (i.e., ABE-14, DEMON-14, etc.) in the normal manner.
2. Once it is loaded, toggle the above program into core in the same manner as the RIM loader.
3. Load the starting address which is 7600.
4. Set the Switch Register equal to the channel number of the PDP-14 to be worked with.
5. Press CLEAR, then CONTINUE.

The program sets up the Channel Status Register, and if CONTINUE is pressed, a jump to location 200 is executed and the program loaded in Step 1 above starts. If the program starts at an address other than 0200, do not press CONTINUE, but instead start the program in the conventional manner.

4.4.8 Scope Loops and How You Get Them

4.4.8.1 General – Scope loops are used to make the controller perform a given function repeatedly in order to scope a given function within the controller. They are particularly useful when troubleshooting functions within a module.

4.4.8.2 Procedure – To set up scope loops, proceed as follows:

1. If necessary, connect the computer using the instructions in Paragraph 2.4.2.
2. If necessary, load RIM and BIN loaders using the instructions in Paragraph 2.4.3.
3. If necessary, load TEST-14 tape using the instructions in Paragraph 2.4.4.
4. To address TEST-14, depress computer STOP key, set SR to 0200, then depress LOAD ADDR key.
5. If Spare Register is not provided, set SR6 to 1, then depress START key.
6. Answer program queries for I, O, and A Boxes by typing 0s, then depress RETURN key.
7. The program now begins testing the controller.
8. When the program detects an error it types out the error, then halts. If it is desired to loop on the first error, simply place SR0 to 1 before the teleprinter completes the error typeout. If not, depress computer CONTINUE key.
9. The program then resumes testing until another error is detected. Repeat Step 8 until the desired point in the program testing is reached.

4.5 I/O TROUBLESHOOTING

The PDP-14 uses four address (ADD) lines and eight package select lines to address inputs and outputs and four sample return (S RET) lines for testing inputs and outputs. The ADD and S RET lines are paralleled to all Input and Output Boxes; therefore, a fault at any point (backplane, cables, I, O, or A Boxes) will affect all boxes.

Each S RET line connects to either all Input Boxes or one-half of all the Output Boxes. On the input side, an S RET line connects to either the lower half (address $0–17_8$) or upper half (addresses $20–37_8$) of all Input Boxes. On the output side, each S RET line connects to either all outputs plugged into the C Row of the controller or to all outputs plugged into the D Row of the controller. If any of these four lines are grounded, it will cause one-half of the inputs (low or high side of the box) or one-half of the outputs (C Row or D Row) to test "on".

The C-Row output S RET line is also connected to one pin of all sockets in the D Row so that Input Boxes may be plugged into slots in Row D to provide additional input capability. When inputs are used in output slots, these inputs must be tested with a TYF or TYN instruction.

Each package select line affects one Input Box and two Output Boxes. Therefore, if one of the package select lines is grounded or open, it will affect a maximum of three boxes.

Because each of the types of addressing lines affect the I/O Boxes in a different way, it is possible to isolate the fault rather quickly with a PDP-8 computer or a BT14 Interrogator Box. Take time in the beginning to establish whether or not the input or output failures are falling into a pattern. Table 4-3 should assist in identifying the fault.

Table 4-3
I/O Fault Identification

Type of Fault	Solution	Paragraph
All tests showing true (or false)	Test True line	4.5.1
0–17 addresses in all I Boxes failing	XS RET 0 H	4.5.2
20–37 addresses in all I Boxes failing	XS RET 1 H	4.5.2
C Row, O Box testing fails	YS RET 0 H	4.5.2
D Row, O Box testing fails	YS RET 1 H	4.5.2
Same address failing in all boxes	ADD 1-2-4-8	4.5.3
Alternate addresses failing in all boxes	ADD 1 H	4.5.3.1
Addresses fail in groups of two	ADD 2 H	4.5.3.2
Addresses fail in groups of four	ADD 4 H	4.5.3.3
Addresses fail in groups of eight	ADD 8 H	4.5.3.4
A maximum of one I Box and two O Boxes failing	Package Select (PS*n*H)	4.5.4
Only one address fails	Module or wire in box	4.5.5
Cannot set or reset outputs	Set or reset lines	4.5.6
SYF 377 will not clear all outputs	Clear line (CLEAR I/O L)	4.5.7
A Box problem	A Box	4.5.8

4.5.1 Test True

The sample return from the Input and Output Boxes is compared with the type of test being performed. The result is placed on the test true line A23C1, TEST TRUE H. For example, if a TXF 001 is being executed and Input 1 is off, TEST TRUE H will go high momentarily. However, if Input 1 in the example is on, TEST TRUE H will remain low. The state of TEST TRUE H is stored in the TEST flip-flop on the M741 module. To check these lines, synchronize the oscilloscope on B23U2 (I/O CYCLE 1 H) and observe A23C1 (TEST TRUE H). The 1 side of the TEST flip-flop can be observed at B23D2. The TEST flip-flop can only be set by the TXN, TXF, TYN, or TYF instructions and is cleared by the JFF or JFN instructions or INITIALIZE.

4.5.2 Sample Return Troubleshooting

Synchronize on B23U2 (I/O CYCLE 1 H). Test all input slots, pins D2 (XS RET 0 H), and pins B2 (XS RET 1 H).

The PDP-14 utilizes four sample return lines (S RET). XS RET 0 H returns the test status for addresses $0_8 – 17_8$ (left side) of all I Boxes. XS RET 1 H returns the test status for addresses $20_8 – 37_8$ (right side) of all I Boxes. YS RET 0 H returns the status of all O Boxes plugged into the C Row of slots in the controller. YS RET 1 H returns the status of all O Boxes plugged into the D Row or YS RET 1 H returns the status of inputs $20_8 – 37_8$ when an Input Box is plugged into the D Row output slots to expand the input capability. YS RET 0 H returns

the low side (0_8 – 17_8) of these boxes. If an input is plugged into the D Row, the slot above it in C Row cannot be used. The most common problem is that one of these lines is grounded and indicates that the input or output being tested is on. The S RET line should remain high until an on input or output is tested, at which time it should go low for 5 to 15 microseconds and then return high. Generally, the fault can be most easily isolated by removing all cables from the processor, replacing them one at a time and checking the sample return after replacing each one. The source of the S RET in the I Boxes is the input converter (K579 or K564) which uses the K136 module to drive the S RET line to the controller. The source for the sample return line in the O Boxes is the K207 module which uses the K135 to drive the YS RET to this controller. The system has no way of knowing if the output module (K616 or K657) is responding. See Paragraph 4.5.8 for a discussion of the sample returns in the A Box.

4.5.3 Address Line Troubleshooting

The PDP-14 utilizes four address lines which select two inputs in the same box and one output in each of two boxes (one O Box plugged into Processor Row C and one in Row D). To test these lines it is necessary to use either a computer running a scope-loop program (Table 4-4) or the interrogator box. Synchronize the oscilloscope on the leading edge of I/O CYCLE 1 H (B23U2) and watch for an 18 to 22 microsecond high-going pulse on the lines corresponding to the address being selected. Use SYF 377 (3377_8) to assert all address lines.

The four address lines are decoded in the I, O, or A Boxes by the K161 decoders to select the appropriate point. Again, a scope loop or interrogator box can be used to determine if they are working properly. Synchronize the oscilloscope on the leading edge of I/O CYCLE 1 H (B23U2) and use the program listed in Table 4-4.

Table 4-4

Scope Loop Program for Testing an Input or Output

Location	Contents		Comments
7600	7300	CLA CLL	/CLEAR AC AND LINK
7601	7604	LAS	/SWITCHES CONTAIN INSTRUCTION
7602	6165	GNI	/INTERRUPT PDP-14
7603	6161	SEF	/WAIT FOR PDP-14 EXTERNAL FLAG
7604	5203	JMP .-1	
7605	5200	JMP .-5	/DO AGAIN

SET SWITCH REGISTER TO:

TXF	2000	+XXX	WHERE XXX IS INPUT TO BE TESTED
TXN	2400	+XXX	WHERE XXX IS INPUT TO BE TESTED
TYF	1000	+XXX	WHERE XXX IS INPUT TO BE TESTED
TYN	1400	+XXX	WHERE XXX IS INPUT TO BE TESTED
SYF	3000	+XXX	WHERE XXX IS INPUT TO BE TESTED
SYN	3400	+XXX	WHERE XXX IS INPUT TO BE TESTED
CLR	3377		SAME AS SYF 377

Example: To test input 24 for an off condition, the instruction is TXF 24 OR 2000 + 024 = 2024.

4.5.3.1 Address Line 1 – Synchronize on B23U2 (I/O CYCLE 1 H). Test A32N2 (ADD 1 H). Address line 1 (ADD 1 H) is the least significant bit. If it remains low (i.e., grounded at some point on the system), it will inhibit the selection of all even-numbered inputs and outputs (i.e., 0, 2, 4, etc.). If it remains high (probably a bad driver on the M743 module), it will inhibit selection of all odd-numbered inputs and outputs (i.e., 1, 3, 5, etc.). Use the procedure described in Paragraph 4.5.3 for troubleshooting.

4.5.3.2 Address Line 2 – Synchronize on B23U2 (I/O CYCLE 1 H). Test A32R2 (ADD 2 H). Address line 2 (ADD 2 H) affects inputs and outputs in groups of two. If it remains low (i.e., grounded), it will inhibit selection of inputs 0 and 1, 4 and 5, etc. Use the procedure described in Paragraph 4.5.3 to troubleshoot.

4.5.3.3 Address Line 4 – Synchronize on B23U2 (I/O CYCLE 1 H). Test A32T2 (ADD 4 H). Address line 4 (ADD 4 H) affects inputs and outputs in groups of four. Therefore, if it is grounded, it will always select a number between 0_8 – 3_8, 10_8 – 13_8, etc. If it remains high, indicating an open wire or defective driver on the M743 module, it will always select an alternate number (i.e., in the range of 4_8 – 7_8, 14_8 – 17_8, etc.).

4.5.3.4 Address Line 8 – Synchronize on B23U2 (I/O CYCLE 1 H). Test A32V2 (ADD 8 H). Address line 8 (ADD 8 H) affects the inputs and outputs in groups of eight. If this line is grounded, it will always select a number between 0_8 – 7_8 and 20_8 – 27_8 in the Input Boxes or 0_8 – 7_8 in the Output Boxes. If the line remains high, indicating a bad wire or open driver on the M743 module, it will always select a number between 10_8 – 17_8 and 30_8 – 37_8 in the Input Boxes or 10_8 – 17_8 in the Output Boxes. Use the procedure described in Paragraph 4.5.3 to troubleshoot.

4.5.4 Package Select Lines

Synchronize on B23U2 (I/O CYCLE 1 H). Test pin L2 of failing input or output slot on the controller (PS*n*, where *n* is 1, 2, ..., 8).

Each package select line selects one Input Box and two Output Boxes. If it is grounded, it will inhibit selection of a maximum of three boxes (depending on the configuration). The inputs or outputs in these three boxes will always test off since no package is being selected. If one of the package select lines remains high, the test results will be correct for the selected boxes and the results for any other boxes will be the inclusive-OR of the selected box and the box whose package select line is high. Package select lines are on pin L2 of each input slot (total of eight lines).

4.5.5 Only One Address Fails

When only one address fails, the trouble may be in a number of places. If the system is rather small (not large enough to have more than one address affected), it could be one of the problems described previously. If it is a Test instruction that fails, the module-swapping technique described by the flow chart in Chapter 2 should be thoroughly utilized. If this does not locate the problem, a broken wire in the box should be suspected since any of the wires connected to the controller will affect more than one input or output.

4.5.6 Set and Reset Lines

Synchronize on B23U2. Test F2 (E SET *n* H) of failing output slot, or K2 (ER SET *n* H) of failing output slot, where *n* is 0 or 1.

The same addressing lines (i.e., address 1, 2, 4, 8 and package select) are used to set or reset the outputs. In order to set an output on, the selection lines are asserted and then one of two set lines is asserted (high). To reset an output, the addressing lines are asserted and then one of two reset lines are asserted. The set lines are E SET 0 H (pin F2 of all C Row output slots) and E SET 1 H (pin F2 of all D Row output slots). The reset lines are ER SET 0 H (pin K2 of all Row C outputs) and ER SET 1 H (pin K2 of all Row D output slots). Each of these lines connect to eight Output Boxes and should one become grounded, it will be impossible to set or reset a large number of outputs.

4.5.7 Clear Lines

The SYF 377 instruction will clear all outputs except the retentive memories. Should the outputs be clearing occasionally, the system could be going into initialize (power low) or the system could have an intermittent ground on the clear line. If the line were held high, it would not permit the system to be cleared. The clear line can be observed on pin J2 of any output slot (CLEAR I/O L).

4.5.8 A Box

The S RET in the A Box is connected to the accessory device rather than the K207 module as in the O Box. The accessory device acts as the connection between the output of the K207 module and the S RET line. For example: the K022 will report the status of the K207 in order to use the output as a storage bit; the K302 module provides an adjustable delay between the time the K207 is set and the time the S RET line indicates to the controller that the output is on; the K272 or K274 modules contain a mechanically-latched relay which is sampled. The relay will not be reset by the initialize condition and will therefore retain its state through a power failure.

4.6 TIMER ADJUSTMENT

4.6.1 Timer Adjustment With a Computer

Use the following procedure to adjust the timer with a computer.

1. Ensure the appropriate capacitors on the timer have been clipped (Figure 2-10).
2. Connect the PDP-8 if not already connected according to Paragraph 2.4.2.
3. If necessary, toggle in RIM Loader using the instructions in Paragraph 2.4.3.
4. If necessary, load ABE-14 tape using the procedure in Paragraph 2.4.4 for loading diagnostic tapes.
5. Turn on computer, teleprinter, and PDP-14.
6. To address ABE-14, depress computer STOP key. Set SR to 0200, then depress LOAD ADDR key.
7. Set SR3 to a 1 which will cause ABE-14 to continually time the first timer and print the time in milliseconds on the teleprinter.
8. Depress computer START key. The program then types:

   A BOX IS CONNECTED TO SLOT.
9. Respond to this statement by typing the connector slot letter for the A Box to be tested. (Refer to Figure 2-1 for connector slot designations and locations.) The program then types:

   IDENTIFY THE HARDWARE ASSOCIATED WITH EACH ADDRESS BY TYPING T FOR TIMER, M FOR RETENTIVE MEMORY. ALL ELSE EMPTY.
10. Identify the hardware in each slot using Figure 2-4 as a guide.
11. The program will automatically run after you identify address 0017.
12. Adjust the timer while the computer is running the test, but be sure to get two successive time typeouts at the time setting you desire.
13. The program may be stopped and restarted by pressing the STOP and CONTINUE keys.
14. To proceed to the next timer, set key SR3=0 until the teleprinter stops printing the time, then set SR3=1 again to repeatedly test the next timer.
15. Repeat Steps 12 through 14 until all timers have been set to the desired time.

4.6.2 Timer Adjustment Without a Computer

If a computer is not available, a timer can be set reasonably close using the following procedure. It is suggested that you practice Step 3 on the new module before attempting it on the defective module.

1. Remove the defective K302 module from the A Box.
2. Use a piece of tape to make a flag on a small screwdriver (Figure 4-11).

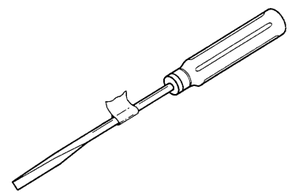


Figure 4-11 Tape Flag for Counting Screwdriver Turns

3. Turn the screwdriver adjustment *counterclockwise* while *carefully* counting the turns; listen carefully for a click. The click must be heard the *first* time it occurs. Count the turns to the nearest 1/8th turn (e.g., 11-3/8 turns).
4. Subtract one turn from the number of turns counted in Step 3 (e.g., 11-3/8 – 1 = 10-3/8).
5. After turning the potentiometer on the new module fully counterclockwise, carefully turn the *same* adjustment on the new module *clockwise* the number of turns determined in Step 4 (e.g., 10-3/8 turns).
6. Repeat Steps 3 through 5 for the other timer adjustment on the K302 module.
7. Clip and remove the same capacitors on the new module that were clipped on the old module.
8. Insert the new module into the slot vacated by the old module.

4.7 MEMORY TROUBLESHOOTING

4.7.1 General

Before attempting repairs at the level described in this section, the procedure outlined in Chapter 2 (Paragraph 2.4.8) should be utilized. Furthermore, the technician must be thoroughly familiar with the theory of operation of the memory as described in Paragraph 3.5.6. Any fault that appears in the memory will usually manifest itself as a group of instructions that are not being retrieved properly. Therefore, thorough analysis of the memory will usually yield a pattern indicating the problem.

To make the above analysis, LOAD-14 and VER-14 diagnostics must be used in conjunction with a computer. It is important that the technician be thoroughly familiar with Paragraph 2.4.8 on using VER-14 for ROM fault isolation. Study the output of VER-14 to determine how it relates to the faults listed in Table 4-5. Once the type of fault has been determined, study the appropriate paragraph and perform the tests outlined in that paragraph.

Table 4-5
ROM Fault Isolation

Type Fault	Cause	See Paragraph
No memory output and:		4.7.2
a. Controller halts	Timing	4.7.2.1
b. Controller is running	Buffer or Strobe	4.7.2.2
One bit in every word set or cleared.	Buffer or MB	4.7.3
Every eighth word bad.	Sense Amp	4.7.4
Groups of eight words bad.	Bad Wire	4.7.5
One bad word out of every 10_8.	Strobe 1–8	4.7.6
Group of 8 bad words in 100_8.	Current Switch	4.7.7
1 or 2 groups of 100_8 words out of 1K memory.	Matrix base drivers	4.7.8
No output from one-half of memory (i.e., 512_{10} of 1024_{10}).	One-half memory select	4.7.9
Count select 1K of memory or selecting more than 1K.	Field select on M742	4.7.10

4.7.2 No Memory Output

The two conditions under which there would be no memory output are: 1) memory timing has failed and the information is never strobed to the buffer contained in the memory system; and 2) the strobe to the buffer in the memory system has failed or the buffer is not being cleared.

The following two paragraphs describe in detail how to troubleshoot these two situations.

4.7.2.1 No Memory Output and Processor is Halting – Synchronize the oscilloscope on PAUSE (1) H (B23T2) and observe MEM GO H (AL2 of the G924 in doubt). Use the procedure described in Paragraph 4.4.5. The presence of the MEM GO H pulse indicates that the memory is getting a start pulse. If this pulse is not present, check the processor timing as described in Paragraph 4.4.4.

If the MEM GO H pulse is present, then check MEM DONE L on pin A23E2. If MEM DONE L is present, it indicates that the memory timing is all right and the timing problem must be solved before further troubleshooting can take place on the memory. If MEM GO H is present and MEM DONE L is not, refer to Paragraph 4.4.6.

4.7.2.2 No Memory Output and the Processor Continues to Run – A number of faults can cause this condition. First, the strobe that loads the buffer on the G923 Sense Amplifier board must be checked. STROBE is generated on the G924 ROM Selection Board and connects to the G923 Sense Amplifier at pin BV1. This signal strobes the data from the sense amplifiers to the buffer, and if it is not present, the buffer will never be loaded. This condition would be characterized by the memory outputting all 0s.

If the memory is outputting all 1s, it is probably not being cleared by PAUSE (1) H at pin BU1 on the G923 board.

4.7.3 One Bit in Every Word Set or Cleared

This condition is usually caused by a fault in the data path on the G923 Sense Amplifier board or the M746 module in C18 or D18. For purposes of clarity, only bit 0 will be discussed, but the data paths of all bits are the same (only the specific pin locations change).

If bit 0 is failing, first determine if it is failing in all memory stacks by observing the output of the memory buffer (C18D2). If part of the memory is working and another portion is not, it suggests that the M746 module is all right. On the other hand, if the bit is always set (or cleared) and the input to the M746 module (C18E1 for bit 0) is changing, the problem is in the M746 module. Replace the M746 module and check again. If the output is still failing, replace the M744 module and recheck. If the M746 output is still bad, check the backplane wiring on the output side of the M746 module.

Having eliminated the M746 as a possibility (i.e., the input to M746 is static) the problem is on the G923 Sense Amplifier board or in the backplane between the two. Use a module extender and check the line connecting to pin 12 of E26 on Drawing G923-0-1 (for bit 0). This is the wired-OR of all the gates that strobe data into the buffer consisting of E25 and E26. If this line is static, determine which gate is causing the problem and replace it.

4.7.4 One Bit in Every Eighth Word is Bad

This condition is caused by a problem on the G923 Sense Amplifier board. Using bit 0 as an example, if T85 (Drawing G923-0-1) is open, gate E6 will always see an AND condition and will always set bit 0 to a 1 whenever STROBE 8 is generated. If the sense winding is shorted or STROBE 8 is not present, gate E6 cannot see the AND condition and the flip-flop formed by E25 and E26 remains cleared. These same conditions could be caused by a broken core in the memory and this possibility should be investigated first. The cores can be examined by carefully disassembling the memory.

4.7.5 Groups of Eight Words Bad

Whenever VER-14 shows one group of eight words to be bad, the problem is on the G922 ROM Braid board or the G924 ROM Selection board. The wire for the defective address is open or shorted to ground. Carefully examine the wires from the braid where they are soldered to the connector pins. Examine the pin corresponding to the defective address and carefully resolder the connection if necessary. If the wire is broken, install a new wire on the other side of the ROM as though you were changing it. For a detailed description of how this is done, refer to the *PDP-14 User's Manual.* This problem could also be due to a failure of the transistor driving the wire in question (i.e., Q1 to Q128 on Drawing G924-0-1).

4.7.6 STROBE 1 to STROBE 8

The three least significant bits of the address contained in PC1 select which strobe line on the G923 board is asserted. PC1, bits 9–11, are decoded to one of eight lines by E34. E32 and E33 then AND the output with the memory strobe from G924 to form STROBE 1–8. A failure anywhere in the strobe system will cause one word in every eight to fail.

4.7.7 Current Switches

PC1, bits 6, 7, and 8, are decoded by E10 (Drawing G924-0-1) to one of eight lines. Each of these eight lines then drives a current-switch transistor which grounds the emitters of sixteen other transistors. If one of the current switches is not functioning properly, a total of 128 words from the memory will fail in groups of eight. The current switches are Q133 to Q140 on Drawing G924-0-1.

Observing the collector of each of the current-switch transistors will indicate whether or not that line is working properly.

4.7.8 Matrix-Base Driver Transistors

Bits 3, 4, and 5, of PC1 are decoded by E5 (Drawing G924-0-1) to one of eight lines. Each of these eight lines drives two gates. One of the two gates is enabled by PC1, bit 2. The output of the selected gate drives the base of eight transistors. The matrix transistor is fully selected when the appropriate current switch is enabled by PC1, bits 6–8, and the base is enabled by PC1, bits 2–5.

4.7.9 One-Half Memory Select

PC1, bit 2, selects one-half of a Read-Only Memory stack. If this line is low, it selects the lower half of the ROM and if high, it selects the upper half of the ROM. A failure in this line (it is held high or low) will not permit the system to access one-half of each ROM. The failure could be in PC1, the backplane wiring, or on the G924 ROM Selection board.

4.7.10 Field Select

Bits 0 and 1 of PC1 are decoded on the M742 module to one of four lines. Each of these four lines connect to 1K of ROM. PC1, therefore, selects the appropriate ROM bank via these lines. A failure in PC1 would cause the system to select the same 1K of memory more than once. A failure on the M742 module would not permit a ROM to be selected or to be selected at all times. If a ROM bank is not selected, system timing fails and if selected all the time, it will cause an inclusive-OR of the selected memory and the defective one.

4.8 TROUBLESHOOTING AND REPAIR TECHNIQUES

4.8.1 Logic Troubleshooting

Logic troubleshooting in the PDP-14 is best accomplished using the technique of "reverse signal tracing". That is, when a malfunction has been isolated to a section of logic, duplicate that type of failure using a small program or a scope loop option in a diagnostic MAINDEC. Then, by comparing the logic drawings with the machine status, and tracing the faulty signal back to the failing gate, that portion of logic which is causing the failure becomes evident.

NOTE
An unconnected input to an M-Series gate, if not tied to a terminator, floats at approximately +2.0V.

Before attempting to troubleshoot the logic, ensure that proper and calibrated test equipment is available. Always calibrate the vertical preamplifier and probes of the oscilloscope before using them. Make certain that the oscilloscope has a good ac ground, and keep the dc ground from the probe as short as possible.

Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control pulses or by level transitions which are available at individual module terminals on the wiring side of the logic. Care should be exercised when probing the logic to prevent shorting between pins. Shorting of signal pins to power supply pins can result in damaged components. Within modules, unused gate inputs are held at +3V.

WARNING
Standard safety practices should be observed when working with energized equipment. Remember that the controller convenience outlet is energized even when the PDP-14 is off.

4.8.2 Module (Circuit) Troubleshooting

Schematic diagrams of each module are supplied with the PDP-14 and should be referenced for detailed circuit information. Copies of the schematic diagrams are contained in Appendix B of this maintenance manual.

Visually inspect the module on both the component side and the printed-wiring side to check for overheated or broken components, etc. If this inspection fails to reveal any signs of trouble or fails to confirm a fault condition, use the multimeter to measure resistance.

CAUTION
Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistance of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. (Front-to-back ratio should always be greater than 10 to 1.) If readings in each direction are the same and no parallel circuit paths exist, replace the diode.

Measure in both directions the emitter-collector, collector-base, and emitter-base resistances of transistors. Short circuits between collector and emitter or an open circuit in the base-emitter path cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base, or between the collector and the base in the forward direction, and an open circuit condition exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back-to-back. In this analogy, PNP transistors would have cathodes connected together to form the base, and both the emitter and collector would assume the function of an anode. In NPN transistors, the base would be a common-anode connection and both the emitter and collector would be the cathode.

Multimeter polarity must be checked before measuring resistance because many meters apply a positive voltage to the common lead when in the resistance mode.

Since integrated circuits contain complex circuits with only the input, output, and power terminals available, static multimeter testing is limited to continuity checks for shorts between terminals. Integrated circuit checking is best done under dynamic conditions and using a module extender to make terminals readily accessible. Figure 4-12 illustrates the technique that is used for locating integrated circuits on a circuit card. Note that integrated circuits are numbered starting at the contact end of the board in the upper-right corner; the numbers increase toward the handle. When a row is completed, the next integrated circuit is located in the next row at the contact end of the board (Figure 4-12). The pins on each integrated circuit are located as shown in Figure 4-13.

4.8.3 Repairs and Replacements

NOTE

DEC recommends replacing defective modules with modules of known good quality on a one-for-one basis and returning the defective module to a DEC field office for subsequent repair and/or replacement. If however, for expediency, field repairs must be performed, it is imperative to take the following precautions.

When soldering semiconductor devices (transistors, diodes, or rectifiers, any of which may be damaged easily by heat, physical shock, or excessive electrical current), take the following special precautions:

a. Use a heat sink, such as a pair of pliers, to grip the lead of the component.

b. Use a 6V iron with an isolation transformer. Use the smallest iron adequate for the work. Use of an iron without an isolation transformer may result in excessive voltages present at the iron tip.

c. Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module-etched wiring.

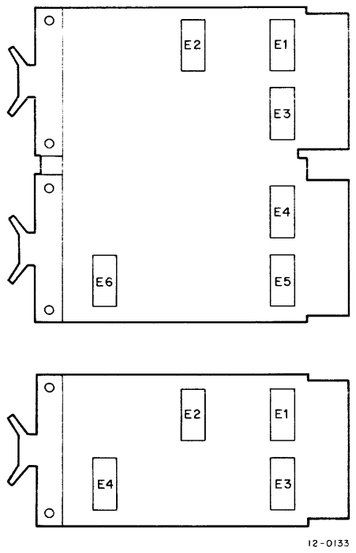


Figure 4-12 Integrated Circuit Location

d. Integrated circuits may be easily removed by using a solder puller to remove all excessive solder from contacts. Then, by straightening the leads, lift the integrated circuit from its terminal points. If it is not desirable to save the defective integrated circuit for test purposes, then the terminals may be cut at the body and each terminal removed from the board individually. Be sure to orient the new integrated circuit in the same position as the one removed.

CAUTION

Never attempt to remove solder from terminal points by heating and rapping modules against another surface. This practice usually results in module or component damage. Always remove solder with a solder-sucking tool.

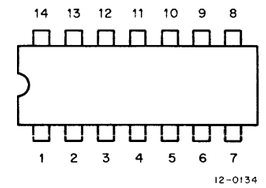


Figure 4-13 Integrated Circuit Pin Locations – Top View

When removing any part of the equipment for repair and replacement, ensure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components with parts of equal or better quality and tolerance.

In all soldering and unsoldering operations involving the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When the repair has been completed, remove all excess flux by washing junctions with a solvent such as trichlorethylene. Be very careful not to expose painted or plastic surfaces to this solvent.

4.8.4 Validation Tests

Always return repaired modules to the location from which they were taken. If a defective module is replaced by a new one during a repair period, tag the defective module, noting the location it was taken from and the nature of the failure. When repairs are complete, install the repaired module in its original location and determine whether or not the repairs have corrected the problem.

APPENDIX A
PDP-14 SIGNAL GLOSSARY

Signal	Module or Source	Source or Access Pin	Logic Reference	Description
AC 00–11 L	M745	AB18	D-BS-DA14-L-2 D-BS-DA14-I-2	Output Register of PDP-14 to accumulator (AC) of computer.
ADD 8 H ADD 4 H ADD 2 H ADD 1 H	M743	CD24CV2 CD24CT2 CD24CR2 CD24CN2	D-BS-PDP-14-0-5 (Sht 1)	Binary-weighted address lines for I, O, or A Box circuit selection. Derived from IR08–11.
BUS 00–11 L or BUS 00–11 H	M746	-------	D-BS-PDP-14-0-4	PDP-14 internal transfer bus. Bit 00 is MSB. This bus is on a wired-OR type that is ground-asserted for a logical 0.
CLEAR I/O	M743	CD24CJ2	D-BS-PDP-14-0-5 (Sht 2)	System reset signal for clearing all output addresses. Derived from an INITIALIZE input or from decoding of a CLR instruction.
CLR MB H	M742	AB22BF2	D-BS-PDP-14-0-3 (Sht 2)	CLEAR MEMORY BUFFER. This signal, derived from INITIALIZE or CLR 1 MB, resets the MB Register at the start of a memory access.
CLR PC1 H	M742	AB22BJ2	BS-PDP-14-0-3 (Sht 2)	CLEAR PROGRAM COUNTER 1. This signal, derived from INITIALIZE, resets PC1.
CLR 1 MB L	M741	AB23AB1	D-BS-PDP-14-0-3 (Sht 1)	CLEAR 1 MEMORY BUFFER. 100-ns pulse that is generated for each memory access. It is ORed with INITIALIZE to clear the MB Register.
CONTINUE	----	AB22AD2	D-BS-PDP-14-0-3 (Sht 2)	Ground level input from CONTINUE switch that starts the processor timing.
CONTROLS ENABLE L	M742	AB22AE2	D-BS-PDP-14-0-3 (Sht 2)	The RUN flip-flop controls this signal. With the RUN flip-flop reset (controller stopped), this signal is at ground level. It is provided to the START and CONTINUE controls to enable the respective function.
DECREMENT ENABLE L	M740	AB24AP1	D-BS-PDP-14-0-3 (Sht 1)	Decoder output signifying bits 4 and 5 of an instruction are a logical 0 and a logical 1, respectively. The DECREMENT ENABLE signal can decrement PC1 or the Spare Register.
(EEM + LEM) H	M740	AB24AK1	D-BS-PDP-14-0-3 (Sht 1)	Decoder output denoting an Enter External Mode (EEM) or Leave External Mode (LEM) instruction is in the IR.
END CYCLE L or END CYCLE H	M741	AB23AF1	D-BS-PDP-14-0-3 (Sht 1)	100-ns negative pulse derived from T pulses. Pulse is generated at the end of TS2 if a I/O cycle is not in progress. For an I/O cycle, this pulse occurs concurrently with the I/O STROBE pulse trailing edge.
EN MEM 01 H 02 H 03 H 04 H	M742	AB22BT2 AB22BV2 AB22BU2 AB22AS1	D-BS-PDP-14-0-3 (Sht 2)	ENABLE MEMORY. Decoded PC1 00 and 01 counts denoting the memory bank selected for the current instruction; EN MEM 01 selects the first 1K of memory, 02 the second 1K, etc.
EN LOOP H	G923	DC2	D-BS-PDP-14-0-3	Enable Loop. When G923 module is removed from the ROM, this signal enables a controller timing test loop that bypasses ROM timing. With G923 module installed, this signal is a ground level and inhibits the timing loop.
ERSET 0 H	M743	CD24CF2	D-BS-PDP-14-0-5 (Sht 2)	Enable reset signal for the following Output Boxes and addresses:

Box	Address (Octal)	Box	Address (Octal)
A	0–17	J	200–217
C	40–57	L	240–257
E	100–117	N	300–317
G	140–157	R	340–357

Signal	Module or Source	Source or Access Pin	Logic Reference	Description
ERSET 1 H	M743	CD24CE2	D-BS-PDP-14-0-5 (Sht 2)	Enable reset signal for the following Output Boxes and addresses: **Box Address (Octal) Box Address (Octal)** B 20–37 K 220–237 D 60–77 M 260–277 F 120–137 P 320–337 H 160–177 S 360–376
E SET 0 H	M743	CD24CH2	D-BS-PDP-14-0-5 (Sht 2)	Enable set signal for the following Output Boxes and addresses: **Box Address (Octal) Box Address (Octal)** A 0–17 J 200–217 C 40–57 L 240–257 E 100–117 N 300–317 G 140–157 R 340–357
E SET 1 H	M743	CD24CC1	D-BS-PDP-14-0-5 (Sht 2)	Enable set signal for the following Output Boxes and addresses: **Box Address (Octal) Box Address (Octal)** B 20–37 K 220–237 D 60–77 M 260–277 F 120–137 P 320–337 H 160–177 S 360–376
EXECUTE (1) H FETCH (0) H	M741	AB23AE1 AB23BP2	D-BS-PDP-14-0-3 (Sht 1)	Output of FETCH/EXECUTE flip-flop denoting current cycle.
EXT DONE L	M745	AB18BF1	D-BS-DA14-L-2 D-BS-DA14-I-2	Pulse denoting the current IOT instruction is complete. Derived from a LDE (6164_8) or GNI (6165_8) when in the external mode or from a 100-ns EXT GO pulse for a single interrupt instruction.
EXT FLAG (1) L	M745	AB18BH2	D-BS-DA14-L-2 D-BS-DA14-I-2	Flip-flop output denoting a GNI instruction has been completed.
EXT GO H	M741	AB23AD1	D-BS-PDP-14-0-3 (Sht 1)	EXTERNAL GO. 100-ns positive pulse generated for interrupt or external mode operation. This pulse is comparable to MEM GO for ROM usage.
(EXT MODE ⊕ INT) L	M745	AB18BJ2	D-BS-DA14-L-2 D-BS-DA14-I-2	EXCLUSIVE OR of external mode with Interrupt Sync. Signal denotes the external mode has been selected or that a Generate Interrupt instruction is being executed.
EXT MODE (1) H	M745	AB18BN1	D-BS-DA14-L-2 D-BS-DA14-I-2	Flip-flop output denoting the external computer is providing controller instruction. Flip-flop is set by an Enter External Mode (EEM) instruction (0600_8) and is reset by a Leave External Mode (LEM) instruction (0400_8) or an initialize operation.
EXT PC1 CLEAR L				Not used.
FETCH (1) H EXECUTE (0) H or EXECUTE (0) L	M741	AB23AJ1 AB23AH1	D-BS-PDP-14-0-3 (Sht 1)	Output of FETCH/EXECUTE flip-flop denoting the current cycle.
HALT L	M740	AB24BP2	D-BS-PDP-14-0-3 (Sht 1)	100-ns positive pulse denoting IR contains a HALT instruction (0007_8). This pulse sets the STOP flip-flop to terminate operation at the end of the current cycle.
INCREMENT ENABLE H	M740	AB24AN1	D-BS-PDP-14-0-3 (Sht 1)	Decoder output signifying that bits 4 and 5 of an instruction are both logical 1s. The INCREMENT ENABLE signal can increment PC1 or the Spare Register.
INITIALIZE H INITIALIZE L	M742	AB22BH1 AB22BK2	D-BS-PDP-14-0-3 (Sht 2)	System reset lines; active during power up, power down, or whenever a timing failure is detected.
IN0 H	M743	CD24DP1	D-BS-PDP-14-0-5 (Sht 1)	This signal denotes the state of the input or output being tested. Bit 01 of a TXD or TYD output word is derived from this signal. IN0 H is positive-asserted if the input or output is off.
INT RQST BUS L	M745	AB18AM2	D-BS-DA14-L-2 D-BS-DA14-I-2	Computer INTERRUPT REQUEST bus from peripheral devices.
INT SYNC (0) H	M745	AB18BL2	D-BS-DA14-L-2 D-BS-DA14-I-2	Output of INT SYNC flip-flop that prevents the incrementing of PC1 if an interrupt operation is in process (controller is performing a GNI).
I/O CYCLE (1) H	M741	AB23BU2	D-BS-PDP-14-0-3	Output of I/O CYCLE flip-flop denoting an I/O instruction is being executed (15–18 μs).
I/O DONE H	M741	AB23BS2		Not used.
I/O STROBE L	M741	AB23BR1	D-BS-PDP-14-0-3 (Sht 1)	6.5-μs negative pulse that strobes SYN and SYF levels to set an output on or off.

Signal	Module or Source	Source or Access Pin	Logic Reference	Description
IRE L or IR ENABLE L	M742	AB22BE1	D-BS-PDP-14-0-3 C-CS-M742-0-1	INSTRUCTION REGISTER ENABLE. A Test and Display instruction (TXD or TYD) generates this signal. IRE in turn, generates the SOR-INPUT gating strobe to transfer the IR contents to BUS 00–11 for transfer to the Output Register. BUS 00–02 is ORed with output of M742. (See TXD or TYD output format.)
IR SYNC (1) H	M741	-------	D-BS-PDP-14-0-3 (Sht 1)	Not used.
IR 00–11 (1) H	M746	CD23	D-BS-PDP-14-0-4	Instruction Register bits 0 through 11.
(JFN + JFF) L	M740	AB24AH1	D-BS-PDP-14-0-3 (Sht 1)	Decoder output signifying a Jump If On (JFN) or Off (JFF) instruction is in the IR (5000_8).
JF-OK (1) H JF-OK (0) H	M741	AB23AV2 AB23AU2	D-BS-PDP-14-0-3	Flip-flop output denoting a jump is required. When set, causes a program jump to the location specified by IR 04–11; i.e., it causes IR 04–11 to be loaded into PC1 to address the next memory access.
(JMP + JMS) H	M740	AB24AM2	D-BS-PDP-14-0-3 (Sht 1)	Decoder output signifying an unconditional Jump (JMP) or a conditional Jump to Subroutine (JMS) instruction (4000_8) is active.
K OUT ENABLE H	M742	AB22BP1	D-BS-PDP-14-0-5	Set and reset signal to M743.
LD EQ 1 H LD EQ 2 H LD EQ 3 H LD EQ 4 H	G782	A32AE2 A32AH2 D32DH2 D32DE2	D-BS-PDP-14-0-5	LOAD EQUALIZER – These lines provide filter time constant equalization for I, O, or A Boxes as G782 modules on BC14A cables are added or deleted.
LD INPUT L	M745	AB18BP1	D-BS-DA14-L-2 D-BS-DA14-I-2	Load Input Register pulse.
LD-IR L	M740	AB24BL1	D-BS-PDP-14-0-3 (Sht 1)	Destination register load strobe for IR (trailing edge jam-transfer).
LD-MB L	M740	AB24BJ1	D-BS-PDP-14-0-3 (Sht 1)	Destination register load strobe for Memory Buffer Register (trailing edge jam-transfer).
LD-OUT L	M740	AB24BV1	D-BS-PDP-14-0-3 (Sht 1)	Destination register load strobe for Output Register (trailing edge jam-transfer).
LD-PC1 L	M740	AB24BN2	D-BS-PDP-14-0-3 (Sht 1)	Destination register load strobe for PC1 (trailing edge jam-transfer).
LD-PC2 L	M740	AB24BP1	D-BS-PDP-14-0-3 (Sht 1)	Destination register load strobe from PC2 (trailing edge jam-transfer).
LD-SPARE L	M740	AB24BM1	D-BS-PDP-14-0-3 (Sht 1)	Destination register load strobe for Spare Register (trailing edge jam-transfer).
MEM DONE H	M741	AB23AB2	D-BS-PDP-14-0-3 (Sht 1)	MEMORY DONE H. 100-ns positive pulse denoting the ROM or computer has completed an instruction retrieval. Pulse is derived from the trailing edge of a ROM MEM DONE or EXT DONE input during normal operation. MEM DONE loads IR and initiates TS1. MEM DONE can be generated from a MEM GO when the G923 module is removed from the ROM. This feature bypasses ROM timing.
MEM DONE L	G924	BL1	D-BS-PDP-14-0-3 (Sht 1)	MEMORY DONE L. 150-ns negative pulse signifying the ROM has retrieved an instruction and the instruction is available in the MB Register.
MEM GO H	M741	AB23AN1	D-BS-PDP-14-0-3 (Sht 1)	MEMORY GO. Nominal 100-ns positive pulse that starts a ROM cycle for instruction access. The ROM responds with a MEM DONE pulse when the memory cycle is complete.
DUT ENABLE L	M742	AB22BJ1	D-BS-PDP-14-0-3 (Sht 2)	OUTPUT ENABLE. This line enables the Output Register to be loaded through the generation of an LD-OUT L pulse during TXD + TYD.
OUTPUT FLAG (1) L	M745	AB18BH1	D-BS-DA14-L-2 D-BS-DA14-I-2	Denotes the PDP-14 has information in the Output Register for transfer to the computer.
PAUSE (1) H	M741	AB23BT2	D-BS-PDP-14-0-3 (Sht 1)	A nominal 650-ns pulse that denotes a ROM access is in progress. The leading edge of PAUSE initiates a MEM GO to begin an access. Pause is terminated by the trailing edge of MEM DONE.
PC1 CARRY	M747	D19A1	D-BS-PDP-14-0-4 (Sht 2)	Carry output from low-order PC1 stages (06–11) to next stage (05) of PC1.
PC1 00–11 (1) H	M747	CD19	D-BS-PDP-14-0-4	Output of Program Counter 1 (PC1). Bit 00 is MSB.
PC2 00–11 (1) H	M746	CD21	D-BS-PDP-14-0-2	Output of Program Counter 2 (PC2). Bit 00 is MSB.
POWER SENSE	+5V Supply	AB22AA1	D-BS-PDP-14-0-3 (Sht 2)	+5V input for sensing a power-up condition.

Signal	Module or Source	Source or Access Pin	Logic Reference	Description
PS1 H 2 H 3H 4 H 5 H 6 H 7 H 8 H	M743	CD24DA1 DJ2 DL2 DN2 DR2 DV2 DU2 DT2	D-BS-PDP-14-0-5	Package select lines for I, O, and A Boxes and BF14-M Storage Modules. PS1 selects a system address of $0–37_8$, PS2 selects $40–77_8$, etc.
RUN (1) H	M742	AB22AH2	D-BS-PDP-14-0-3 (Sht 2)	Output of RUN flip-flop signifying the controller is operating; i.e., it is not in a power-down or an initialize state.
SHUT DOWN L	M742	AB22BU1	D-PDP-14-0-3 (Sht 2)	This signal generates INITIALIZE during a power-up or power-down sequence.
(SKE + SKZ) H	M740	AB24AN2	D-BS-PDP-14-0-3 (Sht 1)	Decoder output signifying a Skip If Equal (SKE) or Skip If Zero (SKZ) instruction is in the IR. Diagnostic instruction.
SKE L or SKE ENABLE L	M740	AB24AJ1	D-BS-PDP-14-0-3 (Sht 1) D-CS-M740-0-1	Decoder output denoting a Skip If Equal (SKE) instruction is in the IR. Output strobes the comparison between PC2 and a source register. Diagnostic instruction.
SKIP BUS L	M745	AB18AK2	D-BS-DA14-L-2 D-BS-DA14-I-2	When low, causes the computer to skip a location.
SKIP-OK (1) H SKIP-OK (0) H	M741	AB23AH2 AB23AJ2	D-BS-PDP-14-0-3 (Sht 1)	SKIP flip-flop output that causes the next memory location to be skipped. Flip-flop is set if source register contents equals PC2 for an SKE instruction or if source register contents equals 0 for an SKZ instruction.
SOR INPUT H	M740	AB24AV1	D-BS-PDP-14-0-3 (Sht 1)	Source register gating signal that transfers contents of Input Register to BUS 00–11.
SOR-IR H	M740	AB24BD1	D-BS-PDP-14-0-3 (Sht 1)	Source register gating signal that transfers the IR contents to BUS 00–11.
SOR-MB (0–3) H SOR-MB (4–11) H	M740 M740	AB24AS2 AB24AT2	D-BS-PDP-14-0-3 (Sht 1)	Source register gating signals that transfer the contents of the Memory Buffer to BUS 00–11.
SOR-PC1 (0–3) H SOR-PC1 (4–11) H	M740 M740	AB24AU2 AB24AV2	D-BS-PDP-14-0-3 (Sht 1)	Source register gating signals that transfer PC1 contents to BUS 00–11.
SOR-PC2 H	M740	AB24AU1	D-BS-PDP-14-0-3 (Sht 1)	Source register gating signal that transfers the contents of PC2 to BUS 00–11.
SOR-SPARE H	M740	AB24BC1	D-BS-PDP-14-0-3 (Sht 1)	Source register gating signal that transfers the contents of the spare register to BUS 00–11.

Signal	Module or Source	Source or Access Pin	Logic Reference	Description
START CYCLE H	M741	AB23AT2	D-BS-PDP-14-0-3 (Sht 1)	200-ns positive pulse that starts processor timing; this pulse is generated 150 ns after an initialize operation or following the trailing edge of an END CYCLE pulse.
START EXT L	M742	AB22AJ2	D-BS-PDP-14-0-3 (Sht 2)	200-ns pulse generated at the end of an initialize condition to clear the STOP flip-flop, set the RUN flip-flop and begin processor timing.
START L	M742	AB22AM2	D-BS-PDP-14-0-3 (Sht 2)	Ground level input from START switch that begins controller operation. This signal initializes the controller, then starts processor timing.
SWITCH ON L	M742	AB22AN2	D-BS-PDP-14-0-3 (Sht 2)	This signal is generated for a power-up sequence, manual START and CONTINUE. For a power-up sequence or CONTINUE, this signal only triggers the START EXT pulses to begin a processor cycle. For a START operation, the signal causes an INITIALIZE pulse and then starts processor timing.
(SYN + SYF) L	M740	AB24AC1	D-BS-PDP-14-0-3 (Sht 1)	Decoder output denoting a Set Output On (SYN) or Off (SYF) instruction is in the IR (3000_8).
T ENABLE L	M742	AB22BH2	D-BS-PDP-14-0-3 (Sht 2)	Not used.
TEST FLOP (1) H TEST FLOP (0) H	M741	AB23BD2 AB23BE2	D-BS-PDP-14-0-3 (Sht 1)	TEST FLOP. Output denoting the result of the last input or output test. Flip-flop is set if condition tested for is true (e.g., for TXN with input on, TXF with input off, etc.). Flip-flop is reset by JFN and JFF instructions.
TEST TRUE H	M743	CD24DN1	D-BS-PDP-14-0-5 (Sht 1)	Denotes the input or output tested was in the state (on or off) defined by the test instruction (TXN, TXF, TYN or TYF). This signal, when asserted, sets the TEST FLOP in the M741 module.
T PULSE H	M741	AB23BH1	D-BS-PDP-14-0-3 (Sht 1)	100-ns positive pulse generated at the end of TS1, TS2 and an I/O cycle.
[TS1 (1) · EXECUTE (1)] H	M741	AB23AL2	D-BS-DA14-L-2 D-BS-DA14-I-2	500-ns pulse derived from TS1 and EXECUTE states.
TS1 (1) H	M741	AB23BM2	D-BS-PDP-14-0-3 (Sht 1)	500-ns pulse that is active for the first time state (TS1) in a cycle.

Signal	Module or Source	Source or Access Pin	Logic Reference	Description
TS2 (1) H	M741	AB23BL2	D-BS-PDP-14-0-3 (Sht 1)	500-ns pulse that is active for the second time state (TS2) of a cycle.
TXD L	M740	AB24AK2	D-BS-PDP-14-0-3 (Sht 1)	Decoder output signifying a Test Input and Display instruction is in the IR (7000_8).
(TXD + TYD) L	M740	AB24AF2	D-BS-PDP-14-0-3 (Sht 1)	Decoder output denoting a Test Input and Display (TXD) or Test Output and Display (TYD) instruction is in the IR (7000_8).
(TXN + TXF + TYN + TYF + SYN + SYF + TXD + TYD) H	M740	AB24AA1	D-BS-PDP-14-0-3 (Sht 1)	Decoder output denoting an I/O instruction is in the IR.
(TXN + TXF) L	M740	AB24AB1	D-BS-PDP-14-0-3 (Sht 1)	Decoder output denoting a Test Input for On (TXN) or Off (TXF) instruction is in the IR (2000_8).
TYD L	M740	AB24AL2	D-BS-PDP-14-0-3 (Sht 1)	Decoder output signifying a Test Output and Display (TYD) instruction is in the IR (7400_8).
(TYN + TYN) L	M740	AB24AE1	D-BS-PDP-14-0-3 (Sht 1)	Decoder output denoting a Test Output for On (TYN) or Off (TYF) instruction is in the IR (1000_8).
XSRET 0 H	I Box	CD24CD2	D-BS-PDP-14-0-5 (Sht 1)	Signal return line for the following Input Boxes and addresses: **Box Address (Octal) Box Address (Octal)** A 0–17 F 200–217 B 40–57 F 240–257 C 100–117 G 300–317 D 140–157 H 340–357
XSRET 1 H	I Box	CD24DD2	D-BS-PDP-14-0-5 (Sht 1)	Signal return line for the following Input Boxes and addresses: **Box Address (Octal) Box Address (Octal)** A 20–37 E 220–237 B 60–77 F 260–277 C 120–137 G 320–337 D 160–177 H 360–377
YSRET 0 H	O Box	CD24CB2	D-BS-PDP-14-0-5 (Sht 1)	Signal return line for the following Output Boxes and addresses: **Box Address (Octal) Box Address (Octal)** A 0–17 J 200–217 C 40–57 L 240–257 E 100–117 N 300–317 G 140–157 R 340–357
YSRET 1 H	O Box	CD24DB2	D-BS-PDP-14-0-5 (Sht 1)	Signal return line for the following Output Boxes and system addresses: **Box Address (Octal) Box Address (Octal)** B 20–37 K 220–237 D 60–77 M 260–277 F 120–137 P 320–337 H 160–177 S 360–376

APPENDIX B
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Registers	D-BS-DA14-L-3	B-24, B-25
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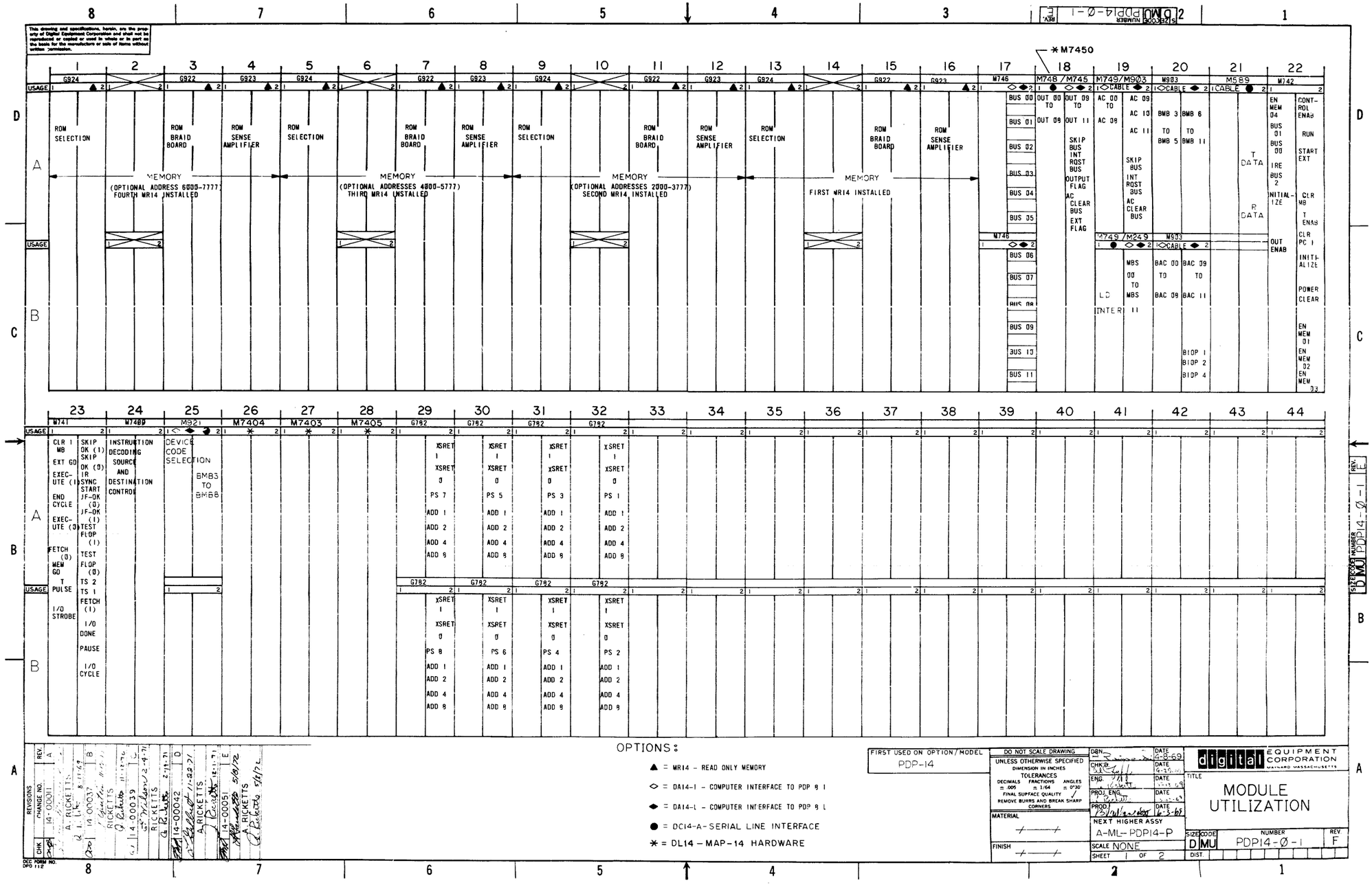
714	Power Supply	B-83
Power Supply Filter Circuit (D-CS-7006314-0-1)		B-84



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*M7450
ROM SELECTION
ROM BRAID BOARD
ROM SENSE AMPLIFIER
MEMORY (OPTIONAL ADDRESS 6000-7777) FOURTH MR14 INSTALLED
MEMORY (OPTIONAL ADDRESSES 4000-5777) THIRD MR14 INSTALLED
MEMORY (OPTIONAL ADDRESSES 2000-3777) SECOND MR14 INSTALLED
MEMORY FIRST MR14 INSTALLED
USAGE
M746
M748/M745
M749/M903
M903
M589
M742
M741
M7400
M921
M7404
M7403
M7405
G782
DEVICE CODE SELECTION
BMB3 TO BMB8
INSTRUCTION DECODING SOURCE AND DESTINATION CONTROL
OPTIONS:
▲ = MR14 - READ ONLY MEMORY
◇ = DA14-I - COMPUTER INTERFACE TO PDP 8 I
◆ = DA14-L - COMPUTER INTERFACE TO PDP 8 L
● = DC14-A-SERIAL LINE INTERFACE
✱ = DL14 - MAP-14 HARDWARE
FIRST USED ON OPTION/MODEL
PDP-14
DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE 4-8-69
NEXT HIGHER ASSY
A-ML-PDP14-P
SCALE NONE
SHEET 1 OF 2
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
MODULE UTILIZATION
SIZE D
CODE MU
NUMBER PDP14-Ø-1
REV. F
DIST.
REVISIONS
CHANGE NO.
14-00011
14-00037
14-00039
14-00042
14-00051
A. RICKETTS
DEC FORM NO. DPD 112

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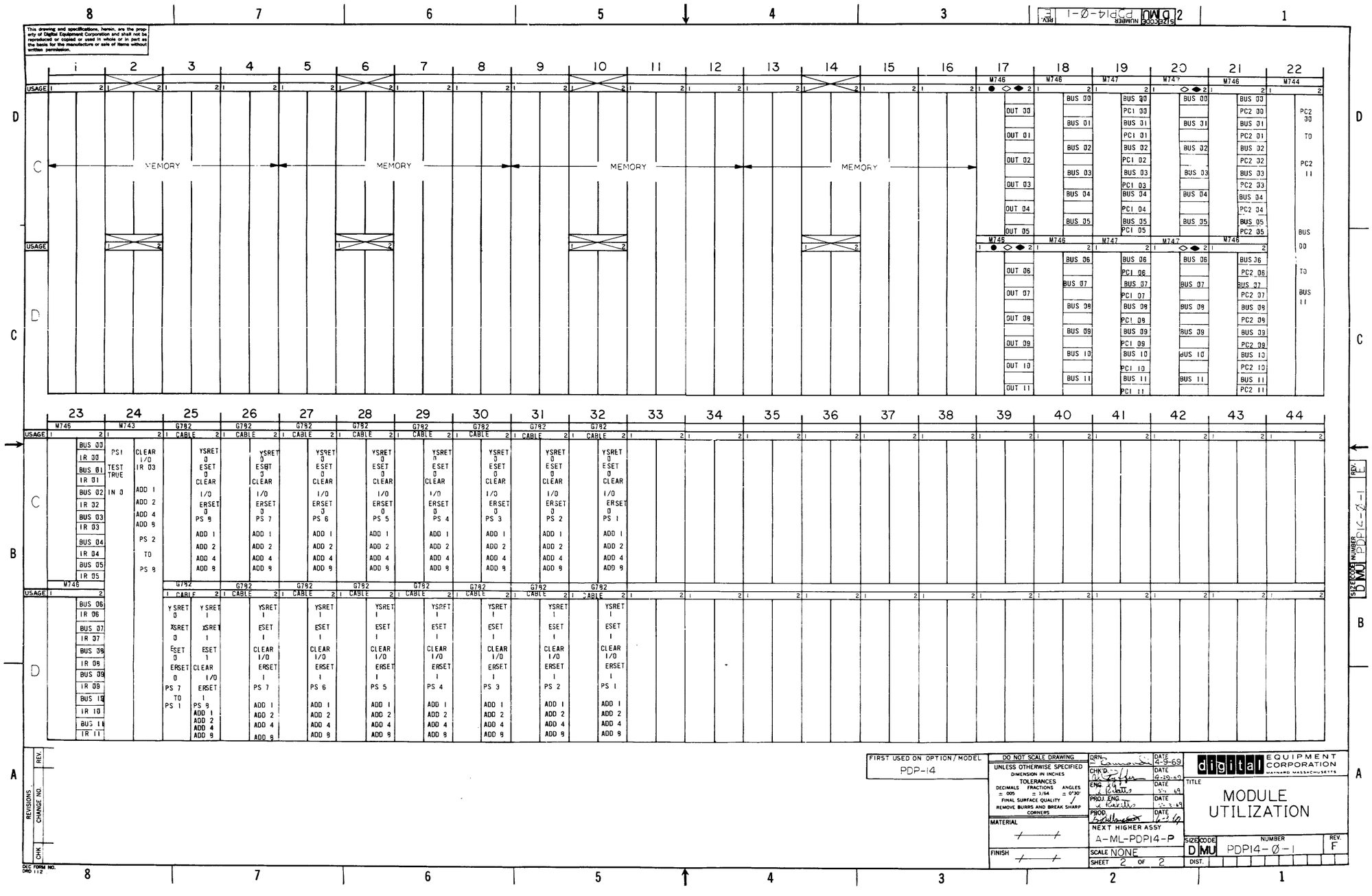

FIRST USED ON OPTION/MODEL	PDP-14
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'. FINAL SURFACE QUALITY. REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL	—
FINISH	—
DRN.	[illegible] DATE 4-9-69
CHK'D	[illegible] DATE 4-10-69
ENG	[illegible] DATE 5-1-69
PROJ. ENG	[illegible] DATE 5-2-69
PROD.	[illegible] DATE 6-3-69
NEXT HIGHER ASSY	A-ML-PDP14-P
SCALE	NONE
SHEET	2 OF 2
TITLE	MODULE UTILIZATION
SIZE	D
CODE	MU
NUMBER	PDP14-Ø-1
REV.	F
DIST.	
REVISIONS	REV. / CHANGE NO. / CHK
DEC FORM NO.	DRD 112

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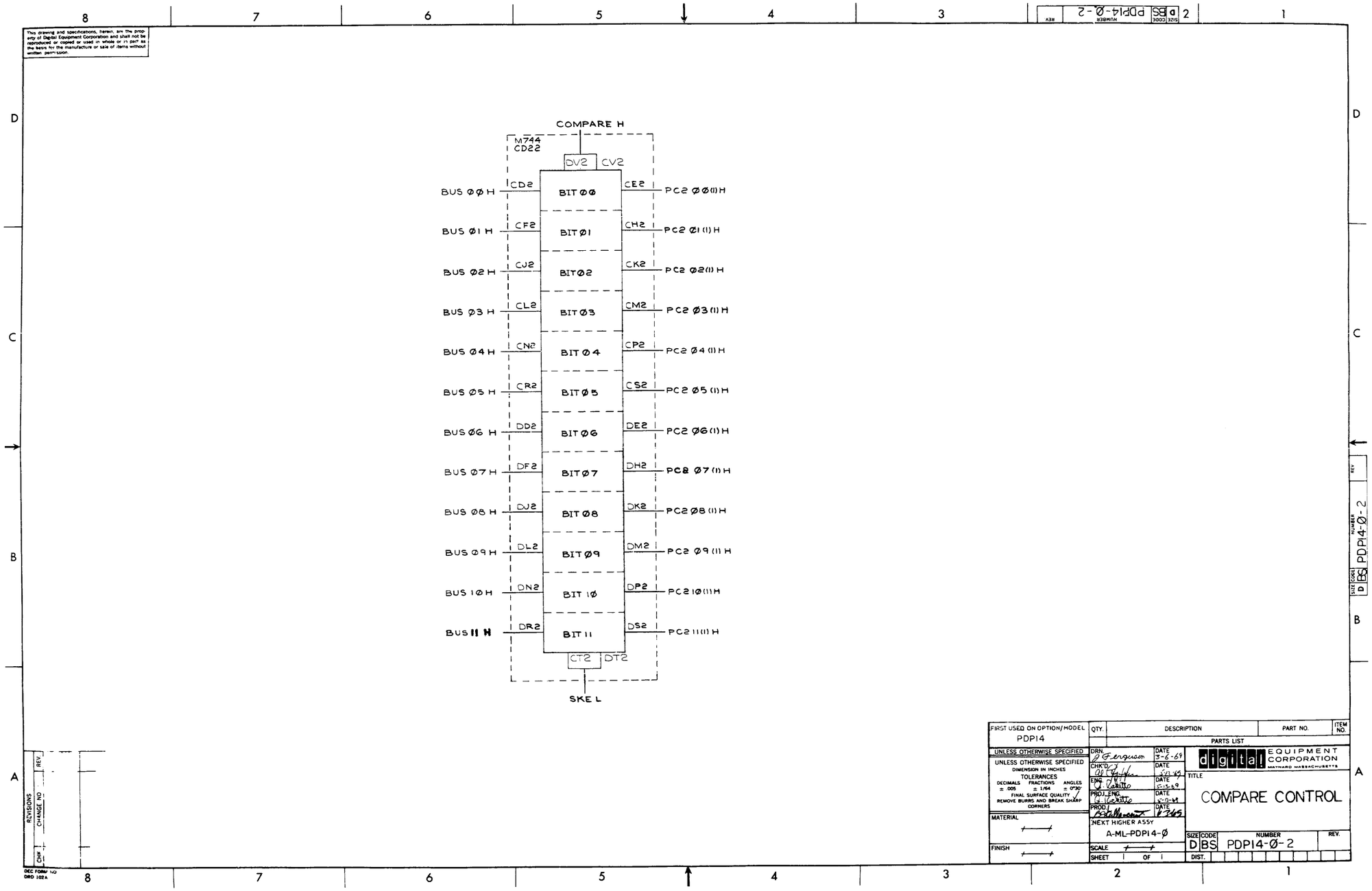

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FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP14		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN.	J. Ferguson	DATE 3-6-69
CHK'D	[illegible]	DATE 5-12-69
ENG.	[illegible]	DATE 5-13-69
PROJ. ENG.	[illegible]	DATE 5-13-69
PROD.	[illegible]	DATE 6-3-69

NEXT HIGHER ASSY
A-ML-PDP14-Ø

SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

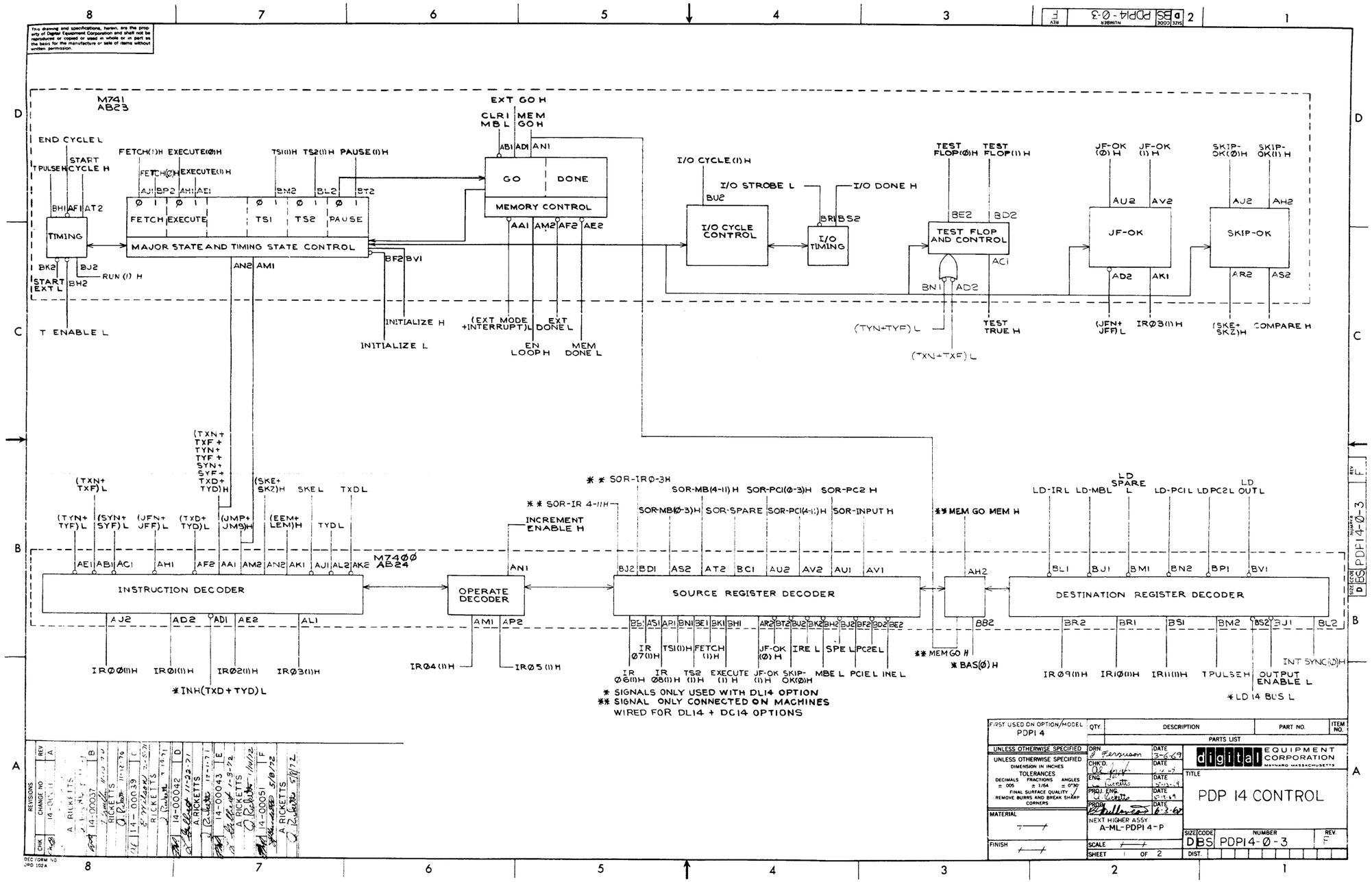
TITLE
COMPARE CONTROL

SIZE	CODE	NUMBER	REV.
D	BS	PDP14-Ø-2	

DIST.

REVISIONS
REV. | CHANGE NO | CHK

DEC FORM NO
DRD 102A


M741
AB23
END CYCLE L
START CYCLE H
TPULSE H
TIMING
START EXT L
RUN (1) H
T ENABLE L
FETCH(1)H EXECUTE(Ø)H
FETCH(Ø)H EXECUTE(1)H
TS1(1)H TS2(1)H PAUSE(1)H
FETCH EXECUTE TS1 TS2 PAUSE
MAJOR STATE AND TIMING STATE CONTROL
INITIALIZE H
INITIALIZE L
EXT GO H
CLR1 MB L
MEM GO H
GO
DONE
MEMORY CONTROL
(EXT MODE +INTERRUPT)L
EXT DONE L
EN LOOP H
MEM DONE L
I/O CYCLE(1)H
I/O STROBE L
I/O DONE H
I/O CYCLE CONTROL
I/O TIMING
TEST FLOP(Ø)H
TEST FLOP(1)H
TEST FLOP AND CONTROL
(TYN+TYF) L
(TXN+TXF) L
TEST TRUE H
JF-OK (Ø) H
JF-OK (1) H
JF-OK
(JFN+ JFF) L
IRØ3(1)H
SKIP-OK(Ø)H
SKIP-OK(1) H
SKIP-OK
(SKE+ SKZ)H
COMPARE H
(TXN+ TXF+ TYN+ TYF+ SYN+ SYF+ TXD+ TYD)H
(TXN+ TXF) L
(TYN+ TYF) L
(SYN+ SYF) L
(JFN+ JFF) L
(TXD+ TYD) L
(JMP+ JMS)H
(SKE+ SKZ)H
SKE L
TXD L
(EEM+ LEM)H
TYD L
M7400
AB24
INSTRUCTION DECODER
OPERATE DECODER
SOURCE REGISTER DECODER
DESTINATION REGISTER DECODER
INCREMENT ENABLE H
** SOR-IR 4-11H
** SOR-IRØ-3H
SOR-MB(Ø-3)H
SOR-MB(4-11) H
SOR-SPARE
SOR-PC1(Ø-3)H
SOR-PC1(4-11)H
SOR-PC2 H
SOR-INPUT H
** MEM GO MEM H
LD-IR L
LD-MB L
LD SPARE L
LD-PC1 L
LD PC2 L
LD OUT L
IRØØ(1)H
IRØ1(1)H
IRØ2(1)H
IRØ3(1)H
*INH(TXD+TYD)L
IRØ4(1)H
IRØ5(1)H
IR Ø7(1)H
IR Ø6(1)H
IR Ø8(1)H
TS1(1)H
TS2 (1)H
FETCH (1)H
EXECUTE (1) H
JF-OK (Ø) H
JF-OK (1) H
SKIP-OK(Ø)H
IRE L
MBE L
SPE L
PC2E L
PC1E L
INE L
** MEM GO H
* BAS(Ø) H
IRØ9(1)H
IRIØ(1)H
IR11(1)H
TPULSE H
OUTPUT ENABLE L
INT SYNC(Ø)H
*LD 14 BUS L
* SIGNALS ONLY USED WITH DL14 OPTION
** SIGNAL ONLY CONNECTED ON MACHINES WIRED FOR DL14 + DC14 OPTIONS
FIRST USED ON OPTION/MODEL PDP14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN. J. Ferguson DATE 3-6-69
CHK'D. DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 6-3-69
NEXT HIGHER ASSY A-ML-PDP14-P
SCALE
SHEET 1 OF 2
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE PDP 14 CONTROL
SIZE D CODE BS NUMBER PDP14-Ø-3 REV. F
DIST.
REVISIONS
CHANGE NO
REV
CHK
A RICKETTS
14-00037 B
14-00039 C
14-00042 D
14-00043 E
14-00051 F
DEC FORM NO DRD 102A

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PCI ØØ (1)H BL1
PCI Ø1 (1)H BM1
MEMORY BANK SELECTOR
BT2 EN MEM Ø1 H
BV2 EN MEM Ø2 H
BU2 EN MEM Ø3 H
AS1 EN MEM Ø4 H

+5V (POWER SENSE) AA1
POWER TURN ON DETECTOR

EXT MODE (1) H
AL2
INITIALIZE
BK2 INITIALIZE L
BH1 INITIALIZE H

EXT PCI CLEAR L
BL2
BJ2 CLR PCI H
AB1
BF2 CLR MB H
CLR1 MB L

START EXT L
PA
AJ2

RUN (1) H
AH2
RUN
AE1
AF1
BD
AE2
ADI HALT L

START
CONTINUE
STOP
AM2
AD2
SCHMITT TRIGGER
AN2 SWITCH ON L

END CYCLE H

CONTROLS ENABLE L

EXECUTE (Ø) L AH1
(TXD+TYD) L AF2
I/O DONE H BS2
TXD+TYD TO OUTPUT REGISTER CONTROL
BE1 IRE L
BH2 T ENABLE L
BJ1 OUT ENABLE L

TEST FLOP (Ø) H BE2
BC1 BUS ØØ L
INØ H BA1
BB1 BUS Ø1 L
+5V BC1
BF1 BUS Ø2 L

POWER FAIL DETECTOR
BR2 SHUT DOWN H
BU1
BN1 +3

M742
AB22

REVISIONS	CHANGE NO.	CHK
REV		

DEC FORM NO ORD 102 A

FIRST USED ON OPTION MODEL PDP14
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

QTY.	DESCRIPTION	PART NO	ITEM NO.

PARTS LIST

DRN. [signature] DATE 4-8-69
CHK'D. [signature] DATE 4-11-69
ENG. [signature] DATE 4-13-69
PROJ. ENG. [signature] DATE 4-11-69
PROD. [signature] DATE 4-11-69
NEXT HIGHER ASS'Y A-ML-PDP14-P
SCALE NONE
SHEET 2 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE PDP14 CONTROL

SIZE D | CODE BS | NUMBER PDP14-Ø-3 | REV. F
DIST.

SIZE D | CODE BS | NUMBER PDP14-Ø-3 | REV F

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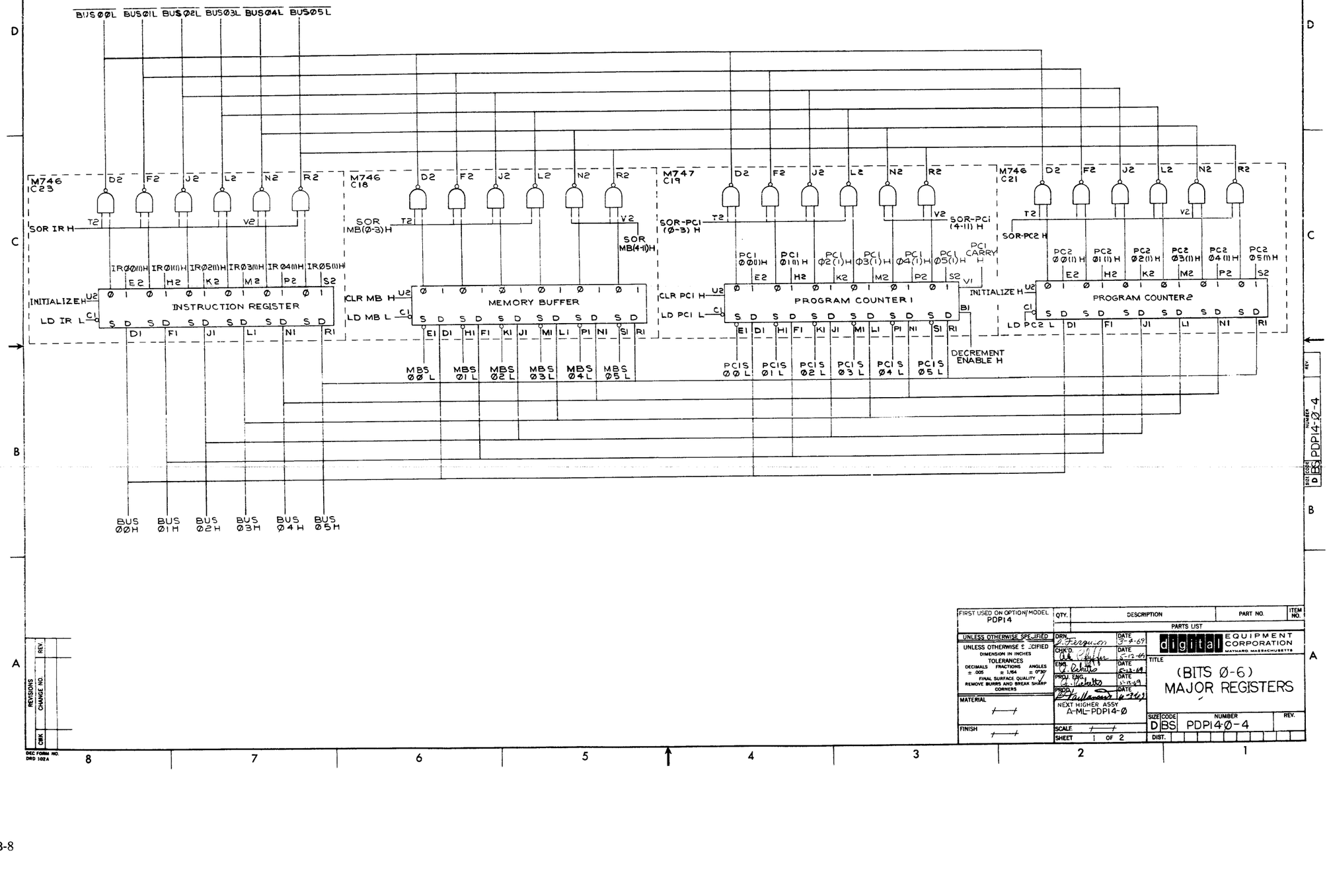


FIRST USED ON OPTION/MODEL: PDP14	QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN	D. Ferguson	DATE 5-8-69
CHK'D	[illegible]	DATE 5-12-69
ENG.	[illegible]	DATE 5-12-69
PROJ. ENG.	[illegible]	DATE 5-12-69
PROD.	[illegible]	DATE 10-24-69

NEXT HIGHER ASSY A-ML-PDP14-Ø

SCALE —

SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE (BITS Ø-6) MAJOR REGISTERS

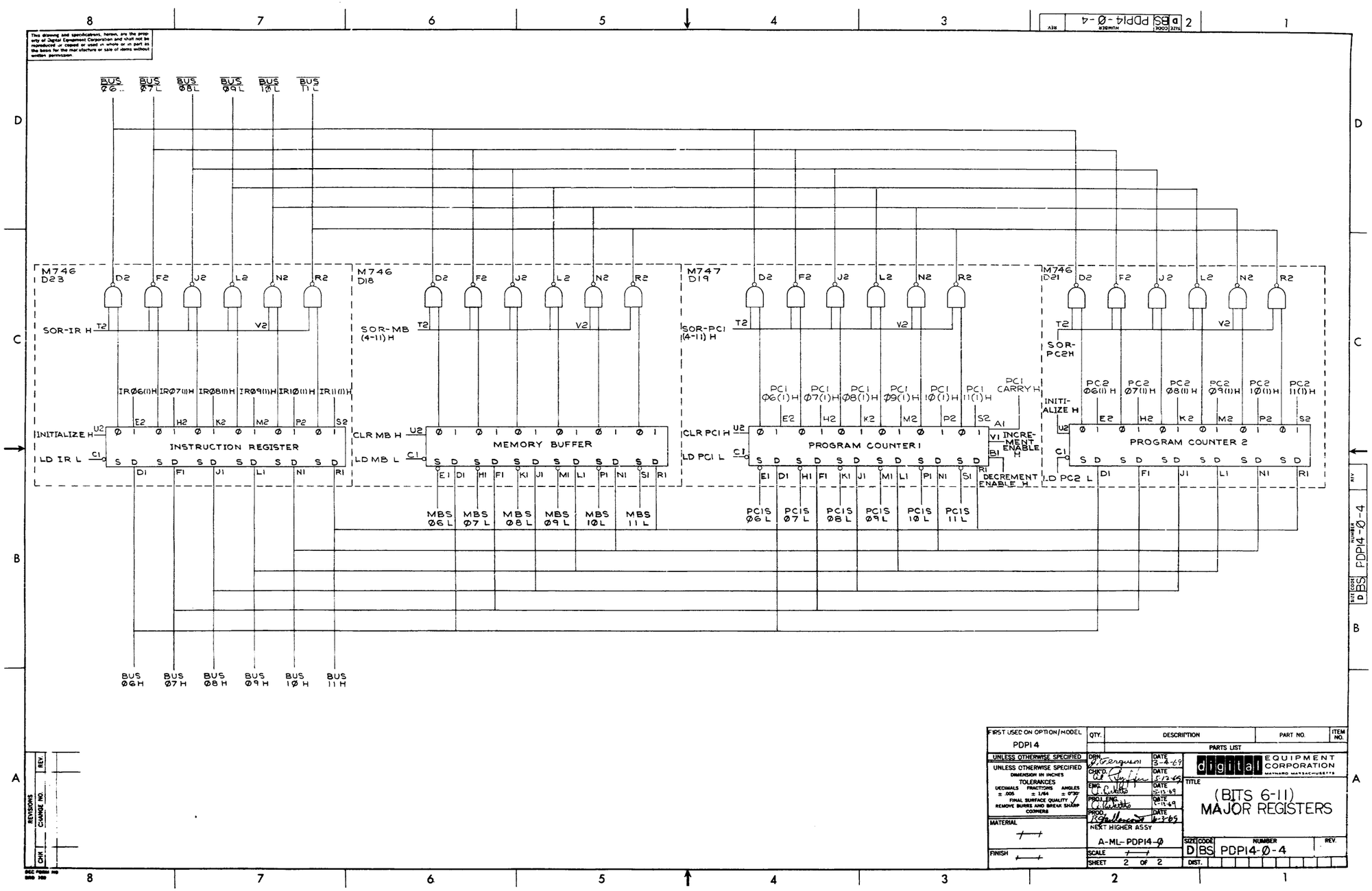
SIZE	CODE	NUMBER	REV.
D	BS	PDP14Ø-4	

DIST.

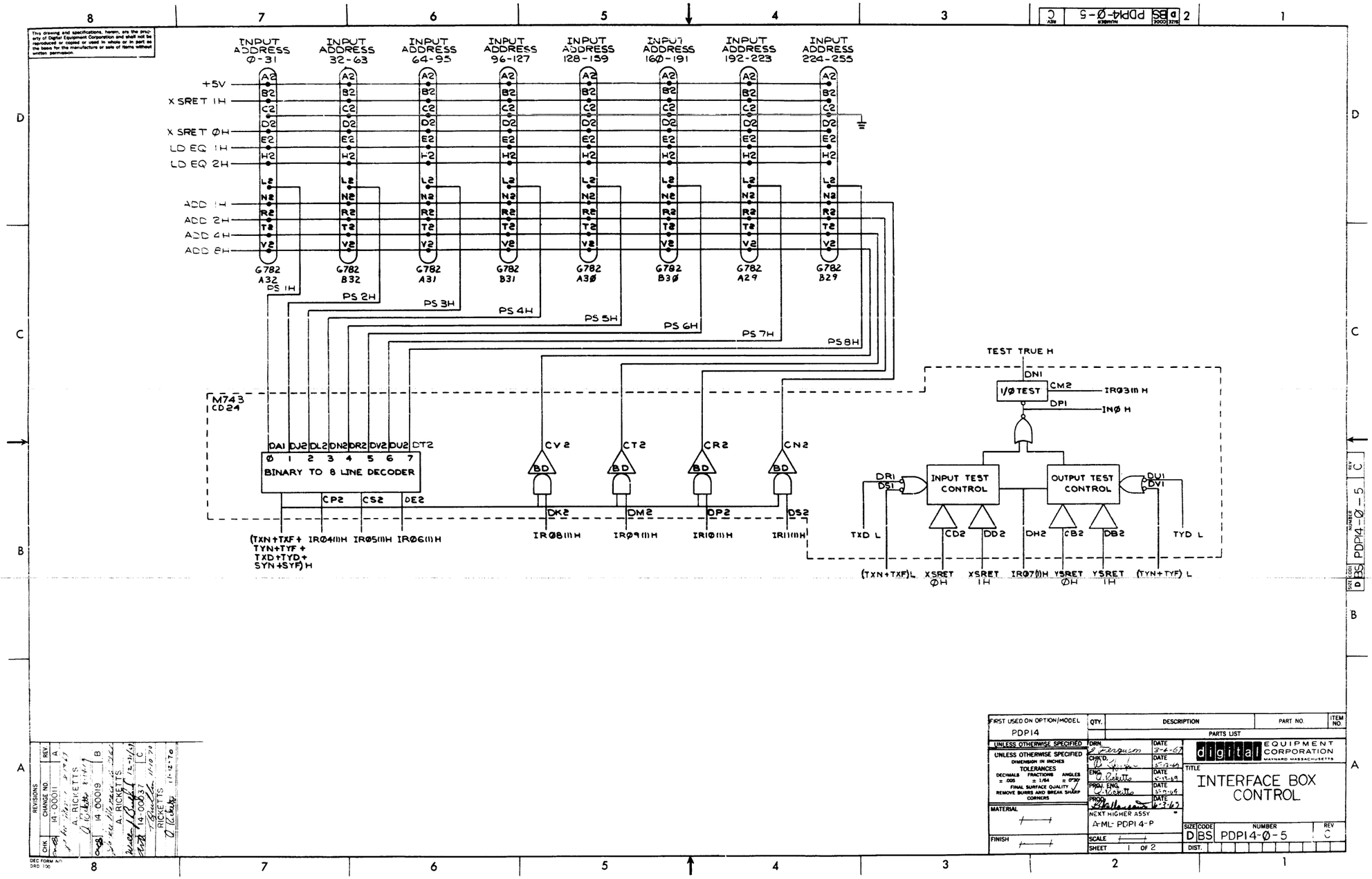
REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 102A

SIZE	CODE	NUMBER	REV.
D	BS	PDP14-Ø-4	



BUS Ø6 L
BUS Ø7 L
BUS Ø8 L
BUS Ø9 L
BUS 1Ø L
BUS 11 L
M746 D23
M746 D18
M747 D19
M746 D21
SOR-IR H
SOR-MB (4-11) H
SOR-PC1 (4-11) H
SOR-PC2H
INSTRUCTION REGISTER
MEMORY BUFFER
PROGRAM COUNTER 1
PROGRAM COUNTER 2
INITIALIZE H
LD IR L
CLR MB H
LD MB L
CLR PC1 H
LD PC1 L
INCREMENT ENABLE H
DECREMENT ENABLE H
LD PC2 L
MBS Ø6 L
MBS Ø7 L
MBS Ø8 L
MBS Ø9 L
MBS 1Ø L
MBS 11 L
PC1S Ø6 L
PC1S Ø7 L
PC1S Ø8 L
PC1S Ø9 L
PC1S 1Ø L
PC1S 11 L
BUS Ø6H
BUS Ø7H
BUS Ø8H
BUS Ø9H
BUS 1Ø H
BUS 11H
FIRST USED ON OPTION/MODEL
PDP14
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DRN. J. Ferguson DATE 3-4-69
CHK'D. DATE 5-12-69
ENG. DATE 5-13-69
PROJ. ENG. DATE 5-13-69
PROD. DATE 6-3-69
NEXT HIGHER ASSY
A-ML-PDP14-Ø
SCALE
SHEET 2 OF 2
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
(BITS 6-11)
MAJOR REGISTERS
SIZE D
CODE BS
NUMBER PDP14-Ø-4
REV.
DIST.
REVISIONS
CHANGE NO.
CHK
REV.



INPUT ADDRESS Ø-31
INPUT ADDRESS 32-63
INPUT ADDRESS 64-95
INPUT ADDRESS 96-127
INPUT ADDRESS 128-159
INPUT ADDRESS 16Ø-191
INPUT ADDRESS 192-223
INPUT ADDRESS 224-255
+5V
X SRET 1H
X SRET ØH
LD EQ 1H
LD EQ 2H
ADD 1H
ADD 2H
ADD 4H
ADD 8H
G782 A32
G782 B32
G782 A31
G782 B31
G782 A3Ø
G782 B3Ø
G782 A29
G782 B29
PS 1H
PS 2H
PS 3H
PS 4H
PS 5H
PS 6H
PS 7H
PS 8H
M743 CD24
BINARY TO 8 LINE DECODER
CP2
CS2
DE2
CV2
CT2
CR2
CN2
DK2
DM2
DP2
DS2
IRØ8(1)H
IRØ9(1)H
IRØ10(1)H
IR11(1)H
TEST TRUE H
DN1
1/Ø TEST
CM2
IRØ3(1)H
DP1
INØ H
INPUT TEST CONTROL
OUTPUT TEST CONTROL
DR1
DS1
DU1
DV1
TXD L
TYD L
CD2
DD2
DH2
CB2
DB2
(TXN+TXF)L
XSRET ØH
XSRET 1H
IRØ7(1)H
YSRET ØH
YSRET 1H
(TYN+TYF) L
FIRST USED ON OPTION/MODEL
PDP14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE
NEXT HIGHER ASSY
A-ML-PDP14-P
SCALE
SHEET 1 OF 2
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
INTERFACE BOX CONTROL
SIZE D
CODE BS
NUMBER PDP14-Ø-5
REV C
DIST.
REVISIONS
CHK
CHANGE NO.
REV
14-00011
A
A. RICKETTS
14-00019
B
A. RICKETTS
14-00037
C
RICKETTS
11-12-70
DEC FORM NO. DRD 100

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OUTPUT ADDRESS Ø-15 / 32-47 / 64-79 / 96-111 / 128-143 / 160-175 / 192-207 / 224-239

+5V
Y SRET Ø H
LD EQ 3H
E SET Ø H
CLEAR I/O L
ER SET Ø H
PS1H PS2H PS3H PS4H PS5H PS6H PS7H PS8H
ADD 1 H
ADD 2 H
ADD 4 H
ADD 8 H

G782 C32 / C31 / C30 / C29 / C28 / C27 / C26 / C25

OUTPUT ADDRESS 16-31 / 48-63 / 80-95 / 112-127 / 144-159 / 176-191 / 208-223

+5V
Y SRET 1 H
LDEQ 4 H
E SET 1 H
CLEAR I/O L
ER SET 1 H
PS1H PS2H PS3H PS4H PS5H PS6H PS7H
LO EQ 3H
ADD 1 H
Y SRETØ H
ADD 2 H
ADD 4 H
ADD 8 H

G782 D32 / D31 / D30 / D29 / D28 / D27 / D26

G782 D25

PS8H
ADD 1 H
ADD 2 H
ADD 4 H
ADD 8 H
PS7H
PS6H
PS5H
PS4H
PS3H
PS2H
PS1H

OUTPUT ADDRESS 240-255
X SRET 1 H
YSRETØ H
X SRETØ H

I/O STROBE L (3R1)
(SYN+SYF) L (3S1)
M742 CD22 (BP1)
X OUT ENABLE H

M743 CD24
CJ2
CN1
INITIALIZE L
CE2 CC1 CF2 CH2
OUTPUT SET-RESET CONTROL
CLEAR ALL OUTPUTS
CM2 DH2
CA1 CB1 K OUT ENABLE H
+3V
IRØ3(1)H
IRØ7(1)H

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP14		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRN. Gordon Ferguson DATE 3-26-69
CHK'D. DATE 5-7-69
ENG. DATE 5-7-69
PROJ. ENG. DATE 5-3-69
PROJ. DATE 5-3-69
NEXT HIGHER ASSY A-ML-PDP14-P
SCALE
SHEET 2 OF 2

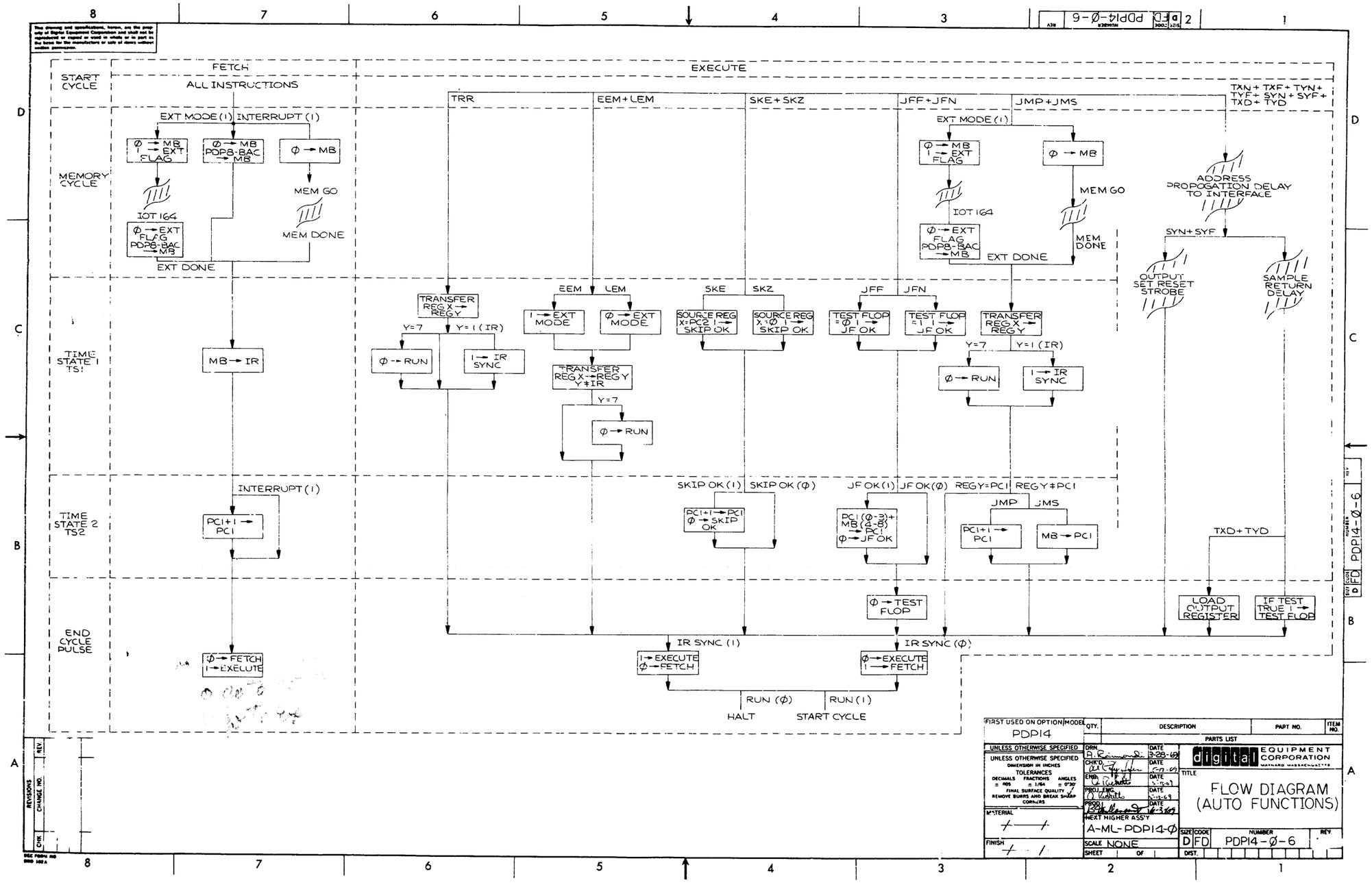
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

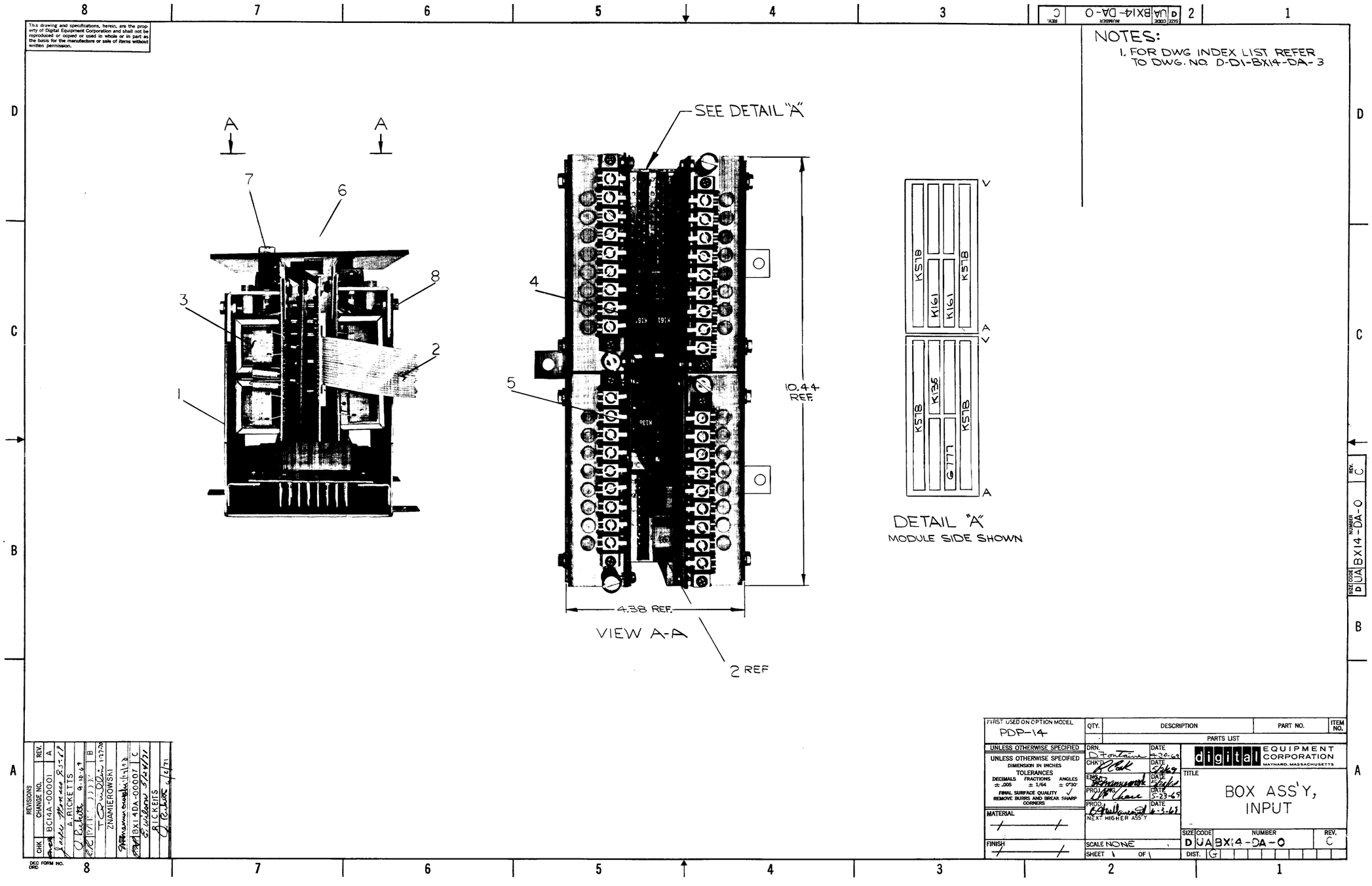
TITLE: INTERFACE BOX CONTROL

SIZE D | CODE BS | NUMBER PDP14-Ø-5 | REV C | DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM NO DRD 102A


START CYCLE
FETCH
EXECUTE
ALL INSTRUCTIONS
TRR
EEM+LEM
SKE+SKZ
JFF+JFN
JMP+JMS
TXN+TXF+TYN+TYF+SYN+SYF+TXD+TYD
MEMORY CYCLE
EXT MODE (1)
INTERRUPT (1)
Ø → MB 1 → EXT FLAG
Ø → MB PDP8-BAC → MB
Ø → MB
MEM GO
MEM DONE
IOT 164
Ø → EXT FLAG PDP8-BAC → MB
EXT DONE
ADDRESS PROPOGATION DELAY TO INTERFACE
SYN+SYF
OUTPUT SET RESET STROBE
SAMPLE RETURN DELAY
TIME STATE 1 TS1
MB → IR
TRANSFER REG X → REG Y
Y=7
Y=1 (IR)
Ø → RUN
1 → IR SYNC
EEM
LEM
1 → EXT MODE
Ø → EXT MODE
TRANSFER REG X → REG Y Y≠IR
SKE
SKZ
SOURCE REG X=PC2 1 → SKIP OK
SOURCE REG X=Ø 1 → SKIP OK
JFF
JFN
TEST FLOP =Ø 1 → JF OK
TEST FLOP =1 1 → JF OK
TRANSFER REG X → REG Y
TIME STATE 2 TS2
INTERRUPT (1)
PC1+1 → PC1
SKIP OK (1)
SKIP OK (Ø)
PC1+1 → PC1 Ø → SKIP OK
JF OK (1)
JF OK (Ø)
PC1 (Ø-3)+ MB (4-8) → PC1 Ø → JF OK
REG Y=PC1
REG Y≠PC1
JMP
JMS
PC1+1 → PC1
MB → PC1
TXD+TYD
END CYCLE PULSE
Ø → FETCH 1 → EXECUTE
Ø → TEST FLOP
LOAD OUTPUT REGISTER
IF TEST TRUE 1 → TEST FLOP
IR SYNC (1)
IR SYNC (Ø)
1 → EXECUTE Ø → FETCH
Ø → EXECUTE 1 → FETCH
RUN (Ø)
RUN (1)
HALT
START CYCLE
FIRST USED ON OPTION/MODEL
PDP14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE
NEXT HIGHER ASS'Y
A-ML-PDP14-Ø
SCALE NONE
SHEET
OF
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
FLOW DIAGRAM (AUTO FUNCTIONS)
SIZE D
CODE FD
NUMBER PDP14-Ø-6
REV.
DIST.
REVISIONS
CHANGE NO.
CHK
REV.



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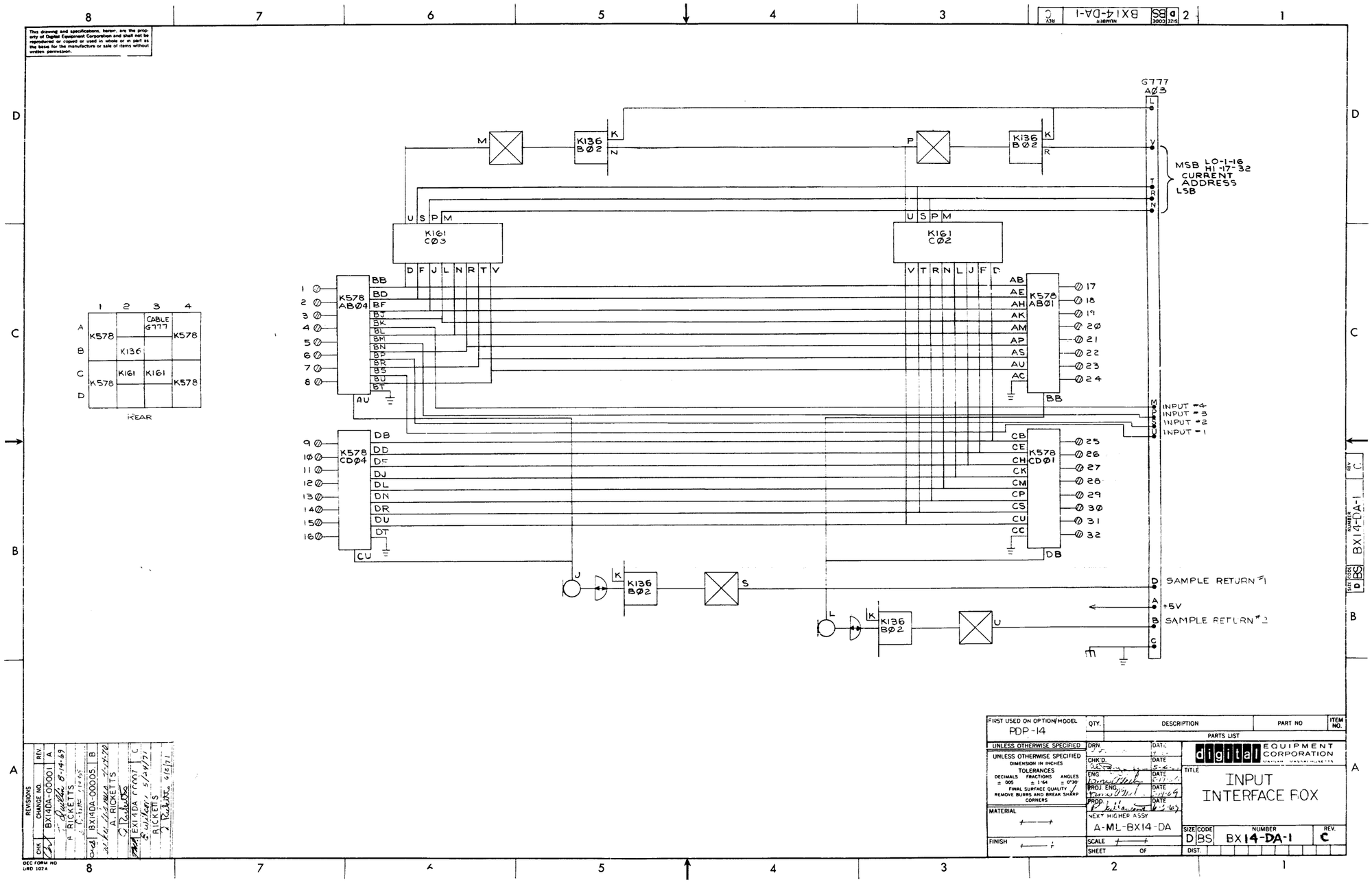
NOTES:
1. FOR DWG INDEX LIST REFER TO DWG. NO. D-D1-BX14-DA-3
SEE DETAIL "A"
A
A
7
6
8
3
2
1
4
5
10.44 REF.
4.38 REF.
VIEW A-A
2 REF
K578
K161
K161
K578
K578
K135
G777
K578
V
A
V
A
DETAIL "A"
MODULE SIDE SHOWN
FIRST USED ON OPTION MODEL
PDP-14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN. D. Fontaine
DATE 4-30-69
CHK'D
DATE 5/2/69
ENG.
DATE 5/2/69
PROJ. ENG.
DATE 5-23-69
PROD.
DATE 6-3-69
NEXT HIGHER ASS'Y
SCALE NONE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
BOX ASS'Y, INPUT
SIZE D
CODE UA
NUMBER BX14-DA-0
REV. C
DIST. G
REVISIONS
CHK
CHANGE NO.
REV.
BC14A-00001
A
A. RICKETTS
B
ZNAMIEROWSKI
BX14DA-00007
C
RICKETS
DEC FORM NO.
DRD



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G777
AØ3
MSB LO-1-16
HI-17-32
CURRENT
ADDRESS
LSB
K136
BØ2
K161
CØ3
K161
CØ2
K578
ABØ4
K578
ABØ1
K578
CDØ4
K578
CDØ1
INPUT #4
INPUT #3
INPUT #2
INPUT #1
SAMPLE RETURN #1
+5V
SAMPLE RETURN #2
CABLE
G777
K578
K136
K161
REAR
FIRST USED ON OPTION/MODEL
PDP-14
QTY.
DESCRIPTION
PART NO
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN
CHK'D
ENG
PROJ. ENG
PROD
DATE
NEXT HIGHER ASSY
A-ML-BX14-DA
SCALE
SHEET
OF
digital EQUIPMENT CORPORATION
TITLE
INPUT
INTERFACE BOX
SIZE
CODE
NUMBER
REV.
D
BS
BX14-DA-1
C
DIST.
REVISIONS
CHANGE NO.
REV.
BX14DA-00001
A
BX14DA-00005
B
A. RICKETTS
DEC FORM NO
URD 102A

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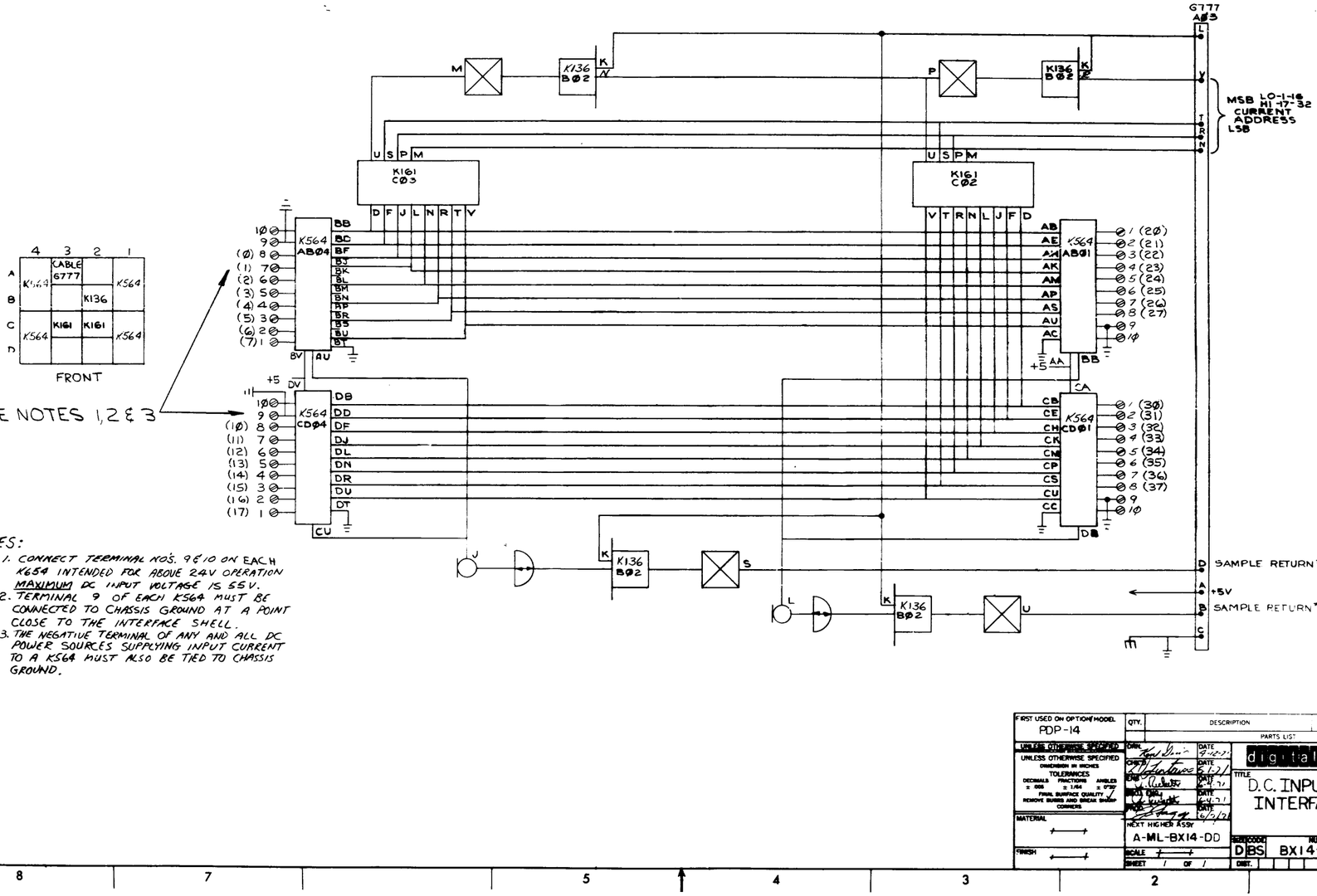

NOTES:

1. CONNECT TERMINAL NOS. 9&10 ON EACH K654 INTENDED FOR ABOVE 24V OPERATION MAXIMUM DC INPUT VOLTAGE IS 55V.
2. TERMINAL 9 OF EACH K564 MUST BE CONNECTED TO CHASSIS GROUND AT A POINT CLOSE TO THE INTERFACE SHELL.
3. THE NEGATIVE TERMINAL OF ANY AND ALL DC POWER SOURCES SUPPLYING INPUT CURRENT TO A K564 MUST ALSO BE TIED TO CHASSIS GROUND.

FIRST USED ON OPTION/MODEL	PDP-14
UNLESS OTHERWISE SPECIFIED	DIMENSIONS IN INCHES; TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'; FINAL SURFACE QUALITY √; REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL	
FINISH	
NEXT HIGHER ASSY	A-ML-BX14-DD
SCALE	
SHEET	1 OF 1
QTY.	DESCRIPTION
PARTS LIST	
DRN	Fred Yen 8-20-71
CHK'D	Jim Andrews 8-21-71
ENG	Wm Mc Kay 8-27-71
APVD	Jim Andrews 8-27-71
MGR	Jim Andrews 8-27-71
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
TITLE	D.C. INPUT INTERFACE BOX
SIZE	D
CODE	BS
NUMBER	BX14-DD-1
REV.	
DIST.	

REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO DRD 102 A

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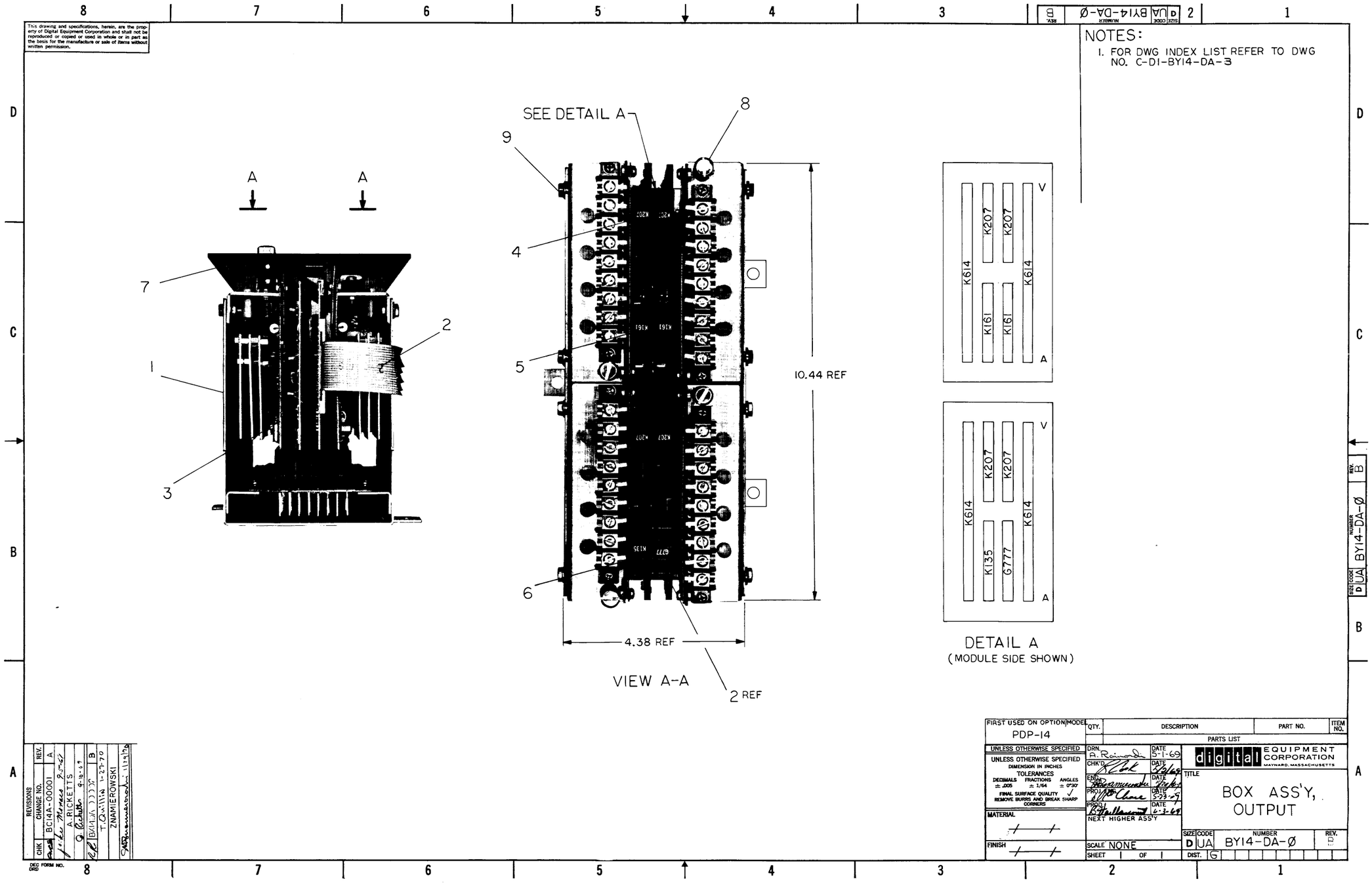

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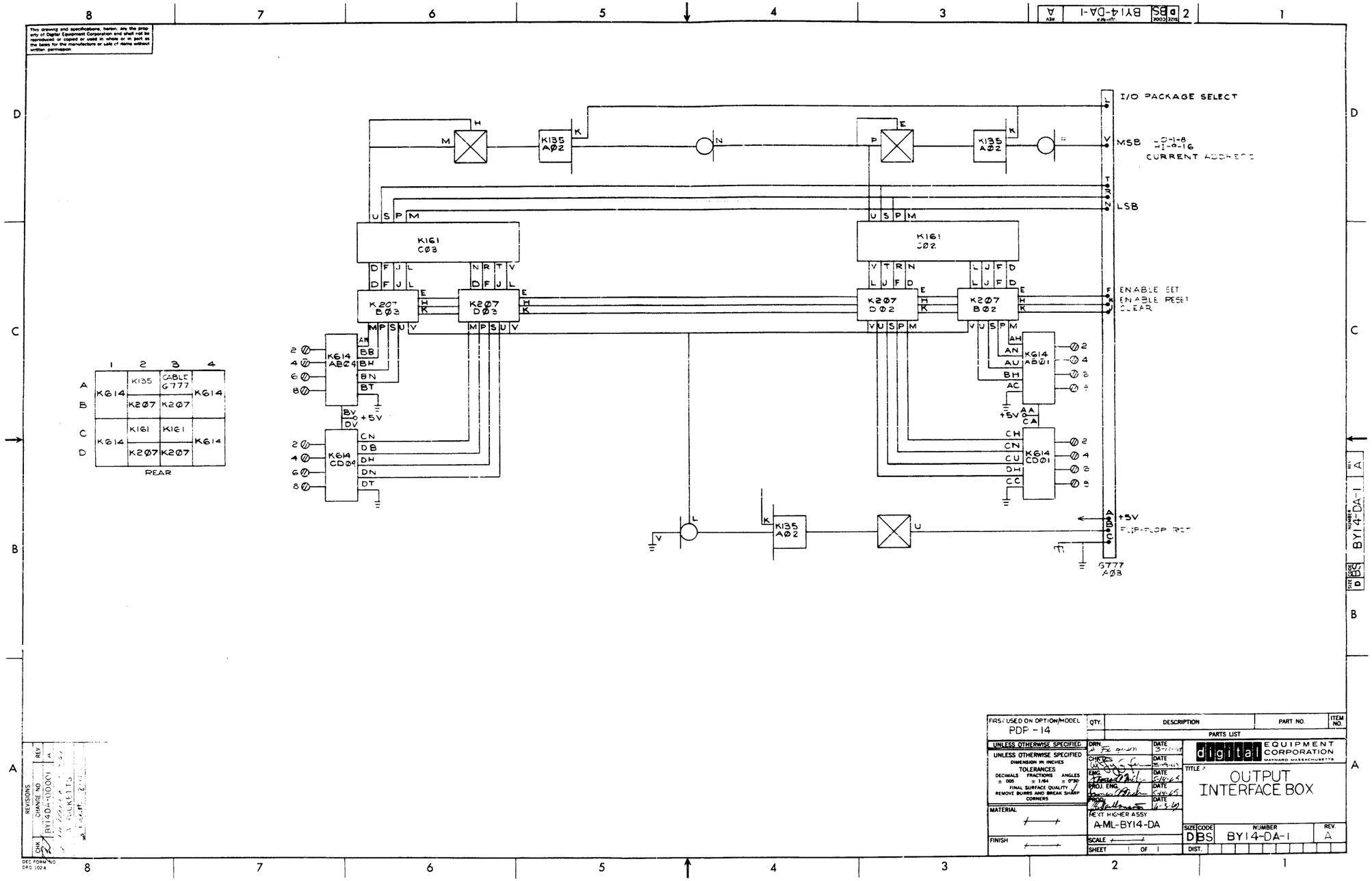
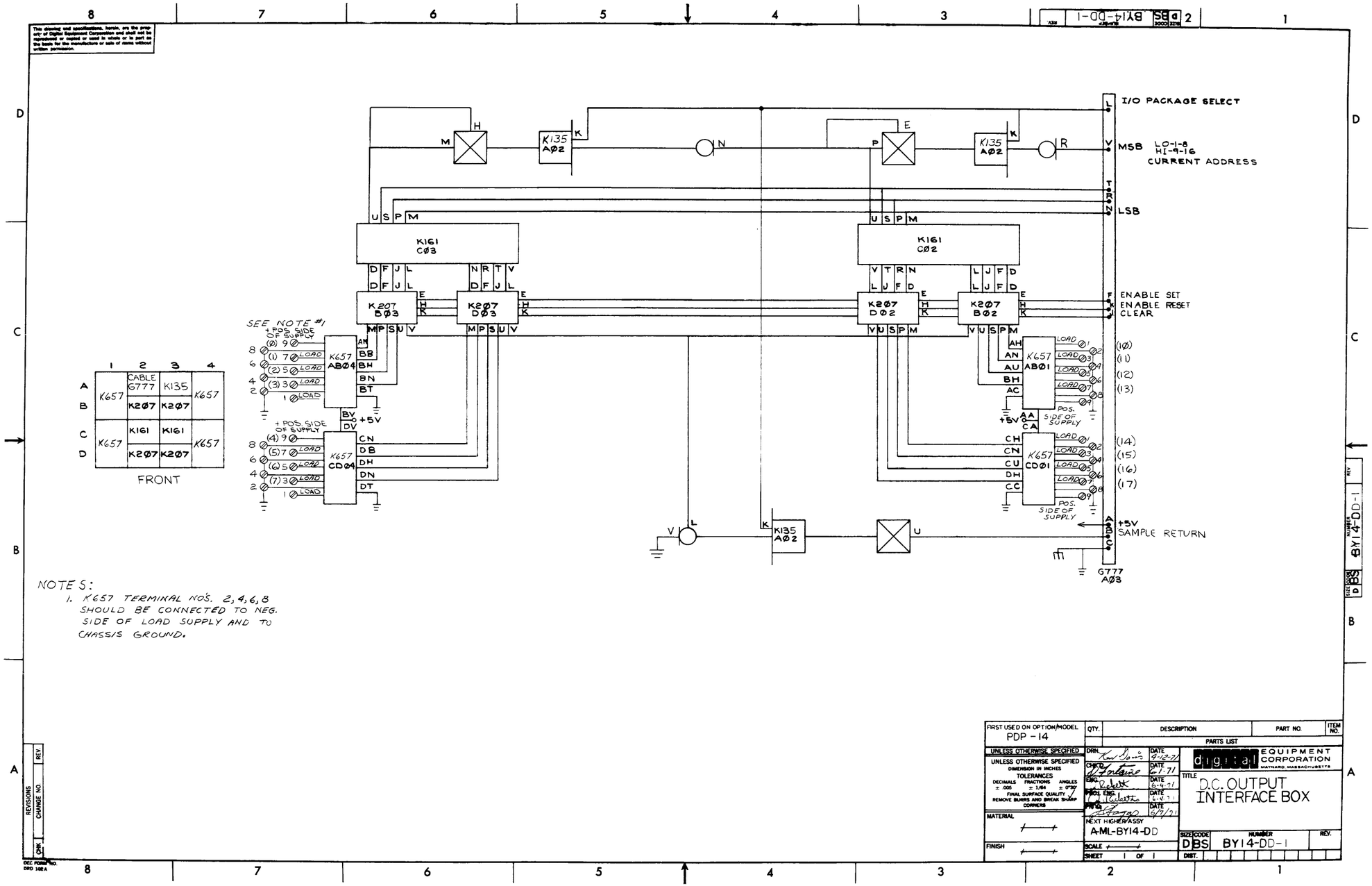
NOTES:
1. FOR DWG INDEX LIST REFER TO DWG NO. C-D1-BY14-DA-3
SEE DETAIL A
A
A
7
2
1
3
9
8
4
5
6
10.44 REF
4.38 REF
2 REF
VIEW A-A
K614
K207
K207
K614
K161
K161
V
A
K614
K207
K207
K614
K135
G777
V
A
DETAIL A
(MODULE SIDE SHOWN)
FIRST USED ON OPTION MODEL
PDP-14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN. A. Raimondi DATE 5-1-69
CHK'D. DATE 5/2/69
ENG. DATE 5/26/69
PROJ. ENG. DATE 5-23-69
PROD. DATE 6-3-69
NEXT HIGHER ASS'Y
SCALE NONE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
BOX ASS'Y, OUTPUT
SIZE D CODE UA NUMBER BY14-DA-Ø REV. B
DIST. G
REVISIONS
CHK CHANGE NO. REV.
BC14A-00001 A
A. RICKETTS
BX14A 1-27-70 B
ZNAMIEROWSKI
DEC FORM NO.


I/O PACKAGE SELECT
MSB
LSB
ENABLE SET
ENABLE RESET
CLEAR
+5V
FLIP-FLOP RST
K135 A02
K161 C03
K161 C02
K207 B03
K207 D03
K207 D02
K207 B02
K614 AB04
K614 CD04
K614 AB01
K614 CD01
G777 A03
REAR
K135
CABLE G777
K161
K207
K614
FIRST USED ON OPTION/MODEL
PDP - 14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
TOLERANCES
MATERIAL
FINISH
NEXT HIGHER ASSY
A-ML-BY14-DA
SCALE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
OUTPUT INTERFACE BOX
SIZE D
CODE BS
NUMBER BY14-DA-1
REV. A
DIST.
REVISIONS
CHANGE NO.
BY14DA-00001
REV A
DEC FORM NO
DPD 102A


I/O PACKAGE SELECT
MSB LO-1-8 HI-9-16 CURRENT ADDRESS
LSB
ENABLE SET
ENABLE RESET
CLEAR
K135 AØ2
K161 CØ3
K161 CØ2
K207 BØ3
K2Ø7 DØ3
K2Ø7 DØ2
K2Ø7 BØ2
K657 ABØ4
K657 CDØ4
K657 ABØ1
K657 CDØ1
SEE NOTE #1
+ POS. SIDE OF SUPPLY
POS. SIDE OF SUPPLY
+5V
SAMPLE RETURN
G777 AØ3
CABLE G777
K135
K2Ø7
K161
K657
FRONT
NOTES:
1. K657 TERMINAL NO'S. 2,4,6,8 SHOULD BE CONNECTED TO NEG. SIDE OF LOAD SUPPLY AND TO CHASSIS GROUND.
FIRST USED ON OPTION/MODEL PDP-14
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
QTY. DESCRIPTION PART NO. ITEM NO.
PARTS LIST
DRN. DATE 4-12-71
CHK'D. DATE 6-1-71
ENG. DATE 6-4-71
PROJ. ENG. DATE 6-4-71
PROG. DATE 6/7/71
NEXT HIGHER ASSY A-ML-BY14-DD
SCALE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE D.C. OUTPUT INTERFACE BOX
SIZE D CODE BS NUMBER BY14-DD-1 REV.
DIST.
REVISIONS CHANGE NO. REV. CHK.
DEC FORM NO. DRD 108A

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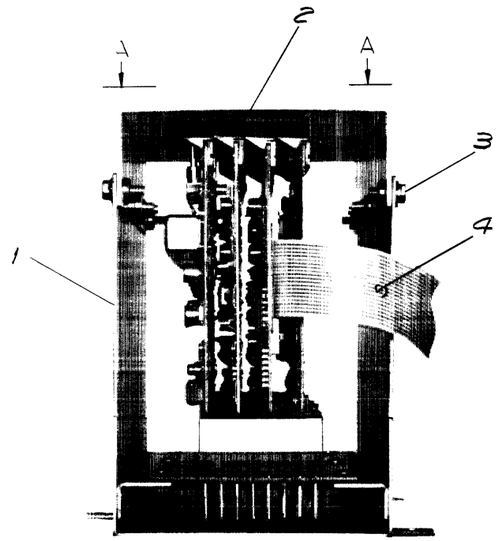
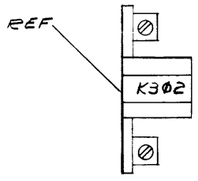
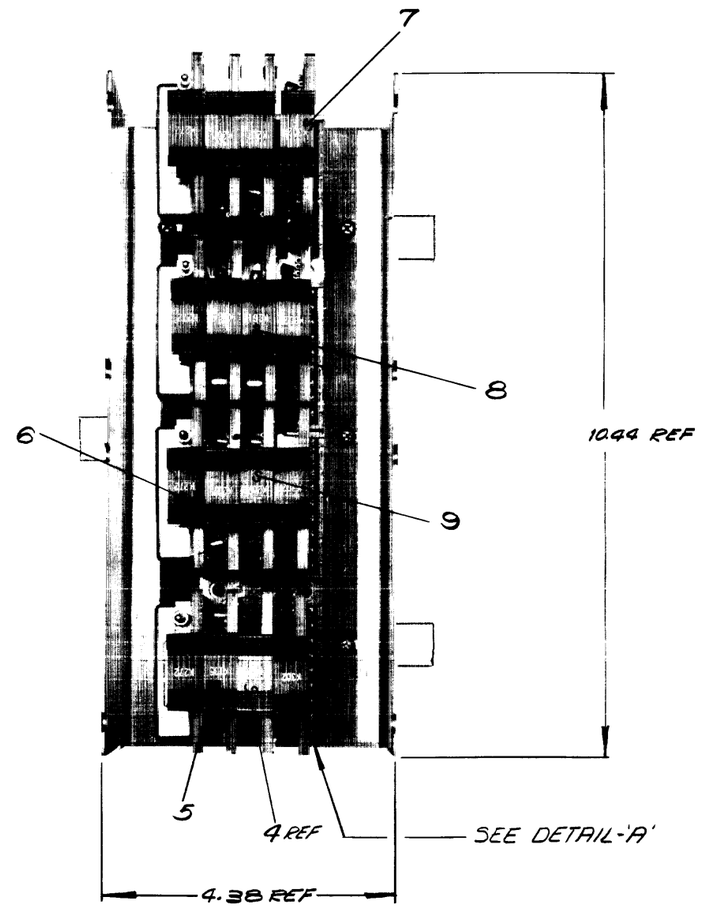
NOTES:
1. FOR DWG INDEX LIST REFER TO DWG NO. D-DI-BA14-Ø-3
2. IN SLOTS MARKED * * K3Ø2, KØ22, K274, OR K272 MODULES CAN BE USED.
3. IN SLOTS MARKED * ONLY K3Ø2, KØ22, OR K274 MODULES CAN BE USED.

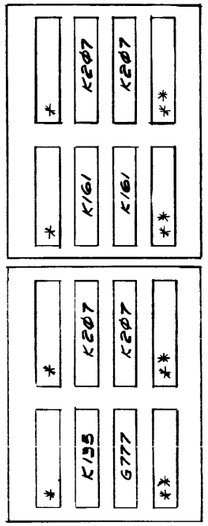




TO ADJUST TIMER MODULE, TURN SCREW CLOCKWISE FOR ADVANCE, AND COUNTER-CLOCKWISE FOR DECREASE.



VIEW A-A
(WITH ITEM 2 & 3 REMOVED)



DETAIL-'A'
(MODULE SIDE SHOWN)
CUSTOMER MUST SPECIFY THE NUMBER OF K3Ø2 AND KØ22, K274 AND K272 MODULES. MAXIMUM NUMBER OF K272 MODULES IS 4.

TOLERANCES
DECIMAL
.XXX = ± .005
.XX = ± .02
.X = ± .1

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

FIRST USED ON OPTION MOD: PDP14
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL —"—
FINISH —"—

DRN. [signature] DATE 5-20-69
CHK'D [signature] DATE 8/29/69
ENG. [signature] DATE 9/11/69
PROJ. ENG. [signature] DATE 9-17-69
PROD. [signature] DATE 9-22-69
NEXT HIGHER ASSY: A-ML-BA14-Ø
SCALE —"—
SHEET OF

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: BOX ASSY ACCESSORY

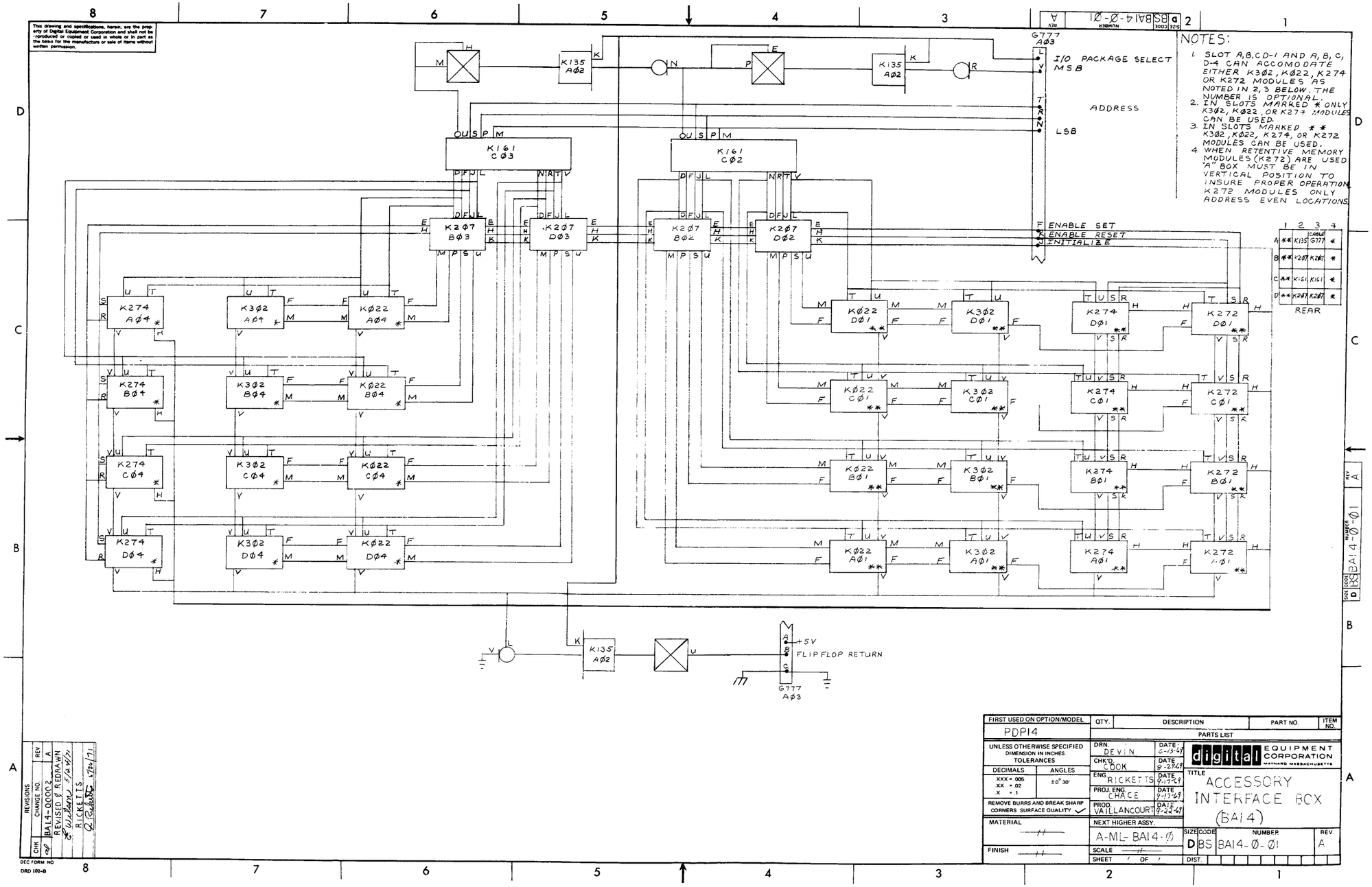
SIZE	CODE	NUMBER	REV.
D	UA	BA14-Ø-Ø	A

DIST.

REVISIONS

CHK	CHANGE NO.	REV.
	BA14-00002	A

DEC FORM NO. DRC



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NOTES:
1. SLOT A,B,C,D-1 AND A,B,C,D-4 CAN ACCOMODATE EITHER K3Ø2, KØ22, K274 OR K272 MODULES AS NOTED IN 2,3 BELOW. THE NUMBER IS OPTIONAL.
2. IN SLOTS MARKED * ONLY K3Ø2, KØ22, OR K274 MODULES CAN BE USED.
3. IN SLOTS MARKED ** K3Ø2, KØ22, K274, OR K272 MODULES CAN BE USED.
4. WHEN RETENTIVE MEMORY MODULES (K272) ARE USED "A" BOX MUST BE IN VERTICAL POSITION TO INSURE PROPER OPERATION. K272 MODULES ONLY ADDRESS EVEN LOCATIONS.
I/O PACKAGE SELECT
MSB
ADDRESS
LSB
ENABLE SET
ENABLE RESET
INITIALIZE
REAR
+5V
FLIP FLOP RETURN
G777 AØ3
K135 AØ2
K161 CØ3
K161 CØ2
K2Ø7 BØ3
K2Ø7 DØ3
K2Ø7 BØ2
K2Ø7 DØ2
K274 AØ4
K3Ø2 AØ4
KØ22 AØ4
K274 BØ4
K3Ø2 BØ4
KØ22 BØ4
K274 CØ4
K3Ø2 CØ4
KØ22 CØ4
K274 DØ4
K3Ø2 DØ4
KØ22 DØ4
KØ22 DØ1
K3Ø2 DØ1
K274 DØ1
K272 DØ1
KØ22 CØ1
K3Ø2 CØ1
K274 CØ1
K272 CØ1
KØ22 BØ1
K3Ø2 BØ1
K274 BØ1
K272 BØ1
KØ22 AØ1
K3Ø2 AØ1
K274 AØ1
K272 AØ1
FIRST USED ON OPTION/MODEL
PDP14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS
ANGLES
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH
DRN. DEVIN
CHK'D. COOK
ENG. RICKETTS
PROJ. ENG. CHACE
PROD. VAILLANCOURT
NEXT HIGHER ASSY. A-ML-BA14-Ø
SCALE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE ACCESSORY INTERFACE BOX (BA14)
SIZE D CODE BS NUMBER BA14-Ø-Ø1 REV. A
DIST.
REVISIONS
CHANGE NO.
REV
BA14-00002
REVISED & REDRAWN
RICKETTS
DEC FORM NO
DRD 102-B

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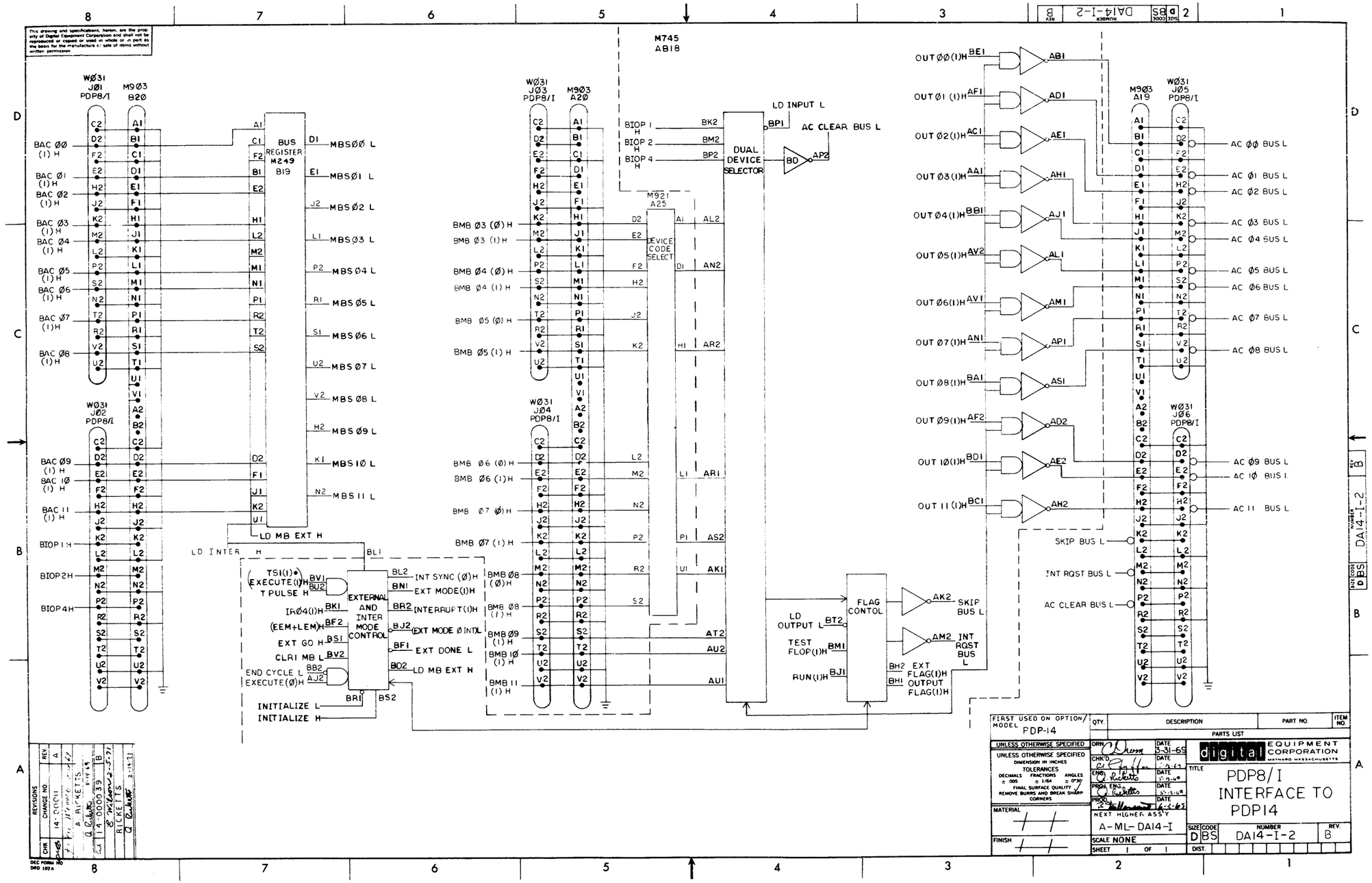


REVISIONS				
CHR	CHANGE NO.	REV		
	14-00011	A	A. RICKETTS	
	14-00039	B	A. RICKETTS	

DEC FORM NO DRD 102A

FIRST USED ON OPTION/MODEL PDP-14

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN		DATE 3-31-69
CHK'D		DATE 4-2-69
ENG	A. Ricketts	DATE 5-13-69
PROJ ENG	A. Ricketts	DATE 5-13-69
PROG		DATE 4-2-69

NEXT HIGHER ASSY A-ML-DA14-I

SCALE NONE

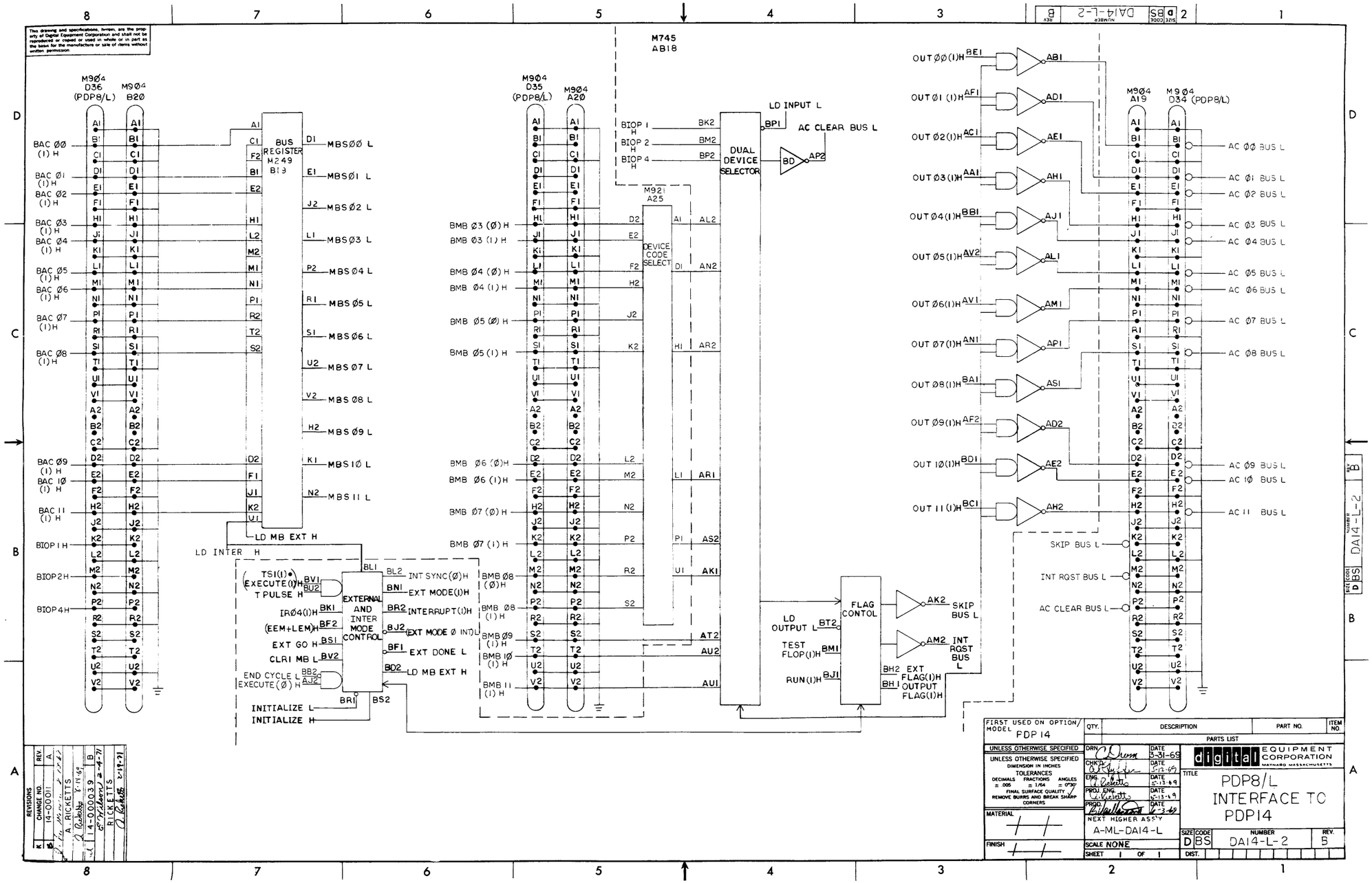
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

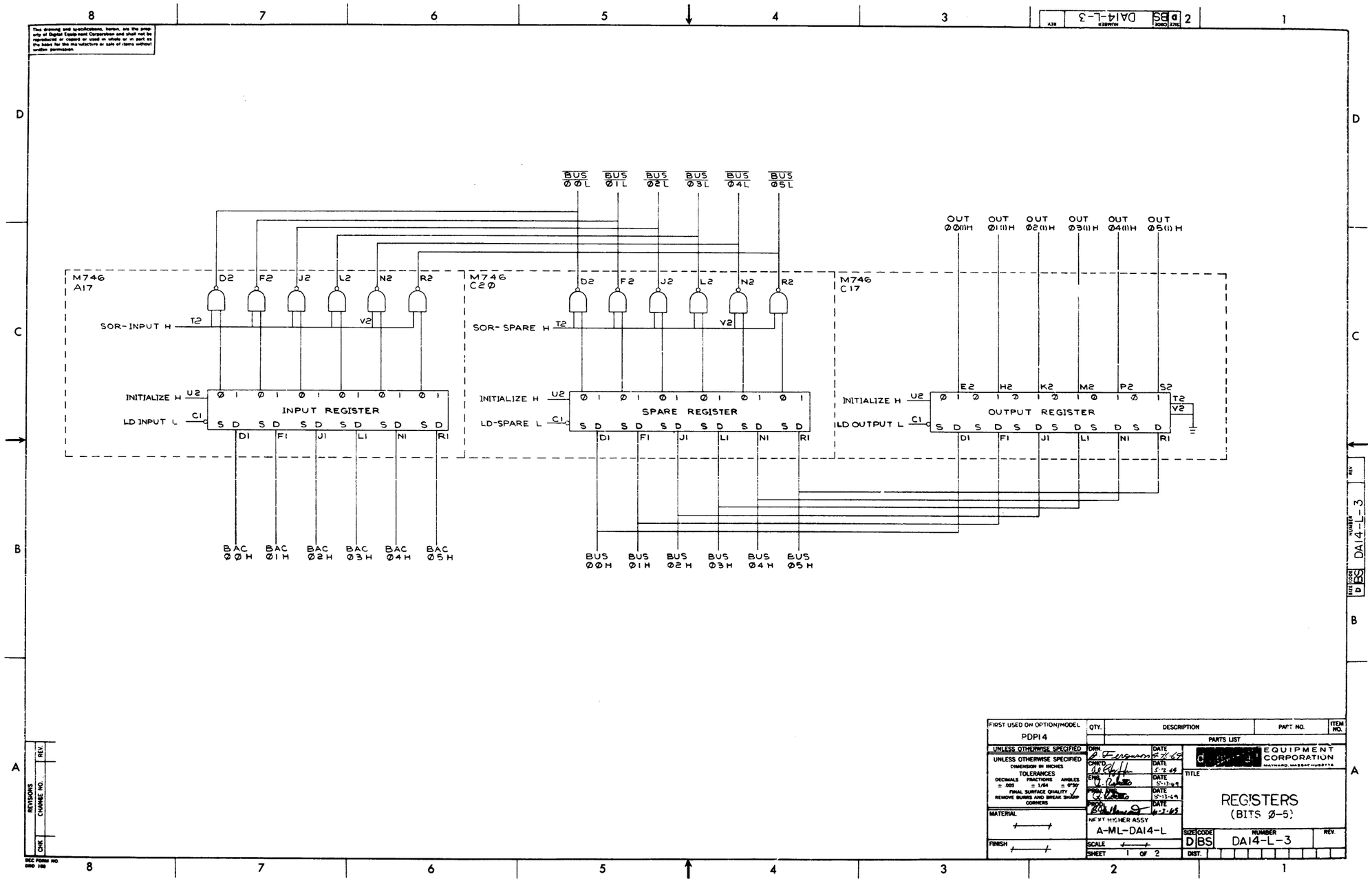
TITLE PDP8/I INTERFACE TO PDP14

SIZE	CODE	NUMBER	REV.
D	BS	DA14-I-2	B

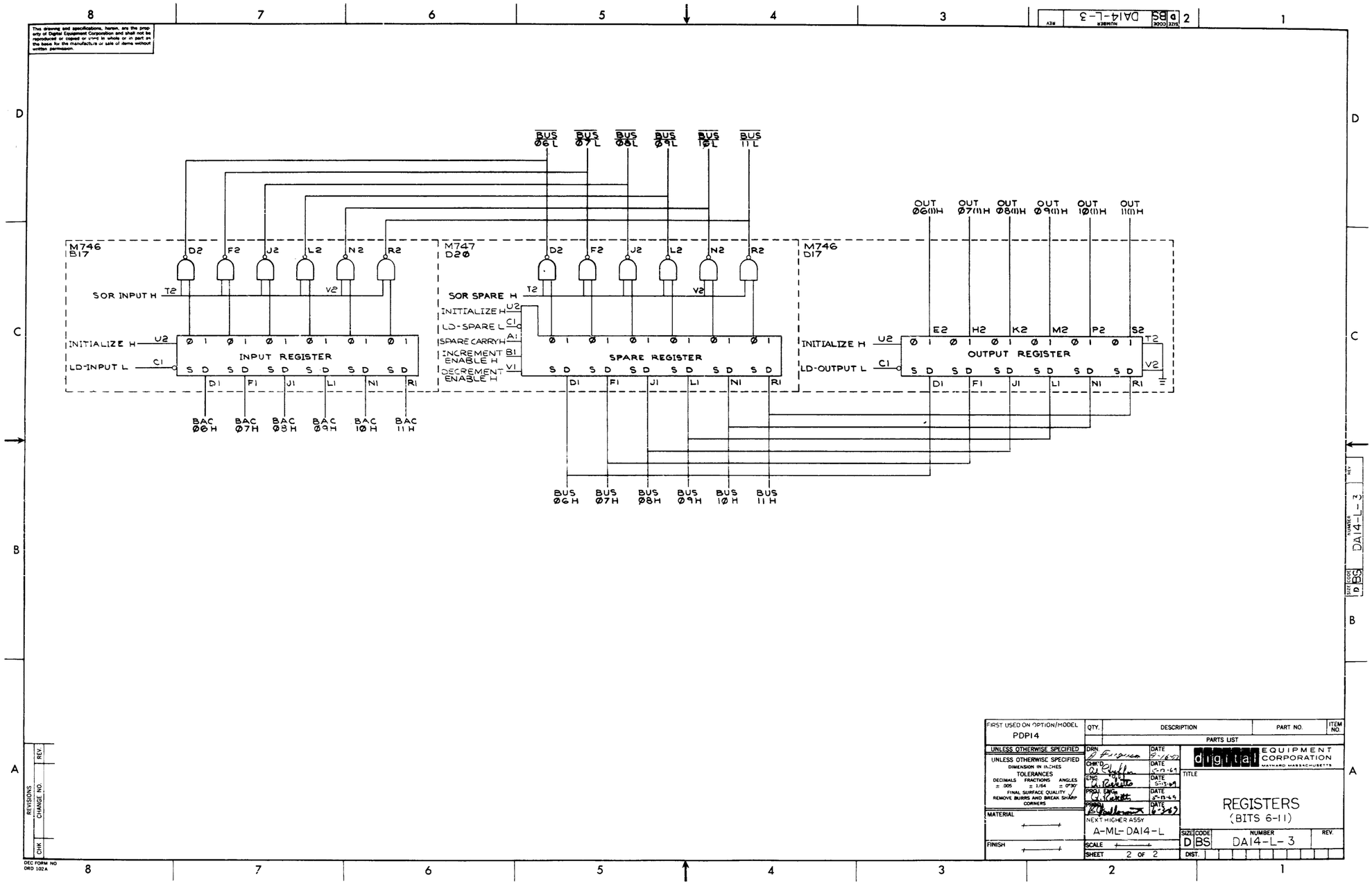
DIST.



M9Ø4 D36 (PDP8/L)
M9Ø4 B2Ø
BUS REGISTER M249 B19
M9Ø4 D35 (PDP8/L)
M9Ø4 A2Ø
M745 AB18
M921 A25
DEVICE CODE SELECT
DUAL DEVICE SELECTOR
LD INPUT L
AC CLEAR BUS L
EXTERNAL AND INTER MODE CONTROL
FLAG CONTOL
M9Ø4 A19
M9Ø4 D34 (PDP8/L)
LD MB EXT H
LD INTER H
INITIALIZE L
INITIALIZE H
SKIP BUS L
INT RQST BUS L
AC CLEAR BUS L
FIRST USED ON OPTION/MODEL PDP 14
UNLESS OTHERWISE SPECIFIED
NEXT HIGHER ASS'Y A-ML-DA14-L
SCALE NONE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE PDP8/L INTERFACE TO PDP14
SIZE D CODE BS NUMBER DA14-L-2 REV. B



BUS ØØL
BUS Ø1L
BUS Ø2L
BUS Ø3L
BUS Ø4L
BUS Ø5L
OUT ØØ(1)H
OUT Ø1(1)H
OUT Ø2(1)H
OUT Ø3(1)H
OUT Ø4(1)H
OUT Ø5(1)H
M746 A17
M746 C2Ø
M746 C17
D2 F2 J2 L2 N2 R2
SOR-INPUT H
SOR-SPARE H
T2
V2
INITIALIZE H
LD INPUT L
LD-SPARE L
LD OUTPUT L
U2
C1
INPUT REGISTER
SPARE REGISTER
OUTPUT REGISTER
E2 H2 K2 M2 P2 S2
D1 F1 J1 L1 N1 R1
BAC ØØH
BAC Ø1H
BAC Ø2H
BAC Ø3H
BAC Ø4H
BAC Ø5H
BUS ØØH
BUS Ø1H
BUS Ø2H
BUS Ø3H
BUS Ø4H
BUS Ø5H
FIRST USED ON OPTION/MODEL
PDP14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE
5-2-69
5-13-69
6-3-69
NEXT HIGHER ASSY
A-ML-DA14-L
SCALE
SHEET 1 OF 2
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
REGISTERS
(BITS Ø-5)
SIZE D
CODE BS
NUMBER DA14-L-3
REV.
DIST.
REVISIONS
CHANGE NO.
REV.
CHK.
DEC FORM NO
DRD 108



M746 B17
M747 D20
M746 D17
SOR INPUT H
INITIALIZE H
LD-INPUT L
INPUT REGISTER
SOR SPARE H
INITIALIZE H
LD-SPARE L
SPARE CARRY H
INCREMENT ENABLE H
DECREMENT ENABLE H
SPARE REGISTER
INITIALIZE H
LD-OUTPUT L
OUTPUT REGISTER
BUS 06 L
BUS 07 L
BUS 08 L
BUS 09 L
BUS 10 L
BUS 11 L
OUT 06(11)H
OUT 07(11)H
OUT 08(11)H
OUT 09(11)H
OUT 10(11)H
OUT 11(11)H
BAC 06 H
BAC 07 H
BAC 08 H
BAC 09 H
BAC 10 H
BAC 11 H
BUS 06 H
BUS 07 H
BUS 08 H
BUS 09 H
BUS 10 H
BUS 11 H
FIRST USED ON OPTION/MODEL
PDP14
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DRN
CHK'D
ENG
PROJ. ENG.
DATE
NEXT HIGHER ASSY
A-ML-DA14-L
SCALE
SHEET 2 OF 2
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
REGISTERS
(BITS 6-11)
SIZE D
CODE BS
NUMBER DA14-L-3
REV.
DIST.
REVISIONS
REV.
CHANGE NO.
CHK
DEC FORM NO
ORD 102A

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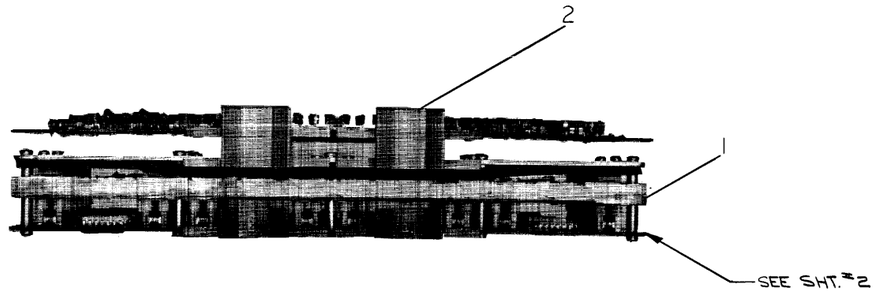

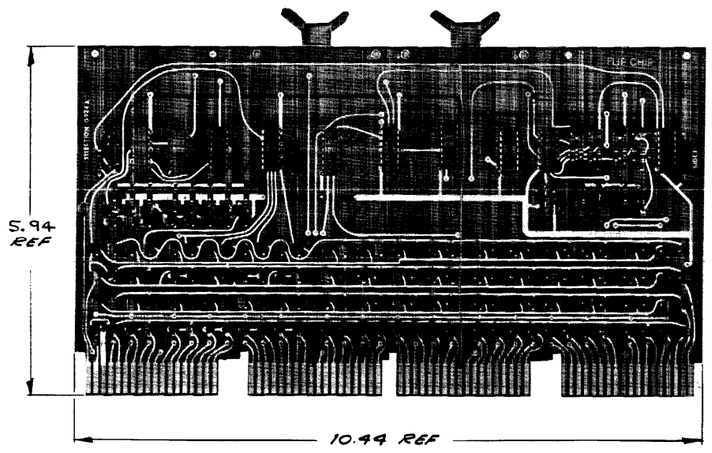

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP14		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. D. Fortier DATE 7-9-69
CHK'D. R. Cook DATE 8/21/69
ENG. S. Ramamurthi DATE 10/2/69
PROJ. ENG. W. P. Chase DATE 10-8-69
PROD. D. Wilder DATE 10/28/69
NEXT HIGHER .. ASSY

SCALE NONE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
READ ONLY MEMORY (MR14)

SIZE D CODE UA NUMBER MR14-Ø-Ø REV.
DIST.

REVISIONS
REV. | CHANGE NO. | CHK

DEC FORM NO. DRC

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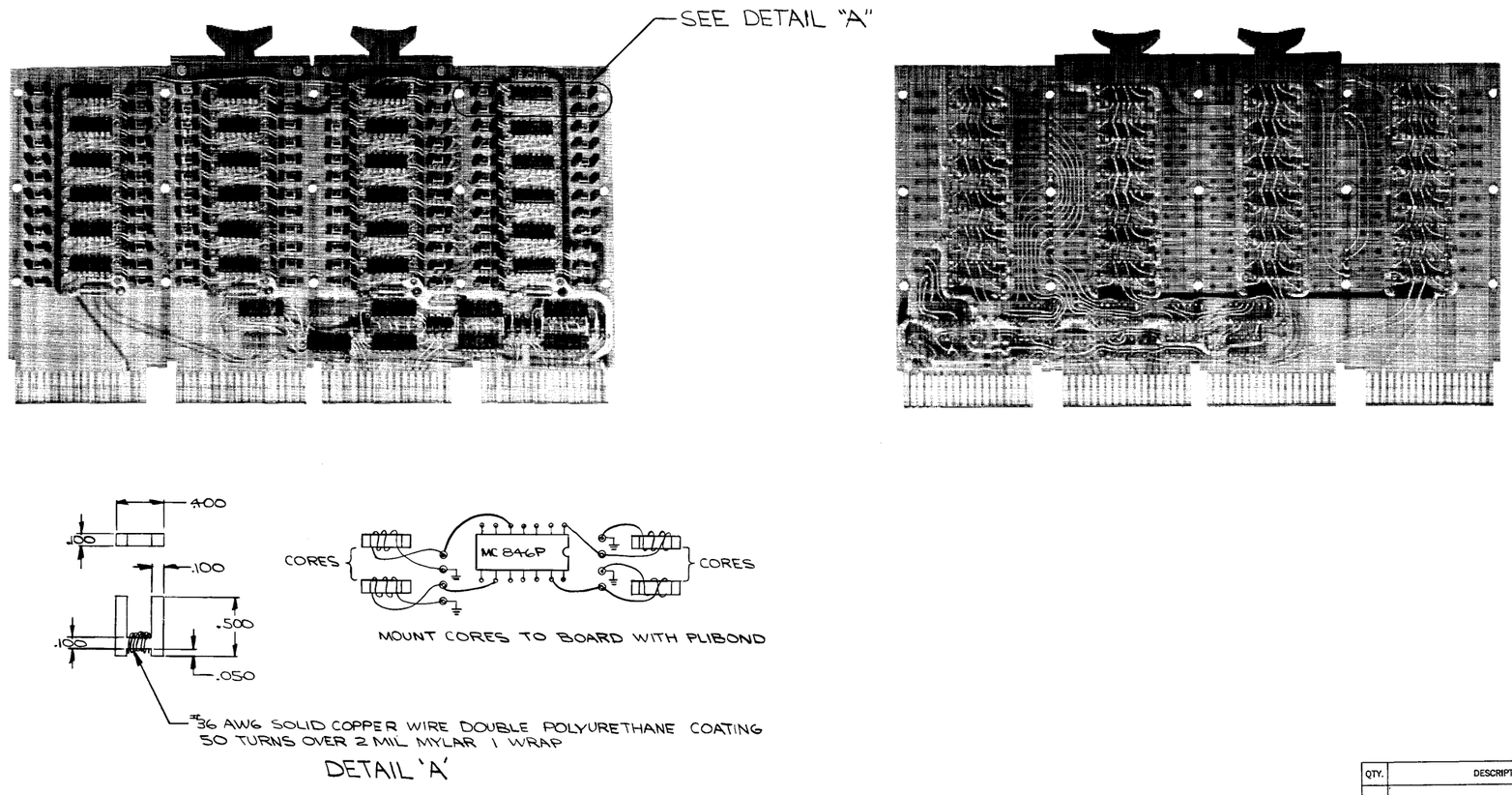

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. D. Fontaine	DATE	
CHK'D R. Cook	DATE 9/24/69	
ENG. [illegible]	DATE 10/2/69	
PROJ. ENG. [illegible]	DATE 10-8-69	
PROD. D. Wallace	DATE 10/27/69	
FIRST USED ON		
SCALE NONE		
SHEET 2 OF 2		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
READ ONLY MEMORY
(MR14)

SIZE	CODE	NUMBER	REV.
D	UA	MR14-Ø-Ø	

DIST. G

REVISIONS
REV.
CHANGE NO.
CHK

DEC FORM NO.
DRD

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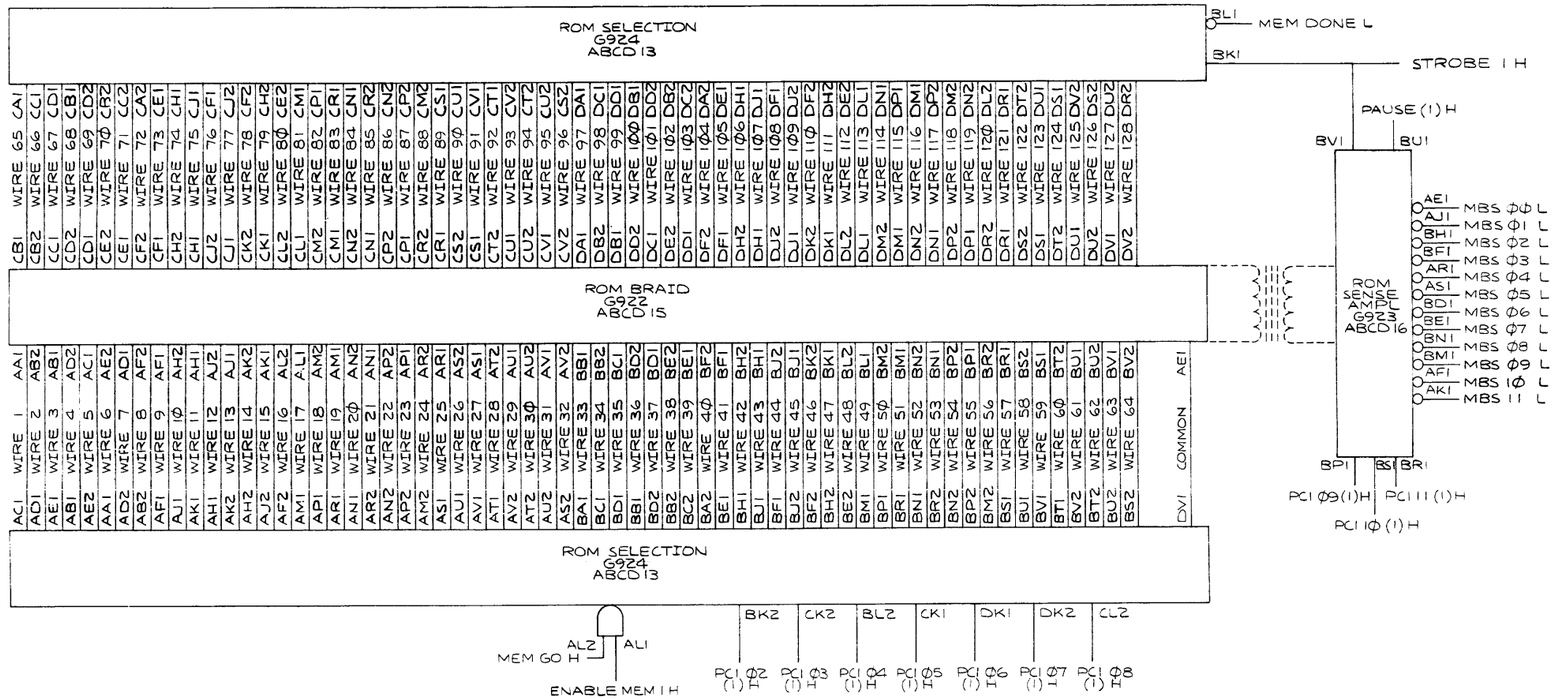


1ST MEMORY OPTION (MR14) INSTALLED

FIRST USED ON OPTION	MODEL
PDP-14	

ITEM NO.	QTY.	DESCRIPTION	PART NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY / REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —/—

FINISH —/—

DRN	A. Bisson	DATE 7-1-69
CHK'D	A.E. Griffin	DATE 7-22-69
ENG	D. Ciletti	DATE 7-23-69
PROJ. ENG	D. Ciletti	DATE 7-22-69
PROG	D. Hebden	DATE 10/15/69

NEXT HIGHER ASSY A-ML-MR14-Ø

SCALE NONE

SHEET 1 OF 4

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
MEMORY (1K)
(OPTIONAL ADDRESSES ØØØØ-1777)

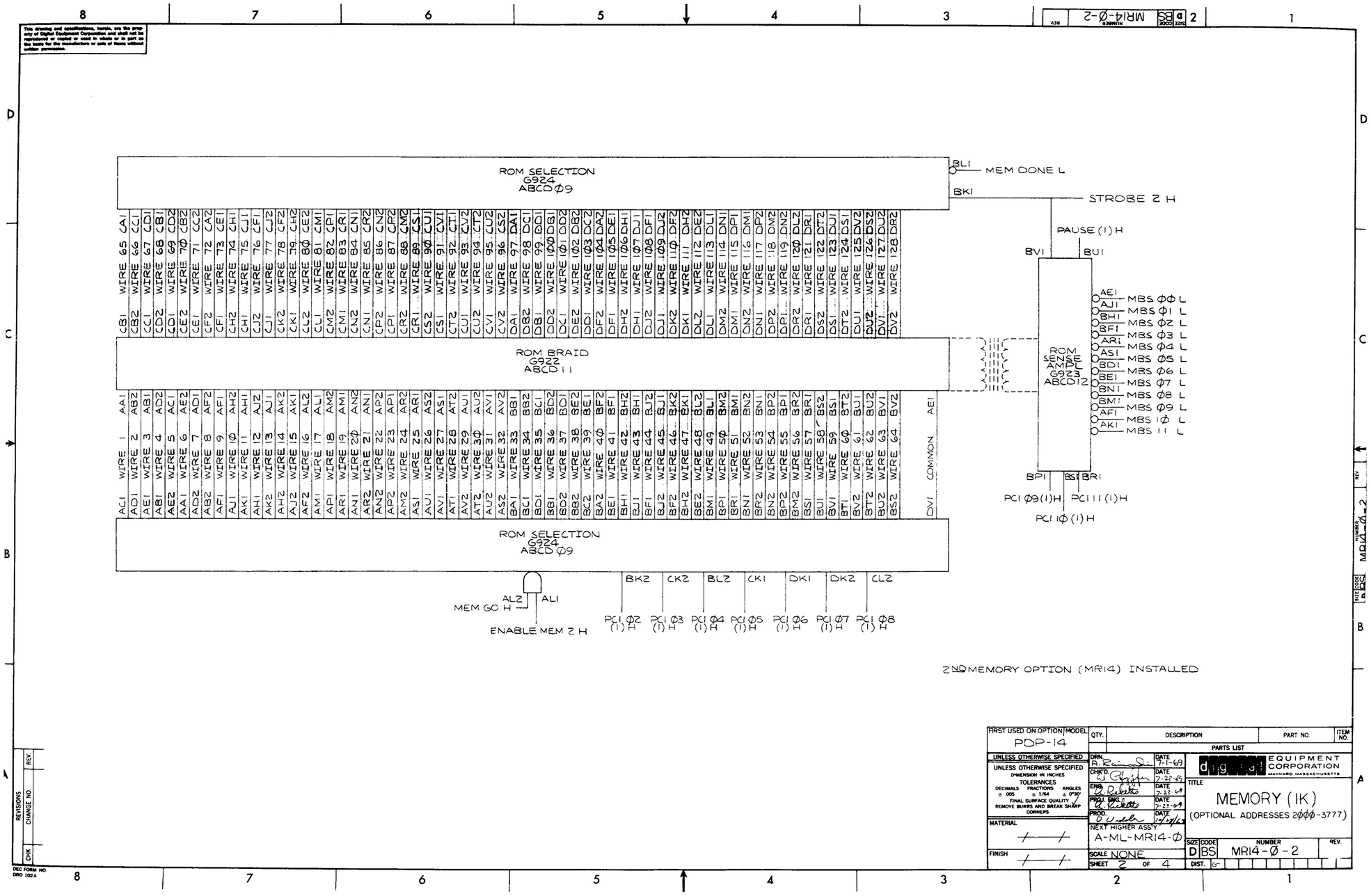
SIZE	CODE	NUMBER	REV.
D	BS	MR14-Ø-2	

DIST.

REVISIONS

REV.	CHANGE NO.	CHK

DEC FORM NO. DRD 102A


ROM SELECTION
G924
ABCD Ø9
ROM BRAID
G922
ABCD 11
ROM SELECTION
G924
ABCD Ø9
MEM DONE L
STROBE 2 H
PAUSE (1) H
ROM SENSE AMPL
G923
ABCD12
MBS ØØ L
MBS Ø1 L
MBS Ø2 L
MBS Ø3 L
MBS Ø4 L
MBS Ø5 L
MBS Ø6 L
MBS Ø7 L
MBS Ø8 L
MBS Ø9 L
MBS 1Ø L
MBS 11 L
PC1 Ø9 (1) H
PC1 11 (1) H
PC1 1Ø (1) H
COMMON
MEM GO H
ENABLE MEM 2 H
PC1 Ø2 (1) H
PC1 Ø3 (1) H
PC1 Ø4 (1) H
PC1 Ø5 (1) H
PC1 Ø6 (1) H
PC1 Ø7 (1) H
PC1 Ø8 (1) H
2ND MEMORY OPTION (MR14) INSTALLED
FIRST USED ON OPTION
MODEL
PDP-14
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DRN.
DATE 7-1-69
CHK'D.
DATE 7-23-69
ENG.
DATE 7-23-69
PROJ. ENG.
DATE 7-23-69
PROD.
DATE 10/27/69
EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
MEMORY (1K)
(OPTIONAL ADDRESSES 2ØØØ-3777)
MATERIAL
NEXT HIGHER ASS'Y
A-ML-MR14-Ø
FINISH
SCALE NONE
SHEET 2 OF 4
SIZE D
CODE BS
NUMBER MR14-Ø-2
REV.
DIST. G
REVISIONS
CHANGE NO.
REV.
CHK
DEC FORM NO. DRD 102A

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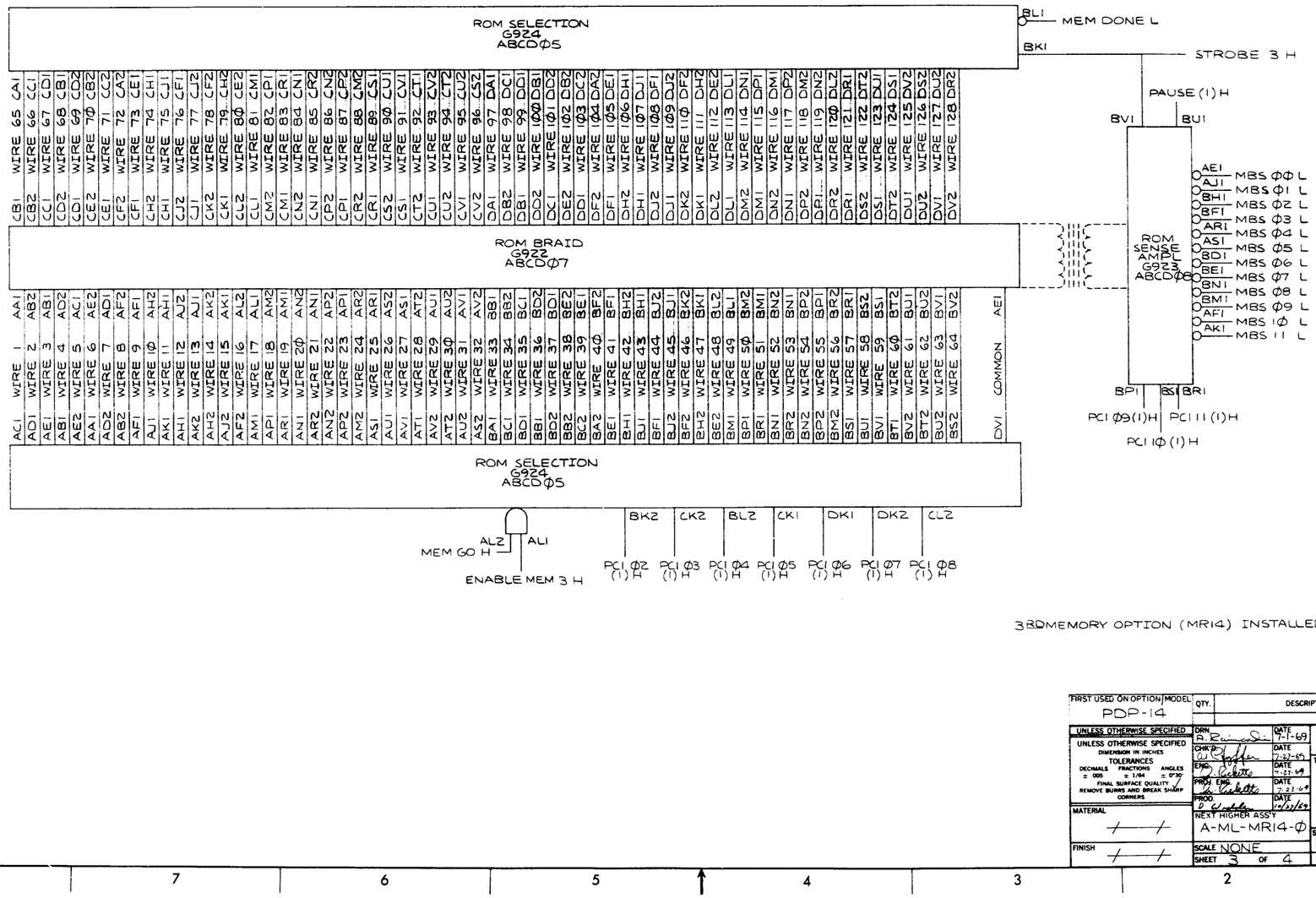

3RD MEMORY OPTION (MR14) INSTALLED

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP-14		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN. A. Rainaldi	DATE 7-1-69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. D. Hallen	DATE 7-22-69	
ENG. D. Corbett	DATE 7-22-69	TITLE MEMORY (1K) (OPTIONAL ADDRESSES 4000-5777)
PROJ. ENG. D. Corbett	DATE 7-22-69	
PROD. D. Hallen	DATE 7-22-69	

NEXT HIGHER ASS'Y A-ML-MR14-Ø

SIZE D | CODE BS | NUMBER MR14-Ø-2 | REV

SCALE NONE | SHEET 3 OF 4 | DIST.

REVISIONS | REV. | CHANGE NO | CHK

DEC FORM NO DRO 102A

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ROM SELECTION
G924
ABCDØ1

CB1 WIRE 65 CA1
CB2 WIRE 66 CC1
CC1 WIRE 67 CD1
CD2 WIRE 68 CB1
CD1 WIRE 69 CC2
CE2 WIRE 70 CB2
CE1 WIRE 71 CC2
CF2 WIRE 72 CA2
CF1 WIRE 73 CE1
CH2 WIRE 74 CH1
CH1 WIRE 75 CJ1
CJ2 WIRE 76 CF1
CJ1 WIRE 77 CJ2
CK2 WIRE 78 CF2
CK1 WIRE 79 CH2
CL2 WIRE 80 CE2
CL1 WIRE 81 CM1
CM2 WIRE 82 CP1
CM1 WIRE 83 CR1
CN2 WIRE 84 CN1
CN1 WIRE 85 CR2
CP2 WIRE 86 CN2
CP1 WIRE 87 CP2
CR2 WIRE 88 CM2
CR1 WIRE 89 CS1
CS2 WIRE 90 CU1
CS1 WIRE 91 CV1
CT2 WIRE 92 CT1
CU1 WIRE 93 CV2
CU2 WIRE 94 CT2
CV1 WIRE 95 CU2
CV2 WIRE 96 CS2
DA1 WIRE 97 DA1
DB2 WIRE 98 DC1
DB1 WIRE 99 DD1
DD2 WIRE 100 DB1
DC1 WIRE 101 DD2
DE2 WIRE 102 DB2
DD1 WIRE 103 DC2
DF2 WIRE 104 DA2
DF1 WIRE 105 DE1
DH2 WIRE 106 DH1
DH1 WIRE 107 DJ1
DJ2 WIRE 108 DF1
DJ1 WIRE 109 DJ2
DK2 WIRE 110 DF2
DK1 WIRE 111 DH2
DL2 WIRE 112 DE2
DL1 WIRE 113 DL1
DM2 WIRE 114 DN1
DM1 WIRE 115 DP1
DN2 WIRE 116 DM1
DN1 WIRE 117 DP2
DP2 WIRE 118 DM2
DP1 WIRE 119 DN2
DR2 WIRE 120 DL2
DR1 WIRE 121 DR1
DS2 WIRE 122 DT2
DS1 WIRE 123 DJ1
DT2 WIRE 124 DS1
DJ1 WIRE 125 DV2
DU2 WIRE 126 DS2
DV1 WIRE 127 DU2
DV2 WIRE 128 DR2

ROM BRAID
G922
ABCDØ3

AC1 WIRE 1 AA1
AD1 WIRE 2 AB2
AE1 WIRE 3 AB1
AB1 WIRE 4 AD2
AE2 WIRE 5 AC1
AA1 WIRE 6 AE2
AD2 WIRE 7 AD1
AB2 WIRE 8 AF2
AF1 WIRE 9 AF1
AJ1 WIRE 10 AH2
AK1 WIRE 11 AH1
AH1 WIRE 12 AJ2
AK2 WIRE 13 AJ1
AH2 WIRE 14 AK2
AJ2 WIRE 15 AK1
AF2 WIRE 16 AL2
AM1 WIRE 17 AL1
AP1 WIRE 18 AM2
AR1 WIRE 19 AM1
AN1 WIRE 20 AN2
AR2 WIRE 21 AN1
AN2 WIRE 22 AP2
AP2 WIRE 23 AP1
AM2 WIRE 24 AR2
AS1 WIRE 25 AR1
AU1 WIRE 26 AS2
AV1 WIRE 27 AS1
AT1 WIRE 28 AT2
AV2 WIRE 29 AU1
AT2 WIRE 30 AU2
AU2 WIRE 31 AV1
AS2 WIRE 32 AV2
BA1 WIRE 33 BB1
BC1 WIRE 34 BB2
BD1 WIRE 35 BC1
BB1 WIRE 36 BD2
BB2 WIRE 37 BD1
BC2 WIRE 38 BE2
BA2 WIRE 39 BE1
BE1 WIRE 40 BF2
BF2 WIRE 41 BF1
BH2 WIRE 42 BH2
BH1 WIRE 43 BH1
BJ1 WIRE 44 BJ2
BF1 WIRE 45 BJ1
BJ2 WIRE 46 BK2
BF2 WIRE 47 BK1
BH2 WIRE 48 BL2
BE2 WIRE 49 BL1
BM1 WIRE 50 BM2
BP1 WIRE 51 BM1
BR1 WIRE 52 BN2
BN1 WIRE 53 BN1
BR2 WIRE 54 BP2
BN2 WIRE 55 BP1
BP2 WIRE 56 BR2
BM2 WIRE 57 BR1
BS1 WIRE 58 BS2
BU1 WIRE 59 BS1
BV1 WIRE 60 BT2
BV2 WIRE 61 BU1
BT2 WIRE 62 BU2
BU2 WIRE 63 BV1
BS2 WIRE 64 BV2
DV1 COMMON AE1

ROM SELECTION
G924
ABCDØ1

AL2
MEM GO H
AL1
ENABLE MEM 4 H

BK2 PCI (1) Ø2 H
CK2 PCI (1) Ø3 H
BL2 PCI (1) Ø4 H
CK1 PCI (1) Ø5 H
DK1 PCI (1) Ø6 H
DK2 PCI (1) Ø7 H
CL2 PCI (1) Ø8 H

BL1 MEM DONE L
BK1 STROBE 4 H
PAUSE (1) H
BV1
BU1

ROM
A22
G923
ABCDØ4

AE1 MBS ØØ L
AJ1 MBS Ø1 L
BH1 MBS Ø2 L
BF1 MBS Ø3 L
AR1 MBS Ø4 L
AS1 MBS Ø5 L
BD1 MBS Ø6 L
BE1 MBS Ø7 L
BN1 MBS Ø8 L
BM1 MBS Ø9 L
AF1 MBS 1Ø L
AK1 MBS 11 L

BP1
BS1
BR1
PCI Ø9 (1) H
PCI 11 (1) H
PCI 1Ø (1) H

4TH MEMORY OPTION (MR14) INSTALLED

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP-14		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —/—
FINISH —/—

DRN. A. Ramos DATE 7-1-69
CHK'D. [illegible] DATE 7-23-69
ENG. J. Packett DATE 7-23-69
PROJ. ENG. [illegible] DATE 7-22-69
PROD. [illegible] DATE 10/27/69
NEXT HIGHER ASSY A-ML-MR14-Ø
SCALE NONE
SHEET 4 OF 4

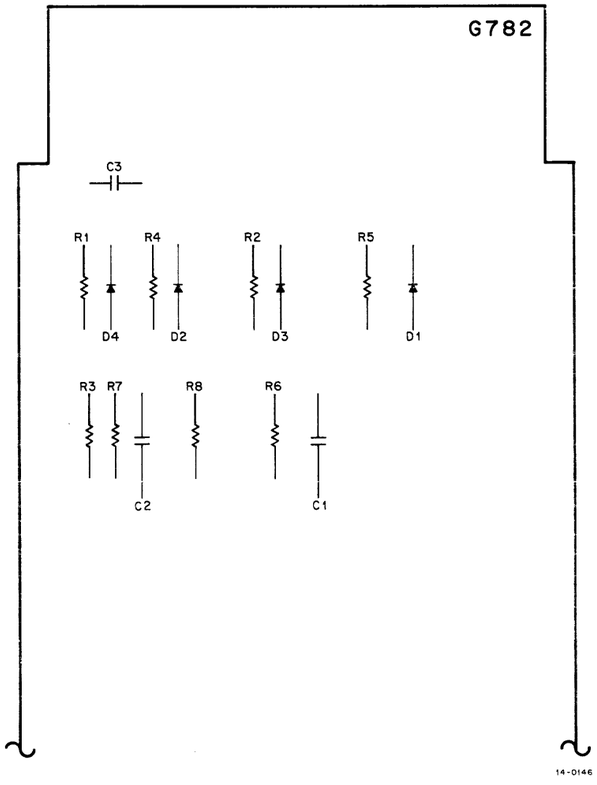
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

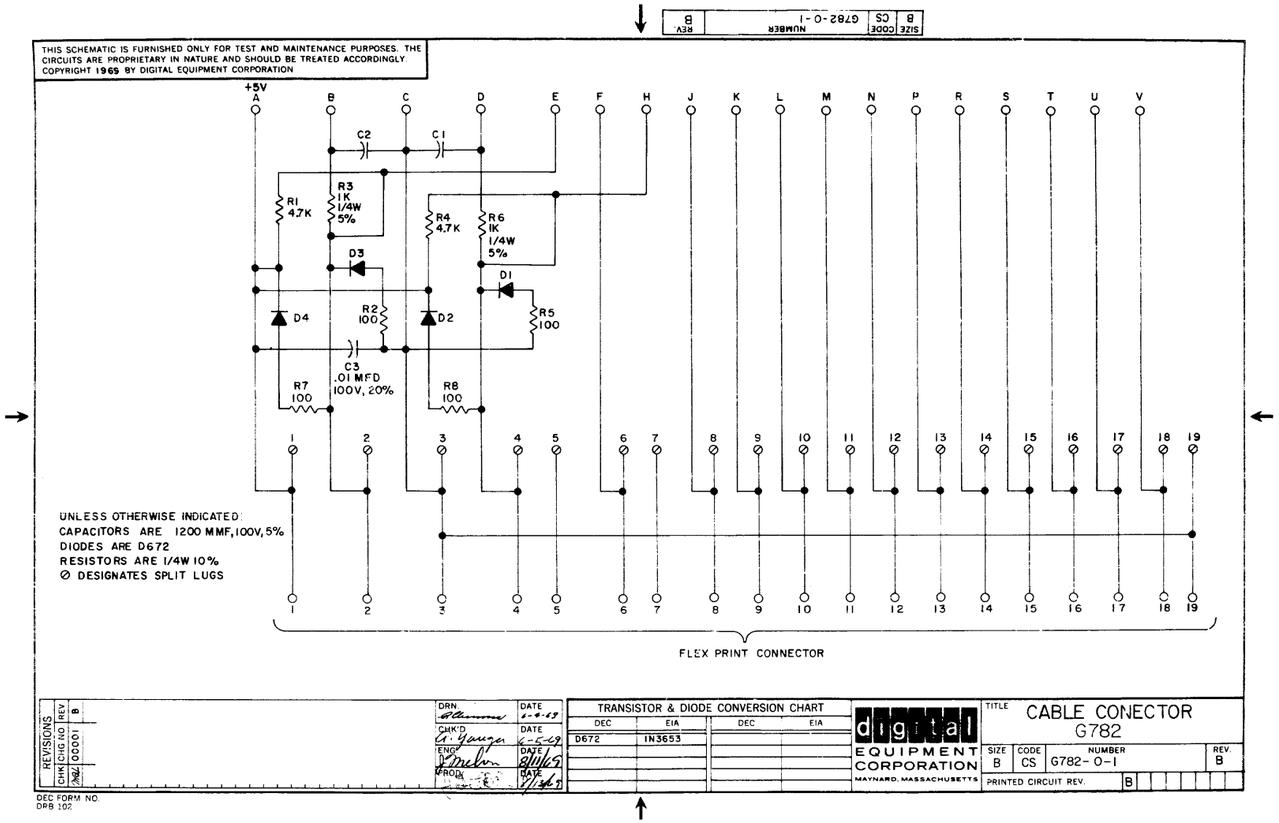
TITLE
MEMORY (1K)
(OPTIONAL ADDRESSES 6ØØØ-7777)

SIZE D | CODE BS | NUMBER MR14-Ø-2 | REV.
DIST.

REVISIONS | REV. | CHANGE NO | CHK

DEC FORM NO DRD 102A


G782
C3
R1
R4
R2
R5
D4
D2
D3
D1
R3
R7
R8
R6
C2
C1
14-0146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+5V
R1 4.7K
R3 1K 1/4W 5%
R4 4.7K
R6 1K 1/4W 5%
R2 100
R5 100
C3 .01 MFD 100V, 20%
R7 100
R8 100
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 1200 MMF, 100V, 5%
DIODES ARE D672
RESISTORS ARE 1/4W 10%
Ø DESIGNATES SPLIT LUGS
FLEX PRINT CONNECTOR
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
D672
IN3653
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
CABLE CONECTOR
G782
SIZE B
CODE CS
NUMBER G782-0-1
REV. B
PRINTED CIRCUIT REV. B
REVISIONS
DEC FORM NO. DPB 102

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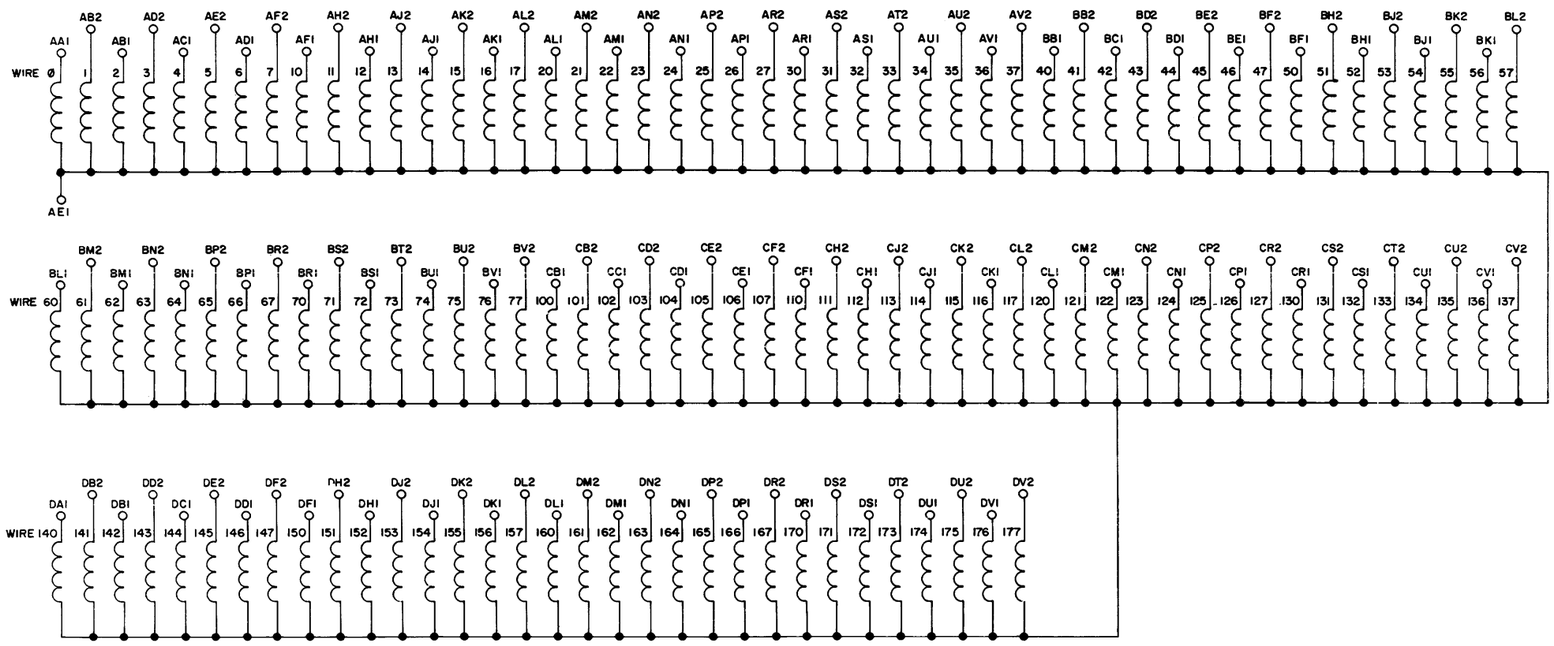


UNLESS OTHERWISE INDICATED:
COMPONENTS TO BE INSTALLED BY BRAID MANUFACTURERS

REVISIONS

CHK	CHG NO	REV
BUTLER	1	A

DRN. BUTLER	DATE 9-3-69	
CHK'D G. Yourek	DATE 9-8-69	
ENG. D. Wetzel	DATE 9-10-69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

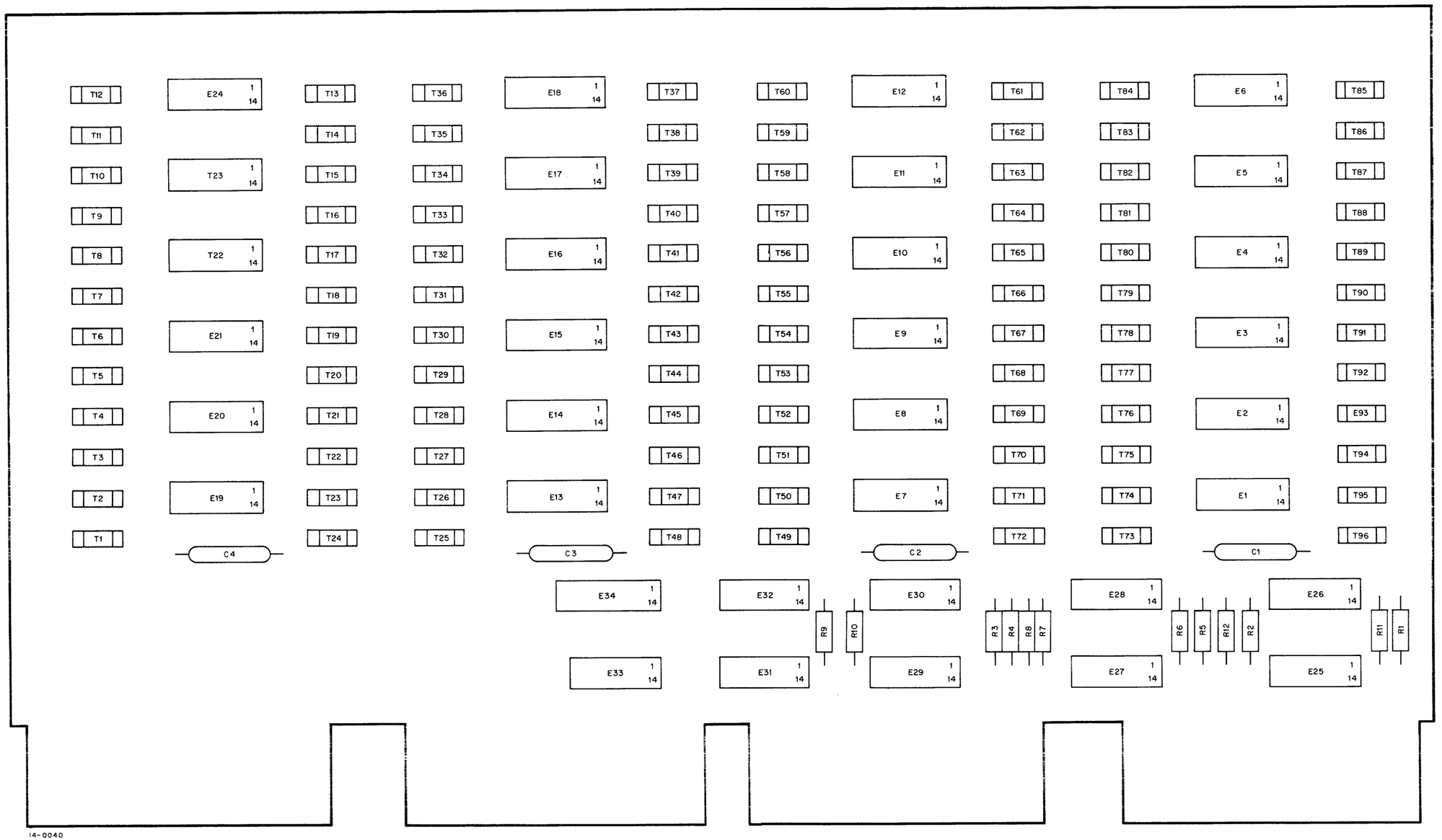
TITLE ROM BRAID BOARD G922

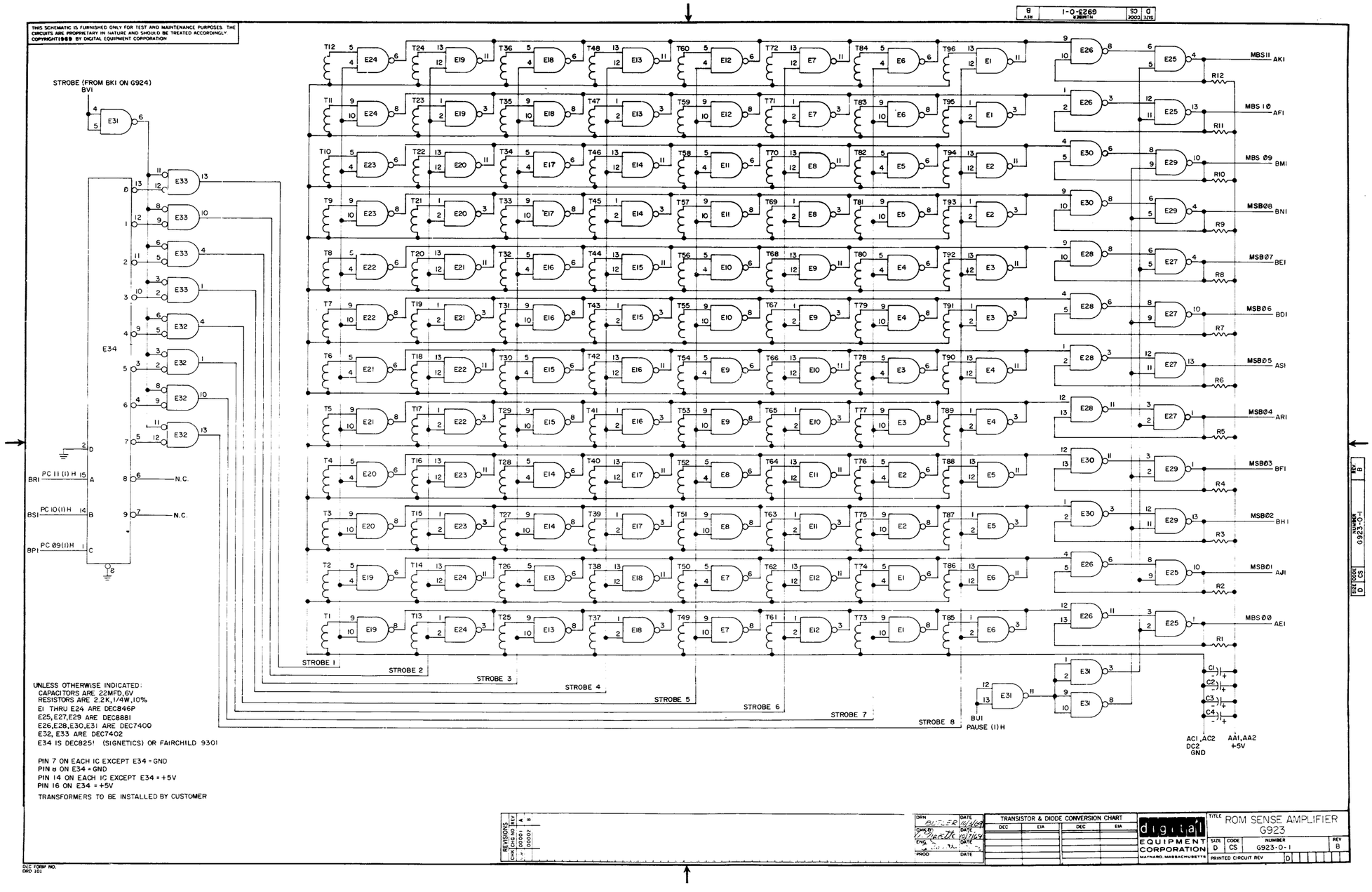
SIZE	CODE	NUMBER	REV.
C	CS	G922-0-1	A

PRINTED CIRCUIT REV. B

SIZE	CODE	NUMBER	REV.
C	CS	G922-0-1	A

DEC FORM NO.
DRC 102


T12
T11
T10
T9
T8
T7
T6
T5
T4
T3
T2
T1
E24 1 14
T23 1 14
T22 1 14
E21 1 14
E20 1 14
E19 1 14
C4
T13
T14
T15
T16
T17
T18
T19
T20
T21
T22
T23
T24
T36
T35
T34
T33
T32
T31
T30
T29
T28
T27
T26
T25
E18 1 14
E17 1 14
E16 1 14
E15 1 14
E14 1 14
E13 1 14
C3
T37
T38
T39
T40
T41
T42
T43
T44
T45
T46
T47
T48
T60
T59
T58
T57
T56
T55
T54
T53
T52
T51
T50
T49
E12 1 14
E11 1 14
E10 1 14
E9 1 14
E8 1 14
E7 1 14
C2
T61
T62
T63
T64
T65
T66
T67
T68
T69
T70
T71
T72
T84
T83
T82
T81
T80
T79
T78
T77
T76
T75
T74
T73
E6 1 14
E5 1 14
E4 1 14
E3 1 14
E2 1 14
E1 1 14
C1
T85
T86
T87
T88
T89
T90
T91
T92
E93
T94
T95
T96
E34 1 14
E33 1 14
E32 1 14
E31 1 14
E30 1 14
E29 1 14
E28 1 14
E27 1 14
E26 1 14
E25 1 14
R9
R10
R3
R4
R8
R7
R6
R5
R12
R2
R11
R1
14-0040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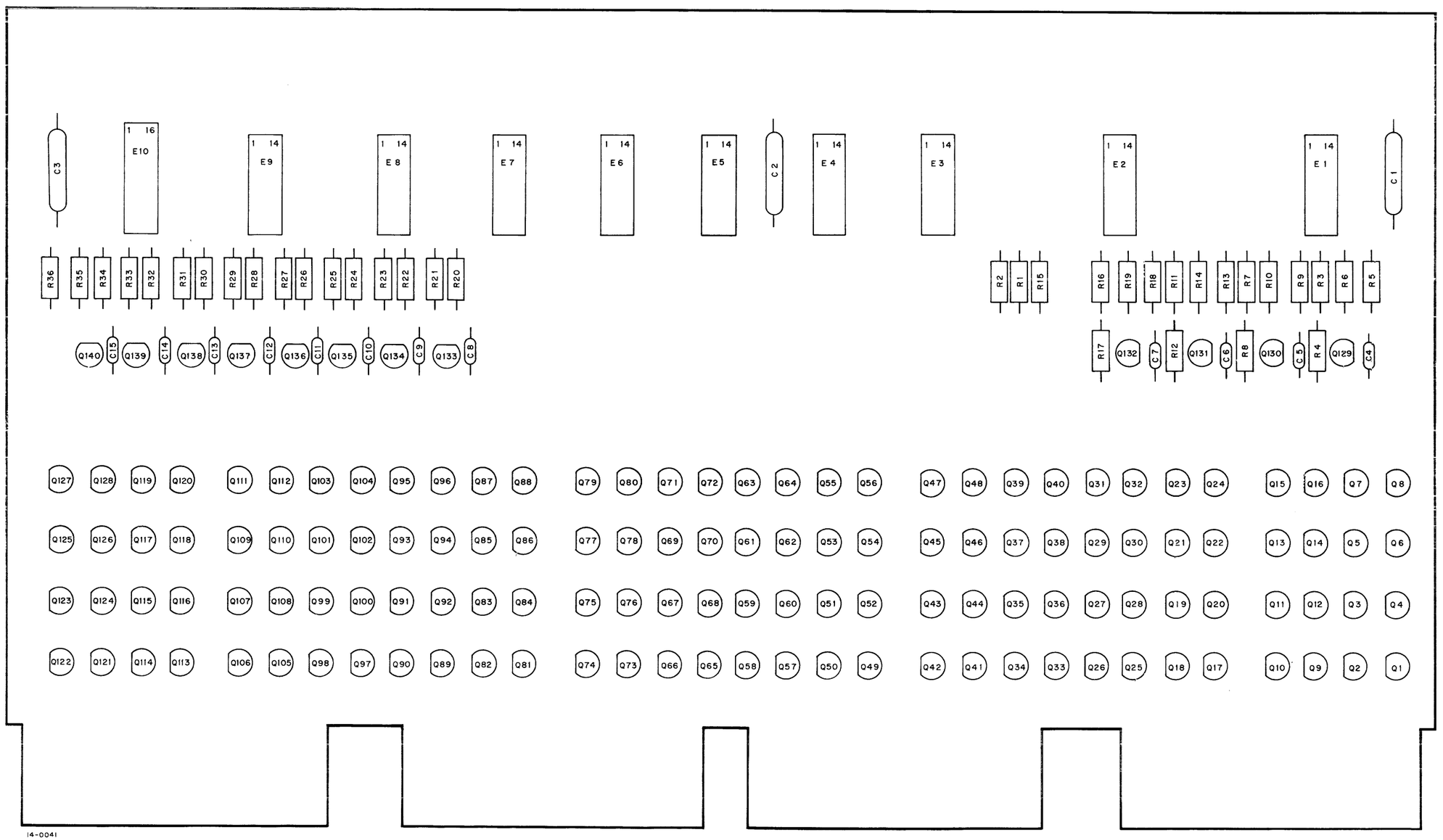
STROBE (FROM BK1 ON G924)
BV1
E34
BR1 PC 11 (1) H
BS1 PC 10 (1) H
BP1 PC 09 (1) H
N.C.
STROBE 1
STROBE 2
STROBE 3
STROBE 4
STROBE 5
STROBE 6
STROBE 7
STROBE 8
BU1
PAUSE (1) H
MBS11 AK1
MBS 10 AF1
MBS 09 BM1
MSB08 BN1
MSB07 BE1
MSB06 BD1
MSB05 AS1
MSB04 AR1
MSB03 BF1
MSB02 BH1
MSB01 AJ1
MBS00 AE1
AC1, AC2
DC2
GND
AA1, AA2
+5V
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 22MFD, 6V
RESISTORS ARE 2.2K, 1/4W, 10%
E1 THRU E24 ARE DEC846P
E25, E27, E29 ARE DEC8881
E26, E28, E30, E31 ARE DEC7400
E32, E33 ARE DEC7402
E34 IS DEC825! (SIGNETICS) OR FAIRCHILD 9301
PIN 7 ON EACH IC EXCEPT E34 = GND
PIN 8 ON E34 = GND
PIN 14 ON EACH IC EXCEPT E34 = +5V
PIN 16 ON E34 = +5V
TRANSFORMERS TO BE INSTALLED BY CUSTOMER
REVISIONS
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE ROM SENSE AMPLIFIER G923
SIZE D
CODE CS
NUMBER G923-0-1
REV B
PRINTED CIRCUIT REV D
DEC FORM NO. DRO 101


C3
E10
E9
E8
E7
E6
E5
C2
E4
E3
E2
E1
C1
R36 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 R25 R24 R23 R22 R21 R20
R2 R1 R15
R16 R19 R18 R11 R14 R13 R7 R10 R9 R3 R6 R5
Q140 C15 Q139 C14 Q138 C13 Q137 C12 Q136 C11 Q135 C10 Q134 C9 Q133 C8
R17 Q132 C7 R12 Q131 C6 R8 Q130 C5 R4 Q129 C4
Q127 Q128 Q119 Q120 Q111 Q112 Q103 Q104 Q95 Q96 Q87 Q88 Q79 Q80 Q71 Q72 Q63 Q64 Q55 Q56 Q47 Q48 Q39 Q40 Q31 Q32 Q23 Q24 Q15 Q16 Q7 Q8
Q125 Q126 Q117 Q118 Q109 Q110 Q101 Q102 Q93 Q94 Q85 Q86 Q77 Q78 Q69 Q70 Q61 Q62 Q53 Q54 Q45 Q46 Q37 Q38 Q29 Q30 Q21 Q22 Q13 Q14 Q5 Q6
Q123 Q124 Q115 Q116 Q107 Q108 Q99 Q100 Q91 Q92 Q83 Q84 Q75 Q76 Q67 Q68 Q59 Q60 Q51 Q52 Q43 Q44 Q35 Q36 Q27 Q28 Q19 Q20 Q11 Q12 Q3 Q4
Q122 Q121 Q114 Q113 Q106 Q105 Q98 Q97 Q90 Q89 Q82 Q81 Q74 Q73 Q66 Q65 Q58 Q57 Q50 Q49 Q42 Q41 Q34 Q33 Q26 Q25 Q18 Q17 Q10 Q9 Q2 Q1
14-0041

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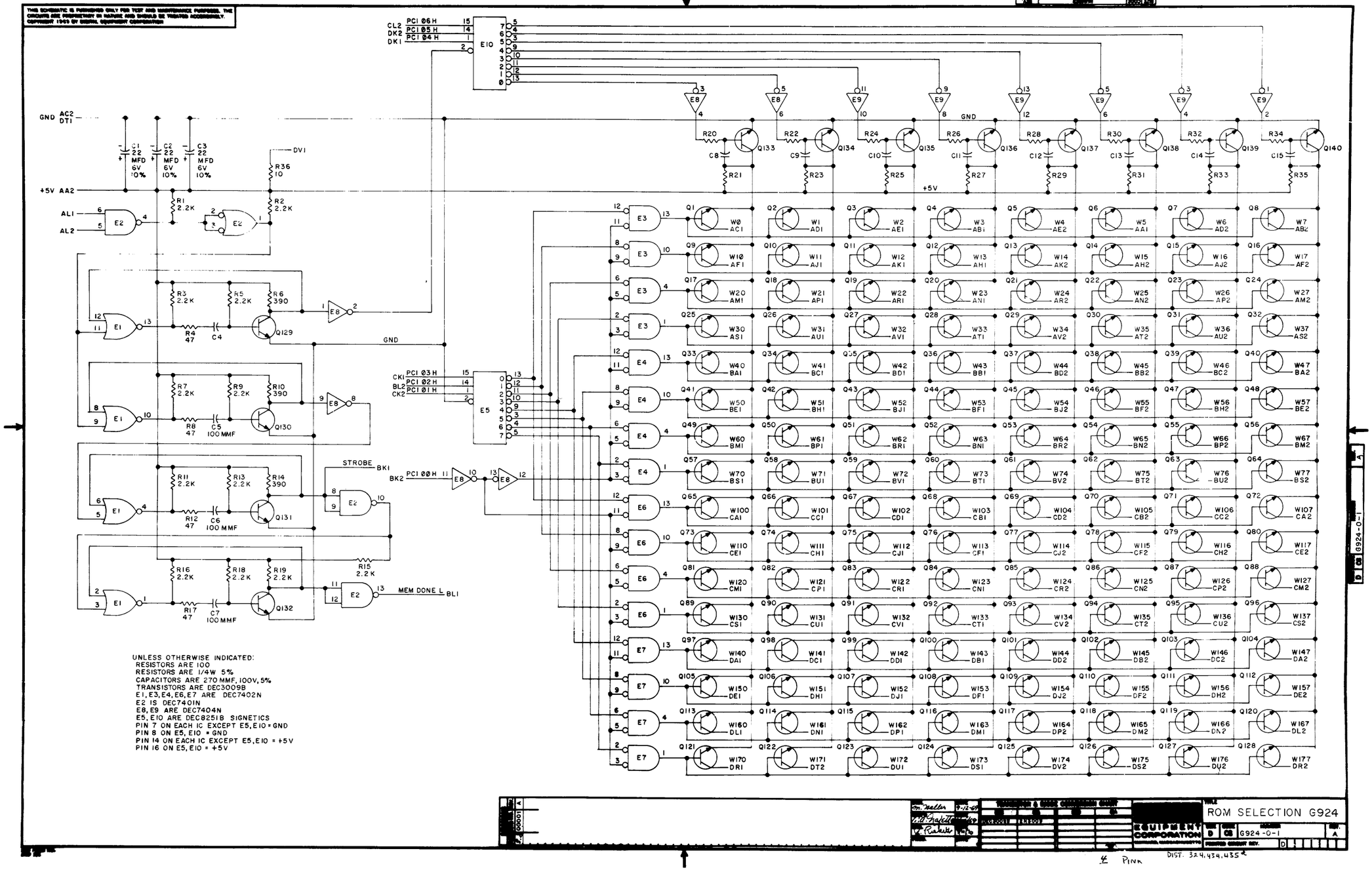
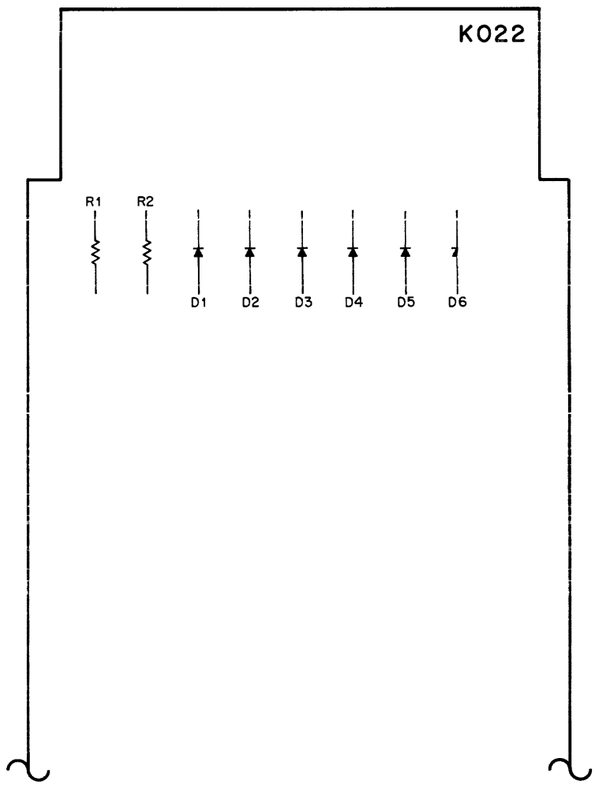
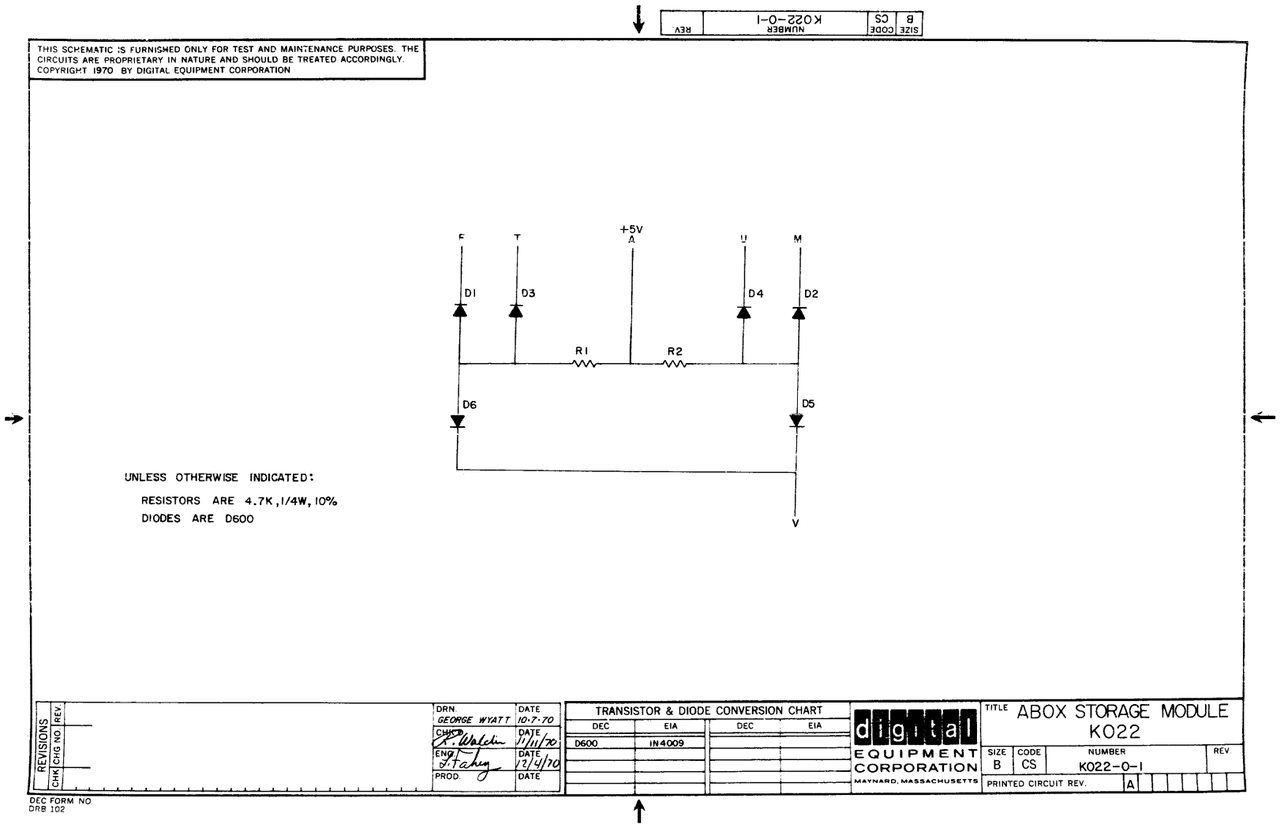


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 10Ω
RESISTORS ARE 1/4W 5%
CAPACITORS ARE 270 MMF, 100V, 5%
TRANSISTORS ARE DEC3009B
E1, E3, E4, E6, E7 ARE DEC7402N
E2 IS DEC7401N
E8, E9 ARE DEC7404N
E5, E10 ARE DEC8251B SIGNETICS
PIN 7 ON EACH IC EXCEPT E5, E10 = GND
PIN 8 ON E5, E10 = GND
PIN 14 ON EACH IC EXCEPT E5, E10 = +5V
PIN 16 ON E5, E10 = +5V

K022


K022
R1
R2
D1
D2
D3
D4
D5
D6
14-0147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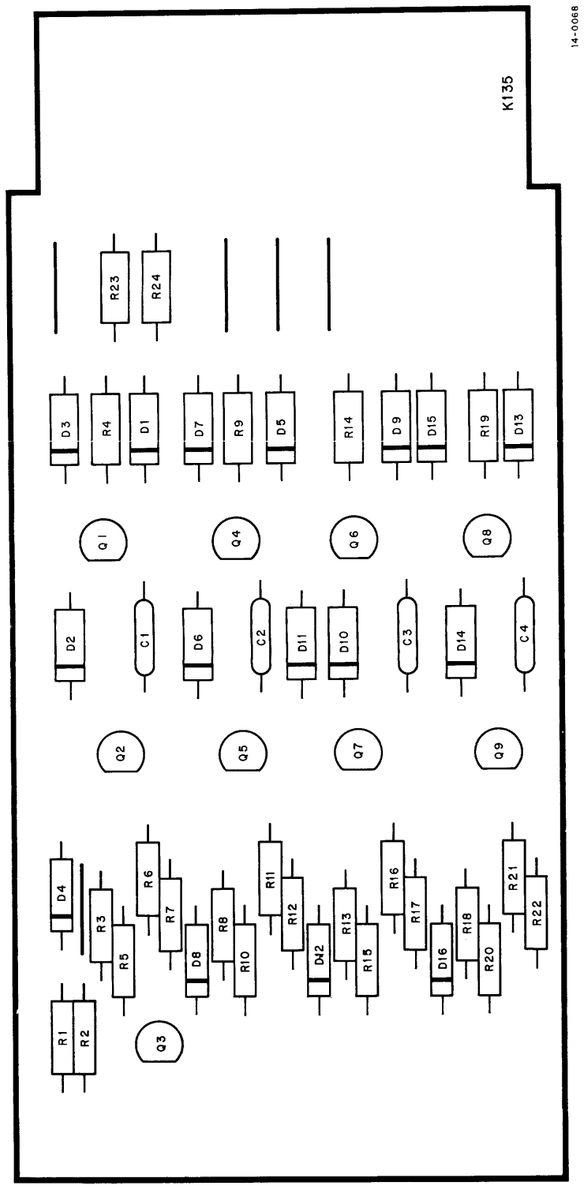
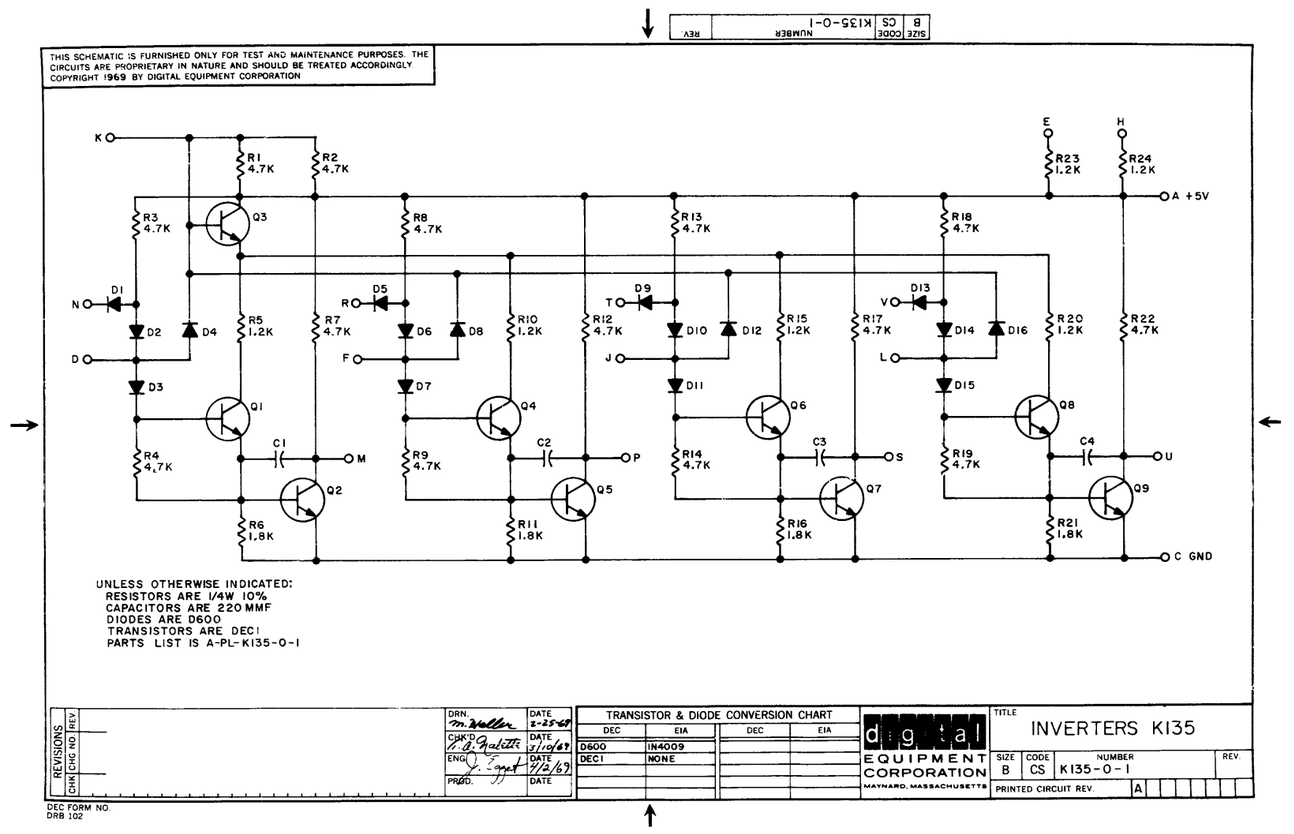
+5V
D1
D3
D4
D2
R1
R2
D6
D5
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 4.7K, 1/4W, 10%
DIODES ARE D600
REVISIONS
DRN. GEORGE WYATT
DATE 10-7-70
DATE 11/11/70
DATE 12/4/70
PROD.
DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
D600
IN4009
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE ABOX STORAGE MODULE K022
SIZE B
CODE CS
NUMBER K022-0-1
REV.
PRINTED CIRCUIT REV. A
DEC FORM NO. DRB 102


K135
14-0068
R23
R24
D3
R4
D1
D7
R9
D5
R14
D9
D15
R19
D13
Q1
Q4
Q6
Q8
D2
C1
D6
C2
D11
D10
C3
D14
C4
Q2
Q5
Q7
Q9
D4
R3
R5
R6
R7
D8
R8
R10
R11
R12
D12
R13
R15
R16
R17
D16
R18
R20
R21
R22
R1
R2
Q3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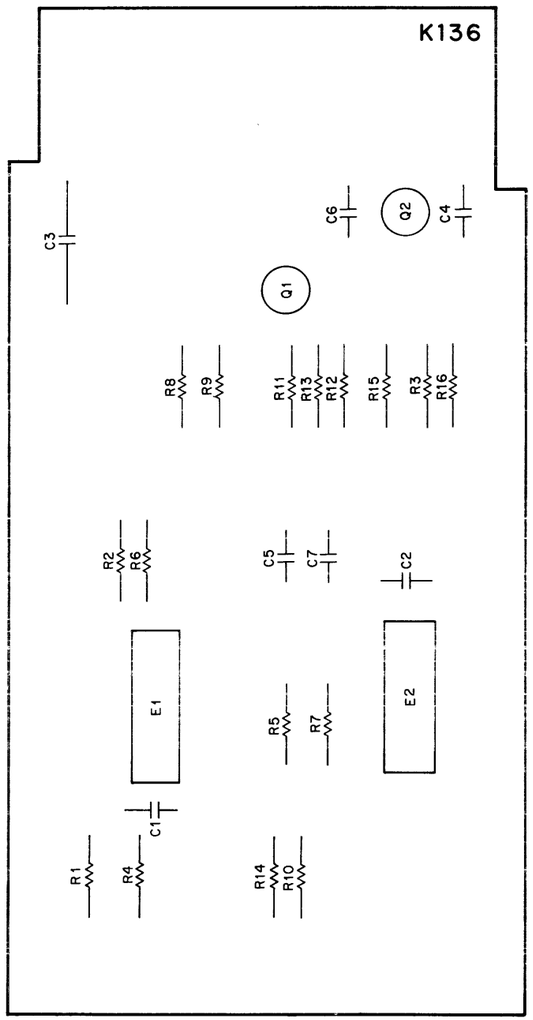
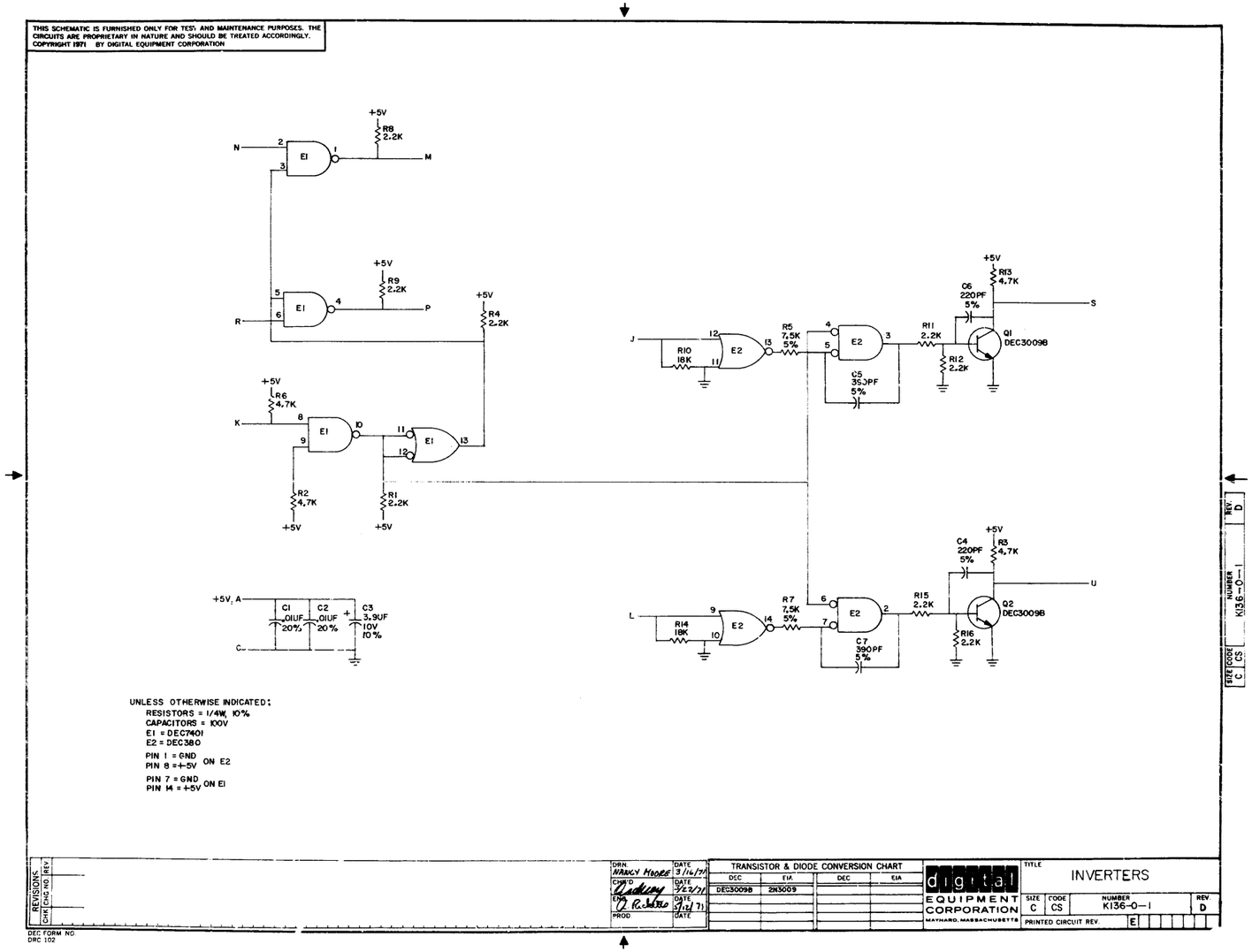
A +5V
C GND
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W 10%
CAPACITORS ARE 220 MMF
DIODES ARE D600
TRANSISTORS ARE DEC1
PARTS LIST IS A-PL-K135-0-1
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
D600
IN4009
DEC1
NONE
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
INVERTERS K135
SIZE B
CODE CS
NUMBER K135-0-1
REV.
PRINTED CIRCUIT REV. A
REVISIONS
DEC FORM NO. DRB 102


K136
14-0148
C3
C6
Q2
C4
Q1
R8
R9
R11
R13
R12
R15
R3
R16
R2
R6
C5
C7
C2
E1
E2
R5
R7
C1
R1
R4
R14
R10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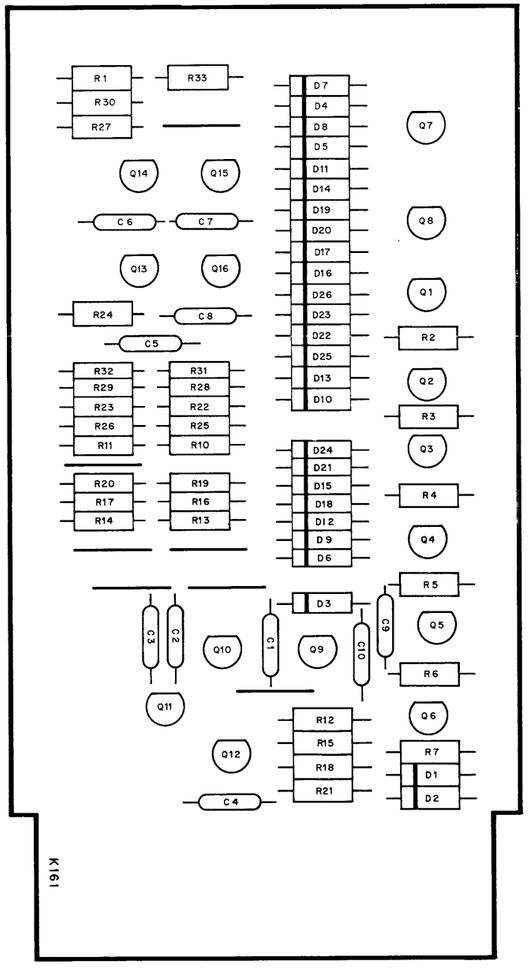
UNLESS OTHERWISE INDICATED:
RESISTORS = 1/4W, 10%
CAPACITORS = 100V
E1 = DEC7401
E2 = DEC380
PIN 1 = GND
PIN 8 = +5V ON E2
PIN 7 = GND
PIN 14 = +5V ON E1
TRANSISTOR & DIODE CONVERSION CHART
DEC 3009B
2N3009
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
INVERTERS
K136-0-1
PRINTED CIRCUIT REV. E
DEC FORM NO. DRC 102



14-0071

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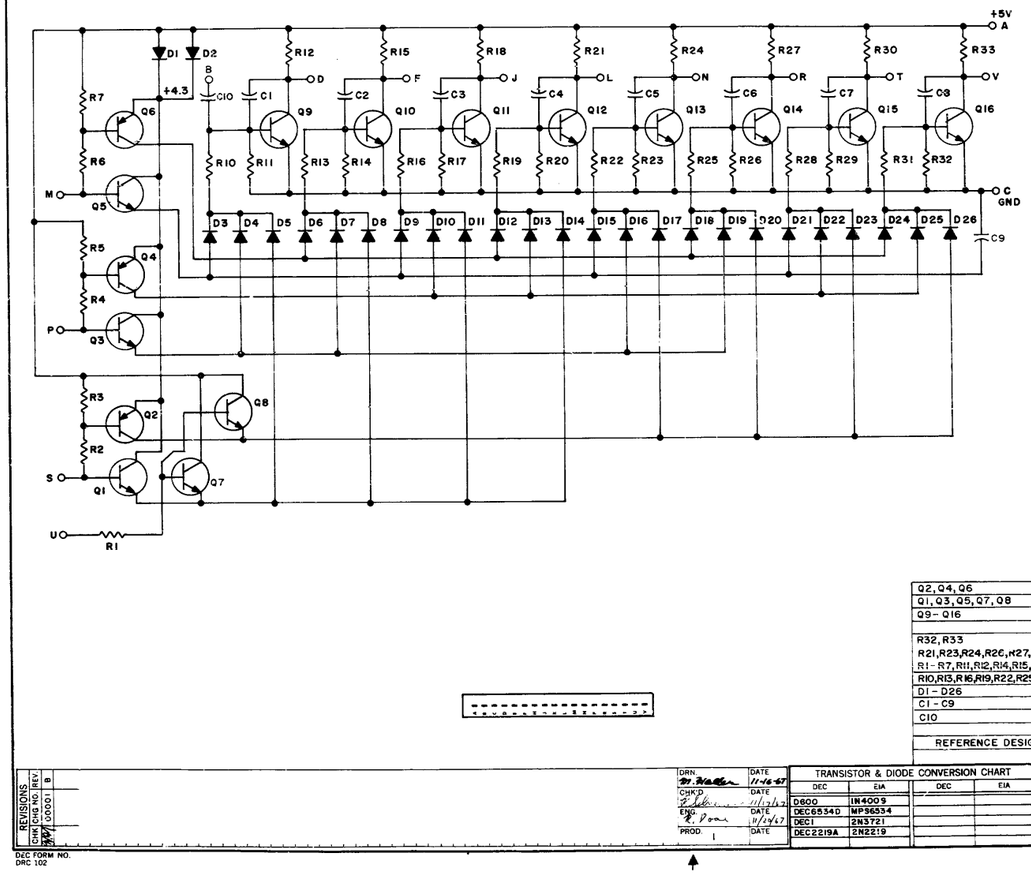


REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-K161-0-0
C10	CAP. .01 MFD 100V 20% DISC	1001610
C1 - C9	CAP. 680MMF 100V 5% D.M.	1000026
D1 - D26	DIODE D600	1105366
R10,R13,R16,R19,R22,R25,R28,R31	RES. 1.2K 1/4W 10% CC	1300386
R32,R33 R21,R23,R24,R26,R27,R29,R30, R1 - R7, R11,R12,R14,R15,R17,R18,R20,	RES. 1.8K 1/4W 10% CC	1301428
Q9 - Q16	TRANSISTOR DEC0001	1505369
Q1, Q3, Q5, Q7, Q8	TRANSISTOR DEC2219A	1501881
Q2, Q4, Q6	TRANSISTOR DEC6534D	1503409

REVISIONS	CHG NO.	REV.
CHK	00001	B

		DATE
DRN.	D. Wade	11-16-67
CHK'D		DATE
ENG.	R. Doan	11/29/67
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D600	IN4009		
DEC6534D	MPS6534		
DEC1	2N3721		
DEC2219A	2N2219		

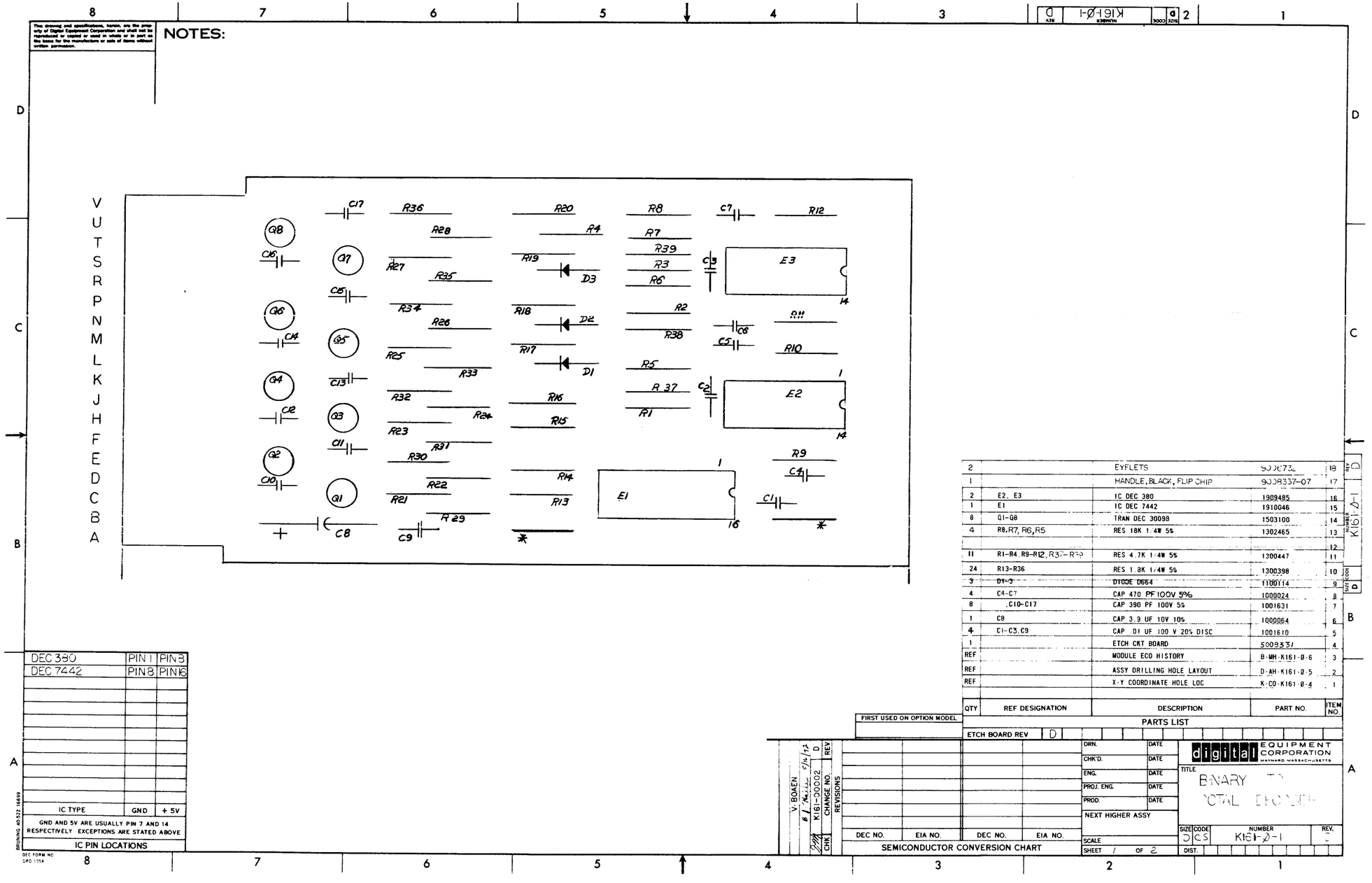
[redacted]
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: BINARY TO OCTAL DECODER K161

SIZE	CODE	NUMBER	REV.
C	CS	K161-0-1	B

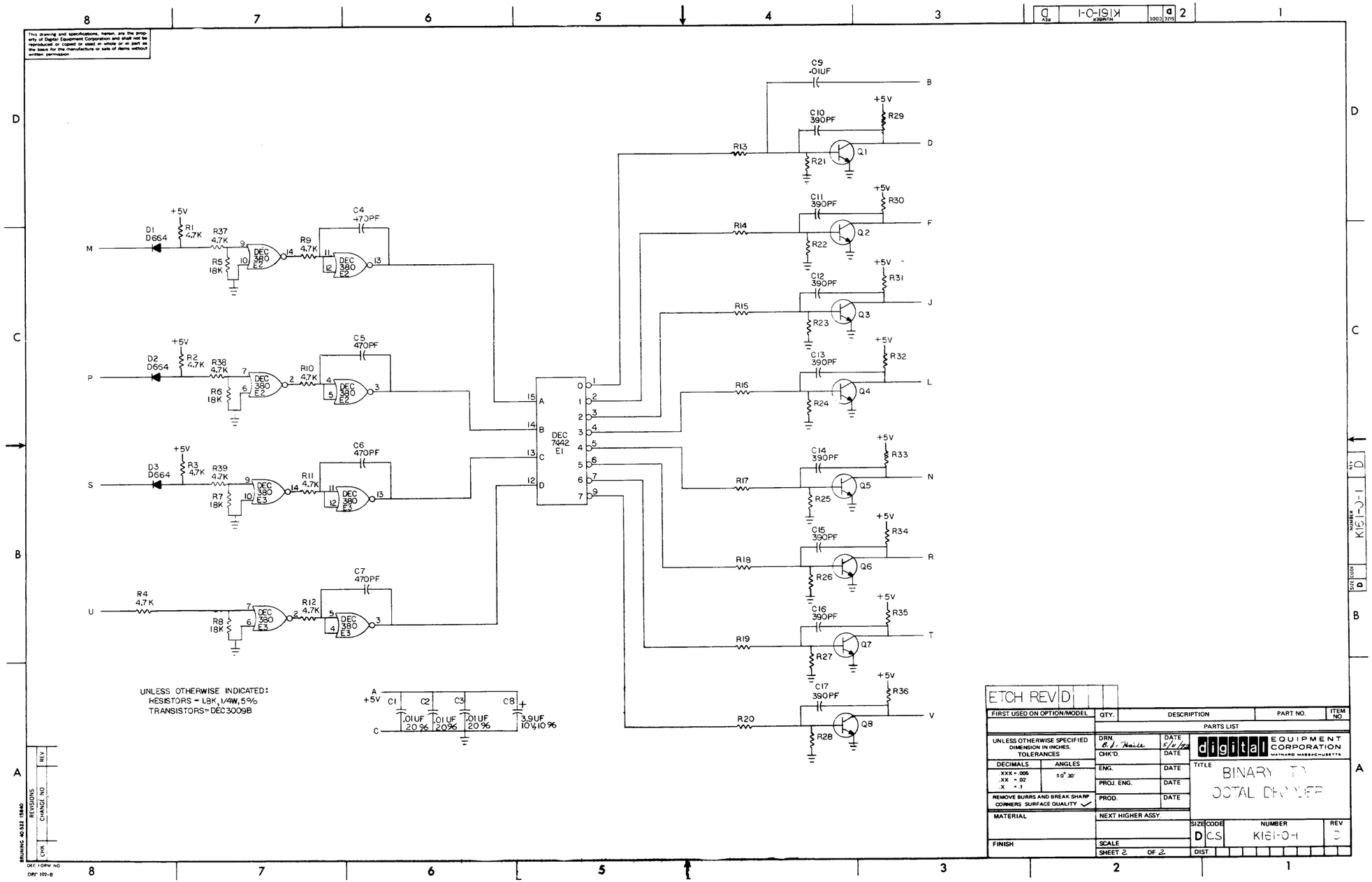
PRINTED CIRCUIT REV. C

DEC FORM NO. DRC 102



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
2		EYELETS	9006732	18
1		HANDLE, BLACK, FLIP CHIP	9008337-07	17
2	E2, E3	IC DEC 380	1909485	16
1	E1	IC DEC 7442	1910046	15
8	Q1-Q8	TRAN DEC 30098	1503100	14
4	R8,R7, R6,R5	RES 18K 1/4W 5%	1302465	13
				12
11	R1-R4, R9-R12, R37-R39	RES 4.7K 1/4W 5%	1300447	11
24	R13-R36	RES 1.8K 1/4W 5%	1300398	10
3	D1-3	DIODE D664	1100114	9
4	C4-C7	CAP 470 PF 100V 5%	1000024	8
8	C10-C17	CAP 390 PF 100V 5%	1001631	7
1	C8	CAP 3.9 UF 10V 10%	1000064	6
4	C1-C3, C9	CAP .01 UF 100 V 20% DISC	1001610	5
1		ETCH CKT BOARD	5008331	4
REF		MODULE ECO HISTORY	B-MH-K161-0-6	3
REF		ASSY DRILLING HOLE LAYOUT	D-AH-K161-0-5	2
REF		X-Y COORDINATE HOLE LOC	K-CO-K161-0-4	1

PARTS LIST



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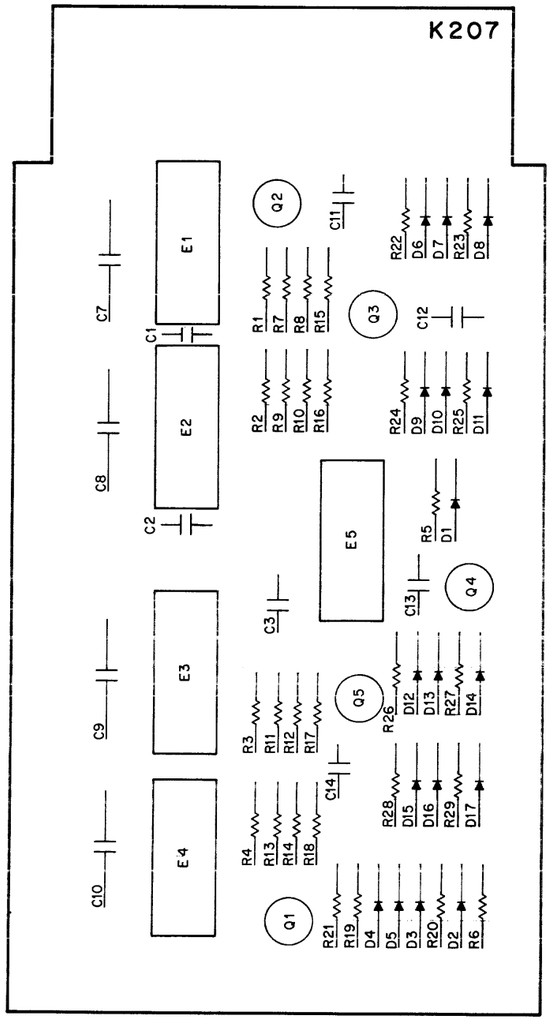
DEC 7442 E1
DEC 380 E2
DEC 380 E3
UNLESS OTHERWISE INDICATED:
RESISTORS = 1.8K, 1/4W, 5%
TRANSISTORS = DEC3009B
ETCH REV D
FIRST USED ON OPTION/MODEL
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS
ANGLES
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
NEXT HIGHER ASSY.
SCALE
SHEET 2 OF 2
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
BINARY TO OCTAL DECODER
SIZE D
CODE CS
NUMBER K161-0-1
REV D
DIST.
REVISIONS
CHANGE NO
REV
CHK
BRUNING 40-522 15840
DEC FORM NO
DPC 102-B


K207
14-0149
E1
E2
E3
E4
E5
Q1
Q2
Q3
Q4
Q5
C1
C2
C3
C7
C8
C9
C10
C11
C12
C13
C14
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
D1
D2
D3
D4
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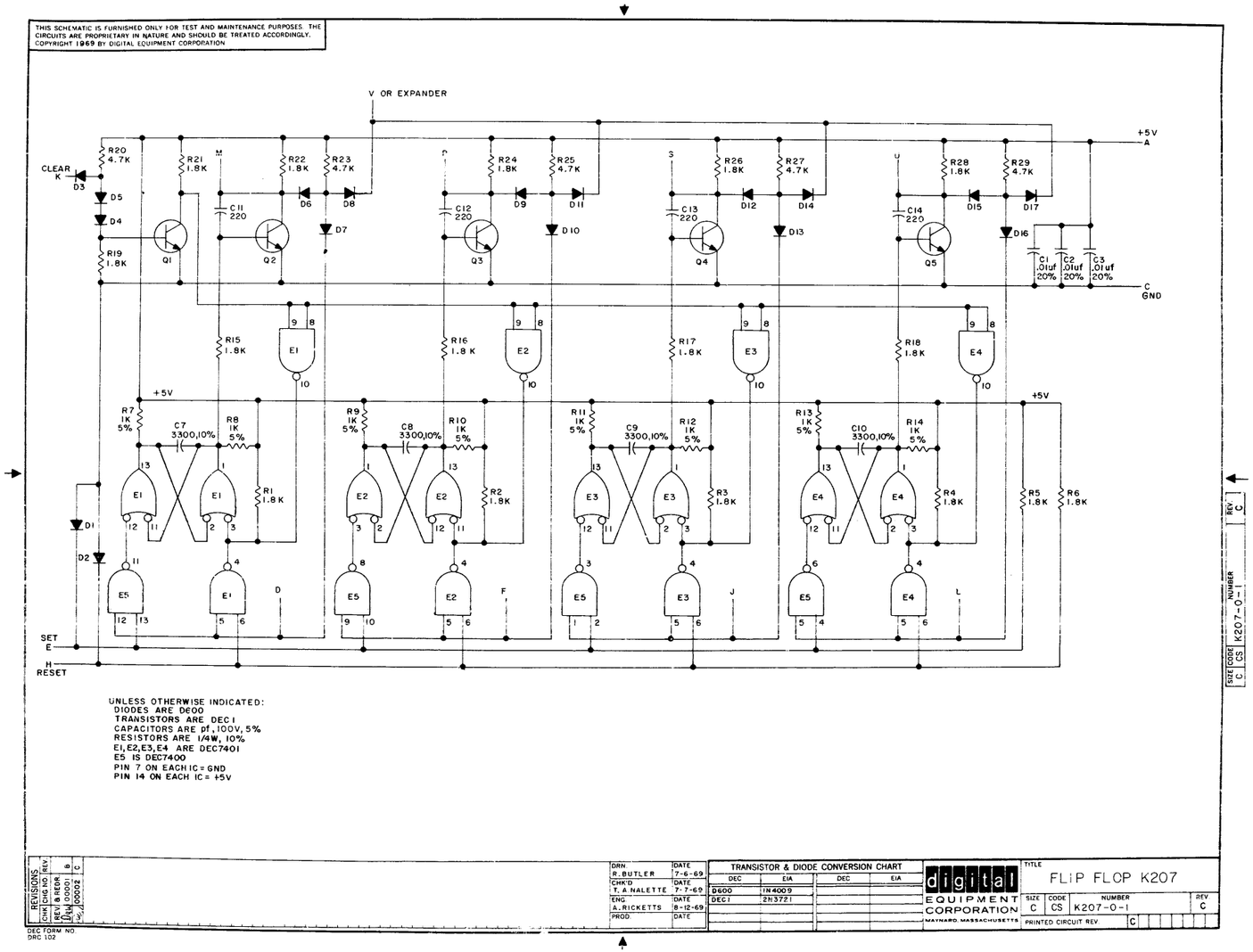
D12
D13
D14
D15
D16
D17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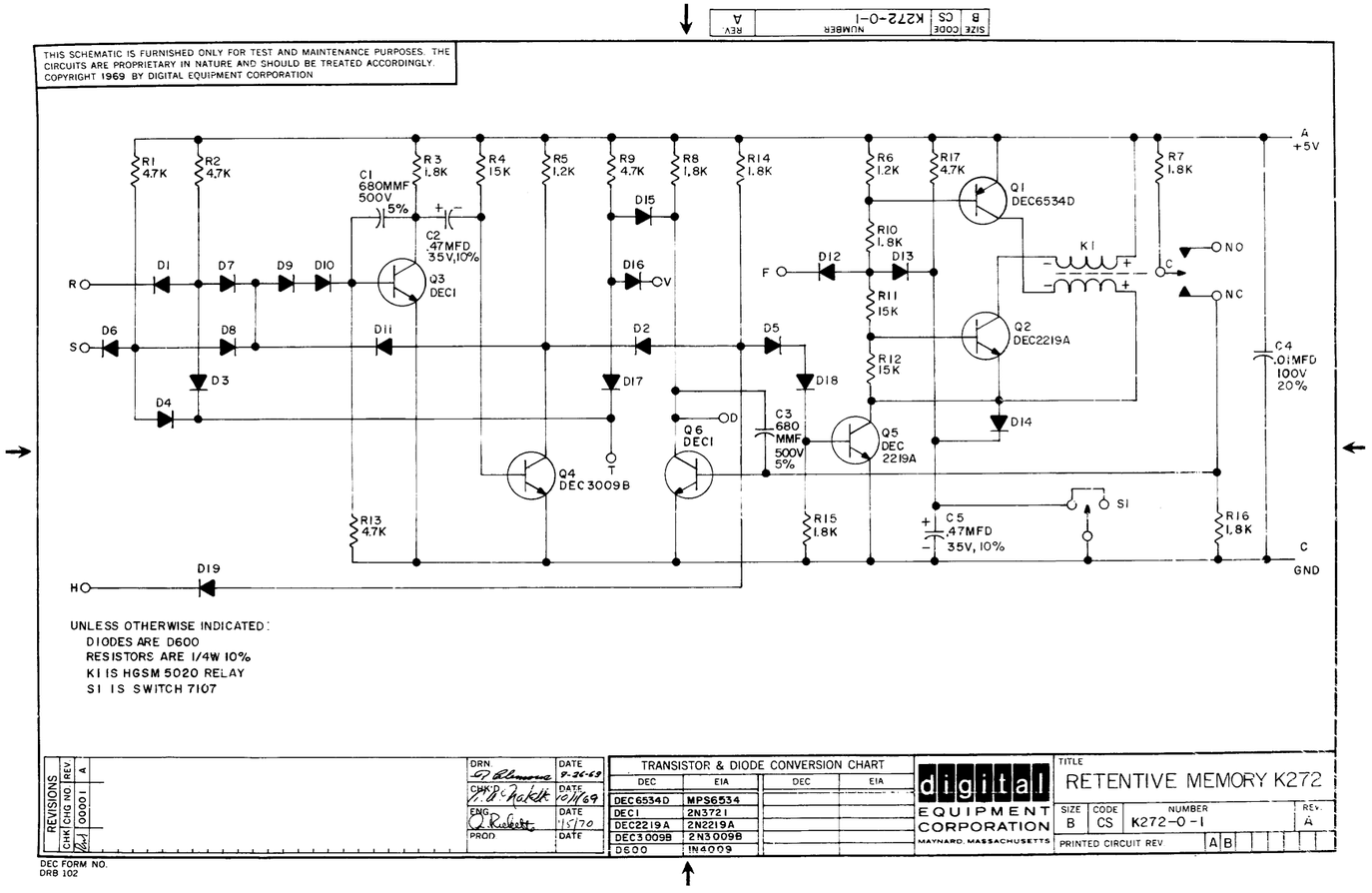
V OR EXPANDER
+5V A
C GND
CLEAR K
SET E
H RESET
+5V
UNLESS OTHERWISE INDICATED:
DIODES ARE DE00
TRANSISTORS ARE DEC1
CAPACITORS ARE pf, 100V, 5%
RESISTORS ARE 1/4W, 10%
E1,E2,E3,E4 ARE DEC7401
E5 IS DEC7400
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
REVISIONS
DRN R.BUTLER 7-6-69
CHK'D T. A NALETTE 7-7-69
ENG A. RICKETTS 8-12-69
PROD
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
D600 1N4009
DEC1 2N3721
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE FLIP FLOP K207
SIZE C CODE CS NUMBER K207-0-1 REV C
PRINTED CIRCUIT REV C
DEC FORM NO. DRC 102


SIZE B CODE CS NUMBER K272-0-1 REV A
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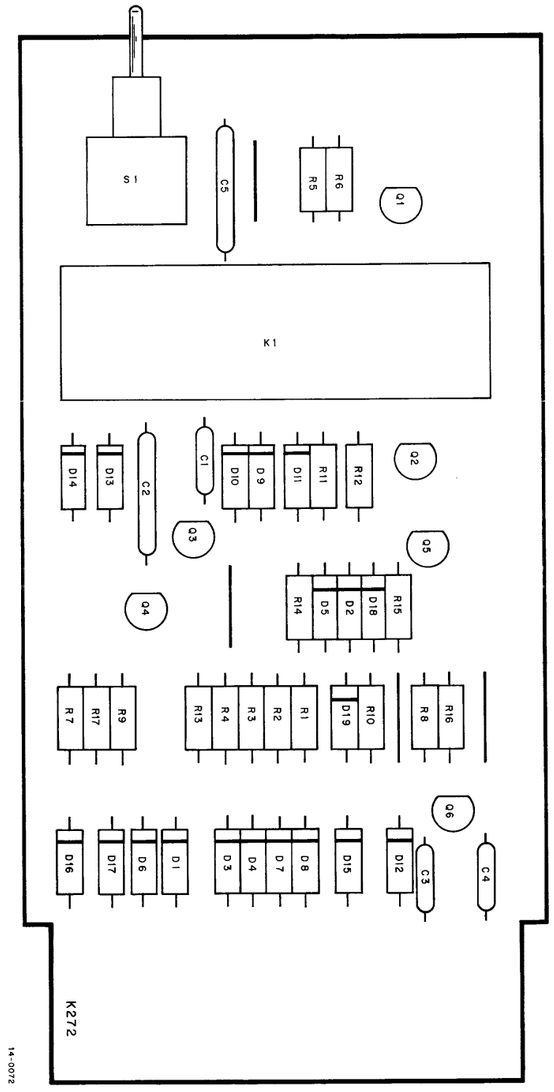
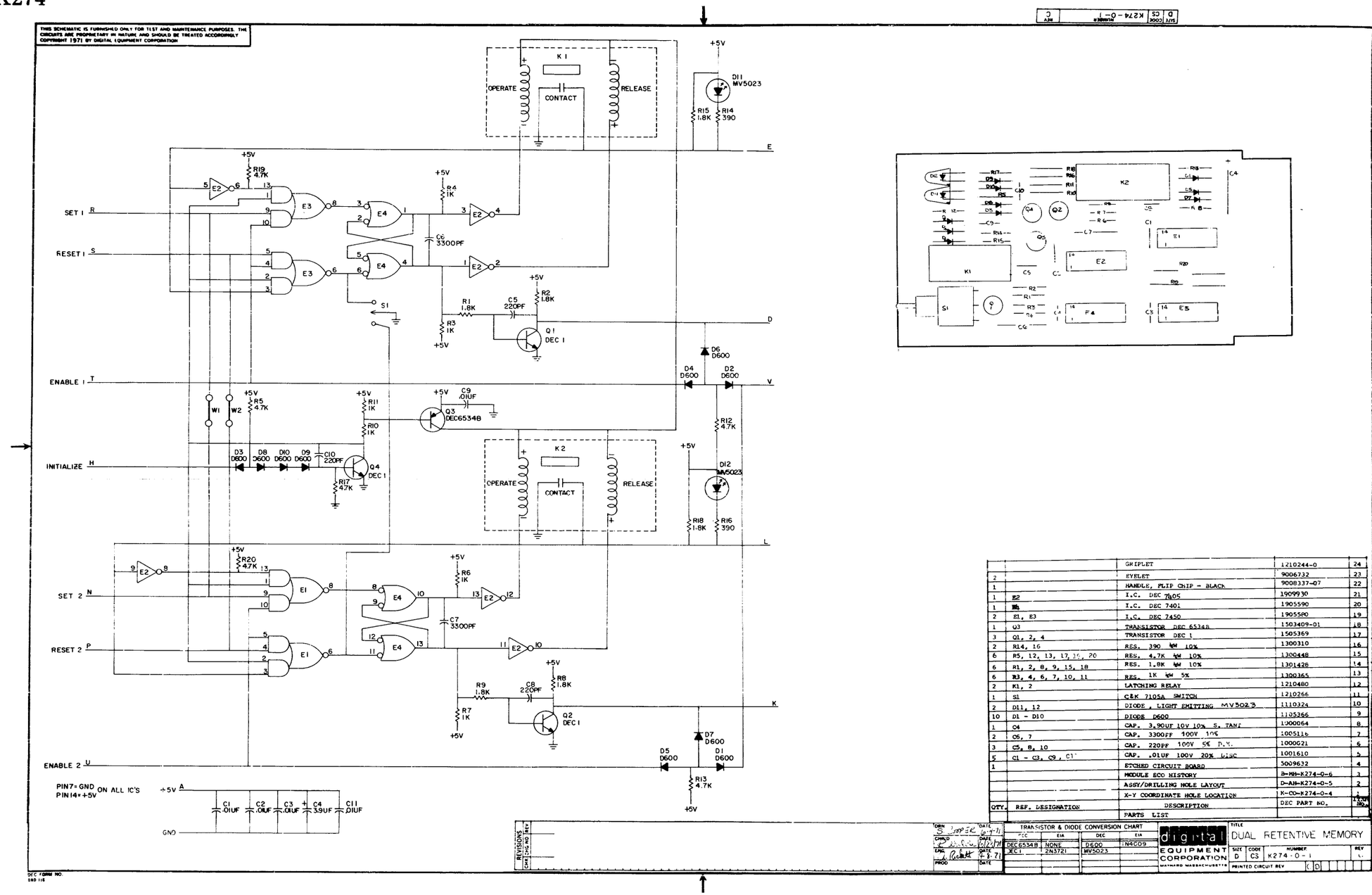
R1 4.7K
R2 4.7K
C1 680MMF 500V 5%
R3 1.8K
R4 15K
R5 1.2K
R9 4.7K
R8 1.8K
R14 1.8K
R6 1.2K
R17 4.7K
Q1 DEC6534D
R7 1.8K
A +5V
C2 .47MFD 35V,10%
D15
R10 1.8K
K1
NO
NC
C
R
D1
D7
D9
D10
Q3 DEC1
D16
0V
F
D12
D13
R11 15K
S
D6
D8
D11
D2
D5
Q2 DEC2219A
C4 .01MFD 100V 20%
D3
D17
D18
D4
Q6 DEC1
D
C3 680 MMF 500V 5%
Q5 DEC 2219A
D14
Q4 DEC3009B
T
S1
R13 4.7K
R15 1.8K
C5 .47MFD 35V, 10%
R16 1.8K
C GND
H
D19
UNLESS OTHERWISE INDICATED:
DIODES ARE D600
RESISTORS ARE 1/4W 10%
K1 IS HGSM 5020 RELAY
S1 IS SWITCH 7107
REVISIONS
CHK CHG NO. REV
A
DRN LJ Blanco DATE 9-26-69
CHK'D J.P. Jakkk DATE 10/1/69
ENG O.R. Cuskett DATE 1/5/70
PROD DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
DEC6534D MPS6534
DEC1 2N3721
DEC2219A 2N2219A
DEC3009B 2N3009B
D600 1N4009
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE RETENTIVE MEMORY K272
SIZE B CODE CS NUMBER K272-0-1 REV. A
PRINTED CIRCUIT REV A B
DEC FORM NO. DRB 102


S1
C5
R5
R6
Q1
K1
D14
D13
C2
C1
D10
D9
D11
R11
R12
Q2
Q3
Q5
Q4
R14
D5
D2
D18
R15
R7
R17
R9
R13
R4
R3
R2
R1
D19
R10
R8
R16
Q6
D16
D17
D6
D1
D3
D4
D7
D8
D15
D12
C3
C4
K272
14-0072

K274



QTY.	REF. DESIGNATION	DESCRIPTION	DEC PART NO.	ITEM NO.
		GRIPLET	1210244-0	24
2		EYELET	9006732	23
1		HANDLE, FLIP CHIP - BLACK	9008337-07	22
1	E2	I.C. DEC 7405	1909930	21
1	E1	I.C. DEC 7401	1905590	20
2	E1, E3	I.C. DEC 7450	1905580	19
1	Q3	TRANSISTOR DEC 6534B	1503409-01	18
3	Q1, 2, 4	TRANSISTOR DEC 1	1505369	17
2	R14, 16	RES. 390 ¼W 10%	1300310	16
6	R5, 12, 13, 17, 19, 20	RES. 4.7K ¼W 10%	1300448	15
6	R1, 2, 8, 9, 15, 18	RES. 1.8K ¼W 10%	1301428	14
6	R3, 4, 6, 7, 10, 11	RES. 1K ¼W 5%	1300365	13
2	K1, 2	LATCHING RELAY	1210480	12
1	S1	C&K 7105A SWITCH	1210266	11
2	D11, 12	DIODE, LIGHT EMITTING MV5023	1110324	10
10	D1 - D10	DIODE D600	1105366	9
1	C4	CAP. 3.90UF 10V 10% S. TANT	1000064	8
2	C6, 7	CAP. 3300PF 100V 10%	1005116	7
3	C5, 8, 10	CAP. 220PF 100V 5% D.M.	1000021	6
5	C1 - C3, C9, C11	CAP. .01UF 100V 20% DISC	1001610	5
1		ETCHED CIRCUIT BOARD	5009632	4
		MODULE ECO HISTORY	B-MH-K274-0-6	3
		ASSY/DRILLING HOLE LAYOUT	D-AH-K274-0-5	2
		X-Y COORDINATE HOLE LOCATION	K-CO-K274-0-4	1
		PARTS LIST		

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC6534B	NONE	D600	1N4009
DEC1	2N3721	MV5023	

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: DUAL RETENTIVE MEMORY

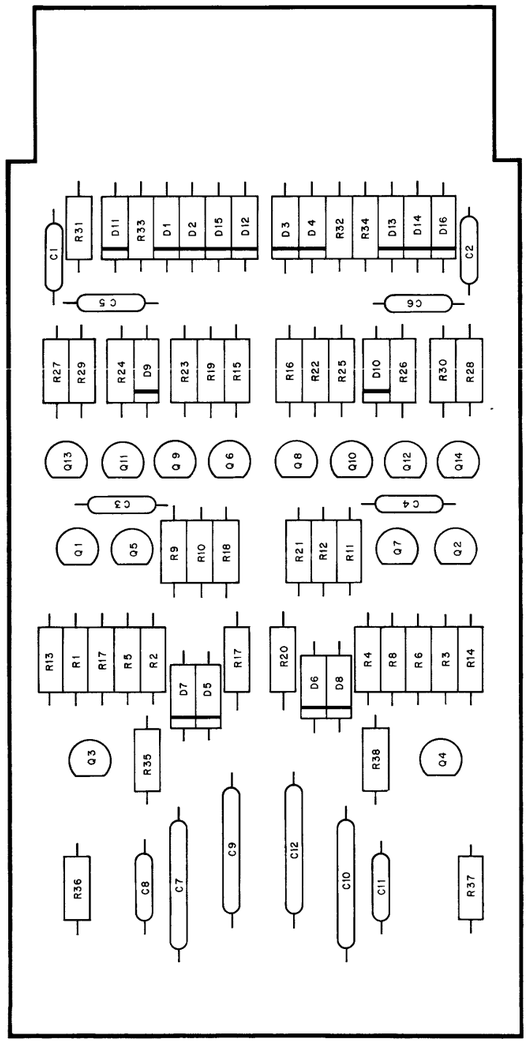
SIZE D | CODE CS | NUMBER K274-0-1 | REV C

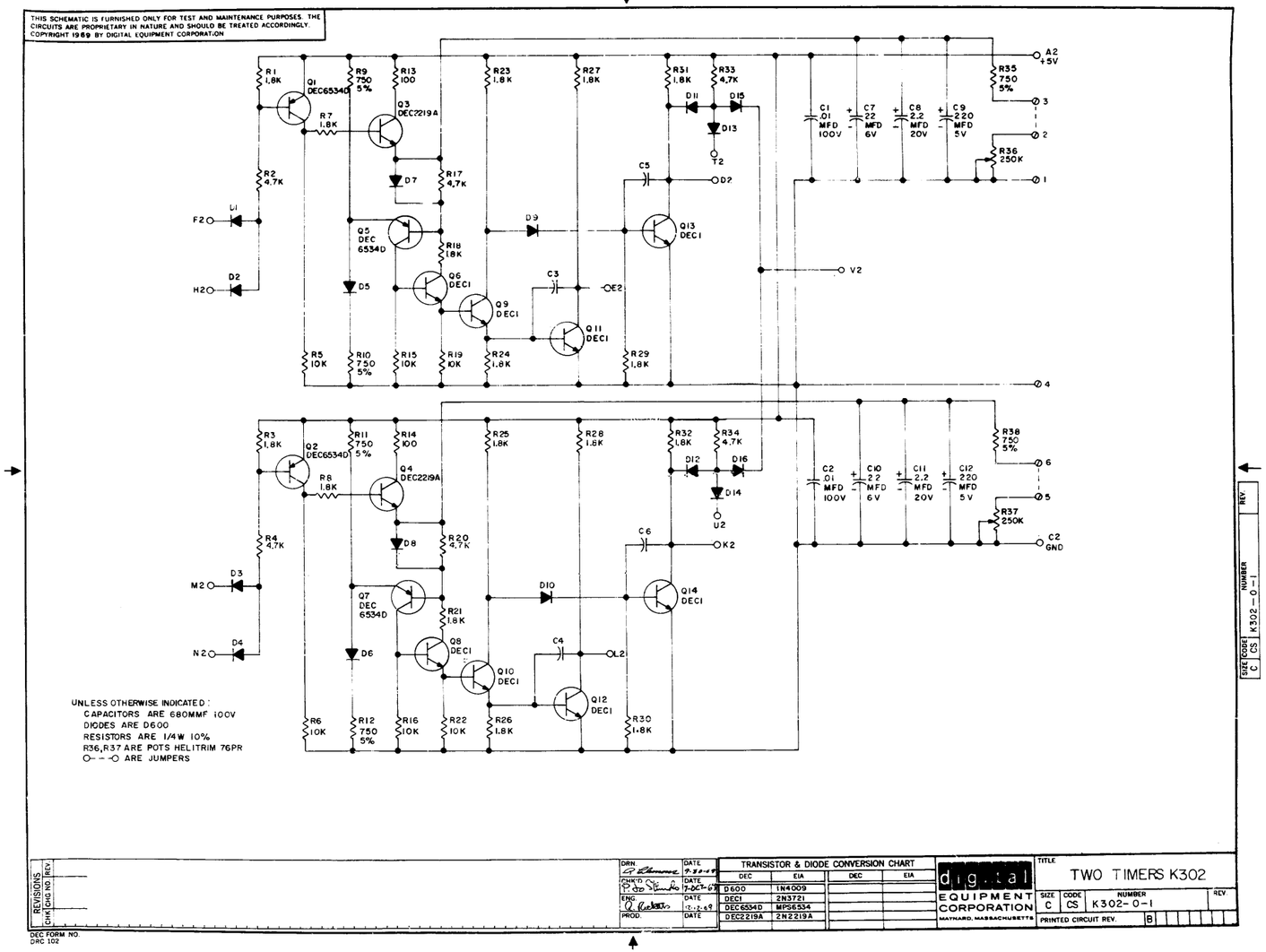
PRINTED CIRCUIT REV C D

DRN S. Cooper DATE 6-9-71
CHKD DATE 6/23/71
ENG DATE 4-8-71
PROD DATE

REVISIONS: CHK | CHG NO | REV

DEC FORM NO. DRD 116


14-0063
C1
R31
D11
R33
D1
D2
D15
D12
D3
D4
R32
R34
D13
D14
D16
C2
C5
C6
R27
R29
R24
D9
R23
R19
R15
R16
R22
R25
D10
R26
R30
R28
Q13
Q11
Q9
Q6
Q8
Q10
Q12
Q14
C3
C4
Q1
Q5
R9
R10
R18
R21
R12
R11
Q7
Q2
R13
R1
R17
R5
R2
D7
D5
R17
R20
D6
D8
R4
R8
R6
R3
R14
Q3
R35
R38
Q4
R36
C8
C7
C9
C12
C10
C11
R37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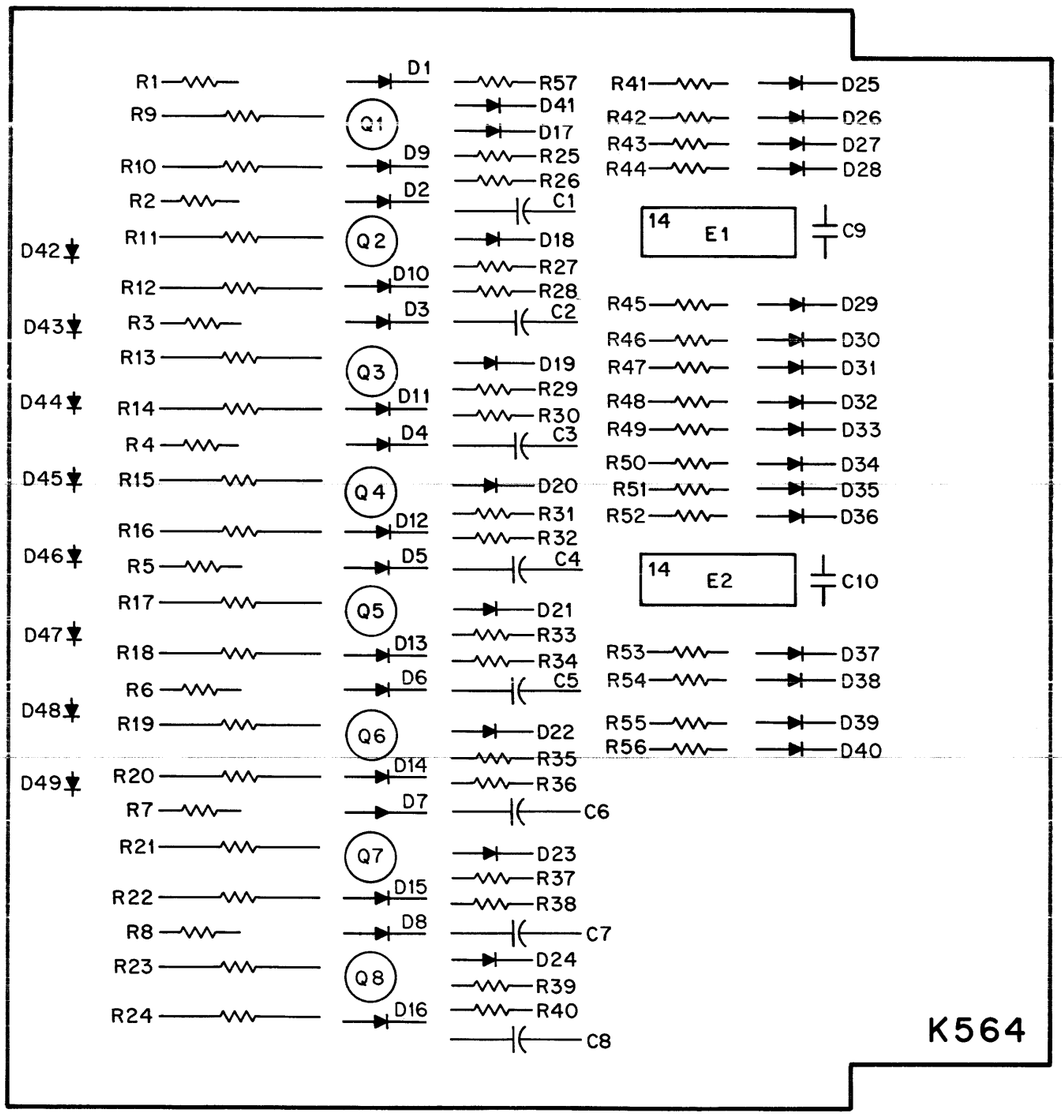
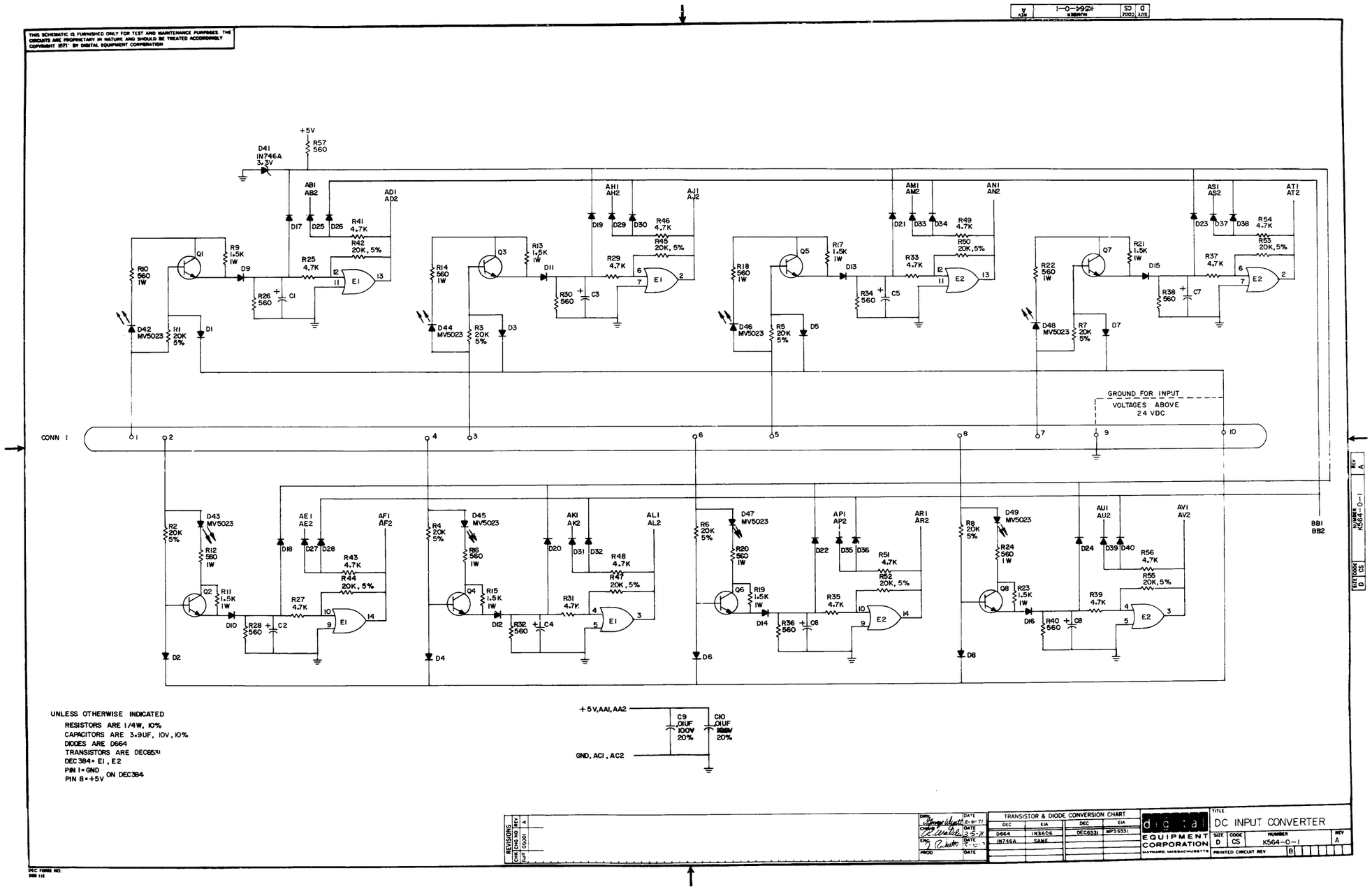
COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION
Q1 DEC6534D
Q3 DEC2219A
Q5 DEC 6534D
Q6 DEC1
Q9 DEC1
Q11 DEC1
Q13 DEC1
Q2 DEC6534D
Q4 DEC2219A
Q7 DEC 6534D
Q8 DEC1
Q10 DEC1
Q12 DEC1
Q14 DEC1
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16
R1 1.8K
R2 4.7K
R3 1.8K
R4 4.7K
R5 10K
R6 10K
R7 1.8K
R8 1.8K
R9 750 5%
R10 750 5%
R11 750 5%
R12 750 5%
R13 100
R14 100
R15 10K
R16 10K
R17 4.7K
R18 1.8K
R19 10K
R20 4.7K
R21 1.8K
R22 10K
R23 1.8K
R24 1.8K
R25 1.8K
R26 1.8K
R27 1.8K
R28 1.8K
R29 1.8K
R30 1.8K
R31 1.8K
R32 1.8K
R33 4.7K
R34 4.7K
R35 750 5%
R36 250K
R37 250K
R38 750 5%
C1 .01 MFD 100V
C2 .01 MFD 100V
C3
C5
C6
C7 22 MFD 6V
C8 2.2 MFD 20V
C9 220 MFD 5V
C10 22 MFD 6V
C11 2.2 MFD 20V
C12 220 MFD 5V
F2
H2
M2
N2
L1
L2
K2
T2
U2
A2 +5V
V2
C2 GND
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 680MMF 100V
DIODES ARE D600
RESISTORS ARE 1/4W 10%
R36,R37 ARE POTS HELITRIM 76PR
O--O ARE JUMPERS
REVISIONS
DRN
CHK'D
ENG.
PROD.
DATE
DEC FORM NO. DRC 102
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
D600 1N4009
DEC1 2N3721
DEC6534D MPS6534
DEC2219A 2N2219A
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
TWO TIMERS K302
SIZE C
CODE CS
NUMBER K302-0-1
REV.
PRINTED CIRCUIT REV. B
SIZE CODE C CS NUMBER K302-0-1 REV


R1
R9
R10
R2
R11
D42
R12
R3
D43
R13
R14
D44
R4
R15
D45
R16
R5
D46
R17
R18
D47
R6
R19
D48
R20
R7
D49
R21
R22
R8
R23
R24
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
D1
D9
D2
D10
D3
D11
D4
D12
D5
D13
D6
D14
D7
D15
D8
D16
R57
D41
D17
R25
R26
C1
D18
R27
R28
C2
D19
R29
R30
C3
D20
R31
R32
C4
D21
R33
R34
C5
D22
R35
R36
C6
D23
R37
R38
C7
D24
R39
R40
C8
R41
R42
R43
R44
D25
D26
D27
D28
14
E1
C9
R45
R46
R47
R48
R49
R50
R51
R52
D29
D30
D31
D32
D33
D34
D35
D36
14
E2
C10
R53
R54
R55
R56
D37
D38
D39
D40
K564

14-0150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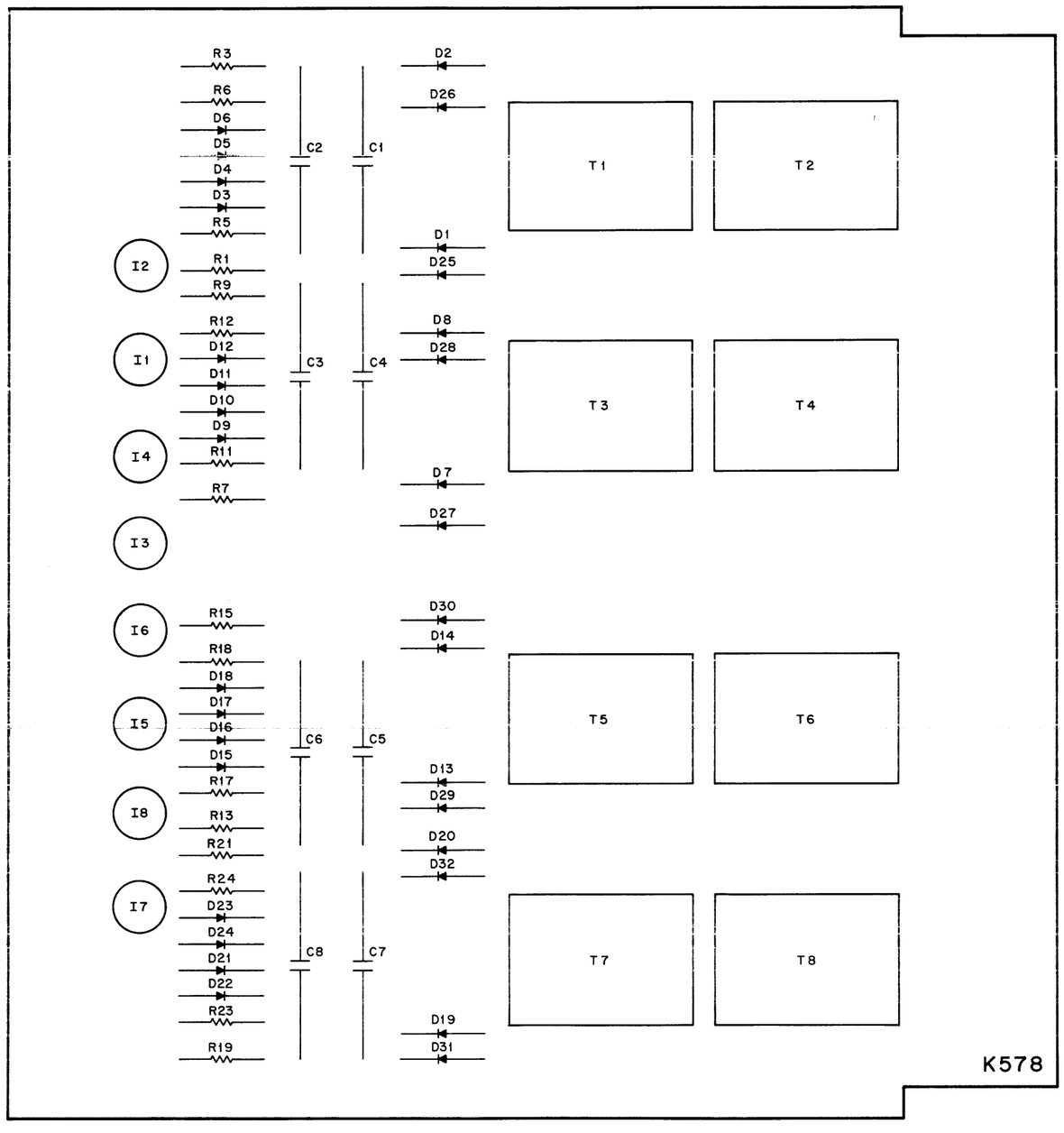
COPYRIGHT 1971 BY DIGITAL EQUIPMENT CORPORATION
+5V
R57 560
D41 IN746A 3.3V
CONN 1
GROUND FOR INPUT VOLTAGES ABOVE 24 VDC
BB1 BB2
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE 3.9UF, 10V, 10%
DIODES ARE D664
TRANSISTORS ARE DEC6531
DEC384 = E1, E2
PIN 1 = GND
PIN 8 = +5V ON DEC384
+5V, AA1, AA2
GND, AC1, AC2
C9 .01UF 100V 20%
C10 .01UF 20%
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
D664 IN3606 DEC6531 MPS6531
IN746A SAME
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE DC INPUT CONVERTER
SIZE D CODE CS NUMBER K564-0-1 REV A
PRINTED CIRCUIT REV B
REVISIONS
DEC FORM NO.


R3
R6
D6
D5
D4
D3
R5
R1
R9
R12
D12
D11
D10
D9
R11
R7
I2
I1
I4
I3
C2
C1
C3
C4
D2
D26
D1
D25
D8
D28
D7
D27
T1
T2
T3
T4
R15
R18
D18
D17
D16
D15
R17
R13
R21
R24
D23
D24
D21
D22
R23
R19
I6
I5
I8
I7
C6
C5
C8
C7
D30
D14
D13
D29
D20
D32
D19
D31
T5
T6
T7
T8
K578

14-0153

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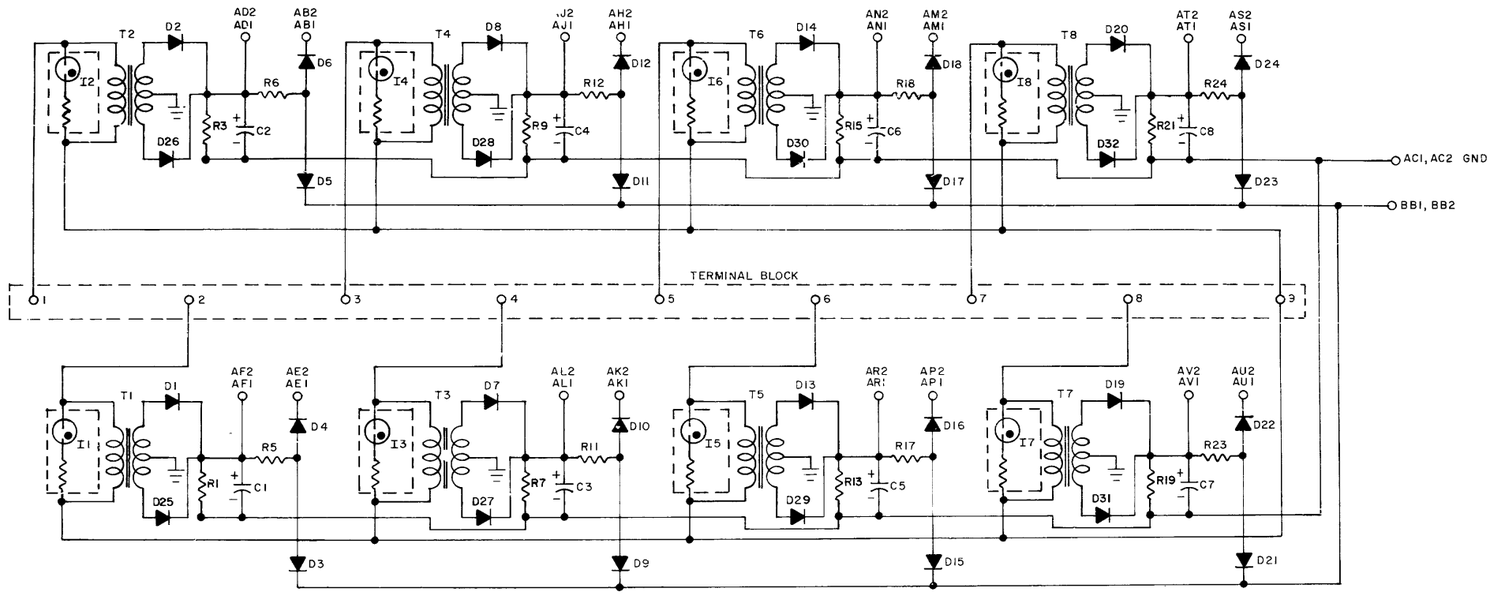

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
TERMINAL BLOCK	BLOCK, 9 TERMINAL 699-2-3701-9	1209083
T1,-T8	TRANSFORMER, POWER	1609844
R5,R6,R11,R12,R17,R18,R23,R24	RES. 4.7K 1/4W 10% CC	1300448
I1-I8	LAMP	1209337
R1,R3,R7,R9,R13,R15,R19,R21	RES. 390 1/4W 10% CC	1300310
D3-D6,D9-D12,D15-D18,D21-D24	DIODE D600	1105366
D1,D2,D7,D8,D13,D14,D19,D20,D25-D32	DIODE D672	1105275
C1 THRU C8	CAP. 68 MFD 15V 10% TANT	1000082
	PARTS LIST	A-PL-K578-0-0

PARTS LIST

REVISIONS		
CHK	CHG NO.	REV.
	00002	A

DRN. M. Haller DATE 2-5-69
CHK'D. [signature] DATE 2-17-69
ENG. [signature] DATE 4/23/69
PROD. DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D600	IN4009		
D672	IN3653		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE AC INPUTS K578

SIZE	CODE	NUMBER	REV.
C	CS	K578-0-1	A

PRINTED CIRCUIT REV. B

DEC FORM NO. DRC 102

SIZE C CODE CS NUMBER K578-0-1 REV. A

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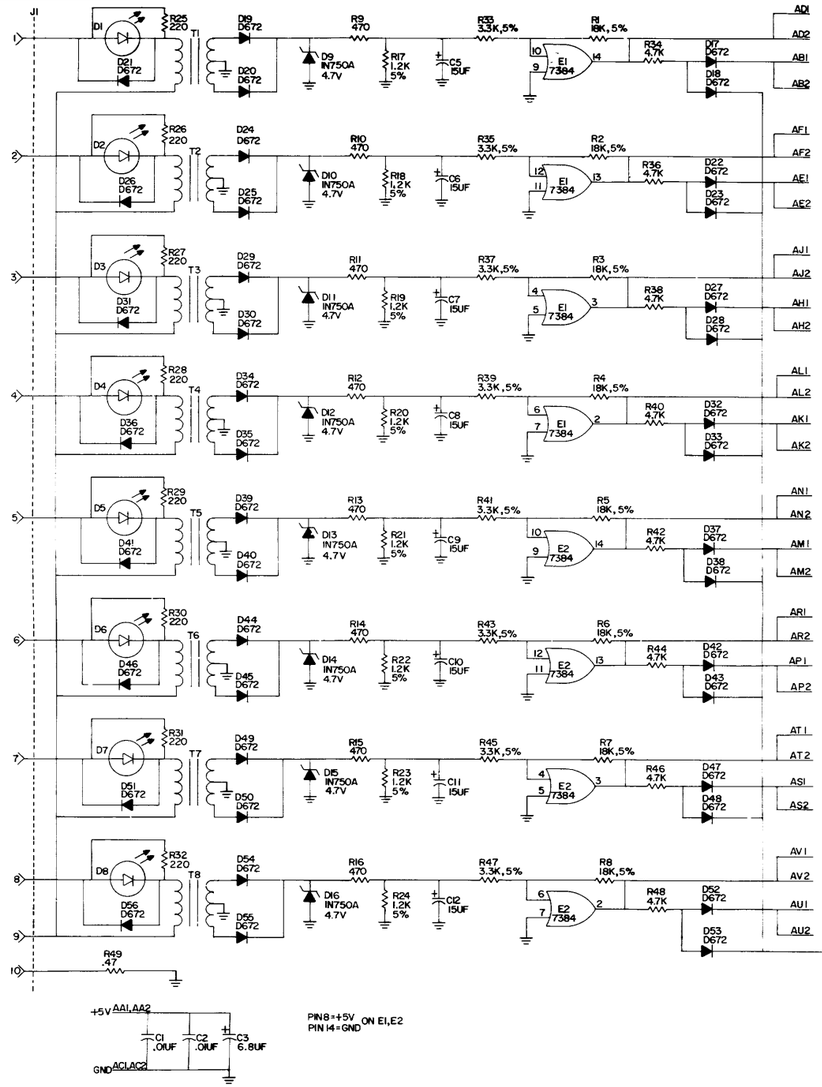
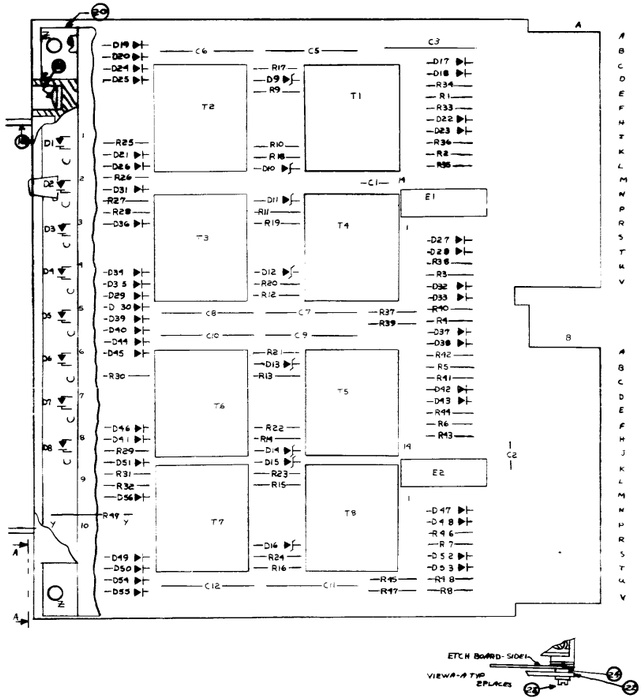




QTY.	REF. DESIGNATION	DESCRIPTION	DEC PART NO.	ITEM NO.
		PARTS LIST		
		X-Y COORDINATE HOLE LOCATION	A-CO-K579-0-4	
		ASSY/DRILLING HOLE LAYOUT	D-AH-K579-0-5	
		MODULE ECO HISTORY	B-M2-K579-0-4	3
1		ETCHED CIRCUIT BOARD	5009776	4
				5
40	D17 - D56	DIODE D672	1105272	10
8	D9 - D16	DIODE 1N750A 4.7V 5% .4W	1105126	9
2	C1, C2	CAP. .01UF 100V 20% DISC	1004416	8
8	C5 - C12	CAP. 15UF 20V 10% S.TANT	1004811	7
1	C3	CAP. 6.8UF 35V 20% S.TANT	1004067	6
8	R25- R32	RES. 22C ¼W 10%	1306271	13
1		TERMINAL STRIP RED	1210324-00	12
8	D1 - D8	LIGHT EMITTING DIODE	1116340	11
8	R17 - R24	RES. 1.2K ¼W 5%	1304324	14
8	R34, 36, 38, 40, 42, 44, 46, 48	RES. 4.7K ¼W 10%	1304448	15
8	R1 - R8	RES. 18K ¼W 5%	1304745	17
1	R49	RES. .47 2W 5% WW	1305456	18
8	R9 - R16	RES. 470 ¼W 5%	1304321	17
1		BRACKET	C-MD-530943G-0-0	21
2	E1, E2	I.C. DEC 7384	1541383	20
1		INSULATOR PLATE	B-MD-5508235-0-0	22
4		SCR BHM #6-32 x 3/8LG	9006602-4	23
2		WASHER FIBER #6	9006693	24
1		DECAL K579	7409365-2	25
8	R33,35,37,39,41,43,45,47	RES. 3.3K ¼W 5%	1304439	26

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D672	IN3653		
IN750A	SAME		

REVISIONS					
Change per ECO M7000	T.C.	6 Mar 72	A. RICKETTS		
63 Thick PCB					
Change per ECO M7000	T.C.	3 May 72	A. RICKETTS		
Change per ECO M7000	T.C.	5 Jun 72	A. RICKETTS		

DRWN: G. Hale 12/17/71
CHK'D: [illegible] 12/17/71
ENG: [illegible] 5/22/72
PROD: DATE

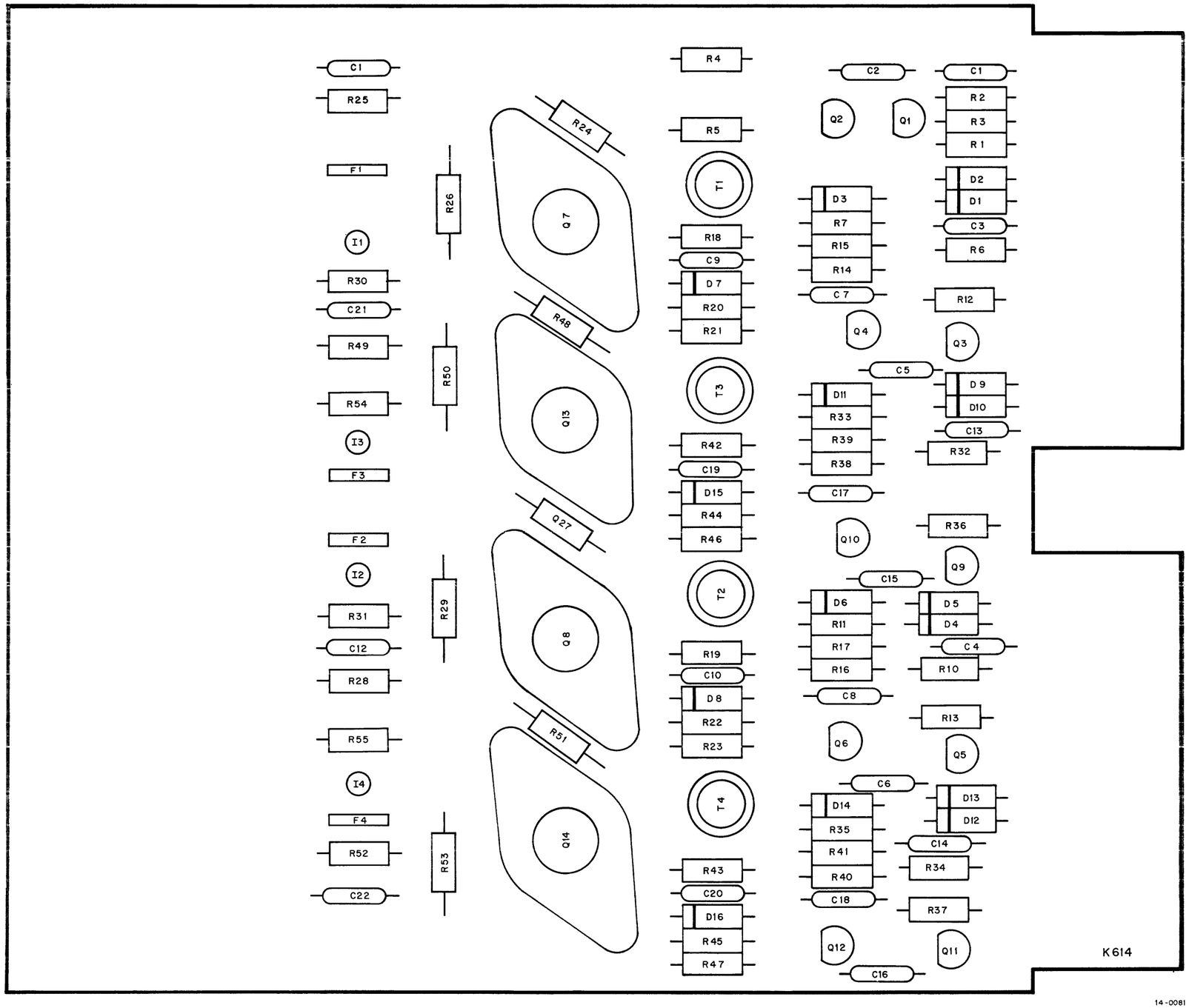
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: A/C INPUT CONVERTER
SIZE D | CODE CS | NUMBER K579-0-1 | REV J
PRINTED CIRCUIT REV C

SIZE CODE D CS | NUMBER K579-0-1 | REV C

DEC FORM NO 542 1

K614


C1
R25
F1
I1
R30
C21
R49
R54
I3
F3
F2
I2
R31
C12
R28
R55
I4
F4
R52
C22
R26
R50
R29
R53
R24
Q7
R48
Q13
Q27
Q8
R51
Q14
R4
R5
T1
R18
C9
D7
R20
R21
T3
R42
C19
D15
R44
R46
T2
R19
C10
D8
R22
R23
T4
R43
C20
D16
R45
R47
C2
Q2
Q1
C1
R2
R3
R1
D2
D1
C3
R6
D3
R7
R15
R14
C7
R12
Q4
Q3
C5
D9
D10
C13
R32
D11
R33
R39
R38
C17
R36
Q10
Q9
C15
D6
D5
R11
D4
R17
C4
R16
R10
C8
R13
Q6
Q5
C6
D13
D14
D12
R35
C14
R41
R34
R40
C18
R37
Q12
Q11
C16
K614

14-0081

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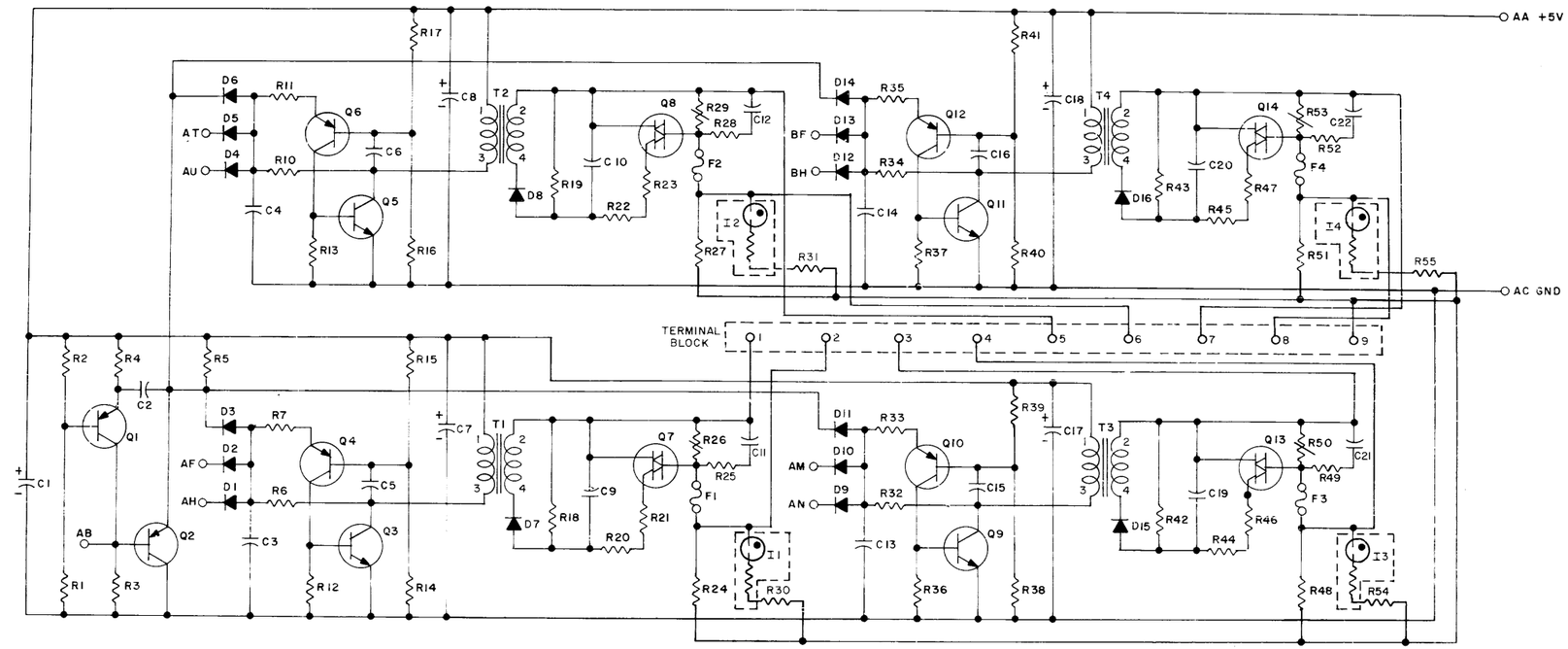

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-K614-0-0
R3	RES 560Ω 1/4W 5%	1301890
R5	RES 220Ω 1/4W 5%	1300271
CC	.022 MFD 100V 10%	1010780
T1-T4	TRANSFORMER	1609751
TERMINAL BLOCK	BLOCK, 9 TERMINAL 699-Z 3701-9	1209083
F1-F4	FUSE, PICO 5A #276005	1209070
Q7, Q8, Q13, Q14	TRIAC RCA 40430	1505564
Q3, Q5, Q9, Q11	TRANSISTOR DEC1008-S	1502155
Q1, Q2, Q4, Q6, Q10, Q12	TRANSISTOR DEC6534D	1503409
R30, R31, R54, R55	RES. 15K 1/4W 10% CC	1300494
R26, R29, R50, R53	VARISTOR 333 BNR-7	1305571
R24, R27, R48, R51	RES. 10K 2W 10% CC	1300482
R44-R47, R49, R52 R7, R11, R20-R23, R25, R28, R33, R35,	RES. 10 1/4W 10% CC	1300170
R3, R4, R14-R17, R38-R41	RES. 4.7K 1/4W 10% CC	1300448
R19, R32, R34, R36, R37, R42, R43, R4 R1, R2, R5, R6, R8, R9, R10, R12, R13, R18,	RES. 1.2K 1/4W 10% CC	1300386
D7, D8, D15, D16	DIODE D672	1105275
D1-D6, D9-D14	DIODE D600	1105366
C11, C12, C21, C22	CAP. .047MFD 400V 20%	1009656
C7, C8, C17, C18	CAP. 2.2MFD 20V 10%	1002627
C5, C6, C15, C16	CAP. 100MMF 100V 5% DM	1000016
C3, C4, C13, C14	CAP. 680MMF 500V 10% CER.	1005726
C2, C9, C10, C19, C20	CAP. .047MFD 250V 20%	1003053
C1	CAP. 22MFD 6V 10% TANT	1005636

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D600	1N4009		
D672	1N3633		
DEC6534D	MPS6534		
DEC1008	MM1008		

REVISIONS			
CHK	CHG NO	REV	
	00001	A	
	00003	B	
	00004	C	
	00006	E	
	00007	F	

DRN. M. Walker DATE 1-21-69
CHK'D. DATE
ENG. DATE
PROD. DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE ISOLATED AC SWITCH K614

SIZE	CODE	NUMBER	REV
C	CS	K614-0-1	F

PRINTED CIRCUIT REV. D

REV F | NUMBER K614-0-1 | SIZE C | CODE CS

DEC FORM NO. DRC 102

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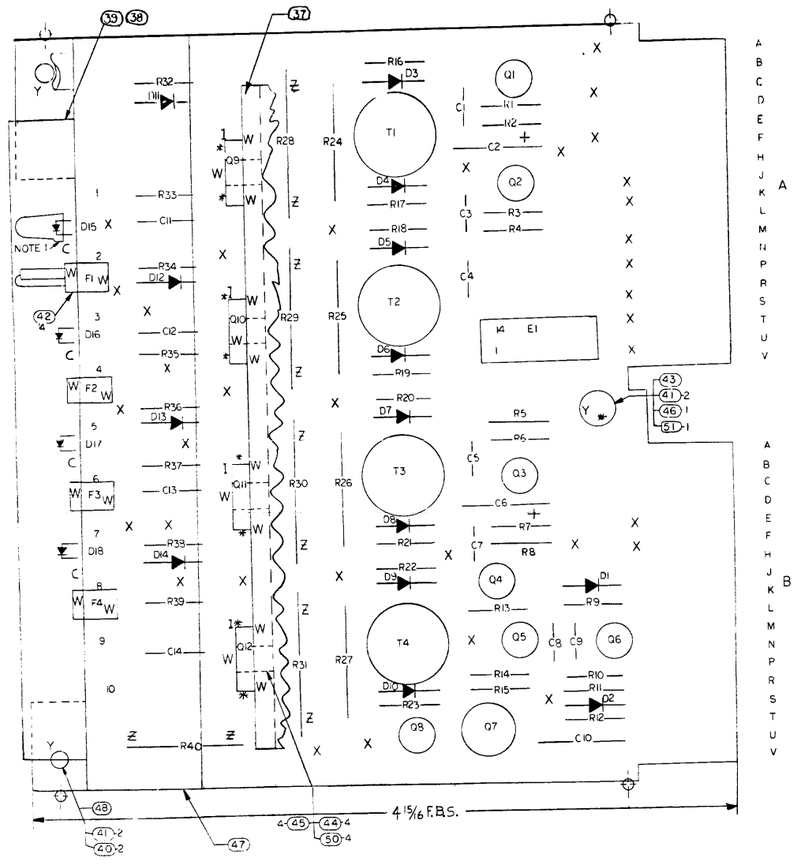

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		
1		ETCHED CIRCUIT BOARD	5010009	4
		MODULE ECO HISTORY	B-MH-K616-0-6	3
		ASSY/DRILLING HOLE LAYOUT	D-AH-K616-0-5	2
		X -Y COORDINATE HOLE LOCATION	K-CO-K616-0-4	1
QTY.	REF. DESIGNATION	DESCRIPTION	Dec PART NO.	ITEM NO.
2	C9, C8	CAP. 1000PF 100V 5% MICA	1000642	6
				5
4	C11, C12, C13, C14	CAP. .047UF 400V 20%	1009652	11
4	C1, C3, C5, C7	CAP. .005UF 100V 20% DISC	1001765	10
1	C4	CAP. .01UF 100V 20% DISC	1001610	9
1	C10	CAP. 680PF 500V 10% CER	1005726	8
2	C2, C6	CAP. 3.9UF 10V 10% S.TANT	1000064	7
14	D1 thru D14	DIODE D672	1105275	13
4	DI5, DI6, DI7, DI8	LIGHT EMITTING DIODE	1110324	14
4	R33, R35, R37, R39	RES. 10 ¼W 10%	1300170	15
4	R17, 19, 21, 23	RES. 12 ¼W 10%	1301430	16
4	R11, 32, 34, 36, 38	RES. 220 ¼W 5%	1300271	17
5	R13, R15	RES. 470 ¼W 5%	1300316	18
				19
1	R10	RES. 2.7K ¼W 5%	1300426	20
1	R18	RES. 4.7K ¼W 10%	1300448	21
				22
4	R28, 29, 30, 31	RES. 10K 2W 10%	1300482	23
1	R14	RES. 120 ¼W 10%	1301418	24
4	R16, 18, 20, 22	RES. 1.2K ¼W 10%	1300386	25
1	R9	RES. 15K ¼W 5%	1300496	26
1	R40	RES. .47 2W 5% W.W.	1305258	27
4	R24, 25, 26, 27	VARISTOR 333 BNR-7	1305571	28
				29
1	Q7	TRANS DEC 1008	1502155	30
3	Q8, Q5, Q6	TRANSISTOR- DEC 65318	1509338	31
4	Q1, 2, 3, 4	TRANS DEC 6534D	1503409-00	32
4	Q9, 10, 11, 12	TRIAC SAC 58	1510939	33
4	T1, 2, 3, 4	TRANSFORMER	1605794-25	34
1	E1	I.C. DEC 7401	1905590	35
4	F1, 2, 3, 4	FUSE 5A	1209070	36
1		HEAT SINK	1210953	37
1	TS1	TERMINAL STRIP RED	1210376-00	38
1		DECAL - (FOR TERMINAL STRIP)	7409406	39
2		WASHER FIBER #6	9006693	40
6		SCR BHM #6-32 x 3/8	9006022-4	41
4		FUSE HOLDER	9009141	42
1		SPACER ¼ x 6-32 x 1" THREADED	9006862	43
4		SCREW, PHM #4-40 x 5/8 LONG	9006044-1	44
4		KEP-NUT #4-40	9006557	45
1		WASHER INT. TOOTH #6	9006633	46
1		BRACKET	5309436	47
1		INSULATOR PLATE	5508235	48
35		EYELETS	9006731	49
4		WASHER INT. TOOTH #4	9006632	50
2		WASHER NYLON #6	9006707	51
A	R1 - R8	RES. 820 ¼W 10%	1300367	52

DEC NO.	EIA NO.	DEC NO.	EIA NO.
DEC 6534D	NONE		
DEC 6531B	MPS6531		
DEC 1008	NONE		
D672	IN3653		
D664	IN3606		

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	CHK
A	K616-00001	
B	K616-00002	

V. BOAEN 11-26-72 — V. BOAEN 3-29-72 — B.F. Wade 4-8-72

ETCH BOARD REV A

DRN. G. Mackenzie 3-29-72
CHK'D. B.F. Wade 3-29-72
ENG. J. Bosca 3-29-72
PROJ. ENG. V. Boaen
PROD. J. Miranda 3-27-72
NEXT HIGHER ASSY
SCALE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ISOLATED A C OUTPUT

SIZE D | CODE CS | NUMBER K616-0-1 | REV. B | DIST.

DEC FORM NO DRD-135

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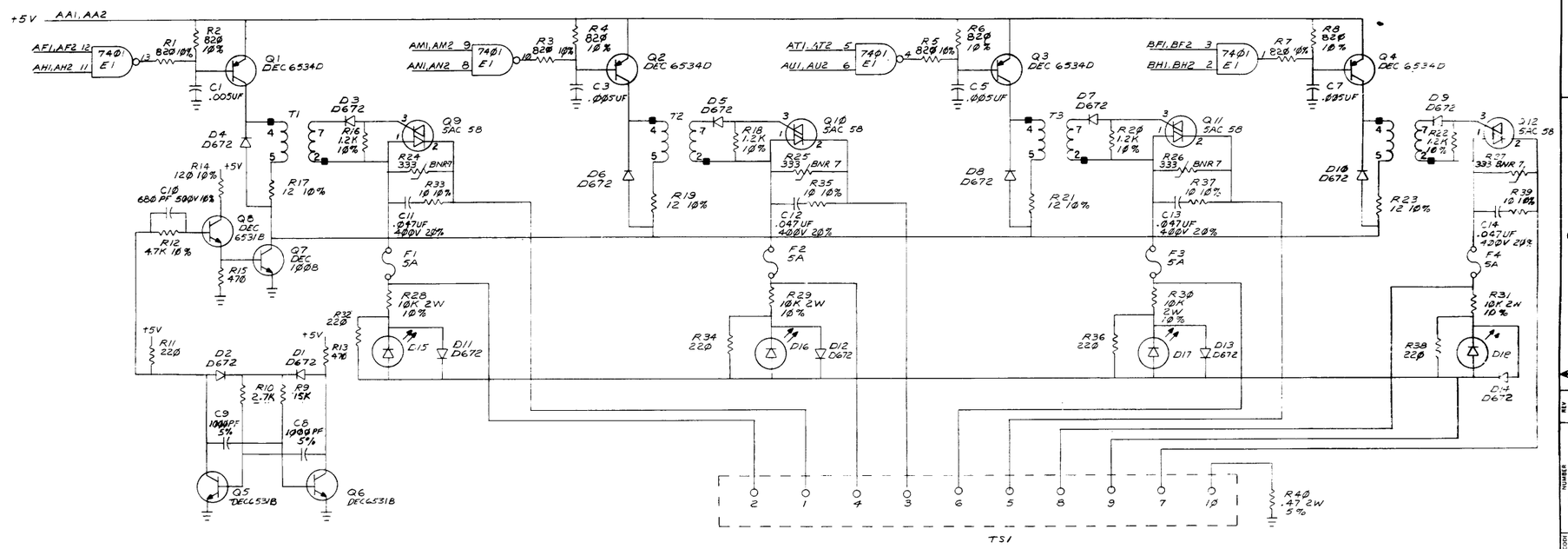
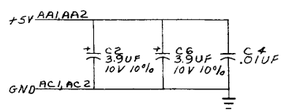




UNLESS OTHERWISE INDICATED:
RESISTORS = 1/4 W, 5%
CAPACITORS = 100 V, 20%
PIN 7 = GND ON E1
PIN 14 = +5V

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

ETCH BOARD REV A

REV	CHANGE NO.	CHK

REVISIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

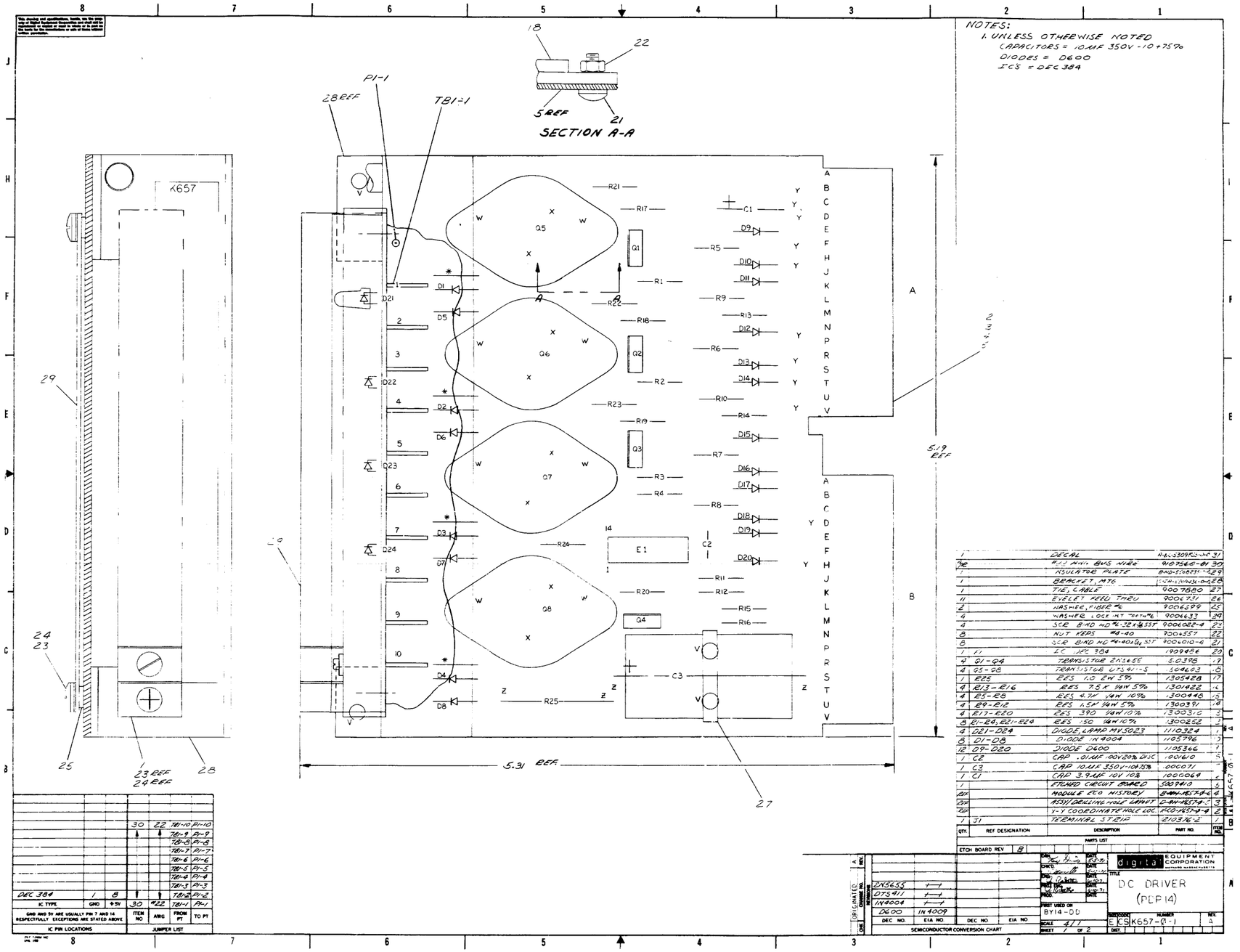
DRN.		DATE 3-20-72
CHK'T.		DATE 3-20-72
ENG.	V. Baeza	DATE 3-20-72
PROJ. ENG.	V. Duran	DATE 3-20-72
PROD.		DATE
NEXT HIGHER ASSY		
SCALE		
SHEET 2 OF 2		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ISOLATED AC OUTPUT

SIZE D | CODE CS | NUMBER K616-0-1 | REV. B | DIST.

DEC FORM NO DRD-135



IC TYPE	GND	+5V
DEC 384	1	8
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTFULLY. EXCEPTIONS ARE STATED ABOVE		
IC PIN LOCATIONS		

ITEM NO	AWG	FROM PT	TO PT
30	22	TB1-10	P1-10
		TB1-9	P1-9
		TB1-8	P1-8
		TB1-7	P1-7
		TB1-6	P1-6
		TB1-5	P1-5
		TB1-4	P1-4
		TB1-3	P1-3
30	#22	TB1-2	P1-2
		TB1-1	P1-1
JUMPER LIST			

QTY.	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1		DECAL	[illegible]	31
AR		#22 AWG BUS WIRE	9107566-01	30
1		INSULATOR PLATE	8104-5108951-*29	
1		BRACKET, MTG	7074-5104434-0428	
1		TIE, CABLE	9007680	27
11		EYELET, FEED THRU	9004751	26
2		WASHER, FIBER #6	9006599	25
4		WASHER, LOCK INT #6 TYPE W	9006633	24
4		SCR, BIND HD #6-32 X 3/8 SST	9006022-9	23
8		NUT, KEPS #6-40	9004557	22
8		SCR, BIND HD #4-40 X 1/4 SST	9006010-6	21
1	11	IC, DEC 384	1109956	20
4	Q1-Q4	TRANSISTOR 2N5655	1.03196	19
4	Q5-Q8	TRANSISTOR 2N5411-5	1694622	18
1	R25	RES 1.0 2W 5%	1305428	17
4	R13-R16	RES 7.5K 1/4W 5%	1301422	16
4	R5-R8	RES 4.7K 1/4W 10%	1300440	15
4	R9-R12	RES 1.5K 1/4W 5%	1300391	14
4	R17-R20	RES 390 1/4W 10%	1300316	13
8	R1-R4, R21-R24	RES 50 1/4W 10%	1300252	12
4	Q21-Q24	DIODE, LAMP MV5023	1110324	11
8	D1-D8	DIODE IN4004	1105796	10
12	D9-D20	DIODE D600	1105346	9
1	C2	CAP .01MF 100V 20% CER	100160	8
1	C3	CAP 10MF 35V(-10+75)%	1000071	7
1	C1	CAP 3.9MF 10V 10%	1000069	6
1		ETCHED CIRCUIT BOARD	5007410	5
1IN		MODULE ECO HISTORY	B-MM-A0744-4	4
1SH		ASSY DRAWING MAT LAYOUT	C-MM-A0744-*	3
TOT		Y-Y COORDINATE HOLE LOC.	ECO-A0744-0-4	2
1	J1	TERMINAL STRIP	2103376-2	1

PARTS LIST

ETCH BOARD REV B

ORIGINATED	DEC NO.	EIA NO.
	2N5655	2N
	2N5411	2N
	1N4004	1N
	D600	1N4009
DRC	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: DC DRIVER (PDP14)

SIZE A | NUMBER K657-0-1 | REV A

SHEET 1 OF 2

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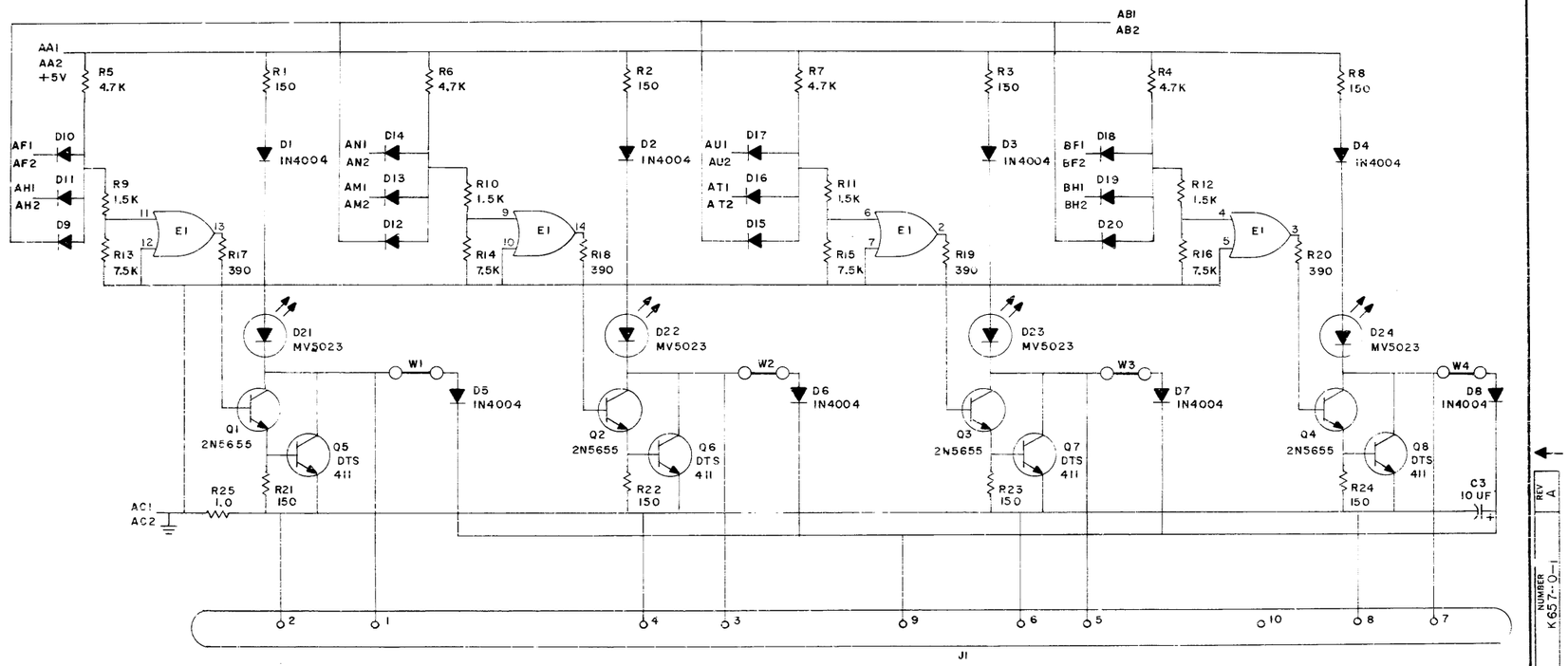
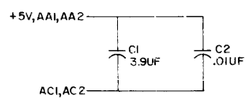


UNLESS OTHERWISE INDICATED:
DIODES ARE D600
PIN 1 = GND ON ALL IC'S
PIN 8 = +5V



SHEET 2 OF 2

REVISIONS			
REV	CHG NO	CHK	

DRN	B. J. Daile	DATE 4/14/71
CHK'D		DATE 5-24-71
ENG	J. Puckett	DATE 6-10-71
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

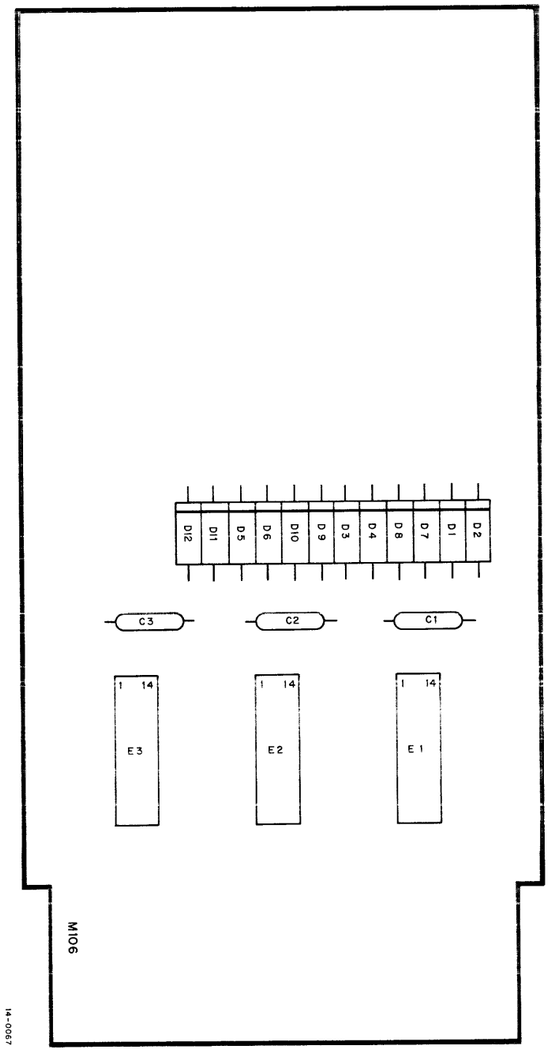
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PDP 14 D.C. DRIVER

SIZE	CODE	NUMBER	REV
C	CS	K657-0-1	A

PRINTED CIRCUIT REV B

REV	NUMBER	SIZE	CODE
A	K657-0-1	C	CS



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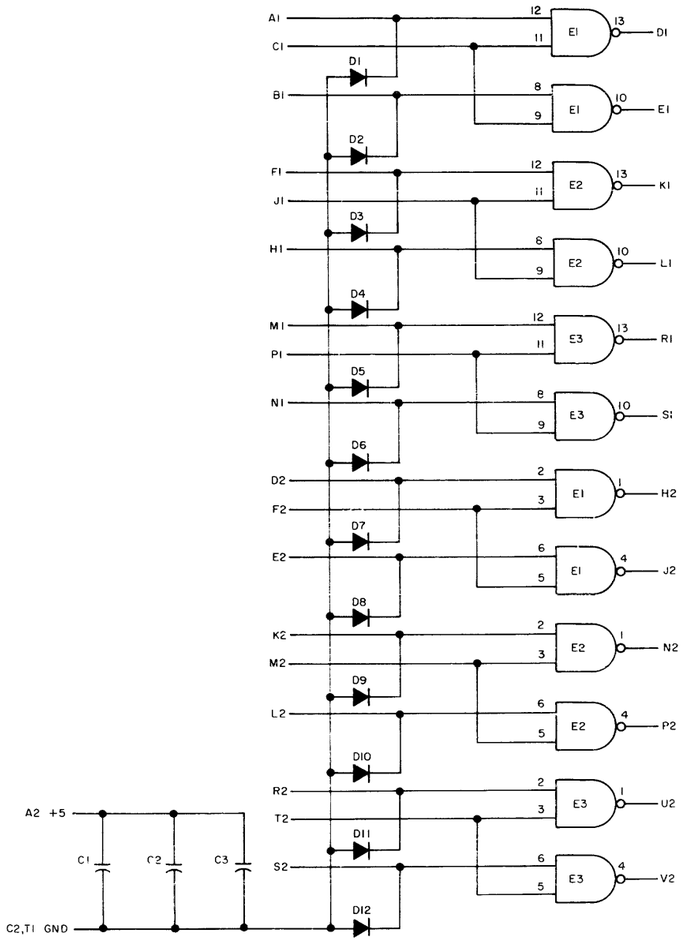


UNLESS OTHERWISE INDICATED:
DIODES ARE D664
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
IC'S ARE DEC8881
CAPACITORS ARE .01uf, 100V, 20%

REV. B

SIZE	CODE	NUMBER
C	CS	M106-0-1

REVISIONS			
REV.	CHG NO.	CHK	
B	00001	[illegible]	

DRN. R. BUTLER	DATE	4/8/69
CHK'D [illegible]	DATE	4-8-69
ENG. [illegible]	DATE	5-1-69
PROD.	DATE	

DEC FORM NO. DRC 102

TRANSISTOR & DIODE CONVERSION CHART

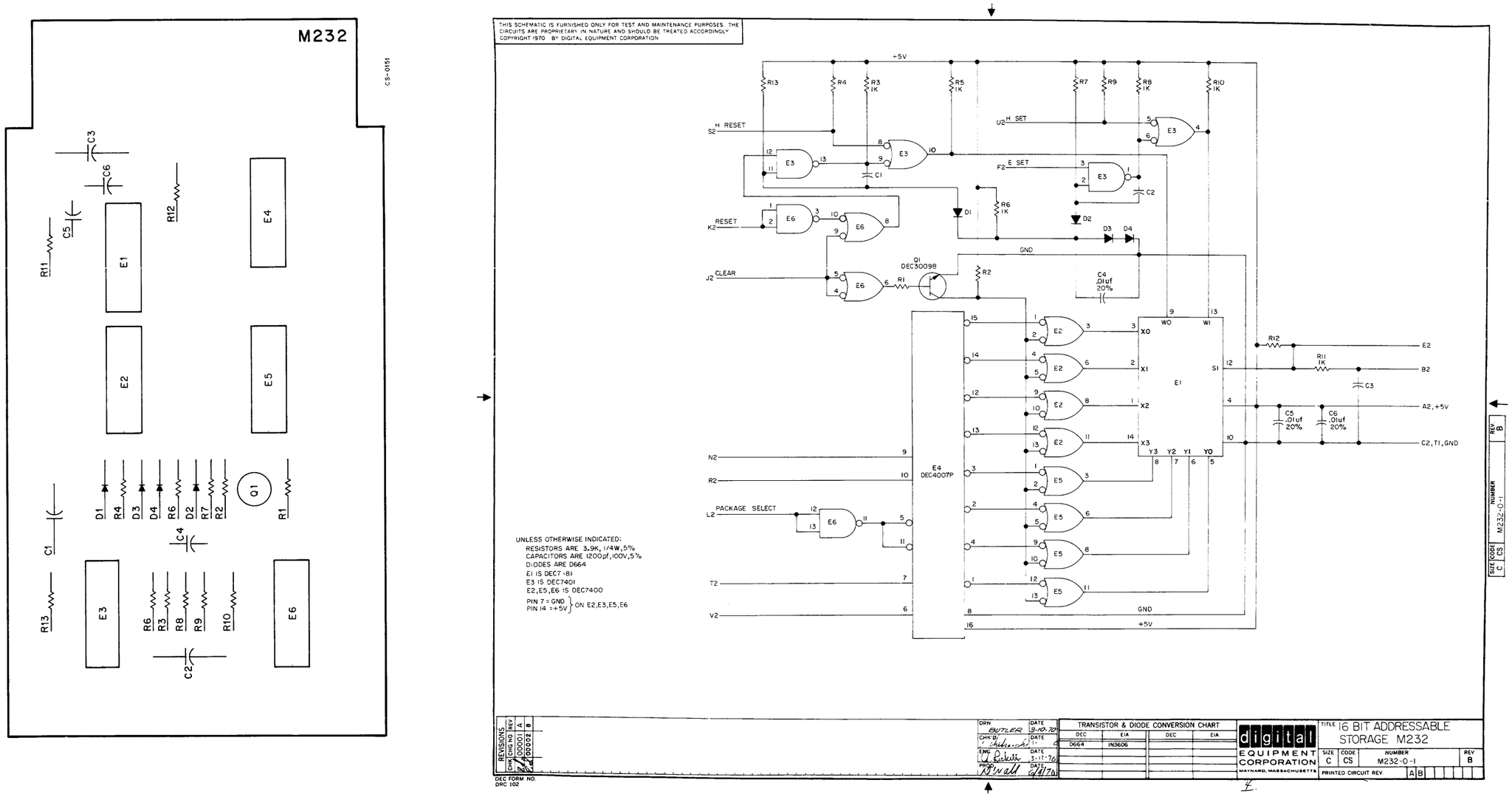
DEC	EIA	DEC	EIA
D664	IN3606		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: DOT NOR GATES M106

SIZE	CODE	NUMBER	REV.
C	CS	M106-0-1	B

PRINTED CIRCUIT REV. A


M232
CS-0151
C3
C6
C5
R11
R12
E1
E2
E3
E4
E5
E6
D1
R4
D3
D4
R6
D2
R7
R2
Q1
R1
C1
C4
R13
R6
R3
R8
R9
R10
C2
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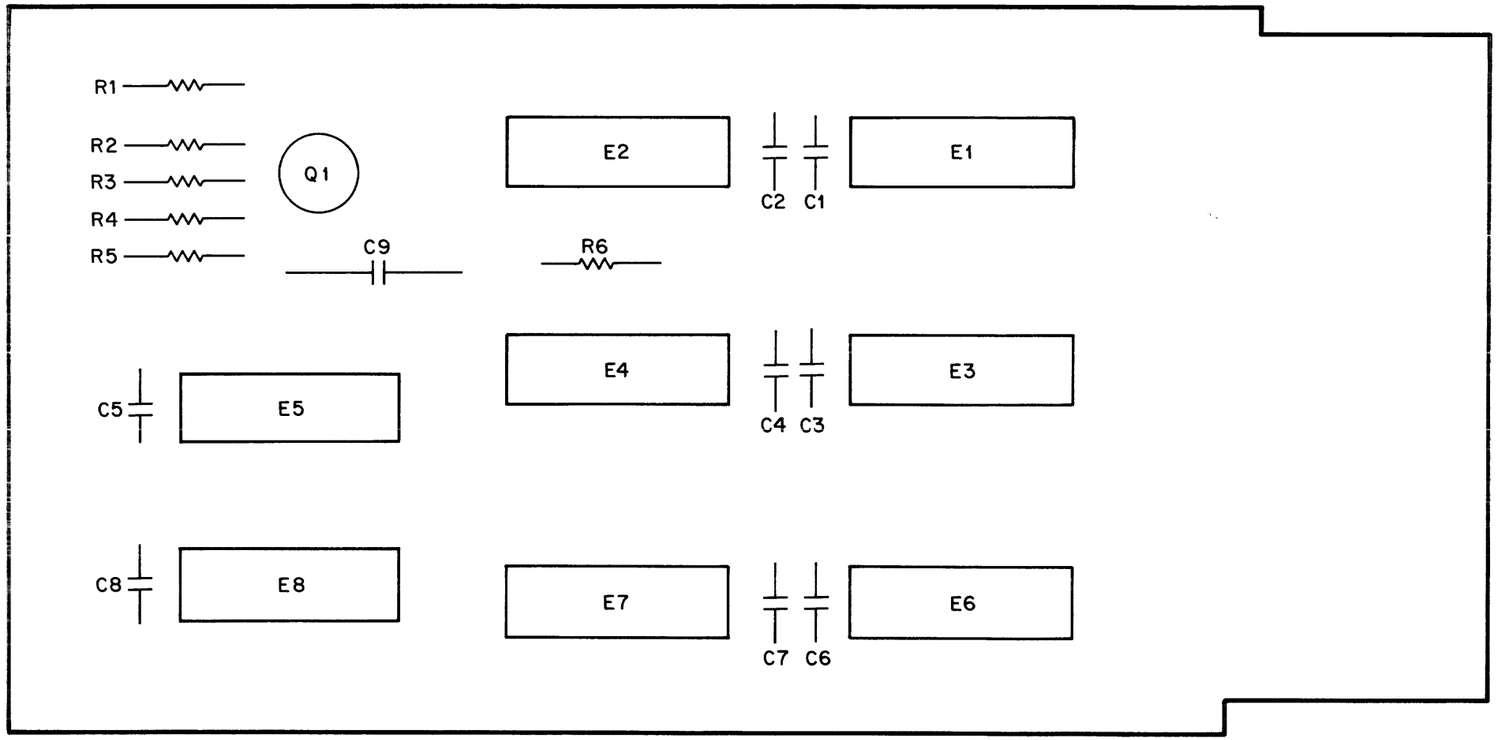
+5V
R13
R4
R3 1K
R5 1K
R7
R9
R8 1K
R10 1K
S2 H RESET
U2 H SET
F2 E SET
K2 RESET
J2 CLEAR
Q1 DEC3009B
R1
R2
R6 1K
D1
D2
D3
D4
GND
C4 .01uf 20%
E4 DEC4007P
N2
R2
L2 PACKAGE SELECT
T2
V2
W0
W1
X0
X1
X2
X3
Y3
Y2
Y1
Y0
S1
R12
R11 1K
C3
C5 .01uf 20%
C6 .01uf 20%
E2
B2
A2,+5V
C2,T1,GND
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 3.9K, 1/4W, 5%
CAPACITORS ARE 1200pf, 100V, 5%
DIODES ARE D664
E1 IS DEC7181
E3 IS DEC7401
E2, E5, E6 IS DEC7400
PIN 7 = GND
PIN 14 = +5V
ON E2, E3, E5, E6
REVISIONS
CHK'D
DRN BUTLER
DATE 3-10-70
CHK'D
DATE
ENG
DATE 3-17-70
PROD
DATE 6/4/70
DEC FORM NO. DRC 102
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
D664
IN3606
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE 16 BIT ADDRESSABLE STORAGE M232
SIZE C
CODE CS
NUMBER M232-0-1
REV B
PRINTED CIRCUIT REV. A B



14-0152

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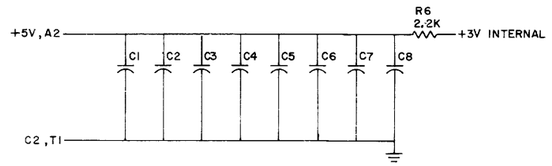
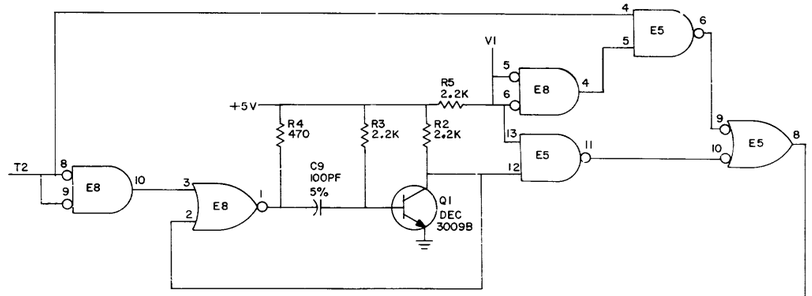
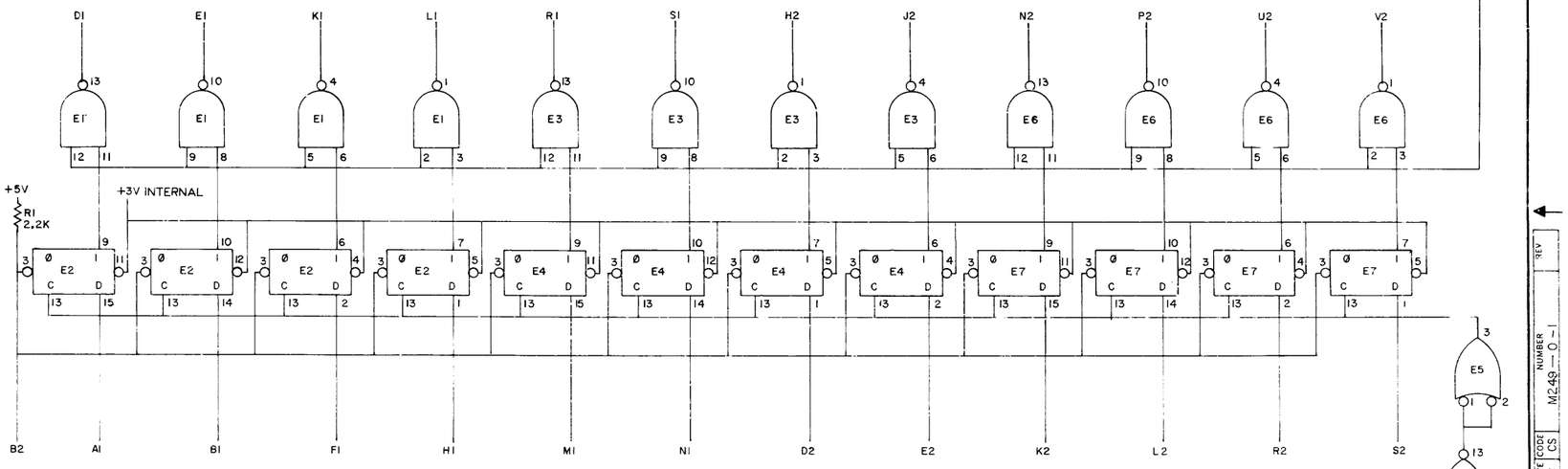
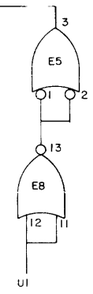








UNLESS OTHERWISE INDICATED:
RESISTORS = 1/4 W, 5%
CAPACITORS = .01UF, 100V, 20%

DEC7402 = E8
DEC8881 = E1, E3, E6
DEC4015P = E2, E4, E7
DEC7437 = E5

PIN 8 = GND
PIN 16 = +5V ON E2, E4, E7

PIN 7 = GND
PIN 14 = +5V ON ALL OTHER IC'S

REVISIONS

CHG	CHG NO	REV

DRN	NANCY MOORE	DATE 3-17-71
CHK		DATE
ENG		DATE 5-24-71
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3009B	2N3009		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

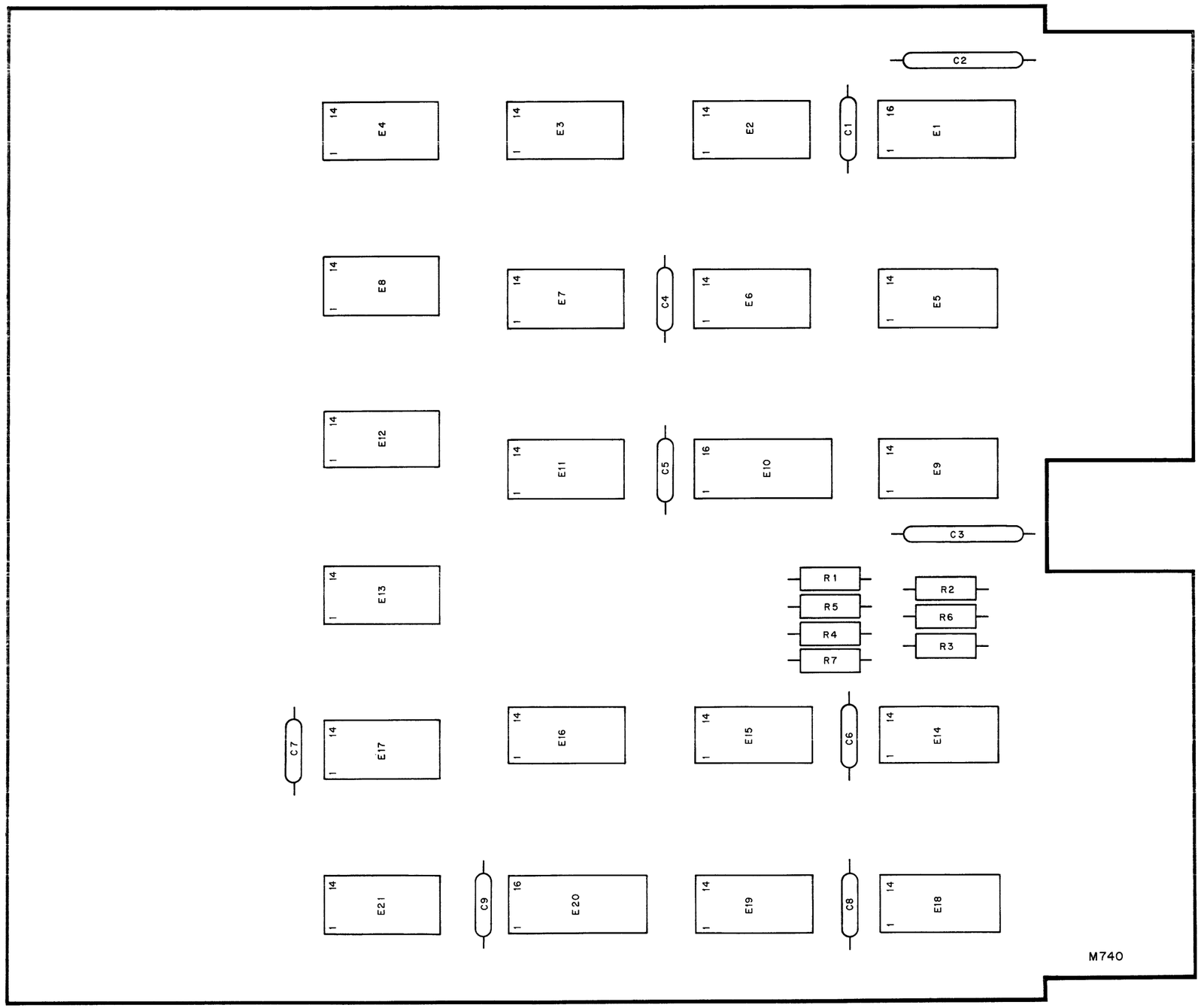
TITLE: BUS REGISTER

SIZE	CODE	NUMBER	REV
C	CS	M249-0-1	

PRINTED CIRCUIT REV A

SIZE C | CODE CS | NUMBER M249-0-1 | REV

DEC FORM NO
DRC 102


C2
C1
C3
C4
C5
C6
C7
C8
C9
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18
E19
E20
E21
R1
R2
R3
R4
R5
R6
R7
M740

14-0043

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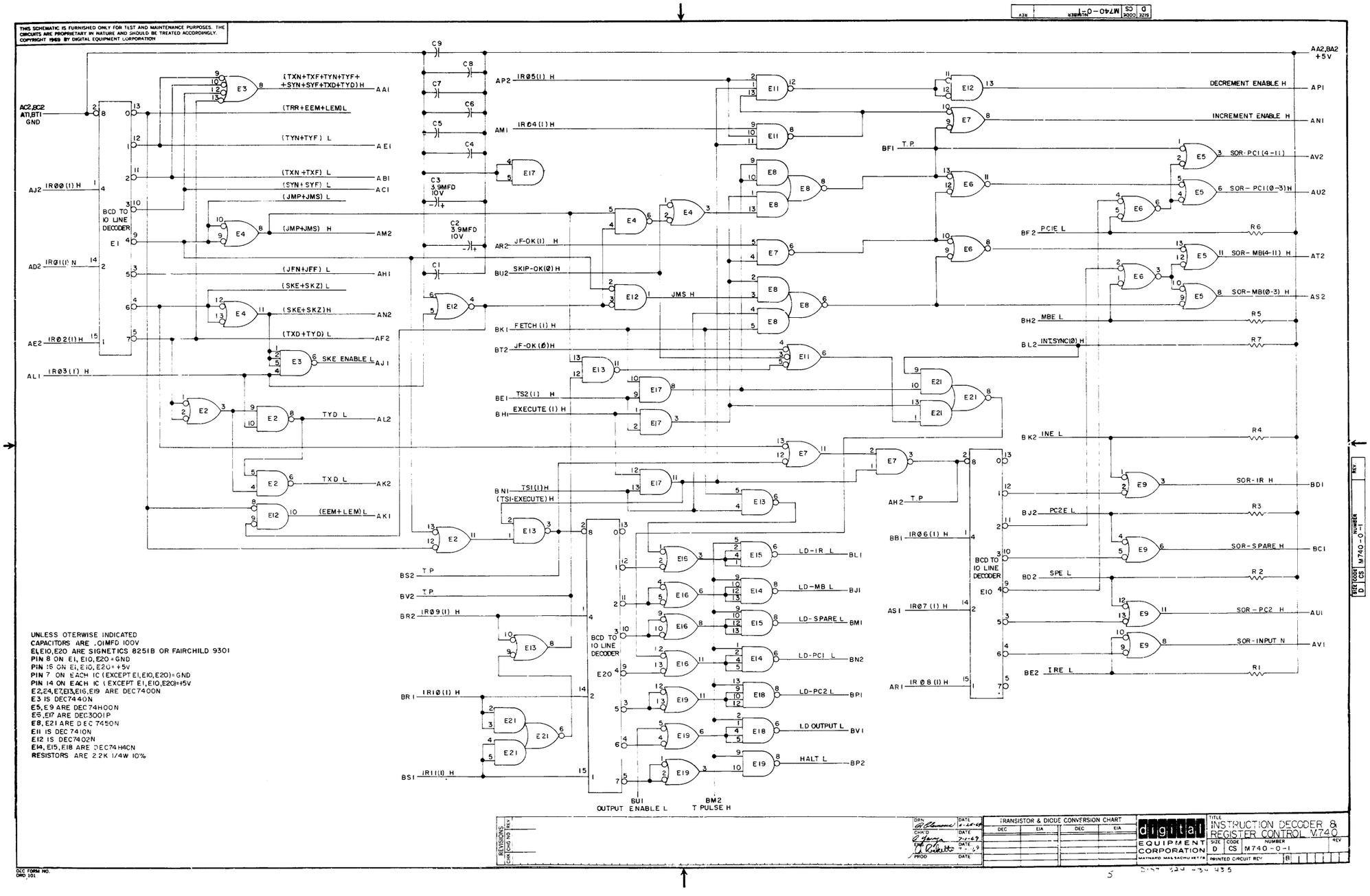

UNLESS OTERWISE INDICATED
CAPACITORS ARE .OIMFD 100V
E1,E10,E20 ARE SIGNETICS 8251B OR FAIRCHILD 9301
PIN 8 ON E1, E10, E20 = GND
PIN 16 ON E1, E10, E20 = +5V
PIN 7 ON EACH IC (EXCEPT E1,E10,E20) = GND
PIN 14 ON EACH IC (EXCEPT E1,E10,E20) = +5V
E2,E4,E7,E13,E16,E19 ARE DEC7400N
E3 IS DEC7440N
E5,E9 ARE DEC74H00N
E6,E17 ARE DEC3001P
E8,E21 ARE DEC7450N
E11 IS DEC7410N
E12 IS DEC7402N
E14, E15,E18 ARE DEC74H4CN
RESISTORS ARE 2.2K 1/4W 10%

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

REVISIONS

DRN	DATE
CHK'D	DATE
ENG	DATE
PROD	DATE

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: INSTRUCTION DECODER & REGISTER CONTROL V.740

SIZE D | CODE CS | NUMBER M740-0-1 | REV B | PRINTED CIRCUIT REV

DEC FORM NO. CMD 101

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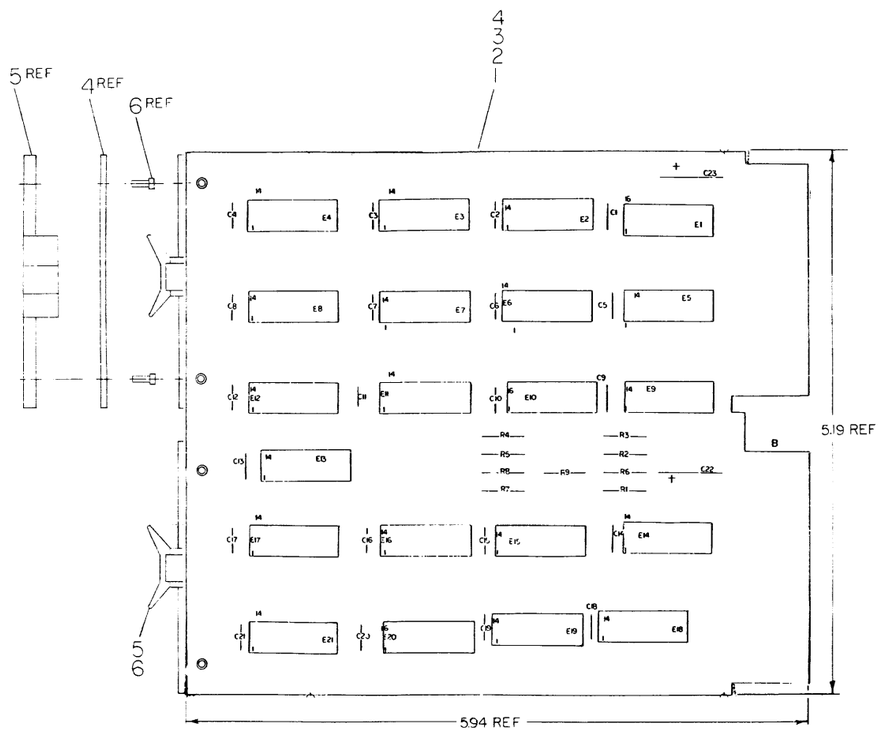
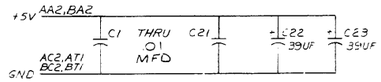
NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS ARE 100V, 20%
2. ALL RESISTORS ARE 1/4W, 5%
3. RESISTANCE IS IN OHMS.
4. CAPACITANCE IS IN PICOFARADS.





QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
9	R1 THRU R9	RES 2.2K 1/4W 5%	1300418	20
2	E6,E17	IC DEC 7408	1910155	19
1	E14	IC DEC 7437	1910291	18
3	E1,E10,E20	IC DEC 8251	1909594	17
2	E5,E9	IC DEC 74H00	1909056	16
1	E8	IC DEC 7402	1909004	15
1	E18	IC DEC 74H40	1905586	14
2	E13,E21	IC DEC 7450	1905580	13
1	E2	IC DEC 7440	1905579	12
1	E12	IC DEC 7410	1905576	11
7	E3,E4,E7,E11,E15,E16,E19	IC DEC 7400	1905575	10
21	C1 THRU C21	CAP. .01 UF 100V 20% DISC	10-01610	9
2	C22, C23	CAP. 39 UF 10V 10% TANT	10-00056	8
A/R		GRIPLET	12-10244-0	7
4		EYELET, GS4-7 STIMPSON	9006732	6
2		HANDLE, FLIP CHIP, MAGENTA	9008337-96	5
1		ETCHED CIRCUIT BOARD	5009926	4
REF		MODULE ECO HISTORY	B-MH-M7400-0-6	3
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7400-0-4	2
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7400-0-5	1

PARTS LIST

ETCH BOARD REV B

FIRST USED ON OPTION MODEL: DL14

IC PIN LOCATIONS		
8251	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REVISIONS: CHANGE NO. / REV / CHK

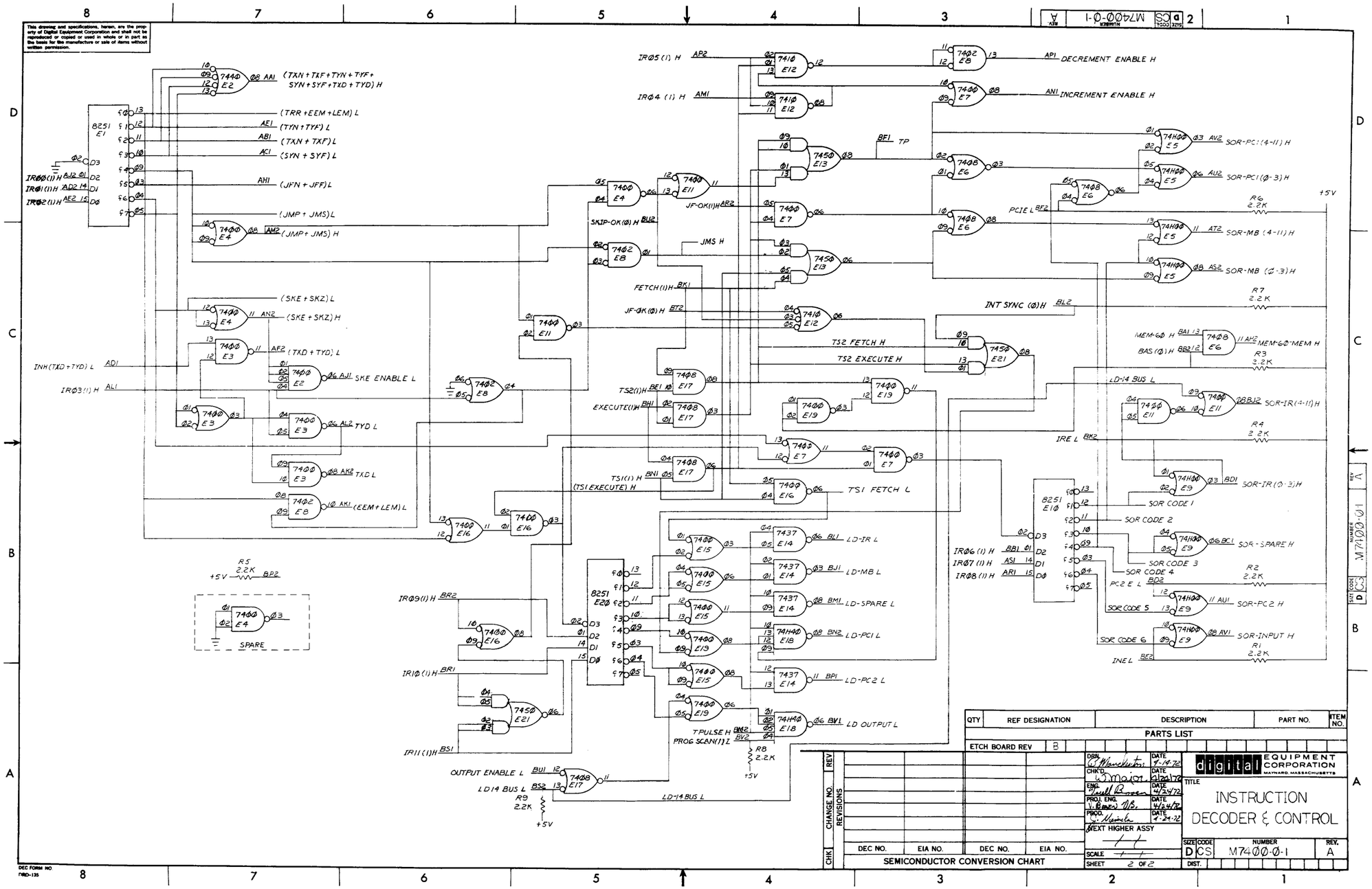
DRN: M. Marvikian DATE 4-12-72
CHK'D: W. Mann DATE 4/24/72
ENG: D. Cooper DATE 4/22/72
PROJ. ENG: J. Green DATE 4-22-72
PROD: W. Winkler DATE 4-24-72
NEXT HIGHER ASSY: —
SCALE: —
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: INSTRUCTION DECODER & CONTROL

SIZE D | CODE CS | NUMBER M7400-0-1 | REV A | DIST

DRAWING 40-522 16899 | DEC FORM NO DRD 135A



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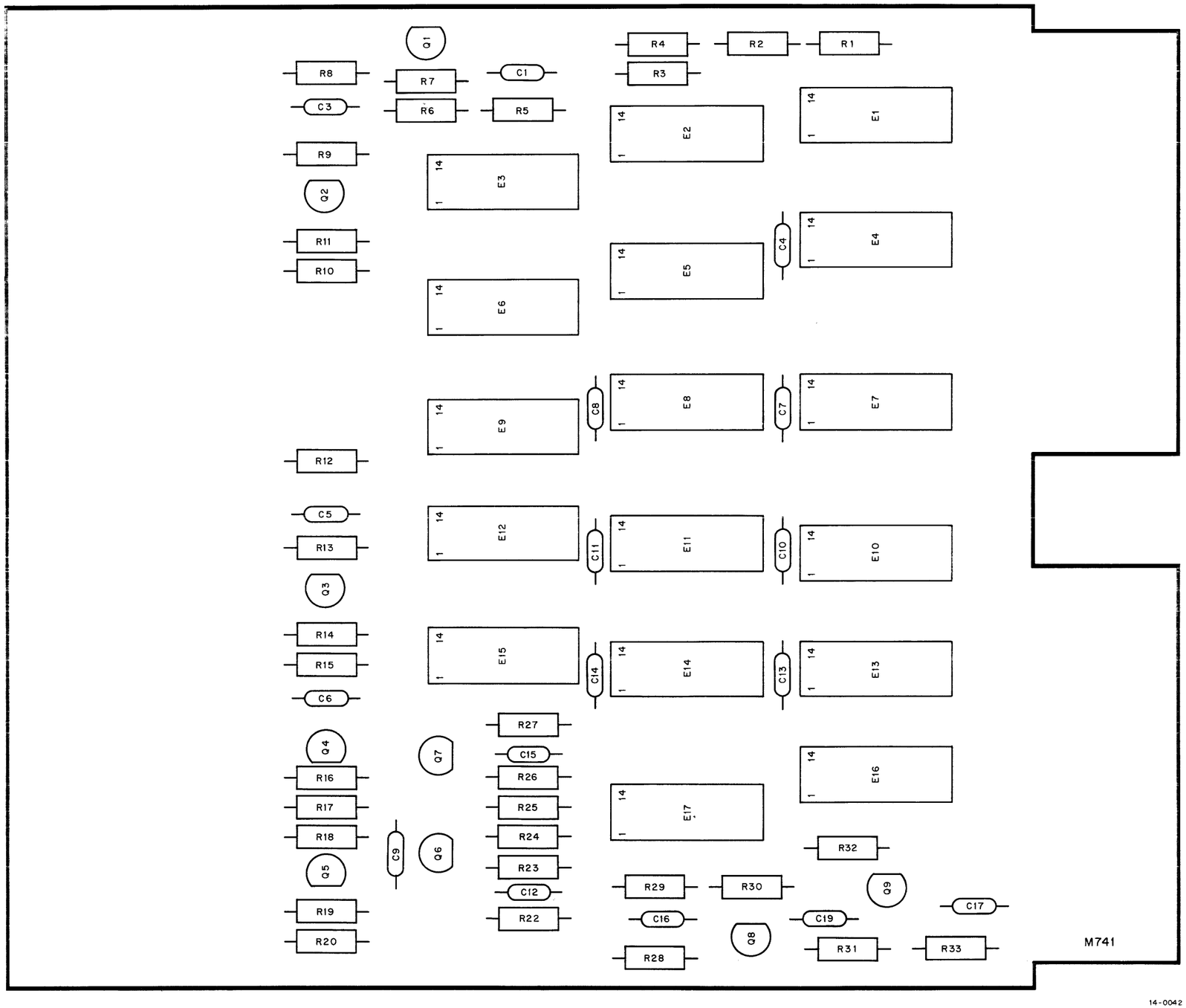
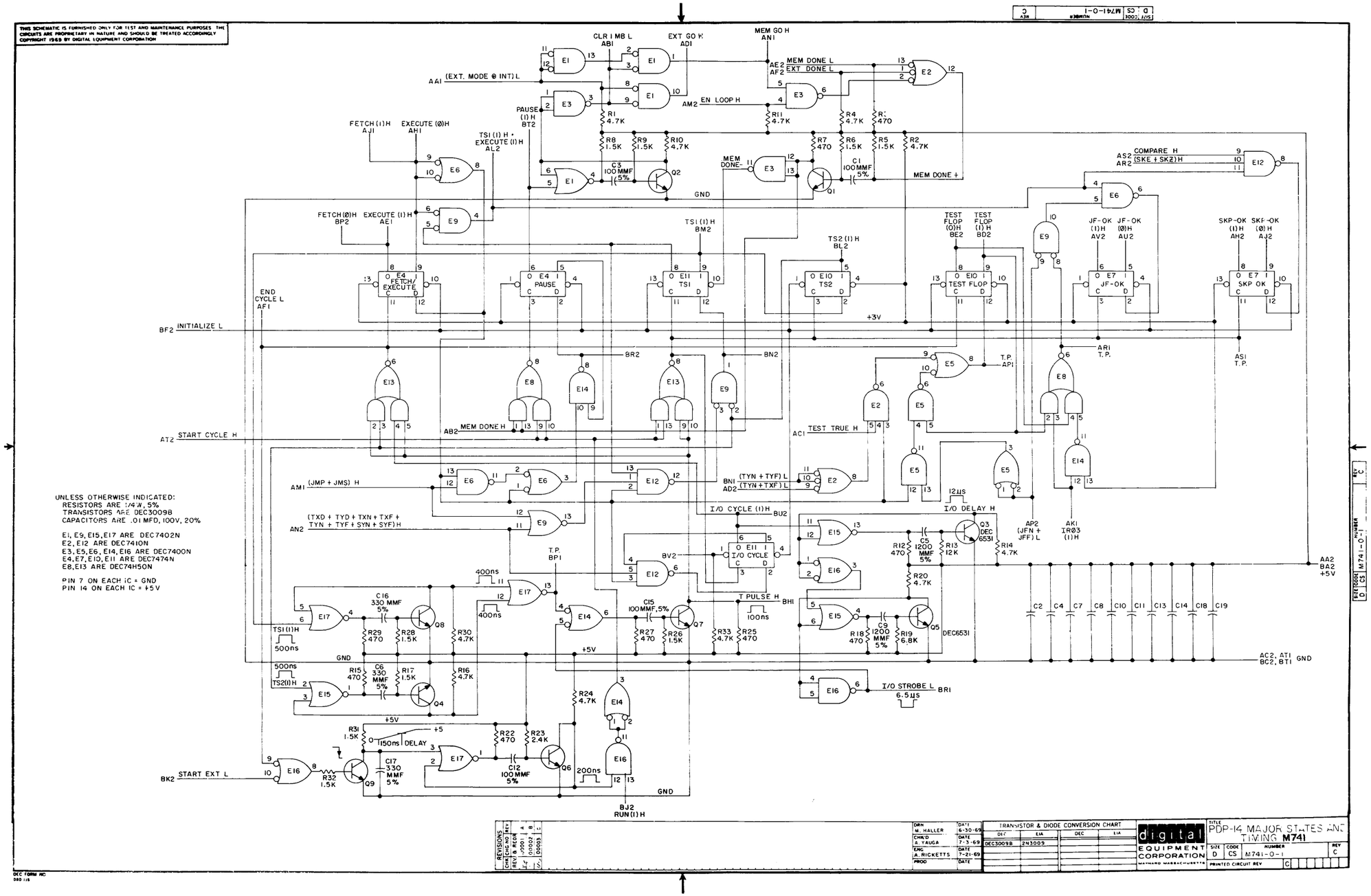
DECREMENT ENABLE H
INCREMENT ENABLE H
SOR-PC1 (4-11) H
SOR-PC1 (0-3) H
SOR-MB (4-11) H
SOR-MB (0-3) H
INT SYNC (0) H
MEM-60 H
MEM-60-MEM H
SOR-IR (4-11) H
SOR-IR (0-3) H
SOR-SPARE H
SOR-PC2 H
SOR-INPUT H
SKE ENABLE L
TYD L
TXD L
(EEM+LEM) L
TS1 FETCH L
LD-IR L
LD-MB L
LD-SPARE L
LD-PC1 L
LD-PC2 L
LD OUTPUT L
OUTPUT ENABLE L
LD14 BUS L
SPARE
PARTS LIST
ETCH BOARD REV B
SEMICONDUCTOR CONVERSION CHART
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
INSTRUCTION
DECODER & CONTROL
M7400-0-1


Q1
R8
R7
C1
R4
R2
R1
R3
C3
R6
R5
R9
E1
E2
E3
Q2
R11
R10
E4
C4
E5
E6
E7
E8
C8
C7
E9
R12
C5
E10
C11
E11
C10
E12
R13
Q3
R14
E13
C14
E14
C13
E15
R15
C6
R27
Q4
Q7
C15
E16
R16
R26
E17
R17
R25
R18
R24
R32
C9
Q6
R23
Q5
R29
R30
Q9
C17
C12
R19
R22
C16
C19
Q8
R20
R28
R31
R33
M741

14-0042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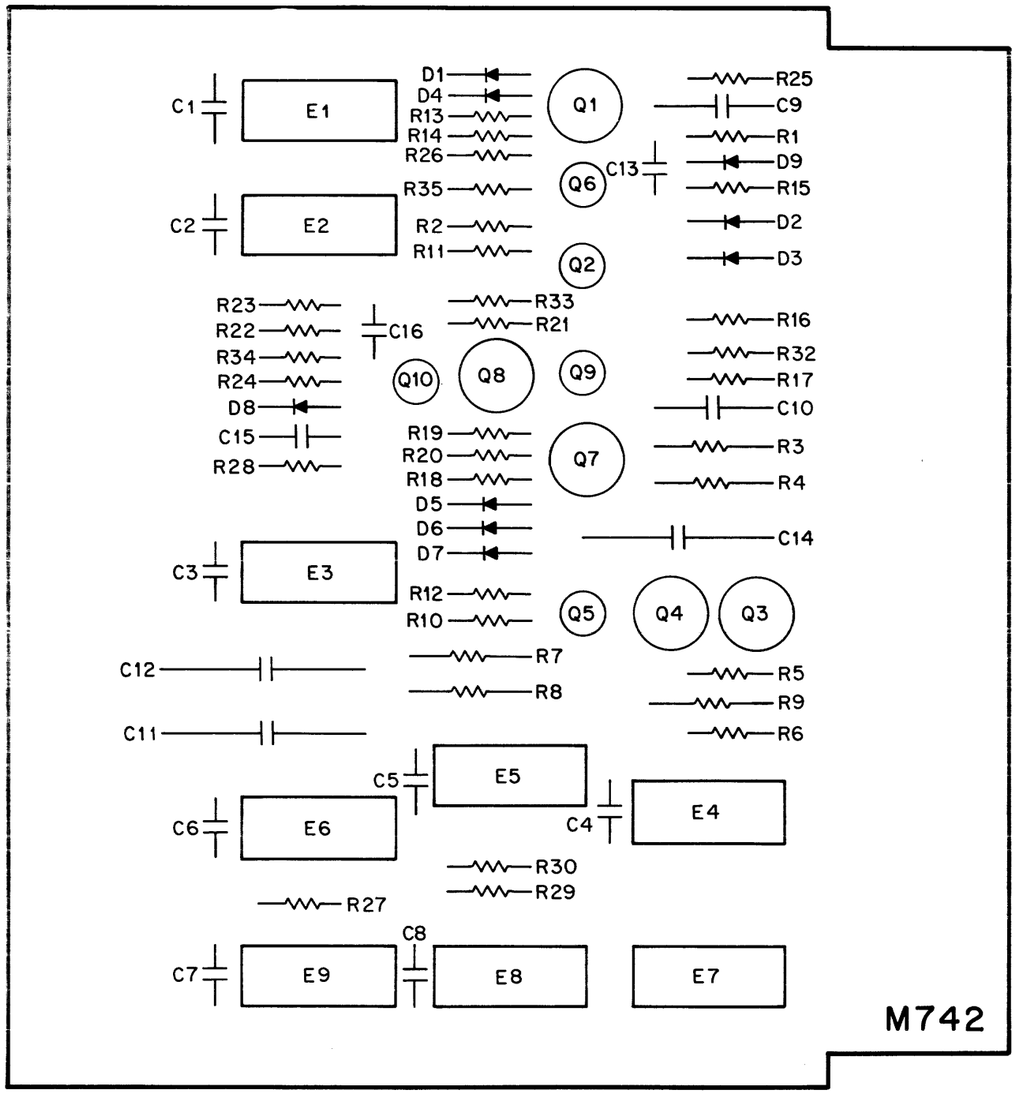
COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
TRANSISTORS ARE DEC3009B
CAPACITORS ARE .01 MFD, 100V, 20%
E1, E9, E15, E17 ARE DEC7402N
E2, E12 ARE DEC7410N
E3, E5, E6, E14, E16 ARE DEC7400N
E4, E7, E10, E11 ARE DEC7474N
E8, E13 ARE DEC74H50N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
TRANSISTOR & DIODE CONVERSION CHART
digital
EQUIPMENT CORPORATION
PDP-14 MAJOR STATES AND TIMING M741
M741-0-1


C1
E1
D1
D4
R13
R14
R26
Q1
R25
C9
R1
D9
R15
D2
D3
C13
Q6
R35
C2
E2
R2
R11
Q2
R23
R22
R34
R24
D8
C15
R28
C16
R33
R21
Q10
Q8
Q9
R16
R32
R17
C10
R19
R20
R18
D5
D6
D7
Q7
R3
R4
C14
C3
E3
R12
R10
Q5
Q4
Q3
C12
R7
R8
R5
R9
R6
C11
C5
E5
C6
E6
C4
E4
R30
R29
R27
C8
C7
E9
E8
E7
M742

14-0155

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RUN (I) H (AH2)
START L OR CONTINUE L
NODE A
SWITCH ON (AN2)
+5V POWER
NODE A
SWITCH ON (AN2)
SHUT DOWN L (BUI)
START EXT L
INITIALIZE H (BHI)

M742 TIMING

UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01 MFD, 100V, 20%
DIODES D672
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

E1 IS DEC7474N
E2,E6 ARE DEC7400N
E5,E7 ARE DEC7402N
E4 IS DEC7401N
E8 IS DEC7440N
RESISTORS ARE 1.8K, 1/4W, 10%
TRANSISTORS ARE DEC3009B
E9 IS DEC7410N
E3 IS DEC 9601

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606		
DEC2219A	2N2219A		
DEC3009B	2N3009B		
DEC6534D	MP36534		

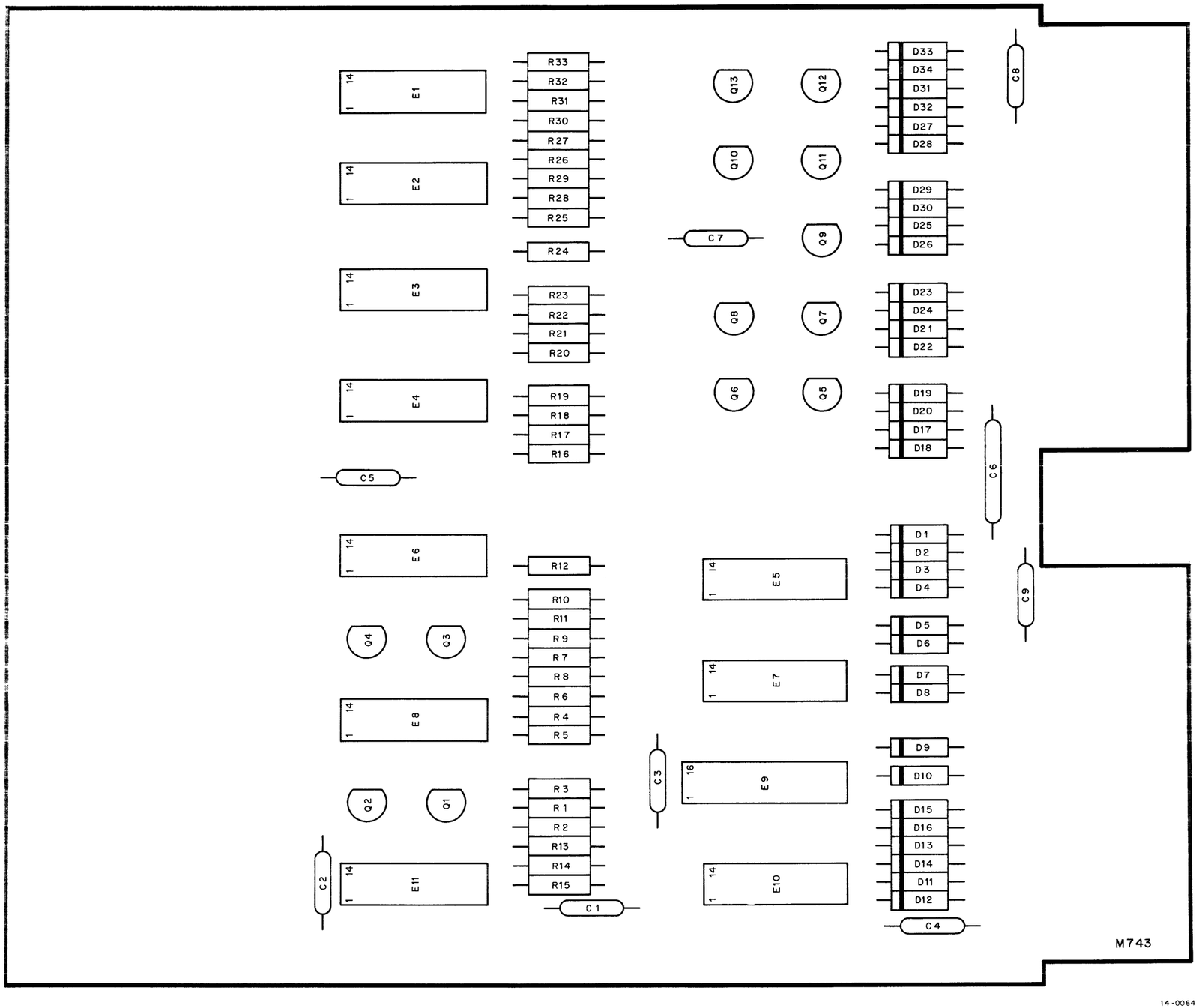
REVISIONS	CHK	CHG NO.	REV
REV. @ REDR		00001	A
		00002	D
		00003	E
		00004	H
		00005	J

DRN. BUTLER 6-17-69
CHK'D M. MARCHAND 6-20-69
ENG. A. RICKETTS 7-21-69
PROD

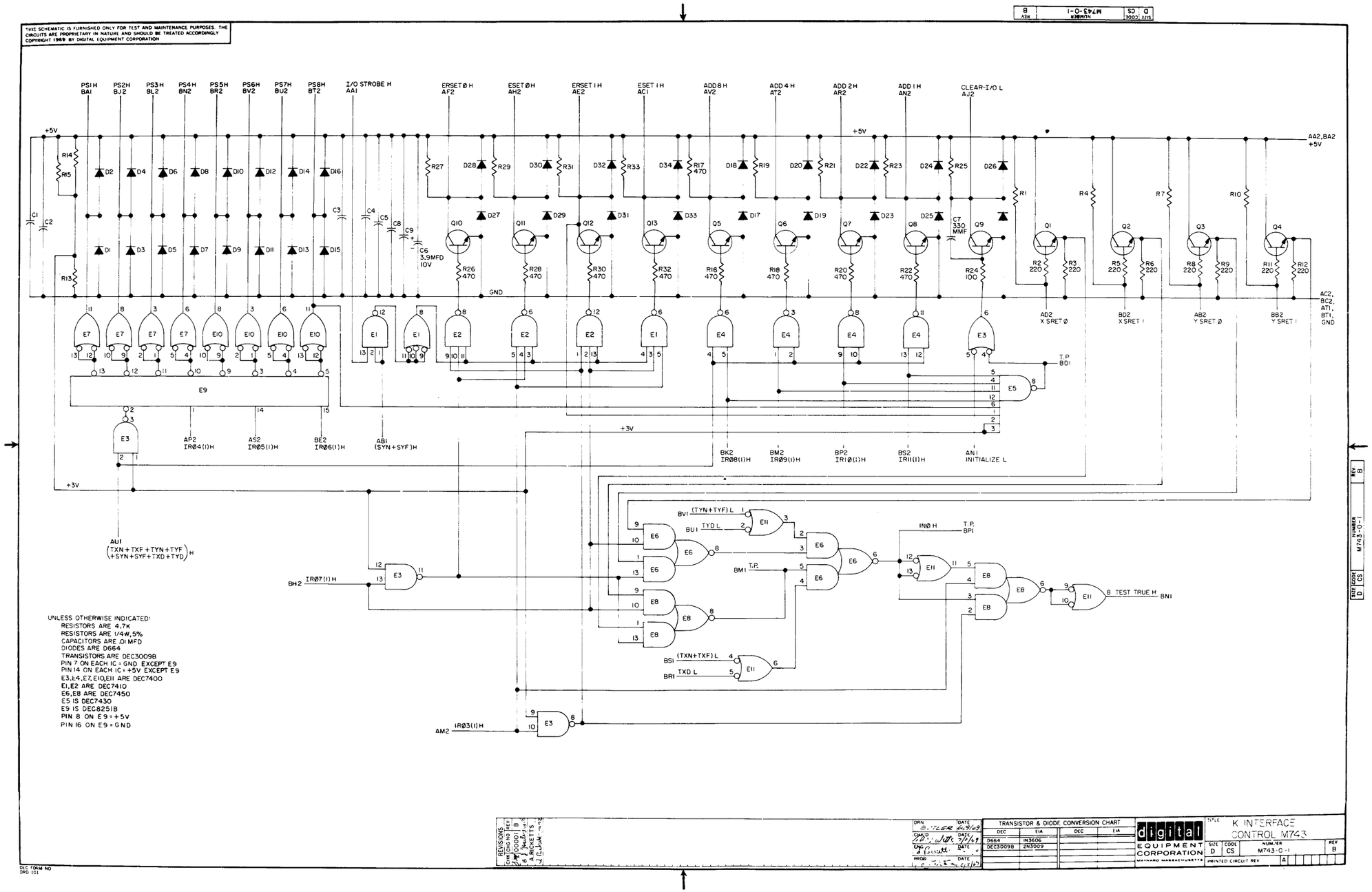
DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SWITCH AND POWER CONTROL M742
SIZE C | CODE CS | NUMBER M742-0-1 | REV J
PRINTED CIRCUIT REV. H

DEC FORM NO. DRC 102


E1
E2
E3
E4
E6
E8
E11
E5
E7
E9
E10
R33
R32
R31
R30
R27
R26
R29
R28
R25
R24
R23
R22
R21
R20
R19
R18
R17
R16
R12
R10
R11
R9
R7
R8
R6
R4
R5
R3
R1
R2
R13
R14
R15
Q13
Q12
Q10
Q11
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
D33
D34
D31
D32
D27
D28
D29
D30
D25
D26
D23
D24
D21
D22
D19
D20
D17
D18
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D15
D16
D13
D14
D11
D12
C1
C2
C3
C4
C5
C6
C7
C8
C9
M743

14-0064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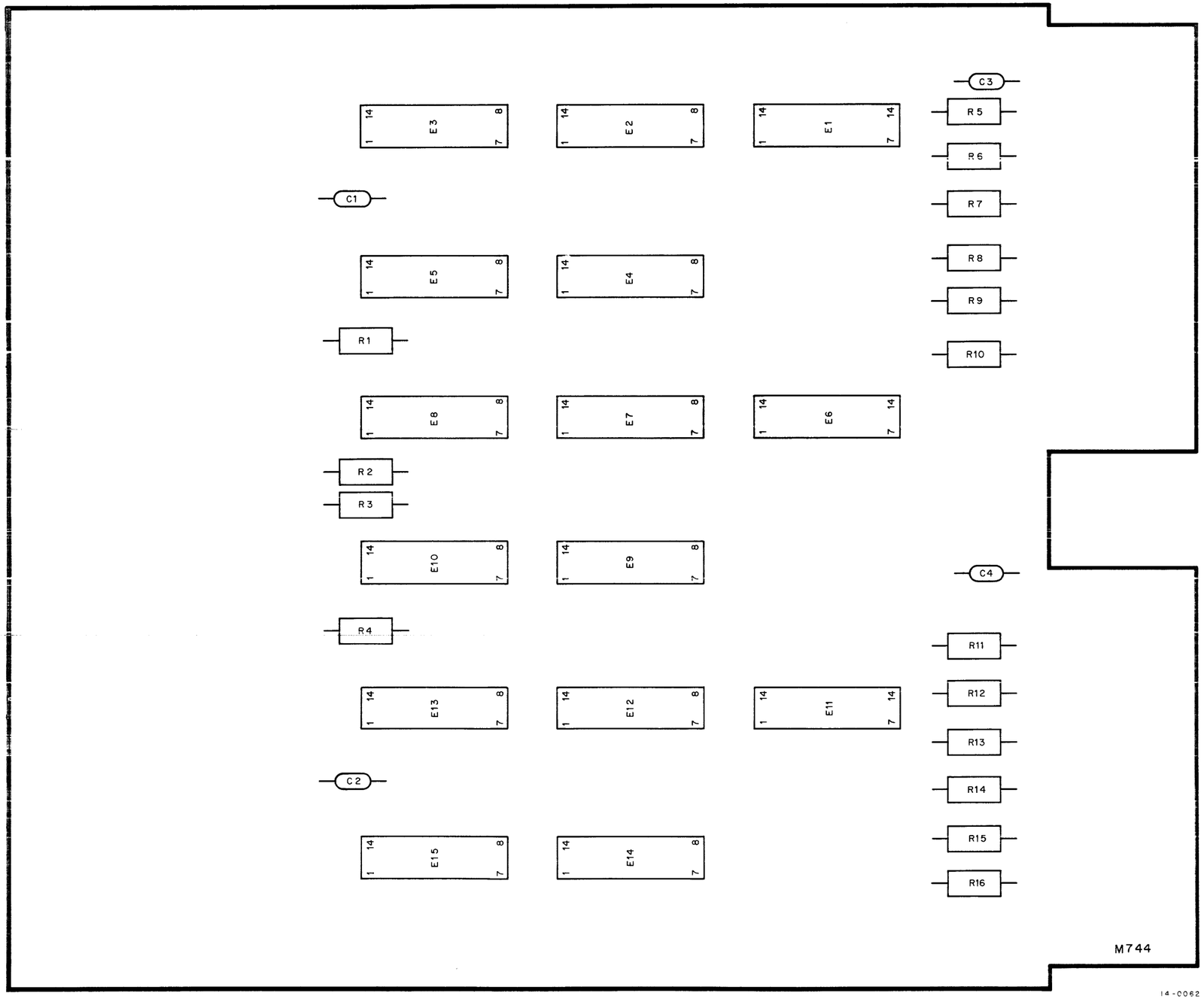
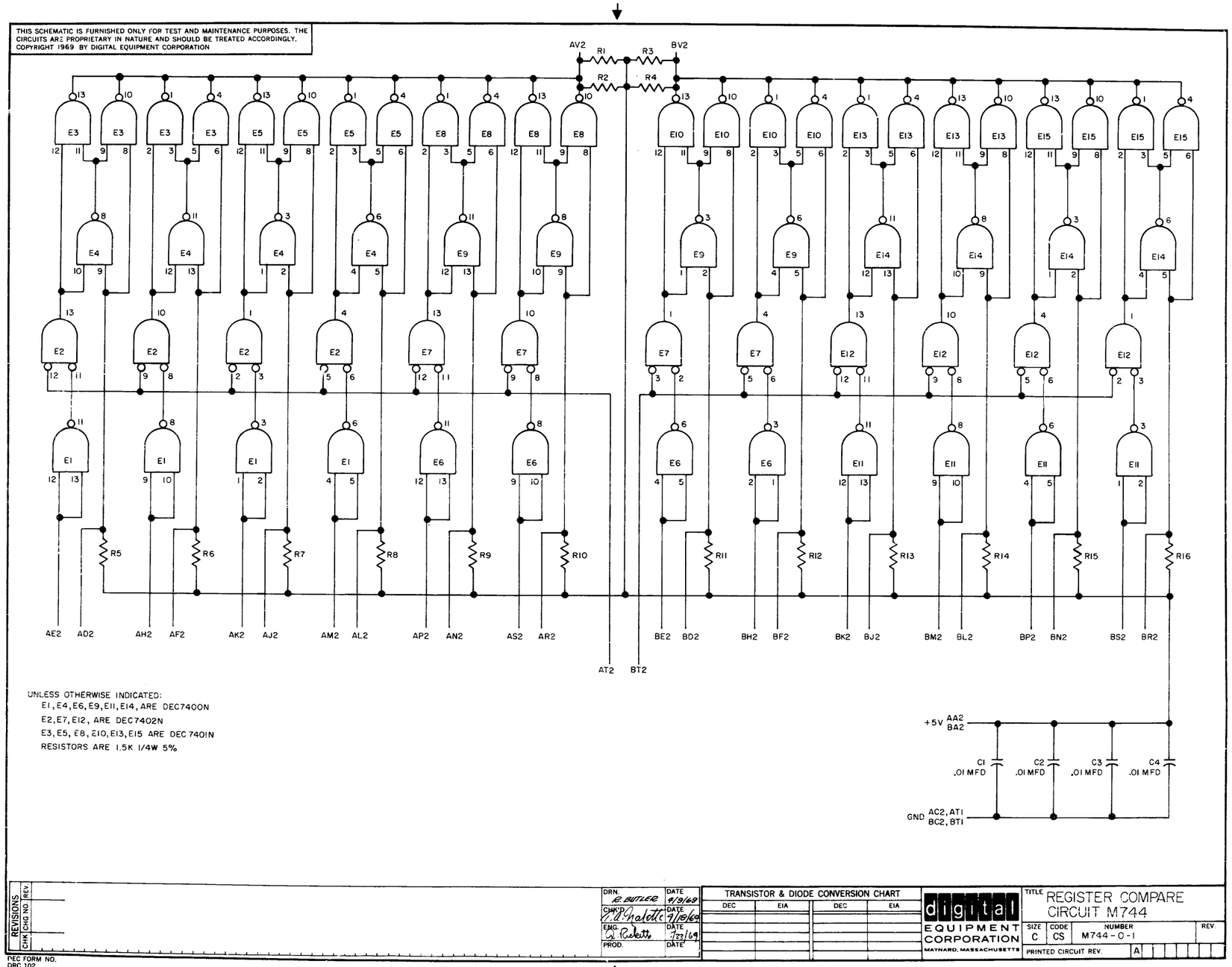
PS1H BA1
PS2H BJ2
PS3H BL2
PS4H BN2
PS5H BR2
PS6H BV2
PS7H BU2
PS8H BT2
I/O STROBE H AA1
ERSET Ø H AF2
ESET Ø H AH2
ERSET 1 H AE2
ESET 1 H AC1
ADD 8 H AV2
ADD 4 H AT2
ADD 2 H AR2
ADD 1 H AN2
CLEAR-I/O L AJ2
AA2,BA2 +5V
AC2, BC2, AT1, BT1, GND
AD2 X SRET Ø
BD2 X SRET 1
AB2 Y SRET Ø
BB2 Y SRET 1
T.P. BD1
AP2 IRØ4(1)H
AS2 IRØ5(1)H
BE2 IRØ6(1)H
AB1 (SYN+SYF)H
BK2 IRØ8(1)H
BM2 IRØ9(1)H
BP2 IRØ10(1)H
BS2 IR11(1)H
AN1 INITIALIZE L
AU1 (TXN+TXF+TYN+TYF +SYN+SYF+TXD+TYD) H
BH2 IRØ7(1)H
BV1 (TYN+TYF) L
BU1 TYD L
BM1 T.P.
BS1 (TXN+TXF) L
BR1 TXD L
INØ H
T.P. BP1
TEST TRUE H BN1
AM2 IRØ3(1)H
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 4.7K
RESISTORS ARE 1/4W,5%
CAPACITORS ARE .01 MFD
DIODES ARE D664
TRANSISTORS ARE DEC3009B
PIN 7 ON EACH IC = GND EXCEPT E9
PIN 14 ON EACH IC = +5V EXCEPT E9
E3,E4,E7,E10,E11 ARE DEC7400
E1,E2 ARE DEC7410
E6,E8 ARE DEC7450
E5 IS DEC7430
E9 IS DEC8251B
PIN 8 ON E9 = +5V
PIN 16 ON E9 = GND
TRANSISTOR & DIODE CONVERSION CHART
D664 IN3606
DEC3009B 2N3009
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
K INTERFACE CONTROL M743
SIZE D CODE CS NUMBER M743-0-1 REV B
PRINTED CIRCUIT REV A
REVISIONS
DRN B. TYLER DATE 6/9/69
CHKD DATE 7/1/69
DATE
APPD DATE
DEC FORM NO DRD 101


C3
R5
R6
R7
R8
R9
R10
E3
E2
E1
C1
E5
E4
R1
E8
E7
E6
R2
R3
E10
E9
C4
R4
R11
R12
R13
R14
R15
R16
E13
E12
E11
C2
E15
E14
M744

14-0062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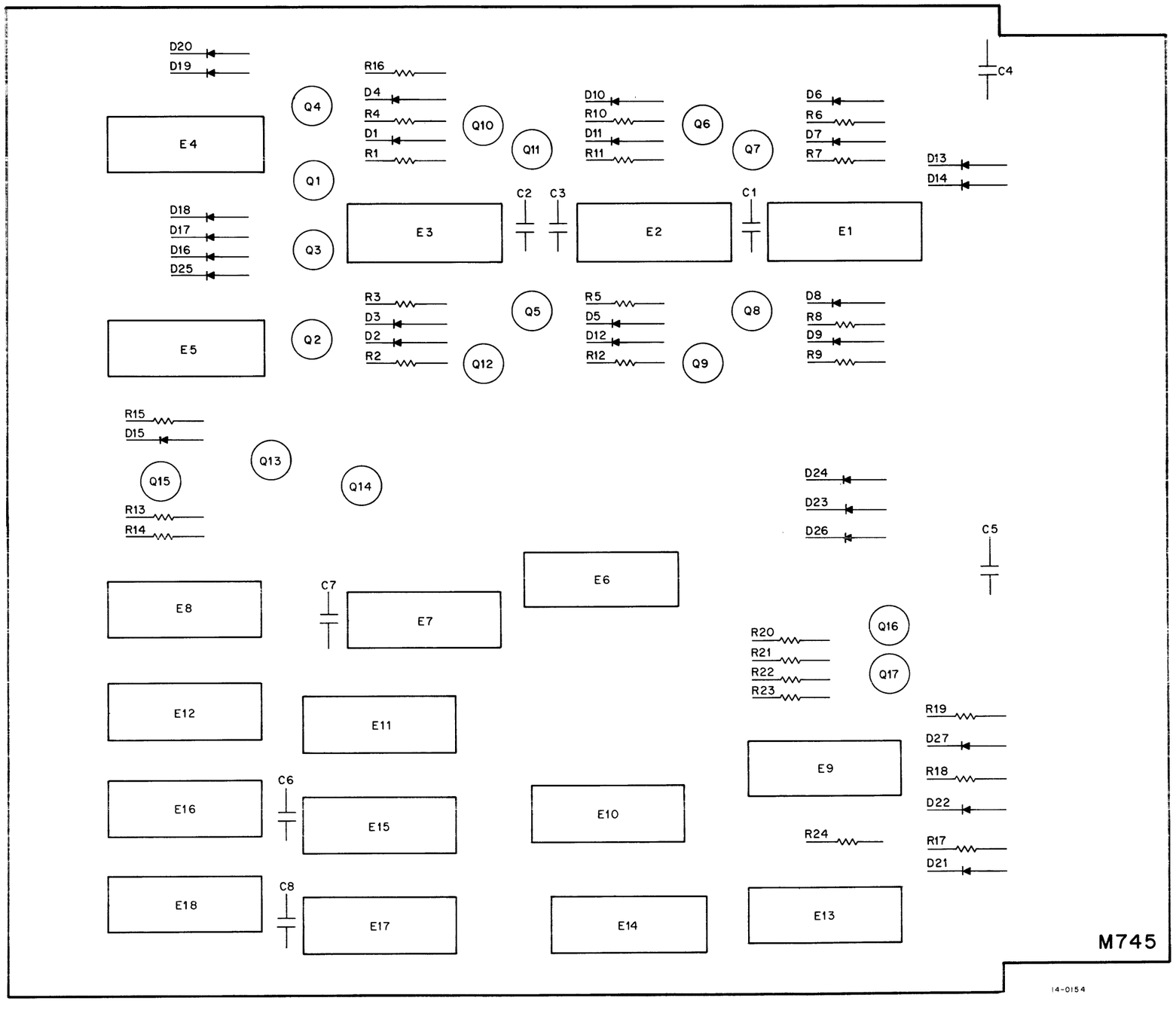
AV2
R1
R3
BV2
R2
R4
AE2 AD2 AH2 AF2 AK2 AJ2 AM2 AL2 AP2 AN2 AS2 AR2
AT2 BT2
BE2 BD2 BH2 BF2 BK2 BJ2 BM2 BL2 BP2 BN2 BS2 BR2
UNLESS OTHERWISE INDICATED:
E1, E4, E6, E9, E11, E14, ARE DEC7400N
E2, E7, E12, ARE DEC7402N
E3, E5, E8, E10, E13, E15 ARE DEC 7401N
RESISTORS ARE 1.5K 1/4W 5%
+5V AA2 BA2
C1 .01 MFD
C2 .01 MFD
C3 .01 MFD
C4 .01 MFD
GND AC2, AT1 BC2, BT1
REVISIONS
CHK CHG NO. REV.
DRN. R. BUTLER DATE 4/9/69
CHK'D 4/18/69
ENG. 7/23/69
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE REGISTER COMPARE CIRCUIT M744
SIZE C CODE CS NUMBER M744-0-1 REV.
PRINTED CIRCUIT REV. A
DEC FORM NO. DRC 102


D20
D19
R16
D4
R4
D1
R1
Q4
Q10
Q11
D10
R10
D11
R11
Q6
Q7
D6
R6
D7
R7
C4
D13
D14
E4
Q1
C2
C3
C1
D18
D17
D16
D25
E3
E2
E1
Q3
R3
D3
D2
R2
Q5
R5
D5
D12
R12
Q8
D8
R8
D9
R9
E5
Q2
Q12
Q9
R15
D15
Q13
Q15
Q14
R13
R14
D24
D23
D26
C5
E6
E8
C7
E7
Q16
R20
R21
R22
R23
Q17
E12
E11
R19
D27
R18
D22
R17
D21
E9
C6
E16
E15
E10
R24
E18
C8
E17
E14
E13
M745
14-0154

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SIZE D | CODE CS | NUMBER M745-0-1 | REV B

EXT. MODE (1) H BN1 | INT. SYNC (0) H BL2 | [EXT. MODE • INTERRUPT] BJ2 | LOAD OUTPUT L BT2 | EXT. FLAG (1) L BH2 | OUTPUT FLAG (1) L BH1

+5V AA2 BA2 | GND AC2, AT1 BC2, BT1 | C1 C2 C3 C4 C5 C6 C7 C8 | R16

BR1 INITIALIZE L

BV1 [TSI(1)·EXECUTE(1)] H
BU2 T PULSE H

9B2 END CYCLE L
AJ2 EXECUTE (0) H

BK1 IR04 (1) H
BF2 [EEM + LEM] H

BS2 INITIALIZE H
BS1 EXT. GO H

E17 EXT. MODE | E15 INT. SYNC | E17 EXT. FLAG | E15 INTERRUPT

T.P. BV2 | -IOT 165 | IOT 164 + IOT 165 | T.P. BL1

R20 R21 Q16 | R22 R23 Q17 | +5V | GND

EXT DONE L BF1 | LD MB EXT BD2

R24 | EN OUT DRIVER BN2 | IOT 162 LD-INPUT L BP1 | BE2 T.P.

AS2 BMB 07(0/1) H | ARI BMB 06(0/1) H | AR2 BMB 05(0/1) H | AN2 BMB 04(0/1) H | AL2 BMB 03(0/1) H
D16 D17 D18 D19 D20

BP2 IOP 4H | BM2 IOP 2H | AU1 BMB 11(1)H | AT2 BMB 09(1)H | AK1 BMB 08(1)H | AU2 BMB 10(1)H | BK2 IOP 1 H
D21 D22 D23 D24 D25 D26 D27
R17 100 10% | R18 100 10% | R19 100 10%

CODE 16 | CODE 17 | IOT 172 + IOT 176 (2)

BJ1 RUN (1) H | BM1 TEST FLOP (1) H

BE1 OUT 00 (1) H | AF1 OUT 01 (1) H | AC1 OUT 02 (1) H | AA1 OUT 03 (1) H | BB1 OUT 04 (1) H | AV2 OUT 05 (1) H | AV1 OUT 06 (1) H | AN1 OUT 07 (1) H | BA1 OUT 08 (1) H | AF2 OUT 09 (1) H | BD1 OUT 10 (1) H | BC1 OUT 11 (1) H IOT 176 (4)

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15

AC 00 L ABI | AC 01 L ADI | AC 02 L AEI | AC 03 L AHI | AC 04 L AJI | AC 05 L ALI | AC 06 L AMI | AC 07 L API | AC 08 L ASI | AC 09 L AD2 | AC 10 L AE2 | AC 11 L AH2 | INT. RQST L AM2 | CLR AC L AP2 | SKIP L AK2

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 470, 1/4W, 5%
TRANSISTORS ARE DEC3009B
DIODES ARE D664
CAPACITORS ARE .01 MFD, 100V, 20%

E1, E2, E3, E7 ARE MC3001 P
E4 IS DEC7430
E5, E10 ARE DEC7402
E6 IS DEC7404
E8, E11 ARE DEC7450
E9 IS DEC7440
E12, E16, E18 ARE DEC7400
E13, E14 ARE DEC7410
E15, E17 ARE DEC7474

PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REVISIONS: CHK CHG NO | REV | A RICH 1 10/69 | B

DRN R. CLEMENS	DATE 7-24-69	
CHK'D T.A. NALETTE	DATE 10-23-69	
ENG A. RICKETTS	DATE	
PROD	DATE	

TRANSISTOR & DIODE CONVERSION CHART

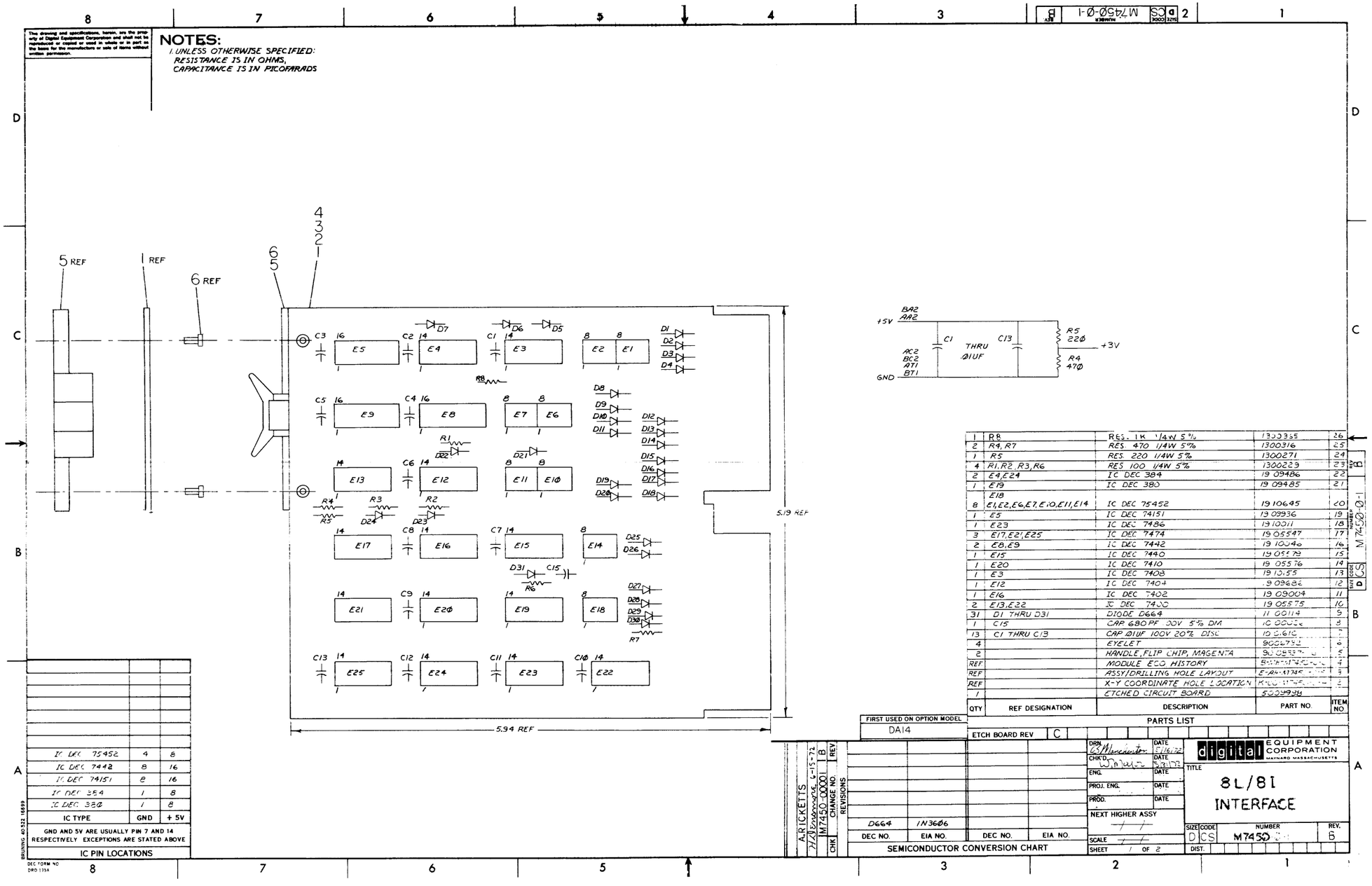
DEC	EIA	DEC	EIA
D664	IN3606		
DEC3009B	2N3009		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE PDP-14 TO PDP 8/L, 8/I INTERFACE M745

SIZE D | CODE CS | NUMBER M745-0-1 | REV B | PRINTED CIRCUIT REV E

DEC FORM NO. DRD 118



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	R8	RES. 1K 1/4W 5%	1300365	26
2	R4, R7	RES. 470 1/4W 5%	1300316	25
1	R5	RES. 220 1/4W 5%	1300271	24
4	R1, R2, R3, R6	RES 100 1/4W 5%	1300229	23
2	E4, E24	IC DEC 384	19 09486	22
1	E19	IC DEC 380	19 09485	21
8	E18 E1, E2, E6, E7, E10, E11, E14	IC DEC 75452	19 10645	20
1	E5	IC DEC 74151	19 09936	19
1	E23	IC DEC 7486	19 10011	18
3	E17, E21, E25	IC DEC 7474	19 05547	17
2	E8, E9	IC DEC 7442	19 10046	16
1	E15	IC DEC 7440	19 05579	15
1	E20	IC DEC 7410	19 05576	14
1	E3	IC DEC 7408	19 10155	13
1	E12	IC DEC 7404	19 09682	12
1	E16	IC DEC 7402	19 09004	11
2	E13, E22	IC DEC 7400	19 05575	10
31	D1 THRU D31	DIODE D664	11 00114	9
1	C15	CAP 680PF 100V 5% DM	10 00006	8
13	C1 THRU C13	CAP .01UF 100V 20% DISC	10 01610	7
4		EYELET	9002732	6
2		HANDLE, FLIP CHIP, MAGENTA	90 08337	5
REF		MODULE ECO HISTORY	[illegible]	4
REF		ASSY/DRILLING HOLE LAYOUT	E-AH-M745[illegible]	3
REF		X-Y COORDINATE HOLE LOCATION	[illegible]	2
1		ETCHED CIRCUIT BOARD	5009998	

PARTS LIST

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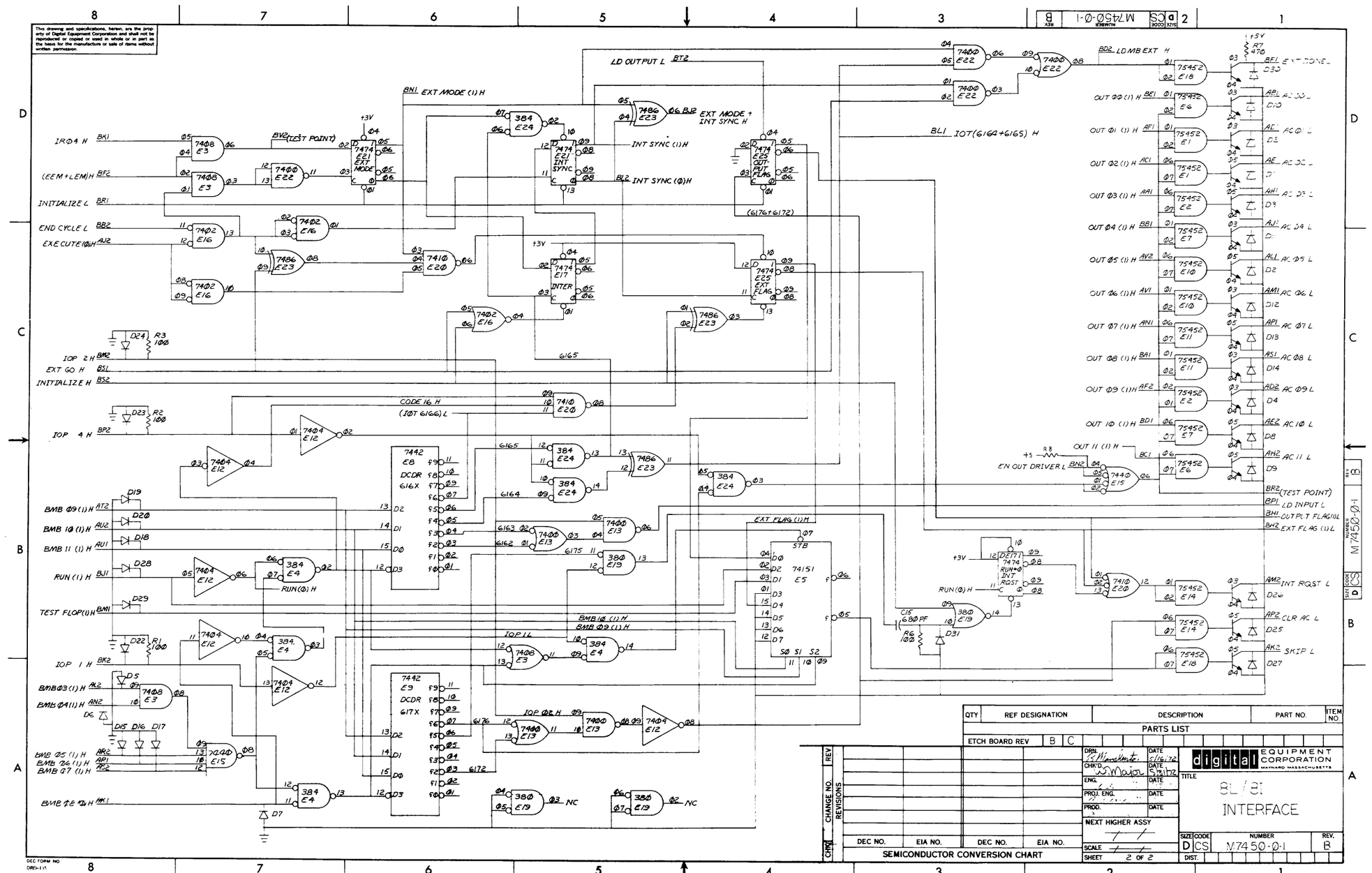


QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		
	ETCH BOARD REV	B C		

REV	CHANGE NO.	DEC NO.	EIA NO.	DEC NO.	EIA NO.
	REVISIONS	SEMICONDUCTOR CONVERSION CHART			

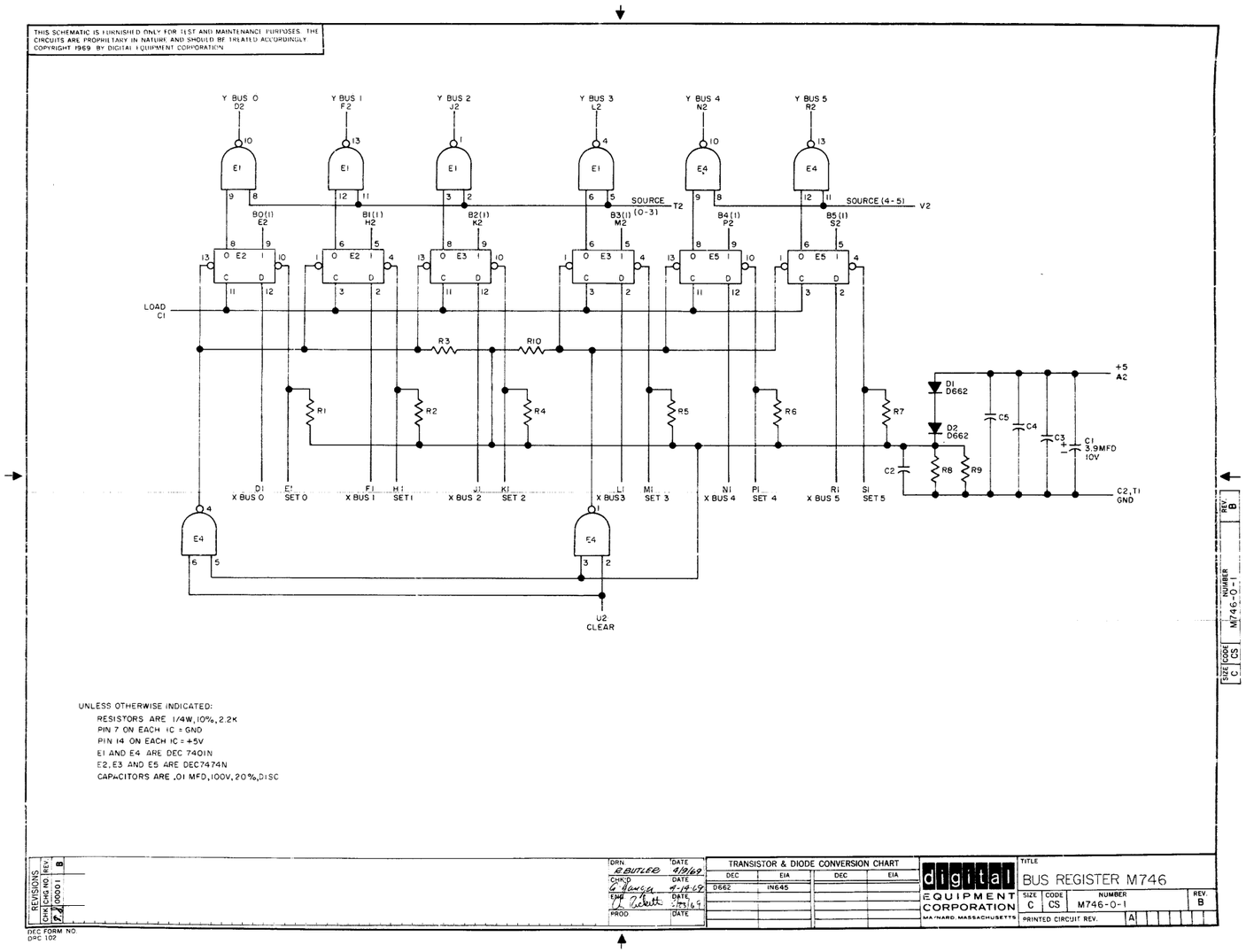
DRN. K.Manente DATE 6/16/72
CHK'D S.Major DATE 5/31/72
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
NEXT HIGHER ASSY
SCALE
SHEET 2 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE 8L/8I INTERFACE

SIZE	CODE	NUMBER	REV.
D	CS	M7450-0-1	B
DIST.			

DEC FORM NO DRD-111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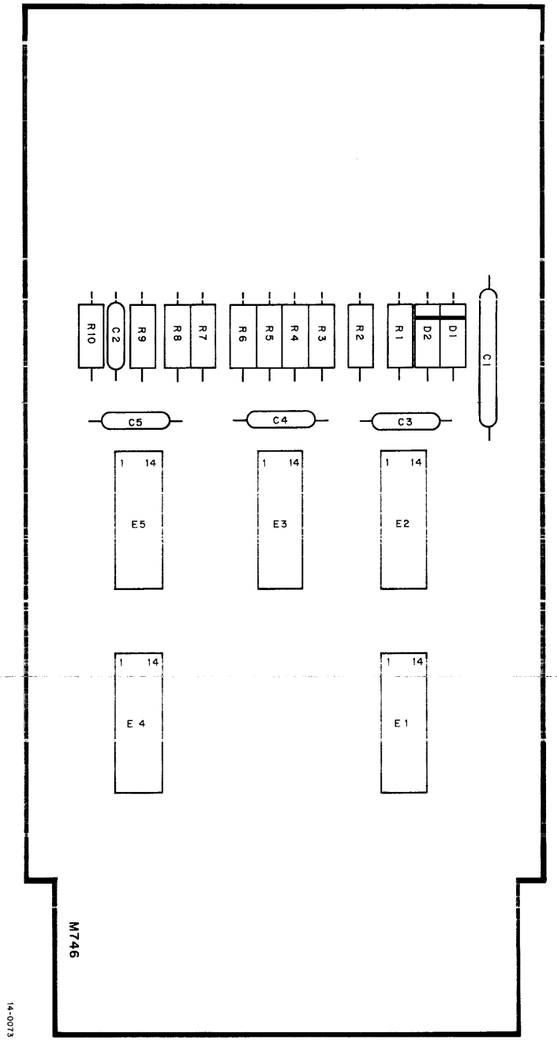
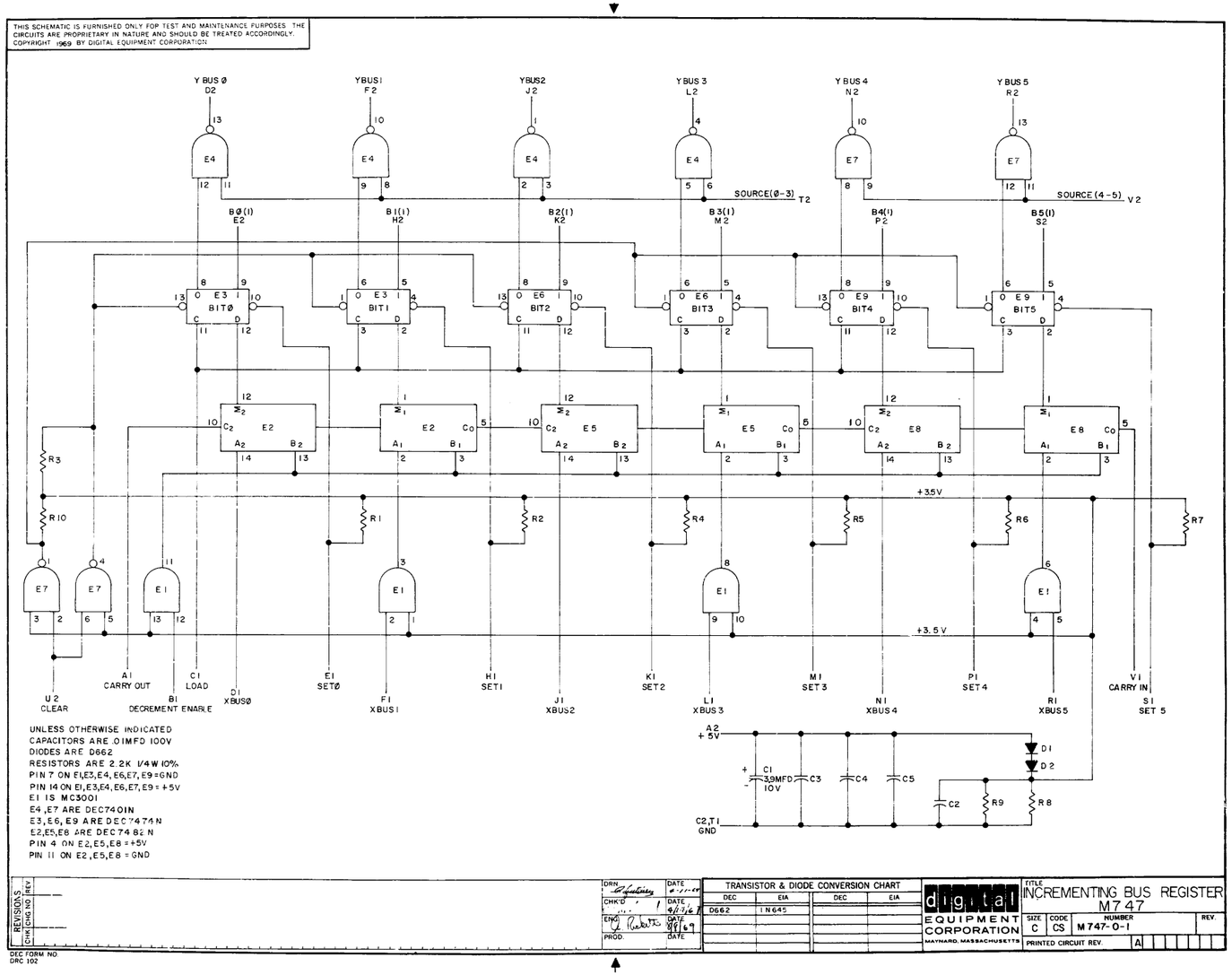
Y BUS 0 D2
Y BUS 1 F2
Y BUS 2 J2
Y BUS 3 L2
Y BUS 4 N2
Y BUS 5 R2
SOURCE (0-3) T2
SOURCE (4-5) V2
LOAD C1
+5 A2
C2, T1 GND
U2 CLEAR
D1 D662
D2 D662
C1 3.9MFD 10V
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%, 2.2K
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1 AND E4 ARE DEC 7401N
E2, E3 AND E5 ARE DEC7474N
CAPACITORS ARE .01 MFD, 100V, 20%, DISC
REVISIONS
DRN R BUTLER DATE 4/9/69
CHK'D G Hanson DATE 4-14-69
ENG R Ackett DATE 5/23/69
PROD DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
D662 IN645
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE BUS REGISTER M746
SIZE C CODE CS NUMBER M746-0-1 REV. B
PRINTED CIRCUIT REV. A
DEC FORM NO. DPC 102


R10 C2 R9 R8 R7 R6 R5 R4 R3 R2 R1 D2 D1 C1
C5 C4 C3
E5 E3 E2
E4 E1
M746
14-0073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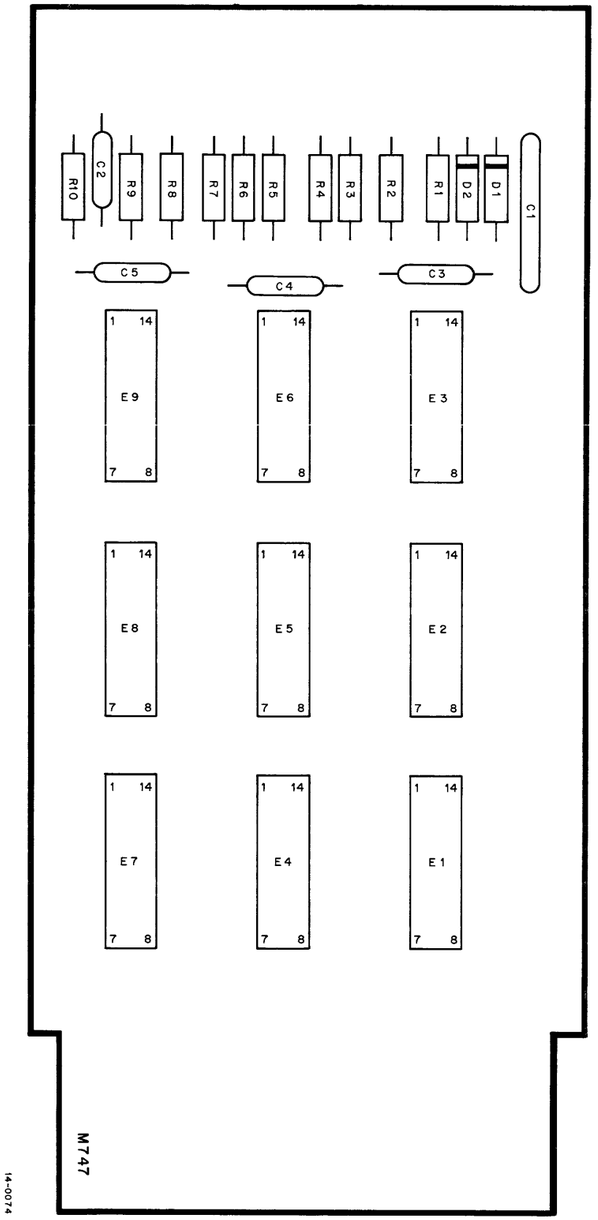
Y BUS Ø D2
YBUS1 F2
YBUS2 J2
Y BUS 3 L2
Y BUS 4 N2
Y BUS 5 R2
SOURCE(Ø-3) T2
SOURCE (4-5) V2
BØ(1) E2
B1(1) H2
B2(1) K2
B3(1) M2
B4(1) P2
B5(1) S2
BITØ
BIT1
BIT2
BIT3
BIT4
BIT5
+3.5V
U2 CLEAR
A1 CARRY OUT
B1 DECREMENT ENABLE
C1 LOAD
D1 XBUSØ
E1 SETØ
F1 XBUS1
H1 SET1
J1 XBUS2
K1 SET2
L1 XBUS3
M1 SET3
N1 XBUS4
P1 SET4
R1 XBUS5
V1 CARRY IN
S1 SET 5
A2 +5V
C1 3.9MFD 10V
C2,T1 GND
UNLESS OTHERWISE INDICATED
CAPACITORS ARE .01MFD 100V
DIODES ARE D662
RESISTORS ARE 2.2K 1/4W 10%
PIN 7 ON E1,E3,E4,E6,E7,E9 = GND
PIN 14 ON E1,E3,E4,E6,E7,E9 = +5V
E1 IS MC3001
E4,E7 ARE DEC7401N
E3,E6,E9 ARE DEC7474N
E2,E5,E8 ARE DEC7482N
PIN 4 ON E2,E5,E8 = +5V
PIN 11 ON E2,E5,E8 = GND
REVISIONS
DEC FORM NO. DRC 102
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
D662 1N645
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE INCREMENTING BUS REGISTER M747
SIZE C CODE CS NUMBER M747-0-1 REV.
PRINTED CIRCUIT REV. A


R10
C2
R9
R8
R7
R6
R5
R4
R3
R2
R1
D2
D1
C1
C5
C4
C3
E9
E6
E3
E8
E5
E2
E7
E4
E1
M747

14-0074

SIZE	CODE	NUMBER	REV.
B	CS	M921-0-1	

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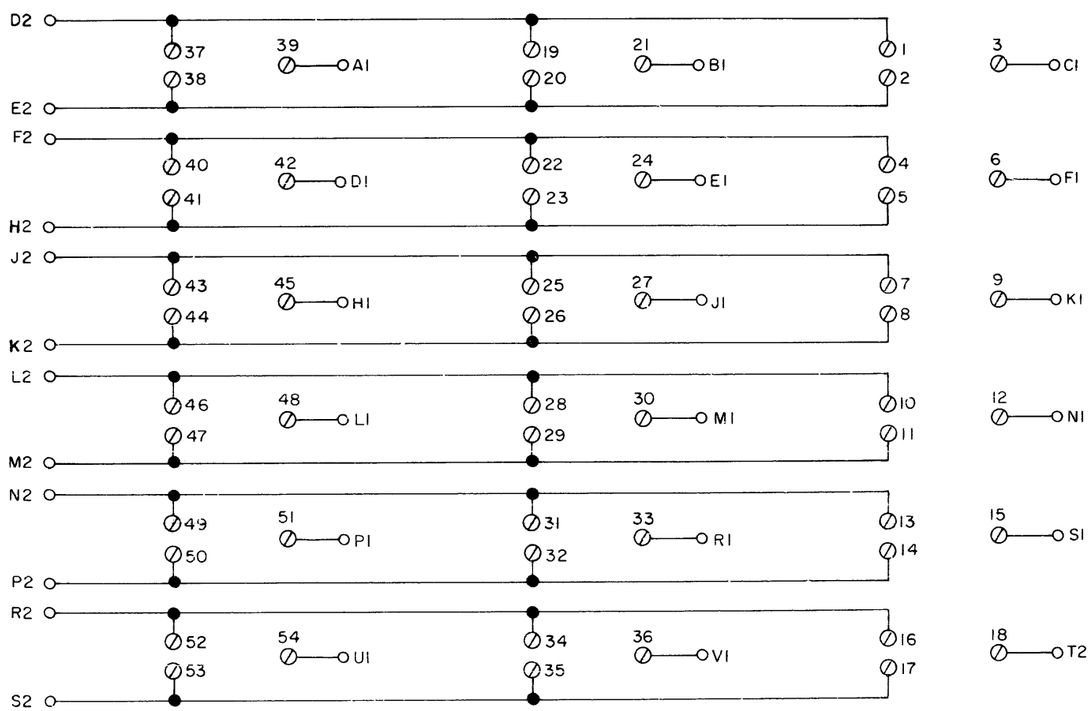
PIN SIGNAL ASSIGNMENTS

OUT			
DEVICE A	DEVICE B	DEVICE C	SIGNAL
AI	BI	CI	MB3
DI	EI	FI	MB4
HI	JI	KI	MB5
LI	MI	NI	MB6
PI	RI	SI	MB7
UI	VI	T2	MB8

IN	
D2	MB3(0)
E2	MB3(1)
F2	MB4(0)
H2	MB4(1)
J2	MB5(0)
K2	MB5(1)
L2	MB6(0)
M2	MB6(1)
N2	MB7(0)
P2	MB7(1)
R2	MB8(0)
S2	MB8(1)



UNLESS OTHERWISE INDICATED:
⌀ ARE SPLIT LUGS

REVISIONS	REV.	CHG NO.	CHK

DRN.	BUTLER	DATE 11/16/69
CHK'D	C.U. Galette	DATE 9/20/69
ENG.	D Scanlon	DATE 9/20/69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

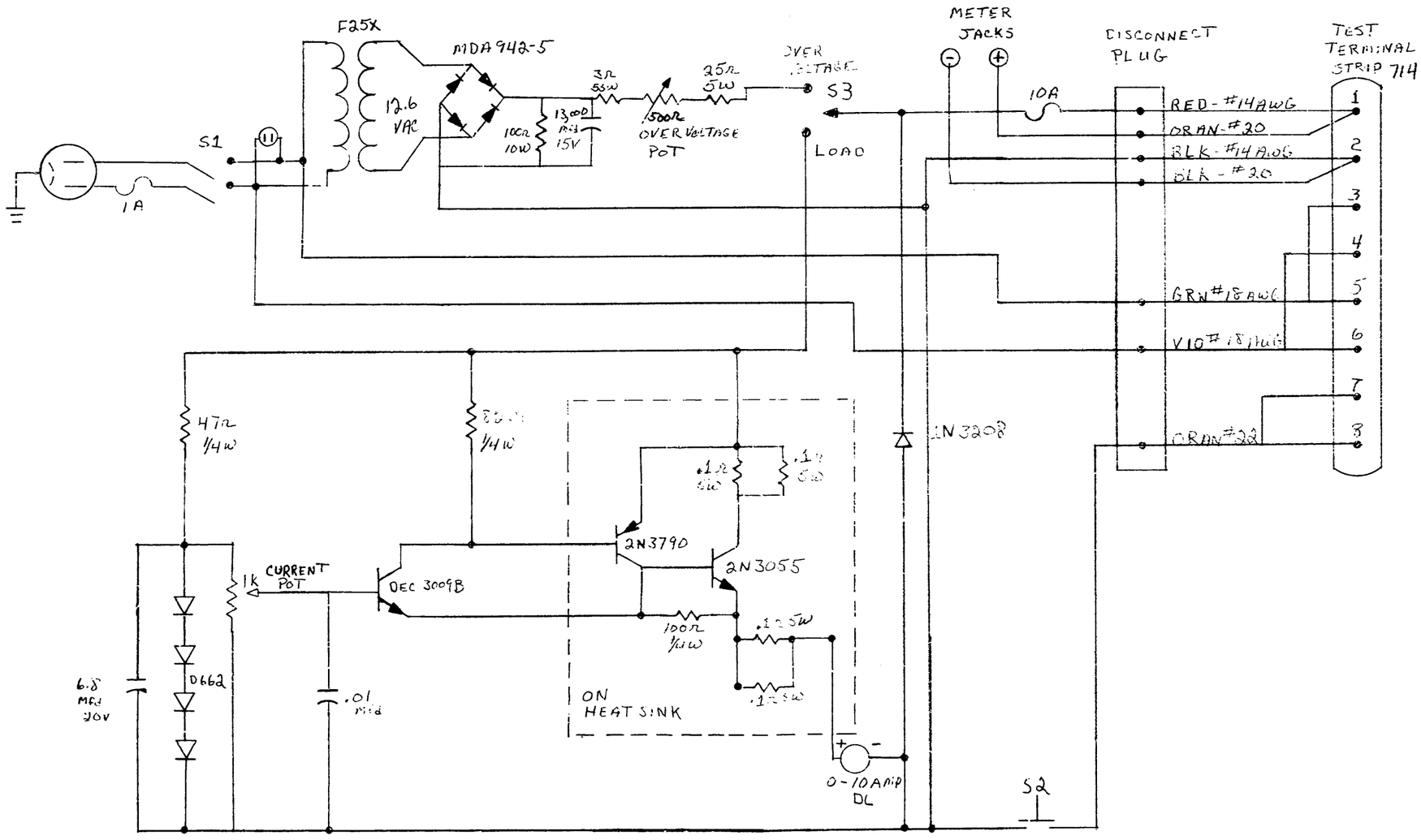
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE DEVICE CODE SELECT JUMPER BOARD

SIZE	CODE	NUMBER	REV.
B	CS	M921-0-1	

PRINTED CIRCUIT PEV. B

DEC FORM NO. DRB 102


F25X
MDA942-5
12.6 VAC
3Ω 5W
25Ω 5W
OVER VOLTAGE
S3
1500Ω OVER VOLTAGE POT
100Ω 10W
1300Ω 1/4W 15V
LOAD
METER JACKS
DISCONNECT PLUG
TEST TERMINAL STRIP 714
10A
RED - #14AWG
ORAN - #20
BLK - #14AWG
BLK - #20
GRN #18AWG
VIO #18AWG
ORAN #20
S1
1A
47Ω 1/4W
1N3209
.1Ω 5W
2N3790
2N3055
1k CURRENT POT
DEC 3009B
100Ω 1/4W
.1Ω 5W
.1Ω 5W
D662
6.8 MFD 30V
.01 MFD
ON HEAT SINK
0-10AMP DC
S2

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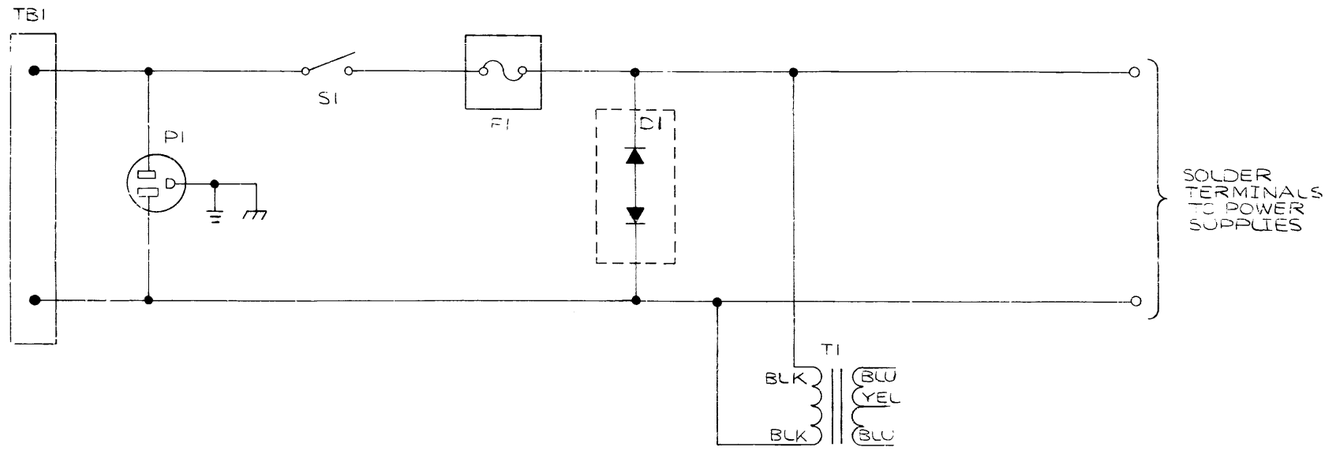

REF DESIGNATION	DESCRIPTION	PART NO.
T1	TRANS F25-X	1601347
D1	THYRACTOR 6RS20SP9B9	1102915
F1	FUSE HOLD. 440	9006996
S1	SW #866-5 SMITH	1201199
P1	SOCKET 160-4	1201251
TB1	TERMINAL STRIP	207596

PARTS LIST

REVISIONS

CHK	CHG NO	REV

DRN — DATE 2-24-69
CHK'D — DATE 5/19/69
ENG — DATE 5/23/69
PROD — DATE 6-3-69

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE POWER SUPPLY FILTER CIRCUIT

SIZE C | CODE CS | NUMBER 7006314-0-1 | REV B

PRINTED CIRCUIT REV

DEC FORM NO DRC 102

SIZE C | CODE CS | NUMBER 7006314-0-1 | REV B

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PDP-14 MAINTENANCE MANUAL
DEC-14-HGZB-D

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What faults do you find with the manual? _____

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