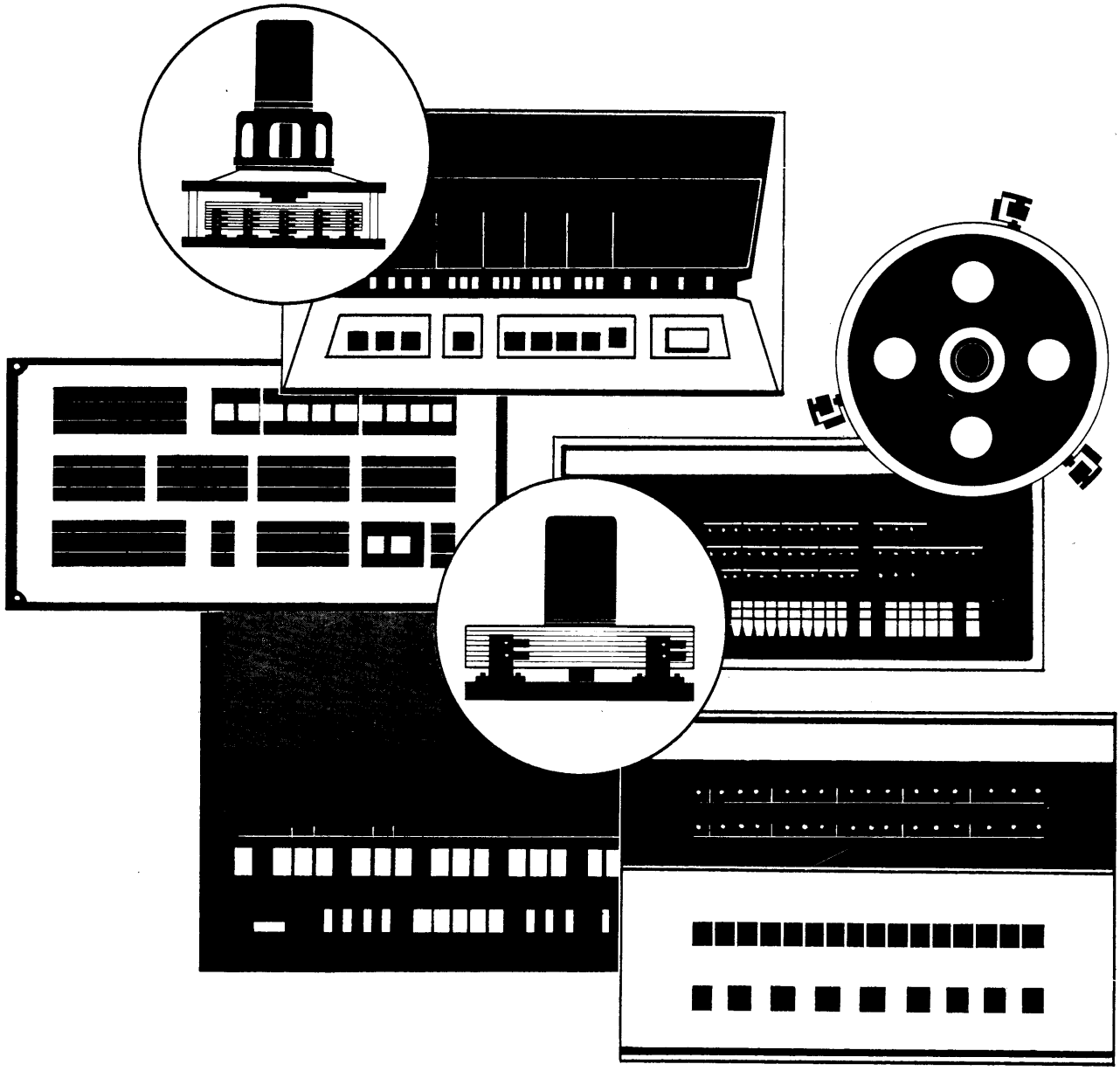
DATUM

CALIFORNIA PERIPHERALS DIVISION

SERIES 88 MASS MEMORY SYSTEMS INSTRUCTION MANUAL



DATUM INC.
CALIFORNIA PERIPHERALS DIVISION

SERIES 88 DRUM MEMORY
INSTRUCTION MANUAL

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SECTION I GENERAL INFORMATION

1-1. INTRODUCTION

This instruction manual pertains to the following Series 88 Drum Memory Models: 388, 688, and 788. The Model 588 Drum Memory is covered in a separate manual.

Each Drum Memory consists of a mechanical unit, associated read/write and track selection electronics, and a power supply. The mechanical unit provides a rotating drum, drum drive motor, and a flying read/write head for each data track and for the clock track. A rhodium plated nickel-cobalt drum is used.

Individual models within the series differ in the number of data tracks, in drum rotational speeds, in bit transfer rates, and in bit storage capacities.

1-2 SPECIFICATIONS

Table 1-1 summarizes the specifications for the three Drum Memory models covered by this instruction manual.

1-3 ACCESSORIES AND OPTIONS

Standard units require 115-volt, 60 Hz, single phase power for operation of the drum motor and of the power supply. Optionally, units which operate on 230 volts, 50 Hz can be supplied.

1-4 PHYSICAL CHARACTERISTICS

Series 88 Drum Memory units are designed for mounting in standard 19-inch RETMA racks. A base structure provides the facility for mounting the mechanical unit, a circuit card module, and the power supply.

The mechanical unit provides the drum, drum drive, heads, and also a portion of the associated electronics. The drum drive motor is mounted above the drum. The flying head assemblies are provided on post assemblies mounted around the periphery of the drum. Adjacent to each post assembly is a diode matrix board which provides diodes and pull-down resistors used in selecting the heads on the post assembly. Also mounted within the drum enclosure are a clock preamplifier circuit board and either one or two read/write select circuit boards (one for every 32 tracks). Location of components within the mechanical unit is illustrated in Figure 1-1.

A cover fits over the drum enclosure creating a protected environment for the drum and heads. During assembly of the unit at the factory, the cover is installed and sealed in a white room.

A read amplifier is mounted on the mechanical unit outside of the drum chamber. The remaining electronics for the unit is provided by three circuit boards accommodated by the circuit card module. These are the encode-decode circuit board, the timing circuit board, and the track selection circuit board. The circuit card module provides additional space for the mounting of drum controller circuit boards. Location of components outside the drum chamber is illustrated in Figure 1-2.

Figure 1-3 illustrated the overall dimensions of the Drum Memory.

1-5. WARRANTY

DATUM, Inc. guarantees this equipment to be free from defects in material and workmanship, for one year from date of delivery. Any repairs, or replacements (which alternative chosen by the manufacturer) will be carried out at the facilities of DATUM with transportation costs charged to the purchaser's account. Should a defect occur in equipment which cannot be returned feasibly because of physical size, or should the defect be trivial, the purchaser will be expected to perform first echelon repairs using materials supplied by DATUM. Subsequent repairs within the period of warranty will be negotiated separately.

If a defect should result from a design error, and both DATUM and the purchaser recognize this error as the cause of the defect, DATUM will correct the error to meet the specifications under which the equipment was delivered.

DATUM retains the right to return the defective equipment to the company's facilities for repair should this course be deemed necessary or advisable.

Equipment, accessories, batteries, and similar items not manufactured by DATUM are subject only to adjustments as can be obtained from the original supplier by DATUM. This warranty does not apply to any equipment, or portion thereof, which becomes defective through misuse, mishandling, or environmental conditions exceeding specifications, after delivery.

No other warranties, expressed or implied, shall apply to any equipment sold under this warranty, and the foregoing shall constitute the purchaser's sole rights under the agreed terms of this warranty.

In no circumstance shall DATUM assume liability for loss, damage or consequential expense arising directly or indirectly from the use of its equipment, separately, or in combination with other equipment.

TABLE 1-1
SERIES 88 DRUM MEMORY SPECIFICATIONS

PARAMETER						
	388		688		788	
SPEED	1800	3600	1800	3600	1800	3600
Bit Transfer Rate	1.5 mHz	1.9 MHz	1.5	1.9	1.5	2.1
Bits Per Track	50,000	32,000	50,000	32,000	50,000	36,500
Bit Storage Capacity	800K	512K	1.6M	1.0M	3.2M	2.3M
Bits Per Inch	2000	1280	1790	1140	1790	1300
Data Tracks	16	16	32	32	64	64
Clock Tracks	1	1	1	1	1	1
Sectors Per Track	Hardware-programmed at factory in accordance with customer specifications – All models					
Read/Write Mode	Bit/ Serial	Bit/ Serial	Bit/ Serial	Bit/ Serial	Bit/ Serial	Bit/ Serial
Recording Method	FM	FM	FM	FM	FM	FM
Data Interface	NRZ	NRZ	NRZ	NRZ	NRZ	NRZ
Interface Circuit	T^2L	T^2L	T^2L	T^2L	T^2L	T^2L
Drive Source	Hys Syn	Hys Syn	Hys Syn	Hys Syn	Induc.	Induc.
50 Hz Available	Yes	Yes	Yes	Yes	No	No
D.C. Power						
+25 volts ±5% (amps)		.5		.5		.5
+12 volts ±5% (amps)		—		—		—
+ 5 volts ±5% (amps)		1.5		1.5		2.0
– 5 volts ±5% (amps)		—		—		—
–15 volts ±5% (amps)		.3		.3		.3
A.C. Power (Drive)						
115V ±5% 1ϕ, 60 Hz±Hz						
Start Current (amps)		1,5		3,3		3,3
Write/Read Recovery (us)		30		30		30
Read/Write Recovery (us)						
Track Switch Recovery (us)		5		5		5
Pre-amble Bits		7		7		7
Post-amble Bits		3		3		3
Signal Levels						
Logical One (volts)		+0.5		+0.5		+0.5
Logical Zero (volts)		+4.0		+4.0		+4.0
Head Inductance (mh)		10		10		10
Head Load (ohms)		1000		1000		1000
Write Current (ma)		60-80		60-80		60-80
Write Rise/Fall Time (ns)		150		150		150
Min. Analog Output (mv)		8		8		8
Resolution		.5		.5		.5
Modulation (percent)		15		15		15
Crosstalk (percent)		5		5		5
Residual Signal (percent)		10		10		10
Bit Clock Jitter (ns)		50		50		50

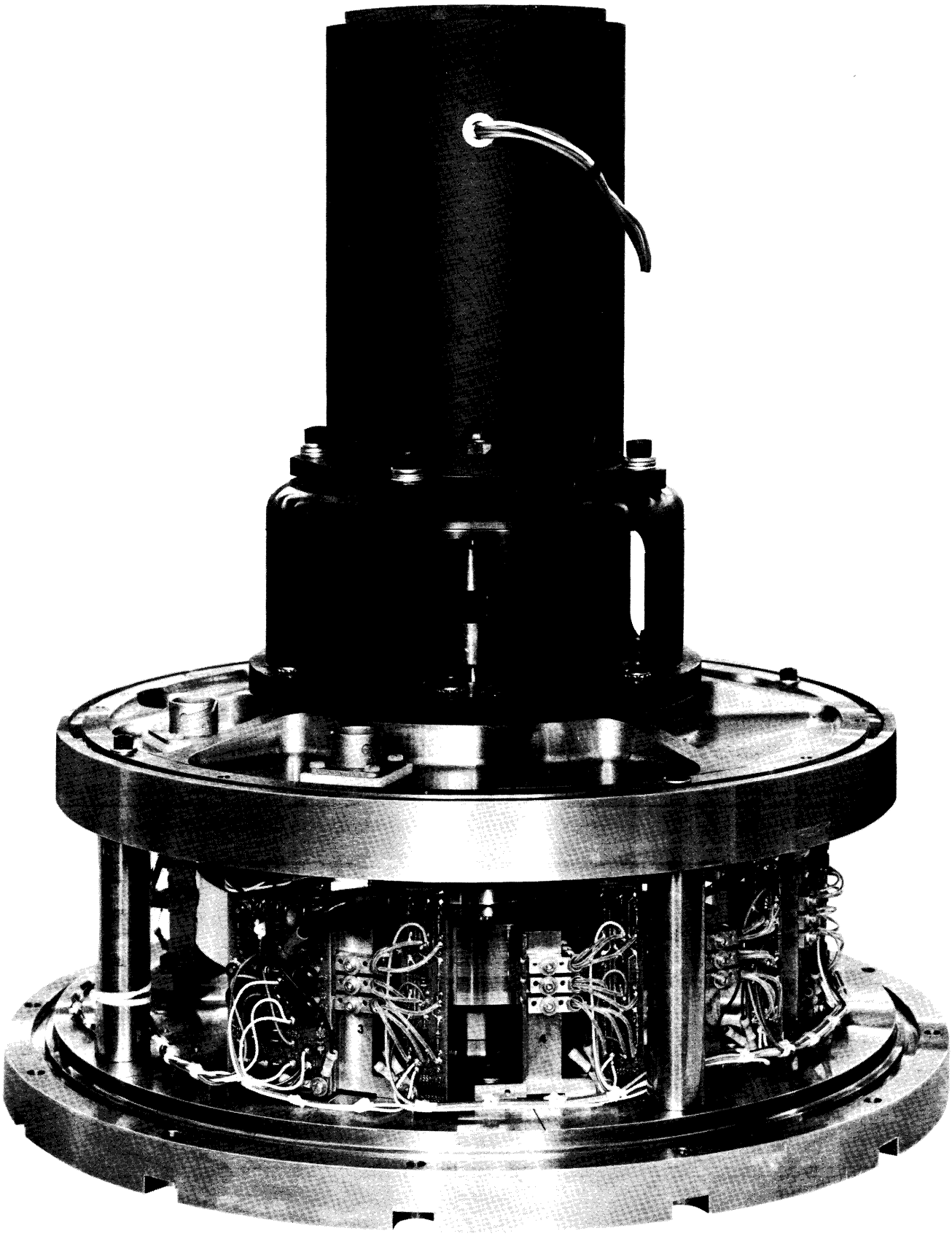


Figure 1-1. Mechanical Unit with Cover Removed

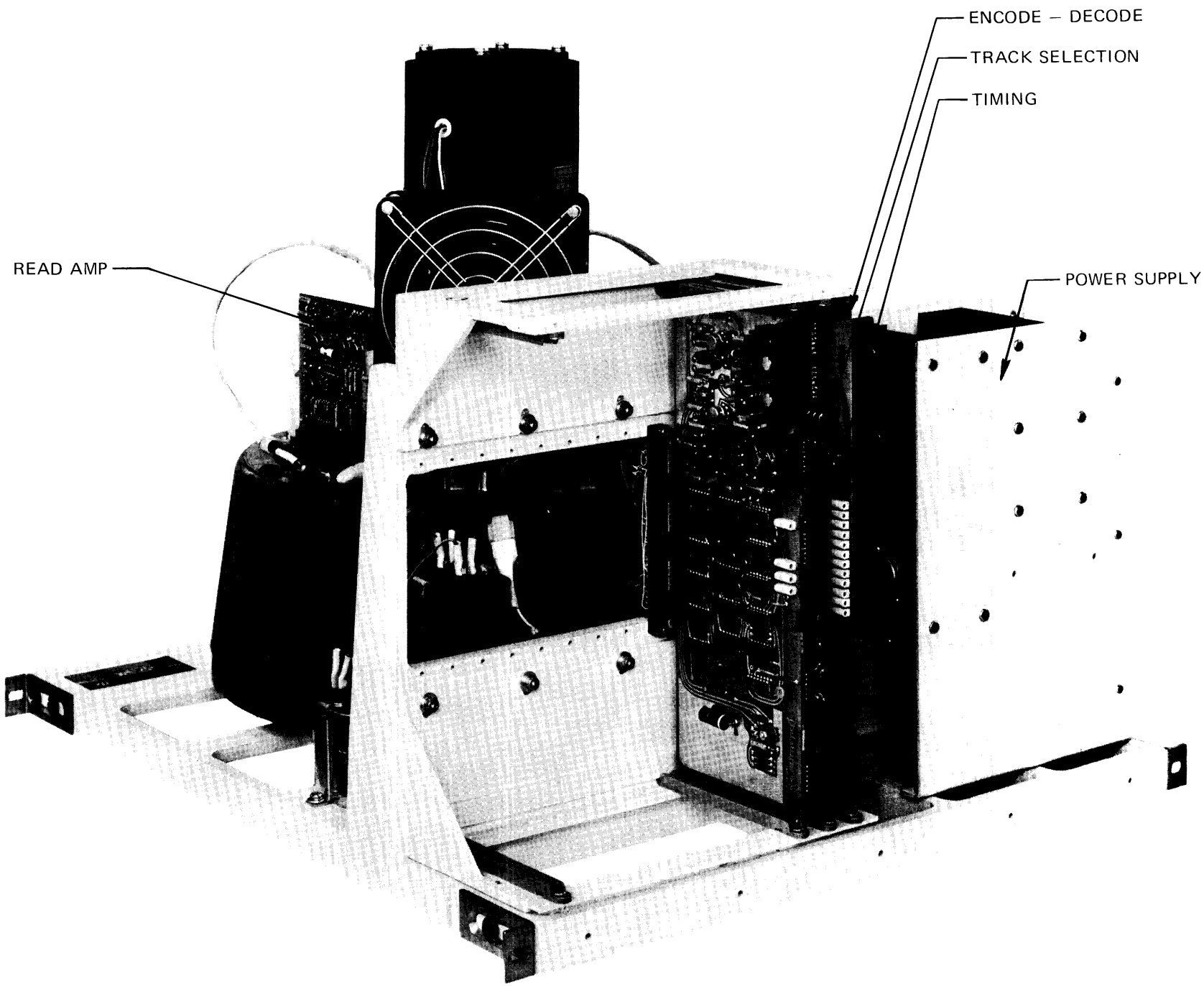
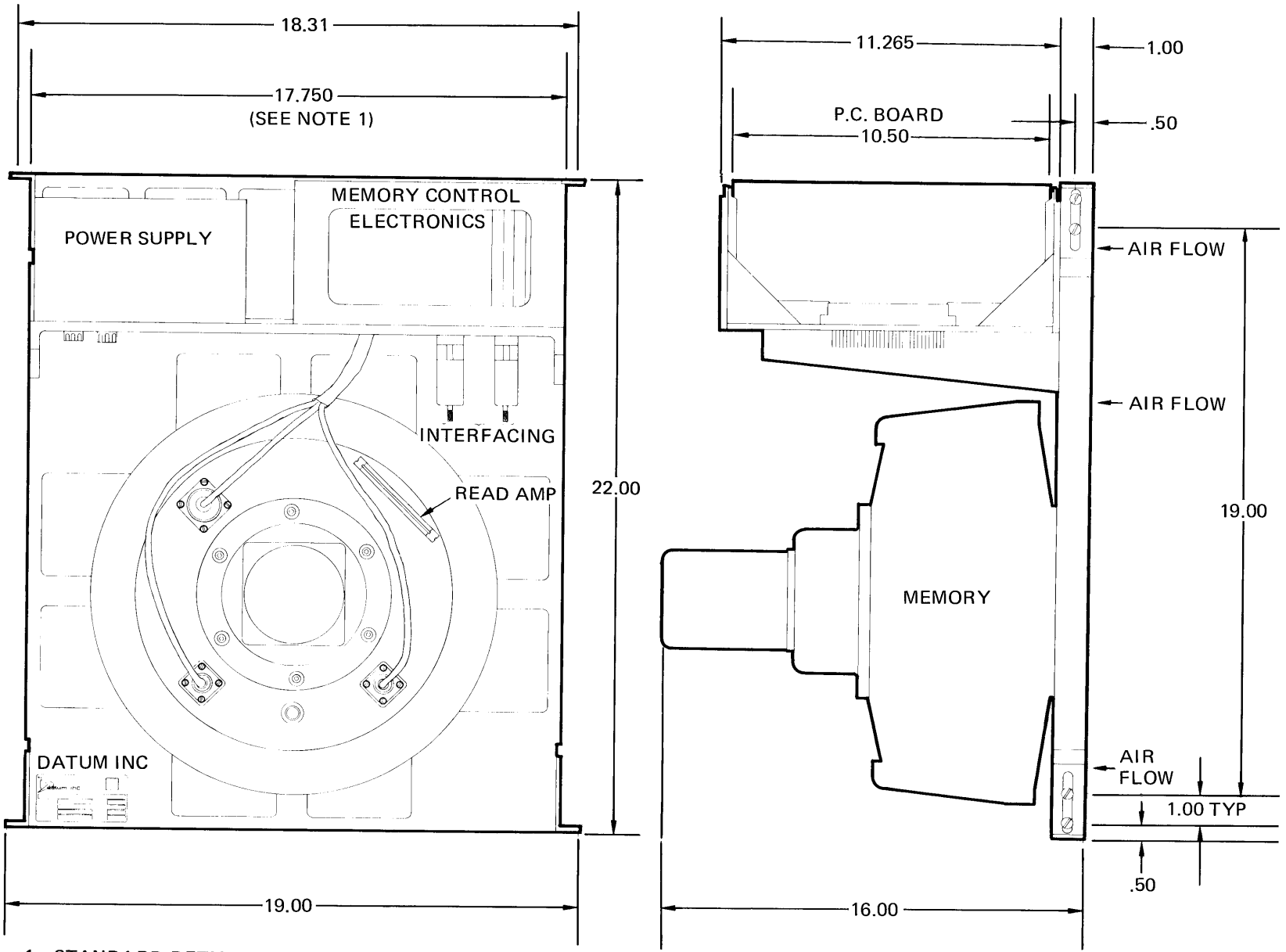


Figure 1-2 Drum Memory Parts Locations



1. STANDARD RETMA OPENING 17 7/8 INCH.

NOTE: UNLESS OTHERWISE SPECIFIED

Figure 1-3. Series 88 Drum Memory Outline Drawing

SECTION II INSTALLATION

2-1. INTRODUCTION

This section provides procedures for unpacking, inspection, checkout, and installation of the Series 88 Drum Memory units. Reshipment information is also included in this section.

2-2. UNPACKING AND INPSECTION

Before accepting the unit from the carrier, inspect the packing boxes for external damage. Any sign of external damage must be noted by both the customer and the carrier and should be called to the attention of an insurance investigator. As soon as the equipment is unpacked, inspect the unit for damage. Check for unusual scratches or dents and damaged cables or connectors. If damage is noted, do not use the unit unless instructed to do so by the insuring agency.

2-3. PRELIMINARY OPERATIONAL CHECK

Before installing the Drum Memory, perform the following check procedure:

1. Connect appropriate source of ac power (see Table 1-1) to terminal board TB1 as specified in Table 2-1.

2. Observe that drum motor starts and brings drum up to speed upon application of ac power. Verify that no unusual sounds are heard and that vibration is barely visible.

3. Arrange an oscilloscope to observe 5-volt level shift signals. Arrange oscilloscope to trigger internally on positive-going transitions.

4. Connect oscilloscope ground to black test point on circuit card 86001 in station A1 of Drum Memory card cage.

5. Connect vertical input of oscilloscope to test point TP2 (second from top) on circuit card 86002 in station A3 of card cage.

6. Verify that pulse observed on oscilloscope has a width of 1 to 1-3/4 bit periods.

7. Arrange oscilloscope time base so as to observe two pulses. Separation between pulses should be approximately 16.7 milliseconds (for 3600 rpm units).

8. Move vertical input connection of oscilloscope to test point TP4 (fourth from top) on circuit board 86002 in station A3.

9. Verify that two super-imposed pulse widths are observed on oscilloscope and that width of narrower pulse is one bit period.

10. Arrange oscilloscope time base so as to observe two pulses. Separation between pulses should be NB where B is the bit period and N is the number of bits per sector.

11. Move vertical input connection of oscilloscope to test point TP3 (third from top) on circuit card 86002 in station A3.

12. Observe square waveform whose period is equal one bit period.

13. Remove power from Drum Memory.

2.4 INSTALLATION

Series 88 Drum Memory units are designed to be mounted in standard RETMA 19-inch racks. Mounting is accomplished by means of four L-brackets each of which is secured to the unit by means of two screws. Slotted holes in the L brackets permit adjustment of the L-bracket positions as required to position the brackets against the mounting members of the rack.

After the unit is bolted into the rack, the installation is completed by connecting ac power to terminal board TB1 in accordance with Table 2-1 and by plugging a signal cable into connector JO1.

The signal cable, which is not supplied, must terminate at the memory unit end in a AMP 57300500 which mates with JO1. Pin assignments for JO1 are listed in Table 2-2. For information about interface signals, refer to Section III.

TABLE 2-1
AC POWER CONNECTIONS

TB1 Terminal	Signal
1	AC High
2	AC Low
5	Chassis Ground

TABLE 2-2
CONNECTOR J101 PIN ASSIGNMENTS

Pin	Function	Pin	Function
1	DATA IN	26	DATA IN GRD
2	DATA OUT	27	DATA OUT GRD
3	WRITE	28	WRITE GRD
4	DEVICE SELECT	29	DEVICE SELECT GRD
5	INDEX	30	INDEX GRD
6	SECTOR	31	SECTOR GRD
7	READ	32	READ GRD
8	ADDRESS 2^0	33	ADDRESS 2^0 GRD
9	ADDRESS 2^1	34	ADDRESS 2^1 GRD
10	ADDRESS 2^2	35	ADDRESS 2^2 GRD
11	ADDRESS 2^3	36	ADDRESS 2^3 GRD
12	ADDRESS 2^4	37	ADDRESS 2^4 GRD
13	ADDRESS 2^5	38	ADDRESS 2^5 GRD
14	ADDRESS 2^6	39	ADDRESS 2^6 GRD
22	$\overline{\text{MEMORY READY}}$	48	BIT CLOCK GRD
23	BIT CLOCK	49	WRITE CLOCK GRD
24	WRITE CLOCK	50	READ CLOCK GRD
25	READ CLOCK		

2.5 RESHIPMENT

When a damaged unit is to be returned to the factory for repair or service, contact your nearest DATUM INC representative for written permission to ship. Shipping instructions and a reject form will insure expedient repair and return of the unit.

2-6. OPERATION

Series 88 Drum Memory units operate automatically under control of external equipment. No controls or indicators are provided.

SECTION III INTERFACE DATA

3-1. INTRODUCTION

This section describes the interface between Series 88 Drum Memory units and external equipment. This interface is illustrated in Figure 3-1. Individual interface signal requirements and required time relationships between these signals are defined in the paragraphs which follow.

3-2. DEVICE SELECTION

The DEVICE SELECT line provides the means for a single drum controller to interface with a group of drum memory units via a common bus. A separate DEVICE SELECT line must be provided for each drum memory unit in the group. The remainder of the interface lines, with the exception of the MEMORY READY line (paragraph 3-9), can then be connected in common to all memory units of the group.

To select a particular drum memory unit, the DEVICE SELECT line to that unit is placed at the +0.5-volt level. DEVICE SELECT lines to other drum memory units in the group are placed at the +4-volt level. If only one drum memory unit is interfacing with the controller, then the DEVICE SELECT line for that unit can be hard-wired to ground so that the unit is continuously selected.

3-3. TRACK SELECTION

Binary track selection data must be supplied to the track address bus. The number of track address bits required depends upon the track capacity of the particular unit. On track address lines; binary 1 = +0.5 volt binary 0 = +4 volts.

Timing requirements for track address data are as follows:

1. Track address data must be present on the track address bus for a minimum of 5 microseconds before reading or writing is enabled and must remain present throughout reading or writing. (See Figure 3-2.)

2. In order to permit writing or reading on the first sector of track (N + 1) after writing or reading on the last sector of track N, without waiting for a complete drum revolution, a dead zone must be provided at the end of each track. This dead zone provides the 30 microseconds necessary for track address switching and write-to-read recovery. This dead zone cannot overlap the post-amble/preamble zone (paragraph 3-8). (See Figure 3-3).

3.4 BIT CLOCK

All timing signals are derived from a bit clock pattern factory-recorded on the clock track. This pattern is read during each drum revolution and digitized to obtain the BIT CLOCK signal which is a square wave whose frequency corresponds to the bit transfer rate for the particular drum. The pattern contains a single cycle whose period is twice the bit transfer period. This cycle (designated as the index gap) is used by the drum memory timing logic to identify the index position.

3-5. SECTOR SELECTION

In order to define positions along each data track, the drum memory supplies INDEX and SECTOR pulses. The INDEX pulse occurs once per drum revolution and identifies the start of sector 0. Sector pulses occur at the start of each sector. Sector length is a customer-specified, factory hardware-programmed parameter.

3-6. WRITE SIGNALS

The Drum Memory accepts three signals relating to a write operation only. These are WRITE, WRITE CLOCK, and DATA INPUT.

The WRITE signal controls the write-current on/off function. A +0.5 volt level on the WRITE line causes the write current to be turned on. The WRITE level should be switched coincident with the trailing edge of the SECTOR pulse as illustrated in Figure 3-4.

The READ signal (paragraph 3-7) must be at the +4-volt (disabling) level for a minimum of 1 microsecond before the WRITE signal is placed at the enabling level and must remain at the +4-volt level until a minimum of 30 microseconds after the WRITE signal has returned to the disabling (+4-volt) level. This relative timing is illustrated in Figure 3-5.

The timing reference for writing is the BIT CLOCK signal derived from the clock track of the drum. In order to compensate for delays encountered in the interface cabling and for controller propagation delays, the BIT CLOCK signal is supplied to the external controller which transmits it back to the Drum Memory on the WRITE CLOCK line. The external controller must accept the BIT CLOCK signal and transmit it, in phase, on the WRITE CLOCK line.

The DATA INPUT signal is an NRZ signal synchronized with the WRITE CLOCK. As illustrated in Figure 3-6, bit

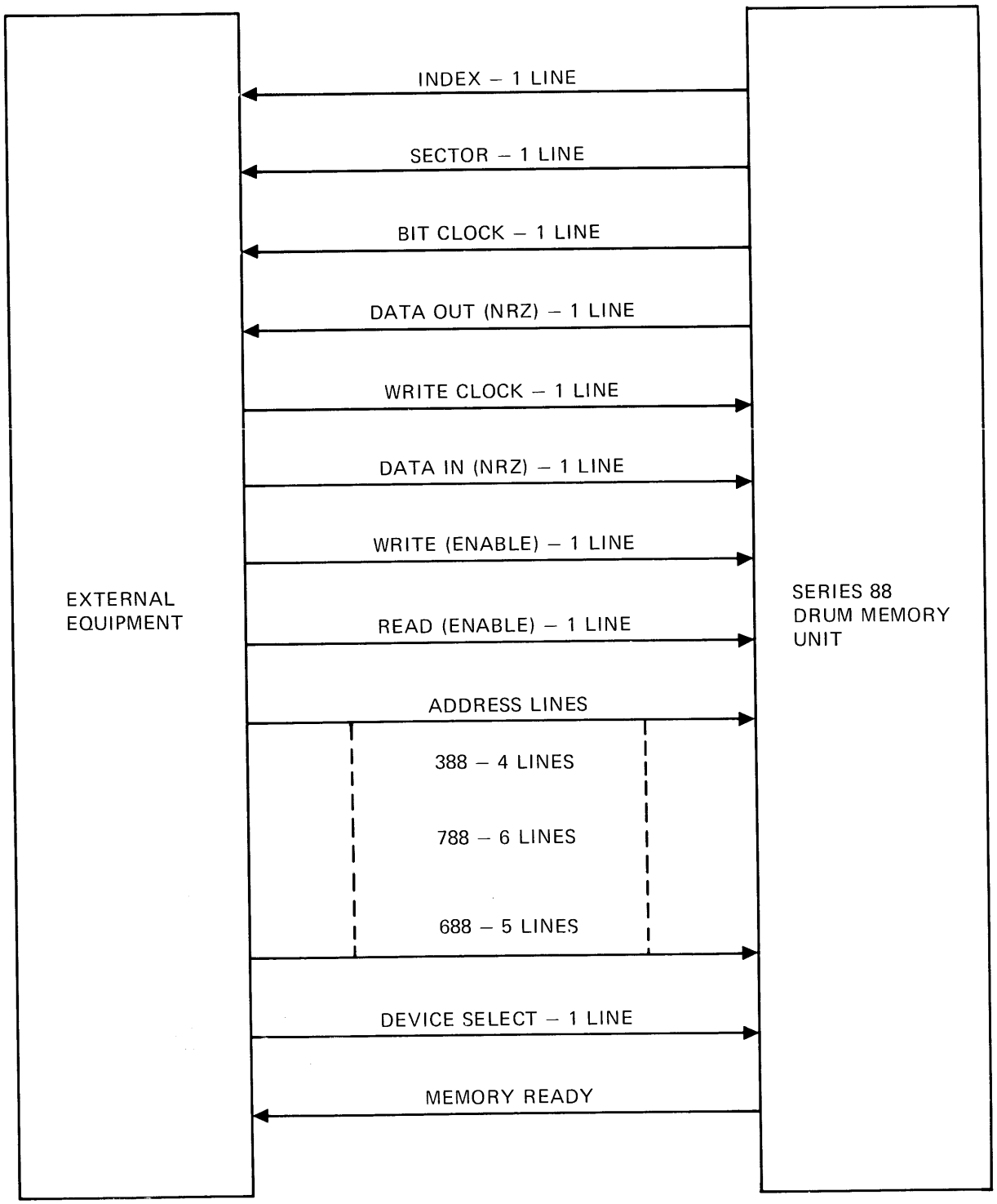


Figure 3-1. Series 88 Drum Memory Interface Block Diagram

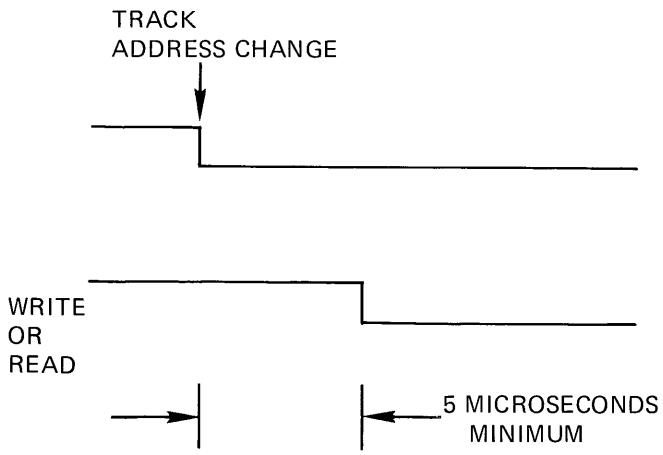


Figure 3-2. Track Address Recovery Timing

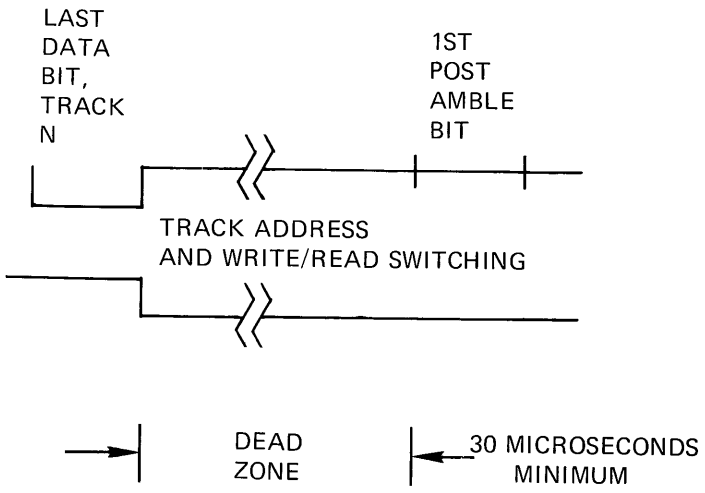


Figure 3-3. Dead Zone Requirements

boundaries are synchronized with high-going transitions of the WRITE CLOCK signal. The +4-volt level of this signal is the binary 0 level while the +0.5-volt level is the binary 1 level.

3-7. READ SIGNALS

The drum memory accepts one signal and supplies two signals that are associated with the read operation only. These are READ, READ CLOCK, and DATA OUT.

The READ signal is accepted by the drum memory and used to gate internal drum memory signals to the interface READ CLOCK and DATA OUT lines. The read-enable level on the READ line is +0.5 volt while the disable level is +4 volts. The READ line must be placed at the +4-volt level at least 1 microsecond before the WRITE LINE is placed at the +0.5-volt level at the start of a write operation. The READ line must then remain at the +4-volt level until 30 microseconds after the WRITE signal has returned to the +4-volt level. This timing relationship is illustrated in Figure 3-5.

The READ CLOCK signal is the clock signal recovered from the data track during reading. It consists of low-going pulses whose leading edges are synchronized with respect to the bit boundaries of the DATA OUT signal. The READ CLOCK is inhibited when the WRITE signal is at the +0.5-volt level or when the READ signal is at the +4-volt level. It is also inhibited for a fixed period following each SECTOR pulse. This prevents the transmission of spurious READ CLOCK pulses resulting from write current turn on and turn off. The duration of this inhibit period is such that the clock pulses associated with the final two bits of the preamble (paragraph 3-8) are never inhibited as illustrated in Figure 3-7.

The DATA OUT signal is an NRZ signal. The +4-volt level of this signal is the binary 0 level and the +0.5-volt level is the binary 1 level.

3-8. SECTOR FORMAT

Each sector record must consist of three segments; a 7-bit preamble, the data record, and a 3-bit post-amble. The preamble and a post-amble provide margins required to prevent timing anomolies from being introduced as a result of skew between the clock track and data tracks. The preamble serves two additional functions:

1. It provides a period during which READ CLOCK pulses can be inhibited so that spurious pulses associated with turn on and turn off of write current are not transmitted on the external READ CLOCK line during reading;

2. It provides a consecutive group of zeroes as required for the synchronization of the decoder logic.

During writing, the external controller must supply the preamble and post-amble segments of each record as well as the data segment. During reading, the external controller must recognize the preamble/data segment boundary.

Figure 3-8 illustrated the timing of the preamble and post-amble during writing. It is preferable for the post-amble to consist of three O's. The preamble must consist of six binary O's followed by a binary 1.

Figure 3-7 illustrates preamble/post-amble time during reading.

3-9. $\overline{\text{MEMORY READY}}$ LINE

The $\overline{\text{MEMORY READY}}$ line is at the +4-volt (not ready) level for a fixed delay period after power turn on or at any time when Drum Memory power is on and any of the power supply outputs is not present.

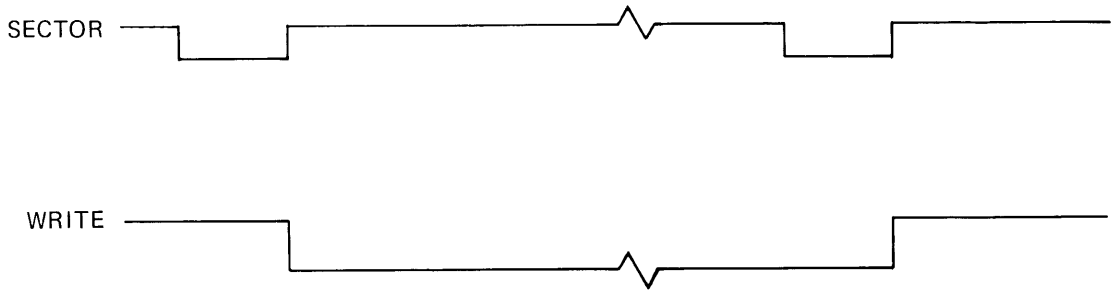


Figure 3-4. Write Turn On/Turn Off Timing

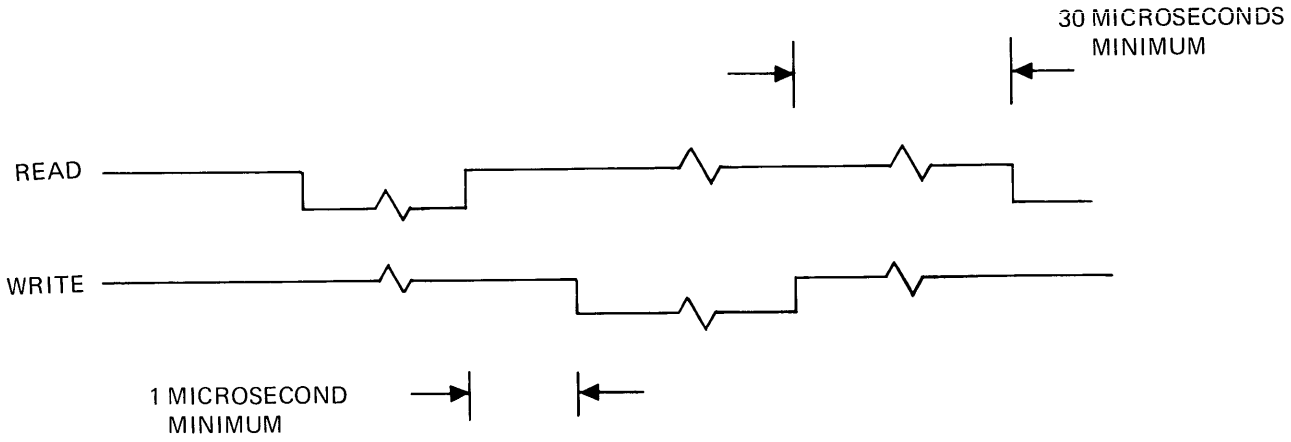


Figure 3-5. Write And Read Timing

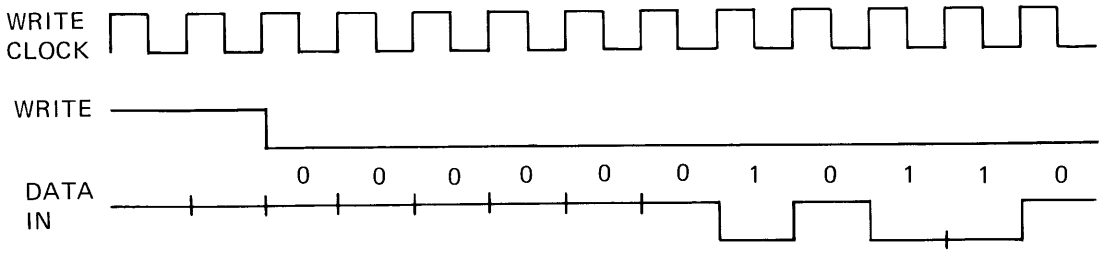


Figure 3-6. Write Timing

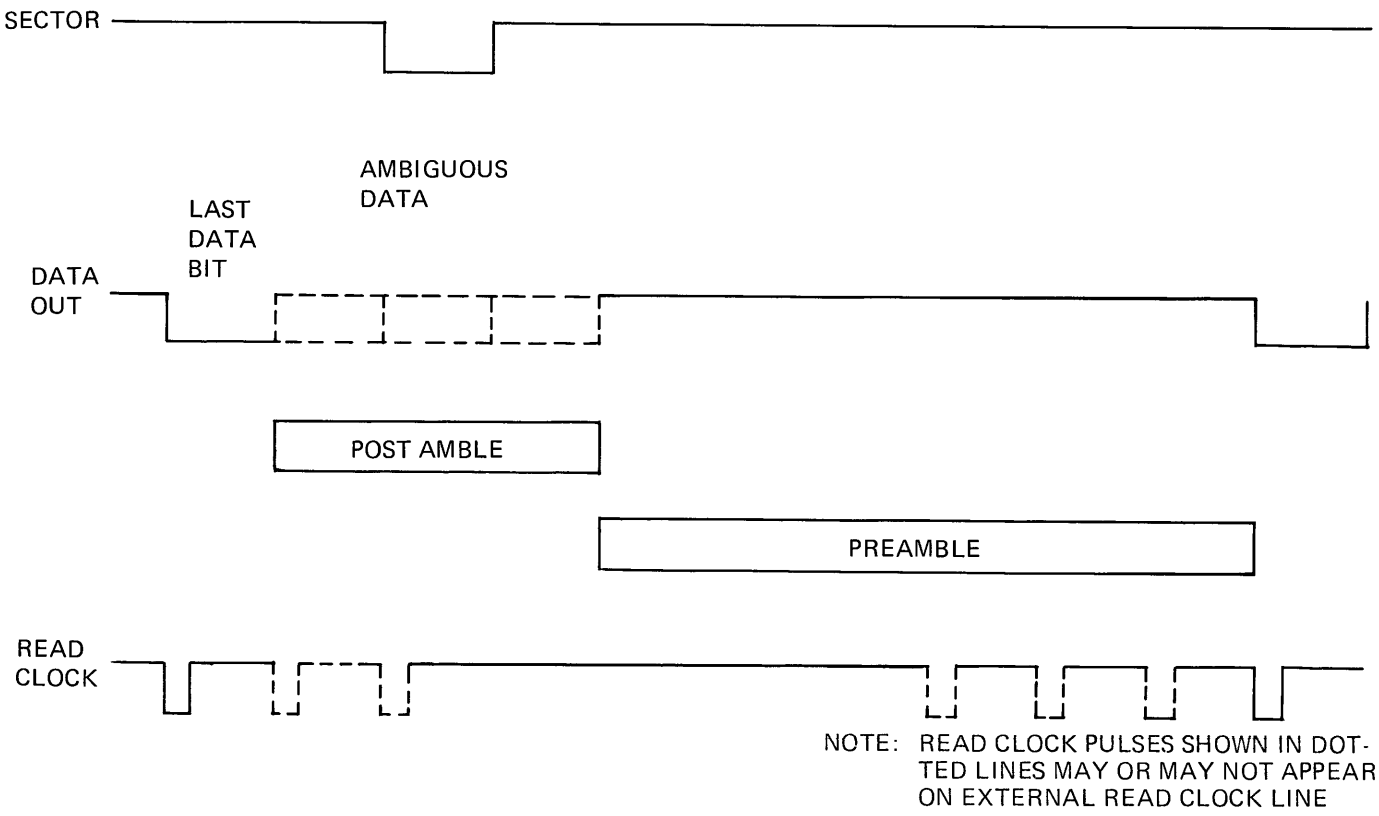


Figure 3-7. Read Clock Inhibit Timing At Start Of Sector

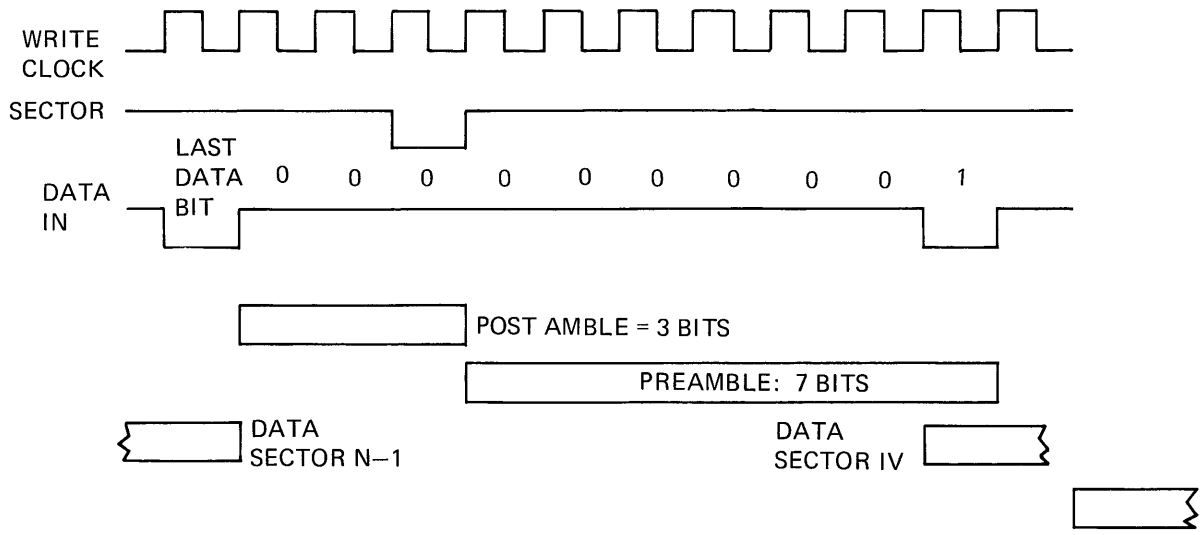


Figure 3-8. Post-amble/Preamble Format (Write)

A +0.5-volt level on the MEMORY READY line indicates that the Drum Memory is ready for reading or writing.

3-10 INTERFACE CIRCUITS

Figure 3-9 illustrates a complete circuit for one interface line including a driver, a twisted line pair, and the interface termination. All input lines to the drum memory are terminated as shown in this figure and all output lines should be terminated in this manner in the external equipment.

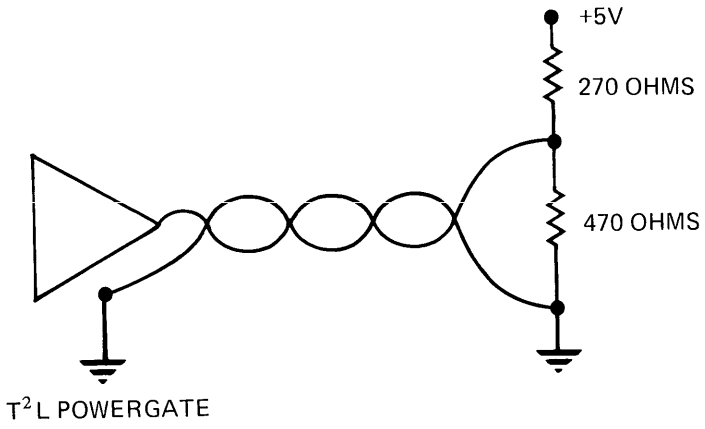


Figure 3-9. Interface Circuit

SECTION IV THEORY OF OPERATION

4-1. INTRODUCTION

The functional components of the Drum Memory are as follows:

1. A continuously rotating drum which serves as the medium on which data is recorded.

2. A clock head and associated timing electronics which recovers a clock pattern recorded at the factory. Bit, sector, and index timing are derived from this clock pattern.

3. A read/write head for each data track.

4. Track selection electronics which connects one read/write head to the read/write electronics in accordance with the status of externally supplied address data.

5. Read/write electronics which accepts NRZ data during writing and supplies NRZ data during reading.

4-2. RECORDING METHOD

The double frequency code is used. This code and its generation from an NRZ input is illustrated in Figure 4-1. This code features a level transition at the start of each bit period. During a binary 1 bit period a second transition occurs at the midpoint of the bit period. During a binary O bit period no second transition occurs.

4-3. OVERALL BLOCK DIAGRAM

Figure 4-2 is an overall block diagram of the drum electronic functions. The numbers within the blocks indicate schematic drawings which are included at the back of this manual. Each schematic covers a particular circuit card.

Timing is derived from a clock pattern pre-recorded on a special clock track. As the drum rotates this clock pattern is recovered by a clock head, amplified by the clock preamplifier, and supplied to the timing logic. The timing logic processes the clock pattern to obtain index, sector, and bit clock signals which are supplied to the controller interfacing with the drum electronics.

The index pulse occurs once per drum revolution and indicates that the start of sector O is passing the heads. The sector pulse occurs at the start of each sector. Sector length is hardware programmed into each unit at the factory. The bit clock is a square wave whose frequency coincides with the bit rate.

To enable either a write or read operation, the drum controller transmits track address data and a device select signal to the drum. The track address data is used to connect a particular data track head to the write amplifier in the encode/decode logic or to the read amplifier in accordance with whether a write or read operation is selected. The device-select signal enables the drum electronics to receive other signals from the controller and to supply output signals to the controller.

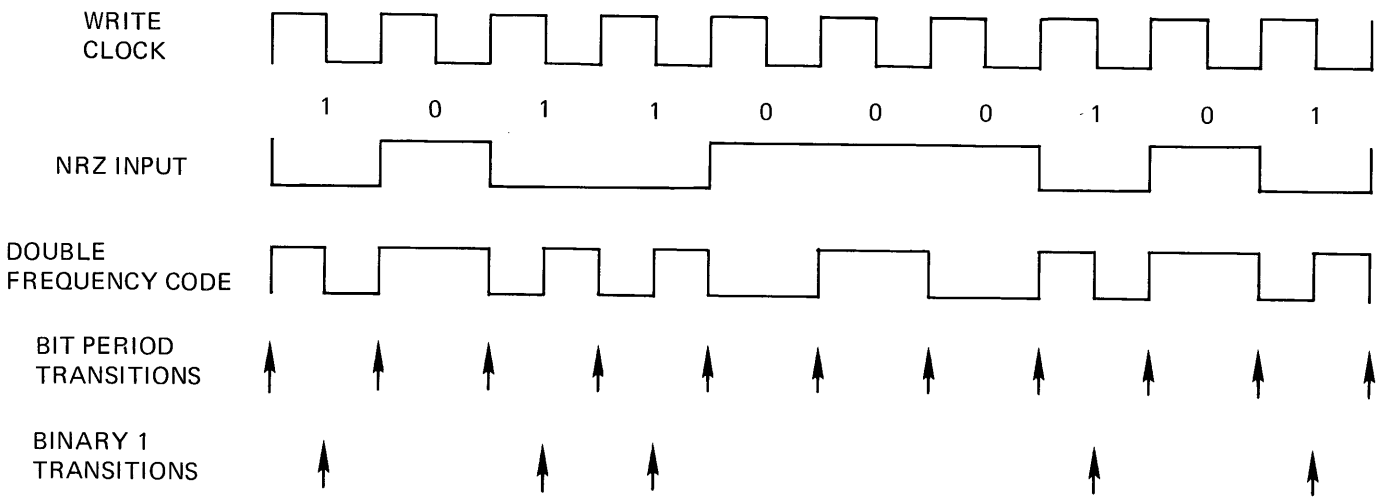


Figure 4-1. Double Frequency Code

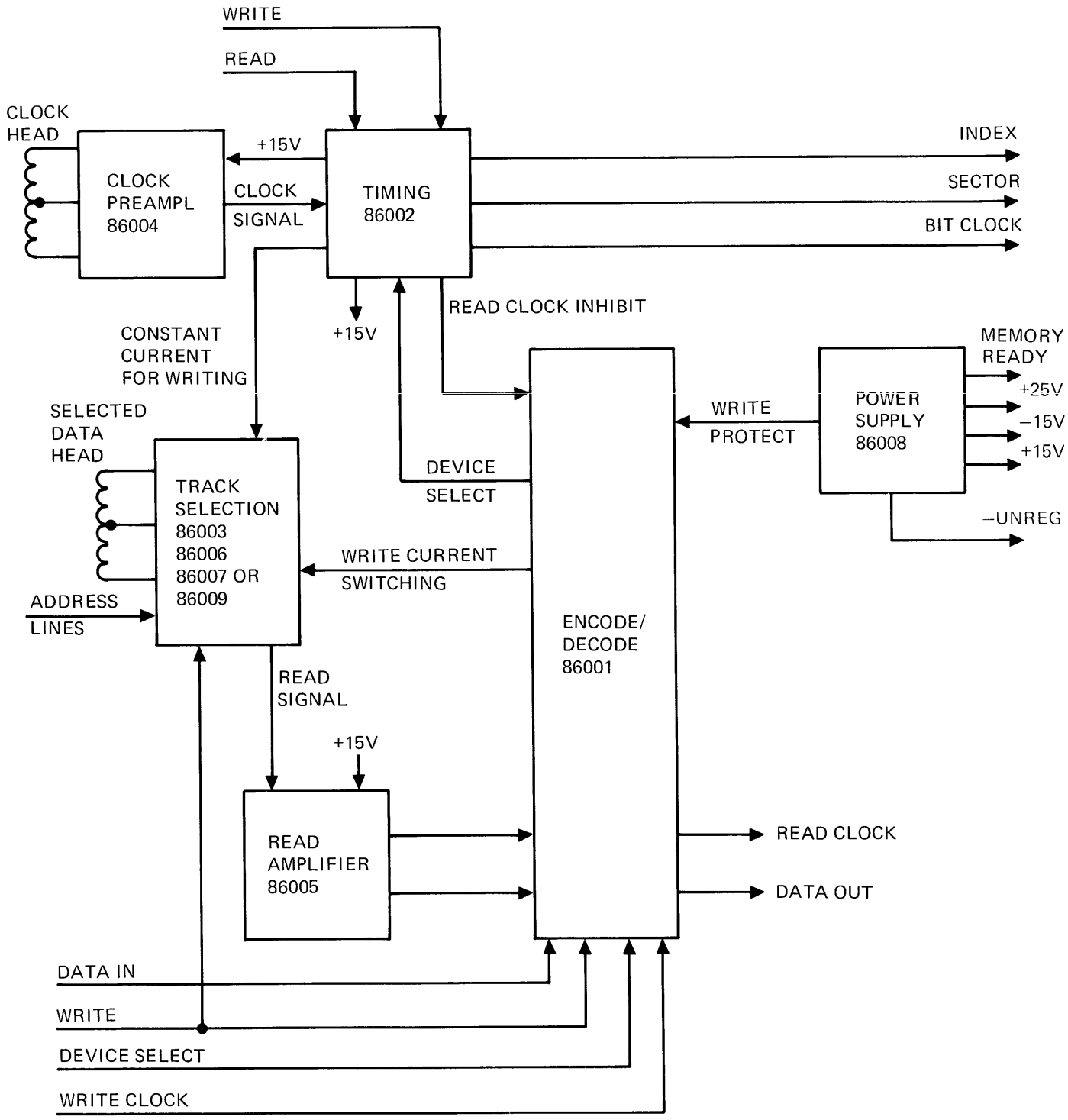


Figure 4-2. Drum Electronics Overall Block Diagram

For a write operation, the drum controller also supplies WRITE, WRITE CLOCK, and DATA IN signals. The WRITE signal conditions the drum electronics for a write operation. The WRITE CLOCK signal is the BIT CLOCK signal turned around in the controller. It is used to time the writing of data. Thus, write timing is derived from the clock pattern pre-recorded on the drum but includes the delays involved in transmission of the clock to the controller and in receiving clock and accompanying data from the controller.

The DATA IN signal is in NRZ form. The encoder logic converts this signal to double-frequency form and supplies write current to the selected data track head via the track selection logic.

A read operation is enabled by the transmission of a READ signal together with a DEVICE SELECT signal and track address data. During a read operation, a data track head is selected via the track selection logic for connection to the read amplifier where the read signal is amplified and digitized in double-frequency form. The complement double-frequency signals + PEAK and – PEAK are applied to the decode logic where they are converted to NRZ form. A read clock is also recovered from the double frequency signals. The read clock and data-out signals are supplied to the external controller.

4-4. WRITE FUNCTIONS

Figure 4-3 is a block/logic diagram illustrating write functions. Figure 4-4 illustrates waveforms associated with both write and read functions. In the absence of the WRITE signal, the WRITE ON/OFF CONTROL flip-flop is in the off status. This holds both outputs of the WRITE DATA flip-flop at inhibiting levels turning off WRITE SWITCHES Q1 and Q2 and preventing write current from flowing.

When the WRITE signal is supplied, the first WRITE CLOCK pulse switches the WRITE ON/OFF CONTROL flip-flop to the on status. Under this condition, one of the two outputs of the WRITE DATA flip-flop is placed at the enabling level. This enables current from the constant current source through one half of the selected read/write head. The direction of current depends upon whether Q1 or Q2 is conducting and this in turn depends upon the status of the WRITE DATA flip-flop.

The WRITE DATA flip-flop is toggled at the start of each bit period by a pulse from CLOCK TRANSITION SINGLE SHOT A1. It is also toggled at the mid-point of each bit period during which a binary 1 level is being received on the DATA IN line. The pulse which times the conditional toggling at the mid-point of the bit period is supplied by the ONES TRANSITION SINGLE SHOT and is gated to the WRITE DATA flip-flop clock line by the DATA IN level.

Both of the single shots are fired in response to the WRITE CLOCK signal. However, one fires on each true-going edge and the other fires on each false-going edge as required to provide start and mid-point timing signals.

WRITE DISABLE switch Q3 disables WRITE SWITCHES Q1 and Q2 in response to a WRITE PROTECT signal from the power supply. This occurs for a fixed interval after power turn on in order to prevent unintentional writing during turn on. It also occurs if any of the power supply voltages is lost.

4-5. READ FUNCTIONS

Figure 4-5 is a block/logic diagram illustrating functions relating to the recovery of an NRZ data signal and a read clock signal from the signal read from a selected data track. Figure 4-4 illustrates associated waveforms.

The low level read signal from the selected data head has an amplitude of from 5 to 15 millivolts. This signal is applied via the track selection logic to the read amplifier. Voltage amplification of the signal is provided by an operational amplifier employing module A1. This is followed by transistor amplifier Q1 which contributes an additional voltage gain.

The output of Q1 is supplied to a voltage follower employing module A2. The voltage follower provides the low impedance drive required for the active delay network which follows it. This active network which includes transistors Q2 and Q3 provides undelayed and delayed versions of the signal which are used for peak detection putposes.

Figure 4-6 illustrates the phase relationship between the undelayed and delayed signals. During the half cycle when the signals are becoming more positive, the undelayed signal is positive with respect to the delayed signal. During the half cycle when the signals are becoming more negative, the delayed signal is positive with respect to the undelayed signal. The crossovers occur midway between the delayed and undelayed peaks.

The delayed and undelayed signals are applied to the two inputs of two differential amplifiers which produce square waves whose voltage transitions coincide with the polarity crossovers. The delayed and undelayed signals are supplied in opposite phase to the two differential amplifiers so as to obtain out of phase square waves at the outputs of these amplifiers.

The two square waves from the differential amplifiers (+ PEAK and – PEAK) are supplied to the decoder logic. These two signals are out-of-phase double frequency waveforms. The first step in recovering clock pulses and NRZ data from this waveform is to convert transitions into pulses. This is implemented by single shots A1 and A2. A1 supplies a pulse in response to each negative-going transition of + PEAK while A2 supplies a pulse in response to each negative-going transition of – PEAK. The two pulse trains are combined by OR gating to produce a pulse train which contains a pulse for each transition of the PEAK signals. The same result could have been obtained

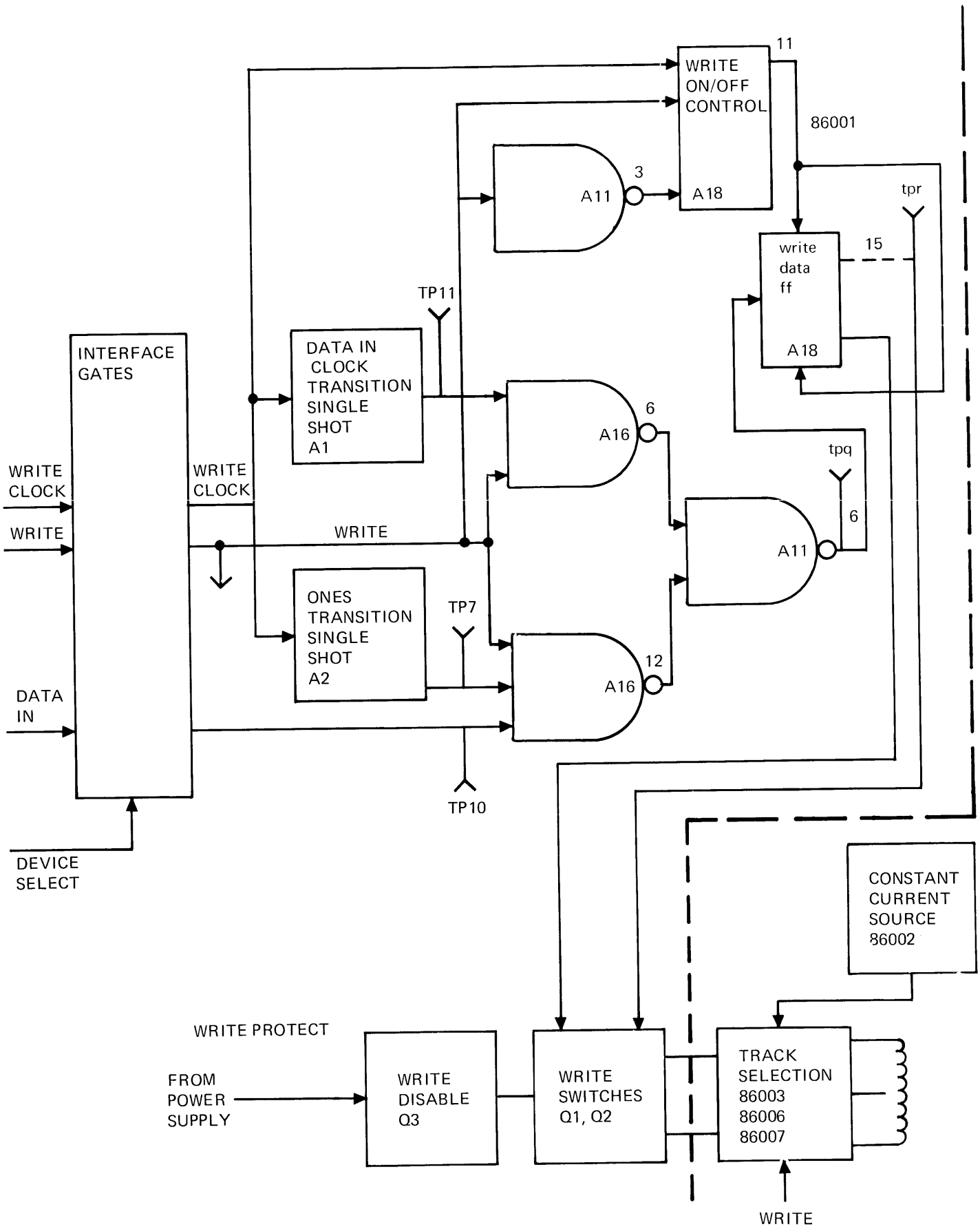


Figure 4-3. Write Functions, Block Diagram

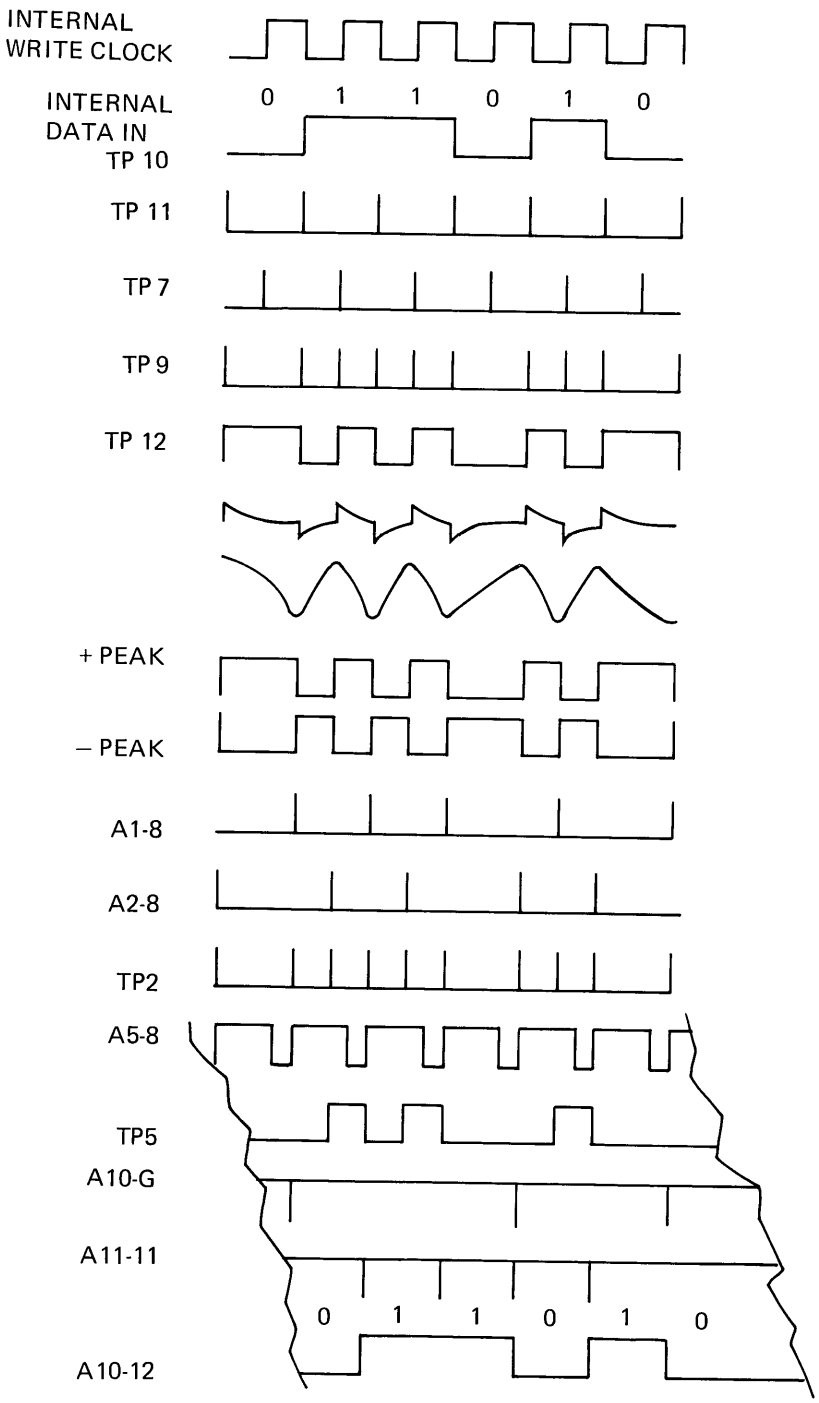


Figure 4-4. Functional Timing Diagram

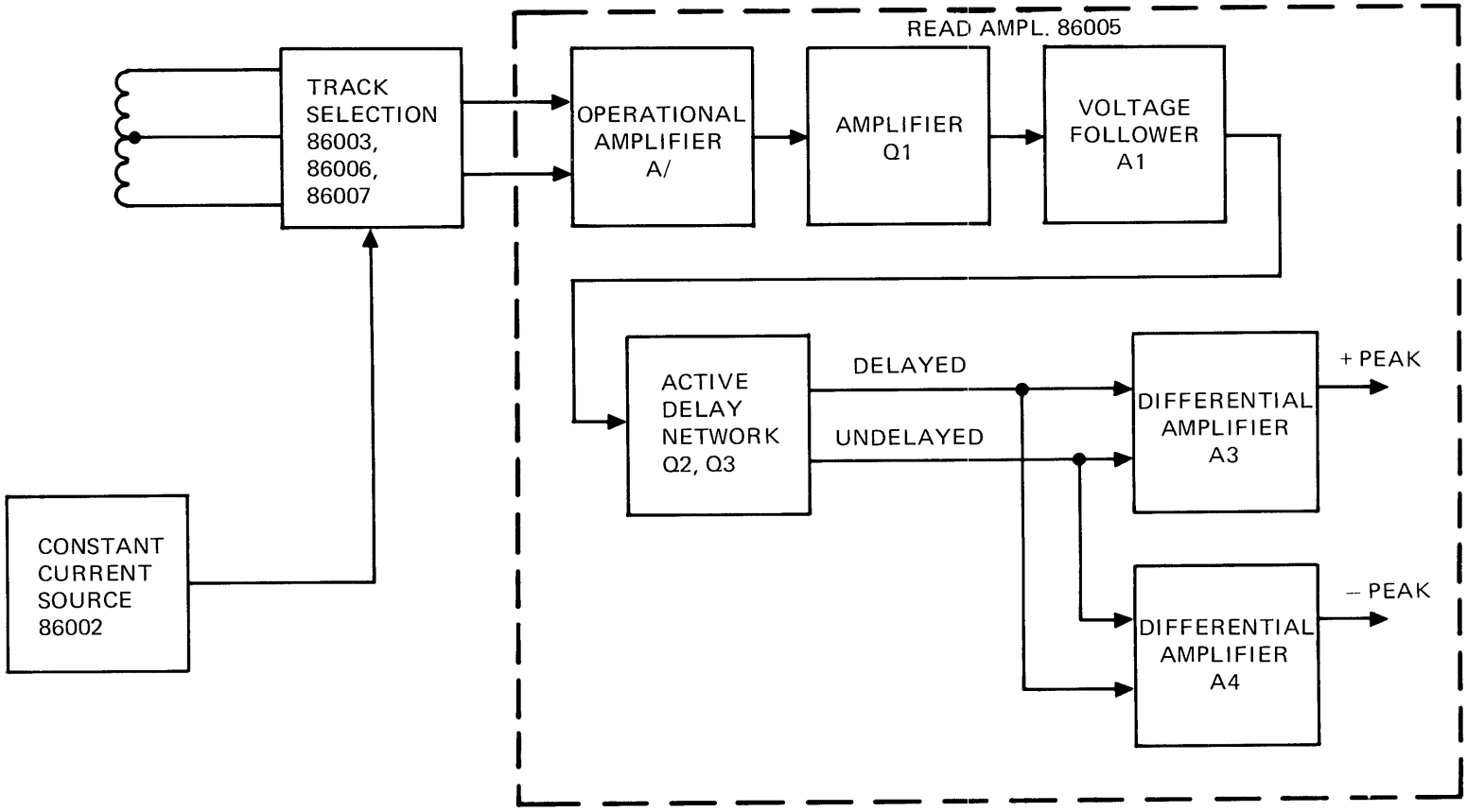


Figure 4-5. READ Functions (Simplified Equivalent) (Page 1 of 2)

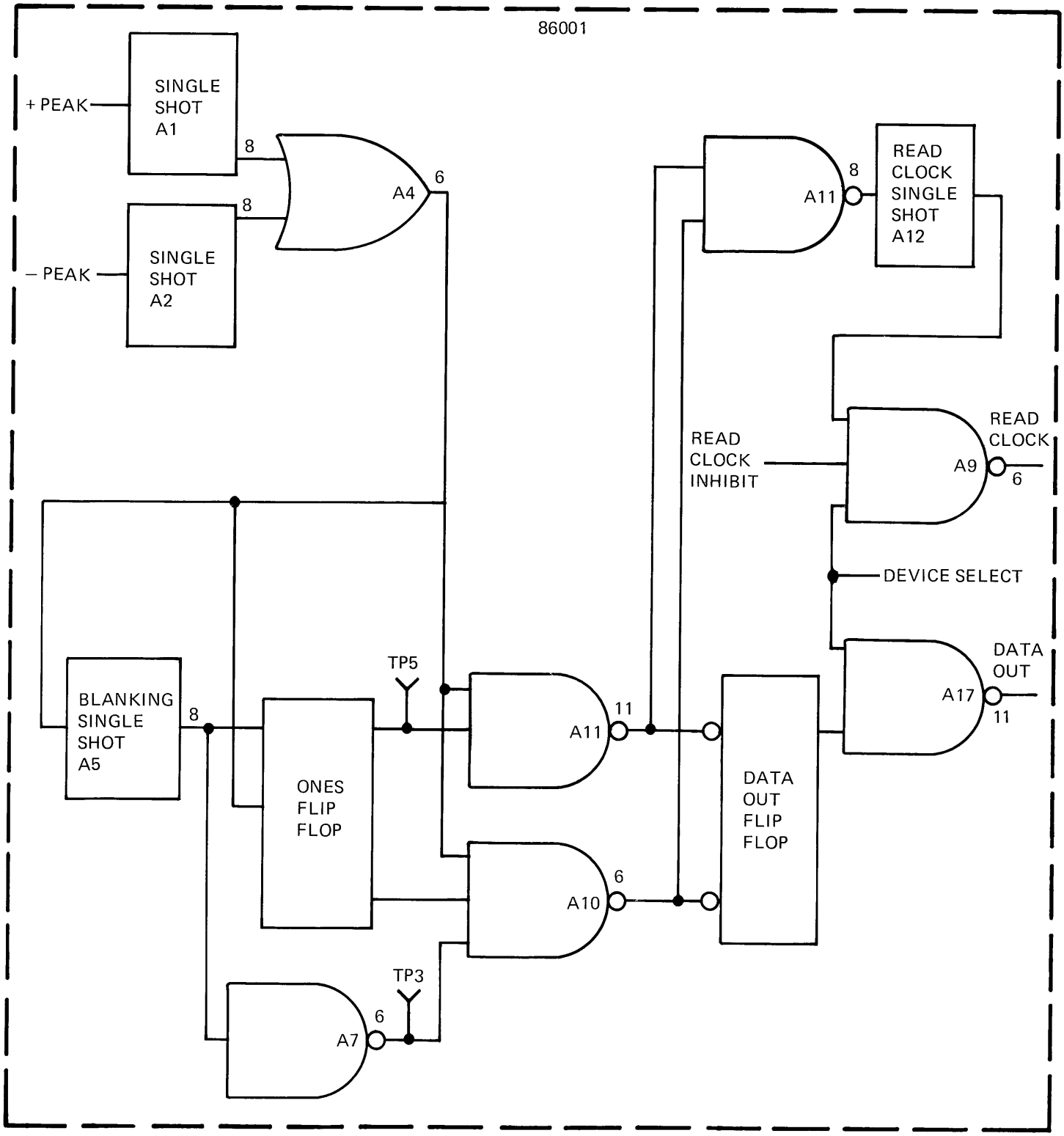


Figure 4-5. READ Functions (Simplified Equivalent) (Page 2 of 2)

by generating a single PEAK signal and generating pulses in response to both positive and negative-going transitions of this signal. However, the method used provides compensation for assymmetry in the detection of positive and negative peaks.

The pulse train obtained from the OR gate contains clock pulses and binary 1 pulses. A blocking single shot provides the means of separating these two types of pulses. Each clock pulse fires the single shot whose pulse width is 3/4 of a clock period. Thus, pulses arriving when the single shot is set are binary 1 pulses. (The preamble of all binary 0's at the start of each sector insures that the blocking single shot is initially fired in response to a clock pulse rather than a binary 1 pulse.)

Each binary 1 pulse clocks the ONES flip-flop to the set status (as a result of the presence of the blocking pulse). Each clock pulse is supplied to the read-clock single shot causing a READ CLOCK pulse to be supplied to the controller. If the ONES flip-flop is in the reset status at clock pulse time, the clock pulse resets the DATA OUT flip-flop (if this flip-flop is in the set state). If the ONES flip-flop is in the set status at clock pulse time, the clock pulse sets the DATA OUT flip-flop (if this flip-flop is in the reset state). It also resets the ONES flip-flop.

The DATA OUT signal is gated to the DATA OUT interface line by the DEVICE SELECT signal. The READ CLOCK signal is gated to the READ CLOCK interface line by the DEVICE SELECT signal unless the READ CLOCK gate is inhibited by the READ CLOCK INHIBIT signal from the timing logic.

4-6. TIMING FUNCTIONS

Figure 4-7 is a block diagram illustrating the generation of the BIT CLOCK, INDEX, and SECTOR signals. All of these signals are derived from the clock pattern that is factory recorded on the clock track and is recovered during each drum revolution. The clock pattern is recovered and digitized in essentially the same manner that data is recovered and digitized by the read amplifier. The only difference is that only a single peak detection differential amplifier is used so that only a single phase of digital signal is obtained.

The digital clock signal is applied through an interface gate to the external BIT CLOCK line. It is also used by the index detector and by the sector counter.

The index position is identified in the clock pattern by a single cycle having a period equal to twice the bit period. The index identifier is detected by a retriggerable single shot circuit which has a pulse duration that is longer than a bit period. Each bit period pulse retriggers the circuit before it returns to the reset status. However, during the longer index position identifier period, the circuit times out and resets. This jam sets the INDEX WIDTH flip-flop. The first bit clock pulse following the index identifier period fires the index detector single shot. This releases the INDEX WIDTH flip-flop and allows it to reset in response to the second bit clock pulse. The INDEX WIDTH flip-flop output is supplied via an interface gate to the external INDEX line. It is also supplied to the SECTOR pulse logic.

Starting with a hardware-programmed preset count value, the sector counter accumulates a bit clock count until it reaches the full count status. The decoding of the full count sets a storage flip-flop which controls the counter preset line. This causes the hardware-programmed starting count to be reloaded into the sector counter as required to start another count cycle. The next bit clock pulse sets the SECTOR WIDTH flip-flop which remains set for a single bit clock period. The output of the SECTOR WIDTH flip-flop is supplied through an interface gate to the external SECTOR line.

The full count decode flip-flop is also set at index time by the output of the INDEX WIDTH flip-flop. This terminates the current sector count, produces a SECTOR pulse, and starts a new sector count.

The timing logic supplies the READ CLOCK INHIBIT signal to the encode/decode logic. This signal is placed at the active level when an external WRITE command signal is received. It is also placed at the active level at any time that an external READ command signal is not being received. The READ CLOCK INHIBIT signal is also placed at the active level during the pulse period of the READ CLOCK INHIBIT single shot. This single shot is fired at each SECTOR pulse time so as to provide a READ CLOCK INHIBIT pulse which prevents spurious READ CLOCK pulses resulting from turn-on or turn-off of write current from reaching the external READ CLOCK line.

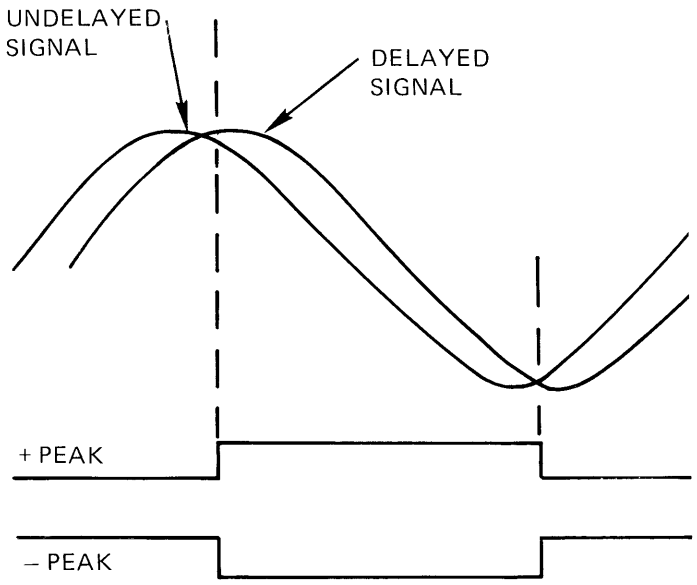


Figure 4-6. Peak Detection Timing

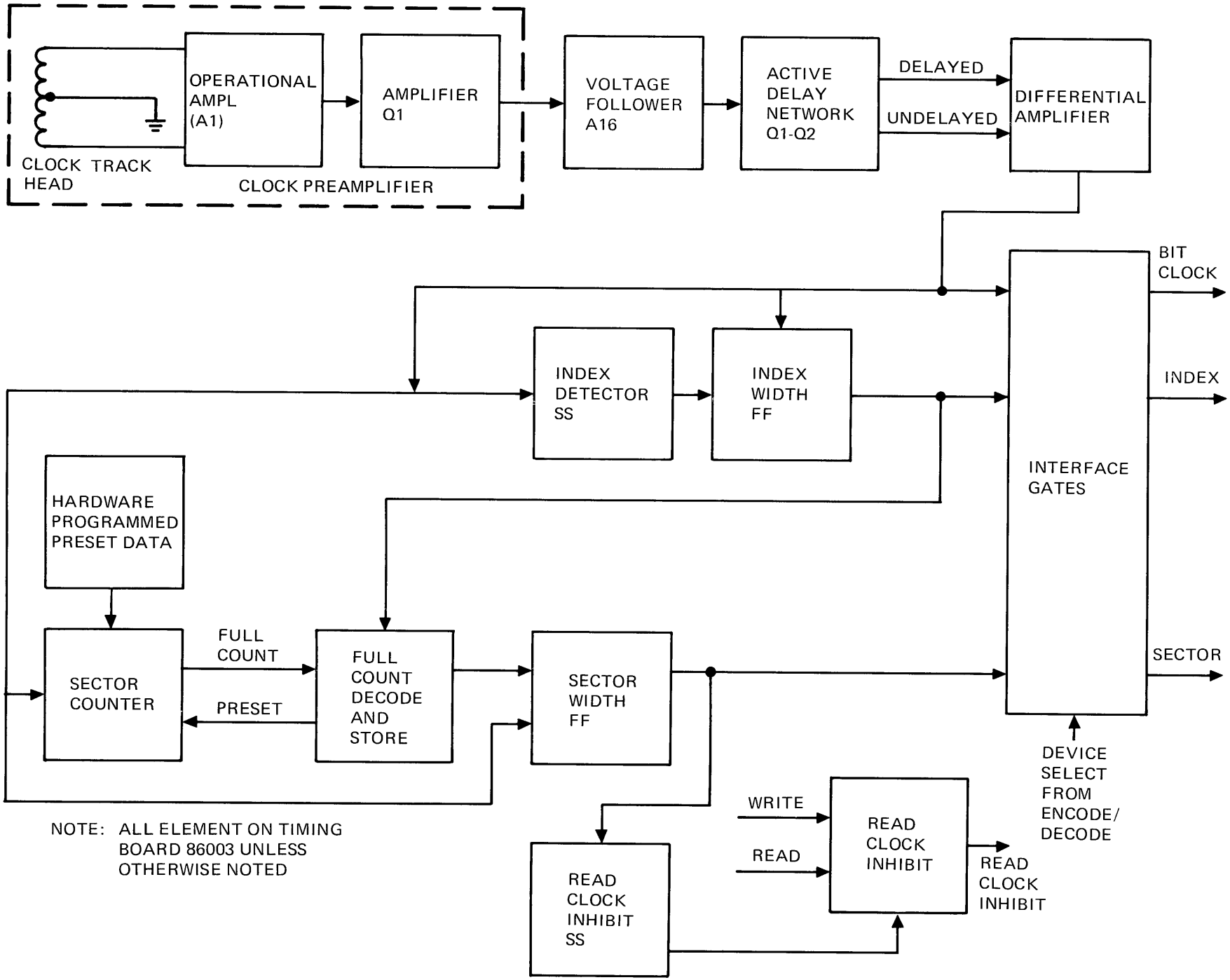


Figure 4-7. Timing Logic Block Diagram

4-7. TRACK SELECTION

Track selection functions for the Model 788 are illustrated in Figure 4-8. The case of the Model 788 is discussed first and then differences pertaining to the Models 388 and 688 are described. A single track selection circuit board 86003 provides track address decoding and drivers for addressing up to 128 tracks. This exceeds the maximum capacity provided by a Serial 88 Drum Memory. Two other types of circuit boards provide track selection functions. Each diode matrix circuit board 86009 provides diodes and pull-down resistors for eight data track heads. Up to 32 data track heads can be connected to a single read/write trunk. Associated with each read/write trunk is a read/write select circuit board 86006. The read/write select circuit board associated with the selected trunk connects that trunk to the read bus and, if a write operation is in progress, to the write bus.

Unselected data track heads within a trunk group are isolated from the trunk as a result of a negative voltage applied to their center-tap connections via pull-down resistors on circuit board 86007. This negative voltage reverse biases the diodes through which the head is connected to the trunk. An extra pair of diodes is used at the trunk output of each diode matrix circuit board. This lowers the total shunt capacitance of the trunk. (The capacitance introduced by each diode matrix circuit board is essentially the capacitance introduced by its output diodes. Without these diodes, each diode matrix board would contribute the parallel capacitance of the diodes associated with the individual heads.)

Figure 4-8 illustrates the read/write select circuit board and one diode matrix board for each of two trunks. External address data from lines 1 through 5 is supplied to a decoder which supplies 32 head selection signals (HCT 1 to HCT32). The true decode signal turns on an electronic switch transistor which connects constant current source CCS to the center tap of one data track head in each trunk group. However, since only one read/write select circuit is selected, current is actually drawn through only one data track head. The read/write select circuit selection is implemented by decoding the status of external address line 6. The two decoder outputs are supplied through driver circuits to the selection inputs of two read/write select circuit cards.

When a read/write select circuit card is selected, it connects the associated trunk to the read bus to the read amplifier. If the WRITE signal is being supplied, it also connects the trunk to the write bus from the encoder logic. When the trunk is connected to the write bus, one of the two lines of the trunk is connected to ground through the low impedance of conducting transisotrs. This permits write current to flow from the current source CCS, through the selected electronic switch, through the center tap connection of the selected data head, through hals of the data head winding and the diode at the end of the winding to the trunk line, through the trunk line and a conducting transistor in the read/write select switch, through the write bus line, and through a conducting transistor in the encoder logic to ground. A reversal of current in the data head is accomplished by reversing the selection of the write bus line which is grounded. This reversal causes the write current to flow from the center tap to the opposite end of the data head winding.

During a read operation, the selected trunk is connected to the read bus but not to the write bus. In series with the relatively high input impedance of the read amplifier, constant current source CCS appears as a voltage source rather than a current source so that relatively little current is drawn through the selected data head winding. However, CCS provides the positive polarity signal required to forward bias the diodes associated with the winding and thus accomplish its selection.

Track selection logic required to implement a 1-of-64 track selection has been described. If the number of tracks is reduced to 32, only one trunk is required and the number of address lines is reduced to 5. If the number of tracks is reduced to 16, only 4 address lines are required. Models 388 and 688 use diode matrix boards 86007 rather than 86009. Each diode matrix board 86007 provides diodes and pull-down resistors for three track heads.

4-8. POWER SUPPLIES

Figure 4-9 is a functional block diagram of the circuits provided by power supply circuit 86008. This circuit provides three power supplies which operate from a common power transformer with three secondary windings. Circuitry which monitors the +5 volt and −15 volt power supply outputs provides off/on control of the +25-volt power supply so that the +25-volt power supply does not turn on until after the other two power supplies are on and turns off as soon as either the +5-volt or −15-volt power supply output starts to drop.

The control signal from the +5-volt and −15-volt monitoring circuit also forms one input to the memory-not-ready/write-protect circuit. Other inputs to this circuit are from a circuit which monitors the +25-volt power supply output and the output of the +15-volt power supply located on timing circuit board 86002 and from a power turn-on delay circuit. As a result of these inputs, the $\overline{\text{MEMORY READY}}$ signal is placed at the active level and the $\overline{\text{WRITE PROTECT}}$ signal is placed at the level which inhibits the memory write function for a fixed delay period after power turn on and at any time when all power supply outputs are not present.

Each of the power supplies includes a series voltage regulator with a zener diode voltage reference. Each power supply also includes a current limiting switch stage which switches the power supply from the voltage regulating mode to a current limiting mode in the presence of a current overload. This protects the power supplies from short circuits. The +5-volt power supply also is equipped with an overvoltage protection circuit. This is an SCR crowbar circuit which places a short circuit across the output if the output voltage becomes excessive.

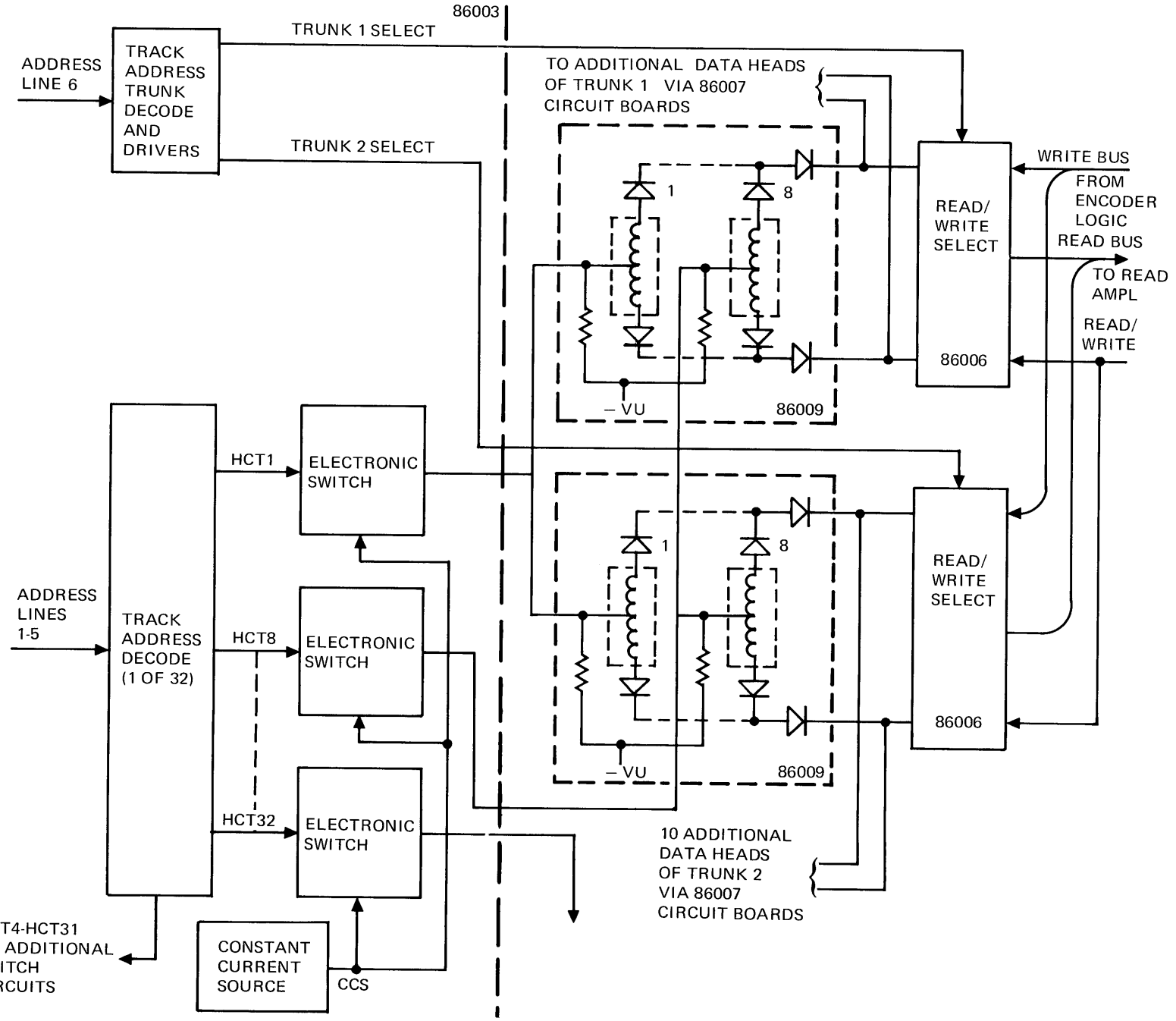


Figure 4-8. Track Selection

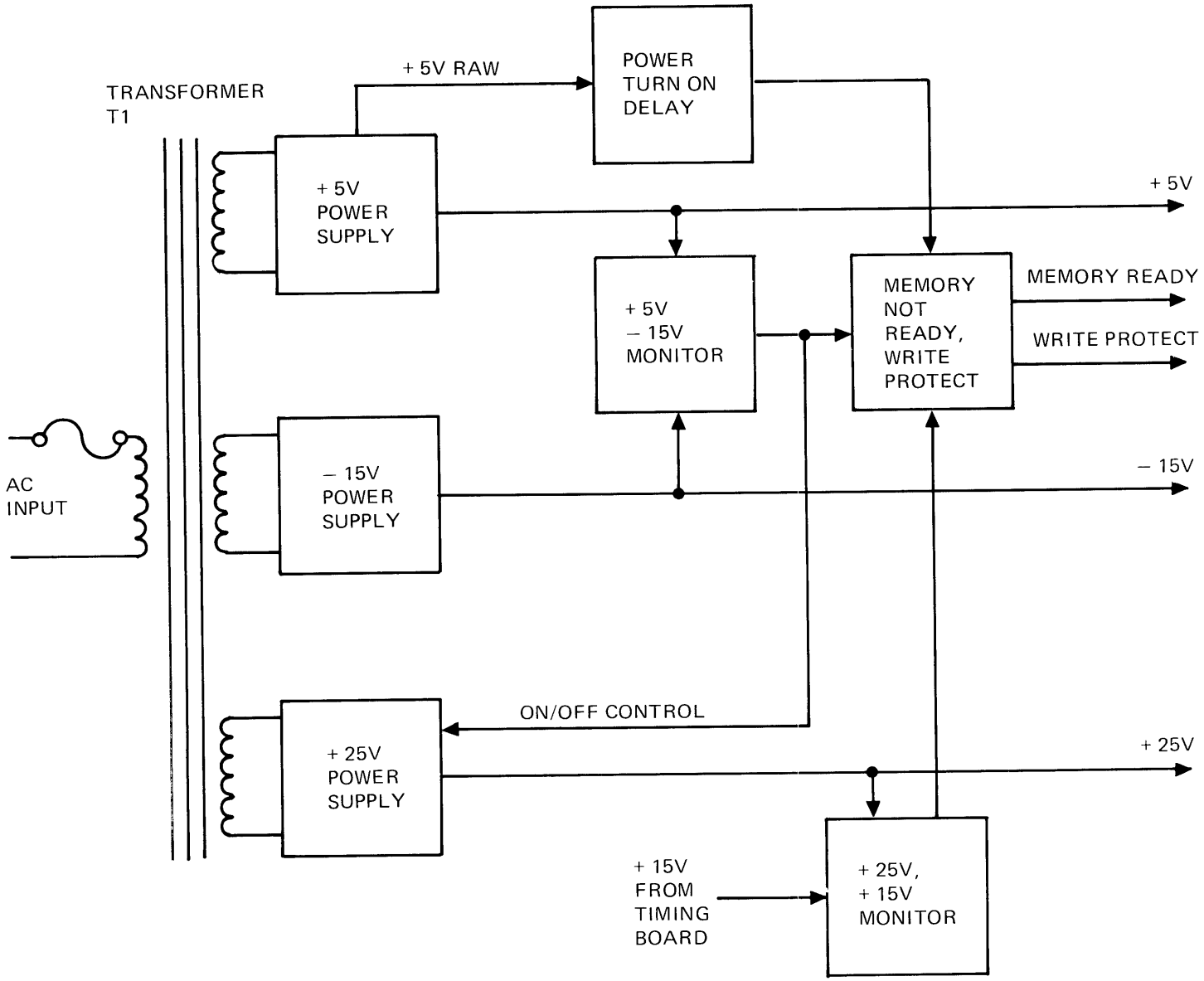


Figure 4-9. Power Supplies, Block Diagram

SECTION V MAINTENANCE

5-1. INTRODUCTION

Series 88 Drum Memory units are designed to give years of trouble free performance with a minimum of maintenance. The drum chamber provides a protected dust free environment for the critical interface between the rotating drum and flying heads. The chamber cover should never be removed unless absolutely necessary.

Caution: *The chamber cover is sealed and must remain in place during the warranty period. Breaking the seal will automatically void the warranty.*

5-2. PERIODIC MAINTENANCE

No lubrication is required nor should any lubrication procedures be attempted. Periodic maintenance is restricted to cleaning of those parts of the unit which are exposed to the environment. Use routine cleaning methods such as vacuum cleaning.

5-3. HEAD REPLACEMENT

Should it become necessary to replace heads, the safest procedure is to return the complete unit to the factory where replacement can be accomplished under controlled conditions and the unit can be purged during re-assembly.

If it does become necessary to replace a head in the field after the end of the warranty period, proceed as follows:

Caution: *This procedure must be performed in a clean, dust free environment and care must be exercized to avoid touching the surface of the drum.*

1. Turn off all power to the unit.

2. Remove top and bottom screws securing cover to unit and remove cover by carefully pulling straight up away from unit.

3. Locate defective head.

4. Unsolder three head leads from diode matrix board.

5. Remove screw securing diode matrix board to unit and move diode matrix board out of way to allow clearance for removal of head.

6. Remove screw securing head to head post and slide head assembly toward right until it clears head assembly.

7. Discard head assembly.

8. Slide new head assembly into groove as far as it will go.

9. Install screw which secures head assembly to post. While pressing down on top surface of head assembly, so as to insure correct orientation of assembly, tighten screw.

10. Position diode matrix board in mounting position and secure with screw removed in step 5.

11. Cut leads to appropriate lengths for connection to terminals on diode matrix board. (Refer to Figure 5-1 for connection information.) Install sleeving (1/16 diameter standard shrink tubing) on leads and solder leads to diode matrix board terminals.

12. Apply power to unit.

13. Write all 1's record on all segments of track whose head has been replaced.

14. Using oscilloscope with differential input preamplifier observe output of head across S and F terminals on diode matrix board.

Caution: *Do not connect oscilloscope probe grounds to C terminal of head. This terminal is at a positive potential. Connect probe grounds to chassis ground on unit.*

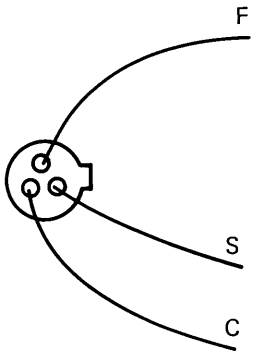


Figure 5-1. Head Connections

15. Loosen screw securing head assembly and observe head output as head assembly position is varied.

Note: *While varying head assembly position and when tightening screw securing head, push down on top surface of head assembly so as to maintain correct orientation of head assembly.*

16. Position head assembly so as to obtain maximum observed signal with minimum modulation. While holding head assembly in this position, retighten screw.

17. Repeat steps 13 through 16 until optimum signal is achieved.

Note: *Three or four passes through these steps is typical.*

5-4. USE OF TEST POINTS

Test points on circuit cards 86001 and 86002 provide a convenient means of verifying important signals. Table 5-2 lists the signal that appears at each test point on these two circuit cards.

Note: *Test points are numbered, in order, from top to bottom on each circuit card.*

TABLE 5-2
TEST POINTS

Test Point	Signal
	Circuit Card 86001 (Station A1)
1	+ PEAK single shot output
2	Decoder peak detector pulses
3	Decoder complement BLANKING single shot output
4	Decoder READ CLOCK single shot output
5	Decoder ONES flip-flop 1 output
6	Not used
7	Encoder ONES transition single shot output
8	Decoder DATA OUT flip-flop 1 output
9	Encoder WRITE DATA flip-flop clock line
10	Internal DATA IN
11	Encoder CLOCK TRANSITION single shot output
12	Encoder WRITE DATA flip-flop 1 output
13	Ground
	Circuit Card 86002 (Station A3)
1	Ungated BIT CLOCK
2	Ungated INDEX
3	Ungated complement BIT CLOCK
4	Ungated SECTOR

SECTION VI RECOMMENDED SPARES

6-1. INTRODUCTION

Table 6-1 summarizes the electronic parts used on each circuit board and on the power supply and lists a recommended number of spares for each different part number.

TABLE 6-1
PARTS COUNT AND RECOMMENDED SPARES

Assy. No. / Part No.	86001	86002	86003	86004	86005	86006	94024 Pwr. Sup.	Total	Recom. Spares
IC NH005C				1	1			2	1
7400	3	1	2			1		7	1
7404		1						1	1
7410	2	1						3	1
7420		1						1	1
7473	1	1						2	1
7476	1							1	1
74H01	1							1	1
74H21	1	3						4	1
74H22	1	1						2	1
74H40	2				1			3	1
8250			4					4	1
8291		4						4	1
9601	7	2						9	1
LM306		1			2			3	1
LM310		1			1			2	1
Transistor 2N1711							2	2	1
2N2905		2						2	1
2N3055							1	1	1
2N3565			36				21	57	5
2N3640				1	1			2	1
2N3643						2		2	1
2N3645			36			1	8	45	4
2N3646		2			2			4	1
2N4441							1	1	1
MJE203							1	1	1
MJE520		1					1	2	1
U1487E						3		3	1
Diode 1N705		1						1	1
1N707							3	3	1
1N749							2	2	1
1N752		2					1	3	1
1N914				4	4	2	17	27	3
US447							2	2	1
Diode 1N4005							1	1	1
Fuse, 1 Amp, S/B							1	1	1
Fuse, 1/2 Amp, S/B							1	1	1

SECTION VII SCHEMATIC DRAWINGS

86001 Data Encode/Decode

86002 Timing

86003 Head Selection

86004 Clock Pre-Amp

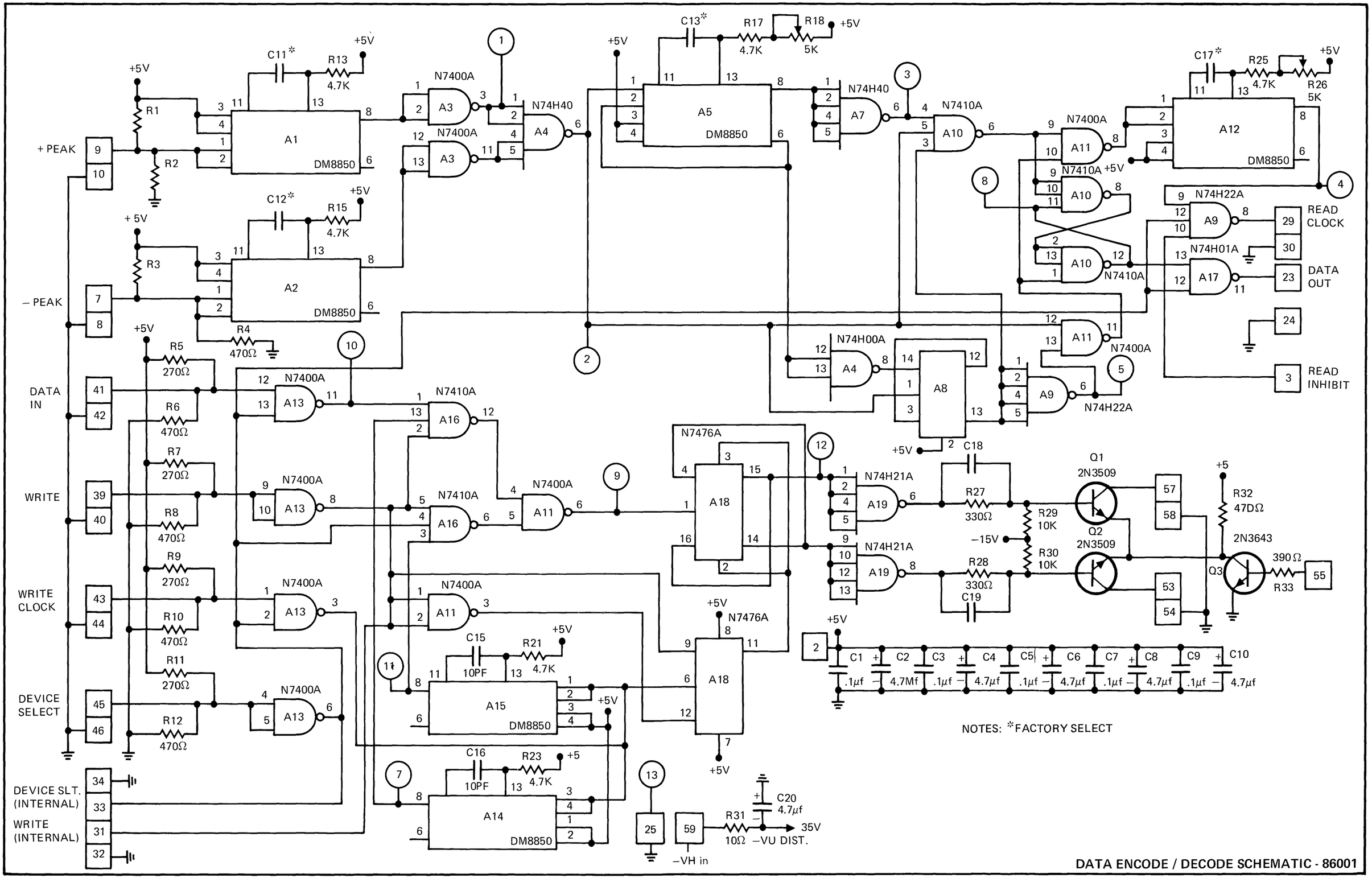
86005 Read Amp

86006 Write/Read Select

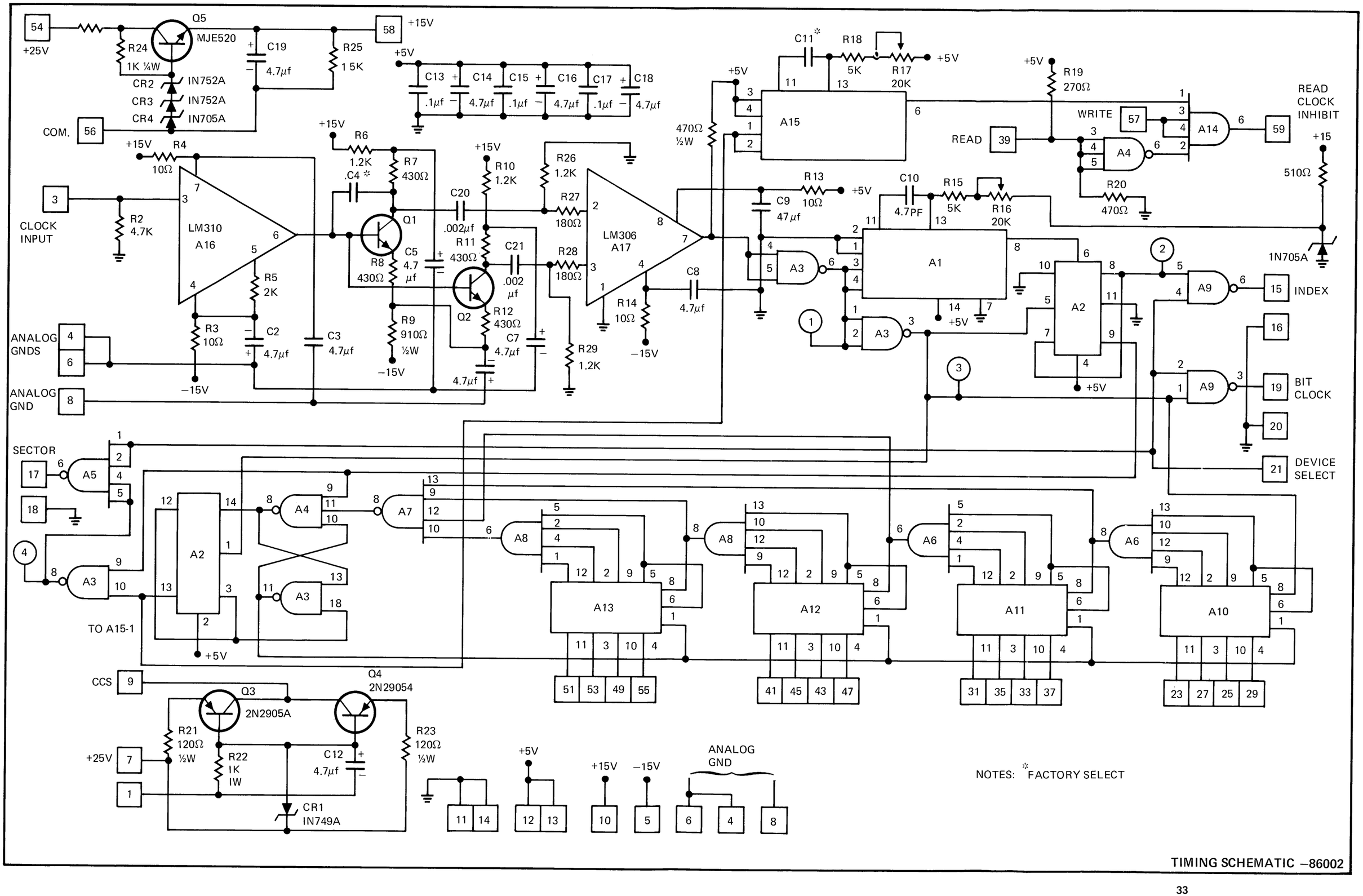
86007 Head Diode Matrix

86008 Power Supply

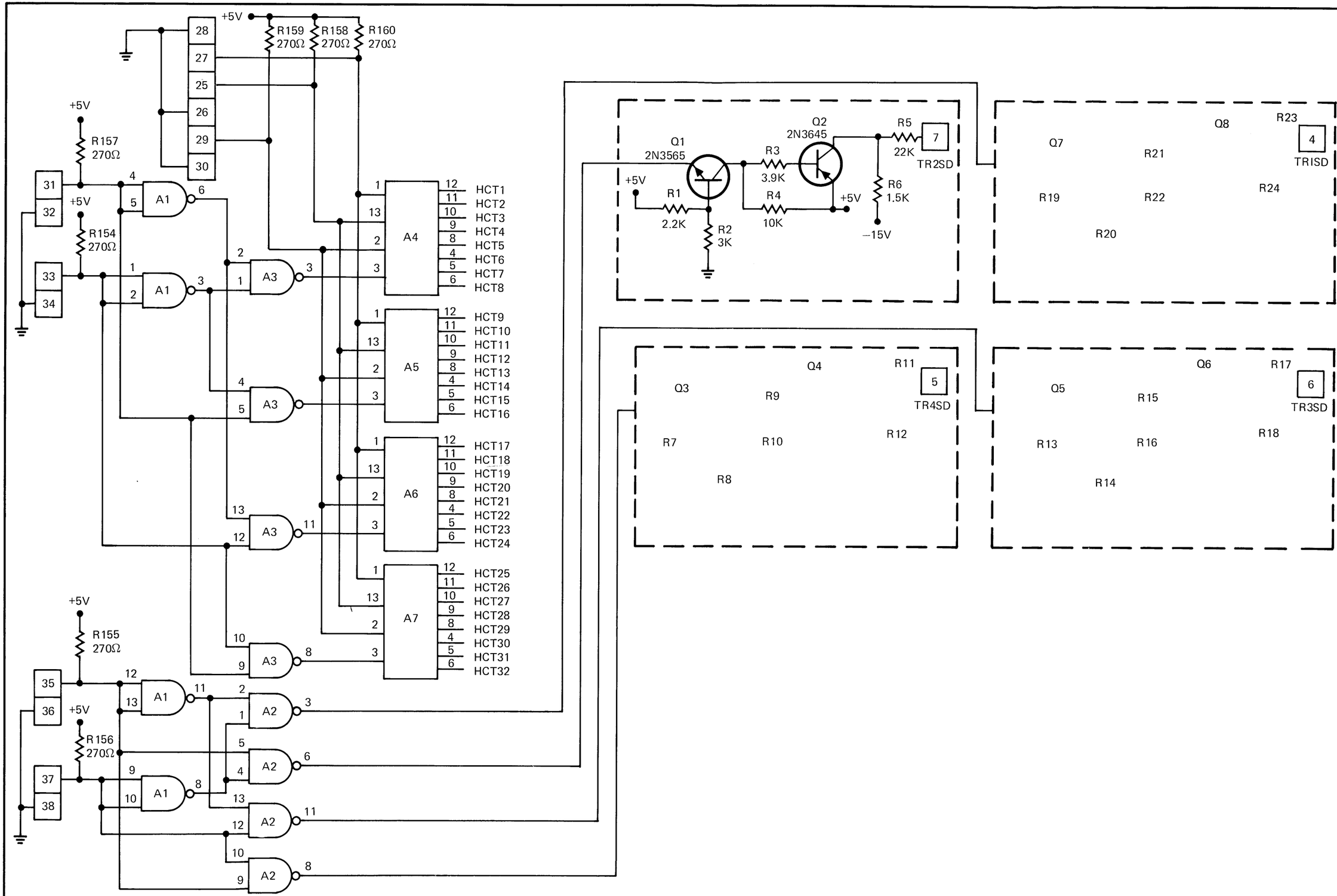
86009 Head Diode



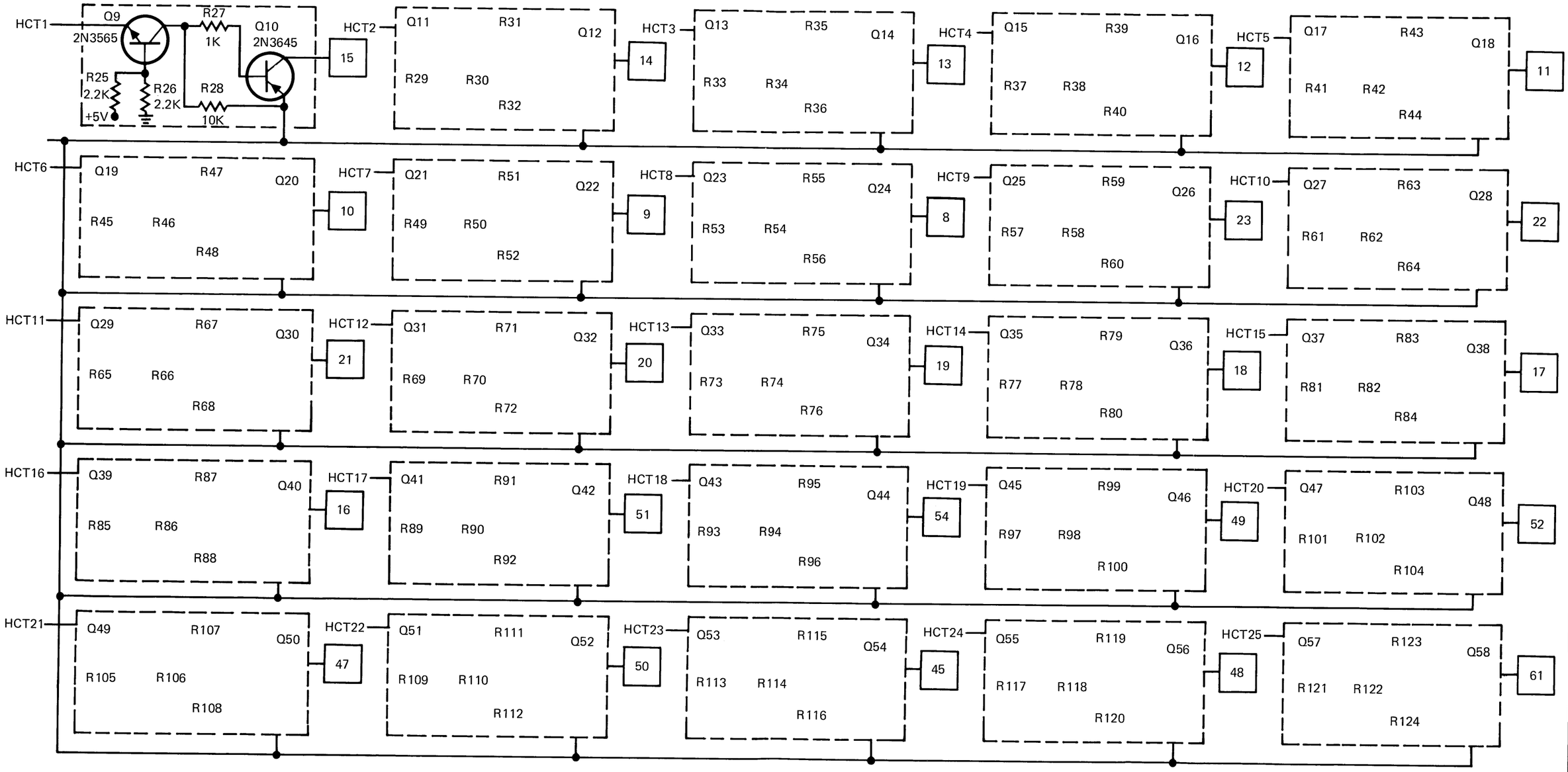
DATA ENCODE / DECODE SCHEMATIC - 86001



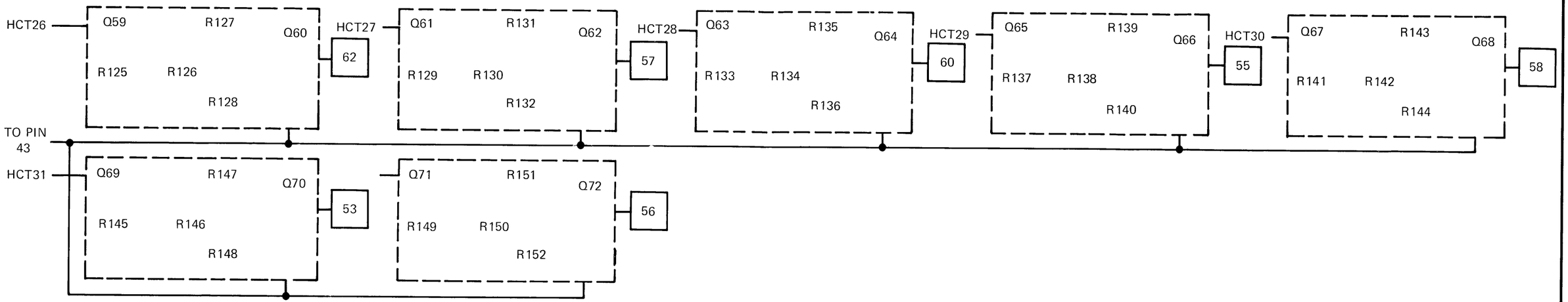
TIMING SCHEMATIC –86002

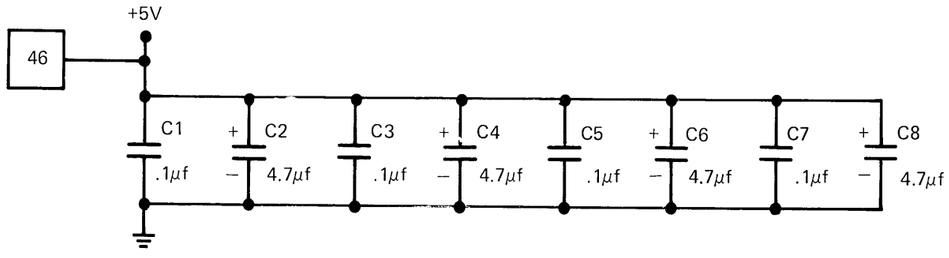


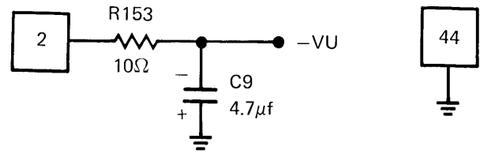
HEAD SELECTION SCHEMATIC - 86003



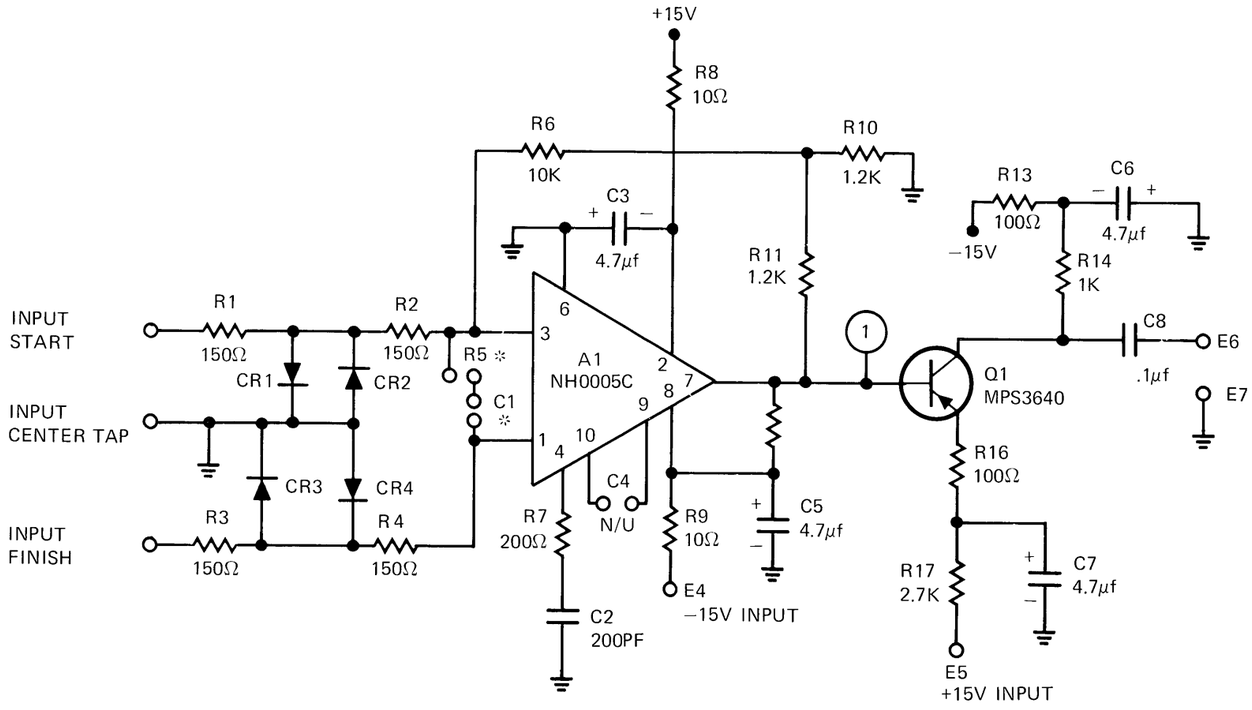
HEAD SELECTION SCHEMATIC – 86003





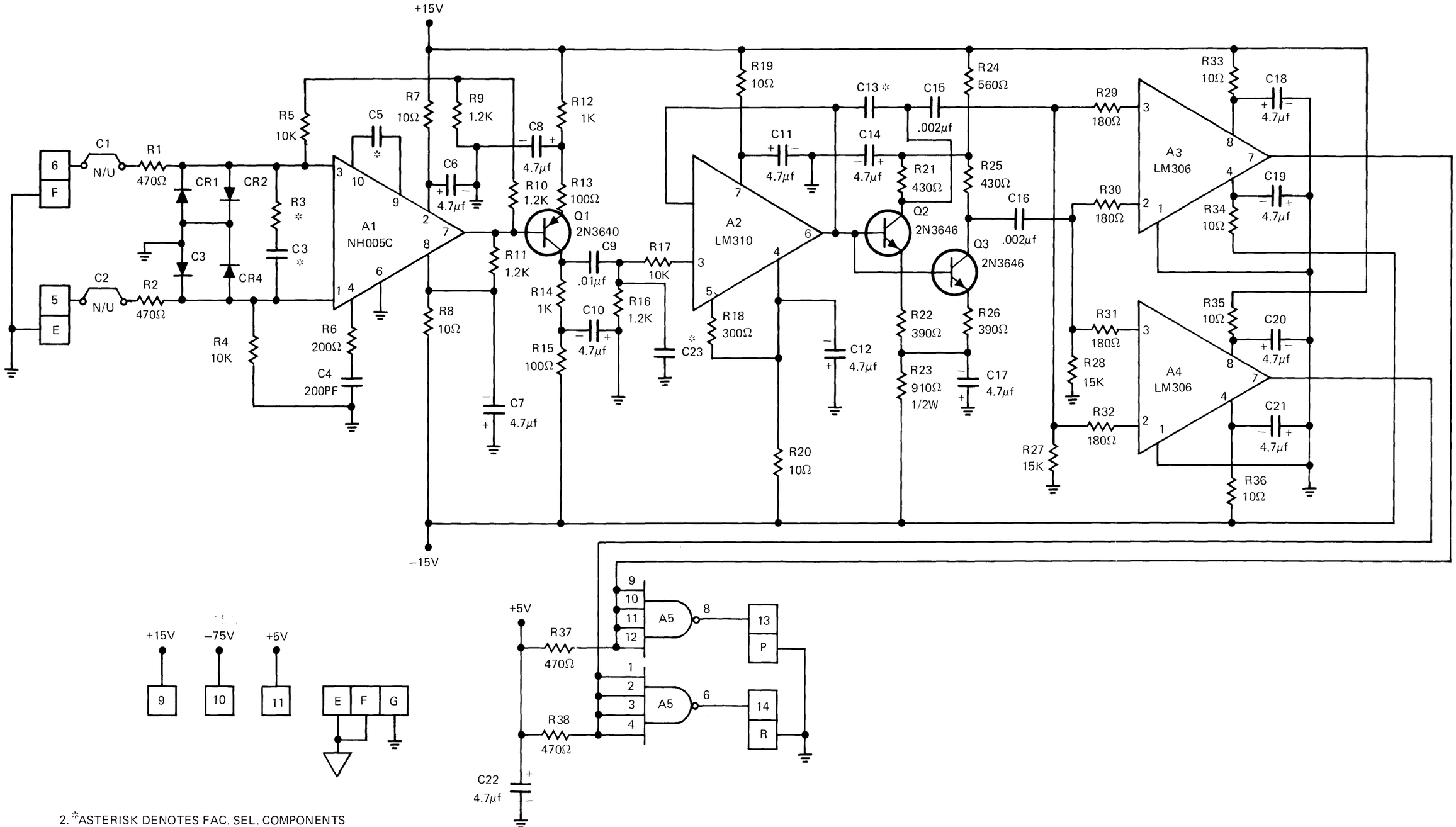


HEAD SELECTION SCHEMATIC – 86003



NOTES: 1. ✲ASTERISK DENOTES FAC. SEL. COMPONENTS

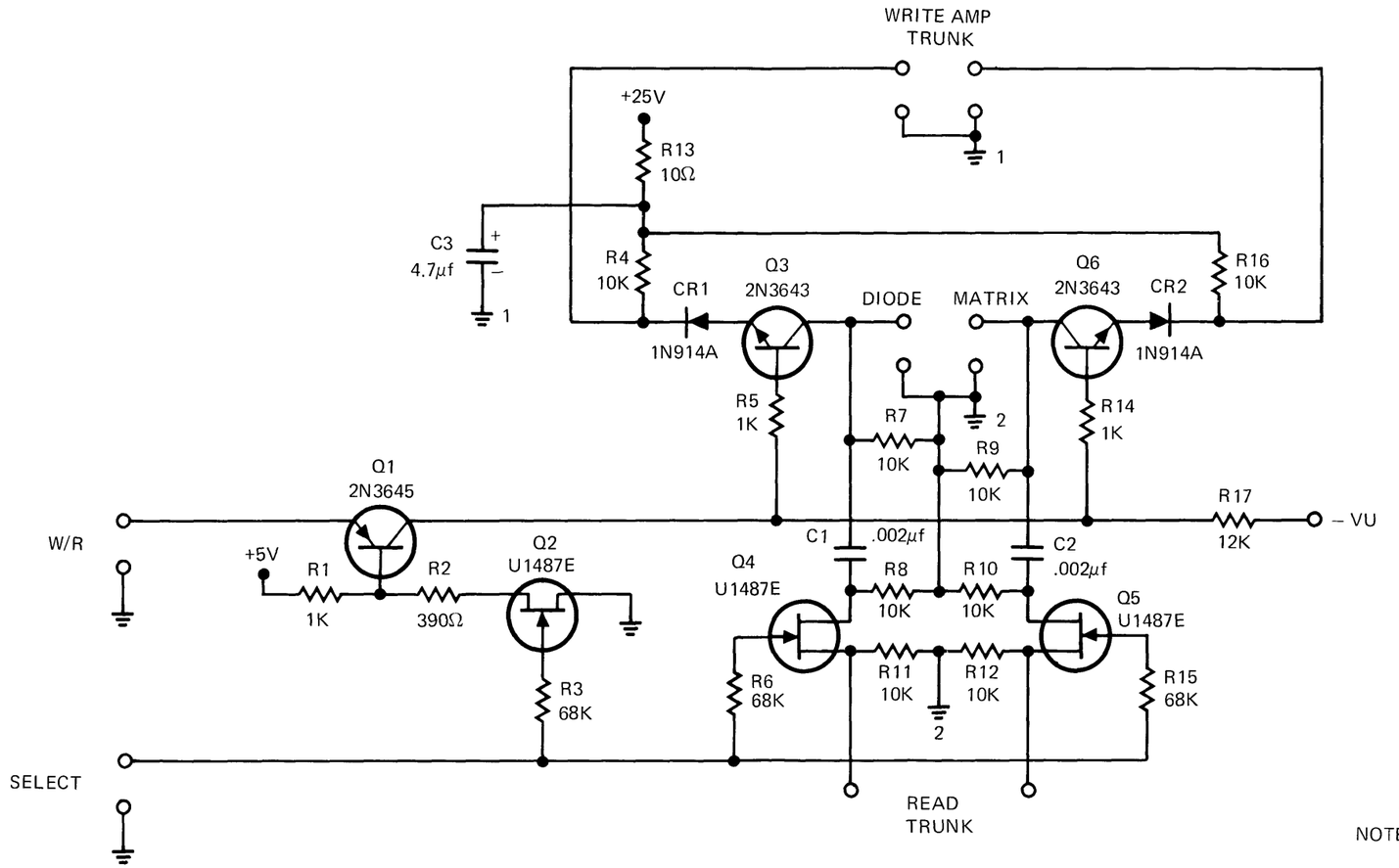
CLOCK PRE-AMP SCHEMATIC – 86004



2. *ASTERISK DENOTES FAC. SEL. COMPONENTS
1. ALL RESISTORS ARE 1/4W, 5%

NOTE: UNLESS OTHERWISE SPECIFIED

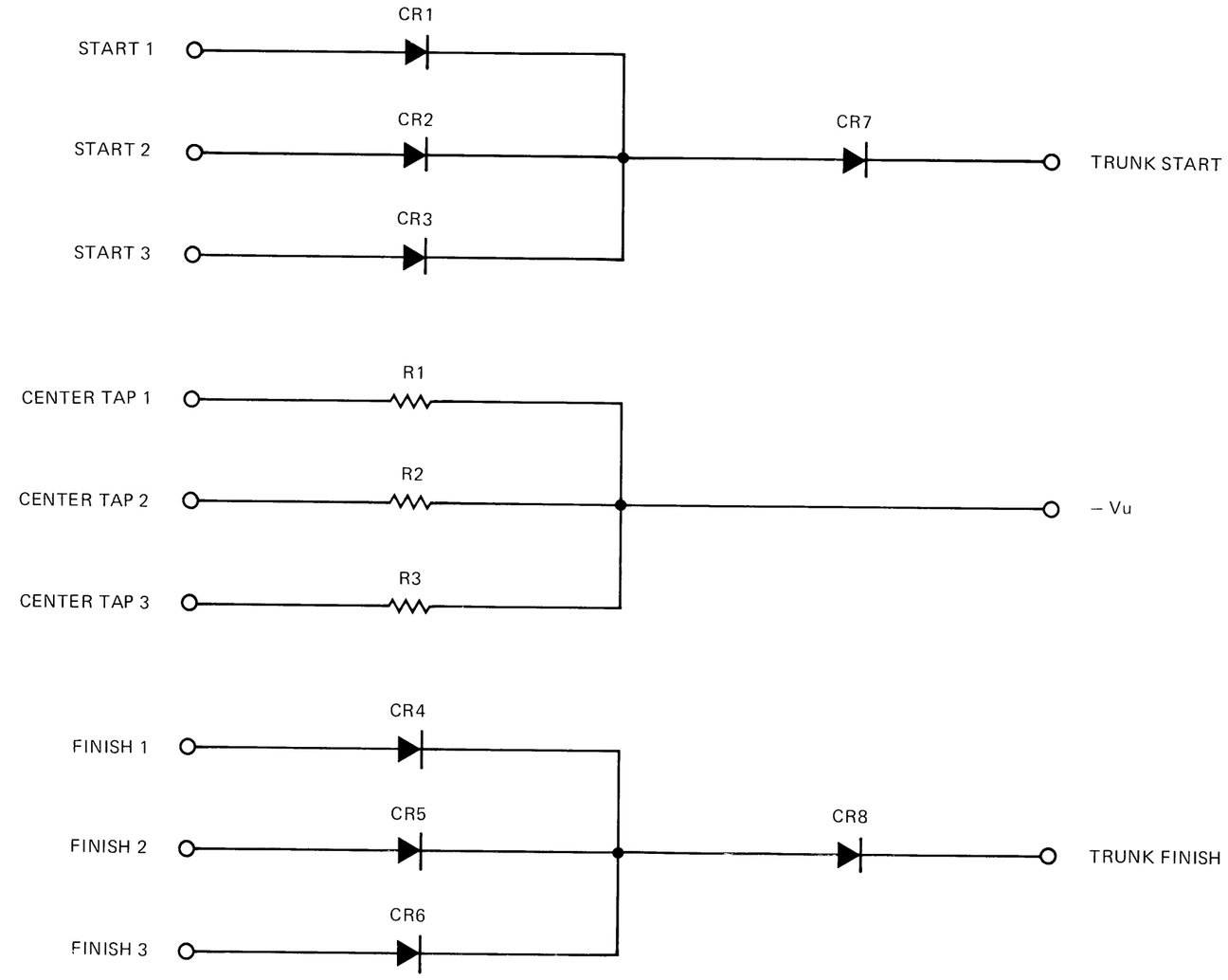
READ AMP SCHEMATIC - 86005



1. ALL RESISTORS ARE 1/4W, 5%

NOTE: UNLESS OTHERWISE SPECIFIED

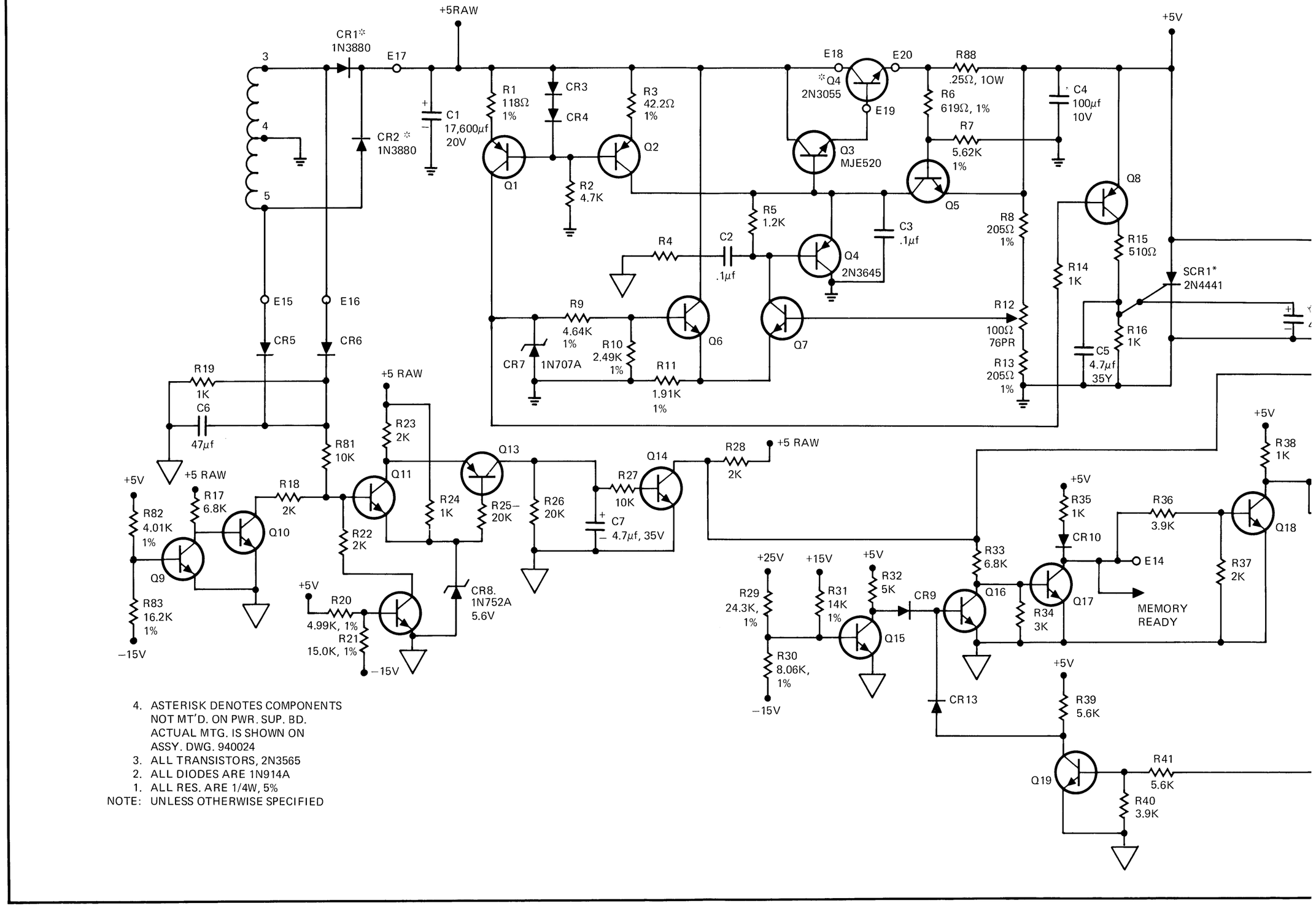
WRITE/READ SELECT SCHEMATIC – 86006



2. ALL RESISTORS ARE 10KΩ, 1/4W
1. ALL DIODES ARE 1N914

NOTE: UNLESS OTHERWISE SPECIFIED

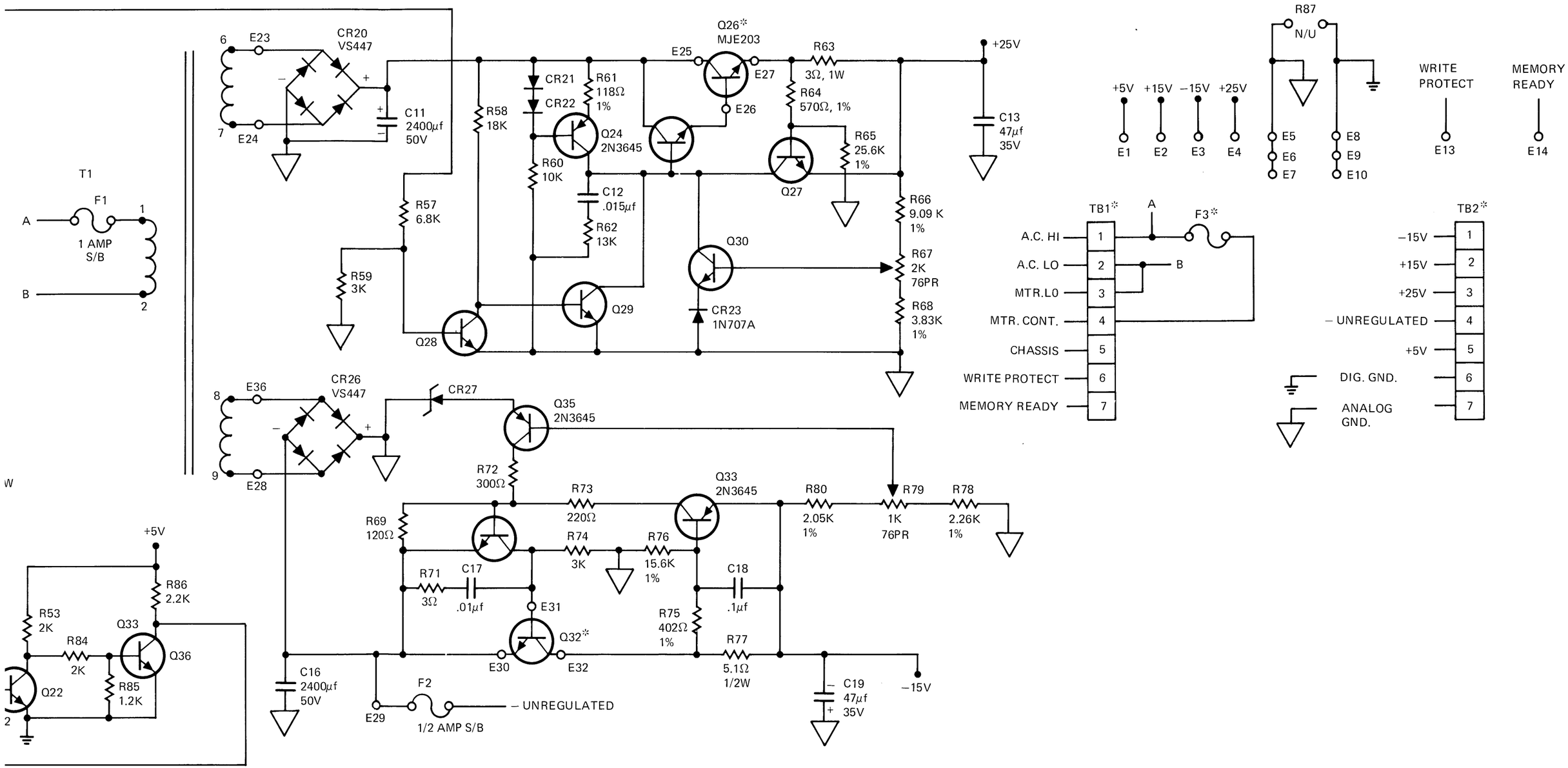
HEAD DIODE MATRIX SCHEMATIC - 86007



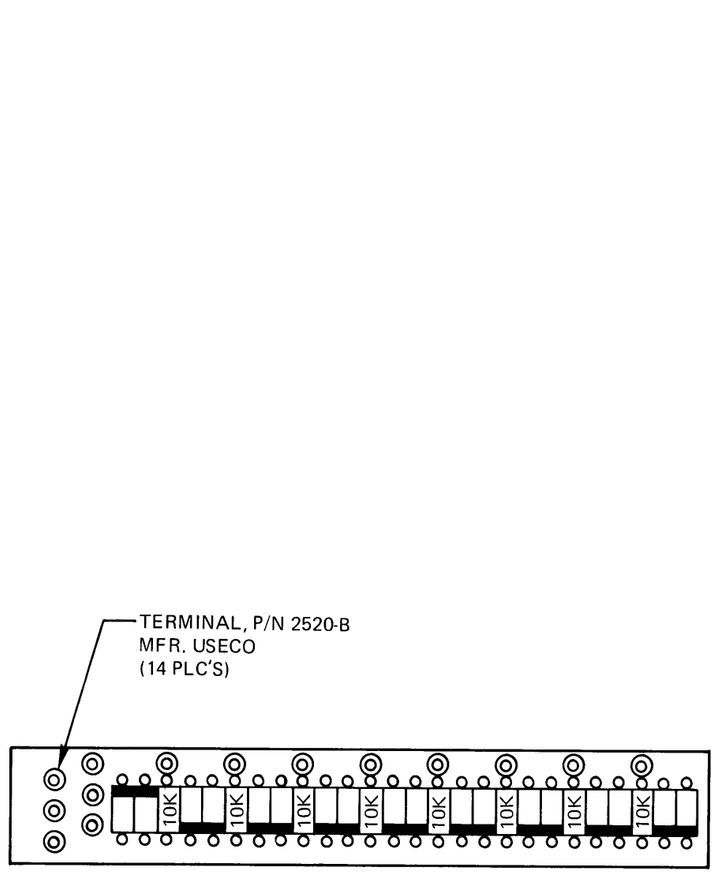
4. ASTERISK DENOTES COMPONENTS NOT MT'D. ON PWR. SUP. BD. ACTUAL MTG. IS SHOWN ON ASSY. DWG. 940024
3. ALL TRANSISTORS, 2N3565
2. ALL DIODES ARE 1N914A
1. ALL RES. ARE 1/4W, 5%

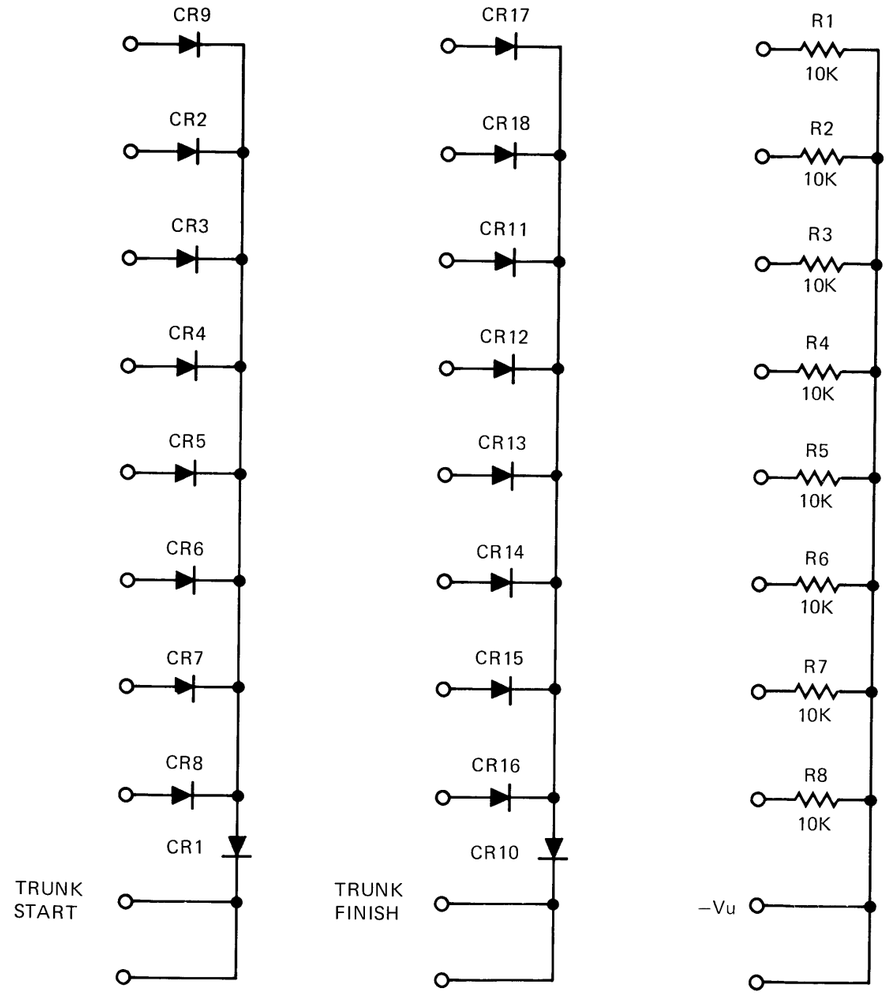
NOTE: UNLESS OTHERWISE SPECIFIED

+5RAW
R1*
3880
E17
C1
17,600µf
20V
CR2 *
1N3880
R1
118Ω
1%
CR3
CR4
R3
42.2Ω
1%
Q1
Q2
R2
4.7K
E18
E20
R88
.25Ω, 1OW
*Q4
2N3055
E19
R6
619Ω, 1%
R7
5.62K
1%
Q3
MJE520
Q5
C4
100µf
10V
+5V
Q8
R5
1.2K
R4
C2
.1µf
Q4
2N3645
C3
.1µf
R8
205Ω
1%
R15
510Ω
R14
1K
SCR1*
2N4441
4.7µf *
35V
R9
4.64K
1%
R10
2.49K
1%
CR7
1N707A
Q6
Q7
R11
1.91K
1%
R12
100Ω
76PR
R13
205Ω
1%
C5
4.7µf
35Y
R16
1K
* 4.7µf, 35Y
T1
F1
A
1 AMP
S/B
B
1
2
6
E23
CR20
VS447
7
E24
R59
3K
8
E36
CR26
VS447
9
E28
C16
2400µf
50V
+5 RAW
R23
2K
Q11
Q13
R24
1K
R25–
20K
R26
20K
R27
10K
C7
4.7µf, 35V
Q14
R28
2K
+5 RAW
R22
2K
CR8.
1N752A
5.6V
–15V
+5V
R38
1K
E13
WRITE
PROTECT
+5V
R35
1K
CR10
R36
3.9K
E14
MEMORY
READY
Q18
R37
2K
+25V
+15V
+5V
R29
24.3K,
1%
R31
14K
1%
R32
5K
CR9
R33
6.8K
Q16
Q17
R34
3K
R30
8.06K,
1%
Q15
–15V
CR13
+5V
R39
5.6K
Q19
R41
5.6K
R40
3.9K
+5 RAW
CR12
CR11
Q20
R43
40.2K, 1%
R44
2.4K
R42
2.4K
100µf
10V
CR14
1N749A
R55
15K
R54
1.2K
Q22
R53
2K
R84
2K
Q33
Q36
R86
2.2K
R85
1.2K



MEMORY POWER SUPPLY SCHEMATIC – 86008





2. ALL DIODES ARE 1N914A
1. ALL RESISTORS ARE 1/4W, 5%
NOTE: UNLESS OTHERWISE SPECIFIED

HEAD DIODE MATRIX ASSEMBLY & SCHEMATIC-86009

DATUM INC., CALIFORNIA PERIPHERAL DIVISION
170 East Liberty Ave., Anaheim, Calif. 92801 • phone (714) 879-3070 twx (910) 592-1289