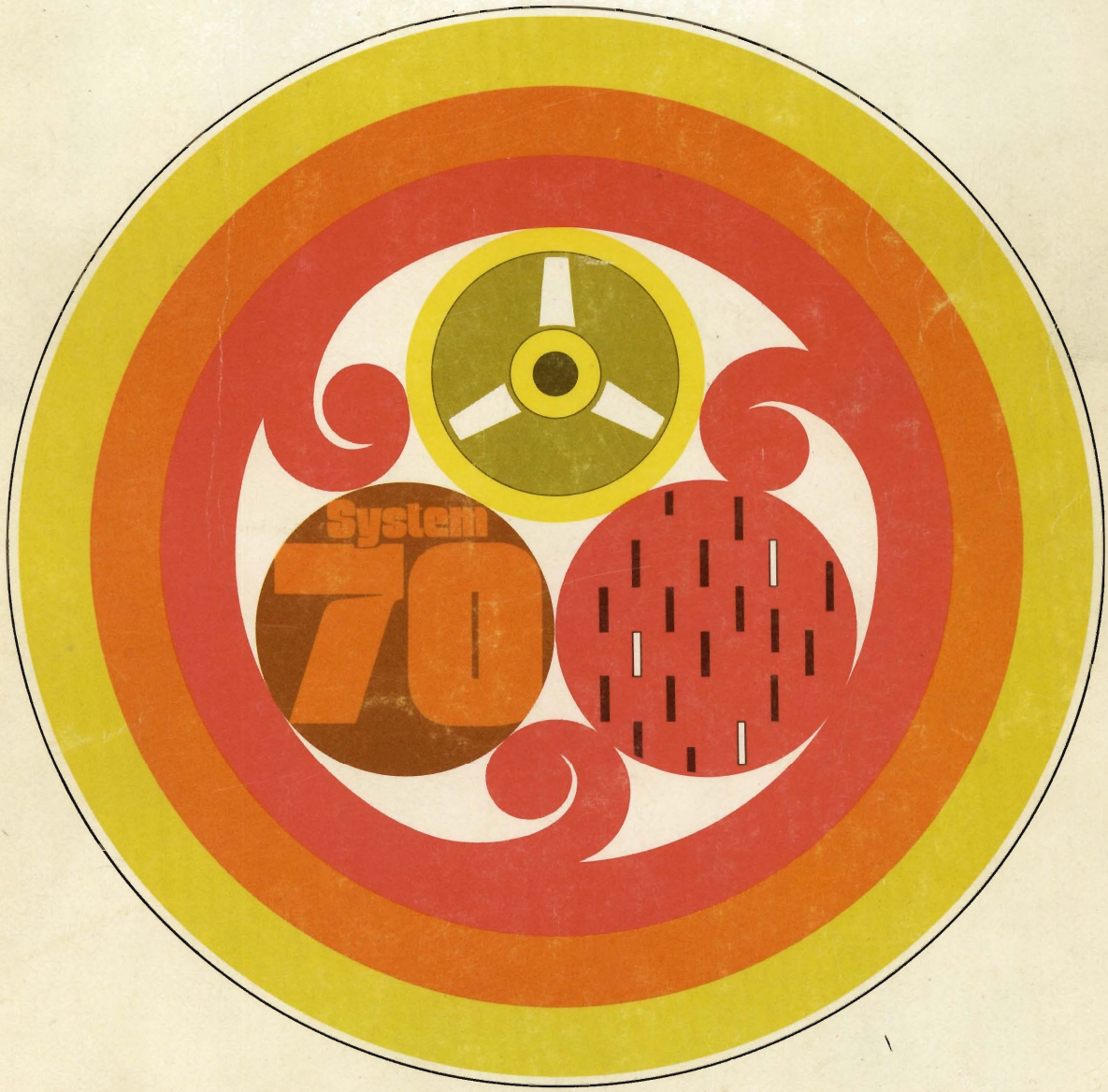
datum



PERIPHERAL EQUIPMENT DIVISION

INSTRUCTION MANUAL
FOR
MODEL 5091-PDP8e
MAGNETIC TAPE CONTROLLER

PUBLICATION NUMBER 1219.3

DATUM INC.
1363 South State College Boulevard
Anaheim, California 92806

ADDENDUM

The jumper table below is the standard configuration for the PDP-8E Tape Controller and is the way the unit will be shipped unless specific differences are called for by the customer.

BOARD	JUMPER POINTS	CONFIGURATION	RESULT
76225	E1 thru E13	Open	No Priority Selection
	E14 thru E24	No etch cut	No Priority Check
	E25 to E26	Open	No Interrupt at End of Data Cycle
	E26 to E27 NOT	Jumpered	Interrupt at end of CBUSY
76232	E1 to E2	Open	No 7-track file mark in 9-track core dump mode
	E3 to E4	Open	0 to 12 Conversion enabled
76233	E1 to E2	Jumpered	Check Vertical Parity on file marks
	E3 to E4	Open	Read after write present

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

List of Figures

List of Tables

SECTION I

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 FUNCTIONAL DESCRIPTION

The DATUM PDP8e Controller provides interface between the DEC PDP8e computer and 9-track, 800 BPI and/or 7-track 800/556/200 BPI tape machines, enabling computer-control of writing and reading IBM- or USACCII-compatible magnetic tapes.

All major operations are performed automatically under command of the Controller. Individual selection and operation with up to four "Daisy-Chained" tape transports is provided. Either single- or dual-gap machines can be accommodated.

Tape transport motion control, Cyclic Redundancy Check Character (CRCC) and Longitudinal Redundancy Check Character (LRCC) generation and checking, inter-record-gap generation and status reporting are included. All Write clocks and delay times are derived from a crystal-controlled oscillator. No "one-shots" or RC delays are utilized.

The unit plugs directly into the computer omnibus and uses computer power.

"On the Fly" operation (continuous read or write at maximum tape speed without stopping in each inter-record gap) is provided.

The IBM-compatible file mark (7- or 9-track formats) is written and recognized.

The "Edit" feature (allows a record anywhere on a previously recorded tape to be replaced with an updated record of equal size) is provided.

No calibration or adjustment potentiometers in the Formatter. All timing is derived from a crystal oscillator.

Compatible to entire 12.5 to 75-ips tape-speed range without changing crystals. A single field-changeable jumper selects the frequencies needed for the tape speed.

1.2 PHYSICAL DESCRIPTION

The DATUM Model 5091 NRZI Controller, complete on three large circuit boards, is designed to be installed in the PDP8e computer mainframe. Figure 1-1 shows this installation.

1.3 SPECIFICATIONS

Inter-record gap (7 track)	.75 inch nominal (.69 inch minimum)
Inter-record gap (9 track)	.6 inch nominal (.54 inch minimum)
Circuits	All silicon
Operating Temperature	0° to 50° C
Storage Temperature	-40° to +70° C
Altitude	0 to 20,000 feet
Relative Humidity	10 to 95% (non-condensing)
Interface Voltages (DTL 900 series or TTL 7400 series compatible)	low = 0V ±.4V high = 3.9V ±1.5V

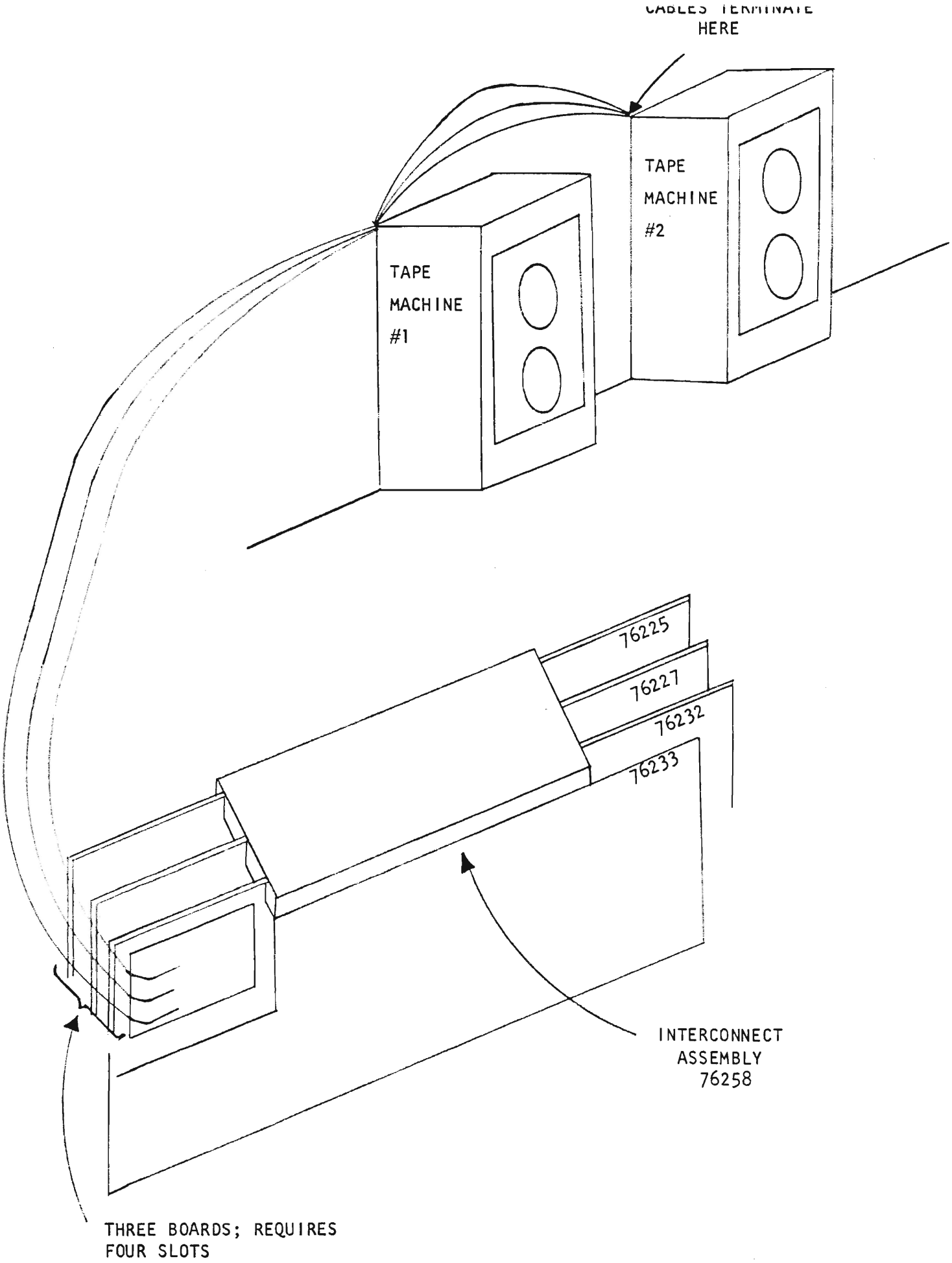


Figure 1-1. Installation of Model 5091 NRZI Controller

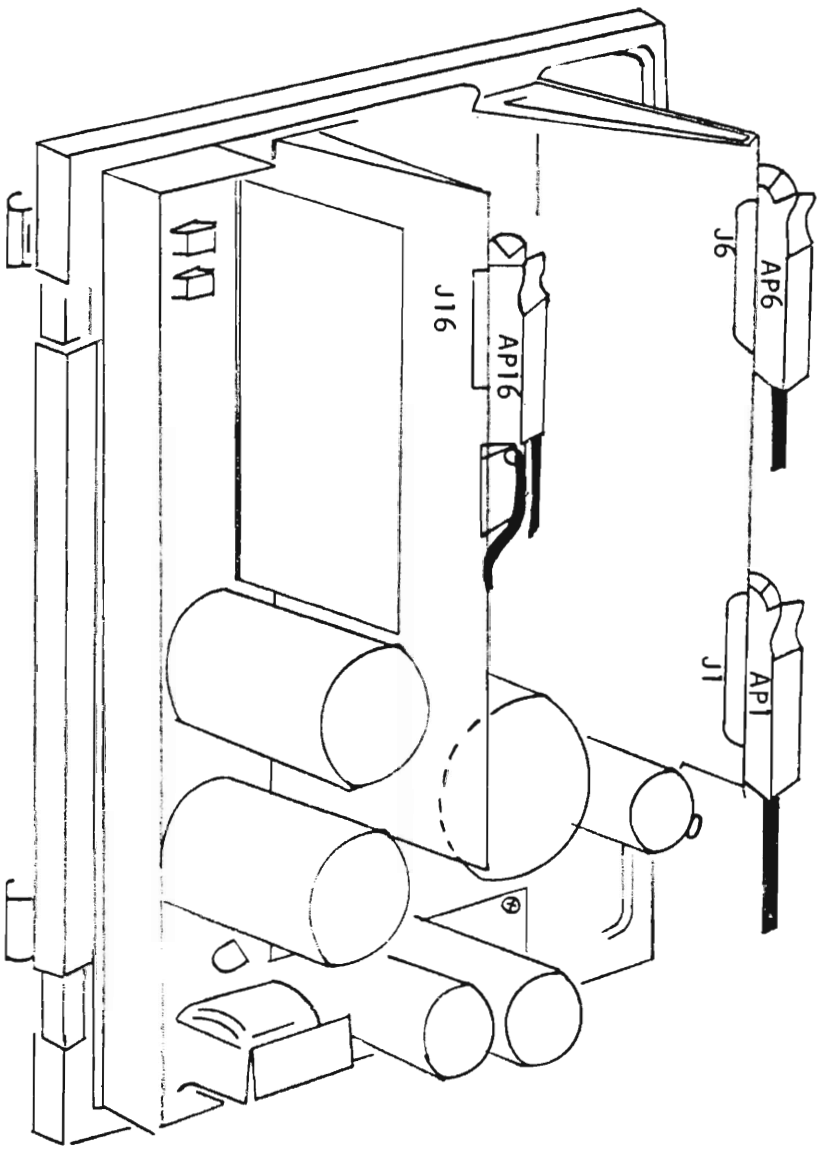


Figure 1-2. Wang NRZ Transport Interface Cable Connections

The interface is designed such that an open circuit is interpreted as a "high" signal.

Figure 1-3 illustrates the configuration for which the interface has been designed.

1.4 MAGNETIC TAPE FORMATS

Figures 1-4 and 1-5 illustrate the IBM and USASCII magnetic tape formats for 7-track and 9-track tapes, respectively.

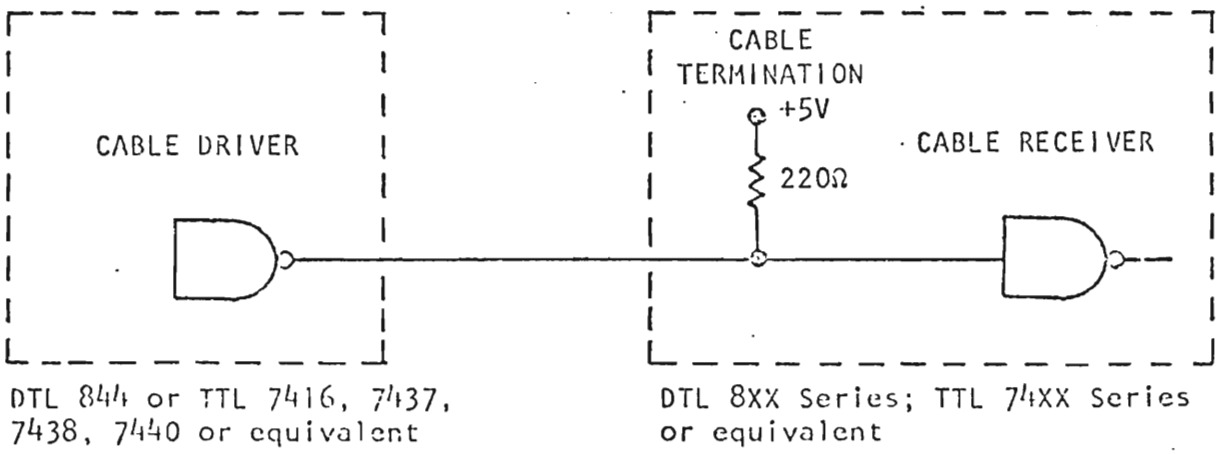
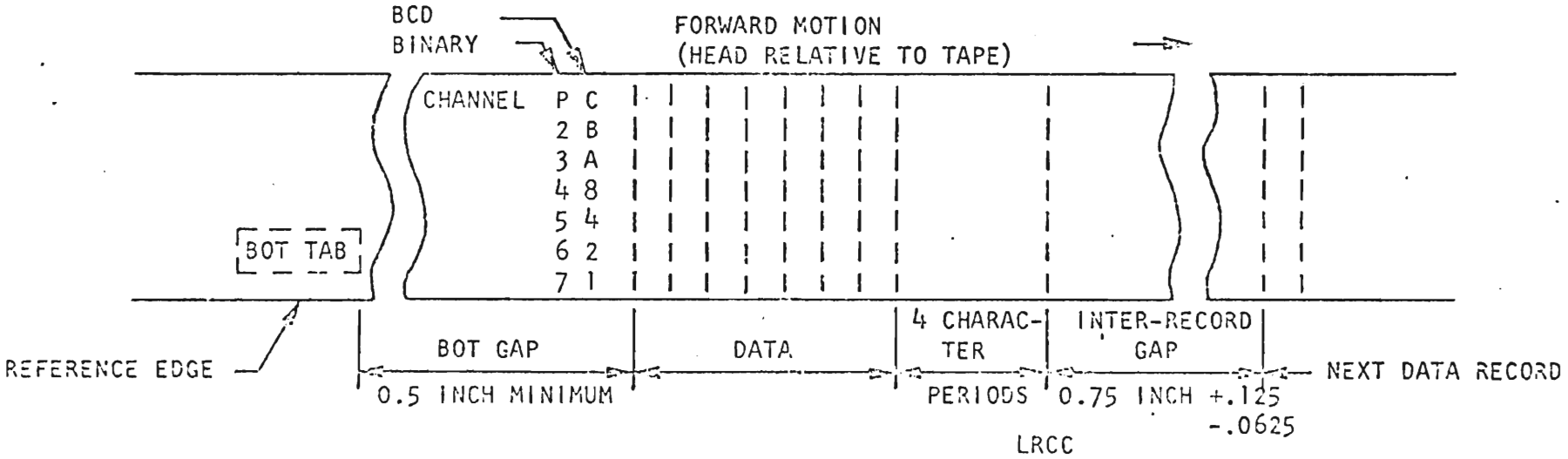


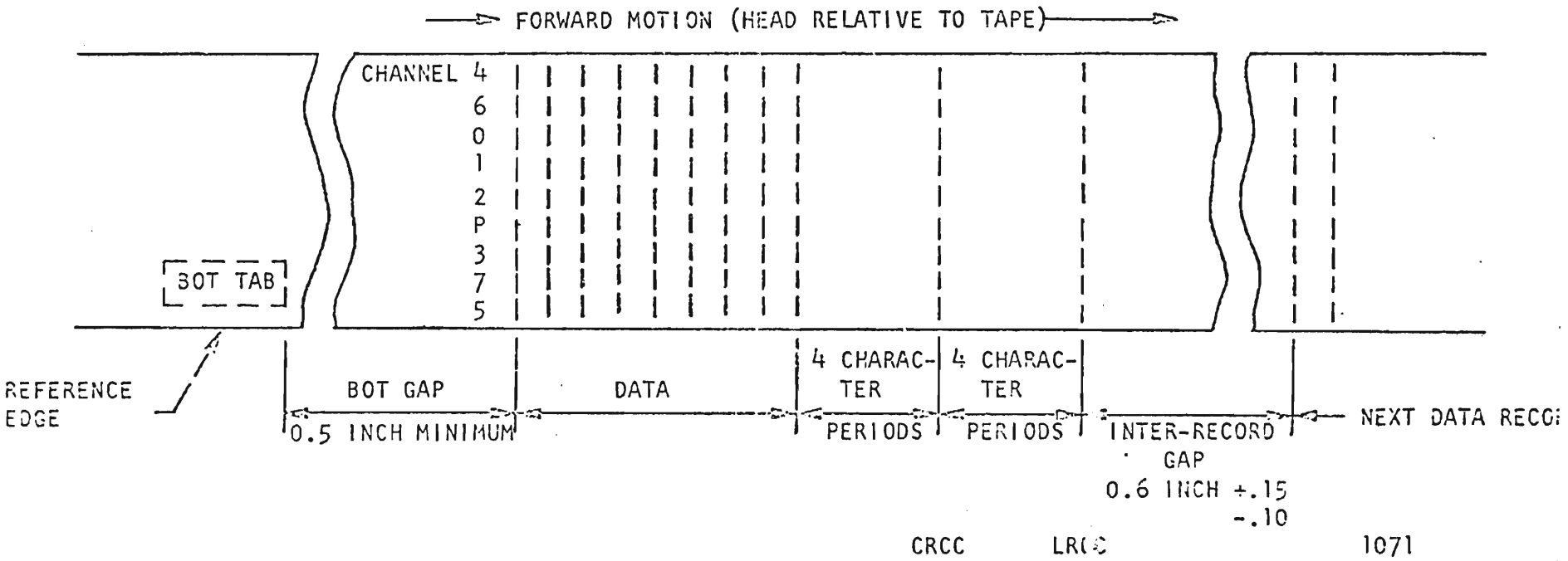
Figure 1-3. Interface Circuits



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) CONTAINS ODD DATA PARITY FOR BINARY TAPES, OR EVEN PARITY FOR BCD TAPES.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE LRCC) IS EVEN. IT IS POSSIBLE IN THE 7-TRACK FORMAT FOR THIS CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
5. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 4, 5, 6 AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE FILE MARK IS SEPARATED BY NORMAL IRG's (.75 INCH) FROM THE PREVIOUS AND FOLLOWING RECORDS. OPTIONALLY, A 3.5-INCH GAP CAN BE ERASED PRIOR TO WRITING THE FILE MARK.
6. DATA PACKING DENSITY MAY BE 200, 556, or 800 BITS PER INCH.

Figure 1-4. 7-Track Format



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRCC AND THE LRCC) IS EVEN. IN THE 9-TRACK FORMAT THE LRCC WILL NEVER BE AN ALL-ZEROES CHARACTER.
5. IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL ZEROES. THE FILE MARK IS SEPARATED BY NORMAL IRG's (.6 INCH) FROM THE PREVIOUS AND FOLLOWING RECORDS. OPTIONALLY, A 3.5 INCH GAP CAN BE ERASED PRIOR TO WRITING A FILE MARK.

Figure 1-5. 9-Track Format

SECTION II

INTERFACE

2.1 INTRODUCTION

There are two interfaces to the Controller Formatter section, one to the computer adapter section and one to the tape units (76232 A1, A2, C1 and C2).

Individual, stranded, 22-26-gauge twisted-pair wires should be used. Maximum length should be twenty feet (total) for the tape-unit "Daisy-Chain" bus.

The twisted-pair wire should have at least one twist per inch and a minimum insulation thickness of .01 inch.

The ground wire of each twisted pair should be terminated to ground as close to the origin or destination of the signal as possible (within 6 inches maximum) to minimize ground-loop-current "crosstalk" effects.

2.2 FORMATTER/TRANSPORT(s) INTERFACE

2.2.1 Formatter to Transport

2.2.1.1 Transport Address

$\overline{\text{SELECT A}}$ through $\overline{\text{SELECT D}}$ - Transport Select Lines. Four select lines to select one of the "daisy-chained" transports. Developed by decoding CR1 and CR2 from the command register.

2.2.1.2 Control

The control lines activate the selected transport when it is "READY" and "ON LINE".

$\overline{SFC}$ - Synchronous Forward Command. A levelwhich, when low, causes the selected transport to "ramp" up to speed and drive forward at the rated speed until the level goes back high. When switches to the high level, the transport "ramps" down to halt.

$\overline{SRC}$ - Synchronous Reverse Command. A level which, when low, causes the same action as $\overline{SFC}$ except in reverse tape motion.

$\overline{RWC}$ - Rewind Command. A negative-going pulse which causes the selected transport to rewind to load point.

$\overline{OFC}$ - Offline Command. A negative-going pulse which causes the selected transport to revert to manual control. Transport must be manually placed "ON LINE" before it can again be operated.

The offline command can be transmitted to a tape transport that is rewinding (even though the transport status indicates NOT READY).

$\overline{SWS}$ - Set Write Status. The level of this signal is inspected within 20 microseconds after an SFC or SRC command is initiated to set the selected transport to the write or read mode. This mode is maintained until the next SFC or SRC command is initiated.

The write mode within the transport is also switched to read mode if:

a) An RWC or OFC command is received.

b) Loss of interlock occurs.

c) The transport is manually switched offline.

$\overline{\text{EDIT}}$ - (Over Write). - This signal is a level that causes the transport write current enable/disable to "ramp" on and off to minimize rate of change of recorded inter block gap magnetism when rewriting a record in the EDIT mode.

This signal level also causes the write current and DC erase head current to be turned off immediately after rewriting the new record (to keep from erasing the beginning of the next record).

$\overline{\text{WARS}}$ - Write Amplifiers Reset. This signal controls the early turn-off of write and erase currents after rewriting a record in the EDIT mode.

The negative-going transition of this signal initiates the write current turn-off. In NRZI transports, this signal also generates the LRC character.

$\overline{\text{DDS}}$ - Select high density. Low = select high density (for NRZI Formatter only) for 7-track transport.

2.2.1.3 Write Data

$\overline{\text{WDS}}$ - Write Data Strobe. This is a clock used to copy the write data ($\overline{\text{WDP}}$ and $\overline{\text{WD0}}$ through $\overline{\text{WD7}}$) into the selected transport write flip-flops. The data levels must be static during $\overline{\text{WDS}}$ and the trailing edge (positive-going) of $\overline{\text{WDS}}$ is used to clock the flip-flops. The clock rate is twice the character rate for 1600 CPI and at the character rate for NRZI.

$\overline{\text{WDP}}$, $\overline{\text{WD0}}$ through $\overline{\text{WD7}}$ - Write data. $\overline{\text{WDP}}$ is the odd parity bit, $\overline{\text{WD0}}$ is the most significant bit, and $\overline{\text{WD7}}$ is the least-significant bit. $\overline{\text{WD0}}$ and $\overline{\text{WD1}}$ are not used for 7-track NRZI operation.

These signals are presented to the selected transport along with the $\overline{\text{WDS}}$ clock. The write data is presented in a logic-level form (low = logic 1, high = logic 0).

2.2.2 Transport to Formatter

2.2.2.1 Status Lines.

$\overline{\text{RDY}}$ - Ready. A level that is low only when the selected transport is:

a) Interlocked

b) Through the initial load or rewind-to-load point sequence.

c) On line

d) Not rewinding

Note: A transport will go NOT Ready for approximately .5-second after reversing into load point and does not go Ready until approximately .5-second after termination of a Rewind.

$\overline{\text{ONLINE}}$ - On line. A level that is low when the selected transport is manually switched on line (to place it under remote control).

$\overline{\text{REWINDING}}$ - Rewinding. A level that is low while the selected transport is rewinding. The level remains low until the transport completes the automatic "return to load point" sequence but the transport does not become Ready until approximately .5 second after the $\overline{\text{RWD}}$ signal terminates.

$\overline{\text{FPT}}$ - File Protect. A level that is low when the selected transport has a supply reel of tape mounted that does not have a write-enable ring installed.

$\overline{\text{LDP}}$ - Load Point. A level that is low when the selected transport's beginning-of-tape reflector is located under the photo sensor, interlocks are made, and the initial load or rewind sequence is completed.

$\overline{\text{EOT}}$ - End of Tape. A level that is low when the end-of-tape reflector is under the photo sensor in the selected transport. This signal is not staticised and neither the positive nor negative-going transition is "clean".

$\overline{\text{SINGLE}}$/DUAL - Head Stack. A level that reports the selected transport head type. Low for single stack, high for dual stack "read while writing".

7 TRK/9 TRK - Transport Type.

Low = 9-track

High = 7-track

$\overline{\text{DDI}}$ - Data Density Indicator

Low = High Density Selected

High = Low Density Selected

2.2.2.2 Read Data & Read Clock

$\overline{\text{RDP}}$, $\overline{\text{RD0}}$ through $\overline{\text{RD7}}$ - Read Data

2.2.2.3 Read Data & Clock

The read data is completely "buffered" in a special register. The data is allowed to change just before the leading edge of the read strobe pulse ($\overline{\text{RSTROBE}}$) and is static throughout $\overline{\text{RSTROBE}}$ and until the leading edge of the next $\overline{\text{RSTROBE}}$ pulse.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section contains information on the operation of the NRZI Magnetic Tape Controller.

The information in this section is divided into two major topics. A discussion of the block diagram (Figure 3-1) is presented first, to provide an overall functional description and to illustrate the relationship between the formatter portion, the adapter portion and a discussion of the command execution, illustrated by timing diagrams, describes operation of the Controller circuitry during execution of computer-originated instructions.

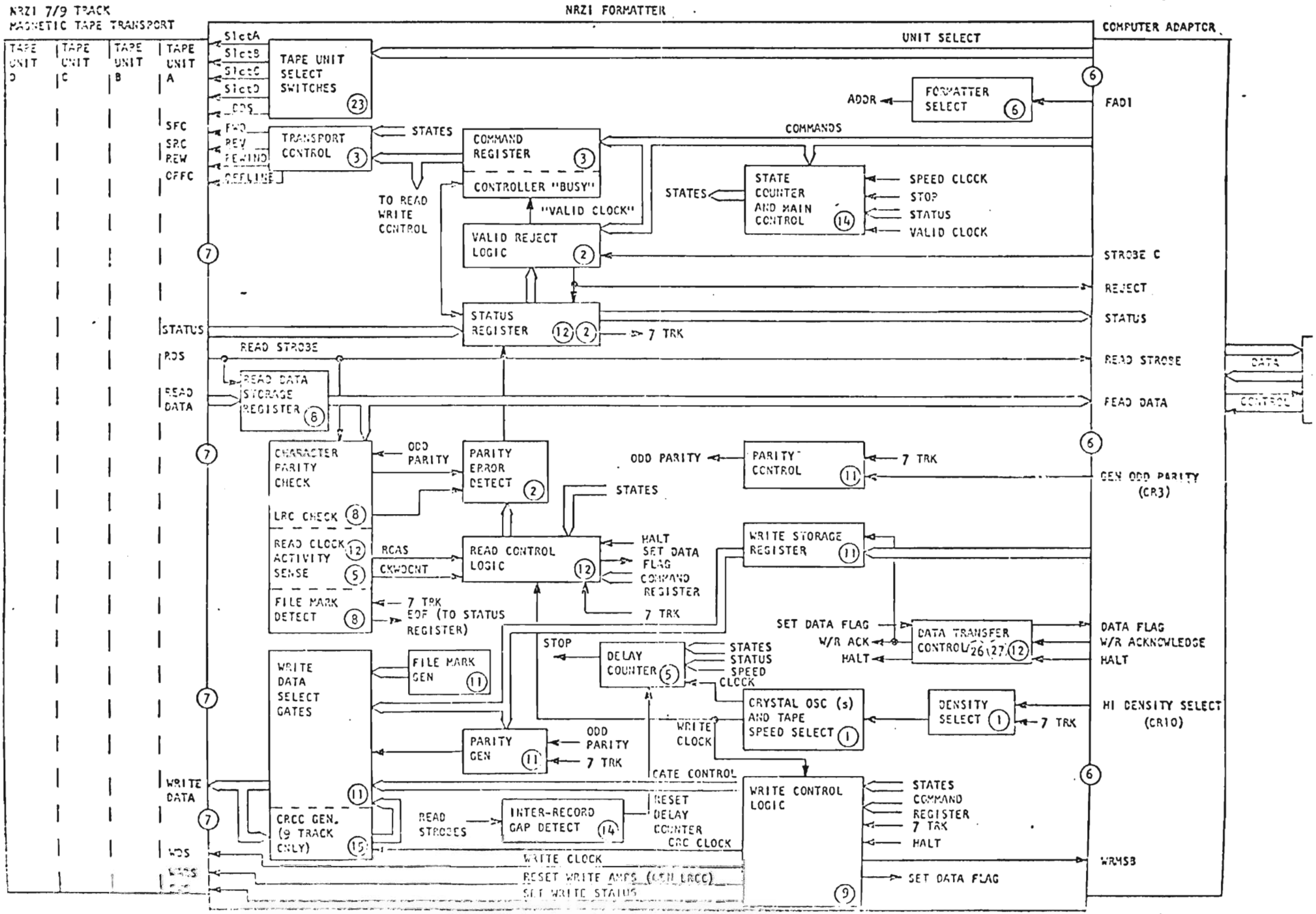
The Controller performs three basic functions. These are:

1. Control
2. Write
3. Read

The Controller provides control over the selected tape unit including all timing necessary to perform automatically all Write, Read, Rewind, Space Forward or Backward, and Rewind commands.

Upon completion of the commanded operation, status is provided so that the computer can ascertain whether the operation was performed correctly.

The Controller performs all the Write functions for erasing tape, writing a file mark or writing a record of data. A 3.5-inch gap is automatically erased before the first record when starting from beginning of tape (BOT). The correct timing delays for erasing the inter-record gap (IRG) are provided and the file-mark code is developed by the formatter portion of the Controller.


NRZI 7/9 TRACK
MAGNETIC TAPE TRANSPORT
NRZI FORMATTER
COMPUTER ADAPTOR
TAPE UNIT D
TAPE UNIT C
TAPE UNIT B
TAPE UNIT A
SlctA
SlctB
SlctC
SlctD
TAPE UNIT SELECT SWITCHES 23
UNIT SELECT
FADI
ADDR
FORMATTER SELECT 6
SFC
SRC
REW
OFFC
FWD
REV
REWIND
OFFLINE
TRANSPORT CONTROL 3
STATES
COMMAND REGISTER 3
COMMANDS
CONTROLLER "BUSY"
TO READ WRITE CONTROL
"VALID CLOCK"
STATE COUNTER AND MAIN CONTROL 14
SPEED CLOCK
STOP
STATUS
VALID CLOCK
VALID REJECT LOGIC 2
STROBE C
REJECT
STATUS REGISTER 12 2
7 TRK
STATUS
READ STROBE
RDS
READ DATA STORAGE REGISTER 8
READ DATA
DATA
CONTROL
CHARACTER PARITY CHECK
ODD PARITY
PARITY ERROR DETECT 2
LRC CHECK 8
PARITY CONTROL 11
GEN ODD PARITY (CR3)
READ CLOCK ACTIVITY SENSE 12 5
RCAS
CKWDCNT
READ CONTROL LOGIC 12
HALT
SET DATA FLAG
COMMAND REGISTER
WRITE STORAGE REGISTER 11
FILE MARK DETECT 8
EOF (TO STATUS REGISTER)
SET DATA FLAG
W/R ACK
HALT
DATA TRANSFER CONTROL 26 27 12
DATA FLAG
W/R ACKNOWLEDGE
HALT
STOP
DELAY COUNTER 5
CLOCK
WRITE DATA SELECT GATES
FILE MARK GEN 11
CRYSTAL OSC (s) AND TAPE SPEED SELECT 1
DENSITY SELECT 1
HI DENSITY SELECT (CR10)
PARITY GEN 11
WRITE CLOCK
GATE CONTROL
WRITE DATA
CRCC GEN. (9 TRACK ONLY) 15
READ STROBES
INTER-RECORD GAP DETECT 14
RESET DELAY COUNTER
CRC CLOCK
WRITE CONTROL LOGIC 9
WRMSB
WRITE CLOCK
RESET WRITE AMPS (GEN LRCC)
SET WRITE STATUS
SET DATA FLAG

The task of writing is reduced to mere transfer of the characters on a demand-response basis for the computer-adapter logic.

The Controller also reduces the reading and spacing operations to a minimum by performing all parity checks and positioning of the head in the IRG's automatically. The task of reading is reduced to transfer of the characters on a demand-response basis.

The Controller can accommodate as many as four magnetic tape transport units simultaneously. All input/output signal lines are daisy-chained to the tape transports. Only the selected tape transport unit will respond to the Formatter commands. Select is determined by unit-select switches located on each tape unit.

3.2 BLOCK DIAGRAM

A simplified block diagram of the NRZI Formatting logic is shown by Figure 3-1. The block diagram illustrates the various functions performed by the standard 7-track, 9-track NRZI Controller and shows the relationship between the control, the tape transport units, and the computer adapter section.

The circled numbers refer to the "Logic Diagram Number" on which the indication function is drawn in detail. This number is located in the lower right hand corner of the detailed logic drawings.

3.2.1 Command Register & Valid/Reject Logic

When a command is output from the computer, the command and a strobe pulse are delivered from the computer-adapter segment to the Controller valid-command-detect logic. If the command is acceptable, a "valid" clock is generated to enable the command to be loaded into the command register. If the command is not valid, a "reject" pulse is returned to the computer adapter. Each "valid" clock initiates a system reset (SRS) pulse, which is, in turn, used to reset the Formatter to initial conditions.

3.2.2 CBUSY

The "valid" clock also sets the controller-busy flip-flop. The controller-busy flip-flop normally is used by the computer adapter to signal termination of all commands. The transport control logic resets the controller-busy flip-flop after all tape motion has ceased for the commanded function. If "on-the-fly" writing or reading is desired, the Data Busy status must be utilized by the computer to initiate the next command as soon as Data Busy terminates.

3.2.3 Transport Control

The transport control logic develops the forward, reverse, rewind and offline commands to the selected tape transport unit under control of the command register and the state counter.

3.2.4 Formatter Select

The Formatter select logic allows a Formatter to be assigned the number zero or one so that two Formatters can be "Daisy-Chain" connected to one adapter section to provide control of up to eight transports or of a mixture of NRZI and 1600 CPI Phase Encoded Transports.

3.2.5 Tape Unit Select

The Tape Unit Select switches allow the operator to assign unit numbers 0, 1, 2 or 3 to any of the four tape units. This allows physical tape units to be switched without requiring changes to the computer program. Indicator lamps give visual indication of which tape unit is selected.

3.2.6 State Counter and Main Control

The State Counter breaks the major operations (such as write and read) down into successive sub "states" that are sequentially stepped-through to perform the operation. These states are:

State Count	Function
0	Reset
1	Predelay (not BOT and not 3-inch gap)
2	Predelay (BOT or 3-inch gap)
3	Write or Read execution
4	Postdelay
5	Forward Motion Halt time out
6	Reverse Motion Halt time out
7	Rewind or Clear execution

The "delay" and "time out" states all use the Delay Counter to determine when the state count should terminate and the next state count entered. These delay count times vary, depending upon such factors as:

1. Tape speed
2. Single or dual-stack head
3. Edit or normal mode
4. Reverse or Forward motion
5. Seven or nine track tape unit selected

The pre and post delays are used to erase the inter-record gaps (IRG) and to halt the head in the correct position in the IRG when reading.

State 0 (the "rest" state) is the state the Controller enters after completing an operation.

State 1 (Predelay) is used to wait for the tape unit to get up to speed and to erase part of the IRG when writing. State 1 is used for predelay when not starting from BOT or not erasing a 3-inch gap.

State 2 (Predelay) is similar to State 1 except a longer delay is implemented to handle the 3-inch gap erased automatically at BOT and the Erase-3-Inch-Gap command.

State 3 (Write or Read Execution) is the State during which the record is written or read. When reading, State 3 is terminated when no more Read strobes occur (indicating the IRG has been reached).

IRG detection also terminates State 3 for Write operations when using a dual-stack read-after-write tape unit (so that the written record can be checked for correct parity). For single-stack writes, State 3 is terminated as soon as the LRC character is written at the end of the record.

State 4 (Postdelay) halts the head in the correct position in the IRG when reading. When writing, State 4 postdelay erases a portion of the IRG.

State 5 (forward motion halt time out) retains memory of the forward direction of motion during the time between the command to stop and the actual stop time. This delays termination of the CBUSY signal until the tape unit has completely halted in the IRG.

The DBUSY status terminates when State 5 is entered. Thus, successive "Writes" or successive "Reads" may be executed on-the-fly, without stopping in the IRG's.

State 6 (reverse motion halt time out) is similar to State 5 except for reverse motion commands. When performing on-the-fly operations, successive commands issued after DBUSY terminates but before CBUSY terminates must be of the same type. A Read cannot follow a Write and a forward motion command cannot follow a reverse motion command (or vice versa). There is, of course, no such restriction if the commands are not issued until after CBUSY terminates.

State 7 (Rewind or Clear) is entered upon issuance of a Rewind or Clear command by the computer. The state is terminated when the tape unit finishes rewinding.

3.2.7 Status Register

The Status Register stores both the tape unit the the Controller status. This makes it possible for the computer to inspect the results of an operation to find out whether it was completed correctly or if some other action must be taken.

The status of the selected tape unit and the Controller are available for access by the computer at any time.

3.2.8 Parity Control

The Parity Control logic provides manual or program control over selection of odd or even parity for 7-track tape units. Odd parity is automatically selected for 9-track tape units. The output (odd parity) is used by the Parity Generator and Check logic.

3.2.9 Parity Error Detect

The Parity Error Detect logic searches for one or more parity errors in each tape record. Any detected errors cause the Parity Error Status bit to be set.

The Read Control logic uses the Read Clock Activity Sense logic (RCAS) output to enable the Parity Error Detect logic to inspect the Character Parity Check output only during the data portion of a record (since CRCC (9-track) and LRCC (7-track) can exhibit either odd or even parity).

The output of the LRC Check logic is inspected only after the entire record (including CRCC and LRCC) has been read.

3.2.10 Character Parity Check

The Character Parity Check logic checks each character read from tape for either odd or even parity.

3.2.11 LRC Check

The Longitudinal Redundancy Character Check logic checks for an even number of 1's for each individual track down the length of the record, including the CRC and LRC characters.

3.2.12 Read Data Storage Register

The Read Data Storage Register stores each tape character at the leading edge of the Read Strobe in such a manner that the Read Data is static to the computer adapter interface throughout the entire period until the leading edge of the next Read strobe occurs. This deletes the requirement for a storage register in the computer adapter section. This register would otherwise be required to retain the data for the maximum possible time after the Data Flag is set, to give the computer the maximum amount of time to accomplish the data transfer.

The outputs of the Read Data Storage Register are routed to the rest of the logic where Read data is utilized on the Controller.

3.2.13 Read Clock Activity Sense

The Read Clock Activity Sense logic separates the data portion of each record from the CRC and/or LRC characters in the forward direction. Thus, the Set Data Flag (in the Read Control logic) is allowed to operate only for the data portion of the record, which "strips" off the CRC and/or LRC characters.

The check word count (CKWDCNT) pulse occurs just after the last data character but before the CRC or LRC character's Read Strobe destroys the contents of the Read Data Storage Register. The CKWDCNT pulse is delivered to the Computer Adapter interface, where it may be used to create an extra data transfer request to the computer for the case where an odd number of characters were read from tape and the "Pack" mode of operation is being used. The CKWDCNT pulse is also typically used by the Computer Adapter to determine if the expected number of characters were read from tape to create status bits which can inform the computer that the record was too long, too short and/or contained an odd number of tape characters.

3.2.14 File Mark Detect

The File Mark Detect logic checks for 7-track or 9-track file marks, depending upon which type of tape is selected. The EOF status bit is developed if a file mark is detected in a forward or backword direction.

3.2.15 Read Control Logic

The Read Control logic controls data transfer during State 3 until the IRG is detected, at which time the Postdelay (State 4) or one of the Halt delays (State 5 or 6) is entered.

The Set Data Flag signal is generated for each Read Strobe that occurs as long as RCAS indicates that the data portion of the record is present and the Halt signal hasn't occurred.

When the IRG is detected or the computer generates the Halt signal (to indicate that it doesn't want any more data), there are no more Data Flag signals generated even though there may be more data in the record.

The Read Control logic also controls the forward and reverse space operations. These operations are identical to reading forward or reverse except that the Data Flag is not set for data transfer requests. All parity checks are valid for the spacing operations as well as for the reading operations and for read-after-write operations when a dual-stack head is employed on the selected tape unit.

In the special, Test Read, mode, the CRC and/or LRC characters are not separated from the data in the Forward Read operation. This mode is used to check the CRC and LRC generator logic with diagnostic programs.

3.2.16 Write Storage-Register

The Write Storage-Register is provided so that the Computer Adapter does not need a register to store computer output data. The Data Transfer logic operates on a request/response basis via the Data Flag and Write/Read Acknowledge (W/R ACK) signals. Each data character is requested a full write-clock-period before it is needed. The computer can respond any time within this period with a W/R ACK strobe pulse to load the Write Data into the Write Storage Register.

3.2.17 Parity Generator

The Parity Generator creates odd or even parity for each character presented from the Write Storage Register and sends the parity bit to the Write Data Select Gates. The Parity Control logic determines whether odd or even parity is generated.

3.2.18 Write Data Select Gates

The Write Data Select Gates consist of three sets of gates that are enabled by the Write Control logic to gate the Write data (and parity bit) or the File Mark code or the CRC Character onto the write data bus to the tape units.

3.2.19 File Mark Generator

The File Mark Generator generates the appropriate file mark. This may be a normal 9-track file mark, a special 9-track file mark or a 7-track file mark. The Write Control logic gates the file mark code onto the write data bus at the appropriate time and generates a Write Clock to write the file mark.

The special 9-track file mark is an option that writes the 7-track file mark code to provide compatibility with some computer manufacturer's hardware and software when writing in the "unpack" mode on a 9-track tape.

3.2.20 CRCC Generator

The Cyclic Redundancy Check Character (CRCC) Generator calculates the CRC Character while writing each record as each data character while writing each record as each data character appears on the write-data bus.

At the end of the record (9-track only) the Write Control logic gates the CRCC onto the bus and generates a Write clock pulse to write the CRC Character. The LRC Character is then written to finish the record. The CRCC may be all zeros and may exhibit odd or even parity.

3.2.21 Write Control Logic

The Write control logic operates during State 3 for write, erase and write-file-mark operations. The Write control logic controls the Data Transfer logic for write operations by developing the Set Data Flag pulse to request each character to be written until the Write operation is terminated by the Halt signal from the Computer Adapter.

Upon receiving the Halt signal, the CRC and/or LRC character is automatically appended to the record and part of the IRG is then erased. If a single-stack (read/write) tape unit is selected, the Write Control logic triggers the State Counter to the State 4 postdelay when it finishes writing the LRC Character at the end of the record. If a dual-stack (read after write) tape unit is selected, the Inter-Record Gap Detect logic is utilized to exit State 3 to State 4 postdelay in order to allow all of the record to be read-after-write parity checked.

The data rate is developed from the write clock frequency (from the Crystal Oscillators) and the tape-speed-select logic.

The Write Control logic also sends the Write Most Significant Byte (WRMSB) signal to the Computer Adapter. This enables the odd/even characters to be separated when "unpacking" a computer word into two sequential tape characters.

3.2.22 Crystal Oscillators and Tape Speed Select

The Crystal Oscillators provide stable precision clock frequencies for packing densities of 800/556/200 bits per inch. One set of crystals covers the standard tape speeds from 12.5 to 75 ips. The Tape Speed Select and Density Select logic divides down the clock rates to the appropriate frequencies and selects the write clock frequency as determined by tape speed and packing density.

The Speed Clock signal is used by the Delay Counter to provide all the precise time delays for the Formatter. The Speed Clock is dependent only on tape speed.

3.2.23 Density Select

The Density Select logic provides control over selection of Hi or Low density for 7-track tape units. Nine-track tape units are automatically operated at only 800 BPI. The Density Selection is controlled by the computer program via the Hi Density Select signal.

3.2.24 Data Transfer Control

The Data Transfer Control operates in conjunction with the Read or Write Control logic depending upon whether a Read or a Write operation is active.

The Read or Write Control logic generates the Set Data Flag pulse to signal that Read data is ready for input or to request a Write Data character. The Computer Adapter returns the W/R ACK signal, which clears the Data Flag and is used to strobe the Write data into the Write Storage Register for write operations. When the Computer Adapter desires to halt data transfer, it generates the HALT signal and the Data Flag signal is disabled.

3.2.25 Delay Counter

The Delay Counter is a flip-flop divider chain that counts the Speed Clock pulses to provide precise time intervals for Pre-, Post-, and Halt delays. The time interval begins when the counter starts counting (from a reset condition) and ends when the STOP signal is generated by the gates that decode various counts from the Delay Counter. The gate selected for a particular time interval depends upon which state the Controller is in as well as its configuration and the selected tape unit (provided by the STATUS signals to the Delay Counter).

3.2.26 Inter Record Gap Detector

The IRG Detector triggers the Formatter from State 3 to the Post Delay State 4, of Halt Delay State 5 or 6 when completing any Read or Space operation or any Write operation with a dual-stack, read-after-write tape unit. The IRG Detector resets the Delay Counter with each Read strobe. After the Read strobes stop, the Delay Counter is allowed to count for a prescribed interval until the STOP time is reached, at which time State 3 is terminated.

3.3 COMMANDS

3.3.1 Basic Commands

Basic Commands provided by the Formatter are:

1. Read (one record)
2. Write (one record)
3. Space
4. Write File Mark
5. Erase 3-inch gap
6. Rewind
7. Offline
8. Clear

3.3.1.1 Read and Space

The Space operations can be a single or multiple record under control of the STOP SPACE Computer Adapter signal. In addition, the backspace operation can be conducted in the EDIT mode. This is to position the Write head correctly in the IRG preceeding a record that is to be replaced with an equal length but updated record. BOT will halt backspacing automatically.

3.3.1.2 Write, Erase 3 Inch Gap and Write File Mark

The Erase-3-Inch-Gap command can be performed by itself or combined with the Write or Write File Mark commands to cause a 3-inch gap to be erased prior to writing the record or file mark. A Write command can be performed in the Edit mode (if the record to be replaced has first been backspaced over in the Edit mode to position the head correctly) to replace a record with an equal length record of updated information.

3.3.1.3 Rewind and Offline

The Rewind command causes the selected tape unit to rewind to Load Point (Beginning of Tape). The Controller goes "Busy" until the rewind is terminated (to provide a means of interrupting the computer upon termination of the operation).

The Offline command never sets the Formatter to the "Busy" state and may be sent to a selected tape unit even if the tape unit is "Not Ready" because it is performing a rewind operation.

3.3.2 Command and Mode Combinations

The list of possible commands executable by the Formatter depends upon the "mode" lines and are listed in Table 3-1.

NOTE 1 The GEN ODD PARITY and HIGH DENSITY mode lines are ignored for 9-track tape units. The GEN ODD PARITY line controls whether odd or even parity is written or checked for. The HI DENSITY line controls the written character packing density and the period of time allowed between read strobes in the Read Clock Activity Sensor Circuits.

TABLE 3-1. COMMAND & MODE COMBINATIONS

FORMATTER	"SET XXX" COMMAND SIGNALS									"MODE" SIGNALS					
	REV	WCC	WFM	GAP	FSR	RCC	CLR	REW	OFL	GEN ODD PARITY	HI DENSITY	EDIT	TRD	STOP SPACE	CD
1. Test Read Forward						X				1	1		X		5
2. Read Forward						X				1	1				5
3. Write 1 Record (normal)		X								1	1				
4. Write 1 Record (edit)		X								1	1	X			
5. Space Forward 1 Record					X					1	1				5
6. Space Forward "n" Records					X					1	1			4	5
7. Space Reverse 1 Record	X									1	1				5
8. Space Reverse "n" Records	X									1	1			4	5
9. Space Reverse (edit mode)	X									1	1	X			5
10. Write File Mark			X							1	1	6			5
11. Erase 3 Inch Gap				X											
12. Erase 3" then Write File Mark			X	X											
13. Erase 3" then Write 1 Record		X		X						1	1				
14. Rewind								X							
15. Off-line									X						
16. Initiate Rewind then Offline								X	X						

SEE NEXT PAGE FOR NOTES 1-4

NOTE 2 The STOP SPACE signal is used only for continuous spacing over multiple records. The DBY signal can be used by the Computer Adapter to count records to determine when the required number of records has been traversed.

NOTE 3 The CD signal (Core Dump) is ignored in 7-track but can be used to write 7-track-type file marks and to check for 7-track file marks on a 9-track tape unit, i.e., an octal 17 with even parity is written (and decoded as a file mark when reading) instead of the normal octal 23 with odd parity.

This provides compatibility with some existing computer manufacturer's software.

NOTE 4 The Edit mode can be used to rewrite a file mark if the file mark is first backspaced over in the Edit mode.

3.4 STATE FLOW

Figure 3-2 illustrates the State Counts that the Controller sequences through in simplified form. Figure 3-3 illustrates the State Flow in detail.

3.4.1 Simplified State Flow (See Figure 3-2)

The Controller is in the "Rest" State 0 at initial conditions. The strobe C command clock is rejected if the command is not a "valid" one. If CBUSY is not set by a valid command then the command must be:

1. Offline
2. Rewind (with no interrupt)

In this event, the command is executed but the Formatter remains in State 0.

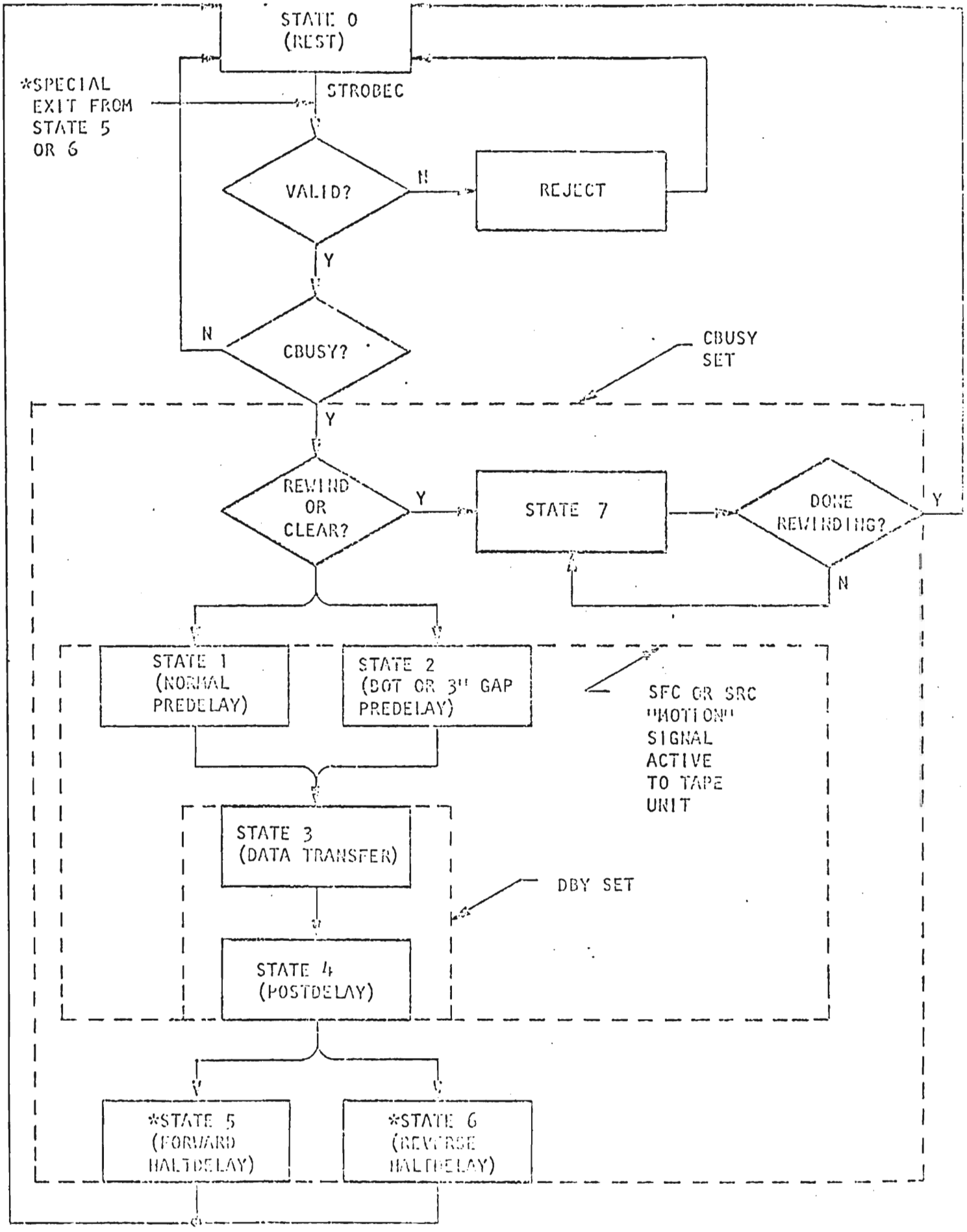


Figure 3-2. Simplified State Flow

If CBUSY is set, than a rewind command causes the Formatter to enter State 7 until the rewinding status signal is false, at which time CBUSY is cleared and State 0 is re-entered.

Any other command causes one of the two Predelay States to be entered. State 1 is normally used, but State 2 is used when the Formatter is at BOT or a 3-inch Gap Command is executed. The appropriate motion signal (SFC for forward motion, SRC for reverse motion) is activated at this time.

The predelays are used to erase a 3-inch gap or part of the IRG when writing and to allow sufficient time for the tape unit to get "up to speed".

The State 3 data transfer then takes place. For writing, the data is written until the HALT signal from the Computer Adapter terminates the record. For "Erase" no data transfer is needed, so State 3 is terminated immediately and State 4 is entered. For "Write File Mark" no data transfer actually occurs, but the Formatter writes the file mark and the LRC character and then enters State 4.

For dual gap (read-after-write) tape units, the transition from State 3 to State 4 is delayed until the read head detects the end of the record (the beginning of the IRG) to allow the full record to be checked for no parity errors. State 4 Postdelay (in conjunction with the .2-inch distance the tape moves <u>after</u> the motion command terminates) is used to erase the first part of the IRG.

For Reading or Spacing operation, State 3 is maintained until the end of the record and the IRG is reached. For reading, the Computer Adapter HALT signal terminates actual data exchange. For reading or spacing, the State 4 Postdelay (in conjunction with the fixed .2-inch distance, the tape moves when halting after the motion command terminates) is used to position the head in the correct position in the IRG to allow for a subsequent write or read operation.

Note that the 53 + 54 (DBY) signal is active only during States 3 and 4, while the "motion" signals to the tape unit are active from the beginning of the Predelay State through the Postdelay State.

After the Postdelay occurs, one of the forward/reverse HALT delays (State 5 or 6) is entered (to insure that the tape is allowed sufficient time to come to a halt in the IRG).

At the termination of the Halt Delay, signal CBUSY is cleared (to signal the computer that the next command can now be executed) and the Rest State 0 is entered.

The "Special Exit" from States 5 or 6 allows continuous writing or reading without stopping in the inter-record gap to optimize data transfer efficiency.

Since the Start/Stop characteristics of the tape units are "ramp" like, the gap traverse time is twice as long (as it would be at full speed) when the next command is delayed until the tape has completely halted.

This "special exit" allows a Write or a Read command to terminate the Halt Delay state and initiate the Predelay state without being "rejected", even though the CBUSY signal is active.

In any other State, with CBUSY active, a command (other than Clear) is rejected.

The computer can accomplish "on-the-fly" writing or reading by initiating the next command when DBY terminates at the end of State 4, rather than waiting until CBUSY terminates.

However, there are certain restrictions on this type of operation:

1. The next command must not switch from a Write or Write-File Mark to a Space or Read (or vice versa).
2. The next command must not switch direction or motion.
3. The next command must not be a Rewind or Offline if the previous one was a Write, or Write File Mark type.

It is the computer program's responsibility to make sure these restrictions are followed.

The Delay Counter is used in States 1, 2, 4, 5 and 6 to generate the prescribed delay times.

3.4.2 Detailed State Flow (See Figure 3-3)

The Detailed State Flow chart shows the control over signals DBY, CBUSY and the motion commands SFC, SRC as well as the use of the Delay Counter. Otherwise the flow chart is like Figure 3-2.

In addition, the IRG detection exit from State 3 is detailed, as is the detour around State 4 Postdelay (to achieve minimum Postdelay) in certain cases.

3.5 COMMAND EXECUTION TIMING

The main commands are discussed step-by-step and a timing diagram is included for each command.

The main commands are:

1. Rewind (with interrupt)
2. Write file mark (7 track)
3. Write file mark (9 track)

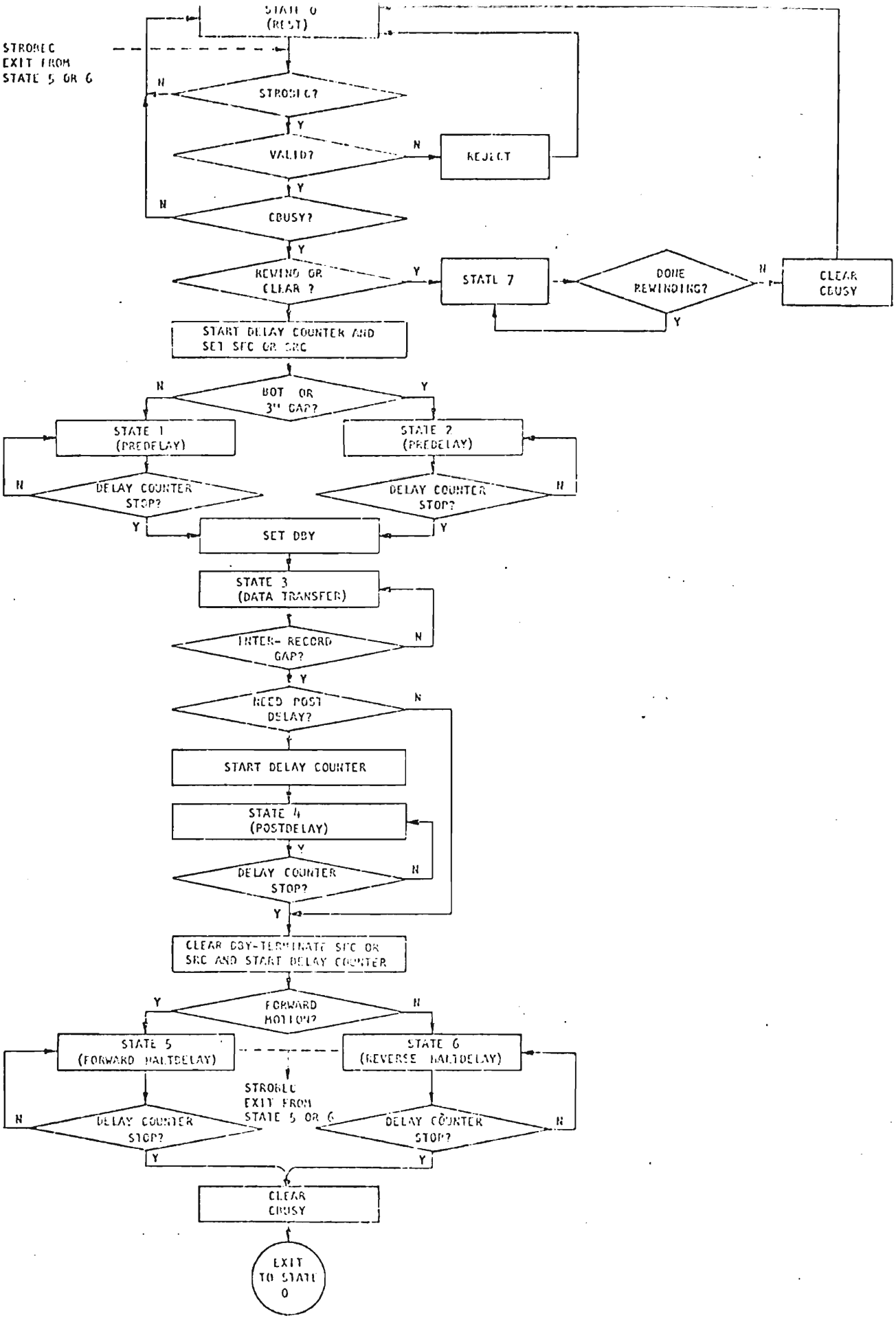


Figure 3-3. Detailed State Flow

4. Forward Space 1 record
5. Backspace 1 record
6. Write 1 record (7 track)
7. Write 1 record (9 track)
8. Read 1 record (7 track)
9. Read 1 record (9 track)
10. Erase 3-inch gap

3.5.1 Rewind (With Interrupt)

The offline command doesn't set CBUSY. In this event, the commands are passed on to the selected tape unit as a pulse.

When the computer adapter generates the 6-STROBEC pulse while 6-SETREW is high and the Controller isn't busy, the command is accepted and the 2-VLD pulse is generated.

The 3-REW flip-flop is set to store the rewind command. When the 6-STROBEC clock pulse terminates, the Rewind command is generated to the selected tape unit (signal 3-$\overline{\text{RWC}}$). When the tape unit responds that it is rewinding (signal 7-REWINDING) the 3-REW flip-flop is reset and the Controller 6-$\overline{\text{RWDG}}$ status bit is set. The tape unit goes "not ready" (7-$\overline{\text{RDY}}$) during rewind. Since the tape unit rewind terminates before the tape unit returns to load point and becomes "Ready" again, the 6-$\overline{\text{RWDG}}$ status bit is interlocked to wait until the tape unit goes ready (7-$\overline{\text{RDY}}$).

The 3-SRS (system visit) pulse clears the status register.

At this time 6-CBUSY* resets to signal that the operation is complete.

3.5.2 Write File Mark (7-Track) (See Figure 3-4)

When signal 6-SET WFM is high during the 6-STROBEC clock pulse, the 3-WFM command-register flip-flop is set to initiate a Write-File-Mark command. The 2-SRS pulse is also generated to reset the Controller to initial conditions. The 3-CBUSY flip-flop is set by the 2-VLD clock, and the 7-$\overline{\text{SFC}}$ command is activated to start the tape moving in the forward direction. The selected tape unit write amplifiers are enabled as the 7-$\overline{\text{WARS}}$* signal is high. Command register flip-flop 3-WFM also sets the selected tape transport unit to the write mode via signal 7-$\overline{\text{SWS}}$. The Predelay signal delays writing of the file mark character until the tape transport unit is up-to-speed and has generated a portion of the required inter-record gap.

If the tape transport unit is at the beginning of tape when the Write-File-Mark instruction is generated, the Predelay is longer to cause a 3-inch gap to be erased before the file mark is written. The Enable Write Data Request flip-flop (9-EWDR) is set upon the termination of the Predelay signal. The Write Data Clock flip-flop (9-WDCL) is set one write-clock-period later and is gated to set the enable blank character counter (9-EBCC) flip-flop. The 9-EWDR flip-flop is immediately reset, which causes flip-flop 9-WDCL to be reset one write-clock-period later. Thus, only one Write Data strobe is generated to the selected tape transport unit. The command register flip-flop 3-WFM gates the file mark code onto the write data bus.

The blank character counter (comprised of flip-flops 9-CC1, 9-CC2, and 9-CC4) begins counting from the occurrence of the Write-File-Mark clock. This causes the 9-WARS flip-flop to be set, resetting the tape unit write amplifier flip-flops, causing the LRC character to be written. The tape transport unit continues running in the forward direction until the file mark passes under the read head, thus the file mark and LRCC character can be checked for vertical parity and longitudinal parity.

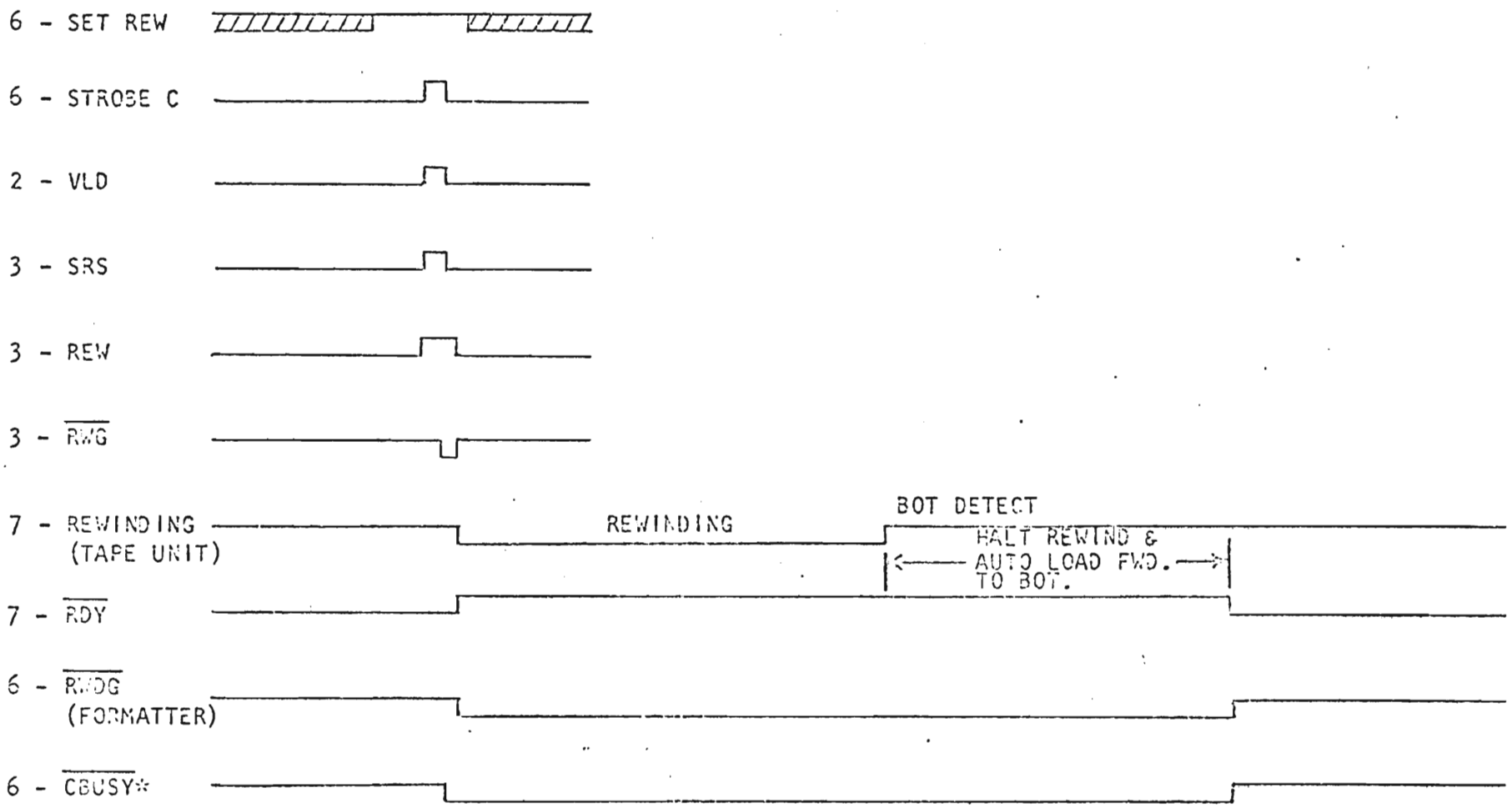


Figure 3-4. Rewind Timing Diagram

The time interval in milliseconds, between writing the file mark and reading back the file mark character, is equal to 150 divided by the tape speed in inches-per-second. As the timing diagram illustrates, the Read Data strobe (7-$\overline{\text{RDS}}$) will occur, and eight character times later (for 9-track), the LRC character read strobe will occur. The LRC character occurs four character times later for 7-track. The read clock activity sensor (12-RCAS) is set upon detection of the first 7-$\overline{\text{RDS}}$ pulse and times out two or three clock periods later. While the 12-RCAS circuit is active, the character parity is checked.

The Delay Counter is reset by each Read strobe and then times out a delay interval after the last Read strobe. Thus, the Delay Counter performs the taks of IRG detection. Upon termination of the Delay Counter time out, the 5-STOP pulse is generated and used to check for an LRCC error in the previous record. The 5-STOP pulse is also used to trigger the State 4 Post Delay circuits (14-S4). When the Post Delay terminates, the 7-$\overline{\text{SFC}}$ signal is terminated, and the State 5 Halt Delay is entered. The Halt Delay insures that the tape transport unit is guaranteed to have ceased all motion in the inter-record gap. If the next command is to be a write-type command, then the IRG can be erased "on the fly" at full tape speed (without stopping in the IRG). This is done by issuing the command after the signal 6-$\overline{\text{DBY}}$ terminates rather than waiting until 6-$\overline{\text{CBUSY}}$ terminates. Status is valid after the 6-DBY signal terminates, hence the status can be checked before issuance of the next command.

3.5.3 Write File Mark (9-Track) (See Figure 3-5)

Writing a File Mark in 9-track mode is similar to the 7-track mode except that eight character times separate the file mark and the LRC character. Note that there is effectively an "all zeros" CRC character, since for data records the CRCC occurs at the 4th character time then 4 character times later the LRCC is written.

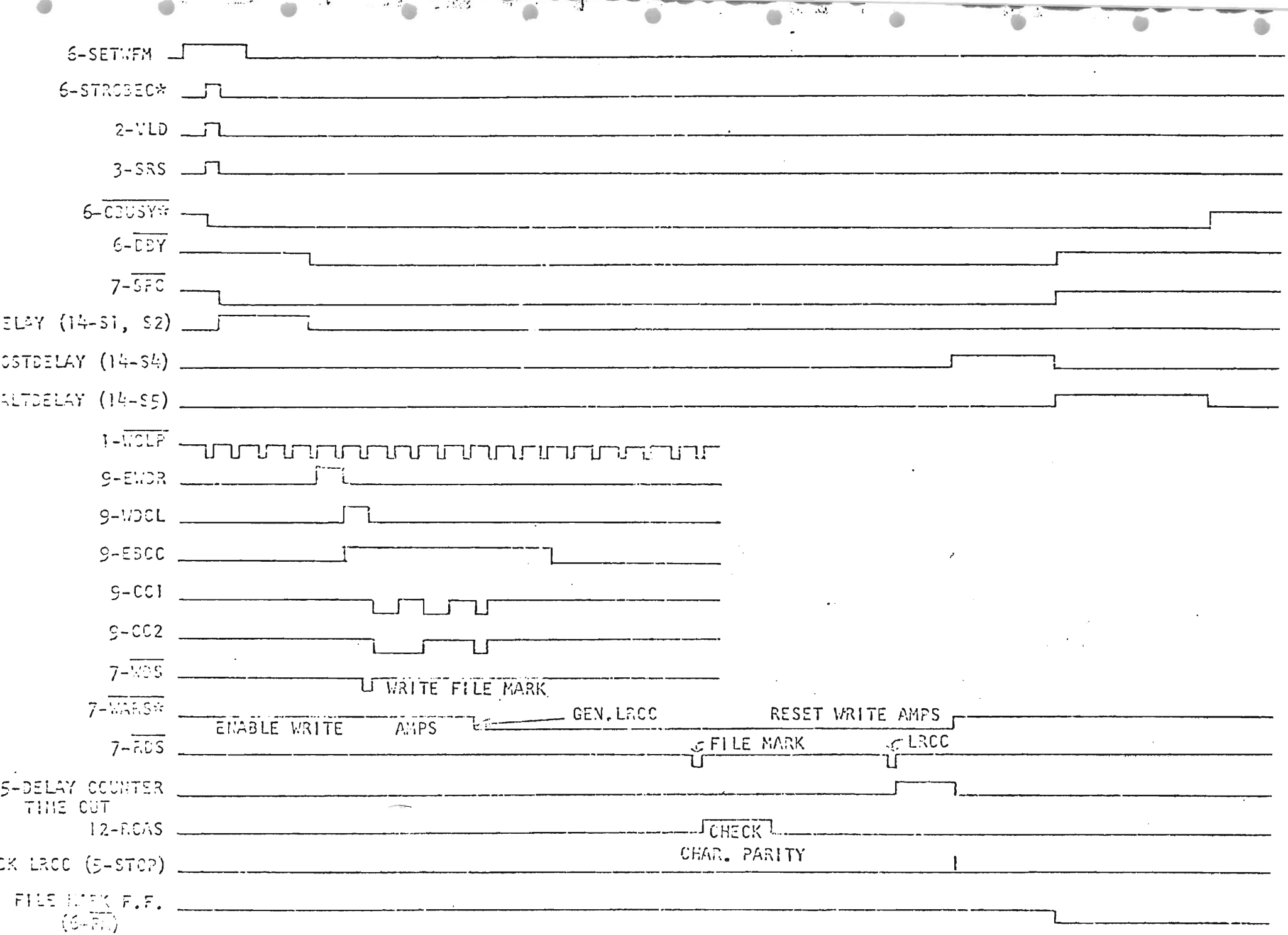


Figure 3-5. Write File Mark Timing Diagram (7-Track Mode)

3.5.4 Forward Space/Record (See Figure 3-6)

When term 6-SET FSR is high with the 6-STROBEC, the 7-$\overline{\text{SFC}}$ signal is activated to move tape forward. The 2-VLD and 3-SRS pulses are generated to reset the Controller and initiate the space-forward operation.

NOTE The Space Forward Command results in spacing over ONE record if signal 6-STOP SPACE is "open circuit" or at the High level. If multiple records are to be spaced over, 6-STOP SPACE is held low until the leading edge of signal 6-$\overline{\text{DBY}}$ occurs for the last record. The 6-$\overline{\text{FM}}$ status signal and 6-$\overline{\text{EOTS}}$ status signal may also be utilized to switch STOP SPACE "high" so that a file mark or the end of tape will halt the multiple record spacing operation.

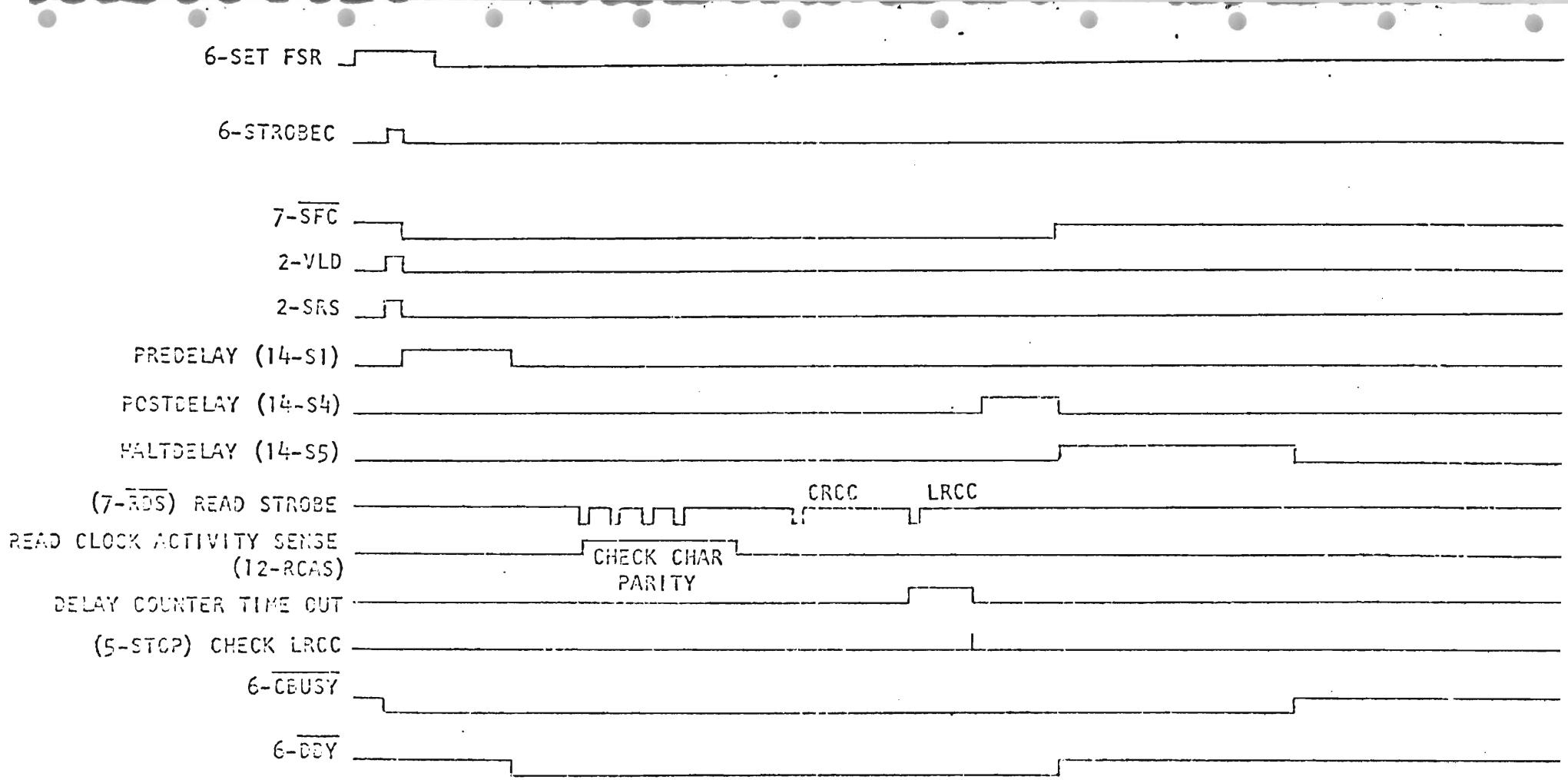
Note that 6-$\overline{\text{CBUSY}}$ remains low (for multiple spacing operations) until the final record has been passed.

The Predelay allows the tape unit to get up to speed before allowing Read strobes to be accepted. The Read strobes activate the Read Clock Activity Sensor (12-RCAS) to enable parity checks to be made while spacing. When the record is past, the Delay Counter times out to detect the IRG and the LRCC check is made. After the Signal 6-$\overline{\text{DBY}}$ terminates, status can be checked and the next command can be issued (if a Read or Space Forward) to accomplish non-stop operation.

If no new command is issued at this time, the normal Halt Delay sequence is entered.

3.5.5 Backspace/Record

Backspace is similar to Forward space except the LRC/CRC characters occur first.



1. CRCC MAY BE MISSING FOR 9 TRACK AND IS ABSENT ON 7 TRACK.

Figure 3-6. Forward Space One Record Timing Diagram

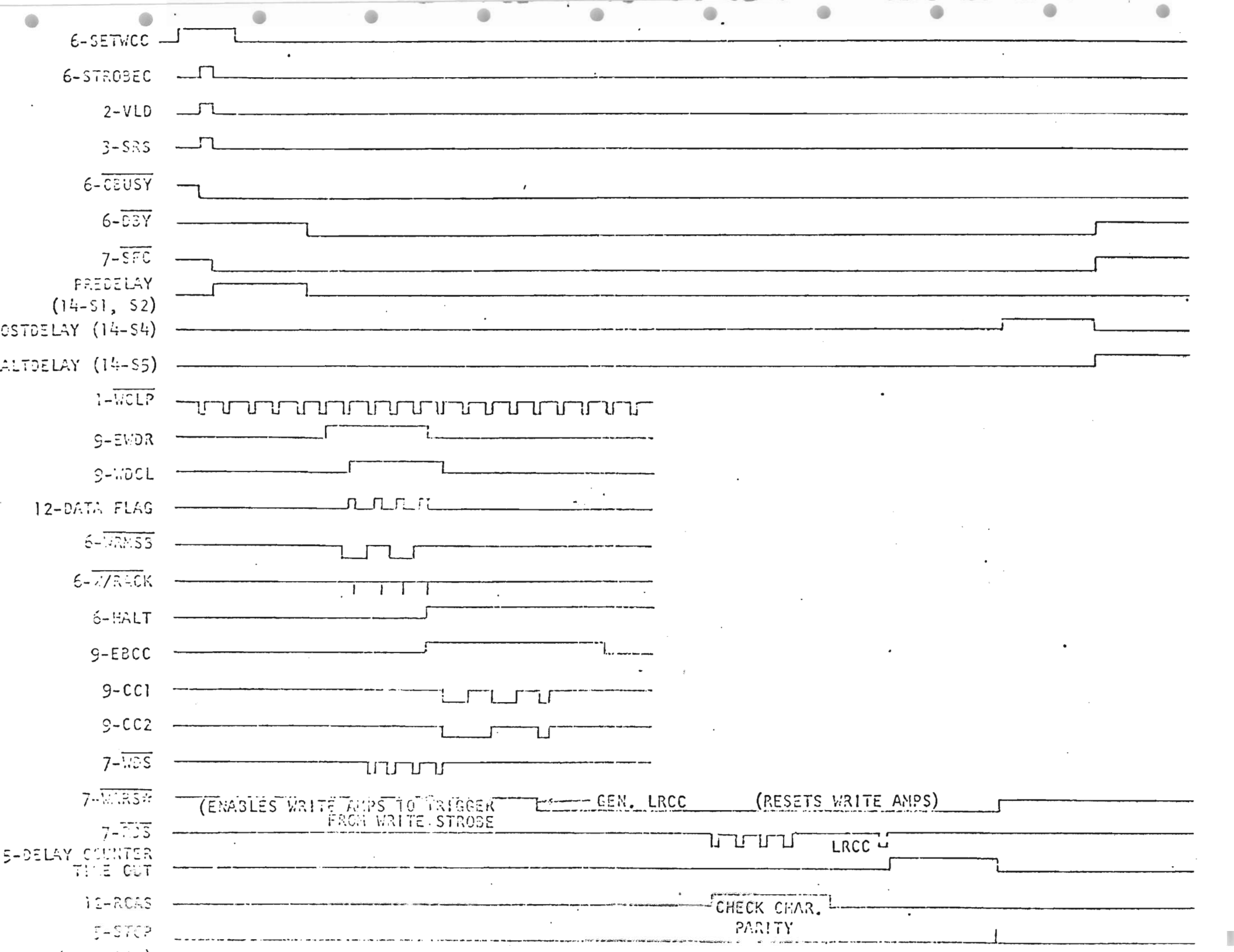
3.5.6 Write-One-Record (7-Track) (See Figure 3-7)

The write-one-record instruction causes the tape transport unit to turn on the write current, enable the write amplifiers, get up to speed, generate a portion of the inter-record gap, then request output data transfers from the computer adapter logic. The requested data characters are written on tape until a HALT signal terminates the record by writing the CRC character (9-track only) followed by the LRC character.

The tape transport unit read-after-write head enables parity checks to be performed upon the record that has just been written. After the parity checks are completed, the tape transport unit erases a portion of the next inter-record gap and is then commanded to halt. After sufficient time has elapsed to ensure that the tape has completely stopped moving, the completion of the write-one-record operation is signaled when 6-$\overline{\text{CBUSY}}$ terminates.

"On-the-fly" generation of the IRG without signal stopping may be accomplished by checking status, at the termination of signal (53 + 54) and issuing the next Write, Erase or Write File Mark command immediately. The Write mode is set by the command clock (2-VLD) to initiate the Write-One-Record instruction. The System Reset Pulse (3-SRS) is also generated by the Valid Command clock to reset the tape transport controller to initial conditions. The Controller Busy flip-flop (6-$\overline{\text{CBUSY}}$) is set by the command clock to initiate the Write-One-Record instruction. The Synchronous Forward signal (7-$\overline{\text{SFC}}$) is sent to the tape unit to initiate forward motion.

After the Predelay (14-S1, S2) times out, the enable write data request flip-flop (9-EWDR) is clocked set to begin the writing of the record. The Predelay erases the last portion of the inter-record gap as the write current is on for this period. The Write Data Clock flip-flop (9-WDCL) is clocked set one clock time after the 9-EDWR flip-flop to enable write strobes to be generated to the tape unit.


6-SETWCC
6-STROBEC
2-VLD
3-SRS
6-CBUSY
6-CBY
7-SFC
PREDELAY
(14-S1, S2)
OSTDELAY (14-S4)
ALTDELAY (14-S5)
1-WCLP
9-EWDR
9-WDCL
12-DATA FLAG
6-WRMSS
6-W/RACK
6-HALT
9-EBCC
9-CC1
9-CC2
7-WDS
7-WCRS*
(ENABLES WRITE AMPS TO TRIGGER FROM WRITE STROBE
GEN. LRCC
(RESETS WRITE AMPS)
7-RDS
LRCC
5-DELAY COUNTER TIME OUT
12-RCAS
CHECK CHAR. PARITY
5-STOP

The first Data Flag signal is sent to the computer adapter. When the Computer Adapter logic has the first character ready to transfer, it generates the 6-W/RACK pulse, which stores the first output character in the Formatter Write Data Register and clears the Data Flag. The first write data strobe (7-$\overline{\text{WDS}}$) is then generated by the next write clock pulse (1-$\overline{\text{WCLP}}$) in order to clock the character stored in the write data storage register onto the magnetic tape. At the trailing edge of the write data strobe, the Data Flag is set to request the next character from the Computer Adapter logic.

The Write Data Strobe (7-$\overline{\text{WDS}}$) is OR'ed with an extra CRC clock generation signal to clock the CRC generator register (logic diagram 15), to begin calculation of the CRC character. The CRC generator register is initially reset. The CRC generator register than monitors the write data output bus to generate a check character that is unique for the data characters written on tape.

If the output data character is not transferred to the tape controller before the next write data strobe is to occur, a "timing error" status bit will be set. The sequence of Data Flag-W/R ACK-Write Strobe continues until the HALT signal is generated by the Computer Adapter to terminate the writing. The HALT signal sets the enable-blank-character-counter (9-EBCC) flip-flop. Flip-flop 9-EBCC enables the Blank Character Counter (CC1, 2, 4), disables the Write Control flip-flops, and resets the Write Most Significant Byte (WRMSB) flip-flop.

The Blank Character Counter controls the generation of the CRC and LRC characters to generate the end of the record.

The character counter is decoded in the 9-track mode to create an extra CRC clock and to gate the contents of the CRC generator onto the write data bus. The character counter is also decoded in order to set the 9-WARS flip-flop to reset the write amplifiers via signals 7-$\overline{\text{WARS}}$ (in order to generate the LRC character).

The tape transport unit continues motion in the forward direction so that the read-after-write head can check parity of the entire record. The Read clocks (7-$\overline{\text{RDS}}$) trigger the Read Clock Activity Sensor circuit (12-RCAS), which defines the characters that are to be checked for vertical parity. Two or three clock-periods after the last character in the record, the 12-RCAS signal terminates and vertical parity checking is disabled. The Delay Counter times out after the LRC character is detected at the end of the record to provide detection of the IRG. The 5-STOP pulse is then used to check for an LRC error. The Post Delay time-out interval ensures that a sufficient portion of inter-record gap is erased in the forward direction after a record is written. This permits the tape transport unit to start in the reverse direction and get up to speed for a backspace read. At the end of the Post Delay, the synchronous forward command terminates, and the Halt Delay begins timing out to ensure that the tape has come to a complete halt before the 6-$\overline{\text{CBUSY}}$ signal terminates.

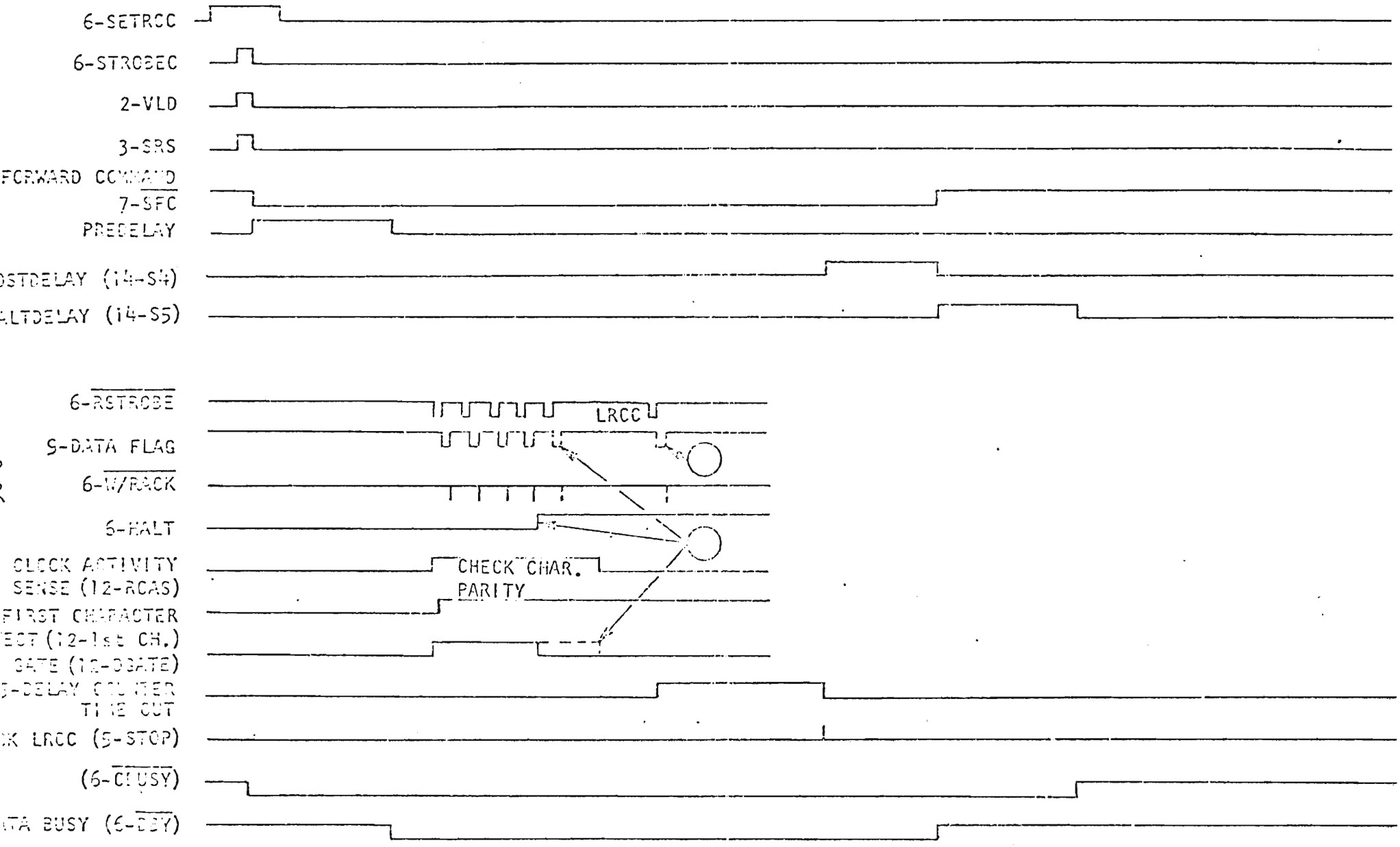
For continuous writing (no stopping in the IRG) the status can be inspected after S3 + S4 signal terminates and a Write, Erase or Write File Mark command can be issued immediately.

3.5.7 Write/Record (9-Track)

Writing in 9-track mode is similar to 7-track except that there is a Cyclic Redundancy Check Character (CRCC) written four character-times after the end of the record, followed by the Longitudinal Redundancy Check Character (LRCC) four more character-times later.

3.5.8 Read One Record (7-Track) (See Figure 3-8)

The Read One Record command is initiated when signal 6-SET RCC is high and the 6-STROBEC pulse occurs. The valid command pulse (2-VLD) clocks the 3-RCC flip-flop set in the command register. The System Reset pulse (3-SRS) is generated by the 2-VLD clock to reset the Controller to initial



2. IF "TEST READ MODE", THE DATA FLAG ALSO OPERATES FOR THE LRC CHARACTER TO INPUT IT TO THE COMPUTER.

1. IF "HALT" DOESN'T OCCUR BEFORE END OF RECORD, THE DATA GATE WILL REMAIN SET AND THE DATA FLAG WILL CONTINUE OPERATION.

NOTES

Figure 3-8. Read One Record Timing Diagram (7-Track Mode)

conditions. The Synchronous Forward command (7-$\overline{\text{SFC}}$) and the 6-$\overline{\text{CBUSY}}$ signal are activated at the same time. After a Predelay interval (to allow the tape to get up to speed) Read strobes are enabled to the read logic. The first Read strobe that occurs sets the data gate flip-flop (12-DGATE) and triggers the Read Clock Activity Sensor (12-RCAS). The trailing edge of the first Read strobe sets the first Character Detect flip-flop (12-1st CH), which, in turn, disables any further read strobes from setting the 12-DGATE flip-flop. When the end of the record is reachec, the 12-RCAS circuit times out two or three character times later, resetting the 12-DGATE flip-flop if the computer hasn't terminated data transfer (via the HALT signal) already.

In the interval during which the 12-DGATE flip-flop is set, the data transfer takes place. During the time that 12-RCAS is set, the characters are checked for parity. The CRC/LRC characters are not checked for parity. If the HALT signal occurs before the end of the record, the 12-DGATE flip-flop is reset to terminate Data Flag requests. (The dashed-line signals annotated with Note 1 illustrate that if the HALT signal is missing, the fifth tape-character shown on the timing diagram is input to the computer and the 12-DGATE flip-flop dies not reset until the 12-RCAS circuit times out at the end of the record. The dashed waveforms annotated by Note 3 indicate that the Data Flag operates for the CRC and LRC characters when the record is read in the Test Read mode.) The Test Read mode is provided so that the CRC/LRC characters can be read into the computer for diagnostic purposes. Regardless of whether the Read One Record instruction is terminated by a HALT or not, the tape continues motion until the inter-record gap is reached, at which time Delay Counter begins timing out. When the IRG is indicated by the Delay Counter time out, the LRC check logis is strobed by the 5-STOP pulse and causes the parity error status flip-flop to set if an LRC error exists. The Post Delay interval is then entered (14-S4) at the end of which the 7-$\overline{\text{SFC}}$ Synchronous Forward Command is terminated to the tape unit. The halt delay (14-S5) then begins timing out to delay reset of the 6-$\overline{\text{CBUSY}}$ signal until the tape transport unit is guaranteed to have halted all motion. If continuous read (no stopping in the IRG) is desired, then the termination of signal 6-$\overline{\text{DBY}}$ can be used to signal that status is ready to be checked. Thus, if the next command is a Read or Space (in the same direction) it can be issued immediately.

The data transfer signals sequence is:

1. Pulse 6-$\overline{\text{RSTROBE}}$ indicates read data is being stored in the Controller Read Data Register. The Read data will be settled by the end of the pulse. At the trailing edge of the pulse, the Data Flag is set.

2. When the 6-$\overline{\text{DATA FLAG}}$ signal goes low, a data transfer is requested.

3. After the computer has accepted the data, pulse 6-$\overline{\text{W/RACK}}$ must be issued to clear the Data Flag.

4. The 6-HALT signal (or the detection of the IRGO resets 12-DATA GATE to terminate transfer requests. 6-HALT should be presented with the last 6-$\overline{\text{W/RACK}}$ pulse (or shortly thereafter).

The 6-$\overline{\text{DATA FLAG}}$ signal reset has a "built in" delay from the 6-$\overline{\text{W/RACK}}$ pulse such that the 6-$\overline{\text{DATA FLAG}}$ signal can be gated to form the 6-$\overline{\text{W/RACK}}$ pulse, when designing a computer adapter that "Packs" 2 tape characters into one computer word. Normally a pulse from the computer is used to generate the 6-$\overline{\text{W/RACK}}$ signal.

The <u>leading</u> edge of the 6-RSTROBE pulse may be used to toggle a binary flip-flop on the computer adapter to determine whether the tape character is an "odd" or "even" one for "Packing" purposes. By using the leading edge, the toggle flip-flop can be gated with 6-$\overline{\text{DATA FLAG}}$ to form the 6-$\overline{\text{W/RACK}}$ pulse on the odd characters while storing the odd characters in a computer-adapter register.

The toggle flip-flop can then be checked at pulse 6-$\overline{\text{CKWDCNT}}$ time to detect an odd number of characters in the record. This "forces" a data transfer to the computer for the extra "odd" character, since "Packing" logic normally expects an even number of characters. Thus, a data transfer to the computer normally occurs after every <u>even</u> character).

3.5.9 Read-One-Record (9-Track)

Similar to Reading 7-track except there can be a CRC character as well as an LRC character. The CRC character can be "all zeros", but there is always an LRC character.

3.5.10 Erase 3-Inch Gap

The Erase-3-Inch-Gap timing is similar to the Write-File-Mark timing except 14-S2 generates the Predelay and no writing occurs.

3.6 CONTINUOUS WRITE OR READ

Continuous Write allows the IRG to be generated at full rated tape speed. If successive Write commands are based upon the termination of the CBUSY command (as is normal), the tape comes to a full stop in the IRG.

Similarly, Continuous Read (or Space) allows the IRG to be traversed at full rated tape speed.

This mode of operation optimizes the usage of the tape units by minimizing the amount of "dead time" in which data transfer cannot take place in the IRG. In order to obtain continuous "on-the-fly" operation, the S3 + S4 signal may be used (instead of the CBUSY signal) as long as certain restrictions are met:

1. The next command may not switch from a Read to a Write mode (or vice versa).
2. The next command may not switch tape direction.
3. A Rewind or Offline command may not follow a Write or Write-File-Mark command.

A Write or Write-File-Mark command can follow another Write or Write-File-Mark command as soon as signal DBY terminates, rather than waiting until signal CBUSY terminates.

Similarly, a Read or Space Forwards command can follow the same type command upon termination of DBY.

A Read or Space Reverse command can follow the same type command upon termination of DBY.

3.7 OPTIONS

The following field-changeable options are provided for in the Controller:

1. Selection of tape speed.
2. Selection of 7-track dual-density pair.
3. Definition of tape units as single stack (read/write) or as dual-stack (read-after-write).
4. BCD 10 to zero conversion (when reading 7-track tapes in even-parity mode).
5. No Parity Error with file mark.

3.7.1 Tape Speed

The tape-speed-selection option provides control over the "Speed Clock" and the "Write Clock" divider chains that operate from the crystal oscillators. The selection is accomplished by controlling the division modulo of a flip-flop divider chain by loading the negative 2's complement of the desired divisor (-1_, whereupon the counter counts up to zero to recycle.

Chip position J1 on card assembly number 76227-2 (Logic (1)) is provided for this purpose. To select speed, locate desired speed in Column 1. Directly opposite the speed in Column 4 is the wiring configuration of the speed chip to establish the desired clock frequencies. The field numbers

TABLE 3-2 TAPE SPEED SELECTION

Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7		Col 8		Col 9	
Tape Speed	Division Ratio	NEG. 2's Complement	16 8 4 2 1 ← BINARY 1 2 3 4 5 ← FIELD	SPD CLK PERIOD 200 BPI	SPD CLK FREQ KHz (PIN D5-11)	WRITE CLOCK FREQ, KHz (PIN)					
						800 BPI		556 BPI		200 BPI	
						Freq	Per	Freq	Per	Freq	Per
112.5	2	-1	1 1 1 1 1	44.44μ	22.5	90	11.1	62.55	16	22.5	44.44μ
75	3	-2	1 1 1 1 0	66.6μ	15	60	16.6	41.7	24	15	66.6μ
56.25	4	-3	1 1 1 0 1	≈88.			22		31.5		
45	5	-4	1 1 1 0 0	111.1μ	9	36	27.7	25.02	40	9	111.1μ
37.5	6	-5	1 1 0 1 1	133.3μ	7.5	30	33.3	20.85	47.9	7.5	133.3μ
32.14	7	-6	1 1 0 1 0								
28.125	8	-7	1 1 0 0 1								
25	9	-8	1 1 0 0 0	200μ	5	20	50	13.9	72	5	200μ
22.5	10	-9	1 0 1 1 1	≈218			54.5		90		
20.45	11	-10	1 0 1 1 0								
18.75	12	-11	1 0 1 0 1								
17.3	13	-12	1 0 1 0 0								
16.07	14	-13	1 0 0 1 1								
15.0	15	-14	1 0 0 1 0								
14.06	16	-15	1 0 0 0 1								
13.23	17	-16	1 0 0 0 0								
12.5	18	-17	0 1 1 1 1	400μ	2.5	10	100	6.95	144	2.5	400μ
11.84	19	-18	0 1 1 1 0								
11.25	20	-19	0 1 1 0 1								
10.7	21	-20	0 1 1 0 0								
10.22	22	-21	0 1 0 1 1								
9.7	23	-22	0 1 0 1 0								
9.38	24	-23	0 1 0 0 1								
9.0	25	-24	0 1 0 0 0								
8.6	26	-25	0 0 1 1 1								
8.3	27	-26	0 0 1 1 0								
8.03	28	-27	0 0 1 0 1								
7.77	29	-28	0 0 1 0 0								
7.5	30	-29	0 0 0 1 1								
7.2	31	-30	0 0 0 1 0								

NOTES:

1. In Col 4, pins marked "0" must be jumpered to K1-13 or 14, pins marked "1" must be jumpered to K1-15 or 16.

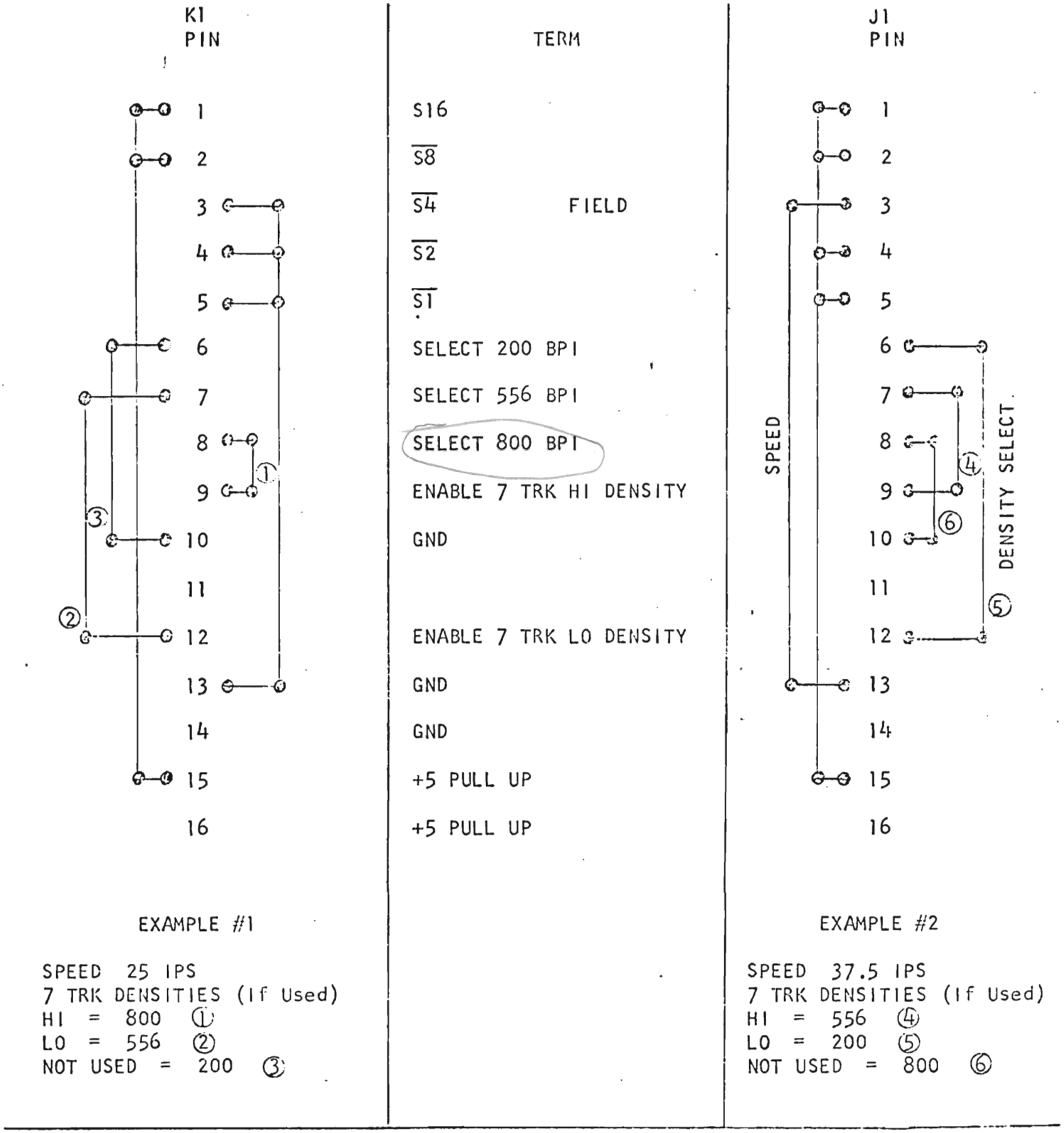


Figure 3-9. Example Tape Speed Selection

Figure 3-9 illustrates two examples of jumper wiring of socket J1 to achieve the desired tape speeds and densities.

1-5 at the top of the columns indicate the pins on K1. All field columns having a "1" are jumpered to J1-15 or 16. All field columns having "0" are jumpered to J1-13 or 14.

NOTE: All SELECT's (J1-6, 7 & 8) must be tied to an ENABLE TERM (J1-9 or 12) or GROUNDED.

3.7.2 Dual Densities

The Controller is configured to operate at 800 BPI when a 9-track tape unit is selected. Different pairs of densities can be selected for the tape units, i.e., tape unit A can be 800/556, 556/200 or 800/200, etc., if 7-track tape units are selected.

The three densities (800, 556 & 200) are selected by jumpers on a plug-in header plugged into J1 of 76227 assembly. (Same header used for speed selection). There are three density-select pins (6, 7, 8) and two density-enable terms. A__ select terms must be wired to the appropriate enable or must be grounded. There will always be at least one density-select grounded. The higher of the remaining selects is wired to "enable high density" (J1-9). The other is wired to "enable low density" (J1-12). If no seven-track machines are used, all three selects should be grounded. (See Figure 3-8 for examples of 800.556 and 556/200 wiring).

3.7.3 Single/Dual-Stack Head Selection

The Controller is configured so that if no jumpers are used in the SS/DS Head Selection Field E3 to E4, (Assembly 76233, Logic Drawing 2) then Dual-Stack (read-after-write) is assumed.

3.7.4 BCD 10 to Zero Converter

The Controller is configured to convert BCD 10 (Octal 12) to zero when reading 7-track tapes in the even parity mode if no jumper is inserted between E3 and E4 on board assembly number 76232 (Logic Drawing 8a).

Insertion of the jumper causes the BCD to be read without conversion to the computer adapter. The BCD 10 code is equivalent to a "one" bit on lines $\overline{R4}$ and $\overline{R6}$ with $\overline{R2}$, $\overline{R3}$, $\overline{R5}$, $\overline{R7}$ and $\overline{RP}$ all "zero" bits.

The all-zeros code is automatically converted to the BCD 10 code when writing on a 7-track tape unit in the even parity mode. Therefore, there will be at least one track with a "one" bit in it to generate a read strobe when reading back. The BCD 10 code is FORBIDDEN as an industry standard when writing on 7-track tapes in the even parity mode unless the program is constructed to handle the following items:

1. Conversion of BCD 10's written to zero upon reading (no jumper).
2. Conversion of zero written to BCD upon reading (with jumper).

3.7.5 NO Parity Error for File Mark

The Controller is configured to blank parity errors when reading a 7-track file mark in the odd parity mode, or a "dummy" 7-track file mark on a 9-track unit (with no jumper installed between E2-9 on 76233-3(2) and GND).

With the jumper installed, the parity error indication is enabled.

3.8 Delay Times

There are three main delay times:

1. Predelay
2. Postdelay
3. Halt Delay

The Pre/Post delays are used to erase portions of the inter-record gap (when writing) or to erase tape. When reading, they are used to position the head correctly in the IRG so that the following record can be either a Read or a Write.

The Halt delay is also used to erase part of the IRG when writing and provides sufficient time to insure that the tape unit is completely stopped (after the motion signal is terminated).

There are many factors that enter into the various delays:

1. 7-track/9-track
2. Tape speed
3. Single/dual-stack head
4. Forward/reverse motion
5. BOT/$\overline{\text{BOT}}$
6. Write/Read command
7. EDIT/$\overline{\text{EDIT}}$ mode

Tables 3-9 through 3-13 give the delay times for a 9-track tape unit selected at the standard speeds of 75, 45, 37.5, 25, and 12.5 ips. Tables 3-14 through 3-18 give the same information for 7-track units.

3.9 COMPUTER ADAPTER SECTION

3.9.1 Computer Adapter Operation

The computer adapter consists basically of a control register, a status register, interrupt and skip logic, and an IOT decoder. The control register selects the tape transport unit, controls the Core Dump mode, stores the next command to be executed, and enables the generation of an Interrupt to the computer when the Magnetic Tape Flag (MTF) or Error Flag (EF) flags are set. The Control Register also controls the 3-cycle data break to the computer. The status register retains the controller status, the selected tape transport unit status, and the results of the last operation. The interrupt logic allows the tape controller to gain the attention of the computer program at the completion of an operation. The skip logic allows the program to test the status of the controller or the selected tape transport unit to ascertain when one or both is not busy. The IOD decoder allows the program to control the tape controller by execution of various IOT instructions.

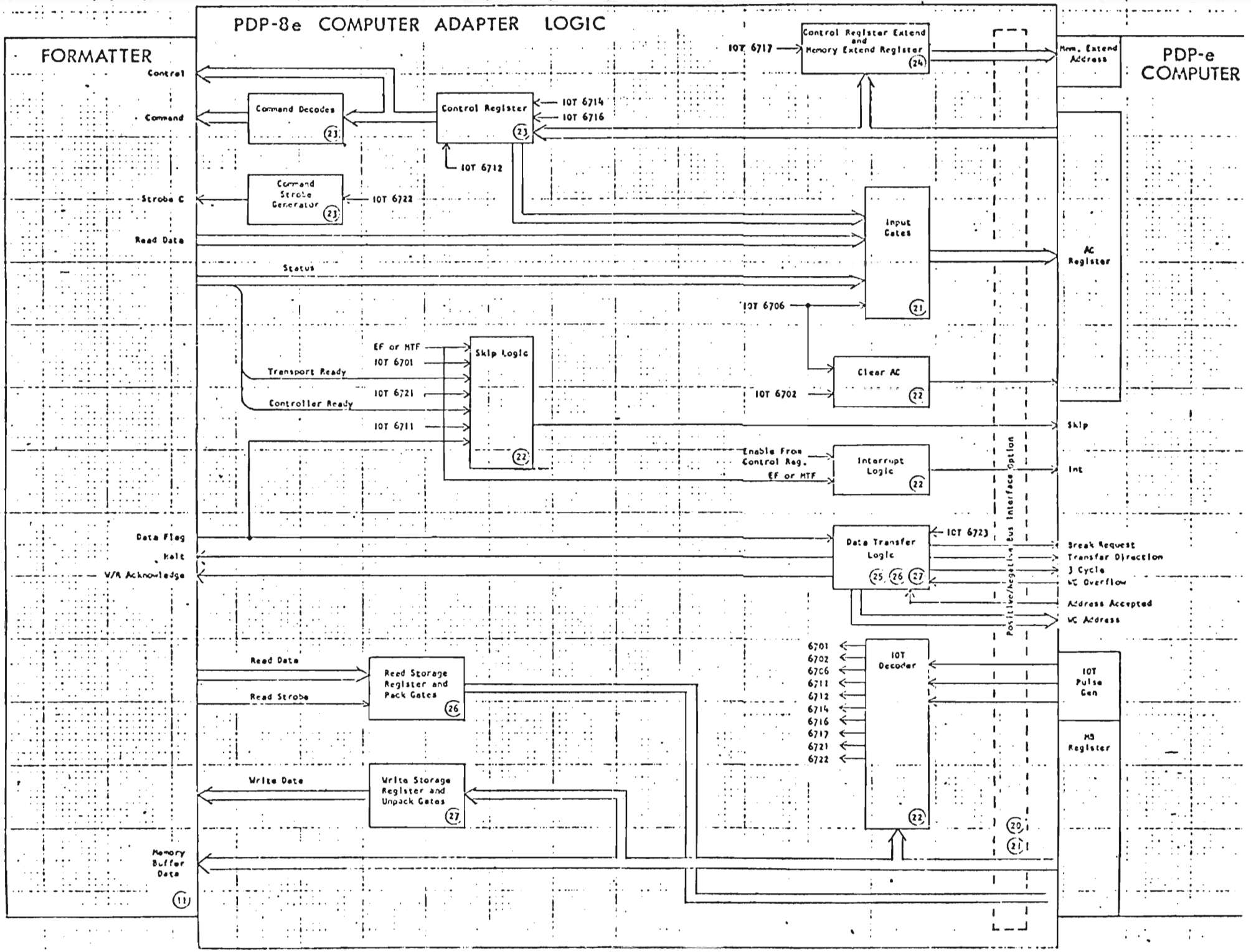
Control and status information transfers are effected by program execution of coded Input/Output Transfer (IOT) instructions. Control codes are output from the computer accumulator (AC) register to the computer adapter control register via the IOT instructions. Status bits are input from the computer adapter status register to the computer AC register via other IOT instructions. The program may be synchronized to controller operations by testing for the Magnetic Tape Flag (MTF) or the Error Flag (EF).

The MTF signifies normal completion of each operation while the EF signifies abnormal termination of an operation. With the 3-Cycle Data Break capability, the program may also be allowed to execute overlapped processing during magnetic tape I/O by using the Interrupt mode of operation. When the program sets bit 9 in the computer adapter control register, the occurrence of the MTF or EF at the termination of an operation will cause an interrupt. This interrupt may be used to interrupt main-line processing long enough to initiate the next magnetic tape I/O operation.

Magnetic tape operations are initiated by program execution of the MTGO IOT instruction. This instruction causes the coded command present in the computer adapter control register to be decoded and transferred into the Formatter command register (if it is a valid command). The operation is then initiated and the Formatter goes to the Busy state. When the operation is completed, the MTF is set. If the operation is terminated under abnormal conditions, the EF is also set.

3.9.2 Block Diagram of Computer Adapter Logic

Figure 3-10 is a simplified block diagram of the Computer Adapter. The Computer Adapter logic is illustrated in the center of the diagram. The Tape Controller is illustrated on the left and the computer interface is shown on the right. The circled numbers within each block designate the logic diagram in which the detailed logic appears. The Interface Option is indicated by the dashed box near the right-hand side of the Computer Adapter block.


PDP-8e COMPUTER ADAPTER LOGIC
FORMATTER
PDP-e COMPUTER
Control
Command
Strobe C
Read Data
Status
Data Flag
Halt
W/R Acknowledge
Memory Buffer Data
11
Command Decodes
23
Control Register
23
IOT 6714
IOT 6716
IOT 6712
Command Strobe Generator
23
IOT 6722
IOT 6717
Control Register Extend and Memory Extend Register
24
Mem. Extend Address
Input Gates
21
IOT 6706
AC Register
Skip Logic
22
EF or MTF
IOT 6701
IOT 6721
IOT 6711
Transport Ready
Controller Ready
Clear AC
22
IOT 6702
Skip
Enable From Control Reg.
EF or MTF
Interrupt Logic
22
Int
Positive/negative Bus Interface Option
Data Transfer Logic
25 26 27
IOT 6723
Break Request
Transfer Direction
3 Cycle
WC Overflow
Address Accepted
WC Address
Read Data
Read Strobe
Read Storage Register and Pack Gates
26
Write Data
Write Storage Register and Unpack Gates
27
6701
6702
6706
6711
6712
6714
6716
6717
6721
6722
IOT Decoder
22
IOT Pulse Gen
MB Register
20
21

3.9.3 Input/Output Transfer (IOT) Control Pulses

The memory extension register allows the three least-significant bits of the computer AC register to be stored in the computer adapter memory-extend register to provide a three-bit extension of the address to the computer. Control and status information is transferred via IOT instructions by the program. In order to effect transfer of the control and status information, the IOT decoder is utilized to gate the three IOP pulses (IOP1, IOP2, and IOP4) to the various logic elements of the computer adapter when the six-bit device-select address code for the tape controller is present on the computer MB register bus. The IOT control pulses are referenced on the block diagram by the actual octal IOT instruction code. The following gives the basic uses of the IOT's by octal code.

OCTAL CODE	INSTRUCTION
-6701	Skip on Error Flag or MTF set
-6702	Clear AC
-6706	Status —▷ AC
-6711	Skip on Controller Ready
-6712	Clear Flags and Control Register
-6714	Inclusive -OR AC—▷ Control Register
-6716	AC—▷ Control Register and Clear Error Flag/MTF
-6717	AC—▷ Control Extension Register (Mode, Offline, Memory Ext.)

AC						
6	7	8	9	10	11	
1	X	X	X	X	X	= Offline Mode
X	X	1	X	X	X	= Edit Mode
X	X	X	0	0	0	= 1st 4K of core memory
X	X	X	0	0	1	= 2nd 4K of core memory
X	X	X	0	1	0	= 3rd 4K of core memory
X	X	X	0	1	1	= 4th 4K of core memory
X	X	X	1	0	0	= 5th 4K of core memory
X	X	X	1	0	1	= 6th 4K of core memory
X	X	X	1	1	0	= 7th 4K of core memory
X	X	X	1	1	1	= 8th 4K or core memory

-6721	Skip on Tape Unit Ready
-6722	MTGO (initiate command)

3.9.4 AC Outputs

The twelve outputs of the Computer Accumulator (AC) register are wired to the inputs of the Computer Adapter control register, the Control Register Extension and the Prog. I/O option to the Write storage register. IOT 6714 will "inclusive-OR" the AC register into the control register. IOT 6716 will replace the contents of the control register with the contents of the AC regi ter. IOT 6712 will clear the control register and the MTF or the EF. IOT 6717 will load the AC register into the control Extension register.

3.9.5 AC Inputs

IOT 6706 first clears the AC register, then gates the contents of the status register through the input gates to the AC register. Since the AC register is cleared automatically by IOT 6706, there is no need for the program to clear the AC register first.

3.9.6 Interrupt/Skip

Control register bit 9 enables the interrupt logic so that the computer is interrupted if either the EF or MTF flag is set. The program may test for the tape controller Interrupt by generating OPT 6701. IOT 6701 will cause a skip pulse to be generated if either the EF or MTF flag is set. IOT 6712 may then be used by the interrupt subroutine to clear the interrupt flags. The computer program may also test for Tape Transport Unit and/or Tape Controller Ready by using IOT 6721 to test for Transport Ready status, and IOT 6711 to test for Controller Ready status.

Once the control codes have been transferred into the computer adapter control register, the tape-transport controller can be signalled to initiate the operation defined by the decoded commands by execution of IOT 6722 (Mag Tape Go). IOT 6722 causes the STROBEC pulse to be generated. The STROBEC pulse then transfers the decoded command into the tape transport controller command register (if the command is a "valid" one) and initiates the operation. When the operation is complete, the status lines may be sampled by the computer program to test for satisfactory completion of the operation. The computer program is signalled that the operation is complete by the EF or MTF flags. These two flags are set from the tape transport controller 2-CBUSY flip-flop, and generate an interrupt if bit 9 is set in the control register. If the command is not a valid one, the "Reject" status bit is set and the Error Flag is set.

Actual data transfer into or out of core memory is controlled by the data transfer logic. The data transfer logic operates the data break mode.

3.9.7 Data Transfer

The data transfer logic interfaces with the tape transport controller via the Data flag and the HALT and Write/Read Acknowledge (W/RACK) signals. The data transfer logic interfaces with the computer via the OMNIBUS and the control lines called BREAK REQ, XFER DIRECTION IN, THREE-CYCLE, WC OVERFLOW, and ADDRESS ACCEPTED, etc.

The THREE-CYCLE control line is always set to the three-cycle state because all transfers are in the three-cycle data break mode.

The XFER DIRECTION IN line indicates to the computer data-break facilities whether the data transfer is to be into core memory (in the case of a Read operation) or out of core memory (in the case of a Write operation).

The BREAK REQ signal is used for each twelve-bit data transfer to be made. The Data flag sets the BREAK REQ for each twelve-bit word transfer into core memory during the Read operation; the Data flag sets the BREAK REQ for each twelve-bit word transfer out of core memory during the write operation.

For write operations, the data output from the computer MB register is split into two successive six-bit characters for 7-track or 9-track core dump operations by the unpack gates. The unpack gates deliver the two successive characters to the Controller on the Write Data bus. For 9-track operations (not in the core dump mode), only the eight least-significant bits of the twelve-bit computer words are utilized. Similarly, for Read operations, two successive six-bit characters are packed into the twelve-bit Read storage register by the pack gates in 7-track or 9-track core-dump modes before inputting to the computer MB register. For normal 9-track operations, the eight-bit tape characters, plus the parity bit, are gated to the nine least-significant bits of the computer MB register bus.

3.9.7.1 Break Requests

When a break request has been initiated by a device, the device at time-state 4 must verify that it is the highest-priority break request device for that particular cycle. This is done by enabling the accumulator bits for all priority levels higher than the priority assigned to the requesting device, and checking time-state 4 to see if any of the higher-priority devices are also breaking. If not, a "go" signal is given to the break device and the break is continued with the requesting device.

When a break request cycle is initiated, a latch is set that tells the computer that there is a break in progress. This also enables a signal called CPMA DISABLE, which takes the control of the memory-address bus away from the CPU and allows the breaking device to control the address bus from the memory address register. As soon as the break device has this capability, a three-cycle break is initiated.

During the word count portion of the three-cycle break, the memory address bus, as shown on Sheet 25B of the logic, allows the hard-wired address (which is pre-wired using chip G6) for the current address number. As indicated on the logic, this hard-wired address is gated on the bus less the least significant bit, to show the computer where the word count is located.

Again, a priority check is made at the end of the word count cycle, to see if another, higher-priority, device has made a break request. If not, the device will continue with cycle 2 and the hard-wired address, with the least-significant bit, will go to the current address on the address bus.

At time 3 of the second cycle, the memory data on the bus is stored in the register shown on this logic to give the current address location that will be used for the third cycle of the break.. During the third cycle, the data will be transferred to the address that is stored in the buffer either to put data into the core during a Read mode, or take it out of core for a Write operation.

During the word count and current-address portions of the break cycles, the data that is brought out of the word count and current address locations is incremented before being restored into memory by a signal called INCR, which is on logic 27. This incrementing is done at the beginning of the cycle to increment the location before the transfer is completed. If, during the word count portion of the cycle, the word count in the location overflows to zero, a word count overflow signal is generated that terminates the data-transfer portion and halts transfer until the next Write or Read operation is commanded by the computer.

If, during a Read mode, the Word Count Overflow is initiated before the end of the record, the record will continue to be read but no more data will be placed into the core. This Word Count Overflow signal also generates the Halt signal, which shuts off the data gate and, in a Write mode, causes the controller to start the countdown for writing the CRC and LRC character.

On a nine-track machine the CRC will be valid; on a seven-track machine the CRC will not be written. If, during any three-cycle operation, it is determined at time 4 of the computer cycle that a higher-priority device is also requesting, the controller will hang in its present state, holding all data and control functions, until the next computer cycle, and at time-state 4 will again check tosee if it has priority. When there are no priority-request devices of a higher priority requesting, then the device will continue on and complete the three-cycle break.

3.9.8 Programmed I/O

3.9.9 IOT Instructions

3.9.9.1 Skip on Error Flag (EF) or Mag Tape Flag (MTF)

MTSF — Octal 6701

The state of the EF and MTF status bits are sampled. If either (or both) is set, a pulse is returned on the skip bus to skip the next sequential instruction. This instruction allows the program (when interrupted) to test the tape controller to ascertain if the tape controller is generating the Interrupt. The EF- and MTR-generated Interrupt is not cleared until either a "Clear Register and Flags" or "Load Control Register" (MTLC) IOT instruction is executed; hence, the ION IOT instruction (octal 6001) should not be executed to enable interrupts until after the MTAF or MTLC instruction is executed in the magnetic tape interrupt service subroutine.

3.9.9.2 Clear AC

Octal 6702

Clears AC register.

3.9.9.3 Read Status

MTRS — Octal 6706

Status register is loaded into AC.

3.9.9.4 Skip on Tape-Controller-Ready

MTCR — Octal 6711

This instruction allows the computer program to test the tape transport controller status (busy or not busy).

3.9.9.5 Clear Register and Flags

MTAF — Octal 6712

This instruction clears the status and control registers (including EF and MTF interrupt flags) if the tape controller is ready. If the tape controller is not ready, this instruction clears only the EF and MTF flags.

3.9.9.6 Inclusive-OR AC Into Control Register

MTCM — Octal 6714

This instruction transfers three command bits (AC_6, AC_7, and AC_8) and three select bits (AC_0, AC_1, and AC_2) into the control register and "inclusive-OR's" the rest of the AC into the control register.

3.9.9.7 Load Control Register

MTCL — Octal 6716

The load control register instruction produces different results, depending upon the status of the tape-transport controller (i.e., busy or not busy).

a. Controller Not Busy - The EF and MTF flags are cleared. The contents of the AC register are loaded into the control register, thereby selecting the designated tape transport unit.

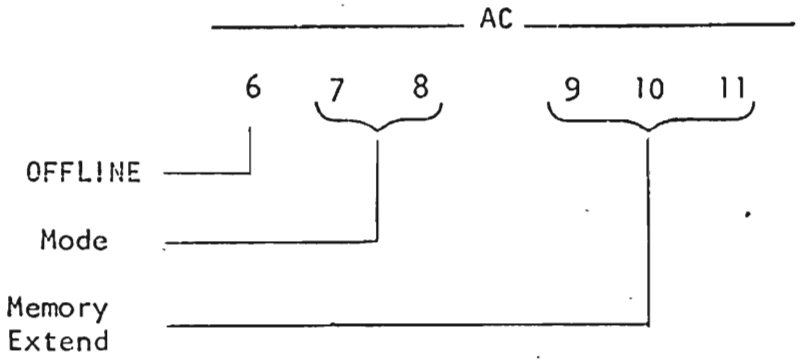
b. Controller Busy - The EF amd NTF flags are cleared. Bits 3, 4, 5 and 9, 10, 11 of the AC register are "inclusive-OR'ed" into the corresponding bits of the control register, while bits 0, 1, 2, 6, 7 and 8 (select and command code) replace corresponding bits of the control register.

3.9.9.8 Load Control Register Extension

Octal 6717

This instruction causes the least-significant six bits of the computer AC register to be loaded into the control extension register. The control extension register extends the most-significant end of the CA to allow addressing of up to 32K memory. It also provides mode control over the EDIT function, the marginal-read threshold for single-gap read-checking of each record after it is written (THR1), and the low data recovery read threshold Z (THR2). The OFFLINE command bit is also located in the control extension register.

Control Register Extension Format



Mode		
7	8	
0	0	Normal
0	1	Edit
1	0	THR1
1	1	THR2

NOT USED

Memory Extend			4K Core Addressed
9	10	11	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

The computer START switch causes the tape controller to reset the extension register to 000 (baskc 4K memory).

3.9.9.9 Skip on Tape-Transport-Ready

MTTR — Octal 6721

This instruction allows program to test the selected tape transport unit status (ready or not ready).

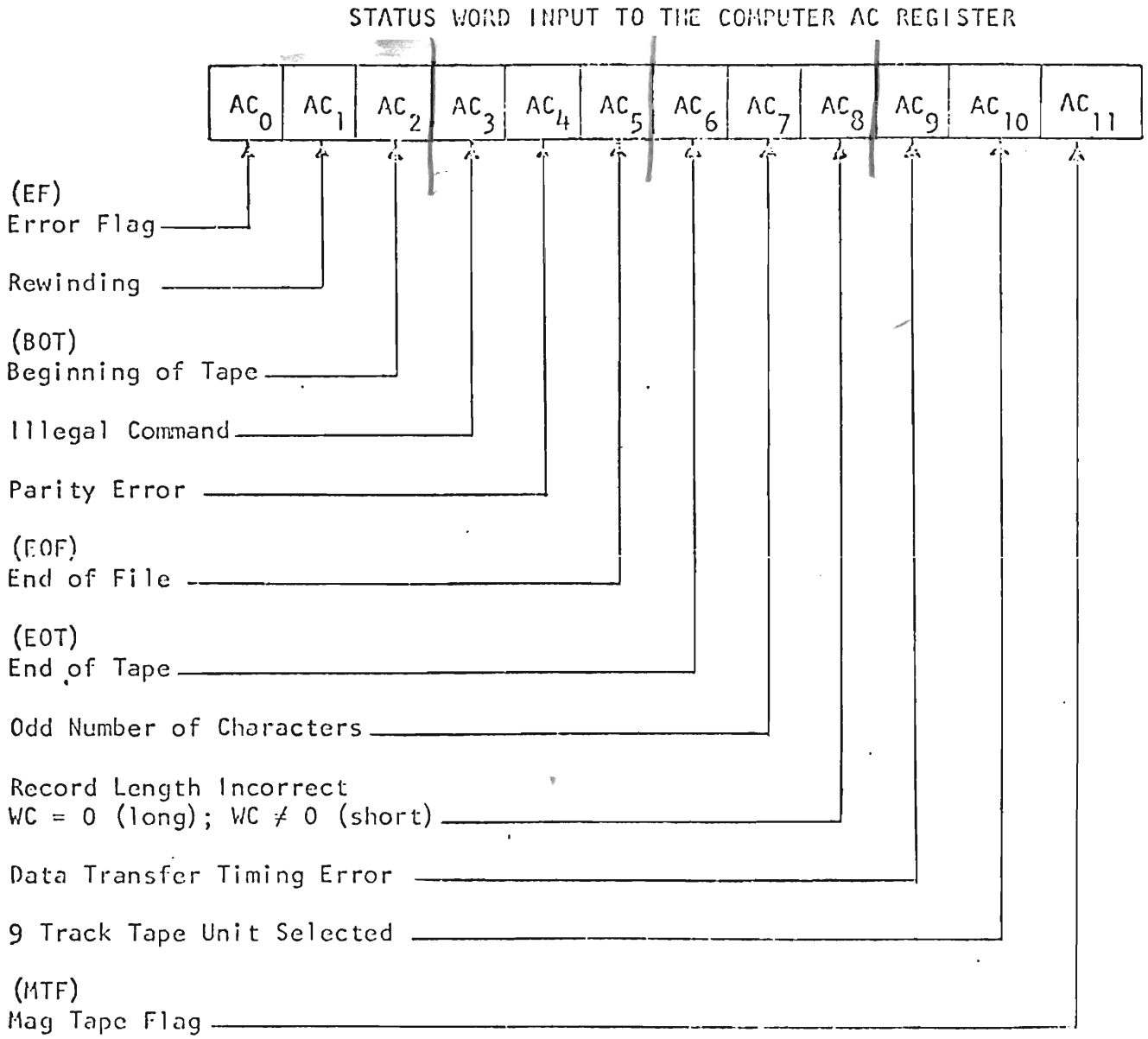
3.9.9.10 Mag Tape GO

MTGO — Octal 6722

This instruction causes the controller to execute the command present in bits 6, 7, and 8 of the control register (if a legal command). It also causes bit 5 (Erase 3" Gap) of the control register to be reset to zero if on. MTGO can be jumper-selected to load the control extension register from the AC register instead of IOT 6717. This gives control over the OFF-line command, edit mode, RTHR1 and RTHR2 modes and memory extension with MTGO.

3.9.10 STATUS WORD FORMAT

The status word is input to the computer AC register with an MTRS (Mag Tape Read Status) IOT instruction, octal 6706.


STATUS WORD INPUT TO THE COMPUTER AC REGISTER
AC0
AC1
AC2
AC3
AC4
AC5
AC6
AC7
AC8
AC9
AC10
AC11
(EF)
Error Flag
Rewinding
(BOT)
Beginning of Tape
Illegal Command
Parity Error
(EOF)
End of File
(EOT)
End of Tape
Odd Number of Characters
Record Length Incorrect
WC = 0 (long); WC ≠ 0 (short)
Data Transfer Timing Error
9 Track Tape Unit Selected
(MTF)
Mag Tape Flag

3.9.11 Error Flag (AC_0)

The Error Flag (EF) sets if any error status bit (AC_4, AC_6, AC_8, or AC_9) is on when MTF is set at the conclusion of an operation, or if an illegal command is attempted. MTF is not set for the illegal command case. EF causes an interrupt if bit 9 is set in the control register. The status or MTF or EF can be tested with IOT instruction 6701 (MTSF) Mag Tape Skip on Flag Set. EF may be reset (to clear the interrupt condition) by IOT MTLC (Load Control Register) or MTAF (Clear Registers and Flags).

3.9.12 Rewinding (AC_1)

Set while selected tape transport unit is in rewind mode.

3.9.13 Beginning-Of-Tape (AC_2)

Set while selected tape transport unit is on the beginning-of-tape (BOT) marker.

3.9.14 Illegal Command (AC_3)

Illegal commands are:

a. MTGO command is issued when tape controller is busy

b. MTGO command is issued to a tape transport unit that is not ready (even though tape controller may be ready).

c. Write-One-Record or Write EOF command is issued when no write-enable ring is in reel.

d. Space-reverse command is issued when at BOT. If the tape requires movement to reach BOT on a space reverse, then the result is not an illegal command.

e. An MTGO command when bits 6, 7, and 8 of the control register are set to 000.

The EF (AC_0) status flag is set, but MTF (AC_{11}) does not set for an illegal command.

3.9.15 Parity Error (AC_4)

The parity error detection is for both vertical odd parity checks on each character and upon longitudinal even parity checks on each track throughout the entire record for an NRZI tape unit. Parity error detector can be indicated by a number of error conditions for a 1600-BPI tape unit (see 1600 Formatter manual).

Once a parity error is detected, the status bit remains set until either the MTAF (6712) or MTLC (6716) instruction is issued to clear the status and control registers. Parity is checked for a Read-One Record, a Write-One-Record, a Space Forward or a Space Reverse operation.

3.9.16 End-of-File (AC_5)

The EOF status bit is set if an end-of-file mark is encountered during any tape movement operation except Rewind.

The EOF status bit is also set if an end-of-file mark is encountered on a Space Forward or a Space Reverse. When the space commands are terminated due to a file mark, the program can interrogate WC to determine the number of records spaced over prior to encountering the end-of-file mark. The end-of-file mark is counted as a record.

3.9.17 End-of-Tape (AC_6)

The EOT status bit sets when the EOF foil is initially sensed (however, the operation is completed). At completion, both the EF and MTF status bits are set and the interrupt is generated (if enabled). The EOT status does not clear until the tape transport is commanded to Rewind or Space Reverse.

3.9.18 Odd Number of Characters (AC_7)

For 7-track or 9-track core dump Read operations, if an odd number of characters is contained within a record, this status bit is set as well as the "Record Length Incorrect" (AC_8) status bit. This occurs because there are normally two 6-bit tape characters packed into each 12-bit computer word. For odd-character record lengths, the least-significant half of the last 12-bit computer word must be discarded by the software.

3.9.19 Record Length Incorrect (AC_8)

During a Read operation, this status bit is set whenever the WC overflow does not agree with the number of words actually read. The EF is set when MTF is set upon completion of the Read operation and the Interrupt is generated (if enabled).

3.9.20 Data Transfer Timing Error (AC_9)

This status bit sets whenever a word is not transferred in time in either a Write or a Read cycle. The EF status bit is set when the MTF is set at the completion of the operation and an interrupt is generated (if enabled).

3.9.21 9-Track (AC_{10})

This status bit is set whenever a 9-track tape-unit is selected.

3.9.22 Magnetic Tape Flag (AC_{11})

The magnetic tape flag (MTF) status bit is set whenever the tape controller has completed an operation and is ready to accept the next command.

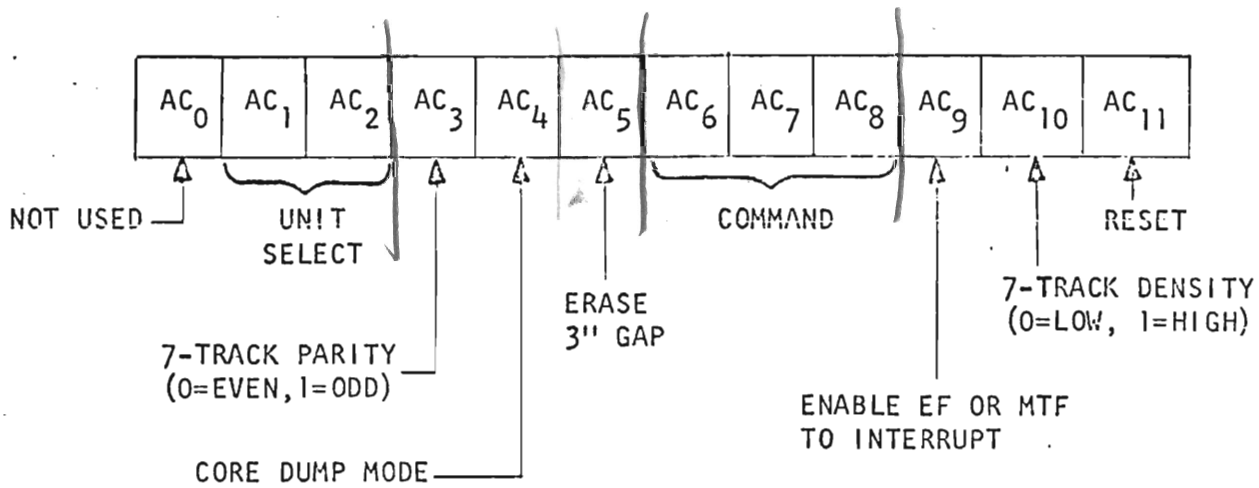
MTF causes an interrupt if bit 9 is set in the control register, When MTF goes set, the Error Flag (EF) will set if any errors are present.

MTF or EF can be tested with IOT instruction 6701 (MTSF) Magnetic Tape Skip on Flag Set.

MTF may be reset (to clear the interrupt condition) by IOT MTLC (load Control Register) or MTAF (Clear Register and Flags).

3.9.23 Control Word Format

The control register bits are illustrated in conjunction with the bits of the computer AC register:



Tape Unit Select Code		Tape Unit Selected
AC_1	AC_2	
0	0	0
0	1	1
1	0	2
1	1	3

The specified tape transport unit is selected when the control register is loaded, regardless of command.

Command Codes			
AC_6	AC_7	AC_8	
0	0	0	No operation
0	0	1	Rewind
0	1	0	Read One Record
0	1	1	Test Read
1	0	0	Write One Record
1	0	1	Write File Mark
1	1	0	Space Forward
1	1	1	Space Reverse

The NO-OP command will cause an illegal-command error. The illegal-command error sets status bit AC_3 and EF to cause an Interrupt (if enabled), if an MTGO instruction is executed while NO-OP code is present in the command register.

The control register is loaded or modified by the computer program, using either MTLC or MTCM IOT instructions. See Section 3.9.11 for commands explanation.

3.9.23.1 Erase 3" Gap (AC_5)

This causes three inches of tape to be erased. This bit may be used by itself or in conjunction with a Write or Write EOF to erase a bad section of tape. A gap will be erased on the tape if MTGO is executed and the command is Read One Record or Space Forward giving an erroneous result. This bit is always reset automatically by the tape controller upon the execution of an MTGO instruction.

3.9.23.2 Reset (AC_{11})

This bit "forces" a reset to the Formatter when IOT 6716 is generated and the jumper is installed between 23X1 and 23Y1 (see logic 22). This is useful for test purposes to halt a "runaway" tape condition and loop on one command sequence for trouble shooting.

3.9.23.3 Enable Interrupt (AC_9)

The computer will be interrupted if this bit is set, and either MTF (Magnetic Tape Flag) or EF (Error Flag), or both MTF and EF are set. MTSE IOT is used to determine whether MTF or EF caused the interrupt.

3.9.23.4 7-Track Parity (AC_3)

When the NRZI Formatter is in the "Remote" mode, this bit controls the Write/Read parity selection for 7-track tape units (0 = even parity, 1 = odd parity).

3.9.23.5 7-Track Density (AC_{10})

When the NRZI Formatter is in the REMOTE mode, this bit controls the selection of Write/Read density (0 = low density, 1 = high density).

3.9.23.6 Unit Select (AC_{1-2})

These two bits select the tape transport unit. Switches are provided on the Formatter for switching tape transport units to any of the four logical unit numbers.

3.9.23.7 Core Dump Mode (AC_4)

This mode allows complete twelve-bit memory words to be transferred as two six-bit tape characters for 9-track tape units. Bits 0 through 5 form character number 1 and bits 6 through 11 form character number 2. When employing the Read One Record command or Write One Record command in core dump mode, it is necessary to load the WC with the negative of the number of twelve-bit words (half the number of tape characters) to be transferred. The core dump mode is ignored unless the operation is a Read or Write One Record.

3.9.24 Commands (AC_{6-8})

3.9.24.1 Rewind

The Rewind command causes the selected tape transport unit to rewind to the beginning of tape. The program may initiate rewind on one unit and then immediately select a different unit and continue operating while the original unit is rewinding.

a. If the program does not execute either an MTLC (6716) or an MTCM (6714) to select a different tape transport unit prior to the termination of the rewind to the original unit, the MTF will be set on the completion of Rewind to cause an Interrupt (if enabled). The selected tape transport unit and the tape controller remain not ready until the rewind is complete so that the program can use MTSF (6701), MTCR (6711), MTTR (6721) or Interrupt to ascertain when the tape controller and tape transport unit are ready.

b. If the program executes an MTLC (6716) or MTCM (6714) to select a different tape transport unit prior to the termination of the rewind operation, the MTF will set a

short time after execution of MTLC or MTCM (providing the second tape transport unit is ready). At this time, an Interrupt will occur (if enabled) and the tape controller is ready for another command. The rewinding tape transport unit will remain Not Ready until the rewind is complete.

NOTE: This is the only time that MTF is set after execution of an MTLC or MTCM that is not followed by an MTGO (6722).

3.9.24.2 Read-One-Record

The Read-One-Record command causes the next record to be read into core memory. Records may be read forward or reverse, and both computer CA and WC core memory three-cycle data break control registers must be set up before issuing the command. The CA register must be set to the initial buffer address, minus one; the WC register must be set to the twos-complement of the number of twelve-bit computer words to be used.

If WC is set to less than the actual record length, the indicated number of words is read in and data transfer halts, although the tape continues moving until it reaches the next inter-record gap. If WC is set to greater than the actual record length, the entire record is input.

In either case, the parity checks are performed on the entire record and the MTF is set to interrupt (if enabled) when the tape transport unit halts in the next inter-record gap. If the record length does not match the WC on completion, bit 8 of the status word is set to 1, the EF is set, and the WC can be interrogated to determine if the record was longer or shorter than expected.

When reading forward, the CRC and LRC characters are stripped off by the NRZ Formatter.

3.9.24.3 Write-One-Record

The Write-One-Record command requires that the CA and WC core locations be set up before execution.

The CA register must be set to the initial core address, minus one; the WC register must be set to the two's complement of the number of twelve-bit computer words or eight-bit tape characters to be transferred (depending on whether the core dump mode is utilized). For 9-track operations, when WC overvlows (indicating the last word to be written), the three-cycle data break transfer ceases, the CRC character is written after three blank characters, the LRC character is written after three more blank characters (per IBM 9-track specifications), and a portion of the inter-record gap (IRG) is erased. The tape transport unit halts and the MTF is set to interrupt the program (if enabled. The Read-After-Write logic performs both vertical (character) and longitudinal parity checks on the written record. For 7-track operations, the CRC character is deleted and the LRC character is generated after three blank characters. If a single-gap tape unit is used, the program should backspace and read the record in threshold 1 mode to perform a marginal check on each record written. If there is a parity error, the program should backspace and erase that section of tape, then rewrite the record.

3.9.24.4 Write EOF

For 9-track NRZI operations, the Write EOF command causes an octal 023 character to be writtin on tape, seven blank characters (no CRCC), then the LRC character (which in this case is another octal 023 character). This format is per IBM 9-track specification.

The tape transport unit erases a portion of the IRG and then halts. The MTF is then set and the interrupt is generated (if enabled). The Read-After-Write logic should cause the EOF status bit to be set to indicate that the EOF has been successfully written. For 7-track NRZI operations, two even-parity octal 17's are written four character-spaces apart per IBM 7-track specification. There will not be a parity error indication for 7-track odd parity mode file marks unless the Controller enable jumper for file-mark parity errors is installed.

3.9.24.5 Space Forward

The Space Forward command requires that the computer WC core location be loaded with the two's complement of the number of records to be spaced over. The computer CA core location need not be set up since it is ignored. When WV overflows, or when EOF or EOT is detected, the tape transport unit is halted in the IRG and MTF is set to interrupt the program (if enabled). Records are spaced-over continuously without stopping in the inter-record gaps. Parity is checked and the EOF status bit is set if an EOF terminates the Space-Forward operation. A file mark is counted as a record.

3.9.24.6 Space Reverse

The Space Reverse command requires that the computer WC core location be loaded with the two's complement of the number of records to be spaced over before execution. The CA register is ignored as in the Space Forward command. When WC overflows, or EOF is detected, the tape transport unit is halted in the IRG and the MTF is set to interrupt the program (if enabled). Records are spaced-over continuously without stopping in the inter-record gap.

Detection of BOT while spacing in reverse will terminate tape movement on the BOT marker with the BOT status bit set. When BOT is detected in a space reverse operation, the tape transport unit becomes not ready for approximately 0.5 second.

The EOF status bit is set if an EOF terminates the space reverse operation. A file mark is counted as a record.

3.9.24.7 Test Read

This function is identical to a Read-One-Record command, with the exception that the tape controller will also input the LRC and CRC (NRZI only) characters to the computer in the forware mode. The WC register should be set to the two's-complement of the number of tape characters plus two (9-track) or plus one (7-track). The command is included for maintenance purposes and should not be used in the core dump mode.

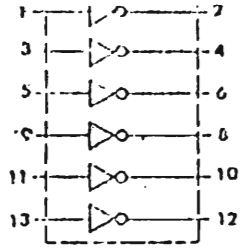
DATUM, INC.'s INTEGRATED CIRCUIT DIAGRAMS

Integrated Circuit Diagrams are presented on the following pages as drawn by DATUM. I. C.'s listed on this page are pin compatible with diagrams existing in following pages as follows:

IC TYPE	PIN REFERENCE	DESCRIPTION
7401	7402	(4) 2 Input Pos. NAND (Open Col.)
7407	7406	HEX Inverter (Open Col.)
7409	7403	(4) 2 Input Pos. AND (Open Col.)
7411	7410	(3) 3 Input Pos. AND
7416	7406	HEX Inverter (Open Col.)
7417	7406	HEX Inverter (Open Col.)
7421	7420	(2) 4 Input Pos. AND
7426	7403	(4) 2 Input Pos. NAND (15v)
7445	7442	BCD To Dec. Decoder/Driver
7451	7450	Dual 2-Wide 2-In AND-OR-INVERT
74141	7441	BCD To Dec. Decoder/Driver
74H00 *	7400	Same as Lower Speed Series
74L00 **	7400	Same as Lower Power Series
15930 ***	15830	Same as High Temperature Series

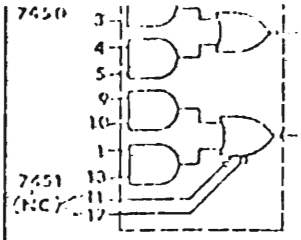
* 74Hxx Series will be found by ignoring the "H" in number.
** 74Lxx Series will be found by ignoring the "L" in number.
*** 159xx Series will be found by looking in the 158xx numbers.

7405
7406
7407
15836
7416
7417



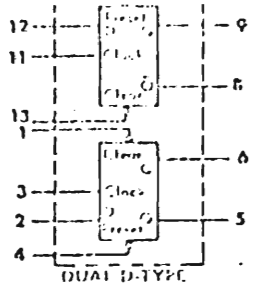
HEX INVERTERS

7450



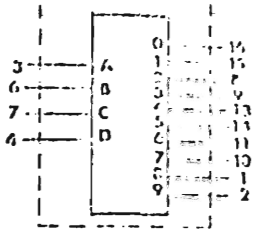
7451 (NC)

EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES



DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

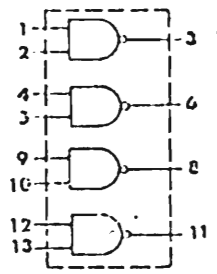
74141



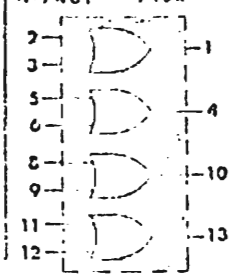
16 (P) 12 • G 5 • V

BCD — DEC DECODE

7400
7403
7408
7409
15846
7426
7437
7438

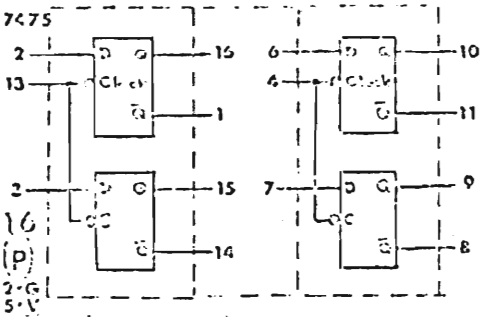


7401 7402



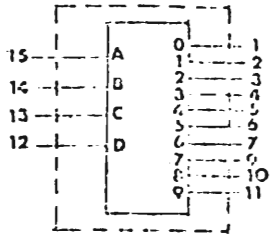
QUADRUPLE 2-INPUT POSITIVE GATES

7475



16 (P) 12 • G 5 • V

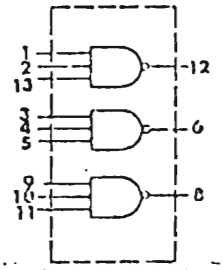
7442
7445
74145



16 (P) 8 • G 16 • V

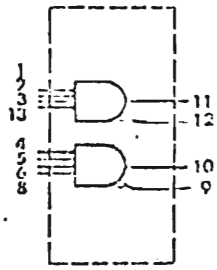
4—10 BCD — DEC DECODE

7410
7411
15862



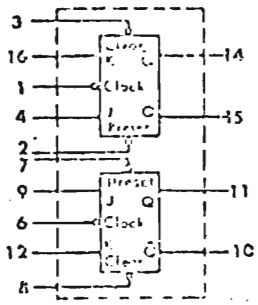
TRIPLE 3-INPUT POSITIVE GATES

7460



EXPANDABLE - DUAL 4-INPUT

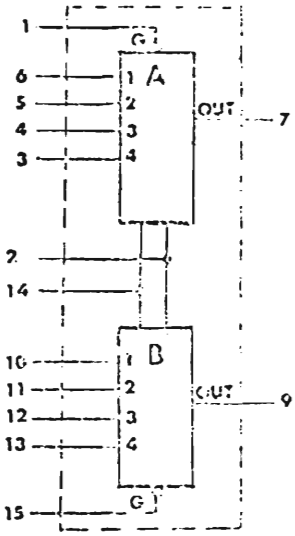
7476



16 (P) 13 • G 5 • V

DUAL J-K MASTER-SLAVE

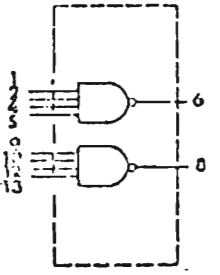
74153



16 (P) 8 • G 16 • V

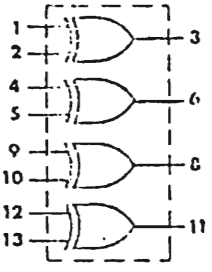
4—1 DATA SELECT/MUX

7420
7421
7440
15830
15844



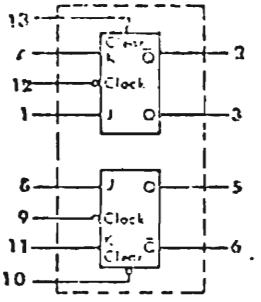
DUAL 4-INPUT POSITIVE GATES

7486

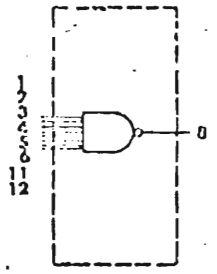


EXCLUSIVE OR QUADRUPLE 2-INPUT

74107

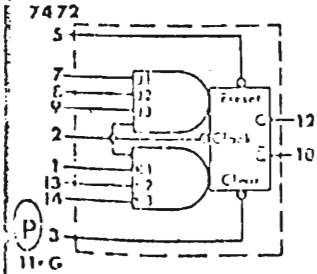


7430



8-INPUT POSITIVE NAND GATES

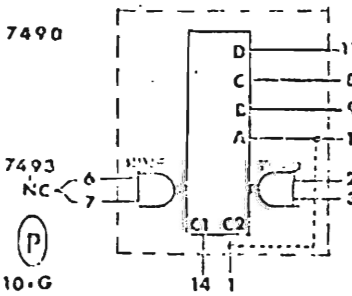
7472



16 (P) 11 • G 4 • V

J-K MASTER-SLAVE

7490

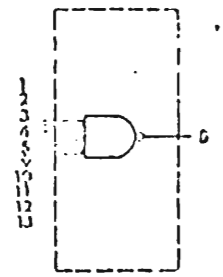


7493 (NC)

16 (P) 10 • G 5 • V

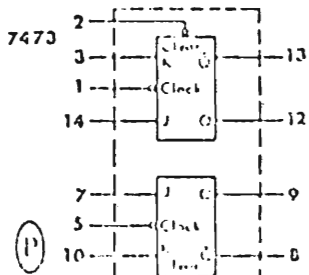
DECADE COUNTER

151804



10-INPUT POSITIVE NAND GATES

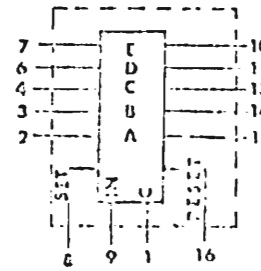
7473



16 (P) 11 • G 4 • V

DUAL J-K

7496



16 (P) 12 • G 5 • V

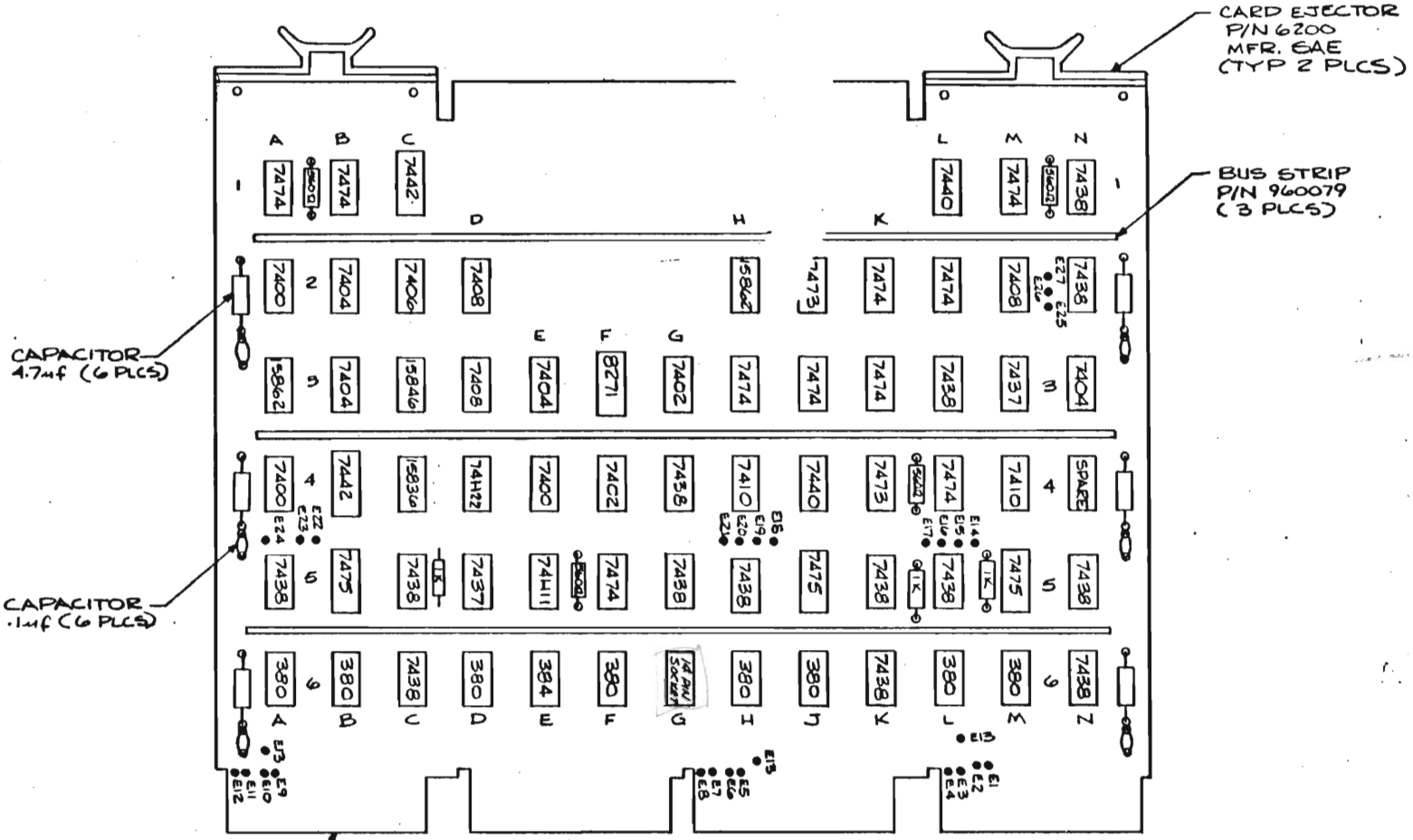
SHIFT REG

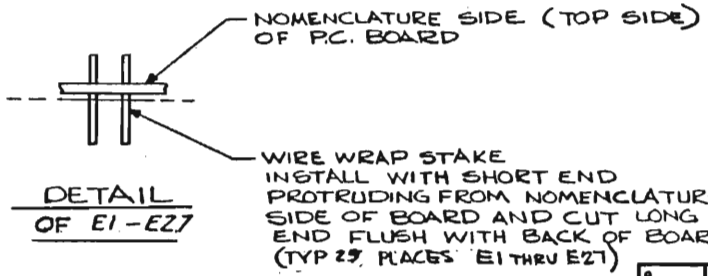
SECTION IV

DRAWINGS

76225	P8e Controller Data Break Assembly
76227	P8e Controller Control and Timing
76232	Tape Control Assembly
76233	Data Transfer Control Assembly
76258	PDP8e Connector Board

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
B	ADDED: R7 1K RESISTOR, 14 PIN I.C. SOCKET AT 66 LOCATION; D4 WAS 7440 R&S	2/21/73	
C	SEE CHANGE ORDER 0062	5-2-73	





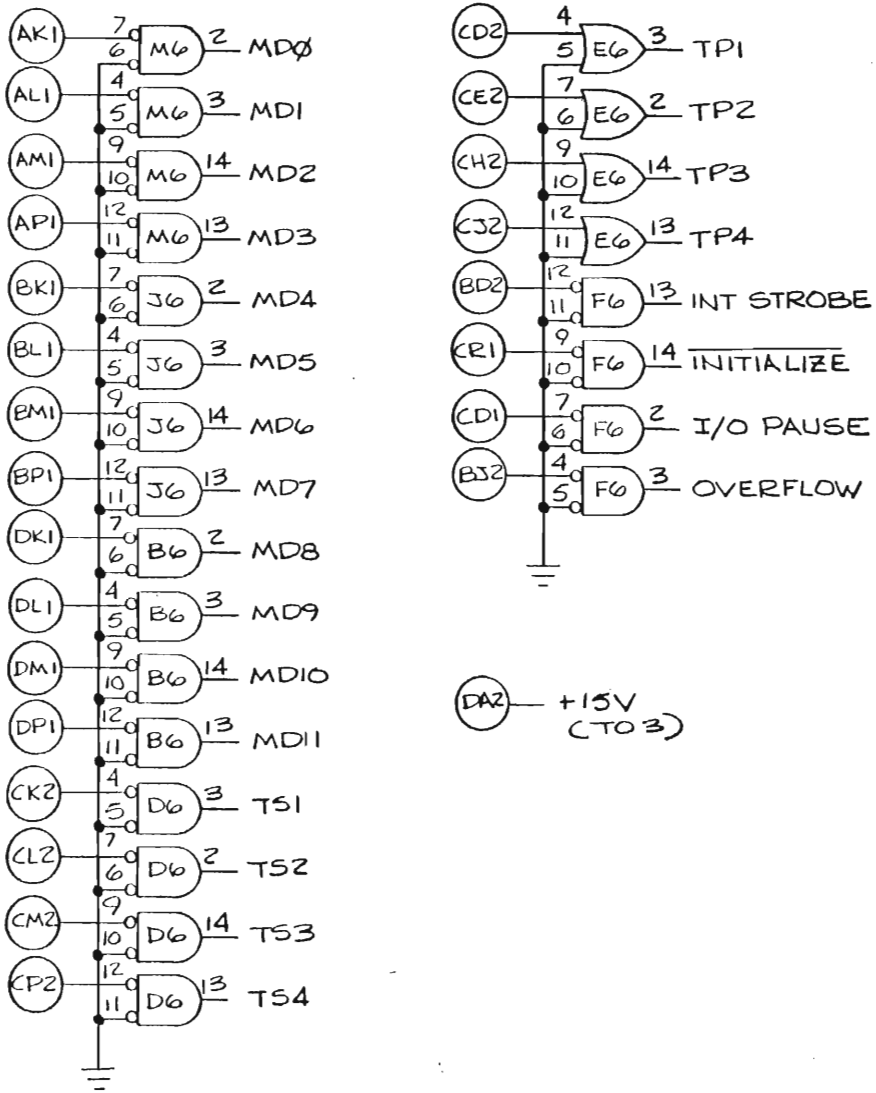
DETAIL
OF E1-E27

1.) • DENOTES W/W STAKE

NOTES: UNLESS OTHERWISE SPECIFIED

TITLE	P8e CONTROLLER DATA BREAK ASSY	datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
DWN Lous 3/21/73	DES	C	76225 C
CHK	ENGR		
SCALE FULL	FSC 31160	SIZE	SHT 1 OF 8 REV

SIGNALS FROM COMPUTER



BI-DIRECTIONAL SIGNALS

21-DAØ — AR1
21-DA1 — AS1
21-DA2 — AU1
21-DA3 — AV1
21-DA4 — BR1
21-DA5 — BS1
21-DA6 — BU1
21-DA7 — BV1
21-DA8 — DR1
21-DA9 — DS1
21-DAIØ — DU1
21-DA11 — DV1
27-MD DIR — AK2
24-$\overline{\text{EMAØ}}$ — AD2

SIGNALS TO COMPUTER

24-$\overline{\text{EMA1}}$ — AE2
24-$\overline{\text{EMA2}}$ — AH2
22-INTERNAL I/O — CL1
22-SKIP — CS1
27-BRK IN PROG — BE2
27-CPMA DISABLE — CU1
27-MS, IR DISABLE — CV1
27-MA, MS LOAD CONT — BH2
27-BREAK CYCLE — BL2
27-BREAK DATA CONT — BK2
22-$\overline{\text{INT REQ}}$ — CP1
22-CØ — CE1
22-C1 — CH1

25-MAØ — AD1
25-MA1 — AE1
25-MA2 — AH1
25-MA3 — AJ1
25-MA4 — BD1
25-MA5 — BE1
25-MA6 — BH1
25-MA7 — BJ1
25-MA8 — DD1
25-MA9 — DE1
25-MAIØ — DH1
25-MA11 — DJ1

(20)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03, .XXX ±.010, ANGLES ± 1/2°

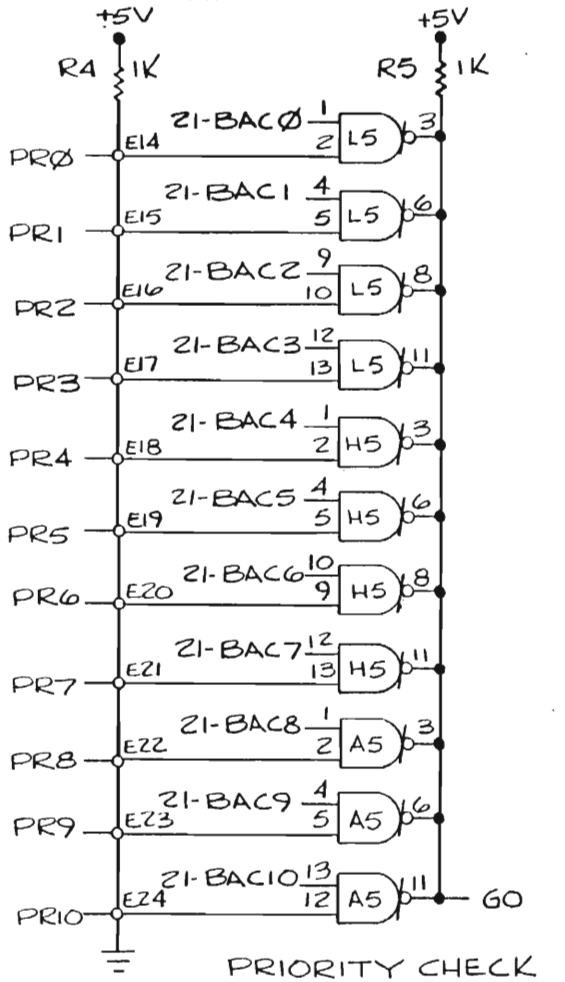
TITLE: P8e CONTROLLER DATA BREAK

DWN Louis 12/10/71 | DES | CHK | ENGR | SCALE NONE | FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

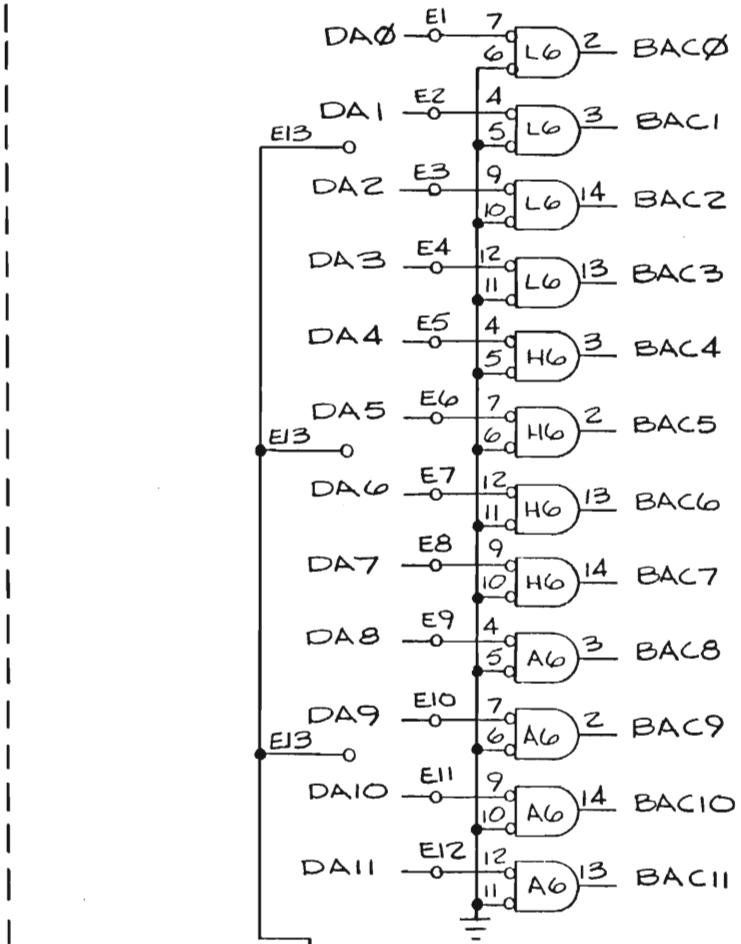
B | 76225 | C
SIZE | SHT 2 OF 8 | REV

DIETZGEN 196 MG-10

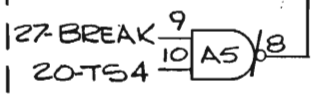


PRIORITY CHECK

25a



21a



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

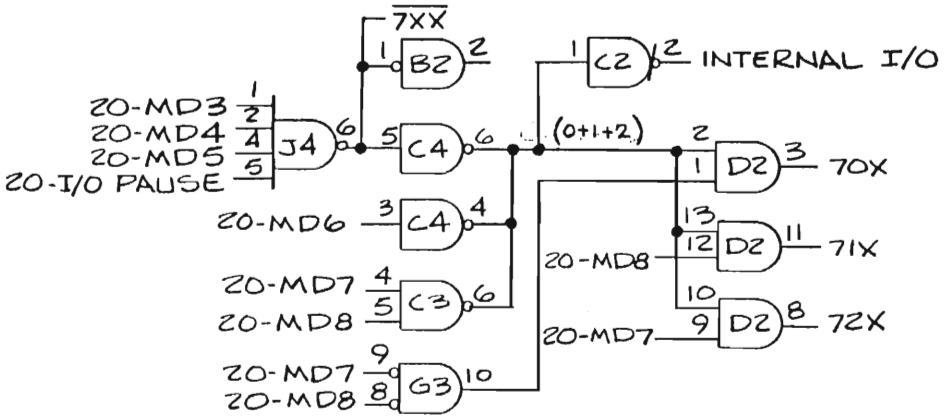
TITLE

P8e CONTROLLER
DATA BREAK

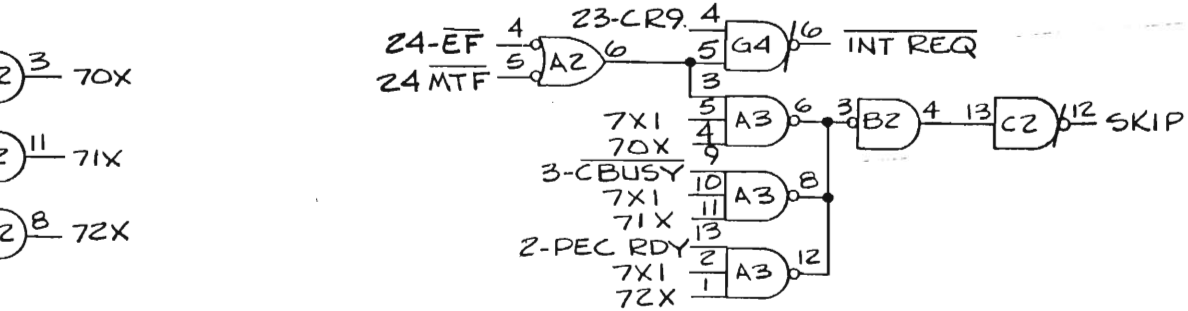
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	LAWS	12/2/71	DES		
CHK			ENGR		
SCALE	NONE	FSC	31160	SIZE B	76225 C
				SHT 3 OF 8	REV

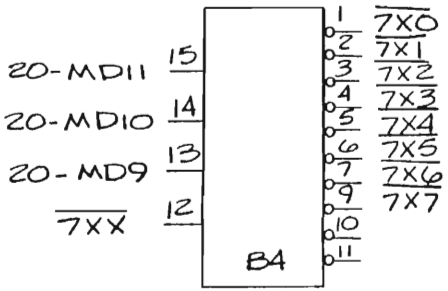
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

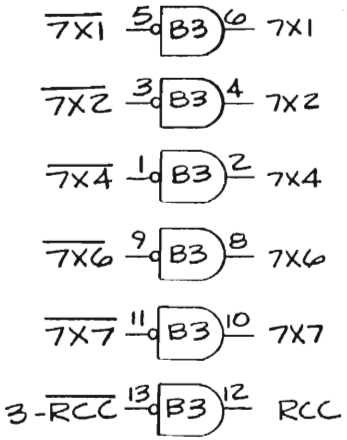


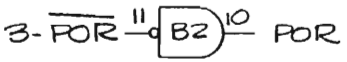
IOT RECOGNITION & DECODE

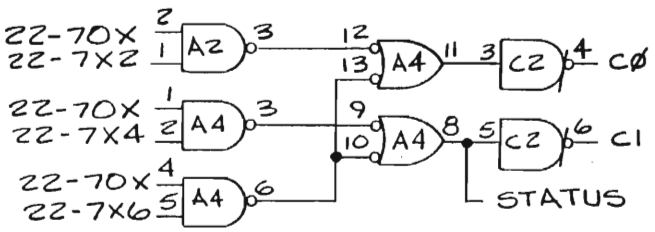


SKIP CONTROL LOGIC









CONTROL LINE GENERATION

(22)

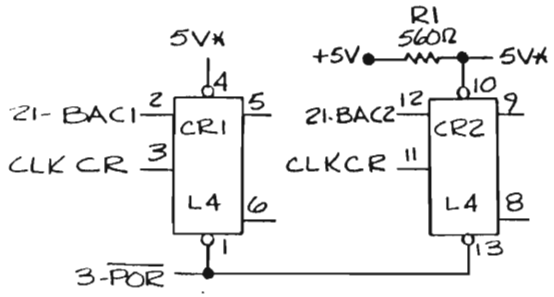
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

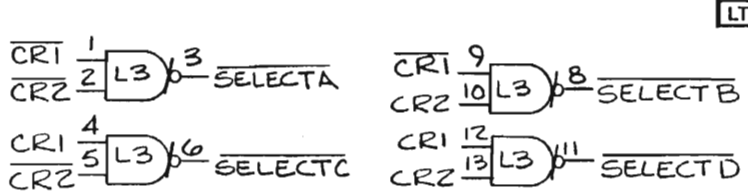
TITLE
P8e CONTROLLER
BREAK DATA

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

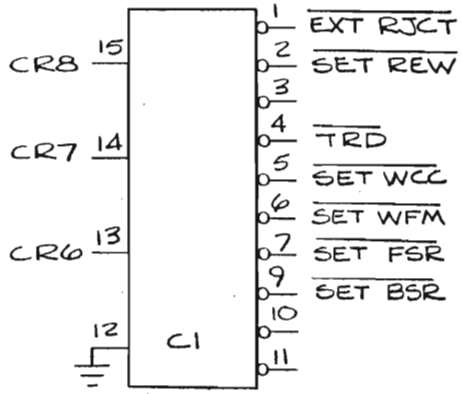
DWN	Laws	12/10/71	DES		B	76225	C
CHK			ENGR				
SCALE	NONE		FSC	31160	SIZE	SHT 4 OF 8	REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

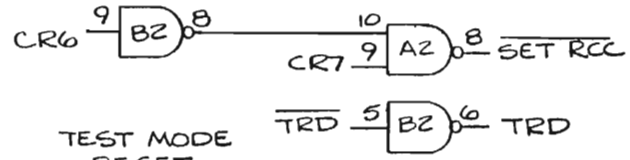


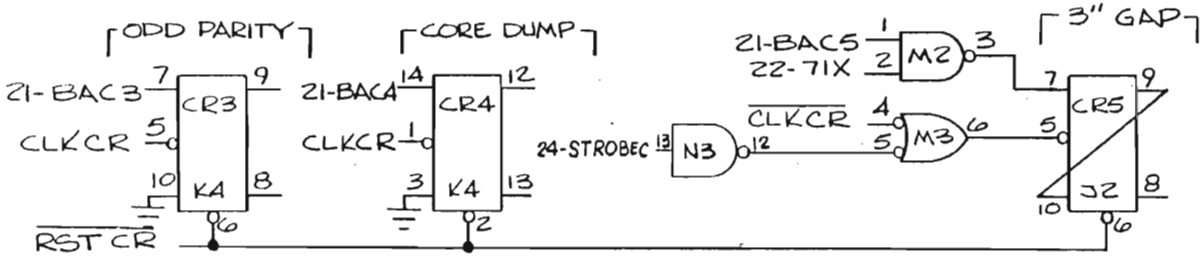


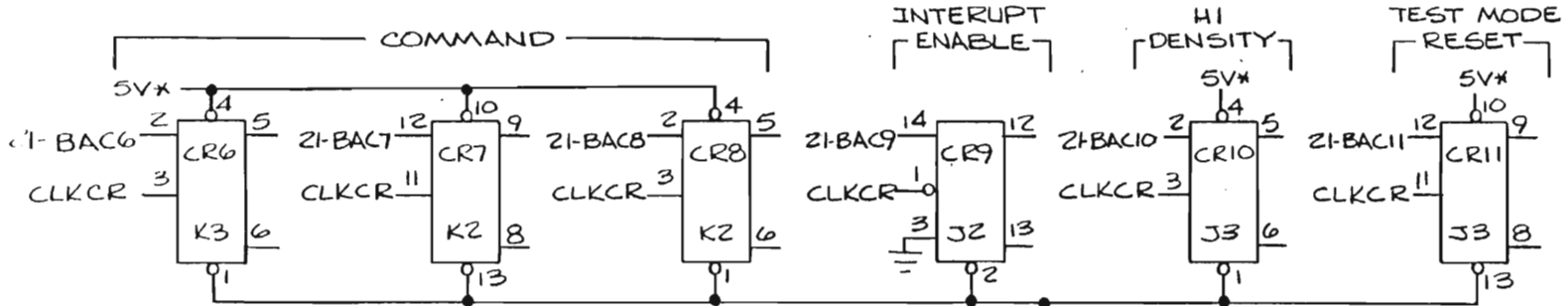
TAPE UNIT SELECTS

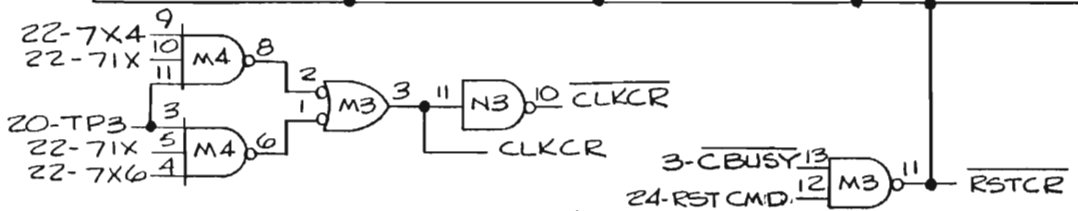


COMMAND DECODER









COMMAND REGISTER CLOCK
(6714 OR 6716)

(23)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

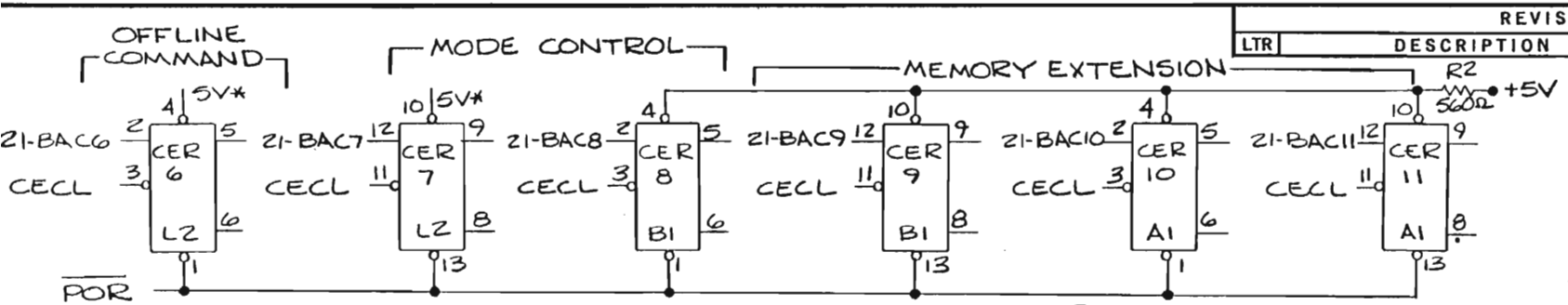
TITLE
P8e CONTROLLER
DATA BREAK

DWN LWS	12/3/71	DES	
CHK		ENGR	
SCALE NONE		FSC 31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

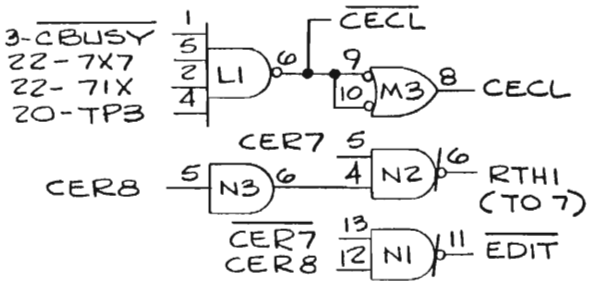
SIZE		REV
B	76225	C
	SHT 5 OF 8	

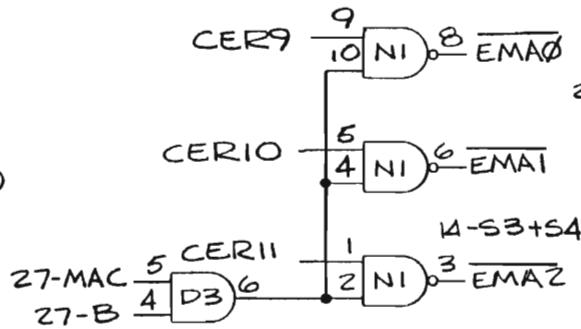
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



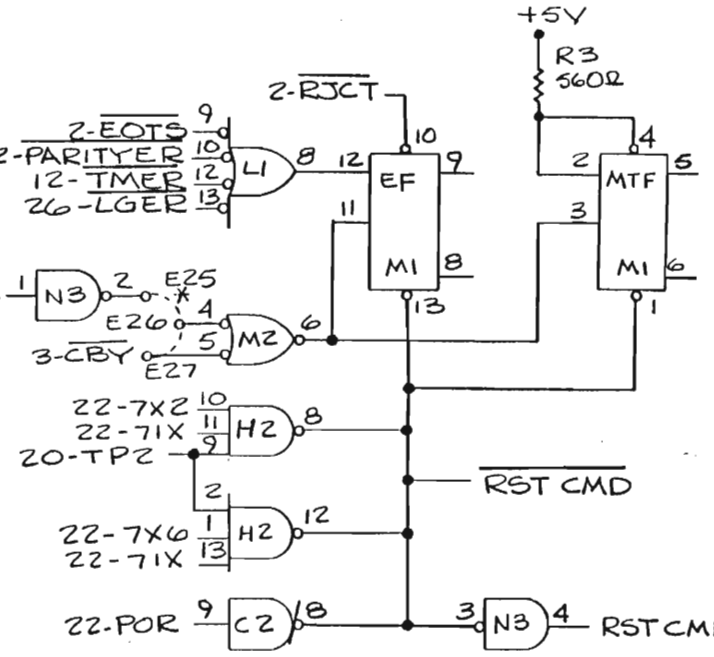
4K CORE ADDRESSED	CER 9	CER 10	CER 11
0-4	0	0	0
4-8	0	0	1
8-12	0	1	0
12-16	0	1	1
16-20	1	0	0
20-24	1	0	1
24-28	1	1	0
28-32	1	1	1

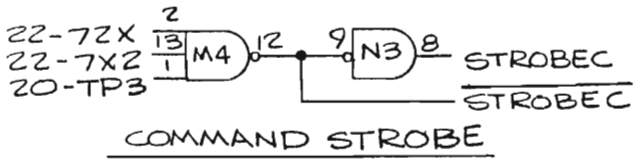
CONTROL EXTENSION REGISTER





MEMORY EXTENSION DRIVERS





COMMAND STROBE

(24)

1. * JUMPER E26 TO E27 FOR INTERUPT AT THE END OF CBUSY ONLY; OR JUMPER E26 TO E25 FOR INTERUPT AT END OF CBUSY AND END OF DATA CYCLE.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03 XXX ±.010 ANGLES ±1/2°

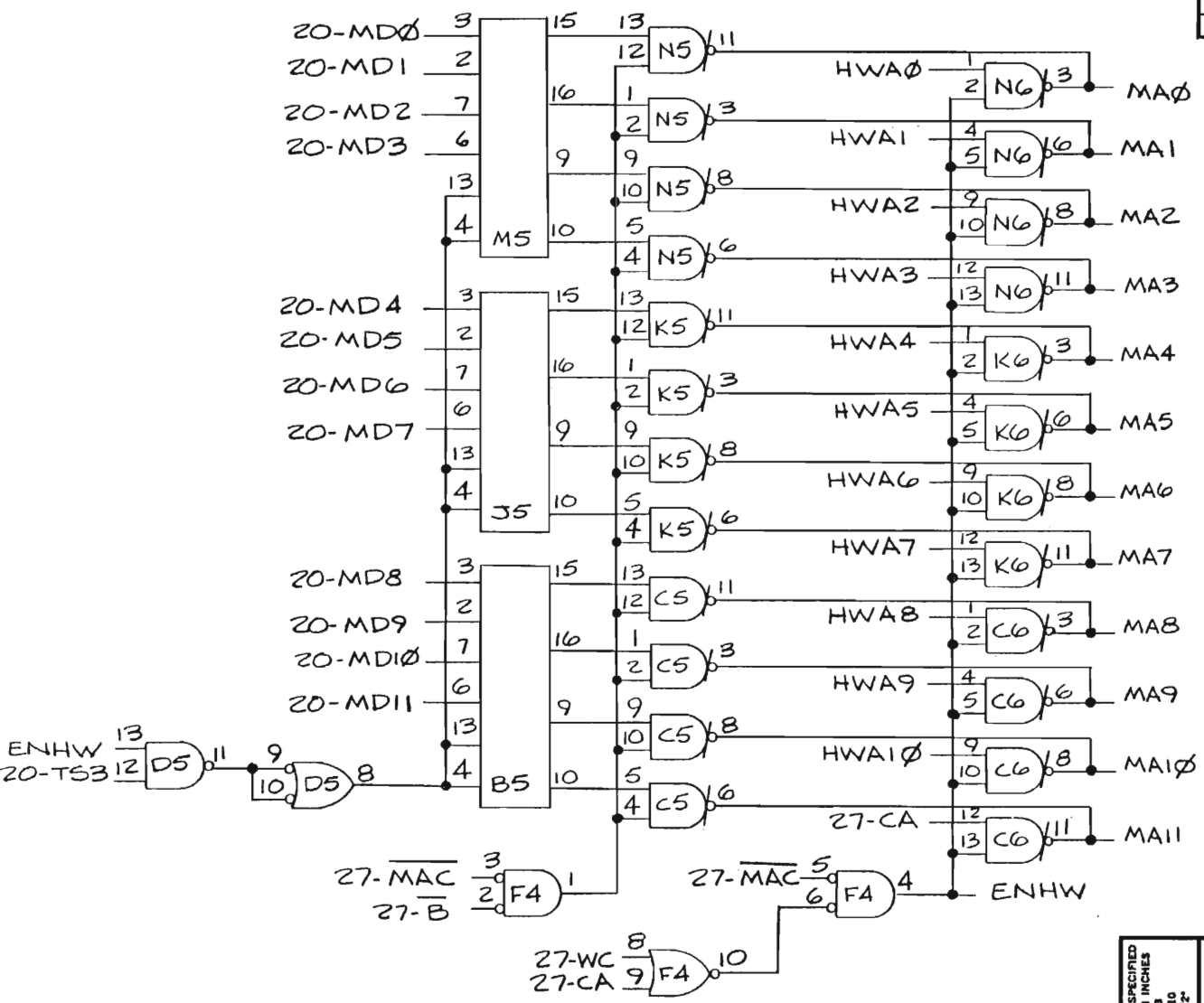
TITLE: P8e CONTROLLER BREAK DATA

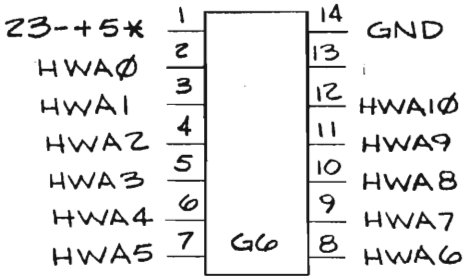
DWN Cows 12/10/71 | DES | CHK | ENGR | SCALE NONE | FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 76225 | C

SIZE | SHT 6 OF 8 | REV





* SELECT DESIRABLE ADDRESS WIRING ALL ADDRESSES "1" BITS TO 5V PULL UP (CURRENT ADDRESS) AND ALL "0" BITS TO GND

25b

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: P8e CONTROLLER BREAK DATA

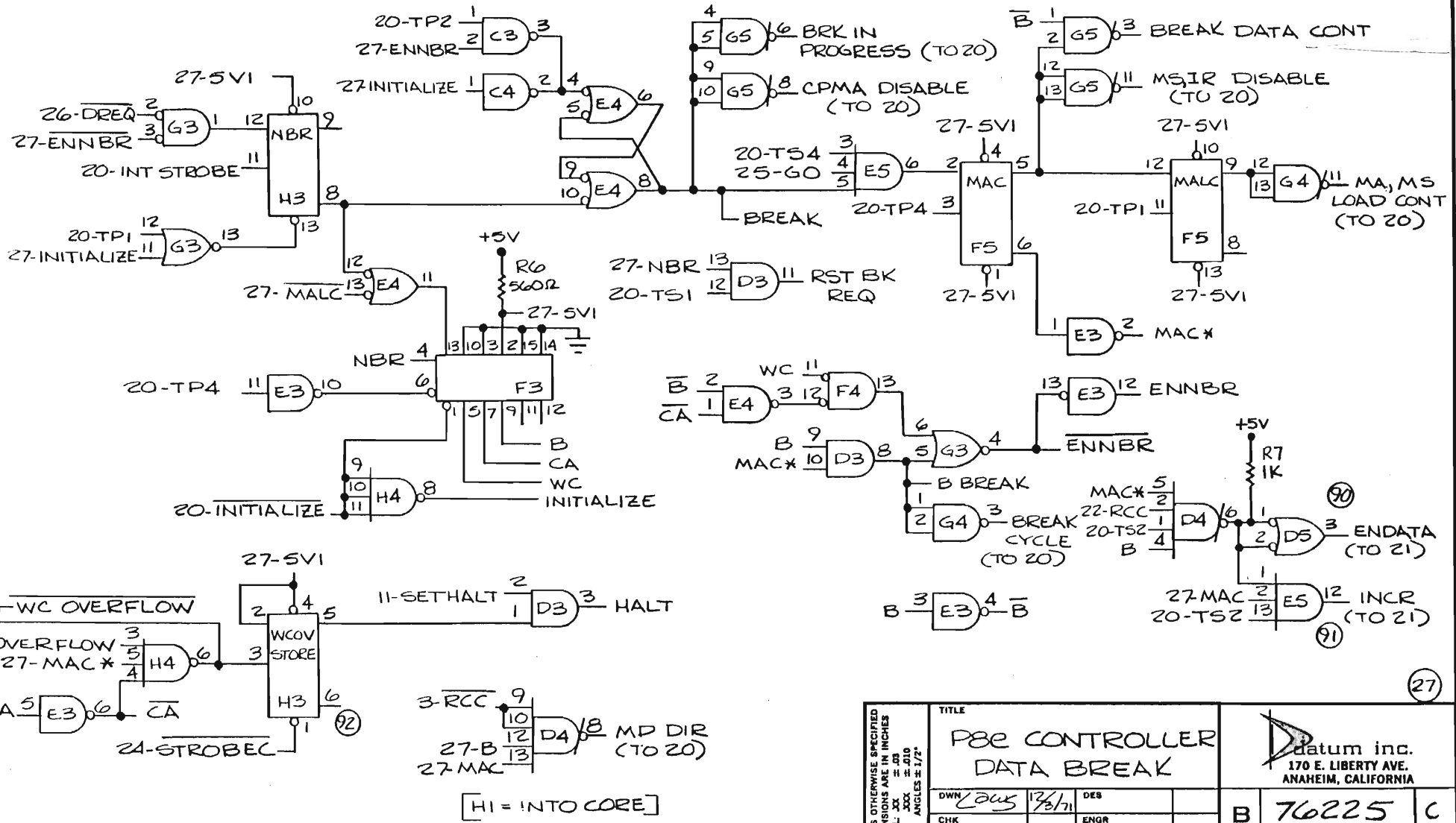
DWN Cows 12/10/71 | DES | CHK | ENGR | SCALE NONE | FSC 31160

datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA

B | 76225 | C

SIZE | SHT 7 OF 8 | REV

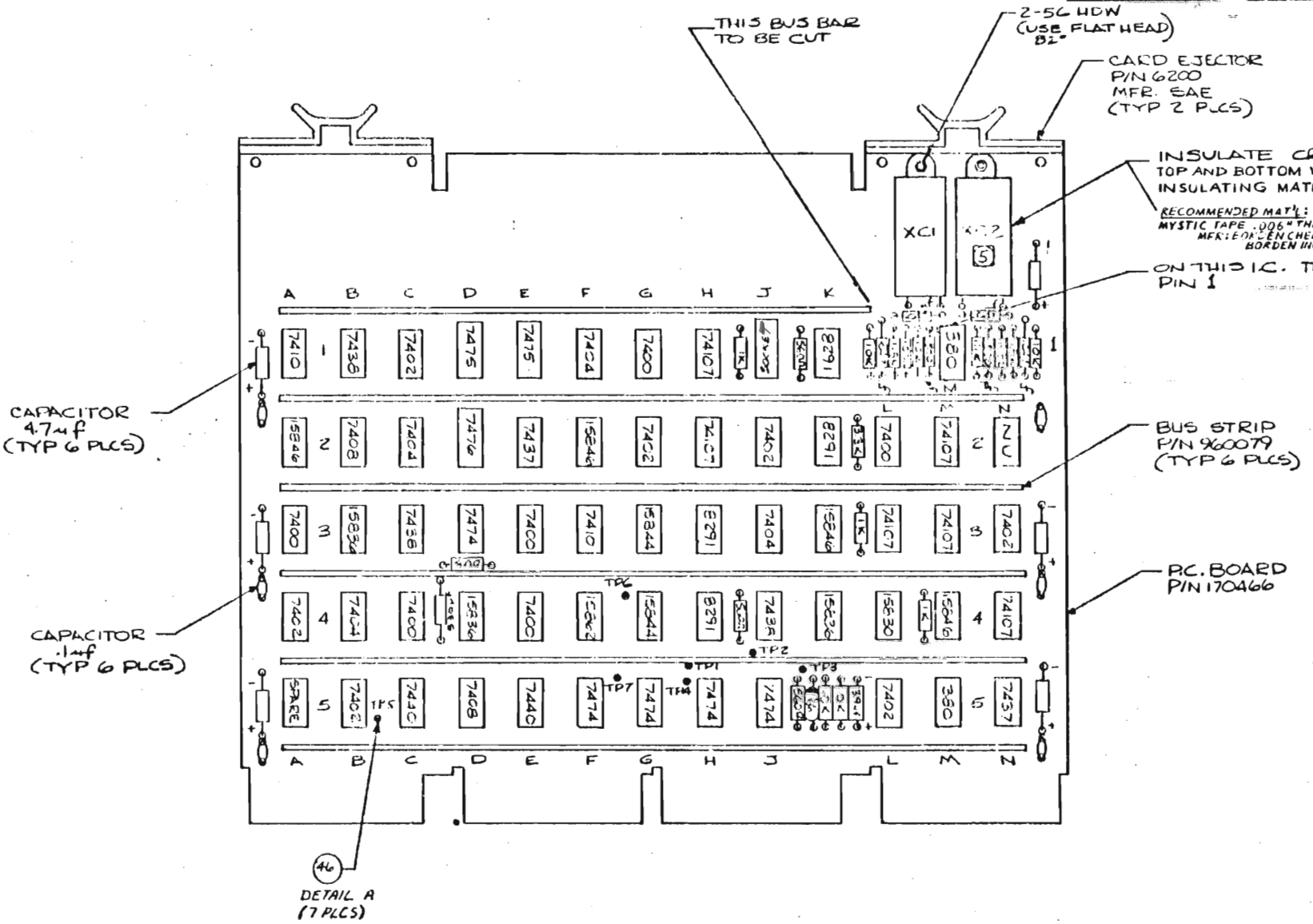
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

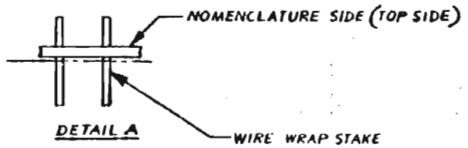


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°	TITLE: P8E CONTROLLER DATA BREAK	datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA
	DWN Lacy 12/3/71 DES	B 76225 C
	CHK ENGR	
	SCALE NONE FSC 31160	SIZE SHT 8 OF 8 REV

LTR	DESCRIPTION	DATE	APPROVED
D	ASSY. NOTE MODIFIED C.O. 308	8-15-73	
E	ADDED NOTE #3 CO 575	1-11-74	
F	DELETED PER C.O. 1391-16 CREATED -2 ASSY & NOTE 4	11-19-74	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	555 CIRCUIT CHANGED	4-5-72	
B	REVISED CHANGE A_S	3-2-73	
C	ADDED NOTE 1 FOR DETAIL A C.O. 0063	5-4-73	





DETAIL A

[5] USED FOR 7 TRACK 1/2" TAPES ONLY. (76227-2).

3. MAXIMUM BOARD CONFIGURATION SHOWN

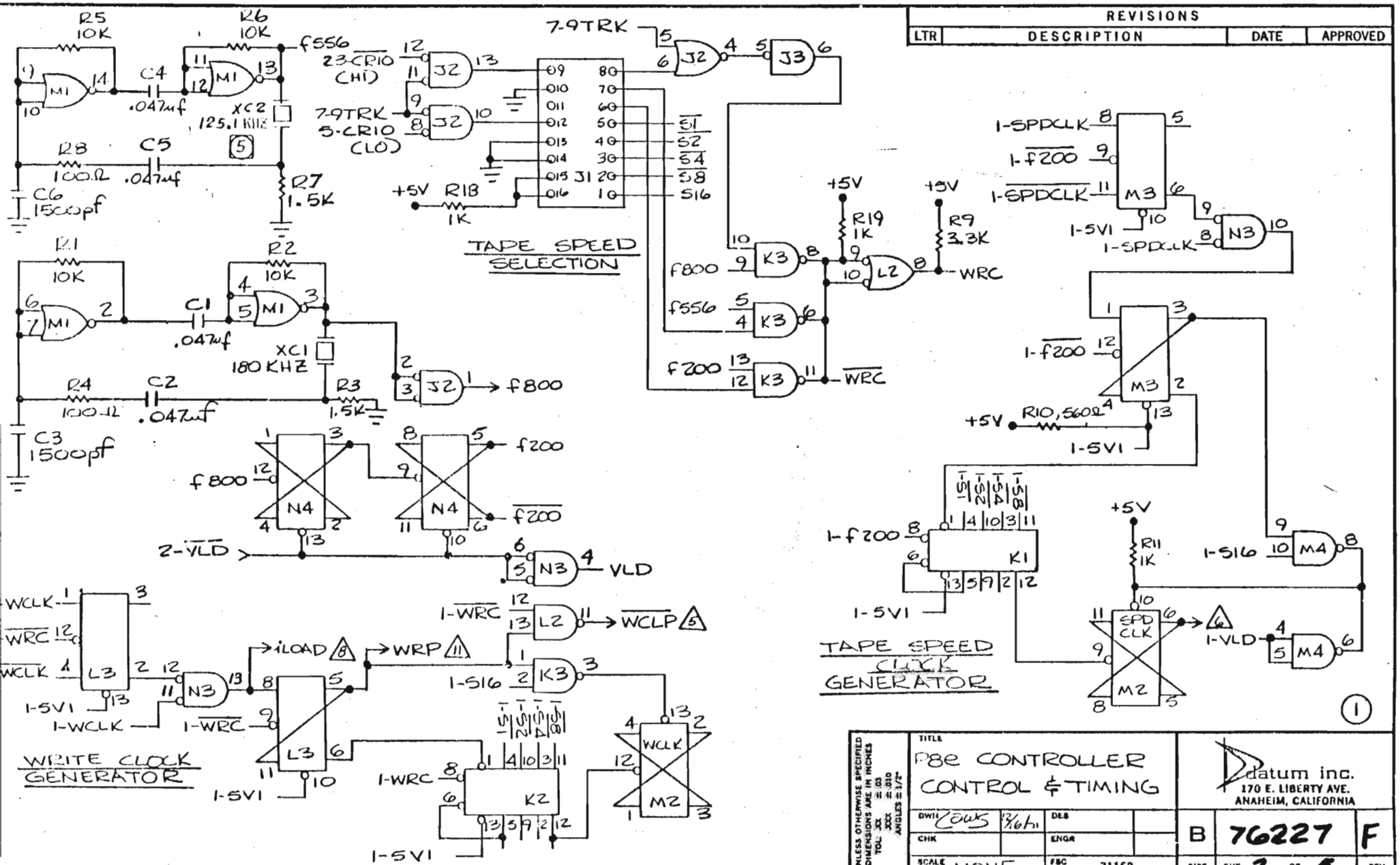
4 DO NOT SOLDER IN THE RIGHT HAND LEAD (TO MI-03) OF THE CRYSTAL

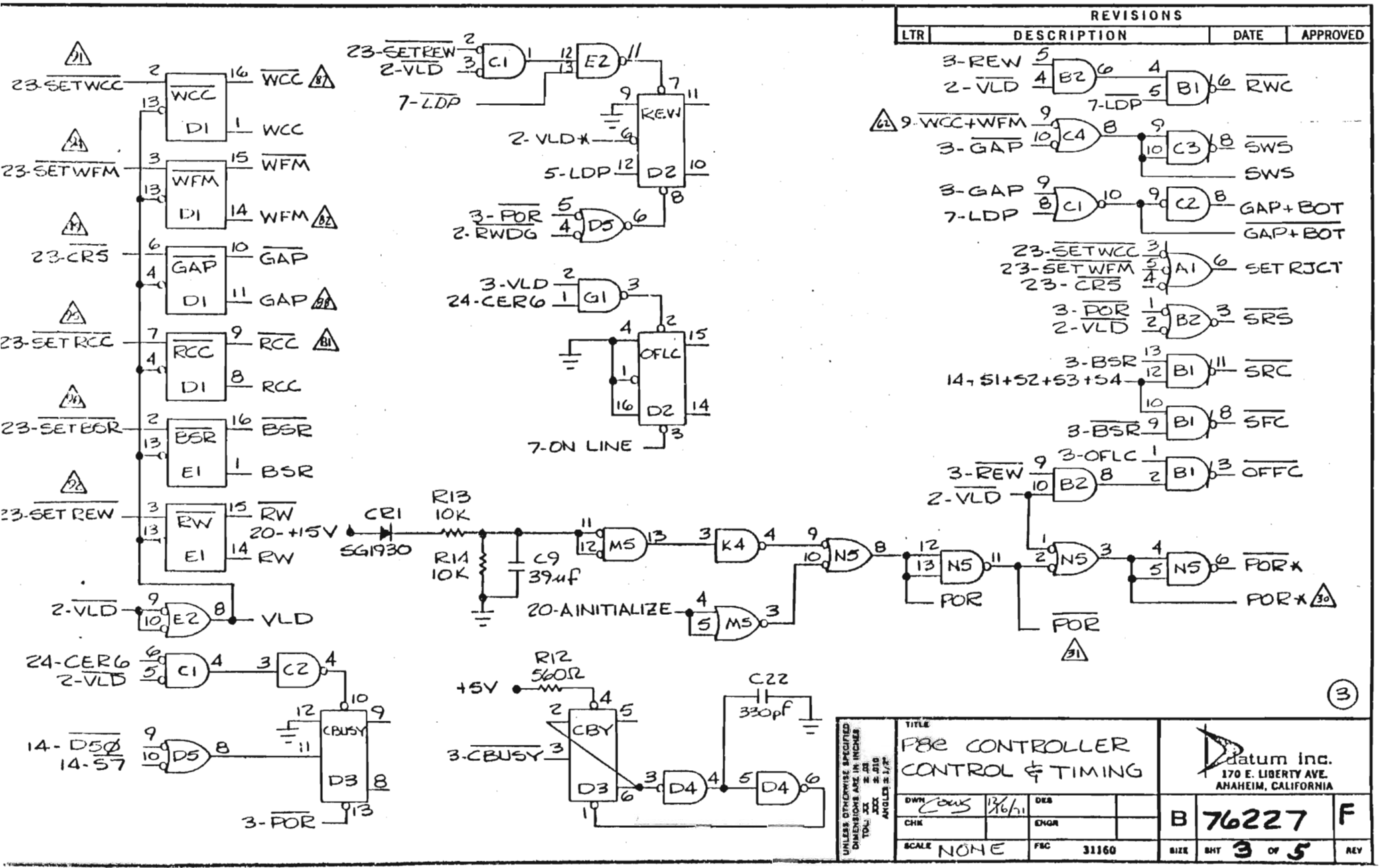
2. REF. 80215H SIGNAL LIST INTERCONNECTED TO ASSY. 76258.

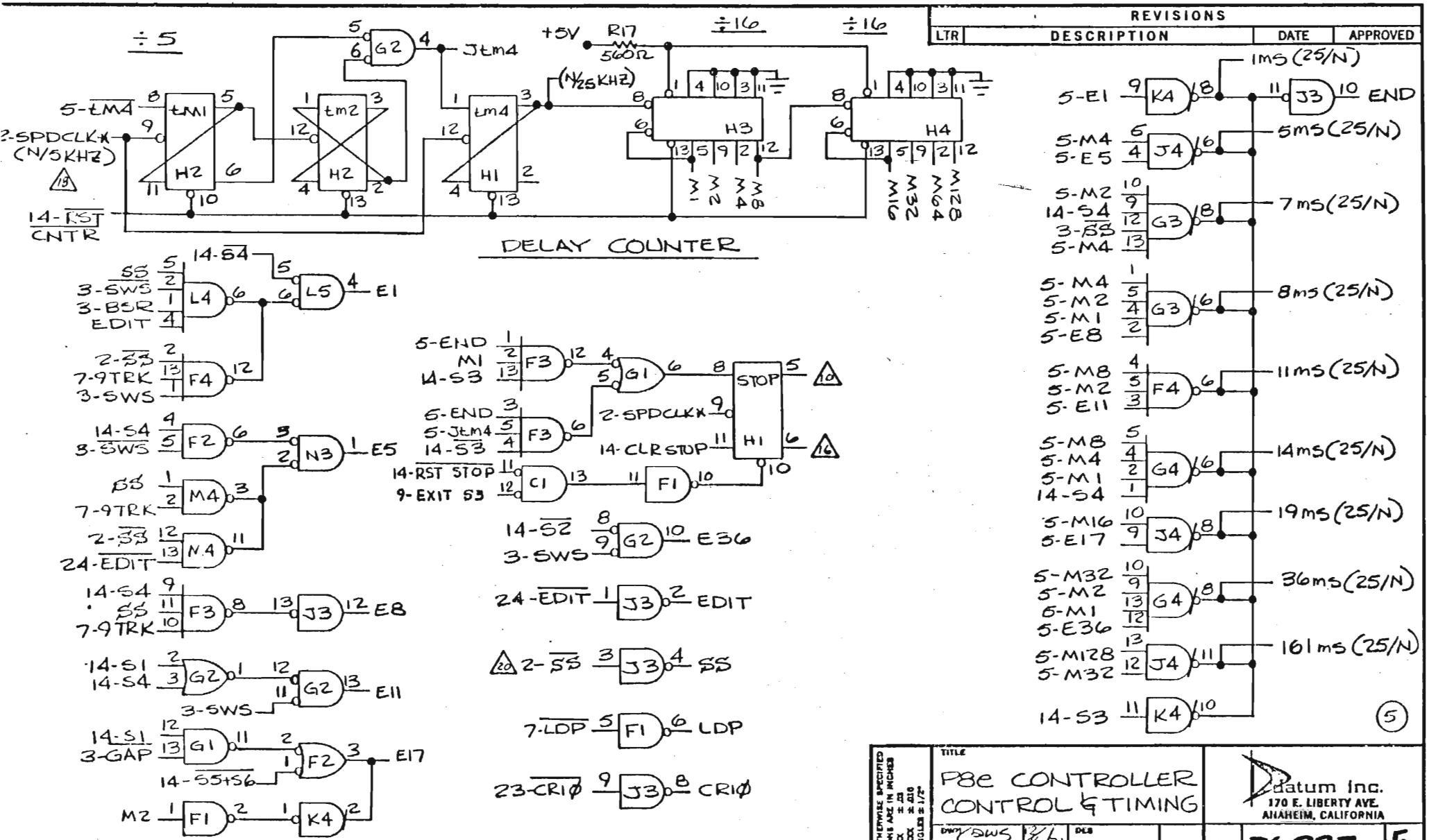
1. ● DENOTES WIRE WRAP PINS

NOTES: UNLESS OTHERWISE SPECIFIED

TITLE	P8C CONTROLLER CONTROL & TIMING	datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
DWN Lewis	DES Lod	C	76227 F
CHK	ENGR		
SCALE FULL	FSC 31160	SIZE	SHT 1 OF 5 REV

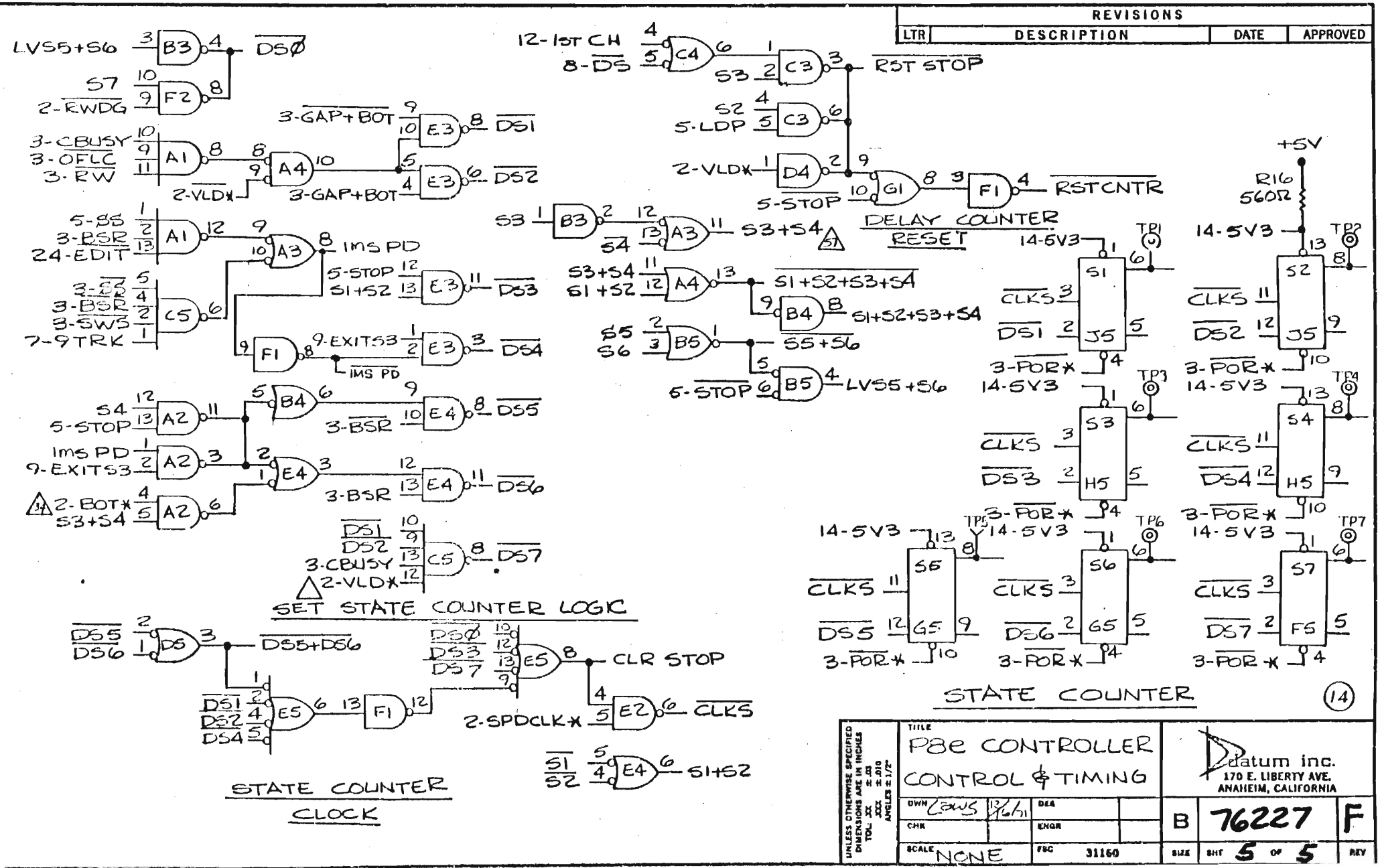

R5 10K
R6 10K
C4 .047uf
XC2 125.1 KHZ
R8 100Ω
C5 .047uf
C6 1500pf
R7 1.5K
f556
23-CR10 (CHI)
7-9TRK 5-CR10 (CLO)
+5V R18 1K
7-9TRK
TAPE SPEED SELECTION
R19 1K
R9 3.3K
f800
f556
f200
WRC
R1 10K
R2 10K
C1 .047uf
XC1 180 KHZ
R4 100Ω
C2 .047uf
R3 1.5K
C3 1500pf
f800
f200
2-VLD
VLD
WCLK
WRC
1-WRC
WCLP
iLOAD
WRP
1-516
1-WCLK
1-5V1
WRITE CLOCK GENERATOR
1-SPDCLK
1-f200
1-SPDCLK
1-5V1
R10, 560Ω
1-f200
1-5V1
TAPE SPEED CLOCK GENERATOR
R11 1K
1-516
1-VLD
REVISIONS
LTR DESCRIPTION DATE APPROVED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
TITLE
P8e CONTROLLER CONTROL & TIMING
DWN Louis 12/16/71
CHK
DES
ENGR
SCALE NONE
FSC 31160
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B 76227 F
SIZE
SHT 2 OF 5
REV


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
23-SETWCC
WCC
D1
WCC
23-SETWFM
WFM
D1
WFM
23-CRS
GAP
D1
GAP
23-SETRCC
RCC
D1
RCC
23-SETBSR
BSR
E1
BSR
23-SETREW
RW
E1
RW
2-VLD
E2
VLD
24-CER6
2-VLD
C1
C2
14-D5Ø
14-S7
D5
CBUSY
D3
3-POR
23-SETREW
2-VLD
C1
E2
7-LDP
REW
D2
2-VLD*
5-LDP
3-POR
2-RWDG
D5
3-VLD
24-CER6
G1
OFLC
D2
7-ON LINE
20-+15V
CR1
SG1930
R13
10K
R14
10K
C9
.39uf
M5
K4
N5
20-AINITIALIZE
M5
POR
N5
N5
N5
POR*
POR*
POR
R12
560Ω
+5V
C22
330pf
3-CBUSY
CBY
D3
D4
D4
3-REW
2-VLD
B2
B1
RWC
7-LDP
9-WCC+WFM
3-GAP
C4
C3
SWS
SWS
3-GAP
7-LDP
C1
C2
GAP+BOT
GAP+BOT
23-SETWCC
23-SETWFM
23-CRS
A1
SET RJCT
3-POR
2-VLD
B2
SRS
3-BSR
14-S1+S2+S3+S4
B1
SRC
3-BSR
B1
SFC
3-OFLC
3-REW
2-VLD
B2
B1
OFFC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .010 .XXX ± .005 ANGLES ± 1/2°
TITLE
P8e CONTROLLER CONTROL & TIMING
DWN Cous 12/6/71
CHK
ENGR
SCALE NONE
FSC 31160
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B 76227 F
SIZE
SHT 3 OF 5
REV
3

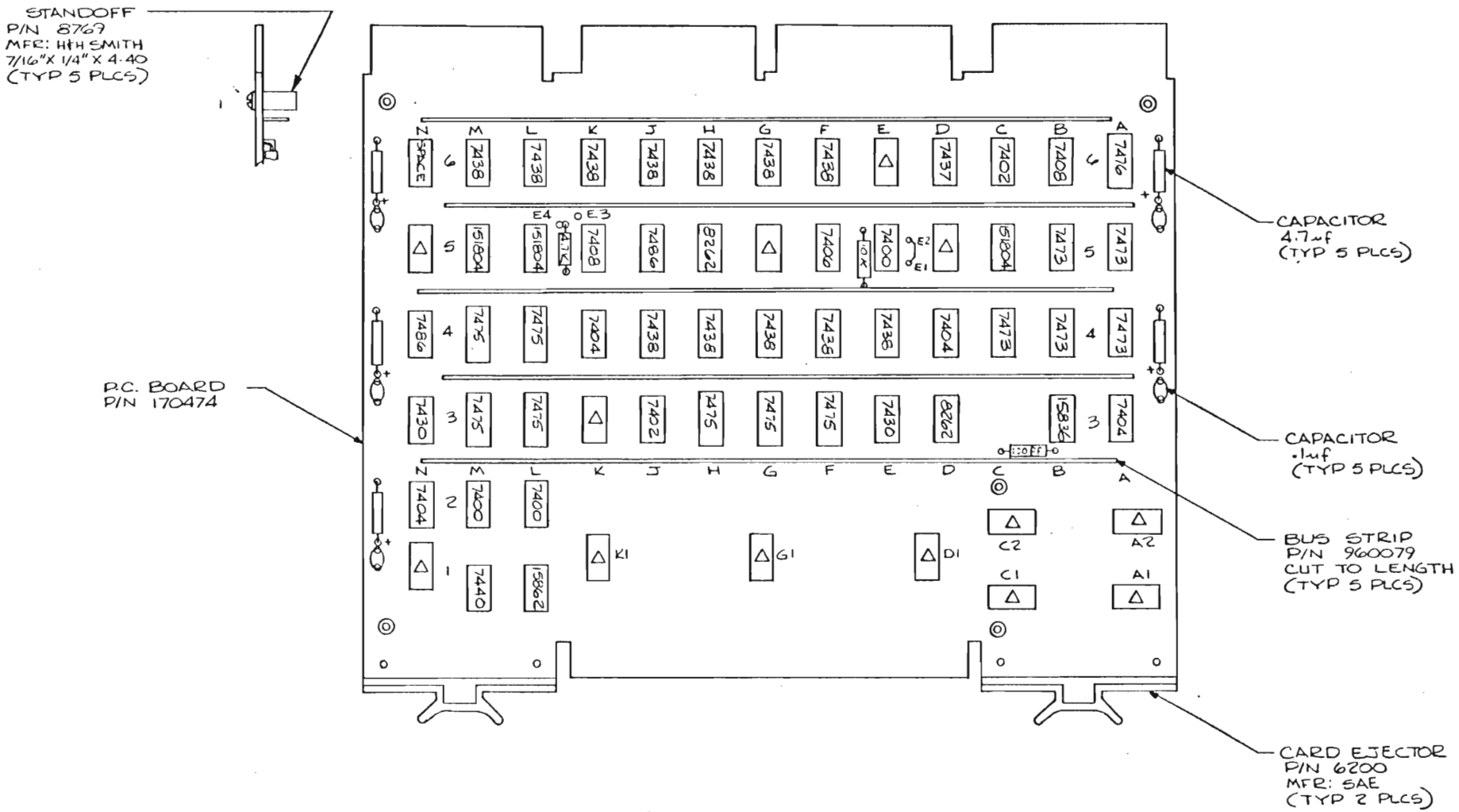


REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°	TITLE: P8e CONTROLLER CONTROL & TIMING	Datum Inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
DWN: ESWS 3/26/71	DES	B	76227 F
CHK	ENGR		
SCALE: NONE	FSC 31160	SIZE	SHT 4 OF 5 REV


REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
LVS5+S6
DSØ
S7
2-RWDG
3-CBUSY
3-OFLC
3-RW
2-VLDX
3-GAP+BOT
DS1
DS2
5-S5
3-BSR
24-EDIT
IMS PD
5-STOP
S1+S2
DS3
3-BSR
3-SWS
7-9TRK
9-EXITS3
DS4
S4
5-STOP
DS5
IMS PD
9-EXITS3
3-BSR
DS6
2-BOTX
S3+S4
DS1
DS2
3-CBUSY
2-VLDX
DS7
SET STATE COUNTER LOGIC
DS5
DS6
DS5+DS6
DSØ
DS3
DS7
CLR STOP
DS1
DS2
DS4
2-SPDCLKX
CLKS
S1
S2
S1+S2
STATE COUNTER
CLOCK
12-1ST CH
8-DS
RST STOP
S2
5-LDP
2-VLDX
5-STOP
RSTCNTR
DELAY COUNTER
RESET
S3
S4
S3+S4
S1+S2+S3+S4
S5
S6
S5+S6
6-STOP
LVS5+S6
+5V
R16
560Ω
14-5V3
TP1
TP2
TP3
TP4
TP5
TP6
TP7
CLKS
DS1
DS2
DS3
DS4
DS5
DS6
DS7
3-PORX
S1
S2
S3
S4
S5
S6
S7
J5
H5
G5
F5
STATE COUNTER
14
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ±.03
XXX ±.010
ANGLES ±1/2°
TITLE
P8e CONTROLLER
CONTROL & TIMING
DWN Lewis 12/16/71
DES
CHK
ENGR
SCALE NONE
FSC 31160
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B
76227
F
SIZE
SHT 5 OF 5
REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
B	REV. PER C.O. 324 - CHGD POS. OF STANDOFF IN SIDE VIEW	12-5-73	
C	REV. PER C.O. 1458	5-17-74	



4. CUT SOCKET PINS (ITEM27) A MAX OF .06 FROM SOLDER SIDE OF BOARD.
3. REF. B02158 SIGNAL LIST INTERCONNECTED TO ASSY 76258.
2 △ DENOTES 14 PIN I.C. SOCKET (SEE NOTE 4)
1. ALL RESISTORS ARE 1/4 W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

5-12-73

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1°

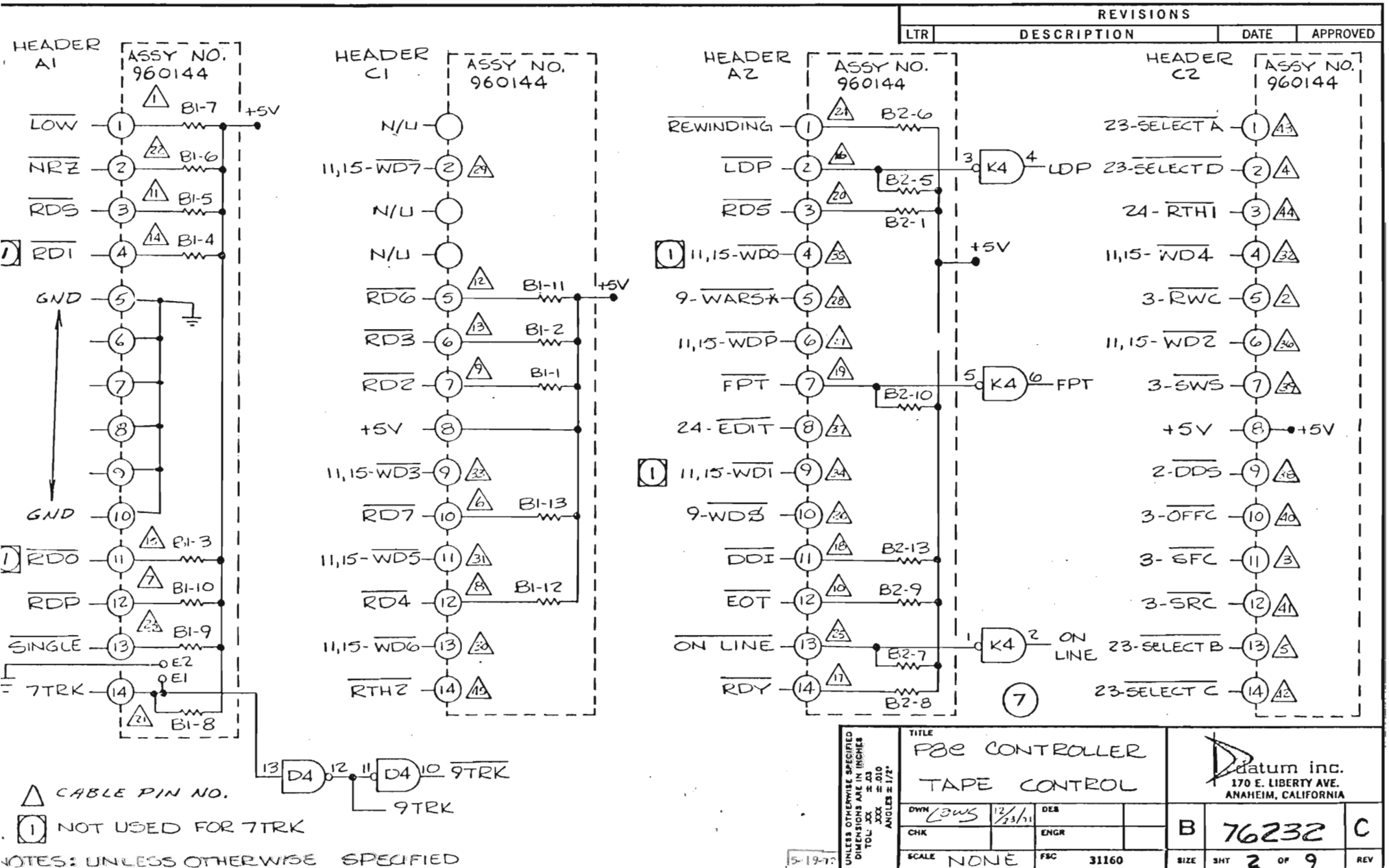
TITLE: TAPE CONTROL ASSY

DWN Cous 1/14/72 | DES | CHK | ENGR | SCALE NONE | FSC 31160

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

76232 C

SIZE | SHT 1 OF 9 | REV



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: F8E CONTROLLER TAPE CONTROL

DWN	CWS	12/23/71	DES	
CHK			ENGR	
SCALE	NONE	FSC	31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE	B	76232	REV C
SHT	2 OF 9		

5-19-72

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

D1	
PIN	TERM
1	RJCT
2	WCC + WFM
3	SET RJCT
4	B BREAK
5	HALT
6	WCC
7	RST BK REQ
8	GAP
9	REC RDY
10	EXT RJCT
11	SET FSR
12	SET BSR
13	RWDG
14	WFM

G1	
PIN	TERM
1	LGER
2	BSR
3	EXIT B3
4	FSR
5	TS3
6	1ST CH
7	S1+S2+S3+S4
8	DLLQ
9	RST CMD
10	VLD*
11	POR*
12	CR10
13	VLD*
14	DDS

K1	
PIN	TERM
1	S5
2	TMER
3	SPD CLK*
4	STOP
5	WCLP
6	SPD CLK
7	RST CMD
8	STOP
9	WRP
10	VLD
11	EOTS
12	SPD CLK
13	PARITYER
14	CR3

N1	
PIN	TERM
1	WRSTR*
2	WRSTR
3	RCC
4	+5V
5	DS*
6	RCAS
7	(FROM L1-6)
8	(FROM L1-8)
9	+5V
10	+5V
11	TMER
12	DATA FLAG
13	RC
14	(FROM N2-8)

K3	
PIN	TERM
1	EOTS
2	LDP
3	FPT
4	FM DET
5	FM DET
6	VPE
7	CR10
8	STROBE C
9	EOT*
10	CR3
11	LDP
12	REWINDING
13	WFMSB
14	FM

D5	
PIN	TERM
1	WRCLK
2	TRD
3	RCC
4	RJCT
5	S3
6	S2
7	GND
8	7 TRK
9	LER*
10	D2
11	D3
12	DCL
13	D3*
14	CR4

G5	
PIN	TERM
1	+5V
2	CR4
3	WDP
4	WD2
5	WD3
6	WD1
7	GND
8	WD0
9	WD4
10	WD5
11	WD6
12	WDCL
13	WD7
14	WCC

N5	
PIN	TERM
1	PARITER
2	REJECT
3	RWDG
4	CRC3
5	CR3
6	WCOV STORE
7	GND
8	GND
9	GND
10	CRC7
11	(FROM N4-3)
12	TRD + 9-CD
13	RST PRCD
14	+5V

E6	
PIN	TERM
1	FPT
2	GND
3	GND
4	GND
5	LGER
6	ALT FLAG
7	TMER
8	WARS*
9	RDY
10	+5V
11	+5V
12	ON LINE
13	EOT
14	WDS

REF HEADER LOCATION

5-197

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: P8e CONTROLLER TAPE CONTROL

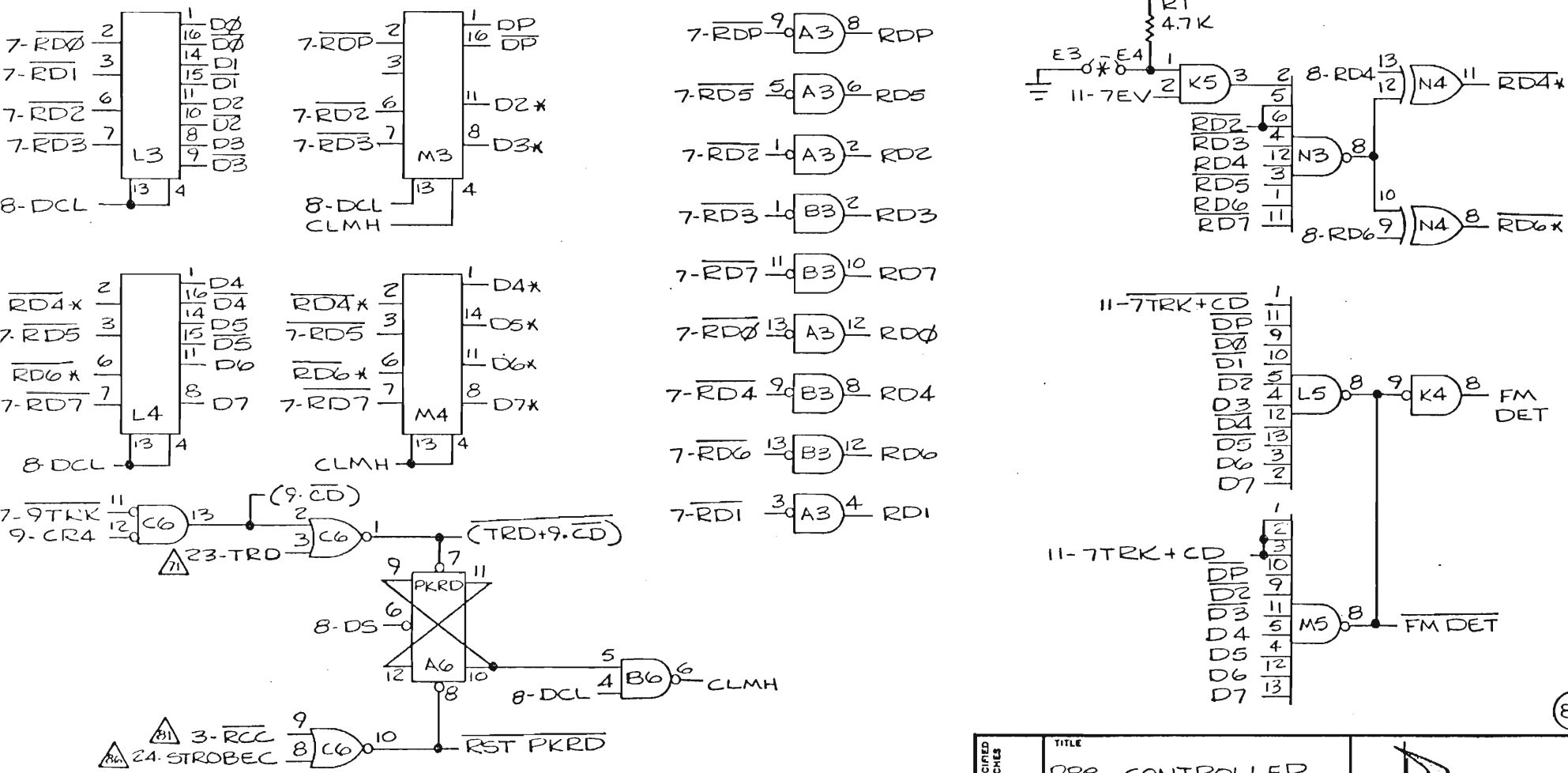
DWN Lows 12/27/11 | DES | CHK | ENGR | SCALE NONE | FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 76232 | C

SIZE | SHT 3 OF 9 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



1. * JUMPER TO DISABLE "12" TO Ø CONVERSION IN 7 TRACK BCD MODE

NOTES: UNLESS OTHERWISE SPECIFIED

5-1972

(8a)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: P8e CONTROLLER TAPE CONTROL

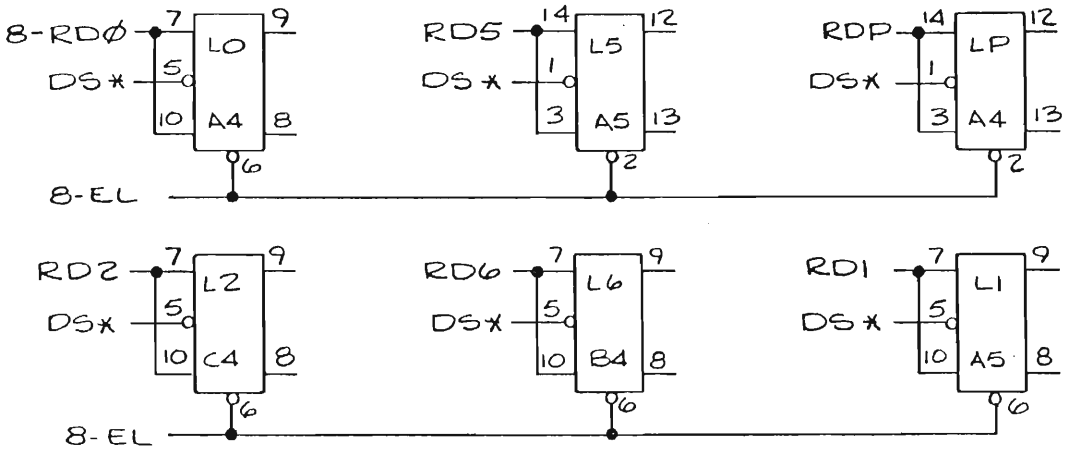
DWN EWS 12/21/71 | DES | CHK | ENGR | SCALE NONE | FSC 31160

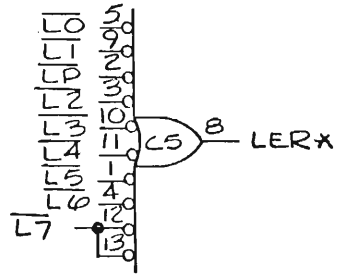
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

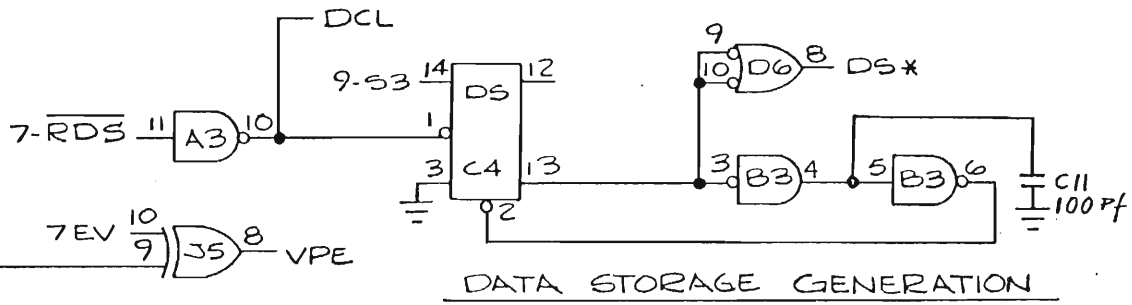
B | 76232 | C

SIZE | SHT 4 OF 9 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED







(8b)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

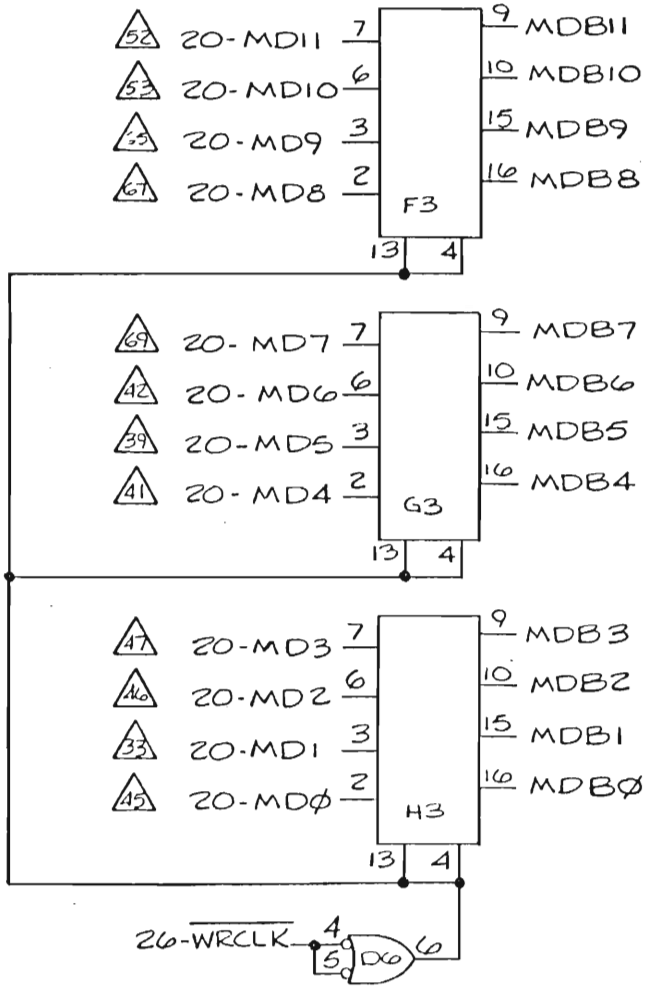
TITLE
P8e CONTROLLER
TAPE CONTROL

DWN Lows	1/4/72	DES		B	76232 C
CHK		ENGR			
SCALE NONE		FSC 31160		SIZE	SHT 5 OF 9 REV

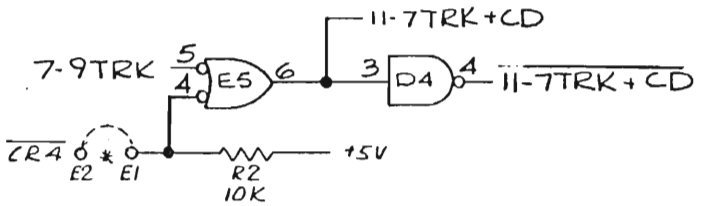
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

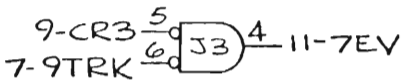
5-19-72

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



MEMORY DATA BUFFER





ODD/EVEN PARITY CONTROL

* JUMPER FOR 7TRK FM IN 9TRK CORE DUMP MODE

(11a)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

5-19-72

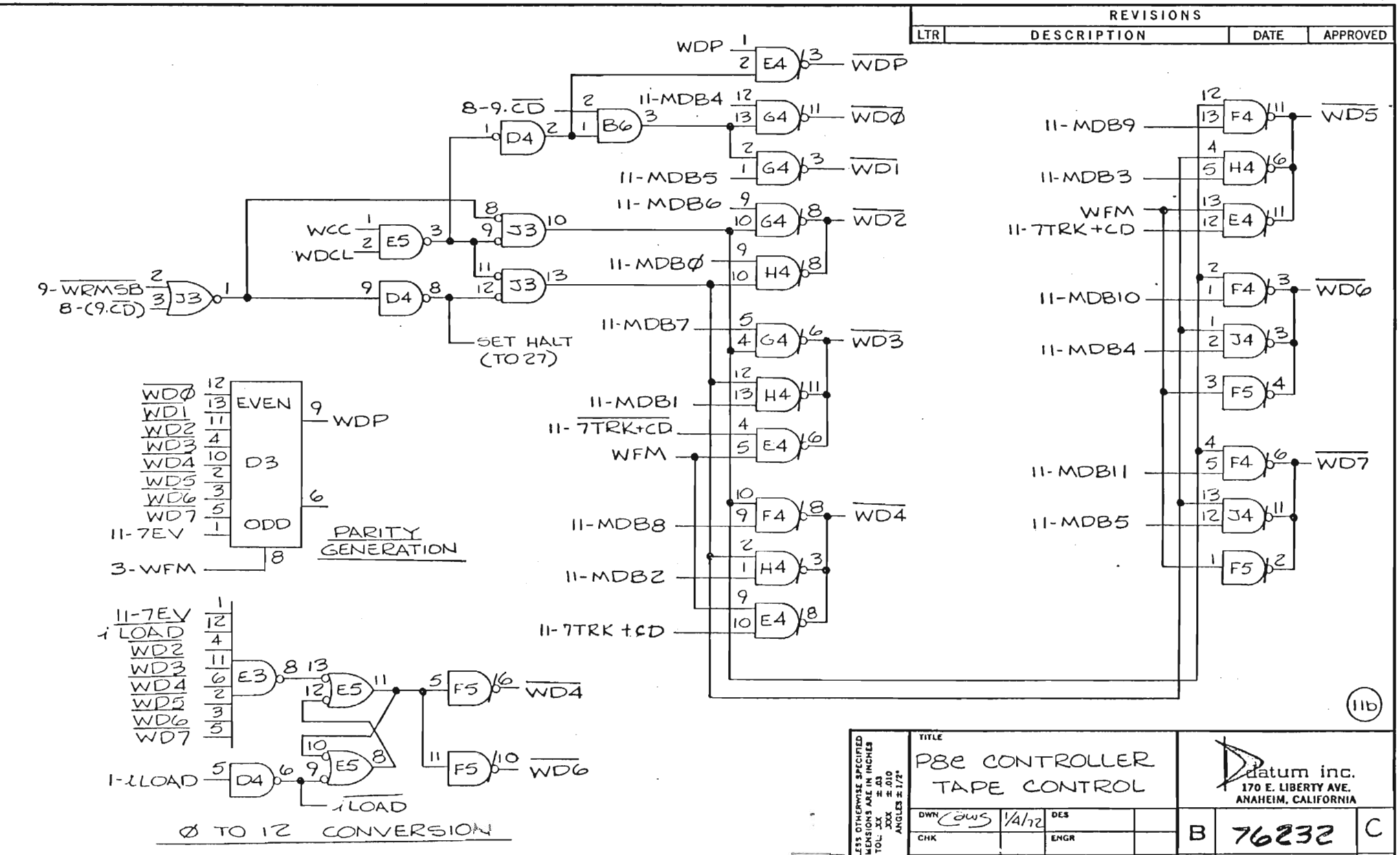
TITLE
P8e CONTROLLER
TAPE CONTROL

DWN Cows	7/21/72	DES	
CHK		ENGR	
SCALE NONE		FSC 31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

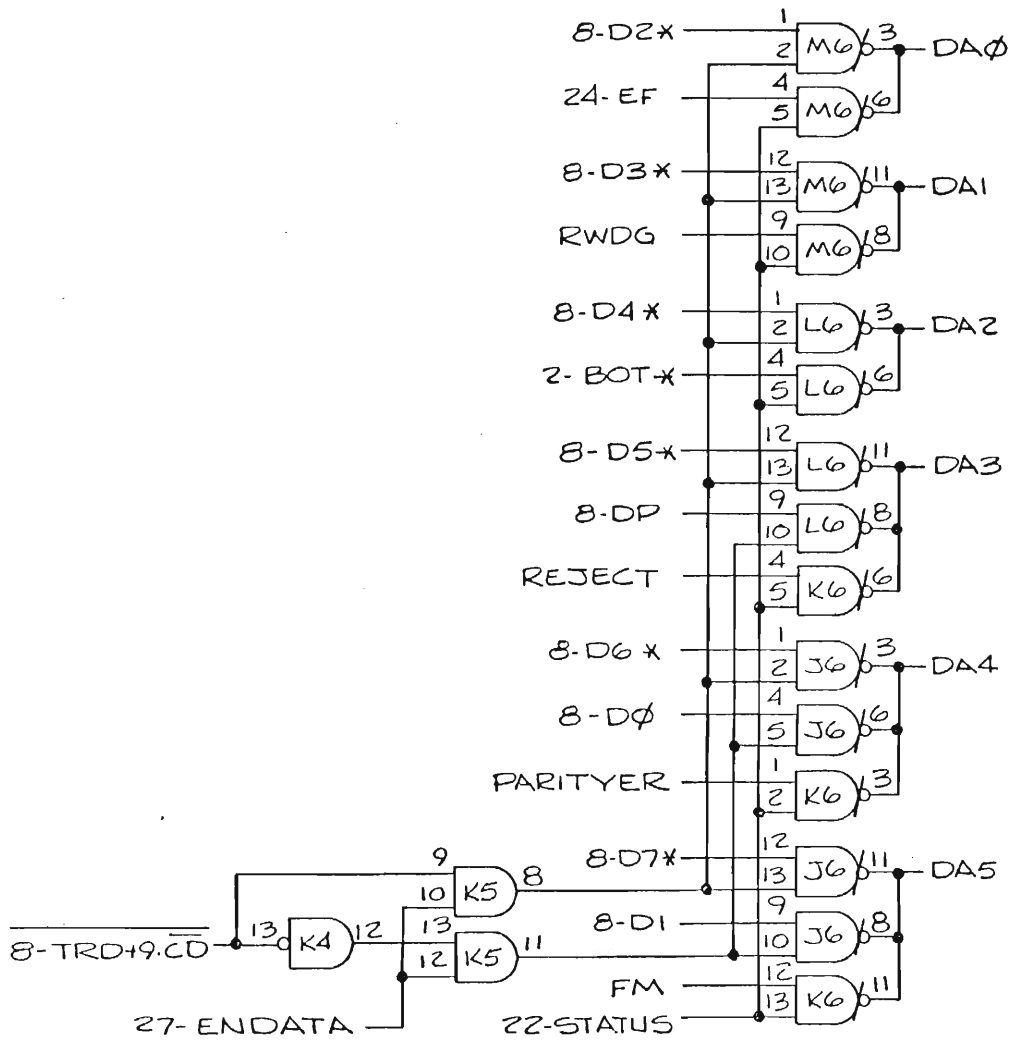
SIZE	SHT	REV
B	6 OF 9	C

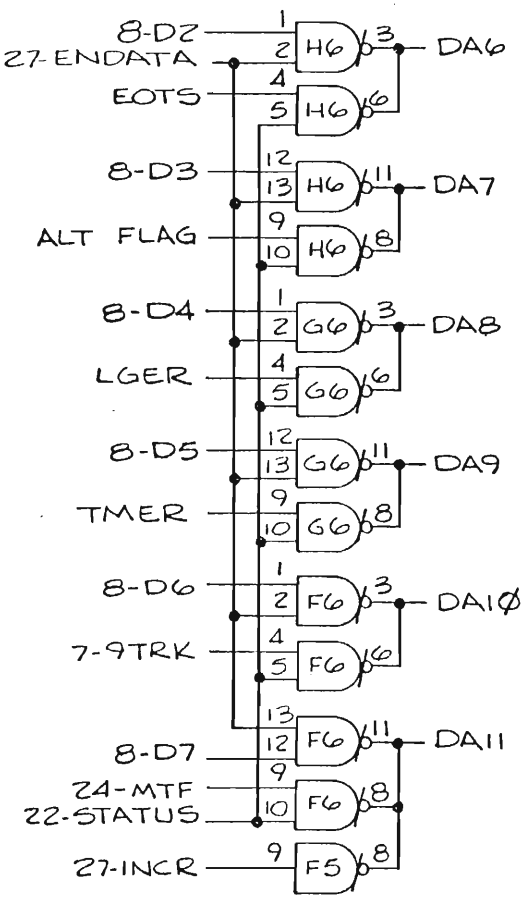
76232



1/GEN 196 MIS 10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





(21)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE
P8e CONTROLLER
TAPE CONTROL

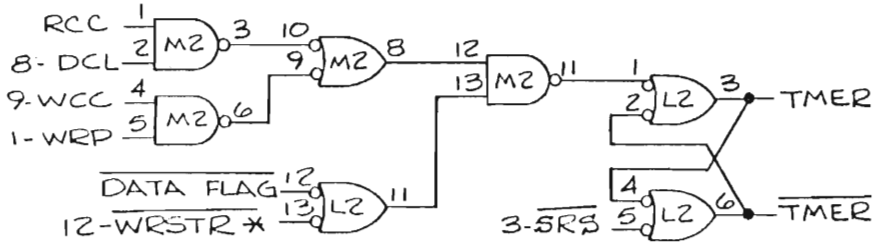
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	DES
Laws 1/4/72	
CHK	ENGR
SCALE NONE	FSC 31160

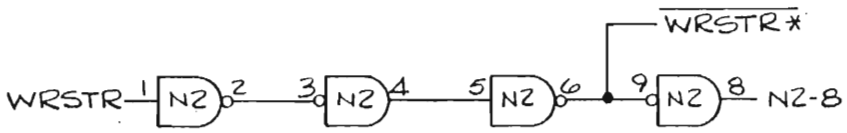
SIZE		REV
B	76232	C
	SHT 8 OF 9	

5-19-72

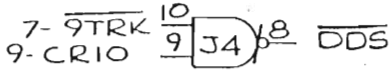
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

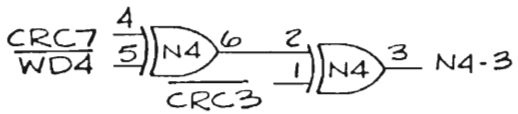


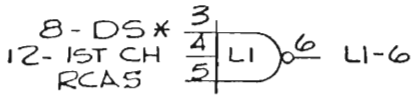
DATA TRANSFER TIMING
ERROR DETECT

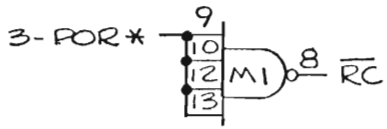


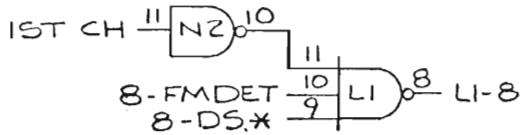
DATA TRANSFER REQUEST











REDRAWN FROM SCHEMATIC NO. 76233

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE
P8C CONTROLLER
TAPE CONTROL

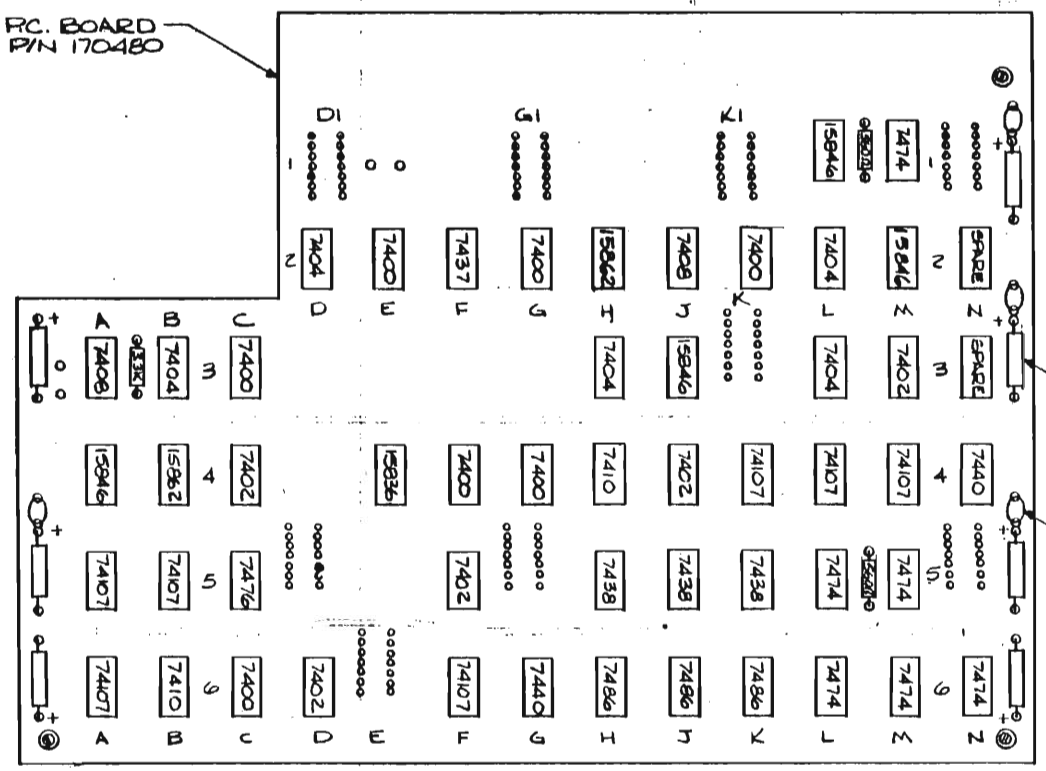
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

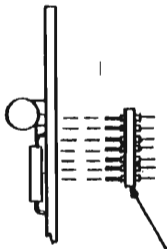
DWN	CWS	1/5/72	DES			
CHK			ENGR		B	76232 C
SCALE	NONE		FSC	31160	SIZE	SHT 9 OF 9 REV

5-19-

GEN 196 MG-10

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
B	BUS STRIP REMOVED, SEE C/O 214	6-29-73	JB
C	REVISED PER C.O. 0410	12-5-73	J.B.





CAPACITOR
4.7uf
(TYP 7 PLCS)

CAPACITOR
.1uf
(TYP 4 PLCS)

1. ALL RESISTORS ARE 1/4 W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

TITLE: DATA TRANSFER CONTROL ASSY		Datum Inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
DWN: CWS 12/31/73	DES		76233 C
CHK	ENGR		
SCALE: FULL	FSC 31160	SIZE	SHT 1 OF 7 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

D1	
PIN	TERM
1	RJCT
2	WCC + WFM
3	SET RJCT
4	B BREAK
5	HALT
6	WCC
7	RST BK REQ
8	GAP
9	REC RDY
10	TXT RJCT
11	SET FSR
12	SET PSR
13	RWDG
14	WFM.

G1	
PIN	TERM
1	LGER
2	PER
3	EXIT B3
4	FOR
5	T03
6	IST CH
7	S1+S2+S3+S4
8	CREQ
9	RST CMD
10	VLD*
11	POR* (N/U)
12	CR10
13	VLD*
14	DDS (N/U)

K1	
PIN	TERM
1	SS
2	TMER (N/U)
3	SPD CLK*
4	STOP
5	WCLP
6	SPD CLK
7	RST CMD
8	STOP
9	WRP (N/U)
10	VLD
11	EOT5
12	SPD CLK
13	PARITYER
14	CR3

N1	
PIN	TERM
1	WRSTR* (N/U)
2	WRSTR
3	RCC
4	+5V
5	DS*
6	RCAS
7	(FROM L1-6)
8	(FROM L1-8)
9	+5V
10	+5V
11	TMER
12	DATA FLAG
13	RC
14	(FROM N2-8)

K3	
PIN	TERM
1	EOT3
2	LDP
3	FPT
4	FM DET (N/U)
5	FM DET
6	VPE
7	CR10
8	STROBE C
9	EOT*
10	CR3
11	LDP (N/U)
12	REWINDING
13	WRMBB
14	FM

D5	
PIN	TERM
1	WRCLK
2	TRD
3	RCC
4	FLG
5	S3
6	S3
7	GND
8	TRK
9	LER*
10	DB
11	DB
12	FCL (N/U)
13	DB*
14	CR4

G5	
PIN	TERM
1	+5V
2	CR4
3	WDP
4	WD2
5	WD3
6	WD1
7	GND
8	WD8
9	WD4
10	WD5
11	WD6
12	WDCL
13	WD7
14	WCC

N5	
PIN	TERM
1	PARITER
2	REJECT
3	RWDG
4	CRC3
5	CR3
6	WCOV STORE
7	GND
8	GND
9	GND
10	CRC7
11	(FROM N4-3)
12	TRD+2-CD
13	RST PKRD
14	+5V

E6	
PIN	TERM
1	FPT (N/U)
2	GND
3	GND
4	GND
5	LGER
6	ALT FLAG
7	TMER
8	WAR3*
9	RDY
10	+5V
11	+5V
12	ON LINE
13	EOT
14	WD8

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ± .02, XXX ± .010, ANGLES ± 1/2°

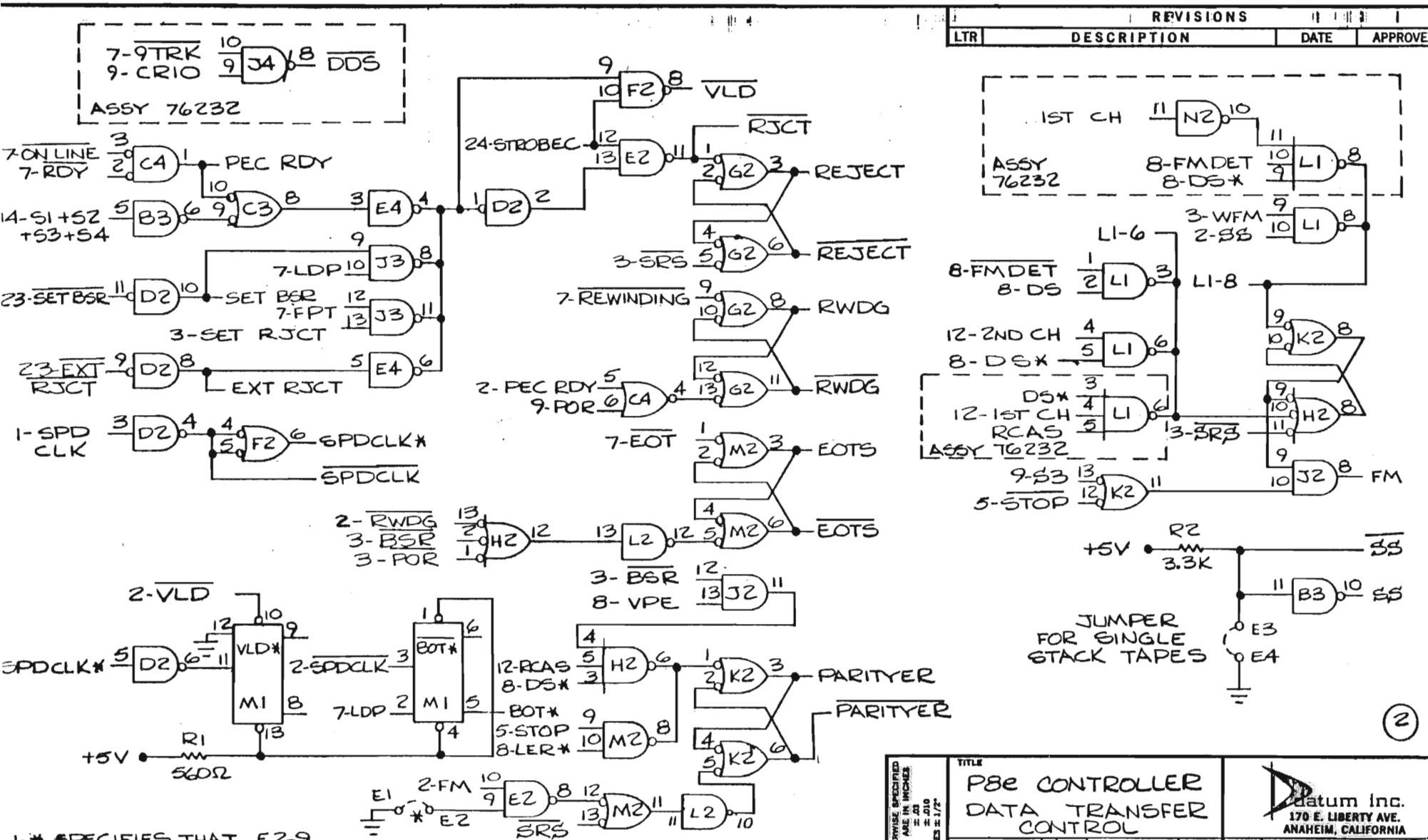
TITLE
P8e CONTROLLER DATA TRANSFER CONTROL

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	DATE	DES	
CHK		ENGR	
SCALE NONE		PSC 31160	

B | 76233 | C

SIZE | SHT 2 OF 7 | REV



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

1. * SPECIFIES THAT E2-9 MAY BE GROUNDED TO INHIBIT BLANKING OF VPE FOR FILEMARKS.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03, XXX ± .010, ANGLES ± 1/2°

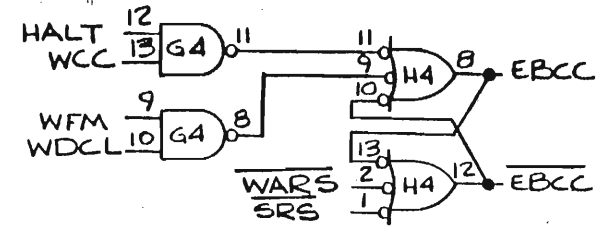
TITLE	P8e CONTROLLER DATA TRANSFER CONTROL		
DWN Laws 1/18/11	DES		
CHK	ENGR		
SCALE NONE	FSC 31160		

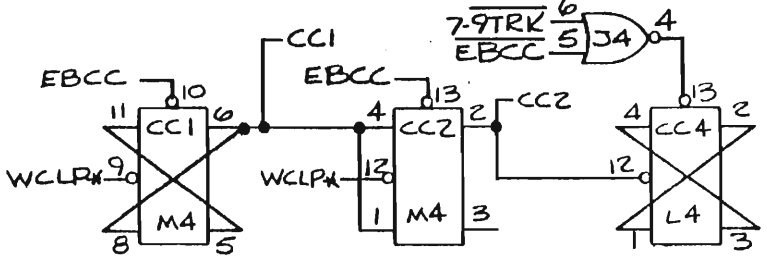
Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B	76233	C
SIZE	SHT 3 OF 7	REV

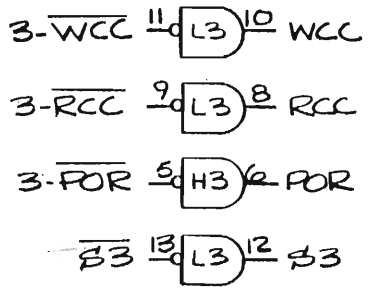
(2)

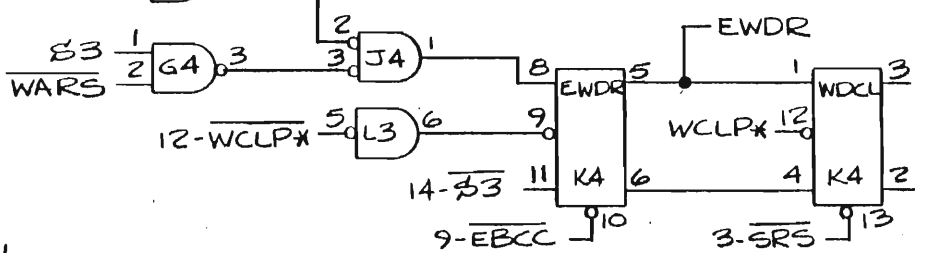
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

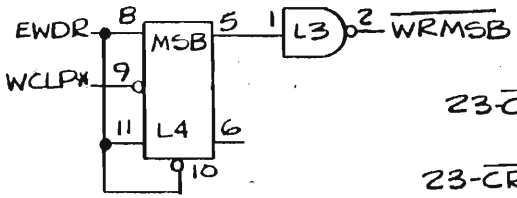




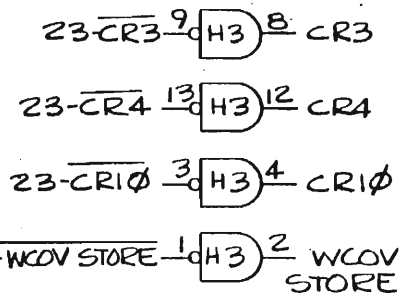
BLANK CHAR. COUNTER

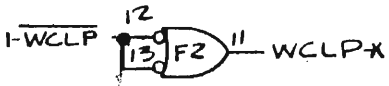


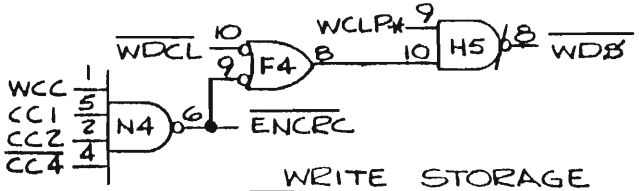




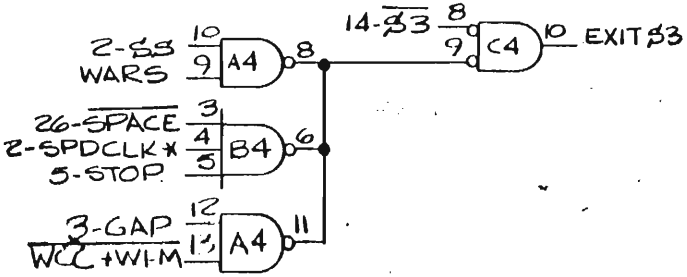
WRITE CONTROL LOGIC



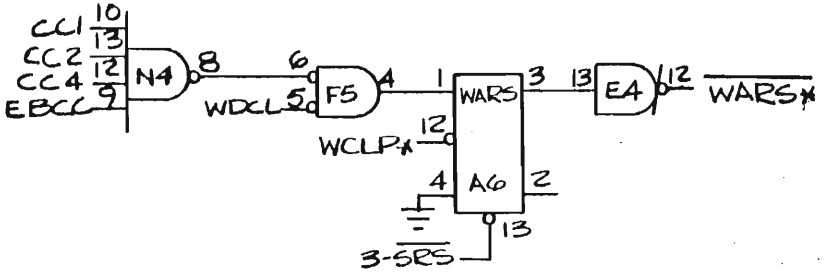




WRITE STORAGE



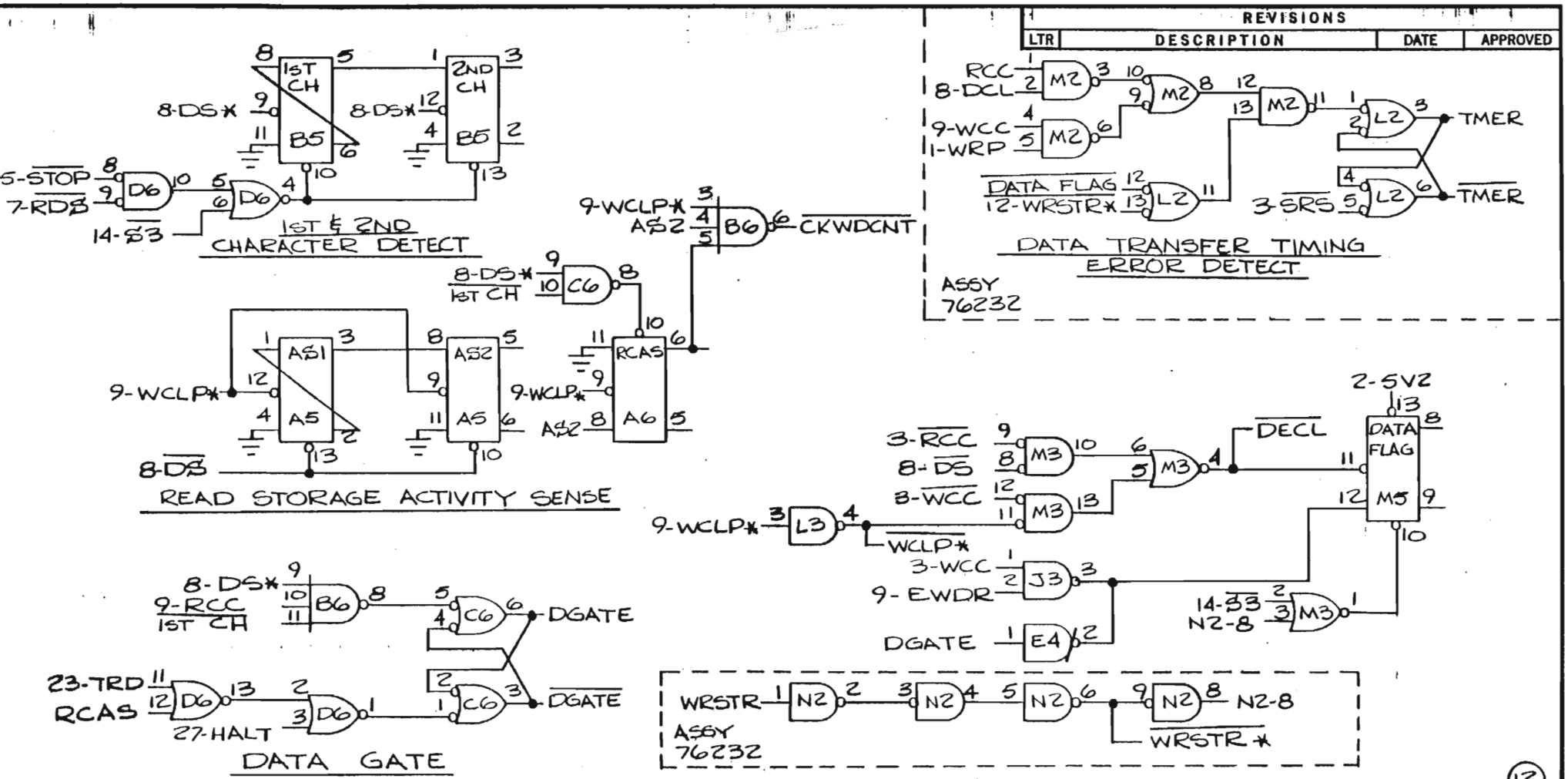
EXIT STATE 3 LOGIC

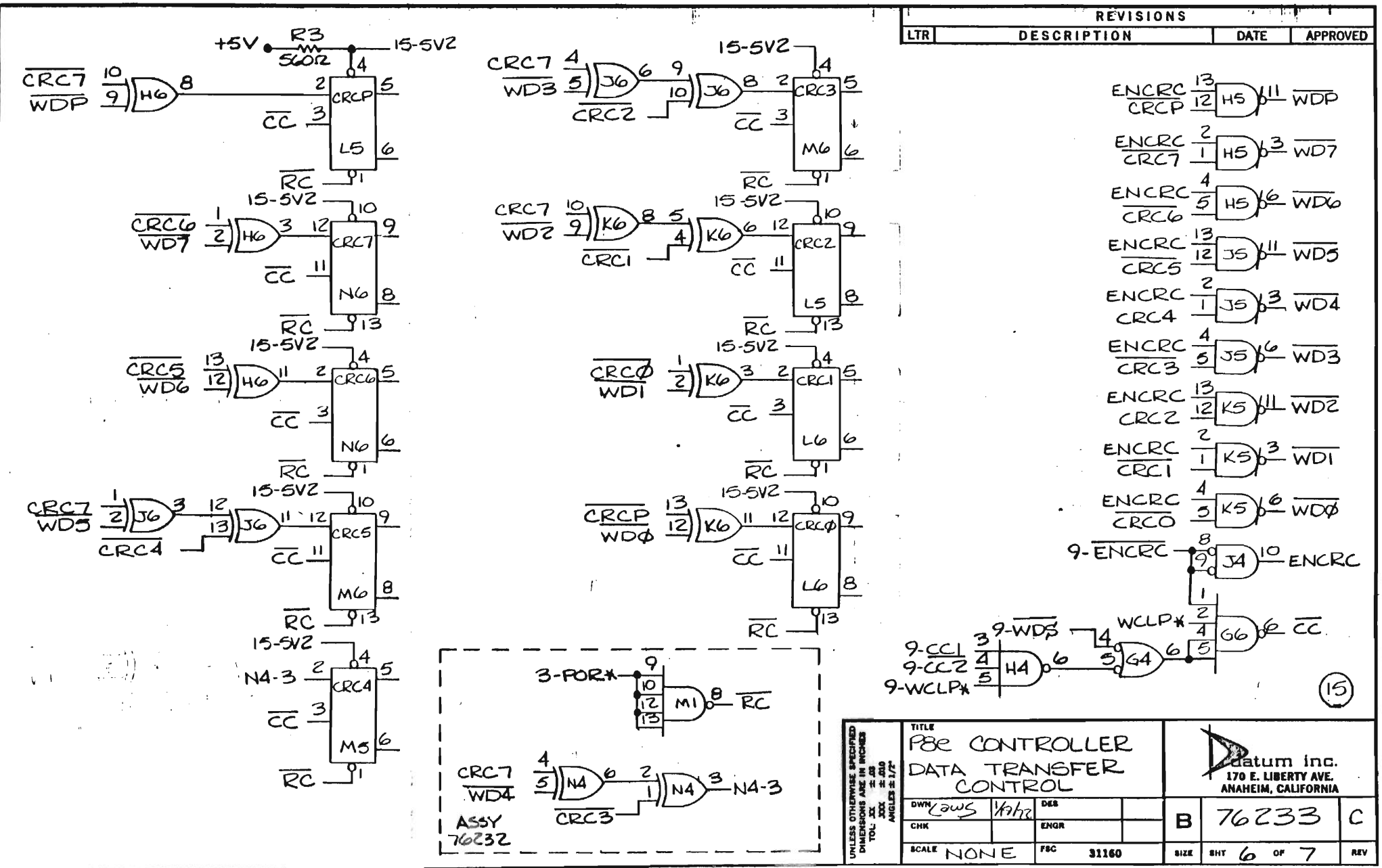


*LRC GENERATOR (WRITE AMP RESET)

9

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°	TITLE: P8e CONTROLLER: DATA TRANSFER CONTROL	datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
DWN Cows 1/14/72	DES	B	76233 C
CHK	ENGR		
SCALE NONE	FSC 31160	SIZE	SHT 4 OF 7 REV





REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

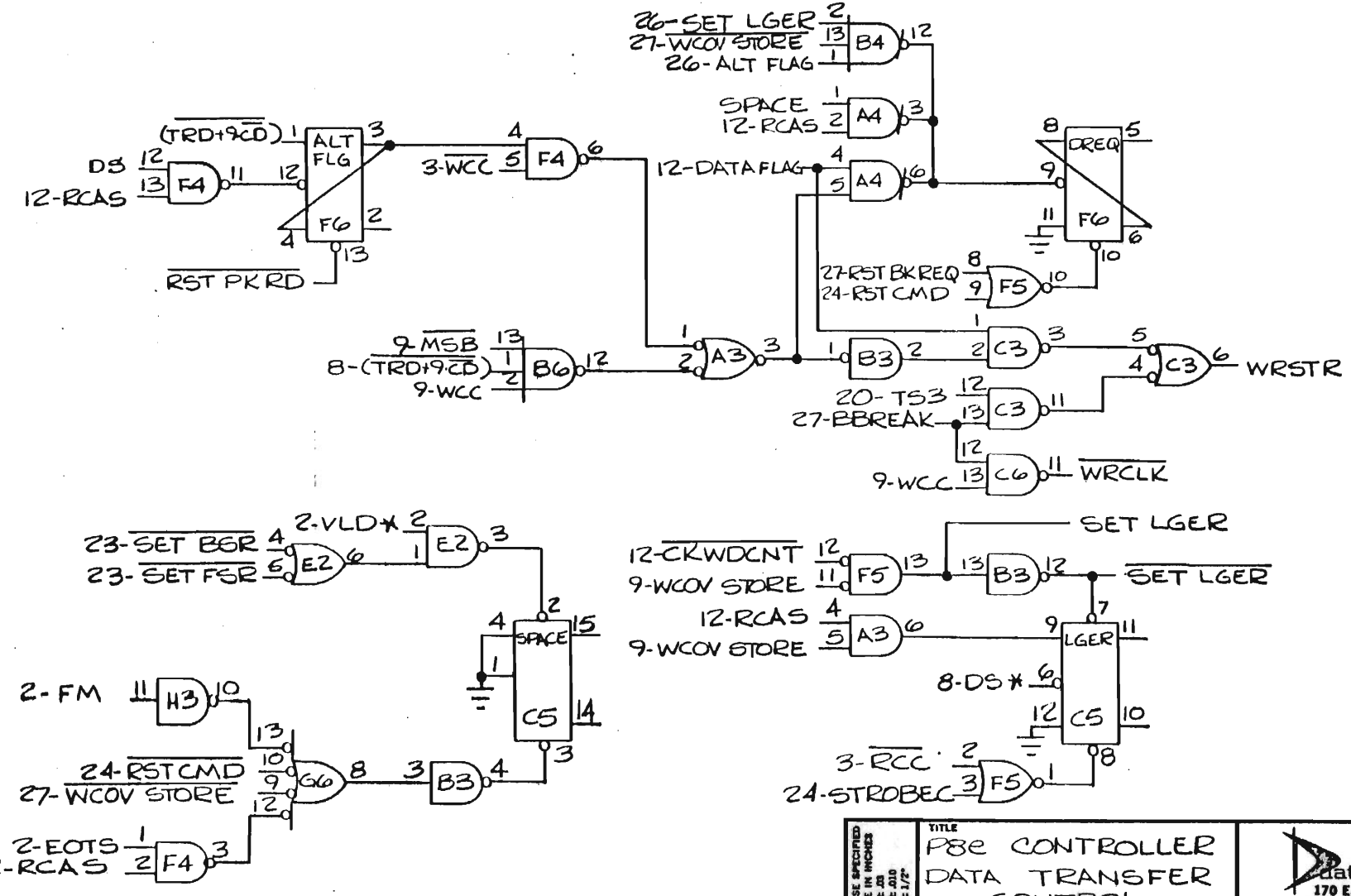
TITLE
P8e CONTROLLER
DATA TRANSFER
CONTROL

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	CHK	DES	ENGR	SCALE	FSC
Lows 1/31/82				NONE	31160

SIZE		SHT	OF	REV
B	76233	6	7	C

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



(26)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03, .XXX ±.010, ANGLES ±1/2°

TITLE: P8e CONTROLLER DATA TRANSFER CONTROL

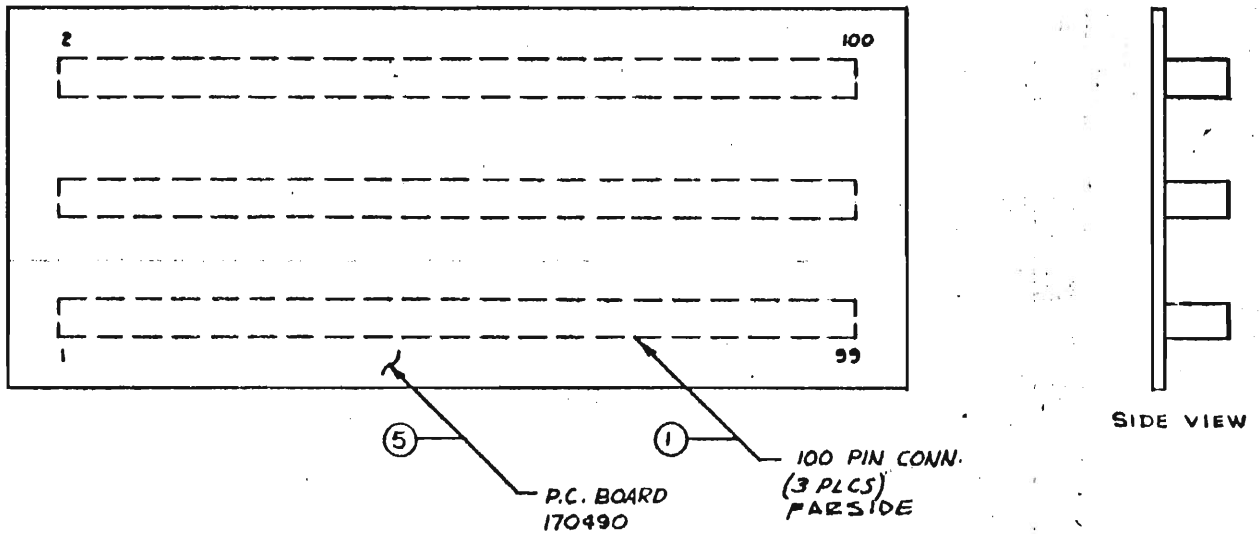
DWN Caws 1/11/82		DES	
CHK		ENGR	
SCALE NONE		FSC 31160	

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE	SHT	REV
B	7 OF 7	C

76233

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	REVISED PER E.C.O. 2138	1-8-75 H.	D.P.



NOTE:

1. MOUNT CONN. OPPOSITE NUMBERED SIDE

7-18-72

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ±1/2°

TITLE: PDP8E CONN. BOARD

DWN: PIZUTO 1/9/72 | DES | CHK | ENGR | SCALE — | FSC 31160

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 76258 | A

SIZE | SHT 1 OF 1 | REV

APPENDIX A

REPLACEMENT PARTS

A.1 INTRODUCTION

This appendix contains information for ordering replacement parts and recommended spare parts for the equipment. Table A-1 lists the recommended spares for the equipment by DATUM part number and includes commercial equivalent where applicable.

A.2 ORDERING INFORMATION

To obtain replacement parts from DATUM, address order or inquiry to the nearest DATUM sales/service office and supply the following information:

a. Equipment model and serial number.

b. DATUM part number of item(s).

c. Quantity of part(s) desired.

d. Reference designation of part(s).

To order a part listed in the table, provide the following information:

a. Equipment model and serial number.

b. Description of the part, including function and location in the equipment.

c. Quantity desired.

DESCRIPTION	DATUM PART NO.	QTY.	COMMERCIAL EQUIVALENT
Resistor, 560Ω, 1/4W, 5%	0102-0561	1	
Resistor, 1K, 1/4W, 5%	0102-0102	1	
Capacitor, 4.7uf @ 35V	0220-0475	1	
Capacitor, .1uf	0226-0104	1	
IC	0301-0380	1	Signetics SP380A
IC	0301-0384	1	Signetics SP384A
IC	0301-0936	1	National DM936(15836)
IC	0301-0946	1	National DM946(15846)
IC	0301-0962	1	National DM962(15862)
IC	0301-7400	1	T.I. N7400A
IC	0301-7402	1	T.I. N7402A
IC	0301-7404	1	T.I. N7404A
IC	0301-7406	1	T.I. N7406
IC	0301-7408	1	T.I. N7408A
IC	0301-7410	1	T.I. N7410A
IC	0301-7437	1	T.I. N7437
IC	0301-7438	2	T.I. N7438
IC	0301-7440	1	T.I. N7440A
IC	0301-7442	1	T.I. N7442
IC	0301-7473	1	T.I. N7473A
IC	0301-7474	2	T.I. SN7474
IC	0301-7475	1	T.I. SN7475B
IC	0301-7H22	1	T.I. SN74H22A
IC	0301-7H11	1	T.I. N74H11
IC	0301-8271	1	Signetics N8271B
Bus Strip 960079	2460-0001	1	
14 Pin Low Profile Socket W/W	1708-3100-1	1	
Resistor, 100Ω, 1/4W, 5%	0102-0101	1	
Resistor, 1.5KΩ, 1/4, 5%	0102-0152	1	
Resistor, 3.3KΩ, 1/4, 5%	0102-0332	1	
Resistor, 10K 1/4W, 5%	0102-0103	1	

DESCRIPTION	DATUM PART NO.	QTY.	COMMERCIAL EQUIVALENT
Capacitor, 1500pf	0225-0152	1	
Capacitor, .047uf	0210-0473	1	
Capacitor, 39uf, 10V	0220-0396	1	
Capacitor, 330pf	0225-0331	1	
Diode SG1930	0500-0116	1	
IC	0301-0930	1	National DM930(15830)
IC	0301-0944	1	National DM944(15844)
IC	0301-7107	1	T.I. SN74107
IC	0301-7476	1	T.I. SN7476
IC	0301-8291	1	Signetics N8291A
Crystal 180 KHZ	1302-0180	1	
Crystal 125.1 KHZ	1302-0125-1	1	
16 Pin Socket	1708-3100	1	
Wire Wrap Pins	5128-5931-2	1	
Resistor, 4.7K, 1/4W, 5%	0102-0472	1	
Capacitor, 100 f	0225-0101	1	
IC	0301-5804	1	T.I. SN151804N
IC	0301-7430	1	T.I. N7430A
IC	0301-7475	1	T.I. SN7475B
IC	0301-7486	1	T.I. N7486
IC	0301-8262	1	Signetics N8262A
IC	0301-0936	1	T.I. 15836
Bus Strip 960029	2460-0001	1	
IC	0301-7486	1	T.I. N7486
14 Pin Header	1702-0014	1	
Connector 100 Pin	702554	1	