TECHNICAL MANUAL

S34/A
STORAGE MODULE DISK CONTROLLER

DATARAM
CORPORATION

TECHNICAL MANUAL

S34/A
STORAGE MODULE DISK CONTROLLER

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1.0 GENERAL

This specification defines the functional, electrical and mechanical characteristics of the Model S34/A, Storage Module Disk Controller produced by Dataram Corporation for the PDP-11* series of computers.

1.1 Description

The Model S34/A Disk Controller emulates the functions and operations of the DEC* RH11 Controller and attached RM02 and/or RM05 Disk Drives. Used with one to four 80MByte, 160MByte, or 300MByte CDC (or equivalent) storage modules or 84MByte Fujitsu M2312 Mini-Winchesters, the Model S34/A is functionally equivalent to a DEC RM02/RM05 Subsystem of the same configuration. Any combination of drive sizes may be mixed on the same controller.

There is a limit of 4 logical drives. Since two logical RM02 disk units are mapped onto one 160MByte Disk Drive, up to 2 physical drives can be connected using 160MByte drives. See Figure 1.1 for typical system configuration. See Table 1.3 for a list of OEM compatible disk drives.

The S34/A Controller also provides dual port capability enabling two controllers to access one or more common disks which are equipped with dual port option. See Figure 1.2 for a typical system configuration. Refer to Table 1.1 and 1.2 for a summary of performance characteristics and a general comparison of S34/A and RM02/RM05 specifications.

The S34/A Controller provides a formatted disk capacity of 67 megabytes as an RM02 on an 80MByte SMD or 84 MByte M2312, and 256 megabytes as an RM05 on a 300MByte SMD. Data when recorded on standard 80 and 300 megabyte SMD Disk Packs is formatted identically to that of an RM02 or RM05 respectively. The disk packs are therefore interchangeable with the equivalent DEC disk packs.

* Registered trademark of Digital Equipment Corporation.

The S34/A Controller provides several forms of redundancy and reliability enhancement with error detection and isolation operations performed on all information read from the disk.

1) The RM02/RM05 compatible header block with provisions for accepting manufacturer or user specified codes to indicate that the sector is unacceptable for data storage.

2) RM02/RM05 compatible thirty-two bit ECC for data error detection allowing correction of a single 11-bit error burst.

3) RM02/RM05 compatible 16 bit CRC for header error detection.

4) Offset commands causing the heads to move off the track centerline to recover data that is not normally recoverable.

These features permit the software to detect and correct errors and recover data that would otherwise be lost. Since the pack, reading format, redundancy, and recovery techniques are identical to those used by the DEC RM02/RM05, data can be easily interchanged between S34/A and RM02/RM05 disk subsystems when standard 80 and 300 MByte disk packs are used.

The functional compatibility of the S34/A with the DEC RM02/RM05 subsystem also provides compatibility with existing DEC software. Standard DEC operating systems and diagnostic software may be used without patching.

1.2 Enhancements

The S34/A has an on-board format feature which may be used instead of host processor-based formatting programs. In addition to formatting the pack, this feature writes DEC compatible manufacturer's and user's bad sector files. The feature formats an 80 MB pack in less than 1.5 minutes. It formats a 300 MB pack in less than five minutes.

Additional performance enhancements over the DEC RM02/RM05 and other similar controllers have been included in the S34/A.

1) A 3584 Byte RAM memory provides a 7 sector data buffer which eliminates data late errors, enables multiple sector, cross-track (spiral) read or write operations, and allows the controller to be operated at a low NPR priority level.

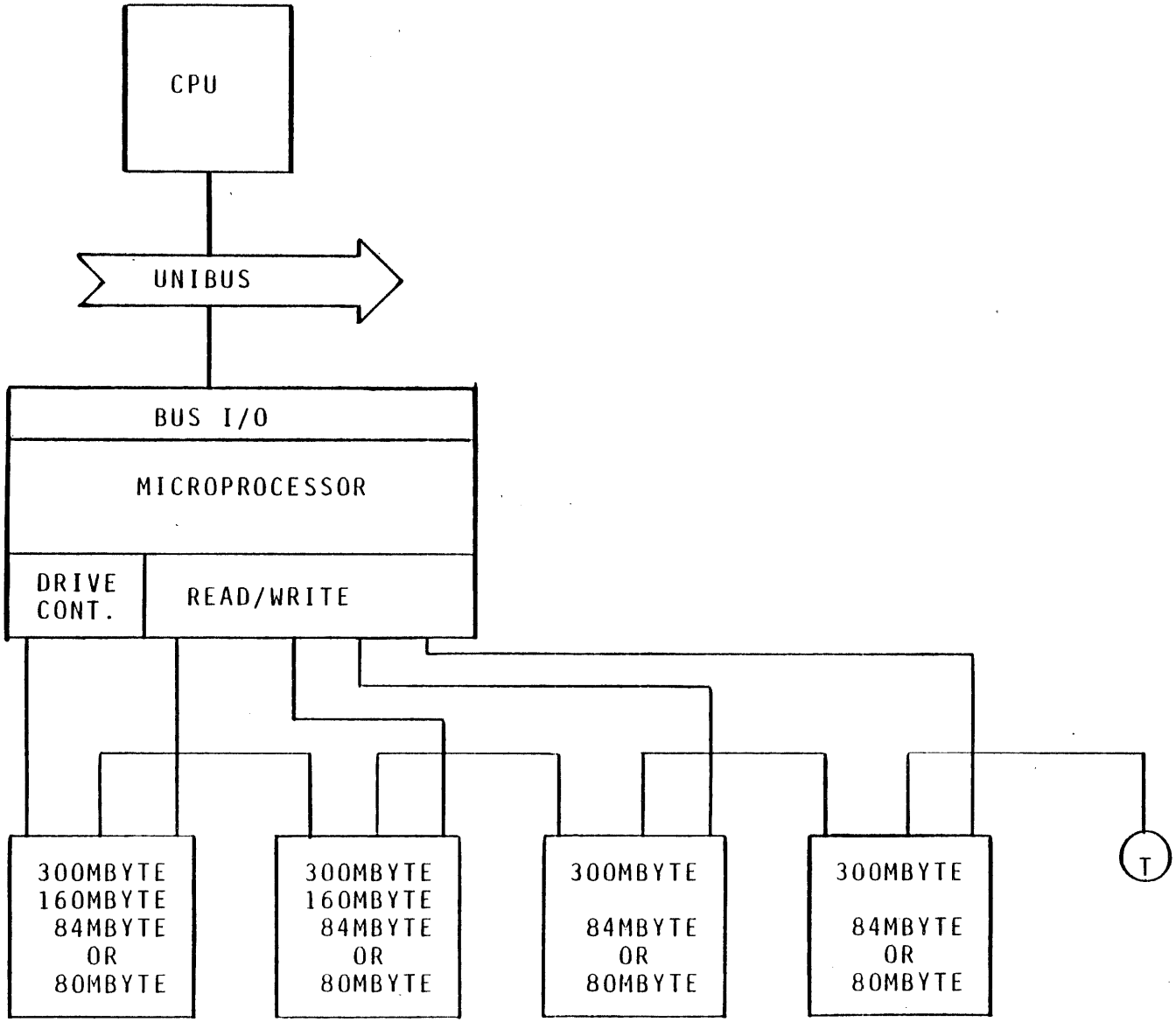
2) Eight selectable burst sizes of 1 to 128 words/NPR cycle can be selected by switches.

3) NPR throttle reduces burst sizes automatically depending on NPR or BR activity of other devices, even if they are at a lower priority. Fixed burst size may be selected by jumper (no throttle).

4) Nine selectable NPR "OFF" times from 0 to 400usec optimize system performance and prevent "bus hogging".

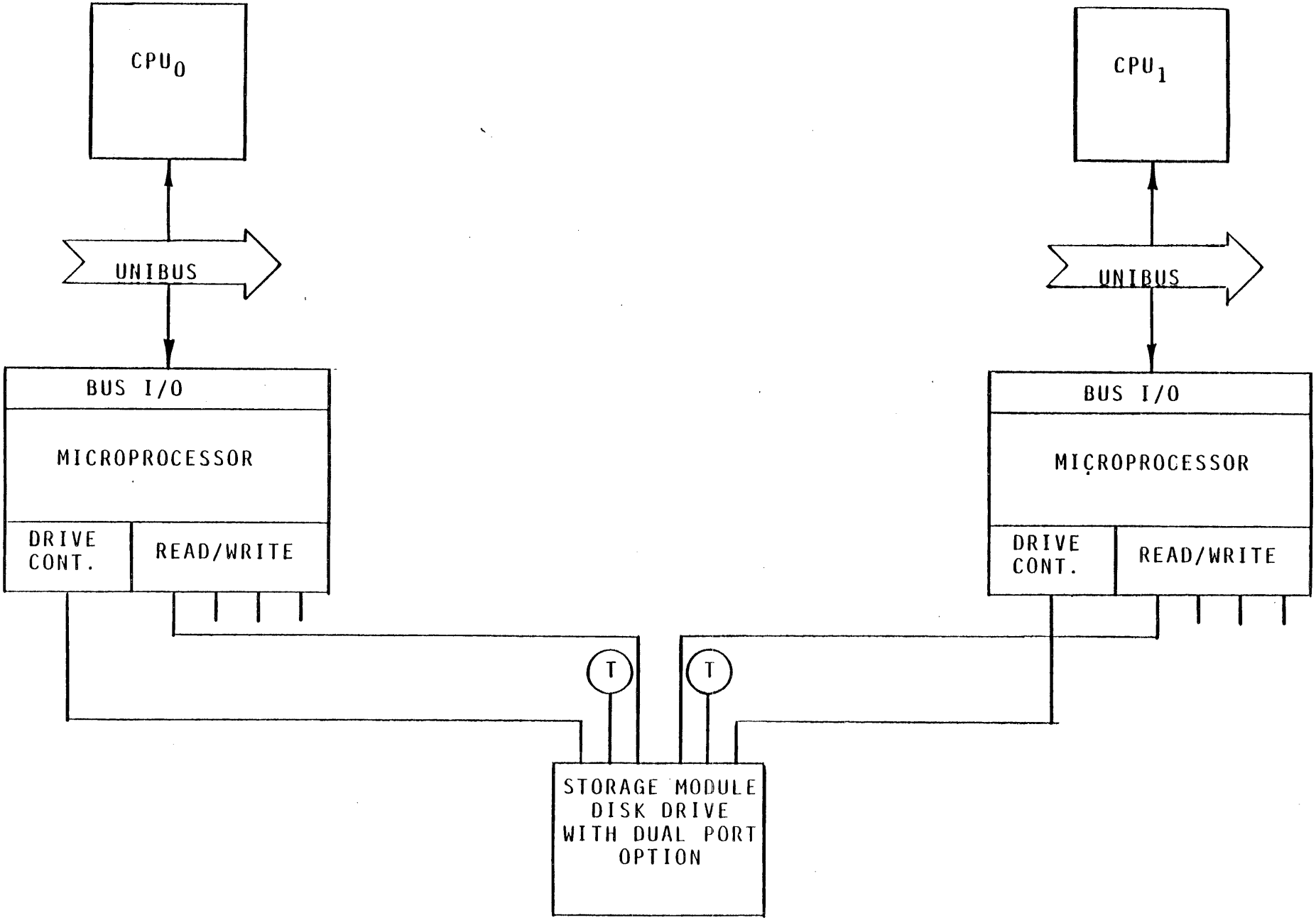
5) Ability to transfer a complete track or cylinder in one revolution without interleave, at 3600 RPM.

6) Optionally selectable 2:1 interleave format on any combination of the connected drives.



S34/A SINGLE PORTED CONFIGURATION - 1-4 PHYSICAL DRIVES

FIGURE 1.1



DUAL PORTED CONFIGURATION - 1-4 DRIVES

FIGURE 1.2

TABLE 1.1
CONTROLLER AND PERFORMANCE
CHARACTERISTICS

FUNCTION	CHARACTERISTICS
Type	Storage Module disk controller.
Application	Direct interface to PDP-11 standard UNIBUS* and to most SMD compatible disk drives.
Software Compatibility	DEC RH-11/RM02/RM05 System: Standard functional diagnostics RSX-11M RSTS/E.
Electrical:	
Power	8.5 amps @ +5 VDC, 0.5 amps @ -15 VDC
PDP-11 Bus Load	1 unit load, a-l lines
Physical:	
Dimensions	15.68" x 8.88" hex
Mounting	Plugs directly into PDP-11 standard UNIBUS SPC slot via C,D,E,F connector.
Drive Cable	60-conductor flat cable, 100 ft. max. 26-conductor flat cable, 50 ft. max.
PDP-11 Interface:	
Compatibility	Direct to PDP-11 standard UNIBUS
Addressing	Direct to 128 words (256 bytes)
Unibus Base Address:	Standard: 776700_8 Selectable: 760000_8 - 777700_8 by switch
Unibus Vector Address:	Standard: 254_8 Selectable: 0 - 774_8 by switches.
Unibus Priority Level:	Standard: BR5 Selectable: BR4-BR7 by jumpers.
Physical Drives	1 - 4 per controller.
Disk Data Rates	Up to 10 mBit per second serial data.
Dual Port Drives	Dual port operations supported on drives suitably equipped.
Media	DEC RM02/RM05 media compatible (See Table 1.3)

* Registered trademark of Digital Equipment Corporation

TABLE 1.1
(CONTINUED)

FUNCTION	CHARACTERISTICS
Register Compatibility	Separate registers for each disk allow emulation of overlapped seeks.
Buffer Memory	3584 byte (7 sector) bipolar RAM buffer, to eliminate data late errors.

TABLE 1.2
SPECIFICATION COMPARISON

SPECIFICATION	DEC RM02/RM05	DRC S34/A 80/300 MB	DRC S34/A 160MB	DRC S34/A FUJITSU M2312
1) SEEK TIME				
Maximum Seek Time (822 cylinders), mSec.	55.0	55.0	55.0	40.0
Average Seek Time, mSec.	30.0	30.0	30.0	20.0
1 Cylinder Seek Time,mSec.	6	6	6	5
Seek to Same Cylinder Time µSec	37.5	37.5	37.5	10
2) LATENCY				
Speed, RPM	2400/3600	3600	3600	3600
Rotational Time, mSec.	25.0	16.7	16.7	16.7
Maximum Latency, mSec.	25.9	16.9	16.9	16.9
Average Latency, mSec.	12.5	8.4	8.4	8.4
3) START/STOP TIME				
Start (Maximum), Sec.	25/35	35	35	20
Stop (Maximum), Sec.	20/35	35	35	40
4) CAPACITY				
Platters/Drive	3/10	3/10	3	4*
Tracks/Cylinder	5/19	5/19	10	7*
Cylinder/Pack	823	823	823	589*
Total Tracks/Pack	4115/15637	4115/15637	8230	4123
Sectors/Track	32	32	32	32
Data Bytes/Sector	512	512	512	512
MBytes/Drive (Formatted)	67.4/256.2	67.4/256.2	134.8	67.4
Drives/System, Max.	8	4	2	4
MBytes/System, Max.	539.4/2049.6	269.7/1024.8	269.7	269.7
5) DATA RATES				
Bit Density, BPI	6060	6060	6060	9550
Bit Cell Time, mSec.	155.0/103.3	103.3	103.3	101.7
Data Rate,KBytes/Sec.	655/1209	1209	1209	1229
6) ERROR DETECTION/CORRECTION				
Bits/Sector	32	32	32	32
Maximum Time for Correction, mSec.	5.96	4.47	4.47	4.47

* Fujitsu Drive is mapped such that 7 TRKS., 589 CYLS. look to the operating system as 5 TRKS. and 823 CYLS.

TABLE 1.3
S34/A COMPATIBLE DRIVES

Manufacturer No.	Capacity (Unformatted)	Emulates	DEC Pack Interchangeable
CDC 9762	80MBytes	RM02	YES
9766	300MBytes	RM05	YES
9730-80	80MBytes	RM02	NO (Fixed Media)
9730-160	160MBytes	(2) RM02's	NO (Fixed Media)
Ampex DM980	80MBytes	RM02	YES
DM9300	300MBytes	RM05	YES
Capricorn 130	330MBytes	RM05	NO (Fixed Media)
Memorex 677-30	300MBytes	RM05	NO
Century T82RM	80MBytes	RM02	NO
T302RM	300MBytes	RM05	NO
Fujitsu M2280	80MBytes	RM02	NO (Fixed Media)
M2284	160MBytes	(2) RM02's	NO (Fixed Media)
M2312	84MBytes	RM02	NO (Fixed Media)
M2294	330MBytes	RM05	NO (Fixed Media)

2.0 ELECTRICAL SPECIFICATIONS

2.1 UNIBUS Interface

The S34/A Controller interfaces directly to the standard UNIBUS of the PDP-11, plugs into any standard hex SPC slot, and completely conforms to UNIBUS protocol. The bus drivers and receivers used present one unit load on all signal lines and are identical components to those used by DEC.

The following types of I/O transfers occur between the controller and the processor and/or memory modules via the bus:

2.1.1 Programmed I/O Transfers

Transfers to the controller may be either an 8 bit byte or a full 16 bit word. Programmed transfers exchange control and status between the controller and the processor. The controller executes DATI, DATO, and DATOB types of bus cycles.

2.1.2 DMA Transfers

All data read or write transfers are performed as full word DMA (or NPR) transfers between the controller and memory. To accomodate the high data rates required by the disk with minimum bus hogging, the S34/A transfers 1 to 128 words (switch selectable size) per NPR request-grant cycle, with switch programmable off time to optimize system performance. NPR throttle control reduces burst size automatically when other devices make "NPR" or "BR" requests. Controller priority for NPR transfers is a function of its position on the bus with respect to other devices. Selection of priority is a system consideration.

2.1.3 Interrupts

The controller generates interrupts to the processor to flag various events (end of transfer, error condition, etc.) using location 254_8 as the standard interrupt vector. Controller priority for interrupt request is a function of:

(1) the priority level assigned the controller, and (2) its position on the bus with respect to other devices with the same priority level. The vector address is switch selectable.

The PDP-11 has four interrupt request levels, BR4-BR7, with BR4 as the lowest level. The standard level assigned to the RH11 is BR5, and this connection is implemented as standard on the S34/A board (along with connection of the associated bus grant level, BG5). The unused bus request levels - BR4,6,7 - and bus grant levels - BG4,6,7 - have their respective in and out lines jumpered together on the S34/A board to assure continuity of these lines to succeeding devices on the UNIBUS. Should it be desired to alter the standard BR priority, jumpers may be incorporated or removed as required.

2.1.4 BUS Signals

The S34/A Controller interfaces to the standard PDP-11 UNIBUS via the C,D,E, and F connectors. The S34/A occupies any hex location designated as a Small Peripheral Controller (SPC) slot. Pin designations are shown in Table 2.1.

The S34/A bus interface circuitry conforms to the bus specification for the Standard PDP-11 UNIBUS.

1) Input Levels
   TTL Logical Low: +0.8 VDC max.
   TTL Logical High: +2.0 VDC min.

2) Output Levels
   TTL Logical Low: +0.4 VDC max.
   TTL Logical High: +2.4 VDC min.

3) Components
   The S34/A uses the following device types for the PDP-11 bus interface:
   Receiver: National 8640
   Driver: TI 7438
   Transceiver: AMD 2908 and National 8641

1	A	2
	A	
	B	
	C	GND
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
GND	T	
	U	
	V	

1	B	2
	A	
	B	
	C	GND
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
GND	T	
	U	
	V	

1	C	2
BUSNPGIH	A	+5V
BUSNPGOH	B	
	C	GND
	D	BUSD15N
	E	BUSD14N
	F	BUSD13N
BUSD11N	H	BUSD12N
	J	BUSD10N
	K	BUSD09N
	L	BUSD08N
	M	BUSD07N
BUSDCLOL	N	BUSD04N
	P	BUSD05N
	R	BUSD01N
BUSPBL	S	BUSD00N
GND	T	BUSD03N
	U	BUSD02N
	V	BUSD06N

1	D	2
	A	+5V
	B	
	C	GND
	D	BUSBR7L
	E	BUSBR6L
	F	BUSBR5L
	H	BUSBR4L
	J	
	K	BUSBGIN7H
BUSINITL	L	BUSBGOUT7
	M	BUSBGIN6H
	N	BUSBGOUT6
	P	BUSBGIN5H
	R	BUSBGOUT5
	S	BUSBGIN4H
GND	T	BUSBGOUT4
	U	
	V	

TABLE 2.1

UNIBUS SIGNALS

1	E	2
	A	+5V
	B	
BUSA12L	C	GND
BUSA17L	D	BUSA15L
BUSMSYNCL	E	BUSA16L
BUSA07L	F	BUSCIL
BUSA01L	H	BUSA00L
BUSSSYNCL	J	BUSC0L
BUSA14L	K	BUSA13L
BUSA11	L	
	M	
	N	BUSA08L
BUSA10L	P	BUSA07L
BUSA09L	R	
	S	
GND	T	
BUSA06L	U	BUSA04L
BUSA05L	V	BUSA03L

1	F	2
	A	+5V
	B	-15V
	C	GND
BUSBBSYL	D	
	E	
	F	
	H	
BUSNPRL	J	
	K	
	L	
BUSINTRL	M	
	N	
	P	
	R	
	S	
GND	T	BUSSACKL
	U	
	V	

TABLE 2.1

UNIBUS SIGNALS
(CONT.)

2.1.5 Initialization and Power Sequencing

The controller response to an Initialize (INIT) signal on the UNIBUS is immediate, terminating any function being executed by any drive.

The controller monitors the DC power status line on the UNIBUS, DCLO (DC Power Low). In the event the DCLO indicates that system DC power is unstable, the controller will terminate and clear the controller unconditionally. When DC power is stabilized, the controller will perform an automatic initialization so that it is ready to execute the initial software commands received.

2.2 Controller Registers

Twenty registers are visible to software and emulated by the controller to communicate control commands, status data, error conditions, and maintenance information.

Specific bit locations in these drive registers are designated as follows:

- Read Only indicates that software can read the bits but cannot load them.
- Write Only indicates that software can load the bits but will read back a zero.
- Read/Write indicates that software may load and read the bits back.

Table 2.2 defines these registers, their mnemonics, their UNIBUS addresses, whether they are read only or read/write, and their basic function.

TABLE 2.2
CONTROLLER REGISTERS

REGISTER	NAME	UNIBUS ADDRESS	MODE	FUNCTION
RMCS1	Control	776 700	Read/Write	Function code, Go bit.
RMWC	Word Count	776 702	Read/Write	2's complement of number o words to be transferred.
RMBA	Bus Address	776 704	Read/Write	Memory address of location where data transfer is to begin.
RMDA	Desired Sector/Track Address	776 706	Read/Write	Disk sector and track address where transfer is to occur.
RMCS2	Status	776 710	Read/Write	Controller status indicati
RMDS	Drive Status	776 712	Read/Write	Non-error status plus erro summary bit.
RMER1	Error No. 1	776 714	Read/Write	Individual error indicatio
RMAS	Attention Summary	776 716	Read/Write	1-bit per drive attention summary status.
RMLA	Look Ahead	776 720	Read Only	Current sector address under heads.
RMDB	Data Buffer	776 722	Read Only	Input and output connectio to silo for maintenance.
RMMR1	Maintenance No.1	776 724	Read/Write	Diagnostic test functions.
RMDT	Drive Type	776 726	Read Only	Drive Character indication
RMSN	Serial No.	776 730	Read Only	Drive Unit No. Plus One.
RMOF	Offset	776 732	Read/Write	Control bit for offset of drive heads, and format mode bit.
RMDC	Desired Cylinder	776 734	Read/Write	Address of cylinder for seek operation.
RMHR	Holding	776 736	Read/Write	Not used; contents always all zeros.
RMMR2	Maintenance No.2	776 740	Read Only	Diagnostic test functions.
RMER2	Error No. 2	776 742	Read/Write	Drive error bits.
RMEC1	ECC Position	776 744	Read Only	Position of error burst.
RMEC2	ECC Pattern	776 746	Read Only	Error Burst.

2.3 Error Correction Code (ECC)

The S34/A Controller contains ECC logic capable of detecting errors in the data read from disk and providing information to the software to permit data recovery. The ECC code employed locates an error that falls within an 11-bit burst. An uncorrectable error includes any error field larger than an 11-bit burst and isolated dropped bits. (For example, one bit in word 0 and one bit in word 225). The S34/A indicates ECC uncorrectable errors to the software by setting the ECC hard error bit (ECH) in Error Register No. 1 (RMER1). The ECC logic performs the following functions:

1. Finds the 11-bit burst where the read error is located.
2. Determines the exact location of the burst within the data field.

This error information is provided to software through two registers.

1. ECC Pattern Register (RMEC2)

   Contains the actual 11-bit correction mask.

2. ECC Position Register (RMEC1)

   Contains the location of the first bit of the error burst within the 4096 bit data field.

The actual correction of the error is done by software using the data contained in these two registers. In the event of a hard ECC error, the contents of the ECC pattern and ECC position registers are of no significance.

2.4 Disk Interface

The controller has an industry standard SMD interface, utilizing Motorola 3450 and 3453 differential transmitters and receivers. These circuits provide a terminated, balanced transmission system and allow disk operation at radial distances up to fifty feet and daisychain distances up to one hundred feet from the controller. Round cable drive connections are shown in Figures 2.3 and 2.4.

The "A" cable is a twisted pair, flat ribbon cable which allows mass termination to the "A" cable connector without stripping. The "B" cable is a flat ribbon cable with a ground plane and drain wire, which allows mass termination without stripping. See Figures 2.1 and 2.2.

2.5 Testability

The design of the S34/A Controller includes provisions for ease of testing in both the factory and field environments.

2.5.1 Factory Testing

Features which aid in the factory test environment include:

1. External Control/Access
   - Disabling on board ROM.
   - Substitution of external ROM/RAM for microdiagnostics.
   - Access to ROM address for breakpoint or sync.
   - Control of internal clock for clock stop, single micro-step or "clock divisible by "n" testing.

2. "Closed Path" structure including:
   - Address/Data moved on to and off of the UNIBUS simultaneously to allow verification of the UNIBUS interface outside a system environment.
   - Disk Control/Status/Data Path ports interconnectable externally to allow verification of disk interface without connection to a disk.

The capability to exercise the controller with external micro-diagnostics in the manufacturing environment is insured by the above provisions which can be implemented by use of a special prom set with micro-diagnostics.

2.5.2 Internal Self-Test

The S34/A Controller firmware contains an automatic self-test feature enabled on power-on with errors/status displayed via on board LED's. Initially the LED's are illuminated with successive tests extinguishing LED's. The microprocessor ALU, and control sequencer are checked. A failure will leave LED's lit and prevent any I/O operations. The same LED's are used for activity indicators during DMA transfer operations.

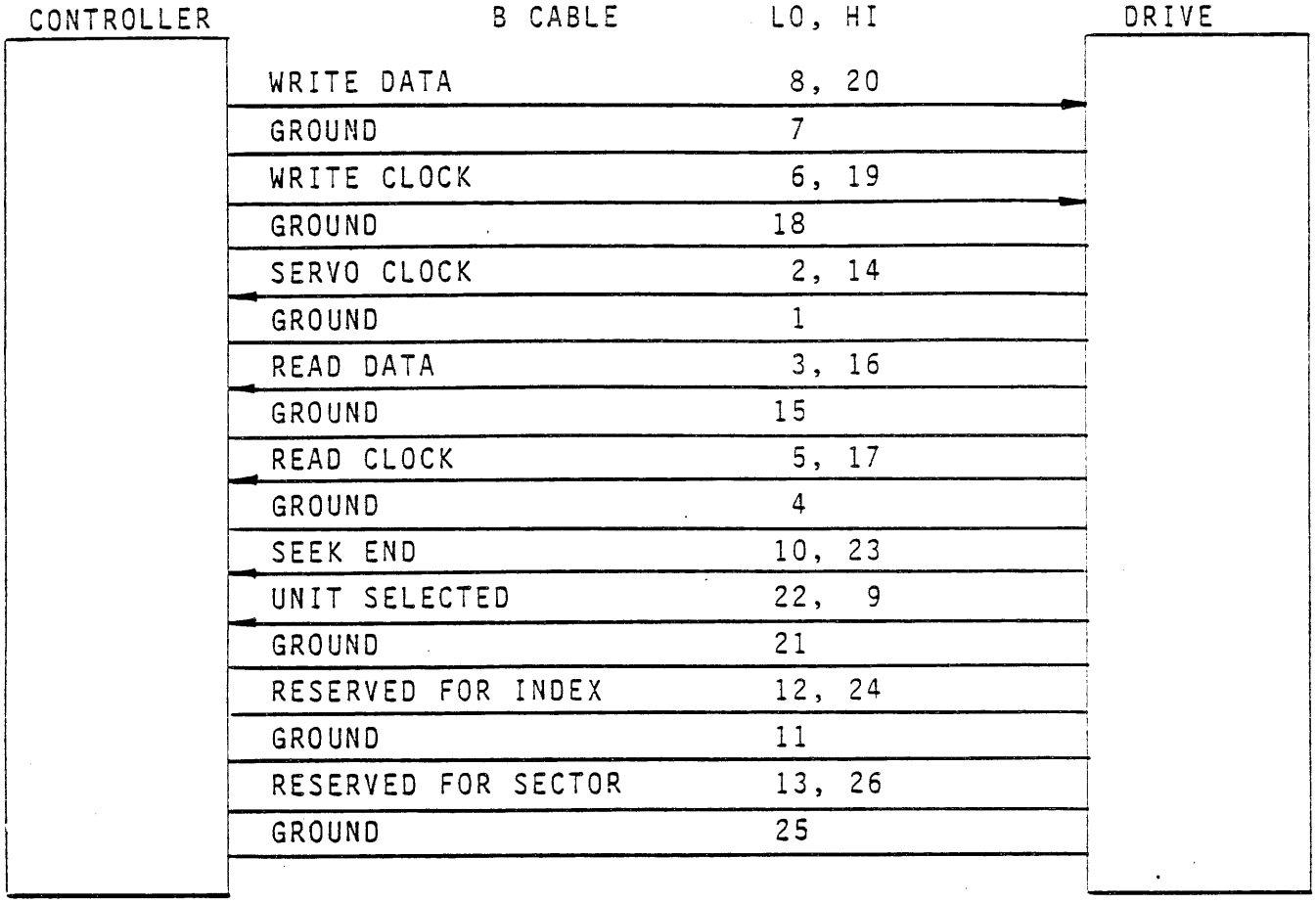
2.6 Power Consumption

Voltage & Current - +5V @ 8.5 amps MAX.
-15V @ 0.5 amps MAX.

CONTROLLER	A CABLE (CONTROL CABLE)			DRIVE
A CABLE			LO HI	A CABLE
	Unit Select Tag		22, 52	
	Unit Select 2^0		23, 53	
	Unit Select 2^1		24, 54	
	Unit Select 2^2		26, 56	
	Unit Select 2^3		27, 57	
	Tag 1	2	1, 31	
	Tag 2	2	2, 32	
	Tag 3	2	3, 33	
	Bit 0	2	4, 34	
	Bit 1	2	5, 35	
	Bit 2	2	6, 36	
	Bit 3	2	7, 37	
	Bit 4	2	8, 38	
	Bit 5	2	9, 39	
	Bit 6	2	10, 40	
	Bit 7	2	11, 41	
	Bit 8	2	12, 42	
	Bit 9	2	13, 43	
	OPEN CABLE DETECTOR		14, 44	
	INDEX	2	18, 48	
	SECTOR	2	25, 55	
	FAULT	2	15, 45	
	SEEK ERROR	2	16, 46	
	ON CYLINDER	2	17, 47	
	UNIT READY	2	19, 49	
	ADDRESS MARK FOUND	2	20, 50	
	WRITE PROTECTED	2	28, 58	
	POWER SEQUENCE PICK		29	ONE TWISTED PAIR
	POWER SEQUENCE HOLD		59	
	BUSY	2 1	21, 51	
	NOT USED (SPARE)		30, 60	

NOTE: 60 POSTITION
28 AWG. 30 TWISTED PAIR - STRAIGHT FLAT CABLE
MAXIMUM LENGTH - 100 FT.
1 DUAL CHANNEL UNITS ONLY
2 GATED BY UNIT SELECT

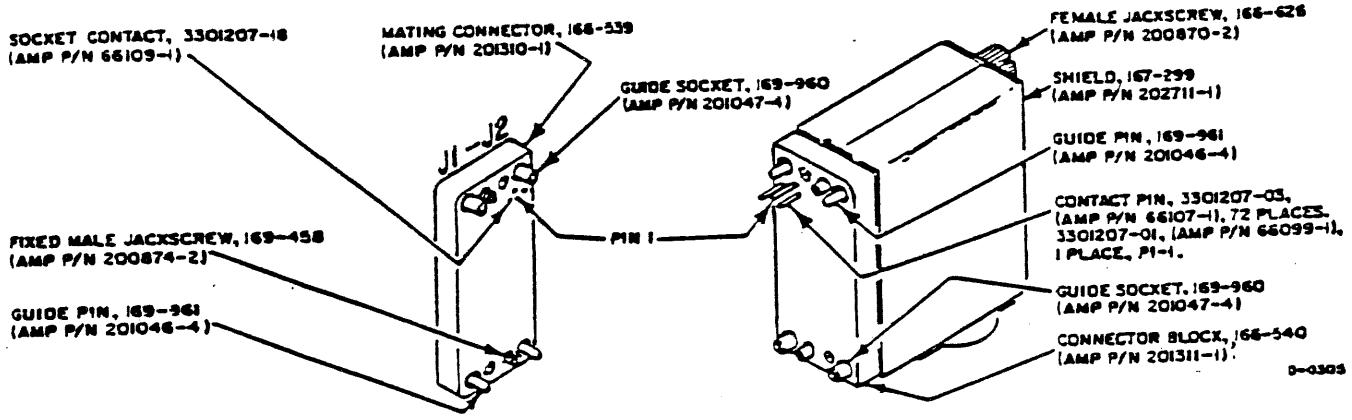
Figure 2.1 - Tag Bus I/O Interface



NOTES:
1. 26 CONDUCTOR, FLAT CABLE. MAXIMUM LENGTH - 50 FT.
2. NO SIGNALS GATED BY UNIT SELECTED.

FIGURE 2.2 "B" CABLE INTERFACE
(DATA CABLE)

"A" CABLE DEFINITIONS
ROUND CABLE DRIVE CONNECTOR



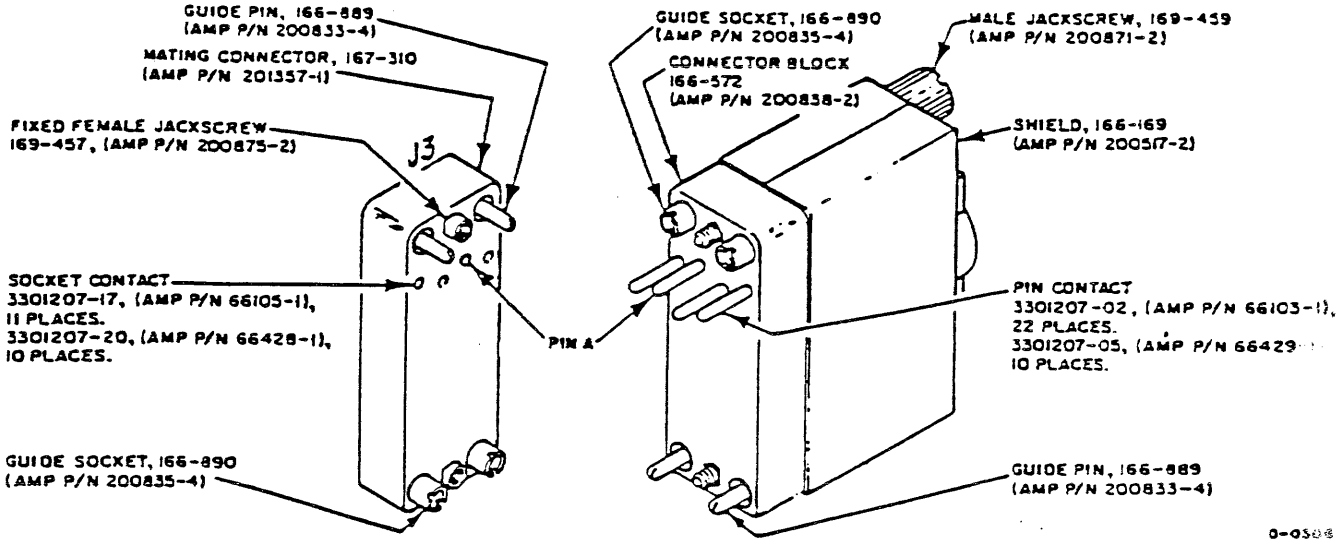
PIN IDENTIFICATIONS

SIGNAL NAME	FLAT CABLE PINS*	J1/J2** PINS	FROM	TO
UNIT SELECT BIT 0	23,53	1,4	CONTROL UNIT	DRIVE
UNIT SELECT BIT 1	24,54	2,5	CONTROL UNIT	DRIVE
UNIT SELECT BIT 2	26,56	3,7	CONTROL UNIT	DRIVE
UNIT SELECT BIT 3	27,57	8,12	CONTROL UNIT	DRIVE
UNIT SELECT TAG	22,52	22,25	CONTROL UNIT	DRIVE
SET CYLINDER (TAG 1)	1,31	46,49	CONTROL UNIT	DRIVE
SET HEAD ADDRESS (TAG 2)	2,32	48,51	CONTROL UNIT	DRIVE
CONTROL TAG (TAG 3)	3,33	52,55	CONTROL UNIT	DRIVE
BIT 0	4,34	23,26	CONTROL UNIT	DRIVE
BIT 1	5,35	24,27	CONTROL UNIT	DRIVE
BIT 2	6,36	28,31	CONTROL UNIT	DRIVE
BIT 3	7,37	29,32	CONTROL UNIT	DRIVE
BIT 4	8,38	30,33	CONTROL UNIT	DRIVE
BIT 5	9,39	34,37	CONTROL UNIT	DRIVE
BIT 6	10,40	35,38	CONTROL UNIT	DRIVE
BIT 7	11,41	36,39	CONTROL UNIT	DRIVE
BIT 8	12,42	40,43	CONTROL UNIT	DRIVE
BIT 9	13,43	41,44	CONTROL UNIT	DRIVE
OPEN CABLE DETECTOR	14,44	16,20	CONTROL UNIT	DRIVE
INDEX	18,48	10,13	DRIVE	CONTROL UNIT
SECTOR	25,55	74,77	DRIVE	CONTROL UNIT
FAULT (UNSAFE)	15,45	11,14	DRIVE	CONTROL UNIT
SEEK ERROR (SEEK INCOMPLETE)	16,46	75,78	DRIVE	CONTROL UNIT
ON CYLINDER (ATTENTION)	17,47	15,18	DRIVE	CONTROL UNIT
UNIT READY (ON LINE)	19,49	17,21	DRIVE	CONTROL UNIT
WRITE PROTECT	28,58	53,56	DRIVE	CONTROL UNIT
ADDRESS MARK (NOT USED)	20,50	42,45	DRIVE	CONTROL UNIT
POWER SEQUENCE HOLD (-)	59	76	CONTROL UNIT	DRIVE
SEQUENCE PICK IN (-)	29	73	CONTROL UNIT	DRIVE
NOT USED (SPARE)	30,60	54,57		
DC GROUND	—	80		
SHIELD GROUND	—	82		
BUSY (DUAL CHANNEL ONLY)	21,51	67,72	DRIVE	CONTROL UNIT

*IN FLAT CABLES HAVING ROUND CABLE CONNECTOR ON ONE END
**FIRST PIN IN PAIR IS (-); SECOND IS (+) IN ROUND CABLE CONNECTOR

FIGURE 2.3

"B" CABLE DEFINITIONS
ROUND CABLE DRIVE CONNECTOR



PIN IDENTIFICATIONS

SIGNAL NAME	FLAT CABLE PINS※	J3 PINS[5]	FROM	TO
WRITE DATA	8,20	A,B	CONTROL UNIT	DRIVE
GROUND[1]	7	D		
SERVO CLOCK	2,14	M,N	DRIVE	CONTROL UNIT
GROUND [1,4]	1	K		
READ DATA	3,16	U,V	DRIVE	CONTROL UNIT
GROUND [1]	15	T		
READ CLOCK	5,17	W,X	DRIVE	
GROUND [1]	4	Y		
WRITE CLOCK	6,19	H,J	CONTROL UNIT	DRIVE
GROUND [1]	18	E		
SEEK END (ATTN)	10,23	AA,CC	DRIVE	CONTROL UNIT
UNIT SELECTED	22,9	DD,BB	DRIVE	CONTROL UNIT
GROUND [2]	21	C		
INDEX OPT. [3]	12,24	EE,HH	DRIVE	CONTROL UNIT
GROUND [2]	11	L		
SECTOR OPT.[3]	13,26	FF,JJ	DRIVE	CONTROL UNIT
GROUND [2]	25	F		

※ IN FLAT CABLES HAVING ROUND CABLE CONNECTOR ON ONE END

1 A SHIELD FOR SIGNAL PAIR WHICH PROCEEDS IT IN ROUND CABLE

2 PRESENT IN FLAT CABLE ONLY, BOTH CONNECTOR TYPES

3 SECTOR AND INDEX MUST APPEAR IN "A" CABLE FOR S03 CONTROLLERS (SMD STANDARD CONFIGURATION).

4 ALSO SHIELD DRAIN WIRE OF FLAT CABLE

5 ROUND CABLE CONNECTOR

FIGURE 2.4

3.0 MECHANICAL SPECIFICATIONS

3.1 Dimensions

The S34/A Controller is physically contained on a single hex height printed circuit board measuring 15.68 inches by 8.88 inches. The card is multi-layer printed wiring board having its power and ground distribution planes on the inner layers and signal lines on the outer layers (See Figure 5.2). The controller plugs into any standard hex SPC slot. This minimizes mounting space requirements, system configuration changes, specially wired system units, and external boxes and cables. Permanently attached insertion/extraction handles are provided to facilitate insertion and removal from the computer.

3.2 Cables

Disk drives are connected to the S34/A via flat ribbon connectors located on the top edge of the controller. One 60 conductor ribbon cable providing address, control and status between the controller and drives is connected to all drives in a daisy-chained fashion with a terminator at the end of the cable. A 26 conductor ribbon cable providing clock and data between the controller and each drive is required for each attached disk and connected in a star configuration.

3.3 Weight

Weight (without cables) is 1 pound, 11 ounces (.76 kg).

4.0 ENVIRONMENTAL SPECIFICATIONS

The S34/A Controller is designed to operate in or withstand shipping environments as follows:

4.1 Temperature

Operating:	0^{o} to $55^{o}C$
Non-Operating:	-40^{o} to $60^{o}C$

4.2 Relative Humidity

Operating:	0 to 90% (without condensation)
Non-Operating:	5 to 95% (without condensation)

4.3 Altitude

Operating:	1000 ft. below sea level to 10,000 ft. above sea level.
Non-Operating:	1000 ft. below sea level to 20,000 ft. above sea level.

4.4 Vibration

Will withstand normal stresses encountered in transportation.

5.0 INSTALLATION AND OPERATION

5.1 General

A major advantage of the S34/A is its ease of installation. Since it is completely contained on a single hex board, it is physically installed the same as a standard PDP-11 hex interface board.

The user is referred to various DEC publications which may contain specific checklist items which should be observed in the installation of standard PDP-11 components as well as the S34 controller. Initial problems with the disk controller when imbedded in a system are, more often than not, the result of failure to observe all necessary installation procedures for all system elements, not just the disk controller. Often, various oversights will not be detected with some system elements connected and will appear only with the addition of new components. Some specific steps to avoid often-incurred problems of a general nature are noted below.

1) Verify that the capacity of the power source is not exceeded, and the source meets the tolerances specified for the minicomputer (and any other system elements of a special nature). An overloaded power source may produce intermittent failures which are difficult to detect.

2) Insure that the bus interrupt and DMA grant daisy-chain lines are properly propagated. Unused option slots should have these lines (NPG and BRG) jumpered.

3) Check to see that all boards in the chassis are properly oriented and that boards and drive cables are properly seated in the connectors.*

CAUTION: It is possible to plug S34/A controller in backwards. If power is applied in this position, controller components will be destroyed.

4) Insure that all necessary signals, including power and ground inputs, are connected as required to the backplane assembly.

5) Check all option switches, option jumpers, and other variable items for proper settings/connection.

5.2 Inspection

A visual inspection of the unit is recommended after unpacking. Specific checks should be made for such items as bent or broken pins or component leads, damaged components, or any other visual evidence of physical damage. The cables (if included) should likewise be visually inspected prior to installation.

The simplicity of the S34/A controller makes such visual inspection most worthwhile because physical damage incurred in shipment will usually be obvious. Should any damage be detected, you may wish to immediately return the unit to Dataram for repair prior to further handling.

5.3 Installation

5.3.1 Computer Installation (See Section 5.6 for Configuration and Option Switches and Jumpers)

After visual inspection and prior to insertion in the computer, it is recommended that the S34/A be checked for proper configuration. The optional selections on the board which control configuration are:

- Proper Interrupt Vector Address Switch Settings
- Proper CSR Address Switch Settings
- Proper Drive Configuration Switch Settings
- Burst Size Jumpers and NPR Off Time Switch Settings
- Throttle Jumpers and Dual Port Jumpers

The S34/A interfaces the UNIBUS via the C,D,E, and F connectors only. The backplane slot must be compatible with Hex Small Peripheral Controllers (SPC). DEC system unit backplane may be either UNIBUS or MUDBUS compatible.

The S34/A controller has DMA capability and utilizes the BUSNPG line. It must be insured that BNPGIH and BNPGOH lines are not wirewrap jumpered on the computer bacakplane in the slot to be occupied by the S34/A (Pins CA1 and CB1). If the S34/A is unplugged, this jumper or a grant card with this connection must be installed for a proper operation without the S34/A.

5.3.2 Drive Installation

5.3.2.1 General

Prior to connecting the drive to the S34/A, confirm the following:

(1) The Drive is configured for the proper number of sectors (32 sector format for S34/A).

(2) Sector and Index are on the A cable.

(3) Make sure the last physical drive is terminated per manufacturer's recommendation.

(4) Ground cable must be installed between computer frame and drive ground lug.

5.3.2.2 Cable Connections

The 60-position A cable connector is installed in the corresponding connector on the S34/A. The 26-position B cable connector of each drive may be installed in any of the four connectors on the S34/A. The four connectors are identical and no particular sequence of physical/logical drive number assignment is required. Arrows marked on connectors must line up.

CAUTION: Use care when inserting into and removing from the drive cable connectors because the connector material can be easily damaged. A connector tool is available from the manufacturer and is recommended.

5.4 Operation and Diagnostics

5.4.1 Power Up

Upon power up, the S34/A performs a self test diagnostic. This can be noticed by observing the LED's located along the edge of the S34/A. During power up, the LED's will appear to flash on simultaneously and then go out.

If the LED's do not all go out but remain lit in some binary code, this will indicate a failure of some sub-test.

The power up tests are to verify proper operation of internal controller circuits only and should run to completion (all lights go out) whether or not a drive is connected. If the board has +5 volts applied and backplane signals BUS BPOK-H and BUS DCOK-H are both high (true), the tests should run successfully on a good controller board.

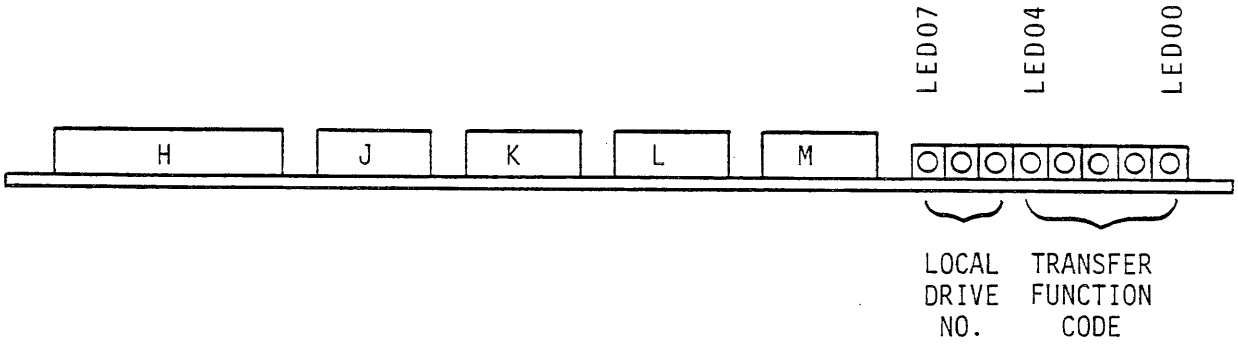
If an error condition is displayed by the LED's the installation procedure should not be continued. Recheck all connections and options and retry the power up self test. If there is still a failure, refer to section 5.5. If the problem remains, contact the factory for assistance or return the S34/A for repair as outlined in Dataram's "Return Material Policy".

Activity Indication

In normal operation, the eight LED's serve as activity indicators. LED07, 06, & 05 are the logical drive number. LED04, 03, 02, 01 & 00 are the transfer function being performed on that drive number, equivalent to CS1 bits 05 thru 01 respectively. (See Table 5.1).

TABLE 5.1
ACTIVITY DISPLAY

OPERATION	RESULTING DISPLAY				
	LED04	LED03	LED02	LED01	LED00
Write Check Data	1	0	1	0	0
Write Check Header & Data	1	0	1	0	1
Write Data	1	1	0	0	0
Write Header & Data	1	1	0	0	1
Read Data	1	1	1	0	0
Read Header & Data	1	1	1	0	1



5.4.2 Diagnostics

The S34/A will run all the DEC RM02 and RM05 diagnostics without patches with the exception of the two Diskless Diagnostic Tests. These diagnostics will not run at all due to the testing of the specific logic/hardware implementation of an RM02 and RM05, and extensive use of maintenance mode operations which are not emulated in the S34/A.

5.4.2.1 Formatting

Prior to running any diagnostics or operating system, the disk must first be formatted by one of two methods. They are the DEC RM05/3/2 format diagnostic CZRMLB1 or the on-board format method. The on-board format does not verify but does not require any special diagnostic program and takes only about 1.5 minutes for an RM02 and about 5 minutes for an RM05. This format could then be verified through use of a bad block utility of the operating system.

1. On Board Format

This feature requires a series of register loads in the proper order, with acceptable values, as well as SW2-8 open or off to enable this feature. This switch should be closed or on to hardware disable this feature.

On board FMT Feature:

SW2-8	OPEN OR OFF	ENABLE
SW2-8	CLOSED OR ON	DISABLE

To run on board format, set SW2-8 to open or off. Then run the following program, starting at any address.

```
012737  000040   176710    MOV   #40,@#CS2        ; CONTROLLER CLEAR
012700  176700             MOV   #CS1,R0          ; 176700 in RØ
012737  00000n   176710    MOV   #0,@#CS2         ; n=LOGICAL DRIVE NUMBER (Ø-7)
012710  000021             MOV   #21, (R0)        ; READ IN PRESET
012737  010000   176732    MOV   #10000,@#0F      ; 16-BIT FORMAT
012737  000001   176724    MOV   #1,@#MR1         ; MAINTENANCE MODE
012737  XXXXXX   176730    MOV   #XXXXXX,@#SN     ; XXXXXX=PACK SERIAL NO. (NON ZERO OCTAL
012710  000023             MOV   #23,(R0)         ; PACK ACKNOWLEDGE
012710  000061             MOV   #61,(R0)         ; WRITE DATA

105710             LOOP:   TSTB  (R0)             ; LOOP TIL DRIVE RDY .
100376                     BPL LOOP

000000                     HALT
```

After program halts, read the following registers. They should contain the values as shown below:

```
776700   RMCS1 = 146260   TRANS ERR, RDY, NO GO
776714   RMER1 = 001000   ADDR OVFL ERR
776734   RMDC  = 001467   CYL 823
```

2. Formatting With the CZRMLB1 RM05/3/2 Formatter

The program is used as supplied by DEC. If the pack has not been previously formatted as an RM02 or RM05 Disk Pack, the bad block directory must first be initialized. The Formatter program can be run and it will report several errors. These are due to improper information in the bad track directory. The Formatter program will pause waiting for an operator response to the prompt "SN": (Serial Number). At this time, enter any octal non-zero pack serial number and a Carriage Return. The Formatter will now write the bad block directory and format the pack. Few, if any, errors should be reported on this pass. Any errors on this or subsequent passes are probably due to marginal media. If there is difficulty in getting the Formatter program to operate successfully on a previously unformatted pack, the following program can be used to initialize the directory sufficiently to allow the Formatter to run.

```
ADR

1000    12737      40    176710   MOV #40,@#176710        ;CNTRL CLR
1006    12737      23    176700   MOV #23,@#176700        ;PACK ACKNOWLEDGE
1014    12737   10000    176732   MOV #10000,@#176732     ;16 BIT FMT
1022    12737    1466    176734   MOV #1466,@#176734      ;CYL ADR=822
1030    12737   *2000    176706   MOV #2000,@#176706      ;TRK=4 SCT=Ø
1036    12737    2000    176704   MOV #2000;@#176704      ;BUS ADR=2000
1044    12737  160000    176702   MOV #160000,@#176702    ;WD CNT=16K
1052    12737  151466      2000   MOV #151466,@#2000      ;1ST HDR WRD
1060    12737    2000      2002   MOV #2000,@#2002        ;2ND HDR WRD
1066    12737      63    176700   MOV #63,@#176700        ;WRT HDR & DATA CMD
1074   105737  176700             NRDY:TSTB@#176700       ;TST RDY
1100   100375                     BPL NRDY                ;LOOP TIL RDY
1102        0                     HALT                    ;RDY

*1030   12737   11000    176706   ;TRK=18,SCT=Ø for RM05
```

A full pass of the format program CZRMLB1 should then be run to fully initialize the bad block directory. Some errors should be expected. A second pass should then be run, resulting in few, if any, errors. Any errors on subsequent passes would probably be due to marginal areas on the pack. These bad or marginal blocks may be flagged bad by use of the formatter utility which is accessed by starting the formatter diagnostic at location 204.

5.4.2.2 Diagnostic Tests

After formatting, the following diagnostic tests may be run without modification:

1. Performance Exerciser CZRMUB1 (RM05/3/2) Best overall single test. Verifies data and seek error rates while exercising the disk system by using all commands and data patterns. This test requires a fully formatted disk pack.

2. Functional Tests
   Part 1 CZRMMB1 (RM05/3/2) - Test Housekeeping and Mechanical Positioning.

   Part 2 CZRMNBØ (RM05/3/2) - Tests Write, Read, and Write Check operations using Header and Data.

   Part 3 CZRMOBØ (RM05/3/2) - Tests Write, Read, and Write Check operations using Data only.

WARNING! The functional diagnostics can leave bad format on the disk if halted before completion. The test must be stopped with a control 'C' from the keyboard. On systems with SOFT 'SWR' type control 'G': then control 'C'.

3. Extended Drive Test CZRMVB1 (RM05/3/2) - Tests disk's ability to perform seeks and data storage and retrieval in the specified access times. Also tested are track and sector addressing. Disk pack must be formatted.

4. Drive Compatibility Test CZRMTB0 (RM05/3/2) - Tests pack interchange between RM02 Drives or RM05 Drives.

NOTE: Some diagnostic programs do not use the bad block directory and will report bad blocks as encountered.

5.4.2.3 Key-In Test Program

The program on Page 5-10 may be used to perform a rough operational check on the disk system at sites which do not have the full disk diagnostic or the means to load it. The contents of buffers may be changed, then Reads, Writes and Write Checks may be done. Proper status following each transfer should be verified by examining location 776700 (CSR1). The pack must have been formatted previously.

5.5 Disk System Troubleshooting Guide

5.5.1 Disk System failures usually fall into one of the following categories:

1) Internal S34/A Controller Problems
2) Drive Cabling Problems (A, B, Ground)
3) SMD Drive Problems
4) Host Processor Chassis Problems (CPU, Memory, Backplane, Power Supply)

The solution of any system problem relies on the successful isolation of the fault to one of these areas. Dataram controller support can be helpful only if the problem falls into the first category.

5.5.2 Fault Isolation Steps

5.5.2.1 Is it an Obvious S34/A Board-Problem?

1) Remove the A and B cables from the S34/A controller, then cycle the AC power to the computer off and on a few times. The self-test indicator lights should flash and then all go out. If one or more LED's remain on, either the S34/A is defective or the backplane wiring is improper. When any of the lights remain lit, the power-up sequence is aborted and the controller will not accept or respond to UNIBUS commands.

```
                                        .TITLE RM02.MAC
                                        ;THIS ROUTINE WILL TRANSFER DATA FROM MEMORY TO THE
                                        ;RM02 DISK, READ THE DATA BACK AND COMPARE FOR ERRORS.
                                        ;TRANSFER PARAMETERS MAY BE ALTERED AS DESIRED.
                                        ;
000000  012737  000040  176710  WRITE:  MOV     #40,    @#176710        ;CLR CONTROLER
000006  012737  000023  176700          MOV     #23,    @#176700        ;SET VOLUME VALID
000014  012737  010000  176732          MOV     #10000, @#176732        ;SET 16 BIT FORMAT
000022  005037  176710                  CLR     @#176710                ;SELECT UNIT 0
000026  012737  000000  176734          MOV     #0,     @#176734        ;SELECT CYCLINDER 0
000034  012737  000000  176706          MOV     #0,     @#176706        ;SELECT TRACK 0, SECTOR 0
000042  012737  010000  176704          MOV     #10000, @#176704        ;SELECT BUS ADDRESS (WRITE)
000050  012737  177770  176702          MOV     #177770,@#176702        ;SELECT WORD COUNT
000056  012737  000061  176700          MOV     #61,    @#176700        ;SELECT FUNCTION & GO BIT
000064  105737  176700                  TSTB    @#176700                ;TEST FOR WRITE XFER DONE
000070  100375                          BPL     .-4                     ;
                                        ;
000072  012737  000040  176710  READ:   MOV     #40,    @#176710        ;CLR CONTROLLER
000100  012737  010000  176732          MOV     #10000, @#176732        ;SET 16 BIT FORMAT
000106  012737  000000  176734          MOV     #0,     @#176734        ;SELECT CYCLINDER 0
000114  012737  000000  176706          MOV     #0,     @#176706        ;SELECT TRACK 0 , SCETOR 0
000122  012737  020000  176704          MOV     #20000, @#176704        ;SELECT BUS ADDRESS (READ)
000130  012737  177770  176702          MOV     #177770,@#176702        ;SELECT WORD COUNT
000136  012737  000071  176700          MOV     #71,    @#176700        ;SELECT FUNCTION & GO BIT
000144  105737  176700                  TSTB    @#176700                ;TEST FOR READ XFER DONE
000150  100375                          BPL     .-4                     ;
                                        ;
000152  012700  010000          CMP:    MOV     #10000, R0              ;SET WRITE DATA POINTER
000156  012701  020000                  MOV     #20000, R1              ;SET READ DATA POINTER
000162  012702  177770                  MOV     #177770,R2              ;SET WORD COUNT FOR COMPARE
000166  022021                  1$:     CMP     (R0)+,  (R1)+           ;COMPARE WRITE DATA WITH READ DATA
000170  001005                          BNE     ERROR                   ;HALT ON ERROR
000172  005202                          INC     R2                      ;INCREMENT WORD COUNT FOR COMPARE
000174  005702                          TST     R2                      ;TEST WORD COUNT FOR COMPARE OVERFLOW
000176  001373                          BNE     1$                      ;CONTINUE COMPARE IF NEGATIVE
000200  000167  177574          DONE:   JMP     WRITE                   ;TRANSFER OK
000204  000000                  ERROR:  HALT                            ;DATA COMPARE ERROR
        000000'                         .END WRITE
```

If the lights extinguish after 200 milliseconds or so as they should, the principal elements of the S34/A will be functioning properly. If the lights remain on, see Figure 5.1 (the Flow Diagram) for remedial action.

5.5.2.2 Is the S34/A Capable of Generating a Slave Response on the UNIBUS? Are the Emulated RM02/RM05 Registers Being Initialized Properly?

Do a "BUS INIT" (System Reset) by pressing the INIT button or cycling power to the computer. Examine the contents of each register at locations 776700 up to and including 776746, comparing each register to the "No Drive Connected" data in Table 5.2. If the data comes back wrong or if bus timeouts occur, check for possible custom address jumpering on the S34/A board, faulty backplane wiring, or dirty connector fingers.

5.5.2.3 Can the Emulated Registers Be Written Into?

Attempt to write the Word Count Register by depositing into and then reading back from address 776702.

1) Deposit all 1's (177777) into WC, then read it back. Repeat with all zeros. Any missing bits or bus timeout could mean poor seating of board, dirty board fingers, faulty backplane connector. Only certain bits in certain registers may be written into, so that writing into registers other than WC may produce confusing results. Modification of some registers causes the contents of other registers not addressed to change also as a result of the emulation process.

5.5.2.4 Can the S34/A Communicate with a Drive and Determine its Status?

1) Connect a single drive to the S34/A controller via A and B cables. Make sure that pin orientation is correct and that the "A" cable is terminated at the drive end. Set Drive Unit Number to UNIT 0 by inserting a "0" button or by setting drive switches on the drive. Install a scratch pack (if removable media), bring drive up to speed, and issue a system reset from the CPU front panel. The DRIVE PROTECT switch should be OFF.

Repeat the examination of RM02/RM05 emulated register per 5.5.2.2, this time comparing the data with the "drive connected and ready" data of Table 5.2. Data should be in agreement. If not, the differences should provide a clue to the trouble. Of particular interest is Drive Status (DS) Register, in which bit 7 set indicates that the drive is ready and bit 12 shows that the medium is on line (See section 6.2).

5.5.2.5 Is S34/A Capable of Completing a Disk Operation (Does Controller Sense Index and Sector Pulses of Selected Disk? Can Controller Operate in the Backplane's NPR Facility?)

With a formatted pack loaded, perform the following test:

1) Write location 776710 with a 40 to clear controller (status and buffer address).
2) Zero main memory location locations $0\text{-}20_8$ to provide a buffer space.
3) Write location 776702 with a 177770 to produce a word count of 8 decimal.
4) Write location 776706 with a zero to clear the DISK ADDRESS.
5) Write location 776700 with a 23 to set the VOLUME VALID bit and allow disk transfers.
6) Write location 776732 with a 10000 to set "16 bit mode" header bit.
7) Key this program into memory starting at location 10000:

```
10000   12737   71   776700   ;MOVE 71 COMMAND (READ) TO CSF
10006     777                ;LOOP AT 10006.
```

8) Start computer at location 10000.
9) Halt computer and examine CS1 at 776700. Status should read 4270 if no error occurred. A 1 in bit 15 indicates that an error was detected, while a 1 in bit 0 (XX71) means that the GO bit is still set and the command never executed. If bit 15 has set, the error bit in the other registers can be examined to better determine the nature of the failure.

10) If the Read was successful, the 8 words transferred should reside in locations 0-16 of main memory and may be examined.

11) Writes and Write Checks can be performed by placing 61 or 51 at location 10002, respectively. If the pack is initially unformatted, use one of the two methods of formatting described in section 5.4.2.1. The use of format (Write Header and Data) commands in this test may require that the pack be reformatted later.

Failing of the GO bit to clear is usually caused by a missing servo clock (B cable) or missing sector or index pulses on the A cable. Cable or drive faults could cause this. BUS timeout under NPR facility may cause (NXM) bit 11 of CS2 (776710) to set or the GO bit to stay set and the activity LEDs to show a transfer in progress, waiting for a grant.

5.5.2.6 <u>If any of the previous tests fail, it may become necessary to employ an oscilloscope to find the fault. This is especially true if cable problems are suspect and there is only one set of cables at the site.</u>

All signals in the SMD interface are current differential. When terminated with 100 ohms to ground the + side of an asserted signal will read 0 volts and the - side will read approximately -.8 volts. With a negated signal, the reverse is true. An unterminated line reads approximately -5 volts regardless of logic state.

If a "B Cable" is suspect, the cable may be disconnected at the controller end and scoped with a probe terminated to ground with 100 ohms. All of the B Cable lines are active whether their drive is selected or not and the signals, particularly the servo and read clocks, should be present all the time. The waveform should be sloped but not ragged and appear on both the + and - sides of the line, 180 degrees out of phase. The "selected" line should pulse periodically

as the drive is selected and its status polled by the firmware.

The "A" cable lines are driven mostly by the controller and probing should be done at the drive end. Exceptions to this are the INDEX and the SECTOR signals, which are gated with UNIT SELECTED and come from the drive.

The most satisfactory method of proving the integrity of an A or B cable is to "ring it out" with an ohmmeter or buzzer. Pin configuration tables appear as Figures 2.1 - 2.4. Continuity of the shield drain on pin 1 of the "B Cable" should also be verified.

It should be pointed out that a relatively high percentage of systems failures have been attributed to defective flat cables, regardless of their source of manufacture. The user should have his cables checked thoroughly (or replaced) before calling the drive or controller manufacturer to task.

5.5.2.7 Functional Testing of the S34/A System
Will the System Format a Pack?

1) Load DEC CZRMLB1 RM05/3/2 Formatter Program into the computer memory and execute. Error reports may be somewhat ambiguous and do not readily substitute for the previous procedures. The operating procedure is a part of the program's listing.

5.5.2.8 Will the System Transfer Data?

1) Load DEC CZRMVB1 RM05/3/2 Performance Exercisor and run. If the program indicates that no drives are on line, be sure that a Unit Select button from 0 to 3 is installed in the drive. If diagnostics cannot find the drive, it will not proceed further.

TABLE 5.2

REGISTER CONTENTS FOLLOWING POWER ON CONTROLLER RESET
AS READ SEQUENTIALLY

Bus Address	Register Designation	Contents w/o Drive	Contents W/Drive Powered But Not Rdy	Contents w/Drive Ø Ready RM02/RM05
776700	CS1	140200*	4200	4200*
776702	WC	0	0	0
776704	BA	0	0	0
776706	DA	XXXXXX	XXXXXX	XXXXXX
776710	SC2	10100*	100*	100*
776712	DS	0*	XX400*	10600*
776714	ER1	0	0	0
776716	AS	0	0	0
776720	LA	0	XXXXXX	XXXXXX
776722	DB	XXXXXX	XXXXXX	XXXXXX
776724	MR1	XXXXXX	XXXXXX	XXXXXX
776726	DT	0	20025/20027	020025*/020027*
776730	SN	0	100	100
776732	OF	0	0	0
776734	DC	0	0	0
776736	HR	XXXXXX	XXXXXX	XXXXXX
776740	MR2	XXXXXX	XXXXXX	XXXXXX
776742	ER2	0	0	0
776744	EC1	0	0	0
776746	EC2	0	0	0
776750	N/U	(Timeout)	(Timeout)	(Timeout)

* Significant Data

X-Indeterminate. Dependent upon emulation ROM revision level

For bit definition summary, see Table 6.1 and Section 6.2.

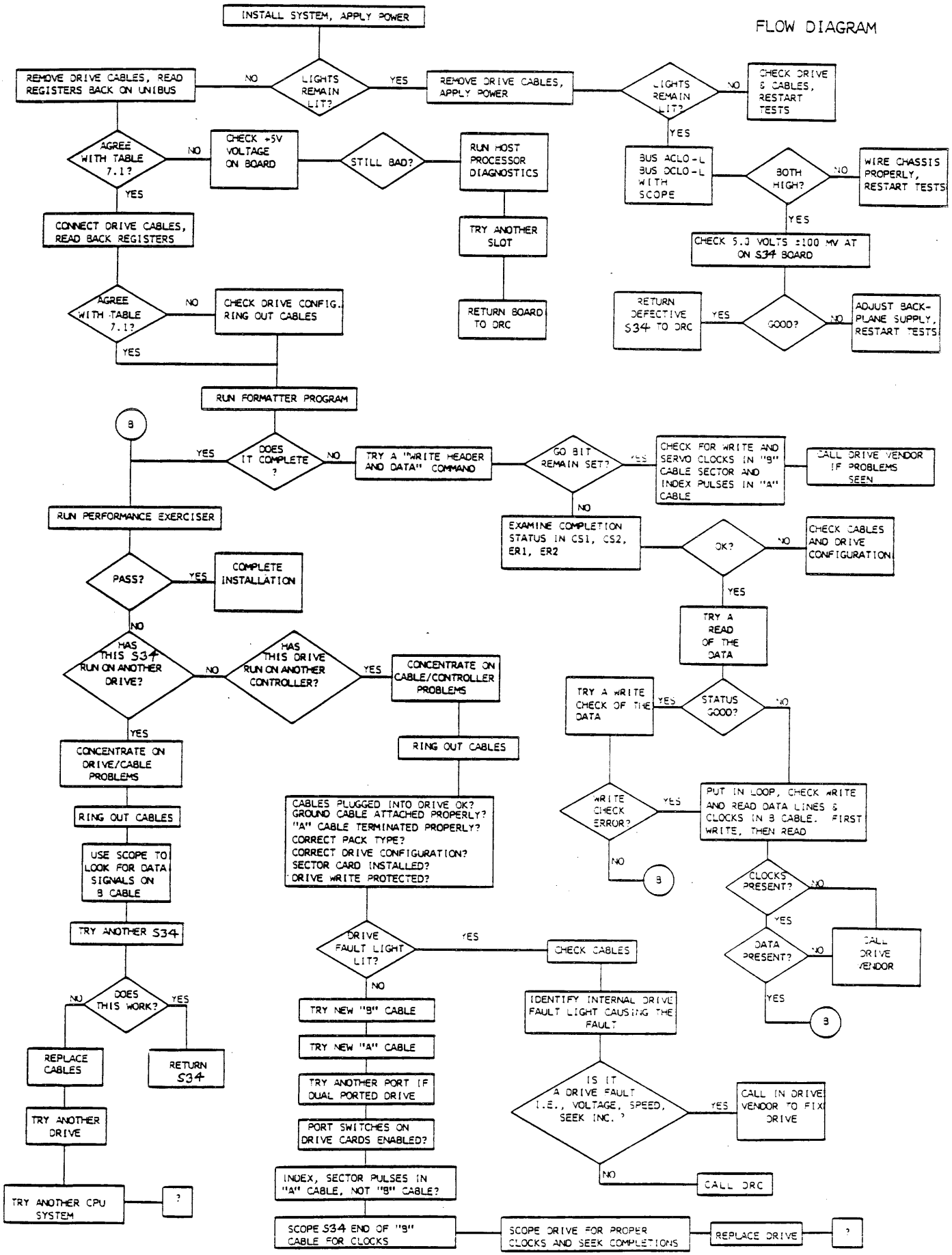
As the program executes, errors of various types may be reported. Some of these may be caused by bad areas of the pack; others may be related to drive head alignment. Poor grounding of the drive chassis to the CPU chassis may cause various types of intermittent "soft" errors.

If errors are logged during this test, the frequency and nature of the errors will determine whether the system is operating at an acceptable performance level. Substitution of disk packs, drives and controllers is about the only method which will enable the user to isolate the trouble down to a particular assembly. Errors which appear at the same disk address on multiple passes of the diagnostic are typical of disk pack problems. A good system with an error-free pack can be expected to run overnight with zero errors detected by this program. Bad or marginal blocks when flagged bad by the formatter diagnostic utility will be skipped over by the performance exerciser. Additional marginal blocks may be flagged bad by running the format diagnostic starting at LOC 204 and specifying those blocks. The complete format program must be rerun to mark these sectors bad and record the same in the bad block table.

5.5.2.9 Troubleshooting Flow Chart

The flow diagram of Figure 5.1 summarizes the steps which should be used to try to isolate system problems before any vendors are contacted. Data collected during this procedure (essentially the same as previously described) will be important to the resolution of the difficulty.

FIGURE 5.1


FLOW DIAGRAM
INSTALL SYSTEM, APPLY POWER
LIGHTS REMAIN LIT?
NO
YES
REMOVE DRIVE CABLES, READ REGISTERS BACK ON UNIBUS
REMOVE DRIVE CABLES, APPLY POWER
LIGHTS REMAIN LIT?
NO
CHECK DRIVE & CABLES, RESTART TESTS
YES
AGREE WITH TABLE 7.1?
NO
CHECK +5V VOLTAGE ON BOARD
STILL BAD?
RUN HOST PROCESSOR DIAGNOSTICS
TRY ANOTHER SLOT
RETURN BOARD TO DRC
YES
CONNECT DRIVE CABLES, READ BACK REGISTERS
AGREE WITH TABLE 7.1?
NO
CHECK DRIVE CONFIG., RING OUT CABLES
YES
BUS ACLO-L BUS DCLO-L WITH SCOPE
BOTH HIGH?
NO
WIRE CHASSIS PROPERLY, RESTART TESTS
YES
CHECK 5.0 VOLTS ±100 MV AT ON S34 BOARD
RETURN DEFECTIVE S34 TO DRC
YES
GOOD?
NO
ADJUST BACK-PLANE SUPPLY, RESTART TESTS
RUN FORMATTER PROGRAM
B
YES
DOES IT COMPLETE ?
NO
TRY A "WRITE HEADER AND DATA" COMMAND
GO BIT REMAIN SET?
YES
CHECK FOR WRITE AND SERVO CLOCKS IN "B" CABLE SECTOR AND INDEX PULSES IN "A" CABLE
CALL DRIVE VENDOR IF PROBLEMS SEEN
NO
EXAMINE COMPLETION STATUS IN CS1, CS2, ER1, ER2
OK?
NO
CHECK CABLES AND DRIVE CONFIGURATION
YES
RUN PERFORMANCE EXERCISER
PASS?
YES
COMPLETE INSTALLATION
NO
TRY A READ OF THE DATA
TRY A WRITE CHECK OF THE DATA
YES
STATUS GOOD?
NO
WRITE CHECK ERROR?
YES
PUT IN LOOP, CHECK WRITE AND READ DATA LINES & CLOCKS IN B CABLE. FIRST WRITE, THEN READ
NO
B
CLOCKS PRESENT?
NO
YES
DATA PRESENT?
NO
CALL DRIVE VENDOR
YES
B
HAS THIS S34 RUN ON ANOTHER DRIVE?
NO
HAS THIS DRIVE RUN ON ANOTHER CONTROLLER?
YES
CONCENTRATE ON CABLE/CONTROLLER PROBLEMS
RING OUT CABLES
CABLES PLUGGED INTO DRIVE OK?
GROUND CABLE ATTACHED PROPERLY?
"A" CABLE TERMINATED PROPERLY?
CORRECT PACK TYPE?
CORRECT DRIVE CONFIGURATION?
SECTOR CARD INSTALLED?
DRIVE WRITE PROTECTED?
YES
CONCENTRATE ON DRIVE/CABLE PROBLEMS
RING OUT CABLES
USE SCOPE TO LOOK FOR DATA SIGNALS ON B CABLE
TRY ANOTHER S34
DOES THIS WORK?
NO
YES
REPLACE CABLES
TRY ANOTHER DRIVE
TRY ANOTHER CPU SYSTEM
?
RETURN S34
DRIVE FAULT LIGHT LIT?
YES
CHECK CABLES
IDENTIFY INTERNAL DRIVE FAULT LIGHT CAUSING THE FAULT
IS IT A DRIVE FAULT I.E., VOLTAGE, SPEED, SEEK INC. ?
YES
CALL IN DRIVE VENDOR TO FIX DRIVE
NO
CALL DRC
NO
TRY NEW "B" CABLE
TRY NEW "A" CABLE
TRY ANOTHER PORT IF DUAL PORTED DRIVE
PORT SWITCHES ON DRIVE CARDS ENABLED?
INDEX, SECTOR PULSES IN "A" CABLE, NOT "B" CABLE?
SCOPE S34 END OF "B" CABLE FOR CLOCKS
SCOPE DRIVE FOR PROPER CLOCKS AND SEEK COMPLETIONS
REPLACE DRIVE
?

5.6 Option Jumpers and Switches (See Figure 5.2)

5.6.1 Drive Configuration

The table below shows the proper settings of SW3 and SW5 for different drive sizes. Any "B" cable can be plugged into any of the four controller plugs. The physical drive unit number set by a plug or switches on each drive will be used by the controller along with SW3 and SW5 to determine drive type.

SWITCH NO.	SWITCH POSITION	PHYSICAL DRIVE NO.
SW3	8 7 6 5	0
SW3	4 3 2 1	1
SW5	8 7 6 5	2
SW5	4 3 2 1	3
DRIVE TYPE	- - - -	EMULATION
80MB SMD	* ON ON ON	1 - RM02
160MB SMD	* ON ON OFF	2 - RM02's
300MB SMD	* ON OFF ON	1 - RM05
84MB M2312	* ON OFF OFF	1 - RM02
330MB M2294	* OFF ON ON	1 - RM05

(Other combinations reserved)
For logical number - see note ##

OFF = OPEN
ON = CLOSED
* = INTERLEAVE OPTION ON FORMAT
ON = NO INTERLEAVE OFF = 2:1 INTERLEAVE

##NOTE: Logical drives are numbered consecutively starting with drive zero. 160 MByte drives emulate two logical drives; all other drive sizes emulate one logical drive. In units with no 160 MByte drives logical unit numbers are equal to physical unit numbers. In systems with 160 MByte drives this is not true. For example, consider a system as follows:

PHYSICAL DRIVE NO.	DRIVE TYPE	LOGICAL DRIVE NO.
0	Not 160 MB	0
1	160 MB	1,2
2	Not 160 MB	3

5.6.2 NPR Burst Size and Off Time

The maximum burst size per NPR is set by SW4. This burst size is automatically reduced (throttled) if other NPR's or BR's become active during a transfer. When E2-1 to E2-2 is jumpered, throttle is enabled and when E2-1 to E2-2 is removed, the throttle is disabled and all bursts will be the selected maximum size. The standard burst is size is 16 words.

When the burst is completed but more data is still to be transferred SW6 determines the wait or "Off Time" before the next request is made. The standard Off Time is 3 usec.

DMA BURST SIZE

SW4	1	2	3	4	5	6	7	8	Set 1 and only 1.
WORDS/BURST	1	2	4	8	16	32	64	128	Switch to ON (or CLOSED)

(STD)

NPR OFF TIME

SW6	*	8	7	6	5	1	2	3	4	Set None or only 1.
uSEC OFF	0	3	6	12	24	48	96	192	398	Switch to ON (OR CLOSED)

(STD) * NO SWITCH ON (OR CLOSED)

	E2-1 to E2-2
ENABLE THROTTLE (STD)	IN
DISABLE THROTTLE	OUT

For further discussion of these settings and there effects on performance see Section 7.5, Theory of Operation.

5.6.3 CSR Address

The standard RH11 Bus Address for CS1 is 776700_8 and is set by SW1. Alternate addresses may be switch selected in the range of 760000_8 to 777700_8. CSR address must end in 00_8.

ADDRESS BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
SW1	--	--	--	1	2	3	4	5	6	7	*8	-	-	-	-	-
776700	1	1	1	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	Ø	Ø	Ø	Ø	Ø
777400	1	1	1	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	Ø	Ø	Ø	Ø	Ø
776300	1	1	1	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	Ø	Ø	Ø	Ø	Ø

*SW1-8 MUST BE ON.

OFF = Open and is equal to "1".
ON = Closed and is equal to "Ø".

5.6.4 Vector Address

The standard RH11 Interrupt Vector is 254_8. This is set by SW2. Alternate vectors may be switch selected in the range of Ø to 374_8.

VECTOR BIT	-	7	6	5	4	3	2	1	0
SW2	-	6	5	4	3	2	1	-	-
VECT = 254	Ø	OFF	ON	OFF	ON	OFF	OFF	Ø	Ø
VECT = 210	Ø	OFF	ON	ON	ON	OFF	ON	Ø	Ø
VECT = 150	Ø	ON	OFF	OFF	ON	OFF	ON	Ø	Ø

OFF = Open and is equal to a "1".
ON = Closed and is equal to a "Ø".

5.6.5 Interrupt Priority

The standard RH11 Interrupt Priority is BR5 and is implemented in jumpers (E1). Other priority levels from BR4 to BR7 are jumper selectable.

Priority	Add E1 Jumpers as below, and remove all others in E1.
BR4	13-1, 14-5, 15-6, 7-8, 9-10, 11-12
BR5	13-2, 14-7, 15-8, 5-6, 9-10, 11-12
BR6	13-3, 14-9, 15-10, 5-6, 7-8, 11-12
BR7	13-4, 14-11, 15-12, 5-6, 7-8, 9-10

5.6.6 Dual Port Enable

Dual port features for drives so equipped:

	E7-1 to E7-2	E7-2 to E7-3
ENABLE DUAL PORT	IN	OUT
DISABLE DUAL PORT	OUT	IN

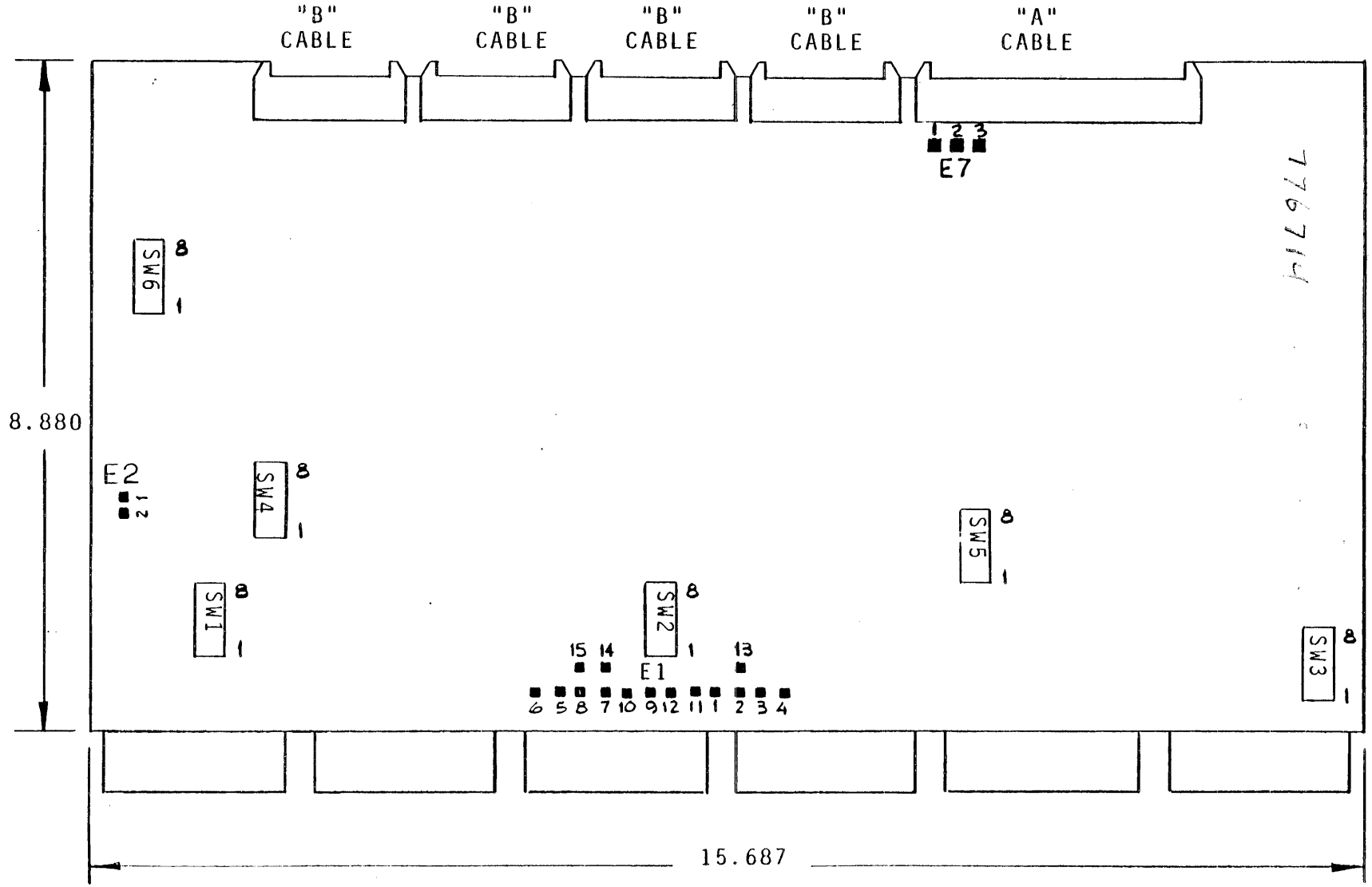

"B" CABLE
"B" CABLE
"B" CABLE
"B" CABLE
"A" CABLE
E7
1 2 3
SM6
SM4
SM1
SM2
SM5
SM3
8
1
E2
2 1
E1
15 14 13
6 5 8 7 10 9 12 11 1 2 3 4
8.880
15.687
77671

FIGURE 5.2

6.0 PROGRAMMING

6.1 Command Codes

Software initiates operations by selecting a drive, loading the control register with a function code and setting the GO bit. The function code specifies the command to be executed upon assertion of the GO bit. The commands can be divided into three categories: positioning commands, data transfers, and housekeeping operations. These commands and their corresponding octal functions are listed below.

Positioning Commands	Function Codes (Octal)
Seek	5
Recalibrate	7
Offset	15
Return to Centerline	17
Search	31

Data Transfer Commands	Function Codes (Octal)
Write Check Data	51
Write Check Header and Data	53
Write Data	61
Write Header and Data (Format)	63
Read Data	71
Read Header and Data	73

Housekeeping Operations	
No-Op	1
Drive Clear	11
Release	13
Read-In Preset	21
Pack Acknowledge	23

6.1.1 Positioning Commands

Positioning commands are used by the software to position the heads over the disk pack.

Seek* - Causes the heads to be moved to the cylinder address specified by the desired cylinder register (RMDC). The current cylinder equals the desired cylinder upon the completion of the command.

Recalibrate* - Positions the heads over cylinder zero.

Offset* - Allows the heads to be moved off the track centerline 200 microinches toward the spindle (positive offset) or away from the spindle (negative offset).

Return to Centerline* - Returns the heads to track centerline after an offset operation.

Search - A Seek command combined with a search for the desired sector address. Used to synchronize software with the desired disk address.

*Since the S34/A utilizes a daisychained control cable to the disk drives, positioning commands for one drive cannot be executed concurrently with data transfers to or from another drive. Therefore, the Seek, Recalibrate, Offset, and Return to Centerline commands are simulated logically with proper status for the software, but the physical positioning is deferred and completed with the next search or data transfer command. Recalibrate functions are completed automatically by the S34/A whenever a drive fault or seek error is encountered.

6.1.2 Data Transfer Commands

These commands transfer data to or from the disk and require the completion of a positioning command or an implied seek as part of the data command.

Read Header and Data - Transfers two words of header information and 256 data words per sector from the disk pack to the PDP-11. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred.

Read Data - Transfers 256 data words per sector from the disk pack to the PDP-11. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred.

Write Check Header and Data - Compares two words of the header and 256 words of data per sector from the disk to 258 words of data per sector from memory. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred or compared.

Write Check Data - Compares 256 words of data per sector from the disk to 256 words of data per sector from memory. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred or compared.

Write Data - Transfers 256 words of data per sector to the drive. If an error is detected in a header, the command will abort following the header CRC check and no further data is transferred.

Write Header and Data - Also referred to as a "format", this command writes all gaps, headers, and data for specified sector(s) including the sync byte, CRC and ECC.

6.1.3 Housekeeping Commands

These commands are used to place the drive logic into a known or initial state.

No-Op - Resets the GO bit. Considered a filler command.

Drive Clear - Clears bits in the following registers:

Status (RMDS)	Bit 14 (ERR) Bit 15 (ATA)
Error No. 1 (RMER1)	All Bits
Error No. 2 (RMER2)	All Bits
Attention Summary (RMAS)	All Bits (for the selected drive)
Maintenance No. 1 (RMAS)	All Bits
ECC Pattern (RMEC2)	All Bits

The drive clear command also clears all error indications in the drive provided the error condition no longer exists.

Release - Logically releases the dual-ported drive for use by the other port. The S34/A physically releases the drive upon completion of each command which required a drive selection for execution. Therefore the Release command is a logical emulation of a function previously completed.

Read-In Preset - Sets the volume valid (VV) bit (06) in the status register (RMDS), clears all bits in the desired sector/track address register (RMDA) and all bits in the desired cylinder address register (RMDC); clears the offset mode and the following bits in the offset register (RMOF):
OFD (Bit 07) - Offset Direction
HCI (Bit 10) - Header Compare Inhibit
ECI (Bit 11) - Error Correction Code Inhibit
FMT16 (Bits 12) - Format (CLRS 16 BIT FMT)

Pack Acknowledge - Sets the volume valid (VV) bit (06) in the status register (RMDS). This command must be issued before any data transfer or positioning commands can be given if the drive has gone off-line and then on-line (i.e., if MOL changes state). It is primarily intended to avoid unknown pack changes.

6.2 Controller Registers

Twenty registers are visible to software and emulated by the controller to communicate control commands, status data, error conditions, and maintenance information. See Table 6.1.

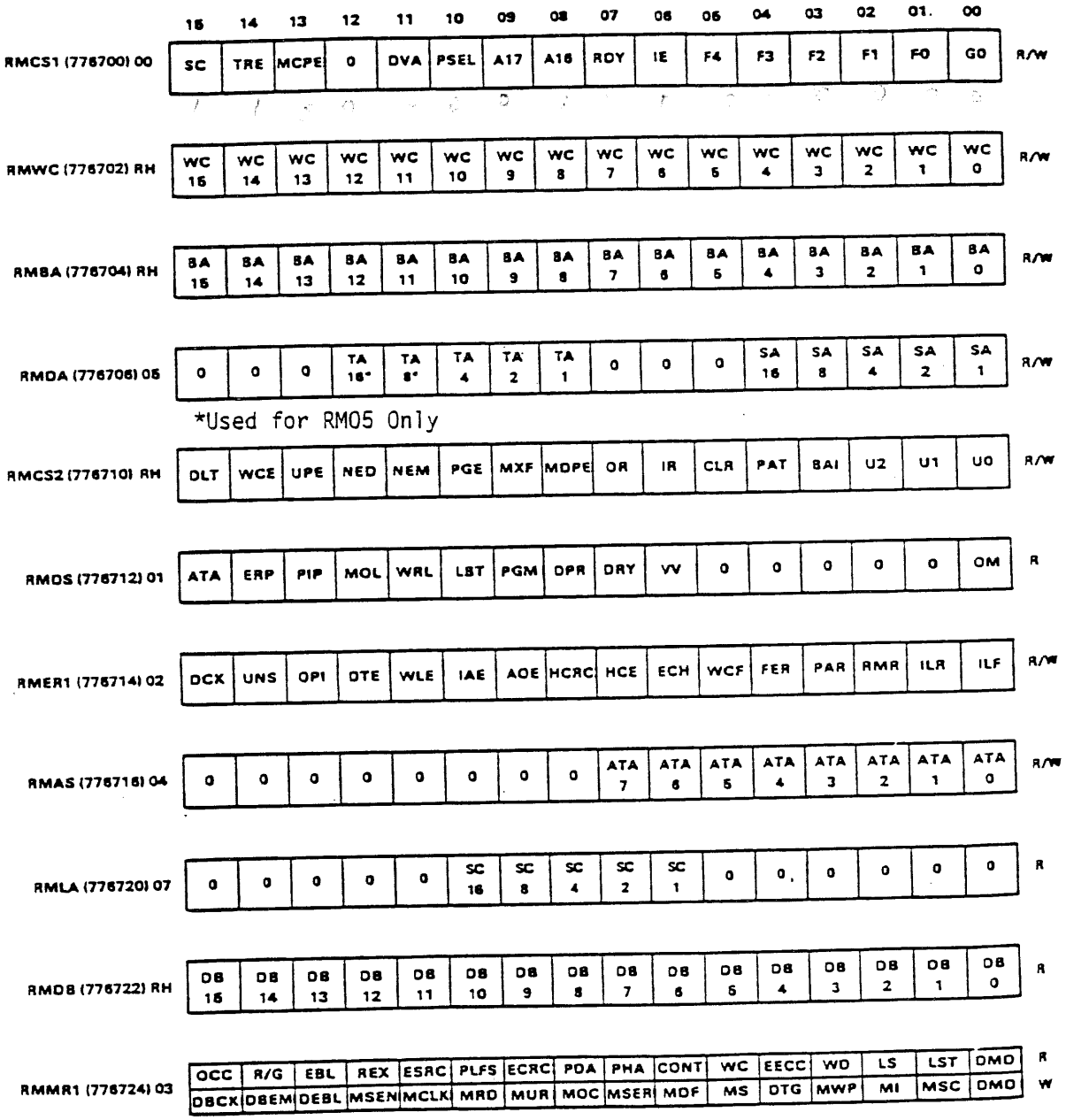
Specific bit locations in these drive registers are designated as follows:

- Read Only indicates that software can read the bits, but cannot load them.
- Write Only indicates that software can load the bits, but will read back a zero.
- Read/Write indicates that software may load and read the bits back.

Table 6.2.1 and the paragraphs that follow define these registers their mnemonics, their UNIBUS addresses, whether they are Read Only or Read/Write, and their basic function.

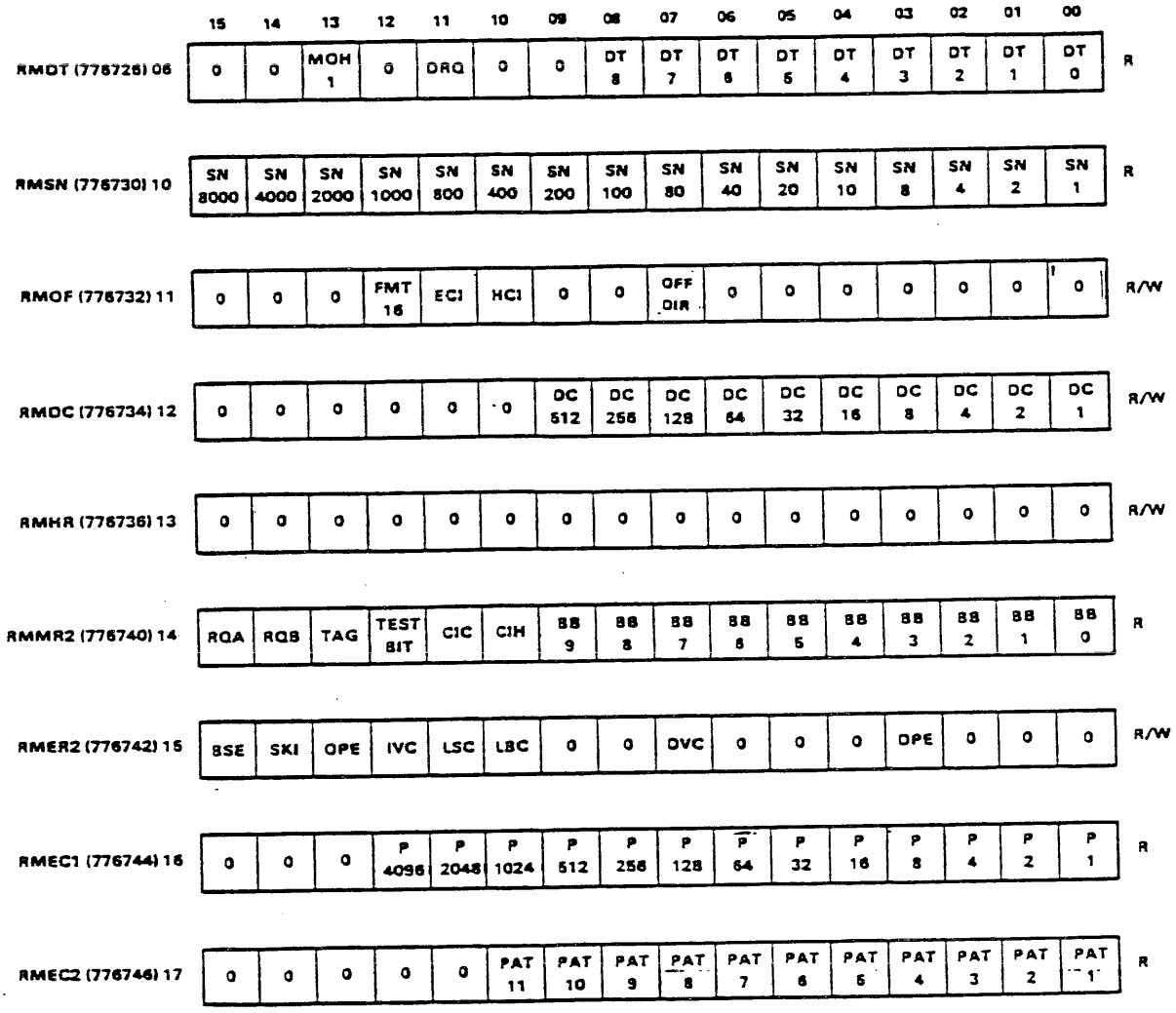
6.2.1 Control Register (RMCS1) (776700)

This register is utilized by the controller to store the disk commands and operational status. The function (command) code designates a function for the drive selected in bits 00 through 02 of the RMCS2 register. Setting the GO bit causes the controller to execute the function code in the control register.



REGISTER SUMMARY, RM05/2 EMULATION

Table 6.1



REGISTER SUMMARY (Continued)

Table 6.1

Bits 00-05 GO and Function (GO, FO-F4) - Read/Write

GO bit and FO-F4 establish the function (command) code control bits that determine the action performed by the controller as shown below.

F4	F3	F2	F1	FO	GO	Octal	
0	0	0	0	0	1	01	No Operation
0	0	0	1	0	1	05	Seek Command
0	0	0	1	1	1	07	Recalibrate
0	0	1	0	0	1	11	Drive Clear
0	0	1	0	1	1	13	Release (Dual-Port Operation)
0	0	1	1	0	1	15	Offset Command
0	0	1	1	1	1	17	Return to Centerline
0	1	0	0	0	1	21	Read-In Preset
0	1	0	0	1	1	23	Pack Acknowledge (Set V.V.)
0	1	1	0	0	1	31	Search Command
1	0	1	0	0	1	51	Write Check Data
1	0	1	0	1	1	53	Write Check Header and Data
1	1	0	0	0	1	61	Write Data
1	1	0	0	1	1	63	Write Header and Data
1	1	1	0	0	1	71	Read Data
1	1	1	0	1	1	73	Read Header and Data

The GO bit (bit 0) must be set to cause the controller to respond to a command. The GO bit is reset after command execution. All other commands are illegal (ILF).

Bit 06 Interrupt Enable (IE) - Read/Write

IE is a control bit that can be set only under program control. When IE=1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled. A program-controlled interrupt may occur by writing 1's into IE and RDY at the same time.

Bit 07 Ready (RDY) - Read Only

This bit is normally set except during data transfers when it is reset. When a data transfer command code (51-73) is written into RMCS1, RDY is reset. At the termination of data transfer, RDY is set.

Bits 08-09 UNIBUS Address Extension (A16,A17) - Read Write

Upper extension bits of the RMBA register. Cleared by INIT, controller clear, or by writing 0's in these bit positions. These control bits cannot be modified while the controller is performing a data transfer (RDY negated).

Bit 10 Port Select (PSEL) - Read/Write

When PSEL=0, data transfer is via UNIBUS A. Cleared by UNIBUS INIT, controller clear, or by writing a 0 in this bit position. The controller only supports Port A operation; therefore, the bit must be 0 and, in addition, cannot be modified while the RH controller is performing a data transfer (RDY negated).

Bit 11 Drive Available (DVA) - Read Only

This bit is used in dual-port disk configurations and set when the drive is not busy on the other port. Since dual port operation is transparent to the operating system this bit is always 1.

Bit 12 Spare

Bit 13 MASSBUS Control Bus Parity Error (MCPE) - Read Only

Set when a simulated parity error is forced by a diagnostic while reading a register logically located in the drive. Cleared by UNIBUS INIT, controller clear, RH error clear, or by loading a data transfer command with the GO bit set. Simulated parity errors while writing a register logically located in a drive cause the PAR error (RMER1 register, Bit 03) to set.

Bit 15 Special Condition (SC) - Read Only

Set by TRE or ATTN or MCPE bits. Cleared by UNIBUS INIT, controller clear, or by removing the ATTN condition.

6.2.2 Word Count Register (RMWC) (776702)

The word count register is loaded by the program with the 2's complement of the number of words to be transferred. During a data transfer, it is incremented by 1 each time a word is transmitted to or from memory. A maximum of 65,535 words can be transferred at one time. It is cleared only by writing zeros into it.

6.2.3 Address Register (RMBA) (776704)

This register is used by the controller to address the memory location in which a transfer is to take place. The register contains the lower 16 bits of address which combine with Bit 09 and 08 of the control register RMCS1 to create the 18-bit memory address. This register is loaded by the program with the starting memory address. Each time a DMA transfer is made, the register is incremented by 2. If the BAI (Bus Address Increment Inhibit) bit (bit 03 of RMCS2) is set, the incrementing of the register is inhibited and all transfers take place to or from the starting memory address. It is cleared by a UNIBUS INIT or by controller clear.

6.2.4 Sector/Track Address Register (RMDA) (776706)

This register is used to address the sector and track on the disk to or from which a transfer is desired. The RMDA register is associated with the drive whose unit number appears in bits 00:02 of the status register RMCS2. Before a transfer, the RMDA is loaded by the program with the address of the first block to be transferred. The RMDA is incremented each time a block of data has been transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred.

The RMDA register contains a 5-bit sector address providing for 32 sectors per data track. The register also contains a 3-bit track address for RM02 and 5-bit track address for RM05 providing for 5 or 19 data tracks, respectively. The sector and track addresses are non-contiguous. However, when the sector count fills up with a count of 31, the next word read or written will cause the track address to increment and the sector address to clear. When the sector address and track addresses reach their full counts, the next word will cause both sector and track addresses to increment to 0 and a mid-transfer seek to occur. The RMDA register can only be loaded with a 16-bit word. Any attempt to write a byte causes the entire word to be written. Any attempt to write in this register while the drive's GO bit is asserted will cause an RMR (Register Modify Refused) error (RMER1, Bit 02) and the register is not modified.

Bits 00-04 Sector Address - Read/Write

Set by the program to specify the sector on which a transfer is to start. Cleared by read in preset command. Incremented after each sector has been transferred.

Bits 05-07 Spare

Bits 08-12 Track Address - Read/Write

Set by the program to specify the track on which a transfer is to start. Cleared by read in preset command. Incremented when sector 31 is reached.

Bits 13-15 Spare

6.2.5 Status Register (RMSC2) (776710)

This Read/Write register indicates the status of the controller and contains the drive unit number. The unit number specified in Bits 00 thru 02 of this register indicates which of the possible eight logical drives is selected.

Bits 00-02 Unit Select - Read/Write

These bits are written by the program to select a drive. Cleared by UNIBUS INIT or controller clear. The unit select bits can be changed by the program during data transfer operations without interfering with the transfer.

Bit 03 Bus Address Inhibit (BAI) - Read/Write

When BAI is set, the controller will not increment the RMBA register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by UNIBUS INIT or controller clear.

Bit 04 Parity Test (PAT) - Read/Write

This bit is used by the controller to simulate a MASSBUS Data Bus Parity Error (MDPE) to support diagnostic programs. Cleared by UNIBUS INIT or controller clear.

Bit 05 Controller Clear (CLR) - Write Only

When a 1 is written into this bit, the controller is initialized. UNIBUS INIT also causes controller clear to occur.

Bit 06 Input Ready (IR) - Read Only

Set when a word may be written in the RMDB register by the program. Cleared by reading RMDB register. Serves as a status indicator for diagnostic check of the silo buffer. An attempt to write the RMDB register before IR is asserted will cause a Data Late Error (DLT). Used for diagnostic mode only.

Bit 07 Output Ready (OR) - Read Only

Set when a word is present in RMDB and can be read by the program. Cleared by UNIBUS INIT, controller clear, or by reading the RMDB register. Serves as a status indicator for diagnostic check of the silo buffer. An attempt to read the RMDB register before OR is asserted will cause a Data Late Error (DLT). Used for diagnostic mode only.

Bit 08 MASSBUS Data Bus Parity Error (MDPE) - Read Only

Set when a simulated parity error is forces by a diagnostic while doing a read or write-check operation. Cleared by UNIBUS INIT, controller clear, or loading a data transfer command with GO set. MDPE causes a transfer error (Bit 14 of RMCS1 sets). Simulated parity errors during write operations are detected by the drive and cause the PAR error (RMER1 register, Bit 03).

Bit 09 Missed Transfer (MXF) - Read/Write

MXF causes a transfer error (Bit 14 of RMCS1 sets). This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive that has ERR (Bit 14 of RMDS set). Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set.

Bit 10 Program Error (PGE)

Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by UNIBUS INIT, controller clear, or loading a data transfer command with GO set. PGE causes a transfer error (Bit 14 of RMCS1 sets). The data transfer command code is inhibited from being written.

Bit 11 Non-Existent Memory (NEM) - Read Only

Set when the controller is performing a DMA transfer and the memory address specified in RMBA is non-existent (does not respond to MSYN within 20us). Cleared by Q-BUS INIT, controller clear, or loading a data transfer command with GO set. NEM causes a transfer error (Bit 14 of RMCS1 sets). The RMBA contains the address +2 of the memory location causing the error.

Bit 12 Non-Existent Drive (NED) - Read Only

Set when the program reads or writes a drive register in a drive that does not exist or is powered down. Cleared by UNIBUS INIT, controller clear, or loading a data transfer command with GO set. NED causes a transfer error (Bit 14 of RMCS1 sets).

Bit 13 UNIBUS Parity Error (UPE) - Read/Write

Set if the UNIBUS parity lines indicate a parity error while the controller is performing a write or write-check command. Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set. UPE causes a transfer error (Bit 14 of RMCS1 sets). When a UNIBUS parity error occurs, the RMBA register contains the address +2 of the memory word with the parity error (if BAI (Bit 03 of this register) is not set). This bit may be set by program control for diagnostic purposes.

Bit 14 Write Check Error (WCE) - Read Only

Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set. WCE causes a transfer error (Bit 14 of RMCS1 sets). If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RMBA (and extension) is the address of the word following the one that did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RMDB).

Bit 15 Data Late (DLT) - Read Only

Set only by the program reading or writing the RMDB register. DLT causes a transfer error (Bit 14 of RMCS1 sets). Cleared by UNIBUS INIT, controller clear, or loading a data transfer command GO set. Used for diagnostic mode only.

6.2.6 Drive Status Register (RMDS) (776712)

This Read-Only register contains the various state indicators for the selected drive. The status indicators displayed are those of the drive that is specified by the unit select bus (00:02) of the RMCS2 register. The register is a Read-Only register. Writing into this register will not cause an error and will not modify any of the status bits.

Bit 00 Offset Mode (OM) - Read Only

Set when an offset command is issued to the controller; reset by any of the following seven actions:

1) Power-Up
2) Mid-Transfer Seek
3) Read-In Preset
4) Write Data or Write Header and Data Command
5) Return to Centerline
6) Writing Desired Cylinder
7) Recalibrate Command

When set and a read command is received, the offset is performed prior to the execution of the read.

Bits 01-05 Spare

Bit 06 Volume Valid (VV) - Read Only

Set by the pack acknowledge or read-in preset commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates when the drive has been put off-line and on-line and a disk pack may have been changed. Therefore, the program should not assume anything about the identity of the pack.

Bit 07 Drive Ready (DRY) - Read Only

Set at the completion of every command, data handling, or mechanical motion. Cleared at the initiation of a command. When set, this bit indicates the readiness of the controller to accept a new command involving data handling or mechanical motion of the drive. If a Read or Write command was issued, the setting of the DRY bit will indicate normal termination. If an error was made during the data transfer, the appropriate error bits and Bit 15 (ATA) of this register will also be set.

If a mechanical movement command was issued, the ATA bit will also be set when DRY is set. If an error occurs during the mechanical movement, the appropriate error bits will also be set.

The DRY bit is the complement of the GO bit. (DRY=GO negated) This is true except when the drive in non-existent; then the DRY bit is reset.

Bit 08 Drive Present (DPR) - Read Only

Always set to "one", if drive is connected and powered on.

Bit 09 Programmable (PGM) - Read Only

In the S34/A controller, this bit will always be reset to "zero".

Bit 10 Last Block Transferred (LBT) - Read Only

After reading or writing sector 31 of cylinder 882 on track 4, the LBT bit is set. With this bit set, the desired cylinder address register contains 823 (illegal address), and the desired sector track address register contains 0. Cleared when a new track or sector address is received. Also cleared during power-up cycle.

Bit 11 Write Lock (WRL) - Read Only

The drive is placed in write protect mode through a manual switch on the drive control panel. When the drive is write protected, any attempt by the operating system to issue a write command to a write-locked device will cause the write lock error (WLE, Bit 11 of RMER1) bit to set. Cleared when the PROTECT switch is not depressed (PROTECT light extinguished).

Bit 12 Medium On-Line (MOL)

After the drive power-up cycle, the heads are positioned over cylinder zero and the MOL bit is set. Whenever the MOL bit changes state (set or reset), Bit 15 (ATA) of this register is also set, except when the heads are unloaded. MOL is cleared when the heads are unloaded.

Bit 13 Positioning in Progress (PIP) - Read Only

Set when a positioning command is accepted. These commands are seek, offset, return to centerline, recalibrate, and search. In addition, PIP is set whenever MOL is reset and drive is powered up. Cleared when the function is completed.

The following chart shows the state of the PIP bit in relation to the type of operation being performed.

Operation	DRY	PIP	ATA at End of Operation (No Error)
No Operation	0	0	NO
Recalibrate	0	1	YES
Drive Clear	0	0	NO
Search	0	0/1	YES
Seek	0	1	YES
Offset	0	0	YES
Write Check	0	0	NO
Write Data	0	0	NO
Write Header and Data	0	0	NO
Read Data	0	0	NO
Head Header and Data	0	0	NO
Implied Seek	0	1	NO
Mid-Transfer Seek	0	1	NO
Return to Centerline	0	0	YES
Pack Acknowledge	0	0	NO
Read-In Preset	0	0	NO
Offset During Read	0	1	NO

Bit 14 Error (ERR) - Read Only

A composite error bit that is the logical OR of all drive error conditions. While ERR is set, only clearing commands are accepted. Set when either of the error registers (RMER1 or RMER2) indicates a drive error. Cleared by drive clear, INIT, writing 0's in error registers or during a power-up cycle.

Bit 15 Attention Active (ATA) - Read Only

Set when a drive attention condition exists as follows:

1. Any error in the error register:
   a) If the GO bit is set; at the completion of the command.
   b) If the GO bit is reset; at the occurrence of the error.
2. At the completion of seek, search, recalibrate, offset, or return to centerline.
3. When the MOL bit changes state.

These conditions are cleared by the following:

1. Drive clear command
2. Writing a 1 into the attention summary register (RMAS)
3. INIT command
4. Writing a 1 into the GO bit if no error condition exists

6.2.7 Error Register No. (RMER1) (776714)

This register contains the error status indicators for the drive whose unit number appears in Bits 00 through 02 of RMCS2. The logical OR of all the error bits in the RMER1 and RMER2 registers will be written into Bit 14 of RMDS.

The RMER1 register is a read/write register and can only be written as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy (GO bit is asserted), an RMR (RMER1 register, bit 02) error is set and the contents of the RMER1 register are not otherwise modified.

Errors can be classified into two categories: Class A and Class B.

- A Class A error is handled at the completion of a non-data transfer command or, in the case of a data transfer command, at a sector boundary.

- o A Class B error causes the command to terminate immediately or as soon as possible.

Bit 0 Illegal Function (ILF) - Read/Write

ILF is a Class B error set when the GO bit is set, there is no previous error, and the function code in the control register does not correspond to a valid drive command. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 01 Illegal Register (ILR) - Read/Write

ILR is a Class A error set when a read or write is attempted on a register address greater than 17. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 02 Register Modify Refused (RMR) - Read/Write

RMR is a Class A error set when a write is attempted into any register (exept RMAS or RMMR1) while the GO bit is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register. The following registers can be written into before or after an operation, but not during.

- o Control Register
- o Error Registers
- o Maintenance Register No. 1
- o Attention Summary Register
- o Desired Sector/Track
- o Address Register
- o Offset Register
- o Desired Cylinder Address Register

The remaining drive registers are read-only registers. When RMR is set, the drive continues to execute the command in progress.

Bit 03 Parity Error (PAR) - Read/Write

This function is not fully emulated. It is set to zero, except when performing a parity test (PAT of RMCS2). Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 04 Format Error (FER) - Read/Write

FER is a Class A error during a read header and data command and a Class B error during all other commands.

Set when reading a sector header if Bit 10 (HCI) of RMOF register is reset and Bit 12 of the first header word does not match the state of Bit 12 (FMT) of RMOF register. Cleared by drive clear, INIT, power-up cycle, or writing 0's in this register.

Error usually indicates that pack and drive are incompatible in data word length (e.g., drive configured for 16-bit format and an 18-bit format pack installed). The S34/A controller will not accommodate 18 bit operations.

Bit 05 Write Clock Fail (WCF) - Read/Write

Always a zero.

Bit 06 ECC Hard Error (ECH) - Read/Write

ECH is a Class B error set at the conclusion of the error correction procedure (Bit 15 of this register is set), indicating that the error was an uncorrectable error. Cleared by drive clear, INIT, power-up cycle, or writing 0's into this register.

Bit 07 Header Compare Error (HCE) - Read/Write

HCE is a Class A error during a read header and data command and a Class B error during all other commands.

Set if Bit 10 (HCI) of RMOF register is reset and one or more of the following occurs while reading the header.

- o Bits 0-9 of the first header word do not match bits 0-9 of the desired cylinder address register (RMDC).
- o Bit 12 of the first header word does not match Bit 12 (FMT) of the offset register (RMOF).
- o Bits 0-5 of the second header word do not match bits 0-5 of the desired track and sector (RMDA) register.
- o Bits 8-10 of the second header word do not match Bits 8-10 of the desired track and sector (RMDA) register.

- Bits 14 and 15 must be 1's; otherwise BSE is set.
- Any bit other than those specified above that is not a zero in either the first or second word of the header.

Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 08 Header CRC Error (HCRC) - Read/Write

HCRC is a Class A error during a read header and data command and a Class B error during all other commands. Set if Bit 10 (HCI) of RMOF is reset and the CRC register in the controller is not zero after the complete header has been read. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 09 Address Overflow Error (AOE) - Read/Write

AOE is a Class B error set when the controller requests a data transfer (read or write) beyond the last sector of the last cylinder of the pack. This results in a cylinder address overflow condition. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 10 Invalid Address Error (IAE) - Read/Write

IAE is a Class B error which causes the command to terminate when the GO bit sets. Set if the contents of either desired cylinder register (RMDC) or desired sector/track address register (RMDA) are invalid and at the receipt of one of the following commands.

- Seek
- Search
- Read Header and Data
- Read Data
- Write Check Header and Data
- Write Check Data
- Write Header and Data
- Write Data

Invalid addresses are: desired cylinder greater than 822; desired track greater than 4 (18 for RM05); desired sector greater than 31. Cleared by drive clear, INIT, power-up cycle or by writing 0's into this register.

Bit 11 Write Lock Error (WLE) - Read/Write

WLE is a Class B error set if a write command is issued when the drive is in the write lock mode. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 12 Drive Timing Error (DTE) - Read/Write

DTE is a Class B error which is not fully emulated. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 13 Operation Incomplete (OPI) - Read/Write

OPI is a Class B error set if either of the following occurs:

1. During a Search command, the correct sector is not located within three revolutions of the disk.
2. If MOL is reset and a command is attempted, it will not execute.

Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 14 Unsafe Drive (UNS) - Read/Write

Set when Bit 07 (DVC) of RMER2 is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

Bit 15 Data Check Error (DCK) - Read/Write

DCK is a Class A error if Bit 11 (ECI) of RMOF is set and a Class B error if ECI is reset. Set after reading the entire data field of the sector if the ECC register bits 11-31 are non-zero. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

6.2.8 Attention Summary Register (RMAS) (776716)

The Attention Summary Register allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention status for a selected group of drives. The bit displayed in each of the four low-order positions of this register is identical to the ATA bit displayed in RMDS for the corresponding drive. When

fewer drives are attached to the controller, the bits corresponding to the missing drives are always 0.

The ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number. (Loading a 0 has no effect.) This allows the program to inspect the RMAS register and later to rest the ATA bits that were set without accidentally resetting other ATA bits that may have become set in the meantime.

This register can be read or written at any time, regardless of whether any particular drive is busy. Note that the controller never asserts ATA during the execution of a command.

Bits 00-07 Attention Active (ATA 00-07) - Read/Write

The ATA bit for each drive is displayed in Bit 15 of RMDS for that drive and in the bit position corresponding to the unit number, e.g., the ATA bit for drive 02 corresponds to bit position 02 in RMAS.

Each bit sets when the corresponding ATA in RMDS is asserted. All bits are cleared by INIT or drive clear. Individual bits are cleared by writing function code with the GO bit to the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.

Bits 04-15 Not Used.

6.2.9 Look-Ahead Register (RMLA) (776720)

This Read Only register contains a simulation of the sector number currently positioned under the heads. This value is represented as a binary number in bit locations 6-10, where bit 6 is the LSB. The maximum count is 31.

Bits 00-05 Not Used. Always read as 0's.

Always read as 0's.

Bits 06-10 Sector Count (SC1,2,4,8,16) - Read Only

Simulates the sector number currently under the heads.

Bits 11-15 Not Used.

Always read as zeros.

6.2.10 Data Buffer Register (RMDB) (776722)

This Read/Write register is used to monitor the data buffer in the controller. If the program attempts to write into the data buffer while it is full or read the data buffer when it is empty, a data late (DLT) error occurs (Bit 15 of RMCS2 is set). The RMCS2 register also provides status indicators showing whether the data buffer can be read or written. When RMCS2 Bit 6 (IR) is set, the data buffer can be written. When RMCS2 Bit 7 (OR) is set, the data buffer can be read.

The RMDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the RMDB register is a "destructive" readout operation: the top data word in the buffer is removed by the action of reading the RMDB and a new data word (if present) replaces it a short time later. The action of writing the RMDB register causes one more data word to be inserted into the buffer (if it was not full).

Bits 00-15 Data Buffer (DB) - Read/Write

Used by the program for diagnostic purposes. When the register is written into, IR is cleared until the data buffer is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word is ready. During a write-check error condition, the data word read from the disk that did not compare with the corresponding word in memory is frozen in RMDB for examination by the program.

6.2.11 Maintenance Register No. 1 (RMMR1) (776724)

The emulation of the RMMR1 register in the S34/A provides a subset of the maintenance and diagnostic functions of the RM02. The register has two distinct 16-bit sections: a Read Only section and a Write Only section.

The Write Only section can be written only after the controller is set in the maintenance mode of operation (bit 00 set). The Read Only section can be read in both normal and maintenance operational modes.

Bit 00 Diagnostic Mode (DMD) - Read/Write

Set by a diagnostic program to configure the controller in the maintenance mode. Must be set before any other RMMR1 bits can be written. Cleared by Drive Clear, INIT, or power-up cycle. Also, when cleared, resets Bits 01-15 of this register.

Bits 01-15 Not Emulated

6.2.12 Drive Type Register (RMDT) (776726)

This Read Only register allows the program to distinguish between different classes of drives. The value returned by the S34/A is 20025_8 for single port RM02 and 20027_8 for single port RM05. Implementation of the dual port capability is transparent to the software.

Bits 00-08 Drive Type (DT) - Read Only

This 9-bit field contains a unique number assigned to each device type. This field contains 025_8 for RM02 and 027_8 for RM05.

Bits 09,10 Not Used. Always zero.

Bit 11 Drive Request Required (DRQ) - Read Only

The status of this bit indicates the availability of the dual port option. The S34/A returns a zero (single port). Dual port is handled by the Drive. Controller will wait until the Drive is not busy.

Bit 12 Not Used. Always zeros.

Bit 13 Moving Head (MOD) - Read Only

Since the RM02/RM05 is a moving head device, this bit is returned in the 1 state.

Bits 14,15 Not Used. Always zeros.

6.2.13 Serial Number Register (RMSN) (776730)

This Read Only register permits the program to distinguish between drives connected to the same controller. This information is useful during error logging of on-line software diagnostics to allow errors to be associated with a particular drive.

The serial number register in the S34/A is actually the logical unit number selected by software plus 100_8.

Bits 00-01 Serial Number (SN) - Read Only

These bits reflect the logical unit number of the drive currently selected by software.

Bits 02-15 Not Used.

Always zeros.

6.2.14 Offset Register (RMOF) (776732)

The controller has the ability to offset the drive carriage approximately 200 microinches from the track centerline in either direction.

The positioner offsetting information is supplied to the controller directly from the software operating system prior to the issuance of the offset command.

Bits 00-06 Not Used.

Always zeros.

Bit 07 Offset Direction (OFD) - Read/Write

Set when the offset direction is toward the spindle. When reset, the offset direction is away from the spindle. The offset direction bit is valid if the following three conditions are met:

1. Read command is loaded into control register (RMCS1) (Bits 0-5).
2. RMCS1 GO bit is set.
3. Offset mode bit (RMDS Bit 00) is set.

Cleared by Read-In Preset command or a software write to this register.

Bit 10 Header Compare Inhibit (HCI) - Read/Write

Set by the software program to inhibit the reporting of header compare errors FER, HCE, and HCRC (Bits 4, 7, and 8 respectively of RMER1). Cleared by a Read-In Preset command or by a software write to this register. The meaning of the HCI bit is valid in both the Read and Write commands. It is strongly recommended, however, that the HCI bit be reset during a Write operation.

Bit 11 Error Correction Inhibit (ECI) - Read/Write

Set by the software to prevent the isolation and correction of a data check error. Cleared by a Read-In Preset command or by a software write to this register.

If a data error is detected at the end of the data transmission in the Read mode with the ECI bit reset, the controller goes into the ECC correction process at the end of the sector. Prior to beginning the correction routine, the device will also set the data check (DCK) error bit RMER1 Bit 15, which will remain set until a drive clear command or an INIT pulse is received.

When the results of the error correction process are available, the device will place the error pattern and the location of the error pattern within the data field in the appropriate ECC registers.

If the error was non-ECC-correctable, the drive will also set the ECC hard error (ECH) bit. If the ECI bit is set, the error correction process will be inhibited. The termination procedure will be done normally as if no data error occurred. Only the DCK bit will be set as soon as a data error is detected. This bit will remain set until a Drive Clear or an INIT pulse is received.

Bit 12 Format (FMT) - Read/Write

Set to a 1 when 16-bit/word format is used (16 bits/word x 256 words/sector). Set to a 0 when 18-bit/word format is used (18 bits/word x 256 words/sector). Cleared by read-in preset command or by software write to this register. This bit is used by the S34/A only to achieve compatibility with diagnostic programs. All data operations to the disk are in 16 bit format.

Bits 13-15 Not Used.
Always zeros.

6.2.15 Desired Cylinder Register (RMDC) (776734)

The Read/Write register contains the address of the cylinder to which the drive carriage moves the heads for a Seek, Search or Data Handling command. Since the maximum number of cylinders in the RM05/2 is 823, only 10 bits are necessary to specify the desired cylinder address.

Bits 00-09 Desired Cylinder (DC) - Read/Write

Set by the program, the cylinder number to which the head will move. Bit DC1 is the least significant bit and bit DC512 is the most significant bit. Cleared by read-in preset. The invalid address error bit (RMER1 Bit 10) sets when, upon asserting the GO bit, the contents of the desired cylinder contain an address larger than 822.

Bits 10-15 Not Used.

Always zero.

6.2.16 Holding Register (RMHR) (776736)

This is an addressable register with no drive function. It is used only by diagnostic software. When writing into this register, all bits remain unchanged and new information is lost. When reading this register (or any illlegal register), the complement of the register contents is read. Whenever writing any legal register, this holding register is concurrently written.

6.2.17 Maintenance Register No. 2 (RMMR2) (776740)

The RMMR2 register operates in conjunction with the Maintenance Register No. 1. No bits of RMMR2 are emulated in the S34/A controller.

Bits 00-15 Not Used.

Always zeros.

6.2.18 Error Register No. 2 (RMER2) (776742)

This Read/Write register contains detailed error status information and is primarily used for monitoring the electromechanical performance of the drive. Whenever any of the bits in this register are set, the ERR bit (Bit 14) in the status register (RMDS) is set and the ATA bit in the RMAS register is set. All Error Register No. 2 errors are considered "catastrophic" errors.

All error bits reset when a drive clear command or an INIT pulse is received. If the heads are retracted from the disk pack upon receiving a drive clear or an initialize pulse, the drive attempts to reload the heads unless the error persists. Errors are classified into two categories: Class A and Class B.

- o A Class A error is handled at the completion of a non-data transfer command, or in the case of a data transfer command, at a sector boundary provided the Run line is inactive.
- o A Class B error is handled immediately and causes the immediate termination of a command or a termination as soon as possible.

Bits 00-02 Not Used.

Bit 03 Data Parity Error (DPE) - Read/Write

This bit is not emulated and will always be set to zero.

Bits 04-06 Not Used.

Always zeros.

Bit 07 Device Check (DVC) - Read/Write

Set to indicate either or both of the following drive errors occurred: DC power fault or head select fault. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register. DVC is a Class B error.

Bits 08,11 Not Used.
Always zeros.

Bit 12 Invalid Command (IVC) - Read/Write

Set when the volume valid (RMDS Bit 6) is reset or unit ready is not active and any command other than read-in preset or pack acknowledge is received. Also set if Drive Clear or NO-OP is received. Cleared by INIT, power-up cycle, or by writing 0's into this register. IVC is a Class B error.

Bit 13 Not Used
Always zeros.

Bit 14 Seek Incomplete (SKI) - Read/Write

Set by the controller upon a drive fault or a seek incomplete status from the drive. Cleared by either a drive clear or INIT then a recalibrate command.

Due to a positioner malfunction, it is possible for the Seek not to complete. The controller will do the following:

- o Set the SKI bit (RMER2, Bit 14)
- o Set the ATA bit (RMDS, Bit 15)
- o Reset the PIP bit (RMDS, Bit 13)
- o Set the RDY bit (RMCS1, Bit 7)
- o Set the UNS bit (RMER1, Bit 14)

This indicates to the software that the Seek operation did not complete and the exact positioner location is unknown.

Bit 15 Bad Sector Error (BSE) - Read Only

Set whenever the controller detects a 0 in Bit 14 or 15 of the first header word. A bad sector is indicated when these bits are cleared. This is a Class B error which causes termination of a read command after checking the CRC word. In the case of a read header and data command, this is a Class A error. Cleared by a Drive Clear or INIT.

6.2.19 ECC Position Register (RMEC1) (776744)

The controller has Error Correction Code (ECC) capabilities that detect and correct errors by reconstructing a portion of the data. In the specified code word length, the ECC code corrects an error that falls within an 11-bit burst. Any errors outside the specified burst length are detected but not corrected. The ECC hardware, in this case, yields an ECC uncorrectable error (Bit 6 of RMER1 sets). The controller contains the hardware to find the burst in which the read error is included and to determine the exact location of the burst within the data field.

The ECC pattern register (RMEC2) contains the actual error burst and the ECC position register (RMEC1) contains the address that determines the actual location of the error burst within the data field.

NOTE: The actual correction of the data field is done by the software with the help of the ECC position and ECC pattern registers.

Bits 00-12 ECC Position (POS) - Read Only

Set by the ECC logic if a data check error occurred (Bit 15 of RMER1 is set) during a data transfer command and the error detected is determined to be correctable (Bit 6 of RMER1 is reset).

The 13 position bits establish the binary address of the first bit of the error burst within the data field. The maximum valid address is 4128. If the ECC logic determines that the error is a non-correctable hard error (Bit 6 of RMER1 is set) or if the ECI bit (RMOF Bit 11) is set, the contents of this register are irrelevant.

Bits 13-15 Spare

6.2.20 ECC Pattern Register (RMEC2) (776746)

This Read Only register is used in conjunction with the ECC position register (RMEC1) and contains the actual error burst available at the completion of the ECC process. The software

uses the contents of the ECC position register to find the actual location of the error burst in the data field. Then the error burst itself determines the bits in error within the 11-bit field.

Bits 00-10 ECC Pattern (PAT) - Read Only

Set by the ECC logic if the detected error is correctable. The 11 pattern bits establish the error burst. Cleared by drive clear or INIT. If the ECC logic determines that the error is a non-correctable hard error (Bit 6 of RMER1 is set) or the error correction inhibit bit (RMOF Bit 11) is set, the contents of this register are irrelevant.

7.0 THEORY OF OPERATION

The theory of operation of the S34A and its interface to the disk drive is explained in detail in the following paragraphs.

7.1 Disk Interface

The controller has a industry standard SMD interface utilizing Motorola 3450 and 3453 differential transmitters and receivers. These circuits provide a terminated, balanced transmission system and allow disk operation at radial distances up to 50 feet and daisychain distances up to 100 feet from the controller.

The "A" cable is twisted pair, flat ribbon cable which allows mass termination to the "A" cable connector without stripping. The "B" cable is a flat ribbon cable with a ground plane and drain wire which allows mass termination without stripping.

7.1.1 "A" Cable

1) Characteristics

Type: 30 twisted pair, flat cable
Impedance: 100 ±10 ohms
Wire Size: 28 AWG, 7 strands
Propagation Time: 1.6 to 1.8 ns/ft.
Maximum Cable Length: 100-ft. cumulative
Voltage Rating: 300V rms

2) Components

Item	CDC P/N	AMP P/N	3M P/N
Connector (60 Position)	94384514	88012-2	3334-6060
Flat Cable (Twisted Pair) 30 pair 28 AWG	95047400	---	SS-455-248-60

3) Mating Receptacle on Controller

Item	3M P/N
60 Pin, Right Angle Header	3372-1002

4) Termination

Termination of the differential signals is provided by the terminator assembly installed on the last disk in the daisy-chain.

7.1.2 "B" Cable

1) Characteristics (with ground plane)

Type: 26 conductor flat cable with ground plane drain wire
Impedance: 130 ±15 ohms (3M P/N 3476/26)
Wire Size: 28 AWG - 7 strand
Propagation Time: 1.65 ns/ft. (nominal)
Maximum Cable Length: 50 ft.
Voltage Rating: 300V rms

2) Components

Item	CDC P/N	AMP P/N	3M P/N
Connector (26 position)	9438-507	86905-2	3399-3000
Flat Cable (26 position) w/ground plane & drain wire	95028509	---	3476/26

3) Mating Receptacle on Controller

Item	3M P/N
26 Pin, Right Angle Header	3493-1002

4) Termination

Termination of the differential signals is provided at the receiving end of the signal on either the controlle or the SMD's logic receiver end as appropriate.

7.1.3 Signal Descriptions "A Cable"

7.1.3.1 Address and Control Bus

Address and Control functions are transferred on a 10-lin bus labeled Bit 0 - Bit 9. See Figures 2.1 and 7.1.

7.1.3.2 Cylinder Address

The controller places the cylinder address on the bus lin and strobes the lines with Tag 1. The unit must be On Cylinder before Tag 1 is sent.

7.1.3.3 Head Select

The controller places head address on the bus lines and strobes the lines with Tag 2.

BUS	TAG 1 CYLINDER ADDRESS	TAG 2 HEAD SELECT	TAG 3 CONTROL SELECT
Bit 0	2^0	2^0	Write Gate
1	2^1	2^1	Read Gate
2	2^2	2^2	Servo Offset Plus
3	2^3	2^4	Servo Offset Minus
4	2^4		Fault Clear
5	2^5		AM Enable [1]
6	2^6		RTZ
7	2^7		Data Strobe Early [1]
8	2^8		Data Strobe Late [1]
9	2^9		

1 Not used by the S34/A Controller

TAG BUS DECODE
FIGURE 7.1

7.1.3.4 Control Select

Tag 3 is used as an enable for the bus lines and must be true for the entire control operation. The functions of Bus Bits 0 - 9 are as follows:

Bit 0 Write Gate - The Write Gate line enables the write driver.

Bit 1 Read Gate - Setting the Read Gate enables read data from the disk to the transmission line. The leading edge of Read Gate triggers the disk's phase-lock oscillator to synchronize on an all zeros pattern.

Bit 2 Servo Offset Plus - Offsets the carriage from the nominal On Cylinder position towards the spindle.

Bit 3 Servo Offset Minus - Offsets the carriage from the nominal On Cylinder position away from the spindle.

Bit 4 Fault Clear - Clears the fault flip-flop in the disk if the fault condition no longer exists.

Bit 5 AM Enable - Not Used. Always a zero.

Bit 6 RTZ - Causes the actuator to seek Track 0; resets the Head Register; clears the Seek Error flip-flop in the disk.

Bit 7 Data Strobe Early - Not Used. Always a zero.

Bit 8 Data Strobe Late - Not Used. Always a zero.

7.1.4 Individual Lines "A" Cable

1. Sector Mark

Derived from the servo track and occurs at the beginning of each sector.

2. Index Mark

Occurs once per revolution and its leading edge is considered the leading edge of Sector Zero.

3. Fault

Indicates one or more of the following fault conditions exist in the SMD. DC Power Fault, Head Select Fault, Write Fault, Write or Read while Off Cylinder, and Write Gate during a Read operation. A fault condition inhibits the writer to prevent

data destruction. The DC power fault indicates a below normal voltage from the positive or negative power supplies. The Head Select fault indicates that more than one head is selected. The Write Fault indicates low (or absence of) write current as well as the absence of write data.

4. Seek Error

Indicates a Seek Error has occurred (e.g., the disk was unable to complete a move within 500ms, the carriage has moved to a position outside the recording field or that a cylinder address greater than 822 has been selected).

5. On Cylinder

This status indicates the servo has positioned the heads over a cylinder. The status is cleared with any Seek instruction causing carriage movement or a zero-track Seek.

6. Unit Ready

This line indicates that the unit is selected; is up to speed; the heads are loaded; and no fault condition exists within the drive. If, after a load sequence, dibits are not sensed within 350ms, the heads will unload; the fault light will be illuminated; and Unit Ready will be dropped.

7. Open Cable Detector

The open cable detect circuit disables the interface in the event that the "A" interface cable is disconnected or controller power is lost.

8. Unit Select Tag

This signal gates the desired unit number into the disk's unit number compare circuit.

9. Unit Select (2^0-2^1)

These two lines are binary coded to select one of four SMD physical units. A unit number (0 thru 3) is selectable by means of a logic plug on the operator panel in each individual disk or by switches on the Fujitsu M2312.

10. Unit Select (2^2 - 2^3)

Always zero.

11. Address Mark Found

Not Used.

12. Write Protected

Enabling the Write Protect function inhibits the writer under all conditions, illuminates a front panel LED and sends a write protected signal to the controller. Attempting to write while protected will cause a fault to be issued.

13. Power Sequencing

Power Sequencing requires AC and DC Power On, START indicator on, and the REMOTE/START switch in the SMD in the REMOTE position. Applying ground to the Pick and Hold lines will cause the first SMD in sequence to power up. Once this SMD is up to speed, the Pick signal is transferred to the next active SMD and is repeated until all active SMD's are powered up.

Individual SMD's may be started and stopped once the power sequencing is complete.

7.1.5 Signal Descriptions, "B" Cable

7.1.5.1 Individual Lines ("B" Cable)

The following signals are provided between the controller and each disk. See Figure 2.2.

1. Write Data

   This line carries data which is to be recorded on the disk pack from the controller to the disk.

2. Servo Clock

   The servo clock is a phase-locked 9.677 MHz clock generated from the servo track dibits. Servo clock is available at all times (not gated with Unit Select).

3. Read Data

   This line transmits the recovered data as NRZ form data from disk to the controller.

4. Read Clock

   The Read Clock defines the beginning of a data cell and is synchronous with the detected data.

5. Write Clock

   This line is synchronized to the NRZ data and is the Servo Clock retransmitted to the SMD by the controller.

6. Seek End

   Seek End is the combination of On Cylinder or Seek Error indicating that a Seek operation has terminated.

7. Unit Selected

   If the Unit Select bit lines match the logic plug in the disk when the leading edge of Unit Select tag is received, the Unit Selected signal is transmitted to the controller.

7.2 Format

7.2.1 Pack Format

Each disk pack is divided into 5 individually addressable data surfaces for RM02 (19 for RM05) as shown in Figure 7.2. Each Read/Write surface (designated 0 through 4 or 18) is sectioned into 823 (0 through 822) concentric cylinders. These cylinders consist of fixed length sectors consecutively numbered 0 to 31 on each surface. Each sector is divided into 2 information fields separated by gaps or spaces. The header field contains 2 words of address information and 2 words of Header CRC. The data field contains 256 data words and 2 words of Data ECC. The controller generates the sector gaps and the computer supplies the header and data information during a pack formatting operation. (Except when on board format is used all sectors will contain the pack S/N and -1 data).

The Read Only servo surface is pre-recorded by the manufacturer with positioning signals used by the servo tracking circuits. Each RM02 disk pack has a maximum formatted capacity of 663, 667,200 bits. Each RM05 pack has a maximum formatted capacity of 2,521,935,360 bits. Table 7.1 shows how these bits are utilized.

The Fujitsu M2312 contains 7 tracks and 589 cylinders. These are mapped in sequential order to look to software like 5 tracks and 823 cylinders. Logical Block No. = $(5 \times CYL_{SMD}) + (TRK_{SMD}) = (7 \times CYL_{FUJ}) + (TRK_{FUJ})$. Interleave sector format may be selected for any physical unit no. by setting the appropriate configuration switch (SEC 5.6.1).

7.2.2 Sector Format

The 5 major divisions of a sector are shown in Figure 7.3. Table 7.2 contains the overall bit/byte assignments for each sector.

1. Sector Gap - Contains 28 bytes of 0's and 1 sync byte. The sync byte, which marks the beginning of valid information, is shown in Figure 7.4.
2. Header Field - The header field is divided into 3 words as follows:

   a. Cylinder Address Word - Contains the address of the respective cylinder. The 16-bit format is shown in Figure 7.4 and described in Table 7.3.

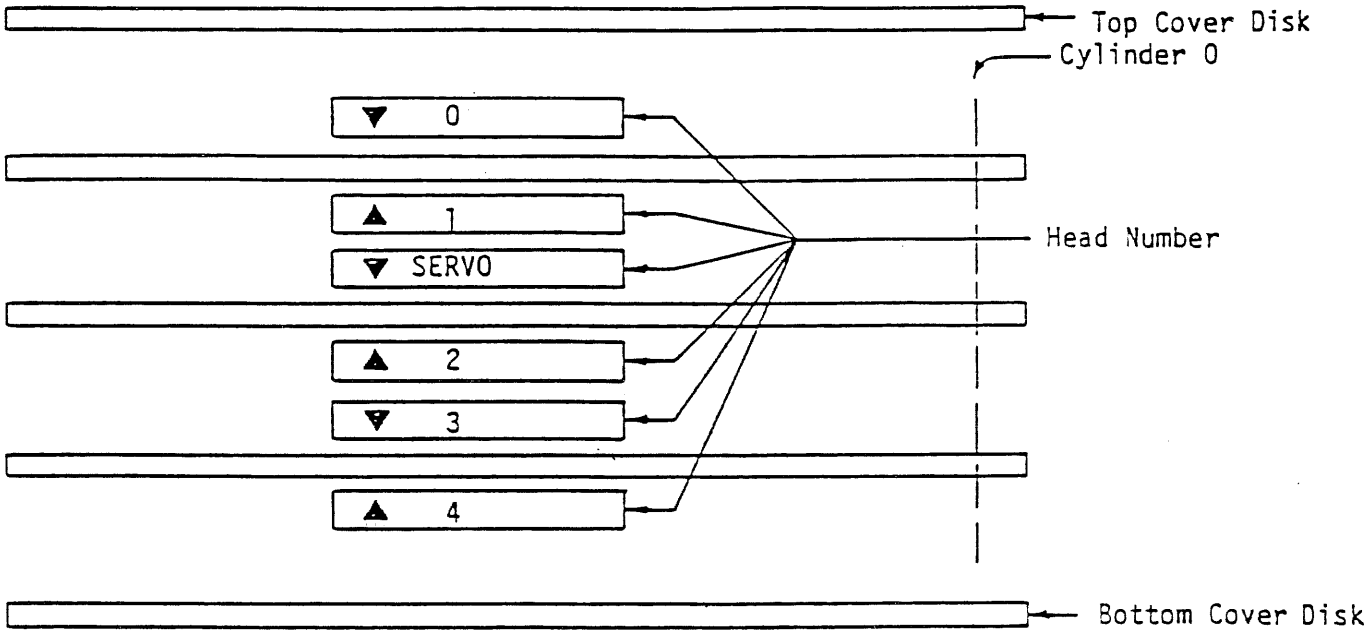
b. Sector/Track Address Word - Contains the address of the respective track and sector. The 16-bit format is shown in Figure 7.4 and described in Table 7.4.

c. CRC Word - This 16-bit word is generated by the cycle redundancy check (CRC) circuits using the data in the first two header words. This CRC provides a method for error detection in reading the Header data.

3. Header Gap - Contains 17 bytes of 0's and one sync byte. The sync byte, which marks the beginning of valid information is shown in Figure 7.4.

4. Data Field - The data field is composed of 512 data bytes provided by software and 4 error correction code bytes generated by the ECC circuits of the controller. The 32-bit ECC word is considered part of the data field and used to detect errors in reading the data.

5. Data Gap - This gap consists of two 0 bytes which are generated by the drive followed by an indefined gap area which fills the remaining sector space.



80 mBYTE DISK PACK WITH HEAD LOCATION

FIGURE 7.2

TABLE 7.1 Pack Capacity Allocation

ITEM	FORMAT (RM02/RM05)
No. of Sectors/Track	32
Bits/Sector	4,864
Total Formatted Capacity	663,667,200/2,521,935,360 bits
Formatted Data	539,361,280/2,049,572,864 bits
Total Number of Words	33,710,080/128,098,304

Table 7.2 Assignment of Bits/Bytes in Sectors

SECTOR LOCATION	BYTES	BITS
Sector Gap	29	232
Header Field	6	48
Header Gap	18	144
Data field	516	4128
Data Gap (fixed)	2	16
Undefined	59	472
Total per Sector	630	5040

NOTE: All byte descriptions in Table 7.2 are in terms of 8-bit bytes.

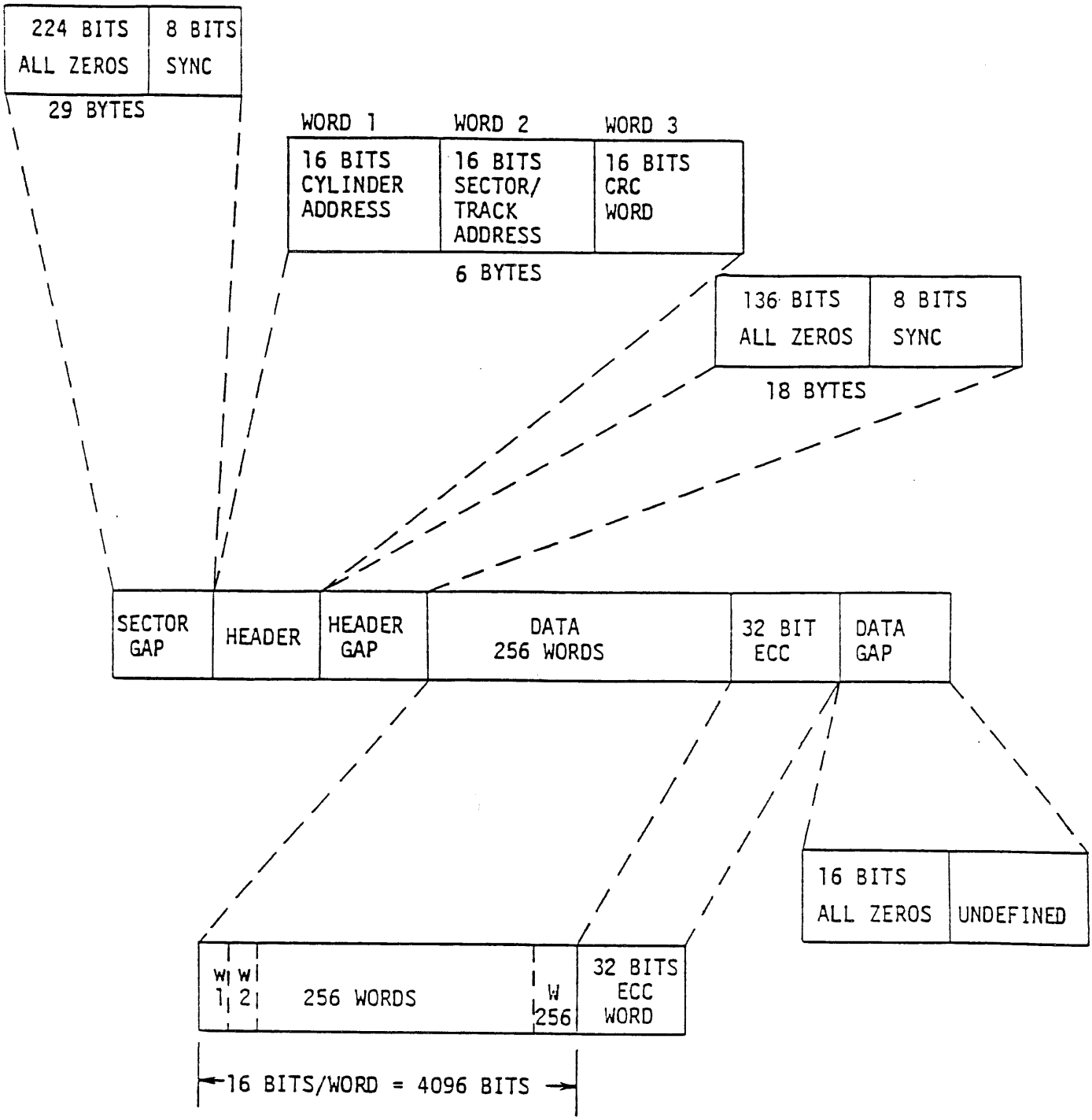


FIGURE 7.3

SECTOR FORMAT RM02/RM05

SYNC BYTE FORMAT

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	1

CYLINDER ADDRESS FORMAT (First Header Word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MF	UF	0	FMT 1	0	0	CYL 512	CYL 256	CYL 128	CYL 64	CYL 32	CYL 16	CYL 8	CYL 4	CYL 2	CYL 1

SECTOR/TRACK ADDRESS FORMAT (Second Header Word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	TA 16	TA 8	TA 4	TA 2	TA 1	0	0	0	SA 16	SA 8	SA 4	SA 2	SA 1

FIGURE 7.4

HEADER BITS AND SYNC BYTE FORMAT

TABLE 7.3 Cylinder Address Word-Bit Assignments

BIT	NAME	DESCRIPTION
0-9	CYL	Ten bit locations for the address of the cylinder. Any decimal number from 0 to 822 is valid. Bit 0 is least-significant bit.
10,11	Unused	Always 0s
12	FMT	The format bit is set to a 1 which establishes the sector is formatted using 16-bit words.
13	Unused	Always 0s
14	UF	The location where the user can identify this sector as being bad so that data is not recorded here. A 0 indicates a bad sector; 1 a good sector.
15	MF	The location used by the disk pack manufacturer to indicate a bad sector. A 0 indicates a bad sector; 1 a good sector.

TABLE 7.4 Sector/Track Address Word-Bit Assignments

BIT	NAME	DESCRIPTION
0-4	SA	These five bits contain the address of the sector. Valid decimal numbers are 0-31
5-7	Unused	Always 0s
8-10	TA	These five bits contain the track address. Valid numbers are 0-4 for RM02; 0-18 for RM05.
13-15	Unused	Always 0s

7.3 HARDWARE DESCRIPTION

The S34/A controller is implemented using an advanced architecture whose unique structure and resulting capability provides exceptional features and performance. The heart of the system is a fast bi-polar microprocessor based on the 2901 family of components. An additional independent microprogrammed sequencer performs detail decision making control for UNIBUS Disk Data movement operations. See sheet 1 of schematic 03351, Section 8 for block diagram.

7.3.1 Microprocessor

Internal data path communication is via a tri-state, 16-bit bus (D Bus). Major elements in the data path include: (Block Diagram, Figure 7.5)

1. Disk Command Register

   This register is loaded by firmware with Bits 01, 03, 05 of the command word and directs the Disk Data Sequencer to execute one of the six following operations:

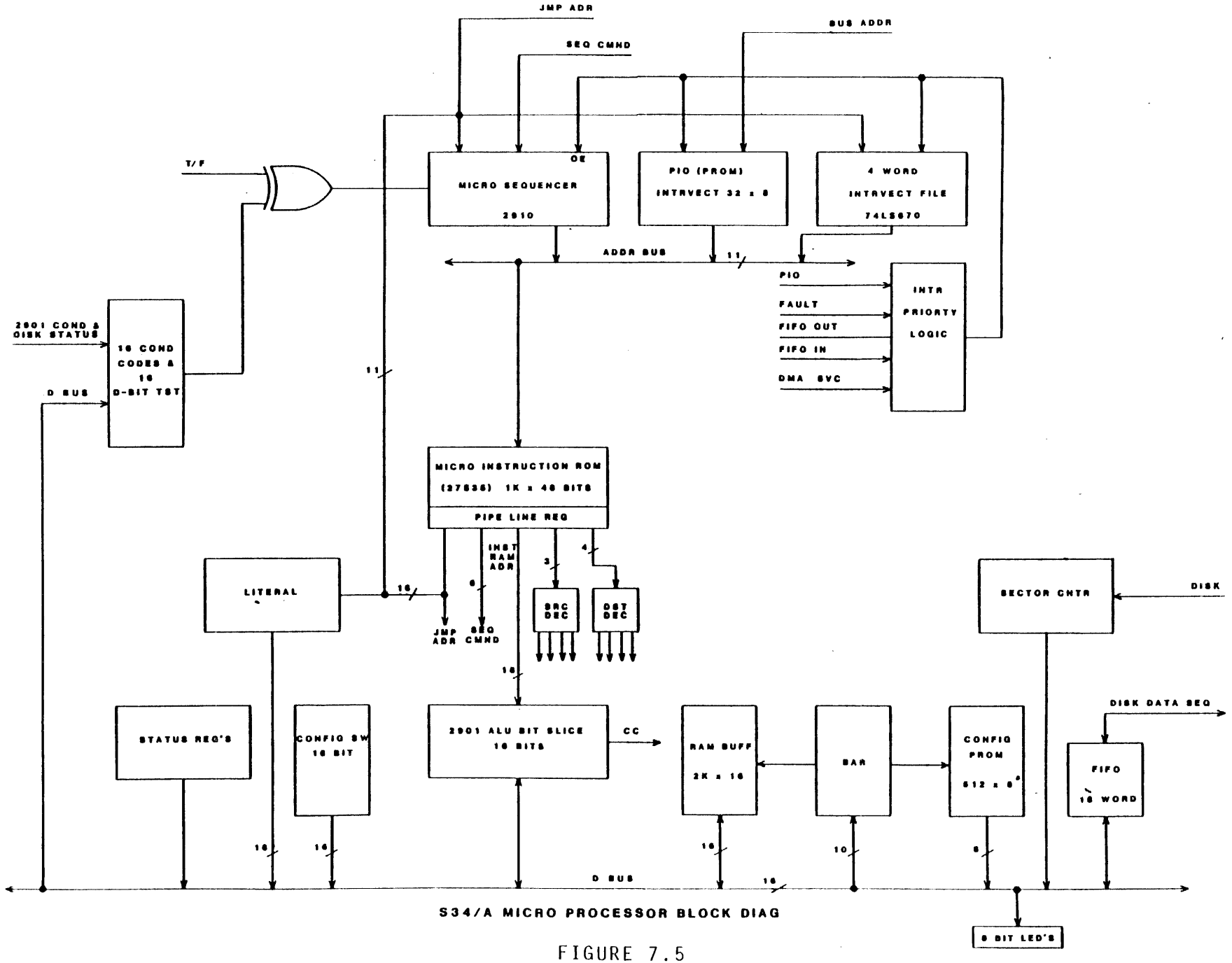
   - o Self-Test
   - o Read Header and Data
   - o Read Data
   - o Write Header and Data
   - o Write Data
   - o Idle

2. A Register

   Contains the Disk Address and Control Bus bits to direct disk operations. The data loaded into this register corresponds to the disk address and control bus defined in Section 7.1.3.

3. FIFO

   Performs serial-to-parallel and parallel-to serial data operations. Acts as the synchronization element between the disk and the controller for all data movements by buffering up to 16 words of data.



S34/A MICRO PROCESSOR BLOCK DIAG

FIGURE 7.5

4. Pattern Register

   Contains the actual data error correction mask after a successful data error correction operation.

5. Position Register

   Contains the location of the first bit of the error burst after a successful data error correction operation.

6. Sector Counter

   Provides rotational position (sector number) for the selected disk drive.

7. Buffer Address Register (BAR)

   Contains the address currently being used to read (Buffer Read Pointer) or Write (Buffer Write Pointer) data in the buffer.

8. Buffer (2K x 16)

   Provides storage of up to 7 sectors of data being transferred to or from the UNIBUS to eliminate data late errors and allow cross-track (spiral) read or write operation. The remaining 256 words are used for temporary and register storage.

9. Microprocessor (2901)

   Provides the arithmetic/logical manipulation capability of the controller under firmware control. It also provides 16 words of storage for various pointers and temporary working registers. All standard 2901 functions are implemented including a shift instructions.

10. Address/Data Registers

    Provides temporary storage for address or data movements between the controller and the UNIBUS.

Major elements in the control structure include:

1. Vector Address Register and Interrupt Logic

   Provides the primary task scheduling mechanism for the firmware by prioritizing the five interrupt events demanding attention by the controller. Provides the firmware address for interrupt sequencing of a task and the orderly return from interrupt.

2. Micro Interrupt Logic

   Provides a unique vector address for the firmware as a function of the PIO register addressed by software and the operations required for handling, DMA events, fault conditions, FIFO register In & Out service.

3. 2910 Sequencer

   Provides the next micro-program address to be executed and resolves all conditional executions.

4. Test Logic

   Selects 1 of 16 firmware testable status flags or testable bits used to direct firmware execution, and the ability to test any one of the 16 internal BUS bits.

5. Control ROM

   1024 words of 48 bit micro-program memory.

7.3.2 Disk Data Sequencer

A block diagram of the disk data sequencer and serial data path is shown in Figure 7.7. Data written to and read from the disk and the verification of data integrity is controlled by this logic. Major elements include:

1. Data Input Shift Register

   Synchronizes disk data with Read Clock and provides 8 bits of storage for Sync Byte comparison.

2. FIFO

   See Section 7.3.1.

3. Position Register/Pattern Register

   See Section 7.3.1.

4. ECC Logic

Generates and checks ECC over the 512 data bytes and provides the proper values for the POS and PAT registers on an error.

5. CRC

Generates and checks 16-bit CRC over the sector header.

6. Comparator

Performs bit by bit comparison of the header read from disk with expected value read from the FIFO.

7. Error Flags

Consists of the error flags associated with header and data.

- o DCK - Disk Data Error
- o ECH - Hard Data Error
- o FMT - Improper Format
- o CRC - Header CRC Error
- o HCE - Header Compare Error
- o BSE - Bad Sector Error

8. Disk Command Register

See Section 7.3.1.

9. Sequencer

Micro-program storage which provides decision making and direct control for disk data movements.

10. Test Mux

Selects 1 of 16 testable status flags to direct sequencer execution.

11. State Counter

A 16 bit counter, testable by the sequencer, used to count the data bits read from or written to disk.

7.3.3 UNIBUS Control Sequencer

In addition to the normally used transceivers and registers, there is an FPLA sequencer, which handles the required control of DMA, Interrupt, and PIO service.

Control of DMA, Interrupt, and PIO operations are handled by an FPLA Sequencer, with associated hardware counters for setting BUS address, burst sizes and selectable DMA delay time. The FPLA takes care of the UNIBUS timing and protocol when requested to do so by the microprocessor, then interrupts the microprocessor to take data or supply data when required. When jumper enabled, this BUS control circuitry monitors the UNIBUS to determine that another device is waiting to become BUS master, for an interrupt or DMA sequence. When detected, the DMA burst is throttled down to allow other devices access to the UNIBUS.

7.3.4 Configuration PROM

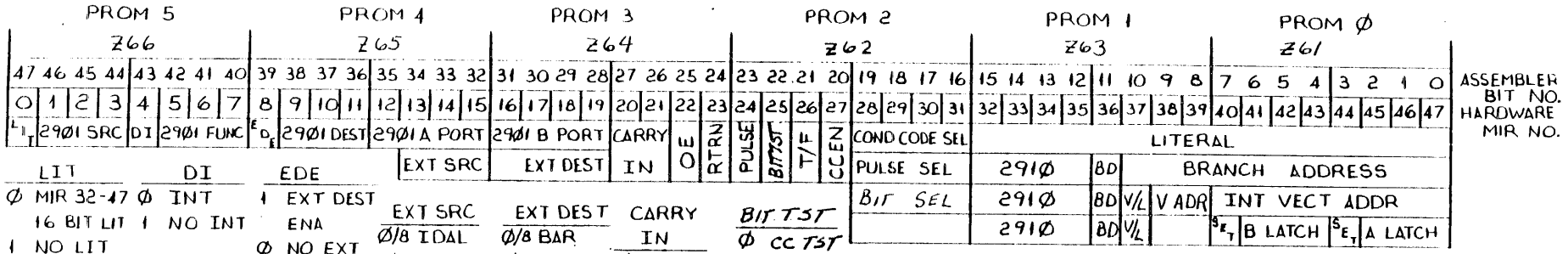
A 512 x 8 PROM contains necessary mapping constants to allow any combination of compatible drive types to be connected to the four ports of the controller. This PROM is used in conjunction with 16 switches (4 for each port) to describe the type of drive and emulation associated with each physical unit number.

7.4 Firmware Description

The firmware in the controller is contained in two independent micro-programmed sequencers to perform the required decision making and control functions. Each sequencer contains its own firmware set implemented in a language appropriate to the task.

7.4.1 Microprocessor

Primary control of the operations of the controller is provided by the firmware for the 2901/2910 microprocessor. This structure also provides supervisory control of the other sequencer,



LIT	DI	EDE
Ø MIR 32-47	Ø INT	1 EXT DEST ENA
16 BIT LIT	1 NO INT	Ø NO EXT DEST
1 NO LIT		

2901 SRC	R	S
Ø	A	Q
1	A	B
2	Ø	Q
3	Ø	B
4	Ø	A
5	D	A
6	D	Q
7	D	Ø

2901 FUNC	
Ø	R+S
1	S-R
2	R-S
3	RVS
4	R∧S
5	$\overline{R}$∧S
6	R∨S
7	$\overline{R \vee S}$

2901 DEST	RAM	Q	
Ø	—	F→Q	F
1	—	—	F
2	F→B	—	A
3	F→B	—	F
4	F/2→B	Q/2→Q	F
5	F/2→B	—	F
6	2F→B	2Q→Q	F
7	2F→B	—	F

EXT SRC	EXT DEST
Ø/8 IDAL	Ø/8 BAR
1/9 RAMO	1/9 RAMI
2/A ECCPAT	2 ODAL
3/B ECCPOS	3/B MARX ②
4/C SCNTR ①	4/C WFIFO
5/D DSTAT	5/D AREG
6/E RFIFO	6/E DCMD
7/F TST WORD	7/F LEDS/UNIT ③ A MAR

CARRY IN	
Ø	Ø
1	Ø
2	COUT
3	1

(LIT=1)

OE	
Ø	2901→ DBUS
1	2901← DBUS

(LIT=Ø)

RTRN	
Ø	2910 RTRN
1	2910 CONT

BIT TST	
Ø	CC TST
1	DBUS BIT TEST

T/F	
1	CC FALSE
Ø	TRUE

CCEN	
Ø	2910 COND
1	TST ENA 2910 UNCOND MODE

COND CODE SELECT	
Ø	ALUZ
1	ALUCO
2	ALUNEG
3	POWER-UP
4	RDY
5	NXM
6	DMABUSY
7	OR_FULL
8	IR_EMPTY
9	SEQBUSY
A	UPE
B	TEST A
C	TEST B
D	TEST C
E	TEST D
F	TEST E

PULSE SEL	
Ø	CLRIMK
1	CLRSMK
2	
3	BUSSEQ
4	CLRFIFO
5	BYTE
6	CCLR
7	CLRDCK

2910	
Ø	RESET
1	CALL
2	
3	GOTO
4	PUSHCNTR
5	CALLR
6	
7	GOTOR
8	RFCT
9	RPCT
A	RETURN
B	POPGOTO
C	LD2910 LDCNTR
D	LOOP
E	CONT
F	TWB

B LATCH	A LATCH
Ø	Ø
1 USTAG	1
2 IC1	2
3 TAG1	3 IRENB
4 TAG2	4 ORENB
5 TAG3	5 POWER-UP
6 ECI	6 IRQ(BR)
7 HCI	7 DMAR (NPR)

BRANCH DISABLE
BD 1 = V/L FUNC
Ø = BRANCH ADR

V/L FUNCTION (LIT=1)
1 = LD VECT ADR
Ø = LATCH ENAB

V ADR	
FAULT_VECT	Ø
IR_VECT	1
OR_VECT	2
UMA_VECT	3

① EXT SRC
4/C Ø-7 CONFIG PROM
8-15 SECTOR COUNT

② EXT DST
3/B 8,9 EXT ADR (16-17)
Ø BAIN

③ EXT DST
7/F Ø-1 DRIVE UNIT#
8-15 LED DISPLAY

S34 MICRO INSTRUCTION FORMAT

FIGURE 7.6

defining and initiating its functions and utiiizing the results to complete its own activities.

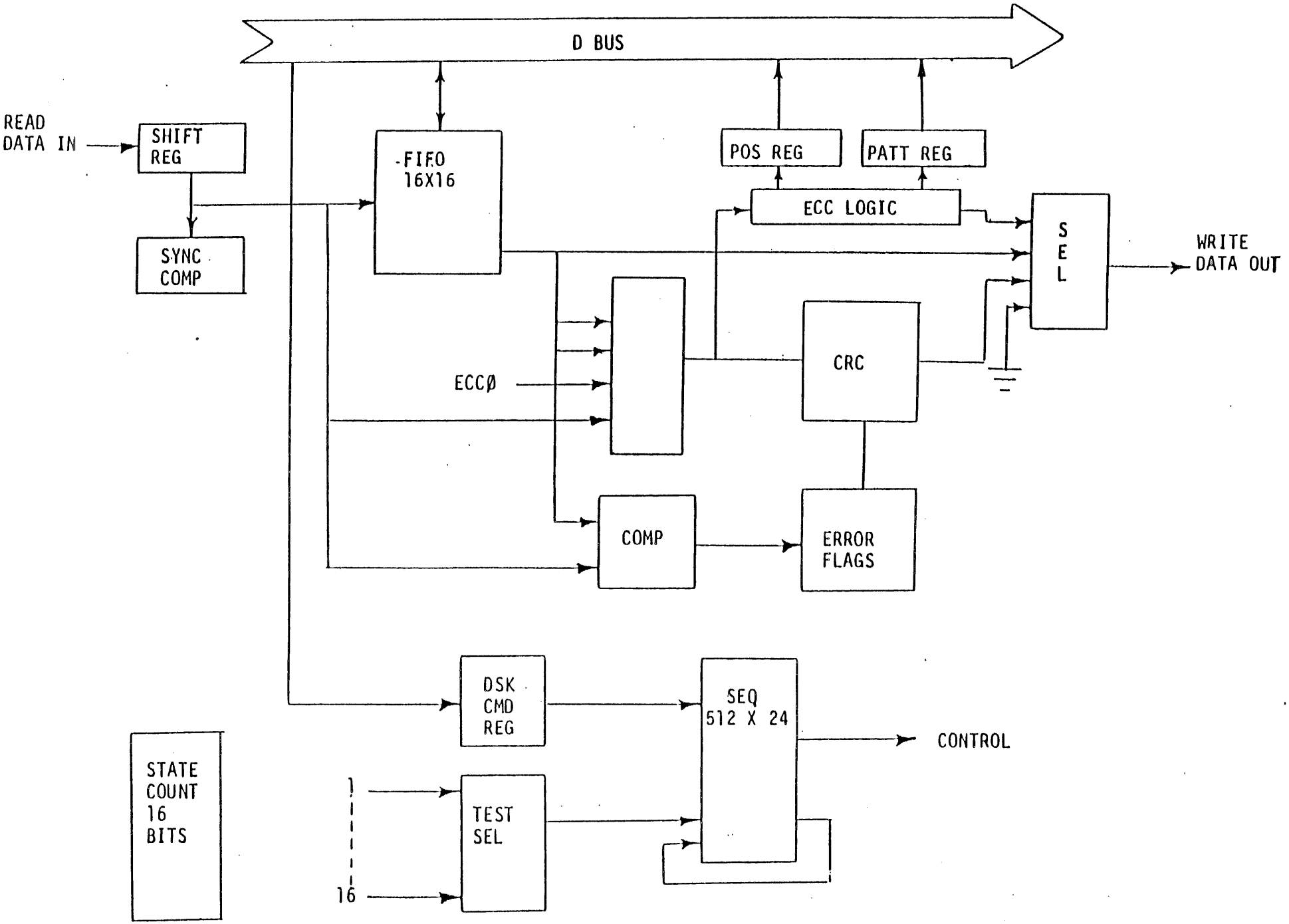
The firmware is contained in a set of ROM's organized as 1K words by 48 bits which is addressed by the 2910 sequencer chip.

Figure 7.6 defines the micro-instruction format, the usage of the different fields, their respective bit assignments, field values, and labels used by the language translator.

7.4.2 Disk Data Sequencer

The disk data sequencer is a set of ROM's orgainzed as a "ROM-Register Sequencer", consisting of 512 words by 24 bits. Primary control of the sequencer's operation is provided by the Disk Command Register which is loaded from the micro-processor "D BUS". This register provides three bits of address for the ROM which may be viewed as defining a "page" of locations or an "OP-Code". Execution is by means of conditional two-way jumps or branches to adjacent location (address) "pairs". The address of the "pairs" is provided from the ROM's output with the decision between the two addresses made based on the test result.

Figures 7.8 and 7.9 define the instruction format, the usage of the different fields, their respective bit assignments, addresses, field values, and labels used by the language translator.



DISK DATA SEQUENCER BLOCK DIAGRAM

FIGURE 7.7

DISK SEQUENCER - MICRO INSTRUCTION FORMAT

ROM Address:

8	7	6	5	4	3	2	1	0
CMD			STATE					T

Micro Instruction Format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
STATE					TEST			MUX		ORDER				BIT ORDERS									
ST					T			M		O				Z	#	ECC		G	H	OFI		W	R

Field Definitions:

Command Field (CMD):

CMD	Name	Field Value	Origin HEX
Disk Idle	DI	0	000
Spare	-	1	040
Disk Test	DT	2	080
Spare	-	3	0C0
Write Data	WD	4	100
Write Header and Data	WH	5	140
Read Data	RD	6	180
Read Header and Data	RH	7	1C0

State Field (State):

Address Label	Field Value	Absolute Address
DIXX	00-1F	000-03F
-	00-1F	040-07F
DTXX	00-1F	080-0BF
-	00-1F	0C0-0FF
WDXX	00-1F	100-13F
WHXX	00-1F	140-17F
RDXX	00-1F	180-1BF
RHXX	00-1F	1C0-1FF

Test Results (T):

Condition	Field Value
Selected test state low	0
Selected test state high	1

FIGURE 7.8

TEST FIELD (Test):

Function	Name	Field Value
Unconditional Jump	True	0
Header Error Summary	Error	1
Index or Sector Mark	IOSMK	2
Sync Byte (Neg True)	-Sync	3
Data Check (ECC Error)	DCK	4
Error Check Inhibit	ECI	5
End of ECC Correction Cycle	END	6
State Counter = 4	C4	7
State Counter = 8	C8	8
State Counter = 16	C16	9
State Counter = 32	C32	A
State Counter = 64	C64	B
State Counter = 128	C128	C
State Counter = 256	C256	D
State Counter = 4096	C4096	E
State Counter = 65536	Carry	F

DATA SELECT FIELD (MUX):

Read Select Function	RMUX Name	Field Value	WMUX Name	Write Select Function
Zeros Fill	Zero	0	Zero	Zeros Fill
Data Input	DIN	1	CRCOUT	CRC Gen Output
ECC CKTS - Bit 0	ECC0	2	ECC0	ECC CKTS Bit 0
FIFO Output	FIFO	3	FIFO	FIFO Output

ORDER FIELD (Order):

Function	Name	Field Value
No Operation	NOP	000
Data Check Error Enable	DCKEN	001
CRC Error Enable	CRCEN	010
Bad Sector Error Enable	BSEN	011
Format Error Enable	FMTEN	100
Set Done Flag	DONE	101
Spare	--	110
Spare	--	111

BIT ORDER FIELD (Bit Order):

Function	Signal Name	Bit Position	Comments
Clear Cmd Register	CLR CMD	14	Default = 1
State Counter Enable	CNTEN	15	
ECC Correction Cycle Enable	ECCTN	16	
Clear ECC - CRC Circuits	ECC-CRC	17	Default = 1
Enable ECR	GENCRC	18	
Header Compare Enable	HCEN	19	
FIFO Output Enable	FIFOOUT	20	
FIFO Input Enable	FIFOIN	21	
Disk Write Gate	WRT - Gate	22	
Disk Read Gate	RD - Gate	23	

FIGURE 7.9

7.5 DMA Throttle and Performance Optimization

The S34/A has the ability to transfer complete tracks or even complete cylinders without burning any extra disk revolutions. The S34/A achieves this by using a new DMA hardware design which allows switch selectable DMA burst sizes of 1 word to 128 words, adaptive NPR (or throttle), and switch selectable NPR off times of 0 to 384 usec. Also the S34/A has a seven sector RAM buffer which helps when there is heavy BUS activity by other devices.

Throttle control on the S34/A gives it the ability to modify its burst size when other DMA or PIO devices request the use of the bus by an 'NPR' or 'BR', even if the requesting device is further from the processor, or lower priority than the S34/A.

If throttle is enabled, the controller will attempt to do DMA transfers of the maximum size as determined by the burst size switches. If, however, any other device requests use of the BUS during the time that the S34/A is transferring data, the burst will stop after completion of one more word, and BUS mastership is relinquished. A new non-processor request (NPR) will be started after a delay of 0 to 384 usec as determined by the NPR off time switches.

The NPR off time gives the user the ability to restrict the time the S34/A can control the BUS, and thereby restrict processor cycles. The need to increase this delay time would be for specific applications. Usually 0 or 3 usec is sufficient for most applications.

For fixed burst sizes (no throttle), the S34/A will transfer the full number of words as determined by the burst size switches.

Larger burst sizes make the most efficient use of the BUS by reducing arbitration delays and time used in taking and relinquishing the BUS. By use of the throttle mechanism, the controller will transfer data at maximum data rates when the BUS is idle and still allow other devices almost immediate use of the BUS when required.

Multiple DMA devices, such as two disk controllers, would tend to see a degrading of performance if they were both throttle controlled and were both doing very large transfers simultaneously In that case it would probably be advisable to set the one with the highest use to large bursts and throttle enabled; and then the other to fixed four word burst with throttle disabled.

As a guide to setting burst sizes and off time, the performance charts (Figure 7.10) show the effects of different combinations of the two variables. This data was taken on a PDP-11/34A processor with semiconductor memory and the S34/A controller connected to a CDC 9766 300 MByte disk emulating an RM05. A maximum data transfer of 64K words was read from or written to the disk. This is the maximum word count that may be set in an RH11/RM02/5 subsystem. On an RM02, a seek would be required after 5 tracks (one complete cylinder) and therefore require an extra revolution to SYNC up with sector zero of the next cylinder. That would be after 160 sectors. The maximum number of contiguous sectors on an RM05 is 256 sectors or 8 tracks, due to the limit of 64K word count. Then a new command must be specified. The processor was performing a continuous branch instruction and no other devices were active.

Recommended settings would be 16 word burst size with 3 usec off time and throttle enabled. This should be changed for special customer applications using the chart as a guide. See Section 5.6 for specific settings of switches and jumpers.

Performance Data
Contiguous Sectors Transferred

PDP-11/34A 9766 300 MByte - Emulation = RM05
Read or Write 64K words (max word cnt)
No other devices active on bus

WRITE TO DISK	usec OFF time (NPR delay)								
BURST SIZE WORDS/NPR	0	3	6	12	24	48	96	192	384
1	16	10	8	5	3	2	1	1	1
2	33	15	10	9	6	3	2	1	1
4	256	28	15	11	9	6	3	2	1
8	256	121	30	16	11	9	5	3	2
16	256	256	123	32	17	11	9	6	3
32	256	256	256	256	36	17	11	9	6
64	256	256	256	256	256	36	17	11	9
128	256	256	256	256	256	256	34	18	12
			Full cyl or max WD cnt			≧Full trk		<Full trk	

64K Word cnt is equal to 256 sectors or 8 tracks

WRITE

READ DISK	usec OFF time (NPR delay)								
BURST SIZE WORDS/NPR	0	3	6	12	24	48	96	192	384
1	22	7	7	7	7	7	7	7	7
2	42	16	11	9	8	7	7	7	7
4	256	29	16	11	9	8	7	7	7
8	256	85	28	16	11	9	8	7	7
16	256	256	63	28	16	11	9	7	7
32	256	256	256	70	28	16	11	8	7
64	256	256	256	256	70	29	16	11	8
128	256	256	256	256	256	74	28	15	10
			Full cyl or max WD cnt			≧ Full trk		< Full Trk	

READ

FIGURE 7.10

8.0 PART NUMBERS/DOCUMENTATION

8.1 Ordering Information

The following part numbers have been assigned to the Model S34/A and accessories:

Part Number	Description
65097	Model S34/A SMD Controller
65013	SMD "A" Cable, 10 ft. (Control Cable)
65015	SMD "A" Cable, 25 ft. (Control Cable)
65014	SMD "B" Cable, 10 ft. (Data Cable)
65016	SMD "B" Cable, 25 ft. (Data Cable)
65028	SMD "A" Round Cable, 10 ft.
65029	SMD "B" Round Cable, 10 ft.
65030	SMD "A" Round Cable, 25 ft.
65031	SMD "B" Round Cable, 25 ft.
65032	SMD Ground Cable, 10 ft.
65033	SMD Ground Cable, 25 ft.

8.2 Documentation

Part Number	Description
03351	Schematic Diagram, S34 CMD/SMD Controller
65087	Assembly Drawing S34 CMD/SMD Controller
65087	Bill of Materials, S34 CMD /SMD Controller
65097	Bill of Materials, S34/A SMD Controller

L

65087 SHEET 1 OF 6

REVISIONS

SYM.	SHEET	DESCRIPTION		APPROV.	DATE
X0		Pre-Production Release	C.L.	JCP	8/26/82
A		RELEASE TO PRODUCTION LM + ECN 3060		JCP	1/3/83
B		ECN # 3071	C.L.	JCP	2/2/83
C		ECN 3137	BL	JCP	4/12/83
D		ECN 3169	BL	JCP	4/12/83
E		ECN 3172	BL	JCP	4/12/83
F		ECN 3182	BL	JCP	4/12/83
G		ECN 3187		JCP	4/12/83
H		ECN 3240	JEJ	Carol L.	12.5.83
J		ECN 3256	JEJ	Carol L.	12.5.83
K		ECN 3339	JEJ	Carol L.	12.5.83
L		ECN W3506	L	Carol L.	2.5.84

DRAWN	DLL
DATE	8/17/82
CHECKED	LEEDS
DATE	8/19/82
ENGR.	JCP
DATE	9/10/82
APPROVED	EW
DATE	1/04/83

TITLE

MASTER
S34 SMD DISC CONTROLLER

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65087
SHEET 1 OF 6

REV. L

TITLE: S34 SMD CONTROLLER, MASTER ASSEMBLY

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	8	18401	LED RED PCMT W/INTL RES	LED00-07
2	1	18101	DIODE SILICON HIGH COND. 1N914	CR1
3	3	10105	RES CC ¼W 100Ω 5%	R16, 49, 2
4	8	10155	RES CC ¼W 180Ω 5%	R3,4,5,7,1,11,17,18
5	4	10164	RES CC ¼W 330Ω 5%	R12,13,14,9
6	2	10110	RES CC ¼W 390Ω 5%	R6,8
7	12	10177	RES CC ¼W 680Ω 5%	R10,19,21,23,24,28,36,38,42-45
8	8	10113	REW CC ¼W 1K Ω 5%	R15,25,26,27,35,37,40,46
9	1	10121	RES CC ¼W 4.7KΩ 5%	R20
10	8	10145	RES CC ¼W 22KΩ 5%	R29-34,39,41
11	1	10616	RES CC ¼W 150KΩ 5%	R22
12	2	10356	RES WW NI 5W 7.5Ω ±1%	R47,48
13	6	11986	RES MDL 56Ω 2%	RM7-9,12-14
14	5	11987	RES MDL 82Ω 2%	RM6,15-18
15	5	11988	RES MDL 1.0KΩ 2%	RM1-5
16	2	11989	RES MDL 22KΩ 2%	RM10,11
17	53	12105	CAP TANT 4.7µf 10V	C1,3,5-8,11,13-15,17-30,33-49,52-63
18	1	12517	CAP SIL MICA 220 PF ±5%	C31
19	4	12332	CAP CER. .001µf ±10%	C4,9,12,16
20	1	12119	CAP TANT 1µf 15V	C51
21	1	12329	CAP CER .1 µf ±20% (CK06)	C50
22	9	16380	IC INTFC XCVR 2908	Z4-Z8, Z13-Z16
23	2	16268	IC 8B COMPTR 25LS2521	Z3,Z177
24	1	16531	IC OCT 3STAT BFR INV 74S240	Z12
25	7	16202	IC 74LS74 DUAL D BIN FF	Z10,27,57,81,94,123,139
26	1	16214	IC 74LS123 DUAL MONOSTABLE MV	Z80

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65087
B/M
SHEET 2 OF 6

REV. L

TITLE: S34 SMD CONTROLLER, MASTER ASSEMBLY

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
27	1	16212	IC 74LS11 TPL 3I/P AND	Z37
28	2	16374	IC 8640 QUAD NOR BUS RX	Z36,39
29	2	16309	IC 7438 QUAD 2I/P NAND	Z11,35
30	1	16345	IC 8641 QUAD UNIBUS XCVR	Z2
31	3	16220	IC 74LS32 QUAD 2I/P OR	Z38,55,156
32	8	16513	IC 74S00 QUAD 2I/P NAND	Z56,40,71,173,142,128,86,122
33	1	16210	IC 74LS04 HEX INV	Z60
34	4	16505	IC 74S86 QUAD EXCL OR	Z110,79,158,120
35	1	16224	IC 74LS30 8I/P NAND	Z9
36	3	16236	IC 74LS393 DUAL 4B BIN CNTR	Z121,29,141
37	11	16245	IC 74LS161 SYN 4B CNTR BIN	Z30-34, 90-93,111,1
38	1	16957	IC FPLA 3STAT UNPROG 82S153	Z28
39	3	16525	IC 74S08 QUAD 2I/P AND	Z58,174,118
40	3	16521	IC 74S32 QUAD 2I/P OR	Z59,135,140
41	5	16253	IC 74LS244 OCT 3STAT BFR	Z85,103,104,46,26
42	4	16701	IC 2901 MICROPROCESSOR	Z67-70
43	1	16508	IC 74S158 QUAD 2 TO 1 MUX	Z133
44	1	16702	IC 2902 LOOKAHEADCARRY GEN	Z102
45	3	16221	IC 74LS174 HEX D FF	Z47,48,97
46	2	16264	IC 74LS259 8B ADD LATCH	Z100,136
47	4	16520	IC 74S138 3 TO 8 DCDR/DEMUX	Z83,112,99,124
48	2	16515	IC 74S10 TPL 3I/P NAND	Z150,134
49	4	16501	IC 74S04 HEX INV	Z87,114,132,138
50	12	16260	IC 74LS374 OCT D FF	Z119,109,41,42,95,106-108,74-77
51	5	16563	IC 74S251 3STAT DATA SEL/MUX	Z43-45,145,175
52	1	16364	IC 74148 8 TO 3 OCT PRI ENCDR	Z96

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65087
B/M
SHEET 3 OF 6

REV. L

TITLE: S34 SMD CONTROLLER, MASTER ASSEMBLY

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
53	1	16554	IC 74S153 4 TO 1 DATA SEL/MUX	Z161
54	1	16275	IC 74LS20 DUAL 4I/P NAND	Z127
55	1	16225	IC 74LS157 QUAD 2 TO 1 MUX	Z131
56	1	16717	IC PROM 3 STAT UNPRGMD 74S288	Z84
57	1	16918	IC AM2910DC MICROPROCESSOR	Z101
58	2	16267	IC 74LS670 4 x 4 REG.	Z129,130
59	1	16263	IC74LS273 OCT D FF	Z82
60	8	16916	IC 9148-70 STATIC RAM	Z18-25
61	1	16911	PROM UNPRGMD 512x8 TBP18S42 (AM27S29DC/HM3-7649-5)	Z17
62	1	16206	IC 74LS08 QUAD AND	Z54
63	2	16522	IC 74S74 DUAL D BIN FF	Z159,117
64	1	16385	IC 74265 QUAD COMPLEMENT O/P	Z157
65	6	16947	IC 27S35 PROM UNPROG 1Kx8 REG.	Z61-66
66	2	16511	IC 74S260 DUAL 5I/P NOR	Z88,116
67	1	16542	IC 74S30 8I/P NAND	Z115
68	3	16246	IC 74LS164 8B SHIFT REG	Z72,73,89
69	2	16377	IC 74276 QUAD J-K FF	Z151,172
70	2	16524	IC 74S174 HEX D FF	Z113,160
71	1	16261	IC 74LS299 8B BIDIREC 3STAT REG	Z176
72	1	16538	IC 74S253 DUAL 4 TO1 SEL/MUX	Z143
73	3	16946	IC 27S25 PROM UNPROG 512x8 REG	Z147-149
74	1	16381	IC 9401 CRC GEN/CHKR	Z146
75	1	16269	IC 25LS2538 DIGITAL DCDR	Z171
76	4	16915	IC 9403 BIPOLAR FIFO BFR MEMORY	Z49-52
77	7	16378	IC 3450 RCVR DIFFERENTIAL	Z152,153,155,162,164,167,168
78	6	16379	IC 3453 DRVR DIFFERENTIAL	Z154,163,165,166,169,170

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65087 B/M
SHEET 4 OF 6

REV L

TITLE: S34 SMD CONTROLLER, MASTER ASSEMBLY

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
79	1	16235	IC 74LS375 4B BISTABLE LATCH	Z137
80	1	16604	IC 75452 DUAL PERIPHERAL DRVR	Z105
81	1	20314	LM320T 5V VOLT REG.	Q1
82	1	14112	IC K1100A 11.111 MHZ XTLO	Y1
83	6	22917	8POS DIP SWITCH	SW1,2,3,4,5,6
84	1	22306	CONNECTOR 60 PIN	H
85	4	22313	CONNECTOR 26 PIN	J,K,L,M
86				
87	9	22353	SOCKET CARRIER DUAL 24 POS	
88	2	22357	SOCKET CARRIER DUAL 20 PIN	
89	1	22390	SOCKET CARRIER DUAL 16 POS	(AUGAT #716-AG2D)
90	1	26322	SCR, PNH PH, STL, 4-40x¼	
91	1	26206	WASHER INT. TOOTH STL #4	
92	1	26102	NUT, HEX, STL, 4-40	
93	2	42650	HANDLE-INSERTOR, EXTRACTOR DR-111	
94	2	26311	SCR, PNH, PHL, STL, 2-56x 7/16	
95	2	26107	NUT, HEX, SELF-LOCK, STL, 2-56	
96	2	42651	SPACER, HANDLE MOUNT, DR-111	
97	2	26212	WASHER-BELVILLE SPRING	
98	4	22214	BEAD PIN	
99	1	40840	P.C. BOARD S34	
100	52	22601	CONTACT, MALE	E1(15), E2(2), E3(12), E4(3), E5(6), E6(4), E7(3), E8(3), TP1-TP4
101	1	12609	CAP SIL MICA 240 pf ±5%	C2
102	A/R	30602	INK MARKING BLACK	
103	REF	03351	SCHEMATIC DIAGRAM	
104	REF	02208	PRODUCT SPECIFICATION	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65087 B/M
SHEET 5 OF 6

REV. L

TITLE: S34 SMD CONTROLLER, MASTER ASSEMBLY

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
105	1	12602	CAP SIL MICA 330pf ±5%	C10
106	1	12506	CAP SIL MICA 470pf ± 5%	C32
107	REF	16985B	I.C., FPLA 534 DMA SEQ 825153 PROG. (S34)	REF, Z28
108	1	10122	RES. CC ¼W 10KΩ	R50
109	1	43123	STIFFENER BAR	
110	10	26407	SCR, FH, PHL, 82° STL 2-56 x 1/2	
111	10	26101	NUT, HEX, STL, 2-56	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65087
B/M
SHEET 6 OF 6

REV L

65097 SHEET 1 OF 2

REVISIONS

SYM.	SHEET	DESCRIPTION		APPROV.	DATE
A		Release to Production + ECN 3060	C.L	JCP	1/3/83
B		ECN 3071A	C.L.	JCP	2/2/83
C		ECN 3137	BL	JCP	4/12/83
D		ECN 3169	BL	JCP	4/12/83
E		ECN 3182	BL	JCP	4/12/83
F		ECN 3187	BL	JCP	4/12/83
G		ECN 3194	JEJ	Carol Ly	12.5.83
H		ECN 3240	JEJ	Carol Ly	12.5.83
J		ECN 3256	JEJ	Carol Ly	12.5.83
K		ECN 3339	JEJ	Carol Ly	12.5.83
L		ECN W3506	L	Carol Ly	2.5.84
M		ECN 3596	M	Carol Ly	4.10.84

DRAWN DLL	DATE 12.13.82	TITLE S34/A SMD CONTROLLER
CHECKED C. Leeds	DATE 12-14-82	
ENGR. JCP	DATE 1/3/83	
APPROVED REW	DATE 1/04/83	DATARAM CORPORATION CRANBURY NEW JERSEY

DWG. NO. 65097 REV. M

SHEET 1 OF 2

USE B/M AND ASSY. 65087 WITH THE FOLLOWING EXCEPTIONS:

B/M

ITEM #56; QTY.1; 08584A FIRMWARE RM02 PIO DEC PROM S34/A
ITEM #61; QTY.1; 08585A FIRMWARE RM02 DRIVE CONFIG. PROM S34/A
ITEM #65; QTY.6; 08583D FIRMWARE RM02/05 EMULATION S34/A
ITEM #73; QTY.3; 08582A FIRMWARE RM02 DISC SEQ. S34/A

ASSEMBLY

ADD TO TABLE 1, THE FOLLOWING JUMPER: E8 PIN 1-2.

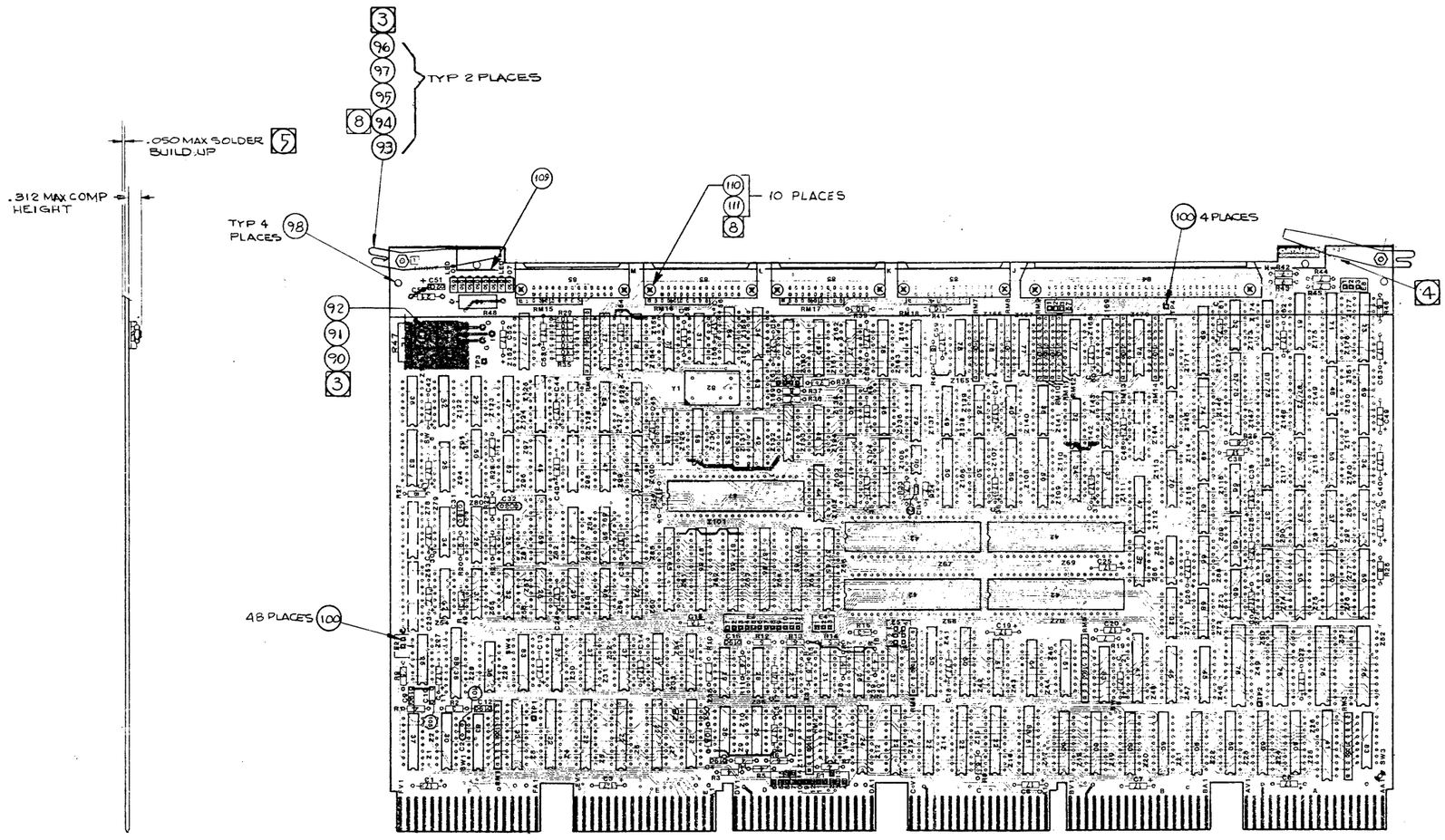
INSTALL PROMS PER CHART BELOW:

PROM	LOCATION	PROM	LOCATION
582-147	Z147	583-64	Z64
582-148	Z148	583-65	Z65
582-149	Z149	583-66	Z66
583-61	Z61	584-84	Z84
583-62	Z62	585-17	Z17
583-63	Z63		

STANDARD SWITCH SETTINGS								
SWITCH #	8	7	6	5	4	3	2	1
1	C	O	O	O	C	O	O	O
2	C	O	O	C	O	C	O	O
3	C	C	C	C	C	C	C	C
4	O	O	O	C	O	O	O	O
5	C	C	C	C	C	C	C	C
6	C	O	O	O	O	O	O	O

NOTE: "C" INDICATES CLOSED.
"O" INDICATES OPENED.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	X0	PRE PRODUCTION RELEASE	[illegible]	[illegible]
	A	RELEASE TO PRODUCTION + ECN 3060	1/3/83	JCP
	B	ECN 3071	2/2/83	JCP
	C	ECN 3137 GL	4/14/83	JCP
	D	ECN 3169 GL	4/14/83	JCP
	E	ECN 3172 GL	4/12/83	JCP
	F	ECN 3182 GL	4/14/83	JCP
	G	ECN 3187 GL	6/7/12/83	JCP
	H	ECN 3240 JEJ	12.5.83	Mark Ky
	J	ECN 3256 JEJ	12.5.83	Mark Ky
	K	ECN 3339 JEJ	12.5.83	Mark Ky



NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SCHEMATIC DIAGRAM SEE DRAWING No. 03351.
2. COMPONENT DESIGNATIONS ARE FOR REFERENCE PURPOSES ONLY AND DO NOT APPEAR ON COMPONENT PART.
3. INSTALL AFTER FLOW SOLDER.
4. MARK LATEST REVISION LETTER, SERIAL No. AND EIA DATA CODE WITH .12 HIGH CHARACTERS USING INK ITEM 102.
5. COMPONENT LEAD TRIM AND SOLDER BUILD UP AS NOTED.
6. SQUARE PAD DENOTES PIN 1 OF RESISTOR MODULES
7. INSTALL JUMPERS PER TABLE 1
8. CLIP SCREWS AND DEBURR. CLIP E7 JUMPER PINS FOR CLEARANCE.

(7)

TABLE 1		NOTE
"E" No.	JUMPER	
E1	2-13, 5-6, 7-14, 8-15, 9-10, 11-12	BRS
E2	1-2	THROTTLE
E3	NONE	TEST
E4	2-3	RESERVED
E5	NONE	RESERVED
E6	NONE	TEST
E7	2-3	BSY DISABLE

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± 1/2 DECIMALS .XX ±.02 .XXX ±.010 ANGLES ± /
MATERIAL —
FINISH —
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN T. PIERCE	5-3-82
CHECKED G. Lynde	9-7-82
ENGR. JCP	9.10.82
APPROVED R E W	1/04/83

DATARAM CORPORATION
CRANBURY NEW JERSEY

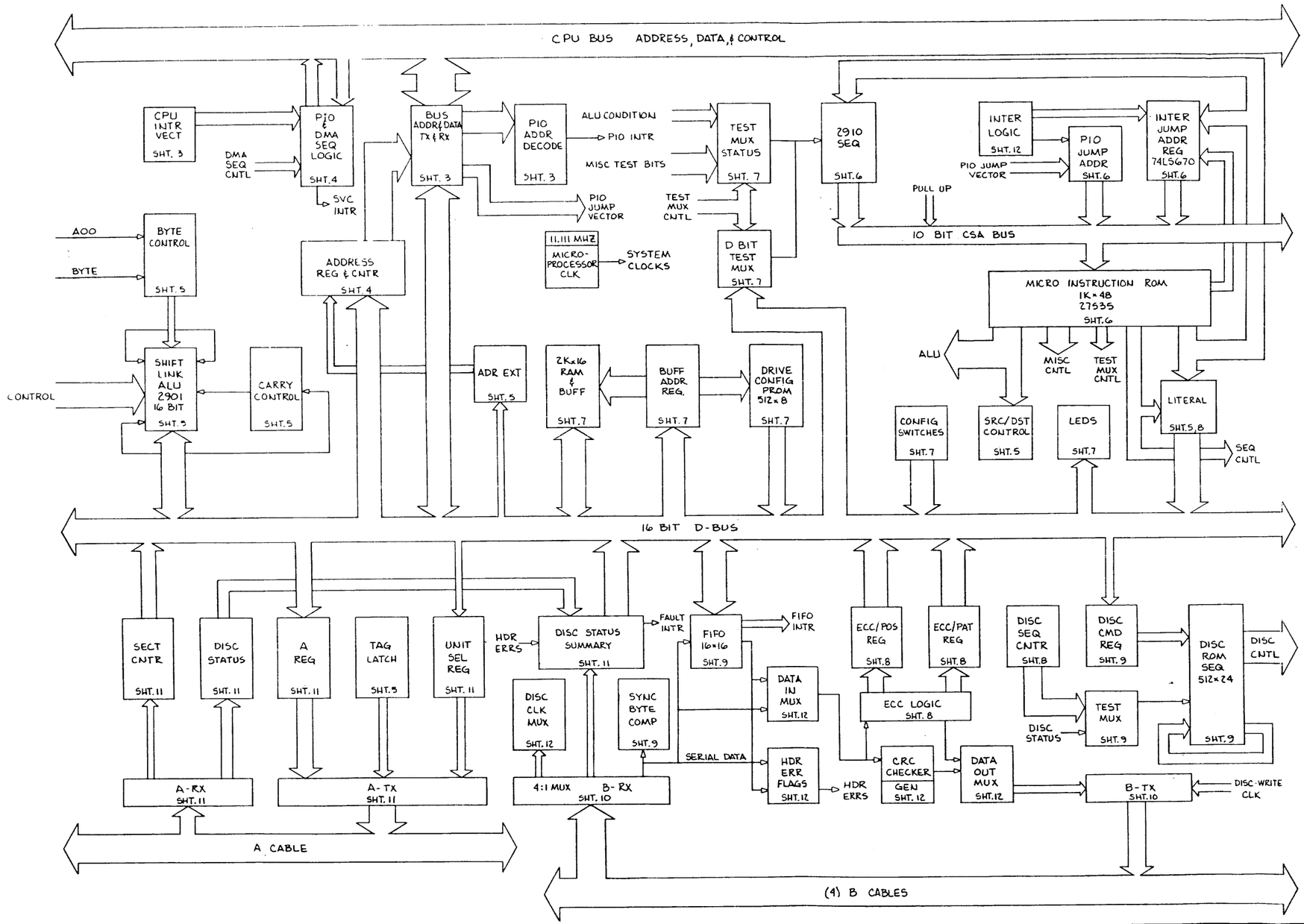
ASSEMBLY 534 SMD DISC CONTROLLER MASTER

SIZE	CODE IDENT NO.	DRAWING NO.	REV
	50473	65087	K

SCALE 1:1 SHEET 1 OF 1

65087

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	X₀	PRE-PRODUCTION RELEASE CK	9/10/82	JCP
	A	RELEASE TO PRODUCTION ECN+ECN 3060	1/3/83	JCP
	B	ECN=3071 CK.	2/2/83	JCP
	C	ECN 3137 BK	4/12/83	JCP
	D	ECN 3182 BK	4/12/83	JCP
	E	ECN W3195 CK.	5/2/83	JCP
	F	ECN W3256 MBJ	12.5.85	Carl Ty
	G	ECN W3359 MBJ	12.5.85	Carl Ty



BLOCK DIAGRAM

	65087
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN L. McMINN	8/16/82
CHECKED C. LEEDS	8/20/82
ENG. JCP	9/10/82
APPROVED REW	10/4/82

DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC DIAGRAM
S34 SMD/CMD
CONTROLLER-MASTER-

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G

SCALE | SHEET 1 OF 12

03351

A			
A			A
B			B
C		GND	C
D			D
E			E
F			F
H			H
J			J
K			K
L			L
M			M
N			N
P			P
R			R
S			S
T	GND		T
U			U
V			V

B			
A			A
B			B
C		GND	C
D			D
E			E
F			F
H			H
J			J
K			K
L			L
M			M
N			N
P			P
R			R
S			S
T	GND		T
U			U
V			V

C			
A	BUSNPGH	+5V	A
B	BUSBGOUTH		B
C		GND	C
D		BUSDISN	D
E		BUSDI4N	E
F		BUSDI3N	F
H	BUSDIIN	BUSDI2N	H
J		BUSDI1N	J
K		BUSD09N	K
L		BUSD08N	L
M		BUSD07N	M
N	BUSDCLOL	BUSD04N	N
P		BUSD05N	P
R		BUSD01N	R
S	BUSPBL	BUSD00N	S
T	GND	BUSD03N	T
U		BUSD02N	U
V		BUSD06N	V

D			
A		+5V	A
B			B
C		GND	C
D		BUSBR7L	D
E		BUSBR6L	E
F		BUSBR5L	F
H		BUSBR4L	H
J			J
K		BUSBGINTH	K
L	BUSINITL	BUSBGOUT7	L
M		BUSBGIN6H	M
N		BUSBGOUT6	N
P		BUSBGIN5H	P
R		BUSBGOUT5	R
S		BUSBGIN4H	S
T	GND	BUSBGOUT4	T
U			U
V			V

E			
A		+5V	A
B			B
C	BUSAI2L	GND	C
D	BUSAI1L	BUSAI5L	D
E	BUSMSYNCL	BUSAI6L	E
F	BUSAD2L	BUSCIL	F
H	BUSAOIL	BUSAOOL	H
J	BUSSSYNCL	BUSCOL	J
K	BUSAI4L	BUSAI3L	K
L	BUSAIIL		L
M			M
N		BUSAO8L	N
P	BUSAIOL	BUSAO7L	P
R	BUSAO9L		R
S			S
T	GND		T
U	BUSAO6L	BUSAO4L	U
V	BUSAO5L	BUSAO3L	V

F			
A		+5V	A
B		-15V	B
C		GND	C
D	BUSBBSYL		D
E			E
F			F
H			H
J	BUSNPRL		J
K			K
L			L
M	BUSINTRL		M
N			N
P			P
R			R
S			S
T	GND	BUSSACKL	T
U			U
V			V

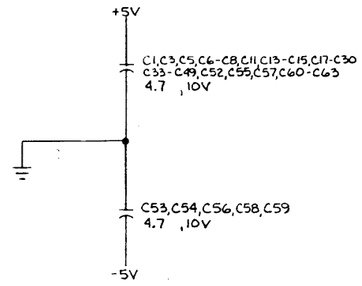
H			
1	TAG1	TAG1	31
2	TAG 2	TAG2	32
3	TAG 3	TAG 3	33
4	DBIT 0	DBIT 0	34
5	DBIT 1	DBIT 1	35
6	DBIT 2	DBIT 2	36
7	DBIT 3	DBIT 3	37
8	DBIT 4	DBIT 4	38
9	DBIT 5	DBIT 5	39
10	DBIT 6	DBIT 6	40
11	DBIT 7	DBIT 7	41
12	DBIT 8	DBIT 8	42
13	DBIT 9	DBIT 9	43
14	OPEN CABLE DET	OPEN CABLE DET	44
15	FAULT	FAULT	45
16	SEEK ERROR	SEEK ERROR	46
17	ON CYLINDER	ON CYLINDER	47
18	INDEX MARK	INDEX MARK	48
19	UNIT READY	UNIT READY	49
20			50
21	BUSY	BUSY	51
22	UNIT SELECT TAG	UNIT SELECT TAG	52
23	UNIT SELECT 2^0	UNIT SELECT 2^0	53
24	UNIT SELECT 2^1	UNIT SELECT 2^1	54
25	SECTOR MARK	SECTOR MARK	55
26	UNIT SELECT 2^2	UNIT SELECT 2^2	56
27	UNIT SELECT 2^3	UNIT SELECT 2^3	57
28	WRITE PROTECT	WRITE PROTECT	58
29	POWER PICK	POWER HOLD	59
30			60

J			
1	GND	SERVO CLK1	14
2	SERVO CLK1	GND	15
3	READ DATA1	READ DATA1	16
4	GND	READ CLK1	17
5	READ CLK 1	GND	18
6	WRT CLK 1	WRT CLK 1	19
7	GND	WRT DATA1	20
8	WRT DATA 1	GND	21
9	UNIT SELD1	UNIT SELD 1	22
10	SEEK END 1	SEEK END1	23
11	GND		24
12		GND	25
13			26

K			
1	GND	SERVO CLK 2	14
2	SERVO CLK 2	GND	15
3	READ DATA 2	READ DATA 2	16
4	GND	READ CLK 2	17
5	READ CLK2	GND	18
6	WRT CLK2	WRT CLK 2	19
7	GND	WRT DATA2	20
8	WRT DATA 2	GND	21
9	UNIT SELD 2	UNIT SELD 2	22
10	END SEEK2	END SEEK2	23
11	GND		24
12		GND	25
13			26

L			
1	GND	SERVO CLK 3	14
2	SERVO CLK 3	GND	15
3	READ DATA 3	READ DATA 3	16
4	GND	READ CLK 3	17
5	READ CLK 3	GND	18
6	WRT CLK 3	WRT CLK 3	19
7	GND	WRT DATA 3	20
8	WRT DATA 3	GND	21
9	UNIT SELD 3	UNIT SELD 3	22
10	SEEK END 3	SEEK END 3	23
11	GND		24
12		GND	25
13			26

M			
1	GND	SERVO CLK 4	14
2	SERVO CLK 4	GND	15
3	READ DATA 4	READ DATA 4	16
4	GND	READ CLK 4	17
5	READ CLK 4	GND	18
6	WRT CLK 4	WRT CLK 4	19
7	GND	WRT DATA 4	20
8	WRT DATA 4	GND	21
9	UNIT SELD 4	UNIT SELD 4	22
10	SEEK END 4	SEEK END 4	23
11	GND		24
12		GND	25
13			26



STANDARD JUMPER CONFIGURATION		NOTE
'E' N2	INSTALL JUMPER ON PINS:	
1	2-13; 5-6; 7-14; 8-15; 9-10; 11-12	BRS
2	1-2	THROTTLE
3	NONE	TEST
4	2-3	RESERVED
5	NONE	RESERVED
6	NONE	TEST
7	2-3	BSY DISABLE

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS CARBON COMPOSITION 1/4 W.
2. ALL CAPACITORS ARE IN μF
3. ALL DIODES ARE DATARAM P/N 18101.

LAST COMPONENT LIST	
INTEGRATED CIRCUIT	Z 177
RESISTOR MODULE	RM 18
RESISTOR	R 50
CAPACITOR	C 63
SWITCH	SW 6
JUMPER / STRAPPING POINTS	E 8
DIODE LED	LED 07
TEST POINT	TP4

ENABLE DUAL PORT	DISABLE DUAL PORT (STD.)
REMOVE E7-2 TO 3	REMOVE E7-1 TO 2
ADD E7-1 TO 2	ADD E7-2 TO 3

DMA BURST SIZE

SW4	1	2	3	4	5	6	7	8
WORDS/BURST	1	2	4	8	16	32	64	128

} SET 1 AND ONLY 1 SWITCH TO "ON" OR "CLOSED."

NPR OFF TIME

SW6	*	8	7	6	5	1	2	3	4
4 SEC.	Ø	3	6	12	24	48	96	192	384

} SET 1 AND ONLY 1 SWITCH TO "ON" OR "CLOSED".

* NO SWITCH "ON" OR "CLOSED"

CSR ADDRESS SW1 (760000_8 - 777700_8)

ADDRESS BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW1	-	-	-	1	2	3	4	5	6	7	8	-	-	-	-	-
776700_8	-	-	-	O	O	O	C	O	O	O	C	-	-	-	-	-
777400_8	-	-	-	O	O	O	O	O	C	C	C	-	-	-	-	-
776300_8	-	-	-	O	O	O	C	C	O	O	C	-	-	-	-	-

VECTOR ADDRESS SW2 ($Ø$-374_8)

VECTOR BIT	-	7	6	5	4	3	2	1	0
SW2	-	6	5	4	3	2	1	-	-
VECT=210_8	-	O	C	C	C	O	C	-	-
VECT=254_8	-	O	C	O	C	O	O	-	-

"O" SIGNIFIES OPEN OR OFF AND IS EQUAL TO A "1"
"C" SIGNIFIES CLOSED OR ON AND IS EQUAL TO A "Ø"

REF. DESIG.	GATES USED	/	TOTAL GATES	TYPE
Z94	1	/	2	74LS74
Z123	1	/	2	74LS74
Z11	3	/	4	7438
Z36	3	/	4	8640
Z38	3	/	4	74LS32
Z55	3	/	4	74LS32
Z71	3	/	4	74500
Z40	3	/	4	74500
Z128	2	/	4	74500
Z142	3	/	4	74500
Z79	1	/	4	74586
Z158	3	/	4	74586
Z110	3	/	4	74586
Z86	1	/	4	74500
Z134	2	/	3	74510
Z138	4	/	6	74504
Z140	3	/	4	74532
Z59	3	/	4	74532
Z122	2	/	4	74500
Z54	1	/	4	74LS08

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G
SCALE			SHEET 2 OF 12

03351

(4B7) IADR 15
(4B7) IADR 14
(4B7) IADR 13
(4C7) IADR 12

(4C7) IADR 11
(4C7) IADR 10
(4C7) IADR 9
(4C7) IADR 8

(4C7) IADR 7
(4C7) IADR 6
(4D7) IADR 5
(4D7) IADR 4

(4D7) IADR 3
(4D7) IADR 2
(4D7) IADR 1

A00L EH2 — Z6 2908 BUS2 — A00 (5A1)
A01L EH1 — BUS1 — A01 (6A1)
A02L EF1 — BUS3 — A02 (6A7)
A03L EV2 — BUSO — A03 (6A7)
BE, RLE, DRCP, GND1, GND2, OE

A04L EU2 — Z4 2908 BUSO — A04 (6A7)
A05L EV1 — BUS3
A06L EU1 — BUS1
A07L EP2 — BUS2
BE, RLE, DRCP, GND1, GND2, OE

A08L EN2 — Z5 2908 BUS2
A09L ER1 — BUS1
A10L EP1 — BUS3
A11L EL1 — BUSO
BE, RLE, DRCP, GND1, GND2, OE

A12L EC1 — Z7 2908 BUSO
A13L EK2 — BUS3
A14L EK1 — BUS1
A15L ED2 — BUS2
BE, RLE, DRCP, GND1, GND2, OE

IBBSYN (4D5)

(5B7,4D5) IC1
(4B7) IADR17
(4B7) IADR16

A16L EE2 — Z8 2908 BUSO
A17L ED1 — BUS3
COL EJ2 — BUS1
CIL EF2 — BUS2
BE, RLE, DRCP, GND1, GND2, OE
R1 — CO (5A7)
R2 — C1 (4B3, 6A7)

ADRLD (4D3)

A13, A14, A15 — Z9 74LS30 — 8

(5B4) DBUS 15
(5B4) DBUS 14
(5B4) DBUS 13
(5B4) DBUS 12

(5B3) DBUS 11
(5B3) DBUS 10
(5B3) DBUS 09
(5B3) DBUS 08

(5B2) DBUS 07
(5B2) DBUS 06
(5B2) DBUS 05
(5B2) DBUS 04

(5B1) DBUS 03
(5B1) DBUS 02
(5B1) DBUS 01
(5B1) DBUS 00

D00L CS2 — Z13 2908 BUS3
D01L CR2 — BUS2
D02L CU2 — BUS1
(3B1) — BUSO
D03L CT2 — BE, RLE, DRCP, GND1, GND2, OE
(3B1)

(5B5) IDATAN

D04L CN2 — Z14 2908 BUS3
(3B1) — BUSO
D05L CP2 — BUS1
(3A1) — BUS2
D06L CU2 — BE, RLE, DRCP, GND1, GND2, OE
(3A1)
D07L CM2
(3A1)
(4B1) DOUTN

D08L CL2 — Z15 2908 BUS1
D09L CK2 — BUSO
D10L CJ2 — BUS3
D11L CH1 — BUS2
BE, RLE, DRCP, GND1, GND2, OE

BUS ADDRESS & DATA TX & RX
(5A3) ODATAN

D12L CH2 — Z16 2908 BUS1
D13L CF2 — BUSO
D14L CE2 — BUS3
D15L CD2 — BUS2
BE, RLE, DRCP, GND1, GND2, OE

(6D1) CLK — Z38 74LS32 — 3

A12, A11, A10, A09, A08, A07, A06 — E IN, E OUT — ADDEN (6A7)
PIO ADDRESS DECODE
Z3 25LS2521

SW1
CSR ADDRESS
760000_8-777740_8
OPEN = 1
RM1 1K
+5V

Z79 74S86 — A05B (6A7)

(4D5) IBBSYN — Z11 7438
(5B7) BR

E1
DH2 BR4L
DF2 BR5L
DE2 BR6L
DD2 BR7L
DS2 BG4HI
DT2 BG4HO
DP2 BG5HI
DR2 BG5HO
DM2 BG6HI
DN2 BG6HO
DK2 BG7HI
DL2 BG7HO
INTERRUPT PRIORITY

+5V
R7 180
Z10 74LS74
Z11 7438

+5V
R5 180
R6 390
Z36 8640
Z11 7438
+5V
R3 180
R4 180
C4 .001
Z37 74LS11
Z38 74LS32 — GRANT (4D5)

R11 180
C16 .001
Z37 74LS11

+5V
R17 180
INPR (4D2)
NPGHI (CA1)
R8 390
Z39 8640
Z35 7438
+5V
R10 680
Z10 74LS74
+5V
R18 180
Z35 7438 — NPGHO (CB1)

(12D4) RESETN
BPB CS1 — Z39 8640
Z81 74LS74 — UPE (7D8)
(4CS) IDATPN
(4D3) IBBSY — Z56 74LS00 — UPEN (12B3)
(5A7) CCLRN

SW2
VECTOR ADDRESS
ϕ-374_8
OPEN = 1
TEST "D"
TEST "E"
TEST D (7C8)
TEST E (7C8)
RM2 1K
+5V

Z12 74S240
(4D3) INTRN
D02L (3C6)
D03L (3C6)
D04L (3C6)
D05L (3C6)
D06L (3C6)
D07L (3C6)
CPU INTR VECT

UNIBUS INTERFACE

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G
SCALE			SHEET 3 OF 12

03351

ADDRESS REGISTER & COUNTER

Z32 74LS161
(4B1) DBUS01
(5B1) DBUS02
(5B2) DBUS03
(5B2) DBUS04
(4C4) ADRCNTN
(4C4) ENBCTN
(12D3) RESETN
(5A3) MARN
IADR1 (3D8)
IADR2 (3D8)
IADR3 (3D8)
IADR4 (3D8)

Z30 74LS161
(5B2) DBUS05
(5B2) DBUS06
(5B2) DBUS07
(5B3) DBUS08
IADR5 (3D8)
IADR6 (3D8)
IADR7 (3D8)
IADR8 (3D8)

Z31 74LS161
(5B3) DBUS09
(5B3) DBUS10
(5B3) DBUS11
(5B4) DBUS12
IADR9 (3D8)
IADR10 (3D8)
IADR11 (3D8)
IADR12 (3D8)

Z34 74LS161
(5B4) DBUS13
(5B4) DBUS14
(5B4) DBUS15
(5A7) IA16
IADR13 (3D8)
IADR14 (3D8)
IADR15 (3D8)
IADR16 (3A8)

Z33 74LS161
(5A7) IA17
IADR17 (3A8)

DMA BURST SIZE (SET ONLY ONE SW)

Z29 74LS393
SW4
IBBSYN (3B8, 3D3, 4A2)

Z60 74LS04

Z1 74LS161
CLK (6D1)

Z60 74LS04

+5V
R27 1K
SW6
NPR OFF TIME (SET ONLY ONE SW)

Z121 74LS393

Z55 74LS132
R45 100Ω
C2 240pf

(3C1) GRANT
(3A8) IC1
(5B7) BR
(5B7) DMAR
(3B4) IDATPN
(5B5) ODADRN
(5A7) BAIN

DMA SEQUENCE LOGIC

Z28 82S153 FPLA
(3C3) INPR
ISACK (4B3)
IBBSY (3A4)
ADRLD (3A8)
SVC (12B2)
IMSYNC
INTRN (3B3)
R9 330Ω
C9 .001

Z56 74LS00
74S04 Z87
Z56 74LS00
74S04 Z87
R1 180Ω
C10 330pf
ADRCNTN (4D8)

Z58 74S08
ENBCNT (4D8)
Z55 74LS32
DMABSY (7D8)

(4A1) JIBBSY
Z35 7438
Z60 74LS04
Z35 7438
FT2 SACKL
SACKL (4B2)
FM1 INTRL
FD1 BBSYL
EE1 MSYNL
MSYNC (4B4)
EJ1 SSYNL
FJ1 NPRL
Z2 8641
R2 100Ω
C12 .001

PIO LOGIC
C1 (3A7)
Z56 74S00
Z58 74S08
DOUTN (3C6)
Z59 74S32

(5A7) BUSSEQN
(4D1) MSYNC
Z57 74LS74
(6A6) PIOSELN
Z60 74LS04
Z57 74LS74
PION (12C4)
(12C2) PIOCLN

SACKL (4D1)
ISACK (4D3)
Z54 74LS08
Z36 8640
REQBUS (4B6)
JIBBSY (4D2)
+5V
R50 10K
E2
IN = THROTTLE
OUT = FIXED BURST
(4D5) IBBSYN
(5B7) THROTN
Z38 74LS32

REQBUS (4B1)
Z27 74LS74
Z27 74LS74

+5V
R21 680
R22 150K
C32 470pf
25MS
Z80 74LS123
Z81 74LS74
DCLON (12C6)
PU1 (12C7, 5A8)
NXM (7D8)
NXMN (12B3)
(5A7) CCLRN

B REV.
03351

DMA LOGIC

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G
SCALE			SHEET 4 OF 12

BISHOP GRAPHICS / ACCUPRESS RECORDER NO. A 9559

(5B1) DBUS 00
(5B1) DBUS 01
(5B1) DBUS 02
(5B1) DBUS 03
(5B2) DBUS 04
(5B2) DBUS 05
(5B2) DBUS 06
(5B2) DBUS 07

Z104
74LS244

(6C4) MIR 00

LITERAL LOW BYTE

Z100
74LS259

(6A1) MIR 44
(6A1) MIR 45
(6A1) MIR 46
(6A1) MIR 47

A- LATCH

THROTN (4A2)
IRENB (12B5)
ORENB (12B5)
PUP (10B)
BR (3D3, 4D5)
DMAR (4C5)

(12C6) DCLON

Z136
74LS259

(6B1) MIR 40
(6B1) MIR 41
(6A1) MIR 42
(6A1) MIR 43

B-LATCH

US TAG (11D)
ICI (3A8)
TAG1 (11D)
TAG2 (11D)
TAG3 (11C)
ECI (9A8)
HC IN (12B2)

(5A3) LATCHN
(12C3) SRESETN

(5B3) DBUS 08
(5B3) DBUS 09
(5B3) DBUS 10
(5B3) DBUS 11

(5B4) DBUS 12
(5B4) DBUS 13
(5B4) DBUS 14
(5B4) DBUS 15

ALU
2901 16 BIT

(6C4) MIR 3
(6C4) MIR 2
(6C4) MIR 1
(6C4) MIR 7
(6C4) MIR 6
(6C4) MIR 5
(6B4) MIR 11
(6B4) MIR 10
(6B4) MIR 9
(6B4) MIR 12
(6B4) MIR 16

(5C1) QLINK
(5C1) RLINK

(5A1) CN+Z

Z69 2901
Z70 2901
Z67 2901
Z68 2901

CN+X (5D1)

QLINK (5C5)
R LINK (5C5)

+5V
R19 680

ALUZ (7D8)

DBUS 00 (5A8, 5D7, 7A4, 7C6, 3D5 7D5, 7C1, 8C1, 8A6, 9D3, 9D1, 11C3)
DBUS 01 (4D8, 5D7, 7A4, 7C6, 7D5, 7C1, 8A6, 9D8, 9D3, 9D1, 11C3, 3D5, 8C1)
DBUS 02 (4D8, 5D7, 7A4, 7C6, 3D5, 7D5, 7C1, 8B6, 9D3, 9D1, 11C3, 8C1)
DBUS 03 (4D8, 5D7, 7A4, 7C6, 3D5, 7D5, 7C1, 8B6, 9D8, 9D3, 9D1, 11C3, 8C1)

(6A4) MIR 22

Z112
74S138

EXT. DEST CLKS

BARN (7B6)
RAMIN (7B4)
ODADRN (4C5)
WFIFON (9C4)
AREGN (11B5)
DCMDENAN (9C5)
UNIT/LEDN (7D3, 11A5)

(6A4) MIR 19
(6A4) MIR 18
(6B4) MIR 17
(6C4) MIR 08
(6D1) CLKFF

Z99
74S138

IDATAN 3C6
RAMON 7B4
EN PARN (9A7, 4D6)
EN POSN 9B1
SCNTENAN (7A4, 9C5)
DSTATN (8B5, 11C5)
RFIFON (9A5)
TST WORDN (7A6)

EXT. SRC ENAS

SRC/DST CONTROL

(6B4) MIR 15
(6B4) MIR 14
(6B4) MIR 13
(6C4) MIR 00

Z83
74S138

(6C1) MIR 31
(6C1) MIR 30
(6C1) MIR 29
(6C1) MIR 24
(6D1) CLK

CLK IMKN (11A8)
CLR SMKN (11A8)
BUS SEQN (4B4)
CLRFIFON (9A3)
CCLRN (3A4, 4A7)
CLRDCKN (8C5)

Z97
74LS174

(5B1) DBUS 00
(5B3) DBUS 09
(5B3) DBUS 08

BAIN (9C5)
IAI7 (4B8)
IAI6 (4B8)

ADDRESS EXT.

(4A6) PU 1

(3C6) A00

Z133
74S158

BYTE CONTROL

(6D1) CLKN
(3A7) C0

Z134
74S10

Z132
74S04

(6D1) OSC

DBUS 08 (4C8, 5D5, 5A8, 7B6, 7D4, 7C3, 8C1, 8A3, 8D5, 9B3, 9B1, 11D3, 3D5)
DBUS 09 (4C8, 5D5, 5A8, 7B6, 7D4, 7C3, 8C1, 8A3, 8D5, 9B3, 9B1, 11D3, 3D5)
DBUS 10 (4C8, 5D5, 7B6, 7D4, 7C3, 8C1, 8A3, 8D5, 9B3, 9B1, 11D3, 3D5)
DBUS 11 (4C8, 5D5, 7A6, 7D4, 7C3, 8C1, 8A3, 8D5, 9B3, 9B1, 11D3, 3D5)

DBUS 12 (4C8, 5D5, 7A6, 7C4, 8B1, 8A3, 10D5, 9A3, 9A1, 11D3, 3D5)
DBUS 13 (4C8, 5D5, 7A6, 7C4, 8B1, 8A3, 8D5, 9A3, 9A1, 11D3, 3D5)
DBUS 14 (4C8, 5D5, 7A6, 7C4, 8B1, 8A3, 8D5, 9A3, 9A1, 11D3, 3D5)
DBUS 15 (4C8, 5D5, 7A6, 7C4, 8B1, 8A3, 8D5, 9A3, 9A1, 11D3, 3D5)

DBUS 04 (4D8, 5D7, 7A4, 7C6, 7D5, 7C2, 8C1, 8B6, 9D3, 9C1, 11C3, 3D5)
DBUS 05 (4D8, 5D7, 7A4, 7C6, 7D5, 7C2, 8C1, 8B6, 9D8, 9C3, 9C1, 11C3, 3D5)
DBUS 06 (4C8, 5D7, 7A4, 7C6, 7D5, 7C2, 8C1, 8B6, 9C3, 9C1, 11C3, 3D5)
DBUS 07 (4C8, 5D7, 7A4, 7C6, 7D5, 7C2, 8C1, 8B6, 9C3, 9C1, 11C3, 3D5)

(6D1) CLKN
(6C4) MIR 00
(6B1) MIR 36

Z134
74S10

Z135
74S32

LATCHN (5B8)

(6B1) MIR 37

Z132
74S04

LDVCTN (6C8)

ODATAN (3B6)

(6B4) MIR 16

MARN (4D8)

(6A4) MIR 20
(6A4) MIR 21

Z58
74S08

Z59
74S32

CARRY LOGIC

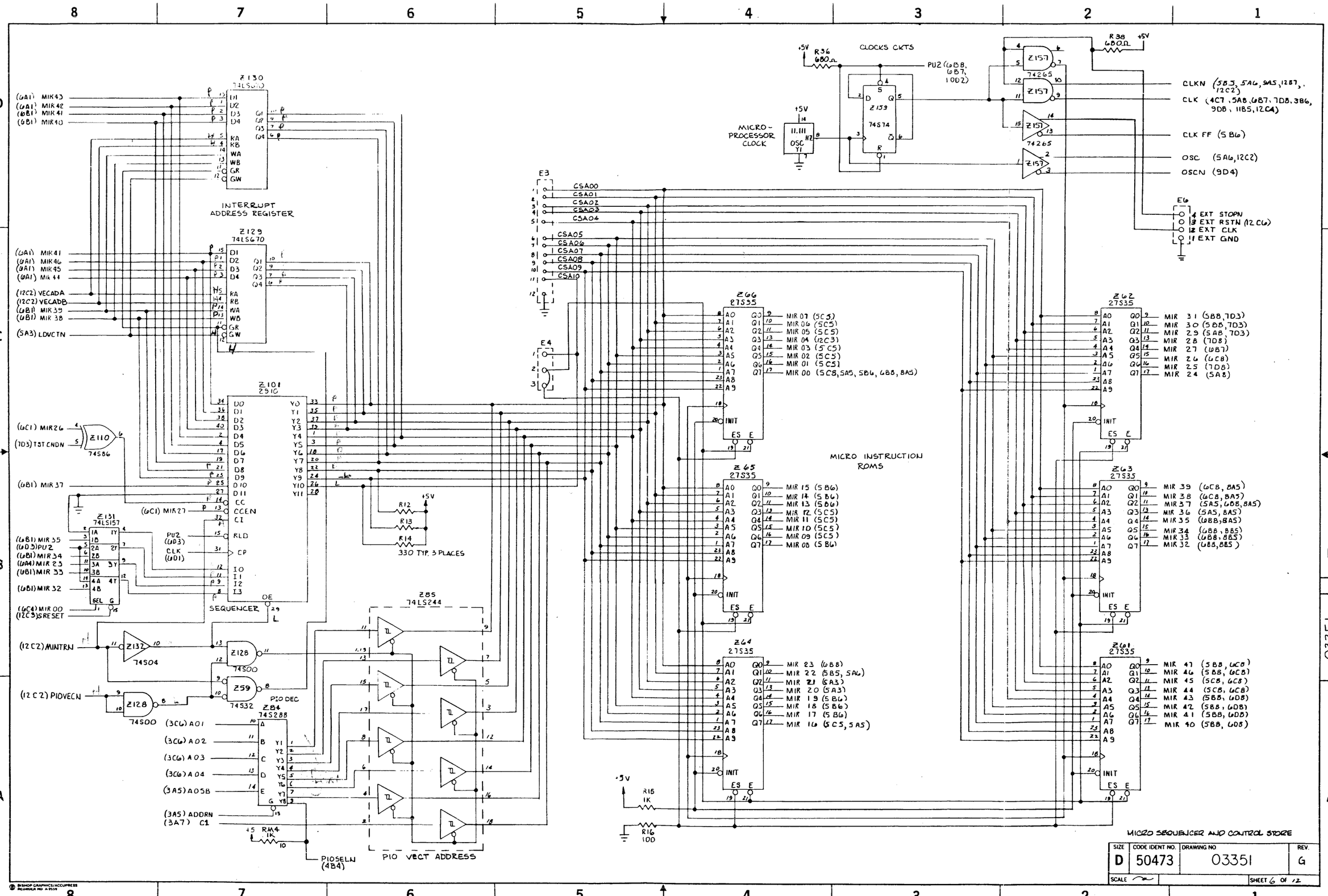
Z102
2902

CN+X (5B3)
CN+Y (5B4)
CN+Z (5B5)

DATA PROCESSOR

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G
SCALE		SHEET 5 OF 12	

03351


Z130 74LS670
(6A1) MIR43
(6A1) MIR42
(6B1) MIR41
(6B1) MIR40
INTERRUPT ADDRESS REGISTER
Z129 74LS670
(6A1) MIR47
(6A1) MIR46
(6A1) MIR45
(6A1) MIR 44
(12C2) VECADA
(12C2) VECADB
(6B1) MIR 39
(6B1) MIR 38
(5A3) LDVCTN
Z101 2910
(6C1) MIR26
(7D3) TSTCNDN
Z110 74S86
(6B1) MIR 37
(6C1) MIR 27
Z131 74LS157
(6B1) MIR 35
(6D3) PU2
(6B1) MIR 34
(6A4) MIR 23
(6B1) MIR 33
(6B1) MIR 32
(6C4) MIR 00
(12C3) SRESET
SEQUENCER
(12C2) MINTRN
Z132 74S04
Z128 74S00
(12C2) PIOVECN
Z59 74S32
PIO DEC
Z84 74S288
(3C6) A01
(3C6) A02
(3C6) A03
(3C6) A04
(3A5) A05B
(3A5) ADDRN
(3A7) C1
RM4 1K
PIOSELN (4B4)
Z85 74LS244
PIO VECT ADDRESS
R12
R13
R14
330 TYP. 3 PLACES
+5V
E3
CSA00
CSA01
CSA02
CSA03
CSA04
CSA05
CSA06
CSA07
CSA08
CSA09
CSA10
E4
Z66 27S35
MIR 07 (5C3)
MIR 06 (5C5)
MIR 05 (5C5)
MIR 04 (12C3)
MIR 03 (5C5)
MIR 02 (5C5)
MIR 01 (5C5)
MIR 00 (5C8, 5A5, 5B6, 6B8, 8A5)
Z65 27S35
MIR 15 (5B6)
MIR 14 (5B6)
MIR 13 (5B6)
MIR 12 (5C5)
MIR 11 (5C5)
MIR 10 (5C5)
MIR 09 (5C5)
MIR 08 (5B6)
Z64 27S35
MIR 23 (6B8)
MIR 22 (5B5, 5A6)
MIR 21 (5A3)
MIR 20 (5A3)
MIR 19 (5B6)
MIR 18 (5B6)
MIR 17 (5B6)
MIR 16 (5C5, 5A5)
INIT
ES E
MICRO INSTRUCTION ROMS
+5V
R15 1K
R16 100
CLOCKS CKTS
R36 680Ω
PU2 (6B8, 6B7, 10D2)
Z139 74S74
MICRO-PROCESSOR CLOCK
11.111 MHz OSC
Y1
R38 680Ω
Z157 74265
CLKN (5B3, 5A6, 9A5, 12B7, 12C2)
CLK (4C7, 5A8, 6B7, 7D8, 3B6, 9D8, 11B5, 12C4)
CLK FF (5B6)
OSC (5A6, 12C2)
OSCN (9D4)
E6
4 EXT STOPN
3 EXT RSTN (12C6)
2 EXT CLK
1 EXT GND
Z62 27S35
MIR 31 (5B8, 7D3)
MIR 30 (5B8, 7D3)
MIR 29 (5A8, 7D3)
MIR 28 (7D8)
MIR 27 (6B7)
MIR 26 (6C8)
MIR 25 (7D8)
MIR 24 (5A8)
Z63 27S35
MIR 39 (6C8, 8A5)
MIR 38 (6C8, 8A5)
MIR 37 (5A5, 6B8, 8A5)
MIR 36 (5A5, 8A5)
MIR 35 (6B8, 8A5)
MIR 34 (6B8, 8B5)
MIR 33 (6B8, 8B5)
MIR 32 (6B8, 8B5)
Z61 27S35
MIR 47 (5B8, 6C8)
MIR 46 (5B8, 6C8)
MIR 45 (5C8, 6C8)
MIR 44 (5C8, 6C8)
MIR 43 (5B8, 6D8)
MIR 42 (5B8, 6D8)
MIR 41 (5B8, 6D8)
MIR 40 (5B8, 6D8)
MICRO SEQUENCER AND CONTROL STORE
SIZE D
CODE IDENT NO. 50473
DRAWING NO 03351
REV. G
SCALE
SHEET 6 OF 12
03351
BISHOP GRAPHICS/ACCUPRESS

CONDITIONAL TEST MUX STATUS

Z42 74LS374 — Z43 74S251 — Z44 74S251 — Z45 74S251

(5B1) ALUZ
(5B4) ALUCO
(5B4) ALUNEG
(5B7) PUP
(11B5) RDY
(4A4) NMX
(4C4) DMABSY
(9A1) OREN
(6D1) CLK

(6C1) MIR 28
(6C1) MIR 25

Z41 74LS374

(9A1) IRFN
(8B3) DONEN
(3B3) UPE

E5 TST

(3A3) TESTD
(3A3) TESTE

RM4 1K

Z40 74S00 ×3

(5B1) DBUS 00
(5B1) DBUS 01
(5B1) DBUS 02
(5B1) DBUS 03
(5B2) DBUS 04
(5B2) DBUS 05
(5B2) DBUS 06
(5B2) DBUS 07

MIR 31 (6C1)
MIR 30 (6C1)
MIR 29 (6C1)

(5B3) DBUS 08
(5B3) DBUS 09
(5B3) DBUS 10
(5B3) DBUS 11

D BIT TEST MUX

TST CNDN (6C8)

Z82 74LS273

(5B5) UNIT/LEDN
DCLON (12C6)

+5V

LED 00
LED 01
LED 02
LED 03
LED 04
LED 05
LED 06
LED 07

DBUS 12 (5B4)
DBUS 13 (5B4)
DBUS 14 (5B4)
DBUS 15 (5B4)

DBUS 08 (5B3)
DBUS 09 (5B3)
DBUS 10 (5B3)
DBUS 11 (5B3)

DBUS 04 (5B2)
DBUS 05 (5B2)
DBUS 06 (5B2)
DBUS 07 (5B2)

DBUS 00 (5B1)
DBUS 01 (5B1)
DBUS 02 (5B1)
DBUS 03 (5B1)

Z25 Z22 Z21 Z18 — Z24 Z23 Z20 Z19 — 9148-70

2K×16 RAM & BUFF

Z47 74LS174 — BUFF ADDR REGISTER

(5B5) BARN

Z48 74LS174

RM5

SW5 — RM5 1K — Z46 74LS244

SW3 — RM3 1K — Z26 74LS244

CONFIGURATION SWITCHES

(5A5) TSTWORDN

DBUS 00 (5B1)
DBUS 01 (5B1)
DBUS 02 (5B1)
DBUS 03 (5B1)
DBUS 04 (5B2)
DBUS 05 (5B2)
DBUS 06 (5B2)
DBUS 07 (5B2)

DBUS 08 (5B3)
DBUS 09 (5B3)
DBUS 10 (5B3)
DBUS 11 (5B3)
DBUS 12 (5B4)
DBUS 13 (5B4)
DBUS 14 (5B4)
DBUS 15 (5B4)

(5B5) RAMIN
(5B5) RAMON

Z80 74S00 — Z71 74S00 — Z81 74S04 — Z71 74S00

Z17 82S29 — DRIVE CONFIGURATION PROM

SCNTENAN (5B5)

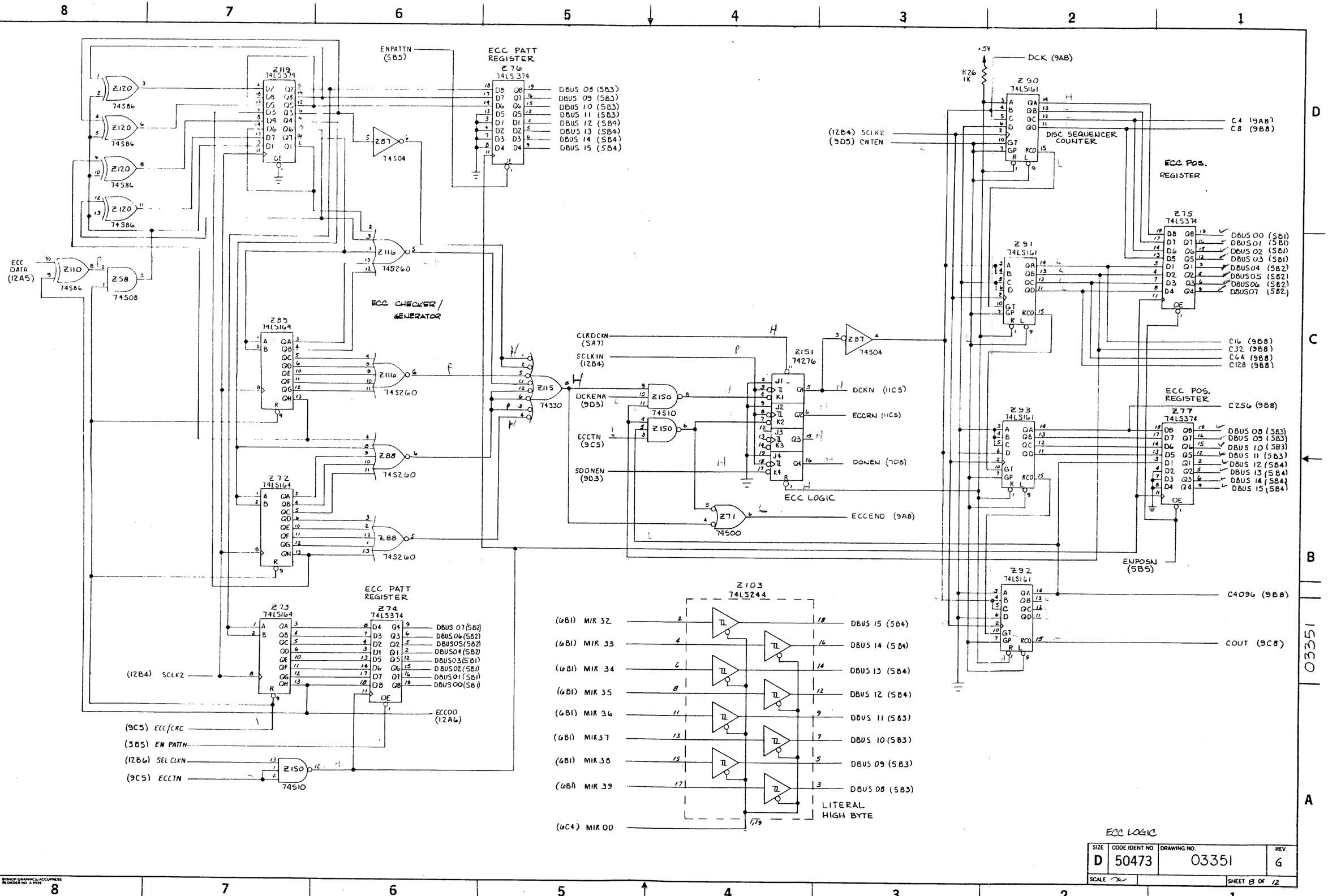
RAM BUFF. AND COND. TEST LOGIC

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G

SCALE — SHEET 7 OF 12

03351

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-9999



ECC LOGIC

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G
SCALE			SHEET 8 OF 12

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DISC DATA SEQUENCER

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G

SCALE

SHEET 8 OF 12

03351

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-9599

B-RX

SERVO CLK 1 — J2, J14
READ DATA 1 — J16, J3
READ CLK 1 — J5, J17
SEEK END 1 — J23, J10
UNIT SELD 1 — J22, J9
SERVO CLK 2 — K2, K14
READ DATA 2 — K16, K3
READ CLK 2 — K5, K17
SEEK END 2 — K23, K10
UNIT SELD 2 — K22, K9
SERVO CLK 3 — L2, L14
READ DATA 3 — L16, L3
READ CLK 3 — L5, L17
SEEK END 3 — L23, L10
UNIT SELD 3 — L22, L9
SERVO CLK 4 — M2, M14
READ DATA 4 — M16, M3
READ CLK 4 — M5, M17
SEEK END 4 — M23, M10
UNIT SELD 4 — M22, M9

RM18 8Z — Z164 MC3450 — R34 22K — RM6 8Z — Z153 MC3450 — R41 22K
RM17 8Z — Z162 MC3450 — R32 22K — RM6 8Z — Z153 MC3450 — R39 22K
RM16 8Z — Z155 MC3450 — R31 22K — RM6 8Z — Z153 MC3450 — R29 22K
RM15 8Z — Z152 MC3450 — R33 22K — RM6 8Z — Z153 MC3450 — R30 22K
+5V, -5V, VEE

SERCLKN (12B7)
R DATA (9C8)
RD CLKN (12B7)
SKEDN (11C5)

Z127 74LS20 — UNSELD (11C5)

BUS -15V — FB2 — R47 7.5 3W 1% — R48 7.5 3W 1% — C51 1 — C50 .1 — Q1 LM820T5.0 — -5V

(6D3) PU2 — WDOUT (12A5) — SCLK2 (12B4) — Z159 74S74 — Z158 74S86

PU5 (11D2) — Z163 MC3453 — J19 WRT CLK 1, J6; J20 WRT DATA 1, J8; K19 WRT CLK 2, K6; K20 WRT DATA 2, K8

R35 1K — Z154 MC3453 — L19 WRT CLK 3, L6; L20 WRT DATA 3, L8; M19 WRT CLK 4, M6; M20 WRT DATA 4, M8

B-TX

SMD "B" CABLE

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G
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03351

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 9559

A-RX

SECTOR MARK
INDEX MARK
FAULT
SEEK ERROR
ON CYLINDER
UNIT READY
WRITE PROTECT
BUSY

RM11 22K
RM10 22K
RM12 56
RM9 56

Z168 MC3450
Z167 MC3450

IOSMK (9C8)

Z140 74S32
Z138 74S04

SECTOR COUNTER
Z141 74LS393

FAULTN (12B3)

Z109 74LS374
DBUS 08 (5B3)
DBUS 09 (5B3)
DBUS 10 (5B3)
DBUS 11 (5B3)
DBUS 12 (5B4)
DBUS 13 (5B4)
DBUS 14 (5B4)
DBUS 15 (5B4)

SCNTENAN (5B5)

Z108 74LS374
(12A1) BSERN
(12A1) FMTN
(12B1) HECN
(8C3) DCKN
(8C3) ECCRN
(12A1) CRCRN

DISC STATUS SUMMARY
DBUS 00 (5B1)
DBUS 01 (5B1)
DBUS 02 (5B1)
DBUS 03 (5B1)
DBUS 04 (5B2)
DBUS 05 (5B2)
DBUS 06 (5B2)
DBUS 07 (5B2)

(11B6) BSY
(10A3) UNSELD
(10D3) SKEND
(6D1) CLK
(5A5) DSTATN

Z107 74LS374

RDY (7D8)

1E7
BSY (11B5)

DISC STATUS

PU5 (11D2)

Z139 74LS74
Z139 74LS74

(5A7) CLRIMKN
(5A7) CLRSMKN

Z106 74LS374
A-REG

(5B5) AREGN

Z137 74LS375
UNIT SELECT REGISTER

Z138 74S04
(5B3) UNIT/LEDN

WRT GATE (9C5)
RD GATE (9C5)

Z140 74S32
Z140 74S32

+5V
R40 1K (11B7) PU5

Z165 MC3453
RM7 56

(5B7) US TAG
(5B7) TAG 1
(5B7) TAG 2
(5B7) TAG 3

UNIT SELECT TAG
TAG 1
TAG 2
TAG 3

Z169 MC3453
RM13 56

DBIT 2
DBIT 3
DBIT 4
DBIT 5

Z170 MC3453
RM14 56

DBIT 6
DBIT 7
DBIT 8
DBIT 9

Z166 MC3453
RM8 56

UNIT SELECT 2
UNIT SELECT 2
DBIT 0
DBIT 1

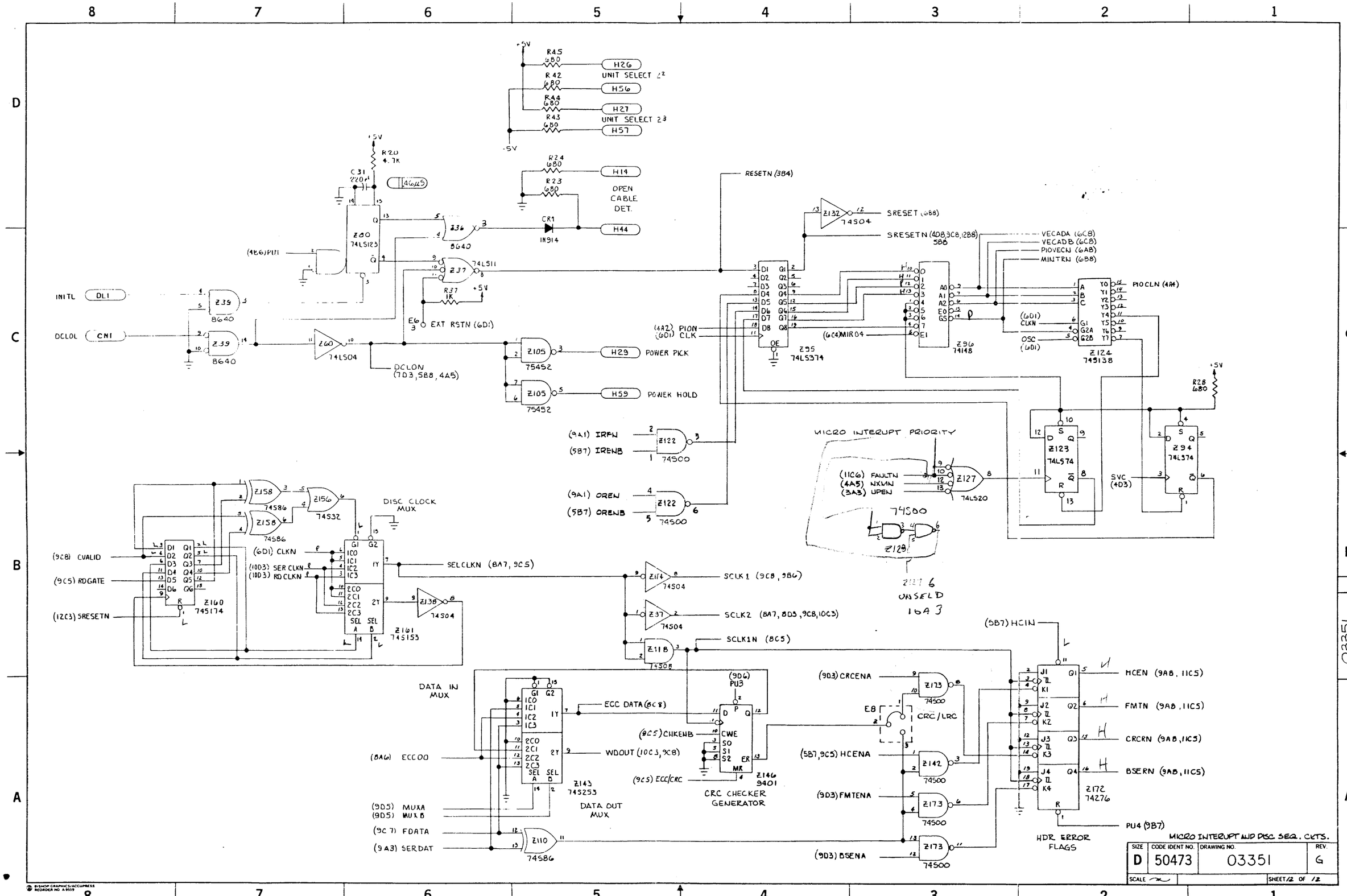
A-TX
SMD "A" CABLE

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G

SCALE
SHEET 11 OF 12

03351

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 9535



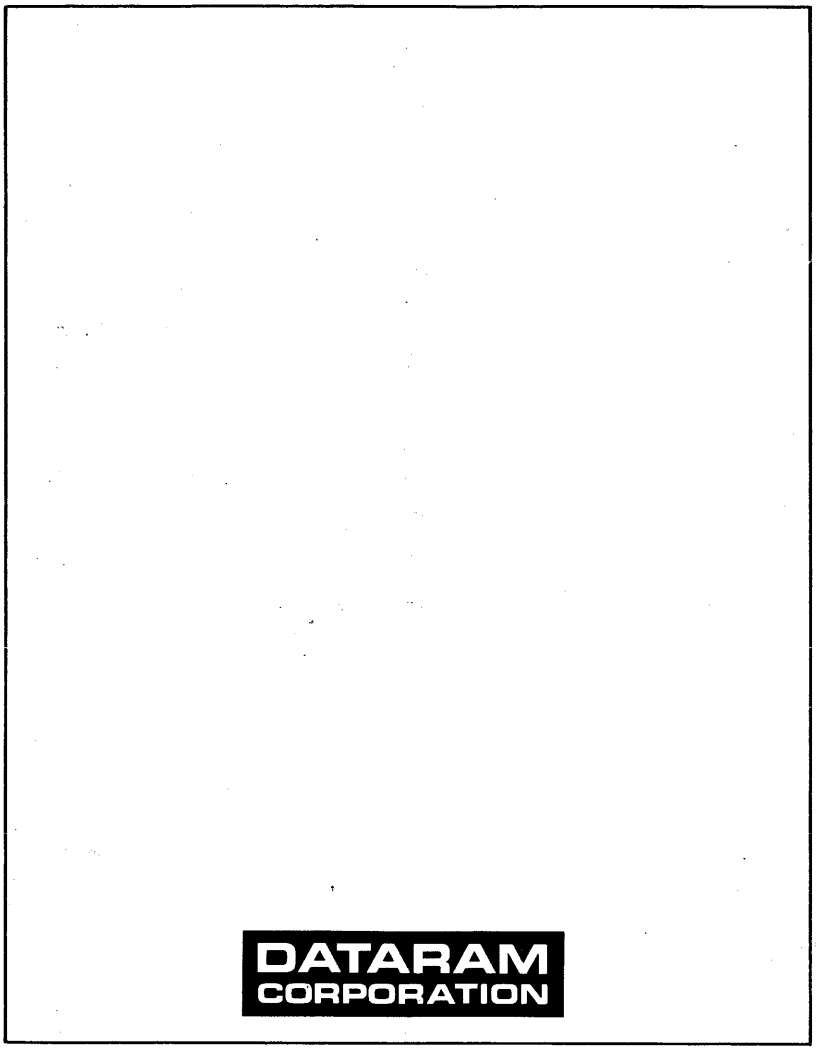
MICRO INTERUPT AND DISC SEQ. CKTS.

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03351	G

SCALE | SHEET 12 OF 12

03351

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-9559



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