

AUERBACH  
BUYERS'  
GUIDE  
TO...

**MINICOMPUTERS**

WINTER 1976-77

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## PREFACE

The **AUERBACH Buyers' Guide to Minicomputers** is a one volume, loose-leaf guide to minicomputers produced and/or marketed in the United States. It is intended to direct the prudent buyer, analyst, or producer of minicomputers through the large number of machines available on the market.

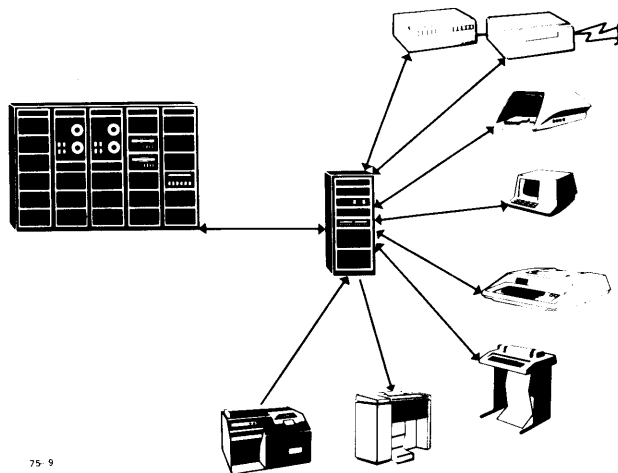
The volume contains information in chart, tutorial, and report format. In chart form look for complete specifications on microprocessors, and central processor and working storage specifications for over 85 minicomputers. In tutorial form there is a complete Introduction to Minicomputers that outlines their history, applications, technological design, and selection criteria. In report form, the major, currently marketed minicomputers are covered in depth. The product reports provide management-oriented overviews, competitive information, hardware and software specifications, reactions from, end-users, and configuration guidelines.

To help in the final selection or analysis of the minicomputer, the volume provides a full list of EDP suppliers and their addresses and phone numbers.



AUERBACH on . . . .

# MINICOMPUTERS



**Figure A. Digital Equipment TC/D (Terminal Control Enhancement): up to 80 devices can connect to four such secondary TC/D processors; the secondary connects to the host processor at left**

## OVERVIEW

The revolution is over. Long live the revolution. The impact of the minicomputer has indeed been revolutionary. As problem-solving tools, their impact has been dramatic. But the torrent has matured to a broad, sweeping river. Indeed, so varied are the options facing the designer today that the very term "minicomputer" is in danger of losing its meaning.

While the range of solutions now spans a complete spectrum — from smallest microprocessor to the grandest minicomputer facility, the fundamental truth remains. The minicomputer represents the fruitful, joyful conjunction of technician and user. The technician can achieve perceptible goals within perceptible time; the user acquires a viable mechanism at reasonable cost.

This paper describes the early days, the frenetic growth, coming finally to a review of present technology. It describes applications that are well suited to this technology, and, by example, the advantages and disadvantages of using a particular technology. Some notes and methodology are presented to help the potential user survive the hazards of selecting a vendor. In applying technology, the problem is to choose from gradations of performance and variations in types of technology delivery: service bureau vs system supplier vs computer vendor.

Finally, in the last section, the broad trends that have influenced small-machine development in the past are cataloged and extrapolated into the future.

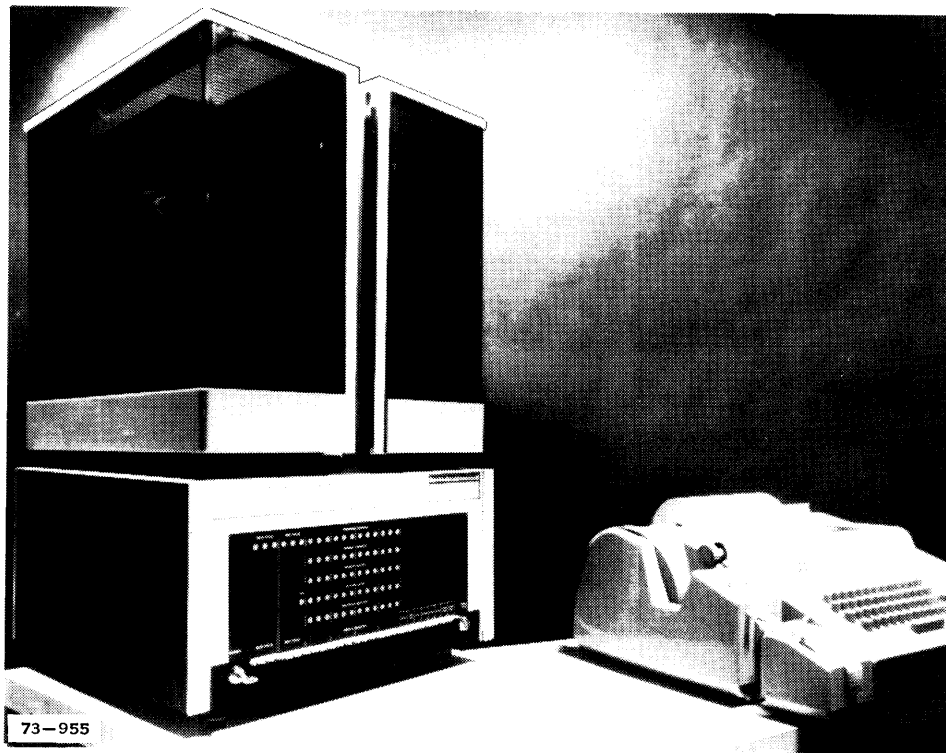
The word "minicomputer" became popular in 1968, to categorize a growing number of small, general-purpose computers. These machines were introduced initially to bring software solutions for the limited processing tasks of data acquisition and communications. These vintage machines, many from new vendors, generally conformed to the following descriptions:<sup>1</sup>

- Basic system configurations cost \$25,000 or less.
- 4,096- or 8,192-word core memory.
- Programmed in Assembly language (and less often in FORTRAN).
- Computer peripherals often restricted to Teletype and paper tape.
- Usually supported customer hardware (sensors, communications lines, and control lines).

The scope of this report, however, is more than just "those processors that cost less than \$25,000." Today, minicomputer is less a description of a black box than a philosophic approach to problem solving:

"Give me just the right amount of hardware and software to solve my problem."

The technology today is broad. It is bounded by the \$1,500 "system" based on the Intel computer-on-a-chip (or three chips), and a vast PDP 11/45 network from Digital worth a quarter million dollars including terminals, peripherals, and discs. With such scope it is clear why the application environment is boundless.



**Figure B. First Tabletop Digital PDP-8 Computer System**

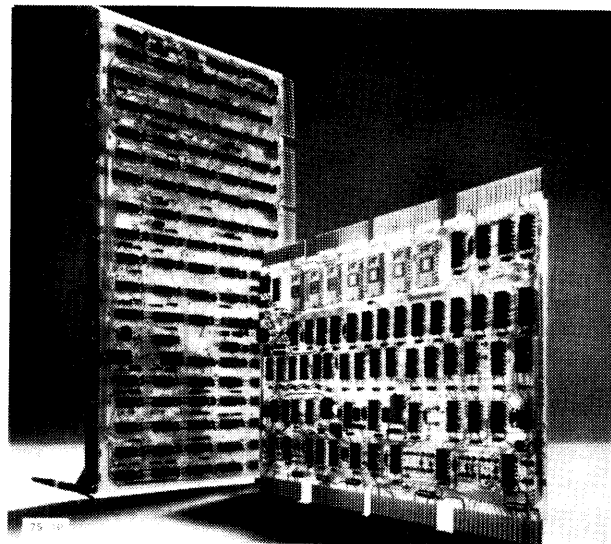
### HISTORY

The computer industry dates from about 1954. Only then did the number of machines extant warrant the name "industry." In the first decade the trade boomed. Initially, reliability was obtained only at great expense, but transistor logic solved the problem of costs. As business organizations became acquainted with computing, configuration sizes grew, and the process was still very expensive. Operating systems were invented to harness the larger number of hardware units, and languages were put in the field to speed problem solution. Both caused operation inefficiencies, so faster, larger machines were required. The computing resource became centralized and vital to the organization, so time had to be scheduled. Batch operations were the standard, and closed shops the rule. If a task could not be made to conform to this mold, only two alternatives were available: do the job manually or design special hardware to do it.

Upon this scene, in 1962, came Computer Control Corporation<sup>2</sup> and Digital Equipment Corporation with small machines for laboratory applications. Digital opted for a 12-bit word machine that balanced the high cost of memory (a function of word size) against popular transducer resolution (1 part in 1,000, sometimes with a sign). Digital has prospered from that time to now, but development of this avenue of computing has always been servant to hardware advances. The introduction of transistor logic in the early 60's made small computers pos-

sible, but the use of integrated circuits in 1968 opened the flood gates of small machine activity.

The hands-on scientist with ill-conditioned data, the small user with limited budget, the executive with untimely reports, all found a new alternative for centralized



**Figure C. The PDP-8/A, Digital's Smallest PDP-8: made up of two modules**



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**Figure D. Alpha/LSI and Naked Mini/LSI**

computing. New minicomputer manufacturers entered the lists monthly until 1970, when the number of vendors stabilized to between 40 and 50 and new product emphasis shifted to low-cost, modest-performance peripherals. Also during this period a large number of small systems houses sprang up. They took the very modular, low-cost components and welded them into systems with software. It took only a modest bankroll to become a minicomputer manufacturer and even less to become a hardware-software shop providing turnkey service.<sup>3</sup>

More recently, other developments have accelerated the production and use of small computers:

- Availability of economical peripherals.
- Large-Scale Integration (LSI) of logic functions.
- Dramatic decline in memory costs (1973-74).
- Accumulation of system software.
- Advances in packaging techniques.

The improved hardware and software have significantly increased speed and reliability. The net effect is a better product at a lower price. With each quantum step of improvement, "minis" have gained wider acceptance and a broader range of applications.



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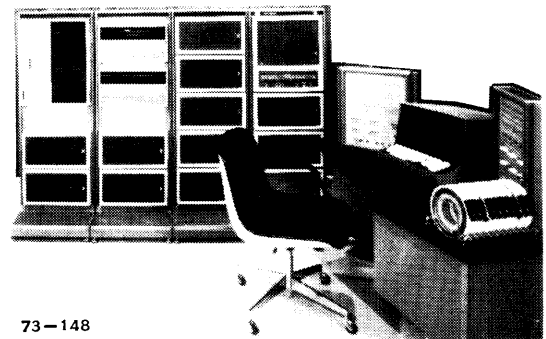
**Figure E. Reality Speaks ENGLISH**

The following table shows how two models of the Nova minicomputer from Data General Corporation compare with Univac 1<sup>4</sup>, the first electronic commercial processor.

Date	CPU	Add Time ( $\mu$ sec)	Memory (words x bits)	Cost
1952	Univac 1	4	1,000x48	\$750,000
1972	Nova 1200	1.2	4,096x16	\$5,200
1975	Nova 2/10	0.8	4,096x16	\$3,800

In the early 70's, the path of development was to extend the market upward by offering "bundled" operating systems and language processors. FORTRAN was available from practically all vendors. ALGOL and COBOL derivatives came later — but they came. Disc-based operating system software was so pervasive by 1974 that Computer Automation — ever an OEM supplier — provided one. Entering the last half of the decade, vendors were supplying machines that spoke ENGLISH<sup>5</sup> and employed some of the optimizing features of the very large systems:

- From IBM 360/85, circa 1968, comes the "cache" memory now on the Data General ECLIPSE.
- From the B5000, circa 1962, comes the "stack" architecture of the HP3000.
- From the IBM-360, circa 1963, comes the "dynamic control store" of the Varian V70 Series and Hewlett Packard 2100MX.



73-148

**Figure F. Hewlett-Packard HP 3000**

At the other end of the scale, LSI allows a computer (with reasonable performance) to be built on very few chips for \$500 and yet have a mean time between failures (MTBF) approaching 50,000 hours. Thus, today's minicomputer range is so broad that equipped with a variety of peripherals, it can be fitted for applications with budgets ranging from \$10,000 to several millions of dollars. The unifying notions are no longer size or price. The term "minicomputer" now denotes modular construction and task-oriented system design.

## MINICOMPUTER TECHNOLOGY

The "mini" in minicomputer acknowledges that these units have generally been associated with limited size.

# AUERBACH ON MINICOMPUTERS

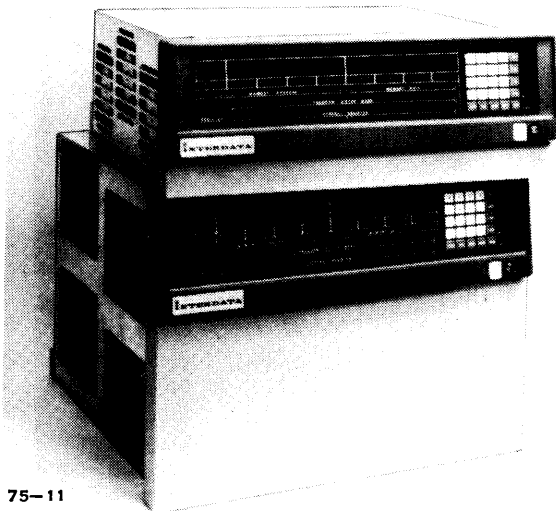
limited price, limited performance, and limited support from the manufacturer. Manufacturers are removing the "limitations" previously associated with minicomputers as fast as they can; superior performance and software are now available — at a price. Discussion will be anchored on middle-line minis, while the extremes of microcomputers and mini-facility configurations are spotlighted.

## Design Philosophy

Minicomputers are designed as general-purpose computers with a mix of logical, arithmetic, and input/output (I/O) functions. These features are complemented with packaging that permits easy build-up from small configurations. Processor options, memory, and peripherals can, in general, be added by plugging-in circuit boards to prewired spare connectors in the computer chassis.

Minicomputer chassis are usually made of light sheet metal, which is satisfactory for practically all commercial installations. If the computer will be moved frequently, a specially ruggedized model might be selected. Recent packaging trends have been toward large circuit boards, which reduce the number of mechanical connections and make the units more reliable. For example, the entire Nova computer is contained on a single 15-inch-square circuit board; the Interdata 7/32 on two 15-inch boards.

Manufacturing economies are often effected by using power supplies of questionable merit. More than one manufacturer has had greater difficulty with the system's power supply design than with the processor.



75-11

**Figure G. Interdata Models 7/16 and 7/32**

The computer design can be shaded towards a broad applications market. A manufacturer can include many features as standard if the intended market requires those options. Machines intended for word-processing or accounting applications generally use shorter word lengths with multiple word instructions, and they implement hardware decimal arithmetic. Machines intended for sci-

entific calculation or process control applications generally use long word lengths and frequently hardware for floating-point arithmetic.

Table 1 summarizes the general characteristics of minicomputers. The "average" column presents a picture of the middle-of-the-line mini. Minimum and maximum columns indicate the range from very small, single task computers to very large, facility-oriented machines. A

**Table 1. Minicomputer Characteristics**

Characteristics	Minicomputer Size		
	Minimum	Average	Maximum
<b>Memory</b>			
Word length (bits)	8	16	32
Type	Core or semiconductor	Core	Mixed
Size (bits)	256-4,096	To 65,536	To 262,000
Increment size (words)	256	8,192, 16,384	16,384, 32,768
Cycle time ( $\mu$ sec)	8	0.75-1.75	0.64 to .3
Parity check	No	Opt	Std
Memory protect	No	Opt	Std
Direct addressing (words)	$\pm 128$	512-4,096	All of memory
Indirect addressing	No	Yes	Multilevel
Sub-word addressing	No	Byte, half-word	Byte, bit
<b>Central Processor</b>			
General-purpose registers	1, 2	2-4	To 64
Index registers	0	1-4	15
Hardware multiply/divide	Opt	Std	Std
Floating-point hardware	No	Opt	Std
Double-word instructions	No	Opt	Std
<b>Input/Output</b>			
Programmed I/O channel	Yes	Yes	Yes
I/O word size (bits)	8	8/16	8/16
Priority interrupt lines	1	1 std, up to 64	4 std, up to 256
Direct memory access	Opt	Std	Std
I/O maximum transfer rate, DMA (words/sec)	125,000	To/Million	To $5.0 \times 10^6$
<b>Other Features</b>			
Real-time clock	Opt	Yes	Yes
Power fail/restart	Opt	Yes	Yes
Largest disc (megawords)	4.8	9	85
Assembler	Yes (not macro)	Yes	Yes (macro)
Compiler	BASIC, FORTRAN	BASIC, FORTRAN, COBOL subset	BASIC, FORTRAN, COBOL, ALGOL
Operating system	Yes: cassette or core-based cassette	Yes: disc, tape, or core-based	Real-time, foreground/background, time sharing
Percentage of Units Installed	38	60	2
Purchase Price*	\$1,000	\$8,000	\$22,000
Est. Annual Growth	+100%	+30%	+200%

\*Purchase price is for the average computer in its class without peripherals.



"maximum" mini would be supported with many peripherals, an operating system, and, probably, a large staff.

## Central Processor Unit (CPU)

The central processors are usually single-address, binary units with negative numbers expressed in two's complement form. Central processors vary most in the number of accessible registers, instruction sets implemented, instruction decoding technique, interrupt handling capability, and I/O facilities.

Arithmetic and logical operations are performed on data brought to the CPU from memory. The data is held and transferred between registers during these operations. A register is merely an assemblage of electronic components (flip-flops) that contain the data word while it is being processed. Some registers are accumulators (of data).

The elements of the computer are connected by buses over which data and instructions move. Generally two buses are used: one for transfers between memory and CPU and another for transfers between the CPU and its peripherals (the outside world).

Most processors use one-word instructions with the following format: 4 to 6 bits for operation code, 2 to 4 bits for modification field, and 8 or 9 bits for the address field. Most of the operation codes are used for memory referencing instructions. Non-memory referencing instructions use additional bits of the instruction word to define the operation code; thus, the number of instructions can be quite large. Most have an instruction set of 64 to 100 instructions; some have many more, over 200. The modification field further defines the instruction, usually specifying an addressing mode (indexing, indirect addressing, or both) and a literal (immediate) address; or specifying a two-word instruction. The address field provides an address increment or a literal. The effective address is calculated in accordance with the address mode; usually the contents of the program counter specify the base address and the address field specifies an increment or the core address within a page. Some minis have page registers that can be loaded with the page number of the core area from which operands are being extracted. Two-word instructions allow direct addressing of large memories — a common method of extending the addressing capability for large minis. The Interdata 7/32, for example, can address 1 million bytes of memory.

The basic instruction set usually includes the arithmetic operations of fixed-point add and subtract; multiply and divide are implemented by subroutine but usually are available with optional hardware.

Double-precision operations are sometimes provided. Most larger minis offer floating-point hardware as an option, but this feature is usually expensive. All offer some form of logical, compare, and shift operations. Many also offer byte and bit manipulation instructions. The I/O instruction is usually very general. It transfers control, status, and data words between the peripheral devices and the processor's accumulator. Commonly, the

I/O instruction also provides control of optional features. They are addressed as external devices.

Classical CPU design includes a program counter, an accumulator, an accumulator extension register, and one or more index registers. Newer designs provide a number of general registers that can be used as accumulators or index registers. Sometimes a condition register keeps track of processor status with respect to overflow, operation mode, or the result of a comparison.

Some newer systems, such as the Digital PDP-11, feature two-address instructions that specify source and destination addresses calculated using the contents of general registers. This architecture lends itself to real-time processing and multiprogramming because the general registers can operate as stack pointers for stack manipulation and context switching.

Unfortunately, many manufacturers are stuck with old processor designs because of the large investment in software. Microcoding, however, has allowed some freedom; the processor can utilize modern design but emulate older systems in microcode for software compatibility. This need for compatibility places many restrictions on system design, but it does protect the users' investment in software.

## Memory

Memory technology has advanced rapidly. In the early seventies, many people predicted that ferrite cores as CPU local memory would be replaced with solid-state memory. The decline in the cost of core, however, has kept core the standard for minicomputer memory. Semiconductor memory is faster, but it forgets when power is removed. A third type is Read Only Memory (ROM). As its name implies, it can only be read, not written. This restriction has two attributes: it is nominally twice as fast as a read/write memory having the same clock rate, and it is secure from inadvertent modification. Therefore, fixed, unchanging data or code can be located in ROM. Often all three types are offered by a manufacturer and can be mixed on a system.

Computer memory can be functionally divided into program storage and data storage. The CPU accesses a program instruction and then, based upon the instruction, recovers or replaces data. Besides communicating with the CPU, memory usually can communicate with I/O devices via direct-memory access (DMA) facilities. Thus, both the CPU and I/O devices share the memory bus.

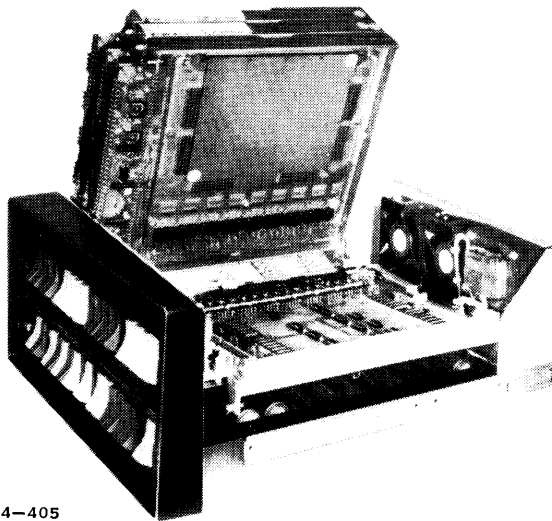
Memory size can range from a few words for a small, fixed process to hundreds of thousands of words for a time-constrained major activity.<sup>6</sup> The addressing techniques used by the instruction set are often supplemented by special memory "mapping" hardware for very large memories. The mapping hardware provides selection of a particular block of physical memory. Memory is usually subdivided into modules of 4K, 8K, or 16K words; some vendors, such as Modular Computer and PRIME Computer, have 32K-word boards. More elegant memories have multiple ports of entry so that a module can be

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shared by two or more CPUs, or by a CPU and a DMA device. Multiple ports can double or triple throughput if data in one memory module can be processed while data is transferred between other memory modules and peripheral devices.

Memory word size can be extended to include provision for error recognition and correction. Simple detection is afforded by adding a parity bit. If several more bits are added to each word, special hardware can not only recognize errors but also correct them.

Memory protection can be accomplished word-by-word by adding a protect bit to each word. Area protection, using separate logic that establishes upper and lower bounds for protected memory, is much more common.



74-405

**Figure H. MODCOMP II/12 with Two 32K-Word Memory Boards**

Core memory construction is very much a manual process; fine wires must be strung through the ferrite doughnuts. Consequently, memories are made in places where labor costs are low — generally outside the United States. This construction method also makes it very expensive to thread tiny ferrite cores, and faster memory speeds are obtained by making the cores smaller. Thus, there is a natural price break for core memory with a cycle time of about 1 microsecond.

### Instruction Set

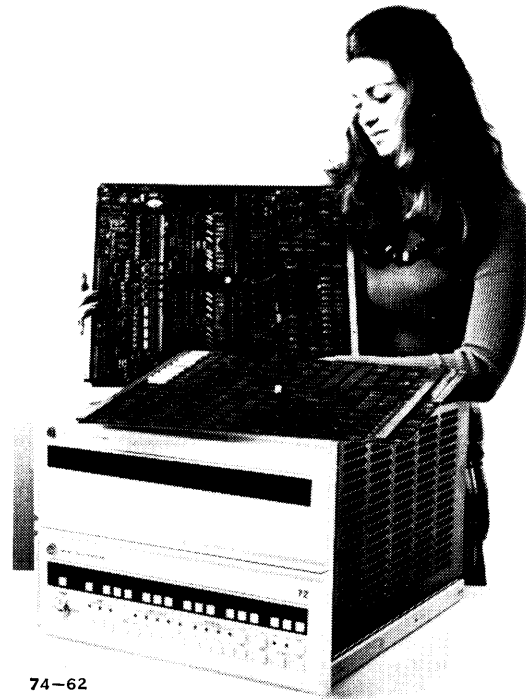
The computer's instruction set defines the most primitive functions that are available to the programmer. When these operations are given mnemonic names (such as ADD for addition operator, BEQ for branch if registers equal) and combined with the rules for instruction use, the result is the machine's Assembly language.

A minicomputer's vocabulary usually consists of from 70 to 200 different operations, including memory reference, logical register manipulations, comparisons, and transfer instructions. The computer word has fields committed to define an operator, a memory address, and

modifications to operator or address fields. Modifications to instructions may specify variations on a basic operator; modification of addresses defines indirect or indexing functions.

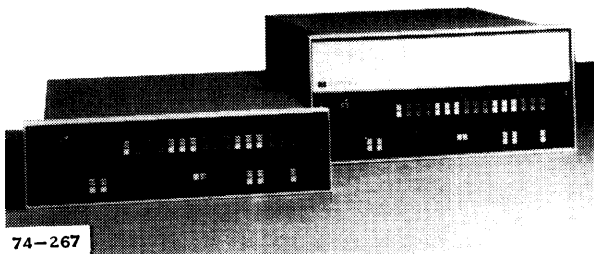
The computer's instruction set is usually determined by fixed wiring of electronic components within the machine. Most recent designs however, employ a concept first advanced by M. V. Wilkes in 1951.<sup>7</sup> Wilkes proposed that a program, that is, a sequentially executed procedure, could be brought inside the CPU and used to define the instruction set of the machine. An ADD instruction, a single operation as seen by the programmer, would actually be effected inside the CPU by a subroutine of microinstructions. Each microstep would deal with intrinsic computer operations that are more primitive than the Assembly language.

This approach, called firmware or microcode, provides a means of making changes in a computer's instruction set without scrapping the hardware design. This facility is of limited value to the user except for special circumstances, such as emulation or specialized, time critical instructions. It does permit the manufacturer, however, to extend or purify the computer's design with minimum pain. Firmware is of negative value if this approach reduces computer throughput. Within the past few years, the increased speed of logic circuits has made the technique practical. Early Interdata machines, for example the Model 3, used firmware but were slower than comparable hard-wired machines. ROM was used for its speed and security. Today, a number of manufacturers — Varian, Hewlett Packard, Prime — have



74-62

**Figure I. Varian Data Machines V-72, Second in V70 Series**



**Figure J. Hewlett-Packard 21MX Computers**

relaxed the read-only constraint and provide writable control store (WCS) for their systems. The speed of solid-state memory makes WCS practical. Now, for some systems, the instruction set can be modified or extended dynamically while the machine is operating.

## Input/Output

Two basic means of I/O are available: programmed and automatic. The processor's data channel (or bus) is generally one word wide (16 bits for a 16-bit word processor). The channel transfers control and status information as well as data. For programmed I/O, all information is passed as a result of executing programmed instructions. For automatic I/O, control information is passed to a device controller specifying the mode of operation, the memory area involved in the transfer, and the amount of data to be passed. Once the transfer operation begins, it proceeds to completion using the DMA facility without further intervention by the program. Often, the completion of a block transfer causes an interrupt from the device controller to signal that the device is available for another transfer.

Fast devices such as tapes, discs, and drums require automatic block I/O. Slower devices can operate under either regime. Since hardware controllers for doing block I/O are relatively expensive, control information governing automatic block transfers can reside in special memory locations associated with one or more data channels, or it can reside in the device controllers.

Most minicomputer vendors provide controllers for industry standard I/O devices: high-speed paper tape units, punched card readers and punches, line printers, magnetic tape transports, plotters, displays, and Teletype units. Almost all manufacturers provide mass storage devices such as disc, drum, or tape for their products. Magnetic tape cassettes and floppy discs are among the latest offerings from the vendors. In addition, a number of independent firms offer peripherals with controllers and controller software for the popular minicomputers.<sup>8</sup>

## Interrupt Function

The interrupt facility allows the computer to recognize the occurrence of an asynchronous external event. Then, the CPU pauses in its processing to service that event. Software analysis of the interrupt is required on the simpler minis to identify what to do. More sophisticated schemes provide a transfer vector and interrupt priorities or levels.

Interrupts include both external — outside world events — and internal — machine-generated events. Internal interrupts, sometimes called traps, include power failure sensing, illegal instructions, memory parity, memory protect, and real-time clock events.

When an interrupt is recognized, processor control is transferred to an interrupt processing routine. At this point, it is usually necessary to save the current status of all registers that will be used by the interrupt processor so they can be restored when the interrupt routine is finished. This status-saving/restoring is done automatically on a number of computers.

External interrupts are under program control and can usually be individually disabled or inhibited. A disabled interrupt level ignores an interrupt signal. An inhibited interrupt level stores the signal but does not cause an interrupt until the inhibition has been removed.

A hardware provision blocks out all interrupts until the interrupt servicing subroutine has stored the status of the processor: the contents of the accumulators, index registers, program counter, and overflow. In addition, hardware also blocks out all interrupt levels of an equal or lower priority than the one currently being serviced.

When each interrupt condition is connected to a unique interrupt level, the source is identified immediately. When several interrupt conditions are connected to a single interrupt level, additional processing is required. Some systems have a hardware provision for reading the address of the highest-priority device with a single I/O instruction. Others require a separate I/O instruction to test each device status flag. Most minis provide multiple interrupt levels; thus devices that require a fast response time can connect to unique interrupt levels, while several devices that can tolerate a longer response time are multiplexed into a lower-priority interrupt level. Some interrupt systems automatically inhibit the interrupt system from the time an interrupt is granted until the system is released by instruction. Others have hold-and-release interrupt instructions.

The efficiency of an interrupt system is determined by the time required for the overhead functions: to identify the interrupt source, to inhibit further interrupts until preliminary servicing is finished, and to initiate the interrupt service routine. These operations can be performed by hardware, software, or a combination of the two.

## Software

All manufacturers supply "system software" to assist the user in developing applications programs. The minimum level of support includes a text editor, assembler, loader, and utility subroutine package. Most vendors also supply FORTRAN and BASIC language processors together with an operating system that permits their use. Such systems generally require at least 16,000 words of local memory and some form of high-speed data entry (disc, magnetic tape, or fast paper tape).

More elaborate operating systems supporting time-sharing and real-time operations are available from most

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vendors. ALGOL, COBOL, and subsets of these languages are also available for some systems. At this level, diagnostics, debugging aids, and useful subroutine libraries are common.

### Training

The major vendors conduct maintenance and programming courses for their customers. Typically an arrangement is made with the salesman when a customer wants to attend these sessions. Detailed reference material defining hardware and software products is generally available free from all manufacturers.

Successful minicomputer user groups that share software and product expertise are a rarity. [DECUS (Digital Equipment User's Society) is a notable exception.] Because machines are often dedicated to a single task, there has been no great pressure from users to maintain communication with each other. The impetus for such activity has been an off-again, on-again interest of the manufacturers. The trend to facility-oriented, big minis may change this situation.

### APPLICATIONS

Appropriate applications for minicomputers are as numerous as leaves on a tree. The key attributes of a task to make it a candidate for solution with today's small computer technology are as follows:

- It requires computation or logical testing.
- Process is repetitive — frequently or cyclically performed.
- Manual method is either too slow or too inaccurate.
- Requirements change with time.
- Expenditure must be modest.
- Process must operate unattended.

Application areas for which minicomputers are used are so broad that whole fields of specialization develop within them. Process control applications, for example, can range from the control of a small, simple laboratory experiment to the control of a large oil refinery or chemical plant. Automating the laboratory process affects little outside the laboratory involved. Automating an oil refinery or chemical plant, however, has ramifications far beyond the computer site and can affect hundreds of people and pieces of equipment. In fact, the personnel problems in setting up a large process control center are so great that most books on the subject devote large portions of the text to ways of handling them.

Small computer applications can be divided into five broad categories, as shown in Table 2. For each application, special equipment and software have been developed and applied, depending on the size of the task in hand. Each satisfies one or more of the attributes identified previously. For further reference, the bibliography has been organized to reflect the breakdown shown in Table 2. Regardless of the nature of the task, the preeminent requirements for successful computer application

**Table 2. Applications of Minicomputers**

#### Computation

Accounting Functions  
Sales Analysis  
Order Entry  
Inventory  
Production Scheduling  
Bill of Materials  
Engineering, Scientific Computation  
Time Sharing

#### Word Processing

Key to Disc, Tape  
Text Editing  
Typesetting, Photo Composition  
Computer-Aided Design  
Computer-Aided Instruction

#### Communications

Remote Batch Terminal  
Line Concentrator  
Front-End Processor  
Message Switching

#### Data Acquisition

Telemetry Decommutation  
Data Reduction  
Data Conversion  
Laboratory Experiment Control  
Medical Test Analysis

#### Process Control

Automatic Testing  
Numerical Tool Control  
Traffic Management

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are that management understand the task and make a solid commitment to the computer-based solution.

Because of their low cost, minicomputers tend to be located close to the hands of the user. Thus, minicomputer systems design must be very attentive to the human engineering of hardware and software.

Rather than look at the uses of a minicomputer from the point of view of a specific application, or vertical industry, one can look at the different ways the computer is used regardless of application. Viewed thus, minicomputers are used in the following ways:

- As stand-alone computer systems.
- As dedicated computers performing the same operation day after day.
- As modules in a hierarchical system.

As a stand-alone processing system, the computer performs a variety of functions depending on its programs. The stand-alone system can be a simple one, with small memory and a single typewriter station with slow paper tape for I/O. Software can include an assembler; a loader; I/O handlers; editing, debugging, and diagnostic routines; and some math subroutines.

On the other hand, the stand-alone system can be large and comprehensive. It could include a large internal

memory, a disc for external storage, and multiple I/O devices, such as key-entry stations, paper tape, magnetic tape, and printers. Software can include a disc operating system with control for several real-time processes in the foreground, and priority-selected batch processing facilities for programs written in an Assembler language, FORTRAN, or ALGOL in the background.

Dedicated processors can be used as an extension of the operator, who can do the job better, as in product or environmental testing, process monitoring, and data acquisition.<sup>9</sup> The computer interfaces directly to control or monitoring equipment and is programmed for interaction with the operator. Parameters for the function performed can be provided by the operator or by sensors. The computer acquires data, analyzes it in relationship to the parameters, and communicates the results to the operator or to equipment that it controls. In addition, the computer can prepare and maintain statistical records on data received.

A minicomputer can also function as one module in a large computer system, preprocessing data for the larger computer, handling communications among many terminals, or performing most functions on its own and calling on the large computer only when problems are too large or too complex for it to handle. These systems can be very efficient with each component performing those functions for which it is best suited.

There is a trend to decentralized systems that operate both as stand-alone computer centers and as terminals to a central facility. In this situation, a minicomputer (or smaller microprocessor) may be located at the remote sites while a larger minicomputer or maxi time-sharing system operates as the parent at the central site. This configuration is attractive to organizations with many remote offices. Large central files need to be maintained, and they are updated from the field offices periodically. Computation needs of both central and remote offices are performed by the on-site processors.

## ADVANTAGES AND DISADVANTAGES OF MINICOMPUTERS

The greatest advantage of the minicomputer, in comparison to large computer systems, is that a user can buy the specific amount of computer power required for a job. The minicomputer is general-purpose and can be used to perform any function, within its size limitation, for which a program has been written. Because the overall cost is low, the minicomputer tends to be located at the problem site rather than in a computer center, and users can interact with it directly. It can be dedicated to a single problem or related set of problems. It can be fine-tuned to solve a problem as the problem should be solved. A general solution need not be adopted; a task-efficient approach is acceptable.

Generally, minicomputers are compact and rugged and do not require specialized environments. In addition,

most minicomputers are as fast as, in some cases even faster than, their larger counterparts and can provide instantaneous response to an external request for service. Because a minicomputer is used by a smaller group of people, the effect of a computer malfunction is not as catastrophic as it is in a larger system. Indeed, hardware redundancy can be structured at moderate cost.

The greatest disadvantage of minicomputers to date has been the difficulty of programming because of the limited amount of software supplied with a system. This difficulty is gradually being overcome, especially for older designs. Vendors are commonly supplying operating systems that allow program development concurrent with on-line tasks.<sup>8</sup> Various manufacturers now supply ALGOL, FORTRAN, BASIC, and COBOL-subset language processors.

The other major disadvantage is the availability of field engineering and spare parts. This problem is endemic and not necessarily confined to new or small manufacturers. As the industry matures, more systems are being based on vendor-supplied operating systems and languages, and system software support is an important factor.

The very reliability occasioned by the move to large boards and wire-free packaging has created a spares problem. When the PDP-8 had 60 circuit boards of nine types, a spares kit could be obtained for a reasonable price. However, a spare for the Nova CPU is another complete CPU.

Other disadvantages relate to manufacturers' attempts to reduce costs. These items tend to be irritating rather than serious: switch toggles that break, lamp sockets poorly made, or inaccessible fuses and lamps. These problems tend to vary from manufacturer to manufacturer.

## SELECTING A MINICOMPUTER

There is no best computer on the market, no computer has the lowest overall price/performance ratio, and no one can guarantee which computer is the best for a particular user application. On the other hand, many good computers are available, many computers have good price/performance ratios, and several computers can probably do a particular job well. The problem is to identify those computers.

Unfortunately, selecting a computer for a specific job is not easy. Still, if done without panic and without rush, the rewards of the search can include raising the staff's technical competence, understanding the individual application better, and building a firm foundation for the decision-making that will accompany future developments within the application.

The wise selection of a computer depends on the selector(s) fully understanding the application. A number

of people can be involved, but cooperation among the ultimate users is essential. The group of end users must develop a set of criteria for selecting a suitable computer; and these criteria must reflect the needs of each user's application area. Expressing these criteria in computer terms is a non-trivial task that must be accomplished, and should involve someone with a computer background. Because it is human nature for each to consider his personal needs most important, some member of the selecting group must have responsibility for leading the group toward satisfactory compromises. Such compromises might be expressed as weights applied to the selection criteria.

Developing the weighted selection criteria is an educational process and is the hardest part of the selection procedure. Application areas must be viewed in terms of what is now done, what can be done better by computers, and what can be expected in the future. Each person in the group must appreciate what computers can do from the functional point of view; each must discern that computers vary in architecture and capability; and each must understand that, whatever the hardware capability, the viability of the system is dependent on successful software.

The goal in any selection procedure is to choose a vendor or vendors that present the best combination of technical solution and system cost. Depending on the size of the project, the procedure for selection will be quite detailed or accomplished in an afternoon (with the back of an envelope for notes).

This procedure can be adjusted as necessary to suit large or small projects. The following algorithm is appropriate for selection:

- Establish minimum performance and maximum cost standards.
- Determine performance criteria, note thresholds or minimum performance levels, for example band width and speed.
- Relate performance criteria to computer and peripheral characteristics.
- Determine vendor characteristics that are important to the project.
- Assign numerical values to the quantifiable hardware and vendor characteristics.
- Rank the various characteristics and weight them, if necessary.
- Determine total cost of proposed solution — cost of vendor proposal plus cost of internal engineering, management, and programming for the proposed solution.
- Map the performance and price data developed.
- Make a subjective decision based on the clear understanding of cost and performance trade-offs provided by the objective data.

Objectivity can be maintained by setting up important criteria in advance of evaluation. Ranking or weight assignment is done before seeking vendor proposals. Ob-

jectivity is guaranteed by using measurable, quantifiable characteristics.

Cost-effectiveness requires considering all elements of a project that contribute to its cost. These factors include training, supplies, and spare parts. Note that even the FORTRAN programmer must relearn the language and the new compiler control mechanisms when moving to new hardware. An inexpensive printer that uses expensive, treated paper may not be a bargain over the system's lifetime.

The final decision is based on solid information. Subjective considerations are restricted to evaluating the importance of adequate cost and performance margins, based on maximum cost and minimum performance initially established. Observe that selection cannot be based on the notion of an absolute performance/cost evaluation. Many criteria, such as personnel experience, are situation- and time-dependent.

The difficult step in this algorithm is the conversion from task specification to computer characteristics. The selection criteria must be expressed in computer terms, and the weight applied to each criterion reflects the importance of that parameter to the particular application.

The following elements of computer systems usually form the basis for selection criteria:

- Central processor.
- Memory.
- I/O structure and channels.
- Interrupt system.
- Standard peripheral devices.
- Software.
- Manufacturer.

### Central Processor and Memory

The central processor and memory determine to a large extent the computing power of a computer system. Important memory characteristics are word length, cycle time, and size. Ideally, the word length should correspond to the data precision required by the application. The cycle time determines the speed of the computer, but the user must beware of considering cycle time alone. How efficient is the instruction set for the specific application? For example, fast instruction execution may not offset a communications interface that requires several instructions for each I/O operation.

The memory size determines the complexity and size of programs the computer can run and the type of software that can be supported. Additional memory features that are often important are memory parity and memory protection.

Important central processor characteristics are the instruction set, addressing capability, speed of instruction execution, number and kind of program accessible registers, number of internal interrupts, and optional features.

If the instruction set does not include a required function such as floating-point arithmetic, software routines must perform the operation. These routines occupy memory storage space. Execution time is longer than for a comparable hardware operation. Some minicomputers have control stores (either writable or read-only) that can implement new, specialized instructions. Additional, pluggable hardware can be added to perform the required function. Floating point and fast Fourier transform processors are examples.

Memory organization can have a profound effect on the way in which software is developed. For example, the most successful mini, the PDP-8, has memory allocated in 256-word pages. An instruction can directly reference only those addresses within its page (or a base page). When working in a higher level language, the programmer is masked from such considerations, but inefficient execution times may result if program size passes certain thresholds.

The speed of instruction execution is usually a function of memory cycle time. Each instruction must be fetched from memory, and many instructions require another memory operation for data.

The number, size, and arrangement of index registers and accumulators affect the time required to do a job and the memory space required by the program. Index registers save memory references to software index registers set up in memory and thus cut down on the number of indirect references made. They can make the programmer's job easier for loop control and linking to subroutines. The number of accumulators also determines the precision of arithmetic operations, the ease with which precision can be increased, and, generally, the efficiency of the processor.

The number of internal interrupts and number of optional features offered are factors in determining the flexibility of the processor for a particular application. The selection criteria should specify all optional features required.

## **I/O Structure**

Small computers are often tied to sensor- or operator-based systems, and the I/O structure is a major factor in evaluation. The most common I/O facility for minicomputers is a programmed party-line channel to which peripheral device controllers interface for transferring data, status information, and commands. The number of devices the channel can support and the maximum allowable length of the bus vary from CPU to CPU. Channel performance is determined by the number and kind of I/O instructions and the facilities for determining which device requires service.

I/O transfer rates are affected by the memory addressing techniques, the instructions provided for controlling and testing counters, and other factors such as the ele-

gance of the I/O instructions. Most minicomputers have a generalized I/O instruction that is used to transfer data control words or status words between the accumulator and a peripheral device controller. The instruction set should be examined to determine how easily the processor identifies a device requiring service.

Most minicomputer systems include a direct memory access (DMA) channel to allow high-speed data transfers between peripheral devices and memory, with the data transfers under control of the channel.

Processor time devoted to I/O operations is a function of the number of peripheral devices in the system, their frequency of use, and the execution time of the software I/O routines. Requirements for the application must be carefully analyzed and the criteria defined to eliminate from consideration all computer systems that do not have minimum performance. Vendor proposals should note the number and kind of I/O channels supplied and the costs for extending these.

## **Interrupt System**

The function of an interrupt system is to signal the processor that an untimed (untimely) event has occurred. A priority interrupt system establishes a hierarchy of importance for the attention-getting signals.

A simple interrupt configuration includes one line to which all devices interface. Software analysis is required to determine which device has caused the interrupt and what action to take. The Nova and PDP-8 machines use this scheme. The order in which interrupt servicing routines test the status of devices that can cause the interrupt establishes the priority of the devices.

A true priority interrupt system provides a number of interrupt lines, with a memory location dedicated to each line to select the interrupt servicing routine appropriate to the interrupt signal. This setup significantly decreases the response time of the processor to interrupt signals.

The priority of interrupt lines can be hardwired and fixed, or controlled by bits set in one or more programmable interrupt control registers. Programmable registers make the interrupt system more flexible — important if the various peripheral devices assume different priorities from program to program.

Normally, the instruction set includes a provision for blocking out all interrupts so that crucial processing can proceed, such as a routine to load or store the interrupt control registers. In addition, the interrupt system can block out all interrupts except those of a higher priority until an interrupt servicing routine is finished. The instruction set also includes some means of restoring the interrupt system to its state prior to the beginning of the interrupt servicing routine.

When a program is interrupted, the volatile CPU registers must be saved. This overhead may be handled in hardware or software. The method should be noted in the evaluation.

### Standard Peripheral Devices

Vendor-offered peripheral devices and their delivery times may eliminate many minicomputers from consideration by the selection group. Most minicomputer manufacturers do not make all of their own peripheral devices. Instead, they buy standard devices and provide the controllers for a particular computer. Generally, the cost for peripheral devices is relatively higher than that for a processor. Recently, many new products have entered the marketplace. Costs have been dropping for two principal reasons:

- Performance standards have been moderated.
- Large minicomputer sales have permitted volume sales of peripherals.

The alphanumeric CRT/display with keyboard is a good example of how prices have been reduced.

Year	Performance	Price (interfaced)	Vendor
1967	250,000 cps	\$40,000	CDC
1972	1,000 cps	3,000	Hazeltine
1975	100 cps	1,800	Digilog

The dilemma faced by the minicomputer manufacturer is which of the many new products to offer with the computer. The dilemma faced by the buyer is how many different vendors to use.

Today, the CPU manufacturer generally offers a wide variety of peripherals, but not necessarily the latest or best. The manufacturer also tends to develop and produce some peripherals, such as Hewlett Packard cartridge discs, Digital DECtapes, Data General cassettes and fixed-head discs.

Meanwhile, the popular computers are supported by many independent vendors who can supply plug-compatible devices. Often, as with a disc, significant software comes from the vendor. These peripheral vendors often are credible though some are not. In the area of peripheral evaluation, much greater emphasis should be on the device's performance in a benchmark situation since only a few devices fit the particular needs of a given project.

### Interfaces Available

A majority of minicomputer manufacturers provide interfaces to standard data communications devices, to analog/digital and digital/analog devices, and to sense and signal modules. Some manufacturers specialize in these applications and have extensive hardware options as well as the software to support the equipment.

If the application requires interfaces to special-purpose devices, the selection criteria should include interface requirements. The cost of designing special-purpose interfaces can become a significant fraction of the total project cost.

### Software

One of the most important components of a new computer is its software. It is critical to performance and is the most frequently underestimated, misunderstood item in the system budget. Because the cost of minicomputers is small, many minicomputers do not have extensive system software. The selection criteria should include the required software, with weights applied to the desired features for future as well as current needs. In fact, the system software supplied by the vendor controls the ease and speed of applications program development.

If the manufacturer writes off software production costs in the hardware price, the system cost increases as more system software is included. On the other hand, if the user needs system software not produced by the manufacturer of the system he buys, the cost for its development must be added to the price of his computer. This cost will be much higher than if the manufacturer distributed the software charge over many computers. In other words, well-conceived system software that is needed for an individual application is much cheaper for the user to buy from the manufacturer than to develop, and the selection criteria should reflect this view.

The user must determine the software selection criteria. Because software needs are tied to an application area as closely as hardware needs, criteria can vary from application to application. Despite the previous disclaimers, certain general software characteristics should be included in the software criteria.

Generally, the cost per line of software developed is inversely proportional to the investment in hardware. In other words, the less expensive the hardware, the more expensive it is to program. It is uneconomical, for example, for the programmer to do clerical chores such as loading a succession of paper tapes or stepping through a compiler process. If the system does not support program development, then an alternative must be identified and its cost.

System software universally includes an editor and an assembler. A variety of conventional and special-purpose compilers are available — not all from the same vendor.

Manufacturers emphasize the following features of their assemblers and compilers:

- Number of passes of the source code.
- Memory required.
- Quality of syntax checking.
- Pseudo-operation codes.
- Absolute or relocatable output code.
- User-defined macros in the Assembly language.
- Library calls and in-line Assembly code provided.



The selection committee must consider the ease and speed with which applications programs can be coded, debugged, and run on the system. An initial decision is what language should serve as a basis for development. The fundamental considerations are as follows:

- Compiler languages are superior because programs can be developed faster, documentation is better, and larger pools of trained programmers are available.
- Assembler languages produce more efficient code.
- Some languages will not be available on otherwise superior equipment.
- Compilers require operating systems for support. Larger, more elegant languages often are not acceptable in the user environment until many months after their first release (caveat emptor).

Most assemblers require a minimum of two passes of the source code to produce an assembled program, and a so-called one-pass assembler either leaves many references to be resolved by a loader or is a two-pass assembler, which does not require the source code to be read from an input device twice. The first pass checks the source code for syntactic errors and builds the symbol table in memory. The second pass completes the assembly and tags unresolved references for the loader. The language compiler adds one translation pass at the front end of this process.

Utility routines should be supplied for arithmetic and data conversion and for source code debugging. I/O handlers should be provided. Loaders should be furnished for all software supplied with the system and all applications programs.

System software should include diagnostic routines for system maintenance. Tests should be provided to check the operation of every unit in the system and to diagnose malfunctions within those units supplied as spare parts. Many manufacturers provide software on a modular basis. Each module requires a specific minimum hardware configuration, number of memory locations, optional features, interrupt lines, mass storage, and peripheral devices.

Operating systems for minicomputers are becoming increasingly important, particularly for systems that include mass storage devices. Most operating systems are of the foreground/background type; one or more real-time programs can be executed in the foreground and one batch program can be executed in the background. Batch background programs are sometimes priority-oriented. Time-sharing operating systems for minicomputers are also available from major minicomputer manufacturers and some independent vendors.<sup>10</sup>

Foreground/background operating systems make minicomputers suitable for real-time control applications, and increase the efficiency of the overall computing system. Real-time programs are incorporated into the operating system and are executed in the foreground, while batch programs can be executed during leftover

processor time in the background. The important feature of these systems for control applications is that new real-time programs can be debugged and prepared for incorporation in the operating system without closing down the system.

Time-sharing operating systems are a variation of the foreground/background operating systems. Instead of real-time control programs being executed in the foreground, all time-sharing users are in the foreground.

Operating systems vary in complexity, depending on the kinds of applications for which they were designed. Most manufacturers who include operating systems in their software packages offer modular systems with more features available as the hardware configuration increases in size. Operating systems handle the following functions:

- Communication between the operator and the system.
- I/O.
- Servicing of the interrupt system.
- File definition and manipulation.
- Processor status.
- Initiation of program execution.
- Core assignment.

User programs have access to the preceding facilities only through the operating system to ensure against inadvertent destruction of the programs in core.

System generation permits tailoring the operating system to a particular hardware configuration. Only those modules required by the application are incorporated into the operating system for that application. For example, if the hardware configuration includes no magnetic tape units, no magnetic tape handler programs are loaded. System generation occurs only once for an installation unless new equipment is added.

Organization of the operating system depends on the type of system. Foreground/background real-time systems execute programs on a priority basis; the priority of each program application is assigned on the basis of the required response time. The execution time of real-time programs is usually short, and any long calculations are performed by background programs. Background programs can be executed in the order received by the operating system, or programs can be executed in accordance with an assigned priority that can be changed by the operator via the console or control cards.

Time-sharing systems can assume all users have equal priority and allocate a time slice to each one. Alternatively, the time-sharing system can assume that some users have higher priority than others; and the programs of high-priority users are permitted to run to completion.

Communication between the operator and the system can be via a Teletype keyboard/printer, card or tape reader and punch, and/or line printer. The operating

system includes an interpreter routine that decodes messages from and generates messages to the operator. The communications codes provided limit an operator's control over the system.

Operating systems handle all I/O for the system; users specify their I/O via logical unit numbers. The operating system maintains queues for the use of I/O devices and overlaps I/O operations with processing.

The manufacturer designing the operating system makes various assumptions on which to base the system. These assumptions or system parameters are based on the hardware and the application for which the hardware will be used; they include such factors as the average core storage required by a foreground or background problem, the maximum number of foreground problems, the maximum number of priority levels allowed, the type of programs that can be run in the foreground and background, and the system software a user can utilize. Thus, a particular operating system can be too big and complex, too small and simpleminded, or about right for a particular application, depending on the parameters used in the system design. The selection criteria must spell out the minimum facilities required of the operating system.

The structures of various files are based on the anticipated needs of the applications for which the system was designed. The means for addressing, changing, and adding to files should be examined in the light of the file use for an application.

The operating system allocates memory for all programs executed. Normally, the memory map includes three main areas; one area is assigned to the resident portion of the operating system, another area is assigned to the resident applications programs, and the third area is assigned for temporary use by all other executing programs — whether system or user. The amount of memory devoted to resident applications programs and to temporary programs determines the size of programs that can be run. If the temporary storage area is too small for applications programs or for the required systems programs, then more memory must be added.

Manufacturers also emphasize the system software packages that can run under the operating system, the ease of inserting programs into the batch stream, the protection safeguards for users files, and the facilities for segmenting large programs into a size that can be handled by the system.

In general, when considering operating systems, the judgement criteria are not very different from those used in evaluating operating systems of larger computers. Usually, the small computer system must respond to new requirements, however. Some insight into operating system organization or methods for making additions — specifically in the I/O area — is desirable.

### Qualifications of the Manufacturer

The characteristics attributed to the manufacturer supplying the system are important in selecting a system because users require many services from this manufacturer. Consideration should also be given to the following factors:

- Reputation of the sales personnel.
- Delivery schedules and reputation for meeting them.
- Maintenance, distance of computer site from manufacturer or service center, and quality of the field engineering staff.
- Software support available for applications programming.
- Number of systems delivered.
- Quality of documentation on hardware and software.
- Training provided.
- General reputation of the hardware and software.
- Financial health of the vendor.

### Settling on a System

At this point, the selection criteria should include only those features that are relevant to the application. Some criteria are critical; these must be identified, and all computers without the critical features should be ignored. From the selection criteria, the selection committee should make up a hardware list and, using AUERBACH reports or other computer surveys, select a group of manufacturers that can do the job.

The committee can calculate hardware costs from price lists or seek bids from the manufacturers of acceptable computers. Seeking bids is preferable if special equipment, special services, or a competitive bid is required.

The first step is to solicit the "long list," which describes the functional requirements and requests a response of qualification and interest in bidding. From this information the "short list" of three to six vendors will do; these are asked for a formal proposal.

Using the performance criteria described previously, the next step is to calculate the system performance for all acceptable computers:

$$P_c = \sum_{i=1}^N W_i S_i$$

- where P = system performance  
c = a particular computer system  
i = a selection criterion for an application  
N = the total number of selection criteria for that application  
W = criterion weight  
S = implementation scale factor. <sup>11</sup>

A unique performance number (P) can now be associated with each acceptable computer system.

When the proposals for the computer hardware are received, the selection committee can compute a total system price. This price includes the manufacturer's system price plus the estimated in-house costs for programming, hardware, and operations. Once the total system costs for all proposed systems are obtained, the price/performance ratios are calculated for each by dividing total system cost by the performance number.

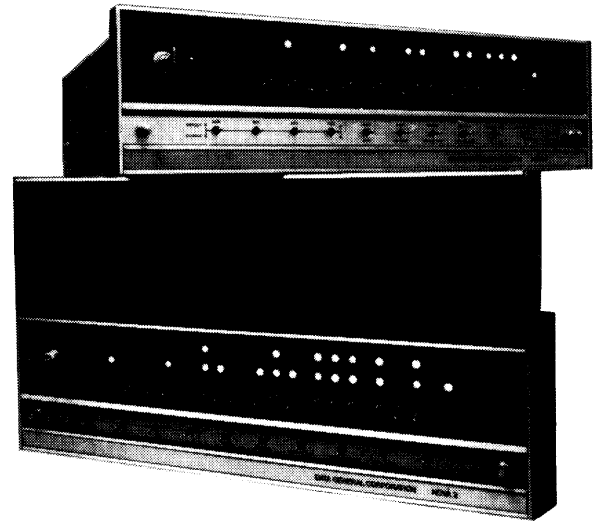
Logically, using this method, the selection committee selects the computer with the lowest price/performance ratio (PPR). Other factors, however, can dictate selecting some other system. The total system cost in relationship to the computer budget, for example, might force the selection of a lower-priced computer with a higher price/performance ratio. If two computers are roughly equivalent, the committee might select one over the other because of delivery schedules. Having performed the analysis described in the preceding paragraphs, the selection committee can make decisions on a sound analytical basis, and that is the main advantage of this approach.

## FUTURE DEVELOPMENTS

The rise of minicomputer technology has been explosive. The diversification of equipment and applications has been dramatic since 1968. Viewed from the standpoint of the problem to be solved, the history of computing technology can be described as follows:

Pre-history	Mechanical computing; abacus to Hollerith.
50's	Widespread computation, but unreliable and expensive.
60's	Centralized large computers with languages and operating systems; problems forced to conform to batch processing regimes.
70's	Decentralized task-oriented processing, using language and processors scaled to the task.
Beyond	Further melding of hardware and software techniques, with highly individual designs extending into the CPU itself.

It is a fact that minicomputer manufacturers are selling larger average systems. One minicomputer manufacturer spokesman notes that the average system now shipped is valued at \$37,000. Four years ago it was only \$14,000. More system software and more peripherals are available. The basic small computer is still very much the big seller; but it has larger cousins now. The genealogy can be observed by looking at Data General as an example of the industry trend maker: first the Nova, then the Supernova; the line was subsequently filled out with Nova 800 and Nova 1200, then the "hairy" (big) 840; all software compatible; followed by the tiny Nova 2/4 and 2/10; now the much grander ECLIPSE. Another example is Varian: first came the simple 620A, then the fast 620F, next the economical L100, and finally the V70 Series; all software upward compatible.



75-12

Figure K. Data General Nova 2/4 and 2/10

The glamour and promotion are concentrated on the maxi-mini and the new compilers, but this rising scale of grandeur is deceptive. At the other end of the spectrum, history is repeating itself. As the mini has challenged large computer designers, now the microprocessor challenges the established minicomputers. The burgeoning activity centers on a new set of suppliers — the computer-on-a-chip vendors who are producing scaled-down minicomputers. The decade ahead should see far greater emphasis on system engineering, task-oriented design than was ever true for minicomputer design. The fortunate user can now choose from an almost complete spectrum of solutions for a problem and truly find just the right amount of hardware and software to do the job.



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Figure L. Data General ECLIPSE® Computer

# AUERBACH ON MINICOMPUTERS

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# SPECIFICATION CHART

## Microprocessors—Microcomputers

AUERBACH Buyer's Guide to . . .  
MINICOMPUTERS

MANUFACTURER	American Microsystems Inc.	Applied Computing Technology	Applied Computing Technology	Applied Data Communications	Applied Systems Corp.
Model Number	AMI 6800	UMPS-4	PPS-4MP	70-100	ASC/8
<b>PHYSICAL PACKAGE</b>					
Number of boards	—	2	7	1	3 minimum
Dimensions	—	5 x 7"	5 x 7"	16 x 15"	Depend on opts
Number of chips	1	4	Variable	—	1
Number of pins/chip	40	42	42	—	40
Power Supply (std, opt)	+5V opt	Opt	Std	Opt	Std/opt
Console (std, opt)	No	Opt	Std	Opt	Opt
Cabinet (std, opt)	No	Std	Std	Opt	Rugged opt
<b>PROCESSOR</b>					
Manufacturer	Motorola	Rockwell	Rockwell	Intel	Intel
Model Number	6800	PPS-4	PPS-4	8080	8080
Technology Used (n/pMOS, bipolar)	nMOS	pMOS	pMOS	nMOS	nMOS
Word size	8	4	4	8	8
Data, bits	8	8	8	8/16/24	8/16/24
Instruction, bits	8, 16	8	8	2000	2000
Clock frequency, KHz	100	200	200	—	—
Add Time, reg to reg, $\mu$ sec	2	4.0 (4-bit wd)	4.0 (4-bit wd)	2	2
Number of instructions	72	50	74	—	74
Number of registers	6 internal	2 (12-bit)	2 (12-bit)	—	—
$\mu$ programmed	No	Yes	Yes	No	No
Fixed-point Arithmetic (+, -, X, $\div$ )	—	—	—	—	—
Implementation (binary, BCD), (std, opt)	Yes	Binary, BCD	Binary, BCD	Std	Std
<b>MEMORY</b>					
Types — (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	nMOS	pMOS	pMOS	NA	nMOS
Word size, bits	8	8	8	—	8
Capacity, words	1K	16K	16K	—	32K
Cycle time, $\mu$ sec	0.575	1.25	1.25	—	—
RAM (std, opt)	—	—	—	—	Opt
<b>RAM</b>					
Technology	nMOS	pMOS	pMOS	nMOS	—
Word size, bits	8	4	4	8	8
Capacity, words	128	4K	4K	16K CPU; 64K system	64K
Cycle Time, $\mu$ sec	1.0	1.25	1.25	—	—
<b>PROM</b>					
Technology	—	pMOS	pMOS	—	nMOS
How programmed?	—	UV erasable	UV erasable	UV reprogrammable	Elect.
Word size, bits	—	8	8	8	8
Capacity, words	—	16K	16K	4K CPU; 64K system	64K
Cycle time, $\mu$ sec	—	1.0	1.0	—	—
<b>INPUT/OUTPUT</b>					
I/O word size, bits	8	Three 4-bit groups	Three 4-bit groups	8/32	8/32
Number of device addresses	10 max	16	16	To 2K	To 2048
Programmed I/O	No	Yes	Yes	Yes	Yes
Direct Memory Access	Yes	Yes	Yes	Opt	Opt
Type of interrupt system	Vectored	NA	NA	Vectored	Vectored
I/O rate, wds/sec	—	4K	4K	500K	500K
Device interfaces available — (List)					
	General purpose communications interface; peripheral interface adapter; async communications interface adapter; universal sync receiver xmitter	Keyboard; display; printer; teletype; RS-232; paper tape reader; Silent 700	Keyboard display; printer; teletype; RS-232; paper tape reader; Silent 700	IBM compatible floppy disc; 3M tape cartridge; 9-track tape; GP I/O card; ROM programmer; memory expansion; real-time clock; RS-232 and current loop; sync or async communications controller	T2L; EIA Communications; teletype; printer; graphic; CRT; disc; keyboard; A/D
<b>SOFTWARE</b>					
Assembler	Yes	Yes	Yes	—	Yes
Cross assembly (what system?)	Yes	FORTRAN IV	FORTRAN IV	—	FORTRAN; (IBM 370)
Simulators (For what)	360/370 IBM	Time share	Time share	—	Yes
Languages	FORTRAN IV	No	No	—	Basic; PL/M
Operating System	No	No	Yes	ADC micro Exec*	Yes
Software (bundled?)	No	Yes	Yes	—	Opt
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	—	Opt
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	—	Prototypes small production systems	Stand-alone development system for Rockwell PPS-4 microcomputer set	Stand-alone small business system; word processing; communication system	Communications controller for IBM bi-sync protocol to multiple async terminals
First Delivery	12/74	12/73	4/73	4/75	1974
Number delivered	—	60	70	—	—
<b>STANDARD SYSTEM</b>					
	—	1K wds ROM; 1K wds RAM	1K wds ROM; 1K wds RAM	CCPC board with RS232/TTY controller; 1K bytes ROM; 4K RAM	1K wds ROM/1K wds RAM
<b>PRICE, \$</b>					
	Single quantities/69	855/695	2495; 2495	1300	1,000
<b>Other Features</b>					
	—	—	Prom programmer; high speed tape reader; RS-232 interface as options	*also ADC Micro DOS, floppy disc in same enclosure opt expandable to 8	Optional communications terminal control features for ASCII/EBCDIC conversion; buffering and multiplexing

# SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Cramer Electronics	Control Logic	Control Logic	Data Architects	Data Numerics
Model Number	CRAMERKIT 1	L Series	M Series	CM101	DL8A
<b>PHYSICAL PACKAGE</b>					
Number of boards	—	3 minimum	3 minimum	1	1
Dimensions	—	3" x 4.5"	3" x 4.5"	13.1 x 6.1 x 2	16" x 8"
Number of chips	25	25	23	92	90
Number of pins/chip	Various	Variable	Variable	—	Varies
Power Supply (std, opt)	Opt	Opt	Opt	Opt	Opt
Console (std, opt)	Std	Opt	Opt	Opt	Opt
Cabinet (std, opt)	Opt	Opt	Opt	Opt	Opt
<b>PROCESSOR</b>					
Manufacturer	Intel/T.I./Motorola/AMD	Intel	Intel	Intel	Intel
Model Number	8080A/8080/6800/9080	8008-1	8080	4004-4040	8080
Technology Used (n/pMOS, bipolar)	nMOS	pMOS	nMOS	pMOS	pMOS
Word size	—	—	—	—	—
Data, bits	8	8	8	4	8
Instruction, bits	8	8/16/24	8/16/24	8/16	8
Clock frequency, KHz	—	250	2000	636	—
Add Time, reg to reg, $\mu$ sec	—	12.5	2.0 +	12.6	—
Number of instructions	—	48	78	45	—
Number of registers	—	7	8	17	—
$\mu$ programmed	—	No	No	No	—
Fixed-point Arithmetic (+, -, X, $\div$ )	—	—	—	—	—
Implementation (binary, BCD); (std, opt)	—	Binary std	BCD & Binary; std	BCD & Binary std	—
<b>MEMORY</b>					
Types – (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	—	NA	NA	Any std	All
Word size, bits	—	—	—	8	8
Capacity, words	—	—	—	4K banks	64K
Cycle time, $\mu$ sec	—	—	—	1.1	Various
<b>RAM (std, opt)</b>					
Technology	Std nMOS	Opt pMOS	Opt pMOS	Any std	All
Word size, bits	8	8	8	4	8
Capacity, words	1024	1K/board	1K/board	4K banks	64K
Cycle Time, $\mu$ sec	0.45	1.5	1.5	1.1	Various
<b>PROM</b>					
Technology	FAMOS <sup>(1)</sup>	Opt pMOS	Opt pMOS	Std FAMOS <sup>(1)</sup>	All
How programmed?	Pgmr avail as kit	UV Erasable; FAMOS	UV Erasable; FAMOS	Electrically	Electrically
Word size, bits	8	8	8	8	8
Capacity, words	1024	512/board	512/board	256 or 512	8
Cycle time, $\mu$ sec	0.45	1.0	1.0	1.0	Various
<b>INPUT/OUTPUT</b>					
I/O word size, bits	8	8	8	4	8
Number of device addresses	8	32	256 in/256 out	32	Various
Programmed I/O	Yes	Yes	Yes;	Yes; std	Yes
Direct Memory Access	Yes	Opt	Opt	No	Yes
Type of interrupt system	1 interrupt	Vectored; 8 levels	Vectored; 8 levels	No; uses polling	8-level
I/O rate, wds/sec	—	13K	43K	20K	To 1M Hertz
Device interfaces available—(List)	RS-232; TTY; audio cassette	TTY; EIA RS 232C; general serial; general parallel; high speed paper tape reader and punch; CRT; floppy disc; PROM programmer	TTY; EIA RS-232C; general serial; general parallel; high speed paper tape reader; high speed punch; CRT; floppy disc; PROM programmer	TTY; 4-bit parallel; 8-bit parallel; time of day; gp serial interfaces all on same board as processor	Mag tape; cassette; cartridge; TTY; CRT paper tape; keyboard
<b>SOFTWARE</b>					
Assembler	Avail 1st qtr 1976	Yes	Yes	Yes	Yes
Cross assembly (what system?)	—	PDP-8	PDP-8	Tymshare	PDP-8/PDP-11
Simulators (For what)	—	N/A	N/A	Tymshare	—
Languages	—	L Series Assembly	M Series Assembly	Assembler	—
Operating System	Yes	ODT	ODT	Custom	—
Software (bundled?)	Yes	Bundled or separate	Bundled or separate	No	—
<b>APPLICATIONS</b>					
Replace Hard wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	—	Yes	Yes	Yes	No
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	Yes	Simulation	Simulation	Communications controller	—
First Delivery	9/75	4/73	9/74	—	1975
Number delivered	—	2,250 L and M	2,250 L and M	—	25 +
<b>STANDARD SYSTEM</b>					
	With 1K wds ROM and 1K RAM	With 1K wds ROM/with 1K wds RAM	With 1K wds ROM/with 1K wds RAM	With 1K words ROM	1K ROM/1K RAM
<b>PRICE, \$</b>					
	495	569/460	729/620	1,740	950/850
<b>Other Features</b>					
	(1) Floating gate Avalanche MOS	LDS series development series contains processor; 4K bytes RAM; Monitor/debugger loader; parallel I/O interfacing; TTY interface; console; powered enclosure; assembler; editor; PROM programmer for 2,340	MDS-M Series development system includes processor; 5K RAM; Monitor/debugger/loader; parallel I/O interface; TTY interface; console; powered enclosure; assembler; editor; PROM programmer costs \$2,340	(1) Floating gate Avalanche MOS	—



MANUFACTURER	Digital Equipment	Digital Equipment	Digital Laboratories	Fabritek	Fairchild Semiconductor
Model Number	LSI-11	MPS System	PB 96	MP12	F8S-simboard
<b>PHYSICAL PACKAGE</b>					
Number of boards	1	1	1	2	1
Dimensions	10.5 x 8.5"	8.5 x 10 x 0.5	9 x 15"	16.3 x 9.5"	12 x 6"
Number of chips	55	50	72	130	5
Number of pins/chip	16	18	14/16	14/16	5/12
Power Supply (std, opt)	Opt	Std	Opt	Opt (+5VDC)	Std
Console (std, opt)	Opt	Std	Opt	Std	—
Cabinet (std, opt)	Opt	Std	Opt	Opt	—
<b>PROCESSOR</b>					
Manufacturer	Digital Equipment	Intel	Digital Labs	Fabritek	Fairchild
Model Number	LSI-11	8008	PB96P	MP-12	3850
Technology Used (n/pMOS, bipolar)	nMOS	pMOS	TTL	Bipolar	nMOS
Word size					
Data, bits	16	8	8	12	8
Instruction, bits	16	8	8/16	12	8
Clock frequency, KHz	833	500K	9600	12,000	2000
Add Time, reg to reg, $\mu$ sec	3.5	20.0	5.9	3.0	5
Number of instructions	Over 400	48	18	28	60
Number of registers	8	—	12	Single accumulator	67
$\mu$ programmed	Yes	Yes	No	No	Yes
Fixed-point Arithmetic (+, -, X, $\div$ )					
Implementation (binary, BCD); (std, opt)	Opt	—	Opt	Binary	—
<b>MEMORY</b>					
Types — (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	nMOS	—	MOS/pROM	Bipolar	MOS
Word size, bits	16	—	8	12	8
Capacity, words	28K	—	1K	2K	1K
Cycle time, $\mu$ sec	0.5	—	1.2	1.5	5
<b>RAM (std, opt)</b>					
Technology	nMOS and Core	nMOS opt	Opt	Core	MOS
Word size, bits	16	8	8	12	8
Capacity, words	28K	4K/board	64K	4K	2K
Cycle Time, $\mu$ sec	0.5; 1.2	1.1	5.6	1.5	5
<b>PROM</b>					
Technology	MOS	Opt	1702A	Bipolar	Bipolar
How programmed?	Fusible link	—	—	FL	Fused link
Word size, bits	16	8	8	12	8
Capacity, words	28K	4K/board	1024	2K	2K
Cycle time, $\mu$ sec	0.7	1.0	1.2	1.5 $\mu$ sec	5
<b>INPUT/OUTPUT</b>					
I/O word size, bits	16	8	8	12	8
Number of device addresses	4K	—	12	63	4
Programmed I/O	Yes	—	Yes	Yes	—
Direct Memory Access	Yes	No	Opt	Single channel	—
Type of interrupt system	Single-line; vectored	—	Opt	Single channel	Vectored
I/O rate, wds/sec	833K wds/sec	—	2.9 $\mu$ sec/byte	PIO 66KHX/DMA 666KHz	—
Device interfaces available — (List)	For serial devices	Full duplex serial interface	RS232C; TTY; punch tape; card reader; floppy disc; keyboard; Burroughs self-scan	Async communication; high speed paper tape; RDR/PCH; TTY; cassette tape; line printer; char printer; digital input/output; D to A; IBM compatible mag tape; extension data store	—
<b>SOFTWARE</b>					
Assembler	Yes	PDP-8	Yes, pass	Yes	Yes
Cross assembly (what system?)	—	PDP-8	PDP-8 pass	IBM 360/370	FORTRAN
Simulators (For what)	—	—	PDP-8	NA	F8
Languages	BASIC; FORTRAN; FOCAL	—	None	PDP-8 compatible	—
Operating System	RT-11	—	Editor	Real-time exec	—
Software (bundled?)	Unbundled	—	Yes	Yes	Debug
<b>APPLICATIONS</b>					
Replace Hard wired logic	—	—	Yes	Yes	Yes
Commercial processing	—	—	Yes	No	Yes
Data acquisition	—	—	Yes	Yes	Yes
Terminals	—	Yes	Yes	Yes	Yes
Device controllers	—	Yes	Yes	Yes	Yes
Process control	—	Yes	Yes	Yes	Yes
Any others?	General purpose mini-computer	—	Word processing; large buffer/controller; communications buffer; programmable calculator interface	—	—
First Delivery	4/75	1974	3/74	—	6/75
Number delivered	—	—	—	—	15
<b>STANDARD SYSTEM</b>					
	4K words RAM	—	With 1K wds ROM/ With 1K wds RAM	With 4K words RAM; power supply; chassis and 12-bit microcomputer	NA
<b>PRICE, \$</b>					
	990	—	295/275	2395	—
Other Features	—	—	Architecture oriented towards use of large serial working memory (CCDS or other shift registers). Made of TTL IC's readily available. Licensing arranged for most users if desired.	—	—

# SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Fairchild Semiconductor	General Automation	General Automation	General Automation	General Instrument
Model Number	F8-C	GA-16/110	GA-16/220	GA-8/55	GIC 1600
<b>PHYSICAL PACKAGE</b>					
Number of boards	7	1	2	1	4
Dimensions	6 x 8"	7-3/4 x 11"	7-3/4 x 11"	7-3/4 x 11"	9.75" x 9.25
Number of chips	—	2	2	1	202
Number of pins/chip	5/12	48	48	40	14.40
Power Supply (std, opt)	Std	Opt (plug in)	Opt (plug-in)	Opt (plug in)	Opt
Console (std, opt)	Std	Std	Std	Std	Std
Cabinet (std, opt)	Std	Opt	Opt	Opt	Std
<b>PROCESSOR</b>					
Manufacturer	Fairchild	GA	GA	Intel	General Instrument
Model Number	3850	—	—	8080	CP1600
Technology Used (n/pMOS, bipolar)	nMOS	nMOS	nMOS	nMOS	nMOS
Word size	8	16	16	8	16
Data, bits	8	16	16	8	10
Instruction, bits	2000	12.6	—	2000	5000
Clock frequency, KHz	5	2.0	2.0	2.0	2.4
Add time, req to reg, μsec	60	91 std; 120 opt	91 std; 120 opt	89	87
Number of instructions	67	16	16	7	8
Number of registers	Yes	Yes	Yes	Yes	No
μprogrammed					
Fixed-point Arithmetic (+, -, X, ÷)					
Implementation (binary, BCD); (std, opt)		Binary std	Binary std	Binary and decimal conversion std	Std
<b>MEMORY</b>					
Types — (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	MOS	Bipolar	Bipolar	Bipolar	nMOS
Word size, bits	8	16	16	8	10-16
Capacity, words	1K	64K	64K	58K bytes	32K/card
Cycle time, μsec	5	0.5	0.5	0.5	0.5
<b>RAM (std, opt)</b>					
Technology	MOS	nMOS	nMOS	nMOS	nMOS
Word size, bits	8	16-18 opt	16-18 opt	8	16
Capacity, words	4K	64K	64K	56K bytes	8K/card
Cycle Time, μsec	5	0.5	0.5	0.5	0.5
<b>PROM</b>					
Technology	Bipolar	Bipolar	Bipolar	Bipolar	pMOS; Silicon gate
How programmed?	Fused link	Fusible link	Fusible link	Fusible link	electrically; UV
Word size, bits	8	16	16	8	16
Capacity, words	4K	64K	64K	56K	4K wds/card
Cycle time, μsec	5	0.5	0.5	0.5	1.5
<b>INPUT/OUTPUT</b>					
I/O word size, bits	8	16	16	16	16
Number of device addresses	4 per board	64	64	64	65K
Programmed I/O		Std	Std	Std	Yes
Direct Memory Access	Option	Std	Yes	Yes	Yes
Type of interrupt system	Vector	Vectored priority	3-level vectored	Vectored priority	Multilevel vectored
I/O rate, wds/sec		PIO 200K; DMA 2M	PIO 200K; DMA 2M	PIO 100K; DMA 2M	—
Device interfaces available - (List)		DIO; AC in; AC out; Analog out; threshold in; async comm; sync; bisync; SDLC; TTY; CRT; paper tape reader/punch; plotter; line printer; cassette; cartridge; floppy disc; magtape; disc	TTY; CRT; paper tape; card reader/punch; plotter; line printer; cassette; cartridge; floppy; magtape; disc	Digital In/Out; AC in/out analog in/out; threshold in; async comm; async mux; sync comm; bisync; SDLC; TTY; CRT; paper tape reader; plotter	TTY; EECO; REMEX or Tally high speed reader/punch; EIA interface devices
<b>SOFTWARE</b>					
Assembler	Yes	—	Yes	No	Yes
Cross assembly (what system?)	FORTTRAN	SPC-16 & GA-16/330	SPC-16 & GA-16/330	360/370	FORTTRAN IV, F level;
Simulators (For what)	F8	SPC-16/GA-16/330	SPC-16 & GA-16/330	360/370	GIC 1600 or host
Languages	—	FORTTRAN, COBOL, BASIC	FORTTRAN; COBOL; BASIC	PL/M 360/370	Assembly
Operating System	Yes	RTX	RTX; FSOS1DBOS; RTOS	No	Resident monitor
Software (bundled?)	Yes	No	No	No	On-line bundled
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?		Communications buffer	Communication buffer	Communications machine control	Telecommunications
First Delivery	9/75	—	—	5/75	—
Number delivered	5	—	—	—	—
<b>STANDARD SYSTEM</b>					
	N/A				CPU, 8K memory, console, ODP firmware, I/O and software
<b>PRICE, \$</b>					
		Compatible with SPC-16 software and I/O; PF/AR; RTC port; integral displays; operations monitor; remote load; single PC board; parity opt; memory protect opt; cold start ROM	PF/AR; lms RTC; integral display; microconsole operator display; TTY/CRT; remote load; operations monitor alarm; microconsole opt complete micro on single board	PF/AR; 1usec RTC; cold start ROM; integral operator display; TTY/CRT; remote load; operations monitor alarm; microconsole opt complete micro on single board	3400
<b>Other Features</b>					



MANUFACTURER	General Instrument	GTE Information Systems	GTE Information Systems	Hollinbeck Enterprises	Hollinbeck Enterprises
Model Number	GIC 1601	IS/1011	IS/1014	MP-68	MP-11
<b>PHYSICAL PACKAGE</b>					
Number of boards	4	1 or more	1 or more	3	3
Dimensions	9.75" x 9.25"	12.5" x 20"	12.5" x 20"	8" x 14"	8.5" x 10"
Number of chips	209	80 +	80	—	—
Number of pins/chip	14 to 40	—	—	—	—
Power Supply (std, opt)	Opt	Opt +5V, +12V, -12V	Std	Std	Std
Console (std, opt)	Std	—	Opt	Std	Std
Cabinet (std, opt)	Std	Opt	Opt	Std	Std
<b>PROCESSOR</b>					
Manufacturer	General Instrument	GTE	GTE	AMI	DEC
Model Number	CP 1600	IS/1011	IS/1014	6800	LSI-11
Technology Used (n/pMOS, bipolar)	nMOS	Bipolar	Bipolar	nMOS	nMOS
Word size					
Data, bits	16	8	8 or 16	8	16
Instruction, bits	10	16	8, 16	8	16
Clock frequency, KHz	5000		.06	1000	1000
Add Time, reg to reg, $\mu$ sec	2.4	0.2	.2 (GP Reg to accum)	2	2
Number of instructions	87	40	80	72	400
Number of registers	8	17	16	5	8
$\mu$ programmed	No	Yes	Yes	Yes	Yes
Fixed-point Arithmetic (+, -, X, $\div$ )					
Implementation (binary, BCD), (std, opt)	Std	Binary std	Binary Std	Std	Binary, std
<b>MEMORY</b>					
Types - (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	nMOS	Opt Bipolar	Opt Bipolar	nMOS	nMOS
Word size, bits	10-16	16	8, 16	8	8
Capacity, words	32K/card	65K (off board)	16K	61K	61K
Cycle time, $\mu$ sec	0.5	0.15	1	1	1
RAM (std, opt)		Opt	Std		
Technology	nMOS	Bipolar/core	Core (off board)	nMOS	nMOS
Word size, bits	16	16	8	8	16
Capacity, words	8K/card	1K	16K	61K	28K
Cycle Time, $\mu$ sec	0.5	0.15	0.75	0.8	0.8
<b>PROM</b>					
Technology	pMOS; silicon gate	Opt Bipolar	Opt Bipolar	nMOS	nMOS
How programmed?	Electrically and UV	Fusible link	Fusible link	Elec	Elec
Word size, bits	16	16	8 or 16	8	16
Capacity, words	4K wds/card	65K	4K on board	61K	28K
Cycle time, $\mu$ sec	1.5	0.15	0.1	0.1	1
<b>INPUT/OUTPUT</b>					
I/O word size, bits	16	8	8	8	16
Number of device addresses	65K	256	256	4096	4096
Programmed I/O	Yes	—	Yes	Std	Std
Direct Memory Access	Yes	—	Yes	Std	Std
Type of interrupt system	Multi-level vectored	—	—	Vector	Vector
I/O rate, wds/sec	—	—	—	45K bytes/sec	90K wds/sec
Device interfaces available - (List)	TTY; EECO; REMEX or Tally high speed reader/punch; EIA interface devices	Buffer memory; interval timer, cyclic redundancy check/generate; code conversion memory	Cash register; modem controllers; debug hardware	Floppy disc RS-232; modem	Floppy disc; RS232; modem
<b>SOFTWARE</b>					
Assembler	Yes	No	No	Resident	Resident
Cross assembly (what system?)	F-level FORTRAN IV	GTE IS 1000	GTE/IS 1000	No	No
Simulators (For what)	GIC 1600 or host	No	No	No	No
Languages	Assembly	No	No	BASIC	BASIC, FORTRAN IV, COBOL
Operating System	Resident monitor	No	No	DOS	RT-11
Software (bundled?)	On-line bundled	No	No	No	No
<b>APPLICATIONS</b>					
Replace Hard wired logic	Yes	—	—	No	No
Commercial processing	Yes	—	Yes	Yes	Yes
Data acquisition	Yes	—	—	Yes	Yes
Terminals	Yes	Yes	No	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	—	Yes	Yes	Yes
Any others?	Telecommunications	—	—	—	Yes
		For hardware debug; memory units; communications interfaces			Floppy disc; RS-232; modem
First Delivery	7/75	1/75	11/74	8/75	12/75
Number delivered	25	—	—	—	NA
<b>STANDARD SYSTEM</b>					
	CPU, 8K memory, console, ODP firmware, I/O and software			With 1K words of ROM	1K words ROM
<b>PRICE, \$</b>					
	3500			7500	9,000
Other Features				Includes 16KB RAM; dual floppy disc; assembler; loader, text editor and operating system; OEM discounts available	Includes 16KB RAM; dual floppy disc; assembler; loader; text editor; and operation system; OEM discounts available

# SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Intel	Intel	Intel	Intel	Intel
Model Number	4004 (MCS-4)	4040 (MCS40) (Intellec. 4)	8008	8080	MDS-800 (8080A)
<b>PHYSICAL PACKAGE</b>					
Number of boards	1	—	—	—	4 std; 14 more opt
Dimensions	6.18 x 8 x .06"	—	—	—	—
Number of chips	7	1	1	1	—
Number of pins/chip	16/24	24	40	40	16/24/40
Power Supply (std, opt)	Opt	Opt	Opt	Opt	Std
Console (std, opt)	Opt	Opt	No	No	TTY; CRT opt
Cabinet (std, opt)	Opt	Opt	No	No	Std
<b>PROCESSOR</b>					
Manufacturer	Intel	Intel	Intel	Intel	Intel
Model Number	4004	4004	8008	8080	8080A
Technology Used (n/pMOS, bipolar)	pMOS	pMOS	pMOS	nMOS	nMOS
Word size	4	4	8	8	8
Data, bits	4	4	8	8	8
Instruction, bits	8, 16	8, 16	8, 16, 24	8, 16, 24	Multiple of 8
Clock frequency, KHz	740	740K	500 to 800	2080 to 3000	2000
Add Time, reg to reg, $\mu$ sec	10.8	10.8	20/12.5	2-1.33	—
Number of instructions	46	60	48	78	72
Number of registers	16	24	7 8-bit data regs	7 8-bit data regs	6 16-bit
$\mu$ programmed	No	No	No	No	No
Fixed-point Arithmetic (+, -, X, $\div$ )	—	—	—	—	—
Implementation (binary, BCD); (std, opt)	Binary, BCD Std	Binary; Logical BCD Std	Binary	Binary, BCD	Binary; BCD Std
<b>MEMORY</b>					
Types – (ROM/RAM/PROM)					
ROM	Std	Std	—	—	—
Technology (n/pMOS, bipolar)	pMOS	pMOS	pMOS, nMOS, Bipolar	pMOS, nMOS, bipolar	All
Word size, bits	4	8	8	8	8
Capacity, words	1K	256	250-2K	250-2K	2K or 14K
Cycle time, $\mu$ sec	—	—	0.5-1.5	0.5-1.5	0.07
RAM (std, opt)	Std	Std	—	—	Std
Technology	pMOS	—	pMOS, nMOS, CMOS	pMOS, nMOS, CMOS	nMOS
Word size, bits	4-bits	—	1, 4	1, 4	8
Capacity, words	320	—	256-4K	256-4K	16K
Cycle Time, $\mu$ sec	—	—	1.5	1.5	1
PROM	Opt	Std	—	—	—
Technology	—	—	pMOS, nMOS, bipolar	pMOS, nMOS, bipolar	nMOS, bipolar
How programmed?	—	—	Fusible link, FAMOS	Fusible link, FAMOS(1)	PROM programmer
Word size, bits	—	—	8; 4	8; 4	4/8
Capacity, words	1K	—	2.8K	2K-8K	12K
Cycle time, $\mu$ sec	—	—	0.5-1.5	0.5-1.5	0.07
<b>INPUT/OUTPUT</b>					
I/O word size, bits	4-bits	—	8	8	8; 16 DMA
Number of device addresses	—	—	256	256	256 expandable
Programmed I/O	—	—	—	—	Yes
Direct Memory Access	No	—	—	—	Yes
Type of interrupt system	None	—	Vectored 8-level	Vectored 8-level	8-user mask
I/O rate, wds/sec	—	—	—	—	—
Device interfaces available—(List)	Clock; memory; I/O	Clock, RAM; I/O	—	—	RS232 (CRT); TTY; High speed reader; Line printer
<b>SOFTWARE</b>					
Assembler	—	Resident	Resident	Resident	Yes
Cross assembly (what system?)	Yes	Yes	FORTRAN IV	FORTRAN IV	Yes FORTRAN IV
Simulators (For what)	Yes	Yes	FORTRAN IV	FORTRAN IV	Yes FORTRAN IV
Languages	FORTRAN IV	FORTRAN IV	PL/M	PL/M	PL/M
Operating System	—	—	Yes	—	Yes
Software (bundled?)	No	No	Yes	No	Yes
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	—	—	Billing, accounting	Avionics	Prototype, development systems support is prime target
First Delivery	—	—	1971	1973	6/75
Number delivered	—	—	1M	—	300 +
<b>STANDARD SYSTEM</b>					
Price, \$	National Semiconductor second source	—	—	—	3950
Other Features	—	—	—	—	ICE (In Circuit Emulator) processor boards & cable with plug to prototype Dip socket, including all software support for user defined break point settling & debugging

MANUFACTURER	Keronix	Martin Research	Martin Research	Micro Computer Machines	MICROKIT
Model Number	IDS 16M	AT 804-3	AT 811-3	MCM/70	8/16
<b>PHYSICAL PACKAGE</b>					
Number of boards	1	4	4	5	4
Dimensions	7 x 10"	5.5 x 7"	5.5 x 7"	—	6 x 8"
Number of chips	50	—	—	—	29
Number of pins/chip	—	16, 18, 20, 24	16, 20, 24, 40	—	40 max
Power Supply (std, opt)	Opt	Opt	Opt	Std	Std
Console (std, opt)	Opt	Std	Std	Std	Std
Cabinet (std, opt)	Opt	Opt	Opt	Std	Std
<b>PROCESSOR</b>					
Manufacturer	Keronix	Intel	Intel/AMD/TI	Intel	Intel/AMD/TI
Model Number	IDS 16M	8008; 8008-1	8080; 8080A	8080	8080
Technology Used (n/pMOS, bipolar)	Bipolar	pMOS	nMOS	nMOS	nMOS
Word size	16	8	8	8	8
Data, bits	16	8	8	8	8
Instruction, bits	16	8, 16, 24	8, 16, 24	—	8, 16, 24
Clock frequency, KHz	100	500; 800	2000; 3200	—	100
Add Time, reg to reg, $\mu$ sec	1.5	2.0; 12.5	2; 1.25	—	2
Number of instructions	192	48	Std	—	78
Number of registers	4	17	8	—	7
$\mu$ programmed	No	No	No	—	No
Fixed-point Arithmetic (+, -, X, $\div$ )	—	—	—	—	—
Implementation (binary, BCD); (std, opt)	Std binary	No	No	—	Binary; BCD std
<b>MEMORY</b>					
Types -- (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	MOS	—	—	MOS	—
Word size, bits	16	—	—	8	—
Capacity, words	2K	—	—	32K	—
Cycle time, $\mu$ sec	0.5	—	—	—	—
<b>RAM (std, opt)</b>					
Technology	MOS	Std nMOS	nMOS	MOS	nMOS
Word size, bits	16	8	8	8	8
Capacity, words	32K	16K	64K	2K, 4K or 8K	56K
Cycle Time, $\mu$ sec	0.8	0.45	0.45	—	0.48 rd; 0.96 write
<b>PROM</b>					
Technology	MOS	pMOS	pMOS	—	—
How programmed?	—	Electric (1702A)	Electric (1702A)	—	EAROM UV erasable Electric
Word size, bits	16	8	8	—	8
Capacity, words	2K	2K +	2K +	—	8K
Cycle time, $\mu$ sec	0.5	1.0	1.0	—	0.45
<b>INPUT/OUTPUT</b>					
I/O word size, bits	16	8	8	8	8
Number of device addresses	62	32	548	199	512
Programmed I/O	Yes	Opt	Opt	Yes	Yes
Direct Memory Access	Yes	No	Opt	—	Yes
Type of interrupt system	Priority	Single level	8-level vectored	—	Vectored; priority
I/O rate, wds/sec	500K one-line	31K one-line	12K (PIO); 2M (DMA)	120	50K
Device interfaces available—(List)	TTY; real-time clock; paper tape reader and punch	TTY; 5-level TTY (Baudot); floppy disc; cassette tape; TV text (planned); PROM programming; multiprocessor (planned); ASCII keyboard (planned); Okidata 110-cps printer	TTY; 5-level TTY (baudot); floppy disc; cassette tape; TV text (planned); PROM programming (planned); multiprocessor interface (planned); Okidata 110 cps printer (avail); CRT monitor (planned)	Printer/plotter; communications subsystem; EIA RS 232C; current loop, APL/ASCII; ASCII; IBM correspondence; any user-defined 5, 6, 7 or 8-level code	Keyboard; CRT display; cassette tape; RS-232C; real-time clock; 110 cps line printer; 8 bit inter-processor port
<b>SOFTWARE</b>					
Assembler	Yes	Yes	Yes	—	Resident
Cross assembly (what system?)	—	Yes	Yes	—	IBM 370
Simulators (For what)	—	Yes	Yes	—	IBM 370
Languages	BASIC; FORTRAN	No	No	APL	—
Operating System	Yes	Monitor	Monitor	AVS virtual OS	Yes
Software (bundled?)	Bundled	No	No	Yes	Yes
<b>APPLICATIONS</b>					
Replace Hard wired logic	Yes	Yes	Yes	—	No
Commercial processing	Yes	—	—	Yes	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	No
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	—	Educational use; OEM prototyping	Educational use; OEM prototyping	Technical problem solving; scientific problem solving	Software development; microcomputer product testing and text editing
First Delivery	10/75	5/75	11/75	11/74	5/75
Number delivered	—	100	—	100 +	12
<b>STANDARD SYSTEM</b>					
	1K words ROM or 1K words RAM	256 bytes PROM, 256 bytes RAM	256 bytes PROM and 512 bytes RAM	With 32K ROM; 2K words RAM	With 1K ROM; 8K RAM
<b>PRICE, \$</b>					
	2000 Fully transparent to all applications for the Data General Nova	395 Extra RAM available to bring capacity up to 1K at \$950/256 bytes; 4K RAM board avail Kit only price—\$295	495 Extra RAM available to bring capacity up to 1K at \$950/256 bytes; kit only price—\$445	6500 Price includes 100K bytes virtual cassette storage; power fail/protect; I/O interface; printer/plotter driver; integral display; keyboard; virtual operating system	3850 Complete development system; 8K RAM, 2 cassette tape drives; keyboard; display, real-time clock interface to printer and PROM programmer
<b>Other Features</b>					

# SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	MITTS	Monolithic Memories	Motorola	Myco-Tek, Inc.	National Semiconductor
<b>Model Number</b>	Altair 8800	MMI 300	6800	MT 8080 PB	PACE
<b>PHYSICAL PACKAGE</b>					
Number of boards	1 to 16	1 to 13	—	1	—
Dimensions	17 x 15"	6.6 x 9.6" cards	—	13.5 x 7.5"	—
Number of chips	1	Various	6	—	1
Number of pins/chip	40	Various; 14 to 40	40, 24	—	40
Power Supply (std, opt)	Std	Std; 5V	No	5V, 3A opt	+5, -12
Console (std, opt)	Std	N/A	No	MT 210 opt	—
Cabinet (std, opt)	Std	Opt	No	Opt	—
<b>PROCESSOR</b>					
Manufacturer	Intel	Monolithic Memories	Motorola	Intel	National
Model Number	8080	MMI 300	MC 6800	8080	IPC-16A/500
Technology Used (n/pMOS, bipolar)	nMOS	Bipolar	nMOS Si-Gate	nMOS	pMOS
Word size					
Data, bits	8	16	8	8	16
Instruction, bits	8	16	8, 16, 24	8	16
Clock frequency, KHz	2000	3300	100 to 1000	1843	2000
Add Time, reg to reg, $\mu$ sec	2	0.9	2	2.71	8
Number of instructions	78	36 (expandable)	72	78	45
Number of registers	6	16	6	7	4
$\mu$ programmed	No	Yes	No	No	No
Fixed-point Arithmetic (+, -, X, $\div$ ) Implementation (binary, BCD): (std, opt)	Opt	—	BCD, std	Std	Binary or BCD
<b>MEMORY</b>					
Types – (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)		Bipolar	nMOS SiGate	pMOS/nMOS	pMOS/bipolar
Word size, bits		1 to 10	8	8	8; 16
Capacity, words		To 10K	1024	2K	512; 1K
Cycle time, $\mu$ sec		100 max	0.575	0.5	—
<b>RAM (std, opt)</b>					
Technology	nMOS	Bipolar; nMOS	nMOS SiGate	Opt nMOS	nMOS
Word size, bits	8	64; 256, 1K bipolar	8	8	4
Capacity, words	4K or 1K	4K nMOS 4K max	128	1/4K to 8K	256
Cycle Time, $\mu$ sec	0.47; 0.85	To 200	0.575	0.650	—
<b>PROM</b>					
Technology	MOS	Bipolar	—	pMOS	pMOS
How programmed?	Electric	Fusible link	—	—	Stored charge
Word size, bits	8	1 to 10	—	8	8
Capacity, words	2K	8K	—	1K std, 4K opt	512
Cycle time, $\mu$ sec	1	100	—	0.850	—
<b>INPUT/OUTPUT</b>					
I/O word size, bits	8	16	8	8	16
Number of device addresses	256	62	4; 2	256	64K
Programmed I/O	Yes	Yes	Yes	Opt	Yes
Direct Memory Access	Yes	Yes	No	Opt	Yes
Type of interrupt system	8-level	microprogrammed	Vectored	8-level vectored	Hardware or software vectored
I/O rate, wds/sec	8.5	—	30K-bytes; 500Kbps	1M wds/sec	60K bytes
Device interfaces available—(List)	Flexible disc drives; 110 char/sec line printer; ASR-33 TTY; CRT terminal; audio tape recorder; cyclops camera; plus general interfaces for most peripheral equipment	—	Modem; clocks; dynamic RAMS; static ROM; error pattern reg; longitudinal redundancy check, static character generators; A/D logic subsystem; bit rate generator polynomial generators	CRT with editor; control panel with monitor; high density memory; 32K on one card; high speed paper tape reader; line printer, dual cassette	16 bit bus transceiver (BTE); System clock (STE); 16-bit address latch (ALE/16); 8-bit address latch (ALE/8); 8-bit bidirectional interface latch (ILE/8); 16-bit bi-directional interface latch (ILE/16)
<b>SOFTWARE</b>					
Assembler	Yes	—	Resident/editor	Yes—MACRO	Yes
Cross assembly (what system?)	—	—	For time share nets	IBM	GE; Tymshare
Simulators (For what)	—	—	Selected 16-bit minis	IBM	—
Languages	Extended BASIC	Diagnostic	FORTTRAN IV	PLM/Assembly	ASMB
Operating System	DOS-OS	Nova-type	EDOS Floppy disc	Yes	—
Software (bundled?)	Yes	Custom	Both bundled & unbundled	Yes	Most
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes	No	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	General purpose computer	—	—	Education in microprocessor field; build up of small quantities	—
First Delivery	1/75	—	4/74	4/75	4/75
Number delivered	3500	—	—	10	—
<b>STANDARD SYSTEM</b>	With 1K words RAM	With 8K RAM	MPU, 2K RAM, 8K ROM, 2 PIAs + one ACIA, diagnostics for debugging; pc board	With 1K ROM/with 1K RAM	—
<b>PRICE, \$</b>	760/(536 for kit) Real-time clock	1,850 Military temp range devices available	149 1-99 Qty Exorciser evaluation modules, floppy disc system, high speed paper tape reader, memory I/O modules, software pkged in various storage media available	750/975 Comb. PC board and wire wrap on one card. On card power converter eliminates 3 power supplies aimed at small quantity prototype build-up	— 8 or 16-bit data handling; 5-level vectored priority interrupts
<b>Other Features</b>					



MANUFACTURER	National Semiconductor	PCS	PCS	Plessey Microsystems	Pro-Log
Model Number	IMP-16	MICROPAC 80	MICROPAC 80/A	MIPROC-16	PLS-401
<b>PHYSICAL PACKAGE</b>					
Number of boards	—	5	5	3	1
Dimensions	—	—	—	10" x 19"	4.5 x 6.5"
Number of chips	5	—	—	44	—
Number of pins/chip	24	—	—	N/A	—
Power Supply (std, opt)	+5, -12	Std	Std	+5V Std	+5V and -10V
Console (std, opt)	—	Std	Std	Std	—
Cabinet (std, opt)	—	Std	Std	Std	—
<b>PROCESSOR</b>					
Manufacturer	National	Intel	Intel	—	Intel, National
Model Number	IMP-16A/500	8080	8080	—	4004
Technology Used (n/pMOS, bipolar)	pMOS	nMOS	nMOS	Bipolar	pMOS
Word size	—	—	—	—	—
Data, bits	16	8	8	16	4
Instruction, bits	16	8-24	8-24	16	8
Clock frequency, KHz	700	2000	2000	3000	714.3
Add Time, reg to reg, $\mu$ sec	4.2	1.5	1.5	0.35	44.8
Number of instructions	43-71	78	78	82	44
Number of registers	4	7	7	256	16
$\mu$ programmed	Yes	No	No	Yes	No
Fixed-point Arithmetic (+, -, X, $\div$ )	—	—	—	—	—
Implementation (binary, BCD); (std, opt)	Binary	Std	Std	Binary	User-programmed
<b>MEMORY</b>					
Types — (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	pMOS/BIP	—	—	Bipolar	—
Word size, bits	8; 16	8	8	16	—
Capacity, words	512; 1K	64K	64K	4K	—
Cycle time, $\mu$ sec	—	1	1	0.075	—
RAM (std, opt)	—	—	—	—	—
Technology	nMOS	—	—	Bipolar	pMOS
Word size, bits	4	—	—	16	4
Capacity, words	256	64K	64K	4K	320
Cycle Time, $\mu$ sec	—	1	1	0.050	11.2
<b>PROM</b>					
Technology	pMOS	—	—	Bipolar	pMOS silicon gate
How programmed?	Stored charge	—	—	Fuse link	Series 90 PROM programmer
Word size, bits	8	8	—	16	8
Capacity, words	512	64K	64K	4K	1K
Cycle time, $\mu$ sec	—	1	1	0.070	11.2
<b>INPUT/OUTPUT</b>					
I/O word size, bits	16	16	16	16	4
Number of device addresses	64K	256	256	512	4
Programmed I/O	Yes	Std	Std	—	—
Direct Memory Access	Yes	No	No	No	No
Type of interrupt system	Hardware or software vectored	Vectored	Vectored	Externally vectored	No
I/O rate, wds/sec	180K bytes	140K	140KB	3M	190K
Device interfaces available—(List)	16-bit bus transceiver (BTE); System clock (STE); 16-bit address latch (ALE/16); 8-bit address latch (ALE/8); 8-bit bidirectional interface latch (ILE/8); 16-bit bidirectional interface latch (ILE/16)	TTL; high and low level digital and analog; TTY; RS 232 high speed communications; strain gage; stepper motor peripheral; interrupt expander; real-time clock; battery pack; PROM programmer	TTL; high and low speed analog and digital; TTY; RS 232; high speed communications; strain gage; stepper motor; peripheral; interrupt expander; real-time clock; battery pack	TTY; RS232;tape reader	TTL; Relay; opto-isolators; TRIAC's TTY; drivers; TTL to Hi-NiNil; MOS
<b>SOFTWARE</b>					
Assembler	Yes	Yes	MACRO	—	—
Cross assembly (what system?)	GE; Tymshare	HP-2100	HP 2100	FORTRAN IV	—
Simulators (For what)	—	No	No	Yes	—
Languages	ASMB; SM/PL	Assembly	Assembly	Yes	Assembly
Operating System	FDOS	BOS 80	BOS 80/A	—	—
Software (bundled?)	Most	Yes	Yes	Bundled	—
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	Yes	No	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	—	—	—	Military	Automatic test equipment
First Delivery	6/72	3/74	6/75	1975	2/73
Number delivered	—	300	5	12	—
<b>STANDARD SYSTEM</b>					
—	—	With 1K words ROM	With 1K words ROM	With 1K wds RAM	With 1K word ROM (single quantity)
<b>PRICE, \$</b>					
—	—	2650	2950	760 in quantity	275 at 500 quantity, price is \$171 with 1K words PROM and 320 bits of RAM
Other Features	Optional instruction sets avail, also user micro-programmable	Hardware used by almost all major industries	—	—	—

# SPECIFICATION CHART — MICROCOMPUTERS — MICROPROCESSORS

MANUFACTURER	Pro-Log	Pro-Log	Pro-Log	R2E	RCA Cosmac
Model Number	PLS-441	MPS-803	MPS-883	MICRAL	Microkit
<b>PHYSICAL PACKAGE</b>					
Number of boards	1	3	3	—	11
Dimensions	4.5 x 6.5"	4.5 x 6.5"	4.5 x 6.5"	—	4.5 x 3"
Number of chips	—	—	—	1	—
Number of pins/chip	—	—	—	—	—
Power Supply (std, opt)	+5V, -10V	+5V, -9V	+12V, +5V, -10V	Std	+5, +12, -9 (110AC)
Console (std, opt)	—	—	—	Std	No
Cabinet (std, opt)	—	—	—	Std	—
<b>PROCESSOR</b>					
Manufacturer	Intel	Intel	Intel	Intel	RCA
Model Number	4040	8008	8080	8008	COSMAC
Technology Used (n/pMOS, bipolar)	pMOS	pMOS	nMOS	—	CMOS
Word size	4	8	8	8	8
Data, bits	8	8	8	8, 16, 24	8
Instruction, bits	8	8	8	—	8
Clock frequency, KHz	714.3	357	625 or 1000	—	2000
Add Time, reg to reg, $\mu$ sec	44.8	14	5 or 8	12.5	—
Number of instructions	52	48	111	52	59
Number of registers	24	7	7	15	16
$\mu$ programmed	No	No	No	No	No
Fixed-point Arithmetic (+, -, X, $\div$ )	—	—	—	—	—
Implementation (binary, BCD): (std, opt)	User-programmed	User programmed	User programmed	Binary	Binary
<b>MEMORY</b>					
Types — (ROM/RAM/PROM)					
ROM	—	—	—	Bipolar	—
Technology (n/pMOS, bipolar)	—	—	—	8	—
Word size, bits	—	—	—	16K	—
Capacity, words	—	—	—	1.0	—
Cycle time, $\mu$ sec	—	—	—	—	—
RAM (std, opt)					
Technology	pMOS	nMOS	nMOS	MOS	nMOS
Word size, bits	4	8	8	8	8
Capacity, words	640	2K	2K	16K	1024
Cycle Time, $\mu$ sec	11.2	2.8	1.6; 1	1.0	0.65
PROM					
Technology	pMOS silicon gate	pMOS silicon gate	pMOS silicon gate	Bipolar	nMOS
How programmed?	Series 90 PROM programmer	Series 90 PROM programmer	Series 90 PROM programmer	—	ER and Elec.
Word size, bits	8	8	8	8	8
Capacity, words	1280	1K	1K	16K	512
Cycle time, $\mu$ sec	11.2	2.8	1.6 or 1	1.0	0.7
<b>INPUT/OUTPUT</b>					
I/O word size, bits	4	8	8	8	8
Number of device addresses	4	4	4	64	Any
Programmed I/O	—	—	—	Std	Yes
Direct Memory Access	No	Yes	Yes	No	Yes
Type of interrupt system	Single interrupt	Multi-level	Multi-level	—	Software
I/O rate, wds/sec	190K	250K	500K	1M	250K (DMA)
Device interfaces available — (List)	TTL; Relay; Opto-isolators; TRIAC's; TTY; drivers; TTL to Hi-NiNiil; MOS	TTL; relay; opto-isolators; TRIAC's; TTY; drivers; TTL to NiNiil; MOS	TTL; relay; opto-isolators; TRIAC's; TTY; Drivers; TTL to HiNiil; MOS	Optical electronic inputs; relay output; TTY, magnetic tape, paper tape; printer	TTY (ASR 33) 38 execution; T.1. silent 700
<b>SOFTWARE</b>					
Assembler	—	—	—	Yes	Cross, batch
Cross assembly (what system?)	—	—	—	—	FORTRAN IV
Simulators (For what)	—	—	—	—	Cross-A
Languages	Assembly	Assembly	Assembly	—	Assembly
Operating System	—	Monitor program	Monitor program	TTY; cassette	—
Software (bundled?)	—	No	No	Yes	No
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	Yes	Yes	—	Yes
Commercial processing	Yes	Yes	Yes	Yes	Yes
Data acquisition	Yes	Yes	Yes	—	Yes
Terminals	Yes	Yes	Yes	—	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	Automatic test equipment	Automatic test equipment	Automatic test equipment	Message switching; preprocessing	Yes
First Delivery	5/75	2/74	6/75	3/73	—
Number delivered	—	—	—	—	—
<b>STANDARD SYSTEM</b>					
	With 1K words ROM (single quantity)	Single quantity with 1K of 1702A PROM	Single quantity with 1K of 1702A PROM	With 256 wds of ROM	With 1K words RAM
<b>PRICE, \$</b>	450 at 500 qty, price is \$265 with 1K words of PROM and 320 bits of RAM	725	865	1,700 OEM discounts available	3000
Other Features					



MANUFACTURER	Rockwell	Rockwell	Scientific Micro Systems	Scientific Micro Systems	Signetics
Model Number	PPS-4	PPS-8	SMS-300	SMS-3000 (MCSIM)	N 3001
<b>PHYSICAL PACKAGE</b>					
Number of boards	—	—	1	14-20	—
Dimensions	—	—	2-5/8 x 6-7/8"	—	—
Number of chips	1	1	1	—	1
Number of pins/chip	42	42	64	—	40
Power Supply (std, opt)	-17V	-17V	No	Std	5V
Console (std, opt)	No	—	No	Std	—
Cabinet (std, opt)	No	—	No	Std	—
<b>PROCESSOR</b>					
Manufacturer	Rockwell	Rockwell	SMS	SMS	Signetics
Model Number	PPS-4	PPS-8	SMS-300	SMS-300	N3001
Technology Used (n/pMOS, bipolar)	pMOS	pMOS	Bipolar	Bipolar	Schottky bipolar
Word size					
Data, bits	4	8	8	8	—
Instruction, bits	8	8	16	16	11 minimum
Clock frequency, KHz	199KC	256KC	6666	6666	222,000
Add time, reg to reg, $\mu$ sec	0.15	0.3	0.3	0.3	—
Number of instructions	50	109	8	8 types	19
Number of registers	7	9	8	8	1
$\mu$ programmed	Yes	Yes	No	No	Yes
Fixed-point Arithmetic (+, -, X, $\div$ )					
Implementation (binary, BCD); (std, opt)	Binary	Binary	Software	Software subroutines	Microprogrammed
<b>MEMORY</b>					
Types — (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	pMOS	pMOS	Bipolar	NA	Bipolar
Word size, bits	8	8	16	NA	4, 8
Capacity, words	4K	16K	512 8-bit	NA	32 to 1K
Cycle time, $\mu$ sec	5	4	70	NA	0.05
<b>RAM (std, opt)</b>					
Technology	pMOS	pMOS	NA	Bipolar	Bipolar
Word size, bits	4	8	NA	16	1, 2, 4, 9
Capacity, words	4K	16K	NA	4K	4 to 1K
Cycle Time, $\mu$ sec	5	4	NA	60nsec	0.05
<b>PROM</b>					
Technology	EEROM (elec erasable)	EEROM (elec erasable)	Bipolar	NA	Bipolar
How programmed?	Microprocessor	Microprocessor	Fused link	NA	NI-CR Link
Word size, bits	8	8	8	NA	4, 8
Capacity, words	256	256	512 8-bit	NA	32 to 512
Cycle time, $\mu$ sec	—	PPS compatible	70	NA	0.05
<b>INPUT/OUTPUT</b>					
I/O word size, bits	4	8	2 to 8	1 to 8	9
Number of device addresses	—	—	512	512	1
Programmed I/O	Yes	Yes	Yes	Yes	—
Direct Memory Access	No	Yes	No	No	—
Type of interrupt system	None	Vectored	Software emulation	Software emulation	Priority
I/O rate, wds/sec	100K	125K	250-35K	200K-350K	—
Device interfaces available—(List)	Floppy disc controller; serial data controller; telecommunications data controller; parallel data controller; gp I/O; gp keyboard and display; keyboard and printer; printer controller; victor dot matrix printer	Floppy disc; serial data; telecommunications data; parallel data; gp I/O; GP keyboard and display; keyboard and printer; victor dot matrix printer; display			All 7400, 8T, 74LS, 74S series devices; all TTL- compatible devices
<b>SOFTWARE</b>					
Assembler	Yes	Yes	Yes	Yes	Micro assembler
Cross assembly (what system?)	IBM 370, GE	370, GE, Tymshare	FORTRAN source	FORTRAN source	—
Simulators (For what)	Hardware/software	Hardware/software	No	Hardware simulation	—
Languages	Assembly	Assembly	—	—	—
Operating System	ROM resident	ROM resident	—	Yes	—
Software (bundled?)	Yes	Yes	No	No	—
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	Yes	No	No	Yes
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	Communication concentrators	Communication concentrators	Data communication controller, mux and concentrator	Data communication controller, mux and concentrator	Electronic games; peripheral equipment; communications
First Delivery	1973	1975	1975	1975	7/75
Number delivered	Over 1 million	Thousands	100 +	12	—
<b>STANDARD SYSTEM</b>					
	With 1K words ROM/ 1K words RAM	With 1K ROM in 100-unit quantities; 1K RAM	With 1K words ROM	With 1K words RAM	With 1K words ROM
<b>PRICE, \$</b>	51/71 (Qty of 100)	68.50/108.50 (100 qty)	505 (for qty 1)	4895 (for qty 1)	20
<b>Other Features</b>	All modular LSI, no TTL required; smart I/O's contain address information so that I/O polling is not required after interrupt occurs; DMAC controls up to 8 blocks of data on a priority basis	All modular LSI, no TTL required; smart I/O's contain address info so that I/O polling is not required after interrupt occurs; DMAC controls up to 8 blocks of data on priority basis	Control-oriented, 1-board system with expandable I/O interface	MCSIM is real-time in- circuit simulation of SMS microcontroller systems. Programs are checked and verified in users environment	Multibus structure; masking capability; non-destructive data testing; zero detection; carry look ahead operation

# SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Signetics	Signetics	Texas Instruments	Texas Instruments	Texas Instruments
Model Number	N 3002	2650PC1001	TMS 1000	TMS 1200	8080
<b>PHYSICAL PACKAGE</b>					
Number of boards	—	1	1-chip	—	—
Dimensions	—	6 x 8	—	—	—
Number of chips	—	43	1	1	1
Number of pins/chip	28	16 to 40	8	40	40
Power Supply (std, opt)	5 Volts	No	No	No	Opt
Console (std, opt)	—	No	No	No	No
Cabinet (std, opt)	—	No	No	No	No
<b>PROCESSOR</b>					
Manufacturer	Signetics	Signetics	TI	TI	TI
Model Number	N3002	2650	TMS 1000	TMS 1200	8080
Technology Used (n/pMOS, bipolar)	Schottky bipolar	nMOS	pMOS	pMOS	nMOS
Word size	—	—	—	—	—
Data, bits	2 <sup>n</sup>	8	4	4	8
Instruction, bits	7 minimum	18, 16, 24	8	8	8, 16, 24
Clock frequency, KHz	222,000	1000	400	400	3000-2080
Add Time, reg to reg, $\mu$ sec	0.3	6.0	72 (mem-mem)	72 (mem-mem)	1.3-2
Number of instructions	40 +	75	43	43	78
Number of registers	11	7 GP, 2 status, 8 RAS	1 accumulator	1 accumulator	7 GP
$\mu$ programmed	Yes	No	Yes*	Yes*	No
Fixed-point Arithmetic (+, -, X, $\div$ )	—	—	—	—	—
Implementation (binary, BCD): (std, opt)	Microprogrammed	Binary and BCD	Binary std	Binary std	Binary, BCD
<b>MEMORY</b>					
Types – (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	Bipolar	Bipolar	pMOS	pMOS	pMOS; nMOS; bipolar
Word size, bits	4, 8	8	4/8	4/8	8
Capacity, words	32 to 1K	1K	1024	1024	250-2K
Cycle time, $\mu$ sec	0.05	1.0	3	3	0.5-1.5
<b>RAM (std, opt)</b>					
Technology	bipolar	nMOS	pMOS	pMOS	pMOS, nMOS, CMOS, bipolar
Word size, bits	1, 2, 4, 9	8	4	4	1-4
Capacity, words	4 to 1K	1K	64	128	256-4K
Cycle Time, $\mu$ sec	0.05	1.0	3	3	1.5
<b>PROM</b>					
Technology	Bipolar	Bipolar	—	—	pMOS, nMOS, bipolar
How programmed?	NI-CR link	Fuse link	—	—	Fusible link, FAMOS
Word size, bits	4, 8	8	—	—	8, 4
Capacity, words	32 to 512	1K	—	—	250-2K
Cycle time, $\mu$ sec	0.05	1.0	—	—	0.50-1.5
<b>INPUT/OUTPUT</b>					
I/O word size, bits	2 <sup>n</sup>	8 or serial	4 in, 8 out	4 in, 8 out	8
Number of device addresses	Unlimited	256 or 4 x 8 or 2 serial	2"	213	—
Programmed I/O	Yes	Std	Yes, 11 bits	Yes, 13 bits	—
Direct Memory Access	Yes	Std	No	No	No
Type of interrupt system	Priority	Vectored	No	No	Vectored, 8-level
I/O rate, wds/sec	—	176KB	Programmed	Programmed	—
Device interfaces available - (List)	All 7400, 8T, 74LS, 74S, series devices; all TTL compatible devices	TTY RS232 8-bit parallel	TMS 6011 UART; FIFO (TMS 4024); linear circuits; display drivers	TMS 6011 UART; FIFO (TMS 4024); linear circuits; display drivers	—
<b>SOFTWARE</b>					
Assembler	Micro assembler	No	Yes	Yes	Resident
Cross assembly (what system?)	—	370 or PDP/11	GE, Tymshare, NCSS	GE, Tymshare, NCSS	FORTRAN IV
Simulators (For what)	—	2650 up	Target system	Target system	FORTRAN IV
Languages	—	FORTRAN IV	—	—	—
Operating System	—	No	No	No	Yes
Software (bundled?)	—	No	Yes	Yes	No
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	No	Yes	Yes	Yes
Commercial processing	Yes	No	Yes	Yes	Yes
Data acquisition	Yes	No	Yes	Yes	Yes
Terminals	Yes	No	Yes	Yes	Yes
Device controllers	Yes	No	Yes	Yes	Yes
Process control	Yes	No	Yes	Yes	Yes
Any others?	Electronic games; peripheral equipment; communications	Prototyping	Home appliances, liquid flow control metering	Home appliances, liquid flow control metering	Billing & accounting avionics
First Delivery	7/75	6/75	11/74	11/74	—
Number delivered	—	25	—	—	—
<b>STANDARD SYSTEM</b>					
	With 1K words ROM	With 1K ROM/1K RAM			
<b>PRICE, \$</b>					
	11	975/975	Single chip 10	Single chip 10	
Other Features	Multibus structure; masking capability; non-destructive testing of data; zero detection; carry look-ahead operation	Std ROM contains PIPBUG, a signetics debugging package			Intel 8080 second source

\*discouraged

\*discouraged



MANUFACTURER	Texas Instruments	Three Phoenix	Toshiba America	Toshiba America	Transitron Electronic Corp
Model Number	TMS 990/04	PTT 8000	TLCS-12 EX-2	TLC-12A EX1A	TDS/16
<b>PHYSICAL PACKAGE</b>					
Number of boards	NA, 1-chip	3	14 boards	13	Rack mount cabinet
Dimensions	—	14" x 5"	—	—	5.25 x 19 x 12
Number of chips	1	—	1 chip CPU	1	—
Number of pins/chip	64	—	42 pins	36	—
Power Supply (std, opt)	Opt	Std	Std	Std	Std
Console (std, opt)	Opt	—	Opt	Std	Std
Cabinet (std, opt)	Opt	—	Opt	Std	Std
<b>PROCESSOR</b>					
Manufacturer	TI	Intel	Toshiba	Toshiba	Transitron
Model Number	TMS 9900	8008	T3153	T3190	TMC-1601
Technology Used (n/pMOS, bipolar)	nMOS	pMOS	pMOS Si-Gate E/D	pMOS Si-Gate E/D	Bipolar (Schottky)
Word size					
Data, bits	16	8	12	16	16
Instruction, bits	16/32/48	8	12, 24	12, 24	16, 32, 48
Clock frequency, KHz	3000	4193.2	1000	1000	5000
Add Time, reg to reg, $\mu$ sec	4.6	—	10	10	0.4 incl memory fetch
Number of instructions	69	—	18	20	95
Number of registers	16	—	8 GP	8 GP	8 gen, 3 dedicated
$\mu$ programmed	No	—	Yes	Yes	Yes
Fixed-point Arithmetic (+, -, X, $\div$ )					
Implementation (binary, BCD), (std, opt)	Binary; hdwr/multiply divide std	—	Binary std	Binary std	Software BCD
<b>MEMORY</b>					
Types — (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	EROM	None	pMOS Si-Gate E/D	pMOS Si-Gate E/D	Bipolar
Word size, bits	16	—	128 x 4	512 x 8 or 1024 x 4	16
Capacity, words	32K	—	8.5K x 12/system	3.5 x 12/system	32K
Cycle time, $\mu$ sec	1.0	—	1	1.0	0.20
<b>RAM (std, opt)</b>					
Technology	nMOS	Std	pMOS Si-Gate E/D	pMOS Si-Gate E/D	Bipolar
Word size, bits	16	8	128 x 4	128 x 4	16
Capacity, words	58K	1K	4K x 12/system	4K x 12/system	32K
Cycle Time, $\mu$ sec	1.33	—	1	1	0.20
<b>PROM</b>	Opt	Opt	—	—	Opt
Technology	—	—	pMOS Si Gate	pMOS Si-Gate	Bipolar
How programmed?	PROM programmer opt	—	Electrical	Electrical	Fusible link
Word size, bits	16	8	512 x 4	512 x 4	16
Capacity, words	32K	3K	3.5K x 12/system	3.5 x 12/system	32K
Cycle time, $\mu$ sec	0.66	—	1.0	1	0.20
<b>INPUT/OUTPUT</b>					
I/O word size, bits	1-16	8	12	12	8 or 16
Number of device addresses	256	16	3K	3K	52
Programmed I/O	Yes	Yes	None	None	Yes
Direct Memory Access	Yes	Yes	Opt	Opt	Data channel
Type of interrupt system	8 vectored interrupts	None	8 priority levels	8 priority levels	Vectored 4-level
I/O rate, wds/sec	1.5M bps; 1M wds/sec	—	—	—	1M wds/sec
Device interfaces available—(List)	EIA RS232; TTL; 16 in, 16 out, EIA 16 in, 16 out; Async; Sync; ASR; KSR; TI 733, Model 913 video display, card reader, floppy disc; printer, PROM programmer, cartridge disc	—	TTY/CASHIO M-500/TEKTRO 4101 interface; PROM programming module; PTR; PTP; printer (Diablo); digital cassette; typewriter (IBM 735); analog input interfaces	TTY/CASHIO M-5000/TEKTRO 4010; PROM programming module; PTR; PTP (FACIT); digital cassette; typewriter (IBM 735); analog input interfaces	Paper tape reader, paper tape punch; card reader; serial printer; line printer; floppy disc; CRT; TTY
<b>SOFTWARE</b>					
Assembler	Yes	—	Yes	Yes	Yes
Cross assembly (what system?)	GE, NCSS, Tymshare	—	GE 635	GE 635 (TOSBAC 5600)	Tymshare
Simulators (For what)	TMS 9900 microprocessor	—	GE 635	GE 635 (TOSBAC 5600)	Tymshare
Languages	Assembler	—	Assembler	Assembler	N/A
Operating System	Yes	—	Yes	No	FLOS (Floppy disc)
Software (bundled?)	—	—	Yes	Yes	Priced separately
<b>APPLICATIONS</b>					
Replace Hard wired logic	Yes	No	Yes	—	Yes
Commercial processing	—	No	Yes	—	Yes
Data acquisition	Yes	Yes	Yes	—	Yes
Terminals	Yes	Yes	Yes	—	Yes
Device controllers	Yes	No	Yes	—	Yes
Process control	Yes	No	Yes	—	Yes
Any others?	Prototype development systems support for TMS 9900	—	Machine tool control; industrial robot instrumentation	System software development	Software development system for TMC/1601
First Delivery	1st quarter 1976	—	1974	1975	Fall/75
Number delivered	—	—	10K kits	1K kits	—
<b>STANDARD SYSTEM</b>	990/4 with 8K wds memory, 6 slot chassis, 20 amp power; programmer's panel and TI 733 ASR	With 1K words RAM	With 1K wds ROM/with 1K RAM	With 1K words ROM/with 1K words RAM	—
<b>PRICE, \$</b>	5,950	2500	2000/2350	1790/2140	—
Other Features	Prototyping system 16K-byte memory, Silent 700 ASR, and PROM kit	—	—	—	Hardware multiply/divide; RAM stack; real-time clock; software-diagnostics; editor; debugger subroutine library; 90 day warranty

# SPECIFICATION CHART – MICROCOMPUTERS – MICROPROCESSORS

MANUFACTURER	Transitron Electronic Corp	Warner & Swasey	Warner & Swasey	Warner & Swasey	Warner & Swasey
Model Number	TMC/1601	Comstar System 4	Comstar System 4A and 4B	Comstar System 8A	Comstar System 8D
<b>PHYSICAL PACKAGE</b>					
Number of boards	1	Depends on configuration	Depends on configuration	Depends on configuration	Depends on configuration
Dimensions	8 x 8"	4.5 x 4.5	4.5 x 4.5	4.5 x 4.5"	4.5 x 4.5"
Number of chips	40	—	—	Variable	Variable
Number of pins/chip	—	—	—	—	—
Power Supply (std, opt)	+5V	Opt	Opt	Opt	Opt
Console (std, opt)	—	Opt	Opt	Opt	Opt
Cabinet (std, opt)	—	Opt	Opt	Opt	Opt
<b>PROCESSOR</b>					
Manufacturer	Transitron	Intel	Intel	Warner & Swasey	Warner & Swasey
Model Number	—	4004	4040	M8-A	M8-D
Technology Used (n/pMOS, bipolar)	Bipolar (Schottky)	pMOS	pMOS	Bipolar	Bipolar
Word size	16	4	4	8	8
Data, bits	16, 32, 48	8, 16	8, 16	8-48	8-48
Instruction, bits	5000	5,185	5,185 & 8000	4000	8000
Clock Frequency, KHz	0.40 incl mem. fetch cycle	10.8	10.8, 7.0	2.75	1
Add Time, reg to reg, $\mu$ sec	95	46	60	114	114
Number of instructions	8 gen; 3 dedicated	16	24	32	256
Number of registers	Yes	No	No	Yes	Yes
$\mu$ programmed	Yes	No	No	Yes	Yes
Fixed-point Arithmetic (+, -, X, $\div$ )	Software BCD	Std	BCD std	Firmware	Firmware
Implementation (binary, BCD); (std, opt)					
<b>MEMORY</b>					
Types — (ROM/RAM/PROM)					
<b>ROM</b>					
Technology (n/pMOS, bipolar)	Opt	—	—	nMOS	nMOS
Word size, bits	Bipolar	—	—	8	8
Capacity, words	16	—	—	64K	64K
Cycle time, $\mu$ sec	32K	—	—	0.5	0.5
RAM (std, opt)	0.20	—	—	Opt	Opt
Technology	Bipolar	Opt	Opt	nMOS & CMOS	nMOS & CMOS
Word size, bits	pMOS and CMOS	pMOS and CMOS	pMOS and CMOS		
Capacity, words	16	4	4	8	8
Cycle Time, $\mu$ sec	32K	2.5K	10.24K	64K	64K
PROM	0.20	10.8	10.8 & 7.0	0.5 & 0.75	0.375, 0.5 & 0.75
Technology	Bipolar	pMOS	pMOS	nMOS	nMOS
How programmed?	Fusible link	Opt programming device	Opt programming device	Opt programming device	Opt programming device
Word size, bits	16	8	8	8	8
Capacity, words	32K	4K	8K	64K	64K
Cycle time, $\mu$ sec	0.20	10.8	10.8 & 7.0	0.5	0.5
<b>INPUT/OUTPUT</b>					
I/O word size, bits	8 or 16	4	4	8	8
Number of device addresses	64	64	64	256	256
Programmed I/O	Yes	Yes	Yes	Yes	Yes
Direct Memory Access	Yes (data channel)	No	No	Multiport RAM	Multiport RAM
Type of interrupt system	Vectored 4-level	—	16 priority levels	7-level	7-level
I/O rate, wds/sec	1M wds/sec	11.5K	11.5K & 17.8K	2M	2M
Device interfaces available - (List)	Paper tape reader; paper tape punch; card reader; serial line printer; floppy disc; CRT tele-type	Line printer; paper tape reader and punch; mag tape cassette; mag tape xport; floppy disc; card reader; A/N display; TTY; RS-232C; analog, digital and power switching interface modules	Line printer; paper tape reader/punch; mag tape xport; floppy disc; card reader; AN display; TTY; RS-232C; analog, digital and power switching interface modules; mag tape cassette	Line printer; paper tape reader/punch; mag tape cassette; floppy disc; card reader; A/N display; LED display; RS-232C or 20 MA TTY current loop thumbwheel switches; serial data comm	Line printer; paper tape reader/punch; mag tape cassette; floppy disc; card reader; A/N display; LED display; RS-232C or 20 MA TTY current loop thumbwheel switches; serial data comm
<b>SOFTWARE</b>					
Assembler	Yes	No	No	No	No
Cross assembly (what system?)	Tymshare	ANSI FORTRAN IV	ANSI FORTRAN IV	ANSI FORTRAN IV	ANSI FORTRAN IV
Simulators (For what)	Tymshare	No	No	No	No
Languages	N/A	Comstar Process	Control compiler	FORTRAN	FORTRAN
Operating System	FLOS (floppy disc)	No	No	Yes	Yes
Software (bundled?)	Priced separately	No	No	Yes	Yes
<b>APPLICATIONS</b>					
Replace Hard-wired logic	Yes	Yes	Yes	Yes	Yes
Commercial processing	Yes	No	No	No	No
Data acquisition	Yes	Yes	Yes	Yes	Yes
Terminals	Yes	Yes	Yes	Yes	Yes
Device controllers	Yes	Yes	Yes	Yes	Yes
Process control	Yes	Yes	Yes	Yes	Yes
Any others?	Yes	Control applications for industrial automation; machine tool control; traffic control	Control applications for industrial automation; machine tool control; traffic control; material handling	Machine tool, traffic, and industrial computer control; data entry and retrieval; material handling control	Machine tool, traffic, and industrial computer control; data entry and retrieval; material handling control
First Delivery	Fall/75	2/72	3/75; 4/75	5/75	7/75
Number delivered	—	1200	40; 10	—	—
<b>STANDARD SYSTEM</b>					
		With 1K words RAM	With 1K words RAM	CPU; real-time clock; 1K RAM; power supply; monitor/control	CPU; real-time clock; 1K RAM; power supply regulators; monitor/control unit
PRICE, \$	—	1200	1200	2000	2300
Other Features	Hardware multiply/divide; RAM stack; real-time clock; software diagnostics; editor; debugger; subroutine library; 90 day warranty	114 I/O modules available incl clocks, modems, timers; Machine language and process control programming equipment; self teaching educator; diagnostic and test equipment	114 I/O modules available includes clocks, timers, modems; machine lang and process control lang; programming equipment; self-teaching educator and complete diagnostic and test equipment	Std system also includes 64 TTL inputs, 32 outputs, cabling; multiply/divide; commercial and wide temp versions available	Std system also includes 64 TTL inputs, 32 outputs, cabling; multiply/divide; commercial and wide temp versions; overflow and floating pt arith



<b>MANUFACTURER</b>	Western Digital	Wintek
Model Number	MCP 1600	W6800
<b>PHYSICAL PACKAGE</b>		
Number of boards	1	Variable
Dimensions	8 x 10	5.75" x 6"
Number of chips	—	Variable
Number of pins/chip	—	—
Power Supply (std, opt)	—	Std
Console (std, opt)	—	Opt
Cabinet (std, opt)	—	Opt
<b>PROCESSOR</b>		
Manufacturer	Western Digital	Motorola
Model Number	MCP 1600	M6800
Technology Used (n/pMOS, bipolar)	nMOS	nMOS
Word size		
Data, bits	8; 16	8
Instruction, bits	16	8
Clock frequency, KHz	3300	100
Add Time, reg to reg, $\mu$ sec	2.1 (16-bits)	2
Number of instructions	84	72
Number of registers	26	Two 8-bit; three 16-bit
$\mu$ programmed	Yes	No
Fixed-point Arithmetic (+, -, X, $\div$ )		
Implementation (binary, BCD); (std, opt)	Microprogrammable	Opt
<b>MEMORY</b>		
Types — (ROM/RAM/PROM)		
<b>ROM</b>		
Technology (n/pMOS, bipolar)	nMOS	—
Word size, bits	8	—
Capacity, words	1K	—
Cycle time, $\mu$ sec	0.3	—
RAM (std, opt)		Static; dynamic
Technology	nMOS	nMOS
Word size, bits	4	8
Capacity, words	256	4K bytes/module; 8K bytes/module
Cycle Time, $\mu$ sec	0.3	0.65; 0.35
<b>PROM</b>		
Technology	—	MOS, eROM
How programmed?	—	1702A programmer
Word size, bits	—	8
Capacity, words	—	2K bytes/module
Cycle time, $\mu$ sec	—	1.5
<b>INPUT/OUTPUT</b>		
I/O word size, bits	16	8
Number of device addresses	65K	Variable
Programmed I/O	Yes	Std
Direct Memory Access	Yes	Opt
Type of interrupt system	4 priority levels	Vectored (opt)
I/O rate, wds/sec	—	1M
Device interfaces available— (List)	Serial communications; floppy disc controller available 1/75	Std I/O and mass memory devices
<b>SOFTWARE</b>		
Assembler	Yes, Tymshare	—
Cross assembly (what system?)	PDP 11 & PDP 10	Tymshare
Simulators (For what)	Micro level	Tymshare
Languages	Assembly	PL/1 (2nd qtr 76)
Operating System	Yes	—
Software (bundled?)	No	—
<b>APPLICATIONS</b>		
Replace Hard-wired logic	Yes	Yes
Commercial processing	Yes	—
Data acquisition	Yes	Yes
Terminals	Yes	—
Device controllers	Yes	—
Process control	Yes	Yes
Any others?	Emulation of existing sets; data base compu- tations; minicomputer applications	Custom hardware and applications
First Delivery	—	9/75
Number delivered	—	—
<b>STANDARD SYSTEM</b>	With 1K words ROM	With 1K wds ROM/ with 1K wds RAM
<b>PRICE, \$</b>	250 (over 100)	1900/1600
Other Features	Microprogrammable to allow 3 levels of applica- tion. 1) emulation; 2) fast micro level control- lers; 3) miniprocessor	For custom applications



# SPECIFICATION CHART

## CENTRAL PROCESSORS AND WORKING STORAGE A—D

AUERBACH Buyer's Guide to . . .  
MINICOMPUTERS

SYSTEM IDENTITY	Cincinnati Melacron CIP/2100	Cincinnati Melacron CIP/2200	Computer Automation Naked/LSI and Naked Mini/LSI	Computer Automation Naked/LSI and Naked Milli/LSI	Computer Automation LSI Mega Bytes
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	2 bytes/word 16 Byte 88 3 1 64 8, 16, 24, + 32 NA NA NA — — — 4.3 Opt 1 msec Yes 768 NA NA NA NA IPL	2 bytes/word 16 Byte 119 3 1 64 8, 16, 24 + 32 11.7 614.9 (16 dec digits) — Opt Opt — 4.3 Opt 1 msec Yes 1536 NA NA NA NA IPL	2/10, 2/20 Word/byte 16 Byte/word 188 2 1 5-256 16 4.12/2.06* 14.84, 15.1 24.3/12.4* Subroutine Subroutine Subroutine 4.8 Opt 0.1, 1.0, 10 KHz Yes NA NA NA NA * 300/150 Bootstrap & binary loader	3/05 Word/byte 16 Byte/word 95 2 1 1-unlimited 16 6.0 Subroutine Subroutine — — — 4.8 100, 120 Hz Yes Yes NA NA NA 250 Bootstrap & binary loader	2/60 Word/byte 16 Byte/word 224 4 1 5-256 16 2.06 14.84 12.44 Subroutine Subroutine — 4.8 Opt 0.1/1.0/10 KHz Yes NA NA NA 150 Bootstrap & binary loader
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core 1 8K/32K 1.1 No — — Parity opt Opt NA No — — Byte I/O, Serial I/O 8 32 25K-86K, 10 Yes 8 32 910K Firmware, multiplexed I/O	Core 1 4K/32K words 1.1 No — — Parity opt — No No — — Byte, Serial 8 25K-86K, 10 Yes 32 910K Firmware, multiplexed I/O	RAM, ROM, PROM; Core, EPROM 1 512/512K 0.98, 1.2 Yes — 1.2, .85 Parity opt No No — — Yes 16 248 130K (via regs); 20K (via memory) Yes 16 16 248 1.17M (1.67M with interleaved memory) DMC, 75-82K, B I/O 450K	RAM, ROM, PROM, Core, EPROM 1 512/512K .98, 1.2 Yes NA 1.2, .85 Parity No No — — Yes 16 248 40K Yes 16 2-64 1.17M (1.67M with interleaved memory) DMC, 40K	RAM, ROM, PROM, Core, EPROM 1 16K/1M .98, 1.2 Yes NA 1.2, .85 Parity opt No No — — Yes 16 248 130K (via regs); 90K (via memory) Yes 16 2-64 1.17M (1.67M with interleaved memory) DMC, 82K, Block I/O 450K
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	PTOS (Paper Tape) CIMOS-22 Job Control; relocating assembler, RPG II NA — 5M/10M — — 7/9 trk; 800 bpi Yes 80-col, 96-col — 60 lpm-200 lpm Async, sync To 2,400 bps, to 9,600 bps	CIMOS (disc based) PTOS Job Control; Relocating Assembler, RPG II NA — 5M bytes High density 7/9 trk; 800 bpi Yes 80-col, 96-col — 60 lpm - 200 lpm Async, sync To 2,400 bps, to 9,600 bps	RTX, DOS, MTOS, FDOS BETA, BASIC, FORTRAN IV, RELO ASSEMBLER, Macro ASSEMBLER NA — 2.46M wd/drive — 1.2M/drive 9-trk, 800 bpi, 25 ips 520K 285 cpm reader 300 cps reader; 75 cps punch 100 cps (60-150 lpm) 80-col Async, sync 75-12.2K bps	RTX (real-time) RELO ASSEMBLER NA — 1 fixed, 1 removable, 2.46M wd/drive — 1.2M/drive 9-trk, 800 bpi, 25 ips 520K 285 cpm reader 300 cps reader, 300 cps/75 punch 100 cps (80-col) Async, sync 75-19.2K bps	DOS, MTOS, RTX, FDOS FORTRAN IV, BASIC, RELO, ALGOL, ASSEMBLER, Macro ASSEMBLER NA — 1 fixed, 1 removable, 2.46M wd/drive — 1.2M/drive 9-trk, 800 bpi, 25 ips Single/dual cassette drives, 520K 285 cpm reader 300 cps reader, reader/punch 100 cps (80-col) Async, sync 75 to 19.2K bps
<b>COMMENTS</b> — - Not Applicable NA - Information Not Available			* First Time is for 2/10 CPU Second Time is for 2/20 CPU		

# SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE A—D

SYSTEM IDENTITY	Computer Signal Processors CSP 30	Computer Signal Processors CSP-125	Control Data 1700	Control Data 1700	Control Data SC 1700
<b>CENTRAL PROCESSOR</b>	CSP 30	Computer Signal Processors CSP-125	Control Data 1700	Control Data 1700	Control Data SC 1700
Data Format	Byte/word	Byte/wd	1704	1714	1774
Word Size, bits	16	16	2 bytes/wd 16 bit + parity + protect	2 bytes/wd 16 bit + parity + protect	2 bytes/wd 16 bit + parity + protect
Address Orientation	—	—	Wd	Wd	Wd
No. of Machine Instr.	212	212	196	196	196
No. of Program Registers	32	32	5	5	5
No. of Addresses/Instr.	1	1	1	1	1
No. of Interrupt Levels	8.57	8.57	16	16	16
Instruction Length, bits	16, 32, 112	16	16	16	16
Execution Times, $\mu$ sec					
Add/Subtract	.250	.250	2.0	2.0	2.0
Multiply	1.250	1.250	6.0	6.0	13.0
Divide	—	—	8.0	8.0	20.0
Floating Add/Sub	—	—	—	—	—
Floating Multiply	—	—	—	—	—
Floating Divide	—	—	—	—	—
Max. Precision, Decimal Digits	4.3	4.3	4.3	4.3	4.3
Real Time Clock Resolution	—	—	No	No	No
Control Memory Size, wds (min/max)	No	No	No	No	No
Word Length, bits	—	—	—	—	—
Cycle Time, nsec	—	—	—	—	—
Processor Cycle Time, $\mu$ sec	125	125	—	—	—
APL	Bootstrap	Bootstrap	Bootstrap loader	Bootstrap loader	Bootstrap loader
<b>WORKING STORAGE</b>	Core; I.C.	Bipolar; core	Mag core	Mag core	Mag core
Technology	Core; I.C.	Bipolar; core	Mag core	Mag core	Mag core
No. of Ports	—	—	2	2	2
Main Memory Capacity, (min/max, bytes)	4K-128K	1K/32K bipolar; 128K core	8K-64K	48K-132K	8K-64K
Core Cycle Time, $\mu$ sec	.9	.900	1.1	1.1	1.5
Solid State Memory	Bipolar	—	—	—	—
Real Time, $\mu$ sec	—	—	—	—	—
Cycle Time, $\mu$ sec	—	—	—	—	—
Error Control	No parity	No parity	Parity std	Parity std	Parity std
Memory Protect	No	No	Std	Std	Std
Memory Management	—	—	—	—	—
Cache Memory	No	No	No	No	No
Size, (min/max, wd)	—	—	—	—	—
Cycle Time, $\mu$ sec	—	—	—	—	—
<b>I/O CHANNELS</b>					
PIO	Yes	Yes	Yes, called AQ	Yes, called AQ	Yes, called AQ
Width, bits	16	16	16	16	16
No. of Devices	4.32	4.32	8/AQ channel	8/AQ channel	8/AQ channel
Max Xfer Rate, bytes/sec	380,000	380,000	Software dependent	Software dependent	Software dependent
DMA	Yes	16	Called DSA; 1 std, 1 opt	Called DSA; 1 std, 1 opt	Called DSA; 1 std, 1 opt
Width, bits	16	16	8/DSA channel	8/DSA channel	8/DSA channel
No. of Devices	0-8	0-8	—	—	—
Max Xfer Rate, bytes/sec	1.4M; 3.3M core; 10M bipolar	1.4M; 3.3M (core), 10M (bipolar)	0.9M	0.9M	0.67M
Other (type; xfer rate, bytes/sec)	—	—	—	—	—
<b>SOFTWARE</b>					
Types of Op. Sys.	—	—	4K Assembly, Utility, Mass Storage OS	4K Assembly, Utility, Mass Storage OS	4K Assembly, Utility, Mass Storage OS
Languages	Ansi; FORTRAN IV	Ansi, FORTRAN IV	Assembler, Macro Assembler, CDC Tape FORTRAN	Assembler, Macro Assembler, CDC Tape FORTRAN	Assembler, Macro Assembler, CDC Tape FORTRAN
Communications	—	—	None	None	None
<b>I/O DEVICES</b>					
Fixed-Head Discs (capacity, bytes)	512K-4M; 128K-1M	128K-4M	3.6M	3.6M	3.6M
Disc Cartridges (capacity, bytes)	—	—	4.4M	4.4M	4.4M
Disc Pack (capacity, bytes)	—	—	—	—	—
Floppy Discs (capacity, bytes)	—	—	—	—	—
Magnetic Tape (type)	9-trk, 800 bpi	800/900 bpi; 75-125 ips	7.5-50Kb (7/9-trk)	7.5-50Kb (7/9 trk)	7.5-50Kb (7/9 trk)
Cassettes (capacity, bytes)	—	—	—	—	—
Punched Card (type; speed cpm)	—	—	300 cpm read; 500 read/460 punch	330 cpm read; 500 read/460 punch	330 cpm read; 500 read/460 punch
Paper Tape (type; speed cps)	—	—	10-120 cps	10-120 cps	10-120 cps
Printers (speed, lpm; col)	356-1,100 lpm, 80 or 132 col	356-1,100 lpm; 80-132 col	300-1,000 lpm	300-1,000 lpm	300-1,000 lpm
Data Comm	—	—	—	—	—
Xmission Rates	—	—	60-40,800 bps	60-40,800 bps	60-40,800 bps
<b>COMMENTS</b>			No longer in production	No longer in production	No longer in production
— - Not Applicable NA - Information Not Available					

— - Not Applicable  
NA - Information Not Available





SYSTEM IDENTITY	Control Data System 17	Data General Eclipse S/100	Data General Eclipse S/200	Data General Nova	Data General Nova 2
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	1784-1; 1784-2 2 bytes/wd 16 + 1 parity + 1 memory protect — 196 8 1 16 16 1.2; 1.8 5.4; 3.6 7.2; 4.8 3.3-11.5 14-15 18-19 4.3 — — None — — — — —	— Wd/2 bytes 16 Byte 86 std, 66 opt 8 1 16 hardware 16 0.6 7.2 9.6 2.4 (opt) 3.9 (opt) 4.6 (opt) 4.3 Yes 10 Hz, 100 Hz, 1,000 Hz ROM; WCS NA; 0/256 56; 56 NA NA Yes	Wd/2 bytes 16 Byte 86 std, 66 opt 8 1 16 hardware 16 0.6 7.2 9.6 2.4 4.6 3.9 4.3 Yes 10 Hz, 100 Hz, 1,000 Hz ROM; WCS NA; 0/256 56; 56 NA NA Yes	Wd/2 bytes 16 — 202 4 1 16 16 5.9 11.1 11.9 17.8/17.8 20.9 24.1 4.3 Opt 10; 100; 1,000 Hz No — — — NA NA	Nova 2/4, 2/10 2 bytes/wd 16 Byte wd 202 4 1 16 16 0.8 8.8 8.8 7.55/8.15 11.7 14.5 4.3 Yes 10 Hz, 100 Hz or 1,000 Hz No — — — NA NA
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wds) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	MOS 1 8K/132K — MOS — 0.9/0.6 Parity Manual switches, protect bit Software No — — Called AQ 16 8/channel Software dependent Called DSA 16 8 std; 8 opt 1.1M; 1.6M wd —	MOS; Core — 32K-128K 0.8 (core) MOS — 0.7 ERCC opt No No Bipolar 16 0.2 Yes 16 59 Std 16 59 2.5M —	MOS; core 1 64K/256K 0.8 (core) MOS — 0.7 ERCC opt Opt (dual user memory maps, 1 data channel mgs) Yes Bipolar 16 0.2 Yes 16 59 Std 16 59 2.5M —	Core — 2K/64K 2.6 No NA NA No parity No No No NA NA Yes 16 62 570K —	Core 1 8K-64K 0.8; 1.0 No NA NA No parity No No No NA NA Yes 16 59 2.5M —
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	Mass Storage Operating Sys FORTRAN, AUTRAN, Assemblers, Draft & BASIC IMPORT (Remote Batch), Message Switching Drum 393K to 3.1M; avg access 8 msec 4.4M-8.8M; avg access 110 msec — — 7/9 trk; 556-1,600 bpi; 25/50 ips Reader 250-1,600 cpm (80/51 col); Pnch 100-400 cpm 400 cps read; 120-150 punch; ctrl for Facit Addio reader/punch 300-1,200 lpm Sync/async; RS232C/CCITT V24 1,200-19,200/110-9,600 baud	RDOS; MRDOS; RTOS; SOS FORTRAN IV, FORTRAN V; ALGOL, BASIC, Assemblers NA 128K-524K 2.4M-5.0M 6M-24M — 556/800/1,600 bpi; 7/9 trk; 12.5-75 ips 1,600 bpi 225-1,000 cpm reader 63.3 cps punch; 300 cps reader 356 lpm (80-col); 165,235 lpm (132-col) Sync, async 50-9,600 baud	RDOS; MRDOS; RTOS; SOS FORTRAN IV, FORTRAN V, ALGOL, BASIC, Assemblers NA 128K-1.4M 2.5M-5.9M 6M-24M — 556/800/1,600 bpi; 7/9 trk; 12.5-75 ips Yes 225-1,000 cps reader 400 cps reader; 63.3 cps punch 165-356 lpm; 80/132 col Sync, async 50-9,600 baud	DOS, RDOS, SOS, RTOS FORTRAN, ALGOL, BASIC, Assembler NA 128K-1.5M 2.5M-5M 6M-24.5M — 556/800 bpi; 7/9 trk; 12.5-75 ips 1,600 bps 225-1,000 cps reader 63.3 punch; 300 cps reader 356 lpm; 245 lpm; 165 lpm Sync, async 50-9,600 baud	RDOS; RTOS; SOS FORTRAN, ALGOL, BASIC, Assemblers 2780 RJE emulation 128K-1.5M 1.2/2.4M — NA 7/9 trk; 12.5/45/75 ips; 556/800 bpi 1,600 bps 225-1,000 cpm reader 300 cps reader; 63.3 punch 356/245 lpm (80-132 col) Async, sync 50-9,600 baud
<b>COMMENTS</b> — Not Applicable NA Information Not Available	CDC provides process control, data acquisition, testing, graphics, OCR applications software; also provides for remote ctrlr for over 100 process I/O		Basis of C300 commercial system	No longer marketed	Commercial software package available as well as Dataprep; Dataplot

# SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE A-D

SYSTEM IDENTITY	Data General Nova 800/820/800 Jumbo	Data General Nova 830	Data General Nova 840	Data General Nova 1200, 1230	Data General Nova 1210, 1220
<b>CENTRAL PROCESSOR</b>					
Data Format	2 bytes/wd	2 bytes/wd	2 bytes/wd	2 bytes/wd	2 bytes/wd
Word Size, bits	16	16	16	16	16
Address Orientation	Wd	Wd	Wd	Wd	Wd
No. of Machine Instr.	202	202	202	202	202
No. of Program Registers	4	4	4	4	4
No. of Addresses/Instr.	1	1	1	1	1
No. of Interrupt Levels	16	16	16	16	16
Instruction Length, bits	16	16	16	16	16
Execution Times, $\mu$ sec					
Add/Subtract	0.8	1.0/1.0	0.8/0.8	1.35/1.35	1.35
Multiply	8.8	8.8	8.8	3.75	3.75
Divide	8.8	8.8	8.8	4.05	4.05
Floating Add/Sub	7.6/8.2	7.6/8.2	7.6/8.2	9.5/9.5	9.5/9.5
Floating Multiply	11.7	11.7	11.7	13.5	13.5
Floating Divide	14.5	14.5	14.5	16.8	16.8
Max. Precision, Decimal Digits	4.3	4.3	4.3	4.3	4.3
Real-Time Clock Resolution	Opt 10 Hz, 100 Hz, 1,000 Hz	Opt 10 Hz, 100 Hz, 1,000 Hz	Opt 10 Hz, 100 Hz, 1,000 Hz	Opt 10 Hz, 100 Hz, 1,000 Hz	Opt 10 Hz, 100 Hz, 1,000 Hz
Control Memory Size, wds (min/max)	No	No	No	No	No
Word Length, bits	—	—	—	—	—
Cycle Time, nsec	—	—	—	—	—
Processor Cycle Time, $\mu$ sec	NA	NA	NA	NA	NA
APL	Opt	Opt	Opt	Opt	Opt
<b>WORKING STORAGE</b>					
Technology	Core	Core	Core	Core	Core
No. of Ports	—	—	—	—	—
Main Memory Capacity, (min/max, bytes)	2K/64K	1K/128K	To 128K wd	1K/32K wd	1K/24; 32K wd
Core Cycle Time, $\mu$ sec	0.8	1	0.8	1.2	1.2
Solid State Memory	No	No	No	No	No
Real Time, $\mu$ sec	—	—	—	—	—
Cycle Time, $\mu$ sec	—	—	—	—	—
Error Control	No parity	No parity	No parity	No parity	No parity
Memory Protect	Opt	Opt	Std	—	—
Memory Management	Opt	Opt	Std	—	—
Cache Memory	No	No	No	No	No
Size, (min/max, wd)	—	—	—	—	—
Cycle Time, $\mu$ sec	—	—	—	—	—
<b>I/O CHANNELS</b>					
PIO	Yes	Yes	Yes	Yes	Yes
Width, bits	16	16	16	16	16
No. of Devices	62	62	62	62	62
Max Xfer Rate, bytes/sec	—	—	—	—	—
DMA	Yes	Yes	Yes	Yes	Yes
Width, bits	16	16	16	16	16
No. of Devices	62	62	62	62	62
Max Xfer Rate, bytes/sec	2.5M	2.5M	2.5M	1.7M	1.7M
Other (type; xfer rate, bytes/sec)	—	—	—	—	—
<b>SOFTWARE</b>					
Types of Op. Sys.	DOS, RDOS, SOS, RTOS	DOS, RDOS, SOS, RTOS	DOS, RDOS, SOS, RTOS	DOS, RDOS, SOS, RTOS	DOS, RDOS, SOS, RTOS
Languages	FORTRAN, ALGOL, BASIC, Assembler	FORTRAN, ALGOL, BASIC	FORTRAN, ALGOL, BASIC	FORTRAN, ALGOL, BASIC	FORTRAN, ALGOL, BASIC
Communications	NA	—	—	—	—
<b>I/O DEVICES</b>					
Fixed Head Discs (capacity, bytes)	128K-1.5M	128K-1.5M	128K-1.5M	128K-1.5M	65K wd-786K wd
Disc Cartridges (capacity, bytes)	2.5M-5M	1.247M-2,494M wd	1.247M-2,494M wd	1.5M-5.0M	1.247M-2,494M wd
Disc Pack (capacity, bytes)	6M-24.5M	3M wd - 12,288M wd	3M wd-12,288M wd	6M-24.5M	3M wd-12,288M wd
Floppy Discs (capacity, bytes)	—	—	—	—	—
Magnetic Tape (type)	556/800 bpi, 7/9 trk	556/800 bpi, 7/9 trk	556/800 bpi, 7/9 trk	556/800 bpi, 7/9 trk	556/800 bpi, 7/9 trk
Cassettes (capacity, bytes)	1,600 bps, speed	1,600 bps	1,600 bps	1,600 bps	1,600 bps
Punched Card (type; speed cpm)	225-1,000 cps reader	225-1,000 cps reader	225-1,000 cps reader	225-1,000 cps reader	225-1,000 cps reader
Paper Tape (type; speed cps)	63.3 punch 300 cps reader	63.3 punch, 300 cps reader	63.3 punch, 300 cps reader	63.3 punch, 300 cps reader	63.3 punch, 300 cps reader
Printers (speed, lpm; col)	356 lpm, 245 lpm, 165 lpm, 80/132 cols	356 lpm, 245 lpm, 165 lpm, 80/132 cols	356 lpm, 245 lpm, 165 lpm, 80/132 cols	356 lpm, 245 lpm, 165 lpm, 80/132 cols	356 lpm, 245 lpm, 165 lpm, 80/132 cols
Data Comm	Async, sync	Async, sync	Async, sync	Async, sync	Async, sync
Xmission Rates	50-9,600 baud	50-9,600 baud	50-9,600 baud	50-9,600 baud	50-9,600 baud
<b>COMMENTS</b>					
— - Not Applicable NA - Information Not Available					



SYSTEM IDENTITY	Data General Supernova	Data General Supernova SC	Digital Computer Controls D-112; D 112H	Digital Computer Controls D-112SC	Digital Computer Controls D-116 Series
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	2 bytes/wd 16 Wd 202 4 1 16 16 0.8 3.8/ 6.9 9.4/9.4 12.5 15.7 4.3 Opt 10; 100; 1,000 Hz No -- -- 800 nsec Std	2 bytes/wd 16 Wd 202 4 1 16 16 0.3 3.7 6.8 9.3/9.3 12.4 15.6 4.3 Opt 10 Hz, 100 Hz, 1,000 Hz No -- -- 300 nsec Std	6-bit bytes/wd 12 -- 56; 72 opt 6 1 16 12 -- -- -- Subroutine Subroutine Subroutine 3.2 Yes 10; 100; 1,000 Hz No -- -- NA Bootstrap loader	Wd/2; 6 bit bytes 12 -- 72 6 1 16 12 -- -- -- Subroutine Subroutine Subroutine 3.2 Yes 10; 100; 1,000 Hz No -- -- NA Bootstrap loader	116S, 116H Wd or byte 16 202 16 1 16 16 1.35; 1.0 3.75; 3.0 4.05; 3.2 -- -- -- 4.3 Opt 10-1,000 Hz No -- -- NA Opt
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core 32K wd 0.8 No -- -- No parity Opt -- No -- -- Yes 62 -- Yes 62 500K wd/sec --	Semiconductor 1K/32K wd 0.8 Yes NA NA No parity Opt -- No -- -- Yes 62 -- Yes 62 500K wd/sec --	Core 4K-32K 1.2; 0.9 No -- Parity opt Via ROM modules No No -- -- Yes 12 62-192 -- Opt 12 62-192 -- Data Break interface	Core, bipolar 4/32K 0.9, 0.2-0.3 (bipolar) NA NA NA Opt parity Via ROM No No -- -- Yes 12 62-192 -- Opt 12 62-192 -- Data Break interface	Core 1 4K/128K 1.20; 0.96 No -- -- No parity Opt Opt No -- -- Std 16 61 Software dependent Yes 16 61 1.67M
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	DOS, RDOS, SOS, RTOS FORTRAN, ALGOL, BASIC -- 128K-1.5M 2.5M-5.0M 6M-24.5M NA 556/800 bpi; 7/9 trk 1,600 bps 225-1,000 cps reader 63.3 punch; 300 cps reader 356 lpm, 245 lpm, 165 cps; 80/132 col Sync, async 50-9,600 baud	DOS, RDOS, SOS, RTOS FORTRAN, ALGOL, BASIC -- 128K-1.5M 2.5M-5.0M 6M-24.5M NA 556/800 bpi 7/9 trk 1,600 bps 225-1,000 cps reader 63.3 punch; 300 cps reader 356 lpm, 245 lpm, 165 lpm, 80/132 col Sync, async 50-9,600 baud	PDP-8 Compatible FORTRAN, Assembler, Compilers, ALGOL -- NA 3.2M NA NA (7/9 trk) 200-800 bpi NA Optical mark reader Read 300, punch 50-100 cps 300 lpm Sync, async 110-10,000 baud	PDP-8 compatible -- 3.2M NA NA (7/9 trk) 200-800 bpi NA Optical mark reader Read 300 cps, punch 50-100 cps 300 lpm Sync, async 110-10,000 baud	MSOS; RTX FORTRAN IV, BASIC Interpreters; Assembler -- NA 2.4M, 4.8M 10M 156K 7/9 trk; 12.5/45/75 ips 250K bytes/cartridge 150 cpm punch; 300 cpm read 300 cps read; 110-50 cps punch 30/125/300 cps; 300 lpm, 80/132 col Sync, async 0-250K baud
<b>COMMENTS</b> -- Not Applicable NA Information Not Available	No longer marketed	No longer marketed	No longer actively marketed	No longer actively marketed	

# SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE A-D

SYSTEM IDENTITY	Digital Computer Controls D-216	Digital Computer Controls D-316	Digital Computer Controls D-416	Digital Computer Controls D-616	Digital Equipment PDP 8/A
<b>CENTRAL PROCESSOR</b>					
Data Format	Wd 16	Wd 16	Wd 16	Wd 16	Wd 12
Word Size, bits					
Address Orientation	Byte, wd	Byte, wd	Byte, wd	Byte, wd	Wd
No. of Machine Instr.	98	98	98	96 std, 16 opt	56
No. of Program Registers	12	12	12	12	5
No. of Addresses/Instr.	1	1	1	1	1
No. of Interrupt Levels	Multilevel	Multilevel	Multilevel	Multilevel	1
Instruction Length, bits	16	16	16	16	12
Execution Times, $\mu$ sec					
Add/Subtract	1.6	1.6	1.6	.66; 0.8	3.0
Multiply	NA	NA	NA	5.2-17.5	Future opt
Divide	NA	NA	NA	16.7-22.0	Future opt
Floating Add/Sub	NA	NA	NA	NA	Future opt
Floating Multiply	NA	NA	NA	NA	Future opt
Floating Divide	NA	NA	NA	NA	Future opt
Max. Precision, Decimal Digits	4.3	4.3	4.3	4.3	3.4
Real-Time Clock Resolution	Yes, plus interval timer 10 Hz, 100 Hz, 1,000 Hz; 10 KHz-160 KHz	Yes, plus interval timer 10 Hz, 100 Hz, 1,000 Hz; 10 KHz-160 KHz	Yes, plus interval timer 10 Hz, 100 Hz, 1,000 Hz; 10 KHz-160 KHz	Yes, plus interval timer 10 Hz, 100 Hz, 1,000 Hz; 10 KHz-160 KHz	Yes Fixed interval; program- mable
Control Memory					
Size, wds (min/max)	ROM 512	ROM 512	ROM 512	ROM, WCS 256-512, 256-1K	No
Word Length, bits	48	48	48	50	—
Cycle Time, nsec	0.2	0.2	0.2	0.2	—
Processor Cycle Time, $\mu$ sec	NA	NA	NA	NA	—
APL	Yes	Yes	Yes	Yes	Bootstrap loader
<b>WORKING STORAGE</b>					
Technology	MOS RAM/PROM/ROM	MOS RAM	Core	Core, MOS	MOS; core
No. of Ports	1	1	1	2	1
Main Memory Capacity, (min/max, bytes)	2K-32K; 256K*	8K-64K; 256K*	8K-64K; 256K*	8K-2M	2-64K (6-bit)
Core Cycle Time, $\mu$ sec	—	—	1.6	0.66; 0.8	1.5
Solid State Memory					
Real Time, $\mu$ sec	MOS 0.6	MOS 0.6	No NA	MOS —	MOS 2.3
Cycle Time, $\mu$ sec	1.6	1.6	NA	0.66	2.8
Error Control	No	Byte parity	No	Error checking and correcting (5 bits)	Parity opt
Memory Protect	Yes*	Yes*	Yes*	Yes*	Software or ROM
Memory Management	Yes	Yes	Yes	Yes	To 64K
Cache Memory	No	No	No	No	No
Size, (min/max, wd)	—	—	—	—	—
Cycle Time, $\mu$ sec	—	—	—	—	—
<b>I/O CHANNELS</b>					
PIO	Yes	Yes	Yes	Yes	Yes
Width, bits	16	16	16	16	12
No. of Devices	60	60	60	62	64
Max Xfer Rate, bytes/sec	Software dependent	Software dependent	Software dependent	Software dependent	Software dependent
DMA					
Width, bits	Std 16	Std 16	Std 16	Std (2 speeds) 16	Yes 12
No. of Devices	60	60	60	62	12
Max Xfer Rate, bytes/sec	1M	1M	1M	1.6M/3M	.666.7K (MOS); 1.7M (core)
Other (type; xfer rate, bytes/sec)					
<b>SOFTWARE</b>					
Types of Op. Sys.	RTX, MSOS, IRIS	RTX, MSOS, IRIS	RTX, MSOS, IRIS	RTX, MSOS, IRIS	OS-8; RTS-8; COS-300 CAPS-8, TS-8-E
Languages	BASIC, FORTRAN, COBOL	BASIC, FORTRAN, COBOL	BASIC, FORTRAN, COBOL	BASIC, FORTRAN, COBOL	BASIC, FORTRAN; Assemblers, FOCAL
Communications	—	—	—	—	Application pkg
<b>I/O DEVICES</b>					
Fixed-Head Discs (capacity, bytes)	—	—	—	—	—
Disc Cartridges (capacity, bytes)	2.4M-10M	2.4M-10M	2.4M-10M	2.4M-10M	64K-524K/drive
Disc Pack (capacity, bytes)	40M-80M	40M-80M	40M-80M	40M-80M	63.2M/drive
Floppy Discs (capacity, bytes)	256K	256K	256K	256K	256K/drive, avg access 483 msec
Magnetic Tape (type)	7/9 trk; 12.5-75 ips	7/9 trk; 12.5-75 ips	7/9 trk; 12.5-75 ips	7/9 trk; 12.5-75 ips	DE Ctape, 7/9 trk 200/ 556/800 bpi
Cassettes (capacity, bytes)	256K	256K	256K	256K	93K/drive, 560 bytes/sec
Punched Card (type; speed cpm)	150-300 reader; 100 cpm punch	150-300 cpm reader/ 100 cpm punch	150-300 cpm reader/ 100 cpm punch	150-300 cpm reader/ 100 cpm punch	300 cpm reader
Paper Tape (type; speed cps)	75 cps punch; 300 cps reader	75 cps punch/300 cps reader	75 cps punch/300 cps reader	75 cps punch; 300 cps reader	300 cps reader
Printers (speed, lpm; col)	80/132 col; 60-600 lpm	80/132 col; 60-600 lpm	80/132 col; 60-600 lpm	80/132 col; 60-600 lpm	165 cps (132-col); 173-356 lpm
Data Comm	Sync, async	Sync, async	Sync, async	Sync, async	Sync, async
Xmission Rates	To 19.2K baud	To 19.2K baud	To 19.2K baud	To 19.2K baud	To 1,200
<b>COMMENTS</b>					
	*With memory management	*With memory management	*With memory management	*With memory management	
— - Not Applicable NA - Information Not Available					

SYSTEM IDENTITY	Digital Equipment 8/E, 8/F, 8/M	Digital Equipment PDP-11/03; LSI-11	Digital Equipment PDP-11/04; 11/05; 11/10	Digital Equipment PDP-11/15; 11/20; 11R20	Digital Equipment PDP 11/35; 11/40
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	2 bytes (6-bit)/wd 12 Wd 56; 72 5 1 1 12 2.6/4.8 7.4/8.6 7.4/8.6 19.0 25.0 26.0 3.4 Yes, 3 Fixed interval; pro- grammable No — — NA Bootstrap loader	KDH-F 2 bytes/wd 16 Byte/wd 400 with variations on 70 basic 8 2 1 16, 32, 48 3.5(1) 12.0(2) 24.64(3) 78(3) 42 52-92 151 4.3 Yes NA Yes NA NA NA NA NA	KD11-B 2 bytes/wd 16 Byte/wd 70; 4 opt 8 2 5 int; 1 or 4 ext 16, 32, 48 3.4: 4.2 6.6; 7.5 7.4; 7.8 Subroutine Subroutine Subroutine 4.3 Yes 10KHz - 100 KHz Yes NA NA Bootstrap loader	KC11; KA11; KAR11 2 bytes/wd 16 Byte/wd 70; 4 opt 8 — 5 int; 1 or 4 ext 16, 32, 48 3.8 6.7 7.0 Subroutine Subroutine Subroutine 4.3 Yes 10KHz-100KHz No — NA NA NA Bootstrap loader	KD11-A 2 bytes/wd 16 Byte/wd 70; 10 opt 9 — 5 int; 4 ext 16, 32, 48 2.66 9.66 11.30 Subroutine Subroutine Subroutine 4.3 Yes 10KHz-100KHz Yes NA NA NA Bootstrap loader
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core 1 8K-64K (6-bit bytes) (min/max, bytes) 1.2; 1.4 (2 accesses) No NA — Parity opt Software or ROM To 32K wd No — — Yes 12 64 Software dependent Yes 12 1.7M —	Core, MOS 1 8K-64K (MOS) 0.64K core 1.2 Static/dynamic RAM; PROM/ROM .350 (RAM) 0.07/0.08 (ROM/PROM) — No No No — Yes 16 NA NA Yes Unlimited 1.67M Serial interface I/O, 50-9,600 baud	Core (11/OS, 11/10); MOS (11/04) 1 8K-56K .90; 0.98 MOS NA 0.73 Parity opt No No No No — Yes 16 Unlimited Program dependent Yes 16 Unlimited 2M —	Core 1 4K-28K .90 No — Parity opt No No No No — Yes 16 Unlimited Software dependent Yes 16 Unlimited 2M —	Core 1 8K-126K .90, .98 $\mu$ sec No — Parity opt Opt Yes, opt No — Yes 16 Unlimited Software dependent Yes 16 Unlimited 2M —
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	OS-8; RTS-8; COS 300; CAPS-8; TSB-E BASIC; FORTRAN; Assemblers; FOCAL, DIBOL Application pkg 64K-524K/drive 3.2M/drive — 256K, avg access 483 msec DECtape; 7/9 trk, 200/556/800 bpi 75K/drive 300 cpm reader 300 cps reader 185 cps (132 col); 173- 356 lpm Sync, async To 1,200 baud	Paper tape, Emulator Macro Assembler — — — — — — — — Sync, async 50 to 9,600	DOS II; CAPS-11; RT-11 RSX-11M/S Assemblers; FORTRAN; BASIC; FOCAL COMTEX II, IBM 2780 Emulator 128K-1M/drive — 2.4M/drive 40M/88M/drive 256K; 483 msec avg access time DECtape; 7/9 trk, 45 ips 300 cpm (80-col) reader 300 cps reader, 50 cps punch 60-1,200 lpm; (80-132 col) Sync, async To 10M baud	DOS-11; RSTS-11; RT-11; MUMPS-11, RSX-11D/M/S Assemblers; FORTRAN; COBOL; BASIC; FOCAL COMTEX-II, IBM 2780 Emulator 128K-1M/drive 2.4M/drive 40M/80M/drive 256K; 483 msec avg access time DECtape; 7/9 trk, 45 ips 300 cpm (80 col) reader 300 cps reader, 50 cps punch 60-1,200 lpm; (80-132 col) Sync, async To 1M baud	DOS-11; RSTS-11; MUMPS- 11, RSX-11D/M/S Assemblers; FORTRAN; COBOL; BASIC; FOCAL COMTEX II 128K-1M/drive 2.4M/drive 40M/80M/drive 256K; 483 msec avg access time DECtape; 7/9 trk, 45 ips 300 cpm (80 col) reader 300 cps reader, 50 cps punch 60-1,200 lpm (80-132 col) Sync, async 50 to 1M baud
<b>COMMENTS</b> — Not Applicable NA Information Not Available	Software also available from DECUS, including ALGOL-8.	PDP 11/03 is boxed version of LSI-11. (1) register to register (2) memory to memory (3) memory to register	Applications programs are available for power and industrial environments. PDP-11/05 is OEM version of 11/10, 11/04 uses MOS memory.	PDP-11R is ruggedized version of PDP-11/20, 11/15 is OEM version of 11/20	PDP-11/35 is OEM version of 11/40

**SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE A—D**

SYSTEM IDENTITY	Digital Equipment PDP-11/45; 11/50	Digital Equipment PDP-11/70	Digital Equipment PDP XVM System (PDP-15)	Digital Scientific META 4
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	KB11 2 bytes/wd 16 Byte; wd 83; 50 16 2 5 int, 4 ext 16, 32, 48 1.84; 1.01; 75(1) 4.68; 3.86; 3.60(1) 8.58; 7.76; 7.50(1) 4.80/6.46; 3.37/5.42; 2.80/5.20(1) 4.80/8.16; 3.37/7.12; 3.00/6.00(1) 4.80/8.86; 3.49/8.82; 3.00/8.60(1) 4.3 Yes 10-1,000KHz Yes NA NA NA NA NA Bootstrap loader	2 bytes/wd Byte/wd/doubleword 400 std; 46 opt 16 2 5 int, 4 ext 16, 32, 48 3.1 5.3 9.9 9.9 11.9 12.9 4.3 Yes 60Hz, 50Hz Yes NA NA NA NA NA Yes	KP15 2 bytes/wd (byte=9 bits) 186 Wd 65; 65 to 222 1 Hcg, 1 index 1 8 levels, 32 sublevel 18 6.6 14.1 11.8 8.2/8.3 16.2 15.6 5.1 Yes Line frequency No NA NA NA NA Yes	4030/4040 2 bytes/wd 16 Wd 139 std; 16 opt 2 1 14 std, 10 opt 16/32 — — — — — — 4.3 Yes — Yes NA NA NA NA NA
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core/MOS/Bipolar 1 16K-126K .9, .98 (core) .495 (MOS) .3 bipolar — — — Parity opt, 1 bit/byte Opt Yes, opt No NA NA Yes 16 Unlimited Software dependent Yes 16 Unlimited 2M —	Core 1 64K-2M 1.0 No — — Parity, 1 bit/byte Yes Yes Bipolar 1K 0.24 Yes (UNIBUS) 16 Unlimited Software dependent UNIBUS; Data Channel (4) 16 Unlimited 4M (UNIBUS) 5.8M (data channel)	Core 1 8K-256K .980 No — — Parity opt Yes opt No, memory relocation only No — — Yes 16 8 channels 2M Unichannel (includes PDP-11 CPU)	Core 1 16K-64K/16K-128K .9 No — — Parity std Std No No — — DPC 16 NA Software dependent and Selector DC (4040), SAC (4030) 16 9 NA OEM channels (4040)
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	DOS-11, RSTS-11; RT-11; MUMPS-11; RSX-11D/M/S Assemblers; FORTRAN; COBOL; BASIC; FORTRAN COMTEX 11 128K-1M/drive 2.4M/drive 40M/80M/drive 256K, 483-msec avg access time 96K/tape, 550 bytes/sec DECTape; 7/9 trk, 45 ips 300 cpm (80 col), reader 300 cps reader, 50 cps punch 60-1,200 lpm (80-132 col) Sync, async 50 to 1M baud	IAS; RSTS/E, RSX-11D FORTRAN IV, FORTRAN IV PLUS; BASIC, COBOL COMTEX-11 128K-1M/drive 2.4M/drive 40M/80M/drive 256K, 483-msec avg access time 90K/tape, 550 bytes/sec NA 300 cpm reader 300 cps reader, 50 cps punch 60-1,200 lpm (80-132 col) Sync, async 50 to 1M baud	XVM/DOS, XVM/RSX, XVM/MUMPS FORTRAN IV, ALGOL, RASP, FOCAL, Assembler — 524K 2.4M 20M/40M NA 45 ips NA 200-1,000 cpm reader 200 cps reader/50 cps Punch 356-1,110 lpm Sync, async 2,400 baud	None Microassembler — 1M 20M (4040) NA NA 7/9 trk; 37.5, 75 ips NA 600-1,000 cpm reader 50 cps punch; 400 cps reader (4030) 800-600 lpm; 165 cps (4030) Sync, async 600 to 2,400 bps
<b>COMMENTS</b> — - Not Applicable NA - Information Not Available	(1) indicates core, MOS and bipolar	Has buses between cache and memory and between and high-speed channel are 32 bits wide.	Other PDP-15 software. PDP-11 peripherals interface to unichannel.	4030 compatible with IBM 1130 and 4040 compatible with IBM 1800



# SPECIFICATION CHART

## CENTRAL PROCESSORS AND WORKING STORAGE E-H

AUERBACH Buyer's Guide to . . .  
MINICOMPUTERS

SYSTEM IDENTITY	Electronic Associates EAI PACER 100	General Automation GA-16/110, 220	General Automation GA-16/330	General Automation GA-16/440	General Automation SPC-12
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	2 bytes/word 16 Word 91 std 10 1 15 16 2.0 6.0 6.6 6.0 9.0 10.2 4.3 Yes 1/5/10/50/100/500/ 1,000 msec No -- -- -- NA Yes	2 bytes/word 16 std; 18 w/parity; 22 w/ERCC Word 91+ 16 1 64 std; unlimited opt 16 2.25 Std (unsigned) Std (unsigned) Opt Opt Opt 4.3 Yes 1 msec Yes NA NA NA 0.450 --	2 bytes/word 16 std; 18 w/parity Word 91+ 18 1 64 std; unlimited opt 16 or 32 2.25 18.9 18.0 Opt Opt Opt 4.3 Yes 1 msec Yes, CROM NA NA 0.450 0.450 --	2 bytes/word 16; 18 w/parity Word 83+ 18 1 64 std; unlimited opt 16; 32 0.78 11.1 12.8 -- External Processor -- -- 4.3 Yes 1 msec Yes, CROM 512/1K 64 -- --	1 byte/word 8 Byte 52 7 1 1.64 16 -- -- 3.4 Yes NA No -- -- -- No No -- -- Yes 12 128 460K Opt 12 128 460K --
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core 2 16K/65K 1.0 No -- -- No parity Yes No No -- Yes 16 64 Software dependent 2 opt 16 2 2M --	RAM, ROM, PROM NMOS, bipolar, dipolar 1 8K/128K -- Yes 0.300 0.450 Parity, ERCC Yes (write) No No N -- Yes 16 240K NA 16; 1(110), 2(220) -- 4M; 2M (220) Serial I/O (220); SPC-16 DMA (220)	Core 1 32K/132K 0.720 No -- -- Parity, 1 bit/byte Yes No No -- Yes 16 64 240K Yes 16 1 std, multiple opt 2M Serial I/O for TTY	Core 1 32K/2M 0.720 No -- -- Parity Yes No No -- Yes 16 64 240K Yes 1 std, multiple opt 2.2M Serial I/O for TTY	Core 1 4K/16K 2.16 ROM -- -- No parity Opt No No -- -- Yes 12 128 460K --
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	PTS, COS, TOS, DOS, RTOS Assembler, FORTRAN IV, HOI NA 720K, 17-msec access time NA NA NA 9 trk, 25-75 ips 90K, 10 ips; 900 bpi Reader, 300 cps Reader, 300, punch 120 245-1,200 lpm; 80/132 cols Sync, async for up to 4 lines/controller To 9,600 baud	FSOS; Control I (220), II, III (220) CAP-16 (both) FORTRAN, BASIC, COBOL (220 only) -- SPC-16 Series devices -- -- -- -- -- -- -- --	Control I, II, III CAP 16, FORTRAN, BASIC, COBOL -- SPC-16 devices -- -- -- -- -- -- -- --	Control I, II, III, IV MACRO, FORTRAN, BASIC, COBOL -- SPC-16 devices -- -- -- -- -- -- -- --	-- Assembler (CAS) -- -- -- -- -- -- -- -- TTY ASR 33/35, 10 TTY ASR 33/35, 10 Sync, async 110 to 9,600 baud
<b>COMMENTS</b> -- Not Applicable NA Information Not Available	HOI is hybrid operation interpreter.	GA-16/110, 220, and 330 use same microprocessor; CPU memory and I/O on one (110, 220) board; RAM memory standard; ROM and PROM piggyback.	Uses same microprocessor as GA-16/110 and 330. User-programmed CROM expansion available.	Processor uses MSI bipolar and tri-state technology. User can program 512 words of CROM.	No longer actively marketed. (1) Double precision, by subroutine.

# SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE E—H

SYSTEM IDENTITY	General Automation SPC-16/40 and 45	General Automation SPC-16/60 and 65	General Automation SPC-16/80 and 85	General Automation 18/30 Industrial Supervisory System	GRI-99 10, 30, 40, 50
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	2 bytes/word 16 Word 83 8 std; 8 opt 1 64 16 or 32 2.3 7.1 10.1 3.2 6.4 7.2 3.4 Yes 1.44 msec No — — — NA Yes (opt)	2 bytes/word 16 Word 83 8 std; 8 opt 1 64 16 or 32 2.6 7.4 10.4 3.5 6.7 7.5 4.3 Yes 0.96 msec No — — — NA Yes	2 bytes/word 16 Word 83 8 std; 8 opt 1 64 16 or 32 3.6 9.9 11.4 4.5 7.7 8.5 3.4 Yes 0.8 msec No — — — NA Opt (paper tape, card, disc, TTY)	Word 16 + parity + protect Word 32 2 acc; 3 index 1 8-61 16; 32 2.4 12.0 13.2 200 (subroutine) 350 (subroutine) 350 (subroutine) 4.3 Yes, 3 — No — — NA —	2 bytes/word 16 Word 229 std; 4 opt; 249 (50) 10; 11; 17; 19 1 No limit/16 lines 16 15.8 NA NA 278 407.8 NA 4.3 Yes 0, 1, 1.0 msec; 50/60 Hz Yes NA NA NA — Autoload feature, TTY, PT reader
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core 8K-64K (16/40); 256K (16/45) 1.44 No — — No parity Opt — No — — Yes 16 64 347K Yes, 4 16 1/channel 1.4M DCM (8 DMA-type subchannels)	Core 8K-64K (16/60); 256K (16/65) 0.960 No — — No parity Opt — No — — Yes 16 64 347K Yes, 4 16 1/channel 2M DCM (8 DMA-type subchannels)	Core 8K-64K (16/80); 256K (16/85) 0.800 No — — No parity Opt — No — — Yes 16 64 347K Yes, 4 16 1/channel 2.5M DCM (8 DMA-type subchannels)	Core 16K-64K 0.960 No — — Parity std Std — No — — Yes 16 944 260K Yes 16 944 833K —	Core; ROM 8K-64K 1.76; 0.88 ROM No NA NA No parity No — — Yes 16 9 (Model 10), unlimited(others) 160K Yes 16 Unlimited 1.36M —
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	BSP-16, FSOS-16, DBOS II, RTX-16, RTOS-II BASIC, FORTRAN IV, Commercial FORTRAN RJE-16 256K/512K 2.5M/5M/drive 6.4M/25M/drive 294K/drive 7/9 trk; 25-75 ips; 556/800 bpi NA Reader, 300; punch 75 125, 200, 600 lpm (132 col) Sync, async 75-9,600 baud	BSP-16, FSOS-16, DBOS II, RTX-16, RTOS-II BASIC, FORTRAN IV, Commercial FORTRAN RJE-16 256K/512K 2.5M/5M/drive 6.4M/25M/drive 294K/drive 7/9 trk; 25-75 ips; 556/800 bpi NA Reader, 300; punch 75 125, 200, 600 lpm Sync, async 75-9,600 baud	BSP-16, FSOS-16, DBOS II, RTX-16, RTOS-II BASIC, FORTRAN IV, Commercial FORTRAN RJE-16 256K/512K 2.5M/5.0M/drive 6.4M/25M/drive 294K/drive 7/9 trk; 25-75 ips; 556/800 bpi NA Reader, 300; punch 75 125, 200, 600 lpm Sync, async, up to 32 75-9,600 baud	DMS FORTRAN IV, Assembler CMS Communication 1M/drive — 5M/20M/drive NA 7/9-trk; 25-75 ips Reader, 300-1,000; punch, 35-100 Reader, 400; punch, 75 600 lpm; 15 cps; 132 cols Yes To 2,400 baud	COS, RTX Assembler — NA 2.4M/4.8M/drive NA NA NA Reader, 300-400; (80 col) Reader, 300; punch, 75 100-1,110 lpm Async, sync To 9,600 baud
<b>COMMENTS</b> — Not Applicable NA - Information Not Available	16/40 is packaged as a system; 16/45 is packaged bare bones.	16/60 is packaged as a system; 16/65 is packaged bare bones.	16/80 is packaged as a system; 16/85 is packaged bare bones.	—	Universal bus; Model 50 includes context switching, stack processing, bit manipulation, block-extended arithmetic, and disc I/O facilities.



SYSTEM IDENTITY	Harris Slash 1	Harris Slash 3	Harris Slash 4	Harris Slash 5	Harris Slash 7
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	Word 24 + 1 parity 15 bits 596 + SAU, BP 5 1 4.72 24 1.2 4.8 9.0 1.8 4.8 9.0 6.8 Yes 1 KHz No — — — NA Hardware bootstrap	Word 24 + 1 parity 15 bits 584 + SAU, BP 5 1 4.24 24 2.0 8.0 15.0 3(1) 7(1) 12(1) 6.8 Yes 1 KHz No — — — NA Hardware bootstrap	Word 24 + 1 parity 15 bits 602 + SAU, BP 5 1 4.48 24 1.5 6.0 11.25 2.25 5.25 9.0 6.8 Yes 1 KHz No — — — NA Hardware bootstrap	Word 24 + 1 parity 15 bits 592 5 1 2.24 24 + 1 parity 1.9 5.7 14.25 37.5 44.0 64.5 6.8 Yes 1 KHz No — — — NA Hardware bootstrap	Word 24 + 2 parity Word, byte, bit 600 6 1 14.48 24 1.0 2.1 6.4 0.8-1.8 5.0 11.7 6.8 Yes 120 Hz No — — — — — Hardware disc bootstrap
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core 1 24K-192K 0.600 No — — Parity std; 1 bit/wd Opt — No — — 1 std; 27 opt 8/24 16/channel 1.2M ABC opt 24 14/channel 5.1M —	Core 1 24K-192K 1.0 No — — Parity std; 1 bit/wd Opt — No — — 1 std; 13 opt 8/24 16/channel 750K ABC opt 8-24 16/channel 3M	Core 1 to 5 24K-786K core; 96K SC 0.75 core; 20 semicon- ductor No — — Parity std; 1 bit/wd Opt — No — — 1 std; 23 opt 8/24 16/channel 1M ABC opt 8-24 16/channel 3.9M/port core 5M/port SC	Core Multiport, singleport 24K-195K 0.950 No — — Parity std; 1 bit/wd Opt — No — — 1 std; 12 opt 8/24 16/channel 789K ABC opt 8-24 16/channel 3M	Core/SC 1; 2; 4 196-786K 0.750/200 No — — Parity std, 2 bits/wd Yes in pgs of 1K wds Yes No — — Yes, IOC 16/channel — CBC/IOF — 3.8M (CBC); 5M (IOF) 5.7M aggregate
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	DMS, DOS, TOS, ROS, VULCAN FORTRAN IV, FORGO BASIC, RPG, SNOBOL — 430K/860K/2.2M 2.7M/10.8M/drive 28M/40M/drive NA 7-/9-trk; 556-1,600 bpi; 45-200 cps NA Reader, 330-1,000; punch, 100 Reader, 300; punch, 75 300-1,200 lpm; 123, 132 cols Sync, async 12.5-9,600 baud	DMS, DOS, TOS, ROS, VULCAN FORTRAN IV, FORGO, BASIC, RPG, SNOBOL — 430Kb/860K/2.2M 2.7M-10.8M/drive 28M/40M/drive NA 7-/9-trk; 556-1,600 bpi NA Reader, 330-1,000; punch, 100 Reader, 300; punch, 75 300-1,200 lpm; 123, 132 cols Sync, async 12.5-9,600 baud	DMS, DOS, TOS, ROS, VULCAN FORTRAN IV, FORGO, BASIC, RPG, SNOBOL — 430K/860K/2.2M 2.7M/10.8M/drive 28M/56M; 40M/drive NA 7-/9-trk; 100-1,600 bpi NA Reader, 330-1,000; punch, 500 Reader, 300; punch, 60 300-1,200 lpm; 123, 132 cols Sync, async 112.5-9,600 baud	DMS, DOS, TOS, ROS, VULCAN FORTRAN IV, FORGO, BASIC, RPG, SNOBOL — 430K/860K/2.2M 2.7M/10.8M 28M/56M; 40M NA 7-/9-trk; 100-1,600 bpi NA Reader, 300-1,000; punch, 500 Reader, 300; punch, 60 300-1,200 lpm; 123, 132 cols Sync, async 112.5-9,600 baud	VULCAN FORTRAN IV, Interactive BASIC, COBOL, RPG — 430K/860K/2.2M 2.7M/10.8M 28M/56M; 40M NA 7-/9-trk; 100-1,600 bpi NA Reader, 300-1,000; punch, 500 Reader, 300; punch, 60 300-1,200 lpm; 123, 132 cols Sync, async 112.5-9,600 baud
<b>COMMENTS</b> — - Not Applicable NA - Information Not Available	(1)With SAU option Scientific Arithmetic Unit	(1)With SAU option Scientific Arithmetic Unit	SC = semiconductor SAU = Scientific Arithmetic Unit BP = bit processor		

# SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE E—H

SYSTEM IDENTITY	Harris S100	Harris S200	Hewlett-Packard 21MX	Hewlett-Packard HP 3000CX	Honeywell System 700
<b>CENTRAL PROCESSOR</b>					
Data Format	Slash 4	Slash 7	M/10, M/20, M/30	50CX, 100CX, 200CX, 300CX	716
Word Size, bits	Word 24 + 2 parity	Word 24 + 2 parity	2 bytes/word 16 + 1 parity	2 bytes/word 16 + parity	2 bytes/word 16 + 2 parity (opt)
Address Orientation	Word, byte, bit	Word, byte, bit	Word	Word	Word
No. of Machine Instr.	600	600	128; 38	172	78 std; 4 opt
No. of Program Registers	6	6	4	11	4
No. of Addresses/Instr.	1	1	1	1	1
No. of Interrupt Levels	10.48	14.48	60	253	3.48
Instruction Length, bits	24	24	16/32	16	—
Execution Times, $\mu$ sec	1.5	1.0	1.94/7.12	0.7/2.6	1.6
Add/Subtract	6.0	2.1	12.3-13.3	6.0/8.2	3.9
Multiply	11.3	6.4	15.9-18.2	—/8.8	7.0
Divide	0.8-2.3	0.8-1.8	22.54/23.57	13.2	Subroutine
Floating Multiply	5.3	5.0	48-57	17.7	Subroutine
Floating Divide	12.0	11.7	41-76	23.6	Subroutine
Max. Precision, Decimal Digits	6.8	6.8	4.3	4.3	4.3
Real-Time Clock	Yes	Yes	Yes	—	Yes
Resolution	120 Hz	120 Hz	100 $\mu$ sec	—	NA
Control Memory	No	No	Yes	Yes	No
Size, wds (min/max)	—	—	1K std; 512 opt	2,048	—
Word Length, bits	—	—	24	32	—
Cycle Time, nsec	—	—	0.325	0.175	—
Processor Cycle Time, $\mu$ sec	—	—	—	—	—
APL	Hardware disc bootstrap	Hardware disc bootstrap	Disc loader	NA	—
<b>WORKING STORAGE</b>					
Technology	Core	Core; SC	MOS X1/X2	Core	Core
No. of Ports	1; 2; 4	1; 2; 4	1	1	1
Main Memory Capacity, (min/max, bytes)	98-196K	196-786K	8K/16K-128K/384K, 512K	96/128K	16K/128K
Core Cycle Time, $\mu$ sec	0.750	0.750/200	—	0.980	0.775/0.855/1.02
Solid State Memory	No	No	MOS; RAM	No	No
Real Time, $\mu$ sec	NA	NA	—	NA	NA
Cycle Time, $\mu$ sec	NA	NA	0.650	NA	NA
Error Control	Parity std; 2 bits/wd	Parity std; 2 bits/wd	Parity; 1 bit/wd	Parity; 1 bit/wd	Parity opt; 1 bit/byte
Memory Protect	Yes, in pgs of 1K wds	Yes, in pgs of 1K wds	2108A only	Std	Memory lockout opt
Memory Management	Yes	Yes	No; opt on 2108A	Std	Base sector relocate
Cache Memory	No	No	No	No	No
Size, (min/max, wd)	—	—	—	—	—
Cycle Time, $\mu$ sec	—	—	—	—	—
<b>I/O CHANNELS</b>					
PIO					
Width, bits	Yes IOC	Yes IOC	Yes	Yes	Yes
No. of Devices	—	—	16	16	16
Max Xfer Rate, bytes/sec	16/channel	16/channel	36; 41	253	64
DMA	—	—	—	2,400 baud, direct I/O	Program dependent
Width, bits	CBC	CBC/IOP	Yes, 2	Yes, 4 channels	Yes
No. of Devices	—	—	16	16	16
Max Xfer Rate, bytes/sec	2.7M; 4M aggregate	3.8M (CBC); 5M (IOP)	1.2M	8/channel	No limit
Other (type; xfer rate, bytes/sec)	—	5.7M aggregate	—	1.9M/channel	1.3M
	—	—	—	MPLX I/O, 2-32 channels	DMC, 644K bytes/sec
<b>SOFTWARE</b>					
Types of Op. Sys.	VULCAN	VULCAN	DOS III, RTE, TSS	MPE/C, MPET	OS/700, BOS, OP-16
Languages	FORTRAN IV, Interactive BASIC, COBOL, RPG II	FORTRAN IV, Interactive BASIC, COBOL, RPG	FORTRAN, FORTRAN IV, BASIC, and ALGOL	BASIC, FORTRAN, COBOL, RPG II, SPL	BASIC, FORTRAN IV, DAP-16
Communications	—	—	—	MPET, 2780/3780 Emulation	RJE (HASP II); RCP 707
<b>I/O DEVICES</b>					
Fixed Head Discs (capacity, bytes)	860K(1)	860K-1.7M(1) 2.1(2)	NA	1M-4M	128K-1M
Disc Cartridges (capacity, bytes)	10.8M-80M	NA	2.5M/5M/drive	5M/drive	NA
Disc Pack (capacity, bytes)	NA	NA	23.5M/drive	47M/drive	2.2M-15M/drive
Floppy Discs (capacity, bytes)	NA	310K	NA	NA	No
Magnetic Tape (type)	9-trk; 800 bpi	9-trk; (800 bpi; 800, 1,600)(2) 25-150 ips	7/9 trk; 200, 1,600 bpi; 45 ips	9-trk; 800, 1,600 bpi; 45 ips	7-/9-trk; 800, 1,600 bpi; 26-70 ips
Cassettes (capacity, bytes)	NA	NA	NA	NA	Yes
Punched Card (type; speed cpm)	Reader, 600-1,000	Reader, 600-1,000	Reader, 200-600	Reader, 200-1,200 punch, 75	Reader, 200-1,050; punch, 100-1,000
Paper Tape (type; speed cps)	NA	NA	Reader 500; punch, 75, 120	Reader, 1,500; punch, 75	Reader, 300; punch, 110
Printers (speed, lpm; col)	200-600 lpm	200-600 lpm	150-600 lpm, 132 cols; 100 lpm, 80 cols	200-1,250 lpm, 132 cols	200-1,100 lpm; 96-136 cols
Data Comm	—	Sync, async	Sync, async	RTC to HP21MX; async (400K bytes/sec)	Sync, async
Xmission Rates	—	—	45-2,400 baud	2,400 baud	10K baud
<b>COMMENTS</b>	(1)S120 only	(1) 220 only (2) 230 and 240	IMAGE 2000, TCS, RJE, and over 1,000 applications software packages available.	Most standard peripherals interface to MPLX. Aggregate xfer rate 880K bytes/sec; IMAGE 3000 with Query/3000 available for DBMS.	For systems with memories above 32K words, cycle time is slowed to 855 $\mu$ sec for first 32K words and to 1.02 $\mu$ sec above 32K.
— - Not Applicable NA - Information Not Available					



# SPECIFICATION CHART

## CENTRAL PROCESSORS AND WORKING STORAGE I-N

AUERBACH Buyer's Guide to . . .  
MINICOMPUTERS

SYSTEM IDENTITY	Interdata 7/16	Interdata 7/32	Interdata Model 8/32 Megamini	Interdata Model 70	Interdata Model 74
<b>CENTRAL PROCESSOR</b>			M83-023		
Data Format	2 bytes/word	4 bytes/word	4 bytes/word	2 bytes/word	2 bytes/word
Word Size, bits	16 + 1 parity	16/32 + 1 parity halfword	32 + 2 parity	16 + 1 parity	16 + 1 parity
Address Orientation	Word	Halfword (16 bits)	Halfword/word	Word	Word
No. of Machine Instr.	113	136 std; 7 opt	219	113	110
No. of Program Registers	16	30	8 stacks of 16	16	16
No. of Addresses/Instr.	1	1	1	1	1
No. of Interrupt Levels	256	1,023	1,024/4 lines	255	255
Instruction Length, bits	16; 32	16; 32; 48	16; 32; 48	16	16; 32
Execution Times, $\mu$ sec					
Add/Subtract	2.25/2.25	3.35	0.2	3.25	3.25
Multiply	2.25	16	3.5	10.75	45.25
Divide	42.00	100	5.8	12.25	56.00
Floating Add/Sub	31	15 to 25	2.3	26.5/31.5	-
Floating Multiply	44	32 to 34	3.0	73.5	-
Floating Divide	69	55 to 57	5.3	109.5	-
Max. Precision, Decimal Digits	4.3	9.2	9.2	4.3	4.3
Real Time Clock Resolution	Yes	Yes	Yes	Yes	Yes
Control Memory	8.3-10 msec	NA	8.3-10 msec	8.3-10 msec	8.3-10 msec
Size, wds (min/max)	Yes	Yes	Yes	Yes, ROM	Yes, ROM
Word Length, bits	NA	NA	NA	NA	NA
Cycle Time, nsec	NA	NA	NA	NA	NA
Processor Cycle Time, $\mu$ sec	0.240	0.12	0.240	0.120	0.120
APL	-	IPL (bootstrap)	Yes	Yes	Yes
<b>WORKING STORAGE</b>					
Technology	Core	Core	Core	Core	Core
No. of Ports	1	-	1	1	1
Main Memory Capacity, (min/max, bytes)	8K/64K	32K/1M	132K/1M	8K/64K	8K/64K
Core Cycle Time, $\mu$ sec	0.750/1.0	0.75/1.0	0.75	1.0	1.0
Solid State Memory	No	No	No	No	No
Real Time, $\mu$ sec	NA	-	-	-	-
Cycle Time, $\mu$ sec	NA	-	-	-	-
Error Control	Opt, 1 bit/word	Parity, 1 bit/byte	Parity, 1/halfword	Parity, 1 bit/word	Parity, 1 bit/word
Memory Protect	Opt	Up to 7 protect states	Yes (MAC)	Opt	No
Memory Management	No	-	Yes	No	No
Cache Memory	No	No	Yes, 1 lookahead	No	No
Size, (min/max, wd)	-	-	2 64-bit regs	-	-
Cycle Time, $\mu$ sec	-	-	0.050	-	-
<b>I/O CHANNELS</b>					
PIO	Std	Std (Auto Drive Channels)	Yes	Std	Std
Width, bits	16	16	16	16	16
No. of Devices	255	1,023	1,023	255	255
Max Xfer Rate, bytes/sec	Software dependent	88K	166	Program dependent	Program dependent
DMA	Std	Std	Yes	Std	Std
Width, bits	16	16	16	16	16
No. of Devices	4	Up to 7	7	4	4
Max Xfer Rate, bytes/sec	5.2M	5.2M	6M	2M	2M
Other (type; xfer rate, bytes/sec)	-	Selector, 4M	Multiplexor, 62.5K	-	-
<b>SOFTWARE</b>					
Types of Op. Sys.	BOSS, RTOS, DOS	OS/32MT; OS/32ST	OS/32MT; OS/32ST	BOSS, RTOS, DOS	BOSS, RTOS, DOS
Languages	Assembler, BASIC, FORTRAN	FORTRAN, BASIC, MACRO CAL	FORTRAN V, MACRO CAL, BASIC	BASIC, FORTRAN IV	BASIC, FORTRAN IV/V
Communications	NA	ITAM, RJE (2780 or 3780)	ITAM	ITAM	ITAM
<b>I/O DEVICES</b>					
Fixed-Head Discs (capacity, bytes)	-	-	-	-	-
Disc Cartridges (capacity, bytes)	2.5M-10M/drive	2.5M-10M/drive	2.5M-10M/drive	2.5M/drive	2.5M/drive
Disc Pack (capacity, bytes)	2.5M-40M	40M	10M-40M/drive	40M/drive	40M/drive
Floppy Discs (capacity, bytes)	-	-	-	-	-
Magnetic Tape (type)	7-9-trk; 556-1,600 bps	7-9-trk; 200, 556, 800, 1,600 bpi; 45 ips	7-9-trk; 160, 1,800 cpi	7-9-trk; 556, 800, 1,600 bpi	7-9-trk; 556-1,600 bpi
Cassettes (capacity, bytes)	500K	500K	500K	500K	500K
Punched Card (type; speed cpm)	Reader, 400-1,000	Reader, 400	Reader, 400-1,000	Reader, 400-1,000	Reader, 400-1,000
Paper Tape (type; speed cps)	Reader, 300, punch, 75	Reader, 300; punch, 75	Reader, 300; punch, 300/75	Reader, 300; punch, 75	Reader, 300; punch, 75
Printers (speed, lpm; col)	200-600 lpm	60-600 lpm; 5/30 cps; 132 cols	60, 200, 600 lpm; 15/30 cps; 132 cols	200-600 lpm	200-600 lpm
Data Comm	Sync, async	Sync, async	Sync, async	Sync, async	Sync, async
Xmission Rates	To 40,800 baud	To 40,800 baud	To 40,800 baud	To 40K baud	To 40K baud
<b>COMMENTS</b>			COBOL is available from Diversified Data Systems.	Multiplexor channel for I/O.	Multiplexor channel for I/O.
- - Not Applicable NA - Information Not Available					

# SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE I—N

SYSTEM IDENTITY	Interdata Model 80	Interdata Model 85	IBM Corp 1130	IBM Corp 1800 Data Acquisition & Control System	IBM Corp System 7
<b>CENTRAL PROCESSOR</b>					
Data Format	2 bytes/word	2 bytes/word	Word	Word	2 bytes/word
Word Size, bits	16 + 1 parity	16 + 1 parity	16 + 2 parity	16	16 + 2 parity
Address Orientation	Word	Word	Word, doubleword	Word, doubleword	Word
No. of Machine Instr.	127	131	29	29	39
No. of Program Registers	16	16	5	6	4 sets of 8
No. of Addresses/Instr.	1	1	1	1	1
No. of Interrupt Levels	256	256	5	12	4; 16 sublevels
Instruction Length, bits	16; 32	16; 32	16; 32	16; 32	16; 32
Execution Times, $\mu$ sec					
Add/Subtract	1.01	1.01	8.0	4.5	800
Multiply	2.73	2.73	15.7	15.25	—
Divide	3.23	3.23	76.0	—	—
Floating Add/Sub	13.01/13.21	11.41/11.91	—	230	—
Floating Multiply	20.47	23.99	—	280	—
Floating Divide	32.29	36.69	—	—	—
Max. Precision, Decimal Digits	4.3	4.3	4.3	4.3	4.3
Real-Time Clock Resolution	Yes	Yes	—	Yes	Yes
Control Memory	8.3-10 msec	8.3-10 msec	—	—	50 $\mu$ sec
Size, wds (min/max)	Yes	Yes, DCS	No	No	Yes
Word Length, bits	NA	1K	—	—	NA
Cycle Time, nsec	NA	32	—	—	NA
Processor Cycle Time, $\mu$ sec	0.120	0.120	—	—	NA
APL	NA	NA	NA	NA	NA
Yes	Yes	Yes	NA	NA	!PL (disc; card rdr)
<b>WORKING STORAGE</b>					
Technology	SS	SS	Core	Core	Monolithic SS
No. of Ports	1	1	1	1	1
Main Memory Capacity, (min/max, bytes)	16K/64K	16K/64K	8K/64K	8K/65K	4K/128K
Core Cycle Time, $\mu$ sec	—	—	3.6	4; 2(1)	—
Solid State Memory	Yes	Yes	NA	NA	SS
Real Time, $\mu$ sec	—	—	NA	NA	NA
Cycle Time, $\mu$ sec	0.270	0.270	NA	NA	0.400
Error Control	Parity, 1 bit/word	Parity, 1 bit/word	No parity	Parity, std	Parity, 1 bit/byte
Memory Protect	Opt	Opt	No	Std	Model E only
Memory Management	No	No	—	—	No
Cache Memory	No	No	No	No	No
Size, (min/max, wd)	NA	NA	NA	NA	NA
Cycle Time, $\mu$ sec	NA	NA	NA	NA	NA
<b>I/O CHANNELS</b>					
PIO	Std	Std	Direct prog cont	DPC channel	Yes, DDC
Width, bits	16	16	—	—	16
No. of Devices	255	255	—	—	1,023
Max Xfer Rate, bytes/sec	Program dependent	Program dependent	—	—	Program dependent
DMA	Std	Std	Yes	Yes	Disc cycle steal
Width, bits	16	16	—	—	16
No. of Devices	4	4	3 std; 9 opt channels	250K-500K	NA
Max Xfer Rate, bytes/sec	4.2M	4.2M	556K-880K	—	660K
Other (type; xfer rate, bytes/sec)	Selector, 6M	Selector, 6M	NA	NA	NA
<b>SOFTWARE</b>					
Types of Op. Sys.	BOSS, RTOS, DOS	BOSS, RTOS, DOS	Card/paper tape; disc monitor system	MPS, TSX	MSP17
Languages	BASIC, FORTRAN IV/V	BASIC, FORTRAN IV/V	FORTRAN, RPG, 1130 COBOL, 1130 Assembler	FORTRAN IV, RPG, Assembler	MACRO Assembler, Cross Assembler
Communications	ITAM	ITAM	—	—	—
<b>I/O DEVICES</b>					
Fixed-Head Discs (capacity, bytes)	NA	NA	NA	NA	Portion of disc pack
Disc Cartridges (capacity, bytes)	2.5M-10M/drive	2.5M-10M/drive	1M	1M	2.4/5M/drive
Disc Pack (capacity, bytes)	40M/drive	40M/drive	2M-4M	—	235M/554M (RPO)
Floppy Discs (capacity, bytes)	NA	NA	NA	7.25M	Internal
Magnetic Tape (type)	7-9-trk; 556-1,600 bpi; 45 ips	7-9-trk; 556-1,600 bpi; 45 ips	NA	9-trk; 800, 1,600 bpi	RPO
Cassettes (capacity, bytes)	500K	500K	NA	NA	RPO
Punched Card (type; speed cpm)	Reader, 400-1,000	Reader, 400-1,000	Reader, 1,000; punch, up to 160	80, 160 col; 300-400	RPO
Paper Tape (type; speed cps)	Reader, 300; punch, 75	Reader, 300; punch, 75	Reader, 60; punch, 14.8	14.8	RPO
Printers (speed, lpm; col)	200-600	200-600	80-600	120-600; 14 cps	RPO
Data Comm	Sync, async	Sync, async	Sync	NA	Sync, async; Sep/360/370 attach
Xmission Rates	To 40K baud	To 40K baud	2,400 baud	1,200-4,800 baud	1,200 bps, 50Kb/sec
<b>COMMENTS</b>					
— - Not Applicable NA - Information Not Available		Multiplexor channel for I/O. DCS = dynamic control store.	First delivery Nov 1965.	(1)First number applies to Model 1, second number to Model 2.	



SYSTEM IDENTITY	Lockheed Electronics SUE	Microdata Micro 1600 Series	Microdata 32/S	Modular Computer System Modcomp I	Modular Computer Modcomp II
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	Word, byte 16 Word, byte 108 std; 38 opt 8 2 4 16, 32 3.5/13.8 3.01 (subroutine) 4.98 (subroutine) — — — 4.3 Yes — ROM 256-2K NA NA NA Opt	2 bytes/word 16 Word 23 std, 107 opt 6 1 64 16, 32; 48 1.5 6.3 7.2 — — — 4.3 Yes — Yes NA NA 0.220 —	2 bytes/word 16 Word, doubleword, byte 52 std; 32 opt 32 1 64 8 to 40 — — Opt Opt 4.3 Yes — Yes, ROM/read-write 512-4K/512 32 0.135 — IPL (bootstrap)	2 bytes/word 16 Word 81 3 1 2.4 16; 32 0.8-3.4 10.3 12.3 — — — 4.3 Yes 1 msec Yes NA NA NA —	2 bytes/word 16 Word 106 std; 176 opt 16 1 3-16 16; 32 0.8-3.4/0.8-2.4 6.0-7.2 11.0-12.2 15.0/20.5 — 12.5/16.0 13.0/16.5 4.3 Opt 1 msec Yes NA NA NA —
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core 1 8K/64K 800 No — — RPQ RPQ NA No NA NA Yes 16 Unlimited Program dependent Yes 16 Unlimited 10M —	Core 1 16K/64K 1.1 (800) 1.0 (1,600) No — — No No NA NA Yes 8 32 20K Yes 4 or 8 910K (800); 1M (1,600) Serial TTY, 10/300 cps	MOS 1 8K/256K — Yes NA 0.350 Software (opt) Opt* Firmware Yes 1K/8K — Std 16 64 Program dependent Std 16 — 5.0M Concurrent I/O	Core 1 8K/64K 0.8 No — — No No NA NA Std 16 64 120K (interrupt mode); 1.7M (burst) DMP 16 4 600K —	Core, ROM, or RAM 1; 4 32/128K 0.8 — — Parity std Opt — No NA NA Std 16 — — Opt — 1.25K —
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm, col) Data Comm Xmission Rates	DOS, Basic Operating System FORTRAN IV, Assembler NA No 2.5M/drive No No No No Reader, 285-600 Reader, 300; punch, 75 100 cps; 200 lpm, 132 cols Async 300-4,800 baud	TOS (teletype/paper tape) Assembler, BASIC opt NA NA 5M-10M/drive NA NA 7-9-trk; 800 bpi; 12.5-25 ips NA Reader, 300 Reader, 300; punch, 75 245-356 lpm, 132-80 cols Sync, async 1,600 baud; 75 to 9,600 baud	GENASYS MPL (Microdata Programming Language) NA NA 5M-10M/drive NA NA 7-9-trk; 800, 1,600 bpi; 25 ips NA Reader, 300 Reader, 300; punch, 75 200-300 lpm, 132 cols Async 75-9,600 baud	MAX I Assembler Remote fill from host 524K-4M 5M-5M/drive 24.5-50M/drive NA 7-9-trk; 556, 800, 1,600 bpi; 12.5/45/75 ips — Reader, 300/1,000 punch, 35/1,000 Reader, 625; punch, 110 50-600 lpm; 132 cols Sync, async, computer link 75-20K baud; 200K bytes/sec	MAX, MAX I/II/III, MAXNET III Assembler, FORTRAN IV, BASIC, RPG MAXCOM, IBM 2780 and other emulators 524K-4M 5M-5M/drive 24.5-50M/drive NA 7-9-trk; 556, 800, 1,600 bpi; 12.5/45/75 ips — Reader, 300/1,000 punch, 35/1000 Reader, 625; punch, 110 50-600 lpm; 132 cols Sync, async, computer link 75-20K baud; 200K bytes/sec
<b>COMMENTS</b> — Not Applicable NA Information Not Available	Optional instructions for scientific processing.				The CP models implement communications instruction set used for RB/RJE, pre-processing, and concentrating.

# SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE I—N

SYSTEM IDENTITY	Modular Computer Systems Modcomp IV				
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	2 bytes/word 16; 32 Word 242 16 sets of 15 1 8-16 16; 32 1.6(1); 2.4(2) 1.6(1); 2.4(2) 1.6(1); 2.4(2) 6.24/10.1(2) 5.2/8.0(2) 6.7/11.2(2) 4.3 Yes 1 nsec Yes NA NA NA NA —				
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	Core 1; 2; 4 8K/512K 0.5/16 bits; 1.0/32 bits No — — Memory parity 4-level protect code Memory mapping No — — Std 32 64 Software dependent DMP, 4 32 16/channel 2.4M —				
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	MAX, MAX II/III/IV, MAXNET III Assemblers, RPG FORTRAN IV, BASIC MA 524K-4M 2.5M/5M/drive 24.5M/50M/drive 1 7-/9-trk; 556, 800, 1,600 bpi; 12.5, 45, 75 ips — Reader, 300/1,000, puech, 35/100 Reader, 625; punch, 110 50-600 lpm (132 col) Sync, async, computer links 75-20K baud; 200K bytes/sec				
<b>COMMENTS</b> — - Not Applicable NA - Information Not Available	(1) Single precision (2) Double precision; ALU is 32-bit, FPP is 64-bit.				



# SPECIFICATION CHART

## CENTRAL PROCESSORS AND WORKING STORAGE O—Z

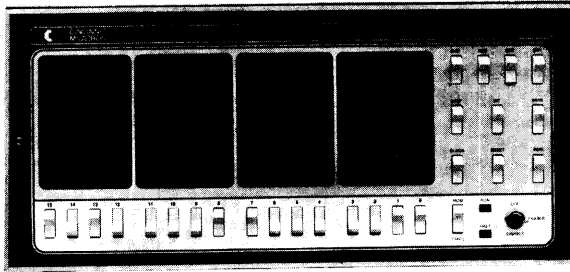
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MINICOMPUTERS

SYSTEM IDENTITY	Prime 100	Prime 200	Prime 300	Raytheon Data Systems RDS-500	SYSTEMS Engineering Labs SEL 32
<b>CENTRAL PROCESSOR</b> Data Format Word Size, bits Address Orientation No. of Machine Instr. No. of Program Registers No. of Addresses/Instr. No. of Interrupt Levels Instruction Length, bits Execution Times, $\mu$ sec Add/Subtract Multiply Divide Floating Add/Sub Floating Multiply Floating Divide Max. Precision, Decimal Digits Real-Time Clock Resolution Control Memory Size, wds (min/max) Word Length, bits Cycle Time, nsec Processor Cycle Time, $\mu$ sec APL	2 bytes/word 16 Word 112 std; 9 opt 26 1 64 16; 32 1.76-2.44 11.26 13.78 — — — 4.3 Yes NA Yes NA NA 64 NA NA TTY, PTR, disc, MT	2 bytes/word 16 + 2 parity Word 117 std; 37 opt 26 1 64 16; 32 1.36 10.48 13.24 9.35 — 27.82 39.46 4.3 Yes NA Yes NA No NA NA TTY, PTR, disc, MT	Word 16 + 2 parity Word 145 std; 29 opt 32 1 64 16 + 2 parity 1.88/1.56 9.04; 8.72 11.20; 10.95 8.75; 8.10 — 25.20; 24.56 37.92; 37.28 4.3 Yes NA Yes & WCS — 64 — — TTY, PTR, disc, MT	2 bytes/word 16 Word 98 std; 132 opt 10 1 16; 256(1) 16 1.6 4.0 5.0 3.5 — 7.0; 10.2 13.8; 18.4 4.3 Yes 1.0 msec std; 0.1 opt No NA NA NA NA NA NA	4 bytes/word 32 Word, doubleword, halfword, byte 152 8 1 128 32 1.2 4.5 5.1 3.0 — 4.5 8.9 9.2/18.9 Yes 1/60 sec; 1/120 sec; 60 Hz ROM NA NA 150 NA NA
<b>WORKING STORAGE</b> Technology No. of Ports Main Memory Capacity, (min/max, bytes) Core Cycle Time, $\mu$ sec Solid State Memory Real Time, $\mu$ sec Cycle Time, $\mu$ sec Error Control Memory Protect Memory Management Cache Memory Size, (min/max, wd) Cycle Time, $\mu$ sec <b>I/O CHANNELS</b> PIO Width, bits No. of Devices Max Xfer Rate, bytes/sec DMA Width, bits No. of Devices Max Xfer Rate, bytes/sec Other (type; xfer rate, bytes/sec)	MOS 1 4K/64K — Yes — 1.0 No No No NA NA Yes 16 No limit Program controlled Yes 16 8 1.3M DMC, DMT	MOS 1 4K/64K — Yes NA 0.750 Parity, 1 bit/byte No No No — Yes 16 8 1.8M DMC, DMT	MOS 1 16K — Yes — 0.60 Parity, 1 bit/byte Yes Yes, virtual addressing No — — Yes 16 No limit Program controlled Yes 16 8 2M DMC, DMT	Core 2 16K/128K 0.8-0.9 No NA NA Parity opt Opt No No — — Yes 16 NA NA 2M	Core 1 32K/1M 0.645 No — — Parity, 1 bit/byte Yes Yes No — — Yes, IOC 32 128 Software dependent Yes 32 128 1.2M/channel —
<b>SOFTWARE</b> Types of Op. Sys. Languages Communications <b>I/O DEVICES</b> Fixed-Head Discs (capacity, bytes) Disc Cartridges (capacity, bytes) Disc Pack (capacity, bytes) Floppy Discs (capacity, bytes) Magnetic Tape (type) Cassettes (capacity, bytes) Punched Card (type; speed cpm) Paper Tape (type; speed cps) Printers (speed, lpm; col) Data Comm Xmission Rates	DOS, RTOS Assembler, FORTRAN IV Software drivers for line controllers 256K-512K 6M-24M 276M NA 7-/9-trk; 800 ips NA Reader, 150 Reader, 200, punch, 75 165 cps; 300 lpm Sync, async —	DOS, RTOS BASIC, Assembler, FORTRAN IV Software drivers for line controllers 256K-512K 6M-24M 276M NA 7-/9-trk; 800 bpi NA Reader, 150 Reader, 200, punch, 75 165 cps; 300 lpm Sync, async 75-9,600 baud	DOS, DOS-VM, RTOS, RTOS VM BASIC, Assembler, FORTRAN IV Software drivers for line controllers 256K-512K 6M-24M 276M — 7-/9-trk; 800 ips — Reader, 150 Reader, 200, punch, 75 165 cps; 300 lpm Sync, async 75-9,600 baud	SOS, MTOS, RTOS, Basic; SOS Assembler, Conversational FORTRAN, FORTRAN IV, RPG — 770K 2.56M-5.13M 25.9M-51.96M — 7-/9-trk; 37.5 ips — Reader, 100-400, 80 col punch, 300-1,000 Reader, 300; punch 110 245-1,100; 80/132 col Sync, async 110-9,600 baud	Real-time monitor FORTRAN IV IBM 2780 & CDC 200-UT simulators 1M/2M/drive 5M/10M/drive 36M/72.6M/drive — 7-/9-trk; 556, 800, 1,600 bpi; 75 ips — Reader, 285-1,000; punch, 100 — 125-600 lpm; 132/136 cols Sync, async 50-9,600 baud
<b>COMMENTS</b> — Not Applicable NA Information Not Available			Microassembler for programming WCS	(1) Software via RTOS and MPS real-time operating system	I/O performed by micro-programmable processors

# SPECIFICATION CHART — CENTRAL PROCESSORS AND WORKING STORAGE O—Z

SYSTEM IDENTITY	Texas Instruments 960B	Texas Instruments 980B	Varian Data Machines V-70 Series	Varian Data Machines V-75	Xerox 530
<b>CENTRAL PROCESSOR</b>			V71, V72, V73, V74		
Data Format	2 bytes/word	2 bytes/word	2 bytes/word	2 bytes/word	2 bytes/word
Word Size, bits	16 + 6 check	16 + 6 check	16 + 2 parity	16	16 + 2 parity
Address Orientation	Word, byte, bit	Word, byte, bit	Word, byte	Byte, word, doubleword	Word
No. of Machine Instr.	78 std; 22 opt	98 std; 106 opt	175 std; 18 opt	187 std; 14 opt	72 std; 10 opt
No. of Program Registers	2-1/2	7	3	8; 7 index	8
No. of Addresses/Instr.	Up to 2,048	367	1	1	1
No. of Interrupt Levels	Software/3 lines	1	0.64 in 8 level increments	Up to 64	16 std; 28/40 opt
Instruction Length, bits	32	16; 32	16; 32	16; 32	16
Execution Times, $\mu$ sec					
Add/Subtract	3.6	1.75	660; 1,320; 2.4	0.7; 1.3; 2.0(1)	1.92
Multiply	8.6 opt	2.25-6.25	4.4-4.8; 4.8-5.3; 5.3-5.8	4.5; 4.8; 5.4(1)	8.00
Divide	10.5 opt	2.75-7.75	4.7-5.6; 5.1-5.9; 5.6-6.5	4.8; 5.2; 6.0(1)	12.12
Floating Add/Sub	Subroutine	Subroutine	5.0	3.7	8.80
Floating Multiply	Subroutine	Subroutine	7.0	6.1	32.96
Floating Divide	Subroutine	Subroutine	9.0	8.6	77.56
Max. Precision, Decimal Digits	4.3	4.3	4.3	4.3	4.3
Real Time Clock	Opt	Opt	Yes	Yes	Yes, 2 std
Resolution	—	10/100 $\mu$ sec, 1/10 msec	10 Hz	—	—
Control Memory	—	No	Yes + WCS	ROM	—
Size, wds (min/max)	—	—	1,528	512	—
Word Length, bits	—	—	64	64	—
Cycle Time, nsec	—	—	NA	NA	—
Processor Cycle Time, $\mu$ sec	—	—	NA	NA	—
APL	—	—	—	Yes	—
	Bootstrap loader (ROM)	Bootstrap loader	Bootstrap loader	Yes	—
<b>WORKING STORAGE</b>					
Technology	Semiconductor	MOS	Core; MOS(1)	Core (2 speeds); MOS	Core
No. of Ports	4	4	1 or 2	1 or 2	1
Main Memory Capacity, (min/max, bytes)	16K-128K	16K-128K	16K-512K with mapping	131K/512K	16K-128K
Core Cycle Time, $\mu$ sec	—	—	1.2; 0.66; 1.2	0.660; 0.990	0.800
Solid State Memory	Yes	Yes	MOS(1)	MOS	No
Real Time, $\mu$ sec	—	—	—	—	—
Cycle Time, $\mu$ sec	0.750	0.750	0.330	0.330	—
Error Control	6 bits/wd, auto correct checking	6 bits/wd, auto correct	Parity, 1 bit/byte	Parity opt; 1 bit/byte	Parity; 1 bit/byte
Memory Protect	Yes	Yes	Std (V-74); opt (V-72/73)	Yes, in pgs of 512 wds	Yes
Memory Management	—	—	—	Yes	No
Cache Memory	No	No	No	No	No
Size, (min/max, wd)	NA	NA	NA	NA	NA
Cycle Time, $\mu$ sec	NA	NA	NA	NA	NA
<b>I/O CHANNELS</b>					
P/O	CRU register	Yes	Std	Yes, firmware	IOP
Width, bits	16	16	16	16	8 or 16
No. of Devices	256 (8K lines)	4 256 ports	64	64	28
Max Xfer Rate, bytes/sec	Software dependent	—	Software dependent	—	940K
DMA	Yes, up to 6 channels	Yes	Std	Yes	Opt
Width, bits	16	16	16	16	16
No. of Devices	6	1-8 ports	765K	64	2
Max Xfer Rate, bytes/sec	2.6M	1M	3.0M (PMA Cos) 6.6M (PMA MOS)	66M std; 2M (high speed); 6M (PMA)	850K
Other (type; xfer rate, bytes/sec)	—	—	—	—	—
<b>SOFTWARE</b>					
Types of Op. Sys.	PSM, PAM	Basic System, DX980	BEST, VORTEX I/II, MOS	VORTEX II, BEST, MOS	BCM, RBM
Languages	SAL; PCL/A; FORTRAN, TILT	FORTRAN IV, BASIC/980, SAPG, Assembler, TILT	DAS, FORTRAN IV, BASIC, RPG IV	FORTRAN IV, RPG II, Compiler, BASIC, DAS	FORTRAN IV, Satellite, IDEN, COBOL, RPG
Communications	NA	NA	VTAM	VTAM	—
<b>I/O DEVICES</b>					
Fixed-Head Discs (capacity, bytes)	1.3M 3.6M/drive	500K-3.6M/drive	122K-982K	122K-982K	0.75M-6.2M/drive
Disc Cartridges (capacity, bytes)	2.2M-4.5M/drive	2.2M/drive	2.34M/4.6M/drive	2.34M/4.6M/drive	2.3M/4.6M/drive
Disc Pack (capacity, bytes)	100M/drive	100M/drive	29M-934M/drive	29M-93.4M/drive	49M-86M/drive
Floppy Discs (capacity, bytes)	NA	NA	NA	NA	NA
Magnetic Tape (type)	9-trk; 800 bpi; 37.5 ips	9-trk; 800 bpi; 37.5 ips	9-trk; 800 bpi; 25-37.5 ips	9-trk; 800 bpi; 25-37.5 ips	7-9-trk; 37.5-150 ips; 200, 556, 800, 1,600 bpi
Cassettes (capacity, bytes)	NA	NA	NA	NA	NA
Punched Card (type; speed cpm)	Reader, 300	Reader, 300	Reader, 300; punch, 35	Reader, 300; punch, 35	Reader, 200-1,500; punch, 100-300
Paper Tape (type; speed cps)	Reader, 75; punch, 300	Reader, 300; punch, 75	Reader, 300; punch, 75	Reader, 300; punch, 75	Reader, 300; punch, 120
Printers (speed, lpm; col)	165/330 cps, 356 lpm; 132 cols	165/330 cps; 356 lpm; 132 cols	245-1,100 lpm; 132 cols	245-1,100 lpm; 132 cols	225-1,500 lpm; 132 cols
Data Comm	Async	Sync, async	Sync, async	Sync, async	Sync, async
Xmission Rates	110-9,600 baud	110-9,600 baud	2,400/50,000 baud; up to 9,600 baud	Up to 9,600 baud	To 230K bps; 45-2,400 baud
<b>COMMENTS</b>					
	PSM = programming support monitor. PAM = process automotive monitor.		(1) Dual ports and MOS for V-73 and V-74	(1) Three times are for 330-nsec MOS/660-nsec core/990-nsec core	Xerox is no longer active in the computer field.
—	Not Applicable				
NA	Information Not Available				





73-1502

### OVERVIEW

The Cincinnati Milacron CIP/2000 Series offers three minicomputer models, the CIP/2003, the CIP/2100, and the CIP/2200. The CIP/2003 is an open frame version of the CIP/2100. The CIP/2100 comprises a maximum memory of 16,334 words with a 1.1-microsecond cycle time per word and 88 standard instructions. The CIP/2100 was first delivered in 1970. To date 310 systems have been installed. The CIP/2200 offers all of the features of the CIP/2100 plus additional features such as 119 standard instructions and decimal arithmetic. Over 139 CIP/2200 systems have been installed since its first delivery in February 1972. The differences and similarities between the two processors are outlined in Table 1.

Cincinnati Milacron markets its systems to both OEM and small end-users. They are particularly good for business systems that require decimal arithmetic. Cincinnati Milacron has incorporated their minis into several Milacron numerical control products, which have been traditionally strong applications for the company.

Cincinnati Milacron's product line has evolved from a basic CIP/2000 processor which was introduced in 1970. The CIP/2000 was basically a microprogrammed controller with expansion capabilities.

In addition to its standard products, Cincinnati Milacron will produce a customized system on order. The major software package for the 2200 is CIMOS-22, a single user disc operating system.

### System Performance and Competitive Position

The CIP/2100 and CIP/2200 are geared toward the OEM house or smaller end-user. Cincinnati Milacron has been an innovator primarily in the

numerical control and machine tool industries. The company also produces customized systems to interface with their machine tools.

Several users of Cincinnati Milacron machines were interviewed for this report and their comments follow.

One CIP/2100 system, now 2 years old, is used in a communications network. This user reported some initial trouble with the I/O control, DMA, modem interfaces, and CPU board, but Cincinnati Milacron solved these problems and the system is now very reliable. This particular user chose the CIP/2100 because of the ROM implementation, I/O structure, and instruction set. The user also suggested some possible improvements to the system. The console lamps on the CIP/2100 are soldered rather than socket connected. When lamps are soldered in place, the computer must be down to change a console light. There was some difficulty aligning the motherboard and chassis, but these difficulties have not prevented this user from purchasing 20 systems.

Another user has 15 CIP/2200's being used as data collection devices on point-of-sales systems. This user liked the quality of the unit and the support provided as well as the ROM-implemented instruction set, although he felt that the cost could be a little less. This user has had no downtime since the system has been in operation. Minimal problems were experienced during engineering and development periods. This user felt the machines could be a bit faster, but he plans to stick with Cincinnati Milacron because of the software investment involved.

A third user has a CIP/2200 scheduling traffic, preparing logs, and billing for radio and television stations. This user feels the system has a good instruction set and finds it extremely reliable. The basic assembly language is good. This user also appreciates the byte and bit orientation of the machine. Downtime is negligible with a 4 hour maintenance turn-around time. Cincinnati Milacron has developed a deferred purchase payment plan for several of its users to alleviate the burden of the large initial investment for computer system development. The CIP/2200 compared favorably in price with Data General, Digital Equipment Corporation, General Automation, Computer Automation, and Hewlett-Packard. This user has 17 more systems on order.

A service bureau uses a CIP/2200 for data processing and software development. This service bureau found the CIP/2200 to be the

Table 1. CIP/2100, 2200: Processor Characteristics

Characteristics	CIP/2100	CIP/2200
Announced	1970	1972
Models	2100	2200, 2210*
Memory		
Type	Core	Core
Word length (bits)	16	16
Cycle time/word ( $\mu$ sec)	1.1	1.1
Capacity (bytes)		
Min	8192	8192
Max	32,768	32,768
Increment	8192	8192
Parity	Opt	Opt
Protect	Opt	Opt
ROM	768 words	1536 words
Use	TTY controller, bootstrap loader, DMA block I/O feature, instruction set extension	TTY controller, bootstrap loader, DMA block I/O feature, instruction set extension
Central Processor		
No. of internal registers	5	5
Use	1 indexable	1 indexable
Number of instructions		
Standard	88	119
Optional	—	—
Fixed-point arithmetic		
Add/subtract	Binary	Binary, Decimal
Multiply/divide	Binary	Binary, Decimal (step)
Add time ( $\mu$ sec)	5.06	11.7
Floating-point arithmetic	N/A	Available with RPG software
Addressing		
Direct (no. of words)	256	256
Indirect	1 level (all of memory)	1 level (all of memory)
Indexed	Yes (all of memory)	Yes (all of memory)
Max no. I/O devices	32	32
Priority Interrupt System		
Lines	7	7
Internal	6	6
External	64	64
I/O Channels		
Programmed I/O	Byte I/O, Serial I/O	Byte I/O, Serial I/O
Direct memory access	Yes	Yes
No. of channels	2	2
Multiplexed I/O	Yes (Firmware)	Yes (Firmware)
Max. transfer rate (bytes per second)		
Within memory	50,000	86,000
Over DMA	910,000	910,000

\*Includes disc IPL ROM.

most reliable machine it has come across, as compared to the IBM System/3, IBM 360/20, and the Honeywell 200. This user feels the CIP/2200 has a powerful interactive operating system. This installation has run for 16 hours a day for 4 months with no downtime at all. The only serious problem involved a faulty 80-column card reader, and Cincinnati Milacron has since changed their card reader manufacturer. This user would like a remote control panel with a CRT and an 80-column card punch available for the system. This service bureau compared the CIP/2200 with a small DEC PDP-11, a Data General Nova, and Digital Computer Controls 116 before choosing the 2200.

Each user commented on the excellent service and maintenance from Cincinnati Milacron. Company response to a problem has been rated excellent by all of the users interviewed.

#### Compatibility

The CIP/2100 is upward compatible with the CIP/2200.

#### Configuration Guide

The CIP/2100 processor includes six operational registers, 768 words of ROM (read-only-memory), a basic console and cabinet, a control board, two data boards, and a power supply. Three input/output facilities are provided: a serial Teletype interface, DMA capabilities, and a byte I/O bus. Additional ROM memory, eight- or nine-bit core memory, a real-time clock, power fail/auto restart, memory parity, memory protect and three control panel styles are available as options. The CIP/2003 is a stripped chassis version of the CIP/2100.

The standard CIP/2200 system includes a basic console and cabinet, a control board, two data boards, a system control panel interface with motherboard, and a power supply. It utilizes microprogramming to implement the serial I/O controller (TTY interface), a bootstrap loader, and a high speed Direct Memory Channel block I/O feature. The Teletype interface, DMA capabilities, and byte I/O bus are also featured on the CIP/2200. Power fail/automatic restart, memory parity detection, an internal timer, and a disc initial program load microprogram are processor options.

Main memory utilizes eight- or nine-bit word core modules with a 1.1 microsecond cycle time per word. The optional ninth bit is a parity bit. Memory modules are available in 4K or 8K byte modules. Sixteen general purpose eight-bit file

registers and memory addressing to 32K bytes are included with the CIP/2200.

The CIP/2200 I/O structure makes four types of I/O transfers available to the user. A micro-programmed serial I/O facility operates at 10 characters per second as a standard interface for a low speed terminal device. Program loop or interrupt I/O capabilities for medium speed devices are provided by a byte I/O facility. Firmware implements a Direct Memory Channel to transfer blocks of data from external devices at a rate up to a total of 25,000 bytes per second without degrading the internal interrupt system response time, but data rates up to 86,000 bytes per second with buffered I/O devices do produce correspondingly longer response time to internal interrupts. Two Direct Memory Access Units can be connected to a system: Each unit is an independent hardwired controller and can transfer data at up to 910,000 bytes per second by competing with the CPU for memory cycles.

The control panel is available in three styles. The basic panel includes all operational switches. A blank control panel incorporates a power socket jumper only. The System Control Panel version is a basic panel extended to include data entry switches and data lights.

#### MAINFRAME

The CIP/2200 is a byte-oriented processor that utilizes a control stack to implement state switching. Storing and removing register values from the control stack accomplishes subroutine linkage and interrupt switching. The control stack saves the Program Counter (P), machine status byte (S), and the B, A, and X registers.

#### Central Processors

The CIP/2200 processor uses an eight-bit wide data path and an eight-bit memory word, although the CPU registers are 16 bits in length. Microprogramming allows more powerful instructions for user applications and functions. The Serial I/O controller and DMA block feature are micro-programmed as is the bootstrap loader. Custom system extensions can also be microprogrammed.

Processor options include power fail and automatic restart, memory parity error detection, an interval timer, and a disc initial program load (IPL) microprogram. The interval timer is a 16-bit counter decremented at 1-millisecond intervals. The timer generates an internal interrupt when the counter reaches zero.

Interrupts are also caused by the power fail and memory parity options. The disc IPL is a

firmware routine used to minimize the basic bootstrap load time. The loader moves up to 32K bytes of core image data from disc to memory with a control transfer to a specified location to load the remaining software. The disc IPL loads 32K bytes in less than 220 milliseconds. See Table 1 for an outline of processor characteristics.

**Data Structure.** Cincinnati Milacron machines are byte-oriented minicomputers with bit manipulation and decimal arithmetic capabilities. Character strings are represented by byte strings up to 256 bytes long. Decimal data can be manipulated as input to eliminate packing and code conversions. Decimal numbers can be up to 16 digits long. A summary of the data formats used for the Cincinnati Milacron machines is outlined in Table 2.

Table 2. CIP/2100, 2200: Data Formats

Data Name	Representation
Byte	8 bits
Word	8, 16, 24, 32 bits
Instructions	8, 16, 24, 32 bits
Decimal Operand	Zoned format byte strings up to 16 ANSI digits in length
Binary Operand	16 bits — fixed length; 8, 16, 24, 32 bits — variable length
Floating Point Operand	Opt (available on CIP/2200 with RPG software)
Strings	Up to 256 bytes

**Special Registers.** The CIP/2200 CPU has three programmable registers: the Accumulator (A), Accumulator Extension (B), and an Index Register (X). Two other registers are used as the Program Counter (P) and the Status (S) register.

- A Register — 16 bits, the operand source location for all binary arithmetic and logical instructions.
- B Register — 16 bits, accumulator extension for variable length binary arithmetic and logical operations; byte mode I/O operations may transfer data to or from the low eight bits of this register.
- X Index Register — 16 bits, used for address modification and base relative ad-

ressing; several instructions are provided for index value modification.

- P Register — 16 bits, Program Counter, contains address of next machine instruction to be executed; contents are stored by subroutine transfer instructions.
- S Register — eight bits, contains CPU internal status indicators.

**Instruction Set.** The CIP/2100 offers 88 standard instructions while the CIP/2200 includes 119 instructions. The instruction set can be extended through microcoding and a 256-byte page of ROM. The CIP/2200 instruction set is divided into the following classes: 14 arithmetic instructions, three moves, 41 register operate, 12 shifts, eight I/O instructions, 19 control transfers, six character string manipulation instructions, 13 control instructions, and seven memory immediate instructions. Bi-directional string moves allow up to 256 bytes of data to be moved by one instruction. Memory to memory moves do not alter the register contents. Table 3 lists some typical instruction execution times.

**Addressing Facilities.** The CIP/2200 can address up to 32,768 bytes of core. The basic addressing mode is extended addressing, which utilizes a 16-bit address word. The 15 least significant bits contain the address while the most significant bit specifies indexing. Direct or single level indirect addressing is to page zero or to the page containing the instruction. A page is 256 bytes long. Index, index plus displacement, literal, and extended indirect are the remaining address modes.

**Interrupt Control.** The priority interrupt system can include internal interrupt levels and 64 external interrupt levels. Internal interrupts are caused by an operational fault, a console interrupt, a high priority event, or the internal timer. External interrupts are generated by an I/O device or some external device. Each interrupt level has its own address pointer in main memory that points to the address of the service routine. Interrupts are executed on a priority basis with internal interrupts rating the highest priority. External interrupt priorities are determined by the device controllers physical placement in the chassis. The program can disable the external interrupts.

#### Main Memory

Main memory is composed of 8192-byte magnetic core modules with a cycle time of 1.1 microseconds. Memory maximum size is 32K bytes. Memory is arranged in eight-bit bytes

Table 3. CIP/2100, 2200: Typical Instruction Execution Times

Instruction Type	Typical Execution Time (microsec)	
	CIP/2100	CIP/2200
Load and Store	*	12.1/11.2
Fixed Point Binary		
Add	*	11.7
Multiply	*	614.9 per two 16 digit numbers
Fixed Point Decimal		
Add	*	84.5 + 7.5 per digit
Multiply	*	Subroutine *
Floating Point		
Add	N/A	— (opt)
Multiply	N/A	— (opt)
Logical	*	Register 6.4; memory 12.1
Branch on condition	*	11.4/12.8
Shift	*	3.3 per bit position
Compare logical character	*	55.4 + 8.6 per character
Move character	*	67.7 + 5.5 per character
I/O	*	Byte from register 8.4; byte from memory 14.5
Misc	*	—
—		Not applicable
N/A		Not available
*		Information not supplied by manufacturer

with an optional ninth parity bit. No storage protection is available. Approximately 256 bytes of storage are reserved for vectored interrupts and DMC buffer pointers.

#### I/O Control

The instruction word can address 32 peripheral devices. Three types of I/O channels are provided: serial I/O, byte I/O bus, and DMA. The serial I/O channel interfaces to a teletype unit and transfers data 10 characters per second.

A Direct Memory Access Unit, implemented by firmware, allows multiplexed block I/O transfers by way of the byte I/O bus. Multiplexed transfers up to an aggregate transfer rate of 25K bytes per second do not degrade the interrupt system's response time. Higher aggregate transfer rates do begin to degrade the interrupt system's response time. Two DMA channels are available to provide a maximum aggregate transfer rate of 910,000 bytes per second CPU. The hardwired DMA Units transfer data on a cycle stealing basis.

Seven slots are available in the processor chassis with 17 more slots available in an expansion chassis. Each controller occupies one chassis slot.

#### PERIPHERALS

Cincinnati Milacron offers a variety of peripherals for the CIP series. The low speed devices include Teletypes, paper tape and punched card equipment, and printers. See Table 4.

High speed peripherals include a disc system and a magnetic tape system. See Table 5.

A Multiplexor, a CRT, and an I/O Driver with Receiver are available for use with the CIP/2200. These devices and their characteristics are presented in Table 6.

#### DATA COMMUNICATIONS

The CIP/2100 and CIP/2200 support a variety of communications devices. See Table 7.

Table 4. CIP/2100, 2200: Low Speed Peripherals

Device	Characteristics	Comments
Teletype		
3000 ASR-33 Teletype	10 cps	
3007 RO-33 Teletype	10 cps	
Paper Tape		
Reader/Punch	300/75 cps, uses 8-level code	Uses 1-inch wide tape.
Punched Card		
3013 Reader	600 cpm, 80-col, with interface	
3018 Reader/Punch	96-col, 300/60-120 cpm, without keyboard; 600-400 card inputs; 600-600 card outputs	Fully buffered input/output.
3019 Data Recorder	96-col, with keyboard and interface	
3020 Data Recorder	96-col, stand-alone, with keyboard, and without interface	
Printers		
Line Printer	200 lpm, band printer, 64 char set, ASCII, 132 col, 10 cpi, 6 lpi	
3014 Line Printer	60 lpm, 132 col, 64 char ASCII set, original plus 5 copies, includes interface and cable	
3015 Printer	165 cps, 125 lpm, 132 col, 132-char buffer, 64-char ASCII set; original plus 4 copies	

Table 5. CIP/2100, 2200: High Speed Peripherals

Device	Characteristics	Comments
Disc		
3037 Disc Drive	Capacity 5M bytes; 24 sectors/track; 1 fixed and 1 removable disc; avg access time 55 msec; transfer rate 195K bytes per sec	Requires 3031 controller.
3038 Disc Drive	Same as 3037 except 10M-byte capacity	Requires 3031 controller.
Magnetic Tape		
3028 Mag Tape Unit	7- or 9-track; 800 bpi, includes interface and cable; read-after-write; 25 ips; 14.4-msec start/stop time, 1800 bytes/sec, 10-1/2 inch reels	Requires 3017 formatter.

Table 6. CIP/2100, 2200: Special Purpose Peripherals

Device	Characteristics	Comments
2705 MUX	4-byte Multiplexor I/O, outputs independently latched, outputs and inputs are std DTL or TTL logic with capability to interface with virtually any peripheral device not covered by peripheral controllers	Expands 8-bit I/O bus into 4-byte I/O under processor control.
CRT	74 char/line, 27 lines, 5 x 7 dot matrix, full cursor control, fully buffered, full alphanumeric keyboard plus numeric pad and control keys	
2700 I/O Line Driver and Receiver	Allows integration of up to 12 peripheral interfaces under program control or concurrent data transfer with interrupt	Expands internal I/O bus to an external bus.

Table 7. CIP/2100, 2200: Data Communications Devices

Device	Characteristics	Comments
2706 Asynch Controller	6 channels; full-duplex; odd/even parity; 5/6/7/8 bits/word; 110 to 4800 bps	
2708 Serial Controller	1760 baud	
2709 Serial Controller	2400 baud	
2801 Synch Modem Controller	For Bell 201/A-3 or equivalent sets; operates with point-to-point or switch networks for either 2- or 4-wire service; half- or full-duplex; byte data transfers under concurrent I/O or programmed control; interface levels EIA std RS232B; 1200 to 9600 bps	
2802 Multi-Asynchronous TTY Controller	*	
2803 Multiple RS232 Interface	*	

Table 7. (Contd.)

Device	Characteristics	Comments
2804 Asynch Modem Controller	For Bell 103/202 data sets; 110, 134.5, 150, 300/1200 bps	

\*Information not available from manufacturer

## SOFTWARE

Cincinnati Milacron offers two operating systems for the CIP/2200: the Paper Tape Operating System (PTOS) and the Cincinnati Milacron Operating System (CiMOS-22). PTOS requires 8K bytes of main memory. It supports an assembler, Library Maintenance Program, Dynamic Debug System, and System Generation Program. CiMOS-22 requires 16K bytes of memory, a disc, and a Teletype. CiMOS-22 supports an RPG compiler and an assembler.

Both operating systems can handle four discs, four tape drives, one card reader, one line printer, and one Teletype.

### CiMOS-22

CiMOS-22 is the major software package available for the CIP/2200. It is a disc-resident operating system that functions with one user acting as both programmer and operator. CiMOS-22 processes one job at a time. The initial release of CiMOS-22 includes a job control language to debug programs, a 2-pass relocating assembler, an RPG II compiler, a linkage editor to permit overlay structures, a text editor to create and modify source files, and a system generation program. Utilities include disc initialization, disc reorganization, catalog list, library maintenance program, file copy, duplicate disc, and disc sort.

A basic configuration of CiMOS-22 uses the first 8K bytes of core. The language processors require at least another 8K bytes of core. System modularity allows various components to be made core resident at System Generation. This option improves throughput but requires at least 24K bytes of core. CiMOS-22 is distributed on a disc pack as a starter system used to develop the completed system at system generation. This allows the user to tailor the system to his needs.

Job Control Language. User-system communication and control is maintained through the system console. The Job Control Language prints a command request when the system is

loaded. The user can perform the following functions in the area of program execution:

- Create or delete a disc file.
- Change file names and file protection.
- Catalog a file or remove it from the catalog.
- Set the system time and date.
- Set user switches as required.
- Execute a selected program.
- Specify options to be in effect during program execution.
- Define new option keywords.
- Cancel a job.
- Assign reference file names to actual files.

The user can also utilize JCL as an on-line debugging system with the following functions:

- Display, with the option of changing the contents of the A, B, X and S register and specified main storage locations.
- Display extended areas of main storage.
- Display address of entries in the user symbol table.
- Perform hexadecimal arithmetic, giving both sum and difference of two operands.
- Load a program and test it.

The JCL permits the user to execute program and utility functions in any sequence with the option of changing that sequence when necessary.

Relocating Assembler. The assembler (ASM/2200) is a 2-pass, disc-oriented component of the CiMOS-22 system, available in either an 8K- or 12K-byte version. The 12K-byte version offers an increase in throughput because more



modules are core resident. Both assemblers produce a relocatable object module as output. The assembler furnishes a printed listing of the source code, machine code representation, and error diagnostics. A series of pseudo instructions is included in addition to the symbolic assembler instructions.

RPG II. The CiMOS-22 RPG compiler accepts source statements from cards, disc, or tape and converts them to machine language object code. RPG II requires the following specifications to process a job:

- Control card and file description specifications.
- Extension and line counter specifications.

- Input specifications.
- Calculation specifications.
- Output specifications.

Other Software. Other operating system modules include a Linkage Editor, Text Editor, and System Generation Program. Utilities are also available and comprise disc and file utilization commands, debugging aids, and a library maintenance program.

#### HEADQUARTERS

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## COMPUTER AUTOMATION INC. LSI Series System Report



74-52

MaxiBus<sup>®</sup>, a registered trademark of Computer Automation, Inc.

### OVERVIEW

Computer Automation's LSI Series consists of low-cost 16-bit, microprogrammed minicomputers aimed exclusively at the OEM market. Like their predecessors, Naked Mini-16 and Alpha-16, the LSI Series is packaged in "naked" versions without power supply or console, as well as in "alpha" versions with these features. All are microprogrammed and organized around a Maxi-Bus<sup>®</sup> with at least three major I/O subsystems: DMA, direct memory channels, and programmed I/O. All LSI Series computers except the 3/05 also have block transfer I/O capability.

The LSI Series uses two basic processors. LSI processor 3/05 uses bipolar MSI technology and is mounted on a half-size 7 x 15-inch board. It competes with microcomputers and small minicomputers. The LSI-2 systems all use the same TTL MSI processor, although the processor cycle time for the Model 2/10 is half that of the 2/20 or 2/60. The 2/60 is the MEGABYTER system, allowing attachment of up to one million bytes of memory. Thus, the line extends across the whole range of the minicomputer market.

All models have the same basic architecture, same number of registers; same priority interrupts; same word or byte addressing using eight addressing modes; same 4K/8K/16K-word core memory modules; same combination modules of RAM, ROM, and PROM; and so on. The chief differences are in speed, instruction set, and memory capacity. Table 1 lists characteristics common to all models.

The LSI-2/60, or MEGABYTER, added to the line in 1975, extends the capabilities of the LSI-2 line upward by adding instructions optimized for real-time, multiprogramming, communications, and business applications and by expanding memory capacity to one million bytes in 32K-word memory banks. The MEGABYTER uses the same processor as the rest of the LSI-2 line, thus it can use all the peripherals and software developed for other LSI-2 models. The LSI-2/60 implements the following facilities in addition to those available for the LSI-2/10 and 2/20:

- Expansion of the 2/20's stack processing capabilities.
- String instructions that can move up to 255 bytes at a time, can compare strings, and can move mismatched characters.
- Decimal arithmetic for adding and subtracting up to 31 digit strings.
- Bit manipulation; direct addressing to the bit level.

CRC (cyclic redundancy check), character generation, hardware multiply/divide, and interleaved memory are standard features.

The NAKED MILLI LSI-3/05, also added in 1975, uses the same basic architecture as the LSI-2 Series; but the processor is different, with a cycle time that is somewhat slower. The LSI-2 Series uses a faster processor and either 960-nanosecond or 1,200-nanosecond memory modules. Although LSI-3/05 uses the same 1,200-nanosecond memory as the LSI-2 Series the processor slows instruction execution time. Thus, execution time for an add or subtract instruction is 6.0 microseconds on the LSI-3/05, 2.4 microseconds on the 2/10, and 2.06 microseconds on the 2/20 and 2/60. The 2/10 uses the same processor as the 2/20 and 2/60, but cycle time is halved.

LSI-3/05 is designed with bipolar MSI circuitry and TTL logic to produce a compact, low-cost system. However, the NAKED MILLI is still upward compatible with the LSI-2 line and can attach the same peripherals and interfaces as the larger systems. Programs developed on LSI-2 systems can run on the LSI-3/05 by using subroutines for missing instructions. Table 2 lists the differences among the LSI Series models.

### HEADQUARTERS

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**Table 1. CAI LSI Series: Common Mainframe Characteristics**

Characteristics	LSI Series
<b>CENTRAL PROCESSOR</b>	
General-Purpose Registers	8
Addressing	
Direct	768 words or bytes
Indirect	Multilevel, to 32K wd or 64K bytes/level; 128K wd max
Indexed	Yes
Floating-Point Arithmetic	No
Priority Interrupt Levels (std; max)	5; 256
<b>MAIN STORAGE</b>	
Type	Semiconductor; core; mixed
Cycle Time (μ sec)	0.96; 1.2
Basic Addressable Unit	Word or byte
Increment Sizes (bytes)	8K, 16K, 32K (core); 1K, 2K, 4K, 8K (MOS)
Memory Parity	Opt
Memory Protect	No
ROM	Yes
RAM	Yes; can be mixed with core
I/O Transfer Rate	
DMA (wd or bytes/sec)	625,000 (1.25M with interleaved memory)
Programmed I/O	34,247 via registers
Programmed (wd or bytes/sec)	24,631 direct to memory
Direct Memory Channels (wd or bytes/sec)	26,738
No. of DMA Channels (std; opt)	2; 64
Conditional I/O Devices	Std 248

Computer Automation (CAI) was formed in August 1967 to manufacture and market minicomputers to the OEM market. Since its introduction of the Alpha and Naked Mini Series and the later LSI versions, the company has shipped more than 9,000 systems. It also produces and markets the Capable Tester System; this computer-driven production line tester for digital logic modules was originally designed for CAI's in-house logic production facility.

The Capable Tester line includes 12 models ranging from test-only models to systems that provide computerized design of test programs using a new simulation software system called BigSim. BigSim is a preproduc-

**Table 2. Differences Among LSI Series Systems**

Model Number	3/05	2/10	2/20	2/60
No. of Instructions	95	162	182	224
Stack Processing	No	No	Yes	Yes
Instructions				
Block Transfer I/O	No	Yes	Yes	Yes
Main Memory				
Min Size wd	256	4K	4K	8K
Max Size wd	32K	256K	256K	512K

tion simulator that builds, refines, and verifies test programs from engineering designs of circuit boards with up to 400 integrated circuits. The models in the mid-range of the Capable Tester line are based on an LSI-2 with 16K words of memory; models using BigSim incorporate a disc-based LSI-2 with a 64K-word memory.

Computer Automation has expanded steadily and now has 18 direct sales offices and service facilities in the United States. A number of distributors market CAI systems in other parts of the world; D.C. Industries in Australia; the Metric companies (Scandia Metric AB in Sweden, Finn Metric oy in Finland, SC Metric A/S in Denmark, and Metric A.S. in Norway) in the Scandinavian countries; Geveke Elektronica en Automatie nv in Belgium, Netherlands, Luxembourg, and Germany; Data Care AG in Switzerland; Tranchant Electronique in France; Computer Advances in South Africa; Alfa-tronica in Spain; and Electro Marketing in Japan. Computer Automation has its own subsidiary, CAI Ltd, in England for sales to the United Kingdom and for support in certain parts of Europe.

Peripherals for the LSI Series include discs, diskette, magnetic tape, printers, card reader, paper tape reader and punch, process I/O, and communications. The new distributed I/O interface can support up to eight intelligent cables, which can connect to a variety of peripherals. These programmable interfaces let users simplify interfacing to any serial or parallel I/O device.

Software for the LSI-2 Series includes DOS, COS, and MOS batch operating systems, BASIC, ALGOL, FORTRAN IV, and assembly language processors. A real-time executive (RTX) allows multiprogramming. An optimized version of the FORTRAN IV compiler, designed to produce more compact object code, was introduced in 1975 at the same time as the MEGABYTER and LSI-3/05 NAKED MILLI.

Software for the LSI-3/05 includes the RTX, an I/O executive (IOX), the OMEGA conversational assembler/editor, loader utilities, and a debug package. Programs developed under DOS on the LSI-2 can usually run on the LSI-3/05 without difficulty.

**PERFORMANCE AND COMPETITIVE POSITION**

The LSI Series extends across the entire minicomputer market, thus its members compete with different systems in different market segments. This has not always been the case. Former CAI systems, represented now by the 2/10 and to some extent the 2/20, tended to compete at the low end of the minicomputer market with the low and middle portions of the Data General Nova or the Digital PDP-11 lines, for example. The minicomputer market has now expanded, both downwards and upwards; and the LSI line has done likewise.

Computer Automation has a competitive advantage over minicomputer manufacturers who sell both to end



users and in the OEM market. Computer Automation sells only OEM, and customers are not concerned about the company becoming a competitor. Also, primarily as an OEM supplier, Computer Automation stresses thorough testing of system components, as well as reliability in meeting production deadlines and living up to contractual obligations.

Although Computer Automation entered the field only 7 years ago, the company grew rapidly until last year when its steady growth rate was slowed somewhat due to the unfavorable economic climate. Expansion of its product line at both ends and the new I/O interfacing has provided other markets for CAI systems and spurred a return to near previous growth levels. The company has delivered 9,000 systems and expects to hit a 10,000 figure in the last quarter of 1975.

The LSI-2/60 MEGABYTER expands the LSI-2 line upwards; it provides an upward path for current customers and should also attract new customers on its own merit. Its new instructions and the million-byte memory capacity make it suitable for large communications, data entry, real-time, or other multiprogramming systems capable of considerable expansion. The range in the instruction set, I/O structure, and memory capacity allow it to compete with the Digital PDP-11/45, Data General ECLIPSE, and Interdata 7/32 and 8/32. These companies sell their systems in OEM as well as end-user versions.

MEGABYTER does not perform memory mapping; instead, programs execute out of a 32K-word memory bank. An instruction is used to switch from one bank to another. Memory protect and hardware floating-point arithmetic are currently unavailable. The Universal Interface should save many OEM manufacturers considerable time and money in system building. The MEGABYTER is particularly suited to control multiterminal distributed processing systems for data entry, accounting, and text editing.

The Computer Automation LSI-3/05 NAKED MILLI occupies an intermediate position in the computer market, between microprocessors and minicomputers. Like microprocessors (the computers-on-a-chip), the 3/05 was designed to be a component. Even the power supply and console are priced separately. Like minicomputers, the LSI-3/05 Series has systems software so the user can quickly implement applications.

Microprocessors range in size and capability from the Intel single chip to National Semiconductor's four-chips-on-a-board. Some manufacturers provide only chip sets, leaving the user to provide I/O, interface logic memory, and programs. Others provide board-level systems that include memory and ease the I/O interfacing problems but rarely provide standard interfaces to peripherals other than Teletypes.

The big advantage of the CAI minicomputer lies in its completeness: memory, peripherals, and software. For

many applications the LSI-3/05 costs the same as or less than an in-house developed microcomputer, and implementation of the total system would be faster with the LSI-3/05. The distributed I/O subsystem option supports the concept of quick and easy interfacing. In addition, the user of an LSI-3/05 can move up to the compatible LSI-2 Series if requirements outstrip the LSI-3/05 processor capability.

The NAKED MILLI LSI-3/05 has several competitors from minicomputer makers also trying to extend market penetration downward. Digital has used the Intel microcomputer in its MPS system, which is not compatible with the PDP-8 or PDP-11 lines.

Digital has also introduced a bottom-of-the-line PDP-11 and PDP-8. The LSI-11 is a 1-board system with RAM memory and a 2-board system with core memory. The PDP-8/A is a compact 1-board CPU that is implemented with MOS technology. Both the PDP-8/A and LSI-11 are more expensive than the LSI-3/05.

Data General's Nova 2 is sold at the board level. It is faster than the LSI-3/05 and also more expensive.

## User Reactions

A manufacturer of blood serum analyzers bought about 200 CAI LSI units as components, partly because of the price but largely because the 1-board CPU means simpler maintenance. The CAI computer is used for mathematical analysis of chemical reactions and for printing reports for doctors. The analyzers are controlled by another computer system. This user is very pleased with the performance of the system; CAI's support has been very good, and response to service requests is prompt. The user made only one criticism; he feels the programming manuals could be improved.

A second user is a prominent POS manufacturer using the system as a ROM simulator and a testing device for customized ROM units. The LSI-2 is programmed with the desired logic pattern, and the pattern is then tested before it is fused into ROM firmware by another system. The resulting chips are then retested by the CAI unit. The company bought 15 of the LSI-2 systems and is now using some as field trial units. This manufacturer has found the mini to be an excellent machine with a very good capacity. He likened it to a Nova system, with capabilities somewhere between the Digital PDP-8 and PDP-11.

A department in a communication equipment manufacturing facility bought a single LSI-2 with an 8K-word memory and a Teletype for an in-house machine control application. The department chose the system over Digital and Hewlett-Packard systems for three reasons: price, I/O structure, and the fact that a neighboring department had one.

This communication equipment user has had no problems whatsoever with his system, so he was unable to

**Table 3. CAI Peripherals**

Model No.	Description
<b>DISCS</b>	
22530	Moving Head Disc Subsystem; 1 fixed, 1 removable cartridge; 2.46M wd/drive; 4 drives/controller
22566	Floppy disc; 243K bytes/disc; dual drive; 2 dual drives/controller
<b>TERMINALS</b>	
22205-00	Teletype ASR 33-20/3JC; 10 cps A/N Display; 1,920 char, 24 x 80 char; 64-char set; to 9,600 baud
22230-00	
<b>PUNCHED CARDS</b>	
22077-20	285-cpm reader
<b>PAPER TAPE</b>	
22223-11	300-cps reader
22223-60	300-cps reader; 75 cps punch
<b>PRINTERS</b>	
22107-06	100 cps printer (60-150 lpm); 80 col
<b>MAGNETIC TAPE</b>	
22224-15	9-track; 800 bpi; 25 ips; 4 drives/controller Single/dual cassette drives; 520K bytes/cassette; 4 drives/controller
<b>PROCESS I/O</b>	
13213-00	Digital I/O; 16-bit DTL/TTL compatible
13214-20	Relay Output Module; 32-bit (1 x 32, 2 x 16, or 4 x 8)
13215-00	Relay Input Module; 32-bit (1 x 32, 2 x 16, or 4 x 8)
13216-00	Output Module; 64-bit (1 x 64, 2 x 32, 4 x 16, or 8 x 8)
13218-00	Input Module; 64-bit (64-, 32-, 16-, or 8-bit inputs)
14223	Utility I/O; 8- or 12-bit-parallel input or output
<b>COMMUNICATIONS</b>	
14236	Single or Dual Interface for 1 or 2 EIA RS232-compatible CRTs, leased line modems, or TTYs (current loop)
14535	Async Programmable Modem Controller; 1 line to 9,600 baud
14512	Async Programmable Modem MUX; for 2 or 4 lines
14513	Sync Programmable Modem Controller; to 50K baud
14523	Automatic Calling Unit MUX; for 1-4 ACUs.

offer any opinion on CAI's service organization. When asked what he thought about the programming manuals, he said they are as good as anyone else's manuals. Readers apparently feel that writers for all the manufacturers seem to leave something out as self-evident, when it is not self-evident to the user. This user's only annoyance was that he could not obtain logic diagrams and documentation on the memory board because it is proprietary. The user wanted to trace causes of trouble himself when it occurred.

**CONFIGURATION GUIDE**

All models in the LSI-2 and LSI-3 Series can be configured without console and power in the Naked line or in a package with chassis and power in the Alpha line.

**Table 4. Naked Mini/Alpha LSI: Software**

Package	Description
<b>Real-Time Executive (RTX)</b>	Modular system consisting of multitasking executive (RTX nucleus); I/O executive (IOX) subsystem; communications executive (COMX); requires 650 wd of memory and console.
<b>Disc Operating System (DOS)</b>	For control of sequential job operations; with system secondary storage on disc; requires 16K wd of memory, disc, Teletype, real-time clock, printer, paper tape I/O.
<b>Operating System (OS)</b>	For batch assembly & execution of user programs; supports disc storage, any combination of std peripherals; runs on any LSI-3 computer.
<b>BETA Assembler (2 versions)</b>	Relocatable; one version requires 4K wd of memory; another (8K) version supports unit record I/O with intermediate mass storage.
<b>OMEGA Conversation Assembler</b>	Adds on-line editing, updating, conversational capabilities to BETA.
<b>360 Cross Assembler (XASM)</b>	Written in IBM FORTRAN IV, Level G; produces output identical to BETA & OMEGA.
<b>Advanced BASIC</b>	Dartmouth BASIC with nested recursive subroutines, calculator mode & other extensions; requires 4K words of memory.
<b>Extended BASIC</b>	Advanced BASIC with string manipulation & matrix instructions; requires 8K words of memory.
<b>Extended Multiple User BASIC</b>	Same as Extended BASIC, but for 8 users; requires 8K words of memory (16K recommended).
<b>FORTRAN IV</b>	ANSI FORTRAN IV with added features; stresses compact object code; requires 16K words to compile, 8K words to run.
<b>File Manager</b>	Program storage & retrieval for small memories; 4K words of memory plus disc, magnetic tape, or cassette unit.
<b>Utilities</b>	Source tape preparation; loader; TTY/CRT utility; math packages; diagnostics.

All minimum Naked Minis consist of a processor with memory but no power or control console. The Naked Mini 16s and LSI-2s also include a chassis and motherboard with varying number of slots available, usually five or six. Jumbo versions have nine slots. The minimum NAKED MILLI LSI-3/05 has no chassis and motherboard; the CPU and up to 8K words of memory are all contained on a single board. Naked systems must be bought in minimum quantities of five units in the LSI Series and 10 units in the older 16 Series.

All Alpha systems include the processor, memory, chassis, power supply, and control console; slots are available on the minimum system for attachment of additional memory and controller/interfaces.



The following processor options are available for the LSI Series: power fail restart (PFR); Teletype 33 ASR interface; real-time clock (0.1, 1.0, and 10.0K Hertz) with two interrupts; autoloader ROM (programmed for paper tape reader, Teletype, cassette, magnetic tape, or disc); and an EIA RS232 CRT interface that can be added to the Teletype interface. In addition, there is a Basic Variables option (a prerequisite for certain other options) offset of processor interrupts, enabling power fail interrupt, and sense register jumpering for operation without console. DMA is a standard feature. Processor options are mounted piggyback on the processor board instead of on a separate card, so they must be factory installed.

The minimum LSI-2 processor is contained on one board with memory on another, leaving three slots for additions. Each expansion chassis adds five or nine slots to the system. System size is limited by the maximum memory size (up to 256K words on LSI-2/10 or 2/20 and up to 512K words on the 2/60 with the Memory Bank Control option) and by the maximum number of peripherals that can be addressed (up to 256 individual device controllers) and handled by the system software. Peripheral offerings are summarized in Table 3.

Both LSI-3/05 and LSI-2 systems can be purchased without memory, or they can be packaged with various memory modules. The LSI-3/05 can attach all RAM, a RAM/ROM module, or RAM/EPROM (Erasable Programmable ROM) modules.

Computer Automation supplies three packaged Alpha LSI-2 configurations that are less expensive than the total of all components. These four configurations are available on short delivery.

- 30010-16 Standard DOS 20 — CPU, 16K words of core memory, all processor options except RS232

interface, disc (2.46 million words), printer, paper tape reader/punch, Teletype ASR 33 expansion chassis and power supply, and DOS software.

- 30010-32 Expanded DOS 20 — same as 30010-16 but with a total of 32K words of core memory.
- 30012-32 Expanded DOS 60 — same as 30010-32, except the LSI-2/20 is replaced by an LSI-2/60 MEGABYTER.

Minimum requirements for the other software packages, together with a brief description of the packages appears in Table 4.

## COMPATIBILITY

The LSI-3 and LSI-2 Series are upward compatible; the 3/05 is upward compatible to the 2/10, 2/20, and 2/60. The 3/05 has subroutines available to simulate missing instructions so that programs developed on the other models can run on the 3/05. The LSI Series is also completely compatible with the earlier Alpha-16 and Naked Mini-16 series. Peripherals can attach to any LSI or the older 16 line, with the exception of discs. The disc interfacing is slightly different for the LSI line than for the older 16 line.

## MAINTENANCE

Computer Automation sells only to OEM manufacturers, it does not provide the type of on-site preventive and emergency maintenance contracts usually associated with end users. The company does offer a 1-year warranty. Components that break down are immediately replaced or repaired free of charge during the first 30 days. After that, parts are repaired at the factory, while the user has access to "loaned" components (20 percent of purchase price) during the repair period.

## TYPICAL PRICES

Model Number	Description	Purchase Price* \$
<b>SYSTEMS</b>		
30010-16/66	Standard DOS 20 (contains Jumbo Alpha LSI-2/20 computer with 16K words of 1,200-nsec core memory, power fail restart, Basic Variables, Teletype interface, real-time clock, EIA RS232 CRT interface, autoloader and autoloader ROM set options, ASR 33 Teletype, paper tape reader & punch with integral controllers, line printer, 4.92-million-byte disc subsystem, enclosure, & software)	29,975
30010-32/82	Expanded DOS 20 (plus 16K words of 1,200-nsec core memory & FORTRAN IV)	33,950
30012-32/82	Standard DOS 60 (same as 30010-16/66 with LSI-2/20 replaced by LSI-2/60 MEGABYTER)	35,550
<b>CENTRAL PROCESSOR AND WORKING STORAGE</b>		
<b>NAKED MILLI</b>		
10300-00	NAKED MILLI LSI-3/05 CPU on Half Card (includes 95 instructions, power/fail restart, vectored priority interrupts, & 16-bit DMA port)	295*
10300-01	Same as 10300-00 with Real-Time Clock & Autoloader	395*
10370-38	Same as 10300-01 with 256 words of RAM Memory & Sockets for up to 8K Words of ROM	465*
10380-04	Same as 10300-01 with 4K Words of RAM Memory	725*
10390-52	Same as 10300-01 with 1K Words of RAM & 2K Words of Ultraviolet EPROM	1,575*
10390-62	Same as 10300-01 with 2K Words of RAM & 2K Words of EPROM	1,725*
10390-64	Same as 10300-01 with 2K Words of RAM & 4K Words of EPROM	2,750*
10373-38	Alpha LSI-3/05A (includes chassis for 3 half cards, 10-amp power supply w/o fans, operator's console, 10300-01 CPU, 256 words of RAM with sockets for up to 8K words of ROM)	825
10373-58	Same as 10373-38 Except with 1K Words of RAM	950
10383-04	Same as 10373-38 Except with 4K RAM-Only Memory	1,146
10393-62	Same as 10373-38 Except with 2K Words of RAM & 2K Words of EPROM	2,100
10393-64	Same as 10373-38 Except with 2K Words of RAM & 4K Words of EPROM	3,125
10375-38	Alpha LSI-3/05B (includes chassis for 5 half cards, fan, 15-amp power supply, operator's console, 10300-01 CPU, 256 words of RAM with sockets for up to 8K words of ROM)	975
10375-58	Same as 10375-38 Except with 1K Words of RAM	1,115
10385-04	Same as 10375-38 Except with 4K Words of RAM Memory	1,345
10395-62	Same as 10375-38 Except with 2K Words of RAM & 2K Words of EPROM	2,275
10395-64	Same as 10375-38 Except with 2K Words of RAM & 4K Words of EPROM	3,300
10376-38	Same as 10375-38 Except with Programmer's Console Instead of Operator's Console	1,190
10376-58	Same as 10376-38 Except with 1K Words of RAM	1,335

# COMPUTER AUTOMATION INC. — LSI SERIES SYSTEM REPORT

## TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price* \$
10386-04	Same as 10385-04 Except with Programmer's Console instead of Operator's Console	1,575
10386-08	Same as 10386-04 Except with 8K Words of RAM	1,995
10396-62	Same as 10395-62 Except with 2K Words of RAM & 2K Words of EPROM & Programmer's Console	2,845
10396-54	Same as 10396-62 Except with 1K Words of RAM & 4K Words of EPROM	3,425
	Options	
13628-01	Autoload ROM	48
12635-01	Piggyback Teletype Interface	150
	Development Systems	
10368-16	Prototype Development System	4,095
10369-16	Program Development System	5,795
	NAKED MINI LSI-2/10 & 2/20	
	NAKED MINI LSI-2/10 & 2/20 CPU includes 188 instructions, multiple stack handling, hardware multiply/divide, memory scan & extensive byte capability, 5 vectored priority interrupts expandable to 256, 2 direct memory channels increased to 64; available in 5-unit quantities only)	
53586-00	NAKED MINI LSI-2/10 CPU on Full Card (power fail restart option)	1,500
10640-04	Same as 53586-00 Except with 4K Words 980-nsec Core Memory	1,750
10660-16	Same as 53586-00 Except with 16K Words of 1,200-nsec Core Memory	3,300
53506-00	NAKED MINI LSI-2/20 CPU on Full Card (power fail restart option)	1,900
10450-04	Same as 53506-00 with 4K Words of 980-nsec Core Memory	2,300
10460-16	Same as 53506-00 Except with 16K Words of 1,200-nsec Core Memory	3,875
	Alpha LSI-2/10 & 2/20	
	(Alpha LSI-2/10 & 2/20 configurations include a central processor, memory, chassis with power supply)	
10780-28	Alpha LSI-2/10 Except with 4K Words of RAM Memory & Operator's Console	1,975
10740-24	Same as 10780-28 Except 4K Words 980-nsec Core Memory	2,440
10741-28	Same as 10740-28 Except Jumbo Version	3,565
10760-36	Same as 10780-28 Except with 16K Words of 1,200-nsec Core Memory	3,990
10761-36	Same as 10761-36 Except Jumbo Version	4,245
10740-04	Same as 10740-24 Except with Processor's Console Instead of Operator's Console	2,540
10741-08	Same as 10740-28 Except with Programmer's Console Instead of Operator's Console	3,665
10550-24	Same as 10740-24 Except for Alpha LSI-2/20 Instead of 2/10	2,765
10551-28	Same as 10741-28 Except for Alpha LSI-2/20 Instead of 2/10	3,915
10550-04	Same as 10550-24 Except Programmer's Console Instead of Operator's Console	2,765
10551-08	Same as 10551-28 Except Programmer's Console Instead of Operator's Console	4,015
	LSI-2 CPU Options	
12500-00	Power Fail Restart	250
12500-01	Automatic Startup	150
12505-39	Option Pack (includes Basic Variables, Teletype interface, real-time clock, and autoload)	485
12505-55	Option Pack (same as 12505-39 except with EIA RS232 CRT interface)	560
13505-01	Autoload ROM	60
13505-02	Same as 13505-01 Except with Loaders for Floppy Disc Controller or Peripheral Subsystem Plus Microdiagnostic Program	145
13505-03	Autoload ROM	145
	MEGABYTES	
10951-08	MEGABYTE (includes 8K words of core 980-nsec memory, jumbo chassis, power supply, programmer's console, power fail restart, Basic Variables, Teletype & EIA CRT interface, real-time clock, autoload, & autoload ROM set)	6,850
10961-16	Same as 10951-08 (with 16K words of 1,200-nsec core memory)	7,900
10951-16	Same as 10961-16 Except Contains 2 Interleaved 8K-Word Core Memory Modules	8,765
	Memories	
11650-38	256 Words of RAM Memory & Sockets for 8K Words of ROM	290
11650-58	1K Words of RAM Memory & Sockets for 8K Words of ROM	400
11642-04	4K Words RAM Memory	550
11530-52	1K Words of RAM & 2K Words of EPROM	1,425
11530-64	2K Words of RAM & 4K Words of EPROM	2,600
11550-08	8K Words of 980-nsec Core Memory	1,950
11560-16	16K Words of 1,200-nsec Core Memory Options	3,050
	Memory Options	
12090-40/20	On-Card Battery Backup	95
12545-00	Memory Bank Control	900
30100-01/02	EPROM Programmer	2,950
	MASS STORAGE	
22566-00	Dual Floppy Disc Drives	3,700
22530-00	Moving-Head Disc Drive	10,200
18566-XO	Dual Floppy Disc Subsystem	12,300
	Input/Output	
22224-15	Magnetic Tape Transport	6,300
18224-15	Magnetic Tape Subsystem	8,275
22205-00	Modified ASR 33 with 16-Ft Cable	1,695
22230-00	Keyboard/Display Terminal	3,175
22077-20	Card Reader (285 cpm)	4,425
22107-06	Line Printer (120 cps; 60-150 lpm; 80 col)	4,950
22223-11	Paper Tape Reader (300 cps)	1,945
22223-60	Paper Tape Reader/Punch	5,625
14223-00	Paper Tape Peripheral Controller	600
14224-00	Magnetic Tape Controller	2,400
14566-01	Floppy Disc Controller	930
14629-04	I/O Distributor (for 1-4 parallel intelligent cables)	380
14629-14	I/O Distributor (for 1-4 serial or parallel intelligent cables, any mix)	445
14629-18	I/O Distributor (1-8 serial or parallel intelligent cables, any mix)	530
14631-11/01/02/03/04	Intelligent Cables	145
19001-00	Advanced BASIC	300
19001-10	Extended BASIC	400
19001-20	Extended Multiple User BASIC	500
20570-00	FORTRAN IV	1,700
19005-02/03	Real-time Executive for LSI-2 or LSI-3	500
19005-05	Real-time Executive for both LSI-2 & 3	750
19007-00	Operating System	2,000

\*Available only in minimum order quantities of 5 units

\*CAI systems are sold OEM, thus maintenance to the end-user is not on typical contract basis. See MAINTENANCE section



# COMPUTER AUTOMATION LSI SERIES ALPHA

## LSI-3/05, REPORT UPDATE

ALPHA LSI-3/05 minicomputers are now available in five series configurations designed to allow the user to move up through the Computer Automation product line. They are well-suited for control applications where system requirements are expected to expand. Typical LSI-3/05 configurations are as follows:

Series A — NAKED MILLI CPU, 10-Amp power supply, three-slot half-card chassis and operator's console.

Series B — NAKED MILLI CPU, 15-Amp power supply, five-slot half-card chassis and operator's console.

Series C — NAKED MILLI CPU, 15-Amp power supply, five-slot half-card chassis and programmer's console.

Series D — NAKED MILLI CPU, 25-Amp power supply, standard five-full-slot chassis and operator's console.

Series E — NAKED MILLI CPU, 25-Amp power supply, standard five-full-slot chassis and programmer's console.

With 256 words of semiconductor random access memory (RAM) and sockets to accommodate up to 8K words of ROM and 2K words of PROM, the lowest priced Series A model is \$701; lowest priced Series B Model is \$829; and Series C lowest priced model is \$1,012. With 4K words of core memory, the lowest priced Series D Model is \$1,921. The Series E Model is offered with core or RAM memory; lowest priced versions are \$2,006 for 4K core and \$1,687 for 4K RAM.

### SOFTWARE MACHINES

Five disc operating systems used in conjunction with Computer Automation's NAKED MINI computer have been introduced for the OEM market. Dubbed the Software Machines, the systems are designed to replace the company's previous disc operating products and to allow command inputs from a keyboard or from job files containing job control language statements. Discs can be loaded with a string of jobs that can be executed without operator attendance. Basically, the new configurations replace paper tape as the system I/O device with floppy disc. For the two smallest configurations, floppy discs also provide bulk storage for the system.

Each machine includes an ALPHA LSI-2 minicomputer, core memory of 16K or 32K words, dual floppy disc subsystem, ASR-33 TTY and operating system package with executive, input/output control system, disc file manager, assembler and macro assembler. Character-oriented text editing, line-oriented source program editing, linking/editing of object programs, alphabetizing/listing cross references of program symbols and other program debug and maintenance functions are supported.

The floppy disc operating system includes basic variables, TTY interface, autoloader, real-time clock, power fail restart, and EIA RS-232 interface options as standard elements.

The following five models are currently available:

Standard DOS 10 — ALPHA LSI-2/10, 16K words of core memory, dual floppy disc subsystem, TTY ASR 33;

Expanded DOS 10 — ALPHA LSI-2/10, 32K words of core, line printer, dual floppy disc subsystem, TTY ASR 33, and FORTRAN IV package that supports ANSI FORTRAN X3.9 1966 language;

Standard DOS 20 — ALPHA LSI-2/20, 16K words of core, line printer, cartridge disc system, dual floppy disc subsystem, and TTY ASR 33;

Expanded DOS 20 — ALPHA LSI-2/20, 32K words of core memory, line printer, cartridge disc system, dual floppy disc subsystem, TTY ASR 33 and FORTRAN IV package;

Standard DOS 60 — ALPHA LSI-2/60, 32K words of core memory, line printer, cartridge disc system, dual floppy disc subsystem, TTY ASR 33, and FORTRAN IV package.

Deliveries are scheduled 30 days after the order is received.

### PRICE DATA

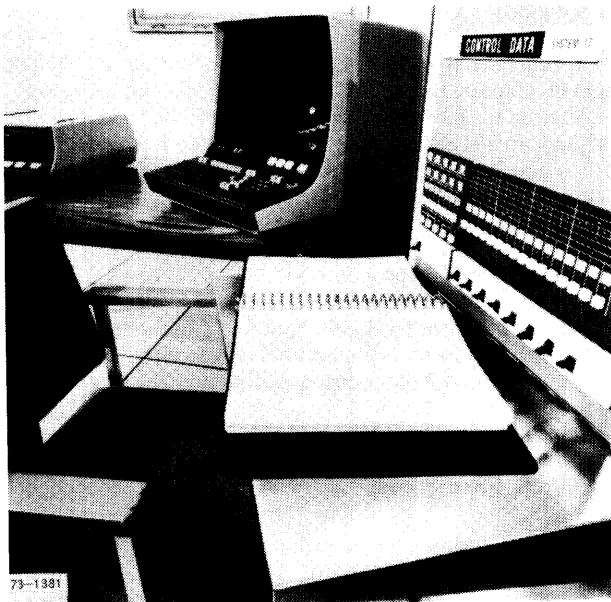
Purchase prices for the basic models are as follows:

Standard	DOS 10	\$13.975
Expanded	DOS 10	\$23.975
Standard	DOS 20	\$29.975
Expanded	DOS 20	\$33.950
Standard	DOS 60	\$35.550



# CONTROL DATA CORP.

## System 17 System Report



### OVERVIEW

The CDC System 17 is a 16-bit minicomputer aimed at both OEM and end-user markets, particularly for industrial applications. The system and its predecessor, the CDC 1700, have been used in industrial control, data acquisition, hospital/medical, optical character recognition, graphics, communications, amusement and recreation, data entry, and supervisory control applications. Its primary orientation as a system is toward industry, however; CDC has sold large orders of these minicomputers to automobile manufacturers.

System 17 borrows much of its architecture and its software from the CDC 1700, but improves on the 1700 by offering lower cost peripherals. The I/O interfacing is somewhat different for the new peripherals, but optional channel adapters can be added to interface 1700 peripherals to System 17 (the 1500 analog/digital subsystem, for instance). Because the two systems are program compatible, the vast library of software developed for the 1700 is available to the System 17. Thus, three factors — cheaper peripherals, large tested software base, and the interface to the vast 1500 subsystem — make System 17 a strong contender in the minicomputer market.

Although System 17 has not embraced the microprogramming concept, it has made use of other popular new developments in minicomputer technology. The new processor uses MOS/LSI semiconductor memory, and thus offers a better price/performance ratio than the 1700.

System 17 is particularly attractive to end users. The policy of offering user-oriented, hardware/software applications packages for all CDC computers has been company-wide for a number of years.

Table 1 lists the mainframe characteristics.

### PERFORMANCE AND COMPETITIVE POSITION

The System 17 places CDC in the best position it has been in for several years in the minicomputer market. Although CDC early recognized the need for real-time small computers and produced the 1700 line for that market, the company didn't follow up by developing minicomputer peripherals for the 1700 line. CDC interfaced a broad range of peripherals to the 1700, but they were generally the same peripherals CDC offered with its large computers and they were expensive. As minicomputer processor prices fell, it became apparent that minicomputers needed their own low-cost peripherals. Thus, the cost of peripherals for most minicomputer systems has dropped markedly in the past few years.

With the System 17, CDC introduced both an excellent, lower-cost processor and minicomputer-sized peripherals: magnetic tape, cartridge disc, printers, conversational display, card reader, and so on. System 17 retains the really fine logic designed into the 1700 line, and it can run all the 1700 software developed over the last eight years. In addition, CDC has many years of experience in real-time processing and has an impressive number of systems operating for varied applications.

One of the competitive advantages of System 17 is its interface to the 1500 analog/digital subsystem, which has a tremendous variety of components of all types, ranges, and speeds. The 1500 originally was designed for the 1700 system but continues to be expanded as a System 17 peripheral as well. One recent addition is the 1590 remote interface, which allows the 1500 to be located at a site remote from the System 17. This is an important addition to the product line; at the time of this writing, only MOD-COMP and Digital Equipment had similar offerings.

### HEADQUARTERS

Control Data Corp.  
P O Box 0  
Minneapolis MN 55440  
(612) 853-8100

**Table 1. CDC System 17: Mainframe Characteristics**

<b>Feature/Characteristic</b>	
<b>Central Processor</b>	1784-1, 1784-2
Microprogramming	No
Control Memory	None
No. of Internal Registers	2 accumulators; 2 index
Addressing	
Direct (no. of words)	256
Indirect	Yes
Indexed	Yes
Instruction Set	Hardware/subroutine
Number	196
Decimal Arithmetic	No
Floating-Point Arithmetic	Subroutine (std); hardware (opt)
User-Microprogramming	No
Priority Interrupt System	
Levels	16
<b>Main Storage</b>	
Type	MOS/LSI
Cycle Time ( $\mu$ sec)	0.900 (1784-1); 0.600 (1784-2)
Basic Addressable Unit	1 word
Bytes/Access	2
Cache Memory	None
Min Capacity (bytes)	8,192 (std)
Increment Size (bytes)	8,192
Error Checks	Parity
Protection Method	Manual switches
ROM	No
<b>Input/Output</b>	
Programmed I/O	Yes (called AQ)
DMA Channels	Yes (called DSA) 1 std; 1 opt
Multiplexed I/O	No
Multiprocessing Adapters	Coupling data channel; also satellite coupler for CDC 3000 or 6000 systems
Max. Transfer Rate	
Within Memory (wds/sec)	278K (1784-1); 417K (1784-2)
Over DMA (DSA) (wds/sec)	1.1M (1784-1); 1.6M (1784-2)

The System 17 competes with the Digital PDP-11/40 and /45, the Data General Nova ECLIPSE line, the Hewlett-Packard 21MX Series, and Honeywell System 700. System 17 can be a strong competitor if CDC takes its own claims seriously and does offer users service rather than hardware. Real-time systems tend to require tailoring to fit a specific application, and the strong competitors in this market must be prepared to perform applications engineering and programming for users. A large market exists for minicomputers like the System 17, and CDC should be able to produce a number of hardware/software System 17 applications packages that will do well.

## USER REACTIONS

Users contacted had previous experience with CDC systems, notably the 1700 Series. For them, the step to the 17 was a logical, orderly one; nevertheless, they first considered alternatives from other manufacturers.

## Manufacturing

A manufacturer of chemicals and drugs obtained one of the first System 17s to use as a front end for its CDC 6400, with terminals connected to several real-time lab opera-

tions. This manufacturer already had a number of CDC 1700s in use in various capacities for process control. A competitive system closely examined was the DEC PDP-11. The System 17 was chosen because it had more software immediately useful to their purpose and it could be used to compile programs for the 1700s they already had. This manufacturer is now considering adding more System 17s for control applications.

The current front-end configuration includes a 1700 channel adapter, two tapes, two discs, CRT terminal, dot matrix printer, and 32K words of memory. The disc drives installed are 854 models; but this user is looking forward to CDC's new line of cartridge discs which use an electronic seek mechanism that is more reliable than current electromechanical ones.

This user found no problems with program compatibility between the 1700 and System 17. As for maintenance, the 1700s have been quite reliable, and he expects the System 17 to be even easier to maintain. This user stressed the excellence of the 1700 operating system, which is also used on the System 17. He noted that CDC has one of the largest software libraries for minicomputers.

## Medical Systems

A medical systems house produces packages for admissions screening, intensive care, coronary care, operating room functions, and the like. About five years ago, this company selected the 1700 as the basis for its medical hardware/software packages because it was one of the few proven systems with nationwide maintenance. Also, CDC had a good FORTRAN package to make programming easier.

Experience with the 1700 has borne out expectations. The evolution to the System 17 is a natural step because of the complete software compatibility, lower cost, and greater reliability of the new system.

## CONFIGURATION GUIDE

A basic System 17 includes a processor (either 1784-1 or 1784-2) and 4K words of MOS/LSI semiconductor memory. Both processor submodels include 16 interrupts, two index registers, DSA, parity, memory protect, and hardware multiply/divide as standard features. The difference between the two models is in the memory cycle time: 900 nanoseconds for the 1784-1 and 600 nanoseconds for the 1784-2.

Two enclosures are available. The first is required and houses the CPU, 32K words of memory, the DSA and AQ channel, a memory hold battery (providing power for eight hours in case of main power failure), and AQ/DSA expansion. Each 4K-word memory module is mounted on one circuit board. Up to 36 circuit boards, plus power supply and cooling equipment, are also housed in the CPU enclosure. Optional features are integral controllers for magnetic tape transport, cartridge disc unit, line printer, card

reader, card punch, paper tape reader, teletypewriter, and conversational display terminal. See Table 2 for specifications.

The second enclosure is required to add memory beyond 32K words. Full memory expansion to 64K words also requires a memory expansion module (1786-1).

Up to eight peripherals can connect to the DSA and AQ I/O channels. The 1785 channel expansion adapter is available in four models to expand the channel capacity.

- 1785-1 expands the AQ channel to handle up to eight additional devices.
- 1785-2 expands the DSA channel to handle up to eight additional devices.
- 1785-3 converts the AQ channel to the standard 1700 bus so the CDC 1700 programmed I/O devices can be connected to System 17.
- 1785-4 converts the DSA channel to the standard 1700 I/O bus so the CDC 1700 DSA devices can be connected to the System 17.

The System 17 can support all the peripherals designed specifically for it as well as peripherals available with the

**Table 2. CDC System 17: Peripherals**

Device	Performance Characteristics
<b>Discs</b> 856-2	1 fixed, 1 removable cartridge disc, 1.1M wds/disc, 4 drives/controller
<b>Magnetic Tape</b> 856-4	Like 856-2, but 2.2M wds/disc
615-73	7-track, 556 or 800 bpi
615-93	9-track, 800 NRZI or 1,600 PE bpi
616-72	7-track, 556/800 bpi, 25 ips
616-92	9-track, 800 bpi, 25 ips
616-95	9-track, 800 bpi, 50 ips
<b>Punched Card</b> 1725-1	100-cpm reader
1729-3	300-cpm reader
415	250-cpm punch
<b>Paper Tape</b> 4021/4022	FACIT readers, 300 cps
4070 Series	FACIT punches, 75 cps
<b>Terminals</b> 1711	33/35 KSR TTY, 10 cps
1713	33/35 ASR TTY, 10 cps
713-10	640- or 1,280-char CRT
274	Digigraphic console (a 1700 peripheral)
<b>Printers</b> 1742-30	300 lpm
1742-120	1,200 lpm
713-120	30 cps
<b>Analog/Digital</b> 1500	A/D, D/A subsystem; extensive subsystem with up to 15 "sub-subsystems" for low-level and high-level A/D, D/A, and digital control
1590-3	Remote interface for up to 100 D/A, A/D devices from Model 1500 subsystem
<b>Communications</b> 1743-1	For 1 or 2 sync lines, to 19,200 baud
1743-2	For 8 async lines, to 9,600 baud
1718	CDC 3000/6000 interface
1716	Multiprocessor coupler
<b>Other</b> 10336	Real-time clock

**Table 3. CDC System 17: Software Systems**

Characteristic	4K Assembly System	Utility System	Mass Storage Operating System
Assembler	Assembler	Assembler or Macro Assembler	Macro Assembler
Compiler	None	Tape FOR-TRAN	Mass Storage FOR-TRAN
Mass Storage Required	No	No	Yes
Minimum Configuration Required	4,096 wds	8,192 wds*	12,288 wds*
Core Storage Occupied by Resident Portion	750 wds	2,250 wds	8,673 wds (largest overlay)
Execute Batch Programs	Yes	Yes	Yes
Execute Control Programs	No	No	Yes
Multiprogramming Program Library	No	No	Yes
	No	Yes	Yes

Note:  
\*If the FORTRAN compiler is used, additional 4K words of core storage are required.

CDC 1700 line, like the massive 1500 analog/digital subsystem. Furthermore, a new controller allows connection of a remote 1500 subsystem over communication lines.

In addition, intercomputer couplers are available to interface it to the CDC 3000, CDC 6000, and Cyber 70 Series computers, or to link two System 17s together with a shared disc data base.

The System 17 is very modular, and CDC offers dozens of application-oriented configurations. Many of these are partially dependent on software requirements. Software packages and their requirements are listed in Table 3.

## COMPATIBILITY

The System 17 is program compatible with the CDC 1704, 1714, and 1774. An intercomputer adapter allows the System 17 to operate as a front end for the CDC 3000, CDC 6000, and Cyber 70 Series computers; to communicate with CDC 1700 systems; and to use the CDC 1700 peripherals. In addition, hybrid A/D configurations incorporate an EAI 680 analog computer as a system component.

## MAINTENANCE AND SUPPORT

CDC provides 24-hour service centers in 42 metropolitan areas in the United States. Preventive maintenance is provided during the primary maintenance period.

# CONTROL DATA CORP. — SYSTEM 17 SYSTEM REPORT

CDC provides training and education for customers at its education institutes. Other services include site planning, systems analysis, and consulting. FOCUS, the international Forum of Control Data Users formed in 1968,

gives users opportunities to exchange ideas among themselves and CDC personnel. A special interest group has been formed for CDC 1700 users. A newsletter is published monthly to distribute information.

## TYPICAL PRICES

Model Number	Description	Monthly Rental \$ 1-Yr	Monthly Rental \$ 2/3-Yr	Purchase Price \$	Monthly Maint \$
<b>CENTRAL PROCESSORS AND WORKING STORAGE</b>					
1784-1	Processor with 4K words of 18-bit MOS memory, 900 nsec	347	258	14,175	100
1784-2	Processor (same as 1784-1 except 600-nsec memory cycle time)	373	364	17,325	121
<b>Systems Options</b>					
1785-1	AQ Channel Expansion	27	26	1,050	11
1785-2	DSA Channel Expansion	27	26	1,050	11
1785-3	1700 AQ Channel Adapter*	69	67	2,625	16
1785-4	1700 DSA Channel Adapter*	42	41	1,575	16
<b>Memory</b>					
1782-1	Memory Module (900 nsec, 4,096 wds)	84	82	3,150	31
1782-2	Memory Module (600 nsec, 4,096 wds)	90	88	4,200	36
<b>MASS STORAGE</b>					
<b>Cartridge Disc</b>					
856-2	Cartridge Disc Drive (1.1M wds on fixed, 1.1M wds on removable discs)	200	195	9,450	57
856-4	Cartridge Disc Drive (same as 856-2 except has 2.2M wds/disc)	315	307	13,125	67
1733-2	Cartridge Disc Controller (single DMA channel connection; absolute cylinder addressing; daisy chain capability; controls up to 4 856-2 or 856-4 drives)	174	168	5,775	31
<b>INPUT/OUTPUT</b>					
<b>Magnetic Tape</b>					
615-73	Magnetic Tape Transport (7-track, NRZI; 556 or 800 bpi)	174	168	5,775	68
615-93	Magnetic Tape Transport (9-track, PE with 1,600 bpi or NRZI with 800 bpi)	189	184	7,350	79
<b>Punched Card</b>					
1729-3	Card Reader and Controller (300 cpm)	179	171	6,300	78
<b>Line Printer</b>					
1742-30	Line Printer and Controller (300 lpm; 64-char set)	389	378	17,850	200
1742-120	Line Printer and Controller (1,200 lpm; 48-char set)	1,533	1,495	52,500	300
<b>Terminals</b>					
<b>TTY</b>					
1711-4	33 KSR	37	36	1,470	32
1711-5	35 KSR	74	72	3,150	39
1713-4	33 ASR	48	47	1,680	36
1713-5	35 ASR	116	111	5,040	97
<b>CRT</b>					
713-10	CRT Console	63	62	2,095	13
711-100	CRT Expanded Memory	11	—	336	11
1781	Hardware Floating-Point Unit	255	NA	9,700	50
1743-1	Communications Controller (Sync, RS232C/CCITT V.24)	70	NA	2,600	24
1743-2	Communications Controller (Async, RS232C/CCITT V.24)	85	NA	2,950	24
1590-3	Remote Computer Interface Subsystem	175	NA	6,500	71
1566-20	D/A Conversion Unit	29	NA	1,063	19
1566-21/22/33	Conversion Unit	49	NA	1,800	28
10336	Real-Time Clock	30	NA	1,200	12
1720-1	Paper Tape Controller	55	NA	2,000	10
1732-3	Magnetic Tape Controller	180	NA	5,250	42
616-72	Magnetic Tape Transport (7-track, 556/800 bpi, 25 ips)	161	NA	6,000	61
616-92	Magnetic Tape Transport (9-track, 800 bpi NRZI/1,600 bpi PE, 25 ips)	191	NA	7,100	71
616-95	Magnetic Tape Transport (50-ips version of 616-92)	207	NA	7,700	77
1725-1	Card Punch & Controller (100/400 cpm)	660	NA	25,000	180

\*To connect CDC 1700 peripherals.

## **CONTROL DATA CORP. SYSTEM 17 System Report Update**

### **SYSTEM 17 AUTOMATIC WEATHER MESSAGE SWITCH SYSTEM**

Control Data Corporation has introduced an automatic weather message switch system based on its SYSTEM 17 central processor. This can be a stand-alone, store-and-forward system if no large-scale data analysis is required, or it can interface to a host computer to prepare analyses and prognosis messages, which the message switch system distributes to other centers in the network. Data entry terminals can be CRT, punched card or tape, or Teletype.

In automatic mode, the message switcher routes information to all pre-selected destinations according to data in the message header, errors are detected and flagged for operator attention. Under manual control, messages can be extracted on a CRT entry/display station. Line protocol with multiple levels of priority interrupt is determined by software (available from CDC). Messages are automatically logged to a printer and/or recorded on magnetic tape or disc for subsequent off-line analysis. The system buffers storage overload by slowing input and speeding up output until all waiting messages are processed.

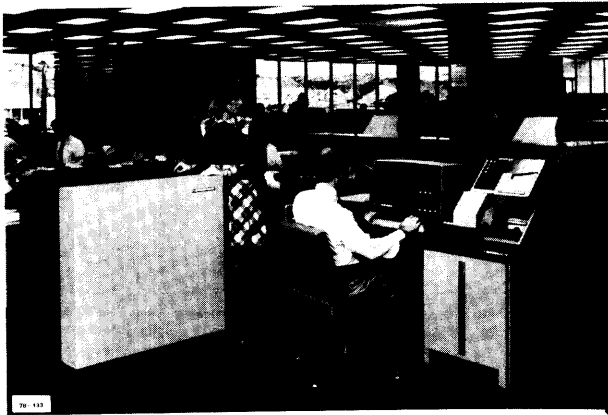
An optimum weather message switch system composed of a central processor with 32K words of memory (expandable in 4K increments to 64K), line printer, card reader, magnetic tape drive, two disc drives, two display units, multiplexor controller, and Teletype costs about \$140,000; software for the system sells for \$30,000.





## CONTROL DATA CORP.

### Cyber 18 System Report



CONTROL DATA'S NEW CYBER 18-20

#### OVERVIEW

With its new CYBER 18, Control Data has ventured into the commercial minicomputer field for the first time. The CDC 1700 and its successor, the System 17, were largely used for real-time control, data acquisition, and scientific applications. CYBER 18 incorporates the System 17 as a subset: the CYBER 18-17 is the System 17; the CYBER 18-10 and 18-20 emulate the System 17 instruction set in the microcode of a new processor. The CYBER 18-30 is a dual-processor configuration using two 18-20 processors, which can share main memory.

The CYBER 18-10 will be marketed as a remote batch terminal that can emulate the IBM 2780 and 3780 terminals as well as the CDC 200 user terminal. The CYBER 18-17 will continue the System 17's real-time control orientation. The CYBER 18-20 is business-oriented, supporting RPG II. CDC will also supply applications packages for general data processing for the manufacturing and distribution industries.

The CYBER 18-30 will run under a new operating system, called TIMESHARE, which is now under development; it will support up to 64 BASIC terminal users. CDC will market the 18-30 to the education market.

The systems are all available for purchase or lease. A 5-year full payout lease is also available. Software is unbundled.

First deliveries of the CYBER 18-10 and 18-17 were in April. The CYBER 18-20 and 18-30 are scheduled for first delivery in August 1976.

#### MAINFRAME

The CYBER 18 mainframe characteristics are summarized in Table 1. The CYBER 18-10, 18-20, and 18-30 systems are built around a new microprogrammed processor. The microcode to implement the basic CYBER 18 instruction set, which includes System 17 instructions as a subset, is stored in ROM control memory. Each word is 32 bits long, and the control memory cycle time is 168 nanoseconds.

The processor includes eight internal registers, seven of which can be used either as accumulators or index registers. Of the 123 instructions on the CYBER 18 but not on the System 17, most are used for operations on the multiple accumulators. Although the basic addressable unit of data is a word, new memory reference instructions can perform operations on a field of 1-16 bits within the word.

New instructions also implement Generate Byte Parity odd/even and a combination of Test/Skip and Decrement/Repeat. The six additional instructions for the CYBER 18-20 and 18-30 are to operate Writeable Control Store, which can be loaded from main store.

Floating-point arithmetic is via software sub-routines on the 18-10 and via microcode on the 18-20 and 18-30. The CYBER 18-17 uses a separate hardware floating-point unit that interfaces to the I/O bus. The floating-point microcode uses exactly the same calls as the hardware unit, so they are completely software compatible.

#### HEADQUARTERS

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Table 1. CDC CYBER 18: Mainframe Characteristics

MODELS	18-10	18-17	18-20	18-30
CENTRAL PROCESSOR	Single	Single	Single	Dual 18-20s
Microprogrammed	Yes	No	Yes	Yes
Microprogrammable	No	No	Planned	Planned
Control Memory	ROM	No	ROM/RAM	ROM/RAM
Word Length (bits)	32	—	32	32
Cycle Time ( $\mu$ sec)	0.168	—	0.168	0.168
RAM Capacity (wds)	—	—	4K	4K
Increment Size (wds)	—	—	512/2K	512/2K
Word Length (bits)	16 + 1 parity & 1 protect	16 + 1 parity & 1 protect	16 + 1 parity std (6 ECC opt) & 1 protect	16 + 1 parity (6 ECC opt) & 1 protect
No. of Registers	8	4	8	8
Accumulators	7	2	7	7
Hardware Index	7	2	7	7
Hardware Stack Memory	No	No	No	No
Addressing (wds)				
Direct	256	256	256	256
Indirect	Multilevel, 32K/64K	32K/64K	Multilevel, 32K/64K	Multilevel, 32K/64K
Indexed Mapping	64K	64K	64K	64K
Instruction Set	No	No	Paging (256K)	Paging (256K)
Implementation	Microcode (ROM)	Hardware	Microcode (ROM)	Microcode (ROM)
Number	195	72	201	201
Floating-Point	Software	Opt	Microcoded	Microcoded
Hardware Stack	No	No	No	No
Writeable Control Store	No	No	Yes	Yes
Interrupts				
Levels	16 macro/16 micro	16	16 macro/16 micro	16 macro/16 micro
Type	Hardware	Hardware	Hardware	Hardware
MAIN STORAGE				
Type	MOS	MOS	MOS	MOS
Cycle Time ( $\mu$ sec)	0.750	0.6/0.9	0.750	0.750
Basic Addressable Unit	Word	Word	Word	Word
Capacity (bytes)				
Min.	32K	8K	32K	32K
Max.	64K	128K	256K	512K
Increment Size (bytes)	32K/64K	8K	32K/64K	32K/64K
Ports per Module	1	1	1	1
Error Checks	Parity	Parity	Parity std; ECC opt*	Parity std; ECC opt*
Memory Protection	Via protect bit & upper and lower bounds	Via protect bit	Via protect bit & upper and lower bounds	Via protect bit & upper and lower bounds
Memory Management	No	No	Yes	Yes
Interleaving	No	No	No	No
INPUT/OUTPUT				
Max. Devices Addressable	16 x 128	16 x 128	16 x 128	16 x 128
Programmed I/O	Yes, via AQ	Yes, via AQ	Yes, via AQ	Yes, via AQ
DMA	No	Yes, via DSA	Yes (4 priority channels)	Yes (4 pri- ority channels)
DMA Transfer Rate (bytes/	—	3.2M/2.2M	2.8M	2.8M

\*Limits memory to 96K (18-20) or 192K (18-30) words.

The macro interrupt system on the CYBER 18 has 16 levels; the 18-10, 18-20, and 18-30 have 16 interrupt levels that are used by the micro-code.

#### Memory

Memory consists of n-Channel MOS memory modules of 16K or 32K words. Each word consists of 16 data bits plus one parity bit and one protect bit as standard. The 18-10, 18-20, and 18-30 memory cycle time is 750 nanoseconds. The 18-17 has both 600- and 900-nanosecond memories. The 18-20 and 18-30 can also use Error Checking and Correcting (ECC) memory modules, which use six checking bits in place of the parity bit. When set, the memory protect bit protects the location from overwriting. The CYBER 18-10, 18-20, and 18-30 also implement upper and lower boundary registers to confine a running program within a memory partition.

Memory management on the CYBER 18-20 and 18-30 divides memory into blocks of pages of 2K words each for allocation purposes. The running program generates 16-bit logical addresses, which the memory management unit translates into 18-bit physical addresses. Thus, each user can address 64K words of memory, and each processor can address 256K words of memory.

The 18-20 chassis can hold only 128K words. The dual-processor 18-30 has two chassis; each has a processor that can address all the memory of the other. Maximum main memory capacity is thus 256K words.

The memory management unit consists of 64 registers of 9 bits each. Each register contains a 7-bit physical page address and a read-only bit; the ninth bit is currently unused. Thus, the memory management unit in one processor can prevent the other processor from writing in its portion of shared memory.

#### Input/Output

All CYBER 18 processors can address 16 device controllers and 128 devices on each controller, for a total of 2K devices. Other parameters, such as slots in the I/O channel and power requirements, make such a number of devices impractical. CDC implements programmed I/O with the AQ channel (via AQ processor registers).

The CYBER 18-10 has no DMA (direct memory access) facility. The 18-17 implements DMA via a DSA (direct storage access) channel. The 18-20 and 18-30 implement DMA with four I/O ports to support four DMA device controllers.

The maximum aggregate DMA rate is 1.4M words (2.8M bytes) per second.

#### Peripherals

New peripherals offered with the CYBER 18 include flexible discs (capacity 262,000 bytes), large discs with 25 or 50 million bytes capacity, microprocessor-controlled console, card readers, line printers, and magnetic tape drives.

#### Software

Software includes RTOS (Real-Time Operating System) and MSOS (Mass Storage Operating System) which were offered for System 17. MSOS 5 will be an upgraded MSOS version for CYBER 18. TIMESHARE, which will support up to 64 BASIC users, will be for the 18-30 only.

The RPG II program package will run on the 18-20 and 18-30. Programs developed using RPG II will run on the 18-10.

Controlware for emulation of IBM 2780 and 3780 RJE terminals and the CDC U200 terminal is available for the 18-10.

#### COMPETITIVE POSITION

Control Data has committed itself to distributed processing with its CYBER 18 systems. Plans call for a substantial investment in system and applications software which will be developed by outside vendors, in cooperation with customers, and in house.

Although the first software available for the 18-10 is designed for enhanced batch processing with RJE to large IBM or CDC host processors, future plans call for applications packages for stand-alone processing. These packages will be largely hand-me-downs from the CYBER 18-20, the central system in the line. RPG II software, as well as substantial numbers of applications packages, will be offered for the 18-20. These programs can run on both the 18-30 and 18-20.

Data base management and COBOL are apparently down the road a bit. A CDC spokesman emphasized that the company's commitment to small computers with stand-alone software and distributed processing support is endorsed by high management levels, including the Chairman of the Board.

As shown in Table 2, the CYBER 18-20 competes with Digital's PDP-11/70, Interdata's Megamini, and Data General's ECLIPSE. The table shows that all the systems are comparable in performance, except the Megamini uses a 32-

Table 2. Comparison of CYBER 18-20 with Some Competitors

	CYBER 18-20	Interdata 8/32 Megamini	Digital PDP-11/70	Data General ECLIPSE 200
Word Length (bits)	16	32	16	16
Instruction Execution Times ( $\mu$ sec, register to memory)				
Integer Add	1.8	1.2	1.8	2.5
Integer Multiply	6.6	3.5	3.9	8.8
Integer Divide	10.5	5.8	8.3	11.2
Floating-Point Add	50-100	2.3	8.2	5.5
Floating-Point Multiply	50-100	3.0	11.2	7.2
Floating-Point Divide	NA	5.3	12.2	7.9
Max. DMA Rate (bytes/sec)	2.8M	6M	4M	2M
Max. Address Capability (bytes)	64K	1M	64K	64K
General-Purpose Registers	1 stack of 8	8 stacks of 16 each	2 stacks of 8 each	1 stack of 4
Prices \$				
CPU + 128KB Memory	43,300	51,900	54,600 <sup>(1)</sup>	35,500
+ 256KB Memory	71,300	70,900	68,800	57,100
+ 512KB Memory	(2)	107,400	101,800	—
+ 1,048KB Memory	—	179,400	163,800	—

Notes:

- (1) Digital bundles parity, console, line clock, and installation in the system price.
- (2) Available only in the bundled 18-30.
- NA Not available. — Not applicable.

bit word and can address 1 million words of memory directly. The CYBER 18 floating-point times reflect the implementation of floating point arithmetic in microcode emulating the System 17 calling sequences.

The CYBER 18-20 is less expensive than PDP-11/70 and Megamini for a CPU with 128K bytes of memory, but is more expensive than the ECLIPSE 200. For a CPU with 256K bytes of memory, the CYBER 18 is more expensive than the other three systems.

The CYBER 18-20 software will run on the 18-30. Initial markets for the 18-30 running under TIMESHARE software, which will support interactive BASIC, will be educational institutions. Up to 64 terminals will be supported. In this market, CDC will compete with PDP-11/70 RSTS/E systems and the HP 21MX and HP 3000. As a dual-processor, shared-memory system, the 18-30 has few direct well-known competitors. Interdata has always envisioned multiple processors with shared memory as a strong offering for the Megamini.

CDC began offering low-cost peripherals for its System 17 a couple of years ago and continues with the CYBER 18. Although CDC has interfaced its systems to Centronics and other inexpensive printers, the CYBER 18 line printer price is quite hefty for a small 18-20 system.

The CYBER 18 offerings are a good mix of systems. CDC has long had a good customer base with its 1700/System 17 line, and the CYBER 18 protects that base while offering much

more for expansion and upgrades, for enticing new customers into the fold, and for developing networks. The 18-10 can function as a batch terminal; the 18-20 and 18-30 can function as concentrators or nodes. The power of an 18-30 would also make it a candidate for a host in a small network. Although these possibilities are there, their reality depends on CDC "putting it all together" with coordinated software and marketing.

PRICE DATA

Model	Description	Purchase Price, \$
CYBER 18-10	CPU, no memory	13,700
CYBER 18-17A	CPU, no memory — supports 900-nsec MOS	11,160
CYBER 17B	Supports 600-nsec MOS	13,643
CYBER 18-20	CPU, no memory	15,300
CYBER 18-30	Dual 18-20 Processor System	110,000
—	32K-Byte MOS Memory Module	8,000
—	64K-Byte MOS Memory Module	14,000
CDC 1833-3	Controller for up to 8 CDC 1867 drives	10,000
CDC 1867	Storage Module Drive	
	25M bytes	12,000
	50M bytes	18,100
CDC 1833-5	Controller for 1865 flexible disc drives	1,500
CDC 1865	Flexible Disc Drive — 262,000 bytes	1,620
CDC 1811	Microprocessor-Controlled Console with 1,920-char display, transfer rates of 110-9600 bps	2,200
CDC 1829	Tabletop Card Reader	
	300 cpm	2,940
	600 cpm	4,410
CDC 1827	Line Printer, 64-char set	
	300 lpm	10,300
	600 lpm	22,000
CDC 1832-4	Magnetic Tape Control	3,300
—	7-Track Tape Drive	6,000
—	9-Track Tape Drive	7,100
	SOFTWARE	
RTOS	Real-Time Operating System	2,540
MSOS 5	Mass Storage Operating System	4,100
RPG II	Report Program Generator	NA
TIMESHARE	Operating System for up to 64 BASIC users	NA
NA	Not Available	





### OVERVIEW

The ECLIPSE® family of computers is Data General's most recent line of general-purpose minicomputers. ECLIPSE systems run the entire gamut of the Nova/Supernova line they replace, but they add a variety of features to increase speed and throughput; to enhance system reliability and error handling; and above all to expand system capabilities while maintaining compatibility with all Nova/Supernova models. With this line, Data General can compete more aggressively in its current markets and open up new ones. The extended processing power gives Data General's current customers a system to move up to.

The slower-speed (1 microsecond cycle) Nova 2 systems, announced in June 1973, overlapped all models of the Nova/Supernova line except the Nova 840 and the Supernova SC. The S/100 and S/200, the first two ECLIPSE computers, overlap these two systems as well as the rest of the Nova line. Nova 2s, however, are considerably cheaper for comparable configurations. Nova 2/4 is not available in single-unit quantities, however; it must be purchased in quantities of five units. The Nova 2/10 is available at the system level in single-unit quantities.

The ECLIPSE S/100 parallels the Nova 800, Nova 1200, and Supernova computer characteristics while the S/200 parallels the Nova 840 characteristics. Both the S/100 and S/200 outperform their predecessors and offer a superset of system enhancements: error checking and correcting (ERCC) memories composed of core or MOS semiconductor (SC) modules; 16-word bipolar cache memory on SC modules; up to 8-way interleaving of core memory modules, and up to 4-way interleaving of SC memory modules; superset of the Nova/Supernova instruction set to perform bit, byte, and word data manipulations and efficient context switching and stack operations; and optional Writeable Control Store for

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**Table 1. Data General ECLIPSE: Mainframe Characteristics**

<b>MODELS</b>	S/100, S/200
<b>CENTRAL PROCESSOR</b>	
Microprogrammed	Yes
Control Memory	ROM
No. of Registers	8 accs: 4 16-bit (2 also used as index regs) and 4 64-bit for fl. pt. arithmetic
<b>Addressing No. of Wds</b>	
Direct	To 64K bytes
Indirect	Multilevel
Indexed	Yes
Mapping	No (S/100); yes (S/200 to 256K bytes)
Overflow Entry	
<b>Instruction Set</b>	
Implementation	Firmware
Types	Single & doubleword
Number	86 std, 66 opt
Floating Point	Hardware option
Hardware Stack	Yes
<b>Writable Control Store (256 56-bit words)</b>	Opt, not software supported
<b>Interrupts</b>	
Levels	16 ext
Type	Hardware
<b>MAIN STORAGE</b>	
Type	MOS, core
Cycle Time, $\mu$ sec	0.8 (core), 0.7 (MOS), 0.2 (cache)*
Basic Addressable Unit	Wd, byte
Bytes per Access	2
Cache Memory	MOS only
Capacity, bytes	
Min	16K (S/100), 32K (S/200)
Max	64K (S/100), 156K (S/200)
Increment Size, bytes	16K
Ports per Module	1
Error Checks	ERCC opt
Memory Protection	No (S/100); opt (S/200); dual user memory maps, 1 data channel mgs
<b>Overflow Entry</b>	
Memory Management	No (S/100); Yes (S/200)
Interleaving	Core; 8-way MOS 4-way
<b>INPUT/OUTPUT</b>	
Max Devices Addressable	59
Programmed I/O	Yes
DMA	Std
DMA Transfer Rate (MA2)	1,250K wds/sec

Note:

\* Effective memory cycle time varies with type of memory and number of memory modules interleaved.

use-oriented microprogramming. The model 200 offers double user maps plus a data channel map in the mapping option to cut processor overhead in context switching. Table 1 summarizes system specifications.

Many of the ECLIPSE features enhance multiprogramming and multiprocessing in communications, text processing, and process control environments. Dual processors or up to 15 processors can attach to IBM systems while controlling 32 communication lines each; configurations are also available for front-end, message-switching, and network processing. Appropriate software support is provided for most options.

Initially, all software and peripherals for the ECLIPSE computers will be the same software and peripherals available for the Nova/Supernova. No new software has yet been developed to use the unique features of ECLIPSE to best advantage. Table 2 summarizes differences between ECLIPSE and Nova 2 Computers.

First deliveries of both the S/100 and S/200 are scheduled for February 1975.

**COMPETITIVE POSITION**

With its ECLIPSE Computer, Data General does not find itself in the same position vis-a-vis Digital Equipment's PDP-11 as it was in 1968 with its Nova vis-a-vis the PDP-8. At that time, Digital had no 16-bit computer. Data General capitalized on that fact and sold its 16-bit Nova aggressively and successfully in the OEM market against the 12-bit PDP-8. In 1970, Digital introduced the 16-bit PDP-11, which was new conceptually and architecturally. Digital "bit the bullet" on software because the PDP-11 was not compatible with any of its previous computers and all software had to be developed from scratch. In the meantime, Data General developed sub-

stantial system software for its Nova/Supernova line, added optional features, and developed the Nova 840, the true forerunner of the S/200. Until now, Data General has mostly sold the Nova/Supernova against the PDP-8, not the PDP-11. The PDP-11, however, has intruded more and more into PDP-8 territory. With the ECLIPSE, Data General is now tackling the PDP-11 as a competitor.

Two things are particularly significant about the ECLIPSE. First, it is upward compatible with the Nova/Supernova computers; thus the system has a substantial body of inherited software, and Data General is not faced with a massive system software development effort. Second, Data General has rejected the unified bus in favor of a distributed bus structure with the I/O bus separate from the memory bus. It appears Data General learned from Digital's experience. The PDP-11 suffered for a couple of years after its announcement because of its lack of software.

On another front, Data General has experienced some inroads into its own Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. The Digital Computer Controls company has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line, because the expandability of the system allows memory sizes equal to the Nova 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically, the popularity of the Nova/Supernova line has been part of Data General's problem, since the underestimating of demand meant that the company slipped behind schedule from

**Table 2. Chief Differences Between ECLIPSE and Nova 2 Computers**

COMPUTER MODEL	ECLIPSE		Nova 2	
	S/100	S/200	2/4	2/10
<b>PACKAGING</b>				
No. of Slots	7	16	4	10
No. of CPU Boards	2	2	1	1
16K-wd Module	No	No	Yes	Yes
Chassis Height (in.)	5.25	10.5	5.25	10.5
<b>MEMORY</b>				
Types	Core; MOS	Core; MOS	Core	Core
Max Size (bytes)	64K	256K	64K	64K
Cycle Time	0.8 Core 0.7 MOS 0.2 Cache	0.8 Core 0.7 MOS 0.2 Cache	0.8 or 1.0	0.8 or 1.0
Memory Management Protect				
<b>CAPABILITIES</b>				
Stack Processing	Yes	Yes	No	No
Multiply/Divide	Std	Std	Opt	Opt
Microprogrammed	Yes	Yes	No	No
ERCC	Opt	Opt	No	No

**Table 3. Comparison of Floating-Point Processor Execution Times in Microseconds**

Operation	ECLIPSE			
	(core memory 4-way interleaved)	PDP-11/45 (core memory)	PDP-11/50 (MOS memory)	IBM 370/158 <sup>(1)</sup>
Load	2.8	4.8	3.4	—
Store	2.0	4.8	3.4	—
Add/Subtract	2.4	6.5	5.4	2.0
Multiply	3.9	8.2	7.1	2.0
Divide	4.6	9.9	8.8	8.6
Add/Subtract (long)	2.4	—	—	2.2
Multiply (long)	7.1	14.2	12.3	3.6
Divide (long)	7.8	17.5	15.4	23.2

Note:

(1) Times assume instruction is in buffer 90% of the time.

time to time, and impatient OEM customers bought from the smaller company. This threat was earlier counteracted by the Nova 2 line which is competitive in price and comparable in speed to the D-116.

Although Data General has compared their floating-point processor's instruction execution times with those of the IBM System/370 Model 158 (see Table 3), the real competition for the ECLIPSE system as a whole will be from systems supplied by the minicomputer manufacturers: Digital Equipment, Hewlett-Packard, Interdata, MODCOMP, Varian Data Machines, Computer Automation, General Automation, and Microdata. All of these manufacturers except Computer Automation, which caters exclusively to the OEM market, produce a broad range of processing power in their computer lines. All have discovered gold in the midcomputer range, once sparsely populated and now getting congested, but none can supply the support required by a truly novice user. All supply system software, and the user must prepare the applications software.

The ECLIPSE extends the processing power of the Nova/Supernova line and gives Data General's customers a compatible system for upgrading. In addition, it retains the relatively new Nova 2 low end of the line for the OEM market. Initial comparison of the ECLIPSE floating-point processor execution times with those for the PDP-11/45 and 11/50 indicate the ECLIPSE is faster. (See Table 1.) The cache memory and interleaving of memory modules also increase throughput substantially. Context switching and multiprogramming on larger systems are facilitated by multiple user maps in the mapping unit, and extended operation macroinstructions that, for example, call a procedure and place relevant return information on the stack all in one instruction. These features are impressive and also necessary to make the ECLIPSE truly competitive with the PDP-11 because the PDP-11 is faster than it appears by looking

at instruction execution times. The 2-address structure of the PDP-11 as well as the instruction set itself produce tight codes. Generally, fewer instructions are executed per task than on more conventional 1-address computers.

All in all, the ECLIPSE appears to be a well-conceived system from a company that has made few wrong moves in its short life. Also, the system's name "ECLIPSE" is refreshing (not a 3 in it anywhere) and perhaps prophetic. The system will certainly eclipse the Nova/Supernova and probably some competitors, but mostly it will win some and lose some to the PDP-11, HP 3000, MODCOMP I, II, IV, Varian 70, and Interdata 7/16 and 7/32.

## MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in France (Paris), West Germany (Frankfurt), England (London), Canada (Hull), and Australia (East Hawthorne-Melbourne). Customer support includes up to 10 customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, software subscription service for automatic timely updates of software and documentation, and summary of available software for users not needing revisions. The Data General User's Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special ECLIPSE computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time and materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

## COMPATIBILITY

The ECLIPSE computer is generally program-compatible with the Nova/Supernova line, given comparable configurations, but there are some restrictions. ECLIPSE computers implement multiply/divide, hardware floating point, and memory management options differently than Nova/Supernova. For the first two, the difference is chiefly a matter of coding which is easy to

change, but memory management is a little more difficult to alter, because of functional differences, such as double user maps. ECLIPSE also uses the codes for "no-load" and "no-skip" Nova options in the standard instruction set, so Nova programs with these instructions are not compatible and must be altered. A compatible program cannot contain the data channel increment, add-to-memory feature, or execution and I/O time-dependent subroutines.

Both computers use the same type of I/O bus structure, and all Nova/Supernova peripherals can attach to ECLIPSE computers.

## CONFIGURATION GUIDE

ECLIPSE S/100, the smallest model, has a memory capacity ranging from 8K to 32K words; core and semiconductor memory modules can be mixed. The CPU has space for seven standard circuit boards. The CPU occupies two boards, and each 8K-word memory module occupies one board. The remaining slots can be used for additional 8K-word memory modules, I/O subsystem controllers, and certain processor options. The S/100, which is designed for instrumentation or control applications with modest requirements, is housed in a small 5.25-inch high chassis but it can be expanded with another 16-slot chassis.

The S/200 system is a larger system designed for medium to large scale end-user applications. The 10.5-inch high chassis can hold 16 circuit boards, and it can be expanded to include another 16-slot chassis. Minimum systems include CPU, 16K words of memory and console. This can be directly expanded up to 32K words; the

Memory Allocation and Protection (MAP) option allows memory to be further expanded to 128K words (256K bytes).

The MAP option available only on the S/200 model adds 12 instructions and occupies a full printed circuit board. Other processor options, such as automatic program load, power monitor/auto restart and a real-time clock are available for both systems. The extremely fast hardware floating point processor (FPP) Data General recently introduced is also available; FPP occupies one board and adds 54 instructions to the instruction set. Another important option is Writeable Control Store, which allows users to microprogram their own instructions.

Either system can attach any of the peripherals previously available to the Nova/Supernova line. These include the wide range of high-speed, low-speed, special-purpose, and communications devices listed in Table 4.

Adapters allow the ECLIPSE systems to be configured into multiprocessor configurations. The interprocessor bus allows dual computer/shared disc systems to be configured for front-end and message switching systems needing redundant CPU. An interprocessor bus allows networks of up to 15 Data General computers (Novas, Supernovas, Nova 2s, ECLIPSES) to be interconnected. An IBM 360/370 adapter allows the ECLIPSE to be interfaced directly to an IBM system.

The various operating systems have different minimum configuration requirements. RDOS and MRDOS are the standard ECLIPSE operating systems but RTOS and SOS subsets can be used as well. Table 5 summarizes software system and includes the configuration required for each major package.

**Table 4. Data General ECLIPSE: Peripherals**

DEVICE MODEL	DESCRIPTION
<b>DISCS</b>	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K wds capacity
6000 Series	Nova discs (fixed-head), 128K, 256K, 512K, 768K wds capacity
4048A	Century 111, 3M wd capacity, IBM 2311 compatible
40578	Century 114, 12M wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M wds capacity
New	Data General, 45.9M-word capacity, like IBM 3330
<b>Magnetic Tape</b>	
4030 I-N	Wang Mag Tape Transports, 7/9-track, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-Drive versions
New	Data General Transports, 7-/9-track, 75 ips
<b>Consoles</b>	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
<b>Paper Tape</b>	
4011B/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
<b>Punched Card</b>	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cpm
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm





**Table 4. (Contd.)**

DEVICE MODEL	DESCRIPTION
<b>Printers</b>	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps
New	Data General Printer, 240, 300 lpm
<b>Displays</b>	
6010/6012	24 lines, 80 char each; 6012 has local edit
4010	Infoton Vista, 20 lines, 80 char each
<b>A/D, D/A Systems</b>	
4032	Basic A/D interface, Models 4055 A/Q converters, 8 to 15 bits, multiplexors, 2 enclosures (128 single-ended channels, 64 differential)
4037	Basic D/A control, Models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters
4085	Wide range analog input, up to 512 channels, 13 to 15 bits
<b>Plotters</b>	
4017 A-D	CalComp 565 Drum or Rack Mountable, 563 Drum, and 502 Flatbed Plotters
4017E	General Interface Board
<b>Digital</b>	
4065	I/O Interface Subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-lpm feed
4008/4079	Read-time clocks, 10/100/1,000 Hz frequencies
4040	General Interface Board
<b>Communications</b>	
4015	High-speed Controller 600-50,000 baud
4025	IBM 360/370 Interface
4038	Multiprocessor Communications Adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async, controller subsystem, up to 1,024 lines

**Table 5. Data General ECLIPSE: System Software**

PACKAGE	DESCRIPTION
RDOS	Realtime Disc Operating System, foreground/background multiprocessing, multiprogramming; requires 16K wds memory, S/100 or S/200 CPU, 2.5M disc, console
MRDOS	Mapped Realtime Disc Operating System, requires 24K wds memory, S/200 with MAP, 2.5M disc, console
RTOS	Small basic, real-time, executive, requires 4K wds of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette or mag tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV, runs under RDOS, MRDOS and SOS, requires 8K wds of memory, CPU, console

**Table 5. (Contd.)**

PACKAGE	DESCRIPTION
FORTRAN 5	Superset of FORTRAN IV, runs under RDOS or MRDOS, requires 28K wds of memory, CPU, console
ALGOL	Extended ALGOL 60, runs under RDOS or MRDOS, or stand-alone, requires 12K wds of memory, CPU, console
BASIC	2 versions, of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions require 4K, 8K and 16K wds of memory, respectively; CPU, console
Utilities	Text editor, library, loaders, debuggers

## DATA GENERAL — ECLIPSE

### PRICE DATA

Model No.	Description	Purchase Price (1) \$
S/100	Computer (microprogrammed CPU with capacity for 64K bytes of memory) with	
	16K Bytes Std Core	9,200
	16K Bytes ERCC Core	11,200
	32K Bytes Std Core	11,900
	16K Bytes Std SC	10,700
	16K Bytes ERCC SC	12,700
S/200	32K Bytes SC	14,900
	Computer (microprogrammed CPU with capacity for 256 bytes of memory) with	
	32K Bytes Std Core	16,300
	32K Bytes ERCC Core	19,300
	128K Bytes Std Core	32,500
	32K Bytes Std SC	19,300
	32K Bytes ERCC SC	22,300
	128K Bytes SC	44,500
	<b>Memories*</b>	
	16K-Byte Core	2,700
	16K-Byte ERCC Core	3,700
	16K-Byte SC Memory	4,200
	16K-Byte SC ERCC	5,200
	<b>Representative Systems</b>	
	<b>Small Process Control System including:</b>	46,600
ECLIPSE S/100		
64K Bytes ERCC Memory		
Fixed-Head Novadisc		
A/D Subsystem		
PT Reader		
Display Terminal		
<b>Remote Data Concentrator including:</b>	33,350	
ECLIPSE S/100		
48K Bytes of Memory		
Communications Interfaces		
<b>Large Data Base Management System including:</b>	186,700	
S/200 Computer		
256K Bytes of Memory		
2 3330-Type Disc Pack Drives		
Line Printer		
Card Reader		
13 Display Terminals		
<b>Large Dual Processor System for message switching or front-end processing</b>	263,000	
2 S/200 Computers each with		
256K Bytes of Memory		
3330-Type Disc Pack		
Fixed-Head Novadisc		
2 Magnetic Tape Transports		
2 Display Terminals		
<b>FORTRAN 5 System in Computation Environment</b>	81,400	
S/200 Computers		
96K Bytes of Core Memory		
64K Bytes of SC Memory		
Floating-Point Processor		
Moving-Head Disc		
Magnetic Tape Transport		
Line Printer		
Card Reader		
Display Terminal		

Notes:

\* ERCC = Error Checking and Correcting.

(1) Quantity discounts range from 10% to 40%.

### HEADQUARTERS

Data General Corporation  
Southboro MA 01772

## DATA GENERAL CORP. ECLIPSE Report Update



### COMMUNICATIONS SUBSYSTEM

Data General now offers a new communications subsystem and software to support it.

The subsystem includes the following components: ALM-16, a 16-line asynchronous multiplexor; ALM-8, eight-line asynchronous multiplexor with full modem control; SLM-2, a two-line synchronous multiplexor; and DCU/50 data control unit for high-level communications throughput. Communications Access Manager (CAM) software provides line handling support.

The DCU/50 user-programmable communications controller performs character processing and line protocol functions in parallel with a central processor or a dedicated communications processor. The unit has a 2048-byte random access bipolar memory and fast instruction execution time of 600 nanoseconds for add and subtract and 900 nanoseconds for load-store. Maximum communications throughput is 48K characters per second. Additional DCU/50s can be interfaced to a host computer's DMA channel for higher throughput and heavy data communications traffic. One control unit can support multiple protocols and up to 256 mixed synchronous and asynchronous lines connected through the ALM and SLM multiplexors.

The Communications Access Manager software includes line handling support for various lines: local asynchronous lines, remote asynchronous lines with modem

control, synchronous lines with or without modem control, and DCU/50-based communications facilities. The CAM software runs under Data General's RTOS, RDOS, and MRDOS operating systems; it has an interrupt service feature that allows it to reside on mass storage when communications tasks are not being performed.

The modular nature of CAM allows users with ALM-8, ALM-16, or SLM-2 multiplexors to add the DCU/50 controller without reprogramming the application. Portions of CAM can reside in the DCU/50, reducing the main CPU overhead for both instruction execution and character handling.

Line procedures include an asynchronous line teleprinter-oriented protocol and synchronous line BISYNC protocol. CAM provides for multi-drop lines using polled or select sequences, allowing easy system expansion. Protocols for unique I/O devices can be generated through a low-level interface incorporating user-written line procedures. A FORTRAN IV or FORTRAN 5 interface is available.

The COMGEN system generation program allows users to specify interactively standard variables such as line types, character size, control characters, buffer size, and time out intervals. Parameters for message assembly/disassembly, code conversion, and control character generation and detection can also be entered.

### PRICE DATA

	Purchase Price
DCU/50	\$ 3000
ALM-16	2640
ALM-8	2000
SLM-2	1500
Basic Subsystem (includes DCU/50 and software; ALM-16, SLM-2, data communications chassis, and cabling)	8940

### IBM 2780 EMULATOR AND HASP WORKSTATION EMULATORS

Data General computers can now work as remote job entry terminals for IBM 360/370 computers via an IBM 2780 emulator and an IBM HASP workstation emulator with multileaving and interleaving. Both programs run under Data General's RTOS and RDOS operating systems; 16K words of memory are required for the HASP program to run under RTOS and 24K words are required for RDOS.

The HASP program features full multileaving for up to seven input and seven output data streams for maximum

use of multiple devices. Data block interleaving and data compression are performed for efficient data transmission. HASP can operate with disc, magnetic tape, video display, card readers, and line printers.

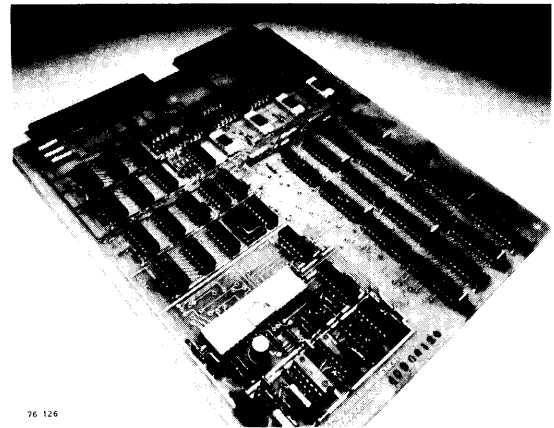
The 2780 and HASP programs are free of charge when ordered as part of a remote intelligent processing system. A minimum RTOS system that includes a processor with 16K words of core, A/N display terminals, and a line printer costs approximately \$20,000. A minimum RDOS system requires an additional 8K words of memory and a disc drive; this system costs about \$35,000.

## DATA GENERAL microNOVA System



76-127

MICRONOVA HAND-HELD CONSOLE



76-126

DATA GENERAL MICRONOVA ON A BOARD

### OVERVIEW

The microNOVA is a new member of the Data General family of NOVA<sup>®</sup> minicomputers. Based on an in-house-developed MOS microprocessor, microNOVA is the first group of Data General products to use microprocessor technology in configurations that range from single chip sets to computers-on-a-board to low-end minicomputer packages. All of the microNOVA systems are aimed at the OEM interested in microprocessor components and microprocessor-based systems.

The microprocessor/microcomputer market has been growing by leaps and bounds. This rapid growth has developed as various industries have recognized the potential of microprocessor based systems for intelligent instruments, intelligent peripherals, control and data acquisition applications, logic implementation, and consumer products.

The most attractive feature of microprocessor systems is their programmability. Programmability provides two important design advantages over hardwired special purpose systems and devices. The first design advantage is the ability to use common, well-known computer programming techniques to implement microprocessor based systems or devices.

\*NOVA is a registered trademark of the Data General Corporation.

A second advantage is inherent in the ease with which a microprocessor based system can be altered or redesigned. In many circumstances, alteration of the program code sequence may be all that's required to reconfigure a microprocessor oriented system. This contrasts with hardwired systems in which the alteration of hardwired function may require a considerable amount of redesign work, rewiring, and new physical components. In most cases, changing or upgrading a microprocessor based device is more cost effective than changing or upgrading a hardwired device.

Microprocessors cannot replace all hardwired systems. For example, in cases where fast response time (in terms of tens of nanoseconds) or the amount of power consumed is critical, microprocessors are less attractive than hardwired logic. However, in applications where slower response times are acceptable, microprocessors will have a broad impact and should be given careful consideration.

### HEADQUARTERS

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## DATA GENERAL — MICRONOVA SYSTEM

Data General offers four general types of packaging for the microNOVA:

- A microNOVA chip set (mN601 CPU, mN603 I/O Controller (IOC), mN606 4K random access memory (RAM), and System Buffer Elements (SBEs)).
- A microNOVA computer-on-a-board (Models 8562 and 8563).
- A microNOVA packaged minicomputer (Models 8560 and 8561).
- microNOVA development systems (for program development - Models 9040, 9041, 9042).

The philosophy behind this packaging is one of providing large-quantity buyers (OEMs) with a microprocessor line that has system-like features (such as hardware and software compatibility), a body of available software, peripheral offerings, and product support (including training and system documentation). This broad range of product offerings provides an integrated set of systems to the user who wants to capitalize on the advantages of distributed programmability, but has shied away from microprocessors because of the limited software available. Users of the new microNOVA line will be able to develop (or implement available) software conveniently on one of the new microprocessor-based minicomputer systems, and then imbed that software in a board or chip-oriented microprocessor system.

The microNOVA architecture is compatible with the architecture of the NOVA minicomputer family. It uses the same instruction set as the NOVA 3 and it has separate hardware stack and frame pointers for context switching and reentrant programming. Like the NOVA, the microNOVA uses a single-word instruction format as well as absolute, relative, indexed deferred, and auto-increment/decrement addressing modes.

Because the microNOVA's instruction set is compatible with that of the NOVA, it can use some of the NOVA software that is already available. All microNOVA configurations use Data General's Real-time Operating System (RTOS) which is a real-time executive with multitasking capabilities that provides standard interrupt servicing, device handling, and execution functions. In addition to RTOS, all microNOVA configurations support the symbolic Debugger, libraries for arithmetic subroutines, and character handling capabilities.

The microNOVA development systems operate under Data General's diskette-based Disc Operating System (DOS). In addition to the RTOS capabilities, DOS provides the microNOVA development systems with NOVA capabilities: command line interpreter, text editor, Macro Assembler, library file editor, relocatable loader, and FORTRAN IV compiler.

Delivery for microNOVA began September 1976. Table 1 lists microNOVA specifications.

**Table 1. microNOVA: Specifications**

<b>CENTRAL PROCESSOR</b>	
Microprogrammed	No
Stack Processing /Context Switching	Yes
No. of Programmable Registers	6 (4 accumulators, 1 stack pointer, 1 frame pointer)
No. of Inst Std Opt	30
Inst Execution Times, $\mu$ sec	—
F-P Add/Subtract	2.4
Multiply	41.3
Divide	59.0
Move	2.4
FI Add/Subtract	—
Addressing Modes	Direct, indirect, relative, indexed, auto-increment, auto-decrement
Priority Interrupt Levels	16
<b>MEMORY</b>	
Cache	No
Types	RAM/PROM
Word Length, bits	16
Cycle Time/word, $\mu$ sec	0.960
Capacity, words	—
Min	4K (2K for board only)
Max	32K
Increments	4K/8K (RAM); 5K/1K/2K/4K (PROM)
Checking Protection	— Software
<b>INPUT/OUTPUT</b>	
Max No. of Devices	61
Programmed I/O Channel	Yes
Multiplexed I/O Channel	No
Direct Memory Access (no. of channels)	1/device
Max DMA Transfer Rate (words/sec)	1M aggregate: 0.148M input or 0.173M output/channel

Notes:  
— Not applicable

## PERFORMANCE AND COMPETITIVE POSITION

Data General's microNOVA adds another well-designed product to the array at the low end of the minicomputer OEM market, which includes the Hewlett-Packard 21MX-K Series 2108K, General Automation's GA-16, the TI 990, Digital's LSI-11, and Computer Automation's LSI-3/05 and NAKED MINI. microNOVA's competitive pricing and versatility will be attractive in this market. Only the TI 990 offers an appreciable price advantage, and that is offset by the limited software available for the TI system. See Table 2 for price/performance specifications of microNOVA and its major competitors.

Now that good and relatively inexpensive hardware is readily available, users can begin to select a product for the software support provided and the service facilities available. microNOVA should score well on those considerations also. Data General offers both system and applications software for all of the microNOVA configurations. Computer Automation and General Automation offer good operating systems and additional software for both

**Table 2. microNOVA: Specifications Compared with Competitors**

	DG microNOVA	TI 990/4	Digital LSI-11	Computer Automation LSI-3/05	General Automation 16/110
Word Length, bits	16	16/16 + 1 parity	16	16	16/16 + 2 parity/ 16 + 6 EDR
Inst Times, $\mu$ sec					
Add	2.4	8.7	3.5-12.0	6.0	2.5
Multiply	41.3(1)	21.3	24-64	—	21.0
Divide	59.0	9.3	78	—	20.0
FI-P Add	—	—	42.0	—	Opt
FI-P Multiply	—	—	52-92	—	Opt
FI-P Divide	—	—	151	—	Opt
Max Memory, bytes	64K	56K	64K	32K	128K
No. of GP Registers	6	16	8	8	16
Max DMA Rate, bytes/sec	2M	DMA not supported	1.7M	1.7M	2M
Price, \$					
CPU + Memory					
8K bytes(2)	950	800(4)	990	725*	1,185
32K bytes(3)	3,745	3,400	4,370	2,650	3,045
64K bytes(3)	5,645	4,900	6,245(5)	4,450	5,525
128K bytes(3)	—	—	—	—	10,485

**Notes:**

- Not applicable because feature not available
- \* Minimum order of 5 units
- (1) Unsigned multiply and divide
- (2) CPU + memory on board
- (3) Configuration includes chassis, I/O interfaces, and console
- (4) Does not include power supply
- (5) Maximum memory is 56K bytes

batch and multiprocessing operations; Hewlett-Packard does likewise, and adds a data base management system as well. DEC offers software comparable to that available for the microNOVA systems, and in addition actively supports a users' society through which additional software is available at nominal cost. This software, however, is not guaranteed to be completely accurate or bug-free. Data General supports a similar users' group.

A big advantage, perhaps the biggest, of Data General's new product line is its availability as chip sets. This will be a cost-effective consideration for users who want to design around fairly powerful central processors without having to buy them accessorized on boards. Chip sets are a new low for minicomputer manufacturers, and Data General got there first.

One possible disadvantage of the microNOVA systems is the absence of a floating-point processor. Many OEMs will not require this feature; for those who do, DEC's LSI-11 will have the edge. Hewlett-Packard could present serious competition if they should decide to extend the HP 2100 line to chip set level. The flexibility of the 2100's instruction set (users can even devise their own instructions) and its floating-point firmware are attractive selling points as is.

Data General designed all components of the microNOVA systems and manufactures them in-house.

## COMPATIBILITY

Except for memory mapping and floating point hardware, microNOVA systems are code-compatible with Data General's NOVA 3, NOVA/SuperNOVA, and Eclipse systems. Much of the NOVA software (RTOS, DOS, and LIBRARIES) will be immediately available to the microNOVA user.

The I/O structure of the microNOVA line precludes plug-to-plug compatibility with Data General peripherals, but a relatively simple interface provides this: the General-Purpose Interface (4210) is used for programmed I/O and DMA transfers. Using IOCs, DMA input can be handled at 148K words per second, and output 173K words per second. If the user wishes to interface directly to the system bus, a more complicated interface is required, and data rates of 1M words per second can be achieved.

## CONFIGURATION GUIDE

All microNOVA configurations are based on the mN601 microprocessor. This 40-pin ceramic-packaged, 16-bit CPU features MOS technology and multiple register architecture.

In addition to the CPU, the microNOVA configurations are based on the mN606, 4,096-bit Dynamic RAM, the

## DATA GENERAL — MICRONOVA SYSTEM

mN603 I/O controller (IOC), and the System Buffer Elements (SBEs). Included among the SBEs are:

- mN634 Memory Bus Transceivers.
- mN633 Memory Address Drivers.
- mN636 IOC I/O Transceiver.
- mN506 Sense Amplifier Bus Drivers.
- mN629 CPU I/O Transceiver.

Packaging of the preceding system elements allows Data General to offer the following microNOVA configurations:

- A microNOVA chip set which includes the mN601 central processor. This chip can be purchased separately or with supporting circuit chips (mN606, mN603, and SBEs) as a package.
- A microNOVA computer-on-a-board (Models 8562 and 8563) incorporates the fully buffered mN601 with 4K words of random access memory (RAM) on one 7½ by 9½-inch printed circuit board.
- A microNOVA minicomputer which is a fully packaged, low-end minicomputer in a 9- (Model 8560) or 18- (Model 8561) slot chassis 5¼ inches high by 14½, 23½ (9-slot with battery backup), or 27½ (18-slot) inches deep. It includes 4K words of MOS memory that can be expanded to 32K words, power fail/auto restart, hardware multiply/divide, and real-time clock. The processor can address up to 61 I/O devices via an I/O bus which provides an interface between IOCs (one per device) and the central processor. The IOC chip in conjunction with the CPU provides the functional equivalent of the 47-line NOVA bus.
- microNOVA development systems, which are packaged configurations for OEMs who are developing and testing programs. The three models (9041, 9042, and 9043) differ in the console device included in the configuration: 9041 includes Teletype ASR 33, 9042 includes Teletype KSR 35, and 9043 includes a Teletype modification kit. All three models include an 18-slot minicomputer chassis, the CPU, 16K words of MOS RAM, terminal interface, power supply, battery backup, and operator's panel housed in a 72-inch cabinet, with a dual diskette system, hand-held operator's console, and the selected Teletype option.

Software support for the microNOVA line is extensive and is summarized in Table 3.

## MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, the Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in Paris, France; Frankfurt, West Germany; London, England; Hull, Canada; and East Hawthorne-Melbourne, Australia. Customer support includes up to ten customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, a soft-

**Table 3. microNOVA Software**

	Chip Sets	8562, 8563 Micro-computers	8560, 8561 Mini-computers	9040, 9041, 9042 Development Systems
RTOS (REAL-TIME OPERATING SYSTEM) <sup>1</sup> includes symbolic debugger; libraries.	x	x	x	x
DOS (DISK OPERATING SYSTEM) <sup>2</sup> includes command line interpreter; text editor; FORTRAN IV compiler; Macro Assembler; library file editor; relocatable loader; symbolic debugger; libraries; RTOS.			x	x

1 Requires 8K words of memory.  
2 Requires 16K words of memory, dual diskette, asynchronous interface, terminal.

ware subscription service for automatic timely updates of software and documentation, and a summary of available software to users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high-priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

## TYPICAL PRICES

Model	Description	Purchase Price \$
<b>DEVELOPMENT SYSTEMS</b>		
9040	microNOVA Development System w/ASR 33	12,265
9041	microNOVA Development System w/KSR 35	13,965
9041A 9042	microNOVA Development System w/Modkit	10,715
9042A 9050	Small NOVA 3 Development System w/ASR 33	13,770
9050A 9051	Large NOVA 3 Development System w/KSR 35	31,530



**TYPICAL PRICES (Contd.)**

Model	Description	Purchase Price \$			
9051A	<b>PACKAGED microNOVA MINICOMPUTERS</b>				
8560	18-Slot Minicomputer with 4K-word RAM	2,595			
8561	9-Slot Minicomputer with 4K-word RAM	1,995			
	<b>BOARD microNOVA MICROCOMPUTERS</b>				
8562	Microcomputer with 2K-word RAM	800			
8563	Microcomputer with 4K-word RAM	950			
	<b>MINICOMPUTER &amp; MICROCOMPUTER OPTIONS</b>				
8565	Automatic Program Load	150			
8575	Edge-Mounted Controls/Indicator	200			
8564	Hand-held Programmer Console	700			
8566	Battery Backup	300			
	<b>MEMORIES &amp; MEMORY SUPPORT</b>				
8572	4K-word RAM	600			
8573	8K-word RAM	950			
8567	1/2K PROM	300			
8568	1K PROM	375			
8569	2K PROM	500			
8570	4K PROM	750			
8574	PROM Programmer Board	1,650			
1116A	Qty 12 1K PROM Chips	100			
1117A	Qty 12 2K PROM Chips	250			
	<b>I/O INTERFACES &amp; DEVICES</b>				
4207	Async Board (110 to 9,600 baud)	250			
4208	Console Debug	200			
6012-H	Video Display	2,700			
4010A	33 ASR Teletype	1,750			
4010C	35 KSR Teletype	3,450			
6038	1-Drive Diskette System (157K words)	2,900			
6039	2-Drive Diskette System (315K words)	3,900			
1098A	Carton of 10 Diskettes	120			
	<b>microNOVA INTERFACING &amp; MAINTENANCE EQUIPMENT</b>				
4210	General-Purpose Interface Card	250			
4211	GPIIO Wirewrap Pins/Sockets	200			
1114	Predrilled Circuit Card	200			
2303A	Extender Card	200			
1115A	Card Puller Tool	50			
	<b>microNOVA CHIP SETS</b>				
8563A	CPU w/4K RAM	950			
4210A	General-Purpose Interface	250			
	<b>CHIPS (OEM only)</b>				
	Item	Qty	Price, \$ each	Qty	Price, \$ each
	mN601 CPU	1	225	500	95
	mN603 IOC	1	100	500	60
	mN606 4K RAM	16	24	8,000	10
	mN629 CPU IOX	1	60	500	25
	mN636 IOC IOX	1	14	500	8
	mN634 OCT MBX	2	20	1,000	8
	mN633 OCT MAD	2	20	1,000	8
	mN506 QUAD SA/BD	4	24	2,000	10





### OVERVIEW

Data General's Nova 2 line is a compact, low-cost replacement system for the Nova/Supernova line, chiefly in the OEM market. Nova 2 is functionally identical to the Nova/Supernova line architecture and compatible with all models except the Nova 840. The CPU has been redesigned to fit on a single circuit board; new low-cost core memory has been manufactured by Data General in 4K- and 8K-word modules that cycle at 800 nanoseconds and in a 16K-word module that cycles at 1,000 nanoseconds. Because Nova 2 is completely software and hardware compatible with the Nova/Supernova, it has a large body of tested facilities for support of many types of applications. Rock bottom prices, at least at this point in time, are possible because of the reduction in component size. This system unquestionably announces Data General's intention to continue vigorously competing in the OEM market, which in the past comprised around 50 percent of all installations.

Nova 2 has two submodels: the 2/4, a 4-slot system in a 5.25-inch high chassis weighing 50 pounds for a minimum system, and the 2/10, a 10-slot system in a 10.5-inch chassis weighing 110 pounds for a minimum system.

Nova 2 architecture, like the Nova/Supernova, is not microprogrammed, and it has a conventional bus arrangement. DMA and programmed I/O and a 16-level priority interrupt system are standard features. Up to 61 devices can be addressed but these can be multiplexed subsystems. Four accumulators, two of which are index registers, and 16 memory registers allow a variety of addressing modes. The instruction set allows a great many permutations of basic arithmetic and logical basic instructions so that several operations can be performed with one instruction. The memory bus is asynchronous, allowing different speed modules to be mixed on a system. In addition to manufacturing its own core, Data General has begun

making a large number of its own peripherals, including discs, magnetic tape and cassette drives, printers, paper tape readers and CRTs. Table 1 summarizes system specifications.

Software for the Nova 2 includes a Real-Time Disk Operating System (RDOS), a Real-Time Operating System (RTOS), and a Stand-Alone Operating System (SOS); FORTRAN IV, FORTRAN 5 and ALGOL compilers; BASIC interpreters; three assemblers; cross assemblers for IBM 360/370, Univac 1100, and CDC 6000 systems; and a variety of utilities and applications.

**Table 1. Data General Nova 2: Mainframe Characteristics**

<b>MODELS</b>	
<b>CENTRAL PROCESSOR</b>	
Microprogrammed	No
No. of Registers	
Accumulators	4
Hardware Index	2
Memory	16
<b>Addressing (wds)</b>	
Direct	1,024
Indirect	32K
Indexed	Yes
Mapping	No
<b>Instruction Set</b>	
Implementation	Hardware
Number	202 (counting implemented sub-instructions)
Floating Point	Option
Hardware Stack	No
Writeable Control Store	No
<b>Interrupts</b>	
Levels	16
Type	Hardware
<b>MAIN STORAGE</b>	
Type	Core
Cycle Time, $\mu$ sec	0.8, 1.0*
Basic Addressable Units	Word, byte
Capacity, bytes	
Min	8K
Max	64K
Increment Size (bytes)	8K, 16K, 32K
Ports per Module	1
Error Checks	Parity option
Memory Protection	No
Memory Management	No
Interleaving	Up to 8-way core, 4-way on MOS
<b>INPUT/OUTPUT</b>	
Max Devices Addressable	59
Programmed I/O	Yes
DMA	Std
DMA Transfer Rate	1,250K wds/sec

*Note:*

\*Effective memory cycle time varies with type of members and number of memory modules interleaved.

## DATA GENERAL — NOVA 2/4 AND 2/10 SYSTEM REPORT

The Nova 2 systems were announced in June, 1973 and first delivered in 1973.

### COMPETITIVE POSITION

Data General has experienced some inroads on its Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. The Digital Computer Controls (DCC) company has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line, because the expandability of the system allows memory sizes equal to the Nova 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically the popularity of the Nova/Supernova line has been part of Data General's problem; the company underestimated demand, slipped behind schedule from time to time, and as a result impatient OEM customers bought from the smaller companies. This competitive threat is counteracted by the Nova 2 line which is very competitive in price, comparable in speed, flexibility, and size.

The small size and reduced number of components work together to make the Nova 2 very competitive with one-board OEM minis and microcomputers from other manufacturers such as Computer Automation and General Automation. The 16K-word memory board allows the user more memory for a very small price increase over the minimum system and at prices lower than minimum systems of a year ago. This can save both OEM and end-user costs because of the ability to handle high-level languages in the larger memory, sometimes cutting programming time and costs by more than half.

The capabilities of the Nova 2 are expanded in Data General's compatible ECLIPSE® line. The ECLIPSE family of computers is Data General's most recent line of general-purpose minicomputers. The ECLIPSE systems

run the gamut of the Nova/Supernova line that they replace, but with a variety of features added to increase speed and throughput; to add to system reliability and error handling; and above all to expand the flexibility of the system while maintaining compatibility with all Nova and Supernova models. With this line, Data General hopes to compete more aggressively in its former end-user markets while opening up new ones. The extended processing power gives Data General's current customers a system to move up to, and, as the line develops, they will undoubtedly find even more upward possibilities. OEM customers with greater speed, size, and checking requirements will be also interested in ECLIPSE. Table 2 highlights some of the chief differences between the Nova 2 and the ECLIPSE systems.

As the second largest minicomputer manufacturer, Data General has the worldwide service and support capabilities so important to many OEM manufacturers. These facilities are receiving increased emphasis, with two new software support services recently announced.

### CONFIGURATION GUIDE

Data General introduced the Nova computers in 1973 as their OEM line. The minimum order for this equipment was five. To bring the price/performance advantages of the Nova 2 to the end user, Data General has announced end-user systems built around the Nova 2s, available in single quantities. These Nova 2 end-user systems now use the standard Data General operating systems.

The chief difference between the Nova 2/4 and 2/10 models is in packaging. The 2/4 is housed in 5.25-inch high chassis with four slots, while the 2/10 is housed in a 10.5-inch high chassis with 10 slots. The CPU in both cases is contained on a single circuit board, and single board modules are available for 4K words, 8K words,

**Table 2. Chief Differences Between ECLIPSE and Nova 2 Computers**

COMPUTER MODEL	ECLIPSE		Nova 2	
	S/100	S/200	2/4	2/10
<b>Packaging</b>				
No. of Slots	7	16	4	10
No. of CPU Boards	2	2	1	1
16K-wd Module	No	No	Yes	Yes
Chassis Height (in.)	5.25	10.5	5.25	10.5
<b>MEMORY</b>				
Types	Core; MOS	Core; MOS	Core	Core
Max Size (bytes)	64K	256K	64K	64K
Cycle Time	0.8 Core 0.7 MOS 0.2 Cache	0.8 Core 0.7 MOS 0.2 Cache	0.8 or 1.0	0.8 or 1.0
Memory Management Protect				
<b>CAPABILITIES</b>				
Stack Processing	Yes	Yes	No	No
Multiply/Divide	Yes	Std	Opt	Opt
Microprogrammed	Yes	Yes	No	No
ERCC	Opt	Opt	No	No

\* Registered trademark of Data General Corporation.

and 16K words of core. The 16K-word module is available only in the slower memory, 1.0 microsecond cycle time, however. Different speed memory modules can be mixed on one system. Options for Nova 2 systems include:

- Hardware multiply divide.
- Hardware floating-point arithmetic.
- Turnkey console.
- Power monitor/auto restart.
- Automatic program load.

Both can attach an expansion chassis adding 16 more slots.

## MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, the Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in Paris, France; Frankfurt, West Germany; London, England; Hull, Canada; and East Hawthorne-Melbourne, Australia. Customer support includes up to 10 customer training courses of-

fered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, a software subscription service for automatic timely updates of software and documentation, and a summary of available software for users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special ECLIPSE computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high-priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

Minimum systems include 4K words of memory. These can be expanded up to 32K words of memory with console, peripherals, communication devices, and so on attached. Peripherals of all sorts are available, as noted in Table 3. Configuration requirements are basically determined by the operating system, language processors,

**Table 3. Data General Nova 2: Peripherals**

DEVICE MODEL	DESCRIPTION
<b>DISCS</b>	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K wds capacity
6000 Series	Nova discs (fixed-head), 128K, 256K, 512K, 768K wds capacity
4048A	Century 111, 3M wd capacity, IBM 2311 compatible
40578	Century 114, 12M wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M wds capacity
New	Data General, 45.9M-word capacity, like IBM 3330
<b>Magnetic Tape</b>	
4030 I-N	Wang Mag Tape Transports, 7/9-track, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-Drive versions
New	Data General Transports, 7-/9-track, 75 ips
<b>Consoles</b>	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
<b>Paper Tape</b>	
4011B/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
<b>Punched Card</b>	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cpm
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm
<b>Printers</b>	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps
New	Data General Printer, 240, 300 lpm
<b>Displays</b>	
6010/6012	24 lines, 80 char each; 6012 has local edit
4010	Infoton Vista, 20 lines, 80 char each
<b>A/D, D/A Systems</b>	
4032	Basic A/D interface, Models 4055 A/Q converters, 8 to 15 bits, multiplexors, 2 enclosures (128 single-ended channels, 64 differential)
4037	Basic D/A control, Models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters

Table 3. (Contd.)

DEVICE MODEL	DESCRIPTION
4085	Wide range analog input, up to 512 channels, 13 to 15 bits
<b>Plotters</b>	
4017 A-D	CalComp 565 Drum or Rack Mountable, 563 Drum, and 502 Flatbed Plotters
4017E	General Interface Board
<b>Digital</b>	
4065	I/O Interface Subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-lpm feed
4008/4079	Read-time clocks, 10/100/1,000 Hz frequencies
4040	General Interface Board
<b>Communications</b>	
4015	High-speed Controller 600-50,000 baud
4025	IBM 360/370 Interface
4038	Multiprocessor Communications Adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async, controller subsystem, up to 1,024 lines

and so forth which are used. Operating systems and their requirements are listed in Table 4.

Data General also offers a dual-processor shared-disc configuration using Nova 2/10s. Each processor has 32K words of memory, a real time clock, and a console terminal. The two CPUs are housed in a dual cabinet and connected by an interprocessor bus. They share a disc subsystem which can include anywhere from 2.5M to 200M words of storage.

The interprocessor bus consists of the following components:

- Buffer — Under control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors both request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — Carries the data for intercomputer communication.
- Dual one-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The Multiprocessor Communications Adapter (MCA) interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of one million bytes per second.

## COMPATIBILITY

The Nova 2 Systems are software compatible, given comparable configurations, with all Nova/Supernova computers except the Nova 840. The line is also software

Table 4. Data General Nova 2: System Software

PACKAGE	DESCRIPTION
RDOS	Realtime Disc Operating System, foreground/background multiprocessing, multiprogramming; requires 16K wds memory, S/100 or S/200 CPU, 2.5M disc, console
MRDOS	Mapped Realtime Disc Operating System, requires 24K wds memory, S/200 with MAP, 2.5M disc, console
RTOS	Small basic, real-time, executive, requires 4K wds of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette or mag tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV, runs under RDOS, MRDOS and SOS, requires 8K wds of memory, CPU, console
FORTRAN 5	Superset of FORTRAN IV, runs under RDOS or MRDOS, requires 28K wds of memory, CPU, console
ALGOL	Extended ALGOL 60, runs under RDOS or MRDOS, or stand-alone, requires 12K wds of memory, CPU, console
BASIC	2 versions, of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions require 4K, 8K and 16K wds of memory, respectively; CPU, console
Utilities	Text editor, library, loaders, debuggers

compatible with the ECLIPSE line except for a few instructions relating to optional features, like signed hardware multiply divide.

Peripherals from all three lines are interchangeable.

**PRICE DATA**

Number	Description	Purchase \$ (1)	Monthly Maint. \$
<b>DATA GENERAL NOVA 2/4 &amp; 2/10 CENTRAL PROCESSORS &amp; WORKING STORAGE</b>			
Nova 2/4 Processors (4 accs; PIO bus; 17-level interrupt; DMA; 4 additional subassembly slots; rack mountable)			
8331	With 4K Words of Core Memory	3,500	40
8332	With 4K Words of Core Memory	4,000	52
8333	With 16K Words of Core Memory	5,600	64
8334	With 24K Words of Core Memory	7,600	96
8335	With 32K Words of Core Memory	9,100	108
Nova 2/10 Processors (4 accs; PIO bus; 16-level interrupt; DMA; 10 additional subassembly slots; rack mountable)			
8351	With 4K Words of Core Memory	4,400	44
8352	With 8K Words of Core Memory	4,900	56
8353	With 16K Words of Core Memory	6,500	68
8354	With 24K Words of Core Memory	8,500	100
8355	With 32K Words of Core Memory	10,000	112
<b>Memories</b>			
8300	Memory with (4K words)	2,000	20
8301	Memory with (8K words)	2,200	32
8302	Memory with (16K words)	3,500	44
<b>Processor Options</b>			
8306	Power Monitor and Auto Restart	400	1
8307	Multiply/Divide	1,600	13
8308	Automatic Program Load	400	2
8020	Floating-Point Processor	4,000	32
<b>Packaged Systems</b>			
Nova 2/10 RTOS Systems			
<b>System A</b>			
9001	Part 1 consists of 8358 Nova 2/10 Computer (with 16,384-word core memory in tabletop enclosure, 8306 power monitor and auto restart, 4007 I/O interface subassembly, 4010 Teletype/video display I/O interface and 4008 real-time clock)	9,150	102
900XA	Part 2 consists of a 4010A Teletype model 33ASR keyboard/printer (for 9001, 9002, 9003, 9004)	1,750	102
Nova 2/10 SOS Systems			
<b>System A</b>			
9005	Part 1 consists of 8353 Nova 2/10 Computer (with 16,384-word core memory and slides for rack mounting, 4007, 4010, 4011 paper tape reader control, 6013 high-speed paper tape reader and 4012 paper tape punch control)	11,000	135
	Part 2 consists of 4010A, 4012A High-speed Paper Tape Punch, and 1012I Single-Bay Rack Cabinet (for 9005, 9006)	5,100	135
Nova 2/10 RDOS Systems			
<b>System A</b>			

**PRICE DATA (Contd.)**

Model Number	Description	Purchase \$ (1)	Monthly Maint. \$
9011	Part 1 consists of 8355 Nova 2/10 Computer (with 4007, 4010, 4011, 6013, 4046 moving head disc control, 4047 moving head disc adapter and power supply, and 5 remaining slots in computer chassis)	19,450	237
90XXH	Part 2 consists of 4010A, 4047A Moving Head Disc Drive with 1.247 Million Words capacity; 4047C Disc Cartridge, and 1012I Single-Bay Rack Cabinet (for 9011, 9012)	7,900	257
9022	Dual Nova 2/10 System Part 1 consists of 8355 Nova 2/10 Computer (with 8306, 8308, 4007, 4008, 4010, 4119, 4011, 6013, 4240 interprocessor bus, 4046, 4047, and 4 remaining slots in computer chassis)	22,600	510
9022A	Part 2 consists of 40101, 1065I Interprocessor Bus Cable, 4047B, 4047C and 1012G 2-Bay Rack Cabinet	13,400	510
9023	Part 3 consists of 8355 Nova 2/10 Computer 8306, 8308, 4007, 4008, 4010, 4240, 4046, and 4 remaining slots in computer chassis	18,850	510
9023A	Part 4 consists of 4010A, EC4047 Moving Head Disc Adapter and Power Supply Cable, and IC4011 Paper Tape Reader Control Cable	2,250	510

*Notes*

(1) Nova 2/4 is available only in minimum quantity orders of 5 systems.

**HEADQUARTERS**

Data General Corporation  
Southboro MA 01772







# DATA GENERAL CORP.

## Nova 3

Data General has announced a new member of its NOVA<sup>®</sup>3 family of computers; a new 32K-word memory board for the NOVA 3 line, and the DASHER<sup>®</sup> family of terminal printers for the NOVA and ECLIPSE<sup>®</sup> systems.

### NOVA 3/D

The NOVA 3/D, announced August 1976, is the new high end of the NOVA 3 family. As an extension to the NOVA 3/12, the NOVA 3/D offers as standard features a Memory Management and Protection Unit (MMPU), dual operations capability, and the new 32K-word MOS memory modules. Otherwise, it is not much different than the 3/12 and is about the same price. The combination of the memory management and protection system and the new 32K-word memory boards should give enhanced performance over the 3/12 when used for multi-programming; for example, the NOVA 3/D can run a multitasking real-time program in the foreground and either a remote job entry or local batch program in the background.

The capability of the NOVA 3/D to run two different systems programs simultaneously and independently has been dubbed "dual operations capability" by Data General. Both systems running under dual operations have access to all the hardware resources of the configuration.

A basic 3/D configuration consists of 12 slots for memory and control boards, a central processor with a 32K-word MOS memory with parity, MMPU, automatic program load, power-fail/auto-restart, and battery back-up. The price for one system is \$14,400. Large quantity discounts are also available. The basic configuration can be extended to 128K words of core, semiconductor, or mixed memory with hardware multiply/divide, hardware floating point, real-time clock, and expansion chassis. Any NOVA peripherals can be attached to the system, and any NOVA software can be run on the 3/D including Real-Time Disc Operating System (RDOS), Disc Operating System (DOS), Real-Time Operating System (RTOS), extended FORTRAN IV and FORTRAN 5, ALGOL, BASIC (single-user and multi-user), and Macro Assembler.

Cycle times for memory modules are  
MOS – 700 nanoseconds  
8K core – 800 nanoseconds  
16K core – 1,000 nanoseconds.

The MOS modules can be incremented in 4K-, 8K-, and 16K-word increments and have optional parity. The memory management system provides dual mapped program spaces allocatable in 1K-word increments with 32 registers in each of two program spaces, a total of 64 data channel map registers, and 32K-word unmapped program space. User programs have access to a maximum of 128K words via four address extension maps – the two program maps and the two data channel maps. MMPU used with RDOS makes dual operations possible on the 3/D.

### Competitive Position

The NOVA 3/D competes with Hewlett-Packard's 21MX and Digital Equipment's PDP 11/34 and 11/45. The NOVA 3/D central unit is less expensive than any of these, but the price of a system with foreground multi-tasking and background batch would depend more on the peripheral equipment than on the central unit configuration, so that equivalent systems could be expected to cost about the same in the final analysis. Actual performance comparisons will have to wait until the systems are benchmarked against one another. Table 1 compares the 3/D with its major competitors.

The PDP 11/34 would seem to be the most direct competitor of the 3/D in price and performance. The PDP 11/45 is more powerful than the 3/D and offers a second high-speed channel to memory, but it is harder to operate and the central unit is more expensive. The HP 21MX is also more expensive than the 3/D and slower in operation and user microprogramming capabilities. However, the 21MX offers a data base management system.

### Compatibility

The NOVA 3/D is hardware and software compatible with the NOVA line of minicomputers and can run Data

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### HEADQUARTERS

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Table 1. NOVA 3/D Compared with Major Competitors

	NOVA 3/D	PDP 11/34	PDP 11/45	HP 21MX
<b>CENTRAL PROCESSOR</b>				
Microprogrammed	No	Yes	Yes	Yes
Hardware Multiply/Divide	Opt	Std	Std	Std
Floating-Point Hardware	Opt	Opt	Opt	Std
User Microprogramming	No	No	No	Yes
Data Structure	16-bit wd	2x8-bit bytes	2x8-bit bytes	16-bit wd
<b>MEMORY</b>				
Type	MOS, core	MOS, core	MOS, core bipolar	MOS
Min Size, MOS (wds)	32K	16K	16K	4K
Max Size, MOS (wds)	128K	128K	128K	196K
Min Increment Size, MOS (wds)	4K	16K	1K	4K
Min Size, Core (wds)	8K	16K	16K	—
Max Size, Core (wds)	128K	128K	128K	—
Min Incr, Core (wds)	8K	8K	8K	—
Cycle Time, MOS (μsec)	0.700	0.725	0.495	0.650
Cycle Time, Core (μsec)	0.800, 1.0	0.725	0.90	—
Memory Management	Std	Std	Opt	Opt

Note:  
— Not applicable

General's ECLIPSE programs as well. An interface and emulation programs allow communications with IBM System/360 and 370 mainframes. Emulators are also available for other mainframes, as well as a considerable range of software from independent vendors. The basic compatibility of all Data General machines facilitates movement within the family lines.

**NEW 32K MEMORY BOARD**

The new memory board may be used on all NOVA 3 computers. It utilizes a conventional two-layer printed circuit board and is organized around Data General's own 4K RAM chips. An alternate board, using Texas Instruments parts, is also available. The board is 15 inches square and contains 144 memory chips, memory refresh control, and interfacing logic. The board is also used in the Data General microNOVA equipment. N-channel silicon-gate technology and a 20-pin package are used. Access time is 160 nanoseconds. Use of the board facilitates dual operation in the NOVA 3/D and faster throughput in the NOVA 3 line in general.

**DASHER TERMINAL PRINTERS**

Data General has gradually been reducing its dependence on outside peripheral manufacturers. The new DASHER printers represent one more step toward independence. They are designed for reliability and maintainability, with all electronics on five removable boards. One module contains the operating logic. Four other modules control carriage drive, paper feed, ribbon drive, and keyboard array. Interconnections and multiple parts are minimized. Four versions are available:

- 6042 30-cps send-receive
- 6043 30-cps receive only
- 6040 60-cps send-receive
- 6041 60-cps receive only.

Keyboard models can be used off-line as typewriters. Form widths from 4 to 15 inches can be accommodated

and forms may be placed anywhere on the carriage. The 60-cps printer may be operated at 30 cps also.

The terminals are compatible with Teletype and other ASCII devices. They can be interfaced to a 20-mA current loop or EIA RS232-C controller. The standard character set contains 96 characters for upper- and lowercase. English, French, German, Swedish, Japanese, and other character sets are available. Twenty-nine function codes may be added optionally by using control character codes; 128-character formats are available, but are mutually exclusive with the optional 29-function-code set. When not printing, the carriage automatically moves, permitting the user to view the last six characters printed.

**TYPICAL PRICES**

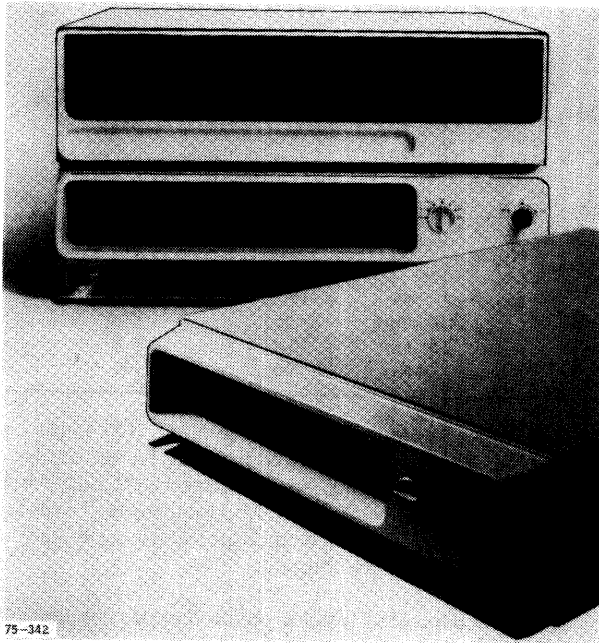
Description	Purchase Price* \$ (Maint. not Incl.)
<b>NOVA 3/D</b>	
NOVA 3/D with 32K words of MOS memory with parity, MMPU, automatic program load, power-fail/auto-restart and battery backup	14,400
NOVA 3/D with 48K words of core memory, MMPU, power-fail/auto-restart, automatic program load, real-time clock, 10-megabyte disc, flexible diskette, Data General 30-cps & 60-cps DASHER terminal printers	36,800
NOVA 3/D with 96K words of 700-ns MOS memory with parity, MMPU, battery backup, memory parity control, power-fail/auto-restart, automatic program load, real-time clock, two 10 megabyte discs, 300-lpm printer, 75-ips magnetic tape drive, 30-cps DASHER terminal printer, & 4 CRT displays	86,950
<b>Memory</b>	
8602 65K bytes of MOS Memory	4,500
8603 32K bytes of Core Memory	8,500
Model 6042 — 30-cps, Keyboard Send/Receive Terminal	2,400
Model 6043 — 30-cps, Receive-Only Terminal	2,200
Model 6040 — 60-cps, Keyboard Send/Receive Terminal	2,650
Model 6041 — 60-cps, Receive-Only Terminal	2,450

Note:  
\* Prices are for single quantity orders.



## DATA GENERAL CORP.

### Nova 3 System Report



#### OVERVIEW

The Nova 3 line is Data General's most recent line of 16-bit minicomputers aimed primarily at the OEM (Original Equipment Manufacturers) market. Like the Eclipse line, Nova 3 extends the previous Nova/Supernova architecture to include stack processing and facilities for more efficient memory management, without loss of compatibility with all previous Nova systems. The Nova 3 line is compact like the Nova 2, but it is faster, less expensive and more versatile, and can support four times as much memory. The Nova 3 essentially replaces all of the Nova/Supernova line, with the exception of some of the larger configurations of the 830 and 840.

The main competitive challenge of the Nova 3 is toward neither the microcomputer (computer-on-a-board) segment nor the midcomputer segment of the market but rather it is toward the central OEM market that has been the mainstay of all minicomputer manufacturers. The popular Nova architecture is retained and extended by Nova 3. Thus, Nova 3 enters the market with a tried-and-true design and a body of proven software larger than that of any other 16-bit system in the marketplace. Best of all, Nova 3s are cheaper than any comparable Data General systems on the market and can use the 700-nanosecond MOS memories produced using Data General's own memory chassis. Table 1 compares the Nova 2, Nova 3, and Eclipse lines.

Like the Nova 2, the Nova 3 has two submodels designated by the number of slots that can be included in the main chassis. Model 3/4 has four slots, and it is housed in a half-size chassis, which is useful for applications requiring a small computer in a restricted space. Up to 32K words of memory can be included in the chassis by using two 16K-word memory boards. Model 3/12 has 12 slots, and up to 128K words (256K bytes) can be housed in the mainframe. But, memory beyond 32K words requires the memory management option. The 3/12 can also attach a 12-slot expansion chassis.

Nova 3 has all the features associated with the Nova/Supernova line plus extensions for stack processing and efficient memory management. Two hardware stack registers have been added to the usual Nova complement of 4 hardware registers, 1 program counter, and 16 autoincrement/autodecrement memory registers. Addressing modes include direct, relative, indexed, and multilevel indirect addressing in various combinations. The register-based stack addressing is on a last-in/first-out and random-indexed basis. The bus system includes separate I/O and memory buses with both standard-speed and high-speed modes on the DMA channels. Up to 61 devices can be addressed, with a supporting 16-level priority interrupt system. The Nova/Supernova instruction set has been expanded to include single-word PUSH/POP and multi-word SAVE/RETURN stack instructions, memory management instructions, and a trap for undefined instruction codes. The trap allows user-defined instructions or emulation of the instructions unique to the Eclipse systems. Thus, Nova 3 can be made compatible with Eclipse.

All previous Nova/Supernova peripherals can be attached to the Nova 3, including discs, tapes, card and paper tape I/O, printers, analog/digital systems, plotters, terminals, communications subsystems, and a variety of other special peripheral devices and subsystems. Data General has recently redesigned its communications subsystems, adding modular programmable multiplexors that can operate from very low to very high speeds.

The MOS memory modules are made up of 4K-bit, n-channel, 20-pin MOS RAM chips manufactured by Data

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# DATA GENERAL — NOVA 3 SYSTEM REPORT

**Table 1. Chief Differences Between Eclipse, Nova 2, and Nova 3 Computers**

COMPUTER MODEL	Eclipse		Nova 2		Nova 3	
	S/100	S/200	2/4	2/10	3/4	3/12
<b>PACKAGING</b>						
No. of Slots	7	16	4	10	4	12
No. of CPU Boards	2	2	1	1	1	1
16K-wd Module	No	No	Yes	Yes	Yes	Yes
Chassis Height (in.)	5.25	10.5	5.25	10.5	5.25	10.5
<b>MEMORY</b>						
Types	Core; MOS	Core; MOS	Core	Core	Core; MOS	Core; MOS
Max Size (bytes)	64K	256K	64K	64K	64K	256K
Cycle Time, $\mu$ sec	0.8 (Core) 0.7 (MOS); 0.2 (Cache)	0.8 (Core); 0.7 (MOS); 0.2 (Cache)	0.8 or 1.0	0.8 or 1.0	0.8 or 1.0 (Core); 0.7 (MOS)	0.8 or 1.0 (Core); 0.7 (MOS)
Memory Management	No	Opt	No	No	No	Opt
Protect	No	Opt	No	No	No	No
<b>CAPABILITIES</b>						
Stack Processing	Yes	Yes	No	No	Yes	Yes
Multiply/Divide	Std	Std	Opt	Opt	Opt	Opt
Microprogrammed	Yes	Yes	No	No	No	No
ERCC	Opt	Opt	No	No	No	No

**Table 2. Data General Nova 3: Mainframe Characteristics**

<b>MODELS</b>	3/4 and 3/12
<b>CENTRAL PROCESSOR</b>	
Microprogrammed	No
No. of Registers	4
Accumulators	2
Hardware Index	2
Hardware Stack	2
Memory	16
Addressing (wds)	
Direct	1,024
Indirect	32K
Indexed	Yes
Mapping	Option on 3/12
Instruction Set	
Implementation	Hardware
Number	212 (counting implemented sub-instructions)
Floating Point	Option
Hardware Stack	Std
Writeable Control Store	No
Interrupts	
Levels	16
Type	Hardware
<b>MAIN STORAGE</b>	
Type	Core/MOS
Cycle Time ( $\mu$ sec)*	0.8, 1.0 (Core); 0.7 (MOS)
Basic Addressable Units	Word, byte
Capacity (bytes)	
Min.	8K (Core); 4K (MOS)
Max.	32K (3/4); 128K (3/12)
Increment Size (bytes)	8K, 16K, 32K
Ports per Module	1
Error Checks	Parity option on MOS
Memory Protection	On 3/12 with MMU
Memory Management	On 3/12
Interleaving	Up to 8-way, core; 4-way, MOS
<b>INPUT/OUTPUT</b>	
Max. Devices Addressable	59
Programmed I/O	Yes
DMA	Std
DMA Transfer Rate (bytes/sec)	434K
DMA High-Speed Mode (bytes/sec)	2.2M, input; 1.66M, output

\* Effective memory cycle time varies with type of memory and number of memory modules interleaved.

General at its Sunnyvale, California plant. The chips are assembled, wired, and packaged in Hong Kong, returned to Sunnyvale for testing, then incorporated into MOS memory modules at Southboro, Massachusetts. Texas Instruments 4K-bit chips will be incorporated in a substantial number of the Nova 3s shipped.

The CPU uses MSI bipolar technology throughout.

Data General offers the 700-nanosecond memory with or without parity. Parity is unavailable for the 800- and 1,000-nanosecond core memory modules. A battery back-up for power loss is also available for systems with MOS memory. Maximum memory capacity is 128K words. Memory expansion beyond 32K words requires the memory management unit, which provides two program maps and two data channel maps but no protection facilities. Data General Nova 3 software does not support dual program maps, thus these features are useful only for OEMs who write their own software.

Software for Nova 3 consists of the software available for the rest of the Nova line: Real-Time Operating System (RTOS), Real-Time Disc-Based Operating System (RDOS), and Mapped Real-Time Disc-Based Operating System (MRDOS). High-level languages include Assembler, Macro Assembler, ALGOL, Extended BASIC, FORTRAN IV, and FORTRAN 5. Table 2 lists the mainframe characteristics.

Nova 3 was announced in October 1975. Deliveries will begin in January 1976.

## Competitive Position

Data General spokesmen use the term "vertical integration" to mean company manufacture and control of all the pieces in a Data General computer system. Manufacturing as many parts as possible allows the company to add value all along the way and to make money doing so. Data

General is selling the Nova 3 only in system packages; this discourages users from adding plug-compatible memories from independent manufacturers.

Data General spokesmen indicated that no plans are afoot to offer board-only or stripped systems. These spokesmen appear happy to let others fight for the low profits inherent in this market; they seem unconcerned that competitors will capture entry-level customers who may upgrade someday. Thus, competitors for Nova 3 are minicomputer *systems*: Digital PDP-11/04, 11/35, and 11/45; Hewlett Packard HP 21MX; Modular Computer Systems MODCOMP II; Interdata 7/16 and 7/32; General Automation GA-16 Series; and Digital Computer Controls 16 Series. Table 3 compares Nova 3 with the PDP-11/04, GA-16/330, PDP-11/45, and HP 21MX.

The PDP-11/45 is more powerful than Nova 3, and it is also considerably more expensive. Also, COBOL is available for the PDP-11/45 and currently unavailable for Nova 3.

The HP 21MX is slower than Nova 3 and also more expensive. Hewlett Packard systems are usually priced higher than those from other minicomputer manufacturers. The company generally does not play cost-cutting games but counts on its service, maintenance support, and software to justify higher prices. For example, IMAGE/2000, a data base management system similar to TOTAL, is available for the 21MX.

The GA-16/330 is somewhat slower than the Nova 3 and also more expensive. COBOL is now available for the GA-16 Series. Other members of the GA-16 Series, such as the GA-16/220, also compete with smaller configurations of the Nova 3.

Digital's PDP-11/04 is also very competitive for smaller Nova 3 configurations. It is a low-cost system that can be upgraded through the whole PDP-11 line.

On one hand, the Nova 3 is a relatively unexciting system because it offers nothing really new. On the other hand, Nova 3 is a very important system for Data General and for other minicomputer manufacturers because it does the same old things very well at a very attractive price.

The price/performance of the Nova 3/4 and 3/12 packages will be hard to beat. Data General knows the OEM market and likes to sell to it. The Nova 3 reflects both this knowledge and desire. Although the result isn't a masterpiece, it should satisfy the user who wants a solid system he can afford.

## CONFIGURATION GUIDE

The Nova 3 line consists of two models that differ in the number of slots in the basic chassis. The number of slots determines the expansion capabilities of the basic system; thus, the Nova 3/4, with a 4-slot chassis, has been designed for small configurations, and the Nova 3/12, with a 12-slot

chassis, is for large configurations. The 3/12 can support an expansion chassis that provides 12 additional I/O slots. Figure 1 shows the typical layout of the slots on a 3/12 system.

A minimum system includes 4K words of memory. Memory for Nova 3 can consist of 700-nanosecond MOS memory available in modules of 4K, 8K, and 16K words, or 800/1,000-nanosecond core memory available in modules of 8K or 16K words. Core cycle time is 800 nanoseconds for 8K-word modules and 1,000 nanoseconds for 16K-word modules.

The following options are available for the Nova 3:

- Memory mapping.
- Battery backup.
- MOS memory parity.
- Hardware multiply/divide (signed).
- Hardware floating-point arithmetic.
- Turnkey console.
- Power monitor/auto restart.
- Automatic program load.

Peripherals of all sorts are available, as noted in Table 4. Configuration requirements are determined by the operating system, language processors, and application programs. Operating systems and their requirements are listed in Table 5.

Data General also offers a dual-processor, shared-disc configuration using Nova 3. Each processor has 32K words of memory, a real-time clock, and a console terminal. The two CPUs are housed in a dual cabinet and are connected by an interprocessor bus. They share a dual-ported disc subsystem which can include anywhere from 2.5M to 200M words of storage.

The interprocessor bus consists of the following components:

- Buffer — Under the control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — These lines carry the data for intercomputer communications.
- Dual one-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The Multiprocessor Communications Adapter (MCA) interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of one million bytes per second.

## Compatibility

The Nova 3 systems are software and hardware compatible with all previous Nova and Supernova systems, including the Nova 2. Software developed for Eclipse sys-

# DATA GENERAL — NOVA 3 SYSTEM REPORT

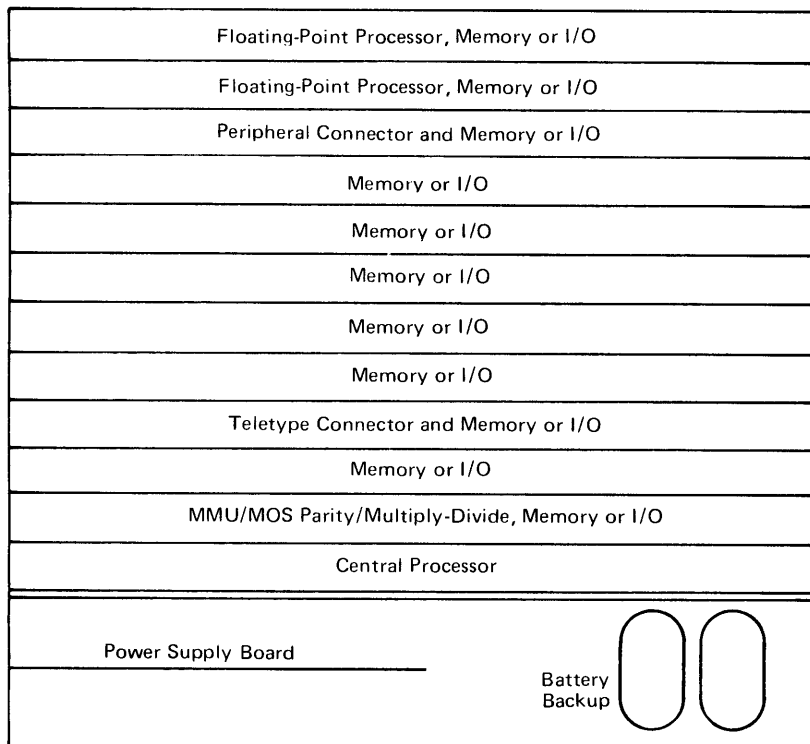
**Table 3. Data General Nova 3 Compared with Major Competitors**

	Data General Nova 3	Digital PDP-11/04	General Automation GA-16/330	Digital PDP-11/45(1)	Hewlett Packard HP 21MX
Word Length (bits)	16/16 + 1 parity	16	16/16 + 2 parity	16/16 + 2 parity	16
Inst. Times (μsec)					
Add	1.8	3.2	4.6	0.8-1.8	1.9
Multiply	6.9(2)	NA	21.2	3.6-4.7	12.8
Divide	7.5(2)	NA	20.3	7.5-8.6	17.0
Floating Pt. Add	7.7*	—	*	2.8-6.5*	22-54*
Floating Pt. Multiply	11.3*	—	*	3.0-8.2*	48-57*
Floating Pt. Divide	13.7*	—	*	3.0-9.9*	41-76*
Max. Memory (bytes)	64K/256K	56K	128K	253,952	512K
No. of GP Registers	4	8	16	16	4
Max DMA Rate (bytes/sec)	2M	2.8M	2M	2M	1.2M
Price, \$					
CPU + Memory					
32K bytes	4,400	(3)	5,250	23,900	7,650
64K bytes	7,100	(3)	8,250	32,000	11,800
256K bytes	34,200	—	—	55,500(4)	36,150

\* Optional, at extra cost.    NA - Not available.    — Not applicable.

**Notes:**

- (1) The PDP-11/45 can use core, MOS, or bipolar memories; the first number is for bipolar memory and the second number for core memory. Price is for core memory.
- (2) Operands are unsigned integers on std.
- (3) Digital has not announced price of unbundled memory although the 11/04 can support 56K bytes. Price for 16K-byte system with 9-slot chassis is \$3 545.
- (4) Maximum memory is 253,952 bytes.



**Figure 1. Nova 3/12 Slot Allocation**

**Table 4. Data General Nova 3: Peripherals**

DEVICE MODEL	DESCRIPTION
<b>Discs</b>	
4019 A/B/C	Alpha Data (fixed-head); 64K, 128K, 256K-wds capacity
6000 Series	Nova discs (fixed-head); 128K, 256K, 512K, 768K wds capacity
4048A	Century 111; 3M wds capacity; IBM 2311 compatible
40578	Century 114; 12M wds capacity; IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge); 1.2/2.4M wds capacity
6030/6031	Data General; 45.9M wds capacity; like IBM 3330
<b>Magnetic Tape</b>	
4030 I-N	Wang mag tape transports; 7-/9-track; 12.5/45/75 ips
4000 Series	Nova cassettes; 1-, 2-, or 3-drive versions
New	Data General transports; 7-/9-track; 75 ips
<b>Consoles</b>	
4010 A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
<b>Paper Tape</b>	
4011B/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
<b>Punched Card</b>	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cpm
4016H-L	Mark sense card readers, 150/285/400/600/1,000 cpm
<b>Printers</b>	
4034A/B	Data Products 356/245 lpm; 80/132 cols
4034C/D	Centronics, 165 cps
New	Data General printer; 240/300 lpm
<b>Displays</b>	
6010/6012	24 lines, 80 char each; 6012 has local edit
4010	Infoton Vista; 20 lines, 80 char each
<b>A/D, D/A Systems</b>	
4032	Basic A/D interface, Models 4055 A/O converters; 8 to 15 bits; multiplexors; 2 enclosures (128 single-ended channels, 64-differential)
4037	Basic D/A control, for 24 converters
4085	Wide range analog input; up to 512 channels; 13 to 15 bits
<b>Plotters</b>	
4017A-D	CalComp 565 drum or rack mountable; 563 drum, and 502 flatbed plotters
4017E	General interface board
<b>Digital</b>	
4065	I/O interface subassembly; 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools; 500-lpm feed
4008/4079	Real-time clocks; 10/100/1,000 Hz frequencies
4040	General interface board
<b>Communications</b>	
ALM-8	Async multiplexor for 4 or 8 lines; to 9,600 baud
ALM-16	Async multiplexor for 8 or 16 lines; to 9,600 baud
SLM-2	Sync multiplexor for 1 or 2 lines; to 56K baud
DCU/50	Communication control unit for up to 256 async and sync lines

**Table 5. Data General Nova 3: System Software**

PACKAGE	DESCRIPTION	PACKAGE	DESCRIPTION
RDOS	Real-time Disc Operating System, foreground/background multiprocessing; multiprogramming; requires 16K wds memory, CPU, 2.5M wd disc, console	FORTTRAN 5	wds of memory, CPU, console Superset of FORTRAN IV; runs under RDOS or MRDOS; requires 28K wds of memory, CPU, console
MRDOS	Mapped Real-time Disc Operating System; requires 24K wds memory, with MAP, 2.5M disc, console	ALGOL	Extended ALGOL 60; runs under RDOS or MRDOS, or stand-alone; requires 12K wds of memory, CPU, console
RTOS	Small basic, real-time, executive; requires 4K wds of memory, real-time clock, CPU console	BASIC	2 versions of Dartmouth BASIC; 1 for single-user calculator mode, 1 for 16 users
SOS	Subset of RDOS for minimum stand-alone; non-disc systems; cassette or mag tape I/O	Assemblers	Standard, relocatable, and macro versions; require 4K, 8K, and 16K wds of memory, respectively, CPU, console
FORTTRAN IV	Extended ANSI FORTRAN IV; runs under RDOS, MRDOS, and SOS; requires 8K	Utilities	Text editor, library, loaders, debuggers

## DATA GENERAL — NOVA 3 SYSTEM REPORT

tems can run on the Nova 3 by trapping Eclipse instructions that have not been implemented on the Nova 3 and emulating them in software. Peripherals common to Nova, Supernova, and Eclipse systems can be attached to the Nova 3.

Communications software includes emulators for IBM 2780 terminals and HASP workstations.

### MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; 8 in Canada; 3 each in France, England, and Spain; 5 in West Germany; 2 in Australia; and 1 each in Austria, the Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in Paris, France; Frankfurt, West Germany; London, England; Hull, Canada; and East Hawthorne-Melbourne, Australia.

### TYPICAL PRICES

Model Number	Description	Purchase Price \$	Monthly Maint. \$
	Nova 3/4 Computer, includes chassis with 4 slots and either MOS or core memory		
8478	With 4K words of MOS	2,600	38
8479	With 4K words of MOS with parity	3,700	36
8480	With 8K words of MOS	3,200	46
8481	With 8K words of MOS with parity	4,500	44
8482	With 8K words of core	3,700	50
8483	With 16K words of MOS	4,400	56
8484	With 16K words of MOS with parity	6,100	54
	Nova 3/12 Computer, includes chassis with 12 slots for memory or I/O controllers and either MOS or core memory		
8486	With 4K words of MOS	3,600	44
8487	With 4K words of MOS with parity	4,700	42
8488	With 8K words of MOS	4,200	52
8489	With 8K words of MOS with parity	5,500	50
8490	With 8K words of core	4,700	56
8491	With 16K words of MOS	5,400	62
8492	With 16K words of MOS with parity	7,100	60
8493	With 16K words of core	6,200	66
8494	With 32K words of MOS	8,100	102
8495	With 32K words of MOS with parity	10,800	98
	Memory Management Unit, 8533 Subassembly Board, 8530 Automatic Program Load, and 8531 Power Fail/Automatic Restart		
8496	With 32K words of core	9,700	110
	Configured Systems, Nova 3/12, with 8535		
8500	With 32K words of MOS and 8532 battery backup	11,400	127
8501	With 32K words of MOS with parity, 8536 Parity Control, and 8532 Battery Backup	13,900	124
8502	With 32K words of core	12,500	135
	Nova 3 Options		
8020	Floating Point Unit	4,000	32
8530	Automatic Program Load	400	2
8532	Battery Backup	500	10
8533	Option Subassembly	200	2
8534	Multiply/Divide	1,400	12
8535	Memory Management Unit	2,800	28
8536	Parity Control	500	5
8537	Expansion Chassis for 3/12 only	2,000	20

Note: Nova 3 uses the same peripherals as the other Nova computers.



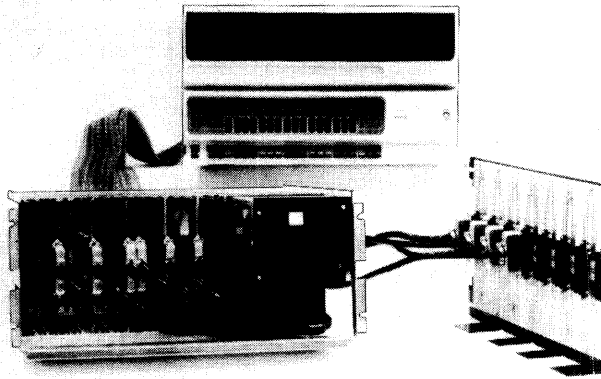
Customer support includes up to ten customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, a software subscription service for automatic timely updates of software and documentation, and a summary of available software to users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special Nova 3 computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high-priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.



## DATA GENERAL CORP.

# Nova 3 System Report Update



76-165

### SENSOR I/O SUBSYSTEM

A new sensor I/O subsystem extends the utility of Eclipse and Nova computers into process control and other applications involving analog-digital I/O functions.

Data General's Data Acquisition and Control subsystem (DG/DAC) interfaces Eclipse and Nova computers to a wide variety of sensors, actuators, and associated electrical circuits with full analog-digital interaction. Each DG/DAC chassis has 16 I/O card slots, control card, power supply, bus terminals and cables, and two terminal boards for sensor signal connections. Up to 16 cards in any assortment (input or output, analog or digital) plug into each DG/DAC chassis; each card handles up to 16 lines. Cards are available for high-speed precision A/D conversion of low-level analog inputs, for high-level voltage ranges, for multiplexing single-ended, differential and current-loop levels, for all common digital signals, and for digital output. Digital signals can be pulsed DC, AC Triac, Form A and Form C relay, and TTL.

DG/DAC subsystems interface to a Nova or Eclipse I/O bus either directly or through a Data General Data Control Unit (DCU) option. The DCU is a dedicated I/O processor

with its own I/O bus, 1K-word semiconductor memory, computer interface, and real-time clock. The central processor uses the DCU to load programs, start and stop execution, run diagnostics, and perform routine operations such as scans, limit and validity checks, conversion calculations, and timed I/O sequences. The DCU can access the main computer for data transfers, or for additional program instructions, or to report status or events. The central processor can interrupt the DCU to issue new commands, change priorities or modify programs. Exchanges operate over the CPU data channel to minimize system response time and line-handling overhead and to make available the CPU's resources for more complex tasks. Multiple DCUs can be configured in one computer.

Two central processors can access a single DG/DAC chassis or a series of daisy-chained chassis. Control can also be alternated between computers or DCUs.

Software support for the DG/DAC subsystems is provided by the Sensor-Access Manager (SAM), a library of device-handlers and subroutines to control I/O transfers between user programs and A/D sensor devices. SAM runs under the real-time operating systems (RTOS, RDOS, and MRDOS); SAM routines can be called by Fortran IV and 5 and Assembly Language programs.

DG/DAC configurations can range from a very basic one-chassis system for the smallest lab or industrial job to a fully-expanded four-chassis model with up to 1,000 A/D lines to handle the most complex data acquisition and control applications. A typical basic DG/DAC subsystem with 64 A/D lines costs \$5,200; a dual-chassis configuration with 500 A/D lines is priced at about \$19,800. A complete system that includes an Eclipse® S/200 CPU with 32K-word memory, diskette subsystem, 10Mb cartridge disc storage, display terminal, DG/DAC chassis with I/O cards for 215 lines, cabling and interfaces, and two-bay cabinet sells for about \$51,500. Deliveries will begin in August, 1976.

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### OVERVIEW

Data General's Nova and Supernova product line includes 10 Nova systems (Nova, Nova 800, 800 Jumbo, 820, 830, 840, 1200, 1210, 1220, and 1230) and two Supernova systems. The Nova/Supernovas are small-scale, general-purpose, 16-bit computers, oriented toward control, scientific, laboratory, and time-sharing applications.

All of the systems currently marketed are upward compatible and differ mostly in memory speed, price, and packaging. All use the same mass storage units, peripheral devices, and software. The Novas utilize core memories in their basic configurations but can support both read-only memory (ROM) and core memory on a single system. The Supernovas utilize core or read/write semiconductor memory in basic system configurations (a Supernova system with semiconductor memory is called Supernova SC). In addition, each can support a combination of ROM, core, and read/write semiconductor memories.

Core memory cycle time is 800 nanoseconds for the Nova 800, Nova 800 Jumbo, Nova 820, Nova 840, and Supernova, 1.0 microseconds for the 830, and 1.2 microseconds for the Nova 1200, 1210, 1220, and 1230. The Supernova SC has the fastest cycle time: 300 nanoseconds. The first Nova, which is available but no longer marketed, has a cycle time of 2.6 microseconds.

The original members of the product line were the Nova and Supernova systems. As the 1200 Series, 800 Series and Supernova SC were added to the line one at a time, they had clearcut differences in performance. However, Data General has responded to the needs of its user community by adapting options originally aimed at the top of the line (as it was defined at a particular point in time). In this way, most users could benefit.

The high-speed data channel is a case in point. Originally it was an option available only for the two Supernovas. This fact, coupled with the Supernovas' greater memory speeds, made them clearly the top of the line. Now differences between the Nova 800 and Supernova processors have been considerably leveled. In fact, the high-speed data channel is standard for all Novas (still optional on Supernova). The Nova 830 and 840 (which are 800 Jumbos with memory management and protection) are the only models able to expand main memory to 128K words through the new memory management and protection unit.

The memory for the 1200 line (cycle time: 1,200 nanoseconds per word) is available in modules of 4K, 8K, and 16K words. Memories for the 800 line are available in modules of 4K and 8K words for the Nova 800 and 820. The 8K-word module is also available for the Nova 840. The 16K-word module for the Nova 830 has a 1.0-microsecond cycle time.

In addition to 2K, 4K, 8K, and 16K core increments, Novas can increment core with 1K-word modules but Supernova cannot; on the other hand, read/write semiconductor memory increments of 256, 512, and 1,024 words are available only for the Supernova.

There are still a few differences among the 800, 1200, and Supernova Series other than memory speeds, but these are not as distinctive as the capabilities that set the Nova "mapped" 830 and 840 apart from the rest of the line. The memory allocation and protection option, available to all of the Supernova and Nova 800 Series but not to the Nova 1200 Series, functions in a limited way like the 830/840 memory management and protection unit by mapping up to 32K words of memory for time sharing. Tables 1 and 2 list current similarities and differences between Nova and Supernova processors.

The Dual Nova computer system is a dual-processor/shared-disc system, built around two or three standard Data General computers (Nova 1200 Jumbo and Nova 830 or 840), one moving-head or fixed-head disc, and the Real-Time Disc Operating System (RDOS).

The advantages of a dual-processor configuration are continual system availability even when one processor is down, plus shared program and data-base files. The first processor can gather and reduce incoming data and monitor real-time operations. The second processor, used in the background mode, can develop new programs or carry out batch processing. Using the Multiprocessor Communications Adapter (MCA), processors can access each other through the I/O bus.

Where high throughput and continuity are prime considerations, the dual-processor system can handle many communication lines and data rates that peak at unpredictable times. The first processor stores or forwards messages to the second processor for peak times. The second processor shares the message load (doubling throughput), handles peak data rates, and controls the switching if the

**Table 1. Data General Nova and Supernova: Common Characteristics**

<b>PROCESSOR</b>	
Power Monitor/Auto Restart	Opt
No. of Instructions	202
Hardware Registers	2
Memory Registers	16
Hardware Accumulators	4
Word Size (bits)	16
Decimal Arithmetic	No
Floating-Point Hardware	Opt
<b>I/O</b>	
Max Devices Addressable	62
Programmed I/O	Yes
DMA Channel	Yes
Interrupt Levels	16
<b>MEMORY</b>	
Min ROM (wds)	256
Max ROM (wds)	31,744
Parity	No
ROM increments (wds)	256; 512; 1,024
<b>SOFTWARE</b>	
Assemblers	3
DOS, RDOS, SOS, RTOS	Yes
Compilers	
FORTRAN	Yes
ALGOL	Yes
Interpreter	
BASIC	Yes

first processor is down. The second processor can also accumulate network statistics, compile management reports, and generate customer service charges.

In a time-sharing situation where common access to programs is needed yet file protection is required, each processor functions as an independent time-sharing system. All terminals can handle Extended BASIC.

For customer service scheduling, the first processor controls the terminals and gathers the customer service requests. The second processor analyzes the data, bills the

customers, and performs engineering calculations in batch mode. It also aids the first processor in peak times.

Data General states that the Dual Nova is well suited for supervisory control, front-end processing, data acquisition, point-of-sale systems, hospital patient monitoring, and data entry.

Along with processor development, Data General continues to fill out its line of available mass storage units and peripheral devices and to enhance its software support for the Nova and Supernova. Currently, the firm offers a variety of models and well-integrated hardware and software packages for its minicomputer systems. The company began manufacturing peripherals with the introduction of the Novadiscs, which are a series of fixed-head disc drives with capacities ranging from 128K to 768K words. To date, Data General has added a series of cassette drives, magnetic tape drives, 6013 high-speed paper tape reader, and two CRTs (the 6010 and 6012) to its roster of in-house peripherals. The company also manufactures its own cores.

Data General has developed comprehensive software that will run on both the Nova and Supernova under two types of disc operating systems that have file handling capability. Both disc operating systems, DOS and RDOS, control relocatable assemblers; loader math library; BASIC, ALGOL and FORTRAN compilers; text editor; symbolic debugger; and command line interpreter. DOS was previously the basic operating system. The newer RDOS, a real-time disc operating system, has all of the facilities of DOS as well as foreground/background processing plus multiprocessor and shared disc capabilities. RDOS is now the basic operating system. Subsets of RDOS, called SOS and RTOS, are also available for small stand-alone systems without disc. All of the operating systems will support one of two BASIC interpreters, one for a single user and one for up to 32 time-sharing users. ALGOL 60, and FORTRAN IV can run stand alone or

**Table 2. Data General Nova and Supernova: Differences between Models**

Characteristic	Nova	Nova 800, 820, 800 Jumbo	Nova 830	Nova 840	Nova 1200, 1230	Nova 1210, 1220	Supernova	Supernova SC
<b>PROCESSOR</b>								
Auto Program Load	—	Opt	Opt	Opt	Opt	Opt	Std	Std
Total Subassembly Slots	7	7; 10; 17	17	17	7; 17	4; 10	7	11
<b>MEMORY</b>								
Capacity (K wds)	32	32	128	128	32	24; 32	32	32
Core Increments (wds)	1; 2; 4; or 8K	1; 2; 4; or 8K	16K	8K	1; 2; 4; or 8K	1; 2; 4 or 8K	2; 4; or 8K	2; 4; or 8K
Read/Write SC Memory Increments (wds)	—	—	—	—	—	—	—	256; 512; 1,024
Memory Protect	—	Opt	Opt	Std	—	—	Opt	Opt
Memory Management	—	—	Opt	Std	—	—	—	—
<b>SPEED</b>								
Core Cycle (μsec)	2.6	0.8	1.0	0.8	1.2	1.2	0.8	0.8
SC Cycle (μsec)	—	0.8	—	0.8	1.2	1.2	0.3	0.3
Interrupt Response Time (μsec)	40.0	11.0	—	11.0	17.8	17.8	9.8	9.8
Transfer Rates (K wds/sec)								
DMA	285	1,250	—	1,250	833.3	833.3	500	500
High-Speed Data Channel	—	1,250	—	1,250	—	—	1,250 (opt)	1,250 (opt)



under DOS or RDOS. RDOS also supports a macro assembler and Fortran 5 (a superset of ANSI FORTRAN, IBM Level H FORTRAN, and Univac FORTRAN V). FORTRAN 5 is designed to optimize a user's entire program so that its efficiency compares to a program written in assembly language.

Multiply/divide and floating point are options available to all processors either as hardware units or as software subroutines.

In addition, Data General provides three cross-assemblers to prepare Nova/Supernova programs on the IBM System 360/370, Univac 1108, and CDC 6600 computers. These assemblers are written in FORTRAN and are compatible with the Nova/Supernova extended assembler.

Data General announced the first Nova in September 1968 and the first Supernova in August 1969. Substantial price cuts for the Supernova were made in September 1970. In October 1970, Data General introduced the Nova 800 and 1200 and the Supernova SC memory modules. In May 1971, the Nova 800 and 1200 Jumbos (subsequently the designation for the 1200 Jumbo was changed to Model 1230) were announced. The Nova 820, 1210, and 1220 were announced on November 10, 1971. The Nova 840 was shown at the Fall Joint Computer Conference in December 1972. Recently, (fall 1974) Data General announced that the 830 combines new lower-cost memory modules in the 840 configuration.

## COMPETITIVE POSITION

The Nova/Supernova line has been Data General's mainstay for the last few years. It has held its own against stiff competition from companies like Digital Equipment, Hewlett-Packard, General Automation, Honeywell, and Varian. Although the company introduced the microprogrammed Eclipse line in 1974 to replace the Nova/Supernova line and to extend the market upward for Data General computers, the company still plans to keep the Nova/Supernova line current for awhile. Thus Model 830 and a series of lower-cost memories have been introduced to reduce the cost of all systems.

In the development of its systems, Data General has consistently utilized the latest technology to improve the price/performance of its systems; all have the same basic logical design as the first Nova. Thus, all software developed for previous models is compatible with new models, even the new Nova 2 and Eclipse systems, which are compatible in most respects and thus can build on the Nova/Supernova software base. The firm steadily continues to develop system software, and the available software is substantial.

Data General has a large OEM and end-user customer base, which is necessary to support continued system development. An increasing number of small business computer manufacturers are using Nova/Supernova processors as the heart of their systems. In addition, the ROLM Corporation builds a Ruggednova for military applications, and licenses the Nova/Supernova software for it.

Data General claims to be number 2 in minicomputer sales and deliveries, having shipped more systems than any other manufacturer except Digital; the company has a firm grip on around 15 percent of the market. This sales record results from Data General's aggressive marketing combined with its ability to produce and deliver systems with attractive price/performance ratios. Data General markets its systems for all minicomputer applications.

A good mix of hardware/software is available for Nova and Supernova minicomputers. The peripherals equipment complement compares quite favorably to that of competitors (particularly noteworthy is the assortment of disc units, the communications subsystems, and the special peripherals associated with numerical control). The Novadisc was Data General's first peripheral; the company now also manufactures the 6013 High-Speed Paper Tape Reader, the 6010 and 6012 CRT Displays, magnetic tape drives, and the Novacassette.

Nova/Supernova's DOS and RDOS operating systems are versatile in their support of an assembler; BASIC, FORTRAN, and ALGOL compilers; and a command language interpreter. RDOS is noteworthy for its ability to handle dual processors combined with a shared-disc environment and multiprocessor networks.

Data General has experienced some inroads on its Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. Digital Computer Controls has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line because the expandability of the system allows memory sizes equal to the Nova 830 and 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically, the popularity of the Nova/Supernova line has been part of Data General's problem; underestimating demand caused the company to slip behind schedule from time to time in the past, and impatient OEM customers bought from the smaller company. This threat is really counteracted more by the Nova 2 (OEM) line, which is competitive in price and comparable in speed. Meanwhile, addition of the Eclipse line, extending into the upper end of the market, provides an attractive upward path for users who anticipate growing systems needs.

Thus, Data General's recent announcements at the upper and lower ends of the market, consistent with the continuing expansion of the Nova/Supernova hardware and software base, put the firm in an aggressive posture

across the entire range of the minicomputer market. Indications are that Data General can hold its own in the marketplace and gradually increase its share at the expense of the weaker, smaller minicomputer manufacturers.

### User Reactions

The Data General users interviewed predictably exhibited a wide range of applications and systems sizes as well as a range of reactions to the system.

Installations included a software house with a number of accounting, inventory, order entry, and forecasting systems installed among its customers; a ship voyage accounting firm; a university physics laboratory; and an investment firm.

All users interviewed felt the system was very reliable. One OEM user, a software service bureau with a number of systems, remarked that he had "blown" only two 8K-word core boards in 2 years; other than that, he has had no downtime. Remarks about service showed more variety; several users of various size systems said it was fine; one user said it was excellent (2-hour response time during emergency), while another (small) user reported problems with slow response. The dissatisfied user remarked that several other small users in his area with down systems had occasionally come to "borrow" his system during off-hours. Although this added to his impression of slow service, he added that the system was very reliable and he had no complaints on that score.

User reactions to Data General software were generally positive. A user of RDOS Version III on three Nova 800s (32K words of core each) had previously used DOS 5 but switched operating systems because of the type of file-handling capabilities and the new editing commands; he was quite satisfied with the change. Other users had no complaints about the way Data General's software functioned. One small user, with a 12K-word Nova 1200 system without disc, mourned that Data General's software development appeared to be aimed at larger disc-based systems and nothing seemed to come in his direction. One user stayed with FORTRAN IV rather than buy the additional memory needed for FORTRAN 5; he said his application was I/O-bound not compute-bound, so he did not need optimized code.

### CONFIGURATION GUIDE

A basic Nova/Supernova central processor includes four accumulators (two of which can be used as index registers); a single-line, 16-level priority interrupt system; a programmed I/O channel; and a direct memory access (DMA) channel. Supernova processors also include an automatic program load feature initiated from the console; automatic program load is an optional feature for the Nova 800 and 1200 Series. The basic processor includes only add and subtract arithmetic operations; hardware multiply/divide and floating point

can be added as options. Each central processor unit is rack mountable or fits in a tabletop enclosure. Table 2 shows the differences in processor submodels.

Working storage for all the Nova/Supernova processors is provided by storage modules that can be added in any combination up to a maximum size of 32,768 words (131,072 words for the Nova 830 and the Nova 840 with a memory management and protection option). All use magnetic core memory except the Supernova SC, which uses semiconductor memory. In addition, read-only memory (ROM) modules are available in 256- to 1,024-word modules. ROM modules and core memory modules can be added in any combination, but total memory size cannot exceed 32,768 words without the memory management and protection option.

Up to 58 I/O devices can be connected to a Supernova and 61 to a Nova. All devices connect to the programmed I/O channel for the transfer of control information. Slow-speed devices such as console typewriters, punched card, paper tape, and line printers also use the programmed I/O channel for data transfers. High-speed devices, such as magnetic tape and disc, transfer data via the DMA channel or via the high-speed data channel if included in the system. Table 3 lists the various models of peripheral devices available.

**Table 3. Data General Nova and Supernova: Peripherals**

Device Model	Description
<b>Discs</b>	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K-wd capacity
6000 Series	Nova Discs (fixed-head), 128K, 256K, 512K, 768K-wd capacity
4048A	Century 111, 3M-wd capacity, IBM 2311 compatible
40578	Century 114, 12M-wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M-wd capacity
<b>Magnetic Tape</b>	
4030 I-N	Wang magnetic tape transports, 7/9-trk, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-drive versions
6020 Series	7/9-trk dual-head, 75 ips, up to 8 drives/controller
4080 Series	Cassette subsystem, 50K wds/cassette, single/dual triple transports, 7 to 8 transports/controller
<b>Consoles</b>	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
<b>Paper Tape</b>	
4011/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
<b>Punched Card</b>	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cps
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm
<b>Printers</b>	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps

**Table 3. (Contd.)**

<b>Displays</b>	
6010/6012	24 lines, 80 char each, local edit (6012)
4010	Infoton Vista, 20 lines, 80 characters each
<b>A/D, D/A Systems</b>	
4032	Basic A/D Interface, models 4055 A/Q converters, 8 to 15 bits; multiplexors, 2 enclosures (128-single-ended channels, 64 differential)
4037	Basic D/A control, models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters
4085	Wide-range analog input, up to 512 channels, 13 to 15 bits
<b>Plotters</b>	
4017 A-D	CalComp 565 drum or rack mountable 563 drum, and 502 flatbed plotters
4017E	General Interface Board
Digital 4065	I/O interface subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-lpm feed
4008/4079	Real-time clocks, 10/100/1,000-Hz frequencies
4040	General Interface Board
<b>Communications</b>	
4015	High-speed controller, 600-50,000 baud
4025	IBM 360/370 interface
4038	Multiprocessor communications adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async controller subsystem, up to 1,024 lines

Dual Nova multiprocessor configurations are hardware and software supported. Each processor has 64K bytes of memory and an interprocessor bus for communication between computers. High-level languages and utility software are included. Under RDOS, both computers have on-line access to programs and data files. Hardware-multiplexed data paths allow access to the data base and programs by both processors. Each processor is independent, but both share the same disc data base.

Three types of disc storage available for the Dual Nova configuration are as follows:

- Fixed-head Novadisks — 256K to 1,536K-byte capacity; up to 8 million bytes of Novadisk storage used for a Dual Nova configuration; provides fast access.
- Moving-head disc with cartridge drives — Removable cartridge model with 2.49 million-byte capacity; one fixed and one removable disc unit with 4.9 million-byte capacity; up to 20 million bytes shared

in a Dual Nova configuration; convenient mass storage.

- Moving-head disc pack drives — 24.944 million-byte capacity; almost 200 million bytes accessible in a Dual Nova configuration.

Combinations of fixed and moving-head discs can be used in configurations. Maximum disc storage is obtained with eight moving-head disc packs (200 million bytes) and 8 million bytes of fixed-head storage.

Communication between the two processors is handled via the interprocessor bus. The bus consists of the following components:

- Buffer — Under control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors both request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — This part carries the data for inter-computer communication.
- Dual 1-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The MCA interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of 1 million bytes per second. These types of multiprocessor network configurations are software supported under RDOS.

Software packages and the minimum configurations required are listed in Table 4.

## COMPATIBILITY

All Nova/Supernova processors are compatible and use the same instruction set as well as the same peripheral and mass storage devices. All currently available software can run on all the Nova/Supernova computers, if the processor can support the required configuration. Software for mapped systems, for instance, must run on an 830 or 840. Cross-assemblers are available so that users with an IBM System/360 or 370, Univac 1108, or CDC 6600 can utilize their more powerful processing capabilities to assemble Nova/Supernova programs. Nova 2 processors are completely compatible with the small processors at the low end of the line.

The Eclipse computer is generally program-compatible with the Nova/Supernova line, given comparable configurations; there are only a few restrictions. Eclipse computers have implemented multiply/divide, hardware floating point, and memory management options differently. In the first two cases the difference is chiefly a matter of coding, which is easy to change. But, memory management is more difficult to alter. Eclipse also uses the codes for "no-load" and "no skip" Nova options for the standard set, so Nova programs with these instructions are not compatible. A compatible program cannot

**Table 4. Data General Nova and Supernova: System Software**

Package	Description
RDOS	Real-time disc operating system, foreground/background multiprocessing, multiprogramming; requires 16K words of memory, CPU, 2.5M disc, console
RTOS	Small basic, real-time, executive; requires 4K words of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette, mag tape, card or paper tape I/O
FORTTRAN IV	Extended ANSI FORTTRAN IV; runs under RDOS and SOS; requires 8K words of memory, CPU, console
FORTTRAN 5	Superset of FORTTRAN IV; runs under RDOS; requires 28K words of memory, CPU, console
ALGOL	Extended ALGOL 60; runs under RDOS or is stand-alone; requires 12K words of memory, CPU, console
BASIC	2 versions of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions; require 4K, 8K, and 16K words of memory, respectively, CPU, console
Utilities	Text editor, library, loaders, debuggers

contain the data channel increment, add-to-memory feature, or execution- and I/O-time-dependent subroutines.

All three computer lines use the same type of I/O bus structure; thus all Nova/Supernova peripherals can attach to Eclipse and Nova 2 computers.

### MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in France (Paris), West Germany (Frankfurt), England (London), Canada (Hull), and Australia (East Hawthorne-Melbourne). Customer support includes 2 to 10 customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers that help users apply their systems, a software subscription service for automatic timely updates of software and documentation, and a summary of available software for users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special Eclipse computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. For a monthly charge, a factory service contract allows equipment to be rapidly fixed at a repair depot. On-call service contracts provide preventive maintenance checks and high-priority emergency service to the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

### TYPICAL PRICES

Model Number	Description	Purchase \$	Monthly Maint. \$
<b>CENTRAL PROCESSORS AND WORKING STORAGE</b>			
4001	Nova Processor	3,950	34
4006	Nova Options	400	1
4022	Power Monitor and Auto Restart	250	NC
4024	External I/O Cable Connector	1,850	10
4031	Expansion Chassis	2,000	16
4003	Multiply/Divide	3,650	28
4004	Nova Memories (16 bit words; 2.6-μsec cycle time)	2,700	20
8016	4,096-Word Core Memory	4,100	32
8230	8,192-Word Core Memory	6,600	53
8231	Nova 800 Processor	8,000	64
8232	With 4K Words of Core Memory	11,200	99
8233	With 8K Words of Core Memory	14,400	134
8235	With 16K Words of Core Memory	7,450	60
8236	Jumbo, with 4K Words of Core Memory	8,850	71
8237	Jumbo, with 8K Words of Core Memory	12,050	106
8238	Jumbo with 16K Words of Core Memory	15,250	141
8239	Jumbo with 24K Words of Core Memory	18,450	176
8253	Nova 820 Processors (with 7 additional subassembly slots)	6,100	63
8254	With 4K Core Memory	7,500	74
8264	With 8K Core Memory	10,700	109
8285	With 16K Core Memory (2 8K modules)	13,900	144
8286	With 24K Core Memory (3 8K modules)	17,100	179
8286	With 32K Core Memory (4 8K modules)		
8139	Nova 800/820 Processor Options	100	NC
8159	Turn-key Console	125	NC
8206	Turn-key Console	400	1
8207	Power Monitor and Auto Restart	1,000	8
8208	Nova 800/820 Multiply/Divide	400	2
8209	Automatic Program Load	3,500	28
8222	Memory Protection and Allocation (for Nova 800 only)	250	NC
8224/5	External I/O Cable Connector (for Nova 800 only)	1,850	10
8281	Expansion Chassis	1,850	10
8268	Expansion Chassis (adds 10 I/O subassembly slots)		
8269	Nova 800/820 Memories	2,500	24
8226/77	Core Memory	3,200	35
8227/78	4K Words	900	9
8228/79	8K Words	1,450	13
	16K Words	1,950	20
8264	Nova 840 Processors	16,530	134
8265	With 16K Words of Core Memory (expansion to 64K words)	13,230	106
8290	With 16K Words of Core Memory (expansion to 64K words; wiring only for memory management and protection; includes 2025 jumper card)	19,730	169
8291	With 24K Words of Core Memory (expansion to 64K words)	22,930	204
8292	With 32K Words of Core Memory (expansion to 64K words)	26,130	239
8293	With 40K Words of Core Memory (expansion to 64K words)	29,330	274
8294	With 48K Words of Core Memory (expansion to 64K words)	35,730	344
8295	With 64K Words of Core Memory (expansion to 80K words)	45,130	438
8296	With 80K Words of Core Memory (expansion to 128K words)	51,530	508
8297	With 96K Words of Core Memory (expansion to 128K words)	64,330	648
8298	With 128K Words of Core Memory	16,430	141
8299	With 24K Words of Core Memory (wired for memory management and protection only)	19,630	176
8269	With 32K Words of Core Memory (wired for memory management and protection only)	3,200	35
8206	Nova 840 Memories	400	1
8207	Core Memory (8K words)	1,000	8
8208	Nova 840 Processor Options	400	2
8021	Power Monitor and Auto Restart	3,500	28
8222	Multiply/Divide	250	NC
8224	Automatic Program Load	1,850	10
8283	Memory Management and Protection Unit	3,000	34
	External I/O Cable Connector		
	Expansion Chassis (adds 7 I/O subassembly slots)		
	Memory and I/O Expansion Chassis (provides 15 additional slots)		
	Nova 830 with Memory Management and Protection Option		





**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase \$	Monthly Maint. \$
8244	With 16K Words of Core Memory	12,650	NA
8245	With 32K Words of Core Memory	16,150	NA
---	With 64K Words of Core Memory	23,150	NA
---	With 16K-Word Memory Board (1.0 μsec cycle time)	3,500	
	<b>NOVA 1200</b>		
	<b>Nova 1200 Processors</b>		
8182	With 4K Words of Core Memory	5,100	40
8183	With 8K Words of Core Memory	5,950	52
8184	With 16K Words of Core Memory	7,550	64
8185	With 24K Words of Core Memory (1 16K module and 1 8K module)	9,550	96
8186	With 32K Words of Core Memory (2 16K modules)	11,050	108
8187	Jumbo with 4K Words of Core Memory	5,950	44
8188	Jumbo with 8K Words of Core Memory	6,800	56
8189	Jumbo with 16K Words of Core Memory	8,400	68
8190	Jumbo with 24K Words of Core Memory	10,400	100
8191	Jumbo with 32K Words of Core Memory	11,900	112
	<b>Nova 1200/1210/1220 Memories</b>		
8120	4K-Word Core Memory	1,800	20
8121	8K-Word Core Memory	2,000	32
8117	16K-Word Core Memory	3,500	44
	<b>Nova 1210 Processors</b>		
8133	With 4K-Word Core Memory	4,000	40
8134	With 8K-Word Core Memory	5,400	59
8140	With 16K-Word Core Memory	7,000	71
8141	With 24K-Word Core Memory	9,000	103
8142	With 32K-Word Core Memory	10,500	115
	<b>Nova 1220 Processors</b>		
8153	With 4K-Word Core Memory	4,900	44
8154	With 8K-Word Core Memory	6,300	56
8165	With 16K-Word Core Memory	7,900	68
8166	With 24K-Word Core Memory	9,900	100
8167	With 32K-Word Core Memory	11,400	112
	<b>Nova 1200/1210/1220/1230 Processor Options</b>		
8106	Power Monitor and Auto-Restart	400	1
8107	Nova 1200/1210/1220 Multiply/Divide	1,600	13
8108	Automatic Program Load	400	2
8122	External I/O Cable Connector	250	NC
8124/5	Expansion Chassis (adds 7 I/O subassembly slots)	1,850	10
8139	Turn-key Console (provides start, continue, reset, and program load functions; for 1200 or 1210 series with 5.25-in. chassis)	100	NC
8159	Turn-key Console (same as 8139 but is for 1210 and 1220 series with 10.5-in. chassis)	125	NC
8181	Expansion Chassis (adds 10 I/O subassembly slots)	1,850	10
	<b>Nova 1200/1210/1220 Memories Semiconductor Read-Only Memory</b>		
8126/77	256 Words	750	8
8127/78	512 Words	1,250	12
8128/79	1,024 Words	1,750	18
8001	Supernova Processor	5,600	54
	<b>Supernova Options</b>		
8006	Power Monitor and Auto-Restart	400	1
8007	Multiply/Divide	1,600	13
8008	Memory Allocation and Protection	3,500	28
8009	High-Speed Data Channel	950	9
8022	External I/O Cable Connector	250	NC
8024	Expansion Chassis (adds 7 additional slots)	1,850	10

Model Number	Description	Purchase \$	Monthly Maint. \$
8025	Supernova SC Memory Expansion Chassis	1,850	10
8003	4K-Word Core Memory	3,650	30
8015	8K-Word Core Memory	4,900	40
8012	1,024-Word Semiconductor Read/Write Memory	2,800	28
8013	512-Word Semiconductor Read/Write Memory	2,200	22
8014	256-Word Semiconductor Read/Write Memory	1,500	15
8015	8,192-Word Core Memory	4,900	40
8077	256-Word Semiconductor ROM	1,000	10
8078	512-Word Semiconductor ROM	1,550	14
8079	1,024-Word Semiconductor	2,050	21
	<b>Option for All Nova/Supernova Processors</b>		
8020	Floating Point Processor	4,000	32
	<b>Dual Nova 840 System</b>		
9028	Part 1 consists of 8291 rack-mounted Nova 840 Computer (with 32,768-word core memory and memory management and protection unit, 8206 power monitor and auto restart, 8208 automatic program load, 4007 I/O interface subassembly, 4008 real-time clock, 4010 Teletype/video display I/O interface, 4119 precision crystal oscillator for 2,400 baud, 4011 paper tape reader control, 6013 high-speed paper tape reader, 4240 interprocessor bus, 4046 moving-head disc control, 4047 moving-head disc adapter and power supply, 4030 magnetic tape control, and 6 remaining slots in computer chassis)	36,550	784
9028A	Part 2 consists of 40101 20-Line, 80-Char Video Display, 1065F Interprocessor Bus Cable, 4047B Moving Head Disc Drive (with 2.494M-words capacity, 4047C disc cartridge, 4030J magnetic tape transport, and 1012G 2-bay rack cabinet)	19,300	784
9029	Part 3 consists of 8291 Rack Mounted Nova 840 Computer (with 32,768-word core memory and memory management and protection unit, 8206 power monitor and auto restart, 8208 automatic program load, 4007 I/O interface subassembly, 4008 real-time clock, 4010 Teletype/video display I/O interface, 4240 interprocessor bus, 4046 moving head disc control, and 7 remaining slots in computer chassis)	28,700	784
9029A	Part 4 consists of 4010A Teletype Model 33 ASR Keyboard/Printer, EC4047 Moving Head Disc Adapter and Power Supply Cable, IC4011 Paper Tape Reader Control Cable, IC4030 Magnetic Tape Control Cable and Major Portion of Supplied Software on Magnetic Tape	2,750	784

**HEADQUARTERS**

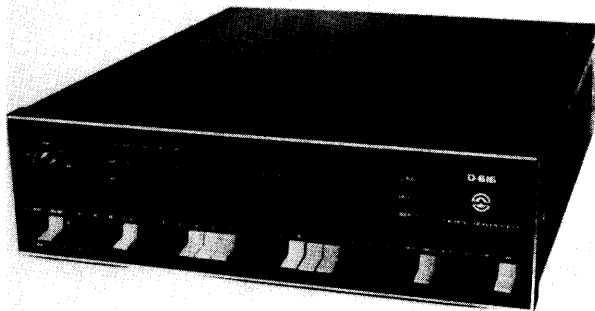
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# DIGITAL COMPUTER CONTROLS INC.

## 16 Series System Report



75-213

### OVERVIEW

The Digital Computer Controls "16 Series" consists of upward-compatible systems that range from microcomputer-sized systems to midcomputers. The earliest models of the series are the LSI/MSI D-116 systems, which started out as Nova replacements. Hardware options combined with new software soon allowed them to compete in a wider marketplace. The recent additions of the microprogrammed LSI D-216, D-316, and D-416 at the bottom of the line and the D-616 midcomputer at the top of the line have expanded competition across the entire range of the minicomputer market.

The success of the company's early approach to the minicomputer market was demonstrated fairly quickly after the firm was formed in 1970. D-112, the first product delivered in August 1970, was compatible with the Digital Equipment PDP-8. By the end of fiscal 1972, Digital Computer Controls (DCC) had delivered more than 400 D-112 systems, started production of the D-116, which was compatible with the Data General Nova 1200, and acquired several subsidiaries. Also, the company was profitable, in spite of the onset of litigation with Data General. To date, the company has delivered more than 750 D-112 systems and 5,000 D-116s. Deliveries of the first models in the new 16 Series began in the last quarter of 1975.

DCC's D-116 Series is program- and interface-compatible with the Data General Nova 1200 Series (Models 1200, 1210, and 1220); options available for the D-116 are similar to those available for the Nova 800 and Supernova systems. Table 1 lists the processor characteristics common to both the D-116 and the Data General Nova/Supernova. Table 2 compares DCC models with specific Data General systems. Both D-116 models use medium- and large-scale integrated circuits to produce a processor on a single circuit board. Core

**Table 1. Processor Characteristics Common to DCC 16 Series and Data General Nova/Supernova**

PROCESSOR	
Power Monitor/Auto Restart	Opt
No. of Instructions	202
Hardware Registers	2
Memory Registers	16
Accumulators	4
Word Size (bits)	16
Decimal Arithmetic	No
Hardware Multiply/Divide	Opt
I/O	
Max Devices Addressable	62
Programmed I/O	Yes
DMA Channel	Yes
Interrupt Levels	16
MEMORY	
Min ROM (wd)	256
Max ROM (wd)	31,744
Parity	No
ROM Increments (wd)	256; 512; 1,024
SOFTWARE	
Assembler(s)	Yes
Mass Storage Operating System or Systems	Yes
Real-Time Executive or Operating System	Yes
Basic Interpreter(s)	Yes

memory units are also compact; the 1,200-nanosecond core memory for the D-116 includes 16K words on a single board. A 16K-word memory board is unavailable for the higher-speed D-116H system — a maximum of 8K words of 960-nanosecond core memory is on a single board.

The three low-end LSI systems, D-216, D-316, and D-416, are slower than the D-116; they are available as a computer-on-a-board with memory (15 x 15 inches) as well as a full-fledged minicomputer system. D-216 is available with 12K words of RAM and 4K words of PROM/ROM. D-316 supports up to 32K words of MOS RAM. D-416 is a core-only system with up to 32K words of memory. The D-316 or D-416 computer-on-a-board offers 32K words of memory along with the CPU, power monitor/auto restart, automatic program load, and a teletypewriter interface. Byte-parity checking is also standard on the D-316 MOS RAM.

As the new high-end system of the 16 Series, the D-616 can support up to 2M bytes of core or MOS RAM

### HEADQUARTERS

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Table 2. DCC D-116 Series Compared with Data General Nova/Supernova

Characteristic	Nova	Nova 800, 820, 800 Jumbo	Nova 830, 840	Nova 1200, 1230	Nova 1210, 1220	Super-nova	Super-nova SC	DCC 116S	DCC 116H
<b>PROCESSOR</b>									
Auto Program Load	—	Opt	Opt	Opt	Opt	Std	Std	Opt	Opt
Total Subassembly Slots	7	7; 10; 17	17	7; 17	4; 10	7	11	4; 7; 10, or 17	4; 7; 10, or 17
Floating-Point Hardware	Opt	Opt	Opt	Opt	Opt	Opt	Opt	No	No
<b>MEMORY</b>									
Capacity (K wd)	32	65	128	65	24; 65	65	65	128	128
Core Increments (wd)	1,2,4	1,2,4	8K	1,2,4	1, 2, 4	2, 4, or 8K	2, 4, or 8K	4, 8, or 16K	4 or 8K
Read/Write SC Memory Increments (wd)	—	—	—	—	—	—	256; 512; 1,024	—	—
Memory Protect	—	Opt	Std	—	—	Opt	Opt	Opt	Opt
Memory Management	—	—	Std	—	—	—	—	Opt	Opt
<b>SPEED</b>									
Core Cycle (μsec)	2.60	0.80	0.80	1.20	1.20	0.80	—	1.20	0.96
SC Cycle (msec)	—	0.80	0.80	1.20	1.20	0.30	0.30	—	—
Interrupt Response Time	40.00	11.00	11.00	17.80	17.80	9.80	9.80	—	—
Transfer Rates (K wd / sec)									
DMA	285	833	833	833.3	833.3	500	500	833.3	833.3
High-Speed Data Channel	—	1,250	1,250	—	—	1,250 (opt)	1,250 (opt)	No	No
Programmed I/O	Std	Std	Std	Std	Std	Std	Std	Std	Std

with a cycle time of 660 nanoseconds. To maintain high throughput, the D-616 memory modules have dual ports and are 2-way interleaved. Memory above 128K words is arranged in up to four external banks. A memory mapping and protection unit similar to that used for the D-116 is required for systems with more than 32K words of memory. Up to 128K words of memory can be housed in the mainframe chassis using a new 32K-word (64-byte) memory board.

The D-616 uses a separate I/O processor, so an I/O transfer rate of 3M bytes per second can theoretically be maintained concurrently with processing, if the I/O channel and the CPU are using separate memory modules. Table 3 compares the system specifications of all five models in the 16 Series.

DCC's peripherals closely parallel Data General's. Data General offers few items that are unavailable from DCC, although the latter's software is not yet comparable. Data General has an extremely large body of software, which is partly responsible for the popularity of the Nova/Supernova series; but DCC is working steadily to narrow the gap. DCC operating systems include MSOS (Mass Storage Operating System), IRIS (Interactive Real-Time Information System), and RTX (Real Time Executive); while language processors include extended FORTRAN IV ("FORTRAN 74"), Business BASIC, and assembly language. A COBOL compiler is scheduled for the end of 1975.

The steady expansion of its software base means that DCC can gain an increasing proportion of revenues from end users instead of marketing only to OEM manufacturers. The software base has grown substantially since the company's inception and now is at the point where

16 Series is a serious contender for the minicomputer dollar on its own merit.

DCC markets its systems directly through eight sales centers in the United States and through a number of sales representatives in the United States, Canada, Mexico, Europe, and other parts of the world. U.S. sales representatives include Datatron, Barnhill, Inland Associates, A & D Devices, Computer Complements, Deerland Distributors, Randal Data Systems, Rush S. Drake Associates, and Aloha Associates (Hawaii). Transword Data Systems markets the system in England and France; Aheam & Soper in Canada; Techmation in the Benelux countries; Teleprint in Germany, Austria, and Switzerland; Datatek in Finland; and Control Proceso Electronics in Israel, Greece, Turkey, and Iran.

In addition to the D-112 and 16 Series, DCC makes a memory expansion unit (add-on memory) that allows Digital Equipment's PDP-8L to be expanded from 4K to 32K words. DCC also produces a POS register and several other minicomputer-controlled devices.

### COMPETITIVE POSITION

Without creating much of a stir, except perhaps in Data General's headquarters in Southboro, Massachusetts, DCC has quietly delivered over 5,000 D-116 computers. Customers include more than 250 OEMs and about 250 end users.

The D-116 has, to judge from the rate of deliveries, become one of the most popular minicomputers on the market. DCC claims it ranks third in number of minicomputer systems shipped per month; only Digital Equipment and Data General ship more. A large number

**Table 3. DCC 16 Series: Mainframe Characteristics**

Characteristics	D-116	D-216	D-316	D-416	D-616
<b>CENTRAL PROCESSOR</b>					
Microprogrammed	No	Yes	Yes	Yes	Yes
Control Memory	No	ROM	ROM	ROM	ROM
No. of Registers	4	12	12	12	12, with 4 used as index registers
Word Length	16 bits	16 bits	16 bits	16 bits	16 bits
<b>Addressing</b>					
Direct	To 64K bytes	To 32K bytes	To 64K bytes	To 64K bytes	To 64K bytes
Indirect	Multilevel	Multilevel	Multilevel	Multilevel	Multilevel to 2M bytes
Indexed Mapping	Yes Yes, to 256 bytes	Yes Yes	Yes Yes	Yes Yes	Yes Yes, to 2 million bytes
<b>Instruction Set Implementation Types</b>					
Number	59	98	98	98	96 with 16 more opt
Floating Point	No	No	No	No	Hardware option
Hardware Stack	No	Yes	Yes	Yes	Yes
<b>Instruction Execution Times (μsec)</b>					
<b>Fixed Point</b>					
Add	0.96 or 1.2	1.6	1.6	1.6	0.66
Multiply	3.0 or 3.8	Times currently unavailable.			5.17
Divide	3.2 or 4.1				16.7
<b>Floating Point</b>					
Add	NA	NA	NA	NA	NA at this time; FPP opt
Multiply	—	—	—	—	—
Divide	—	—	—	—	—
Writable Control Store	NA	NA	NA	NA	Opt; 1K x 50 bits
<b>Interrupts</b>					
Levels	Multilevel	Multilevel	Multilevel	Multilevel	Multilevel
Type	Hardware & software	Hardware & software	Hardware & software	Hardware & software	Hardware & software
<b>MAIN STORAGE</b>					
Type	Core, MOS, RAM, PROM	RAM, PROM, ROM	MOS RAM	Core	Core, MOS RAM, or MOS RAM with error detection & correction
Cycle Time (μsec)	0.96 or 1.20	1.6	1.6	1.6	0.66 for any type
Basic Addressable Unit	Word or byte	Word or byte	Word or byte	Word or byte	Word or byte
Bytes/Access	1 or 2	1 or 2	1 or 2	1 or 2	1 or 2
Cache Memory	No	No	No	No	No
<b>Capacity (bytes)</b>					
Min	128K*	2K	8K	8K	8K
Max	8K, 16K, 32K	24K, 128K*	64K; 128K*	64K; 128K*	2M
Increment Size (bytes)		2K	8K	8K, 16K, 32K, 48K, 64K	8K, 16K, 32K, 64K
Ports/Module	1	1	1	1	2
Error Checks	No	No	Byte parity	No	Error detection & correction
Memory Protection	Yes*	Yes*	Yes*	Yes*	Yes*
Memory Management	Yes	Yes	Yes	Yes	Yes
Interleaving	No	No	No	No	Yes, 2-way
<b>INPUT/OUTPUT</b>					
Max Devices Addressable	60	60	60	60	62
Programmed I/O	Yes	Yes	Yes	Yes	Yes
DMA	Std	Std	Std	Std	Std, with 2 speeds
DMA Transfer Rate (bytes/sec)	833,300	1,250,000	1,250,000	1,250,000	Low-speed = 1.6M (input); high-speed = 3M (input)

\*With Memory Management unit.

of DCC customers buy OEM and do not want to disclose their transactions, so the system has not received the attention from end users that would appear to correspond to its sales record. As of February 28, 1975, DCC's gross sales of \$9,756,140 were up 56 percent and profits doubled over the previous fiscal year. The company now has 8 sales and 12 service offices.

Although DCC no longer emphasized the Series 16's compatibility with Data General's Nova 1200, the press release on the D-616 did compare its cost with the Data General ECLIPSE. The price has been set about 20 percent below the ECLIPSE for comparable configurations. Other 16-bit systems with memory of more than 1 million bytes and enhanced I/O throughput schemes include Digital's PDP-11/70. Some competitive minicomputer systems use a larger word size, such as 24 bits (Harris) or 32 bits (Systems and Interdata), allowing more memory to be addressed directly. Interdata handles compatibility problems with the companies, 16-bit lines through various hardware and software machinations.

DCC compares its smaller 16 Series systems to Computer Automation's LSI configurations. Prices are comparable for small systems, but the 16 Series systems are cheaper when larger memories are included. In the microcomputer marketplace DCC systems also meet board-level computers made by Digital Equipment. Data General's new Nova 3 systems are competing for the same market. At the time of writing, DCC has an advantage in the large amount of memory it can fit on one board, which may be of interest to OEM customers with size restraints. Digital Computer Controls also provides substantial software for its systems. In fact, the company may have COBOL on its systems before some other larger minicomputer manufacturers make it available for their systems. Digital Equipment already has COBOL for the PDP-11/45 and 11/70 and General Automation has it for the GA-16Series.

DCC's new systems are well conceived to be competitive at both the bottom and top of the minicomputer market. They also compete favorably with Data General's comparable offerings. With over 250 OEM customers as well as about that many end users, the company has a considerable base to provide stability.

Our interviews to date indicate the OEM customers are satisfied with DCC as a supplier because the company caters to the market in a flexible way in order to meet customer needs. As the company grows, flexibility will become more difficult. However, any company that can deliver 5,000 computer systems without fanfare must be considered a serious market force.

### User Reactions

**Key/Disc System Manufacturer.** One of the larger D-116 users is the manufacturer of a popular key/disc entry system. This user, who purchases around 600 systems a year, switched from Data General to DCC for a number of reasons. First, this manufacturer started

making its own memories and DCC would sell its processor without a memory; Data General required some memory with its processor. In addition, the long lead time for the popular Data General Nova systems was difficult to accept. Since this key/disc company wrote all its own software from scratch (one of its strong points in the key/disc market), the amount of available software was of no consequence. The key/disc manufacturer is very pleased with the way the arrangement has worked out. The DCC D-116 proved to be compatible mechanically and electrically; no software alterations were needed; service is good; and DCC's accounting department has been responsive to any problems that arose. In addition, this user feels that DCC is attuned to buyers' problems.

**POS System Manufacturer.** Another large user, a manufacturer of point-of-sale equipment, uses a D-116 in each store to control the local terminals directly and at the central supervisory site to communicate with all the controllers in the branch stores. This user switched from Data General to DCC for two reasons: price and the D-116 power supplies, which this user feels are the best it has seen. A careful comparison of the reliability of the Data General and DCC systems in terms of number of man-hours spent to fix defects was made shortly after delivery; both manufacturers were rated good to very good. Data General had the edge over DCC, but the difference in the cost of the few extra man-hours on repair did not equal the amount saved on the DCC systems. This manufacturer found a slight incompatibility in the memory interfacing between its equipment and the DCC memory boards, but adjustment was very minor. The CPU board, I/O board, interfacing, and software were all completely compatible.

**Turnkey Graphics System Manufacturer.** A supplier of turnkey graphics systems is using the D-116 as a controller that replaces the Nova used in earlier systems. This company has used six D-116s so far and has found no problems with the software originally developed for the Nova. Interestingly, this firm had written all its own software from scratch. The company turned to DCC as its supplier when Data General began having trouble meeting delivery commitments due to the unanticipated volume of business in Novas and Supernovas (the demand for the 800 is apparently particularly out of line with projections). DCC promises faster deliveries and has lived up to commitments. Most of the graphics systems use 32K words of core and an assortment of discs and other peripherals to support the displays. This user was quite happy both with the way the system performed and with service — the only complaint was that the racks for the tape drives bent because they were not sturdy enough for the weight they held.

### CONFIGURATION GUIDE

The basic 16 Series processors differ in number of boards required by CPU and memory; some can be purchased at the board level without a chassis. The number of boards per system are as follows:

- D-116S or H — CPU on one board, core memory on additional boards: the 116S uses 1.2-microsecond core and 116 H uses 0.98-microsecond core.
- D-216 — CPU and memory on one board.
- D-316 — CPU and memory on one board.
- D-416 — CPU and memory on one board.
- D-616 — CPU on one board, Writable Control Store and floating-point processor on a second board, memory on additional boards.

The models also use different memory modules. D-116S or H supports 4K to 128K words of core memory available in 4K-, 8K-, and 16K-word increments. D-216 includes 1K to 16K words of memory consisting of 1K to 12K words of MOS RAM available in 1K-word increments and up to 4K words of PROM or ROM available in 512-word increments. D-316 includes 4K to 32K words of core memory in 4K-word increments with byte parity. D-416 includes 4K to 32K words of core memory in 4K-, 8K-, 16K-, 24K-, and 32K-word increments. D-616 supports 4K to 1M words of core or MOS memory; MOS can include error correction and detection facilities. Memory management is required for D-116 systems with more than 32K words of memory. The D-616 houses memory above 128K words in separate cabinets.

All systems can be housed in standard chassis 19 x 23 inches, 5.25 or 10.5 inches deep, with 4, 7, 10, or 17 (16 for the D-616) slots for options, memory, and peripherals. The D-216, D-316, and D-416 can also be ordered as stand-alone boards.

Systems are available as rack or tabletop models and with or without a programmer's console or a turnkey console. Power supply can be either 115 or 220 volts AC.

D-116 processors differ somewhat from the other models in basic specifications. The newer models have more registers, an added vectored interrupt system, more instructions, and microcoded I/O routines. The D-616 has multiported memory and a separate I/O subsystem to enhance system throughput for multiple users. Table 3 compares specifications for the five 16 Series models. All systems have both programmed I/O and DMA channels as standard features.

Up to 60 I/O devices can be connected to a D-116, D-216, D-316, and D-416 computer, while up to 62 can be connected to a D-616. If the Memory Management option is connected to the D-116, it takes up three I/O slots. All peripheral devices connect to the programmed I/O channel for transfer of control information. Slow-speed devices, such as console typewriters, punched card, paper tape, and line printers also use the programmed I/O channel for data transfers. High-speed devices, such as magnetic tape and disc, transfer data via the DMA channel. Table 4 lists individual peripheral devices supplied by DCC.

Especially important interfaces (aside from those for communications) include a multiprocessor adapter for

**Table 4. DCC 16 Series: Peripherals**

Model No.	Description
<b>Terminals</b>	
116410 Series	Teletype Models 33, 35, & 38 ASR & KSR
116424 A/B	A/N displays (4,000/1,600 char; 25 or 12 lines by 80 chars to 9,600 baud)
116480/82/84	A/N displays (1,600 char; 12 lines by 80 char; to 9,600 baud or 15,000 char/sec; models with various interfaces)
116481/83/85	A/N displays (like 116480/82/84 models but 3,200 char; 24 lines by 80 char)
116486/87/89	A/N displays (4,000 char; 25 lines by 80 char, various speeds and interfaces; some both upper- and lowercase)
<b>Paper Tape</b>	
116411B	300-cps reader
116412B	75-cps punch
116412D	Combination 300-cps reader, 75-cps punch
<b>Punch Cards</b>	
116416 Series	150-, 300-, or 600-cpm readers
116416E	300-cpm mark-sense reader
116435A	150-cpm punch
<b>Printers</b>	
116434 Series	60-, 125-, 300-, 600-lpm printers
116460	30-cps printer
<b>Plotters</b>	
116417A/B	Drum plotter (300 steps/sec; 0.01/0.005-in. or 0.1-mm steps)
116417C	Drum plotter (300 steps/sec with 0.01-in. or 0.1-mm steps; 200 steps/sec with 0.01-in. steps)
116417D	Flatbed plotter (300 steps/sec; 0.01/0.005/0.002-in. or 0.05/0.1-mm steps)
116417E	Incremental plotter (300 steps/sec; 0.01/005-in. or 0.25/0.1-mm steps)
<b>Discs</b>	
116418	Flexible disc (128K wd/cartridge; up to 3 drives/controller)
116447	Removable 2315-type cartridge disc (1.2M wd/cartridge; up to 4 drives/controller)
116447B/D	1 fixed, 1 removable (2315-type) cartridge disc (2.4/5M wd/cartridge; 2/4 drives/controller)
116452	Disc pack drives (40M or 80M bytes; up to 8 drives/controller; CDC discs; dual computer access option; 30-msec access; 600K-wd/sec transfer rate)
<b>Magnetic Tape</b>	
16430 Series	NRZI tape drives (7- or 9-trk; 12.5, 24, 45, or 75 ips)
116430 Series	PE tape drives (9-trk; 1,600 bpi; 45 or 75 ips)
116461	Cassette drive (up to 125K wd/cassette)
<b>Process I/O</b>	
116455 Series	A/D & D/A subsystem (up to 64 single-ended (32 differential) inputs with 8/10/12/13/14/15 bits; or up to 16 single-ended together with 2 D/A, or 8 D/A)
116456 Series	D/A conversion subsystem (up to 24 D/A converters with 8/10/12/13/14 bits)
116466	Digital I/O (16 input, 16 output lines)

**Table 4. (Contd.)**

Model No.	Description
<b>Communications &amp; Local Interfaces</b>	
116462/116415 116425	Single-line interfaces (async/sync) IBM 360/370 programmable interface
116426 116427	16-line async multiplexor 4-line voltage interface (EIA RS2326)
116428	4-line current interface (for local teletypewriter)
116431 Series	8-line async line units (for either voltage or current loop interfaces)
116438	Multiprocessor communications adapter (for up to 15 16 series computers)
116450	Teletypewriter junction panel (for up to 16 teletypewriters or displays)
116451	Modem junction panel (for up to 16 lines)
116472	Auto calling unit (up to 4 dialer interfaces)
116475	4-line sync unit (up to 250K baud)

up to 15 processors and an IBM System/360 or 370 interface that allows the DCC computer to be adapted to front-end processing.

Software packages vary in the minimum configurations they require. Table 5 lists the important packages with their configuration requirements.

**COMPATIBILITY**

The DCC D-116 family is fully compatible with the Data General Nova 1200, 1210, and 1220 minicomputers; it is not completely compatible with the Nova 800 or the Supernova. Software requirements for the D-116s are identical with those for the 1200 series, and interchangeability is maintained even through the subassembly level. Peripheral interfaces are also compatible.

D-216, D316, D-416, and D-616 are all upward compatible with the D-116 systems. Even the smallest of those models have instructions that are unavailable to the D-116. They are also upward compatible with each other; that is, the D-216, D-316, and D-416 are directly compatible, while the D-616 is upward compatible with the less powerful systems.

All 16 Series systems use the same peripherals.

**MAINTENANCE**

DCC provides three basic types of service contracts for purchased systems (DCC systems are not leased): on-call maintenance, an extension of the factory warranty, or the services of a dedicated on-site service engineer. The on-call contract provides regular preventive mainte-

nance plus on-site emergency repairs for a fixed monthly charge. The warranty extension contract provides repairs at an authorized service center for a fixed monthly charge that is approximately half that of the on-call contract. The third contract provides the full-time prime-shift services of a trained customer engineer. DCC also offers noncontract service on-site or at a factory service center.

**Table 5. DCC 16 Series: Basic System Software**

Package	Description
Interactive Real-time Information System (IRIS)	Modular data base management and time sharing system; requires 16K wd of memory, disc, paper tape I/O, real-time clock, teletypewriter or keyboard/display
Mass Storage Operating System (MSOS)	Combines real-time executive with file manager; requires 12K wd of core, 1 mass storage device (cartridge or floppy disc, magnetic tape), ASR 33; supports FORTRAN IV, single-user BASIC
Real-Time Executive (RTX)	Multitask monitor, priority-oriented task scheduling; requires 4K wd of memory (resides in less than 2K), real-time clock, teletypewriter or keyboard/display
FORTRAN IV	Extension of ANSI FORTRAN X 3.9-1966 specifications; includes real-time extensions of ISA S61.1/1972 Industrial Computer System FORTRAN Procedures; FORTRAN 74; core-resident version requires 8K wd of memory; MSOS version (disc resident) 8K wd also
Business BASIC	Upward compatible with Dartmouth BASIC; requires 8K wd of memory, TTY control, 1 teletypewriter for single user; allows up to 5 users concurrently; requires 8K wd of memory, TTY control, and 1 teletypewriter for multiusers
Relocatable Assembler	2-pass assembler with third opt verification pass; requires 8K wd of memory, TTY
Editor	Allows user to create, modify, list, and punch source files; requires 8K wd of memory
Octal Debug	Relocatable: requires 4K wd of memory, TTY
Extended Debug	Incorporates symbolic I/O, extensive tracing; requires 4K wd of memory, TTY
D-116 Loader	Loads assembler or debug object tapes
1200 Series Absolute Loader	Used to load absolute object tapes generated by 1200 Assembler; requires TTY or paper tape reader





## TYPICAL PRICES

Model Number	Description	Purchase Price \$
D-116/4	Central Processor (with 4 slots & core memory)	
	4K Words	2,975
	16K Words	4,580
D-116/7	Central Processor (with 7 slots & core memory)	
	4K Words	3,640
	16K Words	5,255
D-116/10	Central Processor (with 10 slots & core memory)	
	8K Words	4,125
	32K Words	8,020
D-116/17	Central Processor (with 17 slots & core memory)	
	8K Words	16,470
	32K Words	
D-216/0	Central Processor Board with RAM (incl. power monitor/auto restart, auto program load, multiply/divide, TTY interface)	
	1K Words	1,800
	8K Words	2,700
D-216/4	Central Processor (with 4 slots & RAM)	
	12K Words	3,300
	1K Words	2,700
D-216/7	Central Processor (with 7 slots & RAM)	
	8K Words	3,600
	12K Words	4,200
D-216/10	Central Processor (with 10 slots & RAM)	
	1K Words	3,000
	8K Words	3,900
D-216/17	Central Processor (with 17 slots & RAM)	
	12K Words	4,500
	1K Words	3,300
D-316/0	Central Processor with Board & RAM (incl. power monitor/auto restart; auto program load, multiply/divide, TTY interface)	
	4K Words	4,200
	20K Words	4,800
D-316/4	Central Processor (with 4 slots & RAM)	
	4K Words	2,000
	20K Words	4,400
D-316/7	Central Processor (with 7 slots & RAM)	
	32K Words	6,200
	4K Words	2,900
D-316/10	Central Processor (with 10 slots & RAM)	
	4K Words	5,300
	20K Words	7,100
D-316/17	Central Processor (with 17 slots & RAM)	
	4K Words	3,200
	20K Words	5,600
D-416/0	Central Processor with Board & Core Memory (incl. power monitor/auto restart, auto program load, multiply divide)	
	4K Words	2,400
	32K Words	6,000
D-416/4	Central Processor (with 4 slots & core memory)	
	4K Words	3,400
	32K Words	6,900
D-416/7	Central Processor (with 7 slots & core memory)	
	4K Words	3,700
	32K Words	7,200
D-416/10	Central Processor (with 10 slots & core memory)	
	4K Words	4,000
	32K Words	7,500

# DIGITAL COMPUTER CONTROLS INC. — 16 SERIES SYSTEM REPORT

## TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price \$
D-416/17	Central Processor (with 17 slots & core memory) 4K Words	4,700
D-616/4	Central Processor (with 4 slots & RAM or core memory; incl. power monitor/auto restart, auto program load; 616880 memory expansion & protection unit in 48K-word or larger configurations) 32K Words	8,200
D-616/6	Central Processor (with 6 slots & RAM or core memory) 4K Words	5,660
D-616/10	Central Processor (with 10 slots & RAM or core memory) 32K Words	12,540
D-616/16	Central Processor (with 16 slots & RAM or core memory) 4K Words	5,960
D-616/4	Central Processor (with 4 slots & RAM with error detection & correction; incl. power monitor/auto restart, auto program load; memory expansion & protection unit in 48K-word or larger configurations; memory capacity beyond 128K words available) 32K Words	12,840
D-616/7	Central Processor (with 6 slots & RAM) 4K Words	7,080
D-616/10	Central Processor (with 10 slots & RAM) 32K Words	13,960
D-616/16	Central Processor (with 16 slots & RAM) 128K Words	41,480
116806	Processor Options Power Monitor & Auto Restart	7,880
116807	Hardware Multiply/Divide	14,760
116808	Automatic Program Load	42,280
116810/216810/316810/416810	High Current Power Supply	7,260
116880	4-User MEU	16,540
216811/316811	Battery Backup	7,560
216812/316812/416812	Backplane Assembly	16,840
216818/316818/416818	Voltage Interface	8,680
616807	Multiply Divide (signed/unsigned)	17,960
616811	Battery Backup	9,480
616880	4-User MEU	55,880
616813	User Microprogram PROM	325
616815	Floating Point Processor	1,430
616816	Writable Control Store	325
616817	Decimal Arithmetic Processor	150
116883	Memory Options 4K-Word Core Memory (960 nsec)	3,500
116885	16K-Word Core Memory (960 nsec)	400/750
116803	4K-Word Core Memory (1.2 μsec)	175
116875	16K-Word Core Memory (1.2 μsec)	150
116876	PROM Memory	500
116877	RAM Memory	200/750
216881	512-Word PROM	2,000
616857/616847	256K-Words Core; 256 Words RAM	500
616838	512K Words RAM with EC	3,000
616853	16K Words Core	4,200
616842	8K Words RAM	3,000
616835	32K Words RAM with EC	1,800
116418	Mass Storage Flexible Disc Control Interface	3,180
116418A	Flexible Disc Control	1,800
116466	Cartridge Disc Control	3,180
116447A	Cartridge Disc Drive (1.2M words)	2,260
		11,840
		1,000
		1,350
		3,500
		5,900

**TYPICAL PRICES (Contd.)**

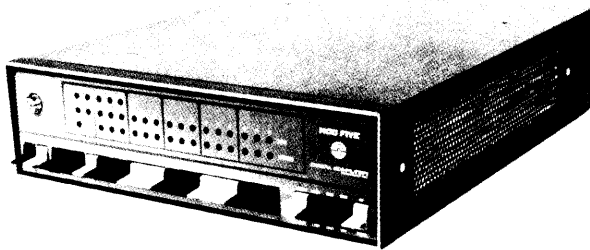
Model Number	Description	Purchase Price \$
116447B	Cartridge Disc Drive (2.4M words)	6,450
116447D	Cartridge Disc Drive (5M words)	6,950
116452	40/80-Megabyte Disc Control	6,700
116452-1	Dual Access	1,000
116452A	40-Megabyte Disc Drive	12,500
116452B	80-Megabyte Disc Drive	22,800
116452C	40-Megabyte Disc Pack	800
116452D	80-Megabyte Disc Pack	975
	<b>Input/Output</b>	
116411	Paper Tape Reader Control Interface	675
116411B	Paper Tape Reader	1,450
116412	Paper Tape Punch Control Interface	560
116412B	Paper Tape Punch	2,000
116412D	Combination Reader/Punch	3,175
116430	NRZI Magnetic Tape Control	3,500
116430-1	Phase-Encoded Magnetic Tape Control	4,200
116430C/D	Magnetic Tape Transport (9-trk, 45 ips)	5,500
116430E/F	Magnetic Tape Transport (7/9-trk, 12.5 ips)	4,000
116430I	Magnetic Tape Transport (9-trk, 75 ips)	8,500
116461	Cassette Loader II	1,850
116414	I/O Interface Board	200
116416	Card Reader Interface	700
116416A	Card Reader (300 cpm)	2,950
116416C	Card Reader (600 cpm)	4,100
116416D	Card Reader (150 cpm)	2,000
116416E	Mark-Sense Card Reader (300 cpm)	4,295
116434	Card Punch Control	850
116435A	Card Punch (100 cpm)	14,250
116424A	Video Display (25 lines, 80 char/line)	3,000
116480	Video Display (12 lines, 80 char/line)	1,405
116434A	Printer (60 lpm)	2,950
116434B	Printer (125 lpm)	6,000
116434D	Printer (300 lpm)	8,500
116460A	Character Printer (30 cps)	2,725
116434E	Printer (600 lpm)	13,900
116410B	Teletype Model 33 KSR	1,300
116410D	Teletype Model 35 ASR	4,475
116410F	Teletype Model 38 ASR	2,500
116417	Plotter Control Interface	1,250
116417A	Drum Plotter	6,850
116417D	Flatbed Plotter	25,500
116417E	Incremental Plotter	5,000
	<b>Clocks</b>	
116408	Real-Time Clocks	325
116468	Programmable Interval Timer	600

A service agreement provides on-site maintenance service, parts, and preventive maintenance. Basic monthly maintenance charge 9:00 a.m. to 5:00 p.m. Monday to Friday is 1% of the list price of the equipment as stated in the price list in effect; 8-hour service Saturday is charged at 25% additional; 35% additional for 16-hour service 7 days a week, and 75% additional for 24-hour service Monday to Friday, 80% for Saturday, and 85% for Sunday. Additional charges are made for equipment located over 100 miles from a service center.



## DIGITAL COMPUTER CONTROLS

### DCC-16 Series System Report Update



76-58

#### OVERVIEW

When Digital Computer Controls (DCC) announced the new computers in its "16 Series," D-216, D-316, D-416, and D-616, a 516 model was conspicuously absent. The older D-116/S and H models fit in price and performance into the void in the new 16 Series. Apparently, the D-116 models were selling briskly, and DCC felt no pressure to announce replacements for them.

On November 7, however, a Delaware Chancery Court order permanently enjoined Digital Computer Controls, Inc. from using the logic design of Data General's NOVA® 1200 for any purpose other than maintenance and from using NOVA 1200 and DCC's D-116 logic drawings for manufacturing minicomputers substantially identical to the NOVA 1200. The injunction was suspended to give DCC a chance to appeal but the company was ordered to post a bond of \$500,000. DCC posted the bond on November 10 and announced its intention to appeal the court decision. Data General originally brought the trade secrets suit against DCC in 1971. If the decision for Data General is upheld, a jury trial will determine the damages DCC must pay Data General.

In the meantime, DCC announced the MOD 5, the D-116 replacement in the new 16 Series line. The MOD 5 is available in two core memory versions and one MOS memory version. The MOD

5/S uses core memory with 1.2-microsecond cycle time; the MOD/H uses core memory with 1.0-microsecond cycle time; and the third MOD 5 model uses MOS memory with 0.8-microsecond cycle time. Table 1 compares the mainframe characteristics of the MOD 5 to the D-116H and the Data General NOVA 3. The prices for the MOD 5/S are identical to the D-116 prices. The MOD 5/H CPU costs \$100 more than the MOD 5/S CPU. The MOD 5 is upward compatible with the D-116 and totally compatible with the rest of the new 16 Series line. The MOD 5 has the extended instruction set of the new 16 Series. Delivery of the MOD 5 is 60 days ARO (After Receiving Order).

#### COMPETITIVE POSITION

Although the MOD 5 was hurriedly introduced, it was obviously planned as part of the 16 Series line. It offers more performance than the D-116 but at the same price. In today's market, the MOD 5 will compete with the Data General NOVA 3 rather than the older NOVA 1200, the system involved in the Data General suit. The MOD 5 core versions are more expensive than the NOVA 3 for systems configured with 32K or 64K bytes of memory. The MOD 5 costs less than the NOVA 3 for systems with 256K bytes. Prices for the MOD 5 MOS memories have not been announced. Table 1 compares MOD 5 with NOVA 3 and the D-116H.

The MOD 5 implements both signed and unsigned multiply and divide in firmware. NOVA 3 implements only unsigned multiply and divide. NOVA 3 can use the same floating-point processor as the rest of the NOVA line. Initially, MOD 5 does not offer a floating-point processor.

#### HEADQUARTERS

Digital Computer Controls, Inc.  
12 Industrial Road  
Fairfield NJ 07006  
(201) 575-9100

Table 1. Digital Computer Controls MOD 5 Compared to 116 and NOVA 3 Computers

	MOD 5/S	MOD 5 (RAM)	MOD 5/H	D-116H	NOVA 3
<b>CPU</b>					
Technology	MSI, T <sup>2</sup> L	MSI, T <sup>2</sup> L	MSI, T <sup>2</sup> L		MSI bipolar
Number of Instructions	76	76	76	39	39 + 31*
Number of Registers	8	8	8	4	4
Number of Interrupt Levels	62	62	62	16	16
Instruction Execution Times, $\mu$ sec					
Add/Subtract	1.2	1.6	1.0	1.0	0.7
Unsigned Multiply	3.8	NA	3.0	3.0	5.8
Unsigned Divide	4.1	NA	3.2	3.2	6.7
Signed Multiply	10.0	NA	8.4	—	—
Signed Divide	28.4	NA	23.1	—	—
Floating-Point Arithmetic					
Add/Subtract	—	—	—	—	7.7
Multiply	—	—	—	—	11.3
Divide	—	—	—	—	13.7
Stack Facilities	Yes	Yes	Yes	No	Yes
<b>Memory</b>					
Technology	Core	MOS	Core	Core	MOS
Word Length	16	16	16	16	16
Cycle Time, $\mu$ sec	1.2	0.800	1.0	0.960	1.0
Parity	No	1 bit/byte	No	No	Opt
Memory Protect	Opt	Opt	Opt	Opt	Opt
Memory Management Unit	Opt	Opt	Opt	Opt	Opt
Capacity, words					
Min	4K	4K	4K	4K	4K
Max	128K	128K	128K	128K	128K
<b>Input/Output</b>					
Number of Devices	62	62	62	62	61
DMA Max					
Xfer Rate, words/sec					
Input	833,333	1,250,000	1,040,000	1,040,000	1,000,000
Output	625,000	1,000,000	750,188	695,000	—
<b>Price, CPU + Memory, \$</b>					
32K bytes	4,580	NA	4,680	4,580	4,400
64K bytes	7,285	NA	7,385	7,285	7,100
256K bytes	29,270	NA	29,370	29,270	34,200

The MOD 5 implements three stacks, while NOVA 3 implements one stack. MOD 5 is available in four chassis sizes: four-slot, seven-slot, 10-slot, and 17-slot. NOVA 3 is available in a four-slot chassis or a 12-slot chassis. Expansion chassis are available for additional peripheral controllers or for additional memory for NOVA 3.

Although DCC initially marketed its systems as software and peripherals compatible with the NOVA 1200, this has been soft-pedaled in recent years. DCC has developed its own software for the D-116. But, DCC has delivered 6,000 D-116 systems, so the Delaware court decision is extremely important to both DCC and Data General. If the decision is upheld, a jury could award

Data General substantial damages. The decision could also have consequences throughout the computer industry. A number of other "look-alike" systems are around, notably the Amdahl 470V/6 and at least two well-advertised replacements for the IBM 1130 — General Automation 18/30 and Digital Scientific Meta 4.

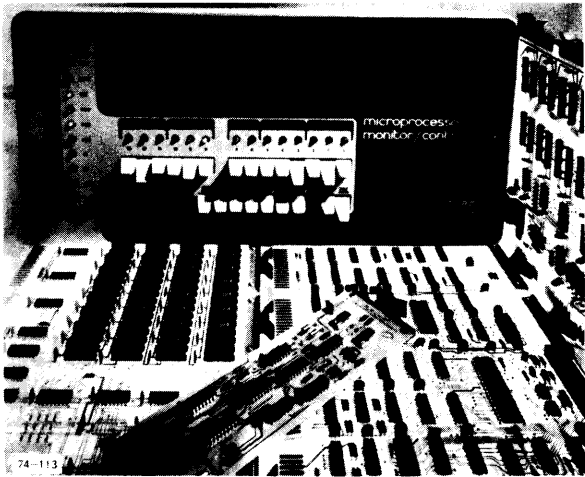
Although the Data General-Digital Computer Controls case is based on special circumstances, the court decision did rule on a broad issue when it enjoined DCC from using NOVA 1200 logic diagrams for anything other than maintenance. Whatever the outcome may be, DCC certainly will discontinue production of the D-116 as quickly as possible and begin delivering the MOD 5.

**TYPICAL PRICES**

Equipment	Purchase Price, \$			
Mod 5 CPU, System with Memory, words	Mod 5/4	Mod 5/7	Mod 5/10	Mod 5/17
4K	2,945	3,640	3,700	5,410
8K	3,365	4,055	4,125	6,130
16K	4,580	5,255	5,320	7,330
24K	6,220	6,890	6,955	8,960
32K	7,285	7,950	8,020	10,020
48K	—	—	13,770	15,770
64K	—	—	16,470	18,470
128K	—	—	—	29,270
Processor Options		Purchase Price, \$		
Mod 5 CPU, H option	100 for each CPU			
Firmware signed and unsigned multiply and divide	700			
Power Monitor and Auto-Restart	325			
Hardware Unsigned Multiply and Divide	1,200			
Automatic Program Load	325			
MEU (Memory Expansion and Protection Unit) Backplane	50			
High Current Power Supply (increases current capacity)	150			
For 10-slot chassis	490			
4-User MEU Unit	3,500			
Equipment		Purchase Price, \$		
Memory, words				
1/1, 2- $\mu$ sec Cycle Time				
4K				
8K	1,800			
16K	2,000			
Expansion Chassis	3,180			
6-Slot	1,350			
15-Slot	1,650			







### OVERVIEW

On March 15, 1974, Digital Equipment Corporation (DEC) announced an 8-bit LSI Microprocessor Series (MPS) and a 12-bit MSI version of the PDP-8 called PDP-8/A. Both systems are aimed at the low end of the computer market, an area DEC has addressed with its do-it-yourself PDP-16 and OEM versions of its popular PDP-8 and PDP-11 minicomputers. The PDP-16 is too loosely organized for this market, while the PDP-8 and PDP-11 are too system-oriented and too expensive.

Computer Automation has prospered in this market area for several years, and General Automation recently announced the LSI 12/16 for the same market. Also, a number of the large semiconductor houses sell microprocessors for control applications that require little conventional I/O facilities and little program variety. DEC has priced the MPS to put pressure on the current competition in this market. The single-unit quantity price of \$745 for a basic MPS configuration of a CPU and 1K bytes of RAM reduces to \$445 for 1,000-unit quantities.

The MPS uses 8-bit logic and LSI circuitry for its five modules.

- CPU module—can address up to 16K memory bytes.

- Semiconductor read/write memory module—expandable from 1K to 4K bytes.
- Programmable read-only memory module—256 to 4K bytes.
- External event detection module—for low voltage monitor or priority interrupt system.
- Monitor/control panel—for diagnostic checkout and program entry.

The CPU uses an 8-bit parallel arithmetic unit, seven 8-bit data registers, and an 8-bit data and memory bus. Eight 14-bit address registers are used to implement a program counter and subroutine nesting.

The control logic is implemented with a dynamic RAM. A single Universal Asynchronous Receiver/Transmitter (UART) provides a full-duplex serial line interface.

DEC supplies software to allow users to prepare MPS programs on a PDP-8 with 4K words of memory. The systems software includes the following packages for the PDP-8:

- Editor—for editing source tapes from the Teletype console.
- Assembler—translates source programs into binary tape output.
- ROM program—programs PROMS from assembler's binary tape output.
- Debugging program—aids debugging binary programs.
- Master tape duplicator—copies paper tapes.
- Host loader—loads binary-coded tapes into PDP-8 memory.

The modules will be manufactured in DEC's Massachusetts facilities. First delivery of the MPS is scheduled for June 1974. Delivery will be 30 to 60 days from receipt of order.



## DIGITAL EQUIPMENT CORP.

### Super-8

#### OVERVIEW

If the automobile business were not in the doldrums, one could imagine going into a showroom on a Saturday afternoon and driving out in a "Super-8." The Super-8, however, is Digital's latest implementation of the PDP-8/A. A parallel processor that performs all fixed- and floating-point arithmetic operations in hardware makes the Super-8 super. The PDP-8/A processor performs system management and input/output operations. The Super-8 adds 64 instructions to control the arithmetic processor, which has direct access to memory and can address 32K words.

The arithmetic processor uses three data formats for operands and results: 24 bits for fixed-point arithmetic and a 24-bit or 60-bit fraction with a 12-bit exponent for floating-point arithmetic. The Super-8 can run ANSI-compatible FORTRAN IV programs under the OS-8 operating system.

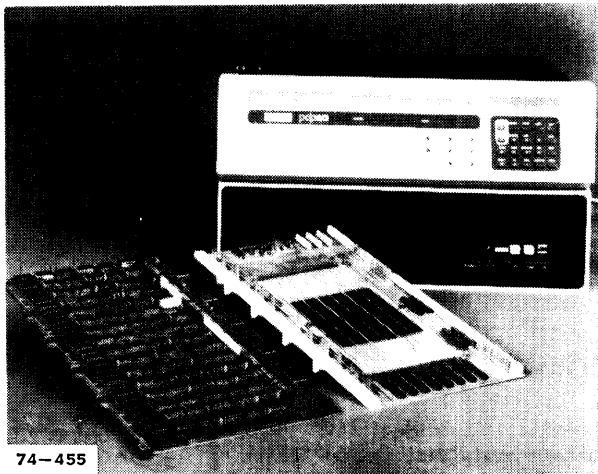
The Super-8 performs calculations much faster than any previous PDP-8 model. Typical instruction execution times are as follows:

Instruction	Execution Time, $\mu$ sec.
Fixed-point (24-bit operands)	
Add	10.5
Floating pt. (24-bit fraction)	
Add	30.0
Multiply	37.5

The PDP-8/A computers already in the field can be upgraded to a Super-8. Two circuit boards must be added to a PDP-8/A-400 to convert it to a Super-8. Other systems must first be upgraded to PDP-8/A-400.

Cost of the Super-8 with 8K words of core memory is \$5995. First deliveries are scheduled for April 1976.





## OVERVIEW

The PDP-8 family of computers were the first computers on the market that combined the small size, processing power, and low cost now associated with the whole class of systems termed "minicomputers." Since Digital's original introduction of the PDP-8, the company has continued to develop this 12-bit line, adding new memories, new processors, new peripherals, and a programmable general-purpose register and changing from the positive external bus on earlier models to an internal OMNIBUS®. The OMNIBUS saves space and eliminates back-panel wiring by allowing all system modules (including memory and the CPU) to communicate over the same bus, with the result that any module can be located anywhere along the bus. Because the PDP-8 continues to be popular, a large body of all types of efficient software is being accumulated, resulting in even more user interest. As a result of this developmental cycle, there are more installed PDP-8s than all other minicomputers put together.

The current PDP-8 models, the 8/A, 8/E, 8/F, and 8/M, can all expand the basic memory to 32K words. The 8/E is the top of the line, with all options and peripherals available for expansion of the basic system. The 8/F is a physically smaller 8/E with lower initial power requirements and somewhat less internal expansion capability. The 8/M is basically an 8/F geared to the OEM market. The 8/A is a new MOS system with a compact 1-board CPU for even greater savings to OEM users.

The 8/E-8/F-8/M models use core modules with a 1.2/1.4-microsecond cycle, while the 8/A uses MOS modules with a 2.3/2.8-microsecond cycle. All can attach ROM and PROM modules; all can attach the same peripherals, use the same software, and perform the same functions.

\* Registered trademark

Peripherals of every variety are provided for the PDP-8: conventional I/O units for cards and paper tape, including a mark-sense card reader; DEC tape or cassette tape as mass storage for small systems, and industry-standard tape for larger storage requirements; fixed- and movable-head disc subsystems for larger systems; terminals, CRTs, and plotters; special-purpose subsystems to handle A/D, D/A, and digital I/O for data acquisition and control applications; and a fairly broad range of communication interfaces for data communication environments.

More than 700 programs are DEC-supported for the 8/A, 8/E, 8/F, and 8/M. Many of these programs were developed by DEC and many by users who also contribute programs to the DECUS (Digital Equipment Corporation Users' Society) software library. Available software includes general operating systems (CAPS — 8-cassette Operating System, RTS-8 Real-Time Operating System, OS-8), a variety of special-purpose operating systems (LAB-8/E, PHA-8, INDAC 8, EDUSYSTEMS, TS8/E time-sharing, COS 300 commercial, and others). Language facilities include BASIC, FORTRAN, ALGOL, FOCAL (a compact interactive language similar to BASIC), DIBOL (a commercial language similar to COBOL) and assemblers. Special application software is available for communication, typesetting, industrial data acquisition, numerical machine control, education, graphic displays, and a variety for scientific laboratory instrument control. The comprehensive OS/8 operating system is an excellent system for combining interactive processing and batch processing; resident core requirements can be as little as 256 words of memory.

## History

In 1965, Digital Equipment Corporation (Digital) delivered the first member of its largest family of computers, which has grown to include Models PDP-8, 8/S, 8/L, 8/I, 8/E, 8/F, 8/M, and 8/A. Related members include the LINC-8 and PDP-12. Only the PDP-8/E, 8/F, 8/A, and 8/M and the PDP-12 are in production. All other family members are "traditional" products, that is, products Digital services and maintains but no longer produces. Generally, Digital retrofits new software and peripheral devices to the traditional products in the line. Returned machines are refurbished and sold at prices competitive with those for newer products.

The first PDP-8 went against the trend toward big, complex, expensive computer systems with massive software. It had a short word length (12 bits), modular memory of 4K to 32K words, a 1.5-microsecond cycle time, simple instruction set, flexible I/O structure, and an \$18,000 price tag. The system lent itself to many scientific and control applications that did not require the power of the computers supplied by the large manufacturers. PDP-8 sold briskly; over 25,000 computers from the family have been installed to date. Its popularity proved there was a large market for this type of computers, now called minicomputers. In 1966, the PDP-8 was followed by the

PDP-8/S, a slower, smaller, cheaper version of the PDP-8 with a curtailed I/O capability. The 8/S was a highly successful system extending the market to users who did not need the PDP-8's speed. It cost about \$9,000 less than the PDP-8.

The PDP-8/S was followed by the PDP-8/I and PDP-8/L in 1968. The PDP-8/I was a redesigned PDP-8 using TTL integrated circuit modules to duplicate the functional capabilities of the PDP-8. PDP-8/I was physically smaller and about \$5,000 lower in price than the PDP-8. PDP-8/L was designed primarily for the OEM market. System expansion capability was removed from the PDP-8/L processor chassis, and expansion modules had to be added to the PDP-8/L system before additional core memory and I/O devices could be connected. Originally the PDP-8/L core memory capacity was limited to 8K words, subsequently raised to 12K words, and eventually increased to 32K words, the same as for the other PDP-8 processors. The basic PDP-8/L sold for about \$5,000 less than the PDP-8/I.

PDP-8/E, first delivered in 1970, is a slightly faster, more compact, more modular, less expensive version of the PDP-8/I, but with more system configuration flexibility in the lower range where the processor can operate as a sophisticated controller. In addition, the PDP-8/E has features not available on previous PDP-8 models: ROM (read-only-memory) in 256-word modules, an OMNIBUS, additional instructions, and an improved EAE (Extended Arithmetic Element) option. A minimum configuration PDP-8/E can include a processor, a 4,096-word core memory, a minimum control console, and a power supply. The PDP-8/F and 8/M, first delivered in 1970, are smaller, less expensive versions of the 8/E. The 8/F is marketed as an end-user system, while the 8/M is directed toward the OEM market.

Because the 8/E is flexible in the lower ranges, price differences for basic systems of the three core-based models do not show the wide differences found among earlier models. The lowest-priced, minimum configuration 8/E costs little more than minimum configurations for 8/F and 8/M. Prices for the 8/E and 8/F include a programmer's console, while the 8/M price includes only an operator's console. Prices for PDP-8/Ms with PROM memory and operator's console, however, are considerably less. The PROM includes 256 words of read/write memory for each 1K words.

The new PDP-8/A, first delivered in December 1974, departs from the 8/E, 8/F, and 8/M in a number of ways, while essentially retaining both hardware and software compatibility. The PDP-8/A has a CPU with MSI circuitry engineered to fit on a single board, and it uses 1K-, 2K-, or 4K-word MOS memory modules. Both the CPU and memory have slower cycles than the 1.2-microsecond 8/E, 8/F, and 8/M: 1.5 microseconds for the PDP-8/A CPU, 2.0 or 2.3/2.8 microseconds for MOS RAM, 1.5 microseconds for core and ROM, and 3.4 microseconds for PROM. Moreover, the PDP-8/A does not yet have an

option corresponding to the Extended Arithmetic Element (EAE), but it is currently under development. These differences may present compatibility problems with some time-dependent or EAE programs and interfaces but, generally speaking, all of the PDP-8 software is available to the 8/A, including the OS-8, RTE-8, and CAPS-8 operating systems. The PDP-8/A minimum prices are well under \$1,000 for board only systems; for a CPU and 1K word RAM, unit prices are \$895 for a single system and \$537 for 100 or more; "boxed" systems with chassis, power, battery back-up for MOS modules and 1K-4K words of memory are in the \$1,745 to \$1,995 range.

## COMPETITIVE POSITION

Despite the proliferation of different minicomputers on the market, the PDP-8 family remains a significant system in Digital's product line and in the entire minicomputer field. It is a dynamic system because Digital keeps the price competitive with new models that reflect current technology, such as the recent addition of the PDP-8/A with its 1-board CPU and MOS memory. Digital also continues to add extensive system and applications software, and interfaces to it almost all of the broad range of mass storage and peripheral devices the company produces. Probably the PDP-8's strongest points in the current market are its enormous body of available software and its wide variety of peripherals. Although other systems have faster cycle times and more efficient hardware architecture, the PDP-8's software is so highly developed that it has circumvented most hardware limitations. The user sees only a highly flexible system that has software on hand for the most diverse applications.

To some extent the low end of the PDP-11 line competes with the PDP-8 for the OEM, process control, communications, and data acquisition markets.

The PDP-11, of course, can be expanded to a powerful system that competes with some of the general-purpose commercial processors. The more extensive communication offerings on the PDP-11 partly reflect the convenience of the 16-bit word in communication networks using standard 8-bit bytes. On the other hand, the PDP-8's 12-bit word is handier for interfacing some types of analog/digital equipment that frequently has 10-bit precision.

Quite apart from inherent characteristics of the two systems, the fact remains that the PDP-8's proven software makes it competitive with many other systems, including the PDP-11, for applications requiring minicomputers of its size.

Its position is doubly unique in that it has the largest share of the market of any single system, and yet it is the only 12-bit system that still retains any sizeable share of the market at all. Other manufacturers have concentrated on 16-bit (or 8-bit or 32-bit) systems that compete more directly with the PDP-11.

At the very lowest end of the market, the PDP-8/A and Digital's MPS both compete for those users who want a 1-board CPU. This market has seen much activity recently due to the new compact memories using both core and semiconductor technologies and advances in microprocessor development. General Automation, Computer Automation, and Data General have all produced 1-board systems that are upward compatible with their major computer lines; consequently, these small systems can take advantage of a body of tested software. All of these are 16-bit systems. Although most of the competing systems have higher performance than the 8/A and some can even fit 1K or 4K words of memory on the CPU board, the 8/A still retains the advantage of its fabulous software base. For users who are not interested in the software, Digital offers the MPS based on the Intel-8 microprocessor, with processor and 1K memory on a board. The MPS has only a Teletype and console for peripherals, and it is not compatible with Digital's other systems, but a PDP-8 cross assembler provides for program development.

## USER REACTIONS

We interviewed a number of PDP-8 users, representing several models and a variety of applications. Without exception, all quoted the reliability of the system as one of its strong points. One user waxed enthusiastic on this subject and then said he didn't want to sound like an advertisement, but he had only experienced 1.5 hours of downtime since he obtained the system a year ago. These users also agreed uniformly on the quality of Digital's service organization and the ease with which the system could be fixed. Response to emergency calls was always prompt.

One user, who is a Digital employee, bought a computer for his own use and chose the PDP-8/E partly because he could just remove a module and carry it to a parts depot instead of having an expensive maintenance call. He has not been able to take advantage of this feature yet, however, because in the 1.5 years he has had the system, the only thing he had to fix was a burned-out lamp on the console, which he replaced himself.

Remarks from several users illustrate the maxim that nothing succeeds like success ("to him who has, more will be given," and so forth). One newspaper installation that has been using three PDP-8s (two PDP-8/S computers and one PDP-8/I) since 1968 for classified section updates, justification, and interfacing to an offset printing press would still choose the PDP-8 because so many PDP-8 installations are successful in that industry.

The chemistry department of a university bought its first PDP-8 system to teach majors how to use the computer in research projects; the PDP-8 was chosen because the department was new to minicomputers and Digital could give them the support needed to develop the software and maintain the hardware. A manufacturer of spectrometers chose the PDP-8 as the control component for a number of reasons. Highest on his list was the size of Digital's sales and service organization, which allowed the

spectrometer company to market its systems internationally without worrying about maintenance for the computer component.

The breadth of hardware offerings was a factor mentioned particularly among scientific users. The chemistry department mentioned earlier felt this was important because future expansion might take on unknown directions. An independent consulting service developing an inexpensive system for analysis of chromosomal aberrations needed the fully software-supported digitizer/writing tablet/spark pen combination. A PDP-8 at the center of a rapidly expanding system for monitoring pacemakers will have to handle up to 1,000 special terminals by next year. The department ordered a second PDP-8 with computer tape to process complete medical records instead of the abbreviated versions currently used.

Almost all users stressed the variety of software available as a powerful factor in selecting the PDP-8. The spectrometer manufacturer wanted a maximum number of routines to choose from so that he had a minimum amount of work to do himself. The Digital employee wanted an efficient high-level language on a 4K machine and was attracted by the FOCAL interpreter. The chemistry department wanted as much help as possible because of its inexperience.

A high school implementing a computer-related mathematics program needed an inexpensive system that could provide the BASIC language. Only the newspaper was not taking advantage of Digital's software; a software house developed the software six years ago, at the time of the initial acquisition.

Last, but hardly least, was the cost of the system. The PDP-8 has remained competitive in price and won the previously-mentioned high school math department contract by bidding to a set of specifications. Price was also an essential element to the laboratory programming for chromosomal aberrations. The big problem here was not how to detect, analyze, and interpret, but how to make the procedure cost-effective enough to become a widely available service. Competitive pricing was quoted as a factor of varying degrees of significance to each of the users.

## CONFIGURATION GUIDE

All basic PDP-8/E, 8/F, and 8/M computers use the same KK8-E Central Processor, power supply, chassis, and OMNIBUS with 20 quad bus slots. Basic systems also include memory modules, mounting, and an operator interface (either an operator's or programmer's console) and TTY control combinations. The PDP-8/E has two sets of submodels with identical specifications: one set has an on-site warranty and one set has a factory warranty. In addition, all submodels on all processors can connect to 115- and 230-volt power sources.

Memory can expand in increments of 4,096 words for core and 256 words for ROM on the 8/E, 8/F, and 8/M.

ROM and core memory can be intermixed in any desired combination, but a memory extension control is necessary when total memory exceeds 4,096 words. Maximum memory on all current PDP-8 systems is 32,768 words.

A basic PDP-8/E, 8/F, or 8/M computer uses eight to 11 of the 20 standard OMNIBUS quad slots in the basic system: central processor, five slots; programmer's console (if included), one slot; 4K-word memory, three slots or 8K-word memory with extension control, four slots; and Teletype control (if included), one slot. The operator's panel on 8/M systems does not require an OMNIBUS slot.

All 8/E, 8/F, and 8/M processors can optionally attach an Extended Arithmetic Element (EAE) and a Floating-Point Processor (FPP). Both are high-speed asynchronous hardware modules that attach to the OMNIBUS like peripheral devices. EAE performs division, multiplication, and other mathematical functions, and FPP performs floating-point and double-precision arithmetic. Both EAE and FPP increase processor throughput indirectly, because OS/8 systems equipped with these modules greatly expedite FORTRAN IV compilations and runs.

A basic 8/E system can be expanded within the main chassis through the BE8A OMNIBUS expander, which adds 18 more usable slots. In addition, a BA8 System Expander Box allows the OMNIBUS to be expanded by 18 more slots outside the chassis. The BA8 itself can be expanded by 18 additional slots for a maximum of 76 slots per 8/E system. Because the 8/F and 8/M models have smaller chassis, the internal expansion option is not available to them, and these models can expand only up to 56 slots through an external BA8 expanded to full capacity.

The PDP-8/A fits on a single 15 by 8.5-inch "hex" size board, housed in an eight-slot chassis. It can attach its own version of almost all 8/E, 8/F, and 8/M options and all of the same peripherals, except the KE8-E Extended Arithmetic Element, the AD8-E Extended Arithmetic Element, the AD8-E Analog-to-Digital Converter and MUX control, and the AM8-EA MUX and preamplifiers. The slower memory cycle of the PDP-8/A CPU (1.5 microseconds) may affect certain time-dependent PDP-8/E interfaces. Autostart is a standard feature which must be switched off if the 8/A's own power-fail/auto restart option is included.

The PDP-8/A uses 1K-, 2K-, and 4K-word MOS memory modules with 2.0 or 2.3-microsecond read and 2.8-microsecond write cycles; each module requires one slot. A special 1.5-microsecond core board is also available for the 8/A. Like the 8/E, 8/F, and 8/M, the PDP-8/A requires the KM8-A extended option board to expand memory beyond 4K words. The KM8-A also includes the PDP-8/A's power fail/auto restart option, time share control to distinguish between user and monitor modes, and a bootstrap loader. ROM memory can be added in 1K-, 2K-, or 4K-word increments, and PROM is added in 1K-word increments. Both ROM and RAM can be included on a system.

The DKC8-AA option board adds a Serial Line Unit, a Parallel I/O interface, a 100-Hertz crystal-controlled real-time clock, and a programmer's console control. The KC8-AA programmer's console is newly designed for the 8/A, with a 5 by 4-inch key pad and LED octal readouts.

The PDP-8/A-100 is offered in three packaged models that differ in the type of memory used, slots available, and power supply. The 8/A-100 is a 10-slot system, with either a 20 amp,  $\pm 5$  volt power supply, or a 1 amp,  $\pm 15$  volt power supply, battery backup for the entire system for 1 to 7 minutes, operator's panel, and chassis. Memory can be the same ROM, RAM, and PROM modules discussed for the 1-board system.

The PDP-8/A-200 is a 12-slot system with the same power options as the 8/A-100, but it has a 1-hour battery backup for the memory only. All other basic system components are the same as the 8/A-100, except that the 8/A-200 has the option of attaching a 4K-word MOS board using 4K chips with a 2.0 microsecond cycle.

The 8/A-400 system is a 12-slot system like the 8/A-200, but with 25 Amp,  $\pm 5$  volt power, no battery backup and core memory. The core board, with a 1.5-microsecond cycle time, is not compatible with the 8/E, 8/F, and 8/M systems.

No bus extensions are allowed for any of the PDP-8/A systems. Mainframe specifications are given in Table 1.

A variety of standard peripherals can be attached to any PDP-8. These are summarized in Table 2. There are some limitations on the numbers of special interfaces that can be attached to any PDP-8. Only one KA8 external interface for positive I/O devices need be attached per system. This interface can handle all traditional positive I/O bus devices. A maximum of 12 Data Break (DMA) Interfaces are allowed, with one interface per device. Up to eight DB8 Interprocessor buffers or DR8 12-channel buffered digital I/O interfaces can be attached. The maximum number of KL8-E or J Serial Line Interfaces per system is 17.

Each DB8-E interprocessor buffer allows two or more PDP-8s to exchange data. The sending computer loads the buffer from the accumulator and sets a flag in a receiving computer. Transfers are one word at a time as the receiving computer senses the set flag.

Digital has a specially-priced prepackaged system for use with the OS/8 operating system. This includes a PDP-8/E with memory extension control and time-share option, 8K or 16K words of core memory, cassette bootstrap loader, dual drive cassette system, disc cartridge system, DECwriter data terminal with a parallel interface and freestanding cabinet.

Each major software package has minimum configuration requirements. Table 3 summarizes PDP-8's system software and the configuration requirements of the major packages.



## COMPATIBILITY

Generally, the various members of the PDP-8 family are compatible with comparable configurations from one model to the next. In some cases, however, users' software must be reprogrammed for an improved optional feature, such as the PDP-8/E EAE (Extended Arithmetic Element), which differs significantly from previous EAE options. This option uses some of the instruction codes previously available for microcoding the Operate instructions.

The Positive I/O Bus Interface allows peripherals originally designed for the PDP-8/I, 8/L, and 8/S systems to be attached to the OMNIBUS on the PDP-8/E, 8/F, and 8/M. Because the PDP-8/A uses an OMNIBUS similar to the 8/E and it can attach the Positive I/O Bus, nearly all PDP-8 peripherals can attach to the 8/A. Exceptions are the A/D converter and its related MUX. The 8/A is slower

**Table 1. Digital Equipment PDP-8: Mainframe Specifications**

MODEL	8/E, 8/F, 8/M	8/A
<b>CENTRAL PROCESSOR</b>		
Microprogrammed	No	No
No. of CPU boards	5	1
No. of Registers	5	5
Addressing		
Direct	256	256
Indirect	1 level to 4K	1 level to 4K
Indexed	1 level "auto index"	1 level "auto index"
Instruction Set		
Number (std; opt)	56; 72	56
Extended Arithmetic	Yes, option	No
Decimal Arithmetic	No	No
Floating Point	Hardware option	Hardware option
Priority Interrupt Levels	1	1
<b>MAIN STORAGE</b>		
Type	Core	MOS; core
Cycle Time ( $\mu$ sec/wd)	1.2; 1.4 (2 accesses)	2.3 read, 2.8 read/write (MOS); 1.5 (core)
Basic Addressable Unit		
Unit	12-bit wd	12-bit wd
Bytes/Access	2 (6-bit)	2 (6-bit)
Min Capacity (wds)	4K	1K
Max Capacity (wds)	32K	32K
Increment Size (wds)	4K; 8K	1K; 2K; 4K
Ports/Module	1	1
Parity	Option	Option
Protect	Software or ROM	Software or ROM
Memory Management ROM	To 32K	To 32K
Use	Program protection	Program protection
Capacity (wds/module)	256	1K-32K/system
PROM	1K-wd module	1K-wd module
<b>INPUT/OUTPUT</b>		
Programmed I/O	Yes	Yes
DMA Channels (no.)	1-12	1-12
Multiplexed I/O	No	No
Data Break (for positive I/O devices)	Option	Option
Max DMA Transfer Rate (wds/sec)	833,333	333,333 (MOS), 833,333 (core)

than an 8/E, and also does not have an EAE like the 8/Es. These may create some compatibility problems with time-dependent programs and interfaces.

## MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks in the United States and worldwide, numbering more than 1,500 engineers.

**Table 2. Digital Equipment PDP-8: Peripherals**

MODEL NUMBER	DESCRIPTION
<b>DISCS</b>	
DF32/DS32	Fixed Disc, 32K wds/drive, 4 drives/controller
RF08/RS08	Fixed Disc, 262K wds/drive, 4 drives/controller
RK8/RK05	Disc Cartridge System, 1.6M wds/drive, 4 drives/controller
<b>MAGNETIC TAPE</b>	
TC08/TU56	DECtape, 8 drives/controller
TD8/TD8-E	Dual DEC cassette, 75K-byte capacity/cassette, 8/system
TM8/TU10	7- and 9-trk DEC MAGtape drives, 8 drives/controller
<b>CARDS</b>	
CM8	Optical Mark Card Reader, 300 cpm
CR8	Punch Card Reader, 300 cpm
<b>PAPER TAPE</b>	
PR8	Reader
PP8	Punch
PC8	Combination Reader/Punch
<b>PRINTERS</b>	
LS8	Dot Matrix Printer, 165 cps
LE8	Line Printers, 173-356 lpm
LS01	Printer for VT8 Display, 165 cps
<b>TELETYPEWRITERS</b>	
LT33/LT35	ASR & KSR Teletypes, 10 cps
LA30	DECwriter, 30 cps
<b>DISPLAYS</b>	
VT8	Alphanumeric and Graphics Display
VC8/VR14, VR20	Plot Display, Subsystem, B & W or 2-color display
VT05	A/N Terminal 1,440 Char (72 x 20)
<b>PLOTTERS</b>	
XY8 Series	CalComp 565, 563, and Houston Instruments DP-1, DP-10
<b>TERMINALS</b>	
RT01	Numeric Data Entry Terminal, 16-digit display
RT02	Alphanumeric Data Entry Terminal, 32-digit display
<b>WRITING TABLETS</b>	
VW01 Series	Tablets, 4 multiplexors/control
<b>COMMUNICATIONS</b>	
KL8 Series	Async Line Interface, 110-2,400 baud models
DP8	Sync Modem Interface
DC08	ACU and 10-channel Multiplexor
<b>PROCESS I/O</b>	
AD8	10-bit Subsystem, up to 16 chan
AD01	10-bit Subsystem, up to 32 chan
AF04A	Integrated Digital Voltmeter, to 128 chan
AFC8	Low-Level Differential Analog Input Subsystem, up to 128 chan
AA50	Digital-to-Analog Subsystem, up to 6 chan
UDC8	Digital I/O to 192 digital pts

Aside from 46 sales and service locations in the United States, Digital has five offices in Canada, six in Australia, five in Germany, six in the United Kingdom, three in Brazil and one or two each in Argentina, Austria, Belgium, Chile, Denmark, Finland, France, India, Israel, Italy, Japan, Mexico, Netherlands, New Zealand, Norway, Phillipines, Puerto Rico, Spain, Sweden, Switzerland, and Venezuela. Although minicomputer manufacturers have traditionally aimed at somewhat "self-sufficient" users, requiring considerably less software support and applications programming assistance than the large commercial system users, this picture is changing, as evidenced by Digital's recently-added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour shifts. An on-site engineer can be hired if requirements are critical, or a user can buy an on-call service or set up his own maintenance staff.

**Table 3. Digital Equipment PDP-8: Software**

PACKAGE	DESCRIPTION
OS-8	Standard PDP-8 operating system for batch and interactive processing, requires 8K-wd memory, cassette I/O and bootstrap, disc, and DECwriter terminal
RTS-8	Real-Time multiprogramming system
CAPS-8	For small cassette-based system, requires 4K-wd memory, 2 TU-60 cassette drives, teletypewriter
TS8/E	Time-sharing system for up to 17 users, requires 8K-wd memory, KM8-E Interface
COS-300	Commercial operating system, requires 8K-word memory, discs, console, printer; can operate in foreground/background mode

**Table 3. (Contd.)**

PACKAGE	DESCRIPTION
BASIC	9 different packages: EDU System 10, 20, 28, 30 versions using OS/8, CAPS-8, LAB 8/E, Industrial real-time BASIC, Dartmouth BASIC. Various requirements range from 4K-12K-wd memories, all require LT33-D or LA30-P terminals, some require PC8-E, others require RK8-E disc, TU56 tape, or DECTape
FOCAL	Interactive language for small computers, requires 4K-wd memory, LT33-D terminal
FORTRAN, FORTRAN IV	FORTRAN in stand-alone or OS/8 versions, FORTRAN IV for OS/8, all require 8K-wd memory, PC8-E, LT33-D or LA30-P terminals, OS/8 versions read disc
DIBOL	COBOL-like language for 8K-wd system under OS/8
ALGOL	From DECUS; ALGOL 60 subset of ALGOL-8
Assemblers	PAL III or PAL C/Macro-8 require 4K-wd memory, and LT33-D terminal; SABR stand-alone, OS/8, PAL-8, CAPS-8, PAL-C, and OS/8 SABR need 8K wds of memory
Utilities	4 Symbolic editors, 3 floating-pt package, libraries, editors, loaders, debuggers, diagnostics, many others
EduSystems	For hands-on classroom use with BASIC or FOCAL single-user to 8 users and batch versions (several versions)
Typeset-8	Several typesetting systems for justifying, hyphenating, etc.
COGO-8	For interactive graphics control, requires 16K-wd memory, OS/8, 2 DECTape drives, DECwriter
LAB-8	Signal Averaging System for 8/E with 10-bit A/D, 10-bit plot display controller, clock, lab panel, and ASR-33
Communications	Programs for concentration, message switching, data collection, remote batch

**TYPICAL PRICES**

Model Number	Description	Purchase \$	Monthly Maint. \$
<b>SYSTEMS</b>			
STD8E CA/CB	Packaged Hardware/Software System RK8-E Cartridge Disk System TA8E DECcassette with dual drives PDP-8/E Central Processor (8K words) Decwriter M18-EL Bootstrap for DECcassette H960-BC Cabinet	18,000	232
STD8E CC/CD	OS/8 Operating System on Cassette	20,000	275
LAB8E-05	Same as STD8E-CA/CB Except with 16K Words of Memory The LAB8E-05 PDP-8/E-PA Tabletop PDP-8/E (4K memory) H945-AA Laboratory Data Panel (tabletop) LT33-D ASR-33 Teletypewriter and Punch AD8-ES 10-Bit A/D Converter VC8-E 10-Bit Point Plot Display Controller DK8-ES Real-Time, Programmable Clock LAB8E Software Kit	9,760	117



**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
LAB8E BA/BB	Laboratory System for General Purpose Computing PDP-8/E-NE/NF Central Processor (8K-wd core memory; terminal control) LT33-DC/DD ASR 33 Terminal AD8-EA A/D Converter AM8-EA 8-Channel MUX and Preamps AM8-EC Control Panel DK8-ES Programmable Clock, Schmitt Triggers, and Front Panel VC8-E Scope Controller H945-AB/CB Cab Mounting Panel H960-BB/CB Cabinet LAB8E Software Kit	13,470	151
OS/8-10	Complete Hardware/Software System PDP-8/E1AE Central Processor (8K-wd core memory) DECwriter Terminal MR8-EC Bootstrap Loader TD8-EM Dual DECTape Drives H967-BA Cabinet H952-HA Table OS/8 System Software	14,400	161
LAB8E-15	System PDP-8/E-NE Rack-Mountable PDP-8/E; 8K Memory less Teletype Control PC8-E High-Speed Paper Tape Reader/Punch DECwriter Terminal H945-AB Laboratory Data Panel; Rack Mountable VC8-E 10-Bit Point Plot Display Controller AD8-EA + AM8-EA + AM8-EC 10-Bit A/D Converter; 8-Chan Multiplexor DK8-ES Real-Time Programmable Clock VR14 7 x 9in Point-Plot CRT H960-BB 19in Freestanding Cabinet QF060-AB LAB8E Paper Tape Software Kit	20,000	202
LAB8E-25	System PDP-8/E-NE Rack-Mountable PDP-8/E; 8K Memory less Teletype Control BE8-A 20-Quad-Slot OMNIBUS Expander DECwriter Terminal H945-AB Laboratory Data Panel (rack mountable) VC8-E 10-Bit Point-Plot Display Controller AD8-EA 10-Bit A/D Converter; 8-Channel AM8-EA/EC Multiplexor DK8-ES Real-Time Programmable Clock VR14 7 x 9in Point-Plot CRT MR8-EC 256-Word OS/8 Read-Only Memory TD8-EM OMNIBUS DECTape Control and Dual DECTape Drive H952-HA Programmer's Table H960-BB 19in Freestanding Cabinet OS/8 Software Kit; OS/8 Extension Kit; OS/8 LAB-8/E Software Kit	22,600	218
<b>CENTRAL PROCESSORS AND WORKING STORAGE</b>			
8A100-AC/AD	ROM Machine (with KK8-A CPU, 1K MS8-AA RAM memory; operator's panel and combination power supply, chassis, and OMNIBUS with 10 slots)	1,745	NA
8A100-AK/AL	Same as 8A100-AC/AD (except 4K RAM memory)	2,600	NA
8A100-FA/FB	Same as 8A100-AC/AD (except 1K PROM memory)	2,375	NA
8A200-AK/AL	RAM Machine (with KK8-A CPU; MS8-BA 4K RAM memory; operator's panel and combination power supply, chassis, and OMNIBUS with 12 slots)	1,995	NA
8A400-EM/EN	KK8-A CPU (with MM8-AA 8K core memory; operator's panel KM8-E memory extension control and combination power supply, chassis, and OMNIBUS with 12 slots)	2,795	43
8A400-BM/BN	CPU (with 8K core memory, 1 1KK8-A CPU; MM8-AA 8K core memory; operator's panel and KM8-AA extended option board)	2,995	44
PDP-8/E-AA/AB*	Computer (4K-core memory and Teletype control; rack mountable; slides included) KK8-E Central Processor MM8-E 4K Core Memory KC8-EA Programmer's Console KL8-E Console Teletype Control Combination Power Supply, Chassis, and OMNIBUS with 20-Quad Bus Slots	4,490	53
PDP-8/E-AE/AF*	Same as PDP-8/E-AA (except MC8-EJ 8K core memory and memory extension control)	5,650	74
PDP-8E-AS	Same as PDP-8/E-AE (except with MM8-EJ 8K core memory added for total of 16K)	7,670	117
PDP-8E-AT			
PDP-8/F-AH/AJ	Same as PDP-8/E-AA (with KC8-EA replaced by KC8-FL programmer's console)	3,990	53
PDP-8/F-AK/AL	Same as PDP-8/F-AH (except with memory extension control and MM8-E core replaced by MC8-EJ 8K core memory)	5,150	74

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price \$	Monthly Maint. \$
PDP-8/F-AS/AT	Same as PDP-8/F-AS (with MM8-EJ 8K core memory module added for total of 16K)	6,870	117
PDP8M-MH/MJ (OEM)	CPU (with 4K core (includes KK8-E CPU, MM8-E 4K core memory; KC8-M operator's panel and combination power supply, chassis, and OMNIBUS with 20 quad bus slots)	3,200	NA
PDP8M-MK/ML (OEM)	Same as PDP8M-MH/MJ (except with MC8-EJ 8K core memory and control)	4,000	NA
PDP8M-DH/DJ (OEM)	Same as PDP8M-MH/MJ (except with programmer's console and KL8-E console Teletype control)	3,800	53
PDP8M-MM/MN (OEM)	CPU with 1 MR8-FB 1K PROM Memory with 256 RAM	2,750	NA
<b>PROCESSOR OPTIONS</b>			
KE8-E	Extended Arithmetic Element (EAE)	1,200	5
KP8-E	Power Fail Detector and Auto Restart	270	2
FPP12-AB	Floating-Point Processor (24 + 12 bits; supporting software requires min OS/8 configuration)	8,500	51
FPP12-AE	Double-Precision Option for FPP12-AB only (provides 60 + 12 bits capability)	2,700	16
<b>PDP 8A OPTIONS</b>			
DKC8-AA	I/O opt board (includes real-time clock, 100 Hz, fixed frequency; programmer's console control, I/O interface; 12-bit parallel I/O; async serial line unit; switch selectable baud rates)	500	8
KM8-AA	Extended option board (includes memory extension and timeshare control; power fail/auto restart; bootstrap loader; switch selectable)	500	8
MR8-SL	PROM Loader	2,625	21
KC8-AA	Programmer's Console for 8/A	400	8
KC8-AB	Remote programmer's console for 8/A	550	8
KM8-E	Memory extension and Timeshare	350	2
MR8-AS	ROM Blasting (programming) Set-up Charge	150/order	—
MR8-AT	ROM Blasting Service	100/board	—
<b>PROM MEMORY</b>			
MR8-FB	1K-wd PROM Memory (with 256-word RAM memory)	995	—
MR8-EC	256-wd OS/8 ROM (for TD8-E Systems)	900	5
MR8-SL	PROM Loader with cables	2,625	21
MS8-AA	PDP-8/A Memory Options reading		
MR8-AA	1K Semiconductor Random Access Memory (RAM) for 8/A 100	480	NA
MR8-AA	1K Semiconductor Blastable Read-Only Memory (ROM for 8/A 100, 200, 400)	480	NA
MR8-FB	1K UV Erasable Reprogrammable Read-Only Memory (PROM for 8/A 100, 200, 400)	995	NA
MS8-BA	4K Random Access Memory (RAM for 8/A 200)	895	NA
<b>MEMORY OPTIONS</b>			
<b>CORE MEMORY</b>			
MM8-EJ	8K-Core Memory Expansion	3,900	
MM8-E	4K-Core Memory Expansion	2,500	
KM8-E	Memory Extension & Time-Share Control	350	
<b>READ-ONLY MEMORY</b>			
MI8-E	Hardware Bootstrap Loader	540	
MR8-EC	256-Word OS/8 ROM and Bootstrap for TD8-E Systems	860	
<b>MASS STORAGE</b>			
<b>Discs</b>			
DF32-DP/EP	Fixed-Head Disc File and Control; 32K Wds; Controls up to 3 DS32-D Disc Expanders	7,000	32
DS32-D/E	Disc Expander (32K wds)	4,000	16
RK8-EA/EB	Disc Cartridge System (controller and 1.6M-wd drive, supports up to 3 addl RK05 drives)	7,900	74
RK05-AA/BB	Disc Cartridge Drive (1.6M wds)	5,100	64
RK05K-8	Disc Cartridge	99	—
<b>INPUT/OUTPUT</b>			
<b>Interfaces</b>			
KA8-E	External Interface for Positive I/O Devices (max 1/system)	270	3
KD8-E	Data Break Interface (max 12/system)	540	3
DR8-EA	12-Channel Buffered I/O Interface	540	5
<b>CLOCKS</b>			
DK8-EA	Fixed Interval Clock, Line Frequency	270	2
DK8-EC	Real-Time Clock (fixed interval; crystal frequency)	320	2
DK8-EP	Real-Time Clock (programmable)	700	3
DK8-ES	Programmable, Real-time Clock (with 3 Schmitt triggers and control panel)	1,350	5



**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
<b>TERMINALS</b>			
	All Terminals Require KL8-JA Interface		
LT33-CC/CD	KSR 33 Keybd	1,400	32
LT33-DC/DD	ASR 33 Sync	1,850	37
LA36-CA/CB	DECwriter Data Terminal (300 cps; 132-col; 96-char uc/lc; 110, 150, & 300 baud)	1,850	
VT05B-AA/AD	A/N Display with Keybd	2,795	23
VT50-AA	DECscope Video Terminal	1,250	22
<b>CARD READERS</b>			
CM8-FA/FB	Optical Mark Card Reader and Control (300 cpm)	5,290	53
CR8-FA/FB	Punched Card Reader and Control (300 cpm)	4,860	53
<b>PAPER TAPE</b>			
PC8-E/EA	Combination Paper Tape Reader/Punch and Controls (rack mountable)	3,900	37
<b>LINE PRINTERS</b>			
LS8-FA/FB	Line Printer and Controller	5,615	58
LV8-BA/BB	Electrostatic Printer/Plotter	11,770	53
LE8-VA/VD	Line Printer and Controller	9,900	72
LE8-WA/WD	Line Printer and Controller	11,900	72
<b>MAGNETIC TAPE</b>			
TA8-AA/AB	DECcassette System	2,990	40
TD8-EH	OMNIBUS DECTape Control and Single DECTape Drive	4,000	32
TD8-EM	OMNIBUS DECTape Control and Dual DECTape Drive	5,500	42
TM8-EA/ED	DEC Magtape Drive and Controller (9-track)	10,745	101
TM8-FA/FD	DEC Magtape Drive and Controller (7-track)	12,500	101
<b>PLOTTERS</b>			
XY8-E	Plotter Control Module Only	540	8
XY8-EK/EL	Incremental Flatbed Plotter and Control	3,995	23
XY8-EH/EJ	Incremental Flatbed Plotter and Control	3,995	23
<b>GRAPHIC DISPLAYS</b>			
<b>DISPLAYS</b>			
VC8-E	Point-plot Display Control	1,185	11
VR14	CRT Display (7 x 9in point-plot)	3,240	19
<b>DATA COMMUNICATIONS</b>			
KL8-JA	Async Serial Line Interface	425	11
KL8-M	Modem Control Interface (for Bell 103 and 202 modems)	400	5
H308	Null Modem Adapter (needed when a modem is not used)	65	—
DP8-EA	Sync Modem Interface (for Bell 201 modems)	1,620	11
DP8-EB	Sync Modem Interface (for Bell 300 modems)	2,000	11
—	Not Applicable		
NA	Not Available		
NC	No Charge		

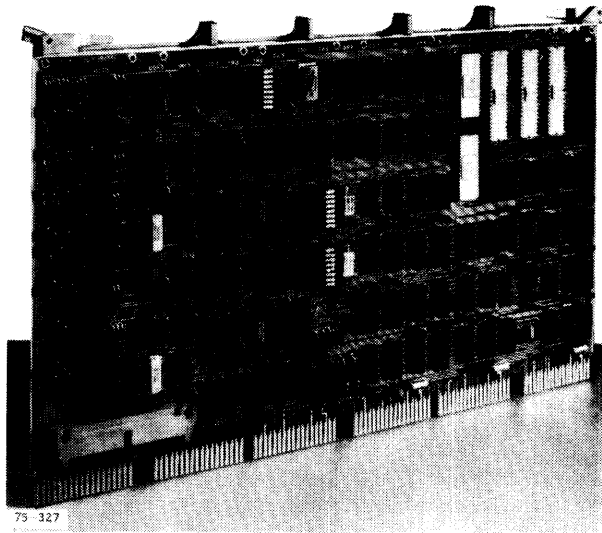
**HEADQUARTERS**

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## DIGITAL EQUIPMENT

### PDP-8 System Report Update



75-327

Digital's KL8-A Four-Channel Multiplexor

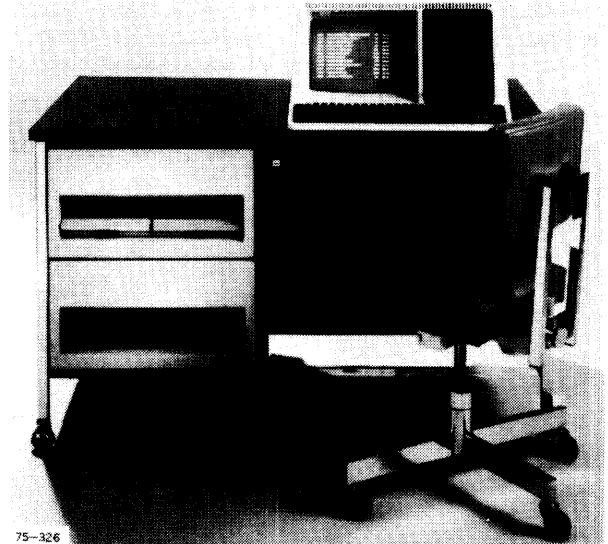
#### Four-Channel Multiplexor

The KL8-A, a four-line serial asynchronous multiplexor for the PDP-8/A, offers partial modem control for three lines and full modem control for one line. The multiplexor gives small PDP-8/A systems multiple-terminal capability; it allows them to operate as a miniconcentrator, intelligent terminal, or cluster controller. The KL8-A includes a 32-character silo (First In, First Out receive buffer) and a branch addressing scheme to provide vectored interrupts for the four lines. Only one PDP-8/A OMNIBUS slot is needed for the KL8-A.

Purchase price is \$995, and the unit is available 60 days after the order is received by Digital.

#### System 800 (or MS800) Announced

System 800 is a new PDP-8/A computer package for the OEM market for office computers. The system is housed in a desk with a dual floppy disc drive unit, and it operates under OS/8 control. The processor features power fail/auto restart, real-time clock, and both a serial and parallel I/O interface. Memory capacity is 8K or 16K 12-bit words. The system can be configured with the VT50 Series of Digital's video terminals or with the LA36 DECwriter terminal printers. ROM-based diagnostics are automatically run to check out the system each time it is turned on.



75-326

MS800 or System 800

The system is designed to operate as a stand-alone system or as a remote station in a computer network.

Two models are currently available:

- MS800-A with 8K words of memory; priced at \$8,995.
- MS800-B with 16K words of memory; priced at \$9,995.

Quantity discounts are available for both models. Deliveries are scheduled for 60 days after receipt of order.

#### CLASSIC™ and CMS/I

Three entry-level hardware/software packages are based on the PDP-8/A: the DEC Datasystem 300 series for business data processing, CLASSIC™ (Classroom Interactive Computer) for educational institutions and CMS/I (Computational Minicomputer System) for construction, civil, aerospace, and other engineers within departments of companies or government agencies. The packages are built around a PDP-8/A processor with core memory, dual diskette drives, VT50 display system and PDP-8 software. Table 1 shows CLASSIC and CMS/I characteristics. The DEC Datasystem 300 series is covered in Small Business Computers, report number 140.3451.080.

™ Trademark of Digital

CLASSIC consists of a PDP-8/A with 16K words of core memory; a VT50 CRT console with keyboard and printer; dual diskette drive unit; and OS/8 operating system with BASIC. The system has no standard options other than FORTRAN IV and the CLASSIC Curriculum #1 and Applications #1 software packages.

The Curriculum #1 package is for secondary schools. It includes computer-aided instruction (CAI) programs for up to 97 texts in mathematics, social science, science, and business studies.



*Digital's CLASSIC*

The Applications #1 package is primarily for higher-education institutions (above 12th grade). It includes user-submitted programs in FORTRAN and BASIC for three major application areas: mathematics, statistics, and business. Programs are designed for students as well as teachers.

CMS/1 consists of a PDP-8/A with 16K words of core memory, VT50 CRT console with keyboard and display, dual diskette drives (capacity of 670,000 characters), and OS/8 operating system with both BASIC and FORTRAN IV. Optional features include a second diskette drive, an electrolytic printer for the VT50 console, LA36 DECwriter II, and COGO (Coordinate Geometry) applications software. Both the CMS/1 and CLASSIC systems will be delivered 180 days after receipt of order.

The CLASSIC and CMS/1 systems are aimed at markets that Digital has traditionally served well. Major competition comes from Hewlett-Packard and Data General.

Since older Digital EDU systems and engineering systems cost considerably more than CLASSIC and CMS/1, they usually had to be timesharing systems for institutions or engineering departments of companies to justify their cost. Many more schools and engineering

departments can afford a CLASSIC or CMS/1 system because the cost is low. In fact, schools may even be able to afford multiple CLASSIC systems within a single classroom. Individual engineers may have personal computers. Undoubtedly, the computers to people ratio will increase.

Furthermore, Digital is marketing CLASSIC and CMS/1 as total systems, with applications software drawn from the DECUS (Digital Equipment User Society) library. These software packages, developed by PDP-8 users, have been put together into coherent applications modules which the company will now support.

The PDP-8 is unique in the minicomputer industry in the amount of applications software that has been programmed for it. Much of that software resides in the DECUS library. Furthermore, Digital has long nurtured and supported DECUS, which is also unique among user's groups because of its organization and vitality. Thus, more user software will undoubtedly be added to the DECUS library.

CLASSIC and CMS/1 are well-thought-out systems, which are based on Digital's strengths. They are aimed at markets that Digital knows well, and use hardware compatible with the PDP-8 (the longest-lived minicomputer), for which an almost endless source of software is available. The systems are tightly bundled, for Digital at any rate, to keep the system cost so low that competitors will have a hard time meeting it. Furthermore, by moving system cost downward, the company considerably increases the market for these systems. Thus, the CLASSIC and CMS/1 systems appear to be ideal Digital products and destined for success.

### Unbundled PDP-8/A

Digital's PDP-8/A-100 and PDP-8/A-400 processors are now available on a board-by-board, building-block basis. The PDP-8/As were unbundled so they could be used in such applications as optical character recognition.



*Digital's CMS/1*



**Table 1. Digital Equipment PDP-8: CMS/1 and Classic**

Characteristic	CMS/1	CLASSIC
<b>CPU</b>	PDP-8/A	PDP-8/A
<b>Memory</b>		
Type	Core	Core
Size	32K char*	32K char*
Cycle Time		
<b>Diskette</b>	2 or 4 drives	2 or 4 drives
Use	Mass storage	Mass storage
Capacity	670,000 to 1.34M	670,000
Speed	NA	NA
<b>Disc Storage</b>		
Type	—	—
Capacity	—	—
Average Access time	—	—
<b>Console</b>		
Keyboard	Typewriter kybd, numeric pad, & 24 function keys	Typewriter kybd, numeric pad, & 24 function keys
Display	12 lines, 80 char each	12 lines, 80 char each
Printer	Opt	Std
<b>Line Printer</b>	30 cps DECwriter II	No
<b>DATA COMM</b>	No	No
<b>Data Entry</b>	Console	Console
<b>Software</b>		
Operating System	OS/8	OS/8
Language	BASIC; FORTRAN IV	BASIC; FORTRAN IV
Applications	Applications Package with COGO (opt)	Applications #1 (opt) #1 (opt)
<b>Minimum Price \$</b>	12,000	7,900
<b>First Delivery</b>	180 days ARO	180 days ARO

Notes:  
Using standard interchange format  
\* 6 bits

patient monitoring, and communications, with low-end computing requirements.

The basic semiconductor-memory configuration includes the central processor, 1K-word semiconductor RAM, 2K words of ROM, and a 6-slot OMNIBUS™. This configuration sells for \$1,830 in single quantities and for \$1,309 in quantities of 20. The typical core configuration includes the CPU with 8K words of core, memory extension, time-share control, bootstrap loader, power-fail/auto-restart, and the 6-slot OMNIBUS.

### AD8-A Analog-to-Digital Subsystem

The AD8-A, a compact analog-to-digital converter subsystem, is now available for use with all the PDP-8 minis. The converter subsystem consists of a 10-bit analog-to-digital converter, 16-channel multiplexor, and a sample-and-hold circuit. Programming for the new model is compatible with the AD8-E analog-to-digital converter now available. The unit is supported under LAB8/E paper tape software, and the OS/8 operating system under BASIC. The maximum program control sampling rate is 28K Hertz. The input range is program-selectable for unipolar (0V to +5V) or bipolar (-2.5V to +2.5V) operation. The AD8-A is priced at \$1,000 for a single unit and \$710 in 20-unit quantities.

### RX8 Floppy Disc System

Digital has also introduced RX8, a new low cost floppy disc system for the PDP-8. The system has a capacity of

256K bytes or 128K 12-bit words and an average access time of 483 milliseconds. RX8 is available in single- and dual-drive configurations and is supported by extensive diagnostic and operating system software.

RX8 data operations are handled in either byte mode or 12-bit word mode. Preformatted industry-compatible diskettes with 77 tracks, 26 sectors per track are used with the system, which fits into a standard 19-inch rack. Only the head contacts the surface during reading and writing, prolonging disc life. RX8 can be used for input-output or, for small configurations, as random access files.

A single disc configuration sells for \$2,900 and a dual-disc drive for \$3,900. Diskettes for the model cost \$40 for 5-diskette lots or \$75 in 10-diskette lots. The RX-8 subsystem is available 30 days after the order is received.

### RTS/8 Real-Time Operating System

The RTS/8, an event-driven, a real-time operating system, is now available to run on a minimum configuration with only 4K words of main memory; a memory-resident executive requires less than 700 words of core or semiconductor memory.

A PDP-8 with only 12K words of memory can support a full foreground/background system. Real-time events can be controlled and programs developed concurrently via the OS/8 operating system.

## DIGITAL EQUIPMENT — PDP-8 SYSTEM REPORT UPDATE

RTS/8 controls up to 63 tasks on a fixed priority basis. Tasks can be stored in memory or on disc and swapped in when needed. Support tasks provide for a variety of peripherals, including analog-to-digital devices, discs, magnetic tape, printers, and monitor units.

The new operating system is memory efficient and reduces software development costs, according to Digital. It supports features such as dynamic task scheduling, multiprogramming, multiple buffered I/O, intertask communication, on-line operator control, and foreground/background processing. The small size of the RTS/8 executive permits the operating system to be used in cost-sensitive applications.

The price of RTS/8 is \$500 for a single-user license. RTS/8 and OS/8 together cost \$750. For OEM customers, a multi-use license is available.

### PRICE DATA

Identity	Purchase Price \$	Monthly Maint. \$
CMS/1	12,000	115
Copier(1)	500	
Second Diskette Drive	3,500	
CMS/1 Applications Package (one-time charge)	395	
CLASSIC	7,900(2)	115
FORTRAN IV option (one-time charge)	700	
Curriculum Package #1 (one-time charge)	395	
Applications Package #1 (one-time charge)	395	

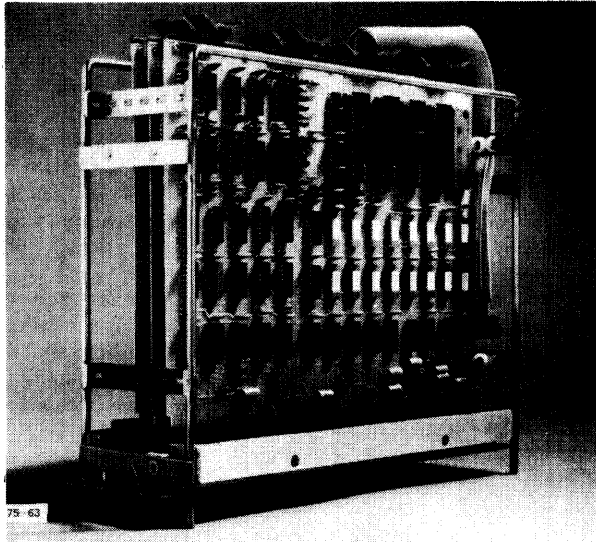
**Notes:**

(1) Unavailable as separate item.

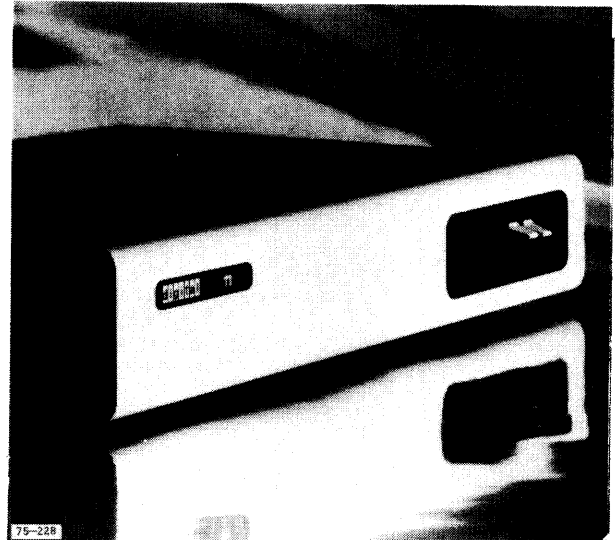
(2) Non discountable; also available under 5- to 7-year full payout lease.

## DIGITAL EQUIPMENT CORP.

### LSI-11 and PDP-11/03 System Report



LSI-11



PDP-11/03

#### OVERVIEW

With the introduction of the LSI-11, Digital reaffirms the company's policy of providing more computing power at less cost. This low-entry-level system in the popular PDP-11 product line (over 20,000 installed) occupies a unique position; it is a microcomputer that implements the PDP-11/40 instruction set and offers the performance of the PDP-11/05. The flexibility and power of the PDP-11 line and the advantages of its upward software compatibility are thus available to users at the microcomputer market level, and at prices lower than previously charged for the 11/05.

In quantities of 100, an LSI-11 processor with a 1,200-nanosecond processor cycle time, I/O bus, 4K-word MOS Random-Access Memory (RAM), real-time clock, single-level interrupt, and power fail/auto restart for stand-alone operation costs less than \$700. All components are mounted on one 8.5-by-10-inch board. A boxed version of the LSI-11, aimed at single-unit users and called the PDP-11/03, contains a processor with 4K words of MOS RAM or core memory, a serial interface, power supply, rack-mountable enclosure, and an operator's front panel; it is available in both 115 and 230VAC models. The purchase price of the MOS RAM boxed configuration is less than \$2,500 while the price of the core 11/03 is less than \$3,000. Table 1 lists mainframe characteristics of the LSI-11 and PDP-11/03.

A multi-user (up to four) timesharing system called the MU/11V03 is also offered. The MU/11V03 includes the

PDP-11/03, a dual flexible disc unit, interactive video display and/or printer terminals, and RT-11 software.

The KD11-F, the LSI-11 processor, is contained on four 16-bit, N-channel metal oxide semiconductor chips manufactured by Western Digital, an independent calculator manufacturer. The processor contains eight general-purpose registers, extended arithmetic, serial line interface module, parallel line interface module, and four expansion memory modules are optional. The bus structure is similar to that of the PDP-11 UNIBUS in that the highest priority device is located closest electrically to the microcomputer, but the LSI-11 bus and the PDP-11 UNIBUS are not compatible.

The core version of the PDP-11/03 uses an alternate processor, the KD11-J, which has no on-board memory. The purchase price for the two-board stripped "microcomputer" version is under \$1,000.

Standard peripherals currently consist of several types of terminals (CRT and Teletype) and a floppy disc subsystem.

#### HEADQUARTERS

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Marlborough MA 01752  
(617) 481-7400

# DIGITAL EQUIPMENT CORP. — LSI-11 AND PDP-11/03 SYSTEM REPORT

**Table 1. Digital Equipment LSI-11 (PDP-11/03): Mainframe Characteristics**

<b>MODELS</b>	LSI-11 & PDP-11/03
<b>CENTRAL PROCESSOR</b>	KD11-F (MOS) or KD11-J (core)
Microprogrammed	Yes
No. of Registers	6 general, 1 stack pointer, 1 program counter
<b>Addressing (no. of wds)</b>	
Direct	32K
Indirect	32K
Indexed	32K
Mapping	No
<b>Inst Set</b>	Same as PDP-11/40
Implementation	Microcode
Types	Singleword, doubleword
No.	
FI P	Opt
Hardware Stack	Yes
<b>Inst Execution</b>	
Times ( $\mu$ sec)	
F P	
Add	3.5 (reg to reg); 12.0 (memory to memory)
Multiply	24-64 (memory to reg)
Divide	78 (memory to reg)
FI P <sup>1</sup>	
Add/Subtract	42.0
Multiply	52-92
Divide	151
<b>Writable Control Store</b>	No
<b>Interrupts</b>	
Levels	1 line, multilevel
Type	Hardware
<b>Processor Cycle Time</b>	1.2 $\mu$ sec
<b>MAIN STORAGE</b>	
Type	RAM; core; PROM/ROM
Speed	350 nsec access time (RAM); 900 $\mu$ sec cycle time (core); 40 nsec access time (PROM/ROM)
<b>Basic Addressable Unit</b>	Byte/word
Bytes/Access	2
<b>Cache Memory</b>	No
<b>Capacity (bytes)</b>	
Min	8K (RAM); none (core); none (PROM/ROM)
Max	64K (RAM); 64K (core); 8K (PROM/ROM)
<b>Increment Size (bytes)</b>	2K/8K (RAM); 8K (core); 512K/1K (PROM/ROM)
<b>Ports/Module</b>	1
Error Checks	No
Memory Protection	No
Memory Management	No
Interleaving	No
<b>INPUT/OUTPUT</b>	
Max Devices Addressable	No practical limit (4,096)
Programmed I/O	Yes
DMA	Yes
DMA Transfer Rate	833K wds/sec

Note:  
(1) Two-word operands

Software can be either a minimal paper tape run-time system or the compact RT-11 operating system. RT-11 has a number of versions depending on user requirements. It can be a single-job batch, real-time, or interactive system or a foreground/background timesharing system with up to three BASIC programs in the foreground and one FORTRAN program in the background. Languages supported

are BASIC, FOCAL, FORTRAN, and MACRO assembly language.

## COMPETITIVE POSITION

The LSI-11 system is aimed at the OEM market and high-volume end users. It is designed for easy interfacing to machines, instruments, and terminals. Digital expects to penetrate markets in business, communications, education, health, industrial control, laboratory automation, process control, and transportation. The boxed PDP-11/03 is aimed at individual end users, basically supplanting the 11/05 (and in many respects the 11/15 and 11/20) with a lower cost, more versatile system. The MU/11V03 is initially aimed at the education market where it can provide low-cost interactive processing for students.

The LSI-11 is slower than most minicomputers and its I/O is rudimentary. It is ideal, however, for dedicated applications that require power but relatively low speed. The LSI-11 offers a challenge to microcomputer manufacturers as well as to minicomputer manufacturers because it is a low-level entry in the PDP-11 line. In addition, microcomputer manufacturers generally cannot offer such an attractive upward migration path.

Minicomputer manufacturers are increasingly entering this low end of the market and provide growing competition for microcomputers and each other. Computer Automation and General Automation both have systems comparable to the 11/03. Texas Instruments also has a new system that undercuts the price of the other three but does not have a long-standing well established product line behind it yet. Of course many OEM users do not care about existing software, but PDP-11/03 and MU/11V03 end users will care a great deal. Table 2 compares specifications of some of these systems.

The popularity of the LSI-11 is well established; the 1,000th unit was delivered only 10 months after its introduction. The PDP-11/03 and MU/11V03 have not yet established track records, but the education market should welcome the economics of a timesharing microcomputer.

Despite Digital's gradual move upward in computing power for its minicomputers, the company management has not forgotten that their initial forte was to provide low-cost, reliable, and convenient computer power. After all, FOCAL was the first higher level language to run on a 4K-word computer system and DECTape was the first random access mass storage device for minicomputers. The LSI-11, PDP-11/03, and MU/11V03 continue Digital's tradition of providing more computer power for entry-level users.

## CONFIGURATION GUIDE

The Western Digital metal oxide semiconductor chip set that contains the LSI-11 central processor includes one 40-pin control chip, one 40-pin data chip, and two 40-pin microcoded MICROMS (MICROcoded Read-Only Memories) that emulate the PDP-11/40 instruction set. A socket

**Table 2. Comparison of LSI-11 (PDP-11/03) with Competitors**

	Digital LSI-11 (PDP-11/03)	Computer Automation LSI-3/05	GA-16/110	TI 990/4
Word Length, bits	16	16	16/16 + 2 parity/ 16 + 6 EDR	16/16 + 1 parity
Inst Times, $\mu$ sec				
Add	3.5-12.0	6.0	2.5	8.7
Multiply	24-64	No	21.0	21.3
Divide	78	No	20.0	9.3
FI-P Add	42.0	No	Opt	No
FI-P Multiply	52-92	No	Opt	No
FI-P Divide	151	No	Opt	No
Max Memory, bytes	64K	32K	128K	56K
No. of GP Registers	8	8	16	16
Max DMA Rate, bytes/sec	1.7M	1.7M	2M	DMA not supported
Price, \$				
CPU + Memory				
8K bytes	1,536	1,145	1,185	800
32K bytes	3,411	2,650	3,045	2,300
64K bytes	5,911	—	5,525	—
128K bytes	—	—	10,485	—

is provided for an optional fifth chip to implement extended fixed-point and floating-point arithmetic.

The processor contains eight general-purpose registers that can serve as accumulators, index registers, autoincrement registers, autodecrement registers, or as stack pointers for temporary data storage. Only registers 6 and 7 are dedicated. Register 6 serves as the hardware stack pointer and stores the address of the last entry in the stack; register 7 is the program counter and points to the address of the next instruction to be executed. The upper 4,096 addresses are reserved for peripheral device addressing. Memory addresses are in the remaining 0-28K locations with addresses 0-376 reserved for traps and interrupt vector locations. The processor cycle time is 1.2  $\mu$ sec.

I/O transfers can be either Direct Memory Access (DMA) or Programmed I/O (PIO). The transfer rate over DMA is 833K words per second.

Basic memory is a 4K-word MOS RAM, but expansion memory modules are also available: 4K-word core memory, 1K-word static RAM, 4K-word dynamic RAM, and 4K-word PROgramMable Read-Only Memory (PROM/ROM) available in 256- and 512-word increments. Memory cycle time is 350 nanoseconds for RAM and 900 nanoseconds for core.

The microcomputer can support two I/O modules and four expansion serial interface modules. The I/O modules are the DLV11 serial module and the DRV11 parallel module. The processor's main bus can support six devices.

The DLV11 provides for 20mA current-loop or EIA interfaces. Jumper-selectable transmission rates (50 to 9,600 baud) and codes are available. The DLV11 is pin, signal, and software compatible with the DL11C interface available on other PDP-11s.

The DRV11 is a general-purpose, 16-bit parallel interface between the LSI-11 bus and a peripheral device. The

DRV11 is pin, signal, and software compatible with the DR11-C available for the other PDP-11s.

The LSI-11 I/O bus is not compatible with the UNIBUS although it is functionally similar in that I/O device registers are addressed as memory locations. The device located closest to the microcomputer has the highest priority.

Currently, chiefly serial devices, such as a Teletype unit, can interface to the LSI-11. A floppy disc can connect to the parallel interface. Digital will provide more I/O interfaces in the future for other devices such as mass storage units. Table 3 lists peripheral specifications.

**Table 3. Digital Equipment LSI-11 (PDP-11/03): Standard Peripherals**

Device	Description
LA36	DECwriter II, Keyboard Printer; 300 baud (30 cps)
LT33	ASR Teletypewriter; 100 baud (10 cps); paper tape I/O
VT05B	Keyboard CRT; 1,440 char (72 x 20); to 2,400 baud
VT50	DECscope Keyboard CRT; 960 char (80 x 12); to 9,600 baud
RT01	DECLINK Numeric Data Entry Terminal; 4-, 8-, or 12-char display; to 300 baud
RT02A	A/N Data Entry Terminal; 32-char display; to 300 baud
RT02-B	A/N Data Entry Terminal; 32-char display; to 300 baud
DF01-A RXVII	Acoustic Coupler; to 300 baud Floppy Disc; 256K (single drive) or 512K (dual drive)

Initially, the LSI-11 must be program loaded from ROM, from a host computer, or from a mass storage device supplied with a turnkey system. Table 4 lists the configuration restrictions imposed by system software.

# DIGITAL EQUIPMENT CORP. — LSI-11 AND PDP-11/03 SYSTEM REPORT

## COMPATIBILITY

The LSI-11 and PDP-11/03 are generally upward compatible with the PDP-11/35 and up. The instruction sets are nearly identical, except that the LSI-11 and 11/03 have two instructions (that manipulate the processor status word) not found in the 11/35 instruction set. Use of these may require software adjustments when moving up to the 11/35. Conversely, it is possible to use 11/35 software on the 11/03, provided the more limited peripheral environment is suitable to the software.

The LSI-11, and PDP-11/03, however, do not have a UNIBUS, so PDP-11 peripheral devices are not directly compatible.

**Table 4. Digital Equipment LSI-11 (PDP-11/03): Software**

Package	Description
PT11	Paper Tape Operating Package; requires 8K words of memory
RT11	Real-Time Operating System, single-user or foreground/background version; requires 8K words of memory, teleprinter, serial interface, RXVII floppy disc subsystem; F/G requires 12K memory
MACRO II	MACRO Assembler; full version requires 12K words of memory, teleprinter; ASEMBL is abbreviated 8K version
BASIC	Multi-user BASIC, for RT-11; can run on 8K system
FORTTRAN IV	Compiler and run-time system for RT-11, can run on 8K system

## TYPICAL PRICES

Model Number	Description	Purchase Price \$*
<b>PROCESSORS</b>		
KD11-F	LSI-11 Microcomputer Module System (includes CPU, 4K x 16 Random Access Memory, 16-bit I/O port, power fail/auto restart, real-time clock input, automatic priority interrupt arbitration, vectored interrupt handling, 8.5 x 10 in board)	990
KD11-J	Same as KD11-F, except with multiple board configuration of 2 8.5 x 10 in boards	1,536
MRV11-AA	PROM/ROM Memory Unit (includes 31 IC sockets; accepts 256 x 4 or 512 x 4 fusible link memory device and masked ROM device; max capacity to 4K x 16)	175
MSVII-A	1K x 16 Random Access Memory (static RAM)	475
MSVII-B	4K x 16 Random Access Memory (dynamic RAM)	625
MMVII-A	4K x 16 Core Memory	625
<b>Processor Options</b>		
H9270	Backplane Assembly (includes 4-slot module connector with PC card backplane interconnect card guide assembly, screw terminal connector for power and ground) and accepts microcomputer module system plus up to 6 memory and I/O options	175
KEVII	Extended Arithmetic Chip (f-p arithmetic and fl-p arithmetic)	125
MRV11-AC	Fusible Link Unprogrammed PROM Chip (512 x 4 array size)	35
<b>Interfaces</b>		
DRV11	Parallel Interface Unit (includes 16-bit diode clamped input, 16-bit latched drive output, protocol and control signals, one Berg connector for input, one Berg connector for output)	195
DLV11	Serial Interface Unit (optically isolated 20mA current loop or EIA interface levels; selectable baud rates from 50-9,600 baud; selectable stop and data bits)	235
<b>Software</b>		
QJV10-AB	Paper Tape Software Package (includes editor, assembler, loader, debugging package [ODT], input/output exerciser [IOX])	100
QPV10-AE	Emulator Software Package (runs under RT11 on PDP-11/34/40 system; includes editor, assembler, linker, debugging program, load package, save package, execute package)	500
<b>Systems</b>		
	PDP-11V03 System includes:	9,950
	PDP-11/03 with 8K-word RAM	1,997(1)
	RXV11 dual floppy disc	2,496(1)
	Floppy disc bootstrap	192(1)
	LA36 printer	1,392(1)
	VT52 CRT	1,277(1)
	RT11 operating system	420(1)
	MU/11V03 System for one terminal includes LSI-11 CPU with 4K x 16 MOS memory, cabinet, power supply:	16,220(2)
RX11-BX	Dual flexible disc unit	
MSV11-B	4K x 16 MOS add-on memory (6 modules)	
BA11-ME	Expander box and power supply	
KEV11	Extended instruction set/fl-p inst set	
LA36 or VT52	Terminal (console) serial line control — 20mA or EIA (CCITT); can be connected remotely via DFOL interface	
	Three additional terminals can be selected from the following:	
VT50-AA	12-line CRT	1,250
VT52-AA (AB)	24-line CRT	1,995
LA36-CA (CB)	30-cps hard copy	2,175
VT55-AA (AB)	Graphics terminal	2,495
VT55-BA (BB)	Graphics terminal w/hard copy	3,295
<b>Software</b>		
RT11	Operating system	NC
BASIC	Compiler and interpreter	NC
MACRO	Assembler	NC
FORTTRAN IV	Compiler	700

NC = No charge. \* Quantity discounts available. (1) 100-unit quantity. (2) Lease rate/month = \$472.

## DIGITAL EQUIPMENT CORP.

### PDP-11/04 through 11/55 System Report



Digital Equipment Corporation PDP-11 T34 System

#### OVERVIEW

The PDP-11 is Digital's popular 16-bit line, the mainstay of its entire marketing thrust in the minicomputer market and in DECNET configurations. Although it still has not matched the phenomenal number of PDP-8 systems sold, the PDP-11 is the most important of Digital's products because it is the one under the most intensive development. It had a late start, entering the market in 1970 after most other manufacturers had settled on 16-bit architecture as the most practical in the minicomputer sector. The initial system, model 11/20, has since been superseded by a variety of others that now span the entire micro-mini-midcomputer market.

Like most other minicomputer manufacturers, Digital has sold mostly to OEM (Original Equipment Manufacturer) and to "sophisticated" self-reliant end-users. The company has the image of a hardware supplier that provides a variety of software options but not much in the way of software support or tailoring. Digital has undergone a number of changes recently in its marketing stance, reflecting the company's larger size, the development of a sizable software base, and the expansion of marketing forces. Like other minicomputer manufacturers, Digital has built on its existing 16-bit architecture, extending it downward into the microcomputer sector, upward into modified 32-bit versions in the so-called "midcomputer" sector, and outward into a variety of related commercial and industrial packaged systems. In addition, Digital has in-

creased software support; it is now closer to the support offered by the major mainframe manufacturers. At the same time, the usual product reshuffling has provided lower-cost and higher-performance systems using more MOS technology components.

The PDP-11 line, as it now stands, consists of the LSI-11 microcomputer, the 11/03 based on the LSI-11, the "main" PDP-11 models (11/04, 11/05, 11/10, 11/34, 11/35, 11/40, 11/45, and 11/55), and the PDP-11/70 midcomputer. The LSI-11, 11/04, 11/05, and 11/35 are aimed at the OEM market and, thus, are sold in a highly modular fashion, with discounts for quantity. The 11/03, 11/10, 11/34, 11/40, 11/45, 11/55, and 11/70 are packaged systems aimed chiefly at end-users (although 11/45 and 11/70 are sold OEM as well). The LSI-11 and 11/03, and the 11/70 are covered in separate reports because of pronounced differences in architecture, performance, and market orientation. This report covers the main body of the minicomputer systems in the line.

The 11/04 and 11/05 are small, low-cost OEM systems (MOS and core memory systems, respectively); the 11/10 is a small end-user system built around the 11/05. The 11/34 and 11/40 add memory management, dual processor modes, instructions, and other features to allow large, versatile operating systems of many types. Model 35 is the OEM version of the 11/40, while model 34 is a low-cost MOS memory version of the 11/40. The model 11/45 adds several major architectural changes (like a second high-speed memory bus to bipolar or MOS memory), high-speed MOS or bipolar memory with dual ports, and a richer instruction set to allow even greater software sophistication and better performance. The 11/55 is an 11/45 that includes the high-speed 11/70 floating-point processor as an integral feature. Also, Digital will market it with bipolar memory for number-crunching in FORTRAN IV applications programs.

The PDP-11 line has three characteristics that distinguished it from other computers in its class when it was introduced: the UNIBUS, multiple general-purpose registers, and the manner of handling I/O operations. Like many of the newer systems on the market, all current models are microprogrammed. Other manufacturers have since incorporated multiple registers, but most have not

#### HEADQUARTERS

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# DIGITAL EQUIPMENT CORP. — PDP-11/04 THROUGH 11/55 SYSTEM REPORT

copied the UNIBUS concept or I/O handling procedure, probably because they would require software redevelopment.

All PDP-11 models, except the PDP-11/45, are organized around a single fast UNIBUS that connects all system components. The processor, memory, and peripheral devices operate as UNIBUS subsystems; the processor allocates UNIBUS time to system components, which communicate with each other in a master-slave relationship.

The distances between devices and the speeds of the connected devices are immaterial because of the master-slave communications technique. This arrangement means, for example, that memory modules with different speeds can be connected to a system.

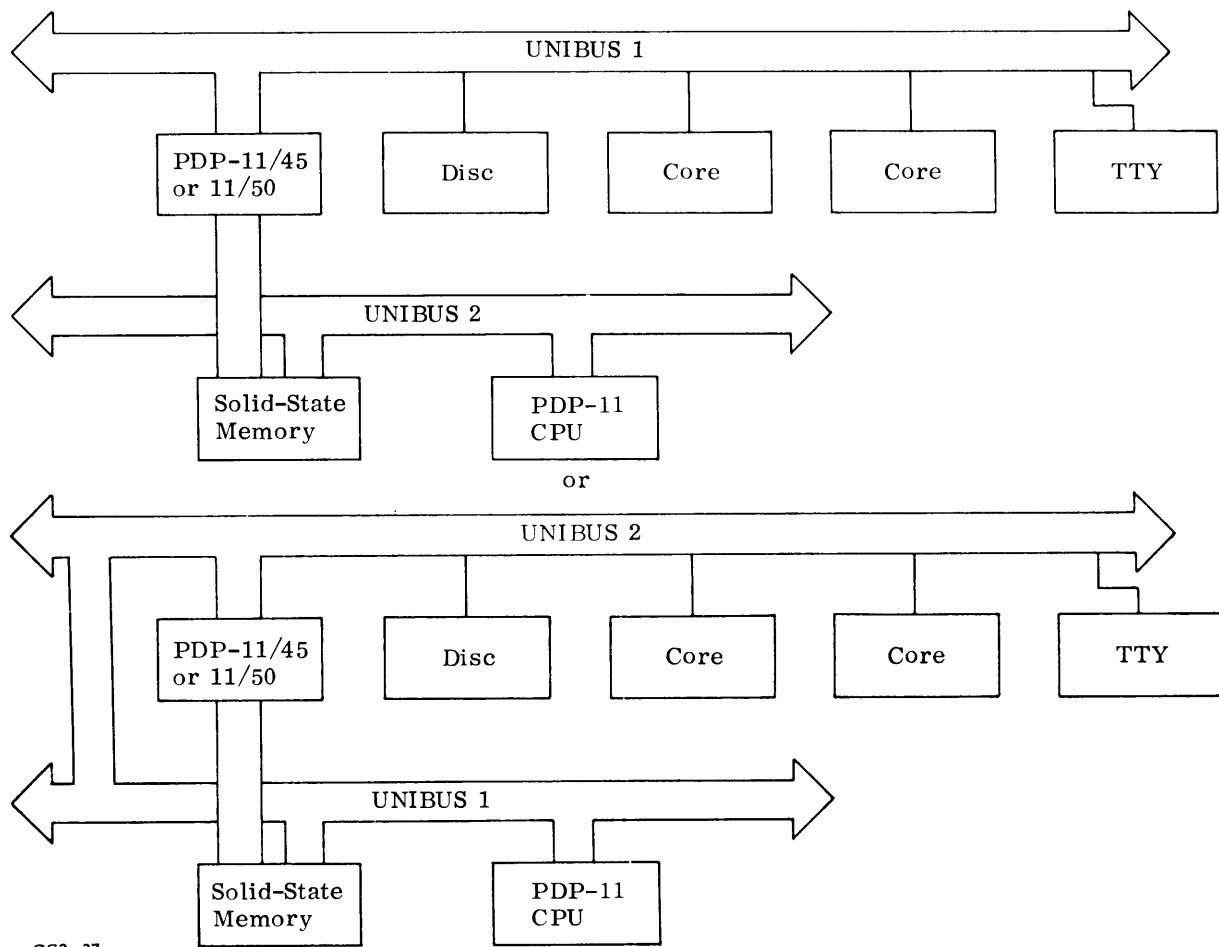
A single UNIBUS inherently limits system speed to that of the UNIBUS because units in the system must time-share it. The PDP-11/45 overcomes this limitation by using a second bus between solid-state memory and the CPU. Also, solid-state memory has two ports of entry; one port

can connect to one CPU, and the other port to a second CPU. Thus, solid-state memory can be shared by two processors (see Figure 1).

The 11/34, 11/35, 11/40, 11/45, and 11/55 can expand memory to 128K words using a memory management option on the 11/34, 11/35, and 11/40, or the memory segmentation option on the 11/45, 11/50, and 11/55. The memory segmentation option is functionally similar to the memory management option although it differs in some respects because of the larger number of registers and processing modes on the 11/45, 11/50, and 11/55. Memory segmentation (or memory management) provides virtual addressing for memories larger than 28K words; it also provides memory protection for multiprogramming environments.

The multiple general-purpose registers and the overall system architecture facilitate stack manipulation. Programming I/O operations is simplified because peripherals are addressed as memory locations, and the entire instruction set can be used on them.

Table 1 lists system specifications common to all models, and Table 2 lists the chief differences among models.



CS2-37

**Figure 1. Digital PDP-11/45, 11/50, and 11/55:  
Use of Multiple Ports to Solid-State Memory**



**Table 1. Digital PDP-11: Characteristics Common to All PDP-11s**

<b>Addressing</b>	
Direct (no. of words)	None (always through internal registers)
Indirect	Yes
Indexed	Yes
<b>INPUT/OUTPUT</b>	
Programmed I/O	Yes
DMA Channels (no.)	1 (any no. of devices) <sup>1</sup>
Multiplexed I/O (no. of sub-channels)	None
<b>MEMORY</b>	
Parity	Option <sup>2</sup>
Basic Addressable Unit	Byte or word
Bytes per Access	1 or 2
<b>DECIMAL ARITHMETIC</b>	No
<b>MICROPROGRAMMED</b>	All current models

Notes:

<sup>1</sup> LSI-11 does not have UNIBUS; PDP-11/70 has four additional high-speed data channels.

<sup>2</sup> Standard on memory modules; checking logic in CPU optional.

Digital provides a comprehensive range of peripherals for its PDP-11 line: conventional paper tape and punched card I/O units including a mark sense card reader; DEC-tape and floppy discs as mass storage for small systems, and industry-standard magnetic tape devices for larger storage requirements; fixed-head disc units and movable-head disc cartridges for larger systems; graphic subsystems; special-purpose subsystems to handle analog/digital, digital/analog, and digital I/O for data acquisition and control applications; and a broad range of communication interfaces for data communications environments.

Software support for the PDP-11 is substantial. Software packages currently offered include a Paper Tape Software System and a Cassette Programming System (CAPS) for small configurations, Resource Time-Sharing System (RSTS), Disc Operating System (DOS), Real-Time Multiprogramming Systems (RSX-11D, M and S), a smaller single-user real-time system (RT-11), a Communications-Oriented Multi-Task Executive (COMTEX-11), and others. Current languages supported are the PAL-11 and MACRO-11, assembly languages, FORTRAN IV, FOCAL, BASIC Plus, and COBOL. These packages support small stand-alone systems, time sharing, batch processing, real-time multiprogramming, communications applications (including 2780 and 2788 emulation for front-end and concentrator configurations), graphics, and laboratory applications.

The recent proliferation of Digital's applications software and hardware/software packages for specific applications has resulted in a many-pronged attack on the end-user market. Increased software support will undoubtedly benefit many existing users, as well as attract new ones.

The PDP-11 is an integral component in DECNET, an overall plan for communication among Digital's computers working together in a network. All PDP-11 systems will support network functions as a host, node, or terminal system.

## PERFORMANCE AND COMPETITIVE POSITION

The minicomputer market changes so rapidly that the relationship of one system to its competitors is extremely variable. An innovative system with a good price/performance can soon be outdated or outpriced. The PDP-11 architecture, so revolutionary when it was introduced in 1970, is now familiar and, although not many manufacturers have imitated it, it has stood the test of time fairly well. The PDP-11 has developed into a major system against which all other minicomputers are compared.

The UNIBUS concept has been useful, particularly for OEM markets, because of the ease of interfacing peripherals and other processors. Other minis that have used this concept are the GRI-909 and the Lockheed SUE. Other manufacturers have not departed from traditional designs to adopt the UNIBUS concept, partly because of the cost of developing new system software but also partly because the UNIBUS becomes overloaded for high I/O data rates. Direct memory access facilities to memory ports, separate from the CPU memory port, can provide high I/O data rates without degrading CPU performance.

As Digital developed the PDP-11 line upward, systems suffered speed and throughput limitations, with everything going over a common universal bus. First, the 11/45 was engineered with a second high-speed channel to MOS and bipolar memory. Then the 11/70 was introduced with both the UNIBUS and four high-speed data channels, as well as a cache memory to increase throughput. Compatibility was maintained, but the PDP-11/70 system was competitive in I/O throughput in the minicomputer market.

The same kind of adjustment to new market demands was made in recent new models introduced at the middle and low end of the line. Minicomputer prices have been dropping as a result of LSI nMOS technology. First, Digital announced the MOS 11/04, a cheaper semiconductor version of the 11/05. Then came the LSI-11, extending the line downward into the microcomputer sector. Recently, Digital added the 11/34, a system with performance equivalent to an 11/40 but with cost reductions of 25 to 30 percent over the 11/40 due to greater use of LSI circuitry. Memory management is a standard feature, not an option. Finally, there is the 11/55, which can support the fast PDP-11/70 floating-point processor. It is a number-crunching system capable of executing FORTRAN IV programs faster than the 11/45.

The PDP-11 is a versatile system, capable of adjusting to a rapidly changing environment. Two months ago, the 11/40 looked expensive in comparison to its competitors. Now there is the competitive 11/34. The same trend of lower price/performance ratios obtains for the 11/04 over the 11/05. The 11/55 lowers the price/performance ratio in another way — performance is enhanced with a new floating-point processor and bipolar memory to fill a market need for a high-speed number cruncher.

# DIGITAL EQUIPMENT CORP. — PDP-11/04 THROUGH 11/55 SYSTEM REPORT

**Table 2. Digital PDP-11: Differences Among PDP-11s**

Model	PDP-11/03	PDP-11/04	PDP-11/05; 11/10	PDP-11/34	PDP-11/35; 11/35F; 11/40	PDP-11/45; 11/50	PDP-11/55	PDP-11/70
<b>ARCHITECTURE</b>								
CPU Models	KD11-J (MOS), KD11-F (core)	KD11-D	KD11-B	KD11-E	KD11-A	KB11-A	KB11-D	KB11-C
Microprogrammed G-P Registers	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Buses	8	8	8	9	9	16	16	16
Automatic Priority Interrupts	I/O, programmed	UNIBUS	UNIBUS	UNIBUS	UNIBUS	UNIBUS + SC memory bus	UNIBUS + SC memory bus	UNIBUS + high-speed data bus
Stack Size	Single line, multilevel	Single line, 4 levels	Multiline, multilevel	Multiline, multilevel	Multiline, multilevel	Multiline, multilevel + 7 software levels	Multiline, multilevel + 7 software levels	Multiline, multilevel + 256 software levels
Floating Point	Fixed	Fixed	Fixed	Fixed std; variable opt	Fixed std; variable opt	Variable	Variable	Variable
<b>MEMORY</b>								
Types	Opt	No	Software	Hardware opt	Hardware opt	Hardware opt	Std <sup>(1)</sup>	Hardware opt
Capacity (words)	MOS, core	MOS	Core	MOS, core	Core	Core, MOS, bipolar	Bipolar <sup>(2)</sup>	Core, bipolar
Min	4K	4K	4K	16K	8K	16K	16K	28K
Max	28K	28K	28K	128K	128K	128K	28K	1M
Increment Sizes (words)	4K	4K, 8K, 16K	8K, 16K	8K (core); 16K (core, MOS); 32K (MOS)	8K; 16K	1K; 4K; 8K; 16K	16K	32K
Management Hardware	No	No	No	Std	Opt	Opt	Opt	Yes, std
Memory Protect Cycle Time (μsec)	No	No	No	Std	Opt	Opt	Opt	Std
Core	0.900	—	0.90, 0.98	0.725	0.90, 0.98	0.90, 0.98	—	1.0
MOS	0.725	0.725	—	0.725	—	0.495	—	—
Bipolar	—	—	—	—	—	0.300	0.300	(Cache) 0.240
<b>INSTRUCTIONS</b>								
Overlapped	No	No	No	Yes	Yes	Yes	Yes	Yes
Extended Arithmetic	Opt	Opt	Opt	Std	Opt	Std	Std	Std
Std Instruction	Basic 11/35 set + 2 added	Basic	Basic	11/40 + EIS	Basic + XOR, SOB, RTT, MARK, SXT	11/40 set + MUL, DIV, ASH, ASHC, SPL	11/4 set + floating point	11/45 (+ floating point opt) in several modes
No. (std; opt)	77	70; 4	70; 4	75; 10	75; 10	83; 50	133	400; 446

— means not applicable.

Notes:

(1) Uses same floating-point processor (FP11-C) as PDP-11/70.

(2) Core and MOS memory can be used on the PDP-11/55, but the system was designed for number crunching and fast FORTRAN program execution; adding slower memory would run counter to this purpose.

Because of the sheer spread of the line from bottom to top, and the large software base, the PDP-11 competes with nearly all minicomputers on the market, and, because of Digital's flexibility in responding to market trends, it competes successfully. The major PDP-11 competitors are the Data General Nova and ECLIPSE; General Automation 16 Series; Honeywell Level 6; Hewlett-Packard 21MX Series; Varian V70 Series; PRIME 100, 200, 300, 400; MODCOMP I, II, and IV; Xerox 530; and Digital's own PDP-8. Hewlett-Packard's powerful HP 3000 competes directly with the PDP-11/45 and 11/55. Other systems compete in specific application areas where they provide strong system support.

The one disadvantage that Digital has in relationship to the large computer manufacturers is that the company still does not lease its computers. This deters some potential users who do not wish to make the total commitment of buying a system. It also means Digital does not have a solid rental base for steady income. So far, this has not thwarted Digital's growth. As the minicomputer manufacturers market to less sophisticated users and to smaller companies, leasing will become more of a competitive factor.

Digital's commitment to distributed processing and networks via DECNET is a wise move. The distributed processing market suits the company's experience and

computers. Digital has a jump on most competitors. Hewlett-Packard has had its 9600/9700 distributed system for a couple of years, but the company has not announced overall networking procedures. MODCOMP has MAXNET, which is not as comprehensive as DECNET. Only IBM with its Systems Network Architecture (SNA) has announced as comprehensive a networking capability.

While IBM is scaling down its hardware required to implement SNA, Digital will be out there implementing small- to medium-size networks. DECNET can be implemented using any number of computers and terminals without requiring a massive host.

## User Reactions

Interviews with several PDP-11 users to get sample responses to the systems produced information on a wide variety of applications since some users have several systems, each used for different purposes. A southern telephone company uses one PDP-11/45 with a 48K-word memory for I/O preprocessing and media conversion to magnetic tape. A second disc-based (300M bytes total) 11/45 polls two computers, which in turn poll 500 terminals for sales and delivery data — also converted to magnetic tape that feeds into a CDC 3301.

A large university laboratory has a disc-based PDP-11/45, a core-based 11/40, and a core-based 11/15, each running different instruments and experiments. The 11/45 is used for program development for the other two, and also to communicate with a CDC 6600.

A large research institution also uses a PDP-11/40 with one disc to tie into the CDC 6600 computer, as well as to run a graphics display. A steel company has two 11/20s and four 11/10s, all used for automatic gauge control on rollers/reversers. A large oil company uses a PDP-11 with 16K words of memory to poll 48 terminals to obtain delivery and service information from all over the country.

Users seem to agree that the PDP-11 CPUs are reliable, and service is prompt. Promptness is variously defined, of course; one user, who is 600 miles from the nearest service center, feels that a 1- or 2-day response time is pretty good. Universally, the CPU is praised for reliability, but some users have found problems with various I/O components that must be adjusted. The steel company, for instance, had some trouble with a power supply that eventually had to be replaced. The steel company does its own maintenance and complains that, under these circumstances, it does not receive news about field engineering changes such as a new power supply.

Users universally feel that the system software is efficient and proves to have no unexpected bugs. One user at the university chemistry laboratory would like to see Digital develop a high-powered time-sharing system that would allow multiple interactive terminals for users to develop and execute programs in FORTRAN or a similar high-level language. A user at the university laboratory

says that the 11/45 hardware could clearly support this type of a system but system software would be needed. The user at the research institute is delighted that the system is considerably more powerful than expected, and has found that it can do more and more of its calculations at the satellite, instead of using the remote CDC 6600 as originally intended.

## Configuration Guide

A PDP-11 system consists of a processor, UNIBUS, memory ranging in size from 4,096 to 28,762 words (126,976 on the 11/34, 11/35, 11/40, and 11/45 and by special order on the other PDP-11 processors), programmer's or operator's console, and peripheral devices. Addresses of the top 4K from the 32K memory words of the basic system are reserved to address I/O device registers.

Minimum system configurations for each of the models are as follows:

- 11/04 — KD11-D CPU, 4K- or 8K-word MOS memory, operator's console, ASCII device control logic, power supply, bootstrap, ROM diagnostics, DMA, 4-level interrupt, 5/4-inch chassis with 14 or 9 slots.
- 11/05 and 11/E05 — KD11-B CPU, 4K- or 8K-word core memory, programmer's console, Teletype control, power fail/auto restart, power supply, line frequency clock, 4-level interrupt system, standard core (900-nanosecond cycle time); Model 11/E05 uses 16K-word core board (980-nanosecond cycle time).
- 11/10 — KD11-B CPU, memory, console, power supply, real-time clock, terminal interface and 5/2-inch assembly for basic configuration; the same features with 16K-word memory, 10.5-inch assembly, DECwriter, RK11D disc, TA11 cassette, and bootstrap loader for larger configurations.
- 11/34 — KD11-E CPU with 4-level interrupt and 32K-word memory (core or MOS), real-time clock, parity, memory management, bootstrap, dual-drive disc pack, dot matrix printer, and terminal.
- 11/35 and 11/35F — KD11-A CPU with 4-level interrupt and 32K-word memory, memory management unit, console, 21-inch chassis, power fail/auto restart, power, OEM diagnostics; prewired slots for clock, extended arithmetic, floating point, and program stack; 11/35F is like 11/35 but with 32K words of 980-nanosecond core modules.
- 11/40 — KD11-A CPU with 4-level interrupt and 8K- or 16K-word memory and console terminal; submodels differ depending on whether memory is 8K or 16K words, whether parity is included, and whether the console terminal is a Teletype, LA30 DECwriter, or VT05 display.
- 11/45 — KB11-A CPU with 4-level interrupt, 16K- or 32K-word core memory or 16K-word MOS memory together with 16K-word core memory, and console terminal; submodels differ depending on whether memory is 16K or 32K words, whether parity or MOS memory is included, and whether terminal is Teletype or LA30 DECwriter; DECwriter version includes clock and bootstrap. An 11/45 with semiconductor memory is called an 11/50.

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- 11/55 — KB11-D CPU with 4-level interrupt, FP11-C floating-point processor, and 16K or 32K words of bipolar memory (300-nanosecond cycle time).

All processors support all of the devices provided for the PDP-11 line, as listed in Table 3. The 11/04 includes a four-slot or nine-slot 5¼-inch chassis. The 11/05 and 11/10 include either a 5¼-inch or a 10½-inch chassis. Larger models use only the larger chassis. The 10½-inch chassis has 20 slots, which can be expanded to 40 slots within the chassis. All PDP-11 systems can also attach one or two external 20-slot bus extensions. The 11/04 and 11/34 were designed as MOS memory systems, but core can be added. Core is located in an external extension chassis in the 11/04, and requires twice the space as for MOS memory.

Models 11/10 and below can expand memory to 28K words. The 11/34, 11/35, 11/40, 11/45, and 11/55 have memory management options allowing memory up to 128K words.

The 11/34, 11/35, and 11/40 processors can support two processor modes with the memory management option and a floating-point arithmetic option, in addition to all the features of the 11/10. The memory management option, which is in most respects similar to the memory management option on the 11/45 and 11/55, allows addressing 128K words of core and provides for programmed memory protection.

PDP-11/45 and 11/55 use a processor that has all the features of the 11/40, plus three processing modes, more internal registers, an internal bus to semiconductor memory, and options for memory management and floating-point arithmetic. They are dual-bus systems. An internal bus connects the central processor to semiconductor (MOS or bipolar) memory modules, and the UNIBUS connects the processor, core memory, and all other system units. All semiconductor memory modules have two ports

**Table 3. Digital PDP-11: Peripherals**

Model No.	Description
<b>Discs</b>	
RJ03/RJ04, RS03/RS04, RK11/RK05	Fixed-head discs — 256K/512K wds/drive; 8 drives/controller
RPR11/RPR03	Moving-head discs — 1.2M wds/pack; 8 drives/controller
RJP04/RP04	Moving-head discs — 20M wds/pack; 8 drives/controller
RX11	Moving-head discs — 3330-type; 44M wds/pack; 8 drives/subsystem
	Floppy discs — single or dual; 256K bytes/diskette
<b>Magnetic Tape</b>	
TC11/TU56	DECtape — 288K char/reel; 4 drives/controller
TA11, TJU16/TU16, TWU16	Dual cassette transport and controller 9-trk magnetic tape system — 800 bpi only or mixed 800 NRZI/1,600 PE; 8 drives/controller
TU10	7-trk/9-trk system — 200, 556, or 800 bpi; 45 ips
<b>Punched Card</b>	
CM11, CR11/CD11-E	Mark sense reader — 40 col; 200 cpm Punched cards — 80 col; 300 or 1,200 cpm respectively

**Table 3. (Contd.)**

Model No.	Description
<b>Printers</b>	
LP11	Line printer series — 170 to 1,200 lpm; 80 to 132 cols; 64 or 96 char
LS11, LV11	Line printer — 60 lpm; 132 cols; 64 char
LA180	Electrostatic printer/plotter — 500 lpm; 120,000 dots/sec DECprinter — 180 cps; dot matrix; 132 cols; 96 char
<b>Paper Tape</b>	
PC11	Reader/punch — 300 cps read; 50 cps punch
PR11	Reader — 300 cps
<b>Teletypewriters</b>	
Teletypes	LT33 & LT35 ASR and KSR units — 10 cps
LA36, RT02, CRT, VT50	DECwriter — 30 cps; local/remote Data entry terminal
VT52	DECscope — 960 (80 x 12) char; local or remote; 75-9,600 baud
VT55	DECscope — 1,920 (80 x 24) char version of VT50
VS60	DECgraphic scope — 1,024 (512 x 256) graphic point version of VT50
	Graphic display — analog, stroke; 1,024 x 1,024 points; 73 x 43 char
<b>Graphic Subsystems</b>	
GT40	VT50, PDP-10, controller, etc., light pen option
GT42	GT40 with larger processor, peripheral expansion capability
GT44	GT42 expanded to stand alone — no host required; can be satellite
VT11	Graphics subsystem with everything but CPU — designed to use existing CPU
EG11	Engineering display subsystem — dot display; 71 x 43 A/N characters; controller
<b>Communications</b>	
DC11	Digital I/O subsystem — 50 to 1,800 baud units
DL11	Full-duplex single serial line interfaces — to 2,400 baud
DJ11, DH11	16-line multiplexor Programmable asynchronous 16-line multiplexor
DV11	Multiple synchronous line MUX — 8 or 16 lines; programmable
DX11, DP11	IBM 360/370 interface Synchronous line module set — full-/half-duplex models up to 40K baud
DU11	Synchronous interface — full-/half-duplex; 9,600 baud
DQ11	Synchronous interface — full-/half-duplex models up to 1.0M baud
DF11	TTL to 20 mA local TTY, or EIA/CCITT voltage
DN11, DC08	System Unit for 4 Bell 801 ACUs
Process I/O, LPS	Telegraph line interface — up to 32 lines
AR11	Laboratory peripheral system — for up to 48 channels of A/D and 8 channels of D/A Analog real-time subsystem — 10-bit compact subset of LPS; limited expansion
ICS/ICR	Industrial control subsystems — local or remote; up to 256 points each



of entry; two processors can share semiconductor memory modules. A PDP-11/45 or 11/55 system can use a mixture of MOS, bipolar, and core memory up to the maximum total memory capacity of 126,976 words.

The 11/45 and 11/55 processors can support two solid-state memory controllers. Each controller can support only one type of memory: up to four 4K-word MOS or bipolar memory modules. Thus, a system can have a maximum of 32K words of MOS or bipolar memory, or 16K words of MOS and 16K words of bipolar memory. The basic 11/45 configuration uses all core memory, but it can use all MOS or a mixture of MOS, core and bipolar. The 11/55 was designed for fast computation using bipolar memory, but it can also support core memory connected to the UNIBUS.

Memory for all PDP-11 models can be read/write or read only. Modules are available in increments of 1K (bipolar), 4K (MOS and bipolar), 8K or 16K (core) words, with only core common to all models. All present core memory modules have a single port of entry, while semiconductor modules for the 11/45 and 11/55 can have two ports. Although any PDP-11 system can support core memory modules with any cycle rate, the memory cycle rates considered standard for the different systems are 900 nanoseconds for 8K-word modules and 980 nanoseconds for 16K-word modules. Parity is now standard on all memory and on all models. The parity option now requires only the parity checking logic board in the CPU.

Software packages may require considerably more than the basic configurations. Table 4 lists configuration requirements for the major software packages. Table 5 lists the DECNET modules that can be incorporated in the various operating systems.

In addition to general configurations, Digital offers hardware/software packages for special applications, which provide savings over using systems configured from a components shopping list. Packages are offered for graphics subsystems, laboratory systems, industrial systems, and communications systems, among others. Some of these are listed in the software table.

## Compatibility

PDP-11 computers based on the UNIBUS are upward compatible, from the PDP-11/04 through the 11/10, 11/20, 11/34, 11/40, to the 11/45, 11/55, and their OEM equivalents. All can use the same peripheral devices and core memory modules, as well as the same instruction and data formats. All use the same basic instruction set; the 11/34, 11/35, 11/40, 11/45, and 11/55 use supersets of the basic instruction set on the 11/10.

The LSI-11 and PDP-11/03 at the low end of the line use a different processor, but have an instruction set that is compatible with that of the 11/34, 11/35 and 11/40, except for two added instructions. They do not have a UNIBUS, however, and have much more limited environments. Because of the environmental limitations, 11/03 software can

be said to be upward compatible with the 11/34, 11/35 and 11/40, rather than the 11/05 or 11/10 (but, as far as the instruction set goes, 11/34, 11/35, and 11/40 programs are downward compatible with the 11/03!). The 11/03 peripherals are not hardware compatible with the major PDP-11 line.

**Table 4. Digital PDP-11: Software**

Package	Description
DOS	Disc operating system; batch package adds job stream processing; requires 8K-wd memory, TTY, disc, DECtape or high-speed paper tape device
RSTS	Time-sharing for up to 16 (RSTS-11) or 32 (RSTS-E) terminals; RSTS-11 requires 20K-wd memory, 256K-wd disc, 2 DECTapes, clock, terminal interfaces; RSTS-E requires 40K-wd memory with parity, larger disc
RT-11	Single-user interactive real-time system for program development in scientific or research environment; requires 8K-wd memory, (foreground/background version requires 16K memory), console terminal, and either dual DECTape, floppy disc, or disc plus paper tape or cassette
RSX-11	Real-time multiprogramming executive in 6 versions, 3 actively marketed; running from 8K-wd core-based or disc-based version with Assembly language support, to full-blown disc-based foreground/background multiprogramming system supporting on-line FORTRAN and COBOL. Configurations vary widely; largest systems require memory management option
IAS	Combines real-time, batch, and time-sharing in foreground/middleground/background system, with extended BASIC and on-line FORTRAN and COBOL; up to 16 time-sharing users, runs on PDP-11/45, 11/50, and 11/55 systems
CAPS-11	Cassette programming system for 4K-wd memory, dual cassette drives, and console terminal
BASIC	Extension of Dartmouth BASIC, language of RSTS and RT-11, also stand-alone version (desk calculator); many versions
FOCAL	Interpreter for small systems in either stand-alone or DOS versions
FORTRAN IV	ANSI standard, batch versions for DOS or on-line versions for RSX-11; FORTRAN IV PLUS version
COBOL	ANSI x 3.23-1974, standard plus extensions; requires PDP-11/40 or larger system with 48K wds of memory, printer, card reader, keyboard/display, and RSX-11D or RSTS/E
Assemblers	Absolute and relocatable PAL-11, stand-alone and DOS, RSTS-11, COMTEX-11, RSX-11 versions
Utilities	Editor, debugger, linker, librarian, loader, and so on
Applications Software and Hardware/Software Packages	MUMPS-11 interpretive data management software; COMTEX-11 communications

**Table 5. Digital PDP-11: System DECNET Functions Implemented**

Function	System/Operating System		System Operating System
	FROM	TO	
Down-Line System Loading	DEC-10/TOPS 10	→	PDP-11 { DAS85 DAS80, 81, 82
	PDP-11 { IAS RSTS/E RSX-11M RSX-11D	→	PDP-11 { TC/D REMOTE/RT-11 RSX-11S RSX-11M
	PDP-11/RT-11	→	PDP-11/Remote
Down-Line Program Loading	PDP-11 { RSX-11D RSX-11M IAS RT-11	→	PDP-11/RSX-11S
		→	PDP-11/Remote
Down-Line Executive Directives	PDP-11 { RSX-11D RSX-11M RSX-11S	→	PDP-11 { RSX-11D RSX-11M RSX-11S
Inter-System File Transfer	DEC-10/TOPS-10	↗	DEC-10/TOPS-10
	PDP-11 { IAS RSTS/E RSX-11D RSX-11M RSX-11S RT-11	→	PDP-11 { IAS RSTS/E RSX-11D RSX-11M RSX-11S RT-11
Remote Job Entry and Terminal Concentration	PDP-11/DAS80, 81, 82	→	DEC-10/TOPS-10
	PDP-11/TC/D	→	PDP-11/RSX-11D
Cross-System Support	PDP-11 { RSX-11M RSX-11D RT-11	→	PDP-11/RSX-11S
		→	PDP-11/TC/D
		→	PDP-11/Remote

The PDP-11 line is, in general, both hardware and software upward compatible with the 11/70 minicomputer. Certain DMA peripherals that interface to the PDP-11/70 high-speed data channels are not compatible with the other PDP-11 processors.

PDP-11 is not compatible with any other computer system.

**MAINTENANCE AND SUPPORT**

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks

outside the large computer companies, both in the United States and worldwide. More than 2,500 engineers man its service staff.

Aside from 56 sales and service locations in the United States, Digital has offices in five Canadian cities, six Australian cities, five German cities, six United Kingdom cities, three Brazilian cities, and one or two cities each in Argentina, Austria, Belgium, Chile, Denmark, Finland, France, India, Israel, Italy, Japan, Mexico, the Netherlands, New Zealand, Norway, Philippines, Puerto Rico, Spain, Sweden, Switzerland, and Venezuela. Although minicomputer manufacturers have traditionally aimed at



somewhat "self-sufficient" users and have thus provided considerably less software support and applications programming assistance than the large systems makers, this picture is changing, as evidenced by Digital's recently added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour periods. An on-site engineer can also be hired if requirements are critical; on the other hand, a user can buy service

on an individual call basis, or set up his own maintenance staff.

An OEM agreement allows discounts up to 44 percent for 100 units of certain classes of hardware/software combinations. The OEM systems, such as PDP-11/04, 11/05, and 11/35, are discounted up to 36 percent for 100-unit quantities. End-user systems, such as PDP-11/45, 11/50, and 11/70, are discounted up to 22 percent for 100-unit quantities. End-user system prices include installation, while OEM prices do not.

## TYPICAL PRICES

Model Number	Description	Purchase Price \$	Monthly Maint. \$
<b>CENTRAL PROCESSOR AND WORKING STORAGE</b>			
PDP-11/04	Computer System with processor, operator's console, bootstrap loader, and 4K MOS	2,475	NA
BA/BB	With 8K memory	3,295	—
PDP-11/05	Computer System (OEM only) with KD11-B Central Processor		
KA/KB*	4K core (space for 8K core and 4 peripheral controllers)	4,395	53
LA/LB*	Same as KA except 8K core (space for 4 peripheral controllers)	4,995	69
NC/ND*	8K core (mounted in 10.5-inch box)	5,995	69
SC/SD*	16K core	7,495	NA
SC/SD*	16K core; 28K chassis	7,495	74
<b>Processor Options</b>			
MM11-K	4K Wd of 16-Bit read/write core memory (900-nsec cycle time)	2,700	20
PDP-11E05	Computer System (OEM only) with KD11-B central processor and 16K core	22,000	246
NE/NF*			
PDP-11/10	Computer System with KD11-B central processor and 8K core	5,995	69
NC/ND*			
SC/SD	With 16K core	7,495	74
XC/XD	With 24K core	8,995	106
YC/YD	With 28K core	9,995	108
KE11-A	Extended arithmetic hardware element (multiply/divide; multiple shifts; normalize)	2,100	11
KE11-B	Hex-mounted extended arithmetic element	1,500	18
KG11-A	Communications arithmetic element	950	6
PDP-11/10	Basic PDP-11/10 with 16K core, DECwriter, line frequency clock, two disc drives, bootstrap loader, and cabinet	22,000	272
NE, NF			
PDP-11/34	Computer System with parity MOS/core memory, memory management, extended instruction set, virtual console, hardware diagnostics, bootstrap loader		
DC/DD	With 16K MOS in 5¼-inch cabinet	9,290	NA
HC/HD	With 16K core in 5¼-inch cabinet	9,290	NA
DH/DJ	With 16K MOS in 10½-inch cabinet	10,490	NA
HH/HJ	With 16K core in 10½-inch cabinet	10,490	NA
	With 32K memory	11,790	NA
	With 64K memory	17,990	NA
PDP-11T34	PDP-11/34 CPU with 32K parity memory, two RK05 disc drives, LA36 DECwriter and control	30,900	NA
PDP-11/35	Computer System (OEM only) with KD11-A central processor and 32K core	20,495	147
FL/FM*			
11/35-SC/SD*	Same as 11/35-FL/FM* except 16K MF11-U memory and 40K chassis	11,495	111
11/35-JE/JF*	Same as 11/35-FL/FM* except 8K ME11-L memory and 56K chassis	9,995	100
11/35-JC/JD*	Same as 11/35-FL/FM* except 8K MM11-S memory and 32K chassis	9,495	101
11/35-JA/JB*	Same as 11/35-FL/FM* except 8K MF11-L memory and 32K chassis	9,495	100
PDP-11/40	Computer System with KD11-A central processor and 16K parity core	16,800	120
BK/BL*			
PDP-11/40	Same as 11/40 BK/BL except 28K parity core	19,500	147
BS/BT			
PDP-11T40	With 32K parity core, LA36 DECwriter and control, line frequency clock, memory management, two DECpack disc drives, bootstrap loader	35,600	293
<b>Options for KD11-A Processor</b>			
KE11-E	Signed integer multiply and divide; extended instruction set (EIS) option	1,400	11
KE11-F	Floating-point processor (4 instructions: multiply, divide, subtract, add; requires KE11-E)	1,500	11
KJ11-A	Stack limit option (permits a soft stack limit violation)	400	5
KT11-D	Memory management option (permits access to 124K wds; includes KJ11-A)	2,480	21
PDP-11/45	Computer System		
BA/BB*	KB11-A Processor with 16K-wd parity core memory console, automatic power-fail/restart, 4-level priority interrupt, hardware multiply/divide, and extended instruction set, DECwriter terminal and control, bootstrap loader, line frequency clock, memory management, OEM basic diagnostics, system schematics, cabinet and power supply	36,000	243
<b>Processor Options</b>			
FP11-B	Floating-Point Processor		
PDP-11/50	Same as PDP-11/45 except with MOS memory	5,600	45
FK/FL	With 16K memory		
FH/FS	With 16K parity memory	32,000	334
FU/FV	With 16K MOS and 16K core	33,000	334
FS/FT	With 16K MOS and 16K parity core	35,000	398
BW/BY	With 16K MOS and 18K parity core	35,500	393
BS/BT	With 32K parity MOS	36,000	397
		40,000	551

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## TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price \$	Monthly Maint. \$
<b>Processor Options</b>			
PDP-11/55	Same as for PDP-11/45 Solid-state version of PDP-11/45 with bipolar memory, memory management, clock, bootstrap loader		
BC/BD	With 16K memory	42,000	302
BA/BB	With 32K memory	48,000	360
PDP-11T55	PDP-11/55 CPU with 32K memory, two (RK05) disc-pack drives, LA36 DECwriter, FP11-C floating-point processor	67,000	NA
BA/BB			
BC/BD	With 16K bipolar and 16K core	61,000	NA
<b>Processor Options</b>			
FP11-C	Floating-Point Processor	5,900	NA
<b>Options for Any PDP-11 Processor</b>			
KG11-A	Communications Arithmetic Element	950	6
KE11-B	Extended Arithmetic Hardware Element	1,500	18
KW11-L	Line Frequency Real-Time Clock	350	5
KW11-P	Programmable Real-Time Clock	700	6
<b>Memory for All PDP-11 Processors</b>			
ME11LA/LB*	Memory system (16-bit read/write; 900-nsec core; rack mountable; power supply; first 8K increment)	5,200	37
MF11-L	8K words of 16-bit read/write core memory (900-nsec cycle time; expandable to 24K in 8K or 12K increments)	4,700	37
MM11-L	8K-word expander for ME11-LA or MF11-LB	4,400	37
MM11-LK	12K-word expander for MF11-L or ME11-L	7,100	58
MM11-S	8K-word core memory and control (900-nsec cycle time)	4,700	38
MF11-U	16K-word core memory and control with expansion capability to 32K (980-nsec cycle time)	4,900	32
MM11-U	16K-word expander core memory (980-nsec cycle time; MF11-U reqd)	4,500	32
MF11-UP	16K-word parity core memory and control with expansion capability to 32K (980-nsec cycle time)	6,300	27
MM11-UP	16K-word parity core memory expander (980-nsec cycle time; MF11-UP reqd)	5,600	27
FM11-U	Conversion kit (to add 16K memory capability)	1,000	—
<b>Memory for 11/40 and 11/45</b>			
MF11-LP	8K-word parity core memory	5,700	32
MM11-LP	8K-word expander parity core memory	5,400	32
<b>Semiconductor Memory for 11/45 and 11/50</b>			
MS11-CC	Bipolar memory control	1,950	13
BC	First MOS memory control	1,950	13
BD	Second MOS memory control	1,500	13
MS11-CM	1K-word bipolar memory (300-nsec cycle time)	1,950	16
CP	1K-word bipolar memory (byte parity; 300-nsec cycle time)	2,500	16
BR	4K-word MOS memory (495-nsec cycle time)	3,000	42
BT	4-K word MOS memory (byte parity; 495-nsec time)	3,400	42
<b>Graphic Systems</b>			
GT40AA/AB*	Computer-based PDP-11/10 Graphic Terminal System	14,500	186
GT40AC/AD*	Same as GT40-AA/AB but ASR33 replaces keyboard	15,720	223
GT40AE/AF*	Same as GT40-AA/AB but LA30 DECwriter replaces keyboard	16,795	217
GT42AA/AB*	Computer-Based Graphic Terminal System	17,500	151
GT42AC/AD*	Same as GT42-AA/AB but ASR33 replaces keyboard	18,720	181
GT44AE/AF*	Same as GT42-AA/AB but LA30 DECwriter replaces keyboard	19,795	176
GT42AA/AB*	Graphic Display Standard System	34,500	424
BM873-YA	Restart/Loader	400	1
MR11-DB	64-Word Bulk Storage Bootstrap Loader	700	5
<b>MASS STORAGE</b>			
<b>Fixed-Head Discs</b>			
RC11-A/B*	64K-word fixed-head disc drive and controller (for up to RS64 drives)	8,300	37
RS64-A/B*	64K-word DECdisc fixed-head drive (16 $\mu$ sec/word transfer rate; 17-msec avg access time)	5,500	16
RF11	256K-word disc drive and controller (for up to 8 RS11 discs; includes cabinet)	16,650	69
AA/BB*			
RS11/RS11-A*	256K-word fixed-head disc drive (16 $\mu$ sec/word transfer rate; 17-msec avg access time)	10,700	40
RJS03	256K-word disc drive and controller (for up to 8 RS03 or RS04 drives; 4 or 8 $\mu$ sec/word transfer rate; 8.5-msec avg access time; includes cabinet with space for 2 additional drives)	14,000	75
BA/BD*			
RJS04	512K-word disc drive and controller (expands up to 8 RS03 or RS04 drives; includes cabinet with space for up to 2 additional drives)	18,000	85
BA/BD*			
RS03	256K-word disc drive (4 or 8 $\mu$ sec/word transfer rate, 8.5-msec avg access time)	9,000	48
AA/AD*			
RS04	512K-word disc drive (4 $\mu$ sec/word transfer rate, 8.5-msec avg access time)	13,000	58
<b>Removable Discs</b>			
RK11-DE/DJ*	1.2M-word disc cartridge drive (expandable to 8 RK05 DECpack disc drives; cabinet includes space for 3 additional RK05s)	11,000	106
RK05-AA/BB*	1.2M-word DECpack moving head disc cartridge drive (11.08 $\mu$ sec/word transfer rate; 70-msec avg seek time)	5,100	64
RK05K-11	Cartridge for RK05	99	—
RP11	20-word disc pack drive and controller (expandable to 8 RP03s)	31,880	233
CE/CJ*			



**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
RP03 AS/BB*	20M-word moving-head disc drive (7.5 $\mu$ sec/word transfer rate; 29-msec avg access time)	20,000	159
RP02-P	Disc pack for RP03 (20M wds)	295	—
KW11-L	<b>INPUT/OUTPUT</b> Real-time clock (line frequency; causes interrupt every 16.6 msec [60 Hz] or 20 msec [50 Hz])	300	3
KW11-P	Programmable real-time clock	700	6
LT33	Teletype ASR 33 (with paper tape reader/punch; 10 cps)	1,850	37
DC/DD* CC/CD	Teletype KSR 33	1,400	32
LT35	Teletype ASR 35 (with paper tape reader/punch; 10 cps)	4,860	32
DC/DD* CC/DD*	Teletype KSR 35	3,240	29
LC11-A	Controller for data terminal LA30-P	500	6
LA30	DECwriter data terminal	2,795	32
PA/PD* CA/CD*	Same as LA30-PA except serial 20 ma current loop; switch selectable 110, 150, or 300 baud	3,195	32
EA/ED*	Serial DECwriter word copy terminal	3,195	30
PC11-A*	High-speed paper tape reader (300 cps) and punch (50 cps) with control	3,900	38
PR11	High-speed paper tape reader (300 cps) with control	2,400	22
H-722	Transformer (required for 230 V operation of PC11, PR11)	100	—
CM11/ CM11-A*	Mark-sense card reader (40 col; 200 cpm)	5,290	50
CR11/ CR11-A*	Card reader (80 col; 300 cpm; tabletop model)	4,860	53
CD11-B/ CD11-A*	Same as CR11 except 1,000 cpm; with DMA interface	10,800	74
CD11- EA/EB*	Card reader (80 col; 1,200 cpm)	15,120	95
CM11- FA/FB*	Mark sense and punched card reader (285 cpm; includes control unit)	5,290	53
LP11	Line printer (300 lpm; includes control logic)		
FA/FB*	(80-col, 64 char; 350 lpm)	12,000	60
HA/HB*	(80-col, 96 char; 250 lpm)	13,500	65
JA/JB*	(132-col, 64 char; 240 lpm)	17,500	75
KA/KB*	(132-col, 96-char; 170 lpm)	19,000	80
RA/RB*	Same as LP11-JA except 1,200 lpm; heavy duty	30,000	154
SA/SB*	Same as LP11-KA except 900 lpm; heavy duty	33,000	154
VA/VD*	132-col, 64-char printer and control unit (300 lpm)	9,900	72
WA/WD*	132-col, 96-char printer and control unit (230 lpm)	11,900	72
LS11-A,B*	132-col, 64-char (60 lpm)	5,615	48
LV11- BA/BB	Electrostatic printer/plotter and controller; 132-col, 96 char; 500 lpm, 120,000 dots/sec	11,770	50
TC11- GA/GB*	DECTape transport and controller (for up to 4 TU56 transports; includes cabinet; 288K char/reel)	9,500	45
TU56	Dual DECTape transport (288K char/reel)	5,100	32
TU10	Industry-compatible tape (1/2-in. tape; 800 bpi; 45 ips; 7-channel model has provision for program-selectable 556 and 200 bpi; up to 7 slave units can be added to each master and control; cabinet included)		
TM11-EA/ ED*	9-track master (1st unit)	10,745	101
TU10-EE/ EJ*	9-track slave	7,505	74
TM11-FA/ FD*	7-track master (1st unit)	12,500	101
TU10-FE/ FJ*	7-track slave	7,505	74
TA11- AA/BB*	Dual cassette transport and controller	2,990	38
TU60-K	Cassette (150 ft.; 90,000 char)	7	—
AA11-A	Control for VT01-A Scope (requires AA11-D and 2 BA614s)	645	2
B	Control for scope (requires AA11-D and 2 BA614s)	645	2
C	Control for VR14 Scope (requires AA11-D and 2 BA614s)	645	2
VT01-A	Tektronix 611 storage tube display	3,240	80
VR01-A	Tektronix RM503 oscilloscope display	1,080	15
VR14/ VR14-A*	Point-plot display (7 x 9 in.)	3,240	19
VT05B- AA/AD* BA/BD*	CRT display (A/N; with keyboard; half/full-duplex; 64/96-char set; 20 lines, 72 char/line; TTY compatible; 110, 150 or 300 baud; requires DC11; no parity)	2,795	23
VT05B- CA/CB* DA/DB*	CRT display (A/N; parity; 64/96-char keyboard; DF01-A or Bell 103 equivalent reqd; BC05-D cable reqd)	2,795	23
VT11-AA/ AB*	Display processor with 17-in. CRT and light pen	9,500	250
<b>DATA COMMUNICATIONS</b>			
DC11-AA	Dual asynchronous serial line system unit and clock (for mounting 2 DC11-DA modules; 110, 134.5, 150, or 300 bps; typical 103 modem speeds program selectable)	350	3
DC11-DA	Full-duplex serial module set for DC11A (5-, 6-, 7-, or 8-bit codes; EIA/CCITT termination for direct use with 103 or 202 modem)	700	7
H312A	Asynchronous null modem (allows direct connection of peripherals with EIA 232 interface with a DC11)	85	2

# DIGITAL EQUIPMENT CORP. — PDP-11/04 THROUGH 11/55 SYSTEM REPORT

## TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price \$	Monthly Maint. \$
DL-11A	Full-duplex single serial line interface (replaces KL11; customer specifies speed group 1 [110 baud] or 3 [50, 75, 150, 300, 600, 1,200, 1,800, and 2,400 baud]; for DEC-supplied TTY or VT05)	500	6
DJ11-AA	Asynchronous 16-line multiplexor for EIA/CCITT terminals or lines	3,400	32
DJ11-AB	Asynchronous 16-line multiplexor for use with external signal conditioning equipment	3,100	27
DJ11-AC	Asynchronous 16-line multiplexor for 20mA level conversion	3,200	32
DH11-AA/AC	Programmable asynchronous 16-line multiplexor and mounting panel with space for up to 4 DM11 line adapters (16 lines)	4,400	32
DH11-AB	Programmable asynchronous 16-line multiplexor with data cable for connection to DC08 telegraph line interface	4,200	29
DM11-BB	Modem control multiplexor	1,295	19
DM11-DA	Line adapter for 4 20mA terminals	170	5
DM11-DB	Line adapter (4 EIA lines; includes four 25-ft modem cables)	485	5
DM11-DC	Line conditioning	860	11
DP11-DA	Synchronous line module set and system unit	1,700	19
CA	Data/sync register extender	400	3
KA	Internal clock	300	3
DP11-DC	Same as DP11-DA, only suitable with direct use with 303 modems; includes 25-ft cable	2,100	19
DU11-DA	Full/half-duplex synchronous interface, data set control included	900	5
DQ11-DA	Full/half-duplex NPR synchronous interface with programmable transmission speeds up to 10,000 baud	2,800	24
DQ11-EA	Full/half-duplex synchronous NPR interface to Bell System 303 or equivalent modems	4,200	25
DQ11-KA	Crystal clock option	150	1
DC08-CS	Telegraph line Interfaces (not for 11/45) Interface Panel (up to 16 DC08-CM dual-line adapters)	2,160	4
CM	1 dual telegraph terminal and receive line adapter	230	2
EB	Telegraph line current adjustment panel	2,160	2
D	Distribution panel	1,080	2
793	Power supply	540	7
893	Fuse panel	1,080	—
H316-A,B*	Dual telegraph line interface for 2 common carriers on private telegraph circuits	1,000	3
DR11-B	General-purpose direct memory access interface	1,400	13
<b>LABORATORY AND SCIENTIFIC SYSTEMS</b>			
PDP-11E10-NE/NF*	Disc Operating System with PDP-11/10	24,000	285
DECLAB 11/10-A	LAB System with ASR-33 terminal	11,495	131
DECLAB 11/10-B	LAB System with DECwriter and 10-bit A/D	15,585	159
DECLAB 11/10-C	LAB System with DECwriter and 12-bit A/D	18,385	191
DECLAB 11/10-D	LAB System with DECwriter; uses Foreground/Background Operating System	26,750	265
DECLAB 11/10E	LAB System with 1.2M-wd disc cartridge drive and control	29,550	297
DECLAB 11/40-AA/AB*	LAB System with PDP-11/40 CPU	37,500	494
RSX-11D System #1	Real-time system executive system with PDP-11/50	111,100	886
RSX-11D System #2	Real-time executive system with PDP-11/40	52,525	444
RSX-11D System #3	Same as System #2 except for RK05 disc cartridge drive instead of TM11 magtape unit	46,880	407
RT-11 System #4	Real-time system with PDP-11/50	57,505	557
RT-11 System #5	Real-time system (same as system #4 except for RK05-AA/BB* disc cartridge drive instead of TM11 magtape)	51,860	520
RT-11 System #6	Real-time system with PDP-11/45	49,505	401
RT-11 System #7	Real-time system (same as System #6 except RK05-AA/BB* disc cartridge drive instead of TM11 magtape)	43,860	364
RT-11 System #8	Real-time system with PDP-11/40	38,945	345
Recommended software:			
RT-11 System #9	RT-11 monitor and system programs, Dartmouth BASIC, and ANSI Std FORTRAN IV	33,050	306
Real-time system (same as System #9 except BM792-YB disc/DECtape bootstrap loader and RK05AA/BB disc cartridge drive instead of TM11 magtape)			
DOS/BATCH System #4	DOS/BATCH Operating System and ANSI Std FORTRAN IV	57,505	557
DOS/BATCH System #5	DOS/Batch System with PDP-11/50	51,860	520
DOS/BATCH System #6	DOS/Batch System (same as System #4 except RK05-AA/BB* disc cartridge drive)	49,505	401
DOS/BATCH System #7	DOS/Batch System (same as System #4 except with 11/45-CU/CV CPU)	49,505	401
DOS/BATCH System #8	DOS/Batch System (same as System #6 except RK05-AA/BB* disc cartridge drive)	43,860	364
DOS/BATCH System #9	DOS/Batch (same as RT-11 System #8 but with recommended software: DOS/BATCH operating system and ANSI Std FORTRAN IV)	38,945	345
DOS/BATCH System #10	DOS/Batch System (same as RT-11 System #9 but with recommended software: DOS/BATCH operating system and ANSI Std FORTRAN IV)	330,050	306
CAPS-11 System #10	Cassette Programming System with PDP-11/10	12,335	147



**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
CAPS-11 System #11	Cassette Programming System with PDP-11/40	19,200	185
MUMPS-11 System #12	Recommended software: Dartmouth BASIC/PTS MUMPS-11 software package, with 11/45	80,195	580
MUMPS-11 System #13	MUMPS-11 software package with 11/40	45,145	386
PHA-11 System #14	Pulse Height Analysis System with PDP-11/40	52,920	456
PHA-11 System #15	Pulse Height Analysis System on PDP-11E10	32,500	330
GAMMA-11 BM11-HA/HB*	Nuclear Medicine System on PDP-11/40	56,500	442
11/45-RP/RR*	RSTS/E Timesharing Systems on PDP-11/45; with dual DECtape and cartridge disc storage; expandable	83,670	485
11/45-RS/RT*	Same as 11/45 RP/RR except industry std 9-track magnetic tape instead of DECtape unit	85,715	538
11/45-RU/RV*	Same as 11/45 RS/RT except with floating point processor and 20M-wd disc pack unit	97,485	635
RSX-11D 11/45-NA/NB*	Real-Time Operating System on PDP-11/45	64,315	433
11/45-NC/ND	Same as 11/45-NA/NB* except with additional 16K parity core memory and H960-D extension mounting cabinet with PDP-11/45 and simultaneous background batch processing	73,015	473
11/45-NE/NF		122,040	743
11/45-NH/NJ	Same as 11/45 NH/NJ except with RK05 DECpack disc drive and no mag tape unit	67,370	438
11/45-PS/PT	Batch Processing System on PDP-11/45	51,205	378
11/45-PU/PV	Same as 11/45 PS/PT except with RF11-A 262K fixed-head disc unit and TC11 DECtape unit instead of RK11-D DECpack disc unit and TM11-E mag tape unit	52,560	290
11/50-NA/NB	Batch Processing System on PDP-11/50	73,015	580
11/50-NC/ND	Same as 11/50-NA/NB* except additional 16K parity core memory	78,615	605
11/50-NE/NF*	High-performance PDP-11/50-based real-time system with simultaneous background batch processing	153,500	990
11/50-NH/NJ*	Same as 11/50-NC/ND* except 1.2M-word DECpack instead of mag tape unit	72,970	570
11/50-PS/PT*	Batch Processing System on PDP-11/50	59,205	525
11/50-PU/PV	Same as 11/50 PS-PT except RF11-A 262K fixed-head disc unit and TC11-G DECtape unit instead of RK11-D DECpack disc unit and TM11-E mag tape unit	60,560	437
11/50-PW/PY	Batch Processing System on PDP-11/50 with high-speed card reader and line printer, floating-point hardware, industry std mag tape and 20M-word disc pack storage	137,980	1,004
11/50-RP/RR	48K 11/50-based timesharing system on PDP-11/50 with dual DECtape and cartridge disc storage; expandable to 32 simultaneous users	92,370	632
11/50-RS/RT	Same as 11/50-RP/RR except TM11-E mag tape unit instead of TC11-G DECtape unit	94,415	685
11/50-RU/RV	Timesharing system on PDP-11/50 with 20M-wd disc pack storage, hardware floating-point processing, industry std mag tape expandable to 32 users	106,185	782

Notes:

- \* Starred submodel is 230V, 50/60 Hz version; unstarred submodel is 115V, 50/60 Hz version; some components are also available for 47 to 420 Hz.
- (1) Digital does not rent equipment.
- (2) Contact Digital in Maynard MA.
- (3) Maximum total memory is 128K; system allowed max of 2 solid-state memory controllers. OEM models available for most equipment.
- Not Applicable      NA—Not Available



## DIGITAL EQUIPMENT CORP.

### PDP-11/04 Through 11/55 System Report Update

#### New Software Package

The Record Management Services (RMS-11) software provides keyed-access record and file management for any PDP-11/04 through 11/55 systems that supports the RSTS/E (Resources Sharing/Time Sharing/Extended) operating system. RMS-11 consists of utility programs for creating and maintaining sequential, relative, or indexed files, and operating system routines for transmitting fixed- or variable-length records to and from user programs.

With RMS-11, files can be organized and reorganized without presorting, and data can be accessed by either physical location or logical organization. RMS-11 also handles multi-level searches (both generic and approximate) and provides privacy control for multi-user environments. RMS-11 supports features of ANS-74 COBOL; this provides compatibility across systems and a growth path to full data base management.

The RMS-11 software is licensed at \$2,500 and will be available by the end of 1976.

#### New BASIC Compiler

BASIC-PLUS-2, Digital's newest compiler, extends the capabilities of previous BASIC compilers. It will be available for all PDP-11/04 through 11/55 systems that run under the RSTS/E, RSX-11M, or IAS operating systems.

BASIC-PLUS-2 incorporates new record I/O facilities (including sequential and relative file organization), code optimizations, a CALL statement, variable names of up to 30 characters, and comprehensive debugging facilities; it is upward compatible with the BASIC-11 and BASIC-PLUS compilers previously offered by Digital. A multi-keyed ISAM (Indexed Sequential Access Management) option is available.

BASIC-PLUS-2 will be available for RSTS/E in January 1977 and for RSX-11M and IAS in March 1977. It will be licensed to new users at \$4,000 and to upgrading users at \$2,500, including on-site installation and field software support.

#### Communication Interfaces

Digital now offers three new communication interfaces for PDP-11 systems: DMC11 is a single-line high-speed

synchronous interface, DPU11 a single-line multiprotocol synchronous interface, and DZ11 a low-cost asynchronous eight- or 16-line multiplexor.

DMC11 provides high-speed linkage between PDP-11s using Digital's Data Communication Message Protocol (DDCMP). DMC11 incorporates a high-speed microprocessor that handles DDCMP functions. DMC11 can operate locally over coaxial cables at 56K to 1M bits per second, or (by further interfacing to asynchronous modems) over common carrier lines at 19.2K bits per second. The DMC11 hardware protocol provides message formatting, header processing, and message acknowledgment and retransmission. The DMC11 interface is priced from \$2,145; deliveries began in September 1976.

The DPU11 interface can handle several protocols including DDCMP, SDLC, HDLC and bisync. DPU11 operates with synchronous modems at speeds up to 9,600 bits per second. DPU11 hardware performs zero-bit insertion and deletion, flag and abort generation and detection, frame checks for SDLC and HDLC protocols, and cyclic redundancy checks for DDCMP. The DPU11 interface is available 30 days after order and is priced at \$1,375.

The DZ11 multiplexor connects eight or 16 local or remote asynchronous terminals or modems to PDP-11 computers, allowing both format and line speed to be programmed on a per-line basis at up to 9,600 baud. Input is by character in a 64-entry first-in-first-out buffer; output is double-character buffered. An eight-line DZ11 model is available for \$2,100 and a 16-line DZ11 is available for \$3,400 in EIA or 20-MA versions.

#### Double-Density Disc Drive

RK05F is a double-density disc drive that Digital has developed for PDP-11 systems. The RK05F, which is nonremovable, is really two logical drives working as one to provide 2.5M words of storage. Data transfer rate is 180K bits per second.

The new drive will cost \$6,500. At the time of this writing, exact delivery dates were unannounced.



# DIGITAL EQUIPMENT

## PDP-11/70 System Report



### OVERVIEW

The PDP-11/70 is Digital Equipment's PDP-11 compatible system designed to compete in the new "midcomputer" marketplace. Many aspects of the 11/70 system architecture resemble that of the 11/45, but the 11/70 has expanded maximum memory capacity and reorganized I/O structure; it incorporates a high-speed cache memory. Digital has added important new software to implement a system with three times the throughput speed of the 11/45; the 11/70 can operate in a multi-user, multi-language, multi-function environment. It solves the throughput problems associated with traffic on the UNIBUS experienced with larger 11/45 configurations. The PDP-11/70 competes with the Data General Eclipse, Interdata 8/32 Megamini, Modcomp IV and Prime 300. All these systems provide real-time interactive capabilities that rival many small scale batch systems in size, speed and scope, at prices drastically lower than those charged by the larger mainframe computer makers.

The PDP-11/70 still uses a 16-bit word, but internal busses are 32 bits wide. A memory management unit and a high-speed cache memory also help achieve high performance. The 32-bit busses are used to transfer data between main memory and cache memory and between main memory and certain high-speed mass memory controllers for moving-head discs, fixed-head discs and magnetic tape drives. This relieves the UNIBUS of traffic for transfers between mass storage device controllers and main memory, although the same discs used on other PDP-11 systems can still be attached to the UNIBUS. Cache memory, a 2,048-byte high-speed bipolar memory that stores a replica of selected portions of main memory, significantly reduces most memory access times. Cache

also controls high-speed transfers between memory and the UNIBUS, memory and CPU, and memory and the four high speed controllers, so that all can operate virtually simultaneously. The management unit, a standard 11/70 feature, increases memory addressing to 4M bytes by adding six addressing bits to produce a 22-bit address. Despite the addressing capability, Digital currently limits memory capacity to 2M bytes. Memory mapping on the 11/70 does not increase instruction execution times.

Cache memory increases system throughput because programs tend to access instructions in sequential order or in small loops and to access data sequentially. Cache stores not only the current instruction or data word but also the next 16-bit word in sequence. This provides a look-ahead feature. Data and instructions remain in cache until they are replaced by a more recently accessed word. This provides a look-back feature. Digital's test indicate the "hit" rate for finding an addressed word in cache is between 90 and 95 percent. This high rate is due to the algorithm for storing and saving data, and to the size of the cache. The cache produces an effective memory cycle time of less than 400 nanoseconds per 16-bit word, while the memory cycle time is 1.0 microsecond.

The 32-bit wide busses are used between cache and main memory and between main memory and the special high-speed data channel controllers used on the 11/70. Data transfers between the CPU and cache are over a 16-bit wide bus, and transfers between the high-speed controllers and mass storage devices or other peripherals are also 16 bits wide. The memory management unit and the UNIBUS mapping unit, which are transparent, code and decode addresses so that the correct 16 bits, 18 bits, 22 bits, 32 bits, or 36 bits (4 bytes plus 4 bits of parity) are sent or received by the appropriate portion of the processor.

The PDP-11/70 is completely compatible with the rest of the PDP-11 line. The central processor generates 16-bit addresses, but the UNIBUS carries 18-bit addresses, the same as other PDP-11s. All peripherals available for other



### HEADQUARTERS

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## DIGITAL EQUIPMENT — PDP-11/70 SYSTEM REPORT

PDP-11 systems can be attached to the 11/70 UNIBUS, and all programs written for comparable configurations can be run on the 11/70. New high-speed controllers that attach to the 32-bit wide bus are used only on the 11/70.

Table 1 compares the characteristics of the PDP-11 mainframes.

Both the RSTS/E and the RSX-11D operating systems from the 11/45 will run on the 11/70.

The PDP-11/70 RSTS/E (Resources Timesharing System/Extended) supports 63 users employing the extended BASIC Interpreter in the foreground with an ANSI 74 COBOL-11 program in the background. (A special feature called "SCOBOL" allows terminals to access the COBOL compiler via BASIC PLUS. Each terminal that accesses COBOL requires 20K words of memory.)

The RSX-11D operating system is for dedicated real-time systems; it supports FORTRAN IV and FORTRAN IV PLUS, an optimizing compiler. In addition, a new multi-user, multi-language, multi-function operating system called the Interactive Application System (IAS) is scheduled for delivery in November 1975. IAS is currently operating at two or three sites. It will handle multi-language timesharing and batch processing concurrently with limited real-time processing. IAS supports FORTRAN IV, FORTRAN IV PLUS, BASIC, COBOL, and MACRO (assembler).

Digital expects to market the PDP-11/70 to all of its usual markets for industrial business, communications, OEM, laboratory, education, computation, and typesetting applications. Digital spokesmen indicated they expect the PDP-11/70 to outsell the PDP-11/45. To date, more than 2,000 PDP-11/45 systems have been sold. Digital

**Table 1. Specifications of PDP-11 Computers Compared**

Model	PDP-11/04; 11/E05; 11/05; 11/10	PDP-11/15; 11/20; 11/R20	PDP-11/35; 11/35F; 11/40	PDP-11/45; 11/50	PDP-11/70
<b>ARCHITECTURE</b>					
Microprogrammed	Yes	No	Yes	Yes	Yes
G-P Registers	8	8	9	16	
Buses	UNIBUS	UNIBUS	UNIBUS	UNIBUS + semi-conductor Memory bus	UNIBUS + high-speed data bus
Automatic Priority Interrupts	Multi-line, multi-level	Single-line, multi-level	Multi-line, multi-level	Multi-line, multi-level + 7 software levels	Multi-line, multi-level + 256 software levels
Stack Size	Fixed	Fixed	Fixed std; variable opt	Variable	Variable
Floating Point	Software	Software	Hardware opt	Hardware opt	Hardware opt
<b>MEMORY</b>					
Types	Core (11/05, 11/10); MOS (11/04)	Core	Core	Core/MOS/bipolar	Core
Capacity (words)					
Min(1)	4,096	4,096	8,192	16,384	28,672
Max(1)	28,672	28,672	126,976	126,976	1M
Increment Sizes (words)	8,192; 16,384	8,192; 16,384	8,192; 16,384	1,024; 4,096; 8,192; 16,384	32,568
<b>MEMORY</b>					
Management Hardware	No	No	Yes, opt	Yes, opt	Yes, std
Memory Protect	No	No	Opt	Opt	Std
Cycle Time ( $\mu$ sec)					
Core	0.90, 0.98	0.90	0.90, 0.98	0.90, 0.98	1.0
MOS	0.725 (11/04 only)	—	—	0.495	—
Bipolar	—	—	—	0.300	(cache) 0.240
<b>INSTRUCTIONS</b>					
Overlapped	No	No	Yes	Yes	Yes
Extended Arithmetic	Opt	Opt	Opt	Std	Std
Std Instruction	Basic	Basic	Basic + XOR, SOB, RTT, MARK, SXT	11/40 set + MUL, DIV, ASH, ASHC, SPL	11/45( + floating point opt) in several modes
No. (std; opt)	70; 4	70;4	70; 10	83; 50	400; 446

Note:

(1) Excluding 4,096 physical words reserved for UNIBUS mapping.



Equipment is the leading minicomputer manufacturer, with sales and service offices in 46 cities in the United States, and 24 countries outside the United States. The 11/70 undoubtedly will be an important system to watch in the developing "midcomputer" market.

## COMPETITIVE POSITION

The PDP-11/70 can be considered from several points of view. It provides upward mobility for current users of PDP-11 systems. It can computerize applications that have not been efficiently computerized before. It can — because of its size and low cost — directly impact batch business systems by offering a timesharing and/or distributed processing alternatives. It can — because it concurrently operates in several modes — be used by manufacturers to combine functions to process control, data entry and business processing that were previously served by several systems.

The PDP-11/70 will fare differently on all these fronts. Unquestionably, sooner or later it will be used to upgrade PDP-11/45 installations. Initial prospects for minicomputertype applications on a large scale include a variety of aeronautics, traffic control and military applications, as well as communications preprocessing and message switching.

Digital, in its initial announcement of the PDP-11/70, introduced the PDP-11/70-based DEC Datasystem 570 with the Commercial Time Sharing System Extended (CTS 500/E) software. This implies that Digital expects the PDP-11/70 to be particularly important as a basis for a mainly business-oriented system, a timesharing type system that would offer an alternative to small- and medium-scale batch processing systems of much higher price. Data General has also developed a commercial system, the C/300, based on their ECLIPSE 200 system. Thus, the PDP-11/70 may find many customers not as an 11/70 proper competing on the mini/midi market, but as a commercial system, with the system's low price offsetting the lack of applications software. The competitive stance of the PDP-11/70 as a commercial system is best examined in the context of AUERBACH business computer reports on the DEC Datasystem line, but it is noted here because of the system's ability to combine timesharing, real-time and batch processing under IAS.

Although the non-commercial market for midcomputers (as distinct from minicomputers) is still undefined and tentative to some extent, the fact that four companies have made new announcements in this area promises an interesting period of new developments. All undoubtedly expect customers to "move up" to bigger systems in process control and communications, and Digital expects multi-language timesharing under IAS to be important in the education market. It will be interesting to see if "midis" turn up new applications that could not have been done by several minis. Data General's ECLIPSE system is nearest to the PDP-11/70 in overall architectural specifications since it is strictly a 16-bit system, with a cache

memory to speed processing and memory management to enlarge capacity. ECLIPSE currently can expand memory only to 256K bytes, it does not have internal 32-bit busses and it supports a smaller number of peripheral devices; both hardware and software facilities for communications are particularly well developed, and the price for a 128K-word system is lower for the ECLIPSE than the PDP-11/70. Interdata's 8/32 is a 32-bit system except for I/O facilities, it is the first 32-bit system by a major mini maker, and it is strongly oriented toward communications and real-time I/O, with speeds and I/O capabilities comparable to the PDP-11/70. SYSTEMS Engineering Laboratories, a small manufacturer, has introduced the SEL 32, a 32-bit word system. Both MOD-COMP IV and Prime 300 also compete to some extent with PDP-11/70 configuration by virtue of their speed and size. Table 2 compares some of the specifications of these "midi" systems with IBM's 370/158.

With regard to Digital's own product lines, the PDP-11/70 was long overdue. Reports for the past 2 years indicated the traffic over the UNIBUS kept throughput down on configurations with substantial I/O requirements. Competitors consistently claimed to outbenchmark the 11/45 in real-time environments. Digital offered dual-ported solid state memory with a second internal bus to the CPU on the 11/45. The second port could support a second UNIBUS for multiprocessor configurations, but generally it was connected to the system UNIBUS. Solid state memory was restricted to 32K words, thus throughput was increased only for programs executed from solid-state memory.

The PDP-11/70 overlaps the low end of Digital's PDP-10 line, notably the older KA10 processor, which has not been actively marketed for 2 years. Digital recently upgraded the PDP-10 with the KL10 processor, which is several times as powerful as the older KA10. When asked if Digital plans to provide a bridge between the PDP-11 line and the PDP-10 line, a spokesman indicated such a bridge is at least 2 years away. One stumbling block is the PDP-10's 36-bit word, which is difficult to match with the PDP-11's 16-bit word.

With the new Digital Network Architecture (DNA), Digital is providing facilities so users can easily tie all the PDP computer systems together in a network. This is a good move, for Digital's systems span a broad performance range. The PDP-11/70 is a powerful system that can provide extensive data processing as well as communications capability.

## Configuration Guide

A minimum PDP-11/70 System consists of a processor, UNIBUS, high-speed data bus with four I/O ports, 2,048-byte cache memory, 128K bytes of core memory, clock bootstrap loader, powerfail detect, disc and console. Standard processor features include 16 registers (12 accumulators, three stack pointers and a program counter), 4-line/8-level interrupt subsystem, memory management

Table 2. Comparison of Midicomputers with General Purpose Computer Systems

	Interdata 8/32 Megamini	Digital PDP-11/70	Data General ECLIPSE 200	SEL 32	IBM 370/158
Word Length (bits)	32	16	16	32	32
Instruction Execution Times (μsec (register to memory))					
Integer Add	1.2	1.8	2.5	1.2	.9
Integer Multiply	3.5	3.9	8.8	4.5	2.0
Integer Divide	5.8	8.3	11.2	5.1	9.9
Floating-Point Add	2.3	8.2	5.5	3.0	2.4
Floating-Point Multiply	3.0	11.2	7.2	4.5	2.3
Floating-Point Divide	5.3	12.2	7.9	8.9	8.9
Hardware I/O	Yes	No	No	No	Yes
Max DMA Rate (bytes/ sec)	6M	4M	2M	6M	6.7M
Max Address Capability (bytes)	1M	64K	64K	512K	16M
General-Purpose Registers	8 stacks of 16 each	2 stacks of 8 each	1 stack of 4	1 stack of 4	1 stack of 16
Prices, & (Dollars)					
CPU + 128KB Memory	51,900	54,600 <sup>(1)</sup>	35,500	43,900	NA
+ 256KB Memory	70,900	68,800	57,100	71,700	NA
+ 512KB Memory	107,400	101,800	NA	128,000	1,779,200
+ 1048KB Memory	179,400	163,800	NA	238,400	1,905,700

Note: (1) Digital bundles parity, console, line clock and installation in the system price.

and protection, and parity. Processor options include expansion of memory in 64K-byte increments up to 2M bytes, and a floating point processor with 46 associated instructions added.

The PDP-11/70 is a dual bus system. One bus is actually 36 bits wide; it carries four data bytes plus four parity bits between memory and the high-speed device controllers. The other bus is the 18-bit wide UNIBUS; it carries two bytes plus two parity bits. Like other PDP-11 systems, most peripheral controllers can connect to the UNIBUS in any order and in any combination. Although the UNIBUS map makes memory modules "look like" they connect to the UNIBUS in the same way as a peripheral device, they actually interface to the CPU via a high-speed cache memory. The 36-bit wide high-speed bus has four integral ports for the attachment of controllers for mass storage subsystems. These ports can attach RWP04 moving head disc subsystems, RWS03 and RWS04 fixed-head disc subsystems, and TWU16 magnetic tape subsystems. Transfers to and from these subsystems include byte parity.

The PDP-11/70 is sold in nine different models that vary in the type of mass storage device(s) included and in single or dual processor versions. Model numbers are as follows:

- PDP-11/70-EA single processor, cartridge disc.
- PDP-11/70-FA single processor, disc pack, and magnetic tape.
- PDP-11/70-FE single processor, dual-access disc pack and dual control, and magnetic tape.
- PDP-11/70-FK single processor, dual-access disc pack and dual control — one for 11/70 and one for any PDP-11, and magnetic tape.

- PDP-11/70-GA single processor, cartridge disc, fixed-head disc, and magnetic tape.
- PDP-11/70-HA single processor, disc pack, fixed-head disc, and magnetic tape.
- PDP-11/70-HE single processor, dual-access disc and dual PDP-11/70 controls, fixed-head disc, and magnetic tape.
- PDP-11/70-HK single processor, dual-access disc and dual controls — one for general PDP-11, fixed-head disc, and magnetic tape.
- PDP-11/77-FE dual processor 11/70s with dual-access discs and two control units and two magnetic tape drives.

All models include controllers for the mass storage units. A corresponding series of 230VAC, 50-cycle systems are also available.

The 11/70 UNIBUS is completely compatible with the UNIBUS for all other PDP-11 systems; it can attach any of the PDP-11 peripherals. These are summarized in Table 3.

Software packages, of course, demand different configurations. Memory requirements are usually satisfied by the minimum configuration, but peripheral requirements vary. Table 4 summarizes the major packages and their configuration requirements.

### Compatibility

PDP-11 computers are upward compatible, from the PDP-11/04 through the 11/10, 11/20, 11/40, to the 11/45, 11/50 and 11/70, and their OEM equivalents. All can use the same peripheral devices, as well as the same instruc-



**Table 3. Digital PDP-11: Peripherals**

Model No.	Description
<b>Discs</b>	
RS03/RS04	Fixed-head discs — 256K/512K wds/drive; 8 drives/controller attach to high-speed data channel
RK05	Moving-head cartridge discs — 1.2M wds/pack; 8 drives/controller attach to Unibus
RP04	Moving-head discs — 3330-type, 44M wds/pack, 8 drives/subsystem attach to high-speed data channel
<b>Magnetic Tape</b>	
TC11/TU56	DECtape — 288K char/reel; 4 drives/controller
TM11/TU10	7 or 9-trk magnetic tape — 45 ips; 8 drives/controller
TA11	Dual cassette transport and controller
TJU16	9-trk magnetic tape system — 800 bpi only or mixed 800 NRZI/1,600 PE, 8 drives/controller
TU16	9-trk 1,600 bpi magnetic tape; 8 drives/controller; attaches to high-speed data channel
<b>Card</b>	
CM11	Mark sense reader — 40 col, 200 cpm
CR11/CD11	Punched cards — 80 col, 300/1,000 or 1,200 cpm respectively
<b>Paper Tape</b>	
PC11	Reader/punch — 300 cps read, 50 cps punch
PR11	Reader — 300 cps
<b>Printers</b>	
LP11	Line Printer series — 170 to 1,200 lpm, 80 to 132 cols, 64 or 96 char
LS11	Line printer — 60 lpm, 132 cols, 64 char
LV11	Electrostatic printer/plotter — 500 lpm, 120,000 dots/sec
<b>CRT</b>	
VT01/TR01	Tektronix 611/RM503, respectively
VR14	Point plot display — 7 x 9 in.
VT05	CRT displays — 1,440 char (20 lines, 72 char/line)
<b>Graphics</b>	
GT40	PDP-11/10-based subsystem — 17-in. CRT, light pen
GT42	PDP-11/40-based subsystem — 17-in. CRT, light pen, disc
EG11	Engineering display subsystem — dot display, 71 x 43 A/N chars, controller
<b>Teletypewriters</b>	
Teletypes	LT33 & LT35 ASR and KSR units — 10 cps
LA30	DECwriter — 30 cps, local/remote
<b>Communications</b>	
DC11	Digital I/O subsystem — 50 to 1,800 baud units
DL11	Full-duplex single serial line interfaces — to 2,400 baud
DJ11	16-line mplr
DH11	Programmable async 16-line multiplexor
DP11	Sync line module set — full/half duplex models up to 40K baud
DU11	Sync interface — full/half duplex, 9,600 baud
DQ11	Sync interface — full/half duplex, models up to 1.0M baud
DF11	TTL to 20 mA local TTY, or EIA/CCITT voltage
DN11	System unit for 4 Bell 801 ACUs
DC08	Telegraph line interface — up to 32 lines

**Table 3. (Contd.)**

<b>Process I/O</b>	
LPS	Laboratory peripheral system — for up to 48 channels of A/D and 8 channels of D/A
AD01	A/D conversion subsystem — up to 32 channels
AA11	D/A conversion subsystem — up to 4 channels

**Table 4. Digital PDP-11: Software**

Package	Description
<b>RSTS-E</b>	Timesharing for up to 63 terminals, using extended BASIC, runs on any minimum system with terminal; roughly requires 4K words of memory for each terminal implemented; requires 20K words of memory for each terminal that has the \$COBOL facility.
<b>RSX-11D</b>	Real-time multiprogramming executive disc-based, uses on-line FORTRAN and COBOL, runs on minimum PDP-11/70 system
<b>IAS</b>	Combines real-time, batch and timesharing in foreground / middleground / background system, with extended BASIC and on-line FORTRAN and COBOL; up to 16 timesharing users, runs on minimum system
<b>BASIC</b>	Extension of Dartmouth BASIC, language of RSTS-E and IAS
<b>FORTRAN IV</b>	ANSI standard, extended, on-line version for RSX-11E and IAS
<b>COBOL</b>	ANSI X 3.23-1974, standard plus extensions
<b>Assemblers</b>	MACRO
<b>Utilities</b>	Editor, debugger, linker, librarian, loader and so on

tion and data formats. All use the same basic instruction set; the 11/35, 11/40, 11/45, 11/50, and the 11/70 use supersets of the basic instruction set.

PDP-11 is not compatible with any other computer system.

## MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks outside the large computer companies, both in the United States and worldwide. More than 1,500 engineers man its service staff.

Aside from 46 sales and service locations in the United States, Digital has offices in five Canadian cities, six Australian cities, five German cities, six U.K. cities, three Brazilian cities, and one or two cities each in Argentina, Austria, Belgium, Chile, Denmark, Finland, France, India, Israel, Italy, Japan, Mexico, the Netherlands, New Zealand, Norway, Philippines, Puerto Rico, Spain, Sweden, Switzerland, and Venezuela. Although minicom-

## DIGITAL EQUIPMENT — PDP-11/70 SYSTEM REPORT

puter manufacturers have traditionally aimed at somewhat "self-sufficient" users and have thus provided considerably less software support and applications programming assistance than the large systems makers, this picture is changing, as evidenced by Digital's recently added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour periods. An on-site engineer can also be hired if requirements are critical on the other hand, a user can buy service on an individual call basis, or set up his own maintenance staff.

### TYPICAL PRICES

Model Number	Description	Purchase Price \$
<b>Processors and Working Storage</b>		
All PDP-11/70 systems include: 11/70 central processor with memory management; 2K-byte parity bipolar cache memory (1 byte=8 data bits and 1 parity bit); 128K-byte parity core memory (MJ11-A plus MJ11-AE); bootstrap/diagnostic loader (M9301-YC); and line frequency clock (KW11-L); DECwriter II console terminal (LA36-C); terminal control (DL11-A); 2 cabinets for central processor and core memory; prewired space within the CPU chassis for mounted options		
11/70-EA/ED*	PDP-11/70 with RK11-DE cartridge disc and control; RK05-AA cartridge disc; and BA11-KE expansion mounting chassis	72,650
11/70-FA/FD*	PDP-11/70 with RWP04-AA disc pack and control and TWU16-EA (ED) magnetic tape and control	105,100
11/70-FE/FJ*	PDP-11/70 system with RWP04-BA dual access disc pack and two 11/70 control units; TWU16-EA magnetic tape and control	117,100
11/70-FK/FN*	PDP-11/70 system with RWP04-CA dual access disc pack with 11/70 control and general 11 control; TWU16-EA magnetic tape control	117,100
11/70-GA/GD*	PDP-11/70 system with RK11-DE cartridge disc and control; RK05-AA cartridge disc; RWS04-BA fixed-head disc and control; TWU16-EA magnetic tape and control and BA11-KE expansion mounting chassis	109,350
11/70-HA/HD*	PDP-11/70 with RWP04-AA disc pack and control; RWS04-BA fixed-head disc and control and TWU16-EA magnetic tape and control	126,300
11/70-HE/HJ*	PDP-11/70 with RWP04-BA dual access disc pack and two 11/70 control units; RWS04-BA fixed-head disc and control; TWU16-EA magnetic tape and control	138,300
11/70-HK/HN*	Same as 11/70 HE/HJ with general 11 control	138,300
11/77-FE/FJ*	Dual processor PDP-11/70 with 2 TWU16-EA magnetic tape and control; RWP04-BA dual access disc pack; and 2 control units	187,200
FP11-B	Floating Point Processor	5,600
MJ11-AC/AD*	256K byte parity core memory	33,000
MJ11-AG/AH*	256L byte parity core memory expansion frame	31,000
MJ11-AA/AB*	64K byte parity core memory unit	13,500
MJ11-AE	64K byte parity expander core memory	7,100
<b>Mass Storage</b>		
<b>Discs</b>		
RWP04-AA/AB*	88 million byte disc pack drive and control unit	35,000
RWP04-BA/BB*	88 million byte disc pack drive (with dual access) and 2 PDP-11/70 control units	47,000
RWP04-CA/CB*	88 million byte disc pack drive (with dual access and 2 control units)	47,000
RP04-AA/AB*	88 million byte disc pack drive (1.25 $\mu$ sec/byte transfer time; 8.3 msec average access time)	25,900
RP04-BA/BB*	Same as RPO4-AA/AB with dual access	30,800
RWS03-BA/BD*	512K byte fixed-head disc drive and control unit	14,900
RWS04-BA/BD*	1 million byte fixed-head disc drive and control unit	21,200
RS03-AA/AD	512K byte fixed-head disc drive	9,500
RS04-AA/AD	1M byte fixed-head disc drive 1 $\mu$ sec/byte xfer time, 8.5 msec average access time	13,800
<b>Input/Output<sup>(1)</sup></b>		
<b>Magnetic tape</b>		
TWU16-EA/ED*	Program selectable 1,600/800 bpi magnetic tape transport and control	15,500
TWU16-EK/EN*	800 bpi magnetic tape transport and control unit	14,450
TU16-EE/EJ*	Magnetic tape transport	8,950
<b>Software</b>		
QP210-AD/AE/AF/AP	IAS (Interactive Application System)	7,800**
QP240-AD/AE/AF/AP	BASIC	500**
QP230-AD/AE/AF/AP	FORTRAN IV	700**
QP010-AD/AE/AF/AP	COBOL-11	7,000**

#### Notes:

\*Indicates 230 VAC, 50 cycle power; first number is 115 VAC, 60 cycle power

\*\*License fee

(1) Other peripherals same as for other PDP-11 systems

# DIGITAL EQUIPMENT CORP.

## PDP-11/70 System Report Update

### New Software Packages

Digital's two new major software products for PDP-11/70 computers are DBMS-11, a comprehensive CODASYL-compatible data base management system, and RMS-11, a file-handling system for creating and maintaining organized files for applications not large enough to require full data base management.

**DBMS-11.** DBMS-11 is based on the Cullinane Corporation's Integrated Database Management System (IDMS) and like IDMS, is a generalized system for creating a central data base that can be accessed by any number of application programs.

DBMS-11 consists of two control languages: a Data Description Language (DDL) to establish the data base and a Data Manipulation Language (DML) to access or alter the data base as necessary. Space is physically allocated into fixed pages that are further subdivided into Schema and Subschema. Using a record (which can have various formats) as the basic unit, DDL defines the Schema, the data elements within it, and the logical relationships of those elements; any number of logical Subschema can be more specifically defined by DDL. A comprehensive set of routines for maintaining or recovering the data base is provided. These include SET membership and linkage, page find/fix, recovery and journaling, journal roll-forward and roll-back, journal tape fix, security dump, security restore, on-line recovery, a calculate routine, and a common access monitor.

Data can be stored in the data base in three modes: direct, calculated (by some user-assigned value), or by association with some occurrence or department within the data base. Data can be retrieved in a single access by DML. DML consists of statements embedded in the procedure division of application programs written in COBOL or in other languages that support a CALL statement (FORTRAN, BASIC, MACRO II). Security protection is implemented via DML Subschema.

A complete DBMS-11 system, including a PDP-11/70 processor with 256K bytes of memory, 88M bytes of disc storage, a 1,600-bpi magnetic tape drive and control, a line printer, video terminal, COBOL compiler, and the IAS (Interactive Application System) operating system, is priced at \$5,016 per month on a lease/purchase plan. DBMS-11 software can be purchased alone for \$15,000; it requires a COBOL compiler and the IAS executive. DBMS-11 will be available after December 1976.

**RMS-11.** The Record Management Services (RMS-11) software provides keyed-access record and file management for any PDP-11/70 system that supports the RSTS/E

(Resources Sharing/Time Sharing/Extended) operating system. RMS-11 consists of utility programs for creating and maintaining sequential, relative, or indexed files, and operating system routines for transmitting fixed- or variable-length records to and from user programs.

With RMS-11, files can be organized and reorganized without presorting, and data can be accessed by either physical location or logical organization. RMS-11 also handles multi-level searches (both generic and approximate) and provides privacy control for multi-user environments. RMS-11 supports features of ANS-74 COBOL; this provides compatibility across systems and a growth path to full data base management.

The RMS-11 software is licensed at \$2,500 and will be available by the end of 1976.

### New BASIC Compiler

BASIC-PLUS-2, Digital's newest compiler, extends the capabilities of previous BASIC compilers. It will be available for all PDP-11/70 systems that run under the RSTS/E, RSX-11M, or IAS operating systems.

BASIC-PLUS-2 incorporates new record I/O facilities (including sequential and relative file organization), code optimizations, a CALL statement, variable names of up to 30 characters, and comprehensive debugging facilities; it is upward compatible with the BASIC-11 and BASIC-PLUS compilers previously offered by Digital. A multi-keyed ISAM (Indexed Sequential Access Management) option is available.

BASIC-PLUS-2 will be available for RSTS/E in January 1977 and for RSX-11M and IAS in March 1977. It will be licensed to new users at \$4,000 and to upgrading users at \$2,500, including on-site installation and field software support.

### Communication Interfaces

Digital now offers three new communication interfaces for PDP-11/70 systems: DMC11 is a single-line high-speed synchronous interface, DPU11 a single-line multiprotocol synchronous interface, and DZ11 a low-cost asynchronous eight- or 16-line multiplexor.

DMC11 provides high-speed linkage between PDP-11s using Digital's Data Communication Message Protocol (DDCMP). DMC11 incorporates a high-speed microprocessor that handles DDCMP functions. DMC11 can operate locally over coaxial cables at 56K to 1M bits per second, or (by further interfacing to asynchronous

modems) over common carrier lines at 19.2K bits per second. The DMC11 hardware protocol provides message formatting, header processing, and message acknowledgment and retransmission. The DMC11 interface is priced from \$2,145; deliveries began in September 1976.

The DPU11 interface can handle several protocols including DDCMP, SDLC, HDLC and bisync. DPU11 operates with synchronous modems at speeds up to 9,600 bits per second. DPU11 hardware performs zero-bit insertion and deletion, flag and abort generation and detection, frame checks for SDLC and HDLC protocols, and cyclic redundancy checks for DDCMP. The DPU11 interface is available 30 days after order and costs \$1,375.

The DZ11 multiplexor connects eight or 16 local or remote asynchronous terminals or modems to PDP-11/70

computers, allowing both format and line speed to be programmed on a per-line basis at up to 9,600 baud. Input is by character in a 64-entry first-in-first-out buffer; output is double-character buffered. An eight-line DZ11 model is available for \$2,100 and a 16-line DZ11 is available for \$3,400 in EIA or 20-MA versions.

### Double-Density Disc Drive

RK05F is a double-density disc drive that Digital has developed for PDP-11/70 systems. The RK05F, which is nonremovable, is really two logical drives working as one to provide 2.5M words of storage. Data transfer rate is 180K bits per second.

The new drive will cost \$6,500. At the time of this writing delivery dates were not firm.



## OVERVIEW

The Digital Equipment PDP-15 is an 18-bit minicomputer system aimed at the midcomputer market and designed for laboratory, control, scientific, and mathematical applications that can benefit from the larger memory and greater arithmetic precision of the longer 18-bit word.

The system, which has been on the market since 1970, has acquired a very respectable body of software. Operating systems include scientific, FORTRAN-oriented DOS-15 and BUS-15 systems, ADvanced Software System (ADSS), and RSX PLUS III. The last is a new foreground/background real-time multiprogramming system supplanting earlier RSX-15 and RSX-PLUS systems. If systems are small, they can also run under a basic monitor and use a stand-alone assembler. Special operating systems are provided for applications like data management (MUMPS) and graphics (GRAPHICS 76). A new subscription service and software updating add to the software support.

All systems use the same central processor, and all are field expandable. Floating-point hardware, power failure protection, and memory parity are among the mainframe options. Features such as the extended arithmetic element, automatic priority interrupt, memory protect, memory relocate, and the real-time clock are either standard or optional depending on the configuration.

Main storage is a core memory that ranges in size from 4K to 132K words. The PDP-15/10, 20, 30, 35, 40, and 50 all use the MM15 and MK15 core memory, which has an 800-nanosecond cycle time. Since these systems are now considered traditional (nonstandard) products, they are available only on special order.

The PDP-15/76 Series uses the ME15 core memory, which has a 980-nanosecond cycle time and is available in 8K- and 16K-word modules. The newest family members are the PDP-15/78 and PDP-15/76C systems, which use the LA36 DECwriter II as the system console.

A memory multiplexer permits multiprocessing. The PDP-15 can support four multiplexers to permit a variety of memory and processor configurations. Several hardware/software system combinations provide for multiprogramming. Multiprocessing is not software supported except on the PDP-15/76, where the PDP-11/05 is supported as a peripheral processor (via Unichannel 15) by DOS-15, BOSS-15, and RSX PLUS III.

A number of applications packages are included in the software. There are electrocardiography (ECG-1500) packages for the medical field. Several interactive graphics packages (ARK-2) are for architectural project design and management and electronic circuit layout. Others cover such subjects as pulse height analysis (PHA-15) and spectral analysis (GASPAN) for the scientific community.

Digital also provides STATPAC (an open-ended package of statistical programs for the user with limited computer knowledge), SCOLDS (Spark Chamber On-Line Data System), two hybrid software systems, CSMP-15 (Continuous System Modeling Program), Lab RSX-15, GRASP-15 (Generalized Remote Acquisition and Sensor Processing), and REDAC (Real-Time Data Acquisition for electronic design tasks).

## Competitive Position

The PDP-15 has been a strong competitor for applications in the midcomputer range. It is cheaper than comparable configurations of large computer systems, and it is more powerful than most top-of-the-line minicomputers. Memory capacity can range from 4K to 132K 18-bit words.

There has been a growing trend among minicomputer manufacturers to expand the capabilities of their major minicomputer lines through memory mapping options and various other stratagems in order to compete at the midcomputer level. Digital itself has done this with the PDP-11/45, while Data General, General Automation, Hewlett-Packard, and Interdata have all developed memory mapped systems and multiprogramming operating systems that can compete in the midcomputer range. Thus, the PDP-15 is going to find an increasingly competitive atmosphere in this sector of its market, particularly from recent systems taking advantage of new lower-cost MSI and LSI technologies to achieve lower prices.

One advantage of the PDP-15 over many competing products is its modular packaging into systems designed for specific markets. Users can add options, peripherals, and software in the field to expand these systems when needs change. This modular arrangement provides maximum performance from an optimum configuration since a user buys only the configuration he needs knowing the system can grow to meet future requirements.

A second advantage of the PDP-15 over competing minicomputer systems is the numeric precision of the

18-bit word over the 16-bit word. Floating-point (real) numbers can be represented in the PDP-15 with a 17-bit exponent and a 35-bit fraction (equal to 10 decimal digits).

Another competitive advantage is the amount of available interface equipment so that almost any laboratory or industrial customer can fit the PDP-15 to his needs using Digital hardware. If a customer requires special interfacing, Digital will usually make it to order.

A fourth advantage of the PDP-15 is its extensive software support.

Prime competitors to the PDP-15 are the new Data General Eclipse, Interdata 8/32, Prime 300, HP 21MX, Xerox 550, SEL System 80, Modular Computer Systems MODCOMP IV, IBM System 360/44, and Digital's own PDP-11/45. The Hewlett-Packard HP 3000 and Varian V70 will also be competing with the PDP-15 for some applications.

Although the PDP-15 architecture has changed little from that of the PDP-7 and 9 (now traditional products), Digital has enhanced the system consistently, providing up to 132K words of memory, floating-point processor, mass storage, many peripherals, and software. The PDP-15/70 Series, for example, uses the ME15 memory, which is considerably cheaper than the older MM15 memory. Use of a PDP-11/05 as a peripheral processor with the PDP-15/76 makes the PDP-11 peripherals available.

Digital as a company is responsive to user needs and supports DECUS (Digital Users Society), an active, outspoken users group.

Users we contacted bought the PDP-15 for a variety of applications. An air force base used one in a complex telemetry processing system that was a satellite to a CDC 6600. A medical school had developed an on-line EKG interpretation facility using a PDP-15 with 28K words of memory and 2 fixed-head discs. Users felt the system was very reliable; both hardware and software have lived up to expectations. The medical school spokesman noted that in today's market, a PDP-11/40 would probably satisfy their requirements and be less expensive.

### Configuration Guide

Each PDP-15 standard model includes a central processor, core memory, and its own complement of features and peripheral devices to configure it for an application. Features and devices offered are common to all the family. Table 1 lists the standard models and their system components. Table 2 lists general system specifications.

Peripherals include a line of display and graphics equipment in addition to the more usual console typewriters, paper tape and punched card units, line printers, magnetic tape units, and disc memories. Process control

**Table 1. Digital PDP-15: System Configuration Summary**

<b>CENTRAL PROCESSOR</b>	
Type	Hardwired
No. of Internal Registers	1 GP, 1 index
Addressing	
Direct (no. of wds)	4,096
Indirect	1 level
Indexed	Yes
Instruction Set	
Implementation	Hardware
Number	65-222
Floating-Point Arithmetic	Optional hardware
Decimal Arithmetic	No
Priority Interrupt Levels	8 levels, 32 sublevels
<b>MAIN STORAGE</b>	
Type	Core
Cycle Time ( $\mu$ sec)	980
Basic Addressable Unit	18-bit word
Bytes per Access	2
Cache Memory	No
Capacity (bytes)	8K-256K
Increment Sizes (bytes)	8K/16K
Ports Per Module	1
Error Checks	Parity; opt
Protection	Yes; opt
Memory Management	No
ROM	No
<b>INPUT/OUTPUT</b>	
I/O Channels	
Programmed I/O	Yes
DMA	Yes
Multiplexed I/O	No
Max DMA Transfer Rate	1M wds/sec

devices and analog/digital equipment are also offered. Data communications equipment includes both controllers and terminals. The PDP-15/76 uses a PDP-11/05 as a peripheral processor to support the RK11E/RK05 Disk Cartridge System. Peripherals are listed in Table 3.

Operating systems and similar system control packages differ widely in the configurations they require. Table 4 summarizes the major system packages and indicates the minimum configuration needed for each.

### Compatibility

The PDP-15 is upward-compatible with the older PDP-9, PDP-7, and PDP-4, but not the PDP-1. PDP-9 is a direct descendant of the PDP-7 and the PDP-4, and has an identical instruction repertoire but with expanded capabilities.

The instruction repertoire of the PDP-15 is even more extensive than that of the PDP-9. Twelve additional instructions are provided to clear, load, store, and increment the index register. Moreover, there are optional floating-point instructions.

Compatibility among programs written for the PDP-9 and PDP-15 varies with the programming language used. FORTRAN-coded programs are compatible because the software accommodates the hardware differences. Assembly language programs are restricted to the instruction subset and the addressing capability common to both the PDP-9 and the PDP-15.



**Table 2. Digital PDP-15: Mainframe Specifications**

Model No.	Description
<b>Discs</b>	
RF15/RS09	Up to 8 RS09 drives per RF15, 256K wds per drive; 15M-, 31M-, or 62M-wd/sec transfer
RP15/RP02	Up to 8 RP02 drives per RP15, 10M wds per drive; 135K-wd/sec transfer
RK15 Subsystem	RK11 control/RK05 DECpack System, 1.2M words per cartridge, 70-msec avg. access
<b>Magnetic Tape</b>	
TC59P/TU10	4 TU10 transports per TC59; TU10 is 7-trk or 9-trk, 800/556/800 bpi, 45 ips
TC15/TU56	DECtape control and dual DECTape transport, block addressable
<b>Card</b>	
CR15 Series	200-, 300-, or 1,000-cpm readers
<b>Paper Tape</b>	
PC15	200-char/sec reader; 50-char/sec punch
<b>Printers</b>	
LP15 Series	356-1,110 lpm or 253-843 lpm; 80 or 132 col; 64 or 96 char sets
<b>Plotters</b>	
XY15 Series	Calcomp 563 and 565 Drum Plotters; 12-inches and 31 inches, respectively
<b>Displays/Graphics</b>	
VP15 Series	Control & display, 5" and 7 x 9" models, BW or 2-color; 10-bit data word per direction; 1 part in 1,024 resolution
VR01	5" diameter P7 phosphor oscilloscope
VR14	Oscilloscope 5 x 7" P31 phosphor oscilloscope
VR20	Two-color x-y oscilloscope 7 x 9"
VT15 Series	Graphic-terminal, 17" diagonal or 21" diagonal
VT04	Display consoles, 17" diagonal VT 15 Graphic Processor
VT07	Like VT04 but 21"
VL04/VL07	Light pens for VT04/VT07
VW01	Writing tablet & spark pen
<b>Communications</b>	
Teletypes	ASR 33, KSR 33, ASR 35, KSR 35
LA 30	DECwriter terminals; 110, 150, 300 baud
VT05	A/N video display terminal; 20 lines, 72 char
<b>Analog/Digital</b>	
AFC-15	Analog input subsystem; up to 192 input channels
UDC 15	Digital I/O; for up to 384 points
BD15	Control unit for up to 11 AFC15s and 11 UDC 15s; 2,048 analog inputs; 4,096 digital points
<b>Laboratory</b>	
NP15	Nuclear physics assembly
CA15-A	CAMAC interface for up to 7 CAMAC crates
AD15	A/D medium-speed subsystem; up to 128 channels
ADF15	A/D high-speed subsystem; up to 36 channels
AA15	D/A subsystem; up to 16 channels
AF04	Digital voltmeter; analog input for 10-1,000 differential inputs

**Table 3. Digital PDP-15: Peripherals**

Package	Description
Basic Monitor	For minimum 8K-word system with paper tape I/O, Teletype
Advanced Monitor	Like basic monitor but can dynamically alter I/O assignments; supports FORTRAN, FOCAL; requires 12K words
Background/Foreground Monitor	Extension of Advanced Monitor to allow foreground/background multiprogramming
MUMPS-15	Massachusetts General Hospital Utility Multiprogramming System; compact systems using JOSS high-level language
DOS-15	Disk Operating System for batch systems; requires 16K words of core, DECwriter, paper tape I/O, clock, magtape, disc
BOSS-15	Batch Operating System; superset of DOS-15 using card reader, line printer
RSX PLUS III	Real-time foreground/background multiprocessing system; requires 32K words of core, 0.5M words of disc storage, terminal, memory relocation hardware, paper tape, magtape or DECTape, real-time clock
ALGOL	ALGOL 60 ECMA Level 1; some restrictions
FORTRAN IV	Core-based and disc-based versions; some exceptions from ASA x3.9-1966
FOCAL	DEC's desk calculator language, single user or multiuser
COMPACT	Absolute assembler; needs less than 3K words of core
MACRO-15 Utilities	Macro Assembler Dynamic Debugging Technique (DDT), 8-15 Translator (ITRAN), System Generator, Copy, Dump, Library Update, System Patch, Editors, Peripheral Interchange, Linking Loader, Math Library, Magtape Dump, I/O Handlers
Applications Packages	Pulse Height Analysis, Gamma Spectral Analysis (GASPAN), Spark Chamber On-Line Data System (SCOLDS) for data acquisition, Continuous Systems Modeling Program (CSMP-15), STATPAC statistical programs, VT15 Graphics, Lab RSX-15, REDAC for electrical design tasks, ECG-1500 for electrocardiograms, ARK-2 for interactive graphics

Within the PDP-15 family, programs used on smaller systems will work on the larger systems without modification, but they generally will not use the full capability of the larger system.

## MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks (not including the large computer companies) both in the

Table 4. Digital PDP-15: System Software Packages

PDP-15 Model	15/76-CE/F	15/76-CK/L	15/76-CP/R	15/76-CS/T	15/78-AA/B	15/78-BA/B
KP15 Central Processor	X	X	X	X	X	X
Core Memory	ME15	ME15	ME15	ME15	ME15	ME15
Model	32K	32K	32K	32K	24K	24K
Size (words)	X	X	X	X	X	X
KE15 Extended Arithmetic Element						
FP15 Floating-Point Processor						
KT15 Memory Relocate						
KA15 Automatic Priority Interrupt						
KM15 Memory Protect						
KW15 Real-Time Clock	X	X	X	X	X	X
DW15-A I/O Bus Converter			X	X		
Teletypewriter						
ASR 33						
KSR 33						
KSR 35						
LT15 Single Teletype Control						
LA36 DECwriter II	X	X	X	X	X	X
PC15 Paper Tape Reader & Punch	X	X	X	X	X	X
TC59-D Magnetic Tape Control			X	X		
TU10 Magnetic Tape Transport			X	X		
TC15 DECTape Control	X	X				X
TU56 Dual DECTape Transport	X	X				X
RF15 DECdisk Control						
RS09 DECdisk Drive						
RP15 Disk Pack Control						
RP02 Disk Pack Drive						
RK15 Cartridge Disk System	X	X	X	X		
Disk Package with UNICHANNEL-15	X	X	X	X		
UC15 Peripheral Processor (PDP-11/10)	X	X	X	X		
Core Memory						
Model	MM11-K	MM11-L	MM11-K	MM11-L		
Size (words)	8K	12K	8K	12K		
RK11E DECpack Control	X	X	X	X		
RK05 DECpack Cartridge	X	X	X	X		

United States and worldwide, numbering more than 2,100 engineers at over 200 service locations. Although minicomputer manufacturers have traditionally aimed at somewhat "self-sufficient" users, those who need considerably less software support and applications programming assistance than are provided by the large computer manufacturers, this picture is changing, as evidenced by Digital's recently added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour periods. An on-site engineer can also be hired if requirements are critical; on the other hand, a user can choose to buy service on an individual call basis or to set up his own maintenance staff.



**TYPICAL PRICES**

Model Number	Description	Purchase \$	Monthly Maint. \$
<b>SYSTEMS*</b>			
PDP-15/76	Spooled Batch System	91,260	
PSX Plus III	Resource Sharing System	93,705	
PDP-15/76	Graphics Computer Aided Design System	121,020	
Graphic 78/REDC	Architectural Graphics System	111,845	
Mumps-15	Printed Circuit Layout Graphics System	104,770	
Data Base Management System includes: <b>CENTRAL PROCESSOR AND WORKING STORAGE</b>			
PDP-15/76-CE/CF	KP15 Central Processor (includes 32K Wds Core Memory; DECwriter II; High-speed Paper Tape Reader and Punch; Extended Arithmetic Element; Real-time Clock; TC15 DECTape Control; Dual DECTape Transport; Cartridge Disk System with UNICHANNEL-15; Peripheral Processor and 8K Core Memory)	68,500	634
PDP-15/76-CK/CL	Same as 15/76-CE/CF Model except peripheral processor has 12K-wd memory	71,200	655
PDP-15/76-CP/CR	Same as 15/76CE/CF Model except TC59-D Magtape control and TU10 Magtape transport used instead of TC15/TU56 DECTape system and DW15-A I/O Bus Converter added	75,000	687
PDP-15/76-CS/CT	Same as 15/76-CP/CR Model except peripheral processor has 12K-wd memory	77,700	708
PDP-15/78-AA/AB	KP Central Processor (including 24K Wds Core Memory; DECwriter II; High-speed Paper Tape Reader and Punch; Extended Arithmetic Element; Real-time Clock;	35,000	318
PDP-15/78-BA/BB	Same as 15/78-AA/AB except with TC15/TU56 Dual DECTape transport added	44,000	371
UC15-HE/HF	Peripheral Processors and memory	15,000	154
UC15-HK/HL	Peripheral Processor includes a PDP-11/10 in 10% in. enclosure, 8K MM11 core memory, MX15-B memory mplx, and interprocessor interrupt link	17,700	175
MM11-K	Peripheral Processor (Same as UC15-HE/HF except that PDP-11/10 contains 12K-wd memory)	17,700	175
MM11-F	4K wds of PDP-11 core memory	2,700	21
KE15	4K wds of PDP-11 core memory	3,780	27
KA15	Processor Options	2,800	27
KM15	Extended Arithmetic Element	2,000	21
KT15	Automatic Priority Interrupt	1,000	15
KS15	Memory Relocation	2,000	32
KF15	Memory Management/Automatic Priority Interrupt Package	5,000	75
FP15	Power Fail	1,000	3
KW15	Floating Point Processor	9,750	80
DW15-A	Real-time Clock (Line frequency)	500	3
BA15	I/O Bus Converter	2,160	21
BB15	Control for LT15-A, PC15, and VP15 options	NC	10
ME15-AA/AB	Processor Expander Panel	1,500	11
ME15-B/C/D	Memory Options		
ME15-E/F/H/J	ME15 Core Memory (18-bit wds; 980 nsec)	6,000	42
	8K Memory	6,000	42
	8K Expansion Element	9,800	85
	16K Memory		
<b>MASS STORAGE</b>			
RF15	Disks		
RS09/RS09-A	DECdisk Control (for up to 8 RS09 DECdisks)	6,000	37
RP152-A/B	DECdisk Unit	9,000	48
RP02-AS/	Disk Pack Drive Unit and Control	27,000	207
RP02-BS	Disk Pack Drive Unit (10.2M wds/unit)	15,000	133
RP153-A/	Disk Pack Drive Unit and Control	32,000	233
RP153-B			
RP03-AS/	Disk Pack Drive Unit (20M wds/unit)	20,000	159
RP03-BS			
RP02-P	Spare Disk Pack for RP02 or RP03	295	-
RK15-HE/	Cartridge Disk System (Includes UC15 HE/HF peripheral processor)	20,600	260
RK15-HF			
RK15-HK/	Cartridge Disk System (Includes UC15 HK/HL peripheral processor)	23,300	281
RK15-HL			
RK05-AA/	DECpack System (1.2M words; DECpack drive and removable disc cartridge)	5,100	60
RK05-BB			
RK03-KA	Spare Cartridge	99	N/A
<b>INPUT-OUTPUT</b>			
CR15-FA/	Card Reader and Control (300 cpm)	5,400	80
CR15-FB			
CR15-DA/	Card Reader and Control (1000 cpm)	10,800	80
CR15-DB			
CR11/CR11-A	Card Reader and Control (300 cpm)	4,860	53
PC15/PC15-A	Paper Tape Reader/Punch	4,210	38
LP15-VA/	Line Printer and Control (300-lpm)	11,500	82
LP15-VD			
LP15-WA/	LP15-VA ILP15VD with 96 char set	13,500	82
LP15-WD			
LP15-RA/	Line Printer and Control (1200-lpm)	40,000	154
LP15-RB			
LP11-VA/	Line Printer and Control (300-lpm)	9,900	72
LP11-VD			
LP11-WA/	Line Printer and Control (300-lpm)	11,900	72
LP11-WD			
LS11-A/	Line Printer and Control (60-lpm)	5,615	58
LS11-B			
LV11-BA/	Electrostatic Printer/Plotter (500-lpm)	11,770	53
LV11-BB			
TC15	DECTape Control	5,400	27
TU56	Dual DECTape Transport	4,700	32
TC59-D	Transport Control	6,950	37
TU10-FE/EE	Transport (7/9-track; 45 ips; requires TC59D)	7,505	74
LA36-CA/CB	DECwriter II Keyboard Printer	1,850	25
XY15-AA/BB	Plotter and Control (Tabletop Model 565)	9,610	32

\*All systems include installation plus 90 days free parts and service. 90 days SPR service for software at no charge, and 6 weeks training.

Model Number	Description	Purchase \$	Monthly Maint. \$
XY15-BA/BB	Plotter and Control (Tabletop Model 563)	14,470	37
XY11	Incremental Plotter Control	1,300	5
CalComp-563	200 and 300 steps/sec	10,150	35
CalComp-565	300 steps/sec	5,830	35
Complot DP-1	300 steps/sec	6,050	35
Complot DP-10	300 steps/sec	3,445	35
XY311	Plotter and Control (1800 steps/sec)	18,900	75
VT05B-AA/AD	A/N Display HDX/FDX (20 lines by 72 chars; up to 2,400 baud)	2,795	23
VT50-AA/AB	A/N Display FXD or FDX with local echo; 12-line by 80-char format; 64 ASCII chars; rates to 9,600 baud std)	1,250	22
VP15-A	Storage Tube Display and Control	6,260	91
VP15-B	Oscilloscope and Control	3,885	32
VP15-BL	VP15-B with Light Pen	5,640	37
VP15-C	Oscilloscope and Control (7 x 9-in. VR14 X-Y display with 10-bit data word per direction.)	6,260	47
VP15-CL	VP15-C with Light Pen	8,015	52
VR01-A	Oscilloscope (5-in. diameter screen)	1,080	15
VR14	Oscilloscope (7 x 9-in. screen)	3,240	19
VT01-A	Storage Tube Display (table mounted)	3,240	80
GT15-SA/SB	Graphic System	24,000	146
GT15-LA/LB	Graphic System Same	29,000	173
VT04-A	Graphic Display Console (CRT; 6 lighted function buttons) VT15	4,860	27
VT04-B	Graphic Display Console	10,800	53
VV15-A	Arbitrary Vector Generator	5,000	21
VV15-K	VV15 Upgrade Kit (to VV15-A)	1,500	-
VM15-A	Display Mplx (for up to 4-VT04's/VT07's)	5,000	21
LK35	Keyboard (for VT04)	1,295	32
LK37	Keyboard (for use with VT07 console)	1,295	32
VL07	Light Pen (for VT04)	755	7
VL07	Light Pen (for VT07)	755	7
VW01-BP	Writing Tablet and Control	3,780	32
VW01-MX	Writing Tablet Mplx (for up to 4 VW01-MA writing tablets)	1,080	5
VW01-MA	Writing Tablet and Spark Pen	2,160	11
VW01-SP	Spark Pen	215	5
VW01-WT	Writing Tablet	860	11
<b>DATA COMMUNICATIONS</b>			
LT19-D	Multi-station Terminal Control	1,940	11
LT19-E	Terminal Line Unit	864	3
LT19-F	EIA Line Adapter	108	3
LT19-H	Cable Set Connects and LT19-F to another LT19-F for interprocessor communication.		
LT19-HA	50 ft	64	-
LT19-HB	100 ft	70	-
LT19-HC	150 ft	75	-
LT19-HD	200 ft	81	-
LT19-HE	250 ft	86	-
LT15-A	Single Terminal Interface	500	3
DC01-ED	Multi-station Terminal Control	6,480	21
DP11-DA	Full/Half Duplex Sync Line Module Set and System Unit	1,700	19
KG11-A	Communications Arithmetic Unit	900	6

**HEADQUARTERS**

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## OVERVIEW

The XVM systems are modified configurations of Digital's PDP-15/76. The big news with the XVM systems is the XM15 memory processor that sits between memory and other system components: CPU, interrupt link from I/O processor, and external processor. Not only does it combine a number of features provided by options on the PDP-15 into one unit (automatic priority interrupt, Unichannel multiplexor, memory protect, memory relocate, memory bus interface, and multiport adapter) but it adds a number of new features: instruction lookahead, wide addressing, dual memory buses, memory interleaving (up to 4-way), dual memory relocation registers, user I/O mode, and new high density memory modules. The instruction lookahead feature increases the instruction execution speed of the XVM over the PDP-15/76 by about 40 percent. The maximum I/O rate via the peripheral processor is also increased because of the increased bandwidth due to memory interleaving: 2-way or 4-way. This increased performance allows most PDP-11 processors to function as the peripheral processor; only the PDP-11/10 is used as the peripheral processor for the PDP-15/76.

Software support for the XVM systems will be provided under RSX-PLUS III and DOS. The XVM systems can run in PDP-19/15 mode and run all PDP-19/15 programs.

## XVM Models

The XVM systems are available in two models: XVM-100 and XVM-200.

The XVM-100 (Figure 1) is a small one-cabinet configuration that includes the CPU, memory processor, 32K words of memory, paper tape reader and punch, high speed multiply/divide, real-time clock, and LA36 DEC writer II. Memory can be expanded to 98K words in the basic cabinet. It can support the full line of XVM peripherals and software and can be configured into much larger systems including multiprocessor master/slave or ring configurations.

The XVM-200 is a dual processor configuration that includes all the features of the XVM-100 plus a PDP-11 with 8K words of memory as a peripheral processor and a 1.28 million-word disc cartridge drive and control. See Figure 2.

The dual memory bus structure of the XVM models lends itself to multiprocessor configurations. Systems can connect to each other in a master-slave relationship or in a ring relationship. The master is defined as the CPU that can address all the memory of all CPUs in the system as well as its own memory. The slave can address only 8K words of the master's memory in addition to its own memory. In a ring configuration, no CPU is the master; all

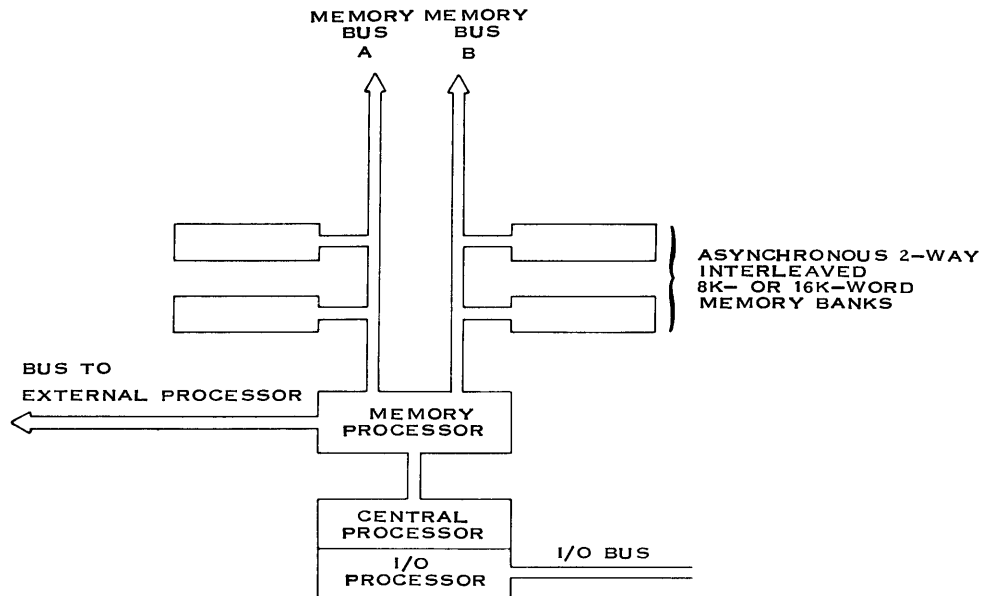


Figure 1. DEC XVM 100: Organization

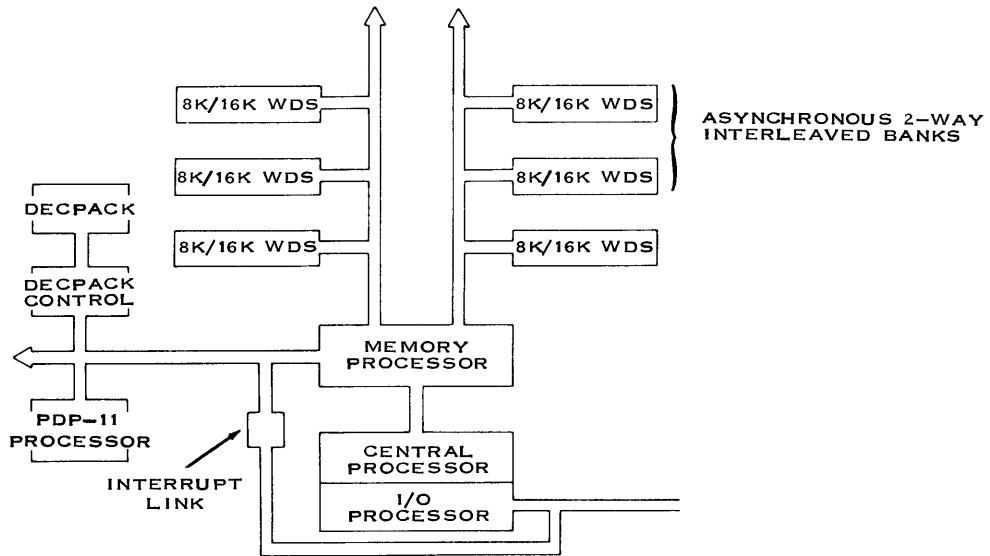


Figure 2. DEC XVM 200: Organization

CPUs in the system can address 8K words of each neighbor's memory in addition to its own memory.

When the PDP-11 is in the configuration, it is always the master because it can address all of the XVM memory. These configurations are now possible with the new PDP-11/70 functioning as a master and XVM systems operating as slaves.

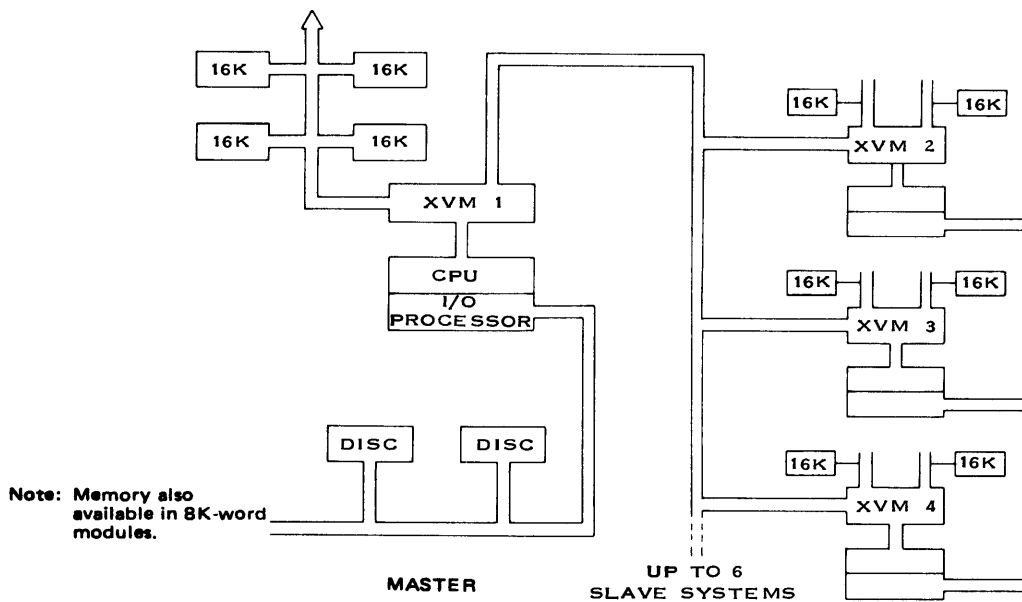
DOS and RSX do not support multiprocessor configurations except for the PDP-11 in a Unichannel configura-

tion. Many PDP-15 users have dual-processor configurations and have altered RSX to support them. Digital will put users in touch with other users who have modified RSX, but Digital does not directly support its operating systems for multiprocessor configurations.

**New Features**

The instruction lookahead feature provides a 4-word, 80-nanosecond buffer between memory and the instruction register. When an instruction is fetched, the CPU first





Note: Memory also available in 8K-word modules.

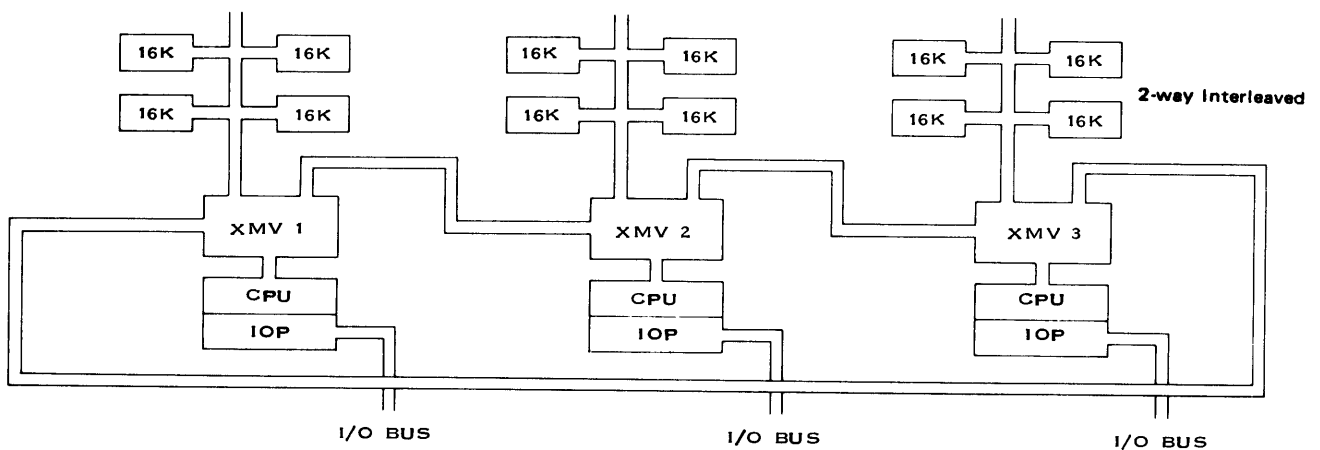
**Figure 3. DEC XVM Systems in Master/Slave Relationship**

checks the buffer to determine if the word is there. If so, the instruction is loaded into the instruction register. While it is executed, a new instruction is fetched from memory to fill up the buffer. Branch instructions reset the buffer and new instructions are fetched in a pipe-line fashion.

programs are restricted to 32K words. The software systems do not support 256K words of data. RSX allows any task to be 32K words and the user's data area to be 64K or 128K words. DOS supports 32K words for the executive and user code area and 128K words for the user data area.

Wide Addressing provides 16-, 17-, or 18-bit indirect addresses for data areas. In PDP-9/15 mode, indirect addresses are 15 bits long. Thus the CPU can address only 32K words in this mode. Instructions are provided to set the addressing mode. The wide addressing allows user programs to address 64K, 128K, or 256K words of data;

Dual memory buses provide 2-way interleaving on each bus for an overall effect of 4-way interleaving. The dual bus arrangement allows memory to connect to one bus and a second XVM system to connect to the other bus. See Figure 3. In the ring configuration, the last processor in the daisy chain connects to the first processor via the mul-



Note: 8K-word modules also available.

**Figure 4. DEC XVM Systems in Ring (daisy chain) Relationship**

tiplexor connection in the memory processor normally used by the Unichannel for the PDP-11. See Figure 4.

Memory interleaving is normally implemented by interleaving two 8K- or 16K-word modules on each of the two memory buses. Although not yet announced as standard models, XVM systems can have a single memory bus on which two or four 8K- or 16K-word modules can be interleaved.

Dual memory relocation registers allow the split segmenting of a user task under RSX into a local and a global section. The local section is private to the task while the global section can be shared with other tasks. The user program can be given read/write or read-only access to the global section.

One common usage of split segmenting is for multiprocessor configurations where the global space resides in the shared memory area. Global area is divided into two logical areas to simplify code sharing: one area contains the code and another area is equivalent to the beginning of the user's local area to provide local variables.

User I/O mode has been added to EXEC and user modes for processing critical user I/O tasks that cannot tolerate the overhead inherent in the executive I/O handling routines. A task operating in user mode can address memory outside its own area or initiate I/O only through the executive. In user I/O mode, the user task runs under memory protection but can execute direct I/O. Which task(s) can execute in user I/O modes is decided at task installation time.

New MF15 memory modules are based on the MF11-UP core modules used for the PDP-11; 16K words are stored on one board. These modules are 18 bits wide (two bytes plus byte parity for the PDP-11); all 18 bits are used for data on the XVM; thus parity is unavailable on XVM systems. Cycle time for these modules is 980 nanoseconds per word. Two 16K-word modules are interleaved on each memory bus; thus the effective cycle time is considerably reduced for most applications.

Higher speed 8K-word modules are available if greater flexibility is needed in configuring memory banks.

Other features include a relocation disable feature for compatibility with operating systems that do not need dynamic address translation but do need extended addressing. It allows the disabling of the feature under program control.

A high-resolution accounting timer is available for apportioning resource costs among users running under XVM/RSX. Time can be allocated in 10-microsecond intervals.

The memory multiplexor resolves conflicts among the three asynchronous elements that can request access to memory; central processor or I/O processor, instruction

lookahead feature, and the multiprocessor adapter for either the PDP-11 or another XVM. The multiplexor is an integral part of each memory port.

### Upgrading to XVM from PDP-15

PDP-15 users can upgrade their systems to the XVM by adding the memory processor and removing the system options now incorporated as standard for the XVM systems. The PDP-15 memory protect and relocation hardware, automatic priority interrupt, memory multiplexor, and MM15 or MK15 memory must be removed. They are replaced by the XM15-U memory processor and MF15-U memory. PDP-15 ME15 memory can be field converted for XVM operation; other PDP-15 memory must be replaced.

PDP-15 users can also upgrade to XVM as part of upgrading to an XVM Unichannel configuration with a PDP-11 peripheral processor.

XVM is upward software compatible with the PDP-9 and PDP-15 operating systems: ADSS, B/F, DOS, BOSS, MUMPS, and RSX PLUS III.

### XVM Software

Digital is modifying their three major operating systems as well as the RASP (real-time language for simultaneous processing) language to take advantage of the new features available to XVM systems.

The three operating systems are XVM/DOS, XVM/RSX, and XVM/MUMPS.

XVM/DOS will execute about 30 percent faster than PDP-15/76 DOS. FORTRAN and MACRO assembler programs can address up to 128K words of memory: 32K words for program code and 96K words for data defined in common blocks. PDP-15 FORTRAN programs will require recompilation and linking to take advantage of the larger arrays available on XVM.

XVM/RSX will execute faster, and thus it can handle more simultaneous users than RSX PLUS III on the PDP-15. It will support partitions of 128K words: the lower 32K words hold the program and data; the upper 96K words must store data defined in common blocks. The dual relocation registers are used to allow user tasks to address system common data blocks.

XVM/RSX supports EXEC, USER, and USE I/O operating modes.

XVM/MUMPS can support 20 to 48 users in a time-sharing data base management environment. MUMPS includes its own language.

### COMPETITIVE POSITION

The XVM systems improve the price/performance of the PDP-15 line. The new high density memories are



cheaper than the older PDP-15 memories. Thus it is more feasible to add memory to enhance performance, especially for RSX and MUMPS systems. In addition, the processor instruction execution speed has been improved over a PDP-15 system by 30 to 40 percent with the instruction lookahead feature. This increased speed makes it feasible to connect larger PDP-11 systems, even the new PDP-11/70, to the XVM systems via the Unichannel.

The major markets for the PDP-15 line have been in the midcomputer range where considerable applications software has been developed by companies outside Digital. Although Digital does not support the software, the company sells configurations that run the software. Initially, Digital is offering configurations for the REDAC and ARK II packages offered by outside vendors for the PDP-15.

The MUMPS software which was developed for Massachusetts General Hospital under a government contract and supported by Digital was first implemented on a PDP-15. It has become popular for hospital applications. In fact, efforts are being made to standardize the MUMPS language. A number of other companies are selling MUMPS systems in competition with Digital, notably Atronix, Inc. Both a MUMPS Users Group and a MUMPS Standards Group have been formed.

The PDP-15 line is increasingly impacted by the surging PDP-11 so in the spirit of "if you can't lick 'em, join 'em," the PDP-15 Unichannel included the PDP-11/10. The "camel" is now even more "in the tent" with XVM. Any PDP-11 system can be incorporated in the Unichannel, and the PDP-11 is the master in the multiprocessor configuration.

The XVM systems will indirectly extend the life of the PDP-15 line. Digital's new network architecture protocols and DECnet software that will be added to RSX will also help. Digital still includes the line in its future plans. Because of its long life, the major development costs have been written off long ago, so the line is extremely profitable.

## COMPATIBILITY

The XVM systems are upward software compatible with the PDP-9 and PDP-15. The XVM I/O processor is compatible with the PDP-15 peripherals and the peripheral processor is compatible with the PDP-11 peripherals.

## CONFIGURATION GUIDE

The XVM systems can be configured to support all software available for the PDP-15. In addition the XVM can be incorporated in multiprocessor configurations with any PDP-11 processor and/or other XVM systems. All PDP-15 peripherals can interface to the I/O processor and PDP-11 peripherals can interface to the Unichannel.

## TYPICAL PRICES

	Purchase Price, \$	Maint \$	Install \$
<b>BUILDING BLOCK CONFIGURATIONS</b>			
XV100-AA/-AB Computer System (all processors [115V, 60Hz/230V, 50Hz])	37,500	410	
Includes, in single-cabinet configuration:			
<ul style="list-style-type: none"> <li>• KP15 central processor</li> <li>• KE15 extended arithmetic element</li> <li>• KW15 real-time clock</li> <li>• PC15 paper tape reader and punch</li> <li>• LA36 keyboard printer</li> <li>• XM15-UJ/-UK memory processor with 32K words of MF15 core memory</li> <li>• KF15 powerfail and automatic restart</li> </ul>			
XV100-BA/-BB Computer System Same as XV100-A except with 64K words of MF15 core memory	46,500	464	
XV100-CA/-CB Computer System Same as XV100-A except with 96K words of MF15 core memory	55,500	518	
XV200-AA/-AB Computer System	57,500	617	
Includes, in two-cabinet configuration:			
<ul style="list-style-type: none"> <li>• XV100-A computer system</li> <li>• PDP-11/10 peripheral processor with 8K words of MM11 core memory</li> <li>• RK15 Unichannel disc system with 1.28M words</li> </ul>			
XV200-BA/-BB Computer System Same as XV200-A except with 64K words MF15 core memory	66,500	671	
XV200-CA/-CB Computer System Same as XV200-A except with 96K words MF15 core memory	75,500	725	
<b>XVM MEMORY PROCESSOR OPTIONS</b>			
XM15-BA/-BB Memory Processor (32K word ME15 memory is prerequisite)	9,000	98	713
Includes:			
<ul style="list-style-type: none"> <li>• Instruction lookahead hardware</li> <li>• Automatic priority interrupt</li> <li>• Memory protect and relocate</li> <li>• Wide address mode hardware</li> <li>• Split segment register</li> <li>• Task accounting clock</li> <li>• 19-inch cabinet</li> <li>• All cables and power supplies</li> </ul>			
XM15-UJ/-UK Memory Processor Same as XM15-B except with 32K words of MF15 core memory	17,500 <sup>(1)</sup>	152	713
XM15-UL/-UM Memory Processor Same as XM15-B except with 64K words of MF15 core memory	26,500 <sup>(1)</sup>	222	713
XM15-UN/-UP Memory Processor Same as XM15-B except with 96K words of MF15 core memory	35,500 <sup>(1)</sup>	276	713
<b>XVM SUPER-UNICHANNEL DISC SYSTEM</b>			
RK15-LE/-LF Memory Processor and Unichannel Disc	35,000	359	916
Includes:			
<ul style="list-style-type: none"> <li>• XM15-UJ/-UK with 32K word MF15 memory</li> </ul>			

# DIGITAL EQUIPMENT CORPORATION — XVM SYSTEM REPORT

## TYPICAL PRICES (cont.)

	Purchase Price, \$	Maintenance \$		Purchase Price, \$	Maintenance \$
• PDP-11/10 with 8K word of MM11 memory			Software(3):		
• KW15 real-time clock			XVM/DOS Operating System(2)	2,000	
• RK11-E disc control and RK05 disc drive with 1.28M words storage			Est. Software Installation and 1-year Services	3,000	
• Interprocessor interrupt link			XVM Graphics System for Architectural Design (ARK II(4))	116,075	
• Shared memory adapter			Components:		
<b>TYPICAL XVM CONFIGURATIONS</b>			XVM-200-A Computer System with 32K Core	57,500	
XVM/DOS or XVM/RSX (Minimum System)	72,600(2)		DEctape and Control	10,100	
Components:			GT15 Graphics Processor with 17-inch Display	24,000	
XVM-200 Computer System	57,500		VW01 Writing Tablet and Control	3,780	
DEctape and Control	10,100		VT05 Video Display Terminal	2,795	
Software:			LT15 Terminal Interface	500	
XVM/DOS-BOSS Operating System <sup>2</sup>	2,000		LV11 Electrostatic Printer/Plotter	12,400	
Est. Software Installation and 1-year Services	3,000		Software(4):		
XVM/MUMPS (Minimum System)	93,430		XVM/DOS Operating System	2,000	
Components:			Est. Software Installation and 1-year Services	3,000	
XVM-100 Computer System	37,500		XVM Two-Station Graphics System for Computer-aided Design	132,600	
9-track Magtape and Control	14,950		Components:		
RP152 Disc Pack Drive and Control with 10-million words	27,000		XVM-200-B Computer System with 64K Core	66,500	
DC01 Multistation terminal control with 8 lines	6,480		DEctape and Control	10,100	
Software:			GT15 Graphics Processor with 17-inch Display	24,000	
XVM/MUMPS Operating System	4,500		Second GT15 Graphics Processor	24,000	
Est. Software Installation and 1-year Services	3,000		Software:		
XVM Batch/Computational System	102,050		XVM/DOS-BOSS Operating System	2,000	
Components:			XVM/RSX Operating System	3,000	
XVM-200-B Computer System with 64K core	66,500		Software Installation and 1-year Services	3,000	
9-track Magtape and Control	14,950				
LP11 Line Printer	10,500				
CR11 Card Reader	5,100				
Software:					
XVM/DOS-BOSS Operating System	2,000				
Est. Software Installation and 1-year Services	3,000				
XVM/RSX Resource Sharing System with 5 Remote Terminals	109,700				
Components:					
XVM-100-B Computer System with 64K Core	46,500				
9-track Magtape and Control	14,950				
RP152 Disc Pack Drive and Control with 10-million words	27,000				
LT19 Communications Interface with Five Lines	7,000				
Five VT50 Video Terminals (\$1,250 each)	6,250				
Software:					
XVM/DOS-BOSS Operating System	2,000				
XVM/RSX Operating System	3,000				
Est. Software Installation and 1-year Services	3,000				
XVM Graphics System for Printed Circuit Layout (REDAC(3))	96,600(2)				
Components:					
XVM-200-A Computer System with 32K Core	57,500				
DEctape and Control	10,100				
GT15 Graphics Processor with 17-inch Display	24,000				

\* All XVM systems and options are discountable.

### Notes:

- (1) XM15 components replace KA15, KM15, and KT15 hardware, and any MM15 or MK15 memory. Customers presently using this hardware and memory can apply it toward the purchase of an XVM upgrade.
- (2) Add \$3,000 for XVM/RSX operating system and services.
- (3) REDAC applications software is sold and supported by REDAC SOFTWARE Ltd., Newtown, Tewkesbury; Gloucestershire GL20 HE; England. Phone: Tewkesbury (0684) 294161. Telex: 43108. In the U.S., contact REDAC, Inc., 225 Great Road, Littleton MA 01776. Phone: (617) 486-8751.
- (4) ARK II applications software is sold and supported by Decision Graphics, Inc., One Court Street, Boston MA 02108. Phone: (617)-742-6395.

## HEADQUARTERS

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## DIGITAL EQUIPMENT CORP.

### XVM System Report Update

#### NEW XVM DECDESIGN SYSTEMS

DECdesign systems are a family of dual-processor graphics systems built around both the XVM and the DECsystem-1080 computers. They include full software support. The XVM system includes an XVM (PDP-15-compatible) central processor and a PDP-11/10 peripheral processor. A large-screen refresh display provides true processor interaction: the smaller 16-bit PDP-11 processor controls plotting and printing and performs utility functions while the design work proceeds uninterrupted on the 18-bit PDP-15.

Two configurations are now available: the stand-alone DECdesign 3000 uses an XVM system; the DECdesign 1080 incorporates both XVM and DECsystem computers.

DECdesign 3000 includes an XVM-200 general-purpose processor with 32K to 128K words of memory and a PDP-11/10 peripheral processor with an 8K-word memory to interface to a full range of standard peripherals. This system supports 1.28M to 10.24M words of disc pack storage, a keyboard printer, an electrostatic printer/plotter with incremental x-y plotting, and up to eight seven- or nine-track magnetic tape drives. It can be configured with from one to four (but usually with two) interactive graphics workstations; each workstation includes a graphics processor, 17- or 21-inch CRT and control, light pen, and writing tablet. Software includes the XVM/RSX and XVM/DOS operating systems. Quickscan for hardcopy, and DECsystem-10/XVM communications linkage using Tenlink protocol.

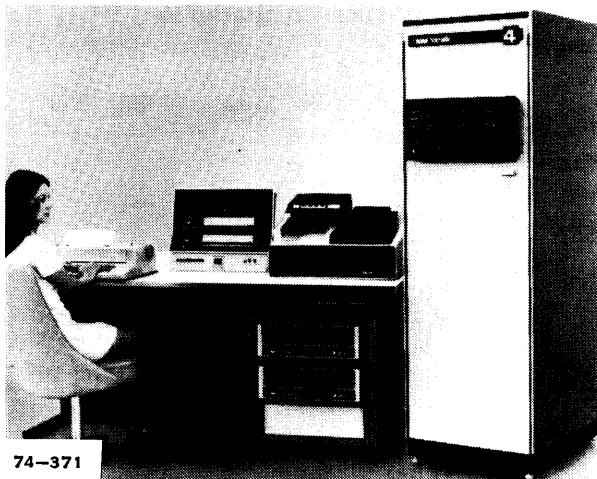
The heart of the DECdesign 1080 system is the large-scale DECsystem-1080 with 256K 36-bit words of memory. Under the TOPS-10 operating system, it can support the DBMS-10 data base management system and COBOL, FORTRAN, and Extended APL languages. This system can include 24 terminals, three tape units, and two dual-processor XVM graphics subsystems. Each subsystem has a complete graphics workstation, an electrostatic printer/plotter, a terminal printer, paper tape reader-punch, and XVM/DOS software. It can be expanded with a full range of peripherals.

DECdesign systems can be used for such complex interactive design applications as printed circuitry, architectural drawing, facilities planning, cartography, mesh and stress analysis, factory layout, and land planning use. Target markets will be the electronics and construction industries, government agencies, architectural and engineering firms, service bureaus, and educational institutions. DECdesign 1080 is particularly well-suited for users with large computational or data base management requirements.

The price of a DECdesign 3000 ranges from \$100,000 to \$250,000; a typical two-station system with 96-word memory costs \$165,000. Rentals for these systems begin at about \$4,000 per month on a 5-year lease-purchase plan, with delivery about 90 days ARO.

A typical DECdesign 1080 is priced at \$1,325,000. Rentals start at about \$30,000 per month with delivery approximately 150 days ARO.





74-371

## OVERVIEW

The Digital Scientific META<sup>®</sup> 4 system is a microprogrammed 16-bit minicomputer aimed at the same markets as IBM's 1130 and 1800 systems. The 4030 and the 4040 models provide complete emulation of IBM's 1130 and 1800 systems, respectively. Faster memory cycle time, faster command execution, higher-performance peripheral subsystems, and microprogrammability combined with lower prices for comparable configurations give the META 4 systems considerably better price/performance ratios than IBM equivalents. All IBM features and comparable peripheral subsystems are available to provide complete compatibility for 1130 and 1800 programs, to the extent that IBM diagnostics can run on a Digital Scientific Computer (DSC) system. Digital Scientific supplies software support for microprogramming and a set of system utilities to operate unique DSC peripherals. Operating systems and all other systems and applications software can be obtained from IBM.

Digital Scientific was started in 1967 as a customized systems house. The META 4 was introduced in 1970 as its only "standardized" product. Although the META 4 processor has been used for other types of applications, emulation of the 1130 and 1800 has continued to be the main marketing focus for the product line.

Digital Scientific has sales and service offices in New York City, Washington (DC), Detroit, Chicago, Dallas, and Los Angeles, with additional service offices in San Francisco, Phoenix, Tucson, Houston, Minneapolis, New Orleans, Pittsburgh, Philadelphia, Baltimore, Flint (MI), Danbury (CT), Clarkesburg (NJ), and Montreal (Canada). Headquarters are in San Diego. Leasing in the United States and Canada is handled by Digital Leasing Company. A distributor agreement with Mitsui and Company provides sales and service in Japan; an entry into western Europe is expected in early 1975.

\*Registered Trademark

## PERFORMANCE AND COMPETITIVE POSITION

Digital Scientific's main competitor in the 1130/1800 replacement market is the General Automation 18/30. The 18/30 is aimed more at 1130 replacement, because there are more 1130 than 1800 installations. IBM 1800 installations are more customized, hence more difficult to replace. General Automation, moreover, provides compatibility only at the CPU instruction level, and uses its own software to achieve comparable operating environments to some extent, but portions of user programs in some installations might have to be adapted. Also, GA does not attempt to provide any type of plug compatibility for peripheral subsystems. Digital Scientific provides compatibility for devices that attach to an IBM SAC channel and a wider range of peripherals.

For certain applications the META 4 has a significant price/performance edge even if GA's peripheral offerings meet software needs. Digital Scientific states that users have cut execution times by factors of 9, 10, and even 20 over the 1130 by using microcode, particularly for programs that use floating-point calculations. The memory cycle times for both DA and GA systems are half that for the IBM systems; consequently both cut execution times by a factor of at least two.

Other factors that increase the system performance for META 4 include overlapped cycle stealing for DMA transfers and the greater capacity of the disc subsystem, which can be expanded from 10M to 20M bytes. Table 1 compares the hardware of the DSC, GA, and IBM computers.

Digital Scientific is a smaller company than General Automation; both are about the same age. The GA system probably has a competitive advantage for small 1130 users who cannot significantly benefit from microcoding on the META 4 simply because the company is larger. In the 1800 replacement market, however, Digital Scientific is in a much stronger position vis-a-vis General Automation because their system is very similar to the IBM 1800, their microcoding capability can substantially improve performance, and they offer a full line of process I/O.

## USER REACTIONS

Digital Scientific META 4 users proclaim it to be a reliable, fast, and price/performance effective system. Most users experienced no problems whatever in converting to the META 4 from their IBM 1130 and 1800 systems. One user said he was "delighted" with the ease of software conversion.

A spokesman for a civil engineering consulting firm handling highway and airport geometry as well as architectural and structural designs for schools, airports, and factories is very happy with the Model 4030. His META 4 improves on the speed and accuracy of this user's former

**Table 1. Digital Scientific META 4: Mainframe Characteristics Compared to GA 18/30 and IBM 1130 and 1800**

MODEL	DSC 4030	DSC 4040	GA 18/30	IBM 1130	IBM 1800
<b>CENTRAL PROCESSOR</b>					
Microprogrammed	Yes	Yes	No	No	No
No. of Instructions	55**	55**	32	29	31
No. of GP Registers	2*	2*	2	2	2
No. of Index Registers	3*	3*	3	3	3
Real-Time Clock	Yes	Yes	Yes	No	No
I/O					
Programmed I/O	Yes	Yes	Yes	Yes	Yes
DMA (no. of channels)	9	9	5	5	3 std, 6 opt
<b>MEMORY</b>					
Cycle Time ( $\mu$ sec)	0.90	0.90	0.96	2.2, 3.6	2.0, 4.0
Parity	Std	Std	Std	Std	Std
Protect	Std	Std	Std	None	Std
ROM (wds)	1K-4K	1K-4K	None	None	None
Core Size (wds)	8K-32K	8K-64K	32K	32K	64K
<b>PERIPHERALS</b>					
Max Speed for					
Card Reader (cpm)	1,000	1,000	1,000	1,000	400
Line Printer (lpm)	600	600	600	600	600
Mag Tape Drive (ips)	75	75	75	None	None
Disc Subsystem					
Capacity (wds/drive)	512K, 10M	512K	512K, 2.5M, 10M	512K	512K, 2.5M
Access Time ( $\mu$ sec)	—	—	45	750	75

\*Assigned from bank of 28 registers.

\*\*34 standard, 16 with optional floating-point firmware.

IBM 1130 and he has had no downtime. This firm ran benchmarks written in FORTRAN using real-number arithmetic and no I/O and found the META 4 outperformed an IBM 370/135. This company had a fast 32K-word memory on the 1130, and FORTRAN programs with no I/O, ran 15 times faster on the META 4 than on the 1130. The firm wanted spooling to a card punch and a plotter. The META 4 system maintained the system cycle time, even with the spooling operations. With the flexibility shown by the META 4 system, the firm plans to add time-sharing terminals to the present 4030. The user investigated the IBM 370/125, DEC's PDP-11/45, the General Automation 18/30, and the option of enhancing the 1130. This user feels the decision to go with Digital Scientific has been a good one for the company.

A consulting firm for aerospace, government, and business agencies uses the META 4 Model 4030 for "scientific number-crunching." The system analyzes data from experimental tests and models physical processes. The META 4 is particularly effective in scientific simulation, handling numerical solutions of partial differential equations. The user looked at the General Automation 18/30, as did most of the users interviewed. This firm was primarily interested in maximum software compatibility with the 1130, which Digital Scientific assures. The user wanted the performance of a Univac 1108 or a CDC 6600

but without the expense of these large systems. The META 4, in this user's estimation, provides comparable performance, a bit slower, and certainly less expensive.

A software house specializing in IBM 1130- and 1800-compatible software uses a Model 4030 for software development and rents the machine to a service bureau for eight hours a day. This user thinks the META 4 is an excellent system, faster, and more capable than an IBM 1130. This user has had the system for over two years and has experienced no problems.

A major advertising agency uses the META 4 Model 4030 for scientific, statistical, and research processing. The firm finds the META 4 quite satisfactory for its needs and faster than the 1130. This system has been installed for over four years; the firm experienced some start-up problems but these have long since disappeared. The firm had minor mechanical problems with the first printer supplied; it was not rugged enough to withstand the beating it was given. Later printers proved more sturdy. One reason this firm chose the META 4 is its IBM-1130 compatibility. Many marketing research companies use 1130-type systems and they share programs among themselves.

Users of the META 4 Model 4040 are generally very pleased with their IBM 1800 emulators. One uses the

Model 4040 in a process control environment. It controls seven or eight laboratory stations handling tests for integrated circuits and frequency selective devices. This company had an IBM 1800 but found it was too slow and required too much space. Price and speed were the deciding factors for the META 4. This firm has recently added 40K bytes of memory and would like to add a high-speed line printer. The user has had problems with the console and systems printers, saying it was rare when both work simultaneously. He considered this a minor problem and stated he had no big problems with the system.

A scientific institute uses the META 4 as a flexible data base management and data acquisition system. This user had found the performance of the META 4 superior to that of his previous IBM 1800. Installed over two years ago, he has experienced no hardware downtime with the META 4 and no software problems. Benchmarks developed for the system ran ten times faster on META 4 than the IBM 1800. This user wanted hardware multiply and divide, which the IBM system did not have and needed to handle complex mathematical equations. The META 4 cost is half the price of the 1800.

A major automobile manufacturer uses the META 4 to test exhaust emission, engine endurance, and carburetor flow. This system was recently installed, so new acceptance tests are still being run. So far, the system is doing well aside from some initial burn-in problems, with no problems with software, previously run on an IBM 1800.

Digital Scientific's maintenance is described as good to excellent by most users; a few users are a little disappointed with response time and competency. One user was impressed with DSC's uniformly bright, knowledgeable, and experienced customer engineers. Another describes the service as competent but response time varies; it is usually within acceptable norms, however. A third user found that the customer engineers lack experience. A simple wiring error was at fault for one user's system failures and repeated visits by DSC brought no solution. This user found the error and corrected it himself.

## CONFIGURATION GUIDE

The basic META 4 processor with an 8K-word memory consists of three models: the 4030 emulates the IBM 1130; the 4040 emulates the IBM 1800; and the 4031 provides for user-supplied emulation. The 4030 and 4040 differ in the standard emulation and I/O backplane controllers; thus, they support different I/O options. The Model 4030 processor options include a real-time clock, hardware (firmware), floating-point arithmetic, 1K-word (16 bits) ROM modules, and a storage access channel (SAC). Six interrupt lines, three index registers, two accumulators, and 39 instructions are standard features. The floating-point option adds 16 instructions for a total of 55.

Model 4040 includes a real-time clock and 14 interrupt levels as standard features, and, like the 4030, it provides ROM modules and floating-point arithmetic options.

Nine DMA data channels are standard features; a set of five OEM channels (to attach non-IBM devices) and a selector channel are available. An I/O typer and controller can supplant the standard console.

Memory can be expanded in 8K-word increments up to 32K words on the 4030 and 64K on the 4040, but memory modules added above 32K words carry an additional field installation charge.

IBM specifies a maximum of 10 I/O devices on an 1130 and up to 12 data channels on an 1800. DS allows up to 28 devices to be attached to either system, but not all devices can go on both. Communications adapters are available for the 4030 for instance, and analog/digital I/O subsystems can be attached to the 4040.

Table 2 lists the peripherals available for the 4030 and 4040 as compared to those available for the 1130 and 1800. Digital Scientific supplies little software for the META 4 because the system is designed to run the software available for the 1130 and 1800. Only the software listed in Table 3 is available.

**Table 2. Digital Scientific: META 4: 4030 and 4040 Peripherals**

Device	DSC 4030	IBM 1130	DSC 4040	IBM 1800
Disc (512K wds)	1448	2310	1448	1810
Disc (100M wds)	1445	NA	NA	NA
M/7 (37 ips)	3412	NA	3412	2401/02
M/7 (75 ips)	3416	NA	3416	2401/02
Card rdr (600 cpm)	3463	2501	3463	NA
Card rdr (1,000 cpm)	3465	2501	3465	NA
Printer Keyboard	NA	NA	4133	1053/ 1816
P/T Reader	3431	1054	3431	1054
P/T Punch	3421	1055	3421	1055
Printer (600 lpm)	3482	NA	3482	NA
Printer (300 lpm)	3484	1403	3484	1443
Plotter	3442	1627	3442	1627
Digital Input	NA	NA	4200	Misc
Digital Output	NA	NA	4232	Misc
Analog Input	NA	NA	4258	1851
Analog Output	NA	NA	4234	1856
Process Interrupt	NA	NA	4214	Misc
Bisync Communica- tions	4101	BSC adapter	NA	NA
Multiterminal Communications Adapter	4108	RPQ	NA	NA
Real-Time Clock	4185	NA	NA	NA
Floating-Point Firmware	9078	NA	NA	NA

## COMPATIBILITY

The META 4 systems are compatible with IBM's 1130 and 1800 computers at the instruction level; they

Table 3. Digital Scientific META 4: Software

Package	Description
Microassembler	Converts symbolic microcode to machine language; requires 8K words of memory, card reader, printer, disc
System Utilities	Object deck punch, ROM debug; require 8K words of memory, disc, card reader, console printer

are also I/O-compatible in that IBM peripherals can be used with the META 4. DSC supplies compatible peripheral subsystems and some compatible controller interfaces to provide better price/performance. Controllers that effectively create 1130 SAC channels or 1800 data channels are attached to the META 4 backplane to allow any IBM controller to be attached.

The IBM 1130 instruction set is a subset of the 1800. Although the 1800 has a fuller complement of peripheral offerings, 1130 and 1800 programs can run on each other's systems if the peripheral environment is the same, and if the 1800 programs do not use instructions unavailable on the 1130. Unlike IBM's 1130, the DSC 4030 has provisions for handling 1800 instructions (among others) on the 1130 emulator.

**MAINTENANCE**

Digital Scientific handles maintenance through area service offices across the United States. The standard maintenance contracts provide for periodical preventive maintenance visits and emergency on-site service. Contracts can cover one, two, or three shifts during the week or on weekends. Users who have purchased systems can also obtain maintenance on an hourly basis instead of through a monthly contract. Provision is not made for a dedicated on-site engineer on a contractual basis although a large remote installation may have the undivided attention of the area engineer.

**TYPICAL PRICES**

Model Number	Description	Monthly Rental \$ YR*	Purchase \$	Monthly Maint. \$
<b>CENTRAL PROCESSOR AND WORKING STORAGE</b>				
<b>Processor and Options</b>				
4001-X(1)	META 4 Basic Processor	—	10,225	—
4011	Memory and I/O Register	—	1,500	—
4012	I/O Register	—	550	—
4013	Double-Bus Accumulator	—	350	—
4025	Scratch-Pad Memory	—	3,000	—
4150	Microprogrammer's Panel Firmware	—	975	—
1425	Read-Only Memory	—	2,725	—
9000	ROM Pattern Boards	—	400	—
9100	Custom Artwork	—	400	—

Model Number	Description	Monthly Rental \$ YR*	Purchase \$	Monthly Maint. \$
9101	Custom ROM Pattern Board	—	25	—
	IBM 1800 Emulator		each	
4040	Basic Processor	1,157	32,800	219
4118	OEM Channels (set of 5)	117	5,000	34
4125	Selector Channel (4040 prereq)	327	9,250	62
9078	Floating-Point Arithmetic	29	1,000	—
4133-0	I/O Typer and Controller	124	3,500	24
	IBM 1130 Emulator			
4030-1	Basic Processor — 8K	1,170	33,175	222
-2	Basic Processor — 16K	1,431	40,575	271
-3	Basic Processor — 32K	1,981	56,200	375
4031	Processor without Emulator	759	21,500	144
4130	Storage Access Channel	43	1,200	8
4185	Real-Time Clock	23	625	5
9078-1	Floating-Point Arithmetic	29	1,000	—
	4031 and 4040 Core Memory Subsystems			
4068-1	8K	351	9,925	67
-2	16K	611	17,325	116
-3	24K	901	25,550	171
-4	32K	1,162	32,950	220
-5	40K	1,475	41,830	279
-6	48K	1,736	45,230	329
-7	56K	2,026	57,455	384
-8	65K	2,286	64,855	433
4069	Auxiliary Core Feature for 4068	283	8,000	54
<b>MASS STORAGE</b>				
<b>For 4040</b>				
1444-2	Disc Subsystem (512K words)(2)	342	9,500	70
1448-2	High-Speed Disc Subsystem (512K)	406	11,500	77
	For 4030			
1445-1	Disc Subsystem (10M words)	775	21,000	175
-2	Additional Drive (20M word total)	604	16,500	132
1448-1	Disc Subsystem (512K words)	406	11,500	77
<b>INPUT/OUTPUT MAGNETIC TAPE(2)</b>				
3410-2A	Single Drive (7-track; 37.5 ips; for 4040 only)	397	11,250	75
3410-2B	Dual Drive (7-track; 37.5 ips; for 4040 only)	608	17,250	115
3412-2A	Single Drive (9-track; 37.5 ips)	405	11,450	77
3412-2B	Dual Drive (9-track; 37.5 ips)	623	17,650	118
3416-2A	Single Drive (9-track; 75 ips)	492	13,950	93
3416-2B	Dual Drive (9-track; 75 ips)	711	20,150	135
	Punched Card(2)			
3463-1/2	Card Reader (600 cpm)	210	6,950	40
3465-1/2	Card Reader (1,000 cpm)	281	7,950	53
3472-2	Controller for IBM 1442 Model 5, 6, or 7	177	5,000	34
3463-1	Card Reader (600 cpm)	210	5,950	40
3472-1	Controller for IBM 1442 Model 5, 6, or 7	105	2,500	33
3474-1	Controller for Univac VIP 1710 Punch	106	3,000	20
	Paper Tape Equipment			
3421-X	Punch (50 cps)	129	3,640	25
3431-X	Reader (400 cps)	111	3,120	21
3432-X	Reader with Spooler Printers(2)	155	4,365	30
3482-2	Printer (600 lpm)	864	24,500	164
3484-1/2	Printer (300 lpm)	442	12,500	84
3482-1	Printer (600 lpm)	731	19,875	163
3486-1	Printer (165 cps) Plotters(2)	362	10,250	69
3443-X(1)	XY Plotter Controller for DSC 3442, Houston DP-1, CalComp 500, and IBM 1627	36	1,000	7





## TYPICAL PRICES (Contd.)

Model Number	Description	Monthly Rental \$ 1YR*	Purchase \$	Monthly Maint. \$
<b>INPUT/OUTPUT MAGNETIC TAPE(2)</b>				
3442	XY Plotter (3443-X required)	177	4,975	34
3444-1	Controller for CalComp 700 Communications (for 4030 only)	53	1,500	10
4101-1	Binary Synchronous Communications Adapter	152	4,275	29
4108-1	Multiple Terminal Communications Adapter (8 lines)	169	4,775	32
0401	Cabinet	27	750	5
4100-X	I/O Chassis Extender	89	2,500	17

**Notes:**

- (1) X = 1 for 1130 Emulation System.  
X = 2 for 1800 Emulation System.  
(2) Subsystems include interface to META 4; generally sub-model 1 refers to 4030 and 2 to 4040.

\*Rental prices include maintenance.  
— Not Applicable.

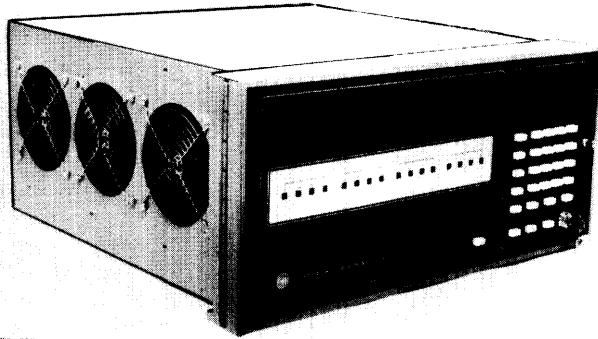
## HEADQUARTERS

Digital Scientific Corporation  
11455 Sorrento Valley Road  
San Diego CA 92121  
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## GENERAL AUTOMATION

# GA-16 Solution Series System Report



75-334

### OVERVIEW

The GA-16 Solution Series consists of four microprogrammed, compatible computer systems — GA-16/110, 220, 330, and 440 — developed for the OEM (original equipment manufacturer) market and for incorporation into systems currently designed around the SPC-16. The GA-16 Series is program compatible with the SPC-16 and surrounds it in power and performance. The low end of the GA-16 Series falls below the SPC-16 and the top end above it. The GA-16/330 is most comparable to the SPC-16/40, while the GA-16/440 is more powerful than either the SPC-16/60 or SPC-16/80.

The big news about the GA-16 Series is the same kind of good news users have been getting from other manufacturers: bigger memories, smaller size, lower cost, COBOL, and a more sophisticated operating system. Soon, the only things mini about minicomputers will be the physical word length, cost, and physical size. Table 1 lists the GA-16 Series mainframe characteristics.

Model 110 is designed as a board-only, load-and-go microcomputer with the CPU and up to 2K words of piggy-back ROM (read-only memory) and RAM (random access memory) able to fit on one board. Model 220 is a 110 processor expanded to support standard DMA and program development facilities. Both models are all-semiconductor systems that can be purchased with or without chassis. Both models can attach a new high-speed "DMT" DMA-type port that is not available on core-based systems.

Model 330, on the other hand, is a slightly faster version of the same processor that can attach conventional 16K-word core memory boards. Model 440 includes a much higher speed bipolar CPU that uses the same core memory as the 330, but memory capacity can expand beyond the

64K-word limit of the other models to a maximum of 1M words (2M bytes).

The GA-16/110, 220, and 330 microprocessor is implemented using LSI nMOS technology. The GA-16/440 microprogrammable processor is implemented with MSI bipolar technology using tri-state Shottky logic. The 110 and 220 use the same nMOS RAM memory, while the 330 and 440 currently use core memory. The nMOS RAM modules are available in three kinds of 4K- and 8K-word modules: without parity, with one parity bit per byte, or with six Error-Detection and Recovery (EDR) bits.

The basic instruction set for all four systems is completely compatible with the SPC-16. Only the GA-16/110 does not have the SPC-16-compatible DMA channel. The basic instruction set includes unsigned integer multiply/divide. An optional high-speed arithmetic unit can provide signed multiply/divide. A separate floating-point processor that connects to the system via the I/O bus is also optional for all systems. Stack processing and argument transfer instructions are optional on the 110, 220, and 330 and standard on the 440.

Currently, operating systems for the new GA-16 Series consist of the SPC-16 operating systems upgraded to handle new features of the GA-16; the new Control IV operating system is for the GA-16/440 only.

Control I — DBOS (Disc-Based Operating System).

Control II — RTX (Real-Time Executive).

Control III — RTOS (Real-Time Operating System).

Control IV — RTMS (Real-Time Multiprogramming System) with memory management for up to 2M bytes of memory.

The GA-16/110 can support Control II, which is designed for real-time dedicated applications. The GA-16/220 and 330 can support Control I, II, and III. The GA-16/440 can support Control I, II, III, and IV. COBOL is now available to run under all program-preparation operating systems; Control I, III, and IV. Models 110 and 220 can also operate with minimal system packages instead of fullblown operating systems; for example, FSOS-16, a freestanding operating system, runs on the 220 and 330.

Peripherals are the same as those for the older SPC-16 Series; both the programmed I/O and DMA busses are

### HEADQUARTERS

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# GENERAL AUTOMATION — GA-16 SOLUTION SERIES SYSTEM REPORT

**Table 1. GA-16 Series: Mainframe Characteristics**

CENTRAL PROCESSOR <sup>(1)</sup>	GA-16/110	GA-16/220	GA-16/330	GA-16/440
<b>Technology</b>	LSI nMOS	LSI nMOS	LSI nMOS	= MIS bipolar & tri-state Shottky
Microprogrammed Control Memory	Yes CROM	Yes CROM	Yes CROM	Yes MSI bipolar
No. of Registers	16	16	16	16
Word Length, bits	16/16 + 2 parity/16 + 6 EDR	16/16 + 2 parity/16 + 6 EDR	16/16 + 2 parity	16/16 + 2 parity
<b>Addressing, bytes</b>				
Direct/Indirect/Indexed Mapping	128K No	128K No	128K No	32K/64K 2M
<b>Instruction Set</b>				
Implementation Types	Firmware Singleword	Firmware Singleword	Firmware Singleword	Firmware Singleword/Doubleword
Number	91+	91 to 116	91 to 116	116 to 130
Floating-Point	Opt	Opt	Opt	Opt
Hardware Stacks	Opt	Opt	Opt	Yes
<b>Instruction Execution Times, <math>\mu</math>sec</b>				
<b>Fixed-Point<sup>(2)</sup></b>				
Add/Subtract	5.0	5.0	4.5	1.6
Multiply <sup>(3)</sup>	23.5	23.5	21.2	11.9
Divide <sup>(3)</sup>	22.5	22.5	20.3	13.6
<b>Floating-Point<sup>(4)</sup></b>				
Add/Subtract				3.1 to 4.7
Multiply	Opt	Opt	Opt	4.8 to 7.9
Divide				7.6 to 8.7
Writable Control Store	No	No	CROM	ROM/PROM
<b>Interrupts</b>				
Levels	64 std; unlimited, opt	64 std; unlimited, opt	64 std; unlimited, opt	64 std; unlimited, opt
Types <sup>(5)</sup>	NI, stack, I/O, external	NI, stack, I/O, external	NI, stack, I/O, external	NI, stack, I/O, external
<b>MAIN STORAGE</b>				
Type	nMOS/bipolar RAM/ PROM/ROM <sup>(6)</sup>	nMOS/bipolar RAM/ PROM/ROM <sup>(6)</sup>	Core	Core
Cycle Time, $\mu$ sec	0.500	0.500	0.720	0.720
Basic Addressable Unit	Word/byte	Word/byte	Word/byte/bit	Word/doubleword/byte/bit
Bytes/Access	2	2	2	2
Cache Memory	No	No	No	No
Capacity, bytes				
Min	256 (RAM) + 1.5 ROM	8K	32K	32K
Max	128K	128K	128K	2M
Increment Size, bytes	8K/16K	8K/16K	32K	32K
Ports/Module	1	1	1	1
Error Checks	Parity, opt/EDR, opt	Parity, opt/EDR, opt	Parity, opt	Parity, opt
Memory Protection	Opt MPP	Opt MPP	Opt MPP	Opt, or MMS
Memory Management	No	No	No	MMS
Interleaving	No	No	No	No
<b>INPUT/OUTPUT</b>				
Max Devices Addressable	64	64	64	64
Programmed I/O, bytes/sec	240K	240K	240K	240K
DMA	DMT type only	Yes, std DMA + DMT	Yes, std DMA	Yes, std DMA
DMA xfer Rate, bytes/sec	4M on DMT	2M DMA; 4M DMT	2M	2.2M
<b>PRICE OF SYSTEM, \$</b>				
No Memory	1,920	2,305	—	—
32K-byte Memory	3,045	3,435	5,250	11,800
64K-byte Memory	5,525	5,915	8,250	75,150

**Notes:**

- (1) GA-16/110, 220, and 330 use same microprocessor.
- (2) Single Precision - one word.
- (3) Unsigned; signed multiply/divide optional.
- (4) Floating-point operations are via a separate processor.
- (5) NI = interrupts that can't be inhibited; stack = stack underflow or overflow; I/O = real-time clock, TTY not busy, or console interrupt; external = peripheral device interrupts.
- (6) Some RAM required; ROM and PROM are piggyback modules on RAM.



completely compatible. Peripherals include discs, magnetic tape, printers, card and paper tape I/O, CRTs, terminal communications interfaces, analog and digital subsystems, and other special purpose units.

Quantity discounts are available for the new systems.

Deliveries of the GA-16/440 began in June 1975. Over 100 have already been produced, and General Automation is in full production of 440 Systems. The GA-16/110 and 220 were first delivered in December 1975. The GA-16/330 was first delivered in January 1976.

The nMOS LSI semiconductor chips for the CA-16/110, 220, and 330 are made by Synertek.

## COMPETITIVE POSITION

The GA-16 Solution Series is an important system for General Automation. It includes replacements for the LSI-16, which was designed around Sapphire On Silicon (SOS) technology, as well as expansion for the SPC-16 line. The LSI-16 was withdrawn from the market early last year because low yields prevented its production at a competitive price. General Automation was probably ahead of competitive SOS technology by one or two years. The GA-16 uses the popular LSI nMOS technology for the 110, 220, and 330, and MSI bipolar technology for the 440. GA's earlier gamble with SOS causes the company to suffer financial losses and reverberations at high management levels. The company has traditionally provided solutions rather than hardware, and it has been especially strong in the automotive industry, which also suffered last year. In the past few years, the company has diversified into data management and real-time systems and into the OEM market. The SOS experience was not a total waste because it gave the company experience in designing a system around semiconductor technology. The GA-16 reflects that experience.

As shown in Tables 2 and 3, the models in the GA-16 Series are price/performance competitive with similar

products from most other manufacturers. The GA-16/110 and 220 will meet the Computer Automation LSI 3/05, as well as the Naked Minis and the Digital LSI-11 in the market place. The GA-16/220 will also compete with the Digital PDP-11/05.

The GA-16/330 competes with the Data General Nova 3, Digital PDP-11/40, Interdata 7/16, and small configurations of Hewlett-Packard HP 21MX. The GA-16/440 has many competitors: Digital PDP-11/45, Data General ECLIPSE and Nova 830, Hewlett-Packard HP 21MX, Computer Automation Megabyte, Modular Computer ModcompII, and Varian Data V70 Series.

Table 2 shows how very competitive comparable systems are, differing for the most part only by about \$40 in price. An exception is the new Texas Instruments 990 line which undercuts the prices of most other minicomputer models. This line marks Texas Instruments' entry into the general-purpose microcomputer/minicomputer market, and it remains to be seen how aggressively TI will develop and market the new systems. The systems shown in Table 3 vary more in price, but much of the variation is represented by built-in features in one system that can be stripped out of another. Which system is the greater bargain depends on a user's specific configuration and software needs.

The Solution Series has been well-planned. Although it contains no radical departures from the SPC-16, it does provide more performance at a lower cost, and enlarges the market in which GA can now compete.

## Configuration Guide

The GA-16/110 is mounted on a single board (7¼ by 11 inches) that contains Control Read-Only Memory (CROM), Register Arithmetic and Logic Unit (RALU), and 1K of RAM. Separate boards are used for 4K or 8K words of nMOS RAM, Memory Parity and Protect (MPP) option, plug-in system power supply, and plug-in auxiliary

**Table 2. GA-16/110 and 220 Compared With Some Competitors**

	Computer Automation LSI-3/05	GA-16/110	Digital LSI-11	GA-16/220	TI 990/4
Word Length, bits	16	16/16 + 2 parity/ 16 + 6 EDR	16	16/16 + 2 parity/ 16 + 6 EDR	16/16 + 1 parity
<b>Instruction Times, <math>\mu</math>sec</b>					
Add	6.0	2.5	3.5 to 12.0	2.5	8.7
Multiply	No	21.0	24 to 64	21.0	21.3
Divide	No	20.0	78	20.0	9.3
Floating-Point Add	No	Opt	42.0	Opt	NA
Floating-Point Multiply	No	Opt	52 to 92	Opt	NA
Floating-Point Divide	No	Opt	151	Opt	NA
Max Memory, bytes	32K	128K	64K	128K	56K
No. of G.P. Registers	8	16	8	16	16
Max DMA Rate, bytes/sec	1.7M	2M	1.7M	2M	DMA not supported
<b>Price, \$</b>					
<b>CPU + Memory</b>					
8K bytes	1,145	1,185	1,536	1,575	800
32K bytes	2,650	3,045	3,411	3,435	2,300
64K bytes	—	5,525	5,911	5,915	—
128K bytes	—	10,485	—	10,875	—

NA = Not available.  
— = Not applicable.

# GENERAL AUTOMATION — GA-16 SOLUTION SERIES SYSTEM REPORT

**Table 3. GA-16/330 and 440 Compared With Some Competitors**

	GA-16/330	GA-16/440	Data General Nova 3	HP 21 MX	Digital PDP-11/45(1)	TI 990/10
Word Length, bits	16/16 + 2 parity	16/16 + 2 parity	16	16	16/16 + 2 parity	16/16 + 1 parity
<b>Instruction Times, <math>\mu</math>sec</b>						
Add	4.6	0.8	1.8	1.9	1.8	3.1
Multiply	21.2	11.1	6.9(2)	12.8	4.7	13.9 to 18.2
Divide	20.3	12.8	7.5(2)	17.0	8.6	7.4 to 10.6
Floating-Point Add	*	3.1 to 4.7*	7.7*	22 to 54*	6.5*	NA
Floating-Point Multiply	*	4.8 to 7.9*	11.3*	48 to 57*	8.2*	NA
Floating-Point Divide	*	7.6 to 8.7*	13.7*	41 to 76*	9.9*	NA
Max Memory, bytes	128K	2M	64K/256K	512K	253,952	2M
No. of G.P. Registers	16	16	4	4	16	16
Max DMA rate, bytes/sec	2M	2M	2M	1.2M	2M	6M
<b>Price, \$</b>						
<b>CPU + Memory</b>						
32K bytes	5,250	11,800	4,400	7,650	23,900	2,975
64K bytes	8,250	15,150	7,100	11,800	32,000	4,975
256K bytes	—	38,750	34,200	36,150	55,500(3)	17,900
512K bytes	—	71,850	—	—	—	33,900

\* Optional, at extra cost.

Notes:

(1) Core Memory assumed, the PDP-11/45 can use faster MOS or bipolar memory.

(2) Operands are unsigned integers on std.

(3) Maximum memory is 253,952 bytes.

power supply for memory retention in case of power shut-down or loss. Memory can consist of RAM, ROM, and PROM. It can range from 512 bytes of RAM to 64K bytes. ROM and PROM are piggyback modules that fit on a RAM module; thus, all systems must have some RAM.

The 220 CPU uses two boards: one for the CROM and one for the RALU. The 220 memory is the same as that used for the GA-16/110. The GA-16/220 has all the features of the GA-16/110 with the following additional features:

- Microconsole ROM.
- TTY Controller and Serial I/O Port.
- SPC-16 DMA Channel.

Both the 110 and 220 can attach a special DMT port that supports two DMA controllers. The port is particularly designed for attaching microprocessor controllers, rather than conventional GA DMA controllers. Both the 110 and 220 can also be housed in GA chassis.

Although the GA-16/330 uses the same microprocessor and is available as a board-only system like the 110 and 220, it is also packaged as a complete, freestanding computing system like the 440. Also like the 440, the 330 is configured with core memory, which has a cycle time of 720 nanoseconds. Core is available in 16K-word boards with or without byte parity. The 330 is offered in three kinds of standard configurations: CPU and memory on a board, packaged without power, or fully packaged. Memory ranges from 8K to 64K bytes.

The 440 is a fully packaged system. The 440 configured with a memory management unit can support up to 2M bytes of core memory. Many features that are optional to lower models, such as stack processing and argument transfer instructions, are standard on the 440.

All processors can address up to 64 peripheral device controllers. Table 4 lists the available peripherals.

**Table 4. General Automation GA-16 Series: Peripherals**

Peripheral Device	Description
<b>MAGNETIC TAPE</b>	
3331, 3332, 3333 Magnetic Tape Subsystems	9-track; 25, 37.5, 75 ips; 800 bpi; 20K, 30K, 60K bytes/sec; 2,400-ft reel
3334, 3335, 3336 Magnetic Tape Subsystems	7-track; 25, 37.5, 75 ips; either 556/800 or 200/556 bpi; 2,400-ft reels; master unit includes 1 drive, can handle 3 more slave drives
<b>FIXED-HEAD DISCS</b>	
3342 Head/Track Storage Drive and Controller	128K or 256K-word capacity; access time 8.5 msec; transfer rate 2 MHz; requires 2 subunit slots
<b>MOVABLE HEAD DISCS</b>	
3341 Disc Storage System	Capacity 3.2M wds/drive; 10 disc surfaces; seek time, 10-65 msec; avg latency, 12.5 msec; master unit has 1 drive; can control up to 3 more slave drives
3343 Disc Storage Subsystem	Capacity 12.8M wds/drive; 20 surfaces; seek time, 10-65 msec; avg latency, 12.5 msec; peak transfer rate; same configuration and submodels as 3341
3346 Disc Storage System	Capacity 2.5M wds/drive; 4 surfaces; seek time, 14-85 msec; avg latency, 20 msec; 1 fixed and 1 removable disc
3347 Disc Storage Subsystem	Capacity 1.25M wds/drive; 2 surfaces; seek time, 14-85 msec; latency, 20 msec; 1 fixed and 1 removable disc
3349 Floppy Disc Subsystem	Capacity 147K wds/drive; 288 wds/sector, 8 sectors/trk, 64 tracks
<b>CONSOLE TYPEWRITERS</b>	
3362 Teletype Model ASR 33	10 cps; includes paper tape read/punch
3363 Teletype Model ASR 35	10 cps; includes paper tape read/punch, uses no subunit slot
<b>PAPER TAPE</b>	
3321 Paper Tape Reader and Controller	8-channel tape; 400 cps
3322 Paper Tape Punch and Controller	8-channel tape; 75 cps
3323 Paper Tape Reader/Punch and Controller	Combines 3321 and 3322; requires 2 slots

**Table 4. (Contd.)**

Peripheral Device	Description
3325 Paper Tape Reader/Punch and Controller	8-channel tape; 300-cps reader; 75-cps punch; fan fold option; requires 1 subunit slot
<b>PUNCHED CARD (std 80-col card)</b>	
3315 Card Reader and Controller	300 cpm; light duty
3316, 17, 18 Card Reader and Controller	400, 600, 1,000 cpm; heavy duty
3314 Card Punch and Controller	35 cpm; includes keyboard
<b>LINE PRINTERS</b>	
3353 Line Printer and Controller	Up to 132 cols/line, 600-lpm; ASCII code
3357 Line Printer/Card Reader and Controller	Printer: 132 cols, 600 lpm; reader: 80-col cards, 400 cpm
3354-1000 Series Low-Speed Printers with Controller (with or without card reader)	132 cols, 7 x 8 dot matrix, 6 lpi, 125 lpm; card reader 300, 400, 600, 1,000 cpm
3354-1200 Series Low-Speed Printers with Controller (with or without card reader)	132 cols, 5 x 7 dot matrix, 6-8 lpi, 200 lpm; card reader, 300, 400, 600, 1,000 cpm
3355 Line Printer/Card Reader and Controller	600-lpm printer, 132 cols; 1,000-cpm card reader (80 cols); print 6-8 lpi option
3358 Line Printer/Card Reader and Controller A/D & D/A Available	600-lpm printer, 132 cols; 6-8 lpi 300-cpm card reader (80 cols)
<b>DATA COMMUNICATIONS</b>	
1561 Asynchronous Communication Controller	For RS232-compatible data set (Bell 103 and 102); full-duplex; 75 to 2,400 bps rates available; 1, 2, or 4 lines
1571 Synchronous Communication Controller	For Bell 201 or equivalent data set; double-buffered, full-duplex; external timing permits wide range of data rates
1581 Series Asynchronous Communications Controller	Interface for full-duplex lines; std rates are same as 1561; 1, 2, or 4 lines
1567 Automatic Calling Unit Subsystem	Provides interface for 4 automatic calling units
1590 Communication Multiplexor Common Equipment	Double-buffered, full-duplex interface for async lines; same baud rates as 1561; up to 16 or 32 lines

Software packages available for the GA-16 and the configurations they require are listed in Table 5.

**MAINTENANCE**

General Automation maintains its own systems out of its 25 sales and service offices in the United States.

**TYPICAL PRICES**

Equipment	Purchase Price \$	Packaged w/o Power	Fully Packaged
<b>GA-16/110</b>	1,185		
1 Board, CPU	585		
4K wds RAM	620		
Packaged w/o Memory	1,920		
<b>GA-16/220</b>	1,595		
2 Boards, CPU	975		
4K wds RAM	620		
Packaged w/o Memory	2,305		
<b>GA-16/330 CPU Board with Core Memory</b>	Board Only		
4K wds	3,250	4,150	4,450
8K wds	3,650	4,450	4,950
16K wds	3,950	4,950	5,250
32K wds	6,950	7,450	8,250
<b>GA-16/440</b>	W/O MMS	W/MMS	
	16 bits	18 bits	
Basic System with Core Memory			
16K wds	8,950	11,800	
32K wds	11,950	15,150	
64K wds	17,950	21,850	
Core Memory Only			
64K wds of 18-bit core for expansion	16,900		
Floating-Point Processor	5,000		
High-Speed Arithmetic	1,500		

**Table 5. General Automation GA-16 Series: Software**

Model No.	Characteristics	Comments
<b>FSOS-16</b>	Freestanding operating system, job-oriented, tape supported	220, 330, or 440 CPU, 8K-word memory, HSPTR/CR, TTY
<b>Control I</b>	Disc-based operating system	220, 330, or 440 CPU, 16K words of memory, disc, TTY or CRT, card or paper tape reader
<b>Control II</b>	Real-time executive	220, 330, or 440 CPU, 8K words of memory, TTY or CRT, card or paper tape reader
<b>Control III</b>	Real-time operating system; multiprogramming, foreground/background	220, 330, or 440 CPU, 24K words of memory, disc, TTY or CRT, card reader or high-speed paper tape reader
<b>Control IV</b>	Control III system with memory management for system up to 2M bytes	440 CPU, MMS option, 48K words of memory, disc, card reader or high-speed paper tape reader
<b>CAP-16</b>	Basic assembler	CPU, 4K words of memory, TTY
<b>CAP-16M</b>	Macro assembler	CPU, 8K words of memory, TTY
<b>FORTRAN IV Compiler</b>	Extended ANSI specifications; real-time compiler with code optimization	CPU, 12K words of memory, TTY Control I, III, or IV
<b>Commercial FORTRAN Compiler</b>	FORTRAN with COBOL-like extensions, string manipulation	CPU, 12K words of memory, TTY, Control I, III, or IV
<b>BASIC Interpreter</b>	Single-user conversational language, or multiple users, real-time conversational mode	220, 330, or 440 dedicated CPU; 8K, 16K, and 24K words of memory, respectively; disc and TTY can run under Control I, II, III, and IV
<b>COBOL Compiler</b>		Control I, III or IV system







# GENERAL AUTOMATION

## GA-16 Solution Series System Report Update

### Microcomputer-Based Remote Batch Terminal

The General Automation RBT-1 is a new low-cost intelligent remote batch terminal based on the GA-16/220, a 16-bit microcomputer. The RBT-1 can communicate with a remote central computer system at high-speed data transmission rates over either a directly connected line or common carrier lines.

The basic RBT-1 consists of a GA-16/220 processor with 8K words of 16-bit semiconductor RAM. Teletype and controller, controllers and cables for card readers and line printers, all power supplies, and a complete communications emulator package. Emulators are available for IBM 360/20 HASP work stations, CDC-U200 terminals, and Univac 1004 systems.

Three card reader/line printer combinations provide versatility for customizing a terminal to specific user requirements: card reader (285 cards per minute) with printer (200 lines per minute) for data rates of less than 2,400 baud; reader (400 cards per minute) with printer (300 lines per minute) for 4,800 baud operation; and card reader (600 cards per minute) with printer (600 lines per minute) for rates of 7,200 to 9,600 baud. Other options include an 8-character, 24-line CRT and a card punch (35 cards per minute).

The RBT-1 is priced from \$10,800. Delivery is 90 to 120 days ARO (after receipt of order).



### OVERVIEW

The General Automation SPC-12 systems are byte-oriented small minicomputers aimed at communications, industrial automation, and process control applications. The SPC-12 was General Automation's first product (1968). It uses a basic hybrid architecture; data is stored in 8-bit words (bytes), but addresses are 12-bit words developed from doubleword instructions.

The company had intended to extend the life of this line by adding an LSI model that used a unique silicon-on-sapphire (SOS) MOS technology. Unfortunately, however, problems with GA's supplier forced the company to withdraw the product, which had excited the interest of the minicomputer market because of its technological advances. GA continues to supply SPC-12 and LSI-12/16 systems to current OEM customers but the company's main computer is its SPC-16 line. Table 1 summarizes the mainframe characteristics.

### PERFORMANCE

The SPC-12 computers enjoyed considerable success during their early years, supplying the foundation on which General Automation built its reputation. They will undoubtedly be sold for some time to OEM manufacturers who use the mini as the base for their own systems.

It is clear that the SPC-16 will supplant the SPC-12 product line for new customers. The only other major 12-bit system that remains on the market is Digital's popular PDP-8, which has remained viable because of the phenomenal volume of software that accompanies it.

### User Reactions

An OEM manufacturer making automatic electronic insertion equipment chose the SPC-12 system over Digital, Data General, and other major minicomputers because of the system's size and reliability, its price and, most important, General Automation's willingness to help him with his problems. He felt that General Automation was particularly strong on support and responsiveness to the customer's individual needs — "they try harder" — and in the five years that he has used the SPC-12, he has been very pleased with the computer and with his relationship with General Automation.

### CONFIGURATION GUIDE

The SPC-12 processor has three submodels which differ in the maximum memory that can be housed in the chassis and the number of slots available for attaching subunit controllers. The 12/10 has a maximum memory size of 16K words (bytes) and no internal provisions for attachment of controllers. The 12/15 has a maximum memory size of 8K words (bytes) and provisions for the internal attachment of up to seven controllers. The 12/20 has a maximum memory size of 16K words (bytes) and

**Table 1. A Comparison of Specifications of General Automation Computers**

MODEL NUMBER	SPC-12	SPC-16	18/30
<b>CENTRAL PROCESSOR</b>			
No. Programmable Registers	7	8 std, 8 opt	15
Addressing (no. of wds)			
Direct	4K	32K	32K
Indirect	16K	32K	32K
Indexed	16K	32K	32K
With Paging	—	64K	—
Instruction set			
Number (std; opt)	52	78; 5	32(2)
Decimal Arithmetic	No	No	No
Floating Point	Sub-routine	Opt	Sub-routine
Priority Interrupt Levels	1-64	64	8-61
<b>MAIN STORAGE</b>			
Type	Core	Core	Core
Cycle Time (μsec)	2.16	1.44; 0.960; 0.800(1)	0.960
Basic Addressable Units			
	8-bit word; 16-bit double-word	Word, byte, bit	Word
Bytes/Access	1	2	2
Min Capacity (bytes)	4K	8K	16K
Max Capacity (bytes)	16K	128K	64K
Increment sizes (bytes)	4K; 8K	8K	8K
Parity	No	No	Std
Protect	Opt	Opt	Std
ROM			No
Use	Boot-strap	Program and/or loaders	—
Capacity (wds)	64	128K	—
<b>I/O CHANNELS</b>			
Programmed I/O	Yes	Yes	Yes
DMA Channels (No.)	Opt	Opt (8)	5
Multiplexed I/O	DMT	No	No
Max Transfer (wds/sec)			
Within Memory (K bytes)	460	173; 260; 320(1)	260
Over DMA (K bytes)	460	700; 1,040;	833
DMT	460 (burst) 100 (inter-leave)	1,250(1)	

(1) Submodels 40(45), 60(65), and 80(85) respectively.  
(2) Additional instruction forms for double precision.

provisions for the internal attachment of up to 19 controllers. All can be configured with 4K or 8K words of memory without impacting the number of available slots for peripherals. A Teletype interface, control panel, parallel and serial I/O, interrupt line, and power supply are standard. A ROM TTY bootstrap loader, memory protect, DMA channel, high-speed I/O access, power fail/automatic restart, and relative time clock/operations monitor alarm can all be added as options. All except the latter two items can be installed in the field; none require a processor slot except the DMA channel, which requires one slot.

# GENERAL AUTOMATION — SPC-12 SYSTEM REPORT

**Table 2. General Automation SPC-12: Peripherals**

Model Number	Description
<b>Teletypes</b>	
1362/63	ASR 33/35, 10 cps
<b>Minicontrollers</b>	
1411	Digital Differential Input for 16 digital inputs
1412	Buffered bipolar power drive for 16 power drives
1413/14	Generalized Input/Output Buffers, 16 bits
1431	Digital Input Relay Receiver to 16 isolated relay coils
1432	Buffered Contact Output for 16 Form A outputs
1441	Analog I/O, 12 bits, 3.3 msec conversion
1451	High Level Input MUX 16 channels
1452	High Level Differential MUX, 8 channels
1453	Low Level Differential MUX, 8 channels
1481	Analog Output Holding Amplifier, 8 channels
<b>Communications</b>	
1541/1551	Bell 103A2 Controller, 110-300 baud, 1551 has 801 ACU
1542/1552	Bell 202C2 Controller, 1,000-9,600 baud, 1552 has 801 ACU

Peripherals for the SPC-12 consist of Teletypes, communication devices, and a series of process minicontrollers (see Table 2). SPC-12 minicontrollers are pre-engineered to eliminate redundant electronics and to permit economical field installations, expansion, and servicing.

The SPC-12 system requires three boards for the CPU, 4K words of memory, and electronics. The enclosure is 5.25 by 17.5 by 20 inches. The basic SPC-12 system weighs less than 30 pounds.

The software packages available for the SPC-12 are listed in Table 3.

## HEADQUARTERS

General Automation, Inc.  
1055 S. East Street  
Anaheim CA 92805

**Table 3. General Automation SPC-12: General-Purpose Software**

Package	Characteristics
<b>LANGUAGE PROCESSOR</b>	
Conversational Assembly System (CAS)	Single-pass absolute assembler with on-line correction
<b>UTILITIES</b>	
PGS Loader/Puncher	Outputs selected areas of memory in object format; loads its own output or output from assemblers or memory load builder
Debug Test and Verify	For processor, memory, peripherals, controllers
Memory Load Builder	Performs program and extended memory linkages, producing absolute or relocatable object code and optional load map
Utilities Text Editor Input/Output System	Output is input to Assembler Calling sequences, std I/O drivers; user can add his own I/O drivers
Arithmetic Library	Floating point, double precision arithmetic, monitor interfacing
Concordance	Cross reference of symbolic names

## TYPICAL PRICES

Model Number	Description	Purchase \$ (1)	Monthly Maint. \$
<b>CENTRAL PROCESSOR AND WORKING STORAGE</b>			
1211-1100	SPC-12/10 (includes 4K words of 8-bit core memory expandable to 16K; 3 hardware index registers; 4 hardware accumulators; control panel; priority interrupt control & interrupt line; 12-bit parallel I/O channel; serial I/O channel with interface for TTY Model 33 or 35; direct memory transfer channel and memory access facility; 5.25-in. high enclosure; cooling; & remote power supply for operation at 115 vac, 47-63 Hz input power)	2,980	30
1211-1200	SPC-12/10 (same as 1211-1100 except has 8K words of memory)	3,850	40
1211-2100	SPC-12/10 (same as 1211-1100 except 230 vac, 47-63 Hz)	2,980	30
1211-2200	SPC-12/10 (same as 1211-1200 except 230 vac, 47-63 Hz)	3,850	40
1215-1100	SPC-12/15 (same as 1100 but expandable to 8K)	3,480	35
1215-1200	SPC-12/15 (same as 1215-1100 except has 8K words of memory)	4,350	45
1215-2100	SPC-12/15 (same as 1215-1100 except 230 vac, 47-63 Hz)	3,480	35
1215-2200	SPC-12/15 (same as 1215-1200 except 230 vac, 47-63 Hz)	4,350	45
1220-1100	SPC-12/20 (same as 1100 except in 10.5-in. enclosure with 19-subunit capacity)	3,980	40
1220-1200	SPC-12/20 (same as 1220-1100 except has 8K-word memory)	4,850	50
1220-2100	SPC-12/20 (same as 1220-1100 except 230 vac, 47-63 Hz)	3,980	40
1220-2200	SPC-12/20 (same as 1220-1200 except 230 vac, 47-63 Hz)	4,850	50

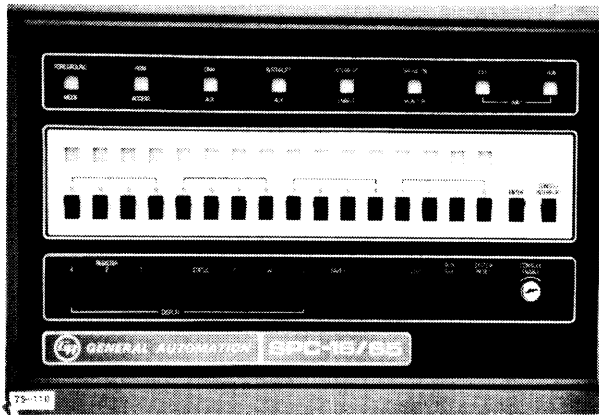


Model Number	Description	Purchase \$ (1)	Monthly Maint. \$
<b>Processor Options (2)</b>			
12XX-0100	Additional 4K Memory	1,600	16
12XX-0200	Additional 8K Memory	2,500	26
12XX-0080	Hardware Bootstrap Loading	250	2
12XX-0090	Memory Protect	225	2
12XX-0001	Direct Memory Transfer Channel	1,500	10
12XX-0002	Memory Access Adapter	500	7
12XX-0004	Relative Time Clock/Operations Monitor Alarm	175	NC
12XX-0008	Power Failure Detection/Automatic Restart	250	NC
1210-0100	System I/O Adapter	400	5
1210-1100	System I/O Adapter and Power Supply	800	12
1210-1209	Power Supply	400	7
1210-2100	System I/O Adapter and Power Supply	800	12
1210-2209	Power Supply	400	7
1210-1110	System I/O Enclosure	800	12
1210-2110	System I/O Enclosure (230 vac, 47-63 Hz)	800	12
1210-0211	Cable Interface Translator	250	3
1210-0212	Function Interface Translator (3)	250	3
1210-0213	Priority Interrupt Expander (3)	500	5
1210-0214	Cable Interface Translator (CIT)	250	3
<b>INPUT/OUTPUT</b>			
<b>Console Teletypewriter</b>			
1362-0500	Teletype Modification Kit for ASR-33	25	—
1362-1000, 1	System Console TTY (ASR-33, 115 vac, 50/60 Hz)	1,250	35
1362-2000	System Console TTY (ASR-33, 220 vac, 50 Hz)	1,350	35
1362-6210	TTY Controller (TTC) (with ASR-33)	500	5
1363-0500	TTY Modification Kit for ASR-35	75	—
1363-1000, 2000	System Console TTY (ASR 35)	4,500	62
1363-6210	TTY Controller (TTC) (for use with ASR-35 half duplex)	500	5
<b>DATA COMMUNICATIONS</b>			
<b>Bell System Data Set Controllers (requires 1210 System I/O Adapter) (3) (4) (5)</b>			
1541-112A	103A2 (& 801 Automatic Calling Unit ACU, half-duplex; requires 2 subunit slots)	720	10
1541-122A	103A2 (& 801 ACU; full-duplex; requires 3 subunit slots)	1,020	15
1542-112B	202C2 and 801 ACU (half-duplex; 4-wire; requires 2 subunit slots)	720	10
1542-122B	202C2 and 801 ACU (full-duplex; 4-wire; requires 3 subunit slots)	1,020	15
1551-112A	103A2 (half-duplex; requires 2 subunit slots)	720	10
1551-122A	103A2 (full-duplex; requires 3 subunit slots)	1,020	15
1552-112B	202C2 (half-duplex; requires 2 subunit slots)	720	10
1552-122B	202C2 (full-duplex; requires 3 subunit slots)	1,020	15
<b>Data Set Interconnection Cable</b>			
1541-7100	For 1541-112A	250	NC
1541-7200	For 1541-122A	400	NC
1542-7100	For 1542-112B	250	NC
1542-7200	For 1542-122B	400	NC
1551-7100	For 1551-112A	250	NC
1551-7200	For 1551-122A	400	NC
1552-7100	For 1552-112B	250	NC
1552-7200	For 1552-122B	400	NC
1901-1100	System Enclosure	1,200	7

**Notes:**

- (1) Most items, excluding system enclosures, power supplies, and TTY units, are subject to discount, RPQ from manufacturer.
- (2) Insert processor identifier in model number. Replace XX with 11 for SPC-12/10, 15 for SPC-12/15, and 20 for SPC-12/20.
- (3) Requires 1 subunit slot, unless noted otherwise. System wiring and test charges are \$100/board. Price shown includes connectors and strain reliefs (cable clamps). If wiring and test are not desired, change 3rd digit of feature code to 4; i.e., 1411-1040. Price remains same.
- (4) Insert baud rate identifier in model number. Replace A with 1 for 110 baud, 3 for 300 baud, and 5 for 150 baud. Replace B with 0 for 1,000 baud, 2 for 1,200 baud, 8 for 1,800 baud, and 4 for 2,400 baud.
- (5) To order controllers without wiring and test or strain reliefs, change 3rd digit of feature code to 0 and reduce price by \$20; i.e., 1541-110A — \$700. Connector on cabling side of controller is included, where applicable.





### OVERVIEW

General Automation introduced the SPC-16 Series as the "super performance" 16-bit industrial automation computers in its family of fourth-generation equipment. Featuring three models that differ only in core speed — 800, 960, or 1,440-nanosecond cycle time per 16-bit word — the company offers each model "bare-bones" OEM (SPC 16/45, 16/65, 16/85) or packaged (SPC 16/40, 16/60, 16/80) with a full set of features for real-time applications. Each SPC-16 model is a dual-speed computer in that its read/write core memories are interchangeable with faster read-only memories operating at 400, 480, and 720-nanosecond cycle time per word, respectively. Construction features multilayer printed circuit boards, medium-scale integrated circuits, and an operating environment of 0°C to 50°C with up to 90 percent relative humidity.

The SPC-16 mainframe characteristics are listed in Table 1.

General Automation recently announced its DM 100 Series, SPC-16/65-based systems. The DM 120 operates as a remote job entry (RJE) workstation that can communicate with other DM 100s or IBM Systems 360/370s. The DM 130 is a data base management system that operates in a multiprogramming/multi-tasking environment. It can support up to four CRT workstations or perform batch compilations or communications in background. A DM 130/2 is a dedicated small business computer available from a distributor network on a turnkey basis. The DM 140, the most powerful system in the series, can support up to 32 remote CRT workstations in the foreground concurrently with background batch compilations or communications.

### COMPETITIVE POSITION

In the past two years GA has been expanding its markets by adding sales and service offices in the United States and abroad and by providing better terms for OEM users. With an installed base of over

**Table 1. General Automation  
SPC-16 Series: Mainframe Characteristics**

CHARACTERISTICS	SPC-16 Series
<b>CENTRAL PROCESSOR</b>	
No. of Internal Registers	8 std; 8 opt
Addressing Direct (no. of words)	32K
Indirect	32K
Indexed	32K
With Paging	128K
Instruction Set Number	78 std; 5 opt
Decimal Arithmetic	No
Floating-Point Arithmetic	Opt
Priority Interrupt Levels	64
<b>MAIN STORAGE</b>	
Type	Core
Cycle Time (msec)	1.44; 0.960; 0.800 (1)
Basic Addressable Unit	Word, byte, bit
Bytes per Access	2
Min Capacity (bytes)	8K
Max Capacity (bytes)	64K; 256K (2)
Increment Size (bytes)	4K, 8K, 16K
Parity	No
Protect	Opt
ROM	
Use	Program and/or loaders
Capacity (bytes)	32K
<b>I/O CHANNELS</b>	
Programmed I/O	Yes
DMA Channels (no.)	Opt (8)
Multiplexed I/O	No
Max Transfer Rate (words/sec)	
Within Memory	173K; 260K; 320K
Over DMA	700K; 1,040K; 1,250K

(1) Cycle times determine whether model number is 40/45, 60/65, or 80/85 respectively.

(2) The first number refers to Models 40, 60, and 80, while the second refers to 4, 65, and 85.

1,000 minicomputers, a substantial amount of system software, new compatible systems to effect cost performance savings, and its edge in the end-user market, GA is a strong competitor.

To encourage OEM users, General Automation rents SPC-16 systems to potential OEM customers while they are designing their systems. OEM users can pass on their leftover warranty time to their customers. In addition, the period for counting time under quantity discount

contracts does not begin until the OEM user makes the first delivery. Quantity discounts of up to 40 percent are available.

GA stresses its strong systems engineering and applications expertise in the face of its competition.

General Automation is apparently going the same system route as other minicomputer manufacturers. Its new DM-100 Series systems (based on SPC-16/65), parallel the M230, M260, and S250 data management systems offered by Hewlett-Packard. Its DM-130/2, offered as a turnkey system via a distributor network, follows the same route Microdata has taken with its Reality system.

In addition, GA is offering a DM-200 Series of systems, functionally similar to the DM 100 Series, but based on the GA-18/30 computer, which has been sold as an IBM System 1130 upgrade since 1968. These systems will also emphasize data management functions, but they are oriented toward industrial applications. The 1130 upgrade system, now called the 230/2, will be distributed on a turnkey basis like the 130/2.

These systems will compete with the small business computers offered by the large mainframe manufacturers, as well as those offered by other minicomputer manufacturers.

**USER REACTIONS**

The SPC-16 users we interviewed were using their systems for a wide variety of applications. A large petroleum manufacturer was using a SPC-16 for high-speed data acquisition of seismologic data used in petroleum exploration — the system had discs magnetic tapes, and punched I/O cards and tape as well as plotters. A manufacturer of discs, tapes, and punched tape peripherals has several operating in engineering and testing applications (using their own peripherals). An OEM manufacturer uses dual processors to run a Telex switching system it markets. Another user had two SPC-16s operating on-line to IBM System 360/65s (special interface) to run an automated warehouse. A branch of a large western university uses a processor with multiplexor as a front end for 20 terminals communicating with a Burroughs 1700; another college was using it as an RJE terminal for an IBM System 370/165.

Users bought their systems for a variety of reasons related to their applications, but one common reason noted by several was the ease of programming. Several users (one of the colleges, the OEM manufacturer, and the petroleum company) were doing their own programming even at the systems level and found the instruction set well suited to their needs. The college found it ideal for communications; the petroleum company believed the Operate On Memory feature on the DMA channel was unique at the time it purchased its systems.

**Table 2. General Automation SPC-16 Series: Peripherals**

Peripheral Device	Description
<b>MAGNETIC TAPE</b>	
3331, 3332, 3333 Magnetic Tape Subsystems	9-track; 25, 37.5, 75 ips; 800 bpi; 20K, 30K, 60K bytes/sec; 2,400-ft reel
3334, 3335, 3336 Magnetic Tape Subsystems	7-track; 25, 37.5, 75 ips; either 556/800 or 200/556 bpi; 2,400-ft reels; master unit includes 1 drive, can handle 3 more slave drives
<b>FIXED-HEAD DISCS</b>	
3342 Head/Track Storage Drive and Controller	128K or 256K-word capacity; access time 8.5 msec; transfer rate 2 MHz; requires 2 subunit slots
<b>MOVABLE HEAD DISCS</b>	
3341 Disc Storage System	Capacity 3.2M wds/drive; 10 disc surfaces; seek time, 10-65 msec; avg latency 12.5 msec; master unit has 1 drive; can control up to 3 more slave drives
3343 Disc Storage Sub-system	Capacity 12.8M wds/drive; 20 surfaces; seek time, 10-65 msec; avg latency, 12.5 msec; peak transfer rate; same configuration and sub-models as 3341
3346 Disc Storage System	Capacity 2.5M wds/drive; 4 surfaces; seek time 14-85 msec; latency 20 msec; one fixed and 1 removable disc
3347 Disc Storage Sub-system	Capacity 1.25M wds/drive; 2 surfaces; seek time 14-85 msec; latency 20 msec; one fixed and 1 movable disc
3349 Floppy Disc Sub-system	Capacity 147K wds/drive; 288 wds/sector, 8 sectors/trk, 64 tracks
<b>CONSOLE TYPEWRITERS</b>	
3362 Teletype Model ASR 33	10 cps; includes pt read/punch
3363 Teletype Model ASR 35	10 cps; includes pt read/punch uses no subunit slot
<b>PAPER TAPE</b>	
3321 Paper Tape Reader and Controller	8-channel tape; 400 cps
3322 Paper Tape Punch and Controller	8-channel tape; 75 cps
3323 Paper Tape Reader/Punch and Controller	Combines 3321 and 3322; requires 2 slots
3325 Paper Tape Reader/Punch and Controller	8-channel tape; 300-cps reader; 75-cps punch; fan fold option; requires 1 subunit slot
<b>PUNCH CARD (std 80-col card)</b>	
3315 Card Reader and Controller	300 cpm; light duty



**Table 2. (Contd.)**

Peripheral Device	Description
<b>PUNCH CARD (std 80-col card) (Contd.)</b>	
3316, 17, 18 Card Reader and Controller	400, 600, 1,000 cpm; heavy duty
3314 Card Punch and Controller	35 cpm; includes keyboard
<b>LINE PRINTERS</b>	
3353 Line Printer and Controller	Up to 132 cols/line, 600-lpm; ASCII code
3357 Line Printer/Card Reader and Controller	Printer: 132 cols, 600 lpm; reader; 80-col cards, 400-cpm
3354-1000 Series Low-Speed Printers with Controller (with or without card reader)	132 cols, 7 x 8 dot matrix, 6 lpi; 125 lpm; card reader 300, 400, 600, 1,000 cpm
3354-1200 Series Low-Speed Printers with Controller (with or without card reader)	132 cols, 5 x 7 dot matrix, 6-8 lpi, 200 lpm; card reader, 300, 400, 600, 1,000 cpm
3355 Line Printer/Card Reader and Controller	600-lpm printer, 132 cols; 1,000-cpm card reader (80 cols); print 6-8 lpi option
3358 Line Printer/Card Reader and Controller	600-lpm printer, 132 cols; 6-8 lpi 300-cpm card reader (80 cols)
A/D & D/A Available	
<b>DATA COMMUNICATIONS</b>	
1561 Asynchronous Communication Controller	For RS232-compatible data set (Bell 103 and 102); full-duplex; 75 to 2,400 bps rates available; 1, 2, or 4 lines
1571 Synchronous Communication Controller	For Bell 201 or equivalent data set; double-buffered, full-duplex; external timing permits wide range of data rates
1581 Series Asynchronous Communications Controller	Interface for full-duplex lines; std rates are same as 1561; 1, 2, or 4 lines
1567 Automatic Calling Unit Subsystem	Provides interface for 4 automatic calling units
1590 Communication Multiplexor Common Equipment	Double-buffered, full-duplex interface for async lines; same baud rates as 1581; up to 16 or 32 lines

## CONFIGURATION GUIDE

All processors can address up to 64 peripheral device controllers. Table 2 lists the available peripherals.

Software packages available for the SPC-16 and the configurations they require are listed in Table 3.

**Table 3. General Automation SPC-16 Series: Software**

Model No.	Characteristics	Comments
BSP-16	Basic systems program package	Minimum configuration: CPU, 4K-word memory and Teletype
FSOS-16	Freestanding operating system, job-oriented, tape supported	Minimum system: CPU, 8K-word memory; HSPTR/CR, TTY
RTX-16	Real-time executive, runs under FSOS-16 or DBOS-II	CPU, 8K words of memory, TTY
DBOS-II	Disc-based operating system	CPU, 16K words of memory, disc, TTY
RTOS-II	Real-time operating system; multiprogramming, foreground/background	CPU, 24K words of memory, disc, TTY
CAP-16	Basic assembler	CPU, 4K words of memory, TTY
CAP-16M	Macro assembler	CPU, 8K words of memory, TTY
FORTRAN IV Compiler	Extended ANSI specifications; real-time compiler with code optimization	CPU, 12K words of memory, TTY
Commercial FORTRAN Compiler	FORTRAN with COBOL-like extensions, string manipulation	CPU, 12K words of memory, TTY
BASIC Interpreter for FSOS, DBOS, and RTOS	Single-user conversational language, or multiple users, real-time conversational mode	Dedicated CPU; 8K, 16K, and 24K words of memory, respectively; disc and TTY

## COMPATIBILITY

The SPC-16 Series computers are all compatible. Programs developed for one system can run on another, except in rare instances where the cycle time is used in some way by the program. The SPC-16 is not program compatible with either the SPC-12 family or the GA 18/30.

## MAINTENANCE

General Automation maintains its own systems out of its 25 sales and service offices in the United States.

## HEADQUARTERS

General Automation, Inc.  
1055 South East St.  
Anaheim CA 92805  
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# GENERAL AUTOMATION — SPC-16 SYSTEM REPORT

## TYPICAL PRICES

Model Number	Description	Purchase Price \$	Monthly Maint. \$
<b>CENTRAL PROCESSORS AND WORKING STORAGE<sup>(1)</sup></b>			
1640-1101	SPC-16/40 Processor (4K 16-bit words of core memory expandable to 16K in chassis; 17 hardware registers including 8 programmable; real-time clock; operations monitor alarm; power fail/auto restart interrupts; system console panel; system console TTY controller; I/O bus port with logic for programmed I/O; unlimited priority interrupts; DMA port with arithmetic and logical functions for opt 0.694-mHz data channel; enclosure; cooling unit and 47-63 Hz power supply; processor cycle time, 1.4 $\mu$ sec)	5,550	60
1640-1102	SPC-16/40 Processor (same as 16/40-1101 except 8K words of core memory, expandable to 32K in chassis; uses 4K, 8K and 16K boards, but only one 4K board/processor)	6,950	70
1640-1202	SPC-16/40 General-Purpose Computer-8K	6,000	70
1640-1203	SPC-16/40 Processor (same as 1640-1202 except has 16K words of core memory)	8,950	82
1640-1304	SPC-16/40 General-Purpose Computer-16K	6,950	82
1640-1305	SPC-16/40 Processor (same as 1640-1202 except has 24K core memory)	10,450	122
1640-1306	SPC-16/40 Processor (same as 1640-1202 except has 32K core memory)	11,450	134
1640-1308	Same as 1640-1305 except has 32K of memory	9,950	134
1640-1309	SPC-16/60 Processor (same as SPC-16/40 except can accept opt 1.04-mHz data chan; memory cycle time is 960 nsec)	6,550	60
1660-1101	SPC-16/60 General-Purpose Computer-4K	6,050	60
1660-1102	SPC-16/60 Processor (same as 16/60-1101 except 8K words of core memory, expandable to 32K in chassis; uses 4K and 8K boards, but only one 4K/processor)	7,950	70
1660-1202	SPC-16/60 General-Purpose Computer-8K	6,400	70
1660-1203	SPC-16/60 General-Purpose Computer-16K	7,250	82
1660-1305	SPC-16/60 General-Purpose Computer-32K	10,250	134
1680-1101	SPC-16/80 Processor (same as SPC-16/40 except can accept opt 1.25-mHz data chan; processor cycle time is 800 nsec)	8,550	70
1680-1102	SPC-16/80 General-Purpose Computer-4K	8,550	70
1680-1202	SPC-16/80 Processor (same as 16/80-1101 except has 8K words of core memory, expandable to 32K in chassis; uses 4K and 8K boards, but only one 4K/processor)	10,150	85
1680-1203	SPC-16/80 General-Purpose Computer-8K	9,050	80
1680-1305	SPC-1680 General-Purpose Computer-16K	12,550	92
1680-1309	Same as 1680-1305 except with 32K of memory	19,550	141
1645-1101	SPC-16/45 Processor (4K words of core memory expandable to 16K in chassis, 32K in chassis with memory expansion board, or 64K with memory expansion chassis; 17 hardware registers including 8 general-purpose; I/O bus port with logic for programmed I/O; unlimited priority interrupts; DMA port with arithmetic and logical functions for opt 0.694-mHz data chan; power failure memory protection; visual real-time debug aid; enclosure; cooling unit and 47-63 Hz power supply; processor cycle time, 1.4 $\mu$ sec)	3,950	55
1645-1102	SPC-16/45 General-Purpose Computer-4K	5,100	60
1645-1202	SPC-16/45 Processor (same as 16/45-1101 except 8K words of core memory expandable to 64K in chassis)	5,350	70
1645-1203	SPC-16/45 General-Purpose Computer-8K	5,550	70
1645-1304	SPC-16/45 Processor (same as 1645-1201 except has 16K memory)	7,350	82
1645-1305	SPC-16/45 General-Purpose Computer-16K	6,500	82
1645-1306	SPC-16/45 Processor (same as 1645-1201 except has 24K memory)	8,850	122
1645-1308	SPC-16/45 Processor (same as 1645-1201 except has 32K memory)	9,850	134
1645-1309	SPC-16/45 General-Purpose Computer-32K	9,500	134
1645-1412	SPC-16/45 with 4K words of 16-bit core using 3 16K-word memory boards (includes memory expansion chassis, memory location display board, power and cables. Expansion to 64K requires additional memory location display board)	14,150	196
1645-1413	SPC-16/45 General-Purpose Computer with 64K Memory Expansion Module	14,250	196
1645-1416	Same as 1645-1412 except with 64K-words of memory, using 4 16K-word memory boards	16,650	253
1645-1417	Same as 1645-1413 except with 64K of memory	17,250	253
1645-1512	Same as 1645-1412 except with 128K-word memory expansion module (allows additional of up to 128K words of memory using either 8K- or 16K-word memory boards)	15,050	219
1645-1516	Same as 1645-1512 except with 64K-word memory using 4 16K-word boards	17,550	271
1645-1520	Same as 1645-1512 except with 80K-word memory using 5 16K-word boards	20,050	323
1645-1524	Same as 1645-1512 except with 96K-word memory using 6 16K-word boards	22,550	375
1645-1528	Same as 1645-1512 except with 112K-word memory using 7 16K-word boards	25,050	427
1645-1532	Same as 1645-1512 except with 128K-word memory, using 8 16K-word boards	27,550	479
1665-1101	SPC-16/65 Processor (same as SPC-16/45 except can accept opt 1.04-mHz data chan; processor cycle time is 960 nsec)	4,950	55
1665-1102	SPC-16/65 General-Purpose Computer-4K	5,600	60
1665-1202	SPC-16/65 Processor (same as 16/65-1101 except has 8K words of 16-bit core memory, expandable to 64K in chassis)	6,350	70
1665-1203	SPC-16/65 General-Purpose Computer-8K	5,950	70
1665-1305	SPC-16/65 General-Purpose Computer-16K	6,800	82
1665-1309	SPC-16/65 General-Purpose Computer-32K	9,800	134
1665-1413	SPC-16/65 General-Purpose Computer with 64K Memory Expansion Module -48K	14,550	196
1665-1417	SPC-16/65 General-Purpose Computer -64K	17,550	253
1685-1101	SPC-16/85 Processor (same as SPC-16/45 except can accept opt 1.25-mHz data channel; processor cycle time is 800 nsec)	6,950	65
1685-1102	SPC-16/85 General-Purpose Computer -4K	8,100	70
1685-1202	SPC-16/85 Processor (same as 16/85-1100 except has 8K words of core memory, expandable to 64K in chassis)	8,550	90
1685-1203	SPC-16/85 General-Purpose Computer-8K	8,600	80
1685-1305	SPC-16/85 General-Purpose Computer-16K	12,100	92
1685-1309	SPC-16/85 General-Purpose Computer-32K	19,100	144
1685-1413	SPC-16/85 General-Purpose Computer with 64K Memory Expansion Module -48K; 800 ns memory cycle time; contains 49,152 words of 16-bit core memory, 1.25 MHz data channel and 115 VAC, 47-63 Hz. Product includes computer, memory expansion chassis, 2 memory location display boards and necessary power and cables.	27,850	206



**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
1685-1417	SPC-16/85 General-Purpose Computer-64K (same as 1685-1413 except with 64K of memory)	34,850	263
	<b>Additional 4K-Word Memory Modules(2)</b>		
16XX-0100	1,440 nsec (for SPC-16/40 or /45)	2,600	26
16XX-0100	960 nsec (for SPC-16/60 or /85)	2,800	26
16XX-0100	800 nsec (for SPC-16/80 or 85)	3,000	30
	<b>Additional 8K-Word Memory Modules</b>		
16XX-0200	1,440 nsec (for SPC-16/40 of/45)	4,000	40
16XX-0200	960 nsec (for SPC-16/60 or/65)	4,200	40
16XX-0200	900 nsec (for SPC-16/8000/185)	4,600	46/45
	<b>Additional 16K- and 128K-word memory modules</b>		
1640-0400	1440 nsec (not for models 1640-1159/2159)	4,600	60
	<b>Processor Options(2)</b>		
16XX-0002	Foreground/Background Processing	250	—
16XX-0004	Extended Processor Option (adds hardware mult/div and foreground/background capability)	500	7
16XX-0015	I/O Enclosure Expansion	N/C	—
16XX-0090	Memory Protect	250	—
16XX-0016	Hardware High-Speed Multiply/Divide (mounts in 2 slots of 1615-1101 I/O expansion chassis)	1,500	16
16XX-0080-0088	Initial Program load (32-wd; semiconductor ROM programmed to load from high speed paper tape reader; TTY; card reader; disc; floppy disc and head-per-track disc)	NC	—
16XX-0070-0077	Initial Program load (64-wd; semiconductor ROM programmed to load from disc; card reader; high-speed paper tape; TTY; floppy disc)	NC	—
	<b>Processor Options (for SPC-16/45, 65, 85 only)(2)</b>		
16XX-0050	Programmer's Console	550	5
16XX-0001	System Console Teletype Controller (for use with ASR 33 or 35)	250	2
16XX-0008	Real-Time Failsafe Group (real-time clock; operations monitor alarm; system safe line; power fail/ auto restart interrupts)	350	5
16XX-0095	Memory Expansion Chassis (control logic for addressing 48K words; can expand memory from 32K to 64K words for — 1200/ — 1300 models; 1645 uses 8K or 16K boards; 1665/1685 use 8K boards)	1,300	10
16XX-0096	Memory Location Display Board (control logic for addressing 48K to 64K words; for systems using 8K boards only)	500	5
	<b>I/O Expansion Options</b>		
1615-X101*	I/O Expansion Chassis (provides chassis, power I/O cable and cable interface card for 19 I/O subunits)	1,200	20
1615-1102/2102	I/O Expansion Chassis 2 (same as 1615-1101/2101 except has unterminated CIT)	1,200	20
1615-0202	Cable Interface Driver (CID; for I/O Expansion on SPC-16/40, 60, 80 processors)	450	20
1615-0203	Cable Interface Translator (signal and control translator within I/O Expansion Chassis; required for I/O Expansion Chassis)	310	10
1615-0208	Multiple High-Speed Data Channel	600	7
1615-0209	Multiple High-Speed Data Channel (8 channels; 16/40/60/80/prereq)	500	7
1615-0210	Computer to Computer Interface (CCIF) (up to 4 computers may be interfaced; 1615-020X prereq)	1,750	30
1615-0211/0212/0213/0214	CCIF Interface Panels (for 16/40/45; 1615-0210 and system enclosure prereq)	310	0
1615-0220	Arithmetic Processing Unit (double precision floating point and integer operations; 1615 expansion chassis-prereq)	5,000	65
1615-1230/1231	Auto Bus Transfer Unit — CIT Unterminated/CIT Terminated	6,000	34
1960-7000	CCIF Interconnection Cable 10 ft	190	0
1960-7001	CCIF Interconnection Cable 25 ft	250	0
1960-7999	CCIF Interconnection Cable, customer specifies length	150 +	0
		\$4/ft over 10 ft.	
	<b>MASS STORAGE</b>		
	<b>IBM 2311 Equivalent Disc Drive</b>		
3341-1000	Drive and Controller for up to 4 drives (3.2M 16-bit words; 45-msec avg access time; includes disc pack)(3)	19,500	125
3341-X110*	Additional Disc Drive	13,500	75
3341-6200	Disc Controller	6,000	NC
	<b>Head-per-Track Disc Drive</b>		
3342-1142-1242	Drive and Controller (128K 16-bit words; 8.5-msec avg access time) (3)	8,000	60
3342-1144-1244	Drive and Controller (256K 16-bit words; 8.5 msec avg access time) (3)	9,300	65
3342-1246	Same as 3342-1242 except 512K words storage	11,500	70
3342-6200	Disc Controller	3,000	NC
3343-1000/1001	Drive and Controller (up to 4 drives per controller; random and sequential access; 12.8M 16-bit words; 45-msec avg access time; includes disc pack) (3)	24,500	175
3343-1110/1111	Additional Disc Drive for 3343-1000/1001	15,500	100
3343-6200	Disc Controller	9,000	NC
	<b>1 Fixed, 1 Removable Pack Disc Drive</b>		
3346-1000	Drive and Controller (up to 4 drives per controller; 2.5M 16-bit words; 60-msec avg access time)(3)	11,000	115
3346-1110	Additional Disc Drive	7,000	100
3346-6200	Disc Controller	4,000	NC
	<b>Floppy Disc Drive</b>		
3349-1000	Drive and Controller (up to 4 drives/controller; capacity of 144K words, 16-bit words; access time 10 ms; includes 1 floppy disc cartridge)	3,750	31

# GENERAL AUTOMATION — SPC-16 SYSTEM REPORT

## TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price \$	Monthly Maint. \$
3349-1110	Disc Drive (includes 1 floppy disc cartridge)	1,250	16
3349-1220	Mounting Hardware and Power Supply (115 vac, 60 Hz)	500	8
3349-6200	Controller (will handle up to 4 disc drives)	2,500	15
<b>INPUT/OUTPUT</b>			
<b>System Console Teletype</b>			
3362-1000/1001	ASR 33 (60 Hz/50 Hz; 115 vac)	1,250	35
3363-1000	ASR 35 (60 Hz; 115 vac)	4,500	62
3363-2000	ASR 35 (50 Hz; 220 vac)	4,600	62
<b>Unidirectional Reader (8-chan paper tape; 400 cps)</b>			
3321-6200	Controller	1,100	NC
3321-1000	Reader and Controller (4)	2,500	18
3322-1000	Punch and Controller (4)	3,000	25
3322-1010	Punch and Controller (with fanfold release and takeup bins) (4)	3,200	25
<b>Reader/Punch</b>			
3323-1000	Reader/Punch and Controller	5,000	40
<b>Punched Card (std 80-col cards; heavy duty; 1615-0209 prereq)</b>			
3316-1000	Reader and Controller (400 cpm)	4,500	35
3318-1000	Reader and Controller (1,000 cpm)	7,000	45
3314-1000	Punch and Controller (with interpreter and keyboard)(3)	11,000	110
<b>Line Printer (600 lpm; up to 132 col)</b>			
3353-1000	Printer and Controller (uses ASCII code)	13,900	110
3353-1001	Line Printer and Controller (with 6/8 lpi option)	14,500	110
3354-1203	Line Printer/Card Reader (200-lpm; printer; up to 132 col; 300-cpm, 80-col reader)	10,400	85
3354-1206	Line Printer/Card Reader (same as 3354-1203 except has 600-cpm reader)	12,400	95
3354-1209	Line Printer/Card Reader (same as 3354-1203 except has 1,000-cpm reader)	13,200	100
3355-1000	Line Printer/Card Reader and Controller (600-lpm printer, up to 132-col and 1,000-cpm reader, 80 col)	19,100	150
3355-1001	Line Printer/Card Reader and Controller (same as 3355-1000 except has 6/8-lpi option)	19,700	150
3356-1001	Line Printer/Card Reader and Controller (same as 3356-1000 except has 6/8-lpi option)	18,900	145
3357-1000	Line Printer/Card Reader (600-lpm printer, 400-cpm reader)	17,000	140
3358-1000	Line Printer/Card Reader and Controller (600-lpm printer, 300-cpm card reader)	16,400	135
3355/3356/3357/3358-6200	Line Printer/Card Reader Controller	3,000	NC
3331-1011	Mag Tape Transport and Controller (controller will handle up to 4 transports; 1 transport included; 25 ips)	10,000	100
3331-6201	MTT Controller (25 ips; will handle up to 4 transports)	4,000	NC
3332-1011	Mag Tape Transport and Controller (controller will handle up to 4 transports; 1 transport included; 37.5 ips)	11,000	100
3333-1011	Mag Tape Transport and Controller (controller will handle up to 4 transports; 1 transport included; 75 ips)	14,000	150
3333-1120	Mag Tape Transport (Add-On) (75 ips)	10,000	125
3334-1002	Mag Tape Transport and Controller: (controller will handle up to 4 transports; 1 transport included; 7-track 25 ips, 556/800 bpi)	10,000	100
3334-6201	MTT Controller (25 ips; will handle up to 4 transports)	4,000	NC
3335-1002	Mag Tape Transport and Controller (controller will handle up to 4 transports; 1 transport included; 37.5 ips)	11,000	100
3335-1112	Mag Tape Transport (Add-On) (37.5 ips)	7,000	75
3335-6201	MTT Controller (37.5 ips; will handle up to 4 transports)	4,000	NC
3336-1002	Mag Tape Transport and Controller (controller will handle 4 transports; 1 transport included; 75 ips)	14,000	150
3336-1112	Mag Tape Transport (Add-On) (75 ips)	10,000	125
3336-6201	MTT Controller (75 ips; will handle 4 transports)	4,000	NC
3371-1001/1002/1003	Plotter and Controller (Drum type incremental plotter, 0.01 inch/step; 0.005 inch/step or 0.1 MM/step; 11 inch carriage)	7,400	60
3372-1001/1002/1003	Plotter and Controller (29.5-inch carriage, 1- or 0.005-inch/step or 0.1 MM/step; includes basic plot package)	10,900	65
3374-1000	Plotter and Controller (34-inch drum; 3 programmable pens; 2,000 steps/sec; .002-inch/step)	16,400	115
3380-1110	A/N Display (RS232; 115 VAC; 60 Hz; split screen with foreground/background intensity control and full editing capability; 1,998-char set; 27 lines; 74 col/line)	3,300	36
<b>DATA COMMUNICATIONS</b>			
<b>Async Controller</b>			
1561-0X01	Async Communication Controller, RS232 (provides 1 double-buffered, full-duplex line between an SPC-16/40/45 series computer and an RS232-compatible async data set)	700	5
1561-0X02	Async Communication Controller, RS232 (provides 2 double-buffered, full-duplex lines)	1,000	7
1561-0X04	Async Communication Controller, RS232 (provides 4 double-buffered, full-duplex lines)	1,500	12
1571-0001	Sync Communication Controller, RS232 (provides 1 double-buffered, full-duplex line)	700	7
1571-0101	Sync Communications Controller, RS232 with Transmit Clock Capability	800	7
1567-0004	Automatic Calling Unit Controller	900	9
1581-0X01	Async Communications Controller, Current Loop	600	6
1581-0X04	Async Communications Controller, Current Loop (same as 1581-0X01 except for 4 full-duplex lines)	1,225	8
1581-2X02	Async Communications controller, Current Loop (same as 1581-2X01 except for 2 full-duplex lines)	775	6
1581-2X04	Async Communications Controller, Current Loop (for 4 full-duplex lines)	1,325	6
1581-3X01	Async Communications Controller, Current Loop, 60 ma (provides interface with limiting resistors for 1 full-duplex line; permits program selection of the number of stop bits, char size, and baud rate; standard baud rates provided are: 75, 110, 134.5, 150, 300, 600, 1,200, 9,600 baud; requires external power)	600	6



**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
1581-3X02	Async Communications Controller, Current Loop, 60 ma (provides interface with limiting resistors for 2 full-duplex lines; permits program selection of the number of stop bits, char size, and baud rate; standard baud rates provided are: 75, 110, 134.5, 150, 300, 600, 1,200, and 9,600 baud; provides external power)	725	6
1581-3X04	Async Communications Controller, Current Loop, 60 ma (provides interface with limiting resistors for 4 full-duplex lines; permits program selection of the number of stop bits, char size, and baud rate; standard baud rates provided are: 75, 110, 134.5, 150, 300, 600, 1,200, and 9,600 baud; requires external power; includes loop back test)	1,225	8
<b>Communication Multiplexor Equipment</b>			
1530-1000/ 1001	DMA Async Communications Multiplexor	5,500	35
1590-1X00	Communication Multiplexor Common Equipment 16 Lines, 115 VAC	3,475	32
1590-1X01	Communications Multiplexor Common Equipment, 32 Lines, 115 VAC	4,000	35
1591-0004	Line Adapter, RS232C Modem Interface	500	6
1592-0004	Line Adapter, Current Loop, 20 ma	400	6

Notes:

NC No Charge — Not Applicable

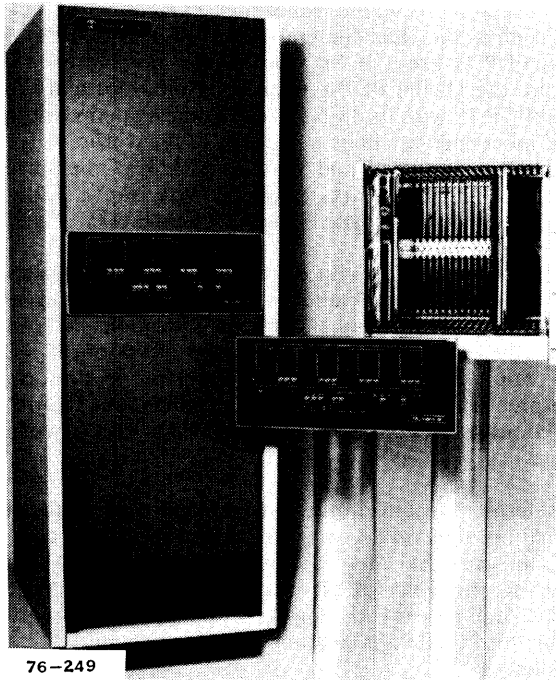
\*X = 2 for 220-vac, 50-Hz operation, otherwise X = 1.

- Processors, most processor options, and controllers for peripheral devices are discountable. RPQ from manufacturer; not available for rental from manufacturer.
- XX = SPC-16 Series processor Models 40, 60, 80, 65, or 85, unless stated otherwise.
- Requires 1615-0209 High-Speed Data Channel.
- Requires 1615-X101\* for use with SPC-16/45, 65, 85 processors.



## HARRIS CORP.

# Slash Series System Report



### OVERVIEW

The Harris Slash series minicomputers are designed for high-speed, real-time, scientific applications requiring minicomputer-to-midcomputer size and power. The six basic models are Slash/1, 3, 4, 5, 6, and 7; a ruggedized Slash/5R model is available for harsh environments.

All Slash series models are 24-bit-word computers; each word can store three bytes. The 24-bit word length provides capabilities unavailable with 16-bit-word computers and vies with 32-bit word machines for many applications. The Slash series models differ from each other primarily in size, speed, and price. Table 1 distinguishes between the models' memory speeds and capacities.

All basic Slash series models are marketed in a modular fashion that appeals particularly to OEM manufacturers and other highly sophisticated users. Many Harris customers are in government installations or universities. However, in addition to the basic Slash series, Harris has introduced two lines of "packaged" systems aimed toward business-oriented mini users. The S100 series is based on the Slash/4 and the S200 on the Slash/7. Both operate under the Vulcan multiprogramming operating system. The S200 series adds virtual memory capabilities to the S100 systems. Vulcan is a demand paging system

that supports time sharing, real-time and batch processing, an impressive array of high-level languages (FORTRAN, COBOL, RPG II, SNOBOL, and FORGO), and a variety of RJE packages. All S100 and S200 software, with the exception of the RJE software, is bundled.

The Slash series was originally marketed by Datacraft as the 6024 systems. Datacraft became a subsidiary of Harris in 1974 and now is part of the Harris Computer Systems Division, which designs and sells core memory modules as well as computers. The Slash series has gained acceptance in several major universities in scientific and time sharing environments. Although Harris emphasizes scientific, control, and data acquisition applications, the Slash series is also marketed for use with communications, optical character recognition, and microfilm processing. The Slash series is marketed in France, West Germany, the United Kingdom, the Netherlands, and Belgium and through eight offices in the United States.

Slash/1 was announced in August 1968 as a 600-nanosecond digital computer. In December 1969 Slash/3, a less expensive, reduced-speed version of Slash/1, was announced. The Slash/3 processor is fully compatible with Slash/1. The Slash/5 was announced in January 1971; it is software and I/O compatible with its predecessors. Slash/5 originally featured a 1,200-nanosecond memory that was limited to 32K words. Today, its memory cycle time is 0.950 nanosecond and memory capacity is 65K words. Slash/5R, a ruggedized version of Slash/5, was delivered in the first quarter of 1973.

Slash/4 was also introduced in 1973; it has a 750-nanosecond cycle time and a 256K-word memory capacity. This system was an important step because it extended the size and power of the systems into the midcomputer range. Slash/4 features bit processing, increased I/O capabilities, and optional multiported semiconductor memory with a 200-nanosecond cycle time. An enhanced version, the Slash/4 VMS, adds virtual memory to the system, forming the basis of the packaged S100 series. Slash/4 is upward software and I/O compatible with the other systems, but virtual memory addressing prevents some Slash/4 software from running on the earlier models.

### HEADQUARTERS

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**Table 1. Slash Series Model Distinctions**

Model	Memory Cycle Time ( $\mu$ sec)	Max Memory Capacity (K words)
Slash/1	0.600	64
Slash/3	1.000	64
Slash/4	0.750/0.200	256
Slash/5	0.950	64
Slash/5R	0.950	64
Slash/6	0.450	256
Slash/7	0.750/0.200	256

Slash/7, initially delivered at the end of 1975, was the first system designed and built under Harris manufacture. Slash/7 has a number of features that enhance throughput over Slash/4 systems. An asynchronous CPU and memory interleaving achieve an effective memory cycle time of 425 nanoseconds on 675-nanosecond core modules. An instruction prefetch feature further expedites instruction execution times. Like Slash/4, the Slash/7 uses a separate I/O processor for high I/O throughput, in keeping with the performance levels of the rest of the system.

Slash/6 was introduced in May 1976 as the intended successor to Slash/4. Slash/6 combines four-bit microprocessor circuits, MOS memory, and an asynchronous single bus to better the performance rate of Slash/4 by about 25 percent. The Slash/6 CPU is a printed circuit board housing six four-bit microprocessor chips that contain the arithmetic logic unit, five general-purpose registers, PROM bootstraps, auxiliary microcoded PROM for instruction decoding and execution, and eight priority interrupts. Hardware floating point is available. The MOS memory on Slash/6 is composed of 18-pin 4K RAM (Random Access Memory) chips with a 600-nanosecond cycle time; 48K bytes of memory can be housed on one board and memory can be expanded to 768K bytes. Single-bit error correction is standard and a memory-save unit optional. With both block-oriented DMA channels for high-speed I/O and an eight-bit programmed I/O channel for low-speed devices, Slash/6 can support up to 32 I/O channels. I/O devices, memory, DMA channels, and all CPU options communicate via the system bus.

Slash/6 is compatible with all Slash/4 and 7 software. This includes four operating systems (disc, tape, resident, and a disc monitor system for concurrent foreground/background processing); six languages (FORTRAN IV, BASIC, MACRO, RPG II, SNOBOL, AND FORGO); six support programs (Sort/Merge, Indexed Sequential File Handler, Interactive Text Editor, Cross-Reference, DEBUG, and Trace); utilities; three remote job entry packages; and host capability for 2780 terminals.

Of the seven models, only Slash/4, 5, 5R, 6, and 7 are actively marketed; Slash/1 and 3 have been superseded. Table 2 lists system specifications.

## PERFORMANCE AND COMPETITIVE POSITION

Harris occupies an almost unique position in the upper range of the minicomputer market. Its Slash series computers use a 24-bit word, while most minicomputer systems, such as the Data General ECLIPSE, HP 3000, and Digital PDP-11 use a 16-bit word. Other notable exceptions are the Digital PDP-8 with its 12-bit word and the Digital PDP-15 with its 18-bit word. Some systems at the top of minicomputer lines are using 32-bit words — for example, Interdata 8/32 and Systems SEL 32. Others use mixed 16-/32-bit words, such as Microdata 3200, MODCOMP IV, Interdata 7/32, and PRIME 300.

Compared with the 16-bit word, the 24-bit word places less constraint on the number of instructions that can be implemented and the number of memory locations that can be directly addressed. In addition, the precision of the 24-bit word allows Slash series computers to perform single-precision operations for many applications that require double-precision operations on a 16-bit-word system.

Furthermore, each 24-bit word can store three bytes of information; thus an 8K-word memory for a Slash computer can store the same amount of data as a 12K-word memory for the typical 16-bit-word mini. At the same time, the Slash computers can compete with larger 32-bit-word systems for certain applications that don't require 32-bit precision.

Slash/4 is the current workhorse of the series, though Slash/6 is expected to replace it. Slash/4 can range in size from a small system with 8K words of memory for under \$25,000 to a medium-scale system with 256K words (768K bytes) of memory at a cost of several hundred thousand dollars. Slash/5 is oriented mainly toward the OEM market. Although it is available by special order in a small configuration with only 4K words of memory, it can be expanded to a rather substantial system with 64K words (192K bytes) of memory. Slash/5R is a ruggedized version of Slash/5 that can withstand vibration and a harsh or abnormal environment. Slash/7 is essentially an optimized Slash/4 with greater processing power, speed, and throughput. Slash/6 combines Slash/4 and Slash/7 capabilities, while incorporating newer technology at a lower cost.

The Slash series competes with the Digital PDP-11/40, -11/45, and -11/70, and the PDP-15; the CDC 1700; HP 21MX and HP 3000; Interdata Models 7/32 and 8/32; Varian V73; Modular Computer System MODCOMP IV; PRIME 300; Data General ECLIPSE; and SYSTEMS SEL 32. All of these systems are designed to operate in real-time environments. For certain applications, such as combined real-time batch and time sharing, Slash/4, 6, and 7 systems can also compete with the Digital PDP-10.



**Table 2. Slash Series Processor Characteristics**

Model	Slash/1	Slash/3	Slash/4	Slash/5	Slash/6	Slash/7
<b>Central Processors</b>						
No. of Programmable Registers	5	5	5	5	5	5
<b>No. of Instructions</b>	596 + SAU, BP	584 + SAU, BP	602 + SAU, BP	592	658 + SAU, BP	602 + SAU, BP
<b>Fixed-Point Arithmetic</b>						
Add/subtract	Hardware	Hardware	Hardware	Hardware	Hardware	Hardware
Multiply/divide	Hardware	Hardware	Hardware	Hardware	Hardware	Hardware
Add time (μsec)	1.2	2.0	1.5	1.9	1.2	0.95
<b>Floating-Point Arithmetic</b>						
	Opt hardware	Opt hardware	Opt hardware	Software	Opt hardware	Opt hardware
<b>Addressing</b>						
Direct (no. of words)	65,536*	65,536*	65,536*	65,536*	65,536	65,536
Indirect	65,536	65,536	262,124	65,536	262,124	262,124
Indexed	65,536	65,536	65,536**	65,536**	65,536**	65,536**
Max no. of I/O Devices	224	224	384	208	Variable	Variable
<b>Priority Interrupt System</b>						
Internal Traps	0-7	0-7	0-7	0-7	0-7	0-7
External Interrupt Levels	4-72	4-24	4-48	4-24	8-24	4-48
<b>Memory</b>						
Type	Core	Core	Core, semiconductor	Core	Semiconductor	Core, semiconductor
Word Length (bits)	24 + 1 parity bit	24 + 1 parity bit	24 + 1 parity bit	24 + 1 parity bit	24 + 5 EDC bits	—
Cycle Time/Word (μsec)	0.6	1.0	0.75 (core); 0.20 (semiconductor)	0.950	0.6	0.75 (core); 0.20 (semiconductor)
<b>Capacity (words)</b>						
Max	65,536	65,536	262,124 (core); 32,768 (SC)	65,536	262,124	262,124 (core); 32,768 (SC)
Min	8,192	8,192	8,192	8,192	16,384	32,768
Increments	8,192	8,192	8,192	8,192	16,384	32,768
Parity	Std	Std	Std	Std	Std	Std
Protect	Opt	Opt	Opt	Opt	Std	Opt
<b>I/O Channels</b>						
No. of Channels	14	14	24	13	32	12
No. of Devices/Channel	16	16	16	16	16	16
Programmed I/O Channel	Std	Std	Std	Std	Std	Std
DMA	Opt	Opt	Opt	Opt	Opt	Opt
No. of DMA Channels (max)	14	14	12	13	16	12
Multiplexed I/O Channel	Opt	Opt	Opt	Opt	Opt	Opt
Max Transfer Rate (bytes/sec)	1,666,667	1,000,000	1,333,333/port (core); 5M/port (SC or IOP with multiple channels)	1,052,636/port (core); 3M/port interleaved	4,540,000 over a UBC channel	1,800,000/port (core); 5M/port (IOP with interleaved channels or SC memory)
<b>Notes:</b>						
* With special instructions						
** Byte indexed to 192K bytes						

Slash/4, 6, and 7 systems, which have optional multiport semiconductor memory, compete most directly with the PDP-11/70 with its four high-speed data channels. Slash/4, 6, and 7 have an optional I/O processor interface that can support four I/O processor channels; I/O transfer rate via their semiconductor memory can be 2.5 million words per second per channel or up to five million words per second for the four I/O processors interlaced. The user can connect directly to the third port of the semiconductor memory and achieve an I/O rate of five million words per second, provided the port is not needed for a second CPU and the first CPU does not require access to the semiconductor memory at that time. Slash/6 can transfer three words between CPU and memory over its 48-bit system bus.

The newer Slash/6 and 7 systems compete in the same market as the Slash/4, but at a higher level. Although Slash/7 has the same memory capacity as Slash/4, it is

considerably faster and more powerful because of hardware features that allow faster instruction execution time, faster effective memory cycle time, and higher I/O throughput. Harris sees the Slash/7 as particularly cost-effective in large simulation applications where several Slash/7s might replace seven or eight smaller and/or slower systems. The Interdata 8/32 and SEL 32 are strong contenders in the simulation market. Slash/6 is aimed at users who require speed, especially I/O speed. Slash/6 is designed for real-time operations and, with block-oriented DMA I/O, is 25 percent faster than Slash/4.

Harris' packaged S100 and S200 series compete with the Digital PDP-11/70, Interdata 8/32 Megamini, and SYSTEMS SEL 32. For sheer processor power, the Harris systems are quite competitive. What sets the S100 and S200 off from these other midcomputers is primarily the software, but the packaging is also different. The other midis don't support RPG II, and only Digital also supplies COBOL as a standard item.

## HARRIS CORP. — SLASH SERIES SYSTEM REPORT

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The S100 and S200 packaged systems run under VULCAN, a sophisticated operating system that supports not only BASIC and FORTRAN IV but also RPG II and COBOL. The software combined with the packaging makes the S100 and S200 more directly competitive with the HP 3000CX Mini Data Centers: HP 50CX, 100CX, 200CX, and 300CX. The HP 3000CX software, which is extensive, is generally unbundled except for the operating system, utilities, and SPL compiler. S100 and S200 software is bundled. The Harris and HP software offering are very similar; both offer an extensive data base management system based on the TOTAL DBMS.

In a complex real-time environment the S200 can be front-ended by an S100. In a similar environment an HP 3000CX or 3000 II is front-ended by an HP 21MX system.

S100 and S200 are less expensive than the HP 3000CX for comparable configurations. This is even more apparent when a substantial amount of software is needed. Certainly the main memory and disc capacities are much larger for the S100 and S200. Both the S100 and S200 systems offer a large variety of peripherals, so the performance can be matched to the application. Plus, the 24-bit word of the S100 and S200 is a distinct advantage over the 16-bit word of the HP 3000CX for certain applications.

Harris has been successful in its chosen markets and is likely to penetrate new ones, especially in the modeling and simulation areas. The Slash systems seem to be good machines for fast simulation computations involving large models. In this market, however, the Harris Assembler and FORTRAN compiler may show need for some improvement. Slash/4, the model most widely marketed at this point, has been well-received, and the faster and cheaper Slash/6 should do as well. With the 24-bit word size and optional 48-bit arithmetic unit, Slash computers offer superior performance in memory sizes significantly lower than most of the competition can offer. The S100 and S200 virtual memory systems reinforce Harris' capability in this direction; they also provide the means for constructing a time sharing network, an area in which Harris has not yet done well.

Harris will probably continue to find its prime market in scientific and engineering applications and perhaps establish a subsidiary market in business simulation. As part of a conglomerate-type organization, Harris' computer division should have little trouble financing the investments necessary to maintain and expand its market share.

### USER REACTIONS

Because most Slash systems are used for aircraft simulation or for research projects, a large number of them are connected in some way to the federal government. Harris has been gradually increasing its proportion of non-government users, however. To date about 425 Slash systems have been installed, and Harris continues to fill orders at the rate of around 25 per year.

Among our contacts were three nongovernment users who had either Slash/3 or 5 systems. One is a major university that has nine Slash systems in operation and one on order. All users have found the systems fast and reliable, and all like the 24-bit word for data manipulation. The systems are used for such varied applications as computer network control, computer-aided instruction, data reduction from satellite, observatory management, ship-based polar exploration, batch processing, data base management, laboratory equipment management, data reduction from a mental retardation center, and a link to an MS 6000 microfilm system. Maintenance for one of the systems is provided through Singer and rated excellent.

**Insurance Company.** A life insurance company has a Slash/4 with virtual memory that is a basic Slash/4, not a Series 100 packaged system. This Slash/4 is used for actuarial research involving high-speed simulation; it was chosen over Data General, Varian, and MODCOMP systems for its speed and word size, but the deciding factor was the Slash/4 virtual memory system, which allows the department to run programs larger than 200K words on a machine with a 48K memory. The user noted that improvements to the operating system come from Harris regularly at about 3-month intervals, and the user is happy with these added features. He noted that the FORTRAN used exclusively for programming is more than adequate, except for being limited to three-dimensional arrays. This Slash/4 was acquired as a replacement for a time sharing service, and the user finds that the Slash/4 halved operating costs and provided full programming freedom to loot.

**University.** A university nuclear physics laboratory is replacing a Slash/4 and a Slash/1 with a Harris Series 110 and plans to acquire a second 110. The systems are used for data acquisition, reduction, and model analysis and are connected to a variety of digital interfaces via both direct I/O channels and DMA channels. This user notes that the Harris computers are relatively easy to interface to experimental equipment. In acquiring its first Slash computer, the laboratory accepted bids from IBM, SDS, DEC, and SEL; competition for the second Slash/110 included DEC and SEL. The Harris computers were chosen over the others for their 24-bit word which allows less core and more speed than competitors, and for their unusually fast 48-bit floating-point unit which provides the necessary accuracy without the need for double-precision computation. This user programs in both Assembly and FORTRAN. He classes the Assembler as somewhat clumsy in executing macro instructions but otherwise adequate, and the DMS operating system as more than adequate for his purposes.

Both users are satisfied with Harris maintenance.

### CONFIGURATION GUIDE

All Slash systems except the 6 and 7 use the same basic configuration: a Slash processor with 8K words of memory (24 bits plus one parity bit per word); hardware multiply,

divide, and square root; priority interrupt system with four external interrupts; five registers, of which three are index registers; eight-bit-wide parallel I/O bus; and basic software. Slash/6 starts at 16K words of semiconductor memory and uses 24 bits plus five Error Detection/Correction (EDC) bits. Slash/7 configurations begin with 32K words of memory and use 24 bits plus two parity bits per word.

Core memory can be expanded in increments of 8K words for all models except Slash/6 and 7, which add memory in 16K-word increments. Core can be purchased in multiple-port (one to five ports) as well as single-port modules. In addition, up to 32K words of the Slash/4 and 7 memory can be multiport (up to five) semiconductor memory with a 200-nanosecond cycle time. Maximum memory capacity is 64K words for all models except Slash/4 and Slash/7, which both have a maximum capacity of 256K words. Slash/6 uses semiconductor memory only, going from 16K to 65K words in increments of 16K words.

An I/O processor interface is available as an option for use with the triple-port semiconductor memory. The I/O processor interface can handle up to four I/O processors.

The following options are available for the Slash series:

- Program restrict and instruction trap (used with memory protect in multiprogramming environment).
- Address trap (address query for software debugging).
- Stall alarm.
- Interval timers.
- Direct Memory Access (DMA) — three types available; up to 16 controllers can interface to each DMA unit.
- Priority interrupt levels — up to a maximum of 24 levels for Slash/3, 5, and 6, 48 for Slash/4 and Slash/7, and 72 for Slash/1.
- Bit Processor (BP) — to retrieve or store bits within a word in memory (unavailable for Slash/5 or 5R).
- Scientific Arithmetic Unit (SAU) — provides floating-point arithmetic (unavailable for Slash/5 or 5R).
- Hardware bootstrap units for paper tape, card reader, disc, and magnetic tape.
- Additional I/O channels — eight-bit-wide channel with up to three integral controllers, dual eight-bit-wide channels, 24-bit-wide channel; maximum of 14 channels for Slash/1 and 3, 24 channels for Slash/4 and Slash/7, and 13 for Slash/5, 5R, and 6.
- I/O processor for Slash/4, 6, and 7.

The Slash/1 and 3 can support 14 DMA channels; the Slash/4 and 7 can support 12 DMA channels; the Slash/5 can support 13 DMA channels; and Slash/6 can support 16 DMA channels.

All models use the same peripheral devices. Mass storage devices include fixed-head disc units, moving-head disc packs, and disc cartridges. Conventional peripherals include Teletype ASR and KSR 33, 35, and 38; paper tape reader and punch; card reader; card reader/punch; card punch/keypunch/verifier/interpreter; and floppy discs and magnetic tape drives. Two drum plotters can also be interfaced, one with a 12-inch and the other a 30-inch drum.

Data communications facilities include a synchronous interface for transmission at 1,200 to 9,600 baud, an asynchronous interface for transmission at 112.5 to 9,600 baud, and a multiplexor that can connect to eight synchronous or 16 asynchronous units via line interface units. Harris also offers a DMA communications multiplexor for Slash/6 and 7 systems. This module controls up to eight asynchronous links and is available for teletype, RS32 terminals or modems, or CRT. Maximum speed is 76,800 bits per second.

Table 3 summarizes specifications for the peripherals.

**Table 3. Slash Series Peripherals**

Device	Description
<b>Terminals</b> 2100/8500/8700 Series 2300 & 8600 Series 2200 Series	ASR, KSR 33/35/38 TTYs; 10 cps CRT displays; 24 lines, 80 char Silent 700 terminals
<b>Punched Cards</b> 3010/20/30	330/600/1,000-cpm readers
<b>Punched Tape</b> 2010/2015 2020/2025 2030/2035 2040/50 2060 2095	300-cps readers 75-cps punches 75-cps punches Reader (300 cps) Spooler Punch (75 cps) Spooler Spooler
<b>Printers</b> 4030/4040 4050/60/70 4700 Series	200-lpm line printers 400/600/1,000-lpm line printers Printer-plotters; 300-1,200 lpm
<b>Magnetic Tape</b> 6040/50/60  6210/20/30  6630 6640 6650 6660/90	9-track; 800/1,600 bpi; 100/150/200 ips  7-track, 556/800 bpi; 100/150/200 ips  7-track; 550/800 bpi; 45 ips 9-track; 800 bpi; 45 ips 9-track; 1,600 bpi PE; 45 ips 9-track; 800/1,600 bpi; 45/75 ips
<b>Discs</b> 5120/5130 5230/5240/5260 5420/40/70  5500 Series	Moving-head discs; 28/56M capacity Cartridge discs; 2.7/5.4/10.8 capacity Fixed discs; 430/860/2,150Kb capacities Disc pack subsystem; 40M bytes/pack
<b>Process I/O</b> 9400	A/D subsystem; to 128 channels; A/D, D/A, digital and high-level analog input systems
<b>Communications</b> 8310  8110 8120/30/40 8400	Up to 16 async, 8 sync lines or 2/1 combination Sync controller; 1,200-9,600 baud Async controller; 112.5-9,600 baud DMA Multiplexor for 8 async lines

The basic software package for the Slash computers includes a Resident Operating System (ROS), MACRO Assembler, FORTRAN support library, utility package hardware diagnostics, and cross-reference package. If magnetic tape is included in the configuration, then a Tape Operating System (TOS) is used instead of ROS.

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For disc systems the Disc Operating System (DOS II) or Disc Monitor System (DMS) controls system operation. DMS supports real-time processing, time sharing, interactive terminals, and batch processing. FORTRAN IV, RPG II, BASIC, FORGO (FORTRAN Compile and Go compiler), and SNOBOL can run under DOS II or DMS. In addition, FORTRAN IV and FORGO can run under ROS or TOS.

Slash/4 and 7 can run under VULCAN, a disc-based, virtual memory system, with appropriate hardware changes to support virtual memory. Configuration requirements for the major software packages are listed in Table 4.

VULCAN requires certain adjustments to system hardware for demand paging. These can be made in the field. A Slash/4 or 7 user who upgrades to run VULCAN is actually changing the Slash system into an S100 or S200 system. Basic S100 and S200 systems include 32K words of memory, a 120-Hertz clock, a stall alarm, a Chain Block Controller (CBC), I/O controller, disc bootstrap, bit processor, CRT, 300 card-per-minute card reader, 200 line-per-minute printer, and a 10.8-million-byte disc.

## COMPATIBILITY

Slash/1, 3, 5, 5R, and 6 systems are completely compatible. Slash/4 and 7 are software and I/O compatible with other Slash systems except for the optional paging scheme (virtual memory configuration) of systems with more than 64K words of memory. The Slash/4 is upward software compatible from the other models. Slash/7 is completely compatible with Slash/4.

RJE packages under Vulcan allow communications compatibility with a large number of computer systems. These emulate the CDC UT-200 for the 6000/7000 series, the IBM 2780 and HASP II M/L for the IBM System/360 and 370, and the Univac 1004 for the 1100 Series.

## MAINTENANCE

Harris supplies contracts for prime-shift, two-shift, or three-shift maintenance. Preventive maintenance and emergency calls during the contracted shift(s) are performed for a monthly fee. Harris can also supply a dedicated on-site service engineer on a contractual basis. If the user does not want a contract, service is available on a per-hour basis (4 hours minimum) plus expenses; or user parts can be shipped to the Florida factory via the nearest service center.

**Table 4. Slash Series Software**

Package	Description
DMS	Disc Monitor System: a foreground multiprogramming system with background batch processing capability; requires console, binary input device (2), 24K words of memory for min system
VULCAN	Virtual memory operating system: disc-based; requires 32K words of memory, Slash/4 & 100 series or Slash/7 & 200 series configuration; console must be CRT, disc, mag tape
DOS	Disc Operating System: uses a disc loader & utilizes a nonresident service area to bring in required modules; requires binary input device; 8K words for min system
TOS	Tape Operating System: uses a mag tape loader; console; 3.5K words for op system, 8K words for min system
ROS	Core Resident Operating System: uses paper tape or card I/O loader; requires 3,500 locations plus I/O areas; console; min system requires 8K-word memory
FORTRAN IV	FORTRAN IV compiler: a superset of ANSI FORTRAN IV; requires 4,600 + $n$ locations ( $n$ = size of the data pool); needs 8K words above operating system, except DMS or VULCAN
FORGO	Compiler (FORTRAN Load and Go): provides extensive debugging features; needs 8K words above min DOS/TOS/ROS; no extra needed for DMS or VULCAN
RPG	RPG II: 8K above TOS or DOS; no extra memory needed for DMS or VULCAN
BASIC	Dartmouth BASIC for user: only available with DMS or VULCAN; no extra memory needed
SNOBOL	Char string manipulation language incl compiler, interpreter, storage allocation; needs 48K words of memory under DMS, TOS, DOS; no extra under VULCAN
MACRO	Assembler: requires 3,100 + $n$ locations ( $n$ = size of symbol table); available in MACRO form when more than 8K system; otherwise use BASIC Assembler
UTILITIES	FORTRAN support library (incl single- and double-precision floating-point routines; utility package provides system software support routines that are not resident in core (source update, etc.); sort/merge; indexed sequential; editor; cross-reference program; hardware diagnostics; object time trace; interactive program debugging aid
TOTAL	Data Base Management System for S100 and S200 systems.

\*Paper tape, magnetic tape, punched card

Note: The appropriate operating system software is provided to meet the system configuration at no charge. Source software is subject to extra charges.

**PRICE DATA**

Model Number	Description	Purchase Price \$	Monthly Maint. *(1) \$
<b>SYSTEMS</b>			
System 110	Series 100 CPU (Slash/4; 96K bytes of core memory; 10.8M-byte cartridge disc with controller; 9-track, 800-bpi, 45-ips mag tape unit with controller; CRT with keyboard, controller, & comm multiplexor)	85,000	760
System 210	Series 200 CPU (Slash/7; 192K bytes of interleaved core memory; 860K-byte fixed-head disc with controller; 40M-byte storage module drive with controller; 9-track, 800-bpi, 45-ips mag tape unit with controller; CRT with keyboard, controller, & comm multiplexor; 600-cpm card reader with controller & stand; 200-lpm line printer with controller; SAU)	159,000	1,375
System 220	Series 200 CPU (Slash/7; 288K bytes of interleaved core memory; 1.7M-byte fixed-head disc with controller; 40M-byte storage module drive with controller; 9-track, 800-bpi, 45-ips mag tape unit with controller; CRT with keyboard, controller, comm multiplexor; 1,000-cpm card reader with controller & stand; 600-lpm line printer with controller; SAU)	189,000	1,910
System 240	Series 200 CPU (Slash/7; 576K bytes of interleaved core memory; 2.1M-byte fixed-head disc with controller; 80M-byte storage module drive with controller; additional 80M-byte storage module drive; 9-track, 800/1,600-bpi, 150-ips mag tape unit with controller; additional 9-track, 800/1,600-bpi, 150-ips mag tape unit; CRT with keyboard, controller, & 2 comm multiplexors; 1,000-cpm card reader with controller & stand; 600-lpm line printer with controller; SAU)	400,000	3,045
<b>CENTRAL PROCESSORS &amp; WORKING STORAGE</b>			
Slash/4-1	CPU (24K bytes of 750-nsec core memory; memory parity, hardware multiply/divide/square root; priority interrupt control system; 4 external priority interrupts; 5 registers, 3 indexable; 8-bit I/O channel, IOC/IC; BP; basic software; in 19-in cabinet)	24,000	165
Slash/4-2	CPU (same as Slash/4-1 except 48K bytes of core)	31,000	215
Slash/5-1	CPU (24K bytes of 950-nsec core memory; memory parity; hardware multiply/divide/square root; priority interrupt control system; 4 external priority interrupts; 5 registers, 3 indexable; 8-bit I/O channel, IOC/IC; basic software; mounted in 19-in cabinet)	16,500	115
Slash/5-2	CPU (same as Slash/5-1 except 48K bytes of core)	21,500	150
Slash/6-1	CPU (48K bytes of MOS memory with error correction; 8 priority interrupts; 120 Hz clock; power-fail shutdown & restart, bootstrap; turnkey panel; power supplies; memory expandable to 192K bytes)	14,500	100
Slash/6-2	CPU (same as Slash/6-1 except memory expandable to 384K bytes)	16,500	115
Slash/7	CPU (96K bytes of 425-nsec core memory; memory parity; hardware multiply/divide/square root; priority interrupt control system; 4 external priority interrupts; 5 registers, 3 indexable; 8-bit I/O channel, IOC/IC; power fail shutdown & restart; 120-Hz clock; bootstrap timing & control; BP; basic software; mounted in 19-in cabinet)	45,000	315
<b>PROCESSOR OPTIONS</b>			
415/715	Scientific Arithmetic Unit (SAU) for Slash/4 & Slash/7	9,900	70
615	SAU for Slash/6	6,000	40
416/716	Program Restrict & Instruction Trap for Slash/4 & Slash/7	1,000	10
616	Program Restrict & Instruction Trap for Slash/6	500	10
417/717	Stall Alarm for Slash/4 & Slash/7	650	10
617	Bit Processor, Stall Alarm & Executive Trap for Slash/6	1,500	10
418/618/718	Interval Timer	750	10
419	Power Fail Shutdown & Restart	500	10
420	Address Trap for Slash/4 & Slash/7	650	10
620	Program Halt & Address Trap for Slash/6	500	10
421	120-Hz Clock	150	10
422/622/722	100-kHz Real-Time Clock	1,500	10
424/724	Run Time Meter	150	10
516	Program Restrict & Instruction Trap	1,000	10
517	Stall Alarm	650	10
518	Interval Timer	750	10
519	Power Fail Shutdown & Restart	500	10
520	Address Trap	650	10
521	120-Hz Clock	150	10
522	100-kHz Real-Time Clock	1,500	10
425-429, 516-519	Hardware Bootstrap	750	10
435-439, 525-539	Additional Hardware Bootstrap	250	10
<b>MEMORY</b>			
401	24K-Byte Memory Increment	7,000	40
402	48K-Byte Memory Increment	12,200	75
415	Scientific Arithmetic Unit (SAU)	9,900	70
703	96K-Byte Memory Increment	25,000	150
710	24K-Byte Semiconductor Memory	26,750	160

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## PRICE DATA (Contd.)

Model Number	Description	Purchase Price \$	Monthly Maint.* (1) \$
<b>MEMORY (Cont'd)</b>			
711	Additional 24K-Byte Semiconductor Memory	22,500	135
404	24K-Byte Core Memory System	12,000	70
405	Additional 24K-Byte Increment (up to 3)	7,000	40
406	48K-Byte Core Memory System	17,200	105
407	Additional 48K-Byte Increment (up to 3)	12,200	75
410	24K-Byte Semiconductor Memory System	26,750	160
411	Additional 24K-Byte Increment	22,500	135
501	24K-Byte Memory Increment	5,000	30
608	48K-Byte MOS Memory with Error Correction	5,500	35
706	48K-Byte Multiport Core Memory System	17,200	100
707	Additional 48K-Byte MP/CM Increment (up to 3)	12,200	75
X47	Chain Block Controller (CBC)	2,200	15
X48	External Block Controller (XBC)	2,000	15
647	Universal Block Channel (UBC)	3,000	20
649	Integrated Block Channel (IBC)	2,000	15
650	Priority Interrupt Group (8 priority interrupts, max 2 groups/CPU)	750	10
X50	Priority Interrupt (1 level)	150	10
X51	Priority Interrupt Expander (above 24 levels)	1,250	10
455/755, 457/757	I/O Processor (IOP) for Multiport Memory	3,500	20
463/763	8-Bit IOC-IC with Multi-CPU Channel Adapter	950	10
464/764	24-Bit IOC with Multi-CPU Channel Adapter	1,450	10
466/766	CBC with Multi-CPU Channel Adapter	2,450	15
470/770	Memory Expansion Chassis (beyond 192K bytes)	7,500	45
670	Memory Expansion Chassis for Slash/6	4,000	NC
484/486, 784/786	Port (IOP) MP/SCM	3,000	20
487 to 489	Port (IOP) MP/CM	1,500	10
676	MOS Data-Save (initial battery backup for 16K words MOS memory)	300	10
677	Additional Data-Save Units (1 for each 16K words)	200	NC
645	Programmed I/O Channel for Slash/6	1,000	10
743	24-Bit IOC	1,200	10
745	8-Bit IOC/Integrated Controller (IOC/IC)	750	10
<b>MASS STORAGE</b>			
<b>Discs</b>			
5120	Moving-Head Disc & Controller (28M bytes)	30,000	300
5130	Moving-Head Disc & Controller (56M bytes)	37,500	375
5230/A	Cartridge Disc with Controller (2.7M bytes; single platter)	10,900	110
5240/A	Cartridge Disc with Controller (5.4M bytes; double platter)	11,500	115
5260/A	Cartridge Disc with Controller (10.8M bytes; double platter)	12,900	130
5410	Fixed-Head Disc with Controller (268K bytes)	14,000	125
5420	Fixed-Head Disc with Controller (430K bytes)	15,500	140
5430	Fixed-Head Disc with Controller (537K bytes)	17,500	160
5440	Fixed-Head Disc with Controller (860K bytes)	20,000	180
5450	Fixed-Head Disc with Controller (1,075K bytes)	23,000	205
5460	Fixed-Head Disc with Controller (1,720K bytes)	26,500	240
5470	Fixed-Head Disc with Controller (2,150K bytes)	30,500	275
5510	Storage Module Drive with Controller (40M bytes)	28,500	255
5530	Storage Module Drive with Controller (80M bytes)	33,500	300
5515	Storage Module Pack (40M bytes)	1,000	NA
<b>INPUT/OUTPUT</b>			
<b>Magnetic Tape</b>			
6210	Controller & MTU (7-track; 556/800 bpi; 100 ips)	38,000	340
6220	Controller & MTU (7-track; 586/800 bpi; 150 ips)	42,000	380
6230	Controller & MTU (7-track; 556/800 bpi; 200 ips)	46,000	415
6240	Controller & MTU (9-track; 800/1,600 bpi; 100 ips)	40,000	360
6250	Controller & MTU (9-track; 800/1,600 bpi; 150 ips)	44,000	395
6260	Controller & MTU (9-track; 800/1,600 bpi; 200 ips)	48,000	430
6630	MTU & Controller for up to 4 Drives (7-track; 800/556 bpi; 45 ips; tension arm; incl cabinet)	11,000	100
6640	MTU & Controller for up to 4 Drives (9-track; 800 bpi; 45 ips; tension arm; incl cabinet)	12,000	110
6650	MTU & Controller for up to 4 Drives (9-track; 800/1,600 bpi [PE]; 45 ips; tension arm; incl cabinet)	16,000	145
<b>Printers/Plotters</b>			
4710	11-in Size, 500 lpm Printer	15,000	150
4730	20-in Size, 300 lpm Printer	17,500	175

**PRICE DATA (Contd.)**

Model Number	Description	Purchase Price \$	Monthly Maint.* <sup>(1)</sup> \$
<b>Paper Tape</b>			
2010	Paper Tape Reader (300 cps) with Controller	2,500	25
2020	Paper Tape Punch (75 cps) with Controller	3,500	30
2030	Paper Tape System (300 cps/75 cps) Reader/Punch with Controller	5,750	50
2130	ASR 33 TTY Unit Only	2,100	50
2140	KSR 33 Unit Only	1,900	35
2150	ASR 35 Unit Only	6,500	80
2160	KSR 35 Unit Only	4,000	50
2170	RO 35 Unit Only	3,900	45
2180	ASR 38 Unit Only	2,750	35
2190	KSR 38 Unit Only	2,400	30
<b>Console Devices*</b>			
2210	ASR 733 (30 cps) with Controller	5,000	65
2220	KSR 733 (30 cps) with Controller	4,000	50
2320	TTY Replacement CRT (24 lines/80 char with keyboard, interface, & controller)	3,200	45
2325	2320 with Hard-Copy Device	6,700	100
<b>Punched Card Equipment</b>			
3010	Card Reader (300 cpm) with Controller	5,000	45
3030	Card Reader (1,000 cpm) with Controller	10,000	90
<b>Line Printers</b>			
4040	Line Printer (200 lpm, 64 char) with Controller	12,200	135
4120	Line Printer (600 lpm, 64 char) with Controller	19,500	175
4125	Line Printer (436 lpm, 96 char) with Controller	21,500	195
4070	Line Printer (1,000 lpm) with Controller	60,000	660
<b>Remote Terminals</b>			
8530	TTY ASR 33	2,100	50
8540	TTY KSR 33	1,900	35
8570	TTY RO 35	3,900	45
8590	TTY ASR 38	2,400	30
8610	Harris-Modified Interactive CRT for Model 8630	5,150	75
8620	Harris-Modified TTY Replacement CRT for Model 8630	2,850	45
8630	Interactive CRT for RS232 Interface	5,150	75
8640	TTY Replacement CRT for RS232 Interface	2,850	45
8720	KSR 733 Terminal	3,500	45
<b>Communications</b>			
8140	Asynchronous Controller for RS232 Terminal or Modem	3,000	30
8310	Communications Multiplexor (handles up to 16 async or 8 sync lines)	3,000	30
8400	DMA Communications Multiplexor for TTY, RS232C Terminal or Modem, or CRT	3,900	

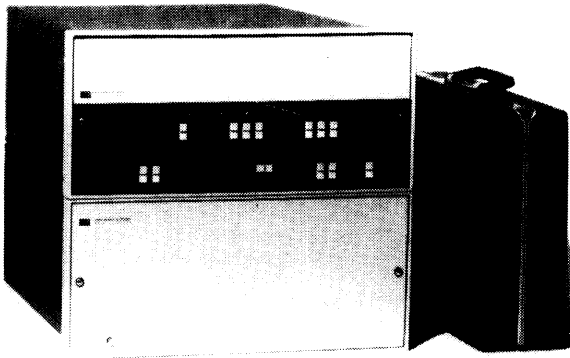
Notes:

\* Require Model 445, 545, 745, or 7310.

(1) Includes on-call service, 7 A.M. to 5 P.M., 5 days per week, with full parts replacement and preventive maintenance. Overtime is at rate of \$32/hour.







74-442

## OVERVIEW

The HP21MX is Hewlett-Packard's latest implementation of its popular 2100 Series of computers. The 21MX is completely upward compatible with the 2100. Virtually all 2100 software can be used on the 21MX, and all 2100 peripherals can interface with the 21MX I/O channels. Features of the 21MX Series include microprogramming ability, semiconductor memories, and a potential address space of 1 million words. The system is intended for both OEM and end-user markets.

The 21MX series initially consists of two models: M/10 or HP 2105A and M/20 or HP 2108A. The M/10 is the smaller of the two models, differing from the M/20 primarily in memory capacity and in control store and I/O expandability.

The central processors provide 128 instructions in the standard set; 80 that emulate the HP 2100 Series, 42 that implement indexing, bit and byte manipulation, and byte and word moves, plus six that perform floating-point arithmetic. The instruction set implemented by microprogrammed firmware is supplied on four ROM modules of 256 locations each. Maximum control store capacity is 4,096 24-bit words. Additionally, writable control store RAMs are optionally available. Each module supplies 256 24-bit locations. The microprocessor instruction set includes 178 microinstructions.

Main memory consists of N-channel MOS semiconductor modules with a cycle time of 650 nanoseconds. Memory parity generation and checking are standard, and memory protect is optional.

Special power failure and brownout protection is standard, providing for memory integrity through a line loss of 10 Hz. Optional stand-by battery power is available to maintain 32K words of memory for two hours if a total power failure occurs. A direct memory access option for two channels is available for high-speed devices.

The system logically structures memory into 1K pages. Through a variety of addressing techniques (direct, indirect, indexing) any location in memory can be addressed.

The optional Dynamic Mapping System (DMS) provides techniques for expanding the system's physical address space to 1 million words. It supplies four sets of 32 registers each — two sets for mapping user and operating system and two sets for data control, permitting scatter/gather I/O operations. The DMS is available only on the M/20. A memory protect feature is included, which supplies both a programmable fence register and page oriented read/write protect.

The 21MX provides 60 levels of chained priority interrupt. The 2105A has four standard I/O channels, and the 2108A has nine standard channels. Both models can expand I/O capacity by 34 channels in increments of 17. The channels support a wide range of high- and low-speed peripherals, TTY and CRT terminals, plus special-purpose gear.

The systems are designed to withstand the same shocks and vibrations as HP's electronic instruments, and are protected against extremely high voltages. They will function in a temperature range of 0° to 55° Centigrade.

Software is provided to perform batch operations, multiprogramming, foreground/background processing, remote job entry, time sharing, and real-time processing. The system supports an assembly language system, FORTRAN, FORTRAN IV, BASIC, and ALGOL. Additionally, a terminal control system for data communications is available, plus a data base management system and over 1,000 canned programs and microcoded routines.

First customer deliveries were made in June 1974.

## COMPETITIVE POSITION

The HP 21MX Series extends the processing capability of a popular line of minicomputers; over 9,000 HP 2100 systems have been installed. The series utilizes modern technology — all semiconductor memory, for example — to provide systems that are smaller, weigh less, consume less power, and cost less than the earlier 2100 systems. Almost all major minicomputer manufacturers are following this same route to modernize their computer lines.

In contrast to Interdata and MODCOMP, which use a 32-bit word for their top-of-the-line systems, Hewlett-Packard has kept the 16-bit word but has incorporated the ability to extend the power of its systems substantially by the simple expedient of adding larger memory capacity and a memory management unit, which generates 20-bit addresses. This allows addressing of 1,048,576 words of physical memory. The feature also provides significant hardware/software control over program and data page allocation with no impact on system cycle time.

The 21MX has a large 4K-word control memory which allows for a fairly broad set of microcoded user

application oriented routines. In the earlier 2100 series, a more limited control store provided throughput improvement over conventional programmed instructions of 10 to 50 times for some applications. Thus, increases of even greater magnitude can also be expected from the 21MX.

Major competition for the HP 21MX will be the Data General Nova/Supernova and ECLIPSE Varian V70 Series, Interdata 7/16 and 7/32, and the DEC PDP-11. Primarily due to its orientation to instrumentation, Hewlett-Packard has generally provided more application-oriented packages than other minicomputer manufacturers.

As processors continue to provide more and more power and performance for less and less money, and plug-compatible peripherals proliferate, minicomputer manufacturers must take the problem-solving system approach to marketing. Less sophisticated users want easy-to-use systems that do a job. This means manufacturers must provide application-oriented systems that can be easily customized for a specific job.

Hewlett-Packard has taken this approach previously with its time-sharing, test and measurement, and distributed processing systems, and is currently expanding it with its data base management and remote job entry systems. The same approach is being followed with the 21MX with its comprehensive range of software including seven operating systems, four languages, special-purpose processors such as data base management and query system and remote job entry, plus an extensive application program library.

The 21MX must be considered a major and serious entry into the minicomputer arena, and it should prove to be the prime contender in many competitive procurements.

**MAINTENANCE AND SUPPORT**

Hewlett-Packard is noted within the industry for its product support. The company maintains 172 field offices in 65 countries throughout the world, including 60 service facilities in the United States and Canada backed by five regional offices. Two service and warranty plans are available under terms of the purchase agreement. One provides for "parts only" warranty for 15 months; a second provides for full services, parts, and labor for 90 days. Follow-on agreements can provide for either guaranteed response times and full service or a per-call time and materials service.

**CONFIGURATION GUIDE**

A minimal 21MX configuration consists of a mainframe and 4,096 words of semiconductor memory. Peripherals can be added to the basic configuration, depending on the requirements of the user. Mainframe characteristics are given in Table 1. A complete list of available peripheral devices is supplied in Table 2.

**Table 1. Hewlett-Packard 21MX: Mainframe Characteristics**

<b>CENTRAL PROCESSOR</b>		
<b>Type</b>	<b>2105A Micro- programmed</b>	<b>2108A Micro- programmed</b>
<b>Control Memory</b>	Yes	Yes
<b>Size</b>	1,024 (24 bits)	1,024 (24 bits)
<b>Use</b>	Firmware	Firmware
<b>No. of Internal Registers</b>	9; additional 16 at micro level	9; additional 16 at micro level
<b>Addressing</b>		
<b>Direct</b>	2,048	2,048
<b>Indirect</b>	Multilevel; 32,768	Multilevel; 32,768
<b>Indexed</b>	Yes	Yes
<b>Instruction Set</b>		
<b>Implementation</b>	Firmware	Firmware
<b>Number (std; opt)</b>	128; 38; 178 micro- instr	128; 38; 178 micro- instr
<b>Decimal Arithmetic</b>	No	No
<b>Floating-Point Arithmetic</b>	Yes, firmware	Yes, firmware
<b>User Micro-programming</b>	Yes	Yes
<b>Priority Interrupt System Levels</b>	60	60
<b>MAIN STORAGE</b>		
<b>Type</b>	SC	SC
<b>Cycle Time (μsec)</b>	0.650	0.650
<b>Basic Addressable Unit</b>	Wd (16-bit)	Wd (16-bit)
<b>Bytes/Access</b>	2	2
<b>Cache Memory</b>		
<b>Min Capacity (bytes)</b>	8,192	8,192
<b>Max Capacity (bytes)</b>	65,563	393,216
<b>Increment Size (bytes)</b>	8K; 16K; 32K	8K; 16K; 32K
<b>Ports/Module</b>	1	1
<b>Error Checks</b>	Parity	Parity
<b>Protection Method</b>	No	Fence reg
<b>Memory Management</b>	No	Opt
<b>ROM</b>	Yes	Yes
<b>Use</b>	Control storage Firmware; loaders	Control storage Firmware; loaders
<b>Capacity</b>	1,024 (24-bit)	1,024 (24-bit)
<b>RAM</b>	Opt	Opt
<b>Use</b>	Writable control Store (WCS)	Writable control Store (WCS)
<b>Capacity</b>	256 (24-bit)	512 (24-bit)
<b>I/O CHANNELS</b>		
<b>Programmed I/O</b>	Yes	Yes
<b>DMA Channels</b>	2	2
<b>Multiplexed I/O (no. subchannels)</b>	4; 32	9; 32
<b>Max Transfer Rate (wd/sec)</b>		
<b>Over DMA</b>	616,666	616,666
<b>Simultaneous Operation</b>	Yes	Yes



**Table 2. Hewlett-Packard 21MX: Peripherals**

DEVICE MODEL NO.	DESCRIPTION
<b>Discs</b>	All Models Moving Head Cartridge, 1 removable, 1 fixed; sectored 2.5M wds, 47.5 access time, xfer rate 126 kws
12960A	
12961A	Same as 12960A except contain only 1 removable platter
12965A	Pack, 11.776M wds/pack, 32 msec access, xfer rate 155 kw/s
<b>Magnetic Tape</b>	
12971A	7-trk, 200/556/800 bpi, 25/37/45 ips
12970A	9-trk, 800 bpi, 25/37/45 ips
12972A	9-trk, 1,600 bpi, 25/37/45 ips
<b>Console</b> (listed under Terminals)	
<b>Paper Tape</b>	
12925A	Pchd PT reader, 500 cps
12926A	Tape punch, 75 cps
12927A	Tape punch, 120 cps
<b>Punched Card</b>	
12986A	Optical mark reader, 200 cpm
12985A	Card reader, 600 cpm
<b>Line Printers</b>	
12980A	200 lpm, 132 cols, 64-char set
12980A-001	150 lpm, 132 cols, 96-char set
12984A	300-1, 100 lpm, 80 cols, 64-char set
12982A	600 lpm, 132 cols, 64-char set
12982A-001	400 lpm, 132 cols, 96-char set
12987A	200 lpm, 132 cols, ROM customized char set
<b>Displays</b>	
7210A	Digital plotter, 20 vctrs/sec
7202A	Graphic plotter, 2 vctrs/sec, 10/15/30 cps
(also see under Terminals)	
<b>A/D Subsystems</b>	
12604A	Data source interface, 32 lines
<b>D/A Subsystems</b>	
12555B	D/A converter, 2 chan, 8 bits/chan
12597A	Duplex register, 8-bit, 48-pin
12566B	Micro-circuit duplex register, 16-bit, 48-pin
12930A	Universal interface, 16-bit
<b>Digital I/O</b>	
12539C	Clock, crystal bases (0.1ms to 1,000 sec Interval)
<b>Data Communications</b>	
12587B	Async data set interface (45-2, 400 bps)
12618B	T/R sync data set interface (9,600 bps)
12589A	Automatic calling unit interface
12531C/D	Async terminal interface (110-2, 400 bps)
12920A	Async multiplexor; 16 dev interfaces, 57-2, 400 baud
12880A	TTY or CRT channel, local or remote, buff/unbuff (110-2, 400 bps)
<b>Terminals Supported</b>	
2754A	TTY ASR 33 (10 cps)
2754B	Heavy-duty TTY ASR 35, (10 cps)
2762A	Term console printer KSR (35 cps, 75 cols)
2762A-006	Term printer KSR (30 cps, 118 cols)
2615A	Char mods CRT buffer 2,000 char
2616A	Pg mode CRT (stores/ 256 25 x 80 pgs)

Users operating under control of any of the operating systems described in Table 3 require (as a minimum) a paper tape reader, a console device such as a TTY, and the system device for the operating system, such as magnetic tape or disc. Beyond these limitations, the user is relatively free to expand the system up to the maximum memory capacity and maximum number of I/O channels — currently 196K words of memory with a potential for 1 million words, and up to 54 directly addressable devices.

The system's basic control memory provides for a maximum of 4,096 words of addressable ROM, the bulk of which is available to the user. In addition, a user can optionally add one (M/10) or two (M/20) modules of writable control store RAM (256 24-bit locations). Both the ROM and RAM facilities provide the user with extremely powerful implementation tools.

The 21MX Series is also available in several preconfigured versions at considerably reduced costs. The M/200 line is oriented towards a business environment;

**Table 3. Hewlett-Packard 21MX: Software**

PACKAGE NAME	DESCRIPTION
Basic Control System (BCS)	Executive monitor providing load, interrupt processing, and I/O drives; memory resident on min system; min config
Magnetic Tape System (MTS)	Batch processing; tape resident; can be used on single tape system; provides job control directives and executive functions
Disc Operating System-III (DOS-III)	Disc-resident batch processor; std executive function plus logical file mgmt and appl prog segmentation; 4,500 wds main mem; 400K bytes disc
Real-Time Executive (RTE)	Core or disc-resident; multi-programming, foreground/background processing; prior prog sched; min config 16K
Time-Sharing System	Extended BASIC interpreter; up to 32 terminals
Language Processors	ASSEMBLY; FORTRAN; FORTRAN IV; BASIC; ALGOL
Special-Purpose IMAGE/2000	DBMS; allows structured data network; query and batch modes; uses min 5.5K memory, 300K bytes disc; will run under DOS-III
Remote Job Entry (RJE)	Remote job interface to OS360; will run under DOS-III
Terminal Control System (TCS)	Multitasking supervisor; up to 32 terminals; requires 6.5 memory
Applications Various	More than 1,000 applications-oriented macro and microcoded routines

the S/200 Series favors a scientific/engineering environment. Both packages provide highly sophisticated levels of data processing. The 21MX/55, a special disc-based configuration, is available for the OEM shop; it is based on M/20 with 32K words of high-density memory and includes 4.9 million bytes of disc cartridge storage.

The 21MX Series also provides facilities for data communication and time-sharing services. As noted in Tables 2 and 3, a wide variety of potential configurations are possible, operating under either the time-shared system or the terminal control system.

**TYPICAL PRICES**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
2124A	OEM Disc System (M/20 processor; 16K X/1 memory; dual channel port controller; 12960A disc subsystem; diagnostic software)	21,500	195
HP21-MX/55-008	8K X/1 Memory	19,400	191
HP21-MX/55-016	16K X/1 Memory	21,500	195
HP21-MX/55-024	24K X/1 Memory	24,000	199
HP21-MX/55-032	32K X/1 Memory	26,100	203
2124A-108	Add 8K X/1 Memory Module	2,500	
2124A-116	Add 16K X/1 Memory Module	4,600	
2124B	OEM Disc System	18,900	189
2124A-204	Add 4K X/2 Memory Module	900	
2124A-208	Add 8K X/2 Memory Module	1,500	
HP MX/65 2125A	DISC computer with M/20 processor; 8K X/2 memory; dual channel port controller and 15 megabytes; 12962A disc subsystem	22,250	181
Options			
2125A-012	Replace M/20 with M/30	900	NC
-016	Replace 8K module with 16K	1,200	NA
-204	Add 4K module	900	+ 2
-208	Add 8K module	1,500	+ 4
Options for 2/24A/B			
2124A-003	Add Fast FORTRAN Processor	1,250	
2124A-004	Add Dynamic Mapping System	1,950	
2124A-005	Add Writable Control Store	1,000	
2124A-006	Add FFP and DMS	2,700	
2124A-008	Replace 16K with 8K	-2,100	
2124A-014	Add Disc Loader ROM	100	
2124A-015	230V/50 Hz	-	
PROCESSORS AND WORKING STORAGE			
HP21-M/10 2105A	Microprogrammable Processor, HP 21-M/10 (supports up to 32K semiconductor memory, provides 4 powered I/O channels and full user microprogramming)	4,150	66
HP21-M/20 2108A	Microprogrammable Processor, HP 21-M/20 (supports up to 32K semiconductor memory; 9 powered I/O channels; opt memory protect and full user microprogramming)	5,300	66
HP M/30-2112A	Microprogrammable processor with 8 memory module slots for up to 128K of memory, fourteen powered I/O channels, and full user microprogramming capabilities	6,200	66
Options for 2105A/2108A			
-003	Fast FORTRAN Processor	1,250	2
-004	Dynamic Mapping System (for 2108A only)	1,950	
-005	Writable Control Store	1,000	9
-006	Dynamic Mapping System and Fast FORTRAN Processor (for 2108A only)	2,700	
-014	Disc Loader ROM	100	-
MEMORY			
2101A	Semiconductor Memory System, HP 21-X/1 (high density 8K- and 16K-word modules)	650	8
2102A	Semiconductor Memory System, HP 21-X/2 (medium density 4K- and 8K-word modules)	500	8
Options for 2101A/2102A			
-001	Dual-Channel Port Controller	750	8
-003	Memory Protect (M/20 only)	500	9
-004	4K Memory Module (for 2102 only)	900	2
-008	8K Memory Module	1,500	4
-016	16K Memory Module (for 2101A only)	4,600	8

**COMPATIBILITY**

The 21MX Series is fully compatible with previous versions of the 2100 line of processors. Virtually all peripherals are interchangeable between the two lines, and all software written for the 2100 line should be convertible to the 21MX with few, if any problems.

**HEADQUARTERS**

Hewlett-Packard Company  
 1501 Page Mill Road  
 Palo Alto CA 94304  
 (415) 493-1501

Model Number	Description	Purchase \$	Monthly Maint. \$
-010	Additional Disc Drive for Subsystem	9,975	95
12961A	790A Cartridge Disc Subsystem (1 removable cartridge disc, moving head; 2.5 megabytes)	11,800	93
-010	Additional Disc Drive	6,775	79
12869A	Disc Cartridge	125	-
12965A	2883A Disc File w/Controller	29,900	157
-020	Additional Disc File as 2nd or 4th Drive	18,000	115
-030	Additional Disc File as 3rd Drive	27,900	152
12868A	Additional Disc Pack	620	-
12610C	Interface for 2766A Fixed-Head Disc Memory INPUT/OUTPUT	4,535	6
2752A	Teleprinter, Modified Teletype ASR-33	2,000	54
2754A	Teleprinter, Modified Teletype ASR-35	6,950	54
2600A	Keyboard Display	3,965	50
2615A	CRT Keyboard Terminal (visual display of input/output 10 to 960 cps)	2,835	32
2616A	CRT/Keyboard Terminal (page mode operation)	4,500	41
2762A	Terminal Printer	4,920	29
-001 or -002	Same as 2762A, 220V/50 Hz, or 240/50V Hz	5,150	29
-006	2762A, Terminal Printer (with kybd, 118 cols)	6,055	29
-007 or -008	Same as 2762A, 220V/50 Hz or 240V/50 Hz	6,280	29
12925A	Tape Reader and Interface	2,295	31
12575C	Tape Winder	100	0
12989A	2894A Card Reader Punch Subsystem	12,450	123
-002	With off-line kybd Punch and Verify	14,250	123
12986A	7261A Optical Mark Reader and Interface	3,775	32
12985A	2892A Card Reader and Interface (600 cpm)	5,665	54
7260A	Optical Mark Card Reader	3,190	30
7261A	Optical Mark Card Reader (automatic feed)	2,760	30
12980A	2610A Line Printer and Interface (200 lpm; 132 cols/line, 64-char set)	14,935	86
-001	2610A-001 Line Printer and Interface (150 lpm, 96-char set, 132 cols/line)	17,035	86
12982A	2614A Line Printer and Interface (600 lpm, 132 cols/line, 64-char set)	30,385	142
-001	2614A-001 Line Printer and Interface (400 lpm, 132 cols/line, 96-char set)	32,960	142
12984A	2767A Line Printer and Interface (300 to 1,100 lpm, 80 cols/line, 64-char set)	13,900	52
12987A	2607A Line Printer and Interface (200 lpm, 132 cols/line)	7,950	2
12982A	2614A Line Printer and Interface (600 lpm, 132 cols/line, 64-char set)	30,385	142
-001	2614A-001 Line Printer and Interface (400 lpm, 132 cols/line, 96-char set)	32,960	142
12984A	2767A Line Printer and Interface (300 to 1,100 lpm, 80 cols/line, 64-char set)	13,900	69
12987A	2607A Line Printer and Interface (200 lpm, 132 cols/line, 64-char set)	7,950	72
-001	2607A-001 Line Printer and Interface (165 lpm, 128-char set)	8,450	72
12970A	Nine-Track NRZI Magnetic Tape Subsystem	8,900	72
-010,			
-011,			
-012	Additional Magnetic Tape Drive for Subsystem	6,850	61
12971A	Seven-Track NRZI Magnetic Tape Subsystem	12,400	105
-010,			
-011,			
-012	Additional Magnetic Tape Drive for Subsystem	6,900	62
12972A	Nine-Track Phase-Encoded Magnetic Tape Subsystem	10,900	109
-005,			
-006,			
-007	Additional Mag Tape Master Unit	9,375	89
-010,			
-011,			
-012	Additional Mag Tape Slave Unit	6,845	81
12935A	Digital Plotter Subsystem	4,235	43
7202A	Graphic Plotter ASCII Input	3,830	40



**TYPICAL PRICES (Contd.)**

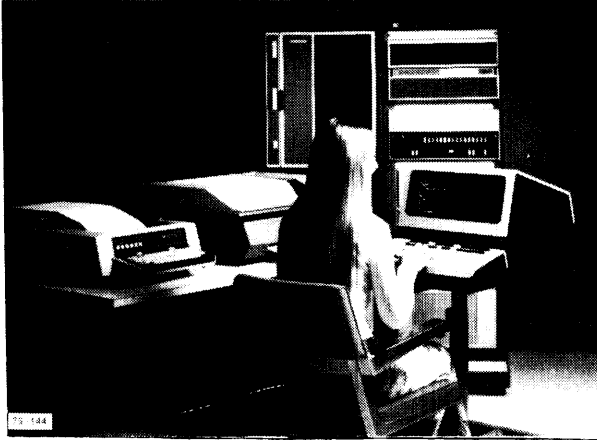
Model Number	Description	Purchase Price \$	Monthly Maint. \$	Model Number	Description	Purchase Price \$	Monthly Maint. \$
<b>ACCESSORIES</b>				7203A	Graphic Plotter (binary input)	3,830	40
12892A	Memory Protect (M/20 only)	500	9	7210A	Digital Plotter	3,400	40
12897A	Dual-Channel Port Controller	750	8	<b>DATA COMMUNICATIONS</b>			
12898A	Dual-Channel Port Controller for I/O Extender	500	10	12587B	Async Data Set Interface	550	6
12944A	Power Fail Recovery System	475	3	12589A	Automatic Calling Unit Interface	400	3
12945A	User Control Store Board	100	—	12618A	Transmit-Receive Sync Data Set Interface	700	5
12976A	Dynamic Mapping System	1,950	—	12880A	Interface for 2600 CRT	350	4
12976A-003	Add Fast FORTRAN Processor	750	—	12889A	Hardwired Serial Interface	750	4
12977A	Fast FORTRAN Processor	1,350	10	12920A	Async 16-Channel Multiplexor for 103A-Type Modems or Terminals	2,200	15
12978A	Writable Control Store	1,250	9	12920A-001	Async 16-Channel Multiplexor for 202-Type Modems	3,000	19
12979A	I/O Extender	2,700	9	<b>SOFTWARE</b>			
-010	Used as Second Extender	2,700	9	24307B	DOS-III Software	2,500	—
HP21-X/1	Field Memory Expansions	—	—	24342A	Terminal Control System (TCS) Software	2,250	35
12990A	Memory Extender	3,500	—	24376A	IMAGE/2100 Software	4,250	40
12991A	Power Fail recovery for M/30 or 129900A	600	3	24380A	HP Remote Job Entry Software Package for BCS	1,250	40
12999A	8K Memory Module	2,600	4	-001	DOS-III Compatible HP RJE	1,250	40
12997A	16K Memory Module	4,700	8	20854A	Timeshare BASIC "F" Software	5,000	—
HP21-X/2	Field Memory Expansions	—	—	20855A	Basic Control System Software	500	—
12994A	4K Memory Module	1,000	2	20856A	Timeshare BASIC "E" Software	2,500	—
12998A	8K Memory Module	1,600	4	24383A	Course Writing Facility for Use with 20854A Software	2,500	45
<b>MASS STORAGE</b>				24383B	Course Writing Curriculum Conversion	255	—
12960A	7900A Cartridge Disc Subsystem (1 fixed disc and 1 removable disc served by the same moving head; 5 megabytes)	15,000	103	24387A	Basic Analysis and Mapping Program Software (requires 2000F system)	3,000	25

— Not Applicable    NC No Charge    NA Not Available



# HEWLETT-PACKARD CO.

## HP 21MX Report Update



ACCESS 2000 Hewlett-Packard 600-lpm Printer

### Medium-Speed Printer

A new medium-speed printer, designated Model 13053A when used with the 21MX or 2100 minicomputer, has been announced by Hewlett-Packard.

The new printer operates at 600 lines per minute and prints 136 columns with a 64-character set. A 96-character ASCII drum is optional and the print rate is 436 lines per minute.

Business forms of up to six parts can be handled by the printer with spacing controlled by a 12-channel vertical format control tape, which can slew as many as 15 lines. Either six or eight lines per inch are switch-selectable. DOS, RTE, and 2000/Access operating systems support the printer.

Purchase price for the printer with controller is approximately \$16,350, depending on the options selected. First delivery was in September 1975.

### ACCESS 2000

This dual-processor system is designed to perform three primary functions:

- Source data entry from 16 or 32 HP 2640 terminals.
- A HASP RJE station to an IBM System/360 or 370 host or a U200 terminal to a CDC host.
- Concurrent local processing for applications programming.

Access 2000 centers around a 21MX Model M/20, which operates as the systems processor, and a 21MX Model M/30, which operates as a communications processor, performing asynchronous interactive communications with the terminals and synchronous communications with the

host processor. The communications processor functions are implemented in firmware to optimize efficiency. This is the first firmware system HP has marketed as a standard product.

The systems and communications processors are closely coupled, physically located in adjoining racks. The terminals can be connected locally, hardwired, or they can be located remotely and connected via telephone lines.

The HP ACCESS 2000 is available in two models: the Model 30 is a minimum configuration that can support 16 terminals. It consists of the following components:

- HP 21MX M/20 with 64K bytes of 4K MOS RAM.
- HP 21MX M/30 with 48K bytes of 4K MOS RAM.
- One 16-line multiplexor.
- Model 7900 Disc Drive with five megabytes of storage capacity.

The basic Model 30 price is \$59,900.

The Model 40 is a larger configuration that can support 32 terminals. It consists of the following components:

- HP 21MX M/20 with 64K bytes of 4K MO RAM.
- HP 21MX M/30 with 64K bytes of 4K MOS RAM.
- Two 16-line multiplexors.
- HP 7905 Disc Subsystem with 15 megabytes of storage capacity.

Card readers and line printers at the local site, as well as the 2640 terminals, can perform RJE input/output functions for the host processor. At the same time users can be running interactive BASIC programs from the terminals.

The systems will be marketed initially to users of IBM System/360 and 370 and CDC 3300 or larger systems, and to Hewlett-Packard's current customer base of distributed processing systems.

The HP Access 2000 will compete with systems from Data 100, Entrex, Four Phase, and Datapoint.

### HP 21MX, M/30

In March 1975, Hewlett-Packard announced a third model in the 21 MX line, the M/30, which extends system size upward from the M/10 and M/20. The M/30 sup-

#### HEADQUARTERS

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ports 32K words of memory in the processor chassis as a standard feature and 128K words with the Dynamic Mapping System option. If the Memory Extender is also added, memory capacity is 256K words. The M/30 uses the X/2 memory modules (650-nanosecond cycle time), which are available in 4K-, 8K-, and 16K-word modules. The M/30 also extends the number of addressable devices to 14 as a standard feature and to 46 with I/O extenders.

The M/30 chassis is 12.25 inches high and weighs 65 pounds. It has space for eight memory modules, 16 I/O channels, and two I/O extenders (16 channels each) in the main chassis.

Like the M/10 and M/20, the M/30 has all the 21MX Series features:

- 16-bit word plus one parity bit.
- Two accumulators.
- Two index registers.
- 12 scratchpad registers.
- Extended Arithmetic Unit (EAU).
- Floating-point arithmetic.
- Fast FORTRAN processor (scientific instruction set) optional.
- Single-ported memory.
- Priority interrupt system with 56 levels.
- Minimum interrupt latency: 4  $\mu$ sec without floating-point and 75  $\mu$ sec with floating-point arithmetic.
- Microprogrammed processor with optional Writable Control Store.
- ROM bootstrap loader.
- Data communications instructions.
- Power supply with "brown out" safety features.
- Memory built around 4K-bit MOS memory.
- Memory operating asynchronously with respect to processor.
- Multiple bus structure: one data bus, one address bus, one I/O bus.
- Line voltage: 88-132V or 176-264V (allows wide swing in line voltage).
- Line frequency: 47.5 to 16 Hz.
- Operating temperature: 0°C to 55°C.
- Operating humidity: 95 percent at 40°C.

The cost of the M/30 as compared to the M/10 and M/2 is as follows:

	M/10 \$	M/20 \$	M/30 \$
Processor with 16K words of X/2 memory, EAU, and floating-point arithmetic	7,350	8,500	9,400
Maintenance	78	78	78
With Dynamic Mapping	NA	10,450	11,350
Fast FORTRAN Processor	1,250	1,250	1,250

Quantity discounts range from 15 percent to 34 percent for orders of 50 or more units.

### Management/280

Management/280 is Hewlett-Packard's new data management system, which is based on the 21MX minicomputer and designed to handle on-line order

processing functions. All the necessary applications software is included with the system.

With the new system, users can enter, update, and question customer orders; update their customer files; request information on products; print invoices; generate pick lists; and initiate sales and credit checks. Batch operations can also be performed: invoices can be printed, a daily list of the status of orders can be generated, or an up-to-date list of customers can be printed out each day.

Software supplied with the system includes ON-TOP (On-line Terminal Order Processing), IMAGE/2000 with QUERY/2000, and TCS (Terminal Control Software). The ON-TOP sales order processing software operates on-line; it can be used with IMAGE/2000 data base management software, to enter, change, and access data, and to create multiple indexes for commonly used information. With the QUERY/2000 module, the user can change information or generate reports without any additional programming. TCS simplifies adding or changing terminals and implementing user-written applications software.

Hardware includes the HP 21MX central processor with 32K words of semiconductor memory, a 1,600-bit-per-inch magnetic tape unit, a 4.9M-byte disc storage subsystem, a 200 line-per-minute printer, paper tape reader, terminal printer, and system console. The system can handle up to 10 additional workstation terminals.

Optional features, such as additional disc storage and A/N display stations, are available. A communications package allows M/280 to interconnect with systems using bisynchronous communications (IBM 360/370, for example).

### PRICE DATA

Model Number	Description	Purchase Price \$
19655B	HP 2108A M/20 24K-word micro-programmable processor, paper tape reader, 2762-A pick-list terminal printer, 4.9M-byte disc, 1,600-bpi mag tape, system table, double bay cabinet, disc operating system software, IMAGE/2000 software, memory expansion to 32K, multiple port I/O extender, ON-TOP software, TCS software, line printer, system console display, console interface	70,235
015	230-V/50-Hz operation	NC
001	Replaces 4.9M-byte disc with 23.5M-byte disc	18,600
003	Replaces 1,600-bpi mag tape subsystem with 800-bpi subsystem	—2,000
213	Adds 14.7M-byte disc storage and cabinets	17,000
406	Deletes 1,600-bpi mag tape	—10,900
401	Deletes pick-list terminal and interface	—6,225
2640A	Order entry display terminals (1-5)	3,000
12880A	Terminal interface	350







## OVERVIEW

The Hewlett-Packard 2100A and 2100S are 16-bit, microprogrammable minicomputers with a core memory cycle time of 980 nanoseconds, and a ROM/RAM cycle time of 196 nanoseconds. The 2100A is aimed at OEM markets, and the 2100S is aimed at end-user markets. They are basically the same machine and can utilize the same software, except many 2100A options that are important to end users are standard on the 2100S, making it a less expensive package than an expanded 2100A. The 2100A/S is upward compatible with the firm's earlier minicomputers, of which Models 2114, 2115, and 2116 are no longer in production.

The 2100A/S features a user modifiable control storage section that can implement an extended instruction set. It can handle any set of instructions that the user develops by combining as microprograms the subinstructions of the machine's assembly language.

The control section of the 2100A/S is actually a hybrid firmware/hardware combination that decodes instructions into signals activating specific functions. In general, the instructions implemented by hardware are those involving bit testing and synchronization; these are alter-skip, shift-rotate, and input-output instructions. Microprogramming these instructions completely would have lowered over-all system performance; thus, they are hardwired but enabled by a microprogram instruction.

Although some instructions are decoded by hardwired circuitry, most of the machine language can be altered and/or extended through Hewlett-Packard's Writable Control Store (WCS®) system and a Programmable Read-Only Memory Writer system, both developed for the 2100A/S.

Four ROM modules, 256 24-bit words each, can be accommodated by the ROM addressing scheme. One module is reserved for the standard instruction set; another usually implements the floating point firmware; 2 remain for user microprograms. The floating point hardware, optional for the 2100A and standard for the 2100S, can be omitted from the 2100S system, allowing the user three 256 24-bit word modules for user microprograms or implementation of new features.

The two 16-bit accumulators in the 2100A/S are addressable as memory locations. Eight additional 16-bit working registers are included: Q, F, SP1, SP2, SP3, SP4, 5, and display. One of them, a utility register, can be addressed as an I/O device to display data on the front panel. Addressing is direct for the current 1,024-word page and the 1,024-word page zero (the base page). The rest of core can be indirectly addressed (multilevel). The multiply/divide and double-load/double store instructions are 32 bits long and can consequently address any of the 32,768 possible memory locations. There are no index registers and, consequently, no indexed addressing.

Peripheral devices interface to the processor through plug-in cards. Fourteen cards can be accommodated and powered in the 2100A mainframe, but only 12 in the 2100S, which uses 2 slots for the standard teletypewriter communications channel and a time base generator. I/O slots are exclusive of memory slots. An optional I/O extender can accommodate 31 more cards for a total of 45 cards or channels. The 2100A/S has addressing capabilities for 56 I/O channels; thus, up to 56 devices (counting the standard time base generator and the teleprinter on the 2100S) can be interfaced to a 2100A/S system through use of an I/O multiplexer. A system, however, cannot use both an extender chassis and multiplexed I/O.

All I/O channels are buffered and bidirectional. Interrupts are handled by a 60-level priority interrupt system; the first 4 levels are reserved for power-fail interrupt, memory-parity and memory-protect interrupt, and 2 DMA interrupt levels, in that order of priority. DMA channels

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are program assigned (and dynamically reassignable) to any of the channels in the mainframe or, if the I/O extender includes a special DMA option, to any of 45 channels. Once initiated, DMA transfers proceed on a cycle-stealing basis independent of the I/O priority structure. The data transfer rate through the combined DMA channels exceeds a million words per second.

Although the processor of the 2100A/S is architecturally different from its totally hard-wired predecessors, it has been designed to be upward compatible. This upward compatibility allows the extensive software already developed for the 2114, 2115, and 2116 to run on the 2100A/S. This includes 3 compilers (Fortran, Fortran IV, Algol) and a Basic interpreter; an assembler; extensive utility routines, including a library of arithmetic functions; several time sharing and real-time executive systems; a basic control system; a magnetic tape operating system; a disc operating system; and over 800 application packages. Systems using time-shared versions of Basic can support up to 32 users simultaneously. The 2100A/S microprogramming options are fully software supported with I/O, diagnostic and editing routines, as well as programs for running the PROM writer. In addition the HP Educational User's Group maintains a software library that expands the number of available programs to several thousand. User programs are maintained by the users, with support provided by HP Software Centers.

The 2100A/S provides a considerably better price/performance ratio than the 2116C, its nearest equivalent among Hewlett Packard's earlier systems. Comparable configurations for the 2100A/S are much less expensive than the 2116C, and all processing is about 40 percent faster (the 2116C has a 1.6 microsecond cycle time). The 2116C performed floating point computations only through software subroutines. The floating point hardware on the 2100A and 2100S is 10 to 20 times as fast as the 2116 subroutines, an important advantage in the scientific and time-sharing computational market that Hewlett-Packard has long made its target.

Users of 2100 A/S systems can select peripherals from the broad range of devices used with the older systems, including widely used special-purpose instrumentation such as counters, thermometers, digital voltmeters, and so forth. Low-cost magnetic tape drives and disc drives used with 2100A/S can also be used with Models 2114, 2115, and 2116.

The 2100A/S is geared to much the same markets as its predecessors. Applications for which

the system and its software are particularly well suited include time sharing, process control, automatic data acquisition, and automatic test and measurement. With DOS/M software, Hewlett-Packard also aims at the market for small business computers (SBCs). Table 1 highlights major characteristics of the entire 2100 series computer models.

## CONFIGURATION GUIDE

A minimal 2100A configuration consists of a mainframe with 4,096 16-bit words of core memory and a modified Teletype ASR 33 for I/O and for operator communication with the central processor. The ASR 33 and its interface are priced separately in case the user wants to purchase only the mainframe and memory as components for another system. This minimal processor has 14 I/O slots available; DMA and floating point hardware are optional.

The minimal 2100S configuration consists of a mainframe with 16,384 16-bit words of core memory and a programmer's console. A programmer's console and interface are part of the 2100S processor. DMA, floating point hardware, a crystal-controlled programmable time base, and a buffered teleprinter communications channel are also standard.

Both systems include extended arithmetic hardware for multiply and divide, memory parity checking, power fail interrupt with automatic restart, and memory protect. Both have 14 I/O slots or channels in the basic CPU, but the 2100S uses 2 for the console and the teleprinter channel; thus, only 12 slots are available for options. Core memory can be expanded to 8K, 12K, 16K, 24K, or 32K on the 2100A, and similarly to 24K or 32K on the 2100S. All memory and its power supply are supported within the mainframe. The 2100A/S does not yet have a memory management option to allow expansion of memory beyond the 32K words.

The control storage section contains provisions for a total of 1,024 24-bit words of ROM. Only the 256 words used for the basic instruction set are supplied with a 2100A; the 512 words that implement the basic instruction set plus floating point arithmetic are supplied with the 2100S. The user can choose 256-word RAM microprogramming modules instead of ROM modules through the WCS option. With the PROM writer, a user can even fuse his own ROM modules to attach to the centrally located control storage cards. Because the same registers are used to address and load or unload both ROM and RAM, corresponding locations cannot be implemented in both

Table 1. Hewlett-Packard HP 2100 Series: Major Characteristics

Characteristic	2100A	2100S	2116C	2114B
<b>CENTRAL PROCESSOR</b>				
General-Purpose Registers	2 ACCs	2 ACCs	1 ACC+1 extender	1 ACC+1 extender
Addressing				
Direct (words)	2,048	2,048	2,048	2,048
Indirect	Multilevel	Multilevel	Multilevel	Multilevel
Indexed	No	No	No	No
Instruction Set				
Number (std; opt)	80; 6; 95 micro-instructions	86; 102 micro-instructions	70; 10	70; 10
Decimal arithmetic	No	No	No	No
Floating-point arithmetic	Subroutine or firmware	Firmware	Subroutine	Subroutine
Priority Interrupt System				
Levels (std; max)	14; 60	60	16; 60	7; 60
<b>MAIN STORAGE</b>				
Type	Core	Core	Core	Core
Cycle Time ( $\mu$ sec)	0.980	0.980	1.6	2.0
Basic Addressable Unit	Word	Word	Word	Word
Bytes per Access	2	2	2	2
Min Capacity (bytes)	8,192	32,768	16,384	8,192
Max Capacity (bytes)	65,536	65,536	65,536	16,384
Increment Size (bytes)	8K; 16K	16K	8K	8K
Memory Parity	Std	Std	Opt	Opt
Memory Protect	Std	Std	Opt	No
ROM	Yes	Yes	No	No
Use	Control storage firmware	Control storage firmware	—	—
Capacity (words)	Std: 256 (24-bit); opt: 1,024 (24-bit)	Std: 256 (24-bit); opt: 1,024 (24-bit)	—	—
RAM	Yes	Yes	No	No
Use	Writable Control Store (WCS)	Writable Control Store (WCS)	—	—
Capacity	Std: 256 (24-bit); opt: 1,024 (24-bit)	Std: 256 (24-bit); opt: 1,024 (24-bit)	—	—
<b>I/O CHANNELS</b>				
Programmed I/O DMA Channels	Yes 2	Yes 2	Yes 2	Yes 1
Multiplexed I/O (subchannels)	56	56	56	56
Max Transfer Rate (words/sec)				
Within memory	255,000	255,000	156,300	125,000
Over DMA	1,020,400	1,020,400	238,000	500,000

memories at the same time, and maximum control memory size is 1,024 words.

Up to 56 peripherals can be attached to the 2100A/S system, counting those peripherals that are standard; any 2 devices can simultaneously use the optional DMA feature. Peripherals range from specially housed, low-noise, console printers through synchronous and asynchronous data communications interfaces to several models of digital plotters. Hewlett-Packard's extensive line of D/A converters, thermal sensors, digital voltmeters, and other special-purpose equipment also function with the 2100A/S. Auxiliary, random access mass storage is available in the form of disc units. A variety of magnetic tape units offers a range of performance in sequential mass storage.

The 2100A is available either with an operator's panel complete with a comprehensive set of operating controls and a display register, or with a controller panel that has only the basic operating controls and no display register for minimum system operation. In applications that require no further software development, the controller panel may be preferable.

The 2100S comes with a programmer's console and a buffered communications channel for a teleprinter. A user can specify at no charge one of several local or remote terminal controls or the interface for the 2600 CRT in place of the teleprinter channel. Table 2 lists the options for the 2100A/S.

#### COMPATIBILITY

Hewlett-Packard's 2100A/S is upward compatible with all models of the firm's 2114, 2115, and 2116 minicomputers. It is downward compatible at the assembly language level as long as the program does not use advanced features unique to the 2100A/S.

#### PERFORMANCE AND COMPETITIVE POSITION

The 2100A/S competes across the board with most minicomputers now on the market. Hewlett-Packard has marketed its systems primarily to end users and is generally prepared to provide full hardware and software support to all its customers. Because the manufacturer provides total system support, its primary competitors are the major minicomputer companies such as DEC, Data General, and Honeywell.

Other manufacturers compete in specific application areas. When applications are geared to scientific and industrial control processing, com-

petition includes Interdata, Control Data, IBM (System/7, 1130, and 1800), Electronic Associates, General Electric, Texas Instruments, Westinghouse, General Automation, Varian Data Machines, and Computer Automation. A fast Fourier Transform processor can be connected to the 2100A/S, and this configuration competes with such systems as Computer Signal Processor's CSP-30.

In the education field, where Hewlett-Packard is particularly strong, the 2100A/S occasionally meets NCR and Xerox as competitors, but its most vigorous rivals are the DEC PDP-8, 11/40 and 11/45 and the Honeywell 1640 time sharing systems. In this market, the HP 3000, considerably more powerful than the 2100A/S, generally competes with larger systems like DEC PDP-11/45 and Xerox Sigma 5.

Hewlett-Packard has a fine reputation for its 2100 series software and interface equipment. Besides the Basic and Fortran languages, the firm offers an Algol language compiler that is rarely available for a minicomputer, and it has long offered a mark sense card reader for input to its time sharing systems. Other manufacturers, such as DEC, now implement a similar input device to allow manual input preparation. This kind of common sense solution to real-life problems best characterizes Hewlett-Packard's approach to the computer field.

Hewlett-Packard reports that customers who have implemented frequently used subroutines in the Control Memory via Writable Control Store (WCS) or PROM chips have achieved speeds 40 to 50 times that of the 2116C, a 1.6-microsecond computer particularly useful for comparisons because it uses much of the same system software as the 2100A/S itself. ROM microprograms are typically 5 to 20 times faster than 2100A/S macroprograms.

Implementation of the WCS option, however, is expensive although the cost has been reduced to \$1500. In addition to the hardware costs, the programming costs for developing microprograms and for making required changes in the user's software to recognize new function codes must be considered. RAM instructions are provided to accomplish this. In addition, each WCS module uses up an I/O slot, and all I/O interrupts (but not DMA) are inhibited during the execution of a microprogram. The increased throughput, and the memory saved by converting software subroutines into firmware must be balanced against these costs. OEM manufacturers, however, may be particularly interested in WCS/PROM combinations that allow one system to microprogram,

Table 2. Hewlett-Packard 2100A/S Optional Features

Feature	2100A	2100S	Model No.	Comments
Multiplexed I/O	Option	Option	12894A	Requires one I/O slot; cannot be used on system with I/O extender.
Direct Memory Access	Option	Standard	12895A	Operates on cycle-stealing basis.
Operator's Panel	Option	Not available	12899A	Included facilities to display or enter data in internal registers.
I/O Extender	Option	Option	2155A	Provides power supplies and prewired slots for 31 additional I/O channels; cannot be used with Multiplexed I/O.
Direct Memory Access for Extender	Option	Standard	12896A	Requires DMA feature, 12895A, installed in 2100A computer.
Floating-Point Hardware (Module 1 of firmware)	Option	Standard	12901A	Includes add, subtract, multiply, divide, and convert using doubleword operands.
Fast Fortran Processor	Option	Option	12907A	Collection of routines used for control and memory address transfers and for double precision floating point arithmetic, precision 11 to 12 digits. Increases throughput 2 to 4 times for regular programs and 9 to 20 times for programs using double precision floating point.
Writable Control Store (WCS)	Option	Option	12908A	Permits software development and dynamic storage in RAM modules as an extension to machine control store.
Programmable ROM Writer (PROM)	Option	Option	12909A	Permits conversion of software developed with Writable Control Store into firmware, by "burning in" ROM flatpacs that are plugged into the space left for additional ROM in the control section of the microprocessor.
Teleprinter Communication, or CRT Channel	Option	Standard	12531C, 12531D or 12880A	Can be local or remote versions of unbuffered (110, 220, 440, 880 or 1,760 baud) or buffered (150, 300, 600, 1,200, or 2,400 baud) EIA Compatible Interface, or can be control interface for 2600A CRT.

debug, and fuse ROM packs for other processors, which are system components for special applications that can benefit from added user-generated micro instructions. End users with serial processing applications in which I/O is faster than

computation may also be interested in the WCS option.

Several 2100A/S end users were interviewed with respect to their experience with the system.

A large health agency has had a 2100A for a year and it has already been expanded to the equivalent of a 2100S. The system includes DMA; 16K words of memory; a 1.25-million-word cartridge disc; one tape drive; one 2767 line printer; one high-speed, paper-tape reader/punch; a Teletype; and floating point hardware. The Hewlett-Packard computer was chosen over DEC, Data General and Varian systems bid because it had a magnetic tape operating system and initially the agency believed it did not need a disc; the Varian system also had a magnetic-tape based operating system available but the bid was higher. The 2100A runs a spectrophotometer and an analytical centrifuge with all software and custom interfaces created in-house. The agency's laboratory staff subsequently discovered that the system was powerful enough to handle the off-line computations previously sent to the agency's massive IBM System/370 installation; so the disc was added to handle this third application.

This user was very enthusiastic about Hewlett-Packard software, particularly their documentation. The manuals are very clear, and the software conforms to its documentation. The chemist responsible for the installation was thoroughly familiar only with FORTRAN, but by using the HP manuals, he taught himself assembly language and the 2 operating systems. He never attended any classes. He had some trouble with the DOS manual because of the complexity of this type of software, but one morning with a representative at Hewlett-Packard's regional office was sufficient to straighten out his problems so that he could use the manual. He wrote all the special programs needed to run the spectrophotometer (up and running), the analytical centrifuge (currently being debugged), and the off-line computations (also running).

The laboratory staff reports that the computer is very satisfactory. It is easy to use, the creation of the customized interfaces has been no problem, and it is ruggedly built; it is operating well in a "dirty" laboratory environment. There were a few hardware problems in the first month, but Hewlett-Packard responded promptly to requests for service, and the problems were traced to a bad power supply. This user has never found a bug in the company-supplied software.

A manufacturer in the clothing industry uses the 2100A as an OEM component to run a laser-cutting system, which the manufacturer then sells to large clothing manufacturers. Information on patterns and layout is read into the 2100A from magnetic tape, whereupon the 2100A system controls the position of one or two laser beams (simultaneously) and movements of a conveyor

belt, in order to cut the fabric in a near real-time situation. The 2100A also controls the fabric spreader that positions the material on the conveyor. The laser cutter is highly accurate as well as fast, and it produces a sealed edge that makes the pieces very easy for the sewers to handle. The limiting factor on speed is the rate at which the physical material can be moved and cut, so this user has no need for the extra speed that could be gained by using the WCS option. This manufacturer supports his entire system himself except for the computer. When his field representative determines the reason for a system failure resides in the computer, he calls in the Hewlett-Packard representative. This arrangement has worked very well.

A second manufacturer for the clothing industry settled on the 2100A as the control component of his system solely because of the greater speeds attainable with the WCS option. This manufacturer makes an automatic marker system that takes the data from the pattern pieces generated by the designer in a base size, calculates the shape and dimensions for all other sizes and the alterations necessary to produce the design in "short" "regular" and "long" sizes, for example, and then calculates how to arrange the pieces on the material for each size to make the most efficient use of the fabric.

Input to the system is an Imlac graphic display with a light pen; output can be the display or a magnetic tape suitable for input to any XY plotter or a laser cutter. This application is compute-bound, so the manufacturer ran a special benchmark before settling on the 2100A. He reports that the DEC PDP 11/40 took 8 minutes with Fortran IV and the Data General Nova took one minute 45 seconds with Fortran V; the microprogrammed HP 2100A took one minute 9 seconds.

Microprogramming is not for everyone, but it allowed this user to develop a system 20 or 30 times faster than some of his competitors. He is consequently in a very good position in his market. He reports that one of his competitors has also developed a system controlled by a 2100A.

## MAINFRAME

The 2100A/S instructions are decoded and executed partly by hardware and partly by firmware in microprogrammed ROM. The first ROM module (256 words) implements the instruction set. ROM, located in the control storage section, can be expanded 4-fold through the incorporation of additional ROM chips to extend the machine's

instruction set. The optional PROM writer permits these chips to be user-programmed to incorporate any functions that can be derived from the initial instruction set.

It is even possible to rewrite the original instruction set to alter it for particular applications. This permits "fine tuning" the instruction sets to the requirements of different markets. Such rework of the control store section, however, requires extremely detailed knowledge of the machine and of the complex effects of instruction changes. Although feasible, Hewlett-Packard warns that its warranties and support guarantees are voided if the original instruction set is modified in any way. The user is free, however, to write microcode for the 3 remaining modules to tailor his machine to his specific application.

The 2100A/S, thus, represents a major departure from prior Hewlett-Packard minicomputers. Although the 2116C offers the capability of assembly language microprogramming, in the sense that a single instruction can consist of several subinstruction combinations, all user-specified instructions are decoded and executed by hardware.

#### Central Processor

The 2100A and the 2100S use essentially the same processor with certain optional features on the "A" model standard to the "S" model. This basic 2100A/S computer has a cycle time of 980 nanoseconds per word. The instruction set uses a straightforward single-address code with a multilevel indirect addressing capability. Addition is the only arithmetic operation in the basic instruction set; subtraction requires a complement instruction followed by an addition. The extended arithmetic instruction set, as defined for older 2100 computers, is standard on the 2100A/S; it provides hardware integer multiplication and division and load/store doubleword.

The 2100A/S has 2 accumulators, registers A and B, which are used as a single, doubleword accumulator by the extended arithmetic instructions. It has no index registers, and list addressing must be performed using indirect or multilevel indirect addressing. An instruction is provided to increment a specified core location and skip the following instruction if the result is zero. This can be useful in incrementing a stored address, for counting, and for loop control.

Memory is conceptually divided into 1,024-word sections called pages. The basic instruction set can directly address only the current

page and the base page. The extended instruction set can address all of core memory directly.

All fixed-point hardware arithmetic instructions use singleword operands, but the floating-point firmware uses 2-word operands. The floating point firmware, stored in Module 1 of the ROM memory is standard to Model S (unless the user wants to incorporate Module 1 into his WCS option rather than use it for floating point arithmetic), and optional on Model A processors. The 12907A Fast Fortran Processor provides double precision floating-point arithmetic using 3-word operands for 11 to 12 digits accuracy.

The basic processor provides 60 priority interrupt levels; 56 of them can be used for I/O devices. The other 4 levels are for power failure with automatic restart, memory parity and memory protect (which share one level), and the 2 DMA channel interrupts.

**Microprocessor.** The microprocessor contains four 256-word instruction modules with each 24-bit word storing, on the average, 6 "micro orders." These modules can be implemented in "hardwired" ROM rows (modules), each consisting of 6 integrated circuit packs. Two rows are located on the Timing and Control Card and 2 on the ROM Control Card in the control storage section. Module 0 contains the standard instruction set. Modules 1-3 can contain extensions to the instruction set although Module 1 is usually reserved for floating point arithmetic. If the user adds RAM Writable Control Store (WCS) modules that correspond to ROM modules, the corresponding ROM module must be disconnected.

When the Programmable ROM Writer (PROM) unit is added to a system, the user can fuse his own ROM packs. Thus the user can mix ROM and RAM modules in one system.

- Module 0. Standard instruction set in ROM, supplied by Hewlett-Packard.
- Module 1. Floating point instruction set in ROM, supplied by Hewlett-Packard.
- Module 2. Dynamically changing user-defined instruction set in RAM with Module 2 row in ROM disconnected.
- Module 3. Static user-defined instruction set created with RAM, but burned into integrated circuit packs with the user's PROM writer and stored on the Module 3 row of the Timing and Control Card.

Each RAM WCS module is a single card occupying a slot on the I/O bus. Figure 1 shows the relation of these WCS cards to the corresponding ROM rows in the storage and control unit. The cards are loaded from the A and B registers in the CPU. The most significant 8 bits of the B register designate the WCS address; the least significant 8 bits in B plus the 16 bits in A constitute the 24-bit microinstruction.

Instructions are executed using the ROM Address and Instruction Registers directly via a flat cable connected to each WCS card. Thus, the cycle time of 196 nanoseconds per word is maintained regardless of whether the module is in ROM or RAM; this speed is degraded only if the macroprocessor memory or I/O is addressed. In this case, the microprocessor may wait for an appropriate entry point into the macroprocessor 980-nanosecond cycle.

User-generated microprograms can be developed in such a way as to allow access to 6 registers in addition to the registers normally accessible to user programs. Use of the 6 extra registers can greatly reduce the number of references to memory, thus, increasing processing speed. The 3-operand format of the microinstruction word allows a function to be performed with the contents of 2 registers, and the result to be so stored in a third, all in one microinstruction cycle.

**Data Structure.** The basic data format for the 2100A/S is a single 16-bit word that can also be divided into two 8-bit bytes, or linked to another 16-bit word to form a 32-bit doubleword. A seventeenth bit is used for memory parity checking.

The byte format is used for character-oriented I/O devices; software drivers perform the packing and unpacking of bytes. The doubleword format is used for software or hardware extended-precision arithmetic. The floating-point option uses 2-word operands. The microinstruction uses a 24-bit word averaging 6 "micro orders;" it can include as many as 3 operands. Table 3 lists data formats used in the 2100A/S.

**Special Registers.** The 2100A/S has 10 programmable 16-bit registers, a Q and F register, a program counter, 2 accumulators, 4 scratch pad registers and a switch register. A 16-bit display register comes with the operator's panel. When the processor is halted, a switch register can be manually loaded from the display register. In the run mode, the switch register can be addressed as an I/O device, and the program can transfer data between either accumulator and the switch register.

Each accumulator operates independently of the other, and each can be used to provide an operand for arithmetic operations and to store the result. The accumulators can be addressed as memory locations 00 and 01 for register-to-register operations.

In addition, the 2100A/S has two 1-bit registers. One is the extend register that operates as a link between the 2 accumulators via a rotate instruction. It stores the carry bit from the accumulator if one occurs during an add or increment instruction. The other register is an overflow register, which is set when an arithmetic operation generates a number too large to be held in the accumulator.

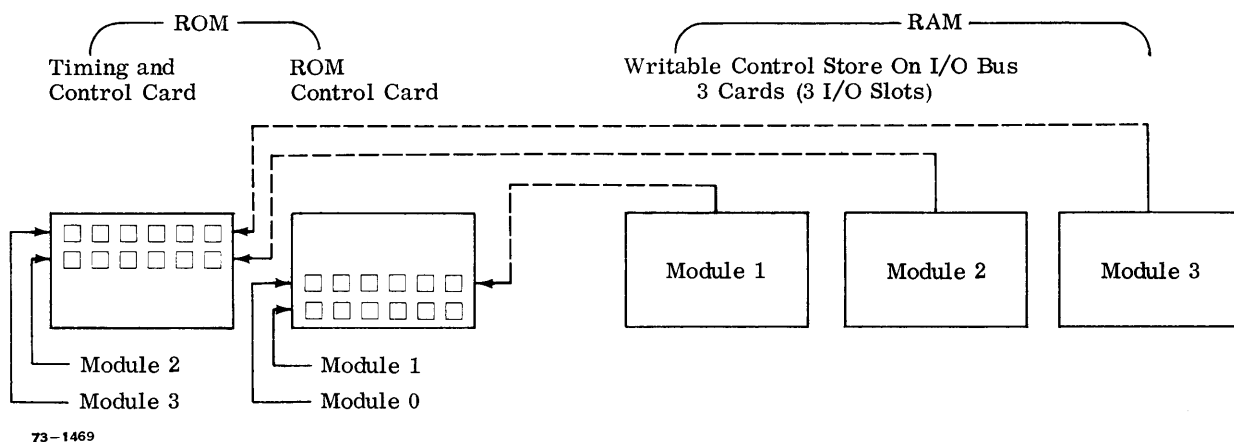


Figure 1. Microprocessing Modules 0-3, as Implemented in ROM or RAM



Table 3. Hewlett-Packard HP 2100A/S  
Data Formats

Type of Data	Representation
<b>Operands</b>	
Nonarithmetic	1 word (bit 15 determines truth value in logical format)
Fixed-point arithmetic	1 word
<b>Floating-point arithmetic</b>	
Single precision	2 words (7-bit exponent + sign, 23-bit fraction + sign)
Double precision	3 words (7-bit exponent + sign, 39-bit fraction + sign)
Complex numbers	4 words (both imaginary and real parts have 7-bit exponent + sign and 23-bit fraction)
Hollerith	1 word (2 ASCII char per word)
Instruction	1 word (basic instruction set); 2 words (extended instruction set)

**Instruction Set.** The 2100A/S has 5 categories of instructions: memory reference, register reference, I/O, extended arithmetic memory reference, and extended arithmetic register reference.

Memory reference instructions can directly address 2,048 words of memory: 1,024 words in the current page (the one containing the instruction) and 1,024 words in the base page (the first 1,024 memory words). Other memory locations can be addressed indirectly.

These instructions address either accumulator as the second operand, if required. In addition, memory addresses 00 and 01 are reserved to address the 2 accumulators; thus either accumulator can be treated as a memory location.

The memory reference class of instructions includes load, store, add, AND, inclusive and exclusive OR, jump, store return and jump to subroutine, compare, and increment memory and skip if zero.

Register reference instructions provide shift/rotate, test and skip on zero, increment, complement, and clear either accumulator. Instructions to clear, complement, and test the extend register E are included. Also the E register can be shifted or rotated in combination with either accumulator. This class includes a no-op instruction. The overflow register is tested, cleared, or set by instructions in the I/O group. Register reference instructions can be microcoded to effect more than one operation per instruction.

The I/O group provides for transferring control and status information between either accumulator and an I/O device; for testing device status; for enabling/disabling individual interrupt levels or the whole interrupt system (except power/fail and parity interrupts, which are always enabled); for setting, clearing, or testing the overflow register; and for halting the processor.

Extended arithmetic memory register instructions provide arithmetic multiply and divide, and load or store doubleword.

The extended register reference group includes left/right, logical/arithmetic shift, and left/right rotate "n" places on the combined contents of the 2 accumulators.

When the floating-point firmware is implemented, 6 instructions are provided: add, subtract, multiply, divide, fix, and float. Fix converts the floating-point number in the accumulators into an integer, which is placed in accumulator A. Float converts the integer in accumulator A into a 2-word, floating-point number that is stored in the 2 accumulators.

For the floating-point arithmetic instructions, one operand is assumed to be the contents of the 2 accumulators, which are treated as a single doubleword; the other operand is a doubleword located in memory. The result is placed in the accumulators. Table 4 lists typical instruction execution times.

**Addressing Facilities.** The basic memory referencing instruction set uses a one-word format, which allows 10 bits for addressing. These bits can address a 1,024-word page of memory. Another bit in the instruction word selects the current page (the one containing the instruction) or the base page (the first page in memory). One bit in the instruction word specifies indirect addressing.

The extended memory referencing instruction set uses a 2-word format. In this scheme the second word is used for addressing; 15 bits for

the address, and the most significant bit for indirect addressing. Indirect addressing is recursive. The most significant bit of the indirect address specifies subsequent levels.

The 2100A/S has no index registers, thus, no indexed addressing.

When the processor attempts to write into non-existent memory in a system, the processor executes a no-op. If a read is attempted from nonexistent memory, a word of zeros is transferred, and a parity error interrupt is not generated.

Table 4. Hewlett-Packard HP 2100A/S:  
Typical Instruction Execution Times

Instruction	Execution Time ( $\mu$ sec)
<b>Fixed-Point</b>	
Load/Store	1.96
Add	1.96
Subtract	3.92
Multiply	10.7
Divide	16.7
Double Load/Store Accumulators	5.9
Shift/Rotate 1-16 places	2.9-7.8
<b>Floating Point</b>	
Add (avg)	41.6* 286 (s)
Subtract (avg)	42.6* 296 (s)
Multiply (avg)	37.2* 251 (s)
Divide (avg)	53.9* 297 (s)
Fix (avg)	7.8*
Float (avg)	17.1*
Indirect Addressing (per level)	0.98

Notes:

\* With floating-point hardware, which is an option for "A", standard to "S".

(s) By subroutine, on "A" computer.

Interrupt Control. The priority interrupt system includes 60 interrupt levels. The 2 highest priority levels are assigned to power fail and parity error. A power fail interrupt cannot be disabled; parity error interrupt can be disabled. The next 2 levels are reserved for DMA interrupts, which are generated by the DMA channels when a DMA block transfer is complete. DMA channel 1 interrupt has priority over the DMA channel 2 interrupt. The other 56 interrupt levels are assigned to the I/O device channels. Channel interrupts have priority according to the order of channel number; the lower the channel number the higher its priority.

The interrupt system control resides in a master control, which enables or disables all of the interrupt system except power fail and parity error interrupts. This master control can be set or reset by instruction or by the Interrupt System pushbutton on the control panel. The master control is automatically reset when power is first turned on; thus programs depending on the interrupt system should set the master control to enable the interrupt system.

The next level of interrupt control resides in flag flip-flops associated with the I/O channels; when a channel flag is set, all interrupts from lower priority channels are inhibited.

The lowest level of interrupt control is an interrupt flip-flop that enables/disables an interrupt level.

When an interrupt occurs, and it is the highest priority waiting for service, the processor relinquishes control at the end of the current instruction (with some exceptions), stores the program counter in a dedicated core location, and jumps to the address stored in the interrupt's pointer location. Jump indirect instructions and instructions that may affect the priorities of I/O devices must be completed, plus part of the next instruction, before an interrupt is granted. This allows for system stabilization and such contingencies as a jump to a protected location.

When any interrupt is granted, the interrupt system is disabled until 2 phases of the interrupt service routine are executed. The interrupt system is then enabled, and only interrupts at a lower priority are inhibited during the execution of the service routine.

Main Memory

The basic 2100A computer includes 4,096 words of core storage. Main memory can be expanded to 8,192; 12,288; 16,384; 24,576; and



32,768 words. The basic 2100S includes a larger memory of 16,384 words, but it has the same expansion limits, 24,576 or 32,768 words. All core is housed in the computer mainframe.

Each word consists of 16 data bits and a parity bit. Memory parity checking is standard.

Although the first 64 locations of main memory are reserved for interrupt handling, some of these locations are available to the program if it requires fewer interrupt levels than the 60 provided. The first 4 words of main memory are not used: memory addresses 00 and 01 are used to refer to the A and B accumulators; addresses 02 and 03 are used for exit sequences if the accumulator contents are used as executable instructions. Memory protection is standard.

Memory cycle time is 0.980 microsecond per word. The effective transfer rate for transferring data within core storage, provided both locations are directly addressable, is 255,101 words per second using straight-line coding and 74,165 words per second using a programmed loop. If one of the operand locations is not directly addressable, the effective transfer rate for straight-line coding is 208,163 words per second.

The upper 64 locations of core memory are reserved for the binary loader, which is permanently resident and protected unless specifically enabled by a panel switch.

Memory Protect. A programmable fence register separates lower protected memory from the upper unprotected memory. Two exceptions are that locations 00 and 01 are unprotected because these addresses are reserved to address the accumulators, and the upper 64 memory locations are protected because the resident binary loader is stored there.

When memory protect is enabled, it prohibits the execution of all instructions that write into or transfer control to protected memory and all I/O instructions except those referencing the switch or overflow register. This limits I/O control to interrupt control only. If I/O interrupts are serviced by executive routines located in protected memory, the executive can have complete control of all I/O operations.

A memory protect violation causes a memory protect interrupt, which operates on the same level as the parity interrupt. The address of the illegal instruction and the bit indicating parity/protect error is located in the violation register, which can be transferred to the accumulator by instruction.

When an interrupt occurs or when the processor is halted and the Internal Preset switch is set to Halt, memory protect is disabled. It is enabled with a Set Control (I/O) instruction with a select code of 5. This instruction must be executed at the end of each interrupt servicing subroutine.

#### I/O Control

All peripheral devices are connected to the computer via standard I/O channels, and each is uniquely associated with a particular interrupt location in main memory. Although 56 interrupt locations are available for standard I/O channels, the basic 2100A contains only enough prewired slots for 14 channels. The basic 2100S has 12 channels; 2 are used by the time-base generator and the teleprinter communications channel which are standard on the 2100S. Thirty-one additional I/O channels are provided by the 2155A Extender Module for either processor model. Multiplexed I/O is available with the optional 12894A multiplexer, which uses a single I/O slot and an external control for 56 channels. A system can accommodate either a multiplexer or an extender module, but not both.

The peripheral device on an I/O channel connects to the computer through a standard I/O interface card. This is a plug-in, printed circuit card, which consists of a buffer up to 40 bits long for the transfer of data; a flag flip-flop controlling interrupts originating from the device connected to the interface; and a control flip-flop, which enables the peripheral device to perform its input or output operation and also controls the interrupt capability of the device. The interrupt location to which each I/O interface connects, and its consequent interrupt priority, is determined only by the position each interface card occupies in a rack in the main computer cabinet; the interrupt locations used need not be contiguous, provided a special "jumper" card is inserted in each location that is skipped.

In general one device attaches to each I/O channel, but controllers for devices such as magnetic tape units and discs for which more than one operation can be programmed require the use of 2 adjacent I/O channels; one of these is used to transfer control information, and the other is used to transfer data. Interface kits are available for connecting a Bell System (or equivalent) data set to a standard I/O channel. A Teletype multiplexer interface, developed for use as part of the HP 2000E/2000F time sharing system, enables connection of up to 16 local and remote teletypewriters to a single standard I/O

channel through Data-Phone® connections or hardwired cable up to a mile long.

A buffer full (up to 40 bits) of data is transferred between the I/O interface and the computer; instructions are provided to pass information between either accumulator and the buffer in the interface. Buffer size depends on the particular peripheral device concerned; it is generally 8 or 16 bits although it can be up to 40 bits.

Transfers between the buffer and the peripheral device are initiated by issuing a Set Control (STC) command. On completion of a transfer the device controller sets the flag flip-flop on the I/O interface card, causing an interrupt. The total data throughput attainable by this method depends on the length of the interrupt servicing routines, but a typical overall limit is about 90,000 transfers per second.

Direct memory access (DMA) adds autonomous block transfer facilities, which directly "steal" main memory cycles. The feature, standard on the S computer but optional for the A, provides 2 DMA channels capable of a combined transfer rate as fast as the cycling rate of main memory (1,020,400 words per second). Two high-priority interrupt levels are reserved for the DMA channels. There is no hardware connection between the DMA channels and particular peripheral devices, and these channels can be used to address any device on a standard I/O channel. DMA is a required feature if disc or magnetic tape units are used on the 2100A.

Transfers are specified to the DMA by a control word. The control word selects: (1) the device, (2) the state in which the control flip-flop in the interface is to be left between each byte of the transfer and after the end of the transfer, and (3) the data format, one or two bytes per word. Registers within the DMA hardware maintain the number of words remaining to be transferred and the next memory address to be used; these registers also require initialization before a DMA transfer is started.

I/O instructions are provided to output the contents of either accumulator to the data buffer on the I/O interface card and to load either accumulator from this buffer after an input operation. Further I/O instructions provide the setting, clearing, and testing of the flag and control flip-flops associated with each I/O interface.

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Each I/O instruction includes a 6-bit select code field, which selects the I/O interface addressed by the instruction by referring to its interrupt level number. Of the 64 possible select code values, 56 are available to address I/O interfaces; the other values select special functions concerned with I/O, the overflow register, and the DMA channels.

Simultaneous Operations. Hewlett-Packard supplies software I/O drivers that let simultaneous I/O operations proceed concurrently with processing. The priority interrupt system provides orderly multiplexing of I/O operations according to the system configuration. A system can have 2 DMA channels; thus 2 devices can transfer data simultaneously via alternate DMA channels. All devices transferring data to or from the accumulators can operate at the same time. The only restriction on I/O simultaneity is that imposed by the overall throughput capacity of the system.

Execution of microprograms inhibits standard I/O interrupts, but DMA transfers can occur simultaneously.

## PERIPHERALS

A broad range of peripherals is available for the 2100A/S, including devices in every standard category. With the exception of those mass storage devices that must use DMA, all peripherals connect to the common I/O bus through their corresponding interfaces. They are serviced in accordance with the priority order of the mainframe slots into which their interfaces are plugged. In some cases Hewlett-Packard offers only a suitable interface and not the device itself. This is done for such OEM equipment as digital plotters, as well as for some data communications equipment and nonstandard I/O devices.

### Low-Speed Peripherals

Table 5 lists the low-speed peripherals available for the 2100A/S. The number listed in the "Comments" column is the model number of the HP interface kit that includes the referenced peripheral device, along with suitable cabinets, power supplies, and an appropriate interface card. One of these interfaces is standard to the 2100S and consequently need not be separately specified, but the 2100A requires both device and interface kits. Interfaces are included with all other types of peripherals except the CRT.

Table 5. Hewlett-Packard HP 2100A/S: Low-Speed Peripherals

Peripheral Device	Performance Characteristics	Comments
<b>Console Printer</b>		
2752A Teleprinter (Modified ASR 33)	10 cps	Friction fed; "A" computer also requires 12531B interface*.
2754B Heavy-Duty Teleprinter (Modified ASR 35)	10 cps	Pin fed; "A" computer also requires 12531B interface*.
2762A Terminal Console Printer KSR	30 cps, 75 cols	Friction fed; "A" computer also requires 12531D-001 interface*.
2762A-006 Terminal Printer KSR	30 cps, 118 cols	Pin-fed; "A" computer also requires 12531D-001 interface*.
27621-009 RO Terminal Printer	30 cps, 118 cols	Same as 2762-006.
<b>Paper Tape</b>		
12925A Punched Tape Reader	500 cps	—
12926A Tape Punch	75 cps	—
12927A Tape Punch	120 cps	—
<b>Punched Card</b>		
12986A Optical Mark Reader	200 cpm	Reads both punched and manually marked cards.
12985A Card Reader	600 cpm	Reads punched cards only.
<b>Line Printer</b>		
12980A Line Printer	200 lpm, 132 cols	64-char set.
12980A-001 Line Printer	150 lpm, 132 cols	96-char set.
12984A Line Printer	300-1, 100 lpm, 80 cols	64-char set.
12982A Line Printer	600 lpm, 132 cols	64-char set.
12982A-001 Line Printer	400 lpm, 132 cols	96-char set.

\*Interfaces for starred items are standard to the "S" computer processing unit.

### High-Speed Peripherals

There is an extensive line of high-speed peripherals for the 2100A/S, including random access mass storage devices with almost 12 million words of storage. Disc and magnetic tape peripherals require the DMA option and interface slots (Table 6).

### Special-Purpose Peripherals

Hewlett-Packard offers a number of special-purpose peripherals and interface kits for use

with the 2100A/S. These include digital/analog converters, a time base generator, interfaces to microcircuits, relay output registers to operate external devices, and graphic plotters (Table 7).

### DATA COMMUNICATIONS

Interface kits for connecting a Bell System (or equivalent) data set to a standard I/O channel are available. A hardware multiplexer, used as part of the 2100A/S time sharing systems, enables attachment of up to 16 local and remote terminals to a single standard I/O channel through

Table 6. Hewlett-Packard HP 2100A/S: Mass Storage Devices

Type of I/O	Peripheral Device	Performance Characteristics	Comments	
Magnetic Tape (1)	12971A Magnetic Tape Subsystem	7-trk NRZI; 200/556/800 bpi; 45 ips, master unit	Requires 2 I/O slots for any master unit; all masters can attach 1-3 more slaves.	
	-010	45 ips, slave unit		
	-001	37.5 ips, master unit		
	-011	37.5 ips, slave unit		
	-002	25 ips, master unit		
	-012	25 ips, slave unit		
	12970A Magnetic Tape Subsystem	9-trk NRZI; 800 bpi; 45 ips master unit		All 12971A Comments apply to 12970A systems.
	-010	45 ips, slave unit		
	-001	37 ips, master unit		
	-011	37.5 ips, slave unit		
	-002	25 ips, master unit		
	-012	25 ips, slave unit		
12972A Magnetic Tape Subsystem	9-trk PE; 1600 bpi; 45 ips master unit	All 12971A Comments apply to 12972A subsystems.		
-010	45 ips, slave unit			
-001	37.5 ips, master unit			
-011	37.5 ips, slave unit			
-002	25 ips, master unit			
-012	25 ips, slave unit			
Moving Head Disc (2)	12960A Cartridge Disc Subsystem (1 fixed, 1 removable platter)	2.5M words; 47.5 msec avg access; 126K wds/sec transfer rate; 24 sectors/trk; 400 trks/platter or 800 total on master unit	Requires 2 I/O slots for any master unit, master can attach 1-3 more slaves; slaves can be 12960A-010 or 12961A-010 models.	
	-010	Slave unit (1 fixed, 1 removable platter)		
	12961A Cartridge Disc Subsystem (1 removable platter)	Same specifications as 12960A except contains only 1 removable platter of 400 trks, 1.25M words	All 12960A Comments apply, but master cannot handle any slave except 12961A-010.	
	-010	Slave unit (also 1 platter)		
	12965A Disk File Subsystem	11.776M wds/pack; 32 msec avg access; 155K wds/sec transfer rate; 23 sectors/trk, 4,000 total trks/pack; master unit, containing all subsystem power, and control and interface for 1 more drive	Requires 2 I/O slots per subsystem; 4 drives per subsystem, but 3rd drive has control for both 3rd and 4th.	
	-020	2nd or 4th slave drive		
	-030	3rd slave, including control for both 3rd and 4th		

Notes:

- (1) All tape units are IBM compatible.
- (2) Hewlett-Packard supports the HP 2773 and 2774A drum memories, the 2766A fixed-head disc memories, and the 2870A moving head disc drives available for the older 2100 series of computers but no longer sells them new.



Table 7. Hewlett-Packard HP 2100A: Special-Purpose Devices

Type of I/O	Peripheral Device	Performance Characteristics	Comments
Converter	12555B D/A Converter	2 D/A channels (8 bits/channel)	—
Clock	12539C Time Base Generator	Generates real-time intervals from 1,000 sec	—
Relay Register	12551B Relay Output Register	Has 16 form-A contacts for operating external devices	With 48-pin mating connector.
	12551B-001 Relay Output Register	Same as H12551B but with readback	
Duplex Register	12597A Duplex Register (positive true)	Dual 8-bit register for bidirectional data transfer between computer and external device	With 48-pin mating connector.
	12597A-001 Duplex Register (negative true)	Same as 12597A	Same as 12597A.
	12554A Duplex Register (positive true)	Dual 16-bit register for bidirectional data transfer between computer and external device	With 48-pin mating connectors.
	12554A-001 Duplex Register (negative true)	Same as 12554A	Same as 12554A.
	12566B Micro-circuit Duplex Register (ground true)	Dual 16-bit register for bidirectional data transfer between computer and external device at DTL/TTL voltage levels	With 48-pin-mating connectors.
	12566B-002 Micro-circuit Duplex Register (positive true)	Same as 12566B	Same as 12566B.
	12566B-001 Micro-circuit Duplex Register (negative true)	Dual 16-bit register with input and output tied to form a single 16-bit bidirectional data bus	With 24-pin mating connector.
	12930A Universal Interface	Provides a dual 16-bit register for bidirectional high-speed data transfer (to 1 mega Hz) between CPU and external device	—
General-Purpose Interface	12620A General-Purpose I/O Interface	Provides control and flag circuitry on I/O bread-board	—
Plotter	12560B Digital Plotter Interface	Interface for CalComp 563 or 565 digital plotter	—
	12935A Computer-Controlled Plotter	Plots on 11 x 17-in. paper under direct computer control; up to 20 coordinates/sec and up to 5 symbols/sec	—

Data-Phone connections or hardwired cable up to 1,000 feet long.

A crystal-based programmable time base generator is a standard feature of the 2100S. This feature measures intervals from 0.1 millisecond to 1,000 seconds. The time interval to be measured is selected by a 3-bit control word that is transferred to the time base generator by a programmed instruction. The generator is of particular use for analog-to-digital devices in real-time systems and for data communication systems.

An unusual communication device, the 7260A Optical Mark Reader, can be connected to a remote 2100A/S computer via a Bell System Data-Phone interface. This device uses standard-size tab cards for data entry; each card contains a maximum of 12 rows and 80 columns of data. Data can be punched as for a conventional card reader, marked in preprinted marking boxes with an ordinary lead pencil, or coded by a combination of punched holes and marks. Reading, which is controlled by clock marks printed along the bottom edge of the card, is at 200 cards per minute. The 7260A has an automatic feed mechanism.

A 2600A CRT/Keyboard can be used either as an on-site keyboard console or as a remote terminal. When used as a console on the 2100S, the 12880A interface for the 2600A is substituted for the standard teleprinter interface, but it must be purchased separately for the 2100A. The 2600A transfers data at 10 to 218 characters per second. Table 8 lists all of the peripherals available for data communication purposes.

## SOFTWARE

Hewlett-Packard provides comprehensive software for the 2100A/S including all software developed for the earlier 2100 computers, 2114, 2115, and 2116. Software for Hewlett-Packard's computers was created gradually by thorough exploration of one application area at a time. As a result, after several years of this approach, 2100A software includes over 800 applications packages, a magnetic tape system (MTS), a data acquisition and control system (DACE), a real-time executive (RTE), 2 disc operating systems (DOS and DOS/M), and a number of time sharing systems. Language compilers for Basic, Extended Basic, Basic Fortran, Fortran IV, and Algol 60, as well as 2 versions of the assembly language are available.

This range of software supports the use of the 2100A/S as a powerful desk calculator through various real-time control applications to a time

sharing system for 32 users. All time sharing configurations can also support DOS. When the time sharing system is not in use, it can be "slept" (rolled out of core), and the proper DOS can be brought in for batch processing. This feature is particularly useful in educational time sharing, one of Hewlett-Packard's strengths, where timesharing is needed for a limited number of hours per day.

## Operating Systems

Hewlett-Packard offers facilities for running programs on small systems as well as large systems.

The smallest configurations can use the basic control system (BCS). These facilities are not operating systems but are collections of utilities that let absolute or relocatable binary programs run under operator control.

For configurations with magnetic tape, these utilities can be transferred from paper tape to magnetic tape and run under the Magnetic Tape System Control.

Seven other operating systems are provided: Data Acquisition and Control Executive, Real-Time Executive, 2000E and F Timesharing Systems, and 2 Disc Operating Systems.

Magnetic Tape System (MTS). The MTS handles assembly, compiling, and loading of both absolute and relocatable programs. Once programs are transferred from paper tape to magnetic tape, they are automatically loaded into core by a supervisory system that executes user requests. MTS tape is organized into program files for permanent storage of absolute programs and linkable subroutines. The remainder of the tape is available to executing programs for storage of temporary data and for scratchpad use.

MTS can handle programs written in Fortran, Fortran IV, Algol, Basic and assembly language. It operates in batch processing mode.

Data Acquisition and Control Executive (DACE). DACE 9600D is designed for use with test equipment. It provides for real-time operation of the system and permits modification of the stored program with respect to system timing and channel assignments directly through the teleprinter keyboard without program recompilation. The system is programmed to perform tasks involving measurement, computation, and output of data from one or a group of channels. A 24-hour clock is maintained by system software, which



Table 8. Hewlett-Packard HP 2100A: Data Communications Devices

Type of I/O	Peripheral Device	Performance Characteristics	Comments
CRT/Keyboard	2600A CRT/Keyboard Terminal	10 to 218 cps; 72 char/line; 25 lines	Requires 12880A interface on "A" computer.
Interfaces	12587B Asynchronous Data Set Interface	Half- or full-duplex; echoplex; strappable to provide discrete clock from 45-2,400 bps; char size to 8 bits; parity and line code under program control	Conforms to EIA RS232B Interface; reverse channel can be keyed/detected; data sets can be Western Electric 103 or 202 or equivalent.
	12618A Transmit-Receive Synchronous Data Set Interface	Half- or full-duplex clocked by data set at speeds up to 9,600 bps; char size to 8 bits; line code under program control; char or block transfer	Same as for 12587B.
	12589A Automatic Calling Unit Interface	—	For use with Western Electric 801A or 801C Automatic Dialer.
	12531C or D Asynchronous Terminal Interface	Half-duplex; internal or external clocking at rates of 110, 220, 440, 880, and 1,760 bps for Model C and 150, 300, 600, 1,200, and 2,400 bps for Model D; internal clocking provided by jumpering; char size to 11 bits (includes start and stop); line code under program control	Current loop or RS232B Interface; data sets can be Western Electric 103 or 202 or equivalent.

allows the user to cue tasks at desired elapsed times from program start.

The system can be switched to a manual operating mode in which task constants can be examined and modified via the teleprinter keyboard. This allows a test engineer to modify test procedures as testing proceeds. DACE requires a minimum of 8,192 words of main memory.

Real-Time Executive (RTE). RTE is available in a core-based system (RTE-C) and 2 disc-based versions. The core-based system is designed for users who want multiprogramming but do not need the extensive off-line storage and on-line program preparation facilities of the disc-based version. It has no background processing

capability and no functions related to disc-file handling, but otherwise it performs the same functions as disc-based RTE. The two disc-based systems are RTE 9600F and 9600E. They differ in that 9600F uses the 2766A Disc Memory and the 9600E uses the 12960A Disc Subsystem. The 2766A is a fixed-head disc unit with 262K words to 1 million words capacity; access time is 8.7 milliseconds. The 12960A is a moving-head disc drive with one fixed and one removable cartridge. Its storage capacity is 2.5 to 10 million words; average access time is 47.5 milliseconds. RTE 9600F is appropriate for applications that require fast response times while RTE 9600E is appropriate for applications that require large storage capacity for programs and data.

RTE provides facilities for servicing events in real-time multiprogrammed mode with background batch processing. Each user program in the system is classified as real-time memory or disc resident, or background memory or disc resident; programs are fetched from the disc for execution automatically by the executive. Only one background disc resident program can be in the system at a time — there is no multiprogramming of background programs. The assembler and the Fortran IV and Algol compilers are available in segmented versions that can be run as background, disc-resident programs under RTE. Fortran and assembly language programs for RTE-C must be compiled while the system is not on-line doing real time processing.

RTE provides the following system functions.

- Program scheduling.
- Interrupt processing.
- I/O processing.
- System request handling.
- Operator request handling.

Programs can be initiated on a time-scheduled basis of hours, minutes, seconds, or milliseconds. When requested by another program, the operator, or an event, programs are placed on a scheduled list that is priority oriented. User priority levels can range from one to 99. The highest priority job is initiated. It executes immediately if core resident. If it is on disc, the current executing program in core is swapped out to disc, and the scheduled program is read into core. When swapping between disc and core is required, RTE checks to determine if another core-resident job can be executed during the swap.

RTE uses the priority interrupt system to establish the priority for power failure, memory protect violation, time-base generator, peripheral I/O, and user-interfaced device interrupts. Depending on the system configuration and current state, the normal system response time to an interrupt is from 1 to 3 milliseconds. For a data acquisition or other system requiring faster response times, RTE provides a privileged interrupt that bypasses the normal interrupt servicing routine. The typical response time to a privileged interrupt is less than 100 microseconds.

The I/O scheduling and control monitor allocates the DMA channels and all standard system devices. It assigns physical units to logical unit designations, stacks I/O requests by the priority

of the calling program, and automatically buffers in memory output to low- and medium-speed devices. All I/O operates concurrently with program execution.

Users can request I/O device operation to be timed out for check purposes. Devices that do not perform the required function within the allocated time are put on a "down" status, and the operator is notified.

User programs communicate with RTE via system requests made by assembly language subroutine calls or by Fortran or Algol statements (RTE-C does not handle Algol). Standard system requests are provided for the following functions.

- Read from or write to any I/O device or disc.
- Perform control function on I/O device.
- Check status of I/O device.
- Schedule programs to run.
- Turn off running program when completed.
- Request time and day of the year.
- Request program retiming.
- Make global tracks available to all programs.
- Release disc tracks.

The operator monitors and controls RTE via the system Teletype. Operator control of the system is by the following operator requests.

- Start or terminate any user program.
- Change priority or timing of any unscheduled user program.
- Initialize time.
- Suspend any executing or scheduled user program and activate it on request.
- Return current status of any user program.
- Specify timeout for an I/O device.
- Load and execute a background program.
- Load relocatable programs and subroutines in the foreground and the background disc-resident area.

- Change I/O logical unit assignment.
- Control I/O device availability.
- Release program tracks.

The minimum hardware configuration to support disc-based RTE includes a 2100A or 2100S processor with direct memory access option and 16K words (24K words of memory for Algol compiler); a time base generator; a high-speed, paper-tape reader; a system Teletype; and 2.5 million words of moving head disc cartridge storage.

Minimum hardware for RTE-C corresponds to the minimum 2100S configuration. Hewlett-Packard recommends a high-speed, paper-tape punch and an auxiliary Teletype to make background operations easier.

RTE will support all 2100A/S standard peripherals and subsystems except the general-purpose interfaces designed for user special-purpose devices. A system generation program will tailor RTE to a user's specific configuration. An optional file manager package for disc-based RTE provides for organization into named files, access to those files from program calls or the console, and protection of files being used by more than one program.

2120 Disc Operating System (DOS/M). DOS/M is a batch processing system that simplifies the creation, checkout, and execution of user programs. Some of the features provided are as follows:

- Keyboard or batch (card input) control via 40 directives.
- Compile or assemble with load and go capability.
- Centralized control of I/O processing.
- Disc file management including facilities to load, store, delete, and list user files and to edit user source statement files.
- Extended file manager to write user data files, which can be accessed randomly or sequentially.
- Job accounting, giving both run and execute times for each job.

Programs written in Fortran, Fortran IV, Algol, or assembly language can run under DOS/M. User programs can be segmented into a main program with subservient segments that can

be stored on the disc and called by the main program. The main program and segments can share a common core area.

Utility routines supplied with DOS/M provide source code editing, program debugging, decimal arithmetic, and formatting for printed report preparation.

The user can customize DOS/M at system generation time to fit a particular application. In fact, several versions of DOS/M can be generated and stored on separate discs. The appropriate version can be called for a specific application.

The minimum hardware configuration to support DOS/M includes a 2100A/S processor with direct memory access, 8K words of core memory, a system Teletype, a high-speed, paper-tape reader, and a 12960A disc system. DOS/M can also support CRT keyboard display, a card and optical-mark reader, a tape punch, a console printer, 7- and 9-track magnetic tape, a line printer, a time base generator, a relay output generator, and up to 23.5 million words of disc file.

Time Sharing System. Two time sharing systems are offered — 2000E and 2000F. The 2000E is a single-processor system that provides interactive time sharing facilities via the Extended Basic interpreter for up to 16 users. The 2000F is a dual-processor system that uses a 2100A processor as a communications front-end to a second 2100S processor. Up to 32 users can access the facilities of the Extended Basic interpreter implemented in the second processor.

Both systems can support terminals wired directly to a system port located up to 1,000 feet away, or terminals connected to a port by a telephone data set. Both systems support multiplexed terminals. The 2000E can handle 10, 15, or 30 character-per-second ASCII-compatible terminals; 2000F handles 10 to 240 character-per-second ASCII-compatible terminals hardwired and ten 14.5, 15 or 30 character-per-second ASCII-compatible terminals over data sets: Teletype ASR 33, 35, or 37; HP 2605A; Univac DCT 500; Execuport; HP 2600A CRT; Datapoint 3300; Memorex 1240; GE TermiNet 300; and IBM 2741 Selectric®. (Call 360 Correspondence and PTTC/EBCD codes are supported on the IBM 2741.)

Time sharing systems consist of the executive, multiplexer control program, accounting system, and library system.

Selectric®, a registered trademark of IBM Corporation.

The executive supervises I/O, bulk memory transfers, program execution, library usage, and the accounting systems.

The multiplexer control program operates in response to signals from the terminals. It assigns users priorities based on the tasks they are doing. The scheduler uses a time-slice method to allocate system resources to the user with the fastest response time requirement.

The accounting system controls access to the system and accumulates system statistical data that can be collected into reports when requested by the operator.

The library system maintains public libraries and private user libraries. Public libraries can be accessed by any user, but can be changed only by the system operator.

When the time sharing system is not in use, it can be transferred to a removable disc cartridge or magnetic tape. The time sharing hardware configuration can support DOS/M, RTE, or the Basic Control System.

### Language Processors

Language processors for the 2100A/S include an assembler; Extended Basic interpreter; and Fortran II, Fortran IV, and Algol compilers.

Assembler. The 2100A/S assembler is an extended assembler that provides one-to-one correspondence between instruction mnemonics and machine language codes. It also provides pseudo-operations to control the assembly and output listings. It produces absolute or relocatable output code. It has a macroinstruction to provide communication with programs written in microcode in the WCS.

Time-Shared Basic. The 2100A/S time-shared Basic is a superset of Dartmouth Basic. Time-shared Basic has the following features.

- Matrix handling — addition, subtraction multiplication, inversion, and transposition of one or 2 dimensional arrays.
- ASCII character string manipulation — input, output, comparison, storage, and retrieval of strings of up to 126 characters.
- Data files — can be created and saved and arranged serially or randomly; maximum file capacity is 6,144 words for the 2000E, 8.4 million words for the 2000F.
- Simultaneous access to data files — allows multiple users to read the same data file and a special group of users to write in the same data file.
- Program chaining — lets one Basic program call another at execution time. A large program can be broken into segments and chained together. A COMMON statement allows variables to be passed between programs.
- System clock — accessible by users at execution time for time of day, day, and year.
- Diagnostics — the Basic interpreter checks format and syntax of statements when entered and performs program structural checks during execution.

The 2000F time-shared Basic has these additional features:

- Unlimited number of data files accessible to a user program — each program can have 16 data files open simultaneously.
- Time input — time for a terminal response to a user-written program can be measured and limited. Maximum response time is 4 minutes before program continues execution.
- Port identification — single and multiple ports can be selected for data entry in response to program queries.
- Formatted output — output lines up to 256 characters wide can be formatted.

Fortran. Two versions of Fortran are available for use with the 2100A/S: Fortran, an extended version of USASI Basic Fortran, and Fortran IV. Fortran IV is a full implementation of Standard Fortran. Programs written in Hewlett-Packard Fortran can be compiled by the Fortran or the Fortran IV compiler.

Hewlett-Packard Fortran includes the following extensions to Basic Fortran.

- Format specifications can be entered at execution time.
- COMMON array declarations are permitted.
- A function subprogram can change the values of its arguments and of COMMON storage; that is, the arguments of function subprograms are "called by name."

- External functions are included for Boolean operations.
- The "S" sign is included in the character set.
- A 2-branch form of the IF statement is included.
- A facility for octal constant specification is provided.

The Fortran compiler is available in paper tape and magnetic tape versions. For the paper tape version the minimum is 4,096 words of main memory and a 2752A teleprinter, but the addition of a paper tape reader and punch significantly increases the compilation speed. Both versions of the compiler produce an object program in relocatable binary format for loading by the Basic Control System. The program can be linked to relocatable binary subprograms originating from assembly code or Algol source code.

Fortran IV compiler requires 7K words of core memory. It can run under DOS or the RTE operating systems. RTE Fortran IV has special statements for real-time control.

Algol. 2100A/S Algol incorporates all the features of the Algol language as described in the ALGOL 60 Revised Report, published in the Communications of the ACM for January 1963. I/O statements are the same as for 2100A/S Fortran. All variables are treated as OWN variables. Other features of the source language include the following.

- Facilities for intermixing identifiers of types REAL and INTEGER in the same assignment statement.
- Provision for initializing variables and arrays.
- An EQUATE statement.

The 2100A/S Algol compiler requires a main memory of 8,192 words and a teleprinter. The compiler operates in a single pass of the source code and produces an object program in relocatable format for loading by the Basic Control System. Relocatable programs generated from Algol source language can be linked to subprograms generated from Fortran or assembly language source code. There are essentially no restrictions on the size of the Algol program that can be compiled.

### Application Programs

A number of special-purpose software packages have been developed by Hewlett-Packard for particular applications. These are generally not based on any of the standard operating systems, but are self-contained software systems marketed as complete packages that include hardware. The following sections describe some of these special-purpose systems from a software standpoint.

Educational Basic System. The Educational Basic System is a package designed especially for the educational market. The software supplied is the standard Basic language system with one addition — a Marked Card Basic program is included. This is the same as the standard (single-user) Basic language program except that the 12986A Optical Mark Card Reader is supported as an input device for Basic language programs. Special preprinted cards are available on which Basic language source statements can be entered simply by marking boxes on the cards with an ordinary lead pencil; thus, pupils can prepare their own source programs without any data preparation equipment. When the reader is loaded, the programs are run under the Basic language system with printout on a teleprinter in the usual way. The teleprinter and reader can be either local to the computer or connected to it via telephone lines.

One related application package provides mathematics drill and practice. This is the Computer Assisted Instruction (CAI) program, which was designed for elementary school grades one through 6.

2060A Digital Logic Module Test System. This is a special-purpose combined hardware/software system designed for the automatic testing of digital logic modules. All types of integrated circuit and discrete-component logic can be tested without special adaptation. The system is based on a 2116C computer with 8,192 words of main memory and includes a 12660A Module Adaptor, which is a unit that enables 2 plug-in modules to be mounted side by side — the module under test and a fault-free module of the same type. A series of tests is carried out on both modules, and any differences between the 2 are logged on the console typewriter.

The software provided includes a special-purpose programming language called AuTest for writing test programs. AuTest has been designed for use by digital logic engineers and includes statements listing all the module signal connector pins and specifying power supply voltages, high

and low logic levels, current limits, and comparison tolerances. The TEST statements include facilities for a programmed delay between changes of logic level to satisfy module timing requirements. There is a PERMUTE instruction that initiates the testing in a single statement of all possible combinations of logic levels up to 16 pins. Maximum speed of the system is 10,000 tests per second per pin with no delays programmed. Between tests, the 2060A system is in a conversational mode, receptive to commands typed on an input keyboard.

**Microprogramming Software.** Hewlett-Packard supports its WCS and PROM Writer options with the HP I/O Utility Routine, the HP Microassembler, the HP Micro Debug Editor, the HP Programmable ROM Writer, the PROM Mask Generator, and a diagnostic package. Two versions of each of these are available; one set operates under BCS and one under DOS.

Microprograms are entered into the system via punched cards or magnetic tape, whereupon the microassembler produces an interim punched tape (BCS) or disc file (DOS) plus a microprogram listing. The microeditor reads the interim record, allows examination of any word in memory (and hence in WCS), and outputs the microprogram. Output can be a block of program in WCS, a new edited interim disc file (DOS) or punched tape (BCS), a record suitable for use by the WCS I/O routines or a record suitable for use by the mask generator.

The mask generator program produces 6 mask tapes for the manufacture of ROM packs. Six are needed to accommodate the 24-bit word because each pack consists of 256 4-bit locations. The PROM driver uses these tapes plus a card temporarily inserted into an I/O slot to fuse ROM chips in the PROM writer, a small box cable connected to the I/O card. The PROM writer software also enables verification of the chips and fusing of any missed bits.

Two companies, Wetherford and Semiconductor Specialists, will burn a board with a one-day turnaround. Cost is about \$50 per board.

The ultimate output of the 2 microprogramming options together with their supporting software can be a customized library of microprograms stored off-line on disc or punched tape, a fully loaded Writable Control Store, and/or fused ROM packs that can be mounted on the Timing and Control or ROM Control cards. The WCS I/O driver can be called by Assembly Language, Basic, FORTRAN and ALGOL programs, allowing loaded WCS microprograms to be dynamically altered using a standard subroutine call.

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## HEWLETT-PACKARD CO.

### 2100A and 2100S Report Update

#### CIS/2000

College Information System (CIS/2000), a Hewlett-Packard educational software package, allows on-line student registration while classes are opened and closed and class size automatically adjusts. Designed to run on the HP 2000F and HP 2000 Access Systems, the package is part of the Terminal Oriented Administrative Data Systems (TOADS) software systems. It is suited for colleges with enrollments of under 10,000 students.

Up to 32 terminals can be connected to the CIS/2000-equipped mini. Students can register by phoning a central terminal operator at the college. Class size can be adjusted and class loads listed while registration is in progress.

The software license for CIS/2000 is \$8,000 and includes 10 days of on-site training for school personnel. An entire HP 2000F or HP 2000 Access System including CIS/2000 costs approximately \$100,000.







### OVERVIEW

The HP 3000CX Series contains a group of preconfigured systems intended to satisfy the batch and on-line data processing requirements of the general user. Each system is based on the HP 3000 16-bit minicomputer configured with 32K to 128K bytes of memory, peripherals, and software. Although the series has a strong orientation towards the terminal user and Hewlett-Packard's traditional market — scientific/engineering, time-sharing, and real-time processing, typical business-oriented components — COBOL, RPG II, and a data base management system — give the system an appeal to an extremely wide market.

Four models or hardware configurations are marketed within the series: 50CX, 100CX, 200CX, and 300CX. The four models use a common operating system (MPE/C) that operates in both terminal and multiprogramming batch mode with full spooling capabilities. Software is built around full hardware implementation in the stack architecture of the HP 3000 CPU. Each model is upward compatible and can be field expanded with a minimum of dislocation.

The CPU stack architecture gives the user reentrant, recursive programming without the excessive overhead of non-stack systems. The code and data segments of a program are segregated so that each functions in its own domain and each is addressable through its own register set. (No instruction in the HP 3000 permits a program operating in task mode to modify the program.)

The system has 176 microcoded instructions that perform fixed- and floating-point arithmetic, relational operations, boolean functions, word and bit tests, byte and word move operations, scan and test functions, plus various shift and program and loop control instructions. In addition, optional decimal and extended floating-point instruction sets are available. Provisions are also made for both indirect and indexed address modification.

In addition to the stack processing mode, the HP 3000CX provides for maximum usage of available memo-

ry space through a virtual memory addressing technique that is largely transparent to the user. Virtual memory address space is 64K words.

The system allows up to 253 separate priority interrupt levels and handles a variety of peripheral equipments. Three modes of I/O operation are available: direct, multiplexed, and selector channel. The organization of the interrupt and I/O systems allows independent ordering of device service priority, device access priority, and device interrupt priority.

The entire system is organized around a Central Data Bus; the CPU, main memory, IOP and selector channels use the central data bus to communicate with each other. Although this path serves as a limiting factor on access time and aggregate transfer rate, its speed of 5.7M bytes per second is sufficient to handle virtually all situations.

Table 1 lists the mainframe characteristics.

In addition to the MPE/C operating system for the HP 3000CX, Hewlett-Packard provides both a BASIC interpreter and compiler, FORTRAN, COBOL, RPG II, SPL (Hewlett-Packard's Algol-like System Programming Language) IMAGE/3000, various utility packages, such as Sort and Trace, and a host of applications programs.

The system can be integrated into a network of HP 3000CX data centers or interfaced to a large computing facility. Additionally, BASIC programs from the smaller HP 2100 and 21MX Timesharing Series can be moved up to the HP 3000CX processors.

Table 2 lists the basic and optional configurations of the four models.

### Competitive Position

The HP 3000CX is in an excellent competitive position for the medium-scale, general-purpose processing environments in which it will be marketed. Its commercial processing features, notably COBOL, IMAGE/3000 (a data base management system), RPG II, and a spooling capability, should appeal to users with a variety of jobs — scientific, engineering, and commercial processing — and a limited budget.

Prime competition for the 50CX and 100CX will be Digital's 11/40 and 11/45 under RSTS-11/E or RSX-11D or M at the lower end, and small Digital System 10s as well as XEROX 550 and 560 with the 200CX and 300CX at the top end. Systems such as the Data General ECLIPSE Series, Burroughs 1700 Series, IBM 370/115, 125, and 135, Modular Computer MODCOMP IV, PRIME 300, Varian V74, General Automation SPC-16/80, and Interdata Models 7/32 and 8/32 compete for some applications.

The prime thrust of Hewlett-Packard's marketing activities will be towards new installations and upgrades of obsolete or obsolescent installations, BASIC timesharing

installations, and small commercial and various engineering applications. Because of its comprehensive software, the 3000CX should be a prime contender for customers with a wide variety of data processing tasks and a small budget. Although minicomputer manufacturers are providing more support for commercial processing, none offer the wide variety available with the HP 3000CX, especially comparable to IMAGE/3000 for data base management. This variety has been the domain of Xerox with its Sigma line (now replaced by 550 and 560) and Digital with its PDP-10. The sophisticated operating systems required to perform this variety of tasks on general-purpose systems are available only for large configurations. Minicomputers such as the PDP-11/45 are moving in this marketing direction. Thus, Hewlett-Packard should "make hay while the sun shines" because the hay fields will soon be full of competing reapers.

### Configuration Guide

Table 1 lists the configurations for the four models of the 3000CX Series. The range of configurations addresses a broad spectrum of applications from the 50CX, which is geared to both the small user and the OEM market, to the 300CX, which is adaptable to most medium-scale environments. It should be noted that all models are based on a common processor and a common operating system. This single feature provides the user with the capability to upgrade his computing, terminal, and I/O power without the usual trauma associated with such changes.

Table 3 lists the peripherals available. Table 4 provides a summary of the available software.

### Compatibility

The four models of the HP 3000CX Series are fully compatible with each other at the CPU and program level.

### DATA COMMUNICATIONS

The HP 3000CX provides a wide variety of data communications facilities from a multi-terminal time-shared mode of operation to a multi-processing distributed network configuration and from a remote job entry or front-end facility to a large 370 type system.

When operating with a second processor, the interprocessor communications operations are multiprogrammed with both other terminal and batch jobs.

### Maintenance and Support

Hewlett-Packard is noted within the industry for its product support. The company maintains 172 field offices in 65 countries throughout the world including 60 service

**Table 1. HP 3000CX Series: Mainframe Characteristics**

<b>Central Processor</b>	
Type	Microprogrammed
Control Memory	
Size	2,048 (32 bit)
Use	Firmware
No. of Internal Registers	11
<b>Addressing</b>	
Direct	Variable for instructions + data
Indirect	1 level, 64K
Indexed	Yes
<b>Instruction Set</b>	
Implementation	Microprogrammed
Number	172
Decimal Arithmetic	Opt firmware
Floating-Point Arithmetic	Yes (opt extended F-P firmware)
User Microprogramming	No
<b>Priority Interrupt System</b>	
<b>Operation Modes</b>	
Levels	253
<b>Main Storage</b>	
Type	Core
Cycle Time (msec)	0.980
Basic Addressable Unit	Word (16-bit)
Bytes per Access	2
Cache Memory	No
Min Capacity (bytes)	96K
Max Capacity (bytes)	28K
Increment Size (bytes)	32K
Ports per Module	1
Error Checks	Parity
Protection Method	Bounds/stack
Memory Management	Yes, stack
ROM	No
Use	
Capacity	
RAM	No
Use	
Capacity	
<b>I/O Channels</b>	
Programmed I/O	Yes
DMA Channels	4
Multiplexed I/O (no. of subchannels)	2 (32)
<b>Max Transfer Rate</b>	
Within Memory (Central Data Bus)	5.7M bytes
Over DMA	3.8M bytes
Simultaneous Operations	Yes

facilities in the United States and Canada, backed by five regional offices. Two service and warranty plans are available under terms of the purchase agreement. One provides for "parts only" warranty for 15 months; a second provides full services, parts, and labor for 90 days. Follow-on agreements can provide for guaranteed response times and full service or operate on a per-call time-and-materials basis.

Hewlett-Packard also provides a set of diagnostics that function as a task of the operating system. A stand-alone set runs directly on the CPU without operating system aid. In addition, a set of microprogrammed micro-diagnostics can be executed and transmitted directly to Hewlett-Packard through a modem and common carrier line for immediate assistance on difficult problems.

**Table 2. HP 3000CX Series: Basic Configurations and Options**

Basic Configurations	50CX	100CX	200CX	300CX
Memory (bytes)	96K	96K	128K	128K
Disc (bytes)	5M (moving hd cartridge)	10M (moving hd cartridge)	2M (fixed hd)	2M (fixed hd)
Tape	800 bpi	800 bpi	47M (mov. hd pack)	47M (mov. hd pack)
Peripherals	—	200-lpm printer	800 bpi	800 bpi
	—	600-cpm reader	200-lpm printer	1,250-lpm printer
			600-cpm reader	reader/punch 200 cpm (30-75 cpm)
Terminal	16-port Async term controller	16-port Async term controller	16-port Async term controller	16-port Async term controller
Software	MPE/C Utilities SPL Comp. lib Trace Editor Sort	MPE/C Utilities SPL Comp. lib Trace Editor Sort	MPE/C Utilities SPL Comp. lib Trace Editor Sort	MPE/C Utilities SPL Comp. lib Trace Editor Sort
Options				
Memory (bytes)	128K	128K	—	—
Disc	Expandable	Expandable	Expandable	Expandable
Tape	1,600 bpi	1,600 bpi	1,600 bpi	1,600 bpi
Peripheral	—	Delete	Delete	Delete
Terminal	Add 202 capability	Add 202 capability	Add 202 capability	Add 202 capability
Software/Firmware*	MPET	MPET BASIC FORTRAN IV RPG Decimal Firmware, expanded floating-pt firmware	MPET Same as 100CX Plus:- COBOL IMAGE	MPET Same as 200CX
Additional Hardware				Real-time data acquisition programmable controller

\*Available in packaged combinations at various prices

**Table 3. HP 3000CX Series: Peripherals**

Device Model	Description
<b>Discs</b>	
30103A	Fixed head; 2M bytes; 236KW/sec
30102A	Moving head; 4.9M bytes; 156KW/sec
30110A	Moving head; 47M bytes; 246KW/sec
<b>Magnetic Tapes</b>	
30115A	9 trk; 800 bpi; 36KB/sec
30115A-100	9 trk; 1,600 bpi; 72KB/sec
<b>Card</b>	
30106	600-cpm reader
30119A	Reader/punch; 200 cpm/30-75 cpm
30119A-001	Keyboard + verify
<b>Printer</b>	
30118A	600 lpm; 64 char set; 132 col
30118A-002	128 char set option
30128	1,250 lpm; 64 char set; 132 col
30128-001	96 char option
30127	300 lpm; 64 char; 132 col
30127-001	96 char set
<b>Paper Tape</b>	
30104A	Reader: 500 cps
30105A	Punch: 75 cps
<b>Data Communications</b>	
30032	16-port async channel
30120A	Terminal/console, 30 cps/75 col, 300 baud
30120A-001	Opt 118 col
30124A	ASR-33, 10 CPS
30123A	CRT, 72 char x 25 line, switchable data rates HP2640 Terminal
30300A	Programmable controller, based on HP 2100 mini

**Table 4. HP 3000CX Series: Software**

MPE/C	Multiprogramming execution, multiprogrammed batch and on-line terminal; full logical level I/O and data communications handle.
MPET	A limited subset of MPE/C oriented to environments using primarily BASIC.
Language Processors	FORTRAN, COBOL, Systems Programming Language (SPL), RPG II, BASIC (both a compiler + interpreter version)
Special Purpose	Image/3000, a data base management system; Query/3000 terminal-based query facility for Image/3000 data base
Scientific Library	A collection of various functions and transforms
Other	Diagnostics, utilities, user library

## HEADQUARTERS

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# HP — 3000CX SERIES

## TYPICAL PRICES

Model Number	Description	Purchase \$	Monthly Maint. \$
<b>PROCESSORS AND WORKING STORAGE</b>			
30000C	Model 50CX (includes CPU with 96K bytes of core memory; multiplexor channel (15 device capacity); async terminal controller (16 ports); system console and cabinets; mag tape unit; 5M byte cartridge disc unit; std power with 120/208V and 3 phase/60Hz)	99,500	687
32400C	Model 100CX (same as 30000C except multiplexor channel (16 device capacity); 10M bytes of disc storage; 5M byte cartridge disc unit plus additional 5M-byte drive; 600-cpm card reader subsystem; 200-lpm dot matrix printer)	129,500	953
32401C	Model 200CX (same as 32400C except CPU with 128K bytes of core memory; 2M-byte fixed-head disc; 47M-byte moving-head disc; 600-cpm card reader subsystem; 200-lpm dot matrix line printer)	171,000	1,134
32402C	Model 300CX (same as 32401C except with 1,250-lpm printer; reader/punch subsystem)	203,500	1,263
<b>Processor Options</b>			
<b>All Processors</b>			
001	MPET operating system in place of MPE	NC	NC
015	System AC power option with 230V	NC	NC
100	1,600-bpi tape unit replaces 800-bpi unit	1,500	30
202	Adds 202 type data set control to async terminal controller	1,240	8
<b>Processor Options 50CX</b>			
181	Increases memory to 128K bytes	10,000	34
403	Delete disc cartridge system	8,000	136
<b>Processor Options 100CX, 200CX</b>			
401	Deletes 600-cpm card reader	-6,000	-66
402	Deletes dot matrix printer	-9,000	-83
600	Timeshare package	NC	40
601	Scientific package	5,000	49
602	Commercial package	5,000	44
603	Commercial and scientific package	9,000	74
<b>100CX and 200CX Option</b>			
102	128-char option for line printer	500	NC
<b>200CX and 300CX Options</b>			
104	Expands fixed-head disc to 4M bytes	6,600	18
<b>300CX Options</b>			
102	96 character option for line printer	2,000	18
106	Keyboard and verify capability added to reader/punch	2,000	NC
404	Delete card reader/punch subsystem	-12,000	-127
405	Delete high-speed printer	-28,000	-151
604	Commercial package without data base management capability	6,000	64
605	Commercial and scientific package without data base management capability	10,000	94
<b>MEMORY AND CPU ENHANCEMENTS</b>			
30011A	Expanded instruction set	3,250	19
30011A-001	Replaces extended-precision floating-point instruction set with decimal firmware instruction set	1,000	NC
30011A-002	Adds the decimal firmware instruction set to the extended-precision floating-point instruction set	2,000	NC
30414A	Field-installed memory upgrade kit (increases memory to 96K-bytes)	11,000	46
30429A	Field-installed memory upgrade kit (increases memory from 64K-bytes to 128K-bytes)	21,500	80
30431A	Field-installed memory upgrade kit (increases memory from 96K-bytes to 128K-bytes)	11,000	34
<b>MASS STORAGE</b>			
30102A/015*	47M-byte disc file subsystem	32,000	216
30102A/010*	Adds drive on same controller	12,000	-40
30103A	Fixed head disc subsystem with 1.0M bytes of storage	20,000	148
30103A-001*	Adds 1.0M bytes of storage	3,300	36
30103A-002*	Adds 3.0M bytes of storage	9,900	54
30110A/015*	Cartridge disc subsystem	15,000	136
30110A-010*	Adds additional 7900 drive (5M bytes)	-5,025	-19
<b>INPUT/OUTPUT</b>			
<b>LINE PRINTERS</b>			
30118A/015*	200-lpm subsystem (132 col; 64 char)	9,750	83
30118A-001*	128 char set	500	NC
30127A/015	300-lpm subsystem with 136 col and 64 char	13,500	135
30127A-001*	96 char set	2,000	NC
30128A/015*	1,250-lpm subsystem with 132 col and 64 char	36,000	151
30128A-001*	96 char set	2,000	NC
<b>PUNCHED CARD</b>			
30106A/015*	Card reader subsystem: 600 cpm	7,160	66
30107A/015*	Card reader subsystem: 1,200 cpm	18,540	126
30107A/001*	Adds double read station	2,575	2
30119A/015*	Card reader/punch subsystem: reads 200 cpm, punches 75 cpm	13,500	127
30119A-002*	Adds off-line keyboard punch and verify capability	2,000	NC
<b>MAGNETIC TAPE</b>			
30115A	Includes 2,400 ft of tape and cabinets; 9 channel, 800 cpi, 45 ips; includes controller interface. Handles up to four 9-channel mag tape units - one 30115A and mixture of up to three additional units (i.e. either 30115A-200's, 30115A-300's, or 30115A-400's)	12,000	93
30115A-100*	9 channel, 1,600 cpi, 45 ips. Includes controller interface, handles up to four 9-channel mag tape units	1,500	30
30115A-200*	Adds an additional 800 cpi, 45 ips, 9-channel drive	-2,450	-22
30115A-300*	Adds a 9-channel, 1,600 cpi, 45 ips, master drive	-975	8
30115A-400*	Adds a 9-channel, 1,600 cpi, 45 ips, slave drive	2,500	NC
<b>PAPER TAPE</b>			
30104A	Cabinets + controller interface included, paper tape reader subsystem (500 cps)	3,350	32
30105A	Paper tape punch subsystem (75 cps)	4,225	52
<b>TERMINALS</b>			
30120A/015*	Printer Terminal (30 cps, 75-col keyboard, and pin feed with paper guide; w/o pedestal)	4,920	38

Model Number	Description	Purchase \$	Monthly Maint. \$
30120A-001*	Adds 118 col facility and replaces pin feed with tractor mechanism; vertical tab/form feed, horizontal tab, and pedestal included	1,135	NC
30120A-003*	Friction feed replaces pin feed; with pedestal	NC	NC
30120A-015*	230V/30Hz ac power option	220	NC
30122A/015*	Character-mode CRT (2615A)	2,835	36
30124A	Teletype terminal (10 cps ASR-33)	2,650	68
30124A-015*	230V/50Hz ac power option	200	NC
<b>EXPANDED I/O CAPABILITY</b>			
30030A	High-speed selector channel	6,080	13
30032B	Async terminal controller (Note: Option 001 or 002 must be ordered)	3,000	18
30032B-001*	For 103 type modems only	1,240	8
30032B-002*	For 103 and 202 type modems	2,480	16
<b>ADDITIONAL DEVICE INTERFACES</b>			
30126A	CalComp plotter interface for 500 Series plotters	1,030	5
30300A/015*	Programmable controller with 8K of memory	18,000	207
30361A	Programmable controller interface kit	5,000	8
<b>REAL-TIME CAPABILITY</b>			
30301A/015*	Real time programmable controller (includes HP 2100S computer with 8K words of memory, DMA, programmable time-base generator, hardware extended arithmetic and floating point instructions; paper tape reader, teleprinter; interconnection interfaces; signal cable, cabinets; software)	23,000	NA
30361A-001*	Option to the programmable controller interface kit replaces BCS/3000 software with the RTE C/3000 software	+2,000	NA
<b>DATA COMMUNICATION</b>			
30130A	2780/3780 Emulation Subsystem	3,500	30
30441A	Adds 202 modem support to async term controller	1,500	8

\* indicates option number  
NA: information not available



# HEWLETT-PACKARD CO.

## HP 3000 Report Update

### SAS/3000

Hewlett-Packard's Student Assignment System (SAS/3000) software package for the HP 3000 minicomputer allows school administrators to build master schedules, assign students to classes and interactively maintain school and student files.

As part of the TOADS (Terminal Oriented Administrative Data System) software system, SAS/3000 compares a manually developed master schedule to student course requests and then produces class schedules based on school-defined priorities. Individual student course requests can be entered on-line and scheduled without rescheduling all the other students. The system is designed for use in junior, senior and vocational high schools.

The HP Mini Data Center equipped with SAS/3000 is also available to students, teachers and school personnel for general problem solving and administrative tasks. The one-time software license charge is \$9,500 and a HP 3000 minicomputer with SAS/3000 ranges in price from about \$100,000 to \$200,000.

### MEDIUM SPEED PRINTER

Hewlett-Packard has announced a new medium-speed printer, designated Model 30133A when used with the HP 3000CX minicomputer.

Print speed is 600 lines per minute with a 136-column line and a 64-character set. A 96-character ASCII drum is optional; print speed is reduced to 436 lines per minute.

Business forms of up to six parts can be handled by the printer, with vertical spacing controlled by a 12-channel tape. Control tapes allow slewing up to 15 lines. Either six or eight lines per inch are switch-selectable.

Purchase price for the printer is approximately \$19,000 including controller, depending on the options selected. Deliveries began in September 1975.

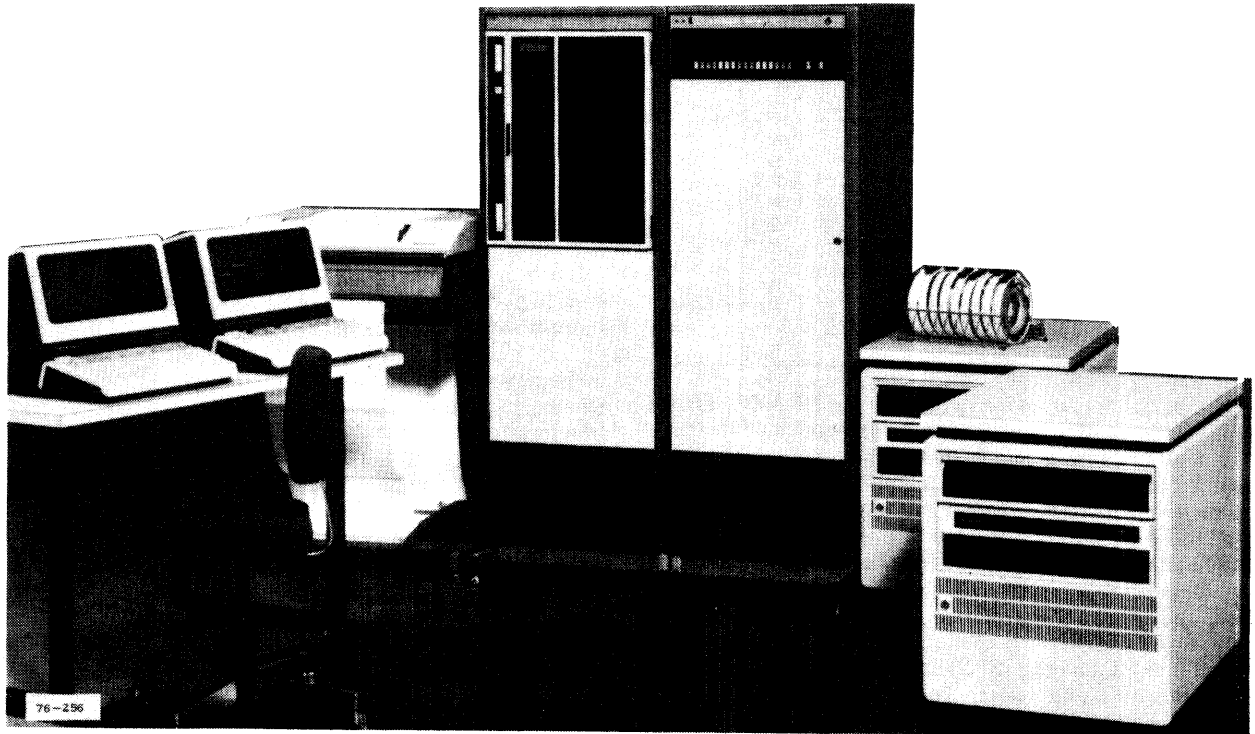
### HEADQUARTERS

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Palo Alto CA 94304  
(415) 493-1501



## HEWLETT-PACKARD CO.

### HP 3000 Series II Preliminary Report



#### OVERVIEW

The HP 3000 Series II is Hewlett-Packard's newest series of mini/midi computers. According to HP, the new series combines better performance, better reliability, and lower cost, to outdistance its predecessor, the HP 3000CX Series. The 3000 II offers 3000CX compatibility, and like the 3000CX it is a family of packaged models.

According to HP, the 3000 II will find a home with small companies, decentralized data processing organizations, educational institutions, and OEMs. The typical user considering the 3000 II will probably be interested in terminal orientation, data base management, concurrent terminal/batch applications, and/or a multilingual environment. Users looking for a system to do batch processing or timesharing alone will probably find that the 3000 II is not the answer.

To span the range of user environments and budgets, HP is offering a compatible series of configurations: Model 5, Model 7, and Model 9.

- The Model 5 is oriented toward the so-called super-mini market, with typical applications being inventory control, order processing, and other com-

mercially oriented tasks. The Model 5 is also targeted for interactive scientific and educational jobs.

- The Model 7 is intended for medium-scale commercial and administrative applications. Data base management software as well as COBOL and RPG II are provided as standard software on the Model 7.
- The Model 9, with its large memory size (up to 320K bytes) and additional language facilities (FORTRAN IV and BASIC), should be suitable for multilingual environments of a medium size.

Table 1 outlines the basic hardware and software configurations for each model.

#### HEADQUARTERS

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**Table 1. HP 3000 Series II: Basic System Configurations**

	Model 5	Model 7	Model 9
<b>Hardware</b>			
CPU	3000 II CPU & bus	3000 II CPU & bus	3000 II CPU & bus
Main Memory (Kb)	128	192	320
Discs (Mb)	15	2 (47)	2 (47)
Mag Tape (bpi)	1,600	1,600	1,600
System Console (1,920 char)	2640A	2640A	2640A
Async Controller	16-port	16-port	16-port
<b>Software</b>	MPE-II	MPE-II	MPE-II
	Sort	Sort	Sort
	Edit	Edit	Edit
	F Copy	F Copy	F Copy
	SPL	SPL	SPL
		IMAGE	IMAGE
		COBOL	COBOL
		RPG II	RPG II
			FORTTRAN
			IV
			BASIC

The operating system for all three of the HP 3000 Series II models is the Multiprogramming Executive II (MPE-II), a new version of the MPE-C, which is used for the 3000CX. MPE-II is a multilingual multiprogramming virtual memory operating system that allows timesharing to be done concurrently with batch processing. Improvements to the MPE-II include a new program dispatcher that alters a job's priority as a function of its being serviced, and firmware-assisted operating system functions. COBOL, FORTRAN, BASIC, RPG, and HP's System Programming Language (SPL) can be run concurrently in interactive or batch mode. Teleprocessing software is standard on Models 7 and 9, and optional on Model 5. An IBM 2780/3780 emulation package is optional on all models.

Accompanying the 3000 II introduction, HP announced that it will continue to enhance customer support by offering a wide variety of services including: preinstallation site planning, installation, personnel training, both hardware and software service at several levels, and programming consultation. Most of these services can be obtained on-site as well as at the manufacturer's facilities.

The new 3000 II system was announced in May 1976, and first deliveries were in June of the same year.

## COMPATIBILITY

The HP 3000CX is upward compatible with the HP 3000 Series II. An upgrade option will cost approximately \$75,000, with a rebate of up to \$10,000 available. User programs should execute with few or no changes. Since the 3000 II uses a new, more accurate floating-point system, programs that use FORTRAN double precision, and BASIC long data options will require examination, and probably modification.

The 3000 II can use the same peripheral devices as the 3000CX, although some new devices have been made available.

## PERFORMANCE AND COMPETITIVE POSITION

The degree of support required by business users is frequently greater than that of a mini user because business end users are usually not well-versed in computers. Since one of Hewlett-Packard's strong points as a mini supplier has been its service and support, it is only natural for Hewlett-Packard to have expanded into the business computer field, where users typically need good support from the manufacturer. Hewlett-Packard's sizeable sales and service network should give them an advantage over the smaller business computer manufacturers who still have to rely to a great degree on system houses, software houses, and service bureaus to provide program support.

The fact that other mini manufacturers (Digital Equipment in particular) have made successful inroads into this sector bodes well for Hewlett-Packard.

The new 3000 II increases both the throughput and the memory capacity of the former 3000CX machines, with a drop in price. Hewlett-Packard has attacked the business data processing market simultaneously at two levels — small business computers and small-to-medium general-purpose computer systems. The Model 5 is the configuration designed for the mini-midi computer market, especially for terminal-oriented applications in both stand-alone and distributed processing environments. Model 7 competes with small business computers, and Model 9 vies with small-to-medium general-purpose computers.

Model 5 is the configuration aimed at the small-to-medium general-purpose commercial, scientific, and educational markets. The PDP-11/70 and the Data General ECLIPSE systems are typical competitors.

Model 7 is the configuration designed to compete in the small business computer market. Although Hewlett-Packard does not have the extensive software a company like IBM has, the price/performance of the HP 3000 Series II and the availability of the IMAGE data base management system will be of particular interest to System/3 Model 10 users as an upgrade system. Hewlett-Packard has an upgrade package for these particular users in anticipation of the demand from this area. The 3000 II will also compete with other terminal-oriented small business systems made by Burroughs, because its speed and memory size allow greater expansion for growing users.

Model 9 is the configuration designed to compete in the low end of the general-purpose computer market. Here Hewlett-Packard meets systems like the DECsystem-20 and the lower end of the IBM 370 line. Since the low end of the general-purpose computer market is largely batch oriented and the Hewlett-Packard and DECsystems are terminal oriented, the attack on the big computer makers is an indirect one: Hewlett-Packard offers a system for a batch user who wants to expand into distributed processing instead of upgrading to a larger batch system.



## USER REACTIONS

Two of the first HP 3000 Series II users were interviewed. One user, an aircraft company, was expanding its on-line inventory computer facility. It already had an HP 3000 Model 20 and decided to stay with Hewlett-Packard, but not before it also had considered an IBM and a Data General system. One reason it decided to stick with HP is the IMAGE data base software, and the good, overall hardware/software package provided by HP. At the time of the interview this user had only done program development on the 3000 II; it had not yet been used to run on-line inventory.

A second user, a small drug company, is also upgrading from an HP 3000 Model 20 that had been used for business accounting (accounts payable, general ledger, etc). The Model 20 had 128K bytes of fixed disc and 15 terminals. The user obtained a 3000 II with 392K bytes of memory, and simply transferred all the peripherals from one system to the other. Programs were also being directly transferred; no re-programming was needed. The company found that the extra memory enabled it to do real multiprogramming, with three jobs running simultaneously and no degradation to terminal response time (about seven or eight terminals were usually operating concurrently). This had not been the case with the 3000 Model 20. This user also liked the fact that the power fail/restart facility did not require operator intervention, and that the operator command set allowed much more flexibility in job control and change of priorities.

## CONFIGURATION GUIDE

The HP 3000 Series II is available in three standard configurations — Models 5, 7, and 9. All models use the same processor and have the same basic mainframe architecture. The configurations differ mainly in the amount of main memory they support and the range of peripherals they attach.

- Model 5 — includes CPU, 128K bytes of fault control MOS memory, a 15M-byte swapping disc, a 1,600-bpi magnetic tape drive, a system console, and a 16-port asynchronous terminal controller. It can be expanded to include 256K bytes of memory as well as any peripherals available for the 3000 II. The MPE-II operating system is included. There are 12 slots for additional peripherals.
- Model 7 — includes CPU, 192K bytes of fault control MOS memory, two 47M-byte disc units, a 1,600-bpi magnetic tape drive, a system console, and a 16-port asynchronous terminal controller. Packaged software features MPE-II, COBOL, RPG, and the IMAGE data base management system. Memory can be expanded to 256K bytes. There are eight slots for additional peripherals.
- Model 9 — includes CPU, 320K bytes of fault-control MOS memory, two 47M-byte disc units, a 1,600-bpi magnetic tape drive, a system console, and a 16-port asynchronous terminal controller. Packaged software features MPE-II, COBOL,

RPG, FORTRAN, BASIC, and IMAGE. Memory can be expanded to 512K bytes, and there are 14 slots for additional peripherals. Table 1 outlines basic 3000 II system configurations.

There are restrictions on the number and size of the peripheral subsystems. Disc storage can be expanded to 436M bytes in a configuration of four 15M-byte drives and eight 47M-byte drives (two subsystems). Two magnetic tape subsystems of eight drives each can be included. A maximum of four line printers, two card readers, one card reader/punch, one paper tape reader, one paper tape punch, three emulation subsystems, and 64 terminals (counting the console) can be accommodated. Table 2 lists peripheral devices.

**Table 2. HP 3000 Series II: Peripherals**

Model	Description
<b>Discs</b>	
30129A	Cartridges; 14M bytes, 25-msec access
30102A	Moving head; 47M bytes, 29-msec access
<b>Magnetic Tapes</b>	
30115A	9 trk, 800 bpi, 36KB/sec
30115A-100	9 trk, 1,600 bpi, 72KB/sec
<b>Card Readers/Punches</b>	
30106A	600-cpm reader
30119A	Reader/punch, 200 spm/30-75 cpm
30119A-001	Keyboard + verify
<b>Printers</b>	
30118A	600 lpm, 64-char set, 132 col
30118A-002	128-char set opt
30128A	1,250 lpm, 64-char set, 132 col
30128-001	96 char opt
30127A	300 lpm, 64-char set, 132 col
30127-001	96-char set
30133A	600 lpm, 64-char set, 132 col
30133A-001	96 char
<b>Paper Tape</b>	
30104A	Reader, 500 cps
30105A	Punch, 75 cps
<b>Terminals</b>	
2640A	CRT, 24 x 80 char
2644A	Mini data station; CRT, 24 x 80 char
2762A	Printing terminal, 30 cps
2762B	Printing terminal, 120 cps
<b>Data Communications</b>	
30032B	16-port async channel controller
30130C	2780/37-0 emulation system
30300B	Programmable controller
30301B	Real-time programmable controller

## MAINFRAME

The HP 3000 Series II does not differ much, architecturally, from its predecessor, the 3000CX. The 3000 II has been implemented with more LSI circuitry to achieve higher speeds, lower power requirements, and lower costs, and its memory handling capabilities have been expanded to allow up to a half-million bytes. The instruction set has been expanded, and portions of the operating system have been microcoded, which contributes, HP claims, to increased system throughput. There are also a great many more registers available to the user. Table 3 lists mainframe characteristics.

**Table 3. HP 3000 Series II: Mainframe Characteristics**

<b>Central Processor</b>	
Type	Microprogrammed
<b>Control Memory</b>	
Size	2,048 (32-bit)
Use	Firmware
No. of Internal Registers	38
<b>Addressing</b>	
Direct	Variable for instructions + data
Indirect	1 level, 64K
Indexed	Yes
<b>Instruction Set</b>	
Implementation	Microprogrammed
Number	209
Decimal Arithmetic	Yes
Floating-Point Arithmetic	Yes
User Microprogramming	No
<b>Priority Interrupt System</b>	
Operation Modes Levels	253
Main Storage Type	Semiconductor
Cycle Time (nsec)	700
Basic Addressable Unit	Word (16-bit)
Bytes/Access	2
Cache Memory	No
Min Capacity (bytes)	128K
Max Capacity (bytes)	512K
Increment Size (bytes)	64K
Ports/Module	1
Error Checks	Parity
Protection Method	Bounds/stack
Memory Management	Yes, stack
ROM	Interrupt handler loader, auto restart, microdiagnostics
RAM	No
<b>I/O Channels</b>	
Programmed I/O	Yes
DMA Channels	4
Multiplexed I/O (no. of subchannels)	2 (32)
Max Transfer Rate Over DMA	1.9 bytes
Simultaneous Operations	Yes

The hardware is organized around a central data bus along which all hardware modules are interfaced. The CPU, I/O processor, main memory, and channel control equipment use the central data bus as a common communications path. The primary drawback of the organization is that total system throughput is a direct function of the speed of the central data bus. Because the CPU uses four scratchpad registers that frequently serve as top-of-stack locations and do not require memory fetches for operands, significant processing can be done in the CPU itself with a consequent increase in throughput.

Each system module is interfaced to the central data bus by a Module Control Unit (MCU), which can be located on one or more cards in the module. The MCU effects all bus transmissions for its module.

### Central Processor

The central processor module is composed of three major components: the Central Processor Unit (CPU), the Module Control Unit (MCU), and an I/O Processor (IOP). The CPU and IOP share a common central data bus interface to memory through a common MCU which has parallel sets of logic for both processors. The IOP has

a higher priority in gaining access to the bus except when the CPU is in the middle of a memory transfer.

The CPU itself is structured in three logical sections: instruction decoder, processor registers, and arithmetic/logic unit.

The instruction decoder contains a current instruction register and next instruction register. The former is loaded from the latter by a microprogram signal; the next instruction register is loaded from memory. Use of the two registers in the design permits overlap of instruction execution with fetching of the next instruction from memory.

Also, the instruction decoder section contains the ROM and its major associated elements: a lookup table, preliminary ROM address register, ROM address register, ROM output registers 1 and 2, and a number of decoders for different fields of ROM words. The preliminary ROM address register provides an initial ROM microprogram address from decoded bits in the instruction word in the current instruction register. ROM output registers hold the 32-bit ROM word, which can be delivered in two 175-nsec clock cycles initially; thereafter, ROM words are pipelined at the rate of one per cycle.

Finally, a preadder in the instruction decoder aids in the efficient computation of absolute addresses for indexed memory reference instructions. It allows the final absolute address to be computed in only one cycle by simply adding the output of the preadder to the contents of the designated base register.

### Simultaneous Operations

Simultaneous operations within the 3000 II are effected through the standard operating system, MPE-II. From a hardware point of view, both overlapped operations and concurrent I/O, either on a multiplexor channel or among combinations of multiplexed operations, selector channels, and direct I/O sequences, are normal within the technology of the system. Additionally, main memory can be structured for either noninterleaved mode or two- or four-way interleaving.

**Data Structures.** The basic data structure of the 3000 II is a 21-bit word, 16 information bits, and a five-bit fault control word. The five-bit fault control word corrects all single-bit errors and many double-bit errors, and detects 30% of all multibit errors. The 16 information bits can be referenced on the eight-bit-byte or 16-bit-word basis, or on a two- or three-word basis in the case of floating-point values. Standard instruction formats use one word. In addition, identified code segments are provided with a special 16-bit status word.

**Special Registers.** Rather than having a small number of general-purpose registers in the 3000 II system, Hewlett-Packard departed from 3000CX design



by expanding the register set from 13 registers to 38. Of these, 20 are accessible to the programmer and/or the operating system, and the others are used by system functions such as interrupt and microprogram processing. The registers include four code segment pointers, eight stack pointers, four top-of-stack registers, two I/O registers, three memory address and data registers, two firmware address registers, nine scratchpad, flag, and interrupt registers, an index register, a status register, a switch register, a program clock register, a current instruction register, and a next instruction register. The registers are conditioned for the system's stack architecture and its division of program processes into separate code and data segments. With a single exception, all registers are 16 bits long. The register set can be broken down into code segment registers, data segment registers, and special-purpose registers. The first two groups are of significance in the processor's addressing scheme.

**Instruction Set.** Instructions are "pipelined" to improve throughput. While one instruction from the CIR register is being executed, the next instruction is being fetched and placed in the NIR register, overlapping operations. Microcode controls the operation of the instruction decoder and the hardware processor. The ROM control logic includes a set of 209 instructions for the user, including procedure call, exit, and other instructions that implement functions previously in operating system software.

In operation, each instruction routinely checks for bounds violations and will interrupt to an error vector if violations occur. The memory protect check is overlapped with the operand fetch; thus it has no effect on instruction execution time. Microinstructions are executed in 175 nsecs.

The stack architecture of the system provides the basic mechanism for a wide range of instructions. Virtually all of the computational and logical operations are performed through stack instructions that implicitly use stack-effective addresses. Additionally, many stack operations can be packed two per word to increase code density.

In addition to the stack operations, which include arithmetic (both integer and floating-point), logical, Boolean, shift, bit test, immediate, and register control, the system provides memory-to-memory moves, scan, compare, loop control, standard conditional branch, and program control instructions.

The I/O control and interrupt instructions/commands plus specific system and program control instructions are privileged and can be executed only by a privileged mode routine, normally the operating system.

## I/O Control

The HP 3000 II can logically accommodate up to 253 devices. Each device is referenced through a DRT, which is known to both the hardware and software. Moreover,

each device is identified by three characteristic numbers that are totally independent of each other: the device number or "name" by which it is known to the software; the device service priority; and the device interrupt priority. I/O operations are privileged and are normally performed through the facilities of the operating system. Concurrent I/O is limited only by the range of total system bandwidth. Simultaneous I/O that overlaps CPU processing is the normal mode of operation within the multiprogramming environment.

Multiplexor and selector channel operations provide direct memory access for medium- and high-speed devices. Direct I/O is used to transfer data between a low-speed asynchronous device and the top-of-stack.

Physical level I/O is initiated by a CPU instruction. Once initiated, the I/O processor executes a command chain out of memory and transfers data asynchronously with respect to the CPU. The command word is a 32-bit double word. Commands included in the I/O repertoire are jump, return residue (count), interrupt, end, control, sense, read, and write. As the count field is 12 bits long, it can provide for blocks of 4,096 words; provision is also made for command chaining.

Data chaining allows reading or writing data on a scatter/gather read/write basis. A full 16-bit data area address is provided in a command; thus, data can be read/written between any area of memory and an I/O device.

## MAIN MEMORY

Memory for the 3000 II consists of 64K bytes of MOS memory with a 700-nsec cycle time (350-nsec access). Each 16-bit memory word has five related error detection/correction bits appended in a special fault correction array (FCA) board for correcting single-bit errors and detecting some multiple-bit faults. A parity bit is retained when memory words are transferred over internal system buses. A memory control and logging (MCL) board controls memory module operation, interfaces the modules to the system, and keeps a log of the detected and corrected faults. This log is periodically updated and stored on disc for inspection by the maintenance engineer, so that consistently faulty chips can be replaced.

Memory array boards hold 64K bytes. The memory size of basic systems differs depending on the model: Model 5 has 128K bytes; Model 7 has 192K bytes; and Model 9 has 320K bytes. Models 5 and 7 can expand to 256K bytes, whereas Model 9 expands to 512K bytes. In Model 9, there are two memory controllers with up to 256K bytes each; both modules can operate concurrently.

Operating power is supplied by a rechargeable battery pack in the power supply. This allows up to 90 minutes of power to maintain memory data if a line power outage is experienced.

# HEWLETT-PACKARD CO. — HP 3000 SERIES II PRELIMINARY REPORT

In addition to main memory, the 3000 II makes use of a virtual memory scheme to swap memory segments back and forth from the disc.

## PERIPHERALS

See Table 2 for a listing of peripherals available for the HP 3000 II.

## DATA COMMUNICATIONS

Asynchronous terminals are attached to the 3000 II through the 30032B Terminal Controller. The terminal can support up to 16 terminals with optional memory expansion. Both the 2000CX and 3000CX will support up to 32 terminals in a timeshared environment. Additionally, the systems can be interfaced to other processors in a distributed network or can serve as remote job entry facilities and/or front-end processors to large computing centers.

The 3000 II Data Communications Controllers are as follows:

- 30032B Terminal Controller — async 16-channel; controls 16 103-type data sets.
- 30300B Programmable Controller Subsystem — to 200K words/sec; based on HP 2100 minicomputer; data acquisition, extended I/O processor.
- 30301B Real-Time Programmable Controller Subsystem — to 200K words/sec; based on HP 2100 computer; adds real-time instrumentation, data analysis, and software development to 30300B capabilities.
- 30130C 2780/3780 Emulation System — to 9,600 baud; all 2780 capabilities except six-bit transcode; all 3780 capabilities except reverse interrupt and conversational mode; 22 options; includes 30055A synchronous single-line controller.

The 3000 II supports the following HP terminals:

- 2640A CRT Terminal — 1,420 characters, supported in character mode only; 24 lines of 80 characters each; plug-in character sets.
- 2644A Mini Data Station — 1,920 characters, 24 lines of 80 characters each; dual magnetic tape cartridge drive; character/line mode with editing, forms mode, on-line or off-line data entry; to 2,400 baud.
- 2762A Printing Terminal — 30 cps; 75 columns; upper- and lower-case; 110, 150, or 300 baud asynchronous.
- 2762B Printing Terminal — 120 cps; 120 columns; upper- and lower-case; asynchronous.

The 3000 II will also accommodate the following non-HP terminals: IBM 2741, Memorex 1240, Execuport, GE TermiNet 300, TTY ASR 35, TTY ASR 37.

## SOFTWARE

The 3000 II fundamental operating software consists of the Multiprogramming Executive (MPE-II) supported by

a text editor, programming debugging aids, a file-copying utility, a sort and merge package, and a System macro Programming Language, SPL. Additionally, RPG, COBOL, FORTRAN, and BASIC languages are available, as well as HP's data base management subsystem called IMAGE, a data base inquiry facility called Query, a library of data entry routines, a scientific library, other utilities, and a variety of applications software packages. Notable among applications packages are two educational administration packages, one for attendances and grade data base management, and one for scheduling and student assignments.

## Operating System

The 3000 II Multiprogramming Executive (MPE-II) is a disc-based timesharing operating system with batch capabilities, implemented in virtual memory/stack processing architecture. It differs from its predecessor, MPE-C, in its concurrent multilingual capability, which allows FORTRAN, COBOL, RPG, BASIC, and SPL programs to run concurrently.

MPE-II's stack processing architecture allows both recursive and reentrant user programs, with code automatically separated from data. Thus more than one user can share a copy of a program without worrying about changes instituted by another user. Resources are allocated dynamically to make efficient use of memory.

On-line terminal processing handles multiple terminals, serviced in accordance with a round-robin, time slicing queue. These jobs are serviced at a higher priority than batch jobs because the timesharing objective is to respond to terminals within a reasonable time period. Besides use for program development, on-line terminals can access all the facilities of the system for full remote batch processing capability. Common terminal uses include computer-aided instruction and information retrieval. Additionally, the operating system provides automatic restart following power-fail system interruption.

Disc storage is used as an extension of main memory, with programs and data automatically augmented and moved back and forth between disc and main memory. MPE-II also provides a spooling facility using the disc as intermediate storage for both input and output. Both the virtual memory and spooling functions are transparent to the user. The operating system requires approximately 37K bytes for the executive kernel functions and table-swapping, supervisory-type procedures on a dynamic basis.

## Languages

Hewlett-Packard provides one unique and three standard high-level programming languages. SPL/3000 is both high-level and machine dependent. FORTRAN, COBOL, and BASIC provide common language facilities for scientific, timesharing, and commercial applications.

**SPL/3000.** Bridging the gap between assemblers and machine-independent high-level languages, SPL/3000 supplies an assembler's efficiency with a compiler's ease of programming. It sacrifices, however, the inherent compatibility of the high-level language. SPL/3000 is similar in structure and syntax to ALGOL. All systems software, including the SPL/3000 compiler, is written in SPL/3000. Routines written in SPL can be called by FORTRAN or BASIC programs.

**FORTRAN.** The FORTRAN compiler accepts an extended version of ANSI Standard (X3.9-1966) FORTRAN language. Added capabilities include character string manipulation with multidimensional string arrays; all MPE-C file capabilities; recursive subroutines with dynamic allocation of temporary local storage; names up to 15 characters long; and mixed-mode arithmetic. FORTRAN IV programs written for the Hewlett-Packard 2100 family of computers can be compiled and run by using FORTRAN/3000.

**COBOL.** COBOL/3000 is an implementation of the highest level of ANSI Standard COBOL, as well as the highest level of United States Federal Standard COBOL as defined by the National Bureau of Standards. In addition, COBOL/3000 provides interprogram communications with COBOL or non-COBOL subprograms. It requires the SORT/3000 subsystems to implement the SORT verb.

**BASIC.** 3000 II BASIC is available in two operational forms: an interactive interpreter mode and a full compiler mode, which allows procedures developed through the interpreter to be compiled into object programs. Execution time can be speeded up by factors of from 10 to 100 times for computer-bound compiled BASIC programs over those executed through the interpreter.

The BASIC language is an extended version of the standard terminal language. Provisions include the following features: four numeric data types (real, integer, complex, and extended precision); mixed-mode arithmetic; multiple line statements and functions; picture I/O formatting; program chaining with common storage; latency timeout factors; external routine calls; strings and string arrays; random and sequential access to files; user ability to create/purge files; password file security; trace/debug facility; program CALL to treat any program as a procedure; IF-THEN-ELSE statements; and DO blocks. Hewlett-Packard calls this the most powerful version of BASIC ever provided with any computing system. Additionally, programs written for the HP 2000 time-shared BASIC systems can run on a 3000 II by using BASIC/3000.

**RPG II.** The 3000 II Report Program Generator II provides standard RPG facilities for report definition and file access. The generator operates under MPE-II utilizing the file processing facilities and file structures of the system.

## Applications Software

**IMAGE/3000.** IMAGE/3000 is a data base management system that operates in a batch and terminal environment. In a batch environment, IMAGE syntax interfaces with the host language (FORTRAN, COBOL, or SPL) through CALL statements. The package provides facilities for describing data base structures; accessing and maintaining developed files; and backup, recovery, and restructuring techniques.

The data base is structured into a network of master and detail record relationships so that various information units can be selectively retrieved or stored. The system provides security and privacy at the data base, record, or field level; and it can handle a total of eight different data types. Additionally, data can be accessed sequentially or directly by relative record number. Deleted record space is automatically reusable.

**Query/3000.** Query/3000 is designed primarily as a terminal system service that provides facilities for addressing IMAGE/3000-stored data, report formatting and generation, and data base updating. The package provides a set of 17 English-like commands in a host language format. Besides security provisions for protecting unauthorized access to private files and records, it can be executed in a batch mode through the standard batching facilities of MPE-II.

**Data Entry Library.** The Data Entry Library includes procedures for creating, chaining, updating, and deleting up to 10 forms for CRT terminals with page mode operation. It also includes eight procedures for editing data and terminal manipulation. Procedures can be called from BASIC, COBOL, FORTRAN, and SPL programs.

**Student Information System (SIS/3000).** SIS/3000 is an administrative package for educational institutions. It includes a district data base and maintenance module, a family information facility, a mark reporting subsystem, and an attendance accounting subsystem. SIS is written in COBOL and uses the IMAGE software for data base management, allowing both terminal and batch access and development of a District Data Base. SIS/3000 is compatible with SAS/3000.

**Student Assignment System (SAS/3000).** SAS/3000 is an administrative scheduling package for educational institutions. It builds master schedules, assigns students to classes, provides reports, and maintains school and student files. Assignments are made based on a variety of school-defined priorities. It checks for co-requisite courses, ability and grade-level restrictions, class and semester load balancing, and a variety of other scheduling problems. Individual students can be scheduled on-line. SAS/3000 is compatible with SIS/3000 so that information can be transferred to the District Data Base.

# HEWLETT-PACKARD CO. — HP 3000 SERIES II PRELIMINARY REPORT

## MAINTENANCE AND SUPPORT

Hewlett-Packard is noted within the industry for its product support. The company maintains 172 field offices in 65 countries throughout the world, including 60 service facilities in the United States and Canada backed by five regional offices. Two service and warranty plans are available under terms of the purchase agreement. One provides for a "parts only" warranty for 15 months; a second provides full service, parts, and labor for 90 days. Follow-on agreements can provide for guaranteed response times and full service or operate on a per-call time-and-materials basis.

Hewlett-Packard also provides a set of diagnostics that function as a task of the operating system. A stand-alone set runs directly on the CPU without operating system aid. In addition, a set of microprogrammed micro-diagnostics can be executed and transmitted directly to Hewlett-Packard through a modem and common carrier line for immediate assistance on difficult problems.

## PRICE DATA

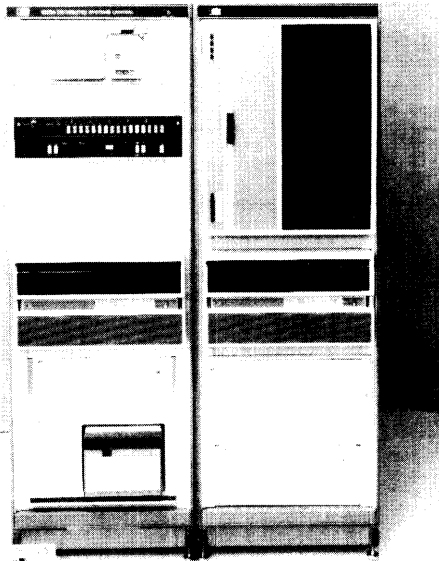
Model Number	Description	Purchase Price \$	Monthly Maint. \$
32415A	Model 5 Computer System with 128Kb memory	110,000	619
32417A	Model 7 Computer System with 192Kb memory	150,000	859
32419A	Model 9 Computer System with 320Kb memory	190,000	926
30408A	Upgrade Model 5 or Model 7 to Model 9 (original system must have 256Kb memory)	40,000	
30409A	Upgrade HP 3000 or 3000 CX to Model 9 (original system must have 256Kb memory)	75,000	
30008A	64Kb Memory Module	5,700	21
30411A	Memory Expansion Sub-system	16,500	21
<b>High-Speed Peripherals</b>			
30102A	Disc File Subsystem & Control; 47Mb	27,500	172
30129A	Disc Drive Subsystem & Control; 15Mb	15,000	96
30329A	Disc Drive without Control; 15Mb	9,975	70
30333A	Disc Pack for 30102A	620	0
12940A	Disc Cartridge	180	0
30115A	Magnetic Tape Drive, Control, & Cabinet, 9-track, 800 bpi, 45 ips	12,000	85
-100	Same as 30115A except 1,600 bpi	14,625	94
-200	Same as 30115A except without control	9,550	64

Model Number	Description	Purchase Price \$	Monthly Maint. \$
<b>Low-Speed Peripherals</b>			
30118A	Line Printer Subsystem; 132 cols, 64 char, 200 lpm	9,950	83
-001	Same as 30118A except with 128-char set	10,200	83
30127A	Line Printer Subsystem; 136 cols, 64 char, 300 lpm	14,000	138
-001	Same as 30127A except with 96-char set	16,000	138
30133A	Line Printer Subsystem; 132 cols, 64 char, 600 lpm	19,000	153
-001	Same as 30127A except with 96-char set	21,000	153
30128A	Line Printer Subsystem; 132 cols, 64 char, 1,250 lpm	39,100	159
-001	Same as 30128A except with 96-char set	41,100	159
30106A	Card Reader Subsystem; 600 cpm	7,700	64
30119A	Card Reader/Punch Subsystem; reads 200 cpm, punches 75 cpm	17,500	129
30104A	Paper Tape Reader Subsystem; reads 500 cps	3,585	23
30105A	Paper Tape Punch Subsystem; punches 75 cps	5,000	48
<b>Terminals</b>			
2640A	Interactive Display Terminal; char mode, 64 uppercase Roman char	3,000	25
-001	Same as 2640A except with 128-char set	3,100	25
2644A	Mini Data Station; char mode, 64 uppercase Roman char, 2 cartridge tape transports	5,000	40
-001	Same as 2644A except with 128-char set	5,100	40
2762A	Printer Terminal with Keyboard; 75 cols, friction feed	4,950	29
-017	Same as 2762A except with pin-feed	5,145	29
2762B	Printer Terminal with Keyboard; tractor feed, 120 cols 10/30/120 cps, switch selectable	6,575	58
<b>Data Communications</b>			
30130C	2780/3780 Emulation Sub-system	4,500	25
<b>I/O Expansion</b>			
30030B	High-Speed Selector Channel	3,600	13
30032B	Async Terminal Controller	3,000	15
<b>Software</b>			
32101B	BASIC/3000 Interpreter	4,500	10
32102B	FORTRAN/300 Compiler	4,500	10
32103B	BASIC/3000 Compiler	4,500	10
32104A	RPG/3000 Compiler	4,500	20
32213B	COBOL/3000 Compiler	4,500	20
32215A	IMAGE/3000 (data base management subsystem)	1,000	30
32216A	QUERY/3000 (data base inquiry subsystem)	1,000	10



## HEWLETT-PACKARD CO.

### 9700 Series Distributed Systems, System Report



#### OVERVIEW

The HP 9700 Series Distributed Systems provides Hewlett-Packard (HP) with another entry into its traditional markets of data acquisition, scientific and industrial control, and medium-sized scientific systems. The HP 9700 is not a new system but rather a new way of marketing the power of several current HP systems.

The HP 9700 is an end-user system that can provide a central control processor and any number of remote or satellite processors. The distributed processing aspects of the network are inherent in the systems' hardware compatibility (all processors, central or satellite, are versions of the same processor, the HP 21MX) and its mature hardware/software communications facilities.

The HP 9700 Distributed System requires at least a 9700A Distributed System Central and an HP control system. Beyond that, the composition of the network could include any of the following HP elements: the 9602A, 9603A, and 9604A Scientific Measurement and Control Systems; the 9611A Industrial Measurement and Control System; the 9640A Real-Time Multiprogramming and Computational System; the 9603R Remote Scientific Measurement and Control Station; and the 9611R Remote Industrial Measurement and Control Station. Figure 1 is a diagram of a typical 9700 Series Network Configuration.

The network is supervised by the operating system at the 9700A Distributed System Central, and each processor, central or satellite, operates under the supervision of

its own operating system. The processing and equipment resources as well as the peripheral storage of the 9700A may be used by the satellite processors, and the 9700A can control the work load and processing schedule of each satellite. In addition, the entire 9700 Distributed System can interface to a system external to the network, such as an IBM System/360 or 370, an HP 3000 system, or another 9700 Distributed System.

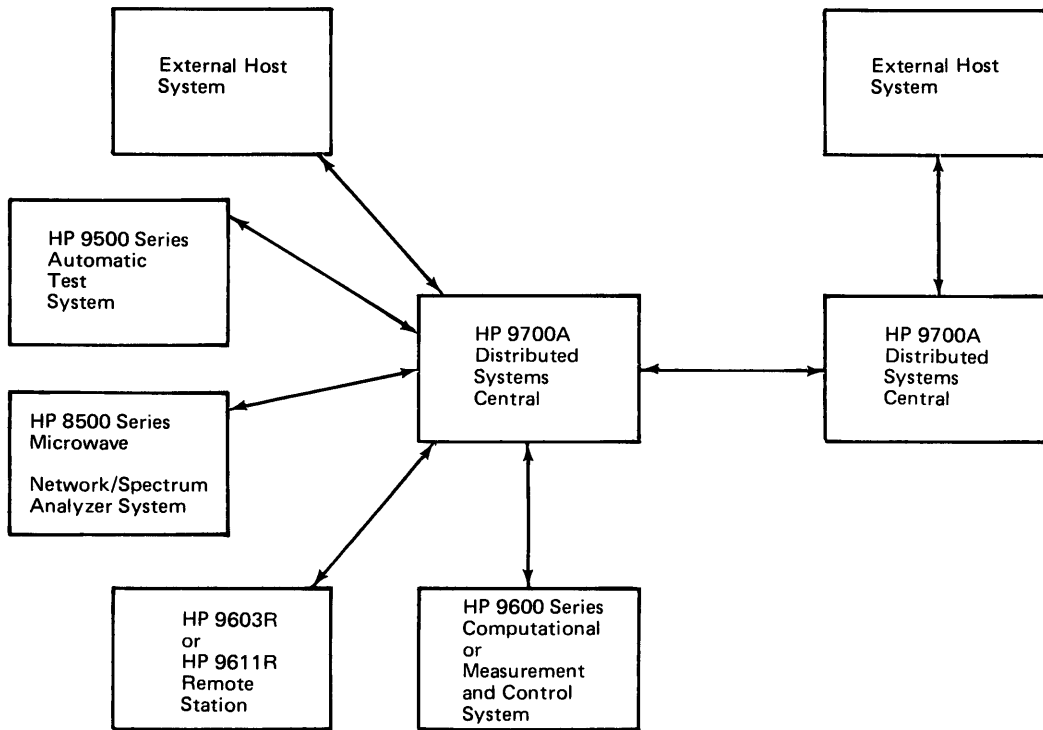
**Network Structures.** The network structures supported by the 9700 Distributed System include the familiar star- or host-dominated network configuration and the ring or node-to-node configuration. Within the star network each remote processor (properly termed "satellite,") is a semiautonomous unit within the system. It normally performs a specific, dedicated operation. However, it can "off-load" some functions and operations onto the host processor and can use the host's facilities for operations such as input/output or file structured data, program development, test and load, and initialization of defined time and/or event triggered processes.

In the satellite/host relationship the satellite relies on the central system for direction in certain areas, including resource sharing, and, under specified critical conditions, must accept and effect the instructions and directions of the central system. The central system must be structured to respond to the satellites in the network, and be capable of initiating operations at the satellite. Also, the central system is responsible for interfacing with any systems outside the network.

The ring network is essentially an extension of the star network. It provides the communications facility to distribute the functional requirements of a system to any number of interconnected processors: one node may function as a communications processor, a second as a data base manager, and a third as a regular data processing system. Also, a star network may plug into the ring at any given point. No one processor would take charge of the network; each of the processors including the central system processor of the star network would be fairly autonomous. The degree of control, interprocessor communications, and multiprocessing flexibility available with

#### HEADQUARTERS

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76-252

Figure 1. Typical Configurations for HP 9700 Series Distributed Systems

a star network is not necessarily available with a ring network. In a ring network each unit has its own domain of interest; each performs a well-defined function; each, in effect, is a central host system in itself.

**Supporting Software.** The 9700A Distributed System Central operates under control of HP's Real-Time Executive II or III (RTE-II, RTE-III), in conjunction with a Central Communications Executive (CCE). The satellite processors operate under control of either the Basic Control System (BCS), Real-Time Executive-B (RTE-B), or Real-Time Executive-C (RTE-C). Each satellite's software includes a version of the Satellite Communications Executive (SCE); the version used depends on the operating system installed and the services required. See Tables 1 and 2 for an analysis of HP 9700 Distributed Systems software support.

Both RTE-II and III are disc-based multiprogramming systems. RTE-III will support up to 64 user paging partitions in a maximum memory environment of 256K words. It also provides a file management system, concurrent processing and program development, concurrent multiterminal access to all system members, and I/O spooling. RTE-II, a subset of RTE-III, operates in a maximum memory environment of 32K words and provides a batch background-multiprogramming foreground type of operation. In RTE-II, both file and spooling facilities are optional features.

The BCS is essentially an interrupt-driven program monitor providing for execution of dedicated programs, an I/O control system, a linking loader, and program development facilities for FORTRAN II, ALGOL, and HP Assembly language programs.

RTE-B is a multitasking (up to 16 user tasks) time and/or event driven operating system with a device independent I/O control system, multiterminal operation, and program development via HP's BASIC interpreter, FORTRAN II, and Assembly languages.

RTE-C is a multiprogramming time- and/or event-driven operating system providing complete I/O capabilities and program development via FORTRAN II and FORTRAN IV and HP Assembly language.

In the satellite systems the program development facilities associated with each operating system are most critical when the satellite is operating in a stand-alone environment. Once a satellite is linked into the network, program development can be accomplished on the central host via the satellite's console or directly at the host.

The Central Communications Executive (CCE) resident in the 9700A provides the software interface among satellites, and to the external central/host processors. The CCE performs translation and queueing functions, maintains



**Table 1. HP 9700 Series: Software and Communications Linkage**

SYSTEM NODE	SOFTWARE	OPERATING SYSTEM	COMMUNICATIONS EXECUTIVE	LINKAGE TO	AVAILABLE LANGUAGES
9700A Central		RTE-II RTE-III	CCE	Each Satellite IBM 360/370 HP 3000 Another 9700A	FORTRAN II/IV, ALGOL, Assembly; Conversational Real-Time BASIC
<b>Satellite Systems</b> 9602A, 9603A 9611A		RTE-B RTE-C	SCE/1, SCE/4 SCE/1, SCE/5	Central and Network Environment	Conversational Real-Time BASIC FORTRAN II and Assembly
9604A 9640A		BCS RTE-B RTE-C	SCE/1, 2, 3 SCE/1, SCE/4 SCE/1, SCE/5		FORTRAN II, ALGOL, Assembly Conversational Real-Time BASIC FORTRAN II and Assembly
9603R, 9611R		BCS Nonintelligent remote stations	SCE/1, 2, 3 Not applicable		FORTRAN II, ALGOL, Assembly Not applicable

**Table 2. HP 9700 Series: Software Space Requirement**

	SYSTEM MAIN MEMORY REQUIREMENTS* (WORDS)	PROCESSOR MEMORY REQUIREMENT (WORDS)	RESIDENCY	FUNCTION	AVAILABLE EXTENSIONS
Operating Systems					
RTE-III	14846	32K-256K	Disc	Central	RJE IMAGE/2000
RTE-II*	6000†	16K-32K	Disc	Central	RJE IMAGE/2000
RTE-C	3750‡	8K-32K	Main Memory	Satellite	RJE IMAGE/2000
RTE-B	8700‡	12K-32K	Main Memory	Satellite	IMAGE/2000
BCS	6200	8K-32K	Main Memory	Satellite	

**Notes:**

- \* Exclusive of global areas, common, library, etc. and Communications Executive.
- † Does not include I/O drivers and 1,024 words of communication area.
- ‡ Does not include 1,024 words of communication area.

orderly system communications, and provides a virtual satellite-to-central system resources interface.

The Satellite Communications Executives (SCE), which provide the interface to the CCE, are installed at the satellite, and are based on either the operational requirements of the individual satellite or the operating system installed. There are five types of SCE (SCE/1 through SCE/5).

## PERFORMANCE AND COMPETITIVE POSITION

Because the 9700 Distributed System is based on the HP 21MX, each of the individual elements within the system maintains its relative competitive position with other similar systems as provided by DEC, IBM, Data General, and Microdata. However, at the network level, Hewlett-Packard's major competition comes from MODCOMP's MAXNET system. Both the 9700 and the MAXNET have virtually the same functional capabilities from an operating system/communications control viewpoint. The differ-

entiating features between the two networking systems lie in their intersatellite communication capabilities and architectural arrangements. MAXNET allows direct intersatellite communications, whereas HP systems can communicate only through the host. Architecturally, the 9700 system is a bilevel system: a host system on one level communicates with satellite systems on a lower level. MAXNET permits a multilevel hierarchy of systems, a central host system on the first level and satellites cascaded in sub-levels. Both networking systems have been successful, and the bottom line for both lies in services and support external to the distributed network itself.

## USER REACTIONS

Hewlett-Packard claims over one hundred distributed systems customers. The users interviewed are all pleased with their systems; all commented on HP's willingness to work with them on improving their systems.

**Laboratory.** The laboratory of a major research company is using three HP distributed systems. The first has

## HEWLETT-PACKARD — 9700 SERIES DISTRIBUTED SYSTEMS, SYSTEM REPORT

been operational for three years and includes two microwave systems and a remote computer running under RTE-I (which has since been replaced by the vendor with RTE-II). This user considered the RTE-I system poorly designed with a lot of inherent problems. His other two systems use RTE-II software (one is an RTE-II to RTE-C system and the other an RTE-II to RTE-II system) and have been working "perfectly" for over a year. One of the RTE-II systems talks to a microwave analyzer and an automatic spectrum analyzer, both older systems that were formerly stand alone. Since RTE-II is fully compatible with the analyzers, the lab can use the software that they spent years developing. Application programs can be compiled at the central site and down-line loaded to the analyzers.

This user has three criticisms of the HP Distributed System; all three are being corrected or have been corrected by HP. First, he feels that the system is designed backwards (i.e., from remote to central) and would benefit from a reversal in the design. Second, he feels there is a real need for a system-to-system interface; currently, calls are possible only between satellites, and the user is obliged to supply the communications software. The third problem, inherent in the calling sequence, is that both systems must be rebootstrapped if either end goes down. Hewlett-Packard has changed this with new software. But this user says the system generally works "beautifully."

**Oil Company.** A top Fortune 25 company is setting up a network to run its oil-pumping operations. This will consist of an HP 9700A central system tied to five field-site computers over 2400-baud lines. Each field site will also use an HP 9700A to monitor operations and perform limited control of the oil field, and to act as host to remote process-type terminals from another manufacturer. One field site has a high data rate because it monitors 70 pumping units; so this satellite is connected to the host by a 1-megabit direct interface. Another field site operates as a remote network multiplexor and uses an HP computer (with a CRT and two printers) for input/output.

The central HP 9700 polls the field sites every half-hour, collecting data and updating files. The central computer is also connected (over a 4800-baud line and HP's 2780 RJE interface) to an IBM System/370 and a Univac 1100 at the company's central information center, which uses the data for computerized production control and for calculating royalties paid to leasees of each oil well.

This user has had extensive experience in implementing a control system; it has used an IBM 1800 control system for 5 years, during which most pitfalls were successfully overcome.

The oil company's initial study group spent a year developing the network plan. When bids were let out about 2 years ago, twelve companies responded. Because the bidder was required to supply off-the-shelf network software, only the MODCOMP and Hewlett-Packard bids were ultimately considered. The final decision was apparently a toss-up, HP winning on the basis of its size, age, and

reputation. (MODCOMP was only 4 years old at the time and quite small.) Hewlett-Packard is shipping the last piece of software at the same time that the oil company's applications software will be ready. Testing and debugging are being done centrally, before placing satellites in remote sites. The first system is scheduled to be field-installed by September, with subsequent installations at 2- or 3-week intervals; the network should be completely operational by the end of 1976. When this is accomplished, the company expects to derive the following major benefits from its distributed system:

- Minimize the number of specialized people needed to check monitoring devices, particularly in remote sites.
- Improve control over the entire operation.
- Standardize software at remote sites through central control.
- Accommodate the needs of individual field sites.
- Save money by providing more comprehensive data for accounting and planning purposes.

The problems encountered have not been unusual, considering the size of the network and the state of networking art involved. Hewlett-Packard had to develop some software for this application, perhaps not exclusively, but it was not off-the-shelf, and it did take time. Both parties were moving targets at times, with the oil company's specifications not firm, and initial problems with a new HP disc. Overall, however, the user is pleased with the system. Hewlett-Packard has been responsive to problems and has honored its commitments. The user is planning to install a second 9700 Central System for program development.

**Laboratory.** A company involved in energy resource management has three HP 2100S computers operating in a distributed system environment, one computer acting as the central CPU and the other two as satellites. The satellites gather data from reed relay scanners, digital voltmeters, and timer counters; the central CPU reduces the data into graphs and printed reports. All I/O devices are linked to the central unit.

This system was one of the first HP Distributed Systems to be installed, and it has been operational for over 2 years. Planning took 80-100 man hours over a period of 3 to 4 months; implementation took about 6 weeks. The first software delivered was unworkable; so a second set (that worked) was delivered without charge. Enhancements since then have improved operations considerably; the software has been trouble-free for the last 6 months. (Another user we interviewed had a similar system installed a year later; RTE-II and the distributed processing systems were fine.)

This user finds he can recover from hardware downtime within 24 hours. If a satellite goes down, the system continues to operate, but if central goes down the whole system goes with it (HP claims that this need not be the case). This laboratory has about a dozen computers, so hardware can usually be swapped and the system is up again within a half-hour.

The biggest drawback to the system is that communication between satellite and central is slowed by software overhead. The biggest advantage is that satellites can handle some real-time functions so that central is freer to execute batch processing.

This user finds the HP Distributed System both modular and flexible, and he likes being able to buy the parts he wants. The user is upgrading to a 21MX Central with 64K words of memory and RTE-III, and will then use the current central as a third satellite.

**University.** A state institute of technology set up an HP 9700 Distributed Network specifically to tie old HP

2000 computers to a central site, a 32K-word HP 2100S. The school has eight computers used as stand-alone systems, and up to three of them can be connected to central at one time. Since the satellites are all 8K-word systems, they run under Satellite Communications Executive (SCE II) software, which provides an interactive operator interface. Communications from a satellite to central is via a hardwired line at 1 megabit per second. Central has disc storage and peripherals which the satellites can address as if they were local devices.

Planning for this system took about 2 months. The system was operational a month after the hardware and software were delivered, and has been for over 2 years, though

**Table 3. HP 9700 Series: Equipment for Distributed Network System Elements**

	Distributed System Central	High-Accuracy Scientific Meas. & Control System	Scientific Meas. & Control Station	High-Speed Variant of 9603A	Industrial Meas. & Control	Real-Time Multi-programming & Computer System
	9700A	9602A	9603A	9604A	9611A	9640A
<b>BASIC HARDWARE</b>						
2108 A (Basic Memory)	(32K)	(16K)	(16K)	(8K)	(16K)	(16K)
ROM Loader	•	•	•	•	•	•
Memory Protect	•	•	•	•	•	•
Direct Memory Access	•	•	•	•	•	•
Dual-Channel Port Controller	•	•	•	•	•	•
Time Base Generator	•	•	•	•	•	•
Power Fail Recovery	•	•	•	•	•	•
Distributed System Kit	•	•	•	•	•	•
<b>PERIPHERALS</b>						
Paper Tape Reader	•	•	•	•	•	•
Cartridge Disc (4.9M bytes)	•	•	•	•	•	•
<b>INSTRUMENTATION</b>						
Integrating DVM A/D Subsystem	(opt)	•	•	•	•	•
Analog I/O Subsystem	(opt)	•	•	•	•	•
Digital I/O Subsystem	(opt)	•	•	•	•	•
<b>OPTIONS</b>						
Additional Peripherals*	•	•†	•	•†	•	•
Expanded/Additional Instrumentation	•	•	•	•	•	•
Expanded Memory To: Remote Data Transmission Subsystem	(256K) •	(32K)‡ (RTE-C Config)	(32K)‡ (RTE-C Config)	(32K)	(32K)‡ (RTE-C Config)	(32K)‡
<b>SOFTWARE</b>						
Operating System	RTE-II/III	RTE-B/C	RTE-B/C	BCS	RTE-B/C	RTE-C
Communications Exec Languages	CCE	SCE1/4	SCE1/4	SCE1/2/3	SCE 1/4	SCE 1/5
FORTAN	•	•	•	•	•	•
ALGOL	•	•	•	•	•	•
Conversational Real-Time BASIC	•	•	•	•	•	•
HP Assembly	•	•	•	•	•	•
Interactive Editor	•	•	•	•	•	•
Software Library	•	•	•	•	•	•
Batch Spool Monitor	•	•	•	•	•	•
Remote Data Base Access to IMAGE/2000	opt	opt	opt	opt	opt	opt

**Notes:**

\* Includes all available Peripherals: Disc, Tape, Special Purpose, Etc.

† Includes Remote Stations

‡ When these devices are used as Centrals, memory is expandable to 256K words.

# HEWLETT-PACKARD — 9700 SERIES DISTRIBUTED SYSTEMS, SYSTEM REPORT

not without some problems. The original software, which used RTE-I, was inadequately documented, and downline loading was difficult to implement. The user upgraded to RTE-II, but then the distributed system was not completely compatible. Hewlett-Packard replaced the distributed processing software.

Although this user's experience with the system has been essentially good, he feels it is too complicated a system for use by students who are concerned not so much with computers as with engineering problems; consequently, he expects to add some HP calculators to the system.

## CONFIGURATION GUIDE

The basic 9700 Distributed Processing System consists of one central system and one or more satellite systems. Basic configurations for the series systems are outlined in Table 3, which shows the major hardware and software available for each unit. A more complete coverage of available peripheral and instrumentation equipment for the systems is shown in AUERBACH reports 180.3964.050 and 180.3964.053, which cover the Hewlett-Packard HP 21MX. Tables 1 and 2 provide supplemental data on the software sizes and system linkage charac-

teristics of the various operating systems available for the distributed network.

## COMPATIBILITY

All the systems within an HP distributed network system are, by definition, compatible. Software is upward compatible from satellite to central. Across satellites, however, programs developed under the BASIC interpreter of RTE-B must be reprogrammed to run under the differing software environments of other satellites.

## MAINTENANCE AND SUPPORT

Hewlett-Packard is noted within the industry for its product support. The company maintains 172 field offices in 65 countries throughout the world, including 60 service facilities in the U.S. and Canada, backed by five regional offices. Two service and warranty plans are available under terms of the purchase agreement. One provides for "parts only" warranty for 15 months; a second provides for full services, parts and labor, for 90 days. Add-on agreements can provide for either guaranteed response times and full service or on a per-call time and materials basis.

## TYPICAL PRICES

Model No.	Description	Purchase Price \$	Monthly Maint. \$
<b>BASIC SYSTEMS</b>			
9602A	High-Accuracy Scientific Measurement and Control System (200 channel)	48,900	184
9603A	High-Speed Scientific Measurement and Control System	22,900	157
9611A	High-Speed Analog/Digital Industrial Measurement and Control System	29,900	176
9640A	Real-Time Multiprogramming and Computational System	15,800	35
9700A	Distributed Systems Central	34,800	298
9603R	Remote Scientific Measurement and Control Station	9,950	32
9611R	Remote Industrial Measurement and Control Station	8,890	29
<b>OPTIONS</b>			
2313B-001	Analog I/O Subsystem	4,720	16
2912A	Reed Scanner	6,300	21
12760A	Relay Low-Level Multiplexor	1,650	3
12761A	Solid-State Low-Level Multiplexor	1,150	3
91110A	High-Level Multiplexor	925	4
91063A	Digital I/O Subsystem	3,450	
91065A	550 MHz Time Counter Subsystem	7,500	23
91226A	Remote Analog Communications Subsystem	950	8
91226A-001	Remote Digital Communications Subsystem	950	8
2615A	CRT Terminal and Interface; 25 lines, 80 char/line	3,185	36
2762A	Teleprinter; 30 char/sec, 75 col	2,350	58
2762B	Teleprinter; 120 char/sec, 75 col	5,555	36
12977A	Fast FORTRAN Processor	1,350	16
12990A	Memory Extender	3,500	16
2102A	8K Memory Module	1,500	4
12926A	Tape Punch Subsystem	3,090	51
12985A	Card Reader Subsystem; 600 cpm, 80 col, auto feed, 1000 card hopper/stacker	5,665	54
12986A	Optical Mark Reader Subsystem	3,995	33
12983A	High-Speed Line Printer Subsystem; 132 col, 1250 lpm, 64 or 96-char ASCII	32,950	153
12984A	Line Printer Subsystem; 80 col at 356 lpm or 20 col at 1110 lpm	13,900	82
12987A	Line Printer Subsystem; 132 col, 200 lpm, 64 char set (128 char set optional)	7,950	75

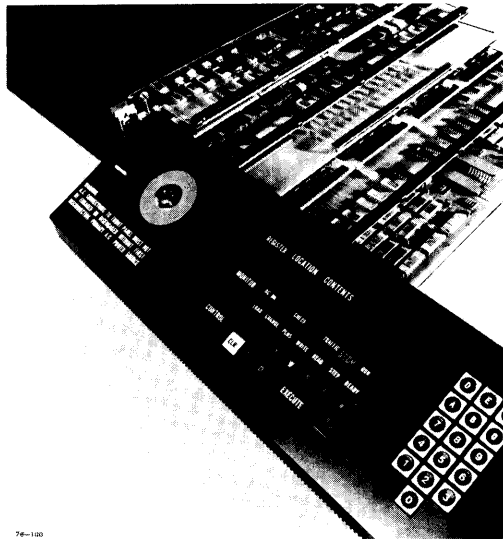
**TYPICAL PRICES (Contd.)**

Model No.	Description	Purchase Price \$	Monthly Maint. \$
12935A	Graphic Plotter Subsystem	4,365	33
12970A	Digital Magnetic Tape Subsystem (NRZ1); 9-track, 800 char/in, tape speed up to 45 ips R/W, transfer speed up to 36K cps	8,900	72
12970A-010	9-track Digital Magnetic Tape Drive (max of three/subsystem)	6,850	61
12971A	Digital Magnetic Tape Subsystem (NRZ1); 7-track	12,400	105
12971A-010	7-track Digital Magnetic Tape Drive	6,900	61
12972A	Digital Magnetic Tape Subsystem (phase-encoded); 9-track, 1,600 cpi, tape speed up to 45 ips R/W, transfer speed up to 72K char/sec, 160 ips rewind speed	10,900	90
12972A-010	9-track Digital Magnetic Tape Drive (phase encoded), max three/subsystem	6,845	90
12960A	Cartridge Disc Drive; 4.9 Mb, expandable to 19.6 Mb, avg access 35-msec; max three/subsystem	9,975	89
91700A	Central Distributed Systems Kit with hardwire or modem interface card, 12-ft cable, and Central Communication Executive (CCE)	3,250	8
91703A	BCS-based Satellite Distributed Systems Kit with two hardwire or modem interface cards and Satellite Communication Executives 1 and 3 (SCE 1 and 3)	3,750	16
91704	RTE-B-based Satellite Distributed Systems Kit with two hardwire or modem interface cards and SCE 1 and 4	3,750	16
91705A	RTE-C-based Satellite Distributed Systems Kit with two hardwire or modem interface cards and SCE 1 and 5	3,750	16
91780	Remote Data Transmission Subsystem	4,250	13
24376B	IMAGE/2000 Data Base Management (software) System	3,000	40
24342B	Terminal Control (software) System	1,600	35
AO1	Real-Time BASIC Operating System (memory based)	1,850	35
A02	Real-Time Executive Operating System (memory based)	1,850	35
A03/05	Real-Time Executive II Operating System hardware-software package (disc based)	14,000	153



# HONEYWELL INFORMATION SYSTEMS

## Level 6 System Report



### OVERVIEW

The Honeywell Level 6 currently consists of three models: the 6/06, 6/34, and 6/36. All models are based on the same 16-bit microprogrammed processor and are specifically aimed at the OEM market. The 6/34 and 6/36 implement a new instruction set unrelated to Honeywell's previous computer offerings. These two systems, which are really the same system packaged differently, represent Honeywell's attempt to re-enter the minicomputer market with a fresh system and a more vigorous approach. Model 6/06, on the other hand, includes hardware to emulate Honeywell's System 700 and a bus adapter to convert the system bus to the System 700 I/O interface so the 6/06 can use all System 700 software and peripherals. The 6/06, consequently, has only the CPU in common with the 6/34 and 6/36. Table 1 summarizes the mainframe characteristics of the 6/06 and the 6/30 models.

The Level 6 processor utilizes a central bus architecture implemented in T<sup>2</sup>L bipolar logic. The central processor, memory modules, and peripheral device controllers all communicate with each other in a master-slave relationship over the system bus, the "Megabus." Cycle time of the Megabus is 300 nanoseconds for each word transferred. On 6/06 systems, a System 700-type I/O bus is attached to the Megabus like a peripheral device. In this way, System 700 DMA peripherals can in turn be attached to the I/O bus.

The 6/34 and 6/36 central processor implements a standard set of 107 instructions. Although fixed-point arithmetic uses single precision (one-word) operands, bit, byte,

and double-word instructions are also available. A bit can be set, reset, or swapped; bytes can be loaded and stored and logical operations can be performed on them; and double words can be loaded into registers or stored in memory. Multiply and divide are included in the instruction set. Hardware floating-point arithmetic is not available.

The CPU uses 18 internal addressable registers that are used to implement eight modes of addressing, multiple accumulators, and indexing. The processor also implements 64 interrupt levels.

Memory for all systems can be 8K word, 650-nanosecond MOS modules with parity; or optionally, with error detection and correction bits. Maximum memory size is 64K words for the 6/06, 32K words for the 6/34, and 64K words for the 6/36. The Megabus, however, can carry 24 address bits; thus future Level 6 models may address over 8M words (16M bytes) of memory.

The 6/34 and 6/36 peripherals include discs, magnetic tape, punched card, I/O printers, terminals and communications lines; the 6/06 peripherals are more extensive, however, because the DMA peripheral complement of the System 700 can be attached to the 6/06.

The 6/06 is the most recent development in the 700 line, which has undergone a number of evolutionary changes and reorganizations. Most of these changes have occurred in an improved price structure marketing (model numbering, definition of "BASIC" systems) and developments in engineering (8K-word memory boards).

The 716 processor that served as the foundation for the 700 Series is architecturally similar to the earlier 316 and 516 models. The 716 instruction set includes the 316 and 516 instructions as subsets. All 16 Series peripherals can attach to a 716 with the aid of the DMC adapter option. Within the same environments, program compatibility is completely maintained. In addition, all 316 and 516 programs can run on the 716. The OP-16 and BOS operating systems developed for the 316 are also available in 716 versions for users who want to run 316 programs on a 716.

### HEADQUARTERS

Honeywell Information Systems  
Computer Controls Division  
Old Connecticut Path  
Framingham MA 01701

# HONEYWELL INFORMATION SYSTEMS — LEVEL 6 SYSTEM REPORT

**Table 1. Honeywell Level 6: Mainframe Characteristics**

Characteristic	Level 6/06	Level 6/30
<b>Central Processor</b>		
Microprogrammed	Yes	Yes
No of Registers	7	18
Addressing Wd Length	16 bits <sup>(1)</sup>	16 bits <sup>(1)</sup>
Direct	1K wds <sup>(2)</sup>	64K wds
Indirect	Multilevel <sup>(2)</sup>	Single level
Indexed	Yes, pre- and post <sup>(2)</sup>	Yes
Mapping	No	No
<b>Instruction Set Implementation Types</b>	Firmware Single-wd/ double-wd	Firmware Single-wd/ double-wd
<b>Fixed-Point</b>		
Add/Subtract	4.1	4.1
Multiply	11.2	11.2
Divide	13.2-14.5	13.2-14.5
Floating-Point	NA	NA
Writable Control Store	NA	NA
Interrupt Levels	63	64
Stack Operations	Limited	Yes
<b>Main Memory</b>		
Type	nMOS RAM	nMOS RAM
Word Length	16+2 parity/ 16+6 EDAC	16+2 parity/ 16+6 EDAC
Cycle Time (nsec)	650	650
Basic Addressable Unit	Wd	Wd or byte
Bytes/access	2	2
Cache Memory	No	No
Capacity (bytes)		
Min	16K	16K
Max	128K	128K
Increment Size (bytes)	16K	16K
Ports/Module	1	1
Error Checks	Parity, std; EDAC, opt	Parity, std; EDAC, opt
Memory Protection	Memory lockout opt	NA
Memory Save	Opt	Opt
Memory Management	No	No
Interleaving	No	No
Input/Output	6/06	6/30
Maximum Addressable Devices	64	1,024
Programmed I/O	Software-dependent	Control wds only
Megabus Transfer Rate (bytes/sec)	6M	6M
Max DMA Transfer Rate (bytes/sec)	1M <sup>(3)</sup>	0.8M-1M
Multiplexed I/O	Sys 700 DMA <sup>(3)</sup>	Via device controllers

**Notes:**

- (1) By instruction. Megabus has 24 address bits; thus, it can address 16M words of memory.
- (2) The Level 6/06 has all the System 700 addressing modes which are upward compatible with the older Series 16 addressing.
- (3) The Level 6/06 is designed as an end-user version of the System 700; thus, it supports only the System 700 peripheral devices.

The 716 processor had stack-register and register-addressing features unavailable on the Series 16 processors. These features included standard DMA channel, a com-

plete line of data communications hardware, a new real-time operating system (OS/700), and host-resident software. In addition, the 716 is 20 percent faster than the DDP-516 and more than twice as fast as the H316.

The 6/06 system follows the development of the 700 line, representing an increase in speed and a decrease in cost over System 700 while maintaining compatibility.

Operating system support for the 6/06 is provided by the System 700 OS/700, a modular real-time, multiprogramming system that provides computer-to-computer communication, priority-oriented task scheduling, and centralized control of all system resources. OS/700 is available in both core-based (COS) and disc-based (DOS) versions. The FORTRAN IV compiler, BASIC interpreter, and Assembler can run under OS/700 or can operate in a free-standing environment. Host-resident software systems allow program development on other Honeywell or IBM computers. In addition, OS/700 can support extensive communications facilities and a file management package. The RJE (HASP II) and RCP 707 system software packages are also available, so a user can implement a network system from a 725 or 735, given the proper configuration.

Two software packages are available for the 6/34 and 6/36: GCOS/BES 1 and GCOS/BES 2. Both provide executive modules for control of on-line, interrupt-driven system operation with task scheduling, input/output control featuring device-independence, timing of tasks and trap handling. The executive modules require no peripherals other than an input unit such as diskette, cartridge disc or paper tape from which modules are loaded. Both GCOS/BES 1 and BES 2 provide program development modules that support an assembler, FORTRAN compiler, editor, command processor, linker and utilities.

The GCOS/BES 2 package is a superset of BES 1. It includes a communications module that supports the Multiline Communications Processor for synchronous line control including IBM BSC/2780 communications support and asynchronous line control. The module is designed to allow users to insert communications software for user-developed terminals and protocol handlers.

The GCOS/BES 2 program development module includes a macro preprocessor to generate macros for use in an assembly-language source program. Thirty-five parameters can be specified in a macro call to allow the user to tailor the macro to a specific application.

## PERFORMANCE AND COMPETITIVE POSITION

In 1970, Honeywell was third largest minicomputer manufacturer: only Digital Equipment Corporation and Hewlett-Packard had installed more minicomputer systems. At that time, however, only 22,000 minicomputers were in use, about 2,000 of which were Honeywell systems. In 1972, when Honeywell introduced the System 700, based on a new 716 CPU, the company announced the





integration of its minicomputer line into its data processing division. Honeywell would sell minicomputers as part of its medium- or large-scale computer installations.

Although logical on the surface, the nature of the minicomputer market, which has been separate from the commercial data processing market was not taken into consideration. Minicomputers are just now beginning to compete with general-purpose systems. In the period since 1972, Honeywell has had little part in the steady growth in the minicomputer field, even though a company spokesman claimed that minicomputer sales were as high as \$80 million in 1975. When Honeywell, in effect, withdrew from the minicomputer market in 1972, Prime Computers built and marketed its Prime Series, which are peripheral- and software-compatible with Honeywell's Series 16.

The Level 6/30 Models were designed as Honeywell's reentry into the minicomputer market. They use a totally new architecture for Honeywell, which is based on the central Megabus, similar to the Unibus of Digital Equipment's PDP-11. The traditional way for companies to enter the minicomputer market is via OEM and Honeywell now stands in the same position as any other newcomer to this market. The end-user market requires a customer base; the fastest way to acquire that base is via OEMs who will sell systems incorporated in a product.

The OEM market is very competitive: Data General, Digital Equipment, General Automation, Digital Computer Controls, Computer Automation, and other manufacturers are all quite well established here.

Table 2 shows that the Level 6/30 is performance competitive with the Nova 3, PDP-11/34, and GA-16/330. It is

very well priced in comparison to the PDP-11/34, but is more expensive than both the Nova 3 and GA-16/330 for small configurations. It is, however, less expensive than the Nova 3 for larger systems. All three systems offer much more software than is available with the Level 6.

Honeywell has been building a special staff to sell the Level 6 minicomputers, consisting mainly of experienced minicomputer salesmen. It will be a difficult task to reenter the OEM minicomputer market with a system that is not substantially better and lower in cost than its major competitors. Honeywell will probably have to lower the price, increase the performance and add more software before the Level 6 is serious competition.

Honeywell is a large company with many resources. Certainly the company's process control devices that can interface to computers are a major advantage. But the major minicomputer manufacturers are also substantial companies with large resources and fine reputations. Companies such as Data General, Digital Equipment, and Hewlett-Packard make few wrong moves. Honeywell faces tough competition, and it will require a considerable investment combined with good product planning and marketing to make an impact on the minicomputer marketplace.

### Configuration Guide

All three Level 6 systems differ in the amount of memory, peripherals and options that can be attached; in addition, 6/06 firmware/hardware makes it compatible with System 700 peripherals, so that that model has a different peripheral complement.

**Table 2. Honeywell Level 6/30: Comparison with OEM Competitors**

	Honeywell 6/30	Data General Nova 3	Digital Equipment PDP-11/34	General Automation GA-16/330
Word Length (bits)	16 + 2 Parity/16 + 6 EDAC	16/16 + 2 Parity	16/16 + 2 Parity	16/16 + 2 Parity
Instr. Times (μsec)				
Add	4.1	1.8	2.7	4.6
Multiply	11.2	6.9(1)	9.7	21.2
Divide	13.2-14.5	7.5(1)	11.3	20.3
Floating-Point Add	Subroutine	7.7*	—(2)	*
Floating-Point Multiply	Subroutine	11.3*	—	*
Floating-Point Divide	Subroutine	13.7*	—	*
Max Memory (bytes)	64K/128K	64K/256K	124K	128K
No. of GP Registers	7118	4	9	16
Max DMA Rate (bytes/sec)	6M	2M	2M	2M
			<b>PRICE</b>	
			\$	
CPU + Memory				
32K bytes	5,570	4,400	9,290	5,250
64K bytes	8,790	7,100	11,790	8,250
128K bytes	17,000	22,700	19,190	NA
256K bytes	NA	37,500	31,590	—

\*Optional at extra cost

**Notes:**

- (1) Operands are unsigned integers on std.
- (2) Floating point not yet officially announced.
- (3) Maximum memory can be only 248K bytes although price is for 256K bytes.



The basic 6/06 system includes the one-board processor in a four-slot Megabus chassis, one memory controller with parity, an 8K word MOS memory PAC, multiply/divide, a Level 6 System 700 Bus Interface, a System 700 Expansion drawer with peripheral slots, a Memory Save unit with batteries for 64K words, and power supply. Basic systems must include an ASR or KSR Teletype console. Memory controllers occupy one Megabus slot and can support three more memory PACs on the same board. Options include real-time clock and watchdog timer, the peripheral controllers, CRC algorithm unit, extended memory and memory lockout option, and error-correction memory.

The Model 6/34 includes the processor in a four-slot Megabus chassis, memory controller with parity, an 8K word MOS Memory PAC, multiply/divide, real-time clock, and ROM bootstrap loader. The processor requires one Megabus slot. The memory controller, which also requires one Megabus slot can support three additional Memory-Pacs. Two slots are left in the four-slot chassis to attach peripheral devices and communications lines. Options include the controllers, Level 6 peripherals, full control panel, Memory Save and Auto Restart, watchdog timer, peripheral power supply, cabinet, and accessories.

The Model 6/36 includes the processor in a five- or ten-slot Megabus chassis that can be expanded to 23 slots, a full control panel, multiply/divide hardware, real-time clock, ROM bootstrap, and power supply. Options include the peripheral controllers, Level 6 peripherals, memory controllers and memory Pacs with parity or EDAC for up to 64K words, Memory Save and Auto Restart, watchdog timer, and basic control panel (for five-slot chassis only).

Memory for Level 6 interfaces to the Megabus via memory controllers. Each controller can support up to four 8K-word memory modules and each requires one Megabus slot. Memory is designed using n-channel MOS 4K-bit dynamic RAMs. Cycle time is 650 nanoseconds per word. Byte parity memory with 16 data bits and two parity bits is standard; memory with Error Detection And Correction (EDAC), 16 data bits and six detection bits, is optional. The Memory Save and Auto Restart option can retain memory contents for 2 hours when main power is down.

Maximum memory capacity is currently 32K words for Model 6/34 and 65K words for Model 6/36.

All 6/34 and 6/36 peripheral devices connect to a Megabus slot via controllers; all controllers except the DMA interface since user-designed devices include a microprocessor and memory. Four types of I/O interfaces are available:

- Multiple Device Controller supports four slow-speed devices (card reader, line printer, serial printer, Teletypewriter, diskette, and TTY-compatible display).
- Mass Storage Controller supports up to four cartridge disc units (2.5- to 40-million bytes capacity); maximum throughput is 312K bytes per second.
- Multiline Communications Controller interfaces with multiple asynchronous or synchronous lines — eight

full duplex low-speed lines (300 bps or less) or medium-speed lines (600 to 10,800 bps), or four broadband lines (up to 72,000 bps) — with an aggregate combined throughput up to 160,000 bps.

- General-Purpose DMA Interface supports one user-designed device; maximum transfer rate between memory and device is 500,000 words per second.

Peripheral devices interface to the standard controllers via Device-PACs, each one designed for a specific device. Each controller requires only one slot on the Megabus, and provides DMA block transfer facilities for the interfaced devices. Tables 3 and 4 summarize the peripherals that can be attached to the 6/30 and 6/06 respectively. The 6/06 peripherals connect to a System 700-type I/O bus which is, in turn, connected to a Megabus. The Megabus has up to 23 slots to connect memory, DMA, multi-device, or multiline communications controllers.

**Table 3: Honeywell Level 6/34 and 6/36: Peripherals**

Model Number	Description
<b>Discs</b>	
DIU 9101	Diskette; single drive, 1-4 drives/controller, 256K bytes/diskette
DIU 9102	Diskette; dual drive version of DIU 9101
CDU 9101	Cartridge disc; 1 removable, 2.5-2.8M wds/pack
CDU 9102	Cartridge disc; 1 fixed, 1 removable, 5.0-5.6M wds/pack, 20.0-22.5 mbytes/subsystem
CDU 9103	Cartridge disc; 1 removable, 5.0-5.6M wds/pack, 20.0-32.5 mbytes/subsystem
CDU 9104	Cartridge disc; 1 removable, 1 fixed; 2.5M wds/pack 10.0-11.2M drive, 40.0-45.0 mbytes/subsystem
<b>Cards</b>	
CRU 9101	Card Reader, 300 cpm
CRU 9102	Card Reader, Mark Sense and Punched Cards, 300 cpm
CRU 9103	Card Reader, 500 cpm
CRU 9104	Card Reader, Mark Sense and Punched Cards, 500 cpm
<b>Terminals</b>	
DKU 9101	CRT/Keyboard Console
DKU 9102	CRT/Keyboard Console
TTU 9101	ASR-33 Teletype, 10 cps
TTU 9102	KSR-33 Teletype, 10 cps
<b>Communications</b>	
Synchronous	1 or 2 full duplex lines-10,800 baud
Asynchronous	1 or 2 full duplex lines-9,600 baud
Broadband	1 full duplex line-72,000 baud

Software packages for the 6/06 differ from those for the 6/34 and 6/36, as noted in Table 5.

## COMPATIBILITY

The Model 6/06 system uses the same instruction set and peripheral interfacing as the System 700. Therefore, it is completely hardware- and software-compatible with that system. The 6/34 and 6/36 models are compatible with each other in every respect since they are essentially different packaging of the same system. Model 6/06 is not compatible with either the 6/34 or 6/36.

**Table 4. Honeywell Level 6/06 (System 700):  
Peripherals**

**Fixed-Head Disc**—64K, 128K, 256K, and 512K wds on 16, 32, 64, and 128 trks, respectively; avg access time, 12.5 msec; transfer rate, 82K wds/sec  
**Removable-Head Disc**—6 drives with capacities of 0.9M to 7.2M wds; 7.5M wds; 1.1M wds; 1.8M wds; 3.7M wds; and 7.5M wds  
**Magnetic Tape**—tape cassette system; 6 subsystems including 7-trk and 9-trk units, with 200-, 556-, 800-, and 1,600-bpi densities  
**Printers**—9 printers at 200, 300, 450, 650, 950, and 1,100 lpm; 96, 120, and 136 cols; 64 and 96 char sets  
**Punched Card**—readers at 300, 600, 800, and 1,050 cpm; punches at 400–1,000 cpm; reader/punches at 400 cpm read, 100–400 cpm punch  
**Paper Tape**—reader at 300 cps max transfer rate, 8-level tape; punch at 110 cps max transfer rate, 8-level tape  
**Teletype**—ASR 33, KSR 33, ASR 35; ASR includes paper tape reader/punch

## MAINTENANCE AND SUPPORT

Honeywell provides world-wide marketing support, including several hundred local offices for its Field Engineering Division. An emergency network provides service 24 hours a day, seven days a week.

For the System 700 and Level 6 systems, Honeywell has trained its commercial data processing field support staff to furnish the applications-oriented service required by

minicomputer users. The total solution approach and the level of support should appeal to a wide range of customers.

**Table 5. Honeywell Level 6 and System 700:  
Software Configuration**

Package	Configuration Required
<b>OS/700</b>	
DOS (disc-based)	6/06 processor, 16K wd main memory, 1 disc with 128K wds min, 1 programmed I/O device
COS (core-based)	6/06 processor, 24K wd main memory, 1 programmed I/O device
<b>BOS (Batch Operating System)</b>	6/06 processor; 12K wd core memory, 0.9M wd disc storage, ASR 33 Teletype
<b>OP-16 Real-Time Operating System</b>	6/06 processor, 4K wd main memory, real-time clock, ASR 33 or 35 Teletype
<b>GCOS/BES 1 Executive</b>	6/34 processor compact run-time/software development executive, 1 interactive user, requires 6/34 processor 8K wd memory, TTY Like GCOS/BES 1 but extended for communications, multi-tasking; requires 6/36 processor 8K memory, disc, console
<b>GCOS/BES 2 Executive</b>	Dartmouth Superset, runs under GCOS/BES 1/2
<b>Basic</b>	Several versions, expansion of ANSI standard, runs under GCOS/BES 1/2
<b>FORTTRAN IV</b>	

## PRICE DATA

Model Number	Description	Purchase \$	Monthly Maint. \$	6/06 6/34 6/36		
				6/06	6/34	6/36
<b>CENTRAL PROCESSOR SYSTEMS (CPS)</b>						
Each 6/30 is rack mountable or freestanding and includes:						
<ul style="list-style-type: none"> <li>• Megabus Chassis with Power Supply</li> <li>• Multiply/Divide Hardware</li> <li>• Real Timer Clock</li> <li>• ROM Bootstrap Loader for keyboard console, diskette, &amp; card reader</li> </ul>						
CPS9450	6/34 Processor in 4-Slot Megabus Chassis including basic control panel, memory controller with parity, and an 8K-wd Memory-Pac. Can add up to 3 more 8K-wd Memory-Pacs (CMM9001) for 32K-wd max	3,990	60		x	
CPS9460	6/36 Processor in 5-Slot Megabus Chassis including full control panel. Memory controller and 8K-wd Memory-Pacs must be ordered separately, up to 64K-wd max	3,200	40			x
CPS9461	Same as CPS9460 except in 10-Slot Megabus Chassis	4,100	42			x
<b>GENERAL OPTIONS</b>						
CPF9401	Watchdog Timer	400	3			x
CAB9401	4-Slot Megabus Expansion Chassis with Power Supply	1,900	8		x	x
CAB9402	9-Slot Megabus Expansion Chassis with Power Supply	3,000	10			x
GIS9001	General-Purpose Interface	900	4		x	x
<b>MOS RAM Memory</b>						
CMC9001	Memory Controller with Parity including 8K-wd Memory-Pac (CMM9001); can add up to 3 more 8K-wd Memory-Pacs	2,400	24	x		x

# HONEYWELL INFORMATION SYSTEMS — LEVEL 6 SYSTEM REPORT

## PRICE DATA (Contd.)

CMM9001	8K-wd Memory-Pac with Parity	1,600	10	x	x	x
CMC9002	Same as CMC9001 except with EDAC instead of parity	2,800	28	x		x
CMM9002	8K-wd Memory-Pac with EDAC	1,800	12	x		x
PSS9001	Memory Save for up to 64K wds with Auto Restart (tabletop model)	700	6		x	x
<b>PERIPHERALS</b>						
MDC9101	Multiple Device Controller	1,200	10		x	x
KCM9101	Device-Pac for Keyboard Console	200	5			
DIM9101	Device-Pac for Diskette	500	5			
CRM9101	Device-Pac for Card Reader	400	7			
PRM9101	Device-Pac for Printer	400	6			
TTU9101	ASR-33 Teletypewriter Console	1,600	48			
DKU9101	CRT/Keyboard Console, 64-char set	1,400	21			
TWU9101	30 CPS Keyboard Typewriter Console (KSR)	2,300	26			
DIU9101	Single Diskette, rack mountable	1,700	17			
DIU9102	Dual Diskette, rack mountable	2,800	28			
CRU9101	300 CPM Punched Card Reader	3,500	41			
CRF9101	51-Col Card Option	600	7			
PRU9101	60 LPM Serial Printer, 64-char set	5,100	40			
PRU9104	300-LPM Printer, 64-char set	8,700	60			
PRU9106	600-LPM Printer, 64-char set	16,000	140			
<b>MASS STORAGE DEVICES</b>						
MSC9101	Mass Storage Controller	2,800	16	x	x	
CDM9101	Device-Pac for Cartridge Disc	1,200	12			
CDU9101	Cartridge Disc Drive, Low Density, for 1 removable disc (1.25M wds)	5,700	50			
CDU9102	Cartridge Disc Drive, Low Density, for 1 removable and 1 fixed disc (2.5M wds)	7,800	60			
CDU9103	Cartridge Disc Drive, High Density, for 1 removable disc (2.5M wds)	7,400	60			
CDU9104	Cartridge Disc Drive, High Density, for 1 removable and 1 fixed disc (5M wds)	8,500	80			
<b>COMMUNICATIONS</b>						
MLC9101	Multiline Communications Processor with Communication-Pacs for 8 async lines up to 9.6KB each, with cables Each 6/06 CPS includes: • 6/06 Processor with high-speed arithmetic/base sector relocation and real-time clock • Megabus Chassis with Power Supply • S700 Bus Interface	3,400	26	x		x
CPS9220	6/06 CPS in 5-Slot Megabus Chassis mounted in 60-in cabinet with all panels and doors (includes Memory Save for up to 64K wds, with Auto Restart, power distribution unit, and any required S700 expansion drawers and add-on cabinets); memory controller and 8K-wd Memory-Pacs must be ordered separately	5,500	60	x		
CAB9010	Extension Table Wing	250	NC			
GIS9002	Additional S700 Bus Interface	850	13	x		

### OVERVIEW

System 700 is a line of general-purpose minicomputers, which are marketed primarily as components of a large data processing network. The 700 offers good I/O and interrupt facilities, a broad range of peripherals, and well-integrated software. Both hardware and software place emphasis on the real-time processing required for process control, data collection, and data communications environments.

The three models currently being offered for the 700 Series are all based on the 716 processor first announced in 1972. The 716 uses a 16-bit word, and memory cycle time is 775 nanoseconds per word. The models have letter suffixes indicating function: G for "general-purpose," S for "sensor-based," and "M" for rack-mounted version targeted at system builders who want to use their own cabinets. The 725-G/735-G General-Purpose System, the 725-S/735-S Sensor-Based System, and the 725-M Rack-Mounted System comprise the newest system offerings.

Standard features for the G and S systems are high-speed arithmetic, real-time clock, and 8K-word memory boards that allow memory to be extended to 64K words within the main processor chassis. Table 1 lists mainframe characteristics.

Peripherals available for the 700 Series include a wide variety of low-speed, mass storage, and special subsystems. Table 2 lists peripherals.

One strong point of the 700 Series is its data communications capability. There are several special-purpose "Datanet" 700 communications systems based on the 716 processor. These Datanet systems are designed to provide minicomputer-controlled remote batch processors, concentrators, and distributed processors that can be configured into a large network controlled by Honeywell or IBM computers. The equivalent of Datanet systems can be configured with 725-G/735-G systems, using RJE (HASP II) or the RCP 707 systems software packages.

Operating system support is provided by OS/700, a modular real-time, multiprogramming system that provides computer-to-computer communication, priority-oriented task scheduling, and centralized control of all system resources. OS/700 is available in both core-based (COS) and disc-based (DOS) versions. The FORTRAN IV compiler, BASIC interpreter, and Assembler can run under OS/700 or can operate in a free-standing environment. Host-resident software systems allow program development on other Honeywell or IBM computers. In addition, OS/700 can support extensive communications facilities and a file management package. Since the RJE (HASP II) and RCP 707 system software packages are also available, a user could implement a Datanet system from a 725 or 735, given the proper configuration. Table 3 lists software configuration requirements.

**Table 1. Honeywell System 700: Mainframe Characteristics**

<b>Central Processor</b>	
Type (microprogrammed)	No
Control Memory (RAM, ROM)	—
Size	—
Use	—
No. of Internal Registers	2 general-purpose, 1 index register; alternate index register
<b>Addressing</b>	
Direct (no. of words)	1,024 <sup>(1)</sup>
Indirect	Multilevel
Indexed	Yes
<b>Instruction Set</b>	
Implementation (hardware, firmware)	Hardware
Number (std, opt)	78 std, 4 opt
Decimal Arithmetic	No
Floating-Point Arithmetic	By subroutine
User Microprogramming	—
Priority Interrupt System	3-48
Operation Modes	Levels
<b>Main Storage</b>	
Type	Core
Cycle Time (μsec)	0.775
Basic Addressable Unit	16-bit word
Bytes per Access	2
Cache Memory	No
Min Capacity (bytes)	16K <sup>(2)</sup>
Max Capacity (bytes)	128K
Increment Size (bytes)	16K
Ports per Module	1
Error Checks	Parity (opt)
Protection Method	Memory lockout (opt)
Memory Management	—
ROM	—
Use	Loaders
Capacity (bytes)	256-2,048 words
<b>I/O Channels</b>	
Programmed I/O	Yes
DMA Channels	Yes (no limit)
Multiplexed I/O (no. of subchannels)	DMC optional (8)
<b>Max Transfer Rate</b>	
Within Memory (wds/sec)	321,500
Over DMA (wds/sec)	1,290,000
<b>Simultaneous Operations</b>	None, except multiple peripherals with processing

**Notes:**

- (1) Base sector and current sector; base sector is optionally relocatable.
- (2) OS/700 requires 32K bytes of memory for a program development system. Execute-only systems can be configured with as little as 16K bytes of memory.

### Relationship to Other Honeywell Products

The 700 line has undergone a number of evolutionary changes and reorganizations; most of these represent changes in pricing (getting more for less) and marketing (model numbering, definition of "BASIC" systems) coupled with some engineering developments (8K-word memory boards). The current 725-6/735-G General-Purpose System, for instance, directly replaces the 720/01 Terminal System and the 720/02 Peripheral System as well as retiring the 720/03 Multipurpose System and the

**Table 2. Honeywell System 700: Peripherals**

**Fixed-Head Disc**—64K, 128K, 256K, and 512K wds on 16, 32, 64, and 128 trks, respectively; avg access time, 12.5 msec; transfer rate, 82K wds/sec.  
**Removable-Head Disc**—6 drives with capacities of 0.9M to 7.2M wds; 7.5M wds; 1.1M wds; 1.8M wds; 3.7M wds; and 7.5M wds.  
**Magnetic Tape**—tape cassette system; 6 subsystems including 7-trk and 9-trk units, with 200-, 556-, 800-, and 1,600-bpi densities.  
**Printers**—9 printers at 200, 300, 450, 650, 950, and 1,100 lpm; 96, 120, and 136 cols; 64 and 96 char sets.  
**Punched Card**—readers at 300, 600, 800, and 1,050 cpm; punches at 400-1,000 cpm; reader/punches at 400 cpm read, 100-400 cpm punch.  
**Paper Tape**—reader at 300-cps max transfer rate, 8-level tape; punch at 110-cps max transfer rate, 8-level tape.  
**Teletype**—ASR 33, KSR 33, ASR 35; ASR includes paper tape reader/punch.

**Table 3. Honeywell System 700: Software Configuration Requirements**

Operating System	Configuration Required
OS/700	
DOS (disc-based)	716 processor, 16K-wd main memory, 1 disc with 128K wds/min, 1 programmed I/O device
COS (core-based)	716 processor, 24K-wd main memory, 1 programmed I/O device
BOS (Batch Operating System)	716 or 316 processor; 12K-wd core memory, 0.9M-wd disc storage, ASR 33 Teletype
OP-16 Real-Time Operating System	716 or 316 processor, 4K-wd main memory, real-time clock, ASR 33 or 35 Teletype

720/05 Batch Processing System, both of which were based on the H316 processor. The current 725-S/735-S directly replaces the 720/20 Sensor-Based System and the 720/21 Extended Sensor-Based System. Both the new G and S systems include as standard features several 720/xx options such as high-speed arithmetic and real-time clock; also both use only 8K-word memory boards, allowing 64K words of memory to be stored within the main processor chassis.

The 716 processor that serves as the foundation for the 700 Series is architecturally similar to the earlier 316 and 516 models. The 716 instruction set includes the 316 and 516 instructions as subsets. Since all 16 Series peripherals can attach to a 716 with the aid of the DMC adapter option, program compatibility is completely maintained given the same environments. In addition, all 316 and 516 programs can run on the 716. The OP-16 and BOS operating systems developed for the 316 are also available in 716 versions for users who want to run 316 programs on a 716.

The 716 processor has stack-register and register-addressing features unavailable on the Series 16 processors. These features include standard DMA channel, a complete line of data communications hardware, a new real-time operating system (OS/700), and host-resident software. In addition, the 716 is 20 percent faster than the DDP-516 and over twice as fast as the H316.

System 700 models can duplicate all of the major Series 16 systems except the 1640 Timesharing Systems. Honeywell currently has no plans to upgrade the time-sharing systems to use the 716 processor.

## COMPETITIVE POSITION

Honeywell is not marketing the 716 processor chiefly as a minicomputer or as an upgrade to the Series 16 processors. The system is marketed by the commercial data processing sales force, which is concerned with the total computer network, so System 700 configurations are sold as component parts of that network.

The Series 16, forerunners of the 700 Series, were strong competitors in the minicomputer field. Unlike Digital with its PDP-11 line, Honeywell did not change the architecture of the 716 processor from that of the older Series 16 line. This evolutionary path to computer development protects the Series 16 users' software and peripherals, and provides the 716 system for upgrading.

The System 700 models span the breadth of the major part of the minicomputer market, including most of the OEM segment. System 700 is offered unbundled for the OEM market; contracts for the system are negotiated with the home office. There is no equivalent to the smaller, slower board-level "microcomputers" that manufacturers like General Automation and Digital are adding at the bottom end of their lines, mostly for OEM applications. Moreover, Honeywell has not added a memory mapping option to extend the line into the larger 128K- and 256K-word systems available from manufacturers like Hewlett-Packard and again Digital and General Automation, plus Interdata and Modular Computers.

The sensor-based systems compete directly with the IBM System/7, 1130 and 1800, CDC 1700, Xerox Sigma 3, and Digital PDP-11 for data acquisition, manufacturing, and process control applications. General-purpose models compete both as business minis and as terminal control systems. As such, they are directly competitive with such intelligent terminal systems as MODCOMP I and III; Four-Phase System IV/70; and, in some cases, IBM System/3. These systems are designed for data collection and limited processing from terminals in banks, factories, and laboratories.

Honeywell's advantage in this market is that customers can obtain a total distributed processing network from a single supplier. Univac offers this capability, but IBM has refrained from embracing this type of distributed systems concept, stressing instead large centralized systems. As a result, independents have developed the distributed processing idea — and Honeywell's 716-based HASP II RTE package directly competes in the general intelligent terminal market geared toward IBM computers.

The System 700's most direct competitor is PRIME Computer's PRIME 100, 200, and 300, which are program and peripheral compatible with the Honeywell Series 16

line. The PRIME computers utilize MSI and LSI technology plus all MOS memories. They offer many enhancements over the Series 16, including a substantial upgrade capability to the mid-range PRIME 300. Honeywell's shift of emphasis away from the minicomputer market to the network market has the advantage of consolidating its computer lines, but it has also left a vacuum in the minicomputer market that PRIME has moved to fill.

## Configuration Guide

All 700 Series systems are based on the 716 processor. The 725 configurations have software and support separately priced, while the 735s have these items bundled. Basic configurations are as follows:

- 725-G/735-G General-Purpose System — includes 716 processor in a 60-inch cabinet with control panel, real-time clock, multiline priority interrupt system with 3 levels implemented, power fail/auto restart, hardware multiply/divide, base-sector relocation, and 8K words of core; a teleprinter is also part of the basic configuration.
- 725-M Rack-Mounted System — for system builders who want to use their own cabinets; identical to 725-G, but no cabinet and power distribution unit.
- 725-S/735-S Sensor-Based System — includes 716 processor with control panel, real-time clock, watchdog timer, multiline priority interrupt system with 3 levels implemented, power fail/auto restart, hardware multiply/divide, base sector relocation, analog/digital subsystem controller capable of holding 8 digital and 8 analog pages (1 digital page is implemented), 8K words of core, and 2 cabinets; a teleprinter is also part of the basic configuration.

Processor options include parity, an additional crystal-controlled clock, watchdog timer (for the 725-G/735-G), 512 to 2,048 words of ROM, the communications controller, and a wide variety of peripherals. Memory can be expanded to 64K words, but expansion over 32K requires an extended memory controller that slows memory cycle time to 855 nanoseconds for the first 32K words and to 1,030 nanoseconds for memory above 32K. Memory is added in 8K-word increments with all eight modules housed in the system cabinet.

DMA and programmed I/O channels are standard to all systems. An optional Direct Multiplex Control (DMC) adapter can be added in order to attach a maximum of eight controllers from the Series 16 line of peripherals.

A Binary Synchronous Down-Line Load Option (2,048-word ROM) and other communications devices can be attached to either processor. Only the 725-S/735-S, however, can handle the real-time interface for sensor-based applications.

## Compatibility

The 716 instruction set includes the H316 and DDP-516 instruction set as a subset. An optional DMC adapter for the 716 allows connection of the H316 and DDP-516 peripherals that transfer data via a DMC unit.

Honeywell has introduced new peripherals that encompass all the other peripherals used with the H316 and DDP-516. As a result, virtually all software developed for the H316 and DDP-516 can run on the 716. The 716 processor has features that are unavailable for the H316 and DDP-516, so any 716 software using the new features cannot run on the other two processors.

## MAINTENANCE AND SUPPORT

Honeywell provides world-wide marketing support, including several hundred local offices for its Field Engineering Division. An emergency network provides service 24 hours a day, 7 days a week.

For the System 700, Honeywell has trained its commercial data processing field support staff to furnish the applications-oriented service required by minicomputer users. Recently, this support has been further enhanced by the opening of nine more new service centers. The total solution approach and the level of support should appeal to a wide range of customers.

## HEADQUARTERS

Honeywell Information Systems  
Computer Controls Division  
Old Connecticut Path  
Framingham MA 01701

**TYPICAL PRICES**

Model Number	Description	Monthly Rental \$ Short Term	Monthly Rental \$ 3 yr.	Purchase \$	Monthly Maint. \$
<b>CENTRAL PROCESSOR AND WORKING STORAGE</b>					
(includes a 716 CPU, real-time clock, auto restart, high-speed arithmetic/base sector relocation, cabinets, and drawers; memory must be ordered separately)					
725-G	General-Purpose Minisystem (with separately priced support)	260	240	7,600	40
725-S	Sensor Based Minisystem (with separately priced support)	625	570	16,700	85
725-M	Modular General-Purpose Minisystem (with separately priced support)	NA	NA	6,000	40
735-G	General-Purpose Minisystem (with bundled support)	393	362	11,800	40
735-S	Sensor Based Minisystem (with bundled support)	758	692	20,900	85
<b>Memory and CPU Options for Models 725 and 735</b>					
700-1209	8,192 Words of Main Memory (excludes parity)	115	105	3,200	30
700-1210	8,192 Words of Main Memory (with parity)	120	110	3,400	30
700-1220	256-Word ROM (for customer-supplied programs)	—	—	840	18
700-1222	1,024-Word ROM (for customer-supplied programs)	—	—	1,260	18
700-2022	Extended Memory System (for over 32K words of main memory; Model 735 only)	110	100	2,520	20
700-3000	Real-Time Clock/Watchdog Timer	26	23	720	5
700-3010	Direct Multiplex Control Adapter (for max of 8 controllers)	94	85	2,650	18
700-3030	Binary Sync Down-Line Load Option (2,048-word ROM)	53	47	1,480	10
<b>MASS STORAGE</b>					
700-4510	Fixed-Head Disc Subsystem (64K words; includes control)	347	313	9,825	40
700-4511	Fixed-Head Disc Subsystem (128K words; includes control)	490	442	13,860	55
700-4512	Fixed-Head Disc Subsystem (256K words; includes control)	620	560	17,385	75
700-4513	Fixed-Head Disc Subsystem (512K words)	925	835	25,960	110
700-4710	Removable Disc Storage Subsystem (1.1 million words; Model 735 only)	655	590	18,000	95
700-4720	Removable Disc Storage Subsystem (7.5M words)	1,830	1,220	35,800	180
700-4721	Additional Disc Pack Drive (7.5M words)	1,505	1,005	29,500	125
700-4740	Removable Disc Storage Subsystem (1.1M words)	480	434	12,515	101
700-4741	Removable Disc Storage Subsystem (1.8M words)	575	525	15,000	120
700-4742	Removable Disc Storage Subsystem (3.7M words)	765	695	20,000	160
700-4743	Removable Disc Storage Subsystem (7.5M words)	1,115	1,010	29,000	200
<b>INPUT/OUTPUT</b>					
<b>Magnetic Tape</b>					
700-4041/51	Mag Tape Subsystem (7/9-track, 26 ips); includes control and 1 tape unit (add up to three 700-4042 units)	355	325	10,000	95
700-4042/52	Additional Mag Tape Unit for 700-4041	245	225	7,000	70





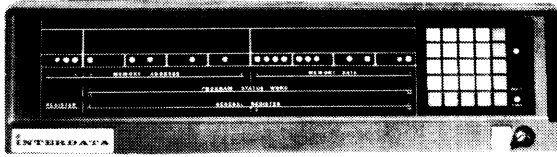
**TYPICAL PRICES (Contd.)**

Model Number	Description	Monthly Rental \$ Short Term	Monthly Rental \$ 3 yr.	Purchase \$	Monthly Maint. \$
700-4150	Mag Tape Subsystem (9-track, 36 ips)	640	426	12,500	145
700-4180	Mag Tape Subsystem (35 ips, 1,600 bpi)	565	515	15,300	150
700-4190	Mag Tape Subsystem (70 ips, 1,600 bpi)	590	540	17,000	160
	<b>Cassettes</b>				
700-5400	Cassette Tape Subsystem	146	133	3,575	35
700-5401	Additional Cassette Drive for 700-5400	38	35	925	10
	<b>Paper Tape</b>				
700-5010	Reader with Control (300 cps)	114	104	3,200	22
700-5210	Punch with Control (110 cps)	118	107	3,300	20
	<b>Punched Card</b>				
700-5100*	Reader Subsystem (300 cpm)	184	164	6,000	40
700-5123	Reader Subsystem (600 cpm)	327	296	6,000	85
700-5121	Reader Subsystem (800 cpm)	378	342	9,000	86
700-5122	Reader Subsystem (1,050 cpm)	429	388	10,000	113
700-5140	Reader/Punch Subsystem (400-/100-400 cpm)	675	615	20,800	120
700-5141	Punch Subsystem (100-400 cpm)	496	496	17,000	105
700-5151	Reader Subsystem (punched cards, 300 cpm)	170	155	4,350	50
700-5152	Reader Subsystem (punched and marked cards, 300 cpm)	225	205	5,800	55
	<b>Printers</b>				
700-5515	200-lpm Printer Subsystem (96 cols; requires 700-3010)	475	429	12,000	100
700-5516	200-lpm Printer Subsystem (132 cols; requires 700-3010)	605	550	12,000	115
700-5520	300-lpm Printer Subsystem (120 cols; requires 700-3010)	665	605	12,000	165
	<b>Teleprinters</b>				
Note: ASR 33 or ASR 35 is mandatory on all systems for maintenance and warranty purposes. A KSR 33 can be substituted for the ASR on those systems that include a paper tape reader, Type 700-5010, or any card reader.					
700-5300	Teleprinter Interface Only	22	20	840	10
700-5307	ASR 33 Teleprinter with Control	92	87	2,150	40
700-5310	KSR 33 Teleprinter with Control	66	60	1,850	35
700-5507	ASR 35 Teleprinter with Control	184	166	5,200	35
	<b>DATA COMMUNICATIONS</b>				
	<b>Synchronous/Asynchronous Equipment</b>				
700-6312	Sync Single-Line Controller	55	50	1,400	15
700-6316	MIL STD 188C Interface	34	31	570	13
700-6321	Low-Speed Multiline Controller	268	241	6,885	40
700-6322	Universal Multiline Controller	277	250	7,140	40
700-6333	Medium-Speed Multiline Controller	58	53	1,615	10

NA Not Available

Notes: NA Not available  
— Not applicable  
\* Not available on new orders





75-17

### OVERVIEW

Interdata's Model 7/32 computer is a microprogrammed 32-bit minicomputer that is at the bottom of Interdata's new 32-bit line; at the same time, it can operate in a 16-bit mode to use application programs developed for Interdata's 16-bit systems. Because it uses a 32-bit word, the 7/32 can directly address 1 million bytes of memory and can handle higher-precision arithmetic operations than the 16-bit line. The 7/32 is a processor designed for the top end of the minicomputer market, designated by Interdata as the "mega-mini" market.

The 7/32 uses memory modules that can store up to 32 kilobytes of core memory on a single circuit board. Memory cycle time is either 750 or 1,000 nanoseconds for 2 bytes. Maximum memory capacity is 1,048,576 bytes for the 7/32.

The 7/32 falls between Interdata's 7/16 and 8/32 minicomputers. The 7/16 is a 16-bit machine that can be expanded in the field to a 7/32. The 7/32 can operate in either the 16-bit mode of the 7/16 or the 32-bit mode used exclusively in the faster 8/32.

Interdata's 7/16 is a 16-bit machine with the same basic architecture as the earlier "New Series," but with a larger instruction set and 32K-byte memory boards. The New Series consisted of Models 50, 55, 60, MS-5, 70, 74, 80, and 85; the first four models use special communications instruction sets and the latter four use general-purpose instruction sets. The 7/16 can be field upgraded to a 7/32 by means of a special "stretch 32" option.

The 7/32 uses the same basic architecture as Interdata's earlier computers but with some notable extensions: 32 hardware accumulators, 30 index registers, both multiplexor and selector I/O channels, large multilevel priority interrupt system, I/O Auto Drive Channels, and large instruction set. The 7/32 uses 136 instructions, a superset of the 16-bit New Series and 7/16 instruction set. Like the 7/16, the 7/32 is well suited for communications by virtue of its sophisticated interrupt handling system (up to 1,023 levels). The 7/32 also has a specialized set of standard instructions for data communications applications including code translation, CRC-16, and special character recognition. Table 1 lists the 7/32 mainframe characteristics.

The 8/32 is a 32-bit machine with a full 32-bit bus structure, four-way interleaved memory, 214 instruction set, up to 1 million bytes of directly addressed memory, dual 64-bit lookahead stacks and eight dual stacks of 16 32-bit general registers for user, I/O, and OS programming as

**Table 1. Interdata Model 7/32: Processor Characteristics**

<b>Central Processor</b>	
Type	Microprogrammed
No. of Internal Registers	32 (2 stacks of 16)
Use	general purpose; 30 indexable
<b>No. of Instructions</b>	
Standard	136
Optional	17
<b>Fixed-Point Arithmetic</b>	
Add/Subtract	Std
Multiply	Std
Divide	Std
Add time ( $\mu$ sec)	3.25 to 3.75
<b>Floating-Point Arithmetic</b>	
	Opt
<b>Addressing</b>	
Direct (16-bit half-words)	524,288 (1M bytes)
Indirect	No
Indexed	Yes (2 levels)
Max I/O devices	1,023
<b>Priority Interrupt System</b>	
Lines	8
Levels	1,023
<b>Memory</b>	
Type	Core
Word length (bits)	32 (two 16-bit fetches)
Cycle time/word ( $\mu$ sec)	0.75; 1.0
<b>Capacity (16-bit half-words)</b>	
Max	524,288
Min	8,167
Increment	2K, 4K, 8K
Parity	Opt
Protect	Opt
ROM	Std
Use	Microinstructions (control store)
<b>I/O Channels</b>	
Programmed I/O	Std (Auto Drive Channels)
Direct Memory Access	Std
No. of channels	7
Multiplexed I/O	Std
Selector Channel	Opt
Over DMA	2.6M
Over selector channel	2.0M

well as rapid context switching. The 8/32 uses the same 750-nanosecond core modules (16-bit words) as the 7/16 and 7/32, achieving greater processing speed by virtue of the four-way core interleaving, the lookahead stacks, and 32-bit wide memory bus.

Software for the 7/32 includes two new operating systems, OS/32ST, a serial (batch) processing system, and OS/32MT, a multiprogramming real-time system. Language processors for the 7/32 include FORTRAN V, the CAL assembler common to both 32-bit and 16-bit lines, and BASIC. The 7/32 was first delivered in August 1974.

### PERFORMANCE AND COMPETITIVE POSITION

The 7/32 is at the bottom of Interdata's 32-bit line, a line extending from minicomputer power at the level of the Digital PDP-11/40 and Data General ECLIPSE all the way up to the middle of the IBM System/370 line with the 8/32. The system will not impact the small-to-medium computer market that used to be the exclusive property

of the large mainframe manufacturers however, because the larger computer manufacturers offer software support and custom programming that puts them in another league. With the 7/32 competing against 16-bit systems in the minicomputer market, Interdata stresses not only cost but inherent software advantages over its competitors due to use of the 32-bit word. The 7/32 can address all large memories directly. Unlike 16-bit word computers, it does not require a memory management hardware unit to convert virtual memory addresses to physical addresses for memories beyond 64K addresses. The advantage is programming simplicity and easy-to-implement operating systems.

In addition, the 32-bit word restricts program size only to that of physical memory and not to the size of the largest virtual memory segment. Virtual addresses need not be converted to physical addresses via a memory management unit. This process slows down program execution time by lengthening memory access time and by increasing the operating system overhead for loading and maintaining memory mapping registers. Also, a real-time operating system is easier to develop when the system does not require a management unit, and it needs less memory for its implementation. Other minicomputer manufacturers, MODCOMP, for instance, have 32-bit machines, but so far, Digital and Data General are still using 16-bit lines. Part of the reason for staying with the 16-bit word is the cost of developing new software. Nevertheless, many industry observers feel that it will not be long before most mini makers will produce 32-bit systems (and cut into the market for big computers).

Interdata has produced both of the 7/32's operating systems on schedule, and this factor has considerably strengthened the system's original position vis-a-vis the minicomputer giants. Although addressing a large market with the 7/32, this market will be expensive to compete in, because of the strong systems already available. Interdata must develop considerable software to compete successfully. Having a larger system to offer users who are moving up strengthens the company's position. The 7/16 is now the entry-level system; users can then advance to the 7/32 for medium-range processing power, or go all the way to the powerful 8/32. The market range for Interdata computers is quite broad; not only have the 7/32 and 8/32 increased the size of the market for which these computers are applicable but they protect the firm's customer base from wandering as their processing needs increase.

**Configuration Guide**

The basic Model 7/32 system consists of a central processor with 136 instructions that include hardware multiply/divide, 32K bytes of core memory with cycle time of 0.75 microsecond, power supply, and chassis with 16 slots. The central processor uses three circuit boards, and each 32K bytes of memory uses one board. The 7/32 can be expanded by 32K-byte core memory modules to a maximum of 1,048,576 bytes. Other optional features include floating-point arithmetic, memory protect, power

fail/auto restart and display console with hexadecimal display and hexadecimal character keys. The 7/32 uses a 16-bit wide I/O bus and can use the same peripherals as the 7/16. Table 2 lists the available peripheral devices.

Configuration requirements for the operating systems and language processors are described in Table 3.

**Compatibility**

Although not 100 percent compatible, the Model 7/32 can run application programs developed for the New Series processors and for the 7/16. The 7/32 uses a 32-bit word, but it can run programs in a 16-bit word mode under control of a mode bit in the program status doubleword. It uses the same chassis, power supplies, peripheral controllers, and memory modules used by all the New Series processors.

**Table 2. Interdata Model 7/32: Peripherals**

Model Number	Description
<b>Punched Tape</b>	
M46-240	300-cps reader
M46-242/250	300-cps reader, 75-cps punch
<b>Punched Card</b>	
M46-230/236	400-/1,000-cps reader
<b>Printers</b>	
M46-204	60 to 200- lpm, 132-col, 64-char set
M46-207/209	200/600- lpm, 132-col, 64-char set
<b>Terminals</b>	
M46-000/001	ASR 33/35 TTY
M46-100-103	A/N display, 4,920 char, to 9,600 baud
M46-108	Graphic display, to 9,600 baud, 1,024 x 1,024 point matrix
<b>Magnetic Tape</b>	
M46-400	Dual-drive cassette, 500K bytes/cassette, 1,000-cps xfer rate
M46-460	9-trk, 800-bpi magnetic tape, 45 ips
M46-465-467	9-trk, 1,600-bpi magnetic tape, 45 ips, 4 drives/controller
M46-476	7-trk, 556- or 800-bpi (not both) magnetic tape subsystem, 4 drives/controller
<b>Discs</b>	
M46-410	2.5M bytes, 5440-type removable cartridge disc, 4 drives/controller
M46-516	10.0M bytes, fixed/removable 5440-type cartridge disc, 4 drives/controller
M46-429	40.0M bytes, 2316-type disc pack, 4 drives/controller
<b>Process I/O</b>	
M48 series	Wide-range analog input, up to 512 channels
M48 series	High-speed low-level analog input, up to 64 channels
M48 series	High-level analog I/O, up to 8 differential or 16 single-ended inputs
M48 series	Real-time analog controller, two 32-word solid-state buffer memories
M07/M48	Digital multiplexor subsystem, 2,048 input & 2,048 output lines
<b>Communications</b>	
M10-022	Auto dial units, 4-lines
M11-200	IBM 360/370 interface multiplexor (burst or block modes) channel
M47-000/001	Bell-type adapters, 201/301, to 9,600/40,800 baud
M47-100	Async line module controller, up to 92 lines, to 1,800 baud
M47-101/102	Programmable single-line module/adapter for Bell 103 & 202



**Table 3. Interdata Model 7/32: Software**

Package	Description
OS/32 MT	Real-time multiprogramming, multitask operating system, up to 255 priority levels; requires 32-bit Interdata computer, 65K bytes of memory, operator console, TTY, memory protect, clock
OS/32ST	Serial task operating system, upward compatible with OS/32MT; requires 32-bit processor, 65K bytes of memory, operator console, TTY
FORTTRAN V	ANSI x 3.9 - 1966 FORTRAN IV with extensions including ISA calls, requires 32-bit CPU, 8K bytes of memory above operating system requirements, operator console, TTY
CAL	Common Assembly Language for both 16-bit and 32-bit systems; requires 8K bytes of memory above operating system requirements on 32-bit CPU, console, TTY
BASIC	Extended Dartmouth BASIC, for single user; requires 32-bit CPU (in 16-bit mode), 10.5K bytes of memory above operating system requirements, console, TTY

The 7/32 programs are upward compatible with those of the 8/32.

### MAINTENANCE AND SUPPORT

Interdata supplies systems on a purchase-only basis. Users can negotiate separate maintenance contracts for on-site engineers (1, 2, or 3 shifts) or they can take damaged boards to a repair depot. Maintenance service can also be obtained on a per-call basis.

Interdata has offices in more than 34 locations in the United States and Canada as well as in Japan, Australia, Great Britain, and Germany.

### HEADQUARTERS

Interdata  
2 Crescent Place  
Oceanport NJ 07757  
(201) 229-4040

### TYPICAL PRICES

Model Number	Description	Purchase \$*	Monthly Maint \$
	<b>MODEL 7/32 GENERAL PURPOSE PROCESSOR</b> 32-bit processor capable of directly addressing 1,000,000 bytes of main memory; includes 32 GP Registers, each 32 bits wide, high-speed multiply/divide, DMA connection, privilege instruction detect, 1,024 hardware vectored interrupt levels, up to 1,024 automatic driver channels and autoload bootstrap instruction for initial loading	9,950	110
M73-023	Model 7/32 Processor with 32,768 Bytes of Core Memory (750 nsec, 16-slot chassis, and power supply)		
	<b>MODEL 7/32 PROCESSOR OPTIONS</b>		
M73-100	Power Fail Detection/Auto Restart	400	2
M73-101	Floating-Point Hardware	3,900	30
M73-103	DMA Buffer	350	5
M73-104	Memory Access and Protect Controller	3,500	25
M73-105	Extended Memory Selector Channel	1,000	10
M73-106	Local Memory Bank Interface	5,900	50
M73-107	Processor Parity Control	1,000	-
M71-101	Binary Display Panel	300	2
M71-102	Hexidecimal Display Panel	600	5
M70-104	Loader Storage Unit controller	500	10
M70-105	128-Byte Storage Module	100	-
M48-005	Multiplexor Bus Buffer	900	-
M71-300	<b>MODEL 7/32 MEMORIES</b> 8,192-Byte Memory Expansion Module (1-µsec core cycle time)	2,000	20
M71-302	16,384-Byte Memory Expansion Module (1-µsec core cycle time)	2,650	30
M71-304	32,768-Byte Memory Expansion Module (1-µsec core cycle time)	3,950	40
M73-306	M71-304 with 750-nsec core cycle time	4,500	45
M71-301	M71-300 with parity	2,500	20
M71-303	M71-302 with parity	3,150	30
M71-305	M71-304 with parity	4,450	40
M73-307	M73-306 with parity	5,000	45
	<b>SYSTEM MODULES</b>		
M48-012	Line Frequency Derived Clock	250	5
M48-000	Universal Clock Module	600	5
M48-001	8-Line Interrupt Module	900	5
M48-002	General Purpose Interface Board (15 inches)	550	NA
M48-013	Universal Logic Interface	650	NA
M48-014	Input/Output Bus Switch	1,500	10
M48-107	Extension Cable Kit, 25 feet	175	-
M48-018/9	Manual Control Panel for I/O Bus Switch	200	-
	<b>DISC</b>		
M46-410	2.5M-Byte Removable Cartridge Disc System	10,000	80
M46-414	2.5M-Byte Removable Cartridge Disc System	10,100	80
M46-411	2.5M-Byte Removable Cartridge Disc Expansion Drive	5,500	50
M46-420	Removable Cartridge Disc Interface (for use with up to four 2.5M-byte disc drives)	4,000	30
M49-023	Expansion Power Supply for Single Drive Disc	500	-
M49-027	Expansion Power Supply for Single Drive Disc	600	-
27-039	2.5M-Byte Removable Cartridge Disc Pack	200	-
M46-416	10M-Byte Removable Cartridge Disc System	12,000	120
M46-417	10M-Byte Removable Cartridge Disc System	12,100	120
M46-418	10M-Byte Removable Cartridge Disc Expansion Drive and Power Supply	8,000	90
M46-419	50-Hz Version of M46-418	8,100	90
M46-421	Removable Cartridge Disc Interface (for use with up to four 10M-byte dual disc drives)	4,000	30
27-056	10M-Byte Removable Cartridge Disc Pack	270	-
M46-429	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	24,950	200
M46-430	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	25,100	200
M46-431	40M-Byte Removable Cartridge Disc Expansion Drive	17,950	200
M46-432	40M-Byte Removable Cartridge Disc Expansion Drive	18,100	200
M46-433	Removable Cartridge Disc Controller (for use with up to four 40M-byte disc drives)	7,000	50
M46-434	40M-Byte Removable Cartridge Disc Pack	500	-
M48-010	<b>TELETYPE CONSOLES</b> ASR Model 33/35 TTY Interface (with internal cable)	350	5
M46-000	ASR Model 33 Teletypewriter (with external cable)	1,450	40
M46-002	50-Hz Version of M46-000	1,550	40
M46-001	ASR Model 35 Teletypewriter (with external cable)	4,200	40
M46-003	50-Hz Version of M46-001	4,300	40
	<b>PAPER TAPE EQUIPMENT</b>		
M46-250	Combination Paper Tape Reader/Punch Interface	900	10
M46-240	Paper Tape Reader, Uni-directional (300 cps)	1,300	20
M46-241	50-Hz Version of M46-240	1,400	20
M46-242	Combination Paper Tape Reader/Punch (300/75 cps)	3,300	40
M46-243	50-Hz Version of M46-242	3,400	40
	<b>PUNCHED CARD</b>		
M46-235	Card Reader Interface (with internal cable)	900	10
M46-234	Hardware Hollerith to ASCII Conversion Option	350	-
M46-230	Card Reader (400 cpm; includes external cable)	3,000	40
M46-231	50-Hz Version of M46-230	3,100	40
M46-236	Card Reader (1,000-cpm; includes external cable)	5,900	80
M46-237	50-Hz Version of M46-236	6,000	80
	<b>PRINTERS</b>		
M46-202	Line Printer Interface (and internal cable for 60 to 200 lpm line printer)	500	10
M46-204	Fully Buffered Line Printer (60 to 200 lpm, 132 cols, 64 char set; includes external cable)	5,000	50
M46-205	50-Hz Version of M46-204	5,200	50
M46-206	Line Printer Interface (and internal cable for 200 or 600 lpm line printer)	750	10
M46-207	Full Buffered Line Printer (200 lpm, 132 cols, 64 char set; includes external cable)	12,350	90
M46-208	50-Hz Version of M46-207	12,650	90
M46-209	Fully Buffered Line Printer (600 lpm, 132 cols, 64 char set; includes external cable)	17,150	110
M46-210	50-Hz Version of M46-209	17,450	110
	<b>MAGNETIC TAPE</b>		
M46-400	INTERTAPE Cassette system with dual transports, 1,000 char per sec read/write speed, hardware read-after-write check, longitudinal redundancy check, 500,000-byte capacity per cassette; includes interface)	4,200	30

# INTERDATA — 7/32 SYSTEM

## TYPICAL PRICES (Contd.)

Model Number	Description	Purchase \$*	Monthly Maint \$
M46-470	9-Track, 800 bpi, Magnetic Tape Transport Interface (interface controls up to 4 IBM compatible continuous read-after-write 45 ips drives; includes cyclic redundancy check hardware and read-after-write check)	2,900	20
M46-460	9-Track, 800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-461	50-Hz Version of M46-460	6,100	90
M46-473	7-Track, 556 bpi Magnetic Tape Transport Interface	2,900	20
M46-474	7-Track, 800 bpi Magnetic Tape Transport Interface	2,900	20
M46-476	7-Track, 556/800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-477	50-Hz Version of M46-476	6,100	90
M46-471/2	Magnetic Tape Transport Direct Connect Cable	100	—
M46-475	9-Track, 1,600 bpi, Magnetic Tape Transport Interface (controls up to 4 IBM compatible, continuous read-after-write 45 ips drives via a phase-encoded formatter supplied with M46-465 or M46-466)	1,500	10
M46-465	9-Track, 1,600 bpi, 45 ips Magnetic Tape Transport and 1 x 4 Phase-Encoded Formatter (continuous transfer rate is 72,000 char/sec)	12,000	120
M46-466	50-Hz Version of M46-465	12,100	120
M46-467	9-Track, 1,600 bpi, 45 ips, Magnetic Tape Expansion Transport (for use with M46-475 and M46-465)	6,800	80
M46-468	50-Hz Version of M46-467	6,900	80
M46-107	VIDEO DISPLAY 1,200 Baud Local Current Loop Interface (with internal cable)	400	5
M46-100	Alphanumeric Video Display Unit (1,920 char (24 lines x 80 char); std 64 char ASCII subset; 110 or 1,200 baud via current loop interface; up to 9,600 baud with RS-232C)	2,250	30
M46-101	Std 50-Hz Version of M46-100	2,350	30
M46-102	M46-100 with complete processor and operator cursor control, a full range of editing features, and message and character modes	3,350	40
M46-103	50-Hz Version of M46-102	3,450	40
M46-108/9	Graphic Display Terminal	6,500	60
M46-104/5/6	External Cable Assembly	—	—
<b>DATA COMMUNICATIONS SYSTEMS MODULES</b>			
M47-000	Bell 201 Type Data Set Adapter or Equivalent	1,200	10
M47-001	Bell 301 Type Data Set Adapter or Equivalent	1,400	10
M47-102	Programmable Async Single Line Adapter (for 103/202 data set or local RS-232 terminal)	400	5
M47-100	Async Line Module Controller	500	10
M47-101	Programmable Async Line Module	1,200	10
M49-021	Programmable Async Line System Chassis	550	—
M10-022	Automatic Dial Unit Controller	1,600	10
M10-054	Data Set Cable (for RS232 compatible data sets)	60	—
M10-056	Data Set Cable (for Bell 301 type data sets)	350	—
M47-200	IBM 360/370 Parallel Interface (single address interface)	3,500	50
M47-201	IBM 360/370 Parallel Interface (multiple address (up to 256) interface)	5,000	60
<b>CABINETS, CHASSIS, AND POWER SUPPLIES</b>			
M49-020	System Chassis	700	—
M49-024	Power Supply	800	5
M49-026	Bulk Power Supply	1,000	5
M49-003	Adapter Card (10 to 15 inches)	150	—
M49-004	System Cabinet	650	—
<b>SOFTWARE**</b>			
S90-000-16	BOSS PLUS Source Paper Tape and Documentation Package	175	—
S90-001-16	DOS PLUS Source Paper Tape and Documentation Package	500	—
S90-002-46	RTEX Source Card and Documentation Package	1,500	—
S90-003-26	RTOS Source Cassette and Documentation Package	2,000	—
S90-004-26	OS/16 MT Source Paper Tape and Documentation Package	950	—
S90-005-11	OS/32 ST Source and Object Paper Tape and Documentation Package	750	—
S90-007-11	OS/32 ST Object Paper Tape and Documentation Package	300	—
S90-006-41	OS/32 MT Source Card and Object Paper Tape and Documentation Package	3,000	—
S90-009-21	OS/32 MT Object Cassette and Documentation Package	2,500	—

\* Quantity discounts are available on most items. NA Not Available — Not Applicable

\*\*Additional Software Documentation Packages available.

ITAM (Interdata Telecommunication Access Method) has been introduced by Interdata for use with the Model 7/32. The package runs under OS/32-MT, Interdata's 32-bit multitasking operating system. A minimum ITAM system includes the Model 7/32 with 65 bytes of memory, OS/32-MT, memory access controller, a real-time clock, control console, and appropriate data set adapters. The 7/32 offers as standard features data communications instructions, auto driver channels, and DMA transfer rates of two megabytes per second.

ITAM provides two levels of communications: device independent and device dependent.

On the device independent level, remote devices are accessed as though they are directly attached peripherals. Asynchronous terminals such as A/N displays and teleprinters can be supported. A remote job entry (RJE) package for the 7/32 can also be included to allow it to emulate an IBM 2780 or 3780 remote batch terminal. Processor-to-processor communication using binary synchronous (BSY) protocol is also supported.

On the device dependent level, users can develop special systems with minimum operating system overhead. Interdata offers asynchronous and binary synchronous modules that can accommodate a variety of facilities, protocol, and networks so the sophisticated user can provide his own terminal protocols. ITAM simplifies the user's software interface. Users, for example, can initiate, via one request, a single message followed by a series of message receptions.

The purchase price for ITAM is \$2,500; it became available in May 1975.

Interdata has also introduced two new language processors to help users increase their programming capabilities: MACRO CAL and BASIC/32.

MACRO CAL provides alternate macro libraries and keyword macro prototypes. It can be used with all Interdata minicomputers, both 16- and 32-bit. MACRO CAL requires 24K bytes of main memory; it includes a macroprocessor, utility program, and reference manual in addition to the system macro library. Each programmer can develop his own library of macros that refer to his programs and applications.

Keyword macro prototypes allow programmers to use symbolic references in the macro routine to the arguments or variables in the macro's parameter list. Operands or data quantities can be written in any order or omitted with default values or standard conditions provided.

The BASIC/32 interpreter requires 10K bytes of main memory. It includes the BASIC Interpreter, Language/Operating procedure, as well as matrix handling, string data manipulation and pattern matching. BASIC/32 is reentrant for multiuser operations in a terminal-oriented environment.

Some Interdata BASIC/32 standard features include run time trace facilities, set trace, end trace, matrix operations, extended interface statement, and INPUT and PRINT via logical unit.

MACRO CAL costs \$300 and BASIC/32 \$150; both are immediately available.







**OVERVIEW**

The Interdata 8/32 Megamini is the first all 32-bit system in Interdata's line of minicomputers. It is at once the top of the Interdata line and a front runner in the upward push of the minicomputer market into the small- and medium-scale ranges. The 32-bit word allows it to address up to 16 megabytes of main memory, although, at present, memory capacity is limited to 1 megabyte. The speed of the system, throughput efficiency, input/output transfer rate and software have all been designed to make it competitive in the midcomputer range. The system is upward compatible with Interdata's 16-bit-line, giving Interdata users a roomy upward growth path. The I/O bus is 16 bits wide to maintain compatibility with standard peripherals. The memory modules are the same ones used with the 7/32 and 7/16 systems, but two 16-bit-word modules operate in tandem over two 16-bit-wide buses to make up the 32-bit word. In other respects, cache memory registers, memory interleaving, I/O organization and a number of other features enhance throughput. Table 1 lists specifications.

Interdata sees a sizeable new market for 32-bit real-time "midcomputers" because of their low cost, high speed and reliability. One area, of course, is data communications, which has long been one of Interdata's strong fields. Other markets identified are power grid analysis, nuclear power plant control and refinery monitoring, all of which could use the Megamini for economic problem solving. Air traffic control and banking applications also show promise.

With these applications in mind, Interdata recently has added more software capability. The Model 8/32 Megamini can run under the OS/32 ST for batch program development and under OS/32 MT, a multitasking operating system which was delivered in December 1974 for the 7/32. FORTRAN V, Level II is available for program development, as well as Macro CAL, the assembler language common to all Interdata computers. BASIC is available as a

**Table 1. Interdata 8/32 Megamini: Mainframe Specifications**

<b>Central Processor</b>	
Microprogrammed	Yes
No. of Internal Registers	32-128
Addressing	
Direct	To 1M bytes
Indirect	No
Indexed	Yes, 2 levels
Instruction Set	
Number	214
Decimal Arithmetic	No
Floating Point Arithmetic	Yes (opt)
User-microprogramming	Not software supported
Interrupt System	
Lines	4
Levels	1,024 std
Main Storage	
Type	Core
Cycle Time (nsec)	750
Basic Addressable Unit	32-bit word
Cache memory	Lookahead Stack
Min Capacity (bytes)	128K
Max Capacity (bytes)	1M
Increment Size (bytes)	32K
Ports per module	1
Memory Interleaving	4-way
Error Checks	Parity
Protection	Opt
Memory Management	Yes (opt)
<b>ROM</b>	
Use	Control Store
<b>I/O Channels</b>	
Programmed I/O	Yes
DMA channels	1 (up to 7 selectors)
Multiplexed I/O	1,024 subchannels
<b>Max Transfer Rate</b>	
Over DMA, bytes/sec	6M
MUX I/O, bytes/sec	62.5K

compiler and as an interpreter. In addition to these, Interdata has added ITAM, Interdata's Telecommunications Access Method, employing both device-independent and device-dependent modes to meet users' needs.

In addition to standard peripherals available for the 16-bit systems and the 7/32, Interdata has added new 360/370 interfaces that allow the 8/32 to interface directly to a block multiplexor, multiplexor, or selector channel of the IBM systems. These interfaces facilitate the development of front-end systems that look like 270X/370X to the host computer and strengthen Interdata's position in the communications marketplace. The dual I/O system, with a multiplexor bus for up to 1,024 low- or medium-speed devices and a DMA bus with selector channels for mass storage (up to 112 controllers) provide powerful I/O facilities which will be particularly useful for multiprocessor configurations for shared data bases that are undoubtedly in Interdata's future.

The first 8/32 Megamini was delivered in June 1975.

Interdata is a small but rapidly growing company, organized in 1966. As of June 1975, it had delivered more than 3,000 systems; the company employs around 1,000 persons world wide, with offices in 25 U.S. cities, and four

other countries — England, Germany, Canada and Australia. Interdata became a subsidiary of the Perkin-Elmer Corporation in 1974, a move designed to enhance the financial position of the company by providing access to more development funds.

## COMPETITIVE POSITION

The Model 8/32 Megamini is a fine addition to Interdata's line of computers, expanding the power and thus the market of its system upward. This upward thrust has been exhibited by all the minicomputer manufacturers, even Computer Automation, and has interesting ramifications for the whole computer industry. The low end of the minicomputer market has been usurped by microcomputers and, with the dispersal of computer power and real-time interactive processing in vogue, all manufacturers have seen that their real-time systems can be expanded and speeded up to compete against medium scale, general purpose systems at much lower prices than, for instance, IBM. There is a trade-off of course. The minicomputer manufacturer does not supply the kind of software support that the large mainframe manufacturer does. On the other hand, the cost of a large mini can be as low as one tenth the cost of the smallest real-time IBM 370, the 158. Because the minis are oriented toward real-time and the 370 series is oriented toward batch processing, many applications are suited to "megaminis" or "midis", which are about the size of a 370/135, a batch system. Thus the midis don't really have competition from IBM because IBM enters at the high end of the real-time market.

The two minicomputer leaders, Digital and Data General, have approached this market with memory management systems that expand their 16-bit systems, instead of producing a 32-bit system. The only other 32-bit minicomputer system now on the market is the SEL32, made by Systems Engineering Laboratories, a small company that has had inconsistent management but good

equipment. Thus, the strongest competition from mini-computer makers are from systems that already are using devices that increase throughput or memory size. These companies will have to devise more and more techniques to expand their systems further. The Interdata 32-bit line is just beginning to explore and exploit its capabilities, and it can easily move upwards, particularly in memory capacity.

The Xerox 550 is also a strong competitor in performance but, unlike other manufacturers like SYSTEMS with its SEL32, Xerox has not managed to bring hardware costs down.

Interdata's chief advantage over medium-scale, general purpose systems like the IBM 370/158 is price. But what a difference. Table 2 presents a comparison of the specifications of five chief competitors in the midicomputer field.

Users of Interdata's smaller computers have a system to move up to as the need for power expands. The name of the game today is to capture the first-time computer user when he enters the market; to maintain the customer base with a diversified compatible supply of computer products reaching up into the medium scale range; and to keep products, price and performance competitive by redesigning products around new technologies. Many computer users are loyal to a product line because of their investment in applications software. A manufacturer cannot expect to capture very many new customers at the high end of the computer line.

Interdata already has a substantial number of orders for the 8/32, primarily for aerospace simulation and data communication applications. Because the 8/32 is powerful but low-cost, Interdata believes new operations will be computerized for the first time, and this will open markets in the midi range. It remains to be seen how big that market is.

**Table 2. Interdata 8/32 Megamini: Comparison With Other Computer Systems**

	Interdata 8/32	Digital PDP-11/70	SEL 32	XEROX 550	IBM 370/158
Word Length	32 bits	16 bits*	32 bits	32 bits	32 bits
Instruction Times, $\mu$ sec (Memory to Register)					
Integer Add	1.2	1.8	1.2	1.8	.9
Integer Multiply	3.5	3.9	4.5	6.2	2.0
Integer Divide	5.8	8.3	5.1	14.4	9.9
Floating Point Add	2.3	8.2	3.0	6.1	2.4
Floating Point Multiply	3.0	11.2	4.5	9.1	2.3
Floating Point Divide	5.3	12.2	8.9	23.3	8.9
Hardware I/O	Yes	No	No	Yes	Yes
Max. DMA Rate/Second	6MB	4MB (UNIBUS); 5.8MB (data- channel)	6MB	4MB	6.7MB
Max. Address	1MB	64KB	512KB	1MB	16MB
GP Registers	8 Stacks of 16 each	2 Stacks of 8 each	1 Stack of 4	4 Stacks of 16 each	1 Stack of 16
Pricing (\$)					
CPU + 128KB Memory	51,900	54,600(1)	43,900	128,700	NA
+ 256KB Memory	70,900	68,800	71,700	178,700	NA
+ 512KB Memory	107,400	101,800	128,000	278,700	1,779,200
+ 1048KB Memory	179,400	163,800	238,400	478,700	1,905,700

**Notes:**

\*Uses 16-bit operands but data paths between cache and memory and high speed device controllers are 32 bits wide.

(1) Console, installation, and parity are bundled with the PDP-11/70.



Interdata, like other minicomputer manufacturers, has traditionally been a tool maker, not a problem solver. As long as customers were sophisticated, they could develop the software techniques to convert the tools into solutions. This market has been largely saturated, at least enough to prevent continued growth of the minicomputer market from that source.

Recognizing this, Interdata has begun to focus its marketing effort toward specific types of applications — not just vertical markets but types of applications that cut across vertical markets. These include such things as industrial continuous and batch process control, test and measurement, seismic data processing, and simulations.

So far, Interdata has steered clear of commercial data processing, although others have developed commercial systems using Interdata computers. Most noteworthy is the COBOL-oriented commercial system developed by Diversified Data Systems, Inc., of Tucson, Arizona. Since it was first delivered for the 16-bit computers during the second quarter of 1974, over 50 systems have been delivered. A version for the 32-bit Interdata systems is scheduled for delivery in September 1975. It is called IBOLS-32 (Integrated Business Oriented Language Support) and provides batch services similar to that of the IBM 360 OS/MFT. It includes the COBOL compiler, sort/merge, ISAM initialize and run-time ISAM support. The one-time system license fee is \$12,500.

It is not surprising that the Interdata hardware is being used for commercial data processing, because the instruction set is very similar to the IBM 360 instruction set.

Interdata is working on a new optimizing FORTRAN compiler for its 32-bit computers. Most of the 8/32 Megamini users will be programming in FORTRAN, and this will enhance system throughput for most customers.

The next year will be crucial to Interdata as a company. So far, Perkin-Elmer has left Interdata alone while financing its expansion. This will undoubtedly continue only if Interdata's revenue continues to increase. In today's transitional market, minicomputer manufacturers are finding they cannot market in the same old way. Customers are more interested in problem solutions than in tools. Thus, companies must spend more creative energy on planning and marketing strategy. Interdata appears to understand today's market; it will be interesting to watch the company's response to it.

## CONFIGURATION GUIDE

The basic 8/32 system consists of a 32-bit processor with two sets of 16 32-bit registers, 1,024 interrupt levels, up to 1,024 multiplexed autodriver channels, DMA channel, 128K bytes of core memory, two power supplies, and a 16-slot chassis. The following processor options are standard:

- Memory expansion up to 1M bytes.
- Register expansion to eight sets of 16 registers each.

- Floating point processor with one or two associated sets of registers (single precision only; or both single and double precision).
- Memory parity generation and checking.
- Field upgrade kit for converting 7/32s into 8/32s.

Memory is added in 32K-byte modules. Although core and semiconductor memories can be mixed on a system, Interdata offers only core at the present time.

Up to 1,024 devices can be addressed. The interrupt subsystem allows up to 1,024 device interrupts, and the multiplexor channel can attach 1,024 slow to medium speed devices. In addition to the multiplexor channel, a DMA channel is also standard. Up to seven selector channels can be implemented on the DMA, with up to 16 high speed and mass storage subsystems per channel.

The disc, magnetic tape, paper tape, card, printer, process I/O and communications peripherals used on the 7/32 can also be used on the 8/32. Table 3 outlines specifications of these.

**Table 3. Interdata 8/32 Megamini: Peripherals**

Model Number	Description
<b>Punched Tape</b>	
M46-240	300 cps Readers
M46-242/250	300 cps Reader, 75 cps Punch
<b>Punched Card</b>	
M46-230/236	400 1,100 cps readers
<b>Printers</b>	
M46-204	60-200 lpm, 132 col, 64-char set
M46-207/209	200/600 lpm, 132 col, 64-char set
<b>Terminals</b>	
M46-000/001	ASR 33/35 TTY
M46-100-103	A/N Display, 4,920 char, to 9,600 baud
M46-108	Graphic Display, to 9,600 baud, 1,024 x 1,024 point matrix
<b>Magnetic Tape</b>	
M46-400	Dual drive cassette, 500K bytes/cassette 1,000 cps xfer
M46-460	9-trk 800 bpi mag tape, 45 ips
M46-465-467	9-trk 1,600 bpi mag tape, 45 ips, 4 drives/controller
M46-476	7-trk, 556 or 800 bpi (not both) mag tape subsystem, 4 drives/controller
<b>Discs</b>	
M46-410	2.5Mb 5440-type removable cartridge disc, 4 drives/controller
M46-516	10.0Mb fixed/removable 5440-type cartridge disc, 4 drives/controller
M46-429	40.0Mb 2316 type disc pack, 4 drives/controller
<b>Process I/O</b>	
M48 series	Wide Range Analog Input, up to 512 chans
M48 series	High Speed Low Level Analog Input, up to 64 chans
M48 series	High Level Analog I/O, up to 8 differential or 16 single-ended inputs

**Table 3. (Contd.)**

Model Number	Description
M48 series	Real Time Analog Controller, two 32-word solid state buffer memories
M07/M48	Digital Multiplexor Subsystem, 2048 Input & 2048 output lines
<b>Communications</b>	
M10-022	Auto Dial Units, 4-lines
M11-200	IBM 360/370 Interface Multiplexor (Burst or Block modes) channel
M47-000/001	Bell-type Adapters, 201/301, to 9,600/40,800 baud
M47-100	Async Line Module Controller up to 92 lines to 1,800 baud
M47-101/102	Programmable Single Line Module/Adapter for Bell 103 & 202

**Table 4. Interdata 8/32 Megamini: Software**

Package	Description
OS/32 MT	Real-time multiprogramming, multitask operating system, up to 255 priority levels, requires 32-bit Interdata computer, 32KB memory, Operator Console, TTY.
OS/32ST	Serial Task Operating system, upward compatible with OS/32MT, requires 32-bit processor, 32KB memory, Operator Console, TTY.
Fortran V	ANSI 3.9 - 1966 Fortran IV with extensions including ISA calls, requires 32-bit CPU, 8KB above operating system requirements, operator console, TTY.
CAL	Common Assembly language for both 16-bit and 32-bit systems, requires 8KB memory above operating system requirements on 32-bit CPU, console, TTY.
Basic 32	Extended Dartmouth Basic, for single user, requires 32-bit CPU (in 16-bit mode), 10.5KB memory above operating system requirements, Console, TTY.
ITAM	Interdata Telecommunications Access Method requires 65K bytes of memory, DMA, clock, control console, and data set adapter.

The major software packages with configuration requirements are listed in Table 4.

**COMPATIBILITY**

The 8/32 is generally upward compatible with Interdata's 16-bit line at the application program level, given similar configurations. System software cannot be interchanged. Peripheral devices are completely interchangeable; the 8/32 uses a 16-bit I/O bus to maintain compatibility. A 7/32 system can be upgraded in the field to an 8/32.

**MAINTENANCE AND SUPPORT**

Interdata supplies systems on a purchase only basis. Separate maintenance contracts can be negotiated for either on-site engineers (1, 2, or 3 shifts), or for taking replacing damaged boards to a repair depot. Maintenance service can also be obtained on a per-call basis.

Interdata has offices in more than 25 locations in the United States and Canada as well as in Japan, Australia, Great Britain and Germany.

**TYPICAL PRICES**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
	Model 8/32 General Purpose Processor 32-bit fully parallel processor; includes 2 sets of 16 general purpose registers; 1,024 hardware interrupt levels; 16-slot chassis; system cabinet; 2 power supplies; binary display panel; power fail detection/automatic restart; privilege instruction detect, and to 1,024 automatic driver channels; memory access and protect controller; provides for program protection, segmentation registers and current loop interface		
M83-023	Model 8/32 Processor with 131,072 bytes of 750 nsec core memory	51,900	500
M83-101	Processor Options Single precision 32-bit Floating Point Hardware	2,500	20
M83-102	Hexidecimal Display Panel	300	
M83-107	Processor/Memory Parity Generation and Checking Hardware	1,000	
M83-110	Extended Register Sets for 8/32 Processor MEMORIES	5,000	20
M84-300	Memory Expansion from 131,072 to 262,149 bytes	19,000	180
M83-301	M84-300 with parity	20,000	180
M83-302	Memory Expansion from 262,144 to 393,216 bytes	18,500	180
M83-303	M83-302 with parity	19,500	180
M83-304	Memory Expansion from 393,216 to 524,288 bytes	18,000	180
M83-305	M83-304 with parity	19,000	180
M83-306	Memory Expansion from 524,288 to 655,360 bytes	18,500	180
M83-307	M83-306 with parity	19,500	180
M83-308	Additional 131,072 byte memory increments	18,000	180
M83-309	M83-308 with parity	19,000	180
	<b>SYSTEM MODULES</b>		
M48-012	Line Frequency Derived Clock	250	5
M48-000	Universal Clock Module	750	5
M48-001	8-line Interrupt Module	900	5
M48-002	General Purpose Interface Board (15")	550	NA
M48-013	Universal Logic Interface	650	NA
M48-014	Input/Output Bus Switch	1,700	10
M48-107	Extension Cable Kit, 25 feet	175	—
M48-018/019	Manual Control Panel for I/O Bus Switch	200	—
M70-104	Loader Storage Unit Controller	600	10
M70-105	128-byte Storage Module (for use with M70-104)	100	—
M48-005	Multiplexor Bus Buffer DISC	900	5
M46-410	2,5M-byte Removable Cartridge Disc System	10,000	100
M46-414	2,5M-byte Removable Cartridge Disc System	10,100	100
M46-411	2,5M-byte Removable Cartridge Disc Expansion Drive for use with M46-410 or M46-414	5,500	60
M46-420	Removable Cartridge Disc Interface for use up to four 2,5M-byte disc drives	4,000	30
M49-023	Expansion Power Supply for Single Drive Disc	500	—
M49-027	Expansion Power Supply for Single Drive Disc	600	—
27-039	2,5M-byte Removable Cartridge Disc Pack	200	—
M46-416/17	10M-byte Removable Cartridge Disc System	13,100	120
M46-418	10M-byte Removable Cartridge Disc Expansion Drive and Power Supply	8,500	90
M46-419	10M-byte Removable Cartridge Disc Expansion Drive and 50 Hz Power Supply	8,600	90
M46-421	Removable Cartridge Disc Interface	4,500	30
27-056	10M-byte Removable Cartridge Disc Pack	270	—
M46-422	2,500,000 byte Movable Head Fixed Disc System	7,200	100



**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
M46-423	One Drive, 50 Hz version of M46-422	7,300	100
M46-429	40M-byte Removable Cartridge Disc Drive and 1 x 4 Controller	24,950	250
M46-430	40M-byte Removable Cartridge Disc Drive and 1 x 4 Controller	25,100	250
M46-431	40M-byte Removable Cartridge Disc Expansion Drive	17,950	150
M46-432	40M-byte Removable Cartridge Disc Expansion Drive	18,100	150
M46-433	Removable Cartridge Disc Controller	7,000	50
M46-434	40M-byte Removable Cartridge Disc Pack TELETYPE CONSOLES	500	—
M48-010	ASR Model 33/35 TTY Interface with cable	350	5
M46-000	ASR Model 33 Teletypewriter with cable	1,750	40
M46-002	50 Hz version of M46-000	1,850	40
M46-001	ASR Model 35 Teletypewriter with external cable	4,850	40
M46-003	50 Hz version of M46-001 PAPER TAPE EQUIPMENT	4,950	40
M46-250	Combination Paper Tape Reader/Punch Interface with direct connect cable	900	10
M46-240	Paper Tape Reader, uni-directional, 300 cps	1,300	20
M46-241	50 Hz version of M46-240	1,400	20
M46-242	Combination Paper Tape Reader/Punch, 300/75 cps, rack mountable for use with fanfold tape	3,300	40
M46-243	50 Hz version of M46-242 PUNCHED CARD	3,400	40
M46-235	Card Reader Interface with internal cable for 400 cpm or 1000 cpm Card Reader	990	10
M46-234	Hardware Hollerith to ASCII Conversion Option	350	—
M46-230	Card Reader, 400 cpm includes external cable	3,060	40
M46-231	50 Hz version of M46-230	3,160	40
M46-236	Card Reader, 1000-cpm includes external cable	6,500	80
M46-237	50 Hz version of M46-236 PRINTERS	6,600	80
M46-202/206	Line Printer Interface and internal cable	990	10
M46-204	Fully Buffered Line Printer, 60 to 200 lpm, 132 cols, 64 char set, includes external cable	5,000	50
M46-205	50 Hz version, of M46-204	5,200	50
M46-207	Full Buffered Line Printer, 200 lpm, 132 cols, 64 char set, includes external cable	11,950	90
M46-208	50 Hz version, of M46-207	12,250	90
M46-209	Fully Buffered Line Printer, 600 lpm, 132 cols, 64 char set, includes external cable	17,150	110
M46-210	50 Hz version, of M46-209	17,450	110
M46-008	Carousel 15 Keyboard Printer Terminal	1,690	35
M48-023	Carousel 15 Current Loop Interface with internal cable	350	5
M46-845/483	Pedestal mount	175	—
M46-820	Paper Tape Reader for Carousel 15 Printer	375	5
M46-010	Carousel 30 Keyboard Printer Terminal	1,950	35
M48-024	Carousel 30 Current Loop interface with internal cable	400	5
M46-880	132 char Print Line Option for Carousel 30 Terminal	300	—
M46-860	Pin Feed adjustable width forms tractor	150	—
M46-803	Carousel 300 Keyboard Printer Terminal	2,450	35
M46-881	96 Char ASCII Character Set	300	—
M46-887	Electronic Format Control for Carousel 300 Terminal	150	—
M46-400	MAGNETIC TAPE INTERTAPE; Cassette system includes dual transports, 1,000 char per sec read/write speed, hardware read-after-write check, longitudinal redundancy check, 500,000-byte capacity per cassette; includes interface	4,200	30
M46-470	9-Track, 800 bpi, Magnetic Tape Transport Interface	2,900	20
M46-460	9-Track, 800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-461	50 Hz version of M46/960	6,100	90
M46-473/4/8	Magnetic Tape Transport Interface	2,900	20
M46-476	7-Track, 556/800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-477	50 Hz version of M46-476	6,100	90
M46-479/80	7-Track 200/800 cpi, 45 ips Mag Tape Transport	6,000	90
M46-471/2	Magnetic Tape Transport Direct Connect Cable	100	—
M46-475	9-Track, 1600 bpi, Magnetic Tape Transport Interface	1,500	10
M46-465	9-Track, 1600 bpi, 45 ips Magnetic Tape Transport and 1 x 4 Phase Encoded Formatter	12,000	120

Model Number	Description	Purchase Price \$	Monthly Maint. \$
M46-466	50 Hz version of M46-465	12,100	120
M46-467	9-Track, 1600 bpi, 45 ips, Magnetic Tape Expansion Transport	6,800	80
M46-468	50 Hz version of M46-467 VIDEO DISPLAY	6,900	80
M46-107	1200 Baud Local Current Loop Interface with internal cable	400	5
M46-100	Alphanumeric Video Display Unit, 1920-char	2,250	30
M46-101	Std 50 Hz version of M46-100	2,350	30
M46-102	Alphanumeric Video Display Unit, 1920-char complete processor and operator cursor control, editing features, and message and character modes	3,350	40
M46-103	50 Hz version of M46-102	3,450	40
M46-108/109	Graphic Display Terminal, local interface	6,500	60
M46-104/105/106	External cable assembly for connection of local current loop interfaces to Video Display, 25 feet	60	—
M47-000	DATA COMMUNICATIONS SYSTEMS MODULES		
M47-001	Bell 201 Type Data Set Adapter or Equivalent	1,200	10
M47-102	Bell 301 Type Data Set Adapter or Equivalent Programmable Async Single Line Adapter for 103/202 Data Set or local RS-232 terminal; 75 to 9,600 Baud; full or half duplex; RS232C/CCITT interface; switched or private line	450	10
M47-100	Async Line Module Controller	500	10
M47-101	Programmable Async Line Module	1,200	10
M49-021	Programmable Async Line System Chassis	500	—
M10-022	Automatic Dial Unit Controller	1,600	10
M10-054	Data Set Cable, for RS232 compatible data sets	70	—
M10-056	Data Set Cable, for Bell 301 type data sets	350	—
M47-200	IBM 360/370 Parallel Interface	3,500	50
M47-201	IBM 360/370 Parallel Interface; capable of operation in multiplex burst or block multiplex modes	5,000	60
M49-020	CABINETS, CHASSIS, AND POWER SUPPLIES		
M49-024	System Chassis	700	—
M49-026	Power Supply	800	5
M49-003	Bulk Power Supply	1,000	5
M49-004	Adapter Card (10 to 15 in.)	150	—
M49-004	System Cabinet	850	—

\* Quantity discounts are available on most items.  
— Not Applicable

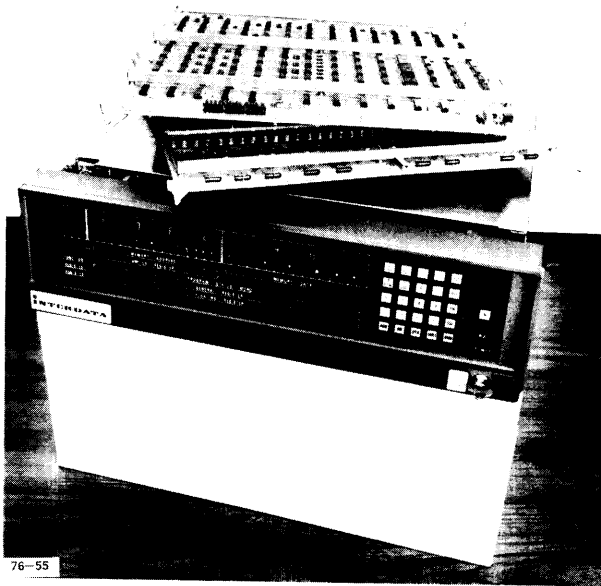
**HEADQUARTERS**

Interdata  
2 Crescent Place  
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(201) 229-4040



## INTERDATA

### Model 6/16 System Report



#### OVERVIEW

The new Model 6/16 offers more for less. It extends Interdata's 16-bit line of compatible computers downward in price, but not performance, making them more competitive to entry-level users as well as to OEM customers. This low end of the minicomputer market is important to manufacturers because users of small computer systems generally add on or upgrade in-line to the next larger system. OEMers also like to use compatible computers. Minicomputer manufacturers have found their best customers are their own customers. Thus, getting customers at the low end of a computer line means more customers at the top end.

Interdata tests indicate the Model 6/16 core version, executing a mix of instructions for general computation, is 30 percent faster than the Model 7/16. The increased speed can be partially explained by the multiply/divide times, which are one-fourth the Model 7/16 times. The Model 6/16 MOS version will be even faster because it uses a faster memory.

First deliveries of the Model 6/16 are scheduled for the first quarter of 1976.

#### Mainframe

The Model 6/16 processor is totally I/O and program compatible with the Model 7/16. It can be upgraded to a Model 7/32 via the Stretch/32 option. Both the 6/16 and 7/16 implement the basic 104 instructions, which include only arithmetic add and subtract in fixed-point, single-precision format. The optional hardware multiply and divide adds six instructions. A bipolar ROM with 60-nanosecond access time stores the CPU firmware. CPU logic is implemented using T<sup>2</sup>L (transistor-to-transistor) MSI (Medium Scale Integration) technology.

The 6/16 uses the same four instruction formats of the rest of the 16-bit line: Register-to-Register (RR), Short Format (SF for single-register operations), register-to-indexed memory (RX), and register immediate (RS). The RR and SF formats use one-word instructions. The RX and RS formats use two-word instructions. All instructions that pull an operand from memory can address up to 64K bytes directly. Addresses can be indexed by the contents of one index register.

The central processor has 16 general purpose registers. All 16 can be used as accumulators and 15 can be used as index registers. Up to 255 interrupt levels can be implemented. Interrupt response time is 7.75 microseconds. Memory for the Model 6/16 is on one board. It can be a core memory with a 1-microsecond cycle time or n-channel MOS memory with a 500-nanosecond cycle time. Core memory boards with 8K, 16K, 32K, and 64K bytes of storage are available. The MOS memory boards are available in 8K-byte increments beginning with 8K bytes up to the maximum capacity of 64K bytes. All memory modules have a single port of entry. Memory parity is optional.

#### HEADQUARTERS

Interdata  
Subsidiary of Perkin-Elmer  
Oceanport NJ 07757  
(201) 229-4040

## Input/Output

The Model 6/16 has the same I/O structure as the rest of the Interdata 16-bit line. DMA is standard, but devices interface to DMA via a standard multiplexor channel or optional selector channels. Up to four DMA channels can be implemented. The multiplexor and selector channels use one DMA channel. The other three DMA channels are available for user-designed interfaces to high-speed devices. Up to 255 devices can be connected to one 6/16 system. Maximum transfer rate over DMA is 2M bytes/second.

## Packaging

The Model 6/16 is available in three combinations of chassis and power supply.

- Chassis with eight slots and 25 amp power supply: CPU and memory use one slot each; thus six slots are available for peripheral controllers and options.
- Chassis with eight slots and 50 amp power supply: CPU and memory use one slot each; thus six slots are available for peripheral controllers and options.
- Chassis with 16 slots and 50 amp power supply: CPU and memory use one slot each; thus 14 slots are available for peripheral controllers and options.

## Peripherals

All the input/output devices available for the rest of the Interdata 16-bit line of computers are available for the Model 6/16. They include a broad range of printers, discs, magnetic tape units, and terminals.

## Optional Features

Optional features include power fail/auto restart, binary or hexadecimal display panel, turnkey console, automatic loader, multiply/divide, selector channel, and Stretch/32.

## Software

Software for the Model 6/16 is the same as that available for the 7/16. Software is unbundled and is available for a one-time license fee.

The major operating system is the OS16MT2, a real-time-based multitasking, multiprogramming operating system. It offers a subset of the features available in the OS32MT for the 32-bit processors.

Two FORTRAN compilers are available: one is extended FORTRAN IV and the other is FORTRAN V, an optimizing compiler.

The assembler language is Common Assembly Language (CAL) for all Interdata processors.

A BASIC Interpreter, which implements a superset of Dartmouth BASIC, is also available.

Interactive debug and operating system edit routines are available for program preparation.

## Competitive Position

The Model 6/16 is a must system for Interdata, a major contender in the minicomputer field. All major minicomputer manufacturers must offer a competitively priced system for entry-level users and OEMs. The system must be an entry into a compatible line that has substantial software and flexible configuration possibilities. Peripherals must include small-, medium-, and large-capacity discs, a variety of printers, and data communications interfaces as well as other conventional peripherals. A small entry-level system nested in this surrounding gives the customer something unavailable with all microcomputer systems except perhaps Digital's LSI-11. Interdata carries its supporting environment farther than most other minicomputer manufacturers. Interdata's small 16-bit computers can even be upgraded to its 32-bit Megaminis without too much trauma via a Stretch/32 option.

Table 1 compares the characteristics of the Model 6/16 with Interdata's former entry-level system, the Model 7/16. Model 6/16 is considerably faster and costs about 40 percent less than the Model 7/16.

**Table 1. Interdata 6/16: Mainframe Characteristics Compared to Model 7/16**

Processor Characteristics	Model 6/16	Model 7/16
<b>CENTRAL PROCESSOR</b>		
Type	Micropgm	Micropgm
No. of Internal Registers	16	16
Use	Accumulators: 15 index regs	Accumulators: 15 index regs
<b>Addressing</b>		
Direct (no. of words)	32K	32K
Indirect	No	No
Indexed	Yes	Yes
Max. I/O devices	255	255
<b>Instructions</b>		
Implementation	Firmware	Firmware
Number	104	104-125
<b>Execution Times, <math>\mu</math>sec</b>		
Fixed-Point Arithmetic		
Add/Subtract	3.00	3.25
Multiply	10.8*	42.00*
Divide	14.5*	56.00*
Floating-Point Arithmetic**		
Add/Subtract	—	31
Multiply	—	44
Divide	—	69
User Microprogramming	No	No
<b>Priority Interrupt System</b>		
Lines		
Internal	1 std	1 std
External Levels	255	255



**Table 1. (Contd.)**

Processor Characteristics	Model 6/16	Model 7/16
<b>Memory</b>		
Type	Core/MOS	Core
Word Length (bits)	16	16
Cycle Time/Wd ( $\mu$ sec)	1.0/0.5	0.75/1.0
Capacity (words)		
Max	32K	32,768
Min	4K	4,096
Increment	8K/16K/32K	4K, 8K, 16K
Parity	Opt: 1bit/wd	Opt
Protect	Opt	Opt
ROM use	Implement	Implement
Writable Control Store	processor logic	processor logic
<b>I/O Channels</b>	No	No
Programmed I/O	Std	Std
Direct Memory Access	Std	Std
No. of Channels	4	4
Selector Channel	Opt	Opt
No. of Devices Handled	16	16
Multiplexed Channel	Std, 255 devices	Std
<b>Maximum Transfer Rate (words/sec)</b>		
DMA via Selector Channel	1M	1M
PRICE of CPU & 32K-byte memory, \$	\$4,800 /4,000	6,800 /6,300

\* Using RX format and optional hardware.  
\*\* To be announced later.

Table 2 compares the Model 6/16 with comparable systems from other manufacturers: Data General's Nova 3, Digital's PDP-11/04, and the General Automation GA-16/330. The Nova 3 is faster than the Model 6/16 and less expensive for the comparable configurations shown in the Table. The Nova 3 price is for a four-slot chassis, which has space for the processor, up to 32K words of memory, and one peripheral.

Prices for the 32K-byte and 56K-byte PDP-11/04 have not yet been announced. The Model 6/16 is faster than the General Automation GA-16/330 and also less expensive.

So far, Interdata has not announced a floating-point processor for the Model 6/16, although one is promised.

Interdata continues to add to its software as well as to its hardware offerings. The Model 6/16 is another indication that Interdata's 16-bit line is not being neglected for the more glamorous Megamini line.

**Table 2. Interdata Model 6/16 Compared with Major Competitors**

	Interdata Model 6/16	Data General Nova 3	Digital PDP-11/04	General Automation GA-16/330
Word Length, bits	16/16 + 1 parity	16/16 + 2 parity	16	16/16 + 2 parity
Inst. Times, $\mu$ sec				
Add	3.00	1.8	3.2	4.6
Multiply	10.8*	6.9 <sup>1</sup>	NA	21.2
Divide	14.5*	7.5 <sup>1</sup>	NA	20.3
FI.P. Add	(2)	7.7*	—	*
FI.P. Multiply	(2)	11.3*	—	*
FI.P. Divide	(2)	13.7*	—	*
Max Memory, bytes	64K	64K/256K	56K	128K
No. of GP Registers	16	4	8	16
Max DMA Rate, bytes/sec	2M	2M	2.8M	2M
Price, \$				
CPU + Memory				
32K bytes	4,800/4,000	4,400 <sup>3</sup>	(4)	5,250
64K bytes	8,200/7,700	7,100 <sup>3</sup>	(4)	8,250
256K bytes	—	34,200	—	—

\* Optional, at extra cost.  
NA Not available.  
— Not applicable.

Notes:

- (1) Operands are unsigned integers on std.
- (2) To be announced.
- (3) Nova 3/4 in 4-slot chassis.
- (4) Digital has not announced price of unbundled memory although the 11/04 can support 56K bytes. Price for 16K-byte system with 9-slot chassis is \$3545.

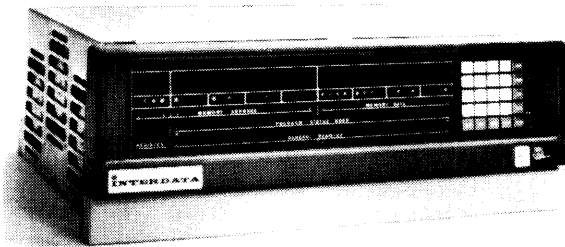
# INTERDATA — MODEL 6/16 SYSTEM REPORT

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## PRICE DATA

	Purchase Price \$
<b>Central Processor and Working Storage</b>	
<b>Equipment</b>	
Model 6/16 CPU in 8-slot chassis, 20 amp power supply, and memory	
<b>With Core</b>	
8K Bytes	2,800
16K Bytes	3,300
32K Bytes	4,800
64K Bytes	8,200
<b>With MOS</b>	
8K Bytes	2,200
16K Bytes	2,800
24K Bytes	3,700
32K Bytes	4,000
40K Bytes	4,600
48K Bytes	5,500
56K Bytes	6,600
64K Bytes	7,700
Substituting 50 amp for 20 amp power supply	500 - 900 (depending on configuration)
Substituting 50 amp for 20 amp power supply and 16-slot for 8-slot chassis	1,000 - 1,300 (depending on configuration)
<b>Optional Features</b>	
Memory Parity Logic	500
Power Fail/Auto Restart	400
Binary Display Panel with Hexadecimal Input Keyboard	300
Hexadecimal Display Panel and Keyboard	600
Display Interface for Binary Display, Hexadecimal Display, or Turnkey Console	100
Turnkey Console for power initialize, and execute	100
Automatic Loader for OS/16 MT2 Loader or Custom-designed Loader	300
Signed Multiply/Divide for 16-bit operands	950
Selector Channel	1,000
Stretch/32 Field Upgrade to software and I/O-Compatible 7/32	5,000
<b>Software</b>	
OS/16 MT2	1,400
MACRO CAL	300
BASIC/16	300
FORTTRAN IV	250
FORTTRAN V	500
ITAM/16	1,200

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75-16

## OVERVIEW

Interdata's line of microprogrammed 16-bit computers consists of the Models 70, 74, 80, and 85, the so-called "New Series" (a set of compatible general-purpose systems), and the 7/16, a newer, lower cost 16-bit word system that will eventually replace all the New Series models; the only models currently marketed are Models 70 and 7/16. The Models 50, 55, 60, 270X, and MS-5 are communications systems that have special instruction sets implemented on a Model 70 processor. The 7/16 system can be expanded in the field to the 7/32, the bottom of Interdata's new, developing 32-bit line for large mini and "megamini" systems. The recently announced Model 8/32 is the powerful top banana of the Interdata computer line.

The original Model 70, introduced in September 1971 and first installed in October of the same year, was quickly followed (in December 1971) by the faster, more powerful Model 80 with all MOS memory. Model 74, the smallest member of the New Series and aimed toward the OEM market, was introduced in July 1972. March 1973 brought announcement of the Model 85 as the most advanced processor in the Interdata 16-bit family. In fact, writable control store is featured as the major difference between Model 85 and the earlier Model 80. First delivery of the Model 85 was in June 1973. Meanwhile, the reconfigured Model 74, using a 16K-byte core memory board, was announced in June 1973 and delivered in the third quarter 1973. In September 1973, Interdata introduced the first member of its new 32-bit line, together with the 7/16, a new entry-level system, which also has a new CPU that can maintain compatibility with the other 16-bit models and expand to the 7/32 in the field via a special "stretch 32" option. The 7/32 performs operations on 32-bit operands but uses a 16-bit wide internal bus and I/O bus. The 8/32, on the other hand, uses a 32-bit wide internal bus and a 16-bit wide I/O bus. The 7/16, 7/32, and 8/32 all use the same core memory modules. Two modules operate in tandem for the 8/32 to accommodate 32-bit words.

These computers are general-purpose systems designed for stand-alone processing, control, data acquisition, and data communications applications. All use a 16-bit word. Core storage modules are used for main memory in Models 70, 7/16, and 74; MOS modules are used in

Models 80 and 85. All models are built around a read-only memory (ROM) control store that holds the microinstructions used to implement the instruction set. All models use preloaded ROM modules. In addition, Model 85 has a writable control store module that can be microprogrammed by the user; Interdata calls this a "dynamic" control store.

The interrupt handling facilities make all of the Interdata computers unusually good for data communications and control applications. Interdata markets special programmable data communications configurations of Model 70 (called Models 50, 55, 60, 270X, and MS-5) with data communications instruction sets. Model 50 uses a single Model 70 processor with an instruction set oriented toward data communications. Model 55 is a dual-processor configuration consisting of a Model 50 and a Model 70. Model 60 is like the 50, but based on the higher-speed Model 80 processor with MOS memory. Model 270X is a plug-compatible front end for an IBM System/360 or 370; it replaces the IBM 2702 and 2703 control units. The MS-5 is a turnkey store-and-forward message switching system using Model 50.

Software for the line includes packages for small stand-alone systems and for systems using the BOSS (Batch Operating System), RTOS (Real-Time Operating System), OS/16 MT (OS/16 Multi-Task Operating System), or DOS (Disc Operating System). The systems support assemblers, BASIC, and several versions of FORTRAN. A compact telecommunications executive called RTEX is available for Models 50 and 60.

This report deals mainly with the general-purpose models, but remarks on the 50, 55, 60, MS-5, and 270X are included to give an overview of these systems. See Table 1 for system specifications.

## Competitive Position

Interdata early recognized the advantage of using firmware — microprogrammed ROM — to implement processor logic, and all of the firm's computers have been built using it. Initially, the instruction execution times for Interdata's computers were slow because each instruction required the execution of several microinstructions. On the other hand, much of the I/O processing and interrupt handling were automatic, and Interdata computers gained a well-deserved reputation for good I/O and interrupt facilities. As ROM modules have become faster, other manufacturers have switched to microprogrammed logic. Now the instruction execution times for Interdata computers are fully competitive with those of other computers.

Model 70 has been the mainstay of Interdata's line, competing with such systems as the Digital PDP-11/40, Data General Nova/Supernova, and Hewlett-Packard 2100S. Model 74, a stripped-down version of the 70, was designed primarily for the OEM market and competed with the PDP-11/05, Nova 1210, and HP 2100A. Model

Table 1. Interdata 16-Bit Models: Mainframe Characteristics

Processor Characteristics	Model Numbers				
	70	74	80	85	7/16
<b>CENTRAL PROCESSOR</b>					
Type	Micropro-grammed	Micropro-grammed	Micropro-grammed	Micropro-grammed	Micropro-grammed
No. of Internal Registers	16	16	16	16	16
Use	Accumulators: 15 index regs	Accumulators: 15 index regs	Accumulators: 15 index regs	Accumulators: 15 index regs	Accumulators: 15 index regs
<b>Addressing</b>					
Direct (no. of words)	32,768	32,768	32,768	32,768	32,768
Indirect	No	No	No	No	No
Indexed	Yes	Yes	Yes	Yes	Yes (1 level)
Max I/O devices	255	255	255	255	255
<b>Instructions</b>					
Implementation	Firmware	Firmware	Firmware	Firmware	Firmware
Number	113	110	127	131	104-125
<b>Fixed-Point Arithmetic</b>					
Add/subtract	Hardware	Hardware	Hardware	Hardware	Hardware opt
Multiply/divide	Hardware	Hardware	Hardware	Hardware	Hardware opt
Add time ( $\mu$ sec)	1.0 (reg-to-reg)	1.5 (reg-to-reg)	0.53 (reg-to-reg)	0.53 (reg-to-reg)	1.5; 1.0
Floating-Point Arithmetic	Hardware	Subroutine	Hardware	Hardware	Hardware
User Microprogramming	No	No	No	Yes	
<b>Priority Interrupt System</b>					
Lines					
Internal	8, 1**	6	8, 1**	8, 1**	
External	2 gen; 3 dedicated	1 gen; 3 dedicated	1 gen; 3 dedicated	1 gen; 3 dedicated	1 std
Levels	256/gen line	256/gen line	256/gen line	256/gen line	255
<b>Memory</b>					
Type	Core	Core	Semiconductor	Semiconductor	Core
Word length (bits)	16	16	16	16	16
Cycle time/word ( $\mu$ sec)	1.0	1.0	0.270	0.270	0.75; 1.0
Capacity (words)					
Max	32,768	32,768	32,768	32,768	32,768
Min	4K, 8K, 16K	4K, 8K, 16K	8,192	8,192	4,096
Increment	4K, 8K, 16K	4K, 8K, 16K	8K	8K	4K, 8K, 16K
Parity	Opt	Opt	Opt	Opt	Opt
Protect	Opt	NA	Opt	Opt	Opt
ROM use	Implement processor logic	Implement processor logic	Implement processor logic	Implement processor logic	Implement processor logic
Writable Control Store	No	No	No	Yes	No
<b>I/O Channels</b>					
Programmed I/O	Std	Std	Std	Std	Std
Direct memory access	Std	Std	Std	Std	Std
No. of channels	4	1	4	4	4
Selector channel	Opt	Opt	Opt	Opt	Opt
No. of devices handled	16	16	16	16	16
Multiplexed channel	Std	NA	Std	Std	Std
<b>Maximum Transfer Rate</b>					
(words/sec)					
Within memory	273,972	273,972	815,660	815,660	340,300; 273,972
DMA	1,000,000	1,000,000	2,100,000	2,100,000	2,600,000
High-speed DMA	—	—	3,000,000	3,000,000	—

Notes:

\* Integrated parallel double-buffered Teletype adapter included with processor Models 70, 80, 85.

\*\* Optional protect interrupt.



80, over twice as fast as Model 70, competed with the PDP-11/45 and 11/50 and the Supernova SC. Model 85, basically the same as Model 80 but with dynamic control store, competed with other systems that have writable control store, such as the Varian 73, the Microdata 3200, and the HP 2100S. Writable control store is of interest to those who can use it to gain substantial increases in throughput for a particular application.

While Interdata is still marketing these systems, the new "bridge" model, the 7/16, has become the entry level system for 16-bit computers while the company's 32-bit line has taken over the medium range applications, formerly filled by the 80 and 85. What makes the 7/16 attractive to new users is its low cost and its role as a bridge system. It gives present users upward growth possibilities while letting them take advantage of Interdata's present software. The firm supplies a broad range of peripherals for its 16-bit systems plus a reasonable amount of software, four operating systems, FORTRAN IV and BASIC compilers, and data communications line handlers. The RTOS is the major piece of software for process control applications. OS/16 is a compact version used on the 7/16.

Interdata's strongest markets have been in data communications and process control applications. Over 60 percent of its business has been to OEM users, while 40 percent has been to end users.

Up to 255 peripheral devices can interface to the processor via the multiplexor bus. High-speed devices, such as discs, transfer only control information over the multiplexor channel, and use an optional selector channel for transferring data directly to or from memory. The selector channels interface directly to the processor through a DMA port. Although each selector channel can support up to 16 devices, only one device at a time can use the channel. Customer-designed channels can also interface to the DMA ports.

Interdata provides a broad range of peripheral devices for its computers. Conventional devices include Teletype units, alphanumeric video displays, paper tape reader/punch, punched card reader, and line printers. Mass storage devices range from magnetic tape cassette through industry-compatible 9-track magnetic tape drives to drum and disc cartridge units. Interdata also provides many data communications devices as well as A/D and D/A subsystems to connect noncomputer devices.

## Compatibility

Model 74 is the bottom of the line, and Model 70 is upward program compatible with the Model 74. Model 80 is upward program compatible with Model 70. The Model 85 processor logic is identical to that of Model 80, except that Model 85 can use the dynamic control store memory.

All Interdata computers have compatible I/O buses and therefore use the same peripheral devices.

## CONFIGURATION GUIDE

Interdata computers function in stand-alone configurations or as satellite or front-end processors for other systems. The basic central processors of Model 70, 7/16, 80, and 85 include 16 general-purpose registers, high-speed multiply/divide, 32-bit floating-point hardware, a buffer multiplexor channel with up to 255 subchannels, four Direct Memory Access (DMA) ports, a Teletype interface, a vectored hardware priority interrupt system for up to 255 devices, a display panel, a power supply, and 3 or 11 additional slots for memory expansion or I/O options.

Model 74 shares many processor characteristics with Models 70, 80, and 85 but also has the following differences: floating-point arithmetic is handled by subroutines; one DMA port is standard; the Teletype adapter and display panel are not included in the basic system; and five slots are provided for memory expansion or I/O options.

Memory ranges differ for the various Interdata New Series models. Minimum memory size is 4,096 16-bit words for Models 70 and 74, and 8,192 words for Models 80 and 85. Maximum memory size is 32,768 words (65,536 bytes) for all models. The Twin Chassis 70 and the reconfigured 74 use a new memory circuit board that stores 8K words of memory in the same space previously used by 4K words. The Twin Chassis 70 also provides 11 subassembly slots and a more powerful bulk power supply in its twin chassis. Model 85 also supports 1K 32-bit words of control memory that can implement a user-defined instruction set.

The basic Model 7/16, the most recent 16-bit system, includes the central processor, 8K bytes of core memory, power supply, and chassis with eight slots.

Standard options include a 16-slot chassis to configure large systems; 8K-, 16K-, and 32K-byte core memory modules with either a cycle time of 0.75 or 1.0 microsecond; memory parity; power fail detection and automatic restart; memory protect; binary or hexadecimal display panel; automatic loader; turnkey console; signed multiply/divide; high-speed arithmetic (multiply/divide, floating-point arithmetic, list processing and privileged instruction detect); and stretch 32 (converts 7/16 to 7/32 processor).

Table 2 lists the peripherals and Table 3 lists the software available for the Interdata computers.

## MAINTENANCE AND SUPPORT

Interdata supplies systems on a purchase-only basis. Through separate maintenance contracts, users can negotiate for on-site engineers (1, 2, or 3 shifts), or take damaged boards to a repair depot (or have them replaced). Maintenance service is also available on a per-call basis.

Interdata has offices in more than 20 locations in the United States and Canada as well as in Japan, Australia, Great Britain, and Germany.

**Table 2. Interdata 16-Bit Models: Peripherals**

Model No.	Description
<b>Punched Tape</b>	
M46-240	300-cps readers
M46-242/250	300-cps reader, 75-cps punch
<b>Punched Card</b>	
M46-230/236	400/1,000-cps readers
<b>Printers</b>	
M46-204	60-200 lpm, 132 col, 64-char set
M46-207/209	200/600 lpm, 132 col, 64-char set
<b>Terminals</b>	
M46-000/001	ASR 33/35 TTY
M46-100-103	A/N display, 4,920 char, to 9,600 baud
M46-108	Graphic display, to 9600 baud, 1,024 x 1,024 point matrix
<b>Magnetic Tape</b>	
M46-400	Dual-drive cassette, 500K bytes/cassette; 1,000-cps xfer
M46-460	9-trk 800-bpi magnetic tape, 45 ips
M46-465-467	9-trk 1,600-bpi magnetic tape, 45 ips, 4 drives/controller
M46-476	7-trk, 556- or 800-bpi (not both) magnetic tape subsystem, 4 drives/controller
<b>Discs</b>	
M46-410	2.5Mb 5440-type removable cartridge disc, 4 drives/controller
M46-516	10.0Mb fixed/removable 5440-type cartridge disc, 4 drives/controller
M46-429	40.0Mb 2316-type disc pack, 4 drives/controller
<b>Process I/O</b>	
M48 series	Wide-range analog input, up to 512 channels
M48 series	High-speed low-level analog input, up to 64 channels
M48 series	High-level analog I/O, up to 8 differential or 16 single-ended inputs
M48 series	Real-time analog controller, two 32-word solid-state buffer memories
M07/M48	Digital Multiplexor Subsystem, 2,048 input & 2,048 output lines
<b>Communications</b>	
M10-022	Auto dial units, 4-lines
M11-200	IBM 360/370 interface multiplexor (burst or block modes) channel
M47-000/001	Bell-type adapters, 201/301, to 9,600/40,800 baud
M47-100	Async line module controller, up to 92 lines, to 1,800 baud
M47-101/102	Programmable single-line module/adaptor for Bell 103 & 202

**Table 3. Interdata 16-Bit Models: Software**

Package	Description
<b>BOSS PLUS</b>	Batch system for 70, 80, or 85 processor with arithmetic traps for 74 and 7/16; requires 8KB memory, operator console, TTY
<b>DOS PLUS</b>	Disc operating system, core resident or disc resident, for 74 and 7/16; requires 16KB memory, operator console, TTY
<b>RTOS</b>	Multiprogramming multitask real-time operating system for 70, 80, 85, or 7/16 with High-Speed ALU option; requires 24KB memory, operator console, memory protect clock, TTY
<b>OS/16</b>	Compact multiprogramming multitask system, for 70, 74, 80, 85, or 7/16; requires 8KB memory, operator console, power fail/auto restart, clock, TTY
<b>FORTRAN IV</b>	ANSI x3.9-1966 with extensions for BOSS PLUS, DOS PLUS, RTOS, and OS/16 MT; requires 70, 74, 80, 85, or 7/16, 16KB above operating system requirements, operator console, TTY
<b>FORTRAN V</b>	FORTRAN IV (above) but can support ISA calls for any operating system (including 7/32); same requirements as FORTRAN IV
<b>BASIC</b>	Interpreter conforms to Dartmouth conventions, with extensions; single-user version requires any CPU (including 7/32), 10.5KB memory above operating system requirements, console, TTY
<b>MUBS</b>	Multi-User Basic Operating System, self contained for up to 32 users (depending on system memory service); for 70, 74, 80, 85, or 7/16 processor, 16KB memory (4-user level) clock, TTY, console
<b>CAL</b>	Common Assembly Language for both 16- and 32-bit processors; requires 16KB memory above operating system requirements, console, TTY
<b>DCSS</b>	For program debugging microcode on 85's DCS option; requires Model 85, CPU, 16KB memory, TTY



**TYPICAL PRICES**

Model Number	Description	Purchase \$	Monthly Maint \$	Model Number	Description	Purchase \$	Monthly Maint \$
<b>MODEL 7/16 GENERAL-PURPOSE PROCESSOR</b> (includes 16 GP regs, buffered mpx bus, 4 high-speed DMA channels, and 255 hardware vectored interrupt levels; auto-load bootstrap instruction for initial loading)				<b>MODEL 80 AND 85 PROCESSOR OPTIONS (Contd)</b>			
M71-011	8,192 Bytes of Core Memory. (1 µsec, 8-slot chassis and power supply)	3,200	45	M70-105	128-Byte Storage Module	100	—
M71-012	16,384 Bytes of Core Memory. (1 µsec, 8-slot chassis and power supply)	3,700	50	M48-005	Multiplexor Bus Buffer	900	5
M71-013	32,768 Bytes of Core Memory. (1 µsec, 8-slot chassis and power supply)	5,300	60	M80-102	Battery Pack	300	—
M71-014	32,768 Bytes of Core Memory. (750 nsec, 8 slot chassis and power supply)	5,800	65	M80-300	<b>MODEL 80 AND 85 MEMORIES</b> 16,384-Byte Expansion Memory Storage Unit (270-nsec average MOS cycle time)	7,900	40
M71-021	M71-011 with 16-slot chassis	4,200	45	M80-301	Same as M80-300 with parity	8,900	40
M71-022	M71-012 with 16-slot chassis	4,700	55	<b>SYSTEM MODULES</b>			
M71-023	M71-013 with 16-slot chassis	6,300	65	M48-012	Line Frequency Derived Clock	250	5
M71-024	M71-014 with 16-slot chassis	6,800	70	M48-000	Universal Clock Module	600	5
<b>MODEL 7/16 PROCESSOR OPTIONS</b>				M48-001	8-Line Interrupt Module	900	5
M7-100	Turnkey Console	100	—	M48-002	General-Purpose Interface Board (15 inches)	550	NA
M71-103	Automatic Loader	400	2	M48-013	Universal Logic Interface	650	NA
M71-104	Power Fail Detection/Auto Restart	400	2	M48-014	Input/Output Bus Switch	1,500	10
M71-105	Signed Multiply/Divide Hardware	950	5	M48-107	Extension Cable Kit, 25 feet	175	—
M71-106	High-Speed ALU	4,900	20	M48-018/9	Manual Control Panel for I/O Bus Switch	200	—
M71-107	Automatic Memory Protect	1,450	5	<b>DISC</b>			
M71-108	Processor Parity Control	500	—	M46-410	2.5M-Byte Removable Cartridge Disc System	10,000	80
M71-109	Stretch/32 Module	5,000	—	M46-414	2.5M-Byte Removable Cartridge Disc System	10,100	80
M70-103	Selector Channel	1,000	10	M46-411	2.5M-Byte Removable Cartridge Disc Expansion Drive	5,500	50
M71-101	Binary Display Panel	300	2	M46-420	Removable Cartridge Disc Interface (for use with up to four 2.5M-byte Drives)	4,000	30
M71-102	Hexadecimal Display Panel	600	5	M49-023	Expansion Power Supply for Single Drive Disc	500	—
M70-104	Loader Storage Unit Controller	500	10	M49-027	Expansion Power Supply for Single Drive Disc	600	—
M70-105	128-Byte Storage Module	100	—	M46-416	10M-Byte Removable Cartridge Disc System	12,000	120
M48-005	Multiplexor Bus Buffer	900	5	M46-417	10M-Byte Removable Cartridge Disc System	12,100	120
<b>MODEL 7/16 MEMORIES</b>				M46-418	10M-Byte Removable Cartridge Disc Expansion Drive and Power Supply	8,000	90
M71-300	8,192-Byte Memory Expansion Module (1 µsec core cycle time)	2,000	20	M46-418	M46-418 with 50 Hz Power Supply	8,100	90
M71-302	16,384-Byte Memory Expansion Module (1 µsec core cycle time)	2,650	30	M46-421	Removable Cartridge Disc Interface (for use with up to four 10M-byte dual disc drives)	4,000	30
M71-304	32,768-Byte Memory Expansion Module (1 µsec core cycle time)	3,950	40	M46-429	10M-Byte Removable Cartridge Disc Pack	270	—
M71-306	32,768-Byte Memory Expansion Module (750 nsec core cycle time)	4,500	45	M46-429	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	24,950	200
M71-301	M71-300 with parity	2,500	20	M46-430	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	25,100	200
M71-303	M71-302 with parity	3,150	30	M46-431	40M-Byte Removable Cartridge Disc Expansion Drive	17,950	200
M71-305	M71-304 with parity	4,450	40	M46-432	40M-Byte Removable Cartridge Disc Expansion Drive	18,100	200
M71-307	M71-306 with parity	5,000	45	M46-433	Removable Cartridge Disc Controller	7,000	50
<b>MODEL 70 GENERAL-PURPOSE PROCESSOR</b> (includes 16 GP reg, high-speed multi/div, 32-bit floating-point hardware; buffered multiplexor bus with up to 255 auto I/O channels; read/write block, interleaved data channel to memory; 4 cycle-stealing DMA ports; character-buffered teletypewriter interface; hardware interrupt discrimination and vectoring for up to 255 devices; display panel and power supply)				M46-434	40M-Byte Removable Cartridge Disc Pack	500	—
M70-000	Model 70 Processor (8,192-byte 1,000-nsec core memory and 8 slot chassis)	6,800	60	<b>TELETYPE CONSOLES</b>			
M70-002	Model 70 Processor (16,384-byte 1,000-nsec core memory and 16 slot chassis)	9,200	80	M48-010	ASR Model 33/35 TTY Interface (with internal cable)	350	5
M70-004	Model 70 Processor (32,768-byte 1,000-nsec core memory and 16 slot chassis)	10,900	90	M46-000	ASR Model 33 Teletypewriter (with external cable)	1,450	40
M70-001	Same as M70-000 with parity	7,800	60	M46-002	50-Hz Version of M46-000	1,550	40
M70-003	Same as M70-002 with parity	10,200	80	M46-001	ASR Model 35 Teletypewriter (with external cable)	4,200	40
M70-005	Same as M70-004 with parity	11,900	90	M46-003	50-Hz Version of M46-001	4,300	40
<b>MODEL 70 PROCESSOR OPTIONS</b>				<b>PAPER TAPE EQUIPMENT</b>			
M70-100	Power Fail Protection/Auto Restart	200	2	M46-250	Combination Paper Tape Reader/Punch Interface (with direct connect cable)	900	10
M70-101	Automatic Memory Protect	2,900	5	M46-240	Paper Tape Reader, Uni-directional (300 cps)	1,300	20
M70-103	Selector Channel (provides true cycle-stealing to memory for 8- or 16-bit transfers at rates up to 2M bytes/sec)	1,000	10	M46-241	50-Hz Version of M46-240	1,400	20
M70-104	Loader Storage Unit Controller	500	10	M46-242	Combination Paper Tape Reader/Punch (300/75 cps, rack mountable for use with fanfold tape)	3,300	40
M70-105	128-Byte Storage Module	100	**	M46-243	50-Hz Version of M46-242	3,400	40
M48-005	Multiplexor Bus Buffer	900	5	<b>PUNCHED CARD</b>			
<b>MODEL 70 MEMORIES</b>				M46-235	Card Reader Interface (with internal cable for 400 cpm or 1,000 cpm card reader)	900	10
M70-300	8,192-Byte Memory Expansion Module (1,000 nsec core cycle time)	2,700	20	M46-234	Hardware Hollerith to ASCII Conversion Option for Card Reader Interface	350	—
M70-302	16,384-Byte Memory Expansion Module (1,000-nsec core cycle time)	4,300	30	M46-230	Card Reader, (400 cpm includes external cable)	3,000	40
M70-304	32,768-Byte Memory Expansion Module (1.0- sec core cycle time)	5,000	40	M46-231	50-Hz Version of M46-230	3,100	40
M70-301	M70-300 with parity	3,200	20	M46-236	Card Reader, (1,000 cpm; includes external cable)	5,000	80
M70-303	M70-302 with parity	4,800	30	M46-237	50-Hz Version of M46-236	6,000	80
M70-305	M70-304 with parity	5,500	40	<b>PRINTERS</b>			
<b>MODEL 80 GENERAL-PURPOSE PROCESSOR</b> (Model 70 processor with 3 additional slots for expansion memory storage units or I/O options; includes M49-022 power supply for processor and I/O; memory fully powered for up to 64K bytes)				M46-202	Line Printer Interface (and internal cable for 60 to 200 lpm line printer)	500	10
M80-000	Model 80 Processor (16,384-byte MOS memory; average access time 270 nsec, and 8-slot chassis)	14,900	150	M46-204	Fully Buffered Line Printer, (60 to 200 lpm, 132 columns, 64 char set; includes external cable)	5,000	50
M80-001	Same as M80-000 with parity	16,400	150	M46-205	50-Hz Version of M46-204	5,200	50
<b>MODEL 85 GENERAL-PURPOSE PROCESSOR</b> (same as Model 80 but with 4,192-byte dynamic control store)				M46-206	Line Printer Interface (and internal cable for 200 or 600 lpm line printer)	750	10
M85-000	Model 85 Processor (16,384 byte MOS memory, average access time 270 nsec; 4,192-byte Bipolar Dynamic Control Store, 1,024 x 32 bits, and 8-slot chassis)	22,800	175	M46-207	Full Buffered Line Printer, (200 lpm, 132 cols, 64 char set; includes external cable)	12,350	90
M85-001	Same as M85-000 with parity	24,300	175	M46-208	50-Hz Version of M46-207	12,650	90
<b>MODEL 80 AND 85 PROCESSOR OPTIONS</b>				M46-209	Fully Buffered Line Printer, (600 lpm, 132 cols, 64 char set; includes external cable)	17,150	110
M80-100	Power Fail Protection/Auto Restart	350	2	M46-210	50-Hz Version of M46-209	17,450	110
M80-101	Automatic Memory Protect	2,900	5	<b>MAGNETIC TAPE</b>			
M70-103	Selector Channel (provides true cycle stealing to memory for 8- or 16-bit transfers at rates up to 3.15M bytes/sec)	1,000	10	M46-400	INTERTAPE (cassette system with dual transports, 1,000 char per/sec read/write speed, hardware read-after-write check, longitudinal redundancy check, 500,000-byte capacity per cassette; includes interface)	4,200	30
M70-104	Loader Storage Unit Controller	500	10	M46-470	9-Track, 800 bpi, Magnetic Tape Transport Interface	2,900	20
				M46-460	9-Track, 800 bpi, 45 ips Magnetic Tape Expansion Transport, (continuous transfer rate is 36,000 char/sec)	6,000	90
				M46-461	50-Hz Version of M46-460	6,100	90
				M46-473	7-Track, 556 bpi Magnetic Tape Transport Interface.	2,900	20
				M46-474	7-Track, 800 bpi Magnetic Tape Transport Interface.	2,900	20
				M46-476	7-Track, 556/800 bpi, 45 ips Magnetic Tape Expansion Transport, (continuous transfer rate is either 25,320 or 36,000 char/sec)	6,000	90
				M46-477	50-Hz Version of M46-476	6,100	90
				M46-471/2	Magnetic Tape Transport Direct Connect Cable	100	—
				M46-475	9-Track, 1600 bpi, Magnetic Tape Transport Interface (controls up to 4 IBM compatible, continuous read-after-write 45 ips drives via a phase-encoded formatter supplied with M46-465 or M46-466)	1,500	10



## INTERDATA — 16-BIT MODELS

### TYPICAL PRICES (Contd.)

Model Number	Description	Purchase \$	Monthly Maint \$
	<b>MAGNETIC TAPE (Contd)</b>		
M46-465	9-Track, 1600 bpi, 45 ips Magnetic Tape Transport and 1 x 4 Phase Encoded Formatter (continuous transfer rate is 72,000 char/sec)	12,000	120
M46-466	50-Hz Version of M46-465	12,100	120
M46-467	9-Track, 1,600 bpi, 45 ips, Magnetic Tape Expansion Transport (for use with M46-475 and M46-465)	6,800	80
46-468	50-Hz Version of M46-467	6,900	80
	<b>VIDEO DISPLAY</b>		
M46-107	1,200 Baud Local Current Loop Interface (with internal cable)	400	5
M46-100	Alphanumeric Video Display Unit (1,920 char (24 lines x 80 char); std 64-char ASCII subset; 110 or 1,200 baud via current loop interface; up to 9,600 baud with RS-232C)	2,250	30
M46-101	Std 50-Hz Version of M46-100	2,350	30
M46-102	M46-100 with processor and operator cursor control, a full range of editing features, and message and character modes. 110 to 9,600 baud with RS-232C connection	3,350	40
M46-103	50-Hz Version of M46-102	3,450	40
M46-108	Graphic Display Terminal	6,500	60
M46-109	50-Hz Version of M46-108	6,500	60
M46-104/5/6	External Cable Assembly	50	-
	<b>DATA COMMUNICATIONS SYSTEMS MODULES</b>		
M47-000	Bell 201 Type Data Set Adapter or Equivalent	1,200	10
M47-001	Bell 301 Type Data Set Adapter or Equivalent	1,400	10
M47-102	Programmable Async Single Line Adapter (for 103/202 data set or local RS-232 terminal)	400	5
M47-100	Async Line Module Controller	500	10
M47-101	Programmable Async Line Module	1,200	10
M49-021	Programmable Async Line System Chassis	550	-
M10-022	Automatic Dial Unit Controller	1,600	10
M10-054	Data Set Cable (for RS232 compatible data sets)	60	-
M10-056	Data Set Cable (for Bell 301 type data sets)	350	-
M47-200	IBM 360/370 Parallel Interface (single address interface)	3,500	50
M47-201	IBM 360/370 Parallel Interface	5,000	60
	<b>CABINETS, CHASSIS, AND POWER SUPPLIES</b>		
M49-020	System Chassis	700	-
M49-024	Power Supply	800	5
M49-026	Bulk Power Supply	1,000	5
M49-003	Adapter Card (10 inches to 15 inches)	150	-
M49-004	System Cabinet	650	-

Not Applicable

\* Quantity discounts are available on most items.

\*\* Additional Software Documentation Packages available.

### HEADQUARTERS

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**New Computer Systems**

Interdata Corporation has announced two new 16-bit computer systems called the RD800 and RD850 for scientific processing applications; they are based on the firm's Model 80 and 85 computers. Both systems include a central processor with 32K, 48K or 64K bytes of MOS memory, floating point hardware, power fail protect, display terminal and 2.5 bytes of disc storage with interfaces. Standard software includes assembly language, FORTRAN IV, BASIC and disc operating system.

The RD850 system includes 4K words of Dynamic Control Store, Interdata's writable control store module that can be microprogrammed by the user. Both systems feature an average memory cycle time of 270 nanoseconds, 16 general purpose registers (including 15 that can be used as index registers), multiply/divide, floating point arithmetic, and 255 vectored interrupt levels.

Interdata is aiming RD systems at the scientific market; they are well-suited for use in university research, as well as in petrochemical, aerospace and simulation applications and in situations that require high-speed numerical analysis. The RD850, with the Dynamic Control Store module that has a cycle time of 60 nanoseconds, can include user-alterable microprogramming in situations requiring high-speed, specially-designed algorithms.

The operating system features disc file structures supporting named access, blocking and de-blocking of input/output, and read/write access protection. Files can be random, sequential and direct physical access types. Catalog procedures can be stored on any device to facilitate batch processing.

The systems are priced from \$32,400 for a complete RD800 system with 32K bytes of memory, to \$42,525 installed with 6 months maintenance. They are available for immediate delivery.

**New Disc Drive**

Interdata also has introduced a 2.5 megabyte fixed disc drive system that will be available in July. The system is designed for low cost random access bulk storage and includes the drive mechanism, controller, power supply and IBM 2315 disc or equivalent. The disc controller interfaces to all Interdata 16-bit and 32-bit processors.

Average access time of the disc drive is 70 milliseconds, and the track-to-track access time is 15 milliseconds. The nominal data transfer rate is 195K characters per second. The controller can cross sector and head boundaries, thus data can be transferred in block sizes from 156 bytes to 12,288 bytes.

The controller operates with a selector channel for autonomous block transfers. It permits simultaneous seek, overlapping seek and data transfers in multiple disc drive configurations to minimize access time. Hardware error checking is also included.

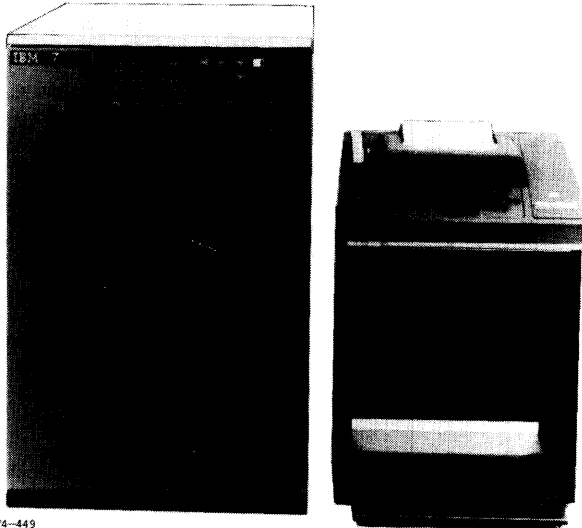
The disc contains a single platter recorded at 2,200 bits per inch on 203 tracks on each surface. Data on each track is divided into 24 equal sectors, which include four main fields — sync, two-byte header, and 256-byte and 16-bit cyclic check fields.

Purchase price of the new disc system is \$7,200 for single units, or \$6,192 in quantities of 10 to 14.



# IBM CORP.

## System/7 System Report



### OVERVIEW

IBM's System/7 is a small processor designed to excel in real-time data acquisition, laboratory automation, process control, and data communications applications. It is designed to operate as a small, stand-alone system for sensor-based applications or as a front-end to a host computer.

IBM offers A, B, and E Series of System/7 processor models. The A and B Series are identical in almost all respects; their memory capacity is the same, but they differ in their ability to function as front-end processors with other IBM computers. Model Bxx (xx is memory size) interfaces directly with the IBM 1130 computer; Model Axx communicates with the IBM 1800, System/360, or System/370 computers via an asynchronous or bisynchronous communications interface. Model Axx can also operate as a stand-alone system. Model Exx is most like Model Axx, but its memory capacity is much larger. Model Exx supports both synchronous and asynchronous data communications. It also has seven additional instructions in its instruction set and has memory protection facilities. Memory protection, however, is not supported by system software.

Main storage is monolithic; capacity ranges from 2K to 16K 18-bit words (one parity bit for each eight-bit byte) for Axx and Bxx models and from 16K to 64K words for Exx models. Memory cycle time is 400 nanoseconds per word. Standard peripheral equipment support for the System/7 includes an operator station with keyboard, printers, and paper tape input/output; communication interfaces; a wide variety of analog/digital and

digital/analog equipment; sensing devices; and disc storage. Disc storage can consist of up to eight 5022 cartridge discs (fixed or removable versions) with a 1.2M or 2.4M-byte capacity and/or the 3340/3348 disc subsystem, an extremely fast high-capacity system that can store up to 34.2M bytes per drive and 273.6M bytes per eight-spindle subsystem. Thus, a maximum of 292.8M bytes of disc storage can be attached to a System/7. Moreover, the 3340/3348 can operate in a 5022 emulation mode for program compatibility or greater flexibility in access methods. A fixed-head option (0.480M bytes per spindle) is available, but the rotational position option sensing is not software supported.

Software for the System/7 allows it to function as a memory-based or disc-based stand-alone process control or DDC system, a front end for the 360/370, 1130, or 1800, a message-switching system, or a member of a distributed processing network. The MSP/7 software has to be expanded to provide a multiprogramming foreground/background system. The software combined with the addition of 3340 disc subsystems increases the flexibility of the System/7 and strengthens its competitive stance. The Executive Feature MSP/7 provides for up to 16 partitions for real-time multiprogramming. One partition can be used for on-line batch processing program preparation, various service routines, or user batch programs.

A number of custom products and features are also available for specific applications, such as for inquiry/response or data communications systems.

The System/7 central processor features two interval timers, four processing levels with 16 sublevels each, an adapter for the 5028 Operator Station, seven index registers, one program counter, and one accumulator. Each processing level has power-failure detection with automatic Initial Program Load (IPL). Internal air isolation allows use of the system in hostile environments. Switching time from one level to another is 800 nanoseconds.

The air isolation feature protects System/7 from atmospheric contaminants that may be present in industrial

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or laboratory environments. Internal air is recirculated through activated charcoal filters to absorb contaminants, and internal heat is dissipated via an air-to-air heat exchange that is part of the feature.

System/7 is designed to operate under severe physical conditions: temperature ranges from 40 to 120 degrees Fahrenheit and relative humidity ranges from eight to 85 percent are tolerable during operation. Thermal warning sensors sound an alarm when the temperature exceeds normal operating limits; and thermal shutdown occurs if component damage is imminent.

This rather impressive set of features and selected peripherals allows System/7 to compete in many application areas: data acquisition, process control, plant automation, and data communications. Table 1 lists the System/7 mainframe characteristics.

IBM announced System/7 A and B Series on October 28, 1970. First deliveries were made in the last quarter of 1971. The E Series was announced in July 1973 and first delivered in December 1973. The 3340/3348 disc subsystems, which are standard RPQ items, are scheduled for delivery in May 1976.

## COMPETITIVE POSITION

IBM is naturally in a strong competitive position with respect to other vendors of front-end processors for its 1130, 1800, System/360, and System/370. Many corporations prefer one major supplier because equipment-related problems become the supplier's responsibility. IBM caters to this preference by offering user training and technical expertise in application areas.

Many corporations in the industrial community also understand the advantages of multiple suppliers and the need to practice economy in data processing operations. Most minicomputers can communicate with large IBM systems via binary synchronous communications facilities. Under these constraints, System/7 must prove its worth.

Initially, the System/7 had extremely limited expansion capability in comparison to other minicomputers, not only in peripherals but in main memory capacity, which was only 16K words. The E Series quadrupled maximum memory capacity from 16K to 64K words and offered memory protection. IBM has also expanded the standard

**Table 1. IBM System/7: Mainframe Characteristics**

Characteristic	5010 Model A	5010 Model B	5010 Model E
<b>Announced</b>	October 1970	October 1970	July 1973
<b>Memory</b>			
Type	Monolithic SS	Monolithic SS	Monolithic SS
Word Length (bits)	16	16	16
Cycle Time/wd (nsec)	400	400	400
Capacity (wds)			
Min	2048	2048	16,384
Max	16,384	16,384	65,536
Increment Size	2048	2048	4096
Parity	1 bit/byte	1 bit/byte	1 bit/byte
Protect	None	None	Yes <sup>(1)</sup>
<b>Central Processor</b>			
No. of Internal Registers	4 sets of 9	4 sets of 9	4 sets of 9
No. of Instructions			
Std	39	39	46
Opt	—	—	—
<b>Addressing</b>			
Direct (no. of wds)	Short: 255 Long: 16,384	Short: 255 Long: 16,384	Short: 255 Long: 16,384
Indirect	None	None	None
Indexed	Yes	Yes	Yes
<b>Priority Interrupt System</b>			
Lines	4	4	4
Levels	16/line	16/line	16/line
<b>I/O Channels</b>			
Programmed I/O	Yes	Yes	Yes
Direct Memory Access (DMA)			
No. of Channels	1	1(2)	1
Multiplexed I/O			
No. of Subchannels	—	—	—
<b>Max Transfer Rate (wds/sec)</b>			
Within Memory	625,000	625,000	625,000
Over DMA	250,000	250,000	250,000

**Notes:**

(1) Memory protect supported by Executive/7 System software only.

(2) The 1130 attachment provides direct memory access but does not provide block transfer of data.



peripherals to include interactive consoles, card equipment, greatly increased disc storage, and serial as well as line printers, all software-supported.

The System/7 is a well-designed system and features an advanced logical and technological architecture. It uses all semiconductor solid state memory with a 400-nanosecond cycle time. The processor always operates in one of four priority interrupt levels, and it can switch from one interrupt level to another in 800 nanoseconds. Each level has its own set of internal registers, and processing at the new level can begin immediately, once the context is switched. Its architecture lends itself to real-time, sensor-based, and data communications applications.

IBM originally had chosen to market System/7 as a sensor-based front end for its 1130, 1800, System/360, and System/370 systems. Initially, the software for a stand-alone System/7 was rudimentary, and program preparation facilities resided in Modular System Program support (MSP/7) incorporated in the software of a host computer: 1130, 1800, System/360, and System/370. This is still offered, but IBM now also offers the MSP/7 program preparation facilities for the System/7. MSP/7 support includes a macro assembler, FORTRAN IV compiler, linking editor, formater, and disc support.

System/7 started out as a powerful, small system surrounded by configuration and software constraints that made it almost inextricable from larger IBM systems. Stand-alone systems were practical only for dedicated applications. IBM is gradually loosening the constraints on the System/7, and configurations for general-purpose processing are now feasible. System/7's expanded standard peripheral offerings, expanded disc storage, multiprogramming software, and greater stand-alone capabilities enable it to be used for a wide variety of new applications.

System/7 is extremely fast and can compete with top-of-the-line minicomputers in sheer processing power. Its 64K-word memory capacity and program preparation facilities make it competitive with other minicomputers on the market. Even though many minicomputer manufacturers (Digital Equipment and Data General, for example) have more developed foreground/background multiprogramming systems — some designed to mix real-time, time sharing with a batch stream — the addition of the present version of MSP/7 will make the system attractive to users because of the overall system speed and IBM's reputation.

Despite its speed and performance characteristics and its IBM label, System/7 has not been a booming best-seller. IBM has not marketed it aggressively or packaged it to compete very well with other minicomputer systems. The software constraints and the RPQ status of many peripherals make it appear to be a reluctant contender. Large discs are now available, but they too are RPQ items. System/7 still seems to be a caged animal that is allowed out only under controlled conditions with the trainer retaining strict surveillance on keys to the cage.

## USER REACTIONS

All System/7 users we contacted were pleased with the performance of the System/7.

One user selected it because it was reliable and fast and was backed up by IBM. Also, IBM first presented the possibility of sensor-based computing for his application. This company uses the System/7 as a front end to a System/360 Model 30 to monitor film processing. The company is expanding the system to control all laboratory functions, including process control and personnel record keeping. System downtime has been minimal and maintenance has been complete and comprehensive. This user finds the software good, the programming language easy to use, the hardware reliable, and the interfacing sensor-based devices simple.

A second user has installed a factory data collection system built around the System/7 and the System 370 Model 125. The System/7 was selected because it was cheaper than its major competitor for the data collection application at the time it was installed. Although the company had some problems with the 2790 system initially, these were ironed out and the whole system now runs smoothly. The System/7 itself ran well from the start. The company has a great deal of time left over on the System/7 but does not have any use for it because the 370 system manipulates and processes the data from the shop floor.

A third user has a stand-alone System/7 with 55 card readers to control the various gates and doors of an airport. The system is installed and operating. Downtime was less than five percent during startup.

Software houses and service bureaus often have very good overall views of a system's strengths and weaknesses. We interviewed two who were engaged in creating different types of data collection and process control systems based on System/7s. They successfully compete with IBM's software development groups because of expertise in particular process control areas. One user remarked that his company takes full responsibility for its installations: hardware interfacing, software development, and system maintenance. These companies also sell packaged systems, based on other minicomputers.

Frequently, control or collection systems are developed utilizing existing System/7s used part time for other purposes. Both of the users characterized the System/7 as an excellent piece of equipment, reliable and well-supported by IBM. One user pointed out that other minicomputer manufacturers survive because they price their systems lower. The other user had one criticism, which he labeled "very minor": IBM makes more software changes than necessary when adding enhancements, making the reprogramming to incorporate enhancements more extensive.

## CONFIGURATION GUIDE

System/7 operates either as a stand-alone computing system or a satellite processor linked to a host processor that is on-site or at a remote location. The system is structured independently of a host processor and is configured according to its application. A system consists of a central processor module and from one to 11 I/O modules housed in the appropriate 5026 enclosure. An I/O module is equivalent to a device controller. The 5026 enclosure provides the cabinetry, power supply, and physical interface connections. Memory and the Direct Control Channel (DCC) are part of the central processor module. The DCC includes the host-processor interface, the operator-station interface, and the two interval timers. Peripherals are listed in Table 2.

### Basic Configuration

The most basic stand-alone configuration includes an A02 processor with 2048 words of memory and one I/O module housed in a nonexpandable 5026 enclosure (Model A2). This configuration also includes an operator's console with paper tape facilities. An operator station is required with each configuration, but multisystem configurations can share a single station. Program preparation via an assembler requires a minimum of 4096 words of memory.

The basic configuration of a System/7-1130 installation includes a B02 processor with 2048 words of memory and one I/O module housed in a nonexpandable 5026 enclosure (Model A2).

Model B includes the 1130 attachment, which interfaces with the 1130 Storage Access Channel (SAC).

### Expanded Configuration

The 5026 enclosure contains power and internal interface connections for the processor, memory, and input/output modules. There are five enclosures that can be used in various combinations for configuring a system. A system, however, can include a maximum of 11 I/O modules.

5026 Model	Accommodates
A2	1 CPU and 1 I/O module
C3	1 CPU and 2 I/O modules
C6	1 CPU and 5 I/O modules
D3	3 I/O modules
D6	6 I/O modules

Model A2 is not expandable; Models C and D contain multiplexors that allow I/O expansion, and they also accept the air isolation feature. Model D can be 200 feet from Model C so that contaminants, humidity, or temperature that affect it do not affect the central processor.

### A/D Equipment Configuration

The input/output model is the basic building block for sensor-based I/O on System/7. Each module is self-con-

Table 2. IBM System/7: Peripherals

Model Number	Description
<b>DISCS</b>	
5022	
-001/-002	One fixed, 1 removable disc; 2.44M wds; 269/126-msec access
-003/-004	Fixed disc, 1.22M wds; 269/126-msec access
<b>PRINTERS</b>	
5024	80 to 155-lpm line printer
7431	85 or 115-cps dot matrix
<b>CARDS</b>	
2502	300-cpm reader
129	50- or 90-cpm reader, 12 to 50-cpm punch
5028	Keyboard printer with paper tape I/O
<b>ANALOG/DIGITAL</b>	
5012	Multifunction analog I/O and digital I/O module, 32 analog input pts
5013	Digital I/O, up to 128 input and 64 output pts
5014	Analog input, up to 128 pts; speed ranges from 200 pts/sec to 20K pts/sec
<b>COMMUNICATIONS</b>	
1610	Async communications
2074	Binary sync adapter
—	1130 channel attachment
2790 DATA COMMUNICATIONS (RJE)	
8185	Up to 16 2791/2793 area stations
	Control for up to 16 subsystems of 16 data entry stations each, up to 128 displays
2795/6/7	Card and badge readers
2798	Guidance display 12/subsystem
1035	Badge reader
1053	Printer
<b>CUSTOM PERIPHERALS (RPQ)</b>	
5029	Magnetic stripe card reader
5096-NI	Digital input multiplexor
5098-NI	Teleprocessing multiplexor, 16 lines
5098-N3	BSC module, 4 lines
5098-N5	Sensor-based control connects 64S/7 to S/370
7414-1	Interactive console (CRT, 480, or 960 char)
1017/1018	Paper tape attachment
—	Tape cassette records
—	Async comm for 1200 or 50K bps
SBCU/SBCA	System 360/370 channel attachment
3340/3348	Up to 8 3348 discs per 3340; up to 34.2M words per data module in "native" mode; or 29.4M wds in 5022 emulation mode
Disc Sub-system	

tained and houses all the hardware to provide I/O functions. All I/O modules are interchangeable and can occupy any position except the processor position in the 5026 enclosure.

Three I/O modules are available for special equipment: the 5014 Analog Input Module, (Models B, C, D, and E); the 5013 Digital Input/Output Module; and the 5012 Multifunction Module. The 5014 can handle up to 384 input points. The 5012 handles analog/digital subsystems (up to 128 digital inputs, 64 digital outputs, 32 analog inputs, and two analog outputs) and the 2790 Communications

Subsystem, which are remote data-entry equipment peculiar to plant automation. The 5013 modules provide for attachment of 128 digital inputs, 64 digital outputs, the 2790 control, and special devices.

### Other Expanded Configurations

The 5022 Disc I/O Module occupies one position in the 5026 enclosure. Only one disc module can be mounted in an enclosure, and a maximum of eight 5022s are allowed per system. Modules not mounted in an enclosure require a 4650 Integral Power Supply. One 5022 disc provides 2.44 million words (Models 1 and 2) or 1.22 million words (Models 3 and 4).

The 3340/3348 disc subsystem differs from the 5022 in that an entire string of eight drives can attach to one enclosure "shelf" position via the D08331 Attachment Module. The D08331 attaches to a C3 or C6 enclosure; the C3 (but not the C6) requires the D08332 power supply option.

A D08331 is required for each Model A2 drive (two spindles). The A2 can then attach three more "B" drives, which can be either Model B1 (one-spindle) or Model B2 (two-spindle) drives. Each spindle can hold a Model 35, 70, or 70F pack. The storage-byte capacity is 17.1M words for the Model 35 and 34.2M words for both Model 70 and Model 70F. The 70 and 70F packs differ in that the Model 70F has five fixed heads and one movable head, whereas the Model 70 has one movable head.

The 3340/3348 subsystem can operate in a 5022 emulation mode, called "7 mode." This allows program compatibility with existing installations and a greater variety of access methods. Up to 12 5022 drives can be emulated, but this reduces total pack capacity because of the small record sizes. Maximum capacity in emulation mode is about 29.4M words for one pack.

A System/7 can use both emulation and native modes on the same subsystem. A System/7 can also use both 5022 and 3340 drives on the same system.

The optional asynchronous or bisynchronous communications feature on Processor Models A and E occupies the same space in the processor as the 1130 Channel Attachment on B models. These features are manually exclusive. The asynchronous communications feature with a line adapter can transmit data at a rate of 134.5 or 600 bits per second. Bisynchronous communications operate in half-duplex mode at a wide range of speeds: 1200, 2000, 2400, and 7200 bits per second and above. The channel attachment transmission rate is based on the cycle-stealing capability of the 1130 processor.

### Software Configuration Requirements

The configurations demanded by the basic system software packages are listed in Table 3.

### COMPATIBILITY

System/7 is not program compatible with any other system produced by IBM; it is marketed, however, as a

**Table 3. IBM System/7: Software**

PACKAGE	DESCRIPTION
MSP/7	Modular System Program for system control; with Disc Support System (DSS/7), requires disc, console, and 4K wds memory if program preparation on host; 8K to 12K wds if stand-alone version with program preparation on System/7
Executive/7	Adds real-time multiprogramming on-line background batch to DSS/7 level support, storage protection, 3340 disc subsystem support, and other features
ASM/7	Macro Assembler, requires 4K-wd memory, console
PREP/7 (HOST ASM/7)	Cross Assembler Link Editor and Loader for program preparation on 360/370; DOS/VS requires 14K bytes of exclusive storage, 3 disc or tape units; OS/VS requires 44K bytes of exclusive storage
HOST PROGRAM (PREP II)	For program preparation on 1130 or 1800; requires same configuration as 1130 or 1800 macro assemblers and linkage editors
FORTTRAN IV	Stand-alone or host versions; stand-alone version requires 12K-wd memory, disc, console
UTILITIES	LINK/7 Linkage Editor, Format/7 formatting Loader, enhanced macro library/relocatable
AML/7	Application Module Library, a set of applications-oriented macros
CCAP/7	Stand-alone Message-Switching Control Program
PCP/7	Process Control Program for monitoring, DDC control
APG/7	Application Program Generator runs on host 360/370 to generate programs using AML/7 macros

front end for a host computer — IBM 1130, IBM 1800, System/360, or System/370. Data compatibility with these processors is maintained via the 16-bit word, which contains two eight-bit bytes. The host computers not only prepare programs for System/7, but they also transmit object programs to System/7 for execution. In addition the host computer can perform System/7 initial program load.

System/7 can communicate with System/3 via BSCA facilities.

The Axx and Bxx models of the System/7 are identical except for external interfaces. Except for the Disk Support System 7 (DSS/7), the user must provide or coordinate the basic control software for System/7. Any physical change that affects either addressing or other I/O service becomes his responsibility. It is expected that without standards for processor organization, there will be little if any program compatibility between systems. Reassembly of programs appears mandatory.

The MSP/7 program preparation facilities under DSS/7 (or EXECUTIVE/7) versions for stand-alone

System/7 configurations are compatible with host computer preparation facilities. IBM releases enhancements to stand-alone and host FORTRAN program products simultaneously to maintain compatibility.

Programs developed for the Model A will run unmodified on a 16K-word Model E, but programs must be reassembled to run on models with more than 16K words.

When a 3340 disc subsystem is added to a system, it can be operated in emulation mode to achieve compatibility with programs developed for 5022 discs. For 3348 packs to be data compatible with S/370 they must be recorded in native mode.

## MAINTENANCE AND SUPPORT

As the largest computer manufacturer in the world, IBM has the most widespread sales and service facilities, reaching into all corners of the globe. Part of IBM's success has been attributed by many industry observers to the efficiency and broad services offered by the sales and service network.

IBM provides a variety of maintenance contracts, depending on what the user needs and can pay for. The standard prime shift maintenance contract provides for prompt emergency service.

## TYPICAL PRICES

Model Number	Description	Monthly Rental (Incl Maint.) \$	Purchase Price \$	Monthly Maint. \$
IBM SYSTEM/7				
CENTRAL PROCESSOR AND WORKING STORAGE				
5010-(1)	System/7 Processor with Integral Memory Modules			
A02	2,048 Words	199	8,670	51
A04	4,096 Words	313	12,400	63
A08	8,192 Words	541	19,900	87
A10	10,240 Words (requires 7401 over 8K words)	654	23,600	99
A12	12,288 Words	767	27,400	111
A16	16,384 Words	994	34,900	135
B02	2,048 Words	307	12,700	60
B04	4,096 Words	421	16,400	72
B08	8,192 Words	649	23,900	95
B10	10,240 Words (requires 7401 over 8K words)	762	27,700	107
B12	12,288 Words	876	31,400	120
B16	16,384 Words	1,100	38,900	144
E16	16,384 Words	1,010	35,400	247
E20	20,480 Words	1,155	40,300	281
E28	28,672 Words	1,440	49,900	347
E32	32,768 Words	1,590	54,700	379
E36	36,864 Words	1,740	59,500	413
E44	45,056 Words	2,025	69,200	478
E48	49,152 Words	2,175	74,000	512
E52	53,248 Words	2,320	78,800	544
E60	61,440 Words	2,610	88,500	611
E64	65,536 Words	2,755	93,300	644
7401	Storage Power Addition (for A2)	16	652	1
2662	Cycle Steal Basic	48	1,830	3
5026-	Processor Enclosure for Processor and Up to 11 I/O Module Positions			
A02	1 I/O Position	108	4,710	26
C03	2 I/O Positions	248	10,200	31
C06	5 I/O Positions	367	14,400	50
D03	Extension of C3/C6 by 3 I/O Positions (requires 3715)	248	10,200	40
D06	Extension of C3/C6 by 6 I/O Positions (requires 3715)	367	14,400	59
3715	Dx Enclosure Attachment	37	1,420	5
4621	Internal Air Isolation (for C3/D3)	48	2,290	12
4622	Internal Air Isolation (for C6/D6)	65	3,060	24
5731	Power Failure Detect and Restart (1/enclosure)	54	2,040	1
7401	Storage Power Addition (for C3/C6)	17	652	1
5028-(1)	Operator Station (Incl keyboard/printer and 10-cps paper tape reader/punch)	150	2,280	51
MASS STORAGE				
5022-	Disc Storage Module			
001	1 Removable, 1 Fixed Disc; 2.44M Words; (269 msec)	421	15,100	91
002	Same as 001 except 126 msec	492	16,500	100
003	1 Fixed Disc; 1.22M Words; Avg Access Time (269 msec)	324	13,500	87
004	Same as 003 except 126 msec	394	14,800	95
4650	Integral Power Supply	37	1,420	1
2664	Disk Cycle Steal	16	612	1
5440	Disk Cartridge (for 5022-001, 002 only)	NA	NA	NA
3340-A02	Two Discs and Control	1,059	40,000	80
3340-B01	One Disc Drive	592	22,000	43
3340-B02	Two Disc Drives	747	28,000	69
D08-331	Interface for 3340	1,125	39,375	168
D08-332	Power Supply (to attach D08331 to C3 enclosure; not needed for C6 enclosure)	32	1,120	1
4301	Fixed-Head Feature	47	1,900	2
3348-35	Removable Data Modules for 3340 (34M bytes)	59	1,600	-
3348-70	69M- or 41M-byte Removable Data Module	82	2,200	-
3348-70F	69M-byte Removable Data Module	165	4,400	-
INPUT/OUTPUT				
5012-A01	Multifunction Module (requires 8185)	42	1,830	8
4115	5024 Attachment Feature	30	1,320	4
5024-1	Provides space, power, and logic to connect line printer to CPU (includes line printer)	482	18,040	71
5024-2	Provides space, power, and logic to connect card reader to CPU	276	10,340	13
5024-3	Combination of Models 5024-1 and 5024-2	640	22,500	77
DATA COMMUNICATIONS				
Asynchronous Communications				
1610	Async Communications Control (5010-Axx models only)	81	3,060	14





## TYPICAL PRICES (Contd.)

Model Number	Description	Monthly Rental	Purchase	Monthly
		(Incl Maint.) \$	Price \$	Maint. \$
2165	Common Carrier Adapter	10	408	2
4750	Line Adapter — Limited Distance Type 2B	27	1,020	15
4751	Line Adapter — Leased Line Type 1A	27	1,020	15
4752	Line Adapter — Leased Line Type 1B	27	1,020	15
2074	Binary Sync Communication Control	194	7,340	59
4703	Internal Clock	21	818	3
4800	Line Interface Type 1D	27	1,020	3
4805	Line Interface Type 1G	54	2,040	1
5500	IBM 1200 bps Integrated Modem, Leased	16	535	3
5501	IBM 1200 bps Integrated Modem, Switched	21	714	3
	Remote Data Entry			
8195	2790 Control (for up to 16 2791/2793 area stations; requires 5012 and 8195; only one 8195/system)	108	4,080	8
2791-001	Area Station Controller (for up to 16 units)	198	8,400	45
3330	Digital Device Read-In	10	510	1
3690	External Alarm Contacts	10	510	1
2791-002	Area Station Controller (used as I/O station without adapters)	146	6,920	45
2793-001	Area Station Controller (for up to 8 2795/2796/2797 units; can support one 8296 Extension Unit, one 1053 Attachment, and the following units)	130	6,180	19
2798-001	Guidance Display Unit (up to 12/area station; max 128)	96	4,400	19

Notes:

(1) Axx models can support a 1610 Async Communications Control for communication via communications lines with the IBM 1800 and Systems/360 and 370; the Bxx models include an 1130 Host Processor Attachment for direct storage-to-storage communication with the IBM 1130.

— Not Applicable

NA Not Available



## OVERVIEW

The SUE (System User Engineered) Computer systems, like their predecessors the MAC 16 and MAC Jr., are designed, marketed, and supported by the Lockheed Electronics Data Products Division, primarily as an OEM product; SUE systems are offered to the business end user as the System III product line. SUE systems are not compatible with the MAC 16 and MAC Jr., but a translator program is available for SUE to translate MAC machine language programs into SUE machine language programs.

SUE processors are 16-bit, byte- or word-oriented microprogrammed processors. Addressing is to the byte level. The SUE is the basic general-purpose system with a 108-instruction set. SUE-SIS designates a scientific version with 38 added instructions in the control ROM. Single processors can support up to 32K words of core.

The SUE systems are modular and flexible. A system can vary from an Infibus controller with user-designed modules to a multiprocessor configuration with up to four SUE processors. Multiprocessor configurations can handle up to 80K words of core by mixing dedicated and common memory banks. SUE is designed to protect the user from system obsolescence by making it easy to add new technology on a function basis. This is accomplished by designing the system around a central bus system called the Infibus, over which system modules communicate with each other on a signal-response basis. System modules operate asynchronously with respect to each other and are synchronized only for information transfer cycles.

Mainframe characteristics are summarized in Table 1. The central data bus architecture is similar to that of DEC's PDP-11 and Hewlett-Packard's HP 3000. SUE will compete with the low end of the PDP-11 line, specifically the PDP-11/05 and 11/15, which are aimed toward the OEM market, particularly the communications sector.

System software includes a Basic Operating System, a foreground/background Disc Operating System, an IOCS operator communications package, various utilities, and, recently, Fortran IV. Peripherals include discs, terminals, slow-speed devices of various kinds, and communications interfaces. Lockheed plans to introduce a multiprocessing operating system, BSC communications, and 2780 emulation during 1975.

The first SUE was delivered in March 1972. Over 2,000 systems have been delivered to date.

Table 1 lists the SUE's mainframe characteristics.

## Competitive Position

The SUE competes primarily in the OEM market. Its software supports assembly language and Fortran

**Table 1. Lockheed Electronics SUE: Mainframe Characteristics**

<b>CENTRAL PROCESSOR</b>	
Microprogrammed	Yes
No. of Internal Registers	8 general-purpose
Addressing	
Direct (no. of words)	32K (doubleword instructions); 256 (singleword)
Indirect	Multilevel
Indexed	Yes
Instruction Set	
Number	108 (std), 146 (opt)
Decimal Arithmetic	Subroutine
Priority Interrupt	
System	
Lines	4
Levels	4 (unlimited sharing)
<b>MAIN STORAGE</b>	
Type	Core
Cycle Time (nsec)	800
Basic Addressable Unit	Byte/word
Bytes per Access	1 or 2
Ports to Memory	1
Min Capacity (bytes)	2K
Max Capacity (bytes)	64K
Increment Size (bytes)	8K; 16K
Parity	RPQ
Protect	RPQ
ROM	
Use	Control memory
Capacity (bytes)	256 or 512K, 2K possible
<b>I/O CHANNELS</b>	
Programmed I/O	Yes
DMA Channels (no.)	Yes (unlimited no.)
Multiplexed I/O	Yes
Max Transfer Rate (words/sec)	
Within Memory	2.2M (overlapped core)
Over DMA	5M

programming, under core-based and disc-based operating systems. LEC provides discounts of up to 37 percent for quantity purchases of SUE systems. Discounts do not apply to peripheral devices because LEC buys the devices and provides only the controller interface. The company has sold SUE to communications, data entry, and COM systems OEMs, among others.

Competitors to the SUE include the DEC PDP-11/05 and 11/15; Computer Automation LSI Alpha 16 and Naked Mini 16; General Automation LSI SPC-16, Data General Nova 2, and Microdata 1600. Because SUE is similar in architecture to the PDP-11 and Digital is a large minicomputer manufacturer, it is not surprising that SUE's most vigorous competitor is the PDP-11.

LEC markets SUE chiefly in the communications and process control OEM markets. The introduction of the new DOS should make the system more competitive in these areas. This operating system is of the foreground/background type with one multitasking program operating in the foreground and one batch program operating in the background. Operating systems for real-time and multiprocessor applications will be developed later.

LEC has one advantage over many minicomputer manufacturers in the OEM market: it is a large core memory

supplier to the computer industry as a whole. Consequently, the cost of core memory for its system is low and total system cost is low.

## User Reactions

SUE users we contacted were in accord both about the excellent SUE hardware, particularly for the OEM market, and the need for LEC to step up the pace of its software development. A spokesman for a cancer research group, using the system as the heart of a multiparameter analyzer for cells, went so far as to call the hardware design and overall system reliability, "Excellent enough to make Lockheed number 2 in the minicomputer market if the company would market the system more aggressively and concentrate more on software development." An OEM manufacturer developing the SUE as a communications network processor explained that the SUE is unique in the minicomputer market — the arbitration function that determines which component has control of the Inibus is separate from the CPU. Thus, it is easy to use the system building blocks in a multitude of patterns. This company developed a bus connector to allow both multiprocessor systems and multibus systems, some with memory, peripherals and processors on different busses.

## CONFIGURATION GUIDE

A SUE computer system consists of a card frame guide; an Inibus and controller; power supply; SUE or SUE-SIS processors; up to 32K words of memory per processor; a control panel; and a universal serial or parallel controller for each peripheral device in the system.

The processors, like all other pluggable system modules, connect to the Inibus, which is in turn controlled by the Inibus controller; also like other pluggable modules, processors can be mixed in a multiprocessor system. Up to four processors can be connected to one Inibus.

The processor models differ basically in the functions they can perform rather than any effect on system configuration. The "SIS" models add instructions to the standard SUE to create a processor suitable for scientific processing and Fortran programming. The master processor is designated by proximity to the Inibus controller in a multiprocessor system, rather than by model. Model numbers are designated as SUE or SUE-SIS 1004, 1008, 1016, 1024, or 1032 depending on the number of words of memory included with the basic CPU.

A chassis consists of an Inibus and the card frame guide. All system modules are mounted on circuit cards that slide into a card guide slot and plug into the Inibus. Twenty-four slots are available for mounting system modules. An internal power supply requires eight slots; if an external power supply is used, other system modules can use the eight power supply slots.

Memory can consist of 4K- or 8K-word core memory modules. Any number of memory modules can be intermixed on a system, provided the total does not exceed 32K words in a single-processor system. Multiple processors can handle up to 80K words in one system by combining 16K dedicated memory banks with a 16K common area. Each core module requires three card slots. Effective memory capacity is limited to 30K words per processor, because the upper 2K-memory word addresses are reserved to address I/O device registers.

Each parallel or serial I/O controller requires one card slot. A block transfer adapter that requires one slot must be inserted next to each controller that needs block transfer capability.

Peripheral devices include Teletype units, high-speed paper tape reader/punch, card reader, line printers, industry-standard magnetic tape units, displays, discs, and asynchronous data communications controllers. A universal logic board is available for designing interfaces for special-purpose devices. The peripheral devices are listed in Table 2.

The 1825 Bus Extender allows two Inibuses to be connected to increase the system card slot capacity. Two SUE systems connected to a common Inibus via communications modules can communicate to obtain many of the advantages of a system doubled in size, including a wider variety of peripherals. The interrupt priority level of the intersystem communication modules can be assigned to any level desired by the system engineer and can be positioned on the Inibus to any priority within its assigned level. Software packages for the SUE with configuration requirements are listed in Table 3.

**Table 2. Lockheed Electronics SUE: Peripherals**

Model No.	Description
<b>Disc</b> 6755	IBM 5444 compatible unit, one fixed and one removable cartridge, 2.5M bytes/disc, 4 drives/controller
<b>Terminals</b> 6710 6762 6770	Teletype, ASR 33, 10 cps Printer Terminal, 100 cps CRT Terminal, 960 char
<b>Printers</b> 6765 6768	Line Printer, 200 lpm Line Printer, 600 lpm
<b>Cards</b> 6733 6734	Card Reader, 600 cpm Card Reader, 285 cpm
<b>Paper Tape</b> 6717/18 6723 6719	Paper Tape Readers, 300 cps Paper Tape Punch, 75 cps Combination 6718 and 6723
<b>Communications</b> 4651 4530 4502 4501/3/6	Async Modem Controller, single line, 300/1200/1800/4800 baud Four-channel Async MUX to 9600 baud Serial I/O Controller, RS232C and 20mA polar control Parallel I/O Controller, TTL compatible

**Table 3. Lockheed Electronics SUE: Software**

Package	Description
<b>DOS</b>	Disc Operating System, foreground/background system, requires CPU, 16K words of core, disc, TTY, Card Reader; available mid 1975
<b>BOS</b>	Basic Operating System, includes loaders, I/O control system, Operator Utility Interface Package (OUIP), Debug, CPU Test, Memory Test, Peripheral Tests; requires 4K words of memory and Teletype; can support FORTRAN IV and assemblers.
<b>FORTRAN IV</b>	ANSI X3.9 - 1966 standard, requires CPU, 8K words of core, TTY.
<b>Assemblers</b>	Basic assembler requires 4K words and Teletypes while the Macro assembler requires 8K words and Teletype.

### Compatibility

The SUE is not compatible with any other computer. Lockheed's System III product line is based on the SUE system so programs written in Fortran IV or assembly language are interchangeable, given comparable configurations. Programs developed for LEC's MAC 16 and MAC Jr., can be translated into SUE machine language code; the translator runs on SUE. Cross assemblers are available for the MAC 16 and the IBM System/360 so that SUE assembly language programs can be assembled on the MAC 16 or IBM System/360. A SUE simulator written in Fortran is available so that SUE-assembled object code can be tested or executed on any larger computer system that supports ANSI standard Fortran.

### MAINTENANCE

Lockheed provides two types of maintenance contracts — a preventive maintenance contract with an extra emergency service charge per visit and an inclusive contract that provides both preventive and emergency service for a single fee. The Field Engineering Department has offices located throughout the United States. Repairs can also be handled at either the local service center or at Los Angeles headquarters. A 10-day course in the basic maintenance of a SUE system is offered free of charge for each SUE customer.

### TYPICAL PRICES

Model Number	Description	Purchase \$
	SUE Central Processor Systems include 16 slot chassis, SUE INFIBUS, integral power supply panel and bezel, power distribution unit and cooling fans; CPU includes 8 general purpose registers, basic instruction set of 108 instructions, 4 levels of shared priority interrupts, power monitor/auto restart and real time clock; core memory full cycle time is 800 nsec	
1004	CPU with Primary Instruction Set and 4,096 words of 16-bit Core Memory	4,350
1008	1004 with 6,192 words of 16-bit Core Memory	5,950
1016	1004 with 16,384 words of 16-bits of Core Memory, 24 slot Chassis, External Power Supply	7,945
1024	1016 with 24,576 words of 16-bit Core Memory	9,945
1032	1016 with 32,786 words of 16-bit Core Memory	11,445
1004/8/16/24/32 SIS	CPU with Scientific Instruction set	+500
1004/8/16/24/32 NCP	No control panel option	-400
	<b>CPU OPTIONS</b>	
1240	Autoload-automatically loads memory from selected input device	565
	<b>MEMORY OPTIONS</b>	
	Can be used in any combination up to 32,768 words of memory	
3310	Random Access Magnetic Core Memory with 4,096 16-bit words	2,000
3312	Same as 3310 except 8,192 words	2,200
	<b>MASS STORAGE DISC</b>	
6755-10	Disc Storage Unit, IBM 5444 compatible	9,630
6755-11	Add-on Disc Storage Unit	6,330
6757	Removable Disc Cartridge	200
	<b>INPUT/OUTPUT</b>	
	Teletypewriter	
6710-10	Teletypewriter-ASR model 33, Controller, Cable Paper Tape	2,030
	Includes controller & cable	
6717-10	High Speed Paper Tape Reader w/o spooler	2,155
6718-12	Same as 6717-10 except with spooler	3,255
6719-30	Combination High Speed Paper Tape Reader and Punch	5,015
6723-20	High Speed Paper Tape Punch	3,560
	<b>Printers</b>	
	Include controller, cable	
6762-11	Printer Terminal — 132 column, 64 character set, 100 characters per second rate, without stand	4,275
6762-12	6762-11 with stand	4,585
6765-21	Line Printer — 132 column, 64 character set, 200 LPM	12,145
6768-31	Same as 6765-21 except 600 LPM	15,820
	<b>Card Readers</b>	
	Include controller, cable	
6733-11	Card Reader — 80 column, 600 cards per minute	5,745
6734-10	Same as 6733-11 except 285 cards per minute	3,895
	<b>Interfaces and I/O Controllers</b>	
4501	Parallel I/O Controller	800
4502	Serial I/O Controller	565
4503	Parallel I/O Controller	800
4506	Low true input and high true output	800
4551	Custom Bus Interface	565
4590	Block Transfer Adapter	500
	<b>Data Communications</b>	
	<b>DATA COMMUNICATIONS I/O CONTROLLER OPTIONS</b>	
4651	Async Modem Controller	565
4530	Four Channel Async Line Multiplexor	1,050

### HEADQUARTERS

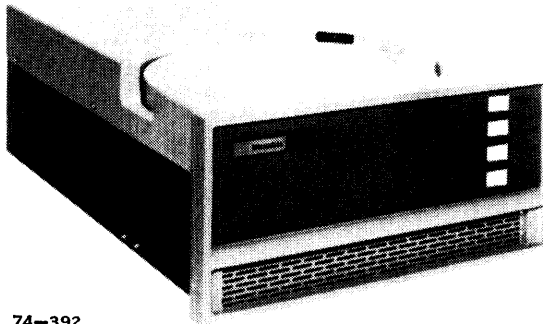
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# MICRODATA

Micro 800 and 1600 Series

AUERBACH Buyer's Guide to . . .  
MINICOMPUTERS



74-392

## OVERVIEW

The Microdata Micro 800 and 1600 Series are microprogrammed, stack-processing, byte-oriented systems aimed at general-purpose OEM markets. The two lines differ slightly in speed and packaging; the 800 series has a 1.1- $\mu$ sec memory cycle time while the 1600 series has a 1- $\mu$ sec memory cycle. The 1600, moreover, has different firmware to improve performance over and above that obtained from the shorter memory cycle time.

Microdata was microprogramming its systems long before microprogramming was widely implemented. The 800 series was introduced in the spring of 1969 by Micro Systems Incorporated, then a subsidiary of Microdata. Subsequently, as the line developed Micro Systems was totally merged into Microdata Corporation. The 800 line is still in production although it is a "discontinued" product; it has been replaced by the 1600, an optimized version that retains the same architecture, instruction set and peripherals as the 800. Both series, moreover, have submodels that differ mostly by the instruction set implemented in the ROM memory. The Micro 800 series includes the 800, 810, 820, and 821, which implement from 23 to 107 instructions. The 1600 Micro Series includes the 1600, 1600/10, 1600/20, 1600/21, 1600/30, 1600/40, and 1600/60, which implement instruction sets ranging from 23 to 111 instructions. The submodels with the same 2-digit ending, for example, correspond with the 821 and 1600/21, both contain the same instruction set. Model 10 has a few less instructions than Model 20. Model 21 has the same instruction set as the Model 20, but it has been recoded to achieve higher speeds. Model 30 has a few more instructions to handle dual processor configurations. Model 40 has a superset of the Model 20, with extra instructions to handle multiuser "Basic." Model 60 has no instructions available to the user; it is designed as a communications front end in a multiple processor configuration with Model 30, and its control ROM is dedicated to handling communications terminals.

The 821 and 1600/21 are so similar there is no compatibility problem in moving from one system to the other at this level — the same peripherals can attach to either, and all programs in similar operating environments can be run on either system. Similarly, all 800 programs can run on

1600 machines. The only exception might be programs with time-dependent subroutines that run on systems without real-time clocks. The 821-1600/21 instruction set, for example, comprises 107 instructions: 16 control, 12 arithmetic and logical shifts, 17 conditional jumps, 6 I/O, 19 interregister, 8 stack control, 5 character/string manipulation, 2 decimal add/subtract, 2 multiply/divide, and 20 memory reference instructions.

Software for the two series includes an operating system, assembler, Teletype debug facility, text editor, and diagnostics. The operating system is a simple Teletype/paper tape operating system (TOS) that requires high-speed paper tape facilities and a card reader in addition to the CPU, 4K words of memory, and Teletype. The assembler (MAP 810/820) is a 2-pass macro translator that generates absolute code. The BASIC language is also available at extra cost.

## PERFORMANCE AND COMPETITIVE POSITION

Until the recent introduction of the 3200 and the Reality™ small business system, Microdata sold its systems almost exclusively OEM. More than 95 percent of the current installations (which now number in excess of 6,000) are OEM. A few universities and colleges also bought Microdata systems as end-user systems. Microdata markets their systems abroad through Inter-technique in France, Tejin Limited in Japan, and Allen Crawford Associates in Canada.

Microdata is vigorously working to expand its installed base, partly because a few customers accounted for a large part of its business and this made the company somewhat vulnerable. In 1973, Microdata reported that 74 percent of its sales went to five customers with one order accounting for 39 percent of total sales.

The 1600 Series has stiff competition from other OEM-oriented manufacturers, some of whom also provide the benefits of microprogramming to OEM customers. General Automation and Computer Automation as well as DEC, Data General, and Hewlett-Packard have big OEM businesses. General Automation and Hewlett-Packard, moreover, provide extensive support for microprogramming for their systems.

Microdata has kept step with its competitors at the low end of the market by introducing the Micro-One bipolar microcomputer, a computer-on-a-board that serves as an entry system to the 800/1600 series. The 3200 Series at the upper end provides another compatible line with higher performance characteristics than the 1600. Thus, the company has an integrated series of product lines with each series upward compatible with the next higher system in the line.

Reality™ and ENGLISH™ are registered trademarks of Microdata Corporation.

### User Reactions

Most Microdata users bought their 800/1600 on an OEM basis and configured them into systems for their own end-users. The users interviewed were acutely aware of the reliability and performance of the Microdata processors; the processor's performance affects the performance of their completed systems and, ultimately, the company's very existence.

All users interviewed expressed pleasure with their Microdata processors. Most users handle their own maintenance; one user has never had a reason to call Microdata. Another user said he dealt more with Microdata engineers than with the field service people. A third user simply returns faulty chips to Microdata, which sends replacements in the mail.

Before selecting the Microdata equipment, users investigated the major minicomputer manufacturers: Digital Equipment, Hewlett-Packard, Varian, Computer Automation, General Automation, Interdata, IBM, and Texas Instruments. One user also looked at Systems Engineering Labs and the Four Phase small business system. Another user considered Intel's microprocessors for the low end of his systems. The reasons for choosing Microdata equipment varied. All users spoke of Microdata's early entry into microprogramming. One user wanted a microprogrammed machine with an instruction set that could be customized and optimized. He required many machines and wanted to be near the vendor. Another user chose Microdata because of the price and the ability to communicate with a CRT and a printer at the hardware and software levels. Another user found the Microdata dual-processor configuration to be the least expensive bid to meet required specifications. One user bought the Microdata 1600 because of its ability to emulate Varisystem's P-16 controller. This emulation afforded continuity for his end-users.

Most users developed their own languages and a few also developed their own operating systems. One user translated his business language into the Microdata assembly language.

Microdata machines are used in many environments. One firm has used the 1600 for two years as a photo unit controller for photocomposition machinery. This user found that service time in the field was reduced by changing from a "repairable" controller to a card controller; replacing the defective card was fast and simple. The user thought highly of the features provided to prevent memory loss. The firm discovered a minor malfunction in the back plane — one chip kept failing. Microdata changed the chip design from thin film to discrete components. The firm is planning to add more core in the near future.

Another user has a 1600 twin-processor configuration which operates as a communication controller for an IBM 360/75; it receives information from terminals in various areas. Most of the operating system is implemented in firmware. The user feels that Microdata has produced a

balance of hardware, firmware, and software resulting in a very economical communication controller. In the dual configuration, the first processor communicates with the host computer through channel communications, and the second processor is dedicated to scanning the communication lines.

A turnkey systems house uses 1600 processors as the core of medical laboratory systems to handle medical billing, accounts payable and receivable. This company also sells its systems to small furniture manufacturers. The user has developed a disc operating system, implemented mainly in firmware. The company had some system integration problems, which were not caused by defects in the processor. This user found the 1600/20 instruction set to be "pretty darn good" operating in one-byte precision.

Another systems house uses a customized 1600 as an index table and controller for data storage and retrieval system which are tied on-line to a host computer. It converts key strokes to a location on film to retrieve data. This user found the 1600 to be reliable and the only computer available in the company's price range and compatible with its application.

A user of 1600/21 and 1600/30 processors configures this equipment into turnkey systems for wholesale pharmaceutical and warehouse applications. The firm has developed its own business language and disc operating system for these purposes. The firm had a good experience with Microdata, although Microdata's response to a minor fault in the disc controller was poor. This user assumes the responsibility of maintaining the finished system.

A company that produces small business systems uses the Microdata 1600 for its central processor. Microdata installs the user's custom firmware and tests it through a comparator for bits. This company also tests the equipment with its own diagnostics. This user has experienced fewer problems than expected and is pleased that Microdata delivers equipment on the date specified. This user believes the Microdata equipment has a proven track record and that is important.

### CONFIGURATION GUIDE

The 800 and 1600 differ mostly in speed, ROM control memory, packaging (different systems panel) and a few options, but configuration details for both series are nearly identical. Basic configurations consist of a CPU, power supply, bank of 16 registers (6 working registers) control ROM implementing the instructions, priority interrupt system with 8 external interrupts, bootstrap loader, 3 I/O modes (DMA, buffered I/O, programmed I/O) and 8K words of memory. Processor options include a real-time clock, 8-level increments for the interrupt system up to 64 levels, expanded DMA capability, and memory expansion to 32K words. Power-fail detect/auto restart is optional on the 800 and standard on the 1600. The control ROM can be expanded up to 1,024 words in 256-word modules. See Table 1.



**Table 1. Micro 800 and 1600: Specifications**

<b>CENTRAL PROCESSOR</b>	
No. of General-Purpose Registers	6
Addressing: Indexed	To 32K words
Indirect	± 128 words
Instruction Set (no.)	23-107
Priority Interrupt Levels	8-64
<b>MAIN STORAGE</b>	
Type	Core
Word Length	16 bits
Cycle Time (μsec)	1.1 (800); 1.0 (1600)
Increment Size (words)	4K, 8K
Capacity (min-max) (words)	8K, 32K
Parity	No
Protect	No
<b>ROM</b>	
Use	Microprogram, user macros
Capacity	1,024 words
<b>I/O CHANNELS</b>	
Programmed I/O	Yes
DMA	Yes
Multiplexed I/O	No
<b>OPTIONS</b>	
Real-Time Clock	Yes
Floating-Point Processor	No

Model 1600/30 can be coupled with a 1600/60 in a multiprocessor configuration, but smaller models do not have this capability. Model 1600/40 has extra instructions to handle multiuser "Basic" configurations.

### Central Processor

Instructions for all 800 and 1600 machines are microprogrammed. ROM control memory, usually implemented in semiconductor memory, contains the microcommands that define instruction sets. Its operation proceeds at the basic 220-nanosecond clock rate of both series. For all instructions except a JUMP, the next ROM word to be used is preloaded into the processor's control register; this lookahead feature reduces instruction execution times.

The CPU uses separate registers to address control memory and to buffer its output. In addition to implementing the instruction set, control memory can store firmware program constants.

Memory referencing instructions have eight possible addressing modes; namely, direct, direct relative, indirect, indirect relative, indexed, biased indexed, extended, and literal. The basic memory reference instruction is one byte containing two fields: a 5-bit operation code and a 3-bit M field that specifies the address mode. Additional bytes (up to five) contain the operand address, indirect address, base address, or a literal depending upon the addressing mode. Direct addressing can access the first 256 memory locations. Relative addressing can access the 127 locations above or 128 locations below the next instruction in memory.

Indirect address words are located in the first 256 core memory locations. Indexing adds the indirect address word and the index register to produce the effective address. Extended addressing and indexing require a multiple-byte instruction that can address all 32,768 words of storage.

Internal interrupts on the MICRO 800 and 1600 are higher in priority than external interrupts. They have the following priorities from lowest to highest: console-triggered interrupt, direct memory access channel termination, real-time clock, memory protect, memory parity, memory boundary error, power fail, and power on.

Individual interrupts from peripheral subsystems are handled by an external interrupt module, which provides for arming/disarming individual interrupts and enabling/disabling recognition of interrupts in a group. Standard external interrupt cards with eight priority interrupt lines are available. A total of 64 external interrupts can be implemented.

Programmable registers include 16-bit accumulator and extension register, 16-bit index register, 15-bit program counter, 2-bit word-length register, and a 1-bit overflow register.

Table 2 summarizes the characteristics of the different processor models.

### Input/Output

Micro 800 and 1600 Series have three input/output facilities: serial Teletype interface, direct memory access (DMA), and a byte input/output bus. The serial Teletype interface can communicate with a full-duplex Teletype; a Parallel Teletype Controller option provides for transfer rates up to 300 characters per second, instead of the standard 10 characters per second. The DMA interface allows direct data transfers between memory and device controllers on an interleaved cycle-stealing basis at transfer rates up to 910,000 (821) or 1,000,000 (1600/21) 8-bit bytes per second.

**Table 2. Micro 800 and 1600 Models**

Model	Instructions
800	23
810	89
820	95
821	107
1600	23
1600/20	95
1600/21	107
1600/30	111
1600/40	107
1600/60	None*

\* None accessible to user; acts as communications front end in multiprocessor configuration with the 1600/30.

The byte input/output facility allows programmed byte-by-byte I/O transfers and buffered block transfers between an external device and memory; maximum transfer rate is 20,000 8-bit bytes per second. All peripherals except Teletype units and discs use the byte I/O bus; discs use the DMA channel and Teletype units use the TTY bus. The byte I/O bus can attach up to 32 devices; the DMA channel can handle 4 standard or 8 optional.

### Peripherals

**Low-Speed Peripherals.** The following peripherals are available.

- Teletype: ASR 33 with paper tape reader and punch, 10 characters per second.
- Paper Tape: Reader/punch reads 300 characters per second and punches 75 characters per second.
- Punched Card Reader: reads 300 cards per minute.
- Line Printers: 80 columns; 150 lines per minute for 80-column lines; 250 lines per minute for 132-column lines.

**Mass Storage.** Subsystems include both discs and magnetic tape units.

- 2853,4,5,6 Disc Systems (use 8000 Series Drives), 2.5, 5.0, and 10.0 million bytes; one removable or one fixed and one removable platter; single or double density recording; 75-millisecond access time (60-millisecond with fast access feature); transfer rate is 195,000 (312,000 with higher-speed feature) bytes per second over DMA channel.
- Magnetic Tape: up to four transports by way of one controller on byte I/O channel, transports can be selected from the following units: 7-9-track, 800 bytes per inch, 12.5 inches per second (10,000 bytes per second), 7-9-track, 800 bytes per inch, 25 inches per second (20,000 bytes per second). All transports on a controller must be the same types.

**Communications Devices.** A variety of interfaces are provided.

- Full-Duplex Synchronous Modem Interface and Control: (programmed, concurrent I/O and interrupt data transfer modes); rates up to 9,600 baud; EIA Standard RS232C interface.

- Synchronous Modem Interface with Auto Call/Answer Unit: full-duplex in the programmed transfer mode; half-/full-duplex in the concurrent I/O mode; rates up to 9,600 baud; EIA Standard RS232C interface.
- Asynchronous Communications Controller and Interface: programmed, concurrent I/O or interrupt on input character ready transfers at 110 to 9,600 baud rates; EIA Standard RS232C or 20-ma current loop interface to be specified at time of order.
- 4-Channel Communications Interface and Controller: simultaneous operation of 4 full-duplex asynchronous lines; each channel programmable for 75 to 2,400 baud; EIA Standard RS232C or Teletype 20-ma current loop interface.
- Eight-Channel Communications Interface and Controller: simultaneous operations of 8 full-duplex asynchronous lines; 75 to 2,400 baud; EIA Standard RS232C or 20-ma current loop interface.
- Modem/Communications Control: full-duplex 16 discrete inputs; 16 discrete outputs; EIA Standard RS232C interface.
- Automatic Call Unit Controller: controls up to 4 Bell Model 801 Automatic Call Units; EIA Standard RS232C interface.
- Eight-Channel Low-Speed Modem Interface: provides 8 full-duplex RS232B interfaces.
- Sixteen-Channel, Low-Speed Modem Interface: provides 16 full-duplex RS232B interfaces.
- Eight-Channel Teletype Control: provides 8 full-duplex 20-ma Teletype interfaces.
- Sixteen-Channel Teletype Control: provides 16 full-duplex 20-ma Teletype interfaces.

### MAINTENANCE

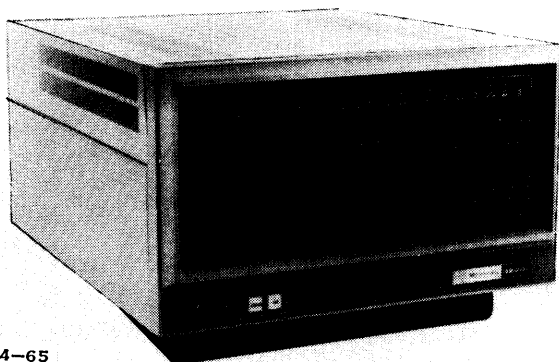
Microdata provides maintenance through 15 plant and service depots and sales offices located in all major cities in the United States.

### HEADQUARTERS

Microdata Corporation  
17481 Red Hill Avenue  
Irvine CA 92705

# MICRODATA CORP.

## 3200 Series System Report



74-65

### OVERVIEW

The Microdata 3200 is a 16-bit microprogrammable minicomputer aimed at both OEM and end-user markets. It consists of the microprogrammable 3200, 32/S, 32/S1, and the 32/S with MPL.

The 3200 is the bare hardware without a microprogram instruction set; no assembly-language level instruction set has been implemented. The 32/S is a complete computer with its architecture designed to make implementation of a compiler language easy. It is designed around a push down stack and a Monobus. The 32/S1 has an extended instruction set; floating-point doubleword arithmetic; string manipulation instructions and swapword in stack instruction set.

Programs are coded in MPL (Microdata Programming Language). MPL is a block-oriented, high-level language similar to PL/1. Currently, programs are cross compiled on an IBM System/360 with PL/1 compiler. A self-compiler implemented in firmware is scheduled for delivery in the first quarter of 1975.

The 3200 hardware modules are organized around a single fast "monobus" connecting all system components. The processor, memory, and peripheral devices operate as monobus subsystems that communicate with each other in a master-slave relationship. This type of bus-centered architecture permits connecting memory modules of different speeds to a system. In addition, the various memory modules and peripheral control cards can be attached in any order to monobus slots. Once initiated, data transfers between high-speed devices and memory can continue while the processor does other work. This architecture is similar to that of the GRI-99 and Digital PDP-11. The 3200 Series addresses peripheral devices as though they were memory locations; thus it has no separate set of I/O instructions.

Main memory can consist of 4K to 128K 16-bit words of MOS memory. The microprocessor utilizes 512 to 4,096 32-bit words of control memory, which can be read-only or a combination of read-only and read/write. Main memory cycle time is 450 nanoseconds for full read cycle; 350 nanoseconds for full write cycle; control memory cycle time is 135 nanoseconds. A high-speed hardware push-down stack, coupled with a look-ahead feature that queues the next software instruction in advance, acts like a cache memory to speed up processor throughput. Addressing is to the byte or word level.

The 32/S is a completely new system; it is not compatible with any system previously offered by Microdata. At present only the MPL cross compiler for the IBM 360, the 32/S self-compiler, and a rudimentary operating system called GENASYS are available.

Peripherals for all models of the 3200 Series are the same as those for Microdata's 800 and 1600 line.

The first 3200 Series system was delivered in January 1974, about 20 have been delivered to date, and over 40 are on order.

Table 1 contains a summary of the mainframe characteristics.

### COMPETITIVE ANALYSIS

The 3200 joins a growing number of minicomputers featuring microprogramming that can be extended by the user. The versatility of microprogrammed systems, as compared with earlier systems which implement assembly/machine language level instructions with "hardwired" logic, has led some industry observers to label microprogrammed systems "the fourth generation." Microdata has already had considerable experience with this type of system. Systems in the 800 and 1600 Series are all microprogrammed.

The 3200 Series combines high-speed, MOS semiconductor technology and a push-pop data stack with the inherent advantages of microprogramming. The stack-oriented Model 32/S, with its MPL language, is the first

### HEADQUARTERS

Microdata Corporation  
17481 Red Hill Avenue  
Irvine CA 92705  
(714) 540-6730

**Table 1. Microdata 32/S: Mainframe Characteristics**

<b>CENTRAL PROCESSOR</b>	
Type	Microprogrammed ROM
Control Memory Size of Memory	512-4,096 32-bit words
No. of Internal Registers	5 (hardware); 32K (memory)
<b>Addressing</b>	
Direct (no. of words)	128K
Indirect	Yes
Indexed	Yes
<b>Instruction Set Implementation</b>	
Number	Firmware 151
Decimal Arithmetic	Yes
Floating-Pt Arithmetic	Opt
User Microprogramming	Yes
Priority Interrupt Levels	10 int; 8-64 ext
<b>MAIN MEMORY</b>	
Type	MOS
Cycle Time ( $\mu$ sec)	0.35
Basic Addressable Unit	16-bit word
Bytes per Access	2
Min Capacity (bytes)	8K
Max Capacity (bytes)	256K
Increment Size (bytes)	8K
Ports per Module	1 (monobus)
Error Checks	Parity, 1 bit/byte
Protection Method	Opt
Memory Management	Firmware
ROM	Yes
Use	Firmware
Capacity	512-4,096 32-bit words
<b>I/O CHANNELS</b>	
Programmed I/O	Std
DMA Channels	Std
Multiplexed I/O (subchannels)	Opt
<b>Max Transfer Rate (wds/sec)</b>	
With Memory	2.5M
Over DMA	3.0M
Simultaneous Operations	Yes

model to implement some of the special advantages of this unique combination of characteristics. The resulting system should be of interest to end users who want to do their own programming, particularly when Microdata develops more supporting software.

Currently, a cross microassembler called "CAP 32" and written in PL-1, Level F and a cross MPL compiler for execution on IBM System/360 running under OS are available. An MPL self compiler is scheduled for the first quarter, 1975.

While the Model 3200 is of greatest interest to the OEM market, Microdata is marketing to end users as well. One of the first 3200s was bought by an end user, who attached it to a PDP-11 for high-speed repetitive calculations. Another is being used to control a high-speed printing operation. Microdata anticipates that most early users of the system will come from the University market.

Microdata has over 6,000 computers currently in operation, and most have been sold to OEMs. Microdata is working to attract more end users to its customer base.

In the past, a large majority of Microdata sales were to five customers, with one order accounting for over a third of total sales. To lessen the market vulnerability inherent in dependence on large accounts, Microdata hopes to extend its customer base so that no customer will account for more than 15 percent of sales.

Microdata also markets Reality, a small business system based on the 1600. For large companies, Microdata markets through its own staff while distributors handle sales to small end-user companies.

At the low end of the market, Microdata has the Micro-One microprocessor. It includes two total systems: a smart CRT terminal and an 8-channel programmable communications controller.

**COMPATIBILITY**

The 3200 and 32/S are not compatible with any other computer system in the Microdata line.

**CONFIGURATION GUIDE**

The basic 3200 system encompasses the CPU, main memories, and I/O controllers attached to a common asynchronous bus (the monobus). Units are mounted on printed circuit boards, three of which are used by the CPU control processor. Additional control memory boards are available. Main memory with power fail protect is supplied in 4K- or 8K-word modules to a 128K-word maximum. Four CPUs can operate on the same bus without overloading. MPL supports multiprogramming; moreover, all hardware is provided for communication between CPUs on a "handshaking" basis. Either a maintenance or an operator's console is included with the system. A battery option is available to maintain memory in case of power fluctuation.

The 32/S includes all the basic 3200 components plus the control memory to implement its architecture and instruction set. Maximum main memory within the CPU chassis is 128K words. System memory protect is an optional feature. An external real-time clock with a variable interval is standard.

Both rack and desktop chassis are available for the 3200. Front panel, power supply, cooling fans, and 16 card slots are included. The card slots are allocated as follows: one for the front panel, three for the processor (including control memory), one for the power supply, and one for each 8K-word main memory module or I/O controller. An expansion chassis for main memory modules and/or I/O controllers is optional. The power supply is integral and can maintain data during power irregularities. A battery pack is available for longer protection.

**MAINTENANCE AND SUPPORT**

Microdata has service and parts centers in major cities throughout the United States. Monthly maintenance contracts are available for all equipment marketed.



Maintenance for the 3200 Series is relatively simple. Any board can be plugged into any connector in the backplane. If a board needs service, it can be plugged directly into the first available connector. No extender boards are needed. Table 2 lists the peripheral devices that can be used with the system. Table 3 lists the available system software.

**Table 2. Microdata 3200 Series: Peripherals**

Model	Description
	<b>Discs</b>
3954	Cartridge, master, 1 fixed, 1 removable; 5M-byte capacity; access time: 35 msec; 1500 rpm
3961	Slave unit to 3954
3956	Same as 3964 but double capacity
3963	Slave unit to 3956
	<b>Magnetic Tape</b>
3815	9-trk, 800 bpi; master, NRZI; 25 ips
3835	9-track; 1,600 bpi, PE
3845	Slave units for 3835
	<b>Paper Tape</b>
3710	Reader/punch; 300-cps read/75 cps punch, Fanfold
3710-1	Same as 3710 but roller
	<b>Card Reader</b>
3721	200-cpm read, 20-col cards
	<b>Line Printers</b>
3733	132-col, 64 char, 300 lpm
3734	132-col, 96 char, 200 lpm
3737	132-col, 64 char, 60 lpm (165 cps)
	<b>Displays</b>
3751	CRT, 1920 char; 27 x 80 screen, 110-9,600 baud
	<b>Controllers</b>
1311	General-purpose I/O, 126 14 or 16 IC sockets
1314	Multipurpose I/O, 75-9,600 baud
1330	Async comm; full-/half-duplex, 75-9,600 baud
Terminals Supported	33 ASR, 33 KSR, 35 KSR, TTY, RS232C
	<b>Consoles</b>
Maintenance	18 pairs, register display, manual interrupt, program load
Basic	Load and interrupt buttons

**Table 3. Microdata 3200 Series: Software**

Package	Description
Microdata Programming Language (MPL)	A PL/1 type language used instead of assembly language
GENASYS/D	A simple, disc-based operating system that allows user program storage on disc
Cross Assembler	For IBM System/360 with PL/1, F level compiler

**TYPICAL PRICES**

Model Number	Description	Purchase Price \$
	<b>SYSTEMS</b>	
3251	32/S General Purpose System (Includes 3250-5 CPU, 16K-word memory with memory, 3015 programmer's console, single-bay cabinet, rack-mounting hardware, 3751 CRT system, 3815 magnetic tape system)	30,650
3252	32/S General Purpose System (same as 3251 except 3250-2 CPU, 32K-word memory, and 3954 disc system)	49,250
3252-1	32/S General Purpose System (same as 3252 except with double bay cabinet)	49,900
	<b>CENTRAL PROCESSORS AND WORKING STORAGE</b>	
3200-5	Microdata 3200 General Purpose Microprogrammable Computer (accommodates up to 2K 32-bit words of control memory, requires 3010 basic panel or 3015 system programmer's console)	6,300
3290-5	Microdata 3290 General Purpose Microprogrammable Computer (Same as 3200-5 except with 512-word control memory for firmware load, accommodates up to 1,536 more words of control memory)	6,750
3250-5	Microdata 32/S Stack-Architecture Microprogrammable Computer (with 2K 32-bit words of control memory; card cage with 12 available assembly slots)	8,050
3200	3200 Card Cage	5,800
1300	Main Memory Microdata MOS Memory Module	
1300-5	8K x 18 Bits, Parity	4,310
1300-6	4K x 18 Bits, Parity	2,930
1313-X	Control Memory Assemble (Requires 1 assembly slot) Accommodates up to 4,096 words of Programmed Read-Only Memory (includes 16 memory)	
	512 Words	700
	1,024 Words	715
	1,536 Words	730
	2,048 Words	745
	4,096 Words	805
3000-XX	ROM with Customer-Supplied Firmware (2) PROM:	
	512 Words	600
	1,024 Words	1,200
	2,048 Words	2,400
	4,096 Words	4,800
	<b>BROM:</b>	
	512 Words	300
	1,024 Words	600
	2,048 Words	1,200
	4,096 Words	2,400
1353	Writable Control Memory (WCM) (512 words, 32 bits)	3,000
3954	Disc System (including 100 tpi, 1,500 rpm; 5M bytes of storage)	10,000
3961	Add-On Disc Drive	7,250
3956	Disc System (200 tpi, 1,500 rpm; 10M bytes of storage)	11,000
3963	Add-On Disc Drive (includes fixed disc and removable cartridge)	7,700
3710 and 3710-1	Paper Tape System (consists of 300-cps reader, 75-cps punch)	4,630
3711	Paper Tape Reader System (300-cps reader)	2,500
3721-1	Card Reader (80-col, 200 cpm)	4,200
3733	Line Printer (132 col, 300 lpm)	10,500
3734	Line Printer (132 col, 96 char set, 200 lpm)	12,000
3733-1	12-Channel Vertical Format (VFU)	500
3737	Line Printer (165 cps, 132 cols)	5,800
	Magnetic Tape System (includes one 9-track tape) Speed, 25 ips	
3815	800 bpi	7,500
3835	1600	8,700
	Add-On Magnetic Tape Drive (9-track)	
3845-X	25 ips, 1600	4,700
	Terminals	
3751	CRT Alphanumeric Display and Keyboard Multipurpose I/O Interface (MPIO)	3,850
	<b>DATA COMMUNICATIONS</b>	
1330-1	Asynchronous Communications Controller	1,100

**Notes:**

- (1) Maintenance contracts on yearly or per-call basis. Cost calculated on per-diem basis for time, materials and travel.
- (2) One-time charge for production set-up of each 512-word page.





# MODULAR COMPUTER SYSTEMS

## MODCOMP II/2 System Report with MEMORY+ and New FORTRAN IV

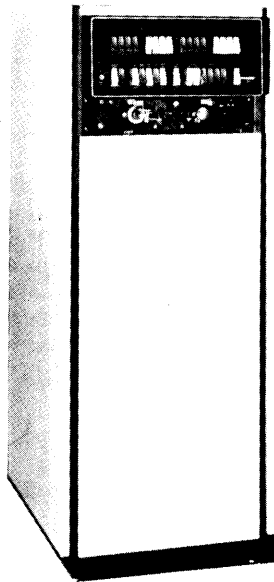


Figure 1. MODCOMP II/2, the low end of the line.

### OVERVIEW

The MODCOMP II/2, the thirteenth model in the II line, is the lowest entry level system. It is designed for small stand-alone applications and for use as a terminal processor in MODCOMP distributed processing networks. The II/2 supports 16K, 32K, or 48K bytes of MOS memory and can run all the standard MODCOMP software that can fit into the memory. Memory cycle time is 600 nanoseconds per word.

The II/2 implements the same basic instruction set as the rest of the II line, but floating point arithmetic and multiprocessor communication hardware are not available. The instruction set is implemented in a 256 40-bit word ROM with 200-nanosecond access time. Instructions are available for fixed-point arithmetic, logical operations, bit and byte manipulation, and interrupt and call, as well as the usual load/store, shift, branch, and input/output. Most instructions can select any of the 15 general-purpose registers for use. Memory referencing instructions can address all of memory directly.

### Input/Output

The input/output facilities include a party-line bus to transfer data between up to 63 devices and the general-purpose registers. The bus contains separate T2L input and output buses. It is compatible with the standard MODCOMP peripheral controller interface. The programmed I/O facility is normally used for interrupt-driven transfers although it can also be used with a polling technique.

A Direct Memory Processor (DMP) is standard. It implements eight data channels; each channel has a pair of 16-bit memory address registers to control block transfers. Thus, all channels can transfer data concurrently on a multiplexed basis. Maximum aggregate transfer rate via DMP is 185,000 words per second.

### Interrupt System

The CPU includes an eight-level interrupt system:

- Two input/output levels; each level can have 63 sub-levels.
- Task Scheduler used by Real-Time Executive of MAX III to maintain a software queue below hardware queue.
- Console Interrupt signaled by switch on console.
- Unimplemented Instruction Trap, always enabled and used to call subroutines to perform unimplemented instructions.
- Real-Time Clock interrupt occurs at 5-millisecond intervals.
- Two external interrupt levels.

A control panel to display and enter data into memory and registers and for program fill, master clear and console interrupt is optional. Remote fill is standard.

Table 1 summarizes the mainframe characteristics.

### HEADQUARTERS

MODULAR Computer Systems  
1650 West McNab Road  
Ft Lauderdale FL 33309  
(305) 974-1380

# MODULAR COMPUTER SYSTEMS — MODCOMP II/2 SYSTEM REPORT WITH MEMORY+ AND NEW FORTRAN IV

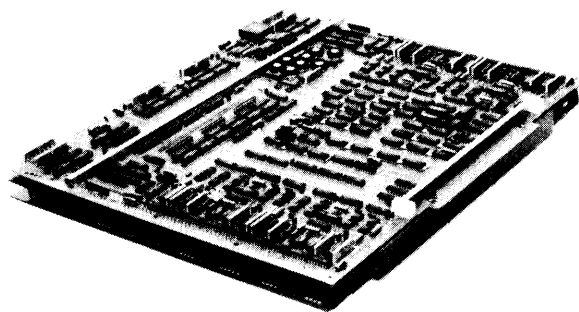
**Table 1. Modular Computer Systems:  
MODCOMP II/2 Mainframe Characteristics**

<b>CENTRAL PROCESSOR</b>	
Microprogrammed	Yes
Stack Processing/Context Switching	No
No of Programmable Registers	15
No of Inst	165
Inst Execution Times	
μsec	
Add/Subtract	2.0 <sup>1</sup>
Multiply	10.2 <sup>1</sup>
Divide	11.2 <sup>1</sup>
Addressing Modes	Direct, indirect, indexed, indexed & indirect, immediate, short displaced, short indexed
Priority Interrupt Levels	8, up to 128 sublevels
<b>MEMORY</b>	
Cache	No
Types	Mos
Word Length, bits	16 + 1 parity
Cycle Time/word, μsec	0.6
Capacity, words	
Min	8K
Max	24K
Increments	8K
Checking	Parity
Protection	No
<b>INPUT/OUTPUT</b>	
Max No of Devices	63
Programmed I/O Channel	Yes
Multiplexed I/O Channel	No
Direct Memory Access (no of channels)	8
Max DMA Transfer Rate (words/sec)	185,000

— Not applicable

1. Using memory to register format instructions.

## MEMORY +



76-142

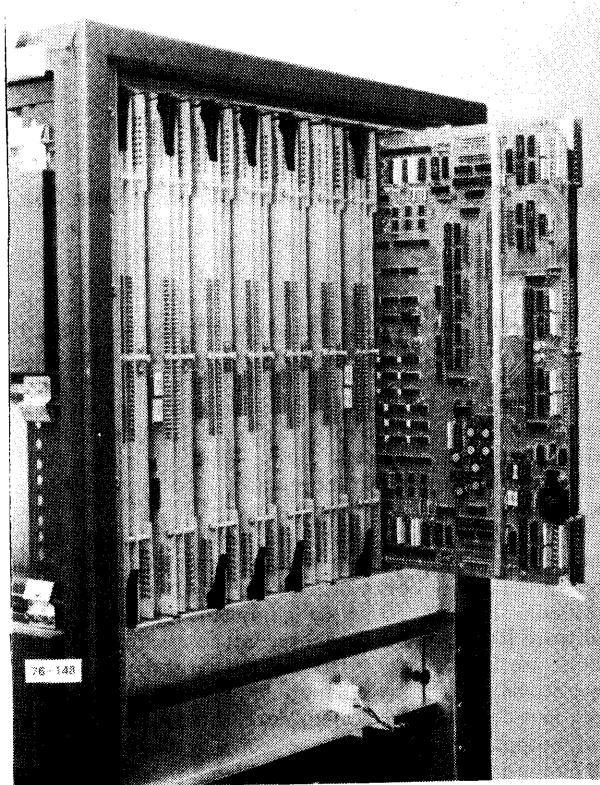
**Figure 2. MODCOMP MEMORY+, 256K-byte core module**

The new MEMORY+ is a bulk core file replacement for fixed-head disc storage. It is used for applications where the program swapping time to and from discs is a bottleneck to throughput. According to MODCOMP, benchmarks show MEMORY+ files can improve throughput by factors of 10 to 20 for certain applications.

A MEMORY + file consists of one to eight modules of 256K bytes of core memory, packed on two 128K-byte boards hinged together into one package. Each storage chassis has its own power supply and can store up to eight modules for a capacity of 2M bytes. Each file can support an extension chassis which can also support up to eight 256K-byte modules. Thus, each Bulk Core Device has a storage capacity of 4 million bytes. A MODCOMP II or IV computer can support up to four Bulk Core Devices for a maximum capacity of 16 million bytes. Bulk core file modules can be either two- or four-way interleaved. Cycle time is 1.5 microseconds per word. Two-way interleaving reduces effective cycle time to 0.8 microseconds.

Either one or two controllers can be used to access the Bulk Core Device memory. Thus, two processors can share a common Bulk Core Device. Access time is 1 microsecond following initiation. Data can be transferred at a rate of 3 to 4 megabytes per second on MODCOMP IV computers. For models without a separate memory port, data is transferred at the channel rate. The Bulk Core Device connects to the processor via a DMP channel.

MEMORY+ can be added to any Model II or IV computer with no change to the software. The fixed-head disc I/O handler can be used unchanged to access blocks of data stored in core the same way as disc storage. Thus, Bulk Core is divided into words, sectors, tracks, modules, files, and devices. There are 128 words per sector, 32 sectors per track, 32 tracks per module, eight modules per file, and four devices per CPU.



**Figure 3. MODCOMP MEMORY+ core memory file, 2.048M bytes capacity**



## New FORTRAN IV

A new FORTRAN IV compiler will be incorporated into the new releases of the operating systems. It improves compile and execution times by as much as 60 percent according to a MODCOMP spokesman. It offers full ANSI X3.9-1966 FORTRAN plus extensions.

## Competitive Position

The MODCOMP II/2 will undoubtedly replace the II/10 because the II/2 offers a considerable price performance advantage over the older model. This will reduce the number of II Models back to 12, a good move not so much because 13 is an unlucky number but because 13 models are quite a few to offer.

Table 2 shows that the II/2 in small configurations is less expensive than a comparable NOVA 3, but it is more expensive than the Digital PDP-11/04 and the GA-16/110. Also, the II/2 can not support floating point hardware while the NOVA 3 and GA-16/110 can. MODCOMP has deliberately crippled the system to narrow the marketing focus for the system. It will be marketed for remote processing in a network and may run unattended for real time applications. Thus, the standard remote fill feature. Networking will attract a sizable market because it is MODCOMP's largest business, representing about 60 percent of the gross sales. The II/2 can also be used in small stand-alone configurations for applications that do not require the power of the larger processors. The II/2 is a competitive system that is undoubtedly needed to round out MODCOMP's networking facilities.

The MEMORY + should be a boon to users operating in a multiprogramming, virtual memory environment and running at full capacity. This should be as painless an upgrade as anyone can make. MEMORY + costs about twice as much as disc storage but about half as much as

main memory. If it does indeed increase throughput by a factor of 10 or 20, it should be a bargain.

MODCOMP has joined in the recent race manufacturers seem to be making to improve their FORTRAN compilers. Digital recently introduced the PDP-11/55 with bipolar memory for fast FORTRAN program execution. Data General has long had an optimizing compiler. Other manufacturers such as Interdata are working on them. A 60 percent improvement in compilation and execution time is quite significant in the heavy FORTRAN world of minicomputers.

## PRICE DATA

Model	Description	Purchase Price \$
<b>MODCOMP II/2</b>	Central Processor with semiconductor memory with parity in 8.75-in vertical rack with power supply and slots for 6 peripheral controllers	
II/2	With 8K wds of memory	3,995*
II/2-1	With 16K wds of memory	5,095
II/2-2	With 24K wds of memory	6,195
<b>MEMORY +</b>	Operator's Control Panel	750
	Controller and one 256K-byte core memory module with space for 7 add'l modules	20,000
	Add'l 256K-byte core memory module	10,000
	Expansion chassis and one 256K-byte core memory module with space for 7 add'l modules	15,000
	Controller for dual access to memory	5,000
<b>FORTRAN IV</b>	Will be incorporated in new releases of the operating systems	No Chg

Notes:

\* \$2,995 each when included with order of \$500,000.

**Table 2. MODCOMP II/2: Comparison with Major Competitors**

	MOD COMP II/2	Data General Nova 3	Digital PDP-11/04	GA-16/110
Word Length (bits)	16 + 1 parity	16/16 + 1 parity	16	16/16 + 2 parity
Inst Times (μsec)				
Add	2.0	1.8 <sub>2</sub>	3.2	2.5
Multiply	10.2	6.9 <sub>2</sub>	NA	21.0
Divide	11.2	7.5 <sub>2</sub>	NA	20.0
Floating Pt Add	—	7.7*	—	*
Floating Pt Multiply	—	11.3*	—	*
Floating Pt Divide	—	13.7*	—	*
Max Memory (bytes)	48K	64K/256K	56K	128K
No of GP Registers	15	4	8	16
Max DMA Rate (bytes/sec)	370,000	2M	2.8M	2M
Price, \$				
CPU + Memory				
16K bytes	3,995	4,500	3,295 <sup>3</sup>	3,160
32K bytes	5,095	6,100	(3)	4,400
64K bytes	—(1)	10,800	(3)	—

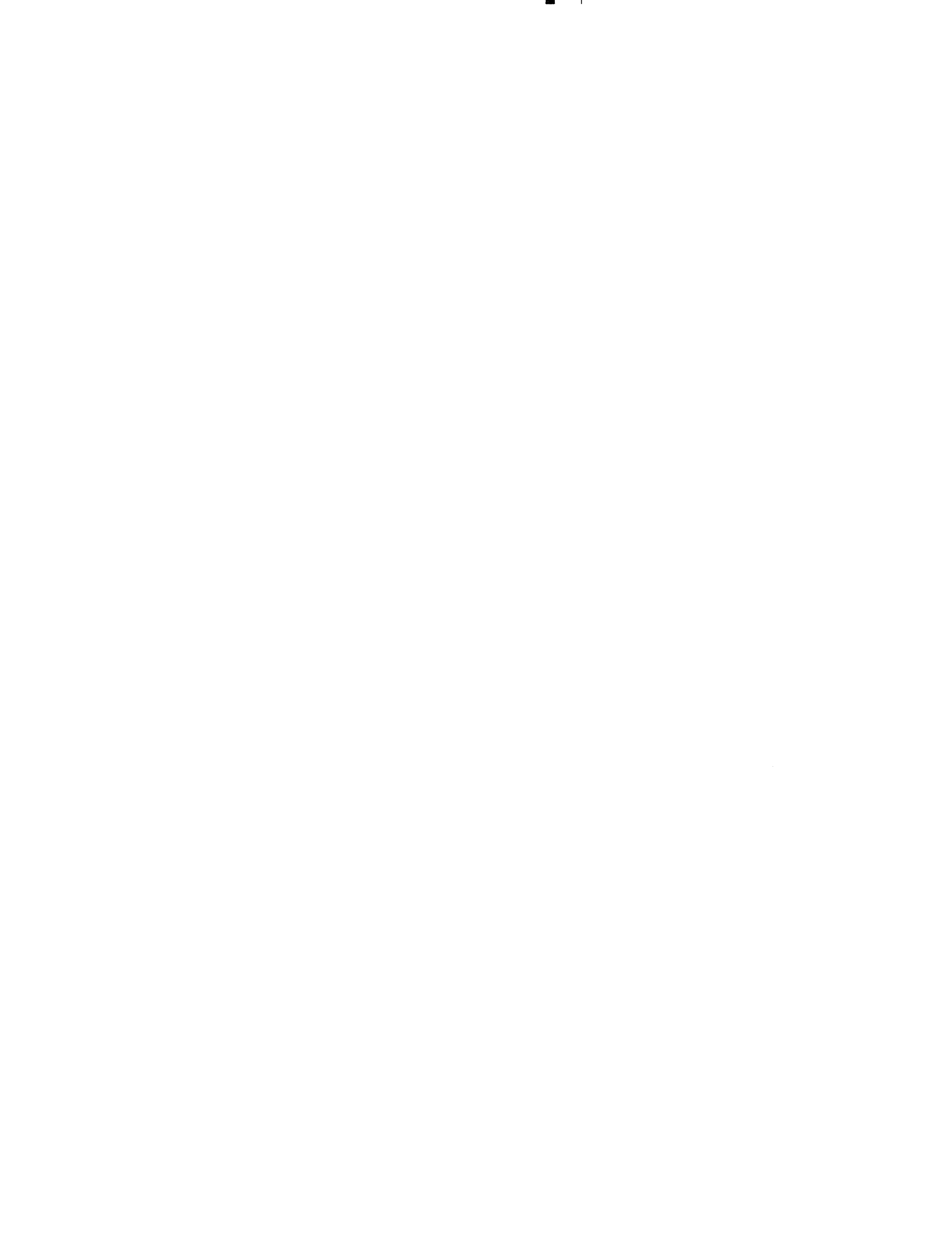
Notes:

\* Optional, at extra cost.

1. Maximum memory is 48K bytes; the II/2 with 48K byte memory is \$6,195.

2. Unsigned integer multiply and divide are standard.

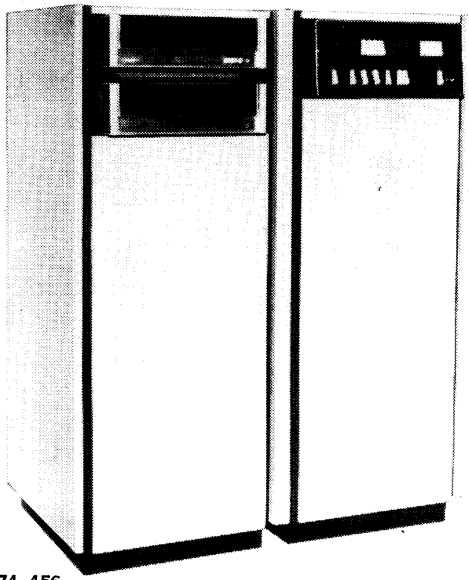
3. Chassis has only two slots available for peripheral controllers; system with chassis that has seven slots available costs \$3,545.



# MODULAR COMPUTER SYSTEMS

MODCOMP I, II and IV

AUERBACH Buyer's Guide to . . .  
MINICOMPUTERS



74-456

## OVERVIEW

The MODCOMP computers are a family of highly modular, microprogrammed 16-bit-word machines with an assortment of RAM, ROM, and core memories that have an 0.8- or 1.0-microsecond cycle time per word. Three basic computers are offered: MODCOMP I, II, and IV, each capable of extensive expansion.

A variety of model numbers have been assigned to configurations that include various subsets of the available features and system options: I/5 and I/15; II/5, II/10, II/20, II/25, II/25 MCP, II/45, and II/45 MCP; IV/5, and IV/25. The II is also available in two system configurations, II/200 and II/220, that support the MAX III operating system. Modular has also developed a 32K-word core memory module that is mounted on one board; six new MODCOMP II computer models have been developed around the new board: II/12, II/26, II/26CP, II/201, II/221, and II/231. All models can be upgraded to higher models by adding options, except that 0.8-microsecond systems cannot use the new 1.0-microsecond 32K-word memory boards. The model package is less expensive than a lower model system that has been expanded in the field.

MODCOMP computers serve in widely varied applications. MODCOMP I was specifically designed as a small dedicated controller for real-time measurement and control functions. It can also operate as a stand-alone processor with a full complement of peripheral devices. The MODCOMP II is a general-purpose computer for measurement, control, communications (MCP models), and information processing.

The MODCOMP IV, which is upward compatible with the I and II, is a dual-word processor with a memory capacity of 262,190 16-bit words (512K bytes). Because of

its dual-word orientation, MODCOMP IV can compete with 32-bit machines for many applications. The first MODCOMP IV was delivered in September 1974.

Modular Computer Systems offers a broad range of software for its computers. Packages available for MODCOMP I includes MAX I Executive, four assemblers, relocatable and link loaders, link editor, utilities, diagnostics, and communication line and remote data acquisition handlers.

MODCOMP II software includes three versions of the MAX III real-time operating system, as well as MAXCOM, MAXNET, Real-Time FORTRAN IV, three assemblers, BASIC, and Real-Time BASIC. Utility processors include a debug executive, source update, source maintenance control, library update, link editor, cataloger, and direct access maintenance processor. MAXNET is a newly announced operating system designed for distributed processing, while MAXCOM is a communications run-time system with low overhead.

MODCOMP IV software includes all the software for Models I and II, plus the MAX IV Real-Time Multiprogramming System (designed specifically for MODCOMP IV), extended BASIC, and RPG II. Machine support software incorporates a file management system, a sort/merge package, and a media-to-media conversion package. Several bisynchronous communication dialects, as well as a remote job entry capability, are available. Table I lists the mainframe characteristics.

The MODCOMP II was first announced in 1970 followed by the I in 1971, the II in 1972, and the IV in 1973. The III is no longer actively marketed.

## PERFORMANCE AND COMPETITIVE POSITION

MODCOMP has an enviable record; it has doubled its sales each year since its founding in 1970 (a period noted for uncertain economy), and the company has consistently been ahead of sales forecasts. To date, Modular has delivered over 1,000 systems, the typical system currently shipped includes 48K words of core memory. Modular has been a quiet competitor that has never participated in the raucous fighting for the low end of the minicomputer market.

From 50 to 60 percent of new orders are from Modular customers. The company tries to stay out of markets where low price is the main criterion for an order. Instead, it seeks markets where no other company can do what Modular does.

However, as minicomputer manufacturers look for new markets to sustain their phenomenal growth rates, Modular Computer Systems, with its gross sales of \$25,000,000 this year, will not be able to hide. When the company branches out into territories already served by Data General, Digital Equipment, and Hewlett-Packard,

Table 1. MODCOMP I, II, and IV: Mainframe Characteristics

MODEL			
<b>CENTRAL PROCESSOR</b>			
Type	Microprogrammed	Microprogrammed	Microprogrammed
Control ROM	Yes	Yes	Yes
No. of Internal Registers	3	16	Up to 16 sets of 16
Addressing			
Direct (no. of wds)	256	256	256
Indirect (no. of wds)	32K	64K	64K
Indexed	Yes	Yes	Yes
Instruction Set			
Implementation	81	106	242
Number (std, opt)	81	106-176	242
Floating Point	No	Opt	Opt
User-Microprogramming	No	Opt	Opt
Priority Interrupt			
Levels	2; 2*	4; 6*	8; 16*
Sublevels	16	64	64
<b>MAIN STORAGE</b>			
Types	Core; solid state	Core	Core
Cycle Times (μsec)	0.8	0.8 or 1.0	0.64
Basic Addressable Unit	Byte; word	Byte; word	Byte; word
Bytes/Access	2	2	2
Cache Memory	No	No	No
Capacity (min/max bytes)	4K-64K	8K-128K*	8K-512K*
Increment Size (bytes)		8K; 16K; 32K; 64K	
Ports/Module	1	1 std; 4 opt	1; 2; 4
Protection	—	Opt*	Opt*
Memory Management	No	No	Opt*
Error Checks	—	Parity option	—
ROM	1K; protect	No	No
<b>INPUT/OUTPUT</b>			
I/O Channels			
Programmed I/O	Std	Std	Std
DMA	Opt	Opt	Opt
Multiplexed	Opt	Opt (8-channel)	Opt (2-channel)
Max Transfer (wd/sec)			
Within Memory	135; 270	135; 270	769; 231
Over DMA	—	1,250,000	1,562,500
Over DMP	300K	300K	300K

\* Depends on submodel or option.

the competition will be rougher. All the major manufacturers are going after the markets for substantial minicomputer systems: Digital with its PDP-11/40, 11/45, and 11/50; Data General with its ECLIPSE; and Hewlett-Packard with its 21MX and 3000. Other competitors are General Automation SPC-16, Interdata 7/16 and 7/32, Microdata 3200, Xerox 530, and CDC System 17.

The manufacturers of all these systems recognize that real-time, on-line applications and network processing fit the traditional minicomputer environment better than the batch environment exploited so long by the large mainframe manufacturers. The real-time operating systems with foreground/background processing were developed for real-time control applications, test and measurement, and data acquisition. The demands made by these real-time applications for on-line program development, backup to avoid downtime, fast response times, and program protection are the same ones now required for real-time, on-line commercial processing.

All the minicomputer manufacturers are scrambling to get a firm place in the market before the large mainframes can become on-line transaction oriented. Furthermore, the large mainframe manufacturers not

only expect larger markups on their system prices than minicomputer manufacturers; they cannot yet compete on a price/performance basis with minicomputers.

Modular's spectacular success proves the validity of its goals. Its system and software orientation has worked. Still, the pressure on the low end of the minicomputer market from microprocessors and the saturation of the market to sophisticated end users have forced all serious minicomputer manufacturers to become system- and software-oriented. Thus, Modular will have to try harder if it is to continue its winning ways as an unquiet competitor.

MODCOMP IV's double-precision instruction set appears to make the system considerably faster than the PDP-11/40 and ECLIPSE for fixed-point double-precision arithmetic. The IV's floating-point hardware, on the other hand, is no faster than the floating-point hardware for the PDP-11/40 and is slower than the new unit for Data General's ECLIPSE. The main area where the IV appears to be at a competitive advantage over these other two systems is in its I/O channel arrangement and multiple ports to memory. Since MODCOMP IV can have up to four memory ports per module, the effective I/O transfer rate can be 3.75 million words per second without degrading processor throughput.

Because of its low price, systems built around MODCOMP's new memory board cost 18 to 27 percent less than comparable configurations using 16K-word boards. The 32K-word module is also substantially more reliable than two 16K-word modules; it has less components and less interconnectors to fail. The MTBF is expected to be 60,000 hours. Currently, the new memory module is available for MODCOMP II only; it will be available for the IV later.

Modular sees Hewlett-Packard as its strongest communications competitor. The Hewlett-Packard 9700 Distributed Processing System is most similar to MAXNET III. Data General's ECLIPSE system also has well-developed software and hardware facilities for distributed processing systems.

## USER REACTIONS

Users interviewed included two OEMs as well as six end users. All customers except one end user are extremely satisfied with their systems and would buy more MODCOMP computers. The one user who had trouble with his system reported less than 10 percent downtime. His system has equipment built especially for the application; it had a few faulty chips, an I/C that was too fast for the application, and a fluke in a multiplexor design which caused trouble during test but not in normal operation. This user, however, is buying three more systems.

Other users feel the architecture is good, the hardware reliable, and the software powerful. One user who is not computer oriented mentioned that MODCOMP FORTRAN allows him to program the system interface to his process control hardware. Most users, including the two OEMs, consider MAX III an excellent base operating system. One OEM who uses the II/25 adds an uninterruptible power supply that keeps current within two percent of ideal; the systems have been installed for several months with no failures.

Several users mentioned that it is easy to interface non-standard devices to the MODCOMP computers. One user selected a MODCOMP computer because an adapter to interface it to a CDC 6000 system is a standard product. This company has a MODCOMP III, another III on order, and a MODCOMP I. It plans to add 30 or more MODCOMP computers in the future.

Our interviews indicate that Modular Computer Systems maintains a good relationship with its users. Most either expressed an intent to buy more MODCOMP computers or said they would buy another MODCOMP system when needed.

## CONFIGURATION GUIDE SYSTEM DESIGN

MODCOMP I is available in two models: the bare-bones I/5 and the I/15 for larger configurations. Model I/5

can be field upgraded to a I/15. The I/15 includes the arithmetic unit, general register file (three registers), modular bus control interface, priority interrupt system with two levels (16 sublevels each), basic control panel, memory expansion to 32,768 words, power supplies and an 8¾-inch rack-mountable enclosure.

The I/15 incorporates the following features in addition to the I/5 features: an option plane with power for two optional features (multiply/divide, custom macro instructions, direct memory processor, Teletype and paper tape reader controller, and asynchronous data modem interface); hardware fill; real-time clock; Teletype controller; I/O connector assembly; and mounting slides.

Memory for either the I/5 or I/15 system can consist of up to 32K words, composed of core, solid-state RAM, solid-state ROM modules, or a combination of all three types. Core is available in modules of 2K, 4K, 8K, and 16K words. RAM is available in 2K-word modules only. ROM is available in 512-word modules only. Memory parity of the bit per byte is optional. Cycle time for all memory is 0.8 microsecond per word.

A power failsafe and auto-start feature is optionally available for either system. With the direct memory processor for automatic block transfers, the system can handle up to eight peripheral devices concurrently for an aggregate maximum transfer rate of 300K words per second.

Peripherals include a variety of high-speed, low-speed, process I/O, and communications attachments as listed in Table 2. Table 3 lists the hardware configurations required by the major software packages.

MODCOMP II is available in 15 versions, which can be roughly grouped into minimum, MAX II, MAX III, and communications configurations. Nine models use 0.8-microsecond memory modules like those on the MODCOMP I, and six models use the new 1.0-microsecond 32K-word boards. Each model represents a different configuration package, which is priced lower than a bare-bones system with all options added in the field. Table 4 shows the components of each submodel.

A minimum configuration (II/5) includes an arithmetic unit, a read-only control memory, a general register file (15 registers), register I/O and three interrupts (two I/O and unimplemented instruction trap), hardware fill, an operator console, memory expansion to 32K words, power supplies, and an 8¾-inch rack-mountable enclosure.

Four external priority interrupts are options with all models. All features are standard for a model, except maximum memory capacity and different speed memory modules, which are optionally available for the other systems. All peripherals available for MODCOMP I can be used on the II.

**Table 2. MODCOMP I, II, and IV: Peripherals**

DEVICE MODEL	DESCRIPTION
<b>Discs</b>	
4102-4103	Fixed-head discs; 128K-, 256K-, 512K-wd capacities
4106	Fixed-head discs; 1M capacity
4108	Fixed-head discs; 384K-wd capacity
4126/4127	1M-wd moving-head discs; 97.8K wds/sec transfer
4128/4129	2M-wd moving-head discs; 97.8K wds/sec transfer
4132/4133	12M-wd moving-head discs; 156K wds/sec transfer
4134/4135	26M-wd moving-head discs; 156K wds/sec transfer
<b>Magnetic Tape</b>	
4148/4151	9-trk; 800 bpi, 45 ips
4149/4152	7-trk; 556/800 bpi, 45 ips
4155	9-trk; 1,600 bpi, 45 ips
4160/4162	9-trk/7-; 12.5 ips
<b>Keyboard</b>	
<b>Printers</b>	
4233-4235	ASR 33; KSR 35; ASR 35 respectively; local
4223-4225	ASR 33; KSR 35; ASR 35 respectively; remote
<b>Paper Tape</b>	
4511/4513	625-cps readers
4512	625-cps reader and 110-cps punch
<b>Cards</b>	
4411/4412	300/1,000-cpm readers
4421	100-cpm punch
<b>Printers</b>	
4211/4214	600/300 lpm; 132-col
4213	50-150 lpm; 132-col
<b>Process I/O</b>	
1200/1500	High-level analog input subsystem; single-ended/differential input
1300	Wide-range analog input subsystem, to 512-channel bipolar signal
1400	Wide-range relay analog input subsystem, to 512-channel bipolar system
1500	Modular data acquisition subsystem; 7 I/O modules
1199	Modular I/O interface subsystem to 16 (16-bit) channels
<b>Communications</b>	
1906	Universal controller (2/system) for 4-32 full-duplex channels
1905	Async controller (4/system) for 2-32 full-duplex channels
5710	Freestanding process data terminal
1115/1116	Async comm interfaces; 110-9,600 baud; 1 half-duplex channel
4810/4811	Async comm interfaces; 75-9,600 baud; 2 full-duplex channels
1911/1912	Async comm channels 2 full duplex lines
4825	Sync comm interface; 110-20K baud; 2 full-duplex channels
4820	16-bit parallel computer link; 100K wds/sec
5813	Async interface with remote fill hardware; 75-9,600 baud, 1 duplex channel
5820	High-speed computer link; 15K-125K wds/sec; 2 half-duplex channels and remote fill

MODCOMP IV Dual Word Processor Computer is marketed in two basic configurations: the IV/10 and the

**Table 3. MODCOMP I, II, and IV: Software**

Device Model	Description
MAX I	Core-resident batch system; requires 4K words of memory, ASR 33; for MODCOMP I
MAX II	Core for disc-resident batch system; requires multiply/divide, 12K words of memory, ASR 33, binary I/O device/paper tape, card, or mag tape; disc version requires DMP channel and 128K-word disc; for MODCOMP II or III
MAX III	Real-time multiprogramming system with foreground/ middleground/ background modes; foreground requires CPU multiply/ divide, 12K words of memory, ASR 33 console; background needs protect and 24K memory; disc version requires 128K disc; extended disc version requires 24K words of memory, 256K words disc; for MODCOMP II or III
MAX IV	Mapped version of MAX III for up to 256K words, (4 maps); requires MODCOMP IV CPU, 24K words of memory, 2.5M disc, ASR 33
MAXCOM	Communications run-time system for high throughput, low overhead; requires 4K words of memory, communications interfaces
MAXNET	Distributed network operating system; requires CPU, 32K words of memory, disc, ASR 33, communications links to satellite CPUs; for MODCOMP II
Assemblers	Standard requires 2K words of Memory and ASR 33; Extended requires 4K words of memory, real-time clock, and ASR 33; Macro requires 12K-word memory and II or IV CPU
Cross Assemblers	IBM 360/370, CDC 6000; both require 65K bytes of memory, card reader, line printer, card punch, disc or mag tape
FORTRAN IV	ANSI 2.9 1966; requires CPU, 20K words of memory, console
BASIC	Subset of macro assembler; generates absolute or relocatable code; also multiterminal Extended version; requires 12K memory, ASR 33
Utilities	Diagnostics, editing, media conversion loaders, debugging, math library

IV/25. The IV/10 consists of a 32-bit and 16-bit arithmetic unit with multiply and divide hardware, a 32-bit parallel bus, executive features (real-time clock, console interrupt, and task scheduler interrupt), 15 general-purpose registers, a priority interrupt system with eight levels (expandable to 16 levels), 32K bytes of core memory with an effective cycle time of 640 nanoseconds for 16-bit words and 1.2 microseconds for 32-bit words, memory parity, memory expansion to 128K bytes with one, two, or four ports to memory, a power failsafe/auto start, control console, and a stall alarm.

**Table 4. MODCOMP II: Submodels**

SUBMODELS	5	10	20	25 25CP	45 45CP	200	220	12	26, 26CP	201	221	231
<b>MEMORY</b>												
Capacity												
Min K Bytes	8	32	8	32	32	64	64	64	64	64	64	64
Max K Bytes	64	64	128	128	128	128	128	128	128	128	128	128
Increments (K bytes)	8/16/ 32	8/16/ 32	8/16/ 32	8/16/ 32	8/16/ 32	8/16/ 32	8/16/ 32	64	64	64	64	64
Cycle ( $\mu$ sec)	0.8	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0
Parity	—	Std	—	Std	Std	Std	Std	Std	Std	Std	Std	Std
Protect	—	—	—	—	—	Std	Std	—	—	Std	Std	—
Ports	1	1	1	1	4	1	1	1	1	1	1	1
CPU												
Multiply/Divide	—	—	—	—	—	Std	Std	Std	Std	Std	Std	Std
INPUT/OUTPUT												
DMA	—	—	—	—	—	Std	Std	—	Std	Std	Std	Std
Modular Bus Control	—	—	—	—	—	—	—	—	—	Std	Std	Std
Peripheral Control	—	—	—	—	—	Std	Std	—	—	—	—	Std
Communications Macros	—	—	—	On CP	On CP	—	—	—	On Cp	Std	Std	—
Universal Communications	—	—	—	—	—	—	—	—	—	—	—	Std
MUX												
MUX Control	—	—	—	—	—	—	—	—	—	—	—	—
Console/Paper Tape	—	—	—	—	—	Std	Std	—	Std	Std	Std	Std
Disc	—	—	—	—	—	—	Std	—	—	—	Std	—

The IV/25 has all the features of the IV/10 plus 16 sets of general-purpose registers (16 registers per set) and a memory management system permitting expansion to 512K bytes, which includes 1,024 memory mapping registers organized in four files of 256 registers, automatic memory allocation hardware, and memory protect on the basis of a 256-word page.

Optional features for the IV include 32K-byte modules of core memory, a simultaneous direct memory processor for up to 12 device controllers, an extended arithmetic unit for floating-point arithmetic (32-bit, 48-bit, and 64-bit operands), system protect compatibility with MODCOMP II, and 3-level increment of external interrupts.

Dual II and IV processors can share common core modules by way of the multiple port option. Special system products are available to link a MODCOMP computer to a CDC 3000 or 6000 by way of the CDC 3000 data channel, or to an IBM System/360 or 370 selector or multiplexor channel. Peripheral controller switches are also available for program or manual switching of up to four controllers between two MODCOMP computers.

The 32K-word memory module and the MAXNET IV communications package are under development for the IV.

## COMPATIBILITY

MODCOMP systems are upward compatible in both hardware and software. The same functional hardware

modules and the same peripheral devices are used in all systems. All programs are upward compatible.

In addition, programs assembled on large MODCOMP II, III, or IV configurations can run on small MODCOMP II or III configurations because unimplemented instructions are trapped and simulated by subroutines. Programs assembled on MODCOMP II or IV using the MODCOMP I instruction set can run on MODCOMP I.

FORTTRAN-coded cross assemblers allow compilation of MODCOMP programs on the IBM System/360 and System/370 computers.

## MAINTENANCE

Modular Computer Systems has 14 sales and 21 service centers located in the United States, Canada, and Puerto Rico. European headquarters are in Surrey, England, with marketing also in Germany. The company plans to expand its marketing organizations in Europe, Canada, and South America in fiscal 1975; currently only 15 percent of sales are from customers outside the United States.

Modular Computer does not rent systems. The company has four maintenance plans for purchased systems: resident service, full service, scheduled maintenance, and on-call. Resident service provides a trained service engineer on a 1-shift basis. Full service provides both scheduled and on-call emergency services for a single fee, while the other two plans are priced separately.

# MODULAR COMPUTER SYSTEMS — MODCOMP I, II, AND IV

## PRICE DATA

Model Number	Description	Purchase \$	Monthly Maint. \$
<b>CENTRAL PROCESSORS AND WORKING STORAGE</b>			
<b>MODCOMP I</b>			
I/5	General-Purpose 16-Bit Digital Computer	2,000	16
I/15	General-Purpose 16-Bit Digital Computer (same as I/5 except includes 3130 option plane, 3742 hardware fill, 3743 real-time clock, 3751 Teletype controller, 3750 control panel interface, 3131 programmer's control panel, 0011 I/O connector assembly, 0010 mounting slides)	3,600	25
I/25	General-Purpose 16-Bit Digital Computer (same as I/15 except with 16,384-word memory module; memory parity; power fail-safe/auto start)	7,400	64
	I/5 and I/15 Memory (max 32K)		
	Read/Write Core Memory (0.8- $\mu$ sec cycle time)		
3603-1	4,096 Words	2,400	12
3608	8,192 Words	4,200	21
3609	16,384 Words	6,500	33
3607	Memory Parity	500	3
	I/5 and I/15 Processor Options		
3504	Multiply/Divide	700	4
3505	Custom Macro Instructions (requires 3130)	NA	NA
	MODCOMP I Input/Output and Interrupt Options		
0010	Slides for MODCOMP I Enclosure (for I/5 only)	70	NA
0011	I/O Connector Assembly	60	NA
3130	Option Plane	200	1
3131	Programmer's Control Panel	250	2
3709	Direct Memory Processor (requires 3130)	1,000	5
3741	Power Fail-Safe/Auto Start	300	2
3742	Hardware Fill	400	2
3743	Real-Time Clock	300	2
3750	Programmer's Control Panel Interface	150	1
<b>MODCOMP II</b>			
II/5	General-Purpose 16-Bit Digital Computer (with 16,384-word memory included)	9,500	8
II/10	General-Purpose 16-Bit Digital Computer (same as II/5 except has multiply/divide; power fail-safe/auto start; memory parity; priority interrupts for executive features; executive features; and 16,384-word memory)	11,500	93
II/12	General-Purpose 16-Bit Computer (same as II/5 except 32K-word memory; arithmetic unit; ROM; memory expansion to 64K words; gen reg file with 15 regs; reg I/O and 8 interrupts; multiply/divide; power fail-safe/auto start)	13,000	
	With 64K-Word Memory	21,000	
II/20	General-Purpose 16-Bit Digital Computer (same as II/5 except modular bus control interface and memory expansion to 65K words)	5,000	50
	With 16,384-Word Memory Included	10,000	83
II/25	General-Purpose 16-Bit Digital Computer (same as II/20 except has multiply/divide; power fail-safe/auto start; memory parity; interrupt levels for executive features; executive features; and 16,384-word memory)	12,500	95
II/25/CP	Communication Processor (same as II/5 with 3513 communication macros and modular bus control logic)	16,000	130
II/26	General-Purpose 16-Bit Computer (same as II/12 with modular bus control interface and controller for both console and p tape reader; expandable for high-performance floating-point processor)	16,000	
	With 64K-Word Memory	24,000	
II/26CP	General-Purpose 16-Bit Computer (same as II/26 with communications macros and modular bus control logic)	20,500	
	With 64K-Word Memory	28,500	
II/45	General-Purpose 16-Bit Digital Computer (same as II/25 with Controller for Teletype and p tape reader; executive features)	16,500	135
II/45/CP	Communications Processor (same as II/45 with communication macros and modular bus control logic)	20,000	170
II/200	Computer System (II/25 CPU with 32,768 words of 800-nsec memory; CPU options required to support MAX III together with a PCI)	19,500	148
II/201	Computer System (same as II/26 with peripheral controller interface enclosure, direct memory processor, system protect; 1 cabinet included)	16,500	
	With 64K-Word Memory	24,500	
II/220	Computer System (II/25 CPU with 32,768 words of memory; options to support MAX III, PCI; moving-head disc; 2 cabinets)	32,000	260
II/221	Computer System (same as II/201 with 2.5M-word moving-head disc; 2 cabinets)	30,000	
	With 64K-Word Memory	38,000	
II/230	Communications System (II/25/CP with CPU options to support MAXCOM software system; PCI and universal communications multiplexor; mounted in 2 std cabinets)	29,500	219
II/231	General-Purpose 16-Bit Computer (same as II/26CP with peripheral control interface enclosure; direct memory processor; multiplexor controller and universal multiplexor; 2 cabinets included)	27,500	
	With 64K-Word Memory	35,500	



**PRICE DATA (Contd.)**

Model Number	Description	Purchase \$	Monthly Maint. \$
<b>CENTRAL PROCESSORS AND WORKING STORAGE (Cont'd.)</b>			
Memory Options for MODCOMP II			
Read/Write Core Memory (0.8- $\mu$ sec cycle time)			
3601-1	4,096 Words	2,400	12
3608	8,192 Words	4,200	21
3609	16,384 Words	6,500	33
3618	8,192 Words	4,200	21
3619	16,384 Words	6,500	33
3606	Memory Parity	500	3
II/5/10/20/25 Processor Options			
3503	Multiply/Divide	500	3
3512	Hardware Floating Point	4,000	20
Input/Output and Interrupt Options			
3704	Direct Memory Processor	1,500	8
3708	External Direct Memory Processor	4,000	40
3629	System Protect Feature (requires 3731)	1,000	5
3730/1	Priority Interrupt Group	500	3
3732	External Priority Interrupt (4 interrupt levels)	500	3
3737	Executive Features (includes real-time clock with 5-msec interrupt, console interrupt, and task scheduler interrupt; requires 3730)	500	3
3739	Power Fail-Safe/Auto Start Feature	500	3
<b>MODCOMP IV</b>			
General-Purpose Digital Computer			
IV/10	General-Purpose Digital Computer (same as IV/10 with memory expansion to 384K bytes; context switching file with 240 reg; memory management system including 1,024 memory mapping reg consisting of 4 files of 256 registers each; auto memory allocation hardware; memory protect on a 256-word basis)	15,500	148
IV/20	General-Purpose Digital Computer (same as IV/10 with memory expansion to 384K bytes; context switching file with 240 reg; memory management system including 1,024 memory mapping reg consisting of 4 files of 256 registers each; auto memory allocation hardware; memory protect on a 256-word basis)	19,500	188
IV/25	General-Purpose Digital Computer (same as IV/10 with 16 sets of general-purpose registers containing 15 registers/set; memory management system permitting expansion to 512K bytes, including: 1,024 memory mapping registers consisting of 4 files of 256 registers each, automatic memory allocation hardware, and memory protect on a 256-word basis; 4-port memory interface)	23,500	224
IV/10 and IV/25 Memory			
3661	Core Memory Module (32K bytes; 16-bit cycle time — 640 nsec; 32-bit cycle time — 1.2 $\mu$ sec; 1 module included with CPU and required for lower half of each 64K-byte module pair)	8,000	40
3662	Core Memory Module (same as 3661 except used in upper half of each 64K-byte module pair)	6,000	30
IV/10 and IV/25 Processor Options			
3712	Simultaneous Direct Memory Processor	4,000	30
3646	Dual Memory Ports	6,500	55
3515	Extended Arithmetic Unit	5,500	28
IV/10 and IV/25 Input/Output and Interrupt Options			
3631	System Protect	1,500	8
3734	External Interrupt Group	500	3
3134	Remote Control Console Control Panel and Enclosure	1,000	10
Input/Output and Interrupt Options for MODCOMP II			
3751	Controller (for Teletype and p t reader)	400	2
3752X	Controller (for async RS232C-compatible console device and for p tape reader)	400	4
3753-X	Controller (for async 420 console device and for p tape reader)	400	4
<b>MASS STORAGE</b>			
Fixed-Head Discs			
4103	262,144 Words (8.7-msec avg access time)	15,000	105
4104	524,288 Words (same as 4103)	19,000	133
4106	1,048,576 Words (same as 4103)	38,000	170
Moving-Head Discs			
4126	1,299,200 Words (70-msec avg positioning time; 20-msec avg latency) <sup>(3)</sup>	11,000	99
4127	1,299,200 Words (same as 4126 except controller not included; requires 4126) <sup>(3)</sup>	7,000	84
4128	2,598,400 Words (same as 4126) <sup>(3)</sup>	14,000	126
4129	2,598,400 Words (same as 4128 except controller not included; requires 4128) <sup>(3)</sup>	10,000	111
4132	12,312,230 Words (35-msec avg positioning time; 12.5-msec avg latency) <sup>(3)</sup>	23,000	145
4133	12,312,230 Words (same as 4132 except controller not included; requires 4132) <sup>(3)</sup>	18,000	130
4134	26,624,640 Words (same as 4132) <sup>(3)</sup>	28,000	185
4135	26,624,640 Words (same as 4134 except controller not included; requires 4134) <sup>(3)</sup>	23,000	160
4140	Disc Cartridge (for 4126-4129)	180	NA
4141	Disc Pack (for 4132-4135)	500	NA

# MODULAR COMPUTER SYSTEMS — MODCOMP I, II, AND IV

## PRICE DATA (Contd.)

Model Number	Description	Purchase \$	Monthly Maint. \$
<b>INPUT/OUTPUT DEVICES</b>			
4903 <sup>(2)</sup>	Peripheral Controller (for 1-4 controllers)	1,200	6
4906	Peripheral Controller (switch for programmed switching of up to 4 controllers between 2 MODCOMP computers)	3,000	25
4701	Interval Timer	1,000	5
4701-10	External Clock	1,000	5
4801	General-Purpose Controller Module	600	—
4705-1	General-Purpose 16-Bit Data Terminal	1,500	15
4810/4811	Asynchronous Communications Interface	1,250	13
4815/17	Synchronous Communications Interface (2 full-duplex channels)	1,250	13
4820	Computer Link Teletypewriters	4,000	40
4205	Data Communication Printer (tabletop; KSR; 30 cps)	4,400	38
4206	Data Communication Printer (same as 4205 except 120 cps; 120 print col; external forms tractor)	6,100	54
Remote Teletypewriters			
4223	ASR 33	1,250	12
4224	KSR 35	3,250	55
4225	ASR 35	5,250	61
Console Teletypewriters (require 3744 or 3751)			
4233	ASR 33	1,500	—
4234	KSR 35	3,500	—
4235	ASR 35	5,500	—
3747/9	Programmable Power On/Off Controls for 4233 Teletypewriters	300	—
4253	Programmable Power On/Off Control for 4223 Typewriter	300	2
Paper Tape			
4512	Paper Tape Reader and Punch	5,000	42
4513	Paper Tape Reader	2,000	12
Floppy Discs			
4521	150-Word Storage Capacity (controller included)	4,000	40
4522	Dual; 300K-Word Storage Capacity Punched Card <sup>(3)</sup>	6,000	60
4411	Card Reader (300 cpm; controller included)	4,000	24
4412	Card Reader (same as 4411 except 1,000 cpm)	9,000	54
4421	Card Punch (100 cpm; controller included)	30,000	162
Line Printer <sup>(3)</sup>			
4211	600 lpm, 132 Columns	17,900	125
4213	50-150 lpm, 132 Columns	7,000	91
4214	300 lpm, 132 Columns	14,000	91
<b>DATA COMMUNICATIONS</b>			
1905	Controller (for async communications multiplexor)	1,200	12
1910	Asynchronous Communications Multiplexor	1,600	16
1911/2/3	Asynchronous Communications Channel	500	5
1906-1	Controller (for universal communications multiplexor)	4,500	45
1920	Universal Communications Multiplexor	1,600	16
1922/3	Synchronous Communications Channel	1,200	12
1924/5/6	Asynchronous Communications Channel	1,000	10
1941	MODCOMP-CDC Satellite Coupler	8,000	80
1950	MODCOMP-IBM 360/370 Interface	7,000*	70
4216	Electrostatic Printer	9,000*	99
4217	Electrostatic Printer/Plotter	13,000	140
4219	VERSAPLOT Plotting Software	1,500*	—
4426	Keypunch/On-Line Card Punch/Automatic Interpreter	15,000	110

\* Delivery subjects to home-office quotation.

### Notes:

- (1) Modular Computer has 4 maintenance plans — resident service, full service, scheduled maintenance, and on-call. Resident service provides a trained service engineer on a 1-shift basis at a cost of \$32,000/year. This column lists the full-service maintenance charge. Cost of other plans available on request.
- (2) No charge if purchased in conjunction with 3 or more peripheral controllers or analog input subsystem controllers.
- (3) Requires any 4900 Series peripheral control unit.

## HEADQUARTERS

Modular Computer Systems  
1650 W. McNab Road  
Ft. Lauderdale FL 33309



## MODULAR COMPUTER SYSTEMS

MODCOMP I, II, and IV Report Update

Modular Computer Systems has introduced both a new 84 megabyte stand-alone disc drive system and a File Management System supported by the firm's MAX IV real-time multiprogramming operating system. The company also announced price cuts of more than 17 percent on their 12.3 and 24.6 megabyte disc storage units.

### NEW DISC DRIVE

The 3330-type disc drive contains its own regulated power supply and has an access time of 28 milliseconds. The system has a single-spindle design that provides 84 megabytes of storage per drive. Capacity can be increased in 84 megabyte increments, linking up to four drives with each controller.

A dual access option makes the new system well-suited for dual processor applications. One unit can be connected to two controllers, allowing two computers to read and write on the same disc.

Four different disc drive configurations are offered. A single disc drive is \$28,000 and a drive with controller is

\$35,000. The drive with the dual access option costs \$33,000 and the drive with dual access device and two controllers is priced at \$46,000. The system will be available the last quarter of 1975.

### NEW FILE MANAGEMENT SYSTEM

The File Manager, based on MODCOMP's MAX IV real-time operating system, provides the mechanism to organize, define, create, or destroy files, and to allocate space to and control access to data records. Files can be multilevel; data files and directories can be nested to any level. With the File Manager, the storage medium is divided into individually accessible files, allowing the user to define file families or libraries. This makes it easier for the user to access libraries of files.

File security is maintained with the File Manager. The system provides several mechanisms that permit the user to secure the files against unauthorized use or modification. The system is supplied at no cost with the MAX IV real-time multiprogramming operating system and will be available the last quarter of 1975.



# PRIME COMPUTER

Prime 100, 200, and 300 Series

AUERBACH Buyer's Guide to . . .  
MINICOMPUTERS



74-451

## OVERVIEW

The Prime series consists of three computers particularly oriented toward software and services designed for users' convenience. The main markets for the systems are currently data communications and industrial control. The largest system also competes in time-sharing and multiprogramming environments.

The Prime 200 is the "pivot" model in the line; it was first delivered in September 1972. The Prime 100 is essentially a slow 200 with a few features missing; it was first delivered in January 1973. The Prime 300 is much more powerful than the 200; it supports virtual memory and allows up to 50 million words of disc storage to be used as an extension of main memory. The 300 was first delivered in September 1973.

All three models are 16-bit microprogrammed minicomputers that feature all-MOS memory, instruction sets compatible with Honeywell Series-16 and extensive software. The 100 is a 4K- to 32K-word system (1.0  $\mu$ sec memory cycle time), the 200 is a 4K- to 64K-word system (750-nanosecond memory cycle time), and the 300 is an 8K- to 256K-word system (600- or 750-nanosecond memory cycle time). The three systems are upward compatible and use the same system software and peripherals.

All three models can address up to 64 peripheral devices: magnetic tape and disc units, printers, paper tape and card equipment, communications devices and analog/digital equipment. The larger minicomputer manufacturers currently have a larger assortment of peripherals than Prime offers with its systems. However, Prime continues to add peripherals to its line, such as an IBM-compatible floppy disc and a 2314-compatible moving head disc.

The I/O structure for the line is flexible with five types of I/O channels available. Stack manipulation instructions and a 64-level priority interrupt system are standard features on all processors. The Prime 200 and 300 can also attach floating-point hardware; the 300 supports writable control store.

The Prime systems are particularly well suited to communications because of their DMC/DMT I/O facility. DMC is like a slower-speed DMA, with channel control words stored in memory instead of the DMA register file; there is no logical limit to the number of devices it can support. The DMT channel is faster than Prime's DMA channel because the current addresses for data transfers are supplied by device controller registers for DMT, rather than channel registers for DMA.

Communications functions are further supported by a line of synchronous and asynchronous single line and multiline controllers.

The software available is quite extensive: two full-fledged operating systems — DOS and RTOS, Macro Assembler, BASIC Interpreter and FORTRAN IV compiler can operate stand-alone. The Prime 300 uses virtual memory versions of the standard operating systems (DOS/VM and RTOS/VM).

There is no software especially geared to communications except the software drivers for the line controllers and the RTOS operating system.

The Prime processors are also marketed as processors for value-added networks and for satellite voice communications.

From its beginning, Prime has used all MOS memory for its computers, thus the company has had considerable experience with it. Prime developed the first 32K-word MOS memory board. It uses 4K chips from a variety of suppliers. The board is 16 by 18 inches. Table 1 lists the mainframe characteristics.

## COMPETITIVE POSITION

The Prime series computers are marketed for industrial control and data communication applications. The line is not being marketed as liberators of H316s or DDP-516s, even though the Prime computers are program compatible with the Honeywell Series 16 computers.

In general, the Prime systems are cost and performance competitive with similar systems, and their hardware and software offerings are well-rounded. The focus on industrial control and data communications is a wise path for a small company to follow, for it can concentrate its resources and be truly competitive with larger companies.

The DMC/DMT I/O channels, together with the communications facilities and related software, make the

**Table 1. Prime Computer Series: Mainframe Characteristics**

	100	200	300
<b>CENTRAL PROCESSOR</b>			
Type (microprogrammed)	Yes	Yes	Yes
No. of Internal Registers	26	26	26
Addressing			
Direct	Yes	Yes	Yes
Indirect	Multilevel	Multilevel	Multilevel
Indexed	Yes	Yes	Yes
Instruction Set Implementation			
Number	112 std, 8 opt	117 std, 37 opt	145 std, 29 opt
Decimal Arithmetic	No	No	No
Floating-Point Arithmetic	Subroutine	Subroutine	Subroutine
User Microprogramming	No	No	Optional
Priority Interrupt Levels	64	64	64
<b>MAIN STORAGE</b>			
Type	MOS	MOS	MOS
Cycle Time (μsec)	1.0	0.75	0.60 or 0.75
Basic Addressable Unit	Wd (16 bits)	Wd (16 bits)	Wd (16 bits)
Bytes/Access	2; 4	2; 4	2; 4
Cache Memory	No	No	No
Min Capacity (wds)	4K	4K	8K
Max Capacity (wds)	32K	32K std, 64K opt	256K
Increment Size (wds)	4K; 8K	4K; 8K	8K; 32K
Ports/Module	1	1	1
Error Checks	None	Parity	Parity
Protection Method	None	None	Software
Memory Management	No	No	Yes
ROM Use	Bootstrap loader, control store	Bootstrap loader, control store	Bootstrap loader, control store
<b>I/O CHANNELS</b>			
Programmed I/O	Yes	Yes	Yes
Direct Memory I/O (no. of subchannels)	8 (programmable)	8 (programmable)	8 (programmable)
DMA	No limit	No limit	No limit
DMT	4,096	4,096	4,096
DMC			
Max Xfer Rate (wds/sec)			
Over DMA	694,444	925,925	1,157,406
Over DMC	225,225	271,739	339,674
Over DMT	694,444	1,084,956	1,250,000

systems particularly good for communications applications. The RTOS operating system allows foreground/background processing, combining real-time data acquisition and control in the background with program development in the foreground. The addition of the larger, faster Prime 300 system adds to the line's range of processing power in both markets, and strengthens its competitive position for multiprogramming and time-sharing applications through the standard memory mapping and virtual memory techniques.

The Prime 100 competes with the DEC PDP-8, PDP-11/05, and 11/10; Data General Nova 1200, and ECLIPSE S/100; and Interdata Model 7/16. The Prime 200 competes with the DEC PDP-11/40, Data General Nova 800, ECLIPSE S/200, Interdata Models 70/80 and 7/16, and General Automation SPC-16. The Prime 300 competes in the upper range of minicomputers with such systems as DEC PDP-11/45, Interdata 7/32, Varian Data Machines V74, MODCOMP IV and Hewlett-Packard HP 21MX.

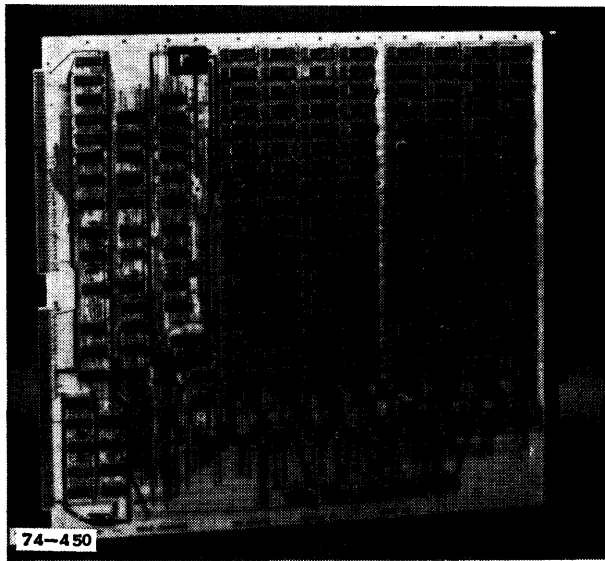
Some of the competitive systems with the 100 and 200 can expand memory beyond 64K words and can use

memory management systems that make them more appropriate for multiprogramming and real-time applications. The Prime 100 and 200 computers do not have hardware memory protection, but the Prime 300 does. It also has a relatively sophisticated memory management option, allowing addressing of up to 256K words of real memory.

Although some manufacturers have had considerable difficulty with MOS memory reliability, Prime has developed a board testing technique to allow consistent production of reliable large memories.

## USER REACTIONS

Users we contacted were unanimous in extolling Prime's service and support organization, and its general attitude of helpfulness when any problem arose. One user had some of its first new DAC boards and had some problems with the Digital Output module. This user expected some problems with a new item, however, and felt confident the company would soon set things right. Another user had a Prime 300 system for more than a



year, and the system had been down only twice: once for an hour, and once, when a part had to be flown in, for less than a day.

Users generally bought the Prime systems after considering the larger, well-established minicomputer manufacturers.

**Appliance manufacturer.** A large appliance manufacturer using a Prime 300 chose the system over those manufactured by Digital and Hewlett-Packard because the company had high performance demands and limited funds. This 32K-word virtual memory system supports engineering design and test functions in a time-shared mode. Various data acquisition instruments are attached to the system, as well as a number of Tektronix graphics terminals. This user is pleased with the result; interfacing to the system has been easy. This user felt the documentation for interfacing could be improved, however. When we spoke to him, he had placed an order for the hardware floating-point processor and was waiting for the RTOS-VM A/D and D/A software drivers to be completed, so they could run their data acquisition system under RTOS instead of DOS.

**Newspaper Production.** Another user bought Prime 200 systems to control a line of automated newspaper production systems. This user looked at Digital, Data General, and others before selecting the 200. The Prime system attracted them because this company already had used Honeywell 316s to run its phototypesetters, and some of the already developed software could be used on the Prime 200. This user feels Prime has particularly good documentation for its software, an important point because the documentation tended to be used over and over again, whereas hardware interfacing documentation problems were usually one-shot affairs.

**Diversified Manufacturer.** A very large diversified manufacturer selected the Prime 300 as the processing unit for a product line in telecommunications routing centers. The CPUs in the system will be used for switching, logging, and routing functions for TV, telephone, and data transmission via satellite. The manufacturer began developing the system using a Honeywell Series 16 processor, but became very dissatisfied with Honeywell's service. The company discovered the Prime product line and is delighted with the change; the Prime 300 is faster, costs less, and has more expansion capability than the Honeywell system. The Prime system software was one of its strong points. This user will undoubtedly become one of Prime Computer's larger accounts; each routing system will consist not only of multiple CPUs (two to four), but also discs, tape drives, and printers — in short, a whole system OEMed, not just the processor.

## CONFIGURATION GUIDE

Minimum configurations include a processor with 4K or 8K words of MOS memory, programmed I/O, eight programmable DMA channels, power supply, 64-level vectored priority interrupt system, and console. Basic systems provide additional subassembly slots for memory expansion modules and I/O device interfaces. The basic models have five standard subassembly slots; 10 or 17 are optional. Each 4K-, 8K-, or 32K-word memory modules requires one slot, and the central processor requires one slot. Modules can be arranged in any order on the universal bus system.

Table 2 lists the peripherals available for the Prime computers.

### Table 2. Prime Computer Series: Peripherals

**Magnetic Disc.** Moving Head: Capacities of 1.5M wds, 3.0M wds, 12.0M wds (access time 15 msec min, 70 msec avg, 110 msec max; 12.5 msec avg latency) and 25M wds (IBM 2314-type).

Fixed Head: 128K wds, 256K wds capacity.  
Diskette: 138 wds. (IBM-compatible.)

**Magnetic Tape.** 7-track, 800 bpi, 45 ips; 9-track, 800 bpi, 45 ips.

**Punched Card.** 150 to 300 cpm reader, 400 cpm/100-285 cpm Reader/Punch.

**Graphics Display.** Alphanumeric Display with keyboard.

**Printer.** 165 cps Serial Printer; 300 lpm line printer; Both 132 col.

**Paper Tape.** Readers at 200 cps; reader/punch at 200/75 cps respectively. 8-channel fanfold tape.

**Teletypes.** TTY 33 ASR, KSR; TTY 35 ASR characteristics.

**Analog/Digital.** A/D Conversion, D/A Conversion subsystems; Digital Input and Digital Output Subsystems.

**Communications.** Async multiline controllers, sync multiline controller, multiple auto call interface.

Prime offers central processor in four submodels for the 100 Series, in 12 submodels for the 200, and in six submodels for the 300. Processor models vary in basic memory size, electrical environment, mounting chassis, and standard processor features, at prices slightly lower than adding them optionally to the processors.

The 200 Series processors have a few standard features that are available as options for the 100 Series; byte parity and an asynchronous serial communications interface are standard features, for instance. In most respects, the 100 is a slower 200, with essentially the same features on a smaller scale.

Memory can be incremented in modules of 4K, 8K, or 32K words. The I/O bus can handle a maximum of eight controllers for high-speed DMA devices like magnetic discs and tapes. All eight can operate simultaneously and time share the I/O bus. Devices with their own control registers can also use the ultra-high-speed DMT channel, which is optional on both the 100 and 200 and standard on the 300. Slower-speed devices like the serial printer, paper tape, card I/O devices, Teletypes, and the analog/digital and communications interfaces use programmed I/O or the DMC — optional on either the 100 or 200 and standard on the 300. The DMC can handle a maximum of 4,096 individual devices, although the system as a whole can directly address only 64 device controllers. The DMC channel requires four memory cycles for each word transferred.

A minimum 300 Series system is similar to a 200 Series minimum system with most options included as standard. For instance, all 200 Series models have the following options to expand processing power: extended addressing to 64K words of memory, hardware multiply/divide, double precision arithmetic, micro-verification routines, automatic program loading from paper tape, and DMC/DMT channels.

These items are standard on the 300 Series, except extended addressing is to 256K words of memory. The following major features provided for the 300 Series are unavailable for the 100/200 Series:

- Virtual memory addressing to 64K words.
- Physical MOS memory capacity to 256K words with virtual memory up to disc capacity.
- Two distinct processor modes — paging mode and restricted mode — can be designated separately or together to allow processing at user, supervisor, or base operating level.
- Memory cycle time of 600 nanoseconds per word.
- Optional floating-point processor that executes 19 floating-point instructions.
- Writable control store.

Three special interfaces are provided: one allows a user's own device to connect to a system, a second allows controllers from the Honeywell Series 16 computers to interface to a system, and the third allows a second Prime processor to be linked to a system.

## COMPATIBILITY

Prime 100 and 200 Series computers are completely program-compatible; given the appropriate configuration, programs compiled on one computer can run on the other. The 100 Series uses a subset of the 200 Series instruction set. Both processors have an "unimplemented instruction" trap that allows a jump to a subroutine to perform the missing instruction. Honeywell Series 16 programs can be run on either the 100 or 200. Both Prime computers use the same software and peripherals, but they use different memory modules. The 100 Series modules do not include memory parity; the modules used with the 200 Series include two parity bits per word, one per byte.

Both the Prime 100 and 200 are upward compatible with the Prime 300. The use of the unimplemented instruction trap on the smaller computers means that programs compiled on the 300 can run on the 100 and 200 as well. The 300 also has the trap, but since all 100 and 200 instructions are standard on the 300, there is no immediate use for it. Table 3 lists the software packages available for the Prime computers.

## MAINTENANCE AND SUPPORT

Prime markets its systems through its own sales and service facilities, and also through representatives. There are 11 sales offices in the United States, and four service centers (Massachusetts, Pennsylvania, Michigan, and California), as well as offices in England, Germany, Sweden, Denmark, Norway, Finland, Belgium, Switzerland, Austria, Netherlands, and Australia. All systems are sold, with monthly maintenance contracts available. These provide for both preventive maintenance and emergency service. Software is warranted for one year, with revisions and corrections made free of charge during that period.

**Table 3. Prime Computer Series: Software**

Package Software	Configuration Required	Comments
OPERATING SYSTEMS DOS	8K memory; Teletype ASR and interface; real-time clock; disc	Basic batch operating system for PRIME computers; written in Fortran; multiple directories, volume control, and access methods. Can run as background task under RTOS-VM.
RTOS	8K memory; Teletype ASR and interface; real-time clock	Compact, real-time multiprogramming system; can be disc- or memory-resident.
RTOS-VM	32K memory; Teletype ASR and interface; real-time clock; disc	Like RTOS but with paging algorithm, swapping, protection.



**Table 3. (Contd.)**

Package Software	Configuration Required	Comments	Model Number	Description	Purchase \$
DOS-VM	Same as RTOS-VM	Up to 15 users can time-share with each user up to 64K words of memory.			
ASSEMBLERS/ COMPILERS					
FORTTRAN IV	12K memory; Teletype ASR and interface	One-pass compiler, extended instruction set, support library.	P3008B-10 P3008C-10	Prime 300 in 10-board chassis P3008B-05 with 600-nsec memory in 10-board chassis	11,700 12,500
Macro Assembler	Minimum configuration	Pseudo Ops, symbol and data definition, program linking, storage allocation, user-defined macros.	157	<b>Prime 100 Options</b> Hardware multiply/divide, double-precision arithmetic and DMC/DMT capability	13,000 1,000
Micro Assembler	32K memory; DOS or DOS-VM	For symbolic assembly of micro-code on model 300 with WCS.	253 257	<b>Prime 200 Options</b> Microverification routines Hardware multiply/divide, double-precision arithmetic, DMC/DMT capability, and microverification routines	800 1,000
BASIC UTILITIES	12K memory, Teletype	Extended; batch, conversational and immediate modes.			
Desectorizing Link Loader	Minimum configuration	Loads, links, binds relocatable, or absolute program modules.	361	<b>Prime 300 Options</b> Writeable control store (256 wds. 64 bits per microinstruction)	3,500
I/O Control Subsystem	Minimum configuration	Control routines and device drives; includes source file editing and merging.	362 369	Double- and single-precision floating-point arithmetic, and writeable control store Microprogramming training course, 1 man, 1 wk	5,000 1,000
Editors	Minimum configuration	Full-context editor for editing lines, characters, and multiple changes of same text in program.	150/250 151/251 142/242 145/245	<b>Prime 100 and 200 Options</b> Hardware multiply/divide and double-precision arithmetic DMC/DMT capability Automatic program load from Teletype and paper tape reader Automatic program load from multi-devices; includes Teletype, paper tape reader, disc, magnetic tape	800 500 400 600
<b>TYPICAL PRICES</b>					
			Model Number	Description	Purchase \$
P1004A-05	<b>Prime 100 Central Processors</b> Prime 100 Central Processor unit (with 4K wds of MOS memory; 1 μsec; 8-chan programmable DMA; full addressing modes; virtual instruction package; 4-chan, bit serial full-duplex interface; 5-board chassis; multi-level vectored priority interrupt system)		4,600		
P1004A-10	Prime 100 in 10-board chassis		5,600		
P1004A-17	Prime 100 in 17-board chassis		7,600		
P2004B-05	<b>Prime 200 Central Processors</b> Prime 200 Central Processor Unit (with 4K wds of MOS memory, 750 nsecs, byte parity; full addressing modes; 8-chan programmable DMA; multi-level vectored priority interrupt system; virtual instruction package; power supply; 10-board chassis; interface)		5,600		
P2004B-10	Prime 200 in 10-board chassis		6,500		
P2004B-17	Prime 200 in 17-board chassis		8,400		
P3008B-05	<b>Prime 300 Central Processors</b> Prime 300 Central Processor Unit (with 8K wds of MOS memory; 750 nsec; virtual memory; stack procedure instructions; microverification routines; hardware multiply/divide; double-precision arithmetic; DMC/DMT Capability; automatic program load; byte parity; full addressing modes; virtual instruction package; 8-chan programmable DMA; bit serial full duplex interface; Multi-level vectored priority interrupt system; 5-board chassis)				
			9501	<b>Prime 200 and 300 Options</b> Field Exerciser Panel (FEP): display unit, control unit and cable	600
			260/360	Double- and single-precision floating-point arithmetic (14-digit accuracy)	2,000
			146/246/346	<b>Prime 100, 200, &amp; 300 Options</b> Custom automatic program loader (256x16-bit wds)	600
			147/247/347	One-time documentation charge for custom APL	1,200
			140/240/340	Power monitor, power failure interrupt and automatic restart protection including battery backup for standby power for MOS memory	600
			141/241/341	Additional battery	200
			4000	<b>MASS STORAGE</b> <b>Discs and Diskettes</b> Disc controller for any combination of two fixed-head and for moving head discs	3,500
			4103/5	128K/256K word fixed-head disc	9,500/11,000
			4121	1.5M word moving-head disc	7,500
			4123	3.0M word moving-head disc	9,500
			4127	6.0M word moving-head disc	11,500
			4300	Diskette controller and 2 drives	5,200
			4166/67	Diskette cartridge, IBM/Prime format (73/77 data tracks)	25
			UM008A-016A	<b>Prime 100 Memory Expansion</b> 8K board, 1-μsec cycle time; no parity	3,800

**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase \$
UM016A-032A through UM048A-064A UM032B-064B	16K board, 1- $\mu$ sec cycle time; no parity (16K to 32K to 48K to 64K words)	6,800
UM008B-016B	32K board, 750-nsec cycle time; parity	11,000
	8K board, 750-nsec cycle time; parity	3,900
<b>INPUT/OUTPUT</b>		
3006/7	Real-time clock (line or external frequency), async line controller	1,800
3022	Sync line control capability	200
3023	Watchdog Timer (100 msec, RTC/PRTC, or external interval)	300
3025	Second 16-bit buffered parallel I/O controller (hdx)	500
3101	Teletype ASR 33	1,500
3103	Teletype KSR 33	1,200
3105	Teletype ASR 35	4,800
3121	Paper tape reader: 200 cps, for fan-fold 8-chan paper tape	1,900
3123	Paper tape reader/punch (reads 200 cps, punches 75 cps, for fan-fold 8-chan paper tape)	3,800
3141	Controller and card reader (300 cpm, binary and Hollerith formats)	5,000
3181	Controller and card reader/punch (400 cpm reader/100-285 cpm punch)	25,000
3161	Controller and line printer (300 lpm, 132 col, 64 char)	12,000
3191	Controller and card reader and line printer	17,000
3195	Controller and card reader/punch and line printer	34,500
3127	Character printer: 165 cps, EIA RS232-C compatible	6,000
4020	Controller for up to 4 magnetic tape transports	3,500
4141/3	Magnetic tape transport: 7/9 track, 45 ips, 556/800 bpi, industry compatible	7,000
3129	Alphanumeric CRT with keyboard, EIA RS232-C compatible	3,100
7000	General-Purpose Interface Board	1,200
7010	General-Purpose Interface Board	1,500
7030	Interprocessor Controller	3,500
	Async Multi-Line Controllers (AMLC; RS232-C/CCITT V24 compatible)	
5002/4	AMLC (for 103/202 data sets; 8/16 lines)	4,000/5,000
5052/4	AMLC (for direct connected devices; 8/16 lines)	2,600/3,000
5201/2/3/4	Multiple Sync Line Controller (RS232C compatible; for 201/203 data sets; 1/2/3/4 lines; + \$200/line)	2,400
5244	Byte packing and char recognition (SYN, DLE, EOM, special)	400
5245	Byte packing, char recognition, transparent mode, and CRC12, CRC16, CRCCITT, LRC	800
5246	Hardware bisync procedures for USASCII, EBCDIC, and SBTC codes	800
5402	MACI for 801 autocal units (4 lines)	2,000

**HEADQUARTERS**

Prime Computer  
 145 Pennsylvania Avenue  
 Framingham MA 01701  
 (617) 879-2960



## PRIME COMPUTER

### Prime 100, 200, and 300 Series System Report Update

A new version of Prime Computer's 300 time-sharing system allows up to 31 simultaneous users 128K bytes of virtual memory each and direct access to all peripheral devices from a user terminal. The system has 512K bytes of MOS main memory, floating-point arithmetic hardware, a 32-line asynchronous multiline controller, line printer, and 60M-byte disc pack. Programs can be written in any Prime programming language, including FORTRAN and BASIC, as well as MACRO and MICRO machine language. Each user has access to a complete virtual computer under control of microprogrammed memory management hardware and new features added to Prime's disc operating system.

The virtual memory disc operating system has the following features:

- Automatic log-out to prevent inactive but connected terminals from holding system resources beyond a pre-determined time limit.
- Read/write lock for file security — controls user access to all files through a system of file access control keys, which determine how users can access files and how files can be read, written, or deleted.
- A main memory scan tests the computer's main memory and bypasses any faulty locations identified.

An important new hardware feature is the Universal Disc Controller that can control any mix of four cartridge or disc pack units (6M, 12M, or 60M bytes capacity) and a fixed-head disc. A variety of disc units can be added to a system without using multiple controllers.

Primary competition for the new system is the Hewlett-Packard HP 3000 Series and the Digital Equipment DECSYSTEM 10. The Prime system is already in use in a variety of applications in the United States and England. Purchase price ranges from under \$50,000 for a 4-user system to approximately \$165,000 for a 31-user system. Deliveries are scheduled 30 to 60 days after receipt of order.

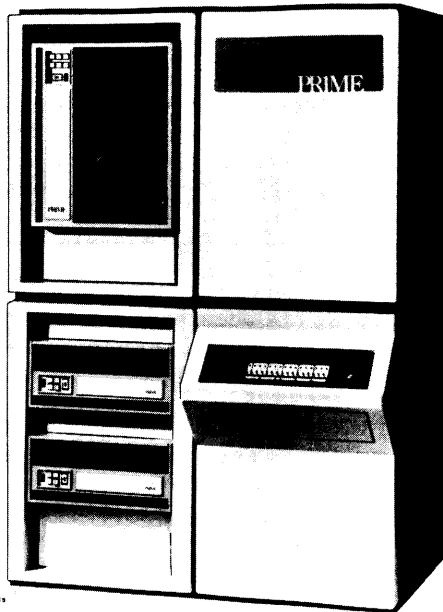
#### HEADQUARTERS

Prime Computer, Inc.  
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## PRIME COMPUTER INC.

### Prime 400 System Report



PRIME 400 WITH 256K BYTES OF MOS MEMORY, 9-TRACK  
MAGNETIC TAPE AND TWO 12M-BYTE DISCS

#### OVERVIEW

The Prime 400 (P400) is a new top-of-the-line addition to Prime Computer's minicomputer offerings, which currently consist of the Prime (P) 100, 200, and 300. The P400 is upward and downward compatible with the earlier models, and it uses the same memory modules and peripherals as the P300. It is three times as powerful as the P300, but out of the 17 circuit boards that implement the 300 Model, the P400 uses all but the two boards that implement the CPU. The new P400 CPU uses a microprogrammed control store and can address up to 4M words of memory. It includes a high-speed arithmetic unit, floating-point hardware, and 2K words of cache memory.

Memory is made up of 64K-byte MOS memory modules. Each module has one port of entry. Pairs of memory modules are interleaved and operate in parallel so that two words are read for each memory access. The internal memory bus that connects main memory to cache is 32 bits wide. Each word read from memory along with

its corresponding word in the interleaved module is stored in cache memory.

Cache memory consists of 2K bytes of bipolar Schottky memory with an 80-nanosecond access time. Cache operates in conjunction with the 32-bit-wide internal memory bus and two-way interleaved MOS memory modules of 64K bytes each to increase effective memory speed. When a memory location is addressed, the processor logic first looks in cache to determine if it is stored there. If so, memory is not accessed. When cache is full and a new word is read from memory or stored in memory, the algorithm overwrites the location least recently used with the new word. When an internal register is stored in memory, it is also stored in cache. Prime estimates that 85 percent of the time addressed words will already be in cache and need not be read from memory. Table 1 summarizes the P400 mainframe characteristics.

Prime has also developed PRIMOS IV, a new operating system for the P400. It supports BASIC, FORTRAN IV, MACRO, and MICRO assemblers, and ANSI Level 1 COBOL languages and large real and virtual memories.

PRIMOS IV is an "embedded" operating system: it is implemented partially in software and partially in the P400 microcode. The PRIMOS IV supervisor is embedded in each user's virtual address space, and each user can call it as if it were a subroutine or program module.

PRIMOS IV performs dynamic linking of program modules as needed at run time. It has a process exchange to switch program context on demand according to process priority. It also has provisions for procedure calls so that subroutines and programs can be reentrant and recursive. The subroutine calls provide fast automatic argument transfers.

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Table 1. Prime 400: Mainframe Characteristics

Characteristics	PRIME 400
<b>CENTRAL PROCESSOR</b>	
Microprogrammed Control Memory	Yes
No. of Registers	Yes
	32: 2 ACC, 1 index, 1 stack pointer, 16 DMA, 1 status, 1 MAP, 4 CAM, 1 unused, 4 $\mu$ program
Word Length, bits	16 + 2 parity or 6 ERCC
<b>Addressing</b>	
Direct	Yes
Indirect	Multilevel
Indexed	Yes
Mapping	Yes, to 8M bytes
<b>Instruction Set</b>	
Implementation	Bipolar ROM
Types	Single- or double-word
Number	174 std, opt
Floating-Point Hardware Stack	Yes, opt
<b>Instruction Execution</b>	
Times, $\mu$ sec	
Fixed-Point <sup>(1)</sup>	
Add	0.920/1.840
Multiply	4.560/9.20
Divide	5.120/10.66
Floating-Point <sup>(2)</sup>	
Add	4.22/5.5
Multiply	9.0/20.14
Divide	11.9/24.04
Writable Control Store	No
Interrupt	64
<b>MAIN STORAGE</b>	
Type	MOS
Cycle Time, $\mu$ sec	0.600
Basic Addressable Unit	Word
Bytes/Access	2
Cache Memory Capacity, bytes	1 x 16 bits
Min	256K
Max	8M
Increment Size, bytes	16K/64K
Ports/Module	1
Error Checks	Parity std; ERCC opt
Memory Protection	Yes, hardware & PRIMOS
Memory Management	Yes, hardware & PRIMOS
Interleaving	2-way
<b>INPUT/OUTPUT</b>	
Max Devices	64
Addressable	Yes
Programmed I/O	8 channels

Table 1. (Contd.)

Characteristics	PRIME 400
DMA	1.16M (DMA)
Transfer Rate, bytes/sec	1.25M (DMT), 0.34M (DMC)
Notes:	
(1)	Fixed-point times are for single-precision (1-word)/double-precision (2-word) operands.
(2)	Floating-point times are for single-precision (2-word)/double-precision (4-word) operands. (Times assume 85% bit rate in cache memory.)

PRIMOS IV will support up to 64 simultaneous users. Each user has access to up to 512M bytes of virtual memory space divided into 4K segments of 128K bytes each.

Subsets of PRIMOS IV are available for the smaller Prime computers. PRIMOS III can support 31 users on a virtual memory system on the P300. PRIMOS II supports a single user on a disc system and provides a real-time operating system on the P100 and P200.

Prime announced support for eight disc units for up to 1.2 billion bytes of on-line disc storage. The disc units are based on the CDC 300-megabyte Storage Module.

Prime Computer is now orienting marketing efforts toward the end-user with a software/hardware-integrated group of application packages called the TEMPUS family. The packages range from small multiuser systems designed around the P100 to large virtual memory systems designed around the P400. The packages are identified by names to represent the applications for which the hardware/software configurations were planned:

- CREATE for computation.
- CONTROL for data acquisition and control.
- RESPOND for communications.
- TRANSACT for business data processing.

**COMPETITIVE POSITION**

The P400 is a major enhancement to Prime Computer's product line. It extends the range upward into the midcomputer range where mini-computer manufacturers have been mining the gold that one might expect to belong to the large mainframers. The miners in this range include the Digital Equipment PDP-11/70, Varian Data



V76, Data General ECLIPSE, and Hewlett-Packard 3000. Table 2 compares the P400 with the PDP-11/70 and V76. The P400 appears to be comparable to both systems in performance, although its floating-point arithmetic is somewhat slower. It is less expensive for comparable configurations than the PDP-11/70 but it is much more expensive than the V76. Varian recently cut memory prices drastically, and the V76 prices reflect those cuts.

The Prime computers are all compatible with Honeywell's Series 16 minicomputer line, which was recently rejuvenated with the new Level 6/06. That system was developed for the low-end OEM market and should not impact Prime Computer systems, which are usually sold in configurations costing \$50,000 upward. The Level 6/34 and Level 6/36 are also at the low end of the mini-

computer market — the basis of a new line of minicomputers. They are not compatible with the Series 16; thus they offer no special competition to the Prime computers.

The P400 is a good upgrade for the P100, P200, and P300. The success of Prime Computer's new marketing orientation with the TEMPUS configurations is another matter. The initial announcement did not present a clear picture of how the TEMPUS family will be marketed. Marketing minicomputers in the competitive commercial arena requires hard planning to identify special situations that cannot be easily solved using a System 3/12 or 15, Burroughs 1700, or NCR 8200. It remains to be seen if Prime has done the difficult homework needed to ferret out those special situations.

Table 2. Prime 400: Compared With Some Major Competitors

	P400	Digital PDP-11/70	Varian Data V76
Word Length, bits	16 + 2	16 + 2 parity	16/16 + 2 parity
Inst Times, $\mu$ sec			
Add	.920	1.0	1.3
Multiply	4.560	3.8	4.8
Divide	5.120	8.3	5.2
F1-P Add <sup>(1)</sup>	4.22	2.0	3.7
F1-P Multiply <sup>(1)</sup>	9.0	3.9	6.1
F1-P Divide <sup>(1)</sup>	11.92	4.9	8.6
Max Memory, bytes	8M	2M	512K
No. of GP Registers	4: 2 accs, 1 index, 1 stack pointer	12: 3 stack pointers; 1 program counter (all 16-bit, all indexers)	8 (7 can be indexers)
Max DMA Rate, bytes/ sec	2M	4M (UNIBUS); 5.8M (data channel)	2M/6M <sup>(2)</sup>
Price, \$			
CPU + Memory			
64K bytes	—	—	17,150
128K bytes	48,700	60,500	22,400
256K bytes	71,200	74,700	35,800

— Not applicable.

Notes:

- (1) All floating-point times are single precision, which uses 2-word operands.
- (2) Via Priority Memory Access (PMA) and dual ports.
- (3) All prices include a floating-point processor and installation. The PDP-11/70 includes DEC-writer II console terminal; the Prime 400 includes operator's panel; and Varian V76 includes programmer's console.

# PRIME COMPUTER INC. — PRIME 400 SYSTEM REPORT

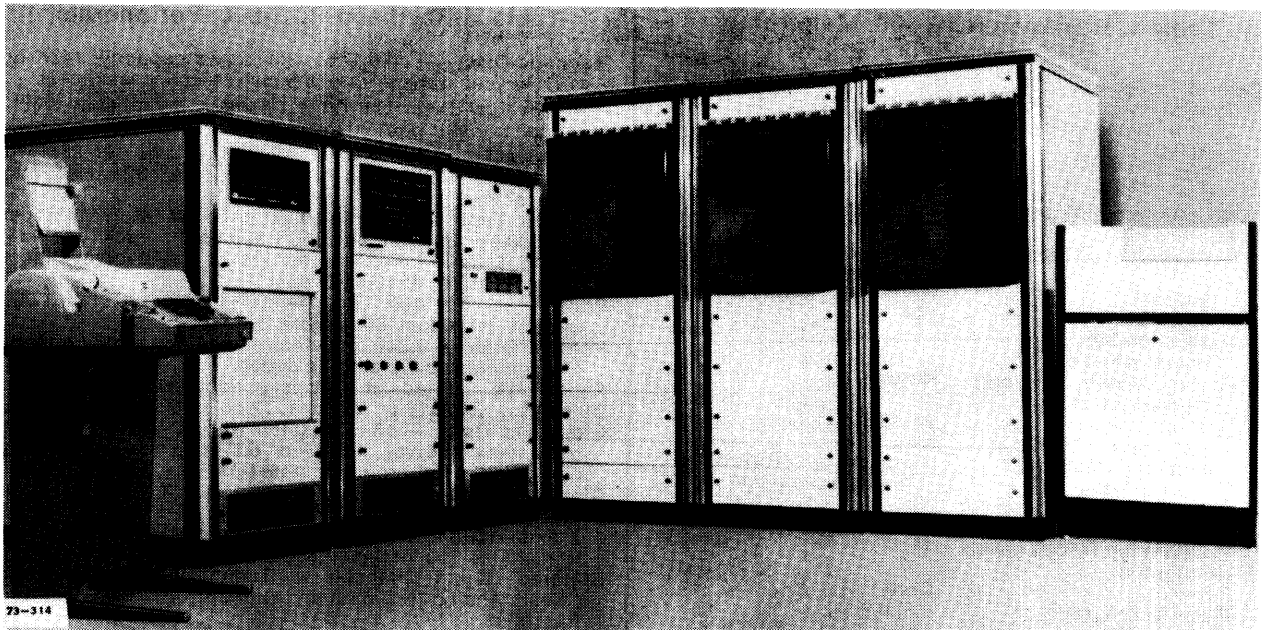
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## PRICE DATA

Equipment	Purchase Price \$
Prime 400 (includes 256K bytes MOS memory)	71,200
MOS Memory	
64K-byte Module	12,000
256K-byte Module	
First Module	30,000
Subsequent Module	24,000
PRIMOS IV Operating System	12,000
Prime 400 System (includes P400 processor with 256K-byte memory, 100M bytes of disc storage, 30-cps printer, 75-cps and 1,600-bpi tape drive, 8 communications lines, PRIMOS IV software)	140,000

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### OVERVIEW

RDS-500 is a general-purpose minicomputer that can operate in a variety of applications: real-time control, high-speed data acquisition, medical and laboratory data collection and analysis, and commercial data processing. The system was first delivered in March 1974. Raytheon offers a number of configuration options as well as language compilers and software utility packages for the system.

One interesting feature is that memories of different speeds can be mixed on one system: the RDS-500 has an internal asynchronous "Superbus I" which connects the CPU, memory, programmed I/O, and DMA direct memory access channels. Peripheral devices can connect to the DMA, and memory can be accessed simultaneously with the CPU because a second internal "Superbus II" attaches to a second port to memory.

A microprogrammed "Apollo" array processor is available to process seismic and signal data independently of the CPU; it uses hardware floating-point, dual port attachment, bit array manipulation, and command chaining to achieve high processing speeds.

Analog/digital, digital/analog subsystems are controlled by a single universal front-end interface called the "Nest" which connects to either DMA or programmable DIO (direct input-output) channels. The Nest and Apollo are recent improvements to the 500 series. Mainframe characteristics are listed in Table 1.

Peripherals available for the system provide for a fine selection of performance ranges. Fixed or removable discs and removable disc cartridges are available. Seven tape

drives, three line printers, four character printers, paper tape equipment, punched card equipment, displays, digital plotters, buffered digital channels, and communications devices round out the picture. Peripherals are listed in Table 2.

Software for the system becomes more complex as the system configuration expands. The Basic system precludes any high-speed input devices; the standard operating system (SOS) is essentially manual and runs on a "standard" configuration; it handles all peripherals but disc. The Magnetic Tape Operating System handles assembly, compilation, and execution of one or more programs automatically; it runs on an Extended configuration. The Extended configuration also supports the Real-Time Operating System (RTOS), which handles a full complement of peripheral types. The Multiprogramming System (MPS) is a superset of RTOS; it offers a variety of capabilities including time sharing. System software characteristics are listed in Table 3.

Languages offered are conversational FORTRAN, FORTRAN IV, RPG II, as well as SYM I and SYM II assembler languages.

### COMPETITIVE POSITION

Raytheon supplies computers primarily for real-time control and high-speed data acquisition applications. A substantial number of systems has been supplied to similar types of military applications. Since its first system was installed in 1960, Raytheon has delivered more than 900 computer systems; over 700 of these systems are computers from the 700 line. Over 150 RDS-500 systems have been sold. Raytheon computers have been used in such diverse applications as aircraft simulator control, closed-loop process control, airline reservations, seismic data

**Table 1. Raytheon RDS-500: Mainframe Characteristics**

<b>Central Processor</b>	
Type (microprogrammed)	No
Control Memory (RAM, ROM)	No
Size	
Use	
No. of Internal Registers	8 general-purpose
<b>Addressing</b>	
Direct (no. of wds)	2K, combined with page pointer to make 64K
Indirect	Via register only
Indexed	64K
<b>Instruction Set</b>	
Implementation (hardware, firmware)	Hardware
Number (standard; optional)	98; 132
Decimal Arithmetic	No
Floating Point	Hardware or software, multiple precision
Arithmetic	
User Microprogramming	No
Priority Interrupt System	
Operation Modes Levels	16
<b>Main Storage</b>	
Type	Core
Cycle Time ( $\mu$ sec)	0.8; 0.9
Basic Addressable Unit	16-bit word or 8-bit byte
Bytes per Access	2
Cache Memory	No
Min Capacity (wds)	8K
Max Capacity (wds)	64K
Increments Size (wds)	8K; 16K
Ports per Module	2
Error Checks	Parity (opt)
Protection Method	opt
Memory Management	No
<b>ROM</b>	
Use	—
Capacity (wds)	265
<b>I/O Channels</b>	
Programmed I/O	16 controllers
DMA Channels	8 or 16 controllers
Multiplexed I/O (no. subchannels)	No
<b>Max Transfer Rate</b>	
Over DMA (words/second)	1M (2M aggregate with dual-ported memory)
<b>Simultaneous Operations</b>	
	2

processing, on-line testing, pipeline station control, signal data analyses, medical research, vibration and shock testing, and laboratory data collection and analysis. Systems are sold and maintained in Europe as well as in the United States; the company's European headquarters is in Amsterdam, Netherlands.

For general-purpose minicomputer applications like medical and laboratory data collection and analysis and commercial data processing, the Raytheon RDS-500 competes with most other minicomputers, for example, DEC's PDP-11, the Data General Nova/Supernova line, and the HP 2100 line. In the process control market, Raytheon meets both the larger minicomputer manufacturers capable of the extensive support needed for these applications and systems that aim particularly at process control, such as the Honeywell 4000 line (formerly GEPAC), IBM 1800 and its lookalikes from General Automation and Digital Scientific, and IBM System/7, Foxboro Fox 2, and General Automation's SPC-16 series.

**Table 2. Raytheon RDS-500: Peripherals**

**Magnetic Disc** — Fixed Disc: 3M/6M-wd capacity; 143K or 187K wd/sec transfer rate; 8.5 msec avg access time.  
 Removable Disc Cartridge: 1.28M-wd capacity; 80K wd/sec transfer rate; 70 msec avg access time.  
 Removable Disc Pack: 12.99M-wd or 25.98M-wd capacities; 128K wd/sec transfer rate; 32 msec avg access time.  
**Magnetic Tape** — 7- and 9-track; either at 37.5/75/125 ips; 556/800 bpi, 800 bpi; and 800/1,600 bpi 21-track tape.  
**Punched Card** — Readers at 300 or 1,000 cpm, 80-col cards. Punches at 100-400 cpm.  
**Printers** — 10 cps char printer; 245-1,100 lpm/1,250 lpm/356-1,110 lpm. 80 to 132 col. 64 char.  
**Printer/Plotter** — 3,240 lpm electrostatic nonimpact printer, 132 col/line; 32,400 plotting speed.  
**Paper Tape** — Reads at 300 cps; punches at 110 cps.  
**Displays** — 2,520 char; 35 lines; 72 col; 1,024 x 780 matrix.  
**Clock and Timer** — 16-bit counter with 10- or 100-sec time base, max interval of 0.65 or 6.5 sec; also time-of-day clock in 32 or 36 programmable bits.  
**Digital Plotters** — 11-in. Y axis, 120-ft X axis; 0.010 or 0.005-in. or 0.10mm increment; or 28.55-in. Y axis, 120-ft X axis; 0.010 or 0.005-in. or 0.10 mm increments; speeds from 200 to 300 increments/sec.  
**Buffered Digital Channels** — Digital Input/Output Unit, "Nest" Analog-to-Digital and Digital-to-Analog Front-End Interface.  
**Communications** — Synchronous modem controller, serial line multiplexor.

In the special data acquisition applications related to seismic and signal data processing, Raytheon meets a number of other systems from less well-known manufacturers, such as the Computer Signal Processors CSP-30 and the Unicomp COMP-16 and 18. Raytheon's past experience, in addition to the high performance capabilities of the Apollo array processor, makes the RDS-500 particularly competitive in the latter market.

**User Reactions**

Two RDS-500 users were interviewed for this report: one uses two systems for process research and the other uses two systems for seismic data processing. Both have Apollo array processors on their systems. The first user bought Apollo as an afterthought while array processing is integral to the second user's application. Both users had previous experience with Raytheon as a vendor because both had 704s in house. Both find the RDS-500 considerably more powerful and easier to use because it does more with upcode than the 704. Both agree the hardware is good and reliable. Both use the MPS operating system and feel the Monitor is the best on the market for interfacing to fast real-time processes. These are handled in the foreground while a batch processor for generating reports, developing programs, or executing programs runs in the background. Both systems came up quickly once power was turned on.

The user with the process control application has had the systems installed for about six weeks and has had only one memory failure since installation. The systems are running, but there are still problems with them. The problems with the Monitor are in-line with what one expects from a process control installation where real-time



**Table 3. Raytheon RDS-500: Software Configurations**

PACK-AGE	DESCRIPTION	MINIMUM CONFIGURATION	OTHER DEVICES SUPPORTED	SOFTWARE SUPPORTED
<b>Basic System</b>	Modules common to all; X-RAY executive, resident monitor, editor,* assembler,* IOS, Conversational FORTRAN, math library, operating system for use without disc	8K-wd memory; ASR 33 TTY	ASR 35; multiply/divide	PTIOS; Basic Loader; SENSOR diagnostics
<b>SOS</b>	Operating system for use without disc	8K-wd memory; ASR 33 TTY; paper tape or card reader	ASR 35; multiply/divide; power fail; DMA; card & tape punches; printers; plotters; mag tape serial MUX	Basic system software + std loader, FORTRAN IV, SENSOR diagnostics, Trace-Debug
<b>MTOS</b>	Magnetic Tape Operating System	8K-wd memory; ASR 33; mag tape; DMA; paper tape or card reader	All SOS devices + operator interrupt	Basic system software + std loader, PTIOS, FORTRAN IV, Trace-Debug, system generator
<b>RTOS</b>	Real-Time Operating System	8K-wd memory; ASR 33; disc; DMA; paper tape or card reader	All SOS devices + operator interrupt	Basic system software + disc loader, PTIOS, FORTRAN IV, Trace-Debug, system generator, SENSOR diagnostics, sort/merge
<b>MPS</b>	Multiprogramming Operating System	8K-wd memory; ASR 33; disc; DMA; paper tape or card reader	All SOS devices + time-of-day clock, MPS, memory protect, operator interrupt	Basic system software + disc loader, PTIOS, FORTRAN IV, Trace-Debug, system generator, Sort/Merge, SENSOR diagnostics

\*SYM I Assembler with Basic, SOS systems; SYM II with others. Operating systems have system editor as well as symbolic program editor.

processes are interfaced. The Monitor does what Raytheon says it will do and the user is pleased with it. Raytheon is working with them to clear up problems.

This user did not look at other vendors because the system applications software was developed on the 704 and the RDS-500 is upward compatible with the 704. Originally, the 704 was selected because of its software. Before purchasing the array processor, the user did look at other vendors, notably from Floating Point Systems. Although their array processor is more powerful than Apollo, the user was afraid of incompatibility with the RDS-500 software. The user ended up writing his own driver for Apollo anyway and found it easy to do.

This user has found the utilities inconsistent from one to another and feels Raytheon fell down on the system approach when writing them, particularly with regard to the user interface. Batch Edit, for example, has been unworkable and will be replaced by a user-written version.

Overall the user is pleased with the system and expects to have the bugs ironed out on schedule.

The user with the seismic data processing application looked at the equipment from 15 vendors and determined that only two systems could do the job satisfactorily: Texas Instruments' TI980 and the RDS-500. The TI980 was eventually ruled out because the RDS-500 software was better suited to the application.

The RDS-500 was selected primarily for the following reasons:

- Raytheon produces a full range of peripherals for seismic data processing, such as 21-track magnetic tapes and large, fast fixed-head discs.
- 21-track tape.
- 3M-word fixed-head disc, 8.5-millisecond average access time.
- 6M-word fixed-head disc, 8.5-millisecond average access time.
- CPU architecture with dual-bus structure and dual-port memories.
- Reliable hardware and all available from Raytheon with no need to integrate other vendors' hardware.
- High-speed, 9-track magnetic tape, 125 inches per second.
- Almost all devices allow data chaining; not available from other vendors.

This user feels the Monitor is especially flexible because it is relocatable as are all the peripheral drivers. The Monitor can be Syggened for a specific configuration in about ten minutes. The RDS-500 CPU was designed to operate on 500-nanosecond cycle; thus the system is memory bound with the 700-nanosecond memories currently available. When faster memories are available, they can be interfaced immediately without difficulty.

This user would like some additional features. Although the system has eight general-purpose registers,

they are not completely useable as such. Because of compatibility with the 704, instructions tend to use only the accumulator and index register. This user would like a Swap instruction to exchange the contents of any two registers.

This user's application was an RDS-500 alpha test site, and thus the systems have been operating for over a year. Raytheon has been most cooperative on software and hardware problems, and the service has been excellent. The user volunteered that he was pleased and proud of his operating system.

We asked about the RDS-500 utilities. This user has found them more powerful than the 704 utilities. They must be used from the RDS-500 perspective because they function differently than those for the 704.

### CONFIGURATION GUIDE

Three types of configurations are identified: Basic, Standard, and Extended. The configuration type indicates the hardware/software package and the devices the software can support. The Basic system has no high-speed input device. The Standard system is punched card or paper-tape oriented, but can handle magnetic tape. The Extended system accommodates magnetic tape and disc, and any other peripheral Raytheon sells for the system.

A minimum RDS-500 system includes the following components:

- CPU, with eight general-purpose registers, 98 basic instructions, DIO bus logic, 16-level interrupt system for DIO, hardware bootstrap, TTY controller, and power failsafe.
- 8K words of memory.
- ASR 33 Teletype.
- Operator panel.

DMA channels, hardware multiply/divide, multiprogramming protection, parity, and hardware floating point can be added as optional features, which also add a total of 34 instructions. Additional 8K-word (800-nanosecond cycle time) and 16K-word (900-nanosecond cycle time) core memory boards allow memory expansion to a maximum of 64K words. Memories with different speeds can be mixed on a system. Raytheon expects to add MOS, bipolar, and ROM modules with various speeds and capacities that can be mixed on the asynchronous bus. A memory module with cycle time of 500 nanoseconds is planned.

Most DIO controllers control a single device, such as a printer, card or paper tape reader or punch, or communications interface. An exception is the serial multiplexor, which controls up to four devices (possibly Teletypes). DMA controllers can usually handle multiple drives. Magnetic tape, disc cartridge, and disc pack controllers handle up to four drives each; the fixed disc controller and plotter controller handle one drive. Most

devices attach to either DMA or DIO, but the Nest (process I/O interface) can attach to either.

The Apollo array processor requires both DMA multiplexors, one on each Superbus, and takes up one channel on each.

The CPU, option board, floating-point processor, and memory modules all attach to an internal asynchronous Superbus I that also connects the programmable DIO interface and one DMA multiplexor. The DIO bus can handle one to 16 DIO controllers, and up to eight DMA controllers can be multiplexed. Superbus II, a second bus, can be included in the system together with dual-port memory modules to allow a second DMA multiplexor and up to eight more DMA controllers to be attached. Thus, a maximum of 32 controllers (16 DIO, 16 DMA) can be included in a system.

### COMPATIBILITY

The RDS-500 is upward compatible with Raytheon's older 700 series of 16-bit minicomputers. The RDS-500 has new internal architecture which allows better performance, greater flexibility in system size, and greater modularity.

The instruction set is larger on the RDS-500 than on the 704 processor, the most recent of the 700 series. RDS-500 also has more internal general-purpose registers, and its memory capacity has been doubled to a maximum of 64K words. All software used on the 700 series has been adapted to the 500.

Apollo and Nest represent improvements over corresponding 700 series subsystems: the Nest can be retrofitted to a 704, but the Apollo cannot because it requires the dual port attachment.

Eventually, the 500 will supplant the 704. Raytheon plans to continue marketing the 704 as long as there is still a market for it. Although the RDS-500 is more flexible than the 704 and can use all the 704 software, the 704 will be more readily available until the RDS-500 is in full production.

### MAINTENANCE AND SUPPORT

Raytheon provides a world-wide maintenance for its systems. It also provides a computer maintenance school in Norwood, Massachusetts, to train customer's employees.

### HEADQUARTERS

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**TYPICAL PRICES**

Raytheon Data Systems — RDS 500				
Model Number	Description	Monthly Rental \$	Purchase Price \$	Monthly Maint. \$
51001	Apollo System (includes Apollo array processor with RDS-500 CPU; 2 16K-word multiport memories; floating point processor; extended processor features; and power fail protect)	2,465	57,000	320
51002	Same as 51001 except 4 8K word multiport Memories	2,575	61,000	340
51010	RDS Central Processor System (includes RDS 500 CPU with 2 16K word multiport memories; extended processor features and power fail protect)	560	14,500	488
51011	Same as 51010 except 4 8K word Multiport Memories	650	18,500	567
<b>Central Processors and Working Storage</b>				
50002	RDS-500 Central Processor (includes high-speed cpu; 8 GP regs; 65K memory; 16 vectored priority interrupts; automatic bootstraps for 4 devices; direct input/output controls; Superbus I and II; operator consoles; printer controller)	205	5,000	30
51201	Floating Point Processor	80	2,000	10
51202	Extended Processor (includes Superbus-I DMA, HS Multiply/Divide, MPS memory protect and memory parity)	35	1,000	5
<b>PROCESSOR OPTIONS</b>				
51203	Power Fail Protect	25	500	5
51204	Operator Interrupt	5	100	NA
51101	8K words of 800-nsec Multiported Memory	105	3,000	15
51102	16K words of 900-nsec Multiported Memory	160	4,000	30
<b>Mass Storage</b>				
51801/3	Controller for 51802 Disc Storage Drives or for up to 4 51804s	215	5,000	35
51802	High-speed Fixed Head Disc Drive (385K wd capacity; avg access time 16.7 msec; 180K wds/sec transfer rate)	240	6,000	40
51804	Disc Storage Drive (includes high-speed fixed-head disc drive; 38.5K wd capacity; avg access time 8.33 msec; transfer rate 180K wds/sec)	260	6,500	45

Model Number	Description	Monthly Rental \$	Purchase Price \$	Monthly Maint. \$
51901	Cartridge Disc Controller for up to 4 51902s or 2 51903s or combination	235	6,000	40
51902	Cartridge Disc Drive (provides removable storage of 1.28M wds/cartridge; cylinder, track and sector format; track transfer rate 80K wds/sec; avg access time 70 msec)	265	5,000	35
51903	Dual Cartridge Disc Drive (with one fixed and one removable cartridge; total storage 2.56M 16-bit wds; cylinder, track, and sector format; transfer rate 80K wds/sec; 70 Msec avg access time)	375	7,500	50
51904	System Disc Cartridge (includes 1.28M wd cartridge with system software)	10	200	NA
51905	Data Storage Disc Cartridge (includes 1.28M wds)	5	125	NA
51951/5	Disc Pack Controller for up to 4 51952s or 4 51956s; includes hardware keysearch feature	400	10,000	70
51952	Disc Pack Drive includes removable storage of 12.9M wds/pack with cylinder, track and sector format; transfer rate of 166K wds/sec; avg access time 32 msec	660	13,000	90
51953/7	System Disc Pack includes 12.9M wd pack and system software; 25.9M wd pack	30	500	NA
51954/8	Data Storage Disc Pack includes 12.9M wd disc pack; 25.9M wd pack	25	325	NA
51956	Same as 51952 except removable storage of 25.9M wds/pack	755	18,000	125
<b>Input/Output Magnetic Tape</b>				
51401/501/503	Magnetic Tape Controller for up to 4 51402s, 51502s, or 51504s	310	5,500	30
51402	Magnetic Tape Drive Attachment to the 51401 (37.5 ips; 7-track; dual density 556/800 bpi ; IBM compatible)	300	5,300	30
51403/05	Magnetic Tape Controller for up to 4 51404s or 51406s	335	5,500	30
51404	Same as 51402 except attaches to the 51403 (75 ips)	490	8,000	45

# RAYTHEON DATA SYSTEMS — RDS-500 SYSTEM REPORT

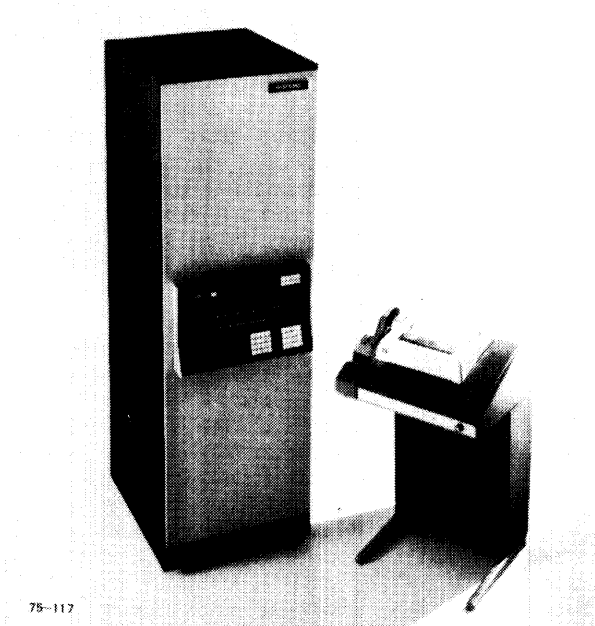
## TYPICAL PRICES (Contd.)

Model Number	Description	Monthly Rental \$	Purchase Price \$	Monthly Maint. \$	Model Number	Description	Monthly Rental \$	Purchase Price \$	Monthly Maint. \$
51406	Same as 51404 except attaches to the 51405	550	9,000	50	52101	<b>Card Punch</b> Card Reader and Controller (80-col cards; 300 cpm)	190	4,000	25
51490/590	Hardware Chaining	50	1,500	10	52102	Same as 52101 except 1,000 cpm	285	6,500	40
51491/591	Extended Cabinet Option (65-in. high cabinet with magnetic tape drive)	5	200	NA	52103	Card Punch and Controller (100 to 400 cpm)	1,400	22,000	130
51502	Same as 51402 except attaches to 51501	295	5,300	30	52201	<b>Printers</b> Printer/Plotter and Controller (11-in. paper; 10.56 in. print/plot line; 1,200 lpm print; 3 ips plot)	555	15,000	85
51504	Same as 51502 except attaches to 51503; 75 ips	410	8,000	45	52202	Same as 52201 except 22-in. paper; 21-in. print/plot line	780	17,300	100
51505	Controller for up to 4 51506s	310	5,500	30	52302	Line Printer and Controller (64-char set, 132 col, 1,250 lpm)	1,685	29,800	175
51506	Same as 51504 except vacuum column, for 51506s	425	9,000	50	52303	Same as 52302 except 245 to 1,110 lpm	1,070	17,500	100
51509	Same as 51505 for up to 4 51510s	540	12,000	85	52304	Line Printer and Controller (80-col; 64-char set; 356-1,110 lpm)	735	12,000	70
51510	Magnetic Tape Drive (vacuum col drive for 51509; 75 ips; 9-track; 800 and 1,600 bpi; IBM and ANSI compatible)	580	14,000	100	52401	Digital Plotter and Controller (Calcomp 565 Plotter)	550	9,000	50
51601	Magnetic Tape Controller for up to 2 51602s	715	15,000	105	52402	Digital Plotter and Controller (Calcomp 563 Plotter)	705	11,500	65
51602	Magnetic Tape Drive (vacuum col, for 51601; 45/90 ips; 21-track; and 712/356 bpi)	1,870	30,000	210	52403	Digital Plotter Controller	550	3,500	50
52001	<b>Paper Tape</b> High-speed Paper Tape Reader; 8-channel; 300 cps	110	2,800	15	52501	<b>Teleprinters</b> ASR-33 Teletypewriter for use with CPU	80	12,000	5
52002	Paper Tape Punch and Controller (HS paper tape punch; 8 channel; 110 cps)	175	3,300	20	52502	ASR-35 for use with CPU	255	4,100	25
52003	Paper Tape Reader, Punch, and Controller (HS paper tape rdr/pnch; 300 cps read; 110 cps punch)	260	5,500	30	52503	ASR-33 for use as terminal	80	1,200	5
52004	Paper Tape Reader Spooler (tension for takeup and supply of paper tape with 52001)	90	4,000	25	52504	ASR-35 for use as terminal	255	4,100	25
					52602	<b>A/N Display</b> A/N Graphics Display	295	5,400	30
					52604	Display Copy unit	255	4,000	25
					52702	<b>Data Communications</b> Serial Line Multiplexor for DIO Bus	125	2,500	15
					52706	Terminal Controller for DIO Bus	40	1,000	5
					52740	Bisync Modem Controller for DIO Bus	165	3,000	15
					52801	Programmable Interval Timer for DIO Bus	35	700	5
					52802	Time-of-day Clock (resolution is 1 msec)	20	600	5

NA — Not Available

# SYSTEMS ENGINEERING LABORATORIES

## SEL 32 System Report



75-117

### OVERVIEW

The SEL 32 is a microprogrammed 32-bit midcomputer designed by the manufacturer of the SEL 86, a 16-bit/32-bit system that has been popular in the process control market. The SEL 32 is a totally new system, but it implements the SEL 86 instruction set; thus, it appears to be an SEL 86 with increased flexibility. The SEL 32 gives the manufacturer a better competitive edge in the general purpose market, as well as in real-time, measurement, and process control, the company's traditional markets. The SEL 32 is extremely modular, currently ranging in size from 32K-bytes to 1,024K bytes of memory; the processor can address up to 16M bytes. Multiprocessor systems can be configured in a number of ways. The main operating system allows real-time foreground/background processing. The overall hardware is versatile and fast enough to be efficient in a wide variety of markets.

Initially, the SEL 32 has two models, which differ only in packaging. The 32/50 is an OEM version without cabinet and power supply; the 32/55 is an end-user system. Both models use the same operating system, software, and peripherals developed for the SEL 86, and both will be marketed for measurement and control applications, SEL's traditional markets.

The SEL 32 is designed around a 32-bit word. It implements 152 instructions. The CPU uses micropro-

grammed logic, implemented in firmware. Two boards implement the arithmetic logic and one board implements the instruction set. The micrologic uses a 150-nanosecond, single-clocked cycle. The CPU uses a mini pipeline and always has three 32-bit instructions in various stages: while one instruction is being executed, a second instruction is being decoded and a third is being fetched. About 30 percent of the instructions are half-word instructions; thus, the mini pipeline theoretically can store up to six half-word instructions.

All system units communicate with each other via the SEL bus, (which can operate at the rate of 26.67 million bytes per second) in a fashion reminiscent of the PDP-11. The SEL bus, however, is synchronous but allows asynchronous I/O and memory, which interface to the bus via Input/Output Microprocessors (IOMs) and Memory Bus Controllers (MBCs). Unlike the PDP-11, the priority of various system elements attached to the bus are determined by switches on the attached module rather than by the position of the module relative to the CPU. The switches and address lines allow for 23 bus priority levels.

MBCs control banks of up to 512 bytes each, which can be shared between two SEL 32 processors by simply attaching another MBC to the same memory bank. Processors can also be attached via interbus links. These two methods can be combined to make multiprocessor systems that interconnect in a variety of ways.

SYSTEMS Engineering Laboratories is not one of the giants of the minicomputer/midcomputer marketplace, but it has managed to carve out a competitive niche in the measurement and control markets, first with hardwired systems in the early 1960s and later with computerized systems. The company has done particularly well in the custom design of systems for nuclear power plant control. It produced the SEL 810 and 840 (1966), the larger 86 (1969), and the software compatible 85 (1970). All these systems except the 840 are still in production. Although the company has had financial problems, its financial picture has improved substantially this year; outstanding

### HEADQUARTERS

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debt was cut in half. The SEL 32 should be successful. It is a powerful but low-cost system. Order backlog reached \$4,000,000 in July 1975, with first delivery due in the 3rd quarter 1975. Table 1 lists the mainframe characteristics.

**Table 1. SEL 32: Mainframe Specifications**

<b>Characteristics</b>	SEL 32
<b>Central Processor</b>	
Microprogrammed	Yes
Control Memory	ROM
No. of Registers	8:3 can be used as index regs
Word Length	32
Addressing	
Direct	To 512K bytes
Indirect	Multilevel to 16M bytes
Indexed	Pre- and post-indexing
Mapping	Yes, to 16M bytes
Instruction Set	
Implementation	Firmware
Types	Half- and full-word
Number	152
Floating point	Firmware std
Hardware Stack	No
Instruction Execution	
Times ( $\mu$ sec)	
Fixed Point	
Add	1.2
Multiply	4.5
Divide	5.1
Floating-Point	
Add	2.5
Multiply	4.5
Divide	8.9
Writable Control Store (256 56-bit wds)	No
Interrupts	
Levels	128
Type	Hardware
<b>Main Storage</b>	
Type	Core
Cycle Time ( $\mu$ sec)	0.6
Basic Addressable Unit	Doubleword, word, halfword, byte bit
Bytes/Access	4
Cache Memory	No
Capacity (bytes)	
Min	32,768
Max	1,048, 576
Increment Size (bytes)	32K
Ports/Module	1
Error Checks	Parity; 1 bit/byte
Memory Protection	Yes in pages of 512 words
Memory Management	Yes
Interleaving	2 reads/ 4 writes
<b>Input/Output</b>	
Max Devices Addressable	Via I/O Controllers
Programmed I/O	Yes, IOC
DMA	IOC
DMA Transfer Rate	1.2M bytes/each; 26.7M bytes/sec aggregate; IOC
<b>Software</b>	RTM: Real Time foreground/background system; IBM 2780, IBM 1100 and CDC 200 Emulators FORTRAN IV, Macro; SCORE (standalone system)

**COMPETITIVE POSITION**

With the introduction of its SEL 32, SYSTEMS Engineering appears to have a robust contender in the real-

time, data processing market. SYSTEMS Engineering has floundered in the past by producing new high-performance but incompatible products. The SEL 32 is another matter — it is totally compatible with the SEL 86 in software and performance, and it competes with the top-of-the-line minicomputers in price. Customers are also recognizing its merits with advance orders, so SYSTEMS Engineering now has a substantial backlog. First deliveries are scheduled for third quarter 1975.

Recognizing the competition from top-of-the-line minis in the relatively large-scale, real-time processing market — SYSTEMS Engineering redesigned the SEL 86 using LSI-MSI circuitry to reduce both the amount of hardware and the price. The SEL 32 CPU, for example, is on three large boards instead of the more than 100 small boards in the SEL 86 CPU.

As shown in Table 2, the SEL 32 competes favorably in performance and price when compared to the latest top-of-the-line minicomputers or midcomputers: the Digital PDP-11/70 and the Interdata 8/32. SYSTEMS Engineering appears to have a winner in its traditional, strong markets — measurement and control. Initial orders are primarily from utility companies. The company's experience combined with truly competitive hardware will be hard to beat.

Expanding the sales effort into other markets will be another matter. Currently, the company is more limited in its complement of peripherals and software than Digital Equipment, Data General, Hewlett-Packard, Modular Computer Systems, General Automation, as well as Interdata.

The market is large, however, and success hinges on the ingenuity a company displays in selecting specific products to market.

**Configuration Guide**

A minimum end-user 32/55 system consists of CPU and SEL Bus with 32K bytes (8K 32-bit words) of memory; the Real Time Option Module (RTOM) with real-time clock and interval timer; floating point firmware; turnkey panel; single equipment cabinet, and 10 SEL bus slots. Packaged submodels of 32/55 differ in base memory size, base memory expansion, and number of bus slots.

Model	Configuration
2202	32K bytes expandable to 256K bytes, 10 slots
2204	32K bytes expandable to 256K bytes, 28 slots
2206	288K bytes expandable to 512K bytes, 28 slots
2210	544K bytes expandable to 768K bytes, 10 slots
2212	544K bytes expandable to 768K bytes, 28 slots
2214	800K bytes expandable to 1,024K bytes, 10 slots





**Table 2. Comparison of SEL 32 With Some Competitors**

SYSTEM	SEL 32	Interdata 8/32	DEC PDP-11/70	Data General Eclipse S/200
<b>Central Processor</b>				
No. of Registers	8	32; 128 opt	16	4
<b>Addressing</b>				
Word Length	32	32	16*	16
Direct, No. of bytes	512K	1024K	64K	64K
Mapping, No. of bytes	4096K	1024K	2048K	256K
No. of Instructions	152	214	400-446	86-152
Max Devices Addressable	128	1024	No limit	59
Interrupt Levels	128	1024	8	16
Max DMA, rate/SOC	6MB	6MB	4MB (Unibus) 5.8MB (HSDC)	2MB
<b>INSTRUCTION EXECUTION</b>				
<b>TIMES, <math>\mu</math>sec</b>				
Fixed-Point Add	1.2	1.1	3.1	0.6
Fixed-Point Multiply	4.5	5.6	5.3	7.2
Fixed-Point Divide	5.1	5.7	9.9	9.6
Floating-Point Add	2.5	2.0	9.9	2.4
Floating-Point Multiply	4.5	3.2	11.9	3.9
Floating-Point Divide	8.9	5.0	12.9	4.6
<b>Main Storage</b>				
Main Memory Core	Core	Core	Core	Core; MOS
Type Cycle Time, $\mu$ sec	0.6	0.75	1.0	0.8; 0.7
<b>Cache</b>				
Type	None	Stack	Bipolar	Bipolar
Cycle Time, $\mu$ sec	—	0.24	0.24	0.20
Interleaving	2-way read 4-way write	4-way	2-way	8-way core 4-way MOS
<b>SOFTWARE</b>				
Operating Systems	RTM; real-time & batch system; text editor for time-sharing		IAS, Real-time & timesharing & batch, also RSTX/E, RSX-D	
Compilers/Interpreters	FORTRAN IV, Macro assembler		Macro assembler	
Emulators	None		2780	

\*With 32-bit wide bus between High-Speed Data Controllers (HSDC) and memory and between memory and cache

The OEM 32/50 Model is the same as the 2202, except it is in a single chassis without cabinet and power supply.

Systems can be expanded in several ways: 32K-byte memory modules can be added, RTOMs can be added (eight interrupt levels each) and I/O capacity can be increased. Increasing I/O upgrades Models 2202, 2206 and 2210 to Models 2204, 2208, and 2212, respectively. Increasing memory beyond the basic capacity changes Models 2202/2204s into 2206/2208s, then into 2210/2212s, then into 2214s (no Model 2216). Upgrading requires a field upgrade kit.

Each I/O device connects to the SEL bus via Input/Output Microprocessors (IOMs), as shown in Table 3. Two IOMs allow processors to be linked together: the 9122 asynchronous data set interface and the high-speed data interface.

Processors can share access to common data banks via a common memory bus, or SEL busses can be linked together. Memory modules do not directly interface to the

SEL bus, but pass through Memory Bank Controllers (MBC). Each supports up to 512K bytes of memory (16 memory modules). By interfacing two MBCs to a common memory bus but to different SEL busses, two processors can share the same memory bank, even if the SEL busses are not linked together. Thus, multiprocessor systems can be configured with linked SEL busses or with shared memory banks or with both, and a single system can be linked with several other systems in different ways. This highly modular concept allows considerable flexibility in multiprocessor configurations, and control of specific peripherals can be distributed, each assigned to specific CPU.

Software packages, of course, make their own configuration demands. The basic standard software packages are listed in Table 4, together with brief descriptions and, wherever appropriate, configuration requirements. In addition to those listed, SEL offers "tailored" systems based on adaptations of other standard packages designed for this purpose, particularly in process control, timesharing and communications.

**Table 3. SEL 32: Peripherals**

Model Number	Performance Characteristics
<b>Console</b>	
9201 KSR 33 Teletypewriter	10 cps
<b>Cards</b>	
9210/9211 Card Readers	285/1,000 cpm
9215 Data Recorder	200 cpm reader, 45-75 cpm punch; keyboard
9216 Data Recorder	Interpreting version of 9215
9217 Card Reader/Punch	200 cpm reader, 45-75 cpm punch
9218 Card Reader/Punch	Printing version of 9217
9219 Card Punch	100 cpm
<b>Printers</b>	
9224 Serial Printer	100 char/sec; 132 columns
9225/9226 Line Printers	300/600 lpm; 136 columns
<b>Discs</b>	
9306 Moving Head Disc	5 MB/cartridge; 4 drives/controller
9308 Moving Head Disc	10 MB/cartridge; 4 drives/controller
9320 Moving Head Disc	80 MB/pack; 4 drives/controller
9335 Fixed Head Disc	1 MB/disc, 4 drives/controller
9336 Fixed Head Disc	2 MB/disc, 4 drives/controller
<b>Magnetic Tape</b>	
9360 Mag Tape Drive	7-track; 556/800 bpi, 45 ips; 4 drives/controller
9361 Mag Tape Drive	9-track; 800 bpi; 45 ips, 4 drives/controller
9362 Mag Tape Drive	9-track; 1,600 bpi; 45 ips; 4 drives/controller
9363 Mag Tape Drive	9-track; 800/1,600 bpi; 45 ips; 4 drives/controller
9374 Mag Tape Drive	7-track; 556/800 bpi; 75 ips; 4 drives/controller
9375 Mag Tape Drive	9-track; 800 bpi; 75 ips; 4 drives/controller
9376 Mag Tape Drive	9-track; 1,600 bpi; 75 ips; 4 drives/controller
9377 Mag Tape Drive	9-track; 800/1,600 bpi; 75 ips; 4 drives/controller
<b>Communications</b>	
9122 Async Interface	Programmable, 4 channels; can link 2 busses
9124 Sync Interface	Programmable, 4 channels
9126 MUX	To 128 lines
<b>Special</b>	
9142 Analog/Digital	6 types of subsystems
9162 General I/O	Blank IDM, no device logic
9132 High Speed Data Interface	Can serve as interbus link, or link to special devices
9134 Serial Data Interface	For attaching special devices

**Compatibility**

The SEL 32 is completely hardware and software compatible with the SEL 86. Programs can be run without al-

**Table 4. SEL 32: Software**

Package	Description
<b>Real Time Monitor (RTM)</b>	Disc-oriented multiprogramming foreground/background system; requires CPU, 128K bytes of memory RTOM option, KSR-33 console, card reader or reader/punch, printer, at least 2MB disc, mag tape
<b>SCORE</b>	Minimum system for program development or small applications; requires 32K bytes memory without assembler or 64K bytes with assembler, plus one input and one output device
<b>FORTRAN IV</b>	ANSI standard with extensions for real-time multiprogramming, runs under RTM as std feature, so no extra memory required
<b>Macro Assembler</b>	Assembler for RTM, with unlimited nesting and recursion of macro structures; runs under RTM as standard feature, so no extra memory required; extra 32K needed for SCORE
<b>Utilities</b>	Mathematical subroutine library; FORTRAN support library, scientific subroutine library, and three diagnostic packages

teration, and Model 86 peripheral devices can be attached. A new 800/32 translator also allows SEL 800 series programs to be translated into SEL 32 programs.

Emulators allow the SEL 32 to "look like" an IBM 2780, an IBM 1100, and a CDC UT 200.

**MAINTENANCE**

SYSTEMS Engineering Laboratories has 14 U.S. sales and service offices, in addition to corporate headquarters in Florida. The company also has offices in Canada, France and Germany.

The standard maintenance contract is prime shift — on call service. Travel charges are added if the installation is more than 25 miles from the service area, or for after-hour service.

SYSTEMS Engineering does not lease its systems.



## TYPICAL PRICES

Model Number	Description	Purchase Price \$	Monthly Maint \$
<b>Central Processor and Working Storage</b>			
2202	SEL 32/55 with 32K Bytes memory	25,000	225
2204	Same as 2202 with 28 Slots	27,000	240
2206	Same as 2202 except 288K bytes core memory expandable to 512K bytes	78,000	730
2208	Same as 2206 with double equipment cabinet and 28 SEL bus slots	81,000	745
2210	Same as 2202 except 544K bytes core memory expandable to 768K bytes; double equipment cabinet	138,000	1,260
2212	Same as 2210 with 28 SEL bus slots	140,000	1,275
2214	Same as 2210 except with 800K bytes of core memory expandable to 1,024K bytes	191,000	1,765
2200	Same as 2202 except 32K bytes of core memory, single chassis without cabinet and power supply and 4 bus slots	18,000	200
2201	Same as 2200 except double chassis, 256K bytes of core and 10 bus slots	21,450	185
<b>Processor Options</b>			
2230	Dual Processor Integrator	**	**
2112	Real-time Option module	2,500	20
2142	System Control Panel	3,000	25
2145	Hexadecimal Display	600	5
2149	Over 512K Bytes Addressing Option	3,000	NC
2150	Memory Bus Controller	3,000	25
2152	32K Byte Memory Modules	6,300	60
2179	Memory Interface Adapter	3,000	25
2181	Logic Chassis	1,000	NC
2182	Memory Chassis provides slots for up to 8 memory modules and up to 2 MBC's	1,000	NC
2188	Maintenance Panel (test panel for accessing and displaying microprogram steps)	5,000	NC
2199	Bay Extender	300	—
2221/22	Input-Output Upgrade	**	**
2223/4/5/6	Memory Upgrade	**	**
<b>Mass Storage</b>			
<b>Disc</b>			
9008	Cartridge Disc Controller	3,000	25
9010	Moving Head Disc Controller	5,000	45
9301	Cartridge Disc Formatter	2,700	20
9306	Cartridge Disc Drive (5M bytes; 312K byte transfer rate)	6,000	75
9308	Cartridge Disc Drive (10M bytes; 312K byte transfer rate)	7,500	25
9320	Moving Head Disc Drive (80M bytes; 1.2M bytes transfer rate)	25,000	75
9321	Moving Head Disc Drive (40M Bytes; 1.2M bytes/sec transfer rate; 30M sec average access time)	18,000	165
9335	Fixed Head Disc Drive (1M Byte; 4.4M Hz; 8.5-msec average access time)	14,000	140
9336	Fixed Head Disc Drive (2M Bytes)	20,000	200
9014	Fixed Head Disc Controller	5,000	45
<b>Input-Output Interfaces</b>			
9102	General-Purpose I/O Module	2,500	25
9104	GP Multiplexor Controller	3,500	30
9122	Async Data Set Interface	3,000	30
9124	Sync Data Set Interface	3,500	30
9126	Communications Subsystem interface	3,500	30
9132	High Speed Data Interface	4,000	30
9134	Serial Data Interface	4,000	35
9136	Inter-Bus Link	6,000	50
<b>Teleprinters</b>			
9201	KSR-33 Teletypewriter	1,600	25
<b>Punched Card</b>			
9210	Card reader (285 cpm)	3,000	55
9211	Card reader (1,000 cpm)	6,000	95
9004	TLC Controller	2,500	25
9006	Card Punch Controller (requires 2 slots)	3,000	25
9215	Data Recorder (card reader-punch; 200/45-75 cpm with keyboard)	14,500	200
9216	Interpreting Data Recorder (card reader/punch/printer; 200/45-75 cpm with keyboard)	16,500	200
9217	Card Reader/Punch (card reader; 200 cpm; punch 45-75 cpm)	12,500	200
9218	Printing Card Reader/Punch (200 cpm; punch/printer 45-75 cpm)	14,500	200
9219	Card Punch (100 cpm, 80 col)	20,000	200
<b>Printers</b>			
9220	Serial Printer (100 cps; 132 cols)	4,000	40
9225	Line Printer (125 lpm; 132 cpl)	5,800	86
9225	Line Printer (300 lpm; 136 cols)	10,000	95
9226	Line Printer (600 lpm; 136 cols)	16,000	200
<b>Magnetic Tape</b>			
9350	Tape Formatter (7- 9-track NRZI, supports up to 4 transports)	2,000	15
9351	Tape Formatter (9-track, PE; supports up to 4 transports)	3,000	24
9352	Tape Formatter (9-track, NRZI/PE; supports up to 4 transports)	4,000	30
9360	Magnetic Tape Transport (tension arm; 45 ips; 7-track; 556/800 bpi; NRZI, 10-1/2 in. reel)	5,000	75
9361	Same as 9360 except 9-track, 800 bpi	5,500	75
9362	Magnetic Tape Transport (tension arm; 45 ips, 9-track, 1,600 bpi; PE; 10-1/2 in. reel)	8,000	75
9363	Magnetic Tape Transport (tension arm; 45 ips; 9-track; 800/1,600 bpi; NRZI/PE 10-1/2 in. reel)	9,000	80
9374	Magnetic Tape Transport (Vacuum Col; 75 ips; 7-track; 556/800 bpi; NRZI, 10-1/2 in. reel)	14,000	90
9375	Magnetic Tape Transport (Vacuum Col; 75 ips; 9-track; 800 bpi; PE; 10-1/2 in. reel)	15,000	90
9376	Same as 9375 except 1,600 bpi	16,000	90
9377	Same as 9375 except 800/1,600 bpi; NRZI/PE	17,000	100
9012	Magnetic Tape Controller (interfaces to 1 formatter with up to 4 transports requires two bus slots)	3,000	25
9399	Peripheral Cabinet	1,000	NC
<b>Software</b>			
1001	Real-Time Monitor		
	Binary	1,500	
	Source	2,500	
1021	Standalone Software System		
	Binary	0	
	Source	250	
1011	Macro Assembler		
	Binary	0	
	Source	1,500	
1012	FORTRAN IV Compiler		
	Binary	800	
	Source	2,500	

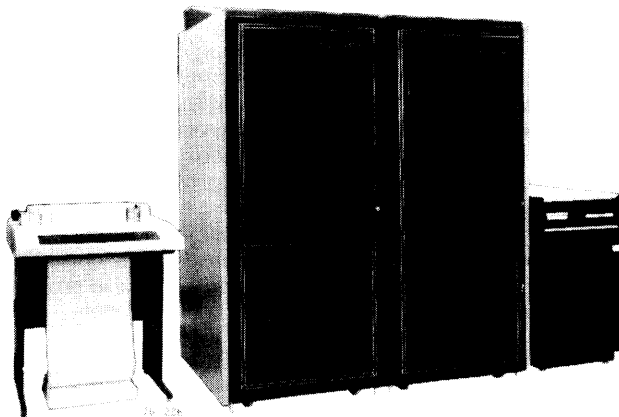
Notes:

- \* Home Office Quote
- \*\* Price depends on configuration; available on request from SEL
- Not Applicable
- NC No Charge



## TANDEM COMPUTERS INC.

### Tandem 16 NonStop™ Systems, System Report



#### OVERVIEW

The Tandem 16 NonStop system is a true multiprocessing system that can accommodate two to sixteen processors along a central bus. It has been designed to achieve zero downtime even in the case of full or partial system failure. This philosophy is supported by the modular construction of the NonStop system — many system elements are doubled, including the interprocessor bus, the DYNABUS™, and as normal procedure run in parallel. In case of failure, redundant elements can perform processing functions while the failed module is being replaced or repaired.

Tandem is aiming the NonStop system at the transaction processing market as a dedicated system for controlling large numbers of terminals. Tandem feels that the failsafe capabilities of the NonStop system are well-designed for transaction driven events, and thus it will find a home in funds transfer, on-line order entry, inventory, retail credit checking, and manufacturing environments. Although the Tandem 16 has been designed as a stand-alone system, it can also be used to front-end a mainframe computer.

To date, only a dual-processor configuration has been realized, which leaves the reality of a working system with sixteen processors a matter of conjecture. Also, the elegant hardware of the Tandem 16 is hampered by the lack of appropriate supporting software. Tandem only offers a virtual memory operating system (T/TOS) for program loading, memory and file management, and hardware diagnostics; a source language compiler (T/TAL); and system generator (TOSYGEN). Communications software and data base management software are noticeably lacking, as well as certain utilities, including sort/merge. Also, applications programming is expected to be handled by the user, and since special programming techniques must be

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learned for implementing continuous operation, the user must employ a staff of highly trained programmers.

Tandem Computers Inc. is a new minimaker, incorporated in November 1974. The company borrowed \$1 million in backing its first year and \$2 million in October 1975; at the time of writing, it still had \$1 million to its credit. The first multiple-processor system was delivered in May 1976. See Table 1 for system specifications.

**Central Processors.** Each processor is a 16-bit minicomputer composed of two 32-bit microprocessors (both microprocessors can address the memory associated with the processor independently); it is roughly equivalent in power to the processors in the upper end of the Data General Eclipse or DEC PDP-11 line, and is manufactured by Tandem. The processor has an internal clock speed of less than 100 nanoseconds. There are sixteen internal interrupt levels; for example, the first is POWER ON, the second is CPU, the third is PARITY ERROR IN MEMORY. Each interrupt level has 32 sublevels. Each processor has its own power supply. In case of power failure, the processor can SAVE its current state. It can be restarted after the source of power failure has been corrected. Each processor has six general-purpose registers. They are arranged in a stack that operates automatically during the normal operation of the system, but the stacking procedure can also be put under direct program control, if desired. There are three index registers per processor.

Each processor has its own memory. There is no direct memory sharing. Both core and semiconductor memory modules are available.

- Core memory is available in 64K-byte modules arranged in 32K words of 16 data bits plus parity bit. Up to four of these modules may be controlled by a processor, giving a maximum core memory of 256K bytes. Core memory modules have a read access time of 500 nanoseconds and a cycle time of 800 nanoseconds.
- Semiconductor memory modules are available in 32K and 64K versions. Cycle time is 500 nanoseconds for both. Single-bit errors are corrected, and double-bit errors are trapped. The 32K-byte version is arranged as 16K words of 16 data bits plus 6 error detection bits.

#### HEADQUARTERS

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**Table 1. Tandem 16: Mainframe Characteristics**

<b>Central Processors</b>	
Possible Number	2-16
Type	Microprogrammed
<b>Registers</b>	
Number of general purpose registers	6
Number of index registers	3
<b>Addressing</b>	
Direct (Number of words)	512
Indirect (Number of words)	256K
Indexing	Post-indexed
Mapping	Under system control
<b>Instruction Set</b>	
Implementation	ROM
Number of instructions	122
Decimal arithmetic	Yes
Floating point arithmetic	No
User microprogramming	No
<b>Priority Interrupt System</b>	
Internal levels	16 (each with 32 sub-levels)
I/O levels	2 (each with 32 sub-levels)
<b>Main Storage</b>	
Type	Core or semiconductor
Cycle time	800 nsec for core 500 nsec for semiconductor
Basic addressable unit	Word (16-bit)
Bytes per access	2
Min capacity	64K for core 32K for semiconductor
Max capacity (bytes)	256K for core 512K for semiconductor
Increment size (bytes)	64K for core 32K for semiconductor
Ports per module	2
Error checks	Parity bit for core 6 error detection/correction bits for semiconductor
Protection method	Automatic
Memory management	Automatic
<b>I/O Channels</b>	
Type	Multiplexed DMA only
Number of output channels	32 per bus
Programmed I/O	System utility routines provided
Transfer rate	2.5 MB for core 4.0 MB for semiconductor

The 64K-byte version is arranged as 32K words of 16 data bits plus 6 error detection bits. A single processor can control up to eight modules of either version, giving a maximum capacity of 512K bytes of semiconductor memory. The semiconductor memories have battery support in case of power failure.

**Processor Interaction.** The processors can talk with one another over an interprocessor bus, called the DYNABUS™ (See Figure 1 for Tandem 16 organization). There are two of these busses working in parallel, and either one can handle all bus tasks if the other is down. Interprocessor communication occurs over the busses in 16-word multiplexed packets, of which 15 words are data and 1 word is the packet check sum. Bus speed is 10M bytes per second. Bus-receive logic in each processor assigns priority to one of the two busses. Each bus has its own bus controller; it handles bus priorities and synchronizes the processors' clocks. Each processor has a 16-word buffer for each bus.

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**I/O Structure.** Up to 32 device controllers can be connected to a single processor. Each controller has two independent ports, allowing it to be connected to two processors. Because each of the two processors has its own power supply, in case of failure any controller can draw on the power supply of a second processor.

The controllers are connected to their processors via an I/O bus, which is in effect a Direct Memory Access (DMA) channel. Essentially, therefore, all peripherals communicate with the processors over a DMA. The I/O bus is controlled by an I/O channel in the processor; it has two interrupt levels, standard and high priority. Each I/O interrupt level can have up to 32 sublevels, providing a means of signaling device error numbers in case of peripheral failure. A controller normally accepts commands from only one processor but can be programmed to accept commands from the second also, particularly in case of processor failure.

The I/O bus transmits blocks of 1 to 4094 bytes. Each word has a parity bit for error checking. I/O bus data flow is multiplexed. Processors with semiconductor memory have an I/O bus speed of 4.0M bytes per second. Core memory processors have an I/O bus speed of 2.5M bytes per second.

**Peripherals.** The following peripherals are available for the Tandem 16 (see Table 2 for listing of peripheral devices).

- 10MB and 50MB CDC formatted moving-head disc drives. Each disc controller can handle 4 disc drives, and there may be up to 128 controllers per processor, depending on other peripheral attachments. Each drive is connected directly to its controller; they are not daisy chained.
- Ampex magnetic tape units. Only a 9-track NRZI, 800 bpi, 45 ips unit is available. Two tape units may be attached to one magnetic tape controller. The system can read IBM standard label tapes, but the system will not automatically output IBM standard labels.
- Documentation card readers. Several controllers are available for card reader control. These controllers can handle one or two card readers, or one card reader plus a line printer. Card reader speed is 600 cpm for 80-column cards.
- Line printers for the Tandem 16 use 64-character ASCII and can have cable lengths of up to 25 feet. A GE 120 printer with a maximum speed of 300 lpm for a 120-character line is at the low end of the available spectrum. Data Products 300-, 600-, 900-, and 1500-lpm 132-column printers form the rest of the printer range offered. These printers all have 12-channel VFU. Up to two line printers can be attached to a controller. A Universal Interface is offered to facilitate the attachment of other peripherals to the system.
- A Lear-Siegler "glass" teletype and a 1920-character CRT with keyboard are currently available as terminals. Terminals may be hardwired to the system or operate over modems. The asynchronous communications controller speed is program dependent and can



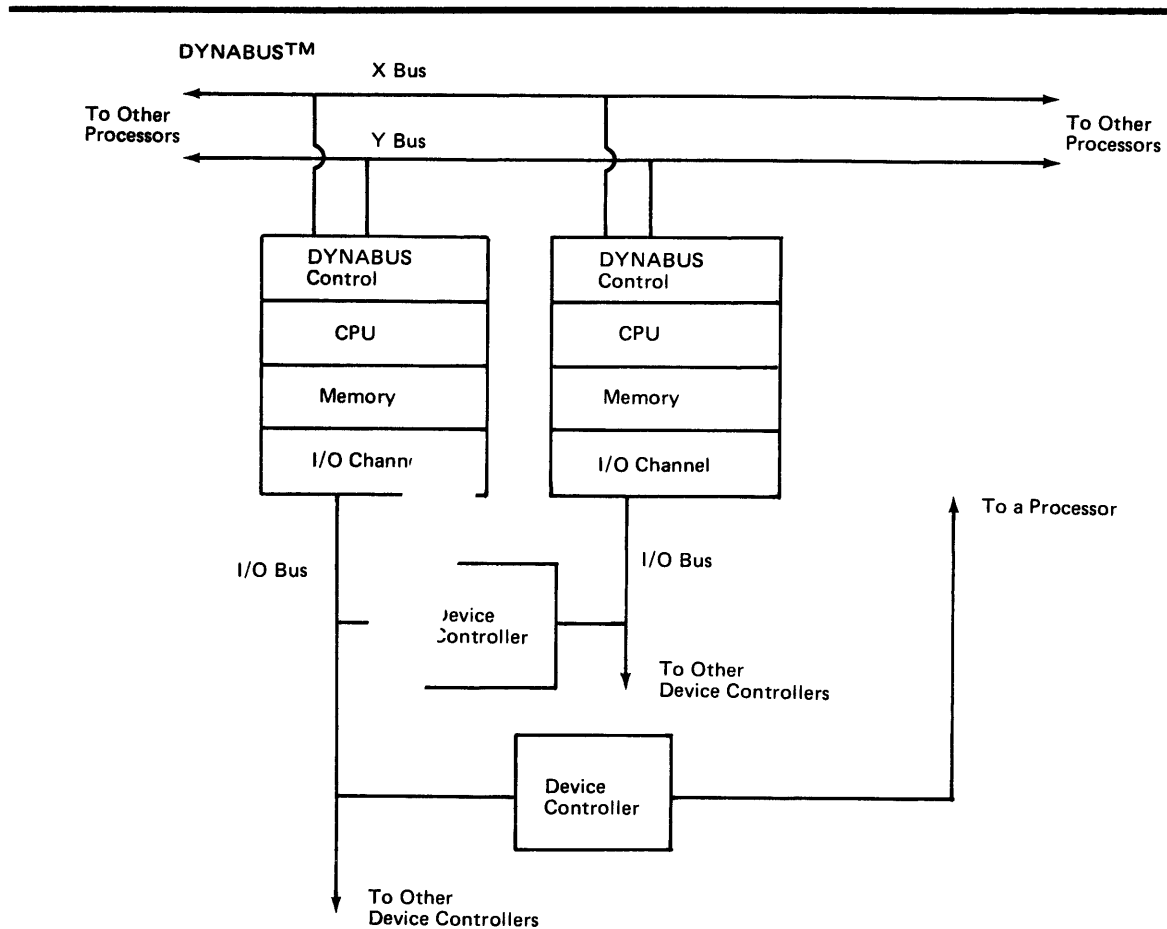


Figure 1. Tandem 16 Organization

vary from 50 to 1920 bps. Each controller has two lines, but it can be complemented by an extension board that provides control for up to 15 lines. In theory, a processor can control as many as 128 lines. With 128 lines per bus and a bus speed of 4M bytes per second, the Tandem 16 makes a powerful terminal controller.

**Software.** The Tandem 16 operates under a multiprogramming operating system called Tandem's Transaction Operating System (T/TOS). As its name indicates, it is designed to facilitate transaction processing. Its main operational task is to coordinate the processor modules, test hardware, and allow the programmer to ignore the actual hardware structure of the machine.

T/TOS is 60 to 80K bytes in size, depending on peripheral configuration. Not all of T/TOS need reside in main memory, but typically 60K of memory will be occupied by systems software at any time, the rest being swapped out to disc.

Copies of T/TOS reside in each processor's memory; for each processor it handles program loading, memory resource allocation, process prioritization, processor interaction, and device control. T/TOS automatically maps memory into four parts (the user cannot override this process): one part for system code, one part for system data, one part for user code, and one part for user data. Only data areas can be written to by the user.

Data areas are arranged as last-in-first-out (LIFO) stacks. Code sections are in read-only memory. All program code and data are relocatable.

A system generation program, TOSYGEN, allows T/TOS parameters to be changed, so that peripheral configurations may be varied. It also allows programs to be designated for automatic starting. The command interpreter, COMINT, can be used by the operator for communicating with the system. The text editor, EDIT, can be called by an applications program, in order to operate in cooperation with it, as well as being used for editing or creating programs. UPDATE can be used to edit compiled

Table 2. Tandem 16: Peripherals

Device Model No.	Description
	<b>Asynchronous Communications</b>
T16/6301	Asynchronous controller, 50-19,200 bps
T16/6302	Asynchronous extension board, to 15 asynchronous lines per board, 2 boards per controller
T16/6701	Hard copy terminal, 30-cps, 132-column printer, current loop interface
T16/6702	Hard copy terminal, 30-cps, 132-column printer, RS232C interface
T16/6511	CRT with keyboard, 24 lines, 80 char per line, switched speeds from 110 to 19,200 bps
T16/6511	CRT terminal with page mode. Not yet available
T16/6552	CRT terminal with polling protocol. Not yet available
	<b>Disc Equipment</b>
T16/3101	Disc controller, can control up to 4 disc drives
T16/4101	Moving head disc drive, 10 MB (CDC drive)
T16/3102	Disc controller, can control up to 4 disc drives
T16/4102	Moving head disc drive, 40 MB (CDC drive)
T16/4103	Moving head disc drive, 80 MB (not yet available)
	<b>Magnetic Tape Equipment</b>
T16/3201	Magnetic tape controller, can control 2 tape drives
T16/5101	Magnetic tape drive, 45-ips, 9-track, 800-bpi NRZI
	<b>Card Equipment</b>
T16/3303	Card reader controller
T16/3304	Card reader controller, can control two card readers
T16/3305	Card reader/line printer controller
T16/5301	600-cpm 80-column card reader
	<b>Printer Equipment (ASCII)</b>
T16/3301	Line printer controller
T16/3302	Line printer controller for two line printers
T16/5501	300-lpm 120-column line printer
T16/5502	300-lpm 132-column Data Products line printer
T16/5503	600-lpm 132-column Data Products line printer
T16/5504	900-lpm 132-column Data Products line printer
T16/5505	1500-lpm 132-column Data Products line printer
	<b>Interfaces</b>
T16/3401	Universal interface, TTL level 16-line controller
T16/3402	Universal interface, differential line drive/receive, 16 lines
T16/3403	Universal interface, TTL level controller for two devices
T16/3404	Universal interface differential line drive/receive controller for two devices
T16/3405	Universal interface for two devices, uses TTL level for one device and differential drive/receive for the other

programs or to combine two or more compiled programs. DEBUG can be used for program testing from a terminal.

The normal cold start-up procedure is to first use EDIT to fill in the necessary parameter values on the system discs. TOSYSGEN is then used to generate the operating system. Tandem 16 operation requires no special skills on the part of the operator. Additional processors can be added to a system by using TOSYSGEN calls.

See Table 3 for a tabulation of Tandem 16 software offerings.

**Programming.** The Tandem 16 is normally programmed in TAL (Transaction Application Language), a

high-level procedure-oriented language similar to ALGOL and PL 1, which was developed by Tandem to facilitate real-time programming. Applications programs in TAL usually reside in only one of the memories, whence it is available through the operating system to all the processors. The operating system also allows one application to monitor and/or start another applications program, even though the programs are in different memories. The same applications program can also be run in two processors, to provide back-up. An interesting characteristic of TAL is that if several processors have the same peripheral configuration their I/O need be programmed only once.

The TAL compiler is a true compiler, not an interpreter, and it compiles into object code in one pass. Compilation speeds average 7000 lpm without disc involvement and 5000 lpm with disc involvement. One Tandem 16 system can accommodate both a TAL compiler and a COBOL compiler at the same time. COBOL will be commercially available in the third quarter of 1977. Tandem provides no cross-compilers for TAL.

There are 122 TAL instructions, including some for double-precision computation. TAL instructions can address bytes as well as words and strings. There are a few bit-oriented instructions as well. There are no multiple-word instructions.

For comparison, it can be noted that an integer ADD requires 0.5 microseconds, a MOVE requires 1.1 microseconds per word and 2.3 microseconds per byte, a SEND from one processor to another requires 150 nanoseconds per word, and a READ or WRITE require 6.3 microseconds. These times include the time required to fetch the instruction.

TAL does not have a program library. The systems utility packages it can use are mostly I/O procedures, fail-safe procedures, and a SORT/MERGE that will be available in the first quarter of 1977. A data base system with VSAM access procedures is expected to become available in December 1976. Synchronous communications software is also expected to be available at that time.

Table 3. Tandem 16: Software

Package	Description
T/TOS	The operating system. Multiprogramming, multiprocessing, program loading, file management, memory management, virtual memory, hardware diagnostics.
TOSYSGEN	The system generator. Sets up the operating system for a given peripheral configuration.
T/TAL	The TAL source language compiler.
EDIT	The source code editor. Also initializes TOSYSGEN and can interact with running programs.
UPDATE	The object code editor. Can combine multiple compilations.
DEBUG	Applications programs test package. Break-points, traces, restarts.



Until that time, however, the user must construct his own program library. Also it should be noted that to implement Tandem NonStop programming techniques, special programmer training is required.

Benchmark tests have provided a transaction speed of 15K transactions per hour per processor using TAL programming. TAL can be used for terminal inquiry, but makes no provisions for background batch processing. Terminal emulation must be programmed in TAL, as Tandem supplies no terminal emulators.

The operating system breaks TAL applications programs down into processes. Each process is assigned a priority (level of 0 to 255) and is executed in the time slice that is assigned to it by the system's multiprogramming procedures. There may be up to 256 processes per processor. Program priorities, however, are supplied by the user.

The operating system divides the memory into pages of 2048 bytes. Each process may have up to 64 pages of code and 64 pages of associated data. The pages are not necessarily in sequence, as all TAL code and data are relocatable. If a disc is used for virtual storage, then the page swapping will be controlled by the system, and the programmer may ignore both the physical and logical locations of both code and data. Swapping to disc is used only for data that changes during program execution. A program may have its code and data in separate memories. Peripheral processes are controlled by the file-handling system.

## PERFORMANCE AND COMPETITIVE POSITION

To date, Tandem has sold the NonStop system only in a dual-processor configuration, though a four-processor configuration exists within the company. In dual processor configurations it competes directly in the minicomputer range of devices, and in larger versions it will compete with mainframe computers and grouped minis that are used for data networking.

In its dual version the Tandem 16 seems to be price-competitive with the larger minis; i.e., although it is slightly more expensive, it provides attractive features for transaction processing. In larger versions it will most likely gain a distinct price and performance advantage over large computers for applications that require fail-safe and continuous operation, easy and fast upward expansion of processing power, and memory size. Its price advantage over grouped minis derives from having a completed operating system (rather than a custom-made, and probably customer-paid-for, operating system) and from not requiring any additional hardware support for the addition of extra processors.

Despite its rather unique charter, the Tandem 16 will meet with many competitors, all of which offer the user viable alternatives for fail-safe operation. Included among them are Bolt, Beranek and Newmans' Pluribus, and the

Lockheed SUE with its Infibus. The Tandem 16 differs from both of them in accenting fail-safe operation. Pluribus and SUE provide degrees of fail-safe operation as a result of designs that have as their end goals other than fail-safe operation. Both devices, for example, lack the redundant modules of the Tandem 16. The SUE system is a small system aimed at commercial business uses, rather than at transaction processing *per se*. Pluribus, on the other hand, is aimed directly at data networking systems, rather than transaction processing.

Other competitors include companies now involved in equipment for systems such as airline reservation, as well as those engaged in the vast message switching and store and forward systems now beginning operation, for example, Collins and RCA. Competition may also come from semiconductor and microprocessor companies. Finally, there will be competition from the large-computer manufacturers. Multiprocessing is no stranger at Burroughs, for example, and IBM is definitely aiming at improved multiprocessing capabilities.

Although Tandem has yet to meet another competitor that makes the same claims for fail-safe operation, it seems likely that when the time comes the Tandem 16 may not be in the most desirable competitive situation. For example, system overhead is quite large; each processor must reserve upward of 60K bytes for the operating system, and program code cannot be swapped to disc. Thus at least one memory module is occupied by the operating system.

Applications such as controlling large terminal systems would also require another entire memory module for terminal control or data entry. And data base system software would also require a lot of memory space. In a dual system the extra memory might not be overly expensive, but with 16 processors the budget begins to hurt.

Tandem 16 also has a surprisingly small range of peripherals for a machine that is meant to expand and be sold as a system with more than two processors. For European sales, for example, a 7-track magnetic tape unit would certainly be necessary. For entry into the data acquisition market, the machine would need to have IBM-compatible flexible disc, and for the process control market paper tape equipment would be desirable. Most striking of all, however, is the limited variety of available terminals.

In the area of software offerings Tandem has a lot of work to do to remain competitive. Both system software as well as applications packages are needed. Because programming for a machine with many processors could become more complex than the average user would desire to bother with himself, applications software is particularly important.

All in all, the Tandem 16 seems to have a stretch of road to cover before it moves from the presently marketed dual-processor machine to a true multiprocessor system. Software and the money to invest in its development might prove to be its main problem.

# TANDEM COMPUTERS INC. — TANDEM 16 NONSTOP™ SYSTEMS, SYSTEM REPORT

## USER REACTIONS

Six Tandem machines have been ordered to date; all of them are dual-processor machines. None of the systems are yet in operation. The current customers are from the areas of banking, order entry, traffic control, manufacturing control, credit authorization, and process control. Users selected the Tandem 16 for its fail-safe and continuous-operation capabilities, large memory capacity, and low price/performance ratio.

One user will be employing the machine as a front end for terminal control into an IBM System/370; the other users will be employing the Tandem 16 as a stand-alone system.

## CONFIGURATION GUIDE

The smallest possible Tandem 16 configuration consists of a dual processor with 32K of core per processor, a 10-MB disc, a magnetic tape unit, an operator console, and 16 lines for terminals.

Tandem markets four packaged Tandem 16 configurations offering either core or semiconductor memory modules. The T16/212 consists of a dual processor with 64K bytes of core memory, two I/O channels, one 17-port communications multiplexor (asynchronous), a disc controller, a magnetic tape controller, and four unassigned I/O slots. An optional memory expansion of up to 128K bytes per processor is offered with this model.

The T16/214 is a core model including all of the features of the T16/212 with the option of expanding to four processors, each with up to 192K bytes of memory.

The T16/242 and T16/244 are configured in the same way as the T1/212 and T1/214, with semiconductor memory modules substituted for core memory.

## COMPATIBILITY

The Tandem 16 is the only machine made by Tandem Computers, Inc. Intermachine compatibility is provided through TOSYGEN and EDIT, which provide parameters for the operating system.

Standard synchronous communications is implemented by the Tandem 16.

## MAINTENANCE AND SUPPORT

The Tandem 16 can be maintained and repaired on-line; this includes preventive maintenance. Maintenance is provided by Tandem Computers, Inc., at its own offices in New York; Chicago; Los Angeles and Cupertino, California; Washington, D.C.; and Frankfurt, Germany. Outside these areas, maintenance is provided by independent service companies under contract. Twenty-four hour service is provided. Each office maintains its own spare-parts supply in the form of modules, rather than subcomponents.

Customer training consists of a three-week course at company headquarters: one week on TAL, the programming language; one week on T/TOS, the operating system, and one week on the special techniques of NonStop™ programming. Each office has a programmer-analyst to help customers with programming problems, but in general the customer is required to do his own programming.

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## PRICE DATA

Model No.	Description	Purchase Price (Maint. not Incl) \$	Monthly Maint. \$
<b>Packaged Systems</b>			
T16/212	Dual processor system with mapping, bootstrap, timer, DMA, powerfail/auto restart, 64K bytes, 800-nsec core memory, 2- to 2.5-MB/sec block multiplexed I/O channels, 17-port communications multiplexor, disc controller, magnetic tape controller, 4 unassigned I/O slots. Memory expandable to 128K bytes per processor	65,300	458
T16/242	Dual processor system like T16/212 except with 500-nsec semiconductor EDC memory, and 4.0-MB/sec I/O channels	67,300	628
T16/214	Expandable dual processor system, like T16/212 except the cabinet allows system expansion up to 4 processors with up to 192K bytes of memory each; and up to 4 block multiplexed I/O channels (1 per processor)	79,500	518
T16/244	Expandable dual processor system like T16/214 except with 500-nsec semiconductor EDC memory and 4.0-MB/sec I/O channels	83,500	858
<b>Central Processors and Working Storage</b>			
T16/1102	Core processor, with 2 subprocessors (program and I/O), DMA, mapping to 256K and hardware multiply/divide, bootstrap loading, power-fail auto-restart, interval timer, control panel, provision for up to 32 I/O controllers, and 64K bytes of 800-nsec core memory.	18,500	106
T16/1104	Core processor, like T16 but with 128K bytes of memory	26,500	136
T16/1106	Core processor, like T16/1102, but with 192K bytes of memory	34,500	166
T16/1108	Core processor, like T16/1102, but with 256K bytes of memory	42,500	196
T16/1402	Semiconductor processor, like T16/1102 except that 500-nsec semiconductor memory is used, I/O channel is 4.0 MB/sec, and mapping is to 512K bytes	19,500	191



**PRICE DATA (Contd.)**

Model No.	Description	Purchase Price (Maint. not Incl) \$	Monthly Maint. \$
T16/1403	Semiconductor processor, like T16/1402, but with 96K bytes of memory	26,000	227
T16/1404	Semiconductor processor, like T16/1402, but with 128K bytes of memory	28,500	306
T16/1406	Semiconductor processor, like T16/1402, but with 192K bytes of memory	37,500	421
T16/1408	Semiconductor processor, like T16/1402, but with 256K bytes of memory	46,500	536
T16/1410	Semiconductor processor, like T16/1402, but with 320K bytes of memory	55,500	651
T16/1412	Semiconductor processor, like T16/1402, but with 384K bytes of memory	64,500	766
T16/1414	Semiconductor processor, like T16/1402, but with 448K bytes of memory	73,500	881
T16/1416	Semiconductor processor, like T16/1402, but with 512K bytes of memory	82,500	996
T16/2102	<b>Memory</b> 64K-byte core memory module with parity 800-nsec cycle time	8,000	30
T16/2401	32K-byte semiconductor memory module with 6 error detection/correction bits per 16-bit word, 500-nsec cycle time	6,500	36
T16/2402	64K-byte semiconductor memory module with 6 error detection/correction bits per 16-bit word, 500-nsec cycle time	9,000	115
<b>INPUT/OUTPUT</b>			
<b>Terminal Subsystems</b>			
T16/6301	Asynchronous 2-channel controller, 1 line per channel, 50-19,200 baud per line; each channel can be expanded by attaching a T16/6302	1,700	15
T16/6302	Asynchronous 15-line extension board, provides control for up to 15 lines for each T16/6301 channel, 50-19,200 baud per line	3,100	18
T16/6701	Hardcopy terminal 30 cps, 20-mA current loop interface	2,500	31
T16/6702	Hardcopy terminal 30 cps, RS232C interface	2,600	31
T16/6401	CRT terminal, 1920 characters (80 x 24), 110-19,200 baud switch-selectable; 6301/6302 or modem compatible	1,500	15
T16/6511	CRT terminal, character or page mode; local editing, function keys; protected fields; blinking brightness modes; 110-9600 baud, hard-wired or modem attachment (not yet available)	2,400	30
T16/6552	CRT terminal like 6511 but polling protocol for multidrop use (not yet available)	2,700	33
<b>Disc Subsystems</b>			
T16/3101	Disc controller with 2 independent channel connections (for 2 processors); up to 4 separately connected disc drives per controller (not daisy chained)	4,400	21
T16/4101	10M-byte moving head disc; 1 fixed, 1 removable platter, 30-msec seek; 12.5-msec average latency	8,000	63
T16/3102	Disc controller, like 3101, except designed for drives with more than 10M-byte capacity	8,800	43
T16/4102	40M-byte moving head disc; 5-platter pack, 30 msec seek, 8.3-msec average latency	12,000	119
T16/4103	80M-byte moving head disc, 5-platter pack, 30-msec seek, 8.3-msec average latency (not yet available)	15,000	119
<b>Magnetic Tape</b>			
T16/3201	Magnetic tape controller with 2 independent channel connections (for 2 processors) up to 2 separately connected drives per controller (not daisy chained)	3,000	20
T16/5101	Magnetic tape drive, 45 ips, 9-track, 800-bpi NRZI; 300 ips rewind, power fail/auto restart	6,950	46
<b>Card Readers and Line Printers</b>			
T16/3303	Card reader controller with 2 independent channel connections (for 2 processors)	1,800	17
T16/3304	Card reader controller with 2 independent channel connections (for 2 processors); controls up to 2 readers	2,600	17
T16/3305	Card reader/line printer controller with 2 independent channel connections (for 2 processors); controls 1 card reader, 1 line printer	2,600	17
T16/3301	Line printer controller with 2 independent channel connections (for 2 processors)	1,800	17
T16/3302	Line printer controller with 2 independent channel connections (for 2 processors); controls up to 2 line printers	2,600	17
T16/5301	Card reader; 600 cpm, 80-column cards	4,800	40
T16/5501	Line printer, 120- to 300-lpm character-dependent 120 columns, 64-character ASCII set	5,600	48

**TANDEM COMPUTERS INC. — TANDEM 16 NONSTOP™ SYSTEMS, SYSTEM REPORT**

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**PRICE DATA (Contd.)**

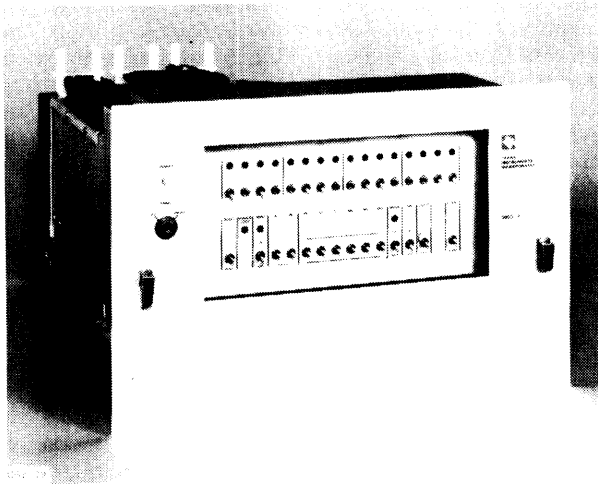
<b>Model No.</b>	<b>Description</b>	<b>Purchase Price (Maint. not Incl) \$</b>	<b>Monthly Maint. \$</b>
T16/5502	Line printer; 300-lpm drawn printer, 132 columns; 64-character ASCII set; 12-channel VFU	11,500	133
T16/5503	Line printer, 600-lpm drawn printer; 132 columns; 64-character ASCII set; 12 channel VFU	14,000	154
T16/5504	Line printer; 900-lpm drawn printer; 132 columns; 64-character ASCII set; 12-channel VFU	21,000	154
T16/5505	Line printer; 1500-lpm; 132 columns; 12-channel VFU; powered stacker; 64-character ASCII set	42,000	165
<b>General-Purpose Controllers</b>			
T16/3401	Universal interface with 2 independent channel connections (for 2 processors); 16-line parallel interface with TTL level line drivers and receivers; for controlling line printers, card readers or similar device	1,800	17
T16/3402	Universal Interface, like T16/3401 but with differential line drivers/receivers	1,800	17
T16/3403	Universal Interface, like 3401 but for 2 devices	2,600	17
T16/3404	Universal Interface, like 3402 but for 2 devices	2,600	17
T16/3405	Universal Interface, for two devices, one using TTL and the other using differential level drivers/receivers	2,600	17

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# TEXAS INSTRUMENTS

## TI 960B System Report



### OVERVIEW

The Texas Instruments 960B minicomputer is a microprogrammed 16-bit "manufacturer's control computer" with MOS semiconductor memory. Hardware features and software support both bit manipulation for communication with control devices and an extremely flexible I/O structure. The system is well suited to data acquisition and process control applications. Texas Instruments offers the 960B to both OEM and end-user markets.

The 960B is the hardware foundation for two important hardware/software packages, the Data Exchange System and the Terminal Polling System. The Data Exchange System (DXS) is a distributed processing system with multiple 960B computers controlling up to 256 interactive terminals. The 960B can be either a stand-alone configuration or a front-end for another manufacturer's host computer. In either case, the central DXS facility allows interactive inquiry/response and data entry to a central DXS data base which can supplement the data base in the host computer in front-end systems. The Terminal Polling System (TPS) is an off-line system for polling up to 200 multidrop terminals connected to up to 8 lines; information is usually transferred from cassettes on the terminals at night and recorded on magnetic tape for use on an off-line host computer the next day.

Because the 960B is a manufacturer's control system and users program in assembly language, the 960B's important characteristics tend to be hardware oriented, such as specifications and system architecture. On the other hand, the capabilities of DXS and TPS systems are to a

large extent determined by the controlling software. The DXS and TPS users tend to program in higher level languages and frequently seek services from TI or software houses for program development.

### The 960B

The 960B uses a high-speed MOS memory (750 nanoseconds) with automatic error checking and correction on a 4K semiconductor random access memory chip; one board can contain 8K, 16K, or 24K words of memory. The main chassis can hold up to 65K words of memory, thus no memory expansion chassis is needed. The 960B replaces the earlier 960A, also a semiconductor-based system but it used a smaller memory chip and requires more memory boards per system. The 960A introduced in November 1971 was predated by the 960, a core-based system no longer in production. Texas Instruments continues to support the 960A but actively markets only the 960B.

A battery pack option for the 960B solves the problem of the volatile nature of semiconductor memory. The battery pack plugs into the processor chassis and can supply standby power to 16K words of semiconductor memory for a minimum of 20 hours. It includes an automatic switchover circuit for power failure and startup and a circuit for fast battery recharge.

The 960B has the following features:

- Sockets for each 4K chip, simplifying plug-in replacement.
- Error detection and correction circuits; light-emitting diodes provide easy identification of failed parts.
- Memory protect.
- 78 basic instructions, the same instruction set as the 960A.
- Up to 8K I/O lines.
- Communication Register Units (CRUs) that allows interfacing devices easily.
- Power fail/auto restart.
- Power supply that accommodates U.S., European, and Japanese ac power requirements.
- Rack-mounted chassis.

### HEADQUARTERS

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An important element in the I/O structure is the Communications Register Unit (CRU) which provides from 32 to 8,192 I/O lines to connect noncomputer and slow-speed peripheral devices to the 960B. The processor can address, sense, and set individual lines or groups of lines.

The 960B rack-mounted processor includes power supply, direct memory access channel, automatic error detection/correction, four CRU ports, and 8K words of memory. Table 1 lists the processor characteristics. Peripherals include standard terminals, magnetic tape, punched card, and paper tape devices, printers, discs, process I/O subsystems, and communications interfaces. A special set of CRU data modules simplifies attaching non-TI equipment.

**Table 1. Texas Instruments TI 960B Processor Characteristics**

<b>CENTRAL PROCESSOR</b>	
Microprogrammed	Yes
Number of internal registers	Two sets of 8 accumulators and index registers
Number of instructions	
Standard	78
Optional	22
Fixed-point arithmetic	
Add/subtract	Standard
Multiply/divide	Optional
Add time ( $\mu$ sec)	3.6
Floating-point arithmetic	Subroutines
Special features	Worker/supervisor operating modes
<b>ADDRESSING</b>	
Direct (number of words)	65,536 for 1-address format
Indirect	Yes, for 1-address format
Indexed	Yes
<b>MAX NUMBER OF I/O DEVICES</b>	256
<b>OTHER FEATURES</b>	Addressing to bit level
<b>PRIORITY INTERRUPT</b>	
System	
Lines	3
Levels	Software
<b>MEMORY</b>	
Type	MOS semiconductor
Word length (bits)	16 data, 6 checking
Cycle time/word ( $\mu$ sec)	750 nsec
Capacity (words)	
Minimum	8,192
Maximum	65,537
Increment size, words	8K, 10K, 24K
Checking	6 bits, auto correct
Protect	Std, not programmable
ROM	Optional
Use	Bootstrap loader, Control ROM
<b>I/O CHANNELS</b>	
Programmed I/O	CRU register
Direct Memory Access (DMA) Channels	1 std; 6 opt
Multiplexed I/O	No
<b>MAXIMUM TRANSFER RATE (WORDS/SEC)</b>	
Within memory	214K without indexing; 170K with indexing
Over DMA	1.3 million

The 960B uses the same software as the 960A; its operating systems are Programming Support Monitor (PSM) and Process Automation Monitor (PAM).

The PSM operating system and PAM — both disc (PAM/D) and nondisc (PAM) versions — provide a multiprogramming environment using executive and worker modes for real-time, on-line processing. Languages are supported Symbolic Assembly Language (SAL) and Process Control Language (PCL/A), which is an extension of basic FORTRAN and uses the Texas Instruments Language Translator (TILT). The 960B FORTRAN language extends basic FORTRAN to support bit processing and real-time operations to make it a Process Control Language (PCL). A general-purpose macro processor translates user-defined languages into the 960B's FORTRAN or ASSEMBLER language for programming special-purpose applications.

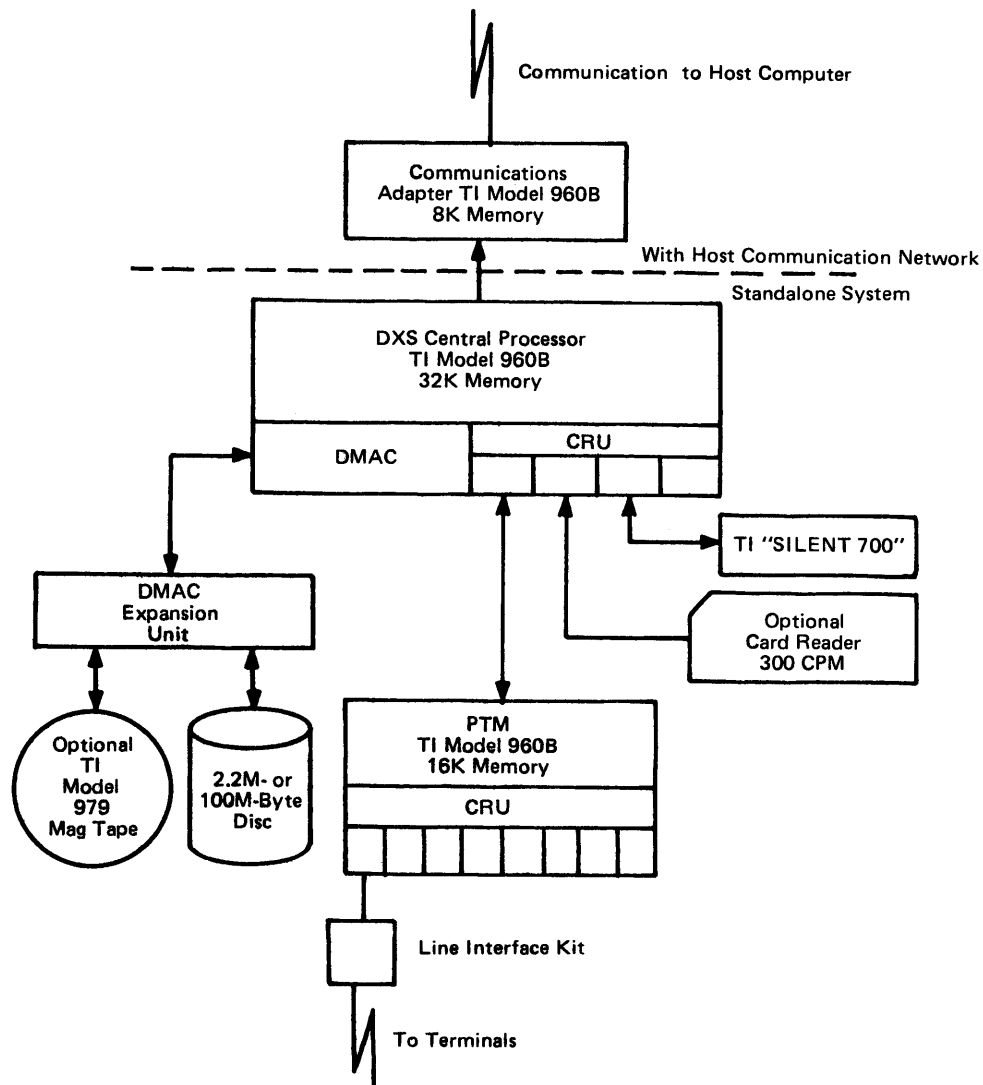
The Data Exchange System is a hardware/software package that places a number of interactive terminals under the control of a DXS facility to manage a central data base. The cost-effective system size can range from a few terminals to a maximum of 256 terminals; all can access the central data base for concurrent interactive inquiry/response and data entry. The DXS central system consists of multiple 960B processors; a "CPU" to process transactions and manage the data base and central I/O, from one to four "Programmable Terminal Multiplexors" to manage up to 64 terminals each, and finally, a 960B-based communications adapter for communications with the host for front-end systems. Figure 1 illustrates a Basic DXS system configuration.

The DXS CPU supports magnetic tape drives, card readers, printers and "Silent 700" terminals in addition to the discs. Model DXS-20 systems use up to four 2.2M-byte cartridges for disc storage. Model DXS-40 systems can also handle up to four 100M byte discs. Memory sizes for DXS processors range from 32K to 64K words.

Each PTM usually has a 16K-word memory and can handle a variety of types of local and remote terminals. These include CRT terminals, Silent 700 data terminals with or without cassette drives, attendance terminals and multicopy page printers (100 characters per second or 500 lines per minute). A Remote Distributive Terminal Controller (RDTC) is used to reduce the number of modems needed at one location by converting asynchronous data to synchronous data.

DXS uses the 960B dual mode architecture, with a double set of registers and program counters, to implement supervisor and worker modes, in a foreground/background environment. Memory management, multitask programming, and telecommunications spooling as well as various types of file management are all standard features.

The Terminal Processing System (TPS) is a low-cost, remote terminal, polling system with up to eight lines with automatic dialing for collecting stored data from a network of remote, low-speed terminals. It is not an interactive system. The central facility usually polls the terminals



**Figure 1. TI 960B: Basic DXS System Configuration**

for data stored on cassettes and logs it onto magnetic tape or disc. Optional features include multidrop line discipline, software development package, and, on disc systems, simultaneous distribution to the terminals and sorting of data from multiple terminals. Table 2 compares DXS and TPS systems.

## PERFORMANCE AND COMPETITIVE POSITION

The 960B minicomputer, the DXS system and the TPS system compete in different market sectors against a different set of competitors, of course, but all three systems have three strong points in common.

The first of these is low cost. Texas Instruments is a major semiconductor maker, and consequently the computer division can obtain its semiconductor chips in-house at a low cost. Even now, when other manufacturers, notably Hewlett Packard, have reliable low-cost semiconductor-based systems, the 960B incorporates a 4K chip with error-correcting logic at a price that makes it highly competitive.

The second selling point is reliability. For many OEM manufacturers, this is the first selling point. Texas Instruments is noted for reliability not only at the component level, with the extensive 6-bit checking logic for each 16-bit word of memory, but also at the system level. In a

**Table 2. Texas Instruments: Differences Among DXS Systems**

MODEL NO.	TPS	DXS-20	DXS-40
<b>MEMORY SIZE, Kbytes</b>			
CPU	48 to 128	64 to 128	64 to 128
PTM	N/A	16	16
Communications Adapter	N/A	8	8
<b>DISCS</b>			
Cartridge, Mbytes	2.2 to 8.8	2.2 to 8.8	2.2 to 8.8
Pack, Mbytes	—	—	100 to 400
<b>TAPES</b>			
800 bpi	1 to 3	1 to 3	1 to 3
1600 bpi	Replacement Option	Replacement Std	Replacement Std
<b>CARD READER</b>	Option	Option	Option
<b>PRINTERS</b>	Option	Option	Option
<b>TOTAL TERMINAL CAPACITY</b>	200	256	256
<b>CPU COMMUNICATIONS</b>			
No. of Lines at 9600 baud	None	1 to 4	1 to 4
1200 baud	1 to 8	Varies	Varies
300 baud	1 to 8	Varies	Varies
<b>PTM COMMUNICATIONS</b>			
No. of lines at 300 or 1200 baud	None	1 to 16	1 to 16
No. of Terminals/Line	None	1 to 16	1 to 16
No. of PTMs/CPU	None	1 to 4	1 to 4
<b>FLEXIBILITY</b>			
Simultaneous Input	Yes	Yes	Yes
Simultaneous Output	Option	Yes	Yes
Sort Received Data	Option	Yes	Yes
Multidrop Line Discipline	Option	Yes	Yes
Interactive	No	Yes	Yes

way, Texas Instruments entered the minicomputer market as an afterthought: first they built the systems for their own use, and then after using them for a while, considered marketing them to the general public. This is true for the DXS systems as well as the 960 and 980 lines. The result is that most Texas Instruments products have been in use for years and have had all the wrinkles ironed out long before they are offered to the public.

The third selling point common to all systems is the increased activity for the whole minicomputer segment of the company, systems development and marketing. The introduction of the DXS and TPS systems heralds this greater activity. All users, including on-going users like OEM manufacturers, benefit from expansion because it means better service, increased software support and greater variety of products as the division grows larger.

For many applications the 960B was the first manufacturer's control computer that was both fast enough and cheap enough to compete with hard-wired systems. While other manufacturers (General Automation, Computer Automation, not to mention the microcomputer manufacturers) now have systems inexpensive enough to compete

with hard-wired logic, the TI 960B hardware and general software are suited for data acquisition, process control, and manufacturing control applications. The Communications Register Unit, the bit manipulation instructions, the 960B FORTRAN and Process Control languages, the Process Automation Monitor, and the TILT macro processor make the TI 960B stiff competition for process and industrial control applications. Competition is strong in this market because almost all minicomputer manufacturers market in this area. However, only systems designed for a specific type of process, manufacturing facility, or data collection application or general systems with software and special-purpose devices for particular applications can match the 960B's price/performance.

The DXS systems face competition from a variety of inquiry/response data base management systems particularly from minicomputer manufacturers. General Automation's DM 100 and 200 Series are oriented toward business and industrial applications. Hewlett Packard offers the M230, M260 and S250 data management systems. Microdata offers the REALIY system via distributors.

### User Reactions

An OEM manufacturer setting up an industrial instrument monitoring data collection system selected the 960A over Interdata and Digital Equipment processors largely because the CRU interfacing allowed the system to handle I/O lines individually instead of in groups of eight. This user felt the system was a "hardware man's computer," in spite of a variety of reliability problems TI had initially with the semiconductor chips. This user noted that TI was stepping up software development and he is impressed with the user's group.

A maker of pneumatic tube systems quoted the reliability of the TI systems as the single most important factor in its control computer selection. A Data General system was exchanged for the TI mini because this manufacturer felt the system reliability would increase with the change. Programming is done in assembly language. This user makes many PC boards and input devices — some boards and an occasional CRT are obtained from T.I. The company is very pleased with the TI 960B and is using several systems in engineering development and manufacturing tests as well as in the company's product as the control component.

Another OEM, a maker of numerical control systems, bought the Texas Instruments minicomputer when it first came out because it was the first one on the market that competed in price and speed with hard-wired controllers. This user particularly liked the architecture of the system, with single bit addressing double precision arithmetic, instruction set, and I/O structure. This customer uses little TI software and few peripherals but does use the 16-bit I/O board, some D/A boards, and a TTY interface in its systems. Even in today's market when more systems com-



pete at TI's price level, this customer would choose the 960B again because of its exceptional I/O flexibility.

An oil company uses 23 960 systems for data acquisition in a unitized oil field. The TI computers were selected over IBM, CDC and Varian systems about 3 years ago largely because of price. The systems collect and monitor flow data from the pumps and compare predicted with actual oil flow. They can turn the oil pumps on and off, although this is usually done manually. Six systems are disc-based, with 32K words of memory, printers, readers, TTYs, and CRTs. Seventeen systems with 4K words of memory are in the field; they use A/D subsystems and communication lines to gather and transmit data. Programming is done largely by a software house; some source code is in FORTRAN. This user stated he had no complaints about the systems: they are reliable and they do the job they were bought for. What else could a user ask for?

### CONFIGURATION GUIDE

The TI 960B is modular and can range from a processor with 8K words of memory, a Teletype ASR/TBE for I/O, and four CRU modules to a system with 65K words of semiconductor memory within the main chassis, line printer, magnetic tape, disc units, and 256 CRU modules. Ten CRU modules are currently available for digital control and data transfers, interfacing with analog devices, data communications equipment, timers, and interrupts.

Optional features include hardware multiply/divide, ROM bootstrap loader; CRU expansion from 4 to 16 ports, battery pack, and auto restart for emergency power; and additional memory.

Up to eight high-speed devices, such as magnetic tape transports or discs drives, can interface to a system via the direct memory access channel. Slow-speed devices interface to a system via CRU ports. Table 3 lists system peripherals.

Table 4 outlines the configuration requirements for the basic general-purpose software packages. In addition, Texas Instruments supplies a special disc-based ATS-960 Automated Test System for operating test instruments on analog, digital, and hybrid instruments at high speeds. The system accommodates up to four test stations, and uses a special ATLAS language designed for testing.

The basic configuration for the DXS systems includes a Central Processor with a 32K-word memory, disc storage, a Silent 700 (733) KSR Console and a Programmable Terminal Multiplexor (PTM). Each PTM includes another 960B Processor with 16K-word memory; it can support up to 16 lines with up to 16 terminals on each line, but the overall system maximum is 64 terminals. Up to four PTMs can attach to a DXS CPU. If the DXS system operates as a front-end processor, a communications adapter using a 960B and 4K words of memory interfaces the DXS system to the host computer. See Figure 1.

**Table 3. Texas Instruments TI 960B Series: Peripherals**

Model No. Terminals	Description
966670	"Silent 700" KSR/ASR Data Terminals, 30 cps
966647	Twin Cassette "Silent 700" ASR Data Terminal, 30 cps, 1200 baud
961755	Teletype ASR33, 10 cps
973305	Keyboard/CRT 24 lines, 80 char, 2400 baud
<b>Paper Tape</b>	
965935	300 cps reader
973523	300 cps reader, 75 cps punch
<b>Punched Card</b>	
966322	300 cpm reader
<b>Printers</b>	
966767	165/330 cps dot matrix printers 64 char set 132 col
917065	356 lpm line printer, 64 char set, 132 col interfaces to DMA channel
<b>Discs</b>	
942541	3330-Type Disc Controller and Primary Disc (50M-word capacity), supports up to 4 drives for 200M-wd capacity
966340	Cartridge Disc Subsystem, 1-4 drives, 1.14M wds/drive
966669	Like 966340 but disc not easily removed
961751	Head-per-track disc, 299K/456K wds/drive
<b>Magnetic Tape</b>	
217536	9-track 800 bpi, 37.5 ips, 1-3 drives/controller
<b>Process I/O</b>	
964562, 964563	Wide-Range A/D Converter Systems, 13-bit, 5 or 10 msec/15 bit, 25 or 33 msec; up to 16 8-channel inputs
965882	High-Level A/D Converter Systems, $\pm 4.096V/\pm 10.24V$
964564	Full Scale analog inputs, up to 16 8-channel inputs
217686	General-Purpose D/A Converter System, 12-bits $\pm 5.12V$ , $\pm 10.24$ and 4-20 ma D/A cards
217690	D/A Converters with 1, 2, or 3 registers, 12-bit number converted to $\pm 5V$ , $\pm 10V$ , or $0-\pm 10V$
<b>CRU Data Modules</b>	
217382, 217380	A/D Converters, 1-6 channels, single-ended analog single converted to 12-bit number
966787	32 lines, all input or all output, respectively
214087	OCI interrupts for 5, 12, or 24 VDC, respectively
214114	Interrupt Module, 8 interrupt flip/flops, 8 mask flip flops
961642	Interval Timers for 1-, 2-, 4-, or 8-msec time intervals
966630	Communications Module for Bell 103A or F, 202C, or D Data Sets; 110, 300, 1200, 2400, 4800 or 9600 baud
214103	Data Module for 16 I/O lines EIA232C compatible
966752	Data Module for 16 Input and 16 Output lines
	Synchronous Communications Module for 201 or 208 data sets

**Table 4. Texas Instruments TI 960B System Software**

Package	Description
<b>DXS</b>	Interactive distributed processing system, up to 256 terminals on-line to disc data base; requires 32K word memory, Programmable Terminal MUX, disc, terminals.
<b>TPS</b>	Terminal Polling System for up to 200 terminals, requires 24K-word memory, terminals, tape or disc.
<b>PSM</b>	Program Support Monitor, single-program executive, requires 8K words of memory.
<b>PAM</b>	Process Automation Monitor, on-line, real-time multiprogramming system requires 12K words of memory.
<b>PAM/D</b>	Disc-based version of PAM, with file handling routines, requires 16K words of memory, disc.
<b>PCL FORTRAN</b>	ANSI X3 10-1966 FORTRAN with extensions and deletions, requires 16K words of memory.
<b>SAL</b>	Symbolic Assembly Language, runs under PSM, PAM, or PAM/D with 6.5K words of memory; cross Assembler version for IBM 360 requires 108K bytes of memory.
<b>TILT</b>	Macro preprocessor for macro definitions
<b>Utilities</b>	Overlay Link Editor, Librarian, Bootstraps Terminal Source Editor, PCL/A Run Time Library, others

DXS systems come in two models. The DXS-20 uses a 2.2M-byte cartridge disc drive, while the DXS-40 can also use 100M-byte 3330-type disc pack drives. Card readers, magnetic tape transports and data terminals can be added to the system.

Basic TPS systems include a CPU with 24K words of memory, a tape drive or 2.2M-byte cartridge disc, a Silent 700 console and a 1200-baud modem. Up to eight communications ports can be supported with up to 64 terminals per port on multidrop lines to an overall system maximum of 200 terminals. Expanded systems can include up to three tape drives and four cartridge discs (8.8M bytes total). Card readers and printers can also be added.

**Compatibility**

The TI 960B is upward program-compatible with the 960A and 960. The 960A and B have some instructions not in the 960's instruction set, thus software developed for the 960A and B may not run on the 960. The 960 line is not program compatible with the TI 980, but they are data compatible and use many of the same peripheral devices. A disc or magnetic tape recorded by one computer, for example, can be read by the other.

**MAINTENANCE**

Texas Instruments provides three types of contract maintenance for purchased systems: basic, standard, and

full coverage. Basic coverage provides for prime shift preventative and emergency maintenance, Monday through Friday, for any 9 consecutive hours between 7 a.m. and 6 p.m. at the user's site. Standard coverage provides preventative and emergency service at the user's site for 16 consecutive hours between 7 a.m. and 1 a.m., Monday through Friday. Full coverage provides for on-site emergency and preventative service around the clock, 7 days a week. In addition to these contracts, Texas Instruments provides service on an on-call basis for users without a contract, or outside of contracted hours, with the fee depending on whether equipment is delivered to a repair depot or is repaired on-site during the prime shift or outside the prime shift, or on Sundays and holidays.

**TYPICAL PRICES**

Model Number	Description	Purchase Price \$	Monthly Maint. \$
<b>CENTRAL PROCESSOR AND WORKING STORAGE</b>			
<b>960B</b>			
949709-0100	960B Central Processor (includes 8K wds of semiconductor memory, memory error detection/correction; memory write protect; power fail warning interrupt; power-up interrupt; removable control panel; keyboard; 3 ports for semiconductor memory modules; 1 port for DMAC interface; 4 ports for CRU cards; 1 port for extended arithmetic opt; space for internal CRU expansion option, power supply, rackmount chassis and slides)	4,350	95
943709-0101	960B CPU with 8K words of memory and battery pack	4,450	95
943709-0102	960B CPU with 8K words of memory, battery pack and internal CRU expansion	4,750	95
<b>Semiconductor Memory Expansion</b>			
975155-0104	8K to 16K memory expansion kit	1,400	6
975155-0106	8K to 24K memory expansion kit	2,800	12
<b>Memory modules</b>			
975155-0002	8K memory add-on module	1,400	6
975155-0004	16K memory add-on module	2,800	12
975155-0006	24K memory add-on module	4,200	18
<b>Processor Options</b>			
943659-0001	Battery Pack		
26855-0001	± 15 V Regulator	200	5
26819-0001	Extended Arithmetic Option (8.3 sec multiply; 10.4 sec divide)	900	10
26882-0001	ROM Bootstrap loader	250	5
<b>MASS STORAGE</b>			
<b>Discs</b>			
955157-0007	DMAC Interface Only kit for moving head disc	3,300	25
955157-0001	Magnetic Disc Master Kit, moving head, removable disc	8,400	80
955157-0002	First and third secondary units w/o disc power supply (additional 1.14 M wds)	4,600	44
955157-0003	Secondary unit with disc power supply	5,100	50
957482-0001	DMA Controller, CPU mounting kit	500	6
966669-0002	Magnetic disc secondary kit; moving head nonremovable (1st and 3rd secondary units w/o disc power supply)	3,850	44
966669-0003	Secondary unit with disc power supply	4,350	50
961751-0004	Fixed-head disc; 229K words, xfer rate 220K wds/sec, av access time 8.7 msec	14,450	100
961751-0008	Same as 961751-0004 except 485K wds	16,500	120
961751-0017	DMAC Interface kit for fixed-head disc	3,100	18
<b>INPUT/OUTPUT</b>			
<b>Punched Card</b>			
966323-0003	Card Reader (300 cpm)	2,700	40
<b>Paper Tape</b>			
965935-0003	High speed sprocket drive reader (to 300 cps)	1,110	17
573523-0003	High speed tape reader/punch combination	3,000	40
<b>Line Printer</b>			
966792-0001	Line printer (132 col, medium duty, 165 cps)	6,250	85
966792-0011	Line printer (330 cps)	6,850	95
217065-0001	Line Printer Kit (80 col, 356 lpm)	13,000	150
<b>Magnetic Tape</b>			
217536-0001	Magnetic Tape Transport, Master Kit (9-track, 800-bpi, 37-1/2 ips)	7,950	80
<b>Teleprinters</b>			
966670-0003	"Silent 700" KSR Data Terminal (30 cps)	1,500	20
966647-0003	Twin Cassette "Silent 700" ASR Data Terminal	3,100	35



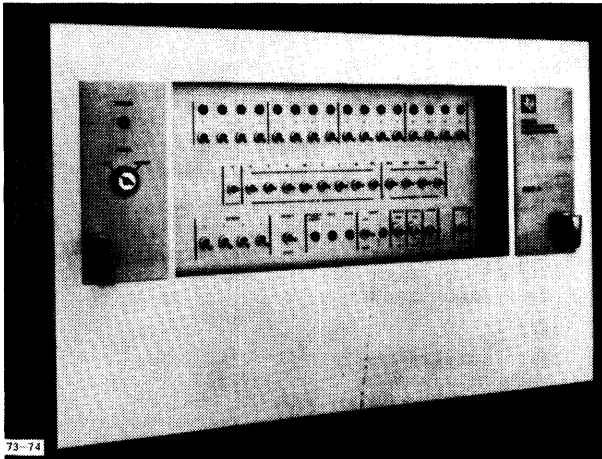
## TYPICAL PRICES (Contd.)

Model Number	Description	Purchase Price \$	Monthly Maint. \$
961755-0001	Teleprinter (10 cps, friction feed paper tape reader/punch, interface kit and stand)	1,950	54
973305-0013	Video Display (912 CRT, detachable keyboard, 1,920 char/screen)	2,100	30
966556-0002	CRU Expansion Chassis (includes + or -15V at 4 amp power supplies for operation of video terminal, EIA, A/D, and D/A converter modules + all other CRU modules)	1,500	15
914103/0001/2/3 and 217380-0001	Interface Modules Data Modules	250	5
973315-0004/3	Termination panels		
973415-0004			
214111-0001	Data Module Contactor	350	5
973316-0001	Contactor termination panel kit	160	1
214087-0001	Interrupt module	200	5
973316-0002	Interrupt module termination panel kit	200	1
966787-0001/2/3	16-Input OIC Interrupt Module	650	6
973316-0003	Termination panel kit for 16-Input OIC Interrupt module	200	1
966630-0001	Data Module 16 IO EIA	350	6
9661642/0005/1/3/4/7/10/11	Full Duplex EIA Communications interface modules from 110-9,600 baud	350	5
966495-0001	Data Module, 32 Input OIC	550	5
966752-0001	Synchronous Communications Module	700	6
966676-0001/2	4 TT Input or Output accessory kits (16 input)	475	20
966676-0003/4/5	Same as above but 32 input, 32 output or 16 input/16 output	650	25



# TEXAS INSTRUMENTS

## TI 980B System Report



### OVERVIEW

The TI 980B is a 16-bit general-purpose minicomputer designed for flexibility and problem-solving power in both batch and multiprogramming environments. It features a low-cost, high-speed semiconductor MOS memory utilizing 4K chips with error correction facilities. Texas Instruments continues to announce drops in memory prices that increase the competitiveness of the system.

The 980B 4K semiconductor random access memory chip allows 8K, 16K or 24K words of memory to fit on one board. The main chassis can hold up to 65K words of memory. The 980B also features:

- Fault isolation indicator lights, providing easy identification of failed parts.
- Built-in single-bit error correction and multi-bit error detection.
- Power supply to accommodate U.S., European, and Japanese AC power requirements.
- 98 basic instructions (16, 32, or 48 bits).
- Bit/word/byte-string data addressing.
- Four hardware priority interrupt levels (optional interrupt expansion).
- Power failure interrupt/auto restart.
- I/O-oriented executive type monitor.
- Plug-in battery pack and auto restart upon power restoration (optional).
- Programmable memory protect.

The 980B is marketed to both end-users and OEM customers. The system developed slowly at first, but the introduction of the DX 980 General Purpose operating system in 1974 and more energetic marketing efforts give it a more important position in the market. Texas

Instruments appears to be working harder than previously to sell its minicomputer products. The 960B, a sister system intended as a manufacturer's control computer, is also being marketed more vigorously and receiving more notice. The 960B is similar to the 980B in many respects, but has hardware features and software to support bit manipulation for communication and control devices, data acquisition, and process control. Two interesting hardware/software packages using 960B components are recent important developments in the Texas Instruments product line. One is a Terminal Polling System (TPS) and the other is a distributed processing system called the Data Exchange Systems (DXS).

The DX 980 General Purpose Operating System forms the central body of software for the 980B; it is a foreground/background multiprogramming system allowing real-time and time-sharing multitasking in the foreground and batch processing in the background. DX 980 foreground programs can be scheduled according to external priority interrupts, time intervals or time-of-day. In addition, an Interactive Terminal Subsystem with RJE and Interactive File Editing and Status Inquiry Modules make the system particularly well-suited to data base inquiry/response and data entry from both local and remote terminals. Background program development facilities include a FORTRAN IV compiler, SAPG assembler and DXOLE, an overlay link editor.

Texas Instruments also offer a Basic System Monitor (IOP) as a minimal operating system, a BASIC/980 Interpreter, and the Texas Instruments Language Translator (TILT).

The TI 980B includes many standard features characteristic of more expensive systems. In addition to the hardware multiply/divide, memory protect/privileged instruction set, and auxiliary processing features already mentioned, a basic system includes a ROM bootstrap loader, power fail detection, auto restart, one DMA channel and four I/O channels (expandable to eight and 256, respectively) and four levels of priority interrupt expandable to 256 levels. Real-time clock option is also available.

### HEADQUARTERS

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TI offers a battery pack option to solve the problem of the volatile nature of semiconductor memory. The battery pack plugs into the processor chassis and can supply standby power to 16K words of semiconductor memory for a minimum of 20 hours. It includes an automatic switchover circuit for power failures and startups and a circuit for fast battery recharge.

Peripherals for the 980B include discs, magnetic tape drives, printers, card and punched tape I/O, process I/O subsystems, and communications devices.

Although the 980B is more powerful than the 960B, the two systems have many characteristics in common, as well as a number of important differences. Both use the same MOS memory modules, power supplies, and peripherals. The 980B interfaces to peripherals via a conventional programmed I/O (PIO) or DMA channel. The 960B, however, has a special process automation interface instead of a PIO bus; this interface, called a Communications Register Unit (CRU), connects special-purpose peripherals and data communications controllers to the 960B.

Texas Instruments has designed special-purpose modules to interface to the CRU; these modules cannot be used with the 980B. Multiply/divide is standard on the 980B and optional on the 960B. Memory protect is programmable on the 980B and jumper selectable on the 960B. In addition, the memory protect feature is more sophisticated on the 980B than on the 960B. It includes a base register for program relocation and an upper limit register so that user programs can be relocated and confined to a specific memory segment. Table 1 lists the specifications for the 980B.

## PERFORMANCE AND COMPETITIVE POSITION

The TI 980B is comparable in performance to other general-purpose 16-bit minicomputers like the HP 21MX, Data General Nova 800, Interdata Model 7/16, Digital PDP-11/40, General Automation SPC-16, Computer Automation Alpha LSI and Prime 200. The TI 980B does not have memory mapping or other facilities for extending systems into the small and medium computer range. Also it has not been extended downward into the "microcomputer" range. However, the step-up in marketing efforts and the introduction of both the DX 980 Multiprogramming Operating System and the BASIC/980 package put the system in a competitive stance in the traditional minicomputer markets. The 980B is now a more important contender than it was a year ago.

Part of the secret of the success of this system is its cost. Texas Instruments is a major semiconductor manufacturer, which partially explains the low price of the large MOS semiconductor memories available for the 980B. Reduction in memory prices continues the trend toward lower prices.

**Table 1. Texas Instruments TI 980B: Mainframe Characteristics.**

<b>CENTRAL PROCESSOR</b>	
Microprogrammed	No
No. of Internal Registers	9
Addressing	15 modes
Direct (no. of words)	65K
Indirect	Yes
Indexed	Yes
Instruction Set	
Number (std, opt)	98, 106
Decimal Arithmetic	No
Floating-Point Arithmetic	Subroutine
Priority Interrupt Levels	4-256
<b>MAIN STORAGE</b>	
Type	MOS semiconductor
Cycle Time (nsec)	750
Basic Addressable Unit	Word
Bytes/Access	2
Min Capacity (wds)	8,192
Max Capacity (wds)	65,537
Increment Size (wds)	8K, 16K, 24K
Checking	6-bits/wd, auto correct
Protect	Yes
ROM	
Use	Bootstrap loaders
Capacity (bytes)	512 (256 words) each
<b>I/O CHANNELS</b>	
Programmed I/O	4-256 slots
DMA Channels (no.)	1-8 slots
Multiplexed I/O	No
Max Transfer Rate Over DMA (wds/sec)	1M (device limited)

A second element in the system's success is its reliability. Elaborate checking facilities make their semiconductor memories core-like in reliability, matched only by Hewlett-Packard's semiconductor memories. Third, the firm is a large user of its own minicomputer systems for control and general processing applications; thus its systems are designed to meet the requirements of this segment of the minicomputer market. Systems offered to the public have usually been in use within the TI organization for a number of years.

The type of software support and its low cost make the 980B extremely competitive for the OEM market as well as to end-users.

## USER REACTIONS

One large OEM user of the 980A incorporated the TI processor into two different types of systems. In one system, the 980A is the central controller driving 40 remote POS terminals. In the second, it is being developed as a front end to a Honeywell CPU for a service bureau. The TI 980A processor was chosen for the POS system over Digital Equipment and Data General systems because it is faster, uses a larger instruction repertoire, and is considerably less expensive. Another attractive feature was the built-in hardware arithmetic. The 980A was chosen over the 960A because the 980A FORTRAN was

better, because the 980 has arithmetic capabilities and a larger instruction set. The 980A was chosen for the communications processor because the OEM user was already familiar with it and had found it to be reliable.

Two users interviewed chose their systems because of a previous satisfactory experience with a 980A system, which has the same system architecture but with core instead of semiconductor memory. Both users chose the 980A after careful consideration of a number of competitors. Both narrowed the field down to either a TI 980A or a Data General Nova before making the final decision — largely on the basis of cost.

One user has a disc-based 980B with 65K words of memory for processing rocket test data. The 980B collects analog data and calculates flight histories. Input devices include a card reader, a 64-channel, low-level, analog input system, and a 128-channel, high-level, analog input system. Output devices include a line printer, CRT, and plotter. Mass storage devices include three Diablo discs and a tape drive. This system was chosen because the man setting it up was familiar with it from a previous application (when it was chosen over a Nova), and the rocket test system had to be set up and running in a period of 2.5 months. The user met all deadlines for hardware and software installation within that time frame and got the system up and running with little trouble. This user likes the DX 980 operating system very much but feels it would be better if it used a little less memory — he anticipates a later version will lower requirements.

The second user chose TI 980s over Novas in a competitive bid that also included bids from six other minicomputer manufacturers. The 980s are used to interconnect various computers with a Data Link Air Defense network being set up for a foreign government. Forty-three 980s are in various stages of development: some are being installed, some are being altered after having run for a while, and some are up and running in their final form. Memory sizes range from 24K words to 64K words. Most have discs, tapes, printers and CRTs; some have radar consoles and extractors. Most of the applications require real-time processing, and many of the systems are used for line concentration. Up and running systems operate around the clock, 24 hours a day and 7 days a week, and this user has been very happy with the reliability and performance of the system under these strenuous circumstances. The systems are programmed in machine language from scratch, so the user had no opinion on the DX 980 operating system. The only criticism offered was that system development would have been easier if the system had multiple ports to memory instead of the CPU and I/O sharing a single port.

Another user chose the TI 980 for a clinical application over Digital Equipment, Data General, and General Automation systems because of both cost and speed. The computer is being used for a Tomograph Analysis system that operates on X-ray cross sections of tissues. In addition to special inputs from the X-ray apparatus, the system has a magnetic tape drive, Silent 700 terminal, and

Ramtek graphics display. Programming was done in machine language. The user was particularly satisfied with the reliability of the system.

## CONFIGURATION GUIDE

The TI 980B basic rack-mounted processor includes CPU, 8,192 words (16,384 bytes) of MOS memory, two slots for memory expansion, one auxiliary processor slot, one DMAC interface slot, five bus interface slots with one I/O extender implemented, four interrupt levels, ROM bootstrap, power supply and line filters. The CPU includes hardware multiply/divide, automatic error detection and correction, programmable memory protect and privileged instructions, and power fail/auto restart. The removable control panel includes a key lock, hardware breakpoint, and program sense switches.

A second version of the basic CPU includes a factory-installed battery pack to utilize the power up interrupt feature. A battery pack can also be installed in the field.

Memory modules are available in 8K-, 16K- and 24K-word sizes. Larger modules can be substituted for the basic memory board, and two more boards can be added to increase memory size within the main chassis. An upper limit of 65,536 words of memory is imposed by the addressing scheme.

One of the five basic I/O slots in the basic chassis is used to interface an I/O expansion card, as a standard feature. The expansion card provides the logic for adding nine more slots within the chassis or a 10-slot external expansion chassis. Expansion cards can be attached to expansion cards. The interrupt and addressing structure can support four groups of up to 64 addresses each. Thus, up to 256 I/O devices can be connected to a system in addition to the eight devices that can attach to DMA. TI tested a maximum system, with 256 I/O devices and 8 DMAC devices, and it ran quite satisfactorily. In addition, level 2 of the four basic interrupt levels can be expanded to 32 vectored interrupt levels total, using 8-level interrupt expansion modules that attach only to the four basic I/O slots. These can be used for nonstandard I/O devices.

In general, peripherals are preassigned priority interrupt levels. The manufacturer must be consulted for custom configurations. Standard slow-speed, analog/digital, communications and special peripherals connect through the I/O subsystem.

Up to eight controllers for high-speed devices, such as magnetic tape transports or disc drives, can interface to a system via DMA. An expansion kit and external chassis is required to expand the original single channel into a subsystem capable of handling multiple controllers. One high-speed device controller connects to each DMA channel: although Texas Instruments usually provides a standard prewired mother board for the magnetic tape, line printer, fixed-head disc and moving-head disc, any combination of up to eight different controllers can be connected to a system with multiple DMA channels.

Table 2 lists the available peripheral devices and sub-systems. Table 3 defines the configurations required for the basic software packages.

**Table 2. Texas Instruments TI 980B: Peripherals**

Model No. Terminals	Description
973346	Silent 700 KSR/ASR Data Terminals, 30 cps
973306	Teletype ASR 33, 10 cps
966645	Model 912 CRT 24 lines, 80 char, 2,400 baud
	Twin Cassette Silent 700 ASR Data Terminal, 30 cps, 1200 baud, full duplex
<b>Paper Tape</b>	
965946	Reader, 300 cps
973526	Reader, 300 cps, punch, 75 cps
<b>Punched Card</b>	
966323	Reader, 300 cpm
<b>Printers</b>	
966792	Dot Matrix printers 64-char set, 132 cols, 165/330 cps
217065	Line Printer, 356 lpm, 64-char set, 132 cols; interfaces to DMA channel
<b>Discs</b>	
942541	3330-Type Disc Subsystem, 1-4 drives 50M wds/drive
955157 or 966669	Cartridge Disc Subsystem, 1-4 drives, 1.14M or 2.28 wds/drive
961751	Head-per-track disc, 229K/456K wds/drive
<b>Magnetic Tape Communications</b>	
966538	9-track 800 bpi, 37.5 ips, 1-3 drives/controller
966637	Synchronous Communications Module for Bell 201 or 208 Data Sets
965955	Communications Module for Bell 103A or F, 202C, or D Data Sets
973300	Data Module for 16 I/O lines, TTL compatible; 510 ohm and 100 ohm
966580	Vectored interrupt Module, 8 levels, preassigned priority
	Interval Timer Module, 12-bit counter, 10 usec, 100 usec, 1 msec, or 10 msec
<b>Process I/O</b>	
964566, 964563	Wide-Range A/D Converter and Systems, 13-bit 5 or 10 msec per conversion and 15-bit, 25 or 33 msec per conversion; up to 16, 8-channel inputs
965866, 965884	High-Level A/D Converter Systems, $\pm 4.096V \pm 10.24V$ full scale analog inputs, up to 16 8-channel inputs; 50 $\mu$ sec per conversion; up to 10,000 conversion/sec.
964567, 964565	General-Purpose D/A Converter system, 12 bits $\pm 5.12V$ , $\pm 10.24$ and 4-20 ma D/A cards

**COMPATIBILITY**

The 980A and 980B are completely compatible with one another, given comparable configurations. TI 980B is

**Table 3. Texas Instruments TI 980B: System Software**

Package	Description
<b>Basic System Monitor (IOP)</b>	Single program monitor for minimum system with 8K-word memory, console terminal; paper tape I/O, card, I/O disc option
<b>DX980 Operating System</b>	Multiprogramming, real-time operating system; requires 48K-word memory, interval timer, operator's console, disc, and input device (magnetic tape or second disc)
<b>FORTTRAN IV</b>	ANSI FORTRAN IV x 3.9-1966 standards with extensions, requires 24K-word memory under IOP or DX980
<b>BASIC/980 Interpreter</b>	Dartmouth BASIC with extensions for up to 8 terminals; requires 16K-word memory and terminals
<b>SAPG Assembler</b>	Two-pass absolute or relocatable assembler; requires 16K-word memory
<b>TILT</b>	Macro processor designed as prepass to assembler or compiler for language extension via macro definitions or added functions
<b>Utilities</b>	Link Editor, Terminal Source Editor, Disc Build Routines, Non-Disc SYSGEN, Expanded Debug, Math Library, code conversion routines

not program compatible with the TI 960 A/B but all are data compatible and use many of the same peripheral devices. A disc or magnetic tape recorded by one computer, for example, can be read by the others.

Memory modules and power supplies for the 960A and 980A are interchangeable, and similarly memory supplied for the 960B and 980B are interchangeable. A cross assembler is available for assembling 980A or B programs on an IBM System/360 operating under either OS or DOS.

**MAINTENANCE**

Texas Instruments provides three types of contract maintenance for purchased systems: basic, standard, and full coverage. Basic coverage provides for prime shift preventive and emergency maintenance, Monday through Friday, for any 9 consecutive hours between 7 a.m. and 6 p.m. at the user's site. Standard coverage provides preventive and emergency service at the user's site for 16 consecutive hours between 7 a.m. and 1 a.m., Monday through Friday. Full coverage provides for on-site emergency and preventive service around the clock, 7 days a week. In addition to these contracts, Texas Instruments provides service on an on-call basis for users without a contract, or outside of contracted hours. The fee depends on whether equipment is delivered to a repair depot or is repaired on-site during the prime shift or outside the prime shift, or on Sundays and holidays.





## TYPICAL PRICES

Model Number	Description	Purchase Price \$	Monthly Maint. \$
	980B		
943866-0100	980B Central Processor (includes 8K words of semiconductor memory, 3 memory ports, hardware multiply/divide, memory error detection and correction, programmable memory protect and privileged instructions, power fail warning interrupt, auto restart, ROM bootstrap loader, removable control panel with key lock, hardware breakpoint, program sense switches, 1 aux processor port, DMAC interface port, 4 I/O bus interface ports, 4 level priority interrupt expandable to 32, power supply and rack mountable chassis)	4,975	95
943866-0101	980B CPU with 8K words of memory and battery pack	5,075	95
	Semiconductor Memory Expansion		
975155-0104	8K to 16K memory expansion kit	1,400	6
975155-0106	8K to 24K memory expansion kit	2,800	12
943740-0002	Memory expansion interconnect	100	—
	Memory Modules		
975155-0002	8K memory add-on module	1,400	6
975155-0004	16K memory add-on module	2,800	12
975155-0006	24K memory add-on module	4,200	18
	Processor Options		
943659-0001	Battery Pack	100	NC
226855-0001	± 15 V Regulator	200	5
	MASS STORAGE		
	Disc		
942541-001	3300-type disc controller and primary disc (up to 4 drives, 50M wds, 403K wds/sec xfer rate)	33,600	368
973671-0001	ROM bootstrap loader for 3330-type controller	250	5
942541-0004/5/6	Add-on disc drives	20,000	138
942508-0001	Disc Pack	1,000	—
955157-0001	Moving head disc with one removable cartridge (1.14M wds, 1.56 M bits/sec Xfer rate)	8,400	80
955157-0007	DMAC Interface Only kit for moving head disc	3,300	25
955157-0002	First and third secondary units w/o disc power supply (additional 1.14 M wds)	4,600	44
955157-0003	Secondary unit with disc power supply	5,100	50
966669-0002	Magnetic disc secondary kit; moving head non-removable (1st and 3rd secondary units w/o disc power supply)	3,850	44
966669-0003	Secondary unit with disc power supply	4,350	50
961687-0001	Disc cartridge	150	—
961751-0004	Fixed head disc; 229K words, xfer rate 220K wds/sec, av access time 8.7 msec	14,450	100
961751-0008	Same as 961751-0004 except 485K wds	16,500	120
961751-0017	DMAC Interface kit for fixed-head disc	3,100	18
	Input/Output		
966322-0003	Card Reader (300 cpm)	2,700	40
965946-0003	High speed sprocket drive reader (up to 300 cps)	1,110	17
973526-0003	High speed tape reader/punch combination	3,000	40
966767-0001	Line printer (132-col, medium duty, 165 cps)	6,250	85
966767-0011	Line printer (330 cps)	6,850	95
217065-0001	Line Printer Kit (80 col, 356 lpm)	13,000	150
217065-0002	Line Printer Interface Kit (80 col, 356 lpm)	700	12
	MAGNETIC TAPE		
217536-0001	Magnetic Tape Transport, Master Kit (9-track, 800-bpi, 37-1/2 ips)	7,950	80
217538-0001	Same as 217536-0001 (except without controller and terminator)	6,000	55
966671-0003	"Silent 700" KSR Data Terminal	1,500	20
966645-0003	Twin Cassette "Silent 700" ASR Data Terminal	3,100	35
973346-0001	Teleprinter (10 cps, friction feed paper tape reader/punch, interface kit and stand)	1,950	54
	A/N Display terminals		
973306-0012	Video Display (912 CRT, detachable keyboard, 1920 char/screen)	2,100	30
973305-0013	Video Display (912 CRT, detachable keyboard, 1920 char/screen)	2,100	30
	I/O Bus Options		
960703-0001	980 Internal I/O bus expansion	450	6
966796-0001	Expansion kit (7.5 amps at 5VDC and .75 amp at ± 15 VDC)	1,200	15
966796-0002	14.5A, 5VDC	1,200	10
960757-0001	980 I/O Expansion Card	200	5
965955-0001/2	16 I/O Data module	350	5
966637-0001	980 Communications Module	450	6
973300-0001	Vectored Interrupt module	550	5
966580-0001	Interval timer module	300	5
966538-0001	Synchronous Communications Module	700	6

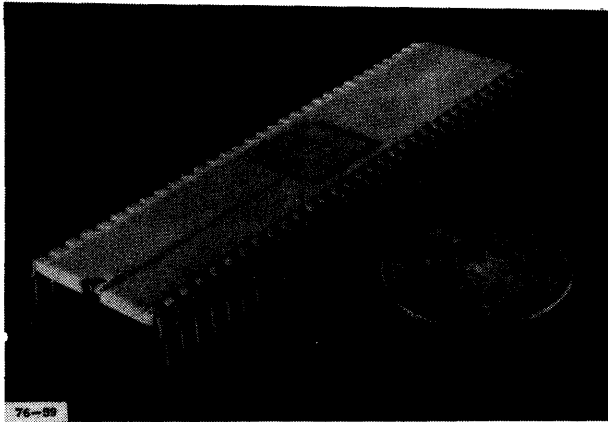
Note:

Maintenance prices are for basic on-call service during 5-day week, 9-hour day.



# TEXAS INSTRUMENTS

## 990/9900 Family System Report



### OVERVIEW

The Texas Instruments 990/9900 family is a new 16-bit line extending upwards from the 16-bit TM 9900 n-MOS microprocessor chip, to the 990/4 computer-on-a-board, up to the 990/10 systems that can map as many as two million bytes of memory. Initially, the system is aimed chiefly at the OEM market, that is, at the low end of the market; but it is by no means restricted to OEMs. This is the line Texas Instruments plans to use as the base of a concerted attack on the whole range of the micro/minicomputer markets, an attack surprisingly long overdue from one of the leaders of the semiconductor industry. Its announcement is spectacular for two reasons: The TMS 9900 is the first 16-bit, single-chip microprocessor from a major semiconductor company; and the 990 line marks Texas Instrument's first really aggressive step toward becoming a major contender in the minicomputer industry.

Although the 990 line is brand new, its architecture is not. Besides the 980 and 960 lines introduced to the public at large and developed slowly in the early 1970s, Texas Instruments had developed a precursor to the 990 for a special, large contract with Ramada Inns. The system design was oriented toward communications and distributed processing, and for that contract, it was implemented in TTL logic using medium- and large-scale integrated circuitry. The result was admirable but expensive by today's standards. When Texas Instruments began designing the microprocessor chip that was to be the basis of the new line, the 990 architecture appeared best suited to the way the market was heading. Thus, although the 990 seems to be totally new and incompatible with Texas Instruments' previous offerings, its design has actually been field tested over a respectable period of time in a TTL version.

The TMS 9900 microprocessor is the foundation of the line. It is implemented on a single 16-bit MOS chip using n-channel silicon-gate technology and a 3-megahertz clock frequency. It is not a microprogrammed chip, but it includes all of the logic for its versatile 69-instruction repertoire on its own real estate. To add flexibility, an extended-operation instruction allows 16 more instructions to be defined in external hardware or software. Also included on the chip are a vectored interrupt facility; separate data and address buses; a Communications Register Unit (CRU) I/O interface; a Direct Memory Access (DMA) interface; hardware context switching; hardware multiply/divide; bit, byte, and word addressing; and 5-mode addressing capable of handling up to 64K bytes, all in a 64-pin DIP package.

The 990/4 microcomputer puts together on a single board the TMS 9900 microprocessor, the CRU and DMA buses, up to eight priority interrupts, powerfail/auto restart logic, a CRU interface for operator or programmer panel, and up to 4K words (8K bytes) of memory. Memory can be RAM, ROM, PROM, or EROM (erasable ROM) modules of various sizes, depending on the type. The 990/4 can also be packaged in a 6-slot tabletop chassis with front panel. Either way, the system can control up to 28K words (56K bytes) of memory. A 733 ASR Data Terminal is supplied with software support, in system packages. Texas Instruments does not implement DMA, however; all mass storage devices interface to the 990/10 TILINE.

The 990/10 is a 3-board TTL version of the TMS 9900 (two boards for CPU, one or more for memory), with mapping of up to two million bytes of memory and a special asynchronous high-speed channel, the TILINE. The 990/10 is a full-blown, high-speed minicomputer system, with supporting disc-based operating systems, high-level languages, and so on. Although current peripherals are relatively low-speed and the discs are in the low storage capacity range, the high memory capacity, high-speed universal bus and rapid context switching are capabilities that will surely be needed for future devices.

Peripherals for the 990 series support the initial marketing thrust toward the low end of the market. An important

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# TEXAS INSTRUMENTS — 990/9900 FAMILY SYSTEM REPORT

peripheral is Texas Instrument's own "Silent 700" KSR and ASR terminals, using cassettes instead of paper tape. Floppy disc, 400 card-per-minute card readers; 88 and 120-character-per-second impact printers; and (with a subsystem) 1.5-million-byte cartridge discs provide standard I/O. Asynchronous and synchronous 1-line interfaces allow transmissions up to 9,600 baud. Two important special peripheral interfaces allow PROM/EROM writing and attachment of custom 16-bit I/O lines. The 16-bit interface allows handling each line separately; one line can be marked an interrupt line.

For a totally new system, the software is extensive. The DX-10 operating system is a multitasking, mapped, disc-based system that supports FORTRAN IV, COBOL, and multiuser Dartmouth BASIC. The cassette-based Terminal Executive TX-990 Operating System is a multitasking system for 990 configurations with up to 32K words of memory. Various smaller support packages are available, including a 990 Prototyping System for encoding PROM/EROM TMS 9900 programs as 990/4 and TMS 9900 software development. A cross assembler allows development of 990 programs on an IBM 360/370 or time-sharing network.

One of the strong points of the entire line is its low cost, which is expected from a major semiconductor manufacturer coming out with a microprocessor and semiconductor memory modules made in-house. TMS 9900 microprocessors with 256 words (512 bytes) of memory are sold in quantities of 50 for \$368 each. The 990/4 board-level system costs only \$575 with 512 bytes of memory and \$800 with 8K bytes of memory. Adding a 6-slot chassis, power supply, and programmer's console raises the price to \$1,900. A 990/10 system with 16K bytes of memory, 13-slot chassis, power supply, and programmer's panel costs \$1,975; raising the memory size to 40K bytes increases the price to \$3,075. Add-on 40K-byte memory boards cost \$2,500 each.

The 990/10 was delivered in March and the 990/4 in April 1976.

Table 1 lists system specifications.

## PERFORMANCE AND COMPETITIVE POSITION

By all accounts, Texas Instruments ought to make rapid inroads into the microprocessor/minicomputer markets, if it makes a reasonably serious attempt to penetrate them. It is a large company with a fine reputation in the semiconductor industry, which supplies computer manufacturers with many of their parts. Yet the firm's initial attempts at market penetration, in the form of the 960 and 980 lines were less successful than many anticipated, in spite of excellent system engineering. This is usually attributed to apathetic marketing and support efforts and partly to the specialized orientation of those computers toward machine and process control applications.

**Table 1. TI 990; Mainframe Specifications**

<b>CENTRAL PROCESSOR</b>	
Microprogrammed	No (extended operation instruction instead)
Stack Processing/Context Switching	Yes ("workspace registers")
No. of Programmable Registers	16
No. of Instructions	
Std	69
Opt	72
Instruction Execution Times ( $\mu$ sec)	
Fixed-Point Add/Subtract	4.662 (990/4); 1.166 (990/10)
Multiply	17.316 (990/4); 11.9-16.2 (990/10)
Divide	5.328 (990/4); 5.4-8.7 (990/10)
Move	4.66 (990/4); 3.60 (990/10)
Floating Add/Subtract	Subroutine
Addressing	
Direct (no. of wds)	32K
Indirect	Yes, 1 level
Indexed	Yes
Mapped	Yes
Priority Interrupt Levels	16
<b>MEMORY</b>	
Cache	No
Types	MOS RAM; ROM; PROM; EROM
Word Length (bits)	16
Cycle Time/Word ( $\mu$ sec)	667 (MOS RAM, PROM)
Capacity, words	
Min	8K (990/10); 256 (990/4)
Increments	4K, 8K, 16K, 24K, 32K MOS RAM; 1K EROM; 256 PROM
Max, without Mapping	32K (64K bytes)
Max, with Mapping	1M (2M bytes)
Checking Protection	Parity, error correcting options
Option	Option
<b>INPUT/OUTPUT</b>	
Max No. of Devices	4,096 CRU; 512 TILINE
Programmed I/O Channel	CRU
Multiplexed I/O Channel	TILINE universal bus on 990/10
Direct Memory Access (no. of channels)	Not supported, but available on 990/4
Max Transfer Rate (words/sec)	
Within Memory	—
Over DMA	3M

The 990 series differs from its predecessors in range of system sizes, which covers the gamut of the existing market. Also, the architectural orientation is towards communications and distributed processing. This line of systems could move Texas Instruments (TI) from a relatively minor position to one of importance. Whether the system lives up to expectations will depend on its software development, and on the energy and imagination of TI's marketing efforts. The company's marketing track record has not been very good, so that area could be a potential weakness. Of course, it is possible that TI intentionally delayed a vigorous entry into the market while the major line was under development.

In any event, TI faces stiff competition at all levels. Its major competitors in the OEM marketplace, fall into two categories. Digital Equipment, General Automation, and Computer Automation compete for the 990/4 board-level systems markets (see Table 2). Digital, Data General,

General Automation and to some extent the Hewlett-Packard 21MX compete at the 990/10 level (see Table 3). As shown in the tables, the TI systems undercut the prices of all the other systems without exception by 15 to 50 percent at the 990/4 level and to a greater extent at the 990/10 level. The DMA rate is potentially the highest available, but that is offset by the facts that more software exists for the competing systems and there are often more built-in features, especially on the larger systems. Nevertheless, the cost difference is clearly significant and is a powerful factor in TI's favor.

At the beginning of 1976, orders were already backlogged for deliveries into May. The significant price break at a time when the OEM market is on the upswing out of a recession may be a tide that will rapidly carry TI to a position of prominence.

## CONFIGURATION GUIDE

The initial marketing thrust of the 990 line is toward the OEM market, and the system configurations emphasize modularity. All three models can be sold with or without chassis, power supply, and programmer's panel. All three have submodels coupling them with various sizes and types of memory. The basic 990/4, for instance, can be configured with 256 words of static RAM, 4K words of dynamic RAM with or without parity, or a self-testing feature. ROM loaders, PROM kits, and EPROMs, as well as 4K-, 8K-, 12K-, 16K-, or 20K-word single-board MOS memory modules, can be added to basic systems. Core memory is unavailable. The system can be housed in a 6-slot tabletop chassis or a 13-slot tabletop or rack-mounted chassis.

Basic 990/10 systems use the same options and memory expansion modules as the 990/4; but all are based on a 2-board TTL CPU with 8K-, 12K-, 16K-, or 20K-word

memories in the basic systems. It is usually housed in a 13-slot chassis with attendant power and programmer's panel. A second series of basic systems is configured with memory mapping. The 990/10 is also available with a group of memory modules that have error-correcting circuitry (ECC). A special (standard) universal bus extension called the TILINE bus interface provides for adding extra memory and high-speed peripheral DMA devices. TILINE mapping provides one million addresses, and is a basis for the extra memory capabilities of the 990/10.

The 990/4 and 990/10 are available in several system packages. The 990/4 Prototyping System packages for development of application programs for the TMS 9900 and 990/4 board-level systems consist of CPU, chassis, power supply, programmer panel, self-testing, memory expansion with parity and write protect, 8K to 24K words of memory, and optionally a 733 ASR terminal, a ROM loader, and a PROM programming module. The 990/4 Program Development Systems are essentially the same except that the 733 terminal and ROM loader are standard items, but the PROM programming module is not supported.

The 990/10 Program Development System is designed to support the DX-10 Operating System. It includes the DS31 disc with its associated ROM loader and the 913A CRT as well as the 990/10 CPU and a 13-slot chassis. Although all peripherals can be attached to either the 990/4 or the 990/10 systems, only the 733 terminals, the PROM kits, and the communications interfaces are software-supported on the 990/4. The CRU can interface to 4,096 devices. The TMS 9900 DMA facility consists of a single line, but the 990/10 asynchronous TILINE bus can support up to 512 high-speed controllers and 1,024K words of memory. Peripheral devices are listed in Table 4.

**Table 2. TI 990/4: Specifications Compared with Those of Competitors**

	TI 990/4	Computer Automation LSI-3/05	GA-16/110	GA-16/220	Digital LSI-11
Word Length (bits)	16/16 + 1 parity	16	16/16 + 2 parity/ 16 + 6 EDR	16/16 + 2 parity/ 16 + 6 EDR	16
Instruction Times ( $\mu$ sec)					
Add	8.7	6.0	2.5	2.5	3.5-12.0
Multiply	21.3	No	21.0	21.0	24-64
Divide	9.3	No	20.0	20.0	78
Fl. Pt. Add	No	No	Opt	Opt	42.0
Fl. Pt. Multiply	No	No	Opt	Opt	52-92
Fl. Pt. Divide	No	No	Opt	Opt	151
Max Memory (bytes)	56K	32K	128K	128K	64K
No. of G.P. Registers	16	8	16	16	8
Max DMA Rate (bytes/sec)	DMA not supported	1.7M	2M	2M	1.7M
Price (\$)					
CPU + Memory					
8K Bytes	800	1,145	1,185	1,575	1,536
32K Bytes	2,300	2,650	3,045	3,435	3,411
64K Bytes	—	—	5,525	5,915	5,911
128K Bytes	—	—	10,485	10,875	—

**Table 3. TI 990/10: Specifications Compared with Those of Competitors**

	TI 990/10	Data General Nova 3	GA-16/330	GA-16/440	HP 21MX	Digital PDP-11/45 <sup>(2)</sup>
Word Length (bits)	16/16 + 1 parity/16 + 2 ECC	16	16/16 + 2 parity	16/16 + 2 parity	16	16/16 + 2 parity
Instruction Times (μsec)						
Add	3.1	1.8	4.6	0.8	1.9	1.8
Multiply	13.9-18.2	6.9 <sup>(1)</sup>	21.2	11.1	12.8	4.7
Divide	7.4-10.6	7.5 <sup>(1)</sup>	20.3	12.8	17.0	8.6
Fl. Pt. Add	No	7.7*	*	3.1-4.7*	22-54*	6.5*
Fl. Pt. Multiply	No	11.3*	*	4.8-7.9*	48-57*	8.2*
Fl. Pt. Divide	No	13.7*	*	7.6-8.7*	41-76*	9.9*
Max Memory (bytes)	2M	64K/256K	128K	2M	512K	253,952
No. of G.P. Registers	16	4	16	4	4	16
Max DMA Rate (bytes/sec)	6M	2M	2M	2M	1.2M	2M
Price (\$)						
CPU + Memory						
32K Bytes	2,975	4,400	5,250	11,800	7,650	23,900
64K Bytes	4,975	7,100	8,250	15,150	11,800	32,000
256K Bytes	17,900	34,200	—	38,750	36,150	55,500 <sup>(3)</sup>
512K Bytes	33,900	—	—	71,850	—	—

\*Optional, at extra cost.

Notes:

(1) Operands are unsigned integers on std.

(2) Core memory assumed, the PDP-11/45 can use faster MOS or bipolar.

(3) Maximum memory is 253,952 bytes.

TI can supply from 4K to 20K words of MOS memory on a single board. TMS 9900 and 990/4 systems can control up to 28K words (56K bytes) of memory. Thus a maximum 990/4 needs two additional memory boards but a 24K-word system requires only one if 4K words are on the processor board. The 990/10 has all memory on separate boards, and it can control up to 32K words without mapping or 1,024K words with mapping.

**Table 4. TI 990: Peripherals**

Model No.	Description
<b>LOW SPEED</b>	
600/601	733 KSR/ASR Silent 700 Data Terminals (30 cps; 1,200 baud)
620	913A Video Display (960 char)
670	120-cps Dot Matrix Printer
677/679	Model 588 "Line" Printer (88 cps; dot matrix)
686	804 Card Reader (400 cpm)
<b>MASS STORAGE</b>	
650	Floppy Disc (242K wd/diskette)
655	Removable Cartridge Disc (1.55M wd/disc; 4 drives/subsystem)
656	Fixed Cartridge Disc (1.55M wd/disc; 4 drives/subsystem)
<b>COMMUNICATIONS</b>	
631/633	Asynchronous (to 9,600 baud)
636	Synchronous
630/632	Asynchronous
634/635	Auto Calling Kits
638	Synchronous Modem (to 2,400 baud)
<b>MISCELLANEOUS</b>	
690	Universal PROM Programming Kit
695	16 I/O EIA Data Module
696	16 I/O TTL Data Module

Table 5 lists the various software packages and their memory and peripheral requirements.

## COMPATIBILITY

The TMS 9900, 990/4, and 990/10 processors use the same basic instruction set with expansions at the 990/10 level. With a few restrictions both hardware and software are upward compatible in the product line. The prototype system software is not compatible with the 990/10 because the software utilizes the 990/4 write protect feature.

Central programs and software modules are upward compatible. Programs written to run under the PX9MTR Prototyping System Software, for example, will also run under TX-990 and DX-10 operating systems. Conversely, programs for the PX9MTR can be created on TX-990 or DX-10 if the user is careful to limit facilities to those available to PX9MTR.

The 990 hardware and software are *not* compatible with any other series of computers, including TI's own 960 and 980 systems. The peripherals for the 990 have different interfaces than those used for the 960 and 980 computer lines, and the 990 software is entirely new.

## MAINTENANCE

Texas Instruments provides three types of contract maintenance for purchased systems: basic coverage, standard, and full.

**Table 5. TI 990: Software**

Package	Description
<b>Prototype System</b>	Resident monitor, assembler, and utilities for application prototyping and PROM memory development for the 990/4 and TMS 9900; requires 990/4, 733 ASR, 8K RAM, 735 ROM programmer front panel, power supply, and chassis; supports up to 28K words of memory and PROM programming module; cannot be used with 990/10
<b>990-733 ASR System Software</b>	For software development on 990 with 733 ASR terminal; includes monitor, assembler, utilities; requires 990/4, 733 ASR; 8K RAM; 733 ROM programmer front panel, power supply, chassis packaging; supports up to 32K words of memory
<b>990/10 Disc System Software</b>	For disc-based software development; includes DX-10 Operating System, Auto-Sysgen, Macro Assembler, 913 editor, link editor, Delong Librarian, card loader (on cassette); requires 990/10, 24 words of memory, ROM, 733 ASR; 913A CRT; DS31 Disc, programmer front panel; supports up to 1M words, card reader, line printers, CRTs, floppy disc, added disc
<b>FORTRAN IV</b>	ANSI X3.9-1966 with ANSI clarifications and ISA recommended extensions; including IBM FORTRAN-compatible direct access I/O; requires DX-10 and 32K words of memory
<b>COBOL</b>	ANSI COBOL subset = Level 1 nucleus plus table handling and sequential I/O as defined in ANSI X3.23-1975, with extensions; requires DX-10 and 32K words of memory
<b>Multuser Basic</b>	Dartmouth Basic equivalent for up to 8 concurrent users; requires DX-10 and 32K words of memory
<b>Asynchronous Communications</b>	Supports async communications to 9,600 baud; auto answer, auto call, error checking; requires 990/4 or 990/10, 2.5K words of memory, and TX-990 or DX-10 async or Bell dataset interface
<b>Synchronous Communications</b>	Supports sync communications to 9,600 baud; auto call, auto answer, error checking; requires 990/4 or 990/10, TX-900 or DX-10, 2.5K words of memory, access to 990/10 disc
<b>IBM S/3xO Cross Support</b>	Cross assembler plus a TMS 9900 simulator 2-pass assembler for System/360 and 370; requires 200K bytes under OS

Basic coverage provides for prime-shift preventive and emergency maintenance Monday through Friday for any 9 consecutive hours between 7 a.m. and 6 p.m. at the user's site. Standard coverage provides preventive and emergency service at the user's site for 16 consecutive hours between 7 a.m. and 1 a.m., Monday through Friday. Full coverage provides for on-site emergency and preventive service around the clock, 7 days a week.

In addition to these contracts, TI provides service on an on-call basis for users without a contract or outside of

contracted hours, with the fee depending on whether equipment is delivered to a repair depot or is repaired on-site during the prime shift or outside the prime shift or on Sundays and holidays.

**TYPICAL PRICES**

Equipment	Purchase Price \$
<b>Systems</b>	
990/4 CPU with 256 Wds of RAM	575
990/4 CPU with 4K Wds of RAM	800
<b>990/4 and 990/10 Memory Expansion Modules</b>	
4K Wds	625
8K Wds	1,000
12K Wds	1,500
16K Wds	2,000
20K Wds	2,500
<b>Write Protect Parity Option</b>	
4K Wds	50
Each Additional 4K Wds	25
<b>990/10 CPU with Memory</b>	
8K Wds	1,975
12K Wds	2,475
16K Wds	2,975
20K Wds	3,475
<b>990/10 CPU with Mapping and Memory</b>	
8K Wds	2,900
12K Wds	3,400
16K Wds	3,900
20K Wds	4,400
<b>990/10 CPU and ECC Memory</b>	
8K Wds	2,925
<b>990/10 CPU with Mapping and ECC Memory</b>	
8K Wds	3,850
<b>990/10 Memory Expansion Modules with ECC</b>	
8K Wds	1,950
8K Wds Add-on	1,400
16K Wds Add-on	2,800
24K Wds Add-on	4,200
<b>990 Prototyping or Program Development Systems with 733 ASR and Memory</b>	
8K Wds	5,950
12K Wds	6,300
16K Wds	6,750
20K Wds	7,225
24K Wds	7,700
<b>990/10 Program Development System with 733 ASR and Memory</b>	
8K Wds	519
<b>990/4 and 990/10 PACKAGING OPTIONS</b>	
3-Slot OEM Chassis without Power Supply (990/4 only)	175
6-Slot Chassis with Operator Panel and 5V, 20A Power Supply	950
6-Slot Chassis with Programmer Panel and 5V, 20A Power Supply	1,100
13-Slot Chassis with Operator Front Panel and 5V, 40A Power Supply	1,400
13-Slot Chassis with Programmer Front Panel and 5V, 40A Power Supply	1,550
Tabletop Chassis Option	150
Standby Power Supply	350
<b>I/O EXPANSION OPTIONS</b>	
CRU Expansion Kit	525
TILINE Expansion Kit	1,200
<b>TERMINAL OPTIONS</b>	
Model 733 KSR Data Terminal Kit	1,975
Model 733 ASR Data Terminal Kit	3,575
TTY/EIA Interface Module	375
Model 913A Video Display Terminal Kit	2,000

# TEXAS INSTRUMENTS — 990/9900 FAMILY SYSTEM REPORT

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## TYPICAL PRICES (Contd.)

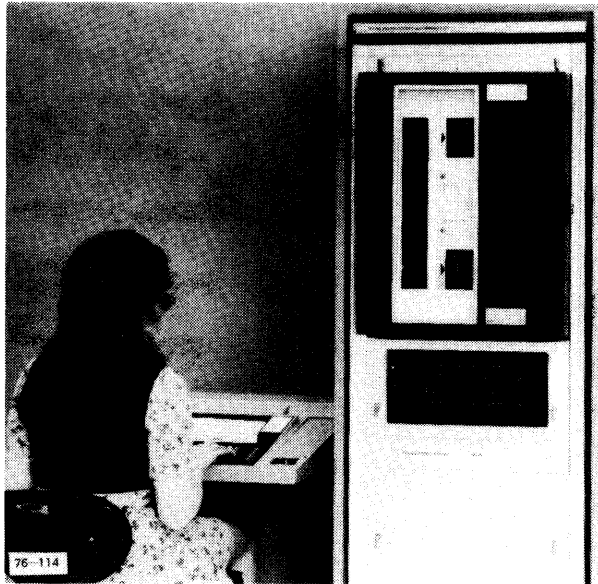
Equipment	Purchase Price \$
<b>DISC STORAGE</b>	
990 Floppy Disc Kit	2,950
Secondary Floppy Disc Unit	1,100
990 Floppy Disc Expansion	750
Model DS31 Disc Master Kit (removable)	9,650
Model DS32 Disc Master Kit (nonremovable)	7,050
Model DS31 Disc Secondary Kit	6,600
DS31 Secondary Kit with Power Supply	7,300
Model DS32 Disc Secondary Kit	4,000
DS32 Secondary Kit with Power Supply	4,700

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## TEXAS INSTRUMENTS INC.

### 990/9900 Family System Report Update



*Texas Instruments 700 Terminal Polling System*

### TERMINAL POLLING SYSTEM

The new 700 TPS (Terminal Polling System) interrogates remote networks of "Silent 700"-model programmable terminals, collects data, and stores it automatically on 9-track tape in IBM-compatible format. The data can be processed by a host computer, and the output redistributed automatically via TPS to the terminal network.

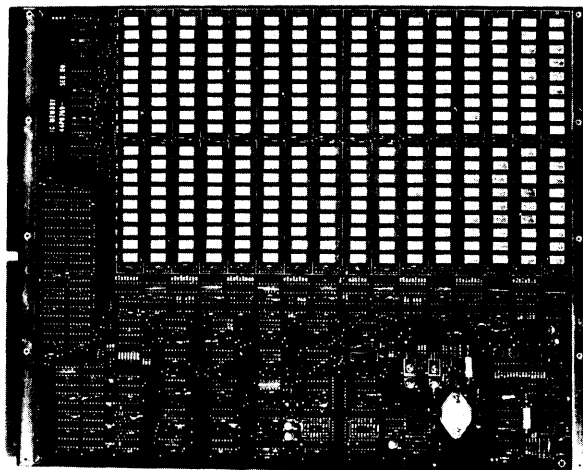
The minimum configuration consists of a TI 900 Series minicomputer with up to 64K bytes of RAM, a TI 9-track 800- or 1,600-bpi tape drive, and a "Silent 700" model 733 ASR data terminal with dual magnetic tape cassettes. The TPS has four built-in modems and auto-call units, and it can poll up to 200 model 742 terminals over four telephone lines. The System can be expanded to support up to eight telephone lines by adding external modems and auto-call units.

The basic TPS sells for \$37,800 or leases (on a 12-month basis) for \$1,200, including maintenance. Deliveries began in March 1976.



## VARIAN DATA MACHINES

### V76 Computer System Report



#### OVERVIEW

The big story with Varian's newest member of the V70 Series is price. The V76 costs 38 percent of the price of the earlier V75 computer with 128K bytes of memory; \$18,950 for V76 versus \$46,500 for V75. The difference in price is totally due to a new n-channel MOS memory developed specifically for the V76. The V76 uses the same processor as the V75, which in turn is the V73 processor with three chips added to implement an extended instruction set. The V75 was the first of the V70 computers to implement instructions to use eight general-purpose registers and to perform byte and double-precision operations.

Varian uses a large memory board and packs 32K or 64K words per board. Words are 16 bits long. A parity option adds one bit per word. Cycle time is 660 nanoseconds per word; access time is 550 nanoseconds. Maximum memory capacity is 256K bit words.

The memory is made up of 4K RAM chips housed in a 16-pin, dual-in-line package. The memory chips are currently supplied by Mostek, but plans call for both National Semiconductor, and Fairchild to supply them also. Varian optimistically offers its memory boards without parity, as well as with parity.

The Varian press announcement stated that the new memory will be compatible with 16K RAM chips when they become available, allowing 128K words or 256K words to be stored on each memory board. This implies that future V76 memory capacity will be 1M words.

The new memory is low in power consumption. This feature, combined with the dense packaging, allows either of the two mainframe chassis offered to house up to 256K words of memory with slots left over for options or peripheral device controllers.

One mainframe chassis is 7 inches high and has five P (for peripheral controller or memory module) slots. The other mainframe chassis is 14 inches high and includes 15 P slots.

The power supply for the CPU and memory is housed separately and requires 5-1/4 inches. A second power supply is required for CPU options, writable control store, memory map, and floating point. A Data Save Power Supply with battery is offered to maintain memory power in case of a main line power failure; it will maintain power to 64K words for four hours and to 256K words for 45 minutes.

Expansion chassis are available to add 22 I/O slots per chassis. Expansion chassis require additional power supplies and I/O party line expanders.

Like other members of the V70 Series, the V76 can implement memory mapping to 512K bytes, and 512 words of 64-bit writable control store (WCS). WCS can be used to implement floating point firmware, Fast FORTRAN firmware, decimal arithmetic, or user-coded firmware.

#### HEADQUARTERS

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# VARIAN DATA MACHINES — V76 COMPUTER SYSTEM REPORT

The V76 is totally upward compatible with the other members of the V70 Series; thus, it supports all the software and peripherals currently available.

The V76 is available like the V73 from a shopping list of components; thus, systems can be configured quite precisely, see Price Data. First deliveries of the V76 are scheduled for the first quarter of 1976.

## COMPETITIVE POSITION

The V70 Series of computers generally competes in the middle range of the minicomputer market. According to trade papers, Dr. Donal B. Duncan, president of Varian Data Machines, promised two new compatible computers for delivery in 1976: one at the bottom of the V70 Series and one at the top. In this context, the V76 must be classified as the top system of the line.

Table 1 compares the V76 with some competitors also in midrange: Data General Nova 3, General Automation GA-16/330, Digital PDP-11/45, and Hewlett-Packard HP 21MX. The V76 is not very price competitive for small systems; the smallest memory size is 64K bytes, and Nova 3, GA-16/330, and HP 21MX are all less expensive for 64K-byte systems. For 256K-byte systems, however, the V76 costs substantially less than the Nova 3 and HP 21MX. In all ranges, the V76 costs much less than the PDP-11/45. The GA-16/330 is unavailable with 256K-byte memory.

The software available for the V76 makes it a very competitive system for the top end of the minicomputer market.

Varian's recent marketing orientation has been toward making the software industry-compatible: COBOL, RPG II, and IBM level G FORTRAN compilers, and the TOTAL data base management system have all been introduced within the last eight months. The company's VORTEX II operating system has long been a big plus for the V70 Series.

Varian has wisely chosen to implement memory using dual-port modules. With the priority memory access (PMA) option, I/O throughput can reach 6M bytes per second.

The hardware and software features make the V76 performance competitive with the PDP-11/70 at less than one-half the price; see Table 2. The V76 is somewhat slower than the 11/70 for both fixed-point and floating-point arithmetic.

The V76 adds to the mounting evidence that Varian is finally "getting it together" on marketing. Public relations continues to lag despite the latest slogan, "Helping a fast world move faster."

**Table 1. Comparison of Varian V76 with Competitors**

	Varian Data V76	Data General Nova 3	General Automation GA-16/330	Digital PDP-11/45(1)	Hewlett-Packard HP 21MX
Word Length, bits	16/16 + 2 parity	16/16 + 2 parity	16/16 + 2 parity	16/16 + 2 parity	16
Inst. Times, $\mu$ sec					
Add	1.3	1.8	4.6	0.8-1.8	1.9
Multiply	4.8	6.9(2)	21.2	3.6-4.7	12.8
Divide	5.2	7.5(2)	20.3	7.5-8.6	17.0
Fl. P. Add(3)	3.7*	7.7*	*	2.8-6.5*	22-54
Fl. P. Multiply(3)	6.1*	11.3*	*	3.0-8.2*	48-57
Fl. P. Divide(3)	8.6*	13.7*	*	3.0-9.9*	41-76
Max. Memory, bytes	512K	64K/256K	128K	253,952	512K
No. of GP Registers	8	4	16	16	4
Max. DMA Rate, bytes/sec	2M/6M(4)	2M	2M	2M	1.2M
Price, \$					
CPU + Memory					
32K bytes	—	4,400	5,250	23,900	7,650
64K bytes	12,200	7,100	8,250	32,000	11,800
256K bytes	30,850	34,200	—	55,500(5)	36,150

\*Optional, at extra cost. NA - Not available. — Not applicable.

### Notes:

- (1) The PDP-11/45 can use core, MOS, or bipolar memories; the first number is for bipolar memory and the second number is for core memory. Price is for core memory.
- (2) Operands are unsigned integers on standard  $\times$  and  $\div$  feature.
- (3) All the floating point times are based on 2-word (32-bit) operands. The PDP-11/45 times are ranges based on memory used and the amount by which the CPU time overlaps floating processor time; the first number is CPU time and the second number is floating point processor time.
- (4) Via Priority Memory Access (PMA) and dual ports.
- (5) Maximum memory is 253,952 bytes.

**Table 2. Varian V76 Compared to the Digital PDP-11/70**

Characteristics	Digital PDP-11/70	Varian V76
<b>CENTRAL PROCESSOR</b>		
Microprogrammed Control Memory	Yes	Yes
No. of Registers	10; 3 stack pointers; 1 program counter; all 16-bit; all can be used as indexers.	8; 7 can be used as index registers.
Word Length, bits	16	16
Addressing		
Direct	To 64K bytes	To 4K bytes
Indirect	Single level to 64K	Multilevel to 64K
Indexed	Yes	Pre- and post-indexing
Mapping	Yes, to 2M bytes	Yes, to 512K bytes
Instruction Set Implementation	Firmware	Firmware
Types	Single word	Single and double word
Number Floating-Point Hardware Stack	400 std; 46 opt	187 std; 14 opt
Hardware Stack	Yes	No
Instruction Execution Times, $\mu$ sec		
Fixed-Point		
Add	1.0	1.3
Multiply	3.8	4.8
Divide	8.3	5.2
Floating-Point(1)		
Add	2.0	3.7
Multiply	3.9	6.1
Divide	4.9	8.6
Writable Control Store		
Interrupts	No	Up to 512 x 64 bits
Levels	4 lines, 8 levels	Up to 64
Type	Hardware	Hardware
<b>MAIN STORAGE</b>		
Type	Bipolar (cache); core (main memory)	n-channel MOS
Cycle Time, $\mu$ sec	0.24 (bipolar); 1.0/32 bits (core)	0.660/16 bits
Basic Addressable Unit	Word, byte	Byte, word, double-word
Bytes/Access	4	2
Cache Memory	Bipolar; 2,048 bytes	No
Capacity, bytes		
Min.	64K	64K
Max.	2M	512K
Increment Size, bytes	64K	64K/128K
Ports/Module	1	2
Error Checks	Parity std	Parity opt; 1 bit/byte
Memory Protection	Yes, memory management and 3 operating modes	Yes, in pages of 512 words
Memory Management	Yes	Yes
Interleaving	Yes, 2 way	No
<b>INPUT/OUTPUT</b>		
Max. Devices Addressable	No limit	64
Programmed I/O DMA	Yes (UNIBUS) Std (UNIBUS); plus 4 high-speed data channels	Yes, firmware Std; high speed; PMA

**Table 2. (Contd)**

Characteristics	Digital PDP-11/70	Varian V76
DMA Transfer Rate, bytes/sec	4M (UNIBUS); 5.8M (data channel)	0.66M (std); 2M (high speed); 6M (PMA)
<b>PRICE</b>		
Price for System with 128K-byte memory	\$54,600(2)	\$20,950(3)

Notes:  
 (1) Times are for 2-word operands.  
 (2) CPU bundled with console, line clock, and installation.  
 (3) With byte parity, programmer's console, installation, and memory mapping to 512K bytes.

# VARIAN DATA MACHINES — V76 COMPUTER SYSTEM REPORT

## PRICE DATA

Model No.	Description	Purchase Price \$	Monthly Maint. \$
<b>Processors</b>			
	V76 Computer, includes $\times/\div$ , automatic bootstrap loader for TTY, memory parity logic, DMA logic, chassis, programmer's console, and expanded instruction set.		
76-1100	V76 Computer in 7-inch chassis with 5 slots. Memory and power supply are not included.	5,400	105
76-1101	Same as 76-1100, except 14-inch chassis with 15 slots.	6,000	105
<b>Memories</b>			
76-2504	32,768-Word, Dual-Port Semiconductor Memory; 660-nsec cycle time.	4,800	45
76-2505	Same as 76-2504, except with parity.	5,300	50
76-2506	63,536-Word, Dual-Port Semiconductor Memory; 660-nsec cycle time.	8,900	85
76-2507	Same as 76-2506, except with parity	9,900	95
<b>Options</b>			
76-3001	Automatic Bootstrap Loader (ABL) for paper tape reader instead of standard for Teletype.	250	6
76-3002	Same as 76-3001, except for disc and operates with DMA.	250	6
76-3003	Same as 76-3002, except for device and operates with Priority Memory Access (PMA).	950	11
76-3004	Same as 76-3003, except for device.	950	11
76-3010	Real-Time Clock (RTC) for special configurations. Customers of non-VORTEX systems may specify source inputs of 10K Hz, line frequency, external input, or alternate counter overflow for both the free-running counter and the variable-interval interrupt counter.	250	6
76-3040	Option Package: Power Failure/Restart, Real-Time Clock, and TTY/CRT Controller	600	6
76-3041	Same as 76-3040, plus Memory Protect	750	8
76-3042	Same as 76-3040, plus Priority Memory Access (PMA).	1,000	10
76-3043	Same as 76-3040, plus PMA and Memory Protect.	1,150	12
76-3060	230V AC, 50 Hz System Power Input for processor.	500	0
70-3100	Block Transfer Controller (BTC) for automatic data transfers via the PMA channel. Max. of four BTCs per V76 processor with PMA.	1,500	11
70-3101	Priority Interrupt Module (PIM) eight levels of external interrupts. Max. of eight PIMs (64 levels) per V76 processor.	500	6
70-3102	Buffer Interlace Controller (BIC), provides block transfer for up to 10 peripheral controllers. Max. of eight BICs per V76 processor.	500	6
76-3200	Data Save Power Supply and Battery for semiconductor memory.	500	6
76-3300	Memory Map with automatic allocation and control for up to 256K words of main memory; includes cable.	2,500	39
76-3400	Floating Point Processor for single and double precision floating point arithmetic operations. Direct parallel connection to CPU and memory.	4,950	39
76-4000	256-Word (64 bits) Writable Control Store (WCS); 190-nsec cycle time; 16-register stack.	3,000	22
76-4001	Same as 76-4000, except 512 word.	4,000	28
76-4002	512-Word (64 bits) Writable Control Store (WCS); 190-nsec cycle time; 16-register stack; instruction register; writable decode control store; writable I/O control store.	5,000	39
<b>Power Supplies and Expansion Chassis</b>			
70-4080	Power Supply for CPU and Memory; 40 Amp.	2,000	15
70-4090	Power Supply for CPU Options: WCS, Memory Map, and Floating Point; 30 Amp.	1,000	6
70-4095	I/O Expansion Power Supply; 17 Amp.	1,000	10
70-4096	I/O Expansion Power Supply; 35 Amp.	1,500	12
70-9006	I/O Party Line Expander for 10-unit load in I/O Expansion Chassis.	600	11
70-9010	First I/O Expansion Chassis with 22 I/O slots and cables. Power supply is not included.	1,400	NC
70-9011	I/O Expansion Chassis with 22 I/O slots and cables. Power supply is not included.	1,400	NC
70-9110	Memory Expansion Chassis "Slave" with cables and 7 slots. Power supply is not included	1,100	NC
70-9111	Memory Expansion Chassis "Master" with cables and 7 slots. Power supply is not included.	1,100	NC

NC — No Charge



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### OVERVIEW

The Varian V-70 Series consists of four models: V-71, V-72, V-73, and V-74, all based on a general-purpose, microprogrammed digital computer. Microprogramming for the basic system is implemented by a read-only memory of 512 64-bit words contained in the processor. Up to three Writable Control Store (WCS) modules of 256 or 512 words (64-bit) can be added to a system to store microprograms. The processor can execute these microprograms from either the basic control or WCS.

Main memory for the V-71 and V-72 consists of core modules only. For the V-73 and V-74, it can consist of

core modules, semiconductor modules, or a combination. Each semiconductor module and some of the core modules have two ports of entry. While the V-71 and V-72 use only single-port modules, the V-73 and V-74 basic systems are dual-port systems that can attach either single- or dual-port memory modules. Differences among the models are summarized in Table 1.

Word length is 16 bits, increasing to 18 bits with the addition of memory parity. Cycle time per word is 660 nanoseconds for core memory and 330 nanoseconds for semiconductor memory.

The basic V-71, V-72, V-73, and V-74 microprocessors are Varian 620/f emulators. Thus, they can execute all the software that has been programmed for the 620 Series of computers and can also use all the 620 Series peripherals. The internal design of the microprocessor, however, has many features that are unavailable for the 620/f: facility for a WCS of 256 to 1,536 words, 16 general-purpose registers, 18-bit-wide address bus, instructions to load the WCS from main memory and to jump to and return from WCS, and (optionally) hardware-implemented floating point. In addition, the microprograms executed from WCS can implement an entirely different instruction set from that of the 620/f, and can address 65K words of memory. Optional memory mapping, standard on the V-74, extends addressing to 256K words for V-72 and V-73. (Memory mapping is unavailable on the V-71.)

Varian uses WCS in three basic ways:

- To enhance the 620/f emulator by adding such features as a microprogrammed floating-point processor, byte move and compare instructions, stack manipulation, Fortran — do-loop terminator, and parameter passing optimizing.
- To microprogram functions specific to a user's application. Varian supplies a microassembler plus test and debug aids.
- To define new instruction sets that utilize the processor's advanced features, such as multiple general-purpose registers and 18-bit-wide address bus.

**Table 1. Differences among V-70 Series Models**

CHARACTERISTIC	V-71	V-72	V-73	V-74
<b>MAIN STORAGE</b>				
Type	Core (single port)	Core (single port)	Core (single or dual port); MOS (dual port)	Core (single or dual port); MOS (dual port)
Cycle Time ( $\mu$ sec)	1.2	0.66, 1.2	0.66 or 1.2 (core); 0.33 (MOS)	0.66 or 1.2 (core); 0.33 (MOS)
Min Capacity (bytes)	32K	16K	16K	64K
Max Capacity (bytes)	64K	64K (in std CPU); 512K with mapping	64K (in std CPU); 512K with mapping	512K (mapping std)
Increment Size (bytes)	32K	Core: 16K, 64K	Core: 16K (dual port), 32K or 64K (single port); MOS: 16K (dual port)	Core: 16K (dual port), 32K or 64K (single port); MOS: 16K (dual port)
Parity	No	Opt	Opt	Opt
Protect	Opt	Std	Std	Std
Memory Mapping	No	Opt	Opt	Std

The memory mapping option with virtual memory addressing of 262,144 words is supported by VORTEX II, a new version of the Varian Omni-Task Real-Time Executive (VORTEX) operating system. With VORTEX II, memory mapping is transparent to the user.

When the models of the V-70 Series are operating as 620/f emulators, they are faster than the 620/f and inherit the extensive software library from the 620 Series, first introduced in 1965. The 620 Series computers have been used extensively for process control, test and measurement, scientific processing, data acquisition, and general-purpose processing. Software support ranges from monitoring for small-scale stand-alone systems to real-time and batch operating systems for medium- to large-scale installations. The V-70 and 620/f specifications are compared in Table 2.

Today, the V-70 Series is a strong contender in the data communications market. Standard hardware configurations are available for front-end preprocessing, remote concentration, data switching, remote job entry, and network control. Special software runs under the VORTEX/VORTEX II operating systems.

Varian markets its minicomputers from 20 sales offices across the United States, four in Canada, and one in Mexico. Outside North America, the company has offices in Australia, Brazil, Germany, Belgium, France, Holland, Israel, Sweden, Switzerland, and the United Kingdom. The European organization's headquarters in Zug, Switzerland, also handles marketing to Yugoslavia, Spain, Portugal, Italy, Greece, Turkey, Africa, India, the Near East, and Socialist countries.

All Varian users are invited to become members of the VOICE Users Group, which promotes library maintenance and program exchange. Varian acts as a communications channel for the group in order to eliminate redundant effort when several users are trying to solve the same problem.

**COMPETITIVE POSITION**

Varian Data Machines has consistently been a leader in the minicomputer field with its 520 and 620 Series of computers. The 520 Series, which is no longer marketed, was based on 8-bit words and aimed primarily at OEM buyers. The 620 Series was well-designed initially, and

**Table 2. Varian V-70 Series Compared with Varian 620/f**

CHARACTERISTIC	620/f	Varian 70 Series
<b>CENTRAL PROCESSOR</b>		
Instruction Set		
Number (std, opt)	142 std, 8 opt	175 std, 18 opt
Floating-point arithmetic	Subroutine	Subroutine or hardware
Microprogramming	No	Yes
No. of Programmable Registers	3	3
Decimal Arithmetic	No	No
Addressing		
Direct (no. of wds)	32K	2K; 32K*
Indirect	Multilevel to 32K	Multilevel to 32K
Indexed	—	Pre and post to 32K wds
Priority Interrupt Levels	0-64 in 8-level increments	0-64 in 8-level increments
<b>MAIN STORAGE</b>		
Type	Core (single port)	Core (single or dual port); MOS (dual port)
Cycle Time (μsec)	0.75	0.66, 1.2 (core); 0.33 (MOS)
Memory Mapping	No	Yes (opt on V-72, V-73; std on V-74)
Min Capacity (bytes)	8K	16K (core); 16K (MOS)
Max Capacity (bytes)	64K	512K with mapping
Increment Size (bytes)	8K, 16K	16K, 32K, or 64K (core); 16K (MOS)
Parity	No	Opt
Protect	Opt	Std
ROM	Opt	Std control store; WCS opt
Use	Program	Microcode
Capacity (bytes)	—	1,528 wds (64-bit wd)
<b>I/O CHANNELS</b>		
Programmed I/O	Std	Std
DMA Channels (no.)	Std (up to 4 with BICs); PMA opt (4)	Std (up to 4 with BICs); PMA opt (4)
Multiplexed I/O (no. of subchannels)	No	No
Max Transfer Rate (wds/sec)		
Within memory	222,222	252,525 (core); 505,050 (MOS)
Over DMA	274K; 1.3M (PMA)	382.7K; 1.5M (PMA-core memory); 3.3M (PMA-MOS memory)





its longevity rivals that of such durable competitive systems (and their compatible successors) as the DEC PDP-8, Honeywell 16 and 700 Series, Hewlett-Packard 2100 and 21MX Series, and IBM 1130. Like the manufacturers of these systems, Varian has kept the 620 Series competitive by adding new features: faster memories, better I/O facilities, more interrupt levels, new peripherals, and extensive software support.

Although the V-70 Series uses a microprogrammed processor that is quite different from the 620 Series processors, the basic system provides upward software and peripheral compatibility with the 620 by emulation. The V-70 Series, however, is much more powerful and flexible than the 620 because it can implement new features and new instruction sets in WCS. Also, fast MOS memory modules can be used on the V-70 to increase throughput.

With memory mapping, the V-70 can support up to 256K words (512K bytes) of main memory as compared to 32K words on the 620 Series (65K on 70 Series systems using WCS). The floating-point processor, released in 1974, is about 30 times faster than the 620 floating-point subroutines.

The V-70 competes with the systems mentioned previously, in real-time data acquisition, process control and industrial control applications, data communications, and general-purpose batch processing jobs. With its expanded memory capacity, using memory mapping, it also competes with such larger systems as the PDP-11/45, PDP-15, Sigma 5, Hewlett-Packard 3000, and the new Data General Eclipse.

The path Varian has chosen for the V-70 Series protects the 620 customers' investment in software and peripherals, and gives the 620 users a system for upgrading. In addition, the V-70 expands the market for Varian computers. Outside the OEM market, customers who will microprogram WCS are probably few. The feature adds considerable system flexibility and can significantly increase throughput for certain applications.

The new V-71 model, meanwhile, extends the V-70 Series downwards, providing new customers with a low-cost entry-level system. The compact 16K-word memory modules can be used on the other processors, effectively lowering the price of the whole line.

Varian's floating-point processor (delivered in 1974) handles both single and double floating-point operations. Tests run by Varian on the V-72 and V-73 indicate problems, such as double-precision  $A = B + C$ ,  $A = B \cdot C$  and  $A = B \div C$  running in the actual operating system environment compare favorably with a Data General 840 operating under FORTRAN V and with a PDP-11/45.

## User Reactions

A southern company that specializes in computer-based law enforcement, hospital, and other special control systems selected the V-73 for its law enforcement system because of the VORTEX software. The company felt that VORTEX was the best real-time operating system on the minicomputer market. At present this company uses Digital and Hewlett-Packard computers as well as the Varian 620 in hospital and other control systems.

The largest of the five law enforcement systems that this firm currently has in operation includes dual processors. Each processor has 32K words of core, a 200-million-word disc subsystem, two tape drives, two TTYs, card reader, paper tape reader, printer, two communication controllers, a variety of user-interfaced terminals, and special peripherals and disc and line switches installed by the user. Since its introduction, the system has been used successfully to emulate IBM 2740s that can communicate with state-owned computers. This law enforcement system is basically a data bank for wanted criminals, stolen goods, vehicle registration checks, and so on. VORTEX software has lived up to the company's high expectations, and the Varian components are extremely reliable. The user noted, however, that the OEM electromechanical devices were not quite as reliable.

A second V-73 user is a manufacturer primarily involved with the design and development of NASA's mission control center in Houston. The company also has a contract with NASA to maintain the medical records' storage and retrieval system for the space center's employees. When the system was set up, the first choice was the Hewlett-Packard 3000. Although Varian 73 was the second choice, it was still selected because of price. Additional savings resulted from "borrowing" peripherals from the seven Varian 620s already being used by the firm for other purposes. The programming staff could readily handle the required major modification to VORTEX because the assembly language was already familiar.

In retrospect, this user was glad the company had chosen Varian, because the installation was set up in a reasonably short time. Hewlett-Packard would have required a longer period because it had some initial problems with the 3000 software. Varian, moreover, compares favorably with other minicomputer manufacturers for system support and hardware reliability. NASA's mission control center has 15 minicomputers, including three Digital PDP-11/45s, seven Varian 620s (used mostly in dedicated applications), the V-73, and four minicomputers from other manufacturers. The V-73 has performed very well — this user, in fact, characterized it as a "better, cheaper 11/45."

## CONFIGURATION GUIDE

All models in the V-70 Series are based on the same processor hardware. The chief differences among the

four models are the type of memory used and its related options. The V-71 and V-72 use single-port core memory exclusively. The V-73 handles dual-port core and MOS memory modules. Minimum systems include 8K words (V-72 and V-73) or 16K words (V-71) of memory; memory expansion to 32K words is standard. With the memory mapping option, memory expands to 256K words. The minimum V-74 system is a 32K-word, dual-port system using either core or MOS modules. A number of V-72 and V-73 options, such as memory mapping, are standard features.

The basic processor for all three systems has hardware multiply/divide, at least one real-time clock, power fail/restart, memory protection, I/O bus with direct memory access (DMA), at least one automatic bootstrap loader (three are standard on the V-74), chassis for up to 32K words of memory, power supply, and programmer's console. In addition to a larger initial memory and memory mapping, the V-74 processor includes as standard the following features: priority memory access (PMA), 512 64-bit words of WCS, the equivalent of the first I/O chassis (18 slots), the equivalent of a memory expansion chassis with power for four memory modules, and a keyboard/CRT display terminal. All of these items are options on the V-73, so it can theoretically expand to the equivalent of any V-74 configuration. However, an expanded V-73 is more expensive than the equivalent V-74 configuration. The V-71 and V-72 are more restricted; they are single-port systems and cannot handle the faster MOS memory modules. As a result, they are slower and

less powerful than the V-73 and V-74; moreover, the V-71 cannot support the mapping option.

All three systems have various submodels to designate whether core or MOS memory, memory parity, or PMA are included. Table 3 lists the features of the various processor submodels.

Up to 32K words of memory can fit the mainframe for all processors; an expansion chassis is attached for each additional 32K words of memory (one expansion chassis is standard on the V-74). Each processor has a number of printed-circuit slots within the mainframe for attachment of options and peripherals ("P" slots). An I/O expansion chassis is available to attach additional peripheral devices and related options (such as the priority interrupt modules). Peripheral devices or options require either an I/O- or P-type slot. In addition to the number of P slots, expansion of the peripheral load must consider the bus load, which expands in increments of 10 loads after the original 10 in the main chassis have been exhausted.

In addition to the optional memory parity, memory mapping, and PMA features already described, a number of important options add flexibility to the processor and facilitate use of the peripherals. The WCS option can add up to three increments of 256 or 512 64-bit words to extend the processor's read-only control memory for additional user- or Varian-defined microinstructions. A data save option provides battery power to preserve the

**Table 3. Varian V-70 Series: Standard Features for Processor Submodels**

Processor Submodel	Memory Size (wds)	No. of P Slots	PMA	Parity (2 bits)	Memory	Data Save	System Availability			
							V-71	V-72	V-73	V-74
1000	32K	5	---	---	Core	---	---	---	---	X
1050	32K	5	---	Yes	Core	---	---	---	---	X
1100	8K	14	---	---	Core	---	---	X	X	---
1101	8K	14	Yes	---	Core	---	---	X	X	---
1200	8K	14	---	Yes	Core	---	---	X	X	---
1201	8K	14	Yes	Yes	Core	---	---	X	X	---
1300	16K	14	---	---	Core	---	---	X	---	---
1301	16K		Yes	---	Core	---	---	X	---	---
1330	16K	4	---	---	Core	---	X	---	---	---
1340	16K	4	---	---	Core	---	X	---	---	---
1350	16K	4	---	---	Core	---	X	---	---	---
1400(1)	16K	14	---	Yes	Core	---	---	X	---	---
1400(2)	32K or 16K	8	---	---	MOS	---	---	X	---	X
1401	16K	14	Yes	---	Core	---	---	X	---	---
1450	32K	8	---	Yes	MOS	Yes	---	---	---	X
1500	8K	4	---	---	MOS	---	---	---	X	---
1501	8K	4	Yes	---	MOS	---	---	---	X	---
1600	8K	4	---	Yes	MOS	---	---	---	X	---
1601	8K	4	Yes	Yes	MOS	---	---	---	X	---

**Notes:**

(1) Two Model 1400 processors are defined: one is a 16K-word core-based processor and the other is a 32K-word MOS-based processor.



contents of semiconductor memory modules during a loss in line voltage. The Priority Interrupt Module (PIM), Buffer Interlace Controller (BIC), and Block Transfer Controller (BTC) are particularly important for efficient handling of the various peripheral I/O subsystems. In addition, the hardware floating-point processor can appreciably enhance throughput for some applications.

In addition to the "basic" V-71, V-72, V-73, and V-74 processors, Varian offers five "standard" hardware/software packages:

- Model 72-0001 — 16K-word, V-72-based Batch/FORTRAN Processing System with cartridge disc, line printer, paper tape reader, and Teletype.
- Model 72-0002 — 24K-word, V-72-based Batch/FORTRAN Processing System with cartridge disc, line printer, nine-track magnetic tape drives, card reader, and Teletype.
- Model 72-0011 — 24K-word, V-72-based real-time operating system under VORTEX, with cartridge disc, card reader, and Teletype.
- Model 73-0020 — 32K-word, V-73-based real-time operating system under VORTEX, with cartridge disc, line printer, nine-track magnetic tape drive, card reader, and Teletype.
- Model 74-0050 — 64K-word, V-74-based real-time operating system with 512-word WCS and FORTRAN accelerator firmware, memory mapping, high-density (14.5-million-word) disc, line printer, nine-track magnetic tape drive, card reader, paper tape reader and punch, keyboard/CRT, and BTC.

Included in each package is the appropriate number of PIMs, BICs, I/O chassis, and cabinets to support the configuration.

The peripheral device complement for the V-70 Series includes: teletypewriters, paper tape and punched card equipment, line printers, and an impressive number of magnetic tape and disc storage units. Special peripherals are an oscilloscope display, plotters, various digital I/O controllers, and an extensive list of analog/digital equipment. Controllers are also offered for a number of commercial communications data sets. See Table 4 for a listing of peripherals with specifications.

Software includes two full-blown operating systems: VORTEX, which provides multiprogramming capability with real-time foreground processing and background batch processing, and MOS, which controls batch processing systems. VORTEX II is a special version of VORTEX used on systems with memory mapping.

Several language processors are available: DAS assembler (three versions), FORTRAN IV, two versions of BASIC, and RPG IV. BEST, a real-time monitor, provides control for small, dedicated real-time systems. Maintenance, debugging, and editing programs are offered, along with a math library. Table 5 lists major software packages and configuration requirements.

**Table 4. Varian V-70 Series: Peripherals**

Model No.	Description
<b>Discs</b>	
70-7500/01	Moving-head disc, 14.5M wds/2316-type pack, 4 drives/controller
70-7510/11	Moving-head disc, 46.7M wds/2316-type pack, 2 drives/controller
70-7600/01	Moving-head dual disc, 2.34M wds/drive, 1 fixed, 1 removable 5540-type cartridge, 2 drives/controller
70-7610/11	Moving-head disc, 1.17M wds/drive, 2315-type pack, 3 drives/controller
70-7700/1/2/3	Fixed-head discs, 61K/123K/246K/491K wds capacity, 17-msec avg access
<b>Magnetic Tape</b>	
70-7100/1	9-trk, 800 bpi, 25 ips; 4 drives/controller
70-7102/3	9-trk, 800 bpi, 37.5 ips; 4 drives/controller
<b>Paper Tape</b>	
70-6300	300-cps reader
70-6310/11	75-cps punch
70-6320	300-cps reader and 75-cps punch
<b>Punched Cards</b>	
70-6200	300-cpm reader
70-6201	35-cpm keypunch/punch
<b>Terminals</b>	
70-6100/2/4	Teletype ASR 33/ASR 35/KSR 35; 10 cps
70-6401	A/N CRT display with keyboard, TTY compatible
70-6400	Oscilloscope, Tektronix 611
<b>Printers</b>	
70-6701	245-1,100 lpm, 132 col, 64 char set
70-6720/21	300 lpm, 136 col, 64 char set
<b>Printer/Plotters</b>	
70-6606	80 styli/in. (1,320 A/N lines/in); 8.5-in. paper width
70-6608/02	100 styli/in. (1,000 A/N lines/in.); 11/14.875-in. paper width
70-6640	Model 70-6606 with 7x7 dot matrix print/plot, 64 char set
70-6641/42	Model 70-6608/02 with 7x11 dot matrix print/plot, 123-char set
70-661/3/5/7	100 styli/in. printer/plotters; 460/410/370/210 A/N lpm, 8.5/11/14.875/22-in. paper widths
70-6621/3/5/7	100 styli/in. printer/plotters with linear writing head, 690/890/690/550 lpm; 8.5/11/14.875/22-in. paper widths
<b>Process I/O</b>	
70-8000 Series	High-Level Analog Input Systems; 16-256 channels, differential & single-ended inputs
70-8100 Series	Low-Level Analog Input Systems; 13-bit A/D conversion, 16-256 channels
70-8200 Series	Digital-to-Analog (DAC) Subsystem; 10-, 12-, and 14-bit channels, to $\pm 10$ volts, $\pm 10$ mA; to 64 channels
70-8300	Digital Controllers; 1 16-bit input, 1 16-bit output register
70-8310/11	Digital Output; 2 16-bit output registers, 1 buffered input
70-8410/11	Digital Input; 4-256 16-bit input registers
70-8500	Relay Contact I/O modules
70-8601	Interface Console; for 16 channels, high-level analog input, 8 analog output, 1 digital I/O, 8 sense and control lines, timer, LED display

**Table 4. (Continued)**

<b>Communications</b>	
70-5201/2/3	MUX; for 16/32/64 sync, async, or direct-connection to 9,600 baud terminals
70-5211/2/3	Like 5201/2/3 but for systems with memory map
70-5702/12	BSC MUX; for up to 8 BSC channels via DMA; without/with memory mapping system
70-5401/02	Single/Dual Data Set Controller; for Bell 103 or 202
70-5501/02/03/04	Single or Dual Synchronous Controllers; to 2,400 or to 50K baud
70-5505/06/15/16	BSC Controller; for 1 or 2 channels, with or without memory mapping system
70-5601/02/03	Universal Async Controllers; with RS-232 C/20-60 ma current loop/20 ma relay
70-570	ACU Controller; for Bell 801

**Table 5. Varian V-70 Series: Software**

Package	Description
VORTEX	Real-time multitasking operating system with FORTRAN IV, RPG IV; requires CPU, PIM, BIC, 24K-word memory, TTY or CRT, and card, paper tape, or magnetic tape I/O
VORTEX II	Like VORTEX but with memory mapping management; same requirements as VORTEX except 32K memory and memory mapping option
MOS	Batch operating system with FORTRAN IV and RPG IV; requires CPU, PIM, BIC, 8K words of memory, magnetic tape I/O
Dataplot II	Adds Statos 31/33 printer/plotter capability to MOS; requires 16K words of memory
BEST (stand-alone)	Core-only real-time monitor; requires PIM, BIC, console
VPERT	Minimum 8K-word system software, paper tape I/O, runs under VORTEX (II) or MOS; requires either card reader or paper tape in addition to operating system
FORTTRAN (stand-alone)	Requires CPU, paper tape I/O, PIM, BIC
RPG IV (stand-alone)	Requires CPU, card reader, card punch, line printer
Microprogramming support	Runs under MOS or stand-alone; requires paper tape card or magnetic tape I/O
BASIC	Single terminal version; requires TTY or CRT, 8K-word memory, paper tape I/O; extended version requires TTY or CRT, 16K words of memory, paper tape I/O, disc
HASP/RJE	Runs under VORTEX (or VORTEX II); requires card or magnetic tape I/O
VTAM	VORTEX telecommunications access method; runs under VORTEX or VORTEX II
NCM	Network Control Module, using Network Definition Language (NDL); interface between operator and system to simplify network definition

**COMPATIBILITY**

The V-70 Series is upward software compatible with Varian's 620 Series computers. Magnetic tape data formats are IBM compatible. The V-70 Series uses the same peripheral devices as the 620.

**MAINTENANCE**

Varian supplies two types of on-call service contracts. The full-service plan provides on-call, on-site maintenance and replacement of needed parts for the contracted shift(s), while the limited-service plan charges lower monthly fees but requires the customer to pay for replacement parts. Full-time, on-site maintenance contracts are also provided. Customers who do not want maintenance contracts can choose individual, on-call, on-site repairs, charged on a per-hour basis. As an alternative, they can take equipment to an authorized factory service location.

**TYPICAL PRICES**

Model Number	Description	Purchase \$	Monthly Maint. \$
<b>CENTRAL PROCESSOR &amp; WORKING STORAGE</b>			
V-71 CPU (includes multiply/divide, I/O bus with DMA, chassis, power supply and programmer console, 1,200-nsec cycle time)			
71-1330	With 16K Core, 4 P Slots	7,200	120
71-1340	With 16K Core (includes power fail/restart, Teletype controller, automatic bootstrap loader for teletypes, real-time clock, 4 P slots)	8,100	120
71-1350	With 16K Core (same as 71-1340 except with memory protect)	9,100	120
71-2102	With 16K Core (includes single-port memory)	3,250	30
V-72 CPU, 14 P slots			
72-1100	With 8K Core	10,500	120
72-1101	With 8K Core, Priority Memory Access (PMA)	11,500	125
72-1200	With Memory Parity and 8K Parity Core	11,500	125
72-1201	Same as 72-1200 with PMA	12,500	130
V-73 CPU Same as V-72 except (chassis for up to 32K of dual-port memory, 14 P slots)			
72-1300	With 16K Core	14,500	120
72-1301	With 16K Core (includes PMA)	10,250	120
72-1400	With 16K Parity Core (includes memory parity)	11,250	125
72-1401	With 16K Parity Core (includes memory parity and PMA)	10,750	125
73-1100	With 8K Core	11,750	130
73-1101	With 8K Core, PMA	14,500	120
73-1200	With Memory Parity and 8K Parity Core	15,500	125
73-1201	Same as 73-1200 with PMA	16,000	130
73-1500	With 8K MOS Memory, 4 P Slots	15,000	130
73-1501	With 8K MOS Memory, PMA, 4 P Slots	16,000	135
73-1600	With 8K Parity MOS Memory, 4 P Slots	15,500	135
73-1601	Same as 73-1600 with PMA, 4 P Slots	16,500	140
V-74 CPU (same as V-73 except keyboard CRT display terminal, 3 automatic bootstrap loaders, console switch selectable PMA, direct memory access (DMA), memory map with memory protection for up to 256K of dual-port memory, 512 words of WCS, control console, processor, I/O, and memory chassis with associated power supplies in a single cabinet; provides 18 I/O slots, 8 MX slots, with power for up to four additional MOS or core memory modules and P slots as noted)			
74-1000	With 32K Core, 5 P Slots	35,900	345
74-1050	With Memory Parity and 32K Parity Core Memory, 5 P Slots	37,900	350
74-1400	With 32K MOS Memory, 8 P Slots	38,400	395
74-1450	With Memory Parity, 32K Parity MOS Memory, Data Saver, 8 P Slots	40,400	400
<b>CONFIGURATIONS</b>			
V71-0007	V71-Based Real-Time Operating System (running under VORTEX 32K core memory; interleaved 1,200 nsec; ASR-33, TTY and a 2.34-M word disc; includes V71 with 16K-core memory; 16K core memory (1,200 nsec); disc - ABL; core memory interleaving; PIM; ASR-33 TTY; card reader, 300-cpm; disc., 2.34-M words; I/O chassis with PIM and BIC; equipment cabinet; VORTEX installation package; Maintain II)	29,500	305
72-0011	24K V-72-Based Real-Time Operating System (running under VORTEX w/a 2.3M-word cartridge disc, TTY, and card reader; includes V-72 with 8K core memory; 8K core memories (2); PIM (2); BIC (2); ASR-33		



**TYPICAL PRICES (Contd.)**

Model Number	Description	Purchase \$	Monthly Maint. \$	Model Number	Description	Purchase \$	Monthly Maint. \$
73-0020	Teletype; card reader (300 cpm); disc (2.34M words); I/O chassis; cabinet; VORTEX installation package)	39,850	380	70-6608	11-in. Wide Printer/Plotter with Controller/110 styli/in., 2.2 ips, 1,000 A/N Ipi)	8,825	70
74-0050	32K Core Memory, V-73-Based Real-Time Operating System (includes V-73 with 8K core memory; 8K core memories (3); PIM (2); BIC (2); ASR-33 Teletype; card reader (300 cpm); line printer (245 lpm); 9-track mag tape (37.5 ips and control); disc (2.34M words); I/O chassis; cabinet (2))	71,600	515	70-6641	Same as Model 70-6608 with 123 char uc/lc, 7 x 11 dot matrix character generator, and simultaneous print/plot options	9,525	70
XX-2100	High Performance V-74-based Real-Time Operating System (includes V-74 with 32K memory; 8K core memories (4); block transfer controller; PIM (2); BIC; card reader (300 cpm); paper tape reader (300 cps) and punch (75 cps); line printer (245 lpm); mag tape (9-trk, 37.5 ips and control); disc (14.5M words); I/O expansion chassis; VORTEX installation package)	101,750	942	70-6602	14-7/8-in. Wide Printer/Plotter with Controller (100 styli/in., 2.2 ips, 1000 A/N Ipi)	9,025	70
XX-2101	Core Memories	3,500	30	70-6642	Same as Model 70-6602 with 123 char uc/lc, 7 x 11 dot matrix character generator, and simultaneous print/plot options	9,825	70
XX-2102	8K Word (16 bits) 660-nsec Cycle	4,000	35	70-6611	Bi-Scan™ Writing Head Models	8,925	70
XX-2103	16K Word (16 bit) Core Memory (1,200-nsec cycle time, single port)	3,250	30	70-6613	8½-in. Wide Printer/Plotter with Controller (100 styli/in., 1 ips, 460 A/N Ipi)	7,975	70
XX-2400	32K Words	15,000	130	70-6615	11-in. Wide Printer/Plotter with Controller (100 styli/in., 0.9 ips, 410 A/N Ipi)	8,175	70
XX-2411	Same as 2401 except 18-bit.	17,000	150	70-6617	14-7/8-in. Wide Printer/Plotter with Controller (100 styli/in., 0.8 ips, 370 A/N Ipi)	8,875	70
XX-2500	Semiconductor Memories	4,000	40	70-6621	22-in. Wide Printer/Plotter with Controller (100 styli/in., 0.6 ips, 210 A/N Ipi)	11,925	70
XX-3001/2	Available in dual-port models for V-73 and V-74. XX indicates the CPU series.	4,500	45	70-6625	8½-in. Wide Printer/Plotter with Controller (100 styli/in., 1.5 ips, 690 A/N Ipi)	7,975	70
XX-3003/04	8K Words (18 bits), 330-nsec Cycle	4,500	45	70-6625	Same as 70-6621 except with 14-7/8-in. Wide Printer/Plotter with Controller	8,875	70
XX-3010	PROCESSOR OPTIONS	250	5	70-6627	Same as 70-6617 except 1.2 ips, 550 A/N Ipi	1,925	70
XX-3030	Auto Bootstrap Loader	950	10	70-6720	Line Printers	8,900	99
XX-3031	Automatic Bootstrap Loader (for rotating memory instead of "standard" for Teletype for 72 & 73)	250	5	70-6721	Line Printer and Controller (300 lpm, 136 col, 64 char, 11-position form length selector switch)	9,900	99
XX-3032	Real-Time Clock	2,000	10	70-6760	Same as 70-6720 except 12-channel paper tape vertical format unit	10,200	102
XX-3050	Odd-Even Interleaving (for single-port 1,200-nsec core memory in expansion chassis, up to 256K for 72, 73)	1,000	10	70-6760	Static Eliminator Option	500	
XX-3060	Odd/Even Interleaving (for 32K words of single-port 1,200-nsec core memory in CPU)	500	10	70-6761	Line Printer (245 to 1,100 lpm, 132-col, segmented, buffered)	15,500	90
XX-3100	Wrap-Around Addressing Feature	250	5	70-7100	Mag Tape Unit and Controller (9-trk, 800 bpi, 25 ips)	7,500	50
XX-3101	230V ac, 50-Hz System Power Input	500	0	70-7101	Mag Tape Unit Slave	5,600	40
XX-3102	Block Transfer Controller (BTC)	1,500	10	70-7102	Same as 70-7100 with 37.5 ips; includes control for 4 units	9,000	75
73-3200	Priority Interrupt Module	500	5	70-7103	Mag Tape Unit Slave	7,000	60
XX-3300	Buffer Interface Controller (BIC)	500	5	70-5201/11	DATA COMMUNICATIONS		
XX-3400	Data Saver Power Supply and Battery for 32K Words of Semiconductor Memory (V-73 only)	500	5	70-5202/12	Data Communications Multiplexor (including message oriented control for up to 16 high-performance communication channels)	2,750	25
XX-4000	Memory Map	2,500	35	70-5203/13	Data Communications Multiplexor (for up to 64 communications channels)	7,000	60
XX-4001	Floating-Point Processor	4,950	35	70-5301	DCM LINE ADAPTERS		
XX-4002	Writable Control Store (256 Words of Semiconductor Memory)	3,000	20	70-5302/3/4	Asynchronous Line Adapter with RS232C and CCITT V24	1,000	6
70-7500	Writable Control Store (512 words)	4,000	25	70-5305	Direct-Connection Line Adapter	1,000	6
70-7501	MASS STORAGE*	5,000	35	70-5306	Synchronous Line Adapter with RS232C and CITT V24	1,500	10
70-7510	Disc Memory and Controller (2316 pack, moving head, 14.5M words single spindle)	16,400	190	70-5307	Binary Synchronous Communication Line Adapter (for 1 communication channel)	1,500	10
70-7511	Slave Unit for 70-7500	12,150	150	70-5308	Automatic Call Unit Line Adapter	1,000	10
70-7600	Same as 70-7500 except 46.7M Words; Dual Head Slave Unit for 70-7510	30,300	275	70-5401	Programmable Asynchronous Line Adapter (with RS232C or CCITT V24 compatibility for 4 channels of full- or half-duplex async operation up to 9,600 baud)	1,400	10
70-7601	Disc Memory and Controller (5440 pack, moving head, 2.34M words, one fixed and one removable disc)	12,500	100	70-5402	ASYNCHRONOUS MODEM CONTROLLERS**		
70-7610	Slave Unit for 70-7600	8,000	75	70-5402	Data Set Controller	650	5
70-7611	Disc Memory and Controller (2315 pack, moving head, 1.17M words)	10,000	85	70-5501	Dual Data Set Controller	800	5
70-7612	Slave Unit for 70-7610	6,000	65	70-5502	Data Set Controller	1,250	8
70-7700	Fixed-Head Disc and Controller (61K words, 17-msec avg access)	7,000	65	70-5505/15	Dual 70-5501 Data Set Controller	1,800	12
70-7701	With 123K Words	8,000	65	70-5506/16	Binary Synchronous Communication (facilities for 1 communication channel)	3,000	20
70-7702	With 246K Words	9,500	80	70-5601/2/3	Binary Synchronous Communication (facilities for 2 channels)	4,500	20
70-7703	With 491K Words	16,000	125	70-5701	UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLERS		
70-6100	INPUT/OUTPUT	1,580	35	70-5702	With RS232C Interface/20 or 60mA Current Loop or With 20 or 60mA Relay Interface	600	5
70-6102	ASR-33	3,265	25	70-5702	Auto Call Unit Controller	1,250	8
70-6104	KSR-35	5,320	30	70-5801	MULTIPLEXOR	2,000	20
70-6200	ASR-35	4,000	40		Binary Synchronous Communication Multiplexor		
70-6201	Card Reader and Controller (300 cpm)	8,000	60		OPTIONS		
70-6300	Card Punch and Controller (35 cpm)	2,300	22		Binary Synchronous Communications (wide-band interface option for Bell 300 Series modems.)	250	5
70-6310	Paper Tape Reader and Controller (300 cps)	3,000	25				
70-6311	Paper Tape Punch and Controller (75 cps, tabletop)	3,000	25				
70-6320	19" panel mounted	4,700	47				
70-6400	Paper Tape System (includes time-share controller, 300-cps reader, 75-cps punch)	5,675	45				
70-6401	Oscilloscope Display	2,850	25				
70-6402	Keyboard and Alphanumeric CRT	3,250	30				
70-6403	Same as 70-6401 with 70-5602 controller	2,950	25				
	Same as 70-6401 with kit and instructions to connect to controllers, or a spare unit						
	PRINTER/PLOTTERS						
	STATOS® 31 FAMILY						
70-6606	8½-in. wide w/Controller (80 styli/in., 2.75 ips, 1,320 A/N Ipi)	8,625	70				
70-6640	Same as Model 70-6606 with 64-char 5 x 7 dot matrix hardware character generator and simultaneous print/plot options	9,325	70				

\* Registered trademark of Varian Data Machines

**HEADQUARTERS**

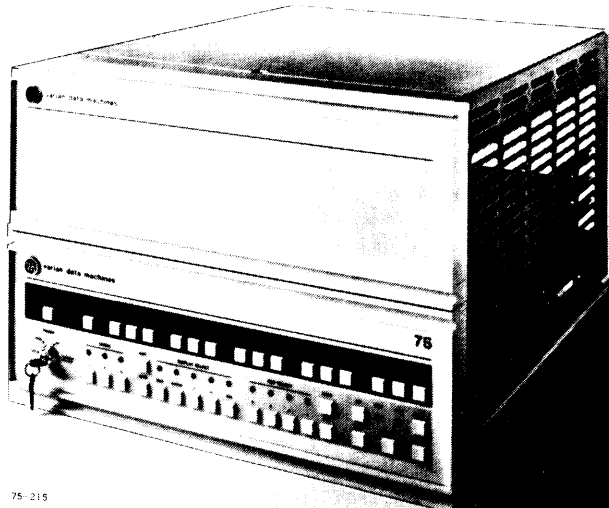
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# VARIAN DATA MACHINES

## V-70 Series System (V-75) Special Report Update



75-215

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### OVERVIEW

The Varian V-75 is a V-73 processor with new control store boards added to implement an extended instruction set. The V-72 and V-74 processors can also be adapted to use the new instruction set. The new instructions operate on eight of the computer's 16 general-purpose registers, previously accessible only to the micro-programmer. The new registers R0 through R7 incorporate the three V-70 register set and add new facilities.

Register	V-70 Use	V-75 Use
R0	A (accumulator)	Byte or word accumulator, most significant half of double word operand
R1	B (accumulator or index register)	General-purpose register, least significant half of double word operand
R2	X (index register)	General-purpose register
R3	—	General-purpose register
R4	—	General-purpose register and most significant half of double word operand
R5	—	General-purpose register, least significant half of double word operand
R6	—	General-purpose

Register	V-70 Use	V-75 Use
R7	—	General-purpose register

The general-purpose registers R1-R7 can be used either as accumulators or index registers.

The new instructions provide the following operations.

- Register to memory — Load/Store/Add/Subtract using any register and a memory location; address can be indirect and indexed by any general-purpose register.
- Double precision — Double Load/Store/Add/Subtract/AND/OR/exclusive OR between either double word register (R0, R1 or R4, R5) and two consecutive memory locations; address can be indirect and indexed by any general-purpose register.
- Jump IF test condition met — Register Zero/Not Zero/Negative/Positive; Double Register Zero/Not Zero; test can be on any general-purpose register or either double word register.
- Byte — Load/Store Byte between right byte in R0 and any memory location; address can be indexed by any general-purpose register.
- Immediate — Load/Add immediate operand into any register.
- Register-to-Register — Transfer/Add/Subtract between any two registers.
- Single Register — Increment/Decrement/Complement any register.

The V-75 System is sold with the following features as standard items.

- V-75 CPU.
- Dual memory buses.
- 64K words of memory.
- Two-way interleaving of core memory.
- Multiply/divide.
- Eight registers.
- Three automatic bootstrap loaders: cartridge disc, high-speed paper tape, Teletype or disc pack.
- Power fail/restart and real time clock.
- Five or eight CPU slots for memory or peripherals.
- Programmer console.
- DMA I/O bus.
- PMA (priority memory access to separate memory port) bus.
- Memory map with protection for 256K words (512K bytes) of memory.
- Writable control store of 512 words, 64 bits each.
- I/O chassis with 19 I/O slots and I/O expander.
- System cabinet.
- Keyboard/CRT display terminal.
- On-site installation.
- 90-day warranty.

#### Memory

Memory can consist of combinations of single port, two-way interleaved/non-interleaved core memory with 800/990-nanosecond effective cycle time; dual-port, two-way interleaved core memory with 450/660-nanosecond effective cycle time; and dual-port 330-nanosecond MOS memory. Byte parity is optional on all memory modules. Memory interleaving is also optional. Core memory is available in 8K-word and 16K-word modules. Bulk core modules of 64K words are also available; they consist of four 16K modules packaged together.

A second Writable Control Store (WCS) module can be added to the system or a Floating Point Processor. The new Fast FORTRAN Firmware in addition to the floating Point Processor not only decreases the amount of memory required for FORTRAN programs but shortens execution time substantially. The Fast FORTRAN Firmware performs the following functions:

- Array indexing.
- Parameter passing.
- DO loop termination.
- Double precision integer operations.
- Floating Point compare and branch.
- Square root.
- Converts relational expression to logical value.

#### Peripherals

The V-75 supports all the peripherals available for the rest of the V-70 line. With dual

memory ports and the PMA bus, the V-75 can support an I/O rate of 6M bytes per second as long as the CPU and the PMA channel are not in contention for the same memory module.

#### Software

Software for the V-75 is the same as that available for the rest of the V-70 Series, which is substantial. Recently, additional system software has been released for the V-75 as well as the rest of the V-70 line. The VORTEX II operating system release E2 supports the new V-75 instruction set. New additions to the Varian V-70 Series software include enhancements for data base management, telecommunications, and timesharing.

The Total data base management system developed by Cincom is now available to run under VORTEX II; which requires a V-70 CPU, 64K words of memory, an input device and a disc. It is the basic version of Total, a single task, fully reentrant system, which uses a random file organization. It supports the standard Total hierarchical network concept. Master files can be linked to several detail files. The random file organization is economical of disc space. The system has no query facility and no data security, thus the user must develop his own. A data base definition language and a data base generator are available to help the user develop a data base.

The Total license fee is \$9,500.

Cincom under Varian's supervision, will install Total in the VORTEX II operating system. First delivery implementation is scheduled for October 1975.

A single pass RPG II compiler that is industry compatible is now available.

A Time Sharing Subsystem is available under VORTEX II to support Basic from multiple terminals.

VTAM (VORTEX Telecommunications Access Method) Communication Software provides control functions for message switching, data concentration, and front-end processing under VORTEX. A terminal or communication line is handled like a logical unit, and the user can issue READ and WRITE commands to a terminal once it has been "Opened." The VTAM software handles line, data and device-dependent constraints.

Additions have recently been made to the FORTRAN IV compiler to bring it more in line with IBM FORTRAN Level G as well as to optimize the output code.



First production line deliveries of the V-75 are scheduled for August 1975. The VORTEX II support of the V-75 was released in July 1975.

### Competitive Position

The V-75 mainframe characteristics are compared to some of its major competitors in Table 1. These are Digital's PDP-11/70, the Interdata 8/32, and the SEL 32. Other strong competitors are the MODCOMP IV, Data General ECLIPSE 200, Digital Computer Control DCC-616, PRIME 300, and Hewlett-Packard HP 21MX. As Table 1 shows, members of the pack at the top of the minicomputer lines have a lot in common, yet there are significant differences inherent in innocuous-looking numbers. For example, the number of ports to memory modules entry shows that only the V-75 of those listed has dual memory ports. Memory modules on other systems, however, have multiple ports — MODCOMP IV modules can have up to four ports, the DCC 616 can have two. An operating system with any kind of elegance, even almost by accident, can substantially increase throughput using multiple-ported rather than single-ported memory. For multiple processor configurations, multi-ported memory allows processors to share memory modules with little contention.

A second item unique to the V-75 among the computers shown is writable control store. Interdata will probably provide it eventually for the 8/32, but it is not now available. It is available for the HP 21MX and the DCC 616. Writable Control Store is of little interest except to sophisticated users, but it is useful for OEM's who want to implement special features.

Of course, the V-75 is a 16-bit, word-oriented processor but, like the PDP-11/70, it has instructions for double word operands. Unlike the PDP-11/70 or Interdata 8/32, the V-75 does not have cache memory.

Instruction execution times on the four systems are very comparable, but the fixed-point times given are for 32-bit operands on the 8/32 and SEL 32 and for 16-bit operands on the PDP-11/70 and V-75.

For features not listed in the table, such as peripherals, the V-75 has a broad range of standard peripherals, disc and tape drives, printers, card and paper tape readers and punches. One device that Varian is well known for is its STATOS® Printer/Plotter. It is extremely fast and versatile. It is software supported by MOS under Data Plot II and by VORTEX.

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Varian is also a major instrumentation supplier, thus many A/D, D/A, and digital controllers are available.

Varian's strongest selling point must be its software. Although data base management systems are being discussed, selected, or whipped into shape by software gnomes at all the minicomputer factories, few are being delivered. Only Hewlett-Packard beat Varian's version of TOTAL to the punch with its Image 2000, which is like Total in many ways.

VORTEX II is a fine operating system, rivaled only by Digital's RSX-11D and MODCOMP's MAX IV. For commercial processing, Varian offers RPG II and IV, but Digital offers COBOL and Diversified Data Systems, Inc., with Interdata's blessing, offers COBOL for the 8/32.

Over the years, Varian's biggest problem has been public relations and a discernible, consistent, or sustained marketing policy. Varian's new president appears to be bringing new stock and climate to the vineyards from which rarer, finer policies can spring and, hopefully, flourish.

The Varian hardware has been good since the company brought out 620 in the 1960s. Its current software is outstanding. If the marketing and sales forces do team up and catch up with the hardware and software, the V-70 Series will be hard to beat.

### TYPICAL PRICES

Model Number	Description	Purchase Price \$	Monthly Maint \$
75-1000	V-75 computer with 64K words of single-port, 800-nsec core memory	35,000	380
75-1050	V-75 computer with 64K words of single-port, 800-nsec core memory with byte parity	37,000	385
75-1200	V-75 computer with 32K words of dual-port, 400-nsec core memory and 32K words of single port, 800-nsec core memory	44,500	380
75-1250	Same as 75-1200 with byte parity	46,500	385
75-1400	V-75 computer with 32K words of dual-port, 330-nsec MOS memory and 32K words of single-port, 800-nsec core memory	48,500	435
75-1450	Same as 75-1400 with byte parity	50,500	440
75-1600	V-75 computer with 64K words of dual-port, 330-nsec MOS memory	55,000	440
75-1650	Same as 75-1600 with byte parity	57,000	440
75-2100	8K words of 450/660-nsec dual-port	3,500	33
75-2101	Same as 75-2100 with byte parity	4,000	39
75-2104	16K words of 800/990-nsec single-port	4,500	36
75-2105	Same as 75-2104 with byte parity	4,000	42
75-2400/1	32K words (4 8K-word modules) of 450-nsec, dual-port — includes slave/master memory expansion chassis and power supply	15,000	143
75-2410/1	Same as 75-2400/1 with byte parity	17,000	165
75-2420/1	64K words (4 16K-word modules) of 800-nsec, single port; includes slave/master memory expansion chassis and power supply	16,000	150
75-2430/1	64K words (4 16K-word modules) of 800-nsec, single port memory; includes memory expansion chassis and power supply	18,000	172
75-2500	Semiconductor Memory		
75-2501	8K-word dual port MOS 330-nsec cycle time	5,000	44
	Same as 75-2500 with byte parity	5,500	50
	Processor Options		
75-3100	Block transfer controller	1,500	11
75-3101	Priority interrupt module (automatic storing and vectoring of 8 levels of external interrupts)	500	6
75-3102	Buffer Interlace controller	500	6
75-3400	Floating point processor (single precision and double precision operations)	4,950	39
75-4000	256-word writable control store	3,000	22
75-4001	512-word writable control store	4,000	28
75-4002	512-word writable control store (with instruction register, writable decoder control store, writable I/O control store)	5,000	39

Table 1. Varian V-75 Compared to Major Competitors

Characteristics	Digital PDP-11/70	Interdata 8/32	SEL 32	Varian V-75
<b>CENTRAL PROCESSOR</b>				
Microprogrammed	Yes	Yes	Yes	Yes
Control Memory	ROM	ROM	ROM	ROM
No. of Registers	10 accs: 3 stack pointers; 1 PC; all 16-bit; all can be used as indexes	2 stacks of 16 32-bit gen regs std; 6 more sets opt	8:3 can be used as index regs	8:7 can be used as index regs
Word Length	16	32	32	16
Addressing				
Direct	To 64K bytes	To 1M bytes	To 512K bytes	To 4K bytes
Indirect	Single level	No	Multilevel to 16M bytes	Multilevel to 65K bytes
Indexed	Yes	Yes	Pre- and post-indexing	Pre- and post-indexing
Mapping	Yes, to 2M bytes	Yes, to 1M bytes	Yes, to 16M bytes	Yes, to 512K bytes
Instruction Set Implementation Types	Firmware Single word	Firmware Single and double word	Firmware Half and full word	Firmware Single and double word
Number Floating-Point Hardware Stack	400 std; 46 opt Hardware opt Yes	214 Hardware opt No	152 Firmware std No	187 std; 14 opt Hardware opt No
Instruction Execution Times ( $\mu$ sec)				
Fixed Point				
Add	1.0	1.1	1.2	0.7/1.3/2.0 <sup>(2)</sup>
Multiply	3.8	5.6	4.5	4.5/4.8/5.4 <sup>(2)</sup>
Divide	8.3	5.7	5.1	4.8/5.2/6.0 <sup>(2)</sup>
Floating-Point <sup>(1)</sup>				
Add	7.9	2.0	3.0	3.7
Multiply	9.9	3.2	4.5	6.1
Divide	10.9	5.0	8.9	8.6
Writable Control Store	No	No	No	Up to 512 x 64 bits
Interrupts				
Levels	4 lines, 8 levels	1,024	128	Up to 64
Type	Hardware	Hardware	Hardware	Hardware
<b>MAIN STORAGE</b>				
Type	Bipolar (cache); core (main memory)	Core	Core	Core (2 speeds); MOS
Cycle Time* ( $\mu$ sec)	0.24 (bipolar); 1.0 (core; 32 bits)	0.750	0.600	0.660/0.990; 0.330
Basic Addressable Unit	Word, byte	Word, half word, byte	Double word, word, half word, byte, bit	Byte, word, double word
Bytes/Access	4	4	4	2/4
Cache Memory Capacity (bytes)	Bipolar, 2,048 bytes	Bipolar, 16 bytes	No	No
Min	64K	131,072	32,768	131,072
Max	2M	1,048,576	1,048,576	512K
Increment Size (bytes)	64K	128K	32K	8K/16K (Core); 8K (MOS)
Ports/Module	1	1	1	1/2
Error Checks	Parity std	Parity opt	Parity: 1 bit/byte std	Parity (opt); 1 bit/byte
Memory Protection	Yes, memory management and 3 operating modes	Yes, with memory management	Yes, in pages of 512 words	Yes, in pages of 512 words
Memory Management Interleaving	Yes, 2-way	Yes, 4-way	Yes, 2 reads/4 writes	Yes, 2-way
<b>INPUT/OUTPUT</b>				
Max Devices Addressable	No limit	1,024	Via IO Crs	64
Programmed I/O	Yes (UNIBUS)	Yes	Yes, IOC	Yes, firmware
DMA	Std (UNIBUS); plus 4 high-speed data channels	Std for 112 devices	IOC	Std; high speed; PMA
DMA Transfer Rate	4M bytes/sec (UNIBUS); 5.8M bytes/sec (data channel)	6M bytes/sec	1.2M bytes/sec each; 26.7M bytes/sec aggregate	0.66M bytes/sec (std); 2M bytes/sec (high speed); 6M bytes/sec (PMA)
Price for System with 128K-byte Memory	\$54,600 <sup>(3)</sup>	\$51,900	\$43,900	\$46,500 <sup>(4)</sup>

Notes:

\*Effective memory cycle time varies with type of memory and number of memory modules interleaved.

- (1) PDP-11/70 times include operand load times. Also floating-point processor operates in parallel with central processor. Floating-point times are for 64-bit operands.
- (2) Three times are for 330-nsec MOS/660-nsec core/990-nsec core.
- (3) CPU bundled with console, line clock, and installation.
- (4) With 64K bytes of 660-nanosecond, dual-port interleaved core memory with byte parity, 64K bytes of 990-nsec, interleaved, single-port, core memory with byte parity, keyboard/CRT console, installation, memory mapping to 512K bytes, and writable control store.



# DIRECTORY OF SUPPLIERS

## A

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(513) 242-4220

**ACEC** (See Ateliers de Constructions  
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DATA SERVICES DIV  
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Union City NJ 07087  
(201) 865-3220

**ACS INC** (See Action Communication Systems  
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**ACTION COMMUNICATION  
SYSTEMS INC**  
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Dallas TX 75231  
(214) 750-3000

**ACTION/DICTOGRAPH PRODUCTS**  
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Meriden CT 06459  
(203) 238-2326

**ACTRON INDUSTRIES INC**  
700 Royal Oak Dr  
Monrovia CA 91016  
(213) 359-8216

**ACTS COMPUTING CORP**  
29200 Southfield Rd  
Southfield MI 48075  
(313) 557-6800

**ADAGE INC**  
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Boston MA 02215  
(617) 783-1100

**ADDRESSOGRAPH MULTIGRAPH  
CORP**  
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(216) 283-3000

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Schaumburg IL 60172  
(312) 397-1900

**VARITYPER DIV**  
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Mountainside NJ 07092  
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**ADL SYSTEMS INC**  
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Burlington MA 01803  
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**ADLER** (See Triumph-Adler AG)

**ADPAC COMPUTING LANGUAGES  
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San Francisco CA 94105  
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**ADS** (See Anker Data Systems)

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New York NY 10022  
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(703) 524-8330  
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London SW1X 7JP, England  
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(408) 734-4330

### ADVANCED SYSTEMS INC

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### ADVANCED TERMINALS INC

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Mohawk NY 13407  
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Steiheimerstrasse 117, West  
Germany

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London, WC 2,  
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### ALOS LTD

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Skokie IL 60076  
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### AMERICAN APPRAISAL CORP

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### AMERICAN AUTOMATIC TYPEWRITER

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Chicago IL 60639  
(312) 384-5151

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#### CORPORATE HDQTRS

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(203) 552-2000

### AMERICAN INFORMATION DEVELOPMENT

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(415) 441-4422

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### AMERICAN MICROSYSTEMS INC (AMI)

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(408) 246-0330

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Atlanta GA 30309  
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Whitinsville MA 01588  
(617) 234-7455

**AMERICAN USED COMPUTER CORP**

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Boston MA 02215  
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Sunnyvale CA 94086  
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790 Greenfield Dr  
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(714) 442-3451

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(717) 845-5602

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Oak Brook IL 60521  
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**ANKER WERKE AG**

D4800 Bielefeld (West Germany)  
Am Stadtholz 39  
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German Democratic Republic  
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Ann Arbor MI 48103  
(313) 769-0926

**APL SERVICES INC**

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Trenton NJ 08628  
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**APPLICATIONS SOFTWARE INC**

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(714) 547-6954

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155 Whitney Ave  
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(203) 787-4107

**APPLIED DATA PROCESSING SUBSIDIARY OF COMPUTER DATABANKS**

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North Haven CT 06473  
(203) 787-4107

**APPLIED DATA RESEARCH INC****HDQTRS**

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CN-8  
Princeton NJ 08540  
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(201) 540-6300

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Alexandria VA 22314  
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**AUTOMATIC ELECTRIC CO**

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106 Bureaux de la Colline  
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Hachioji-Shi  
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Stamford CT 06902  
(203) 359-2100

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Monroe NC 28110  
(704) 289-3128

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Newton MA 02195  
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Newport Beach CA 92663  
(714) 833-4600

**COLUMBIA SCIENTIFIC**

**APPLIED COMPUTER SYSTEMS DIV**  
PO Box 6190  
Austin TX  
(512) 258-5191

**COMCET (See Comten Inc)****COMDATA CORP**

8115 N Monticello  
Skokie IL 60076  
(312) 677-3900

**COMGRAPHIX INC**

**SW MICROFILM DIV**  
2601 E Yandell Dr  
El Paso TX 79903  
(915) 566-9351

**COMMONWEALTH INFORMATION CORP**

5001 W Broad St  
Richmond VA 23230  
(804) 649-9073

**COMM-PRO ASSOCIATES**

638 14th St, Suite 700  
Manhattan Beach CA 92066  
(213) 376-1344

**COMM-SCI SYSTEMS CORP (See Argonaut Information Systems)****COMMUNITY COMPUTER CORP**

185 W School House La  
Philadelphia PA 19144  
(215) 849-1200

**COMNET (See Computer Network Corp)****COMPAGNIE HONEYWELL-BULL SA**

**EUROPE AND LEVEL 61 DESIGN CTR**  
94 Ave Gambetta  
75 Paris 20 France  
(1) 355-44-33

**COMPAGNIE INTERNATIONALE**

**POUR L'INFORMATIQUE**  
68 Rte de Versailles  
78- Louveciennes, Seine, France

**COMPATA INC**

6150 Canoga Ave  
Woodland Hills CA 91364  
(213) 884-5400

**COMPRO CORP**

3001 Red Hill Ave, Bldg V1-103  
Costa Mesa CA 92626  
(714) 540-7153

**COMPUCORP**

12312 W Olympic Blvd  
Los Angeles CA 90064  
(213) 820-5611

**COMPUTA ELECTRONIC GMBH**

4322 Sprockhovel 1 (West Germany)  
Wuppertaler Strasse 50  
(02324) 7577

**COMPU-DIAL**

21 Diney Ave  
Cherry Hill Industrial Pk  
Cherry Hill NJ 08034  
(609) 424-4700

**COMPUGRAPHIC CORP**

Industrial Way  
Wilmington MA 01887  
(617) 658-5000

**COMPUNETICS INC**

1100 Eldo Rd, Monroeville Ind Pk  
Monroeville PA 15146  
(412) 373-2520

**COMPUSCAN INC**

900 Hayler St  
Teterboro NJ 07608  
(201) 288-6000

**COMPU-SERV NETWORK INC**

5000 Arlington Ctr Blvd  
Columbus OH  
(614) 457-8600

**COMPUTATION PLANNING**

7840 Aberdeen Rd  
Bethesda MD 20014  
(301) 654-1800

**COMPUTEK INC**

143 Albany St  
Cambridge MA 02139  
(617) 864-5140

**COMPUTEL LTD**

Eastern Rd  
Bracknell, Berkshire, England



**Computel System Ltd**

**COMPUTEL SYSTEM LTD**  
 1200 St Laurent Blvd  
 Ottawa, Ontario, Canada K1K3B8  
 (613) 746-4353

**COMPUTER AUTOMATION INC**  
 18651 Von Karman St  
 Irvine CA 92664  
 (714) 833-8830

**COMPUTER CO**  
 Westmoreland Ave  
 Richmond VA 23219  
 (804) 358-2171

**COMPUTER COMMUNICATIONS INC**  
 2610 Columbia St  
 Torrance CA 90503  
 (213) 320-9101

**COMPUTER COMPLEX INC** (See Tymshare Corp)

**COMPUTER CORP OF AMERICA**  
 575 Technology Sq  
 Cambridge MA 02139  
 (617) 491-3670

**COMPUTERCRAFT SERVICES INC**  
 Hamley Industrial Ct  
 St. Louis MO 63119  
 (314) 645-6336

**COMPUTER DEVICES INC**  
 9 Ray Ave  
 Burlington MA 01803  
 (617) 273-1550

**COMPUTER DYNAMICS INC**  
 112 Shawmut Ave  
 Boston MA 02118  
 (617) 357-8170

**COMPUTER ENTRY SYSTEMS CORP**  
 2141 Industrial Pkwy  
 Silver Spring MD 20904  
 (301) 622-3500

**COMPUTER EQUIPMENT CORP**  
 14616 Southlawn Dr  
 Rockville MD 20850  
 (301) 424-4790

**COMPUTER GENERATION INC**  
 3781 NE Expwy, Suite 101  
 Atlanta GA 30340  
 (404) 458-2371

**COMPUTER HARDWARE CONSULTANTS & SERVICES**  
 10 Pheasant Run  
 Newtown PA 18940  
 (215) 968-5900

**COMPUTER INFORMATION MANAGEMENT CO**  
 325 Oak Plz Bldg  
 3707 Rawlins St  
 Dallas TX 75219  
 (214) 526-4280

**COMPUTER INNOVATIONS**  
 70 W Hubbard St, Suite 401  
 Chicago IL 60610  
 (312) 329-1561

**COMPUTER INTERACTIONS INC**  
 425 Northern Blvd  
 Great Neck NY 11021  
 (212) 895-7435

**COMPUTER INVESTORS GROUP DATA RECALL PRODUCTS DIV**  
 65 Washington Ave  
 Stamford CT 06902  
 (203) 359-2100

**COMPUTERISTICS** (See Uniroyal Inc)

**COMPUTER LINGUISTICS INC HDQTRS**  
 24 Aviation Rd  
 Albany NY 12205  
 (518) 458-1860

**COMPUTER LINK CORP PERIPHERY INC DIV**  
 14 Cambridge St  
 Burlington MA 01803  
 (617) 272-7400

**COMPUTER MACHINERY CORP**  
 2500 Walnut Ave  
 Marina del Rey CA 90291  
 (213) 390-8411

**COMPUTER MANAGEMENT CORP**  
 4900 Water's Edge  
 Raleigh NC 27604  
 (919) 851-7300

**COMPUTER MANAGEMENT GROUP LTD**  
 Sunley House, Bedford Pk  
 Croydon CRO 2AP, Great Britain

**COMPUTERM CORP**  
 201 Penn Ctr Blvd  
 Pittsburgh PA 15235  
 (412) 823-6116

**COMPUTER NETWORK CORP**  
 5185 MacArthur Blvd  
 Washington DC 20018  
 (202) 244-1900

**COMPUTER OPERATIONS INC**  
 10774 Tucker St  
 Beltsville MD 20705  
 (301) 937-5377

**COMPUTER OPTICS INC**  
 Berkshire Industrial Pk  
 Bethel CT 06801  
 (203) 744-6720

**COMPUTER PROCEDURES CORP**  
 181 S Franklin Ave  
 Valley Stream NY 11581  
 (516) 791-2000

**COMPUTER PROCESSING INC**  
 200 Manhattan Bldg  
 Muskogee OK 74401  
 (918) 683-3231

**COMPUTER PRODUCTS**  
 1400 NW 70th St  
 PO Box 23849  
 Fort Lauderdale FL 33307  
 (305) 974-5500

**COMPUTER RESEARCH INC**  
 4 E Kings Hwy  
 Haddonfield NJ 08033  
 (609) 428-0020

**COMPUTER RESOURCE SERVICES INC**  
 6501 N Black Canyon Hwy  
 Phoenix AZ 85015  
 (602) 242-9121

**COMPUTER SCIENCES CANADA LTD**  
 Place du Canada  
 Montreal 101, Quebec, Canada  
 (416) 449-0500

**COMPUTER SCIENCES CORP**  
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 El Segundo CA 90245  
 (213) 678-0311

**COMPUTER SERVICES CORP**  
 23225 Northwestern Hwy  
 Southfield MI 48075  
 (313) 354-2491

**COMPUTER SHARING SERVICES**  
 2498 W Second Ave  
 Denver CO 80223  
 (303) 934-2381

**COMPUTER SIGNAL PROCESSORS INC**  
 209 Middlesex Tpk  
 Burlington MA 01803  
 (617) 272-6020

**COMPUTER SOFTWARE CO, THE**  
 6517 Everglade Dr  
 Richmond VA 23225  
 (804) 276-9200

**COMPUTER SYSTEMS INC**  
 PO Box 10, 69 E Main St  
 Little Falls NJ 07424  
 (201) 785-4160

**COMPUTER SYSTEMS AND EDUCATION CORP**  
 111 Ash St  
 East Hartford CT 06108  
 (203) 528-9216

**COMPUTER TASK GROUP INC HDQTRS**  
 5586 Main St  
 Buffalo NY 14221  
 (716) 634-9090

**BRANCH OFFICE**  
 1703 South Ave  
 Syracuse NY 13207  
 (315) 475-2126

**COMPUTER TECHNOLOGY LTD (CTL)**  
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 Hemel Hempstead, Herts HP2 7EQ  
 England  
 (0442) 3272

**COMPUTER TERMINAL CORP** (See Datapoint Corp)

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 22 Newton Pl  
 Plainview NY 11803  
 (516) 293-6611

**COMPUTER TRANSCIEVER SYSTEMS INC**  
 PO Box 15  
 Paramus NJ 07652  
 (201) 261-6800

**COMPUTER TRANSMISSION CORP**  
 2352 Utah Ave  
 El Segundo CA 90245  
 (213) 973-2222

**COMPUTER WARES INTL** (See General Computer Services)

**COMPUTERWISE INC**  
 13124 S 71 Hwy  
 Grandview MO 64030  
 (816) 765-3330

**COMPU-TIME INC**  
 PO Box 960  
 Daytona Beach FL 32014  
 (904) 255-2486

**COMPUTING TECHNOLOGY CO** (See Informatics Inc)

**COMPUTONE SYSTEMS INC**  
 361 E Paces Ferry Rd NE  
 Atlanta GA 30305  
 (404) 261-0070

**COMPRESS** (See Comten Inc)

**COMSERV CORP METRO OFFICE PK**  
 3050 Metro Dr  
 Minneapolis MN 55420  
 (612) 854-2020

**COM-SHARE INC CORPORATE HDQTRS**  
 900 Wolverine Tower  
 PO Box 1588  
 Ann Arbor MI 48106  
 (313) 994-4800

**COM-SHARE LTD**  
 230 Galaxy Blvd  
 Rexdale, Ontario M9W 5R8, Canada

**COMSTAR CORP**  
 7413 Washington Ave S  
 Edina MN 55435  
 (612) 941-4454

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 PO Box 784  
 Reston VA 22070  
 (703) 471-7141

**COMTEN INC PERFORMANCE & EVALUATION DIV**  
 2 Research Ct  
 Rockville MD 20850  
 (301) 948-8000

**COMTERM LTD**  
 147 Hymus Blvd  
 Montreal 730, Quebec, Canada  
 (514) 697-0810

**CONCAP COMPUTING SYSTEMS**  
 303 Hegenberger Rd  
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 (415) 635-5750

**CONCORD COMPUTING CORP**  
 7 Alfred Circle  
 Bedford MA 01730  
 (617) 275-1730

**CONDATA INC**  
 Alison Bldg  
 1809 Walnut St  
 Philadelphia PA 19103  
 (215) 569-4240

**CONRAC CORP**  
 Mill Rock Rd  
 Old Saybrook CT 06475  
 (203) 388-3574

**CONRAC CORP**  
 600 N Rimsdale Ave  
 Covina CA 91722  
 (213) 966-3511

**CONSCO ENTERPRISES**  
 1180 Ave of the Americas  
 New York NY 10036  
 (212) 575-8084

**CONSOLIDATED ANALYSIS CENTERS INC**

12011 San Vicente Blvd, Suite 350  
Los Angeles CA 90049  
(213) 476-6511

**CONSOLIDATED COMPUTER INC**

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Don Mills, Ontario, M3C 1Z3 Canada  
(416) 449-1120

**CONSTRUCTION COMPUTER CONTROL CORP**

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Milwaukee WI 53202  
(414) 272-6112

**CONTINENTAL ILLINOIS NAT'L BANK/TST**

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Chicago IL 60690  
(312) 828-2345

**CONTROL DATA CORP CORPORATE HDQTRS**

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Minneapolis MN 55440  
(612) 853-8100

**CYBERNET SERVICE DIV**

2401 N Fairview Ave  
St Paul MN 55113  
(612) 633-0371

**MDM COMMUNICATIONS DIV**

3519 W Warner Ave  
Santa Ana CA 92704  
(714) 540-2820

**CONTROL INFORMATION INC**

9575 W Higgins Rd  
Rosemont IL 60018  
(312) 696-1844

**CONTROL LOGIC INC**

9 Tech Circle  
Natick MA 01760  
(617) 655-1170

**CORDELL ENGINEERING INC**

210 Broadway  
Everett MA 02149  
(617) 289-4200

**COSSOR ELECTRONICS LTD**

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Harlow, Essex, England

**COURIER TERMINAL SYSTEMS INC**

2202 E University Dr  
Phoenix AZ 85034  
(602) 244-1392

**COVER-ALL COMPUTER SERVICES LTD**

1468 Victoria Pk Ave  
Toronto 375, Ontario, Canada

**CPC SYSTEMS INC**

PO Box 328  
East Hanover NJ 07936  
(201) 887-9220

**CPT CORP****HDQTRS**

1001 2nd St S  
Hopkins MN 55343  
(612) 935-0381  
E 79th St  
Minneapolis MN 55807  
(612) 854-7101

**CRAMER ELECTRONICS INC**

85 Wells Ave  
Newton MA 02159  
(617) 969-7700

**CRAWFORD AND GRAUER**

10 Surryhill Pl  
Huntington NY 11743  
(516) 368-5051

**CREED & CO LTD**

Hollingbury  
Brighton, Sussex BN1 8AL, England

**C S COMPUTER SYSTEMS INC**

116 John St  
New York NY 10038  
(212) 349-3535

**CTL (See Computer Technology Ltd)****CTM-COMPUTER TECHNIK MULLER GMBH**

775 Konstanz-Litzelstetten  
Komturweg 12, West Germany

**CTRAC INC**

20325 Ctr Ridge Rd  
Rocky River OH 44116  
(216) 333-3475

**CUBIC INDUSTRIAL CORP**

9233 Balboa Ave  
San Diego CA 92138  
(714) 279-7400

**CULLINANE CORP**

Wellesley Office Pk  
20 William St  
Wellesley MA 02181  
(617) 237-6600

**CUMMINS-ALLISON CORP**

800 Waukegan Rd  
Glenview IL 60025  
(312) 724-8000

**CUSTOM PROGRAMMING INC**

W 51st St  
Shaunee Mission KS 66222  
(913) 262-6333

**CUTLER WILLIAMS INC**

2655 Villa Creek Dr  
Dallas TX 75234  
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**CYBERNET TIME-SHARING LTD**

47 Berners St  
London W1, England

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Chicago IL 60606  
(312) 454-1865

**CYPHERNETICS CORP**

175 Jackson Plz  
Ann Arbor MI 48106  
(313) 769-6800

**C3 INC**

11425 Isaac-Newton Sq  
South Reston VA 22090  
(703) 437-0200

**D****DACONICS CORP**

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350 Potrero Ave  
Sunnyvale CA 94086  
(408) 738-4800

**DAKOTA GRAPHICS**

9655 W Colfax Ave  
Lakewood CO 80215  
(303) 237-0408

**DANIEL J. EDELMAN INC**

777 Third Ave  
New York NY 10017  
(212) 557-1020

**DARTEX (See Tally Corp)****DATA 100 CORP****HDQTRS**

7725 Washington Ave S  
Edina MN 55435  
(612) 941-6500

**DATA ACCESS SYSTEMS INC**

100 Rte 46  
Mountain Lakes NJ 07046  
(201) 335-3322

**DATA ARCHITECTS INC**

460 Totten Pond Rd  
Waltham MA 02154  
(617) 890-7730

**DATA CARD CORP**

7625 Parklawn Ave  
Minneapolis MN 55435  
(612) 835-5511

**DATACHRON**

174 Fifth Ave  
New York NY 10010  
(212) 675-5333

**DATACOM**

PO Box 278  
Fort Walton Beach FL 32548  
(904) 244-6121

**DATA COMPUTER INC (See Tally Corp)****DATACROWN LTD**

650 McNicoll Ave  
Willowdale, Ontario, Canada  
(416) 499-1012

**DATA DESIGN ASSOCIATES**

1229 Rousseau Dr  
Sunnyvale CA 94087  
(408) 732-3442

**DATA DISC INC**

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Sunnyvale CA 94086  
(408) 732-7330

**DATA DYNAMICS LTD**

Data House, Springfield Rd  
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**DATA FINANCIAL SYSTEMS INC**

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4350 E Camelback Rd  
Phoenix AZ 85018  
(602) 959-9240

**DATAFLUX CORP**

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Sunnyvale CA 94086  
(408) 732-7070

**DATA FOR MANAGEMENT DECISIONS**

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Richton Park IL 60471  
(312) 784-2900

**DATA GENERAL CORP**

Rte 9  
Southboro MA 01772  
(617) 485-9100

**DATA INPUT INC**

4401 West 76 St  
Minneapolis MN 55423  
(612) 831-6500

**DATA INSTRUMENTS**

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Sepulveda CA 91343  
(213) 893-6464

**DATALINE SYSTEMS LTD**

40 St. Clair Ave W  
Toronto, Ontario, Canada  
(416) 964-9515

**DATALOG****DIV OF LITTON SYSTEMS**

1770 Walt Whitman Rd  
Melville NY 11746  
(516) 694-8300

**DATALOGICS**

University Circle Research Ctr  
11001 Cedar Ave  
Cleveland OH 44106  
(216) 229-1300

**DATA-MAN LTD**

PO Box 9234  
Bow Valley Sq II  
205-5th Ave SW  
Calgary, Alberta T2P 2W4 Canada  
(403) 266-6358

**DATAMARK INC (See Bright Industries)****DATA MEASUREMENTS CORP**

2115 De La Cruz Blvd  
Santa Clara CA 95050  
(408) 249-1111

**DATAMEDIA CORP**

7300 N Crescent Blvd  
Pennsauken NJ 08110  
(609) 665-2382

**DATA NUMERICS INC**

141-A Central Ave  
Farmingdale NY 11735  
(516) 293-6600

**DATA PATHING INC**

370 San Aleso Ave  
Sunnyvale CA 94086  
(408) 734-0100

**DATAPPOINT CORP (FORMERLY COMPUTER TERMINAL CORP)**

8400 Data Point Dr  
San Antonio TX 78229  
(512) 690-7000

**DATA PRINTER CORP**

600 Memorial Dr  
Cambridge MA 02139  
(617) 354-4700

**DATA PROCESSING ENTERPRISES**

914 S Hoover St  
Los Angeles CA 90006  
(213) 380-7200

**DATAPRODUCTS CORP****HDQTRS**

6219 De Soto Ave  
Woodland Hills CA 91364  
(213) 887-8000

**STELMA DIV**

17 Amelia Pl  
Stamford CT 06904  
(203) 325-4161



## Dataram Corp

**DATARAM CORP**

Princeton-Hightstown Rd  
Cranbury NJ 08512  
(609) 799-0071

**DATA RECALL PRODUCTS** (See

Computer Investors Group)

**DATA RESOURCES INC**

29 Hartwell Ave  
Lexington MA 02173  
(617) 861-0165

**DATAROYAL INC**

235 Main Dunstable Rd  
Nashua NH 03060  
(603) 883-4157

**DATASAB SYSTEMS INC**

USA HDQTRS

437 Madison Ave  
New York NY 10022  
(212) 754-0680

**DATA SCIENCES INC**

HDQTRS

1 Indiana Sq, Suite 1755  
Indianapolis IN 46204  
(317) 632-3916

**DATASERV**

770 Airport Blvd  
Burlingame CA 94010  
(415) 342-0877

**DATA SYNECTICS CORP**

41 B St  
Burlington MA 01803  
(617) 273-0220

**DATA SYSTEMS DESIGN INC**

1122 University Ave  
Berkeley CA 94702  
(415) 849-1102

**DATA TECHNOLOGY INC**

4 Gill St  
Woburn MA 01801  
(617) 935-8830

**DATA-TEK CORP**

1211 Chestnut St  
Philadelphia PA 19107  
(215) 564-4133

**DATA TERMINALS & COMMUNICATIONS INC**

1190 Dell Ave  
Campbell CA 95008  
(408) 378-1112

**DATA TERMINAL SYSTEMS INC**

HDQTRS

124 Acton St  
Maynard MA 01754  
(617) 897-3221

**DATATROL INC**

Kane Industrial Dr  
Hudson MA 01749  
(617) 568-1411

**DATA-TRONICS CORP**

310 Towson Ave  
Fort Smith AR 72901  
(501) 785-6331

**DATATYPE**

1050 NW 163rd St  
Miami FL 33169  
(305) 625-8451

**DATA VIEW INC**

PO Box 537  
Mexomonee Falls WI 53051  
(414) 255-3200

**DATENFERN VERARBEITUNG MBH**

(See Gesellschaft Fur Datenfern Verarbeitung MBH)

**DATUM INC**

1363 S State College Blvd  
Anaheim CA 92806  
(714) 533-6333

**DEARBORN COMPUTER LEASING CORP**

4849 N Scott St, Suite 401  
Schiller Park IL 60176  
(312) 671-4410

**DEC** (See Digital Equipment Corp)**DECISION CONCEPTS INC**

280 Park Ave  
New York NY 10017  
(212) 752-1000

**DECISION DATA COMPUTER CORP**

100 Witmer Rd  
Horsham PA 19044  
(215) 674-3300

**DECISION INC**

5601 College Ave  
Oakland CA 94618  
(415) 654-8626

**DECISION STRATEGY CORP**

708 Third Ave  
New York NY 10017  
(212) 687-2660

**DECITEK**

DIV OF JAMESBURY CORP

250 Chandler St  
Worcester MA 01602  
(617) 798-8731

**DELTA DATA SYSTEMS**

Woodhaven Industrial Pk  
Cornwells Heights PA 19020  
(215) 639-9400

**DESIGN AUTOMATION CORP**

809 Massachusetts Ave  
Lexington MA 02173  
(617) 862-8988

**DESIGN ELEMENTS INC** (See M12 Data Systems)**DESK TOP COMPUTER** (See Eugene

Dietzgen Co)

**DEST DATA CORP**

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(408) 734-1234

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Marlton NJ 08053  
(609) 983-3353

**DIABLO SYSTEMS INC**

26460 Corporate Ave  
Hayward CA 94545  
(415) 786-5000

**DIALCOM INC**

1104 Spring St  
Silver Spring MD 20910  
(301) 588-1572

**DI/AN CONTROLS INC**

944 Dorchester Ave  
Boston MA 02125  
(617) 288-7700

**DICK CO. A. B.**

5700 W Touhy Ave  
Chicago IL 60648  
(312) 775-7766

**DICOM INDUSTRIES**

715 N Pastoria Ave  
Sunnyvale CA 94086  
(408) 732-1060

**DICTAPHONE CORP**

120 Old Post Rd  
Rye NY 10580  
(914) 967-7300

**DIEBOLD INC**

818 Mulberry Rd  
Canton OH 44702  
(216) 453-4592

**DIETZ & CO** (See Heinrich Dietz Industrie-Elektronik)**DIETZGEN CO EUGENE** (See Eugene

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**DIGI-DATA CORP**

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Jessup MD 20794  
(301) 498-0200

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Babylon Rd  
Horsham PA 19044  
(215) 672-0800

**DIGITAL COMPUTER CONTROLS**

12 Industrial Rd  
Fairfield NJ 07006  
(201) 575-9100

**DIGITAL EQUIPMENT CORP**

HDQTRS

146 Main St, Bldg PK3-1  
Maynard MA 01754  
(617) 897-5111

COMPONENTS GROUP

1 Iron Way  
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(617) 481-7400

**DIGITAL LABORATORIES**

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(617) 876-6220

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(714) 453-6050

**DIGITAL SOLUTIONS INC**

100 Menlo Pk  
Edison NJ 08817  
(201) 549-1700

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Novato CA 94947  
(415) 883-5981

**DIGITECH DATA INDUSTRIES INC**

HDQTRS

66 Grove St  
Ridgefield CT 06877  
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**DIGITEK CORP**

15303 S Broadway  
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(213) 327-5410

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LOGISTICS

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(609) 667-6233

**DIVA INC**

607 Industrial Way W  
Eatontown NJ 07724  
(201) 544-9000

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PO Box 8922  
Greensboro NC 27410  
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**DIVERSIFIED COMPUTER**

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(415) 324-2523

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(602) 792-3250

**DNA SYSTEMS INC**

1258 S Washington  
Saginaw MI 48601  
(517) 793-0185

**DOCUMATION INC**

PO Box 1240  
Melbourne FL 32901  
(305) 724-1111

**DOCUMENTOR SCIENCES CORP**

2921 S Daimler St  
Santa Ana CA 92705  
(714) 836-8608

**DOCUTEL CORP**

2615 E Grauwylar Rd  
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(214) 438-1818

**DRESSER SYSTEMS INC**

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Houston TX 77001  
(713) 784-6011

**D.R. MCCORD ASSOCIATES INC**

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Dallas TX 75207  
(214) 630-2670

**DUKANE CORP**

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St. Charles IL 60174  
(312) 584-2300

**DUQUESNE SYSTEMS INC**

355 5th Ave  
Pittsburgh PA 15222  
(412) 281-9055

**DYMAT PHOTOMATRIX CORP**

2225 Colorado Ave  
Santa Monica CA 90404  
(213) 828-9585

**DYMO GRAPHIC SYSTEMS INC**

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6631 E Kellogg, Suite 214  
Wichita KS 67207  
(316) 265-5277

**N****N.A. PHILIPS (See North American Philips Corp)****NATIONAL CASH REGISTER CO (See NCR)****NATIONAL COMPUTER ANALYSTS INC**

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Princeton NJ 08540  
(609) 452-2800

**NATIONAL COMPUTER NETWORK OF CHICAGO**

1929 N Harlem Ave  
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(312) 622-6666

**NATIONAL COMPUTER PRODUCTS INC**

Chesapeake Ave  
Towson MD 21204  
(301) 823-2248

**NATIONAL COMPUTER SYSTEMS**

4401 W 76th St  
Minneapolis MN 55435  
(612) 831-4100

**NATIONAL COMPUTING INDUSTRIES**

8075 Roswell Rd NE  
Atlanta GA 30328  
(404) 252-9479

**NATIONAL CSS INC**

300 Westport Ave  
Norwalk CT 06851  
(203) 853-7200

**NATIONAL MICRONETICS**

PACIFIC DIV  
5600 Kearney Mesa Rd  
San Diego CA 92111  
(714) 279-7500

**NATIONAL SEMICONDUCTOR CORP**

2900 Semiconductor Dr  
Santa Clara CA 95051  
(408) 732-5000

**NCB COMPUTER POWER**

Cannock, Staffs, England

**NCR****WORLDWIDE HDQTRS**

Main & K Sts  
Dayton OH 45409  
(513) 449-2000

**NETWORK DATA PROCESSING CORP**

321 Third St SE  
Cedar Rapids IA 52403  
(319) 365-8691

**NEW ENGLAND TELEPHONE & TELEGRAPH**

Franklin St  
Boston MA 02109  
(617) 227-9950

**NEW MAX**

720 Old Willits Pass  
Hauppauge NY 11787  
(516) 582-3311

**NEW YORK CITY DATA CENTER (See Burroughs Corp)****NICHOLS & COMPANY**

1888 Century Park E  
Los Angeles CA 90067  
(213) 556-2757

**NIHON ICL MACHINERY CO LTD**

102 Kyomachibori 5-Chome  
Nishi-Ku, Osaka 550, Japan

**NIPPON COLUMBIA CORP OF AMERICA**

6 E 43rd St  
New York NY 10017  
(212) 682-5060

**NIPPON ELECTRIC CO**

5-33-1 Shiba Minato-Ku  
Tokyo, Japan  
454-1111

**AMERICAN I L C HEAD OFFICE**

Pan Am Bldg  
200 Park Ave, Suite 4321  
New York NY 10017  
(212) 758-1666

**NIPPON TIME SHARE CO LTD**

17th Mgr Bldg  
2, Sakuragawa-Cho, Shiba Nishikubo  
Minatoku, Tokyo, Japan  
(03) 562-0551

**NIXDORF COMPUTER AG****USA HDQTRS**

O'Hare Plz Mall  
5725 E River Rd  
Chicago IL 60631  
(312) 693-6600

**WORLD HDQTRS**

4790 Paderborn, West Germany  
Fuerstenweg  
(05251) 2001

**NOLLER CONTROL SYSTEMS (See Badger Meter Inc)****NORAND CORP**

550 Second St SE  
Cedar Rapids IA 52401  
(319) 366-7611

**NORD (See A/S Norsk Data-Elektronikk)****NORELCO**



## North American Philips Corp

**NORTH AMERICAN PHILIPS CORP***(Also See Philips Business Systems Inc)***EXECUTIVE OFFICES**

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(212) 697-3600

**NORTH AMERICAN PHILIPS CORP DIV**

91 McKee Dr, Box C  
Mahwah NJ 07430  
(201) 529-3800

**NORTHEASTERN SYS ASSOCIATES***INC (See Mark/Ops)***NORTH ELECTRIC CO**

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Galion OH 44833  
(419) 468-8100

**NORTHERN ELECTRIC CO LTD**

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Boston MA 02110  
(617) 482-0995

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Beaver St  
New York NY 10011  
(212) 269-7124

**NORTHWEST MANAGEMENT SERVICES**

2300 Eastlake Ave E  
Seattle WA 98102  
(206) 329-9990

**NOVATION INC**

18664 Oxnard St  
Tarzana CA 91356  
(213) 996-5060

**NUCLEAR DATA INC**

Golf & Meacham Rds  
Schaumburg IL 60172  
(312) 884-3600

**NUMERI/COMP**

1330 E State St  
Rockford IL 61108  
(815) 963-2435

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Utrecht, Netherlands

**IG OFFICE MACHINES**

Bldg 'Hertoghof' HSM  
Eindhoven, Netherlands  
(040) 79 1111

**NV PHILIPS-ELECTROLOGICA BV****WORLD MARKETING****GENERAL SYSTEMS**

Bldg HSM Hertoghof  
Eindhoven, Netherlands  
040-755024

**NV PHILIPS ELECTROLOGICA****NEDERLAND****TIME SHARING DIV**

Mariahove, De Horst 4  
The Hague, Netherlands

**NV PHILIPS****GLOEILAMPENFABRIEKEN****HDQTRS**

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2 Rue Hippolyte-Lebas  
Paris 9E, France

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North Hollywood CA 91602  
(213) 763-5144

**OCÉ INDUSTRIES INC****HDQTRS**

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Chicago IL 60645  
(312) 338-1700

**ODEC COMPUTER SYSTEMS**

25 Graystone St  
Warwick RI 02886  
(401) 738-9500

**OHIO VALLEY DATA CONTROL INC**

2505 Washington Blvd  
Belpre OH 45714  
(614) 423-9501

**OKIDATA CORP**

111 Garther Dr  
Moorestown NJ 08057  
(609) 235-2800

**OKI ELECTRIC INDUSTRY CO LTD**

10 Shiba Kotohira-Cho  
Mimami-Ku, Tokyo 105, Japan

**OKI ELECTRONICS INC**

500 SE 24th St  
Fort Lauderdale FL 33316  
(305) 563-6234

**OLD STONE BANK COMPUTER CENTER**

443 Jefferson Blvd  
Warwick RI 02886  
(401) 274-7800

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New York NY 10022  
(212) 371-5500

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500 Park Ave  
New York NY 10022  
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Frankfurt am Main  
West Germany

**OLYMPIA USA INC**

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Somerville NJ 08876  
(201) 722-7000

**OMEGA-T SYSTEMS INC**

300 Terrace Village  
Richardson TX 75080  
(214) 231-9303

**OMNIS CORP**

500 S Ervay  
Dallas TX 75201  
(214) 651-0201

**OMNITEC CORP**

2405 S 20th St  
Phoenix AZ 85034  
(602) 258-8244

**OMRON SYSTEMS INC**

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(408) 734-8400

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115 Evergreen Heights Dr  
Pittsburgh PA 15229  
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**ONTEL CORP**

3 Fairchild Ct  
Plainview NY 11803  
(516) 822-7800

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1928 Isaac Newton Sq W  
Reston VA 22090  
(703) 471-5060

**OPTICAL SCANNING CORP**

Newtown Industrial Commons  
Newtown PA 18940  
(215) 968-4611

**ORBIS SYSTEMS INC**

Franklin St  
Tustin CA 92680  
(714) 838-1491

**ORBITAL SYSTEMS INC**

Church & Fellowship Rds  
Moorestown NJ 08057  
(609) 234-1700

**ORDO (See Societe des Ordoprocresseurs)****OXFORD SOFTWARE CORP**

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(201) 944-0083

**P****PACE APPLIED TECHNOLOGY**

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Arlington VA 22209  
(703) 573-9131

**PACIFIC INTERNATIONAL COMPUTING CORP**

50 Beale St  
San Francisco CA 94105  
(415) 764-9990

**PACIFIC PLANTRONICS**

111C Josephine St  
Santa Cruz CA 95080  
(408) 426-5858

**PACIFIC STOCK EXCHANGE**

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San Francisco CA 94104  
(415) 392-6533

**PANSOPHC SYSTEMS INC**

709 Enterprise Dr  
Oak Brook IL 60521  
(312) 886-6000

**PARADYNE CORP**

8550 Ulmerton Rd  
Largo FL 33540  
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**PENRIL DATA COMMUNICATIONS INC**

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120 N Center St  
Bloomington IL 61701  
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**PEOPLES TRUST BANK**

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Fort Wayne IN 46820  
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237 W Tuscarawas St  
Canton OH 44702  
(216) 455-6741

**PERIPHERAL BUSINESS****EQUIPMENT INC (See Pertec Business Systems)****PERIPHERAL DYNAMICS INC**

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(215) 539-5500

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1724 Marlton Pike E  
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(609) 474-2008

**PERIPHERAL TECHNOLOGY INC (See Pertec Business Systems)****PERIPHERY INC (See Computer Link Corp)****PERIPHONICS CORP**

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Bohemia NY 11716  
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Santa Ana CA 92705  
(714) 540-8340

**PERTEC CORP**

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(213) 882-0030

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Willow Grove PA 19090  
(215) 659-7700

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(Also See North American Philips Corp)  
175 Froehlich Farms Blvd  
Woodbury NY 11797  
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Raleigh NC 27605  
(919) 828-6831

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Commerce Pk  
Danbury CT 06810  
(203) 792-1600

**PITTSBURGH NATIONAL BANK**  
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Pittsburgh PA 15230  
(412) 355-2000

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Santa Clara CA 95050  
(408) 249-1160

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Hillside NJ 07205  
(201) 628-0050

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AUTOMATION GROUP  
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London N7, England  
COMMUNICATIONS SYSTEMS DIV  
9 Dallington St  
London EC1V 0JO, England

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170 Finn Ct  
Farmingdale NY 11735  
(516) 694-7900

**PLESSEY MICROSYSTEMS**  
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Irvine CA 92714  
(714) 540-9945

**PLESSEY TELECOMMUNICATIONS DATA SYSTEMS**  
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Poole, Dorset BH177ER England  
(02013) 5161

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**POTTER INSTRUMENT CO INC**  
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(516) 681-3200

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Rutherford NJ 07070  
(201) 933-1650

**PRC COMPUTER CENTER INC**  
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McLean VA 22101  
(703) 893-4880

**PRECISION INSTRUMENT CO**  
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Santa Clara CA 95051  
(408) 249-5801

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Palo Alto CA 93403  
(415) 494-7225

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145 Pennsylvania Ave  
Framingham MA 01701  
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**PRINCETON ELECTRONIC PRODUCTS INC**  
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(201) 297-4448

**PRINCETON MICROFILM CORP**  
Alexander Rd  
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(609) 452-2066

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Sixth Rd  
Woburn MA 01801  
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(206) 885-4171

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(617) 661-3020

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**PROGRAM PRODUCTS INC**  
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Montvale NJ 07645  
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Burlington MA 01803  
(617) 272-7723

**PROGRESSIVE SYSTEMS**  
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(408) 372-4593

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75 Paris 8E, France

**PROPRIETARY COMPUTER SYSTEMS INC**  
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Falls Church VA 22041  
(703) 820-0657

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**R**

**RAIR INC**  
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**R2E MICRAL MICROCOMPUTERS**  
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**RANDOLPH COMPUTER CO**  
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**RATH & STRONG**  
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**RAYTHEON-COSSOR**  
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Harlow, Essex CM19 5 BB England  
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**RAYTHEON DATA SYSTEMS CO**  
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**RC** (See Regnecentralen Scandinavian)  
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(201) 722-3200

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Building 203-3  
Dept 1614  
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(609) 963-8000

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**REGMA**  
Société La Cellophane  
110 Blvd Haussman  
75360 Paris Cedix 08, France

**REGNECENTRALEN**  
SCANDINAVIAN INFO PROCESSING  
SYSTEM  
Hovedvejen 9  
DK-2600 Gloustrup, Denmark

**REI** (See Recognition Equipment Corp)  
**RELIABLE COMMUNICATIONS**  
PRODUCTS  
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Franklin Park IL 60131  
(312) 455-8520

**REMCOM SYSTEMS INC** (See CMC  
Remcom Inc)

**REMEX**  
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Santa Ana CA 92705  
(714) 557-8860

**REMINGTON RAND OFFICE**  
SYSTEMS (See Sperry Rand Corp)

**REMOTE DATA TERMINALS INC**  
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2928 Nebraska Ave  
Santa Monica CA 90404  
(213) 829-2611

**REPCO INC**  
1940 Lockwood Way  
Orlando FL 32804  
(305) 843-8484

**RESEARCH INC**  
Box 24064  
Minneapolis MN 55424  
(612) 941-3300

**REYNOLDS & REYNOLDS CO**  
800 Germantown St  
Dayton OH 45401  
(513) 226-0808

**RFL INDUSTRIES INC**  
COMMUNICATIONS DIV  
Powerville Rd  
Boonton NJ 07005  
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**RICOH CO LTD**  
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Ota-Ku  
Tokyo 143, Japan

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2120 Industrial Pkwy  
Silver Springs MD 20904  
(301) 622-2121

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COMPUTER SERVICES  
PO Box 455  
Harrisonburg VA 22801  
(703) 434-1331

**ROCKWELL INTERNATIONAL**  
INFORMATION SYSTEMS DEPT  
PO Box 2515  
2201 Seal Beach Blvd  
Seal Beach CA 90740  
(213) 594-3311

**MICRO-ELECTRONICS DEVICES DIV**  
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Anaheim CA 92803  
(714) 632-8111

**SPACE DIV**  
12214 Lakewood Blvd  
Downey CA 90241  
(213) 922-2111

**ROLM CORP**  
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Cupertino CA 95014  
(408) 257-6440

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150 New Park Ave  
Hartford CT 06106  
(203) 523-4881

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CH-8040 Zurich  
Badenerstrasse 595  
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**RXDS** (See Rank-Xerox Ltd)

**S**

**SAAB-SCANIA AB**  
EUROPEAN HDQTRS  
DATASAAB DIV  
S-581 88 Linköping, Sweden  
013-11 15 00

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**SAGEM** (See Societe d' Applications  
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Nashua NH 03060  
(603) 885-4321

**SANGAMO ELECTRIC CO**  
PO Box 359  
Springfield IL 62075  
(217) 544-6411

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400 Columbus  
Valhalla NY 10595  
(914) 769-9500

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Norristown PA 19401  
(215) 277-0500

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100 Prestige Pk  
East Hartford CT 06108  
(203) 289-6001

**SCICON** (See Scientific Control System Ltd)  
**SCIENCE ACCESSORIES CORP**

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Southport CT 06490  
(203) 255-1526

**SCIENTIFIC CONTROL SYSTEMS**  
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520 Clyde Ave  
Mountain View CA 94043  
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**SCIENTIFIC SYSTEMS TECH**  
3530 Forest La  
Dallas TX 75234  
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**SCM CORP**  
299 Park Ave  
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(212) 752-2700

**SCM CORP**  
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Lake-Cook Rd  
Deerfield IL 60015  
(312) 945-1000

**SCOPE DATA INC**  
3728 Silver Star Rd  
Orlando FL 32808  
(305) 298-0500

**SCORPIO DATA SYSTEMS INC**  
445 Sadde River Rd  
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(914) 356-8089

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PO Box 391  
Holyoke MA 01040  
(413) 536-7800

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437 Madison Ave  
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(212) 758-2058

**SDSI PERIPHERALS AG**  
US OPERATIONS DIV  
PO Box 77  
Wyckoff NJ 07481  
(201) 447-5321

**SEACO COMPUTER-DISPLAY INC**  
2714 National Circle  
Garland TX 75040  
(214) 276-1153

**SECRE** (See Societe d'Etudes de Constructions  
et de Recherches en Electronique)

**SEIN** (See Societe d'Electronique Industrielle  
ete Nucleaire)

**SEL** (See Systems Engineering Laboratories)

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COMPUTER PERIPHERALS GROUP  
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Audubon Rd  
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**SELENIA** (See Industrie Electroniche  
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**SEQUENTIAL INFORMATION**  
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249 N Saw Mill River Rd  
Elmsford NY 10523  
(914) 592-5930

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(812) 423-1133

**SHARED COMPUTER SYSTEMS**  
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Miami FL 33132  
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**SHARED MEDICAL SYSTEMS**  
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King of Prussia PA 19406  
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**SHINTRON CO INC**  
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(617) 491-8700

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FACHBEREICH DATENTECHNIK  
8000 Munich 70, West Germany  
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Postfach 700072  
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**SIERRA RESEARCH CORP**  
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Bethesda MD 20014  
(301) 881-4451

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(404) 458-0286

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(408) 739-7700

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Elkhart IN 36514  
(219) 294-6621

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**SMI INC**

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St. Louis MO 63123  
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**SOCIETE D'APPLICATIONS  
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MECANIQUE**

PO Box 445  
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Derry NH 03038  
(603) 432-2013

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94 Alfortville, France

**SOCIETE DES ORDOPROCESSEURS**

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AUTOMATIQUE DE DONNES  
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11 Rue de la Vistule  
75013 Paris, France  
Paris 707-3719 or 589-0903

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RECHERCHES EN  
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75 Paris 10 eme, France

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NOUVELLES TECHNIQUES  
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**SOFTWARE DEVELOPMENT/  
CANADA**

PO Box 32  
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(416) 485-7715

**SOFTWARE ENGINEERING**

1945 Pauline, Suite 16  
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(617) 475-5040

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(714) 752-8455

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Rochester NY 14603  
(716) 482-2200

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San Diego CA 92138  
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Ottawa 8, Ontario, Canada  
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**SYSTEMS ENGINEERING LABORATORIES**  
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Santa Ana CA 92707  
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(408) 255-4800

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Lexington MA 02173  
(617) 862-6035

**TECHNICAL ECONOMICS INC**  
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Berkeley CA 94707  
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PO Box 9033  
Berkeley CA 91709  
(415) 525-7774

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Los Angeles CA 90064  
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Beaverton OR 97005  
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Miami Beach FL 33169  
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**TELECOMMUNICATIONS RADIOELECTRIQUES ET TELEPHONIQUES**  
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75640 Paris Cedex 13  
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(312) 694-3590

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**TELEFUNKEN COMPUTER GMBH FACHBEREICH INFORMATIONSTECHNIK**  
775 Konstanz BW, West Germany  
Bucklestrasse 1-5

**TELEGEST**  
68 Rue Jouffroy  
75017 Paris, France

**TELEMECANIQUE SA**  
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33 Avenue de Chatou  
92 Rueil, France  
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(202) 785-8444

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**TRIUMPH-ADLER AG**

85 Nurnberg  
Fuerther Strasse 212  
West Germany  
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BP 34  
92360 Meudon-La-Forêt, France  
630 23 80

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**DIVISION OF VIDAR**

77 Ortega Ave  
Mountain View CA 94040  
(415) 961-1150

**VOGUE INSTRUMENT CORP**

131st St & Jamaica Ave  
Richmond Hill NY 11418  
(212) 641-8800

**VORIAN ASSOCIATES OF CANADA LTD**

45 River Dr  
Georgetown, Ontario, Canada  
(416) 457-4130

**VYDEC INC**

9 Vreeland Rd  
Florham Park NJ 07932  
(201) 822-2100

**W**

**WANGCO INC**

5404 Jandy Pl  
Los Angeles CA 90066  
(213) 390-8081

**WANG COMPUTER SERVICES**

836 North St  
Tewksbury MA 01876  
(617) 851-4111

**WANG LABORATORIES INC**

836 North St  
Tewksbury MA 01876  
(617) 851-4111

**WARNER & SWASEY CO (COMSTAR)**

30300 Solon Industrial Pkwy  
Solon OH 44139  
(216) 368-6200

**WARRINGTON ASSOCIATES INC**

5600 Lincoln Dr  
Minneapolis MN 55435  
(612) 935-3300

**WAVETEK DATA COMMUNICATIONS HDQTRS**

9045 Balboa Ave  
San Diego CA 92123  
(714) 279-2200

**WEILAND COMPUTER GROUP INC, THE**

814 Commerce Dr, Suite 101  
Oak Brook IL 60521  
(312) 325-9300

**WESTCOM INC**

501 Rogers St  
Downers Grove IL 60515  
(312) 971-2010

**WESTERN DATA SCIENCES INC**

5055 N 12th St  
Phoenix AZ 85014  
(602) 264-2630

**WESTERN DIGITAL CORP**

19242 Red Hill  
Newport Beach CA 95051  
(714) 557-3550

**WESTERN SYSTEMS CO (See Informatics Inc)**

**WESTERN TELEMATICS INC TELEPROCESSING DIV**

Bldg 5-107  
3001 Red Hill Ave  
Costa Mesa CA 92626  
(714) 979-0363

**WESTERN UNION DATA SERVICES**

90 McKee Dr  
Mahwah NJ 07430  
(201) 529-6000

**WESTINGHOUSE CANADA, LTD**

Box 510  
Hamilton, Ontario, Canada

**WESTINGHOUSE ELECTRIC CORP**

COMPUTER & INSTRUMENT DIV  
2040 Ardmore Blvd  
Pittsburgh PA 15221  
(412) 256-5583

**WHELOCK SIGNALS INC**

273 Branchport Ave  
Long Branch NJ 07740  
(201) 222-6880

**WILLIAM D. WITTER INC**

1 Battery Park Pl  
New York NY 10004  
(212) 483-0000

**WILLMORE ACCOUNTING & TAX SERVICE**

2624 Chestnut St  
Columbus IN 47201  
(812) 372-3217

**WILTEK INC**

Glover Ave  
Norwalk CT 06850  
(203) 853-7400

**WINTEK CORP**

902 N 9th St  
Lafayette IN 47904  
(317) 742-6802

**WITTER, WILLIAM D. INC (See William D. Witter Inc)**

**WOLF RESEARCH AND DEVELOPMENT CORP**

6801 Kenilworth Ave  
Riverdale MD 20840  
(301) 779-2800

**WORLD WIDE TIME SHARING INC**

(See Reynolds & Reynolds)

**WRIGHT CORP, BARRY (See Barry Wright Corp)**

**WYLE COMPUTER PRODUCTS**

128 Maryland St  
El Segundo CA 90245  
(213) 322-1763

**WYLY CORP (FORMERLY UNIVERSITY COMPUTING COMPANY)**

1500 Ucc Tower, Box 6228  
Dallas TX 75222  
(214) 637-5181

**X**

**XEBEC SYSTEMS INC**

566 San Xavier Ave  
Sunnyvale CA 94086  
(408) 732-9444

**XEROX COMPUTER SERVICES (See Xerox Corp)**

**XEROX CORP COMPUTERS, ADMINISTRATION & ENGINEERING DIV**

701 S Aviation Blvd  
El Segundo CA 90245  
(213) 679-4511

**COMPUTER SERVICES DIV**

5310 Beethoven St  
Los Angeles CA 90066  
(213) 390-3461

**HDQTRS**

Xerox Sq  
Rochester NY 14644  
(716) 423-9200

**OFFICE SYSTEMS DIV**

1341 W Mockingbird La  
Dallas TX 75247  
(214) 630-2611

**Y**

**YASUKAWA ELECTRIC MFG CO LTD**

(Yasukawa Denki Seisakusho)  
Otamachi Bldg  
6-1 Otamachi  
1-Chome, Chiyoda-Ku  
Tokyo, Japan



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**Z**

**ZENTEC CORP**  
2368-C Walsh Ave  
Santa Clara CA 95050  
(408) 246-7662

**ZETA RESEARCH**  
1043 Stuart St  
Lafayette CA 94549  
(415) 284-5200

**ZUSE KG**  
Grosse Industrie Strasse 19-21-D  
Bad Hersfeld, West Germany



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