A PENNWELL PUBLICATION JUNE 1992

COMPUTER DESIGN

Technology and Design Directions

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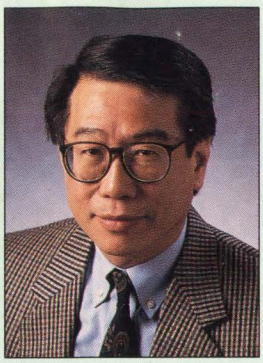
FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



Lattice's Cyrus Y. Tsui on:
Programmable logic

PC-based CAE/CAD: any task, anywhere, anytime

Graphics ICs target Windows acceleration

Peripheral interfaces offer fast networking solutions

Don't miss SBus News in this issue

06
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MAYBE YOU JUST NEED BETTER DRIVERS.

Stuck in a SCSI data-transfer bottleneck?

A first-class SCSI-2 VME board *could* get you out of that jam... *if* getting that board up and running doesn't leave your whole engineering team in gridlock.

That's why, when you buy a Rimfire SCSI-2 VME board from Ciprico, you don't just get a product. You get a partner.

As your partner, we'll help you write the drivers you need, and provide on-site installation. We'll even work with your engineering team to customize hardware or software for your special application needs.

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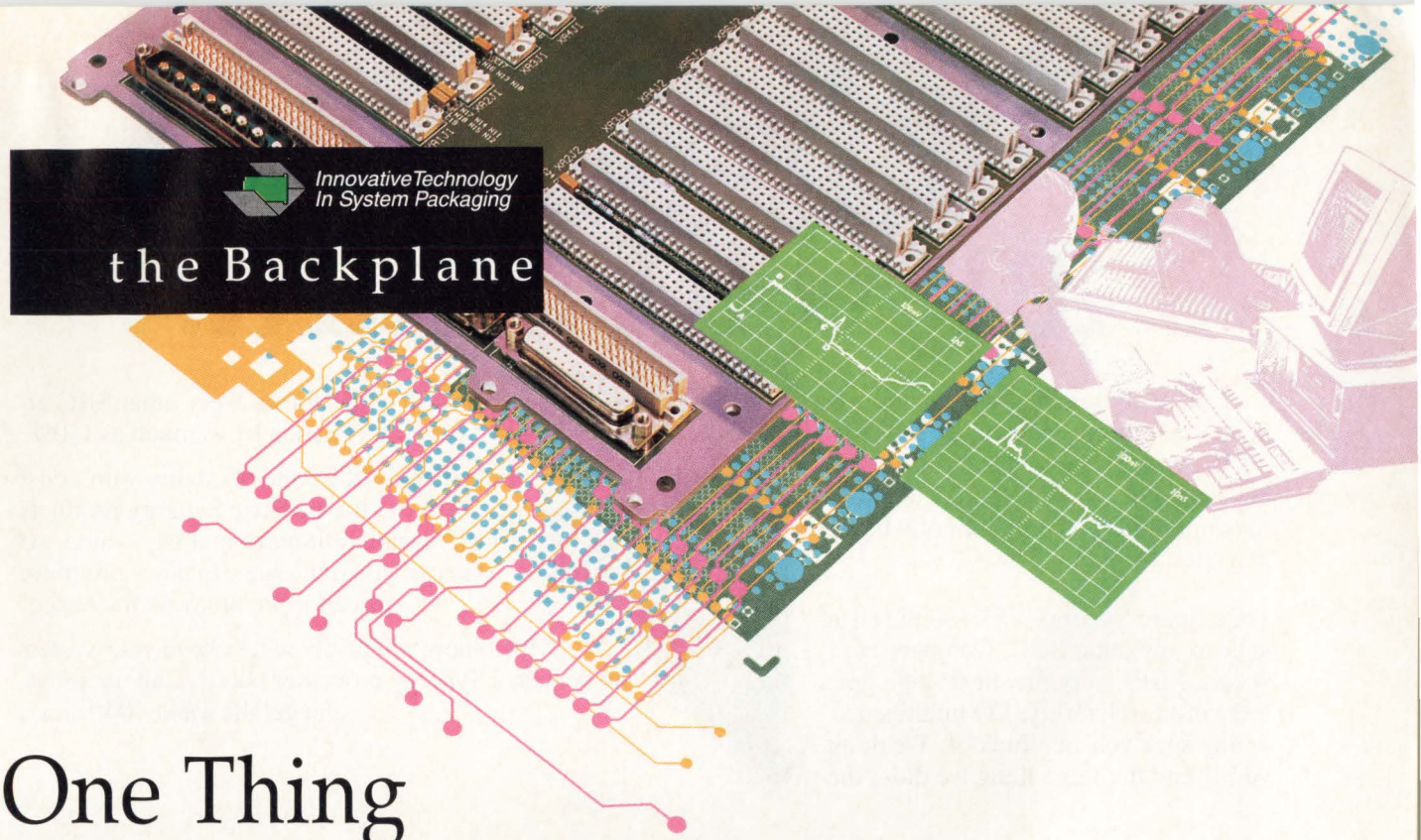
CIRCLE NO. 1

CIPRICO



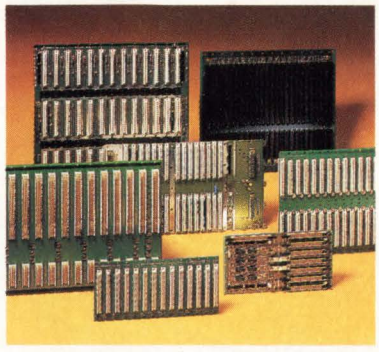
One Thing Separates a Great Backplane from a Good One.

It's the innovative application of cutting-edge technology to your specific requirements. It's what we do at Electronic Solutions.

There was a time when a backplane was little more than a few connectors mounted to a simple pc board. But today's higher performance systems require higher performance multilayer backplanes. Someone has to resolve the difficult issues faced in designing a backplane that will handle your high-speed system—a balancing act between design parameters that affect crosstalk, reflections, impedance, ground shift, and power distribution.

That's where Electronic Solutions can make your job easier! You can rely on our experience and expertise to resolve the design issues you're facing quickly—at a price that even your bean counters will be pleased with.

For industry standard backplanes such as VME, Multibus I or II, Sun, VXI, or Futurebus+ we have a line of high performance backplanes available off the shelf. Our backplanes have been independently tested and ranked as the "Best Balanced" backplanes available.



VMEbus
VXI bus
Sun bus
Multibus I
Multibus II
Futurebus+
Mixed buses
Proprietary buses

For proprietary backplanes, no matter how exotic or unusual, we'll apply the same design expertise exemplified by our standard products and build you a backplane tailored to your specific requirements.

Let us prove it to you! Just call and request information on our backplane design capabilities and we'll FAX the FACTS right to you. Or ask to talk to one of our Applications Engineers who will help you translate your requirements into a backplane spec.

For standard or proprietary applications, there's only one way to get a backplane that's just right for your system. That's to call Electronic Solutions and put our experience to work for you.

One example of our design innovation is our patented **Active Automatic Daisy Chaining** which eliminates the number one field service probem— improperly placed Bus Grant Jumpers. It's superior to the passive auto-daisy chaining touted by other vendors, and it's available *free of charge* on our new VME backplanes.

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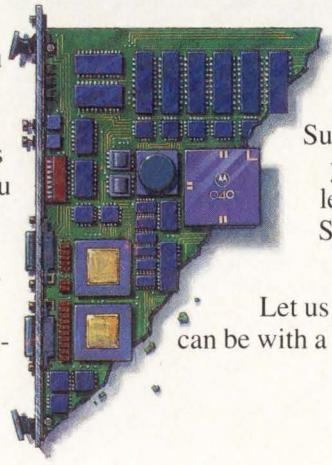
CIRCLE NO. 2

Why Settle for ½ an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

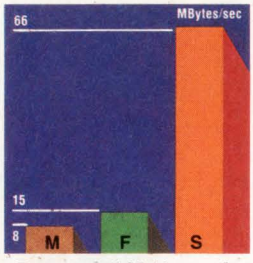
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.



Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

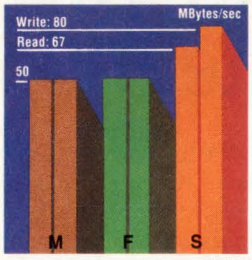
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



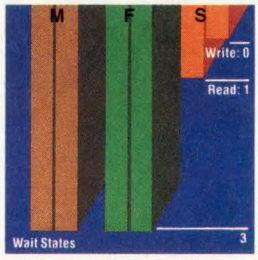
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



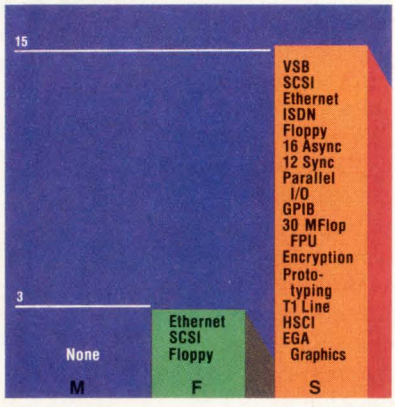
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



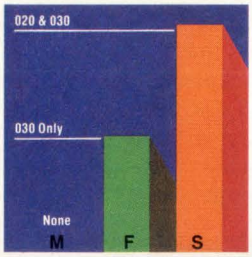
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



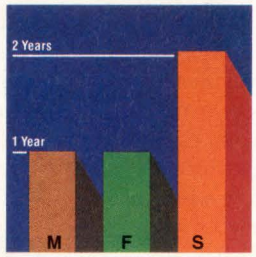
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



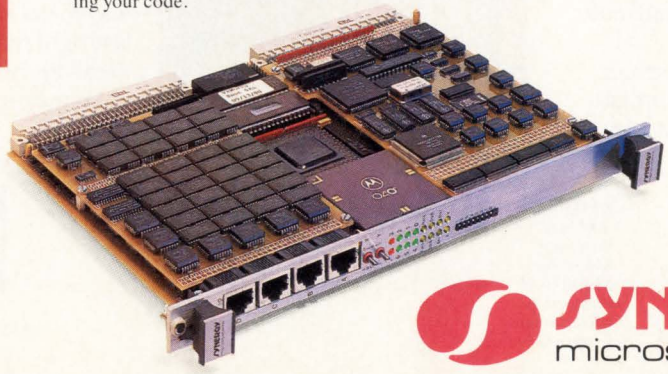
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 **(619) 753-2191** FAX: 619-753-0903

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CIRCLE NO. 3

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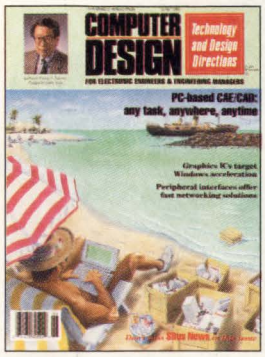
Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



This month's cover story discusses the many PC-based CAE/CAD systems available to engineers. Can you pick out the phoney software in our vacationing designer's baggage? **83**

Illustration by Mike Gardner

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High-performance network interfaces

Benchmarking digital and mixed-signal simulators

Software testing

Logic analyzers

NEWS BRIEFS

Price cuts up the ante in programmable market . . . Hardware emulation pioneer Quickturn sues PiE . . . New Sparcs in a new Sun . . . Teradyne looks to shrink EDA product line . . . CFI puts its standards to the test . . . Turf tiff threatens IBM/Siemens DRAM deal . . . X Windows, NFS come to embedded systems . . . Second helpings . . . FDDI — killed at the starting gate? **10**

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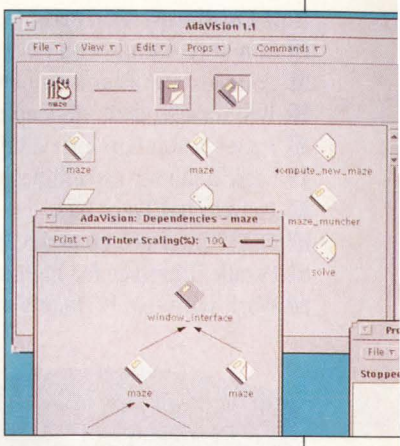

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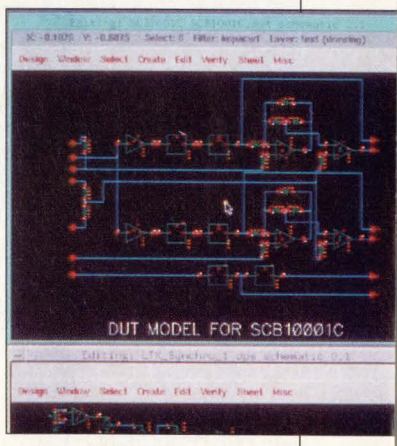

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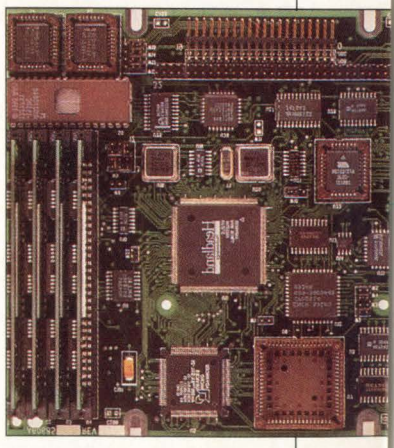

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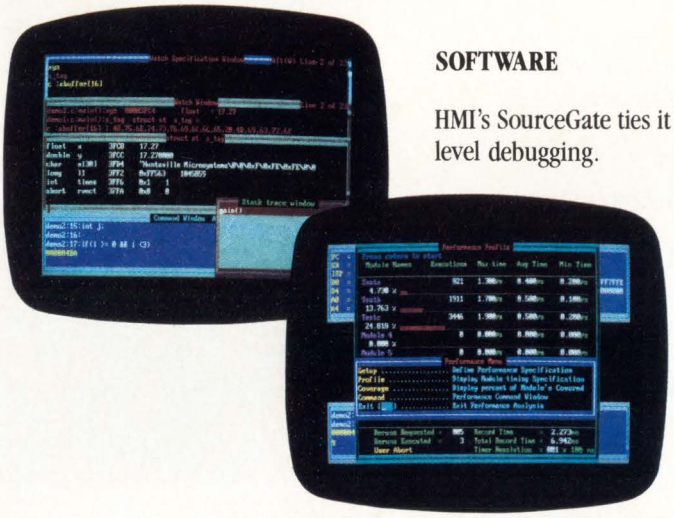
HMI development systems do it all!

HMI provides complete development systems—in-circuit emulator, window driven source level debugger and software performance analyzer—that address all aspects of the microprocessor system design cycle, from prototype to production:

HMI Emulators Feature:

- Run at real-time with no wait states.
- Complex events and sequences for break and trigger conditions.
- Two independent 4K deep trace buffers.
- 1 μsec resolution interval timer.
- Logic analyzer capabilities built into the emulator.
- 16 External Trace bits.
- RS232 Interface up to 115.2K.
- Parallel Interface for high-speed downloading.
- Work with IBM PC family and UNIX based machines including SUN and Apollo.

EMULATORS



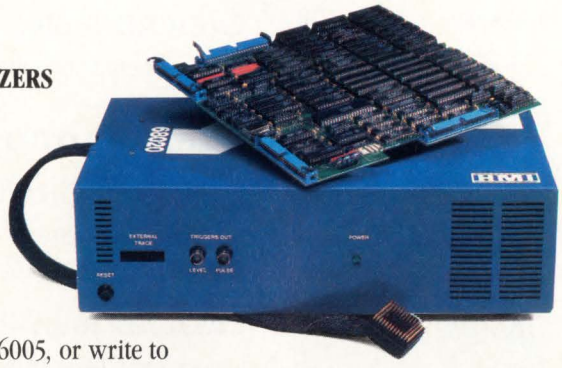
SOFTWARE

HMI's SourceGate ties it all together, so emulator features aren't sacrificed to gain source-level debugging.

HMI SourceGate® Features:

- Custom window configuration determined by user.
- Support for major C, PL/M, Pascal and ADA compilers.
- Source code in the trace buffers.
- C variable tracking.

ANALYZERS



Add our Performance Analysis Card to complete your development package.

Performance Analysis Features:

- Real-time hardware implemented software performance analyzer.
- 100 nsec resolution time-stamp in trace buffer.
- Setup trigger conditions to start and stop analysis.
- View covered and not covered pieces of code.

If you are looking for one development system that does it all, call (205) 881-6005, or write to Huntsville Microsystems Inc., 3322 South Memorial Parkway, Huntsville, AL 35801. Ask for *free* demo disk.

AVAILABLE EMULATORS

68000	68330/333	68HC001
68008	68331/332	8051 Family
68010	68340	DS5000
68020	6809/6809E	8096/80196 Family
68030	68EC020	8085
68302	68EC030	64180/Z180
68301/303	68HC11 including F1 and D3	Z80
		68HC16 Family

Now supporting 68040 Series

HMI

IBM is reg. T.M. International Business Machines, Inc. UNIX is reg. T.M., Bell Laboratories, Inc.

CIRCLE NO. 4

COMPUTER DESIGN
Technology and Design Directions

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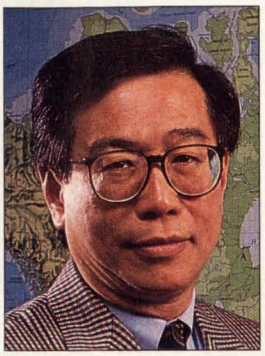

Lattice Semi's Cyrus Y. Tsui on: Programmable logic

Given the rapid pace and great diversity of the computer industry, it's sometimes difficult to stand back, take stock of the past and apply lessons learned to the many possible directions of the future. **23**

Special Section

SBus News
Technology and Market Update for SBus Users and OEMs
Sun hangs onto share of VME market
Embedded computing trends
SBus competition heats up

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TECHNOLOGY & DESIGN REPORTS

Peripheral interfaces offer fast networking solutions

HiPPI and Fiber Channel may have been defined as peripheral interfaces, but designers are taking advantage of their high data transfer rates to solve their networking problems. *—Warren Andrews* **59**

Graphics ICs target Windows acceleration

With GUIs such as Windows setting new standards, chip vendors are rethinking the most cost-effective way to speed up graphics. So instead of a few solutions, designers now have many. *—Dave Wilson* **71**

COVER STORY

PC-based CAE/CAD: any task, anywhere, anytime

The PC is today's most popular engineering platform. Portable, powerful, fast, and inexpensive, it's a match for workstations in all but the most demanding CAE/CAD applications. *—Jon Gabay* **83**

DESIGN STRATEGIES

The fastest single-shot scope in the west

The new HP 54700 series digitizing oscilloscope from Hewlett-Packard represents an absolute triumph of mixed-signal design. *—Dave Wilson* **99**

PRODUCT FOCUS

What's real in real-time operating systems?

One of the most critical "build or buy" decisions facing real-time system designers is whether to purchase an off-the-shelf real-time operating system (OS) or make your own. *—Jeffrey Child* **107**

COLUMNS

MIXED-SIGNAL DESIGN *—Stephan Ohr*

Analog behavorial simulation: not yet system-level. **139**

PCs IN DESIGN *—Jon Gabay*

Inside looking out. **143**

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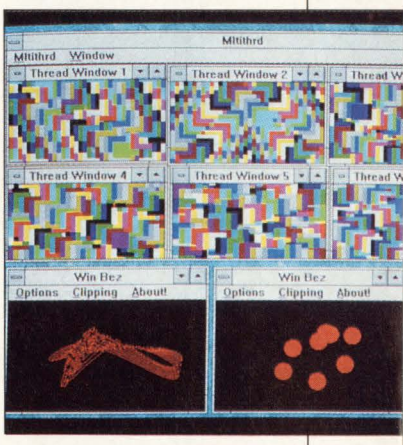

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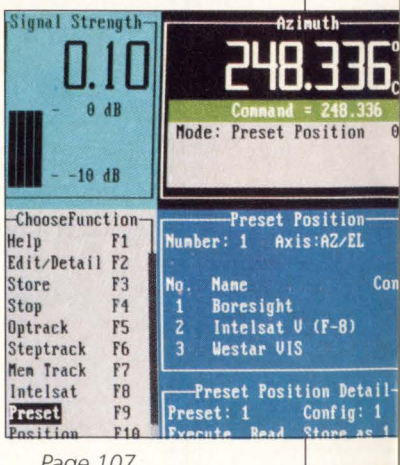

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If you're looking for realtime computing that's really open, there's only one place to really get it. Digital.

Our longtime leadership in realtime computing, combined with our total commitment to standards, makes it possible to offer you

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the industry's most complete, product-rich, open realtime environment. And, best of all, it's available now.

Digital's adherence to standards provides you with a truly open advantage. Not only does it give you flexibility in your choice of realtime systems that afford you unmatched portability and interoperability, but it also fully protects your computing investments. Digital's support for a wide range of standards includes POSIX 1003.1, draft 1003.4, TCP/IP, DECnet™/OSI, Motif® and the VME, SCSI and TURBOchannel™ buses. Plus, we now offer realtime extensions to OSF/1.®

In addition to complying with open standards, Digital makes available a host of development tools that will boost your productivity.

Besides expanding the scope of our VAXELN™ Realtime toolkit for the VMS™ environment, we're introducing the same capabilities for UNIX® environments with our DECelx™ toolkit. Once again, our open approach leaves the choice up to you.

Digital's open realtime story continues with our Network Application Support (NAS) standards-based open computing products. You can share applications from different vendors across computing platforms. What that means is no matter what size computers you have in your realtime environment—from embedded processors to mainframes, no matter what operating system you're using, Digital can tie it all together. A better solution because it's an open solution.

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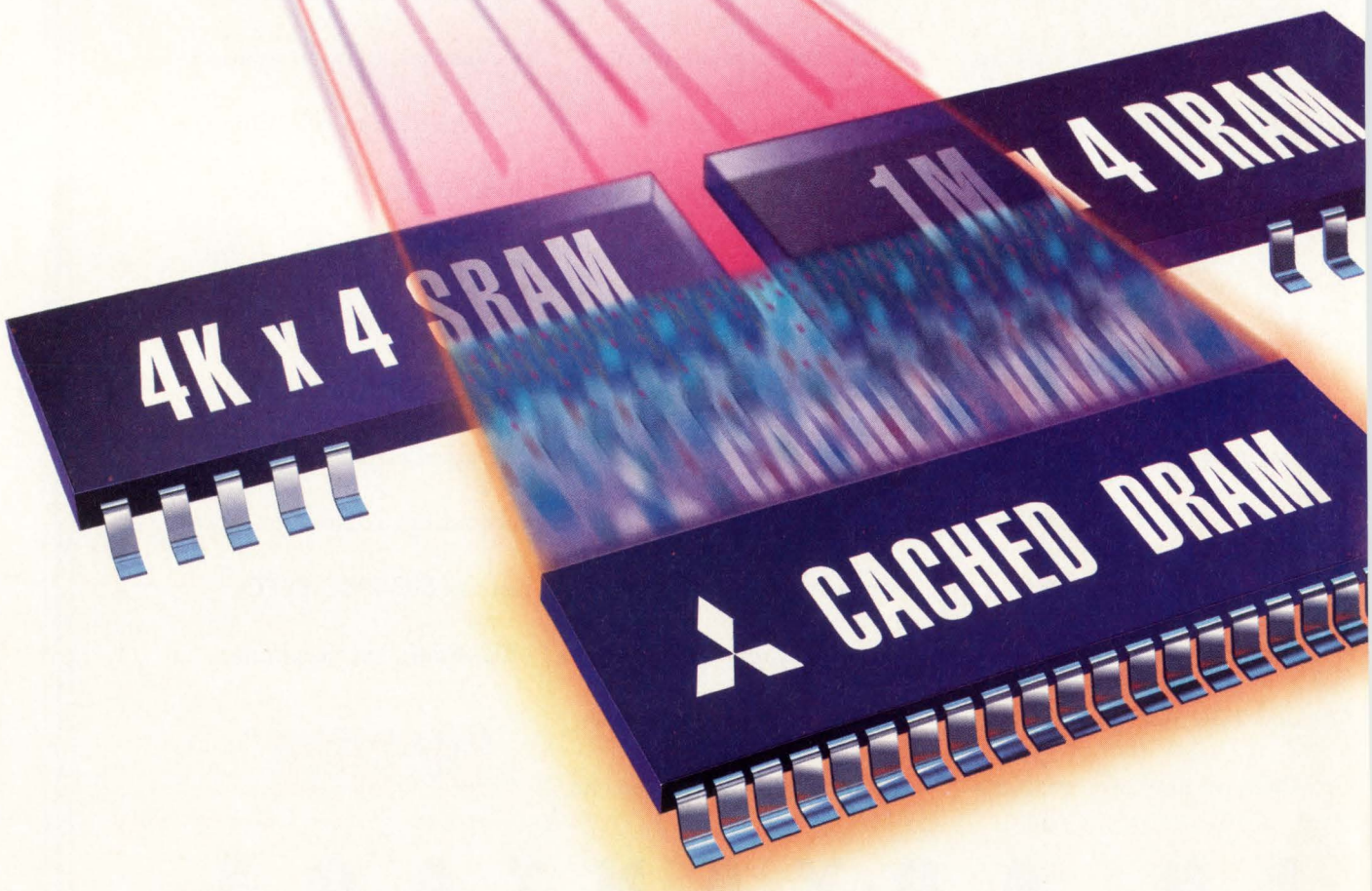
Synchronous 4Mb At 100MHz,



Cached DRAM. It Screams!

Matching low-cost DRAM technology with today's high-speed CPUs can be a design engineer's nightmare. Until now. **Introducing the 100MHz 4Mb Cached DRAM from Mitsubishi.**

FIRST SYNCHRONOUS DRAM

Mitsubishi combined a fast, 4K x 4 SRAM and a 1M x 4 DRAM with a wide, 16 x 4 bit internal bus and a synchronous clock design, all into one tiny TSOP IC. The result is the industry's first synchronous DRAM with on-board cache.

100MHz OPERATION

The Cached DRAM's large, 16 x 4 bit internal data path can transfer a 16-line data block in just one cycle, allowing the small on-chip cache to perform like a much larger external cache. The result is fast, 100MHz performance at a much lower cost than separate cache configurations. Plus, the Cached DRAM's fast copy-back scheme significantly reduces the miss cycle penalty time.

COST-EFFICIENT, SMALL SIZE

The Cached DRAM die and package are only 7% larger than those of a standard 1M x 4 DRAM. And, since they are manufactured with the same process and on the same production line as Mitsubishi's standard 4Mb DRAMs, Cached DRAMs are highly cost-efficient to manufacture.

LOW POWER OPERATION

With a clock that can be stopped to reduce power consumption to as low as 1mW, the Cached DRAM is ideal for portable and highly integrated applications where low power consumption, compact size and fast operation are essential.

MITSUBISHI'S CACHED DRAM PERFORMANCE

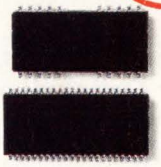
Part Number	Cache Hit Access/Cycle	Cache Miss Access/Cycle	Direct Array Access/Cycle	Package
M5M44409TP-10	10ns/10ns	70ns/280ns*	70ns/140ns	TSOP**
M5M44409TP-15	15ns/15ns	75ns/300ns*	75ns/150ns	TSOP**
M5M44409TP-20	20ns/20ns	80ns/320ns*	80ns/160ns	TSOP**

*Cache hit cycles can resume after one miss access time, while the copy-back completes in the background.

**TSOP Type II. Also available in reverse pin-out TSOP.

Samples Available June 1992

Not your ordinary next-generation DRAM, Mitsubishi's 4Mb synchronous Cached DRAM sets a totally new standard for cost-effective, high performance memory. For more information and technical specifications, please call **(408) 730-5900, ext. 2106 or 2226.**



Standard 4Mb DRAM.

Actual size.

4Mb Cached DRAM is only 7% larger than a standard 4Mb DRAM.

VISION® ACTION REALITY

MITSUBISHI
ELECTRONIC DEVICE GROUP

CIRCLE NO. 5

Price cuts up the ante in programmable market

Not long after Actel (Sunnyvale, CA) announced price reductions of up to 28 percent on its ACT 1 and ACT 2 FPGAs, industry leader Xilinx (San Jose, CA) lowered the price of its XC2000 family of FPGAs to under $5, putting the programmable devices at about 3× the cost of equivalent gate arrays. "It has been our goal since the inception of Xilinx to drive down the price of FPGAs until there was a limited cost incentive to use a custom gate array," says Xilinx president Bernard Vonderschmitt. Users are willing to pay the 3× price premium, claims Xilinx, because of other cost savings associated with FPGAs.

While Xilinx positions its FPGA silicon to cut into the gate array market, Actel is placing its FPGA design tools in competition with traditional PLD/PAL tools by cutting prices as much as 33 percent on its Action Logic System Release 2.1 toolset for ACT 1 and ACT 2 FPGAs. Commenting on dramatic price reductions of PLD synthesis software from Minc (Colorado Springs, CO), worldwide sales manager Mark Smith says, "We've taken state-of-the-art software technology for PLD design and made it available to virtually everyone." For the next three months, Minc's entry-level PLDesigner System 200 will be $495 (from $1,950) and the PLDesigner System 300 will be $795 (from $2,950). *—Barbara Tuck*

Hardware emulation pioneer Quickturn sues PiE

Days after being issued a patent on its reprogrammable hardware emulation technology, Quickturn Systems (Mountain View, CA) filed legal action against PiE Design Systems (Sunnyvale, CA), charging patent infringement by PiE with its recently introduced MARS product line. The patent, filed on December 2, 1988, protects the fundamental technology essential to the construction of any reprogrammable hardware emulator, according to Quickturn, which claims to have spent $25 million developing and bringing to market its Xilinx-based RPM Emulation System.

PiE's marketing strategy has been to present its Xilinx 4005-based emulator as a "second-generation architecture" to the 3090-based Quickturn system. Quickturn president and CEO Phillip A. Kaufman says, "Quickturn believes in open competition and providing the market with choice, which is what we did when we brought a new technology to a market dominated by software simulators and simulation accelerators. However, legitimate competition should come from the development of new technologies, and not from exploiting the inventions and intellectual properties of others." PiE's product marketing director Lavi Malhotra replies that Quickturn's claim that PiE's product is virtually identical to Quickturn's product is blatantly false. "PiE uses a radically different and more advanced architecture in its logic emulation system," insists Malhotra, "and does not in any way infringe Quickturn's patent." *—Barbara Tuck*

New Sparcs in a new Sun

Sun Microsystems (Mountain View, CA) has introduced the Sparcstation 10, its newest high-end workstation. Built around a 40-MHz version of the new superscalar SuperSparc chip (formerly called the Viking) from Texas Instruments (Dallas, TX), the workstation runs at speeds of up to 200 SPECint92, 228 SPECftp92 and 300 Mips. This is the first workstation to provide built-in Integrated Services Digital Network (ISDN) capabilities, the standard for worldwide digital telephone and networking services.

The real innovation, however, is the modular design, allowing up to four CPUs in one system, making it the first RISC workstation from a major vendor to include multiprocessing capabilities. Using M bus modules, the system can support one, two or four microprocessors. The module also permits upgrades to external cache—1, 2 or 4 Mbytes of cache can be provided via modules. While Sun chose the 3.1-million-transistor TI chip over the new, smaller Pinnacle superscalar chip from Cypress Semiconductor (LOCATION), the implication of the modular architecture is that either can be used—in fact, any superscalar, Sparc-compatible chip on an M bus module could be utilized. If this approach works, Sun won't be tied to any single semiconductor vendor.

Maintaining its commitment to open systems, Sun has also announced that it will sell the logic chips needed to build Sparcstation 10. These five ASICs are available immediately from LSI Logic (Milpitas, CA). *—Jeff Child*

Teradyne looks to shrink EDA product line

Teradyne (Boston, MA) is set to end several frustrating years of trying to make its mark in the EDA arena by selling off tools it acquired through its 1987 merger with Case Technology and Aida. Teradyne's EDA division (Santa Clara, CA) is looking for a buyer for the Vanguard PCB design tools developed by Case, as well as the automatic test pattern generation tools, logic simulation software and timing analysis tools developed by Aida.

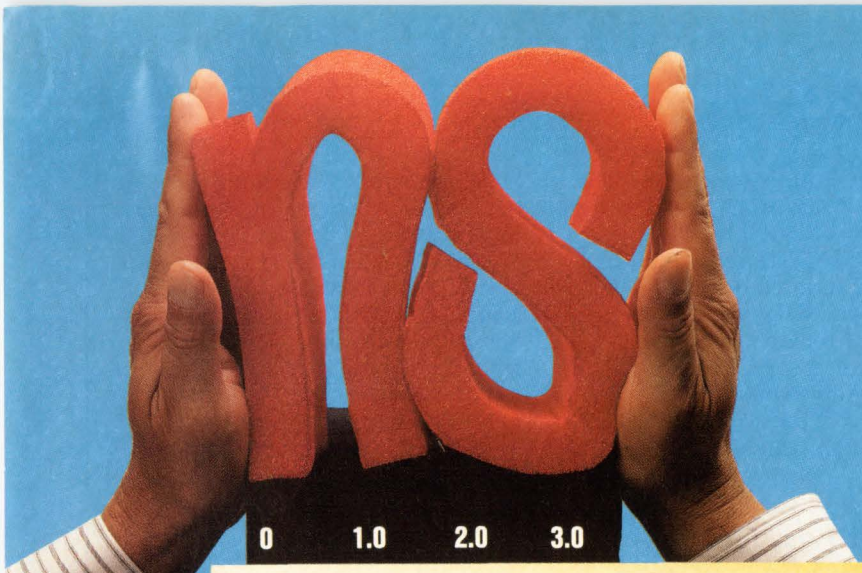
Teradyne also intends to terminate further development plans on its MultiSim Architect, a tool that was to include logic synthesis capabilities developed by Dassault Electronique (Saint Cloud, France).

Teradyne will remain active in EDA with the MultiSim Interactive Designer and the Lasar simulator, products which now account for about 80 percent of its EDA sales. *—Mike Donlin*

CFI puts its standards to the test

With the announcement of major EDA projects from four leading computer companies, the CAD Framework Initiative (CFI—Austin, TX) hopes to produce some real-world implementations of its Release 1.0 framework standard. The four firms are Hewlett-Packard (Palo Alto, CA), IBM (Armonk, NY), Siemens-Nixdorf (Pederborn,

Continued on page 12



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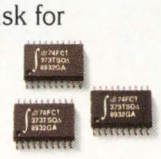

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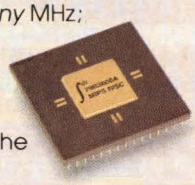

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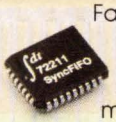

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CIRCLE NO. 6

Continued from page 10

Germany), and Sun Microsystems (Mountain View, CA).

According to Andy Graham, president of CFI, the joint efforts of the four computer companies and several leading EDA vendors reflect a commitment by CFI to become more customer driven. "The projects that these companies are involved in are implementations of the CFI standard that are intended to solve design problems within their respective organizations," says Graham. "These aren't idle exercises for academic purposes, but integration tasks that will result in products being developed and sold. We believe that their success will validate the promises that we've been making for the last few years."

—Mike Donlin

Turf tiff threatens IBM/Siemens DRAM deal

Since 1990, IBM (Armonk, NY) and Siemens (Munich, Germany) have been working under a technology transfer arrangement to develop the next generation of 64-Mbit DRAMs before the Japanese can hit the market. Now the time has come to build the fab line and a three-way tug-of-war between the two electronics giants and the German government over where to locate the plant could throw a monkey wrench into the project. According to the news magazine, *Der Spiegel*, IBM and Siemens had been negotiating over whether to build the plant outside Munich (where Siemens is headquartered) or near IBM's German headquarters in Stuttgart. Enter the German government.

Bonn is desperately trying to breathe some economic life into the eastern part of Germany, and appears unwilling to grant any subsidies whatever unless the new plant is located near Dresden. Since the costs are estimated at around $1.5 billion, both IBM and Siemens have been counting on government help. Siemens appears to be willing (however grudgingly) to go along with the idea, but IBM, which will only produce chips for internal use, is balking and might decide to produce them in East Fishkill, NY. Siemens, on the other hand, is being wooed by Singapore with offers of subsidies and cheap skilled labor. The stakes are especially high for Siemens, which is planning on leveraging off the 64-Mbit memory technology for its later generations of processors. And any delay will only allow the Japanese to get in ahead of what was planned as a U.S./German first.

—Tom Williams

X Windows, NFS come to embedded systems

The E-Venix/386 Unix real-time operating system from VenturCom (Cambridge, MA) has been enhanced with the ability to embed X Windows and the NFS (Network File System) file sharing protocol on a diskless single-board computer. The ability to embed X Windows will make it easier to design dedicated equipment with a graphical interface for use by nontechnical users. Until now, a window-based GUI for an embedded system had to be located on a separate system or terminal and communicated with the embedded code via a serial or network link.

The ability to embed the NFS protocol, in addition to the advantage of file sharing during runtime, will make it easier for programmers to do remote downloading, backup and debugging, according to VenturCom. E-Venix/386 is based on USL Unix System V. *—Tom Williams*

Second helpings

It's been rumored that Futurebus+ maker CCT (Anaheim, CA) will soon be looking at its first follow-up order from the U.S. Navy as a result of successfully completing the first part of the Next-Generation Computer Resources (NGCR) contract. Now that its equipment has passed full compliance testing and received approval of the Navy and the first systems have been delivered, CCT is looking to receive a second order for what the company now calls its 2010 Graphic Workstation. This comprises the basic boards and rack offering the functionality called for in the initial contract, plus a CCT-developed Futurebus+ array processor.

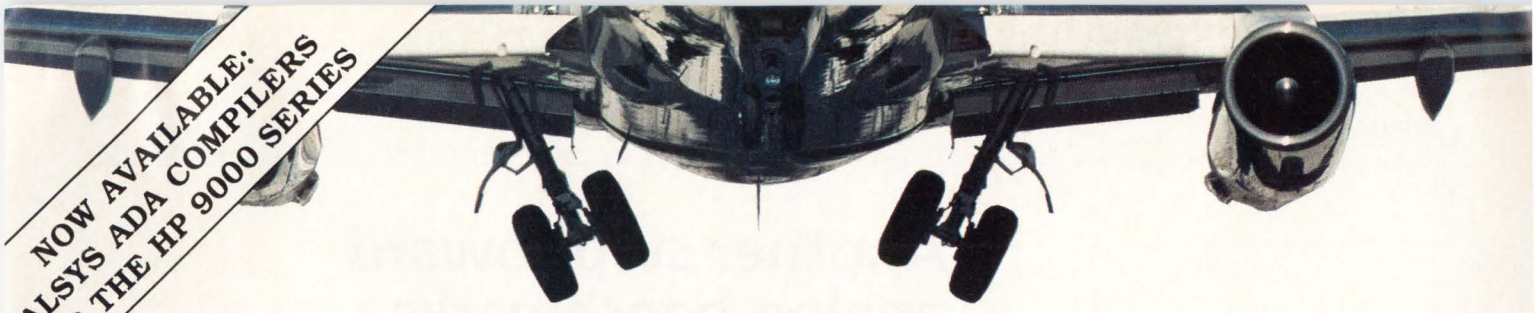
CCT's board set includes a CPU board, central arbiter/analyzer module, error-correcting memory module, and SCSI and VME adapter module. According to the company, all cards are fully compatible with the 896.1 and 896.2 specifications, complying with the Profile A standard, including cache coherence. The company's CPU card, the FBP-030, is based on a 33-MHz 68030 processor with DRAM, as well as onboard PROM containing Microware's OS-9 real-time OS.

CCT appears to have beaten the other prime contractors, Litton and Raytheon, to the punch in delivering acceptable Futurebus+ hardware in fulfillment of a contract awarded by the Navy almost two years ago. Raytheon, working with its subcontractor, Nanotek, has delivered a partial system (without cache coherence) based on the earlier Futurebus+ form factor, but hasn't delivered a complete item. *—Warren Andrews*

FDDI—killed at the starting gate?

The lifetime of FDDI-II may be cut short by ATM (Asynchronous Transfer Mode), a wide-area network that hopes to find its way down to the desktop. Fore Systems (Pittsburgh, PA) is already developing and commercializing a LAN system based on the ATM standard. Robert Sanson, executive vice-president of Fore, says that his network system is an R&D development sponsored by the U.S. Naval Research Lab in Washington, DC. In operation, each workstation on the network must have an ATM adapter card; in the center of the network, an ATM switch supports up to 64 ATM connections, each running over multimode fiber at up to 155 Mbit/s. A 16-connection version of the switch is running at beta test sites, and the same ATM architecture will be used to develop a 64-connection version later this year. Presently, adapter cards are available for both Sun and Digital workstations. Adapter cards cost around $5,000, the switch is around $4,000 per connection.

—Dave Wilson



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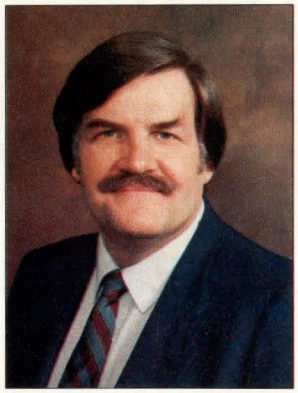
CIRCLE NO. 7

Another step toward analog benchmarks

We'd like to hear from you if you're involved in analog/mixed-signal design and have gone through the effort of developing your own benchmark circuits or procedures.



John C. Miklosz
Associate Publisher/
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If you think that sorting the facts from the fiction in advertising claims, promotional material and the statements made by enthusiastic salesmen about PLDs is difficult (see "We need more PEP(s)," *Computer Design*, May, p 22), welcome to the world of analog and mixed-signal simulation. Benchmarking PLDs and digital simulators, by comparison, is child's play.

When it comes to analog, there's no agreement about the meaning of "behavioral" simulation, for example, and there's an ongoing debate about whether "it" is as reliable or as accurate as traditional Spice simulations, about who should develop device models, about what's an "adequate" device model, and what's the "best" way to simulate a mixed analog/digital circuit.

Some of these issues were addressed last year at the first Analog & Mixed-Signal Design Conference, held in Santa Clara, CA. Two presentations in particular, "Understanding Mixed-Mode Simulators," presented by Mark Chadwick of Analogy, and "Benchmarks, Benchmarking and Other Forms of Deception," presented by Hal Alles of Mentor Graphics, stand out, as do the panel discussions "Simulation and Device Modeling," moderated by Mike Donlin and Steve Ohr, and "Who Really Won BCTM," moderated by Steve Ohr. The panel discussions last year were especially lively because the audience could challenge any statements made by the panel members, most of whom were representatives of EDA tool vendors.

Well, the *second* annual Analog & Mixed-Signal Design Conference is coming—October 28-30 at the San Francisco Airport Hyatt Regency. We have the opportunity to tackle some of these tough issues again and, we hope, move a little closer to providing analog and mixed-signal designers with tangible help in making their simulator choices. Prompted by the interest shown by conference attendees last year and a proposal from Mentor's Hal Alles, Steve Ohr is organizing an extended panel discussion on "Guidelines for Benchmarking Mixed-Signal Simulators," to be held the first day of the conference. In connection with this panel discussion, Steve is asking EDA tool vendors and mixed-signal IC vendors to contribute specific circuits/devices that they believe could be used to exercise and evaluate an analog/mixed-signal simulator or a specific capability of a simulator. Steve isn't looking for circuits that will "crash" a simulator, or a circuit that will produce a "winner" or a "loser," or one that every tool vendor could claim to have simulated "best," with the definition of best being up to the individual tool vendors. In essence, Steve is looking to model these analog simulator benchmarks and benchmarking procedures along the lines used by PEP, the programmable device evaluation consortium discussed in this editorial last month. On Steve's behalf, I'd like to reach out to all of *Computer Design*'s readers and ask for your help. If you're involved in analog/mixed-signal design and have gone through the effort of developing your own benchmark circuits or procedures, we'd like to hear from you. Call Steve (at 908-232-1380) or me (at 508-392-2114) and let's talk about how you can contribute to this effort. Thanks.

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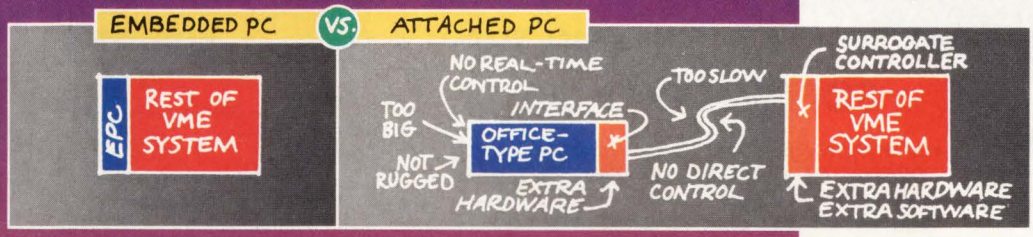

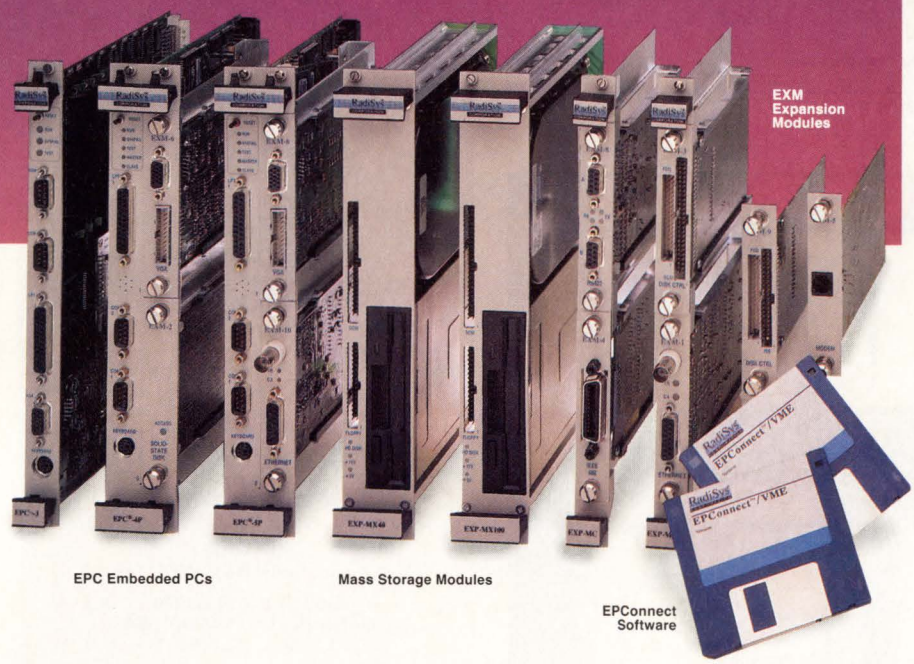

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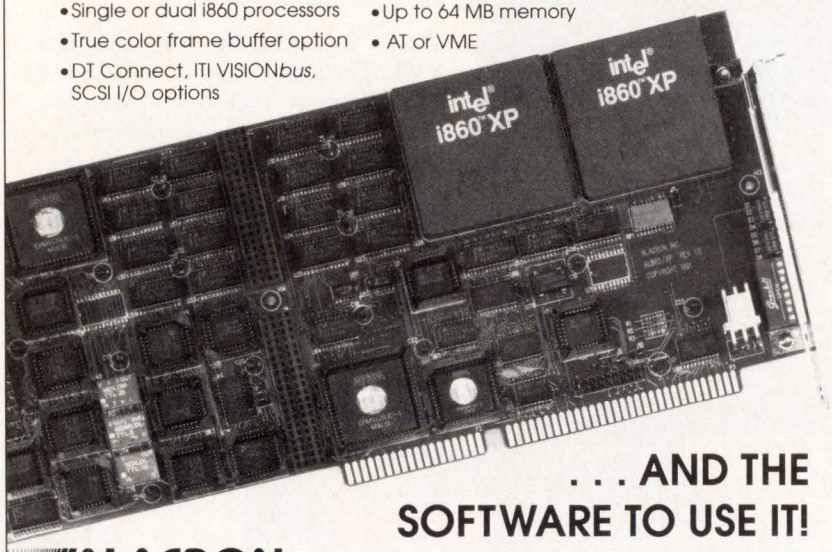

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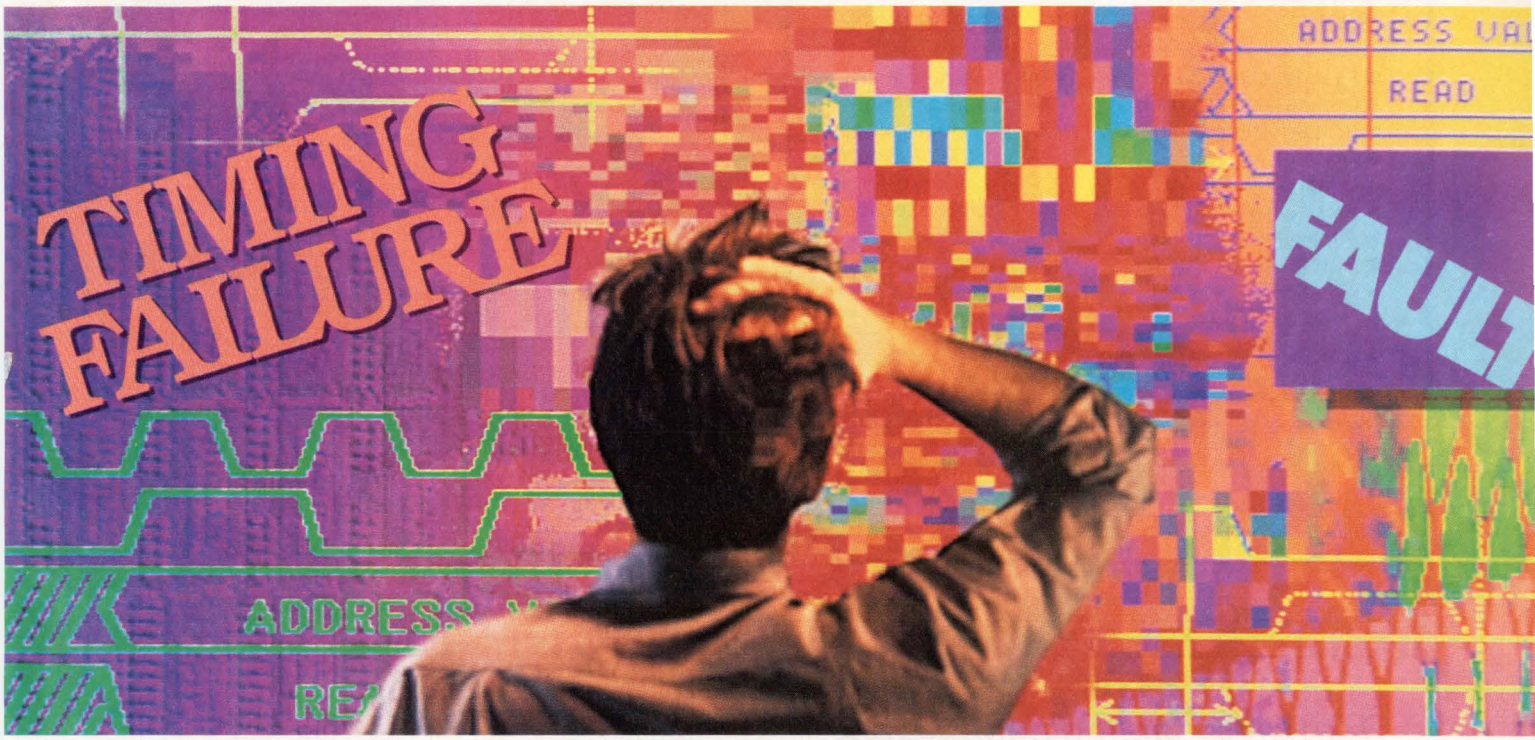

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CIRCLE NO. 13

CALENDAR

CONFERENCES

June 8 - 11

DAC

Anaheim Convention Center, Anaheim, CA. The 29th Design Automation Conference is geared toward electrical engineers, computer scientists and management, and will offer technical programs, tutorials and vendor exhibits. New at DAC are sessions on real-world EDA user problems and solutions targeted at high-level company executives. User sessions include "Why is today's CAD inadequate for designing tomorrow's computers?" Contact: MP Associates, 29th DAC, 7490 Clubhouse Rd, Ste 102, Boulder, CO 80301, (303) 530-4333, Fax (303) 530-4334. **Circle 366**

June 16 - 18

Nepcon East '92

Bayside Exposition Center, Boston, MA. This conference will feature products and technologies for the design, fabrication, assembly, packaging, inspection, and testing of printed circuits and electronic assemblies. Technical session topics address surface-mount technology, pollution problems when switching from solvent cleaning, concurrent engineering, and surface-mount components. There will also be a workshop on low-volume SMT. Contact: Reed Exhibition Companies, Cahners Plaza, 1350 E Touhy Ave, Des Plaines, IL 60018, (708) 299-9311, Fax (708) 635-1571. **Circle 367**

June 23 - 25

AFCEA 46th International Convention & Exposition and ITEMS '92

Washington Convention Center, Washington, DC. This convention is the world's largest communications, intelligence and information systems event. The show focuses on professional development and information exchange for military, government and industry personnel. Panel topics include: "The electronic battlefield: tomorrow's approach to training, rehearsing and testing," and others. Also AFCEA will launch Imaging Technologies & Evolving Management Systems Conference and Exposition (ITEMS), featuring the latest imaging software and hardware. Contact: AFCEA Programs Office, AFCEA International Headquarters, 4400 Fair Lakes Ct, Fairfax, VA 22033-3899, (703) 631-6125, Fax (703) 631-4693. **Circle 368**

July 6 - 9

Professional Developers Conference

Moscone Center, San Francisco, CA. Microsoft is holding a technical prerelease conference focusing on 32-bit Windows development for professional, commercial and corporate developers. General sessions will cover Win32 API (including Win32s), Windows NT and development tools. More than 40 breakout sessions will feature tracks on Win32 development, the Windows programming environment, development tools, corporations and Win32, writing device drivers for Windows, international localization, and Windows extensions. Contact: (800) 227-4679. **Circle 369**

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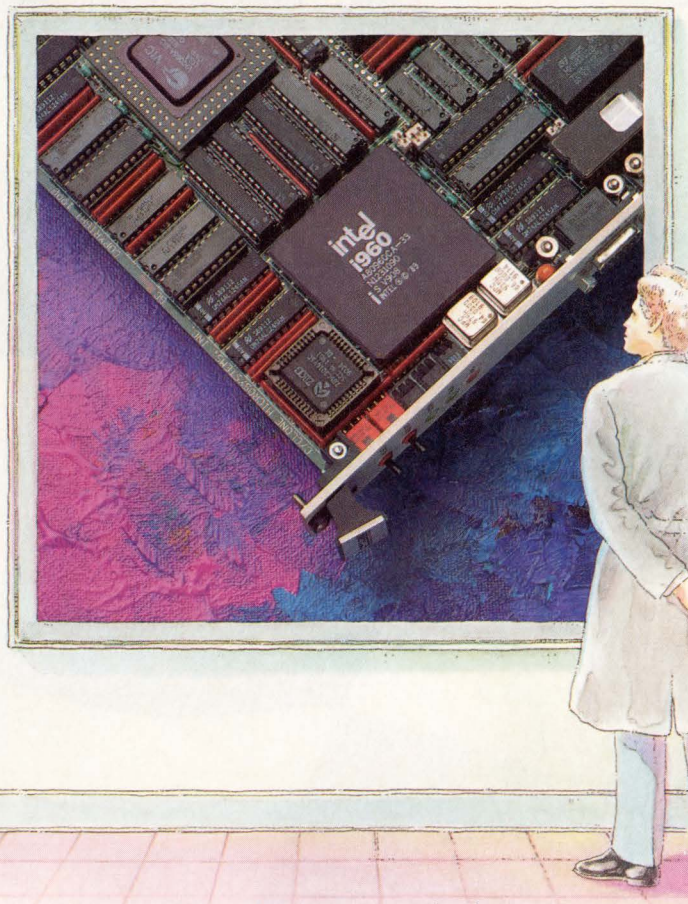

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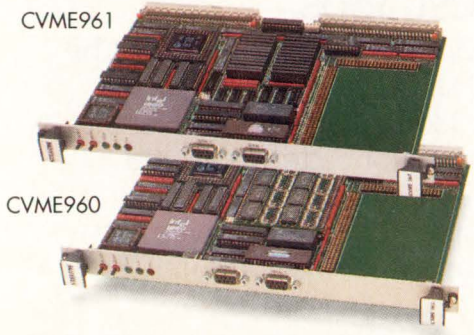

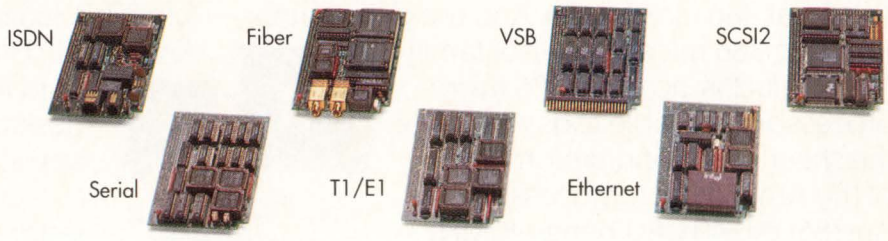

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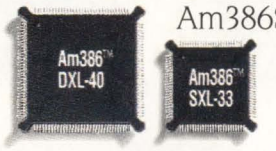

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CIRCLE NO. 16

Cyrus Y. Tsui on: Programmable logic

Given the rapid pace and great diversity of the computer industry, it's sometimes difficult for those of us in the trenches to stand back, take stock of the past and apply lessons learned to the many possible directions of our future. We can be forgiven for attaching great importance to our own particular subfields at the expense of others, especially in view of the rich contributions made by every sector in furthering speed, flexibility, affordability, and market growth. At the risk of being accused of such a narrow focus, I want to suggest that some of the most important developments of this decade will be the result of innovations to come in programmable logic.

Obviously, no one can accurately predict the future. But the programmable logic industry, now nearing its 20th birthday, has accumulated the kind of wisdom that comes with age and experience. While the field can still be considered young and burgeoning, significant innovations are commonplace, and we can now look to the past as a window on our immediate future.

Today there are programmable logic technologies competing for the attention of designers that are stupendous in their sophistication and capabilities, each promising massive potential rewards for marketers and end-users alike. Even considering the potential, however, it's my conviction that the greatest innovation—indeed, a fundamental shift in the programmable logic paradigm—is yet to come and will occur in this decade.

Four key lessons from history

Driving this fundamental paradigm shift will inevitably be scientific breakthroughs. These breakthroughs will be expedited by the wisdom gained from four key lessons learned in our 20-year history.

John Birkner, a product planner at Monolithic Memories Inc. (MMI), found PLAs, the original programmable logic devices, to be large, cumbersome and slow. He proposed the first PAL, a device that would be smaller, faster, field-programmable, and significantly easier to use. As with many new product ideas, the PAL architecture wasn't met with applause when it was proposed to the MMI design community. MMI designers saw it as a step backward. It was viewed as a subset solution of the PLA problem, and far less flexible from an architectural standpoint.

However, H. T. Chua, a newcomer to MMI's design department at the time, began to see the possibilities that this new device held. Together, Birkner and Chua implemented the idea in silicon and went forward to produce the PAL device, the first PLD standard.

The team successfully overcame entrenched objections to bring the new paradigm to life. But more important, the new paradigm was made possible by Chua's openness to the idea, no matter how farfetched it seemed to others. Had he sided with the rest of the MMI design community and decided that Birkner's concept didn't warrant further consideration, the history of the PLD would have been dramatically different—and quite possibly nonexistent.

The first lesson from history, then, is the need for champions—individuals with the ability and willingness to step outside of conventional thought and authorize the prudent exploration of a new concept until it has been accredited or exhausted.

Unfortunately, in many corporate environments inertia often makes it easier to dismiss a new idea because "it's never been done that way" and, therefore, it can't possibly work. This deadly attitude can open the door to a flood of smart, nimble competitors who can easily exploit this kind of entrenchment. At MMI in the mid-1980s, for example, we looked at CMOS technology for the PAL architecture simply because of the high volume required, rather than fully exploring the potential advantages that the new technology might bring to bear. Today, less than a decade later, CMOS is the dominant technology. AMD has

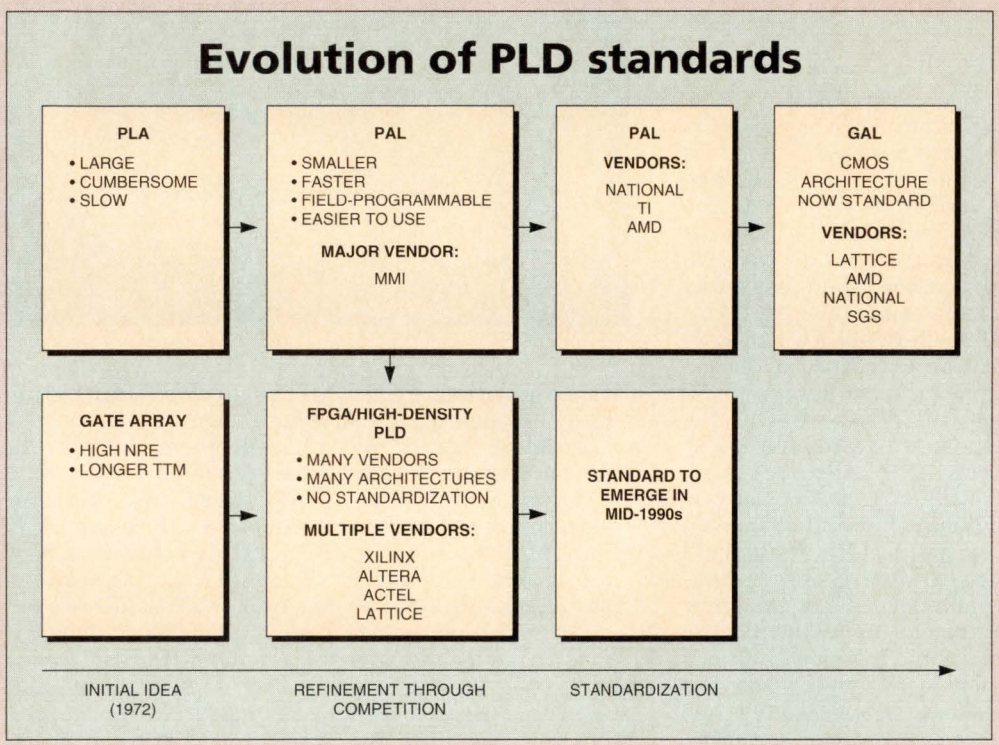
Cyrus Y. Tsui is president and CEO of Lattice Semiconductor Corporation, Hillsboro, OR

found itself with a host of new competitors, my company among them, and the PAL device is no longer the only PLD standard.

When organizations let champions flourish and new ideas proliferate, they make it possible for the next generation of Birkners and Chuas to emerge, and potentially stimulate the next important advance in PLD technology.

Benefits, not specs, determine success

A champion embraces and promotes a new idea for what it is: a technology, a design or a departure from the past. In many cases, the tactical and market forces that can fully develop a blossoming idea remain obscured. Consequently, the champion can only be viewed as a partial solution.



Our own PLD market is a perfect illustration of this phenomenon. While the PAL device was a marvelous product in itself, the customer ultimately defined the product and the market. We thought we were selling field-programmable silicon; our customers were buying risk reduction and faster time-to-market.

Today, rapid developments in PLD technology and increased competition have sparked a virtual "war of specifications" in which the relative merits of E^2CMOS, SRAM and antifuse or differing device architectures are widely debated. While these developments make for good advertising copy and headlines, they haven't substantially changed the commodity our customers wish to purchase.

I'm convinced that any technological advance in the programmable logic industry, whether expressed in throughput, density, cycles, or any other attribute, must speak to the issues of risk reduction and time-to-market. As we look to the future, technologies that make the most of these qualities and maximize their inherent benefits to customers will enjoy a dominant position in the marketplace. That's the second lesson history teaches us.

In-system programming (ISP), or the ability to program and reprogram a device while on a circuit board or *in-system*, is an excellent example of a technology focused on risk reduction. The concept of ISP isn't new in the computer field; the dynamic RAM in millions of personal computers used worldwide illustrates this concept perfectly. Memory is programmed over and over again as new data is obtained and stored. When put in the context of logic, however, ISP represents a dramatic breakthrough with tremendous potential for market expansion.

The mechanics of this technology are of relatively little interest to most customers. Few will explore the product specifics in terms of circuitry or the processing technology that makes it all possible. What matters to the user is that ISP technology lets the manufacturing department program or reprogram boards after they are built. Design corrections can be made without reworking the board. New product features can be added to hardware via a software upgrade. What matters is that the in-service programming of PLDs now represents the best means available of reducing risk, limiting nonrecurring costs and accelerating the time it takes to bring complex electronic products to market. With customer vision, ISP technology can change the programmable logic market into the reprogrammable logic market.

These qualities, not specifications in silicon, are what drive the market—and determine what customers ultimately buy.

Competition will clean up your market

As a market expands, it becomes attractive. Each new entrant has the advantage of watching the technology develop in the early stages of market acceptance. This typically results in a dozen or so new products and competitors, each pursuing the original market opportunity with a slightly different slant, from a slightly different vantage. This was clearly the case in the PLD industry as we saw the original PAL product replaced by the now-dominant CMOS GAL device. As a result, the once-dominant PLD makers have taken a backseat in the most rapidly expanding market segments.

There are many lessons to be learned about competition from the makers of the PAL device.

MMI/AMD was one of the first high-technology companies to protect its intellectual property in this area. In the mid-1980s, for example, the company brought suit or the threat of suit against at least a dozen companies for infringement of the original PAL device patent. In this case, litigation was used not only to protect the company's property, but also to literally define the competitive playing field. As a result of suits brought against its competitors, MMI/AMD gained access to patents and technologies otherwise unavailable to the company—not the least of which was the GAL device from Lattice Semiconductor. In addition, litigation served as an offensive weapon by preventing easy market access to foreign competitors. The programmable logic industry, like the microprocessor market, is one of the few billion-dollar industries without significant foreign competition.

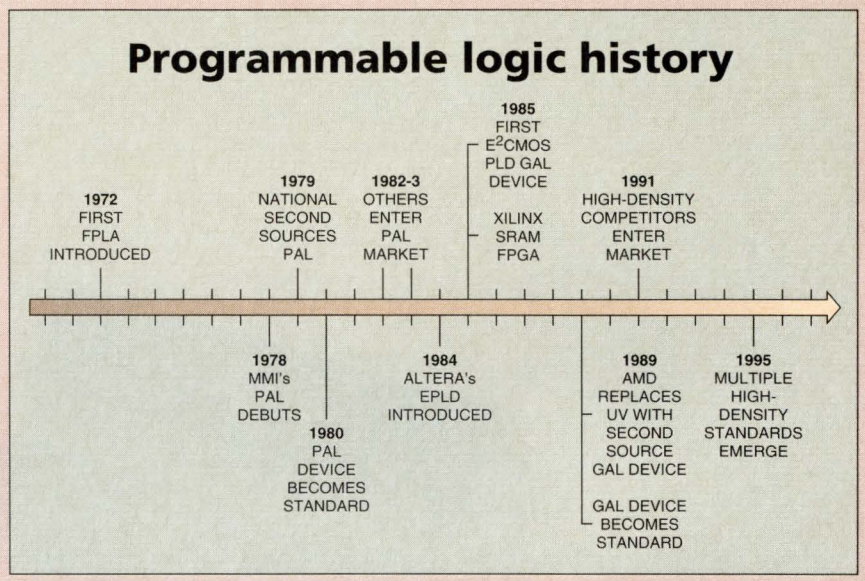
Another lesson comes from the ability (or inability) of an innovative company to watch market trends while focusing on product or market development. Many companies have good ideas and enjoy the rewards of those ideas for only a short time. Few are able to continually adapt those ideas to meet the changing competitive threat and customer demands. A company that's inwardly focused ignores the subtle messages that herald technological opportunity. It misses quick acceptance of competitive technologies and dismisses small, unknown competitors. Perhaps the high-density PLD market lacks large, potentially dominant suppliers for just this reason.

Any lesson on the potential threat of competition would be incomplete without mentioning a life-threatening disease affecting most companies at virtually every level. The "not invented here" syndrome is prevalent within many American companies. The American dream was built on ingenuity and innovation. A loose translation might be that fresh ideas are the only ones with the big payoff. We as a nation have trouble seeing innovation in refinement or optimization of an already great idea. As a result, it's very tempting to "roll the dice" on that new and potentially risky idea. An old idea isn't necessarily a bad idea. At the risk of offending our noble neighbors to the East, Japan has built a world economy on refining old ideas with timely market execution. It's important to recognize when a design, manufacturing or marketing idea shouldn't be reinvented.

The market makes the standard

The PAL standard encompassed many different devices. In essence, multiple standards were housed under a generic PAL architecture. The high-density market is awash with competitors, many of whom are new to the programmable logic arena. Each company is currently expounding the architectural advantages of its devices. Clearly each of these vendors—and Lattice is no exception—is competing to be the next market standard. But a standard is rarely set by an individual company. A product becomes a standard by being recognized by the company's customers and legitimized by the competition. That's the last key lesson.

PAL and GAL devices have each attained the status of industry standards. But they wouldn't have attained this status if the market hadn't responded favorably to the product concept and competitors hadn't adopted the product architecture. Although there are companies within the high-density PLD market enjoying significant market dominance, neither customers nor competitors have embraced any of their architectures as an industry standard. As a result, there are at least a dozen different competing companies and technologies in this rapidly expanding market, with additional emerging competitors.



A device standard isn't likely to emerge soon in the high-density PLD market, either. The programming elements and device architectures vary too greatly. The diversity of technologies will probably first result in multiple PLD product standards. Groups of products or technologies will compete to be the standard in speed-intensive applications. Others will compete for applications requiring high utilization. And still others will compete in terms of advanced features such as ISP. In other words, device technologies and product architectures will evolve to best serve their own market niches.

I do believe, however, that we'll see a new industry standard for high-density programmable logic by the end of this decade. It will probably be marked by a drastically different architecture and process technology; the product evolution readily observable in today's market will not take us there.

By the year 2000 this market will have seen unbelievable, unpredictable changes. Although historical introspection can't necessarily help predict the future, it can help avoid foolish mistakes of the past. The next "big idea" in programmable logic will come from the company that's both technologically focused on customer needs and flawless in its execution. May the best company win!

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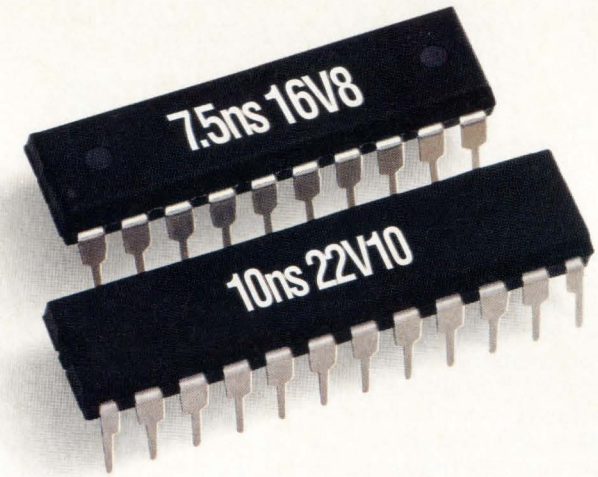

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INTEGRATED CIRCUITS

ASIC core brings fuzzy logic to semiconductors

Tom Williams, Senior Editor

A licensable core technology for fuzzy logic processors is now available to semiconductor manufacturers, specialized ASIC users and vertically integrated industrial companies. The technology will allow integration of silicon fuzzy capability in custom designs. Togai Infralogic (Irvine, CA) is offering what it calls fuzzy computational acceleration (FCA) technology for licensing and custom-chip development.

For several years Togai has provided a digital fuzzy processor, the FC110, and a number of board-level products based on the FC110. The company also offers a range of fuzzy software development tools.

FCA is billed as second-generation fuzzy ASIC technology, aimed at giving manufacturers the ability to design information-intensive "smart" products around highly integrated silicon. FCA technology can be applied in three ways: as a custom ASIC incorporating a fuzzy core with custom logic, as an integrated processor including a conventional CPU core with a fuzzy core or as a fuzzy coprocessor working with a host CPU. Togai's vice-president of operations, Daniel Bochsler, predicts that "semiconductor-based fuzzy technology will be as prevalent in products by the end of the decade as microprocessor technology is today."

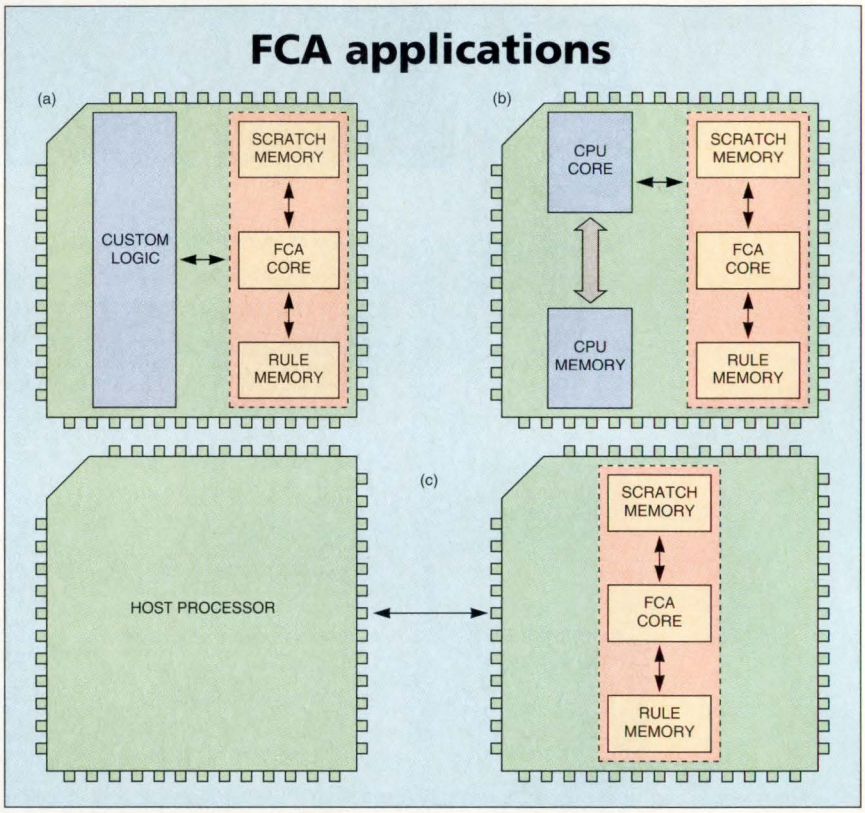
Scalable technology

The FCA technology is scalable from 8 to 32 bits and includes, in addition to the fuzzy processing core, rule-base and scratch-pad memories that can be built to different sizes, depending on the customer's requirements. A 10-bit implementation of the core technology, for example, can handle up to 1,024 inputs and up to 1,024 membership functions per input. Output variables can also have up to 1,024 membership functions.

Membership functions are fuzzy sets assigned to a variable to indicate degrees of belief in that variable's conditions; for example, almost empty, half full, full. Such functions are most often represented as graphs that map an input value to a degree of "truth," or membership, in that set. With the FCA core, you can define membership functions graphically to be any arbitrary shape.

Practical applications wouldn't make use of 1,024 inputs with 1,024 membership functions each; that would require enormous amounts of memory in any case. Still, the numbers indicate the flexibility of the core technology. Practical combinations of variables and membership functions are limited by available rule-base memory and the realistic needs of the application. One of the virtues of fuzzy logic is that it's able to address problems with a relatively small number of rules. The benefit of this hardware implementation is that it speeds up rule evaluation over what can be achieved with conventional processors.

For example, running at 20 MHz, a 10-bit FCA core in a system with eight inputs and four outputs can evaluate in 70 ms a base of 20 rules, where each rule has five antecedents, or input conditions, and two consequences. The 70 ms includes the time it takes to "defuzzify" the output, or arrive at a "crisp," unambiguous answer. Another way of looking at the FCA's performance: the same core implementation, given a rule-base of 40 rules, each with two inputs and one output, can evaluate up to 800,000 rules per second, including defuzzification.



Implementations using Togai's fuzzy computational accelerator (FCA) technology include customizing ASICs to incorporate fuzzy capability (a), integrating fuzzy processing on-chip using a conventional microprocessor (b) and linking fuzzy coprocessors with a host CPU (c). FCA implementations can be from 8 to 32 bits, and can vary as in the size of rule-base and scratch-pad memories.

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CIRCLE NO. 19

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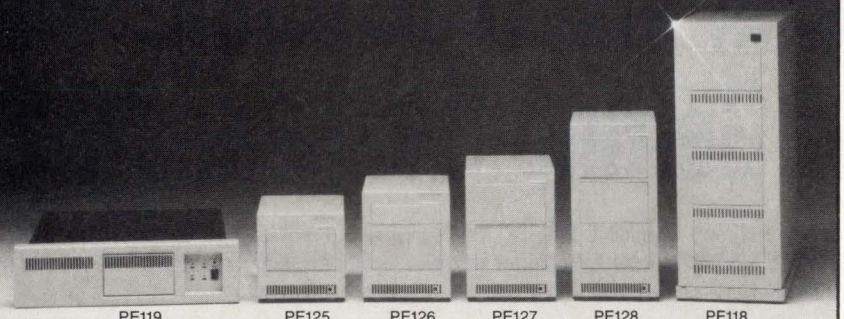

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CIRCLE NO. 20

development for the FCA will depend on tools already offered by Togai, according to Douglas Leo, Togai's manager for VLSI and hardware development. TILShell, for example, is a graphics-based development environment that lets you graphically design inputs and outputs and process objects for a fuzzy system; it also lets you draw membership functions, write and edit

"Semiconductor-based fuzzy technology will be as prevalent in products by the end of the decade as microprocessor technology is today."

—Daniel Bochsler, Togai Infralogic

rules and compile code. One of the formats output by TILShell is Togai's Fuzzy Processing Language (FPL).

Togai has developed a new rulebase format for use with the FCA technology, so there will be a tool to convert FPL files into this new format. Run-time generators will be developed for each custom FCA design that is licensed to a customer. These will let you convert the rulebase files from a general format into run-time binaries for individual FCA implementations.

"At this point," says Leo, "there has been no decision on third-party tools." That is to say, the company isn't at this point providing a means for developers to use tools other than Togai's to develop FCA-based applications. ■

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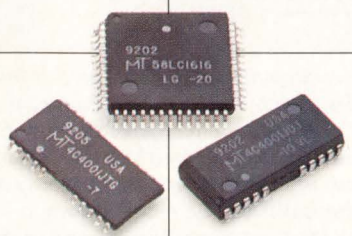

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MT5C2561 LP		256K x 1	Now
MT5C2564 LP		64K x 4	Now
MT5C2565 LP		64K x 4 $\overline{OE}$[5]	Now
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*Self Refresh [1]DW– Dual Write Enable [2]DC– Dual $\overline{CAS}$ [3]FPM– Fast Page Mode [4]SC– Static Column [5]$\overline{OE}$– Output Enable

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CIRCLE NO. 21

INTEGRATED CIRCUITS

Setting the record straight on SRAM loading

Dave Wilson, Senior Editor

Michael Davis, formerly a product marketing engineer at Cypress Semiconductor (San Jose, CA), believes that certain SRAM manufacturers are involved in the process of specifying the speed of their SRAMs with zero capacitance load on their outputs—a process that makes them look faster than they might operate in an actual design environment. Indeed, it's not hard to find engineers that agree with him. John Peters, technical director of VMEbus products at Performance Technologies (East Rochester, NY), a VME and SBus bus-board design house, is one of them. He says that such underhanded practices are commonplace. "Playing the game of changing the capacitive loading to improve the performance specifications of devices is quite common. I've seen that game played in a lot of different places, not just with SRAMs. PAL vendors are good at that, too," he says.

The other side of the argument

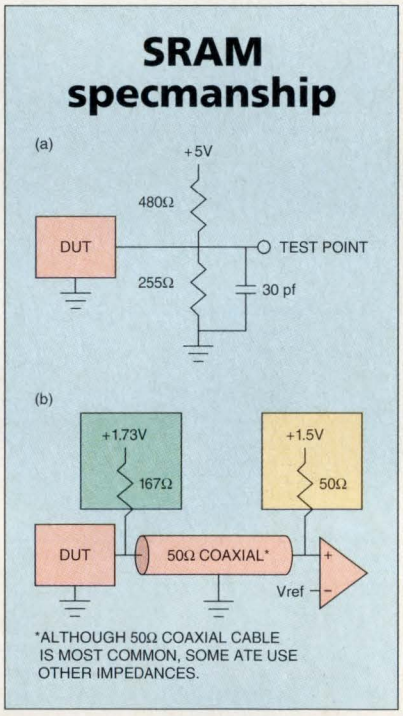
David Chapman, applications manager for fast SRAMs (FSRAMs) at Motorola (Austin, TX), takes umbrage at Davis' statement, however. He argues that the capacitive load becomes irrelevant as the speed of SRAMs becomes faster. "The ac test load diagram that fast SRAM vendors have traditionally put into their data sheets has been around since the days of 55-ns SRAMs. Since then, SRAMs have gotten considerably faster. As a consequence, the test environment has started to behave as if it were a transmission line. At that point, the lumped capacitive effects go away," he says.

But do they? Many designers don't know. "Since we don't have the elaborate test fixtures, we have to trust the SRAM vendors," says Dean Moss, an engineer at Diversified Technology (Ridgeland, MS). "We are held at the mercy of what those guys tell us." While Moss agrees with Motorola's Chapman that test fixtures are antiquated, especially for under-12-ns SRAMs, he finds it hard to believe that the capacitive component is of no consequence.

His proof's on paper

Motorola's Chapman has put forth his arguments in detail in a paper called "Regarding SRAM Specmanship." In it he shows the ac test load that's traditionally printed in SRAM data sheets, as well as a load that looks more like a transmission line load—one he claims should better describe the behavior of FSRAMs. He says that once the RAM begins "swinging its outputs fast enough," the capacitive effects "disappear." They are "replaced" or "overcome" by transmission line effects.

Don't believe that just because the capacitor may "disappear" as a function of the SRAM's speed, vendors who continue to use the traditional loading diagram in support of their SRAMs haven't bothered to test them with a real capacitive load. Many, such as Cypress and Toshiba, still use a 30-pF capacitor as the test load, even on their faster parts, just to conform to a standard—the philosophy being that any standard, poor or not, is better than none at all.



The traditional lumped capacitive ac test load is used by many manufacturers as a way to specify the test environment of SRAMs; it's diagrammed in (a). As SRAM speeds increase, this model gives way to the transmission line model shown in green (b). Here, capacitive loading of the device becomes less important. The ac test load diagram used by Motorola's SRAM operation shown in yellow (b) uses a 50 Ω termination resistor and a 1.5-V supply, requiring two to three times more dc current drive than the transmission line model.

Which model to use?

But for what class of devices is the lumped capacitive model ineffective? Where is it more appropriate to use the transmission line model? Tom Baillio, senior development engineer at Mercury Computer Systems (Lowell, MA), has some answers. He says that the lumped-load/transmission-line crossover point has more to do with SRAM edge rates than it does with access times.

The transmission line effects, according to Baillio, are more a result of the speed at which the output buffers in the SRAM switches from a 1 to a 0 state, or vice versa. "That rate will give you an indication of whether you are looking at a transmission line or a lumped load," says Baillio. "The line begins to look more like a transmission line as the edge rates of the SRAMs fall. Typically, an etch in a circuit looks more like a transmission line than a lumped load when the round-trip propagation delay of the signal along that line is less than either the rise or fall time of the SRAM. That's when you start to see reflections back from the remote termination of the line."

The ac test load diagram used by Motorola's FSRAM operation is a good representation of the actual test environment in both physical and electrical terms, according to Chapman. Note the difference between the ac test load diagram for a transmission line and that for the Motorola FSRAM. In the former, the load resistor is set to 167 Ω with a 1.73-V load voltage, a combination that behaves identically to the resistive portion of the circuit in the test load diagram usually attributed to SRAMs.

Unfortunately, Chapman says,

when signals are fast enough for transmission line effects to come into play, failure to terminate the transmission line that runs back to the automatic test equipment's comparator in its characteristic impedance introduces noise into the circuit. The noise can make the SRAM appear to be either faster or slower than it actually is, complicating correlation between testers and the test environment. Chapman notes that the 50 Ω termination resistor tied to the 1.5-V line used in the test load diagram for the Motorola FSRAM adds another layer of conservatism into the design, since it requires two to three times more dc current than the environment shown in the test load diagram for the transmission line.

"Since we don't have the elaborate test fixtures, we have to trust the SRAM vendors. We are held at the mercy of what those guys tell us."

—Dean Moss, Diversified Techonology

It may not matter

Unfortunately for the argumentative, it may be all moot anyway. Most SRAM vendors—Cypress and Motorola included—say their customers prefer to have a Spice model of their SRAMs and then simulate the loading effects in the particular application. After all, using Spice lets you model the exact kind of parasitic capacitances that will be seen on a board, allowing both the trace lengths and the number of devices that will be driven to be taken into account.

Of course, there will be those designers that may not have the time or who can't go to the trouble of getting Spice models. They'll just have to use extremely conservative design rules in their memory designs and keep their fingers crossed that they don't run into any transmission line problems. ■

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CIRCLE NO. 23

ASICs & ASIC DESIGN TOOLS

Technologies move toward hardware/software codesign

Barbara Tuck, Senior Editor

Recent advances in high-level synthesis technology and system verification through reprogrammable hardware emulation have pushed in the direction of hardware/software codesign and promise to enhance your ability to bring error-free systems to market.

Architectural-level synthesis got a boost recently when the European Development Center (EDC—Leuven, Belgium) announced that the DSP Station digital signal processing design environment was commercially available. With DSP Station, you can go from one high-level DSP and system specification down to processor assembly code and synthesized custom ICs or ASICs with bit-serial datapath architectures.

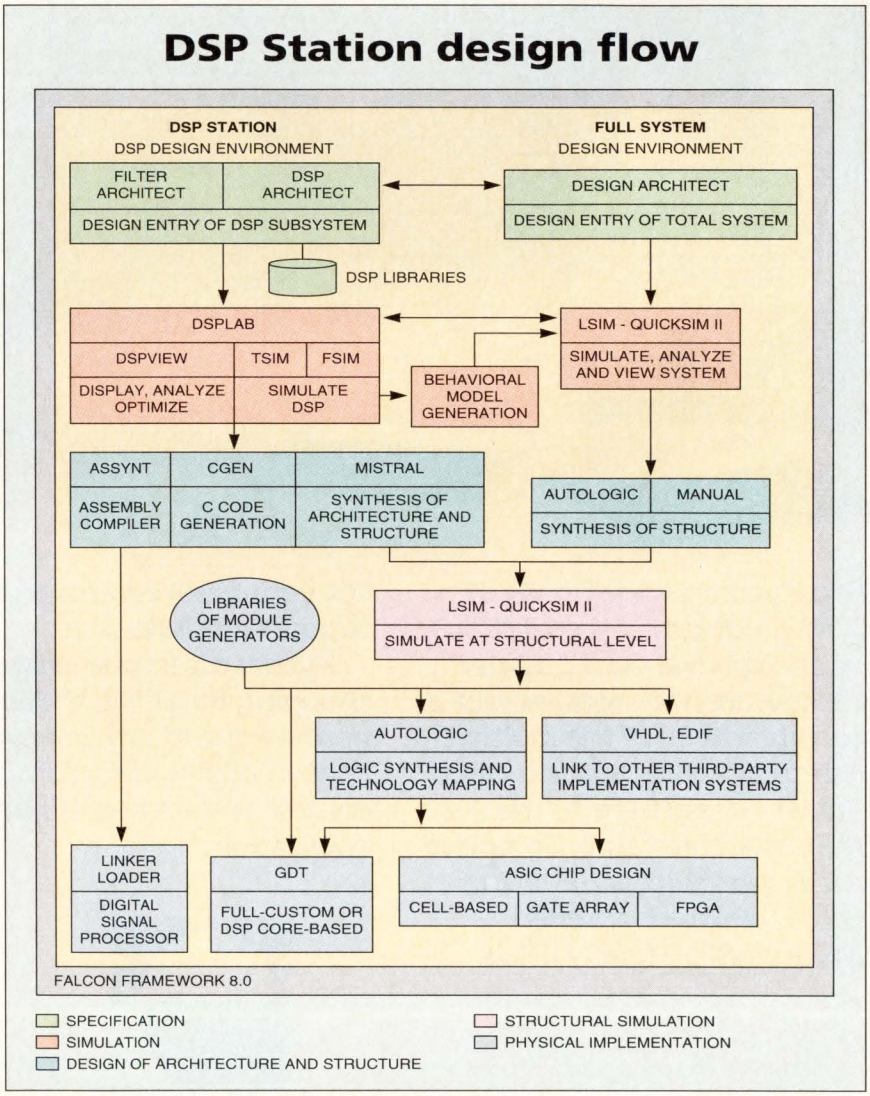
In the early phases of design, you can decide on hardware/software partitioning and on the selection of the optimal algorithm for the application. DSP Station distinguishes itself from most synthesis tools by embracing the high-level synthesis tasks of system partitioning and scheduling. It also provides resource allocation, memory management and delay optimization.

Hooked into Falcon

By using DSP Station, you gain access to more generic design tools through the Falcon Framework from Mentor Graphics (Wilsonville, OR), into which EDC's environment has been integrated. Mentor is an equity partner with EDC, along with Philips International (Eindhoven, The Netherlands) and the Interuniversity Microelectronics Center (IMEC—Leuven, Belgium). Through these ties, EDC has combined the expertise of a leading EDA vendor, a large tool user and a research institute to develop and bring its DSP Station to market. Research results from IMEC and Philips Research have been used in developing DSP Station, and will continue to be used in revising the product. For example, the high-level synthesis capabilities of DSP Station's Mistral I compiler are based on the Cathedral I silicon compiler of IMEC. All together, IMEC has tuned a total of four silicon compiler environments to specific domains to generate area-efficient chips.

Hugo De Man, vice-president of the VLSI systems and design methodologies division at IMEC, claims that tool developers will have to make difficult choices as synthesis is extended to higher levels in system building. "Nobody has the recipe for a general high-level synthesis system," he says. "You can't enter general code and get efficient silicon. Within a C++ object-oriented synthesis database, users will have to put tools to work on a high-level data model and a library of knowledge of the particular application being addressed. Synthesizing algorithms and architectures is definitely much more complex than synthesizing gates."

DSP Station design flow



EDC's DSP Station focuses on the DSP portion of a system—but when connected to broader system design tools through the Falcon Framework, it spans the complete analog and digital design environment. The output of its Mistral compiler, at the register-transfer level in VHDL, goes to Mentor's LSim/QuickSim II for structural-level simulation, then to Mentor's AutoLogic for logic synthesis and technology mapping, and finally to either GDT for implementation as full-custom or core-based chips or to Mentor's ASIC design tools for implementation as cell-based chips, gate arrays or FPGAs.

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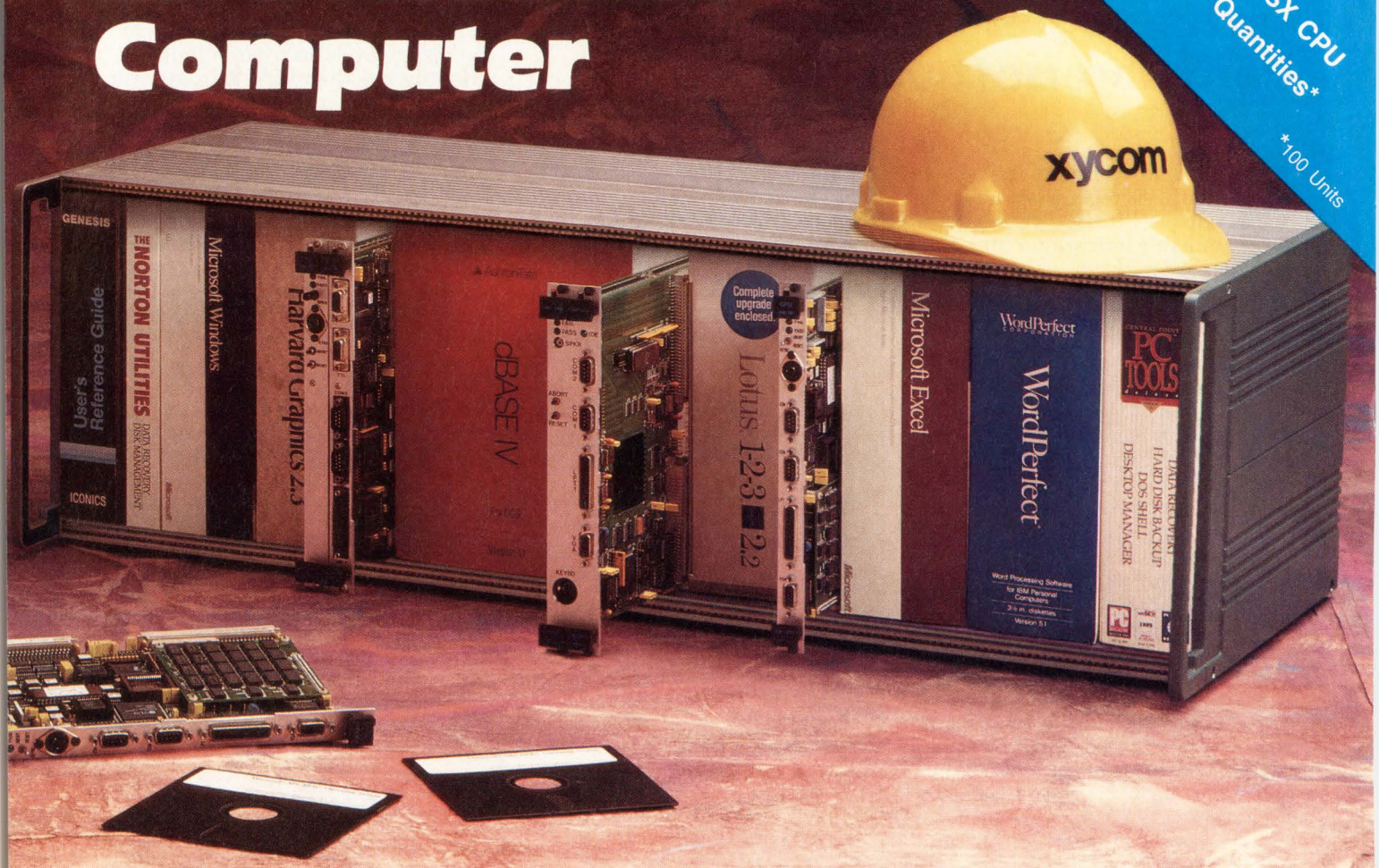

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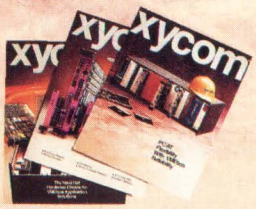

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CIRCLE NO. 24

ASICs & ASIC DESIGN TOOLS

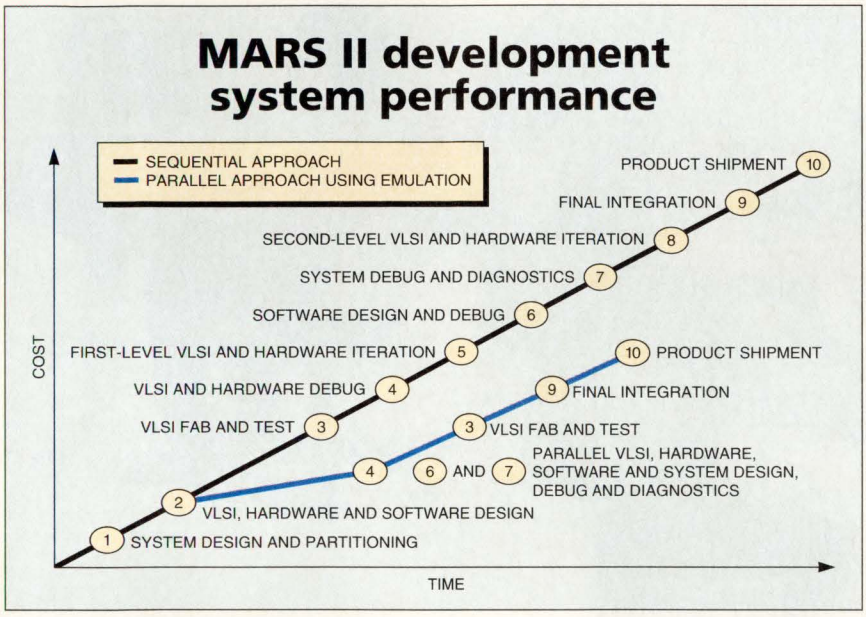
Within the next year, EDC plans to extend DSP Station's synthesis capabilities to bit-parallel microcoded multiprocessor architectures using Mistral II, which is based on IMEC's Cathedral II silicon compiler and Philips Research's Piramid system. Mistral II will produce a netlist in terms of a library of module generators targeting standard cells, gate arrays or general cells. The Cathedral III and IV silicon compilers target datapath architectures and regular arrays of processors respectively. Though they target different architectural styles, the compilers all accept the same behavioral specification as input.

Though emphasis on hardware efficiency is paramount in all the Cathedral projects, IMEC has built the ability to interactively fine-tune results in critical subparts of the application into the compilers. "We don't guarantee the global optimum," says De Man, "but we do guarantee something that's very difficult to beat by hand."

Since DSP Station has been integrated into Mentor's Falcon Framework, you can have access to Mentor tools at every level of a DSP design—from high-level specification of the algorithm through simulation and optimization and into physical implementation.

DSP Station users can enter algorithms through a schematic editor or through textual entry in data flow language (DFL), a commercial version of the Silage flow-graph-based specification language developed at the University of California at Berkeley. For filter design, you can describe the gain and phase characteristics of the filter you need, and DSP Station's Filter Architect will generate an algorithm.

Mentor will distribute DSP Station worldwide. The first signal processors supported by DSP Station are the Texas Instruments TMS320C30 and the Motorola 56000.



The MARS II system emulators from PiE Design Systems facilitate parallel hardware and software development tasks by enabling emulation of ICs in their end products. In contrast to conventional logic simulation methods, emulation techniques let you exercise complex VLSI components in target hardware systems.

Other DSP synthesis solutions

EDC is not the first to take up the challenge of easing system-level DSP design. Comdisco Systems (Foster City, CA) pioneered this area with its Signal Processing WorkSystem (SPW) which today, five years after its introduction, boasts of an installed base of over a thousand. Neither the Comdisco tools nor the Synopsys synthesis tools to which they interface, however, support high-level synthesis tasks. With the

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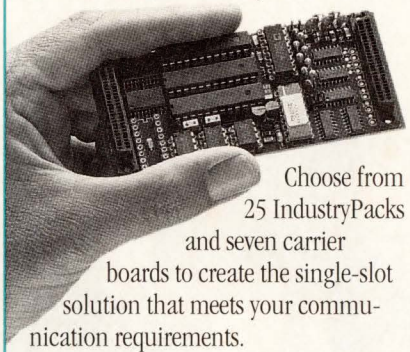

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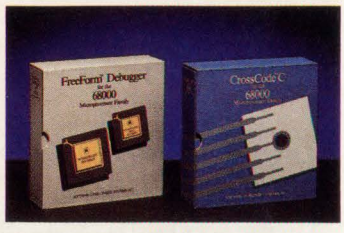

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ASICs & ASIC DESIGN TOOLS

SPW, you have to manually partition your designs into hardware and software by using the DSP Designer block-diagram editor. Nevertheless, you can develop hardware and software in parallel. Comdisco has just begun shipping beta versions of the DSP Framework top-down DSP design environment which supplements the SPW core technology by adding new functions and features, new paths to implementation and new interfaces to standard design tools. The DSP Framework integrates all of Comdisco's DSP design elements through an intuitive user interface. Production versions will be available by next month, and the toolset will have been integrated into Mentor's Falcon Framework. The DSP Framework supports programmable DSP chips, DSP ASICs, FPGAs, PC-board designs, and DSP core-based designs.

We don't guarantee the global optimum [with Cathedral], but we do guarantee something that's very difficult to beat by hand.

—Hugo De Man, IMEC

When satisfied with DSP designs created within the DSP Framework, you can call on Comdisco's optional Hardware Design System to convert your optimized bit-accurate block diagram into a VHDL netlist. You can then use this netlist to generate logic gates using Synopsys synthesis tools or other third-party tools. The DSP Framework's VHDL generation capability and full design testbench let you use the toolset for verifying your design all the way down to final layout sign-off, claims senior vice-president Mike Walsh. You can modify designs, test them, and send them back down to the implementation tool to continue the design process.

Signal Calculator added

With the introduction of the DSP Framework, Comdisco has added the Signal Calculator to the SPW's interactive DSP design, simulation and analysis tools. The Signal Calculator applies the look and feel of a hand calculator to the tasks of editing, manipulating and analyzing signals and simulation results. Comdisco packages DSP expertise into its systems applications library as well as its library of over 500 function-level DSP blocks. Last month, Comdisco began shipping an assembly code generator to add to its optional C-code generator and multiprocessor code development option.

Dr. Emil Girczyc, R&D director for high-level synthesis for Synopsys (Mountain View, CA), reports that the company is working on those capabilities. When you go above logic and register-transfer-level (RTL) optimization to domain-specific synthesis, Girczyc agrees with IMEC's De Man that a generic synthesis kernel and specialized tools are required. "A scheduling algorithm might be successful for only a very narrow application area," he says.

And how does DSP Station compare to the VHDL-based Frenchip synthesis tool from Dassault Electronique (Saint-Cloud, France), which can synthesize ASICs with DSP function blocks? "The synthesis in DSP Station starts one level above that in Frenchip," says EDC's general manager, Herman Beke. "We first synthesize an optimal architecture to implement an algorithm and then continue, like Frenchip or other VHDL synthesis packages, with the synthesis of a structural implementation of that architecture. One of the intermediate results of DSP Station is RTL, which could be fed into Frenchip as an alternative to our own structural synthesis." Frenchip has recently been integrated into the MultiSim Architect VHDL toolset from Teradyne EDA (Boston, MA).

Dr. Lev Markov, director of optimization at Racal-Redac (Mahwah, NJ), reports that his company has developed the prototype of a generic performance-driven architectural synthesis tool that would sit on top of RTL tools such as Racal-Redac's SilcSyn or Synopsys; the tool lets you explore domain-specific architectures under your control. From a single behavioral description, you

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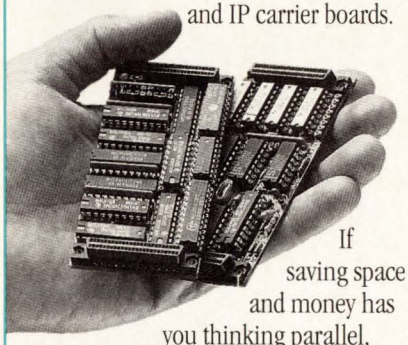

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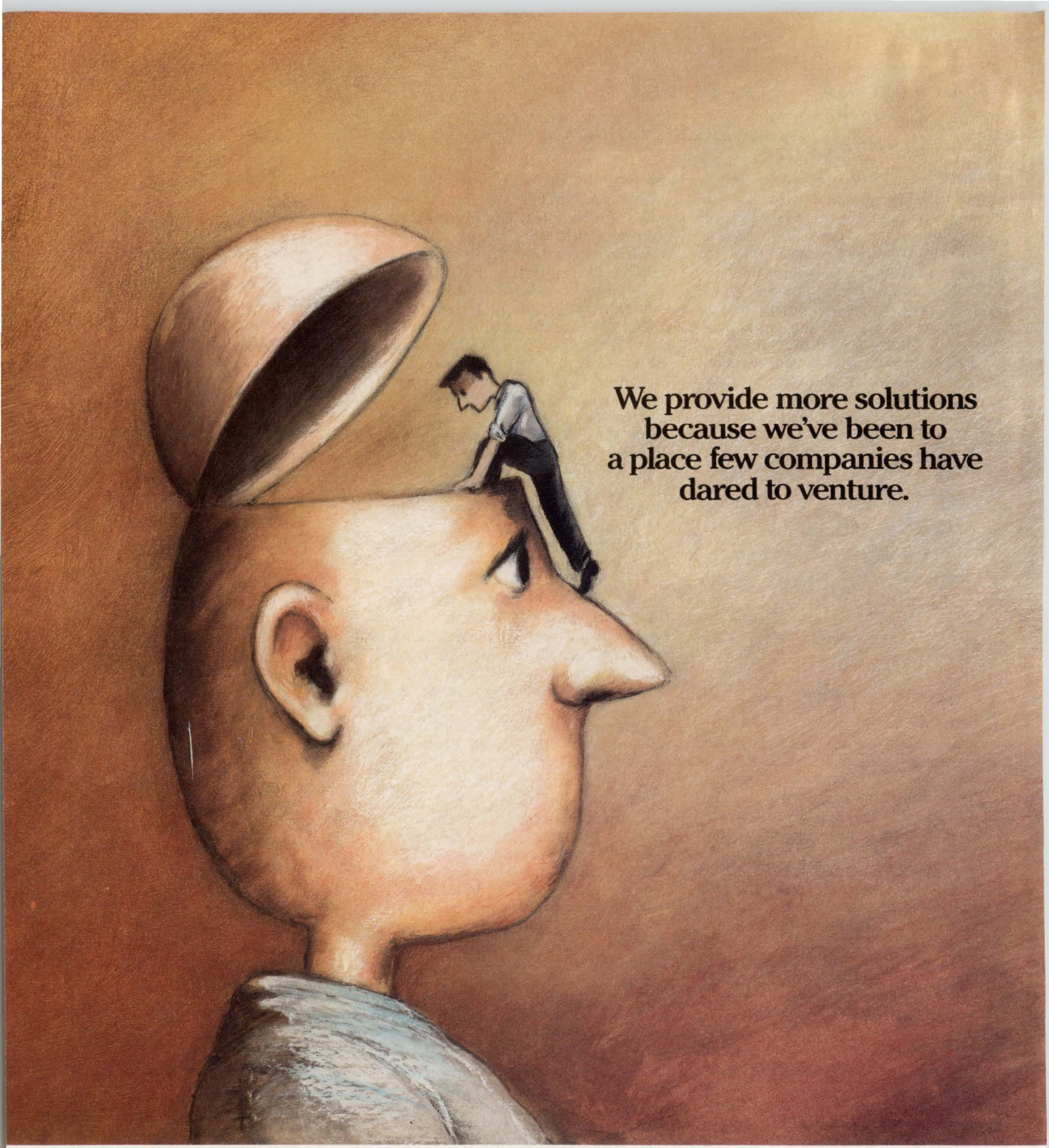

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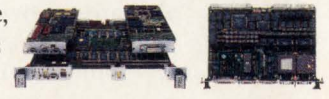

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ASICs & ASIC DESIGN TOOLS

would create application-specific RTL structures and would interactively deal with performance, area, timing constraints, and required and prohibited resource sharing, so that the RTL netlist would satisfy all design requirements. You would have to partition a system design into hardware and software components, however, before picking up the architectural synthesis tool.

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One of the intermediate results of DSP Station is RTL, which could be fed into Frenchip as an alternative to our own structural synthesis.

—Herman Beke, EDC

■■■

which validates VLSI designs in the final product. Since its introduction in 1989, the RPM Emulation System of Quickturn Systems (Mountain View, CA) has been without head-on competition. But PiE Design Systems (Sunnyvale, CA) has now introduced its MARS II series of system emulation products. (MARS is an acronym for modular, automatic, retargetable, and scalable.)

MARS II is based on Xilinx 4000 FPGAs and is claimed to operate at speeds up to 8 MHz. You can use it to verify the system-level operation of microprocessors, complex function-specific ICs and ASICs. MARS II includes timing-driven partitioning software, resulting in a system that can reduce time to emulation from weeks to hours. A specialized algorithm automatically partitions a design and maps it to the logic emulation hardware—all in a single pass.

Debugging and emulation functions are separate in the MARS II series, with the Ethernet-based debugger being a shared resource supporting several emulation modules. Both debugger and emulator can be expanded in increments. Also, future emulation modules based on newer FPGA technologies will be able to coexist with older modules used on the same project.

Just weeks after PiE Design Systems brought its system emulator to market, pioneer Quickturn enhanced its own Xilinx-based reprogrammable hardware emulator, making it a moving target for its new competitor. The newly introduced 50,000-gate RPMplus, for systems using ASICs or full-custom chips, brings the emulation of nonsynchronous and asynchronous design styles to Quickturn customers for the first time. A pair of new algorithms analyzes complex designs and maps them into a representation guaranteed to be free of any timing violation. These algorithms map all synchronous and nonsynchronous designs without user intervention. For asynchronous portions of the design, the algorithms allow precise control of emulation timing. RPMplus offers full X Windows support, automatic transfer of data between CAE and emulation environments and integration into the Verilog and Mentor Graphics simulation environments. ■

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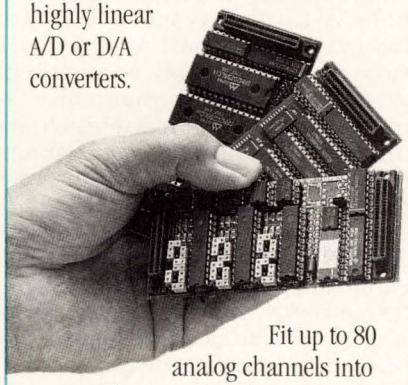

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THE CHOICE WITH A FUTURE

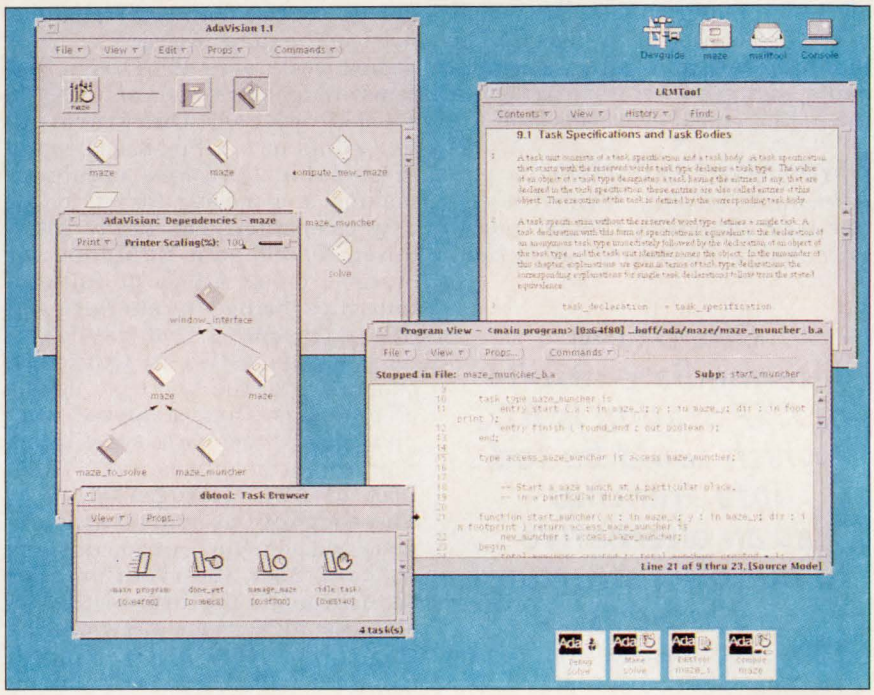
CIRCLE NO. 29

SOFTWARE & DEVELOPMENT TOOLS

Tools wed Ada compilers to integrated development environments

Tom Williams, Senior Editor

Vendors of software development tools find themselves in a sea of possibilities in terms of what to offer and support and what to leave to other vendors. This is an industry where partnerships blossom—in bundling, say, another company's compiler with your toolset, or in working out compatibilities and interfaces so that your programming toolset (for example, an editor, compiler, library, and debugger) can be used with another company's higher-end CASE tools. But the promise of comprehensive, all-encompassing frameworks where any tool can be plugged in and used with any other has yet to become reality.



The Sun Ada development environment, via the AdaVision graphical interface, lets you use a single toolset, such as the library management, debugger, editor, and help facilities shown here, to develop software for Sparc workstations, as well as a number of embedded target systems.

Two paths for Ada

Building efficient Ada compilers, for example, has apparently become such a specialized task that vendors of development tools and environments are quite content to either adapt and bundle compilers from third parties or build in hooks that let you integrate your choice of compilers into your environment. Rational (Santa Clara, CA) is an example of a company that's announced a new tool that lets you integrate your choice of Ada compilers into its extensive software engineering environment. On the other hand, SunPro, a division of Sun Microsystems (Mountain View, CA), has purchased a very efficient Sparc compiler from Verdix (Herndon, VA) and has established hooks so that users of its Sparcstation-based Ada development environment can cross-compile, edit and debug code for target systems using other processor-specific compilers from Verdix without leaving the Sun Ada development environment.

Sun's Ada development environment consists of the Sun Ada compiler for the Sparc and a set of tools called Sparcworks/Ada. Sparcworks/Ada supports the edit/compile/debug cycle, but it also includes an Ada source-code generator for a drag-and-drop graphical interface builder named Devguide. Sparcworks/Ada consists of AdaVision, an OpenLook-based graphical tool for managing the Ada library unit structure and dependencies; a window-based debugger called dbtool; an editor named EditTool that synchronizes compiler errors with source code; and an on-line reference manual, LRMTool.

The Rational Environment, by contrast, encompasses a wider range of tools but also stops short of supplying its own compilers. Like Sun, it's also establishing partnerships with CASE vendors such as Cadre Technologies (Providence, RI). The Rational Environment incorporates support for the edit/compile/debug cycle, configuration management and version control (CMVC), and a repository that manages details about the program such as requirements, design, and information about system builds and releases from the CMVC facility.

Both companies have an interest in supporting as many processors and as many compilers as possible so that, according to SunPro product manager David Spenhoff, "A user on a Sparcstation only has to learn one interface to develop software to run on the Sparcstation, and can also use that same interface to create embedded software for different target systems." Sun has added cross-compiler support for a number of the VADScross compilers produced by Verdix. They include VADScross 6.0.5 for the Motorola 680X0 family, as well as VADScross for the Sparc and the MIPS 3000. Using these compilers, you can edit, compile and debug code with the Sparcworks/Ada tools directly over a network from your Sparcstation.

The Rational approach

Rational's approach has been to supply a tool that lets you immediately use a number of compilers that have been adapted by the company, and

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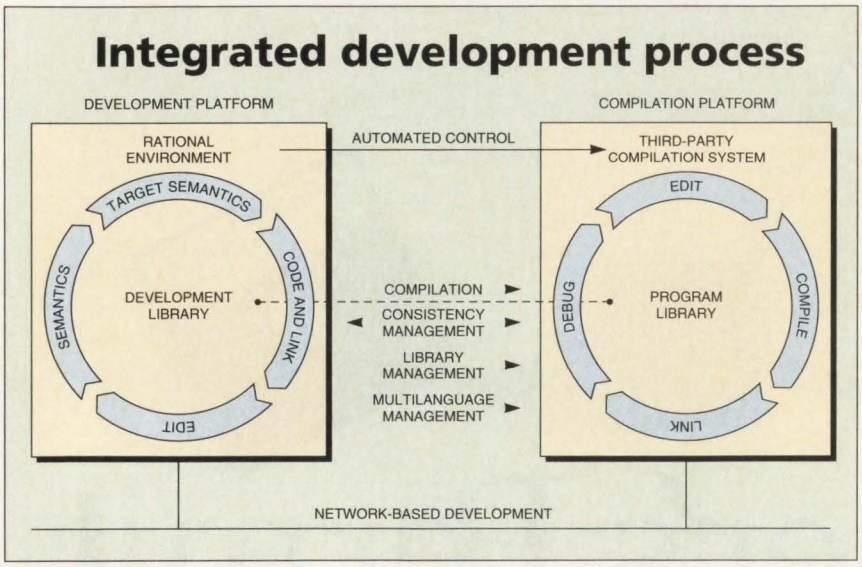

Rational's Compilation Integrator lets you access a variety of third-party compilation systems, including libraries and linking facilities, from a single, integrated software engineering environment which includes third-party development tools as well as Rational's own development and configuration-management tools.

then adapt additional compilers of your choice. Rational Compilation Integrator then lets programmers have their choice of a wide variety of high-quality Ada compilers on the market. "It's quite common for large projects to have multiple compilers," says Gerard Rudisin, director of marketing for Rational. "In the space station project, there are four compilers in use."

The advantage of the Compilation Integrator is that Ada programs for different machines can be developed, tested and managed within a single software engineering environment, but Rational doesn't have to develop cross-compilers itself for use with its system.

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SOFTWARE & DEVELOPMENT TOOLS

maintains state and history information in the Rational Environment for each unit in a remote program library, letting you check for consistency and incorporate changes that are made back into the software engineering environment's control after they are recompiled.

While the Ada language is standard, individual compilers differ in terms of the nuts-and-bolts characteristics of the processors they support, optimization features, data layout, and other attributes. Rational found a way to configure its environment to take the nitty-gritty differences among compilers into account. The Rational Environment then serves as a universal host, supporting all of the program development and much of the testing. Final compilation can be done with a native compiler on the target system, or with a cross-compiler that has been adapted to the Compilation Integrator on the host system.

Differences accommodated

The kinds of differences that are accommodated by the Compilation Integrator are such things as the length of words, floating-point representation and whether a machine automatically rounds numbers or not. The different "pragmas," or instructions to the compiler that tell it which optimization modes to turn on and off—determining the length of arrays, for example—have to be defined for each compiler. All of this detail is fairly easy to do, taking about a week according to Rudisin, and it's something that customers can do as well. Rational currently provides several 'shrink-wrapped' integrations of popular compilers. These include the AIX Ada/6000 from IBM, the SunOS Sparc Ada, the LYNX i386 and Unix i486 Ada compilers from Alsys, the DEC VMS VAX compiler, and the VMS i960 compiler from Tartan.

The Rational Environment is required to use the Compilation Integrator. The Environment, which sells for $25,000 per user, also lets third-party tools such as the Teamwork CASE toolset from Cadre be incorporated, along with Rational's own Design Facility front-end tool. The Compilation Integrator sells for $2,000 per user. The Sun Ada development environment ranges from $10,000 for a single network license to, for example, $7,480 for a 25-seat license package. ■

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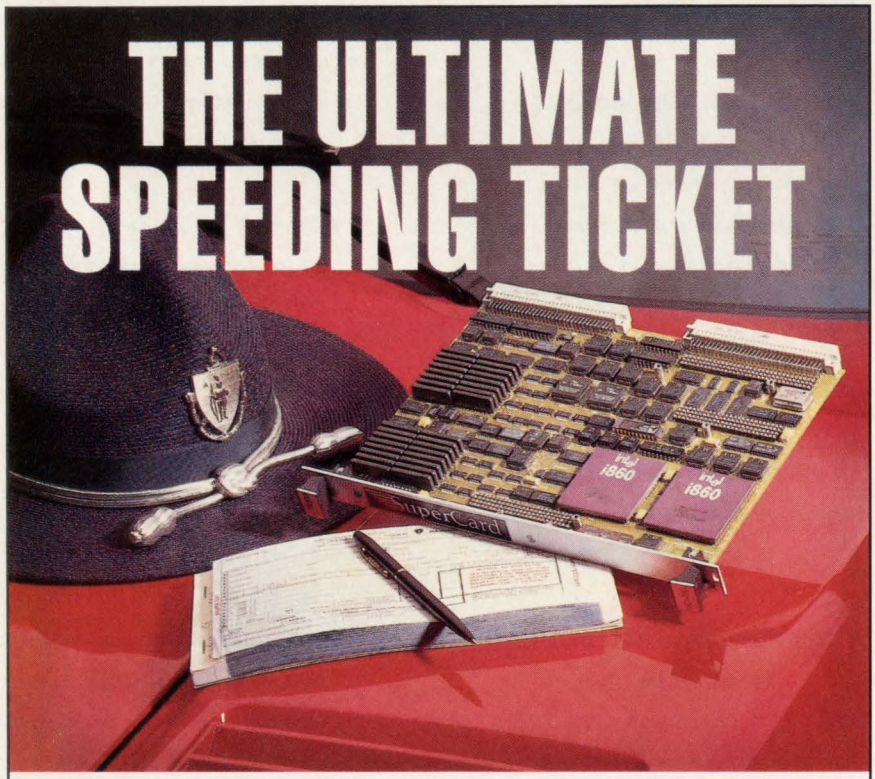

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CIRCLE NO. 34

COMPUTERS & SUBSYSTEMS

VMEbus SSBLT spec now on target

Warren Andrews, Senior Editor

The proposed source-synchronous block transfer (SSBLT) addition to the VMEbus Revision D specification has had some rough sledding over the past several months, but it looks like clear sailing from here on. Making the approach viable, however, has called for some sweeping but much needed upgrades to the original VME specification.

The proposed SSBLT addition to the specification, which calls for the elimination of VMEbus handshake signals and lets the data lines provide the clock signal for transferring information, was initially looked upon favorably by most of the technical committee members of VITA (VME International Trade Association). But SSBLT subsequently came under attack as the proposed addition to the specification was more closely scrutinized. Criticism focused on two areas. First, the proposal called for using the rising edge of the signal, as opposed to the falling edge, which is used exclusively in the VMEbus 1014 specification. Second, because SSBLT is a source-synchronized protocol and doesn't use a handshake signal, timing parameters must nominally be set using a "worst-case" approach.

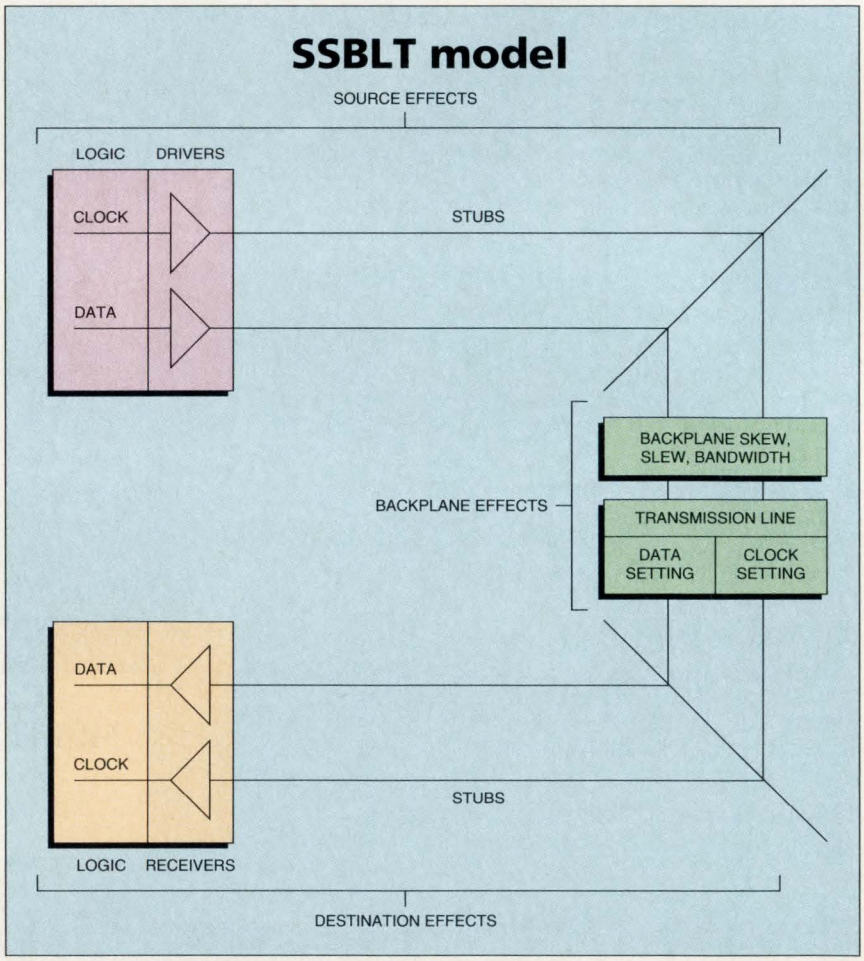
Some VITA members feared that rushing into a new specification before it's well tested could be an embarrassing mistake. "We certainly don't want to approve some specification that won't work, or won't be compatible with existing equipment," says Wayne Fischer, SSBLT proponent and director of strategic marketing for Force Computers (Los Gatos, CA).

Handling the worst case

The main criticism of the SSBLT proposal came from Dieter Nattkemper, former product manager for Openbus products for Newbridge Microsystems (Kanata, Ontario). "The 160-Mbyte/s transfer rate currently defined for the SSBLT protocol can't be achieved over VMEbus," he says. "The protocol takes an open-loop approach and, as such, doesn't have any handshake to guarantee successful completion of the cycles. The SSBLT protocol must guarantee reliable operation for the worst-case scenario; in effect, this would limit its performance to about 86 Mbytes/s, according to my model. The only way to reliably realize the promoted rate of 160 Mbytes/s would be to either redesign the physical interface of the VMEbus or limit the number of slots," Nattkemper concludes.

Performance Technologies (Rochester, NY), too, has done some preliminary analysis which tends to confirm the worst-case study done by Nattkemper. In addition, others have reviewed Nattkemper's model and find it accurate. Richard DeBock, leading engineer at Matrix (Raleigh, NC) and one of the original researchers of the VME specification, has looked at Nattkemper's figures and comments, "they [the timing figures] look a lot like mine"—referring to his initial timing definition of VMEbus.

Early in the debate Fischer was optimistic. "I feel totally confident that SSBLT will provide a tremendous advantage to VME, although I believe it will be necessary to do some heavy analysis and test," he said. He believed it might be necessary to adjust the mechanism somewhat, especially since the rising and falling edges of VMEbus signals are not, as defined, symmetrical. But



According to Newbridge Microsystems, the SSBLT model produces a number of delays, including source effects, backplane effects and destination effects. When considered in a worst case, these effects result in a significant slowing of the SSBLT protocol if reliability is to be maintained.

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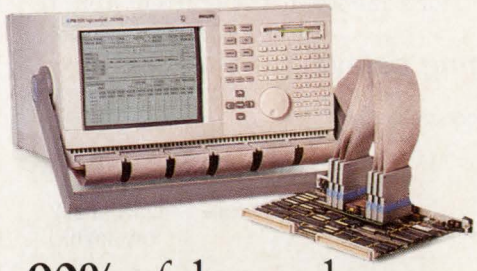

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this can be dealt with by using the data strobe lines DS0 and DS1 alternately, and the bus will still run at very high data rates.

A little adjustment

In the end—or at least thus far—a little adjustment is what both the proposed SSBLT approach and the VMEbus specification received. When Nattkemper's results were reviewed, they were seen to have some merit, but were criticized as being too pessimistic. But even strong proponents of SSBLT were willing to admit that the approach could experience problems in systems which implemented the VME specification as written.

Everyone was using the timing parameters described in the initial VMEbus specification for their SSBLT models. "But," comments Fischer, "the VMEbus specification was written more than ten years ago and the state of the technology, particularly for transceivers and backplane design, has changed. Systems made today—even those made a few years ago—use improved transceiver components, backplanes, boards, and, in truth, implement a much more robust version of the VMEbus specification than the original document calls for." Virtually all VME boards and systems built today implement the modifications called for by this more robust version of the standard. Also, boards built to either the old or the proposed revised version of the specification are fully compatible.

One significant modification calls for a change in drive current from 48 to 64 mA for all address and data lines. Although virtually all the drivers available today implement the 64-mA drive current, the specification still calls for the lower current. In addition, the new proposed specification calls for tighter threshold characteristics for the transceivers. The threshold will be reduced to 200 mV, with the low level (or 0) at 1.4 V and a high level (or 1) at 1.6 V. "This will bring the transmission characteristics closer to incident-wave switching, such as that used in Futurebus+," says Fischer. Though not a true incident-wave transmission system, the tighter parameters of the revised spec will clean up waveforms and remove the effects of reflections sufficiently that the SSBLT approach will be totally reliable. In addition, the SSBLT strobe has been moved from the beginning to the middle of the data period to further eliminate time quantization of data.

SSBLT timing delays

Source effects	- logic that generates data/clock (delta time)	5 ns
	- delta driver skew	5 ns
	- delta driver slew	1 ns
	- delta stub skew	1 ns
	Total=	**12 ns (max)**
		3 ns (min)
Backplane effects	- delta skew (delta velocity)	5 ns
	- delta slew (bandwidth limit)	1 ns
	- delta clock/data setting	33 (41) ns
	Total=	**39 ns (max)**
		0 ns (min)
Desitination effects	- delta stub skew	1 ns
	- delta receiver threshold	1 ns
	- delta receiver skew	5 ns
	- logic setup	3 ns
	Total=	**10 ns (max)**
		3 ns (min)
Other effects	- logic quantization time (50 MHz, 0.5 clk)	10 ns
	- logic hold	3 ns
	Total=	**13 ns (max)**

The source, backplane and destination effects produced by the SSBLT protocol result in a worst-case delay of 61 ns, which must be added to 13 ns from other effects. This mandates a significant timer delay—in the area of 55 ns to the standard VME timing. In total, source, backplane, destination, and quantization delays result in a combined delay of 126 ns.

Reduced capacitive loading

Besides the tighter transceiver specifications, the new proposal calls for reducing the capacitive board loading from 24 to 16 pF, and tightening the backplane impedance to make it look like 100 W. This lets the backplane take advantage of a transmission-line effect. Also, as part of the specification's amendments, a shielded DIN connector will be optional.

Though it appears the specification is headed for certain approval, there are still some in the VME community who are sitting on the fence. "I'd like to see the VME capability expanded, and certainly the type of transfer rates being discussed would be an advantage," says Pete Yeatman, president of Radstone Technology (Montvale, NJ). "But such an addition is going to have to be completely compatible with, and transparent to, the existing standard."

"The installed base," continues Yeatman, "is too large and too important to risk with an addition to the specification which may or may not work, or may or may not be fully compatible." While he sees some strong advantages to the faster transfer capability, Yeatman says he wants to make sure it's fully tested before it's incorporated into the specification. ■

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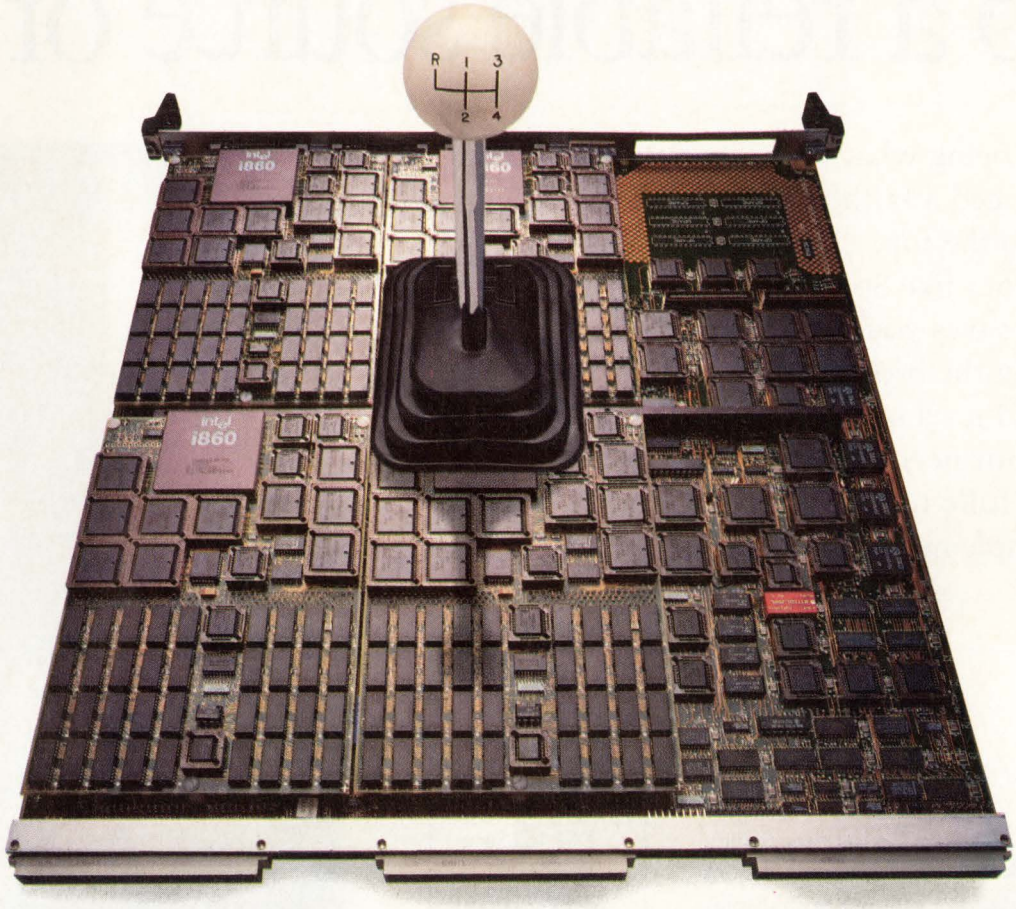

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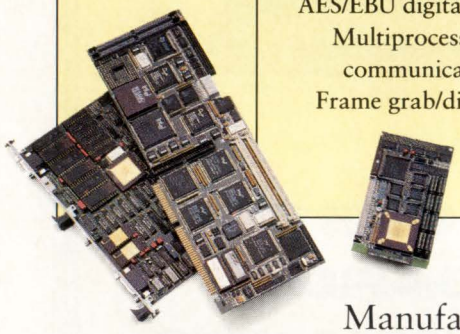

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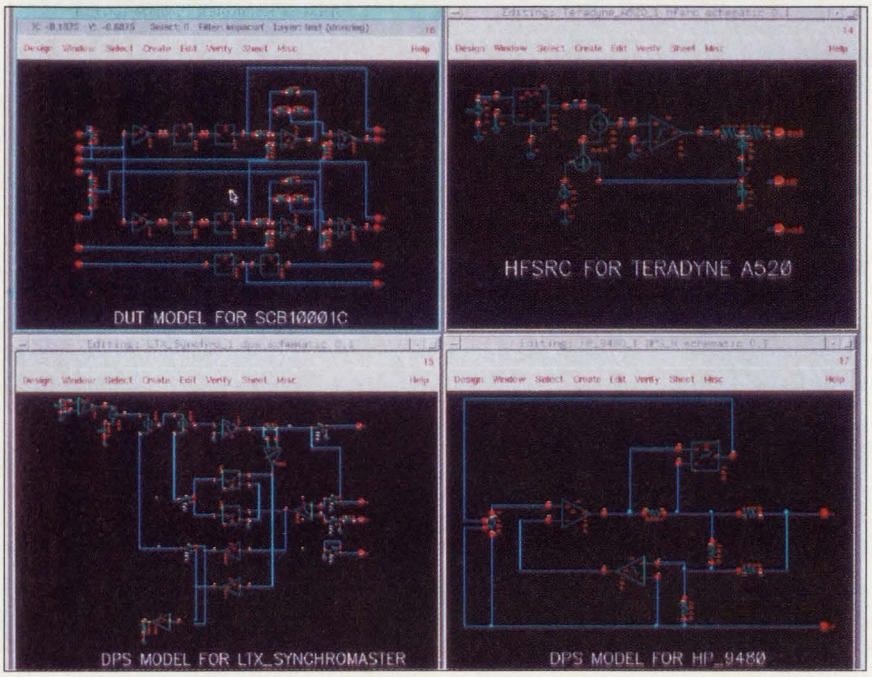
CAE/CAD TOOLS

Alliances help bridge the gap between IC design and test

Mike Donlin, Senior Editor



In this photo of Cadence's recently introduced Dantes tool, the upper left window shows a model of a device under test (DUT). The remaining three windows show tester resource models provided by several ATE vendors. The upper right window shows the model for the high-frequency source for the Teradyne A520. The lower left window contains the DUT power supply (DPS) model for the LTX Synchromaster. The lower right window shows the DPS model for the HP 9480.

The increasing complexity of ICs is making prototype verification and failure analysis more daunting than ever before. Trying to locate and probe a single transistor or even a bank of transistors in a sea of millions of components can challenge even the most sophisticated test systems. The obvious solution would be to use the design, layout and simulation data that was used to develop the device to guide the test equipment through the maze of components to find the suspect portion of the circuit. Test equipment and EDA vendors are beginning to work together to bring about such a link, but the going has been rough.

"Both the EDA and test industries grew up independently," says Thomas Sherby, chairman and CEO of Knights Technology (Santa Clara, CA). "Consequently, the tester people don't understand the EDA world very well, and the EDA people don't know how to interface their software to all the various pieces of equipment that make up a test area. A lot of valuable data that was developed during a device's design has never made it over to the test area simply because neither side wanted to take the time and use the resources to interface one to the other."

A recent alliance of Cadence Design Systems (San Jose, CA), Integrated Measurement Systems (IMS—Beaverton, OR), Knights Technology, and Wentworth Laboratories (Brookfield, CT) is geared toward breaking down the barriers that have separated these disciplines. The resulting system, which IMS calls the Analytical ProbeStation, gives test engineers the ability to observe and insert data into internal nodes of an IC while using CAE/CAD data to guide a probe to the suspect portion of a circuit.

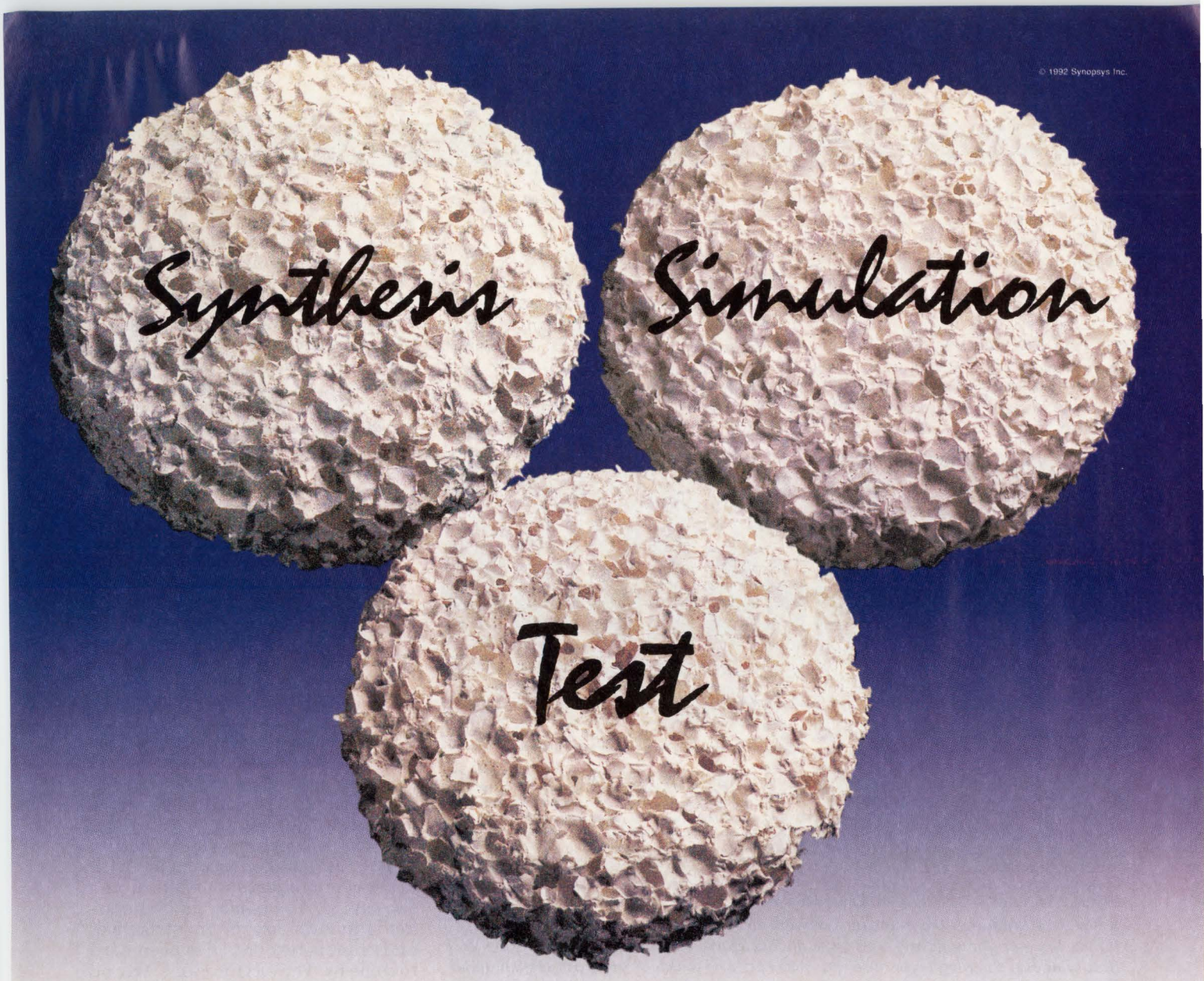
"Our customers have had difficulty integrating all of these separate elements in the past," says Steve Morris, director of marketing at IMS. "Companies have had to use teams of engineers to connect a test system to stimulate the device, a prober to test internal nodes, a floating table to reduce the effects of vibration, fixturing to connect the tester to the device installed in the prober, and software to automate probe positioning. This takes a lot of effort to get all the parts working together, and our customers are telling us they just don't have the resources to do that."

Connecting the pieces

The alliance that IMS has forged with Cadence, Knights and Wentworth brings together the various pieces of equipment and software to answer these complaints. The IMS portion of the package—its family of device testers—supports components with up to 448 I/O pins. Wentworth Laboratories provides its CAP-4000 programmable probe head with 0.1-μm resolution and a floating table to isolate the device from mechanical vibration. The CAP-4000 also controls a microscope mount for visual guidance and a laser cutter for passivation removal or machining vias to access buried layers.

Cadence's schematic, netlist and layout databases provide the front-end design information to the system, while Knights Technology is responsible for the software that ties the ProbeStation together. Knights' Merlin Framework lets you control a variety of post-silicon test and modification procedures from a Sun workstation. The software uses a multiwindow technique to let you view layout, netlist or schematic data to navigate the other portions of the ProbeStation to the feature of interest on the silicon. Additional windows let you view outputs from the test equipment, such as the image from the microscope, and to acquire, display, store, and recall signals for analysis.

"We think that this link between CAD data and physical test is especially important for analyzing today's complex circuitry," Knights' Sherby points out. "A typical microprocessor design has well over a million transistors. Trying to find a



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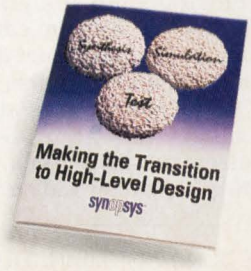

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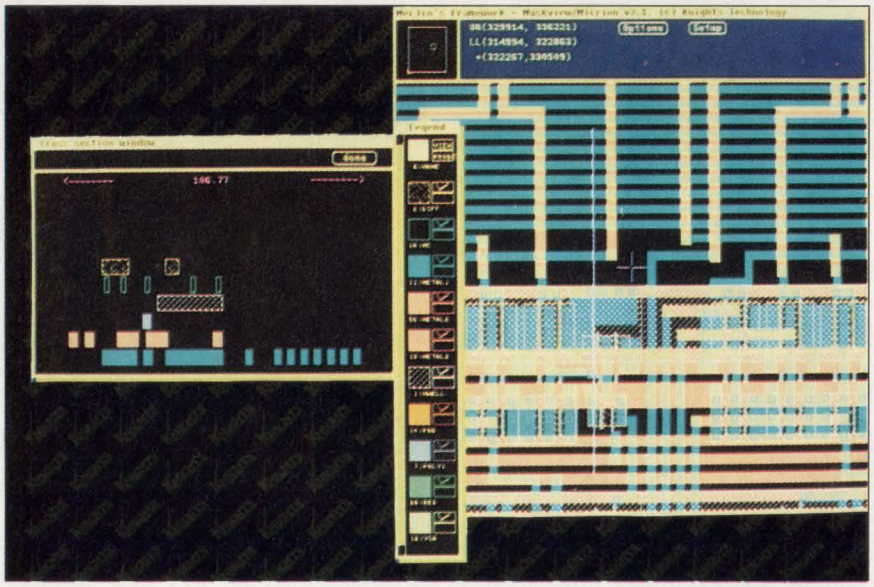
problem is like looking for a needle in a haystack. At least with this approach, we let you look at the whole haystack. After problems are isolated and solved, it's important to go back and change your CAD database so that the design information reflects the changes made."

Knights' software also works with E-beam equipment, which gives a more detailed view of the silicon under test and doesn't require physical contact with the device like a prober does. "We feel that E-beam and CAD integrated analytical probing are different and generally complementary, not competing technologies," says IMS' Morris. "E-beam equipment can be used in a dynamic imaging application to scan voltage contrast images of a faulty IC so it can be compared with a good IC. You can't do that with physical probers. On the other hand, there are several things that an analytical prober can do that an E-beam can't. A physical probe lets you insert data instead of just sensing it. It also lets you probe two or more nodes simultaneously and get very accurate voltage measurements. An E-beam needs a vacuum chamber and can cost as much as our entire system, about $400,000."



Knights Technology's Cross-Section Tool lets you draw a line on the silicon mask (white line in right window), and gives an idealized cross-section view of the device (left window) showing layer ordering, thickness and width of the cross-section under the selected line. The middle window gives a color-coded guide which shows what material is visible in the cross-section and lists its function. This information is useful when it's necessary to open holes in passivation or modify the device with a laser.

The ATE connection

Partnerships such as those forged by IMS focus on the probe and test of individual designs and single pieces of silicon, but there's also been activity in the automatic test equipment arena to bridge the gap between high-volume device testing and CAE data. Cadence has recently unveiled Dantes, an analog and mixed-signal design-to-test product. Dantes is a bidirectional design and test environment which integrates Cadence's Analog Artist Design System into the ATE environment, a coupling which lets you incorporate test specifications early in the design cycle.

"The test development process for analog and mixed-signal circuits is an area where little progress has been made," says Thomas Quan, director of analog IC solutions at Cadence. "In the digital arena, widely accepted testability metrics have been developed. But for analog and mixed-signal designs, the IC vendor's test engineer is still required to interpret the design specification. The engineer must construct test hardware and generate code for ATE to properly verify functionality and parametric performance. This labor-intensive effort can often delay prototype development and product shipment, which, in turn, increases costs."

Dantes was developed in cooperation with several leading ATE vendors, who provided tester-specific information that can be ported to the design phase of the device. At present, Dantes can generate source code for the Teradyne A500 series of testers as well as the LTX Synchromaster, the Hewlett-Packard 9480 and the Yokagowa TS-1000. The tools in the suite include a test rule checker to ensure that designs will be testable once they reach the tester floor; a composer tool to assist in the development of the device under test loadboard design; a test sequencer to order and prioritize tests; and test program generators to automatically create test programs.

Though the IMS partnership and the Cadence software target different portions of a device's design cycle, they both signal a trend in the IC industry. Test bottlenecks have long been the bane of both design and test engineers, who've had to work in isolated environments with little communication between the two camps. As a result, time-to-market windows are often stretched, and reliable test data has been hard to come by. The alliances of CAE and test vendors must certainly be welcome for designers who want to make their designs testable and for test engineers who want to ensure that their test vectors are accurate and exhaustive.

But, integrating the needs of design software vendors, the ATE community and leading IC houses will remain a challenge for some time, because until recently each assumed the burden of testability was the responsibility of the other. ■

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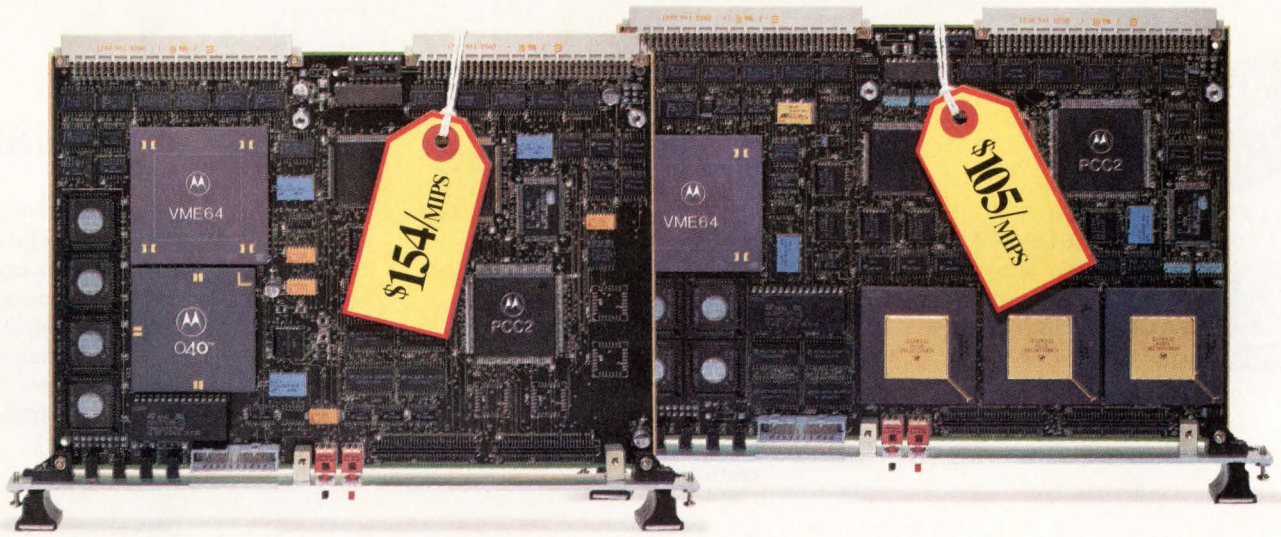

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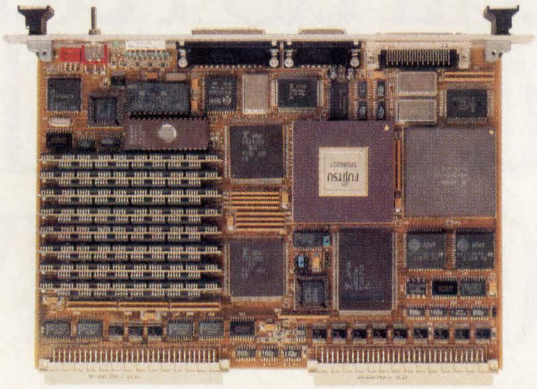

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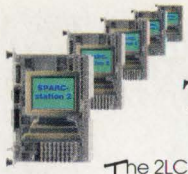

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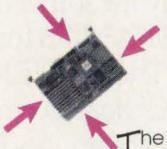

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CIRCLE NO. 40

Peripheral interfaces offer fast networking solutions

HiPPI and Fiber Channel may have been defined as peripheral interfaces, but designers are taking advantage of their high data transfer rates to solve their networking problems.

Warren Andrews,
Senior Editor

Broadband Communications is releasing a new HiPPI-to-fiberoptic module for OEMs to use on board- and system-level products. Broadband president Jim Toy points to the compact size of the new module and says it will fit on many standard board architectures or motherboards.

High-speed processors and complex applications demand more from a system's memory subsystems and I/O interfaces. With processor clock speeds running at better than 50 MHz—and going up all the time—and the increasing emphasis on graphics, imaging, multimedia, and hypermedia, the amount of information to be transferred from one subsystem or processor to another is enormous.

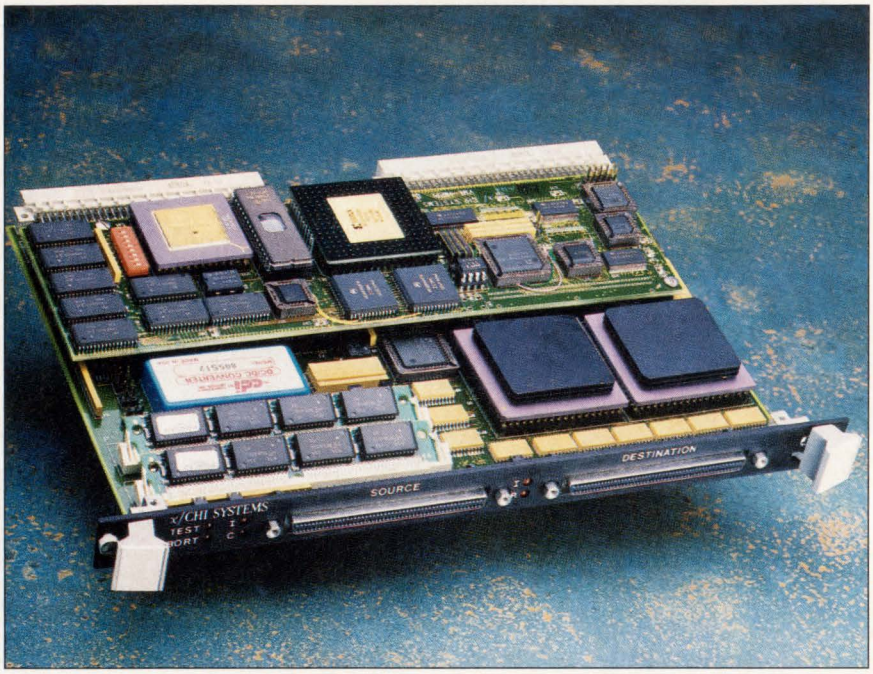
In response to these very high-speed data transfer requirements, fast copper-cable and fiberoptic interfaces are starting to emerge. While some follow protocols such as SCSI, HiPPI and Fiber Channel, others are basically proprietary—their manufacturers are not waiting for the resolution of standards issues. And, protocols such as HiPPI and Fiber Channel were defined for peripheral interfaces, there's a growing tendency to take advantage of their high data-transfer rates for larger network interfaces such as LANs.

"The idea behind any peripheral interface," says Joel Silverman, marketing manager for commerical products at Radstone Technology (Montvale, NJ), "is to move data as quickly as possible from the host or subsystem to the peripheral and back. Also, the architecture of the host bus adapter must be suited to swapping data across the peripheral bus with as little overhead as possible on the main system bus or main processor."

For the SCSI-1 generation, with a maximum transfer rate of only about 5 Mbytes/s in a synchronous mode, even moderate demands can keep the SCSI bus busy; all that needs to be done is to isolate the SCSI channel from the host bus. But the emergence of SCSI-2 (see "The emergence of SCSI," p 65), with its attendant fast and wide interface, has let data rates reach

20 Mbytes/s for a 16-bit bus width and 40 Mbytes/s for a 32-bit bus width. Such rates are at the theoretical limit for VMEbus transfers, and far exceed real-world transfer rates; in many traditional applications, they can't be utilized at either the source or destination.

But this scenario will change rapidly as new technology invades the traditional I/O world. RAIDS (Redundant Array of Inexpensive Drives) approaches, for example, are surfacing that are capable of using bandwidths of 40 Mbytes/s and more. And devices such as scanners, high-speed printers and other



Chi Systems is one of the only companies to make a HiPPI interface on a standard VME module. Says company vice-president Douglas Felder, "While our VME board fits the bill well in many applications, SBus, with its faster transfer, can better take advantage of HiPPI capabilities."

subsystems tied into the I/O interface will continue to make new performance demands.

With the introductions of fast and wide SCSI and a number of interface chips from the major manufacturers supporting this latest revision, SCSI is holding its own in many traditional applications such as disk drives. "In many system applications," says Silverman, "SCSI can even be used as a small network where other networks such as Ethernet or token ring approaches are too expensive or complex."

SCSI will undoubtedly continue to be an industry leader in many application areas for quite some time. But there are many other areas where even the fastest SCSI performance doesn't come close to matching system needs. Very high-performance RAIDS arrays, for example, are capable of bursting data at rates far faster than current SCSI allows. Also, to solve real-time (and not-so-real-time) high-resolution imaging problems, technologies faster than SCSI have had to be developed.

A supercomputer start

Not unexpectedly, many high-speed I/O interfaces were born in the supercomputer world. HiPPI, one of the first standard high-performance I/O interfaces, got its start as a "high-speed channel (HSC)" project undertaken by a group including Cray Research, IBM and Los Alamos National Laboratories. The project, subsequently adopted by ANSI, became the X3.183.199X High-Performance Parallel Interface, with both the HiPPI and HiPPI acronyms deemed correct. Cray Research was one of the first implementers of the approach.

HiPPI is defined as an I/O channel supporting a bandwidth of 800 Mbits/s, with an alternate transfer rate of double that—or 1.6 Gbits/s, achieved by doubling the bus width from 32 to 64 bits. The primary design goal of HiPPI is to provide a point-to-point channel between CPUs, and from CPUs to storage systems, printers and other peripherals. Its specification calls for 32 data lines, four parity lines and an assortment of control lines in each direction. It also defines many layers, including a physical layer, framing protocol, link encapsulation, memory interface, and switch control. In addition, the ANSI Committee is busy looking at other protocols to include in the specification.

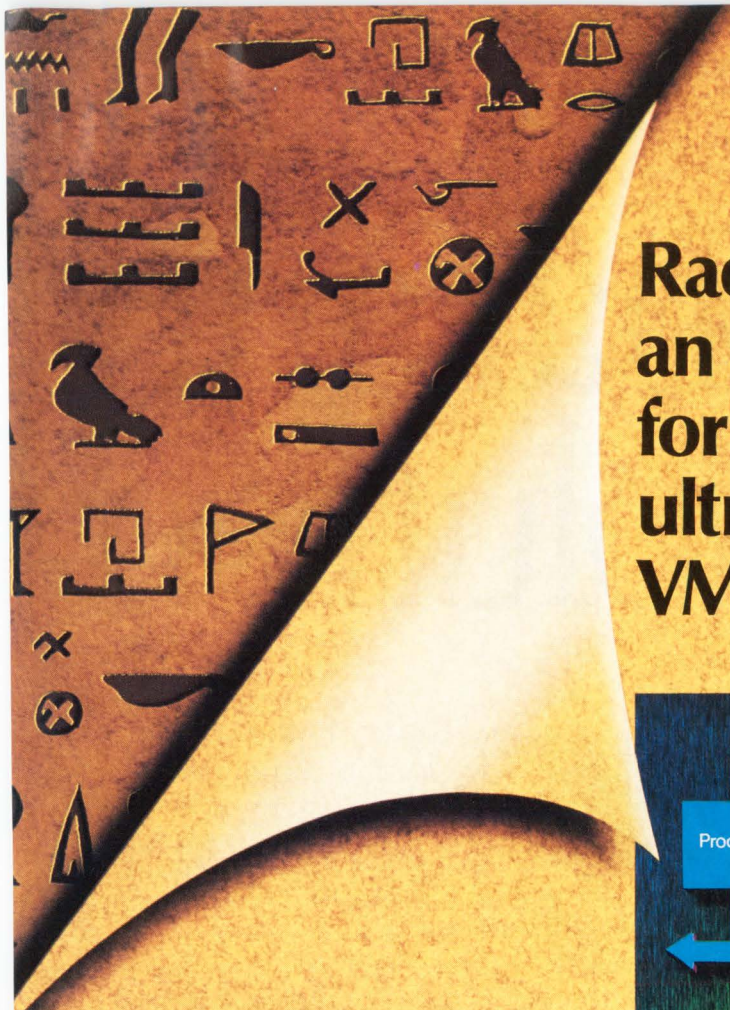
HiPPI was initially designed to be implemented with relatively inexpensive, readily available components to encourage rapid acceptance by a large number of users. But those same factors, along with the need for a large bundle of copper wires (almost 100 for a 32-bit bidirectional connection) and a limitation on distance to less than 25 m, may well limit the lifetime of traditional HiPPI and pave the way for other approaches.

Alternatives such as fiberoptic versions of HiPPI are already emerging, and the committee assembling the Fiber Channel specification is in the process of adding HiPPI protocols as a subset of its document. "But," says Jim Toy, president of Broadband Communications (Melbourne, FL), "the practical implementation of Fiber Channel is still a ways off, and HiPPI, particularly as implemented in optical fiber, will continue to be a major winner."

Growing base of users

HiPPI is currently in use—or under development—by most of the major supercomputer makers, including Convex, Cray Research, Digital Equipment Corporation, IBM, Intel Supercomputer, Network Systems, Thinking Machines, and others. Although the interface hasn't yet made its mark on smaller systems, Sun Microsystems has been participating in developing the specification—the only workstation maker to do so—and IBM is reportedly looking at a HiPPI interface for its RS/6000 family, as is Silicon Graphics.

"HiPPI is a very convenient way to interconnect major subsections of a system with the kind of transfer rate needed for things such as real-time graphics," says Jim Hanlon, director of marketing for IOTEK (Halifax, Nova Scotia). "Our system comprises two units: a powerful signal processor and a high-resolution display processor. Because of the tremendous amount of data that has to flow between the two units, we



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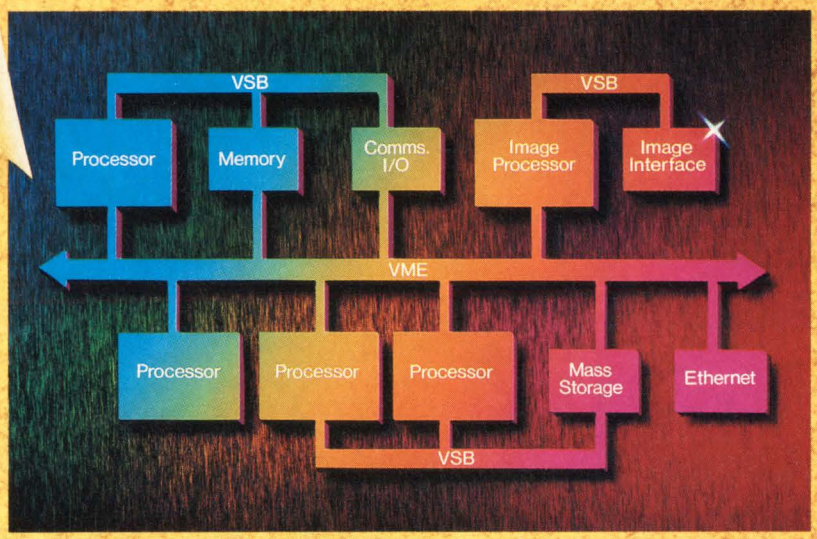

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had to find a high-speed I/O channel and HiPPI fit the bill. And, since the two units are always in the same room and never more than several feet apart, the relatively low cost and straightforward approach of the copper cable works well. But it's good to know that a fiber version is available, just in case circumstances should warrant it."

On standard platforms

Because of its growing use in a variety of systems other than supercomputers, HiPPI has spawned some high-performance board and module products. Chi Systems (Pleasanton, CA) was the first to implement a full HiPPI interface on VMEbus, and now offers 9U versions for Sun-based systems as well as a recently released 6U version. Chi's background is in software and hardware for high-performance data acquisition systems, many of which are built for large government projects.

Says Douglas Felder, vice-president of sales and marketing at Chi, "Our present commercial VME products emerged from some very specific high-end, high-speed data-acquisition government projects. But VME is still relatively slow and we're currently working on an SBus version of our HiPPI adapter. Because the transfer rate of SBus is much greater than that of VME [160 Mbytes/s versus 40 Mbytes/s for standard VMEs, 80 Mbytes/s for VME64], it makes much more sense to connect HiPPI to the SBus than VME. This is particularly true in the Sun workstation arena, because Sun does not support a block transfer on VME and, therefore, the throughput is very slow." To handle the requisite circuitry and connector on the very small form factor SBus card, Chi Systems will have to use two SBus slots for its SBus-to-HiPPI adapter.

"In putting together our HiPPI products, we're defining and developing specific hardware platforms and adding critical software components," says Felder. "For example, the company offers drivers for Sun machines and Silicon Graphics workstations, as well as drivers for such networking protocols as TCP/IP. In addition, we're doing some custom interfaces in conjunction with a consortium known as the National Storage Lab."

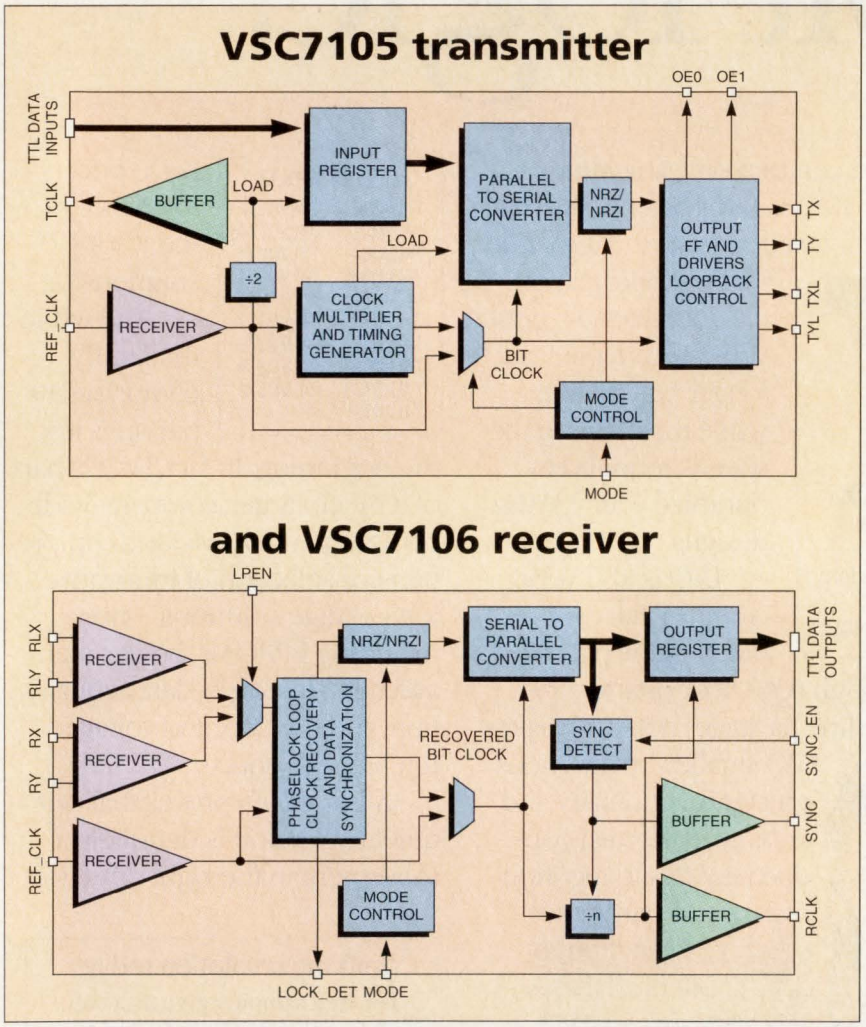
The National Storage Laboratory—a group of companies working with Lawrence Livermore Laboratories and including Ampex Tape Systems, General Atomics, IBM Federal Systems, IBM Storage Systems, Maximum Strategies, Network Systems, and Zitel—is putting together a test bed of storage devices tied together with a HiPPI interface. The object is to demonstrate that it's possible to transfer data to and from mainframes and workstations at HiPPI rates.

"Until now," explains Felder, "such transfers were limited to FDDI [Fiber Distributed Data Interface] raw data rates of 10 Mbytes/s. Now we're able to increase that by an order of magnitude, to 100 Mbytes/s. Chi is participating in the project by providing Sun-, Silicon Graphics- and Zitel-to-HiPPI interfaces. In addition, we're also supplying the upper-level protocol for IPI-3 to run over a HiPPI interface."

The next step

Despite the seeming success of HiPPI, it hasn't yet achieved wide acceptance outside the fringe of supercomputer makers. Cabling requirements and distance limitations make it difficult to implement in the workstation environment. In response to these limitations, board- and module-level products are starting to emerge that provide conversion from parallel HiPPI to serial fiberoptic format.

Broadband Communications is one of the leaders in this area, currently offering a box-level product and having just introduced a compact module. The box-level product, its Model 1200 fiberoptic HiPPI extender, receives standard parallel HiPPI signals and converts them to serial fiberoptic out-



Vitesse is working with partners Interphase and Seagate on a new Fiber Channel system. Functional blocks of the transmit and receive nodes indicate the primary functions required for a Fiber Channel node.

ZIATECH CORPORATION

CONTROL POINT

Test and Control Product News from Ziatech Corporation — Summer 1992

First

CREDIT CARD SIZE I/O AND FIXED MEDIA ON STD BUS

A new STD 32 interface accepts two rugged, removable, business card sized PC Card™ modules.

Credit card sized memory and I/O devices that adhere to the PCMCIA standard can be plugged into any STD system via a new STD 32 interface, the ZT 8921. Compact, low-power modules called "PC Cards" can be conveniently installed and removed at any time, even during system operation.

A ZIATECH FIRST

Ziatech, with its ZT 8921 PCMCIA 2.0 Interface, is the first

continued 4

Low-Cost SBC Hosts Extensive Features

Ziatech's new ZT 8801 is a low-cost, STD Bus computer with a unique combination of I/O ideal for control applications. It provides a low-cost, very compatible alternative to Ziatech's V53-based processor card, the ZT 8901.

V40 CPU, LOADS OF I/O

Its NEC V40 processor is code-compatible with the Intel 8088 CPU and features DMA support, an interrupt controller, three counter/timers, and a serial channel integrated with the core processor.

SBX, RAM AND ROM

The serial channel onboard is configurable to RS-232 or RS-485 standards and is complemented onboard by up to 48 points of Opto 22-compatible digital I/O, an SBX connector, and up to 512 Kbytes of EPROM or Flash Memory, and up to 1 Mbyte of RAM.

continued 3

INSIDE

- STARWindows DDE/Console
- NetBIOS in a Box
- New STD 32 Enclosures

ZIATECH CORPORATION

STAR SYSTEM Gains NETBIOS–

NETBIOS® SIMPLIFIES INTERPROCESSOR AND NETWORK COMMUNICATION

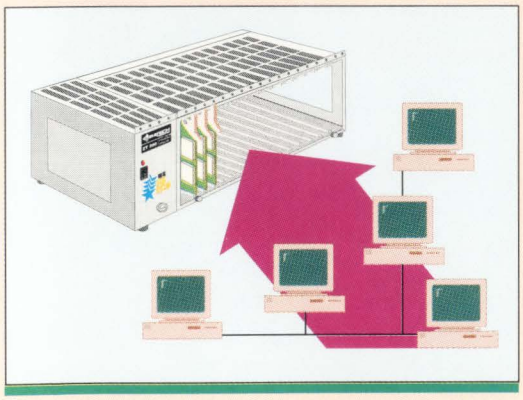
New NetBIOS compatibility in the STD 32 STAR SYSTEM™ provides a standard software interface for communication between multiple processors in this STD 32 system. NetBIOS also allows STAR SYSTEM processors to easily communicate with other nodes in a local area network (LAN). Both of these new capabilities shorten the development time of multiprocessing applications requiring interprocessor communications, and make these applications portable to other NetBIOS-compliant systems.

STD 32 STAR SYSTEM HOST

The STAR SYSTEM allows up to seven DOS-based processors to operate in a single enclosure, with equal access to system peripherals such as disk drives, video, and industrial interfaces. The STAR SYSTEM's NetBIOS approach complies with the STD 32 specification for interprocessor communication (IPC). The IPC also uses the NetBIOS standard.

NETWORK IN A BOX

The availability of NetBIOS on the STAR SYSTEM brings standard network functionality to this unique multiprocessing system.



NetBIOS-compliant LANs can now be replaced by one STD 32 STAR SYSTEM.

NetBIOS carries out communication services on a network in the same way the BIOS in a desktop PC provides support for disks, terminals, and keyboards.

REACH BEYOND THE STARS

With NetBIOS compatibility, each processor within a STAR SYSTEM "looks" like a network node to other processors in the system. When a network card is installed in this STD 32 system, third party software running on STAR SYSTEM processors can use NetBIOS to communicate with processors on a LAN outside of the system. NetBIOS not only provides this transparent communication between the multiprocessing system and/or the LAN, but its standardized interface also simplifies the programmer's task.

BRINGS NEW PRODUCTS TO THE STAR SYSTEM

A growing supply of control-oriented software programs, such as GENESIS (ICONICS, Foxborough, MA), GELLO (Event Technologies, Indianapolis, IN), and DOS NX (On-Line Systems, Kitchener, Ontario, Canada), are NetBIOS-compatible, further streamlining the implementation of multiprocessing control applications on the STAR SYSTEM.

NetBIOS compatibility in the STAR SYSTEM lets users of NetBIOS-compliant LANs easily condense their application from several industrial or personal computers to a single multiprocessing STAR SYSTEM with minimal software reprogramming.

This NetBIOS capability is now supplied with all STD 32 STAR SYSTEMS at no extra charge.

(Request a STAR SYSTEM data sheet on the Control Point return card.)

NetBIOS software on the STD 32 STAR SYSTEM shortens development time.

A Window to the Stars–

STD 32 STAR SYSTEM™ DEVELOPS WINDOWS®

A new software option to Ziatech's STD 32 multiprocessing system provides a window for each processor on the system console, and allows processors to exchange data with Microsoft® Windows® DDE-compatible programs such as Microsoft Excel®.

A STAR CAST

The STAR SYSTEM uniquely accommodates up to seven DOS-based processors in a single system, condensing the multiple PCs and peripheral sharing qualities of a LAN into a single, compact unit designed for real-time control applications. The STARWindows software option includes Microsoft Windows, STARWindows Console, and STARWindows DDE (Dynamic Data Exchange) Server.

WINDOW WITH A VIEW

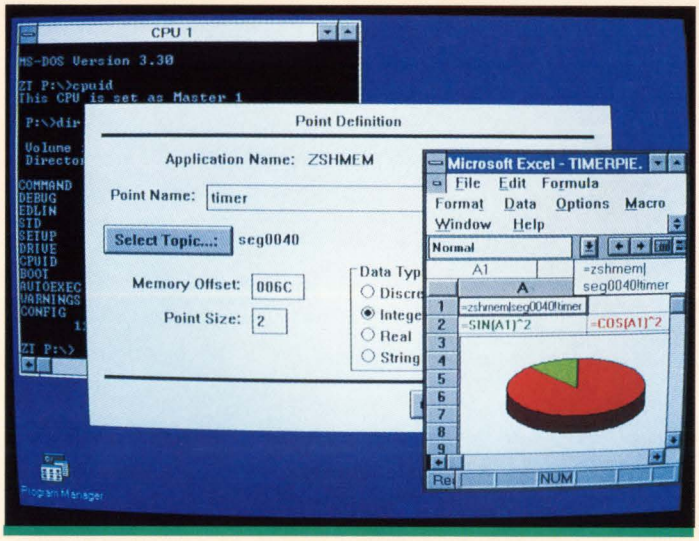
The STARWindows Console allows a window in the Microsoft Windows environment to serve as a console for each processor in the system.

STARWindows Console supports popular development programs such as Microsoft QuickBASIC® and Borland's Turbo-Debugger®, making it an effective design tool for implementing real-time multiprocessing systems. This utility is equally helpful in the final target application, where it lets a single user interface "look" at multiprocessor activity.

EXCHANGE SERVICE

STARWindows DDE Server incorporates the Windows DDE message passing protocol, allowing STAR SYSTEM processors to share data with other processors running Windows programs. The STARWindows DDE Server includes an interactive configuration utility that simplifies system configuration by defining data types and assigning shared memory addresses.

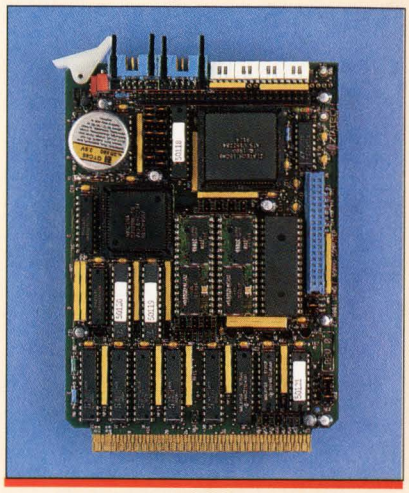
(Request STARWindows info on the Control Point return card.)



This screen shot of the STARWindows Console and DDE software shows CPU output in a window concurrent with interprocessor data exchange.

Low-Cost SBC Hosts Extensive Features

(continued from page 1)



ZT 8801 Single Board V40 Computer offers many features.

SOFTWARE SUPPORT

The new single board computer is supported by Ziatech's STD DOS and STD ROM software environments. Common I/O software support is provided by Ziatech's STD Device Driver Package (STD DDP).

The ZT 8801 is also available in a low power, extended temperature version (ZT 88CT01).

FAMILY OF PROCESSORS

The ZT 8801 joins a large family of Ziatech processor choices ranging from low-cost products featuring the NEC V20 to high-end Intel processors.

(Request a ZT 8801 data sheet on the Control Point return card.)

ZIATECH CORPORATION

STD 32® BUILT TOUGH AND TINY

New Enclosures Make Ruggedness More Accessible

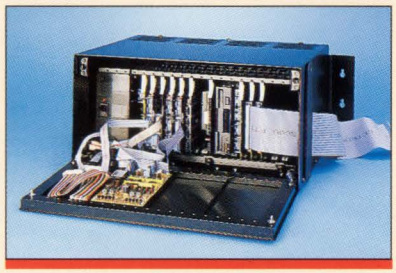
The new ZT 250 and ZT 300 Industrial Computer Enclosures are designed for reliability in harsh environments.

INDUSTRIAL TOUGH

By enclosing a low-noise STD 32 backplane, the ZT 250 and ZT 300 protect signal integrity and allow reliable operation during shock, vibration, and 0° to +70° Celsius temperatures. The corrosion-resistant steel card cage allows for efficient ventilation and cable routing while providing system-level protection from falling debris.

UNIQUE I/O

The front panel on these enclosures hinges down for complete accessibility. Individual I/O plates, which make up the front panel, can be optionally equipped with connectors, signal conditioning boards, and cables for I/O.



Both enclosures have hinged front panels for easy access.

DIVERSE USES

The ZT 250 has a small footprint for 12" NEMA cabinet installation. It is convection cooled and can be panel, desk, or pedestal mounted.

The ZT 300 is 19" rack-mountable, has dual fans, and holds card cages of up to 24 slots.

(Request ZT 250/ZT 300 data sheets on the Control Point return card.)

The ZT 250 and ZT 300 offer 9- to 24-slot STD 32 backplanes, removable I/O plates, mounting options, and steel construction.

Credit Card Size I/O and Fixed Media *(continued from page 1)*

company to offer the "PC Card" standard on the STD Bus. The ZT 8921 features dual PC Card support, hardware and software resets, a 16 Kbyte PROM socket for BIOS extensions or other code, and support for multiple ZT 8921 interfaces in a single STD system.

The ZT 8921 comes with Microsoft's Flash File System Version 2.0 (FF2) device drivers.

TOUGHEST ON THE BACKPLANE

PC Card-based memory and I/O installed in the ZT 8921 are resistant to shock, vibration, and temperature extremes that hamper standard peripherals in such environments.

UNLIMITED ABILITIES

A variety of PC Cards exist for the ZT 8921. Flash, SRAM, ROM, OTP, and EEPROM memory cards, modems, and local area network interfaces are some of the PC Cards offered in this increasingly popular format.

(Request a ZT 8921 data sheet on the Control Point return card.)

CONTROL POINT

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The emergence of SCSI

What started in the early 1980s as a simple disk-drive interface has developed into an interface capable of interconnecting many different device types over a wide range of computer platforms. SCSI was born when Shugart Associates, a manufacturer of disk drives, designed a simple parallel I/O bus called the Shugart Associates System Interface (SASI). The company's goal was a low-cost interface for connecting disk drives to small computers.

In late 1981, SASI was turned over to the ANSI X3T9.2 Committee, and then it was renamed the Small Computer Systems Interface (SCSI). The SCSI-1 specification was completed in 1984 and finally approved and published in 1986.

SCSI-1 to SCSI-2

SCSI-1 had a number of limitations that SCSI device manufacturers addressed in various nonstandard ways. The X3T9.2 Committee soon started work on SCSI-2 to address these limitations. However, what was to be a quick effort to improve the SCSI command set and support devices other than disks turned into major enhancements to SCSI-1.

The changes to SCSI were many. Fast SCSI increased the data transfer rate to 10 Mbytes/s for 8-bit transfers and up to 40 Mbytes/s for 32-bit transfers. Bus arbitration was added to support multiple initiators. New commands, messages and command queuing were added to support other device types and aid in managing the SCSI bus. Members of the Committee worked on cabling, termination and connectors to make SCSI more reliable and easier to implement. SCSI-2 now supports disk, tape, CD-ROM, optical drives, printers, scanners, and other devices. In fact, not only are these devices supported in the SCSI-2 specification, but they can all coexist on the SCSI bus.

The SCSI connection

SCSI consists of two to eight devices connected to an I/O bus. Each device is either an initiator, a target or both. The initiator sends commands to a target to perform an action. A simple example is a computer (the initiator) sending a read block command to a disk drive (the target). The drive responds by reading the area of the disk specified in the command descriptor block and transferring the data read back to the computer.

At a minimum, the SCSI bus needs one initiator and one target. It becomes more powerful as more devices are added. A typical configuration has one or more disk drives, a tape drive for backup and a CD-ROM drive. These are all target devices that connect through a SCSI host adapter (initiator) to the computer system. A more advanced configuration involves multiple host adapters sharing target devices.

The host adapter communicates with a target device by placing its SCSI ID along with the ID of the target on the bus. The target responds when it sees its ID and an I/O process begins. The initiator sends a command descriptor block plus any messages needed to handle the command. The target has the option of staying on the bus (staying connected to the initiator) and performing the requested command or breaking the connection (disconnect). A disk drive may disconnect when it needs to move read/write heads to a new area on the disk to read/write the requested data. Since this may take several milliseconds, disconnecting frees up the bus for other devices. At this point the initiator is free to send commands to other targets. When the target has its data ready, it reestablishes the connection with the initiator and sends the data. At the end of the operation the target sends status information to the initiator with the completion results.

The physical SCSI bus

The SCSI bus is a parallel bus consisting of nine control signals, eight data signals and one parity signal, along with termination power and ground signals.

SCSI-1 defined a 50-conductor cable that is also used in SCSI-2. SCSI-2 defines an additional 68-conductor B-cable that extends the data bus to 32 bits (from 8 bits) to increase the data transfer rate. A new cable configuration, called the P-cable, is a single 68-pin conductor cable that contains 16 data bits. This seems to be the configuration of choice because of its single-connector design, which easily fits on the current small SCSI disk drives. Unfortunately, the P-cable wasn't introduced in time to become part of the SCSI-2 standard.

SCSI defines two types of electrical connections: single-ended and differential. Single-ended references each signal to a common ground and has a maximum length of 6 m. Differential uses two wires per signal, which improves noise immunity and extends the cable length to 25 m. Single-ended is used when all the connecting devices are within the same cabinet. Differential is used when devices extend to multiple cabinets.

Differential comes with some disadvantages. It consumes more power and requires more real estate on the printed circuit board. Additional board space is needed, because most SCSI protocol chips support single-ended internally but require external devices for the differential driver/receiver.

Every good bus must come to an end and SCSI has two of them. Terminators must be placed at each end of the SCSI bus to reduce signal reflections. SCSI-1 defined a simple 220/330-Ω passive terminator. SCSI-2 defines an active terminator that consumes less power and provides a better impedance match. Proper cabling and termination are vital to proper SCSI operation.

The future of SCSI

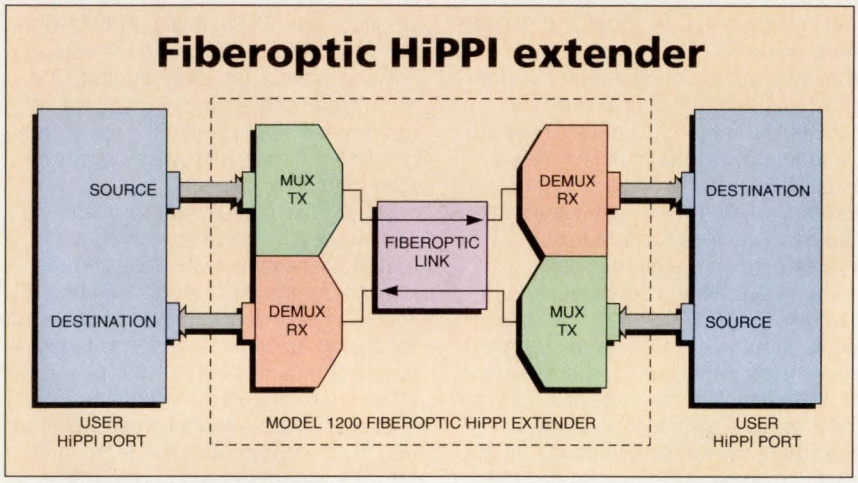
Adaptec and several other companies comprise the X3T9.2 Committee driving SCSI standards. Work on SCSI-2 is finished and the standard is out for public comments, a process that will conclude in July 1992. The Committee has already begun work on SCSI-3. The goal is to provide compatibility with SCSI-2 devices and to move the device-dependent intelligence out to the SCSI-3 devices.

SCSI-3 will support the current parallel I/O bus as well as define a new serial interface. Serial SCSI uses the same phases, commands and messages as SCSI-2, but this information is encoded and sent in the form of packets across the serial interface. While the Committee hasn't chosen the physical serial interface (Fiber Channel, P1394, or some other), "packetized" SCSI lets you send information faster and more reliably. In the end, SCSI-3 may define multiple serial interfaces which will extend the power of SCSI to more devices and over greater distances.

Thomas Newman, engineering manager, peripheral products operation, Adaptec, Milpitas, CA

put. The unit multiplexes data and control signals to a 1.1-Gbaud serial link; the signals are then demultiplexed and reconstructed at the receiving end.

"The interface," says Broadband's Toy, "is virtually transparent, but provides the capability to transmit at distances up to 15 km, as opposed to the 25 m conventional HiPPI is restricted to." Combined with the reduced bulk and high reliability—the typical BER [bit error rate] is 10^{-14}—of fiberoptic transmission, the approach provides many advantages. But the cost of such implementations isn't low. Broadband's HiPPI extender cost more than $25,000.



Broadband Communications' current fiberoptic HiPPI extender comprises the multiplexing and demultiplexing blocks, which serialize the parallel HiPPI data and control signals and feed them to a fiberoptic transducer. In reverse, the signals are picked up off the cable, decoded and sent on to their destination.

But prices are coming down rapidly and the circuitry is becoming more compact. Adds Toy, "The features of the stand-alone HiPPI extender are now available in compact module format for incorporation by OEMs onto standard or custom board-level products."

Life after HiPPI

Life after HiPPI seems to be thriving, and, in fact, Fiber Channel, another emerging ANSI standard (ANSI X3T9.3), is targeted to be compatible with—or a superset of—existing HiPPI. "HiPPI is here now and in use with a growing base of users," says Felder. Fiber Channel, because of its superior transfer rate (pegged at 1.0625 Gbits/s and above), will probably start to encroach on HiPPI sockets after the standard stabilizes. "But that's still at least two years away," Felder adds.

Felder believes that HiPPI's lifetime will be extended with fiber, and it will remain the preferred interface standard for at least the immediate future. Interestingly, the same factors that will make serial HiPPI less expensive and more widely used will also benefit Fiber Channel. These are a high-speed parallel-to-serial data link and fiberoptic transducers.

The most recent introduction providing a full Fiber Channel parallel-to-serial and serial-to-parallel interface comes from gallium arsenide specialist, Vitesse Semiconductor (Camarillo, CA). Called the G-TAXIchip, Vitesse's product is a GaAs version of a chip set developed a few years ago by Advanced Micro Devices (Sunnyvale, CA), which it called its TAXIchip. Vitesse's GaAs version is designed to operate at the 1.0625-Gbit/s rate of Fiber Channel, and can also operate at a rate of up to 1.25 Gbits/s in other proprietary schemes.

TAXI?

"Originally the AMD TAXIchip chip set was targeted at only 100-Mbit/s rates for point-to-point communication and was not designed to address a particular protocol standard," says Bob Nunn, Vitesse marketing director. "When we designed the G-TAXIchip, we wanted to conform to the emerging Fiber Channel standard." This design includes a coding scheme for serializing parallel data and encode, as well as setting up a number of serial strings that are used as control characters.

"For example," Nunn continues, "there's something known as an idle pattern which, when no data is being transmitted across the link, the link will automatically transmit so the receiving end knows that there is nothing coming across. In addition, there are other mechanisms for sending interrupt and error messages which had to be included in the chip set."

The Fiber Channel standard provides for uniform overhead and a common way for everyone to treat that overhead. Using the approach, different devices, such as a workstation and a disk drive, can talk to each other without either one knowing any more about the connection than the basic Fiber Channel rules.

"Similarly," continues Nunn, "HiPPI was defined only as a parallel, rather than a serial, interface." Because there are some differences in the way HiPPI and Fiber Channel manage information, there's currently no direct translation from parallel to serial HiPPI. "There is, however," says Nunn, "an ad hoc committee—a group of interested companies acting outside the ANSI body—attempting to define a serial HiPPI standard. This group has come up with its own overhead and encoding requirements."

Either/or

"Our chip set will support serial HiPPI but it will require additional chips to conform to those standards—some kind of formatting logic," Nunn says. He explains that Vitesse developed its four-chip set so that the two high-speed devices could interface with a number of different encoder or multiplex/demultiplex chips. To create serial HiPPI, the basic transmitter and receiver can be mated to a discrete circuit or gate array mux/ demux circuit. The mux and demux for the existing G-TAXIchip chip set are basically gate arrays with Fiber Channel protocols; they could be modified to handle HiPPI protocols.

"Looking into a crystal ball, I believe Fiber Channel will overcome serial HiPPI applications just because it's [Fiber Channel] supported as the standard communication protocol by ANSI," says Nunn. And because he believes this transition from HiPPI to Fiber Channel is imminent, he says Vitesse has no plans at this time to develop or market standard HiPPI protocol chips.

"There are a number of people that

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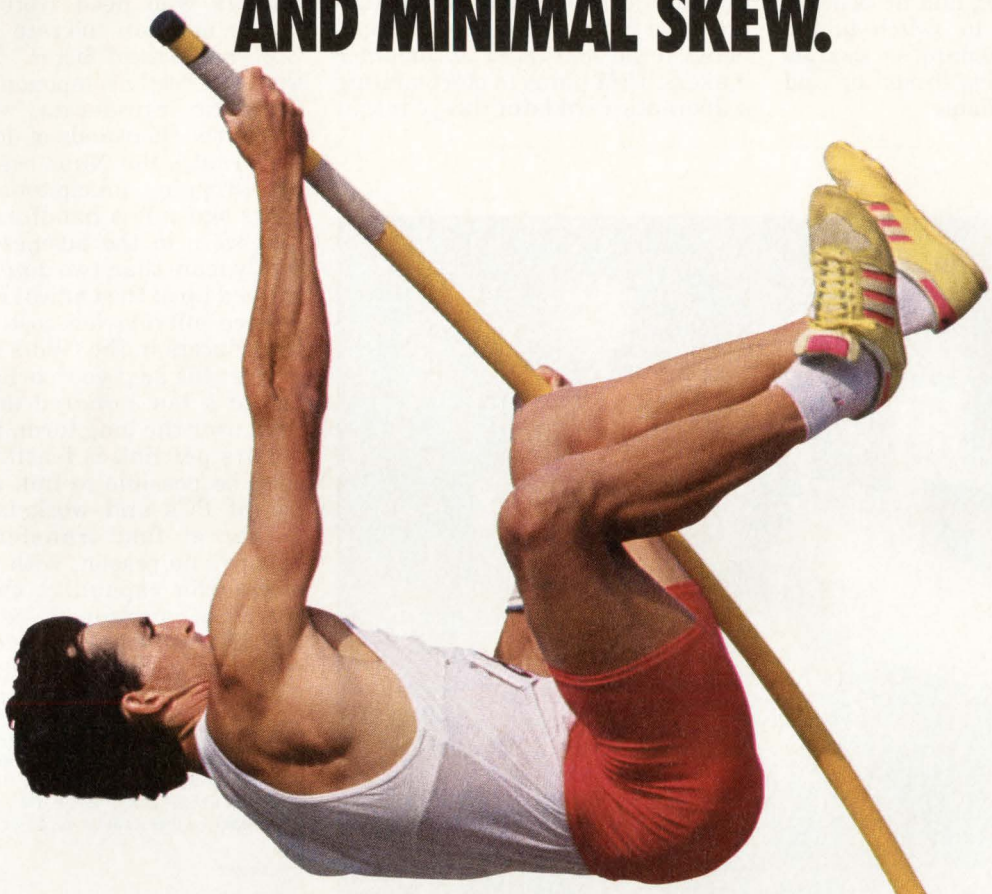

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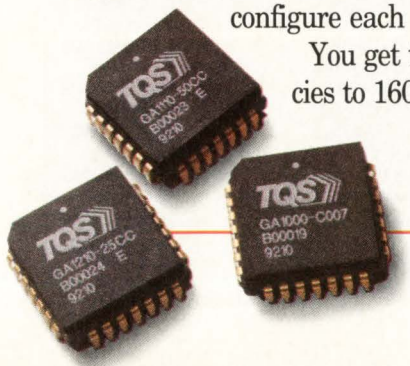

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CIRCLE NO. 42

have adopted HiPPI while they're waiting for the Fiber Channel specification to be completed," says Nunn. He says he's talked to many of these customers and potential customers, however, and he believes they fully intend to switch to the Fiber Channel standard as soon as the specification gets firmed up and parts become available.

Another team of companies has also jumped on the bandwagon to offer Fiber Channel technology. Hewlett-Packard (Palo Alto, CA) and IBM (Armonk, NY) announced a joint effort to develop and manufacture a family of fiberoptic components to be marketed to computer makers. IBM plans to start offering a fiberoptic card later this year that complies with the FC-0 level of the ANSI standard.

According to Nunn, "Fiber Channel, like HiPPI, will get its first impetus from the supercomputer makers who need Gbit/s performance and can tolerate the price. Cost is a critical factor." Currently, the most costly components are the fiberoptic transducers, which now run in the thousands-of-dollars-per-node range. But Nunn sees that figure dropping precipitously. A few years ago only a handful of companies were in the business, but recently more than two dozen vendors showed up at the Optical Fiber Conference offering low-cost fiberoptic transducers in the Gbit/s range.

Over the next year, prices should fall to a few hundred dollars per link; over the long term, under ten dollars per link is feasible. It will then be possible to link any number of PCs and workstations together at fast transfer speeds. "There's no reason, with that kind of transfer capability, that a network of personal computers couldn't work as a single parallel machine with supercomputer performance," predicts Nunn. ■

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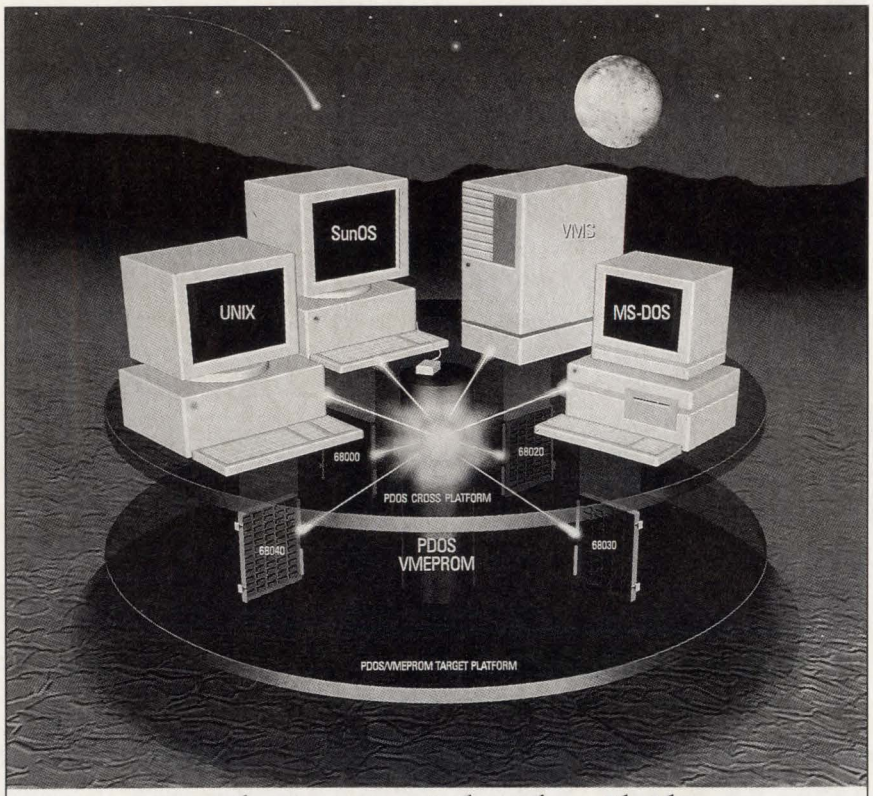

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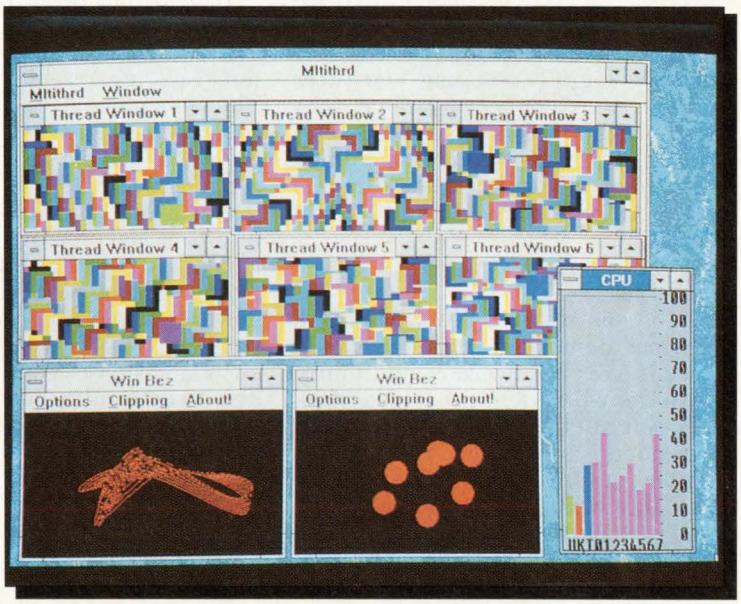
CIRCLE NO. 44

Graphics ICs target Windows acceleration

With GUIs such as Windows setting new standards, chip vendors are rethinking the most cost-effective way to speed up graphics. So instead of a few solutions, designers now have many.

Dave Wilson
Senior Editor



Windows NT runs several threads simultaneously on different CPUs. As shown here, one application has six threads running. Two sample applications are drawing Bezier curves.

It's always been easy to figure out what's going on in personal computer graphics. IBM (White Plains, NY) set the standard and the rest of the world just followed. The hard part has been keeping up with the pace of change. In the past 10 years, there's been a plethora of graphics standards thrust on the unsuspecting PC designer. And although the changes may have benefited the user with higher performance and resolution, the real winners may have been those engineers gainfully employed writing software drivers to ensure that applications packages could keep up with newer computer graphics hardware.

In the PC world, a variety of alternatives exist for the designer wishing to build a PC graphics subsystem. And now, with the Windows graphical user interface (GUI) and its standard application programming interface (API) replacing the traditional hardware register-compatible models of EGA and VGA, the old way of maintaining PC compatibility by building register-compatible hardware may not cut the mustard for much longer. This trend will accelerate with the arrival of Windows NT and other advanced OSs. Graphics and even processor hardware compatibility will then become even less of an issue than it is today.

Back to the future

After the introduction of the Hercules monochrome card in 1982, IBM announced its first color standard, the CGA, in 1983. It provided four colors in graphics mode with an on-screen resolution of 320 × 200 pixels. In 1985, IBM introduced the EGA. Its 640 × 350 matrix allowed 16 colors in graphics mode. In 1987, IBM developed what's now the current standard—VGA—and built it into the motherboard of the PS/2. It provides 640 × 480 resolution with 16 colors on-screen.

Since then, a new standard has emerged, although this time IBM wasn't responsible for developing it. That standard, Super VGA, was developed, endorsed and adopted by a group of graphics companies and monitor vendors known as VESA (Video Electronic Standards Association). Super

VGA represents a significant enhancement of the VGA standard, but there's no one resolution associated with it. In fact, there are many. The standard has gone from 800 × 600 to 1024 × 768, and now chips are available that will support 1280 × 1024 resolution.

For its part, IBM launched yet another standard in 1990—extended graphics adapter (XGA). To push the XGA as a standard, IBM licensed the XGA technology to SGS-Thomson (Phoenix, AZ), which currently offers two chips—a serializer palette digital-to-analog converter and an XGA display controller. XGA supports 256 colors at screen resolutions up to 1024 × 768, and adds a new color mode that allows 65,536 colors to be displayed at 640 × 480 resolution.

Inside XGA

As the son of VGA, XGA has three distinct modes of operation. Not only does it offer backward compatibility with the VGA standard, it also offers 132-column text mode as well as an extended graphics mode. In the extended graphics mode, XGA devices can accelerate and improve screen updates by the use of an autonomous graphics processor that's used to handle custom line drawing, area fill, pixel block transfer, scissoring, and map masking. The coprocessor works on pixels within pixel maps, and the XGA standard allows pixel maps of any arbitrary size up to 4096 × 4096.

XGA also supports some useful features of modern GUIs. Map masking is an important characteristic of XGA that lets you draw only in the exposed area of a window, rather than the whole window. Fast text drawing, crucial to windowing environments, is supported through an on-chip block-transfer function.

In addition to graphics features, XGA has also addressed some concerns of the system designer. It offers bus mastership, for example. That lets video data move from system memory to video display memory without the main system processor intervening.

But are all of these functions really necessary? While XGA has the capability to perform local bus mastering, it's not exercised in the Windows environment. Worse yet, at the present time bus master devices such as graphics controllers are unable to determine how the processor virtualizes physical addresses. And because today's systems are not truly multithreaded, even if a graphics controller can perform bus mastering operations, under present operating systems, it's difficult to do independently of the CPU.

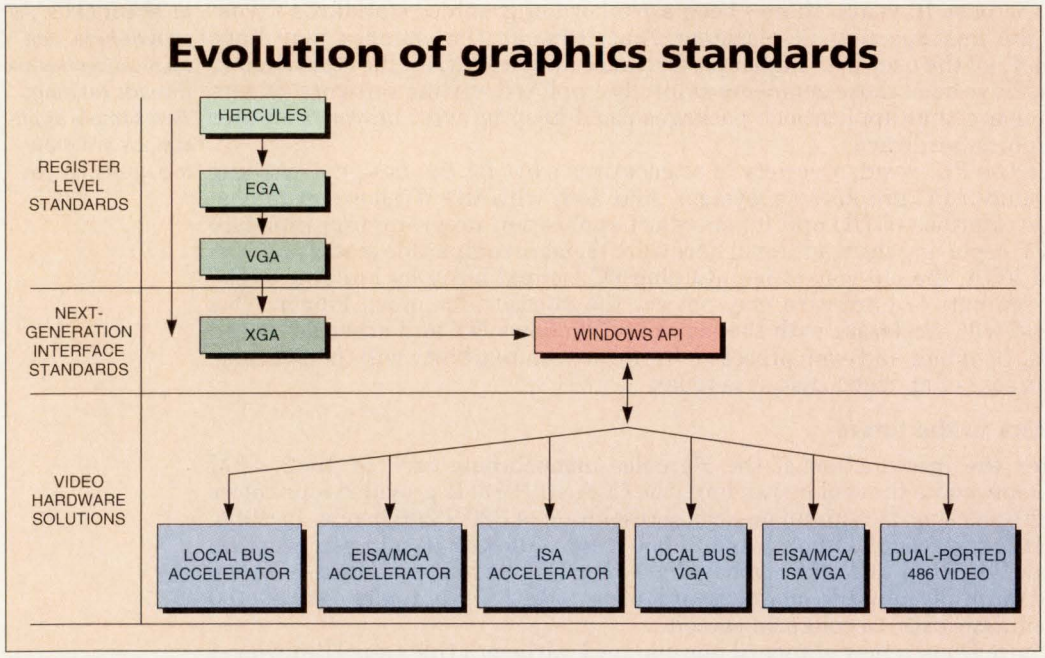
The other "gotcha" is that the CPU, under the direction of the operating system, may be able to transfer data just as fast as a mastering graphics controller could. "In short, [bus mastering] doesn't buy designers that much today," says Larry Vandendriessche, director of graphics products at NCR (Colorado Springs, CO). "In the graphics world, there's almost nothing it can do, especially in Windows. In OS/2 it has a minor capability. It's a fairly expensive piece of hardware. It's not like a disk drive application, where there's a need to perform some serious transfers back and forth from memory to disk."

Who needs XGA hardware?

Most people believe XGA will take over from the VGA market at a modest pace, limited by developments in Windows NT and OS/2 Version 2.0. If these OS alternatives aren't quickly forthcoming, however, XGA might gain ground at a faster pace. In that case, XGA may have a limited market share as graphics designs continue to become more fractured and as the importance of the OS and GUI come into play.

Vandendriessche thinks that XGA as a register-level standard isn't all that necessary. "Ninety percent of the applications programs are Windows-based, not XGA-based. With the popularity of Windows, the Windows API is the one that everyone writes to," he says. "By using emulation techniques, hardware that doesn't look exactly like XGA can take the commands that are written by an XGA software driver and display them. We can get a better price/performance by using a slightly different architecture. It's very possible to write an XGA emulator [a program that will look like XGA to applications] and with it make the non-XGA-compatible register hardware much faster than XGA. That's even with an emulation step in between. It will still be compatible with XGA, but it's typically at the driver level and not at the register level."

But there are still those who value



The evolution of graphics standards from hardware to software has opened up a variety of hardware processor solutions. These range from add-on local bus accelerators to full-fledged add-in AT and EISA processors. The solution that's optimal depends on the architecture of the machine.

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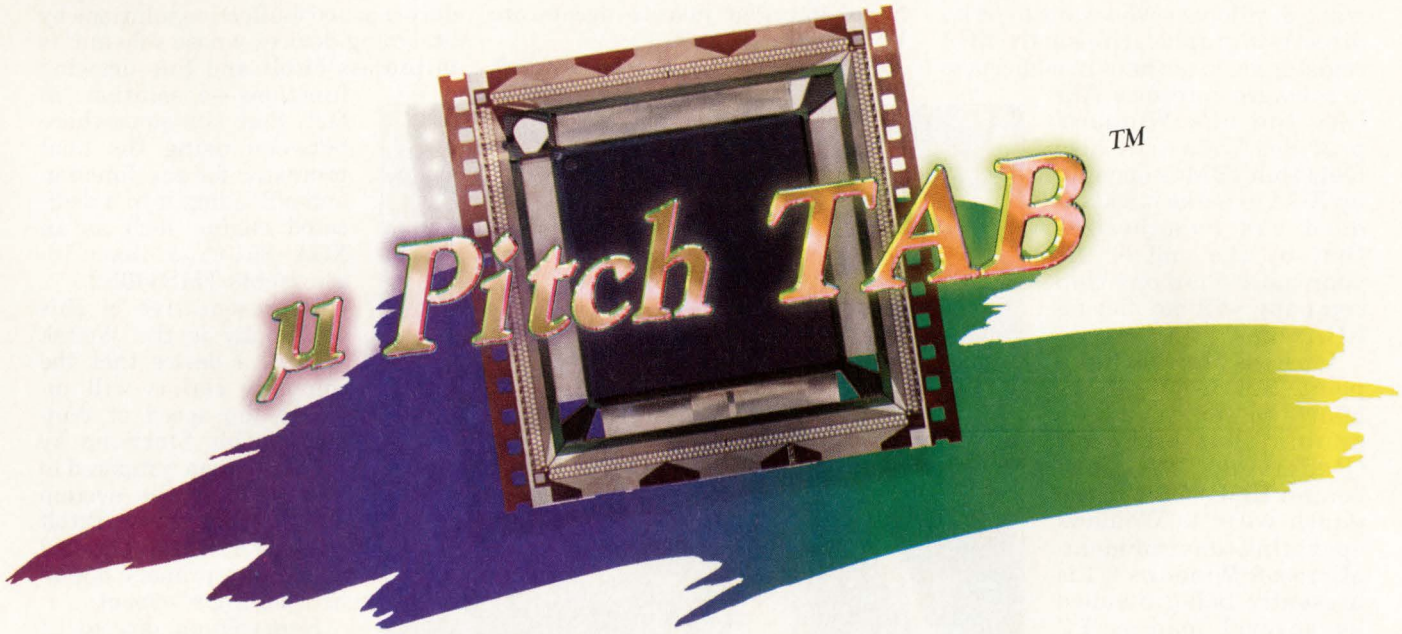

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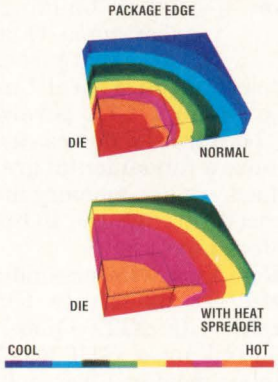

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XGA. "XGA not only offers Windows performance but is a standard graphics reference for people who don't want to work in the Windows environment," argues Nunzio Martelli, technical marketing manager of SGS-Thomson (San Jose, CA). "And that's important for some software developers who want to write directly to graphics chips at the XGA register level, perhaps in addition to a software interface API like the one Windows provides." Martelli also feels that IBM is opening up XGA to make it a standard and hypothesizes that by the end of the year more than one chip company will be offering XGA chips.

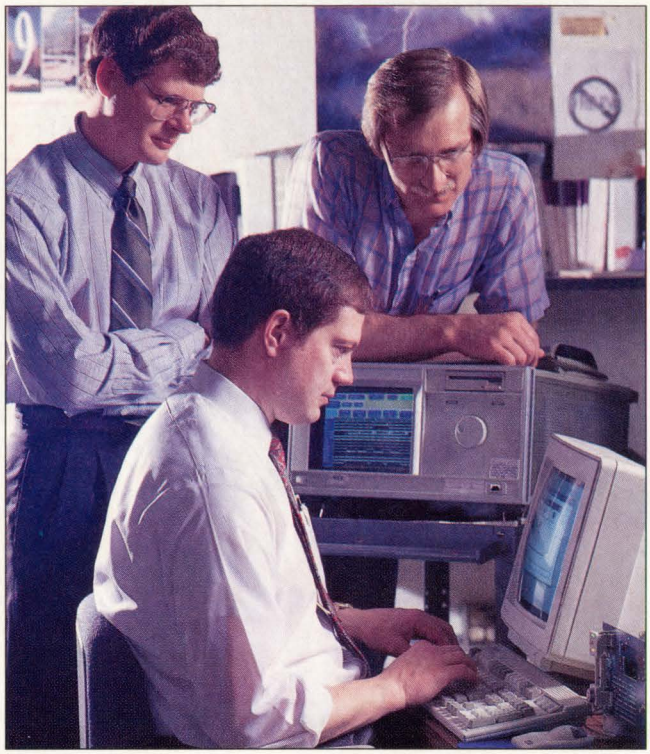
Perhaps Martelli has a point. But despite IBM's efforts to stop it, no one doubts that Microsoft (Redmond, WA) has beaten IBM's OS/2 to the punch with its Windows operating environment. Microsoft Windows 3.1 is presently being bundled by several leading PC vendors while OS/2, it seems, has been left on the shelf, despite user claims of superior robustness and performance.

Windows opens options

Microsoft Windows is divided into three parts: the graphical device interface (GDI) that supervises all interaction between the application and output devices, such as a monitor or a printer; the user interface that supervises interaction between the user and input devices; and the kernel that manages memory. Windows drivers, loaded at start-up, communicate directly to the GDI, informing it of specific functions that specialized hardware might offload from the CPU. This lets existing systems and software take advantage of new hardware without further modifications.

Although the graphics marketplace might already seem gloriously fragmented, Windows will make it more so, at least according to Michael Maia, vice-president of sales and marketing at Trident Microsystems (Mountain View, CA). Maia expects to see several key areas emerge in the next few years: graphics coprocessors, local bus interface graphics chips, high- and low-resolution VGA graphics chips, and, perhaps most important, GUI accelerators. Because of the sluggishness of Windows applications, many new graphics accelerator architectures have emerged just to accelerate Windows.

Martin Booth, senior product marketing engineer at Fujitsu Microelectronics (San Jose, CA), notes that the ubiquity of Microsoft Windows has freed PC designers from becoming register-level-compatible with IBM. On the down side, 50 to 80 percent of a CPU's execution cycles are consumed just by running the subroutines of Windows. This, of course, results in a reduction in application performance when compared to DOS applications. Booth says that bitblt and line drawing are the two primary functions used by Windows to represent text and graphics information on screen. Accelerating those functions accelerates Windows applications, then.



Larry Vandendriessche (seated), director of graphics products at NCR, thinks that register-level compatibility with XGA is unnecessary. Emulation techniques will give better performance at a lower price, he argues.

A master at going faster

While IBM has established some sort of direction with XGA, many vendors, such as Weitek (Sunnyvale, CA), agree with NCR that many features of the XGA architecture, such as memory management and bus mastering capabilities, are unnecessary for mainstream office-automation applications. These vendors argue that it's possible to produce more cost-effective solutions by designing devices whose sole aim is to process bitblt and line drawing functions—a solution, in fact, that sits somewhere between using the host processor for the function and offloading it to a dedicated engine such as an XGA, 8514A or Texas Instruments TMS340X0.

Representative of this philosophy is the Weitek W5086, a device that the company claims will increase the speed of Windows bitblt functions by over 26× when compared to simply using the system CPU for the purpose. Bitblt and line draw are targeted as the two primary operations for improvement.

Henry Quan, director of marketing at graphics chip and board vendor ATI (Scarborough, Ontario), feels that, when comparing accelerators, the comparison shouldn't just be based on the speed of acceleration functions such as bitblt at the expense of ignoring architectural issues in building graphics subsystems. Quan goes on to say that just putting an accelerator on a local bus will not help improve GUI performance at all, because the device itself doesn't remove a fundamental graphics bottleneck—video memory must be addressed through the I/O port of the system processor.

Ron Yara, vice-president of marketing at S3 (Santa Clara, CA), agrees with ATI's Quan. He says that linking a GUI accelerator to display memory over a high-speed local bus interface eliminates the graphics performance bottleneck present in systems that require that the CPU pass through an I/O bus and then the display controller before reaching display memory and executing a graphic function. In the ATI graphics architecture, graphics data avoids going through the I/O port of the 486 when it needs to be

Printer graphics mirror those of CRTs

The move from text-based user interfaces to high-resolution graphical user interfaces is creating graphics demands that host CPUs can't efficiently handle. At the same time, the move to high-resolution color and gray-scale laser printers working at 600 dots per inch (DPI) or better is outstripping the graphics capabilities of today's laser printer controllers. In both cases, the industry is moving to graphics coprocessors that can offload the host CPU and printer controller of compute-intensive functions such as graphic rendering.

The processes of producing images for CRT display and laser printer output are quite similar. In the case of CRT output, the host CPU generates a high-level description of the image (in Graphical Device Interface for Windows and QuickDraw for Apple machines), executes the display list and writes the pixels to video memory. In the case of laser printer output, the host CPU sends the page description (in PostScript or PCL5) to the laser printer controller, which interprets the page description, executes the display list and writes the resulting image to laser printer memory.

Controllers carry the burden

Because laser printer controllers must produce much higher-resolution images—300 DPI for an HP Laserjet III versus 96 DPI for a 1024 × 768 Super VGA display—they often bear a much higher computational and graphics burden than CRT controllers. The move to 600-DPI resolution in laser printers will increase this burden by a factor of four to five, with the addition of gray-scale and color capabilities upping the ante even more.

At 300 DPI, graphics operations such as executing the display list and rendering images consume only about 20 percent of the controller's cycles. As a result, the controllers in 300-DPI printers are able to get by with RISC processors such as Intel's i960, or CISC processors such as the 68020 working in conjunction with a dedicated bitblt (bit boundary block transfer) processor.

At 600 DPI, however, the graphics load increases substantially, occupying 35 to 80 percent of the controller's time. To keep up with graphics operations that have real-time requirements, such as building characters to put in the font cache, the controller must steal cycles that would normally be used for page interpretation. As a result, printing speed suffers.

Offloading responsibilities

One way to offload the printer controller of its graphics responsibilities is to use a dedicated graphics acceleration coprocessor such as Peerless' banding coprocessor. As in CRT graphics, relatively few operations, such as bitblt and fill, account for the bulk of the graphics load. By accelerating these operations, a graphics coprocessor can provide a dramatic increase in graphics throughput.

Bitblt, for example, can be greatly accelerated by working on several aspects of the bitblt operation, such as calculating and applying masks, moving bit fields and aligning source and destination addresses in parallel. Anticipating common sequences of operations can also yield a significant speedup. For example, when setting up halftone patterns, the coprocessor should also set up to perform three-operand bitblts, which will be needed to apply the halftone patterns to characters.

In addition to improving drawing speed, a graphics coprocessor can greatly reduce laser printer memory requirements and cost by using image banding techniques. Depending on the resolution, banding can provide a saving of two to eight times the memory used by full-page buffered designs, which must provide a separate memory location for each pixel on the page.

Limited technology

But lack of efficient storage representations, innovative algorithms and controller horsepower has limited the use of banding technology. To band an image in real time, the controller must be able to execute the display list and output the image fast enough to keep up with the drum. At 8 pages per minute, the controller must be able to convert a PostScript page description to a 1-Mbyte image every 7.5 s. A 25-MHz i960, by contrast, requires 15 to 18 s to perform this conversion for a Ventura Scoop image.

Many 300-DPI PCL5 laser printers, such as the HP Laserjet III, exploit banding but are limited to simple graphics. When you try to output complex images, the printer controller loses its ability to band the image in real time. To print such images, you must buy additional memory, which defeats the purpose of using banding.

To make banding feasible, Peerless has developed a compression technique that lets interpreted page descriptions be more efficiently represented and executed. For even higher resolution (greater than 600 DPI), Peerless has added a hardware banding capability that lets its coprocessor band images in 500 to 600 ms, independent of resolution. At 1200 × 600 DPI, for example, a printer based on Peerless' coprocessor and using the PostScript language requires only 2 Mbytes of memory, compared to 16 Mbytes for designs that use full-page buffering.

Because the graphics requirements of laser printers and CRTs are so similar, manufacturers are looking for opportunities to use coprocessors for both display and printing applications. Such a coprocessor could even serve double duty, providing graphics acceleration for both display and printing.

Steve Butterfield, vice-president of hardware development, Peerless, Redondo Beach, CA

written to the video memory from the system RAM. Instead, high-speed data can stream into video memory under control of the 486 and the bus interface controller on the ATI graphics chip.

Quan adds that the problem with some accelerators is that they can't access video memory alone. A graphics engine must be set up to read the pixel data back through the I/O port of the system processor. That approach, he argues, is very inefficient. "The way to overcome it is to combine the best of both worlds—use VGA for compatibility to boot the system, and after that use the accelerator to boost the performance of the graphics," Quan says. Similarly, S3's S86C911 GUI accelerator performs linear addressing, letting

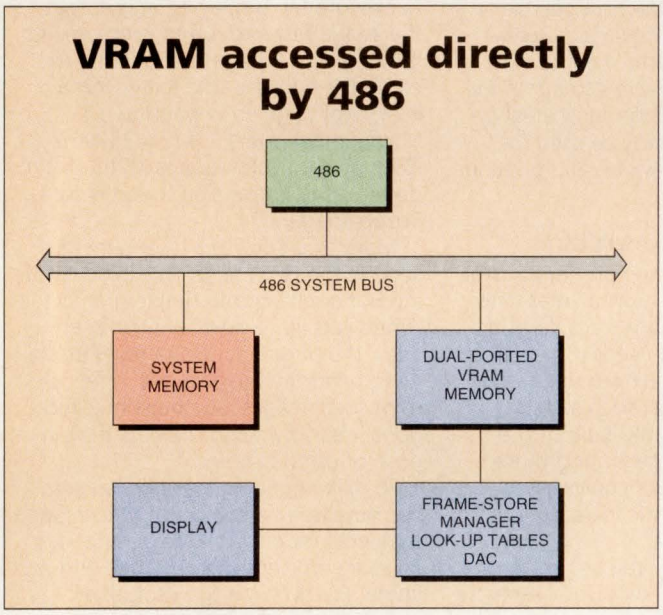
the part gain direct access to memory.

Say no to coprocessors?

For its part, the Texas Instruments Graphics Architecture (TIGA) has represented one of the more cost-effective means to obtain high-performance, high-resolution graphics on the PC/AT bus. Certainly, it looks as though TIGA hasn't been forgotten by Microsoft. The recently released Windows Version 3.1 includes a TIGA driver, giving users the ability to accelerate Windows applications at higher resolutions. In fact, of the selected group of drivers included in the latest version of Windows 3.1, Texas Instruments (Dallas, TX) claims that the TIGA driver is the only one capable of resolutions of 1280 × 1024 and beyond.

The TIGA driver is optimized to let new features in Windows 3.1 take advantage of TI's 340X0 family of processors that are at the heart of the TIGA architecture. For example, the driver lets the TrueType scalable font technology in Windows 3.1 tap the font-caching capabilities of the TIGA-340 processors. "With the capability to take Windows 3.1 into the future with support for true-color images and support for resolutions beyond 4096 × 4096, it's easy to see why we supported TIGA as the highest-resolution driver in the 3.1 package," says Rich Tong, Windows product manager at Microsoft. Nevertheless, solutions still aren't all that inexpensive. Some TMS34010 boards are now under $500 and TMS34020 boards are falling below the $1,000 mark.

Despite these facts, not everyone paints the same kind of graphical success story for its coprocessors that TI does. Some, such as NCR's Vandendriessche, see a trend away from graphics coprocessors altogether. As an example, he cites Dell Computer's (Austin, TX) 486 PC demonstrated at Comdex, which had no graphics processor chip.



The power of the 486 may be unleashed to handle graphic functions and be every bit as fast as a dedicated graphics accelerator—if the memory architecture is built correctly. Dell Computer has demonstrated a fast PC graphics system working with dual-ported video memory and Inmos color video controllers.

In the Dell design, a central 486 processor performs graphics drawing operations as well as general-purpose applications. On the motherboard, high-bandwidth, dual-ported video memory appears to the host processor just like system memory. In other words, the host processor has direct access to video memory as well as its own program memory. The other port of the video RAM, the serial shift port, is hooked to an Inmos triple 8-bit D-A converters as well as a look-up table that's used to convert and display the VRAM data.

"The result is that the 486 is several times faster at graphics than some 'accelerator' chips, and noticeably faster than a Sun workstation," says Vandendriessche. Naturally, the Dell machine is not "truly" register-set-compatible with VGA, but the fundamental principle that a 486 can be used in such a fashion, Vandendriessche feels, is a strong argument against coprocessors.

Yet another factor limiting the appeal of graphics coprocessors is their price. For the cost of a high-end graphics card ($1,000 or so), PC users can move up a generation in CPU. You can purchase the next generation of 486 for $1,000 more. That creates a lot of backward price pressure on intelligent graphics cards. On the other hand, PC designs that support tightly coupled processor/video sections such as Dell's let you capitalize on the power of the processor not only for video processing but also for all other non-video-related processing too.

That's why most VGA suppliers, such as NCR and AT&T (Allentown, PA), are moving to architectures where the graphics chip will reside on a 486 or 586 local bus, letting the video chip perform only those functions that the processor doesn't do well. Color expansion, as well as line and curve drawing, for example, require more registers than are locally available in a standard X86 architecture. These are likely to remain areas where acceleration can be performed at a tolerable price to the end user.

Going direct to the CPU

In addition to hardware-based bitblt support and hardware cursors, many of the newer VGA designs sport a direct interface to the onboard processor as well. As for any standards associated with that interface, that's a horse of a different color. "Currently, there is no standard for the local bus," says Steve Gary, director of marketing for video imaging and graphics at Oak Technology, a VGA chip company based in Sunnyvale, CA. When Gary describes his chip as compatible with a local bus, the bus is defined as the one that's used to communicate between the cache controller, CPU and memory.

There is, however, a VESA standards committee working on defining a local bus. It's currently at the draft level. For its part, Intel (Santa Clara, CA) has proposed another standard—the PCI (peripheral component interconnect). Recently, Intel has offered its proposal to the local bus standards committee for consideration.

NCR's Vandendriessche agrees that there are many definitions of a local bus at the moment. "We see most people putting the VGA chip directly on the processor bus or a local bus such as Opti, which is like using the processor bus plus or minus one signal," he says. He feels

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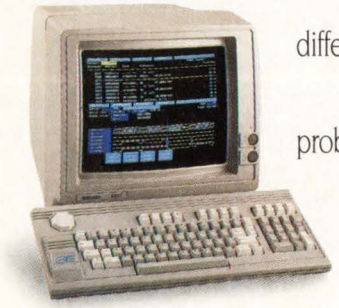

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that actual processor bus architectures, such as Intel's PCI, are a little farther down the road, and really only make sense when you have more than just the VGA chip sitting on the local bus. He describes the two camps as processor-direct—where the bus actually talks to the processor—and those that rely on newer interfaces such as Intel's PCI.

For their part, motherboard manufacturers are moving toward a modular architecture where a single board design can be used in a variety of market segments. Some current PC chip sets let you build motherboards that sport EISA-like connectors bringing out the signals of the microprocessor to the end user. In that way, if you wish to upgrade a system to a 486 processor, it's only necessary to purchase an add-in processor card to slip into that slot. With such a backplane approach, you could upgrade processors or add an upgraded local bus graphics card simply by adding a new card.

Placing a frame buffer controller onto a local bus is extremely efficient—an order of magnitude increase in performance can be achieved without going to the added expense of going to a programmable solution. "Part of the reason that the local bus will be used in conjunction with the frame buffer approach is that the processor itself is becoming more powerful," says Oak's Gary. "With a 286, you didn't want to burden it with the heavy computation required for graphics operations. With the 486- or an R3000-based machine, the processors may be more capable of performing the graphics operations than the limited graphics hardware that can be built into a dedicated graphics controller."

Add processors for more speed

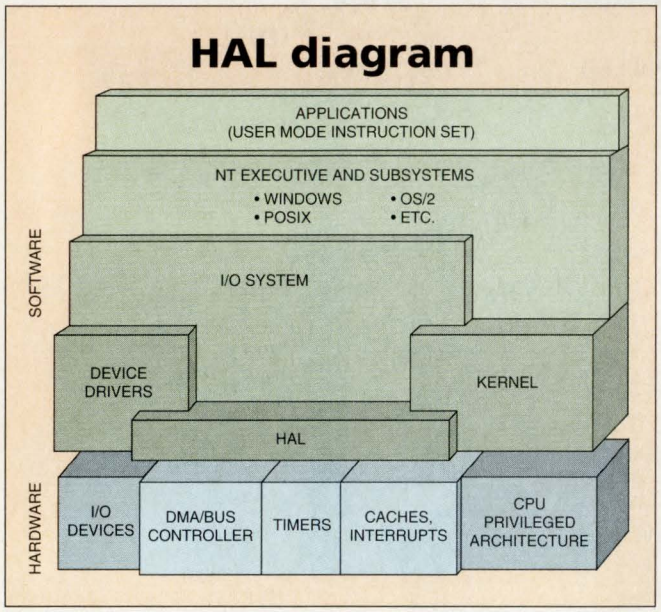
That's not to say that there's no demand for coprocessors at all. Even Vandendriessche admits that a coprocessor solution based on an AT add-in card can still make a lot of sense. And, at present, the largest opportunity for graphics coprocessor chip vendors is still on expansion boards like AT adapter cards. In those cases, applications can benefit from the autonomous operation of the video chip—performance can be improved by using a graphics coprocessor connected to the host across a slow bus such as ISA.

There's also no reason why today's current generation of VGA devices can't address the requirements of the AT add-in market as well as those of the market for local buses. Vandendriessche argues, however, that when designers have the option of building graphics devices directly onto a local bus and running at the speed of a 486, then a coprocessor on an AT bus can't match the performance.

Undoubtedly, Windows NT and OS/2 Version 2.0 will change the face of PC and PC graphics design forever. As multitasking, multithreaded operating systems, they'll let hardware designers build modular PCs that will permit end users to extend the processing power of their machines by simply adding another general-purpose X86 processor directly onto the motherboard.

That approach may sound the death knell for the graphics processor. If the user wants to upgrade the video, this can be done by plugging another X86 processor into an open slot on the motherboard. "For the price of a graphics processor, users will purchase another 486 to accelerate all their applications—not just the graphics element. It's a move away from specialized processing to general-capability processing which is shared by a range of tasks," says NCR's Vandendriessche.

As for graphics, it may be the greenback alone that determines the success of one graphics solution over another. "The PC world is a cutthroat business," says Surinder Rai, AT&T's manager of product definition and applications. "After all, most of the graphics solutions are attempting to do the same thing—speed up Windows." ■



The world according to Gates—Windows NT removes the intricacies of the hardware from the developer of the software application, letting you make changes in hardware without hurting application compatibility. This is achieved through the hardware abstraction layer (HAL) that isolates the OS from the specifics of the hardware.

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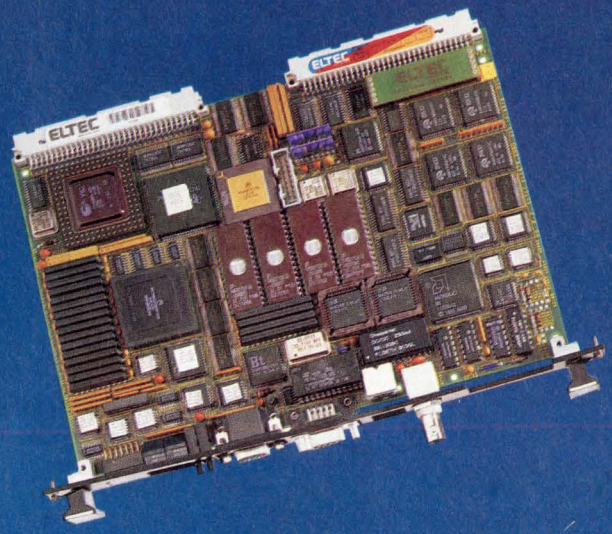

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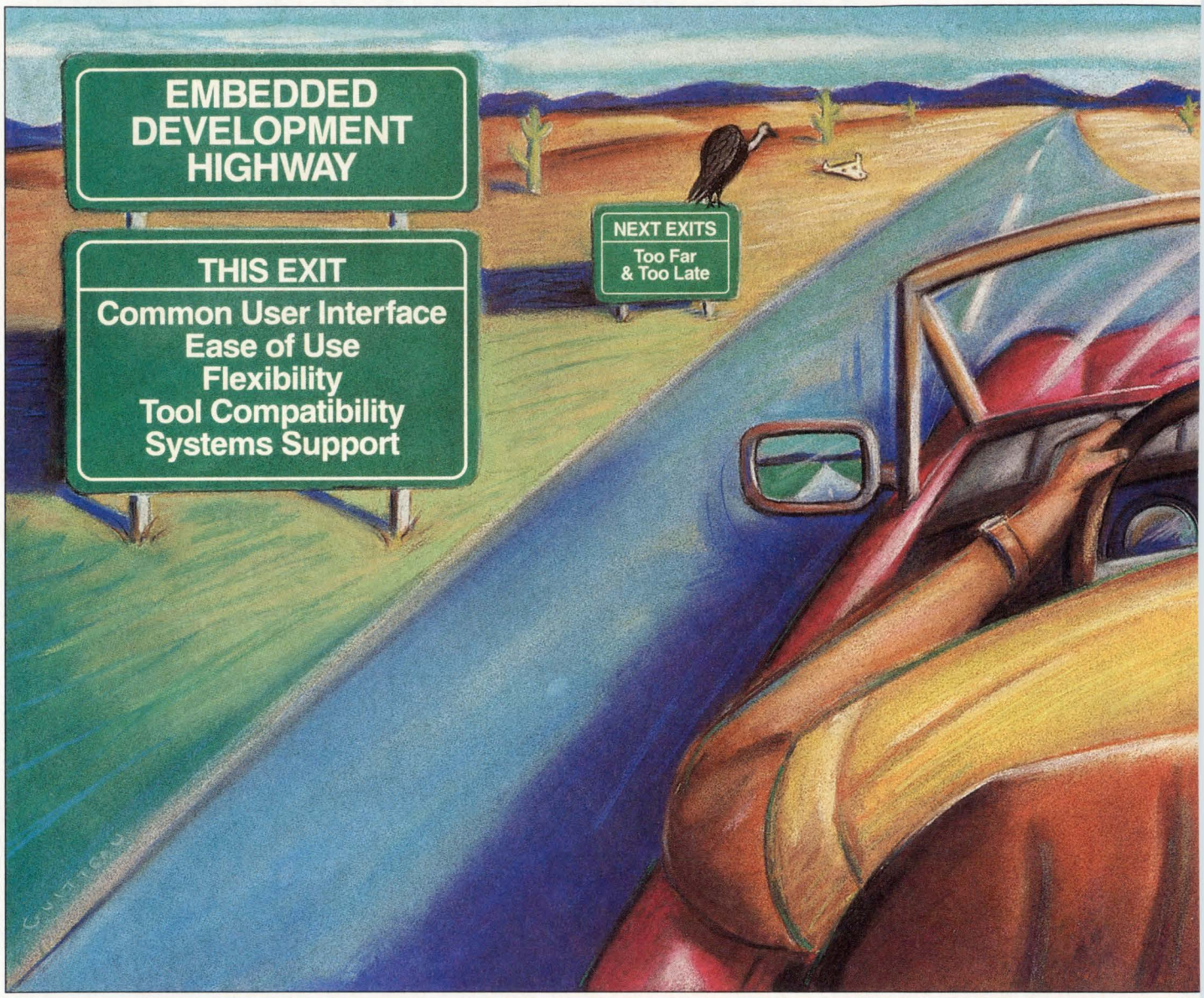

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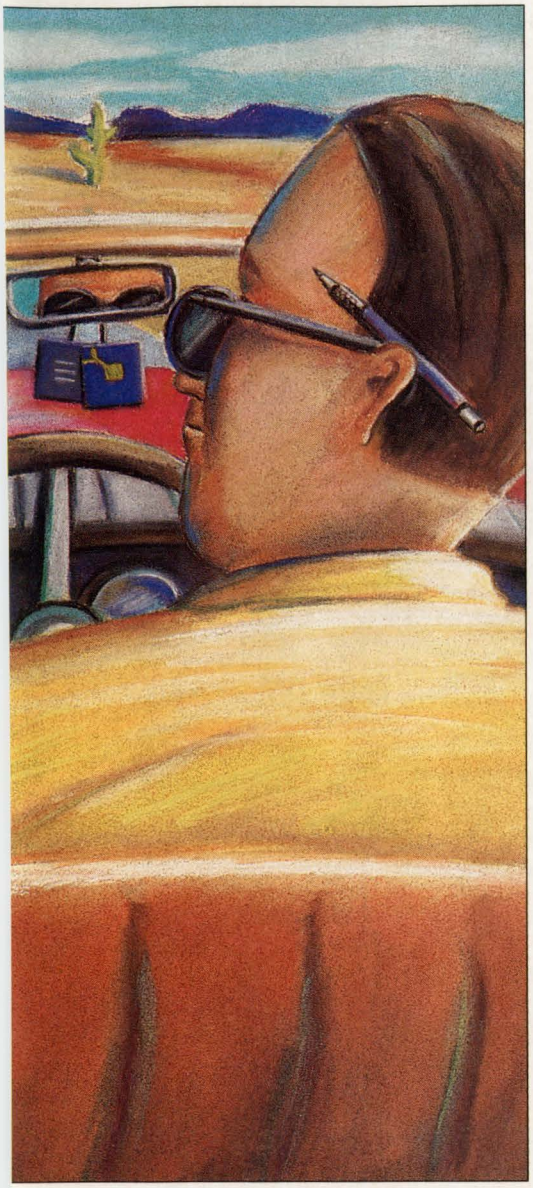

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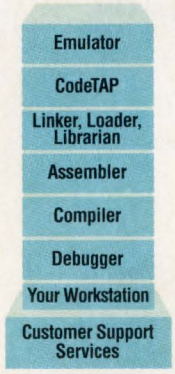

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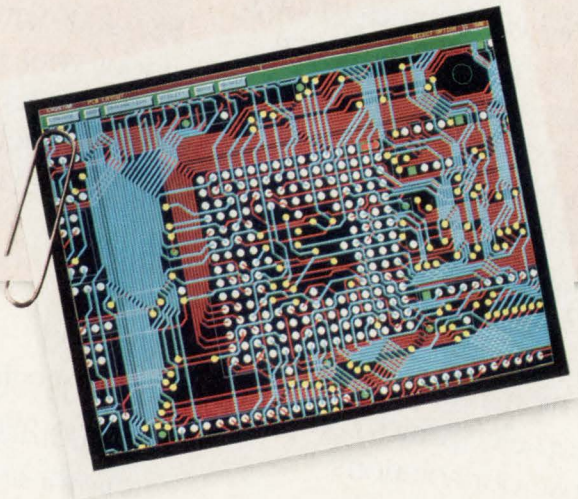

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The personal computer has gained wide acceptance as a platform for computer-aided engineering and design (CAE/CAD). Not an 8-bit slowpoke anymore, today's PCs are as fast and effective as workstations were a few years ago. It's true that workstation technology has also improved, so they're still an order of magnitude faster and more powerful than most PCs—at least as far as raw Mips are concerned. Nevertheless, the PC has proved to be powerful enough to handle almost any task associated with electronic product and system definition and design.

The PC—and more specifically, the IBM PC, PC/XT, PC/AT, PS/2, and compatibles—has become by far the most common platform for CAE/CAD design, in part because for many years such a machine was almost always found in offices and labs to help document, budget, track, and perform other nonengineering related functions. Today, 286-, 386- and 486-based machines rank first, second and fourth respectively as the most widely used engineering platforms.

The sheer size of the overall PC market has made this dominance possible by spurring all types of peripheral offerings. This keeps competition at its sharpest and provides users with the benefits of low-cost, high-quality equipment. Of most interest to engineers, however, aren't issues of cost or operating speed; rather, they're concerned with the PC as a serious platform for design automation, test, debug, documentation, and management. "A lot of the engineers we deal with use our tools rather than wait for time on one of the large workstations," says Carl Droste, engineering manager at Omation

Jon Gabay,
Contributing Editor

(Richardson, TX). "Why should an engineer wait to get his design in the queue when he can lay it out, simulate it and route it on a PC? With a 50-MHz 486 PC, our tools can get a board design completed in time that rivals workstation-based tools."

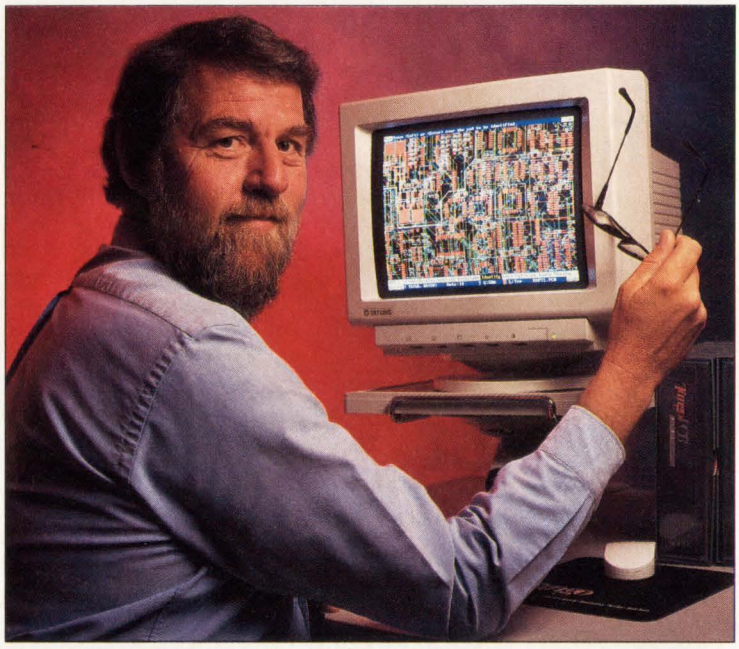
Start with schematic capture

At the front end of the design process is schematic capture. This constitutes perhaps the largest use of the PC in engineering. An effective schematic capture tool creates an automated way of solidifying concepts in graphical form. Primitive elements from vendor-supplied or user-generated libraries are placed in a graphical workspace and moved around and interconnected as needed. Labels define key signals; text documents comments; and connectors, headers, standoffs, and module ports connect to all signals—I/O, power, test points, and intersheet schematic pages. Output is generated as documentation, and can be produced in formats which can be passed along to other design tools aimed at specific disciplines.

Choosing the right schematic capture program for your specific needs is like buying a new car. Price is a factor, as are speed and performance, as well as the options that tailor a vehicle to individual preferences. Especially important is compatibility.

With a car, you don't buy a Miata if you need to haul furniture. With schematic capture software, don't get a package suitable for ASICs if you're designing printed circuit boards. "I've always contended that the most important consideration isn't the platform but the application," says John Durbetaki, CEO at OrCAD (Hillsboro, OR). "If you can do your job on a PC, there's no reason to look elsewhere. The important thing is to know what you want to do and then choose the tool and the platform for the job."

A distinguishing characteristic of schematic capture programs is whether they're bundled into applications or come in flexible general-purpose packages. Bundled packages, such as Master Designer from P-CAD, EE Designer III from Visionics and Highwire from Wintek, offer systems with consistent user interfaces and operating environments. Included in these packages are digital and analog simulators, layout aids such as rat's nesting and force vectors, autorouters, design and electrical rule checkers, and library maintenance tools for schematic, simulation and layout models. They provide automated placement of components, as well as photoplot generation tools for Gerber output.



"We know that the majority of PCBs today continue to be designed on PCs and not workstations," says Jerry Burwell, vice-president of engineering at Accel Technologies. "With affordably priced design software and powerful 386- and 486-based machines in plentiful supply, the price/performance curve is still skewed in favor of the PC and complementary tools as a system alternative to the workstation for PCB design."

In the beginning

P-CAD (San Jose, CA) was among the first companies to offer an integrated schematic capture, simulation and PCB layout package. It now offers an entire suite of discrete and integrated CAE tools. Its entry-level Master Schematic Capture program features over 6,000 parts in a comprehensive library, up to 99 levels of hierarchy, design rule checking, and forward and backward annotation.

FutureNet (Redmond, WA), a Data I/O company, another pioneer of PC-based CAE, developed the Dash schematic capture environment. Later acquired by Data I/O, FutureNet developed a netlist format which is still widely used as a de facto standard for both third-party and its own tools.

OrCAD also offers a widely-used schematic capture program. OrCAD SDT IV, the current version of the company's schematic design tool, has matured to include an operational shell that manages designs by helping you keep track of all filenames and extensions associated with a project. In addition, the shell lets you integrate your own or other company's tools into the design environment. This framework also lets you use OrCAD tools all the way through a design, or you can pass along schematic data to third-party toolsets.

An important feature of OrCAD's low-cost design tool for board- and system-level designs, as well as PLD and ASIC designs, is its large library of design elements, as well as the ease with which designers can define custom parts either graphically or via text files.

Other companies with low-cost schematic capture tools include Accel Technologies with its Tango Schematic Series, Omation with Schema III, Pads Software with its namesake, Pads, Visionics with EE Designer III, and Wintek with Highwire. Recently released by Accel (San Diego, CA), Tango Schematic Series Version 1.3 features a user interface based on the company's Tango PCB software that's both easy to use and to learn. It also boasts a third-party library with more than 20,000 unique elements.

"We hear many reasons why people opt for PC-based EDA tools," says Jerry Burwell, vice-president of engineering at Accel. "One of the most often cited, after price, is ease of use. PC-based software is likely to be much easier to use than its workstation-based counterparts, with capabilities and performance that far outshine what was available just a few years ago."

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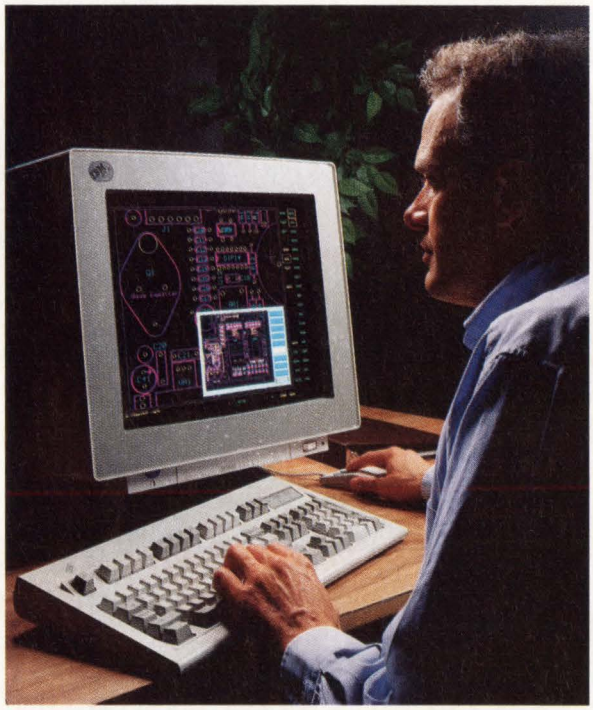
"P-CAD helps us transform abstract engineering concepts into sound designs."

Jeff Rowland, President



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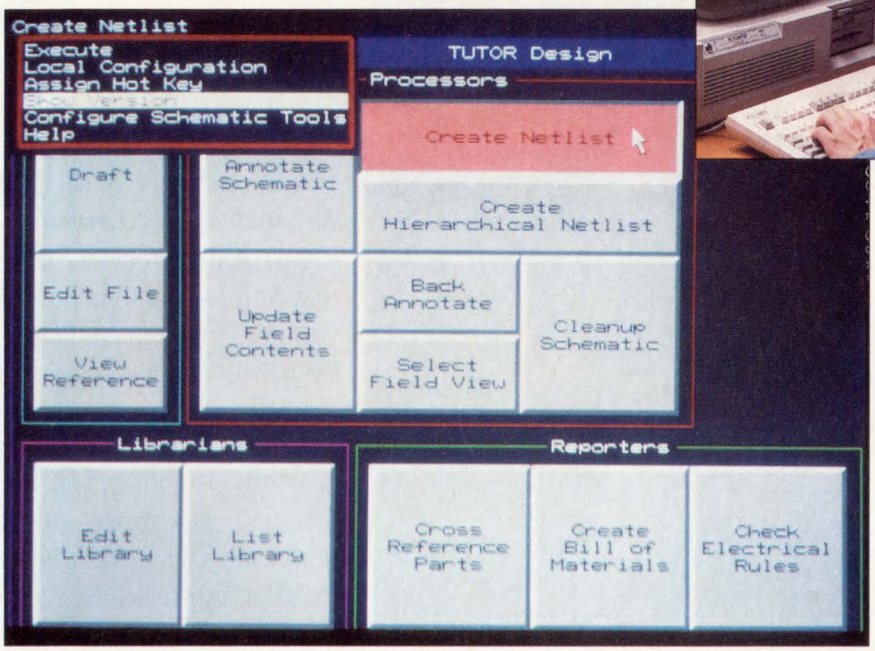
CIRCLE NO. 50

Another very recent entry into the low-cost schematic capture market is Schema III by Omation, which features an easy user interface, a 7,000-part library, design rule checking, unlimited hierarchy, and more. Schema III also lets you export design data to ASCII, AutoCAD DXF, DBase, Lotus, PostScript, and TIFF formats, so you can send design data to other departments and integrate with tools they may be using.

Viewlogic Systems (Marlborough, MA) is another force in PC-based schematic capture and simulation, with a product line that's a bit more costly than most. But its philosophy, shown in advanced features such as multiwindowed operation, tightly coupled and seamless integration between digital and analog simulation with schematic capture, and strong alliances with ASIC, PLD and FPGA vendors, as well as PC-board design automation systems currently in use, has paid off.



The design shell implemented in OrCAD's SDT IV permits you to easily and quickly configure for different projects and mix various third-party tools within a single design environment.

Alike, but different

While all the schematic capture programs mentioned share common features, such as the ability to create and maintain symbol libraries and schematics and to generate netlists for use with other design automation tasks, special features differentiate these packages. For example, P-CAD features a unique trace density histogram as a placement aid. Viewlogic supports VHDL, making its simulator ideal for ASICs, PLDs and FPGAs. Visionics includes a thermal analysis package for heat modeling.

An interesting new product from Dazix/Intergraph (Huntsville, AL) is Ace+ PC Entry software. Dazix/Intergraph, primarily in the workstation market with ASIC, PCB and multichip module designs, has recognized the usefulness of the PC as a design entry system and has targeted Ace+ PC Entry as a low-cost way to get started with the company's comprehensive design environment. File-compatible with the larger and more costly Dazix/Intergraph workstations, Ace+ PC Entry transparently integrates the PC into the Dazix/Intergraph CAD/CAE/CAM environment and can run on 286, 386 and 486 systems under Microsoft Windows 3.0.

Although the PC is just an entry station, symbols and schematics created on it can be used as source files for workstations, which can then simulate and lay out designs, providing the engineering department with more design seats for the buck. The design of PLDs is a task that was first undertaken on PCs, and is still, for the most part, handled on that platform. In the early days of proprietary software, there was Palasm from Monolithic Memories, Inc (MMI) and Amaze from Signetics, as well as products from third-party PLD software pioneers: Abel from Data I/O and CUPL from Assisted Technologies (now part of Logical Devices).

Many companies, both third-party suppliers and manufacturers, provide PLD support tools for the PC. Third-party tools are the most flexible, since they generally support parts from various manufacturers. "In general, there's more software available for engineers because of the inroads that PC-based tools have made," according to Karen Wills, product marketing manager at Viewlogic Systems. "If you're looking to develop and market a design tool, a PC platform is more accessible than a Unix one. It only follows that good PC software will be developed to help people use the latest devices, whether they're PLDs, FPGAs or other ASIC technology."

Third-party downside

On the down side, however, is the fact that third-party tools often come later in supporting new devices on the market than the tools of the device manufacturers. The latter, then, usually provide the fastest way of designing in a new part.

The most popular third-party tool by far is still Abel from Data I/O (Redmond, WA). Abel has grown from a strict Boolean transformation software to a comprehensive environment for capturing, synthesizing, testing, programming, and partitioning designs onto PLDs. It's also a plus for Abel that parent company Data I/O is the leader in PLD and FPGA programmers. The company can provide a complete solution for design, prototyping, testing, and production of almost any part in the marketplace.

CUPL may be an old timer by comparison, but it hasn't been standing still in terms of develop-

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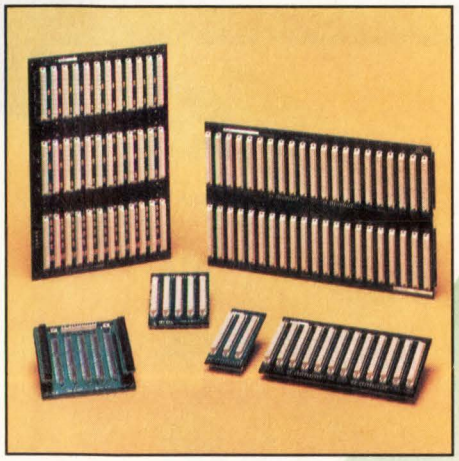

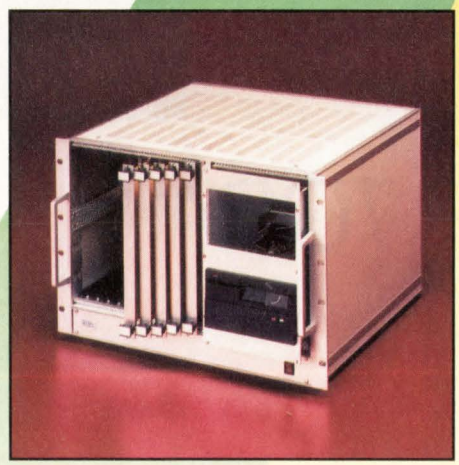

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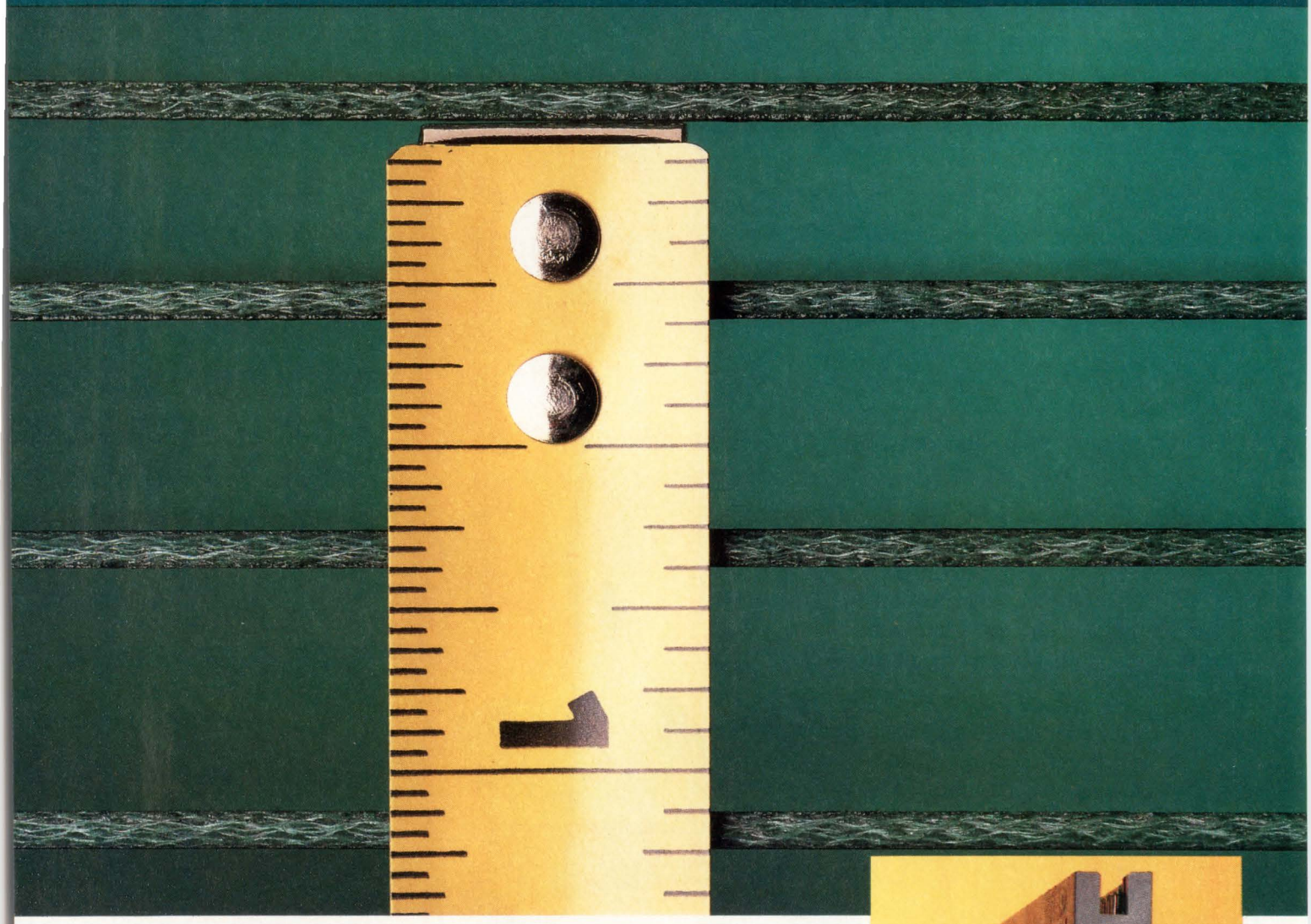
.050 centerline stackers. Close, closer, closest.



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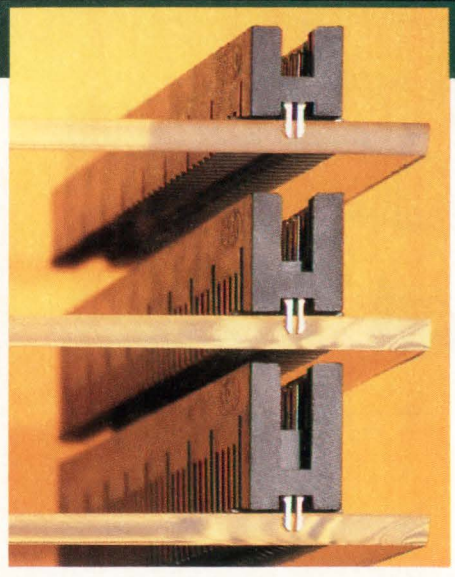

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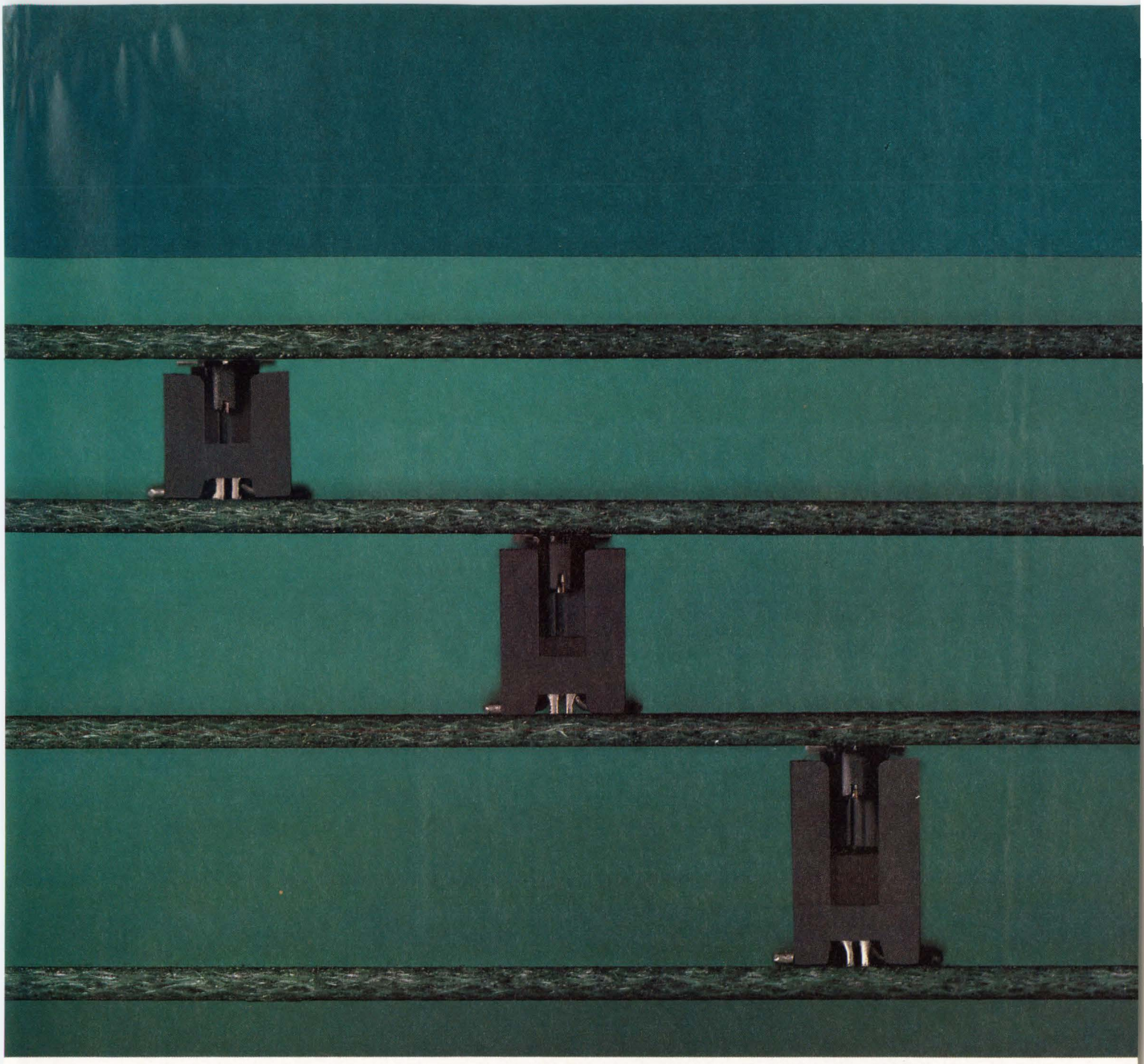

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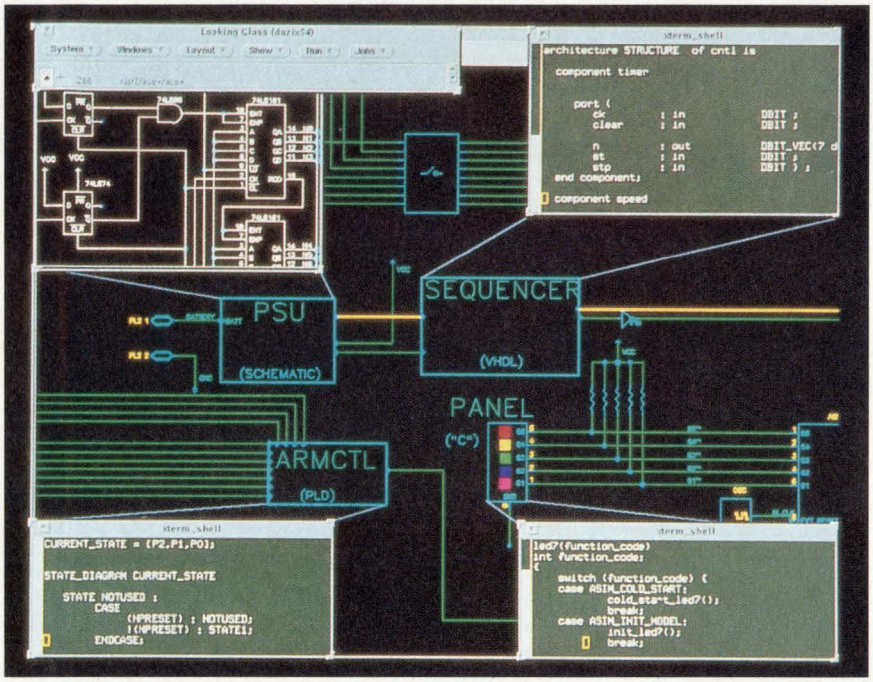
ment and it's still very widely used. Originally developed by Assisted Technologies, CUPL was later acquired by P-CAD, and then was sold to Logical Devices (Ft. Lauderdale, FL), where it's now marketed both with and without the company's PLD and PROM programmers. CUPL has many advanced features, such as mixed input formats (schematic, truth table, Boolean, state-machine syntax, and high-level language constructs), a powerful simulator (CSIM for verification and test vectors) and a choice of one of four reduction/minimization techniques. Although CUPL isn't as popular as Abel and doesn't come from as large a manufacturer as Data I/O, it benefits from the expertise of Logical Devices, which is a PLD and FPGA software vendor as well as a device manufacturer.



Using simultaneous windows, Ace+ PC Entry software from Dazix/Intergraph lets you take advantage of low-cost PCs as entry stations which integrate with the company's higher-powered workstations for ASIC, PCB and MCM designs.

New and traditional approaches

Recent tools from OrCAD, Accel, Omation, Minc, and Adams MacDonald have been hitting the streets with both traditional and new approaches to the PLD design problem. OrCAD, with its OrCAD PLD software, has come up with an advanced syntax and notation for expressing complex functions compactly. OrCAD PLD lets you choose a notation format which is most suitable for a specific design, including schematic capture, compact indexed notation, powerful transformation mapping, and standard Boolean, truth table and state-machine syntax.

Accel's recently introduced Tango-PLD supports 113 PAL, GAL and PEEL devices, including parts from Altera. Tango lets you enter in design equations or schematics, and then performs minimization and reduction before you've chosen a target part. You can then simulate for functional verification, choose a part and generate a JEDEC fusemap. The simulator can model multiple PLDs, meaning that test vectors can be generated for several devices to aid in board-level testing.

Omation's Schema PLD logic compiler also provides schematic capture input. In addition, it accepts Boolean, truth table and state-machine input formats and features a variable-like language to help simplify equations. Schema PLD incorporates minimization (which can be enabled or disabled), as well as reduction (Presto, Quine-McKlusky and a proprietary technique), to help generate resultant equations more efficiently for a particular device's architecture.

A powerful PLD software for PCs is the PLD Designer from Minc (Colorado Springs, CO). Accepting schematic netlists from FutureNet, OrCAD and Viewlogic, PLD Designer also accepts Boolean, truth table and state-machine input formats, and can combine different parts of a design in different formats into one homogeneous whole for single and multiple PLDs.

PLD Designer also features powerful reduction and optimization algorithms for simplifying the PLD design, and has an automated device partitioning and selection scheme. Device partitioning and selection lets you enter such constraints as type of technology (CMOS, bipolar, ECL, or any combination), type of package (plastic or ceramic DIP, LCC, SO), number of devices, maximum power, and speed constraints.

In the next step, PLD Designer checks through its large library of parts and comes up with all the possible solutions that can house the design. You then choose the optimum solution, and PLD Designer generates the fusemaps and documents the design. PLD Designer also includes a simulator which can use waveform entry to define the simulation stimulus pattern.

A unique tool providing synthesis support for a device-independent FPGA design comes from Exemplar Logic (Berkeley, CA). The company's Complete Optimization/Retargeting Environment (Core) lets you target a specific FPGA anywhere in the design cycle. Supporting multiple design entry formats (VHDL, schematic, Boolean in Abel, Minc and Palasm formats), Core permits you to merge new or existing PAL or FPGA designs together, reduce and optimize for a target FPGA and generate fusemaps for that particular flavor of FPGA. Currently supported are Actel, Altera, Concurrent Logic, Crosspoint, Cypress, QuickLogic, and Xilinx parts.

Manufacturers make tools, too

In addition to third-party PLD tools, manufacturers offer tools that aren't to be scoffed at. Take Snap, for example, the latest generation of PLD design tools from Philips/Signetics (Sunnyvale, CA). This streamlined tool links to schematic capture and features waveform entry (for simulation vectors), reduction, minimization, resource allocation, fusemap generation, and programmer support. Although initially targeted for the new programmable macro logic (PML) family of devices, the software is being extended by the com-

pany to cover all its PLDs and has replaced the earlier Amaze software.

Altera (San Jose, CA) also has an advanced PLD design package, called APlus+, which runs under DOS, and Max Plus II, which runs under Microsoft Windows 3.0. The software includes schematic capture, simulation and fusemap generation. Recent introduction of the company's PLS-EDIF translator now lets PC users work with workstations from Cadence, Dazix, Mentor, Valid, and Viewlogic.

Xilinx (San Jose, CA) offers a powerful PC-based FPGA design tool for the PC. The very popular RAM-based Xilinx FPGAs have found widespread use, part-ly due to the good quality of XACT software. Using Viewlogic software as a front end, the highly graphic Xilinx development system places and routes your functions, estimates timing of the resulting design, back-annotates timing information into the Viewlogic Viewsim simulator, generates fusemaps, and lets you hand-tweak resource allocation and placement and routing of critical paths.

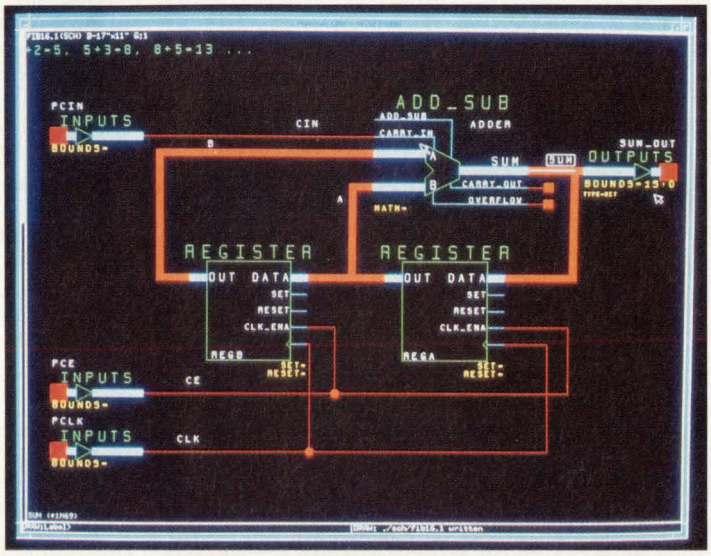
A new Xilinx tool called Blox generates custom cells from user-defined input parameters, much like a silicon module compiler. In addition, Xilinx has forged alliances with Data I/O for Abel support, as well as with Minc for FPGA Designer support.

Actel and Texas Instruments also use Viewlogic schematic capture and simulation capabilities in their software. (Both companies manufacture one-time programmable fusing-link FPGAs.) Primary rivals of Xilinx software, the tools are similar as far as design capture and simulation are concerned, but they're a bit more automated and don't let you manually edit the layout, as do the Xilinx tools.

Some designers feel this is a plus, since it eliminates another step in the already iterative design process; others disagree, feeling it's a minus since design optimization is solely in the hands of the automated tools.

New arrivals

New to the scene is QuickLogic (Santa Clara, CA), which recently introduced the pASIC Toolkit for its family of antifuse-based, high-density FPGA devices created by John Birkner, co-inventor of the PAL. The pASIC Toolkit combines design capture (schematic capture and language entry) with simulation, automatic test pattern generation and place-and-route under Microsoft Windows 3.0. As is the case with Xilinx software, a physical layout and path editor lets you manually tweak designs for optimum performance—important since the device touts a 100-MHz operating speed.



Blox software for Xilinx FPGAs allows you to define functional blocks which the software then compiles to a semicustom cell for use in the Xilinx LCA families of parts.

Another recent arrival is the Lattice Semiconductor (Hillsboro, OR) pDS development system, which also runs under Windows 3.0. While Lattice has provided simple PLD tools for quite some time now to support its popular GAL family of devices, the pDS package is dedicated to the new EEPROM-based 1032 super-PLD. Only providing Boolean entry at present, the software is scheduled to have a schematic capture-based version which will also synthesize logic from VHDL source code. Unique to the Lattice product is the capability of reprogramming the parts in-system while remaining nonvolatile, thanks to 5-V-only EEPROM. The pDS development system generates the fusemaps for in-system programming or for using standard packages.

Other part manufacturers offering PC-based PLD and FPGA design tools include Advanced Micro Devices, Concurrent Logic, Crosspoint, Gould, ICT, National Semiconductor, Plessy, and Texas Instruments.

The PC PCB era

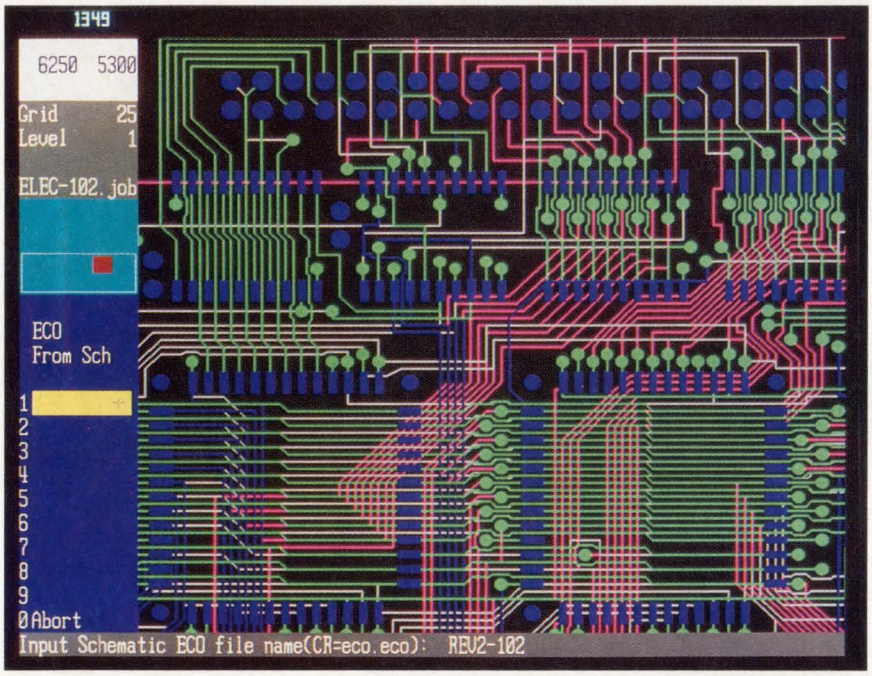
No matter what parts are being designed, sooner or later they'll be fitted into a PCB. This is yet another major area where PCs have made much headway.

The PCB dominates almost every type of electronic system and subassembly. A mature industry, PCB manufacture is still subject to rapid advancements in development tools and methodology, prototyping alternatives, test requirements, and production capabilities and limitations. Reasonably priced and widely available, PCB design tools and services relieve designers of the painstaking, error-prone and time-consuming handwork they had to perform only a few years ago. Such tools provide a uniform design environment from which you can easily place components, wire tracks, verify integrity between schematic and physical layout, and generate artwork for manufacturing. Also, highly efficient autorouters take the headaches out of squeezing traces into dense areas, and some tools even perform parameter extraction and thermal analysis.

Some systems, such as Racal-Redac's Maxi/PC and Cad Star, the Great Softwestern Company's Autoboard, Highwire from Wintek, P-CAD's Designer Series, the Visionics EE Designer series, and ProCAD Xtra from Interactive CAD Systems, provide their own proprietary schematic capture tools tightly coupled to PCB tools. An advantage of integrated schematic capture is the uniformity of the user interface. If you use a common interface, you don't have to master the personalities of several different software packages, and you can be up and running quicker. A disadvantage of this approach is that integrated schematic capture may be clumsy or lacking in some features which you

require or desire, such as automated bus member labeling, auto-incrementing reference designation or on-line library editing. You don't want to pay for redundant software, so whatever is currently used in-house should play an important role in decision-making, unless it lacks some crucial feature.

In the latter case, you may want to put your own system together. Some companies, such as Accel, Omation, OrCAD, and Pads, let you choose third-party schematic capture tools as front ends to their PCB design programs, or you can use bundled tools from the same company.



The quality of a PCB designed using a PC-based layout tool can be just as good—or better—than that achieved using a high-end workstation-based tool, since the deciding factor is really the designer's experience. This PCB designed on a Pads PCB Designer is a case in point, and is as good as one designed on a workstation-based layout tool.

An early entry in this area, and still a strong one, is P-CAD's Master Designer PCB design tool, boasting over 14,000 installed systems. Integrating tightly with the parent company's or third-party schematic capture tools, Master Designer has the power to handle up to 32 layers of a 60 × 60 in. board with up to 2,500 components, 4,000 nets and 32,000 pins. Master Designer also has special rules, such as filled polygons, trace hugging, curved traces, and trace plowing, to help analog designers create analog or mixed analog/digital PCBs.

An extensive PCB library includes surface-mount as well as throughhole-mounted devices. Design aids such as rat's nesting and rubber banding make placement iterations easier, since uniform trace density becomes visible. In addition, a rip-up and reroute router guarantees 100 percent route completion, even when priority routes are defined to help minimize the trace length of critical path signals.

OrCAD, Omation, Accel, Visionics, Racal-Redac, Ultimate, Wintek, and others also provide fine PCB design tools. The OrCAD PCB II software now features a rip and reroute router; backannotation support; PostScript, IGES and DGIS graphics support; and a more comprehensive surface-mount library. Again, the user interface follows OrCAD's tradition of pop-down menus, macro support and flexible I/O device support, making OrCAD PCB fit easily into OrCAD's or your existing design center.

Omation's PCB software, Schema PCB, also has some nice features. An autoplace option speeds part entry. Calculated minimum distance algorithms facilitate ideal placement of components. Autoplacement is almost always modified by a designer, but the function saves time in instantiating and relocating every component on the board. Connection rat's nesting and rubber banding are also provided to help optimize placement.

Accel's latest PCB tools are also outstanding. The new version of Tango PCB/PCB Plus Version 2.X adds many features to this already smooth, effective and easy-to-use program. Tango PCB now provides polygon support for analog design assistance, automated component placement, autopanning, keyboard macros, backannotation, and enhanced expanded memory specification (EMS) support. Another improvement is a multipass maze router, which breaks up routes to speed up the routing process and utilize memory more efficiently. A nice feature of Tango PCB is the ability to check physical layout against a schematic to verify that what you've gotten is what you want.

Visionics (Santa Clara, CA) offers an advanced PCB layout and design package which is still among the top contenders. Although Visionics offers the EE Designer III integrated design environment for schematic capture, logic simulation, linear simulation, and PCB design, the company also markets its PCB design tool separately for those who want to use a different front end.

The EE Designer III layout package features a clean user interface which uses a shell structure to walk through each design phase. The automated place feature speeds design instantiation and gives a good overall starting point from which to optimize component placement. In addition to rat's nesting, EE Designer III also features force vectors to aid in component placement.

One feature that makes EE Designer III stand out is its thermal analysis capability. This feature calculates component and junction temperatures as well as board temperature gradients. Parameters from a library file or ones that are interactively loadable or editable include board dimensions, board thickness, conductivity, copper thickness, component package types, package thickness, cooling (emissivity coefficient), and much more. Analysis is displayed as a temperature map on the screen.

What you sim is what you get

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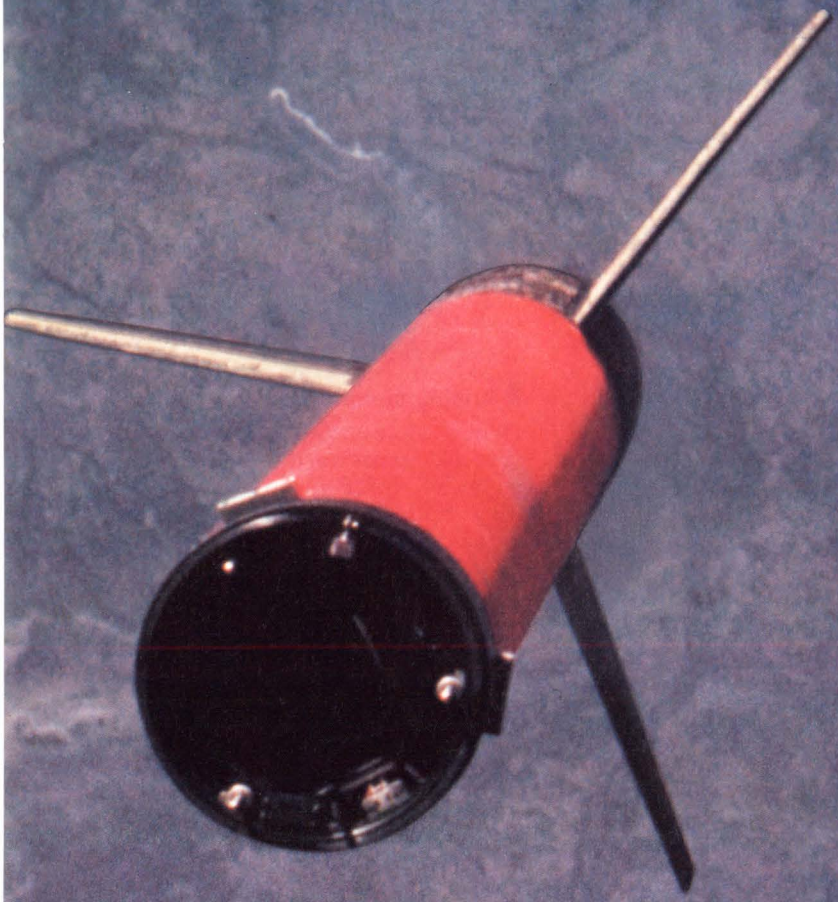

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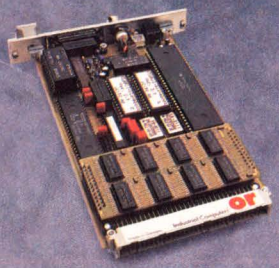

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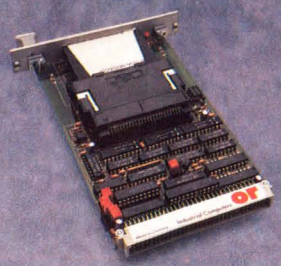

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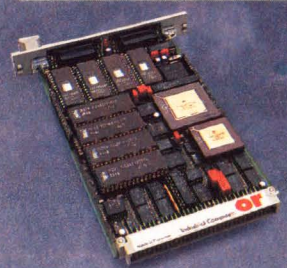

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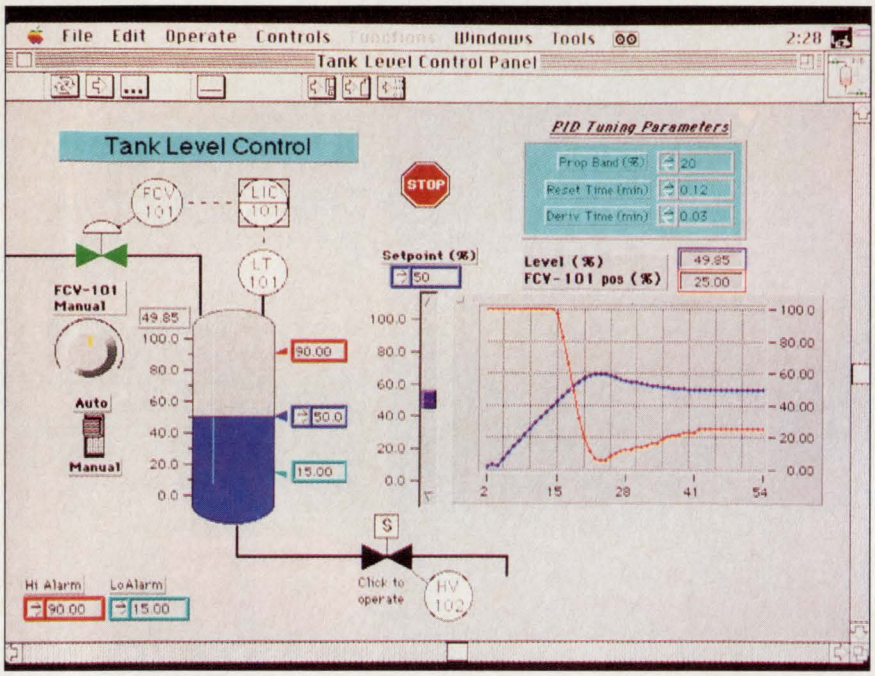
tors include OrCAD, Aldec, Cadat, and Mimic. Their programs accept netlists from schematic capture programs and let you verify the functionality of designed circuits, as well as timing characteristics.

OrCAD VST simulation tool is a powerful yet moderately priced digital simulator which is easy to use, fast and well integrated into OrCAD's design environment. VST features the same interface as OrCAD's SDT tools and can accept commands via keyboard, mouse or



LabView, LabWindows and DAQ Designer from National Instruments let you acquire data, control processes and set up virtual instruments on a PC using plug-in cards as well as remote equipment connected via RS-232, IEEE-488 and VXI interfaces.

combined for highest-speed use.

A trace editor feature lets you create, load and save stimulus and test pattern vectors with absolute or relative timing characteristics. Signals displayed in logic analyzer format can be individual (bit), nibble, byte, and word length displayed in a hex radix. Up to 16 breakpoints composed of AND/OR conditional statements can vector you to the events in question quickly, and up to three simultaneous markers permit rapid extraction of simulated time intervals. OrCAD VST comes with a basic library of TTL, CMOS, ECL, and memory devices. User-definable models are available so you can create your own simulation components.

The Susie (Standard Universal Simulator for Improved Engineering) from Aldec (Newberry, CA) is one of the most powerful of the PC-based logic simulators. It's been adopted by Accel, Omation, P-CAD, and others as part of their design environments. The present version, Susie 6.X, features a streamlined user interface which lets you load netlists from schematic capture programs, define input waveforms for circuit stimulus (from waveform entry, tabular vector lists and program-supplied stimulus generators), and perform accurate unit delay and timing simulations for single chips, PLDs, ASICs, and circuit boards. Susie's power comes from speed. Completely memory-resident models live within the PC, meaning that disk accesses and memory swaps that drastically slow performance aren't necessary.

A second important feature of Susie is its ability to accept high-level models in either Aldec proprietary format or VHDL. This permits a PC to simulate microprocessors, ROMs, RAMs, and other VLSI functions behaviorally, along with PLDs, TTL, CMOS, ECL, and GaAs components—all with a high degree of accuracy (10-ps resolution) and speed. Simulation models available from Aldec include microprocessors and peripheral chips from Intel, Motorola and Zilog, and third-party VHDL models from Logic Automation and Quadtree.

Another powerful digital simulator is integrated into Viewlogic's Workview. While Workview is a fully integrated and automated design environment, the schematic capture and simulation packages are available bundled for designers. Like Susie, Workview can accept high-level VHDL behavioral models, and it simulates quickly and accurately on a PC. It also integrates with linear simulation, and can network easily for multiuser design support, which is especially important if design teams will be working on different parts of a project. Workview's clean and effective user interface lets you open up a window for each task, making it easier to iterate through the design process.

Analog simulators

Digital simulation is not the only type of circuit verification possible on a PC. Analog simulators from MicroSim, Intusoft, Tesoft, Etron, EEsof, Interactive Solutions, Meta Software, and others permit accurate linear predictions of designed circuit performance. PC-based analog simulators are mostly based on Spice, a public-domain analog simulation scheme developed at the University of California at Berkeley.

The most widely used to date is Pspice by MicroSim (Irvine, CA). It accepts Spice netlists and generates waveforms from selected nodes as a result of user-defined input stimuli. Pspice is available in different flavors for DOS, Windows, stand-alone analog, and mixed analog/digital simulation. It's useful for determining proper responses to filter design, amplifier stability, noise and impulse response and immunity, and much more. Monte Carlo analysis lets you vary parameters on a random basis, showing yield deviations from tolerance differences between components. The Probe program in Pspice lets you probe on selected nets and display stimulus waveforms right next to resultant waveforms at different points in the linear signal path.

Another improved Spice derivative is the ICAP/386 software from Intusoft (San Pedro, CA), which features behavioral modeling, mixed mode capabilities, Monte Carlo analysis, and sensitivity analysis.

ICAP/386 also integrates a schematic capture program with its simulator. While it and most other analog simulators can accept netlists generated by third-party tools, the integration of schematic capture

streamlines the back-and-forth iterations of design and verification. It also simplifies stimulus and response queries, since you can place iconic probes and signal generators directly into the schematic.

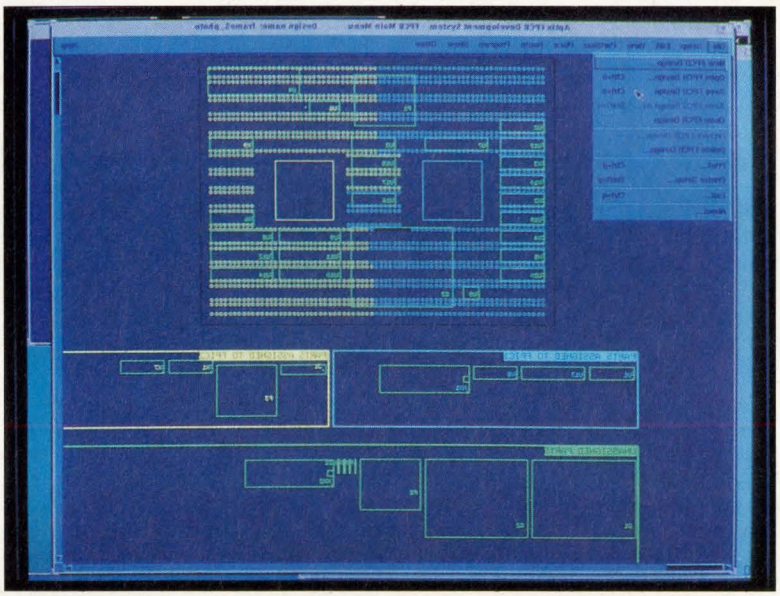
Analog simulators aren't limited to linear ICs and transistors. Tesoft (Roswell, GA) provides an interesting product, the Tess (Transient Electronic System Simulator), an interactive communications block diagram simulator that's easy to use and very effective. Instead of simulating the physical effects of transistor devices, it uses a block diagram approach where every block has its own set of transfer functions and parameters. System-level advanced analog simulation takes place very quickly, and as accurately as you need it to be.

Tess is useful for simulating complex analog circuits made up of blocks such as phase-locked loops, audio companders, filter networks, voltage controlled oscillators, phase detectors, function generators, and demodulators. The simulator accepts netlists from OrCAD and P-CAD, and generates clean and visible output plots with powerful features such as spectral analysis, mixed log and linear plots and Lissajou patterns. Since each block is effectively a black box, digital circuits can be simulated too. It's also important that Tess simulates the interfaces between digital and analog circuits.

Another product, RF Notes from Etron Radio Frequency Enterprises (Diamond Bar, CA), is aimed at radio frequency engineers who need to verify filter responses, modulators/demodulators, phase-locked loops, strip line capacitance, resonant circuits, impedance matching, and other specialized RF effects. Menu-prompted queries guide you through parameter entry to resultant response plots of the circuit. In addition to electrical calculations, RF Notes also models magnetic parameters, making transformer, inductor, torroid, and wire size calculations accessible. This is useful for the design of high-speed digital PCBs and sensitive analog circuits.

XTK 4.2 simulation software is a unique product from Quad Designs (Camarillo, CA) that spans the analog and digital worlds; it's the first software to predict the effects of ground bounce on PCBs. Combining circuit information from schematic capture with layout information from PCB design systems, Quad Designs software can predict crosstalk, ground inductance, power factors, backplane effects, transmission line effects, ringing, and over- and undershoot. Of special importance when working with high-speed circuits and mixed analog and digital circuits, XTK's unique abilities can be invaluable to uncover layout-induced errors on critical system designs before going to production.

Similar to XTK is the Contec CAE (CCAE) simulator from Contec Microelectronics USA (San Jose, CA), which supports high-speed digital and analog PCB, MCM and ASIC designs. Along with the company's ContecSpice simulator, this software predicts voltage spikes, crosstalk, impedance mismatch, and reflections in layout of signal traces. In addition, high-frequency clock distribution trees associated with signal skews that can offset critical timing can be modeled.



The Aptix PC-based development system lets hardware prototypes be tested immediately instead of having you wire breadboards together. Computer-based wiring changes can optimize a design, and instant connection to logic analyzers is achievable without having to connect dozens of microclips in hard-to-reach places.

The PC as a development system

The microprocessor has made the PC possible, but it's also true that the PC has made low-cost and accessible microprocessor development possible. The PC has been instrumental in facilitating the design of microprocessor-based systems, on both the hardware and software sides. So effective are third-party microprocessor development tools, in fact, that microprocessor vendors often don't offer their own development systems anymore.

Microprocessor design is simplified when the code can be debugged on the native system. For example, when writing code for a Z80, a Z80-based PC is ideal to write the source code and assemble, compile and then debug it. But it's unlikely that every microprocessor and microcontroller has a native PC which can be used to debug new code. Instead, dedicated external development systems which can connect to any computer have become the standard, thanks to standard ports such as the RS-232 and Centronics parallel ports. As a result, the most popular computer in use today for microprocessor- and microcontroller-based design and code development is, again, the PC.

"There's a large segment of the market who make PC chip sets, peripherals and PC compatibles who want to develop their next-generation products on their own systems," says Bruce Kane, director of PC products at Racal-Redac (Westford, MA). "It's not only a matter of loyalty to their own products, it's simply more cost-effective for them to use their own equipment. Fortunately, there are plenty of PC-based tools that let them assemble a complete design environment in-house with their own platforms."

PC-based tools available for such

development include PROM programmers, in-circuit emulators, logic analyzers, ROM emulators, assemblers, compilers, and debuggers. Dozens of companies offer PROM programmers; some noteworthy ones are Data I/O, Logical Devices, Quantec Systems, Stag, and Storey Systems. Likewise, more than a dozen companies provide in-circuit emulators for microprocessors, including American Automation, Hewlett-Packard, Huntsville Microsystems, Kontron, Metalink, Nohau, Orion, Signum Systems, and Sophia Systems. Popular micros supported by these companies are from AMD, Intel, Motorola, National, NEC, Philips/Signetics, Texas Instruments, and Zilog.

Developing DSP, too

One area especially well-suited to the number-crunching abilities of the PC is DSP applications. Digital circuits have demonstrated their effectiveness for dealing with analog functions in many applications, and DSP is a rapidly growing area absorbing more analog designs every day. While typically more expensive to implement than analog, DSP provides many key benefits, making it the ideal choice for many of today's signal processing tasks. With the introduction of DSP chips from vendors such as AT&T, Analog Devices, Motorola, Star, TI, and Zoran, to name a few, designs once in the realm of hardcore analog designers using discrete analog components are now found in the digital designer's arena.

One recent offering targeted at the emerging multimedia market comes from AT&T (Allentown, PA), which provides development hardware and software for its video compression/expansion chip sets for JPEG and MPEG. Another is from Analog Devices (Wilmington, MA), which makes available the EZ-Lab development board and software to support the company's DSP chips.

Perhaps the most impressive PC-based DSP development system comes from Star Semiconductor (Warren, NJ), which manufactures the Sproc DSP chip containing four processors. It handles data up to 24 bits wide through two serial inputs, two serial outputs, a bidirectional parallel port, and an independent probe port. Unique to this system is your ability to design and test a DSP application without having to write a line of code. SprocLab software transforms your schematic into code that's directly executable by the Sproc chip and can be tested on an evaluation board that comes with the development system.

There are many other engineering areas where the PC is beginning to find extensive use. To detail these fringe technologies would fill an encyclopedia. Among such applications are neural computing, mechanical design and drafting tools, reliability software, and CASE tools. ■

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Post Script

What's ahead for PCs in the engineering world? While 286s are still out there, the platform of choice today is the 386. The 486, with on-chip math coprocessor and cache RAM, will probably replace the 386 over the next two years.

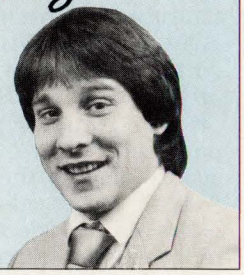
PS/2 and some clone manufacturers are relying on Micro Channel bus architecture, but the standard AT bus or the ISA bus remain more popular. Micro Channel is faster, making it better for networks, but engineers usually need faster processor speed, not faster bus speed. EISA is going to be the next bus standard, because if offers both Micro Channel speed and compatibility with AT-bus expansion cards.

Plagued with bugs and crashes, the multitasking OS/2 operating system never had a major impact on the engineering community. Instead, as noted in this article, the OS of choice is Windows. Windows already takes care of many device drivers and system interfaces, letting you concentrate on other things, like your job. For more demanding applications that can't afford the slow speed and high overhead of Windows, DOS will continue to be available.

A multitasking operating system that may give DOS a run for its money is Unix, which seems to be migrating down from larger machines and gaining popularity in the PC market. But Unix requires a great deal of RAM and disk space, and it's less easy to learn.

Apple is offering the Mac to the engineering community—and it has some attractive features, such as a multitasking OS, a powerful processor and an icon-based user interface. It lacks the third-part support of the IBM, though, and the latter will remain the mainstay for CAD/CAE engineers for years to come.

Jon Gabay



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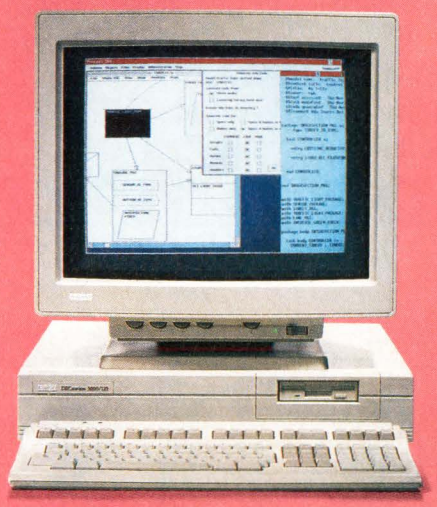

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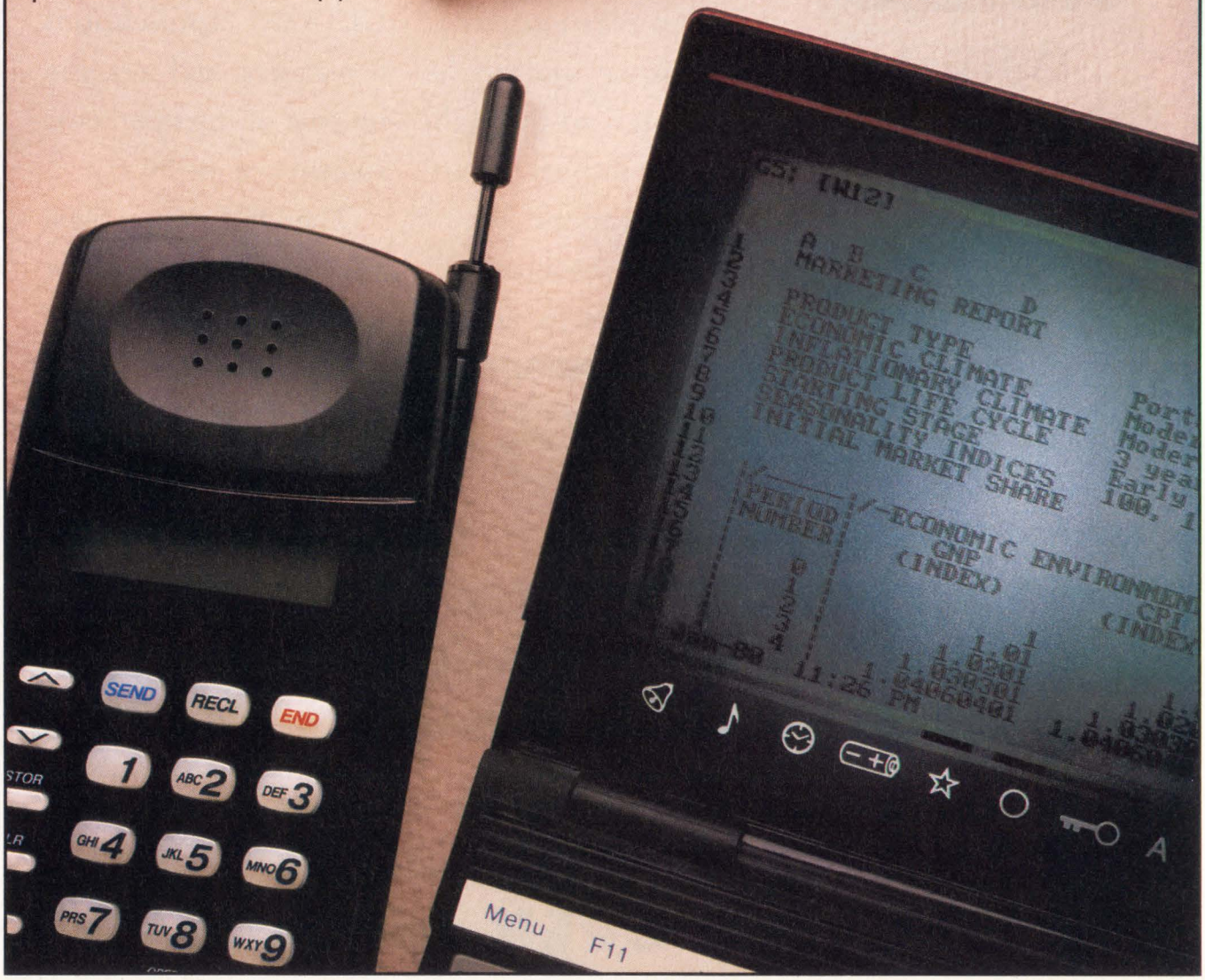


CIRCLE NO. 53

The fastest single-shot scope in the west

The HP 54700 series design team. Standing, left to right: Allen Montijo, circuit/system design engineer for hardware and software; Pat Byrne, R&D section manager for chip development; Mike McTigue, R&D project manager for plug-ins; John Scharrer, R&D section manager for high-performance oscilloscopes; Mike Manley, manufacturing manager for high-performance oscilloscopes; and Dave Long, R&D project manager for software. Seated, left to right: John Campbell, mechanical engineer for system box design; Dale Walz, thick-film hybrid R&D engineer; Tom Uhling, probe development engineer; and Ken Rush, R&D project manager.

The new HP 54700 series digitizing oscilloscope from Hewlett-Packard (Colorado Springs, CO) represents an absolute triumph of mixed-signal design. Not only did the design call for custom attenuators, a new converter technology, thick-film hybrid mixed-signal circuitry, and several analog and digital custom IC designs, but it also required the development of a high-speed real-time computer system and display processor to boot. It's hardly surprising that the project represented the cumulative effort of several divisions of the company.

The company set the goal of designing a single-shot digitizing box, according to John Scharrer, R&D section manager for high-performance oscilloscopes, to outperform the fastest analog storage oscilloscopes available. To accomplish this, the new design needed to achieve 1-GHz-bandwidth single-shot capability—meaning a sampling rate of no less than 4 Gsamples/s.

Potential customers for the new instrument were pushing clock rates beyond 40 or 50 MHz in their designs—running into difficult signal integrity problems on their printed circuit boards (PCBs) and in their multichip modules (MCMs). They needed the ability to probe signals unobtrusively in searching for problems such as ground bounce, undershoot and overshoot—problems that sometimes occurred infrequently.

Dave Wilson, Senior Editor

"We wanted to let designers trigger on a signal and then look back in negative time to observe and characterize those rarely occurring, very narrow pulses," Scharrer says.

When the project was begun, there wasn't much off-the-shelf technology to help the HP design team build such a product. "Whether it was the mechanical box, the software design, the digitizer, or the probe, we designed everything from scratch," Scharrer adds.

Prior to the development of the new HP box, high-performance oscilloscopes were analog in nature. "Our vision," says R&D project manager Ken Rush, "was to replace the analog system with a digital machine." Using digital techniques, the new scope could capture, analyze and display data at high speed. So as not to disappoint designers accustomed to interpreting data displayed on an analog scope, the HP design team even went so far as to make the display "look and feel" like its analog counterpart.

Probing the problem

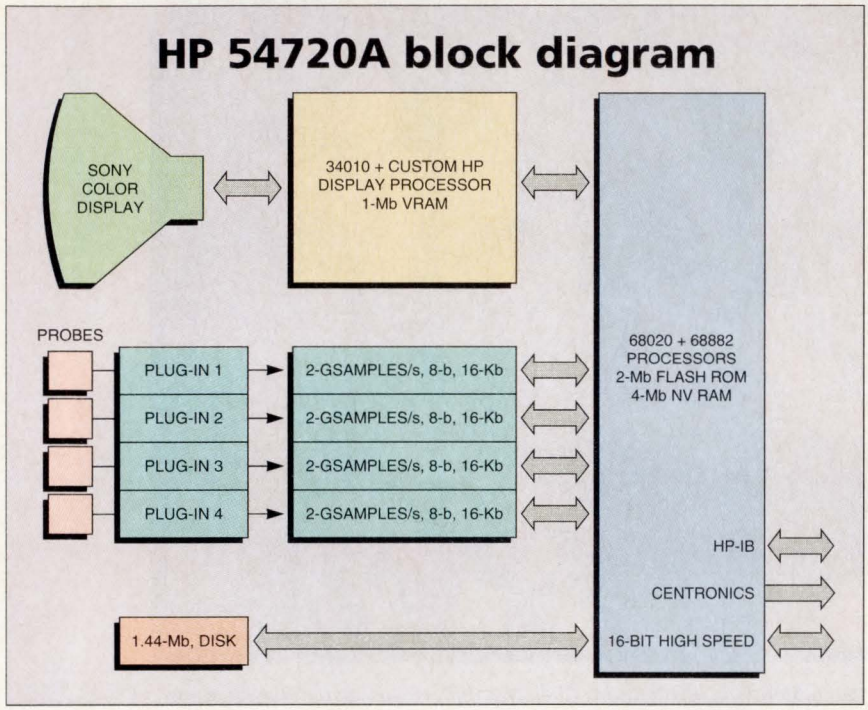
Conceptually, the new oscilloscope was built around five major functional elements that were designed concurrently. They comprised probes, a number of plug-in modules used for attenuation and amplification, a conversion subsystem, a processing and display subsystem, and a custom Sony display.

Tom Uhling, designer of the HP 54701A active probe, admits that probes have traditionally frustrated many scope users. That's because the probe can change the characteristics of the circuit being measured by loading it, so designers have no idea whether they're seeing a "true" signal or not.

Typically, active probes have been designed in the past using FET technology. But to maintain a high input impedance and lower input capacitance, especially important when dealing with high-frequency signals, HP decided to use bipolar technology instead. The results were worth it. HP's new HP 54701A active probe offers some impressive specs—0.6-pF input capacitance and 100 kΩ input resistance with up to 2.5 GHz of bandwidth.

Bipolar transistors offered other benefits to Uhling as well. "They're more robust than FETs," he says. FETs are easily damaged by electrostatic discharge and it's common for probes based on FET technology to be destroyed when inadvertently exposed to 100-V sources, rather than the 5 V they were designed to work with. The HP probe, on the other hand, is very robust. "It's specified to withstand 200-V ac but we've tested it to 600-V ac," Uhling claims.

Inside the probe, the input signal is routed to a 10:1 attenuator; from there it's fed to a high-frequency amplifier comprising four microwave bipolar transistors. The output from the amplifier is then fed to a 50 Ω cable. At the same time it's sensed and fed back to the amplifier through an op amp. "Radio frequency amplifiers typically don't have good dc performance. They drift unless you build an op amp in the feedback path to compensate for it," says Uhling. That feedback circuit also solves the problem of "thermal tails" on the RF amplifier. Thermal tails occur as a result of the heating that occurs when a pulse is fed into an amplifier. A pulse causes the temperature of the transistor junctions to rise and hence changes the bias conditions of the amplifier—the transistors cool off as heat dissipates through the ceramic substrate. Left uncompensated, such an effect would cause an erroneous signal to be sent into the attenuator section of the scope.



Inside the 54720A digital scope. High-speed signals are attenuated and amplified by dedicated custom plug-in modules, then fed to a custom hybrid converter where they are digitized before being sent to a real-time custom computer for analysis and display.

Functionally modular

Plug-in modules perform signal conditioning functions such as attenuation and amplification. An important part of the new scope, they're accommodated by four different plug-in slots in the box.

All of the plug-in modules can be inserted and withdrawn from the scope while it's under power. Although the ability to reconfigure the scope without shutting off the power is clearly of benefit to the customer, the HP team wasn't always sure of the merits of the idea. "Initially, we were going to put a warning on the front panel not to remove the modules while the box was running," says Scharrer. "We even designed a front panel with warnings on it. Then we realized we weren't solving the customer's problems."

According to Mike McTigue, R&D project manager for the plug-ins, the need for them was driven by customer demand. "Some customers want high impedance on the input so that they can use standard passive—rather than active—probes. Some of them have high bandwidth requirements, while others need ac

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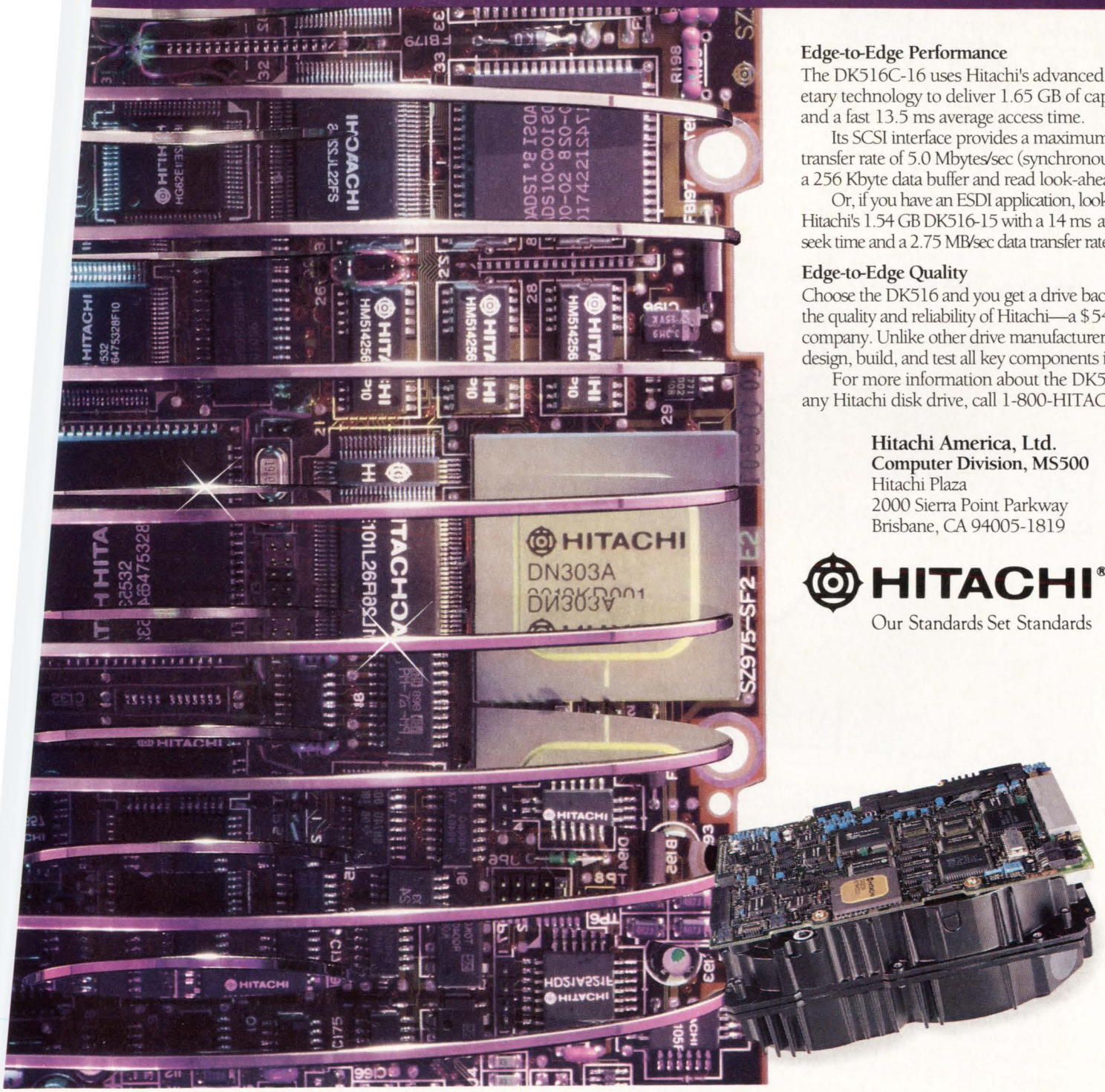

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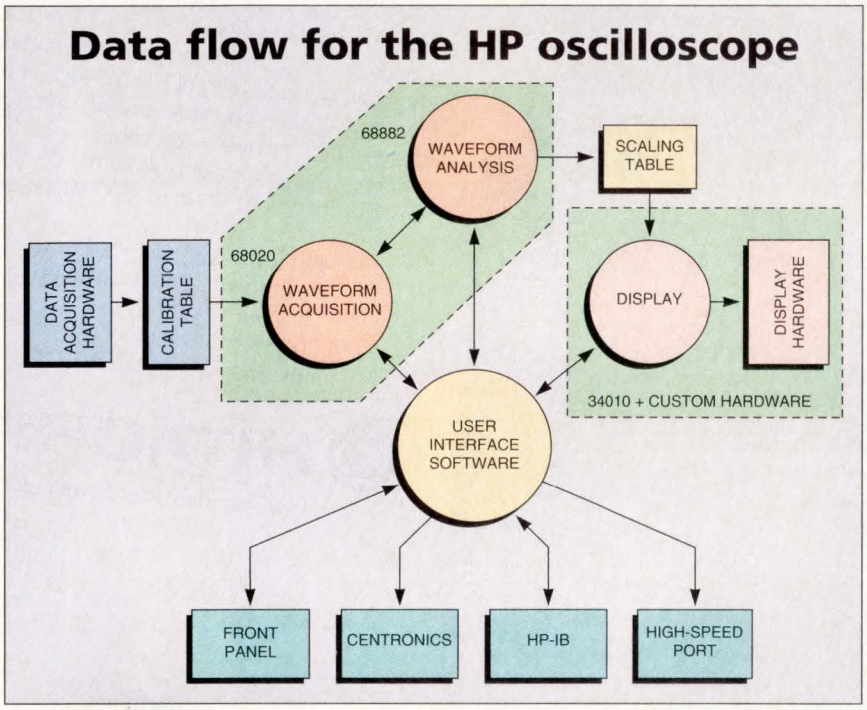
coupling so they can look at small signals riding on a lot of dc. Others need to perform extensive filtering—maybe they have a lot of high-frequency noise riding on the signal and need to filter it out," he says. To meet this broad set of requirements, HP developed several plug-in modules for different applications.

Prospective customers were also interested in interleaving the plug-in modules to increase the single-shot bandwidth of the signal that can be measured. "A plug-in is a way to interleave input signals to obtain higher sample rates," according to McTigue. "If you interleave them, you can get 2 × 2 Gsamples/s, or 4 Gsamples/s."

The concept of plug-in modules also had some benefits for the scope's designer. "If we didn't use modules, we would have to put microwave switching back in the frame of the scope, and that would have been more expensive," adds McTigue.

HP debuted a number of plug-ins modules when the company introduced the new scope. But the plug-in that permits access to the highest digitizing rate—and the one that was the most challenging to the design team—is the HP 54721A. A two-wide plug-in, it accommodates two channels of 1-GHz, single-shot simultaneous bandwidth and has 4 Gsamples/s capability. "This is the plug-in that lets us replace the analog architecture of the past. It's the highest bandwidth single-shot channel you can buy," says McTigue.

The most critical parameter was the timing of the two outputs from the plug-in, which had to be routed to the two A-D converters. The design team had to achieve better than 1 ps of alignment between the signals. "This plug-in takes a 50-Ω input signal, runs it through a microwave attenuator, then puts it through an internal amplifier that drives two vertical 50-Ω signal channels and one 50-Ω trigger channel. All three outputs have a bandwidth better than 1 GHz, and a timing alignment between the vertical channels of better than 1 picosecond," McTigue says. "That took some doing."



Dedicated hardware was necessary to get system throughput to an acceptable performance level. The acquisition and analysis of the waveforms are tightly coupled processes—the 68020 is used predominantly in the acquisition process while the analysis software makes heavy use of the 68882. Dedicated hardware was built to handle calibration and scaling functions, as well as to take care of variable persistence.

A new converter architecture

After attenuation and amplification, the signal must be converted into digital form prior to processing and display. HP's goal on the converter subsystem was to achieve a sample rate four times as great as on its previous generation of instruments. But, while HP wanted to make a 4:1 leap in sample rate, it had to do so using only a 2:1 improvement in IC process technology. To pull it off, the analog subsystem designers rethought the whole architecture used in the conversion process.

A new architecture, called sample-and-filter, was critical to the success of the project. It replaces and betters the industry-standard methodologies of sample-and-hold or track-and-hold. "Conceptually," says Pat Byrne, R&D section manager for chip development, "the sample-and-filter subsystem comprises a sampler, four filters and two dual A-D converters, as well as memory." All of these items were designed and manufactured by HP.

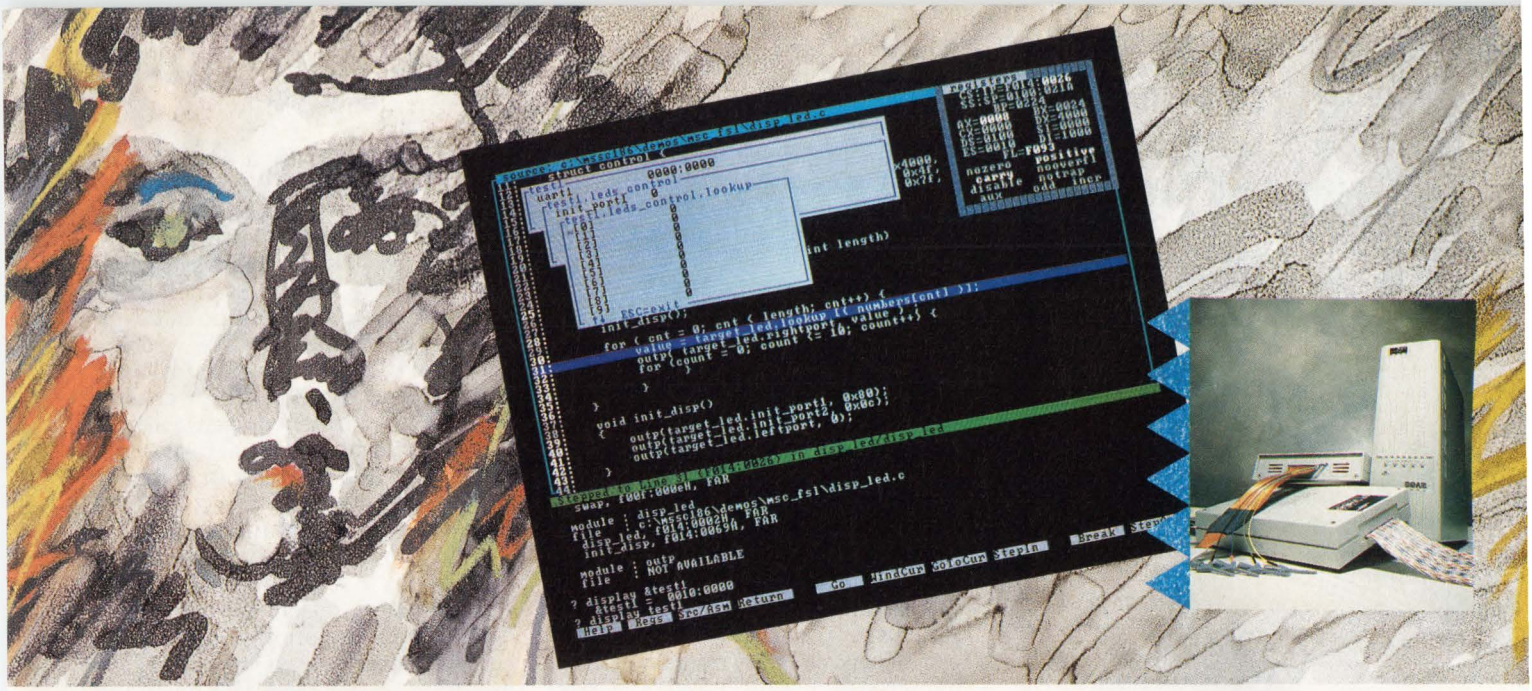
The sampler is a 500-Msample/s bipolar IC. Interleaving the four samplers in time achieves a 2-GHz sample rate. The low-pass filters are printed LC (inductance-capacitance) ladders networked on thick film. The filter response is matched to the sample rate to minimize noise and intersymbol interference. Digitization is carried out by two dual 500-MHz silicon bipolar A-Ds. Interleaving the voltage of the two 7-bit A-Ds results in a resolution of 8 bits. Data is stored in two 4k × 16-bit 500-MHz fast-in slow-out (FISO) CMOS memory devices.

All the custom devices designed for the sample-and-filter subsystem are packaged on thick film. Indeed, the design itself couldn't have been realized without such a thick-film package, because signal integrity would have been lost at the interfaces between the devices.

Computer design was key

"The goal of the computer subsystem is to display a picture of the signal, while giving the impression that the signal being probed is tied directly to the screen," says Dave Long, R&D project manager for software. That meant getting 250,000 to 500,000 waveform data samples onto the screen every second. "The computer has about two microseconds to process each point," Long adds.

To do the job, HP built the scope's computer hardware around a 16-MHz Motorola 68020/68882 combination, a Texas Instruments 34010 graphics display processor, a lot of custom specialized hardware to as-



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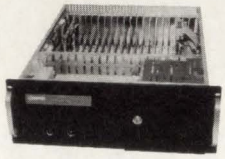

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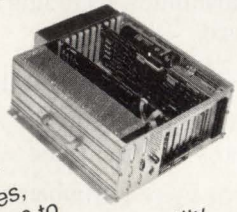

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sist the processor, and the pSOS real-time operating system. This array of parts was chosen because it was consistent with code that HP's software engineers had written in the past.

With previous HP designs, the computer would be purchased off the shelf and software engineers hired to code it, but the HP 54700 project was different. "With the HP 54700, we did the software design first. We then optimized the hardware for the execution of the specific algorithms," says Long.

Customized hardware, for example, was employed to calibrate the data from the A-D converter. Since no converter is entirely linear, some points need to be corrected before being processed or displayed. To correct the nonlinearity errors, HP designed a hardware read-through table. When a sample is read out of the acquisition system, it's corrected as it passes through the table—and before the processor sees it. Another example of a custom assist is a hardware table used to scale graphics data after analysis but prior to display.

A two-processor solution was chosen after careful analysis showed that earlier HP oscilloscopes were spending up to 90 percent of their processing energy erasing old data points from the screen. "It's a complicated problem keeping track of where the points are, how long they have been there, and when they need to go away. We found that actually drawing data points took a lot of time and was a slow process too," says Long.

Although Long's team chose to use a Texas Instruments 34010 processor as the display processor, there were certain capabilities it lacked. One was the ability to handle gray-scale variable persistence. Variable persistence lets new data appear very bright on the screen, while at the same time older data is shown fading out in intensity.

The older analog scopes boasted this capability, and designers had developed a knack for interpreting the rate at which the signal faded away. Unfortunately, since the 34010 didn't have the requisite features to handle it, HP's design team emulated the phosphor persistence of the analog design by building a dedicated custom processor just for that purpose.

To discover the features that designers preferred in a scope interface, HP wrote an X Windows application that modeled the look of the scope on the screen of a workstation. Eventually, this X Windows application, used as a simulation for the front panel, was turned into a development environment. "We wrote a lot of the code on the workstation in ANSI C and ran it on the workstation. Once we finished, we were able to recompile on the actual target and have it up and running in a day or two," says Long.

"After we had finalized the user interface on the scope, we then took the box out to users and made some final changes based on more user input. At the beginning of the project, we weren't sure if we would gain anything or not from the modeling process, but in the end it was worth it," Long concludes.

Cost of ownership

Ken Rush says that when HP started the project, cost-of-ownership issues were carefully analyzed. At just under $30,000, the price of the scope isn't unreasonable, but it's still high enough to make ownership prohibitive. "When a scope breaks, the customer has traditionally paid about $100 per hour for labor to get it fixed. Although we can isolate a bad board and swap in a new one in 10 minutes, it might take another three hours for the technician to recalibrate the instrument," says Rush. To circumvent that expensive scenario, Rush's engineering team decided to incorporate the calibration standards right into the instrument itself. "We designed the whole instrument so that there are no potentiometers inside it. You don't have to take the cover off and tweak things to calibrate it," he boasts.

A similar problem arose over updating or changing software internal to the instrument. Usually, UVROMs or UVPROMs are used in HP equipment for firmware storage. While reliable, problems can arise should the software ever need to be changed or modified—the instrument must then be taken apart and new ROMs inserted. "That's a pain in the neck," says Rush, "so on this machine, we installed flash EEPROM so that we can download code via a disk drive in the system." According to Rush, flash EEPROMs were chosen because they are very reliable in a hostile environment. ■

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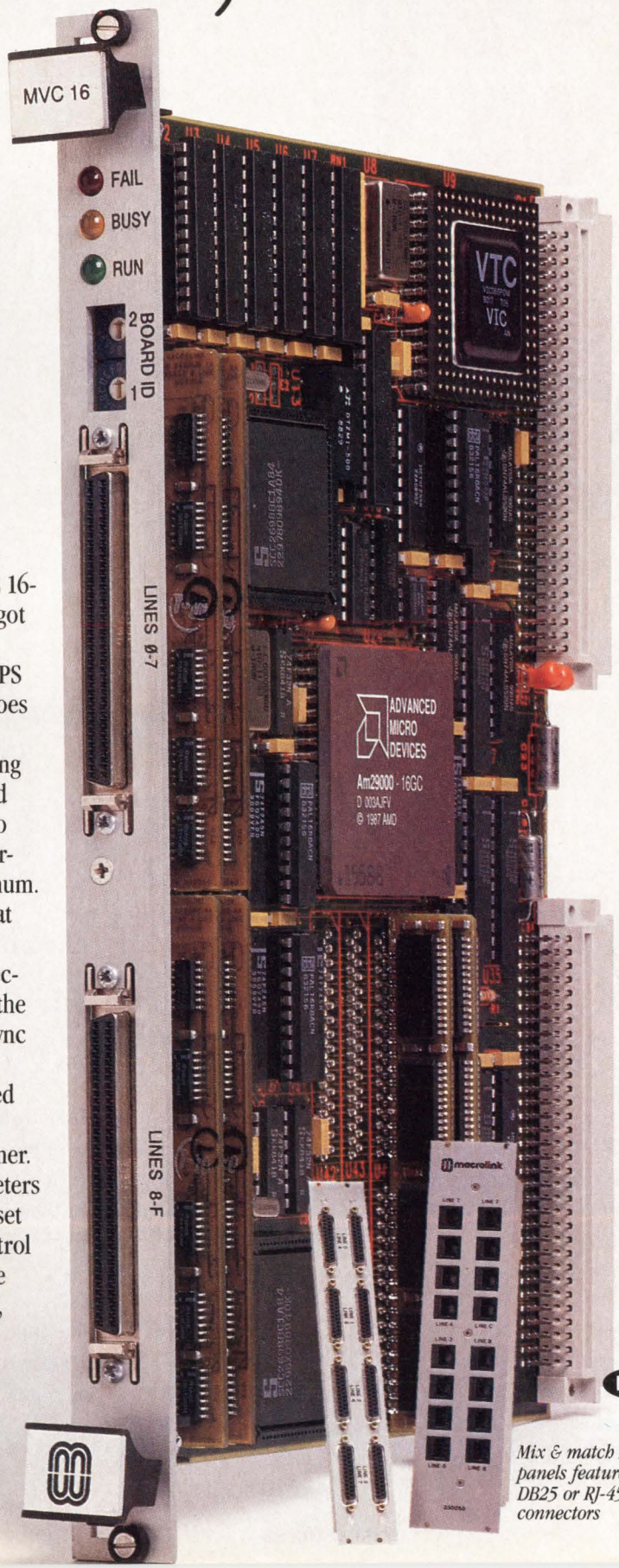

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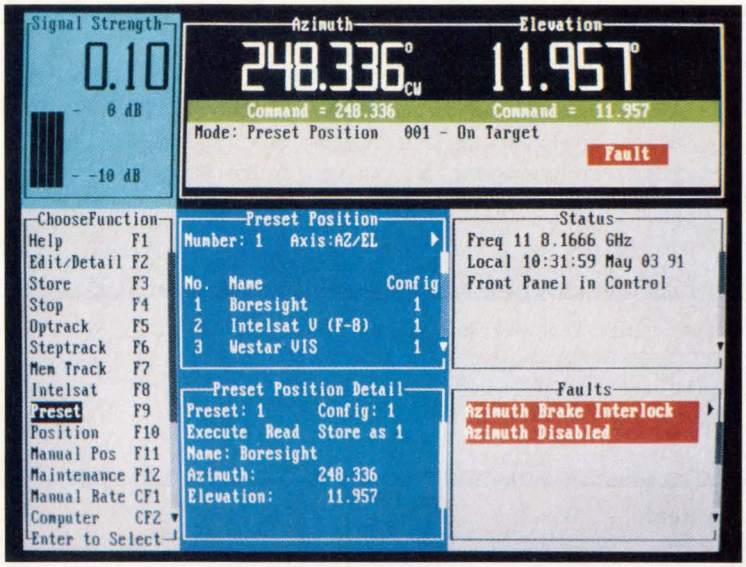
CIRCLE NO. 58

SOFTWARE & DEVELOPMENT TOOLS

What's real in real-time operating systems?

Jeffrey Child, Associate Editor



Designers at Radiation Systems selected the QNX real-time operating system from Quantum Software Systems for an antenna controller system that controls a 7,500-ton, 100-m radio telescope. Using the QNX development environment, the software development team averaged between 2.5 and 3 lines of executable code per hour.

One of the most critical "build or buy" decisions facing real-time system designers is whether to purchase an off-the-shelf real-time operating system (OS) or make your own. If you opt for the first alternative, the current selection of off-the-shelf real-time kernels and OSs ranges from small, fast kernels to full-blown, Unix-like operating systems with a variety of graphics and networking support features. Because no one vendor supports all microprocessor targets and host platforms, you may need to use products from several different vendors to perform separate functions in the same real-time system.

Hoping to entice designers away from roll-your-own solutions, today's real-time software vendors generally offer more than just a kernel. Most provide complete OS packages including a real-time kernel, input/output executive, file management executive, language interface libraries, hardware interface support, debugger, network management support, and cross-platform compilers. These packages are usually sold for a development system price per number of users. Often the kernel can be purchased at quantity prices for embedding into the final design.

The reasons for choosing a real-time OS or kernel and buying off-the-shelf real-time software can be confusing. A study done last fall by consulting firm International Data Corporation (Framingham, MA) found that most real-time software vendors don't actively seek to specialize by application or industry, although many have a de facto focus. According to the study, key differentiators among vendors today are development tools, operating system response time (performance), and relationship to Unix.

One cause for confusion in the real-time OS market is the overuse of "context switch speed" as a way of comparing performance. But as Stuart Schlitt, vice-president of marketing at Integrated Systems, software components group division, (Santa Clara, CA), points out, context switching speed isn't a very good metric for judging performance. "Context switch speed doesn't have anything to do with the performance of the kernel," he says, "especially if it's a nested interrupt, and you're responding to the second interrupt."

Because customers ask for it, Integrated Systems does provide context switch figures for its pSOS+ kernel, part of the pSOS+ real-time integrated OS development environment. The company calculates the number using two other metrics it believes are more relevant to overall performance. One is the interrupt response time, which is defined as the greatest length of time that the kernel turns off interrupts. Using this metric pSOS+ yields a 6 μs response time on a 25-MHz 68020.

The other metric used is the time it takes a waiting task to begin to run. "We publish a series of numbers which document how long it takes to make a system call," says Schlitt. "[Using those numbers] you could figure out how long it takes to run under different situations." In a typical situation, a high-priority task may be blocked at a message queue, waiting for a message to come in. When an interrupt comes in, an interrupt handler sends a message to the queue where the task is waiting, causing it to preempt a low-priority task. What's measured is the time it takes to send the message, and also the time it takes for the task awaiting that message to receive it and ready itself to indicate that the task is running. That number is usually referred to as task latency time. "Out of those numbers we extract something called a context switch time, but only because people keep asking us for that," adds Schlitt.

Posix a plus

For a long time, both vendors and users of real-time OSs have seen a need for some kind of standard. The most successful attempt at this so far is the IEEE Posix standard. For designers familiar with Unix, compliance won't be a problem, because Posix is based on Unix. The other benefit of Posix is flexibility. It can ease the task of switching an R3000-to an R4000-based design, or from MIPS to Sparc, or to another vendor's Posix-compliant real-time OS.

As the chart shows, a significant percentage of real-time OS vendors have Posix 1003.1 and 1003.4 in their plans. Many are waiting to see the final draft before making any changes in their products.

PRODUCT FOCUS: REAL-TIME KERNELS AND OSs (32-bit)

Model name	Target processor	Platform support	Network support	Graphics support	Interrupt latency	Posix compliancy (IEEE)	I/O and file systems features	Kernel-only price (Qty 100)/ development environment price
Accelerated Technology PO Box 850245, Mobile, AL 36685 (205) 661-5770								**Circle 301**
NucleusRTX	68XXX, 80X86, MIPS, Sparclite, i960, 29000, and several DSPs	—	—	Metagraphics	0.6 µs, 25-MHz 29000	—	MS-DOS compatible	$3,500-$5,000/ $495 (for PC)
A.T. Barrett & Associates 11501 Chimney Rock, Suite R, Houston, TX 77035 (800) 525-4302								**Circle 302**
RTXC	680X0, 80386, 29000	PC	—	—	8 µs, 33-MHz 80386	No	Optional DOS-compatible file system	$2,995 (no royalty)/ Included
RTXC/MP	TMS320CX0, T8XX transputer	PC	—	Optional graphics server	6 µs, 25-MHz T800	No	—	$12,900 (no royalty) /Included
Byte-BOS Integrated Systems PO Box 3067, Del Mar, CA 92014 (800) 788-7288								**Circle 303**
Byte-BOS	68XXX, 80386, 80486	—	—	—	8 µs, 33-MHz 80386	—	Stream serial I/O libraries for "on chip" and external UARTS	$995 (no royalty)/ —
Diab Data 323 Vintage Park Dr, Foster City, CA 94404 (415) 571-1700								**Circle 304**
D-NIX	680XX, 88100	Eltec, Aydin, Diab systems	ARPA, OSI, NFS, SNA	X Windows, Motif	50 µs, 25-MHz 68030	1003.1	Unix file system	—/—
Digital Equipment Corporation 146 Main St, Maynard, MA 01754-2571 (508) 493-6717								**Circle 305**
DECelx	68020, 68030, Lockheed STAR, Omnibyte VR3000	DECstations, DECsystems	TCP/IP, NFS, UDP, telnet, FTP, RPC	—	6 µs, 25-MHz 68030	Selected 1003.1/ 1003.4 functions	I/O device drivers; RT11 and MS-DOS file system	$528/$2,563
VAXELN	VAX, rtVAX, MicroVAX	VAX/VMS	DECnet, TCP/IP	DECwindows, Motif	9-12 µs, rtVAX	Partial 1003.1 and 1003.4	Sequential, buffered, direct access	$502/$874
Emerge Systems 114 6th Ave, Indialantic, FL 32903 (407) 723-0444								**Circle 306**
RTUX	680X0, 683XX, 88XXX	HP, Motorola, Sun	TCP/IP, ARCnet, Bitbus	X Windows	10 µs	No	Unix-compatible; network accessible	$300-$500/—
Encore Computer 6901 West Sunrise Blvd, Fort Lauderdale, FL 33313 (800) 587-2900								**Circle 307**
µMPX, µARTE	88X00	Encore 91, 93	TCP/IP, NFS	X Windows	20 µs, 88x00	Yes	Buffered, sequential, direct	$2,500/$6,500
Enea Data AB Box 232, Nytorpsvagen 5 B, S-183 23 Taby, Sweden, +46 8 792 2500								**Circle 308**
OSE	680X0, 683XX, 80X86, Z180	Apollo, HP-9000, PC, Sun, VAX	TCP/IP, NFS, Internet and OSI protocols	—	—	Yes	Advanced I/O	$16,000/ $8,000-$16,000
Eurostart PO Box 7722, 2433 Frances Dr, Loveland, CO 80537 (303) 669-5068								**Circle 309**
Exeloc	80x86	PC/AT	—	—	20 µs	No	Drivers for digital/analog I/O, 16 serial lines; MS-DOS compatible	$10/$699 (25 licenses)
RTXDOS	80286, 80386, 80486	PC/AT	Novell	MS Windows	25 µs	No	Drivers for digital/analog I/O, 32 parallel lines; MS-DOS compatible	$125/$4,950 (25 licenses)

Model name	Target processor	Platform support	Network support	Graphics support	Interrupt latency	Posix compliancy (IEEE)	I/O and file systems features	Kernel-only price (Qty 100)/ development environment price
Eurostart PO Box 7722, 2433 Frances Dr, Loveland, CO 80537 (303) 669-5068								**Circle 309**
RTXDOS-Lite	80286, 80386, 80486	PC/AT	Novell	Mosy MMI	25 µs	No	Drivers for digital/analog I/O, 16 serial lines; MS-DOS compatible	$15/$1,499 (25 licenses)
MOSY-32	80386, 80486	PC/AT	Novell	Mosy MMI	20 µs	Planned	Drivers for digital/analog I/O, 32 serial lines; MS-DOS compatible	$145/$6,450 (25 licenses)
Eyring, Systems Software Division 145 W 820 N, Provo, UT 84601 (801) 375-2434								**Circle 310**
PDOS v4.1, VMEPROM v4.1	68000 family	SunOS, VMS, MS-DOS, Unix, target	TCP/IP, Sockets, Link Level, UDP	GKS	3 µs	Yes	Posix-compatible file system, contiguous files	$55/—
Forth 11 N Sepulveda Blvd, Manhattan Beach, CA 90266 (310) 372-8493								**Circle 311**
cF32-68332/ µSD	68332	PC	—	—	—	—	Serial, parallel	—/$3,950
pF32-386/ µSD	80386, 80486	PC	—	—	—	—	Standard PC I/O	$1,495/—
General Software PO Box 2571, Redmond, WA 98073 (206) 391-4285								**Circle 312**
Embedded DOS	80X86	PC/XT/AT	Netware 286/ Netware 386	DOS graphics libraries	—	—	All DOS file I/O (fully re-entrant)	$600/$495 (unlimited users)
Booter Toolkit	80X86	PC/XT/AT	—	—	—	—	Sequential, random	—/$149
Industrial Programming 100 Jericho Quadrangle, Jericho, NY 11753 (516) 938-6600								**Circle 313**
MTOS-UX	680X0, 88X00, 80X86, i860	Sun, HP, PC, DG, Motorola	TCP/IP	No	3 µs, 20-MHz 88100	Planned	Multi-buffered, sequential MS-DOS compatible file system	$5,000/$200
Integrated Systems, Software Components Group 3260 Jay St, Santa Clara, CA 95054 (408) 980-1500								**Circle 314**
pSOS+	680X0, 68EC0X0, 683XX, i960, 80X86, 88100, 88110	PC, Sun 3, Sparc, HP, VAX/VMS, DECstation, IBM RS6000	TCP/IP, UDP, IP, tftp, NFS	X Windows	6 µs, 25-MHz 68020 8 µs, 16.7-MHz 80386	1003.14	User defined I/O; choice of MS-DOS or Unix file structure	—/—
Intel 5200 NE Elam Young Pkwy, Hillsboro, OR 97124 (800) 438-4769								**Circle 315**
iRMX for Windows	80386, 80486	PC	iNA ISO transport, MSnet	MS Windows	4 µs, 50-MHz 80486	Partial 1003.1	Adjustable buffering w/overlapped I/O, disk caching & mirroring	$150 (qty 1)/ $5,595
iRMX III	80386, 80486	PC	iNA ISO transport, MSnet	Via 279 RGI	4 µs, 50-MHz 80486	Partial 1003.1	Same as above	$180 (qty 1)/ $5,650
iRMK	80386, 80486	PC	—	—	4 µs, 50-MHz 80486	Partial 1003.1	Posix I/O via companion Unix processor	$1,500/ $1,500 per user
JMI Software Consultants 904 Sheble Ln, PO Box 481, Spring House, PA 19477 (215) 628-0840								**Circle 316**
C Executive	i960, i860, 80X86 family, 29000 and 68000 family, MIPS, Sparc, and others	DOS, Sun, VMS, Unix	—	—	7 µs, 33-MHz i960CA, 19 µs, 20-MHz 68030	Partial	Unix-style I/O; DOS system with buffered, random, and sequential I/O	$70/$2,500 (unlimited users)

PRODUCT FOCUS: REAL-TIME KERNELS AND OSs (32-bit)

Model name	Target processor	Platform support	Network support	Graphics support	Interrupt latency	Posix compliancy (IEEE)	I/O and file systems features	Kernel-only price (Qty 100)/ development enviroment price
Kadak Products, Ltd. 1847 W Broadway Ave, Vancouver, BC V6J 1Y5 (604) 734-2796								**Circle 317**
AMX386	80386, 80486	PC	No	No	22 µs, 20-MHz 80386	No	No	$4,000/Included
AMX68000	680X0, 683XX	PC	No	No	29 µs, 12.5-MHz 68020	No	—	$3,000/Included
Lynx Real-Time Systems 16780 Lark Ave, Los Gatos, CA 95030 (408) 354-7770								**Circle 318**
LynxOS	80X86, 680X0, i860, 88100, PA-RISC, 29000, Sparc 2, R3000, R6000	386 PC, OS/2, MVME147/167, Sun, DG, Okistation, Intel 860 station	TCP/IP, NFS	X Windows, Motif	10 µs, 33-MHz 80386	1003.1, 1003.4 (draft 9), 1003.4a (draft 4)	File system funtionally identical to Unix plus contiguous files	$290-$490/ $1,495
Micro Digital 6402 Tulagi St, Cypress, CA 90630 (800) 366-2491								**Circle 319**
SMX	80X86	PC	Any DOS package	Any DOS package	15 µs, 10-MHz 80188	No	Runs with DOS	$1,995 (no royalty)/ Included
Microware Systems 1900 NW 114th St, Des Moines, IA 50325 (515) 224-1929								**Circle 320**
OS-9	680X0, 683XX	Sun 3, Sparcstation, HP9000, SGI, DOS, Delta, VAX	TCP/IP, NFS	X Windows, Rave	18 µs, 33-MHz 68030	—	Unified, modular I/O system with pipe, sequential, disk, tape, X, etc.	$51/$1,250 per system
OS-9000	80X86, 680X0	OS-9000, Sparcstation, HP9000, SG Iris, DOS, Delta	TCP/IP, NFS	X Windows, Rave	18 µs, 25-MHz 80386	—	Same as above	$135/$995 per system
Modular Computer Systems 1650 W McNab Rd, Ft Lauderdale, FL 33309 (305) 974-1380								**Circle 321**
REAL/IX	68030	REAL/STAR	TCP/IP, X.25	X Windows, Motif	5-105 µs	—	Preallocated files, asynchronous and direct I/O, standard Unix	$1,595/$6,000 (unlimited users)
REAL/IX	88100, 88110	REAL/STAR	TCP/IP, NFS, FDDI, X.25	X Windows, Motif	20-160 µs	1003.1 now, (.2 and .4 planned)	Same as above	$1,595/$6,000
Motorola, Computer Group 2900 South Diablo Way, Tempe, AZ 85282 (602) 438-3244								**Circle 322**
VMEexec	680X0, 88100	Delta	TCP/IP	Delta Windows, X-Lib	10 µs	1003.13, 1003.4 planned	Real-time file system with contiguous files; Unix file system access	$125/$7,500
Novell, Desktop Systems Group 70 Garden Ct, Monterey, CA 93940 (408) 649-3896								**Circle 323**
FlexOS	80386	PC	TCP/IP, NetBIOS	Multitasking graphics environment	18 µs, 25-MHz 80386	1003.1	Device-independent Unix model for device, pipe, and disk I/O	—/$3,995
Objective Systems C.P. 265, Ville Mont-Royal, P. Quebec H3P 3C5 (514) 344-1674								**Circle 324**
Interactors C++	80X86	PC	SL/IP,UDP	No	4 µs, 33-MHz 80486	No	Timer, RS-232, mouse and DOS files	$495 (no royalty)/ $4,990

Model name	Target processor	Platform support	Network support	Graphics support	Interrrupt latency	Posix compliancy (IEEE)	I/O and file systems features	Kernel-only price (Qty 100)/ development environment price
Precise Software Technologies 301 Moodie Dr, Suite 308, Nepean, Ontario K2A 3Z5 (613) 596-2251								**Circle 325**
Precise/MPX	680X0, 68302, 80X86, TMS320C30	Sun, PC (386+)	SDLC, LAPB, Milstd 1553, TCP/IP	No	20 µs, 68020	1003.4	Posix-compatible serial I/O, host I/O compatible	—/$4,000
Quantum Software Systems 175 Terrence Matthews Crescent, Kanata, Ontario K2M 1W8 (613) 591-0931								**Circle 326**
QNX 4.1	80486, 80386, 80286, 8088	PC, EISA, MCA, Ampro, Gespac, STD-Bus, VMEbus	Ethernet, Arcnet, TCP/IP, X.25, TCNS	Open Look	6 µs, 33-MHz 80486	1003.1, 1003.2 utilities and shell, 1003.4 real-time extentions	Fault-tolerant load balancing on multiple network links	$168/$795
Ready Systems 470 Potrero Ave, Sunnyvale, CA 95062 (800) 228-1249								**Circle 327**
VRTX Velocity 68k	680X0	Sun 3, Sparc, HP9000, DEC Ultrix	TCP/IP, NFS, RPC, XDR, TFTP	X Windows, Motif	10 µs, 25-MHz 68020	Planned	Synchronous/asynchronous I/O, buffered, sequential	$4,070/$655
VRTX Velocity DOS386	80386	PC (386/486)	TCP/IP	WIX-GUI	20 µs, 16-MHz 80386	—	Same as above	$655/$17,000-$25,000 (base)
RTMX-UniFLEX 800 Eastowne Dr, Suite 111, Chapel Hill, NC 27514 (919) 493-1451								**Circle 328**
UniFLEX	680X0	Self-hosted	TCP/IP, NFS	XV11R5, PEX	6 µs, 25-MHz 68040	1003.1	Buffered, sequential, contiguous	$500/$5,600 (unlimited users)
RTMX	680X0, 80X86, MIPS, Sparc	Self-hosted	TCP/IP, NFS, ISO	XV11R5, PEX	10 µs, 25-MHz 68040	1003.1, 1003.2, 1003.4	Buffered, sequential, contiguous	$200/$995 (users)
Spectron Microsystems 5266 Hollister Ave, Santa Barbara, CA 93111 (805) 967-0503								**Circle 329**
Spox	TMS320CX0, DSP96002, MC56000, ADSP-21020, ADSP-2100	PC, Sun	—	—	1 µs	—	ANSI C I/O interface, proprietary DSP stream, I/O interface	—/$12,000
Wind River Systems 1010 Atlantic Ave, Alameda, CA 94501 (510) 748-4100								**Circle 330**
VxWorks 5.0	680X0, 683XX, Sparc, MIPS, i960	Sparc, IBM RS/6000, DECstation, SG Iris, HP 9000	TCP/IP, NFS, RPC, XDR, rlogin, telnet, Sockets	X-11, Athena Widgets, Motif	8 µs, 25-MHz 68020	—	Fully Posix compliant I/O	$200/$22,500 (10)

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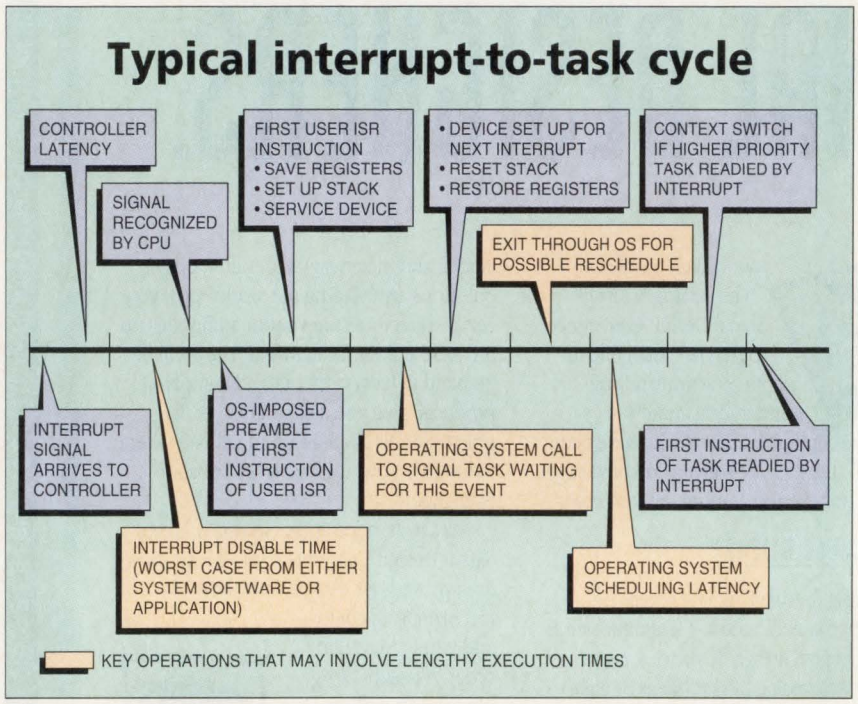
SOFTWARE & DEVELOPMENT TOOLS



Although context switch speed is often used to judge a kernel's performance, there are more metrics to use. As the diagram shows, context switch time is only a small fraction of the total interrupt-to-task-implementation cycle. Other parts of the cycle (shaded) have much more effect on performance.

According to Inder Singh, president and CEO of Lynx Real-Time Systems (Los Gatos, CA), the Posix committee is getting close to finalizing the standard. "1003.1 is already approved. There's a very good chance that 1003.4 will be approved this year, possibly by September."

While many real-time OSs already contain some elements that require Posix compliance, Lynx has probably put more emphasis on Posix than most. In Lynx's product, Lynx/OS, there are Posix system calls in the kernel. According to Singh, this will give Lynx/OS a performance advantage over other real-

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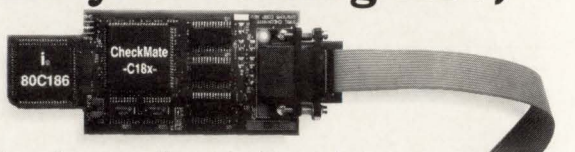

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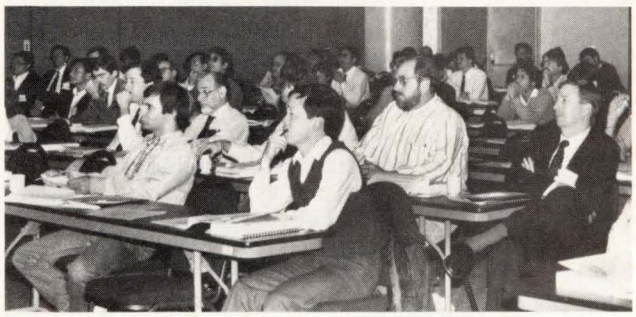

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CIRCLE NO. 61

SOFTWARE & DEVELOPMENT TOOLS

time OSs which were not designed to be Unix-like. "When other vendors provide Posix, it's probably going to just be part of their libraries, and the performance isn't going to be as fast," Singh predicts.

For its part, RTMX-UniFlex (Chapel Hill, NC) offers a real-time version of Unix designed to let development be done directly on the target, rather than using cross-development with a host system. Derived from public releases of BSD Unix, the new system includes RTMX/RN, containing networking and real-time functions, and RTMX/XW, containing MIT X11R5+ Motif. Key features of the system are fixed-priority real-time tasking, contiguous file support, Network File System (NFS) support, and shared memory.

If you need it all

Although Posix-compliant real-time OSs look like Unix, they're not full Unix versions. Designers that need both real-time capabilities and full Unix may want to consider Venix, a real-time embedded OS from VenturCom (Cambridge, MA). Not a Unix look-alike, Venix is actually Unix System V with real-time enhancements. The Venix kernel can boot and run without an operator, and can be embedded into ROM.

In its first use of a commercial real-time OS, Rockwell International chose Venix for its Boeing 777 systems. Venix controls several systems, including separate display/computers for the pilot, copilot and flight attendants. All of these systems support X Windows and are networked to a common database through Open Systems Interconnection over an FDDI (Fiber Distributed Data Interface) fiberoptic cable.

One trade-off with most of the highly functional, Unix-like real-time systems stems from their size. While this isn't an issue for large systems where the software is stored on disks or distributed across several boards, size can be a serious constraint in high-volume, deeply embedded applications such as fax machines and laser printers.

With this is mind, VxWorks from Wind River Systems (Alameda, CA) offers a scalable system. The full development system includes the target tools, file system and high- and low-level networking services. At the bottom are the tools and the kernel. The latter includes a small set of components surrounding the kernel that are actually used in the application, such as message queues, semaphores and schedulers. "Depending on your application, you may require a networked operating system and a file system," says Tony Barbagallo, manager for product marketing at Wind River Systems. "For data acquisition and control, for example, you may want to have the local disk run VxWorks. You could have your disk connected to one board, but get your data across the network from another VxWorks. But once you're in

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CIRCLE NO. 62

that final application, you probably don't need your development tools. VxWorks lets you take those pieces away as needed."

Ready Systems, a company that focuses specifically on hard real-time applications and deeply embedded applications, plans to release Version 2.4 of its VRTX-Velocity environment soon. The product is currently shipping in beta form on the HP/9000 425 system, while updates for the Sun 3 and 4 workstations supporting X Windows and Motif will be available early this month.

The new release includes an enhanced run-time kernel, along with the latest releases of Microtec Research and Oasys compiler tools. Full, integrated support for the 68040 and 68332 is also provided, along with major enhancements to the networking component, file management system and multiprocessing part of VRTX.

According to Ready Systems' (Sunnyvale, CA) Jim Ready, adding support for the 68040 required careful attention because of the chip's data cache. On the 68040, the memory management unit (MMU) must be used in conjunction with the data cache, or else errors can occur. The new VRTX release supports the MMU and lets pages be set individually. "There's a problem of consistency between the cache and the main memory, and if you don't do something special, things may run for a long time, but it can eventually crash," says Ready.

For the cost-conscious

When designing an antenna controller system for a 7,500-ton, 100-m radio telescope, David Lamb, senior software engineer at the Precision Controls Division of Radiation Systems (Richardson, TX), chose to use the QNX operating system from Quantum Software System. "The main reason we chose QNX 2.0 was because it could do everything we needed it to do at the best price," says Lamb. "And since we were using the PC bus, there were some others that were not really appropriate."

Another aspect of QNX that Lamb found impressive was its development environment. "[Using QNX] our team is averaging between 2.5 and 3 lines of code per hour, executable," says Lamb. "This includes the initial time of deciding how to proceed all the way through test." On the down side, Lamb points out that because QNX runs on the PC, the company couldn't tie CASE tools to the same platform it's using for development. "When CASE tools don't tie directly into your development, they aren't used well enough—CASE tools become front-end-only tools, rather than complete-lifecycle tools." This is perhaps an area were the Unix-like real-time OSs offer an advantage, since most of today's sophisticated CASE tools run under Unix. ■

CIRCLE NO. 60

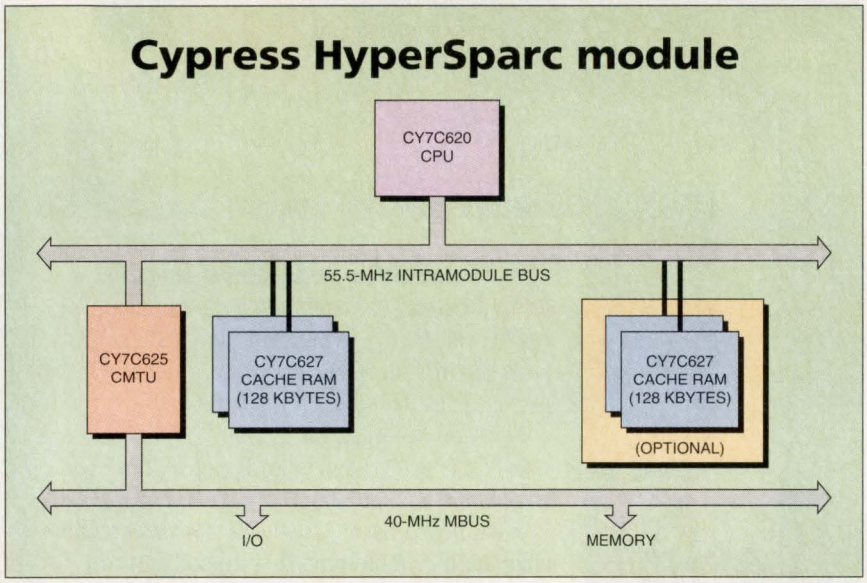
INTEGRATED CIRCUITS

Next-generation Sparc—can less be more?

HyperSparc, the second generation of Sparc processors from Cypress Semiconductor (San Jose, CA), can be thought of as a small hop, rather than a giant leap, down the road toward VLSI integration. In effect, three new devices comprise the chip set's cast of characters. The CPU itself boasts less than 1.1 million transistors.

Does it matter? Apparently not. "Our aim is to make small chips perform like big chips," reports Roger Ross, president and CEO of Ross Technology, the Cypress subsidiary responsible for HyperSparc.

The CY7C620 is an integrated CPU with an on-chip integer and floating-point unit. Second in command is the triple-duty CY7C625 cache controller/MMU/tag unit (CMTU); bringing up the rear is the CY7C627 cache data unit (CDU) with on-chip write buffers. Together, the devices form the heart of several different modules that Cypress offers at a variety of different price/performance points.



Here comes 64 bits! The Cypress CY7C620 processor communicates with the CY7C627 cache RAMs and CY7C625 CMTU over a 3.3-V, 55.5-MHz intramodule bus with a data width of 64 bits.

CPU is superscalar pipeline

The CY7C620 processor is a multiprocessing, superscalar, six-stage pipeline device with a CPU datapath that handles all integer instructions, plus load and store instructions. It provides eight overlapping register windows and eight global registers. A core instruction scheduler decodes, groups, schedules, and dispatches instructions.

It can launch two instructions per clock cycle to any of four logic blocks: load/store, branch/call, integer, and floating-point units. It also identifies and controls interrupts. The core instruction fetch unit selects the next instruction, maintains the program counter and executes branches and calls. Hardware interlocks handle conflicts that result from resource dependencies, relieving compilers of the burden.

The CY7C625, in addition to boasting all the same features as Cypress' earlier CY7C605 multiprocessing cache controller/MMU, adds a clock synchronizer that makes the module's dual clock scheme run efficiently. Special multiprocessing features include a tag memory that's physically tagged and virtually indexed for snooping, write-through or copy-back protocols, and direct data intervention with memory reflection.

Each CY7C627 synchronous CDU incorporates on-chip address data latches, an on-chip pipelined write buffer and separate input/output power supplies.

While other manufacturers such as Digital Equipment Corporation (Hudson, MA) have already moved to true 64-bit CPUs as well as 3.3-V operation, this generation of devices from Cypress didn't make it that far. The CPU is very much a traditional 32-bit device, and it works from a traditional 5-V supply to boot.

This isn't to say that Cypress ignores the advantages of 64 bits. The intramodule bus connecting the processor, CMTU and CDU, for example, does operate from a 3.3-V level to minimize noise at high clock rates. And the chips do communicate over this bus, which sports a 64-bit datapath as well as 32-bit addressing. Nevertheless, the instructions and addresses are all 32 bits.

To make life easier for designers, Cypress will make the devices available in modules, so you won't have to trouble yourself with the nuances of 40-MHz design rules. The first HyperSparc modules in the Sparccore family are the uniprocessor CYM6221K M bus module with 128 kbytes of cache, the dual-processor CYM6222K M bus module with 128 kbytes of cache per processor, and the dual-processor CYM6226K M bus module with 256 kbytes of cache per processor.

All three Sparccore modules operate with 55.5-MHz internal clocks and will be in full production in the fourth quarter. Samples of modules with clock rates up to 80 MHz will be available later. For the CYM6221K single-processor module, the price is $3500 in quantities of 100. *— Dave Wilson*

HyperSparc at a glance

- High-speed intramodule bus
- CPU with on-chip IU/FPU
- 62 specmarks
- Preconfigured modules

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CIRCLE NO. 65

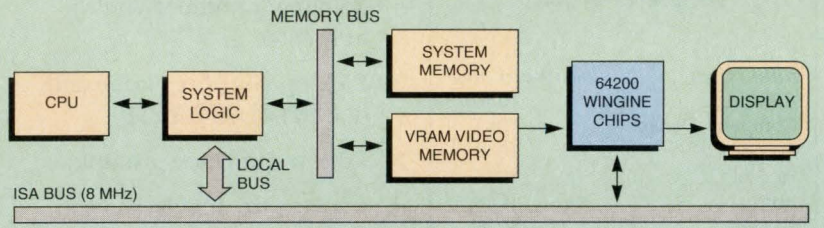
INTEGRATED CIRCUITS

Simpler is faster for new Windows chip

A new accelerator chip enhances performance of the Microsoft Windows graphical user interface by leaving most of the work to the CPU. Called the 64200 "Wingine" by Chips and Technologies (San Jose, CA), the chip eliminates bottlenecks in graphics performance caused by single-port DRAMs and the PC's ISA system bus. It also avoids complex electrical interfacing and timing problems associated with connecting graphics accelerators to the CPU's local bus. The result is that any upgrade in CPU performance, whether it's an improvement in clock speed or an upgrade to a faster class of CPU, has an immediate effect on Windows performance.

The Wingine lets the CPU access display memory, which uses a dual-port video RAM as part of its system memory. The CPU simply writes the graphical data into video memory via the video RAM's parallel port. The Wingine shifts the pixel data out via the VRAM's serial port and sends it directly to the display. Graphic data flows in a single direction and avoids both the system bus and the local bus.

Wingine memory bus architecture



The 64200 Wingine's memory bus architecture lets the CPU address VRAM video memory as system memory. The CPU is able to do all the graphic computational work and write to VRAM. The Wingine processes the pixel data out of VRAM to the display, all without involving either the CPU's local bus or the system bus.

Going against convention

For a number of years, the conventional wisdom in graphics acceleration has been to unburden the CPU from the details of graphics processing by using a chip that could process high-level commands sent by the host processor into pixels to be displayed on the screen. The two main bottlenecks were the load on the CPU caused by doing low-level graphics computation and the bandwidth of the system bus, which had to transport all the pixel data.

In PC systems, the system bus—typically the AT or ISA bus, with its 8-MHz bandwidth—remains an obstacle to higher performance. Another is the path that graphics data has to take—commands go from the CPU via the system logic over the ISA bus to the VGA controller. The VGA controller processes the commands and puts pixel data into DRAM video memory. Then it removes pixel data from DRAM and sends it to the display.

One common method of increasing VGA performance for Windows has been to add a bitblt (bit boundary block transfer) engine to the VGA controller. But this still means reading data out of DRAM memory and writing it back in at a new location. Another approach has been to interface the VGA controller directly to the CPU's local bus. This avoids the system bus bottleneck, but it entails complex electrical and timing issues, making system design more difficult, and there are as yet no standards for a local bus interface.

It's the blinding speed of today's CPUs that's allowed rethinking of the graphics coprocessor approach—at least for Windows in PCs. It appears now that it's faster to let the CPU handle the 2-D drawing, bitblt, rectangle fill, and other operations common to Windows, while taking advantage of the speed of the CPU's memory bus and of dual-port VRAMs. As a result, graphics throughput is directly scalable as a function of processor speed.

Compatibility preserved

The 64200 Wingine maintains VGA compatibility, so that a system in which it's used can run DOS-based, non-Windows VGA applications unaltered. The Wingine contains Super VGA logic, and, when it first powers up, it's in SVGA mode. Chips and Technologies has developed a switch that works in conjunction with its PEAK/DM family of 386 and 486 system logic products to detect whether or not Windows is running. When this so-called "Winglue" 64201 chip detects that the system is in DOS mode, it switches data going over the system bus to the Wingine running in SVGA mode. When Windows is running, the Wingine takes over.

Production quantities of both the 64200 and the 64201 are scheduled to be available in June. In large volumes the price of the 64200 will be $18.00, and the 64201 will be $7.00. —*Tom Williams*

64200 Wingine at a glance

- 32-bit data path directly from host CPU to VRAM display memory
- In Windows mode, accesses video memory as system memory
- Data transfer rates of 20-40 Mbits/s
- Uses standard 256k × 4 VRAMs, up to 2 Mbytes
- Supports resolutions of 640 × 480, 800 × 600, 1024 × 768, and 1280 × 1024
- Refresh rates up to 72 Hz

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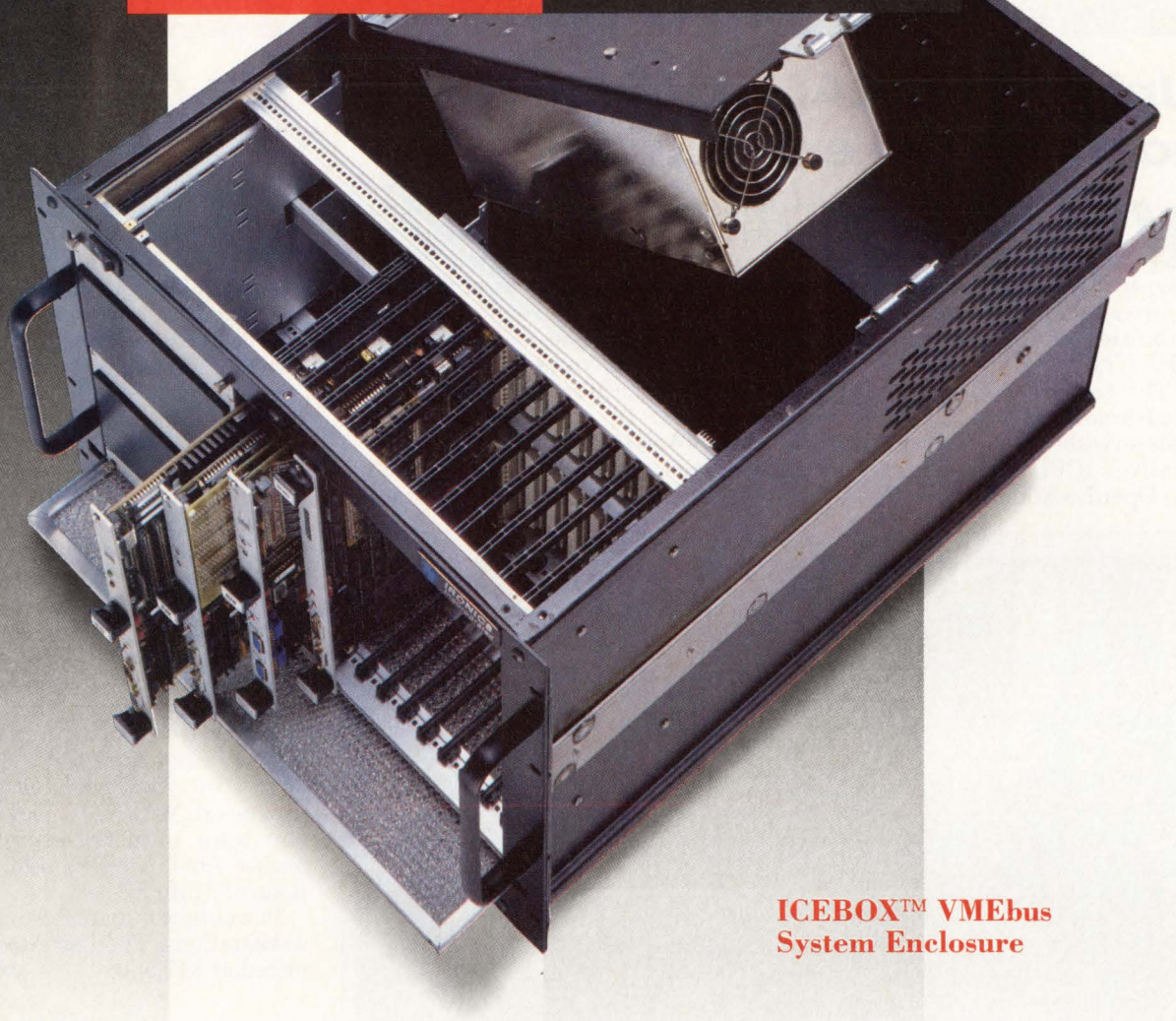

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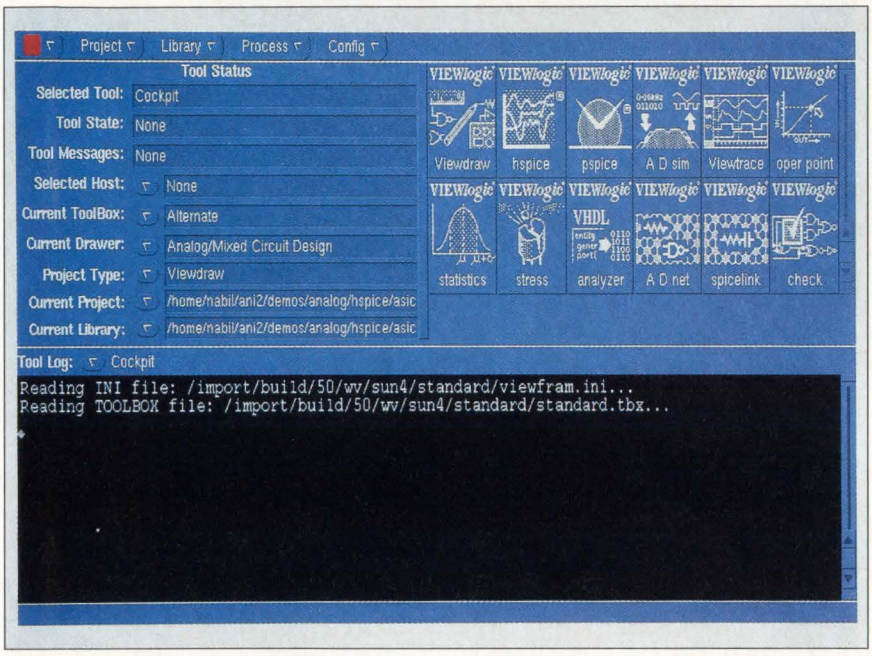
CIRCLE NO. 66

CAE/CAD TOOLS

Unix-based CAE suite adapts to multitool environments

Viewlogic Systems (Marlborough, MA) has revamped its suite of EDA tools by optimizing them for Unix-based workstations, adding new simulation capabilities and offering a graphical VHDL entry format.

The software, dubbed Powerview, is a framework-based suite that's consistent with the CAD Framework Initiative's (CFI) 1.0 standards, as well as OpenLook/Motif and EDIF 2.0.



Viewlogic's Powerview cockpit provides a customizable environment through which all tools can be launched. Here, the palette of available tools is displayed in the top window. The bottom window displays a log which tracks the tools currently in use.

The new software is also compatible with Viewlogic's DOS-based toolset, Workview, which means that data can be shared between the two environments over a network of personal computers and workstations.

By basing Powerview on CFI's standard, Viewlogic has implemented methods for tool encapsulation, intertool communication and design representation. To Powerview, a tool is simply an executable program, regardless of its function. An encapsulated tool is surrounded by a shell that maps the syntax required to invoke the tool into graphics and icons—the invocation syntax becomes an icon. This lets you assimilate tools into the framework without modifying any source code, either the tool's or Powerview's—for example, each tool definition carries its own file. The framework interprets and invokes the file with the tool's own command line syntax.

Viewscript customizes GUIs

Viewlogic has also developed an extension language called Viewscript which lets you adapt Powerview to individual environments and interactively access the application programming interface of framework tools. With this capability, you can customize the graphical user interface (GUI) as desired and incorporate in-house and third-party tools. All tools are managed through a front-end "cockpit" which lets you manage portions of designs and the tools associated with them.

The new simulator in Powerview, Viewsim/XL, provides incremental netlisting and save-and-restore features. With incremental netlisting, you don't have to recompile entire designs whenever you make changes. With save-and-restore, you can pause during the design of a large ASIC and save the state of the simulator at any point in time and restart later exactly from that point.

To help overcome the complexity and tedium associated with writing high-level circuit specifications, Viewlogic offers two aids—Envision VHDL and a graphical source-level VHDL debugger. Envision VHDL, a front-end tool that Viewlogic has licensed from i-Logix (Burlington, MA), lets you represent designs graphically via state-transition and data-flow diagrams. It then automatically produces VHDL code which is compatible with Viewlogic's simulator and the synthesis tools from Synopsys (Mountain View, CA). With the VHDL source-level debugger, you can interactively step through VHDL source code and correct it as it executes.

Powerview also features ViewPLD, a synthesis capability developed jointly by Viewlogic and Data I/O (Redmond, WA). With ViewPLD, you can map industry-standard formats—Abel, CUPL, JEDEC, and Palasm—into FPGAs.

Powerview is available now on Sun workstations. The basic tool suite is priced at $17,500. —*Mike Donlin*

Powerview at a glance

- Conforms to CFI 1.0, OpenLook/Motif and EDIF 2.0
- Adapts to in-house and third-party tools by encapsulating them as executable programs
- Features the Viewsim/XL simulator which provides incremental netlisting and save-and-restore capabilities
- Envision VHDL lets you represent designs graphically and generates VHDL code automatically
- ViewPLD software provides migration path for programmable logic into other technologies such as ASICs and gate arrays

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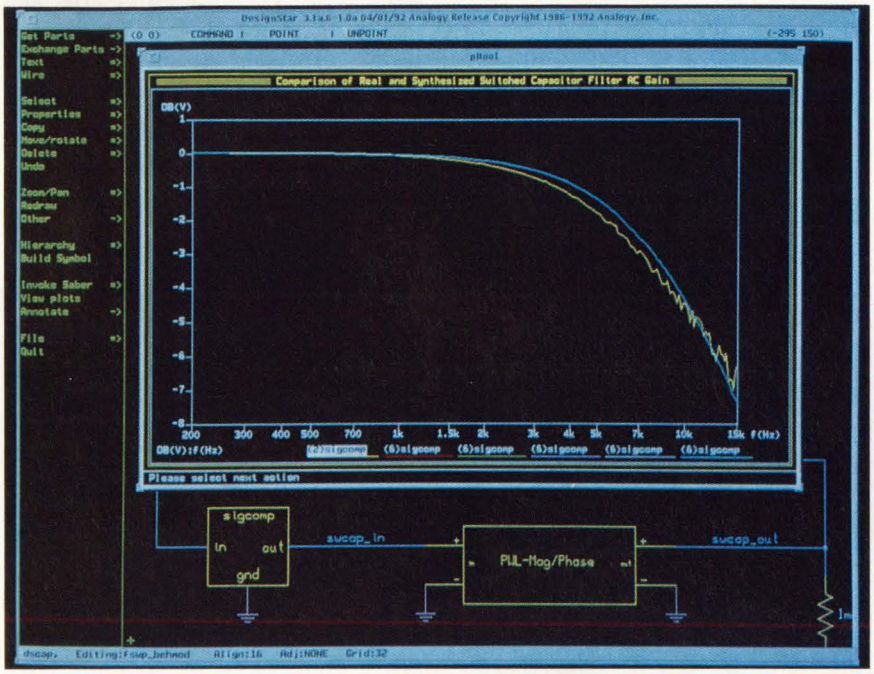
CAE/CAD TOOLS

Software generates analog behavioral models



In this comparison of the frequency response of a switched capacitor filter, the waveform for Analogy's synthesized behavioral model (blue trace) closely correlates with the actual device output (yellow trace) over the entire operating frequency.

Critics of Analogy's (Beaverton, OR) Saber simulator and Mast analog hardware description language have cited difficulty of use as a stumbling block to their widespread acceptance. With the announcement of Analog Model Synthesis for Saber, Analogy has taken a step toward silencing these complaints. The tool uses graphical data from previous simulations or from laboratory measurements and automatically transforms them into behavioral models, a capability that Analogy says eliminates the need for equations or modeling code.

Automation speeds things up

To create a behavioral model, you specify the waveform that you want to use for model generation captured from previous simulation or from lab instruments. Then, by activating the Saber simulator, the model is automatically loaded.

Key data is automatically extracted from the waveform and used to create the behavioral model. For example, in a frequency-domain simulation, the appropriate poles and zeroes are extracted and placed in the proper frequency positions. Mast code is generated from this data and the model is created.

According to Analogy, model synthesis also reduces simulation time because behavioral models run faster than equivalent circuit-level models. Analogy uses a behavioral model for a switched capacitor filter (SCF) to back up this claim. Because of the high-frequency switching inherent in this type of filter, primitive-level simulations can take hours. A behavioral model, on the other hand, will simulate in seconds with accurate results. To synthesize the behavioral model, the frequency range of a primitive-level simulation of the SCF is swept using a preexisting instrument template created in Mast. The resulting frequency response is then loaded directly into the synthesized model for specific applications, an approach that ensures accuracy on a behavioral level.

Data from lab instruments can also generate waveform input. For ICs that will be inserted into a printed circuit board, for example, you can make measurements of the target circuit board and input this data as stimulus during the simulation of the IC. The data can also be fed back from simulation to the measurement equipment, which lets you test the board with the simulated IC data.

In addition to model synthesis, Analogy has also created a technique for analog stimulus generation. Like analog model synthesis, stimulus generation has its origins in waveforms which can be transformed into stimuli for circuit simulation in either the time or frequency domain. For example, if you want to simulate a sensor and a signal-conditioning circuit followed by a Z-domain filter, the resulting waveform can be used as the input stimulus for the filter. Alternatives to stimulus generation, such as simulating the entire circuit each time an individual stage needs to be analyzed or manually entering stimulus data for each stage, can increase overall simulation time.

The Analog Model Synthesis software will be available in July as part of Analogy's DesignStar environment. Prices begin at $2,000.

— Mike Donlin

Analog Model Synthesis at a glance

- Uses graphical data from previous simulations or from laboratory measurements to create behavioral models
- Eliminates the need to use equations or modeling code to create behavioral models
- Creates analog stimulus data in either the time or frequency domain
- Available in July with prices starting at $2,000

Analogy
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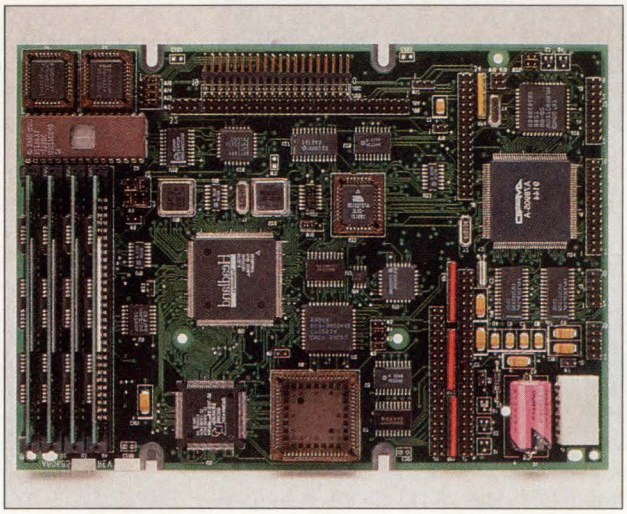
COMPUTERS & SUBSYSTEMS

Mini motherboard helps PC/104 expansion

Dubbed Little Board/386SX by its developers at Ampro Computers (Sunnyvale, CA), a compact, low-power 80386SX-based PC/AT puts all the power of a full-sized industrial PC on a 5.75 × 8 in. board. In addition to on-board features, the board can accept standard PC/104 modules for a variety of add-on options, such as EGA or VGA graphics, specialized communications and other functions. Scores of such modules are offered for the platform by Ampro and more than 20 other companies that have adopted the PC/104 proposed standard.



Ampro Computer's Little Board/386SX is a high-performance, low-power (below 5 W) industrialized 80386SX motherboard in a compact form factor (5.75 in. × 8 in.). Consistent with its small form factor, expansion capabilities, when required, use PC/104 accessory modules.

In addition to a 25-MHz 386 processor, the Little Board accepts up to 16 Mbytes of on-board DRAM, and has dual serial and parallel controllers, a floppy drive controller, an IDE hard disk drive interface, and a SCSI port.

Enhanced BIOS

Consistent with its targeted applications in embedded systems, Ampro's product includes a set of enhanced BIOS services. These include a bootable "solid-state disk" to make the board particularly attractive for embedded applications where rotating media may cause mechanical or reliability problems. In addition, the BIOS is tailored to support a wide variety of SCSI drives, and has a unique SCSI/BIOS function to simplify development of custom SCSI applications. The BIOS also supports the board's watchdog timer, allowing for initialization and providing BIOS functions for application software.

The specially modified BIOS also supports other functions critical to embedded applications. These include the ability to download executable code from a remote device prior to system boot, an EEPROM access function that allows high-level access to the nonvolatile OEM data area in the configuration memory, and OEM hooks which let the system execute custom code prior to system boot, allowing for system customization without modification.

"What we offer," says David Feldman, Ampro president, "is a complete platform for a high-performance AT-based computer on a compact board. With the Little Board, as well as our other compact PC-compatible embeddable computers, [it] isn't just an alternative to 'build your own.' We're offering that all-important time-to-market advantage inherent in complete, tested and reliable subsystems. And because it's based on the industry-standard DOS operating system, software development is simplified—and often available commercially for many applications."

Designed for embedding

The Little Board, as Feldman explains, is designed specifically to be embedded into another system. That's why, for example, a graphics interface isn't included. Unlike other features, such as the serial and parallel ports, graphics interfaces can be more costly and are often specialized for specific display types such as LCDs or other flat-panel industrial displays.

The Little Board uses CMOS circuitry that makes it extremely stingy in the power consumption department. This lets the board be used in small and confined areas, because it dissipates only 5-W—less than a single Christmas tree lightbulb—and doesn't require additional forced-air cooling.

Yet, even with all these features, Little Board/386SX sells for only $720 each in quantities of 100 and is available now.

With a broad customer base, Ampro continues to support its products despite rapid changes and evolution in the PC market. This support includes maintaining end-of-life inventories of critical PC chip sets, providing full documentation for any product or subsystem upgrades and maintaining compatibility with previous generations of products.

— Warren Andrews

Little Board/386SX at a glance

- PC/AT-compatible single-board system
- AT motherboard features
- 25-MHz 80386 CPU
- Up to 16 Mbytes of DRAM
- Dual serial and parallel controllers
- Floppy drive and IDE hard disk controllers
- SCSI interface
- Bootable solid-state disk
- Watchdog timer
- PC/104 module expandable
- 5-W operation

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CIRCLE NO. 67

COMPUTERS & SUBSYSTEMS

Data acquisition marries DSP on single board

A new series of data acquisition boards now offers combined test, measurement and processing in a PC/AT format. The boards include precision analog and digital I/O subsystems combined with a Texas Instruments 320C40 digital signal processing (DSP) chip. The family of three boards, each providing different sampling rates and resolutions, comes from Data Translation (Marlborough, MA).

Designed as a total test solution, the boards include analog waveform digitizer and synthesizer subsystems for analog signal input and output, dynamic digital input and output subsystems and host communications over the ISA bus.

"It takes all the I/O capabilities of the 320C40 to handle the communications," according to Mitch Reifel, marketing manager for DSP products at Texas Instruments (Houston, TX). "Every C40 data I/O facility, all six communications ports plus the six-channel DMA engine are needed to service the board's high-throughput analog and digital I/O subsystems, while leaving the processing power to squeeze an entire test and measurement system onto a single PC/AT board."

No host interaction

Clever application of the 320C40 lets it manage all data capture, control, transfer, and calculation without any host interaction. Communication with the host operating system uses the 320C40's high-level message passing. Data can be preprocessed in the 320C40, or sent directly to the host using the DMA. All communication between the board and the host is performed transparently by device drivers.

Data movement is performed as I/O through the 320C40 communication ports and under control of its multichannel DMA. Data movement is concurrent with data processing. Contention for memory access is minimized, letting the 320C40 CPU spend a larger percentage of its time on processing—and less on overhead.

The six DMA channels access two separate memory spaces via two independent buses. Each data interface subsystem uses a 320C40 communication port and DMA channel to send data to and from memory. This provides high-speed data transfer and minimizes bus contention.

The four separate subsystems—waveform digitizer, waveform synthesizer and dynamic digital input and output—provide the capability to address complex test and measurement needs. The waveform digitizer lets an analog waveform be captured and stored anywhere in the 320C40 memory space. Each 12- or 16-bit sample, depending on the board model, can be automatically sign-extended to 32 bits for direct processing by the 320C40 as two's complement integer data. Alternately, data packing is supported for memory conservation in non-real-time applications.

The Data Translation DT3801 series of boards also offers a flexible triggering scheme. The subsystems can use any of four independent software and two external polarity-selectable digital triggers. Triggers may start transfer with any combination of subsystems simultaneously. For samples to be stored both before and after an event, a separate digital trigger is used for pretriggering on an analog input. In addition, any of the subsystems can be operated by a delayed trigger, the delay determined by a user-programmable sample count.

The three-board family

The current family of DT3801 boards comprises three models, the DT3801G, DT3808 and DT3809, each providing different choices of analog input for different applications. The DT3801G provides eight differential channels with 12-bit resolution and sampling rates up to 250,000 samples/s. Software-selectable anti-aliasing filters are available to reduce high-frequency noise. Inputs can range from ±10 V, with selectable gains of 2, 4 and 8 available to increase the effective resolution.

The DT3808 includes an internal simultaneous sample-and-hold for channel-to-channel phase alignment. Like the 3801G, it also accepts signals from ±10 V from eight differential channels, but includes a 16-bit, high-resolution converter. This limits the aggregate acquisition rates to 160,000 samples/s.

The 3809 is aimed at applications calling for high-speed sampling. It can capture a single channel at up to 1 Msamples/s. It can be configured to read either eight differential or 16 single-ended inputs at 12-bit resolution.

Shipments of the new boards are expected about mid-August 1992. Quantity-one prices for the family vary, with the DT3801G being the most expensive at $7,595, and the DT3808 the least expensive at $7,195. The high-speed DT3809 is in the middle at $7,495. Data Translation also offers a variety of development tools, including a complete developer's kit in which the company repackages the Spox DSP operating system and TI's tools.

— Warren Andrews

DT3801 series at a glance

- Integrated test, measurement and processing boards
- Full PC/AT (ISA) interface
- Independent A-D I/O subsystems with internal or external clocking
- TI 320C40 DSP with Spectron Spox DSP OS
- Uses 320C40 communication ports and intelligent DMA
- 4 Mbytes of DRAM (1 Mword × 32 bits)
- 512 kbytes of SRAM
- 8 kbytes of nonvolatile RAM
- Software development support
- High performance A-D subsystems, up to 1 million 12-bit samples/s
- Two-channel 16-bit waveform synthesizer
- Real-time clock, two 16-bit counters, four-bit static DIO channels

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ASICs & ASIC DESIGN TOOLS

Oki enhances sea-of-gates performance

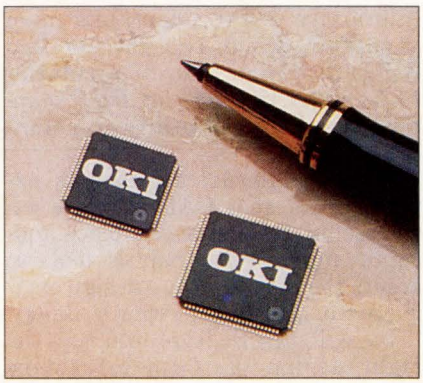
Two weeks ago, Oki Semiconductor (Sunnyvale, CA) announced the 0.8-μm CMOS three-layer metal MSM30S0000 sea-of-gates arrays, with up to 225,000 gates, of which 135,000 are usable. Based on Oki's first-generation 16-Mbit DRAM technology, the gate arrays are 30 percent faster with 75 percent more usable gates per die size than the company's earlier 0.8-mm products.

Also just announced are Oki's 0.8-μm CMOS two-layer-metal MSM91S000 customer-structured arrays, with usable gate counts of more than 150,000 two-input equivalent gates. Based on Oki's more mature 4-Mbit DRAM technology, these products are logically compatible with the new MSM30S0000 gate arrays. MSM91S000 users can merge sea-of-gates "soft" macrofunctions with fully diffused memory and "hard" macrocells on any of Oki's 35 predesigned masterslices, with up to 225,000 total gates. Oki claims that users of customer-structured arrays will improve prototype turnaround time over totally cell-based manufacturing techniques.

Though the MSM91S000 customer-structured arrays will operate from 2.7 to 5.5 V—at oscillator speeds of up to 50 MHz at 3 V—the MSM30S0000 gate arrays operate at 5 V (with clock speeds higher than 50 MHz), with a 3-V version planned for release in July. Marketing manager Cliff Vaughan explains, "Since the MSM30S0000s are fabricated in a new high-speed process, we're having to characterize the 800-cell library at 3 V. We have to be satisfied with the accuracy."

High-performance options

Both the sea-of-gates and structured array products have up to 840 configurable I/O cells. Ensuring high performance in both technologies, according to Oki, are timing-driven layout and clock tree macrocells. "With timing-driven layout," says Vaughan, "users can trust that their silicon will match the prelayout simulation." Oki's clock tree driver macrocells guarantee less than 1-ns clock skew at a fanout of 2200 at 70 MHz. To optimize clock tree implementation, Oki's layout software uses a dynamic-driver-placement and a subtrunk-allocation procedure. By offering both gate-array and structured-array users a choice of designing in high-speed macrocells for critical paths or high-density macrocells for noncritical paths, Oki provides the opportunity to trade speed for density and thus reduce total chip power and cell area.



Tiny surface-mount packages, such as the 80- and 100-pin TQFPs shown here, can be very cost-effective for 3-V ASICs like Oki's MSM91S000 customer-structured arrays. The 100-pin TQFP can handle about 0.6 W, making it suitable for about 25,000 gates at 20 MHz, or 20,000 gates at 25 MHz. A 128-pin TQFP, capable of handling about 0.75 W, will be available before year's end.

The MSM30S0000 gate arrays, available in seven sizes starting at 11,000 gates, offer a standard product library of 82CXXs, UARTs and multiport memories. Other features include typical gate delays under 250 ps, with I/Os and registers usable to over 150 MHz.

The MSM91S000 customer-structured arrays offer a higher level of integration than the gate arrays and faster design capture and simulation than cell-based products. For embedded SRAM, you can use Oki's predefined SRAMs, with 6- to 12-ns access times; or you can compile up to 64 kbits of SRAM optimized for speed, with access times ranging from 6 to 15 ns, or up to 256 kbits of SRAM optimized for density, with access times from 12 to 20 ns. ROMs optimized for speed are available with densities greater than 256 kbits, and ROMs optimized for density to over 10 bits/gate area. Oki's sea-of-gates macrocell logic functions are also available to MSM91S000 users.

Both of the new ASIC technologies feature automatic test vector generation using scan macros, with JTAG boundary scan in development. Circuits designed with MSM91S000 customer-structured arrays are available in quad flatpacks of up to 304 pins, with power dissipation capabilities greater than 3 W. Both gate arrays and structured arrays are available in thin quad flatpacks (TQFPs). Oki supports ASIC design software from Cadence, Dazix, Ikos, Mentor Graphics, Synopsys, and Viewlogic.

NREs (nonrecurring engineering expenses) for the MSM30S0000 start at $29,300, with price/gate at 0.066 cents for quantities of 50,000 pieces a year. NREs for MSM91S000 customer-structured arrays start at $53,600, with price/gate at 0.07 cents for quantities of 50,000 pieces a year. —*Barbara Tuck*

0.8-μm ASICs at a glance

- Three-layer-metal sea-of-gates arrays at 5 V
- Two-layer-metal customer-structured arrays, 2.7 to 5.5 V
- Up to 225,000 total gates
- Up to 840 configurable I/O cells
- Clock tree macrocells with < 1-ns clock skew
- Timing-driven layout software
- Automatic test vector generation using scan macros

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ASICs & ASIC DESIGN TOOLS

High functionality per cell in AT&T FPGAs

AT&T Microelectronics (Allentown, PA) has announced the first two devices in its new FPGA family which will ultimately have 3,000 to 20,000 usable gates. Initial family members are the 5,000-gate ATT1C05 and the 11,000-gate ATT1C11, both fabricated in 0.8-µm two-layer-metal CMOS. AT&T has fine-tuned its FPGA toolset to the Optimized Reconfigurable Cell Array (ORCA) architecture of the new FPGAs.

The company based its ORCA FPGA line on what it refers to as a homogeneous, rectangular and symmetrical architecture. ORCA devices comprise arrays of programmable logic cells (PLCs), with each PLC containing a programmable function unit with four latches and a 64-bit configurable lookup table (four 16-bit SRAMs plus a group of seven multiplexers and a two-input NAND gate), along with associated routing. The 64-bit configurable lookup table in the ORCA FPGAs is the largest currently available, according to AT&T, and lets you combine larger logic into a single PLC, permitting the most critical paths to be compacted into very few PLCs.

On the move

Though initial ORCA devices are being fabricated in 0.8-µm two-layer-metal CMOS, AT&T plans to move to 0.5-µm three-layer-metal technology. User-defined I/Os in the new FPGA family will range from 120 on a 10×10 PLC array in the 3,000-gate device, to 288 I/Os on the 20,000-gate device on a 24×24 array. AT&T claims that system clock rates for ORCA devices go as high as 80 MHz.

Built into the AT&T FPGAs is the capability to perform nibble-wide datapath operations (addition, subtraction, shift-register, and counter) on two bused signals, whether four, eight or 16 bits wide. Also available in the ORCA devices are buffers for driving heavily loaded nodes that are speed critical.

AT&T says its software tools, developed hand-in-hand with the silicon, unlock a number of architectural features to relieve you of the burden of having to know architectural details. "Today's first-time FPGA design success rate is terrible compared to that of ASICs," says Robert L. Bailey, AT&T ASIC product line director. "That's due largely to the relative inefficiencies of available CAD tools."

AT&T tools supporting the ORCA FPGA devices include a pre-layout static timing analyzer, post-layout hazard analysis tool, automatic timing-driven technology mapper, and place-and-route tools, as well as an interactive design editor, bitstream generator, design rule checker, and SoftPath design migration translators and partitioners for direct mapping to and from gate arrays or standard cells.

"AT&T Microelectronics is exploiting its vast CAD software expertise in timing-driven place-and-route and circuit analysis tools to create the most efficient design environment possible," reports Bailey. "This will provide logic designers the right design platform to achieve first-pass success on the ORCA high-density, high-speed, high-I/O reconfigurable FPGAs."

Timing input

Input to the pre-layout static timing analyzer includes such timing specifications as clock periods and I/O timing requirements. With that data, the timing analyzer generates a set of timing requirements to be passed on to the technology mapper and place-and-route tools. Because the ORCA architecture features passive, active and long lines to optimize routing, the software can choose the fastest connection for critical paths. The new tools can perform incremental logic changes, layout changes during packing, placement and routing, as well as post-layout edits where only the sections of the FPGA design being changed are affected. Post-layout timing analysis tools backannotate timing data to simulation tools and also to AT&T's interactive editor. AT&T supports Cadence, Data I/O, Mentor, and Viewlogic for design entry, high-level synthesis and simulation.

Beta CAD tools will be available next quarter, with production tools expected fourth quarter. CAD licensing fees range from $6,995 to $14,995 for PC platforms, and from $13,450 to $21,450 for Sparcstations. Samples of the ORCA FPGA devices will be available fourth quarter. In 100-piece quantities, the ATT1C05 5,000-gate device in a 208-pin quad flatpack is priced at $240, and the 11,000-gate ATT1C11 in a 304-pin quad flatpack is $710.

— Barbara Tuck

FPGA ORCA family at a glance

- From 3,000 to 20,000 gates
- From 120 to 288 I/Os
- Up to 80-MHz system clock rates
- Configurable lookup tables for optimized logic utilization
- Direct mapping to and from gate arrays and standard cells
- Pre- and post-layout timing analysis
- Hierarchical routing

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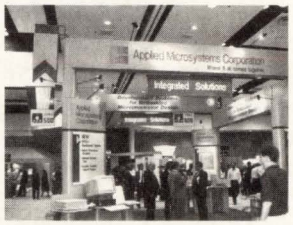

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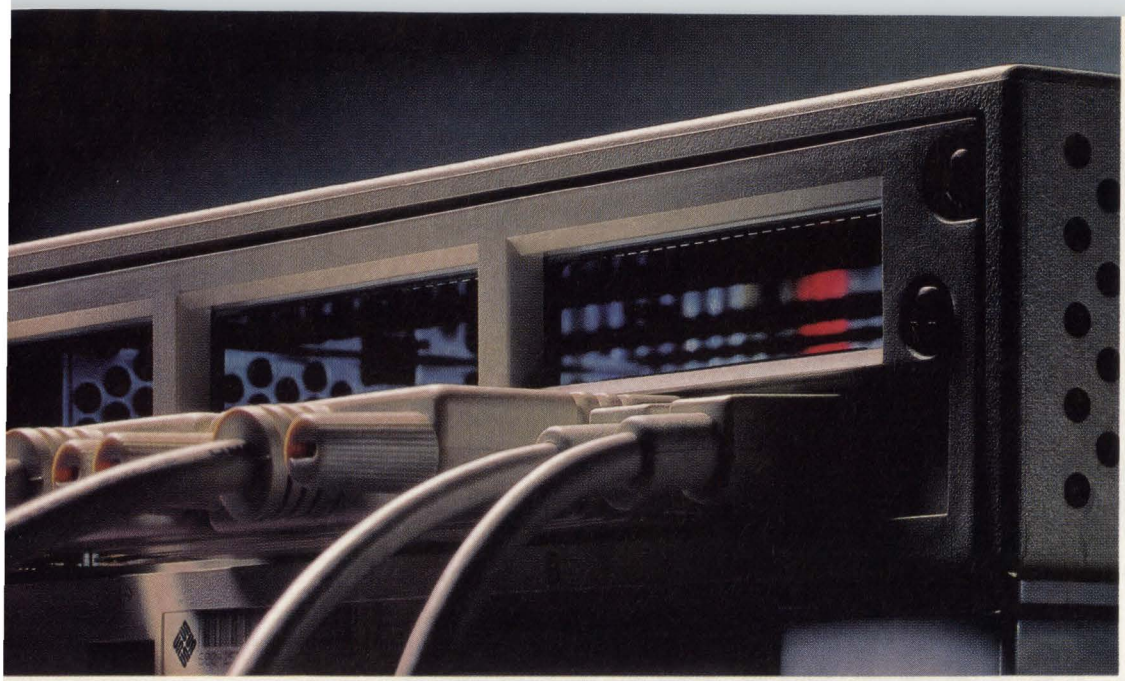

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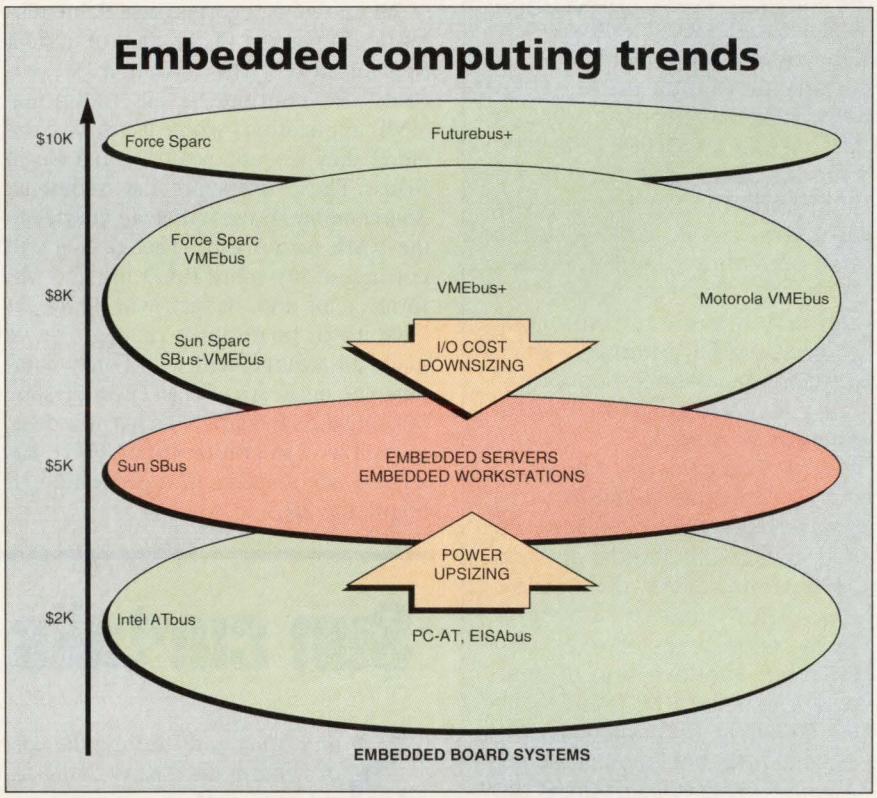
SBus News®

Technology and Market Update for SBus Users and OEMs

Sun hangs onto share of VME market

According to a recent survey by Venture Development Corporation (Boston, MA), Sun Microsystems of Mountain View, CA has an impressive 17.1 percent of the single-board computer market. This places the company behind only Motorola (Phoenix, AZ), which has a 26.8 percent market share, and ahead of Force Computers (Los Gatos, CA), with 9.6 percent. Peter Palm, director of board marketing at Sun, believes that the company will retain as much as—and perhaps more than—70 percent of its total board business as SBus, with the remainder shifting to Sparc-based VME products.



Market divisions

"The market will be divided into roughly three areas," says Palm. "Right off the bat, some 50 percent of those customers [using Sun products] will shift directly from VMEbus to SBus for I/O." Many of these customers, he says, are more traditional embedded workstation users who'll take advantage of the smaller SBus form factor to streamline their product designs.

"Another 20 percent of those currently using Sun SBCs," continues Palm, "will eventually move over completely to SBus. However, because of a hesitancy to abandon VME, or because some VME functions may not yet be available on SBus, these users will remain on VME and use an SBus-to-VMEbus adapter. These users build systems where the packing considerations can be handled, and the performance penalties of the bus-to-bus adapters can be tolerated."

Such adapters are available from a variety of manufacturers, among them Bit-3 (Minneapolis, MN) and Performance Technologies (Rochester, NY). "In fact," according to Don Turrell, SBus

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SBus competition heats up

As a straightforward workstation bus, SBus holds the lead by a wide margin over its closest competitors, Turbochannel from Digital Equipment Corporation (Maynard, MA), and, to the extent that it can be separated from the personal computer market, MCA (Micro Channel Architecture). But the competition is heating up, with Turbochannel in particular making major gains. A handful of SBus developers are starting to see demand grow for Turbochannel, and they're beginning to offer it as well as SBus option cards.

"Though SBus certainly has a lead in the market now," says Bill Kehret, president of Themis Computer (Pleasanton, CA), "Turbochannel has been growing steadily over the past several months. We see a need for Turbochannel hardware, particularly in the high-performance communication and networking arena."

DEC also sees Turbochannel as being slightly behind SBus in the rankings, but believes it's coming on strong. "We now count more than 400 members in our TRI/ADD program," says DEC TRI/ADD communications director

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Goldchip at alpha sites

Although the Motorola/Sun Goldchip won't be commercially available until sometime in August, a handful of companies have been busy with alpha site development projects. One of those companies is Chi Systems (Pleasanton, CA), which has been working with Sun to squeeze a full HiPPI interface onto an SBus card. "Sun has a high-performance connectivity problem," says Chi Systems vice-president Douglas Felder. "The only way that people can connect high-speed channels such as HiPPI to the Sun environment has been through VMEbus. SBus has not been much of an improvement."

"The Goldchip set, however," Felder continues, "lets SBus correlate much more closely to the real bandwidth needs of such communications channels." Since Sun doesn't support a block mode, transfer rates with the VME interface are, at best, only a couple of Mbytes/s. With the Goldchip, on the other hand, the first round of chips has been able to achieve rates of 80 Mbytes/s, and this will go to 160 Mbytes/s downstream. The basic HiPPI data rate is 100 Mbytes/s.

Chi Systems' SBus board is a major achievement in terms of board density, even though the finished board occupies two SBus slots. In addition to the Goldchip set, the board has to house the HiPPI chip set as well as the 100-pin HiPPI connector. "If we had to use discrete parts for the interface," Felder says, "it wouldn't have been possible to get everything on the board within either the real estate or power budget."

Sun hangs on

continued from page 131

marketing head at Performance Technologies, "Performance was primarily a VMEbus maker and became involved in SBus by offering an SBus-to-VME adapter. Since then, Performance has experienced a rapid expansion of its SBus business."

Those two categories, says Palm, represent 70 percent of the total of current Sun business. "The remaining 30 percent," he continues, "are traditional VME applications where users have decided they do not want to upgrade to SBus. These users are the traditional Sparcengine 1E users that are married to the VME form factor. Though Sun will not invest any more R&D in the VME form factor and, in fact, will no longer have its 1E board in its catalog, we've made an arrangement with Force Computers to take care of such customers, by offering the 1E board, which it now does, as well as a migration path." Force has already announced a next-generation 1E board, the 2E.

The penalty for staying with the VME form factor and VME SBCs, instead of going to Sun Sparcstation motherboards with SBus I/O, according to Palm, is that VME users will be about a year behind Sparcstation performance levels. For example, Force's 2E board will be available this spring without the VME interface, and later in the year with the interface. Sun's Sparcstation 2 as a board-level part has been available for over a year. "And very soon," says Palm, "we will be announcing a more powerful machine. Sun will transfer this technology to Force, but it's expected to take about a year for it to ramp up."

Upsizing and downsizing

In addition to hanging on to the bulk of its traditional business, Palm believes Sun, through its Sparcengines, will gain an increasing share of the embedded computer market because of the performance and small form factor of its product. Performance requirements in computing, graphics, networking, and other compute-intensive functions are forcing

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Sun curtails support

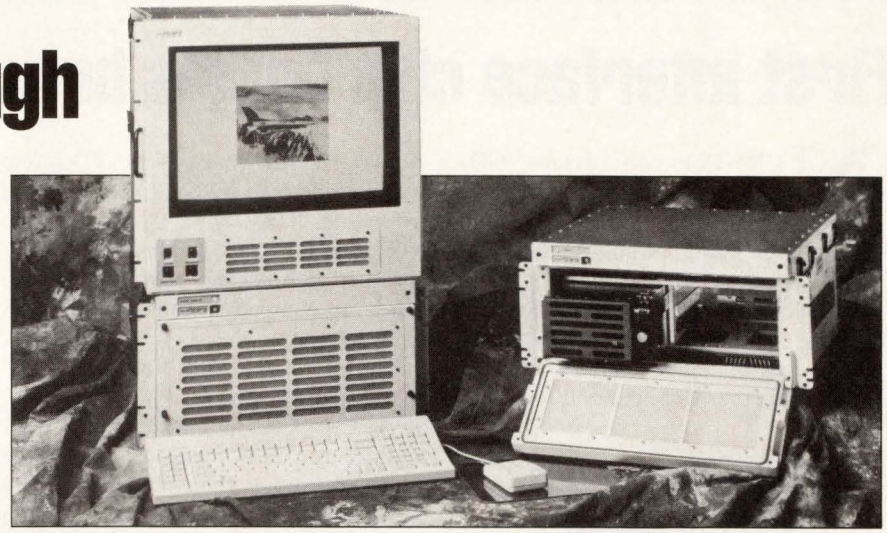
Sun's apparently feeling the cost of helping third-party SBus developers and has stopped accepting inquiries for SBus support. The company is suggesting that potential SBus product developers take advantage of some of the private consulting services available. Sun previously offered a full support package, including layout and design assistance for SBus vendors. In addition, it offered a full technical staff, the use of company workstations and a variety of software and hardware design assistance.

The program apparently did what was intended, attracting more than 100 SBus vendors offering more than 260 different SBus option cards. But the cost of such support—with the growing numbers of SBus users and vendors taking advantage of it—seems to have become unmanageable.

The company will continue to offer the SBus developer's kits and other support materials, but not the other support services. Included in the kit are the *SBulletin*, a quarterly publication with tips and hints for software and hardware development, and the *SBus Rule Book*, intended to guide designers. Further, has been quoted as saying that it's "very adept at anticipating problems and questions with forthcoming products from Sun, and is proactive about getting hints, tips and workarounds to users."

Says Sun's director of board marketing, Peter Palm, "There is now a network of third-party professional consultants available with the necessary expertise to help any SBus developer with any project. And while Sun cannot continue that support, the third-party consultants are trained professionals and have a going dialog with Sun." ●

SBus gets tough



With its relatively compact form factor (about 8 ½ × 11 in.), the Sparcengine board and associated SBus card is suited for a variety of military applications with a little hardening. Recently, a major contract was awarded Codar Technology (Longmont, CO) to provide Sun with ruggedized/Tempest Sparcstations and disk subsystems as part of a four-year Combat Air Forces Workstation (CAFWS) project.

Under the contract, Codar will supply its ruggedized/Tempest Sparcstation 2 with 28.5-Mips performance along with its 2.4-Gbyte disk storage subsystem. The company's Sparcstation 2 is enclosed in a ruggedized/Tempest system chassis and includes 32 Mbytes of memory, a GX graphics card, a ruggedized/Tempest 19-in. high-resolution color monitor, and a keyboard and mouse.

According to Steven McCann, Codar's manager of business development, "The new ruggedized Sparcstations comprise a Sun Sparcengine 2 motherboard with graphics SBus card mounted on a special shock isolation tray which floats on an isolated platform." He says the Tempest unit carries all the EMI and signal isolation, including EMI gasketing, required for Tempest operation.

"Though the unit isn't qualified to full mil temperature range," says McCann, "it's designed to operate over a 0 to 50° C range. When we receive incoming boards, they go through a 100 percent AQL inspection and an environmental stress screening."

Similarly, the SBus option boards included in these systems are thoroughly screened. "Currently," McCann says, "we use boards from Sun, Performance Technologies and Force."

And while the current contract—some $48 million to the prime contractor, Sun—has Codar busy, the company has some other exciting new products right out of the lab. One is a notebook Sparcstation, fully ruggedized and Tempest-compliant, using an active TFT matrix display. This unit will bring Sparcstation 2 power, complete with sophisticated graphics, to the battlefield.

In June the company also introduced a flat-screen monitor based on a new CRT developed by Zenith which uses a flat tension mask. In addition to the flat screen, which provides distortion-free images, the tube uses a finer dot pitch (0.26 mm instead of the conventional 0.31), which gives a brighter, clearer and higher-resolution image. ●

Sparcengines serve broad application base

Sun Sparcengines and attendant SBus I/O boards are being found in an increasing number of applications that have traditionally been the domain of backplane buses, PCs or proprietary designs. The combination of relatively low overall cost, compact form factor, rugged construction, versatile and inexpensive I/O, and flexible operating system have endeared SBus to many who normally use other buses.

One of the fastest growing market segments is mission-critical data routing. These applications are found in routers and gateways as well as voice response systems that allow you to check bank and credit-card balances using your touch-tone phone buttons. The Sparcengine/SBus board is especially suitable for information routing because of its Unix multitasking environment and software-handling capability.

The size of the Sparcengine/SBus board—about 8 ½ × 11 in.—has endeared it to customers requiring rugged construction. As a result it can handle many military C^3I applications. And in medical imaging, Sparcengines have been designed in by the top three manufacturers of MRI and CAT scanners. The combination was selected for its power to handle complex imaging and the ease with which it provides complete networking capability.

On the factory floor, Sparcengine/SBus solutions have been particularly successful in test machines—especially electronic test equipment—though some can also be found in power-plant and process control. And in computer-integrated manufacturing (CIM), Sparcengines, with their networking capability and available software, occupy a secure position. Factory automation systems are increasingly specifying more complex graphics displays, such as operator stands with multiple windows showing concurrently. New windows must be able to pop up if a process control parameter goes out of limits. Such applications

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First interface chip boasts broad functionality

NCR (Colorado Springs, CO) has now joined LSI Logic (Milpitas, CA), Motorola (Phoenix, AZ) and Nimbus Technology (Santa Clara, CA) in offering SBus interface ICs. NCR's offering differs from the others in two ways, however: first, it's a chip set comprising two chips which can be used together or separately, and second, the chips provide specialized I/O functionality in addition to straight SBus interface and DMA.

This chip set is a compact and inexpensive way to add a lot of functionality.

Chris Cronan, NCR

▼ ▼ ▼

"NCR's SBus chip set represents a major difference in direction from those existing products on the market," says Lyle Wallis, the company's director of chip set products. "While we do provide the SBus interface with second-generation DMA support, we will be the first chip vendor to also include a number of significant other functions."

The first of the two chips in the set is a full SBus controller, with an on-board DMA 2 controller supporting virtual address accessing and improved caching. In addition, the chip includes a 7990-compatible Ethernet controller core, a 53C90 fast SCSI core, a parallel port, counters, timers, an interrupt controller, and system reset logic.

The second chip contains only a minimal slave-only SBus interface along with other functions that wouldn't require the DMA function. These include a dual-channel 85C30-compatible serial controller, a high-speed 8277A-compatible floppy disk controller and hardware logic.

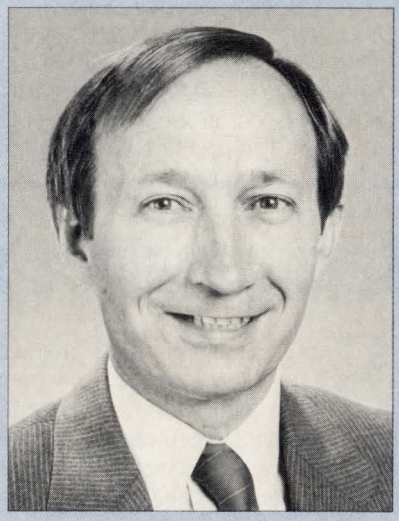
The chips are the result of a joint development effort by NCR and Sun Microsystems (Mountain View, CA), and will be marketed by NCR under license from Sun. They were developed as a collection of macrocells in NCR's standard cell library, and will be fabricated using the company's submicron CMOS process.

Chris Cronan, NCR's product manager for chip sets, says the chips will target two basic areas. First, makers of Sparcstation clones will want to use the chip set to supply the extra functionality to Sparcstation motherboards. Cronan didn't discuss whether or not Sun itself would be taking that approach. The second major area is add-on adapter boards. "Many adapter boards need additional functions, and this chip set is a compact and inexpensive way to add a lot of functionality," says Cronan. A key word here is compact, since an SBus card is not much larger than a normal 3- × 5-in. file card.

Though the chip set has been designed, NCR is cautious about providing any release date and pricing at this time. "We've seen silicon, and it looks good," says Wallis, "but we're still a ways off from production." Wallis wouldn't let himself be pinned down on a date, but he indicated that the release date would be this year. He was even more indefinite about price. But the chips will be packed in 160-pin flatpacks and will probably be a sizable die—even using a submicron process. ●

Spec Sightings

Working group letter ballot complete



IEEE P1496 Working Group chairman Wayne Fischer reports that a significant step in the SBus standard approval process has been completed, and the group continues on schedule. "The core working group," he says, "has completed the initial task of converting Sun's SBus specification, Rev B.0, into a proposed IEEE standard." In the process, it worked its way through a number of problems encountered in turning the specification into IEEE language and settling some ambiguous points.

The standard then went out for a 30-day ballot, the returns of which were expected early in May. Comments received will be reviewed, and any updates to the draft will be completed for a possible 10-day recirculation of the draft. "Our plan is to start the official IEEE sponsor ballot on June 4," says Fischer. He optimistically feels that the balloting should be concluded by October 15—in time to submit the necessary paperwork to the IEEE to make P1496 a standard by year's end.

In tabulating the working group letter ballot, Fischer says the 75-percent rule is being invoked—75 percent of the returns must be affirmative, since some of the members have been unable to attend any working group meetings. At press time the ballots hadn't been tabulated, but Fischer reports that progress is steady and he anticipates no problems.

DSP provides submicrosecond interrupt response

Tony Agnello
President
Ariel Corporation

Michael Peck
President
Berkeley Camera Engineering

While digital signal processors (DSPs) are probably best known for their high-speed multiply-accumulate capabilities, they're equally adept at performing high-speed I/O and interrupt processing. In fact, DSPs such as Motorola's DSP56001 can routinely achieve submicrosecond interrupt response times, more than an order of magnitude faster than conventional microprocessors such as the 68030.

DSPs in space

Because of this high-speed I/O capability, DSPs are beginning to find their way into interrupt-intensive real-time applications that sometimes require no DSP processing in the conventional sense. The University of California at Berkeley Space Science Laboratory, for example, uses an Ariel DSP56001-based SBus board as a real-time controller for acquiring high-speed telemetry data from the Faust (Far-ultraviolet space telescope).

The Faust flew on board the space shuttle *Atlantis* between March 24 and April 2, 1992. Its mission was to electronically photograph a seven-degree area of the sky at far-ultraviolet wavelengths and telemeter the data back to earth. The Ariel boards were used as a real-time data-acquisition front end for a Sun Sparcstation 2 workstation, which was responsible for displaying and archiving the data to tape.

In operation, the DSP board receives telemetry data from the space shuttle as separate 4-Mbit/s and 56-Kbit/s streams. The 4-Mbit/s bitstream is used to relay photographic data at in excess of 80,000 photons/s. The 56-Kbit/s stream contains housekeeping information such as the instrument's position, voltage, currents, and temperature.

Upon receiving the data, a Xilinx gate array on the Ariel board parallelizes each data stream and signals the DSP. The DSP, in turn, executes an interrupt handler that reads the data a word at a time from the Xilinx chip, interleaves the two data streams, does some error checking, and moves the data into a buffer located in the board's 96-Kbyte local SRAM.

A Unix application that resides on the Sparcstation is responsible for emptying the DSP buffer, moving the data to a buffer on the Sparcstation and writing it to the tape drive. To do this, the application periodically issues read calls. In response, a Sparcstation-resident device driver configures an LSI Logic SBus DMA controller, which resides in the Ariel board; the DMA controller moves the data to a buffer in the Sparcstation's main memory. From there, the SCSI bus transfers data to a tape drive for archiving. Some of the data, such as instrument voltages, currents, and shuttle position, is also displayed in a window on the Sparcstation.

Stiff real-time requirements

To keep pace with the two incoming data streams in real time, the system has to meet tight real-time constraints in two areas. First, it must to be fast enough to move the data from the Xilinx controller to the DSP buffer. Second, it must be able to continuously empty the DSP buffer, move the data to a Sparcstation buffer and write the data to the tape drive.

To process the two incoming data streams, the DSP must be able to service two interrupts, one from each data stream every 4 µs. The requirement makes it impractical to use most conventional microprocessors. A 25-MHz 68030, for example, requires 5 µs just to respond to the interrupt, and that doesn't include the time required to execute the handler. If the 68030 uses a real-time OS such as pSOS to manage the handler, the interrupt latency increases to 13 µs.

The DSP56001, by contrast, can respond to an interrupt in 300 ns. Moreover, the interrupt handlers for the 4-Mbit/s and 56-Kbit/s data streams require only 1.5 µs and 1.0 µs respectively. As a result, the DSP can respond to and execute the handlers for both interrupts in less than 4 µs.

The time DSP56001 can respond to interrupts much faster than conventional microprocessors for several reasons. One is that it doesn't have to save as much state information. When the DSP is interrupted, it needs to save only an accumulator and two registers, if resources can be dedicated to the interrupt handler. Another reason is that the DSP's interrupt vectors can contain two instruction words which can include six operations (one ALU and two data moves). As a result, short ISRs can be executed without branching to a separate handler. A third reason for the DSP56001's rapid response to interrupts is that it requires no real-time OS. A C program, which runs under Unix on the Sparcstation, controls the DSP, schedules tasks, invokes DSP-resident ISRs, and performs housekeeping tasks such as setup and buffer management by writing to the DSP's host command register.

To keep pace with the incoming data streams and avoid a buffer overflow, the system must also be capable of emptying the DSP board's buffer at the same rate that it's filled. The DSP requires about 200 ms to fill the buffer. To keep pace, the Unix system must issue and complete a new read call about 20 times per second.

Unix tricky

Ensuring that Unix issues a new read call at any rate is tricky, because Unix is neither preemptive nor deterministic. The frequency at which it issues read calls is dependent on the other tasks that are running on the system and their relative priorities. To ensure that the data acquisition task is serviced on a regular basis, it's run as a -19 NICE superuser.

In tests done using the system configuration described for the Faust application, the average time between read calls was about 1.5 µs. Even the worst-case time between read calls, which was about 50 to 100 ms, was well within the 200 ns required for the DSP to fill the buffer. ●

SBus Competition

continued from page 131

Joan Peterson, "and more than 75 percent are directly involved in Turbochannel projects." One of the significant factors in Turbochannel's increase in market share, says Larry Robinson, software engineering manager for DEC's TRI/ADD program, is that DEC is trying to broaden Turbochannel's support.

"Originally," says Robinson, "we were a MIPS Ultrix-based support organization, but with Turbochannel starting to appear on some of the VAX platforms and being slated for future Alpha processor-based products, we're moving support into the VMS and OSF operating systems, into the realm of the other architectures—both VAX and Alpha."

Robinson reports that DEC has been busy increasing technical staff and trying to put in place support for those architectures. "There are already 46 Turbochannel products shipping," says Peterson, "fifteen of which are from DEC. These cover a broad spectrum, from communications and networking cards including Ethernet-, token ring- and ATM [Asynchronous Transfer Module]-based networks to a variety of bus adapters."

"We're beginning to cover all the solutions," adds Robinson, "perhaps not in as much depth as SBus, but at least with critical option cards. What's important is that we have all the required solutions. For example, it's sufficient to have four or five serial communication cards—we don't need 20."

DEC is working to make sure all the critical areas are covered, either by the company itself or through third-party vendors. "We supply a constantly updated hot list of customer's requirements so third-party option card makers can address significant areas," says Sonia Fahey, North American recruiter for DEC's TRI/ADD program.

New developments

Turbochannel will probably be in even hotter pursuit of SBus in the near future as several new developments emerge. First, says Robinson, "We're in the process of completing our Turbochannel ASIC, which will serve as the front end for option cards, replacing a handful of discrete cards." Second, the independent group of nine vendors now charged with maintaining the Turbochannel specification is discussing the possibility of increasing the data bandwidth of the approach, compatible with earlier versions.

Turbochannel can't take advantage of the approach used by Sun in its B.0 version of SBus, nor can it use the MCA or VME approach, where data is multiplexed over the address lines to effectively double bandwidth; this is because Turbochannel already multiplexes address and data lines to minimize pin count. Instead, faster Turbochannel cards will simply double the clock rate from 25 to 50 MHz. Compatibility will be maintained with earlier generations by encoding the configuration ROMs so that the system automatically transmits at the correct rate for each card. ●

Sparcengines

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need the full multitasking capability of Unix.

While the Sparcengine is being adopted into many such applications, it's not the only entrant. Certainly, in applications calling for multiprocessor functionality, the Sparcengine/SBus combination isn't easily used. Many other real-time applications also require software support that hasn't yet emerged in the Sparc environment. It's reported, however, that help is on the way in the form of a joint announcement from Lynx, the Posix-compatible RTOS developer, and Sun, with its own soon-to-be-released Solaris 2 OS, which reportedly has real-time capability. ●

Sun hangs on

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users to upsize computer performance from PC AT, EISA, STD, and other devices. At the same time, many applications, from machine control to medical imaging systems, are looking for smaller form factors and lower power supply requirements than can be provided by traditional VME or Multibus systems.

"In addition," continues Palm, "those moving up are also looking to take advantage of more flexible operating systems. For example, many users are looking for the networking advantages of a Unix-type operating system instead of DOS. And those looking to downsize from VME and Multibus II not only want to reduce the physical form factor, but the Sparcengine platform also lets them significantly reduce the cost of I/O through SBus."

What's precipitating much of this change is the use of specialized I/O chips and ASICs, which let many I/O functions reside on a single board with a mezzanine card handling any additional I/O. The very high volumes in the PC and workstation markets have significantly reduced the cost of these chips. Palm believes downsizing will have a significant impact on the traditional backplane-bus market. ●

The next installment of **SBus News** *will appear in the September issue of Computer Design magazine.*

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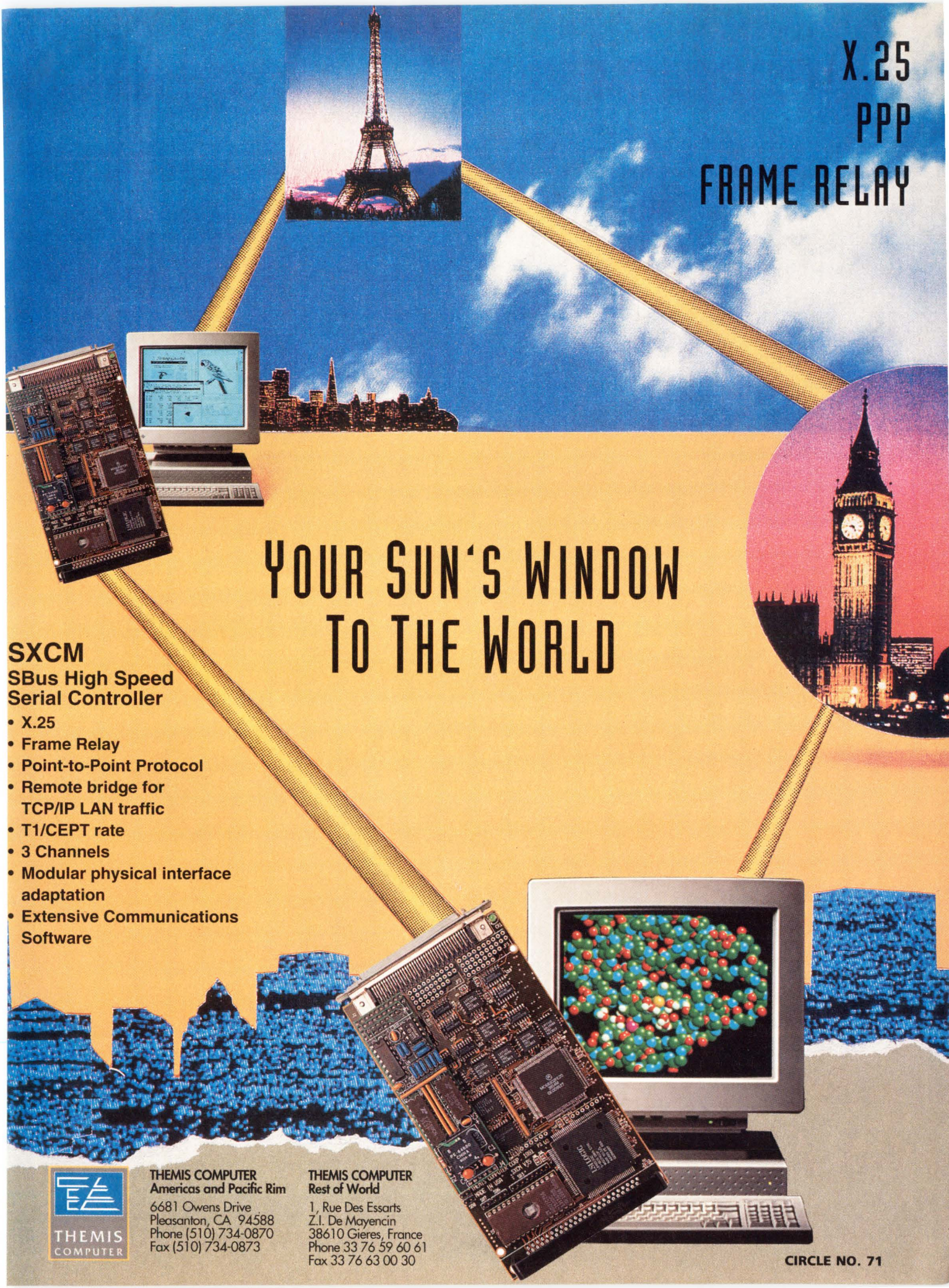
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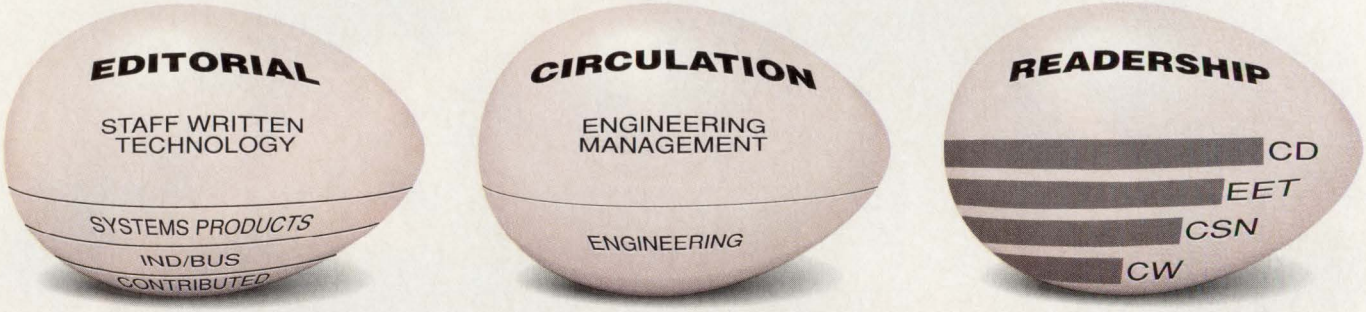

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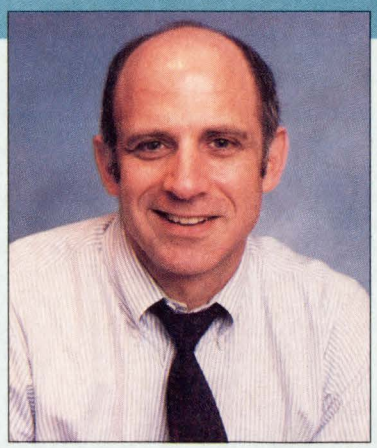

Analog behavioral simulation: not yet system-level

I seem to be getting it from both sides these days. On one side, people who work extensively with Spice believe I've overstated the case for high-level modeling. On the other, people in the forefront of abstract model development feel I've underestimated the physics and mathematics that go into behavioral modeling, even the streamlined models that offer simulation speedups.

I've suggested in earlier columns that analog must follow digital behavioral modeling in shifting its focus toward system-level activity and away from the physics of individual devices. While no one questions the direction I say we're going in, the "grand leap" I've projected for analog behavioral modeling—a separation between structure and function—will not occur anytime soon. The march toward a system-level description capability for analog and mixed-signal designs—an analog hardware description language (AHDL)—is inexorable, but it will be a long march.

AHDL years away

"AHDL won't be here for another four years," predicts Jim Solomon, president of the analog division of Cadence Design Systems (Santa Clara, CA). Until it comes, top-down design for analog will be limited. Without a synthesis capability, in fact, even top-down digital design is a questionable proposition, according to Solomon. More simulation work will be done on an intermediate level, for example, with Spice primitives. "We're above the physics level," Solomon points out, "but not that many levels up."

I've suggested many times before that if you're slinging 1s and 0s around, you can afford to be removed from the actual electronics that implement a digital circuit. If you're controlling voltages and currents, however, you must get much closer to the electronic devices that produce them. Much of the current behavioral model development, as a consequence, is taking place on a circuit level which remains fairly close to the transistor- and semiconductor device-level. This includes Saber model development by Analogy (Beaverton, OR), as well as Spice macromodeling efforts by companies such as Meta-Software (Campbell, CA) and Microsim (Irvine, CA). This mid-level modeling effort is also the focus of Spice-compatible extensions from Electrical Engineering Software (EES—Santa Clara, CA) and Cadence Design Systems.

It's perhaps the 20-year marriage to Spice and other device-level modeling techniques that will effectively delay top-down design tools for analog. Because analog design is decidedly a bottom-up activity, mid-level modeling activity will remain interesting and important for some time to come.

No smart models for analog

While dedicated modeling companies such as Logic Automation (Beaverton, OR) have developed elaborate digital simulation models (Smart Models) for microprocessors, DSPs and math coprocessor components, there's little work on this level of integration in the analog and mixed-signal realms. The most integrated linear components in Analogy's model libraries, for example, are op amps and linear voltage regulators. Mixed-signal devices—analog-to-digital and digital-to-analog converters, in particular—exist as templates and hypermodels which must be more fully developed by the user for particular applications. The majority of the 3,000-odd devices in the Saber model catalog, in fact, are diodes, small-signal transistors and analog renderings for 7400-series logic. Let's be clear about this: there's a considerable amount of complexity embodied in these models, because they view logic transitions over continuous time rather than as events occurring at discrete time intervals.

It's insufficient in analog terms, for example, to suggest that everything above 2.4 V is a logic 1 and everything below 0.9 V is a logic 0. We really need to see everything that happens to a voltage as it transitions from 0 to 1 and back again. Even a rectifier diode model will require considerable mathematical sophistication if its nonlinearities are to be modeled accurately. Whatever speedups over Spice have been attributed to Analogy's Saber simulator, Saber models utilize the same equation system—Modified Nodal Analysis. Despite their mathematical rigor, however, there's nothing among the Saber models that depicts

an IC with several thousand (or even several hundred) transistors.

A brief visit to a Saber users' group meeting in February, however, suggested that ever-higher levels of integration may not be among the highest priorities for analog and mixed-signal system designers. The modeling of electromechanical interfaces—the inductive kick from a motor coil, for example—was a major area of concern for the attendees of Assure '92, which included a high proportion of aerospace and automotive engineers. A proud new addition to the Saber device model library, in fact, is an IGBT, an insulated gate bipolar transistor. High-voltage, high-current IGBTs will be used as power driver transistors in all-electric cars—one of the most promising developments of this decade.

"Many engineers are simply looking for models of new devices that didn't exist before," suggests Kevin Walsh, president of EES. The thin-film transistors (TFT) used to illuminate new-generation LCD panels is one example. IGBTs are another. EES's Spice-compatible simulator, in fact, is being used by engineers at Ford to model the crosstalk generated by electrical arcing across the high-current switches of an automotive system.

"We tend to think of vehicles as complete systems," says Gary Zack, the technical specialist for analog simulation at Ford Motor Company (Dearborn, MI). "With just four or five lines of code, we can define an electromechanical extension to Spice primitives." Using both EES's Precise and Analogy's Saber, Zack's department generates models for sensors, relays and other electromechanical devices. An entire project, in fact, simulated the inrush current for lamps. "You need thermal models as well as electrical ones," says Zack. "You want to know what that lamp is going to do when you turn it on—whether it's a cold day in Minnesota or a hot one in Florida."

The availability of accurate models remains a key concern. Participants in a panel on modeling at last year's Analog and Mixed-Signal Design Conference agreed that there would always be considerable labor and expense involved in model development, but they were split as to whose job it should be. Stephen Parks, the bipolar ASIC product manager at AT&T Microelectronics (Reading, PA), expressed a view which should be typical of ASIC vendors, though it may not be. He said, "We're obligated to provide detailed models for our customers."

Hal Alles, corporate architect at Mentor Graphics (Beaverton, OR), however, said that CAE tool vendors can't be expected to provide models of devices and semiconductor processes. This sentiment was echoed in a recent conversation with Cadence's Solomon. "No CAD supplier can provide the models," he said, "the user has to do that." What the tool vendor can supply, however, is easy-to-use toolsets for model development.

Keys to the kingdom

The keys to a usable AHDL, it's becoming increasingly clear, reside with the tools for behavioral model development. There are several worth considering. Analogy's C-like Mast language, for example, is considered a candidate for an IEEE AHDL standard, and is being considered by the DARPA-funded MHDL (Mimic HDL) development group as a standard for microwave systems hardware. While not a formal language, Cadence's Profile is a Spice-compatible behavioral modeling extension which Solomon feels could easily be a subset (with the emphasis on subset) of a future AHDL standard.

Both Saber and Profile, however, are supported by what I'd classify as rudimentary graphical code generators. Both model generators provide a graphical environment in which you can describe transfer functions (or block-level elements such as amplifiers, comparators or phase-locked loops); you can also embed these descriptions with other device models in a full subsystem simulation. In the case of Saber, its graphical extension lets you quickly generate a model that can be used with other models in a Saber simulation. Profile does the same for Spice or Spectre.

While if/then/else software statements are typically required for any kind of interaction with digital system elements (i.e., for mixed-signal simulation), they're typically most distracting to an analog designer. However, they can be handled automatically by the model generator. The analog transfer functions, which are easier for the analog designer to specify, are entered in much the same way as solver statements or formulas are entered into the cells of a Lotus- or Quattro-type spreadsheet. To be sure, there's a little more work involved than evoking a graphics screen and filling in the parameters, but the description of transfer functions isn't as difficult as generating C code from scratch.

Models without programming

The graphical code generators serve as a partial response to the problem of generating behavior models without learning a software programming language. "Modeling is different than programming," maintains Eric Filseth, director of analog system marketing at Cadence. "Analog designers are language-resistant."

One can argue that Filseth is absolutely right; that analog designers don't feel comfortable with C-like programming constructs. One can also argue that most digitally-trained designers—who will, in fact, take more responsibility for analog and mixed-signal design in years to come—feel comfortable with high-level language constructs. I've certainly given voice to both viewpoints in this column.

"Top-down design depends on an analog hardware description language," Dr. Ian Getreu, Analogy's cofounder and vice-president of modeling, wrote in a technology trend piece. While few would challenge this statement, the open questions are: Which language? What level of abstraction? How much graphical support? It may be many years, in fact, before analog modeling moves beyond the middle level on which it's currently focused.

Stephan Ohr is president of Indian Forest Research and editor of the monthly newsletter, Mixed Signals.

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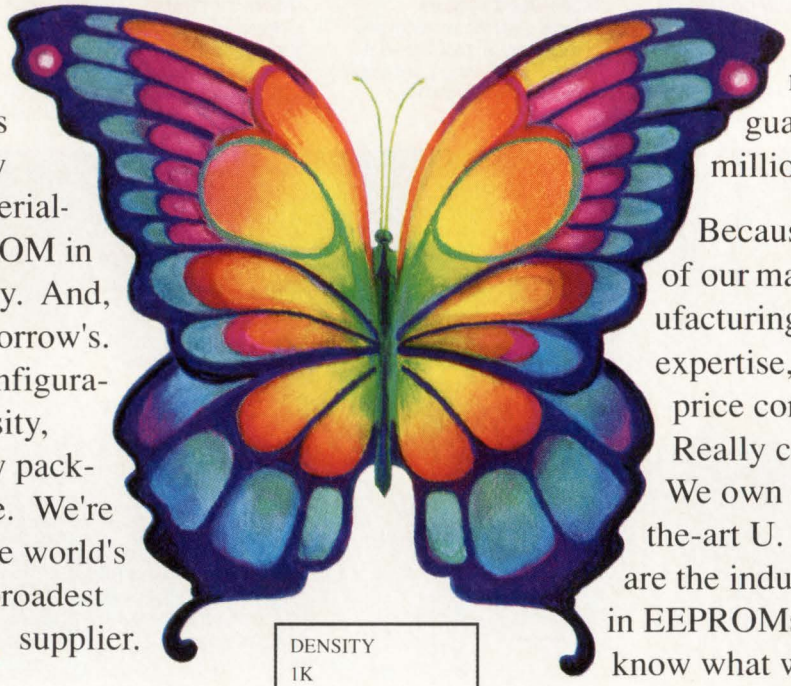

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Inside looking out

For years I've watched as graphical user interfaces and operating systems have come and gone. While many have promised the world, none has delivered more than a small continent, and lack of widespread use and market momentum have kept most of these islands unto themselves.

Recently OS/2 held the most promise as a multitasking environment, but it never panned out. Crash after crash sent many would-be users back to the drawing board after being burned by spending money and time with development systems, compilers and procedures that lacked a well-implemented core.

Each new version of DOS has provided a few more features and hooks, but none has solved the problems of serious CAE developers. Even the latest incarnation, DOS 5.0, carries with it many of the older problems that have shackled the personal computer in tackling complicated engineering problems.

Programs running under DOS 5.0, for example, are still limited by segmented architecture to 640 kbytes of RAM, even though many device drivers and other programs are TSR (terminate-and-stay-resident) that can load in higher RAM. TSRs free up most of the 640 kbytes for program execution, especially since DOS 5.0 takes up less run-time RAM—but the 640 kbyte barrier still exists.

While DOS extenders from third-party companies have found ways around memory-related problems, they're expensive. CAE vendors don't want to foot the bill for an OEM solution to what they consider to be an inherent defect in the operating system, because such a solution may put their products in a higher price bracket. Moreover, DOS extenders don't solve some other important problems, such as those related to graphical and I/O device standards.

Real engineers don't use icons

I must admit that, as a power user, I don't like icons. True, it's sometimes a pain to remember a string of invocation switches and parameters, and it's often a hassle to traverse partitions and directories to get to a program while manipulating data in other files. But you get a strange feeling of accomplishment when you've filled up your command line buffer.

While icon-based shells are obviously simpler to use, they remove you a level or two from the actual processing, and this can lead to sloppier operations. I like to know every file in my directory; I like to be able to delete unneeded device drivers and maintain my disks and files myself. While utilities will let me do that, even within an icon-based environment, less experienced computer users will quickly fill up their hard disks and won't know how to clean up their directories and files, since they typically won't go through the school of hard knocks.

But even apes must evolve, and I have to admit that icon-based user interfaces may have their place in the newest and up-and-coming Windows software from Microsoft—not because of the pretty screens or point-and-shoot operations, but because of the environment which they offer to software developers who want to pack a lot of punch in their software and still keep the price within reach of the average engineer.

Windows eases software development

Many of today's popular CAE vendors now provide or will provide Windows-based engineering software. Note that a truly native-mode non-Windows implementation will always outperform a Windows-based version of the same software as far as processing speed, graphics redraw speed and overall performance are concerned—and by a factor of 10 to 100 percent.

But Windows provides a higher platform upon which to stand. This is true, first, because the graphical environment is taken care of. Instead of having to write several—or even dozens—of special drivers for the many graphic card versions available for the PC, the CAE vendor depends on Windows to handle the graphics. It then becomes the graphic card manufacturer's responsibility to provide a Windows driver for that card. This leaves the CAE software vendors time to make their high-priority products better and more comprehensive.

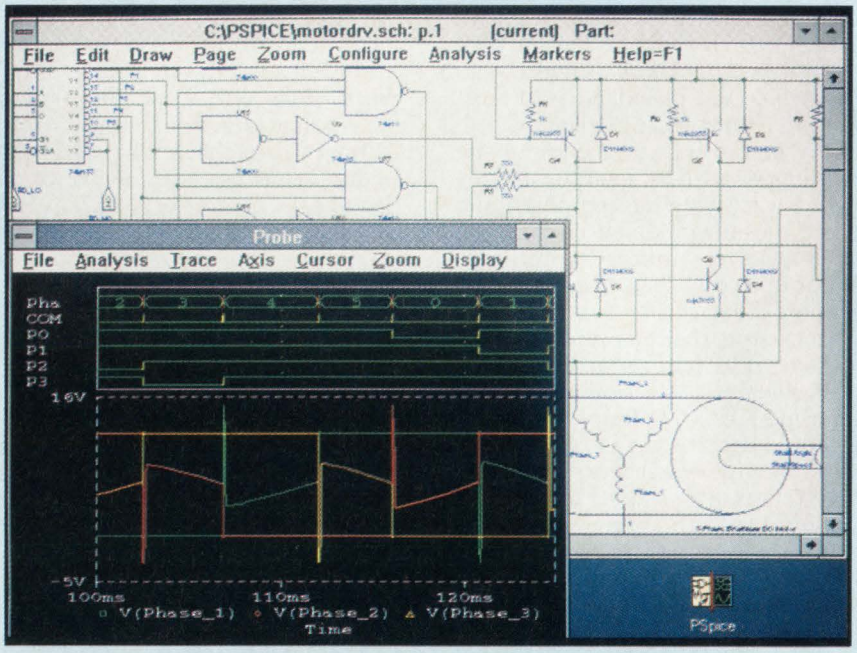
The same is true with input devices such as mice, tablets and digitizers, as well as output devices such as printers. Note, however, that specialized, less popular equipment—plotters, PLD programmers, in-circuit emulators, and other equipment in unique or proprietary formats—may have to be coded into the CAE application. But Windows can make basic I/O device handling easier for software vendors.

More important is the ability of windows to overcome memory limitations. Through expanded and extended memory managers, Windows lets your programs use larger chunks of memory—as much memory, in fact, as you can stuff in your sockets. By handling swapping and even the virtualization of memory through disk usage, Windows lets you use many of the programs that couldn't be implemented without that extra memory.

But Windows applications are not the easiest to program and come with quite a bit of overhead. One programmer I spoke to gave an example. The standard function of resizing a window can be handled in different ways. An application can clip a graphic rendering at the borders of the resize, or it can scale the image. Each case must be taken into account separately, and each is not a trivial task.

This example points up both a benefit to users and a burden to programmers—the benefit being multiple ways to perform a task, and the burden being the multiple ways the task must be programmed. To effectively integrate into the Windows environment, then, requires an extensive familiarity with the Windows program and the many intricate and subtle case scenarios that a Windows application must deal with. This carries an entirely new overhead with it, one that's independent of the application.

As a result, many bugs may exist in a Windows program which may not manifest themselves until a specific combination of operations occur. While these bugs will inevitably be nailed down, the burden of their debugging may ultimately lie with the user.



The Windows version of pSpice provides the familiar Windows personality, letting you configure the working environment specifically to your application.

The rush to Windows is on

Windows-based CAE programs are now emerging at a rapid pace. But beware: while many programs may run under Windows, they may not be true Windows application programs. If the program runs directly from DOS, it's not a true Windows application, which can only run in the Windows environment.

Many FPGA design tools are finally taking advantage of the benefits of using a Windows operating environment. Altera, for example, provides the MAX + Plus II software as a Windows application. So, too, is the Quicklogic pASIC Toolkit for the new family of FPGAs from that company. New on the block is Lattice, which is now starting to ship the pLSI Development System for its newly announced EEPROM-based FPGAs. Data I/O's popular Abel PLD and FPGA software is reportedly on Windows and soon to be shipping in Windows flavors. All of these systems can take advantage of the Windows clipboard for importing text and cutting and pasting around different files, as well as for using the big blocks of memory often required to tackle large PLD and FPGA designs.

Another nice feature of the Windows environment is that several independent but related windows can be open at the same time, showing schematics, logic equations, block diagrams, pinouts, prompts, status blocks, and other functions which used to be combined into one display in non-Windows applications. Here, each subapplication can be resized, moved, closed, and reopened as a matter of user preference. This provides you with more flexibility, decreases learning time and supplies a more homogeneous work environment.

Schematic capture and PCB applications are also coming to Windows. Accel Technologies has already demonstrated a new 32-bit database version of its PCB package with increased resolution (down to 1 μm) and 99 layers of support. CAD Software will also be shipping its PCB design packages as a Windows application.

OrCAD and P-CAD are still waiting for a faster Windows (the up-and-coming Windows NT) before they migrate their schematic capture and PCB tools to Windows. Omation's schematic capture and PCB tools will be on Windows soon, as will Futurenet schematic capture and Protel PCB, schematic capture and digital logic simulators.

One company that's always opted for the highest performance is Viewlogic. Before Windows, the company used DOS extenders to take advantage of deep memory arrays for large designs. Keep an eye out for a true Windows-based Workview to emerge from the company. This may be a more comprehensive pro-

gram, and it may even be less expensive than the original Workview, since the cost of the DOS extenders won't be passed along to users.

Something for the linear designers, too

While it may seem that linear simulation is too compute intensive to benefit from Windows, this may not be the case. Microsim has already shown a Windows-based schematic capture program for linear simulation and will soon provide its linear simulator and Probe waveform analyzer as Windows-based applications.

Deutsch Research is also using Windows for its Spicewindows Professional analog simulation software. The benefit of providing schemat-ic windows with waveform windows is that it helps coordinate the debug, analyze, reiterate, and optimize processes, because they all can be running and displayed simultaneously.

Another area where Windows shines is in data acquisition and control. The new Lab Windows from National Instruments is a shining example of a Windows-based instrument monitoring, data gathering, display, and control application which really makes good use of the windowed environment. Until now, these tasks have been less graphic when performed on PCs, and they've consequently been left to Apple computers, which have always had a window-like environment with true multitasking.

True multitasking is still around the corner for Windows. And its pseudo-multitasking capabilities are limited, awkward and difficult to use. You may have to become an expert on Windows to take full advantage of the more advanced features. But while you're waiting for a simulation run you can be modifying the next source file or editing your documentation—all more slowly than each task would take by itself, but requiring that you take fewer coffee breaks overall.

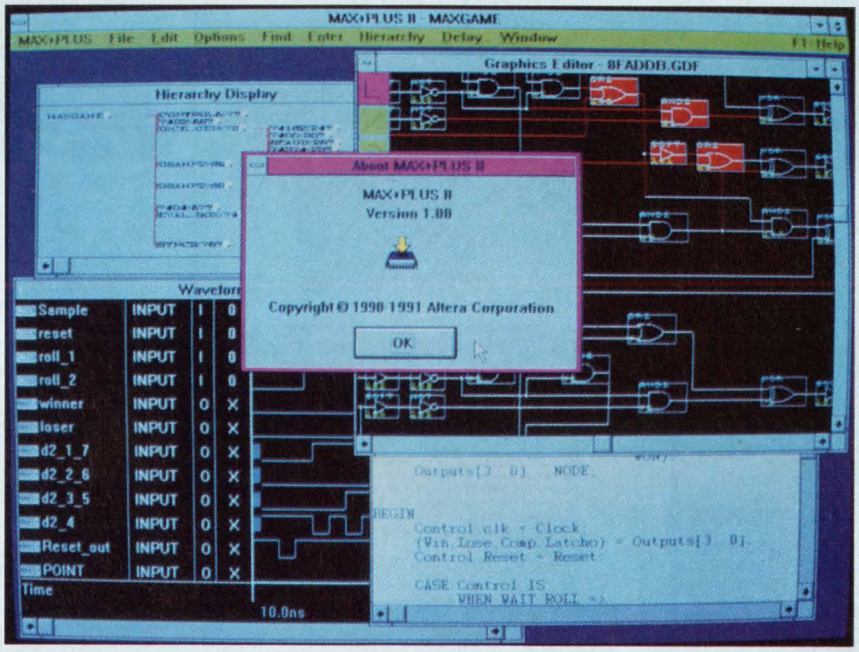
Getting on a stronger horse

To really take advantage of these applications, a more powerful PC is required. While older XTs and 286 machines were fine for the days of Palasm, OrCAD, Tango, and the like, the newer breed of software will require a full-blown 386- or 486-based machine. The ever-popular SX machines may still work but could introduce unacceptable delays. The 286 machines are out, since they can only run in the real mode and won't let you take advantage of the higher-level, enhanced 386 features—they're just too slow.

Windows still has a few problems to be solved. One important one has to do with peripheral device sharing and concurrent control by different processes. For example, we're always running out of serial ports. We may use a mouse, modem, plotter, in-circuit emulator, PROM programmer, PLD programmer, serial printer, and so on. Windows doesn't make direct provision for the external switchers and the multiplexers. This holds true for all parallel ports, although not as critically because fewer devices use parallel port interfaces.

And finally, Windows isn't the only option anymore. Most CAE vendors who have traditionally stuck to PCs are now moving closer to Unix-based workstations. This leads to a higher horsepower migration path while maintaining file compatibility with lower-cost PC-based design seats, it still represents a minor share of the engineering platforms. During the last year, 286- and 386-based PCs still dominated the engineering workplace. The 486 will soon be right up there—the only reason it's not on top now is that 486 machines are still relatively new and have not yet fully penetrated the design labs.

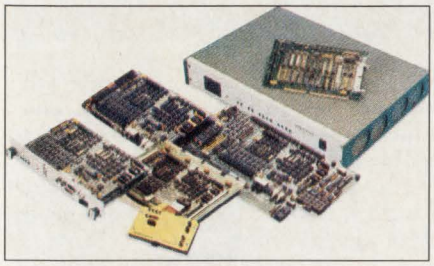
Also, as more companies provide Unix operating systems for PCs, more designers will opt to go Unix. But DOS- and Windows-based operating environments will dominate for quite some time. The low prices of DOS and Windows make them too attractive for companies which are very conscious of cost and performance.



The MAX + Plus II lets you divide the screen, showing logic, equations, waveforms, and reports simultaneously. This speeds design iterations, since all editing can be done in a single environment rather than having to run and rerun each application.

Jon Gabay is a freelance editor with extensive design experience. He has written for all of the specialized CAE/CAD publications at one time or another, including High Performance Systems, Engineering Workstations *and, most recently,* Design Automation.

SYSTEM SHOWCASE



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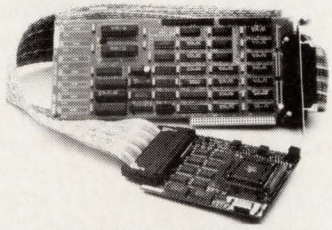

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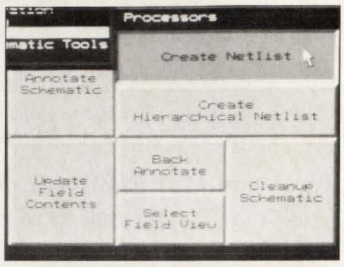

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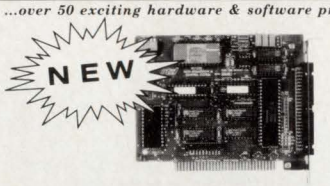

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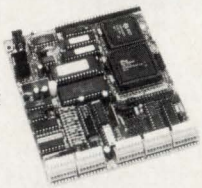

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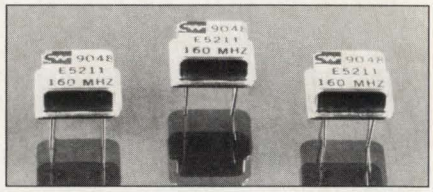

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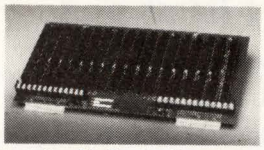

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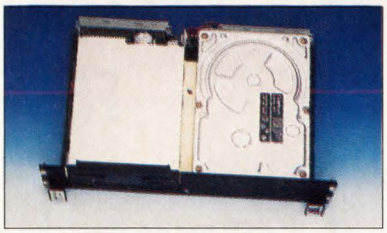

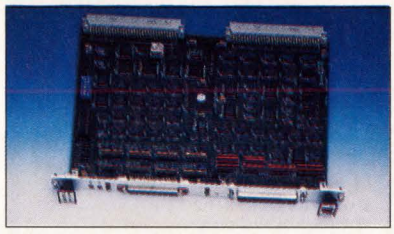

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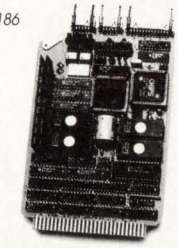

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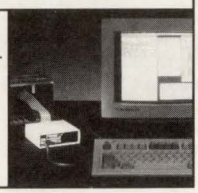

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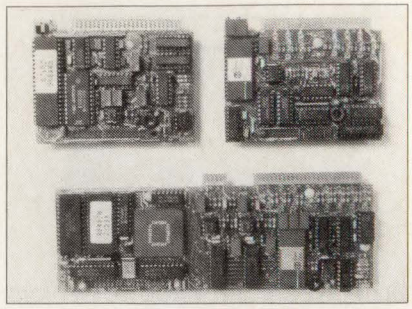

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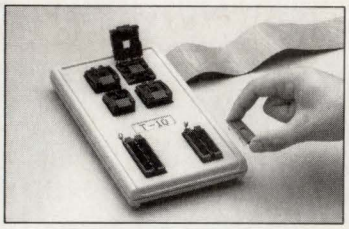

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Last year our March special report on **Fuzzy Logic** generated over **4,100 reader inquiries** and the **April 1992 Fuzzy Logic report** is already poised to generate an even higher number of inquiries! **Reprints of the April article are available now**–quantities of 100 or less are $1.00 each, quantities over 100 are .75 each. To order, call Patti Kenney at (508) 392-2124.

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LETTERS, COVERS & OTHER DIVERSIONS

THIS MONTH'S COVER:
The PC and compatibles have become powerful CAE/CAD platforms and there's a wealth of software packages available to designers. The cover highlights a few, but we've thrown in a couple of ringers. Can you find them?

In the March 1992 issue of *Computer Design*, your Special Report by Jeffrey Child refers to Step Engineering's Express emulator in a very unfavorable light. A customer is referenced criticizing the user interface, and a comment is made about a Windows front-end that ameliorates the problem. The reporting infers that this statement is representative of Step's machine, and erroneously infers that our Windows front-end is a mere replacement for Exmon, which is a Nindy-like interface, familiar to many designers using Intel parts.

In fact, the reference to Peerless as a typical customer is pretty far afield. Peerless was an early adopter of i960CA architecture, using the B-step version of the part. In addition, the early work with the Express emulator was done using an early beta version of the machine. The company also found it feasible to buy a second unit within 90 days of receiving the beta loaner, since it was the only emulation equipment available from July 1990 to about June 1991.

Peerless was also working with early silicon, and much of the chip-emulator interface wasn't fully debugged. The combination of non-working target, an early version of Express and an early revision of the chip made progress slower than might be expected compared to using a mature part and mature support of a relatively new architecture.

Two of the functions that the Express performed and still provides are an execution history with the cache turned on and the ability to set a hardware breakpoint on a cached instruction. These functions were a leap forward from anything else available. The price for these first units was below $15,000, accounting for the skinny feature set and the cryptic user interface.

Peerless stopped using the Express somewhere around November or December of 1990.

In March 1991, Step began shipping an integrated source-level debugger, SDBug, with its Express products. This debugger uses Microsoft Windows as a GUI. This is a much more capable product than just an emulator front-end. It provides the full functionality of a source-level debugger—steps a C line at a time; sets software breakpoints symbolically; displays source code; spawns a watch window for looking at program variables, arrays and structures in native or alternative formats; displays registers at each breakpoint; shows stack information, source code scoping and much more. Its just like the most competitive debuggers on the market.

It has taken a while to round out a state-of-the-art emulator running at 40 MHz, providing full-feature capabilities for a superscalar, cache-based, 32-bit architecture. Step has been supporting these designs from the beginning, and continues to expand its products to provide increasing levels of productivity.

Peerless had special needs, was an early adopter of the chip and emulator, did not take advantage of upgrade opportunities, and hadn't used the emulator for over one year from the time of publication of the article. Couching its input as a typical response, and not allowing Step to respond in the report, did not follow through on the 'when,' 'where' and 'why' of the reporting process. The result has been an unfair representation of Step and Step products.

Kerry W. Pike
Director of marketing
Step Engineering

[The Editor-in-Chief replies.] In an effort to break the one-way flow of communication—from vendor to reader—that has traditionally characterized electronics design publications, we began about a year ago to aggressively pursue input from designers, users and readers of Computer Design. *Our editors now routinely talk to several users for each article they do, choosing them*

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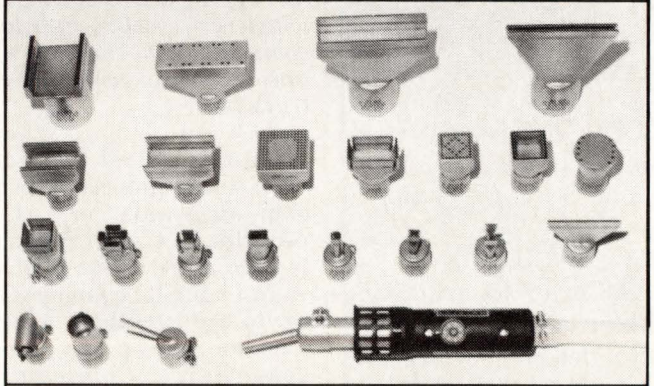

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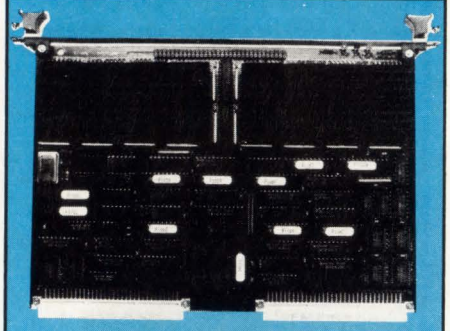

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CIRCLE NO. 77

LETTERS, COVERS & OTHER DIVERSIONS

from names given to us by vendors, from our subscriber list and by calling companies that they believe might be users of the technology or products that are the focus of an article. It's obvious that an editor can't conduct a comprehensive user survey for every article he or she is writing and so tries to determine, during the interview, whether the user is knowledgeable and experienced enough to speak with authority. Even though the user may be knowledgeable and experienced, as was the case with Peerless, there's still a chance that his or her views may not be typical for a variety of reasons; the reasons here were that the experiences being related were a special case, and even worse, were badly out of date. That Jeff failed to uncover these two important facts was an oversight for which he has been duly chastised, and for which both Jeff and I apologize.

From the day we began to gather input from users and readers we knew that we'd run into problems if the comments, observations and assessments we received from users were negative and potentially damaging to a vendor or supplier. We believe, however, that user input is so important that we can't let this deter us. To minimize these problems in the future, every Computer Design *editor will give any vendor or supplier whose product(s) may be cast in an unfavorable light the opportunity to respond to what's been said. If we believe a user's comments are valid, we're going to publish them. We'll try, whenever possible, to balance those comments with the vendor's reponse and let the reader decide where the truth lies.*

I am flattered that you [Steve Ohr] would propose to put me on a chip—or a wafer, or a platter, or a pedestal. But I think you are proposing too ambitious a plan when you want to distill down my wisdom and try to use it without me (see "CAE tools for analog: just interesting or essential?", *Computer Design*, March 1992, p 131). I don't think it's really feasible to take any experienced person, and take all his ideas, and then say that you can use that knowledge in a computer, to be as smart as he is. Isn't that what the expert systems have proposed to do? I think they are not overwhelming successes. I think you need intelligent *people* to interpret and adapt good ideas.

For example, I have written a book on troubleshooting analog circuits, *Troubleshooting Analog Circuits* (Butterworth-Heinemann). I spilled out in this book all of the good ideas that I and my friends had—how to solve (or, better yet, avoid) problems with linear circuits. For a mere $35.00 or so, you, too, can take advantage of this wisdom. But I don't think you can just put that book in a computer, and let the computer do the job. You need intelligent engineers and technicians to ask the right questions and measure the right data before you can even tell which part of the book may be helpful. Requiring a computer to do all the work is *not* going in the right direction.

Human judgment and experience are the necessary ingredients, either to solve a problem and get out of trouble *or* to design a circuit that just works and does not get you in trouble in the first place. I agree that computers can be useful tools to help a wise designer, but when they take their own steering wheels and try to drive themselves, they often crash and burn. So I think that kidnapping Bob Pease is not likely to be a profitable deal, but using the circuits he has designed, *is* likely to be....

Robert A. Pease
Staff Scientist
National Semiconductor

In the design of a computer, the most admirable innovation and skill is displayed in hiding its power switch in a different and most unexpected location.

Nick Atakkaan

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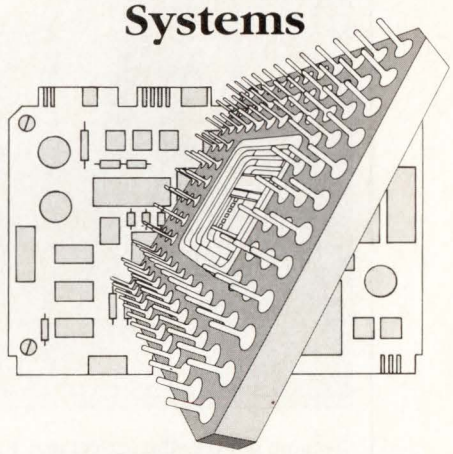

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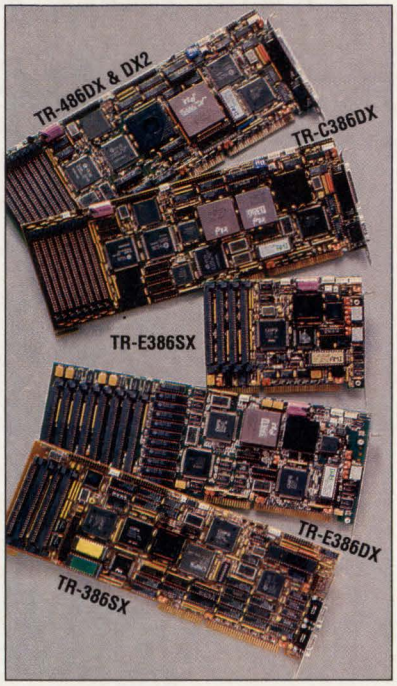

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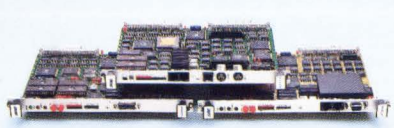

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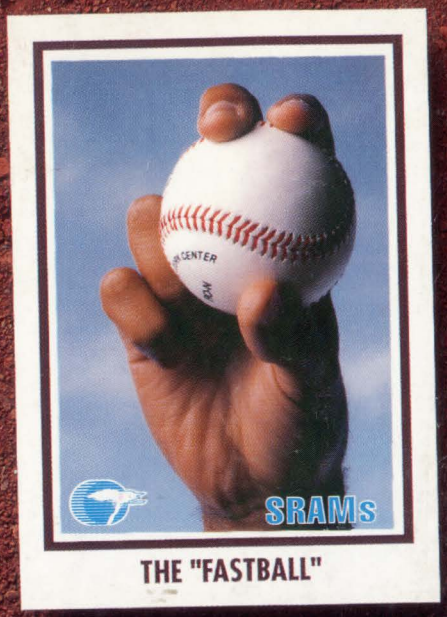

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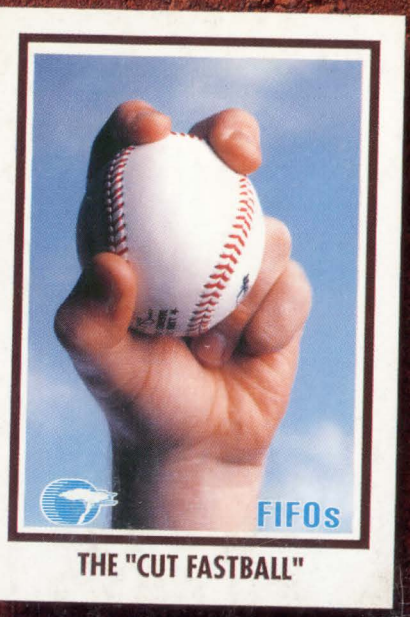

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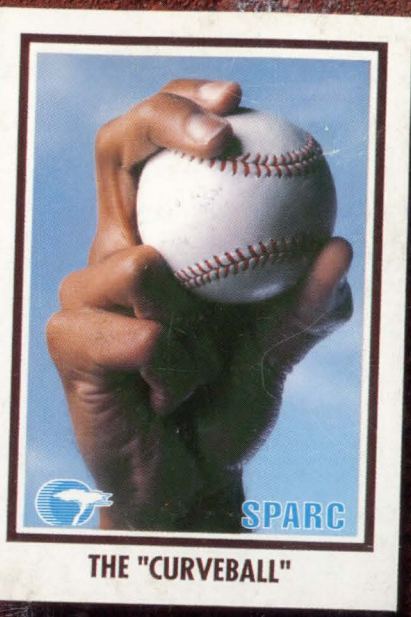

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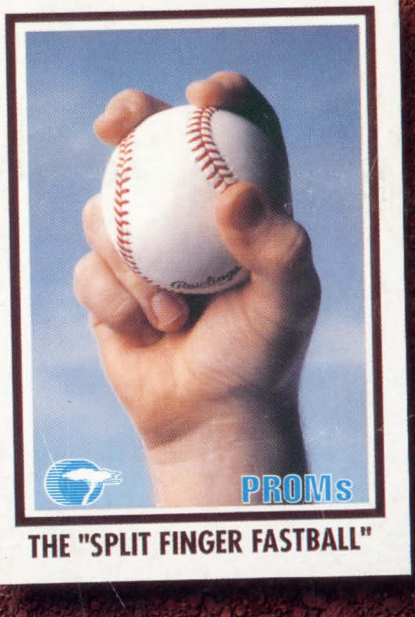

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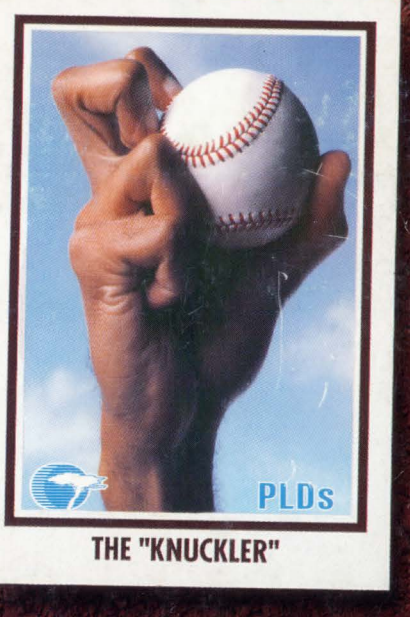

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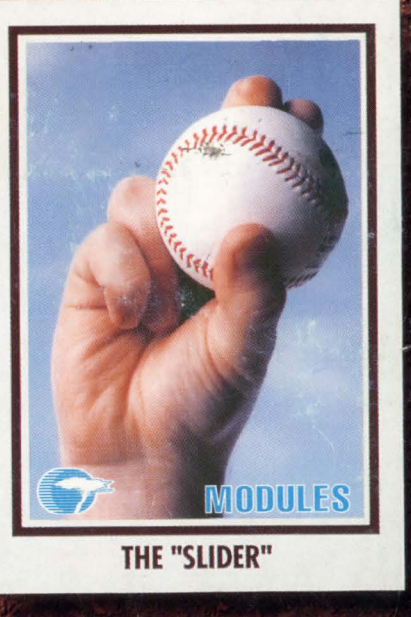

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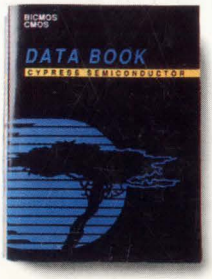

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