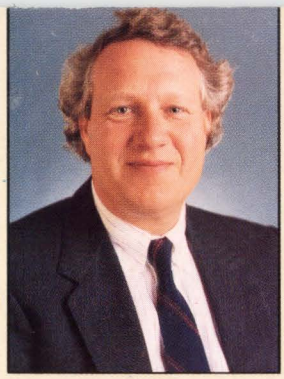
A PENNWELL PUBLICATION FEBRUARY 1992

# COMPUTER DESIGN

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

Technology and Design Directions

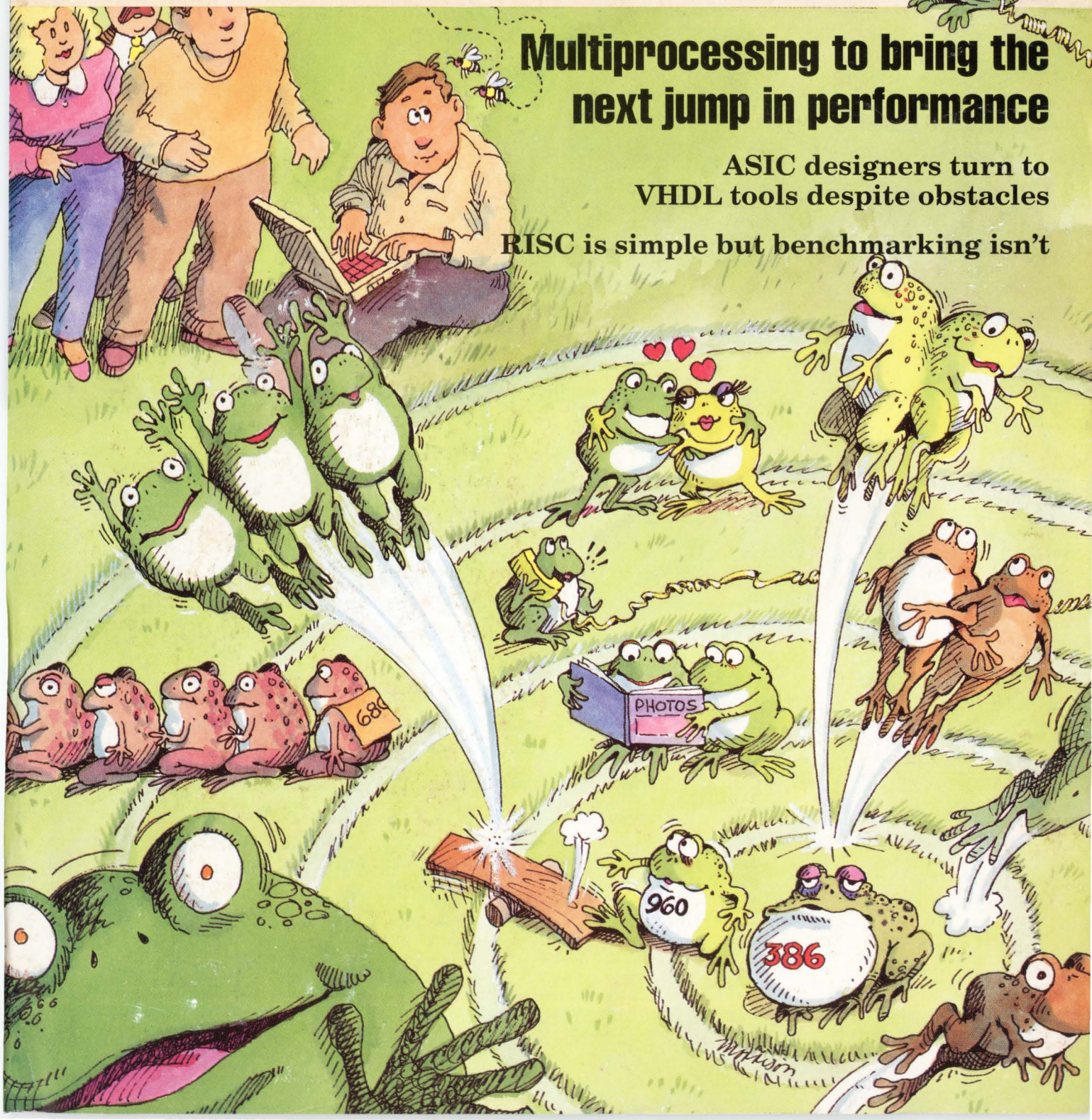


Force's Behrendt on: VME's 10th birthday

## Multiprocessing to bring the next jump in performance

### ASIC designers turn to VHDL tools despite obstacles

### RISC is simple but benchmarking isn't



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**CIRCLE NO. 1**

CIPRICO

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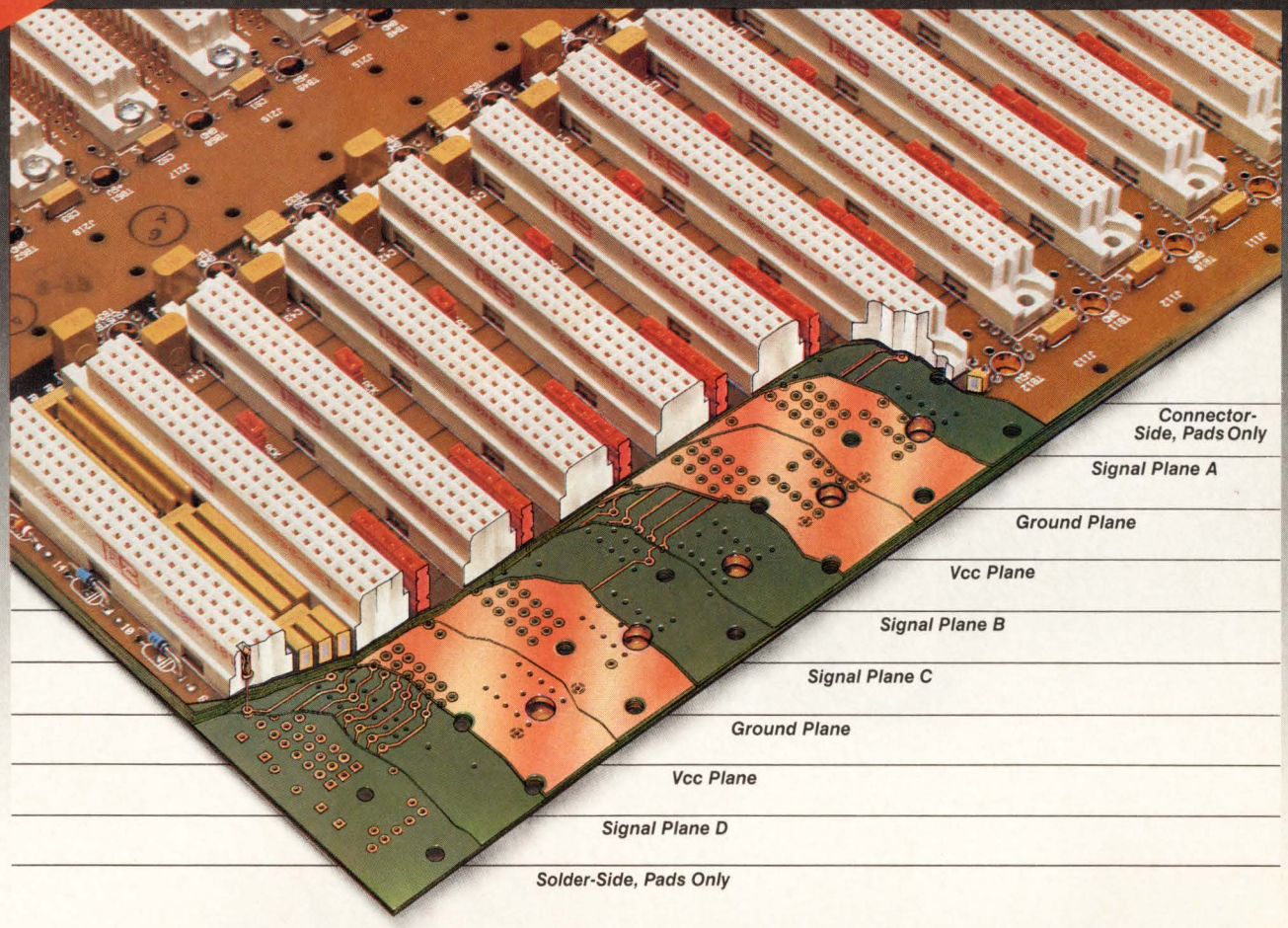


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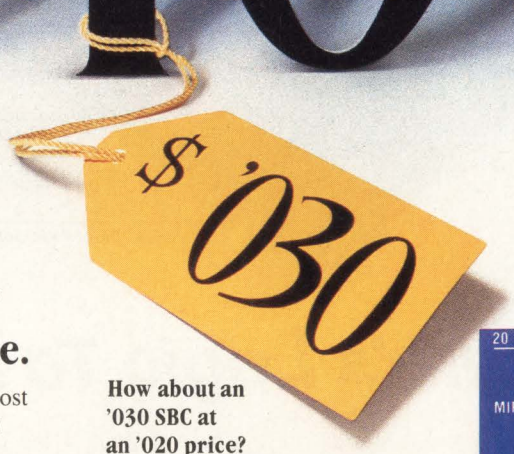
**CIRCLE NO. 2**

# '040




## Synergy brings you the power of an '040 SBC at an '030 price.

It's true. For only $2865*—less than the cost of most '030 boards—you can have a *full-featured* '040 SBC that gives your VME system vastly superior performance.

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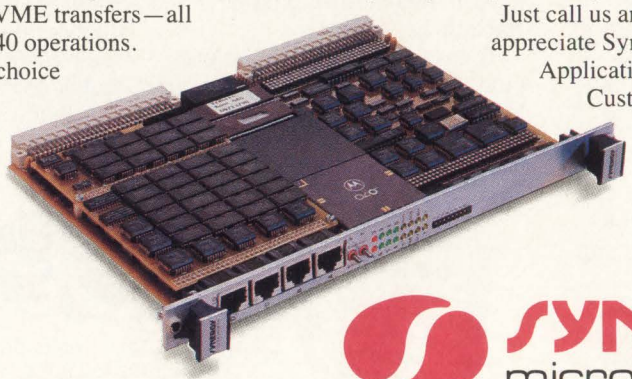
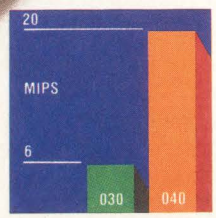
Best of all, there's your choice of over a dozen EZ-bus modules with intelligent I/O—fully compatible with Synergy's entire line of '020, '030 and '040 SBCs. Compare that with any other manufacturer!



**How about an '030 SBC at an '020 price?**

Our new VW30 SBC can plug '030 power and capability into your '020-based system, and at $1595* we'll keep your system price competitive.




The '040 has 3× the performance of the '030; 20 vs 6 MIPS at 25 MHz.

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**CIRCLE NO. 3**

Force's Behrendt on:
VME's 10th birthday
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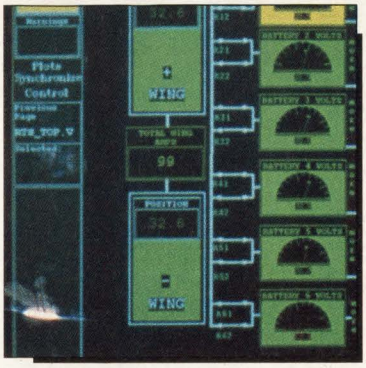
VOL. 31, NO. 2 FEBRUARY 1992

# COMPUTER DESIGN

Technology and Design Directions®

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



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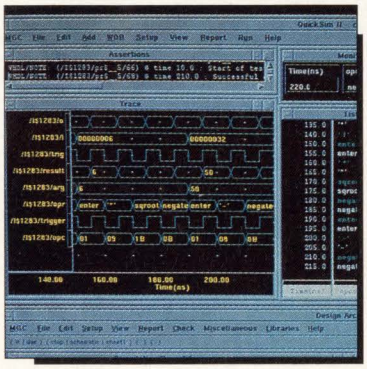
## TECHNOLOGY DIRECTIONS





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## TECHNOLOGY AND DESIGN FEATURES




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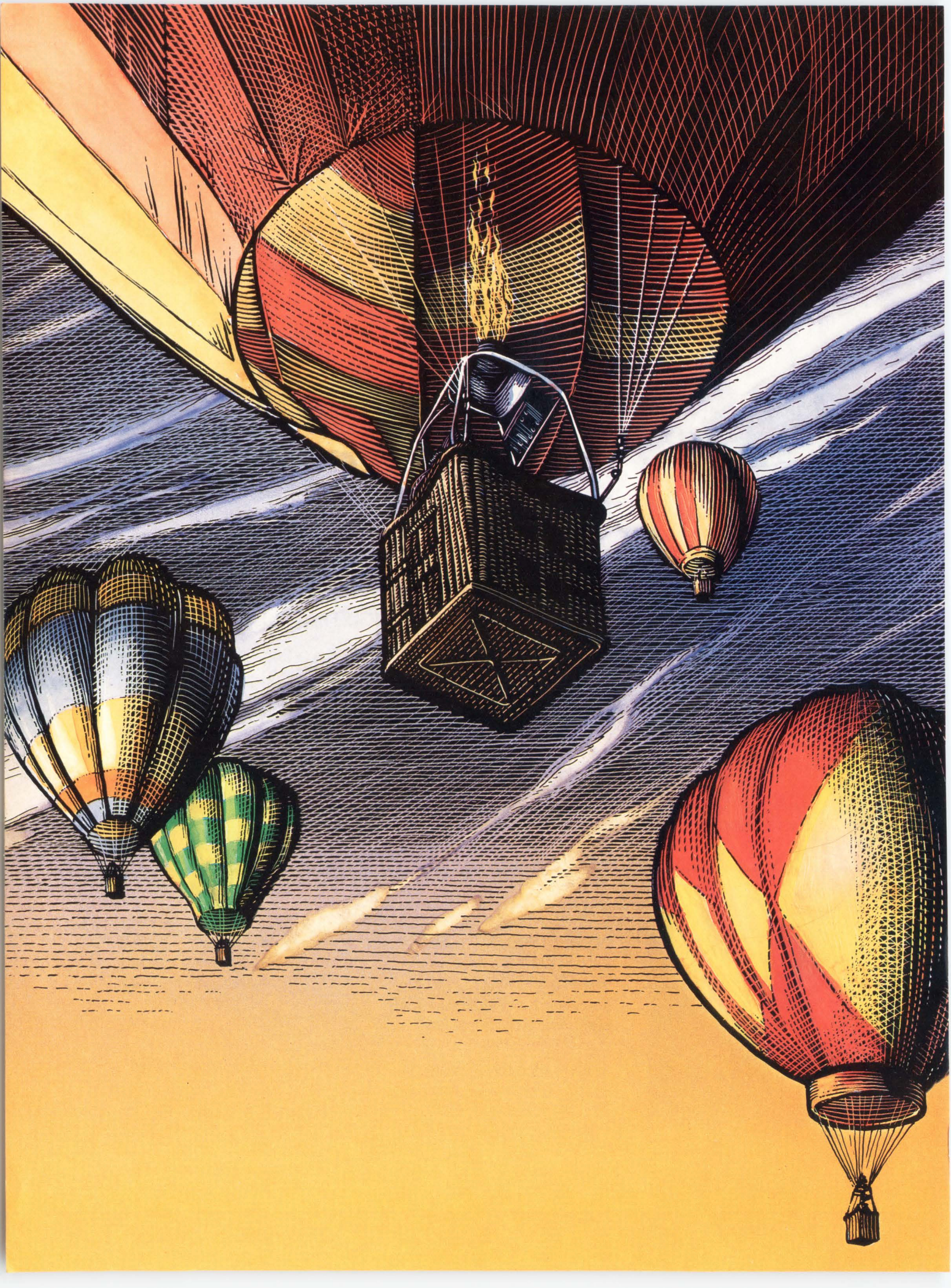
*Cover Illustration: Bill Morrison*

## NEW PRODUCT HIGHLIGHTS



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## THE PATHWAY TO PERFORMANCE.

MOTOROLA

## Will Windows NT sound the death knell for Intel?

Of all the features of the upcoming Windows NT operating system from Microsoft (Bellevue, WA), none is more important than its ability to run on both Intel 386/486 microprocessors and MIPS RISC hardware. The implications of this dual processor strategy are obvious: in the long term, the MIPS architecture, being RISC based, will compete directly with the Intel (Santa Clara, CA) 80X86 architecture. But Intel doesn't intend to give up easily. The 3.1 million-transistor "586"—out this year according to Intel—will borrow superscalar RISC-like technology to give it 100-Mips performance. Oddly enough, 100 Mips is also the figure bandied about by those marketers of the latest high-performing MIPS processor, the R4000. If the two processors do indeed meet the 100-Mips expectations, a price war between the two architectures will decide their fate. And that's a war the multiple-sourced R4000 may win against the sole-sourced 586.

*—Dave Wilson*

## Intel under clone pressure to lower prices

As Intel readies its next-generation 586 CPU and the world prepares to head into a new generation of machines and operating systems, prices for the company's current crop of 32-bit CPUs are coming down. For example, the 25-MHz 386DX processor is expected to drop form $152 to $99 in quantities of 1,000.

The downward pressure on prices is fueled by the successful cloning of the 386 by AMD and the common knowledge that a version of the 486 cannot be far behind. In addition to AMD, Chips and Technologies is known to be working on a 486 clone. Intel will try to remain a vanguard player for these CPUs while preparing to roll out the 586.

The 586, along with the MIPS R4000, will form the backbone of the new Advanced Computing Environment (ACE) that will use the Windows NT operating system being prepared by Microsoft. While NT will run on 386 and 486 machines, it will require 8 Mbytes of memory and will probably slow those processors noticeably in comparison to the speed with which they run DOS/Windows. Given the enormous number of installed 386/486 systems, it will probably take Intel a while to turn the 586 into a real money-maker. The 386/486s are expected to remain big players in the embedded and notebook arenas long after desktop users have switched to NT-based machines, so Intel has a real interest in fighting for market share against the clone makers.

*—Tom Williams*

## At last, LSI Logic is shipping Silicon 1076

LSI Logic (Milpitas, CA) announced about a week ago that it has finally begun to ship its VHDL-based Silicon 1076 ASIC design environment to users. Since the start of Silicon 1076's development a few years ago, LSI Logic has billed the toolset as the first complete concept-to-silicon VHDL solution. Silicon 1076 users can begin an ASIC design at the architectural level, register transfer level (RTL) or the gate level, according to LSI Logic.

Integrated into the Silicon 1076 design environment is the Vantage (Fremont, CA) VHDL simulator and Synopsys (Mountain View, CA) synthesis tools. Asked what Silicon 1076 offers over the use of Vantage and Synopsys as point tools, an early Silicon 1076 user, Mike Payne, VLSI manager at Cossor Electronics, a division of Raytheon, (Harlow, Essex, England), puts an integrated environment first on the benefits list, LSI Logic's block-level synthesizers for memory and datapath elements second, and the ability to work at a higher level of synthesis third.

Though Cossor has saved time with Silicon 1076 on the design of a 300,000-gate system, Payne reports designers have had to synthesize their ASICs—which use pipelined rather than state-machine design—at the RTL level, rather than at the much-talked-about architectural or behavioral level. "The number of gates the tool was producing when synthesizing the pipelined designs at the architectural level was too high," says Payne. LSI Logic reports working on a mechanism for the next Silicon 1076 version that will get around the problem of pipelined design.

*—Barbara Tuck Egan*

## Vitesse in production with first 350K-gate GaAs array

Vitesse Semiconductor (Camarillo, CA) will disclose the manufacture of the first production samples of its 350,000-gate VGFX350K GaAs ASIC in an announcement this month. A member of the FX family of four-layer-metal GaAs gate arrays, this is the largest GaAs ASIC ever produced and validates claims, according to its maker, about the manufacturability of the Vitesse 0.6-μm H-GaAs process technology.

With over 1.2 million active transistors out of 1.5 million total, the VGFX350K incorporates a pair of 44-kbit blocks of fully diffused SRAM, two fully diffused five-port register files and over 200,000 raw gates, based on a test implementation done for a customer. The embedded SRAM and register files have an access time of less than 3.5 ns.

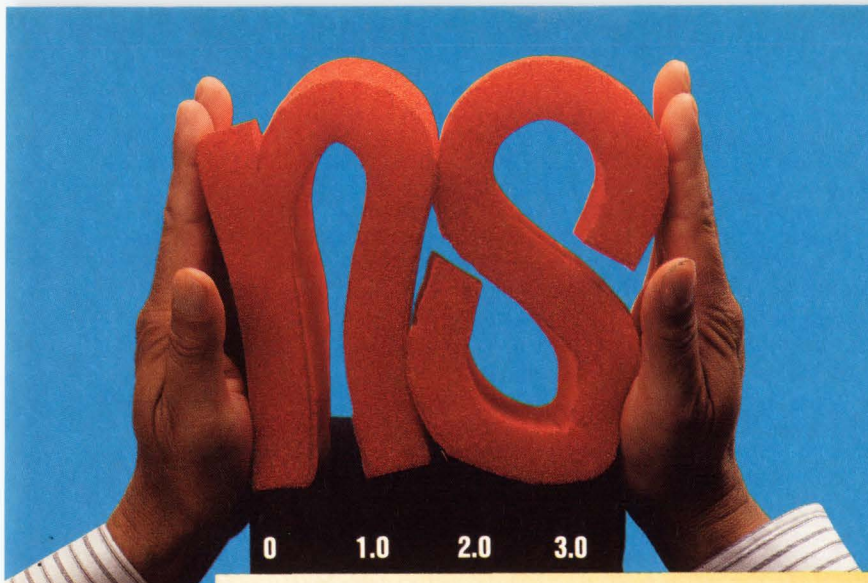
Vitesse will also be announcing the addition of 20,000- and 40,000-gate members to its FX family. A typical two-input NOR gate in each of the three new GaAs gate arrays has a worst-case delay of 60 ps unloaded and dissipates 0.18 mW, resulting in a speed-power product of 11 fJ, significantly better than silicon BiCMOS, according to Vitesse.

*—Barbara Tuck Egan*

## NEC partners with CrossCheck for ASIC test methodology

With NEC Tokyo having agreed to license the CrossCheck Technology (San Jose, CA) ASIC test and diagnostic methodology, CrossCheck's ASIC partners now represent more than 50 percent of the worldwide CMOS gate array market, according to the *ICE ASIC Outlook 1992 Report*. In securing rights to CrossCheck's patented on-chip test electronics and its fault simula-

*Continued on page 8*

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|---|---|---|---|
| Buffers | 4.1ns | 5.8ns | 5.2ns |
| Transceivers | 4.1ns | 5.8ns | 4.8ns |
| Registers | 5.2ns | 5.5ns | 5.0ns |
| Latches | 4.2ns | 5.5ns | 5.0ns |

## Free Logic Design Kit

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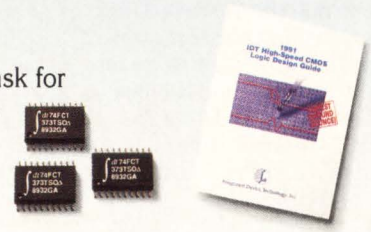

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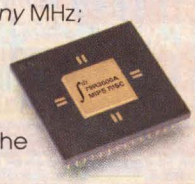

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CIRCLE NO. 4

*Continued from page 6*

tion, automatic test pattern generation and device diagnostics software, NEC joins Fujitsu, Harris, LSI Logic, Oki, Raytheon, and Sony as CrossCheck partners. NEC will implement the CrossCheck test methodology in its new CMOS gate array family, to be introduced this year.

Recent benchmark data from the Raytheon Advanced Device Center, which acted as a test site for CrossCheck's latest software tool, CX-Probe, shows that CX-Probe used CrossCheck's on-chip test structures to isolate and identify functional failures in five ASICs (11,100 gates) in 16 hours compared to the conventional diagnosis time, using an electron beam prober, of seven to 10 days.

*—Barbara Tuck Egan*

## Cadence/Valid merger gets the nod

The proposed merger between Cadence Design Systems (San Jose, CA) and Valid Logic Systems (San Jose, CA) was recently approved by shareholders of both companies, making the deal official and the EDA market smaller. The combined company will operate under the Cadence name, with Joseph Costello, founder of Cadence, serving as president and CEO, while George Klaus, Valid's current president, will become executive vice-president and COO. Additional organizational changes and staff cuts will be announced in the next few weeks, while product information will be released over the next few months.

Customers of both companies are particularly interested in which of the overlapping products from each company will get the axe, though spokespeople for Cadence are assuring the nervous design community that support will be available for all products during the transition.

*—Mike Donlin*

## Workstation wars still raging

Hewlett-Packard (Palo Alto, CA) is expected to roll out an under-$10,000 workstation with nearly twice the throughput of similarly priced systems from rivals Digital Equipment Corp (Maynard, MA) and Sun Microsystems (Mountain View, CA). The workstation, code-named Bushmaster, reportedly performs at a clip of 50 Mips and 35 to 40 Specmarks and will sell for $7,000 to $8,000.

HP will keep the pressure on in the competitive workstation market with a system due out by midyear that's rumored to perform at more than 100 Specmarks.

*—Mike Donlin*

## Moto going superscalar

Motorola's computer group is expected to announce this month it will market a family of single-board computers based on the company's 88110 superscalar processor. The first product, expected soon, will be a VME board that supports SCSI 2, multiple users, networking, and VSB (VME subsystem bus).

It's expected the new board will be the next generation of the MVME187, the attempt by Motorola to see if it can use the 147 approach to make a successful RISC machine. The new board is said to have three to five times the performance of the 88100-based product, "which is expected to make the symmetric superscalar SBC well suited for the most demanding application," says Motorola Computer Group vice-president, Tom Beaver.

*—Warren Andrews*

## Lynx picked as real-time leader

At least two analyst groups—the Gartner and Yankee Groups—have come to the conclusion that LynxOS is positioned to take advantage of what they described as an "explosion of new CIE [Computer Integrated Engineering] products." Says the Gartner Group, "Users and software developers indicate that it [LynxOS] is one of the fastest, if not the fastest, Unix or Unix-compatible real-time systems available." The studies go on to describe how real-time flavors of Unix will make it possible to manage "both the real-time process control and the event-based data of MIS."

According to the Yankee Group, there will be a 30 percent annual growth rate in shipments of real-time operating systems for the industrial market and it's predicted that the availability of real-time Unix systems such as LynxOS "could break down the barriers that have long hampered data transfer between different vendors serving the process-control and MIS sides." In its report the Yankee Group stated, "Sun [Microsystems] and HP have the most to gain from the movement toward Posix standards, while DEC has the most to lose because of its proprietary software and hardware." The Yankee Group's statement is hard to document, especially considering DEC's recent move toward developing Posix-compliant VAXeln and DECelx.

*—Warren Andrews*

## ISI offers first distributed real-time Unix

The Software Components Group of Integrated Systems (Santa Clara,CA) has unveiled what it claims to be the first distributed real-time Unix for embedded systems. The product, which will be called Aria, is based on the microkernel technology developed by Chorus Systems (Paris, France). Aria is targeted at distributed control engineering, communications and automation applications. ISI is tracking the Posix P1003.1 general portability standards as well as the yet-to-be-finalized 1003.4 real-time extensions. In addition, the distributed nature of Aria makes it necessary to track and eventually comply with the 1003.4a multithreaded standards.

The initial version of Aria will be offered for the Motorola 68030-based MVME147S series of single-board computers, with other versions to follow. According to ISI, the initial version has been certified Unix SVR3.2-compatible and will shortly be followed by an SVR4 version. *—Tom Williams*

# *VME ala Card*

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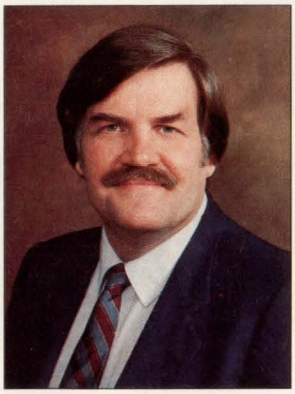
CIRCLE NO. 6

# Cryptic Cover Contest rules

***When 100 readers write you about anything, you can count on thousands who are just as interested but don't write.***



**John C. Miklosz**
**Associate Publisher/**
**Editor-in-Chief**

Wow! We discovered last month just how much *Computer Design* readers like our unorthodox covers, and how much they love contests! From time to time in the past, we've embedded some symbolism or a hidden message in a cover primarily for our own amusement. Our little diversions didn't go completely unnoticed and we would frequently receive unsolicited comments. How much the majority of readers were interested in our covers, however, we couldn't tell without running a test. The December cover was that test and we were delighted with the response and the comments we received.

By the time we closed the January issue, we had received about 60 letters deciphering the rebus writing on our "Indiana Jones and the Last Crusade" cover. We published the names of those who guessed correctly, along with some of their general comments about *Computer Design*, on pages 141-142 in a section entitled "Letters, covers & other diversions." Since then, we received additional responses and the total at the time this editorial is being written is something over 100. Now, 100 reader responses for a publication with a circulation of over 100,000 might not seem like a lot, but I've been in the publishing business long enough to know that when 100 readers write you about *anything*, you can count on thousands who are just as interested but don't write because they're extra busy, forget or, with a contest, don't think they'll ever win. With that said, do you think we can resist a gimmick that's fun for us, we think will be fun for you, and that will get you to look, not only at the cover, but at the Special Report that's tied to the cover illustration? No way!

So, here are the official rules for the monthly *Computer Design* Cryptic Cover Contest:

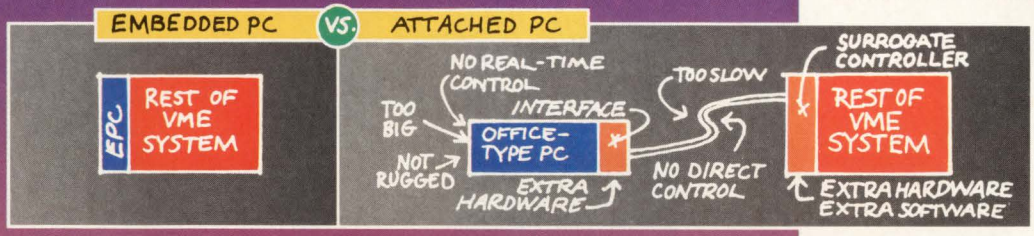
Each month, the cover will contain some rebus writing, a coded message (we haven't done this yet), or some symbolism or metaphorical images related to the contents of the Special Report. This month, for example, the elements comprising the cover illustration represent various terminology or buzzwords related to multiprocessing. To qualify for the prize, you must decode the rebus writing or coded messages, or explain the symbolism or metaphors.

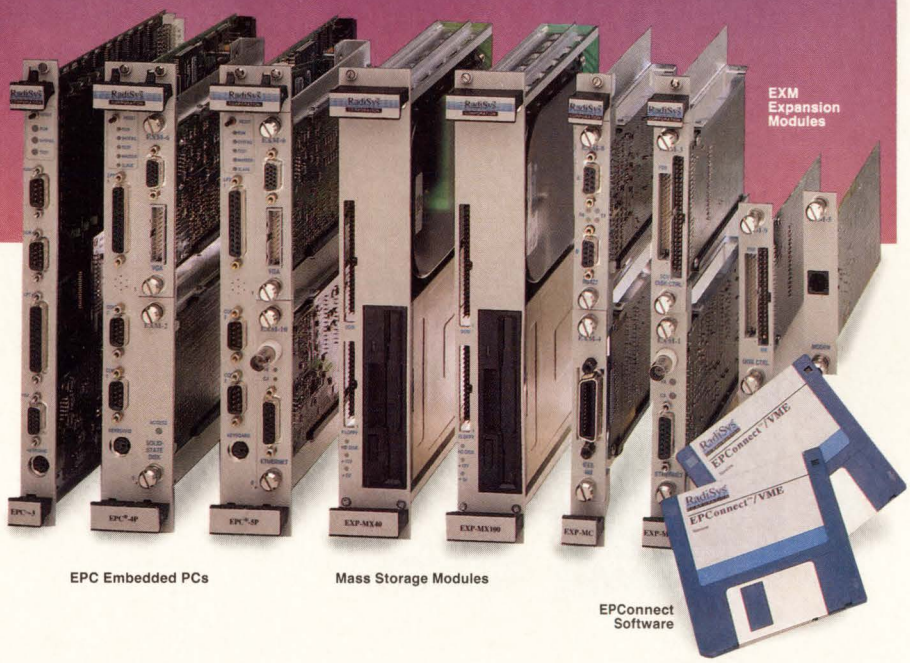
Responses will be accepted until the end of the issue month (e.g., until the end of February for this issue) and the prize winner will be randomly chosen from all correct responses received by that time.

The explanation of the cover will be published two months after the issue (e.g., this month's cover will be explained in the April issue), along with the names of all those who responded correctly. Everyone who succeeds in the decipherment will receive a certificate identifying them as a Wizard of the Cryptic Cover.

As to the prize. We *still* haven't figured that out (too busy dreaming up this month's cover, among other things). We've been playing with the idea of software, a gift certificate to Brookstone, Nordstrom's, or Victoria's Secrets, or whatever. We'd appreciate any suggestions along with your entries. Good luck.

# RADISYS GIVES VME THE INSIDE ADVANTAGE

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| **Processor Modules:** | | | | |
| CPU | 80386 | 80386SX | 80386 | 80486 |
| CPU Clock | 16 or 20MHz | 16MHz | 25 MHz | 25 or 33 MHz |
| DRAM | 1 or 4 MBytes | 1, 2 or 4 MBytes | 4, 8 or 16MBytes | 4, 8 or 16 MBytes |
| Graphics | EGA (640 x 350) | VGA (800 x 600) | VGA (800 x 600) | VGA (800 x 600) |
| **Mass Storage Modules:** | | | | |
| Hard Disk Capacity | 40 MBytes | 40, 100 or 200 MBytes | | |
| Floppy Drive Size/Cap. | 3.5" / 1.44 MBytes | 3.5" / 1.44 MBytes | | |
| **Expansion Capabilities:** | | | | |
| PC Add-in Cards | Yes | Yes | | |
| EXMbus Expansion | N/A | EXM Expansion Modules: | | |
| | | EXM-1 Ethernet | EXM-5 Modem | EXM-9 IDE/Floppy Ctrl. |
| | | EXM-2 Solid State Disk | EXM-6 VGA Graphics | EXM-10 Ethernet |
| | | EXM-3 SCSI/Floppy Ctrl. | EXM-7 RS232 Serial I/O | EXM-11 Timer/Counter |
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CIRCLE NO. 7

# The 29K Family.


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# The 29K Family.


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So call AMD at **1-800-292-9263 Ext. 3** for information on the 29K Family, or a Fusion29K product catalog or newsletter. You'll find all the support you need in one big happy family.

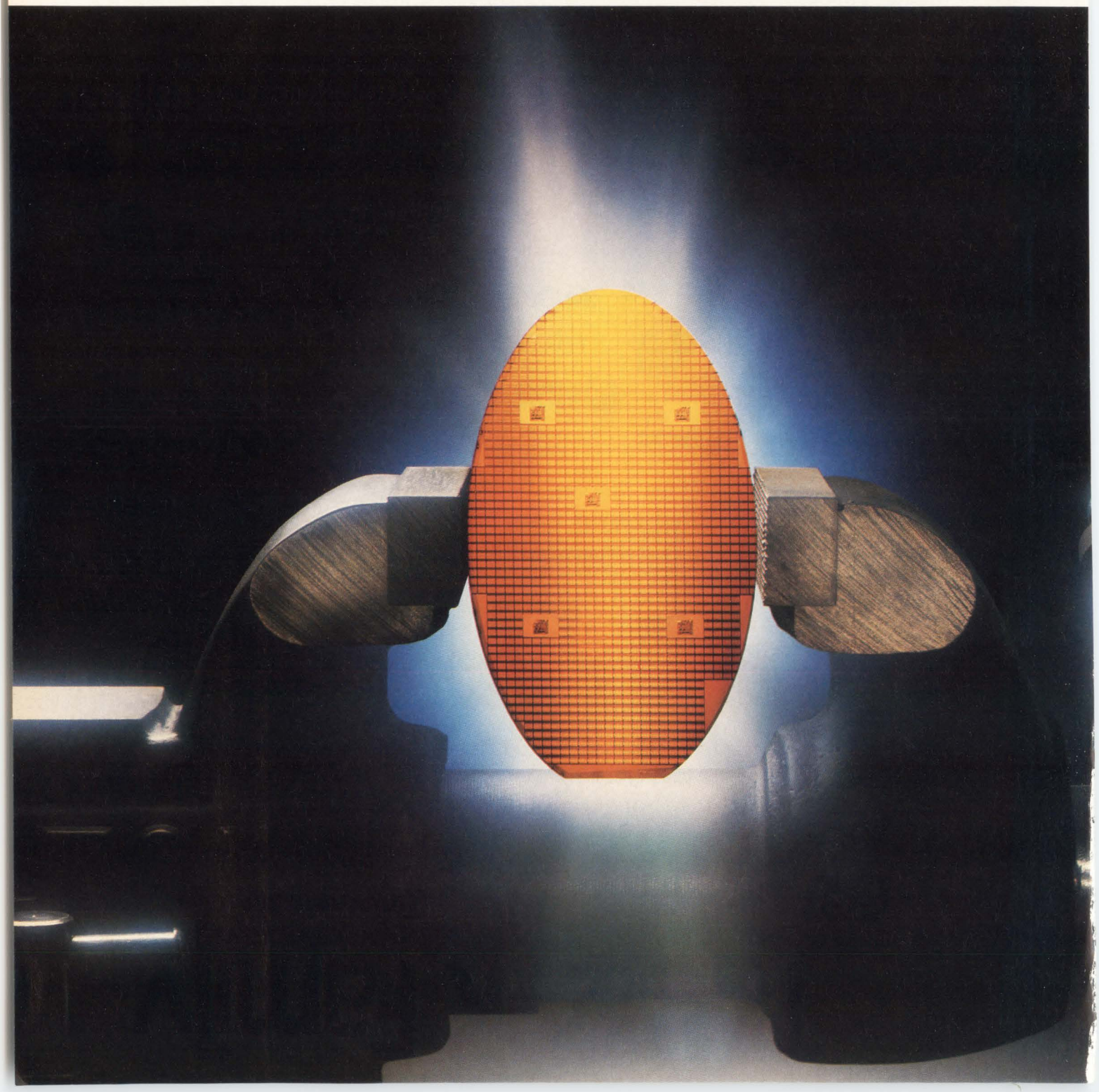
**Advanced Micro Devices**



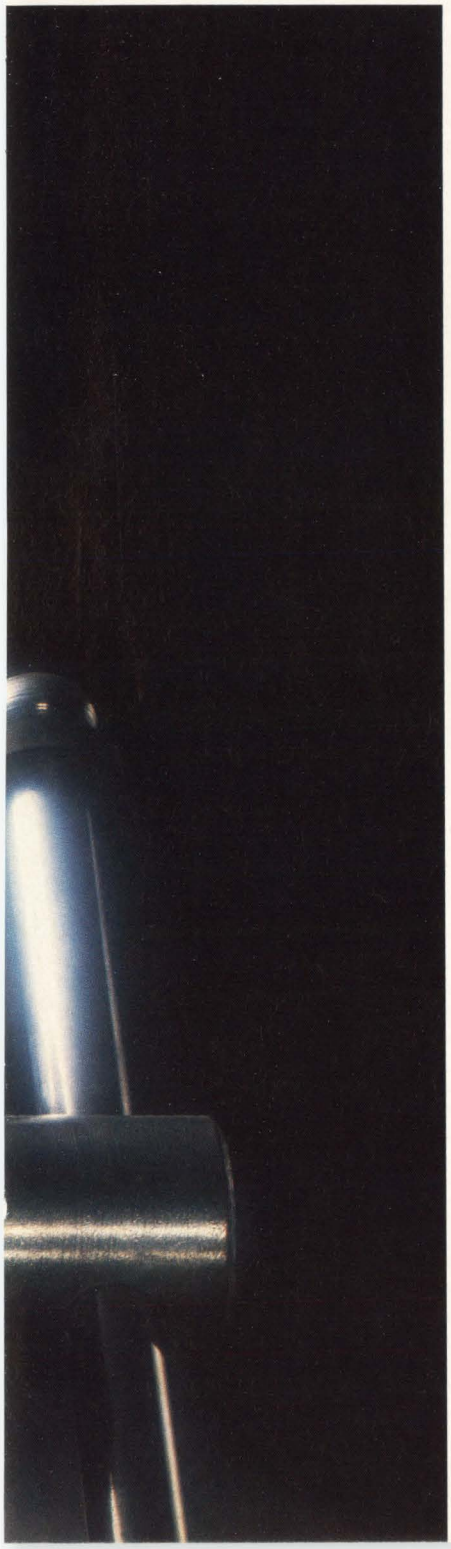
**CIRCLE NO. 8**

IN THE ERA OF MegaChip™ TECHNOLOGIES

# We've squeezed more ABT Widebus as fast



# speed from our logic. as 4.1 ns!



With our new Advanced BiCMOS interface logic (ABT) family, you get the speed, drive and low power you need to optimize the performance of processors operating at 33 MHz and above.

Fabricated in our 0.8-micron BiCMOS process, this new family delivers maximum speeds down to 4.1 ns over recommended operating conditions. Typical performance of the devices is in the 2.5- to 3.0-ns range.

Other critical performance parameters are as impressive. Drive capability is 32 to 64 mA. Static power consumption is typically 2 mA ($I_{CCH}$, $I_{CCZ}$) and 30 mA ($I_{CCL}$). Ground bounce is less than 800 mV typ.

## All this in Widebus

Our ABT family, a second-generation advance of our leadership BiCMOS (BCT) family, includes versions of our 16-, 18- and 20-bit-width Widebus™ functions.

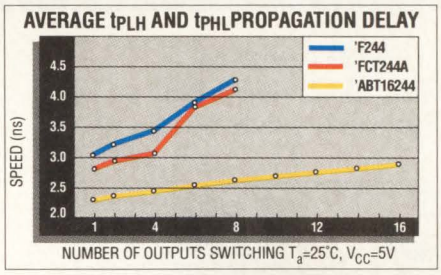
Among the many ABT Widebus functions released is the 'ABT16244, a 16-bit buffer and line driver. It exhibits much greater stability of propagation delay *(see chart)*, which results in a lower derating factor across the number of outputs switched.

Also in volume production are the Widebus 'ABT16245 16-bit bidirectional bus transceiver and the 'ABT16543 and 'ABT16952 16-bit bidirectional registered bus transceivers.

As in our successful Advanced CMOS Logic (ACL) Widebus family, these devices come in our leadership surface-mount shrink small-outline package (SSOP) that gives you twice the number of I/Os as a standard small-outline package in the same space.

## Unique additions included

There are also new devices in our ABT Widebus family featuring greater density and functionality. Our 'ABT16500A is a good example. An 18-bit registered transceiver, it combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

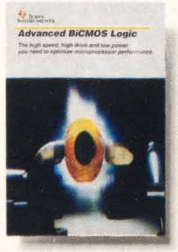



***TI's speed advantage:*** *In a one-to-one comparison, a TI 'ABT16244 16-bit Advanced BiCMOS driver proves to be much faster and more stable than Advanced Bipolar and standard CMOS octal drivers.*

To complement our full line of Widebus products, our ABT family will include at least 39 octal buffers/drivers, flip-flops, transceivers and registered transceivers.

## Squeeze more out of your system with a free sample 'ABT16500A: Call 1-800-336-5236, ext. 3009

To learn firsthand how our new ABT family can boost the performance of your bus-interface designs, get a free 'ABT16500A transceiver and data sheet. Just complete and mail the return card or call the number above.

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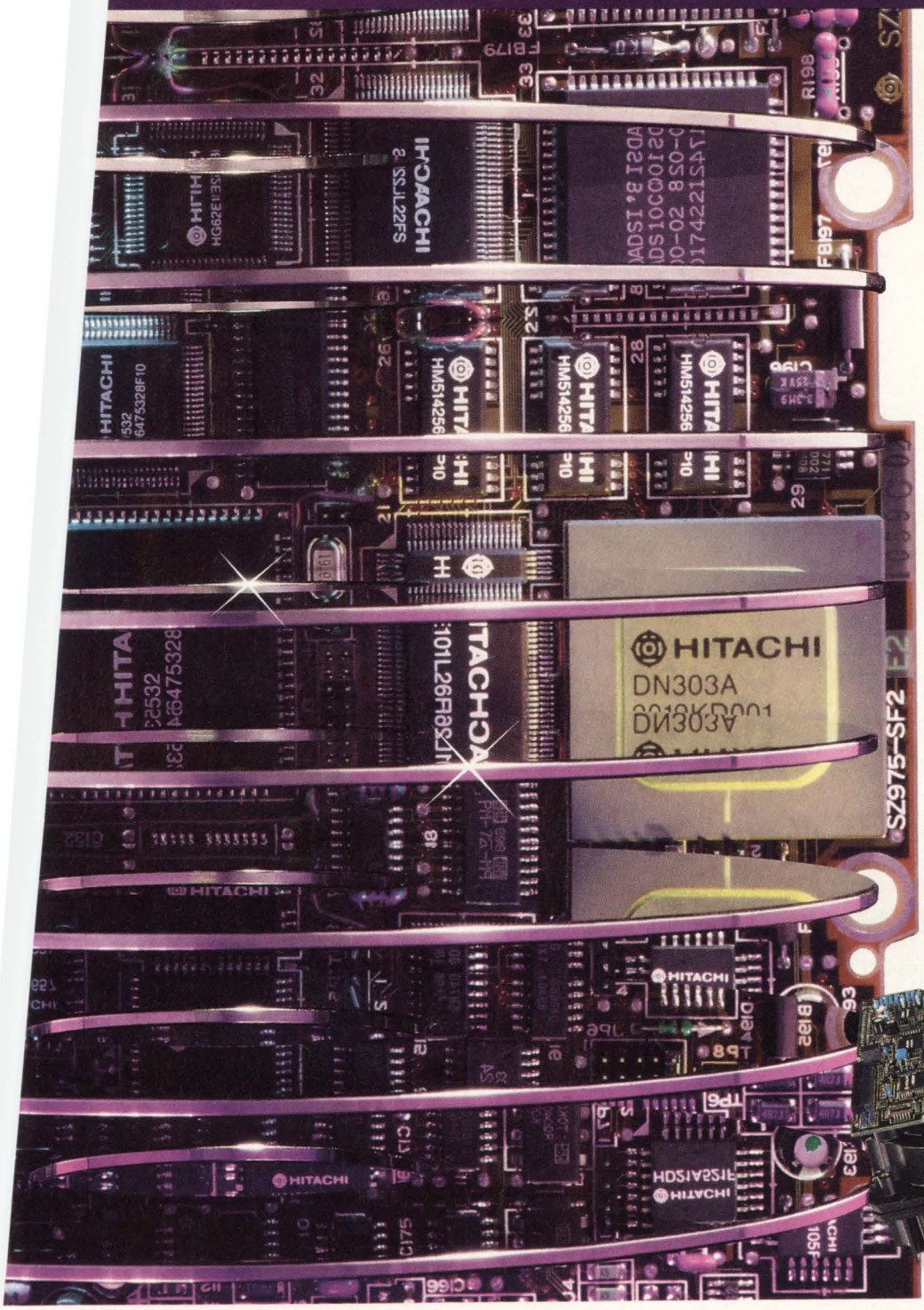


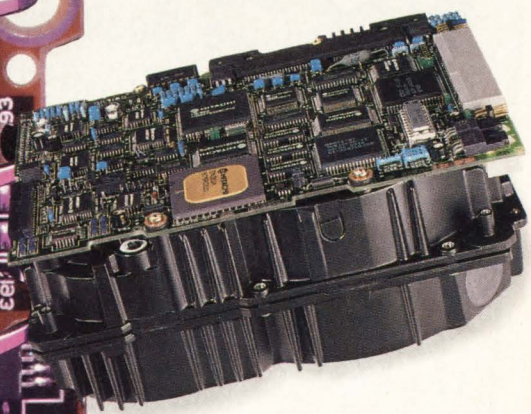

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CIRCLE NO. 12

## CALENDAR

### CONFERENCES

***February 11 - 14***
***MICAD '92***

MICAD 1992

Port de Versailles, Paris, France. France's premiere CAD-CAM event will celebrate its 11th anniversary by welcoming more than 250 exhibitors and 25,000 visitors to Port de Versailles. MICAD has become one of the leading computer graphics conferences and exhibitions in the world. It's the European showcase for introducing new products and technology. Contact: The World Computer Graphics Association, 2033 M St NW, Suite 399, Washington, DC 20036-8446, (202) 775-9556, Fax (202) 775-8122. **Circle 366**

***February 18 - 20***
***SysComp/92 West***

SysComp

San Jose Convention Center, San Jose, CA. The only OEM system/subsystem components conference and exposition. The technical program will cover microprocessor, system and bus architectures, power sources, display and interface technologies, mass storage, and new developments in media, embedded software programming, system packaging, concurrent engineering and achieving cost, quality and time-to-market goals. The exhibition will feature vendors of OEM computers, ICs, board-level products, power sources, mass storage, displays, backplanes, enclosures, and much more. Contact: Paul LaGris, 3432 Timberlake, Costa Mesa, CA 92626, (714) 966-1526, Fax (714) 241-1108. **Circle 367**

***February 18 - 20***
***RISC '92***

RISC '92

Le Baron Hotel/San Jose Convention Center, San Jose, CA. To be held in conjunction with SysComp/92 West, RISC '92 will be the foremost gathering of designers and design managers involved with RISC architectures, systems, programming, and applications. A combination of lectures, tutorials and panel discussions will cover areas such as RISC-based multiprocessing systems; fundamentals of Sparc, MIPS R3000/4000 and other architectures; advances in RISC-based CPU boards for standard buses; RISC in multimedia applications; compilers and software development tools; and many more topics. Contact: Paul LaGris, 3432 Timberlake, Costa Mesa, CA 92626, (714) 966-1526, Fax (714) 241-1108. **Circle 368**

***February 24 - 27***
***International Control Engineering Exposition***

INTERNATIONAL CONTROL ENGINEERING EXPOSITION & CONFERENCE

McCormick Place North, Chicago, IL. The ICEE is specifically aimed at control engineering, with a focus on innovative and useful applications of control, instrumentation and automation systems in the discrete parts and processing industries. Conference topics include: expert systems and neural networks in real-time control; developments in distributed control system architectures; control systems for management—competing with time; next-generation controllers; and customizing control systems. Also, an exhibition will feature programmable controllers, sensors, control soft-

## CALENDAR

### CONFERENCES

ware, process control systems, and industrial computers. Contact: Cahners Exposition Group, 999 Summer St, PO Box 3833, Stamford, CT 06905-0833, (203) 964-0000, Fax (203) 964-8489. **Circle 369**

***February 25 - 27***
***NEPCON WEST '92***

Anaheim Marriott, Anaheim Hilton and Anaheim Convention Center, Anaheim, CA. The 30th annual National Electronic Packaging and Production Conference and Exhibition is the only show in the electronics manufacturing industry to span all areas of concurrent engineering from design through final testing of printed circuit boards. There will be 117 conference sessions and more than 1,000 exhibitors will display the latest in products and technology for design, fabrication, assembly, packaging, inspection, and test of printed circuits and electronic assemblies. This year's theme is "The New World of Electronics Manufacturing." Contact: Cahners Exposition Group, 1350 E Touhy Ave, Des Plaines, IL 60017-5060, (708) 299-9311, Fax (708) 635-1571. **Circle 370**

***March 10 - 12***
***SEMICON/Europa 92***

Zuspa Convention Centre, Zurich, Switzerland. SEMICON/Europa is the largest trade show in Europe dedicated to the newest products and equipment in semiconductor processing and materials. Semiconductor Equipment and Materials International (SEMI) will hold standards meetings March 9 - 12. More than 600 companies will be displaying new technologies. There will be five technical conference themes: "Process tool integration," "Manufacturing science," "Quality requirements for media and supply systems," "Process monitoring," and "The face of European test applications in the 1990s." Contact: SEMI North America, 805 E Middlefield Rd, Mountain View, CA 94043-4080, (415) 964-5111, Fax (415) 967-5375, or SEMI Europa, Avenue de Cortenberg, 79, B-1040 Brussels, Belgium, 32-2-736-2058, Fax 32-2-734-0622. **Circle 371**

***March 10 - 12***
***Southcon/92***

Orange County Convention/Civic Center, Orlando, FL. This important electronics conference and exhibition in the Southeast brings together design, test, manufacturing, and telesystems in one show. More than 300 exhibitors will feature the latest networking and data communications products; semiconductors; electronic design automation tools; test and measurement instruments; and passive components. Technical sessions and tutorials will include such topics as high-speed data communications, computer imaging and real-world applications of neural networks. Contact: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045, (800) 877-2668, Fax (213) 641-5117. **Circle 372**

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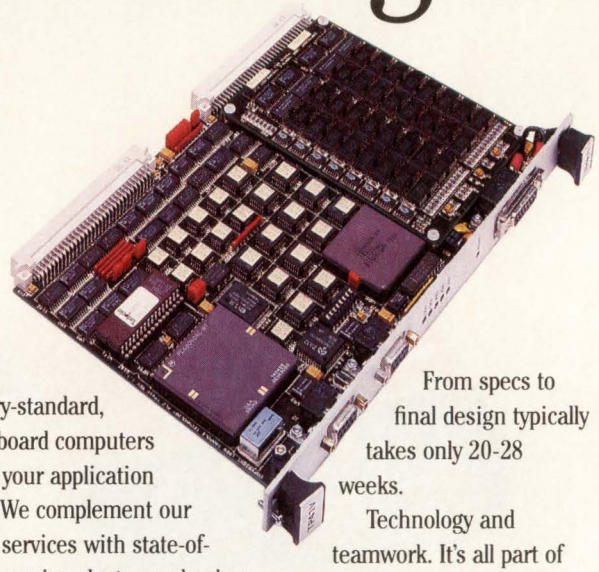

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T A D P O L E

CIRCLE NO. 19

# Sven Behrendt on: VME's 10th birthday

VME recently celebrated its tenth birthday. Whom do we congratulate at the birthday party—the child or its parent? I tend to congratulate the parents first, since they are the creators. The companies that created VME have much to be proud of, especially the manner in which they have conducted themselves as colleagues and competitors.

What do we do next at a birthday party, after respects have been paid to parent and child? We tend to reflect on the person's past and look forward to the future. Like loving but realistic parents, while we applaud our child's beauty and brilliance, we must also acknowledge his or her limitations.

## The success of a standard

VME, originally the brainchild of Motorola and created to help promulgate its 68000 family of processors, started as a European standard. In an unusual development, the European drivers of the technology, such as Force, Motorola and Thomson, brought the technology to the U.S. instead of the other way around, and a European standard spread to the U.S. and beyond. VME is now a worldwide standard.

The reason for VME's success is that it beautifully meets real-time and embedded application needs where high performance is required. Profound and logical extensions to the VMEbus are taking place, ensuring VME's longevity over the next decade. We have already seen a significant throughput increase in the development of VME64/Plus, including SSBLT. Other key developments will continue to appear.

Time is on our side. Customers are requiring ever more solutions to which they can add value. Increasingly, they will be buying "off-the-shelf" solutions and adding their own software. The value added by the integrator will shrink from today's 70 percent to about 50 percent in 10 years. This is because time-to-market is so critical. System vendors will buy base-level technology rather than developing it in-house, as has historically been the tendency.

*Sven Behrendt is chairman of Force Computers, Campbell, CA and Munich, Germany*

VME vendors won't be pressured by competition from Japan, Korea and Taiwan. This is both good and bad news. On the one hand, we won't be fighting the fiercely competitive economic wars that others have had to wage with Asia. On the other hand, the lack of competition from Asia is due to VME's limited market, predicted to peak at about $1 billion. The Asians are looking for bigger, higher-growth markets. On the high end, VME is squeezed by Futurebus+, and on the low end, by PC technology.

Nonetheless, between these two pressure points VME has a secure position. It will continue to be a cost-effective alternative to minicomputers in real-time or embedded applications—a $20,000 solution to a $200,000 minicomputer application.

## The impact of Futurebus+

VME is a 5-V TTL technology. Despite innovations, TTL technology is stretched to the limits of its capabilities by the latest generation of high-speed microprocessors. Futurebus+, a 3-V BTL technology, takes over where VME leaves off, providing a very high bus speed to complement higher microprocessor speeds.

Although I have said that VME will be squeezed at the high end by Futurebus+, Futurebus+ technology is in no way a threat to VME. Futurebus+ is a system architecture that addresses a market that VME can't address. Applications where high availability (downtime is unacceptable) and very high data throughput are critical, such as telecommunications, are ideal for Futurebus+. Additional characteristics such as microprocessor and software independence make Futurebus+ a prime candidate for open system architecture in workstations, mainframes and minis.

This means Futurebus+, unlike VME, has a much

larger market. The Japanese, with their nose for growth markets, are currently developing mainframes, minis and workstations based on Futurebus+. With companies such as AT&T, Digital Equipment Corp., Ericsson, Fujitsu, Hitachi, NEC, and OKI and applying their huge resources to Futurebus+ system development, there's little doubt that the stage is being set for a worldwide battle.

VME, while not part of this battle, will face other challenges.

## Challenges

The increasing tendency of VME system integrators to demand more integrated solutions from VME vendors poses new challenges. The cost of research and development will increase about 15 percent over the next decade. Whereas VME began with the 68000, it now supports several additional families of microprocessors, including Sparc, 88000 and R6000. This requires additional investment in software development tools, internal software development and support.

The industry is also investing heavily in advanced manufacturing techniques such as SMT, TAB and multichip modules. Changes in manufacturing technologies have been matched by changes in manufacturing systems. Kitting, subcontract assembly and just-in-time manufacturing require new knowhow to implement these processes effectively.

Much of the investment mentioned above is due to higher standards of quality. This is the price of being a player in a game where a third of the world market—Western Europe—is now demanding ISO 9001 compliance, and another third of the market—Japan—has already set stringent quality standards. Of course, in the long term, high product quality will pay for itself in product savings.

There will continue to be no real-time software standard, and multiple real-time software vendors. VME developers must invest appropriately in staff, development environments and support to provide the value-added demanded by the market.

As a niche technology, VME will never enjoy the reduced per-unit sales cost of a commodity product like the PC. VME will continue to be sold through direct sales forces and manufacturer's representatives. These intensive channels will only increase in cost, which means that manufacturers must keep other costs in line to remain competitive.

Finally, VME faces the challenge of connectivity, an issue that the industry has never really resolved. VME must find more satisfactory solutions for bus-to-bus and bus-to-busless connectivity applications than communication through the VME backplane or over Ethernet provide. There are many busless applications to which VME could make a contribution. Ethernet doesn't have the bandwidth for adequate chassis-to-chassis data transfer. A solution must be found to enable VME technology to make its maximum contribution to the needs of the market.

Despite the challenges outlined above, VME is looking forward to another successful decade. The past 10 years were successful because VME companies worked together as a community, and not as lone wolves looking for the easiest kill. It's this close cooperation that will provide the technical solutions required and allow VME to continue to satisfy its particular market niche.

Like most children, VME is brilliant in specific areas. And like most children, VME is not perfect in all areas. It's the job of VME vendors in the next decade to assure that our brainchild reaches its full potential.

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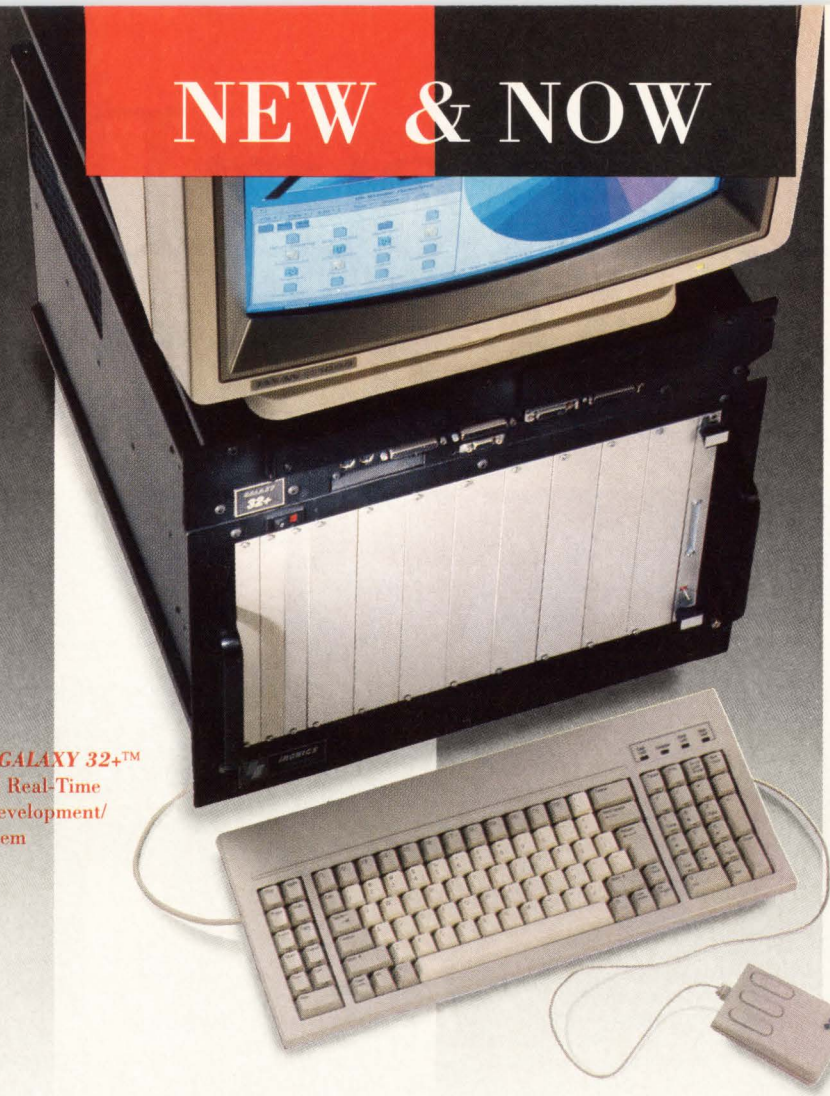

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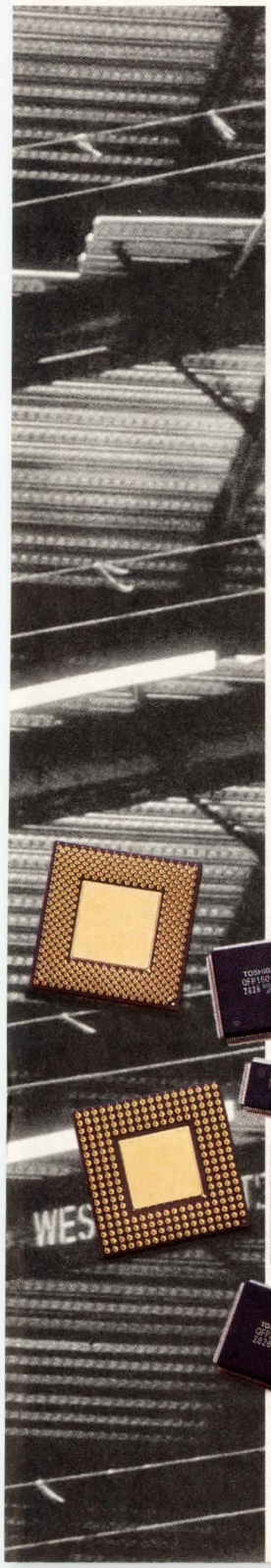


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CIRCLE NO. 20

ASICs & ASIC DESIGN TOOLS

# One-upmanship in competitive FPGA contest

*Barbara Tuck Egan, Senior Editor*

Vendors of complex PLDs and FPGAs have been intensifying their efforts in a hotly contested battle to capture some of the thousands of gate array design wins. Veteran vendors and start-ups alike have been leapfrogging one another with FPGA announcements, with almost every one of them claiming to have the densest, fastest and highest-I/O parts.

The SRAM-based 0.8-µm CMOS CLi6000 FPGA architecture, announced a few weeks ago by start-up Concurrent Logic (Sunnyvale, CA), has thousands of registers—eight to 10 times more than Actel, Altera or Xilinx products, says marketing director Joel Rosenberg. The medium-grained architecture is ideal for pipelined and compute-intensive applications according to Concurrent.

## Symmetrical arrays

Density of the CLi6000 family will range from 1,200 to 10,000 gates, with anywhere from 50 to 100 percent utilization for register-intensive designs. The first of the symmetrical arrays, the 132-pin, 5,000-gate CLi6005, is sampling now, with production quantities expected in April. The product has 3,136 cells (and so a maximum of 3,136 registers) and 108 I/O pads, and it can accommodate system speeds up to 70 MHz, claims Concurrent. Because of the architecture's granularity, Rosenberg says Concurrent has the ability to proliferate I/Os in the future.

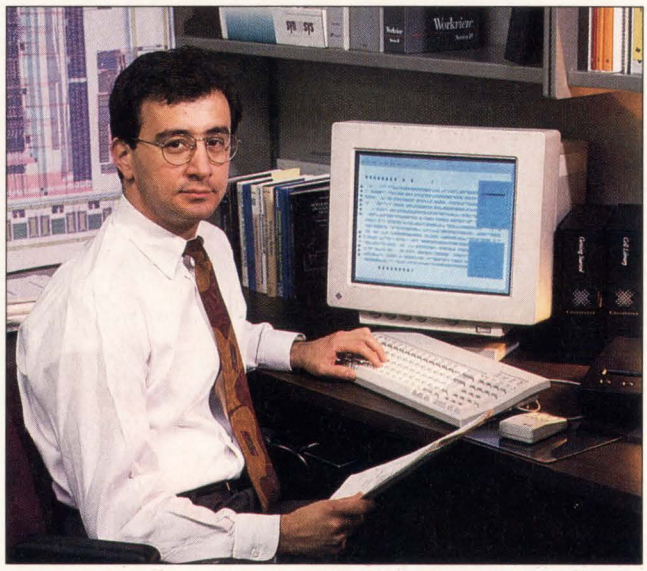
Concurrent is counting on its timing analysis tools to differentiate its FPGAs in the marketplace. President Ed Browder says, "We have been able to overcome many of the limitations of existing FPGAs and their associated design tools. Timing analysis has been largely ignored by FPGA design software." Since actual wire lengths and loading delays are used to calculate the timing of Concurrent's parts, post-layout simulations accurately predict real-world performance, claims Browder. CLi6000 designers can use Viewlogic for schematic capture and simulation.

## Gate array replacements

Like Concurrent Logic, Crosspoint Solutions (Santa Clara, CA) is attempting to break into the FPGA market, claiming its antifuse-based, 0.75-µm CMOS CP20K devices are the first FPGAs to have gate-level granularity and compatibility with masked gate arrays. Crosspoint expects samples of its 4,245-gate CP20420 to be available this month. The company claims to be 50 to 100 percent faster than veteran FPGA players, with toggle rates to 150 MHz and counters operating to 90 MHz, according to preliminary information. "Crosspoint's transistor-level granularity," explains director of marketing Vacit Arat, "provides users the facility to fine-tune logic and create faster paths." Crosspoint is the first company that actually deserves to be called an FPGA vendor, Arat says, because its FPGA design granularity is the first to be equivalent to a gate array. "We'll distinguish ourselves by fitting perfectly into the present ASIC design methodology," he claims. Crosspoint supports third-party tool vendors with kits for front-end design and offers its own placement and routing tools.

The CP20K series will range from 2,200 to 20,000 gates, with utilization between 60 and 80 percent and with 91 to 270 I/O pads. The 155-pin CP20420 has 130 I/Os. Crosspoint plans to have a 12,000-gate device by midyear and a 20,000-gate device by year's end. Like Actel and QuickLogic, Crosspoint is basing its FPGAs on antifuse technology.

When programmed, the resistance of the antifuse is about 100 Ω. Since the fuse adds less than 1 pF of capacitance, the resistance-capacitance (RC) delay in the signal path is very small, permitting the FPGAs to operate at fairly high frequencies. "We're similar to QuickLogic in terms of on-resistance and capacitance, making our RC constant the same as QuickLogic's and one-thirtieth of Actel's," says Arat.



*Crosspoint's Vacit Arat says his company is acutally the first that deserves to be called an FPGA vendor—because Crosspoint's FPGA design granularity is the first to be equivalent to a gate array.*

## Accurate delay models

Still in a start-up mode itself, QuickLogic (Santa Clara, CA) recently announced that by optimizing the programming sequence of ViaLink interconnects in the most heavily loaded nets of its pASIC (programmable ASIC) devices, it has reduced the resistance of those links to less than 50 Ω, boosting overall device speed by as much as 25 percent. To achieve this speed enhancement, QuickLogic is using a technology called asymptotic waveform evaluation (AWE), which uses moment-matching approximations to more efficiently evaluate the delays caused by distributed resistance and capacitance.

QuickLogic has integrated an AWE technology-based timing analysis package into Release 2.0 of its pASIC Toolkit, claiming the tech-

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**CIRCLE NO. 21**

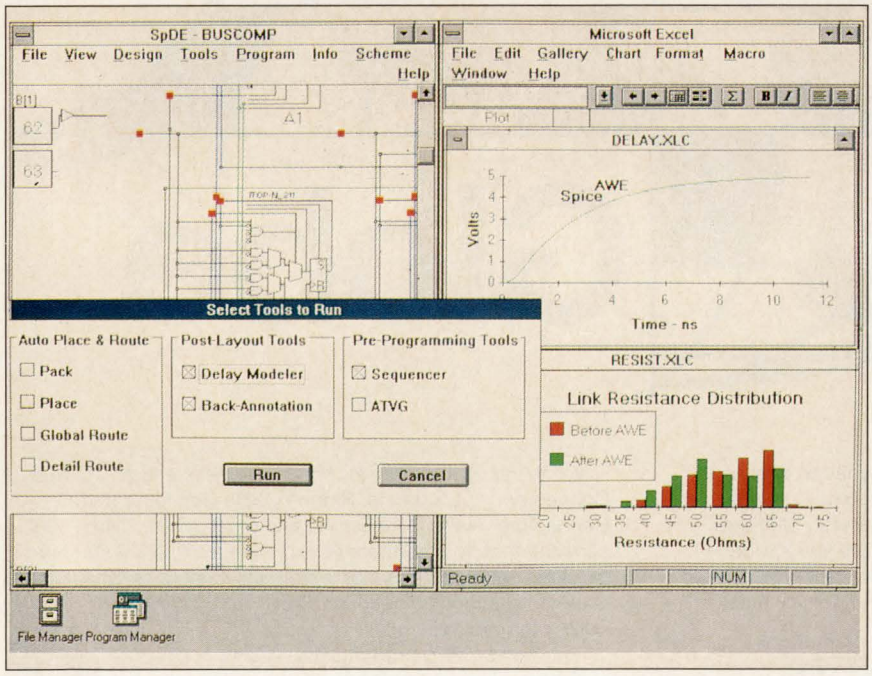
## ASICs & ASIC DESIGN TOOLS

nology is completely transparent to the user. Whereas traditional RC tree models describe FPGA circuit interconnects to a first-order approximation, AWE technology extends those techniques to an $n^{th}$ order level, according to the company. AWE-based timing analysis will also give designers the most accurate timing models possible for the back-annotation of delay information into the timing simulator, according to president and CEO David Laws. "AWE technology makes possible very accurate delay models so that simulators can give very accurate answers," he points out.

Though Laws claims pASIC technology can accommodate more gates on a given die size than any other, QuickLogic is sticking to modest-sized arrays because that's what designers want. The next pASIC to be announced will double the density of QuickLogic's 1,000-gate part. "Our 2,000-gate pASIC will be equivalent to a 6,000-gate part from Xilinx or Actel," Laws adds.

As newcomers struggle to make their presence felt in the market, veterans Xilinx, Actel and Altera are enhancing architectures and increasing speed to protect their own hard-earned positions. Less than two weeks ago, Actel (Sunnyvale, CA) disclosed preliminary details of its ACT 3 family, while Altera (San Jose, CA) announced it was sampling the first two MAX 7000 members. (See "Max 7000 family faster, denser, more flexible than MAX 5000 parts," p 118.)

Fabricated using Hewlett-Packard's 0.8-µm CMOS process, Actel's PLICE-antifuse-based ACT 3 family will range in density from 1,000 to more than 10,000 gates, with up to 95 percent module utilization. Pin count will exceed 200, and 16-bit counters will operate in excess of 125 MHz, Actel claims. ACT 3 parts will have an I/O circuit that will produce a 10-ns clock-to-Q time to let designers get signals on and off chip quickly, according to the manufacturer.




*QuickLogic's pASIC Toolkit Release 2.0, with asymptotic waveform evaluation (AWE) technology, programs FPGA interconnects that comprise critical nets (highlighted by red squares in the physical layout schematic on the left) to a value less than 50 Ω. QuickLogic claims that the application of AWE to pASIC designs increases speed by as much as 25 percent. The Excel spreadsheet on the right illustrates the result of the AWE technique applied to delay modeling and resistance distribution. The first chart shows that, while AWE simulations execute in the short run time associated with RC tree models, they also provide the accuracy associated with Spice simulations. The second chart illustrates the distribution of link resistance values for a programmed QL8X12 FPGA, both before and after AWE was applied. With the application of AWE technology, the peak of the distribution moved from 65 to 50 Ω.*

### To the Max

The denser of Altera's MAX 7000 pair being sampled is the EPROM-based, 256-macrocell, 10,000-gate EPM7256 erasable programmable logic device (EPLD), fabricated in Cypress Semiconductor's 0.8-µm CMOS process. The 192-pin device has 164 I/Os and operates at 70 MHz in-system, Altera claims. With the 44-pin, 32-macrocell EPM7032, the company's first EPLD manufactured using EEPROM technology, Altera is expanding MAX technology to include EEPROM implementations. MAX 7000 family members will range from 4,000 to 40,000 gates, with 50 percent utilization. Maximum pin count will be 288. Altera claims that MAX parts will have the advantage in speed, density and pin count throughout this year.

In the meantime, market leader Xilinx (San Jose, CA) announced a new speed grade for its XC4000 FPGAs. Made possible by an advanced 0.8-µm CMOS process, this new speed grade has reduced internal logic block delays to 4.5 ns, input delays to 3 ns and output delays to 7 ns, Xilinx claims. Memory access time for on-chip SRAM is 4.5 ns.

How can you evaluate all these claims? Since silicon can't always accommodate the functionality and speed trumpeted by FPGA vendors, make yours an educated choice. Be as informed of other users' experiences as you are of vendor's promises. ■

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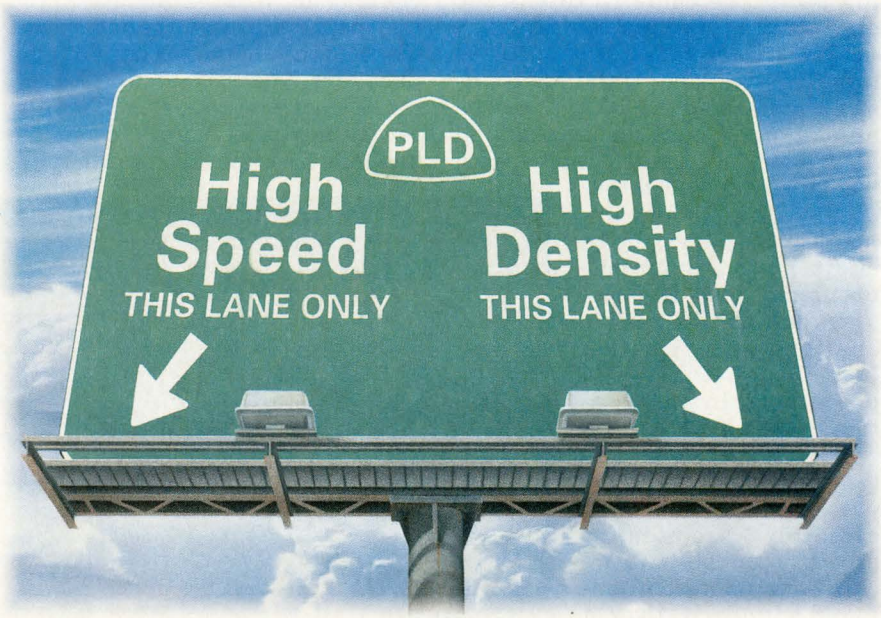


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INTEGRATED CIRCUITS

# Embedded RISC may be good for workstations too

*Dave Wilson, Senior Editor*

With the introduction of its RISC-based R3051 embedded controller, Integrated Device Technology (Santa Clara, CA) gave designers the option of using RISC chips in applications outside the realm of the workstation. Following up on the chip's success in the embedded arena, the company has decided to pursue two new routes—a lower-cost version of the R3051 itself, code named the LC, that will be announced later in the year, as well as a more integrated, higher-performance embedded controller, the R3081, announced this month. In addition to higher-performance embedded design wins, the R3081 may challenge the position held by low-end R4000 processors in workstation design.

For the embedded system designer, the R3000 processor may have been attractive architecturally, but probably wasn't cost effective when compared with derivatives of the 68000 architecture. Then the R3051 came along. An integrated RISC, it let system cost be reduced while promulgating the acceptance of the MIPS architecture. To broaden the appeal of embedded MIPS machines further, the R3081 is a R3051 derivative that has added a number of new features, including a floating-point unit (FPU) as well as larger caches. IDT has also tweaked the bus interface to let designers build faster systems.

*Phil Bourekas says that his company's new R3081 embedded RISC processor will rate 30 Mips at a 40-MHz clock speed.*

## Speeding right along

Offered at speeds of 20 to 40 MHz initially, the on-chip caches should be very acceptable to designers of laser printer controllers. A four-kbyte data cache is complemented by a 16-kbyte instruction cache. For those designers that need a different configuration, IDT has made the cache dynamically reconfigurable as eight kbytes of data and eight kbytes of instruction.

Some operating systems may require the organization of the cache be based on system activity. If your system is performing many matrix multiply operations, for example, or working on a large database, you may prefer to use a large data cache. On the other hand, for graphics applications, you may prefer to use a larger instruction cache. Both the caches are parity protected in the bus interface unit upon cache refill.

The bus interface on the new part has been changed to support higher system speed; nevertheless, it's still superset-compatible with the R3051. A higher drive system clock output lets you drive more critical logic from an unbuffered clock. Enabled as a reset option, a half-frequency memory bus interface operation can increase cache memory bandwidth without increasing the complexity of the memory subsystem as well. The chip can also operate from a 1× clock input, since generating a 100-MHz clock is a nontrivial design task.

In a head-to-head comparison with the R4000 family of devices also manufactured by IDT, the R3081 fares extremely well. IDT reckons that between 40 and 50 MHz, the R3081 will rate around 30 Mips. The 50-MHz R4000PC, on the other hand, makes its mark at between 32 to 35 Mips. At a similar performance level, the R3081 should cost substantially less than the R4000PC. In part, that's due to the small die area of the new chip—the R3081 is less than 180,000 mils$^2$ compared with the 360,000 mils$^2$ of the R4000PC. In addition, the 84-pin package of the R3081 will be less expensive than the 179-pin PGA package of the R4000PC.

Despite the fact that comparisons are bound to be drawn, IDT's manager of product definition and application engineering, Phil Bourekas, is quick to point out that he sees the R4000PC as the beginning of a new CPU family targeted at the high-performance marketplace, rather than at low-cost applications as is the case with the R3081. He thinks that both processors will find homes in their respective fields. This view may have some merit.

Certainly, the external cache supported by the R3081 isn't as sophisticated as that of the high-end R4000 devices. While tightly coupled multiprocessing support in hardware may have been left to the R4000, the R3081 does allow an external secondary cache to be built. In a secondary cache interface design somewhat analogous to the Intel 486, the chip can support the caching of snoop tags only, or a superset of the primary cache. Nevertheless, with the imminent release of Windows NT, the new Microsoft operating system that will run on both 80X86 and MIPS processor chips, there may be more than one personal computer manufacturer considering the R3081 as a viable alternative to the low-end R4000PC. ■

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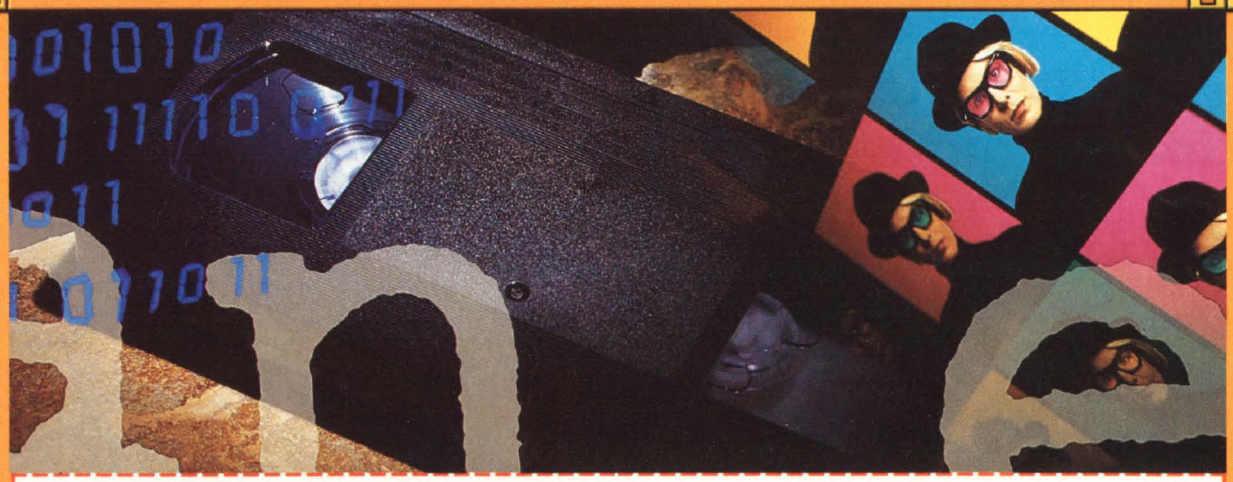

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INTEGRATED CIRCUITS

# Real-time DSPs target multimedia motherboards

*Dave Wilson, Senior Editor*

Recognizing that "multimedia" developers cannot live by chips alone, AT&T (Allentown, PA) has come up with a triple digital signal processor punch that includes a tightly integrated operating system, a DSP chip and signal-processing software modules. The DSP operating system is called VCOS for Virtual Caching Operating System. Residing under the control of a host operating system such as DOS, it provides an environment in which the DSP can operate as a parallel processor to the main CPU on the host motherboard or as a bus master on add-in cards. While the VCOS performs as a task under the host operating system, the kernel of the OS runs on a new "multimedia" DSP chip—the DSP3210 (See "Board, software tools speed DSP development on Mac host," p 116.) A library of signal-processing modules covers such functions as fax, modem and JPEG image compression and decompression.

## Adding to the motherboard

But questions remain. "How do you make DSP economical? How do you make it do something that people actually want?" asks Tony Agnello, president of Ariel (Highland Park, NJ). With the DSP3210, Agnello thinks that AT&T has attempted to do both. By restructuring the bus interface of an earlier DSP chip, the DSP32C, AT&T has created a new device that can perform bus arbitration and retry, as well as sit on a motherboard so that it can share system resources such as system memory, rather than use its own expensive SRAM. If the part's cost is $50, Agnello thinks that integrated voice mail, audio I/O and speech recognition will become feasible.

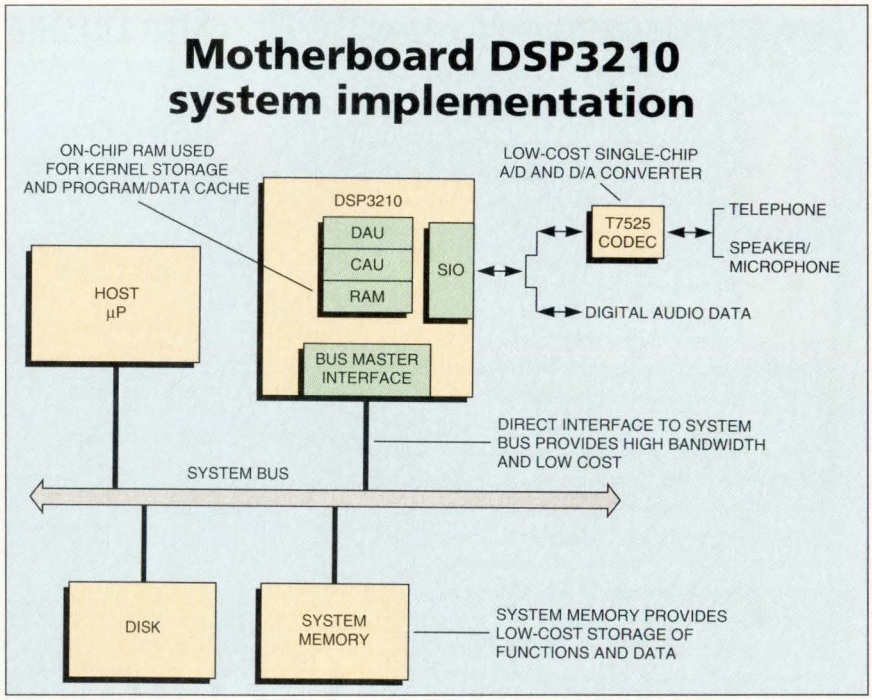
"The idea is to get the DSP3210 designed into motherboards, and the VCOS operating system is designed with that specific architecture in mind. It's not a general-purpose design," says David Wong, founder of Spectron Microsystems (Santa Barbara, CA), developers of the Spox real-time operating system. Indeed, the goal of VCOS is to schedule a small number of sequential tasks that are going to be cached in and out of memory under the control of the motherboard CPU. "The DSP has no memory. It's a subroutine engine on the motherboard," adds Wong.

All very well and good. But don't such approaches already exist in the marketplace? Other real-time operating systems and DSP chips certainly do. In fact, all the other major DSP IC houses—Analog Devices, Motorola, Texas Instruments, to name a few—have embraced the Spox real-time operating system.

Nevertheless, AT&T claims to offer a couple of advantages over the Spox solution. First, since the complete package—hardware, OS and software library—comes from a single vendor, you don't have to shop around for pieces to solve the problem. Second, because the VCOS operating system can let the DSP3210 use the existing memory in the PC, you don't have to use dedicated SRAM for DSP data and program storage, lowering the system cost.

## Limited ability compared to Spox

Most agree that AT&T does have a unique—if rather inflexible— approach. And, although it's possible to use a general-purpose OS like Spox to solve the same class of DSP/motherboard problems, the hardware will undoubtedly cost a little more. It's a trade-off. While the Spox kernel offers a universal solution that can work in a motherboard/DSP hardware combo, a stand-alone situation or an add-in card, the VCOS is most effective when tightly coupled to the CPU on the motherboard. "The OS is also very small and very limited. Its main purpose is to be a scheduler of the library of functions that AT&T provides," says Wong. Unlike Spox, he adds, the AT&T VCOS is not a preemptive multitasking kernel, so it's very specific to the DSP3210, which isn't capable of running a multitasking OS anyway. "The model is basically a single-tasking environment. Preemption is not at all possible," he




*By sharing system DRAM resources, rather than using its own dedicated SRAM, the AT&T DSP3210 device lets designers build low-cost motherboards with DSP. To help minimize glue logic, the port features a bus interface compatible with Intel and Motorola processor families. The question is, who will use the device on a motherboard first?*

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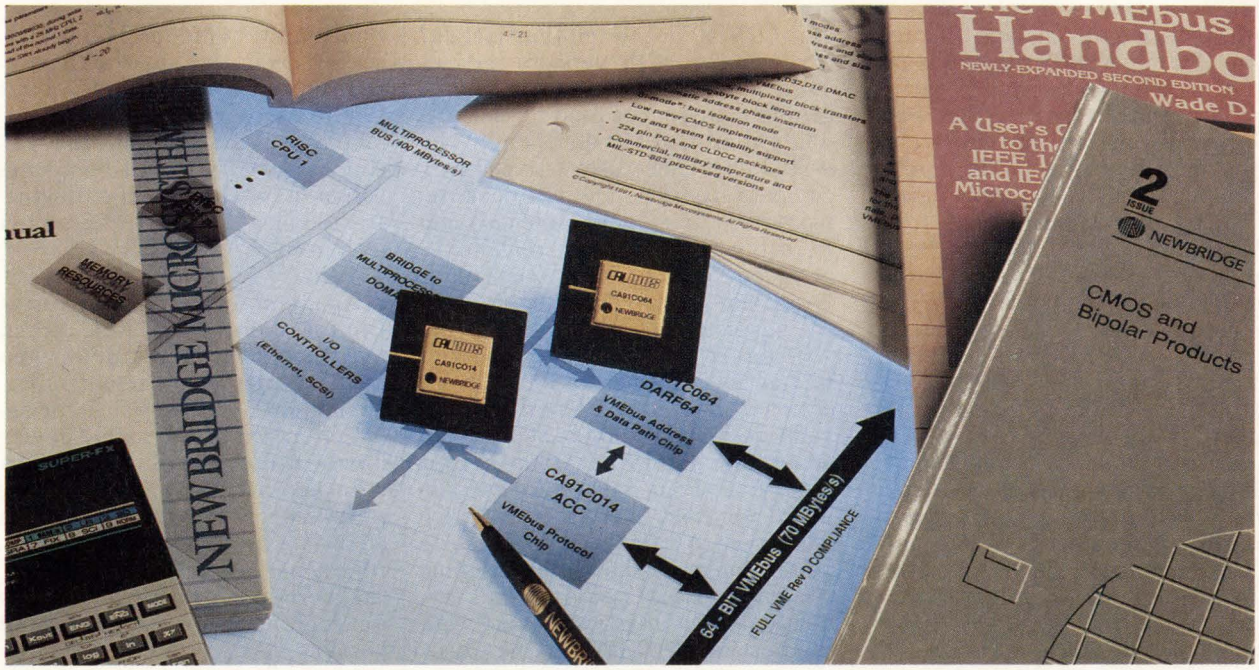


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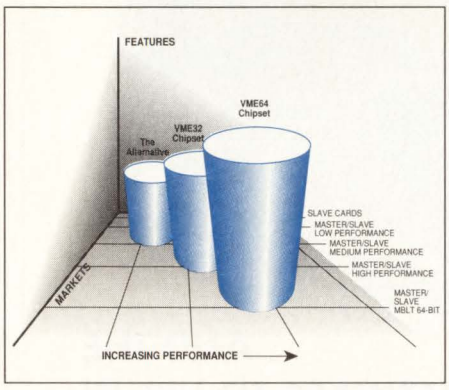


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states—although perhaps the real value of what AT&T is trying to sell is in the signal processing library.

Ariel's Agnello agrees. "The Spox OS provides portability across platforms and DSP chips that isolate the developer from the details of the underlying hardware," he says, "whereas VCOS is built to be as simplistic as possible, and also very specific to a particular chip." In fact, he adds, VCOS won't even run on some other AT&T DSPs—it's specifically tailored to run on the DSP3210, which is designed to operate as a component running under the host OS, just as the DSP3210 is designed to be a component working on a motherboard. Agnello agrees with Wong that VCOS is a task scheduler rather than a full-blown OS, unlike Spox. "But, unlike the Spox OS, VCOS needs less code space to run in—it's lean and mean," says Agnello.

Despite the benefits, some important questions remain. First, are PC or workstation vendors ready to design DSPs on to motherboards? Since many such vendors haven't even committed to putting VGA graphics there, the answer is somewhat doubtful. Even though the AT&T approach costs less than its competitors, just how low does the price need to be? "I know of only one PC company that thinks that VCOS is a good solution," says Wong. Justifying this statement, he confirms the suspicions of others. "Nobody is willing to put the DSP on the motherboard. Where are the applications?" he asks. With that in mind, vendors may be tempted to turn to designing add-in cards as a first step, but Wong suspects that the AT&T solution is inappropriate for that type of approach. "If you're [sharing memory] over the ISA bus, it's going to cost you a lot [of overhead] moving programs to and from the host to the DSP chip," he says.

## DSPs at home in workstations

Although PC designers may not be leaping at DSPs as the solution to their multimedia problems, workstation designers have dabbled with the technology. Digital Equipment Corporation (Maynard, MA), for example, uses the Motorola 56001 DSP chip as part of its multimedia audio solution, although the device is treated as a dedicated resource and isn't user-programmable.

John Morse, engineering manager of multimedia products at Digital, admits that the company has thought about DSPs when a special-purpose processor is needed on a motherboard, or as an option in a user-accessible device to accelerate a particular function, whether it's 3-D rendering for graphics or imaging. But Morse adds, "we haven't committed to putting a user-programmable DSP on the motherboard. Our philosophy is to avoid that whenever it's humanly possible."

It's really a question of what Digital gets for its investment. "We're really looking at next-generation workstations where the main workstation processor has the horsepower to do what the DSP is doing today. That's the philosophical direction that we're heading," he says. Rather than spending money on a DSP, Digital prefers to spend the dollars on beefing up the single-workstation CPU. "It retains the general-purpose nature of a programmable device rather than a special-purpose device," says Morse, but he likes to hedge his bets too. "That's not to say that Digital will never put a DSP on the motherboard..." ■

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CIRCLE NO. 27

SOFTWARE & DEVELOPMENT TOOLS

# Strategic alliances to broaden standards, tool offerings

*Tom Williams, Senior Editor*

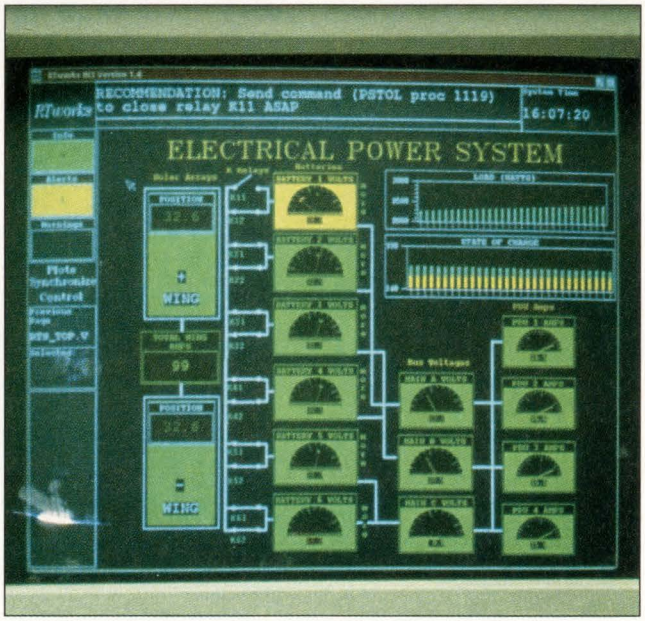
As vendors of real-time executives succeed at weaning designers from "roll-your-own" kernels, they find themselves in a double bind. The dual pressures of customer demands and time-to-market issues are causing designers to ask for standard interfaces to real-time operating systems, and to request development tools to design around these operating systems. Real-time kernel vendors, on the other hand, face a build-or-buy decision with regard to such interfaces and tools to meet the challenges of their market.

Some vendors, such as Ready Systems (Sunnyvale, CA), have chosen to develop their own CASE tools—in this case CARD-tools—while others are seeking strategic alliances. Wind River Systems (Alameda, CA) is taking the latter route, expanding its standard interface offerings to its real-time system environment, VxWorks and the VxWorks real-time kernel called Wind.

To offer compatible tools for building complex real-time control systems, Wind River has forged an alliance with Digital Equipment Corporation (Maynard, MA). This will make its VxWorks kernel compliant with the Posix standard interface for Unix systems.

## Real-time standard inevitable

There's something inexorable about standards. For all the infighting over defining them, for all the protests from purists that they don't promote the utmost in performance, and for all the jockeying among vendors to get their existing ideas accepted, standards have a way of emerging as a natural process in a maturing industry. So it was with graphics and user interfaces, so it is with operating systems, and so it shall be with real-time. There will always be alternatives to standards for those willing to pay the price in money and time-to-market for higher performance or specialized needs. Posix—for all its critics, but with the backing of the government—is taking on the momentum of an emerging standard. Now that a set of real-time extensions is close to approval for Posix, real-time software developers are being attracted by the advantages of standards.




*Talarian's RTworks includes a human-computer interface module, RThci, that lets you build point-and-click user interface screens to monitor and control real-time processes via other RTworks modules.*

Under the agreement with Digital, DEC and Wind River will jointly develop Posix-compliant real-time software. Digital is licensing VxWorks as the core technology for the new product, DECelx. DECelx will then form the key technology for a comprehensive strategy on Digital's part to resume the position it held in the 1970s real-time market with its PDP-11 machines, which ran the RSX-11 and RT-11 operating systems. Digital will now focus on developing real-time and embedded applications in the Unix arena targeted mainly at VME bus boards.

For its part, Wind River will have Digital's assistance in making VxWorks fully Posix-compliant. "Wind River was one of the early supporters of Posix as a tool for providing an open systems interface between real-time applications and systems," says Mitch Bishop, director of marketing for Wind River. "This agreement acts as a catalyst for providing full Posix real-time compliance in standard VxWorks for our customers."

The initial version of DECelx, based on Wind River's VxWorks 5.0 release, will include a suite of development tools such as the GNU compiler and debugger and will support networking facilities such as TCP/IP (Transmission Control Protocol/Internet Protocol), network file systems (NFSs) and sockets; it will also be compliant with the Posix 1003.1 file system. In addition, Version 1.0 will include timers, semaphores and signals, some features of the 1003.4 real-time extensions to Posix. Other real-time extensions will be added as they move toward final adoption as a standard. Initially, DECelx will run on DECstation host computers and support target systems based on Motorola 680X0 and MIPS R3000 processors.

## Real-time tool support

In addition to teaming up with a company producing a standard operating system, Wind River has expanded its reach in tool support through an agreement with Talarian Corporation (Mountain View, CA). It will port that company's RTworks real-time development tools to VxWorks. RTworks is more than a set of CASE and programming tools; it's a suite of modules that lets you develop intelligent distributed operator systems for complex real-time control applications. Talarian gains by the alliance in that its control systems can now be easily used with an off-the-shelf real-time kernel and can move into more embedded designs.

Talarian's RTworks modules are based on a client-server model that

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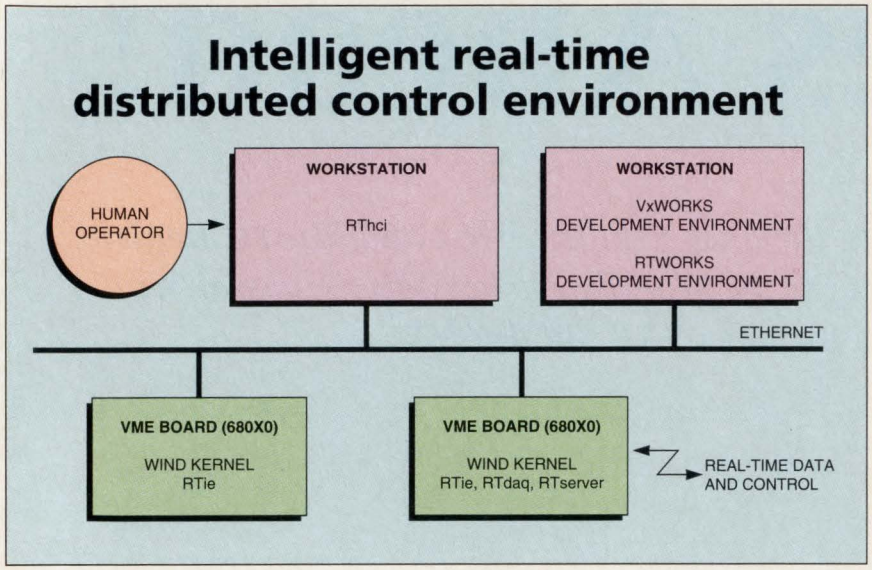
## SOFTWARE & DEVELOPMENT TOOLS




*The combination of Wind River Systems' VxWorks with Talarian's RTtools lets designers build distributed real-time systems with a deterministic real-time kernel at dedicated nodes and distribute data anywhere it's needed on the network. Talarian modules will work with applications created with development tools already available under VxWorks.*

lets you set up control systems including interprocess communication, data acquisition and an inference engine. A module called RThci is used for building graphical human interfaces. The inference engine module, RTie, uses rule-based inferencing to build expert knowledge into a real-time control system.

The RTie module can be set up to evaluate rules expressed in an IF-THEN syntax via three different methods. The methods are temporally-driven (i.e., periodic testing), data-driven by the change of some specified data or goal-driven to achieve some condition. The inference engine can be embedded in a C program and, thanks to the port to VxWorks, can now be easily built into a board-level controller.

The distributed nature of RTtools means widely different configurations can be created with inferencing dedicated to a single node or made available to the entire system

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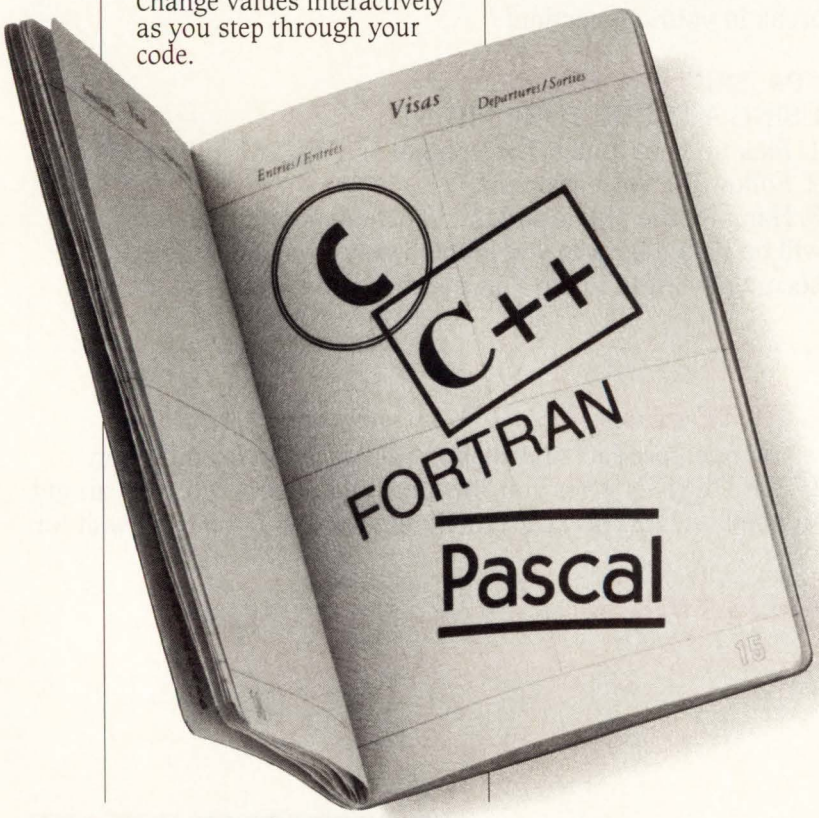


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via the network—depending on the critical needs of the application. The communication server, RTserve, supports TCP/IP and DECnet. It uses message passing to send or broadcast messages to a specific process, all processes of a particular type, all processes on a given node, or to all processes that receive a given type of data (e.g., all data from a thermal monitoring system).

***"We're giving our customers the added bonus of knowledge-based systems and the ability to distribute applications over multiple processors."***

*—Mitch Bishop, Wind River*

The RTdaq data acquisition module is RTworks' link to incoming data from the real world. It acquires, filters, preprocesses, and converts incoming data from either sensors, disk files or RTworks' own data generation module used in designing and testing systems. RTdaq routes data to real-time nodes on a distributed system via the server module.

According to Talarian president and CEO David Mandelkern, the agreement with Wind River first gives "our customers the ability to provide deterministic real-time data acquisition and control, and second, allows us to extend our technology beyond the Unix workstation arena and into the world of embedded real-time systems." Wind River's Bishop adds that, for its part, "We're giving our customers the added bonus of knowledge-based systems and the ability to distribute applications over multiple processors." ■

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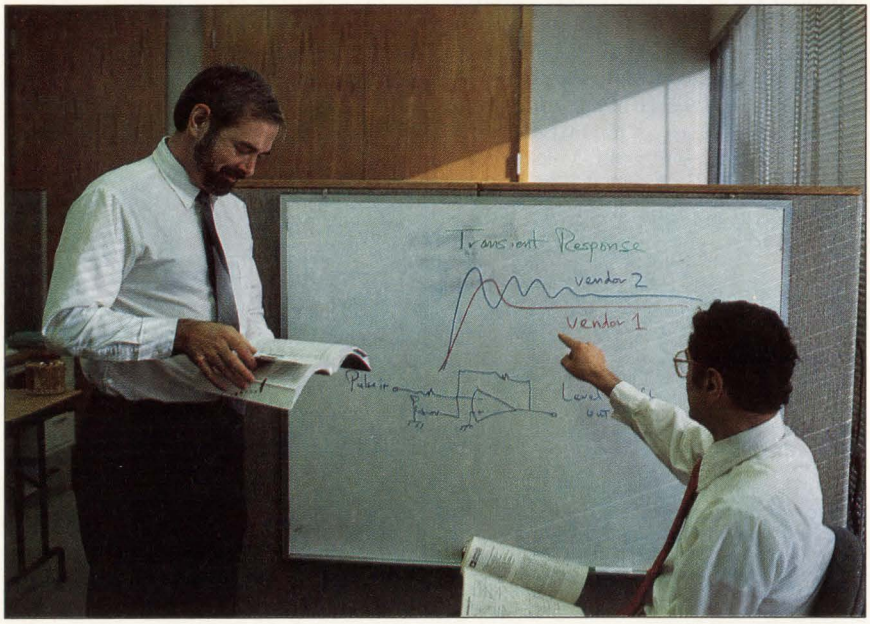
CAE/CAD TOOLS

# Start-up breaks new ground with analog hardware modeling

*Mike Donlin, Senior Editor*




***"In a perfect world, all electronic circuit operations could be accurately predicted using mathematical abstractions," says Wayne Fretwell (left), software program manager at Zeelan. "But no component remains constant over all operating conditions, which is why a hardware/software approach is best for modeling accuracy."***

As more and more analog parts find their way on to what were once purely digital PCBs, designers are seeking analog device models for simulation. They're frustrated, however, by a lack of models, for both analog effects and devices, that can be used efficiently for PCB simulation. In response to this need, start-up Zeelan Technology (Beaverton, OR) has just introduced ModelStation, a hardware/software combination that generates analog models of hardware from actual devices.

The system, controlled by PC- or workstation-based software, lets you extract analog and mixed-signal primitive or behavioral models from devices mounted on test fixtures. According to Zeelan, you can use ModelStation to specify real-world operating conditions, characterize a device within a specific environment and extract a mathematical model based on a comprehensive set of measurements taken from the actual behavior of the device. The system supports analog behavioral models, Spice macromodels and Spice primitive models and can be used with a number of analog simulators from major CAE vendors.

## Software models inadequate

The product introduction is significant because today's high-speed, tightly integrated PCBs are plagued by analog effects such as crosstalk, ringing and transmission line effects which digital designers must design around. There are numerous Spice model packages which boast accuracy and aren't too expensive, but a detailed device model is cumbersome at the PCB level and the resulting simulation can take an inordinate amount of time to run. Alternatives to Spice exist—for instance, the MAST hardware modeling language from Analogy (Beaverton, OR) or Spectre, a C language-based analog simulator from Cadence Design Systems (San Jose, CA). But these analog simulators are based solely on software models; few hardware modeling options have been available in the analog domain.

## The hardware model solution

Though the market for analog hardware models is new, Zeelan is hoping to persuade engineers to spend $80,000 and up for the ModelStation. "Fewer than 5,000 of the 600,000 available analog components have been modeled to date because model development is a difficult, time-consuming and expensive process," says Hiro Moriyasu, CEO and president at Zeelan. "Even when designers undergo the arduous task of creating models from data book specifications, they often discover that their models are inaccurate because they don't take real-life operating conditions into consideration."

To accommodate the variables a device will encounter in real-life circumstances, Zeelan supplies a signal acquisition and processing system as well as intelligent test fixtures for connection to physical devices. To develop a model, you insert a sample of the required device into the fixture and complete a menu-based setup routine specifying operating voltages, output loads and other operating parameters. After setup, the device is exercised and the resulting data saved to the host system. The system automatically generates appropriate pulses, measures the device response and calculates the model parameters. The model can be extracted to the accuracy you desire. According to Zeelan, devices that can be modeled include discrete devices, high-speed logic devices, linear ICs, transmission lines, and fully loaded backplanes.

ModelStation uses a time-domain approach that compares inputs to outputs. This approach, according to the manufacturer, is superior to those of network analyzer-based systems because it permits modeling of switching as well as linear devices. "Time-domain characterization also permits the measurement of dynamic nonlinearities such as stored charge effects in semiconductor junctions, as well as differences in positive and negative rise and fall times," Moriyasu adds.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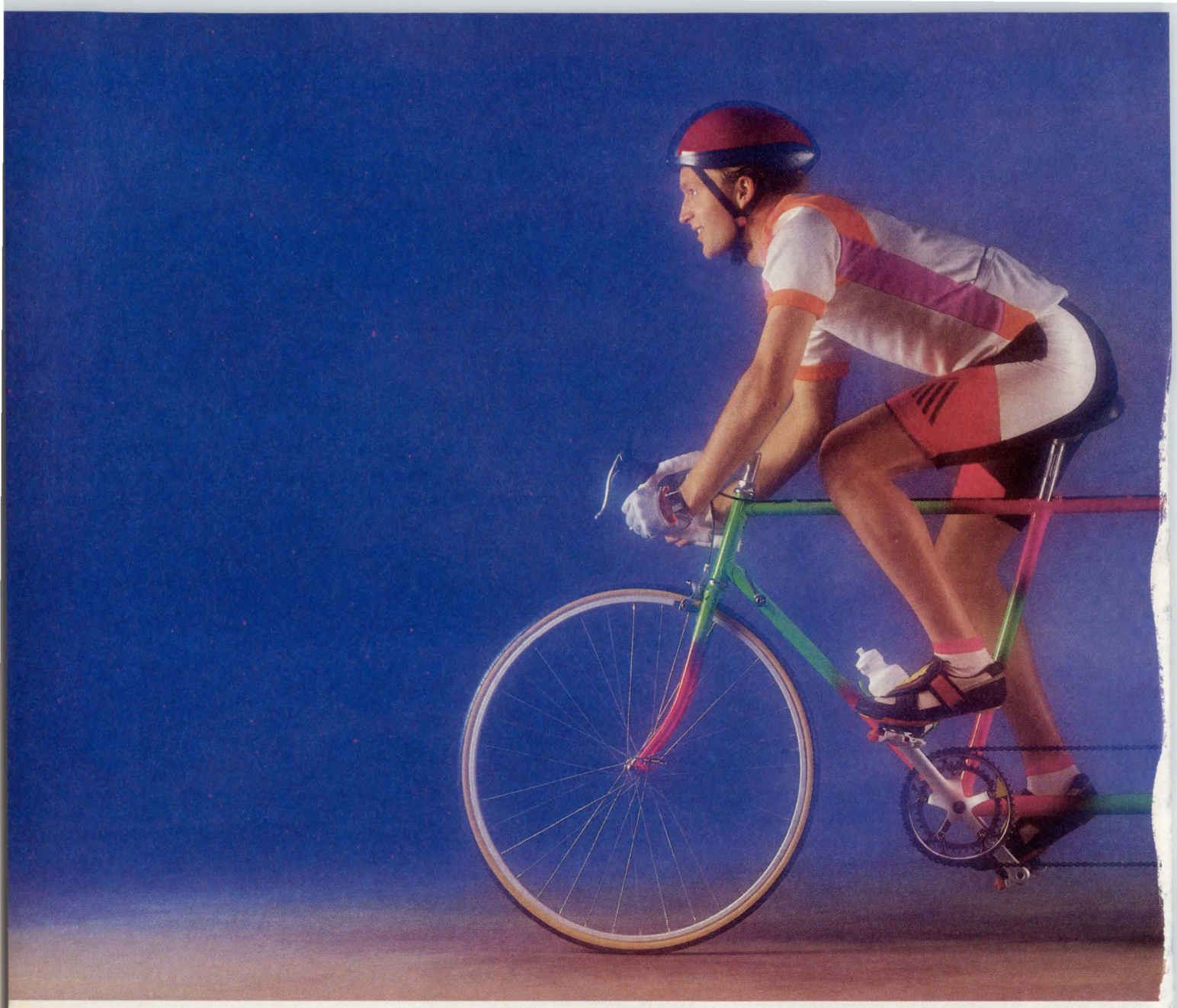

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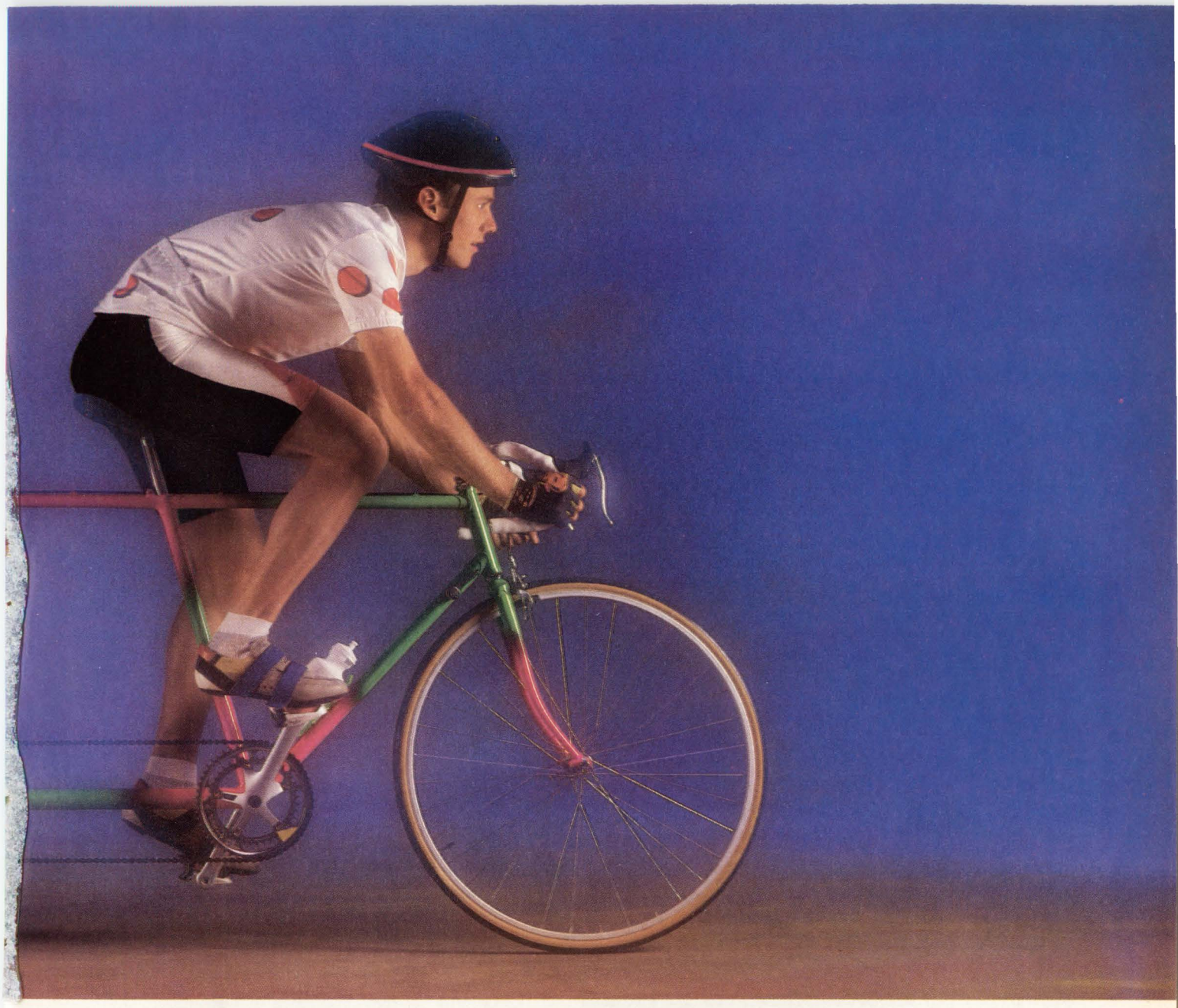

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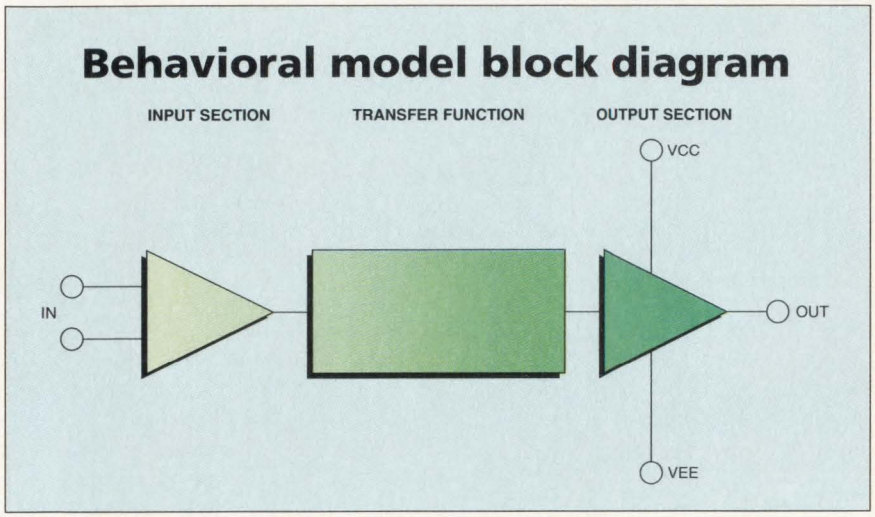



*Zeelan's ModelStation has a proprietary, automated root extraction capability which produces Laplace transform behavioral models of analog components or circuits. The system can produce a "black box" transfer function from input and output responses in a single-pass operation. According to Zeelan, the resulting behavioral model can simulate about 1,000 times faster than a comparable detailed circuit-level simulation and still provide almost as much accuracy.*

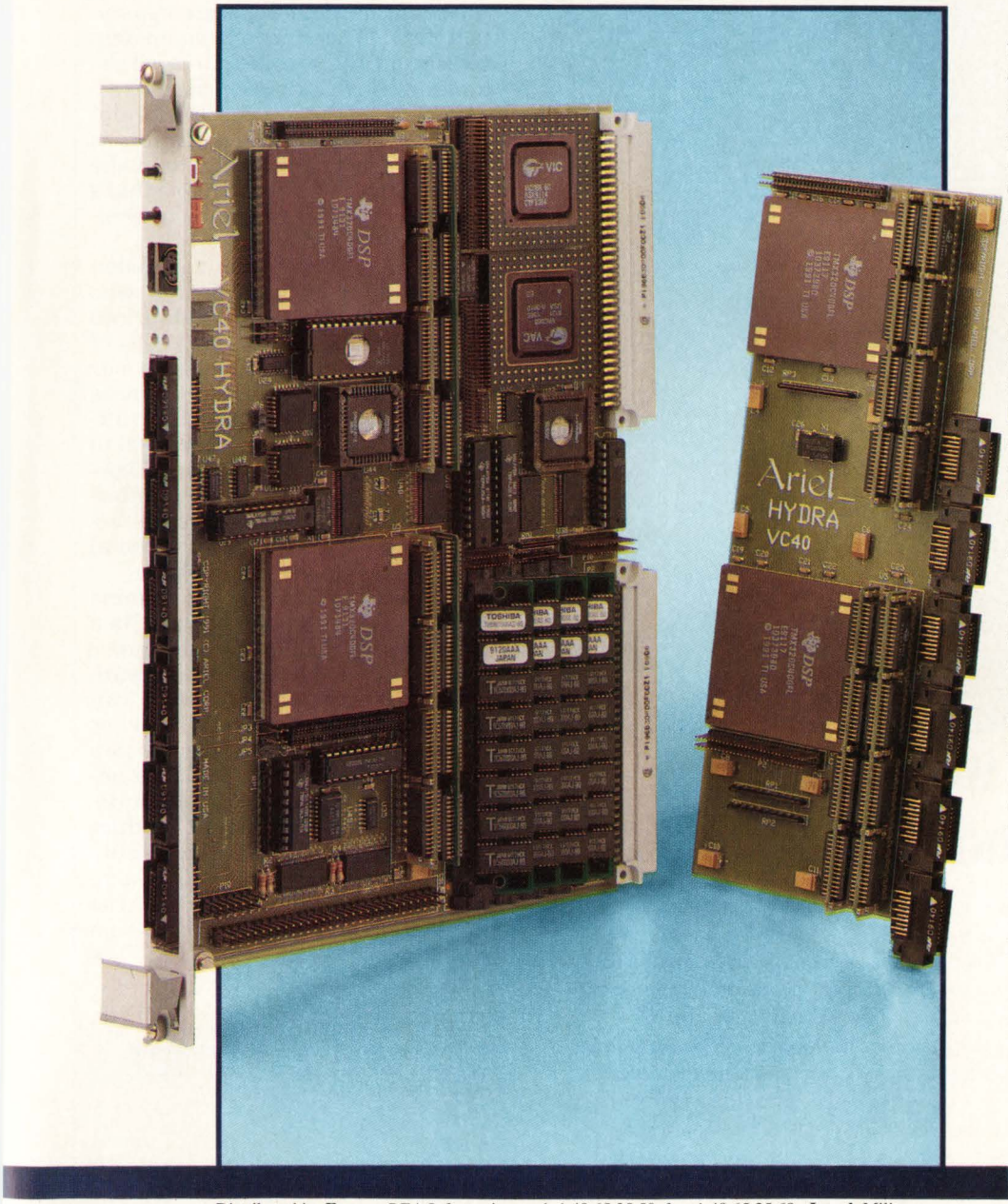
"Competitive methods can only measure dc nonlinearities."

### Too small a niche?

Though it would seem that Zeelan's solution to the analog modeling problem will play to an eager audience, several CAE vendors are skeptical about the system's capabilities and wonder whether it does enough to justify its price. "The major problem I see is that their models are based on small signals," says Charles Hymowitz, vice-president at Intusoft (San Pedro, CA), a CAE vendor specializing in Spice modeling techniques. "This means that they're only going to work at one bias point and can't account for the various nonlinearities that designers are interested in. Their system reads the bias point on the device and generates a transfer function that's very accurate at that particular bias. You can run an ac analysis and a transient analysis from that

# Ariel V-C40 Hydra Breaks the BOPS Barrier

## 1.1 billion operations per second sets the record for 6U VMEbus coprocessor cards

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**CIRCLE NO. 34**

CAE/CAD TOOLS

point, but what happens if you want to put in a very large signal and saturate an op amp? It doesn't look like the system can handle it."

Zeelan answers this objection by citing the designer's need to generate responses to a normal stimulus, not necessarily the whole gamut of stimuli a device might conceivably encounter. "The key element here is that an engineer should have a handle on the range that a device is going to experience on a particular PCB," says Joe Skovron, vice-president of marketing and sales at Zeelan. "So a designer might define a bias voltage from –3 to +7 volts and measure the device with our stimulus response capabilities over that specified range."

Other CAE vendors wonder whether Zeelan is trying to market equipment that's already available. "I think people are going to ask if the Zeelan system is going to do anything that a good analog tester can't already do," says Shawn Hailey, president of Meta-Software (Campbell, CA). "There have been op amp testers on the market for a while, and certainly you can characterize a device with the proper lab equipment. I suppose the question is whether Zeelan is going to make something generally available that's only been [in] the domain of well-equipped laboratories."

Zeelan is indeed aiming ModelStation directly at designers who have had to depend on high-priced lab equipment or the vagaries of software models. "It's true that our system will be competing with racks of test equipment and modeling software, but they're in the $100,000 to $300,000 range," says Zeelan's Skovron. "In addition to the price difference, the competition addresses active components only. No behavioral modeling capability is available."

Is Zeelan uncovering a gold mine or is it offering a product that fits a tiny niche? Most everyone agrees that an affordable analog hardware modeling system that really can characterize the transient behavior of components and transmission line effects would be a welcome addition to any designer's tool suite. The problem is trying to produce accurate results across the infinite range of possibilities that have made analog device modeling the holy grail of today's PCB design community. ■

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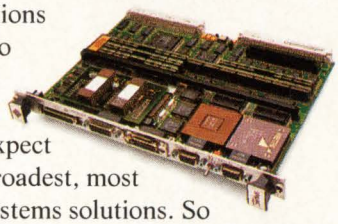

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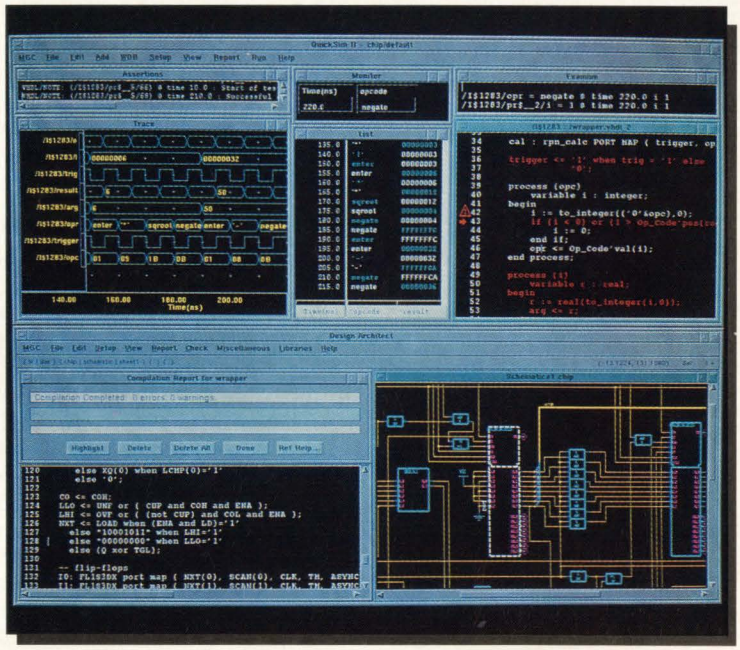
**CIRCLE NO. 36**

# ASIC designers turn to VHDL tools despite obstacles

***Though still quite primitive, VHDL simulation and synthesis tools are shipping in abundance. Committed users are establishing design methodologies that get around unresolved issues in performance and modeling.***

**Barbara Tuck Egan**
**Senior Editor**



*Mentor Graphics' VHDL-based System 1076 works in conjunction with Mentor's AutoLogic VHDL and AutoLogic Blocks synthesis tools. The VHDL compiler, which identifies errors and shows the areas in which errors occurred, lets users change code during compilation, with resulting textual changes being noted.*

It's no longer asked if VHDL will ultimately be adopted as the standard hardware description language. The only remaining questions are: When will the majority of designers embrace VHDL? And how much will it boost their productivity?

With new VHDL tools to wrestle with and dramatic changes in design methodology to adapt to, engineers are having to get past many stumbling blocks to get results. Ta-Wei Chien, director of VLSI engineering at the Entry Systems Division of Silicon Graphics (Mountain View, CA), reports that simulation gives him more of a problem than anything else. "If designers pay attention to the process, they can get the job done," Chien says. Since Chien's division adopted VHDL two years ago, designers have completed about 14 chips using it for simulation and synthesis. Since most vendors didn't have VHDL simulators ready in 1989, Chien's engineers used an internal simulator and translated VHDL syntax to C language models with VTIP (VHDL Tool Integration Platform) from CLSI (Rockville, MD).

Today Silicon Graphics uses VHDL synthesis from Synopsys (Mountain View, CA), and early last year the company purchased the Vantage (Fremont, CA) simulator to reach full VHDL capability. "Now, with the VHDL simulator, we have to be more explicit in syntax," says Chien, who reports that the group switched to a commercial VHDL simulator because Silicon Graphics didn't have enough resources in the CAD group to maintain and support its internal software. "It's better to have a whole company behind a tool," Chien adds.

## Room for improvement

The Vantage simulator still has a lot of room for improvement, according to Chien. "Verilog is more fine-tuned than the Vantage algorithms and coding. Every new release of Vantage has double or triple the simulation performance, which indicates to us that the simulator is just growing.

Eventually, it will compare to Verilog."

When it comes to verifying a large number of ASICs at the board level, the key for Silicon Graphics, according to Chien, is its proprietary distributed systems simulation environment. Designers can run Verilog and VHDL simulators concurrently to solve capacity and performance problems. At the ASIC level, Chien's engineers have, until recently, designed their own VHDL models according to a five-state value system, rather than using the more detailed nine-state value system (MVL-9, or multivalued logic 9) which is being declared an IEEE standard. "We have been using MVL-5 because we get a 20 to 30 percent performance boost over MVL-9," reports Chien.

At present, Silicon Graphics has an alpha library of VHDL models from LSI Logic (Milpitas, CA) for LSI Logic's 1-µm LCA100K gate-array family. LSI Logic is waiting for the official adoption of the nine-state value system before offering VHDL models to the general public. According to LSI Logic, MVL-9 models are fast enough for high-level simulation and efficient enough for gate-level.

How smoothly does the VHDL design flow go for Chien? "The reality is that we do a lot of iterations through Synopsys," he explains, "a few to several iterations at each step." The user's only control, according to Chien, is through constraints or coding style. "You have to force the synthesis tool to change the architecture," he adds.

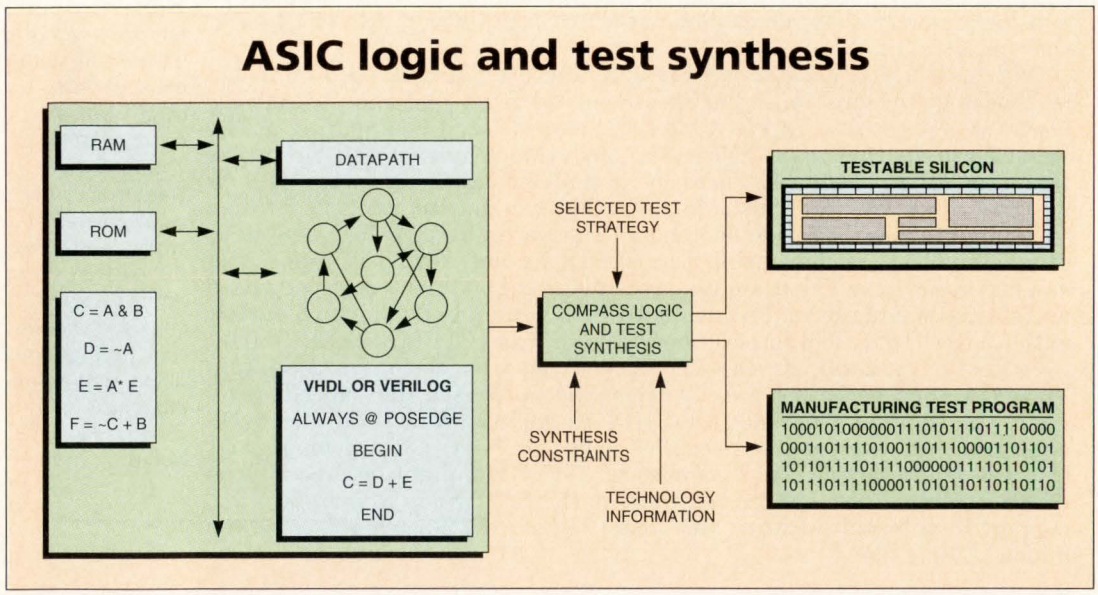
As for test, Chien's group uses ATPG software from foundry LSI Logic. Why not use the Synopsys Test Compiler test synthesis tool? "Every time I do ATPG, I have a problem matching my test vectors to the silicon vendor's tester," explains Chien. "If I have such a hard time with the silicon vendor's own software, how can I expect a third party to do it any smoother? All those new tools take a lot of additional effort." Chien's group will begin using the Test Compiler to check test coverage, but not to generate vectors.

## Drawing black boxes for ASICs

When engineers under Jim Keeley, senior staff engineer and technical leader at Zenith Data Systems (Billerica, MA), made the switch half a year ago from a proprietary language and mainframe-based proprietary tools to VHDL and third-party tools, they chose to go with the graphical entry and VHDL-XL simulator tied into Design Framework II from Cadence Design Systems (San Jose, CA). The dozen or so ZDS designers, about six weeks into a 250,000-gate, multi-ASIC project, blocked things out using graphical entry. "There's not even one ASIC designer on the team," says Keeley, who explains that "we don't differentiate between subsystem and ASIC design. We draw a black box that says ASIC—we don't pound gates."

Because Cadence's VHDL-XL simulator basically has the same simulation engine as Verilog, Keeley's team can use gate-level models for Verilog. For synthesis, the team went with Synopsys. Though Cadence's VHDL synthesis is shipping this quarter, it wasn't available when ZDS was assembling tools.

Whether the Cadence VHDL tools or similar offerings from Valid Logic Systems (San Jose, CA) will survive the merger of the two companies remains to be seen. Unlike the Synopsys, Valid and Vantage offerings, and the new VHDL simulators from Model Technology (Beaverton, OR), all of which support VHDL in its entirety, Cadence's VHDL-XL falls short of supporting all VHDL constructs. Cadence could take advantage of the full language support of the Valid simulator and, at the same time, hang on to the leverage afforded by the XL algorithm and the support of all the Verilog libraries. Full VHDL support becomes significant, Cadence admits, where model interoperability is involved. In the meantime, Valid has integrated its VHDL simulator into the Logic Workbench TD to provide connection to a library base through Valid's gate-level simulator RapidSIM, which supports at least 140 ASIC libraries.




*Compared to other tools, Compass Design Automation (San Jose, CA) claims that its ASIC Navigator toolset offers a broader test synthesis solution to VHDL users, one that enables an entire ASIC and its associated test circuitry to be synthesized. Compass users can synthesize not only random logic, but also RAMs, ROMs and datapath elements. In addition to manufacturing test, Compass offers BIST and boundary scan for field diagnostics.*

Valid VHDL user Damian Deneault, principal engineer at PictureTel (Peabody, MA), is reasonably confident with regard to the survival of Valid's simulation backplane technology, which lets users mix VHDL simulation with gate-level simulation on RapidSIM. Deneault has just begun designing a million-transistor video signal processor with Valid's VHDL. Why Valid? Deneault says that the ability to integrate the VHDL

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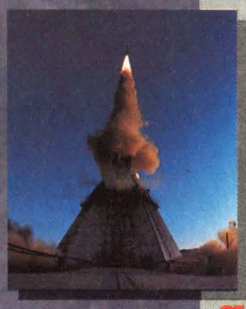

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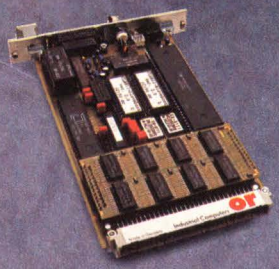

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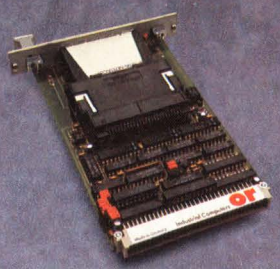

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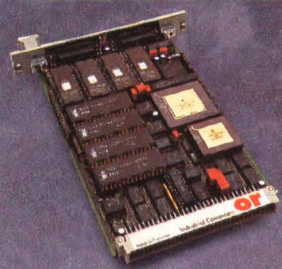

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## What users need to know to be productive with VHDL tools

For designers working on advanced systems and products, the lure of synthesis is all but irresistible. The growing number of specialized tools now reaching the market—for FPGAs, PLDs, and so on—makes the use of synthesis even more compelling, especially since these tools can take the user so close to the final implementation of any design. Ideally, the emergence of VHDL permits users the freedom to mix and match different synthesis tools with a single VHDL simulator and front end. As tool specialization increases, however, and as more and more designers attempt to put the tools into play, the problems and pitfalls are beginning to emerge in more detail.

In effect, these problems can negate the advantages that synthesis tools offer, especially when they are being applied in top-down design methodologies based on VHDL and sophisticated simulation.

### Problems, problems

Perhaps the most serious general problem identified by an increasing number of users involves the time and effort required to meet specific demands or requirements of a particular synthesis tool. The effect is that the synthesis tools shift the effort from one portion of a design to another, with users trading design time for tool-tweaking effort. Such a task can become almost as difficult and time-consuming as simply designing specific gates by hand. This problem is, of course, compounded if the design team is applying more than one type of synthesis tool in its design, such as gate or test synthesis or an accelerator with a synthesis front end. In effect, designers are forced in many instances to design to the synthesis tools' limitations.

The basic lack of synchronization among synthesis tools is common at this stage of the technology, and evidence of problems or potential difficulties is not hard to find. Recently, a Vantage customer explained that his design team was having problems with the considerable task of using both simulation and synthesis in an advanced design. The synthesis tool was generating incorrect gates because the tool could not understand a sufficient amount of VHDL code.

For example, the statement "PROCESS (a)" indicates that VHDL in the following process should *only* be evaluated when signal "a" changes, that output should only be altered if there's a change in "a." The process isn't supposed to react to any change in the value of any other signal.

Unfortunately, the synthesizer our customer was using ignored the list of signals to which the process is intended to be sensitive, resulting in the gates being sensitive to changes on either "a" or "b" rather than *only* if the signal "a" changes value. The synthesizer did give the message that it would be "ignoring process-specific sensitivity lists," and then it went ahead and generated faulty gates.

The solution for the user in this case was to recode the design using "WAIT" rather than "PROCESS" statements. Fortunately, the design team was working with a full VHDL simulator that understands both kinds of statements; but it took considerable time to isolate the problem and recode the processes. (The WAIT statement recording, which is neither clear nor concise, is far from an ideal solution.)

### Three key points

From this experience and others gathered from customers using simulation and synthesis tools together come three key points for designers formulating a simulation/synthesis design methodology:

1. Synthesis doesn't always guarantee correctly functioning gates. Also, it's absolutely imperative to simulate after synthesis for a final check. This post-synthesis simulation should functionally match the behavioral simulation.

2. Specialized synthesis tools are emerging now, each with its own idiosyncrasies and limitations. Each tool requires a different variation of the input VHDL language; so choose the synthesis tool before modeling at the RTL level.

3. Meeting the requirements of the synthesis tool can quickly negate much of the time saving generated in top-down design. Without careful planning, you will find yourself trading one lengthy task for another.

When basic issues are taken into consideration during the design process, top-down design with synthesis can provide the benefits it should. Here are four suggestions, again from users of recent vintage:

First, remember that the benefit of top-down design is high-level simulation, where architectural trade-offs can be studied and quality can be designed into the product rather than being tested back into it. Sacrificing these advantages by designing for a specific synthesis tool will prove to be a poor trade-off that will take up all or much of the time that could be saved by using advanced tools.

Second, be sure to allow time in the design schedule to simulate *prior to and following* synthesis. In a five-month process, for example, the first four months might be applied to high-level design and simulation. The last month should be set aside strictly for synthesizing, then resimulating.

Third, use a full VHDL simulator, as opposed to any subset or superset. This is the only way to be certain the VHDL will synthesize correctly. Don't expect any kind of standardized subset. It will never emerge; intense competition is almost guaranteed to prevent it.

Finally, disregard claims about the level of integration between tools and focus instead on generating a design at the highest level to gain the significant benefits available from top-down design. Manually tweak code for each specific tool, as required.

As more RTL-driven electronic design automation tools come to market, most of you will apply far more than just one of them. Since it isn't possible for each of these to be integrated with each other, keep focused on the top-down design approach and on simulation capability. Also, expect that each team of six design engineers will require at least four simulators and one synthesis tool. The simulation investment should focus on ease of use, speed and capacity. You should demand that the simulator be versatile enough to work with a wide range of the emerging synthesis tools, including RTL-to-gate-mappers, test synthesis, process-specific synthesis (e.g., for FPGAs), and others. Since most synthesis tools will never optimally support every situation, the toolbox approach is best.

**Pam Rissmann,** senior product support engineer, Vantage Analysis Systems




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tools with Allegro, which PictureTel had in-house, was a factor in his choice, as was full compliance to the spec. Also very appealing, according to Deneault, is the ability to mix gate-level and VHDL models and have the tools act like a single simulator—with the same user interface and the same test vectors.

## No gurus here

A Verilog user in the past, Deneault says that "we're not interested in the extra capabilities of VHDL. No one here is a guru." Though Deneault reports some frustration with the inherent complexity and verbosity of VHDL, he says that its flexibility has let his design team do some things they couldn't with any previous language.

However, the fact that VHDL isn't automatically synthesizable discouraged Peter Willaert, manager of electronic hardware engineering at the R&D equipment department of Agfa-Gevaert N.V. (Mortsel, Belgium), from using it. A fan of the SilcSyn synthesis tool from Racal-Redac (Mahwah, NJ), Willaert chose to go with Racal-Redac's SDDL proprietary language, which is limited to synthesizable operations. Though VHDL was never intended to be a synthesis language, many designers are using it for that purpose (see "What users need to know to be productive with VHDL tools," p. 64).

"VHDL synthesis can produce a very high productivity level if you know how to drive it and how to write VHDL to get that productivity," says John McBride, hardware tools and design services manager at GPT (Dorset, England). McBride's team is using Racal-Redac's SilcSyn II for a multi-ASIC telecom system project. In the main, telecom ASICs require hand customization of logic more than other application areas, according to McBride. "We believe that engineers should work on sections of logic that they're particularly concerned about," he explains, "and let the synthesis tool do the 'don't care' parts."

To write synthesizable VHDL code, McBride's group took standard functions, coded them and compared the number of gates and timing against results they would have achieved if they had designed at the gate level. "We're not always happy. But by subtly changing the code, we get better results," he concludes.

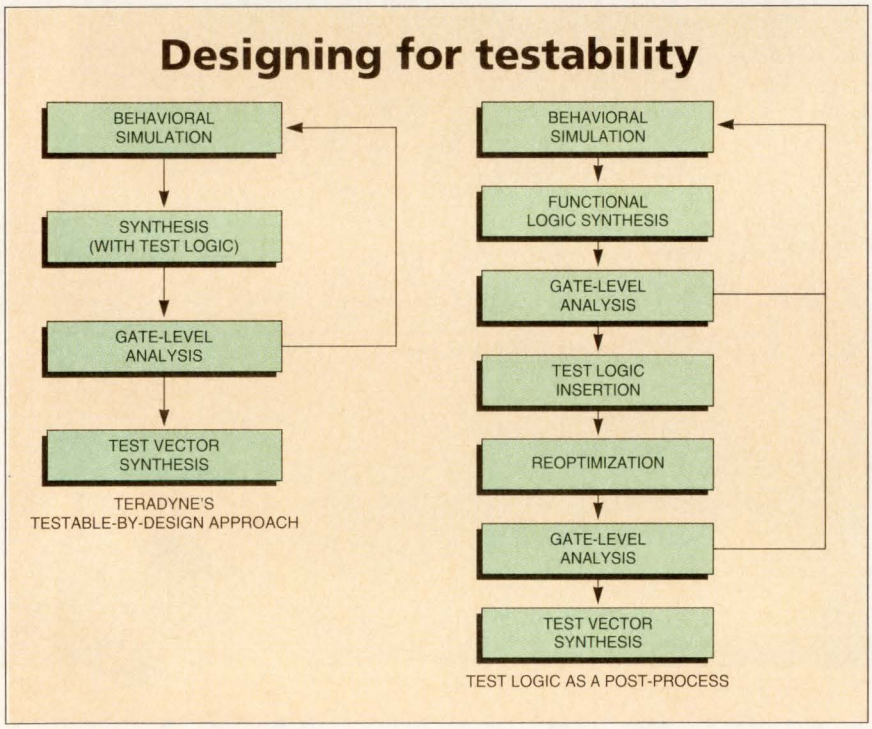
Though not in a position to quote fantastic returns yet, McBride says his group believes that VHDL will give them added value in time-to-market and right-first-time design. One of the main benefits of VHDL, according to McBride, is that it helps GPT reach its objective of using the same simulator, one geared to do system design and evaluation, in the ASIC and PCB arenas. "We can simulate an ASIC on a PC board without having fabricated the PC board or having gone to silicon with the ASIC," explains McBride. "If VHDL and a top-down process in the ASIC world can get us to the gate level with Cadat, moving then to the PC-board world is straightforward."

Partial to Cadat, McBride reports that Racal-Redac has integrated its VHDL 2000 simulator and SilcSyn II very well with Cadat. "The day has gone," he says, "when you can offer an engineer a point solution. Engineers are using tools much more interactively today and don't want to transfer data from one tool to another."

## Integrated design methodology

After evaluating VHDL simulators and doing some benchmarks a year ago, Andre Klap, manager of the EDA group at Hollandse Signaalapparaten, a division of Thomson CSF (Hengelo, The Netherlands), reports that his company also stuck with the simulator to which they were accustomed. With a strong belief in an integrated design methodology, Signaal uses Advansim from Dazix (Huntsville, AL) for board and ASIC simulation. When Signaal switched from the Dazix proprietary language to VHDL, it chose to go with the Dazix VHDL option. "It's not full VHDL, but we can simulate it on the the board," says Klap. With the VHDL option, Signaal can simulate VHDL, Dazix proprietary language, gate-level, and physical models all together.

When it came to choosing a synthesis tool, Klap and the engineers at Signaal did a lot of comparing of Synopsys with Racal-Redac. In the end, the company went with Racal-Redac's SilcSyn II "because of the structures of VHDL it supports and the way Racal-Redac interfaces with the silicon foundry," says Klap. Sig-




*This flow diagram illustrates the difference between a testable-by-design approach such as that taken by Teradyne EDA (Boston, MA) and an approach that inserts test logic as a post-process. By specifying test logic at the behavioral level, the designer has control over the logic and can simulate test control before implementation. Adding test logic as a post-process means that the VHDL source code doesn't accurately reflect what ultimately gets implemented. Teradyne EDA offers the Vantage VHDL simulator and Dassault Electronique's Frenchip VHDL synthesis to complement its own tools.*

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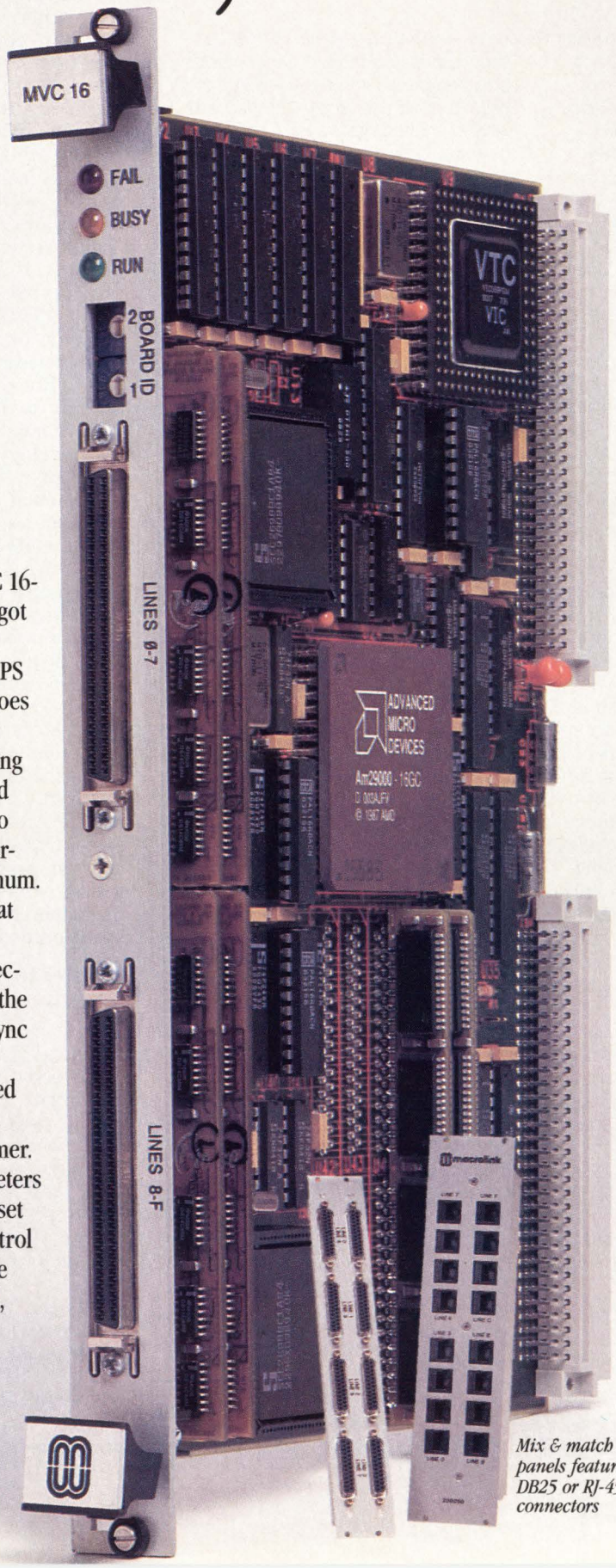


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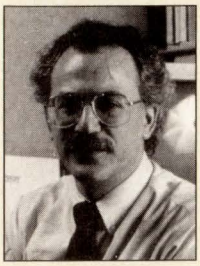
**CIRCLE NO. 40**

## *Timing representation in VHDL*



When the first formal language specification for VHDL was introduced in 1987, there was little doubt that during the next five years there would be much debate and discussion about what was in the language—and what was left out. Under the guidelines that govern an IEEE standard, the VHDL language specification will be reballoted in 1992, and many of the concerns raised during VHDL's initial acceptance period will be addressed. Significant issues to be postponed in VHDL 1992 include: analog extensions to the language, high-level predefined types (e.g., queues) and explicit notations for finite state machines.

Among the issues that will be addressed in the "new" VHDL, which will be voted upon on a first ballot in June, are: interfaces to other design and programming languages such as the Verilog hardware description language and C, clarification of I/O and file handling, improved visibility into nested packages, and the availability of hierarchical path names. While all of these hold the promise of a VHDL more usable to designers concerned with implementing a production-worthy VHDL-based design environment, perhaps the most critical need being addressed—particularly for ASIC design—centers around the issue of timing estimation and delay calculation.

### Timing and delay

The timing model in VHDL was developed to allow very sophisticated modeling of complex interprocess interactions which occur at the system level. The unique characteristics of this model allow timing computations to be freely mixed between behavioral and structural elements of the design. This flexible model, however, creates problems for typical ASIC designers since there's no industry-accepted standard practice for the representation of timing data in VHDL models and libraries.

Delay calculation and back annotation are typical applications where data—in this case, delay values—are specified in an external file that needs to be incorporated into the user's design. In order for VHDL to work effectively with ASIC models, a neutral format for technology-specific data is needed so that ASIC vendors can transmit data such as delay information in a simulator-independent manner. The IEEE has formed a working group to develop a methodology for accomplishing this goal.

Given the importance of this issue for ASIC design, this IEEE group will see significant participation from ASIC vendors. The chairman of the group, Vassilios Gerousis, is manager of CAD system evaluation at Motorola's ASIC Division. Many of the participants will bring valuable HDL experience. A standard delay file format developed for the Verilog HDL has been introduced as the straw man candidate with which the IEEE group will be working.

Essentially, the standard delay file (SDF) simplifies the number of utilities needed by a vendor to update the appropriate information in the design, whether for simulation or synthesis. For the user, this results in a common file that is portable. The SDF that has been proposed can be used by a number of tools and applications.

An SDF itself will not solve the problem of sharing timing information within a VHDL environment. Also needed—and being addressed by the IEEE working group—are standard access routines for VHDL for incorporating this information and additional constructs into the language to improve the representation of timing relationships. One such construct proposal that would benefit ASIC designers is the RELATION declaration and RELATION-specific statements. This construct, which conveys technology-specific information separate from functionality information, allows for the representation of pin-to-pin timing delays.

VHDL understanding and usage has come a long way since 1987, when the original language specification was introduced. Today, with the opportunity to improve on the language's shortcomings before us, the challenge is to apply our collective experience toward making a more usable design standard.

**Victor Berman,** chairman of the North American Chapter of VHDL Analysis and Standardization Group (VASG)

naal is using Fujitsu as a foundry. "Fujitsu has very strict clocking rules, but SilcSyn can incorporate the design rules within the library," Klap adds.

When Signaal ran its design through Synopsys, it had fewer gates than with SilcSyn, but the clock tree was unusable, according to Klap. "We're building naval combat systems," he explains, "so getting the design right the first time is more important than getting a small silicon area."

Test issues also became very significant as Signaal designers evaluated synthesis tools. Signaal didn't want ATPG from the third-party vendors, but it did want scan path accommodated to Fujitsu design rules. Racal-Redac built an option specific to Fujitsu into SilcSyn to accommodate Fujitsu's scan path methodology, according to Klap.

He says that at first it was hard to get used to working at SilcSyn's level of abstraction—what Racal-Redac calls the microarchitectural level. "We had to rethink ourselves and go up a level—so as not to think in terms of ALUs, but rather in terms of processes where we want to do additions. We did some manual decomposition of our ASIC. We split it up into 10 functional and manageable blocks and wrote a VHDL description for each one. We used SilcSyn as a black box—VHDL in and EDIF out." Klap reports that 12 of the 19 weeks of the design cycle were actually spent on design and the remaining seven on implementation, whereas previously only 30 to 40 percent of the cycle could be spent on design.

### Faster textual entry

A recent convert from Verilog to VHDL, Guru Raj, a member of the technical staff at start-up Adaptive (Redwood City, CA), echoes Klap's sentiment. "For 80 percent of the design cycle, there was no dependency on a silicon vendor's library," Raj says. Adaptive has just gotten back gate arrays from foundry LSI Logic after having used VHDL to design a 35,000-gate networking chip from the requirement specification. Raj used the Vantage VHDL simulator, Synopsys synthesis and Mentor's QuickSim with LSI Logic libraries for gate-level simulation.

With LSI Logic as his foundry, why didn't Raj purchase LSI Logic's Silicon 1076 VHDL simulation/synthesis design system, which is now

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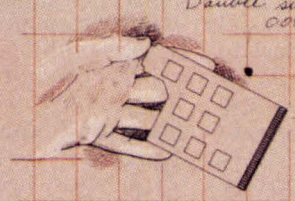
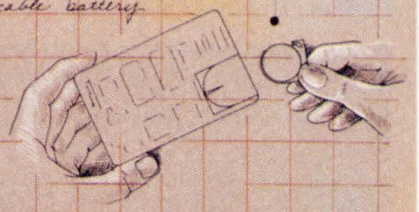
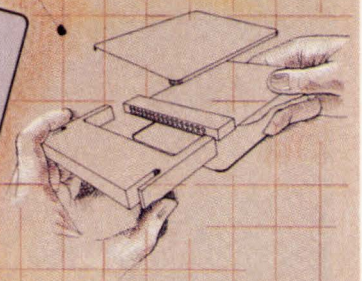
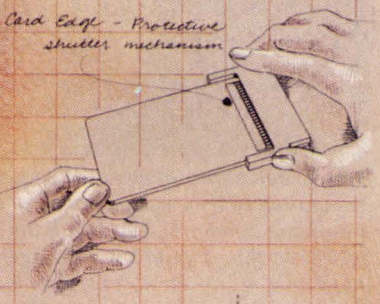



68 Pin and Socket (JEIDA)



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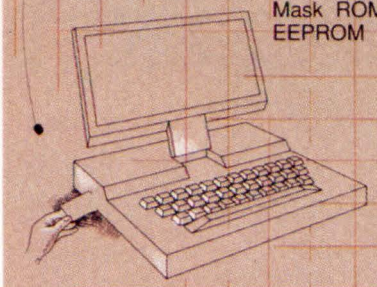


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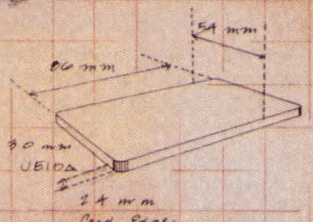
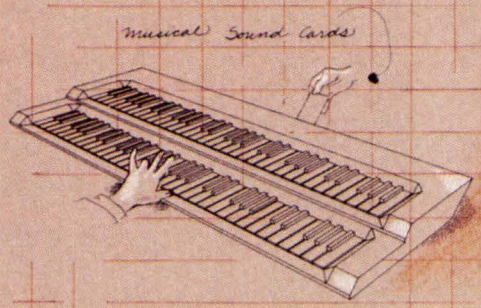
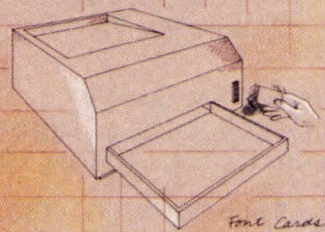
| EEPROM | 8kB | to | 32kB |





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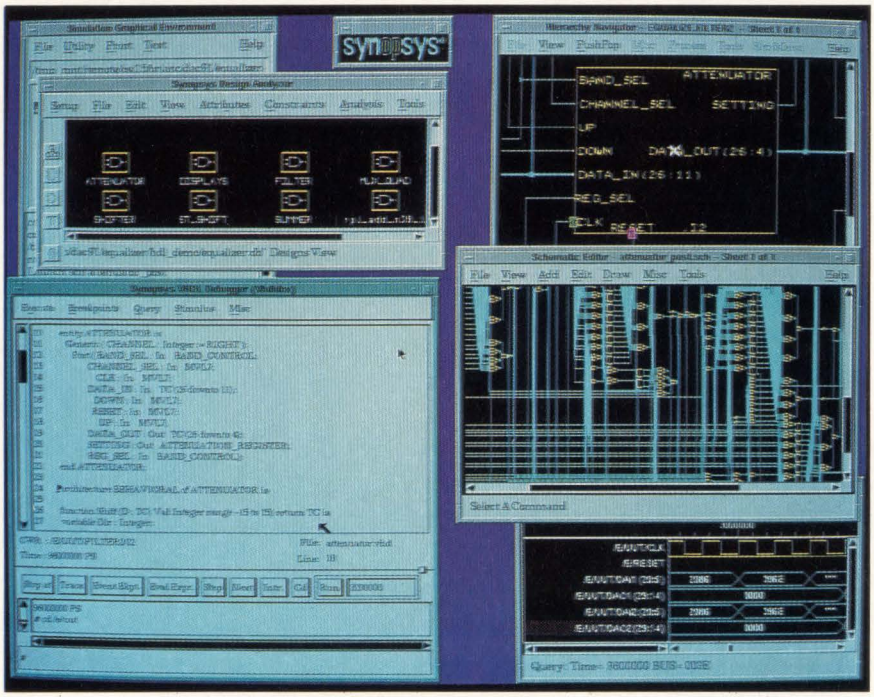
CIRCLE NO. 41

shipping to customers? "It's much too expensive for a few ASICs a year," he says. "It's not cost effective." LSI Logic has opened up its toolset so that users can interface to foundries other than LSI Logic by going back up through Synopsys synthesis, which is integrated into Silicon 1076.

Timing became top priority during the synthesis step, according to Raj. "How you break up your design and architect it is very critical to timing," he warns. "It goes back to whether you've architected your design correctly. It's where design experience comes in. The VHDL tools are still first-generation tools. You have to understand the tools to use them efficiently. They require a lot of iterations and a lot more handholding than you might expect."

Paul Tien, director of R&D at Arche Technologies (Fremont, CA), agrees with Raj that engineers have to take a more realistic view of the new VHDL tools, especially synthesis. "It's not a substitute for engineering knowledge," he says. "It replaces low-level knowledge—Boolean algebra and gate-by-gate design. Some engineers throw all sorts of specifications at the synthesis program and expect it to deliver a reasonable circuit." Engineers at Arche used Workview and Viewsim/SD with its VHDL compiler and analyzer, from Viewlogic (Marlboro, MA), to build the chips that went into the company's Legacy Series of workstations. Viewlogic, in turn, purchased Arche's in-house VHDL synthesis and migrated it into its own coresynthesis product called ViewDesign.




*This screen photo shows the Synopsys Version 2.2 integrated VHDL synthesis and simulation toolset being applied to the design of filters for a graphic equalizer. Both filters are being simulated with the Synopsys VHDL System Simulator, one at the RTL level and the other at the gate level using the transparent interface to Zycad's XP hardware accelerator. VHDL code for the RTL version of an attenuator in one of the filters can be seen in the VHDL Simulation Debugger window, and the filter blocks, including the attenuator, are shown in the Design Analyzer synthesis window. The waveform data (signal values flowing through both filters) is back-annotated into the VHDL simulator's Hierarchy Navigator.*

## Onward and upward

Dan Hafeman, vice-president of engineering at Ikos Systems (Sunnyvale, CA), also says that you have to know how to use the new VHDL tools to be productive with them. "It's very easy to screw up, especially with VHDL, but we're excited about the power," he comments. Hafeman's engineers are using Synopsys synthesis tools, as well as the Synopsys VHDL System Simulator, to design four 70,000- to 100,000-gate chips that will go into Ikos' next-generation hardware accelerator.

In the meantime, Ikos has entered into an exclusive arrangement with Racal-Redac to build the VHDL Accelerator, based on Racal-Redac's VHDL 2000. While Ikos has chosen exclusivity, competitor Zycad (Menlo Park, CA) has become a generic provider by coupling its XP family of accelerators to several VHDL simulators. The two accelerator vendors also differ in their approach to accelerating VHDL. Whereas the Zycad solution involves synthesizing the VHDL code to gates before accelerating, the Ikos/Racal-Redac solution takes the VHDL-synthesizable source code and translates it to run on a hardware accelerator without going through the entire synthesis process.

As users struggle to overcome the stumbling blocks to VHDL design, VHDL International and the IEEE are promoting standardization of tools and models. Users are likely to see across-the-board compliance with the full VHDL specification, as well as the adoption of the nine-state value system for models, well before they see a solution to the much bigger problem of timing representation. ■

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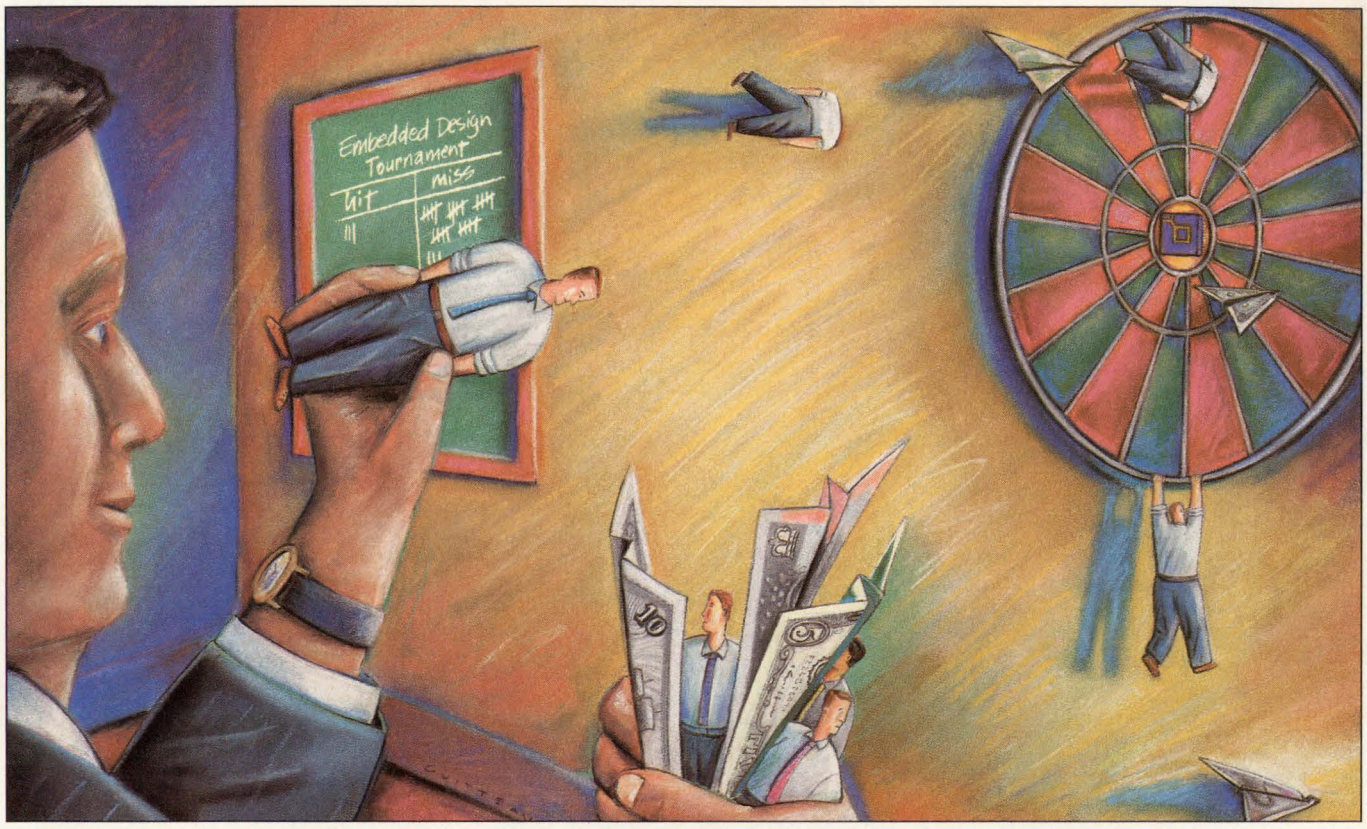


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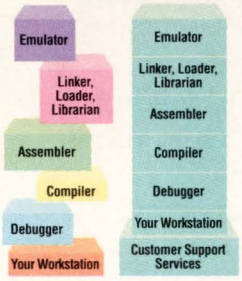


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CIRCLE NO. 43

# RISC is simple, but benchmarking isn't

***Measuring the performance of RISC-based designs is a lot like benchmarking traditional processors—only worse.***

**Tom Williams,**
**Senior Editor**

***Performance measurement tools for real-time systems can be used to test relative performance of systems and software. The Real-Time Tester from Modcomp lets you select a number of real-time processes in a pipeline and pass data through them. The data then forms an image at the end of the pipeline. Watching the image grow gives you a feel for the speed of the system.***

**B***enchmark -n. 1. A surveyor's mark made on a stationary object of previously determined position and elevation and used as a reference point in tidal observations and surveys. 2. A standard by which something can be measured or judged."*

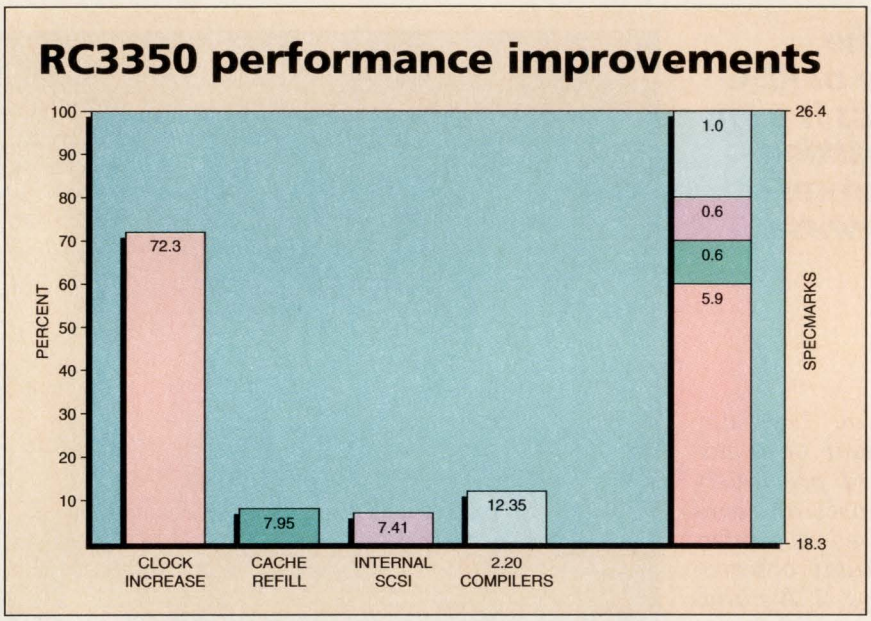
***—The American Heritage Dictionary***

Most people react with suspicion to benchmark data published in sales and marketing literature, and rightly so. Competitive benchmarks published by vendors that show their products in comparison to others very frequently result in rebuttal papers that point out how the results were skewed—intentionally or otherwise—in favor of one processor or another. If one ran *truly* comparative benchmarks, the results would look quite different. The question harks back to the dictionary definition. What is the "previously determined position and elevation" and how is the reference measured?

In terms of the competitive struggle between CPU vendors, that question may never be finally answered, and so the use of benchmark data as a sales and marketing tool will always be a slippery subject. Even so, designers will continue to use benchmarks to help decide which CPU to use for a given project. But benchmarks have another, more significant use—as engineering tools increasingly important to system designers as processors become faster and more complex and as system design decisions play an ever-greater role in determining overall performance.

The advent of RISC architectures and very high-performance CISC CPUs has made the supporting system design even more critical to deriving the full potential of the CPU. It does no good, for example, for a processor to be able to execute at one cycle per instruction if it can't get the instructions from memory at that rate. The complex interplay of CPU architecture, cache design, I/O design, memory system design, compiler technology, and the specifics of the application all influence system performance. Today's benchmarks must aid the CPU designer in building chips that will operate optimally within feasible system memory and I/O architectures. They must also help you, the system designer, make cost/performance decisions when designing the new generation of CPUs into products that will run real applications.

Benchmarks today are focusing less on measuring one isolated aspect of performance, such as Dhrystones per second, and more on overall system performance. What should concern you is how modifications in some aspect of the system (such as CPU, cache or I/O) affects overall performance. Ultimately, the only true test of a system is how well it runs a given customer's application. But somewhere between basing performance judgments on isolated aspects of the CPU and attempting to design full-custom application-specific systems, there has to be a convenient and meaningful metric. Such a metric can't by definition be ideal but if it can be a benchmark in the true sense of providing a stable reference against which performance trade-offs can be measured—and telling you *what's* being measured, it can be a vital tool in the day-to-day task of system design and engineering.




***The 100 percent scale on this graph represents a 44 percent improvement of the 33-MHz MIPS RC3350 RISC CPU board over the 25-MHz RC3260—from 18.3 Specmarks to 26.4. That improvement represents more than a change in clock speed, which as shown here, accounted for 72.3 percent of the improvement. Other factors included a change in the cache design, addition of an on-board SCSI controller and improvements to the compiler.***

## Toward a level playing field

Trying to get a handle on the performance characteristics of today's high-performance CPUs has, of course, never been as straightforward as measuring Mips or MFlops. Many processors have internal pipelines that need to be fed and which can stall under a variety of circumstances. And almost all the modern RISC and CISC processors have on-chip cache memory and demand secondary caches to keep them fed with instructions. The smaller, more familiar and traditional benchmark programs—such as the Whetstone, which measures floating-point performance; the Dhrystone, which measures a general mix of instruction execution; and the Linpack may give an indication of the internal execution speed of the processor, but that can be a misleading indication of how the CPU will run in any real system.

Given today's primary cache sizes, the "WDL" trio is prone to give misleading information because these benchmarks can execute entirely within the cache, which isn't the case for real-world applications. Tim Olson, manager of 29k system hardware for Advanced Micro Devices (Austin, TX), calls such benchmarks "reductionist" because, by focusing on their results, "you lose the forest for the trees." Getting good floating-point performance while running out of the cache doesn't necessarily indicate how an application will perform if the data it needs isn't in sequential memory locations and available at zero-wait states. That will involve a lot of cache misses and main memory accesses, which will considerably slow performance.

In addition, says Olson, these benchmarks can be "prone to some compiler optimizations that totally modify the effect of the benchmark, whereas in very large, realistic programs there isn't much of an effect." For instance, he notes that in the Dhrystone 1.1, several optimizing compilers "totally threw one multiply and one divide out of the outer loop because they weren't used anywhere and that biased what Dhrystone was trying to do in terms of relative frequency of operations." Performance figures on processors, especially RISC processors, are never going to be free of the effects of compiler technology, but the newer benchmarking techniques attempt to take the effects of compiler optimizations into consideration in evaluating performance.

## Popular but not perfect

Today's most popular suite of general benchmark programs—although all involved admit it isn't perfect—is the Spec benchmark suite established and maintained by the Systems Performance Evaluation Cooperative (Fairfax, VA). Spec is currently a cooperative of 22 companies established to endorse a standardized set of relevant benchmarks that can be applied to the next generation of high-performance computers.

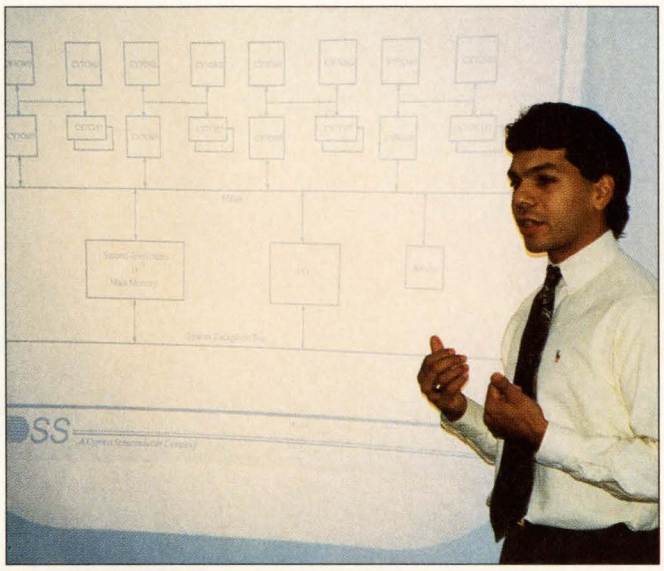
The Spec Benchmark Release 1 consists of 10 programs that are real applications and are large in comparison with earlier benchmark programs—on the order of ¼ megabyte of code. According to Robert Novak, product marketing manager for MIPS Computer (Sunnyvale, CA), "the Spec benchmarks were specifically designed to make sure they would bust primary caches." He adds, however, that the current Release 1 is still CPU-intensive because it tends to emphasize computation functions and performs relatively little I/O. Nevertheless, because real-world programs need more data than normally fits into the cache and must often make nonsequential data accesses that go outside it, the Spec programs are more useful for evaluating designs for actual applications.

Even though the current Spec suite is oriented toward scientific and engineering applications—as opposed to commercial applications such as large databases—and given

that it has admitted limitations, there appears to be quite a bit of acceptance of it among the design community. Matthew Gutierrez, senior applications engineer for Ross Technology (Austin, TX), a subsidiary of Cypress Semiconductor (San Jose, CA), comments that "in our opinion, they're not the perfect benchmarks but they're still the best thing out there in terms of standardization and in terms of running real applications."

The Spec cooperative, for example, controls the source code for the benchmarks and doesn't allow alterations. In addition, Spec insists that commercially available compilers be used so that the effects of optimization can be recognized—and so some vendor doesn't get to show results that come from an in-house compiler to which nobody else has access.

Still, there are caveats. Trevor Marshall, chairman of the board and CEO of Yarc Systems (Newbury Park, CA), notes that "Spec is becoming less useful these days because the large manufacturers are spending money and effort on optimizing their compilers so they produce better Specmark figures." MIPS' Novak cautions that the nature of the Spec benchmarks and what might be added to them could potentially influence the design of future CPUs in ways that might not be to the ultimate advantage of applications. "The only thing that benchmarks have ever measured is the performance of benchmarks," Novak says.



*According to Ross Technology's Matthew Gutierrez, Spec benchmarks are useful in testing cache and CPU core designs. "Given a stable memory and I/O environment—realizing that it doesn't represent a real or optimal system environment— you can get useful information about cache and core CPU design trade-offs."*

## Measuring CPUs and systems

Perhaps the biggest concern of designers building high-performance RISC-based designs is the cache memory. Cache is almost a given in any RISC-based design today because it's absolutely imperative to keep the processor pipeline fed with instructions if the chip is to meet its performance potential. Cache considerations are important for the CPU designer in determining the cache interface, line size, fill, and other parameters of the CPU; they are also important for the user who is trying to design the chip into a system with on-board secondary cache and I/O. Both can use benchmarks as an engineering tool to mark a known performance level and then to examine the effects of design alternatives against that initial benchmark. If a design change affects the benchmark numbers, you know you've done something.

It's possible, then, to attribute performance changes to different factors. MIPS Computer, for example, measured the performance improvement of its 33-MHz RC3350 CPU board over its 25-MHz RC3260 as a 44 percent increase based on Spec benchmarks. Of that 44 percent increase, the bulk of the improvement—72.3 percent—was due to clock frequency. MIPS had also plotted the effects of varying the cache-block refill size and varying the size of the cache as well. It actually realized 7.95 percent of the overall performance improvement by reducing the refill size from 16 to eight words. The MIPS team attributed another 7.41 percent of the total performance increase to the use of an on-board SCSI controller—to the extent that the Spec suite exercises I/O in comparison with real-world applications. Another 12.35 percent of the improvement was due to enhancements in the compiler technology.

While Specmarks are the geometric mean of the entire benchmark suite results, it's also possible for you to look at the results of individual programs and draw conclusions about the possible suitability of different design alternatives for a given application. Ted Kubik, software engineer for Omnibyte (Chicago, IL), notes that sometimes the most favorable cache/memory configuration depends on the application. "We've tried to offer a variation so our customers can look at the benchmarks and try to fit the price/performance and cache/main memory configuration to fit their application."

Yarc Systems, which produces Am29000-based coprocessor cards for the Macintosh and AT buses, has put together its own in-house set of benchmarks that president Trevor Marshall, who already has expressed reservations about the Spec suite, says are quite handy for evaluating the effect of the cache. "They're small, very simple benchmarks that grow in size. You plot the time taken for each size and you can see where you go outside the cache and see where the machine 'goes virtual,' where it runs out of RAM." But even here, you must pay attention to the kind of application you have in mind. "Compilers lend themselves to cache because they tend to be very sequential, but if you're dealing with ray tracing or Postscript there's a lot of random accessing and the cache becomes less effective," he adds.

## Applications count

Ultimately, most people agree that the proof of the pudding is really in the customer's application. And increasingly, customers are approaching vendors with their actual applications before committing to a purchase. Borko Furht, senior director of development and advanced research for Modcomp (Fort Lauderdale, FL), says, "That's the way customers are going. Today you can't just go to the customer and say, 'OK, I have the best machine and this is 50 Mips.' They want to really make sure you meet their requirements."

Furht says his company has run at least 35 to 40 customer benchmarks in the last four months. "It's especially important in the real-time

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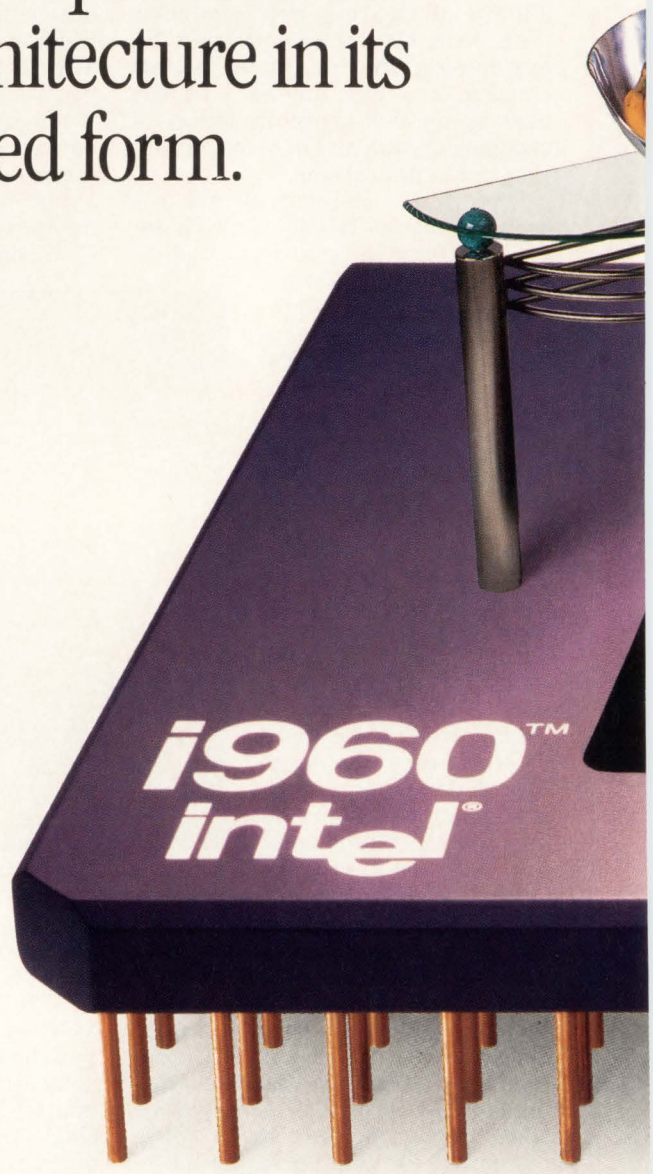


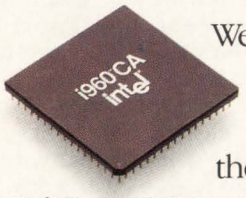


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## The Spec Benchmark Suite, Release 1

**001.gcc35**—C compiler benchmark that measures time-to-convert source code into optimized assembly language files.

**008.espresso**—A program for generation and optimization of PLAs. Relatively small and manipulates arrays and loops. Exercises storage allocation and is sensitive to cache size.

**013.spice2g6**—An analog circuit simulation tool that uses double-precision floating-point data. While not itself floating-point intensive, the program's many data accesses cause a high rate of cache misses.

**015.doduc**—A high-energy physics simulation that uses 64-bit floating-point numbers. Does little I/O but many short branches, loops and subroutine calls.

**020.nasa7**—A Fortran program that tests common scientific equations in double-precision floating-point. Data accesses cause high cache misses on some platforms.

**022.li**—A Lisp program written in C and a CPU-intensive integer benchmark that solves the 9-Queens problem. Recursive algorithms challenge register window architectures.

**023.egntott**—CPU-intensive integer benchmark whose primary computation is sort operations.

**030.matrix300**—Double-precision floating point that exercises a Linpack routine on matrices of order 300. Data accesses can cause significant cache misses.

**042.fpppp**—A double-precision Fortran quantum chemistry benchmark, including a very long basic block that challenges many compilers.

**047.tomcatv**—A highly vectorizable Fortran mesh generation program. Favors superscalar and vector machines and can cause high data cache misses.

- The **Specmark number** is the geometric mean of the benchmark suite results. The geometric mean is fairer than the arithmetic mean because it compensates for isolated Specratio extremes while giving each program equal importance.
- The **Specratio i**s the result of dividing the Spec reference time by a machine's run time for a benchmark.
- The **Spec reference time** is the time it takes to run a benchmark on a DEC VAX 11/780 machine.

environment," he says. "Maybe in straight number-crunching you can rely on the Spec benchmarks." But Spec doesn't let you simulate the inflow of external events or measure interrupt latency, I/O setup times and other things that are vital to real-time. Here, the designer and customer are still pretty much on their own to devise in-house measurement methods. There's certainly no commonly agreed-on standard comparable with the Spec suite for real-time.

Modcomp has devised a set of measurement tools for its internal use which it's now making available to its customers and will be selling commercially. One, the Real-Time Tester, runs under real-time Unix systems; it's a program that consists of a high-priority head process, a number of lower-priority real-time processes and a tail process.

Data is taken in by the head process and passed to a pipeline containing a user-selected number of successive real-time processes, where one process activates the next one as it passes the data along the pipeline. Each transfer causes a full real-time context switch. The tail process displays the data as an image. The speed of image generation can give an intuitive feel for the performance of the system. In addition, the Real-Time Tester measures context switch time, interprocess communication and synchronization, the file I/O system, and Unix system calls.

A second tool from Modcomp is the Tri-Dimensional Analyzer, a PC-based system that measures three interdependent aspects of a real-time computer. The system contains interface software and software for measuring the performance of the computer under test. It also includes a board for generating interrupts, controlling the I/O and measuring the CPU speed of the system under test. A software package called Cue runs on the system under test and contains benchmark routines, interrupt handlers and I/O tasks. The output of the Tri-Dimensional Analyzer is a three-axis graph displaying the relative performance of CPU in Mips, interrupt handling in millions of interrupts per second, and I/O throughput in millions of I/O byte transfers per second.

### Compilers, RISC and benchmarks

There's no doubt that a good optimizing compiler can dramatically improve the performance of a system. The amount of improvement is dependent on many factors, such as the kinds of optimizations used and the nature of the application. Compiler optimizations, therefore, can improve the benchmark performance as well. The Spec cooperative has recognized this and allows for it, since many optimization techniques are not processor-dependent. Op-

### SELECTED RISC SYSTEM PERFORMANCE

| SYSTEM TYPE | 001.gcc | 008. espresso | 013.spice 2g6 | 015. doduc | 020.nasa7 | 022.li | 023. egntott | 030. matrix300 | 042. fpppp | 047. tomcatv |
|---|---|---|---|---|---|---|---|---|---|---|
| OMNIBYTE VR3000 128K/16M 25MHz R3000/3010 | 90 | 124 | 1736 | 107 | 1056 | 299 | 61 | 496 | 150 | 165 |
| OMNIBYTE VR3000 32K/16M 25MHz R3000/3010 | 108 | 134 | 2065 | 120 | 1160 | 331 | 64 | 523 | 328 | 170 |
| OMNIBYTE VR3000 128K/8M 25MHz R3000/3010 | 431 | 125 | 1861 | 109 | 1093 | 309 | 63 | 525 | 177 | 175 |

*Different cache and memory configurations for the Omnibyte MIPS R3000-based CPU board show different performance characteristics for various Spec benchmark routines which may be indicative of applicability to different types of applications. Units in table are seconds to complete benchmarks.*

timizations such as removing loop invariants or in-lining subroutines will yield performance improvements across processors and can thus be used and still maintain an "apples-to-apples" comparison.

## Fine-tuning compilers

There are, however, certain aspects of processors for which an intimate knowledge of the hardware can let the compiler be fine-tuned for optimal performance. MIPS, for example, in a "chicken-and-egg" scenario has developed its R3000 and R4000 CPUs concurrently with its compilers—and has developed the compilers concurrently with the CPUs. MIPS understands the latencies in each pipeline and can tune the compiler to launch instructions exactly timed to their length and the internal latencies of the chip.

The Sparc community doesn't have quite the same luxury, since a Sparc processor isn't defined as a mask set but as an implementation of an architectural specification. "The stress in the Sparc architecture," says Ross Technology's Gutierrez, "is on compatibility, not clone-ability. And that's software compatibility." A benchmark will run differently on each implementation of Sparc. "In reality," he adds, "the first generation of Sparc architectures was based on the core design of the integer unit. The performance differences were not so great."

But Sparc is proliferating to a wider number of implementations, with different cache designs, implementations of the floating-point unit and so on. It's even available in multichip modules (MCMs), which as integrated units will exhibit their own unique performance characteristics. And even now there are performance differences between existing implementations. You can expect that more diverse Specmark numbers will begin to emerge among the various implementations, and also that eventually some Sparc compilers will be tuned for specific implementations to take advantage of individual hardware characteristics. When that happens, Sparc performance figures will have to be more closely scrutinized with the knowledge of which implementation and compiler combination are at work.

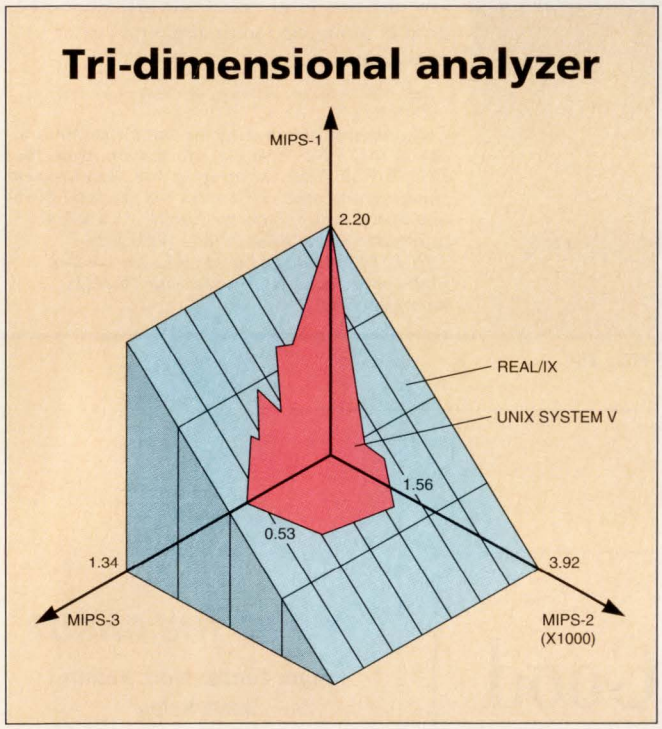
Of course, another way to factor out the effects of a compiler is simply to look at the clock speed and the number of cycles per instruction (CPI) a processor executes. M. Somasundaram, director of embedded control for Fujitsu Microelectronics (San Jose, CA), notes that benchmarks he has run on the Sparclite using different compilers and benchmarks show a relatively invariant number in terms of CPI. Such a number is good to keep in mind when looking at the effects of optimizing compilers on benchmark times. "So now if we do the same thing for MIPS, 29K, etc., we might have a better way of figuring out how a customer's code might work," he says. This is because no matter how that code has been optimized, a customer knows that his compiled application has X number of instructions. "And he's really interested in how fast he can run that X number of instructions," says Somasundaram.

The effects of compiler technology on performance become more significant when RISC designs are implemented as superscalar architectures, which have several computational resources in parallel and are therefore capable of executing more than one instruction during a single cycle. A good compiler must schedule instructions so that all the parallel units (for example, adder, multiplier, address unit) are kept as busy as possible, ensuring the minimum number of CPI.

## Superscalar hard to measure

Superscalar compilers have to be implementation-specific to be efficient. An unexpected problem can arise, as Ross' Gutierrez points out, when a compiler optimized for a processor implementation that launches two instructions every cycle (i.e., has two parallel resources) is used on a CPU implementation with three parallel units. The compiler optimized for the two-unit machine (e.g., adder, multiplier) would make sure that two add instructions were not back-to-back, both wanting to use the adder. The next add instruction would follow by at least one instruction.

If that same compiled code were run on a machine that launches three instructions at a time, you might not see much of a performance improvement because two add instructions might be launched at the same time when the CPU launches a set of three instructions in parallel. You would want a compiler that would, say, launch an instruction group containing an add, multiply, load instruction (avoiding an add, multiply, add grouping) and schedule the next add for the next launch so as not to compete for the adder and stall the pipeline. Given the subtleties of superscalar architectures, it will be necessary to use benchmarks not only to judge the efficiency of the CPU but the efficiency of the compiler as well. This




*The Tri-Dimensional Analyzer from Modcomp shows relative throughput for CPU (MIPS-1), interrupt handling (MIPS-2) and I/O throughput (MIPS-3) for a real-time system. This graph compares real-time performance of Unix System V (red plot) with the Real/IX version of Unix designed for real-time. Real/IX shows a much more symmetrical relationship among the three parameters.*

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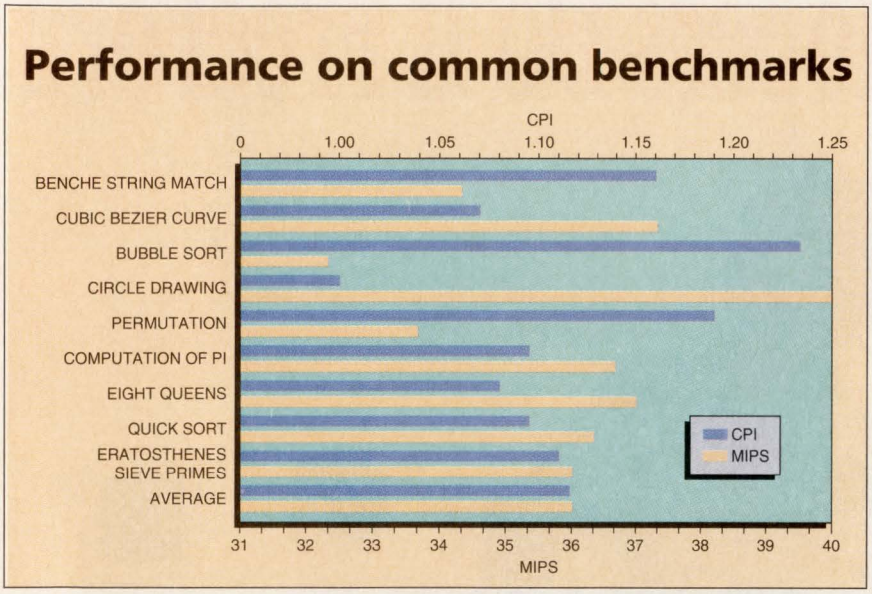


*Different benchmarks run on the Sparclite processor at the same clock speed show relative invariance in terms of cycles per instruction (CPI). Fujitsu reports this same invariance over several different compilers, although the completion times for the benchmarks vary because of compiler differences.*

will be further complicated by the fact that the efficiency with which even the best compiler can schedule instructions for a superscalar processor is highly dependent on the application code.

But the idea of improving actual application performance—let alone measuring it—by using a superscalar architecture just brings us back to the memory issue that's so much a part of RISC design. Fujitsu's Somasundaram points out that "launching three instructions and doing three data fetches only makes the memory problem worse. It's hard enough to keep one pipeline filled, now imagine three pipelines." There's probably some crossover point in the size of the cache, he says, where going to superscalar will offer significant improvements. But the kind of application being run can throw such considerations into a cocked hat. "Superscalar doesn't solve the problem of image processing because it's not sequential enough that the data can be brought into the cache in good order," he comments. So if the choice is between having cache or going superscalar, the choice for Somasundaram is cache, "because if you don't have cache, you need at least two cycles to do an external access."

## Prospecting for performance

Whether superscalar or not, the internal details of RISC architectures hold nuggets of performance improvement for those willing to go prospecting. While porting its C Executive real-time kernel to the Intel i960, JMI Software Consultants (Spring House, PA) recently discovered a way to significantly improve the context switching performance of the processor that even the chip's creators at Intel hadn't thought of.

The i960 uses a state bit to keep track of whether it's running a user task or servicing an interrupt. Normally, when the i960 is servicing an interrupt and then needs to switch to a higher priority task as the result of another interrupt, it must copy task context information to a task control block to keep it from being overwritten on the interrupt stack.

One of JMI's software engineers realized that by inverting the use of that status bit, the processor could be fooled into thinking it's already on the interrupt stack, when in reality it's on a user task stack executing a user task. When an interrupt occurs, the status flag changes to indicate that the processor is executing a user task (when it's really servicing an interrupt). When the next and successive interrupts occur, the processor saves task data on the interrupt stack and doesn't copy it to a task control block, eliminating a significant number of instructions and memory accesses. JMI determined that for a process interrupt with task preemption, its technique required 13 fewer instructions, including flushing the registers, and 33 fewer memory accesses than the procedure in the i960 manual. Just how such an improvement will affect the actual performance of an application is, of course, dependent on the frequency and type of interrupts involved, but it shows how important intimate knowledge of RISC hardware can be to squeezing out performance.

Getting a true picture of the performance characteristics of a CPU has never been a straightforward proposition. The fundamental problem is that system designers must produce CPUs and systems that deliver high performance over a wide range of applications, while users are looking for optimal performance for their specific applications. A good set of benchmarks helps both sides grope toward a middle ground. The emergence of the Spec benchmark suite has been generally accepted as an advance in performance evaluation. But you will want to use more specialized metrics for looking at other performance characteristics, especially real-time. And everyone, vendor and customer alike, must be constantly aware of all the factors that can go into producing a set of numbers—because, as MIPS' Robert Novak puts it, "the decisions you make are only as good as the programs you use for the measurements." ■

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CIRCLE NO. 47

# Multiprocessing to bring the next jump in performance

Warren Andrews, Senior Editor

***As microprocessors come up against physical and architectural limits, multiprocessing may finally emerge to lead the way to the next level of computer performance.***

By whatever name it's known, from distributed processing to tightly coupled, multiprocessing involves a single concept: it's an effort to increase system performance by using more than a single processor.

This concept isn't new. At some level it's been around as long as computers have. Minicomputers, mainframes and supercomputers have taken advantage of some sort of multiprocessing for many machine generations. But it's been the emergence of the microprocessor that's brought new meaning to multiprocessing. This may seem ironic, since on the one hand the advent of the microprocessor has retarded the development of multiprocessing, yet on the other hand it's set the stage for what's being forecast as the most dramatic advance in computer performance ever realized.

## No pain, no gain

The gains won't be free, though. Most likely the great potential shown by multiprocessing architectures will be realized slowly as hardware and software companies struggle to overcome seemingly insurmountable obstacles while trying to retain compatibility with existing structures. But the march to multiprocessing has already begun, as witnessed by the announcement of any number of board-level systems, application accelerators and array processors, RISC-based graphics and supercomputers—not to mention the latest server, Galaxy, from Sun Microsystems.

"Progress toward multiprocessing using single-chip microprocessors has been thwarted," says Bill Kehret, president of Themis Computer (Pleasanton, CA), "because silicon makers were just too good. Each time a technique for doing multiprocessing on a microprocessor-based system started to be developed, a next-generation processor would emerge that outperformed even the anticipated gains of the multiprocessing approach." But fundamental physical limits are being reached, and perhaps the higher costs of the exotic levels of processing needed for faster parts are driving designers to look to architectural enhancements such as superscalar designs and multiprocessing to gain performance.

## Leapfrogging

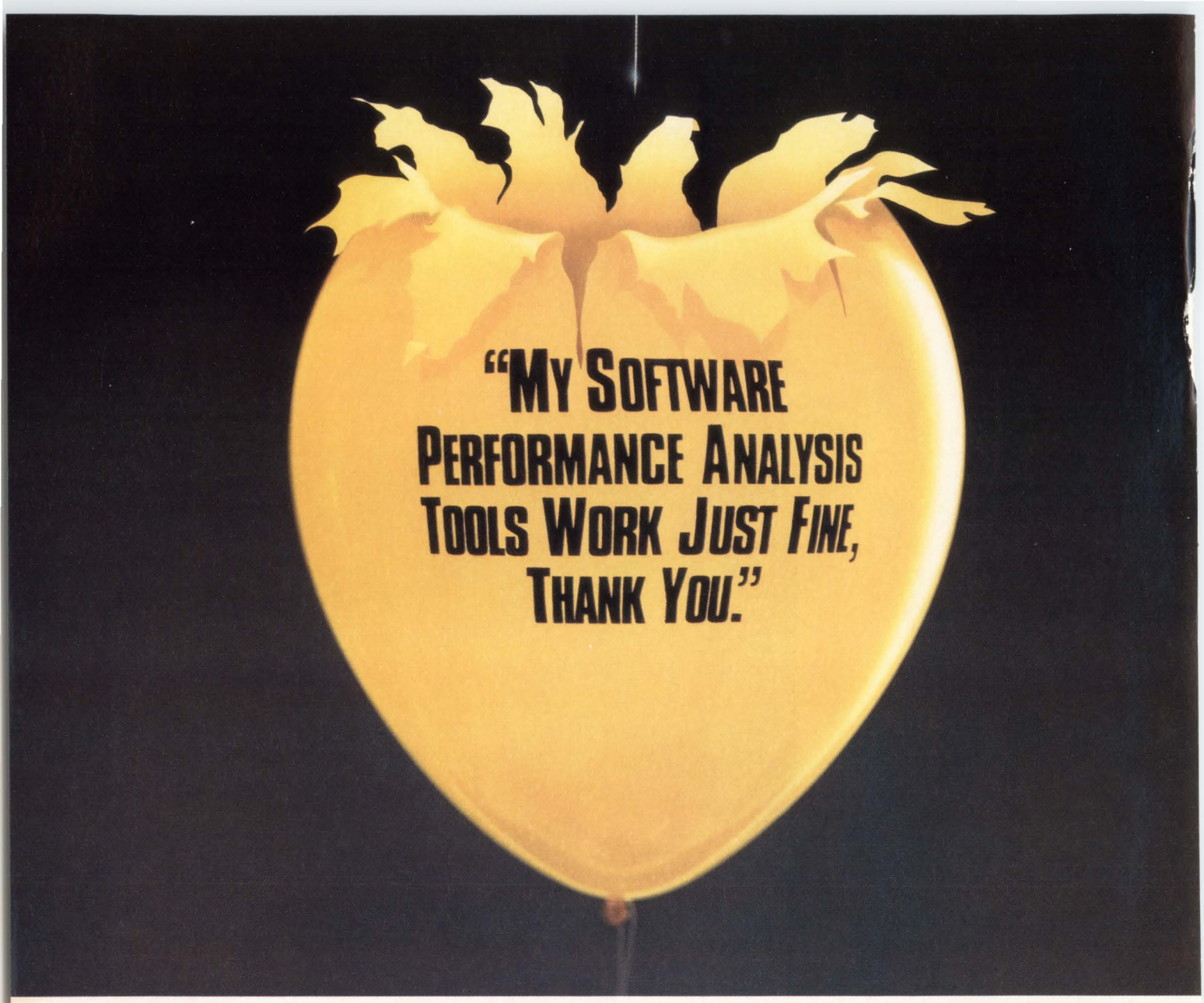
At least two events have mitigated processor gains and enhance the likelihood that multiprocessing architectures will emerge at the top of the heap. First, dramatic gains in microprocessor performance from generation to generation are slowly eroding as the laws of physics become increasingly larger obstacles. Clock speeds of 40+ MHz are now in production, and speeds will jump to as much as 100 MHz over the next three to five years. This is a big increase, but not of the same magnitude as previous gains—say, the jump from three to 12 MHz, which took place over a corresponding time period. At the same time speeds were increasing fourfold, datapaths and address space were moving from eight to 32 bits. The biggest jump current-generation processors can expect is from 32 to 64 bits.

Other factors, such as the increase in number and type of registers, the use of pipelining and the trends toward RISC and superscalar architectures, have also contributed to the advances in processor performance over the past several years. It's unlikely that similar architectural approaches will yield the same gains in single-processor systems of the future. The rate of performance increase in future generations, therefore, isn't likely to parallel that realized in the

past few—and yet users have become accustomed to tremendous performance gains from generation to generation.

The second factor, equally important in the evolution of multiprocessing architectures, is the role played by increasingly complex applications, which have grown dramatically in number over the past 10 years. On one hand, new and more complicated tasks have to be performed. On the other, program size has mushroomed as programmers take advantage of relatively inexpensive memory and fast processing capabilities to simplify the programming task. These gains have made it possible for computers to be applied to entirely new tasks, such as signal processing and image manipulation.

Perhaps there's also a third impetus to the rapid evolution of multiprocessing—particularly in the standard-bus, board-level arena—and that's a sharp drop in the number of users willing to accept proprietary solutions, such as minicomputers, compared with those looking for open systems. These users range from commercial ones involved in data processing to industries with control applications through military electron-

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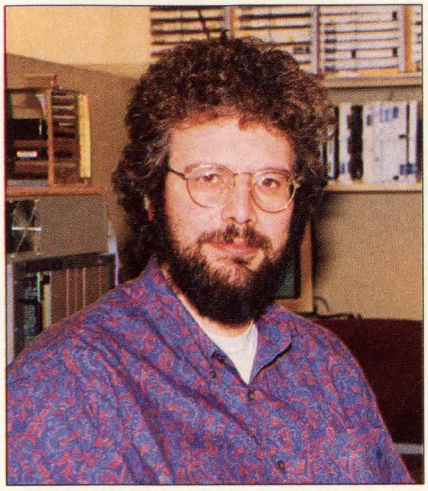
ics, which is beginning to mandate systems based on standard hardware and software—in many cases, standard buses such as Multibus II, VMEbus and Futurebus+.

## Multiple levels of processing

Multiprocessing architectures are diverse and it's difficult to determine where each one fits in the continuum from chip to module, module to board, board to system, and system to network. "Multiprocessing can take place at any number of different levels," says Thanos Mentzelopoulos, engineering product manager for Ironics (Ithaca, NY), "though the fundamentals are largely the same. That is, at its simplest level, a number of processors are put to work on a single task sharing some level of common resources."



*Thanos Mentzelopoulos, engineering product manager for Ironics, defines multiprocessing as "a number of processors put to work on a single task sharing some level of common resources."*

At the next level of architectural complexity, you have to determine what resources are to be unique to each processor, duplicated for each processor and shared in common, observes Mentzelopoulos. "For example, in its simplest incarnation, a multiprocessing system might comprise a number of personal computers networked together. Common resources might include certain I/O functions, but basically each processor has all its own resources, including memory, its own copy of an operating system, power supply and other resources of a standalone system."

Linking processors a little more closely, a number of single-board computers can reside on a backplane, sharing some resources, yet maintaining enough independence that each board has its own memory and an operating system. Such systems can also share a global memory and frequently share I/O. Each processor has its own task and operates on that task, passing the result along to another processor. Because each processor operates relatively independently of its neighbors, this approach—as well as the networked approach—are referred to as loosely coupled, or distributed-memory, approaches.

## The highest level of all

At the next level are tightly coupled or shared-memory multiprocessing architectures. In this approach, processors share a common memory space, operating system and all other system resources. Individual tasks are divided into subtasks, such that each processor operates on one segment of a task. While tightly coupled multiprocessing is viewed as having the greatest potential for performance gains, it's not yet a viable approach outside of certain specific applications where it's possible to write painstaking multithreaded programs with processor segmentation written into them. Furthermore, some applications are better adapted to loosely coupled systems.

While there are several commercial examples of tightly coupled multiprocessing architectures—the most recent being Galaxy server from Sun Microsystems (Mountain View, CA) and machines from NCR, Sequent and Stratus—they have thus far been limited in application because they lack effective software. There are a number of operating systems with at least some multiprocessor hooks included—such as SCO Unix, Mach, Unix System V Release 4, and SunOS—but they are unable to do more than very coarse processor allocation at this time.

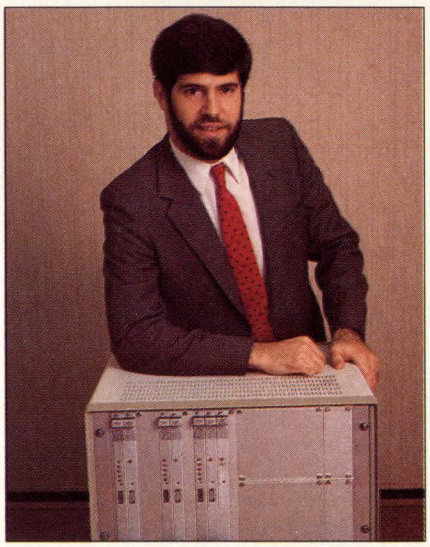
In the real-time arena, a couple of preliminary approaches have been introduced. The multiprocessing version of Lynx/OS from Lynx Real-Time Systems (Los Gatos, CA) and Realix from Modcomp (Ft. Lauderdale, FL), for example, both claim conformance to the emerging Posix (Portable Operating System Interface for Unix) standard.

Most of the commercial multiprocessing today, particularly that involved in real-time applications, falls somewhere between networked and tightly coupled applications. Lynx has created its own taxonomy, calling networked systems loosely coupled, shared-memory systems tightly coupled and board-level approaches "snugly coupled." The "snugly coupled" definition, however, is somewhat blurred beyond specific boundaries and its applications fit more comfortably in the general category of loosely coupled systems.

There's no particular limitation on how systems can be assembled. Different processor configurations can be combined in a mix-and-match fashion to achieve optimum performance. Ironics, for example, has developed a Sparc-based VMEbus board which can incorporate multiple processors interconnected over the Sparc M2 bus in a tightly coupled multiprocessing configuration. Ironics has also put together systems where multiple boards are plugged into a backplane in a loosely coupled fashion while allowing multiple crates to be interconnected using a standard network or proprietary protocol.

## Hardware/software trade-offs

As with any system, there are both hardware and software issues that determine the efficiency and applicability of any particular design ap-



*Radstone's Joel Silverman advocates the use of multiple datapaths in multiprocessing environments where heavy data-flow requirements are evident. Radstone offers a variety of different data avenues on its CPU boards, including VSB (VME subsystem bus), SCSI, Ethernet, a mezzanine bus, and a number of local buses on-board to keep the main processor free of unwanted interruption.*

# Interface chips applied to multiprocessing architectures

Interface chips have several advantages for the board designer. They can reduce parts count and lessen the complexity of the design, simplifying testing and decreasing time-to-market. Other advantages are not always obvious. Because interface chips simplify the integration of boards into systems, reduce the complexity of multiprocessor software and assist in achieving the performance requirements of a multiprocessor application, they can increase the salability of a board to a system integrator who needs to develop a multiprocessor application.

Many system integrators are building multiprocessor systems using off-the-shelf hardware compatible with industry-standard parallel backplanes integrated in a single chassis. A large number of these applications use VMEbus hardware and require the integration of compatible products from more than one vendor. Opting to use a parallel backplane bus only requires that the backplane will become the single interconnect between VMEbus cards.

The system integrator must determine what kind of system architecture meets the requirements of an application. Possibilities include a distributed memory system where the VMEbus is used purely as a communications mediim and there's no data sharing, a shared memory system where all data is accessible through global memory or dual-ported memory, or a mixture of distributed and shared memories.

## Common integration problems

Commonly occurring multiprocessor system integration problems for these applications are vendor incompatibilities, nonuniform interboard communication and performance. These issues often result from the level of definition of the VMEbus specification, which is limited to attributes such as the physical connection, electrical signals and arbitration. The specification doesn't fully address systems issues such as integration, interboard communication, configurability, and responsiveness. In spite of this, there are many successful and sophisticated VMEbus systems.

The additional flexibility of a multiprocessor architecture requires that the system designer make more major decisions regarding the system design including: How will tasks communicate? How will tasks be allocated to hardware?

The answers to these questions should be based upon the required performance, the functional attributes of the hardware and reliability—and they should not be limited by the problems associated with integrating hardware and differing VMEbus interface designs.

Interboard communication problems result from vendors' nonstandard communication models. The VMEbus standard provides enough information for a vendor to design an interface including arbitration, interrupting and data transfer. Multiprocessor systems, however, communicate at a higher level and the system designer will want to define a uniform communication mechanism.

Hardware vendors have addressed these problems by using bus interface chips in designing VMEbus cards. From the system integrator's viewpoint, the main advantages of interface chips are:

- vendor-independent bus interface
- reliable, consistent bus interfacing
- less complex system integration
- support for intercommunication, and
- flexible addressing schemes.

The first three advantages are evident if the interface chips are fully compliant with the VMEbus spec.

The last two advantages are not as evident. Presumably the multiprocessor application will be a concurrent program consisting of several tasks configured via some mechanism to execute on the multiprocessor. Tasks executing on different boards will need to communicate with each other. Intertask communication can be implemented by placing data in memory accessible to both boards. This mechanism has the advantage of being simple, but it doesn't produce systems that are predictable or efficiently use resources.

## Board signals board

The more common approach is to let one board *signal* another that information needs to be communicated. Such signaling has the benefit that the information is communicated expediently and the VMEbus resources are not needlessly occupied.

The typical hardware mechanism supporting the signal is an interrupt. The problem is the VMEbus physically supports only seven point-to-point interrupt possibilities. If there are 10 boards in a chassis, each of which must interrupt any of the other nine boards, then 90 distinct interrupts are required.

Designers of VMEbus chip interfaces have identified this need and have implemented a memory-mapped interrupt scheme. Usually there are from 20 to several hundred interrupts supported by a chip set. Some chip set implementations will generate a local interrupt to the board being signaled and simultaneously pass some unique application-defined message information, all with one four-byte VMEbus transfer. Interface chip sets for very high-end multiprocessing include interrupt buffering circuitry that minimizes the number of context switches the local microprocessor must execute to process signals, and also provide DMA circuitry to transfer information at VMEbus rates when the size of the data exceeds four bytes.

The last major advantage of a VMEbus chip set is flexible addressing schemes. Ideally memory addressing should be such that memory resources appear uniformly to all microprocessors in the system. The immediate advantage of this is that the multiprocessor design, including the allocation of tasks and the supporting intertask communication mechanism, can be determined independently of the hardware configuration. In addition to making all memory accessible, flexible memory addressing makes all memory uniquely addressable—commonly called "flat." A pointer to an object in memory, therefore, is universally valid when used by any microprocessor.

This greatly simplifies additional important systems issues: application portability, reconfigurability (especially if reconfiguring from a single processor to a multiprocessor), design, and testability. Also, extensions needed by a high-level programming language to support multiprocessing will be minimized, because special address conversions are not required and very simple intertask communication primitives can be used to construct concurrent programs.

**Jeremy James,** president, Precise Software Technologies

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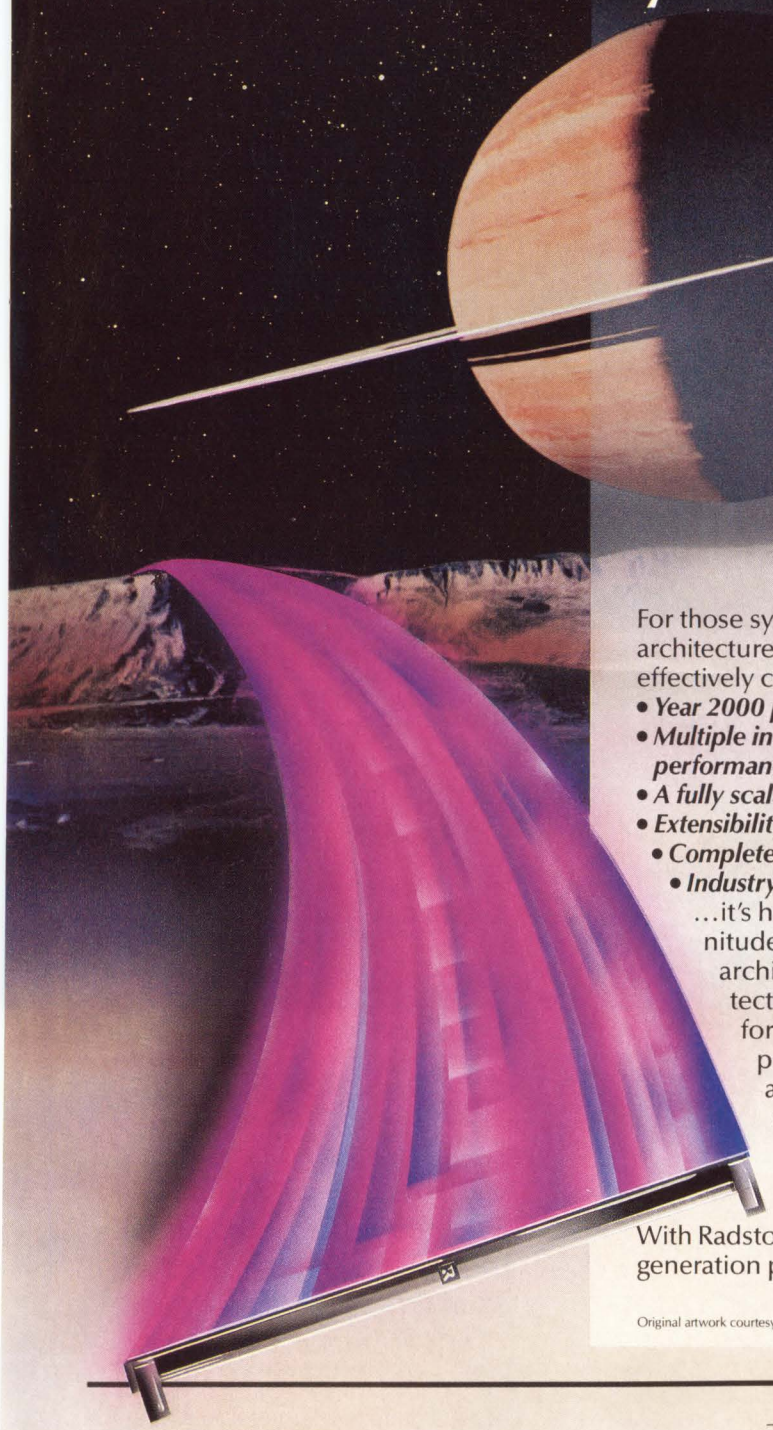

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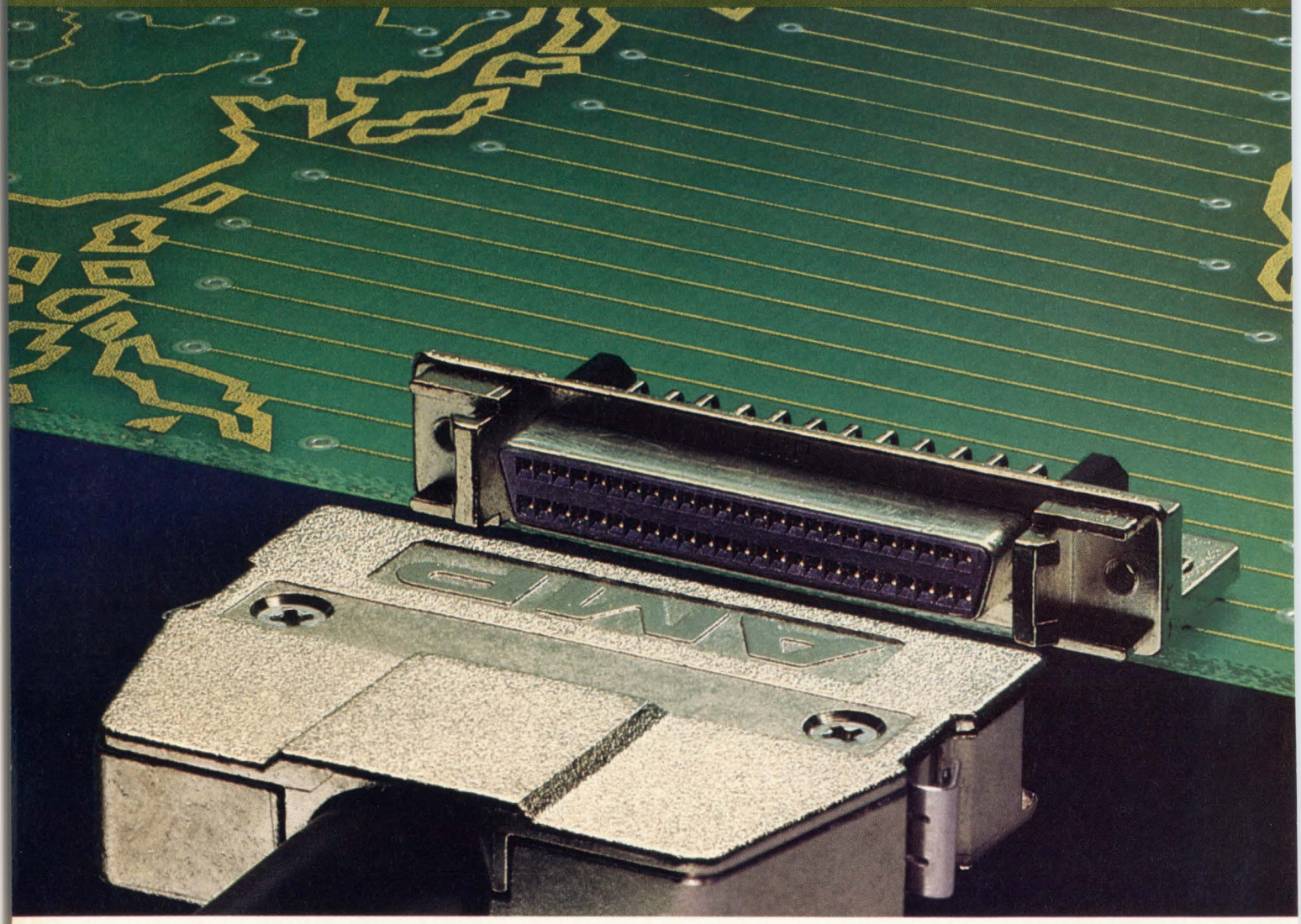

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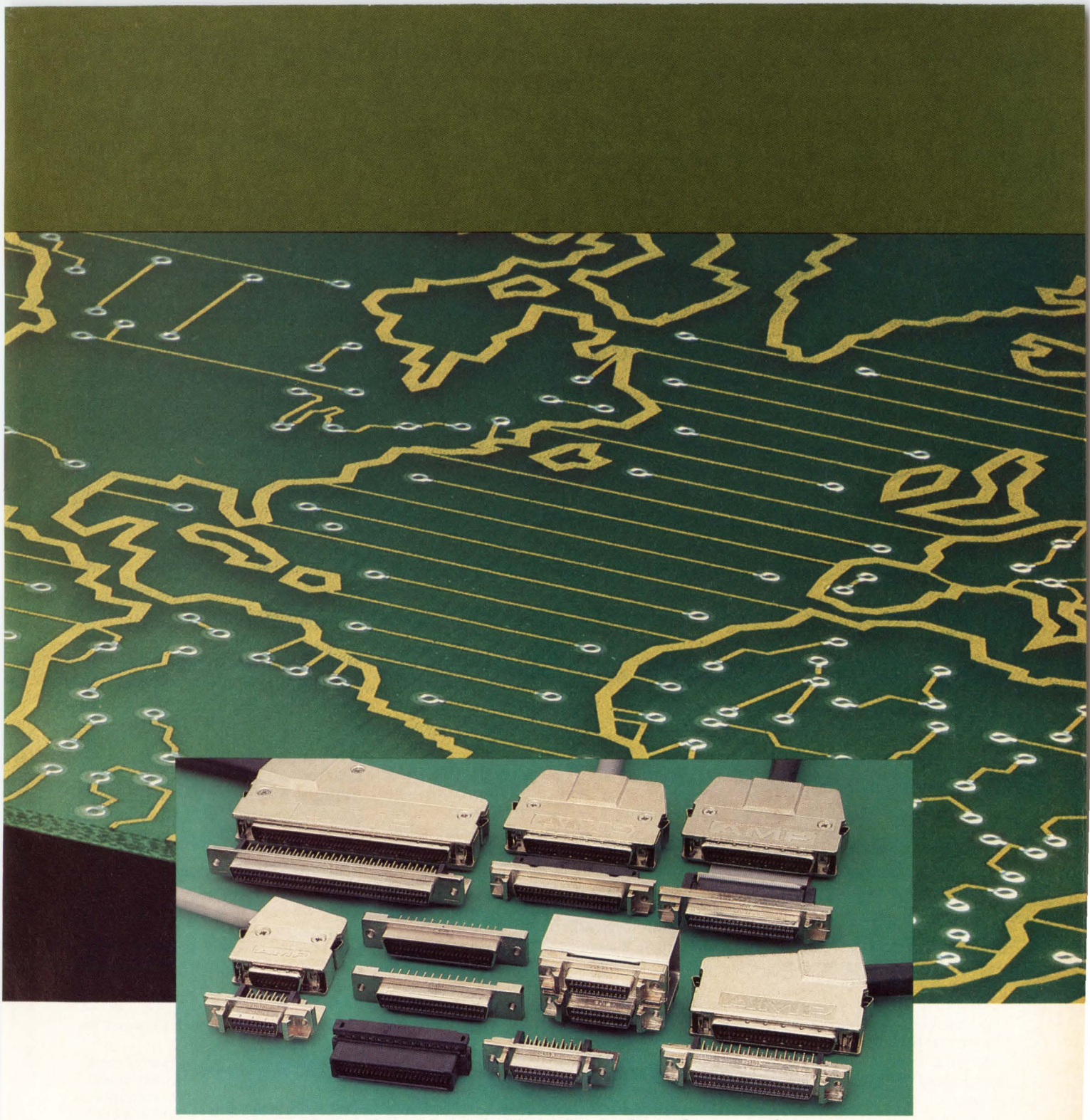

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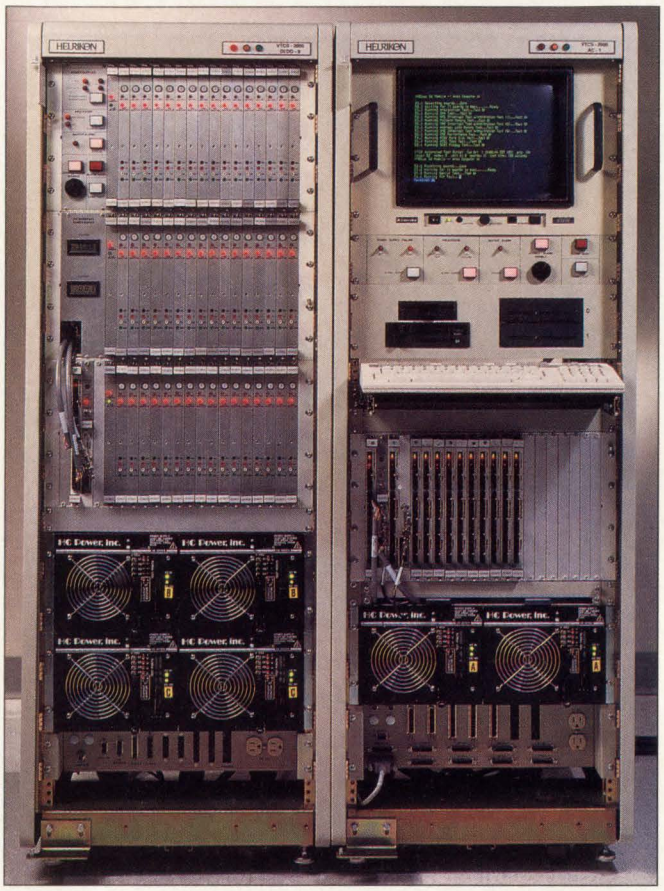


*New York City's new Vehicular Traffic Control System is composed of 11 digital I/O subsystems (left) and 18 area computers (right), designed and manufactured by Heurikon. Each area computer contains 10 to 12 Heurikon V30XE CPUs. Each DIOS contains 48 digital I/O cards, three controllers and one V30XE CPU.*

proach to a given application. And, as always, there are trade-offs to each approach. "Tightly coupled designs," says Cypress Semiconductor/Ross Technology's senior applications engineer, Matt Gutierrez, "depend on each processor in the system having access to a common memory area. But if each processor is attempting to get access to memory at the same time, there's bound to be a bottleneck."

Even in loosely coupled systems, it's critical to avoid bus bottlenecks in multiprocessing applications. "Anyone can create a bottleneck," says Joel Silverman, commercial products marketing manager from Radstone Technology (Montvale, NJ). "It's critical to architect a system to avoid such problems. It doesn't matter what kind of processor performance you have, even the fastest 68040 or RISC processor can quickly be brought to its knees if it has to wait to service a slow I/O request."

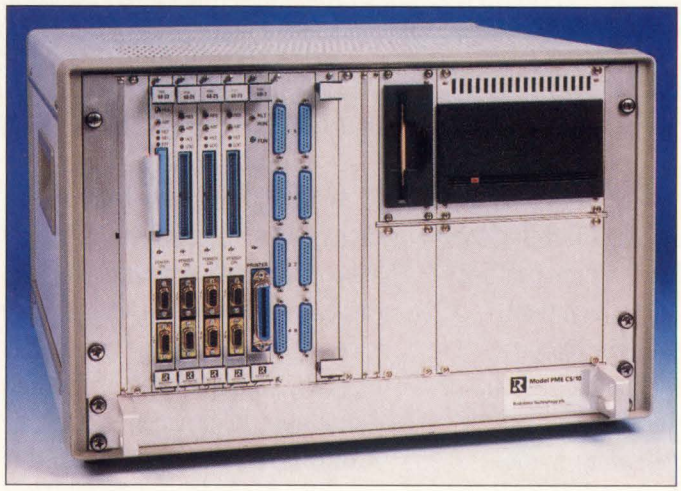
In putting systems together, says Silverman, too often designers focus only on the processor or software without looking at potential data flow problems. "It's as important to map out data flow when designing a system as it is to select the right operating system or processor," he continues. "If you can identify critical areas and start mapping datapaths on to hardware, it's possible to avoid potential problems."

"Radstone's approach," according to Silverman, "is to offer what the company calls its 'free-flow architecture,' where each board has a number of different datapaths or buses so no one bus becomes a bottleneck." He points out that in the company's 6841/6842 board, which incorporates both a 68040 and a 68020, the 68040 takes care of all the high-powered processing while the 68020 handles the bus traffic. The 68040 has its own memory and local bus so it need not be bogged down each time an interrupt is sent to that board.

For even more demanding applications, explains Silverman, Radstone offers its 6842 board, which includes a VSB (VME Subsystem Bus) channel in addition to the VME channel. This lets users with high-performance systems get on and off the board with a very fast datapath. "In addition," he adds, "it's possible to extend your data bandwidth budget by clever application of SCSI and Ethernet ports—and even additional serial ports, which can easily be added to a CPU card using a mezzanine, or daughter, board."

"What it boils down to," says Silverman, "is simply planning a system with the data flow requirements in mind. Not every system requires a tremendous amount of bandwidth beyond a VME system bus, but a powerful system can be quickly humbled if bandwidth is not considered early in the design process."

A secondary bus helps alleviate some of the potential bottlenecks on a board, and for many applications a simple memory interface bus is all that's required. With the advent of RISC processors and multiprocessor architectures, however, some microprocessor designers have developed a pseudostandard of their own which serves two purposes: first, it keeps the processor and memory architectures of a CPU board independent from the host bus, and second, it can be rigged with hooks to permit shared-memory multiprocessing.



*A typical multiprocessing system comprises a number of CPU boards and some I/O functions in a single crate. Systems can be as compact and self-contained as the one pictured here.*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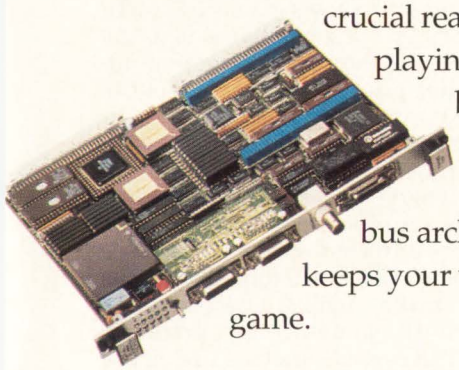

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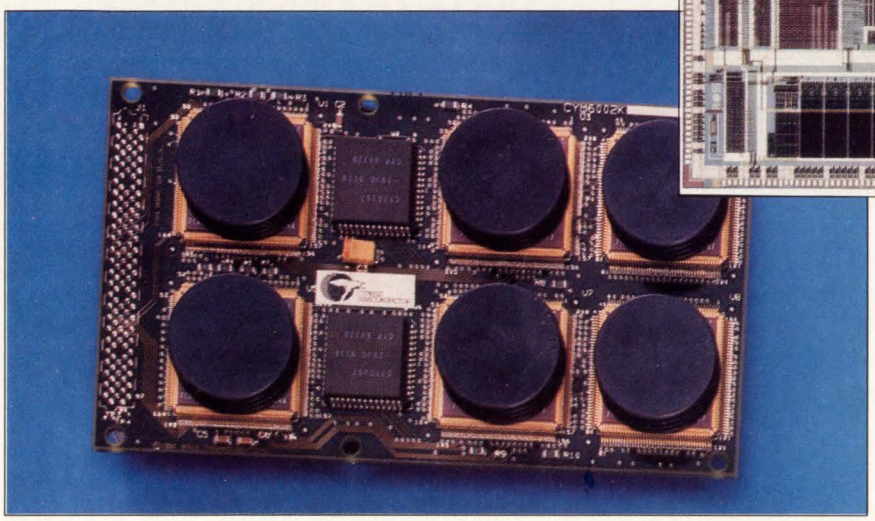
Motorola, for example, has its own version of an "M bus" for its 88000 family of processors, while Sun has a Sparc-based M bus that's starting to get more attention. The Sparc M bus, which has been adopted by all the major Sparc chip makers, was originally defined as either Level 1 or 2. The Level 1 bus definition includes all the signal lines required for processor-to-memory interconnection, but doesn't have the hooks for multiprocessing.

The Level 2 specification includes memory share (MSH) and memory inhibit (MIH) which, combined with the reserved modes of Level 1, provide the signals needed to permit tight coupling of the processors in multiprocessing applications. Both Motorola, with its 88000 family, and Cypress Semiconductor, with its Sparc-based processor, include similar mechanisms in their M bus-based multiprocessor systems.



*Cypress has integrated a multiprocessor subsystem on a multichip module (MCM) using its Sparc processors and CMU. Both processors and boards are interconnected using M bus. Shown is the Cypress Sparcore module for dual-processor multiprocessing, the CYM6002K. The heart of the system is the 605 CMU (insert), the solid-state implementation in silicon of the M bus multiprocessing protocol.*

## Keeping everybody busy

A key issue in multiprocessing, mentioned by Silverman, is having sufficient bus bandwidth to keep all the processors in a multiprocessing system supplied with data and instructions. "One way to do this," says Mentzelopoulos, "is to keep as much information as possible local to each processor. Cache memory serves this function, as well as providing some quantity of very high-performance local memory."

Gutierrez claims that the popularity of cache architectures for microprocessors began to climb at about the same time interest in multiprocessing surged. But, he points out that the cache introduced yet another level of complexity into the multiprocessing paradigm—one best summarized as making sure all processors are operating on current information, which is known as cache consistency or cache coherency.

"In the past," says Gutierrez, "cache-coherent systems existed on multiprocessing systems such as the Solbourne computer, which used up to 16 Sparc nodes in a multiprocessing architecture. But, although maintaining cache coherency has been possible, it's usually achieved at some cost—either through a large discrete component count or by a penalty in performance as cycles are wasted while caches are updated."

The cache coherency mechanism, according to Gutierrez, screams out for some kind of VLSI hardware solution, but it also needs a bus protocol to support it. Those familiar with Futurebus+ activity are aware that the 896.1 protocol specification calls for Futurebus+ to offer a superset of all bus caching approaches. "Other buses also address cache coherency," asserts Gutierrez, "the most recent is the Level 2 of the Sparc M bus."

"In putting together our multiprocessing VLSI hardware," he continues, "it was necessary to look at what functions we'd already done for single processing, and decide what had to be maintained and included in our cache control and memory management unit. What we did with the 605CMU [cache controllerand memory unit] is implement the multiprocessing [Level 2] M bus protocol in hardware. Since Cypress had the advantage of helping to coauthor the M bus protocols, the part was designed to implement them with the best possible performance."

One of the things Cypress discovered in the process was the need to incorporate two sets of cache tags in the multiprocessing controller. "Motorola's 88000 architecture, the only other high-performance RISC VLSI microprocessor targeted at multiprocessing," says Gutierrez, "was excellent as far as it went, but, whether for lack of process technology or other reasons, it only included a single set of cache tags."

## Tag, you're it: tag, you're it

Cache tags, which identify the addresses for the data that resides in cache, are memory cells that eat up a lot of silicon real estate. Normally, the CPU uses these tags to index into the cache and pull data when there's a cache hit. In multiprocessing architectures, though, cache tags have a secondary function—snooping the physical bus. In this process the CPU takes the address that shows up on the main memory bus and compares it to the memory in the cache. Snooping always has priority over the use of the cache by the processor.

If only a single cache tag is used, each time an address shows up on the memory bus and the processor snoops, the processor's access to cache memory is frozen because it has to use the tag to check whether the data is in the cache. Adding a second set of cache tags eliminates lost processor cycles, since separate tags are on the memory and processor sides. In the

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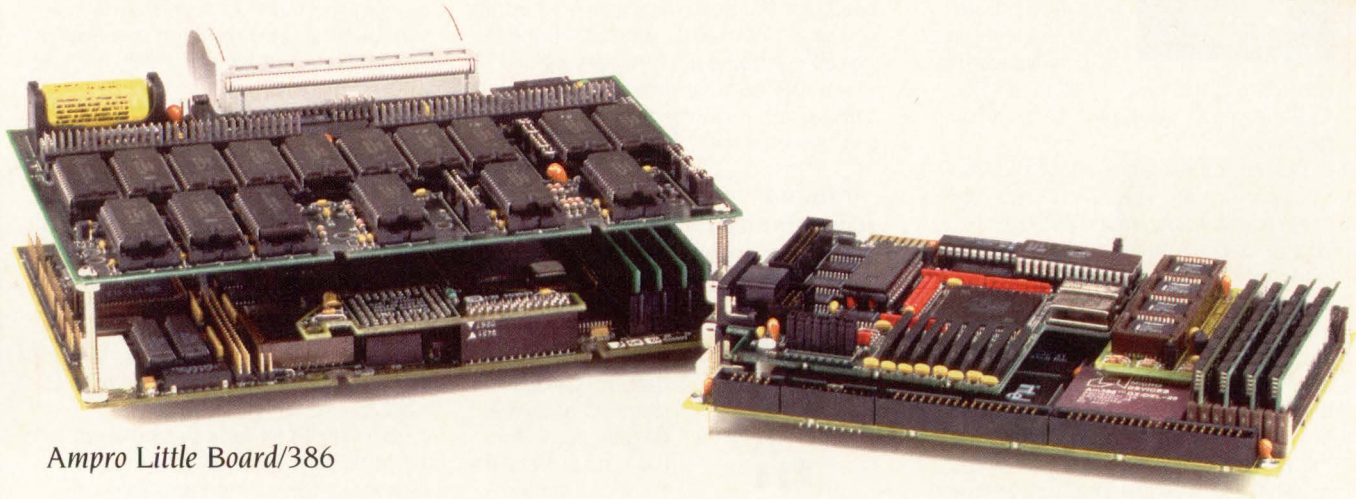

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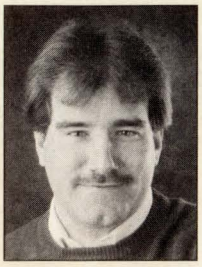
# Design considerations for multiprocessor VMEbus systems



In theory, boards that comply with the VMEbus specification should work together in the same enclosure, at least at the hardware level. In practice, however, this is often not the case—particularly in multiprocessor systems with multiple bus masters.

Part of the problem is that the VMEbus specification leaves room for interpretation in many areas. As a result, boards that are functionally correct often employ marginal design practices that are exposed when subjected to the increased rigors of a multiprocessor environment. In such an environment, increased bus activity and contention for bus resources, increased signal coupling between data and control lines, and higher capacitive loading result in reduced noise margins and tighter timing constraints that demand a much more robust design.

The VMEbus specification attempts to head off incompatibility problems by addressing many design pitfalls and making recommendations in many areas. However, these recommendations don't address all design issues. One way that designers can avoid problems in their own boards is by taking advantage of single-chip VMEbus interface devices—such as the VIC chip—which have already solved many of these problems.

Unfortunately, system integrators must worry about more than their own designs. Many existing boards already use custom VMEbus interfaces, and many new designs will continue to use custom interfaces as a cost-cutting measure.

## Reducing data bus transitions

One of the most common causes of interoperability problems in multiprocessor VMEbus systems is the coupling of spurious signals from data lines (and to a lesser extent, address lines) on to control lines. Bus Busy (BBSY*) is particularly troublesome because of its proximity to the data lines and because it's wired from each slot to the central arbiter in slot one. In a multimaster system, erroneous signals on BBSY* can cause the arbiter to simultaneously grant the bus to more than one master.

The VMEbus handbook prescribes several filtering techniques (RC, ferrite bead and flip-flop) that resolve this problem under normal conditions. Poorly designed control logic, however, particularly in the buffer enable circuitry, can cause glitches on the data lines that can't be effectively filtered using the techniques described in the VMEbus handbook.

***Problems encountered in multiprocessor systems can be avoided by following a few simple design practices.***

One situation in which these glitches often arise is when bidirectional logic is used for the control signals that derive enable signals for the data buffers. Because the same logic and physical trace are used in both the transmit and receive paths, the state of the control lines will be indeterminant for a brief time during transitions between transmit and receive operations. This, in turn, can result in glitches on the enables that are coupled on to the data lines, and subsequently on to BBSY*.

Slave memory accesses are another frequent cause of glitches on BBSY*. In many board designs, on-card data lines are left floating (not pulled high) when the memory isn't driving data. If the VMEbus data buffers are enabled before the memory is ready to provide data, the indeterminant state of the floating lines can result in oscillations on the VMEbus data lines that are coupled to BBSY*.

Both problems have obvious solutions. Avoid the use of bidirectional logic on control lines and use pullup resistors on on-card data lines. As an added precaution, however, more robust filtering techniques should be used on BBSY*. Heurikon, for example, uses a digital filter to suppress glitches on BBSY*. The filter samples the BBSY* signal at three different times using daisy-chained flip-flops. The outputs of the three flip-flops are then ANDed to derive the BBSY* signal. This time delay ensures that spurious activity on Bus Busy will be ignored.

Many system failures that occur in multiprocessor systems can be traced to capacitive loading. As boards are added to a system, capacitive loading increases, thereby decreasing signal rise and fall times and resulting in a host of timing-related problems.

## Take care loading the bus

Consider, for example, how slower rise and fall times impact control logic. When a new state is driven on to a line, the line oscillates somewhat as it transitions to its new state. In a lightly loaded system, the rise time is fast enough so that the receiving control logic ignores this noise. However, as bus loading increases, the signal takes longer to transition and the receiver has more time to react to erroneous signals.

One way to address this problem is to use logic with built-in hysteresis. With such logic, the turn-on and turn-off values are separated by a few hundred millivolts—for example, 200 to 400 mV in an LS244 line driver.

Unfortunately, even logic with built-in hysteresis can't protect against noise that equals or exceeds 400 mV. To increase noise margins even more, a good technique is to speed up rise and fall times by resending control signals prior to tristating them. (Drive high, rather than waiting for them to be pulled high through a backplane termination.) Again, however, this strategy isn't a cure-all, since it can't be used with control signals which may be monitored and driven simultaneously by multiple boards, such as SYSFAIL, DTACK (when used with location monitors) and SYSRESET.

Many of the problems encountered in multiprocessor systems can be avoided by following a few simple design practices. Familiarizing yourself with common design pitfalls and solutions is an important step in helping resolve interoperability problems. Reducing the number of vendors who supply your boards may be just as important for avoiding trouble in the first place. Typically, multiple boards from a single vendor are more likely to work together. If they don't, at least you'll have a single point of accountability.

**Jeff Durst,** associate hardware engineer, Heurikon

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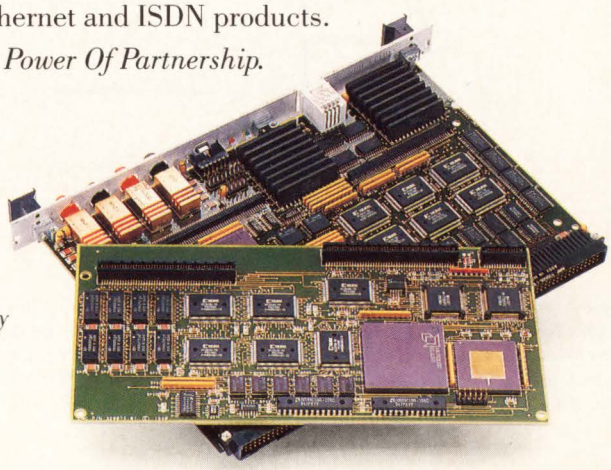

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event of simultaneous cache and snoop hits, where both memory and processor are trying to access the cache line, the snooping hit will always have priority. It will supply data to the requesting CPU, and processor access will be held until the transaction is completed.

"Part of the efficiency of our multiprocessing approach," says Gutierrez, "is some of the hooks we put into the bus protocol. One of the most significant of these is something we call direct data intervention. This refers to the ability of a CPU to supply data directly to another CPU. In comparison, indirect data-intervention schemes require additional steps."

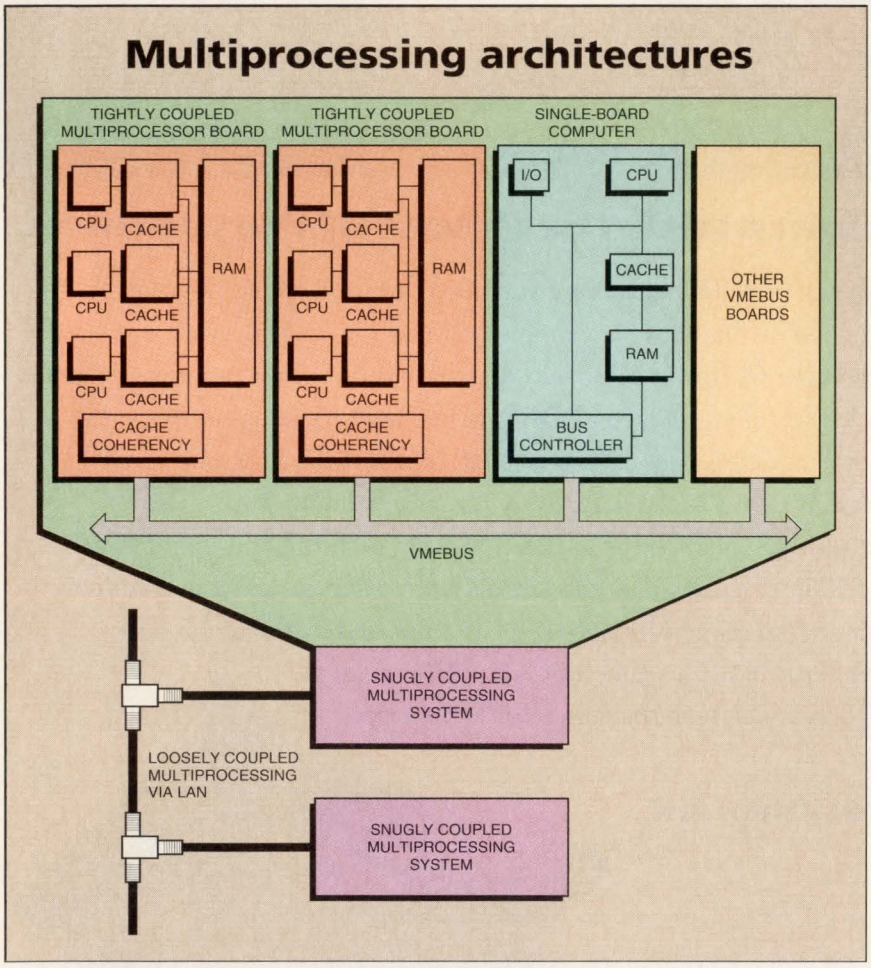
The indirect data-intervention process works as follows. First, a requesting CPU puts its message on the bus, and the CPU with the data in cache snoops the bus and discovers a hit. The latter CPU then arbitrates for the bus (causing the first processor to essentially see a cache miss) and writes the snooped cache line into main memory. It then releases the bus, and the initially requesting CPU must reacquire the bus, go out to main memory and pull the data.

Depending on the arbitration scheme and other bus variables, indirect data intervention can take anywhere from eight to 10 clock cycles to start data flowing. In extreme cases where other processors may grab the bus, thousands of clock cycles can intervene before the transaction is complete. Though somewhat slower than direct data intervention, the approach offers the benefit of simplicity. It's relatively easy to implement, since a processor is always getting the latest version of its data from main memory.

Direct data intervention is more complex. When a CPU puts a request on the bus and realizes a hit on another processor's cache, the second CPU can directly supply the requesting CPU with the new data. This puts an extra burden on the CPU with the requested address in cache. First, it must prevent the requesting CPU from getting its data from main memory, since the updated version of the data resides in the second CPU's cache and not main memory. The second CPU must also put the data on the bus and notify the requesting CPU that the data is there.

"One of the big advantages of the direct data intervention scheme," says Gutierrez, "is that there is virtually no overhead. From the time that the first CPU makes its request, data can start flowing on the next successive clock cycle." Since cache data is stored in 32-byte cache lines, the data transfer on the 64-bit M bus takes four cycles. However, the requesting CPU doesn't care where the data comes from, so no identification of the data source is required.

In direct data intervention, main memory is not updated in the same way as in the indirect approach. Instead, whatever processor takes data out of main memory into cache and modifies it has ownership of that memory. This entails two major responsibilities: first, the processor taking data must provide direct copies of it to requesting CPUs; and second, it must write a copy of the data to main memory before flushing that particular line. This, says Gutierrez, is known as an "ownership protocol."




*Lynx Real-Time Systems has its own definitions of the hierarchy of multiprocessing architectures—shared-memory approaches it calls tightly coupled, networked systems are loosely coupled, and systems linked by a backplane are "sungly coupled." As the diagram shows, all three categories can function in a single system.*

## Reflections

In addition to direct data intervention, multiprocessing systems based on M bus can take advantage of yet another feature, reflective memory. "By adding a little complexity to the memory architecture," says Gutierrez, "it's possible to let the main memory snoop the bus and detect whenever there is a transfer of data across the bus. When the memory controller's snoop circuitry detects a transfer, it automatically writes a copy of that data into main memory, eliminating the need to transfer information when a cache line is flushed—the main memory already has all the updated information."

Reflective memory is also used in some loosely coupled systems. Ironics, for example, has suggested using hardware semaphores in real-time systems to minimize penalties that reduce system backplane band-

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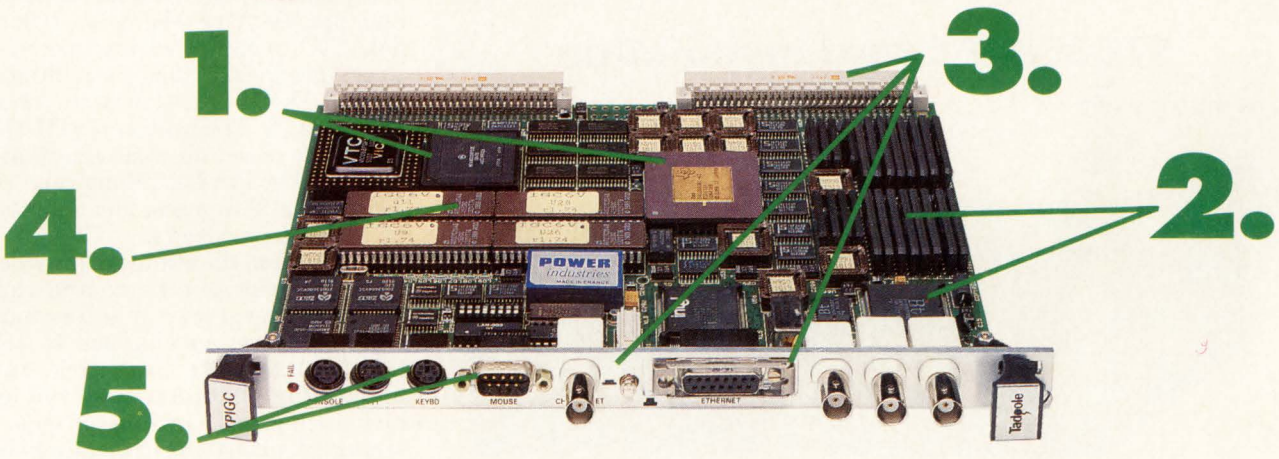


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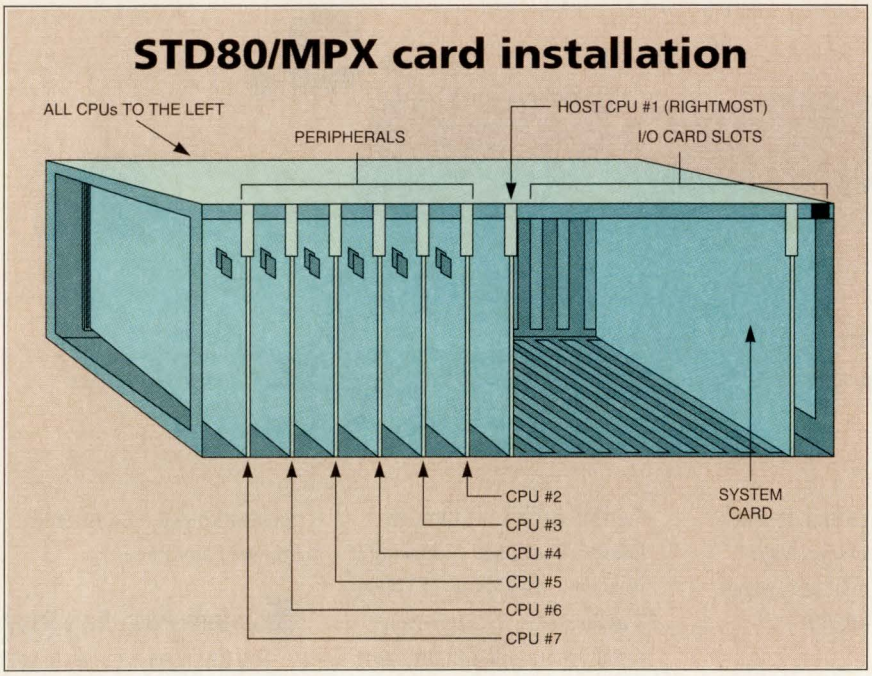
width. On VME-based systems such penalties result because of latencies in updating semaphores (spinning on a semaphore).

Reflective memory in such an architecture operates similarly to a coherent local cache. The technique is accomplished by reserving writes to a specific memory space that are only to be performed by a single master. By using reflective memory and defining a new address space and an address modifier (AM) code on VME to access the space, the technique makes all reads to the memory local and, therefore, the semaphores never appear on the VMEbus. Not too different from the M bus approach, Ironics' mechanism helps keep traffic off the bus while providing full cache-coherent support for semaphores without the overhead required for full cache coherency.




*The new multiprocessing architecture proposed by the STD MG, the STD80/MPX, uses a simple arbitration scheme assigning CPU boards priority based on the slot in the backplane in which they reside. The CPU farthest to the right has the highest priority, with decreasing priority going to the left. The right-hand card slots are used for I/O.*

## Tailored to multiprocessing

Multiprocessing architectures are by no means the exclusive domain of Futurebus+ and VME. In fact, the Multibus II protocol was designed expressly to simplify multiprocessing design through its message-passing paradigm. This approach simply lets the Multibus II backplane work like a high-speed LAN for loosely coupled systems. This eliminates many of the more complex structures, such as location monitors and mail boxes, that are required by VME to accomplish much the same task.

In addition, Multibus II defines a message-passing coprocessor (MPC) which, with its own FIFO, efficiently handles transfers without getting involved with different levels of understanding on each board in a system. "The multiprocessing hooks in VME are inherent in the particular interface IC used and there's not necessarily a lot of compatibility," says Silverman (see "Design considerations for multiprocessor VMEbus systems," p 90).

For example, one board made with the VME consortium's VIC chip will not necessarily work well with Force's FGA002 in a multiprocessing system. And, even though Motorola attempted to keep its proprietary interface IC compatible with the VIC/VAC family, those designers that are serious about large multiprocessing systems will quickly learn to shy away from boards with different interfaces.

In fact, some users are cautious about multiprocessing on VME at all. "Once you get more than a couple of processors on a VME backplane and try to make them work together," comments a critical user who claims to have sampled a broad variety of hardware and software, "problems crop up at some exponential rate." Despite such a strong negative comment, however, the anonymous user remains with the VME architecture.

## Multiprocessing on STD

The advantages multiprocessing offers have captivated STD makers and users, as well as those of other major buses. Ken Finster, a member of the board of directors for STD MG and president of Micro/Sys (Glendale, CA), reports that the manufacturers' group is finalizing a multiprocessing DOS-based approach called STD80/MPX. The proposed STD MG version is based on a scheme that's been used by Pro-Log (Monterey, CA) for the past few years, and supports up to seven processors.

In addition, the standard provides a simple priority scheme and support for interprocessor interrupts, while making no changes to the traditional STD Bus rack and maintaining minimal overhead for bus exchanges. In the proposed standard, priority is determined by the physical placement of the card in the STD rack—the right-hand slot has the highest priority. A simple priority chain, already on the STD Bus for interrupt priority, is used to resolve conflicts.

Control of the bus is carried out through a latching protocol which lets a card that has gained control of the bus keep it until another CPU explicitly requests the bus. This, says Finster, reduces overhead by permitting a single arbitration cycle to cover many following STD Bus accesses. The proposed standard also supports bus locking for single instructions and blocks of instructions.

The leading proponents of the specification are Micro/Sys, Pro-Log and WinSystems, with some other members of STD MG in support. But the STD community seems to be divided since Ziatech introduced its 32-bit STD32. Just as it offers 16- and 32-bit transfers through a specially designed STD80-compatible connector, STD32 also offers its own version of multiprocessing support.

Because STD32 is based on the EISA standard, however, and even uses an EISA bus interface chip set, it can take advantage of multiprocessing architectures already developed for that bus (see "A new

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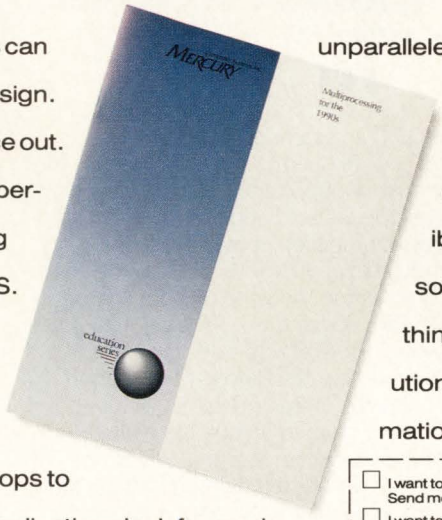


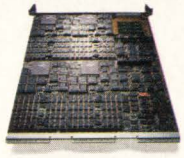

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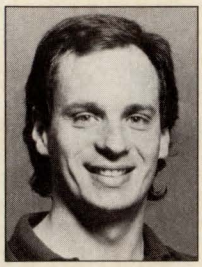
# A new multiprocessing technique brings DOS to real-time control



A new multiprocessing technique using the STD32 bus combines the functionality of personal computers with the real-time responsiveness of high-performance, industrial bus computers. The approach lets several DOS-based processor cards share peripherals, such as disks and video, in a single STD32-based control system. This unique capability permits systems engineers to simply segment their application over distributed processors, rather than programming a complicated multitasking operating system on a single processor.

Complex, real-time control systems require that the critical portions of their processes occur at precise times, without delays for operator input, network response or other, less critical functions. These real-time control tasks are often tackled with extensive programming and time-consuming development of interrupt service routines

In some cases, a real-time multitasking executive or operating system is necessary, and the programming grows in complexity, time and expense.The multiple DOS processor technique, used on Ziatech's STD32 Star System, lets designers allocate one or more processors to each real-time process, while another processor monitors the less critical functions.

## EISA techniques in STD32

The STD32 hardware approach to multiprocessing is similar to the technique used by EISA, with some important distinctions. STD32 and EISA interleave existing signals with new extended signals to provide more capabilities, such as multiprocessing, while maintaining compatibility with established standards (ISA for EISA and STD for STD32).

Both EISA and STD32 also use centralized arbitration for multiprocessing, but in different ways. EISA's arbitration logic is placed on the system motherboard, while STD32 designates a Slot X in its passive backplane for a simple arbiter card. The arbiter card monitors access to the bus, supporting up to seven processor cards using either a fixed or rotating priority scheme. These schemes determine which processor card is granted access to the bus when simultaneous requests are received.

The centralization of arbitration logic reduces the cost and complexity of a multiprocessing system. Placing arbitration logic on the Slot X card instead of on individual board computers lets these boards optimize their space for CPU, memory and I/O functions. Centralized arbitration also enhances system reliability because the logic is located in one simple circuit instead of across multiple circuits on several boards.

## BIOS manages peripheral access

While the arbiter card monitors hardware access to the backplane, an industrialized, 100 percent PC/AT-compatible BIOS monitors each processor's access to shared DOS peripherals, such as disks and video consoles.This multiprocessing BIOS is an extension of an STD DOS BIOS developed to provide functions for industrial applications not available in a desktop BIOS. In addition to its multiprocessing function, it includes features for industrial applications, such as the ability to define the system's boot source (PROM, floppy drive, fixed drive, or network), the ability to select a fast boot (no memory test) and built-in support for PROM, RAM and FLASH drives.

***Each processor is, in fact, a virtual PC.***

The system uses multiple instruction and data multiprocessing, which employs a distributed memory architecture. Each processor has its own memory for instructions and data and communicates with other processors via a messaging system. This distributed memory design is a scalable system that provides a proportional performance increase as processors are added. Such modularity lets control system designers configure their application's precise performance requirements, and lets them upgrade processing power easily when necessary.

## A network in an STD32 box

In the multiple DOS processor approach, the messaging system is built around an area of common memory on the backplane. This technique is similar to that used in a very fast and transparent LAN, except that all the processors are on the same STD32 bus.

The location of DOS on each processor simplifies application development. Each processor is, in fact, a "virtual PC," except that it shares its disks with other PCs. The video display and keyboard console can be switched from processor to processor by the Ctrl-Alt-Space key combination. Virtual video memory on the other processors acts as a video card and the application program continues uninterrupted.

When the system's video card is switched to the processor, it's automatically updated with the current state of the display for that processor. The multiple DOS processor technique also lets most of the popular PC development tools, such as Borland's Turbo Debugger and Microsoft's QuickBASIC, run simultaneously on different processors sharing the same video card. The ability to run these familiar PC debugging tools on each processor greatly speeds application debugging.

And finally, the multiple DOS processor system is designed to accommodate the ever-advancing capabilities of PCs, and to adapt these capabilities to control applications. Its 32-bit STD32 bus will accommodate new, 32-bit single-board computers scheduled for introduction in mid-1992, increasing the system's upper-end performance options. The system's PC/AT-compatible BIOS supports the industry-standard Microsoft Windows 3.0 user interface, allowing the use of Windows for the user interface processor and other DOS processors for the real-time controllers.

**Rob Davidson,** product manager, Ziatech

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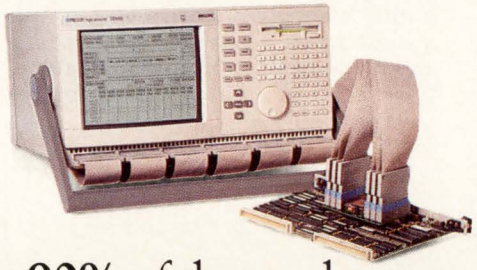

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multiprocessing technique brings DOS to real-time control," p 96). As Ziatech product manager Rob Davidson explains, the beauty of the STD32 approach is its simplicity, which translates in turn to reliability. "Our arbitration card, which is responsible for granting access to the bus with relatively simple arbitration logic, carries an MTBF [mean time between failures] of hundreds of years," comments Davidson.

## Keys to the castle

Hardware architectures abound, but they don't stand alone; software is also needed. Back in the early days of multiprocessing, processors often stepped on each other's toes, and incremental gains in computing power achieved by adding more processors quickly leveled out and in some cases became negative after only a few processors were added. Long strides have been taken since then, but it's still far from easy, from the standpoint of software, going from one to several processors.

"There are several factors involved," says Kim Rowe, president of Multiprocessor Toolsmiths (Nepean, Ontario). "In putting together a system with multiple processors, even in a loosely coupled architecture." Some considerations are: How do you balance the load between different processors? Which processors should you assign what tasks? And how do you make sure that each processor is being used optimally?

"Toolsmiths," says Rowe, "offers a variety of tools that help designers develop and debug multiprocessing systems. Depending on the application, it can be as easy as simply recompiling code and running. More complex programs may require the designer to look at the system and see exactly how CPU assets are deployed. Our debug environment lets the designer do exactly that."

But real-time software for tightly coupled systems is more elusive. The application will determine the effectiveness of any solution, but since the operating system must determine processor allocation, and do it deterministically, it's not a trivial task. Even in the Unix environment, processor allocation is still relatively coarse-grained—if it functions at all.

Until the software catches up, hardware architectures will continue to bend to the needs of the application, and the kernel will incorporate every technique available to reduce bus traffic while providing enough hardware services to keep the system running.

In the meantime, software developers are feverishly working to create a software environment that can handle virtually any complement of processors in a multiprocessor system. In theory, the operating system should be able to automatically configure the system as a massively parallel, symmetric multiprocessing environment for highly compute-intensive jobs, or as a dissociated series of array processors to handle multiple slices of related data. In reality, that capability may be some time away. ■

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## Postscript

*Purists, whether discussing single-processor or multiple-processor systems, comment that an application should be totally divorced from the hardware it runs on. They insist that ubiquitous interfaces such as Windows NT, Posix-based Unix and other standard platforms will totally obscure the hardware from the software.*

*But we live in the real world, and in that world it turns out certain applications tend to operate more efficiently—faster—on certain hardware platforms than on others. In this special report, we dwelt at considerable length on the 'cost' of getting data to each processor fast enough. What should be implicit in that discussion is that the benefit should be commensurate with the cost.*

*Hardware architectures providing multiple datapaths or with well-managed cache controllers are great for applications with high data-flow requirements. But for applications with more cohesive data streams, such architectures may represent overkill, and could even result in less efficient processing. In either case, efficient software can go a long way toward solving problems, but efficient software running on well-tuned hardware will always perform a lot better than the same software on poorly-tuned, general-purpose platforms—unless, of course, you don't care if things can run any faster. Then you should look to reduce cost or realize other gains.*

*A well-designed system obviously calls for a good mix of both software and hardware. Failing to consider both at the time you put together an application can be hazardous. It may result in delays in getting to market, a more costly product, headaches about reliability problems, and all manner of system integration nightmares.*

Warren Andrews


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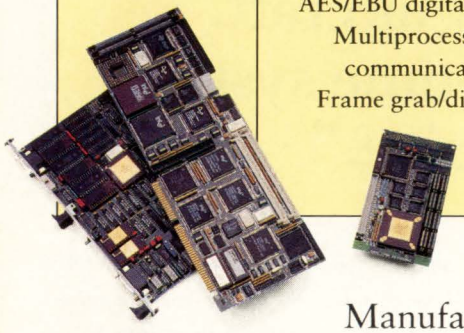

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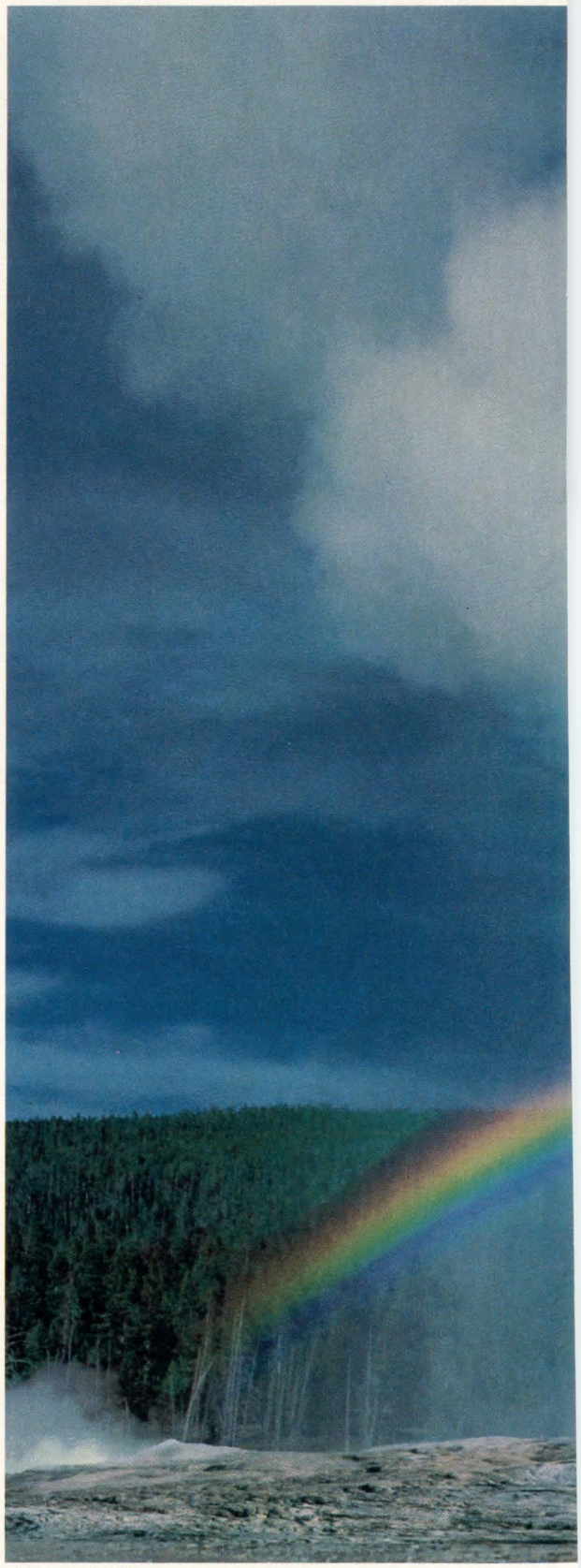

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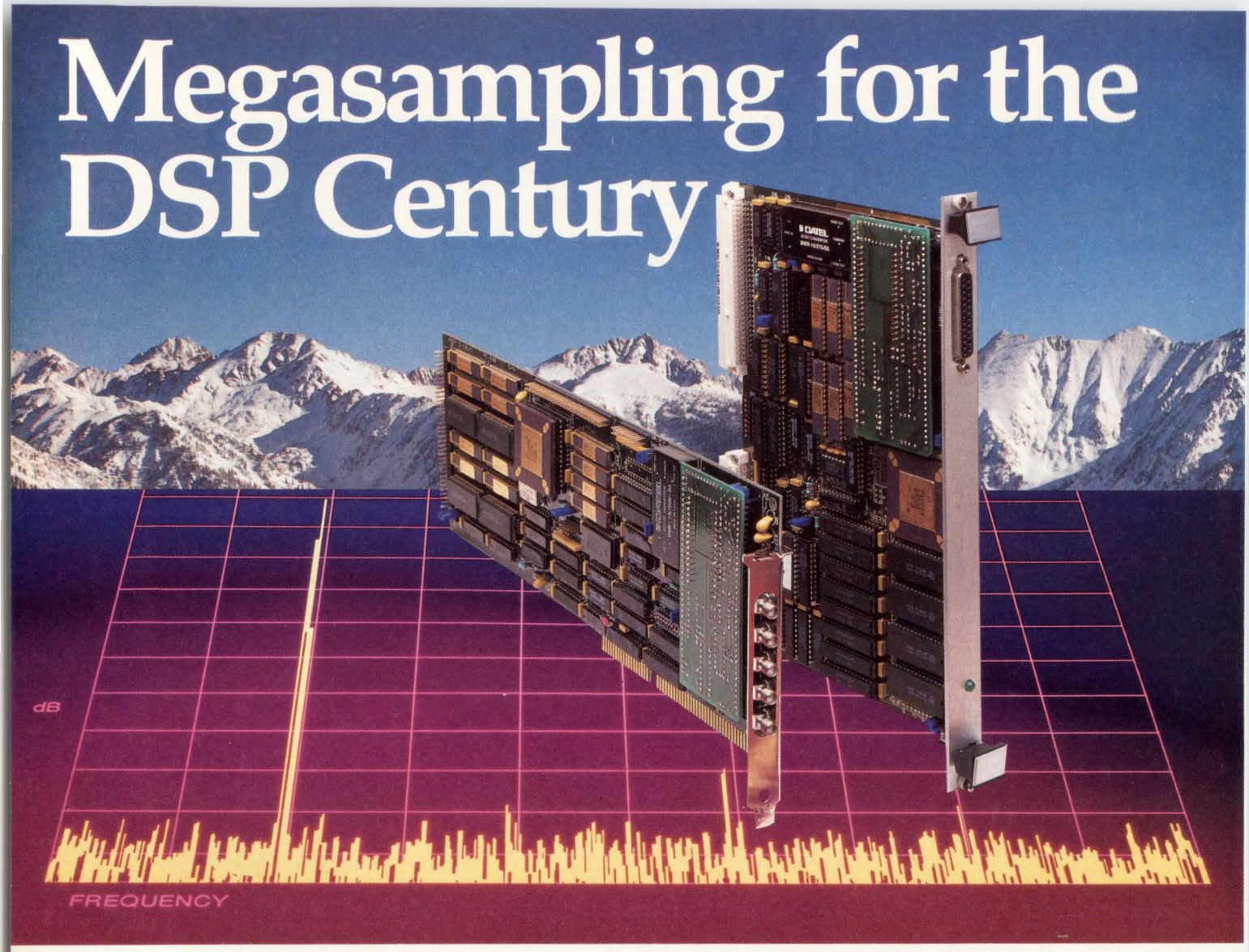


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# Spirit's story evokes the make-or-buy decision

*The Spirit development team from left to right: Feng Mo, senior software engineer; Bill Lutz, senior design engineer; Dan Lombardi, senior design engineer; Glenn Isensee, project manager; and Dr. Che Chi, Spirit project manager. In the center of the photo is the Nicolet Spirit with some of the custom boards exposed.*

One key to the wide acceptance of evoked-potential testing is the clinician's ability to measure and quantify the brain's electrical activity in patients unable to cooperate with conventional testing methods. To solve this problem, Nicolet Biomedical Products (Madison, WI) recently introduced "The Spirit." This new, low-cost ($20,000 to $30,000) evoked-potential system (EPS) can discover hearing problems in infants within hours of birth. Alternatively, it can aid in the early detection of both multiple sclerosis and subtle visual problems during infancy or early childhood.

Nicolet Biomedical has developed high-end EPSs for years, but the last mid- to low-range system the company produced was designed more than eight years ago. The company had needed a new low-end product for some time, but didn't have the resources available to build one until the spring of 1990. At that time Dr. Che Chi, Spirit project manager, started to formulate her ideas about the design of the new system. "I decided upon which computer platform and what add-in hardware would have to be designed to do the job. I evaluated different operating systems, different vendors' graphics library support requirements as well as the hardware itself," she says.

According to Glenn Isensee, a Nicolet project manager, the key features of any EPS are a general-purpose controller that's OS-driven, stimulators that provide a stimulus to the patient and a data-acquisition system that collects the data created in response to the stimulus. Because of time-to-market considerations, components associated with the Spirit system comprise off-the-shelf hardware and software and custom hardware and software designs.

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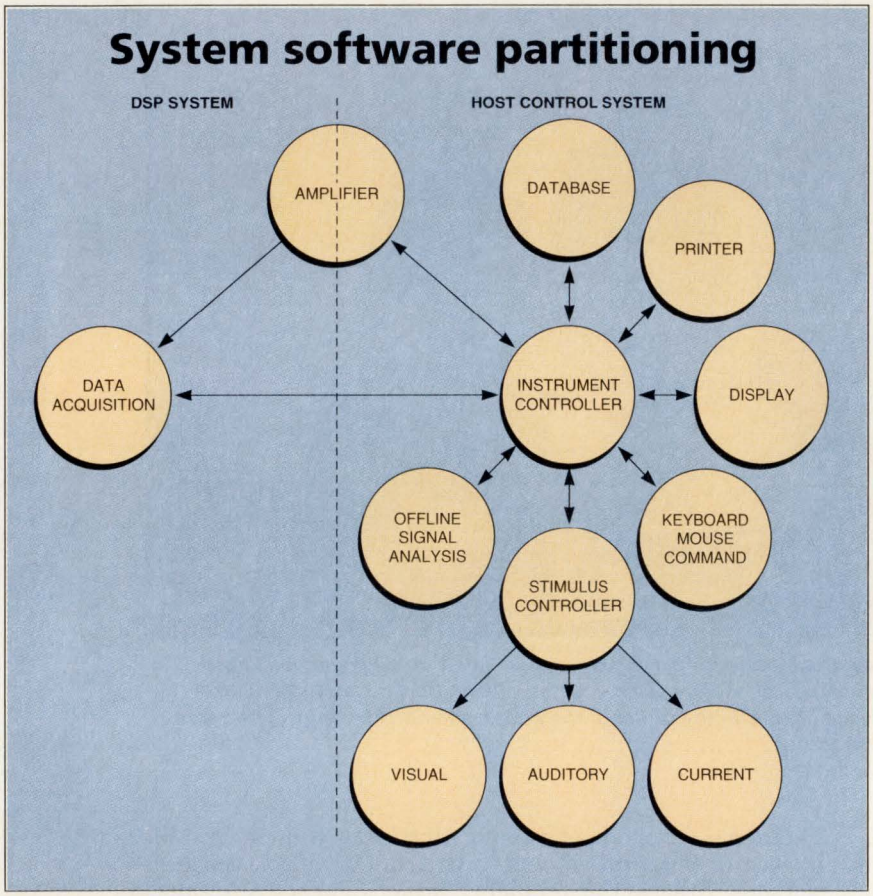
**Dave Wilson, Senior Editor**

Instruments such as the Spirit work on the principle of acquiring data that must be time-locked to a stimulus, much as a logic analyzer correlates data to a clock. In the case of the Spirit, though, the stimulus may be electrical, visual or auditory and the "probes" used to acquire the data are attached to a patient rather than a microprocessor.

Regardless of what signal is used as a stimulus, once the latter has been delivered to the patient, every other system component in the Spirit "time-locks" to the signal and a set of data is captured. The procedure of stimulation/data capture is repeated as many times as necessary; each time, the system time-locks to the signal and records data. The system then applies signal averaging to the data acquired over a number of sample sets. The resulting data is presented to the clinician in a graphical form.

Because the system must provide both electrical current and auditory stimulation to the patient, Nicolet designed two custom PC/AT boards. The auditory stimulation board design was based on a Motorola 56001 DSP. Both stimulation boards reside in the back of an AT-based Intel Computer Systems 386SX personal computer. A digital amplifier, located in a separate headbox placed near the patient, is used to boost signals and reduce the noise. The data is acquired from electrodes attached to the patient.

In the headbox, the signal is amplified and filtered. After filtering, the analog signals are converted into a digital format and the channels of digital data are serialized into a multiplexed digital bit stream. The data is sent to a data-acquisition card residing in the AT bus of the Intel 386SX box. There, the data is deserialized. After some real-time processing by the DSP chip, the 386SX is responsible for displaying information on the screen.




*The software development team was divided into two groups—while one group worked on 56001 assembler code to handle real-time/data acquisition, the other developed control code in C for the OS/2-based graphical user interface. The partitioning of the two groups let them work at their own rates.*

Time-to-market issues were clearly at the top of the priority list for the company. "We wanted to develop the system in the shortest possible time," says Che. Fortunately, at the time there was another high-end product under development at Nicolet. So Che's first task was to determine what existing hardware could be reused to reduce the development cycle of her own project.

## Borrowing from within

That other project was a system development being headed up by Isensee. His project included the development of both an amplifier and an acquisition board. "That was great for us," says Che, "because we borrowed that hardware technology for the Spirit system." As a result, the Spirit system uses a modified version of the amplifier developed for Isensee's project, as well as a modified version of the PC acquisition board. For the stimulators, Che used already existing designs.

In addition to time-to-market considerations, the final customer cost of the system was a major factor in the development process. "We had established a good relationship with Intel," Che says. "We wanted to use a reliable vendor across the company's product lines. That would help us increase the volume of units we purchased and lower the cost." That's how she ended up using the Intel 386SX OEM System, which at the time was also in use in other Nicolet products targeted toward different fields, such as analytical chemistry. "Our concept is to use as much general-purpose off-the-shelf hardware as possible to reduce time-to-market, but the application-specific hardware still had to be designed in-house," states Che.

On the higher-end Nicolet system developed by Isensee, a data-acquisition board had been built around two Motorola 56001 DSP chips. That system was required to process eight channels of data. In the case of the Spirit, however, only four channels of data were needed, and that meant that Bill Lutz, the senior design engineer on the project, could redesign the DSP board to accommodate just one DSP, also reducing the time-to-market of the system. "It certainly made a lot of sense to our management to reuse as many existing boards as possible and to keep the design more cost effective," adds Che.

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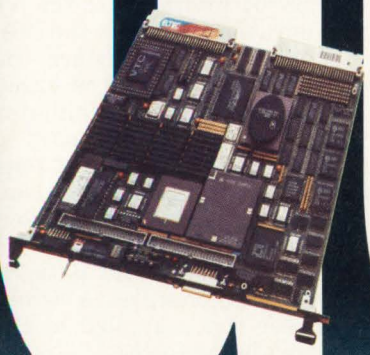

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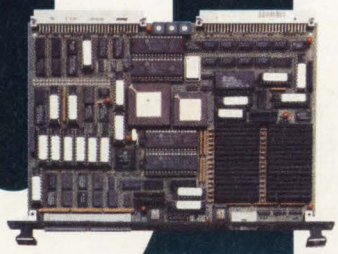
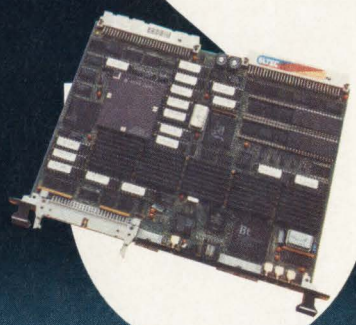


**OPAC-200 Color Graphics Interface board**



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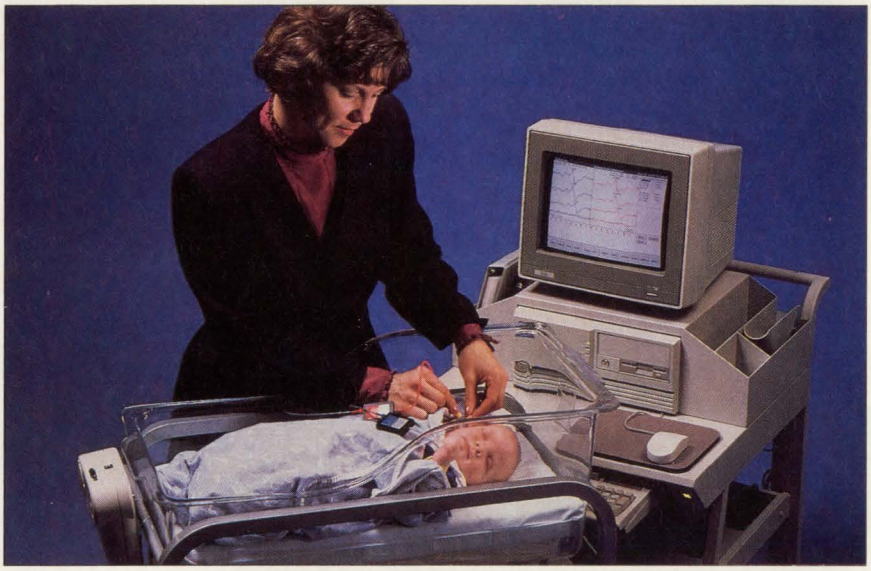
CIRCLE NO. 60

As the Spirit system was developed, it became clear that the analog signals acquired from the patient should be presented as a multiplexed data stream of digital (rather than analog) words to the data link—and then demultiplexed at a later time on the PC. That's because a digital design was easier to implement than an analog design—the isolation scheme is simpler. Second, there were fewer devices involved in the link, making it more reliable. Then there were issues concerning interference pickup on analog interconnects over long distances. "Analog signals running on two or three hundred feet of cable through electrically hostile environments get contaminated with noise. This is especially true when you're looking for signals in the 0.1-microvolt range," says Dan Lombardi, senior design engineer responsible for amplifier design. "It doesn't take a whole lot of interference on a signal before that signal is very difficult to recover."



*The Nicolet Spirit is an evoked-potential system based around a 386SX personal computer from Intel. Potentials are evoked through visual, auditory or current stimulation. The resulting responses are acquired, amplified and averaged before being presented to the clinician through a custom DSP subsystem designed at Nicolet.*

The amplifier not only has a high-speed digital data link, but it also sports an RS-232 low-speed data link as well. That link is used by the host to reconfigure the functionality of the amplifier.

The software model developed for the Spirit doesn't change when the number of channels is increased—the data is still brought into a "live" multiple data buffer, demultiplexed, filtered, and then placed into a fixed-length averaging buffer. It's through this process that the data captured by each of the individual channels is reconstructed. Averaging improves the signal-to-noise ratio of the signal to be displayed.

The software model supports another important user need, that of independent channel control. "It's a situation where the users need to identify unique characteristics on each channel, their sensitivity and their filter settings. But it's not until the data gets into those unique buffers that the software has to worry about which filter sets get applied to each channel. You can make the link very general and the software doing the processing more specific," says Feng Mo, senior software engineer. In the design of the software acquisition system, Mo cites the importance of isolating these two processes so that, if necessary, the number of channels on the system could be changed without rewriting much of the code associated with deserializing the data stream.

The system has interstimulus intervals where there's no data acquisition activity being performed by the instrument. During data acquisition, however, there's only a finite "time window" in which a lot of data must be collected. That window might be only 10 ms for data triggered by an auditory stimulus. "By using the concept of software buffers, we can control the sweep lengths, the amount of data being presented and decimate the data if that's necessary," says Mo.

## Three custom cards

As mentioned earlier, the 386SX-based AT platform has three custom cards, two for stimulus generation, the other for acquisition. The acquisition card receives the data stream from the front-end amplifier, presenting the data to a Motorola 56001. It's the 56001 that performs the digital low-pass filtering, demultiplexing and averaging on the signal. The 56001 interfaces to the AT bus through a port built into the DSP chip. Like the acquisition board, the auditory stimulator board is based on the 56001. On the stimulator board, though, the 56001 is used to generate a series of clicks or tone bursts; the digital signal is then converted by a 16-bit audio D-A converter and amplified enough to drive headphones worn by the patient. The DSP also generates a white noise masker that's applied to the ear that isn't being tested.

The third board, the electrical stimulator, provides either a high-current or a high-voltage pulse to the patient; again, electrodes placed on the body pick up the response. "The current stimulator board is a function that's very proprietary to Nicolet," says Lombardi, the designer of the board. "On the current stimulator board is a collection of D-A converters, transformers and transistors. They perform the level shifting and feedback mechanisms to control the amount of current being delivered to a patient." In addition, patient isolation circuitry ensures that the current flow is only through the tips of the probe and not through a ground attached to the patient.

## 24-bit word length

Bill Lutz points out that the major reason for his choice of the Motorola 56001 DSP chip for the Nicolet Spirit designs was its 24-bit integer word length. "In the case of the auditory stimulator board, you need to generate a very high-quality waveform, and 16-bit processors wouldn't have provided enough precision. And, since the DAC expects integer data, it wasn't worth using floating point. I also liked the part's synchronous serial interface that let us hook directly into the serial audio D-A converter on a three-wire interface. It also has a fairly attractive

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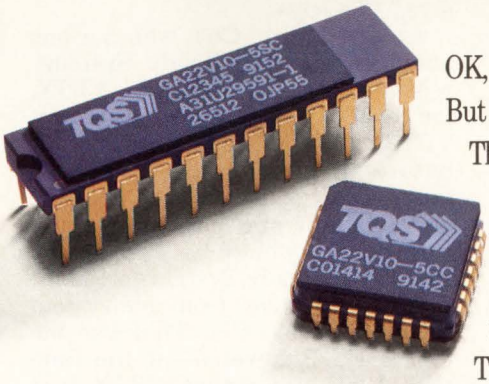


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host interface that lets us talk back and forth on the AT bus to the host," Lutz adds.

In most circumstances, Lutz says, the averaged data is sent back across the AT bus to the 386SX-based host controller for further processing—and it's the host that decides if the data is to be analyzed, printed, displayed, or stored. "Like other evoked potential systems, the Spirit system collects data at a predetermined rate called the stimulus rate," says Che. "Generally, the data sweep time is shorter than the interstimulus interval. Only portions of real-time data from the amplifiers are collected. That cuts down on the data stream flowing from the DSP board to the host, and the bandwidth of the bus that's needed to do the job." So, an AT bus-based system fit the bill nicely for the Spirit.

Graphical user interfaces (GUIs) are becoming an important part of most systems developed today—as important in the biomedical world as on a Unix-based workstation. At the time the Spirit system was being developed, project manager Che evaluated several operating systems, some with GUIs, some without. "I evaluated OS/2, real-time Unix, DOS, Windows 2.0, as well as a real-time operating system—VRTX [from Ready Systems]," she says.

"Right away, DOS was discounted because we needed a true multitasking operating system to perform the job," Che adds. DOS is a single-tasking operating system. And, while Windows 2.0 was evaluated, it became clear to Che that, after talking to a number of technical people at Microsoft, Windows wasn't a true multitasking operating system either. "At that time, Windows 2.0 was a pseudomultitasking operating system and it was extremely slow," says Che. "And for our system, performance is important."

## Heavy overhead prohibitive

While Che liked Unix as a multiuser multitasking OS, she didn't like its heavy system overhead. "For us, it was too expensive. The royalty price was too high and the resource requirements were too great." At the time, just the operating system would have required a 40-Mbyte hard drive, not to mention eight Mbytes of DRAM memory to run X Windows. "Prices ranged from $400 to $1,000 a copy. X Windows was more money added on top. When you add it all up, it was much too expensive," Che says.

At one point, Che was serious about considering Ready Systems' real-time operating system, VRTX, for the job. But the disadvantage of VRTX to Nicolet was its proprietary nature. "If, in the future, we need to move from one platform to another, or change the microprocessor in the system, we would be relying too heavily on Ready Systems to adapt their device driver from one system to another," says Che. That was one drawback. But worse—at the time the 32-bit version of VRTX just wasn't available. Furthermore, Nicolet would have been forced to select its own GUI package, since Ready didn't offer one at the time—and anything chosen would have been proprietary.

Although Nicolet needed a system that could respond to real-time

events, it was the hardware and software partitioning that allowed Che to use OS/2. That's because the Motorola 56001-based front end was used for the real-time data acquisition and digital filtering, while the 386SX-based host was freed from dealing with events that require an immediate response.

Because of the partitioning, the host didn't need to be a real-time system. Also, interrupt latency became less of an issue, because it was controlled by the Motorola 56001 processor. "The DSP board has a 1-µs worst-case interrupt latency—that's better than any real-time system could achieve," says Che. To pull it off, however, Feng Mo had to develop his own real-time kernel to run on the device to control the data acquisition. In addition, using C programming tools, he built a software library to help the DSP communicate with the host.

## Threads versus real-time

With OS/2 and a real-time kernel in place, the responsibility of the host processor was relegated to responding to user commands, graphics requirements, database reporting, and communication with the DSP processor—responsibilities well suited to a true multitasking operating system. The concept of "software threads" in OS/2 was used extensively by the Spirit development group, in part to replace separate processes. "The concept of the thread is much more efficient methodology than a standard process," says Che. "A thread lets us share data and code segments between two processes with separate stacks. To us that's completely equivalent to having different tasks under a real-time operating system."

The independent software operating system kernel running on the DSP board talks to the host through the AT hardware interface. The software interface between the host and the DSP board was built using C library function calls that provide the host with all the necessary access to the DSP board. "At the beginning of the project we spent a lot of time defining the functions of a C library that would be used by the host to communicate to the real-time data-acquisition subsystem," says Mo. The real-time system is controlled by this general set of predefined C library functions.

From a software perspective, the data-acquisition front end takes the input data and passes it through a dedicated interface (called the host port interface) to the PC. The idea of the software interface is to isolate the PC from as many details of the data-acquisition subsystem as possible. "The PC doesn't really need to know what's on the other side of the host port interface," says Mo. "All it knows is that there's an acquisition subsystem capable of acquiring data from multiple channels, synchronizing them, generating the averaging records, and performing filtering."

Dividing the system software design teams into two groups, one dealing with OS/2 software development and the other with real-time development, helped speed up development. As an added benefit, the two groups work concurrently and independently, even though the work itself had to be tightly synchronized to meet the deadlines imposed by the design schedule. ■

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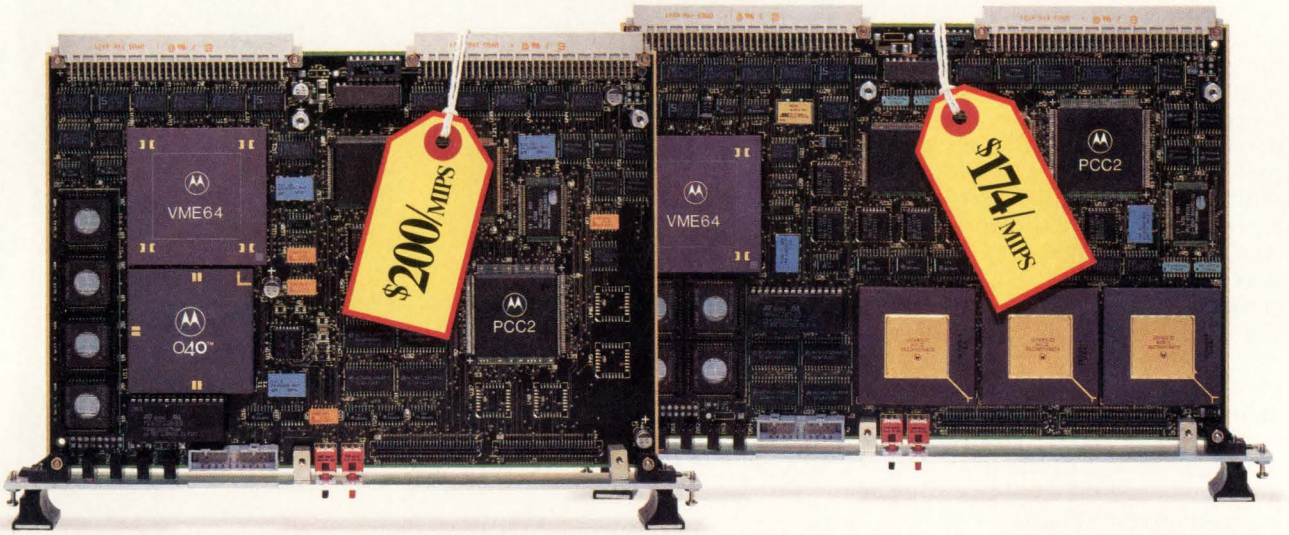


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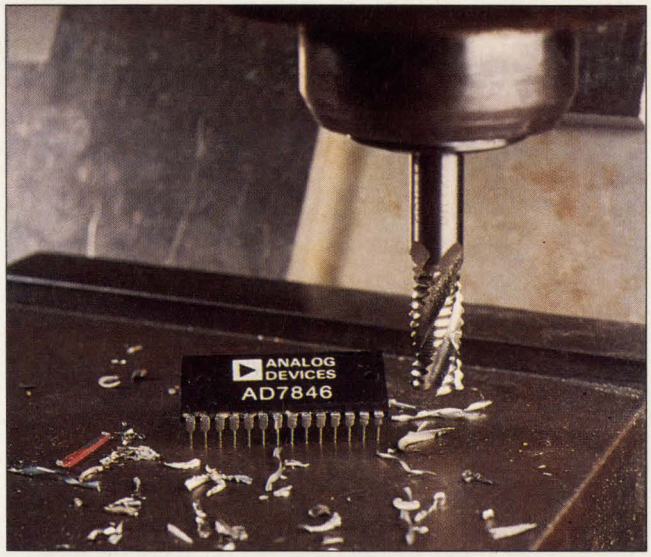


*In closed-loop servo control applications such as this drilling machine, D-A specifications such as monotinicity determine the degree of precision at which the tool can operate. Analog Device's AD7846 is 16-bit monotonic over a temperature range of –55 to +125°C. Its 100-mW power dissipation and small 28-pin package make it suitable for portable applications.*

Whether the focus of your design effort is on better sound or better servo operation, the high-resolution digital-to-analog converter (DAC) you choose will directly affect your system performance. Today's selection of high-resolution (16-bit and higher) DACs for industrial control ranges from general-purpose parts specified over wide operational parameters to targeted devices tailored for particular application needs. Meanwhile, a host of new audio DACs is also making a splash. Among these are audio-specific parts with multibit architectures and the cheaper, but slower, sigma-delta parts that settle at audio speeds.

Although arguably in a separate category unto themselves, audio converters have been a driving force in high-resolution converter technology. The volumes required for the consumer audio market have forced DAC makers to improve their processes and increase manufacturing efficiencies. By leveraging such improvements, they've been able to cut the costs of general-purpose DAC products.

## True 16 bits?

Among those designers who have already made the move from 12- and 14-bit to 16-bit DACs, many are frustrated by the confusing specmanship played by DAC vendors. What a vendor might call a 16-bit device may not necessarily be accurate to a 16-bit level operating over the specified temperature range—or it may not be 16-bit monotonic. Monotonicity is the resolution at which, for every increase in the value of a digital word applied to the input, the output doesn't go negative but stays the same or increases.

Monotonicity is critical in closed-loop servo control applications. "Take a precision machine tool application, for example," says Pat O'Doherty, product marketing manager at Analog Devices (Norwood, MA). "If you're programming in codes to place a drill bit, those codes must constantly increase to move that drill bit in one direction. It's very important not to have, at any point, a decrease in the output."

Designed for closed-loop servo applications, such as control of machine tools and robotic systems, Analog Devices' AD7846 is 16-bit monotonic over a temperature range of –55 to +125°C. Built on a BiCMOS process, the AD7846 includes signal hold amplifiers (SHAs) to ensure a low-glitch buffered output. The part's low 100-mW power dissipation and small 28-pin package also makes it suitable for portable applications.

## AC for audio

In classic dc voltage-control applications, specifications such as accuracy, monotinicity and linearity are key. If you're doing signal reconstruction, however, such as playing back digital audio from a compact disc player or some other digital source, ac specifications take priority. "Audio signal-to-noise ratio (SNR) and total harmonic distortion are the important specifications because those things will degrade the spectral purity of the signal you're generating," says Doug Grant, strategic marketing manager at Analog Devices.

The latest buzzword to pervade the audio data converter world is sigma-delta. Also referred to as delta-sigma, or "bit stream," this conversion technique uses a very accurate one-bit DAC to convert a serial bit stream into a continuous analog signal. With a slower overall throughput than multibit DACs, sigma-delta parts have generally been restricted to audio speed applications. In fact, it's the audio market in which sigma-delta is able to directly replace multibit technology.

Unlike the multibit DAC architectures, sigma-delta is about 90 percent digital and only 10 percent analog (the modulator). As a result, data converter vendors have found it relatively easy to integrate one or more sigma-deltas, as well as support circuitry, on one chip. Exemplifying this trend are the integrated codecs (coder/decoders) announced late last year by Analog Devices and Crystal Semiconductor (Austin, TX). These integrate A-D/D-A converters and compression algorithms, all on the same chip.

For its part, Philips/Signetics (Sunnyvale, CA) offers the SAA7350, a 20-bit DAC that uses sigma-delta technology. Built using a CMOS process, the SAA7350 provides a choice of two system clock frequencies synchronized to the audio sam-

| Model | Resolution (bits) | Output (Voltage=V, Current=C) | Typical integral non-linearity (± LSB) | Internal reference (Y/N) | Gain error (±% of FSR) | Setting time (µs) (±1/2 LSB) (voltage/current) | Power dissipation (mW) | Process | Price | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| **Analog Devices** 1 Technology Way, PO Box 9106, Norwood, MA 02062-9106 (617) 329-4700 | | | | | | | | | | **Circle 301** |
| AD1851 | 16 | V, C | — | Y | 1.0 | 1.5/0.35 | 100 | ABCMOS | $12.60 | PCM audio DAC settles to 0.0015% FSR, 16X sampling |
| AD1856 | 16 | V, C | — | Y | 2.0 | 1.5/0.35 | 175 | BiMOS I | $12.60 | PCM audio DAC, settles to 0.006% FSR |
| AD1860 | 18 | V, C | — | Y | 2.0 | 1.5/0.35 | 110 | BiMOSII | $14.05 | PCM audio DAC, settles to 0.0015% FSR |
| AD1861 | 18 | V, C | — | Y | 1.0 | 1.5/0.35 | 100 | ABCMOS | $14.05 | PCM audio DAC settles to 0.0015% FSR, 16X oversampling |
| AD1862 | 20 | C | — | Y | 2.0 | -/0.35 | 288 | BiMOSII | $17.20 | audio DAC |
| AD1864 | 18 | V, C | — | Y | 1.0 | — | 225 | BiMOS I | $20.45 | dual PCM audio DAC, 8X oversampling |
| AD1865 | 18 | V, C | — | Y | 0.2 | — | 225 | ABCMOS | $20.45 | 18-bit dual PCM audio DAC, 16X oversampling |
| AD1868 | 18 | V | — | Y | 1.0 | — | 50 | ABCMOS | $11.70 | dual, PCM audio DAC, single 5V supply |
| AD669 | 16 | V, C | 1.0 | Y | 0.1 | — | 365 | BiMOSII | $16 | DACPORT |
| AD766 | 16 | V, C | — | Y | 2.0 | 1.5/0.35 | 120 | BiMOS I | $11 | DSP DAC, settles to ±0.003% FSR |
| AD7846 | 16 | V | 4.0 | N | 0.012 | 9 | 100 | $LC^2MOS$ | $19 | readback DAC |
| **Burr-Brown** 6550 South Bay Colony Dr, PO Box 11400, Tucson, AZ 85734 (602) 746-1111 | | | | | | | | | | **Circle 302** |
| DAC703 | 16 | V | 1.0 | Y | 0.10 | 4 | 530 | bipolar | $20 | precision multi-use |
| DAC707 | 16 | V | 2.0 | Y | 0.10 | 4 | 535 | hybrid | $22 | 16-bit µP interface |
| DAC708 | 16 | V | 2.0 | Y | 0.10 | 0.35 | 370 | hybrid | $41.80 | 8-bit µP interface or serial |
| DAC709 | 16 | V | 2.0 | Y | 0.10 | 4 | 535 | hybrid | $41.80 | 8-bit µP interface or serial |
| DAC725 | 16 | V | 2.0 | Y | 0.10 | 4 | 920 | hybrid | $37.40 | 8-bit µP interface or serial dual DAC |
| DAC729 | 18 | V, C | 2.0 | Y | 0.10 | 5/0.3 | 1220 | hybrid | $119.70 | — |
| DSP201/202 | 18 | V | 4.0 | Y | 1 | 4 | 280 | hybrid | — | dual audio DAC |
| PCM63 | 20 | V | 4.0 | Y | 1 | 0.2 | 225 | bipolar | $17.35 | audio DAC |
| PCM1700 | 18 | V | 4.0 | Y | 1 | 4 | 280 | bipolar | $16.10 | dual audio DAC |
| **Crystal Semiconductor** 4210 S Industrial Dr, Austin, TX 78744 (512) 445-7222 | | | | | | | | | | **Circle 303** |
| CS4328 | 18 | V | — | Y | — | — | 700 | CMOS | $29 | sigma-delta DAC, 93 dB harmonics |
| **Datel** 11 Cabot Blvd, Mansfield, MA 02048 (508) 339-3000 | | | | | | | | | | **Circle 304** |
| DAC-HP16 | 16 | V | 1 | Y | 0.1 | 15 | 660 | hybrid | $68 | meets mil-std-883 |
| **Harris Semiconductor** PO Box 883, Melbourne, FL 32902-0883 (800) 442-7747 | | | | | | | | | | **Circle 305** |
| ICL7121 | 16 | C | 0.0015 | N | 0.002 | 1.8 | 3 | CMOS | $18.95 | — |

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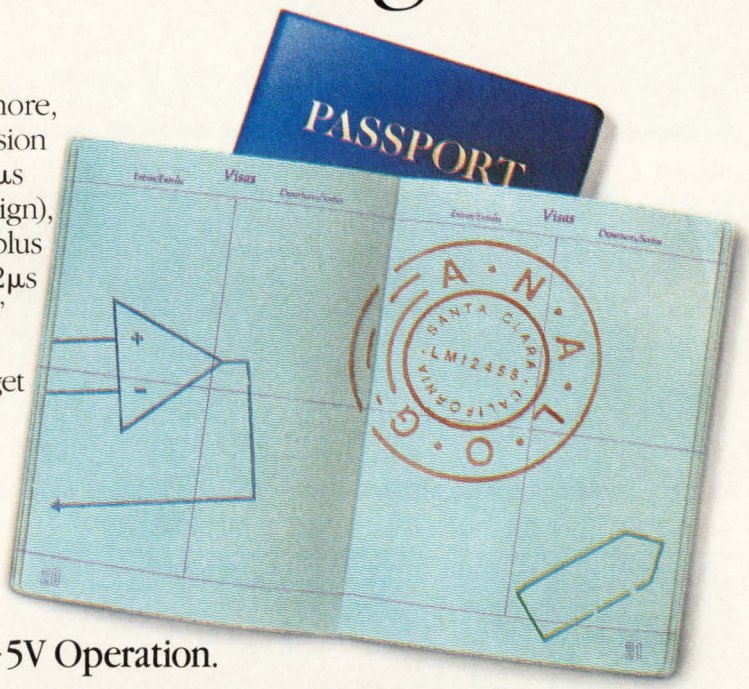


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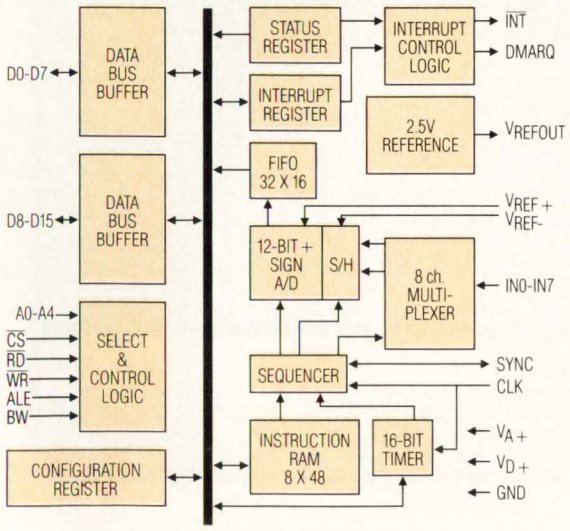


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| Model | Resolution (bits) | Output (Voltage=V, (Current=C) | Typical integral non-linearity (± LSB) | Internal reference (Y/N) | Gain error (±% of FSR) | Setting time (µs) (±1/2 LSB) (voltage/current) | Power dissipation (mW) | Process | Price | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| **Micro Networks** 34 Clark St, Worcester, MA 01606 (508) 852-5400 | | | | | | | | | | **Circle 306** |
| DAC71 | 16 | V, C | 1 | Y | ±0.05 | 10/1 | 525 | bipolar | $32.50 | industry standard |
| MN3290 Series | 16 | V, C | 1 | Y | ±0.1 | 8/1 | 525 | bipolar | $31 | full mil-temp and screening |
| **Micro Power Systems** 3100 Alfred St, Santa Clara, CA 95056 (408) 727-5350 | | | | | | | | | | **Circle 307** |
| MP7616 | 16 | C | 6 | N | 0.8 | 6 | 6 | CMOS | $16.71 | — |
| MP7626 | 16 | C | 1.5 | N | 0.1, 0.3 | 6 | 5 | CMOS | $27.30 | low-glitch energy |
| MP7636A | 16 | C | 1.5 | N | 0.1, 0.3 | 6 | 5 | CMOS | $25.90 | low-glitch energy |
| **Signetics** 811 E Arques Ave, Sunnyvale, CA 94088 (408) 991-2000 | | | | | | | | | | **Circle 308** |
| SAA7323 | 16 | V | 2 | Y | — | — | 300 | CMOS | $11.32 | — |
| SAA7350 | 20 | V | 1 | Y | — | — | 375 | CMOS | $22.66 | — |
| TDA1541AS1 | 16 | C | 0.5 | Y | — | 0.5 | 700 | CMOS | $11.87 | stereo DAC, 8X oversampling |
| TDA1545 | 16 | C | 1 | Y | — | 0.2 | 20 | CMOS | $3.14 | stereo DAC, 8X oversampling, 3 to 5.5V operation |
| TRA1543 | 16 | C | 1 | Y | — | 0.5 | 250 | CMOS | $3.14 | stereo DAC, 4X oversampling |
| TDA1547 | 20 | V | 0.2 | Y | — | — | 800 | BiCMOS | $18 | — |
| **Sipex** 22 Linnell Cir, Billerica, MA 01821 (508) 667-8700 | | | | | | | | | | **Circle 309** |
| DAC370 | 18 | C | 0.5 | N | 0.2 | 5 | 60 | hybrid | $166 | 4-quadrant multiplying, mil version avail. |
| DAC377 | 18 | V | 0.5 | Y | 0.15 | 20 | 400 | hybrid | $315 | mil version avail. |
| HS3160 | 16 | C | 0.5 | N | 1 | 2 | 30 | CMOS | $40 | mil version avail., decoded arch. |
| HS9371 | 16 | C | 0.5 | N | 0.1 | 5 | 45 | hybrid | $75 | 4-quadrant mult. mil version avail., 8/16-bit interface, double-buffered inputs |
| HS9378 | 16 | V | 0.5 | Y | 0.2 | 16 | 425 | hybrid | $149 | 8/16-bit interface, mil version avail., double-buffered inputs |
| HS9390 | 16 | C | 1 | Y | 0.1 | 150 ns | 900 | hybrid | $189 | segmented architecture, mil version avail. |
| SP7516 | 16 | C | 1 | N | 1 | 2 | 30 | CMOS | $30 | 4-quadrant multiplying |
| SP9316 | 16 | C | 1 | N | 0.2 | 2 | 60 | CMOS | $36 | 4-quadrant multiplying, high stability, mil version avail. |
| SP9320 | 16 | C | 1 | N | 0.2 | 2 | 120 | CMOS | $45 | double-buffered inputs |
| SP9380 | 18 | V | 0.2 | Y | 0.1 | 50 | 600 | hybrid | $300 | mil version avail., extremely stable, 18-bit monotonic |
| **Sony Semiconductor** 10833 Valley View St, Cypress, CA 90630 (714) 229-4189 | | | | | | | | | | **Circle 310** |
| CXD2552Q | 18 | V | — | N | — | — | 275 | CMOS | $13 | audio DAC, 96 dB S/N ratio |

pling frequency ($f_s$). The DAC will accept digital input formats of 16 to 20 bits at audio sampling frequencies from 16 to 53 kHz. The clock frequency can be either 256 × or 384 × $f_s$, with internal oversampling factors of 128 × or 192 × $f_s$. The part integrates third-order noise shapers designed to boost the SNR to 118 dB.

One problem with sigma-delta converters has been the crosstalk between digital and analog sections.

*When designers at Apogee needed to choose an audio D-A converter to use in their digital audio monitoring system, they decided that the sigma-delta converters, although cheaper, didn't have the performance they needed. Instead they chose the PCM63P, Burr-Brown's 20-bit audio DAC. They liked the way its dual-DAC per channel architecture prevents glitches.*

"That crosstalk has been limiting the specifications of sigma-delta converters," says Craig Aine, Signetics application engineer. "When placed in a series, sigma-delta converters can achieve incredible performance. In fact, they should be able to blow away the multibit devices without any problem, but the crosstalk limits their performance."

To break the crosstalk barrier, Signetics has done several things on the SAA7350. To reduce common-mode crosstalk, the part uses one-bit differential-mode switch capacitor DACs, as well as differential-mode post-filtering op-amps.

Despite its crosstalk-limiting features, the SAA7350 can't adequately operate in high-performance applications without its companion part, TDA1547. Containing only switch capacitor filters and post-filtering op-amps, the TDA1547 is itself a one-bit converter. To ensure that the analog and digital sections are well separated, 30 percent of the TDA1547's die is open space. Designers can rout the output of the SAA7350's noise shapers to the TDA1547. Because the TDA1547 is built on a BiCMOS process, it can use bipolar transistors in its digital section to reduce digital noise. The key here is to use both parts to isolate the digital processing in the SAA7350 from the analog processing in the TDA1547.

"When you look at the numbers that you can achieve using this two-chip solution, it's incredible," says Aine. Equivalent performance "would require at least a 24-bit multibit DAC (which is nonexistent), a dynamic range of 109 dB and a linearity deviation of less than 0.2 dB for input signals in the range of –60 to –120 dB. There's no way that a multibit D-A converter is ever going to get that close."

## One bit versus multibits

For engineers at Apogee (Santa Monica, CA), a maker of professional audio equipment used in recording studios, sigma-delta DACs just don't measure up. "Our experience is that the supposed 'high-resolution' one-bit DACs don't sound as good as a well-done multibit D-A converter," says Bruce Jackson, Apogee's chief engineer. "The one-bit sigma-delta or bit stream D-A converters are cheaper to produce and are, therefore, proliferating everywhere, but in the critical listening applications they just don't make it."

Having decided not to use a sigma-delta device, Apogee engineers had to choose from the available multibit audio converters for their digital audio monitoring system. "Our choice was the PCM63P, Burr-Brown's 20-bit audio D-A converter," says Jackson. "What's nice about that part is that there's no center most-significant bit (MSB) transition. The transition across the MSB is a least-significant bit (LSB) transition. The biggest error in D-A converters typically occurs in the MSB transition. So when you're listening to low-level music it's basically bouncing from one side of the MSB to the other side of the MSB. This puts all sorts of glitch energy and nastiness in the data stream." Other DACs get around this by offsetting the MSB to a point where the low-level music can't be detected.

Burr-Brown (Tucson, AZ) took a different approach on the PCM63P by integrating two DACs on-chip to share the transition task. As a result, one DAC can go all the way up to the center point while the other one goes from the center point to the next level. Because the second one starts on an LSB transition, the chance for error is reduced.

The PCM63P also offers a SNR of 116 dB and a –96 dB total harmonic distortion, plus noise (THD+N). According to Burr-Brown, the THD+N is essentially flat over the audio bandwidth. The PCM63P's current output settles in 200 ns for a 2-mA step—fast enough for 16× oversampling in the audio range. ■

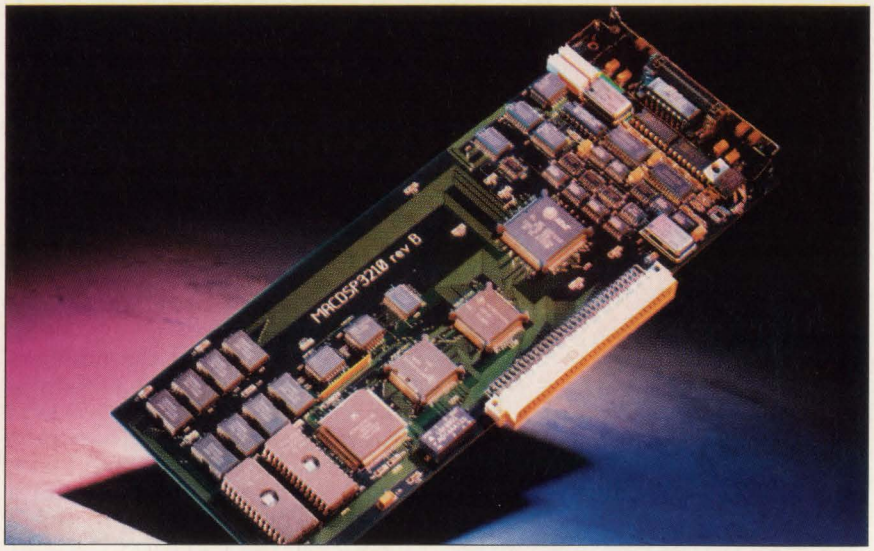
SOFTWARE & DEVELOPMENT TOOLS

# Board, software tools speed DSP development on Mac host

Software development support for systems based on AT&T's DSP3210 floating-point digital signal processor is available now as a bundled package from Spectral Innovations (Santa Clara, CA). Spectral has put together a development board with the DSP3210 for the Macintosh NuBus.

The company has also ported AT&T's VCOS Multimedia Development Environment (VMDE) to the Macintosh. (VCOS is AT&T's Virtual Cache Operating System for the DSP3210.) The MacDSP3210 board is oriented toward low-cost multimedia applications, but could be used for a wide variety of DSP systems using the 32-bit floating-point processor.

In addition to its DSP3210 processor, the board contains a Motorola 68020 that runs a VCOS application server. This server communicates with the host environment via Apple's A/Rose real-time operating system.




*The MacDSP3210 board and AT&T development software let designers use a Macintosh host system to develop low-cost multimedia and digital signal processing systems and applications.*

The DSP3210 processor runs at between 25 and 33 MFlops and has a full 32-bit address range and a 32-bit host port. It can share host memory and pass data over the NuBus. It can also reduce the need for special DSP memory for some applications that may run on desktop systems. The processor has 2,048 32-bit words of on-chip RAM and is compatible with Intel and Motorola processors.

The board also contains two analog-to-digital and two digital-to-analog channels that can interface directly to four Mbytes of on-board DRAM. The stereo analog converters can operate with 16-bit resolution at a sampling rate of 44.1 kHz for compact disc-compatible sound.

## Software tools

The software development tools that Spectral Innovations has licensed from AT&T include the VCOS multimedia development kit (VDK), the VCOS multimedia desktop (VMD) and a set of DSP3210 design tools.

The VCOS is a real-time, multitasking operating system that uses a technique developed by AT&T, called virtual caching, that lets

DSP chips share existing system memory. VCOS has a kernel that runs on the DSP3210, and the entire operating system runs as a task under the host operating system.

The VDK has tools for DSP algorithm and device driver development, and also for development of the VMD. The VMD includes an application server, the VCOS kernel and a module library. The module library provides a set of multimedia modules for such things as speech coding and recognition, modem/fax interfaces, data and image compression, and graphics. The modules can be used as examples or built into larger applications. The design tools include a C compiler, assembler, linker, and simulator for the DSP3210, along with a C library of DSP routines.

### Low-cost systems

The MacDSP3210 board and its support software are intended for developing low-cost systems and applications. The VCOS development environment is loaded on the board and runs under the 68020 processor, while the kernel executes on the DSP.

The kernel manages the processing, data communication and context switching for real-time and non-real-time tasks; the application server under the 68020 manages communication between host and kernel. Once an application development is complete, the four Mbytes of on-board DRAM are no longer needed, so a much less expensive production system can be manufactured.

Available 30 days after receipt of the order, the MacDSP3210 board is priced at $3,995 and the full Macintosh version of the VMDE is available for $1,995. The assembler, C compiler and simulator are also available separately for $1,500.

*— Tom Williams*

### *MacDSP3210 at a glance*

- 25 to 33 MFlops DSP
- Direct interface to host memory
- Stereo digital-to-analog and analog-to-digital channels
- Four Mbytes on-board DRAM
- 68020 processor for host/target communication
- VCOS DSP real-time, multitasking operating system
- Full set of development software and example library modules

**Spectral Innovations**
4633 Old Ironsides Dr
Suite 401
Santa Clara, CA 95054
(408) 727-1314
*Circle 352*

ASICs & ASIC DESIGN TOOLS

# MAX 7000 family faster, denser, more flexible than MAX 5000 parts

With the introduction of its Multiple Array matriX (MAX) 7000 family, Altera (San Jose, CA) is claiming to cover a broader range of applications than any other complex programmable logic device manufacturer. Designers can use the 0.8-µm devices, ranging in density from 4,000 to 40,000 gates and having as many as 288 pins, as alternatives to gate arrays or for PAL and GAL integration.

While incorporating the same basic elements as the MAX 5000 family, the MAX 7000 includes enhancements that deliver twice the speed, five times the density and more flexibility than the MAX 5000 architecture, claims Altera. Sandeep Vij, strategic marketing manager for Altera, says that MAX 7000 family members will be ahead of competing products in speed, density and pin count throughout this year.

Two MAX 7000 parts are available now. The denser of the pair is the EPROM-based EPM7256, a 256-macrocell EPLD with 164 I/Os and 10,000 gates; gate utilization is at about 50 percent. Altera states that the 7256 achieves 70-MHz in-system clock rates.

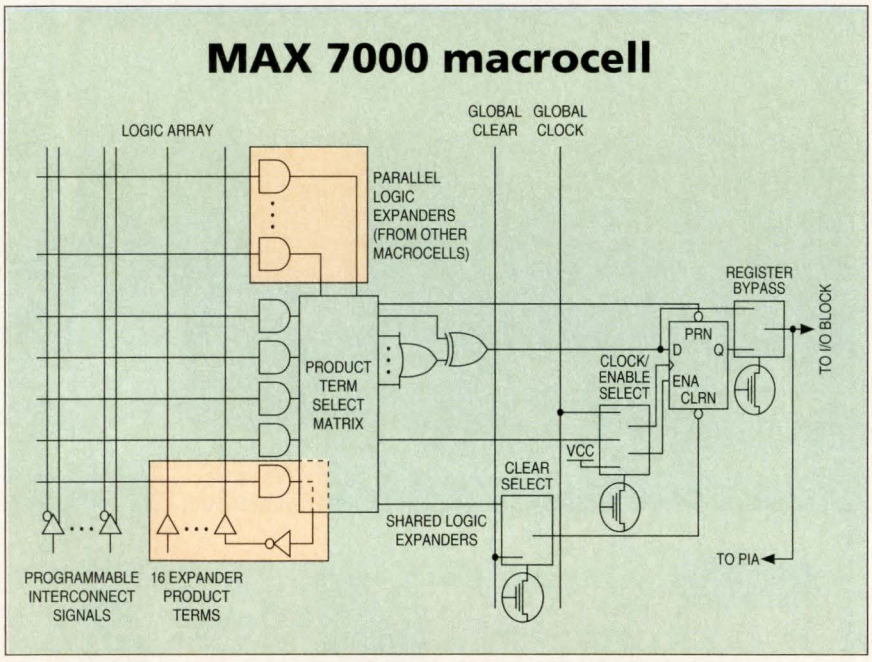
The second MAX 7000 family member, the EPM7032, is the first EEPROM-based EPLD from Altera. The 32-macrocell, 44-pin 7032 shares the same architectural features as the EPROM-based 7256. The only difference is that an electrical pulse erases the 7032, whereas UV light is required to erase the 7256. The 7032 has 12-ns logic delays and delivers in-system speeds of up to 83.3 MHz, according to the manufacturer.

The MAX 7000 has an improved Programmable Interconnect Array (PIA), or programmble wiring path between Logic Array Blocks (LABs), that gives a 3-ns signal delay between any two logic elements on the device. Although it's fed by all macrocell and I/O pin feedbacks, the PIA routes only the signals required to implement logic in each LAB.

For complex logic functions that can't be built with the five basic product terms in each MAX 7000 macrocell, the new architecture provides extra product terms called logic expanders. There are 16 shared logic expanders in each LAB, each with an inverting output that feeds back into the LAB. Use of these expanders incurs a 6-ns logic delay. Parallel logic expanders employ unused product terms from macrocells in the LAB to construct fast, complex logic. These expanders cause only a 2-ns delay, according to Altera.

Altera's MAX+PLUS II software, available for PCs and workstations, supports the design of MAX 7000 EPLDs. The Windows 3.0-based design system includes schematic, text and waveform design entry, as well as automatic logic synthesis and design partitioning into multiple EPLDs. Design verification options include a full timing simulator, timing analyzer and delay predictor. For Sun and H-P/Apollo workstation users, Altera offers the MAX+PLUS II compiler, with EDIF netlist input and output for use with tools from Cadence/Valid, Mentor Graphics and Logic Automation.

The EPM7256, packaged in a 192-pin windowed, erasable, ceramic pin grid array, is available now in single-unit quantities at a price of $395. The EPM7032, packaged in a 44-pin plastic-leaded chip carrier, is available at a price of $14.75 in 100-unit quantities. —*Barbara Tuck Egan*




***Macrocells within the MAX 7000 LAB provide both sequential and combinatorial logic capability, ensuring the most efficient implementation of a wide range of logic functions, according to Altera. Built into the MAX 7000 architecture are two types of logic expanders, shared and parallel (shaded areas); they provide additional product terms directly to any macrocell.***

## Max 7000 family at a glance

- 0.8-µm CMOS EPLD family with from 4,000 to 40,000 gates and pin counts to 288
- EPROM-based EPLD with 10,000 gates and 164 I/Os
- Single, uniform signal delay between any two logic elements
- Extra product terms called logic expanders
- Supported by Windows 3.0-based MAX+PLUS II toolset

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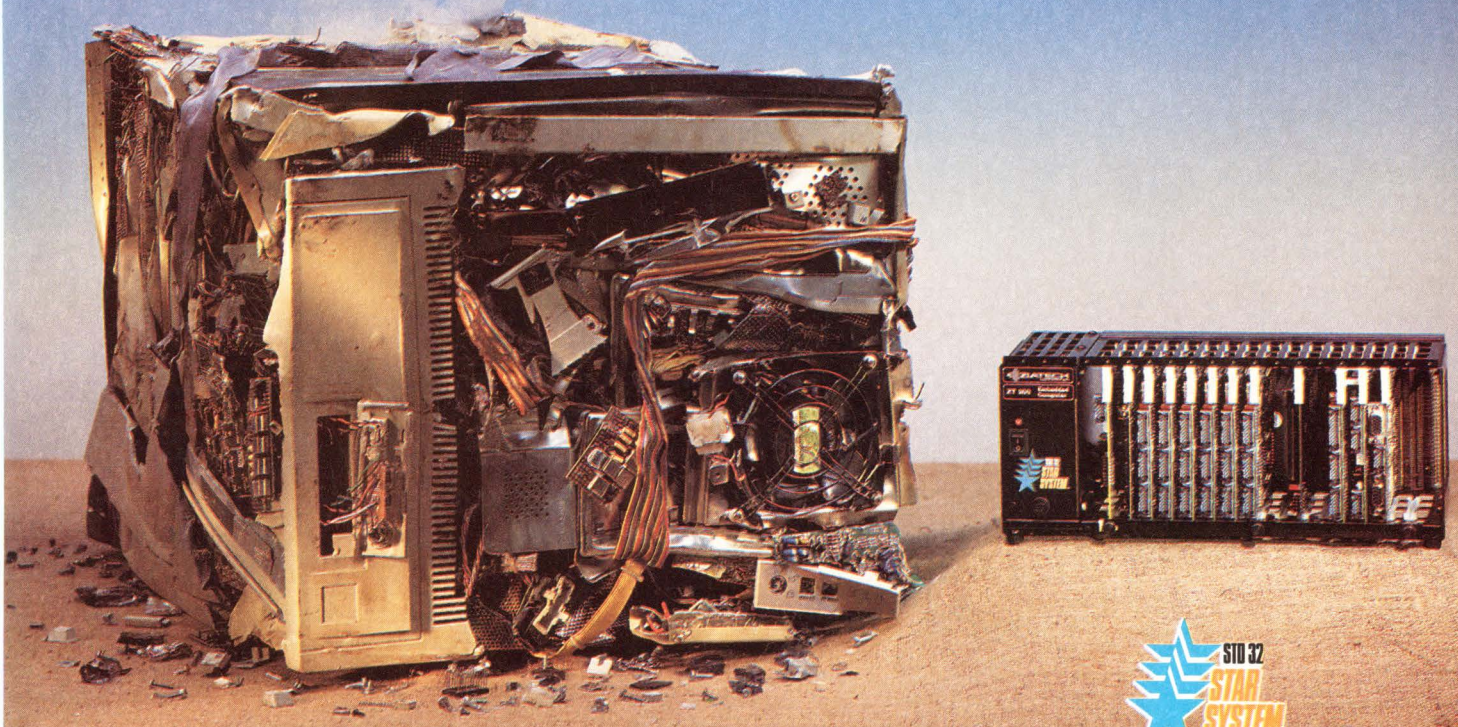

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# OEM PRODUCT UPDATE

## Canon Laser Beam Printer Family

The Canon family of OEM Laser Beam Printer Engines comprises the largest installed base in the laser printer market. This success has been built on Canon's well-documented reputation for reliability and low maintenance, innovation and high quality images.

There's a Canon engine for every OEM application. Personal printers. Desktop publishing and printing. Spreadsheets. Engineering. Graphics production. CAD/CAM. A unique feature of Canon's table top models is the patented EP cartridge system. Housing virtually all consumables, the EP cartridge makes user maintenance simple.

As an OEM associated with Canon, you'll work with a leader in laser technology and engine reliability. You'll get the product and technical support you need to serve existing customers and respond to emerging market opportunities.

For more information, call **1-800-323-0766**. Or write to Canon USA, Inc., OEM Operations, Printer Division, One Canon Plaza, Lake Success, NY 11042-1113.

**Canon**
**OEM Operations**
**Printer Division**



### LBP-LX Laser Beam Printer Engine

A compact, affordable printer engine ideal for desktop applications. Utilizes the disposable EP-L cartridge. Available in both Video (external OEM controller) and PCB (internal OEM controller) models.

| | |
|---|---|
| Monthly prints: | 750 |
| Resolution: | 300/400 dpi |
| Print Speed (PPM): | 4 |
| Dimensions: | 16.7"W x 14.1"D x7.6"H |

### LBP-SX

The most popular laser beam printer in the world. Clamshell top cover permits easy access to paper path and disposable EP-S image cartridge. Available in Video and PCB models.

| | |
|---|---|
| Monthly prints: | 5000 |
| Resolution: | 300/400 dpi |
| Print speed (PPM): | 8 |
| Dimensions: | 18"W x 19.5"D x 9.1"H |

### LBP-TX and LBP-RX

Hard-working laser beam printers featuring expanded paper handling. The RX model offers duplex capability. Dual cassettes hold up to 400 sheets and two types of paper. EP-S cartridge in all versions. Available in Video and PCB models.

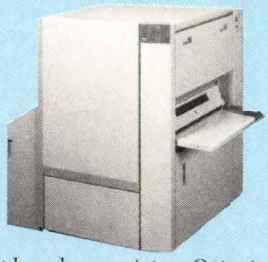
| | |
|---|---|
| Monthly prints: | 5000 |
| Resolution: | 300/400 dpi |
| Print speed (PPM): | |
| TX Simplex | 8 |
| RX Duplex | 7 (impressions) |
| Dimensions: | TX 18"W x 19.5"D x 12.5"H |
| | RX 18"W x 25.0"D x 12.5"H |

### LBP-20

A heavy-duty laser beam printer for large-format printing. Modular design allows multiple product configurations.

| | |
|---|---|
| Monthly prints: | 30,000 |
| Resolution: | 300/400/480 dpi |
| Print speed (PPM): | |
| Simplex: Letter | 20 |
| 11" x 17" | 10 |
| Duplex: Letter | 14 (impressions) |
| 11" x 17" | 8 (impressions) |
| Dimensions: | 29"W x 24"D x 20"H |

### LBP-DX



Our largest-format laser beam printer. Outputs high-quality photographs, halftones and line art prints on vellum or paper. Ideal for engineering and graphics production. Handles 500-foot rolls of 24" wide paper or cut sheet sizes up to D (24" x 36").

| | |
|---|---|
| Monthly prints: | 5000 |
| Resolution: | 400/508 dpi |
| Print speed (PPM): | |
| D size (24" x 36") | 3 |
| C size (18" x 24") | 5 |
| Dimensions: | 30"W x 39"D x 46"H |

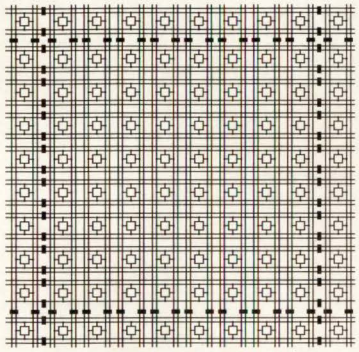
**CIRCLE NO. 69**

*ASICs & ASIC DESIGN TOOLS*

## Register-rich FPGA for pipelined designs

The CLi6000 series of SRAM-based FPGAs, introduced by start-up Concurrent Logic (Sunnyvale, CA), is fabricated in 0.8-µm CMOS and can accommodate system performance of up to 70 MHz, the company claims. Density for the reprogrammable arrays ranges from 1,200 to 10,000 gates, with utilization anywhere from 50 to 100 percent for register-intensive designs, according to Concurrent. The first member of the family is the 132-pin, 5,000-gate CLi6005, with 108 I/Os.

### Bussing network




***For design flexibility, Concurrent Logic developed a symmetrical array of identical cells for its CLi6000 FPGAs. Except for "repeaters," or connective units spaced every eight cells, the array is continuous and completely uninterrupted from one edge to the other. Repeaters are aligned in rows and columns, thereby partitioning the array into 8 × 8 blocks of cells.***

The CLi6000 series has a symmetrical, register-rich architecture that lends itself to register-intensive, pipelined designs. The CLi6005 is a symmetrical array of 3,136 cells. Since each logic cell can function as a register, 3,136 registers are available for applications such as noise reduction, pattern recognition or video compression and decompression. Connective units or repeaters divide each bus—both local and express—into segments spanning eight cells. They can be programmed to provide any one of 29 connecting functions.

Along the top edge of the CLi6005 array is logic for distributing clock signals to the D flip-flop in each logic cell. The distributed network is organized by column, permitting columns of cells to be independently clocked. Through the global clock, the network provides low-skew distribution of an externally supplied clock to any or all the columns of the array. Along the bottom of the array is logic for asynchronously resetting the D flip-flops in the logic cells.

Concurrent Logic's suite of design tools for the CLi6000 series includes schematic capture and simulation using Viewlogic System's Viewdraw and Viewsim, logic optimization, schematic regeneration, automatic or manual placement and routing, and pre- and post-layout timing analysis. Concurrent also offers a library of over 200 fully specified hard and soft macros. CLi6000 design tools run on any 80386- or 80486-based IBM or fully-compatible PC with MS-DOS Versions 3.0 to 4.01. Versions for use on Sun Workstations will be available in the second quarter of 1992.

The CLi6005 is available in an 84-pin PLCC and a 132-pin PQFP. Engineering samples are available now, with commercial quantities expected in April. Price in volume will be $180.

CLi6000 design tools are offered in four modules. The Basic Design Package, including the Design Manager, Viewdraw schematic capture, interactive layout editor, and macro library, is priced at $3,995. The Timing Analysis Tools Package is $2,995. *—Barbara Tuck Egan*

### *The CLi6005 FPGA at a glance*

- 0.8-µm CMOS SRAM-based symmetrical array
- Register-rich architecture for pipelined designs
- 5,000 gates and 3,136 cells
- Toggle rate to 150 MHz and in-system speed to 70 MHz
- 132-pin device with 108 I/Os

**Concurrent Logic**
1270 Oakmeade Pkwy
Sunnyvale, CA 94086
(408) 522-8700
*Circle 353*

INTEGRATED CIRCUITS

# MCU series delivers 16-bit punch in an 8-bit package

Designers hunting for something new in 8- and 16-bit microcontrollers haven't had many options recently, aside from slightly revamped derivatives. With its new H8/500 series of high-performance microcontrollers, however, Hitachi seems determined to break this trend by offering a completely new architecture targeted for systems that need 16-bit processing in an 8-bit package.

Following the path of Hitachi's H8/300 MCU family introduced last year, the company's H8/500 series targets designers interested in upgrading beyond standard 8-bit performance without a significant cost penalty. Unlike the H8/300, however, the H8/500 is built to rival 16-bit MCU performance.

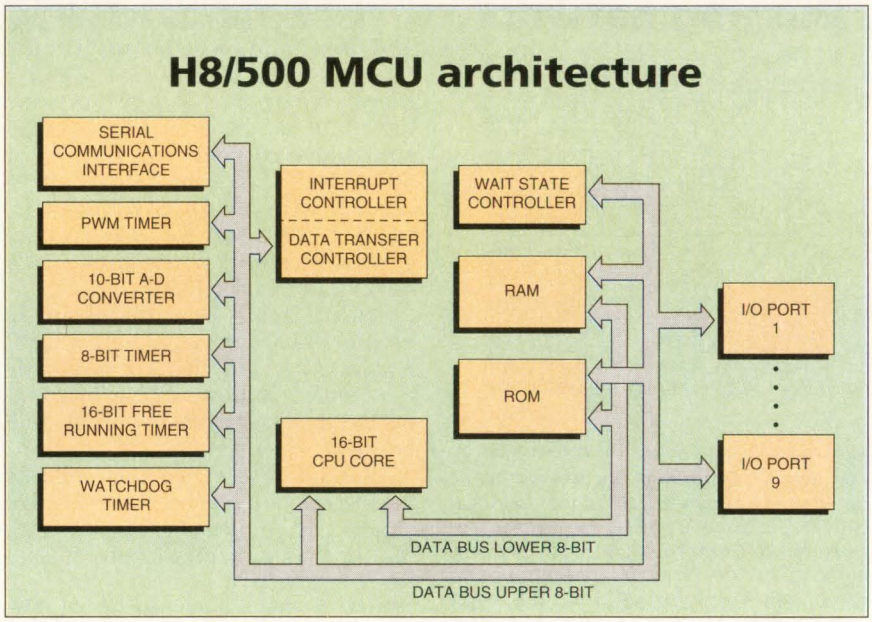
Although the assembler code is compatible with the H8/300's, the H8/500 uses a less RISC-like instruction format. Instructions are variable in length (from two to seven bytes) and are not of fixed size.

## Suited for C

Because more and more designers are writing embedded code in C, Hitachi made sure the H8/500 is especially suited for high-level language use. To accommodate the large overhead of code typical when using high-level languages, the device provides up to 62 kbytes of on-chip ROM and a 16-Mbyte address range. And, with up to two kbytes of RAM, the H8/500 can handle operations, such as parameter passing, that occur often when high-level language code is used. The chip's highly orthogonal instruction set optimizes C compiler use and increases execution speeds.

While the controller's external data path is eight bits wide, it has a full 16-bit internal CPU. The H8/500 has a minimum instruction cycle time of 200 ns and a 10-MHz clock rate. In benchmark tests, the H8/500's performance is about 60 percent higher than that of the most widely used 16-bit microcontrollers, and two to three times higher than standard 8-bit parts.

The key to the H8/500's performance is its innovative instruction format. This format increases the CPU's performance by enabling the effective address to be calculated




*While the H8/500's CPU core and internal CPU-to-memory data bus are 16 bits wide, the chip's data transfer controller can be programmed to automatically move 8- or 16-bit values between any type of on-chip peripheral including timers, interrupt controllers, memory, and general-purpose I/O. Address bus not shown.*

and the data to be fetched while the instruction is being decoded.

### Peripheral packed

Hitachi squeezed a wide selection of high-performance peripherals on to the H8/500. The 10-bit A-D converter on-board offers a 13.8 µs conversion speed. Also impressive is the internal, full-duplex serial communications interface that transfers data at up to 2.5 Mbits/s.

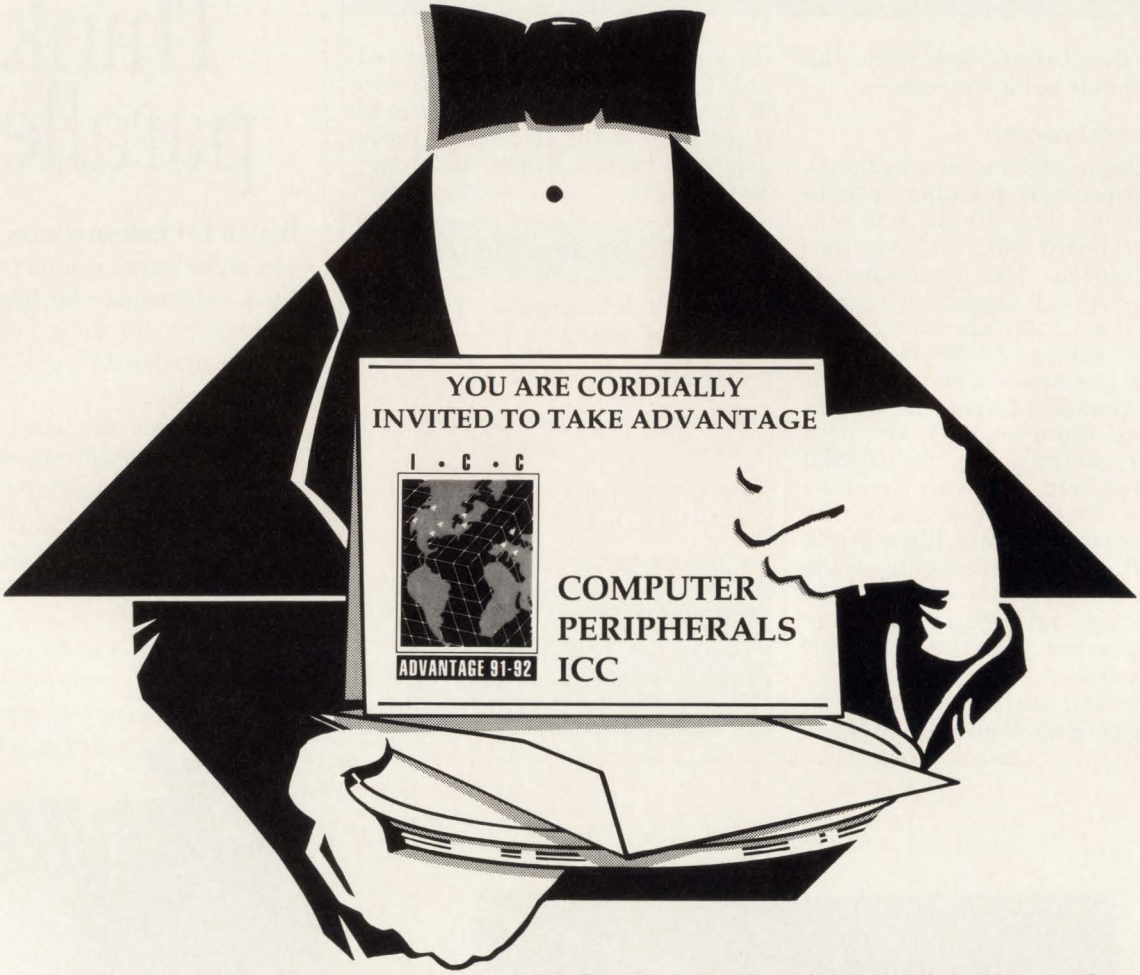
Other peripherals include eight on-chip timers, interrupt controllers and general-purpose I/O. The data transfer controller on the H8/500 can perform direct memory accesses. This controller can be programmed to automatically move 8- or 16-bit values between any of the on-chip peripherals and on-chip memory without CPU intervention.

Available now, prices for the H8/500 microcontroller vary depending on memory size, peripheral configuration and package choice. The H8/520, the lowest-cost family member priced at $11.45. Prices for the H8/536, with 62 kbytes of ROM and two kbytes of RAM, begin at $34.10. Package types available include 84-pin PLCC and 80-pin PQFP. — *Jeffrey Child*

#### *H8/500 at a glance*

- 10-MHz, 8-bit external, 16-bit internal microcontrollers
- Up to 62 kbytes of ROM
- Suited for high-level language use
- 200 - 300 percent faster than any 8-bit microcontroller
- Broad selection of peripherals

**Hitachi America**
2000 Sierra Point Pkwy
Brisbane, CA 94005-1835
(800) 448-2244
***Circle 359***

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**CIRCLE NO. 74**

INTEGRATED CIRCUITS

# Fast, wide, two-way TTL/ECL translators

Designers of CMOS and bipolar TTL systems can achieve greater performance by using ECL parts in portions of their designs where speed is critical. Key to this approach may be a new bidirectional TTL/ECL translator/driver implemented in BiCMOS from Cypress Semiconductor—the CY10E/101E383.

Each CY10E/101E383 TTL/ECL translator-driver can support 10 independent channels in each direction. Propagation delay in the TTL-ECL direction is 3 ns, in the ECL-TTL direction it's 4 ns. The device is designed with ample ground pins to reduce bounce and has separate ECL and TTL power and ground pins to reduce noise coupling between logic families. The part can be powered by a traditional dual power supply or a single-voltage +5V TTL supply, while still providing full single- or double-ended ECL I/O. It's offered in standard 10K/10KH (10E) and 100K (101E) ECL-compatible versions with –5.2V or –4.5V power supply. The TTL I/O is fully TTL compatible.

## ECL used anywhere

The differential (double-ended) ECL signaling offered by the CY10E/101E383 lets you use the chips for backplane signaling, even when you don't use ECL anywhere else in the system. The ECL differential mode helps minimize noise in backplane buses in three ways: low voltage swing minimizes slew rate, reducing electromagnetic interference; transmission line design rules for ECL are clearly established, making it simple to implement terminations; and double-ended signaling virtually eliminates susceptibility to common mode interference, minimizing shielding requirements.

The device has internal 2kΩ pulldown resistors on each ECL output. They are tied to $V_{ee}$ to decrease the number of external components. For system testing purposes or for driving light loads, the resistors are used as the only termination, thereby eliminating up to 20 external resistors. The part meets the standard 10K/10KH logic levels with the internal pulldown while driving 50Ω loads to –2V.

The CY10E/101E383's ECL differential I/O lets TTL-based systems exchange data transmissions at up to 300 MHz via ECL over long cables in noisy media such as unshielded ribbon and twisted-pair as well as coaxial cables. The ECL differential I/O cancels out common noise, allowing the use of less expensive cables such as ribbon or twisted-pair. Specifically, common-mode noise reduction decreases crosstalk in twisted-pair cable, and the reduced skew between differential outputs lessens electromagnetic interference. The result is high-speed, high-integrity data transmission over inexpensive media.

Cypress claims that the CY10E/101E383's 20 channels offer greater density than the four to six channels available in competing solutions, allowing the part to replace three to five devices. The part itself is available in an 84-pin surface-mountable plastic leadless chip carrier (PLCC) package. In quantities of 100, the unit price is $37. — *Dave Wilson*

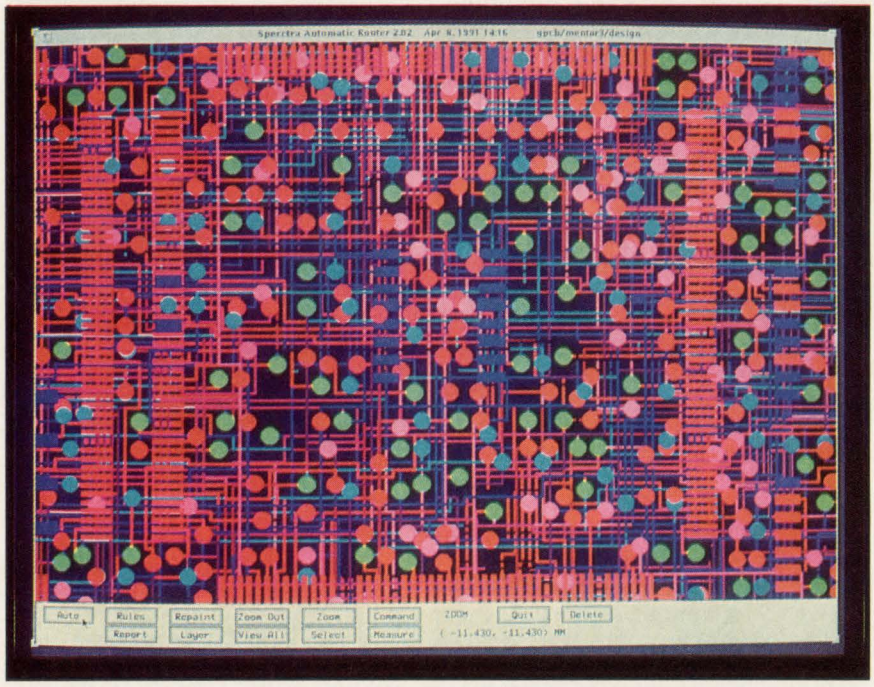
### CY10E/101E383 at a glance

- ECL differential I/O mode minimizes noise
- Greater density than competing parts
- TTL-ECL propagation delay of 3 ns
- Dual power supply or single-voltage +5V TTL supply

**Cypress Semiconductor**
3901 North First St
San Jose, CA 95134
(408) 943-2600
*Circle 355*

CAE/CAD TOOLS

# Autorouters target surface-mount, high-speed PCBs




*The Specctra autorouters incorporate complex design rules into the autorouting algorithms to account for SMD-specific manufacturing constraints. Soldering requirements, component densities and through-hole options are considered during routing.*

Cooper and Chyan's latest version of its shape-based autorouter, Specctra Version 3.01, boasts the flexibility to take advantage of the latest advances in device technology while retaining the rules needed to use older, less-costly packaging options whenever possible. Autorouters in particular must also have built-in intelligence to place traces that accommodate the technology of choice during the route while following rules for manufacturability; Specctra 3.01 has this ability as well.

The new release is composed of two products, SP20 and SP50. The SP20 provides autorouting solutions for the special requirements of high-density surface-mount device (SMD) PCBs with complex design rules, while the SP50 adds features such as crosstalk and wire length control that handle the special requirements of high-speed PCBs. Both Specctra products provide automatic functions that let you incorporate manufacturing requirements into the autorouting process.

Surface-mount technology requires that you follow specific design rules during the component placement and routing processes, or the resulting PCB will be inefficient or unmanufacturable. The router, for example, must take into consideration the escape distance from a surface-mount pad to the first bend point in the wire. A wire bend that's too close to the surface-mount pad increases the risk of an acid trap that could cause a solder bridge between the wire and the SMD pad. To remedy this condition, Specctra provides a special clearance rule to control this distance and avoid shorts and manufacturing defects.

## Soldering considerations

Another SMD constraint involves the distance between a surface-mount pad and the first via in the wire attached to that pad. A process that applies heat, such as wave soldering or board rework, may radiate heat through the via and keep the SMD pad from maintaining sufficient heat during the process. SMD components may "float" because of this, resulting in open or intermittent connection between the component lead and the pad. The distance from an SMD pad to an adjacent via that's not in the same net, however, isn't as critical because there's no direct connection between the SMD pad and the via. The Specctra autorouters provide a specific clearance rule that controls the distance from an SMD pad to the first via in the same net and a more general rule for the distance between SMD pads and vias of different nets.

In some instances, SMD technology lets you place through-hole or "buried" vias on or under surface-mount pads, permitting maximum space utilization during autorouting. Manufacturing results for boards using vias on or under SMD pads are improved when the via is placed completely within the SMD pad boundary, eliminating possible solder bridging to adjacent pads and wires. Specctra's special "fit" parameter selects a via from those available to fit within the boundaries of the SMD pad. If the router can't find a via that fits, a via is placed outside the pad boundary.

Specctra autorouters are available on most Unix workstations, including Apollo DN4000, DECstation, H-P 700 and 9000 series, IBM RISC System 6000, and Sun Sparcstations. Both autorouters are available now. The SP20 is priced from $29,900, the SP50 from $44,900. — *Mike Donlin*

### *Specctra at a glance*

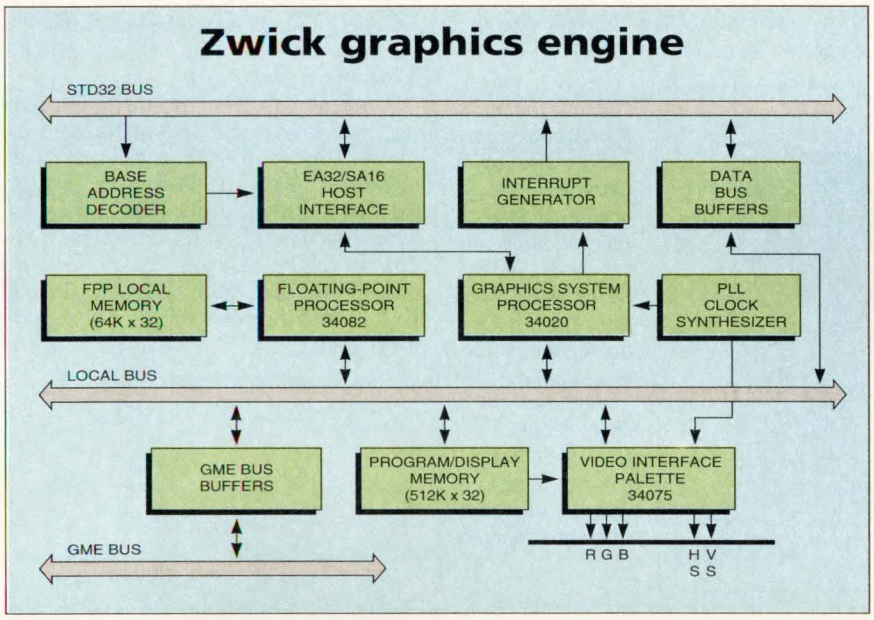
- Two products are available in the Specctra autorouter Version 3.01—SP20 and SP50
- SP20 provides autorouting solutions for high-density surface-mount PCBs
- SP50 adds a set of design rules for fast circuit considerations such as crosstalk and wire length control
- Runs on Unix workstations from Apollo, DEC, H-P, IBM, and Sun
- The SP20 is priced from $29,900; the SP50 from $44,900

**Cooper and Chyan Technology**
1601 Saratoga-Sunnyvale Rd
Suite 255
Cupertino, CA 95014
(408) 366-6966
***Circle 351***

COMPUTERS & SUBSYSTEMS

# STD32 bus gets high-performance graphics card

Though the STD32 standard is still in its infancy, Zwick Systems (Nepean, Ontario) is already offering a high-performance graphics card based on this 32-bit alternative to STD80. Called the Zwick Graphics Engine (ZSTD-778), the company's new card is based on the 32-MHz version of Texas Instruments' TMS34020 Graphics System Processor. The board features up to two Mbytes of high-speed dual-port video memory and full support for 32-bit extended architecture with complete STD80 backward compatibility.




*One of the first high-resolution graphics engines to emerge on STD32 provides flexibility by using a multiple-bus architecture. It uses its own local bus in addition to the STD32 host bus. It also provides a GME (Graphics Memory Expansion) bus which is essentially an extension or pin-out of the graphics processor. The GME also lets the board operate with other subsystems adhering to the GME specification.*

## Variety of formats

The Zwick board provides a broad variety of standard video display formats, ranging from 640 × 480 to 1280 × 1024 60-Hz noninterlaced, and 1024 × 768 43.49-Hz interlaced. It also has a flexible programmable frame buffer organization offering anywhere from one to 32 bits per pixel. In addition, the Video Interface Palette permits the selection of 256 colors from a 16-million-color palette and has a 24-bit "true color" mode with 8 bits per pixel of graphics overlay on the true color input.

The on-board dual-port memory serves for both program and video memory and is dynamically allocated at run time. The VRAMs support the TMS34020's special function cycles, including color mask load, block write, and write mask. The board is configured with RS-343-compatible RGB outputs, with separate TTL, HSYNC, VSYNC, and programmable HSYNC-on-green capability. It uses an industry-standard DB9 card-edge connector for ease of system integration.

The Zwick Graphics Engine also offers an optional floating-point processor—TI's TMS34082—with up to 256 kbytes of local high-speed memory. Operating at 40 MFlops, this processor increases system performance in calculation-intensive applications such as 3-D imaging and fractal graphics. Further advantages can be gained by adding local SRAM to the floating-point processor bus, so that it can act independently of the parallel processor in the system.

The makers of the board have in addition provided a high-speed GME (graphics memory expansion) bus, which includes an extension of the graphics processor's local bus and supports operation with other special-function GME-bus-compatible modules such as Video Frame Capture, Image Compression, Memory Expansion, and SCSI2 interface cards. The GME offers the advantage of removing most of the graphics processing overhead from the system, reducing traffic and freeing the STD32 system bus for other operations. Drivers supporting the Texas Instruments Graphic Architecture (TIGA) are available and let the card take advantage of hundreds of existing software programs.

Zwick Systems expects that availability of the new card will open up many new opportunities for the STD32 architecture. Already there are nine companies supporting the bus, with products ranging from CPU cards to highly flexible I/O cards. Zwick's Graphics Engine is the first card to provide high-performance graphics to 8-, 16- and 32-bit systems based on either the STD80 or STD32 specification. The card is priced at just under $1,000 in OEM quantities. — *Warren Andrews*

### ZSTD-778 at a glance

- Full STD32 architecture
- STD80 compatibility
- Resolution up to 1280 × 1024, 60 Hz, noninterlaced
- Programmable frame buffer organization
- 256 of 16 million colors, or 24-bit "true-color" capability
- Two-Mbyte, high-speed video memory
- Optional floating-point processor

**Zwick Systems**
17 Fitzgerald Rd
Suite 104
Nepean, Ontario, Canada
(613) 726-1377
***Circle 358***

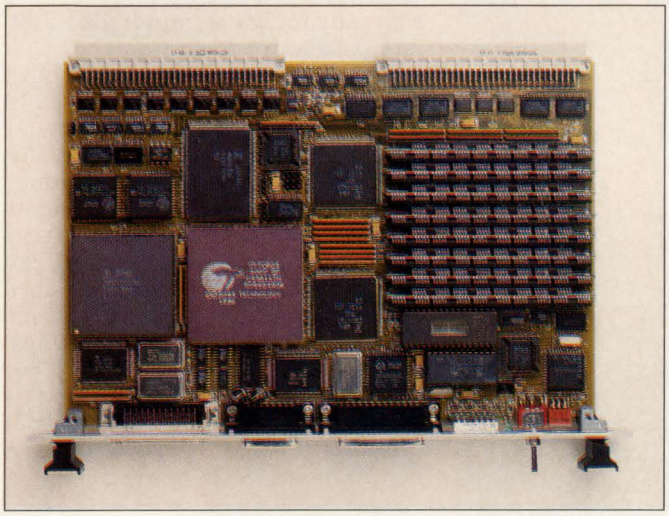
COMPUTERS & SUBSYSTEMS

# Full-featured Sparcstation 2 surfaces on VMEbus

One of the industry's first full-featured Sparcstation 2 products in a standard 6U VMEbus format comes from board maker Themis Computer Systems (Pleasanton, CA), better known for its 680X0 CPU boards and its broad array of communications products. The new board, based on the Sparc M bus architecture, uses 40-MHz integer and floating point processors to achieve a full 30 Mips.

Themis announced two versions of its SparCard product: the 2LC, designed as a low-cost single-board computer, and the 2SE, providing a complete workstation environment, including a pair of SBus slots. In addition, says Themis president Bill Kehret, a third version that will offer full multiprocessing support will be available later this year. All three versions will fully support SunOS for Unix applications and either Wind River's VxWorks RTOS or Lynx Systems' Posix 1003.4 Version 9-compliant LynxOS.

"One of the keys to the performance of our SparCard compared with other VMEbus offerings," says Kehret, "is the fact that the main internal bus is designed around the high-performance, 64-bit M bus—the same one used in Sun Microsystems' recently announced server, Galaxy."



*The first SunOS Sparcstation-compatible VMEbus CPU to emerge outside of Sun is this 2SE high-performance single-board computer from Themis. The board, the first to be designed around the Sparc M bus, features SCSI and Ethernet ports as well as a selection of memory options.*

## Advantage: flexibility

"This offers us a number of advantages," he adds. "First, it will let us easily scale our design up as newer and better processors become available from any of the major Sparc chip makers, including Fujitsu, Cypress, Texas Instruments, or LSI Logic. Second, it will also let us quickly migrate to any M bus-based multiprocessing scheme, such as [the one] currently implemented in Cypress' 605 CMU. And finally, M bus provides a 64-bit data path which will let us migrate, when required, to handle 64-bit transfers."

Sun won the race to be first to market with a second-generation Sparcstation VME board (its 2E board), but it's likely that other manufacturers such as Themis and Force will strip Sun's board of the performance honors. The Themis board is based on the latest 64-bit M bus architecture, while the Sun 2E uses an earlier proprietary 32-bit internal bus structure with no ready upgrade path to future higher-performance processors.

## Host of features

Themis' low-cost OEM solution, the SparCard 2LC, includes most of the features OEMs need for embedded applications. The 40-MHz processor is supported by a 64-kbyte cache, 8- to 32-Mbyte DRAM, Ethernet, SCSI, a pair of serial channels, and, of course, a full VMEbus interface. In addition, it has a host of other features that designers would expect to find in a single-board computer.

The VMEbus interface is implemented with the Fujitsu Microelectronics MVIC IC. The card is priced at $5,995, and, according to Kehret, offers twice the Mips performance of Motorola's 68040-based MVME167. Kehret adds that the company has not yet completed the Specmark testing, but he expects the board to perform at the same relative level or better.

The SparCard 2SE is designed to provide more of a workstation environment than the 2LC. In addition to all the features provided on the other member of the family, the 2SE can handle up to 64 Mbytes of DRAM, features two SBus slots and includes on-board SCSI 2. It sells for $7,995.

Both boards also include byte parity, two kbytes of SRAM backed up by battery power, a memory management unit, a 64-Gbyte virtual address space, and 256 contexts. The boards also have three programmable timers, a real-time clock/calendar, boot EPROM plus ID ROM, and a front-panel diagnostic indicator. — *Warren Andrews*

### *SparCard 2SE at a glance*

- 40-MHz Sparc MPU
- VMEbus block transfer up to 50 Mbytes/s
- Up to 30 Mips
- 64 kbytes cache memory
- Integrated floating-point coprocessor
- 64 Mbytes DRAM
- Two-kbyte battery-backed-up SRAM
- Two SBus slots
- On-board SCSI 2
- Front-panel diagnostic indicator

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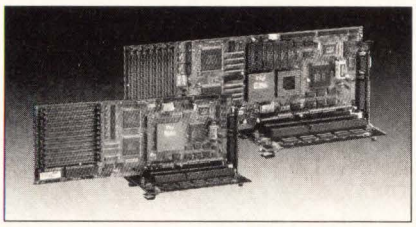
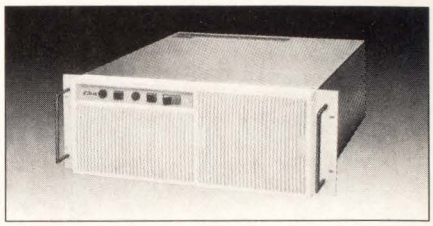
### I386, I486 single board computers—versatile, powerful



Built around a 25-33MHz 80386DX, the versatile I386 features 32K cache (I386/25), or 128K cache (I386/33), with up to 32MB of 70ns SIMM DRAM, plus either an 80387DX Coprocessor or a Weitek 3176 Numeric Data Processor. The I486 offers superior processing power for any system configuration using either the 80486DX (25 or 33 MHz) or 80486SX (25MHz) CPU, with optional 256K cache. Both incorporate an IDE hard disk interface, a floppy disk controller, two serial and one parallel port, and a programmable Watchdog timer. **Contact I-Bus,** 9596 Chesapeake Drive, San Diego, CA 92127. **Tel. (800) 382-4229, Fax (619) 268-7863.**

**CIRCLE NO. 76**

### Model 4820 — maximum slots, maximum disks



Now for the first time, OEMs and Systems Integrators can implement designs incorporating up to 20 full-length AT cards, using the new 4820 enclosure from I-Bus to advance current limits of passive backplane enclosure technology. Rack mount, tower and desktop configurations provide an adjustable mechanical hold-down bar, plus front access to up to five half-height drives or two full-height drives and one half-height floppy drive, in a shock-mounted drive bay. Options include 275W or 375W power supplies. **Contact I-Bus,** 9596 Chesapeake Drive, San Diego, CA 92127. **Tel. (800) 382-4229, Fax (619) 268-7863.**

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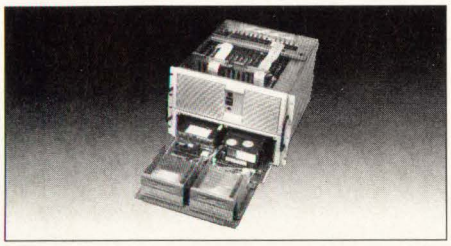

### Customer input guides Model 16I Enclosure design

Design and development of the revolutionary new 16I PC Bus System from I-Bus has been totally governed by customer input – as the 16I's unparalleled array of features demonstrates. The 16I offers 16 full-length AT slots, with an adjustable mechanical hold-down bar. 275W or 375W power supplies are optional. Or, if the backplane is segmented (8X8), two separate 150W power supplies are provided, one dedicated to each segment. Power supplies are easily replaced on their own service module. Up to eight half-height drives or four full-height drives (or any combination) are located in a shock-mounted drive bay, accessed from the front via a slide-out drive drawer for easy drive addition or replacement. Rack mount, tower and desktop configurations are available. **Contact I-Bus,** 9596 Chesapeake Drive, San Diego, CA 92127. **Tel. (800) 382-4229, Fax (619) 268-7863.**

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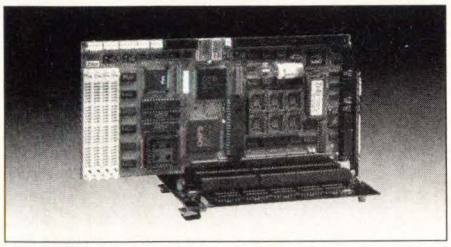

### I386SX — high performance package

Incorporating a 20 or 25MHz 80386SX CPU and using VLSI, surface mount and CMOS technologies, the I386SX is the most compact I-Bus single-board computer. Also, it operates on less than 6.5W of incoming power. The I386SX features 64K cache, a programmable Watchdog timer, advanced power-fail detect circuitry, 1.5MB of Flash EPROM/EPROM, an IDE hard disk interface, a floppy disk controller, plus two serial and one parallel port. **Contact I-Bus,** 9596 Chesapeake Drive, San Diego, CA 92127. **Tel. (800) 382-4229, Fax (619) 268-7863.**

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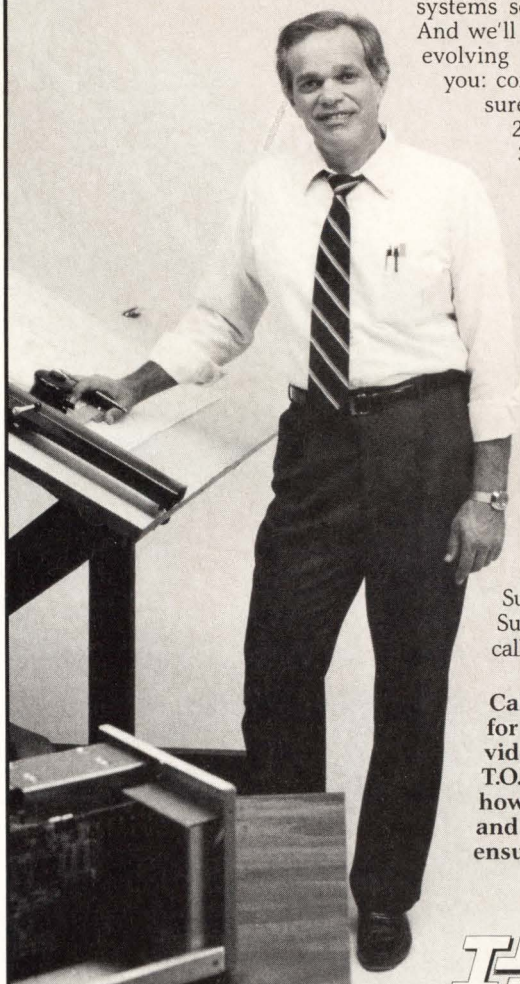

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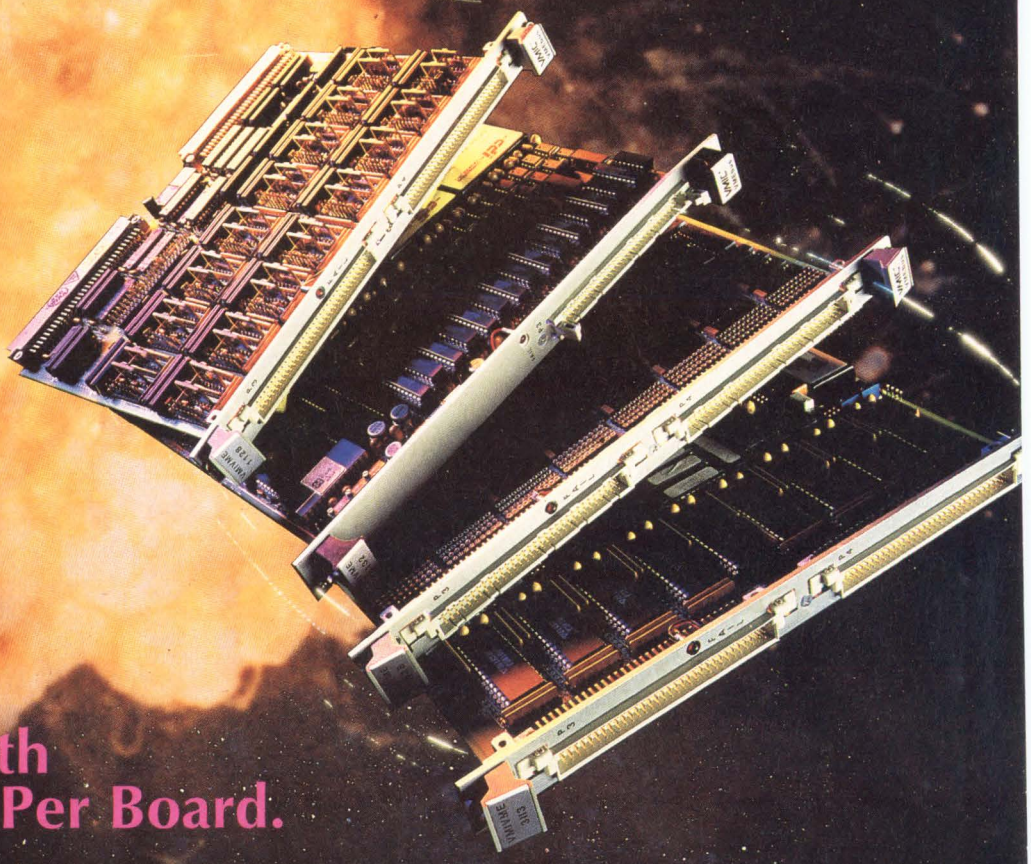

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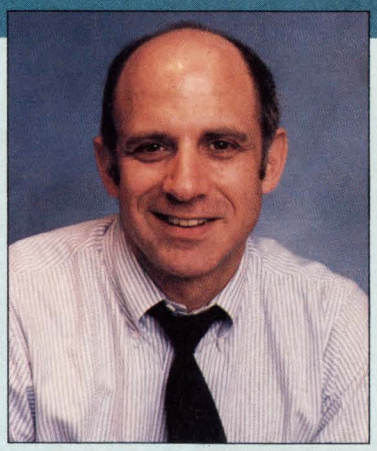

# Power transistors—where rubber meets the road

Much of the growth in mixed-signal technology will stem from putting mechanical devices—motors, relays and solenoids—under microprocessor control. Semiconductor manufacturers in this area are distinguished by the ability to handle large voltages and currents. This is invariably the job of power transistors.

In almost all servo-control loops, the output transducers draw currents large enough to require power transistor drivers. This is especially true for motors and solenoids, where the transducer uses some kind of magnetic field to produce mechanical motion. You typically produce a magnetic field, for example, by putting current through a wire coil. It sounds simple enough, but—as a reminder for those who've come to assume the microprocessor can do *anything*—it's not a job for digital CMOS transistor pairs.

## Carrying the load

The major problem is in the load that the transistor must carry. If you leave a "dead short" across the source and drain terminals of an MOS transistor (or across the emitter and collector of a bipolar transistor), it will latch in the "on" state, overheat and die. Many knowledgeable engineers will argue about whether a motor coil or audio speaker actually constitutes a "dead short," since the impedance of the wire coil will still be several ohms, and will actually depend on the intermittent frequency of the signal you put through. (Even a straight copper wire soldered across source and drain will have a resistance of 0.1 to 0.6 Ω, and may not constitute a "dead short.") But driving even an intermittent signal through a low-impedance load will require transistors with much more current drive capability than is typically available with CMOS LSI processes.

These load currents will be as small as 100 mA for motors in handheld consumer equipment such as cassette players and cameras, or as high as 200 or 300 amps in next-generation electric cars. The trend line, suggests Randy Frank, an engineer with strategic planning responsibilities for power products at Motorola Semiconductor (Phoenix, AZ), is to bring the microprocessor and control circuitry closer together with the power devices that handle the large voltages and currents. At one side of the current scale, it's possible and desirable to put control circuitry together with power transistors on the same chip—an integration popularly known as "smart power."

The larger the voltages and currents the power device must handle, however, the more limited the control circuitry will be. Consequently, at the opposite end of the current scale, where on-chip control circuitry is limited, there's still a tendency to make the power transistor "microprocessor friendly." This is accomplished, says Frank, by reducing the turn-on requirements for the power device and building in current sensors and other feedback mechanisms.

One example of a smart power product is a microprocessor Motorola produced for Canon Cameras as part of its "CSIC" (customer-specific integrated circuits) program. A variation of the popular 68HC05 controller family, this part has a full H-bridge motor drive on-chip. The transistors will handle up to 300 mA at 6 V, and are used to control automatic focus and film-advance motors on handheld cameras.

## Smart power for disk drives

Equally dramatic are the smart power products developed by SGS-Thomson Microelectronics (Agrate, Italy and Phoenix, AZ) for hard disk drive motor controls. The latest-generation 2.5-in. drives, the next-generation 1.8-in. drives and the over-the-horizon 1.3-in. drives will all depend on increasingly higher levels of semiconductor integration to decrease control board real estate, power consumption and cost. While disk drive electronics typically reflect two separate systems—one for reading and writing data, another for controlling motors and actuators (i.e., head positioning)—there's an increasing need to bring these two together on one chip.

This is because the track and bit densities of the data on the disk surface are increasingly dependent on specialized motor control techniques. With zoned-bit recording, for example, the bit density on the inner tracks of the disk can be increased by *slowing down* the rotational speed of the disk—ordinarily 3,600

rpm—while the inner tracks are written. Embedded servo technology, meanwhile, increases track densities but requires the read-channel electronics to detect servo pulses in the data stream and reposition the read-write head according to the amplitude of these pulses. With the current state-of-the-art, the separate read-channel and motor-control electronics are each highly-integrated chips, but the technology direction is to bring separate channels together as one chip in late 1993 or 1994.

Already, SGS-Thomson is delivering an SO-packaged device that controls both the actuator and spindle motor to the largest American and Japanese 2.5-in. drive makers. The device implements the servo control circuitry and power transistor motor drivers on one chip, using what the company calls its BCD process. This smart power process combines CMOS, bipolar NPN, lateral PNP, lateral DMOS, vertical DMOS, and high-voltage (up to 60 V) transistors.

National Semiconductor (Santa Clara, CA) produces a similar product, the HPC46100, a highly integrated servo engine with an on-chip 8-bit analog-to-digital converter (ADC). The HPC46100 boasts Integral Peripherals, pioneer of the 1.8-in. form factor, among the first customers for the part. Others developing integrated motor controllers are Allegro Microsystems and Cherry Semiconductor.

## Cost issues

Larger voltages and currents require larger transistors to avoid latch up or burn out. These transistors are often 10 times larger than typical digital CMOS devices. Smart power chips integrating both microcontrollers and power drivers are often much larger than either stand-alone controllers or discrete power transistors. While smart power experts such as Motorola, National Semiconductor, SGS-Thomson, and Texas Instruments have perfected manufacturing processes to minimize the number of masking steps—up to 15 for integrating high-density CMOS logic—the large die sizes will not be economical to fabricate without high manufacturing yields. Yields, in turn, cannot be perfected without high volumes.

Projected volumes for small form factor disk drives, used in laptop and notebook computers, are in the millions. As a consequence, SGS-Thomson can deliver its combination actuator and spindle motor controller for $7, says product manager Sandro Cerato in Italy. In fact, the volumes on an integrated solenoid driver developed by SGS-Thomson for Olivetti portable electronic typewriters (yes, typewriters) were so high that SGS could easily claim a world leadership position in the production of smart power components.

Where volumes are lower, or where cost is an issue, smart power components have difficulty competing with discretes and microcontrollers in separate packages. Siliconix (Santa Clara, CA), for one, markets power transistors and switches in SO packages for applications which need the space-conserving advantages of smart power but a lower entry cost. There are applications, however, in which even the most inexpensive power discretes cannot compete in cost with mechanical switches and relays. Al Kelsch, National's power IC product manager, says a $1-and-change transistor switch used to activate power door locks on high-end automobiles is several times more expensive than the flimsy mechanical leaf switches Detroit has used to do the same thing. Slowly, some of the automakers' most advanced products—such as the Cadillac Elante—are incorporating power devices on a single multiplexed bus running through the door hinge. These devices control motorized windows, power door locks and interior lighting in the car.

## Smart power: hot in the 1990s

Convincing automotive and household appliance manufacturers to replace electromechanical controls with electronics will be one of the hottest issues of the 1990s, says Art Fury, founder and president of Modupower (Santa Clara, CA). Fury, one of the most visible advocates of smart power during the 1980s, believes appliance manufacturers will be resistant and slow to embrace electronics, but will follow the leadership of commercial heating, lighting and air conditioning (HVAC) equipment manufacturers. Under pressure from consumers seeking to minimize electric power consumption in homes, appliances such as air conditioners and washing machines will show the same shift toward electronic control.

Full use of electronic control, though, will not be possible without a redesign of the entire servo system. To give an example, implementing an electronic washing machine will require that standard one-speed ac inductive motors be replaced with variable-reluctance motors. The chief advantage of the variable-reluctance motor is that it offers very high torque at low rotational speeds. Instead of putting an ac voltage across the motor coils, the variable-reluctance motor is powered by a train of dc pulses. The speed, direction and torque of the motor are all controlled by the frequency and duty cycle of these pulses.

The pulse stream must be driven by fast-switching (50 kHz-1 MHz) power transistors—essentially the same kind of devices that go into current-generation switching power supplies. In fact, Modupower's own product line—dc-to-dc converters using National's smart power devices to produce a variety of regulated computer system voltages—will eventually pair discrete power transistors with switch-mode regulators. The resulting DIPs will provide higher current capability than is typically available from one-chip devices, but at a lower cost than a fully-integrated smart power IC. "It looks simple," jests Fury, "but it ain't."

An additional benefit of replacing mechanical drivers with power transistors and ICs is that the latter provide instantaneous feedback and, in many cases, remote diagnostics. Even "midrange" power transistors—TO-220 devices rated for 60 V and 20 A—will provide current and temperature sensing that can be used to detect overload conditions. A dc motor jam, for example, will force both the current consumption and temperature of the power transistors to shoot up dramatically. On-chip circuitry—as few as 10 or 12 additional components, says Motorola's Randy

Frank—will provide these "smart discretes" with protection mechanisms such as voltage clamps and current limiting, as well as a means of signaling the microprocessor controller.

Some of the largest and most powerful transistors are used on the power buses running through the joints of construction steam shovels and the Lockheed C5A aircraft. The all-electric battery-powered car will use some of the largest power semiconductor devices. "The $di/dt$'s and $dv/dt$'s here," says Frank, "are 'big numbers.' " While the acceleration/deceleration curves for the electric car will be controlled by digital signal processors, the dc-to-dc boost converters and motor drivers must be capable of producing several hundred amps at voltages between 230 and 300 V. At a cruising speed of 40 MPH, the main motor of an electric car such as General Motors' Impact will consume a continuous 20 A—more than the central air conditioning of your house on a hot day in Phoenix.

A major problem with this technology is minimizing the size and weight of the semiconductor devices. The dominant means of increasing the voltage capacity of the semiconductor—its safe operating area—is to increase the oxide thicknesses and epitaxial layers between gate, source and drain (although this makes the device increasingly difficult to turn on). The dominant means of increasing current capacity and minimizing on-resistance is to put power MOS transistor cells in parallel. But at the voltages and currents required by electric cars, you get something that sounds more like a pan pizza than a computer chip.

Consequently, the IGBT—the insulated gate bipolar transistor—is making a comeback for this application, says Mike Jenkins of IXYS Corporation, which is also developing parts for electric cars. Though the IGBT is limited by lower switching frequency than MOSFETs, it is considerably cheaper because it produces a smaller die size.

The consequences of running too much current through an undersized transistor should be obvious. It's like revving a car engine too high. An eight-year-old boy once questioned me about driving in foreign countries. "If you drive a car too fast on the German autobahn," he sputtered with obvious glee at his thought, "the engine blows up—right?" Right.

*Stephan Ohr is a consultant with Indian Forest Research and editor of the monthly newsletter,* Mixed Signals.

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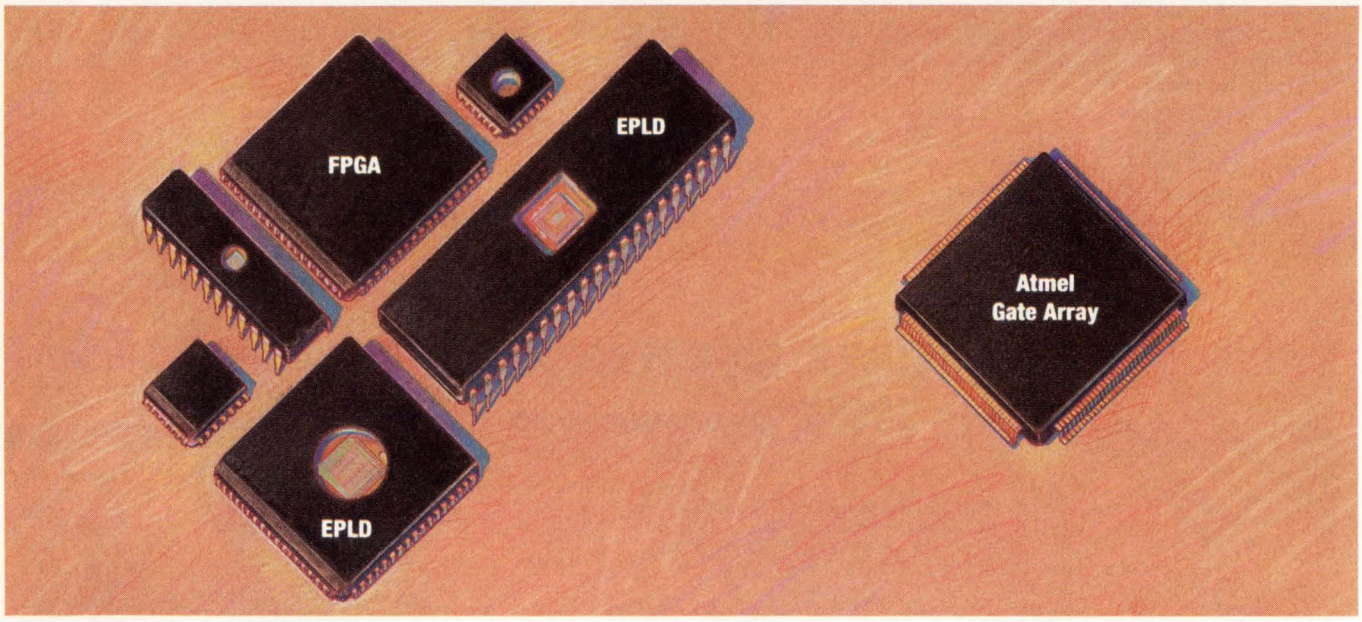


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CIRCLE NO. 83

# PC-based analog simulation

While most engineering areas are plentifully supported by companies producing personal computer software, analog simulation isn't. PC-based analog simulators are available, but only a handful of companies provide detailed support for this specialized and compute-intensive application.

Like many PC-based CAE tools, analog simulators come in various levels of integration and have specific focuses. Some packages such as EEsof's Libra and Touchstone, Etron's RF Notes, Microwave Spice, and Omnisys are designed specifically for RF designers and high-frequency applications. Meta-Software's HSpice is ideally suited for ASICs. Venable Industries Model 220 is aimed at switching power supply and servo designs while RLM Research's AFDPlus is dedicated to filter design and analysis.

General-purpose simulators also exist, the most common being from Interactive Solutions (Promise), Intusoft (ICAP), Meta-Software (HSpice), Microsim (PSpice), Viewlogic (AA Architect), and Visionics (EE Designer III).

Integration levels range from discrete simulators which require third-party schematic capture and netlist translator tools to fully integrated design capture, netlist, simulate, display, and document tools. You have the choice of an integrated environment where all intertask interfaces are taken care of, or a segmented environment where you must format the design database in different stages to pass along to the next stage. The integrated solutions from companies such as P-CAD, Viewlogic Systems, and Visionics are easier to install and use, since all the interface work has been done by the CAE vendor. Sometimes, however, desired features may be lacking and you may want to cherry pick and put together your own mix of tools.

## A matter of trust

A major issue for PC-, workstation-, and mainframe-based analog simulators alike is the question of trust in the results. While digital simulators have done a fairly good job of squashing out prototypes and breadboards, this just isn't the case with analog simulators. Even though a designer may simulate before building a breadboard, a prototype is usually still built before a production run is attempted.

Simulation runs are good for determining if gains are set properly, filters are adjusted correctly and transistors are biased in the proper operating regions. But, while analog simulators are good for theoretical circuit verification, a real-world circuit is often the only way satisfy you can be certain that what's on paper is what you will get functionally. This is especially true with high-frequency and RF designs. Here, few simulators are equipped to accurately predict real-world behavior.

Underlying the entire accuracy question are the models chosen and the level of detail in each model. While every analog simulator comes with a component library of standard parts, these are general-purpose models with parameters optimized for a predetermined trade-off in simulation speed and accuracy. A false sense of security can result when you pick a component from a supplied library and place it on your schematic, thinking that including it is analogous to soldering it to a breadboard.

There's no perfect Spice model, and it's often necessary for you to become intimately involved with the model being used and the parameters set for that model. Many software vendors try to lead designers to the false conclusion that it's acceptable to just plug a model into a design and simulate away. But, the choice of model, and even the choice of subcircuit element models, drastically affects the run-time and accuracy of the simulation result.

Becoming intimately familiar with a model and its structure isn't all that bad and can be useful in helping optimize a design. When a simulation run detects that a part isn't responding in the desired way, you can simply modify the model parameter of the part until the simulation runs as desired, then choose a part which matches the model's parameters.

While many packages let you simulate the digital portions of a design in one pass and the analog portions in another pass, true mixed-mode simulators which can perform both simulations and time-align the results on a single output plot or waveform trace graph are a rare breed.

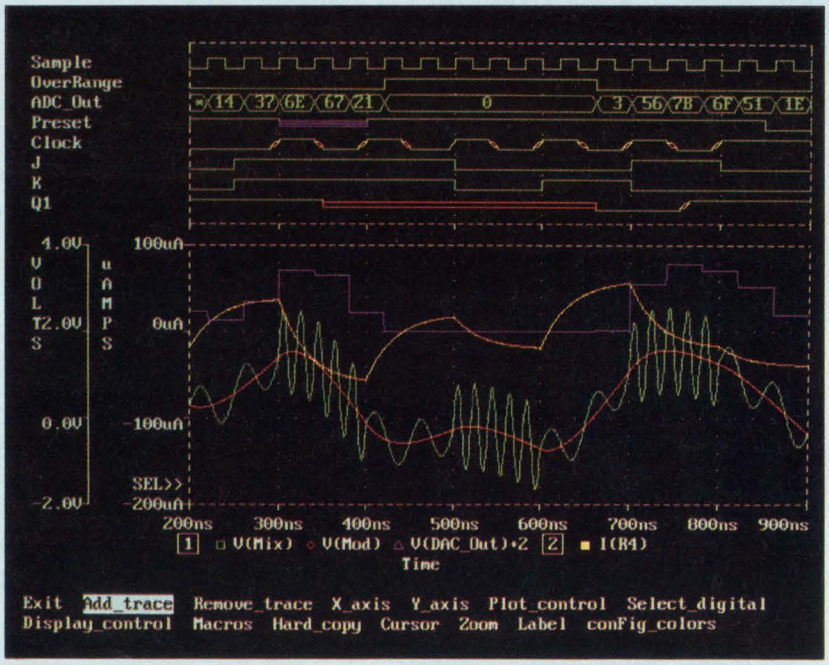
It's only recently that PC-based analog simulation systems have addressed mixed-mode simulation. Mixed analog and digital designs often require two separate but intertwined simulators which run like square dance partners, each swinging the other until a common timeslice has occurred where results can be tabulated.

In many cases, you can debug a design using the digital and analog simulators separately. As designs get more critical, however, a mixed-mode simulator becomes more desirable, especially when it comes to the often delicate interfaces between analog and digital circuitry.

While purely analog circuits are generally only susceptible to crosstalk, mixed analog and digital designs are prone to hits from clocks and digital transitions from low to high and high to low. Sharp edges found in digital systems induce noise across the spectrum which can be picked up and can affect sensitive analog circuits.

## A few players

PC-based analog simulators are proving themselves and are gaining more acceptance, especially as capabilities and resolution increase and prices stay low enough to tempt many to try them. P-CAD, Viewlogic Systems and Visionics provide bundled CAE tools that include an analog simulator. (P-CAD bundles Microsim's PSpice with its tools and takes care of all the netlist formatting and interfacing.) These simulators are general-purpose dc-transient-response and ac-analysis simulators which can be used with any design, providing the designer knows the model characteristics.




*PSpice features mixed-mode simulation where analog and digital waveforms are displayed, aligned in time.*

Third-party companies providing discrete analog simulators have products ranging from the general purpose to the highly specific. They may include schematic capture or link to other schematic capture tools through netlist translators (or both). Some of these companies include EEsof, Etron, Interactive Solutions, Intusoft, Meta-Software, Microsim, Tesoft, and others.

The most widely used product to date is MicroSim's PSpice program, which accepts Spice netlists and generates waveforms from selected nodes based on user-defined input stimuli. PSpice is useful for determining proper responses to filter design, amplifier stability, noise and impulse response and immunity, and much more. Monte Carlo analysis lets a designer vary parameters on a random basis, showing yield deviations from tolerance differences between components. The Probe program in PSpice lets you probe on selected nets and display stimulus waveforms next to resultant waveforms at different points in the analog signal path.

Although initially available only for PC-based platforms, PSpice is now offered for Apple's Macintosh machines, Digital Equipment Corp.'s VAX systems and Sun's Sparc systems. Prices range from $2,500 to $8,200 for PC-based systems and up to $29,000 for DEC- and Sun-based systems. You can see that software for PC platforms is one-third the price of that for higher-end machines.

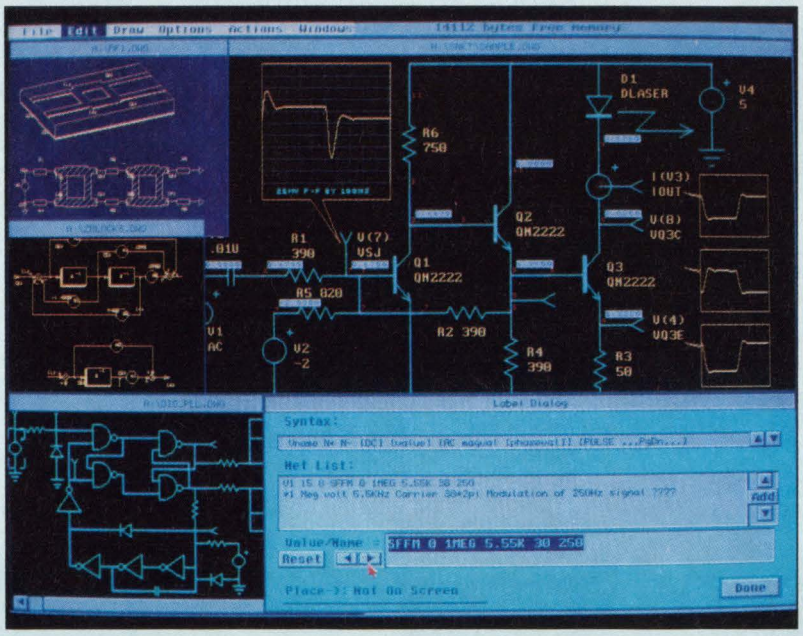
## PSpice now tackles mixed-mode

PSpice has recently been introduced with support for mixed-mode simulation. The new Design Center software uses just one graphical interface with pull-down menus and provides a fully integrated schematic capture program for analog, digital and mixed simulation. Waveforms can be displayed simultaneously along a common time axis, and over 5,700 device models (4,000 analog and 1,700 digital) exist in the company's library of components supplied with the program.

A nice feature of Design Center is that you can probe on the schematic window instead of having to feed net names into the simulator. This eliminates the time-consuming iterative loop of exiting one program and entering another to edit the design and then resimulate. Other advanced features include analog behavioral model support, sensitive and worst-case simulation capabilities, statistical analysis, and device characterization.

Another improved Spice derivative is ICAP software from Intusoft, available for 286, 386, 486, and

Macintosh machines and featuring behavioral modeling, mixed-mode capabilities, Monte Carlo analysis, and sensitivity analysis. Intusoft has demonstrated that the key to effective analog simulation revolves around the models of the simulation components. You can choose higher-efficiency models for more accuracy, and lower-efficiency ones to reduce simulation time when certain parameters are not important.




*ntusoft's embedded schematic tools permit simultaneous display of schematics and waveforms at selected nodes of the circuit.*

ICAP also integrates a schematic capture program with its simulator. While it and most other analog simulators can accept netlists generated by third-party tools, integration of the schematic capture tool streamlines the back and forth iterations of design and verification. It also simplifies stimulus and response queries, since you can place iconic probes and signal generators directly into the schematic.

Intusoft boasts that ICAP's open nature makes it capable of accepting any netlists from other schematic capture programs or even from other analog simulators that conform to Berkeley Spice 2G.6 format. In addition, you can display, manipulate and plot on the PC using the company's IntuScope program, results from other simulators making ICAP an ideal low-cost simulation analysis tool, even when workstation-based simulators exist in-house.

ICAP is the fastest PC-based Spice simulator and also among the most memory-efficient—and, in fact, is comparable to workstation-based simulators, claims Intusoft. By taking advantage of protected mode programming and extended memory, the company says there's no real limit to the size of the circuit that can be simulated—about 1,000 components can be handled per megabyte of expanded memory. The reasonably priced ICAP software costs $890 to $1,181 and is sure to make headway, especially since most other analog simulation software costs so much more.

Focusing on key issues such as high-accuracy models and the ability to calculate nodal capacitances, the HSpice program from Meta-Software is an advanced analog simulator which has proven itself in the ASIC world—so far to the 0.7 micron level. HSpice features a unique ability to handle process scaling and shrinking—for example, FETs and diodes whose parasitics are affected by process shrinks can be recalculated, as can undersized and oversized poly interconnects.

In addition, HSpice can process subcircuit multiplication quickly and efficiently. This is useful for repetitive circuit elements such as ROM, SRAM and DRAM, where identical cells have the same characteristics except for interconnect characteristics, which HSpice handles separately. Full-chip 1.4-million transistor SRAMs and various DRAMs are among the test cases HSpice has successfully handled.

HSpice has been greatly enhanced over plain Spice to include code that implements special techniques handling nonconvergence problems that can plague many Spice simulators. Where there's nonconvergence, HSpice applies proprietary techniques to resolve the problem. If nonconvergence still persists, HSpice provides you with useful diagnostics that list problem nodes, elements and pertinent troubleshooting information.

Including steady-state, transient and frequency-domain support, HSpice has been successfully used to analyze high-speed circuits with time intervals below 1 ps and frequencies above 100 GHz.

HSpice is available on most platforms, from the 386 PC to Cray, with Amdahl, Apollo, Convex, Digital, HP, IBM, Intergraph, Silicon Graphics, Solbourne, and Sun support—to name a few. HSpice also boasts interfaces to various design environments, including Cadence, HP, Mentor, Valid, Viewlogic, Seiko, and Zuken.

*Jon Gabay is a freelance editor with extensive design experience. He has written for all of the specialized CAE/CAD publications at one time or another, including* High Performance Systems, Engineering Workstations *and, most recently,* Design Automation.

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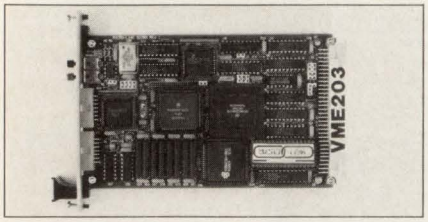


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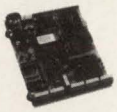

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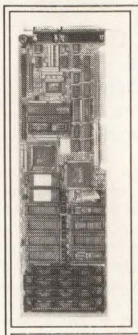

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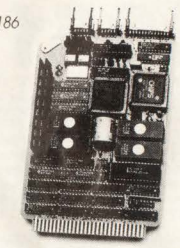

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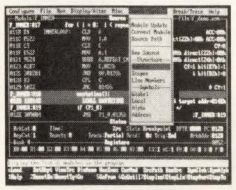

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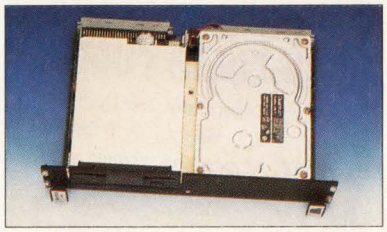

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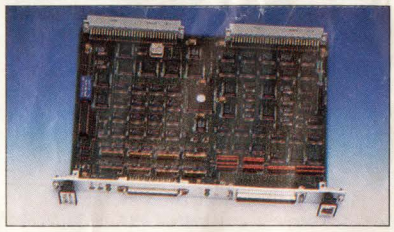

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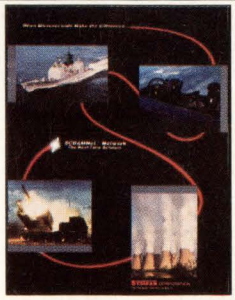

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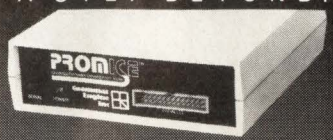


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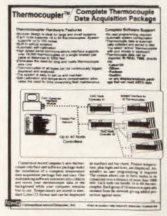


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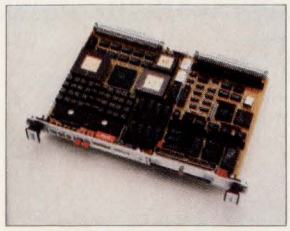

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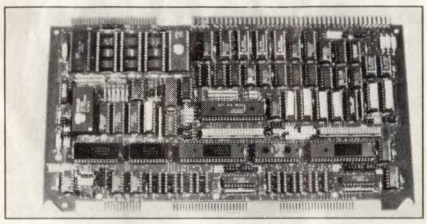

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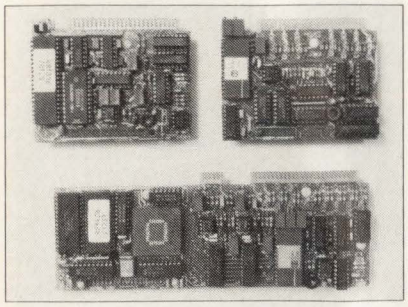

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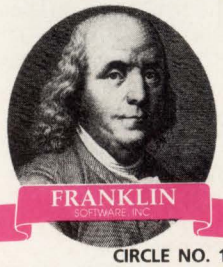


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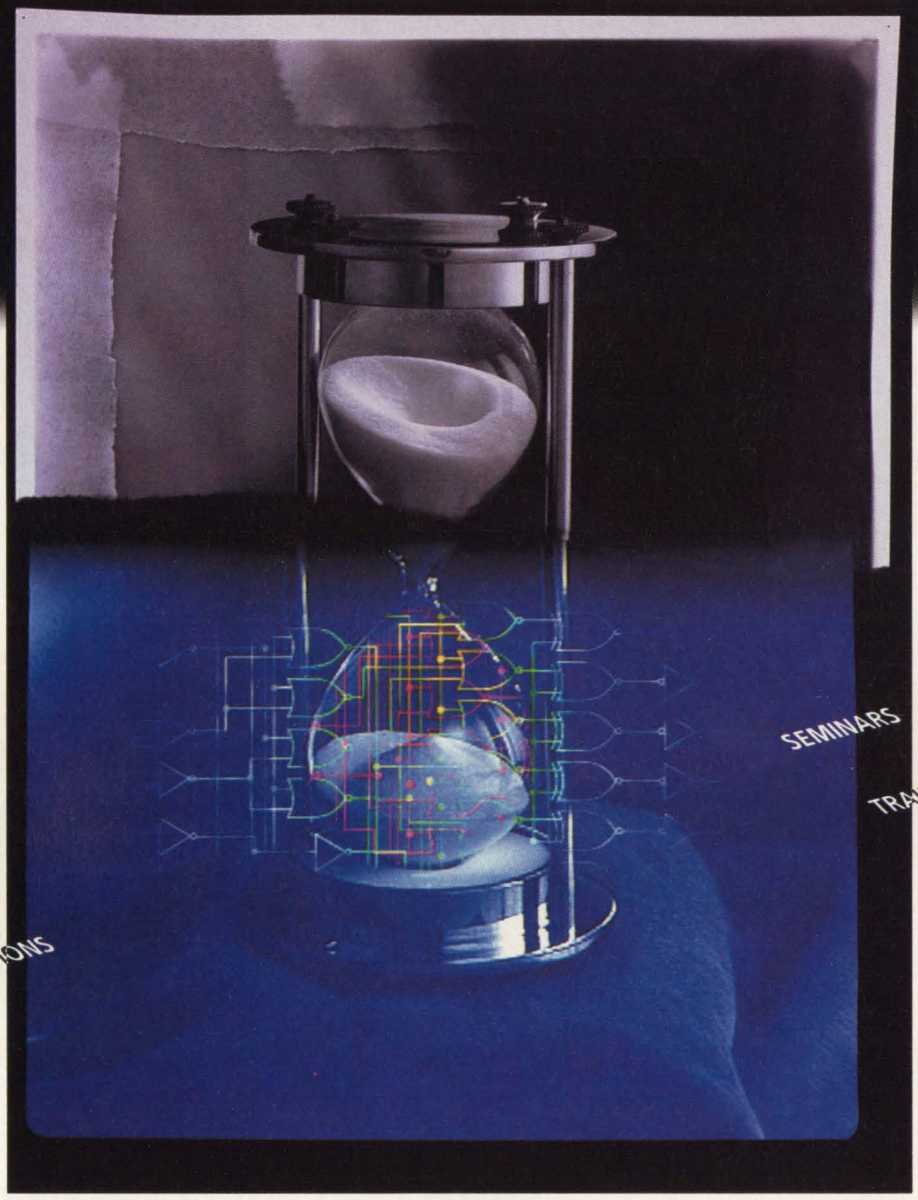

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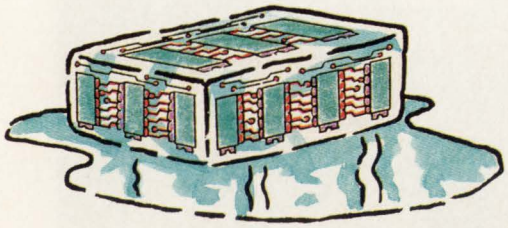

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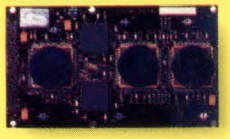

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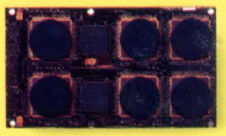

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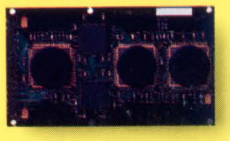

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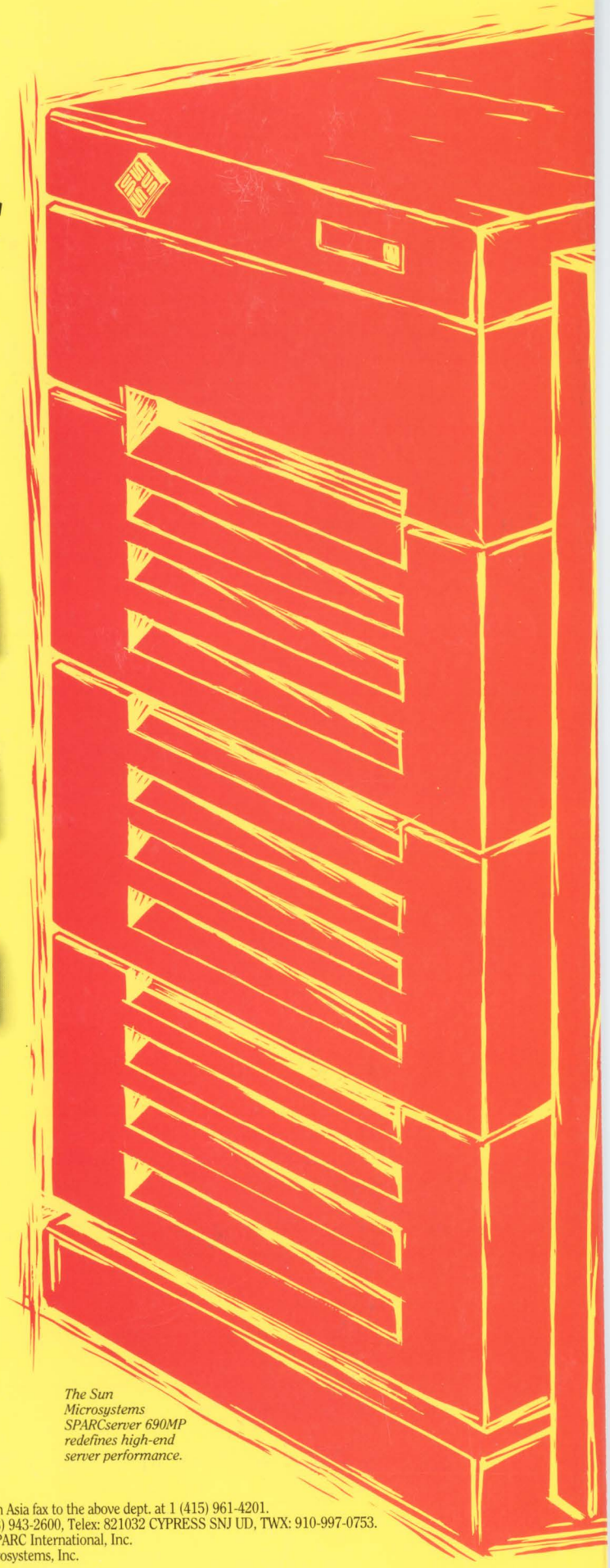

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