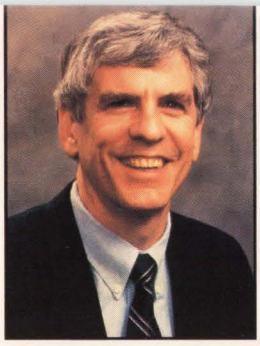


John East on:
Technology
Transparent Design

A PENNWELL PUBLICATION DECEMBER 1991

COMPUTER DESIGN

Technology and Design Directions

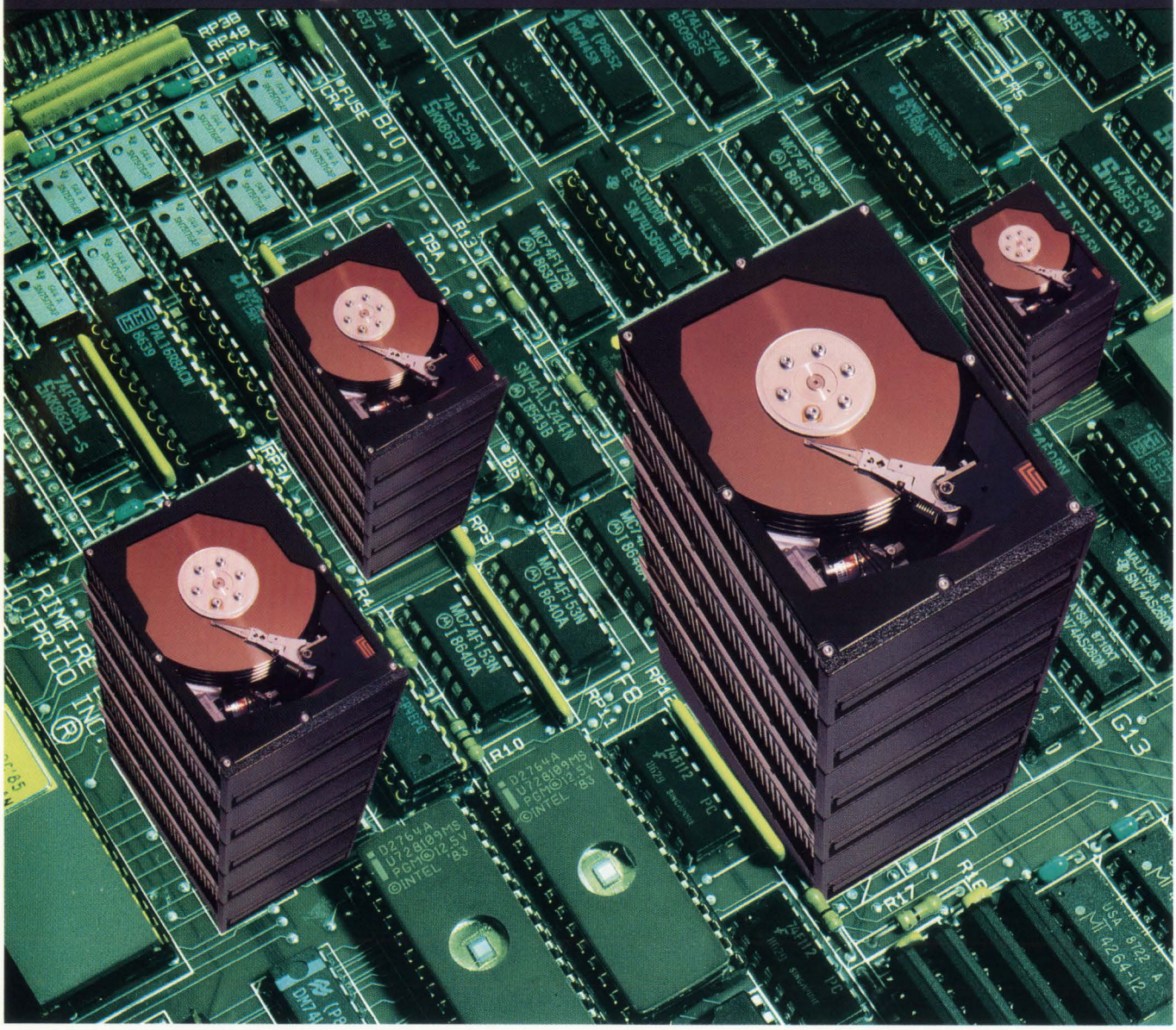
FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

Designers search for the secret to ease ASIC migration

Cellular phone designs call for mixed-signal solutions

Add-on boards boost real-time performance

Unparalleled, parallel performance.



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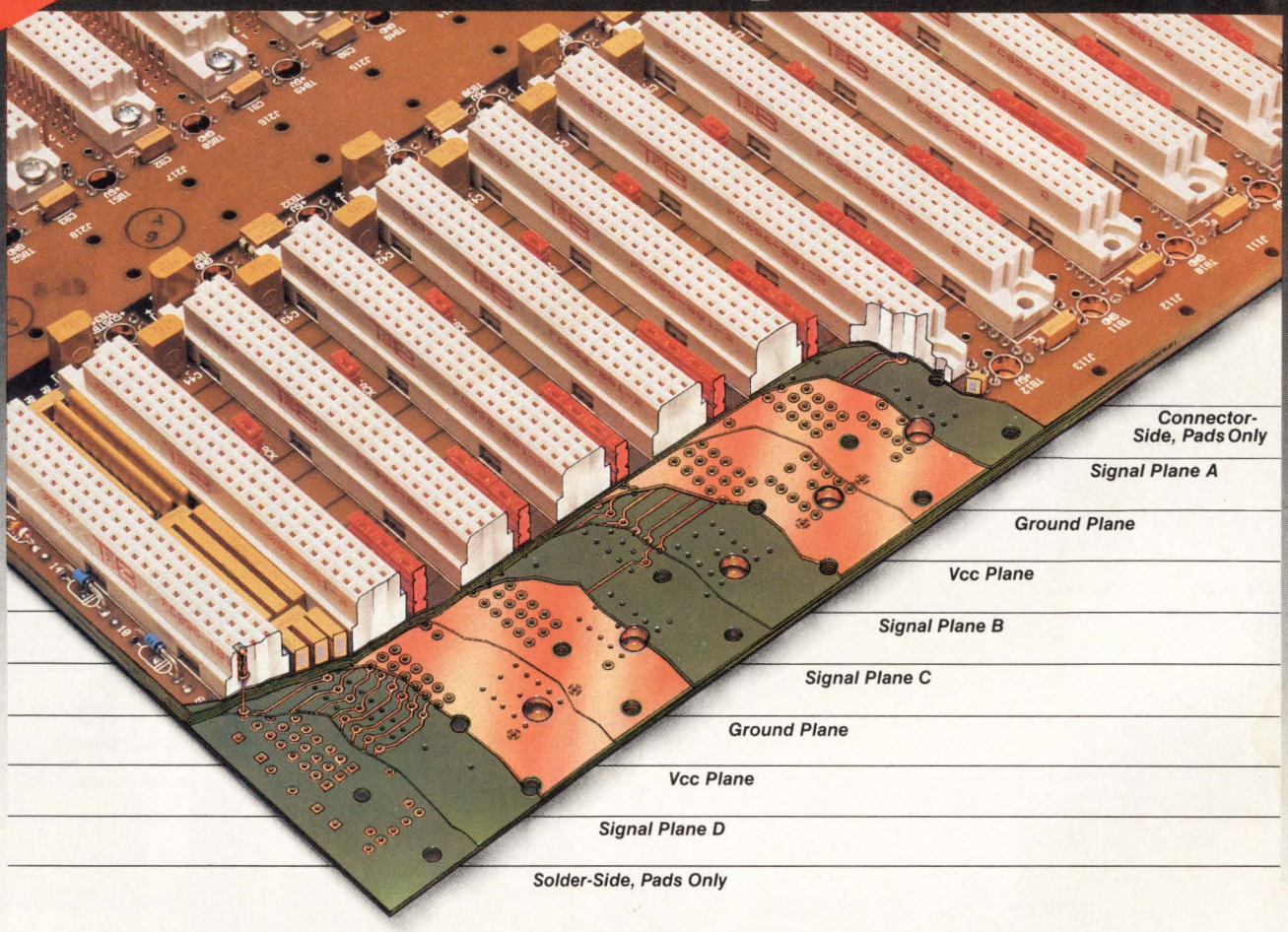
CIRCLE NO. 1

New

10-Layer VME Backplane!



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Start with the signal layers—four of them—with the most "noise sensitive" lines isolated from the others. The spacing and placement of the layers in this stripline (with embedded microstrip) design was calculated to enhance the backplanes' high frequency bypass characteristics.

It's the quietest backplane ever! Sharply reduced crosstalk is achieved by the increased separation of signal lines—both within and between the layers. Superior decoupling comes from the placement of both ceramic and tantalum capacitors between each slot.

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CIRCLE NO. 2

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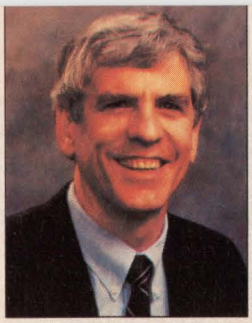
CIRCLE NO. 3

VOL. 30, NO. 15 DECEMBER 1991

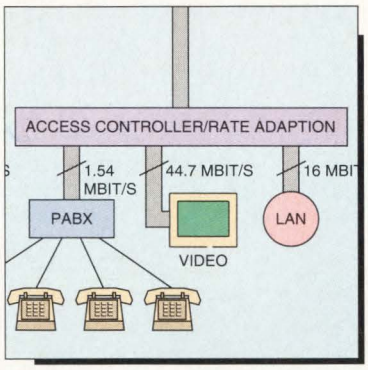
COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



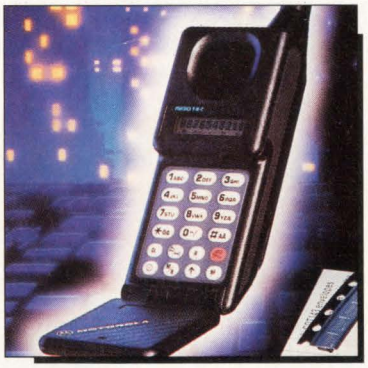
John East on: Technology transparent design
Page 25



Page 28

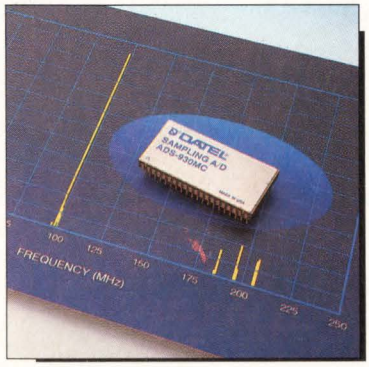
TECHNOLOGY DIRECTIONS

*Special **SysComp '92 West** Show Preview (see inside back cover)*



Page 57

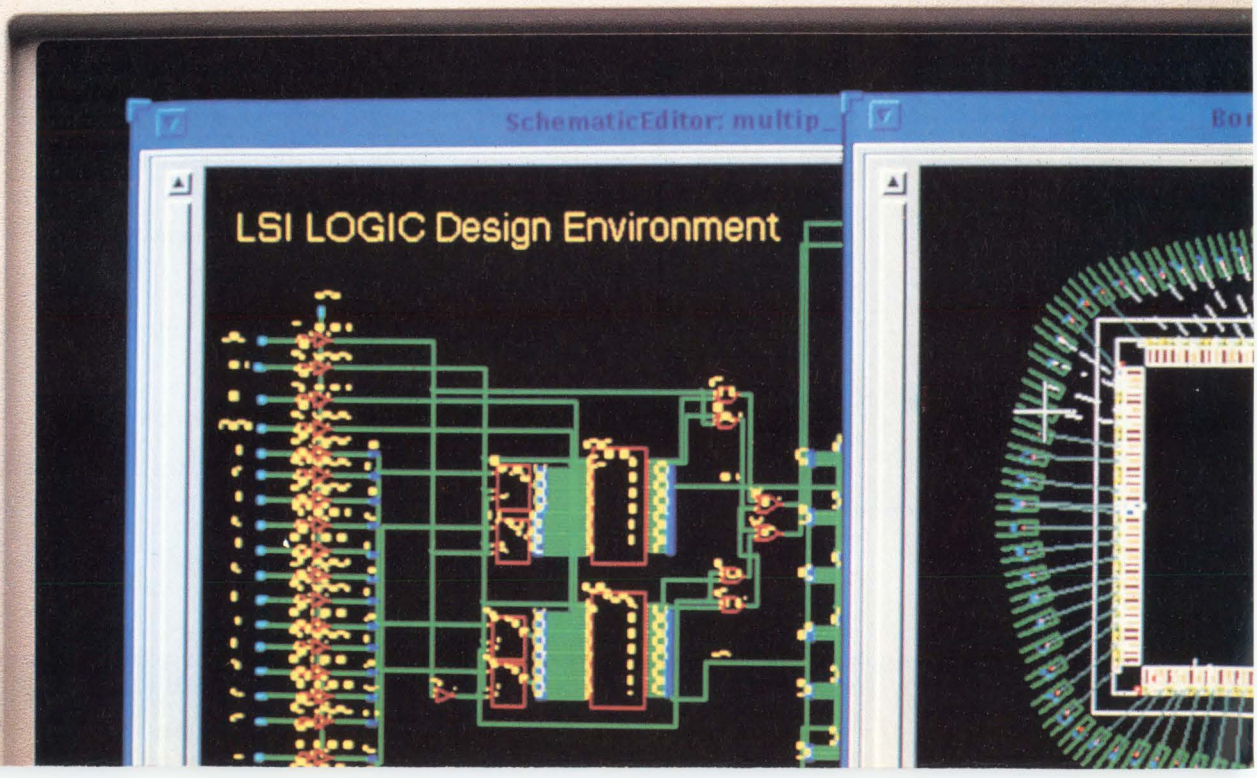
TECHNOLOGY AND DESIGN FEATURES



Page 107

NEW PRODUCT HIGHLIGHTS

OUR RELATIONSHIP



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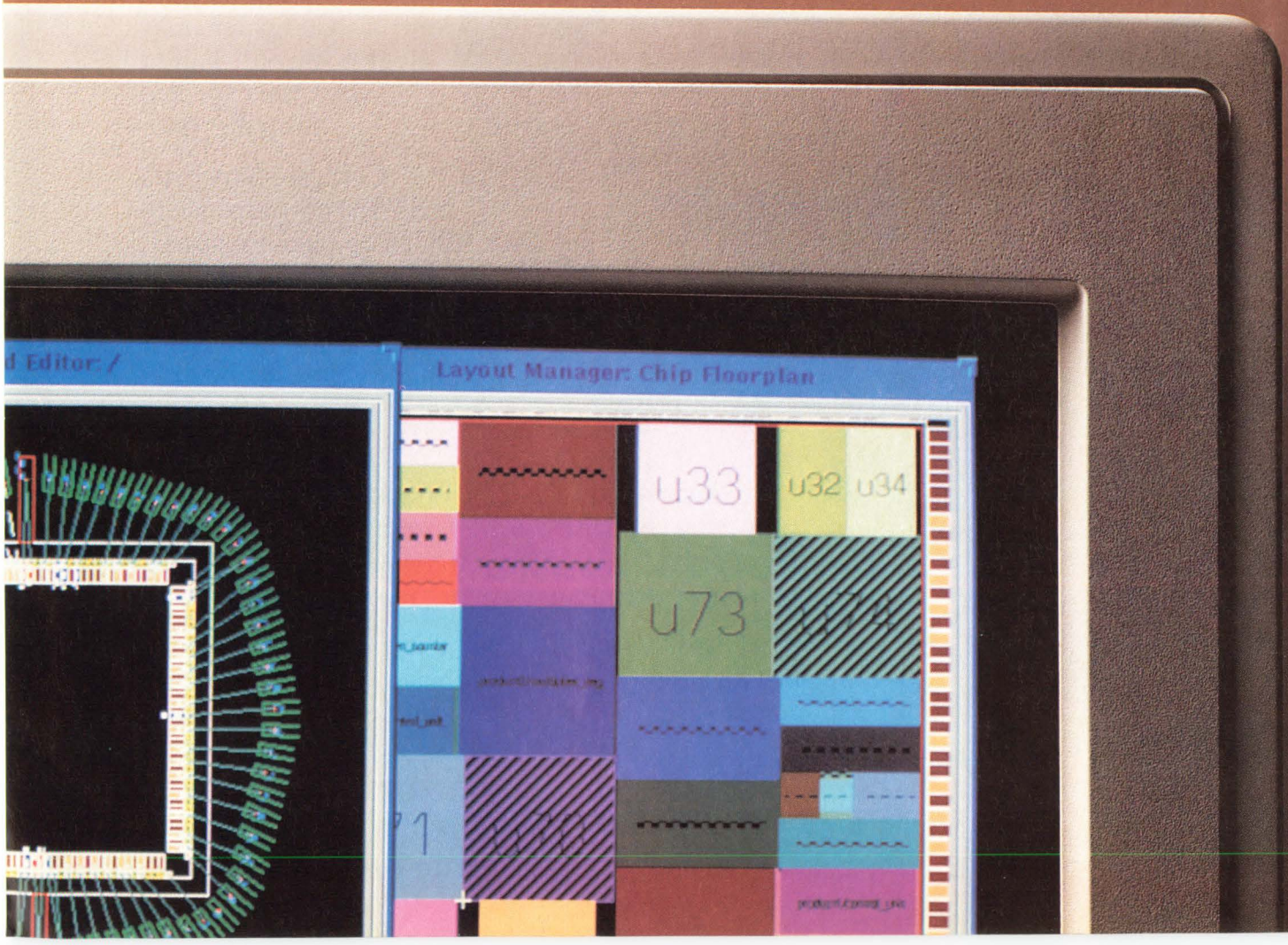
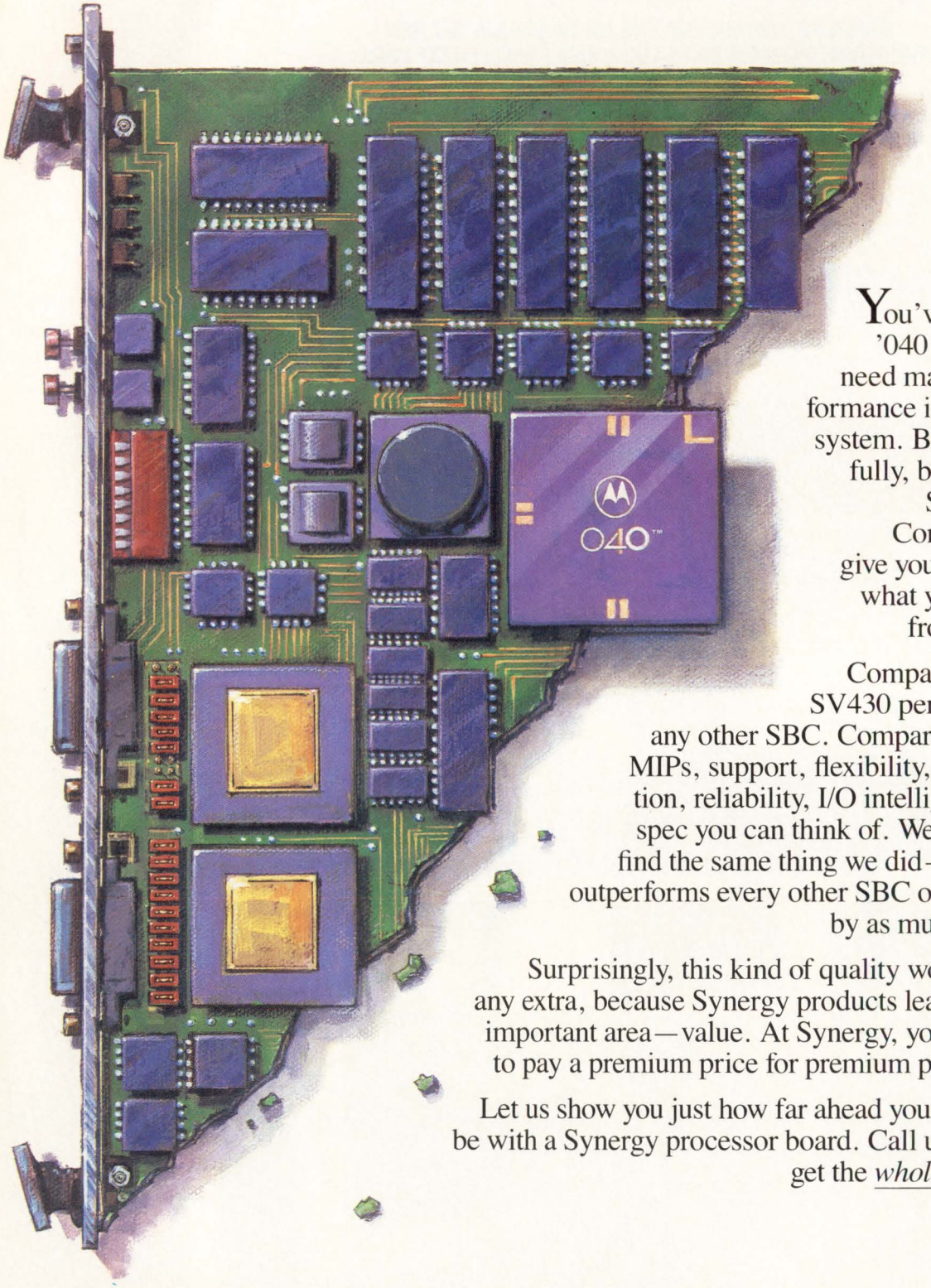
ACROSS THE BOARD

CIRCLE NO.4



Why Settle for ½



You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may give you only half of what you expected from the '040.

Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

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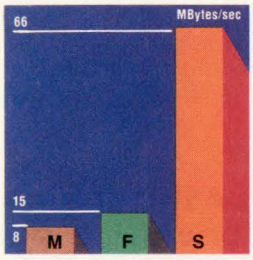
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

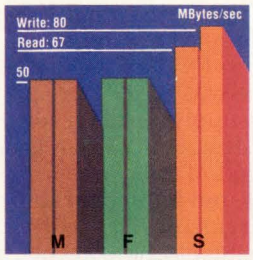
an '040 Board?

Compare our specs. Synergy is superior across the board!



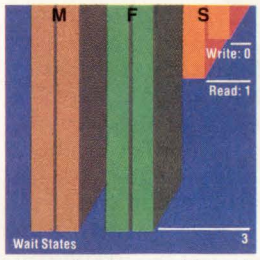
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



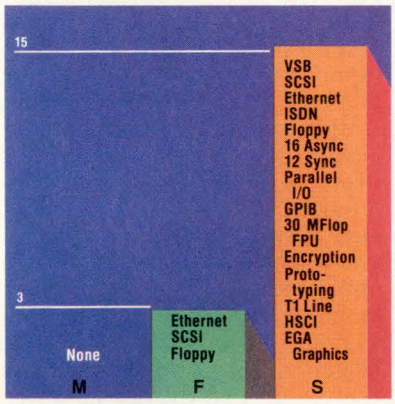
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.

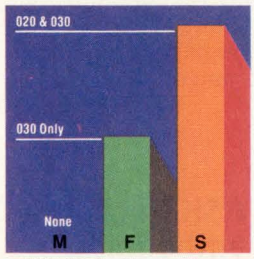


I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.

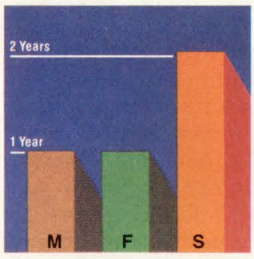
Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.



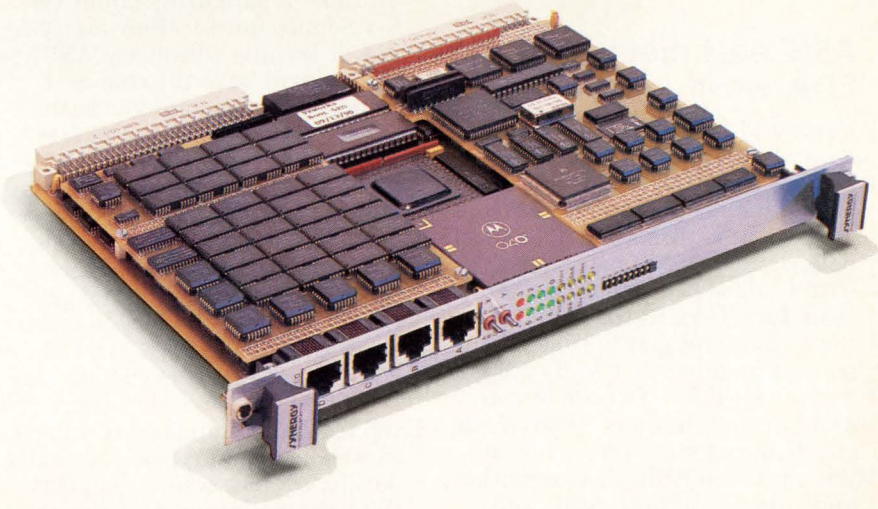
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



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FAX: 619-753-0903

SYNERGY microsystems

CIRCLE NO. 5

Air Force gets tough on top-down design

Defense contractors who have been waffling on whether to commit to VHDL top-down design methodologies have gotten a nudge from the Department of Defense. A new Air Force procurement policy goes way beyond current regulations (which call only for VHDL documentation of designs) by basing contract awards on the use of VHDL throughout the design cycle. While the policy stops short of limiting awards to contractors that fully embrace VHDL, it's clear that those who use such tools have a better shot of landing a lucrative government contract than those who don't.

Currently, many contractors use traditional design tools to complete a project and submit documentation written in VHDL after the fact. The Department of Defense is seeking tighter controls on design quality by demanding that projects follow a top-down design paradigm with measurable results at three milestones—concept, prototype and production. It's expected that the Army and Navy will soon follow suit, a move which will light a fire under traditionally complacent defense contractors.

—Mike Donlin

ASIC east meets EDA west

Fujitsu Microelectronics (Tokyo, Japan), in an effort to provide designers with a more advanced level of tool support, has formed a long-term, multimillion dollar technology partnership agreement with Cadence Design Systems (San Jose, CA). In the deal, the companies will jointly develop and market an advanced ASIC design system for Fujitsu's commercial and internal markets. Fujitsu's desire to direct more resources on the advanced ASIC design market, and support for both ASIC and board-level designers, was the main reason for the deal.

Scheduled for release in 1992, the first jointly developed products will include a front-to-back end, advanced ASIC design system for sub-micron high-performance ASICs of 20,000 to over 200,000 gates. Distribution and support of ASIC libraries are also spelled out in the deal. Initial joint efforts will focus on key ASIC design methodologies such as timing-driven design, clock-skew management, hierarchical design, and incremental design. For its part, Cadence will enhance several of its tools including those for simulations, timing analysis, synthesis, composition, and place-and-route.

According to Fujitsu, the deal with Cadence was a recognition that merely supplying the traditional ASIC design kits is not good enough in light of today's shorter design cycles and higher performance requirements. Joseph B. Costello, president and CEO of Cadence, described the partnership as an example of the sort of relationships ASIC vendors must forge with EDA vendors if they wish to provide designers with advanced design environments.

—Jeffrey Child

Teaming ASIC technologies and embedding function blocks

With the recently announced TC165G/E gate arrays from Vertex Semiconductor (San Jose, CA), now a Toshiba subsidiary, ASIC designers will have the chance to evaluate the combination of the Vertex expertise in system-level ASIC design with Toshiba's proven 0.8-μm CMOS process (gate delay less than 260 ps). Like LSI Logic and Motorola, Vertex is offering users the option of embedding fully diffused SRAM on the gate arrays—up to 256 kbits on masterslices that range from 33,000 to 361,000 gates. Users can also embed ROM, multipliers, adders, subtracters, ALUs, and barrel shifters, as well as other macros. Internally developed masterslice compiler software can generate a masterslice with embedded functions, "in a matter of minutes," according to Vertex.

An ardent proponent of an up-front design-for-test methodology, Vertex automatically inserts testability into embedded functions, as well as the rest of the gate array design, with the Vertex-developed test logic synthesis and scan insertion tools. Vertex guarantees users greater than 99 percent stuck-at fault coverage with no test vector development and no performance penalty in the datapath. And with its proprietary physical synthesis tool, Vertex claims that it optimizes the logic of the entire chip at one time to ensure that the entire design is optimized for the highest level of performance.

—Barbara Tuck Egan

Compass ASIC tools primed for VHDL design

During the nine months since being launched as a wholly owned subsidiary by VLSI Technology (San Jose, CA) to sell open tools and libraries to ASIC and ASSP (application-specific standard products) designers, Compass Design Automation (San Jose, CA) has been improving the ASIC tools pioneered by VLSI. With that toolset, dubbed the ASIC Navigator Design System and released about two weeks ago, users can now mix and match design-entry methods, including graphical high-level design entry from which VHDL can be generated. Compass' goal has been to tighten the design flow and to generally enhance the tools, which are no longer silicon-specific, for top-down design.

Compass president, Dieter Mezger, says, "The Navigator series demonstrates our ability to leverage a 10-year heritage of providing cutting edge technology to address the increasing demands to place systems on silicon. The capabilities that we are announcing today define the direction that EDA vendors will have to follow to provide the tools necessary to handle the level of complexity demanded by the market."

Among the Compass capabilities to which Mezger was referring is the production of a behavioral VHDL description of the entire specification and the ability to par-

Continued on page 10

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And that's just the beginning. FORCE will spark embedded systems for generations to come, based on our partnership with Sun. In fact, we're already designing the SPARC CPU-2E. Of course, our entire family of SPARC-based products is 100% SunOS-compatible.

So nothing stands between you and the most powerful development environment in embedded systems. With SunOS and the SPARC CPU-1E, you can program, debug and observe real-time code. All within the same development and target system, thereby slashing costs and development time.

The SPARC CPU-1E accommodates up to 80 Mbytes of DRAM. You can run real-time, UNIX,® Sun Windows™ and utility programs. Standard DMA-driven SCSI and Ethernet interfaces give you full network access. There's even an SBus™ interface for I/O expansion.

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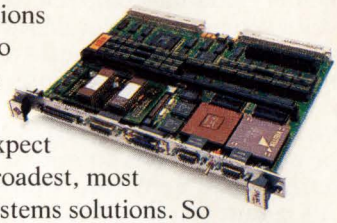

But that's what you'd expect from the vendor with the broadest, most flexible line of embedded systems solutions. So call 1-800-BEST-VME, ext. 10 for more information or fax a request to (408) 374-1146.

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OUR NEW PARTNERSHIP IS AS HOT AS IT GETS.

CIRCLE NO. 6

Continued from page 8

tition and synthesize directly from that same specification. Compass' ASIC Synthesizer accommodates specialized structures such as memory and datapath elements as well as general logic, and its test synthesis tools incorporate a BIST methodology as well as internal scan and boundary scan. Compass doesn't have its own VHDL simulator and thus relies on a joint marketing agreement with Vantage in this country and an OEM relationship with Vantage in Europe.

—Barbara Tuck Egan

New C for DSP

A new software toolkit from Motorola's Digital Signal Processor Operation (Austin, TX) should help boost the performance of code running on that company's 24-bit 56001 DSP chip. The GNU-based 56001 C compiler with a source-level debugger costs a mere $709. Users of the 96002 "Media Engine" and 16-bit 56100 chips will have to wait a little longer for Moto to produce a version to run on their processors. Meanwhile, NEC Electronics (Mountain View, CA) has turned to Intermetrics (Cambridge, MA) to provide its C-compiler and XDB debugger for NEC's uPD77240 DSP processors.

—Dave Wilson

Disparity between desktop and real-time CPU power?

The demand for more raw CPU power seems to be increasing in the embedded market, but languishing in the arena of desktop systems. The reason: the ability of software to take advantage of the power offered by today's microprocessors. Compaq (Houston, TX) and IBM (Armonk, NY) have recently introduced high-performance systems selling for premium prices and those systems have gone begging because software applications do not exist which let users derive the benefits of the higher-performance hardware. The situation may get even more extreme with the introduction of new Advanced Computing Environment (ACE) machines and the expected fruits of the Apple/ IBM alliance.

Conversely, embedded systems appear to be about to make a significant shift from the mostly 4- and 8-bit systems of today to more and more 16- and 32-bit systems. The shift here is spurred by the demands of possible applications. That, in turn, according to a study by International Data Corporation, will lead to a doubling of the real-time embedded software market over the next three years, from $3.4 to $6.7 billion, with an increasing number of developers seeking off-the-shelf solutions to improve their time-to-market. In the embedded arena, the development is pushed by a demand for more functionality and will doubtless spur more RISC-based designs. In the desktop arena, users will have to be convinced by the availability of applications that fulfill their needs that they should buy the higher-powered machines.

—Tom Williams

Happy New Year, Vic...

Although it's been available for years, the VIC VME interface chip still isn't working properly under all circumstances—at least according to one VME vendor intimate with the device. Apparently, when a slave access and a write-posted access occur on the VMEbus at the same time, the VIC chip can't handle the pressure and comes to a screeching halt. The chip's owner, Cypress Semiconductor (San Jose, CA), is committed to developing a better VIC sometime next year. For its part, VME vendor and VME64 developer Performance Technology (East Rochester, NY), is rumored to be brewing some fresh SBus interface silicon together with LSI Logic (Milpitas, CA) to support Performance's line of SBus cards.

—Dave Wilson

TI pitches standard to IEEE

Texas Instruments (Dallas, TX) is proposing a serial vector format (SVF) standard to the IEEE 1149.1 Working Group that will let boundary scan test information pass between design and test tools and equipment. The standard, developed by TI, Teradyne (Boston, MA) and other test equipment suppliers, will let engineers incorporate boundary scan testability throughout a product's design cycle by providing portable test vectors for chips, subsystems and systems.

The IEEE 1149.1 standard, adopted in 1990, describes a four-wire serial test interface and boundary scan architecture useful throughout a system's life cycle—from design through assembly to test—and at any level of integration. Without any standard for transferring information from parallel-oriented tools, such as simulators, to the serial format required by 1149.1 has led to proprietary SVF solutions.

—Mike Donlin

X marks the spot

Lots of excitement is building around X Windows—especially at developers of real-time operating systems. Microware Systems (Des Moines, IA), for example, has announced an X Server package for its OS-9/68000 real-time operating system. Known as the X Windows support pak, the package will let system integrators build stand-alone, real-time systems that utilize the X Window system for the user interface. Meanwhile, the news from Hewlett Packard (Waterloo, Ontario, Canada) is that Wind River Systems (Alameda, CA) has been selected to provide real-time performance to HP's i960-based X stations. Apparently, HP needs the operating system to add local client functionality to the terminals, offloading host systems. In a separate announcement, Wind River Systems has also disclosed that it has two new tools—windX and VxGDB —which will let real-time developers create GUIs and debug VxWorks applications.

—Dave Wilson

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CIRCLE NO. 7

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  - Interrupter and handler
  - 16 vectored interrupts
  - DTB Master/Slave
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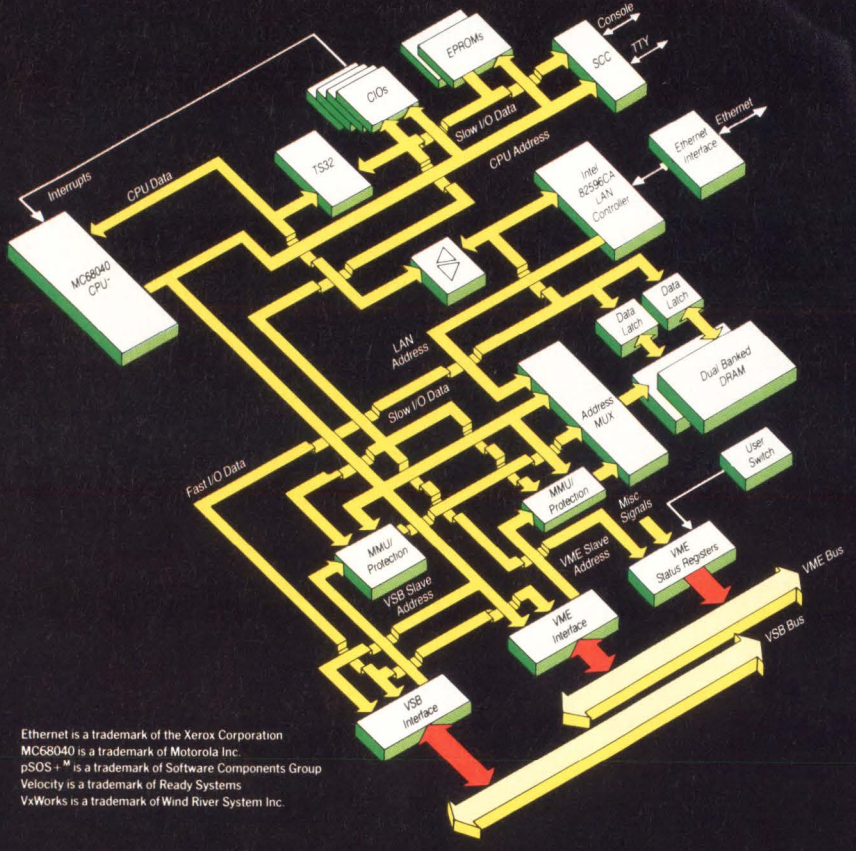
- VSB Master/Slave
  - Interrupter and handler
  - 16 vectored interrupts
- Ethernet IEEE802.3 with 32bit DMA Controller
- 128Kb to 2Mb EPROM in 2 JEDEC sockets
- 2 x RS232 • 4 x CIO • 12 x Counter/Timers
- Software support includes:
  - pSOS+™ • Velocity • VxWorks
  - TP-IX/68K V.3.2 implementation of UNIX



Ethernet is a trademark of the Xerox Corporation
MC68040 is a trademark of Motorola Inc.
pSOS+™ is a trademark of Software Components Group
Velocity is a trademark of Ready Systems
VxWorks is a trademark of Wind River System Inc.

If you would like information on these, or any other Tadpole products, call us TOLL FREE on:

1 800 232 6656 for US enquiries

For European enquiries contact:

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Cambridge Science Park
Milton Road
Cambridge CB4 4WQ
ENGLAND

Tel: 0223 423030
Fax: 0223 420772

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77210
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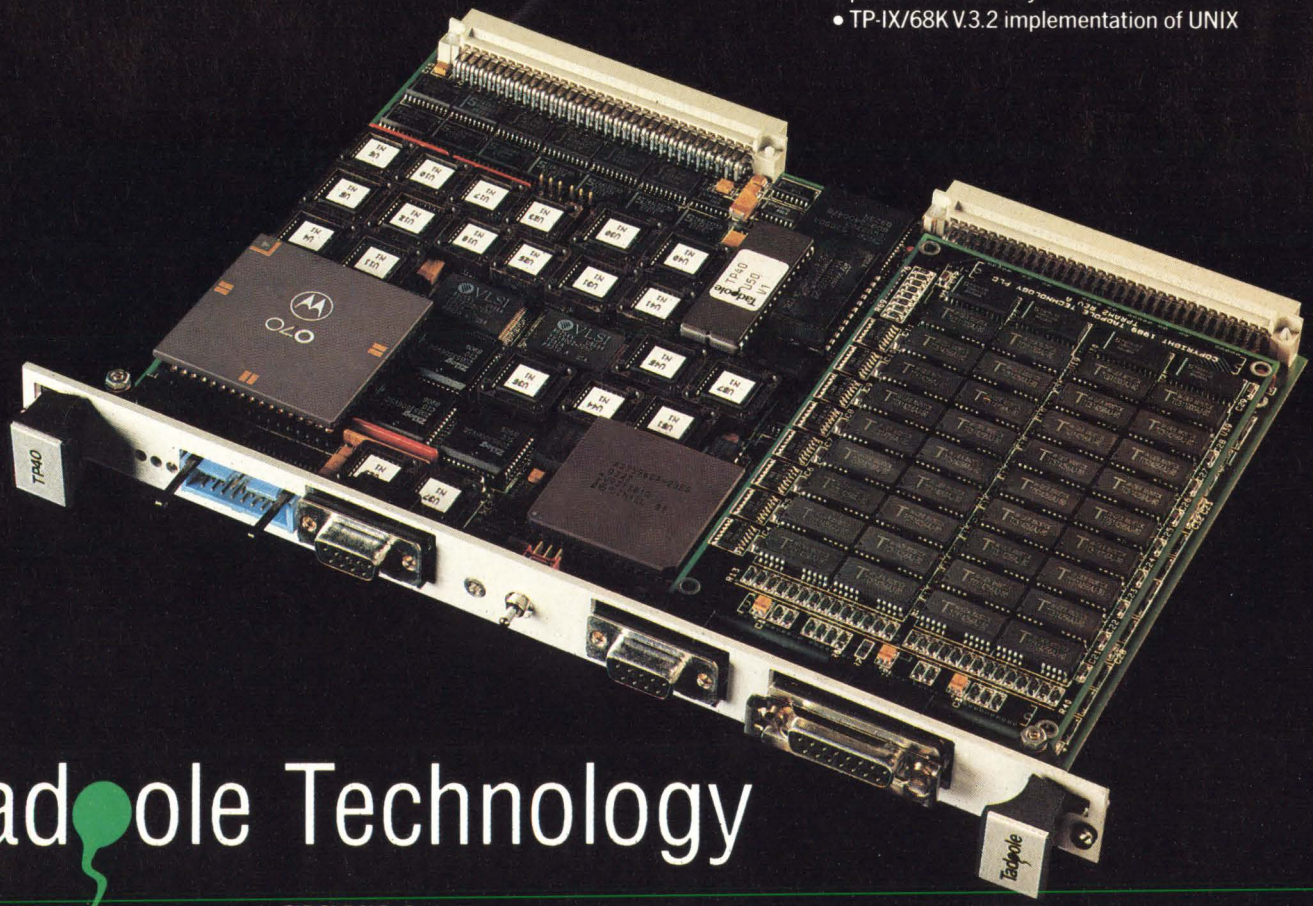
40 BY TADPOLE

TP40V VERY HIGH PERFORMANCE SINGLE BOARD VME COMPUTER

- MC68040 25-33MHz: 20MIPs, 3·5MFLOPs at 25MHz, Integral FPU, 2 x 4Kb Caches
- 2-32Mb Exchangeable DRAM Module, Dual banked, quad-ported to SCSI, VME, LAN and CPU
- VME Rev C IEEE1014:
  - System Controller
  - Interrupt handler
  - 4Kb Mailbox
  - DTB Master/Slave
  - BLT transfers
- SCSI interface on P2. 32bit DMA and NCR 53C90A achieving sustained data transfers up to 4.5Mb/sec
- Ethernet IEEE802.3 with 32bit DMA Controller
- RTC with 2Kb SRAM
- 8bit user I/O
- 2 x RS232 • 2 x CIO
- 6 x Counter/Timers
- Software support includes:
  - pSOS+™ • Velocity • VxWorks
  - TP-IX/68K V.3.2 implementation of UNIX

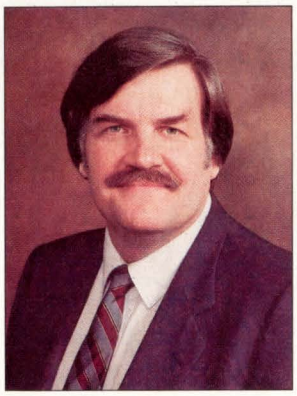


Tadpole Technology

CIRCLE NO. 8

Anything but routine

Being creative is more fun than being routine



John C. Miklosz
Associate Publisher/
Editor-in-Chief

Here at *Computer Design*, we like to think of ourselves as a *technology* magazine as opposed to a *product* magazine. As such, we focus more on design decisions than on design details, on design issues more than on design implementations, on future developments more than on available features, on strategies more than on specifications, and—perhaps most important of all—on trying to provide some insight rather than instruction. It's the difference between what we call our "why-to" editorial and the "how-to" editorial that comprises the stock and trade of the traditional product-oriented design magazines.

What we provide is essential reading for the design engineering managers and senior design engineers like yourself, and something you won't find in any other publication. But there comes a time each month when I envy the chief editors on the product-oriented publications. It's the time of the month when I sit down with the editor who wrote the Special Report for the upcoming issue, our presentation manager, and any other editor who's unlucky enough to be walking past my office when we sit down for our monthly cover meeting. Because product-oriented magazines use product-oriented covers, they don't really have to push their creativity. They can simply base a cover concept on a specific product. What's more, they can get a lot of "free" help from any of the multitude of vendors they routinely write about because *every* vendor wants to have his product featured on a magazine's cover. Not only will a vendor offer to come up with the cover idea, he'll do all the work as well!

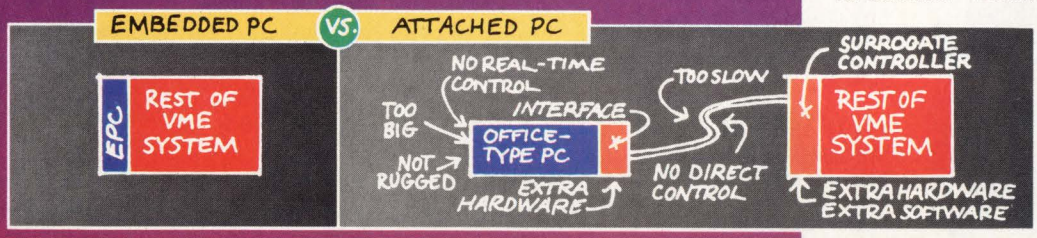
But how do you illustrate a technology development, a design issue, a concept, a strategy, a performance enhancement, or a trend? Believe me, it's a lot tougher than asking someone to come up with a product photo. But it's also a lot more fun because being creative is more fun than being routine.

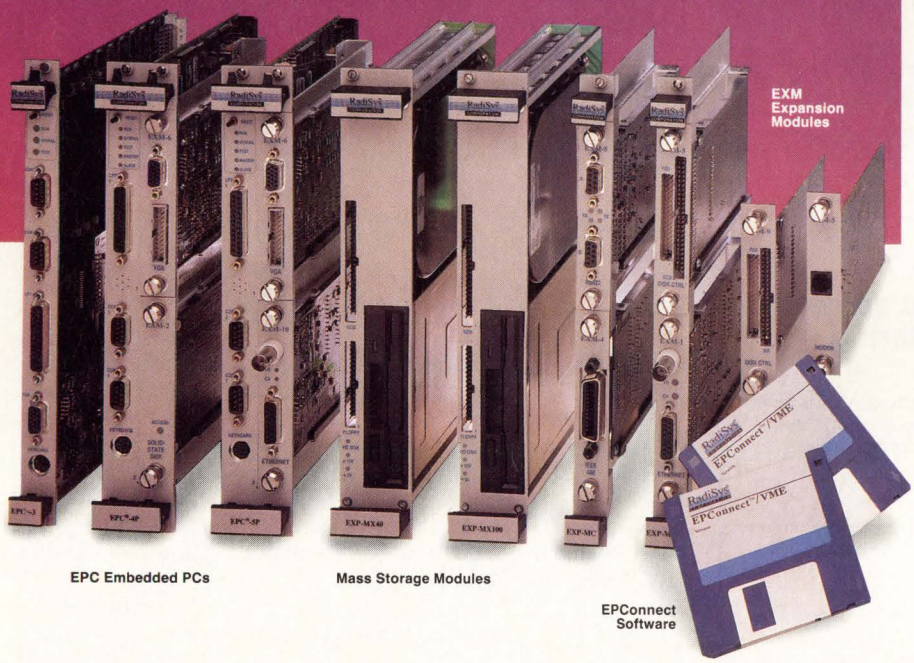
I would like to think that all of our readers understand that we're having a lot of fun with our covers. We want you to find them amusing, sometimes inscrutable, entertaining. We want you to find them anything but routine. We want you to understand that they're different, and that the difference between our covers and those of other publications in this business are as different as the editorial between the covers.

But perhaps you don't look at our covers too closely. To give you a bit more incentive, we've been embedding little bits of "business" (as they say in the theater), sometimes subtly—as in last month's cover where the sirens' notes chirped CAE, AD, CAD, AD—and in the rebus writing on this month's cover. Can you decipher what's on the doors? If you can, drop us a note.

Whoever gives us the correct explanation wins a prize. If we receve more than one explanation, we'll throw them into a hat and choose one. What's the prize? We're keeping that a mystery until next issue.

RADISYS GIVES VME THE INSIDE ADVANTAGE





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The PC Advantage belongs inside your VME system. Not attached to it. By embedding a PC inside your VME card cage, instead of attaching it externally, you break through the inherent communications bottleneck that constricts system performance. You also eliminate the superfluous hardware and software needed to attach two system architectures.

Only RadiSys EPC® Embedded PCs completely integrate the strengths of PC and VME. An EPC, with its exclusive EPConnect™ Software, is the only 386- or 486-based, PC-compatible computer with software that integrates the VMEbus into the DOS, Windows, UNIX and OS/2 environments. EPCs give your VME systems:

- **Highest system performance** from the real-time responsiveness of the direct 32-bit interface between the 386 or 486 and the VMEbus.
- **Improved system packaging** in 1/10th the volume, with integral VME ruggedness, and no bus link baggage.

And EPCs cost you less. EPC-based systems avoid the costly pitfalls of attached PC systems. No extra interfaces, cables, surrogate controllers, or the software to make them work.

Give your VME systems the EPC advantage. Call (800) 950-0044. We'll send all the details. No strings attached.

EPC MODEL	EPC-1 (shipping since Aug '88)	EPC-3 (shipping since Aug '89)	EPC-4 (shipping since Mar '90)	EPC-5 (shipping since Oct '90)
Processor Modules:				
CPU	80386	80386SX	80386	80486
CPU Clock	16 or 20MHz	16MHz	25 MHz	25 or 33 MHz
DRAM	1 or 4 MBytes	1, 2 or 4 MBytes	4, 8 or 16MBytes	4, 8 or 16 MBytes
Graphics	EGA (640 x 350)	VGA (800 x 600)	VGA (800 x 600)	VGA (800 x 600)
Mass Storage Modules:				
Hard Disk Capacity	40 MBytes		40, 100 or 200 MBytes	
Floppy Drive Size/Cap.	3.5" / 1.44 MBytes		3.5" / 1.44 MBytes	
Expansion Capabilities:				
PC Add-in Cards	Yes		Yes	
EXMbus Expansion	N/A	EXM Expansion Modules:		
		EXM-1 Ethernet	EXM-5 Modem	EXM-9 IDE/Floppy Ctrl.
		EXM-2 Solid State Disk	EXM-6 VGA Graphics	EXM-10 Ethernet
		EXM-3 SCSI/Floppy Ctrl.	EXM-7 RS232 Serial I/O	EXM-11 Timer/Counter
		EXM-4 IEEE 488	EXM-8 RS422 Serial I/O	EXM-12 Prototyping Card
Software Support:	EPConnect development, run-time, and multiprocessing software package for DOS, Windows, UNIX, and OS/2			

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THE INSIDE ADVANTAGE

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CIRCLE NO. 9

CALENDAR

CONFERENCES

January 14 - 15, 1992
San Diego Electronics Show

San Diego Convention Center, San Diego, CA. The Pacific Southwest Technology Expo, the San Diego Electronics Show features seminars, demonstrations and technical sessions on electronics packaging for military and design engineers, converting to ISO-9000 standards, FDDI basic architecture and implementation, VME packaging, PLDs, and switch technology for the European Community. Over 300 exhibitors are expected and the show features an all-new CAD/CAM computer lab offering hands-on experience. Information: Epic Enterprises, 3838 Camino Del Rio North, Suite 164, San Diego, CA 92108, (619) 284-9268, Fax (619) 284-7750. **Circle 202**

January 14 - 16
ATE & Instrumentation West

Disneyland Hotel, Anaheim, CA. This conference for test professionals will offer conference sessions, tutorials, minicourses, and forums on systems integration, service, manufacturing, design, and defense issues. More than 75 companies will be exhibiting test equipment and services. Information: Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215-1135, (800) 223-7126, Fax (617) 232-0854. **Circle 203**

January 22 - 25
Internepcon Japan '92

Makuhari Messe (Nippon Convention Center), Chiba, Japan. INJ '92 serves the electronic manufacturing industry and is one of the most well-established electronics trade shows in Asia. INJ '92 will feature more than 30 technical sessions covering design packaging, printed circuit fabrication, circuit assembly, surface mount technology, and testing. Information: Cahners Expositions Japan, Ltd, Shinjuku Nomura Bldg, 1-26-2 Nishishinjuku, Shinjuku-ku, Tokyo 163, Japan, Phone: 03-3349-8501, Fax 03-3345-7929 or The Reed Exhibition Companies, 999 Summer St, PO Box 3833, Stamford, CT 06905, (203) 964-0000, Fax (203) 964-0176.

Circle 204

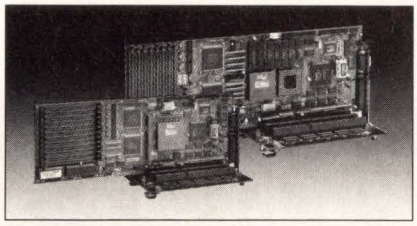
February 4 - 6
AFCEA 3rd Annual Computing Conference & Exposition

Hyatt Regency Crystal City, Arlington, VA. The AFCEA Annual Computing Conference & Exposition (ACCE) presents tutorial sessions and five technical tracks offering in-depth coverage on artificial intelligence; information security; software development; CIM; civilian applications of information technology; and modeling and simulation. More than 80 exhibitors will present state-of-the-art technologies. Information: AFCEA International, Programs Dept, 4400 Fair Lakes Ct, Fairfax, VA 22033-3899, (703) 631-6200, Fax (703) 818-9177.

Circle 205

continued on page 18

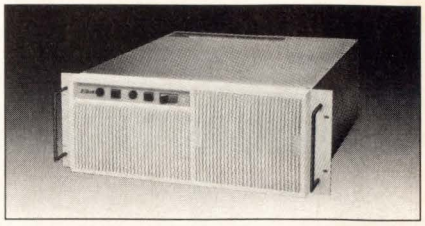
I386, I486 single board computers—versatile, powerful



Built around a 25-33MHz 80386DX, the versatile I386 features 32K cache (I386/25), or 128K cache (I386/33), with up to 32MB of 70ns SIMM DRAM, plus either an 80387DX Coprocessor or a Weitek 3176 Numeric Data Processor. The I486 offers superior processing power for any system configuration using either the 80486DX (25 or 33 MHz) or 80486SX (25MHz) CPU, with optional 256K cache. Both incorporate an IDE hard disk interface, a floppy disk controller, two serial and one parallel port, and a programmable Watchdog timer. **Contact I-Bus,** 9596 Chesapeake Drive, San Diego, CA 92127. **Tel. (800) 382-4229, Fax (619) 268-7863.**

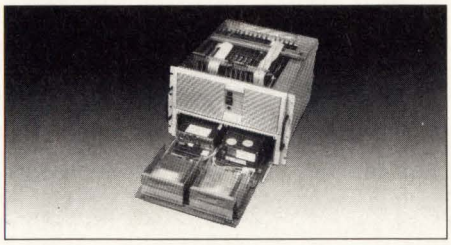
CIRCLE NO. 100

Model 4820 — maximum slots, maximum disks



Now for the first time, OEMs and Systems Integrators can implement designs incorporating up to 20 full-length AT cards, using the new 4820 enclosure from I-Bus to advance current limits of passive backplane enclosure technology. Rack mount, tower and desktop configurations provide an adjustable mechanical hold-down bar, plus front access to up to five half-height drives or two full-height drives and one half-height floppy drive, in a shock-mounted drive bay. Options include 275W or 375W power supplies. **Contact I-Bus,** 9596 Chesapeake Drive, San Diego, CA 92127. **Tel. (800) 382-4229, Fax (619) 268-7863.**

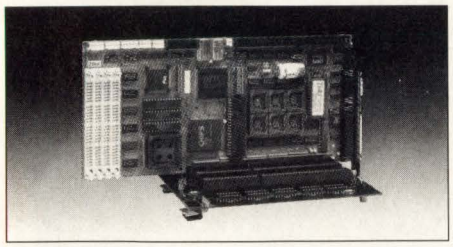
CIRCLE NO. 101



Customer input guides Model 16I Enclosure design

Design and development of the revolutionary new 16I PC Bus System from I-Bus has been totally governed by customer input – as the 16I's unparalleled array of features demonstrates. The 16I offers 16 full-length AT slots, with an adjustable mechanical hold-down bar. 275W or 375W power supplies are optional. Or, if the backplane is segmented (8X8), two separate 150W power supplies are provided, one dedicated to each segment. Power supplies are easily replaced on their own service module. Up to eight half-height drives or four full-height drives (or any combination) are located in a shock-mounted drive bay, accessed from the front via a slide-out drive drawer for easy drive addition or replacement. Rack mount, tower and desktop configurations are available. **Contact I-Bus,** 9596 Chesapeake Drive, San Diego, CA 92127. **Tel. (800) 382-4229, Fax (619) 268-7863.**

CIRCLE NO. 102



I386SX — high performance package

Incorporating a 20 or 25MHz 80386SX CPU and using VLSI, surface mount and CMOS technologies, the I386SX is the most compact I-Bus single-board computer. Also, it operates on less than 6.5W of incoming power. The I386SX features 64K cache, a programmable Watchdog timer, advanced power-fail detect circuitry, 1.5MB of Flash EPROM/EPROM, an IDE hard disk interface, a floppy disk controller, plus two serial and one parallel port. **Contact I-Bus,** 9596 Chesapeake Drive, San Diego, CA 92127. **Tel. (800) 382-4229, Fax (619) 268-7863.**

CIRCLE NO. 103

CIRCLE NO. 104

CALENDAR

CONFERENCES

continued from page 16

February 4 - 6
BUSCON '92 West

BUSCON/92-WEST

Long Beach Convention Center, Long Beach, CA. More than 150 exhibitors will be featured at this bus- and board-systems conference. Technical seminars will include more than 66 lectures and tutorials for software developers and systems engineers working with backplane buses. Attendees can choose from topics which will highlight physics, architectural features, specifications, and protocols and design issues associated with major buses such as VMEbus, Multibus I and II, STD and STD32, PC/AT/EISA and MCA, as well as Futurebus and SBus. Information: Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856, (800) 243-3238.

Circle 206

February 18 - 20
SysComp/92-West

SysComp

San Jose Convention Center, San Jose, CA. The only OEM systems/subsystems components conference and exposition. The technical program will cover microprocessor/system and bus architectures, power sources, display and interface technology, mass storage and new developments in media, embedded software programming, system packaging and concurrent engineering and achieving cost, quality and time-to-market goals. The exhibition will feature vendors of OEM computers, ICs, board-level products, power sources, mass storage, displays, backplanes and enclosures and much more. Information: Paul LaGris, 3432 Timberlake, Costa Mesa, CA 92626, (714) 966-1526, Fax (714) 241-1108.

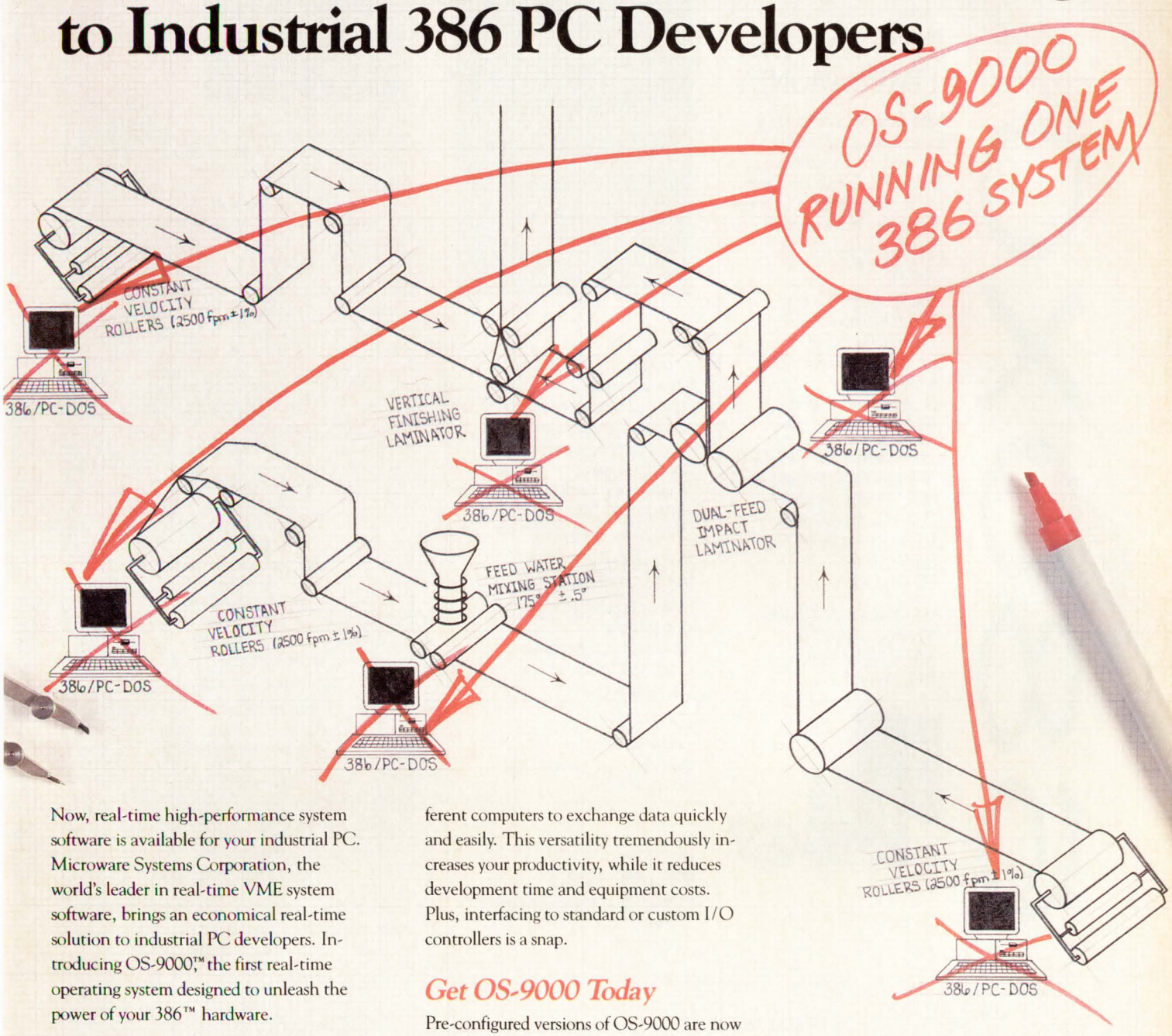
Circle 207

February 18 - 20
RISC '92

Le Baron Hotel/San Jose Convention Center, San Jose, CA. To be held in conjunction with SysComp/92-West, RISC '92 will be the premiere gathering of designers and design managers involved with Reduced Instruction Set Computer (RISC) architectures, systems, programming and applications. A combination of lectures, tutorials and panel discussions will cover areas such as RISC-based multiprocessing systems; fundamentals of Sparc, MIPS R3000/4000 and other architectures; advances in RISC-based CPU boards for standard buses; RISC in multimedia applications; compilers and software development tools, and many more topics. Information: Paul LaGris, 3432 Timberlake, Costa Mesa, CA 92626, (714) 966-1526, Fax (714) 241-1108.

Circle 208

OS-9000. Bringing Economy of Design to Industrial 386 PC Developers



Now, real-time high-performance system software is available for your industrial PC. Microware Systems Corporation, the world's leader in real-time VME system software, brings an economical real-time solution to industrial PC developers. Introducing OS-9000,™ the first real-time operating system designed to unleash the power of your 386™ hardware.

Real-Time Response To Control Multiple Tasks

Why waste the power of your 386 by letting it control only one function at a time? Unlike PC-DOS, OS-9000 is a true multi-user and multi-tasking real-time operating system. Now you can utilize a single PC as a powerful time-sharing system able to control multiple processes simultaneously. And by using industry-standard protocols (like Ethernet and Arcnet), OS-9000 allows PCs to be interconnected and connected to different computers to exchange data quickly and easily. This versatility tremendously increases your productivity, while it reduces development time and equipment costs. Plus, interfacing to standard or custom I/O controllers is a snap.

Get OS-9000 Today

Pre-configured versions of OS-9000 are now available for your 80386™ PC-compatible hardware. These systems include integrated development tools such as a "shell" user interface, over 70 powerful utilities, a superlative C compiler, a C source-level debugger and a screen editor. Your full-featured, "plug-and-play" OS-9000/386 system is now available for just $995.

Call Microware® today to order your copy of OS-9000. Or order a FREE copy of the OS-9000 Catalog (your complete guide to the OS-9000 Real-Time Operating System).

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CIRCLE NO. 14

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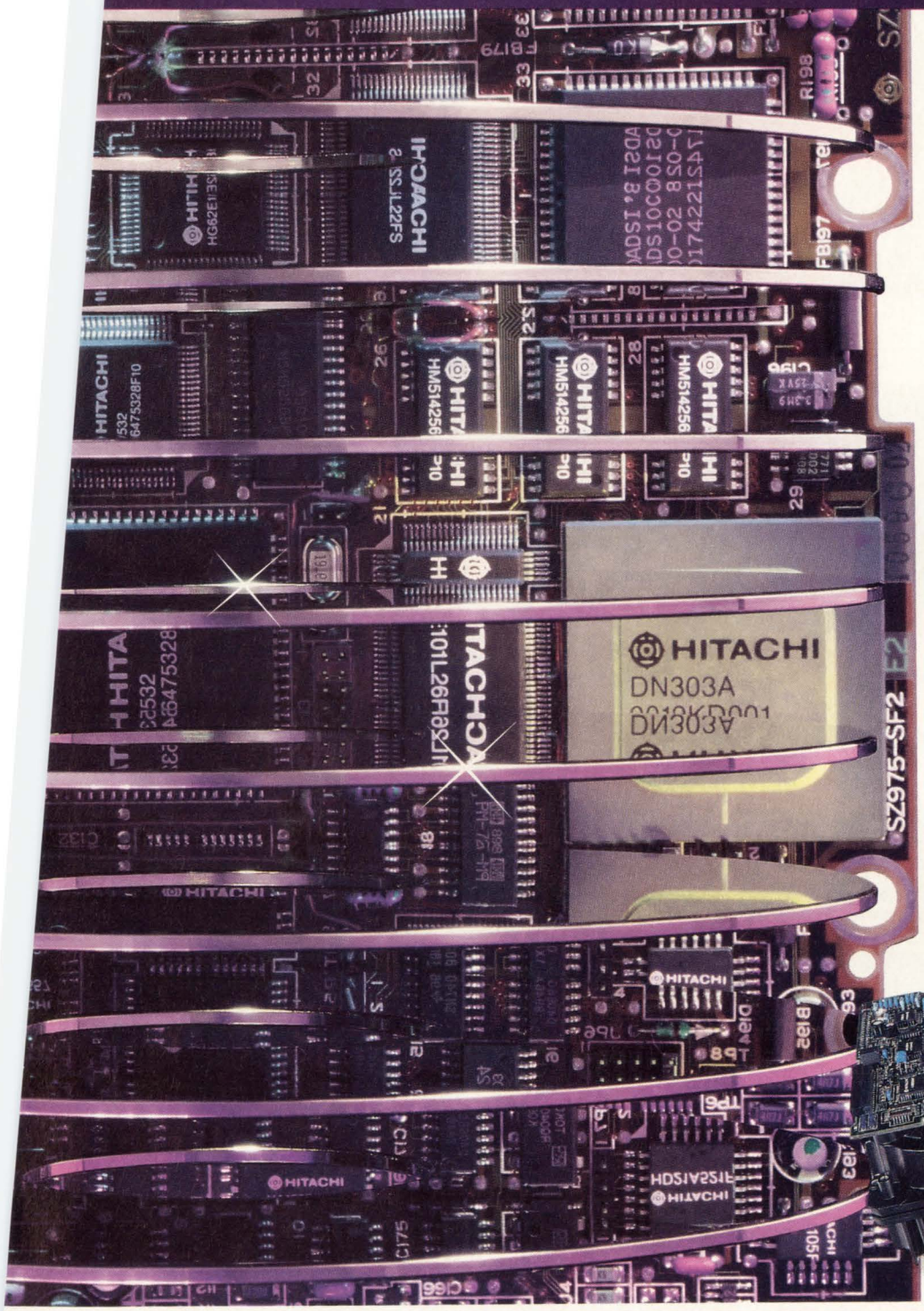

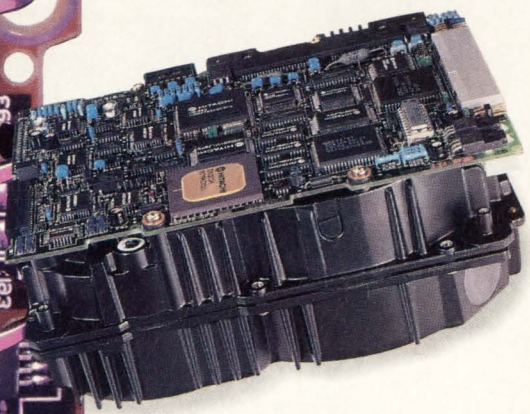

Edge-to-Edge Performance

The DK516C-16 uses Hitachi's advanced proprietary technology to deliver 1.65 GB of capacity and a fast 13.5 ms average access time.

Its SCSI interface provides a maximum data transfer rate of 5.0 Mbytes/sec (synchronous), with a 256 Kbyte data buffer and read look-ahead cache.

Or, if you have an ESDI application, look into Hitachi's 1.54 GB DK516-15 with a 14 ms average seek time and a 2.75 MB/sec data transfer rate.

Edge-to-Edge Quality

Choose the DK516 and you get a drive backed by the quality and reliability of Hitachi—a $54 billion company. Unlike other drive manufacturers, we design, build, and test all key components in-house.

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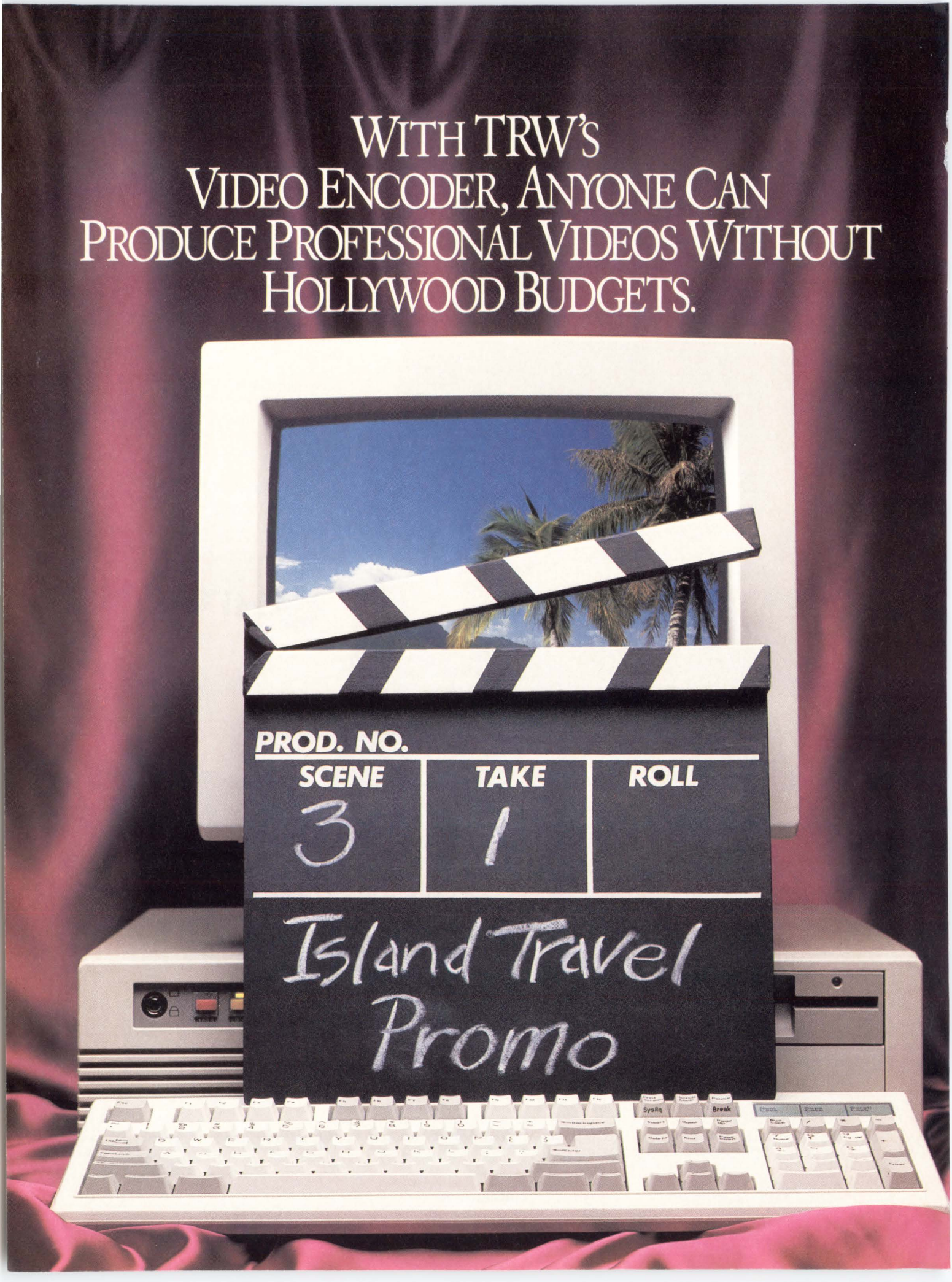
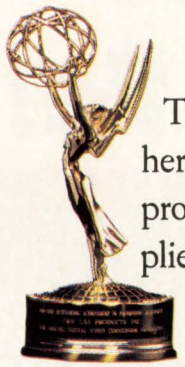
CIRCLE NO. 16

WITH TRW'S VIDEO ENCODER, ANYONE CAN PRODUCE PROFESSIONAL VIDEOS WITHOUT HOLLYWOOD BUDGETS.





1988-1989 Emmy Award

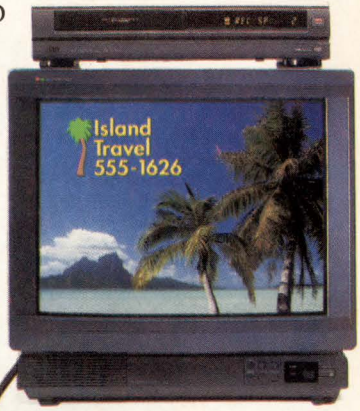
Lights. Camera. Action. The monolithic Video Encoder is here. Created by TRW, the film and production industry's leading supplier of high-performance ICs. And the only company ever to be awarded an Emmy for its video IC technology.

Now, TRW brings you the first in its new line of affordable multimedia ICs for desktop video: The TMC22090.

And that means converting RGB, YUV or color-indexed computer images and graphics into studio-quality NTSC, PAL or S-Video signals can now be done with a single, low-cost chip. One fabricated in TRW's Omicron-C™ 1 μ CMOS process. Packaged in an 84 lead PLCC. And, of course, designed with the full-spec performance that is synonymous with TRW standards.

The TMC22090 boasts a 256x8x3 color lookup table, a pixel mask register and compatibility with 171 and 176 RAMDACs. All of which means transparent interface with existing device drivers.

Better still, the high performance Hollywood has come to rely on is provided by 4:4:4 digital encoding, oversampled 10-bit outputs, and built-in test signals. The TMC22090 even gives you a JTAG interface for low cost production testing. So for everything from simply providing an affordable video output for computer display boards, to developing complex desktop video workstations, you can design in confidence. With the video encoder from the leader in video ICs: TRW.



Overlay graphics and titles onto video by selecting a transparent color for the Video Encoder chroma key.

And you can count on TRW to keep you at the forefront of multimedia, too. This Video Encoder, after all, is just our debut. We've got some great sequels in development.

For data sheets, applications and other information on TRW's TMC22090 Video Encoder, as well as to be first in line for coming attractions, call or write today:

TRW LSI Products Inc.,
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(619) 457-1000, FAX (619) 455-6314
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STANDARDS SET. STANDARDS TO BE MET.

CIRCLE NO. 18

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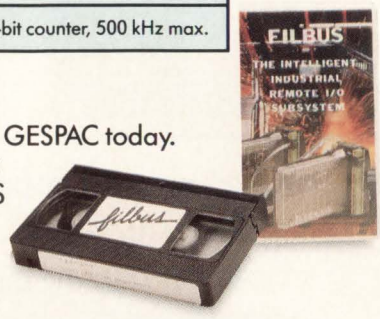

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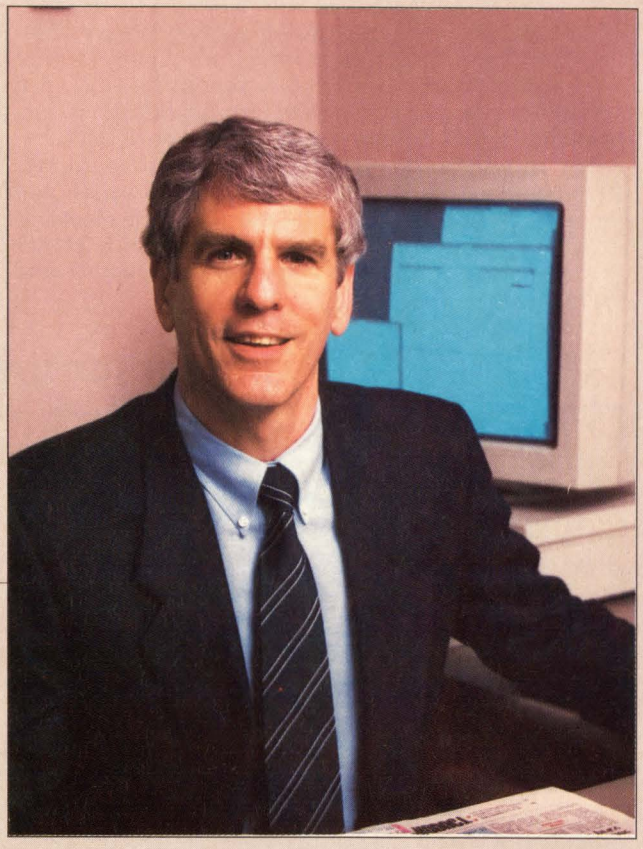
CIRCLE NO. 19

John East on: Technology transparent design



Having watched the programmable logic market over the past 20 years, I believe the industry is at a crossroad. While system designers helped make the logic market one of the fastest growing segments of the semiconductor industry in the late 1980s, designers' productivity is at risk in the 1990s unless market players can provide higher levels of integrated solutions to help customers get innovative, new products to market at an ever-faster pace. Instead of focusing on integrated solutions, I've found that many of today's suppliers of logic-integration solutions are just protecting their turf—hardly unexpected given the high-growth nature of the business.

The programmable logic market was established in the 1970s with the introduction of simple programmable logic devices and currently comprises PLAs, PLDs, field-programmable gate arrays (FPGAs), and variations of these devices. The programmable logic market grew rapidly in the 1980s—a trend that's expected to continue well into the '90s.

But the development of higher density, better performing PLDs is only part of the answer to continued market growth. For programmable logic to meet market demands in the 1990s, vendors must begin working together to provide open, standards-based, integrated-logic solutions that span the design task linking these logic solutions to CAE/CAD tools, EDA software, highly-integrated ASICs, and a host of other hardware-, software- and silicon-based capabilities.

TTD to the rescue

One can summarize this open concept with a single phrase—Technology Transparent Design (TTD). The concept, popularized by Alberto Sangiovanni-Vincentelli at the University of California, Berkeley, refers to a vendor-independent hardware-, software- and silicon-based design solution. TTD provides the ability to design any system while putting off key process and ASIC methodology decisions until the end. In short, TTD is to logic integration what open systems are to the computer industry. Without this level of openness, the market will remain highly fragmented—with many players offering proprietary pieces of the total solution.

TTD is an industry imperative. Today, designers using one schematic capture or EDA tool on one hardware platform cannot easily share data with designers using other tools on other platforms. Compounding the problem, when designers need to make a transition from one type of PLD to another, interfaces have either been lacking altogether or provided with great reluctance.

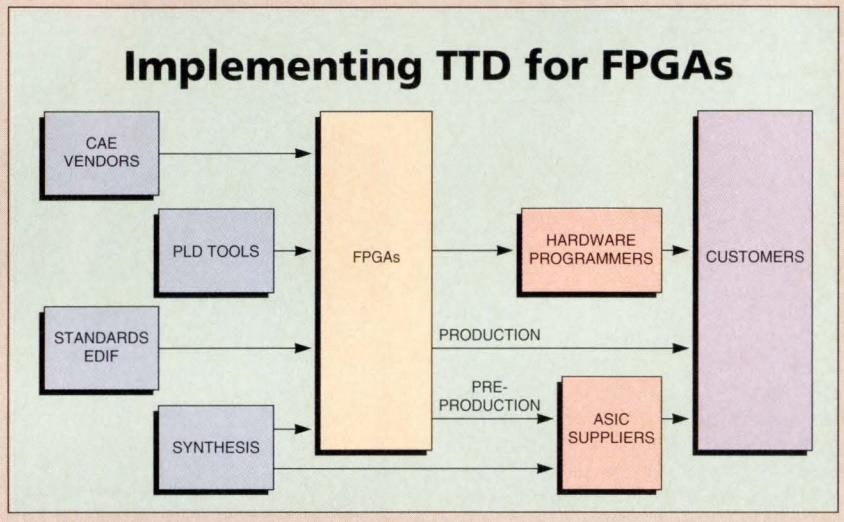
This lack of "ease-of-use" is more than just a nuisance. The obvious lack of integration between hardware, software and silicon hampers engineering productivity. As time-to-market pressures continue to escalate, this bottleneck becomes an ever-more-vexing issue for systems designers. Whether or not U.S. companies—which currently dominate the programmable logic market—respond in a timely fashion to this challenge, it's just a matter of time before industry innovators seize the opportunity. We have all seen this free market truism play out in every market sector, from automobiles to computer systems to electronics.

The need for TTD and FPGAs—as logic-integration product vehicles—are heavily intertwined. Indeed, TTD and FPGAs could actually transform the industry. Over the past several decades, the electronics industry has been transformed several notable times by the entrance of new technologies. The first such occurrence of a transformational development—or paradigm shift—in the electronics industry occurred in the 1970s when core memory was finally dislodged by semiconductor memory. The wide-scale availabil-

John East is president and CEO of Actel (Sunnyvale, CA).

ity of inexpensive, highly integrated memory revolutionized the industry, spawning a whole new family of computer systems—the minicomputer—and such notable market players as Data General (Westborough, MA) and Digital Equipment Corp. (Maynard, MA).

The popularization of the microprocessor in the late 1970s and early 1980s had a similar impact and represents the second paradigm shift in the electronics industry. Once the single-chip microprocessor gained a foothold in the early 1980s, systems and peripherals developers completely abandoned the practice of designing and building processors and operating systems software. The impact on the industry was nothing short of revolutionary. Development costs and time-to-market plummeted. And a multibillion dollar industry—for personal and desktop computers—was born.



In FPGA applications, TTD would give designers access to CAE software, PLD systems, synthesis tools, hardware programmers and design platforms and a vendor-independent gate array migration path.

Meeting the logic-integration requirements of the 1990s is going to require more than a cooperative spirit among vendors who service the logic-integration market. Vendors will need to fully embrace the concept of TTD to allow the integration of disparate systems, technologies, tools, and software into a single solution for the end user. Clearly, users of EDA tools continue to face the risk of system or tool incompatibilities. These barriers must be overcome if design productivity through the use of programmable logic is to proliferate in the coming years.

FPGAs: The third paradigm shift

For system designers, TTD would eliminate dependence on any one company's schematic capture or simulation software, high-level synthesis support or silicon/ASIC methodology. In the application of FPGAs, TTD would provide designers with access to the CAE software, PLD systems, synthesis tools, hardware programmers, and design platforms of choice, as well as vendor-independent gate array migration paths.

Consider, for example, the ability to let designers, for the first time, input and synthesize any high-density FPGA from a hardware description language specification using an industry-standard tool such as VHDL. Or, alternatively, consider the benefit of FPGA design entry using a standard interface such as the EDIF (Electronic Data Interchange Format). Within the context of a TTD environment, either design-entry scenario is available to designers. Moreover, a direct migration path and access to gate arrays from any of the industry's suppliers will provide designers with complete flexibility at "design exit." And between input and output, the ability to program devices using industry-standard hardware is also important.

The emergence of TTD capabilities in all segments of the logic-integration industry—from EDA to ASICs to foundries—would not only decrease time-to-market, increase competitiveness and heighten innovation, but would put FPGAs in the same league as semiconductor memory and the microprocessor as industry-revolutionizing developments. In fact, TTD could become the leading FPGA market driver.

TTD is important given the escalating pressure to reduce time-to-market. Many new products are obsolete in as little as a year. This trend is only expected to intensify as time passes. As a result, the ability to innovate sequentially and rapidly is becoming a matter of market survival. The emergence of TTD is essential if engineers and designers are to keep pace.

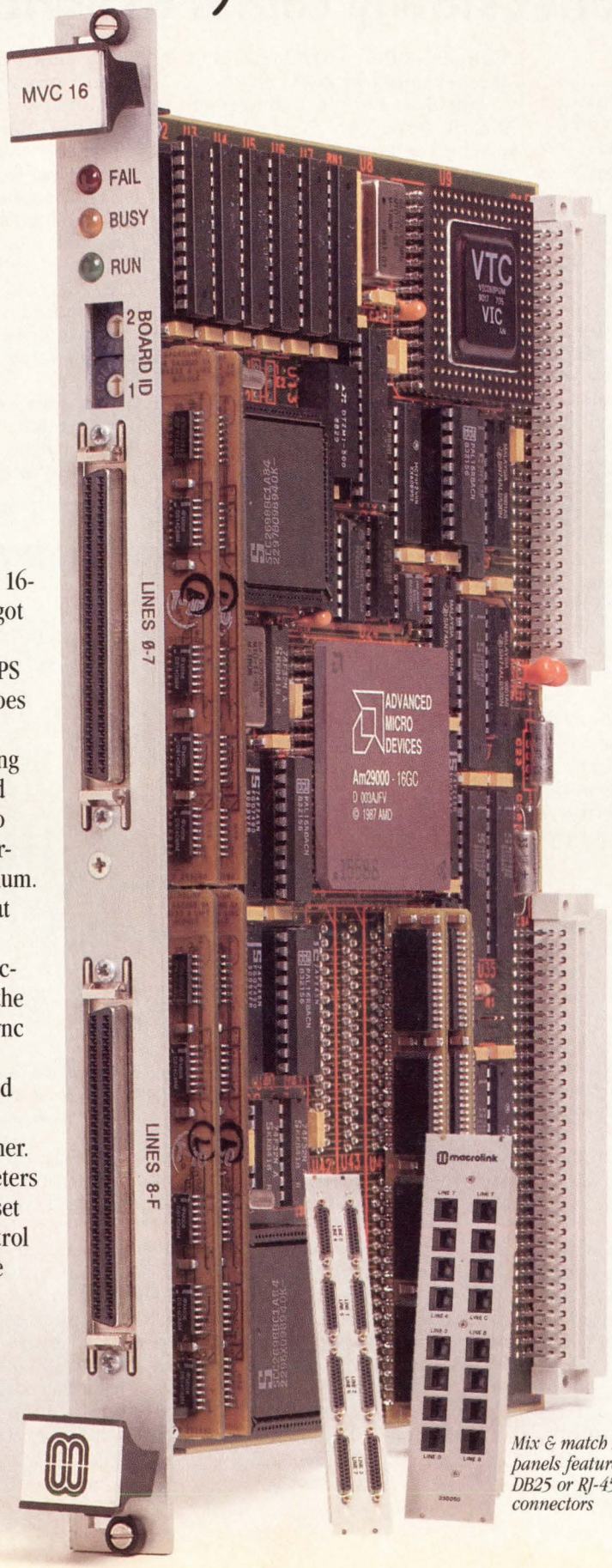
The state of the industry

The logic industry, by and large, is beginning to address the TTD challenge. The emergence of EDIF—an output language that supports file exchange—is a promising development to help bridge the chasm between today's divergent suite of EDA tools. Also promising are the emergence of industry frameworks, non-proprietary hardware programmers, standards-based hardware platforms, and translators that streamline the transition from one PLD to another.

The challenge for the logic industry is to offer an ever greater degree of openness—TTD—among complementary and competitive products and technologies. The closer the industry moves toward this ideal, the better positioned it will be to meet evolving customer demand for quicker time-to-market and reduced development costs.

In fact, we believe that the rapid proliferation of FPGAs is leading quickly to a new era of logic integration in which PLDs—like semiconductor memory and microprocessors—are essential components in every new system on the market, replacing the discrete components and chip sets still used by many vendors today to differentiate their product offerings. Such wide-scale use and proliferation, accelerated by TTD, is fueling a multibillion dollar market for FPGAs, underscoring them as the electronics industry's third major paradigm shift.

16 lines, No waiting.



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CIRCLE NO. 20

INTEGRATED CIRCUITS

Silicon for Sonet slowly comes to light

Dave Wilson, Senior Editor

Digital telecommunications networks are optimized for voice traffic and aren't really suited to the transmission of data. What's more, they provide relatively low bandwidth and carry a central computing overhead just to control them. Central to their philosophy is a rigid multiplexing hierarchy, where the identity of an individual channel is lost after it's multiplexed up to high speeds for transmission with other channels. Low transmission rates would be fine if users would be satisfied with simple voice communications. But applications such as "multimedia" demand that these networks embrace higher bandwidths, so that users can transmit voice, data and video over them.

Two standards—one from the United States and one from Europe—are providing direction for next-generation telecom networks. The U.S. standard is Sonet (Synchronous Optical Network), the European CCITT standard is SDH (Synchronous Digital Hierarchy). Compatible with one another (at least at higher data rates), both are optical standards that define a means of transmitting data at rates up to 2488.32 Mbit/s.

Slow growth at first

But Sonet and SDH networks won't spring up overnight. At present, the majority of work in the area is purely semicustom design work by telecom houses such as Fujitsu and Northern Telecom. Only when the networks are more established will smaller telecom vendors start to build terminal equipment that can attach to the Sonet or SDH networks. That's the time when a market for standard chips and chip sets may emerge.

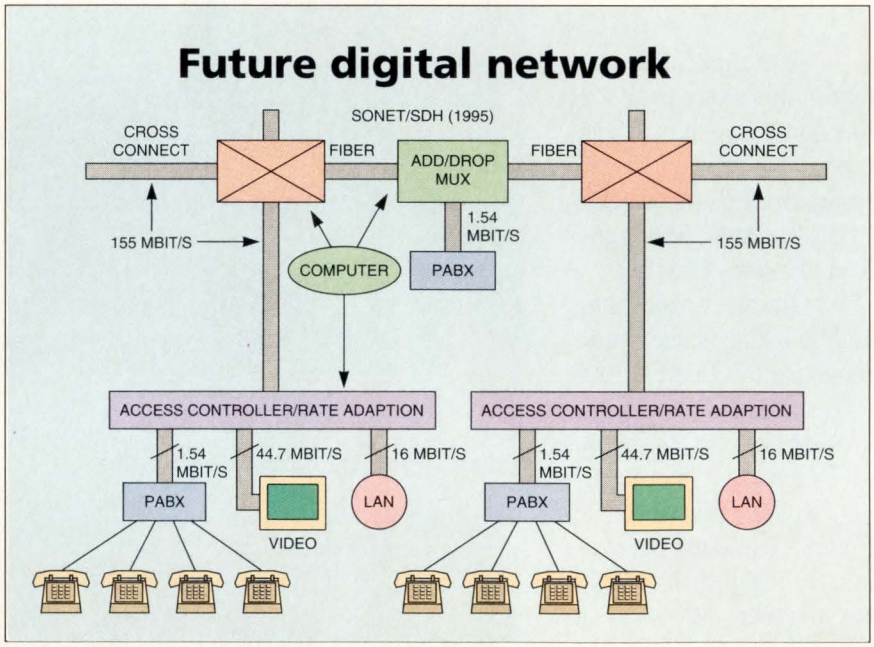
"Up until the development of Sonet as a standard, a lot of the major communications manufacturers had their own proprietary protocols for high-level multiplexing and communication, and that created interoperability problems among different vendors' equipment," says Al Kozak, MCM marketing manager at Pacific Microelectronics Centre, (Burnaby, British Columbia, Canada). "But with Sonet, that interoperability problem is gone."

David J. Berrill, manager of the North American marketing ASIC product department of Texas Instruments (Dallas, TX) agrees. "With Sonet, a small guy can design to the standard without having to reverse-engineer proprietary interfaces," he says.

In the short term, current implementations have shown that chips for Sonet aren't going to be cheap. They will use technologies such as ECL, gallium-arsenide and bipolar, sometimes—especially at the higher Sonet speeds—within the same multichip module (MCM). Pacific Microelectronics Centre, for example, developed an MCM just to build a device to interface three channels of STS-3 signals to a Sonet STS-12 622.08 Mbit/s data stream. The company recently disclosed it will jointly develop several Sonet products with AMCC (San Diego, CA). The first products from that union will be bipolar line interfaces for 155- and 622-Mbit/s applications. Future products include chips for 2.4-Gbit/s applications, available in 1992.

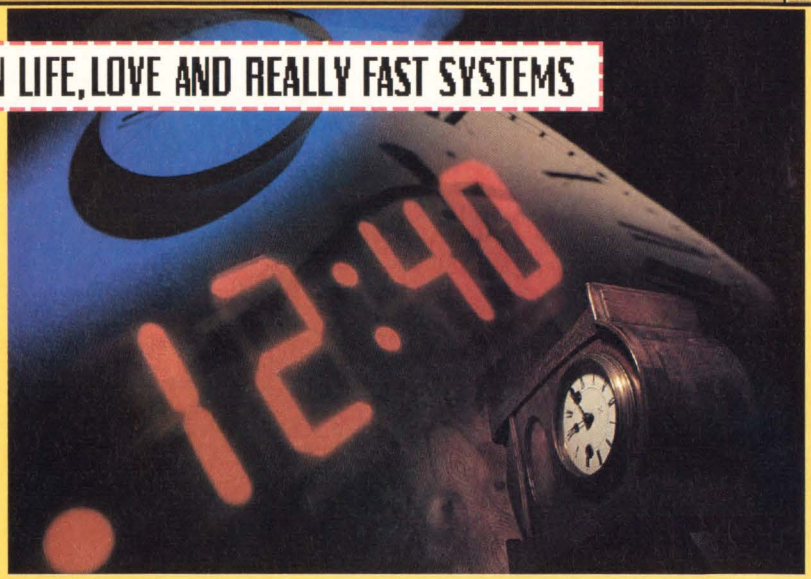
For its part, Transwitch (Shelton, CT) has developed a number of Sonet products based on 1.5μ-CMOS technology. But Jitender Vij, director of applications engineering at Transwitch, says the company is planning to move to BiCMOS and GaAs technology because some 155-Mbit/s interfaces will demand it. "We are also looking into using multichip modules," he adds. Through a licensing agreement, Texas Instruments will manufacture and market some of Transwitch's Sonet devices, although TI has yet to disclose which ones they will be.

In addition to the Transwitch arrangement, TI has a strategic alliance with a Swedish telecommunications manufacturer, Ericsson Telecom. TI recently demonstrated a digital cross-connect switch based on its TGB1066 gate array family that may have been developed in conjunction with that company. The digital crosspoint switch could be used in the design of a self-routing digital cross-connecting router. The part, built using the company's TGB1066 0.8μ ECL gate array family offers the ability to demultiplex eight channels of Sonet at 155 Mbit/s, route the channels through



Future digital networks, such as Sonet and SDH, will make multimedia a reality. They will let users integrate video, LANs and PABX systems into fiberoptic networks.

TIMING IS EVERYTHING, IN LIFE, LOVE AND REALLY FAST SYSTEMS



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Editorial contributions: Tim Wilhelm, Luis Pineda, Ali Mesri and Cynthia Jones.

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The continued evolution of workstation monitor resolution is about to write a new chapter. The evidence: 1600 x 1280 displays have dropped into the $4,000 range, just the price point that made today's widely popular 1280 x 1024 monitors "acceptable" several years ago.

Besides price—and the fact that higher resolution is an unending "gotta have" for workstation users—1600 x 1280 resolution acceptance is being driven by the growing desktop video/multimedia movement in the U.S. and Europe and, in Japan, by the high-resolution demands of displaying kanji.

Customers using our Bt468 RAMDAC are ready for the move to 1600 x 1280. That's because the frame buffer architecture for 1280 x 1024 and 1600 x 1280 monitors are the same. It's an easy upgrade path. At 200 MHz or more, with 8:1 MUX and 25 MHz VRAM compatibility, it's a necessary component for 1600 x 1280 screens. If "early to market" is part of your systems strategy, you may want to take a good look at the readily available Bt468.

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a crosspoint switch and multiplex them out at similar speeds.

"From an ASIC standpoint, we're providing the vehicle to let certain standardized functions be embedded within a high-density ASIC, along with customer-specific circuitry that would personalize it for different applications," says TI's Berrill.

Telephone switching systems may change dramatically over the next few years.

Ericsson Telecom is due to roll out multiplexers, digital cross connects and network-management tools initially to meet the SDH specification. "At the higher data rates, the worldwide telecom leaders don't have high enough product volumes at 2.5 or 10 Gbit/s to drive any economy of scale," says Gregory Waters, strategic marketing manager at TI. Of course, TI would like to standardize some functions at the higher speeds to lower costs. "We have BiCMOS and sub-micron bipolar and GaAs," he says. "At the 156-Mbit/s level, we will make devices using a combination of CMOS and BiCMOS processes," he adds. Designers can expect TI to bring out some devices in addition to the Transwitch devices later in 1992.

Self-contained Sonet

There are two major components to the Sonet packet—the first component is overhead, the second is payload. Each Sonet or SDH frame carries its own identity and synchronization information contained in the overhead. That includes the source of the data as well as information on where the data starts within the frame. This will force some dramatic changes to telephone switching systems over the next few years. The central office computer, for example, will no longer be needed for functions such as frame synchronization. And the dynamic bandwidth of the network can be allocated under centralized software control.

The ultimate aim of digital network designers, at least according to TI's Berrill, is to build more advanced packet-switched networks that would build on Sonet or SDH as the transport layer. Packets on the network would contain source and destination addresses plus data synchronization information. And making use of them, future digital networks will include "intelligent" cross-connect switches that will perform self-routing without the need for a central computer.

Four join forces

To further Sonet compatibility goals, AT&T Microelectronics, BT&D Technologies, Fujitsu, and Hitachi agreed earlier this year to establish internationally compatible sources of fiberoptic transmitter and receiver modules in support of the Sonet and SDH industry standards. The four will support common product specifications, including pin-for-pin compatible transmitters and receivers. The result of these and other standardization activities will be a digital network in which the present chain of proprietary multiplexers is replaced by access controllers and rate adoption mechanisms that will let a number of different sources, such as video and fiber LAN, be mixed into the data stream at different rates. Also, Sonet protocol features will reduce the dependency on large computer systems to handle trafficking.

■

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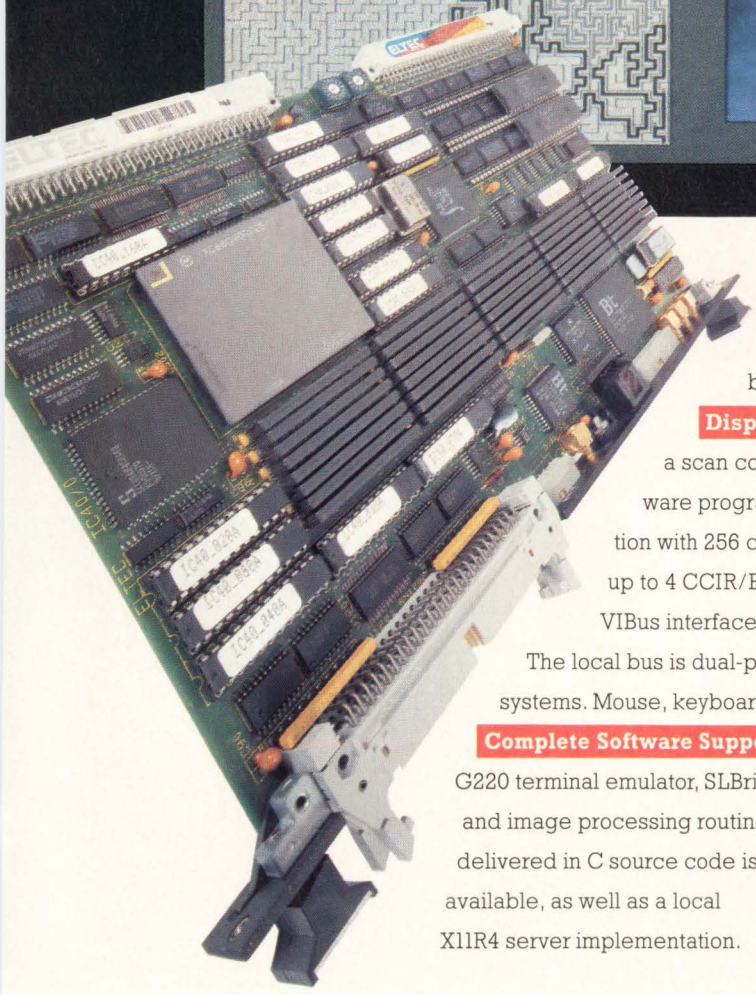
When Speed is Paramount:

IC40 – The VMEbus Board for Graphics and Image Processing

Photograph of Original Monitor



Speed Optimum throughput is achieved through the use of the MC68040, one of the most powerful CISC processors available, offering 20MIPS and 3.5MFLOPs combined with a local bus bandwidth of 40MB/sec. Picture aquisition occurs in video realtime.

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Complete Software Support The IC-40 Toolpack with OS-9 operating system, G220 terminal emulator, SLBridge host communications link and library of graphics and image processing routines, delivered in C source code is available, as well as a local X11R4 server implementation.

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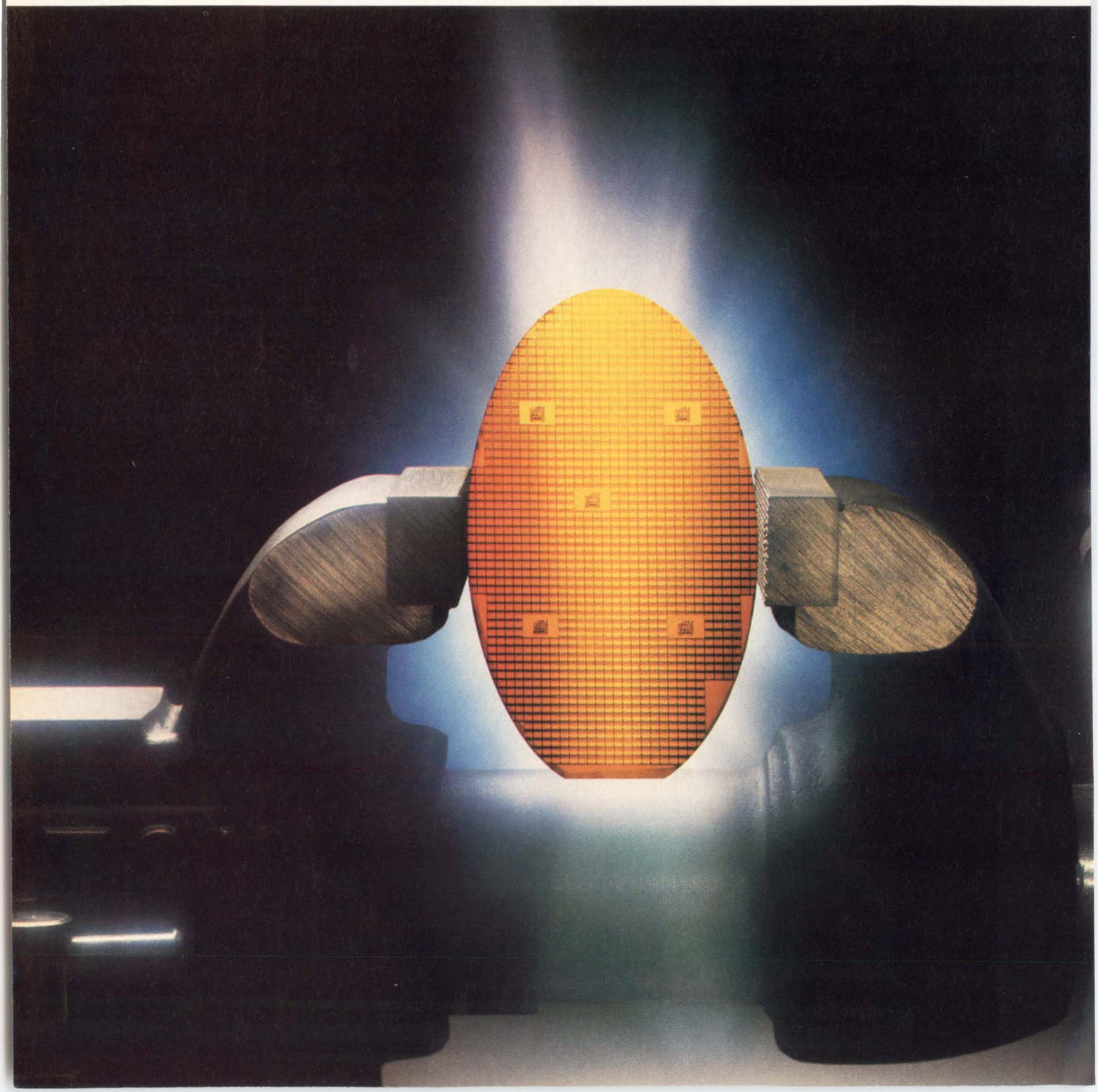

speed from our logic. as 4.1 ns!

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All this in Widebus

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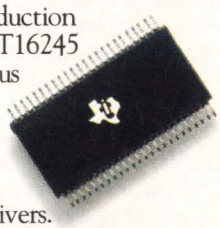
Among the many ABT Widebus functions released is the 'ABT16244, a 16-bit buffer and line driver. It exhibits much greater stability of propagation delay *(see chart)*, which results in a lower derating factor across the number of outputs switched.



Also in volume production are the Widebus 'ABT16245 16-bit bidirectional bus transceiver and the 'ABT16543 and 'ABT16952 16-bit bidirectional registered bus transceivers.

As in our successful Advanced CMOS Logic (ACL) Widebus family, these devices come in our leadership surface-mount shrink small-outline package (SSOP) that gives you twice the number of I/Os as a standard small-outline package in the same space.

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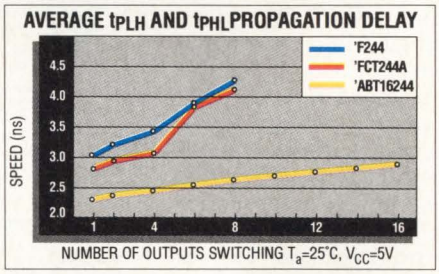

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TEXAS INSTRUMENTS

08-1139

INTEGRATED CIRCUITS

RISC processors dressed up for embedded applications

Dave Wilson, Senior Editor

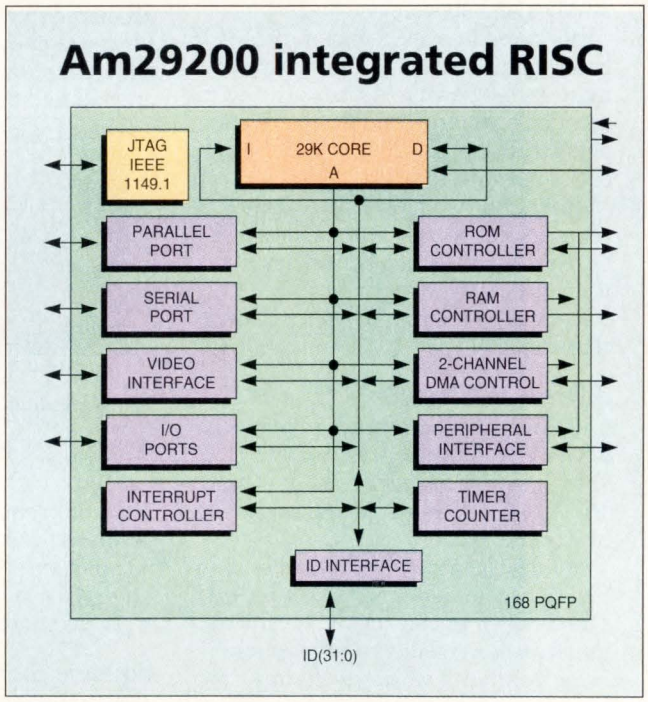
First-generation embedded RISC processors sported relatively generic feature sets that weren't cost-effective in high-volume, low-cost applications. Newer embedded RISC processors, however, are targeted at specific markets and applications, integrating most of the application-specific system interface logic on-chip. The result is a number of highly integrated, highly targeted, inexpensive RISC embedded machines that provide an irresistible alternative to Motorola's processor offerings (see "RISC champions challenge Moto in embedded control," Computer Design, October, p 98).

There are so many vertical markets where embedded controllers could live that a single processor vendor can't be expected to craft architectures to cover all the bases. In the short term, then, RISC vendors are carving out niches where they expect to find the greatest revenue.

Three recently announced processors testify to the trend. The first, the R33020 from LSI Logic (Milpitas, CA), is a complete X terminal controller on a single chip (*sans* Ethernet controller). The second, the AMD 29200, a 29000 derivative from Advanced Micro Devices (Austin, TX), integrates all of the system logic for a laser printer onto a single chip. Finally, the NS32AM160, a National Semiconductor (Santa Clara, CA) part, represents a RISC/DSP-based controller that lets designers of digital answering machines (DAMs) build a fully functioning system in about 1 in.^{2} of printed circuit board (PCB) space.

Breaking into X Windows

By integrating many of the peripheral functions needed in an X terminal design with a MIPS R33000 RISC controller, LSI Logic has built the world's first embedded processor specifically aimed at solving the system demands of X terminal designers. Indeed, the integration/price level offered by LSI Logic ($129 in volumes of 1,000 for the 25-MHz part) makes it certain the device will seriously challenge both the established high-performance AMD-based 29000 and Intel-based i960CA terminals, as well as older, dual processor Motorola/Texas Instruments hybrid designs—not to mention the role of Texas Instruments' (Dallas, TX) graphics processor family in graphics accelerators for personal computer platforms. The LSI Logic chip has already received accolades from AGE Logic (San Diego, CA), a software house well-known in the X business for its expertise in porting X code to a number of different processors, including the i960 and 29000 families. "We see this chip becoming a major factor in the X terminal market," says Peter Shaw, AGE's CEO.



The newest member of AMD's 29000 family is the 29200 microprocessor. AMD has integrated most of the functions currently found on laser printer controller boards on a single chip in an effort to kick Motorola's 68000 out of low-cost machines.

The new LSI Logic device, dubbed the LR33020 GraphX Processor, is based around the company's R33000 MIPS chip introduced in Oct. 1990. On-chip are the MIPS RISC core, a dedicated graphics coprocessor, a 4-kbyte on-chip instruction cache, a 1-kbyte data cache, as well as a four-deep write buffer, three timer counters, a DRAM controller, two PS/2-style serial I/O ports, and video control logic. The memory interface supports a direct interface to interleaved or noninterleaved DRAM, a glueless 8- or 32-bit PROM interface, four-channel DMA, chip selects, and programmable wait state generators. To help out with the graphics, the chip includes a bitblt (bit boundary block transfer) processor, video FIFO with DMA, video timing generators, direct support of video RAM, burst reads and writes for pixel data and hardware cursor support. The chip itself will be available in a 208-pin metal quad flatpack (MQFP) package and a ceramic 224-pin grid array (CPGA). Sampling begins this month.

Just as LSI Logic claims to have produced the ideal device for the world of X terminals, AMD hopes its 29200 will be the processor of choice for designers of laser printers. Even though the 29000 family has been very successful in that arena already, Motorola's 68000 and highly integrated derivatives of it continue to account for high volumes at the low end of the laser printer business. With the 29200, AMD hopes to change that picture. The device aims to minimize the system cost by incorporating a complete set of peripherals commonly found in laser printer applications. On-chip functions include a ROM controller, a peripheral interface adapter, a DMA controller, a programmable I/O port, an IBM PC-compatible parallel port, a serial port, and an interrupt controller.

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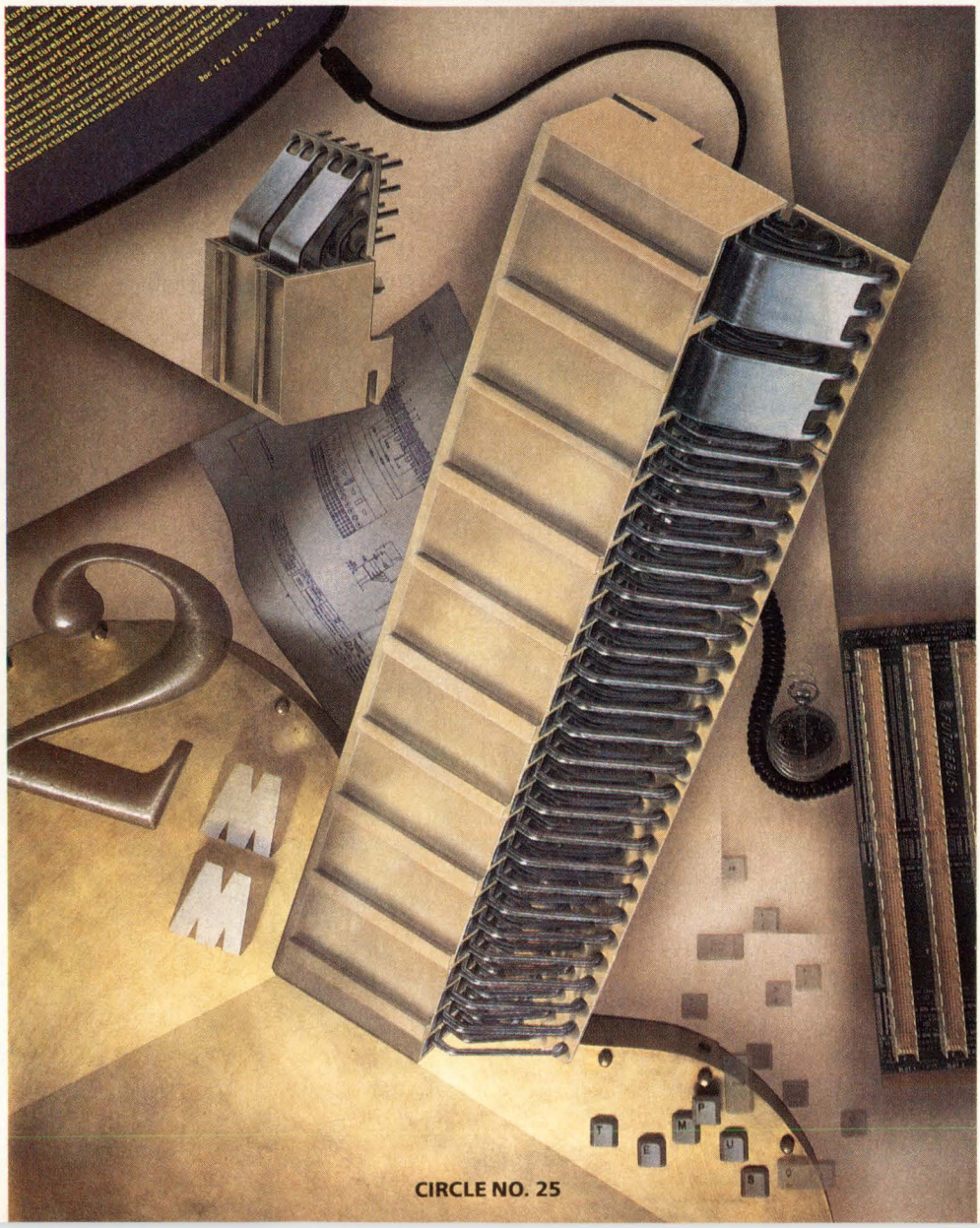

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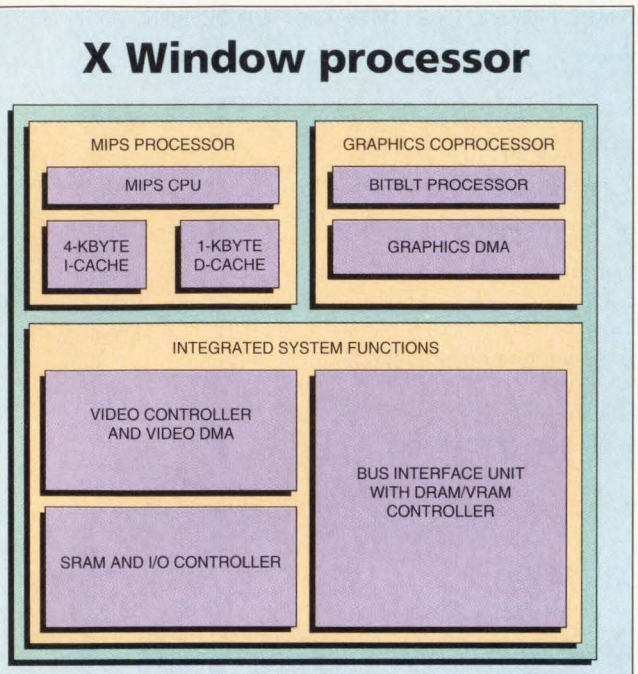
INTEGRATED CIRCUITS



X marks the spot where LSI Logic hopes to build terminals around the LR33020, the world's first RISC-based X windows terminal controller. LSI Logic has integrated most of the peripheral control circuitry needed to build X terminals onto the device.

Of course, for some designers, a high level of on-chip integration represents a "Catch 22" situation. While they appreciate the fact that high integration levels lead to a lower-cost system solution, they are concerned there is little room to add their own value to a design. To circumvent that problem, AMD engineers offer some flexibility with the 29200 part. It not only provides programmable memory widths and programmable wait states, it also offers burst mode and page mode access support as well. In addition, the ROM controller accommodates memories that are 8-, 16- or 32-bits wide and the DRAM controller accommodates memories that are either 16- or 32-bits wide. Memory can be added in 512-kbyte increments, a particular advantage for applications that don't require larger memory upgrades.

Intel (Santa Clara, CA), AMD's closest RISC competitor in the laser

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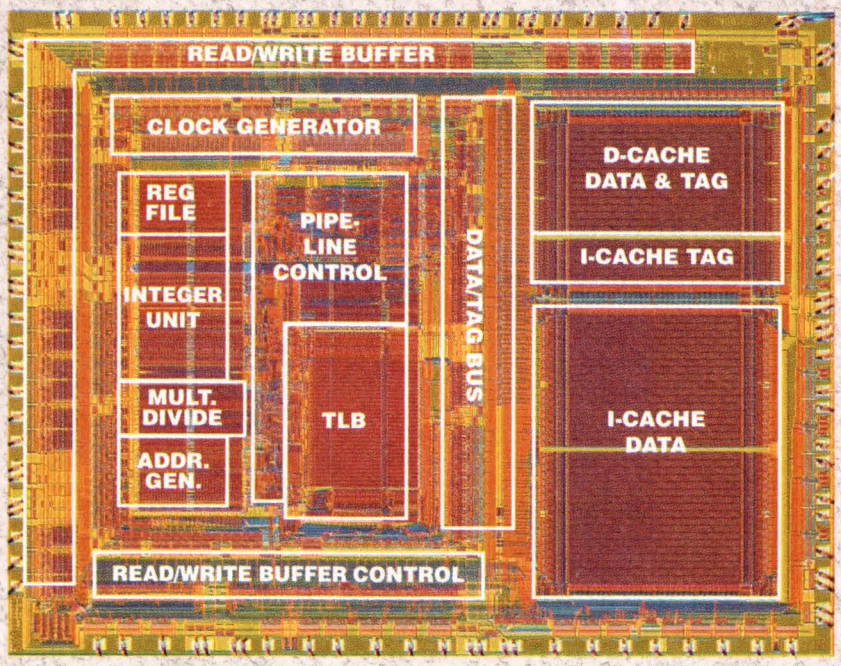

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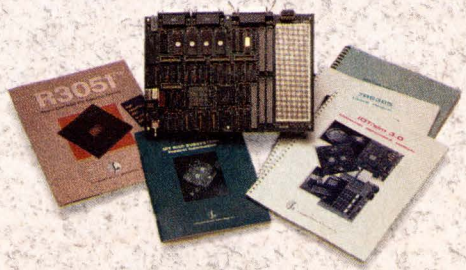

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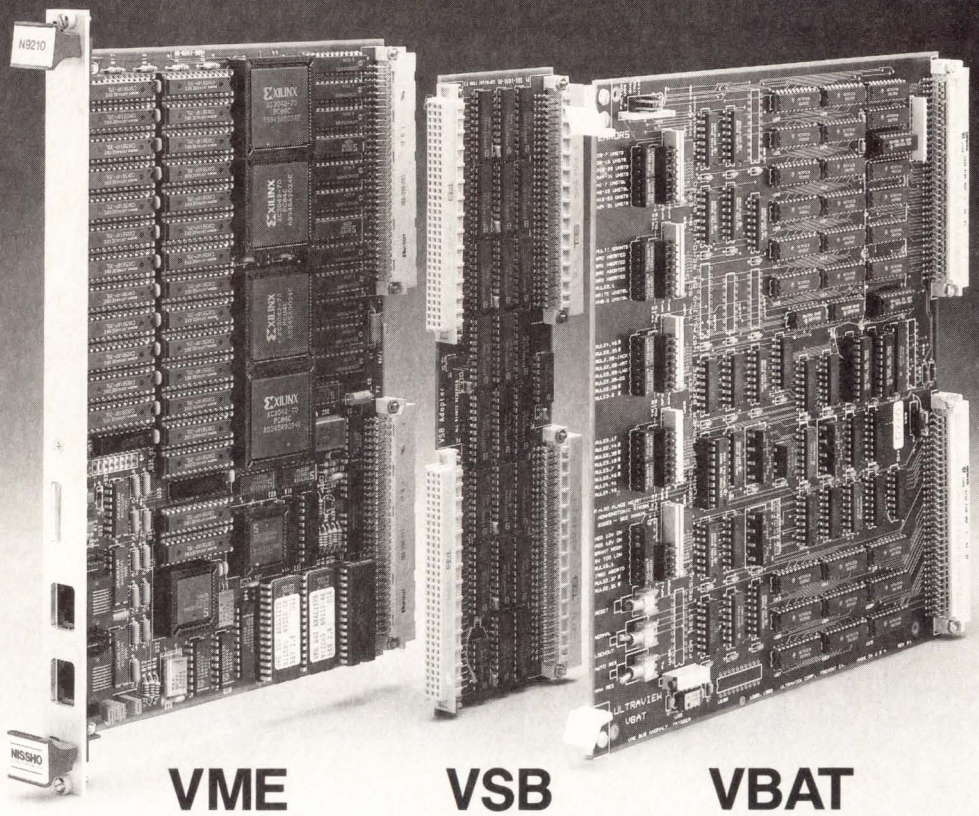

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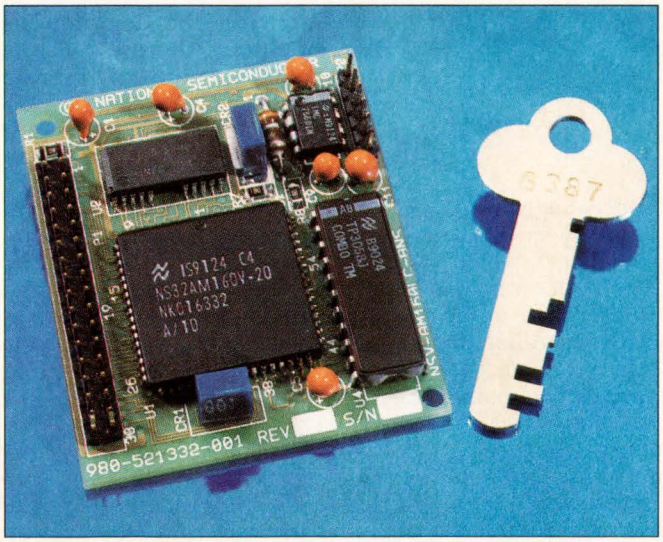

Smaller than a business card, this digital answering machine is based on the NS32AM160 voice processor from National Semiconductor.

printer business, offers an application-specific standard product (dubbed the 82961) to work with its 960KA and KB processors in laser printer designs, albeit at an additional cost of $20. Intel recommends designers use that chip if they need to incorporate common laser printer support logic, such as a DRAM interface, I/O interface and printer video interface into a design.

National dials in

Working in conjunction with AT&T, National Semiconductor has developed a RISC-based approach that's optimized for the control, compression/decompression and dual-tone multifrequency (DTMF) tasks found in DAMs. National's part, the 32AM160, integrates not one, but two processing cores on-chip in addition to system interface logic. What's more, support functions include a DRAM controller, interrupt controller, pulse width modulator, watch dog timer, and clock generator. ARAM memory and a codec (coder/decoder) are about the only external components needed to build a complete answering machine.

Three main tasks are performed by the 32AM160: system control, compression/decompression and DTMF detection. The system control includes user interface via keyboard and display handling. The chip also controls and monitors activity on the phone line, as well as keeping track of the time and detecting power failures. The voice compression/decompression task performs transformations between voice samples and compressed digital data. And it's the on-chip DSP that allows different voice algorithms, such as subband coding and LPC (linear predictive coding) to be implemented. The DTMF task monitors the incoming data to detect any DTMF signaling. DTMF signals are used as commands for the system control task, to change the current state of the answering machine.

X terminals, DAMs and laser printers are just a few of the applications RISC devices will target in their embedded form. Other applications for embedded RISCs include controllers for bridges, routers and brouters (bridge/routers) in LAN, wide area and metropolitan area networks now coming under the spell of RISC processors. ■

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SOFTWARE & DEVELOPMENT TOOLS

New emulator rounds out support for AM29200

Tom Williams, Senior Editor

The good news about software development tools for the Am29200 is there's not much news. Because the Am29200 is binary compatible with all other members of the 29000 family, almost all development tools in Advanced Micro Devices' (Sunnyvale, CA) Fusion 29K program will work unaltered with the 29200. The list includes a variety of compilers, debuggers and real-time kernels. The few tools specifically tailored to the Am29200's needs include evaluation boards, an in-circuit emulator and an architectural simulator.

Because the Am29200 incorporates on-chip peripherals such as the DMA controller, serial and parallel I/O ports, video interface, and peripheral interface adapter (PIA), it's not pin-compatible with other members of the family. This has necessitated changes in certain support items (e.g., the emulator) and production items (e.g., sockets).

C compilers and debuggers are available from AMD as well as from Corelis, Cygnus Support, Metaware, Microtec Research, and Multiprocessor Toolsmiths. The Verdix Ada Development System (VADS) by Verdix (Chantilly, VA) allows development in Ada and YARC Systems (Newbury Park, CA) supplies Fortran development support. Real-time operating system kernels and operating systems are available in the form of RTX RTOS from Accelerated Technology (Mobile, AL), the 29000 version of VRTX32 from Embedded Performance (Santa Clara, CA) and RealTime Craft RTOS from GSI Tecsi (Paris, France).

New emulator needed

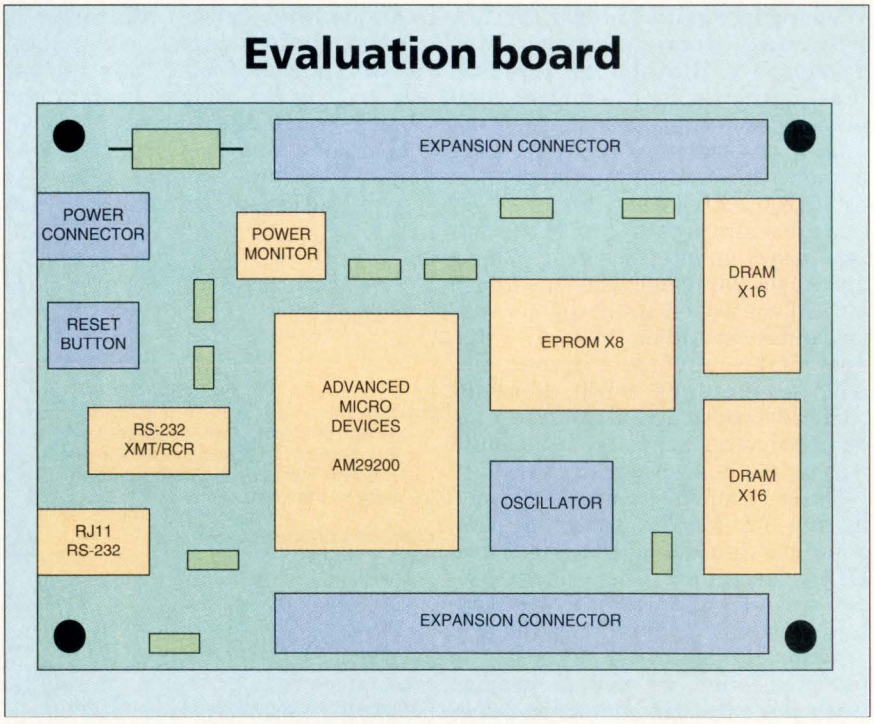
The most significantly different tool for the Am29200 is the SYS29K-Puma emulator from Embedded Performance (EPI) (Santa Clara, CA). In addition to the emulator, EPI is supplying some minor "tweaks" to its 29000 assembler and debugger to let the user monitor the additional on-chip registers and control lines. The changes are minor and will appear as a new revision number of the assembler/linker and debugger. At setup, the user will simply specify a switch to tell the debugger which member of the Am29000 family (29000, -05, -030, -035, or -200) he or she is working with. According to EPI president Norbert Laengrich, all customers who are on the maintenance program will automatically receive upgrades of the debugger.

But the in-circuit emulator "is a whole different situation," says Laengrich. Because the 29200 is unique in its pinout and what it incorporates on-chip, EPI has had to design a new model of the emulator. Changes include significant modification of some of the earlier emulator's firmware and a redesign of the target specific interface (TSI) board, which is internal to the emulator. The new model also includes a redesign of the two boards in the probe head—the buffer card and the overlay memory card "so it really is a new model," says Laengrich. For customers owning previous models of EPI's emulators, there will also be an upgrade or trade-in program available.

Because of the high integration of the 29200, however, the Puma will not support multiple versions of the 29000. The Puma emulator will let the user examine and modify all on-chip registers and target resources and set conditional hardware and software breakpoints, do conditional signal traces and optionally perform non-intrusive execution profiling and branch coverage.

JTAG to the rescue

Because many of the 29200's on-chip devices come between the external pins and the core processor, not all internal states are accessible in real-time. "Many of the things you normally did with the external pins with the emulator will now have to be done by JTAG interface," says Laengrich. The Joint Testing Action Group (JTAG) has specified a method of boundary scan testing to shift internal state information out of highly integrated boards and ICs where there's not direct access via external pins. This entails stopping the device and shifting out internal



The Eval29200 evaluation board available from AMD lets users immediately begin prototyping Am29200-based designs. An on-board monitor allows quick access by a debugger running on a host development system.

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SOFTWARE AND DEVELOPMENT TOOLS

state data. The emulator will allow a combination of real-time analysis and the ability to get to other state information via boundary scan.

There are those who are satisfied with logic analysis of external pins to verify their designs. For those users, there will be a preprocessor board available for the Hewlett-Packard (Palo Alto, CA) HP16500A logic analyzer. Hewlett-Packard will, according to AMD's marketing director for embedded processors, Subodh Toprani, support the disassembly of code via the attachment of the instruction bus on the part so that a logic analyzer can also read the instruction stream.

Almost all development tools in Advanced Micro Devices' Fusion program will work unaltered with the 29200.

In addition, AMD will be supplying two evaluation boards: the Eval29200 and the Laser29200. The first is a general-purpose evaluation board that contains the Am29200, 1 Mbyte of DRAM, a 256k × 8-bit EPROM, an on-board monitor and can be used with an optional expansion prototype board. The second evaluation board, the Laser29200, is oriented toward users who are designing laser printer controller applications. There also will be two simulation packages from AMD: one is an instruction set simulator, which is available now, mainly because it's the same for all members of the family, and the other is an architectural simulator. The latter will be available shortly and will specifically support the 29200 and its on-chip peripheral devices. ■

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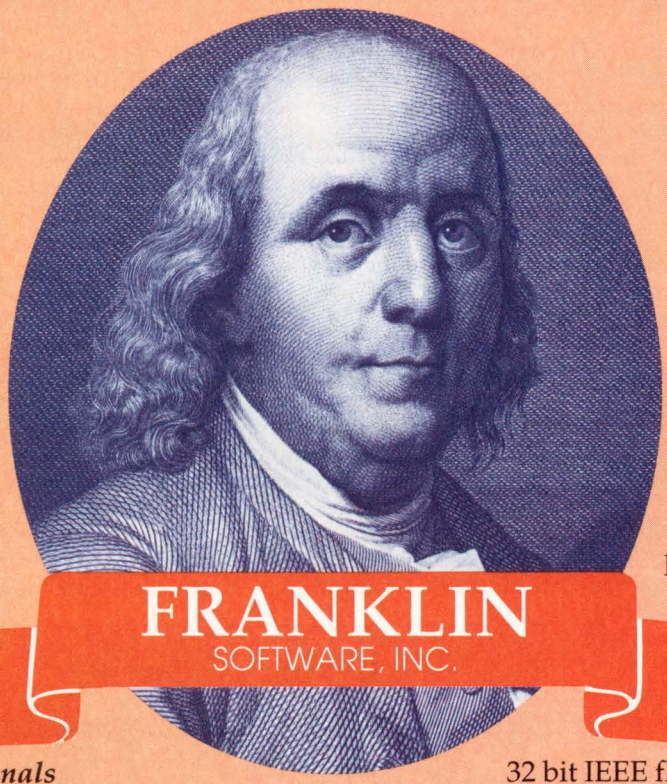

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COMPUTERS & SUBSYSTEMS

SCSI-3 to pick up where SCSI-2 leaves off

Warren Andrews, Senior Editor

The SCSI standard that ANSI approved in 1986 started the ball rolling for a standardized peripheral interface. But it was discovered early on that it fell short in a number of important areas. Almost before its approval, therefore, work had already begun on the next revision, SCSI 2. That document is now complete and has passed all the obstacles for final approval, expected later this year or early next. "SCSI 2 represents a lot of cleaning up and added capability to the initial specification," says Anthony Kozlowski, product manager for NCR (Colorado Springs, CO) and the originator of SCSI.

Despite its bulk of some 600 pages, it looks as if it, too, will fail to meet all expectations and discussions about SCSI 3 have already begun. Even before such a document emerges, some significant de facto changes, such as cabling, connectors and termination, are expected to occur. In addition, the next generation will start dealing with such things as serial SCSI and perhaps even a fiberoptic version.

Much of the SCSI 2 document deals with support for a wide variety of devices. "Traditionally," says Kozlowski, "SCSI has been thought of as a disk drive or tape drive interface. And while the standard certainly addresses those areas, it also provides support for such things as optical devices, printers and communications devices. In fact, the bulk of those 600 pages—some 570 pages—talks to software changes in SCSI, such as how to execute commands and which commands to execute."

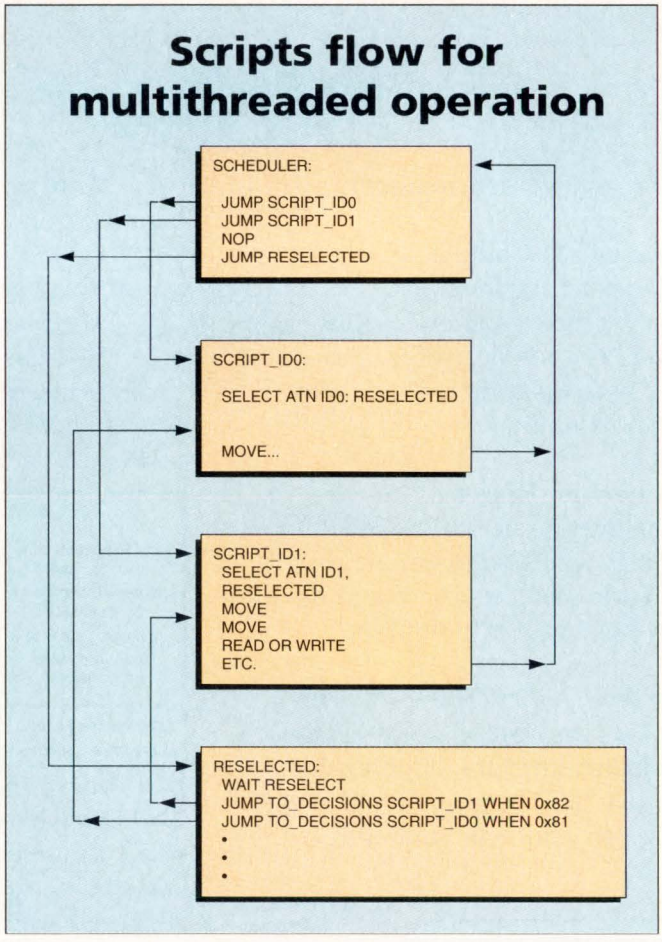
"Only 30 pages of the SCSI 2 document," says Kozlowski, "deal with the physical interface of SCSI—connectors, cables, terminators, and all the other things required to connect what is the SCSI bus." Despite the fact that less than five percent of the document talks about physical interconnect, there's a tendency to think in terms of hardware changes. "There's a perception that SCSI 2 offers only two options: fast and wide." Kozlowski notes that these hardware changes will probably be among the first to be modified as the committee moves toward SCSI 3.

Flexible solutions emerging

"There are just now a number of chips coming available addressing both wide and fast SCSI," says Kozlowski, "but the physical implementation may not conform too closely with that in the SCSI 2 document." Kozlowski points out, for example, that the initial idea behind wide SCSI was to have full compatibility with the earlier SCSI 1 implementations. This calls for a dual-connector configuration—one 50-pin connector as in SCSI 1, and a second, 68-pin high-density connector.

While the two-connector solution maintains compatibility, it causes problems with small-profile peripherals. For example, 3.5-in. disk drives barely have room for a single connector, not to mention two. "In an effort to get the SCSI 2 specification out the door," says Kozlowski, "it was decided to let the two-connector solution stand." But in the final analysis, very few manufacturers—and no major developers—are using the two-connector approach. In some cases, where they have control of both ends of the connection, SCSI developers have vied for proprietary approaches. But in most cases, they've remained with a "narrow" SCSI definition.

The definition of a single-cable, single-connector 16-bit SCSI is already on the table among those discussing SCSI 3. But that may not be quite enough to satisfy drive makers. Manufacturers making 3.5-in. drives may have problems accommodating even a single, high-density connector for 16-bit SCSI. As a result, it appears that serial SCSI is getting more attention. And



SCSI Scripts make it easy to have more than one task active at a time. The main driver running the host computer keeps track of I/O requests in a table or scheduler. Each time an application program requests a new I/O instruction, the main driver enters a Scripts Jump instruction into the scheduler. Each time an I/O is completed, the main driver replaces the I/O request with an NOP instruction.

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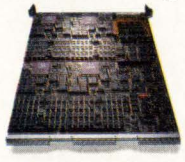

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CIRCLE NO. 33

COMPUTERS & SUBSYSTEMS

Writing a Script for SCI implementation

The growing sophistication of operating systems, particularly the implementation of multithreaded SCSI I/O operations, places extra demands on SCSI I/O subsystems. Efficient operation in a multithreaded environment requires fast context switching, efficient scatter/gather operations and the ability to perform host processor-to-SCSI processor communication without interrupts, preferably via mailboxes or semaphores.

The ability to make complicated phase sequence decisions at the hardware level requires flexibility and some intelligence. Earlier generations of chips (for example, the NCR 53C90) had some decision-making ability at the hardware level, but weren't able to handle complex or unique sequences without processor intervention. To solve the problem, NCR developed its SCSI Scripts programming language. The approach was designed to simplify the SCSI designer's steep learning curve and has been implemented in the company's 537XX family of SCSI controller chips. But Scripts is NCR's native programming language, specific to its family of SCSI processors, just as 80386 assembly is the native language of the Intel 80386 processor.

There's a direct, one-to-one correlation between the SCSI protocol and SCSI Scripts to allow the handling of any SCSI requirement. Scripts instructions are divided into five classes: I/O, block move, transfer control, register read/write and memory-to-memory move.

Because unique phase sequences require the ability to branch arbitrarily within the Scripts program, the processor can't merely buffer a linear sequence of commands. The Scripts processor can fetch instructions directly from the RAM memory. To eliminate constraints on the size of the Scripts code, system memory is used to store Scripts programs, instead of an on-chip buffer or a dedicated external memory (although such a memory can be supported).

The Scripts concept also solves the problem of frequent interrupts to the host CPU. A typical nonintelligent SCSI controller requires an interrupt every time the SCSI bus changes phases. Not only does this contribute to the protocol overhead, but it robs the CPU of valuable processing time. NCR's approach allows the processing of multiple I/O operations completely without interrupts as long as there are no errors. Hardware errors such as DMA bus faults and SCSI timeouts still result in an interrupt.

it's likely that as even smaller drives become available, it's possible that a serial interface will become even more critical.

Wider may not be the answer

"Increasing the transfer rate of SCSI will continue to be an issue," says Kozlowski, "but making it wider and wider may not be the answer." The solution will be to adopt some kind of serial protocol that will save some of the software investment companies have made in SCSI, but that will actually implement the protocols through some kind of serial link such as a fiber channel. "But it's probably not going to happen tomorrow," adds Kozlowski. "If the last document is any indication, it may be some four to five years before we see SCSI 3 start to reach maturity."

But SCSI 3 will probably not be the same as earlier-generation documents. In SCSI 2, the committee generated a massive 600-page document covering all aspects of the specification. In future versions, different areas will have their own documents. The new approach will be like the Futurebus+ specification with separate logical, physical and implementation specifications (896.1, 896.2 and 896.3). There will be separate specifications for physical implementations and for protocols, both parallel and serial.

It's expected that a single-connector-wide SCSI will be among the first of the new specifications. "In fact," says Kozlowski, "chip makers such as NCR have anticipated this development in the design of SCSI 2 silicon. NCR's 53C720, for example, is designed to implement all SCSI 2 options, but has been designed to operate with a single request acknowledge signal and, therefore, will operate only in a single-cable implementation. Other chip makers," adds Kozlowski, "are doing much the same."

Kozlowski is quick to add that NCR also makes a SCSI 2-compatible chip with dual request acknowledge signals. This chip is offered as part of the company's Raid (redundant array of inexpensive disks) chip set and is, therefore, compatible with dual-cable systems. "Wide SCSI is just now starting to take off," he says, "and it's expected that there will be many single-cable implementations over the next several months."

Raids

One of the driving factors for a wider bandwidth SCSI has been the recent activity on the Raid front. From a hardware point of view, all Raid implementations suffer from limitations in their interface bandwidth. Today's disk drives operate at about 3 Mbyte/s or better. The difficulty in Raid's approaches is that four or five such drives operating together yield a data stream of somewhere be-

tween 15- and 20-Mbyte/s. Traditional SCSI can't keep up. SCSI 1, at 5 Mbytes/s, won't make it. It's necessary to go to all wide and fast SCSI 2 options to keep up with such an array.

"NCR offers two Raid boards," says Kozlowski, "one with a fast SCSI operating at 10 Mbytes/s, the other incorporating both wide and fast SCSI providing transfer rates up to 20 Mbytes/s." While Raid doesn't require SCSI, the bandwidth is attractive to a Raid developer.

"From a software standpoint," says Kozlowski, "there are also expected to be some interesting developments." SCSI 2 doesn't have a command set for Raid. While its command set can address individual drives within such an array, it doesn't address the array itself. "What manufacturers such as NCR are doing is use the disk-drive command set to address the array as a single drive and perform necessary functions, such as disk striping, separately," he says.

"Operationally it's possible to run that way," says Kozlowski, "but when you start running diagnostics and other special things you have to do in a Raid setup, that starts to fall apart. There's really incomplete support for Raid in SCSI 2. And I'm not sure that these will even be addressed in SCSI 3." Kozlowski says, however, that NCR and others have developed what the SCSI community calls "vendor-unique" commands to handle some of the special needs of Raid systems. "There's an opportunity to do something that may be a common command set for Raid," he adds.

SCSI was originally designed to be a universal peripheral interface. Until recently, though, it has remained almost exclusively a medium for interfacing disk drives. With the enhancements already introduced and those on the way, however, a number of device vendors are beginning to give serious attention to SCSI as a broader communication medium for everything from printers and scanners to modems and other communications equipment. In fact some manufacturers are even using SCSI in a specialized LAN approach. ■

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CIRCLE NO. 36

CAE/CAD TOOLS

Boundary scan makes inroads into PCB testing

Mike Donlin, Senior Editor

As designers push printed circuit board (PCB) performance to the limit with advanced IC packaging, traditional test methodologies become ineffective. Bed-of-nails testers are useless with the fine pitches of surface mount devices and multichip modules (MCMs), but designers must use these packaging techniques to keep their products competitive. The answer to this evolving dilemma is boundary scan technology which potentially lets PCB designers put test electronics into every pin of a board's components. Though boundary scan isn't new, only recently has a standard emerged—IEEE 1149.1—that lets IC designers, PCB designers and automatic test equipment vendors speak the same language. But while the concept of boundary scan seems like an idea whose time has come, there are challenges that await anyone deciding to use it.

From an IC designer's viewpoint, boundary scan exacts a real estate penalty which can affect a device's performance. And though IEEE 1149.1 only uses four I/O pins to operate, some IC designers are reluctant to give up any silicon or pins for testing. But as concurrent engineering becomes a reality, the needs of test will invade the domain of the design engineer and boundary scan, both at the IC and PCB level, will become a necessity.

This transition can't come a moment too soon for ATE vendors who have seen the market for their high-priced, bed-of-nails testers dry up over the last few years. Boundary scan circuit boards will give them a new market in which to peddle their wares, if PCB designers and test engineers can be convinced that boundary scan is worth its salt.

"I think in about five years or so, boundary scan will be the dominant test methodology," says Peter Lwin, product marketing manager at Schlumberger Technologies (San Jose, CA). "It will be an evolutionary process though, while IC vendors incorporate boundary scan into their devices and board designers learn how to take advantage of boundary scan capabilities."

For ATE vendors such as Schlumberger, the biggest challenge is developing software to analyze the complex tangle of signals that come from a host of boundary scan devices on a circuit board. Currently, boundary scan software can pinpoint open and shorted circuits and "stuck at" faults. This basic level of testing can target manufacturing faults, but stalls out at isolating design problems, that is, making sure that the array of ICs on a PCB are performing according to plan. "The fact that ASIC designers have been using boundary scan for years makes it look like it's easy to adopt," Lwin points out. "But at an ASIC level, a designer just has to verify the behavior of an isolated part. When a board designer has to piece together the behavior of the various devices—standard parts, ASICs, boundary scan, and non-boundary scan ICs—things get a lot more complicated."

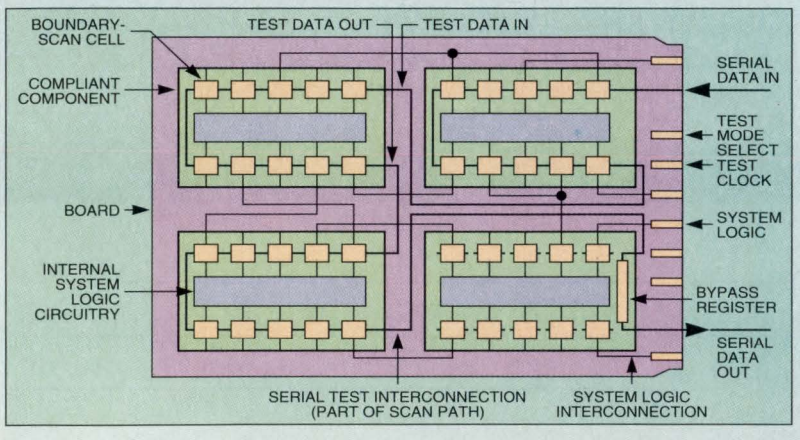
Making connections

In addition to getting ATE to unravel the complexities of IC behavior, testing the interconnecting circuitry for each device also poses a formidable challenge. "There are four basic ideas behind boundary scan interconnect testing," says Gordon Robinson, senior staff scientist at GenRad (Concord, MA). "First, a sequence of patterns is applied to the nodes, one pattern at a time, such that each node should see a different sequence. The sequence acts as identifier to the node. Second, each pin or significant point connected to each node is sensed. Third, an open is detected if any sense point fails to return the same identifier as another sense point on the same node. Finally, a short is detected if any sense point returns the same identifier as a sense point on a different node."

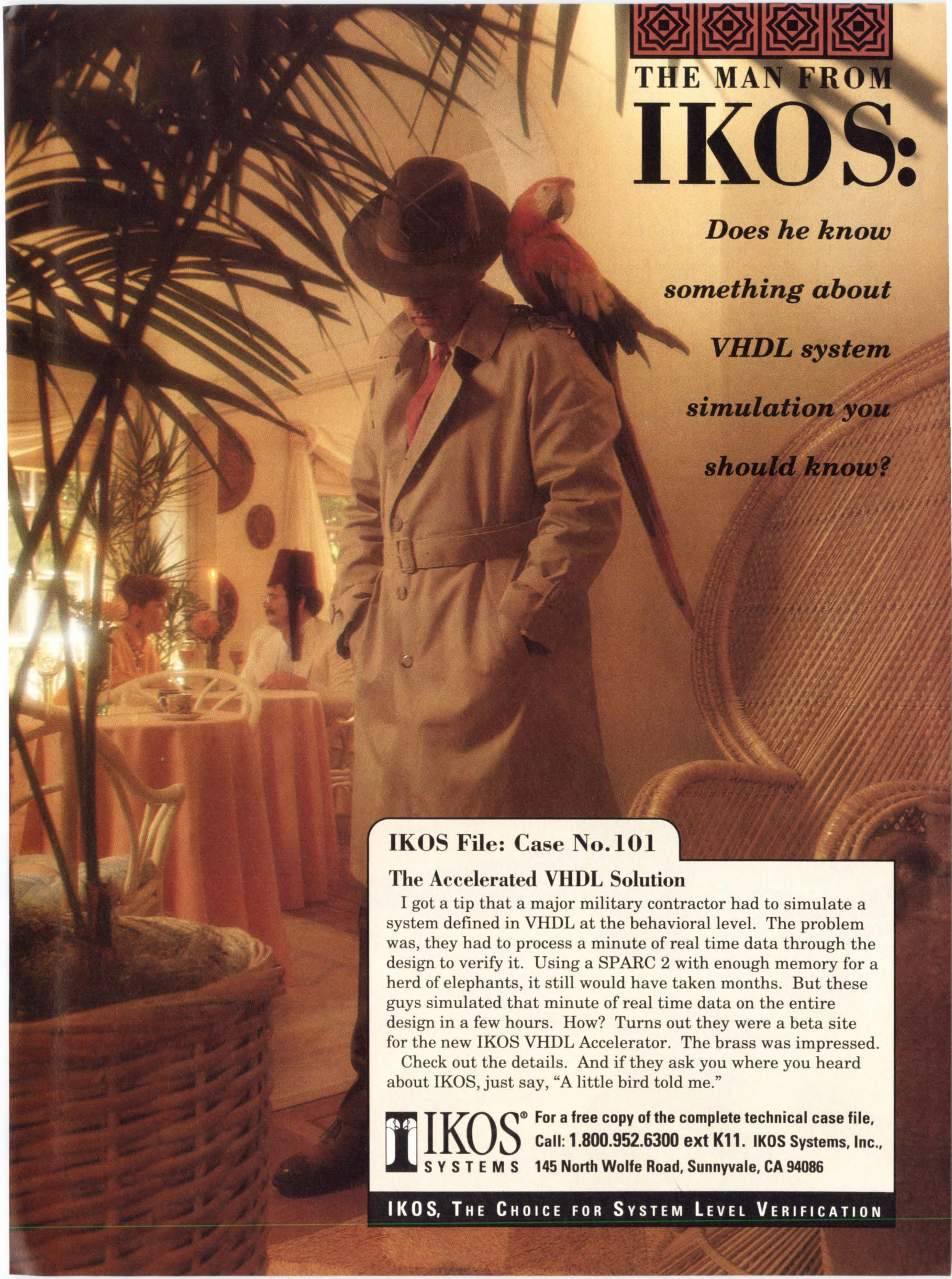
Interconnect diagnosis requires a complicated test strategy, Robinson explains, because it requires software features not commonly found in digital testers. In particular, the tester needs the capability to analyze a mass of fault data in the software, rather than relying on a fault dictionary. Correct diagnosis may require software to construct special test patterns depending on preliminary findings in the analysis.

In spite of these difficulties, ATE vendors are working furiously on the software and hardware capabilities that will let them hop on the

A boundary scan PCB



The Bypass instruction, a mandatory requirement for IEEE 1149.1 compliance, selects the Bypass register so that the serial data path (bypassing all other test data registers) is as short as possible. Using this instruction for each component whose testability features are not being used, minimizes the scan path length across the board, saving time. The Bypass instruction makes the component behave as a single-stage shift register.



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boundary scan bandwagon. And to ensure boundary scan's acceptance, these vendors are promising improved PCB quality and fewer problems in the field.

"While it's true that good component testing results in fewer bad ICs being placed on circuit boards, our research shows that structural faults dominate as reasons for PCB failure," says Peter Hansen, engineering manager of the assembly test group at Teradyne (Boston, MA). "Those structural faults occur mainly at device pins. Even in field returns, structural faults outnumber performance failures."

Evidence that structural faults lie at the heart of PCB failure has pushed companies such as Teradyne to develop software to generate boundary scan tests for their ATE systems. The latest version of Teradyne's Victory software—Version 2.0—features two new software modules, one for testing non-boundary scan circuitry which lacks bed-of-nails test access, and the other for testing the internal circuitry of boundary scan devices.

Software, of course, is only part of the equation. The hardware portion of the tester market must also follow the transition to fully populated boundary scan PCBs. This means having a combination boundary scan and non-boundary scan tester at the ready. GenRad's GR2288 combinational board test system is an example of a tester trying to stay in touch with the multiple facets of the evolving PCB market. According to GenRad, the GR2288 can execute all types of testing—continuity, in-circuit, functional, and cluster testing, as well as mixed-signal, internal and boundary scan testing. Being all things to all designs presents challenges to ATE vendors, especially when they try to keep the notoriously high prices of their systems down.

"We've implemented a technique that lets us test both types of devices—boundary scan and non-boundary scan," says John Deshayes, software development engineer at GenRad. "But in general, manufacturers of PCBs aren't convinced that boundary scan is worth the effort, so we have to provide capabilities for all types of test."

If boundary scan is to win full acceptance of the design community, then it must be able to prove its worth without a significant amount of investment for board manufacturers. Products at the less expensive end of the test spectrum might aid in this acceptance. John Fluke Manufacturing (Everett, WA) hopes to encourage the use of boundary scan with the latest enhancement to its line of logic analyzers. The PM 8660/30, an automatic test program generator and boundary scan option for Fluke's PM 3580 family of logic analyzers, lets users debug proto-

How well does Texas Instruments support

type boards with boundary scan technology. The package tests for opens, shorts, bridges, and also supports cluster testing. In addition, a bus analyzer option simplifies debugging IEEE 1149.1 hardware and software problems.

Seeing is believing

The availability of boundary scan test capabilities at the bench level will undoubtedly fuel its acceptance, but old habits die hard. "Even though boundary scan solves a lot of problems, you still need a way to provide real-time tests," says Bob Roth, product marketing manager for logic analyzers at Fluke. "After all, a lot of test engineers are still hands-on types who trust proven methods. We think it's possible, in the future, to have real-time test and boundary scan integrated and synchronized. From a hardware point of view, it isn't that hard. But getting the software to provide for both scenarios and incorporating it into one piece of equipment is a real challenge. But boundary scan will be adopted. After all, if circuit board designers don't use the smallest, densest packaging technology, they won't be competitive. And if they ignore testing issues completely, they'll produce a board whose quality can't be verified. The decision to use boundary scan will be a given over time."

■

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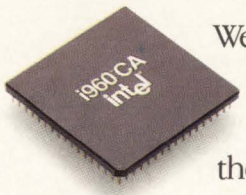

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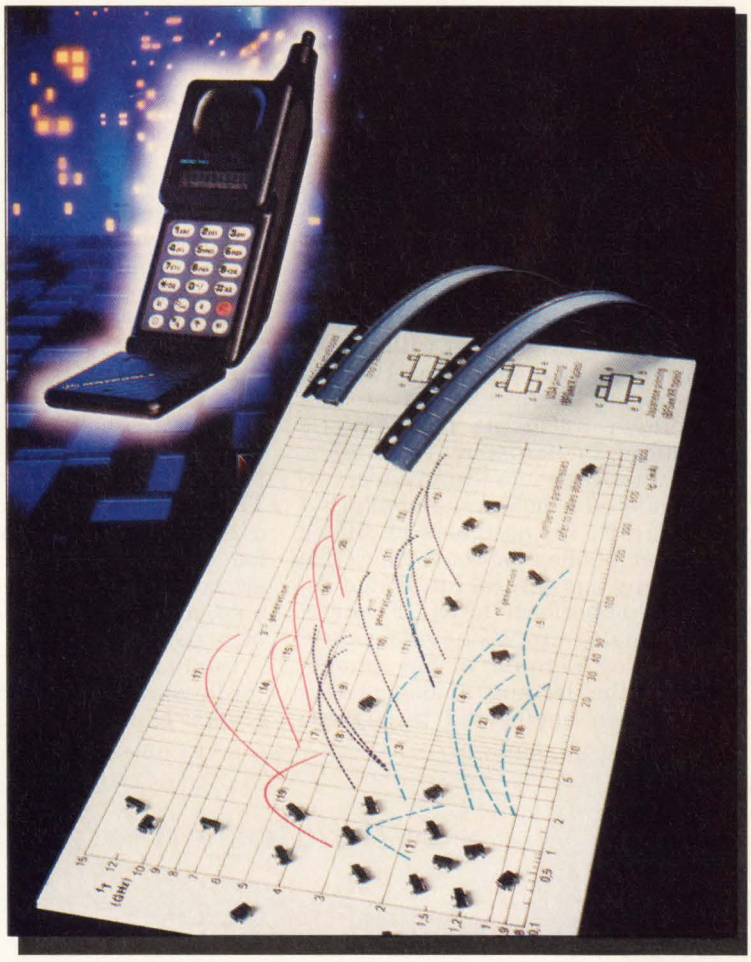
CIRCLE NO. 39

Cellular phone designs call for mixed-signal solutions

Chip vendors are addressing the mixed-signal needs of cellular phones. The result will be a single-chip cellular solution that may also find a home in wireless communications for personal computers.

Dave Wilson
Senior Editor



Discrete components, like those shown here from Philips/Signetics, are still used in the RF section of digital cellular phones. But future integration plans by all the major IC houses may result in a single chip that handles not just the RF, but all the functions in a cellular phone .

Chips and Technologies changed the face of the computer industry when it gave designers the ability to build personal computers from a handful of chips. Now, a host of semiconductor vendors are hoping to do the same for "the personal communicator," whether it takes the form of a cellular phone, a cordless telephone or a wireless LAN communicator. While many Japanese and U.S. telecom manufacturers may still build proprietary communications chips at their own foundries to gain a price/performance edge in these markets, smaller communications companies will profit greatly from standard off-the-shelf cellular silicon and/or gallium-arsenide solutions. So, too, will chip vendors such as Analog Devices, AT&T Microelectronics, GEC Plessey, National Semiconductor, Philips/Signetics, Sony, and Texas Instruments that can muster the expertise to build chip sets to meet the market's needs.

A mix of challenges

Building cellular phones represents one of the final frontiers of mixed-signal design. Designers must work with analog radio frequency components operating in the GHz range, as well as digital signal processors in the MHz range. As a result, they must familiarize themselves with a number of different technologies. They must also be extremely conscious of power consumption issues. Lastly, since the product is a consumer item, being competitive in price is especially important.

Designers must also keep an eye on the standards front (see "Standards

make it happen," p 60). Things aren't clear cut here. For one, the U.S. and European marketplaces abide by different communications standards. Worse, in some applications such as digital telephones, standards haven't been set and committing to a design before they are may put the success of the product (and possibly the designer's job) in jeopardy.

Despite nuances in design and manufacturability, all phones must perform the same function; that is, transmit and receive voice signals. Simplistically, an analog cellular phone has five major functional blocks: an RF receiver, an RF transmitter, an audio processor, a microcontroller, and a power supply.

Analog phones must support full duplex operation—the transmitter and receiver must be on at the same time. Hence, "analog phones require very good signal filtering to stop the transmitter interfering with the receiver," according to Jon Hudson, European linear telecom product manager at Texas Instruments (Bedford, Bedfordshire, England).

Philips/Signetics (Sunnyvale, CA) has offered a mixed-signal chip set specifically for designers of analog cellular phones for some time. The company has several integrated devices that perform the RF/IF conversion, analog processing and control of analog signals in the phone. Today, the leading analog phones have been engineered through so many iterations that just one analog processor is all that's required to process the analog baseband signal. Notably, most phones still have a separate printed circuit board (PCB) for the RF section. That's because the filters in the IF transmitter and receiver sections of the phone take up a lot of room and a discrete approach is still taken for much of the RF circuitry to keep costs down.

Advantages of digital

Despite the popularity of analog cellular phones, the move to digital cellular networks and digital telephony is well underway. The motivation for the move comes from the telephone system operators themselves. The operators have two main problems: the first is the lack of capacity in urban regions where there just isn't enough bandwidth in the analog system to support the demands on the system; the second is the quality of the technology. Analog phones suffer badly from multipath fading, as well as problems in cell handover.

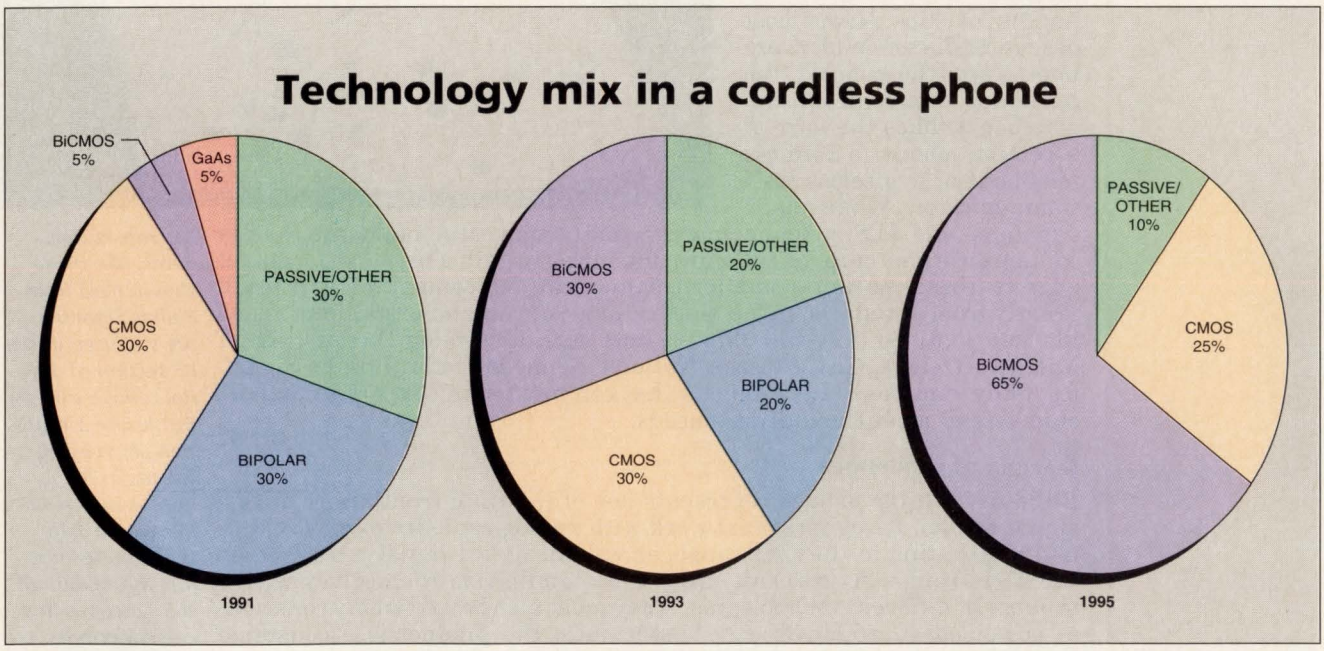
"Digital phones are more spectrally efficient because they employ time division multiplexing," says TI's Hudson. "You can also use a lot of error correction to overcome problems with fading. Better yet, you can actually lose fractions of a second of a speech signal and still recover it," he adds.

Compared with analog, digital cordless and cellular phones offer a greater bandwidth and higher quality transmission and reception because of error correction. They also have an advantage because they can embrace security features such as voice encryption and frequency hopping.

The strategies that Analog Devices, AT&T Microelectronics, National Semiconductor, Philips/Signetics, Texas Instruments and the rest of the chip vendors are taking toward building silicon for digital cellular phones are very similar. All are working with a few large customers to optimize the DSP, RF/IF and power chips for the specific requirements of the market. Most likely, the resulting silicon (or GaAs!) won't be all that different. That's because there's no getting around the basic functions that need to be performed by a digital cellular phone. According to Peter Ehlig, member of the technical staff at Texas Instruments (Houston, TX), a basic digital cellular phone system comprises just a few functional blocks.

How they work

Predictably enough, processing in a digital phone is performed digitally. The speech from the microphone is digitized by an A-D converter. An D-A converter on the output side reconstructs the voice and outputs the result to a speaker. Interestingly enough, neither the A-D nor the D-A converters need to meet very stringent specifications. The European Groupe Speciale Mobile (GSM) cel-



Today, a cellular phone makes use of a number of different technologies—some expensive. By 1995, the aim is to bring down the cost of the phone by manufacturing the bulk of the radio frequency/power devices in BiCMOS, and the digital logic in CMOS.

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Communication protocols govern the way a cellular phone call is established. In the United States, the Advanced Mobile Phone Service (AMPS) is the analog cellular system in use. It uses analog frequency modulation from 824 to 849 MHz and 869 to 894 MHz for transmitting voice and data. In Europe, each country has its own analog standard and each works on different frequencies.

Nevertheless, there are two standards which are firmly supported (with frequency allocation) by the European community. The first is the 900-MHz Groupe Speciale Mobile (GSM) digital cellular system. The second is the 1.9-GHz Digital European Cordless Telecommunications (DECT) system. The European Telecommunications Standards Institute (ETSI) had originally announced that GSM would be operational in major European metropolitan areas by July, 1991. But, the GSM schedule has slipped; some say because the network is not in place, others blame it on the lack of handset availability. The DECT standard is still being finalized by ETSI, and will be available toward the end of this year. The commercial rollout of DECT (expected in early 1993) is initially intended for PABX use, and later for Telepoint and residential applications.

In North America, the Telecommunications Industry Association (TIA) has established the IS-54 standard for digital cellular systems. This system will "share" the frequency allocation that AMPS uses today (i.e., analog channels will be converted to digital, based on the need for increased capacity in specific geographic areas). These phones will be dual mode—working in either digital or analog mode. IS-54 will offer a three-fold, and then a six-fold (with a half-rate codec [coder/decoder]) increase in subscriber capacity compared to analog. The IS-54 standard is based on a Time Division Multiple Access (TDMA) method, but there have been proposals suggesting that Code Division Multiple Access (CDMA), a spread-spectrum technique, may offer greater capacity.

A short-term solution for analog cellular capacity problems has been tested by Motorola and dubbed Narrow-band AMPS (NAMPS). NAMPS uses the same frequency bands as AMPS, but rather than using a 30-kHz channel spacing, only 10 kHz is required. This promises a three-fold increase in capacity over AMPS, but network operators installing the NAMPS upgrade may still be forced to move to digital to satisfy subscriber demand for air time. Motorola's new MicroTAC II (see pg 57) is claimed to support both NAMPS and the AMPS standard.

luar standard, for example, doesn't have very tight converter specifications—a 10-bit converter with a sample rate between 8 to 20 kHz and a conversion time of less than 15 μs is all that's required. Not surprisingly, vendors like Analog Devices (Norwood, MA) with its ADSP-21MSP50 and AT&T Microelectronics (Berkeley Heights, NJ) with its DSP16C, have incorporated the A-D and D-A functions for the speaker and microphone onto the DSP chip to reduce component count and lower system cost.

Unlike the converter, the DSP inside the phone must be a high-performance engine that consumes little power and be housed in a miniature package. These considerations, coupled with cost concerns, point to the use of a 16-bit fixed-point device. Once speech data has been processed, it's sent from the processor to a modem where it's modulated. Another set of converters convert the digital signal back to analog where it's fed to a linear RF subsystem which transmits the radio signal.

Clearly, the industry trend is to produce a highly integrated, inexpensive phone solution, where just a few chips—a DSP, an RF/IF chip and a power amplifier—are all it takes to perform the functions involved. But before it becomes a reality, several things need to happen. First, DSPs must become better at solving some of the very application-specific problems involved in mobile phones, such as speech compression, equalization and echo cancellation. In addition, if costs are to be reduced, those DSPs may need to be tailored (perhaps as standard cells) to meet the specific algorithm demands of individual cellular standards more effectively while addressing the power and packaging issues. Second, IF modulator/demodulator stages must be capable of working at higher frequencies. And, finally, on the power output side, power transistor technology must become more efficient.

The DSP inside the phone performs many functions—equalization, speech compression, I/O control of the signal, signal refining, echo cancellation to eliminate the multipath reflections in the RF loop, and noise filtering, as well as the digitization and regeneration of an audio signal.

To determine the processing mix, researchers at Philips/Signetics performed a performance estimation of the computational load on a DSP in a cellular GSM application while designing their latest PCF5080 DSP. They showed that 35 percent of the processing power of the Philips/Signetics device is used to perform the equalization function. The second most computationally intensive areas are the speech and channel codec (coder/decoder) functions.

Channel coding is performed by the DSP to interpret the control information sent from the base station to the phone to indicate which frequency has been allocated for transmit and which for receive. "When you're in a time division multiplexed mode (for IS-54), you're looking at a 30-kHz wide channel of data that's divided into three time slots. The DSP must decode the information out of the time slot pertinent to the call," says Scott Erickson, manager of market development for celluar systems at AT&T Microelectronics. Error correction and equalization are then applied to the signal to overcome problems associated with momentary loss of signal path. That data is then sent to a speech coder—a function also performed by the DSP. All this so that a clean set of digital data can be converted and sent to the speaker in the earpiece.

Shiv Verma, president of Verma Labs (Woodbridge, NJ), a design house specializing in celluar communications, currently uses multiple processors in his designs. He feels that it's difficult today for just one DSP to handle all the processing functions in a hand-held phone. And, ultimately, he thinks that the most cost-effective approach in processing will be to use a custom DSP design rather than an off-the-shelf solution. "We will certainly use custom DSP, although at present we're currently using off-the-shelf," he says.

Some core solutions

But there may be problems with going with a fully custom approach too early. It's because of those reasons that, at the present time, AT&T is

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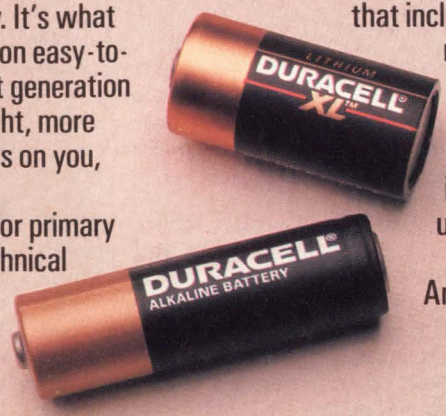

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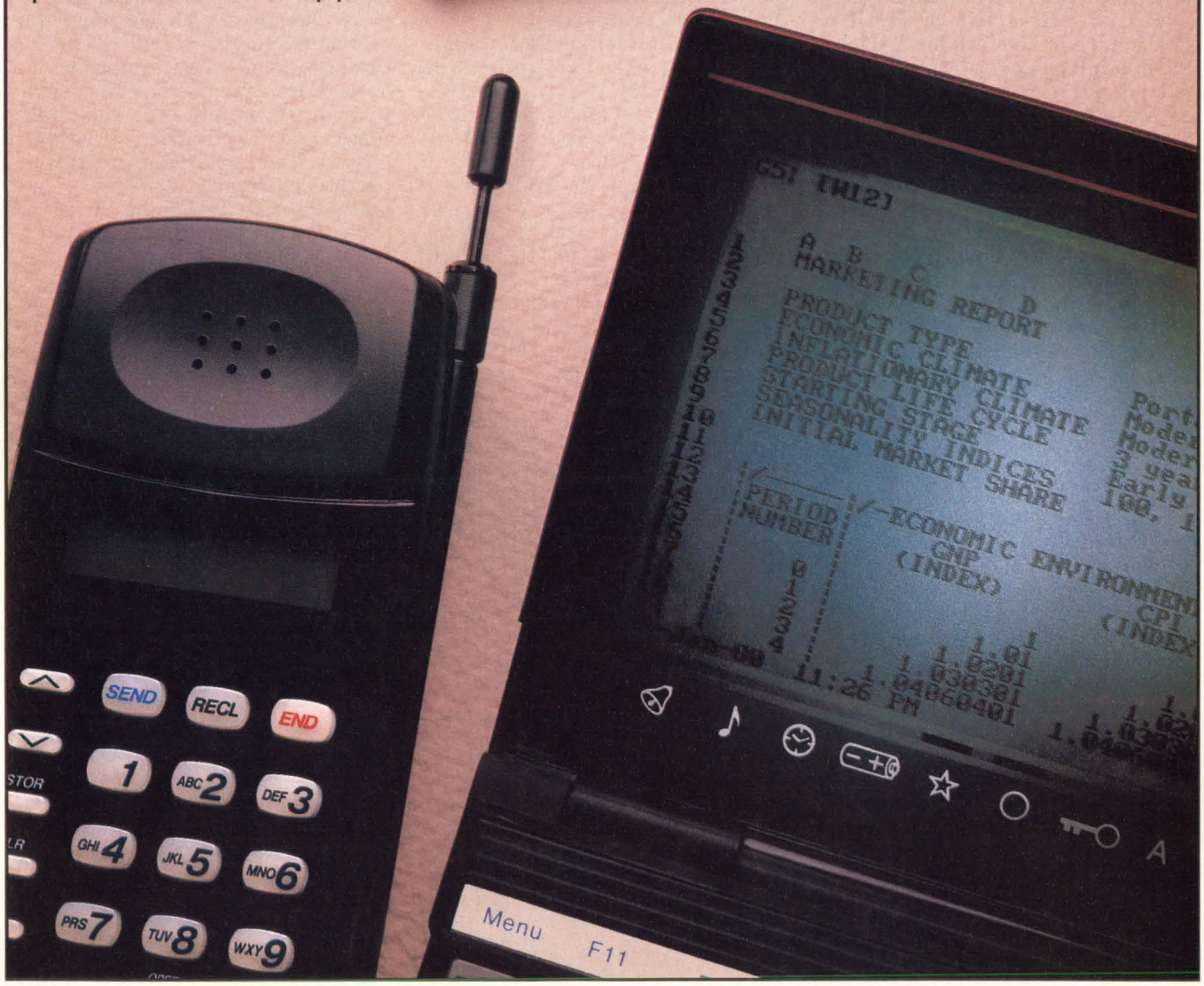
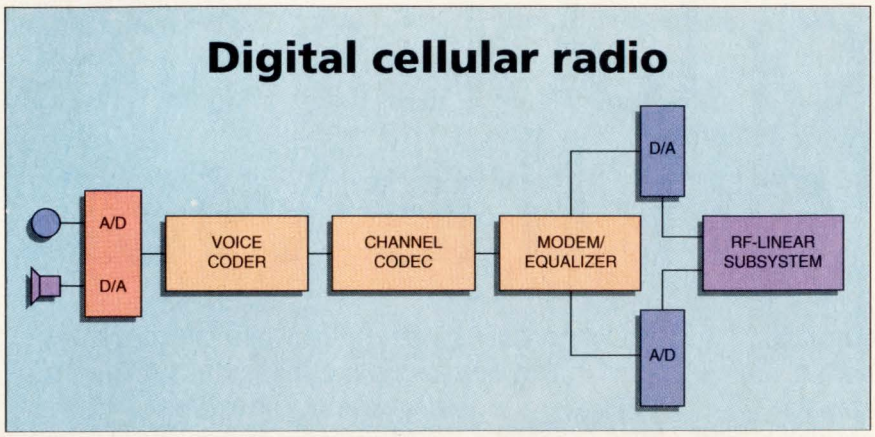




The basic building blocks of a cellular telephone include voice converters, a voice coder, channel codec, modem/equalizer, more converters, and a radio frequency subsystem. The functions of voice and channel coding, as well as modem equalization, are performed with a digital signal processor or an ASIC.

offering application-specific programmable DSPs based on its core technology for the processing of signals in the baseband section. "You could take a hard-wired ASIC approach, but not before communications standards stabilize," Erickson says. Indeed, Erickson thinks that it will be at least a year or so before designers are comfortable with designing full custom silicon. "You can get a minor cost savings, at best," he says. And since DSPs are beginning to find their way into high-volume products, a process already driving down cost, Erickson isn't convinced that it may ever be feasible to move away from a fully programmable approach to a custom ASIC approach; rather that the DSP will be integrated with custom ASIC logic. "When we start to manufacture DSPs on our 0.5μ fabrication process, we will be pushing 60 Mips on a single device at 60 percent of the power required today. Hence, one DSP will be adequate to execute all the algorithms in a digital cellular telephone," he adds.

While others have standard DSPs targeted at this kind of application, TI is offering more of a configurable solution with its core DSP (cDSP) technology. "The idea is to make it easy to use the TMS320 but optimize it for applications. You can optimize the device for power consumption as well as retain your investment in software," TI's Hudson says. Clearly, using TI's approach, designers could craft custom processors that sport not only A-D and D-A converters on-chip, but other algorithm-specific application accelerator blocks as well.

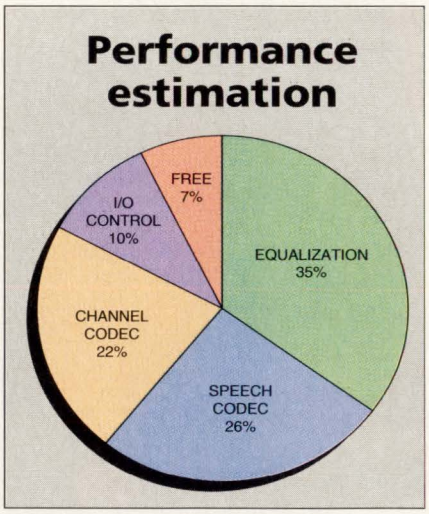
AT&T's Erickson says that his company looked at the algorithms required to perform the equalization, channel coding and speech compression (compressing 64 kbit/s of speech down to 8 kbits/s for IS-54 U.S. digital and to 13 kbit/s for GSM European digital), as well as the type of instructions that were required by the DSP before setting out to build a processor for mobile phones. "The result was an application-specific programmable DSP—the DSP1610/DSP1616—whose instruction set was optimized to handle these types of signal-coding algorithms." Erickson notes that while the IS-54 speech coder running on the earlier DSP16A/DSP16C architecture required upwards of 40 Mips of processing power, the new DSP1610/DSP1616 chips can handle the same algorithm with less than 20 Mips.

Like Analog Devices' DSP, AT&T integrated a sigma-delta codec with its DSP to provide a single-chip solution to the speech conversion problem. "Adding a codec on-chip adds to the complexity of manufacturing. And it's not necessarily cheaper than building a system around a DSP and adding a separate codec," Erickson admits. On the positive side, it takes up less board space and consumes less power. "You have to look at all the trade-offs with this level of integration. And lower power in the digital section of the phone is a requirement close to many designers hearts," he concludes.

While standards for digital cellular and digital cordless phones have been set in Europe, the standards in North America are still in a state of flux. That's why National took the approach it did with its work in the RF arena. "We thought it more conservative to introduce building blocks that can be incorporated into a number of different systems and then, in the second- and third-generation products, begin to integrate more functionality and gear the devices towards a particular standard," says Curtis Schmidek, National Semiconductor's product marketing manager for wireless communications products. National Semiconductor (Santa Clara, CA), in cooperation with Dancall Radio (Pandrup, Denmark), demonstrated a working cordless phone transceiver chip set for the Digital European Cordless Telecommunications (DECT) system at October's Telecom '91 in Geneva, Switzerland.

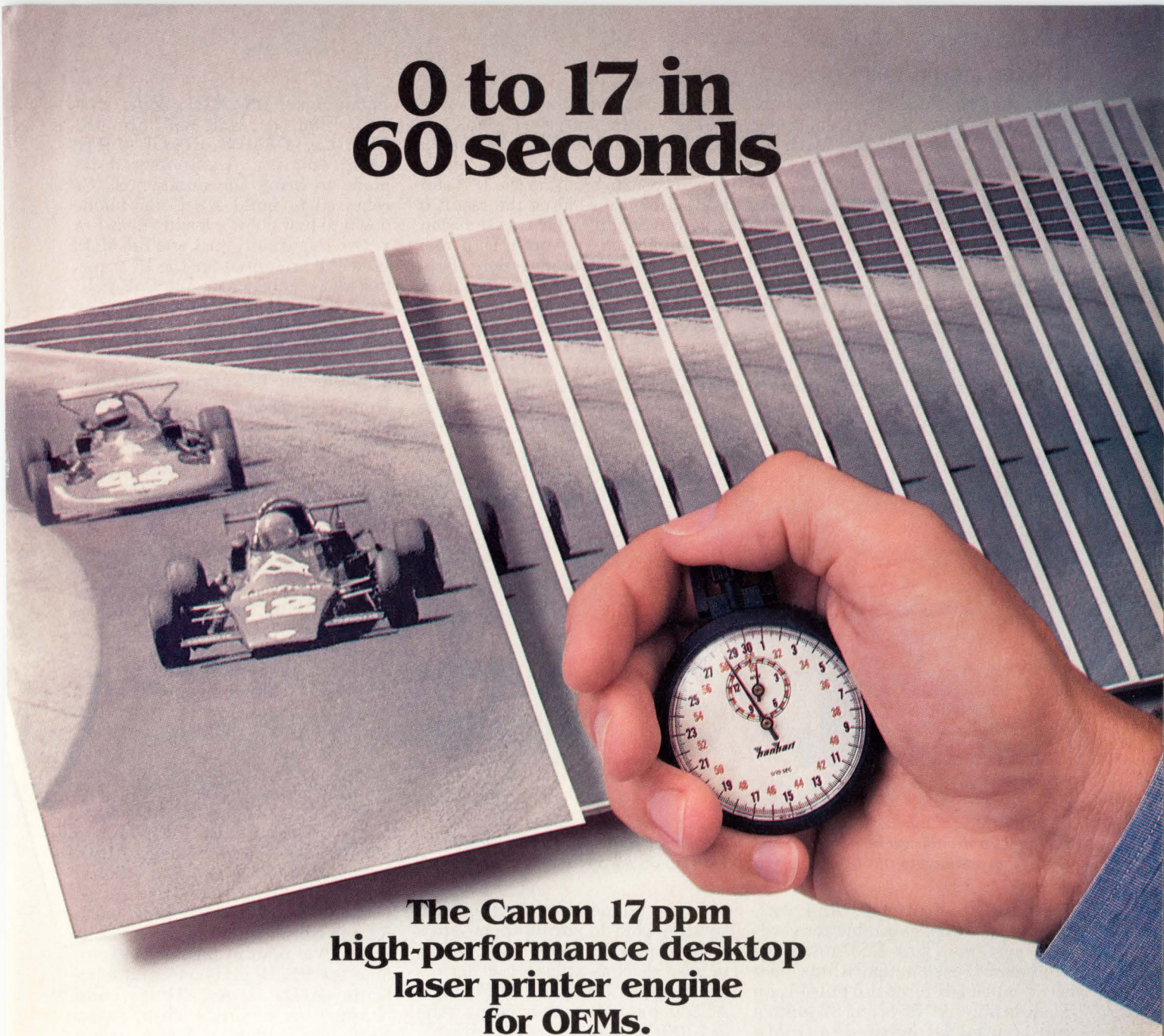
Unique architectures

Digital cordless and cellular systems have very different technical requirements, making the respective RF/IF/baseband architectures of each unique. Cellular systems, unlike cordless, must operate in a high-speed mobile environment over great distances and overcome the associated Rayleigh fading effects. Cordless phones, on the other hand, operate in a far less "hostile" environment, generally over short distances and at pedestrian speeds. As a result, the larger transmit power, heightened receiver sensitivity and DSP-intensive techniques used to overcome the conditions found in a cellular environment may be re-



Philips/Signetics prepared a performance estimation illustrating the computational load on a digital signal processor inside a cellular phone. As can be seen, the equalization is most demanding on the DSP's time, followed by the speech and channel codec functions.

0 to 17 in 60 seconds



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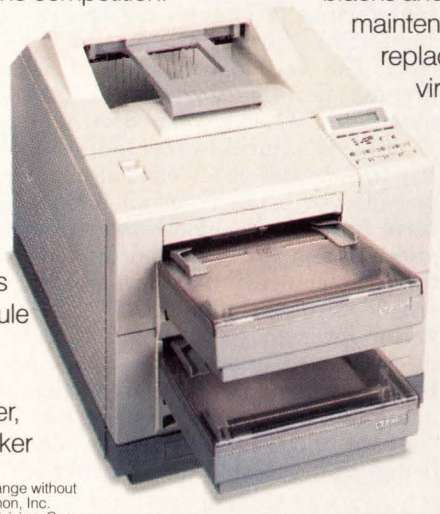

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laxed for a cordless implementation. The RF requirements of emerging digital cordless systems (such as with DECT at 1.9 GHz), however, will present the real challenge to designers working within system cost constraints.

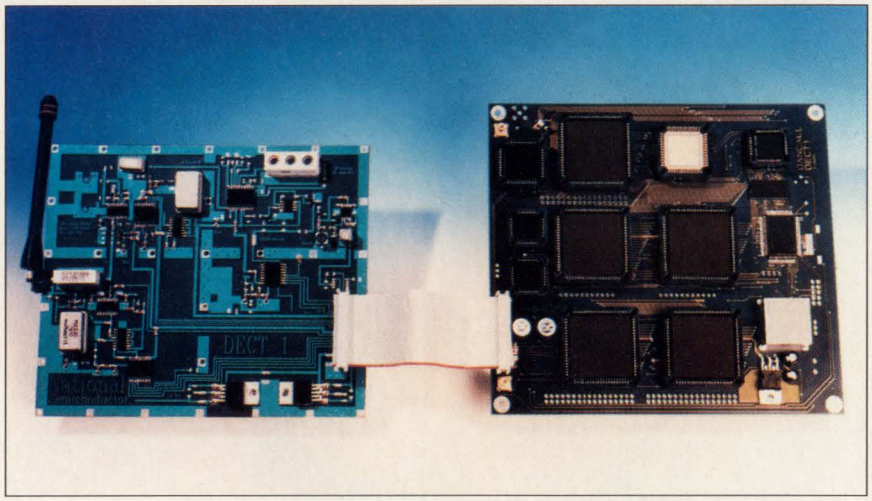
In a digital cellular system, the data rate is kept as low as possible (270 kbits/s for GSM) to efficiently support many users spread over large distances (up to 10 miles). A cordless system, such as DECT (with a data rate of 1.152 Mbits/s), operates within 100 yards or so of the base station and thus can support much higher data rates (making it well-suited for data applications). And with higher bit rates available for cordless systems, less DSP-intensive voice compression algorithms such as advanced differential pulse-code modulation (ADPCM) at 32 kbits/s can be used (as opposed to GSM's RPE-LTP at 13 kbits/s).

In a digital cellular system, the incoming 850 MHz RF signal must pass through a variety of mixers, IF amplifiers and filter stages, much as it does in an analog cellular design, before a signal processor working in the 20- to 30-MHz range can deal with it. As the signal comes into the phone, the RF section quadrature demodulates the RF signal, (a process that strips the data off the RF carrier) and presents the analog I and Q signals (representing the in-phase and quadrature components of the recovered signal) to A-D converters where the signal is converted before being sent to a modem/equalizer.

The modem/equalization function may be performed by an ASIC or by a DSP. On the output side, the process is reversed. The RF section quadrature modulates the I and Q signals converted from the D-A subsystem before sending the result to a power amplifier for transmission. An integrated converter chip may provide the A-D conversion of the in-phase and quadrature signals in the receive path as well as the D-A conversion of the in-phase and quadrature signals in the transmit path.

Many vendors, including Sony (Cypress, CA) and GEC Plessey (Scotts Valley, CA) produce bipolar parts aimed at the IF section of a cellular phone. Ultimately, most vendors plan to shrink them into a single BiCMOS device. At present, in most designs at least two devices are needed for the IF/RF stage. AT&T provides two chips (the W1000/W1452) for the RF/IF, up/down conversion function. Filtering is still performed by passive components (resistors, crystal, ceramic SAW filters) external to the chip. The W1000 combines an RF preamplifier, mixer and quadrature modulator. When combined with the W1452 IF amplifier/demodulator IC, filters and local oscillators, it provides both the transmit and receive functions needed between the antenna and the baseband. In addition, the company has developed a single-chip baseband A-D/D-A converter for signal conversion of the in-phase and quadrature signal in both the transmit and receive modes.

Similar approaches are being pursued at most other vendors, one being Philips/Signetics. When the company recently disclosed an integrated chip set that will meet the GSM and DAMPS (digital AMPS) requirements, it announced its plans to bring the number of ICs required to build a cellular phone down to just a few over the next few years. Eventually, just one BiCMOS IC will be required for the IF transmit and receive path, one CMOS IC for baseband digital signal processing and one CMOS part for the microcontroller function.



National Semiconductor demonstrated its DECT chip set at the Telecom '91 show in Geneva. In addition to DECT, National is also working on silicon for cellular phones.

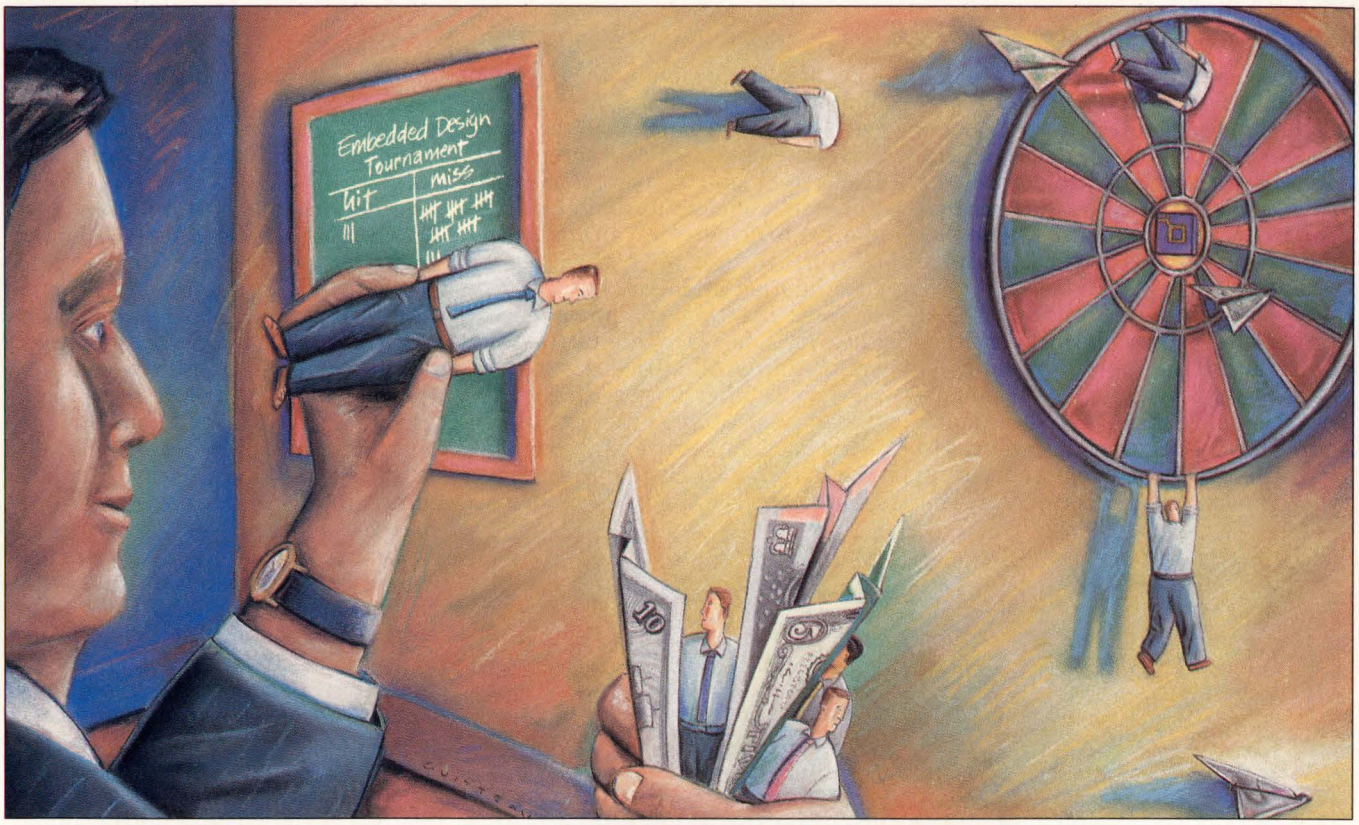
Single-chip RF solution coming

Hudson at TI also predicts that the RF section of the phone will be a single chip solution by 1995. "Our technology will allow you to get a cellular phone down to a few chips," he says. "Ultimately, in 1993, we will have all the A-D and D-A and the RF components all on a single baseband chip. All you will be left with is another microcontroller to control a display," he concludes. To make it happen, Texas Instruments is working on some new technologies, including heterojunction bipolar transistor technology for RF power amplification—a technology that Hudson feels should be more affordable than the GaAs FET technology currently in use by some manufacturers.

To reduce component costs, National Semiconductor plans to use its BiCMOS technology, ABiC. In addition to the European digital cordless (1.88 to 1.90 GHz) arena, National is also developing parts for the cellular (900 MHz) marketplace. "We plan eventually to combine the RF, IF and baseband functions (A-Ds, D-As, filters, and timing) on a single chip," says National's Schmidek. When such a chip emerges, it's certain to be aimed at a specific standard since there are differences between GSM and DECT architectures.

"The RF parts exhibited in the DECT demonstrator were built on a bipolar/BiCMOS process which allows us to implement circuits that operate up to 2.5 GHz. That should cover cellular, cordless and personal communications systems in Europe and Japan as well as the UK," he adds. First-generation parts implemented in National's BiCMOS process will include a variety of transmit, receive, frequency synthesis, and baseband processor functions.

If the processing becomes more computationally intensive as designers move from analog to digital



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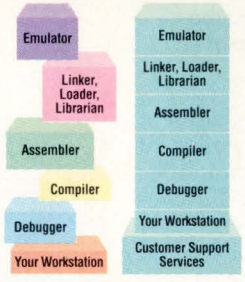

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CIRCLE NO. 43

designs, what happens to the RF section? According to TI's Hudson, it becomes less of a problem. "In some ways, the RF side in a GSM phone gets easier as you go to digital," he says. That's because, unlike an analog phone, in a digital phone the transmitter and receiver don't have to be working continuously.

"Because digital phones use a time division multiplexed (TDM) address and data approach, you don't have to be continuously transmitting and receiving," Hudson points out. This means that designers will have less of a problem separating the transmit and receive paths inside the unit to prevent crosstalk.

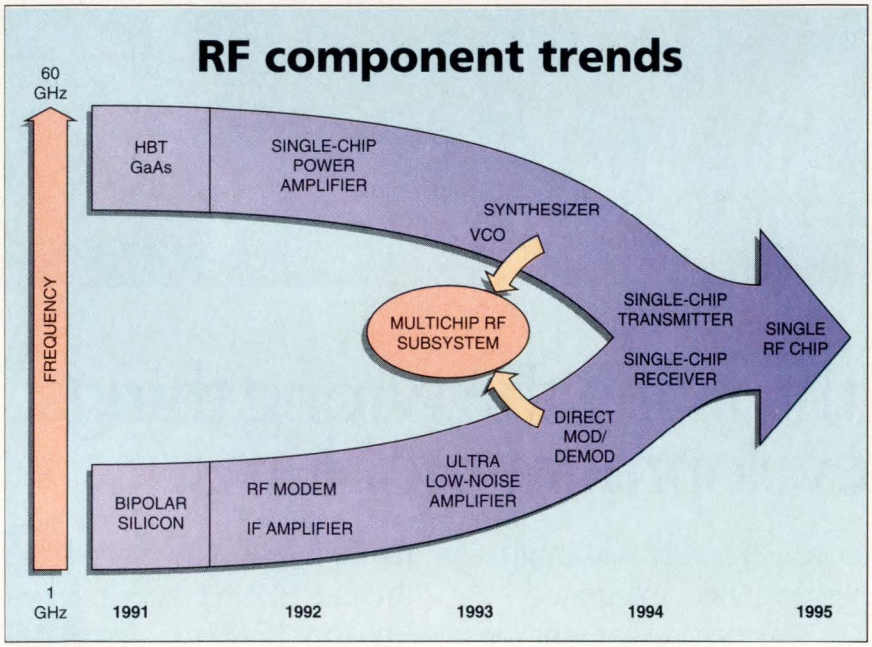
Also, digital phones have less of a power consumption problem than their analog counterparts. "Because it's always on, the one thing that really flattens the battery in an analog phone is the transmitter. Hence, power consumption is a major problem," Hudson says. "The advantage of a digital system is that data is sent in bursts, so the average power level is reduced. And the requirements for efficiency can be reduced in a digital RF power output stage," he adds.

Verma Labs' Verma says that because the transmitter must be turned on and off at given instances of time in a digital phone, a power amplifier that can be stabilized quickly is required. "In an analog design, you can live with a class C amplifier. In a digital design, you need a class A/B design," he says. Nevertheless, he does agree with Hudson in one respect: "The only thing that makes (a digital phone) simpler to design than an analog one is that there's less of a power consumption problem".

But it isn't just stabilization, it's linearity, too. In a digital system, maintaining the linearity of the power amplifier is very important. "We're designing power amplifiers using our GaAs process technology," says AT&T's Erickson. "We believe we will achieve the performance requirements for high linearization of the power amplifier," he adds. To help keep existing power amplifier circuits linear, one of AT&T's customers turned to an additional D-A converter between the baseband and RF section of the phone to help control the linearization of the power amp. The linearization control software runs on the DSP, naturally enough.

National's Schmidek feels that with an analog cellular phone, it's easy to build a power amplifier in a bipolar technology. "GaAs would give you a more efficient solution, but if you want to do it cheaply, it's better to do it with bipolar," he says. Schmidek feels, however, that the class C amplifiers found in today's analog cellular phones are commonly implemented with discrete bipolar devices, often in costly hybrid modules. GaAs implementations are available, but are only used in the most-expensive phones. Integrated bipolar and BiCMOS solutions in surface mount packages are the next logical and most cost-effective step. The class A and A/B amplifiers required for some digital systems will present another challenge for designers, but there's some promise here as well. The DECT demonstrator in the National/Dancall Radio used a class A/B transmit amplifier IC implemented in National's bipolar process.

Today, most cellular designers are also having problems dealing with the power dissipation of the digital section. But before long, due to advancements in CMOS technology, the power dissipation there will become less of an issue. The most power hungry device will be the RF power amplifier. For GaAs, a technology that held so much promise in the '80s yet delivered so little, might find a high-volume application after all. "We think with GaAs we can produce a very high-performance device. Models will be available early next year to prove out our theory," AT&T's Erickson says. ■



By 1995, a single RF chip is all that will be required for the transmitter/receive section of a cellular phone. This road map shows how Texas Instruments aims to get there.

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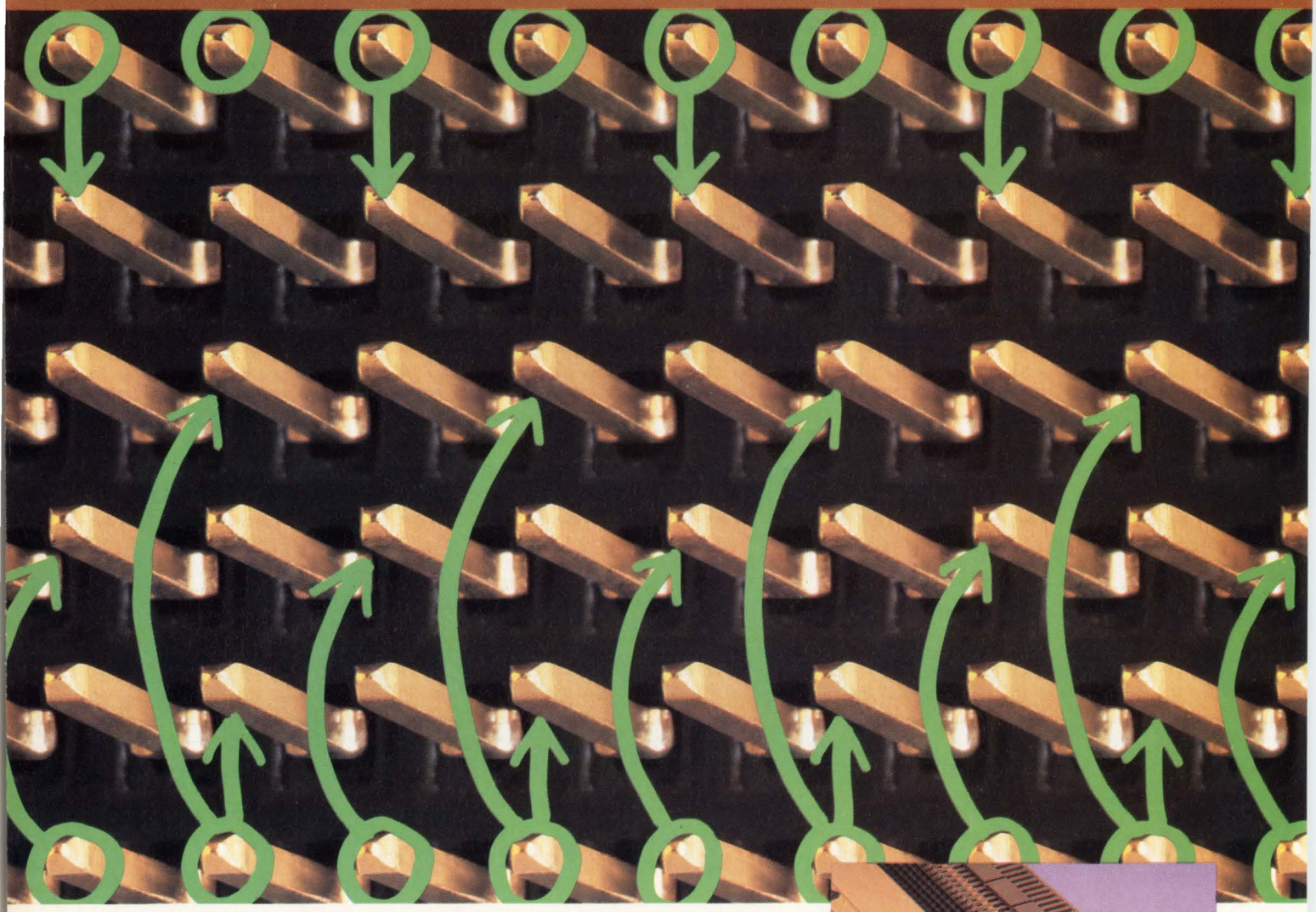

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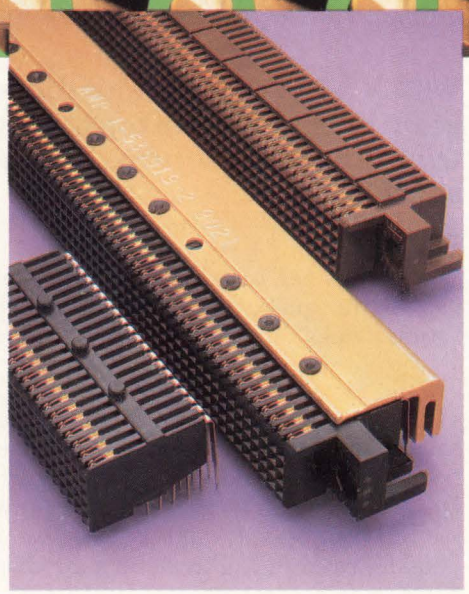

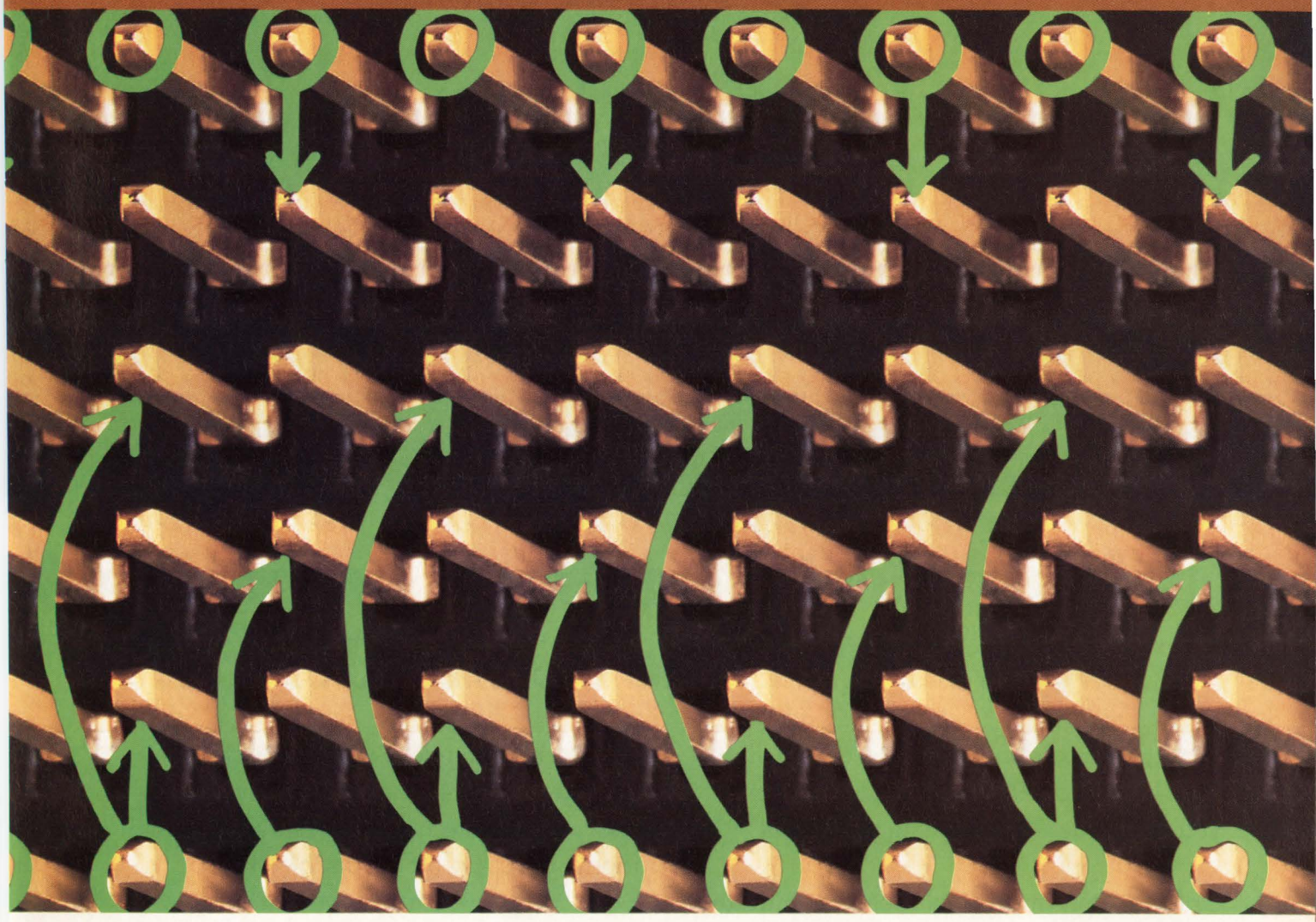

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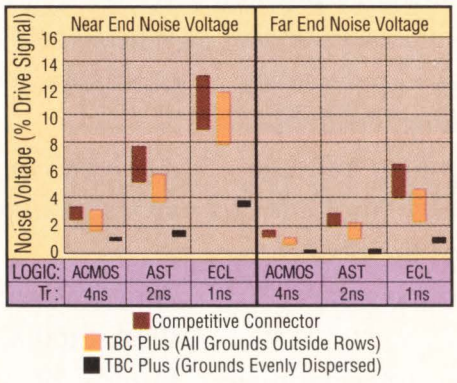

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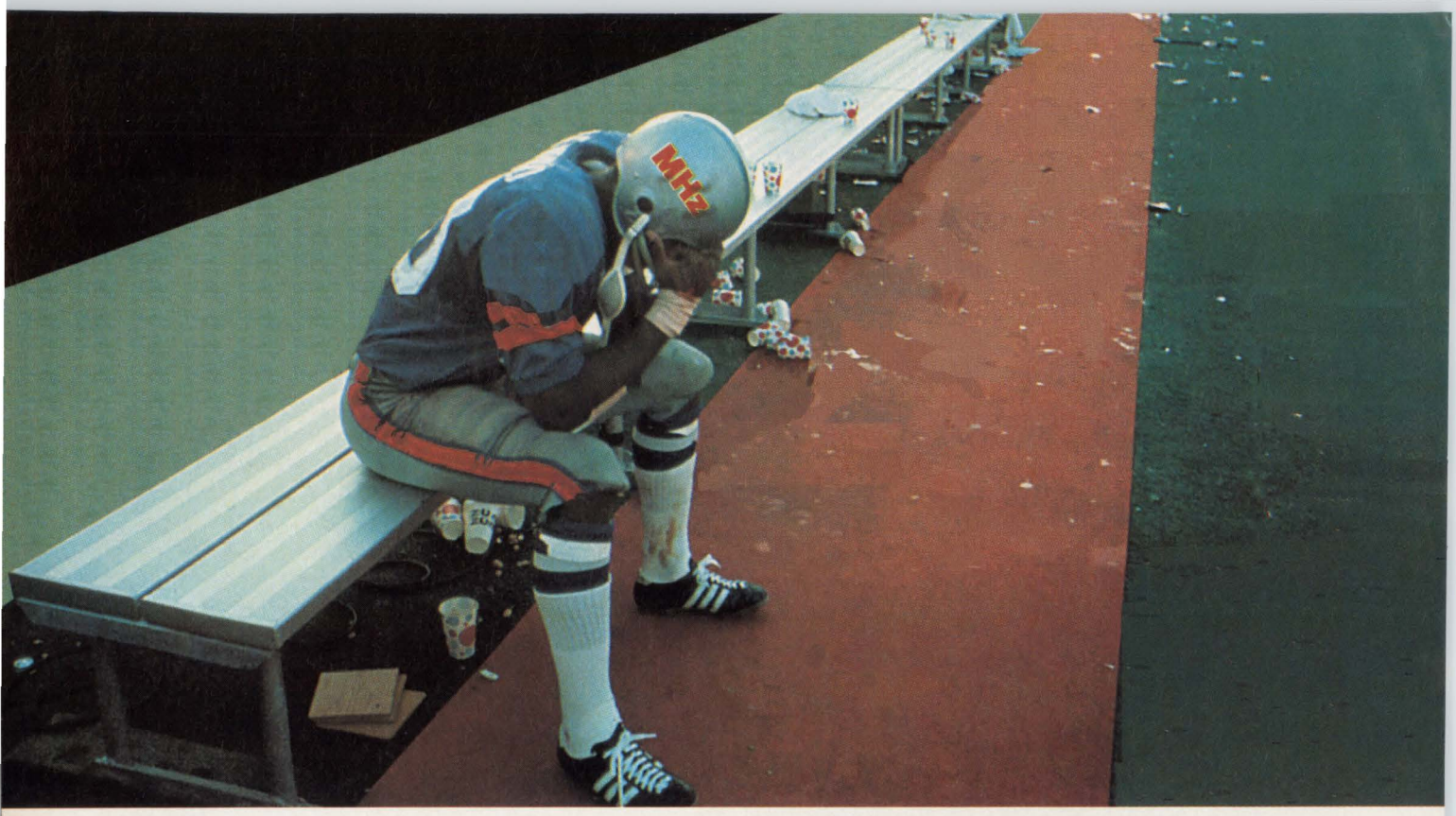

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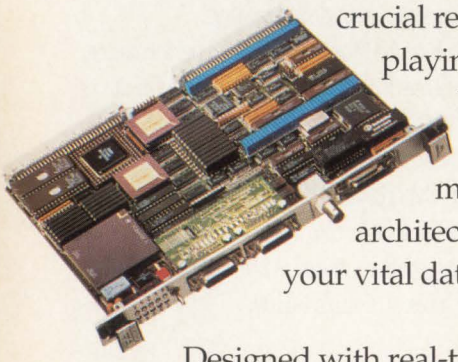

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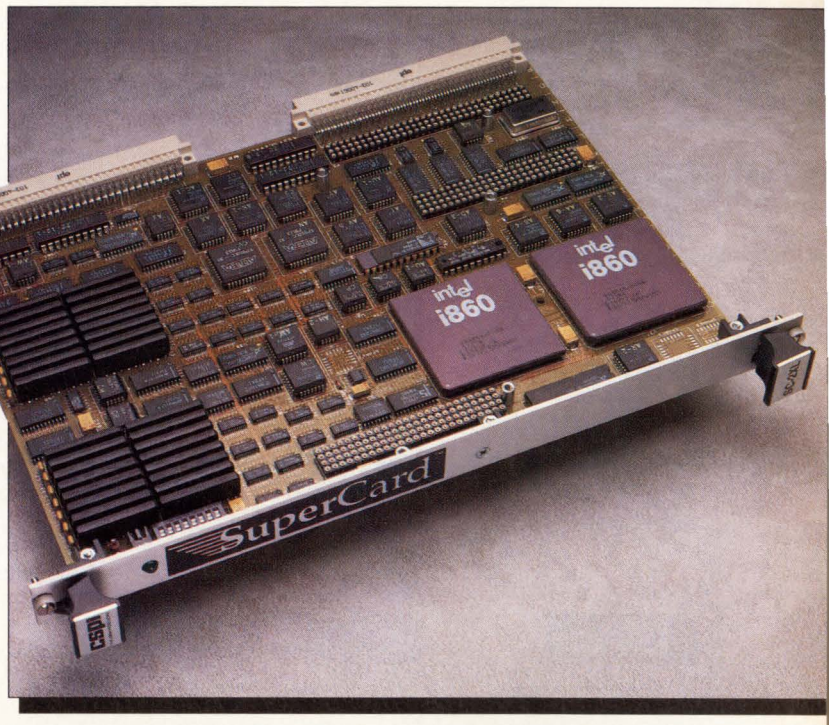
CIRCLE NO. 46

Add-on boards boost real-time performance

Add-on boards can increase performance, but their use still isn't straightforward.

Warren Andrews
Senior Editor



CSPI has developed SuperCard, a i860-based vector processing subsystem for the DECstation 5000. The board interconnects with the DECstation via DEC's Turbochannel—or optionally via direct I/O ports. The DEC version of CSPI's SuperCard is finding use in a variety of applications, such as signal processing, sonar, radar, ASW, image research, medical imaging, and electronic publishing.

Almost as long as there have been computers, there have been attempts to add something to them to boost their performance. At first, these add-ons were chips and boxes, but with the spread of standard buses, the idea of add-on boards became a reality. Now, with the array of real-time applications fitting into such standard-bus hardware platforms, add-on boards to accelerate performance are gaining importance.

But accelerator add-ons still are not magic; there's some penalty associated with their use in terms of additional software overhead in one form or other, and there's still no universal way to have additional processors speed up applications in any direct proportion to the number of processors. In addition, the loud clamor for standards in both hardware and software adds still another constraint to the implementation of accelerator-type products. Despite the obstacles, however, dramatic progress has been made—particularly in specialized areas.

In many applications in the real-time arena, such accelerators are a major boon to performance enhancement. Newer and more clever techniques are beginning to let large multiprocessor configurations provide systems with tremendous speed advantages. And tools to help developers adapt, debug and simulate applications using specific configurations of processors—and to sample scenarios with different processors—are emerging and greatly simplifying such implementations.

Traditionally, the idea of add-ons to increase performance began with the simple math-coprocessor-chip approach, sockets for which have been included in almost every CPU from lowly desktop personal computers to more powerful VME and Multibus II engines. "The biggest advantage of this approach," says Geoffrey Cohler, product marketing director for CSPI (Billerica, MA), "is that it's one of the easiest and least expensive techniques for increasing performance. As long as the compiler knows the coprocessor is present, it will generally speed up the application. "On the down side," he continues, "it's necessary to trade performance for ease of use. Such coprocessors offer

only a limited speed advantage."

The limitations of the single chip-math-coprocessor approach have led designers to look to better solutions, such as using digital signal processor-based boards as well as more generic multiprocessing boards. These can include boards with multiple DSP chips, one or more of the same processor chip, or different combinations of specialty and generic CPUs.

Such products essentially operate in one of three modes. "The first and simplest mode of operation is that of simple application acceleration," says Barry Isenstein, product planning manager for Mercury Computer (Lowell, MA). "By this, I mean simply take the application, compile for the accelerator processor and go. In such a mode, it's not necessary to write any code for the host computer at all. The accelerator board takes care of everything including I/O from a standard I/O library offered by Mercury in C and Fortran languages, as well as in assembly code."

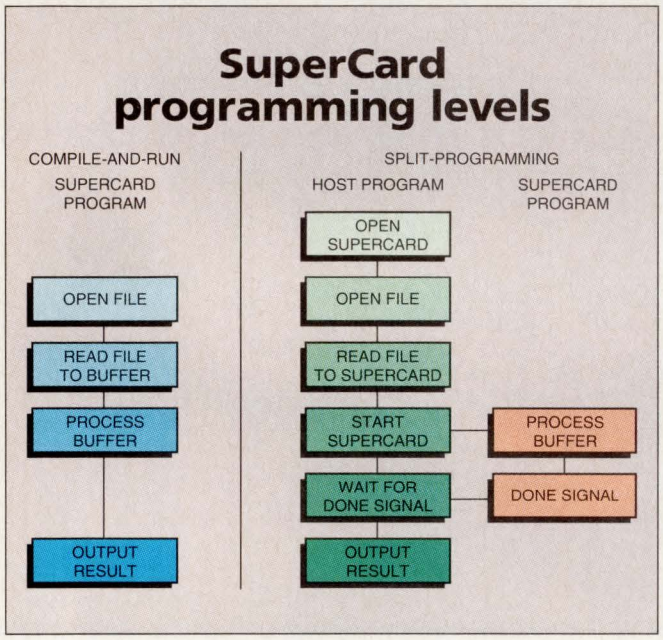
The second mode of operation is a subroutine engine. "Traditionally, this approach is what most designers refer to as the classic array processor," says Isenstein. "In this mode, the processor is treated as a peripheral of the host processor. As a peripheral, the attached processor handles a small number of fixed functions such as DSP. And while users can add some bells and whistles, essentially, the designer is writing a program that operates on the host computer as opposed to running on the application accelerator." Isenstein explains that this approach is very asymmetric in that there are certain specific tasks that the host processor runs, and others are run by the accelerator.

"In the third mode," says Isenstein, "designers use such application accelerators in a multiprocessing or multicomputing environment. In our approach, we have an API (Applications Processor Interface) that essentially treats all the processors—accelerators as well as host—as a real computer that addresses multiprocessing problems. For that, we have an API that uses standard processing techniques that users are familiar with such as sockets for message passing, shared memory areas and semaphores.

"In this mode," he continues, "you're looking at applications that definitely want to use more than one processor. The other two modes don't necessarily rule that out, but this third approach lets them be programmed in a way designers are familiar with."

Mercury isn't the only company to be actively working on multiple-processor systems. Just about everyone in the application accelerator game is working with some kind of multiprocessor system. For example, CSPI, like Mercury, offers both a compile-and-run approach as well as a split-programming mode.

In what CSPI calls its compile-and-run mode, the user simply compiles a program using the development tools supplied by the company (either the Metaware C compiler or the Lahey Fortran Compiler), producing an object file. This is then linked with an i860 linker to produce executable code for the accelerator board. Calls to various run-time libraries are linked in the linking process.



CSPI offers two levels of programming for its SuperCard, depending on the speed-up desired and the level of effort to be expended. The compile-and-run mode lets designers compile, link and run any C or Fortran program with few, if any, changes. For greater speed-up, it's possible to replace program loops with subrouting calls to one of CSPI's libraries.

A toolkit approach

CSPI has also worked closely with Multiprocessor Toolsmiths (Nepean, Ontario, Canada) in developing integrated software to work on the i860 processor. Says Toolsmiths' president Kim Rowe, "What we've looked to do is develop a multiprocessor operating system to work with the i860, as well as other processors, to provide a total solution to real-time multiprocessing problems."

According to Rowe, the object is to take data in, manipulate it through some signal-processing algorithms and provide some output. "Typically," he says, "engineers begin with some kind of signal flow graphs. Today there are a number of tools to help generate such flow graphs automatically and do limited simulations which at least let the developer know the algorithms are correct." But how does the designer convert this flow graph to a real implementation on a multiprocessor system?

Rowe explains: "Once the flow diagram is completed, Toolsmiths' OnTime program lets the designer develop a concurrent model for totally transparent multiprocessing using a graphical design approach. The graphical approach lets the designer graphically design, generate code, pull in libraries for algorithms, make calls to hardware elements, etc."

Continues Rowe: "The next step, is to let the host simulate the selected hardware. The software has an implicit understanding of the macro-parallel model to do the computation, but the designer must break up the algorithm," he says. Rowe cites the example of a 24-tap IIR filter. "The designer can, for example, break the job up into three tasks in a pipeline, each comprising eight taps. The software can run all three tasks on a single card in that card's pipeline, or run each task on each of three different cards."

"The software is based on the pSOS+ real-time kernel on top of which Toolsmiths provides a set of graphical tools and Unix-compatible

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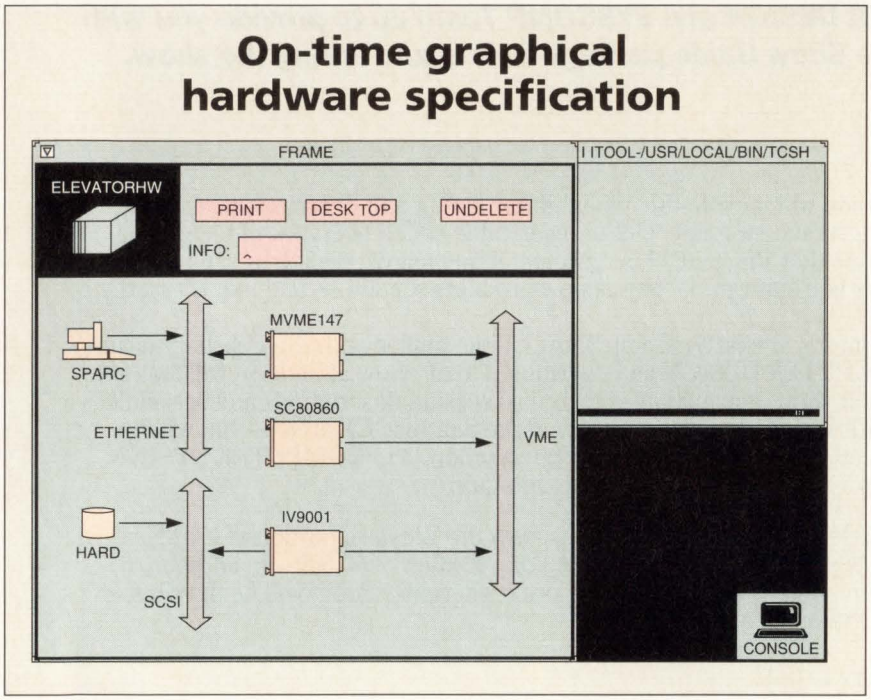
layers for I/O and other system functions. Toolsmiths has provided standard file I/O, networking protocols such as TCP/IP, a network file system (NFS), an external file system, serial support, tape support, X Windows, X View, X file, RPC (Remote Procedure Call), Open-Look window manager and XDR (a data-exchange protocol).

"Using these features," says Rowe, "it's possible to develop a very fancy user interface with, for example, 68030 or 68040 processors and including a mouse and windows, and interface it directly with a real-time application. The entire application can be tested on a Sun workstation and downloaded via X View commands directly to an X Terminal and real-time, low-cost target system."

According to Rowe, Toolsmiths' software lets the entire application run transparently. "It doesn't matter where [on what board], for example, a network server resides, when there's a call to that server it automatically goes to the right place."

Another special feature of Toolsmiths' development tool is its visual source and system debugger. "Among other things," says Rowe, "we've developed the ability to monitor the utilization of each CPU in the system and can display a history of each processor's usage." According to Rowe, this lets designers tune a system by looking at the idle time of each CPU and reassigning tasks.

"In this way," he adds, "it's possible to balance CPU loading and converge on an ideal solution that will optimize performance in a multiprocessing system. All that's required to reallocate the system resources is to relink the application." Similarly, says Rowe, it's possible to look at different numbers and combinations of processors to seek a solution optimizing a particular application.



Graphical hardware descriptions of the mixed multiprocessor architecture provide documentation and the necessary information for users to quickly build pSOS+/Unison or VMEexec applications. The transparent multiprocessing of the operating systems works with these descriptions to insure fast incremental enhancement without application changes or painful rebuilding.

The i's have it

While most of the i860-based accelerator boards use the main processor for both high-speed array processing and I/O, at least one company, Sky Computers (Chelmsford, MA), developed its Warrior 3 array processor board combining an i860 to do the signal processing with an i960 to handle the I/O. "In most accelerator applications at today's compute rates," says Dr. Gerald Shapiro, chief technical officer at Sky, "data movement, rather than processing power, becomes a limiting factor. You have to swallow the whole problem to get around the data-movement limitation. This means the code that the host computer used to run, now has to run on the accelerator card."

"In looking at an application program," continues Shapiro, "we don't only worry about the main processing code, but also about what happens when there are calls for a windows access or a disk access, for example. Designers don't want to be concerned with going through all their code looking for all the graphic, disk drive and other system-level calls. By simply running the code through some software tools, the entire program can run on the accelerator."

According to Shapiro, designers don't have the luxury of spending six months to a year to tune up an algorithm and gain perhaps another 4 or 5 percent. Instead, a more appropriate metric might be whether performance can double in one year or 18 months. To get this type of performance, it's necessary to use a brute force approach.

"To be fully compatible with our earlier Warrior 1 and Warrior 2 array processing boards," Shapiro continues, "we let our next generation appear to look to the designer like earlier generations. While technically a true application accelerator, our latest board, with some specialized software on top, looks like a typical array processor.

"And while the processor on the Warrior 3 is based on an i860, we also use an i960 as an intelligent I/O processor. We did this because we realized that many of our customers run large programs including much more than basic math processing. Because, while the 860 is good at those things, it doesn't do such a good job with things like, for example, interface control. We therefore free up the i860 to do what it does best and let the i960 take care of all the other critical I/O and system functions like interrupt handling, context switching and system interface."

Despite the ability of the i860 to operate effectively in a variety of stand-alone and multiprocessing applications, there are many arguments which continue to favor more traditional, DSP-based accelerator boards (see "Evaluating vector processors for real-time DSP applications," p 76). "There's little question," comments Scott Israel, director of marketing at Alacron

Evaluating vector processors for real-time DSP applications

While the i860 was originally developed for graphics, its high-speed vector arithmetic capabilities are being exploited in a wide range of compute-intensive applications. One example is digital signal processing, where the i860 is often evaluated as an alternative to conventional DSP microprocessors.

In choosing between a DSP and a general-purpose vector coprocessor such as the i860, however, designers must evaluate more than raw cycle time and MFlops. In applications such as real-time signal processing and embedded control, data movement, I/O, context-switch speed, interrupt response, integer performance, and determinism are often just as crucial as number crunching.

Peak performance quotes

Because real-time DSP applications are often compute-bound, one of the first parameters that designers typically evaluate is the processor's MFlops rating. Direct MFlops comparisons between DSPs and vector coprocessors, however, can be misleading.

The i860, for example, quotes a peak performance of 80 MFlops, which is theoretically 2 to 3× that of most DSPs. Because the i860 relies heavily on pipelining, however, it can achieve that performance level only in vector applications. In nonvector applications, such as signal coding, or even in vector applications that require frequent branches, context switches, or interrupts, cache misses and pipeline flushes can reduce actual performance to a fraction of the rated performance.

Most DSPs, by contrast, don't use pipelining in their arithmetic unit. Consequently, they can achieve a much higher proportion of their peak rated performance in a broader range of vector and nonvector applications. The lack of pipelining also makes DSPs easier to program. Because the results of one instruction are always immediately available to the next instruction, DSPs not only simplify hand coding, but facilitate the design of more powerful, optimizing compilers.

Another important factor that designers should evaluate when choosing a processor for a real-time DSP is how fast it can access data. To keep their arithmetic units busy and achieve their theoretical peak MFlops ratings, the processor must be able to fetch a new instruction and two data operands on each cycle.

Data on the move

Some DSPs make this possible by providing two external data buses, together with separate address generators that can independently generate new instruction and data addresses on each clock cycle. The i860, by contrast, provides only one external data bus and one address generator. Consequently, it can support concurrent data/instruction accesses only when operating out of on-chip cache. When executing programs that use larger data sets (such as a 4-k fast Fourier transform) that are stored externally, performance may degrade significantly.

Another critical factor to evaluate when selecting a processor for DSP applications is I/O performance. To handle this requirement, most DSPs provide one or more high-speed serial I/O ports. Most DSPs also provide DMA controllers with multiple channels that can move data between one or more serial/parallel ports and the CPU without interrupting program execution.

By performing data acquisition and data movement in parallel with program execution, programmers can keep the DSP's arithmetic unit continuously supplied with new data. The i860, by contrast, provides no serial I/O port and no DMA controller. Consequently, the CPU must perform all data movement, making it impossible to access and process data in parallel.

The i860's single data bus and limited I/O also make it cumbersome to use multiple i860s for applications that require higher throughput. Because the i860s can't be directly linked, designers must typically use some type of shared memory architecture. DSPs, by contrast, may be linked directly in a broad range of multiprocessor configuration via either their address buses, parallel or serial I/O ports. Moreover, because most DSPs provide multiple independently programmable DMA channels, data transfers and communications between the DSPs may be conducted without interrupting program execution.

Another factor that designers should consider when selecting a processor for a real-time DSP application is context-switch performance, which is important for both multitasking and servicing interrupts. Vector processors such as the i860 tend to have relatively poor context-switch performance because of their large register sets and pipelines, which must be saved and restored with each context switch.

DSPs, on the other hand, speed context switching and interrupt handling by using smaller register sets and minimizing the number of registers that must be saved (as few as 18 cycles on a DSP, versus 81 on the i860). In fact, many DSPs provide mechanisms that enable critical interrupts to be serviced in as little three instructions (24 instructions on the i860) without any context switch at all.

Designers should also evaluate determinism when selecting a processor for a DSP application. Because DSPs must frequently operate on incoming signals in real-time, in order to accurately budget available processing time, their performance must be predictable.

Predicting performance

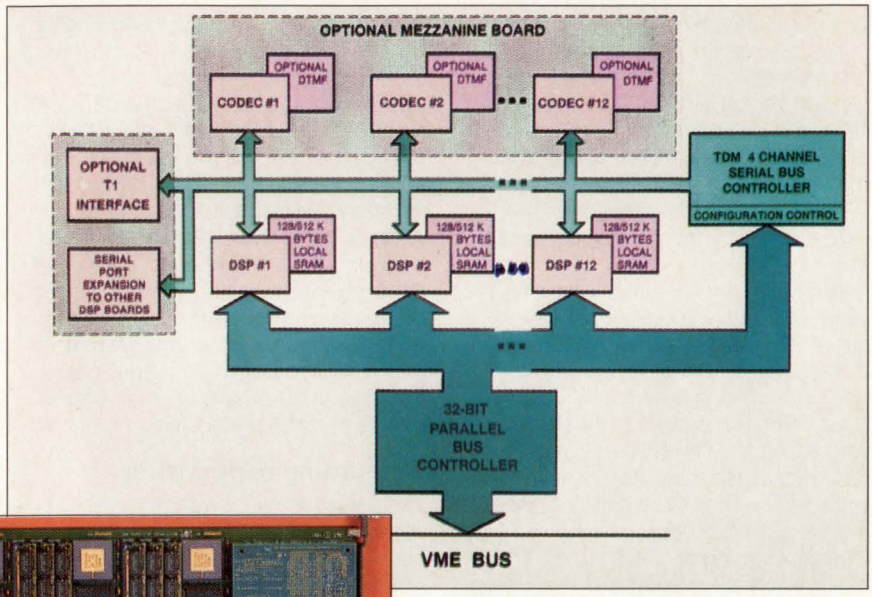
The performance of vector processors such as the i860 is often unpredictable because it depends on the cache hit rate, which may vary considerably depending on the contents of the cache. While many DSPs also provide cache, they enable portions of the cache to be independently locked. Because this locked region can't be overwritten, programmers can ensure a 100 percent hit rate and predictable performance for critical real-time tasks by locking the portion of the cache that contains the data and instructions associated with those tasks.

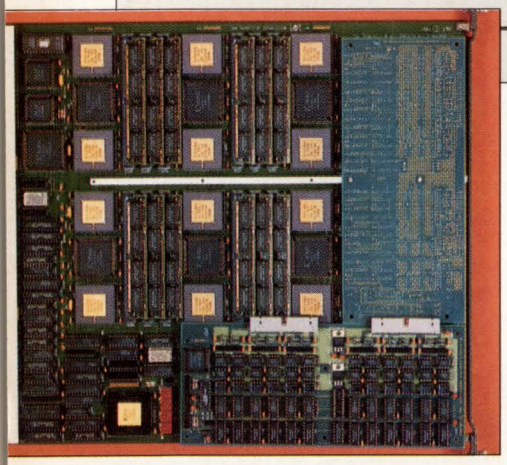
In spite of their real-time limitations, vector coprocessors such as the i860 may be successfully employed in many compute-intensive DSP applications that require limited real-time I/O. One way to overcome the i860's I/O limitations is to use a DSP as a front-end processor to handle real-time I/O, and an i860 as a back-end processor to handle number crunching (as in Ariel's IRCAM SPW). Still, for I/O intensive real-time DSP applications, particularly those that require multiprocessing, arrays of high-speed DSP microprocessors make the most sense.

Tony Agnello, president, Ariel Corp

(Nashua, NH), "that products will become increasingly specialized as, on one side, applications become more specific, and on the other, as general-purpose processors include more and more processing power."

The number of applications that can take advantage of specialized processors is increasing dramatically—due largely to the cost-effective approaches now available. "Applications that would have been unimaginable only a few years ago," says Shapiro, "will soon be a reality."





Communication Automation & Control's VME9U12 provides users with up to 300 MFlops of processing power using 12 AT&T DSP32C processors. To fit everything on a single board, plus offer the expansion of full-featured mezzanine boards, CAC had to resort to a full 9U board. The board is intended for communications applications and can be used with an add-on mezzanine board providing 1.544 T1 communications or a board comprising 12 8-bit companding codecs to provide 12 channels of voice I/O at an 8-kHz sampling rate.

He cites, for example, an application used in the detection of hazardous substances for things such as airport security. Another application includes recognizing musical tunes/lyrics for the purpose of collecting royalties.

Other applications include the traditional bastions of signal processing technology such as sonar, radar and medical imaging. In the latter arena, developments combining new sensor technology on one side and new signal-processing capability on the other have led to diagnostic tools such as PET (positron emission tomography) scans.

Where does it end?

But the end is nowhere in sight—and we can't even see the whole beginning. Intel's i860 started life as a graphics processor and users were quick to see its potential as a general vector processor. But this processing capability will soon be appearing on conventional microprocessors—if not Intel's 80586, then perhaps on its 80686. But users will continue to need more speed.

This insatiable need for performance is only partially the avarice of system designers. The other part stems from the application of standards—particularly operating systems and programming languages. As these needs increase, specialized accelerators will have to answer in much the way that general-purpose application accelerators do now. In large measure, this will include a host of specialized software tools. But in other areas, it will include some highly specialized hardware.

Already some highly specialized hardware is emerging in the telecommunications area. Communications Automation and Control (Allentown, PA), for example, has developed a 9U VME card with 12 AT&T DSP32C floating-point processor chips. The board was designed to handle such complex tasks as voice recognition, speaker identification, advanced differential pulse-code modulation (ADPCM) compression, dual-tone multifrequency (DTMF) tone detection and other features expected on advanced voice mail systems.

According to CAC president James Bridges, the board also has provisions for specialized mezzanine cards which include a T1 and codec-daughterboard. In operation, each of the board's 12 DSPs executes programs and accesses data out of a local zero-wait-state SRAM. The board can act as either a VMEbus master or slave for either DMA or memory-mapped transfers.

Undoubtedly, more such highly application-specific boards will start to emerge as the technology and application mature together. In all manner of acoustics, from noise cancellation to music enhancement, accelerators will provide the necessary punch to perform in real-time what's possible now only in very slow motion. Similarly, in image processing, we're at the tip of a major new area of specialization. And, adding the two together, we've got one of the industry's top buzz words, multimedia. This has already resulted in the development of a number of what some board makers glibly call "multimedia adapter cards" but which are basically specialized application accelerators. ■

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COMPUTER DESIGN Technology and Design Directions

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Designers search for the secret to ease ASIC migration

Barbara Tuck Egan
Senior Editor

Designers are migrating from one technology to another—from FPGA to gate array, gate array to standard cell, PLDs to standard cell, and so on. Exploring uncharted territory, these designers are looking for the secret—from brute-force netlist translations to VHDL synthesis—that will help them create the most-cost-effective implementation.

There's no doubt that more designers are talking about migrating from programmable logic devices and field programmable gate arrays to full ASICs than are actually doing so today. Nonetheless, a small number of brave souls have taken a blind leap of faith into migration.

Those who are finding their way out of the jungle of tools and FPGA architectures tend to be designers who are either using silicon and tools with which they are already familiar, or trying more sophisticated methods but thinking ASIC design up-front. The methodologies and tools used to migrate depend very much on the reason for migrating in the first place, the target technology and the level of performance required in the end product, as well as the tools and hardware platforms available to the designer.

The single largest component in this migration fever is the FPGA. Whether chosen as the target technology or as a stepping stone on the way to an ASIC, the FPGA is the silicon technology most responsible for the changes taking place in the way users design their end products. Differing markedly from one another, FPGAs are not the easiest things to design and a number of designers have been disillusioned with the industry darlings. Because the majority of users to date have designed-in devices from Xilinx (San Jose, CA), which maintains the lion's share of the market, it follows that Xilinx has taken the brunt of users' complaints about FPGAs.

Timing close to gate array

"Each one of the FPGAs I've used has disappointed me," says Jack Regula, hardware engineering manager at Force Computers (Campbell, CA). That was before Force Computers acted as a beta site for QuickLogic's (Santa Clara, CA) antifuse-based programmable ASICs (pASICs). By the time Regula got his hands on QuickLogic's pASICs, he had given up on a Xilinx device, finding that it was too slow to implement a DRAM controller on an 88000-based CPU board.

Moving from Xilinx to QuickLogic meant Regula had to re-enter his schematics into the QuickLogic toolset, an effort that took a few days of drawing. He programmed QuickLogic's QL8X12 to be almost pin-compatible with the Xilinx part. Regula achieved a speed of 33 MHz in the QuickLogic pASIC, whereas the top speed he could get out of the Xilinx Logic Cell Array (LCA) was 20 MHz.

To get high performance and speed out of the Xilinx FPGAs, Regula reports, you can't do a purely synchronous design. "You have to tweak the design to fit the layout and to fit the board. How far apart the Xilinx CLBs [configurable logic blocks] are affects the propagation delays between them," he continues. "You don't know what the delay is 'til you route them." Unlike the Xilinx devices whose interconnect delays can be greater than logic delays, QuickLogic logic delays are always larger than interconnect delays, according to Regula. "They're predictable no matter what the layout is," says Regula, "very much like a masked gate array." At a maximum of 1,000 gates, though, QuickLogic can replace only the low-end Xilinx parts.

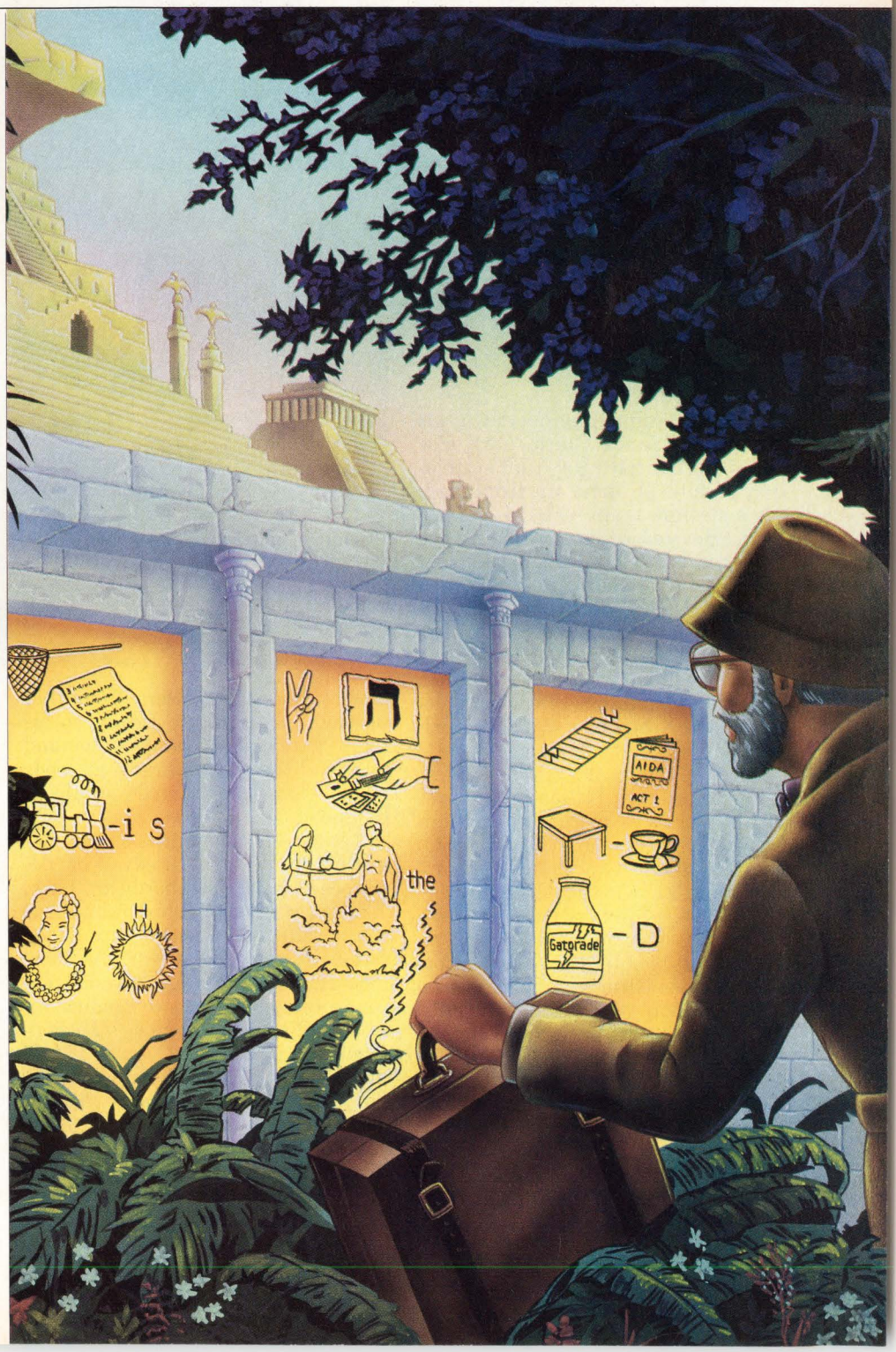
Design difficulties

Dave Hicks, staff engineer at SpectraLink (Boulder, CO), also had a bad experience with a Xilinx design, to some extent because they pushed their design. His design

team was using Xilinx 3090s in SpectraLink's indoor cellular phones. The phones act as add-ons to PBXs and replace phone mail. As SpectraLink engineers added more functionality to the Xilinx parts, they couldn't get the software to route the parts successfully.

But Chuck Fox, director of IC marketing at Xilinx says, "Xilinx parts are just as easy to convert as others. There's not much we can do to make it easy to convert a hard design." While Xilinx advises users not to push beyond a 50 to 60 percent utilization on the 3090s, Hicks explains that his team had more functionality and needed more logic than that, so they used about 80 to 90 percent of the chip. What's more, SpectraLink designers didn't go to Xilinx training sessions and didn't call field support as much as they could have. "It took us a long time to learn the intricacies of the software," Hicks says.

When engineers at SpectraLink received a beta-site copy of start-up NeoCAD's (Boulder, CO) device-independent FPGA layout software, they put it to work on the Xilinx parts. "We got better performance from NeoCAD, with better-quality



ASIC MIGRATION

routes, higher-speed signals through the routes and much closer to 100 percent routing," Hicks reports. NeoCAD has optimized its tool to route 100 percent the first time, according to Hicks. That's in contrast to the Xilinx approach, based on simulated annealing and random placement, which involves generating as many runs as you can and choosing the best one, according to Hicks.

SpectraLink was attracted to Xilinx because of claims that a number of vendors could convert Xilinx FPGAs to full ASICs, but Hicks says, "We've discovered that it's not as simple as handing off XNF [Xilinx Netlist Files] and getting back an ASIC." At press time, SpectraLink was in the process of evaluating vendors to help in the migration process. "We don't have the time to learn everything we need to know to migrate. We have done no simulation because the development process was hurried," explains Hicks. "When you don't simulate from the beginning, it's hard to go to an ASIC," Hicks warns.

When designing the handset of SpectraLink's wireless 2000 Pocket Communication System (inset), Dave Hicks, staff engineer at SpectraLink, used a Xilinx FPGA to prototype circuitry before final implementation in a gate array. Hicks used NeoCAD's device-independent design tools to shorten design cycles by reducing both the place-and-route iterations for Xilinx parts, as well as the execution time for each iteration.

Be safe: simulate

Bob Briody, senior engineer at Apple Computer (Santa Clara, CA), also found out the hard way that simulation should be done up front. Briody's design team used a pair of Xilinx devices when developing the Personal Laser Writer LS: the laser engine control went into one FPGA and the DRAM controller and decompression logic went into the other. "We had a problem with test vectors because we didn't pay much attention to simulation when we designed the Xilinx parts," admits Briody. When the time came to cost-reduce by going to a gate array, Apple found that NCR was the best fit and chose to go through Design Engineering Inc (DEI) (Boulder, CO) because it had experience converting Xilinx FPGAs to NCR ASICs.

"Using the Xilinx devices as prototypes let us develop some statistics on what users would see as to performance," says Briody, "and it let the software team write code in advance." After making last-minute changes to the reprogrammable Xilinx parts, the Apple engineers took their OrCAD schematics of the 3090 designs and converted them to Mentor Graphics (Wilsonville, OR) schematics. "Once the design was on Mentor, we had to be very careful about clock distribution," explains Briody. The Xilinx architecture buffers users from that problem, according to Briody, so his team anticipated the problem and designed the schematics so all loads on the clock tree members would be balanced.

Apple used no synthesis in its migration path says Briody, who describes himself as a hardware hack. "I'm not willing to give up control of the design. I like getting my hands dirty with gate-level design." And how long did it take the Apple team from conception of product to product release—including technology development and prototyping? April 1990 to mid-March 1991, says Briody. "Now I'm doing another project, and I'm doing a lot more simulation," he says. Apple introduced the Personal Laser Writer LS with the NCR VGX1500 1.5-µm CMOS gate array and plans to migrate to an NCR VS1500 1.5-µm CMOS standard cell to further cost-reduce the product.

After a false start on attempting to prototype a high-speed 31,000-gate ASIC with Xilinx XC4000 devices and encountering a bug in the 4000 software, Briody gave up on the idea of prototyping the design altogether. Since then, Xilinx released the Blox (Blocks of Logic Optimized for Xilinx) module generation system to aid designers of XC4000 devices. Blox, which resembles the LPM (Library of Parameterized Modules) intermediate format being backed by Xilinx, lets users describe designs at the block diagram level rather than at the gate level.

VHDL synthesis

In contrast to "hardware hacks" such as Apple's Briody, some design-

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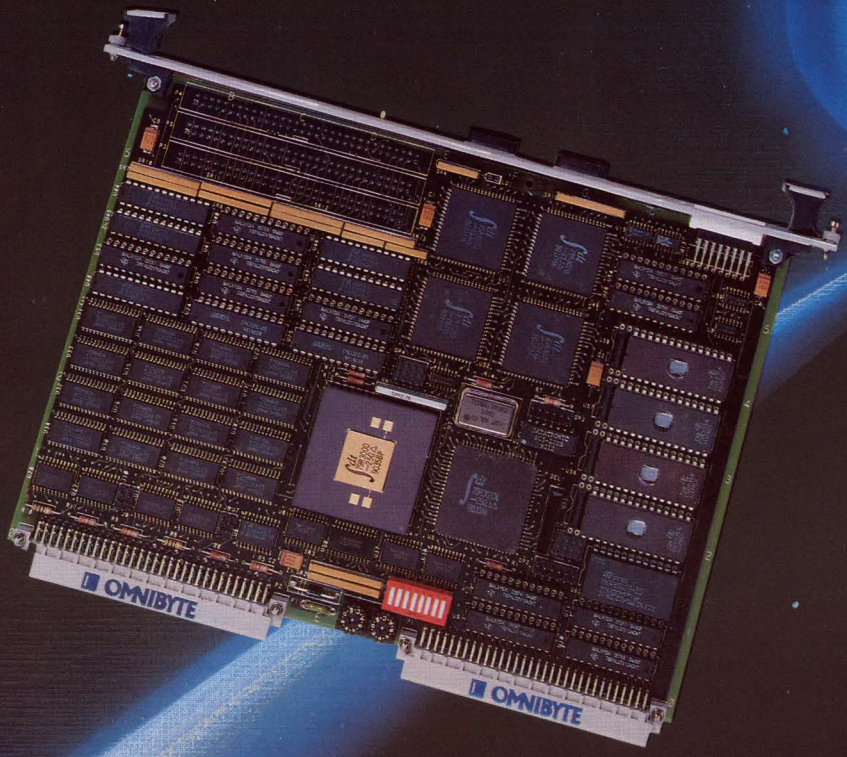

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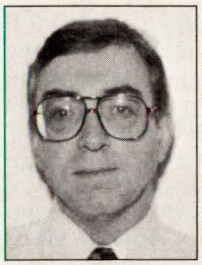
CIRCLE NO. 119

Retargeting in a mixed top-down/bottom-up design methodology



There are many articles advising the use of top-down design methodology as the new way for designers of FPGAs and ASICs to become more productive. This is the best design approach to deal with the problems of increasing design complexity and time-to-market pressures. It also reduces the chance of design errors inherent in the cumbersome and tedious tasks of gate-level schematic-based design.

Hardware designers need the same advantages that software programmers have long enjoyed. Designing software using C as the high-level programming language has proven advantages. Programming complexity has been greatly reduced, programmers are more productive, and programs can easily run on different computer architectures.

Keeping up with the hardware

The state of hardware design using VHDL, however, isn't at the same point of sophistication as writing software in C. Designers are just beginning to use VHDL and need to stay in close touch with the hardware of the design being synthesized. Sometimes they want to retain tight control over the implementation of some parts of the chip. In addition, over half of the new designs need to reuse all or pieces of an old design which may have been originally created with different technology in mind. A new ASIC or FPGA may be developed which incorporates one or more older PLDs or TTLs and combines it with new logic to gain added functionality, as well as reduce product cost. In both cases, elements of a bottom-up design approach still have a place.

Designs can be partitioned into hierarchical pieces, many of which can be totally described in VHDL. Good choices for behavioral VHDL are control and random logic sections of the design, since designers usually like to separate their data path logic design from the rest. Some designers may prefer to use the Abel language over VHDL for parts of their design. In data path design, designers may want tight control over the implementation and may want to instantiate large functional blocks such as 16-bit adders, multiplexers, etc. This can be done with a variety of techniques including schematic capture or structural-level VHDL.

The designer needs, therefore, a complete set of design tools to handle all of these design scenarios. These tools need to be well-integrated to give the designer the flexibility to handle existing and new design technologies. Synthesis technology alone is not a sufficient solution.

Viewlogic offers the designer many products to deal with each of these design elements in an integrated environment. Schematics along with a text editor are used to create the top-down design. Schematics are used to define the hierarchy, with symbols being created and used to point to lower-level schematics or files containing VHDL, Abel or JEDEC. High-level parts like adders and multiplexers from a vendor library or parameterized parts can also be instantiated directly in the schematic.

Abel or existing JEDEC PLD designs can be converted into full timing-simulatable and synthesizable VHDL using new alternate forms of entry (AFE) tools. A VHDL system simulator can be used to verify the design at this point in the design process, mixing schematic and VHDL descriptions. VHDL modules can be inserted into the design to create the stimulus for the simulation using high-level language capabilities.

The logic designer can then use synthesis applications supporting behavioral VHDL to implement the VHDL descriptions in the design into vendor-specific logic, using that vendor's specific library, and optimizing the results for the target technology. The designer has extensive control over the design being implemented by specifying timing requirements.

Making all the pieces fit

Today, existing designs in different technologies can be retargeted and optimized to current technologies. TTL, PLDs or FPGAs in netlist or schematic form can be converted into newer FPGAs or ASIC technologies. Likewise, retargeting can be used to optimize schematics generated in the current technology. Schematic generators can be used to convert the results of synthesis or retargeting into readable schematics which the designer might find useful to check results. The VHDL simulator can again be used to simulate the final design after synthesis to ensure that all the pieces fit together. The same stimulus module written in VHDL can again be used.

ASIC foundries provide toolkits for many CAE systems which take the final optimized design out of the design database and convert it into its required format. Tools are also available to base-annotate the design with final timing numbers after the layout process. The same simulation process can then be used for final timing verification.

When the target chip technology is an FPGA or ASIC, the designer will usually have partitioned the design from the start to fit onto a single device. In these cases, the synthesis and retargeter tools will produce designs optimized for the technology of choice, and the designer only needs to output the design to the vendor using the toolkit provided.

When FPGAs are being used to prototype an ASIC, the designer may need to deal with partitioning and also fitting the parts onto the board which is compatible with the final ASIC. Design tools are also available to automatically and interactively partition PLD designs into one or more PLDs, select the best PLDs available which meet the designer's specifications, output each JEDEC file after partitioning, and automatically produce the final schematic of the partitioned multiple-PLD design ready for board layout. If the chip is being initially implemented as an FPGA for rapid prototyping or initial production, retargeting tools can again be used to convert the entire design into an ASIC for cost reduction.

Finding common ground

Experienced logic designers need a complete and integrated tool set which allows a mixing of top-down and bottom-up design approaches, letting the designer select the best approach for the problem at hand. Designers not yet experienced with VHDL synthesis or retargeting need the same environment so that they can gradually take advantage of the benefits of high-level design without also having to immediately change their entire design style.

Roland Mattison, synthesis product manager, Viewlogic Systems

ers are using VHDL to describe their designs conceptually at a high level and then relying on a synthesis tool to optimize the design in the target technology. Victor Duvanenko, a member of the technical staff at Truevision (Indianapolis, IN), is putting most of the digital logic of a PC add-in board into an Actel FPGA and then, after field-testing a few hundred prototypes, plans to reduce costs by migrating to a gate array. He chose VHDL because he had heard that it could be done painlessly.

Duvanenko synthesized to the Actel (Sunnyvale, CA) library using synthesis tools from Synopsys (Mountain View, CA). "It's not a good idea to do the gate array netlist first, since Actel speeds are so inferior to gate array speeds," warns Duvanenko. His prototype board has proven that the design methodology works, according to Duvanenko. More than two months were spent, he says, learning the trade-offs involved with VHDL, synthesis and the Actel antifuse-based FPGAs. A lot of time was also spent debugging the Actel library elements, according to Duvanenko.

Since Truevision's design goal is to directly replace the FPGA with the gate array on the board, the prototype and the ASIC have to be pin-for-pin compatible. "Pin compatibility between FPGAs and gate arrays can be a problem—you have to make sure there's a match between power and grounds." Though Duvanenko doesn't expect a problem with timing when migrating to a gate array, he claims that "nobody can guarantee a timing match between Actel and a gate array." When starting with an FPGA, a gate array can be technology overkill, he says.

The inability to preserve the timing of the original design has been one of the stumbling blocks to migration, especially for situations where a direct on-the-board swap is being made between an FPGA and an ASIC. To enable FPGA users to extract timing constraints from the original design when migrating to a full ASIC, Synopsys has recently enhanced its Design Compiler with Version 2.2. It lets designers with technology libraries for both the FPGA and the ASIC target technology transfer path delays as well as capacitance information.

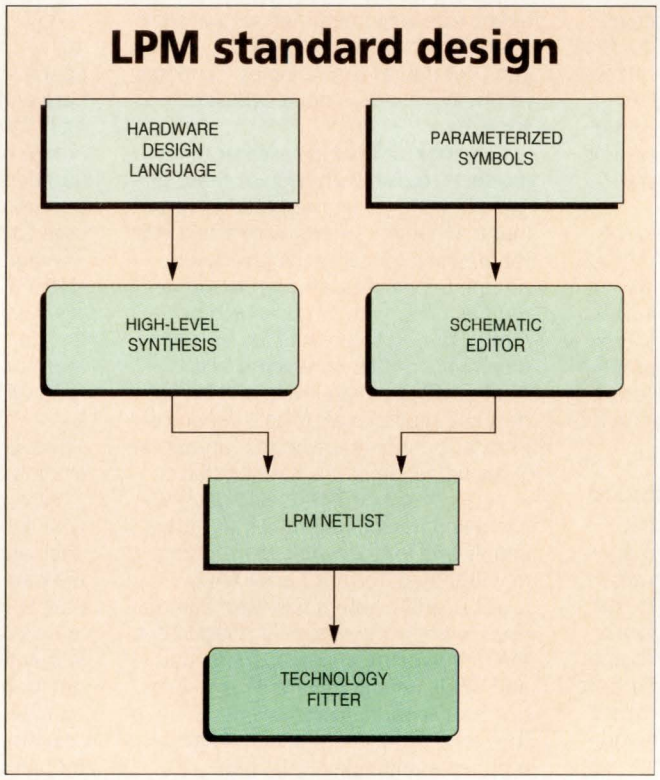
Think ASIC up-front

Tom Stall, hardware engineer at the Oki Advanced Technology Center (San Jose, CA), also entered his design description using VHDL so one design effort would cover both prototype and full ASIC. "If the design is going to be optimized as an ASIC and sold as an ASIC, it makes sense to start at the ASIC level," says Stall, who is designing a graphics product for a laser printer. His target technology is a 0.8-μm gate array for which he will most likely go to Oki Semiconductor. The prototype will have some 10-ns PLDs for the very fast section of the design, says Stall, a Xilinx LCA for a large section of the design that's not very fast, and maybe an Actel antifuse device. "The prototype may have a few extra parts in it, but I'd much rather design a very good ASIC than a very good prototype," he explains.

Using a Viewlogic Systems (Marlboro, MA) tool for schematic capture, Stall is writing VHDL at the module level. "Partitioning your design into modules gives you the advantage of synthesizing definable blocks," says Stall. With Viewlogic, the schematic ties together the individual blocks described in VHDL, Stall explains, so that the entire design is covered by one big netlist. "When I synthesize that netlist, I can do a system-level simulation on it."

There's no tool available today, Stall explains, that synthesizes VHDL to PALs, so he created his own tools to supplement the Viewlogic toolset. "My tools take a netlist and translate that to what looks like a source file for Minc," says Stall who uses the PGADesigner from Minc (Colorado Springs, CO). As he hands off blocks of logic to Minc, Stall is specifying the PLD part in which it's to be implemented. In the future, he plans to take a larger chunk of VHDL, translate it and let Minc automatically partition it. "If I were to use Abel instead of Minc, I'd have no choice—I'd have to specify the part myself," says Stall.

Minc's spring release of its Version 3.0 products will include a set of VHDL constructs for programmable logic synthesis, being jointly developed by Minc and CLSI Solutions (Rockville, MD). And Teradyne EDA (Boston, MA) is working closely with Minc toward a system that will let designers of large ASICs do a single, system-level description, independent of device implementation. In the meantime, ASIC-emulation pioneer Quickturn Systems (Mountain View, CA), addresses the problem of system-level verification by mapping gate-array netlists



A committee of silicon and tool vendors is pushing the Library of Parameterized Modules (LPM) toward standardization with the hope that its adoption might ease the task of prototyping in FPGAs and migrating to ASICs. The objective of the LPM standard is to facilitate access to FPGA and complex PLD architectures for designers who lack detailed knowledge of the various vendors' silicon architecture. LPM defines a set of 18 parameterizable modules to be used in constructing an EDIF netlist to describe a design. Designers adopting LPM could use entry tools completely independent of the target technology and later rely on synthesis tools to map the design to the target technology.

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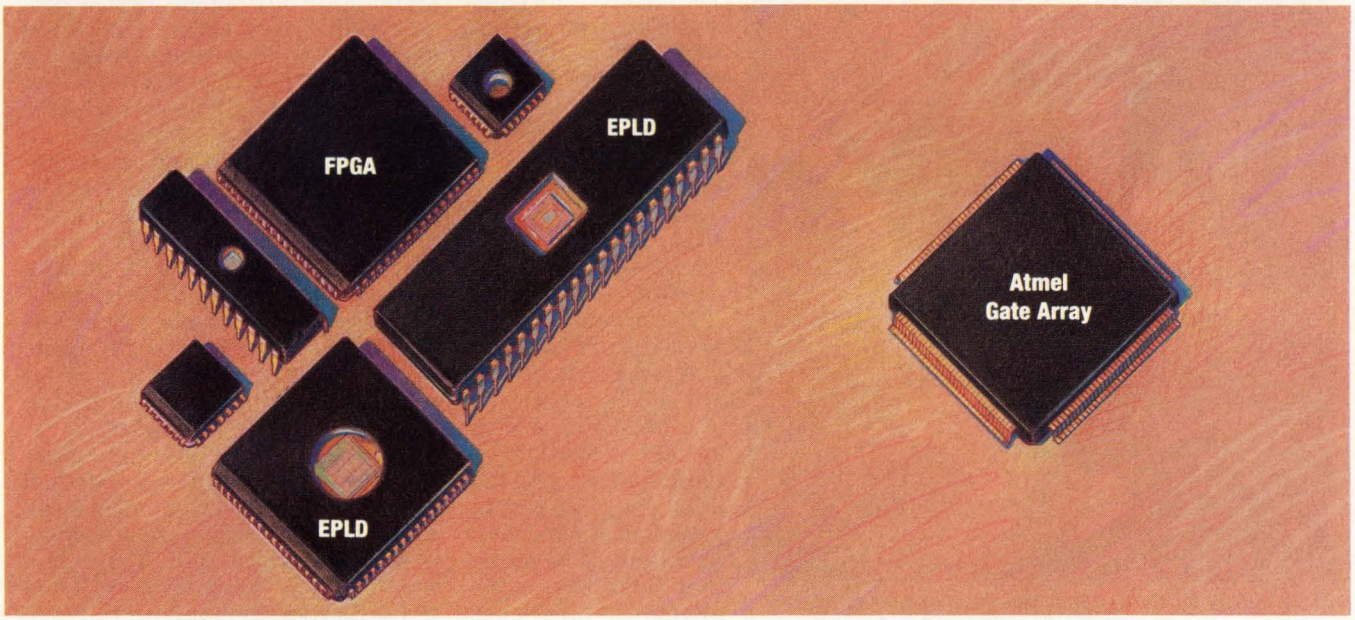

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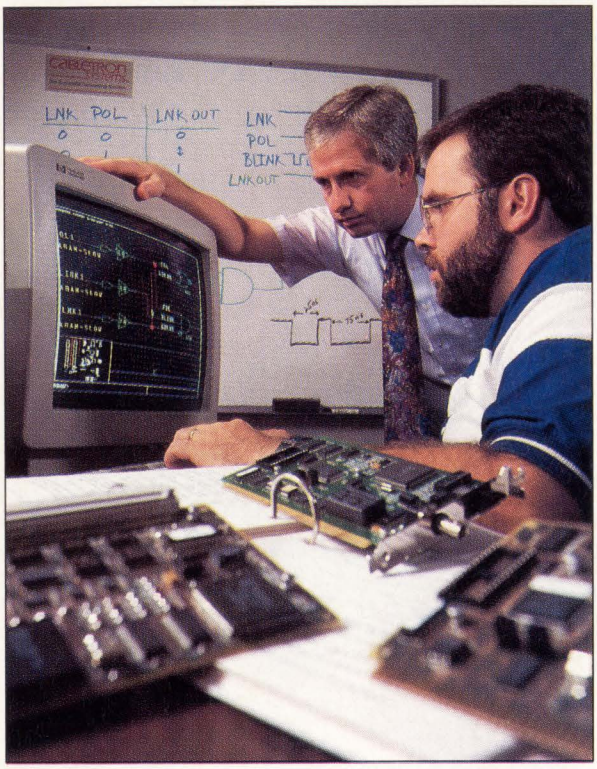
to a large bank of FPGAs in its RPM emulator, which in turn is plugged into the target system for emulation of the target gate array.

From PLDs to standard cell

The LOG/IC family of compilers from German vendor Isdata (U.S. headquarters, Monterey, CA) is popular with designers in Europe, where designers have also been susceptible to migration fever. In a development effort for the automotive market, designers at Doduco in Germany used LOG/IC tools to design a programmable intermittent windshield wiper relay that would adjust itself to the actual amount of falling rain. Designers selected a gate array for the final product, but for in-car trials, they implemented the circuit in a pair of ATV750 EPLDs from Atmel (San Jose, CA). The LOG/IC gates compiler translated the combinatorial and sequential logic of the PLD design into a multilayer gate structure which could then be implemented at a later stage as a gate array or even as a standard cell.



At Cabletron Systems, Bob Lapointe, manager of PC networking products (standing) and senior hardware engineer, Paul Sprague, work toward implementing their design for a LAN controller as a full ASIC. The Cabletron design team put four PALs, a bunch of external logic, plus added functionality into a Xilinx XC3030 FPGA and then migrated to an S-MOS gate array with the help of Viewlogic's Retargeter tool.

Doduco designers reprogrammed the PLDs to accommodate minor alterations and then made the step to a gate array without the risk of a redesign. The automatic logic synthesis and simulator of the LOG/IC software were just what they needed to get the job done, say Doduco designers who especially appreciated the strict separation between logic design and physical design during the test phase. In the meantime, Doduco reports that a German car maker intends to include the new relay in production starting with model year 1992. The lead time from start to production was just under six months, and it took only one year to cover development costs, Doduco reports. The company is now anticipating order volumes that would justify transition to a standard cell.

Performing conversions from FPGAs and gate arrays to standard cells is 60 percent of the business performed by ASIC Technical Solutions (ATS) (San Jose, CA), says president Kash Johal. ATS is an ASIC house that turns out multiproject, low-cost wafers. ATS users share multiproject wafers to reduce NREs (nonrecurring engineering expenses). Johal says the company has done 80 Actel conversions, 15 Xilinx, 25 LSI gate arrays, and is planning to do QuickLogic conversions in the future. ATS uses Exemplar synthesis in its conversion because, Johal says, no one else has come as close to a standard tool. "With Exemplar, users can design in VHDL or with LSI Logic libraries," says Johal. "They don't have to learn the vagueries of the different architectures."

ATS began only recently to do Xilinx conversions, and Johal says that "as long as we take great care, we don't have a problem." A difficulty with Xilinx, he adds, is that users sometimes go in and tweak a design after they've generated an XNF file, and then they don't go back in to update the XNF file. "If you have a design that's been tweaked manually, you have no database to work with," Johal explains. ATS does netlist translations into its macros—not blind translations, he says. "We have a two- or three-hour design review with the user, going through the schematics to see if he used any tricks and to decide what to do about it if he did."

Re-entering schematics

For his migration path, Alan Rubinstein, senior project engineer at 3Com (Santa Clara, CA), went from a 100-pin Xilinx LCA—first a programmable part, then a hardwired device—to a 136-pin gate array from NEC (Mountain View, CA) to reduce the cost of a 16-bit Ethernet adapter board. 3Com put the hardwired Xilinx part, five PALs and some random logic into the gate array. "The original design was very much influenced by the speed of the Xilinx parts," explains Rubinstein, "and we had to put the faster things outside." Rubinstein used Synopsys synthesis to convert equations to the same logic descriptions in Verilog format and then to translate to NEC gate-array technology. He used Viewlogic's schematic capture to re-enter those parts of the design that had been entered in schematic form. Having done no simulation whatsoever, Rubinstein had a problem when he went to a gate array. "I had to use Verilog to simulate the gate array to prove that what I had entered was correct," he says.

Rubinstein took advantage of Synopsys' synthesis for speed/area tradeoffs. "I knocked off a few nanoseconds from the critical path and did as well on the decode path as I could have by hand," reports Rubinstein, who admits that he has decode duplications in his design. "I had plenty of gates to play with and wanted to keep the architecture. The goal wasn't to be clever—I didn't have a simulation to compare against."

How long did it take Rubinstein to migrate from the hardwired Xilinx part to the NEC gate array? Count two months for the schematic capture and PAL equation phase, three-and-a-half months for the simulation phase of the design cycle, add half a month for validation with the original designer, plus another

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Integration through standards is key to migration

To reduce the cost of design migration, many system designers are turning to integrated design environments that support a wide range of design entry methods for many different implementation technologies. This is true both for the cost-driven migration of existing PLD and FPGA designs to FPGAs and ASICs, as well as for programmable-based prototypes with a planned ASIC migration. Support for different design-entry methods, ranging from schematics, to logic and state-machine descriptions, to register-transfer-level (RTL) and behavioral synthesis, lets the user use familiar tools and techniques and lets existing designs be readily migrated.

System-level simulation, particularly timing simulation, is required to verify that both the original and migrated implementations have the same functionality. The timing vectors generated for the PLD and/or FPGA implementation can be used to verify the ASIC implementation.

To address this, Abel-FPGA has been tightly integrated with packages from several major CAE vendors. Programmable logic designs specified using the Abel-hardware description language can then be synthesized into ASICs. Conversely, designs specified in Verilog, VHDL or schematics can be synthesized into PLDs, complex PLDs and FPGAs using Abel's device fitters.

Data I/O's PLD-modeler generates a VHDL or Verilog model from the JEDEC file used to program PLDs and complex PLDs from vendors like Altera, AMD and Atmel. These models, coupled with Data I/O's timing database, enable detailed timing simulation of designs incorporating these devices.

In Abel, the Abel-HDL description is compiled into a technology-independent intermediate form, generally Open-Abel. This is accepted as input by several technology-dependent synthesis tools often referred to as fitters. Multiple fitters are required as different FPGAs and complex PLDs have very different architectures and require radically different synthesis, optimization and physical design algorithms. The Open-Abel format can then be input to ASIC synthesis tools, for migration to higher-level ASIC devices.

No single synthesis tool can be expected to support both ASICs and the ever-increasing number of different FPGA architectures. Currently, the de facto intermediate form for most ASIC and FPGA high-level synthesis tools is a technology-dependent netlist of low-level gates and storage elements. Migration between different implementation technologies is generally accomplished via netlist translators which map a netlist, optimized for one technology, into a netlist acceptable for another.

A problem with retargeting at the primitive netlist level is that high-level functionality such as arithmetic operations and state machines has already been synthesized to gates. To obtain the best utilization and performance, different technologies often have different methods of implementing high-level functions. For example, one hot-state encoding works well in register-rich architectures such as Xilinx's FPGAs, but may not be appropriate in architectures where additional registers imply additional silicon. Unfortunately, once the design is at gate level, it's difficult to extract the higher-level functionality needed to make the best technology-dependent synthesis decisions.

One standard effort currently underway is the Library of Parameterized Modules (LPM), which Data I/O is pursuing with Abel connections. The proposed LPM standard will provide a more abstract, technology-independent interface between design entry and the technology-specific synthesis tools. The LPM intermediate representation is an EDIF 2.0 netlist of generic, technology-independent primitives. These parameterized modules include small primitives (AND, OR, XOR, INV, MUX, TRI), arithmetic primitives, tabular representations for truth tables and state machines, storage primitives, and pad primitives.

The higher-level intermediate representation provided by LPM can represent both parameterized schematics and the output of state machine, RTL and behavioral synthesis tools. Technology-specific device fitters can then efficiently map this logic to the underlying architecture. For some logic, such as arithmetic primitives, mapping to vendor-provided preplaced and routed macros may provide the best silicon usage and performance. Other logic will require additional synthesis and optimization, utilizing technology-dependent algorithms for tasks such as design partitioning, state assignment and register synthesis.

A technology-independent intermediate form lets the user utilize the most appropriate design-entry method for the module being designed and incorporate existing designs. Multiple technology-independent synthesis tools will enable efficient retargeting of the design to many implementation technologies including PLDs, complex PLDs, FPGAs, and ASICs.

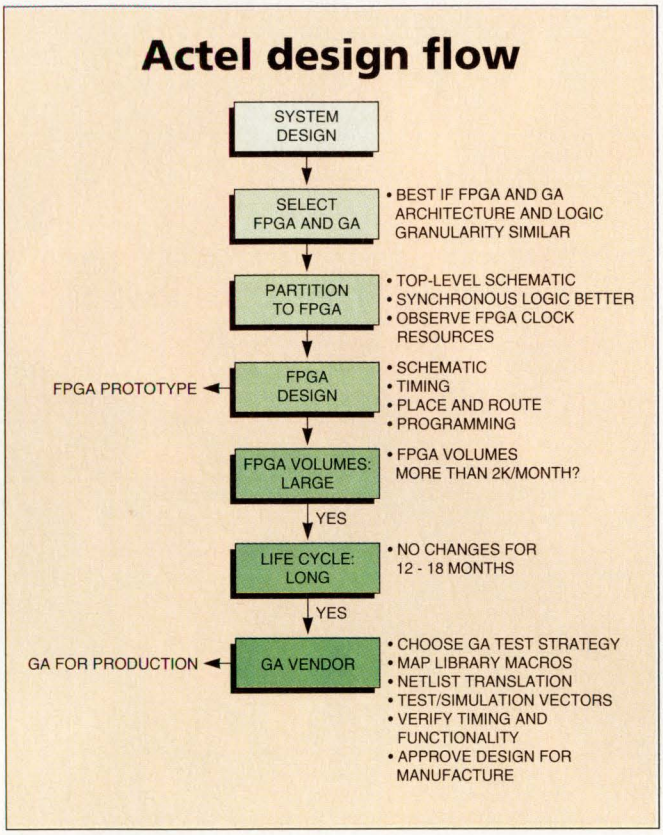
Karen Bartlett, senior software engineer, Data I/O

month for the hand-off process and test vectors. Rubinstein qualifies the seven months, though, by saying that he had to catch up on a lot of technology because he had gone from being a designer to a manager and then back to a designer.

Retargeting designs

Xilinx users at Cabletron Systems (Rochester, NH) skipped the interim step of going to a Xilinx hardwired device when cost-reducing their project, a LAN controller for a personal computer. Instead, they used the Xilinx FPGA for development with the up-front intention of going to a gate array from S-MOS (San Jose, CA). Bob Lapointe, manager of Cabletron's PC networking products explains, "The Xilinx hardwired device was not that attractive. It winds up that the piece price came out substantially higher than a gate array." Instead, the designers chose to use Viewlogic tools to move to the S-MOS gate array. S-MOS recently became the first gate array supplier offering Viewlogic's Retargeter FPGA conversion software.

The Cabletron design team had put four PALs, a bunch of external logic, plus some added functionality into a Xilinx XC3030. Although the design wasn't purely synchronous, the designers were able to use 75 to



The Actel design flow for migrating from an FPGA to a gate array makes clear that Actel emphasizes that designs turn out best when users early on try to match the FPGA to the gate array with regard to architecture and logic granularity.

80 percent of the Xilinx device. Top on the designers' priority list when migrating to an S-MOS gate array were silicon area as it related to cost and the ability to drop the gate array onto the board as a direct replacement for the Xilinx part.

Paul Sprague, a Cabletron hardware design engineer, explains that the designers were able to capture their schematics under Viewlogic for the Xilinx FPGA design, simulate, run test vectors, and then generate the Xilinx parts and put them on the board. At that point, the Xilinx schematics were passed off to S-MOS which ran them through the Retargeter. Sprague explains, "The Retargeter takes the schematics from the FPGA and automatically generates gate array schematics. That means that we can rerun the simulation and test vectors on the S-MOS gate array schematics. From the time we got the schematics converted over, it didn't take us long to create simulation files that matched or exceeded the Xilinx files," says Sprague. Cabletron released the end product to the market last month.

In a previous migration attempt, Cabletron had manually re-entered schematics. Like 3Com's Rubinstein, they had taken the physical schematics and reentered them into the ASIC format, "It took us weeks to debug the entry errors," says Sprague.

Marcus Julian, program manager at Fluent Machines (Framingham, MA), where everyone works on PCs, reports that his design team is moving to an Atmel gate array through third-party tools to reduce cost and power, as well as real estate, on a second-generation multimedia graphics board for an AT. Julian reports that designers threw together the first erasable programmable logic device-based multimedia board. "We didn't have time to simulate the complete system and wanted the flexibility to modify the design as a result of alpha testing and debug, as well as customer feedback," says Julian. "To reduce the initial design cycle, we partitioned the design into functional blocks which were then quickly implemented using 11 of Atmel's ATV2500 EPLDs."

Each Atmel gate array will replace three or four of the EPLDs on the AT board, says Julian. "It's essentially a repartitioning or repackaging as opposed to a redesign," he says. "We capture and compile; they convert; we have a design review; and then the actual physical design takes place. Atmel has promised that timing and exact functionality to gate level will be preserved," Julian continues. "Atmel assures us there's little risk—it's a very simple turn of the crank." In the meantime, the board has been released to alpha and beta sites with the EPLDs on it.

Sticking with the familiar

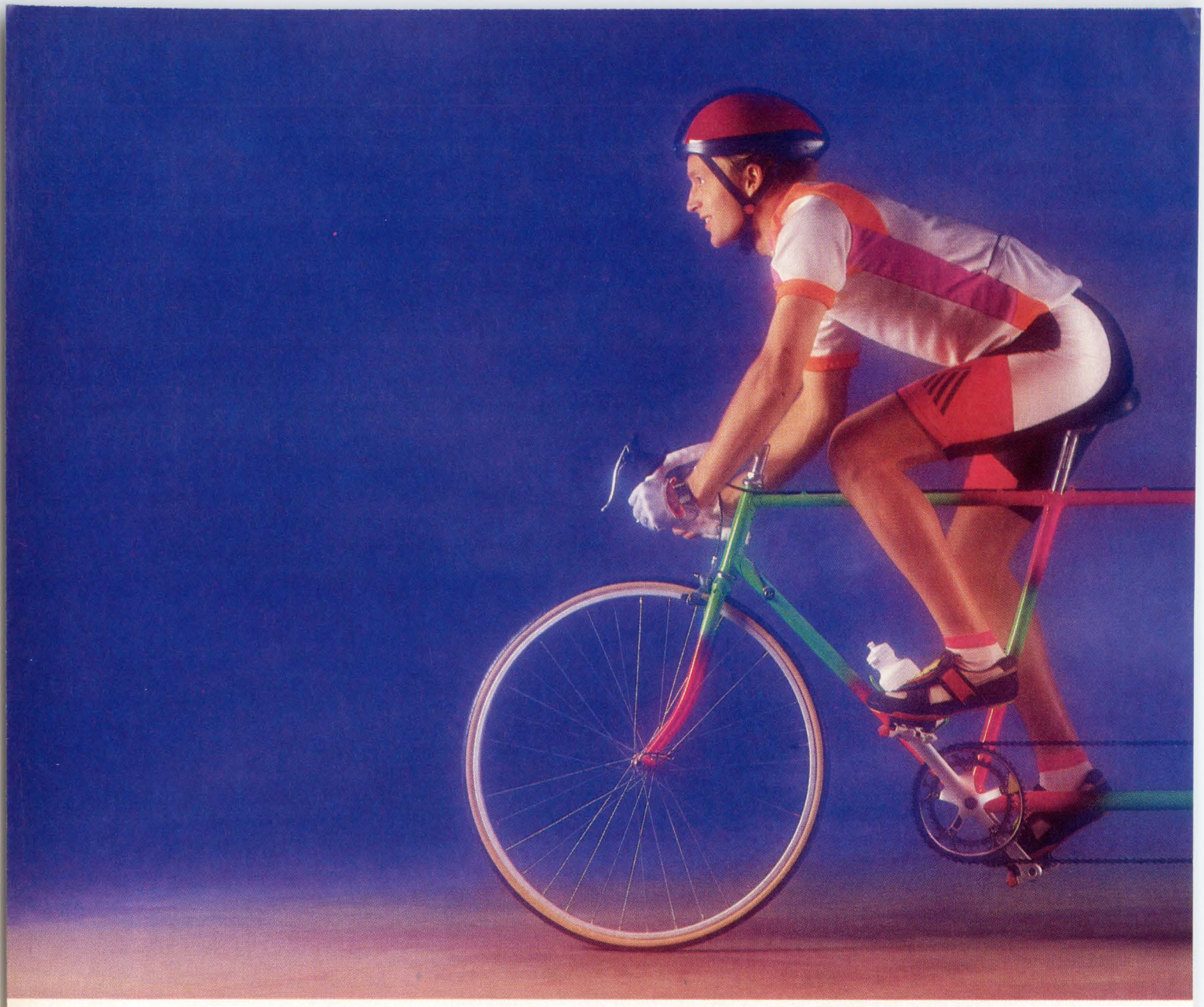
When it came time to convert a breadboard of 68 PALs plus TTL chips to a standard-cell-based design, engineers at Extended Systems (Boise, ID) contacted about a dozen vendors. Working exclusively on PCs, designers at Extended Systems make add-on boards which permit four to eight users to share a single laser printer. The project under discussion is a cell-based modular solution that will eventually go into many products.

As a starting point, the designers had the equations they used to burn the PALs and the schematics from which they had built the breadboard. According to Extended Sys-

PLD-to-gate array-conversion methodologies

Conversion Methodology	Gate Utilization	Timing Match	Comments
Logic Synthesis	Best	Low	Best used when performance improvement is required or when several PLDs are combined.
Deterministic	Moderate	Moderate	Eliminates internal timing concerns.
Timing Matching	Lowest	High	Eliminates both internal and system timing concerns.

When converting EPLDs and FPGAs to gate arrays, Atmel users can consider the trade-offs involved in these three conversion methodologies. Timing matching and deterministic conversions reduce potential timing problems whereas logic synthesis provides the highest gate utilization. If a customer wants to match the timing of the original FPGA/EPLD, the design is converted and delays added to the elements to slow down the gate array. All that a designer needs, Atmel claims, is a JEDEC file with good test vectors, and the conversion process can begin.



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FPGA-to-TGC100 migration program

Task/Deliverable	Mentor/Valid Users			Viewlogic/OrCAD Users
	Option 1	Option 2	Option 3	Option 4
Input databases	.ADL	.ADL	.ADL	.ADL
Simulation Print-On-Change (POC) file	N/A	N/A	N/A	User
TGC100 design kit required	Yes	Yes	Yes	No
TGC100 output schematic (TI provides)	Yes	Yes	Yes	No
Timing report output (TI provides)	Yes	Yes	Yes	Yes
Netlist functional verification (TI provides)	Yes	Yes	Yes	Yes
TGC100 area optimization (TI provides)	No	Yes	Yes	Yes
TGC100 speed optimization (TI provides)	No	Yes	Yes	Yes
Scan chains inserted (TI provides)	No	No	Yes	Yes
ATPG — 1-MHz patterns only (TI provides)	No	No	Yes	Yes
Fault grade report output (TI provides)	No	No	Yes	Yes
TI's hardware description laguage (HDL) created by:	User	User	TI	TI
TI's test description language (TDL) created by:	User	User	TI	TI
System timing verification	User	User	User	RTC with POC file (Optional)
At-speed TDL creation option	User	User	User	User at RTC (optional)
Back annotation after layout (TI provides)	Yes	Yes	Yes	Yes, with user at RTC (optional)
Cycle time/design *	1-2 days	2-3 days	4-5 days	4-5 days

* Option 1: Simple translation.
Option 2: Translation with optimization.
Option 3: Translation with automatic test pattern generation for Mentor/Valid users.
Option 4: Translation with automatic test pattern generation for Viewlogic/OrCAD users. The user has the option of IKOS verification using supplied Print-On-Change (POC) file.

All cycle times are in addition to the normal TGC100 cycle times. RTC = Regional Technology Center.

Texas Instruments offers a choice of migration flows from second-sourced Actel parts to TI's TGC100 gate arrays—netlist translation only, translation with optimization, and lastly, a design flow that includes automatic test pattern generation (ATPG). For a multiple-FPGA to single gate array migration flow, TI users must combine FPGAs into one design and submit a single netlist.

tems development engineer Bob Haines, some of the two dozen vendors contacted were willing to help with translating the equations and schematics to a cell library, but had little experience doing so. "And with some other vendors, we would have had to re-enter all the schematics, equations and JEDEC files by hand since the vendors offered no way to translate," reports Haines. The design team wound up going with Gould/AMI (Pocatello, ID) which "had the best price and the best interface," says Haines.

The Extended Systems design team started at the basic gate level and worked in small chunks from the bottom up. The first step was to send Gould/AMI the netlist they had developed using OrCAD schematic capture, plus JEDEC files for all the PALs, plus test vectors for the PALs to verify logic. The designers, who had simulated only at the PAL level, simulated the ASIC themselves at a Gould/AMI site. In the end, going from breadboard to standard cell was a two-month effort from start to finish, except for fabrication. "We turned out a chip, and it worked like a champ," boasts Haines.

When asked about Gould/AMI's netlist translation as opposed to other higher-level migration methods, Haines says, "My feeling is that Gould/AMI is providing a general-purpose migration path. With it, you can use what you're familiar with. If you don't have bucks," points out Haines, "you want to use whatever software you have in-house; not proprietary, high-end packages that force you to stick with them."

At Synoptics (Santa Clara, CA), engineers have done a dozen conversions through Gould/AMI, from prototypes to full ASICs. Steve Mullaney, product manager for Ethernet products, has converted Actel FPGAs to Gould/AMI gate arrays. Like Haines at Extended Systems, Mullaney is a proponent of sticking with the familiar if it gets the job done. "We have Viewlogic CAE tools, and we started to prototype in Actel devices about two years ago. We have all the libraries and we're familiar with them," Mullaney explains. Mullaney reports that it takes six to eight weeks to get prototype chips from Gould/AMI, but, in the meantime, products can be shipped with Actel devices.

Adhere to purely synchronous design rules, Mullaney advises. "The

Silicon vendor provides single point of contact

The variety of FPGA, gate array and standard cell products available on the market today lets system designers tailor development plans while remembering both product development and production cycles. The possibility of designing initial prototypes using FPGAs with ramp-up and production in gate arrays and standard cell provides the designer with the right design flexibility, schedule and cost at each stage of a product's life cycle.

Until now, once a design was implemented in one target technology, migration to a new technology was possible only with a manual redesign into the new target technology. As CAD tools become available to aid in the migration, designers are closer to their dream of designing independent of the target technology, choosing the technology when the design is complete.

Four migration steps

There are a number of possible steps and methods for migrating from one technology to another, each providing a different level of migration. Definitions are given here describing the four steps used in a circuit migration and discussing the conversion level that can be achieved. AT&T's SoftPath Tool is an example of a technology-migration system.

Netlist translation changes the syntax of a netlist from one format to another. It doesn't change cell types, libraries or circuit connectivity. While this is necessary to make a technology translation, it's also used for moving a design from one CAD tool or system to another. An example would be a translation of a tool-dependent netlist format to a universal format, such as EDIF (Electronic Data Interchange Format).

Library mapping converts each cell type in one library to one or more cells in another library. Preserving cell functionality is a minimum requirement. But meeting other constraints is possible, including matching performance, voltage levels (e.g., CMOS vs. TTL), drive, power consumption, etc. An example of a one-to-one mapping would be changing from the ATT3000 FPGA INV inverter to the ATT656 gate array L101 inverter.

Resynthesis takes a netlist with certain characteristics and transforms it into a netlist with different characteristics. Examples of these characteristics are area, performance, testability, or technology. Netlist resynthesis usually consists of two steps. First, a library mapping of sequential and other non-combinatorial cells to the target technology is performed. The combinatorial cells produced during the first step are then combined with all original combinatorial cells and transformed into a technology-independent format (e.g., Boolean equations). Logic resynthesis then operates on the decomposed logic, eventually mapping it into the target technology. This process coverts blocks of combinatorial logic into circuits that are functionally equivalent, but not necessarily a one-to-one conversion. It looks for conversions that may be superior to one-to-one mapping in terms of performance and area. For example, in converting an ATT3000 FPGA circuit to an ATT656 gate array circuit, logic minimization during resynthesis allows efficient use of the gate array library cells and takes advantage of the macro functions available to reduce the gate count.

Partitioning converts a random-sized block of logic, such as an entire chip or board design, into multiple blocks of logic of a desired size. A circuit might be partitioned from one large circuit to a number of smaller circuits to allow use of different technologies. A large standard cell design, for example, may need to be partitioned into many smaller circuits, each of which will fit into an FPGA for prototyping.

CAD tools aid migration

Recently, CAD tools have become available to perform these migration tasks. The AT&T SoftPath Tool is an example of how migration among FPGA, gate array and standard cell technologies can be accomplished. The goal is to provide technology resynthesis—the complete transformation of a chip implemented in one technology into chip(s) implemented in a different technology. Today, AT&T's SoftPath capability consists of software to migrate between ATT3000 FPGA and ATT656 gate array families. During 1992, AT&T will add the capability to perform standard cell to FPGA and standard cell to gate array migrations.

The SoftPath migration software, available on SUN 4 workstations, takes a netlist as input and provides a converted netlist as output. A single command line initiates the operation. The migration is virtually user independent, except when special blocks are used requiring user intervention. A RAM circuit that doesn't have a one-to-one match in the target technology may need the user to specify a replacement. Once the output is available in EDIF netlist format, the converted circuit design can continue on either the AT&T Design System, or on a third-party CAD tool and design kit of choice.

Netlist translation is used throughout the entire SoftPath system. For conversion operations to be completed, all initial netlists must be translated into a common netlist language; in this case, the AT&T Design Database (DDB) format. FPGA designs come into the process in XNF format, gate array designs are in EDIF and standard cell designs will be in either AT&T netlist format or EDIF.

Library mapping and resynthesis are used together by SoftPath to do the actual conversion. All combinatorial logic is decomposed into Boolean equations where it then undergoes logic optimization and synthesis into the target library.

AT&T is currently developing software that automatically partitions standard cell netlists into multiple FPGAs. The partitioner works from the mapped FPGA descriptions and produces n+1 netlists, one for each partition and one for the top-level connectivity. All the user specifies is the target part number (i.e., ATT3030) and a utilization factor to account for place-and-route overhead.

Point-to-point tools are currently the only effective way of doing the technology resynthesis job since many issues can be resolved automatically. For example, non-logic mappings, such as mapping pads, I/O buffers and special cells, can be performed by the point-to-point tool, whereas general synthesis tools require user intervention. AT&T believes the SoftPath methodology is the most efficient and affordable way to provide a quality migration path between technologies.

R. L. Bailey, ASIC product-line director for AT&T Microelectronics, also contributed to this panel.

Lauren L. Brust, supervisor, gate-array development group, ASIC libraries and technology, AT&T Bell Laboratories

ASIC MIGRATION

Actel device will work in the breadboard, but when you transfer the design to a faster gate array, you'll have race conditions if you don't stick to synchronous design rules."

Broadening support

Also addressing migration issues, GEC Plessey Semiconductor (Scotts Valley, CA) is looking to eliminate the need to generate test vectors, as well as all pre- and post-engineering simulation when converting from one technology to another. In the meantime, GEC Plessey has recently released its second-generation ERAs (Electrically Reconfigurable Arrays). GEC Plessey's and Toshiba's (Irvine, CA) FPGA technology has been licensed from Pilkington Microelectronics in England. Place-and-route software for the GEC Plessey ERAs has been rewritten, having been a bust the first time around, and a PLD-to-ERA synthesis tool has been added. GEC Plessey offers a migration path from FPGAs to its QuickGate gate array family. Toshiba's FPGA design philosophy, it claims, has been to design its FPGA so that it can be mapped closely to the target ASIC.

National Semiconductor (Santa Clara, CA) will also be providing a path from its MAPL complex PLD products to National ASICs, but users will also have the ability to go to any other solution through open formats that National has adopted. MAPL users will be able to go to any gate array vendor that supports Synopsys, for instance. The Synopsys Test Compiler figures largely in Texas Instruments' (Dallas, TX) FPGA-to-gate-array migration solution for commercial and military users of Actel FPGAs, which TI second-sources. Military users can also go to the United Technologies Microelectric Center (Colorado Springs, CO) for conversion from Actel FPGAs to UTMC's rad-hard SystemASIC gate arrays. AT&Ts migration path is discussed in "Silicon vendor provides single point of contact," p 93. ■

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Postscript

The enthusiasm of users I spoke to while doing this article has convinced me that migration is, indeed, a user-driven technology and not a marketing strategy on the part of silicon and tool vendors. With enthusiasm alone, though, users are likely to waste both time and money rather than achieving the time-to-market and cost-reduction benefits that prototyping and migration are all about.

It's clear that where a strong user demand exists, vendors will make tools available that may not yet be equipped to do the job. And yet, it may not be a good bet to wait until the tools mature if competitors are, in the meantime, figuring out how to migrate successfully and thus how to release cost-effective end-products to market. That puts the burden on you, the user, to be methodical and disciplined—even painstakingly so—in your approach to migration.

It's up to you to take an up-front look at the alternatives and trade-offs involved. There's no single migration methodology that will apply successfully across a broad user base. You need to figure out what migration path is best for you by planning a long-term product strategy and by setting your design priorities.

While you're doing that, I encourage you to come up with a checklist for vendors—requirements that you need to reach your design objective. Don't hesitate to ask vendors to put you in touch with their users who have successfully migrated designs. Have a list of questions ready for them, too. I wish you luck and Merry Christmas, too.

Barbara Tuck Egan

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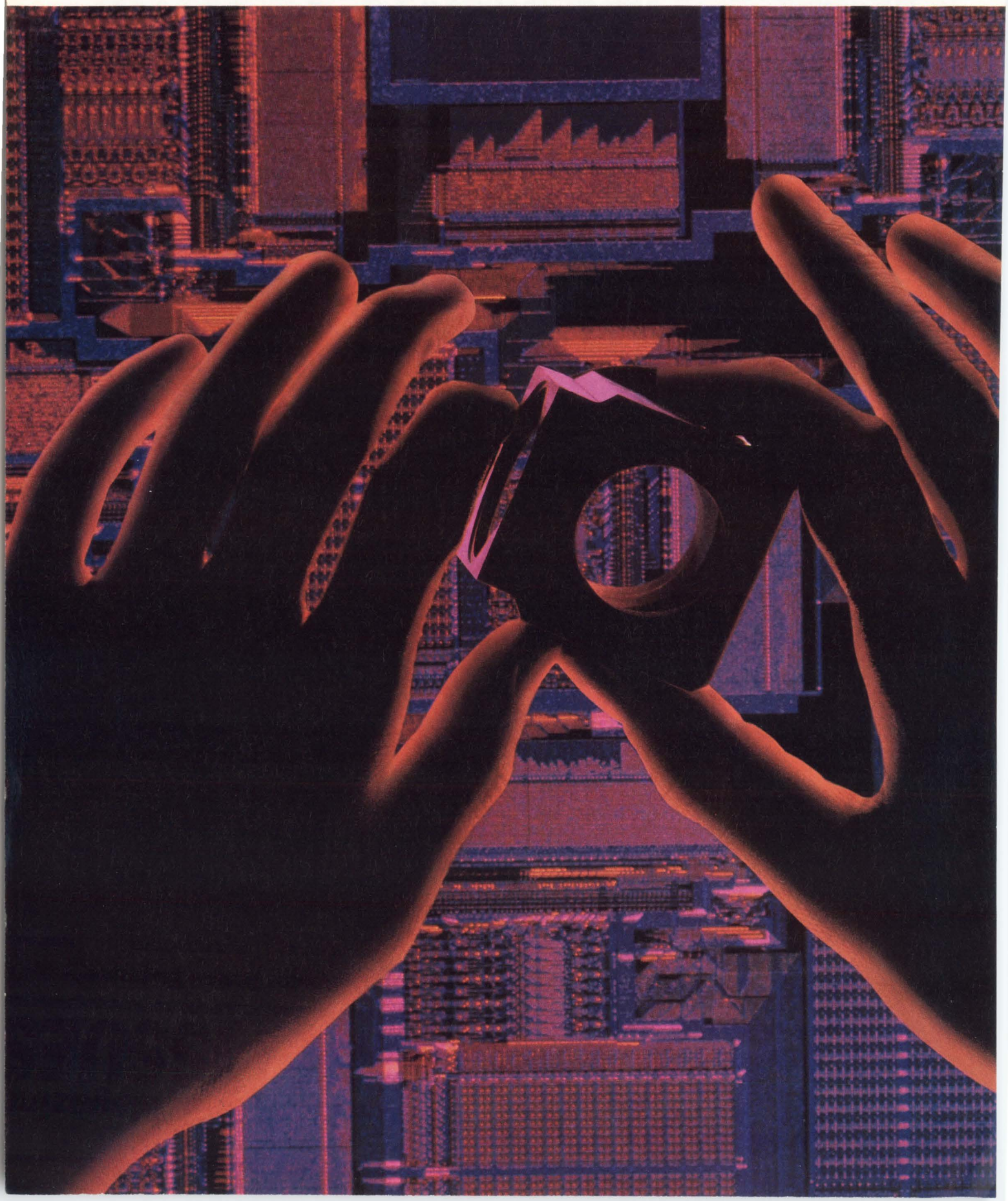

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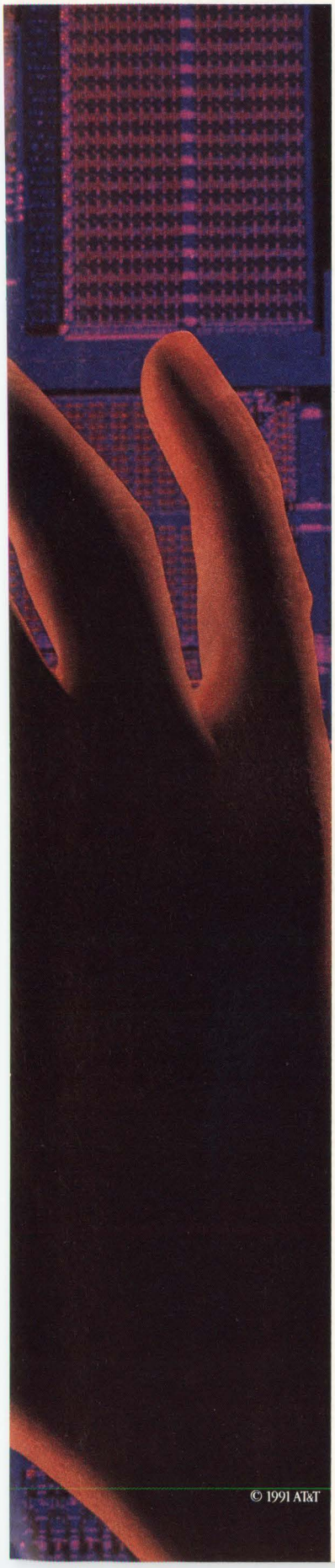

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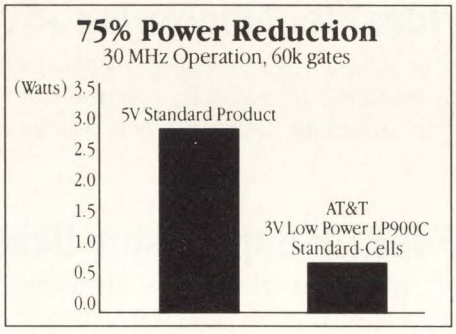

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CIRCLE NO. 55

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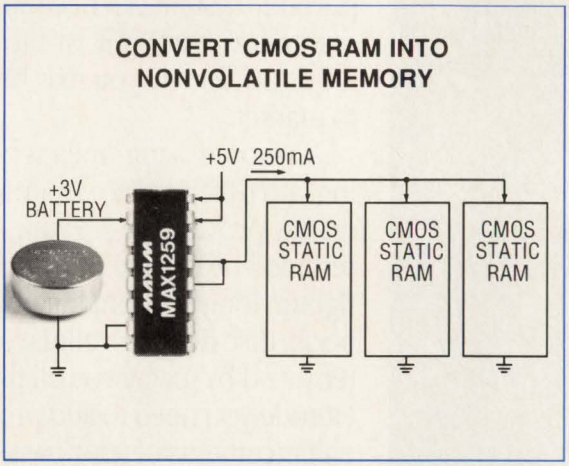

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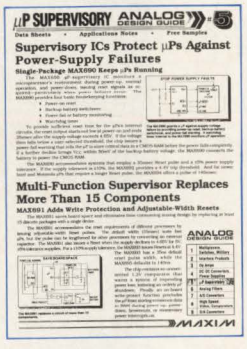
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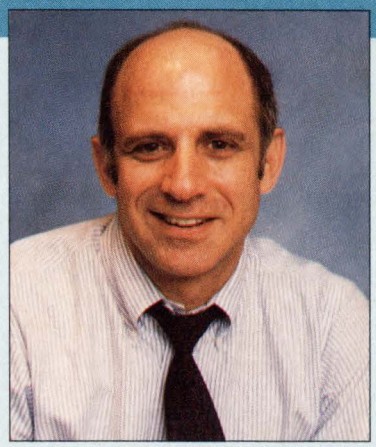

The simulator Superbowl: BCTM revisited

More than a year after simulation tool vendors presented their results at the September 1990 Bipolar Circuits and Technology Meeting (BCTM) in Minneapolis, MN, engineers are still talking about it. Though not intended as a competition, many regard the BCTM challenge as the "Superbowl" of simulator contests. Tool vendors are still debating "who won"—who has the fastest mixed-signal simulator, the most accurate simulator and who was able to most thoroughly document what was done to the audience's satisfaction.

On one level—a "feel good" level—everyone won. Every tool vendor that participated in the challenge felt stimulated and excited about what its tools could accomplish. "We really enjoyed participating in this," says Kevin Jorgensen product marketing manager of Viewlogic Systems (Marlboro, MA), who invested 10 man-weeks in the project. "The customer won," says Kim Hailey, vice-president of engineering at Meta-Software (Campbell, CA). "The BCTM challenge demonstrated the feasibility of commercial mixed-signal simulation. It was no longer a laboratory curiosity."

Even John Shier, manager of technology development at VTC (Bloomington, MN), who mounted the challenge under the auspices of the IEEE, acknowledges that all the manufacturers who participated "demonstrated usable products."

But while Shier and the IEEE refused to declare "a winner" (to endorse one product over another), there are lingering feelings among CAE tool vendors and potential users as to "who really won BCTM" and why. The battle lines seem to be drawn between tool vendors who modeled the BCTM circuits on the behavioral or macromodel level, and those who employed "direct methods," actually calculating the response of each transistor in the circuit with node-level matrix equations. While the behavioral models returned simulation results much faster, Spice advocates believe a great deal of complexity was sacrificed.

The BCTM challenge was essentially a gauntlet thrown at the feet of CAE tool vendors. Shier was hoping to create a "benchmark" for mixed-signal simulation, similar in intent to the benchmarks used to evaluate the Mips rate of dissimilar computers. Six months prior to the BCTM, he presented CAE tool vendors with a modified version of the AD574, a widely-sourced 12-bit A-D converter that uses successive approximation techniques. "Here guys," Shier seemed to say, "simulate *this*."

In the operation of AD574, an input comparator weighs bits one at time and places them in a successive approximation register (SAR). Data in the SAR is converted by a D-A converter back into a voltage which is used to reset the reference level on the input comparator. Each bit handled by the converter, from the most significant bit (MSB) to the least significant bit (LSB) will require the comparator to take a progressively finer slice of the input voltage. The MSB reflects some number greater or less than one-half of the whole analog input voltage range. The LSB, for a 12-bit A-D converter, represents 1/4096th of the input. Because each weighted bit is registered and recycled through the SAR one by one, it takes at least 13 clock cycles to generate the full 12 bits.

The gauntlet is thrown

In his challenge, Shier provided both the block- and transistor-level circuits for the A-D converter and asked tool manufacturers to work at this level of detail. The complete process, Shier felt, would require the tool vendor to enter the circuit from scratch into a workstation database, simulate the circuit and analyze the performance of the circuit based on what the simulator revealed. Ideally, a final report would document the entire process of entering, simulating and analyzing the circuit, and give potential customers a real feeling for how "easy or difficult" the task was to complete. Of special concern were the simulation waveforms produced, the required run time on the computer and the documentation produced.

Challenge participants included Analogy (Beaverton, OR), Cadence Design Systems (San Jose, CA), Electrical Engineering Software (Santa Clara, CA), Integraph (Huntsville, AL), Mentor Graphics (Beaverton, OR), and Viewlogic Systems. Meta-Software participated as the HSpice provider for both Mentor and Viewlogic.

The results indicated some simulators were faster

than others, some provided a deeper level of analysis than others, but there was little basis for an "apples-to-apples" comparison. For example, there was no standardized workstation platform among the challenge participants, so many claims for speed must be balanced against the Mips rate of the workstation used. Some manufacturers put a large team of engineers to work on the benchmark and began their investigation months in advance of the meeting. Others took the challenge as a part-time, after-hours activity and responded to the challenge with a few workers in the wee small hours before the meeting.

At face value, simulators using "behavioral" models, like Analogy's Saber (or Spice macromodels), seemed to return simulation results faster (i.e., with shorter run times) than simulators that went through all the node-level computations inherent in Spice. Where Saber goes head-to-head with Spice on speed—as on the challenge posed by BCTM—it usually wins. On the transistor level, Saber simulated all 13 clocks of the 12-bit A-D converter in 75 minutes; HSpice took 47 minutes—for one clock. On the abstract behavioral level, Saber simulated the entire 12-bit A-D converter in 20 seconds. HSpice took 140 seconds—again, for one clock.

Critics of the Saber approach to mixed-signal simulation, however, argue that it represents a trade-off between accuracy and speed. Saber, in fact, is more appropriately called a "modeler" than a "simulator." Its accuracy is entirely a function of the models in use. It's possible, for example, to tweak the accuracy of Saber by embedding a set of matrix equations in the model. However, a good deal of Saber modeling activity will replace matrix equations with algorithms (i.e., software *approximations* of a process). A good algorithm will often bring you to within 1 or 2 percent of a full matrix calculation, but with a fraction of the computer run time. But critics of the algorithmic approach—BCTM participants and competitors—will argue effectively, *1 or 2 percent isn't good enough.*

Analogy's position was perhaps analogous to the San Francisco 49ers first Superbowl victory of the 1980's. They maintained the lead despite a strong second-half showing by the Cincinnati Bengals—but the Pontiac Silverdome where the Superbowl was held was packed with booing Cincinnati fans. The 49ers left the field feeling angry rather than celebratory, and would have to demonstrate their strengths as a team (i.e., prove that their January 1982 Superbowl victory was not a fluke) many times in following years.

In Analogy's case, its Saber simulator demonstrated a clear speed advantage over the other kinds of simulators, but its demonstration modeled transistors and other A-D converter components as behavioral or block-level elements. *Boo, boo,* in the minds of the Cincinnati Spice fan, *if you're not struggling with the math, if you're not doing the node-level calculations, you're a bum.* "If you hide complexity to gain speed," says Hailey, "what did you hide?"

Even Shier, who moderated the original event, now admits his bias as an IC designer is toward node-level computations. "Those using macromodels went fast," he says, "but they missed a lot." Real-world phenomena such as glitches, dc offsets and noise were often smoothed-over in the macromodeling process.

Shier points out that there's a large feedback loop in every successive approximation converter (the contents of SAR are fed back through a D-A converter to an op amp which resets the level on the first trip comparator). All the simulators, he found, did a fine job of modeling the feedback loop, but only the Spice-based simulators uncovered the inherent instability of the op amp-comparator pair. (Algorithmic simulators, he suggests, missed the capacitor poles in the right half-plane of the D-A converter circuit.) Moreover, dc bias was critical here, Shier insists, but not everyone was dealing with it. "Chip designers probably feel more comfortable with 'down and dirty' transistors," Shier sums up, "board designers probably feel more comfortable with macromodeling."

Analogy isn't thrown by these boos from Cincinnati. Dr. Ian Getreu, Analogy's vice-president in charge of modeling, suggests that there are several different functions a mixed-signal simulator may perform during the course of a design project. One function is to test system-level concepts with block-level models. Another function is to test designs with different components. A third function requires the models to predict the performance of a new IC before it's fabricated. Each level requires a different degree of modeling accuracy, and a deeper involvement with the effects of frequency, temperature, power supply voltages, etc.

The movement toward higher-level modeling

With industry-wide emphasis on "system-level" design, however, it's becoming imperative to raise the level of abstraction in both describing *and* simulating analog and mixed-signal systems. While some might argue that the goal of this movement is to improve the computer run time for simulation, others would argue that the high-level description presents a way to manage increasing system complexity, and to test system-level design assumptions. Not everyone will agree on the best method for raising the level of abstraction in analog, and this issue will intensify in the next few years.

But the BCTM challenge still strikes a resonant chord in the design community. One CAE tool manufacturer not invited to participate but whom nonetheless took the BCTM challenge to heart, is Dr. Paul K.U. Wang, president of the CAE division at Contec Microelectronics USA (San Jose, CA). Using Spice macromodels and an algorithmic retuning of Spice3C, Contec modeled the entire 12-bit A-D converter in 99 minutes (5,940 seconds) on a Sun-4. (Digital circuit elements—the SAR, DLatch, and comparator output—were analyzed in 426 seconds.) Wang's white paper on the subject was presented to potential Contec customers, even as the impact of the BCTM presentations are still being assessed.

If the competition were re-run today, would its participants use the same set of tools? Or have different things to say? Since the BCTM challenge went out, there have been several revisions and tweaks to

Spice, all dealing with speed. One modification, like Cadence's Spectre simulator, represents an algorithmic tuning of Spice's direct methods. The other, like Valid's Profile modeling language, simplifies the construction of Spice macromodels.

Spectre proposes to be a re-make of Spice, by the same Berkeley professors and students that did the work on Spice3. Spectre uses existing Spice models, but replaces many of the node-level matrix equations with carefully-tuned algorithms. Thus, Spectre claims a 10× improvement over Spice, with comparable accuracy and better time step control.

Valid's Profile simulator tool is intended to make it easier to generate Spice macromodels. It provides a means for easily entering formulas and macro-level transfer functions on a workstation screen. A compiler assembles these as Spice-compatible macromodels. Like Saber, this product is targeted toward designers who need to test system-level concepts with a behavioral model, and ease-of-use is one of its main features.

The ease-of-use issue, however, was never properly resolved with the BCTM challenge. Each tool vendor demonstrated what it could do with its own tools. How a tool user might respond to this challenge is still uncertain. Hailey likens some tool promotions to the kitchen knife advertisements that show up on late-night television: " 'It slices, it dices'," he jests, " 'but all *you* can do is cut your finger.' " The next challenge, he suggests, might bring in more tool user experience.

Panel discussions at October's Analog and Mixed-Signal Design Conference (Santa Clara, CA) did little more than rake over the coals on a still smoldering debate. But one role the conference can play in its next incarnation (1992) is to put down a new challenge to match the one offered a year ago by Shier and the IEEE. In the months to come, we will distribute a mixed-signal circuit and challenge tool vendors—and tool users—to enter and simulate it. The circuit we imagine will be largely representative of the kind of circuits mixed-signal IC vendors are currently struggling with. Challenge participants will have about six months to work out their designs, and the findings will be presented at next year's *Computer Design*/Miller-Freeman conference.

Stephan Ohr is editor/publisher of the monthly newsletter, Mixed Signals.

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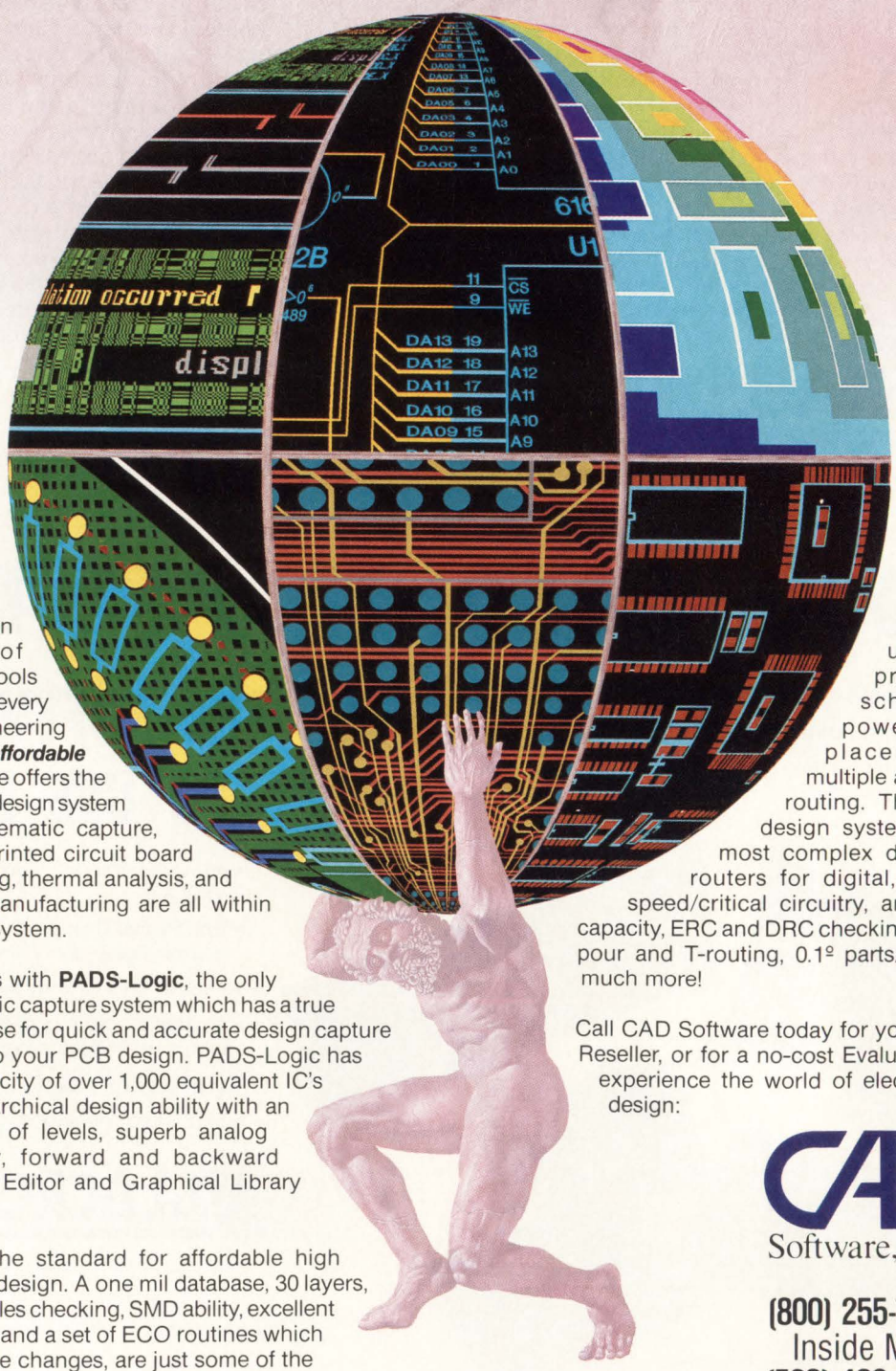

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CIRCLE NO. 58

In search of the optimum device programmer

III

Choosing a universal device programmer involves a bit of research. For the most part, they all seem to work fairly well; that is, they program and verify parts according to the device manufacturer's specifications. Quite often, the programmer manufacturers actually refine the programming algorithms for the device manufacturers. The decision-making criteria when choosing a programmer, therefore, are price, vendor reputation, features of the programmer, ease of use, stand-alone vs. PC-hosted operations, efficiency of software, and number of devices supported—not necessarily in that order.

Originally, simple low-cost programmers were all an engineering department needed to keep up-to-date. PROM and EPROM programmers were relatively simple devices which handled a few similar devices, all with essentially the same architectures and technologies, although from various manufacturers. Programmable logic devices also came from a handful of device manufacturers who made similar parts with similar architectures using similar fabrication technology.

This is no longer true. On the up side, the introduction of more and more parts with diverse architectures and technologies have given engineers more choices with which to match more specific applications. Higher-speed parts make it possible to use PLDs for more-demanding tasks. In addition, higher-density parts, with new and improved architectures, let PLDs incorporate more logic then ever before to offer the benefits of higher functional integration that had been the realm of low-end gate arrays.

While EPROMs, for the most part, have retained the same personality although with changes in their densities, the diversity of PLD parts, technologies, architectures, and tools has made PLD design more challenging. Not only do engineers have to become more familiar with many more parts, architectures, trade-offs, and design techniques, they must also be involved in the logistics associated with PLD design and programming.

While it's still true that common subsets of simpler parts, such as PALs, provide similar capabilities without requiring much added expertise, the down side is that the newer and improved parts require that designers be aware of all the parts they can use and program in-house without having to invest in more advanced tools and programming equipment.

What's more, as new parts come on the scene, third-party development tools and programmers are not always ready to support them. So, engineers who want to take advantage of the latest technology must often acquire specialized development tools and programmers (often from the device manufacturers) to use this new technology.

The result is a slew of specialized hardware and software tools needed to develop, program, verify, and test parts. This is no bed of roses for engineers and engineering managers. Engineers must familiarize themselves with the parts, tools and software personalities. Managers must keep projects on time and on budget, and the cost of using the newest technology may be too high for conservative managers who don't want to put all their logical eggs in one logical basket.

Back to the future

When programmable devices were in their infancy, programmer manufacturers took the logical approach of creating relatively inflexible programmers, specialized to certain families of parts. As new parts came out, adapter modules were added to the original programmer, making it possible to upgrade programming capabilities at a lower cost than buying an entirely new programmer.

While this worked well for a while, problems arose. First, older PLDs were made, for the most part, using bipolar technology. When CMOS parts started to appear, different voltage levels, timing requirements and programming algorithms became necessary. While some parameters could be handled easily with adapter modules, many couldn't, and the adapter modules became as sophisticated, or more so, than the programmer itself.

The second problem arose when new approaches to connectivity were introduced to the PLD pile. All early PLDs used fusible links as the connecting elements. This approach worked well for the programmer man-

ufacturers because programming algorithms were similar. To the engineer, however, this meant parts were one-time programmable, used rather large amounts of silicon area for the relatively small amount of logic they held, and were not fully testable on incoming inspection.

Today, devices using EPROM-, EEPROM- and RAM-based fuses, as well as anti-fuses, are readily available. This is advantageous to the engineer because reusability is high and complete incoming inspection test is possible. But for programmer manufacturers, it's a nightmare. To combat this proliferation of devices, programmer manufacturers started developing more flexible pin driver circuitry. Specialized pin driver designs for the newer breed of universal programmers were often implemented as ASICs, hybrids or other more-costly technology compared to the standard parts and through-hole technology previously used.

This solution worked well and is a stalwart today, but newer parts are pushing beyond the limits of pin driver technology. PALs, now available in ECL flavors, offer I/O level schemes entirely different from the widely used bipolar and CMOS parts. Also, as parts become faster, older pin drivers may not be able to verify a part's operation at speed. Already, 5 ns and faster parts are here, and the cabling and socketing alone can skew signals beyond workable verification. While the programmer manufacturers' answer was to offer more sophisticated pin driver electronics, this translated into higher costs per programmer and engineering teams had to byte the silicon bullet and purchase these high-priced programmers.

Stocking every socket

The wrinkles didn't stop there, though. New packaging technology has meant that universal programmers had to supply every type of socket required on a single programmer, or use specialized adapter modules. Special socketing schemes again helped drive the prices of truly universal programmers up even higher.

Related to packaging, but still a separate issue, is automated parts handling. Even if the programmer manufacturer has done its homework and kept up-to-date with the plethora of parts and packages, it was apparent that manually programming, verifying and testing each part was not feasible. A design that uses more then one PLD multiplies the problem, because inventories must include varieties of programmed and unprogrammed parts.

The FPGA presented yet another challenge to programmer manufacturers because the densities and architectures were so different from anything yet encountered. To overcome this, programmer manufacturers are trying to make pin driver technology as inexpensive as possible. Typically, 40- to 80-pin drivers have been available, but as parts emerge with higher and higher densities and pin counts, this may not be enough.

A solution to this problem is a return to adapter modules. Many programmer manufacturers are finding that a universal programmer incorporating every conceivable socket is too expensive an approach. What's needed is a lower cost per pin and a more flexible socketing scheme.

Movement on the evolutionary chain

A solution to this problem that's gaining momentum is "in-system" programming. Boards are stuffed with unprogrammed parts and a special in-system bus is used to program and verify each part during production. While this solves many of the logistical and cost problems associated with individual programming runs, labeling, inventory, and tracking, the design engineer who must work within a tight set of constraints has new problems to solve.

First of all, a way of isolating the PLDs from other circuitry is required. The generally high-voltage programming pulses used can destroy other parts connected to the PLDs. Jumpers and special headers are required to isolate the PLD programming power and signals.

This also means that another header or connect scheme must be added to a printed circuit board (PCB) for this purpose. For many applications, this is acceptable, but, when density is pushing the limits, an extra connection scheme uses valuable board real estate.

To complicate this even more, every signal pin must be driven and monitored at speed if the part needs complete verification after programming. If a design uses five 20-pin devices with 18 signal pins each, this translates into the need to isolate and connect up to 90 signal lines. With some PLDs using 68-pin packages, it's easy to see how this can add up to a big headache.

What's more, high-performance designs often require multilayer boards, ground plane isolation and transmission line modeling and impedance matching. The extra needs of in-system programming may such designs impossible. Nevertheless, programmer manufacturers are making headway in the fight against high-cost, quickly outdated programmers. While lower-cost, less-sophisticated dedicated programmers can minimize the risk, engineers don't want to be shackled by this limiting factor. For example, an engineer designing a very dense and fast circuit board may not be able to use the parts for which programming support is available in-house. At some point, a universal programmer may be the best approach, even though this represents a more-costly initial investment, and there are no guarantees that the programmer will meet future needs.

Dozens of companies make device programmers today. Some just for memory devices, some just for PLDs, some for both, and some encompassing nearly every part available. Instead on discussing every solution provided by programmer vendors, let's look at a few of the key players and their approaches to meeting a design team's programming needs.

Data I/O

Data I/O is one of the oldest and largest device programmer manufacturers. Its family of programmers includes higher-priced universal programmers which

can be linked directly to parts handlers, as well as lower cost universal programmers which are flexible and satisfy the needs of most design groups.

In addition to the original Unisite and the newer, lower-priced 2900, Data I/O is introducing the 3900 programmer. The 3900 features Data I/O's proprietary modular socketing technique which handles DIP and surface mount parts and eliminates the need for costlier adapters. A base board uses a "Squirt Pin Array" which has signals delivered via relays through a "matchbook," a plastic template for the part to be programmed. This technique assures positive contact without straining or bending any of the delicate leads.

Like the 2900 and Unisite, the 3900 is capable of performing detailed tests on itself and the parts to be programmed. Blank tests, incorrect insertion tests, already-programmed tests, and illegal bit tests are but a few of the assurances the 3900 provides along with the ability to force test vectors to the parts (included in the JEDEC files which are downloaded to the programmer). In addition, auto calibration keeps critical power supply levels within specification and assures that the programmer isn't the weak link in the production cycle.

All three programmers can be driven via a host computer (over its serial port), a dumb terminal or a remote computer. PC-based software is included which helps automate the power-up defaults, device selection, file uploading and downloading, data format selection, and so on. In its standard configuration, the 3900 provides support for 48-pin devices, expandable to 84-pin devices. A 3.5-in. floppy disk that comes with the unit holds the programming algorithms for the various parts that are supported. In this way, regular updates are as easy as switching floppies. Standard 128 kbytes of programmer memory is expandable to 2 Mbytes. Prices start at about $5,500.

Logical Devices

In the past, Logical Devices' Allpro family of programmers has been interfaced to a host PC using an interface card. It's now introducing the new Allpro-88 XR programmer which extends the Allpro family and provides more advanced features. Like earlier Allpro programmers, the 88 XR can talk to a host PC through an interface card. But unlike the earlier units, it also provides a serial port (RS-232), a parallel port (printer type) and a SCSI port. This lets the unit talk with other host computers like the SUN, Apollo, HP, DEC, and Macintosh machines.

The Allpro-88 XR uses a universal socket adapter for both DIP and PLCC devices (from 20- to 84-pin). Using the company's proprietary DAC-Per-Pin approach, each of the supported 88 pins can be driven and sensed to meet the demanding requirements of the different device manufacturers. It also includes a built-in front LCD panel display and keypad. This permits stand-alone operation for the over 3,000 devices currently supported. A 3.25-in. floppy drive in the unit can also be used for future upgrades and support of new parts and algorithms.

A key feature of the new Allpro programmer is the object-oriented graphical user interface (GUI). The "MAC-like" resizable windows can be accessed under Microsoft Windows 3.0, or can be command-line driven for power users.

The Stag

Stag Microsystems has been making device programmers for about 20 years. Its various models provide stand-alone, as well as computer-driven capabilities for those needing universal device programmers. Stag Microsystems is introducing a new version of its top-of-the-line System 3000 programmer which includes several advanced features. One of these is the use of memory cards rather than floppy disks to provides much quicker access to device libraries and programming algorithms.

Unlike the other programmers discussed, the System 3000 has its own built-in CRT. Combined with a front-mounted keyboard, this permits the 3000 to function in both stand-alone as well as computer-hosted modes. A keyswitch mounted on the programmer can lock it into local, remote or no-edit modes. The no-edit mode is ideal for production environments where accidental changes in device programming files could ruin a production run.

Computer-hosted modes include RS-232 serial port control (via PC Stagcom 3 software provided) or access via IEEE-488 bus. The unit can function in a pass-though mode permitting device handlers to be used and controlled from the host computer through a parallel port built into the programmer.

The standard adapter provides support for DIP devices from 16 to 40 pins. An optional module adapter supports SMDs from 20 to 68 pins. Remaining compatible with older units, the new System 3000 can support on-board programming and new packages as they emerge. Pin driver circuitry provides programmable voltage, current and rise times with the ability to sense every pin and apply variable load conditions. This assures proper programming with automated parts handlers which may have nominal connections to one or more pins.

In stand-alone mode, the programmer can accept all setup and operational parameters and commands via a built-in keypad. The numeric, Hex and special function keys are used to access and control all function when stand-alone mode is used.

The remote-control mode gives complete control of the programmer to a host computer. The no-edit mode lets the programmer locally copy and burn parts, but doesn't let any fusemap edits or changes take place.

Jon Gabay is a free-lance editor with extensive design experience. He has written for all of the specialized CAE/CAD publications at one time or another, including High Performance Systems, Engineering Workstations *and, most recently,* Design Automation.

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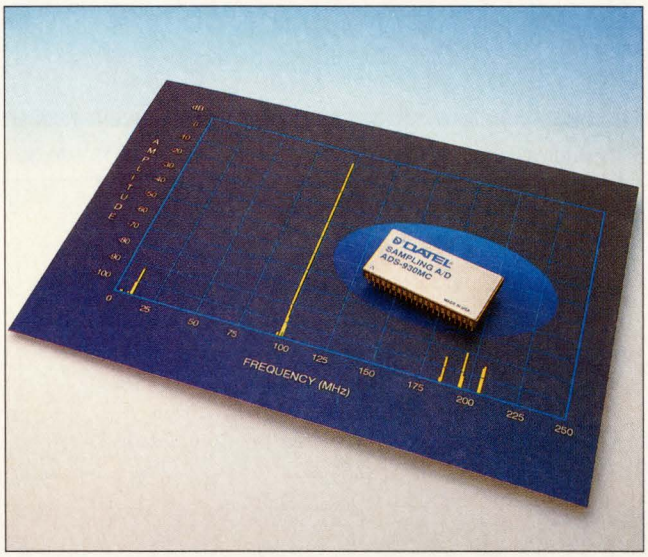
CIRCLE NO. 59

INTEGRATED CIRCUITS

High-resolution ADCs tailored to system needs

Jeffrey Child, Associate Editor



The ADS-930, a 16-bit, 500-kHz converter from Datel, offers several features geared toward signal processing applications. The device offers an SNR of 87 dB and –90 dB harmonics. An on-board FIFO provides smoother operation with DSP chips while reducing the number of DSP interrupt instruction cycles necessary.

Driven by the demands of applications such as medical imaging systems, high-resolution scanners and audio input for multimedia systems, designers continue to hunger for faster and more accurate analog-to-digital conversion. The current selection of high-resolution A-D converters ranges from very fast hybrids with multipass architectures to slower, highly integrated sigma-delta converters that digitize at audio speeds.

Raw performance is only part of today's A-D converter story. Choosing an A-D converter means considering a host of system-level factors. With this in mind, A-D converter makers are offering products that help designers stay in step with components on either side of the converter. On the analog side, there's the problem of coping with high-resolution sensors. On the digital side, there's the issue of interfacing with digital signal processors.

Focus on ac specifications

The special requirements of signal-processing applications have spawned a whole new category of A-D converter. Until recently, most high-resolution A-D converters were targeted at dc measurement applications where static accuracy is key. Today, driven by the affordability of DSPs, designers are looking for parts with good ac specifications. Providing such specifications has become much easier now that A-D converter makers can integrate a sample-hold amplifier (SHA) onto the same chip.

"In the signal-processing realm of A-D converters, one of the problems with past-generation A-D converters was that they weren't complete digitizing systems in that they didn't include the sample-hold function on-board," says Jerry Whitmore, new product marketing manager at Analog Devices (Wilmington, MA). "That presented designers with a problem. In a signal-processing application like digitizing audio, for example, the usual specifications such as gain error, offset error and linearity error are not critical. In terms of the accuracy or fidelity of the signal to be digitized, specifications like distortion or signal-to-noise ratio [SNR] are much more meaningful. It was impossible to specify those things on an A-D converter if it didn't have the S/H amplifier on-board. Without the S/H amplifier you didn't have a complete digitizing system, so you couldn't characterize the converter's performance. In fact, the distortion products and modulation products would often be affected more by the sample-holds that you put in front of the A-Ds than by the A-Ds themselves."

Although A-D converters with SHAs on them have been available for over a year at 12-bit resolutions, 16-bit parts started to come out in force this year. One such device is Analog Devices' AD1385, a 16-bit, 500-kHz A-D converter. It provides an SHA, a three-pass subranging A-D converter and linear calibration circuitry in a single hybrid package. For ac performance specifications, the AD1385 delivers a minimum SNR of 90 dB and –88 dB harmonics at 100 kHz.

An easier interface

Taking the next step in A-D conversion for signal-processing applications, Burr-Brown (Tucson, AZ) developed DSP101 and DSP102, parts specifically designed to interface with DSP chips. The single-channel DSP101 and the dual-channel DSP102 are both successive-approximation converters. Instead of using an ASIC or programmable logic to implement the interface, designers can connect the DSP101/102 directly to a DSP or other processor. According to George Hill, strategic marketing manager for Burr-Brown's data-conversion division, the devices were made for the designer who's a couple of steps removed from the analog world and would rather focus on the DSP software. "Many designer's don't want to worry about the interfacing logic to the A-D converter. They'd rather just buy a DSP and start playing with software."

Both the DSP101 and DSP102 provide sampling and conversion speeds up to 200 kHz. Internal reference, a timing/clock circuit and all the DSP interface logic are included on these devices. With 18 bits of serial data output, the DSP101 lets users drive 16-, 24- or 32-bit DSP ports. The two-channel DSP102 offers conversion with either two 18-bit ports or the ability to cascade two

Model	Resolution (bits)	Sample Rate (ksamples/s) or conversion time	Input bandwidth	Linearity error (±LSB)/MMC (no missing codes)	Power dissipation (W)	Sample & hold	Internal reference	Package type	Price	Comments
Analog Devices One Technology Way, PO Box 9106, Norwood, MA 02062-9106 (617) 329-4700										**Circle 301**
AD1378	16	16µs	—	0.003	0.8	N	Y	hybrid	$179	PIN compat. with AD1376, MIL-STD-833 qualified
AD1385	16	500	2000	1.0	2.8	Y	Y	hybrid	$895	auto-calibration, –88 dB harmonic, 91 dB S/N ratio at 200 kHz
AD1876	16	100	1	—	0.235	Y	Y	monolithic	$33	auto-calibration, –88 dB harmonic, 83dB S/N ratio
AD7710	21	—	—	NMC	0.045	N	Y	monolithic	$15	single or dual supply operation, power-down mode
AD7711	21	—	programmable	0.03	45 mW	N	Y	monolithic	$16	programmable input bandwidth
AD7712	21	—	programmable	0.03	45 mW	N	Y	monolithic	$14	sigma-delta auto-zeroed modulator w/low pass filter and serial interface
AD1879	18	—	20	—	900 mW	N	Y	monolithic	$42	stereo sigma-delta, 95 dB harmonic
Analog Solutions 85 W Tasman Dr, San Jose, CA 95134-1703 (408) 433-1900										**Circle 302**
ZAD2718	18	100	50	0.5	2.3	Y	Y	module	$250	—
ZAD2846	16	300	250	0.5	3.5	Y	Y	module	$495	—
ZAD2716	16	100	50	0.5	2.3	Y	Y	module	$198	—
Burr-Brown 6550 South Bay Colony Dr, PO Box 11400, Tucson, AZ 85734 (602) 746-1111										**Circle 303**
DSP101/102	18	200	500	6	250	Y	Y	hybrid	$29.95	direct interface to DSP chips, single or dual channel
PCM1750	18	200	500	6	210	Y	Y	mono	$38.65	two ADC's on one chip
ADC614	14	5, 120	40,000	1.0	6.1	Y	Y	hybrid	$990	88 dB spurious free dynamic range at Nyquist rates
ADC701	16	512	3.10	1.0	2.8	N	Y	hybrid	$589	107 dB spurious free dynamic range at 20 kHz
ADC700	16	67	—	0.008	0.645	N	Y	hybrid	$49.60	microprocessor interface
Crystal Semiconductor 4210 S Industrial Dr, PO Box 17847, Austin, TX 78760 (800) 888-5016										**Circle 304**
CS5014	14	56	—	1.0	0.12	Y	N	monolithic	$45	self-calibrated
CS5016	16	50	—	1.0	0.12	Y	N	monolithic	$76	self-calibrated
CS5101A	16	100	—	1.0	0.28	Y	N	monolithic	$42.20	self-calibrated
CS5102A	16	20	—	1.0	0.044	Y	N	monolithic	$37.70	self-calibrated
CS5336	16	50	20	NMC	0.45	Y	Y	monolithic	$56.40	sigma-delta
CS5328	18	50	20	NMC	0.45	Y	Y	monolithic	$84.70	sigma-delta

Model	Resolution (bits)	Sample Rate (ksamples/s) or conversion time	Input bandwidth	Linearity error (±LSB)/MMC (no missing codes)	Power dissipation (W)	Sample & hold	Internal reference	Package type	Price	Comments
Crystal Semiconductor 4210 S Industrial Dr, PO Box 17847, Austin, TX 78760 (800) 888-5016										**Circle 304**
CS5501	16	—	0.01	0.25	0.025	Y	N	monolithic	$18.20	on-chip filter rejects to 460 Hz self- calibration
CS5503	20	—	0.01	4	0.025	Y	N	monolithic	$27.70	same as above
C5505/7	16	—	0.01	±1	0.0015	Y	Y	monolithic	$15.70 - $16.20	1 or 4 input channels
CS5506/8	20	—	dc-10 Hz	±8	0.0015	Y	Y	monolithic	$13.50 - $18.00	same as above
CS5516	16	—	dc-12 Hz	±1	0.035	Y	Y	monolithic	$17.40	on-chip circuitry for off-set removal
CS5520	20	—	dc-12 Hz	±8	0.035	Y	Y	monolithic	$20.50	same as above
Datel 11 Cabot Blvd, Mansfield, MA 02048 (508) 339-3000										**Circle 305**
ADS-930	16	500	2,000	1.0	3.4	Y	Y	hybrid	$337	on-board FIFO, overflow pin, 3-state outputs
ADS-942	14	2,000	6,000	0.5	2.8	Y	Y	hybrid	$374	-85 dB, harmonics, over-flow pin, 3-state outputs
ADS-941	14	1,000	6,000	0.5	2.9	Y	Y	hybrid	$337	same as above
ADS-928	14	500	6,000	0.5	3.1	Y	Y	hybrid	$299	overflow pin, 3-state out-puts
ADS-924	14	300	4,500	0.5	1.4	Y	Y	hybrid	$199	24-pin DIP
ADS-926	14	500	1,500	0.25	1.4	Y	Y	hybrid	$207	28-pin DIP
ADS-927	14	1,000	2,000	0.25	1.5	Y	Y	hybrid	$224	28-pin DIP
ADC-908	14	1.0µs	—	0.5	2.7	N	Y	hybrid	$243	standalone ADC
ADC-914	14	2.4µs	—	0.5	0.925	N	Y	hybrid	$175	standalone ADC
Harris Semiconductor PO Box 883, Melbourne, FL 32902 (407) 724-3704										**Circle 306**
ICL7115	14	25	—	1.5	0.040	N	N	monolithic	$39	—
ILC Data Device 105 Wilbur Place, Bohemia, NY 11716 (516) 567-5600										**Circle 307**
ADC00145	14	5,000	20,000	1.0	4.0	Y	Y	hybrid	$785	-55°C to +125°C temp range, unipolar, bipolar; 5V, 10V and 20V input ranges
Micro Networks 34 Clark St, Worcester, MA 01606 (508) 852-5400										**Circle 308**
MN6405	16	50	25	0.25	0.75	Y	Y	hybrid	$200	FFT tested, (8-bit words)
MN6450	16	50	25	0.25	0.75	Y	Y	hybrid	$210	FFT tested, (16-bit word)
MN6500	16	100	50	0.25	0.73	Y	Y	hybrid	$225	FFT tested, serial output, sleep mode
MN5280	16	100 µs	—	0.5	1.8	N	Y	hybrid	$169	—
MN5282	16	50µs	—	0.5	1.8	N	Y	hybrid	$187	—
MN5284	16	50µs	—	0.5	0.3	N	Y	hybrid	$249	—

PRODUCT FOCUS/High-Resolution ADCs

Model	Resolution (bits)	Sample Rate (ksamples/s) or conversion time	Input bandwidth	Linearity error (±LSB)/MMC (no missing codes)	Power dissipation (W)	Sample & hold	Internal reference	Package type	Price	Comments
Micro Networks 34 Clark St, Worcester, MA 01606 (508) 852-5400										**Circle 308**
MN5290/ MN5291	16	40µs	—	0.5	1.08	N	Y	hybrid	$150 - $175	full military temp. range
MN5295/ MN5296	16	17µs	—	0.5	1.2	N	Y	hybrid	$162 - $194	same as above
MN6290/91	16	20	10	0.5	1.5	Y	Y	hybrid	$180	FFT-tested
MN6295/96	16	50	25	0.25	1.7	Y	Y	hybrid	$187	FFT-tested
MN6400	16	50	25	0.25	0.75	Y	Y	hybrid	$210	FFT-tested, 8-bit bus drivers
Maxim Integrated Products 120 San Gabriel, Sunnyvale, CA 94121 (408) 737-7600										**Circle 309**
MAX135	18	0.016	—	0.005	1.25 1.69 mW	N	N	monolithic	$8	integrating ADC ±5V supply, 8-bit µP data interface
MAX132	18	0.016	—	0.005	same as above	N	N	monolithic	$8	same as above
Motorola 6501 William Cannon Dr W, Austin, TX 78735 (512) 891-2020										**Circle 310**
56ADC16	16	6,400	100	0.5	0.4	Y	Y	monolithic	$16.68	sigma-delta, single 5V supply, zero glue interface to DSP
PREMA Precision Electronics 4650 Arrow Highway, Bldg E-5, Montclair, CA 91763 (714) 621-7292										**Circle 311**
5601	25	20s	—	0.0001	0.45	N	N	module	$360	unipolar/bipolar
Sipex 22 Linnell Cir, Billerica, MA 01821 (508) 667-8700										**Circle 312**
SP9490	16	1,000	250	2	3.2	Y	Y	hybrid	$735	—
SP9478	14	500	100	1	2.75	Y	Y	hybrid	$320	—
SP1676	16	8	20	2	0.350	Y	Y	monolithic	$45	—
Texas Instruments PO Box 809066, Dallas, TX 75380 (800) 232-3200										**Circle 313**
TLC7135	14	0.03	—	0.5	0.03	N	N	monolithic	$3.47	dual slope integrating ADC with 4.5 digit drive outputs

16-bit converters into a 32-bit word.

Engineers in the DSP Applications Group at Texas Instruments (Dallas, TX) are naturally pleased with the DSP101/102. Besides making TI's customers more comfortable about designing with DSP chips, the DSP101/102 eased their task of making demo boards for their own DSP chips. "It lets you build a real low-cost system with just a DSP, an A-D converter and some memory", says Leor Brenman, TI's floating point applications engineer. "Normally, if you were using a parallel A-D, you'd need some decode logic so that you wouldn't be reading your memory while you're sampling."

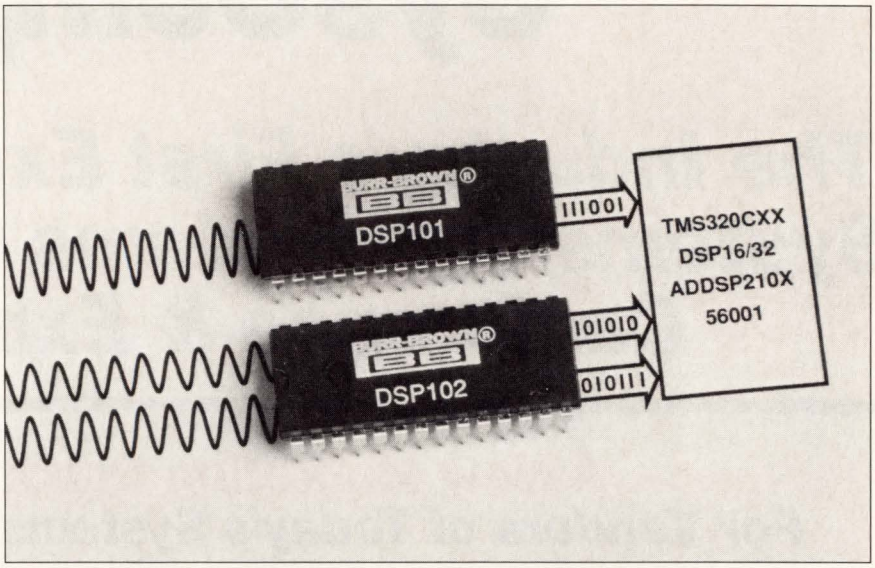
Brenman also likes the DSP102's ability to take two sets of 16-bit samples in parallel because it lets the TMS320C31, TI's lower-cost floating-point DSP, do 32-bit processing of A-D samples. Although the TMS320C31 has only one 16-bit serial port, the DSP102 can take in two 16-bit samples and send them both to the TMS320C31. In software, the DSP can then separate the samples into a right and a left side, making a 32-bit sample, Brenman explains.

The ADS-930, a 16-bit, 500-kHz converter from Datel (Mansfield, MA) also offers features to make smooth operations with DSPs. It offers an on-board FIFO memory—a unique feature among high-resolution converters. The 16-bit wide, 16-word deep FIFO can be simultaneously filled and emptied. This reduces some of the interrupt instruction cycles that must be sent to the DSP. Two control pins on the ADS-930 let the user access the FIFO when it's half full or on command.

Based on a two-pass, subranging architecture, the ADS-930 is packaged in a single 40-pin hybrid. The part requires ±15-V and +5-V power supplies. Also featured is a differential input that can reject common mode noise from sensitive ground layouts.

Limiting factors

While the requirements of interfacing with DSPs are affecting A-D converter designs from the digital side, components on the analog side are also a factor. Advances in sensor technology have driven up their accuracy to the point where they are no longer the limiting factor. Used in everything from camcorders to pre-



Burr-Brown's DSP101 and DSP102 are both 200-kHz, 18-bit A-D converters specifically designed to interface with DSP chips. Instead of using an ASIC or programmable logic to implement the interface, designers can connect the DSP101/102 directly to a DSP. The parts interface with the serial ports on DSP chips from Analog Devices, AT&T, Motorola, and Texas Instruments.

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CIRCLE NO. 61

press imaging applications, charge-coupled device (CCD) sensors exemplify this trend. Dynamic ranges over 90 dB are quite common in CDD sensors today. To keep pace, designers need to upgrade to a higher-resolution A-D converter to keep the converter from becoming the weak link in the system performance.

"If your sensors have a dynamic range that's pushing past 90 dB, you really want a 15-bit or 16-bit converter," says Bob Leonard, product marketing manager at Datel. "If your sensor is that accurate, you need to choose an A-D converter that can take advantage of the sensor's accuracy."

Upgrading to a higher-resolution A-D converter is especially attractive when the alternative is adding memory or processors to the design. "When sensor arrays were only 256 × 256 pixels, the microprocessor could easily keep up in real-time," says Leonard. "Now there are sensor arrays as large as 4k × 4k pixels. These require an incredible amount of processing to digitize the output. In the past, the processor could take some extra time and do some signal averaging. But now, you can easily consume the power of a 50-MHz processor. Then it's all you can do to read a pixel and get the accuracy right from that one pixel. There isn't time to go back and do any averaging." Instead of getting more memory and putting several processors in parallel, designers can opt to use just one processor and a higher-resolution A-D converter, says Leonard.

A-D converters for multimedia

Long before the term "multimedia" became a buzzword, A-D converters were key components in the architecture of systems designed to convert video and audio signals into digital data. High-resolution A-D converters for multimedia today means audio bandwidth up to 20 kHz. In that range, the most interesting development is the emergence of sigma-delta technology. While Analog Devices and Crystal Semiconductor (Austin, TX) offer various sigma-delta parts today, Burr-Brown will introduce its own line of sigma-delta converters next year, says Burr-Brown's Hill.

In a sigma-delta architecture, a fast 1-bit converter oversamples the input signal. The sigma-delta converter then does some processing of the signal, producing a parallel output representation of the input. The signal is then sampled at a high data rate and yields a low-frequency output.

Unlike other A-D converter architectures, sigma-delta is about 90 percent digital and only 10 percent (the modulator) analog. Because of this, A-D converter vendors have found it relatively simple to integrate one or more sigma-delta converters onto one chip, as well as other support circuitry. This trend should fit nicely with the needs of multimedia systems designers as they strive to pack a lot of audio circuitry into as small a space as they can.

Ron Malcolm, senior design engineer at New Media Graphics (Billerica, MA), is looking at providing advanced digitized audio capability on PCs. "As far as we're concerned, it's what's integrated along with the rest of the chip that matters in multimedia. To get into a computer you need to integrate peripheral functions along with that function." With this in mind, Malcolm wouldn't choose a simple A-D-only part, but rather one of the more integrated audio codecs (coders/decoders) such as those recently announced by Analog Devices and Crystal Semiconductor. These new devices will combine A-D/D-A converters and have built-in compression.

In general, Malcolm doesn't expect data converter technology to be the limiting factor as multimedia designers strive for CD-quality sound. "Once you put the converter on a board with a lot of digital stuff, it gets very difficult to keep the noise down to get that level of performance. It's going to be very difficult for the multimedia designers to get high SNRs on a multimedia card. So I don't think it's going to be converter limited, its going to be limited to the board layout." ■

COMPUTERS & SUBSYSTEMS

Turning a corner on graphics processing

The latest addition to the growing family of high-performance VME graphics solutions is a two-board set from Array Microsystems providing high-resolution, real-time 2-D imaging. The board set includes an image processing board (a66545) and a frequency domain array processor (FDAP) board (a66540) which, when combined, can process an entire 256 × 256 pixel frame of image data in 15.2 ms, translating to a real-time rate of 65 frames/s. At 512 × 512 pixels, the board set transforms images in 71 ms, a rate of 14 frames/s.

Designed for applications in medical imaging, radar, sonar, machine vision, and other real-time 2-D image-processing applications, Array Microsystem's board set is compatible with standard 6U VMEbus systems. To achieve the real-time processing rates, the board set operates on entire arrays of pixels, using frequency domain processing. The board set operates with a clock rate of 40 MHz and is capable of performing at 400 Mops.

Dubbed Cornerturn, the pair of boards perform all the necessary functions for full-frequency domain processing at real-time frame rates. The a66545 performs all the complex addressing, normalization and scaling required in 2-D frequency domain processing such as finite impulse response (FIR) filters, correlations and convolutions. Two-dimensional processing consists of performing 1-D fast Fourier transforms on each individual row of data followed by 1-D FFTs on each individual column of data in a frame.

The Cornerturn board accepts complex I/O data through 10-MHz, double-buffered external I/O connectors or through the VMEbus and stores it in one of four, on-board frame store buffers. The frame store memory, configured as either 1 or 4 Mbytes (32-bit words) of SRAM, supports image matrices of up to 256 × 256 or 512 × 512 pixels, respectively. Row and column size is user programmable up to 16 points. The a66545 also provides simultaneous in-phase/quadrature (I/Q) and polar magnitude and phase outputs.

Array Microsystems' board set is supported by the company's image-processing application-development package, Arraysoft, written for the OS/9 operating system. It features high-level routines for all register-level control and frame-level frequency domain processing functions. The board set and development package is priced at $25,800 in single units. A 25-MHz version is priced at $18,800. The boards are also available separately.

— Warren Andrews

Cornerturn at a glance

- Real-time 2-D processing
- High-resolution 256 × 256 or 512 × 512 pixels
- Real-time performance at 70+ frames/s
- 10-MHz double-buffered I/O channel
- Provides I/Q and polar magnitude and phase outputs

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CIRCLE NO. 63

CAE/CAD TOOLS

Behavioral model allows simulation of VMEbus interactions

While the increasing number of device models has bolstered support for simulation as a design tool, there are limitations if an engineer wants to move beyond ASIC or circuit board simulation into the realm of total system simulation. One of these stumbling blocks is the availability of adequate models for the system bus. Logic Automation hopes to fill this gap with SimuBus, a behavioral model for the VMEbus standard.

According to Logic Automation, a designer using SimuBus can see a broad range of interactions between a board under development and the rest of the system. The SimuBus model contains extensive error checks on the simulation in progress, including set-up, hold and pulse widths on all bus transactions.

Logic Automation decided to adopt a behavioral model approach after examining the alternatives available, such as macro and algorithmic methods. "With these other approaches, the action and interaction of the test vector and the test board are predetermined," says Rick Denker, product marketing manager for SimuBus. "This means that the test stimulus is built matching only one static view of a set of bus transactions. If the design is altered, causing a delay when a data acknowledge is returned, or if an interrupt occurs at a different time, then the previously created test stimulus must be painstakingly modified."

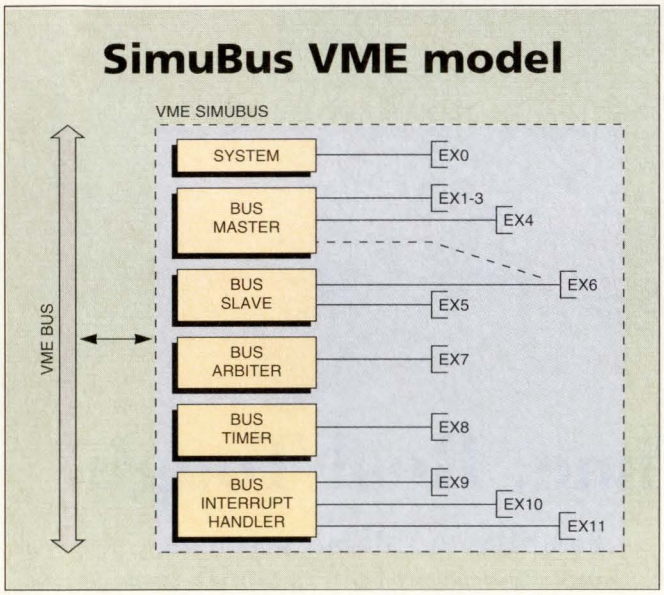
Logic Automation's SimuBus model waits when a data acknowledge is delayed. "This ensures that the acknowledge still falls within the timing specification," Denker explains. "After a successful acknowledge, the SimuBus model continues with the simulation stimulus. Because the SimuBus is event driven, masters, slaves and interrupts don't have to happen in a predefined order for the simulation to work."

The SimuBus model lets a designer set up a system environment without having to write complex models of all the other boards in the system. By developing top-level models of how different boards in the system act on the bus, a designer can see how the system will interact with the circuit board under development.

The SimuBus model implements the requirements of IEEE 1014-1987, supporting system, master and slave segments, as well as all critical VMEbus operations including read, write, read-modify-write, interrupts, block reads, block writes, and arbitration. The model also provides programmable timing delays to catch complex multiple-board interaction problems. In addition, the SimuBus model lets designers increase design complexity as a system design unfolds. For example, the designer can start with arbitration and simple reads and writes. Then, as the design progresses, block reads/writes, interrupts and additional masters and slaves for testing complex system-level interactions can be added.

The SimuBus model is controlled using Logic Automation's Processor Control Language (PCL). Through PCL files, the user can algorithmically configure the bus operations for the system. This source file input method lets users save input files for use in the next project.

The SimuBus VME model is available immediately for a single license price of $10,000. Site licenses are $25,000. — *Mike Donlin*



The SimuBus VME model consists of six exception-driven modules. Designers direct the actions of these independent modules by writing Processor Control Language exception routines.

SimuBus at a glance

- Behavioral model for the IEEE 1014-1987 VMEbus standard
- Supports system, master and slave segments, as well as all critical VMEbus operations
- Provides programmable timing delays
- Lets designers develop models of board behavior on the bus without developing complex models of other boards in the system
- Available now for single license price of $10,000

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Beaverton, OR 97075
(503) 690-6900
Circle 355

ASICs & ASIC DESIGN TOOLS

Device-independent layout toolset for FPGAs

The FPGA Foundry toolset of design and layout tools from NeoCAD initially supports Xilinx and Actel architectures and claims to achieve higher clock speeds and greater gate utilization than tools from the FPGA vendors themselves. "With FPGA Foundry, a designer has a single set of tools which can be used in the design of devices as different as the Xilinx 3000 series and Actel's Act 1 family," says Bob Anastasi, NeoCAD's president. The FPGA Foundry toolset includes a timing analyzer and circuit optimizer/mapper, timing-driven automatic place-and-route, graphical editor, back annotation, and report file generation.

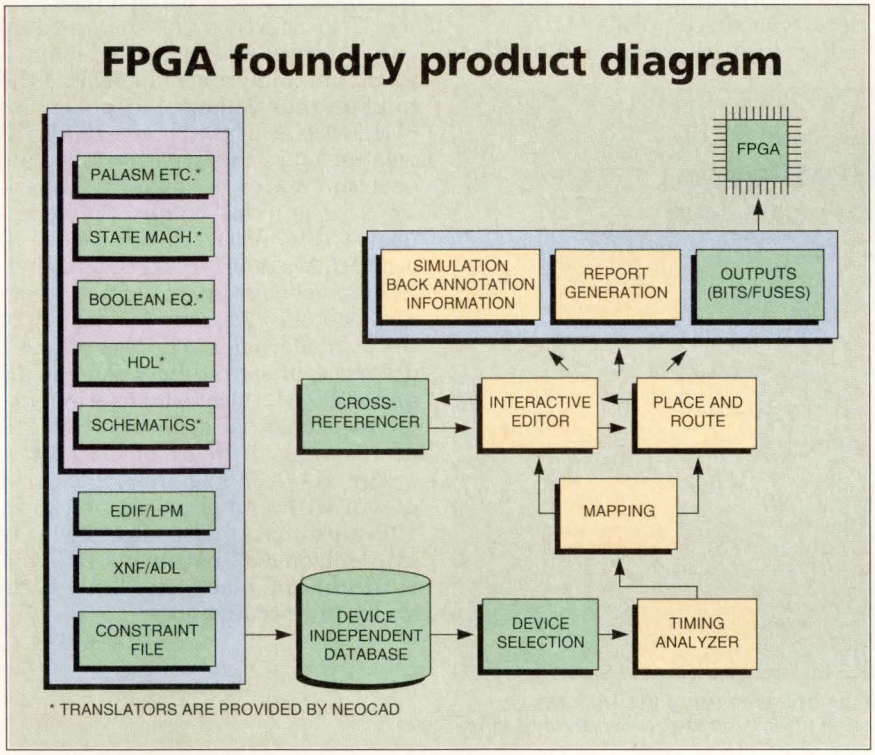
After an FPGA Foundry user identifies nets requiring critical path delays, minimum clock speeds and any other desired constraints, the toolset's Timing Analyzer examines the design and automatically generates additional path-delay information required by the Mapper and the Automatic Place and Route (APR) tool. The Mapper then combines FPGA Foundry's device-independent database with device-specific data files to determine how the logical design description would best fit into the physical device. The Mapper then assigns the logical description to elements within the device's physical blocks.

The APR tool, driven by the same timing and constraint information as the Mapper, executes algorithms to converge toward an optimal set of interconnections. Both the Mapper and the APR use tightly coupled automatic-feedback mechanisms. The place-and-route functions are integrated into a single tool, says NeoCAD, to guarantee they will satisfy the design requirements while maximizing efficient gate utilization. NeoCAD claims its automated process reduces the need for many attempts to achieve completion and the required timing results.

The toolset's graphical editor, Epic (Editor for Programmable ICs), lets designers route critical nets interactively. Response time is virtually instantaneous, claims NeoCAD, regardless of the operation. Epic supports push-button, menu-driven and command line-editing capabilities and lets place-and-route tools run on individual signals, logic blocks and groups of signals within the editor. Epic can also highlight signals by delay characteristics.

A delay report generated by FPGA Foundry lists path and net delays within the design, logic block and I/O utilization, and available resources. Back annotation tools provide timing data to simulators and output netlists in various formats.

Since FPGA Foundry is a device-independent toolset, it has been designed to be fully compatible with major CAE vendors' design-entry and simulation tools. It accepts designs in standard descriptions including EDIF (Electronic Data Interchange Format) 2.00 and LPM (Library of Parameterized Modules), as well as vendor-specific netlist formats such as the Xilinx XNF and the Actel ADF. The toolset runs on 386/486 PCs operating under Microsoft Windows and on Unix-based workstations running X Windows and Motif. FPGA Foundry is available now with prices starting at $18,000. — *Barbara Tuck Egan*



The device-independent FPGA Foundry design and layout toolset accepts designs in standard descriptions as well as vendor-specific netlist formats.

FPGA Foundry toolset at a glance

- Handles multiple FPGA architectures
- Support of device-specific macros/attributes
- Timing/constraint-driven implementation
- Industry-known algorithms with proprietary scoring and costing
- Incremental place and route
- Standards-based environment
- Runs on PCs and workstations

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Circle 354

INTEGRATED CIRCUITS

20-bit DAC boasts signal-to-noise ratio of 118 dB

Claiming to be the highest resolution D-A converter to use the company's "bitstream" or delta-sigma technology, the Philips/Signetics SAA7350 is a 20-bit D-A converter designed for decoding digital audio signals. It provides a choice of two system clock frequencies synchronized to the audio sampling frequency (f_s). The D-A converter itself will accept all digital data input formats of 16 to 20 bits at audio sampling frequencies varying from 16 to 53 kHz. The clock frequency can be either 256× or 384× f_s with internal oversampling factors of 128× or 192× f_s. Integrated third-order noise shapers are designed to improve the signal-to-noise ratio (SNR) to 118 dB. To reduce common mode crosstalk, the SAA7350 features 1-bit differential-mode switched-capacitor D-A converters, as well as differential-mode post-filtering op amps.

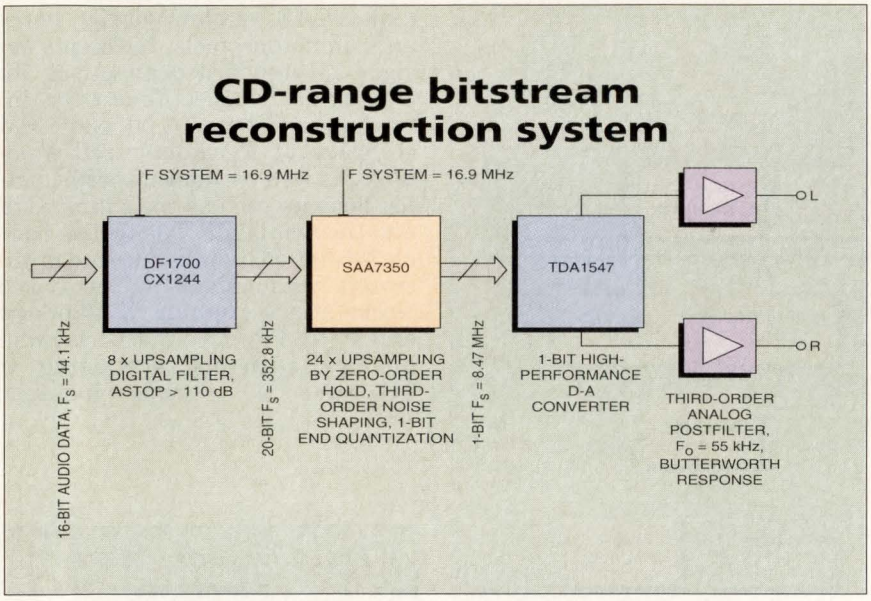
In the SAA7350's bitstream conversion process, the high-speed switched-capacitor network is used to convert a serial bitstream into a continuous analog signal. An analog waveform is reconstructed from the pulse density of the bitstream by transferring a fixed amount of charge on a capacitor to a summing node of a first-order integrator. (A data "1" in the bitstream, for example, will transfer a positive amount of fixed charge to the summing node, while a data "0" will extract the same amount of charge.) The rate of charging and discharging will vary with the pulse density of the bitstream. The analog signal is reconstructed from the rate and density of these pulses.

For high-performance applications, Signetics recommends that the output of the 7350's third-order noise shapers be routed to a separate 1-bit converter, the TDA1547. The TDA1547, manufactured in BiCMOS technology, contains an improved and optimized switched-capacitor, 1-bit D-A converters and post-filtering Class A op amps. In the digital logic and drivers, bipolar transistors are used to optimize speed and reduce digital noise generation. In the analog section of the chip, bipolar transistors are used to achieve the high performance of the Class A op amps. Signetics researchers decided to implement the analog processing function in a separate device when it was discovered that crosstalk between the noise shapers and switched-capacitor networks in the 7350 reduced performance in high-performance applications. When used in conjunction with a Burr-Brown (Tucson, AZ) 8-f_s digital filter as a front-end and Signetics' own TDA1547 1-bit D-A converter, a complete 192× oversampled digital audio system can be built.

To measure the performance of the device, a 1-kHz, 20-bit, –60-dB sine wave was fed into the system shown. The fundamental frequency was then removed using a notch filter. The spectrum of the residual output signal was measured using a spectrum analyzer to determine the total harmonic distortion, plus noise (THD+N). A THD+N of –108.5 dB was measured relative to full scale over the entire bandwidth. According to Signetics' application engineer Craig Aine, this exceeds all other D-A converters on the market. Similar measurements aimed to determine the linearity deviation of the part showed it to be less than 0.2 dB for input signals between –60 dB and –120 dB. Other measurements found a channel separation of 115 dB and digital silence of –110 dB.

The SAA7350 is available in a 44-pin QFP and is priced at $23 in 100-piece lots. The TDA1547 is available in a 32-pin shrink DIP and is $18 in 100-piece lots. Both parts are in full production.

— Dave Wilson



A 192× oversampled bitstream CD system can be designed using the Signetics SAA7350 in conjunction with an 8× oversampling filter, 1-bit D-A converter and third-order Butterworth filters.

SAA7350/TDA1547 combo at a glance

- Highest resolution stand-alone 20-bit DAC
- Signal-to-noise ratio of 118 dB
- Linear deviation less than 0.2 dB

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INTEGRATED CIRCUITS

Audio codecs play to a multimedia tune

As multimedia moves into the forefront of workstation and PC development, system designers are seeking high-performance, low-cost audio converters for interfacing to compact disk, digital audio tape, system memory, and user input/output devices such as microphone, speaker, headphones and telephones. And to make room for the video and graphics circuitry on their boards, designers would prefer to keep the audio section as small as possible.

With this in mind, Crystal Semiconductor developed the CS4215 and CS4216, a pair of stereo audio coder/decoders (codecs). Announced at October's Analog & Mixed Signal Design Conference (Santa Clara, CA), the CS4215 and CS4216 are designed to provide integrated solutions for designers involved in implementing CD quality audio in a computer environment. The devices are capable of operating at various sample rates (programmable from 8 to 48 kHz), making them suitable for processing signals ranging from voice to full digital audio rates.

According to Craig Ensley, vice-president of marketing at Crystal, these parts also break some critical cost barriers for the sound card designs. The cost of data converters taken in aggregate with the cost of digital signal processors has limited many sound card designs to playback only, he says. Many would use a high-performance D-A converter, but would forego the A-D conversion circuitry needed for audio authoring. They could take existing software libraries, and generate sound from those software libraries, but they couldn't record and create new libraries. Because of cost, only the most expensive sound cards had both A-D and D-A converters, enabling them to perform both authoring and playback.

Taking the next major leap of faith, the CS4215/16 integrates both A-D and D-A for the audio functions onto a single chip and adds a number of other capabilities to form a complete audio analog interface. According to Crystal, the parts replace up to 20 $in.^2$ of circuitry with one chip. Besides large A-D and D/A converter chips, the CS4215/16 replaces six or seven high performance op amps, and around 50 analog discrete components.

Both the CS4215 and CS4216 are based on sigma-delta data conversion techniques and include interpolation, anti-aliasing and output-smoothing filters on-chip. The chips also offer programmable input gain and output attenuation. Both devices support a signal-to-noise ratio of 85 dB while operating at the maximum sample rate. The CS4215 accepts either line level or microphone inputs and has a headphone driver stage on-chip. It also features data-compression/decompression circuitry consistent with telephony A-law and μ–law standards. The CS4216 has fewer value-added features, making it a lower-cost alternative to the CS4215. As such, the CS4216 is targeted for systems that simply require basic conversion functions, such as computers that support the Microsoft Multimedia Windows 3.0 standard.

Available this month, pricing for the CS4215 begins at $30 in 1,000 piece quantities, while the CS4216 is priced at $23 in 1,000 piece quantities. Both are offered in 44-pin PLCC packages. *—Jeff Child*

CS4215/CS4216 audio codec at a glance

- Programmable sample rates from 8 to 48 kHz
- Contains sigma-delta A-D and D-A converters on-chip
- Provides interpolation, anti-aliasing and output smoothing filters
- 85 dB SNR at maximum sample rate
- Accepts line level or microphone inputs
- Compression/decompression per A-law and μ-law telephony standards

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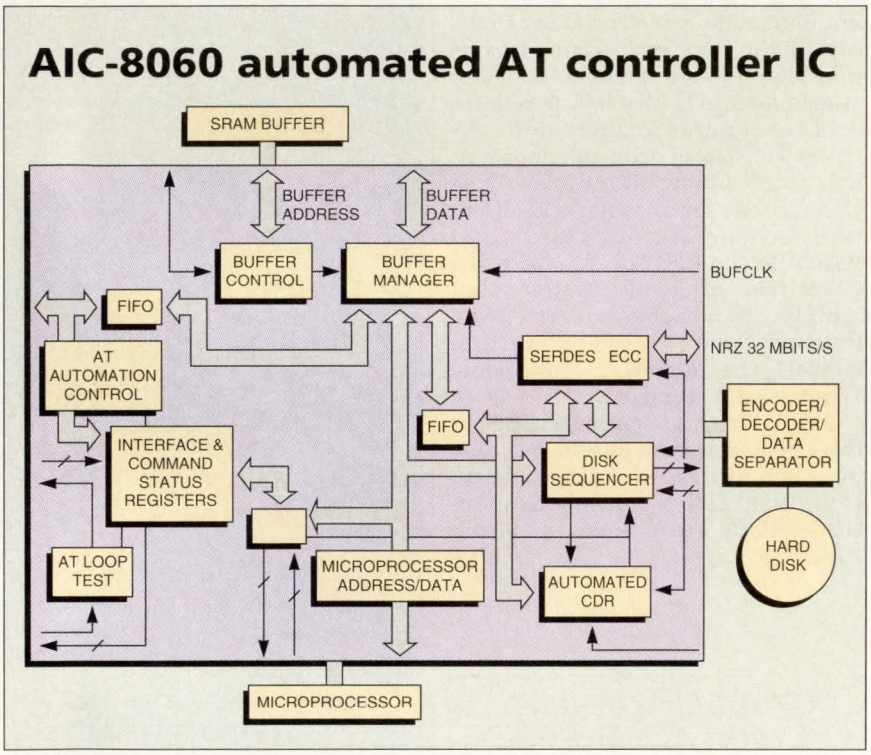
Circle 358

INTEGRATED CIRCUITS

ICs put the brains back into disk drives

It's hard not to be impressed by the colossal amounts of memory capacity disk drive vendors are offering in their latest small form factor drives. To get a smaller form factor drive requires giving up some features that users expect. As the smaller form factor drives hit the streets, consequently there are few features.

But if a servo takes up 60 percent of the processor's time, there's very little bandwidth for the processor to take care of requests from the host system. The 8060 handles these transfers, automatically transferring multiple sectors, updating the task file register, keeping track of the sector addresses, and performing handshakes with the AT bus.



Offering several automation features, the AIC-8060 handles routine tasks across the AT bus. This frees the drive's microcontroller to concentrate more time on functions that are local to the disk drive, such as embedded servo control.

That was the case with 3.5- and 2.5-in. drives, and as 1.8-in. drives emerge, designers will want to offer features that distinguish their drives from the competition. The AIC-8060, Adaptec's newest embedded disk controller chip, may help drive designers do just that. With its array of features, the AIC-8060 frees up other electronics on the disk drive for local duties.

To get higher densities into a smaller area, today's drive manufacturers are increasing bit density by embedding servos directly on the media. A microcontroller embedded on the drive manipulates the servo for higher densities without losing any performance on the host bus.

Based on the architecture of the AIC-7000, Adaptec's earlier family design, the AIC-8060 shares many of the same features. While the 7000 introduced the concept of disk automation from the disk side, the 8060 takes automation a step further by automating functions on the AT-bus side.

The 8060 also features the ability to test the drive without connecting it to an AT bus. The drive can output data, as if it were being sent to the AT bus, and then read data back to the drive. In this way, drives can be tested using only a simple test fixture rather than an entire AT host computer.

Providing a further boost to drive performance, the 8060 has an automated caching scheme that lets the drive respond more quickly to commands. For single sector transfers on the AT bus, the next command is known ahead of time. Before the read comes in, all the necessary pointers may be set up. And as soon as the command comes in, the chip will automatically start the AT read operation upon receiving the read command.

For drive designs with large buffers, designers may want to set up certain tracks as read-ahead tracks that are accessed quite often. To achieve this, the 8060 offers programmable buffer-size segmentation. A drive designer may, for example, set off a 32-kbit area of the look-ahead area for caching, and use the remaining area for other functions. The chip also supports features that go hand-in-hand with high-density media such as constant density recording and 88-bit Reed-Solomon error-correction code. And because compatibility is all important for the AT, Adaptec assures that the chip works with several vendor's BIOSs. These include BIOS from AMI, Award, IBM, and Phoenix.

To meet the space requirements of 1.8-in. drives, the device is offered in a small, 128-pin, fine-pitch QFP. Available this month in production quantities, the AIC-8060 is priced at $17.50 —*Jeff Child*

AIC-8060 disk controller at a glance

- Automates AT task file updates
- Automated caching scheme boosts response time
- Loop-back capability permits testing without a complete AT system
- Programmable disk-buffer size
- Supports 88-bit Reed-Solomon error correction code
- Compatible with BIOS from AMI, Award, IBM, and Phoenix

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Circle 357

SOFTWARE & DEVELOPMENT TOOLS

Gello molds object-oriented control software

Gello, an object-oriented, real-time programming environment for the control and monitoring of process and manufacturing operations, lets control engineers graphically connect functional elements together and simulate their behavior. Developed by Event Technologies (Indianapolis, IN), Gello (Graphically Enhanced Ladder LOgic) consists of a target-resident Gello engine and a graphical CASE tool called Gellix.

The user creates a control program with Gello by using a mouse to select familiar control objects and hook them together to define control relationships. Objects are precompiled functions, 16 bytes in length, having up to three inputs, one output and three static variables. Objects can be linked together to form new objects in two ways. First, for vertical functions, several objects can be connected to form a larger object with more inputs and variables. Second, a group of objects specifying some discreet subset of a control program can be defined as a "page," which is itself an object with distinct inputs and outputs and rigorously defined internal behavior. Objects and pages created under Gellix can be saved in the user's library and reused for other applications.

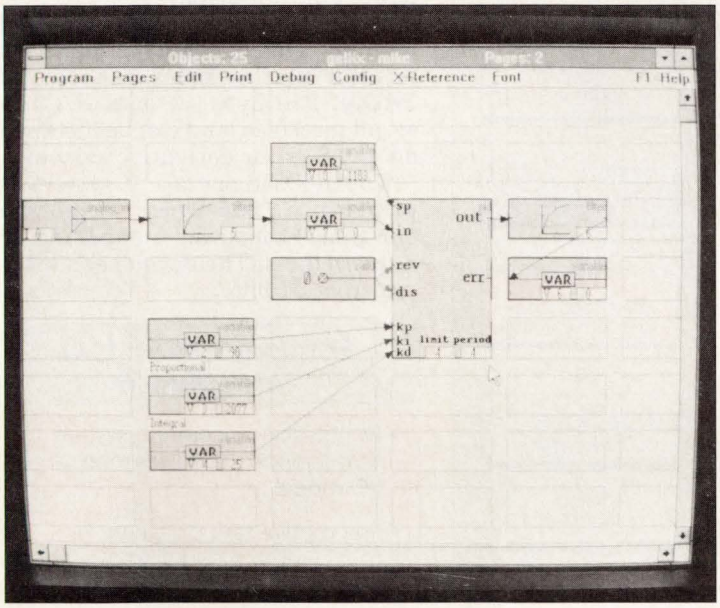
The graphical representation of a control program is hierarchical. Pages can be represented as icons which, when clicked on, reveal the next lower level of program structure down to the level of the rectangular icons supplied in the basic object library. Using ETI's development kit, users can create their own objects by following the three-input, three-variable rule. The result is a default graphical icon represented as a rectangle with "Name" in the upper right corner. Custom icons can be created using the Microsoft Paintbrush program. To incorporate an icon into Gellix, it must be submitted to ETI for recompilation, but ETI will soon offer complete icon capability in Gellix.

The Gello engine runs under the target system's operating system. ETI currently supports MS-DOS for 80X86 CPUs and OS/9 running on Motorola 680X0 processors. The engine is ported to the operating system, not the CPU, so a wide variety of board support will be available. ETI has also announced plans to port to Lynx/OS from Lynx Real-Time Systems (Los Gatos, CA) and VxWorks by Wind River Systems (Alameda, CA). ETI also currently supports Hewlett Packard's Bitbus (RS485) and Ethernet via TCP/IP.

While Gello will run with a multitasking operating system, allowances must be made for real-time performance penalties because the task scheduler steals cycles from Gello, reducing its deterministic real-time response. For process control applications normally requiring response times in the 10- to 100-ms range, this is seldom a problem. In real-time, event-driven systems, however, the company points out that attention must be paid to CPU and I/O speeds.

ETI supplies a number of "define" files with the product so a user can set up to run on a specific system. Normally, the user selects the target processor when running Gello. The Gello engine can run out of PROM or RAM, while instructions (the code defined by the objects) download RAM. In an embedded system, instructions can be stored in battery-backed RAM or EEPROM because Gello is designed to boot and run on power-up. Gellix currently runs on DOS platforms under Microsoft Windows 3.0 and will soon be available for Unix platforms under X Windows.

ETI has licensing arrangements for the Gello engine under which OEMs may license the source code for inclusion in custom designs. The binary engine product itself sells for $900 and the Gellix CASE environment sells for $6500. — *Tom Williams*



The Gellix CASE tool lets users put control programs together by graphically linking precompiled routines in a hierarchical structure.

Gello at a glance

- Gello engine size ranges from 4 to 12 kbytes on 8-bit processors, about twice that size on 16- and 32-bit CPUs
- Gellix CASE tool runs under MS-Windows and soon under X Windows
- Object-oriented control programs use precompiled objects
- Objects have up to three inputs and three static variables
- Complex object hierarchies can be built
- User-defined objects are reusable
- Engine ported to DOS, OS/9, Bitbus and soon to Lynx/OS and VxWorks

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Circle 351

SOFTWARE & DEVELOPMENT TOOLS

Real-time OS teams with development tools to tackle 8051 applications

A real-time operating system designed specifically for the 8-bit control world workhorse, the 8051 and its derivatives, has been introduced by Franklin Software (San Jose, CA). RTX51 can be teamed with a set of compatible tools which include an assembler, linker and a debugger/simulator. The operating system is available in two versions, one for full multitasking with a choice of scheduling paradigms, and an abbreviated version with round-robin scheduling.

RTX51 has been adapted to the memory and I/O characteristics of the 8051 family. Along with preemptive and nonpreemptive task scheduling, it provides intertask communication, management of both internal and external ROM and RAM, and multiple event management. Communications include an operating system task supporting the Hewlett Packard Bitbus interface for setting up microcontrollers on a simple serial network.

Designers can select either round-robin or preemptive task switching and define up to 256 tasks with 19 open at any given time. Task processing can be suspended by an operating system wait function which reactivates processing on receipt of an interrupt, a time-out or a message from some task or interrupt.

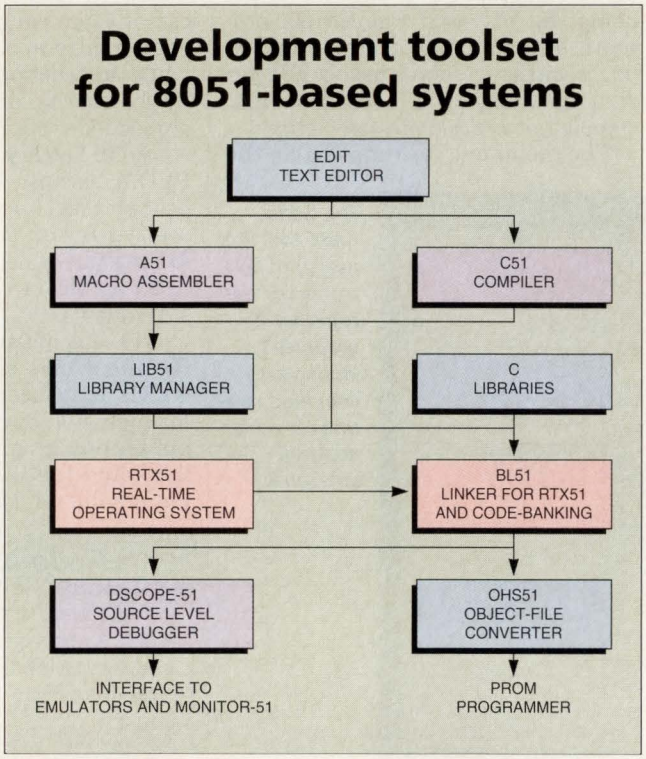
RTX51 is shipped along with a new banking linker called BL51, which supports up to 16 banks of memory for code and data, letting users develop programs of up to 1 Mbyte. BL51 has an automatic analysis feature that analyzes the code and inserts intrabank jumps only where needed. The linker automatically creates a jump table for program calls to different memory banks, reducing memory and stack overhead.

Also shipped with RTX51 is the source code for RXTINY, a reduced version of the operating system supporting only round-robin scheduling. RXTINY occupies as little as 800 bytes and can run on single-chip 8051 systems that don't require data memory. Designers can define up to 16 tasks and the abbreviated operating system supports parallel interrupts and signal passing, as well as the operating system's wait function.

In addition, Franklin is shipping a developer's kit that includes its C51 compiler, the A51 macro assembler, the BL51 linker, and the dScope51 debugger/simulator. Source code for the RXTINY abbreviated operating system is included at no extra charge. The C51 compiler supports multitasking and memory bank switching and includes a compile switch called SRC, which generates assembler source code rather than object code. This lets the designer hand-tune the program or parts of it before generating binary code.

The dScope51 debugger/simulator supports the compiler and the macro assembler. It can simulate the entire 8051 CPU along with the peripheral features of most derivatives. Designers can also simulate external I/O events to prototype an entire system before committing to hardware. The debugger/simulator supports a mouse and multiple windows, and can display C source, assembler source or interleaved listings. The dScope51 supports a monitor that occupies 4 kbytes of PROM, 256 bytes of data RAM, a serial interface, and can be installed on any 8051 or derivative system.

The RTX51 operating system is priced at $1,995 which includes a one-time license for embedding in any products. The developer's kit is priced at $1,995. — *Tom Williams*



The complete set of Franklin development tools for 8051-based systems includes the RTX51 real-time executive and a simulator/debugger that lets designers simulate almost all derivatives in the 8051 family.

Franklin's 8051 tool at a glance

- Multitasking operating system that supports 8051 memory and I/O model
- Preemptive task switching or round-robin scheduling available
- Bank switching linker generates jump tables
- C51 compiler generates assembler listings or binary files
- Debugger for C source or assembler
- Simulator supports most 8051-derivative hardware
- Abbreviated operating system supplied free as source code

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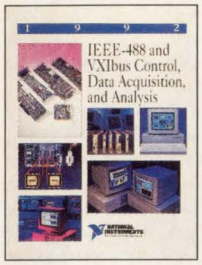

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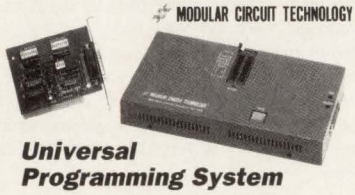

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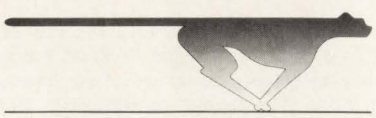

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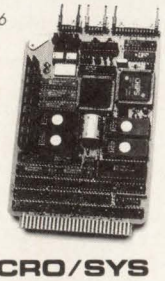

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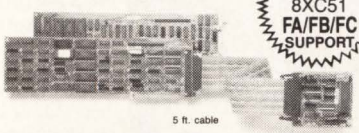

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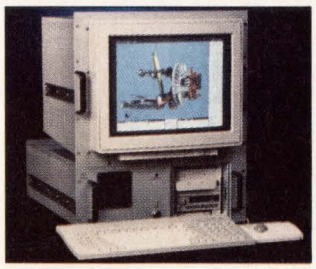

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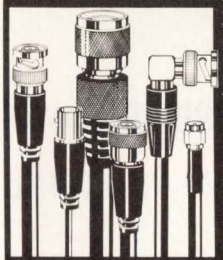

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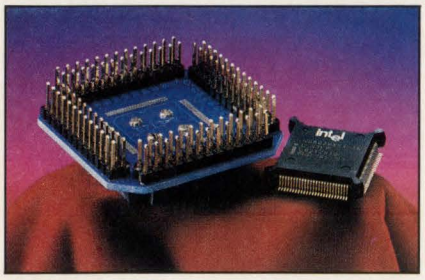

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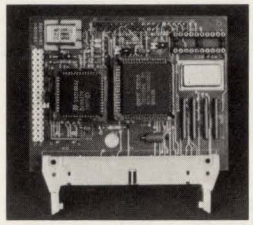

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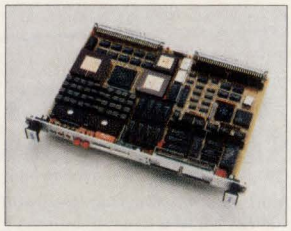

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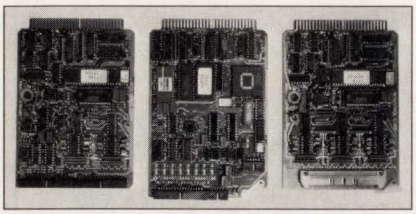

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SysComp/92 West PREVIEW

SysComp/92 West — it's about OEM systems design

A successful product—one with all the performance and features demanded by the marketing people, one that's world-class in quality, competitively priced and brought to market quickly, requires an understanding of how all the components and subsystems come together and all of the trade-offs that have to be made from the day product development begins. More correctly, from the day the product is *conceived.* That's what OEM systems design is all about and it's what SysComp is all about.


San Jose McEnery Convention Center

(continued on page 2)

SYSCOMP FEATURES:

- OVER 100 SYSTEMS, SUBSYSTEMS EXHIBITORS
- FULL 50 SESSION TECHNICAL PROGRAM *(registration form inside)*
- RAYTHEON PATRIOT MISSILE DISPLAY
- REDUCED TUITION FOR ADVANCE REGISTRATION
- FREE TICKET TO EXHIBITS *(inside)*
- SPECIAL EVENTS AT SHOW:
  - *Presidents' Night*
  - *All-industry party*
  - *Keynote address*

And a RISC Conference, too

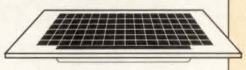
RISC processors aren't restricted to workstations. They're also making in-roads into a wide variety of products and systems that require embedded control—laser printers, network routers and robots, for example. Because of the key role that RISC will play in systems ranging from robots to workstations, RISC '92 has been organized to run in conjunction with SysComp/92 West. As the *only* technical conference devoted *exclusively* to RISC processors, RISC-system architectures and RISC software and software development tools, RISC '92 will provide a wealth of practical, hands-on, application-oriented information you could find nowhere else. With its 60+ lectures and tutorials, RISC '92 is a must for anyone designing products that incorporate a RISC processor, or for key members of concurrent engineering teams developing a RISC-based product.

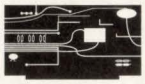
Welcome to SysComp

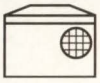
COME TO SYSCOMP FOR TECHNICAL INFORMATION ON THESE PRODUCTS:

- HIGH-PERFORMANCE ICS
- REAL TIME/ EMBEDDED SOFTWARE
- POWER SOURCES
- DISPLAY DEVICES
- STORAGE DEVICES
- BACKPLANES & ENCLOSURES
- I/O DEVICES
- BOARD-LEVEL PRODUCTS
- OEM COMPUTERS









THANKS ... TO THESE COOPERATING PUBLICATIONS:

- COMPUTER DESIGN
- SYSTEMS INTEGRATION
- ELECTRONIC BUYERS' NEWS
- ELECTRONICS
- MILITARY & AEROSPACE ELECTRONICS
- ELECTRONIC DESIGN
- ASIAN COMPUTER SOURCES
- EE TIMES
- ELECTRONIC BUSINESS
- ELECTRONIC NEWS

(continued from page 1)

There are conferences and exhibitions devoted to disk drives, to power supplies, to display technology. There are conferences and shows that concentrate on computers, on software, on programming. There are seminars on project management and concurrent engineering. But there's never been a conference or exhibition that brought all of these together. *Until now!*

If you're a design engineering manager, a systems designer, a senior design engineer or a member of a concurrent-engineering product-development team, you know that it takes more than specialized knowledge of narrowly defined component or technology areas to be successful. Yes, expertise about bus architectures, disk drives, power supplies, user interfaces and software are all essential to creating a product. But you need more.

The SysComp/92 West Technical Development Program has been organized with system requirements and trade-offs always in mind. Individual presentations will be devoted to system and bus architectures, mass storage technology and the impact of new development s on performance and cost, display and interface technology, power sources and power management, OEM systems programming, system packaging and manufacturing. But regardless of the specific topic, the focus is the system as a whole and how the choice of all of the system components affects performance, cost, quality and time-to-market.

SPECIAL FEATURES—

PATRIOT MISSILE

By special arrangement with Raytheon a display of the now famous Patriot Missile will be featured on the show floor.

KEYNOTE ADDRESS / PRESIDENTS' NIGHT

Keynote Address - Tuesday, February 15th 5-6 P.M. Immediately following the Keynote Address, Presidents and CEOs from exhibiting companies will be at hand in their booths to greet attendees in person. Complimentary refreshments will be served.

ALL-INDUSTRY RECEPTION

Wednesday 5–8:00 P.M.. A special industry reception will take place for all exhibitors and attendees. This will provide a special time for attendees and exhibitors to network and establish new relationships or renew old ones.

What is SysComp?

THE INDUSTRY'S FIRST EXCLUSIVE OEM SYSTEMS/SUBSYSTEMS COMPONENTS CONFERENCE & EXHIBITION

SysComp is the only conference/exhibition specifically designed for those of you with the engineering/technical responsibility for designing and integrating OEM systems and subsystems. If you specify and/or integrate building blocks for commercial, industrial, and military/aerospace applications, you can't afford to miss SysComp/92 West.

THE SYSTEMS ENGINEERING TECHNICAL DEVELOPMENT PROGRAM

More than 50 sessions

The SysComp Systems Engineering Technical Development Program provides a fresh, systems-oriented view of microprocessors, OEM software, interface technology, power sources, mass storage, OEM computers, systems packaging and manufacturing, and reliability. It's a forum where you can interact with other OEM systems engineers, exchange ideas and learn about new developments and solutions that you can immediately apply to your applications.

THE EXHIBITORS

SysComp is proud to present a comprhensive list of world class exhibitors. These exhibitors will display a full range of critical systems building blocks including software, boards, complex microcircuits, power sources, storage systems, displays, packaging and other ancillary products and services.

THE ATTENDEES

Attending SysComp/92 West will be design engineering managers, systems engineers and senior design engineers. Also attending will be managers responsible for QA/QC, test, manufacturing and purchasing/procurement. They'll be representing all major industries such as military/aerospace, automotive, communications, medical equipment, industrial control, test equipment and consumer electronics, nor to mention computers and computer peripherals. SysComp/92 West is a unique opportunity for you to mingle with the key people responsible for getting state-of-the-art products to market quickly.

EXHIBITORS FROM COMPANIES SUCH AS:

Adaptec
AT&T
Borland International
Cache Computer
DDC Pertec
Elma
Heurikon
IBM
Intel
Interphase
Motorola
Maxoptix
Maxtor
Mistumi
Schroff
Silicon Systems
Synergy Micro Systems
and more

SysComp

SysComp/92 Technical Program

TUESDAY

8:30 - 10:45

101 Implementing a Six-Sigma program

Paul Noakes, Motorola

Six-Sigma quality has become synonymous with world-class quality standards. This tutorial outlines the basic steps to establishing a Six-Sigma program beginning with data collection and benchmarking through closer, more responsive relationships with suppliers.

102 Electro-mechanical design automation: getting to market first

Edwina Wedeking, SDRC

This tutorial describes how system designers can help speed the integration of electronic and mechanical design by correlating design automation data and working early in the design cycle with the mechanical design team to prevent integration and reliability problems.

8:30 - 9:30

103 Impact of new floppy disk technologies on system design

J. Leland Strange, Brier Technology

New technologies, in concert with developments in interface and controller design, promise to boost floppy disk storage technologies to 50 Mbytes and beyond. This discussion reviews the latest developments in high-density media, SCSI and caching controllers, embedded servo and zonal recording techniques, and discusses their combined impact on system performance.

104 Advances in rechargeable batteries and the impact on system design

Jon S. Eager, Gates Energy Products

Much of the explosive growth in portable electronic products stems from improved rechargeable battery performance. This presentation will focus on the latest developments in nickel-metal hydride, its performance compared to traditional nickel-cadmium, and the benefits and liabilities of both technologies.

9:45 - 10:45

113 State of the art in text-to-speech conversion

Michael H. O'Malley, Berkeley Speech Technologies

While it's now possible to add text-to-speech conversion technology to virtually any system, it still usually requires access to some kind of system processor, a digital signal processor, and memory to store rules which model human speech production. This session examines the variety of methods available to system designers and the hardware and software implications of adding such capability.

114 Minimizing shock and vibration in disk drives

Steve Cornaby, Connor Peripherals

This session describes some of the intense shock and vibration forces portable system designers must contend with and reviews how disk drive designers are attempting to cope with high rotational and lateral accelerations through on-board intelligence and mechanical approaches.

11:00 - 12:00

121 Advances in small-format Winchesters for portable systems

John Klonick, Quantum

This presentation steps through the variety of issues designers must assess from traditional desktop criteria such as capacity, reliability and form factor to issues that play a pivotal role in the success of a portable system including spin-up time, power consumption, acoustic noise, and weight.

122 Selecting and integrating touch-screen technology

Wayne Wehrer, Carroll Touch

This lecture describes the touch-screen options available, their respective advantages and disadvantages and what effect each technology selection has on system cost, software development, manufacturability, and product-development time.

123 Implementing distributed power systems

Kerry Glover, AT&T

Designing a distributed power system around dc/dc converters is not as straightforward as it may seem. This session outlines a few of the issues designers must consider including the operating parameters of the individual converters, noise generated by the equipment connected to the bulk distribution system, isolation between the input and output of each converter, and the overall configuration of the system.

124 Minimizing life-cycle costs for new PCB designs

Michael Carpenter, Electronic Design Tools

This presentation outlines the characteristics of an ideal CAD/CAE/CAM system and how those features can minimize the costs of PCB designs. Discussion topics include integrated databases, automatic forward and backward annotation from schematic and layout, automatic verification of layout, tracking and recording revisions, and rework and documentation aids.

SysComp Technical Program—at-a-Glance

DAY / TIME	8:30 - 9:30	9:45 - 10:45	11:00 - 12:00	2:00 - 3:00	3:15 - 4:15
TUESDAY	**101** Implementing a Six-Sigma program		**121** Advances in small-format Winchesters for portable systems	**131** Designing for testability	**141** Benchmarking real-time systems
	102 Electro-mechanical design automation: getting to market first		**122** Selecting and integrating touch-screen technology	**132** Using memory cards in portable PCs	**142** Specifying switching power supplies
	103 Impact of new floppy disk technologies on system design	**113** State-of-the-art in text-to-speech conversion	**123** Implementing distributed power systems	**133** Meeting ISO 9000 quality requirements	**143** System implications in the use of optical storage
	104 Advances in rechargeable batteries and the impact on system design	**114** Minimizing shock and vibration in disk drives	**124** Minimizing life-cycle costs for new PCB designs	**134** Primary battery options for portable electronics	**144** Design issues for embedded PCs
WEDNESDAY	**201** Issues in the design of backplane-based systems		**221** SBus as an I/O bus	**231** Futurebus+ for next-generation systems systems	**241** Minimizing the effects of power supply harmonics on the system
	202 Critical issues in military systems design		**222** Using SCSI to implement a RAID architecture	**232** Emergence of standards for real-time applications	**242** The impact of the SCSI on disk drive technology
	203 Determining the true reliability of Winchester drives	**213** Re-engineering the real-time/embedded application	**223** Practical guidelines for the design of LCD panel interfaces	**233** Integration of OEM cartridge drives	**243** Choices in development platforms for real-time systems
	204 Overview of EMI/RFI issues	**214** Trade-offs in the design of front-ends for distributed power systems	**224** Issues in desktop connectivity	**234** Using on-line databases to speed OEM system designs	**244** Integrating input technologies beyond the keyboard: keypads, bar code, mag stripe
THURSDAY	**301** Managing large system-development projects		**321** Partitioning disk drive electronics between the drive and the system	**331** Issues in integration of gigabyte capacity magnetic drives	**341** Design considerations in using DAT drives
	302 Concurrent engineering in electronic and computer system design		**322** Technology trends in LCDs	**332** Integrating backup drives UPS into systems	**342** Incorporating data communications boards into system designs
	303 Power conservation issues in laptops and notebook computers	**313** Selection and integration criteria for monitors	**323** Software testing for customer satisfaction	**333** Software architecture simulation for real-time embedded systems	**343** Implementing the HIPPI interface
	304 Testing embedded disk drives	**314** Evaluating the cost and performance of packaging system designs	**324** SCSI-2 as a peripheral I/O bus	**334** Building multitasking tape backup systems	**344** OEM issues in integrating LCD panels

SysComp/92 Technical Program — Continued

2:00 - 3:00

131 Designing for testability

Asghar Noor, Motorola/Codex

Today's complex systems demand a design for testability approach that encompasses all aspects of the system from the individual ICs to the board and system level. This presentation proposes a new design methodology that, supported by an integrated modeling environment, will verify the correctness of a design while leaving enough hooks to let designers test against manufacturing-related defects.

132 Using memory cards in portable PCs

Pratix Parikh, VLSI Technology

Advances in memory density and packaging technology have led to memory cards that offer storage capacities competitive with floppy drives. This lecture reviews the latest specifications for a memory card's hardware and software interface and delineates how designers can take advantage of these standards through an in-depth look at a typical portable system.

133 Meeting ISO 9000 quality requirements

Donald Harris, DiagSoft

This paper reviews the ISO 9000 series of standards that establish a model for quality assurance at all stages of the product-development process. It explains the three quality models integral to the ISO 9000 standards and how system makers can comply with those requirements.

134 Primary battery options for portable electronics

David Linden, Duracell

The rechargeable nickel-cadmium battery is no longer considered the single battery of choice for portable electronics. This presentation explores primary, replaceable batteries as an option. It compares and contrasts primary and secondary battery features and examines their performance and cost trade-offs.

3:15 - 4:15

141 Benchmarking real-time systems

Daniel G. Fritch and Reed W. Cardoza, Eyring

This session uses independent test results to compare the real-time performance of leading real-time vendors and to demonstrate that off-the-shelf kernels can provide performance comparable to proprietary custom designs. The discussion includes an in-depth review of how the benchmark tests were developed.

142 Specifying switching power supplies

Peter Gaujewski, Shindengen America

While it plays a critical role in system performance, the power supply still remains the last-selected and least-understood component in many systems. This session outlines the wide range of issues a system designer must consider including footprint, topology, reliability, and output before selecting the right switching power supply for a system.

143 System implications in the use of optical storage

Kent Ekberg, Pioneer

While multifunction optical drives alleviate the need for choosing between write-once and erasable systems, they still leave a number of decisions to the system designer. This session will define what a multifunction drive can do, look at the three technological approaches drive vendors use, and identify which applications are best served by which technologies.

144 Design issues for embedded PCs

Rick Lehrbaum, Ampro Computer

The IBM PC has evolved into a system-level standard thanks to its widespread and familiar hardware architecture and its pervasive software applications base. This presentation reviews the advantages and disadvantages of using the architecture in embedded applications and examines where the PC architecture can accelerate the development of embedded designs.

WEDNESDAY

8:30 - 10:45

201 Issues in the design of backplane-based systems

Bill Fujitsubo, Engineering Solutions

Transmission-line design is a foreign term to many designers. This workshop attempts to familiarize system designers with the problems they can expect to encounter in any backplane-based system. In particular, it focuses on the intricacies of controlling impedance in higher-speed systems with rise times approaching 1 ns.

202 Critical issues in military systems design

Tobias Nagle, Military & Aerospace Electronics

Increasing pressure on the defense budget will force military system designers to find new cost-effective ways to upgrade existing inventory. This session looks at the technology already available to the military in the commercial sector and how designers can take advantage of the cost and performance advantages of off-the-shelf products while coping with the Pentagon's entrenched approach to system design.

8:30 - 9:30

203 Determining the true reliability of Winchester drives

Dennis Hill, Fujitsu Computer Products

Reliability has been a key factor in the development of the Winchester disk drive. This presentation reviews the most common causes of disk drive failure — shock, thermal change and mechanical malfunctions — and gives system designers a formula for estimating true disk drive reliability.

204 Overview of EMI/RFI issues

Ron Brewer, Instrument Specialties

This session looks at the myriad issues involved in tackling EMI/RFI problems. After a general overview of the cause of the problem, it outlines the basic commercial and military requirements for EMC, shielding and RF gaskets and how designers can meet those needs.

9:45 - 10:45

213 Re-engineering the real-time/ embedded application

Jerry Fiddler, Wind River Systems

Topics covered in this presentation include a review of current embedded systems development technologies, the migration from in-house systems software and tools to third-party solutions, and a discussion of the anticipated effects of next-generation embedded systems development tools on traditional engineering paradigms.

214 Trade-offs in the design of front-ends for distributed power systems

Steve Hall, Brandt Electronics

While most of the attention in the design of distributed power systems has focused on the local dc/dc converters, the front-end ac/dc converter also plays a prominent role in system performance. This presentation discusses the pros and cons of designing a front-end in-house, building a front-end from commercially available modules, or buying a complete front-end.

11:00 - 12:00

221 SBus as an I/O bus

Speaker to be announced, Sun Microsystems

An in-depth discussion of the technical attributes of the SBus will outline the benefits of the architecture as an I/O bus. Topics covered include hardware design, DMA control, firmware, programming environments, and device drivers.

222 Using SCSI to implement a RAID architecture

Keith B. Dalec, NCR Peripheral Products

Using simulation results, the speaker demonstrates how a system designer can configure host SCSI channels to reach performance goals. Included is an examination of the trade-offs designers must make in total storage capacity, RAID levels, transaction rates, system logical block size, SCSI bus overhead, utilization, and bandwidth to arrive at the optimum configuration for a particular installation.

223 Practical guidelines for the design of LCD panel interfaces

David Fong, Cirrus Logic

While LCD manufacturers typically provide specifications to their panels, they rarely instruct the system designer how to quickly, safely and reliably interface the panel to the rest of the system. This presentation reviews the specifications most manufacturers provide and then suggests a series of basic principles to help designers build manufacturable and reliable interfaces.

224 Issues in desktop connectivity

Ata Kahn and Greg Goodhue, Signetics

Desktop connectivity has become a major issue in system design. This session identifies the criteria for evaluating a desktop bus or interconnect from data transfer rates and protocol flexibility to ease of implementation. It also compares the performance and cost implications of the typical desktop connectivity alternatives.

2:00 - 3:00

231 Futurebus+ for next-generation systems

Harrison Beasley, VITA

Futurebus+ is the future of standard-board computer architectures. This session reviews the architectural and design concepts behind Futurebus+ and how system designers can best utilize its enhanced parallel protocol, cache coherence and message-passing capabilities to reach the next level in system performance.

232 Emergence of standards for real-time applications

Inder M. Singh, Lynx Real-Time Systems

While the real-time world is currently dominated by multiple proprietary operating systems and kernels, it is moving to open systems based upon the emerging IEEE Posix standards. This presentation examines the two recently proposed standards for extended operating system support, Posix.4 and Posix.4a, to see if they really provide the necessary facilities to support real-time systems. It looks at what Posix provides for the real-time developer, where it is deficient and how the designer can use the standard to start building portable, real-time systems.

233 Integration of OEM cartridge drives

Stan Miller, 3M

Transfer rate, interface, form factor, compatibility, and price all play a part in tape backup selection. This presentation reviews the critical issues system designers must consider when integrating a cartridge drive into their systems and how technology developments in quarter-inch data cartridge technology will impact those decisions.

234 Using on-line databases to speed OEM system designs

Steven R. Petersen, Achiever's Edge

How can system designers make the best use of on-line databases of new technologies, manufacturing processes, standards, and component specifications? This session offers an overview of the major on-line systems available and demonstrates how they might be used through two in-depth applications.

3:15 - 4:15

241 Minimizing the effects of power supply harmonics on the system

Forrest Sass, Computer Products

All systems sold into the European market by 1995 will have to meet IEC 555.2, the European regulation designed to limit pollution of the ac line by power supply harmonics. This session explores the system design ramifications of the specification and the approaches to controlling harmonic distortion.

242 The impact of SCSI on disk drive technology

Gene Milligan, Seagate Technology

Over the last decade, SCSI has attracted a growing number of adherents because it allows significantly more freedom for advancement and control of the drive's technology. This presentation reviews the evolution of SCSI and ways designers can best utilize its attributes to achieve their specific design goals.

243 Choices in development platforms for real-time systems

Daniel G. Fritch and Walt C. Jones, Eyring

The tools available to the developer of real-time systems can be as important to a project's success as the selection of the target hardware and operating system. Once a developer is familiar with a particular tool set, changing platforms can result in a significant short-term loss of productivity. This paper outlines the various platforms available and offers solutions that allow different platforms to synergistically work together to solve a common application.

244 Integrating input technologies beyond the keyboard: keypads, bar code, mag stripe

Speaker to be announced

Innovative uses of new input technologies will be a key factor in the success of portable electronics systems. This session describes the range of options available to the designer seeking solutions other than the traditional keyboard and the power, ergonomic and interface implications of each alternative.

THURSDAY

8:30 - 10:45

301 Managing large system-development projects

Richard C. Jensen, Applied Microsystems

Thanks to rapid advances in microprocessor technology, embedded applications have grown by more than an order of magnitude in size over the past decade. Today, it's not uncommon to find embedded systems containing over a megabyte of code and data. Controlling and coordinating these large-scale development projects can pose new and formidable challenges for the project manager. This tutorial identifies some of the more common mistakes managers make transitioning from smaller to larger projects and suggests new management methods to tackle these problems.

302 Concurrent engineering in electronic and computer system design

Jon Turino, Logical Solutions

Concurrent engineering is a discipline for continuous product and process design improvement that supports and enables Total Quality Management and Computer Integrated Manufacturing. This seminar not only explains what concurrent engineering is, but offers a specific step-by-step plan to implement the discipline within an organization.

8:30 - 9:30

303 Power conservation issues in laptop and notebook computers

Ahmet Alpdemir, Chips & Technologies

Using simulation data of the same notebook system designed with different power-management techniques, this session offers some startling insights into which power-management techniques really work. The speaker outlines the basic techniques needed to compete with most low-power designs as well as identifying a few approaches often considered mandatory to limit power consumption, that may not be worth the effort.

304 Testing embedded disk drives

Thomas W. Martin, Adaptec

Traditional test methods won't work with disk drives featuring embedded intelligence. This discussion reviews the challenges designers using embedded SCSI drives confront and offers new test strategies that focus on time-to-data, self-test and logical block addressing.

9:45 - 10:45

313 Selection and integration criteria for monitors

Speaker to be announced, Zentec

This session discusses the basic specifications of a monitor and explains how to interpret the relationship between resolution, vertical refresh rates, horizontal frequency, dot pitch, interlacing, and video bandwidth. An overview of trends in monitor technology will help designers identify which monitor is appropriate for their application and what impact their selection will have on system performance.

314 Evaluating the cost and performance of packaging system designs

Jeff Dieffenbach and Lee Ng, IBIS Associates

In the design of electronics packaging systems, there is rarely a material or technology that delivers the best solution for all design criteria. The speakers in this session present a methodology for evaluating the cost and performance of complete packaging system designs for the same application through the use of simulation and cost models.

11:00 - 12:00

321 Partitioning disk drive electronics between the drive and the system

Tim Jackson, Silicon Systems

The continuing shrinkage of Winchester disk drives has forced both system and disk drive designers to ever-higher levels of integration. This session looks at some of the power-management issues and packaging considerations those designers must consider as they distribute the control and interface electronics between the drive and the system.

322 Technology trends in LCDs

Steve Sedaker, Sharp Electronics

An overview of the manufacturing process will explain how recent developments will enhance the yields and performance of next-generation LCDs and how those panels will compare with alternative flat panel technologies on the cost/performance scale.

323 Software testing for customer satisfaction

Speaker to be announced, Motorola

Traditional formal methods of software testing find several classes of bugs, but a large number of problems can only be discovered by acting as an "ignorant" user. This presentation shows a development team how to become an alpha site, emulate some of the real-world problems users confront and locate those problems in hardware, software, requirements and documentation.

324 SCSI-2 as a peripheral I/O bus

Gary Crow, Ciprico

The latest ANSI SCSI-2 specification adds a number of features of special interest to system designers. This session outlines the various device-level and peer-to-peer interfaces available to designers and how SCSI-2 systems differ. Using examples, it reviews how the new SCSI-2 features are being implemented and the impact they have on system performance.

2:00 - 3:00

331 Issues in integration of gigabyte capacity magnetic drives

Jonathon Hubert, Maxtor

Increasing market penetration by 3.5-in. Winchesters has driven up the performance and capacities of 5.25-in. drives into the gigabyte range and beyond. This session reviews the new issues that system designers must address as they integrate extremely high capacity drives into their systems including the impact of SCSI-2, the options the interface presents, how system designers might have to change their system configuration, and how costs are changing.

332 Integrating backup UPS into systems

Dave Kemp, Sola

With systems operating at lower and lower voltages, power quality has quickly become a major issue for system designers. One way to compensate for poor power quality is to integrate an uninterruptible power supply into the system. This presentation looks at the system implications of taking such a strategy.

333 Software architecture simulation for real-time embedded systems

Joseph Rothman and Gabi Leshem, Ready Systems

A software architecture simulation can pay significant dividends in real-time applications. This paper explains how a simulator, in conjunction with a generic front-end CASE tool, can minimize the damage caused by improper design decisions made early in the design.

334 Multitasking tape backup systems

Speaker to be announced, Cipher Data

Although PC networks have begun to emulate mainframe environments in processing power and utility, they lag far behind in terms of a fast, low-cost, universally accepted off-line storage solution. This paper reviews the diverse and generally incompatible off-line storage method available, describes what defines the data interchange and capacity limitations of available technologies and describes the ideal system solution.

3:15 - 4:15

341 Design considerations in using DAT

Speaker to be announced, Hewlett-Packard

Available since 1987, Digital Audio Tape has quickly emerged as a viable backup technology. This paper reviews the latest developments in DAT technology and examines how an emerging ANSI standard and increasing capacities will help make the technology increasingly attractive to system designers.

342 Incorporating data communications boards into system designs

Sam Perry, SBE

Data communications boards using high-speed protocols demand a new approach by system designers. This paper examines the bus bandwidth, protocol processing, network management, physical connectivity and interoperability considerations presented by high-speed serial and FDDI technologies.

343 Implementing the HIPPI interface

Ken Bisson, Aptec Computer Systems

For many system vendors, the High Performance Parallel Interface offers a way to circumvent single-vendor dominance in high-performance computers and peripherals. This session will provide background on the HIPPI standard and how it can impact system performance.

344 OEM issues in integrating LCD panels

Paul Gulick, In-Focus Systems

OEMs must choose between a number of LCD technologies and must calculate how their selection will impact performance, manufacturability, cost, service, and support. A close look at the relative merits of triple super-twisted nematic, thin-film transistor and active matrix technologies and the integration challenges each poses will help simplify the decision process.

SysComp

Exciting San Jose... the Heart of Silicon Valley

Here's the information you need to make your travel and hotel plans

SAN JOSE HAS IT ALL!

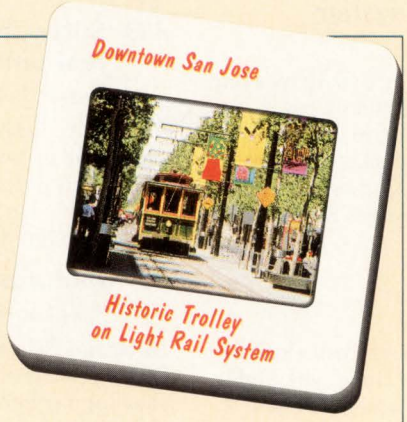
California's third largest city delights visitors with its diversity—world-class museums and galleries, exciting family attractions, nearly 50 award-winning wineries, and 125 beautiful gardens and parks. End your day by dining at one of San Jose's fine restaurants, enjoying the city's festive nightlife, or relaxing in the comfort of one of San Jose's outstanding accommodations.

SAN JOSE'S HISTORIC FIRSTS ...

California's oldest civil settlement, El Pueblo de San Jose de Guadelupe under Spanish rule, was founded in 1777 to raise crops and cattle to feed soldiers encamped at Monterey and San Francisco. In 1850, the settlement officially became the city of San Jose. San Jose is also known as California's first state capital, with the first legislature convening in 1849.

LOCATION: Strategically located at the sunny, southern tip of the San Francisco Bay, San Jose is nestled in the heart of the Santa Clara Valley, surrounded by rolling hills and striking mountains. Within minutes, you can be relaxing at ocean beaches, hiking through scenic recreation areas, or marveling at the majestic California redwoods.

CLIMATE: With nearly 300 days of sunshine, San Jose symbolizes the best that California has to offer. Mid February daytime temperatures average in the high 50's to low 60's. Nights average in the 30's.



GETTING AROUND SAN JOSE:

There's a world of exciting destinations in San Jose. and the "Light Rail" is the best way to get to shopping, hotels, convention center, downtown area, etc. Riders can purchase tickets at the numerous light rails stations. Service runs seven days a week, from 6 am to midnight.

INFORMATION: More information about San Jose is easy to obtain by contacting or visiting one of the city's Visitor Information Centers. Two are located at San Jose International Airport, and a third is located in the main lobby of the Convention Center. In addition to answering any questions you may have about the San Jose area, the experienced staff can provide you with free brochures describing attractions, accommodations, dining, entertainment and recreation.

DINING IN SAN JOSE:

AMERICAN

Grandview
94 Mount Hamilton Rd
408 259 3434 $$

CHINESE

House of Cathay
1339 N.First St. Gish Rd
408 453 8148 $$

Pagoda in the Fairmont Hotel
170 S. Market St.
408 998 3937 $$

CONTINENTAL

Paolo's
520 E Santa Clara St.
408 294 2558 $$$

FRENCH

Emile's Restaurant
545 S. Second St. at Williams
408 289 1960 $$$

Le Papillon
410 Saratoga Ave. at Kiely
408 296 3730 $$$

GERMAN

Hochburg von Germania
261 N. Second St. at Julian
408 295 4484 $$

ITALIAN

The Old Spaghetti Factory
51 N. San Pedro St. at Santa Clara
408 288 7488 $

The Olive Garden
940 Blossom Hill Rd.
at Almaden Expway
408 225 1420 $$

Original Joe's
301 S. First St at San Carlos
408 292 7030
No credit cards $$

Mexican

Carlos Goldsteins
111 50-D Murphy Ave
408 437 1986 $$

$ = Inexpensive
$$ = Moderate
$$$ = Expensive

HOTEL INFORMATION

ALL RESERVATIONS SHOULD BE MADE THROUGH THE SYSCOMP HOUSING BUREAU

CONVENTION HOUSING MANAGEMENT
1625 The Alameda, Suite 707
San Jose, CA 95126
Phone: (408) 283-5280
Fax: (408) 993-0944

HOLIDAY INN-
Park Center Plaza
(Directly across from the Convention Center)
282 Almaden Boulevard
San Jose, CA 95113
Rates: $90/night, Single or Double

LE BARON HOTEL
(Site of the RISC Conference)
1350 N. First Street
San Jose, CA 95112
Rates: $88/Night Single or Double

FAIRMONT HOTEL
170 S. Market Street
San Jose, CA 95113
Rates: $103/Night, Single or Double

SHERATON SILICON VALLEY
1801barber Lane at 880
Milpitas, CA
Rates: $103/Night, Single or Double

AIRLINE INFORMATION

AMERICAN AIRLINES IS THE OFFICIAL AIRLINE OF SYSCOMP.

Substantial discounts are available for SysComp participants traveling from anywhere in the world to any of the three Bay Area airports—San Jose, San Francisco, Oakland—including:

- 5% OFF any promotional fare
- 45% OFF the Coach Fare at the time of ticketing with a 7-day advance purchase
- Rental car reservations for HERTZ or AVIS are also available through American Airlines.

For Reservations and Information on these special discounts, call toll-free:

(800) 433-1790

Toll-free hours:: 8:00 am - 8:00 pm CST
Outside the U.S. call (713) 954-7503 or fax (713) 965-7733.

Mention Star #S0422UY

Registration Form

Name _____ Title _____

Company _____ M/S _____

Street Address _____

City/State/Zip _____

Phone # ( ) _____ FAX # ( ) _____

I WISH TO REGISTER FOR THE FOLLOWING SESSIONS: (CIRCLE)

101	102	103	104	113	114	121	122	123	124	131	132	133	134
141	142	143	144	201	202	203	204	213	214	221	222	223	224
231	232	233	234	241	242	243	244	301	302	303	304	313	314
321	322	323	324	331	332	333	334	341	342	343	344		

SESSION PACKAGES:

Five (5) Sessions @ $125 ($150 at-the-door) $ _____

Ten (10) Sessions @ $200 ($250 at-the-door) $ _____

Fifteen (15) Sessions @ $275 ($350 at-the-door) $ _____

INDIVIDUAL SESSIONS:

_____ Sessions @ $35 ea ($45 at-the-door) $ _____

Total Technical Development Investment $ _____

☐ Check Enclosed ☐ Please bill my Credit Card:

☐ VISA ☐ Mastercard ☐ American Express

Card #: _____ exp. date: _____ Signature: _____

☐ Count me in for "Presidents' Nite" on Tuesday, February 18th

☐ Please invite my company President Mr./Ms. _____

Please complete this form and mail with proper payment to:

SysComp/92 West
c/o Computer Design
P.O. Box 990
Westford, MA. 01886-9937

For fast action, fax this form to:
(508) 692-7780

Note: This form and the guest ticket below may be duplicated for colleagues.

SYSCOMP FEB 18 -20

ATTEND SAN JOSE

SPECIAL GUEST — REGISTRATION FORM — EXHIBITS ONLY SYSCOMP/92 WEST FEB. 18–20

OPEN TO THE TRADE ONLY. NO ONE UNDER 18 ADMITTED.

Please type or print clearly. One person per form. Photocopy this form for additional registrants.

NAME (FIRST / LAST)

TITLE (M-S)

COMPANY

ADDRESS

CITY (STATE / ZIP)

PHONE (AREA CODE – NUMBER) (COUNTRY)

SysComp

COURTESY OF: COMPUTER DESIGN

Mail by January 17, 1992 for preregistration to:
SysComp/92—West
c/o Computer Design
P.O. Box 990
Westford, MA 01886-9937
or present this ticket at the show.

FREE $10.00

FREE VALUE

I. Job Description (check one)
1. ( ) President, Owner Vice President
2. ( ) Project Manager Senior Engineer
3. ( ) System Engineering Manager
4. ( ) Other Engineering and Engineering Support
5. ( ) Purchasing
6. ( ) Educator
7. ( ) Consultant
8. ( ) Sales/Marketing
9. ( ) Other _____ (please specify)

II. Main Company Activity (check all that apply)
2. ( ) Board Manufacutrer
3. ( ) System Manufacturer
4. ( ) Systems Integrator
5. ( ) Subsystems Manufacutrer
6. ( ) Board/Systems Marketer
7. ( ) Industrial Process Control
8. ( ) Scientific Computation
9. ( ) Commercial/Data Processing
10. ( ) Medical
11. ( ) Communications
12. ( ) Government/Military
13. ( ) Transportation/ Automotive
14. ( ) Aerospace
15. ( ) Consultant
16. ( ) Other _____ (please specify)

III. Area(s) of Main Product Interest (check all that apply)
17. ( ) Storage Devices
18. ( ) Display Devices
19. ( ) Real-time/ Embedded Software
20. ( ) I/O Devices
21. ( ) OEM Computers
22. ( ) Board-Level Products
23. ( ) Backplanes/Enclosures
24. ( ) Power Sources
25. ( ) High Performance ICs

26. Number of Employees in Company (check one)
1. ( ) 1 – 50
2. ( ) 51– 100
3. ( ) 101– 250
4. ( ) 251– 500
5. ( ) 501– 1000
6. ( ) Over 1000

27. Approximate Dollar Sales Volume (check one)
1. ( ) 0 – 100,000
2. ( ) 101,000 – 500,000
3. ( ) 501,000 – 1 Million
4. ( ) 1.1 Million – 5 Million
5. ( ) 5.1 Million – 10 Million
6. ( ) 10.1 Million – 15 Million
7. ( ) 15.1 Million – 50 Million
8. ( ) Over 50 Million

28. Do You Have Purchace or Specification Authority
1. ( ) Yes
2. ( ) No

Here is Your Chance to Win Valuable Borland Software

All registrants at SysComp/92 West are eligible to win their choice of Borland Software. The following three lucky winners have already been chosen in the Advance Registration Drawing:

SEAN LAMB, Sr. Systems Engineer,
Loral Space Info., Houston, TX

Ed Balough, Hdw Mgr.,
UNISYS, San Jose, CA

West Kurihara, Engineer,
NASA, Moffett Field, CA

Three more attendees are still to be chosen from the registrants to SysComp/92 West. Time is running out. Register immediately!

No Matter What the Application,

SBE Fits.

Matching your high-speed data communications requirements with a quality supplier has never been easier. Whether you're a manufacturer of mini/superminicomputers, workstations or high-performance data communications products, *only* SBE provides a perfect fit.

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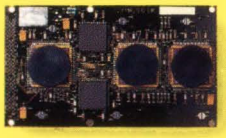
CIRCLE NO. 68

SBE
Communications & Real-time Solutions

HOW SUN SNAPPED UP THE LEAD IN SPARC MULTIPROCESSING.

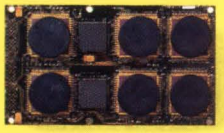
Sun Microsystem's™ new 90 SPEC thruput multiprocessing SPARCserver is powered by our new SPARCore Modules.

We have consistently delivered a performance advantage in SPARC RISC chipsets. Now, we are introducing SPARCore™ high-performance uniprocessing and multiprocessing *Modules*. Cypress modules provide you (and Sun) with significant competitive advantages based on innovative technology:



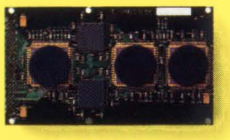
CYM6001K Uniprocessor SPARCore Module

1. Short-Cut to Market. With this much complexity running at 40+MHz speeds, there are non-trivial issues to integrating the CPU chipset. Using our fully integrated, tested SPARCore modules, you save time, not to mention manufacturing and testing costs. We deliver fully tested modules, with MPU, FPU, MMU, and Cache, for the price of the chipset.



CYM6002K Dual Processor SPARCore Module

2. Plug and Play on MBus. You design your system to the MBus standard, and you can plug in modules offering a range of speed/power options, to keep your product current without major redesign. This modular approach provides a designed-in upgrade path to keep you on the leading edge.

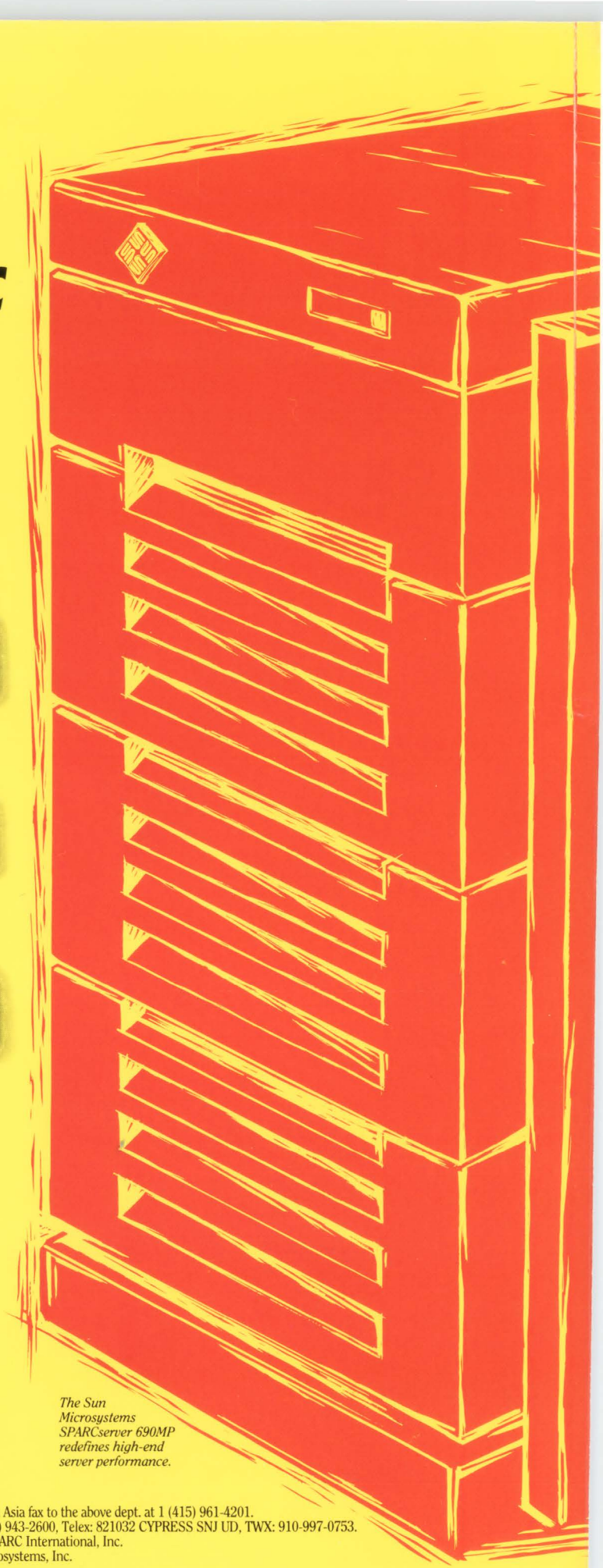


CYM6003K Uniprocessor SPARCore Module for Multiprocessing systems

Call for your Free SPARCore Whitepaper and Data Sheets. Hotline: 1-800-952-6300.* Ask for Dept C11W.

SPARCore
ROSS TECHNOLOGY

CYPRESS SEMICONDUCTOR



The Sun Microsystems SPARCserver 690MP redefines high-end server performance.

*In Europe fax your request to the above dept. at (32) 2-652-1504 or call (32) 2- 652-0270. In Asia fax to the above dept. at 1 (415) 961-4201.