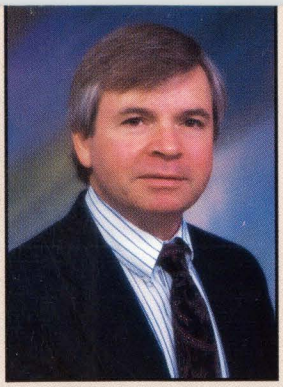


John Nelson on Multimedia

A PENNWELL PUBLICATION APRIL 1, 1991

# COMPUTER DESIGN

Technology and Design Directions®

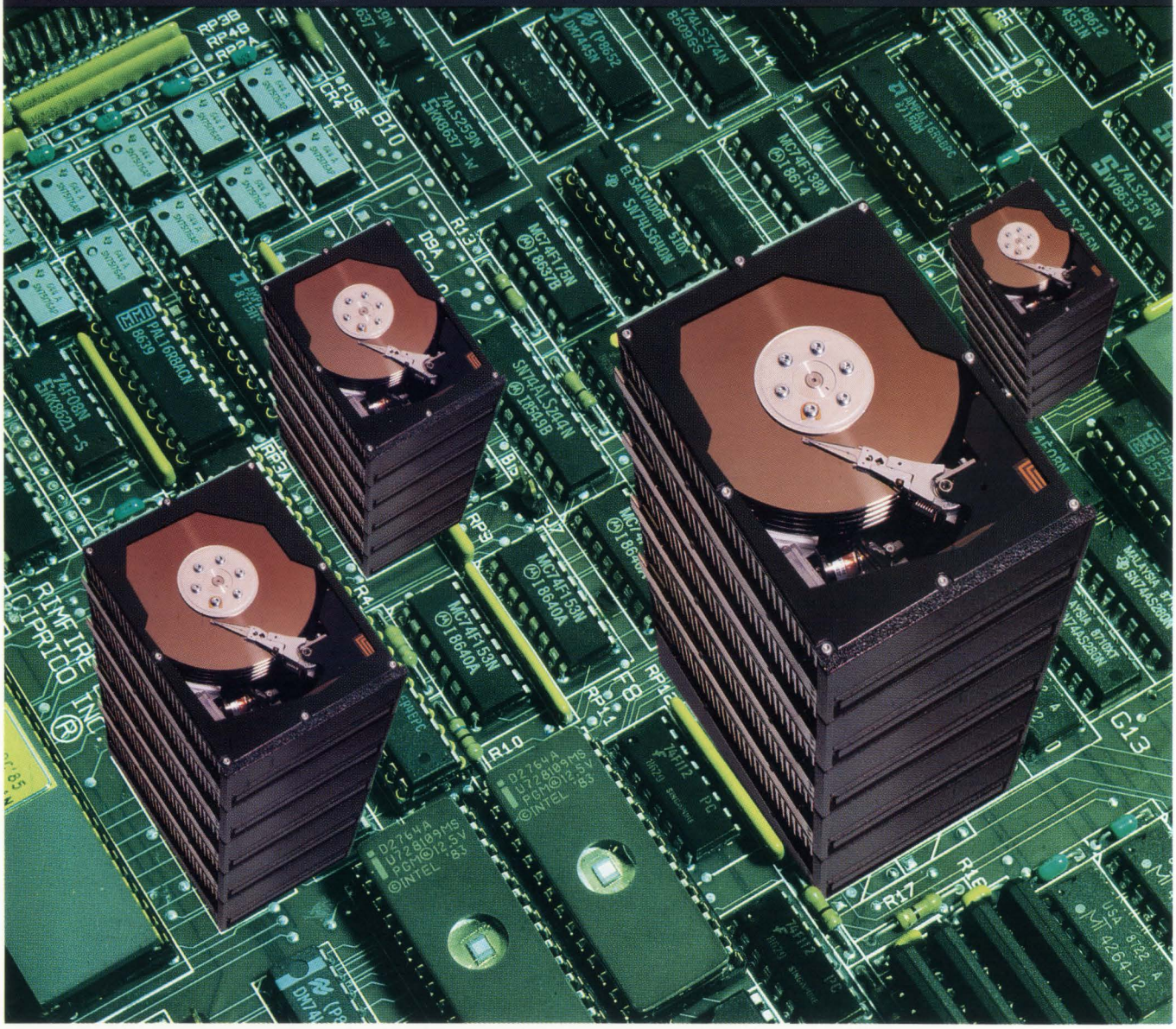
FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

## Designers discover new tools to overcome PCB layout hazards

### High-density ASICs force focus on testability

### Communications standards pit convenience against speed in standard buses

# Unparalleled, parallel performance.

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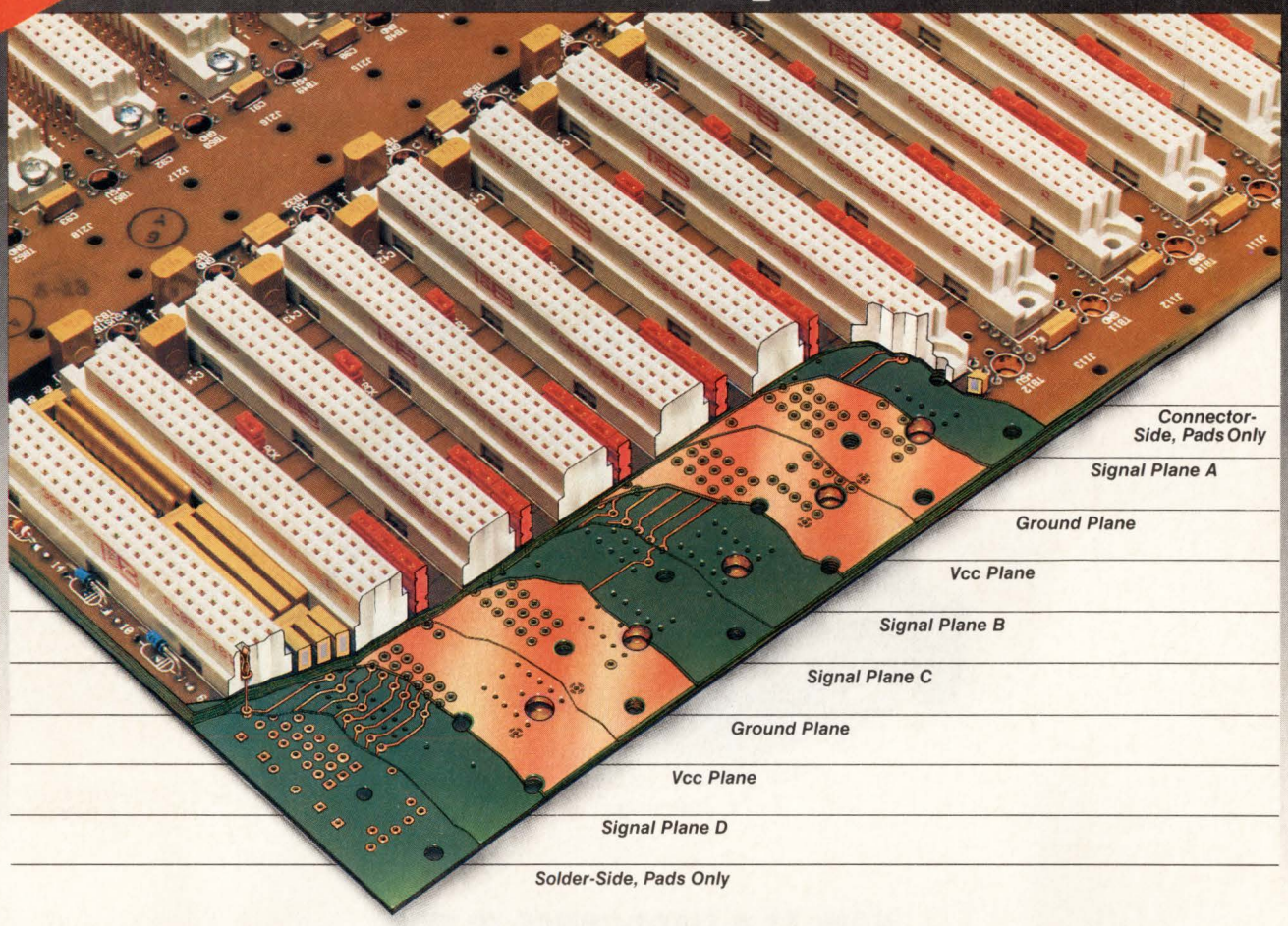
**CIRCLE NO. 1**

New

# 10-Layer VME Backplane!

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Look inside the first truly reliable, glitch-free VME backplane and you'll see the logic behind each detail of its design.

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There's more logic on the outside. Schottky diode terminations. Interrupt and Bus Grant jumpers accessible from either side. Wire wrap pins with shrouds on the end slots of the J1 and every slot of the J2. Ground pins in between J2 slots to provide I/O cabling with interstitial grounds. And much more.

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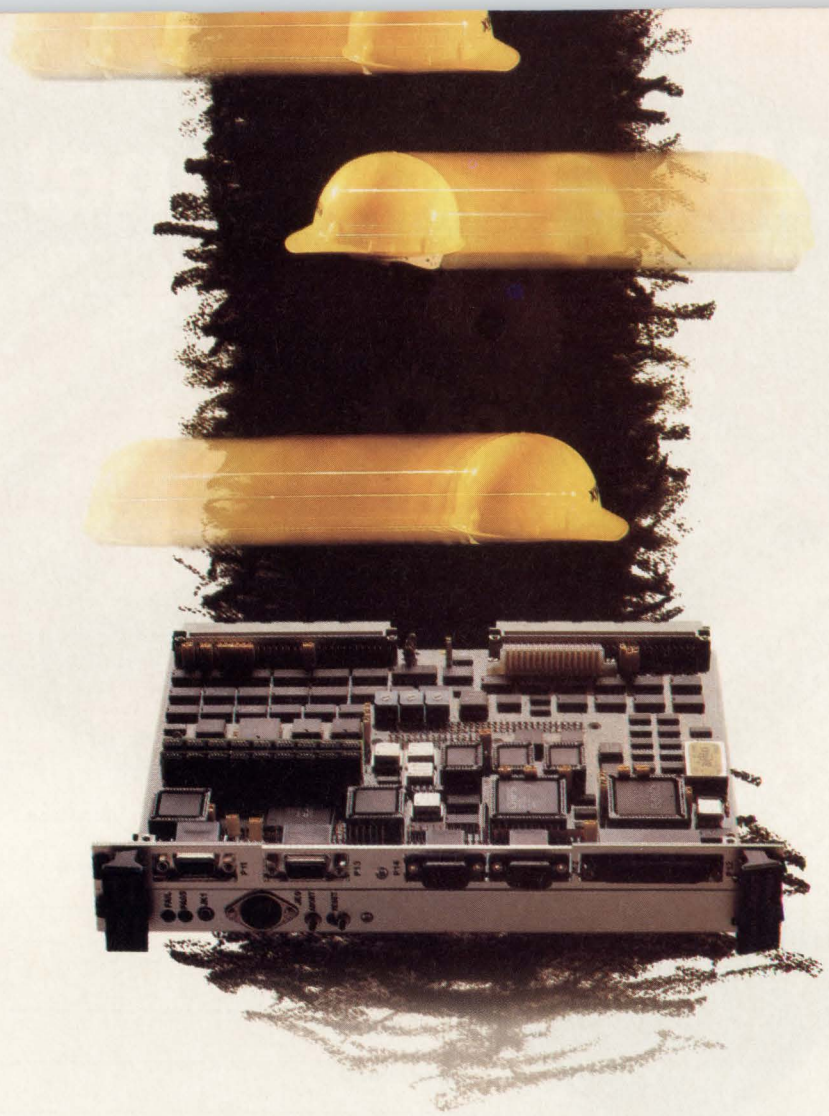

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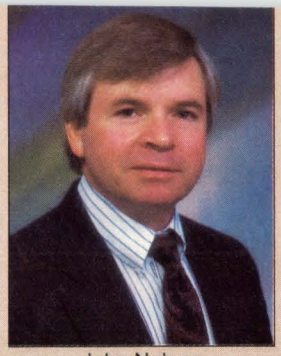
VOL. 30, NO. 7 APRIL 1, 1991

# COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



John Nelson on Multimedia
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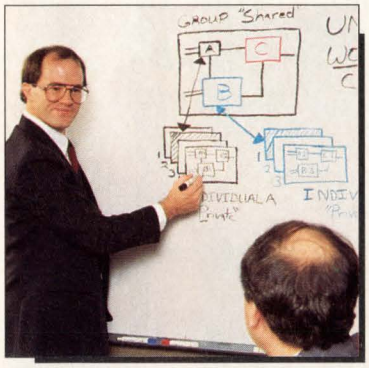

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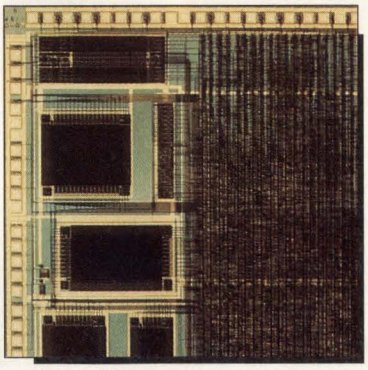
## TECHNOLOGY UPDATES





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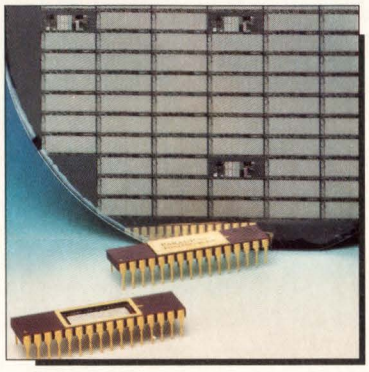
## TECHNOLOGY AND DESIGN FEATURES





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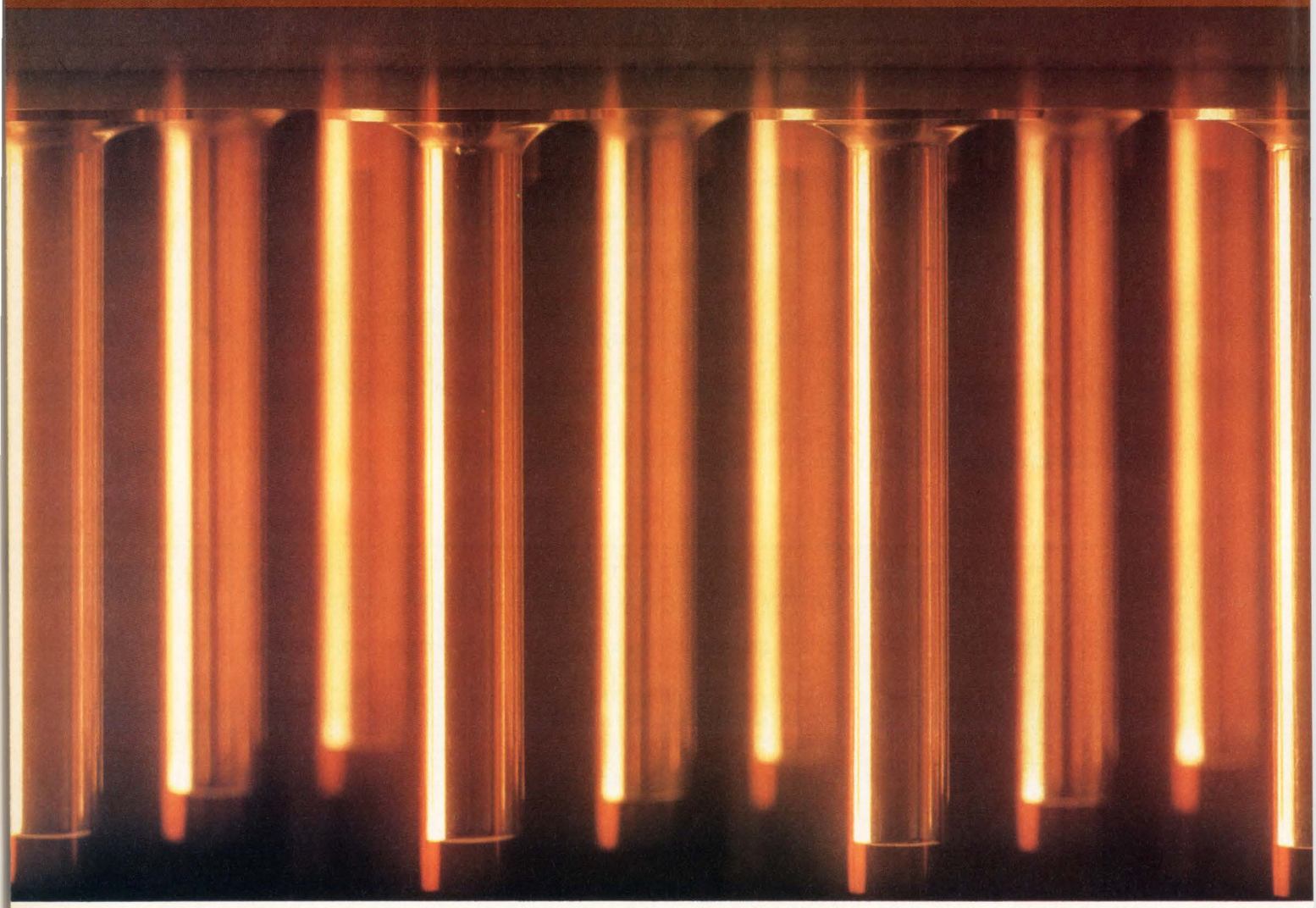
## NEW PRODUCT HIGHLIGHTS



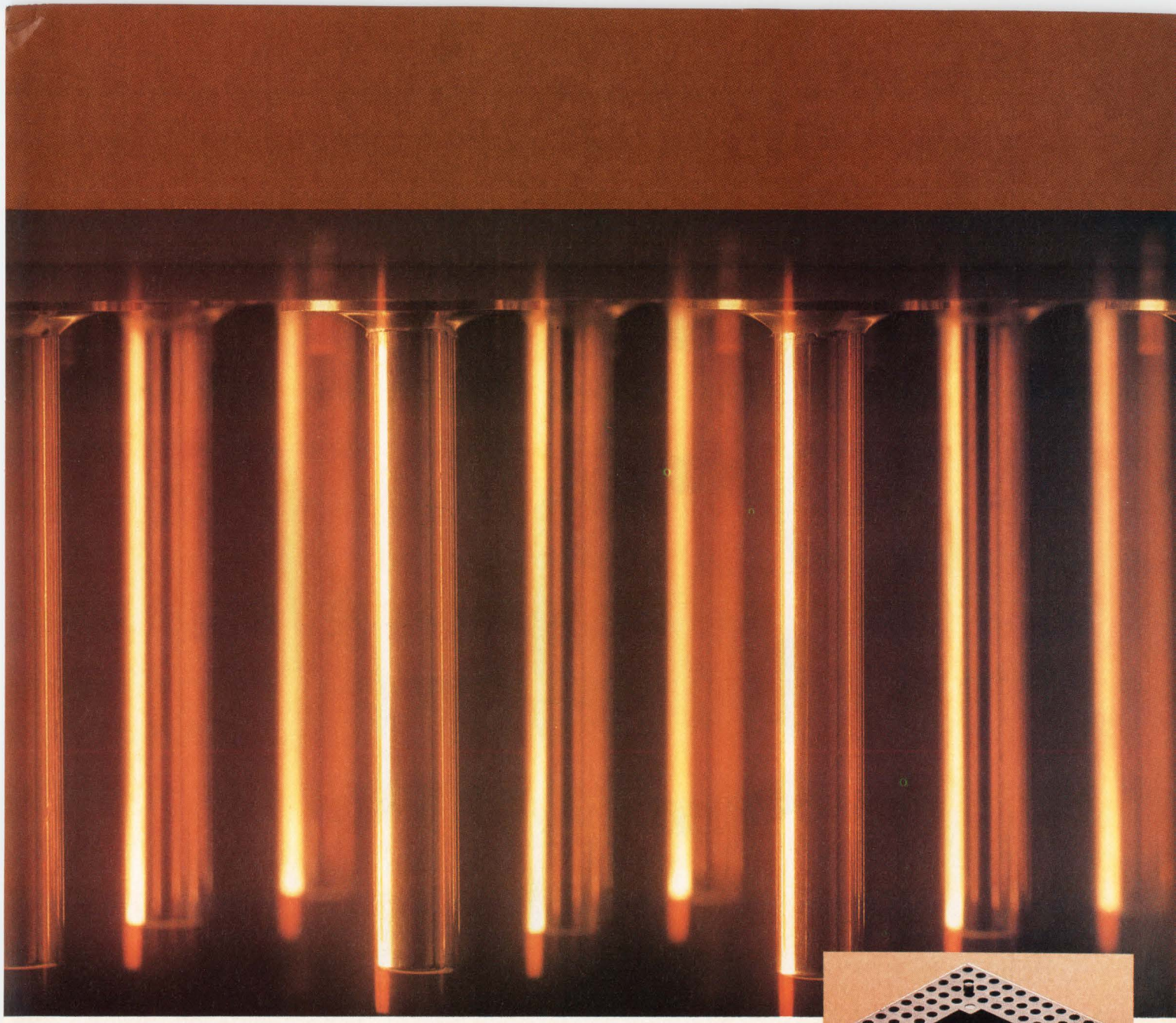
## DEPARTMENTS

# *Helping production cope with the pressures of high pincount packages.*



# *THIS IS AMP TODAY.*

*J. B. Cullinane, "A User's Evaluation of Pin Grid Array Sockets", *Connection Technology*, June 1990.



As PGA pincounts go up, so do the insertion/withdrawal forces required to socket them. When counts reach about 121, conventional socket contacts put your total insertion force in the 28 to 50 pound range—hardly conducive to efficient manufacturing.

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And our exclusive design provides excellent normal contact force as well—the contacts utilize a long beam geometry, providing ample deflection with no compromise between normal force and insertion/extraction force.

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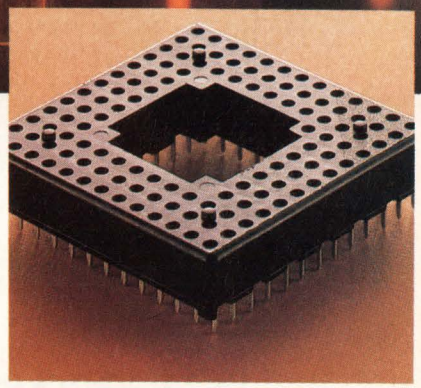

*Dual-beam contact LIF PGA*

AMP

CIRCLE NO. 4

# 57


## 57 MIPS/$12K

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# Numbers speak louder than

# NEWS BRIEFS NEWS BRIEFS NEWS BRIEFS NEWS BRIEF

## Conceptual spreadsheet tool eases VHDL design work

Who says you have to be a programmer to design with VHDL? At the spring meeting this month of the VHDL Users' Group in Cincinnati, OH, Lewis Systems (Irving, TX) will present a paper on a new concept that could take some of the terror out of designing in VHDL, a language that's more than a little imposing to designers who don't happen to be adept at programming. The Lewis Systems tool, called HUM, takes a spreadsheet with a functional description at the conceptual level and generates the proper VHDL constructs and syntax to create VHDL designs and models.

Ed Lewis, manager of the HUM development group, says the tool's users would never have to write VHDL code, although they would most likely want to understand it well enough to debug models in VHDL. "HUM is to behavioral design what schematic capture is to structural design," Lewis says. The HUM user selects behavioral constructs from a menu and uses a mouse to click those constructs onto the screen in the sequence in which the user wants the circuit to behave, he says. Since the HUM spreadsheet can be as wide or as long as desired, there's no limitation on the density of an ASIC that can be designed with the tool. In fact, with data-book information on the AMD 29000, Lewis Systems has used HUM to create a 29000 behavioral model, which was then verified on a hardware modeler.

Lewis says there's a gap between HUM and synthesis tools that don't implement the full IEEE 1076 VHDL standard. So far, small models created with HUM have been synthesized successfully, and Lewis Systems will continue to work with both Synopsys and Racal-Redac to make larger HUM models compatible with the leading-edge synthesis tools. *—Barbara Tuck*

## Rivals combine forces for software standard

Sun Microsystems (Mountain View, CA) and Hewlett-Packard (San Jose, CA) have teamed up to develop next-generation, object-oriented distributed computing standards. Sun and HP are taking several steps toward creating a common software environment that will be available through licensing. First, the two companies have submitted a jointly developed object management specification as a proposed standard to the Object Management Group, a vendor and user consortium responsible for defining object management architectures. Second, Sun and HP will work through standards bodies to promote interoperability between Sun's Open Network Computing environment and HP's Network Computing System. Finally, the companies will make a common distributed application environment for Unix and other systems so that users connected to a network will be able to seamlessly integrate data (for example, a spreadsheet, graphic and block of data) from systems made by different vendors. *—Mike Donlin*

## Intel loses rights to "386"

In a final humiliation in Intel's ongoing squabble with Advanced Micro Devices (AMD) over the rights to manufacture and market an 80386 processor, a federal judge has ruled that Intel does not have exclusive rights to trademark the number "386." AMD (Austin, TX), which had earlier won the right to make and market its version of the 80386, had been deliberating over what to call its chip because of the suit by Intel (Santa Clara, CA). AMD plans to come out with a powerhouse 40-MHz version this month—presumably to be called the Am386—that's expected to challenge the price/performance position of Intel's stripped-down version of the 80486.

AMD apparently will also introduce 16-, 20- and 25-MHz DX versions of the chip. The company still has some work to do to establish complete confidence in the chip's reliability and compatibility, but the device reportedly has already passed compatibility tests with five manufacturers and is being evaluated by some 20 more.
*—Tom Williams*

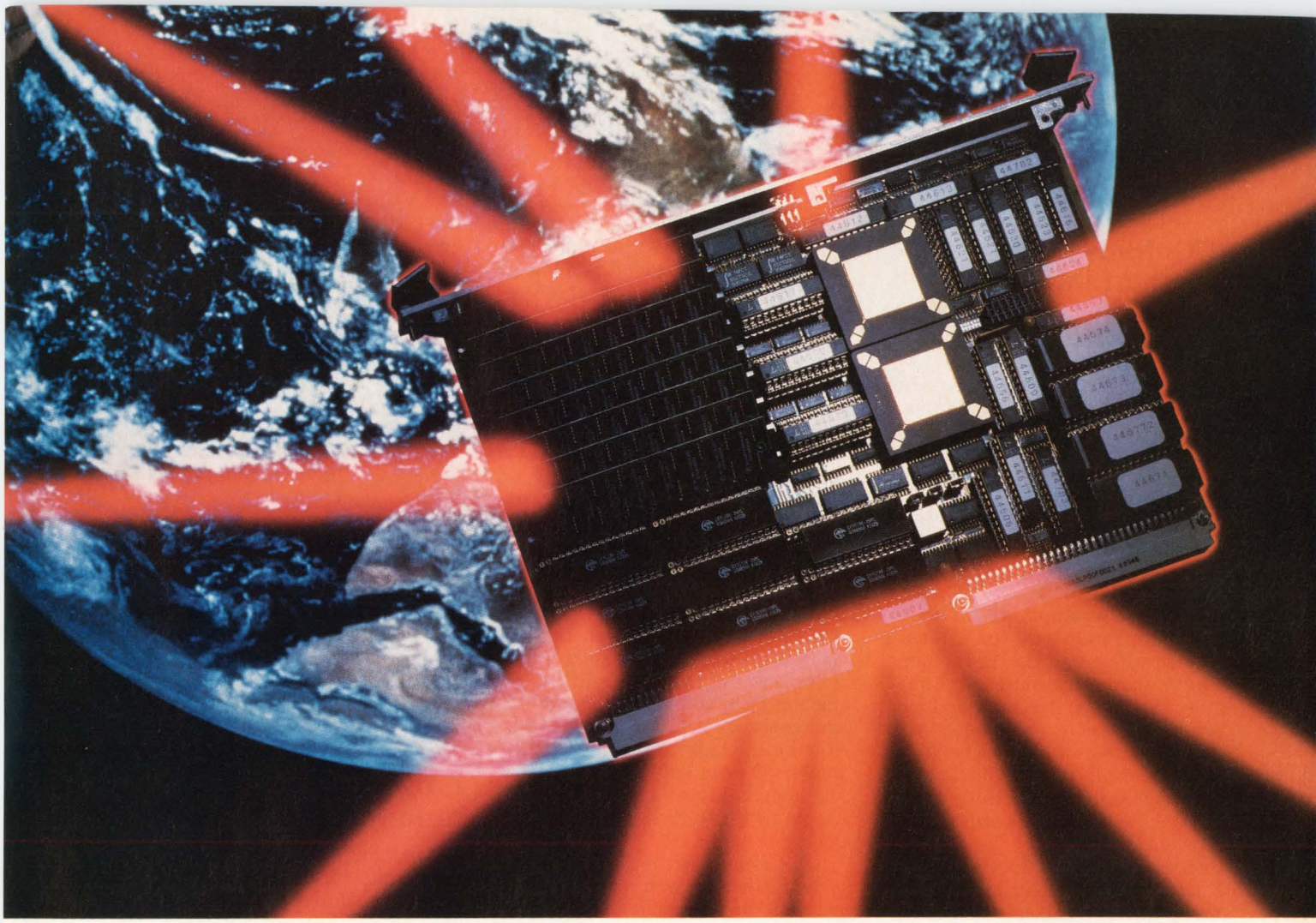
## Mizar out from under?

Reports are surfacing that long-suffering Mizar may be on its way to recovery. Marketing director Tom Kane said the company had recently shown a long-awaited profitable quarter. Kane said Mizar will soon announce some advanced VME products, including a 68040-based CPU card. But the return to profitability may have come at some cost to the company. Former and current Mizar engineers have said that president Joe Ramunni didn't have the company on track; meanwhile, administration sources blamed engineering for the company's poor sales performance.
*—Warren Andrews*

## International group writes Sonet specs

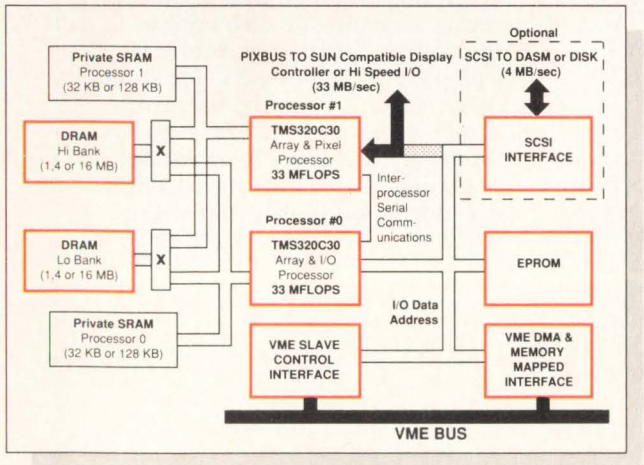
An agreement by a group of international component vendors will provide specifications for the Synchronous Optical Network (Sonet), a set of standards for fiber-optic communications. Spearheaded by AT&T Microelectronics (Holmdel, NJ), the accord allows seamless communication across transmission equipment from different vendors. The coalition also includes BT&D Technologies (London, England) and Fujitsu Microelectronics (Tokyo, Japan). While the agreement ensures compatibility based on pinout, logic interface, optical performance, and power supply considerations, it doesn't mandate the sharing of proprietary technologies. Negotiations for the Sonet standards have been going on for about 18 months.
*—Mike Donlin*

*Continued on page 10*



# For Those Who Like It HOT

## *Announcing the MSP-6C30 66 MFLOP VME Array Processor*




The MSP-6C30 is a 66 MFLOP, floating-point, VME array processor optimized for signal and image processing. High performance is assured through a unique, multi-banked, crossbar memory architecture, and high bandwidth is achieved with multiple, fast, industry standard I/O ports. Also available in a PC-AT version with optional VGA compatible display controller.

### Features

- Under $100/MFLOP (single qty.)
- Dual TI TMS320C30 Processors
- 66 MFLOP, 32 MIPS Peak Rate
- Up to 32 Mbytes On-board Dynamic RAM
- High Speed Private SRAM
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### Applications

- Medical
- Geophysics
- Defense
- Communications
- Digital Signal Processing

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ANALOGIC®
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CIRCLE NO. 6

*Continued from page 8*

## VUGI folds due to lack of interest

VME Users Group International (VUGI) is facing dissolution, according to a recent letter from its chairman, Martin Timmerman. He says he regrets that the computer evolution, the recession and other difficulties have lead to a decrease in group activities and a resultant diminution in revenue generated by commissions and fees. The condition is so severe that "the only option left open to us is to dissolve VUGI."

In a membership note early last fall, Timmerman said the interests of Futurebus+ and the VME community were not necessarily the same. "Futurebus+ is intended for parallel architecture machines with RISC processors where cache is intensively used," he said at the time. "These types of architectures are not likely to be used in an industrial market where people are actually screaming after 68000-based boards. [...] For industrial applications, VMEbus and the complementary buses such as VSB and VXIbus will still go a long way and will easily reach the year 2000. This is one of the fundamental reasons why our organization will not follow VITA, which stands now for VFEA International Trade Association, which tries by all means to push for Futurebus+."

VITA technical director Ray Alderman has strongly hinted that Futurebus+ is the wave of the future, and those who fail to follow may be left behind. But not to fear—it looks as though VUGI will be replaced in Europe by FMUG (Futurebus+ Manufacturers and Users Group), which already boasted its first seminar early in March. *—Warren Andrews*

## Software tools married with logic analyzer

In what may be the first integration of a logic analyzer and software development tools, Tektronix (Beaverton, OR) and Microtec Research (Santa Clara, CA) have announced the availability of LA-Connect, a combined hardware and software system for real-time debugging of embedded systems.

With microprocessors becoming faster and more complex, the costs of developing traditional in-circuit emulation support are becoming a barrier. The problems vendors face today in emulating 32-bit processors have caused serious concerns about the difficulties in working with tomorrow's faster processors. LA-Connect may provide a practical alternative to emulation-type development tools.

The joint product application unites Tektronix's DAS 9200 logic analyzer with Microtec's C, C++ and Pascal cross-compilers and Xray source-level debugger. A software link extracts symbolic information from the object module and converts it to a format readable by the logic analyzer. This helps software engineers correlate the logic analyzer's real-time trace display with their high-level source code.

LA-Connect will initially offer code generation and debug support for the Motorola 680XO processor family and the Intel 960. Versions for the Motorola 88000 and the AMD Am29000 microprocessors will be available soon.

*—Jeffrey Child*

## VLSI on the move in ASIC silicon, software

VLSI Technology (San Jose, CA) has entered into a codevelopment and manufacturing alliance with QuickLogic (Santa Clara, CA), formerly Peer Research. With VLSI manufacturing muscle added to the design knowledge of Peer Research founders, who created the original PAL devices, the soon-to-be-introduced pASICs (programmable ASICs) are likely to create a stir in the already-sizzling FPGA market. Under the agreement, VLSI will manufacture the pASICs for QuickLogic, using process technology jointly developed by the two companies. The VLSI/QuickLogic team claims the pASICS will be the first programmable devices based on logic process technology.

Meanwhile, VLSI made an emphatic move into the ASIC design automation market by launching Compass Design Automation, formerly VLSI Design Technology Business Unit, as a wholly owned subsidiary. "By opening up previously proprietary tools, our customers will have freedom of choice in their selection of CAE environments, hardware platforms and silicon foundries," says Compass president Dieter Mezger. The VLSI framework-based toolset, with support for EDIF (Electronic Data Interchange Format) and VHDL, includes synthesis, built-in self-test compilers, automated test tools, and floorplanning.

*—Barbara Tuck*

## CAD group forms technical subcommittee

Recognizing the need to develop guidelines specifying the digital representation of electrical components, CAD Framework Initiative (Boulder, CO) has formed a new technical group. The Component Information Representation (CIR) subcommittee will be lead full time by Joseph Flanigan, director of IBM's EDA Laboratory and member of CAD Framework Initiative's board of directors. CIR's first project will be to develop a requirements document to determine the scope and focus of the subcommittee's efforts. Proposed initiatives include developing guidelines for library interfaces, component models and electronic data books. The group will continue to gather requirements by inviting companies to scheduled meetings. CIR plans to complete the document by the end of this year. *—Jeffrey Child*

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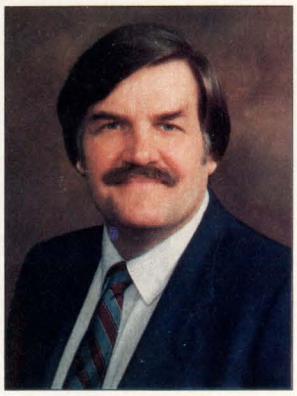
CIRCLE NO. 7

# Some more lessons worth learning

*People, not just hardware, won the war.*



**John C. Miklosz**
**Associate Publisher/**
**Editor-in-Chief**

The success of our high-tech weaponry in the Persian Gulf has shown that we can make quality hardware that works the way it should. But that wasn't all that contributed to our success in the gulf. Our victory was also an organizational one. People—not just hardware—won the war, and all of the elements that make *people* successful were brought into sharp focus.

There was, first of all, purpose. The people in the field knew what the job was and why they were doing it. And while the politicians and public back home may have been less than unanimous in their support of the war, there was unanimity of purpose among those who had to carry out the work.

The "work force" was highly motivated. The value of a voluntary army, navy and air force came through clearly time and time again. The reasons people join the services are as varied as the reasons people take jobs anywhere—opportunity, advancement, security, money, and so on. Whatever the reasons, people are in the services because they chose to be there, and they chose to be there with full knowledge of all the downsides.

Freedom of choice goes hand in hand with motivation. Add unanimity of purpose to that motivation, and the results can become inspirational.

The work force also was well-trained. Say what you will about the military, it spends a lot of time and energy training its people. The military knows that battle is no place for on-the-job training. Preparation for success always precedes success.

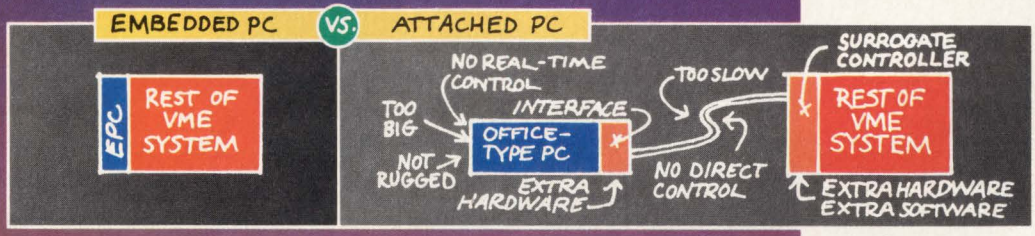
But military training includes more than job-specific areas, and in an organization aiming at high effectiveness in a stressful environment, interpersonal skills and mutual respect are essential. (Our soldiers in Kuwait were saying "Ma'am" as they were helping Kuwaiti women out of ruins.) In the civilian world, the watchword has become "self," but in the military the watchwords are still "courtesy" and "teamwork." The concern is for the group first, and then self.

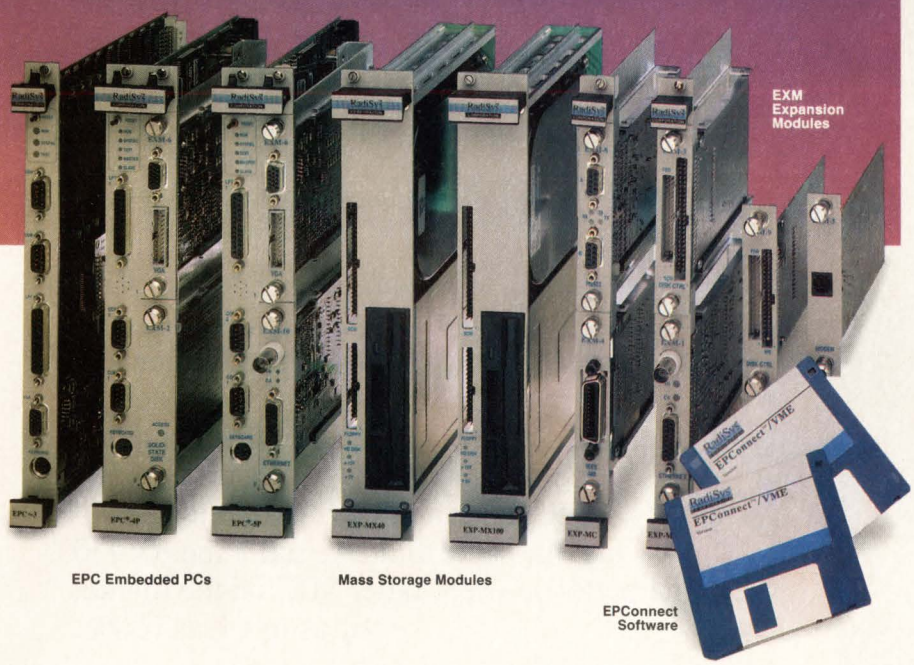
The work force had support. The logistical support, from necessities to conveniences, was there, provided by the services themselves and by the people at home. With adequate logistical support, and with the command that was in place, those on the battle lines knew implicitly that they wouldn't be left to go it alone.

And, finally, the work force had outstanding leadership. Not just command or management—both of which we had—but *leadership.* What's the difference? Hussein commanded but Schwarzkopf led, and that says it all.

The importance of purpose, motivation, training, teamwork, support, and leadership is what the Gulf War should have taught us. If we apply those lessons in the commercial world, success will be just as certain.

# RADISYS GIVES VME THE INSIDE ADVANTAGE

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| CPU | 80386 | 80386SX | 80386 | 80486 |
| CPU Clock | 16 or 20MHz | 16MHz | 25 MHz | 25 or 33 MHz |
| DRAM | 1 or 4 MBytes | 1, 2 or 4 MBytes | 4, 8 or 16MBytes | 4, 8 or 16 MBytes |
| Graphics | EGA (640 x 350) | VGA (800 x 600) | VGA (800 x 600) | VGA (800 x 600) |
| **Mass Storage Modules:** | | | | |
| Hard Disk Capacity | 40 MBytes | | 40, 100 or 200 MBytes | |
| Floppy Drive Size/Cap. | 3.5" / 1.44 MBytes | | 3.5" / 1.44 MBytes | |
| **Expansion Capabilities:** | | | | |
| PC Add-in Cards | Yes | | Yes | |
| EXMbus Expansion | N/A | EXM Expansion Modules: | | |
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| | | EXM-2 Solid State Disk | EXM-6 VGA Graphics | EXM-10 Ethernet |
| | | EXM-3 SCSI/Floppy Ctrl. | EXM-7 RS232 Serial I/O | EXM-11 Timer/Counter |
| | | EXM-4 IEEE 488 | EXM-8 RS422 Serial I/O | EXM-12 Prototyping Card |
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CIRCLE NO. 8

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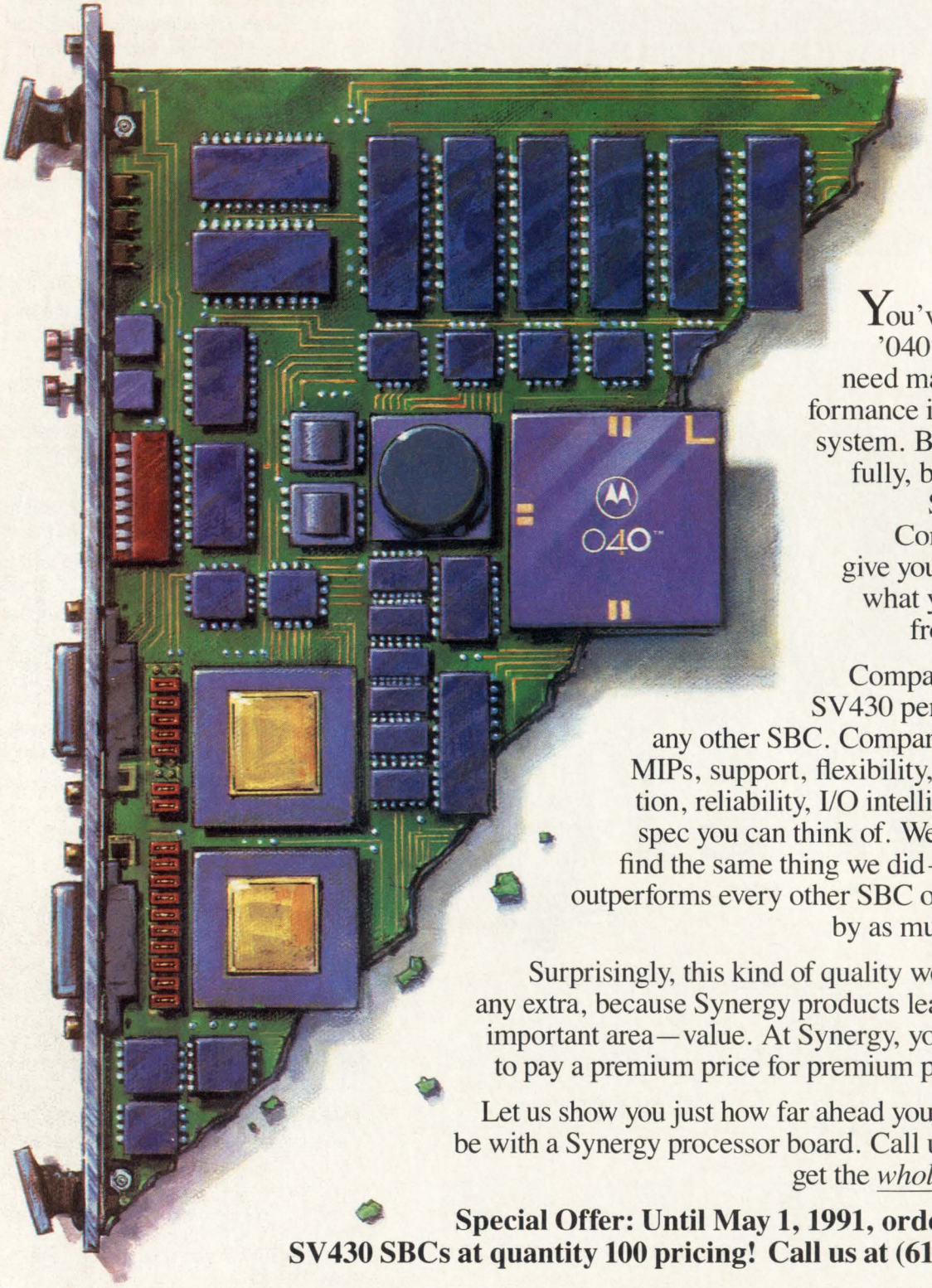


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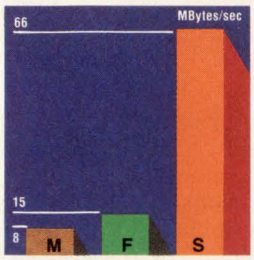
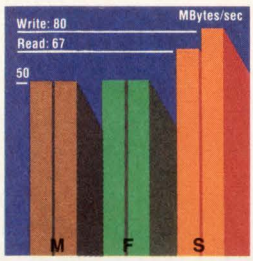


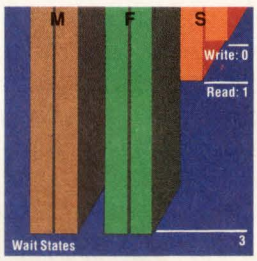

**VME Transfers**

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



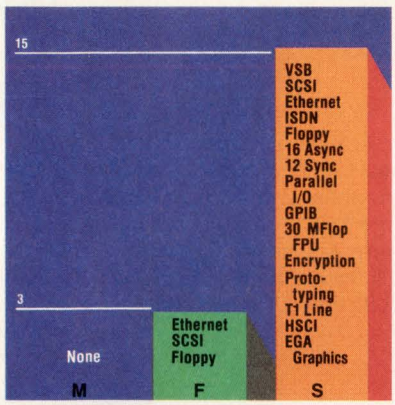

**DRAM Burst Rates**

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.




**DRAM Random Accesses**

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.

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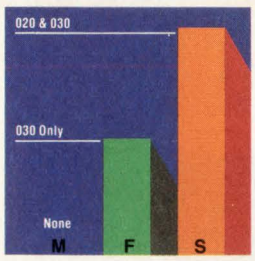
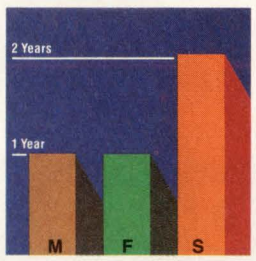



**'020/'030 Compatibility**

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.

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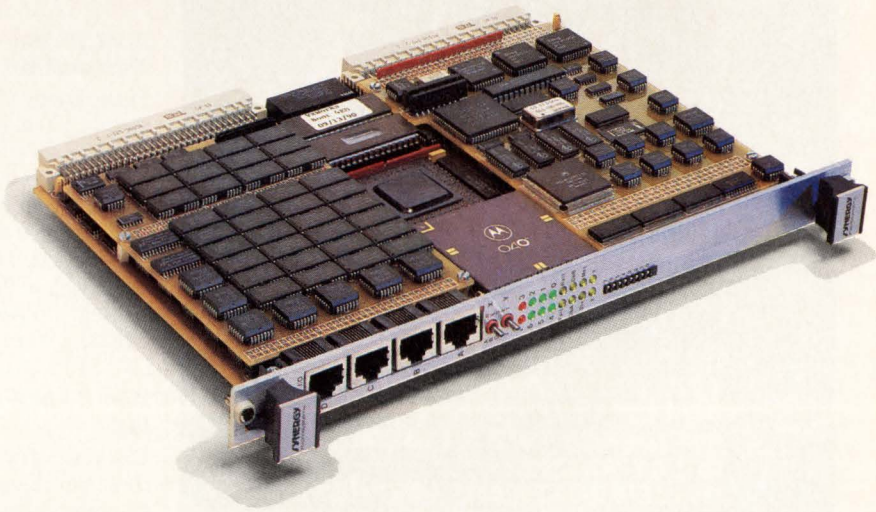
Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.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SYNERGY microsystems

**CIRCLE NO. 9**

# CALENDAR

## CONFERENCES

***April 9-12***
***SMTCON***

Trump Plaza Hotel and Atlantic City Convention Center, Atlantic City, NJ. More than 250 suppliers will demonstrate products at the second annual Surface-Mount Technology Conference and Exposition. The show will offer a comprehensive range of components, equipment, materials, and services used in the design and manufacture of surface-mount and mixed technology products. Information: IC Management, 900 N Franklin St, Suite 700, Chicago, IL 60610, (312) 944-3434. **Circle 366**

***April 16-18***
***Electro/International***

Jacob K. Javits Convention Center, New York, NY. This three-day electronics conference and exhibition will feature more than 500 exhibits and demonstrations; a technical program with tracks including digital systems and software and IC technology; a purchasing conference; and a VMEbus/Futurebus+ seminar. Information: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045-3194, (800) 877-2668. **Circle 367**

***April 22-25***
***NCGA '91***

McCormick Place North, Chicago, IL. The 12th annual conference and exposition sponsored by the National Computer Graphics Association will feature more than 200 exhibitors and a conference program geared toward computer graphics applications, including architecture, engineering, graphic design and publishing, and more. Information: National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031, (703) 698-9600. **Circle 368**

***April 30-May 1***
***The Canadian High Technology Show***

Place Bonaventure, Montreal, Quebec. Nearly 500 exhibitors from Canada, the United States, Europe, and Asia will display products in components and microelectronics, instrumentation, production and packaging equipment, and design automation systems. This electronics exhibition and conference attracts engineers, purchasers, management and marketers from high-tech industry, government and institutions. Information: Connelly Exhibitions, 2487 Kaladar Ave, Suite 214, Ottawa, Ontario K1V 8B9, (613) 731-9850. **Circle 369**

***April 30-May 2***
***EDS***

Las Vegas Hilton Hotel, Las Vegas, NV. The three-day Electronic Distribution Show and Conference will feature exhibits, conferences and seminars on topics including limited distribution lines, market opportunities, and the distributor's role in enabling concurrent engineering. Information: Electronic Industry Show, 222 S Riverside Plaza, Chicago, IL 60606, (312) 648-1140. **Circle 370**

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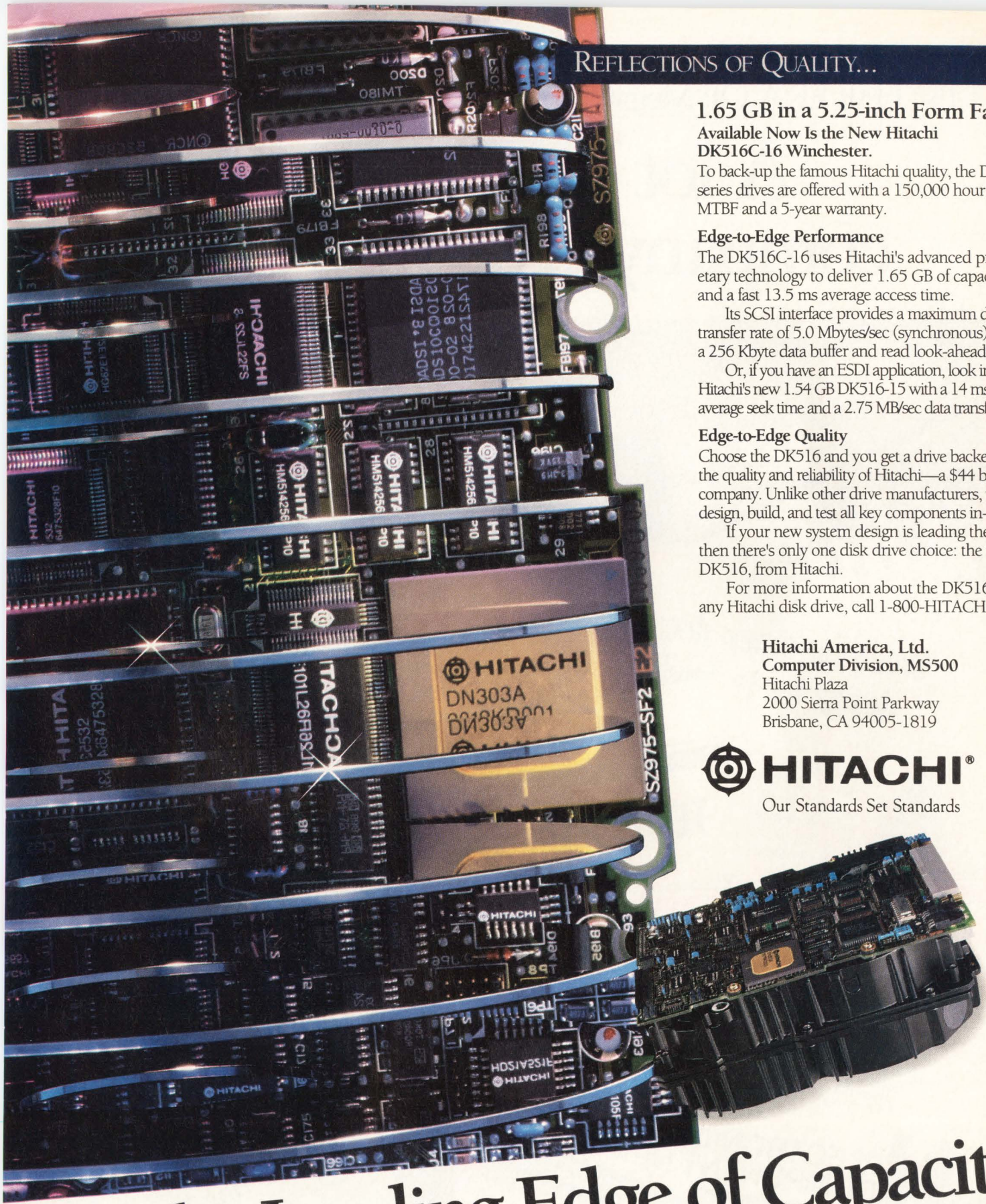


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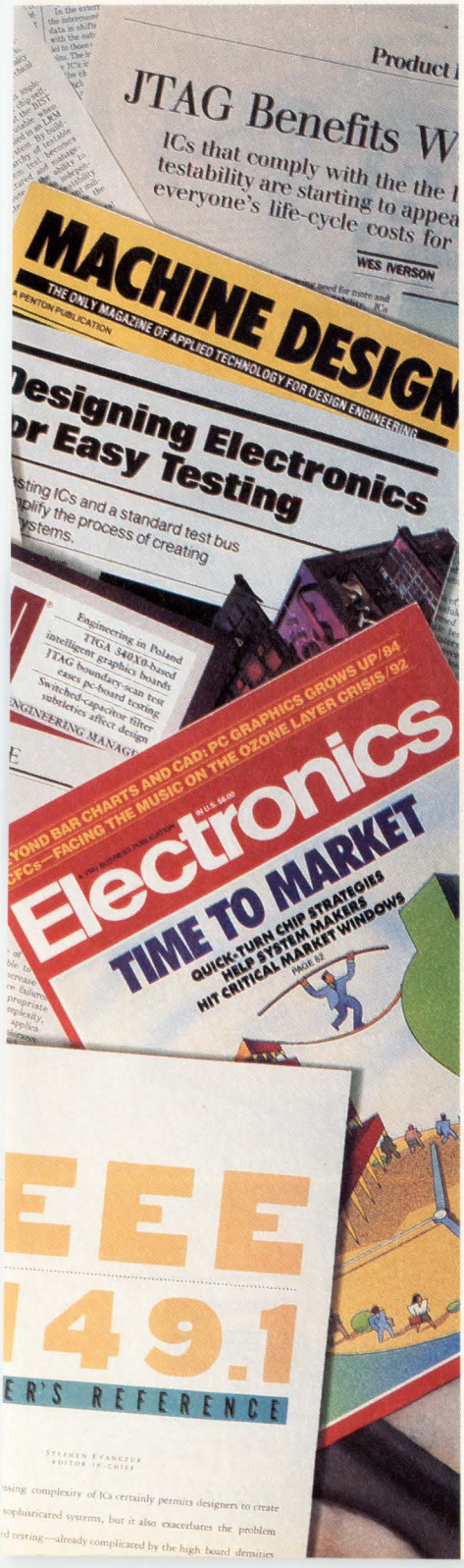
**CIRCLE NO. 15**

IN THE ERA OF MegaChip™ TECHNOLOGIES

# A lot has been said about company is doing a lot about

# testability, but only one it. Texas Instruments.

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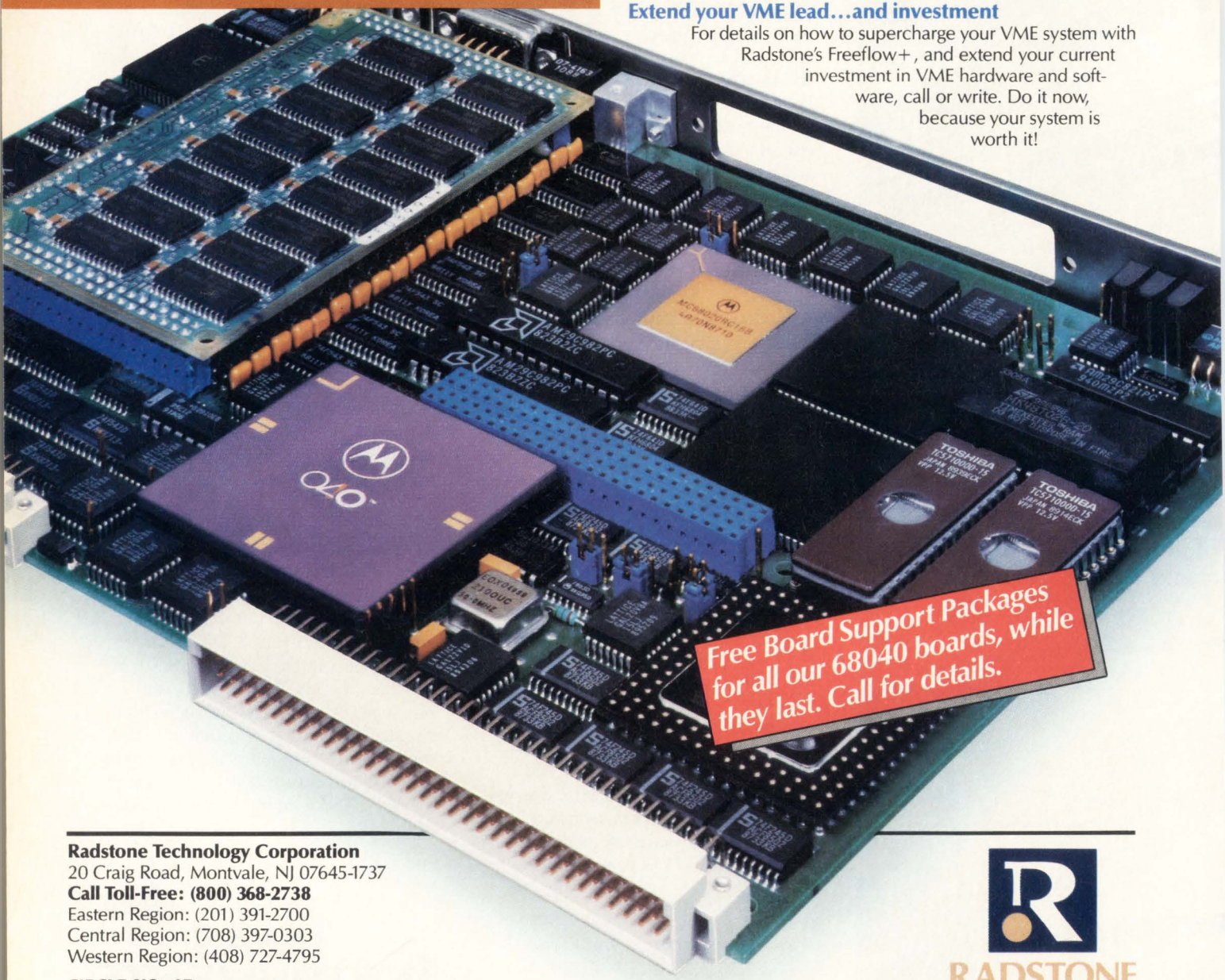


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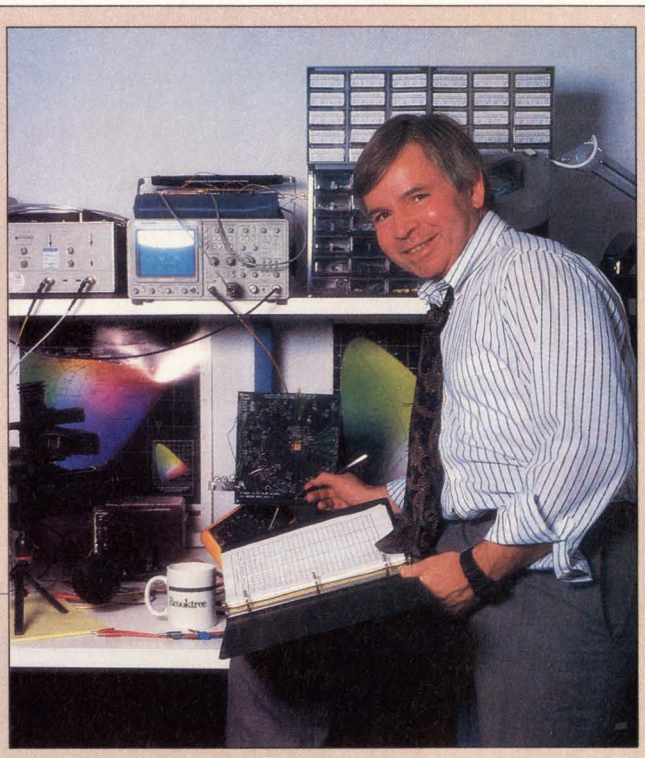
**CIRCLE NO. 17**

RADSTONE
TECHNOLOGY

# John Nelson on: Multimedia



Since its appearance in the late 1980s, the term "multimedia" has been marked by changing definitions and premature product announcements. However, it appears that the '90s may be the decade in which multiple media—graphics, text, audio, and video—are finally consolidated and integrated into a variety of computer-based systems.

Audio has already emerged as an important new data type, with machines such as the Macintosh and the Next computer offering applications including voice mail, high-quality music, and voice annotation of text. Manufacturers of other computers are struggling to find footholds in what's forecasted to be an exploding market in the '90s.

But the key component of multimedia will be full-motion video for applications such as LAN-based video mail, computer-based industrial training systems, and high-quality random-access video editing and production stations—not to mention the eventual merger of home computers and TV. This ability has yet to be fully achieved. While it's relatively easy to display a TV-quality still picture on a computer screen, it's not yet possible to display a high-quality, digitally processible, full-motion video image. The ability to effectively compress vast amounts of data is one of many remaining obstacles.

With the proliferation of "silicon solutions" that allegedly provide computer/video integration capability, designers attempting to incorporate full-motion video into their multimedia systems often have difficulty distinguishing between hype and reality. They're faced with an array of single-chip, multichip, and board-level products from vendors claiming that these products can implement various proprietary and nonproprietary compression algorithms and standards.

Nonproprietary, open standards appear to offer the best hope for designers. The major computer manufacturers insist that any multimedia platform be able to decompress a compressed video stream from any source, just as TIFF or Postscript graphic images can now be handled by most personal computers. The industry is increasingly turning to the standards of three international organizations—the CCITT H.261 group, the Joint Photographic Expert Group (JPEG) and the Moving Picture Expert Group (MPEG). But even with compatible hardware, multimedia system designers still face difficult decisions regarding technical and cost-related problems.

## Silicon will lead

Early graphics systems evolved from the printed circuit board and card-cage level to VLSI solutions that made them cost-effective for desktop machines. But with digitized motion video, silicon is leading rather than following. Massive data storage requirements and the complexity of video data compression algorithms have ruled out board-level solutions. Powerful dedicated VLSI products are required to support motion video with Winchesters, LANs and optical disks. As the market develops, more of these specialized VLSI products will be introduced, further complicating the choices designers have to make.

One important choice confronting designers is image quality. Establishing the image-quality level for a particular multimedia system is largely dependent on the intended application. Video teleconferencing, for example, requires a lower-quality image than a video editing/authoring system does, since most of the information resides in the audio data. Products for the teleconferencing market are therefore designed to display images at lower than VHS quality.

On the other hand, VHS-quality video images aren't adequate for many desktop computer and workstation applications. If you doubt this, sit in front of your color TV at the distance you usually sit in front of your computer screen, and try to imagine interacting with the image over a period of time. Delivering high-quality video to a computer-based multimedia system will be initially expensive because of several factors.

First, video data is real time. Today's PC architectures—particularly Unix- and DOS-based systems with their unpredictable response times—aren't de-

signed to handle real-time data.

Second, computer displays typically operate at different screen refresh rates than video. Multimedia applications need to do more with video data than simply record it to another medium.

Third, the NTSC system (the system used on color TVs in the United States) uses a different resolution rate than computers. Today's workstations and PCs have resolution rates ranging from 640×480 pixels on up, while studio NTSC uses a 720×485-pixel resolution. In addition, with today's computer windowing systems, users expect video to be scaled to fit into arbitrarily sized windows—an expensive proposition.

Fourth, most video sources use an interlaced display format, while most computers generally don't. When interlaced video is stored in a noninterlaced frame buffer, distortion artifacts frequently occur.

Though all these considerations are important, the major barriers to the widespread implementation of motion video on computer systems can be summed up in two words: memory and bandwidth. Video frames must be shrunk small enough for storage, and displayed rapidly enough to achieve the illusion of motion. This becomes clear when you consider still-image manipulation. Most color scanners use 24 bits/pixel—a basic requirement for photographic-quality digital imaging. An 8½×11-in. color scan requires 25 Mbytes—thus, only one 24-bit color image can be stored on a typical 40-Mbyte hard disk. In addition, a fast hard drive can sustain a data transfer rate of only 1 Mbyte/s, requiring 25 s just to move an image on and off the disk. Transmitting a 10-Mbyte file takes about a minute over a fast network such as Ethernet. Transmitting the same size file over a 2,400-baud modem takes over 5 hr.

*Memory and bandwidth are the major barriers to widespread implementation of motion video on computer systems.*

In contrast, full-motion digitized video requires a data rate up to 28 Mbytes/s, and a 1-min segment requires over 1.7 Gbytes of storage. The solution, of course, is image compression.

## Compressing/decompressing video images

Since a sequence of video images contains a great deal of redundancy, compression schemes are designed to retain only that information needed to reconstruct the image at the desired quality.

Image compression techniques have made great strides in the past several years, but semiconductor support is immature. Manufacturers typically advertise their hardware products in terms of the compression ratios. Designers seek ratios high enough to produce data streams compatible with today's storage devices, yet low enough to produce a reasonable-quality image for their particular applications. Trade-offs must often be made. When a high-quality, high-resolution image is compressed at a high ratio to fit onto inexpensive media such as CD-ROMs, it may actually look worse when displayed than an uncompressed, lower-resolution image.

A 640×480-pixel image, for example, requires 10,000,000 pixels/s to sustain full motion. At 2 bytes/pixel, this is 20 Mbytes/s. To compress this down to the level needed for reasonable CD-ROM storage requires a 100:1 compression ratio, and image quality will suffer greatly. However, if the initial image has a resolution of only 320×240 pixels, a data rate of only 5 Mbytes/s is needed.

No matter what compression algorithm is used, moving to a higher compression ratio means that image quality will suffer. Note that video compression ratios are statistical in nature—any ratio quoted is an average. If successive frames don't have a good match—that is, if there's a great deal of motion, panning or zooming—the compression ratio drops drastically for those frames. Consequently, the compressed data stream may have high burst rates. This causes serious problems for the designer, since a buffer can overflow and produce a rapid overload of the system. In addition, this varying data stream complicates synchronizing audio with video.

Another related problem, commonly referred to as the "editing problem," also concerns designers. A video segment compressed at a nominal ratio of 100:1 can include sections compressed at only a 20:1 ratio, and it's possible for an editor of such a segment to choose only the 20:1 sections for the final version. This means that the resultant video won't run on the system. Consequently, designers are being forced to overdesign their systems and include additional algorithms to monitor the buffer, incorporating sets of rules that allow the system to degrade "gracefully" rather than catastrophically under overload conditions.

## Inhibiting design flexibility

Among the best-promoted technical approaches to multimedia today are Intel's DVI (Digital Video Interactive) and Philips-Sony's CDI (Compact Disc Interactive). Both of these multimedia "standards" make use of proprietary image compression technology and offer designers a complete, turnkey multimedia system. Since DVI and CDI approaches may be difficult to add to existing equipment, these systems may not be appropriate for the integration of motion video into today's computers because of their compatibility and image-quality limitations.

Other proprietary algorithms and hardware are available today, but most are targeted specifically at video teleconferencing. The image quality achieved by these systems isn't sufficient for most other computer-oriented multimedia applications.

DVI is Intel's proprietary multimedia technology. It's been driven largely by the desire to achieve full-motion video from a modest data rate. Since it uses an asymmetrical, or unbalanced, algorithm, compression and decompression are handled by different means. Compression is done by high-end, specialized machines. (Initially, Intel envisioned countrywide DVI "service bureaus" to handle compression tasks.) Decompression is handled in real time by chip sets installed in users' desktop machines.

Although DVI was a breakthrough at the time of its announcement, the quality of the video produced isn't high enough for many multimedia applications.

DVI incorporates compression/decompression in a system that combines video, still images, graphics, and text. It fixes all of these technologies in terms of quality, and allows designers little flexibility.

Like many other manufacturers, Intel has seen the shift away from proprietary multimedia technology, and recently announced its support for future standard algorithms, such as JPEG and MPEG algorithms, as well as its own proprietary compression schemes. However, the current DVI chip set doesn't actually implement these other algorithms, leaving that task up to the purchaser.

Another major multimedia system is CDI, promoted jointly by Philips and Sony. This proprietary technology is targeted primarily at the consumer market and offers audio, high-resolution color images, animation, and text on 5¼-in. optical disk media. Although full-motion video capability has been announced, products aren't available. CDI employs a stand-alone player that interfaces to a TV set rather than to a computer. Like DVI, CDI is also a turnkey system that imposes its own quality levels on the designer for each data type handled. CDI defines the frame buffer architecture and how it should be controlled, again leaving little room for design flexibility.

***No matter what compression algorithm is used, moving to a higher compression ratio means that image quality will suffer.***

Despite the abundance of proprietary technology, almost everyone currently involved in multimedia acknowledges that the rapid evolution of the technology will depend on open international standards that define coding standards for data compression and decompression. In the past, standards of this type have emerged largely from industry acceptance and adherence to certain dominant manufacturers' specifications. In the case of both JPEG and MPEG standards, however, the caliber and scope of scientific research performed during standards development have been almost unprecedented.

Both standards committees solicited algorithm recommendations from companies, universities and research laboratories, and selected the best algorithms from those submitted. Although implementation cost was a consideration, the most important factors were image quality and media data rate. Many in the scientific community now feel that the JPEG and MPEG algorithms represent the current state of the art. (Many of the proprietary compression algorithms being touted today were evaluated and rejected by the JPEG and MPEG committees.)

The JPEG standard is aimed primarily at grayscale and color still images. It's solely a compression/decompression standard—it doesn't specify image representation (that is, color space, spatial resolution, color representation, or other image aspects). JPEG is a symmetrical compression scheme, meaning that the same hardware is used to compress and decompress images.

While JPEG deals primarily with still images, some companies have announced JPEG hardware that's fast enough to keep up with motion video rates. But JPEG can't support full-motion video at CD-ROM data rates (1.5 Mbits/s). Also, although JPEG is visually lossless on still images at 30:1 compression ratios, above that level the image quality deteriorates rapidly—and much greater ratios are needed in order to implement high-quality, full-motion video.

Although higher bit rates produce higher quality levels at a given compression ratio, the MPEG standard is targeted at CD-ROM data rates as a minimum, and VHS-level image quality with 100:1 compression ratios. The MPEG standard, unlike JPEG, is an image representation standard that addresses image formats. It also addresses audio compression and techniques for synchronizing the audio signal with the video image.

While MPEG defines a bit stream for both video and audio, it specifies only how the bit stream should be decoded, not how it should be encoded. It's important for designers to realize that the term "MPEG-compatible" doesn't mean anything regarding the actual quality of the image. Since some schemes will do a good job of encoding and others won't, two different silicon solutions, both touted as capable of delivering MPEG images, can produce images at disparate quality levels. The quality of MPEG video should improve over time, as more-sophisticated encoders are developed.

## What should designers look for?

Although the first multimedia-like hardware and products were shipped in 1989 and 1990, and new product announcements are being made regularly, it will be a few years before high-quality motion video images become just another data type. Silicon is available today that implements various JPEG and MPEG building blocks, but nothing yet exists that enables implementation of the MPEG motion estimator. Motion estimation, crucial for obtaining compression ratios close to 100:1 with acceptable picture quality, represents a major cost/performance problem.

It's important for designers to carefully evaluate every aspect—not just the compression ratio—of a multimedia VLSI product before deciding to incorporate it into their systems. Isolated product specifications may look attractive, but when the total picture is considered, the situation can change. Designers should try to answer the following questions:

- What are the source and playback image resolutions?
- Does the compression algorithm introduce any artifacts or distortions that affect image quality?
- What's the picture quality in terms of the signal-to-noise ratio?
- What frame rates will the product support?
- What data rates can be achieved?
- What kind of media will be used to deliver this motion video, and what data rates can that media support?
- Will future storage and communication media accommodate higher data rates and support better-quality images?

*John Nelson is chief engineer of imaging applications at Brooktree (San Diego, CA).*

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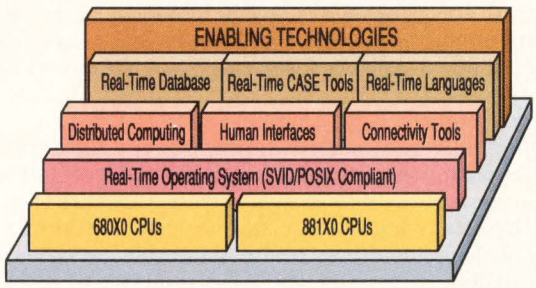


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CIRCLE NO. 18

DESIGN AND DEVELOPMENT TOOLS

# Data management tools tie frameworks to concurrent engineering

*Mike Donlin, Senior Editor*

Though the concept of CAD frameworks is attractive, the claims and counterclaims that surround it are confusing. The very nature of a true framework, namely a software infrastructure that lets multiple tools from multiple vendors run on multiple platforms, opens it to this confusion. Anything that tries to accommodate many architectures and corporate strategies is bound to run into problems.

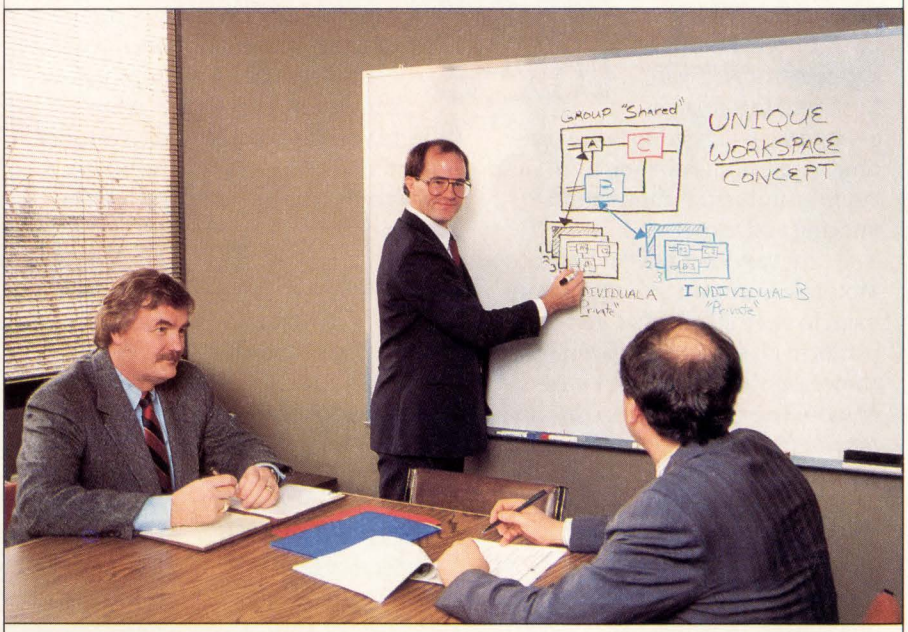
Though a framework doesn't have to be "open" to exist, most everyone agrees that a closed, proprietary system just won't sell because users are leery of getting locked into a single vendor. But for a framework to really live up to expectations, it not only has to be open to multiple tools and platforms, but it also must give users a way to manage information flow as a design is passed from one development phase to the next. With today's shrinking time-to-market windows, no one has the luxury of passing a project through unnecessary iterations because one team worked on the wrong revision level of a design or because parts were chosen that couldn't be used by manufacturing equipment.

## Design management is critical

Design management, therefore, is a key part of any framework, and CAD vendors are constantly enhancing their existing frameworks to improve these management capabilities. Valid Logic Systems (San Jose, CA), for instance, has just unveiled the Design Manager as a component of its ValidFrame design process framework. The Design Manager provides design data management and administrative capabilities with features that support configuration management (including automatic version and release control), project tracking, workgroup organization, and library maintenance.

"We've seen a lot of customer demand for these kinds of management facilities," says Larry Rice, ValidFrame product marketing manager. "Today's complex designs demand that the traditional barriers between design groups be broken down. It's simply not efficient for engineers to work in isolation and hope that everything comes together in the end. So instead of focusing on one particular step in the design process, we're bringing computerized administration to all phases of the design, while managing the interrelationships between them."

The Design Manager uses a commercial object-oriented database management system from Objectivity to store administrative data such as versions, user-defined attributes and configuration information. Valid's decision to use a commercially available database indicates a trend in the EDA industry to incorporate existing tools and technologies into a vendor's environment rather than invent every single part. But selecting Objectivity's product also shows how Valid chose to manage the data along the framework. By separating application-specific data from administrative data, the Design Manager provides unified data management across the design process without the performance trade-offs that Valid says occur in single database approaches.




*"In a large design project that has been partitioned among teams," says Valid Logic Systems' Larry Rice (standing), "a shared departmental workspace lets each team supply the stable version of a design to the other teams for simulation and analysis, while individual engineers can refine their designs in private workspaces."*

## Debating database approaches

The debate over which approach is better, a combination of multiple databases or a single database, is one of the more confusing aspects of framework technology. This critical point—how the unwieldy data in a design environment is represented, addressed and manipulated—is debated among framework vendors. Companies such as Valid maintain that the amount of data a set of tools needs to share is relatively small, so there's no need to burden a system with a huge database. On the other side of the debate are companies such as Mentor Graphics (Wilsonville, OR) and Cadence Design Systems (San Jose, CA) that use a common database architecture.

"The common database approach is based on a common data model or data view," says Jayaram Bhat, marketing director of design framework at Cadence. "But it's not an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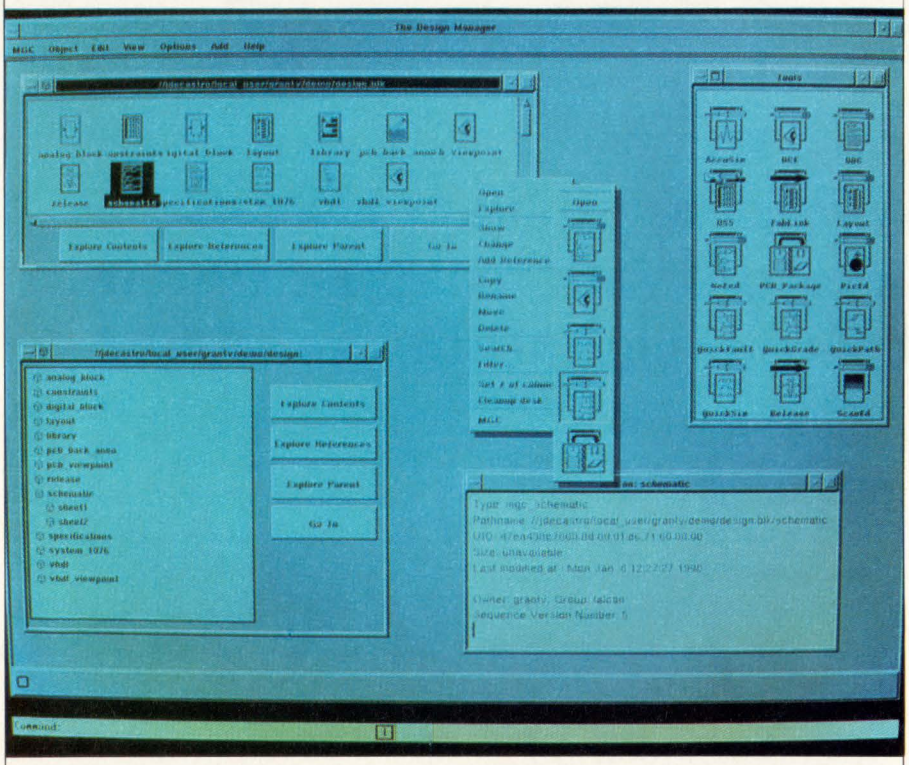
## DESIGN AND DEVELOPMENT TOOLS

unwieldy structure where every time a tool needs some data it has to sift through irrelevant information. A unified data approach defines one data model with different data views, and different tools use these various views. A schematic editor, for example, needs a schematic view, an HDL description needs an HDL view, and so on.

"The advantage of this approach is that you can exchange views in memory while different tools are running. Without the common view, you bring up separate databases for each window, which might result in no correlation between data in different windows."




*With Mentor Graphics' Falcon Framework Design Management Environment, users can call up windows to view the various parts of a complex design. In this object-oriented view of design data, information about a schematic, its associated tools and released version are displayed.*

Proponents of the common database approach accentuate the difference between the database access mechanism (the part that knows how to get the data) and the data that's used (the data model). An IC layout editor, for example, needs to work from a data model that's different from the one that the simulator's using, but that doesn't mean that there's a separate database access mechanism for every tool: It means that there are multiple data models with a common access mechanism. This approach, say its proponents, isn't a clumsy, monolithic structure, but a unified structure with many parts.

### Configuration management

Though the confusion, claims and counterclaims about databases aren't likely to go away soon, just about everyone agrees that for any framework to succeed, it must give users the ability to track the continual changes that take place in the design process. In its Design Manager offering, Valid incorporates a "workspace" concept to administer these changes. Workspaces define each user's environment in terms of the tools, libraries and versions of data appropriate for the user's particular design activities. Each user typically has a private workspace for individual design activity and belongs to one or more shared workspaces where stable libraries or design data can be accessed by various workgroups or entire design teams.

"We think that the workspace concept brings a dynamic approach to configuration management," says Rice. "Prior to this, configuration management has been limited to static approaches such as checkpointing. In a dynamic environment, designs are released by a team when they have a version that's stable enough for other teams to work on. This can be done on a daily or weekly basis as a design progresses, rather than the cumbersome approach that people use in a static environment."

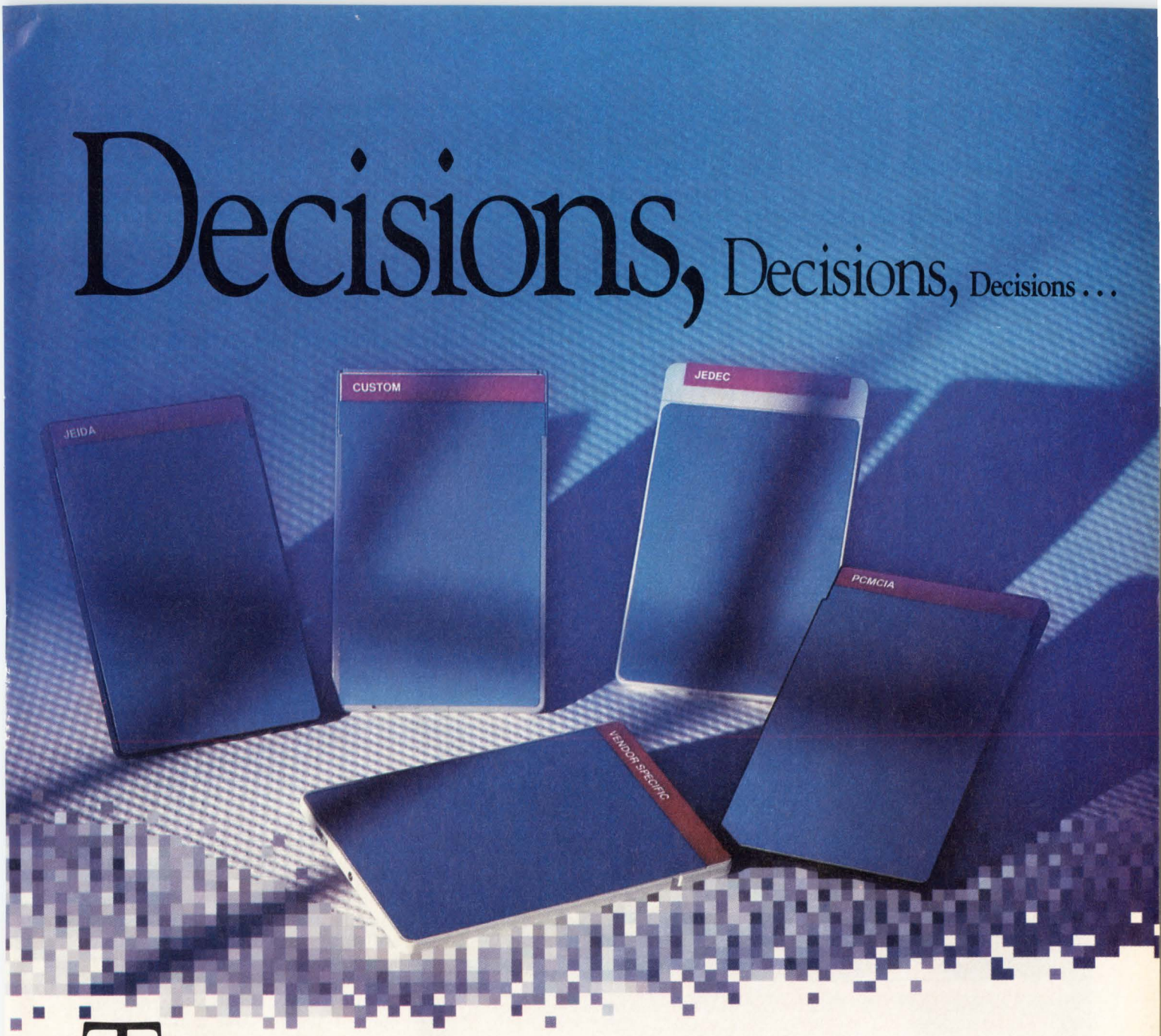
The distinction between dynamic and static configuration management can be a confusing one, especially because other tools, such as Mentor's Falcon Framework Design Management Environment, lay claim to many features similar to Valid's Design Manager. In the Mentor environment, users can partition toolboxes to suit their individual needs. Different toolboxes can contain Mentor tools, third-party tools or site-specific tools. Designers can invoke these tools, work on a version of a design, and then move, copy, release, or archive these designs.

"Obviously the most important thing in a concurrent engineering environment is making sure that everyone is working on the right release of a design," says Bill Stevens, marketing manager at Mentor for the Falcon Framework. "This means not only proper management, but ease of use. When a team releases an update of a design in our system, only those things that have been changed since the last release need to be updated. This is an important feature, especially in large, complex designs."

In spite of claims by other vendors, Valid makes the distinction between a static management system such as design checkpointing and the company's dynamic design flow. "Workspaces provide the means to manage dynamic changes in the state of the design and synchronize a work in progress," says Rice.

"Without the dynamic configuration management provided by workspaces, designers would have to stop work to assemble checkpoints based on predetermined schedules or data release dates, which often go unmet,"

# Decisions, Decisions, Decisions . . .

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he says. "Having to rely on these static updating methods delays work in progress and has a serious impact on the magnitude of changes made to designs. On the other hand, dynamic updating of design data eases the process of incremental change, eliminates an individual designer's concern for data accuracy and shortens the overall design cycle."

### Library management

No matter which type of environment an engineer uses—static or dynamic—the need for updated, accurate parts libraries is an important concern. Without proper library management facilities, designers can operate inside their individual environments and possibly choose parts that are obsolete, not approved by manufacturing or simply overpriced.

Valid cites a traditional lack of enforceable guidelines for library management's shortcomings, as well as a tendency for engineers to circumvent such guidelines when they exist. The Design Manager contains library management facilities that concentrate parts-release authority in the hands of a library administrator who can assign designer access to various approved libraries. Individual designers can use only those libraries that have been released to their shared and private workspaces. Once in a library, designers can determine where a particular part has been incorporated into the designs in their workspaces or which parts cost higher than a certain dollar amount.

Library management tools such as Valid's do more than involve software to help control library information: They affect the philosophy of a company concerning how much authority an engineer has in a design environment. "Without taking the individual customer's needs into consideration, library management will fail," says Ken Salzberg, marketing manager for library management systems at Mentor Graphics. "While it's necessary to have a development library and a released library, we find that individual customers need consulting services to make them aware of the value of library management tools."

In order for frameworks and data management tools to succeed, they must insinuate themselves into a company's design philosophy or face distrust from users who are leery of sacrificing autonomy over their design projects. ■



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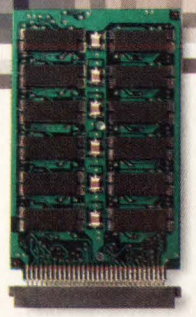

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| | 16MB | ✔ | ✔ | | ✔ | ✔ |
| EEPROM | 8KB - 192KB | ✔ | ✔ | | ✔ | ✔ |
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**CIRCLE NO. 22**

COMPUTERS AND SUBSYSTEMS

# Multibus II looks to secure its future

*Warren Andrews, Senior Editor*

The primary trustees of Multibus II are beginning to review the specification to make sure it will meet customers' expectations and needs in the coming years. The reviewers include Siemens AG, Bull SA, the Intel Industrial Computer Division (formerly the OEM Modules Group) and the Multibus Manufacturers Group.

"We're not making any announcements at this time, nor discussing any definite changes," says Intel's Mike Richmond, product marketing manager of the Industrial Computer Division (Hillsboro, OR). "We simply looked at what would be needed for the future, and proposed some possible solutions to the MMG technical committee." He emphasizes that any recommendations will be carefully reviewed by the MMG technical committee and submitted for a full approval cycle before any commitment is made.

The major new developments, says Richmond, include physical hardware removal and insertion capability ("hot-swap"); extending Multibus II beyond the 21-slot limit; increasing the bus transfer rate; and, in special cases, adding intelligence to the protocol hardware. Though Richmond emphasizes that all these Multibus enhancements are merely ideas that have been discussed, Len Schulwitz, executive director of the MMG (Aloha, OR), hints that development is already under way. "I think we can expect to see prototypes including all the enhancements discussed as soon as the next Buscon," says Schulwitz.

## Hot-swap

The hot-swap concept isn't new—such a capability has been on the wish list of the military and other customers for high-availability, fault-tolerant board-based systems for a long time. But implementing this capability is more difficult than it might at first appear. The difficulty lies not so much in the software as in the hardware.

"The Multibus System Architecture firmware already provides the basic system software required for hot-swap, such as recognizing board ID and system reconfiguration," says Richmond. "What the firmware can't do is manage the transients as a board is plugged in and makes contact with the power and ground connectors."

The proposed solution for this problem requires a separate power connector for each slot, and each power connector would be driven by a power transistor or power FET and controlled by some intelligent system controller. Richmond wouldn't indicate exactly how the connectors would work; however, it's not hard to imagine the standard power connections on the backplane being rerouted such that any existing board could be used, without modification, in the system. In effect, there would be no separate power connector.

The major changes would be in the backplane, where one power device would have to be included per slot, and some kind of intelligent microcontroller installed on the backplane or power-supply board. When the microcontroller sensed that a board was removed, or inserted, it would shut off or turn on power to that slot. The sensing mechanism could be as simple as sensing some resistance on the standard backplane power pins of that slot.

## More slots for Multibus

The second challenge addressed by the Multibus II trustees was extending the backplane beyond the 21 slots allowed for in the specification. Extendibility has always been considered one of the strong suits of Multibus II.

Since the bus is essentially a "network in a box," its logical extension is through a standard network, such as Ethernet, where multiple chassis can be joined to make a larger system. Ethernet, however, is too slow to handle the full message-passing paradigm.

The solution, says Richmond, is to provide "infinite backplane software" and a router that let Multibus II crates communicate over a given media as if all boards were in a single system. The trick is allowing the network and the Multibus transport library to address and pass messages to each board in the system as if all boards were on a single backplane. And, depending on the media, there would be little or no performance degradation.

Another goal of the Multibus II reviewers is to increase the transfer rate of the bus. However, Richmond


*"We simply looked at what would be needed for the future, and proposed some possible solutions to the MMG technical committee," says Mike Richmond, product marketing manager of Intel's Industrial Computer Division. He emphasizes that any recommendations will be carefully reviewed by the committee.*

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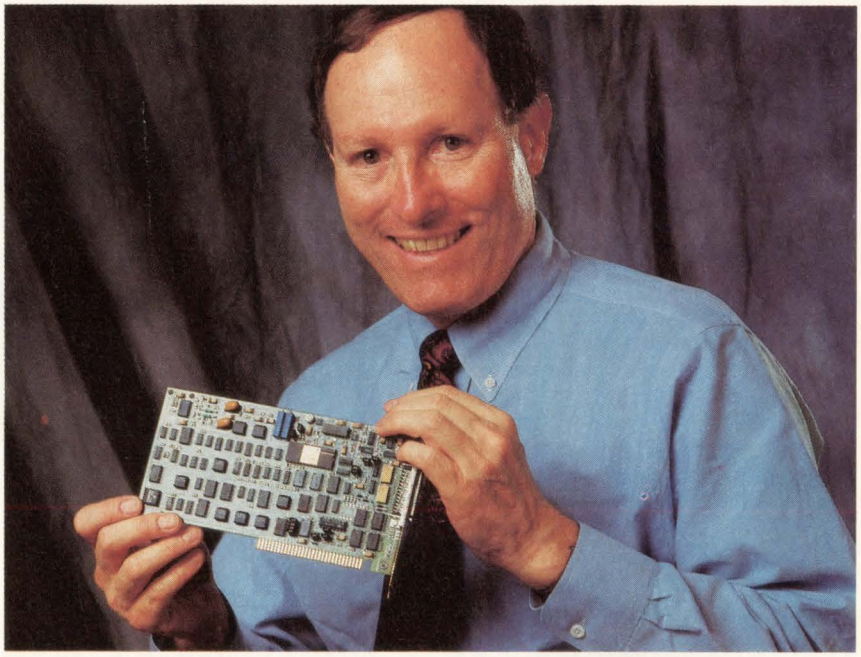

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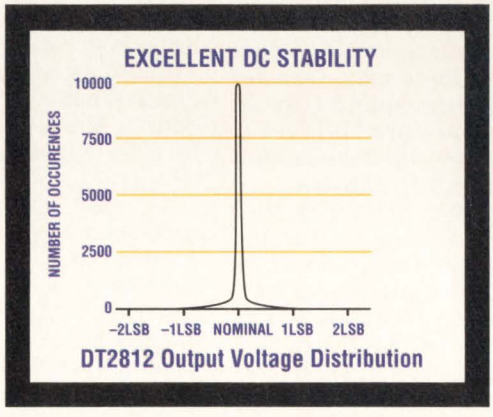


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**CIRCLE NO. 23**

## COMPUTERS AND SUBSYSTEMS

emphasizes that the requirement for more speed across the Multibus II backplane is currently not an issue, and that it's being considered only in anticipation of future requirements. "We haven't yet run into any problems where the current—and real—transfer rate of 40 Mbytes/s across the Multibus II backplane is insufficient to handle any current applications," Richmond says. "But we're obviously participating in an environment where processor and memory speeds are increasing dramatically and will soon call for faster bus transfers.

### Never fast enough

"We constantly hear the comment," says Richmond, "that because Multibus II is a synchronous bus it can't run any faster than 40 Mbytes/s. That just isn't so." In explaining his position on speeding backplane transfers, and on the ultimate proposal, Richmond invokes a bit of common sense mixed with more-conventional backplane logic (see "Comparing bus speeds" at right).

With the combination of a faster Message-Passing Coprocessor (MPC) and the new 200-mA BiCMOS transceivers from Texas Instruments (Dallas, TX), it looks like it will be possible to trim about 31 ns off what Richmond calls the "useful-data-to-useful-data cycle." This translates to a 48-ns max. transfer time, which corresponds to 21 Mtransfers/s. And since Multibus II defines a 32-bit (or 4-byte) bus, that translates to about 84 Mbytes/s.

The MPC, says Schulwitz, has been shrunk to a 1-μm process and is running almost twice as fast as the original devices. As a result, critical clock-to-setup times are cut in half. And, while the objective of doubling the bus speed itself to 20 MHz is certainly achievable, a totally straightforward approach may not be practical. It may, says Schulwitz, call for some kind of radial-clock distribution scheme or some combination of approaches that could result in adjusting the clock rate to the number of slots in the system.

In addition to the TI driver approach, other alternatives are being explored, including one using the ABT245 from Philips-Signetics (Sunnyvale, CA), which is simply a faster pin-compatible replacement

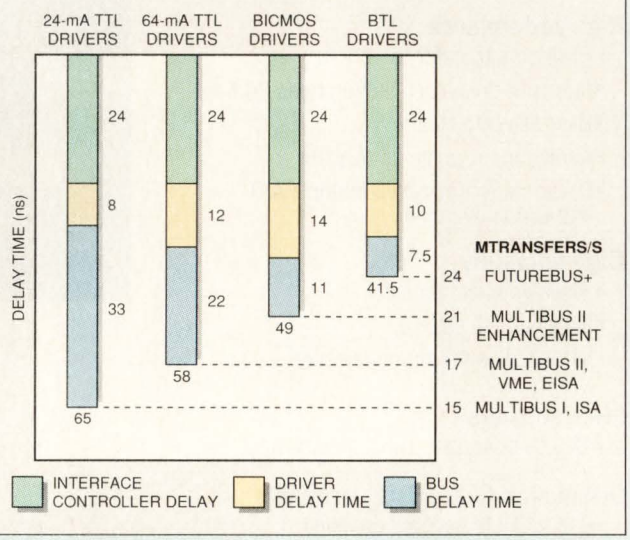
### Comparing bus speeds

Without going through the mathematics of transceiver threshold levels, drive currents and transmission-line effects, let's take a look at the transfer rates of some typical bus approaches. First, the backplane itself is responsible for some significant propagation delays. Standard 24-mA TTL drivers result in a propagation delay of 11 ns, but take at least two full reflections (down and back on a 16-in., 32-bit backplane) before settling enough such that the reflection is below the logic threshold level. The result is a theoretical total transfer time of 33 ns.

Conventional 64-mA TTL logic (used in Multibus II, VME, EISA and other buses) has the same propagation delay but requires only a single reflection, so the theoretical total transfer time is 22 ns. The new 200-mA BiCMOS driver family developed by Texas Instruments (Dallas, TX) also has a propagation delay of 11 ns; however, the additional drive current requires no reflections, and therefore the total propagation delay remains 11 ns. BTL still has the edge, with only a 7.5-ns propagation delay and no reflections, totaling the 7.5 ns.

On either end of the backplane is some kind of transceiver—receiver and transmitter—with its own typical propagation delay. In the case of the 24-mA transceivers, this delay is 4 ns each for both the transmitter and the receiver, totaling 8 ns. The higher-current drivers, in turn, exact their toll, with the 64-mA driver showing delays of 6 and 6 ns, the 200-mA BiCMOS driver yet higher with 7 and 7 ns, and the BTL dropping back down to 5 ns each for transmit and receive.

#### DELAYS AND TRANSFER RATES

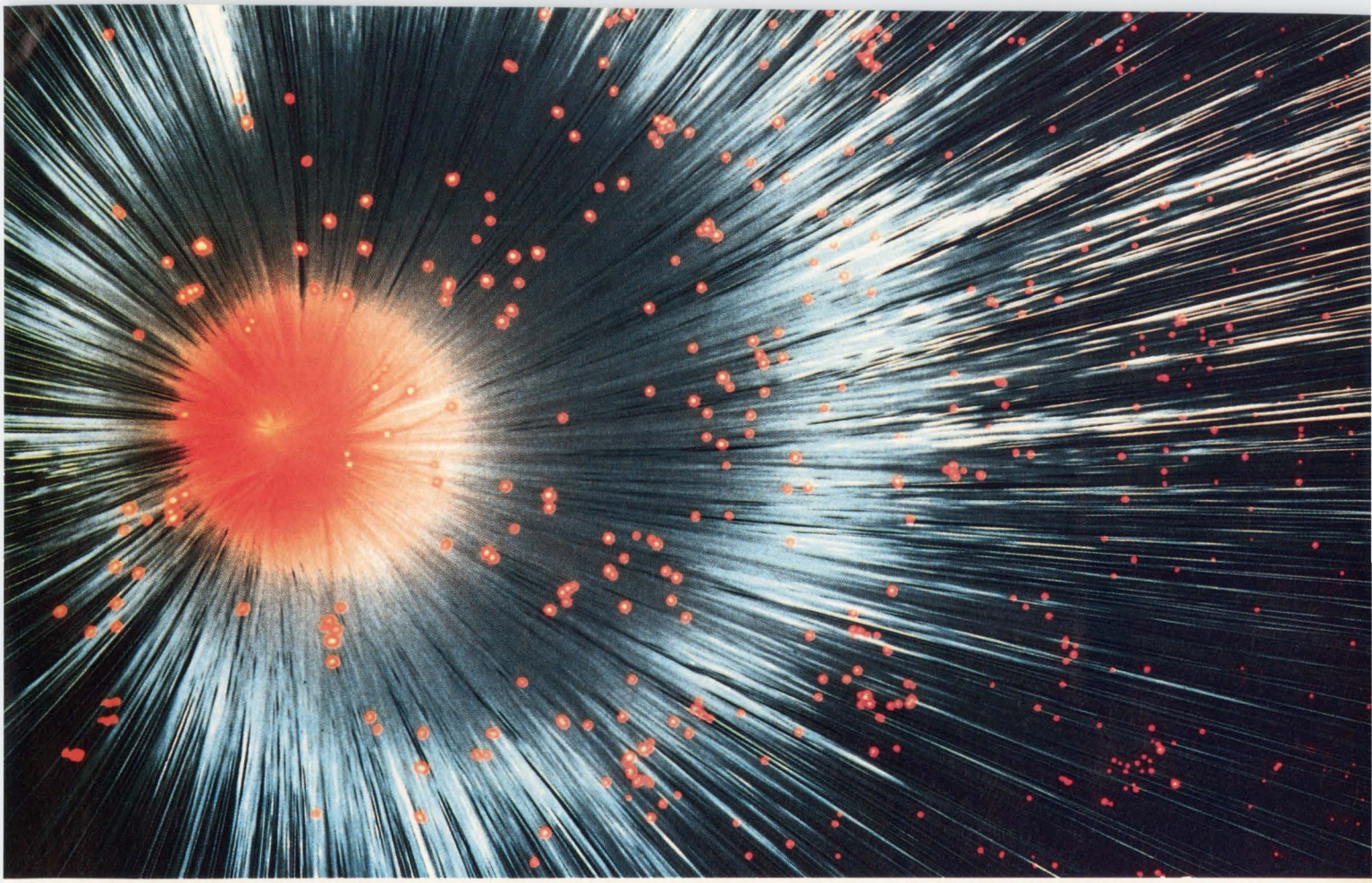



***The maximum transfer rates for standard buses are limited by the delays of their backplanes, transmitter/receiver drivers, and message processors. The bus-dependent delays are illustrated along with their resulting transfer rates. A delay time of a state-of-the-art Message-Passing Coprocessor is assumed for all buses.***

But there's yet another layer before any useful work can be done, and that's the bus interface silicon. Depending on the particular process, interface architecture and implementation, transmit/receive delays can vary. For the sake of argument, let's use the Intel Message-Passing Coprocessor as a benchmark. Current-generation parts guarantee a 25-ns transmit delay and a 29-ns receive delay. But let's discard that and look at the next generation, predicted to have a 13-ns transmit delay and an 11-ns receive delay. And let's apply the same delays for all bus categories discussed.

Yes, BTL technology comes out ahead, but not by as much as first impressions may lead one to believe. Total delays for the BTL system—backplane, transceiver and interface silicon—add up to 41.5 ns, which corresponds to an optimal possible transfer rate of 24 Mtransfers/s. An Intel proposal to improve Multibus II through the use of the TI transceivers comes in a close second, with a total delay of 49 ns, or 21 Mtransfers/s.

**Mike Richmond,** BSCS, product marketing manager, Intel



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**CIRCLE NO. 24**

## COMPUTERS AND SUBSYSTEMS

for the more-conventional Fast logic used, the 74F245.

### More transport intelligence

Attention has also been focused on the conditions that can cause Multibus II systems to get bogged down, especially the case when all cards want to talk to a single module. In a conventional system, the MPC of the target card gets saturated, slowing the system down.

In response to this particular situation, the technical development team came up with what they call a Transport Processor Module (TPM), which is based on Intel's high-performance RISC processor, the i960. The TPM greatly reduces the amount of overhead a CPU will experience while sending and receiving messages. Using the i960CA will reduce component count in the bus interface because this processor incorporates the DMA controller and 8751 interconnect microcontroller. Schulwitz reports that in one test, processors were generating about 4 Mbytes/s of bus traffic per send/receive pair. CPU utilization was about 50 percent when the host programs transported directly, compared to 9 percent when the TPM was used.

***"I think we'll see prototypes that have these enhancements at the next Buscon."***

*—Len Schulwitz, Multibus Manufacturers Group*

■■■

The enhancements to Multibus II will certainly keep the bus in the current generation, but they aren't likely to shift demand from VME in the immediate future. VME, it must be remembered, includes VME64, which allows transfer rates approaching 70+ Mbytes/s. Furthermore, other advanced features of Multibus—such as auto configuration, board and vendor ID—haven't swayed VME advocates in significant numbers. It's therefore unlikely that hot-swap and extended-chassis capabilities will attract more users, outside of those designing for applications that require such features. ■

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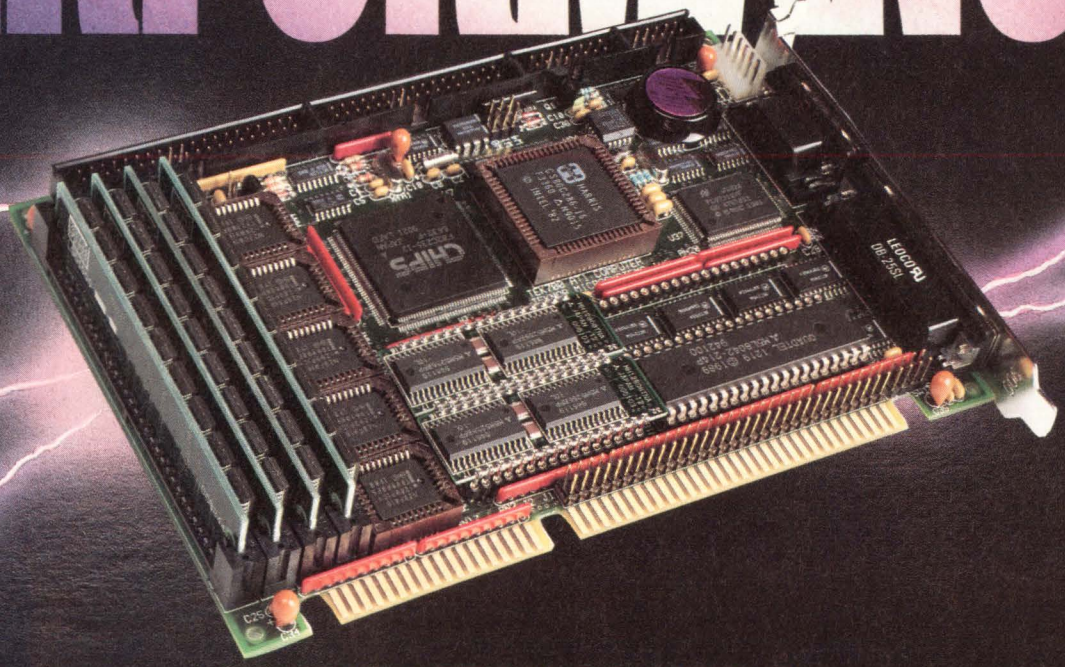

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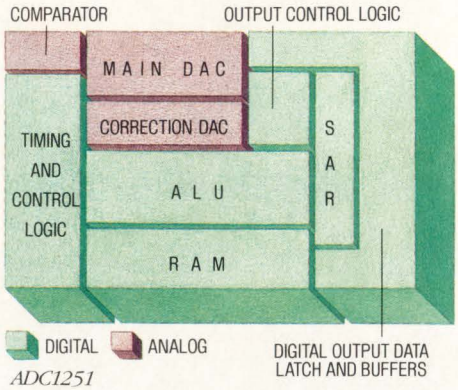

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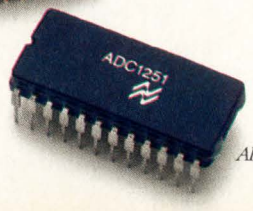

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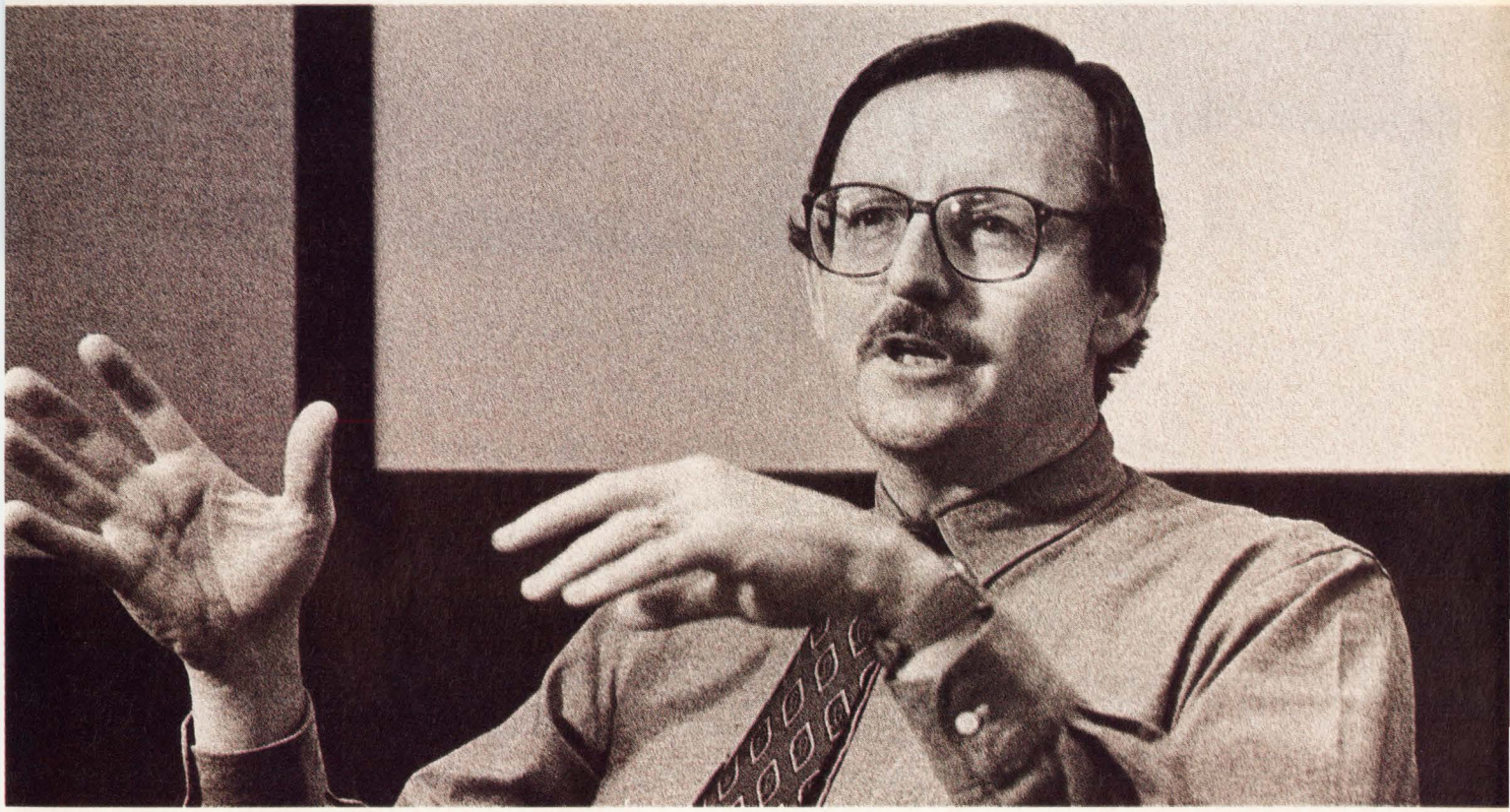

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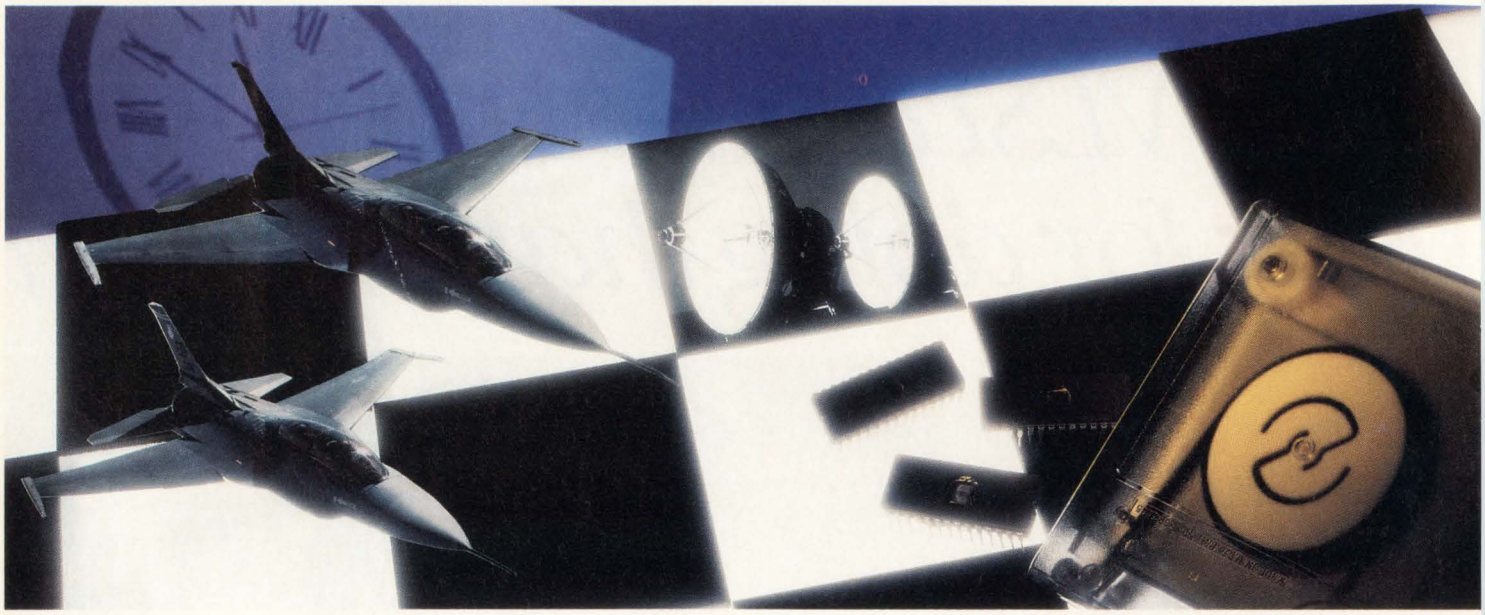

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**CIRCLE NO. 28**

SOFTWARE

# Trusted Unix version points way to secure embedded systems

*Tom Williams, Senior Editor*

The ability of computer systems to protect sensitive information has long been recognized as an important consideration in government and business, but protecting critical programs and data from unauthorized access in embedded and real-time systems is becoming an increasing concern as well. In addition, there's often the need to control access to information in the development environment, especially when "need to know" restrictions must be put in place. Trusted computing environments allow such secure partitioning among users with different access privileges on the same system, as well as—eventually—secure partitioning among components and code in embedded systems.

In a development that may herald the wider availability of secure computer systems for development environments as well as embedded control, Trusted Information Systems (Glenwood, MD) recently introduced the first operating system for an Intel-based personal computer to be certified by the National Computer Security Center to the B2 level of trusted computer systems. B2 is a hierarchy indicating confidence in the system's ability to enforce access to information at different classification levels. The confidence levels range—lowest to highest—from D, C1, C2, B1, B2, B3 to A1. The product is called Trusted Xenix and is a version of the Microsoft Xenix flavor of Unix that has been engineered to meet the government requirements.

## Secure computing

The government specifications define what is required for a trusted computer base (TCB). The TCB focuses primarily on controlling access to information at various classification levels by users with different levels of clearance within a system. Other elements of an overall computer security system are additional methods of user identification (such as retina scanners and smart cards), physical security and encryption. "For example," says Lauren Rudd, Trusted Information's director of marketing, "the files are encrypted, but that's not the key to the security. Even if you could break the encryption, you wouldn't be able to get at the files."

The TCB requirements fall into six major sections. First, there must be an explicit security policy, or set of rules used by the system to govern access between subjects and objects (such as users and user programs and data). Second, access control labels must be associated with objects. In addition, identification and authorization information must be securely maintained. There must be an audit facility so that actions affecting security can be traced to the responsible party.

***"Even if you could break the encryption, you wouldn't be able to get at the files."***

*—Lauren Rudd, Trusted Information Systems*

The final two criteria concern assurance. It must be possible to evaluate the hardware and software mechanisms to assure that they enforce the first four requirements. Finally, the security methods themselves must be protected against tampering.

The B2 class to which Trusted Xenix complies is called structured protection. Access privileges between users and named objects are defined by labels. A user with "Secret" clearance, for example, would have access to all files labeled "Secret," as well as to lower levels of security, but not to "Top Secret."

In addition, categories can be set up within a level to define access more specifically in order to, for example, implement a "need to know" policy. A user cleared for "Secret" and "Secret NATO" would have access to those files, but not to files labeled "Secret Foreign."

## Labels track resources

The system requires that labels be associated with every system resource that is directly or indirectly accessible by subjects. "Subjects" refers mainly to users and programs created by or invoked by users. System resources include storage objects, files, terminals, or ROMs. The ability to label hardware resources as well as ROMs makes it possible to secure parts of an embedded system. One could limit download access to a selected board on a bus, or protect data acquisition from unwanted snooping. ROM code could be limited to access by selected programs or even routines.

Like a user, a resource can have single or multiple levels of security. A given physical terminal could allow access only to a determined level. Just as resources and users are labeled by security level, programs that are written or invoked by a user are marked with that user's label(s). This helps protect against indirect access. In addition, all human-readable output, such as hard-copy printouts, is labeled with the access level of the output on each page.

The audit facility must be able to record the use of identification and authentication methods, use of object in a user's address space (such as file opens or program initiations), deletion of object, and actions by the system's administrators and security officers. This facility also must be secure from tampering.

And, if that isn't enough to put into any PC operating system, there's the requirement that the system be kept as simple as possible so that its compliance with the requirements can be analyzed and verified.

The trusted Xenix system allows five different classes of user in addition to normal users. One person may have more than one of the five roles but can perform only one role for each log-in. ■

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SOFTWARE

# Transputer attracts support for Ada and real-time Unix developers

*Tom Williams, Senior Editor*

As a vehicle for multiprocessor real-time systems, the transputer architecture created by the Inmos division of SGS-Thomson (Colorado Springs, CO) is attracting more software support. The architecture is optimized for efficient operation in multiprocessing systems, and it simplifies the building of multiprocessing systems without limiting the system topologies that can be implemented.

In systems made up of multiple transputers, individual processors run local code in local memory and pass data and other messages among each other via serial links (each transputer has four links). This separation of communications from memory avoids contention problems involving shared global memory among multiple processors. Data written to or read from another processor's memory goes by way of the link. Different interconnect topologies can be combined, and data intended for a processor farther away than an adjacent node simply passes through intervening processors.

## Real-time software

Two approaches to real-time software are just appearing on the transputer, and both take advantage of the processor's ability to operate locally and communicate globally. One approach is the porting of the Ada compilation system by Alsys (Burlington, MA) to the transputer. The Alsys system is being bundled and sold with various hardware modules made by Alta Technology (Sandy, UT). It's also available as an add-on option to the Transputer Education Kit made by Computer Systems Architects (Provo, UT). The kit, intended for training as well as application development, contains an AT board with a transputer, a C cross-compiler and an Occam 2 compiler, along with about 1,500 pages of documentation.

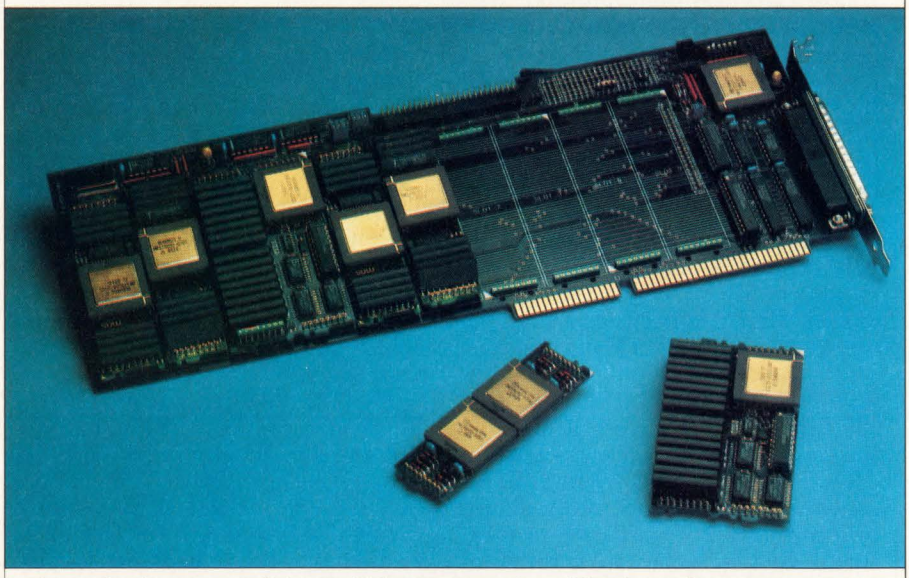
The other approach is the agreement between Inmos and Chorus Systems (Paris, France) to port the Chorus microkernel-based operating system to the next-generation H1 transputer. The Chorus operating system offers a Unix-like application programming interface (API) for multiprocessor embedded systems. According to Will Neuhauser, president of Chorus' U.S. operation (Portland, OR), the initial use of Chorus will be for real-time systems, but Inmos also wants to start building a software base to bring later versions of the transputer into mainstream computing. The Unix compatibility offered by Chorus is a key element in that strategy.

## Operating kernel or system?

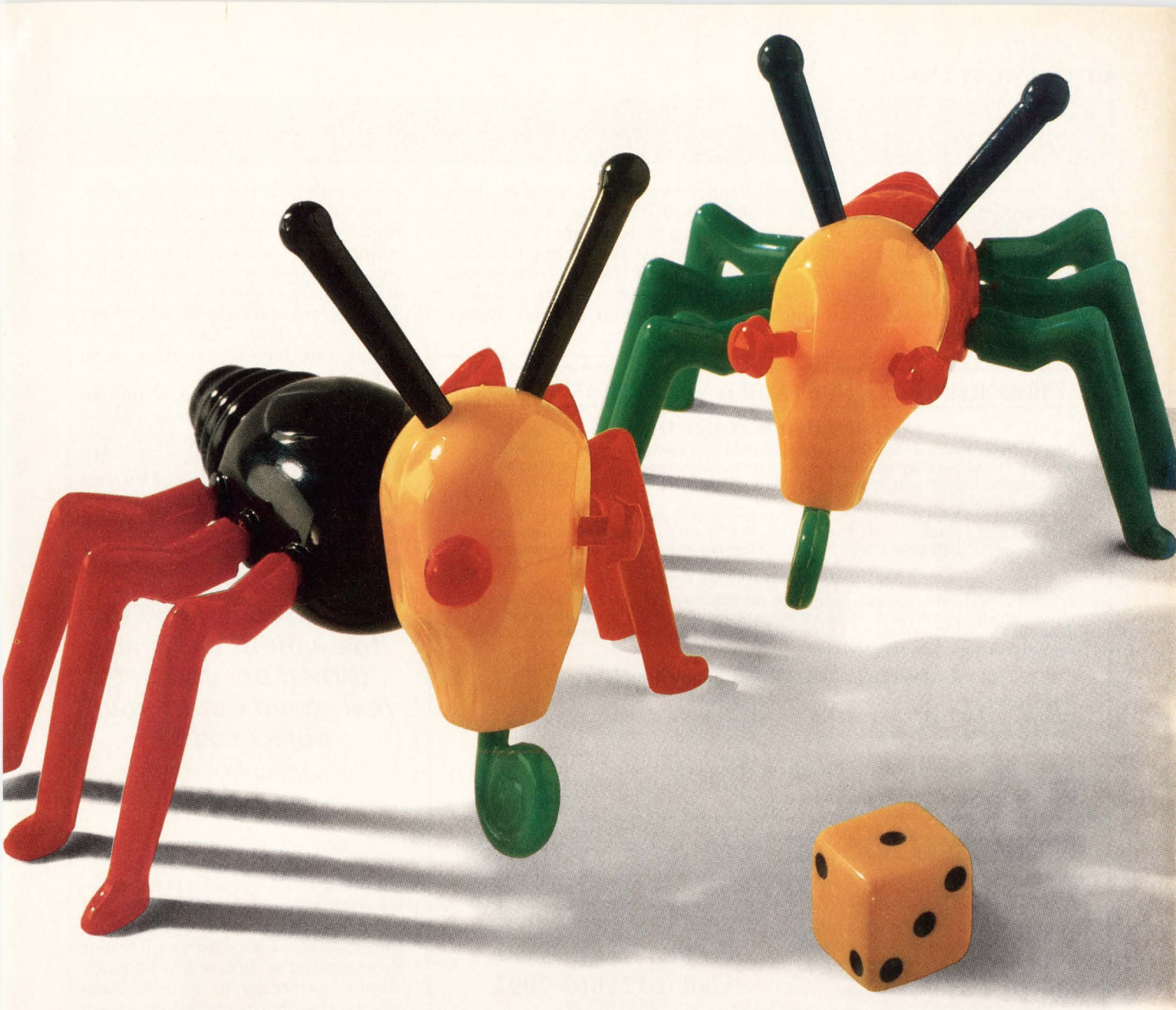
The major difference between the use of the direct Ada compilation system and Chorus on the transputer is that in the latter case, there's an operating system layer present. An embedded application written with the Alsys Ada compilation system tries to eliminate the operating system by absorbing the real-time executive functions into the program proper. As a result, there's no distinct kernel "layer" sitting between the application tasks and the hardware. In the Chorus approach, a copy of the microkernel, process manager and the interprocess communication mechanism resides on each transputer in the system.

In the parallel Ada approach, the programmer can develop code on a single transputer—for example, one plugged into a personal computer or a workstation. But then the programmer has to think about the computing requirements of the application and decide what tasks to assign to which processors. The application can be built with intertask communication taking place between tasks on a single transputer just as if it were being done in any single-processor real-time application. "But when you go to bind the thing into run modules, you can specify which tasks go on which transputers," says Glen Lowry, president of Alta Technology.

Intertask communication between tasks on different transputer nodes still takes place as it was designed in the software, but the hardware mechanism is the serial links between the processors. The advan-



*Alta Technology's Superlink/XL add-in transputer board for the AT bus can serve as an application development platform for multiprocessor transputer applications. Up to 10 modules can be plugged into the board, each module containing two transputers with up to 8 Mbytes of RAM. In addition, I/O modules that connect transputer serial links to RS-232 ports can be plugged into available positions on the board. The Alsys Ada compilation system running on the host personal computer can then be used for application development and debugging.*



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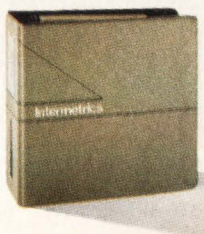


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**CIRCLE NO. 29**

## SOFTWARE

tage from a development point of view, according to Lowry, is that each task can be "designed as a separate, programmable, testable entity that a separate programmer can work on." Determining which tasks or groups of tasks to assign to which transputer node is aided by the use of a profiler that measures the amount of time spent in various tasks. In a real-time application, the programmer would also have to consider how critical various tasks are and whether to dedicate a transputer node to certain critical tasks.

The Alsys compilation system includes several levels of optimization options. High-level optimization includes procedure inlining, which places copies of short called routines at each place in the object code where they are called. This results in larger but faster executing code modules.

Constraint check removal gets rid of Ada checks on variable ranges once those ranges have been verified. "If you choose to compile with the various switches turned on, you get real speed out of it," says Lowry, "and the constructs of Ada allow you to verify all your work, so why slow it down with an operating system?"

***"If you compile with the various switches turned on, you get real speed out of your object code."***

*—Glen Lowry, Alta Technology*

Chorus would no doubt answer, "In order to give it a Unix-compatible environment." And Chorus would probably dispute that a final runtime Ada application produced under its operating system would be much slower. According to Chorus' Neuhauser, the Chorus operating system offers both Unix compatibility and a programming environment that can make use of standard tools that are adapted to the transputer.

### Faster systems

Chorus is porting its operating system to the newest member of the transputer family, the H1. The H1 will be instruction set-compatible with the current T805, but is expected to have a sustained performance rate of about 60 Mips, peaking at 150 Mips. Floating-point performance is expected to be between 10 and 20 MFlops. The links between the new-generation processors are four-wire interfaces that operate at 10 Mbits/s in each direction with a message size of 32 bytes.

The next-generation transputer after the H1 is expected to support

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CIRCLE NO. 31

## SOFTWARE

virtual memory, which, according to Neuhauser, will make implementing Unix easier than on the current version of the H1.

### Ada or Unix?

Unix programs communicate with the system via the Unix-compatible API, which passes microkernel calls to the microkernel—or in this case, microkernels resident on each transputer node. In addition, the presence of the microkernel and communication protocols offers operating system services should a real-time program choose to take advantage of them. But programs such as those written in Ada that have their own real-time services can run without making any Unix or microkernel system calls if the programmer so chooses. Programs written in other languages, such as C, might need the operating system or some other real-time executive features.

The job of allocating hardware resources is expected to be eased somewhat by the Chorus system. Plans now call for it to include a program that would perform load balancing by assigning tasks to processor nodes according to their utilization. Of course, this would entail overhead and might or might not be chosen by programmers with critical real-time requirements. But Neuhauser also notes that Chorus supplies a nucleus simulator that can run on the host development system, allowing the programmer to get his application running and then map it to the target system in stages using the communication protocols.

Running a real-time program under Chorus is similar to loading a device driver. It's a Unix procedure but doesn't necessarily make any Unix system calls. The only difference is that the microkernel remains resident. ■

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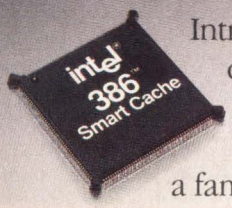


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CIRCLE NO. 34

INTEGRATED CIRCUITS

# High-level synthesis unlocks potential of FPGAs

*Barbara Tuck, Senior Editor*

Field programmable gate arrays (FPGAs) are proving to be not only the hottest technology but also the most unfathomable. Promising close to a magical solution, FPGAs offer low-risk design, rapid turnaround, no NRE (nonrecurring engineering expense) to be amortized over a product's life cycle, and pushbutton migration to ASICs. But the mystery of how to release the full magic of FPGAs and how to make that technology accessible to designers is far from being solved.

Synthesis technology is beyond a doubt the key to unlocking the potential benefits of FPGAs. Nevertheless, the best way to optimize the different FPGA architectures for the most-efficient silicon has yet to be determined. With customers screaming for FPGA synthesis as well as migration paths from programmable logic devices to FPGAs and FPGAs to full ASICs, software and silicon vendors are making initial offerings available and, at the same time, are reexamining strategies in an effort to put all the pieces together.

A trio of silicon vendors recently made FPGA libraries available on the Design Compiler from Synopsys (Mountain View, CA). That move put high-level FPGA synthesis and the ability to migrate to gate arrays in the hands of ASIC designers. In the meantime, an ad hoc committee of FPGA and tool vendors are pushing for a standardized description of netlist components at the macro level by defining a set of parameterized macros that could be interchanged through EDIF (Electronic Data Interchange Format).

## Libraries on Synopsys

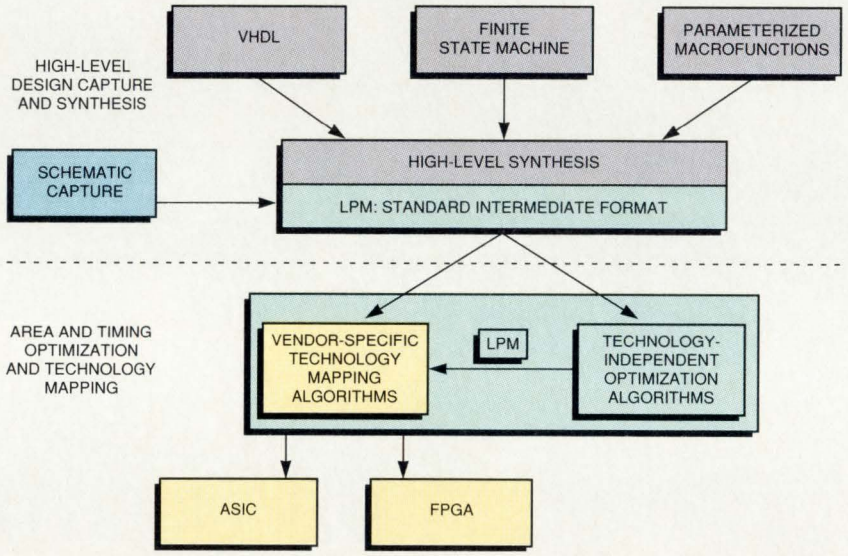
As a first step toward integrating FPGA synthesis into its toolset, Synopsys announced, along with the release of Version 2.0 of its software, that FPGA libraries for the Design Compiler are available from Actel (Sunnyvale, CA), Texas Instruments (Dallas, TX) and AT&T Microelectronics/ASICs (Allentown, PA). Users can enter design descriptions in VHDL or Verilog as well as state tables, equations or netlists; synthesize the design to an Actel, TI or AT&T FPGA; and then use EDIF to transfer the netlist to the FPGA vendor for place and route. Device-specific data has been captured within the library elements by the silicon vendors, according to Jerry Rau, Synopsys marketing manager. The library primitives contain architecture-related information pertaining to performance and area cost functions.

With the FPGA libraries, designers can use the Synopsys tools for technology retargeting, technology translation and hardware emulation. When retargeting to an ASIC design, customers can use the Synopsys Test Compiler test synthesis tool to insert scan structures and to generate test vectors. As for technology translation, a functional description of a netlist is read into the tool, which synthesizes, optimizes and turns out a new implementation that's functionally identical, claims Rau. And where an FPGA is being used as a prototype vehicle in a hardware/software codevelopment effort, designers can build a hardware emulator of the ASIC with FPGAs and then use the emulator to tune the software. The hardware design can be changed by tweaking the FPGA through modifications to the HDL code.

## Actel architecture a plus

Actel is supporting both its ACT 1 and ACT 2 FPGA families with libraries on the Synopsys Design Compiler. The technology libraries will go to beta test this quarter, according to Actel marketing director Andy Haines. The marriage of synthesis and FPGAs is significant to system development, says Haines, who reports that 70 percent of Actel customers also do gate arrays and that

**LPM SYNTHESIS-TO-SILICON DESIGN FLOW**




***A standard for LPM (library of parameterized macros) is one goal of an ad hoc committee of FPGA and tool vendors to ease integration of vendor-specific design implementation software with general-purpose design capture and synthesis tools, as shown in this diagram from committee-member Mentor Graphics. The LPM intermediate format standard, while providing a link to VHDL and synthesis tools, will let designers use their preferred design environment and methodology to create FPGAs and ASICs, says Bob Erickson, AutoLogic engineering manager in Mentor's Design Synthesis Division.***

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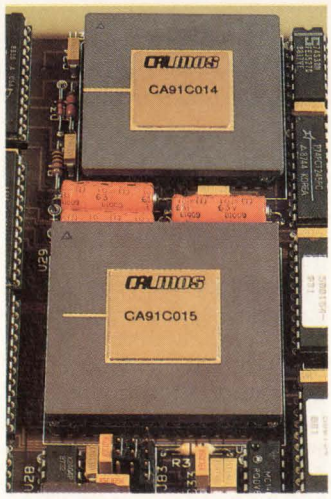


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30 percent use Actel parts for prototypes. For synthesis and optimization, the regularity of Actel's channeled-architecture devices, much closer to gate arrays than other FPGAs, is an advantage, he says. Having been shrunk from 2 μm to 1.2 μm, the ACT 1 devices now toggle at up to 90 MHz, with an 8-bit counter capable of running a system clock speed of 38 MHz.

TI, which manufactures and sells Actel FPGAs, is committed to giving its customers the synthesis capability they're demanding, says FPGA marketing manager Tim Schnettler. In addition to making a TI library available on the Design Compiler, the company recently announced that it would be offering a turnkey FPGA-to-gate array service at its regional technology centers.

The company will also be releasing the ASICPrototyper, based on the PLD and FPGA optimization technology developed by Minc (Colorado Springs, CO) for customers going from ASIC to PLD or FPGA. Another TI/Minc tool, for going from PLD or FPGA to ASIC, will not see the light of day. "As we learn to build FPGAs more economically and more efficiently, we'll approach a point where FPGAs and gate arrays will have more of an economical parity," says TI's Schnettler. "At that point, it will make sense to use FPGAs in the tens of thousands."

### A migration path

AT&T reports that customer demand is strong for a migration path from FPGAs to gate arrays and vice versa. Through an agreement with Xilinx (San Jose, CA), AT&T is in full production of five Xilinx 3000 Logic Cell Arrays and will support those devices on the Synopsys Design Compiler. AT&T has run silicon on the denser Xilinx 4000 devices and expects to ship samples late this quarter. Bill Wiley-Smith, industry veteran and director of programmable products at AT&T, says that synthesis is the only reasonable migration path. "You can do it by just mapping one library to another, but not efficiently, and you can't get a good timing match."

Wiley-Smith says no FPGA on the market today was designed with migration in mind. "Gate arrays don't have programmable elements in the interconnect. If customers really want to get the maximum out of an FPGA when migrating from a gate array, they'll have to resynthesize the logic into an FPGA netlist, reoptimize to take advantage of the specific architecture, redo timing simulations with the FPGA netlist, and compare that timing with the gate array timing." The Synopsys Test Compiler is essential to migration, he says, since the supplier has to test a gate array derived from an FPGA as a custom circuit. AT&T will offer its own stand-alone cross-compiling software sometime this summer.

Though involved in a five-year agreement with Xilinx, AT&T has just begun development of its own family of easily migrated FPGAs. With those FPGAs, its own software capability and third-party tools, Wiley-Smith says AT&T will be in a position to offer a single-package, consistent design methodology that will include pushbutton technology migration.

***"The problem with logic synthesis is that you have to map what you synthesize onto silicon."***

*—Cecil Kaplinsky, Plus Logic*

Xilinx, meanwhile, isn't among the silicon vendors supporting the Synopsys Design Compiler. Lee Farrell, vice-president of marketing, says the company isn't avoiding synthesis and is working with Synopsys. The Xilinx Logic Cell Array, however—with each chip consisting of I/O cells, an array of logic cells with lookup tables, and programmable local and global interconnect—can't be fully optimized with Synopsys synthesis, which is best at optimizing gate array and gate array-like architectures.

### Going for a standard format

The Xilinx FPGA architecture is not the only one that presents a real challenge to synthesis tools. Multi-array devices from Plus Logic are even less like gate arrays than Xilinx FPGAs. To address the difficulties of providing much-needed synthesis tools for device families with unique architectures, a group of silicon and tool vendors, including Xilinx and Plus Logic, has formed an ad hoc committee. The group aims at defining a design methodology that provides optimization in two phases, one technology independent and one architecture specific.

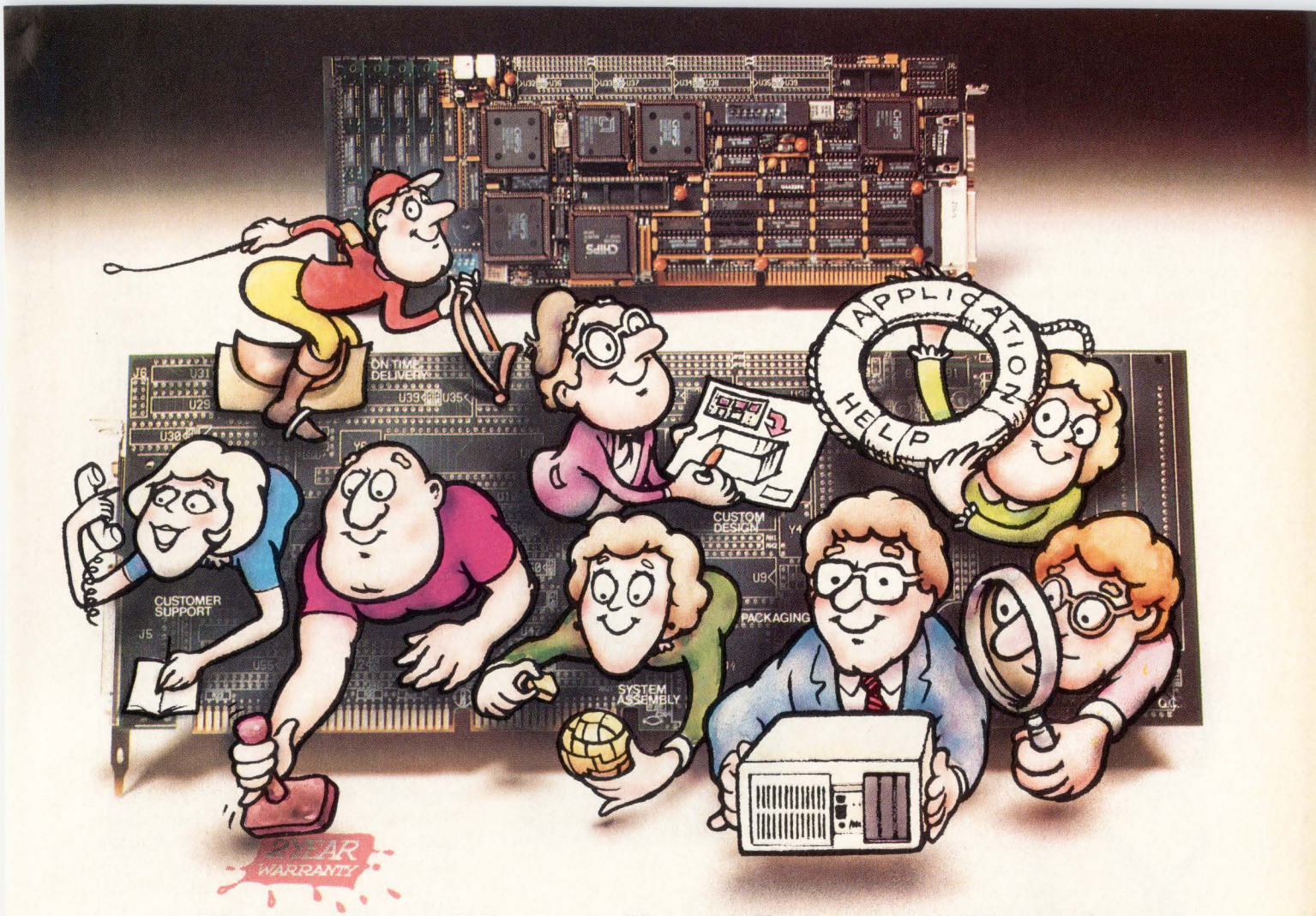
To maximize the benefits of synthesized FPGAs, the committee is working toward a design methodology that will combine technology-independent optimization with architecture-specific optimization. As the first step, the group is writing a standard intermediate format called LPM (library of parameterized macros). Designers will be able to use these parameterized macros, embedded in the EDIF syntax, to describe macro-level netlist components.

The committee's goal is to facilitate the transfer of design data between front-end synthesizers and back-end device-specific optimization and layout tools. Any silicon vendor's fitter—with device-specific algorithms for the most-efficient "fit" of the design to the silicon—that can interface to this standard intermediate format can also accept design data from any synthesis tool with an interface to the format. The committee is also working on a better representation of truth tables and state machines for FPGA synthesis.

"The problem with logic synthesis is that you have to map what you synthesize onto silicon," says Cecil Kaplinsky, vice-president of research and development at Plus Logic (San Jose, CA) and chair of the committee. "No one but the silicon vendor has a detailed knowledge of the silicon, or as much incentive to map efficiently to silicon."

No synthesis tool yet has taken advantage of FPGA architectures. "The way software people like to figure cost functions doesn't correspond to reality," Kaplinsky says. The cost functions of FPGA library elements have to be figured at a subsystem level as a combination of multiple logic functions, taking into account not only the interconnect but also how that subsystem relates to the outside world.

The committee has presented the

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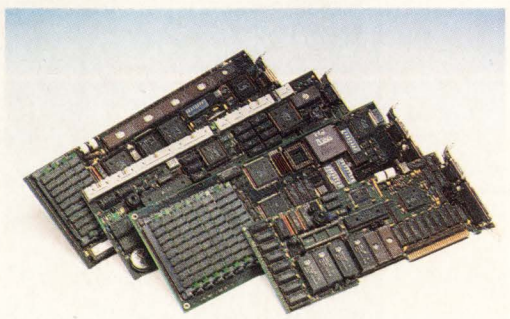

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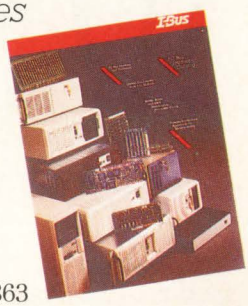


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standard to members for discussion and seeks acknowledgement of support by the end of this month. Kaplinsky expects 90 percent of the vendors to back the standard.

With this new standard in place, Kaplinsky says, designers would use an HDL to enter a design into the synthesis tool of their choice, synthesize the netlist to the standard, feed the standard into the fitter of the target FPGA vendor to be mapped onto silicon, and then, if dissatisfied, feed it to another vendor's fitter without having to resynthesize.

While Synopsys and other vendors are concentrating on the ASIC-to-FPGA and FPGA-to-ASIC market, Data I/O (Redmond, WA) is focusing for the most part on the PLD-to-FPGA market. Data I/O has recently announced Abel-FPGA Design Software, which incorporates enhanced Abel-HDL features and extends to DOS users the FPGA synthesis developed by Exemplar. Abel-FPGA is built around device fitters, via the Open-Abel format, for Xilinx, Actel and Plus Logic FPGAs, as well as Altera Max and AMD Mach devices.

Exemplar's FPGA synthesis is also integrated into toolsets from Viewlogic. And shipments of a standalone Exemplar VHDL FPGA Compiler are under way as are plans for extending that software to target CMOS gate arrays. At the same time, Minc is reportedly working on multichip mapping. Minc's FPGA optimization software has been integrated into many toolsets, including that of Valid Logic Systems.

Though high-level synthesis for FPGAs continues to be elusive, the problems involved, at least, are being clarified. Users are likely to end up with both generic and silicon-specific libraries, as well as front- and back-end optimization with technology-independent and silicon-specific algorithms. The best bet for customers is to choose a synthesis vendor that works closely with silicon vendors. ■

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INTEGRATED CIRCUITS

# Data pump chips away at 9,600 bits/s

*Jeffrey Child, Associate Editor*

Usurping the well-entrenched 2,400-bit/s modem as the standard in data communications won't be a simple task for the 9,600-bit/s V.32 modem. A collection of performance enhancements, especially those addressing data compression, has boosted the capabilities of modems that ply the telephone lines at 2,400 bits/s, increasing their effective throughput to higher levels.

Because these standards let modems exchange data at greater throughput rates, they're satisfying users' demands for speed without the need for a new hardware platform. In fact, many manufacturers of chip sets based on V.22bis, the protocol for 2,400-bit/s communication, are integrating these features into their latest designs. By offering the V.42bis data compression standard along with their 2,400-bit/s V.22bis chip sets, modem manufacturers can provide a total throughput of 9,600 bits/s.

A point to consider, however, is that these benefits will multiply as V.32, the hardware protocol for 9,600 bits/s, becomes the protocol of choice. "A fact that's often overlooked is that the same 4:1 ratio of data compression, as specified by V.42bis, can be applied to a V.32 modem as well," says Bob Rango, product marketing manager at AT&T Microelectronics (Berkeley Heights, NJ). "If you put the same V.42bis on top of a V.32 modem, then you have a 38.4-kbit/s modem."

## Getting in the market

The V.32's penetration into the small-computer market could be its first step toward overtaking V.22bis. "In order for V.32 modems to become as prevalent as V.22bis modems," says Rango, "they must meet the requirements of the desktop and laptop computers. For this to happen, the price, size and speed of V.32 modem chip sets must shrink."

AT&T, the newest entrant into the V.32 modem IC market, recently announced a low-power three-chip V.32 modem data pump. Called DSP16A-V32, the chip set could make V.32 practical for laptop and portable computers. The data pump comprises a 16-bit fixed-point digital signal processor, a linear codec (coder/decoder) and an interface controller. Using the chip set, system designers can implement the data pump function of a V.32 consuming less than 2 in.$^2$ of board space.

The DSP16A-V32 implements V.32 and slower standards in a single DSP—a key element of the chip set. AT&T developed its own compact algorithms for use in the DSP. Because the algorithms are so compact, the DSP has enough ROM on-chip to hold program instructions and sufficient RAM for scratchpad use. No external RAM or ROM is required to support the data pump function.

***"For V.32 modems to become as prevalent as V.22bis modems, they must meet the requirements of desktop and laptop computers."***

*—Bob Rango, AT&T*

In-house software development expertise is essential to modem chip design, Rango says. "Even within these standards there's a lot of room for interpretation. V.32 is a set standard, but the capabilities that you provide during V.32 startup and during steady-state make the modem either hard or easy to implement."

The data pump will also support V.22bis, V.22, V.21, and V.23, and the Bell 212A and 103 standards. AT&T plans to add V.42, V.42bis and Group 3 fax algorithms to the chip set soon. Another built-in feature is an automode capability, which lets the data pump negotiate speeds up to the standard of the originating modem.

The small size, low power consumption and completeness of the AT&T data pump caught the attention of a least one modem manufacturer. Using DSP16A-V32 samples, designers at Vocal Technologies (Santa Clara, CA) implemented the data pump in a portable V.32 modem housed in a 2-in.$^3$ enclosure.

Vocal included an additional 8-bit microcontroller to create a complete V.32 modem. The controller handles the modem's autodialing, error-correction and data-compression functions. Some RAM and ROM chips are included to support those functions. "If you're running V.42bis, you're going to need quite a bit of RAM to run the large block tables that are desirable when using V.42bis," says Fred Hirzel, president of Vocal. "If you're just doing error correction, you can have small external RAM." Also included are the circuit elements needed to get sound into the modem, known as the data access arrangement.

Hirzel notes, however, that RAM and ROM are used only by the 8-bit microcontroller. No additional memory devices are required to support the data pump function.

## Modems to go

Excessive power consumption is another factor that has locked V.32 modems out of the laptop and portable markets. Using its submicron CMOS process, AT&T keeps the data pump's power consumption at 450 mW typical, with a sleep-mode consumption of 50 mW. The low power dissipation and sleep-mode feature give users an added benefit. "Using only a 9-V battery, our modem can wait three days for an incoming call," says Hirzel.

As users have long recognized, higher-speed modems reduce both time and communications charges. This ongoing appetite for speed makes inevitable the day when V.32 replaces V.22bis as the most popular modem standard. To compete in today's more feature-driven modem IC market, however, standards for data compression and error correction will continue to be part of the equation. ■

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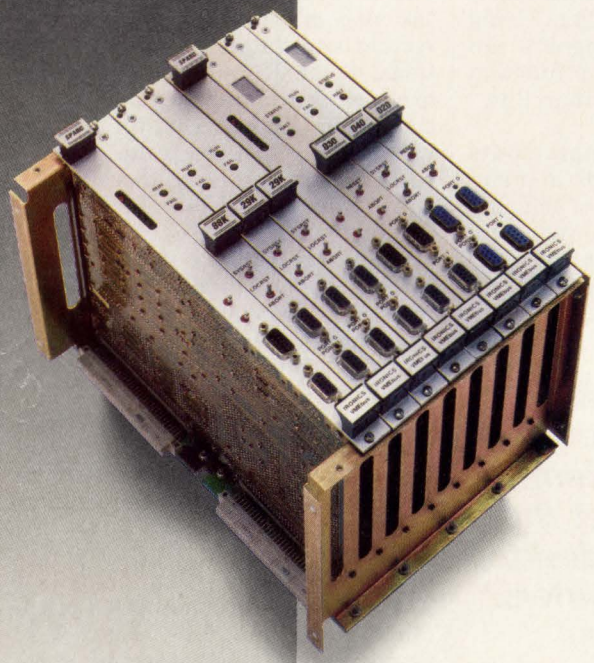

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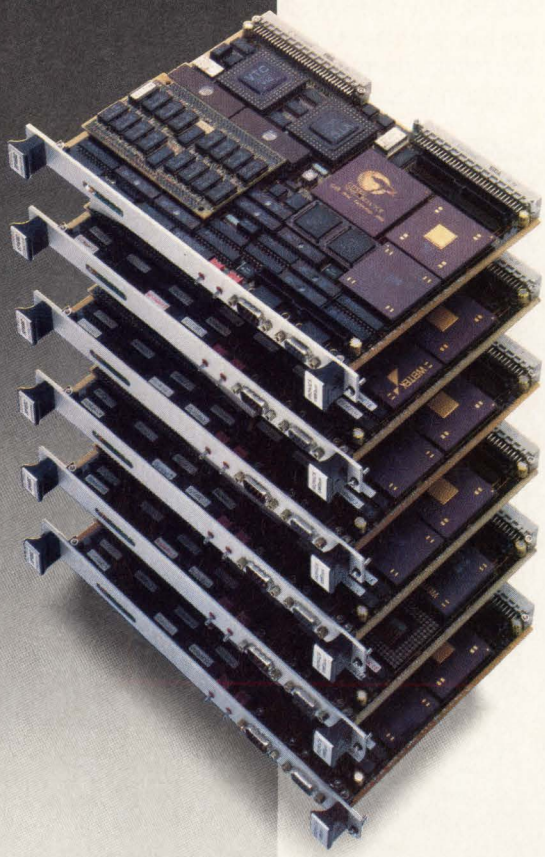

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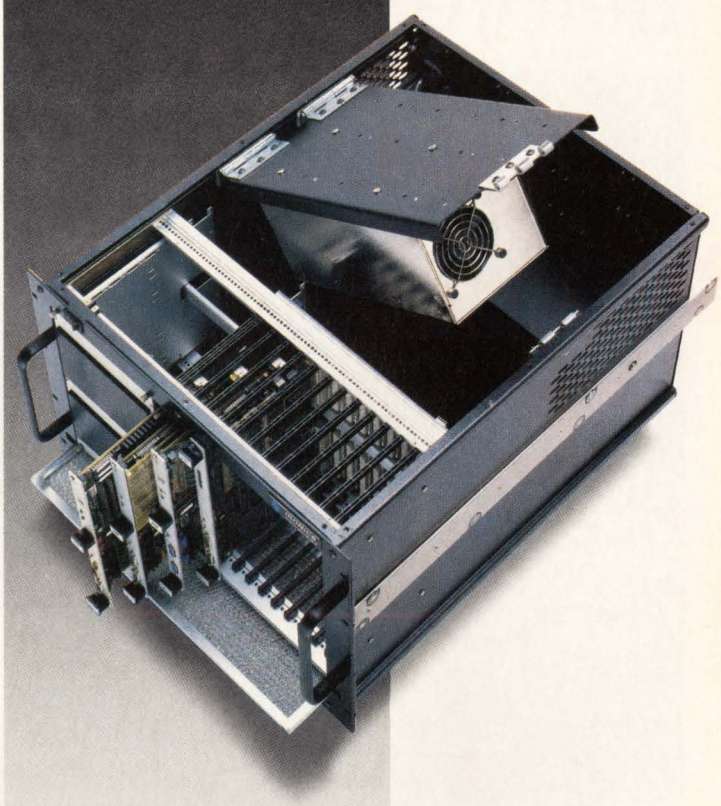

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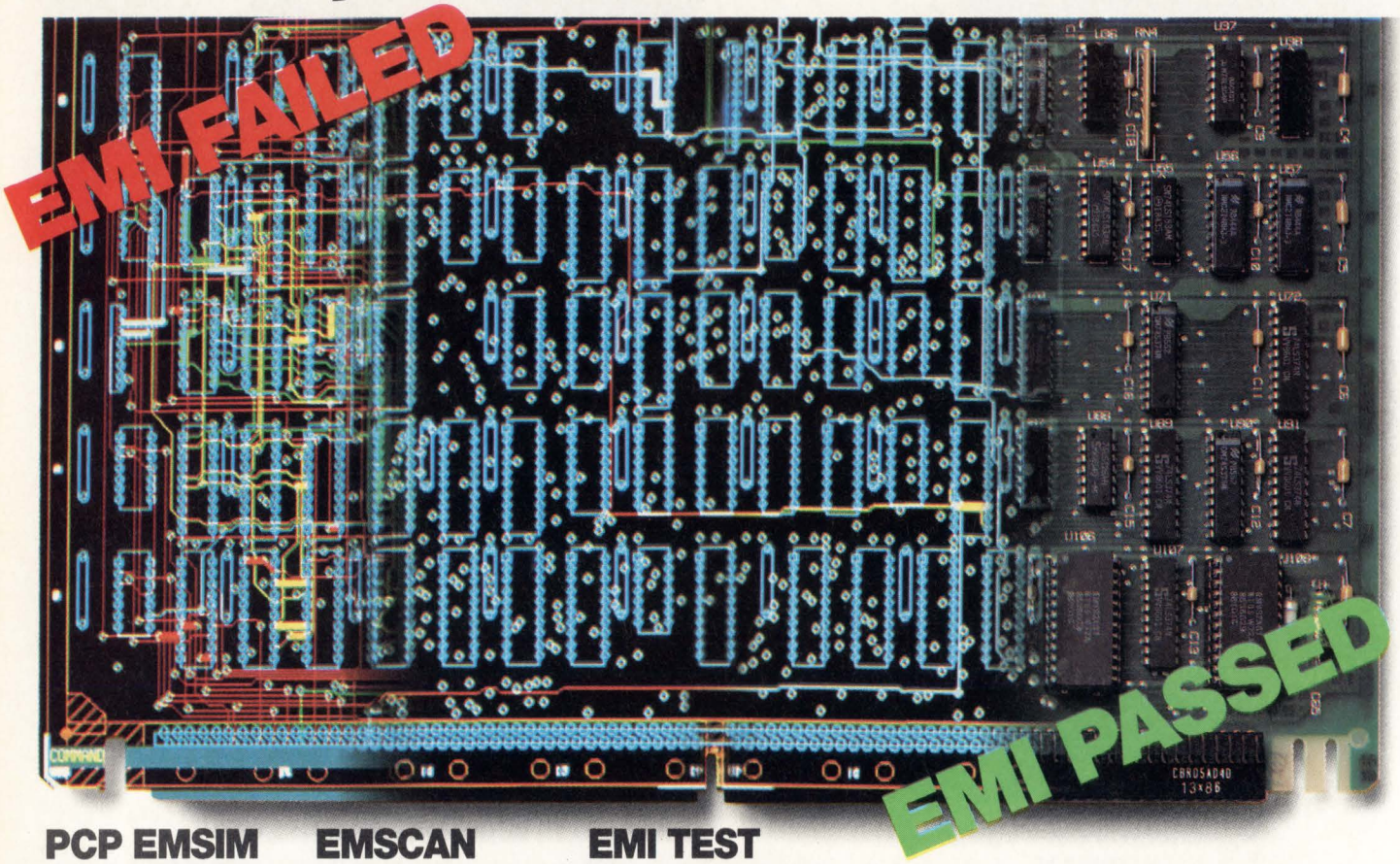


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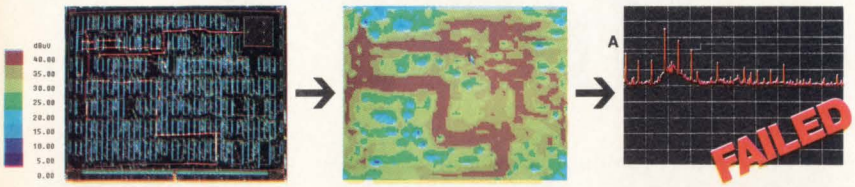


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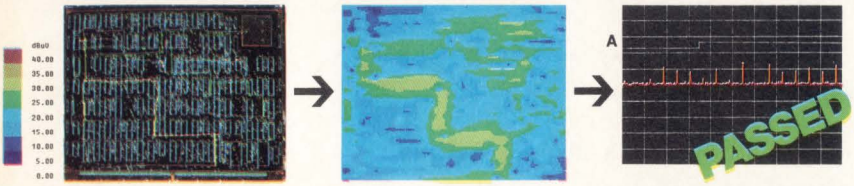


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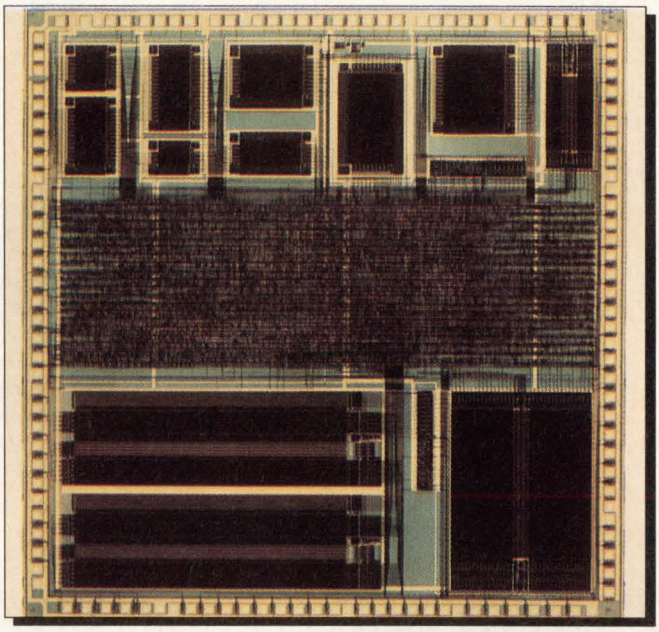
CIRCLE NO. 39

# High-density ASICs force focus on testability

***Getting an ASIC of 20,000-plus gates to market on time means building testability into the design flow. Designers must take a hard look at the merits of competing methods.***

**Barbara Tuck**
**Senior Editor**



***Complex ASICs, such as this macrocell-laden telecommunications circuit built in AT&T Microelectronic's 0.9-μm CMOS Standard Cell Library, combine high density with testability. Fault coverage for the macrocells and BIST (built-in self-test) overhead is greater than 99 percent. Test time is less than 1 percent of that required without BIST.***

High gate counts and maturing software tools have changed the economics of ASIC design. While ever-more-sophisticated tools have automated other tasks, the reliance on ad hoc approaches has made testability a ravenous consumer of vital resources—it currently eats up about 40 percent of the design cycle and almost 50 percent of the cost. The top economic concern of designers has shifted from area overhead for built-in test structures to getting a product to market on time.

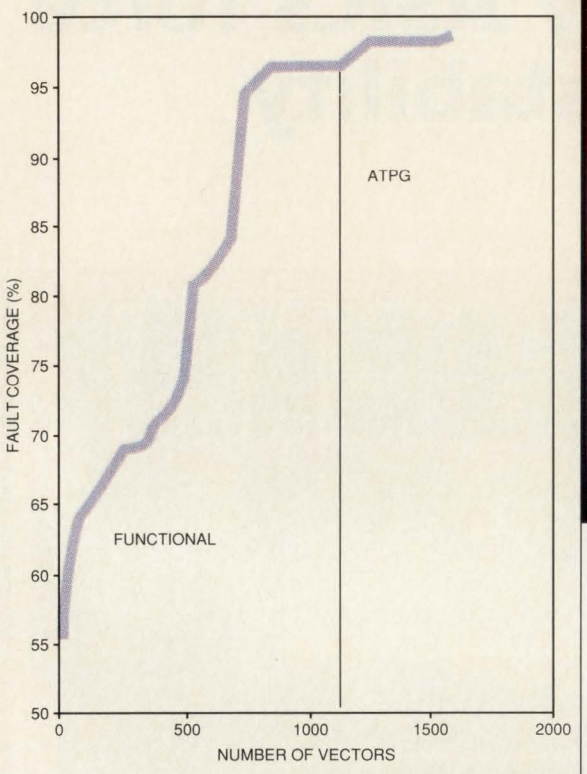
The choice of methods for designing observability and controllability into ASICs to make them highly testable isn't a simple one. There's no single approach or point tool that will give high fault coverage for all design styles. Though silicon and software vendors are finally zeroing in on up-front testability approaches that will make test transparent, there are trade-offs with every technique.

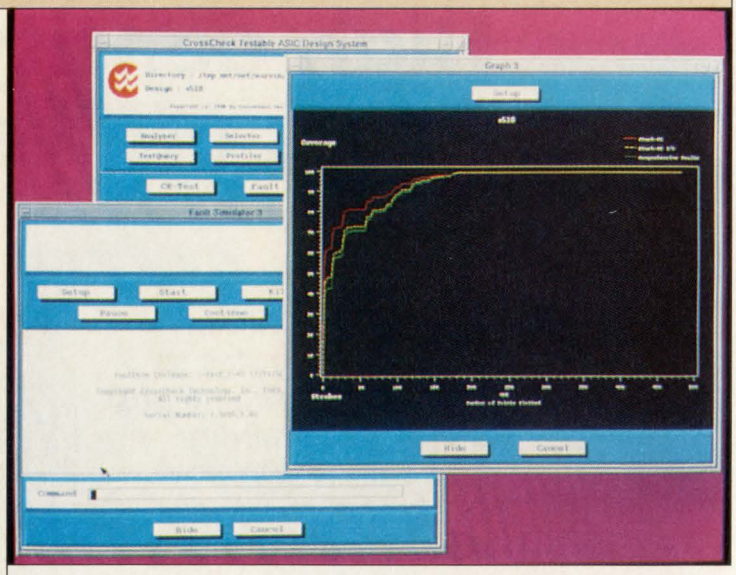
Vendors are telling users today that while they may not suffer too much from using manual brute-force approaches to testability on ASICs of 10,000 gates, the real economic threat begins at 20,000 gates and the horror at 50,000 gates. For ASICs of that density, designers can mix techniques that include embedding test electronics onto the base wafer; relying on software tools to synthesize test structures and develop a test program; or choosing a silicon vendor that offers scan cells and built-in self-test (BIST) compilers in its library as well as a good automatic test-pattern-generation (ATPG) tool. No one choice presents a panacea. The most significant issue to the ASIC designer isn't so much the approach chosen, but making that choice up front in the cycle and then strictly adhering to the design style recommended.

## CrossCheck technology

Perhaps the most complete solution to designing ASICs for testability, and the most transparent to the designer, is an inside-out, hardware/software approach being promoted by CrossCheck Technology (San Jose, CA). Certainly, the CrossCheck approach embeds test electronics onto the base wafer and requires a complete commitment on the part of the silicon vendor licensing the technology.

## COMPREHENSIVE FAULT COVERAGE VS. NUMBER OF TEST VECTORS



*CrossCheck CX-Test 1.4 software adds controllability to the 100 percent observability provided by a matrix of test points embedded onto the base wafer. As shown in the chart, CrossCheck's observability achieves high fault coverage, typically better than 95 percent, with fewer vectors. Automatic test-pattern generation provides additional coverage (between 2 and 4 percent). The system test level ASIC design display shows a graph that identifies fault coverage vs. the number of vectors used.*

Customers designing CrossCheck-based ASICs can achieve 100 percent observability as well as controllability with no performance penalty. The cost to the customer comes instead in terms of dollars, with a price premium of as much as 50 percent, and in terms of area, with an overhead somewhere above 10 percent. The LSI Logic (Milpitas, CA) CrossCheck-based 1-µm CMOS LFT150K gate array masterslices with up to 190,000 raw gates.

CrossCheck recently announced its CX-Test software products, which will add the controllability portion of the solution to the 100 percent observability provided by the embedded matrix of observation points. Controllability can be provided either by the designer or by CrossCheck's new automatic test-vector-generation (ATVG) software module.

The CrossCheck ATVG software takes a designer's functional vectors and uses three techniques, either separately or in combination, to generate additional vectors to achieve the desired level of controllability. The first technique is an algorithmic one that works well on data paths and other pipelined designs to control logic. The second, a deterministic backtrace method, works well on most sequential logic, and the third is a proprietary vector-splicing technique for difficult-to-control sequential logic.

If an ASIC designer's functional verification vectors provide a controllability level of 75 percent to around 94 percent, CX-Test's ATVG software will usually increase that level to around 98 percent.

There are a few significant advantages to the CrossCheck approach. One is that CrossCheck only needs to solve for controllability. That's in contrast to approaches that have to solve for both observability and controllability. In such cases, the computational problem of fault simulating and generating test vectors grows as a function of the square of the number of gates in a design, sometimes requiring days or even weeks of CPU time.

Another advantage is that, unlike most testability approaches, CrossCheck ATVG software operates on asynchronous as well as synchronous designs and produces race-free vectors. With most testability approaches, designers have to avoid asynchronous design styles. Also unlike most testability schemes, CrossCheck provides fault coverage for transistor-level faults. In addition to finding stuck-at faults, comprehensive fault coverage applies to shorted transistors and interconnects, as well as open transistors.

What might be considered a disadvantage to the CrossCheck testability approach is that it requires the ASIC vendor/CrossCheck licensee to edit physical libraries to add observation points. This editing process is likely to take longer than editing the storage elements required for a scan methodology. For the special libraries required for the CrossCheck ATVG and fault simulator, CrossCheck supplies vendors with silicon software that automatically generates library elements. The company also offers diagnostics software.

### Extending synthesis to test

For ASIC designers who have integrated high-level synthesis into their design systems, the most natural starting point in the exploration of testability techniques would be with test synthesis tools. Most in the industry agree that a test synthesis tool or toolset should incorporate both the synthesis of test struc-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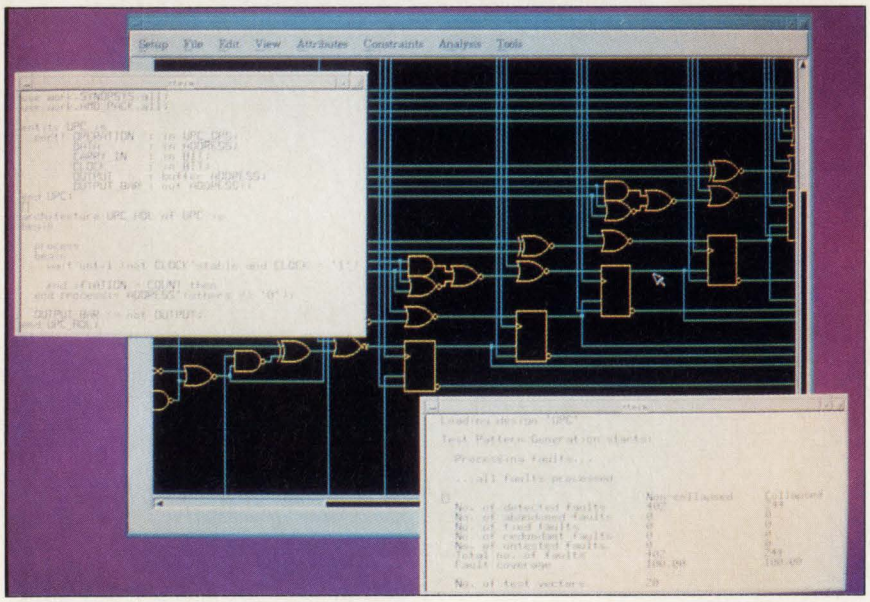
CIRCLE NO. 40

tures and the automatic generation of a test program. And those tasks are exactly what the Test Compiler from Synopsys (Mountain View, CA) adds to the company's well-established products for hardware description level synthesis and circuit optimization.

Using a full-scan approach and the conventional combinational ATPG method, the Test Compiler synthesizes testable ASICs by eliminating redundant logic, inserting test structures, reoptimizing the design for area and speed, and automatically generating a test program for 99.9 percent fault coverage.

Solbourne Computer (Longmont, CO), a user of Synopsys synthesis tools, has been acting as a beta site for the Test Compiler. Manager of ASIC design, Dan Ganousis, reports that it took only one afternoon to fit the test synthesis program into the Synopsys flow. Solbourne's goal was to take HDL-level gate arrays with 10,000 to 30,000 gates and redesign them for testability with the aid of the Test Compiler. Solbourne had previously relied on the well-proven Teradyne (Santa Clara, CA) Aida testability tools, with automatic scan-ring generation, ATPG capability, and fault simulation.

Though the Solbourne design team encountered glitches with the Test Compiler beta tool, Ganousis reports that the new Synopsys tool runs 5 to 10 times faster than the Teradyne tool. Teradyne offers a hardware accelerator to speed the task; however, Ganousis frowns on the need to be locked into hardware. Fault coverage (between 95 and 100 percent) and area overhead are indistinguishable from the Teradyne to the Synopsys tool, according to Ganousis.



*The Synopsys Test Complier displays a synthesized VHDL module that has had scan registers inserted. The fault coverage report (lower window) shows fault coverage and a breakdown of faults. Test Compiler synthesizes scannable gate-level designs from register-transfer-level VHDL descriptions.*

## Some design fixes required

Western Digital (Irvine, CA) is another beta site for the Synopsys Test Compiler, and design automation engineer Lori Farnworth says that the time saved writing test vectors made design changes to an 8,000-gate ASIC absolutely worthwhile. "The use of the tool was straightforward; it gave us a fault coverage of at least 99 percent," Farnworth reports.

One problem encountered by the Western Digital team is that the Test Compiler wants to insert scan structures into shift registers, which are, of course, inherently scannable. The Test Compiler is overenthusiastic about shift registers, admits Synopsys product manager Pierre Wildman, and Synopsys will be modifying the tool. As to the read/write register blocks that required manual intervention from the Western Digital team, he says, designers will have to intervene to make blocks that shouldn't be scanned—including RAMs and ROMs—invisible to the Test Compiler.

As potential customers evaluate the Test Compiler, a universal gripe concerns its single-scan-chain limitation. Synopsys is scrambling to add multiple-scan-chain capability, which should be incorporated into production code by this summer, according to Wildman. A solid Joint Test Action Group approach will also be added within the year. The company is looking at adding a BIST capability, but isn't likely to do so within the near future.

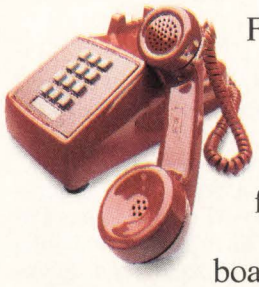
Sequential ATPG is another area receiving considerable research attention from Synopsys. As the outcome of sequential ATPG becomes more predictable across a broad spectrum of designs, says Wildman, Synopsys will be moving from full scan and combinational ATPG to partial scan and sequential ATPG. Sequential ATPG is far more complex than combinational ATPG, according to Wildman, and presents a messy computational problem.

## Test synthesis joins team

Intelligen from Racal-Redac (Westford, MA) is a sequential ATPG tool and can thus accommodate partial-scan methods. Racal-Redac won't be releasing Version 2.0 of the SilcSyn test synthesis module until the testability and ATPG capabilities of Intelligen can be combined with the improved test synthesis of SilcSyn. Racal-Redac is delivering production-quality test synthesis to several customers this month.

SilcSyn employs the register-transfer scan (RTS) approach to testability. With RTS, an arbitrary sequential design is turned into a feed-forward sequential design, where all sequential feedback paths are broken and their storage elements incorporated into a partial-scan chain during test mode. Designers can specify the maximum feed-forward sequential depth and trade off area efficiency against test-pattern-generation time and test-pattern length. SilcSyn will automatically modify even asynchronous designs for testability; optimize the test logic and functional logic to ensure efficiency; and generate a full set of manufacturing test patterns to achieve near 100 percent fault coverage.

According to Racal-Redac, SilcSyn 2.0 will allow either pushbutton testability or interactive testability. In the pushbutton mode SilcSyn will automatically insert partial or full scan and JTAG IEEE boundary



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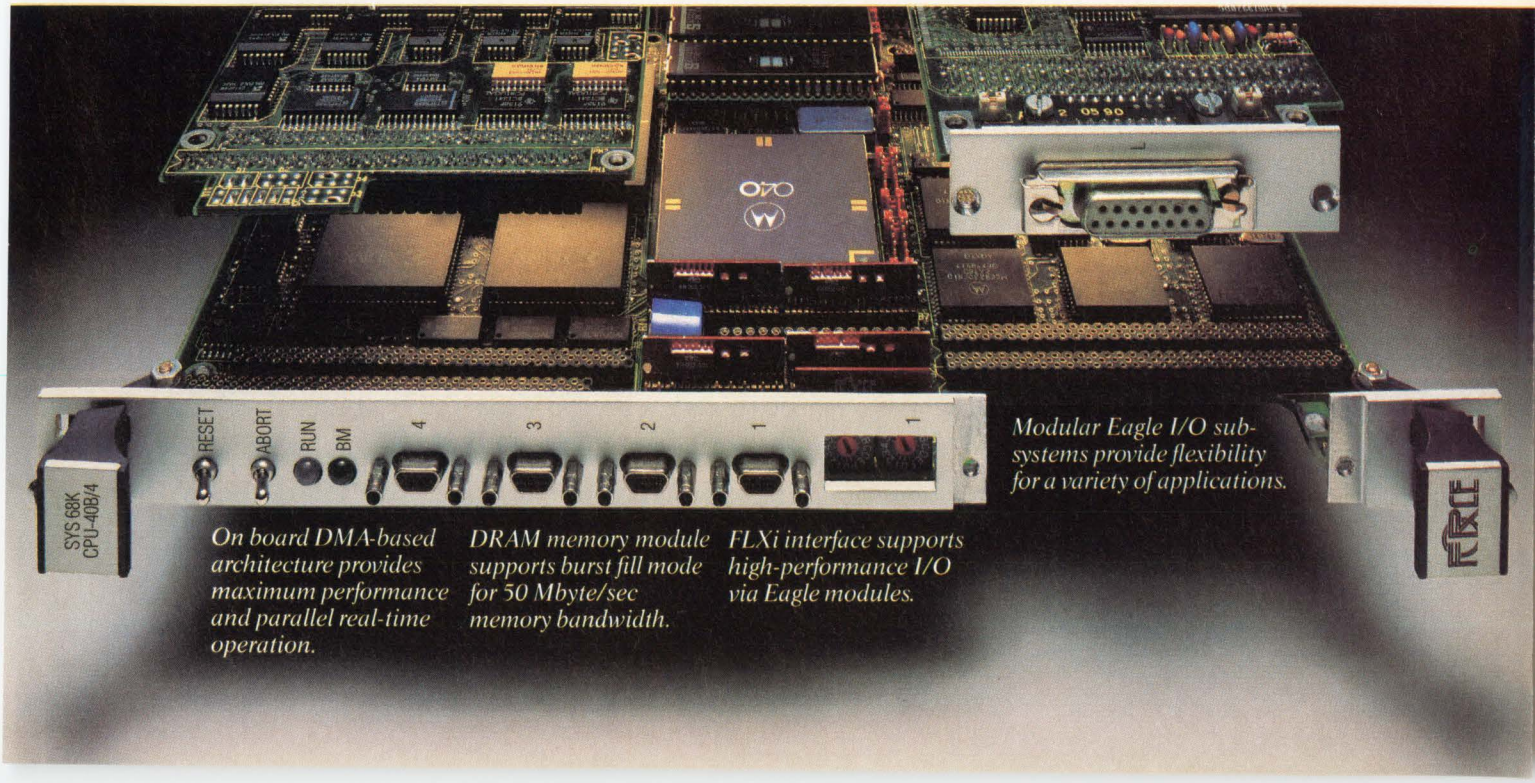
**CIRCLE NO. 41**

# WHY THE FIRST 040 VME MIGHT AS WELL BE THE LAST.

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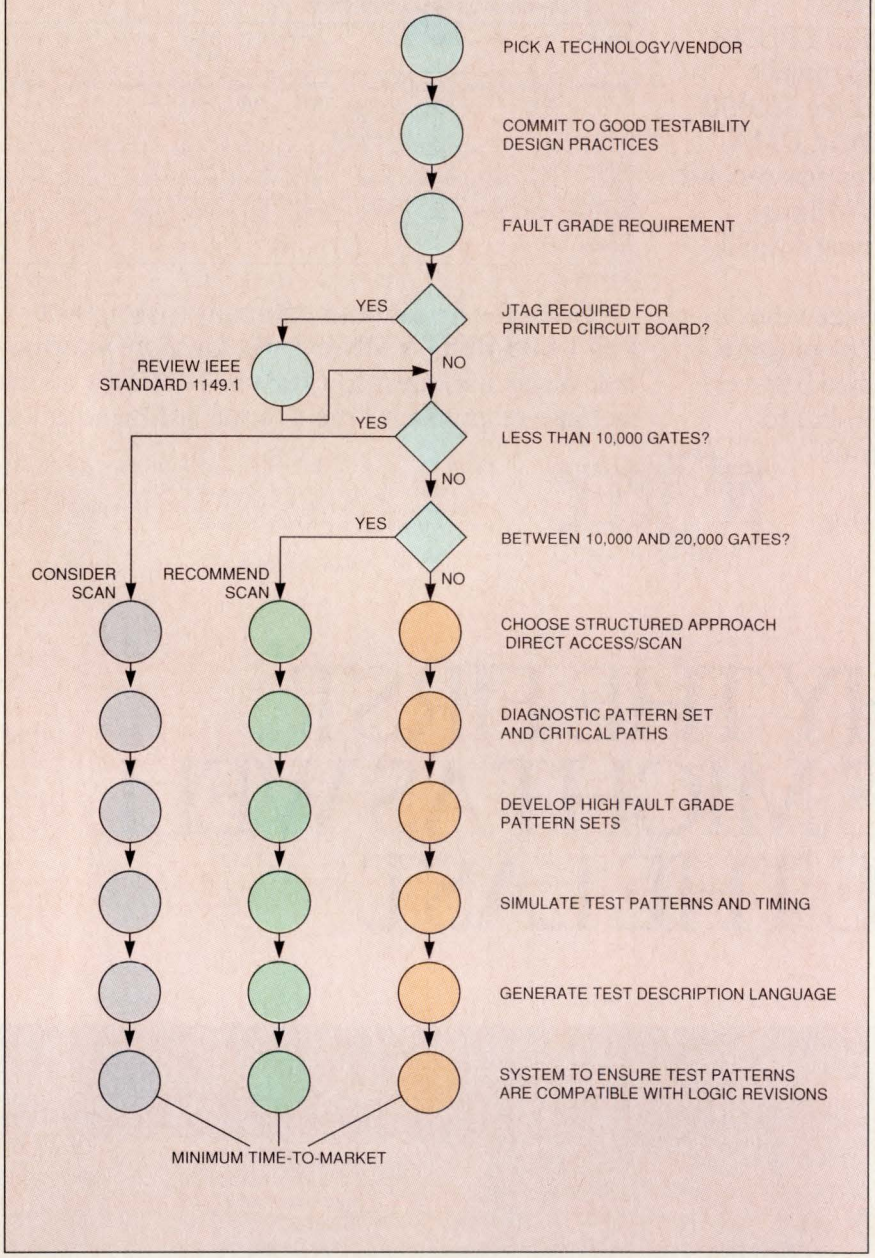
## HOW TO SELECT A DFT APPROACH




***Texas Instruments recommends that customers designing ASICs of 20,000 gates or more incorporate design-for-testability techniques into their design flow. TI urges customers to define a test strategy up front in the design cycle but reports that, to date, 60 percent of its customers don't do fault grading.***

scan with little performance impact. The interactive choice has Intelligen providing dynamic testability analysis and test generation by guiding the designer's selection of minimum scan path for no performance impact.

When used together, SilcSyn and Intelligen complement each other's expertise. SilcSyn's knowledge of the design, such as which signals are clocks and which registers hold state values, is used to improve Intelligen's application of reduced-intrusion-scan-path methodology. Intelligen, in turn, uses SilcSyn to automatically insert its test logic cells and reoptimize the design. The system can automatically highlight on Visula schematics the circuit nodes recommended for testability improvement. For fault grading, Intelligen transparently uses Cadat's fault simulation capabilities.

The tight integration of Racal-Redac's VHDL synthesis (released to beta sites), simulation, and test software that synthesizes even asynchronous designs makes for a design environment that bears watching.

Like the Racal-Redac software, the Test Design Expert (TDX) from ExperTest (Mountain View, CA) also generates test vectors for asynchronous as well as synchronous designs. Though TDX synthesizes only test vectors, not test logic, it's often classified as a test synthesis product.

TDX combines knowledge-based ideas and the algorithmic approach to achieve between 90 and 100 percent fault coverage, depending on circuit size and complexity. ExperTest claims that customers can get good test programs with TDX whether or not they use a design-for-testability method. For combinational or full-scan designs, TDX requires only a netlist. For sequential circuits, a behavioral description at the register-transfer level (RTL) is also required. TDX uses VHDL-T, an RTL-level subset of VHDL, as its behavioral modeling language.

Among EDA vendors integrating TDX into their design systems are Valid Logic Systems (San Jose, CA) and Viewlogic Systems (Marlborough, MA). A software interface between TDX and Valid's Design Process Framework will let VHDL behavioral and gate-level descriptions be fed from ValidGED design capture into TDX. TDX will then generate test vectors and import them into Valid's RapidTest concurrent fault simulator. Though Valid users can access TDX, the ExperTest software won't provide back annotation to ValidGED until it's more tightly integrated into the Valid environment.

### Test: a design-flow issue

Valid isn't the only broad-line EDA vendor integrating DFT tools into its framework-based toolset. But whereas Valid is adopting a third-party tool, Cadence Design Systems (San Jose, CA) and Mentor Graphics (Wilsonville, OR) are developing their own test synthesis products. Just last month, Cadence introduced its two-part synthesis product—the Improvisor and the Optivisor.

For Cadence, test synthesis will involve developing a test program

and synthesizing for testability by inserting test structures, according to Rick Friedman, test products manager at Cadence's Systems Division (Lowell, MA). The Cadence philosophy, explains Friedman, is to look at testability as a design-flow issue, not as something that can be solved with a single point tool. Testability rules will be separate from test-pattern generation—with the rules built into the Improvisor front-end synthesis product, and ATPG occurring later in the design flow than the Optivisor. Users will be able to analyze technology-specific trade-offs before doing ATPG.

Customers using high-level synthesis will be forced to use test synthesis, says Bob Erickson, engineering manager for AutoLogic at Mentor's Design Synthesis Division. Mentor's own test synthesis solution is presently under development. The company's intent is to make its Explorer sequential ATPG tool, an option to Genesil, part of the AutoLogic high-level synthesis tool. Mentor's test strategy includes the incorporation of scan insertion into AutoLogic; users will have the option of full or partial scan. And company also plans to add the capability of optimizing for area and speed after the insertion of scan structures.

Mentor reports a letter of intent from CrossCheck Technology with regard to CrossCheck's becoming an Open Door partner of Mentor. It's not likely that CrossCheck software will be accessible to Mentor users, though, until some time after Mentor has completed the first-phase release of its Concurrent Design Environment Version 8.0.

## Look for DAC demo

The HiDesignA logic and test synthesis product from GenRad (Fareham, Hampshire, England) will be released following demonstrations at the Design Automation Conference in June, says Wesley Ryder, GenRad's business development manager for synthesis. HiDesignA will accept design descriptions in various formats—VHDL, GenRad's own HDL (GHDL), EDIF, equations, truth-table inputs, state-machine and programmable-logic-device. GenRad has been integrating into its System Hilo 4 environment the synthesis technology it acquired from Aptor early in 1990. Common library elements will be shared across simulation, synthesis, test, timing analysis, and fault simulation.

The HiDesignA test synthesis module, according to Ryder, will automatically insert test structures and generate test vectors for both internal-scan and JTAG-compliant boundary-scan solutions. Users will be able to verify a design at the board level with a description written in boundary-scan description language. If users modify the order of scan elements following physical layout, Ryder says that they will be able to reorder the vectors to reflect the new topology. A potential enhancement to this approach, is for HiDesignA to accept placement information before routing in order to generate a scan netlist that minimizes interconnect and thus overcomes problems due to excessive loading. HiDesignA will interface directly to System Hilo 4's HiTest modules for testing imported blocks such as embedded memories or purely sequential logic.

***There's no single approach or point tool that will give high fault coverage for all design styles.***

Beta-site testing of the VHDL version of the Frenchip synthesis product from Dassault Electronique (Saint-Cloud, France) began last month. Frenchip can synthesize partial- or full-scan paths. For JTAG-compliant designs, it can synthesize a JTAG ring. And for BIST, Frenchip provides built-in logic block observation (BILBO) cells, pseudo-random pattern generators, and dedicated options for testing functions such as counters. Frenchip also lets designers describe and use their own JTAG and BILBO cells. The synthesis software runs on Sun-4 workstations and will be ported to other Unix workstations this year.

## Silicon vendors' strategies

Most silicon vendors are choosing to stick with their own techniques until the newer approaches mature. Texas Instruments (Dallas, TX), for instance, sees the Synopsys Test Compiler's single-scan-chain capability and CrossCheck's inability to supply test coverage for fully diffused, embedded memories as indications of the tools' immaturity.

There are consistent restrictions among tools that do scan insertion and ATPG, says Bob Gruebel, TI's manager of ASIC test development. Some of these restrictions include requirements for synchronous design, externally controlled clocks, combinational feedback loops, and libraries that are compatible with the tools. Gruebel also says that only 40 percent of TI's customers define a testability strategy up front, and that noses are beginning to get bloodied. "It's one thing to have a single ASIC on a board and get a 5 percent fallout rate," Gruebel says, "but when you have 10 ASICs on a board, that fallout rate will get unacceptably high."

With testers costing megabucks, Gruebel says customers have to define a structured approach to keep costs down. TI urges customers to avoid asynchronous design practices and recommends the use of internal scan and JTAG boundary-scan cells at 20,000 gates. Direct access through I/O pins is made available for fully diffused and metalized function blocks buried deep in designs (TI calls such blocks megamodules). TI supplies vectors for these blocks, which include FIFOs, SRAMs, PROMs, DSP core cells, multipliers, and ALUs. TI accepts test programs from third-party tools such as Intelligen, Cadence's Testscan and GenRad's Hilo.

## No speed penalty

Vertex Semiconductor (San Jose, CA) will also go with sequential pattern generation as tools improve, according to Carey Chin, test engineer manager at Vertex. At present, sequential tools tend to have problems with some kinds of circuits and are far more difficult to work with. Vertex relies on its combinational, full-scan Fascan tool to integrate testability into its high-performance ASICs.

Motorola (Chandler, AZ), a strong proponent of scan, relies on its proprietary Mustang combinational ATPG tool to modify a design to conform to scan methodology. Mustang ignores customers' asynchronous circuitry for which designers must write functional vectors. Motorola is evaluating the Test Compiler, says Roy Jones, principal staff engineer for ASIC design, and might work with Synopsys to incorporate the advanced algorithms of Mustang into the Test Compiler and then make

the Synopsys tool accessible to customers through Motorola's Open Architecture CAD System.

## BIST for cell-based ASICs

AT&T Microelectronics/ASICs (Allentown, PA) uses its Macrocell Layout Generator to automatically generate BIST in ASIC macrocells for cell-based designs. An advanced cell-based design may have more than 20 macrocells, each macrocell carrying with it its own set of potential faults. By exploiting a macrocell's functional and structural characteristics, AT&T produces BIST algorithms based on specific macrocell fault models.

BIST procedures used in macrocells such as SRAMs, ROMs, register files, content-addressable memories, and FIFOs yield greater than 99 percent fault coverage, according to AT&T. For SRAMs, fault coverage is extended to the BIST overhead. AT&T's CMOS standard-cell library contains a standard JTAG boundary-scan test access port that can be designed into BIST-based ASICs.

BIST methodology for regular structures such as RAMs is also among the DFT techniques backed by VLSI Technology (San Jose, CA). VLSI's Test Assistant automates BIST as well as multiplexed block isolation and scan. The VLSI BIST library contains a BISTRAM compiler that generates circuitry for testing RAM blocks and a compiler that generates linear-feedback shift registers for application-specific BIST pattern generators or signature analyzers.

In addition to supporting a manual ad hoc method, the Plessey Design System (PDS) from Plessey Semiconductor (Scotts Valley, CA) supports the BIST test method for large ASICs. PDS-BIST requires the designer to partition the circuit into a number of smaller testable blocks.

## Scan cell libraries

As ASIC gate counts multiply, an increasing number of ASIC vendors are including scan cells, both for internal scan rings and JTAG-compatible boundary-scan rings. SGS-Thomson Microelectronics (Carrollton, TX) now offers scan test flip-flops and latches for its ISB18000 Continuous Arrays series. And for mixed analog/digital ASICs, International Microelectronic Products (San Jose, CA) offers analog scan intrusion cells for redirecting the signal flow during test; analog scan measurement cells for measuring internal nodes; and digital scan cells for random-access scan.

Beginning this month, Gould AMI (Pocatello, ID) is extending its ASIC design services to include the NetTag boundary-scan test service. NetTag automates the process of making ASIC designs compatible with JTAG by inserting boundary-scan circuitry and serializing parallel functional test patterns. NetTag operates with Gould AMI's NetTrans netlist translation service and NetScan scan insertion and ATPG tool.

***"It's one thing to have a single ASIC on a board and get a 5 percent fallout, but when you have 10 ASICs, the fallout's too high."***

*—Bob Gruebel, Texas Instruments*

Among the library elements supporting the VS700 submicron mixed-signal cell-based ASICs from NCR's Microelectronic Products Division (Fort Collins, CO) is a family of internal and JTAG-compatible boundary-scan cells. Customers also have access to NCR's DesignTest and DesignSim Automated Test Language tools, as well as Racal-Redac's Intelligen ATPG tool. NCR has plans to support the Synopsys Test Compiler.

Perhaps test methodology will eventually evolve to the point where there will be a single approach that suits all ASIC design styles and densities, but right now, most silicon vendors are mixing and matching techniques. Oki Semiconductor (Sunnyvale, CA), for instance, will be offering CrossCheck-based silicon for its new family of 0.8-µm ASICs having more than 20,000 gates and test synthesis as well as JTAG soft macros, at the customer's request, for ASICs with fewer than 20,000 gates. Oki is also developing a scan cell library.

LSI Logic, the first to implement CrossCheck silicon, supplements that test approach with its Test Builder scan insertion and ATPG tool, which resides within the LSI Concurrent Modular Design Environment (C-MDE). LSI customers will also be able to use the VHDL-based Silicon 1076 to synthesize ASIC designs into CrossCheck. LSI is targeting early summer for first customer ships of both C-MDE and Silicon 1076.

Creating highly testable ASICs has become such an enormous task that some industry watchers believe there will be specialty test houses springing up around the country. What's certain at present is that designers who want to get quality product to market on time need to match their ASIC design and performance objectives to a test strategy that takes all aspects into consideration. ■

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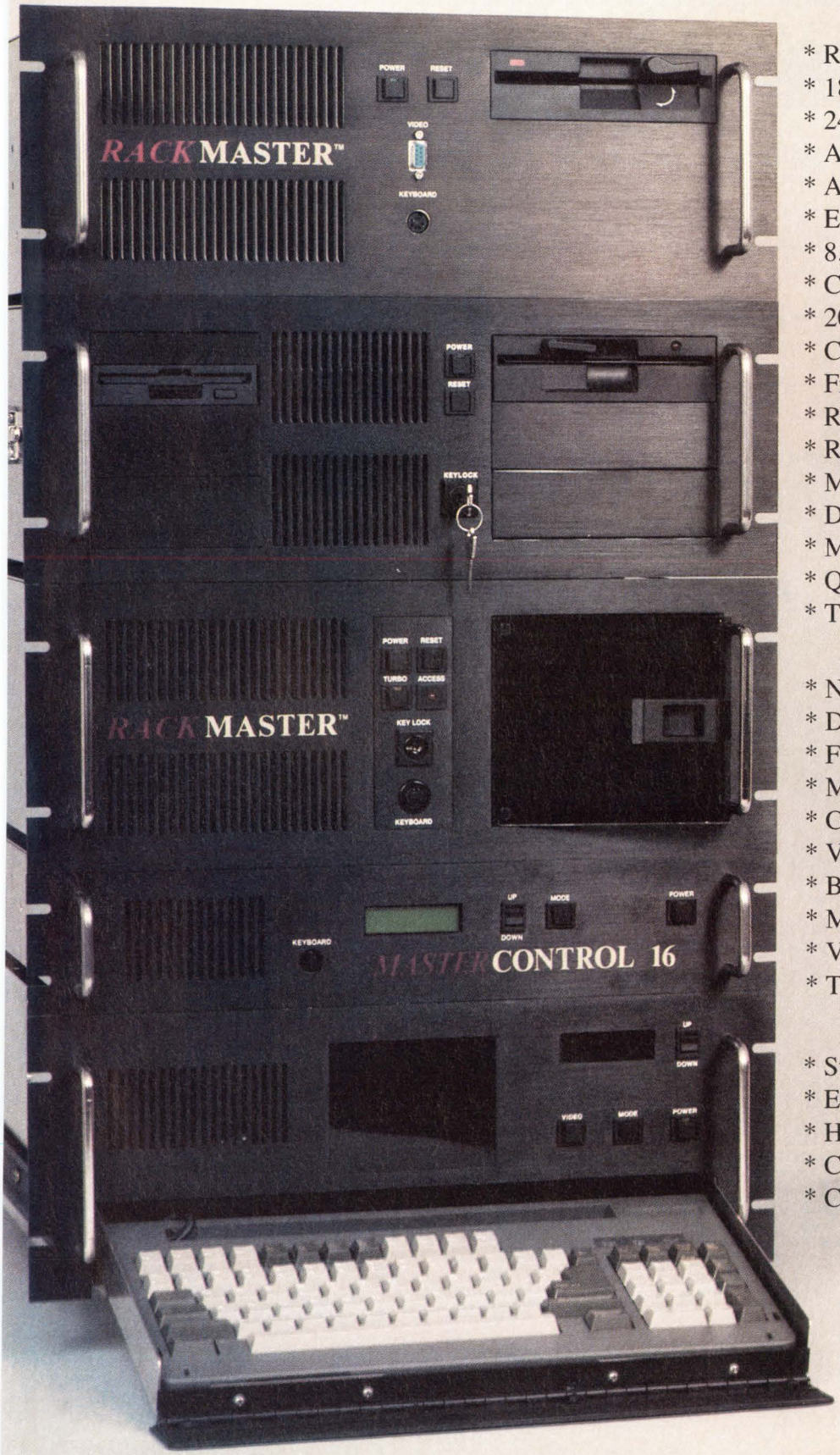


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CIRCLE NO. 42

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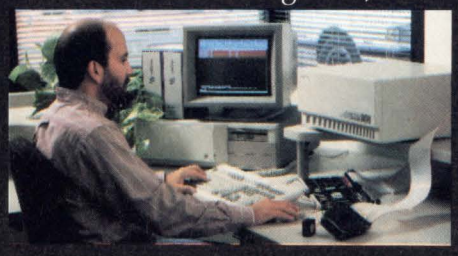

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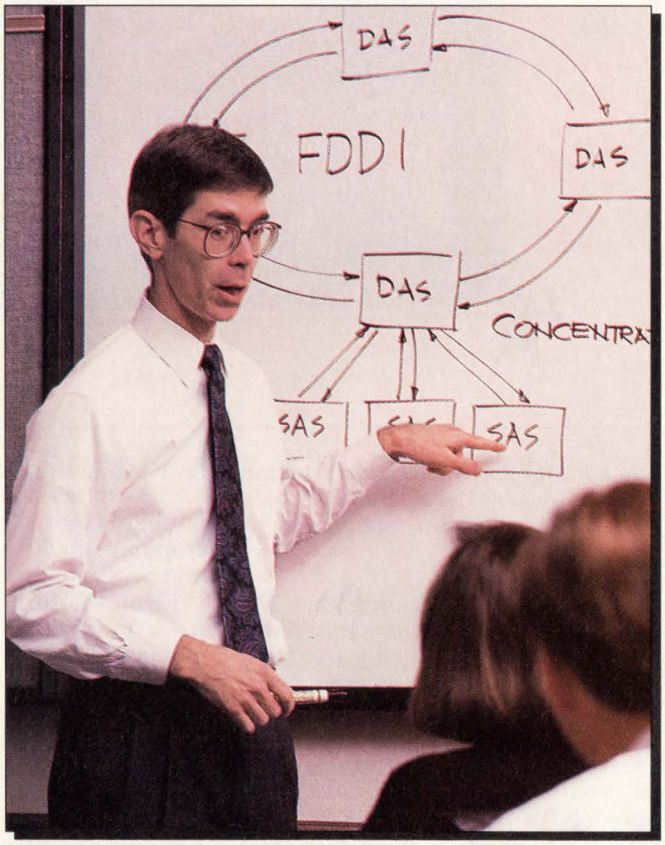
CIRCLE NO. 43

# Communications standards pit convenience against speed in standard buses

## Intelligent trade-offs are key to providing a cost-effective communications scheme for standard buses.

**Warren Andrews**
**Senior Editor**

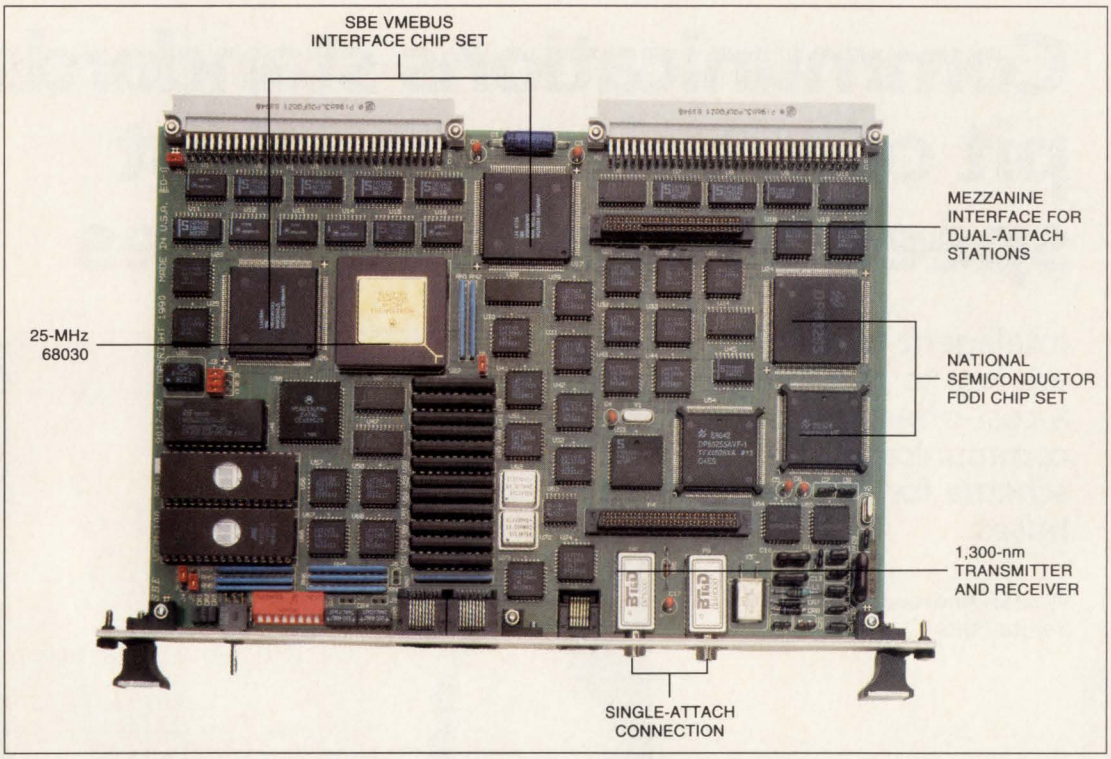



Communications schemes used in standard-bus environments—VMEbus, Multibus, Futurebus+, and so forth—vary widely, depending on individual application requirements. Major variations are in speed, price, media, and standardization. Speeds range from a couple of kilobytes per second, offered by some older token-ring networks, to rates of 100 Mbytes/s and beyond. High-speed options currently under development include Hippi (High-Performance Peripheral Interface) and Fiber Channel. Prices start at few dollars per node and top out at tens of thousands per node. Media choices similarly embrace simple twisted-pair copper through twisted-pair ribbon cable, coaxial cable, and single- and multimode fiberoptic cable. Communication formats range from well-disciplined link and network standards to stand-alone point-to-point approaches.

It's some combination of these requirements—speed, media, cost, and degree of standardization—that represents the trade-offs currently seen in the marketplace. The level of standardization, however—and the way it's implemented—have the greatest impact on the other parameters. On one hand, the standardization results in some level of interconnectivity, providing some assurance that the various system nodes will be able to talk to each other. But on the other hand, the penalty paid to provide this standardization can be high, both in terms of direct overhead and in terms of the processing power required to implement the various protocols.

Further, with the growing emphasis on wider area communications triggered by the need to transmit large amounts of information beyond the limits of a local network, there's an increasing need for boards to be compatible with standard telecommunications approaches. Standard boards will have to address point-to-point and short network approaches such as Ethernet and FDDI (Fiber Distributed Data Interface), and be compatible with telecom rates of T3 and Sonet (Synchronized Optical Network), which

***"In both FDDI and Ethernet the bottleneck is the protocol," says Ernest Godsey, marketing director for Interphase, "not the technique or the media. And the solution is more processing power, but whether to add it to the host or directly to the communication controller is up to the systems designer."***




*Efficient communications using a standard such as FDDI requires some means of handling the considerable overhead of its protocols. High-performance controller cards (such as SBE's 68030-based VCOM-100) depend on local processors keep the protocol from slowing the system host. This configuration supports single-attach FDDI; dual-attach connections require a daughtercard.*

has a scalable transfer rate starting at 155 Mbits/s (see "Single-attach FDDI links workstations," p 71).

## Going optical

There's a growing feeling that the future of communications is in fiberoptics or, more specifically, in FDDI. Telecommunications companies, for example, have been taking advantage of the higher bandwidth and greater distance capability of fiber for some time. Yet traditional system OEMs using board-level products have shied away from optical approaches in standard network applications. "The industry isn't really comfortable with anything that doesn't run on copper," says Pete Yeatman, president of Radstone Technology (Montvale, NJ).

Nevertheless, he reports that there's the beginning of an undercurrent among users looking toward FDDI. "When this undercurrent builds into a full-fledged demand," he says, "all the problems will quickly melt away and a variety of products will become available." Yeatman's belief that all FDDI problems "will quickly melt away" might be overly optimistic, however.

"As FDDI chip sets emerge—most notably from Advanced Micro Devices (Sunnyvale, CA) and National Semiconductor (Sunnyvale, CA)—more and more board-level products are expected to emerge as well," says Ernest Godsey, marketing director for Interphase (Dallas, TX). "But it's not likely that FDDI nodes will start cropping up all over like Ethernet and SCSI anytime soon."

First, the technology isn't trivial. After a day-long presentation by a major FDDI chip maker, says Godsey, one VME board maker was firmly convinced that the technology is best left to those with special expertise. Second, the chip real-estate requirements for implementing FDDI provide another obstacle to its use. "Despite the chip sets that are available, an FDDI implementation can easily take up all the real estate of a full-sized 9U card," says Godsey.

In addition to the chip set and associated glue logic, fiberoptic drivers and an interface are required, along with a megabyte or more of buffer memory. A state-of-the-art RISC or CISC processor is next, and to run the processor, a sizable amount—at least half a megabyte or so—of high-speed SRAM must be used. "Because of the high chip count," says Godsey, "there are less than a handful of 6U VME product announcements, and even fewer real products."

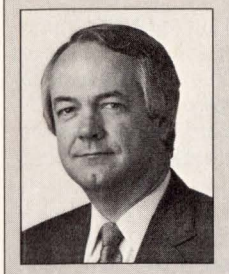
## Ethernet—stronger than ever

Though a few manufacturers are struggling to stuff the proverbial 10 lb in a 5-lb bag, some board makers see Ethernet as the strong leader for the time being. "There are very few OEM applications that can't be satisfied with Ethernet," claims Joel Silverman, Radstone's director of marketing, "even though it runs at 750 kbits/s at best, instead of the theoretical 10 Mbits/s."

"It's such a well-established standard," says Mike Strang, advanced technology vice-president at SBE (Concord, CA), "that almost every system includes at least one or more Ethernet nodes." Interphase's Godsey adds, "Ethernet nodes residing on CPU or multifunction cards are quite satisfactory except for systems where communications is a major function. In those situations, a full-fledged intelligent controller board is required."

There are some OEMs that opted to wait for FDDI instead of developing Ethernet implementations, according to Silverman, but these companies have had to rethink their approach as the FDDI timetable has stretched out. And despite Silverman's claim that many OEM applications can be satisfied with Ethernet, a few OEMs are screaming for higher transfer rates. "Ethernet was developed over 10 years ago to provide a 10-Mbit/s transfer rate," says one supercomputer OEM. "Now, 10 years later, we see FDDI with only a single-order-of-magnitude improvement, but memory has increased by three orders of magnitude in den-

## *Single-attach FDDI links workstations*



Up until recently, Ethernet met most networking demands. Computers within departments were linked over Ethernet LANs, and the LANs were connected by bridges. Department-level servers were connected directly to the LANs. Communications with remote sites was accomplished through a wide-area network server connected to a T1 link.

As the applications and complexity of computing grew, data communication requirements increased, and the LAN/bridge approach began to lose its effectiveness. Networks became bogged down as more users tried to access common equipment, such as servers. Powerful workstations and high-bandwidth applications, such as imaging and graphics, made greater demands on network bandwidth.

### LAN evolution

To address this problem, FDDI (Fiber Distributed Data Interface) was developed as a standard for new, high-speed networks. Acceptance of FDDI backbone networks was early and brisk, especially in graphics and imaging applications. The typical FDDI topology includes Ethernet subnetworks of workstations that are connected to the backbone via intelligent Ethernet/FDDI dual-attach bridges. To keep performance of the Ethernet LANs reasonably high, the number of workstations is kept low and the file servers are removed to the 100-Mbits/s FDDI backbone.

FDDI offers better performance, but at a price, usually several times more than Ethernet. The FDDI standard defines two counter-rotating rings of fiber cable for fault tolerance. Systems requiring implementation of the fault-tolerant capability of FDDI must connect to the main ring through primary and secondary fiber attachments. This configuration requires dual-attach interface cards, at $12,000 to $15,000 for each station, a cost that prohibits the direct connection of workstations to an FDDI ring.

Directly connecting workstations to the backbone also creates network-management problems. For example, as users power down their stations or as local work groups are rearranged, the entire backbone must be reconfigured.

### Lowering FDDI cost

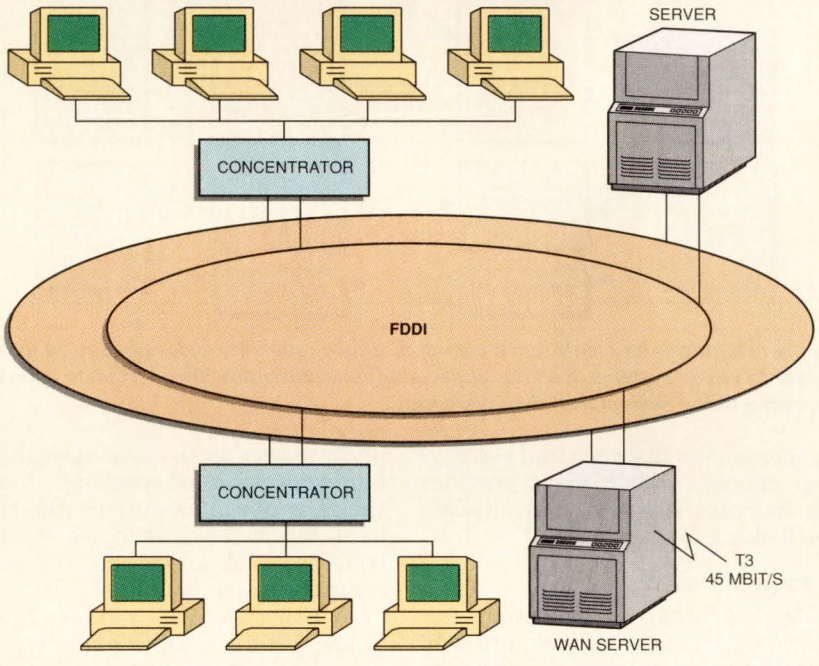
However, a cost-effective solution for obtaining the performance benefits offered by FDDI is increasing in popularity: connecting single-attach workstations directly to an FDDI network concentrator. In this approach the concentrator serves a function similar to a bridge. It connects via dual-attach cables to the main FDDI ring, while single-attach fiber cables run between the workstations and the concentrator.

Centrally used stations, such as servers, are directly connected as dual-attach stations to the network. And WAN capabilities are improved because a WAN server on an FDDI backbone can be upgraded from a T1 (1.544 Mbits/s) link to a T3 (45 Mbits/s) link.

The single-attach/concentrator approach offers several benefits. On the performance end, when one station powers down or the fiber breaks, the concentrator can automatically reconfigure its local connections without degrading the performance of the network. The concentrator provides the local cabling simplicity of a star topology (in which individual cables run directly from each workstation to a central point) to a network that has the communication efficiency of the logical ring configuration. This architecture also improves network manageability by eliminating the reconfiguration problems presented by large numbers of dual-attach stations.

The single-attach/concentrator approach is cost-effective for workstations. Single-attach FDDI adapter cards currently range from $4,500 to $8,900, and pricing is expected to decrease over time.

### FDDI FOR WORKSTATIONS

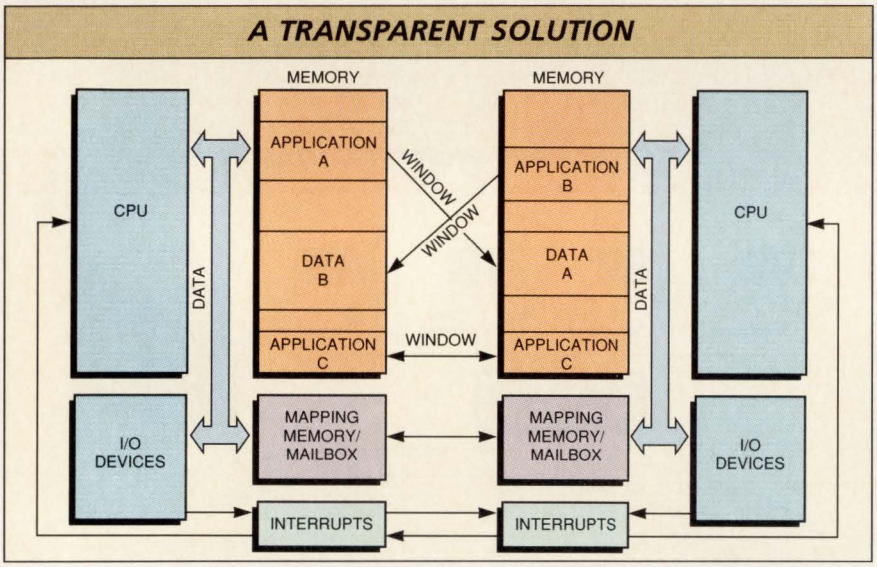



***The cost of implementing FDDI links can be brought in line with typical workstation budgets by opting for a single-attach link. Each workstation shown is linked to the network by a single fiberoptic cable. The network is implemented as two redundant fiberoptic cables, providing fault tolerant capabilities.***

**Mike Strang,** vice-president of advanced technology, SBE

sity, microprocessors have jumped two orders of magnitude in clock speed, and logic has dropped almost two orders of magnitude in propagation delay."

Today's conventional computer architectures, however, are hard put to handle transfer rates in the 100-Mbit/s range, says Russ Sharer, director of marketing for Rockwell subsidiary CMC (Santa Barbara, CA). "FDDI is being embraced for a lot of reasons," he says. "First, it's the first true computer-based fiberoptic standard to emerge. Second, it provides an increase in distance and security over copper, and third, it provides the increase in speed many OEMs are looking for."




*Augment's proprietary high-speed communications capability is designed to be transparent to linked systems. It allows applications executing on either system to access data on a linked system as if they were local.*

## Bogged down

FDDI, like Ethernet, can become terribly bogged down when burdened with the heavy overhead of standard communications protocols such as TCP/IP (Transmission Control Protocol/Internet Protocol). "Just handling the protocols to put TCP/IP on top of FDDI transfer rates can quickly bring even a very powerful workstation to its knees," says SBE's Strang.

"In both FDDI and Ethernet," says Godsey, "the bottleneck is the protocol, not the technique or media. The problem just becomes 10 times worse with FDDI. But solutions to the protocol problems come from two different camps, and neither camp talks to the other, except under duress. I'm not going to say any one approach is better than any other, because Interphase supports both camps with different products."

The first approach, which has considerable support, is to put more processor bandwidth on the host machine. "Some customers are absolutely adamant that the only sane way to improve performance in the machine is to put more processor bandwidth where you run the protocol—the host processor," says Godsey.

"The other camp," continues Godsey, "says that 'the way to improve performance is to have specialized hardware designed specifically to optimize protocol execution—the best bang for the buck is to use specialized protocol processors for each communication channel."

In Ethernet, for example, Interphase offers a high-performance Ethernet controller card with an on-board 68020 processor. Both Interphase and CMC use an AM29000 RISC processor on their FDDI boards. SBE uses a Motorola 68030 in its FDDI approach. "Right now, we offer our FDDI board as a link-level product, though the obvious intention is to move some protocols on-board," says Godsey.

## Specialized processing

While high-bandwidth processors such as the 29000 or 680X0 permit fast protocol execution, some inefficiency arises because they're general-purpose microprocessors. The next logical extension is the creation of application-specific protocol processors designed exclusively for the execution of various communication protocols.

"Protocol Engines (Santa Barbara, CA) is putting together a custom chip set designed to execute specific communications protocols," says Godsey. "For that segment of the market that wants, or needs, the specialized performance levels available through dedicated hardware, the Protocol Engines approach is the way to go. Of course, this requires a protocol processor per node."

The system architecture, however, can affect the way communications protocols are handled. In a system where networks are segmented, for example, adding new sections will require extra CPU cycles from the host computer. So it makes sense to look at some kind of incremental approach that allows the user to increase the protocol-crunching hardware along with the number of network connections. It's easier to add a separate on-board protocol processor along with the controller node than it would be to beef up the host processor. "In this way," says Godsey, "you don't take a hit on whatever application you're running on the host processor."

## Different strokes

"FDDI is finding two very different base applications," says Godsey. "On one side, users want to take advantage of the high speed and inherently fault-tolerant characteristics of FDDI as a network backbone, while using slower approaches for local communications. If a node is lost, the system continues, and even if the cable is cut, the ring will wrap around in both directions. This provides high availability on a high-bandwidth backbone.

"On the flip side," Godsey continues, "some customers want to use FDDI for a local work group in a client/server interface. In these applications, the system may want to transfer a lot of information, such as large image files, quickly to and from server and client. These applications are segmented such that the backbone need only pass a minimal amount of information back and forth."

Perhaps there's even a third major application area, that of tying computer to computer. The main advantages seen here are in the level of standardization of FDDI and relatively high bandwidth. And while

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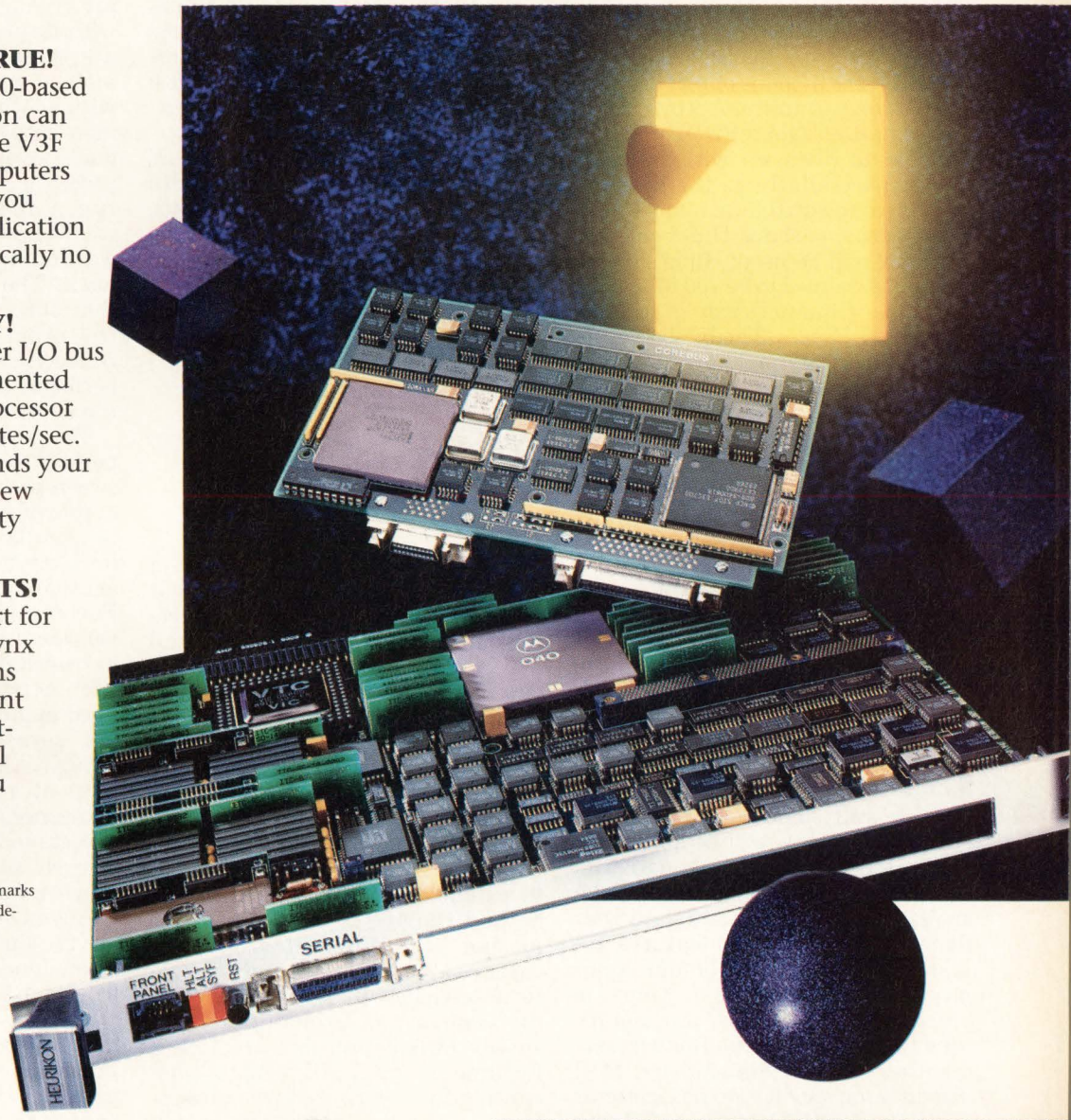


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it's interesting that a single technology can address both the first and the second approaches (network backbone and local client/server interface) and provide serious advantages to both, it's this third category that may drift away to other technologies.

For straight data transfer from point to point, or computer to computer, FDDI may suffer in a number of respects. At the low-performance end of the spectrum, Ethernet is a clear winner in terms of cost per node and the amount of real estate—board slots—it takes. At the higher-performance levels, FDDI may not be able to keep up with industry needs, particularly as the industry migrates toward Futurebus+. For these areas, perhaps Hippi or Fiber Channel will be used; Hippi's transfer rate is claimed to be 100 Mbytes/s, and Fiber Channel's rate is scalable well above Hippi's. Though both Hippi and Fiber Channel have been designated as peripheral interfaces, it's likely that the scope will be enlarged to encompass more traditional networking.

For the industry to accept these communications schemes fairly soon, however, some stringent hardware and control standards will have to be devised. The predominant consideration is that it won't be possible to maintain high data rates if a processor is in the communications path. The standards will have to establish rules for direct memory-to-memory communication.

## Proprietary communications

There's still some time before the standards groups will be able to tie down all the loose ends, though. And even at that, the result may well be such a watered-down standard that little of the desirable features remain. In place of such standard communications approaches, there is emerging a variety of proprietary schemes for tying computer systems together. Bit 3 (Minneapolis, MN) provides various box-to-box communications systems capable of tying almost any combination of standard-bus systems together. For example, the firm offers bridges from Micro Channel Architecture to VME, Multibus II to VME, SBus to VME or Multibus II, and just about every other combination available.

Furthermore, there's a growing demand for higher data rates in systems that are tied together. An early leader in crate-to-crate communications, Ironics (Ithaca, NY) offers the Multicrate Pipeline (MCPL), which uses backplane transceiver logic to achieve data rates better than 30 Mbytes/s over twisted-pair ribbon cable. The MCPL can transfer data from one VME system to another at distances up to 100 ft. Ironics also provides a high-speed DMA, real-time I/O daughterboard capable of 100 Mbytes/s on its 29000-RISC CPU board. According to Ed Schulman, vice-president of marketing, the company will double that transfer rate by doubling the data width from 32 bits to 64 bits on its Sparc-based CPU board.

These approaches, says Schulman, offer a major advantage in bandwidth over FDDI in specific applications.

***"There are very few OEM applications that can't be satisfied with Ethernet."***

*—Joel Silverman, Radstone Technology*

"FDDI is targeted at a maximum of 10 Mbytes/s," says Schulman, "but in reality, the best any real products have been able to achieve is about 6 or 7 Mbytes/s. In comparison, MCPL can operate more than four or five times faster. And up to four pipelines can be included on a single 9U card, each pipeline capable of connecting up to 12 systems—a far more efficient arrangement than existing FDDI approaches."

Schulman says Ironics is looking to extend the usefulness of MCPL beyond the 100-ft limit, and is exploring both different drivers for copper-cable solutions and fiberoptic approaches. In addition, he says, the company is exploring a high-speed DMA approach to replace a Futurebus+ to VME bridge—discarding the layers of overhead associated with the bridge and necessary translations. While making no commitment, he also indicated that SBus might be a strong consideration as a mezzanine card for such a bridge.

## Point-to-point fiber

The need for high-performance computer-to-computer communications has spurred the formation of a company dedicated to providing such channels. Industry veteran and former Xylogics executive Chap Cory is president and one of the founders of the new start-up, Augment Systems (Bedford, MA).

"Our objectives are not to provide a universal communications solution," says Cory, "but to provide a mechanism to get data from one standard-bus backplane to another in real time."

There are two main application areas Augment plans to approach with its product family. "First, there are those applications where a remote crate wants to communicate with another crate and execute common software," says Corey. "Users don't want to have to put another processor in the remote crate and run a real-time operating system with a layer of communications software on it just to pass data back and forth. The system is configured so that one crate can have direct control over the other such that the connection is almost transparent: it performs as if the board(s) were in the same crate."

The second application area is point-to-point communications between processors. Cory cites the example of a group of users who need to pass large image files back and forth but don't need some of the conventional amenities of a network. Furthermore, for these users, conventional networks are far too slow in transferring large image files. "We offer a trimmed-down and streamlined approach for these kinds of users," says Cory. "Our boards run data straight through to the application layer at a 4-Mbyte/s rate." The second-generation boards, which Cory expects to announce late this spring or early summer, will jump to a 16-Mbyte/s rate.

Augment's products comprise a relatively simple board at each system interconnected with a fiberoptic cable. "Our boards essentially provide maps and windows to the system's memory. Because of the mapping approach, the boards offer a wide degree of flexibility allowing them to be tied to a host's memory management system," says Cory. In operation, a master device at the host end writes to a window that has been set up previously. The data "magically" appears on the other bus with no special protocol involved—in many cases, not even a driver.

Augment currently provides boards for VMEbus, NuBus and some of the earlier Digital Equipment Corp machines; the company is working on

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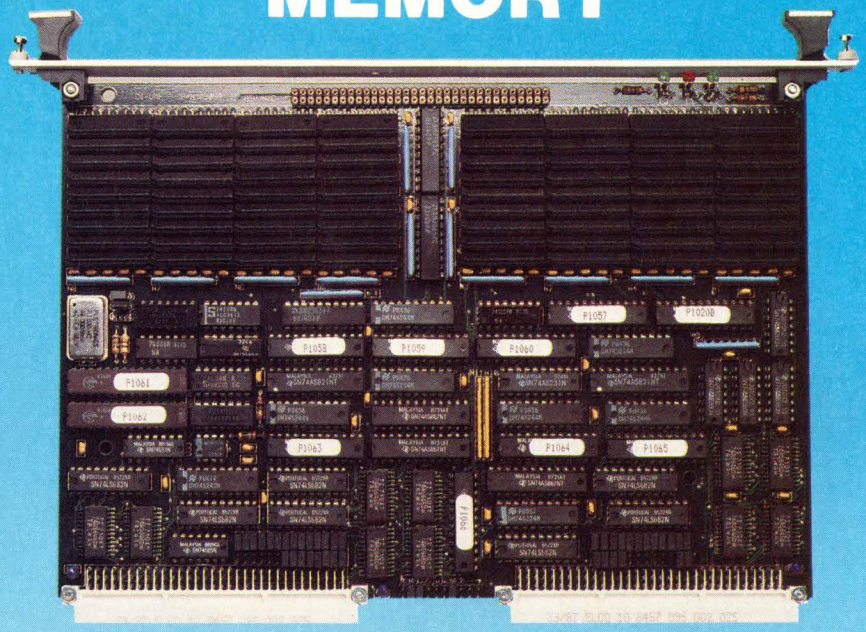

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CIRCLE NO. 45

an SBus system it expects to have ready later this year. Augment is also working on some software tools to simplify implementation of the company's boards.

Many board makers serving the communications market, such as SBE and Themis Computer (Pleasanton, CA), offer VMEbus solutions and are fast discovering even this bus wanting in the performance range. "VME64 will be the mid-life kicker for VME," says CMC's Sharer, "allowing it to participate in the next generation or two of advanced processor products.

"Traditional computer architectures are having a hard time taking advantage of a 100-Mbit/s network," Sharer continues. "I compare it to trying to take a drink of water out of a fire hose. The hose has a lot of capacity but if one isn't ready to handle it, it can bog down the whole system." In most cases, what we're seeing today is that board-level systems are running at only a fraction of their capacity—at a maximum of perhaps 20 to 25 Mbits/s.

A VME system, for example, theoretically has a capacity of 40 Mbytes/s. In reality, most VME systems are operating in only a 40- to 60-Mbit/s range. The result is that the bus-based systems have been designed to accommodate a 10-Mbit/s traffic flow. "Now, we're asking the bus to do 10 times the amount of work," Sharer points out. "It's no longer a matter of building a better computer by putting on a faster chip; it's a matter of streamlining the I/O to take advantage of the faster chips."

## Questions remain

FDDI will gradually take over many of the existing Ethernet nodes. The present high cost of FDDI—$6,000 to $10,000 per node—will continue to intimidate many potential users.

Faster technologies, most notably Hippi and Fiber Channel, will undoubtedly remain some distance off. Hippi, originally designed for copper interconnection, will probably turn to fiber fairly soon. Both technologies will undoubtedly find applications beyond that of a simple peripheral interface. But before either takes its place on standard-board products, the questions of protocol management and how to translate high data communication rates into high performance for an entire system will have to be resolved. ■

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At Interferometrics Laboratories Todd Brackett, Control System Group Leader on NRL's Big Optical Array Project, adjusts the optics on a laser interferometer.

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**CIRCLE NO. 47**

# Designers discover new tools to overcome PCB layout hazards

**Mike Donlin**
**Senior Editor**

***Complex PCBs and high-speed components demand that designers bring more information to the front of the design cycle. Layout tools are helping by providing software models of a circuit board's behavior before the expensive prototype stage.***

Printed circuit board layout tools are no longer just a mechanized way of translating netlists to a physical design. To meet the needs of escalating technologies and shrinking time-to-market windows, printed circuit board layout must encompass the concerns of design and test engineers, while addressing the vagaries of analog and thermal effects, signal integrity and, ultimately, manufacturability.

Traditionally, printed circuit board layout has been the domain of designers who were versed in the art of component placement and routing efficiency. Layout departments were often autonomous, as were the design, test and manufacturing facilities. Consequently, the needs of each were often misunderstood by the others. Most circuit boards would undergo many iterations before a board was developed that met the needs of all. Those days of leisurely design cycles and disparate management are vanishing, and printed circuit board layout tools reflect this phenomenon.

"Companies can't think of layout as an isolated discipline," says Kenn Perry, director of CAD marketing for the systems division at Cadence Design Systems (San Diego, CA). "The gap between logical design and physical implementation is being bridged by design tools that address the critical areas of timing constraints, thermal effects and parasitics. Design for testability and manufacturability are also finding their way into the layout process."

At the heart of this evolution of printed circuit board layout tools is the need to reduce prototype iterations, not only for the sake of cost and time-to-market, but also because in many instances a prototype, especially if it's a breadboard model, isn't really a representation of the finished product. Surface-mount technology components, greater densities due to multilayer boards and shrinking architectures, and the clear trend toward increasing clock rates are causing board designers to reexamine the value of using a breadboard as a debugging tool.

"A breadboard can be misleading in a high-speed, complex design," says Jim LeBrun, Board Station product marketing manager in the printed circuit board division at Mentor Graphics (San Jose, CA). "Because they're so large compared with the final product, breadboards might not accurately model transmission line effects and other parasitics. That's why a software predictor of these effects is so useful. Even if the predictions are only a best- or worse-case scenario, a designer can be forewarned about the effects of component placement before routing. That can save a lot of time."

EDA vendors are taking this need to predict circuit board behavior seriously. Printed circuit board design and analysis tool suites, such as Board Station from Mentor Graphics and Scicards from Harris Scientific Calculations, as well as environments from Calay, Intergraph and ViewLogic, offer an interface to signal analysis tools from Quad Design (Camarillo, CA). Quad Design's Crosstalk Tool Kit (XTK) offers signal analysis and simulation capabilities for ultrahigh-frequency circuit boards, while the company's modular timing verifier, Motive, provides detailed explanations for signal delays in complex ICs and printed circuit boards.

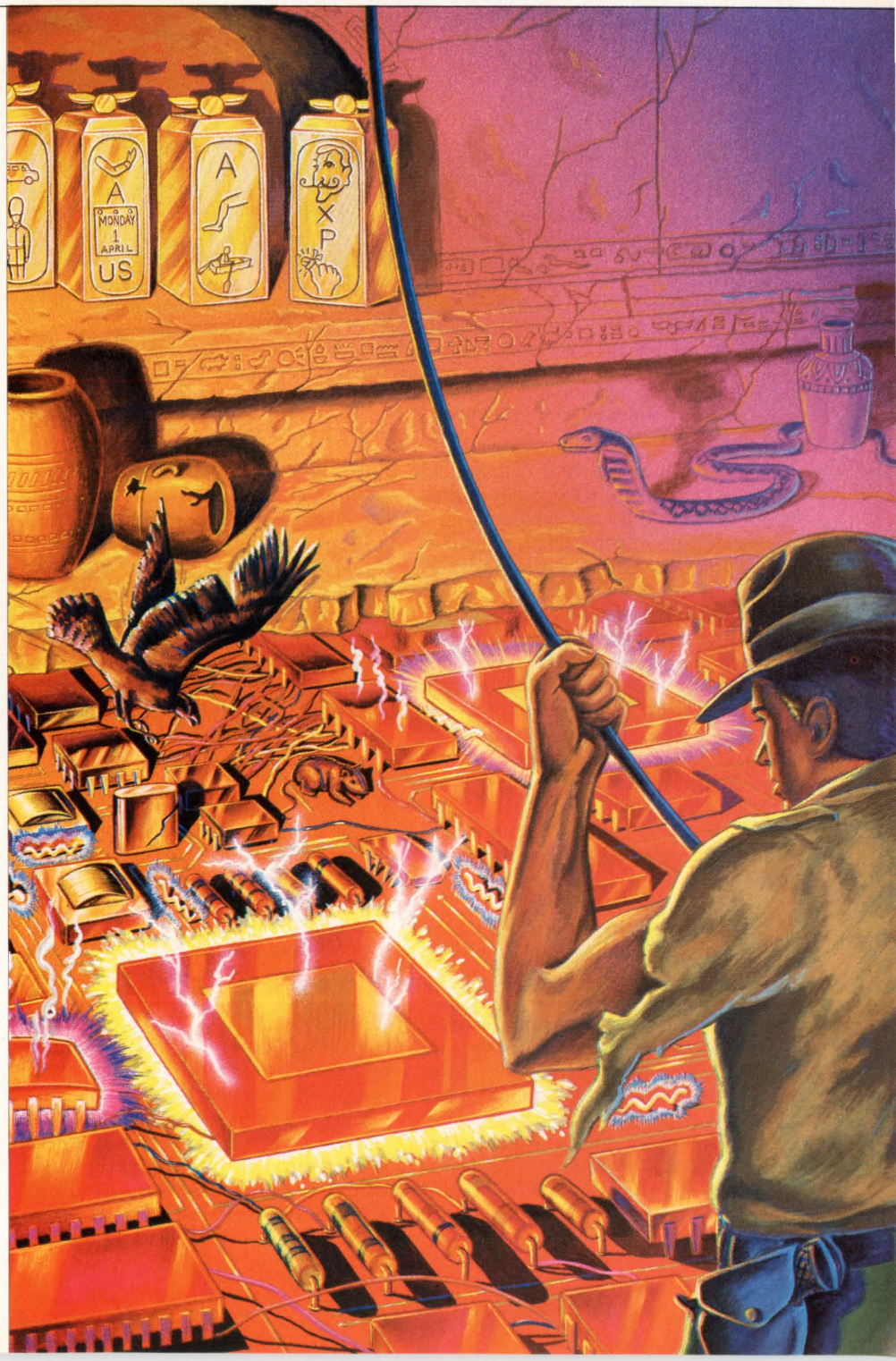
## VLSI fuels needs

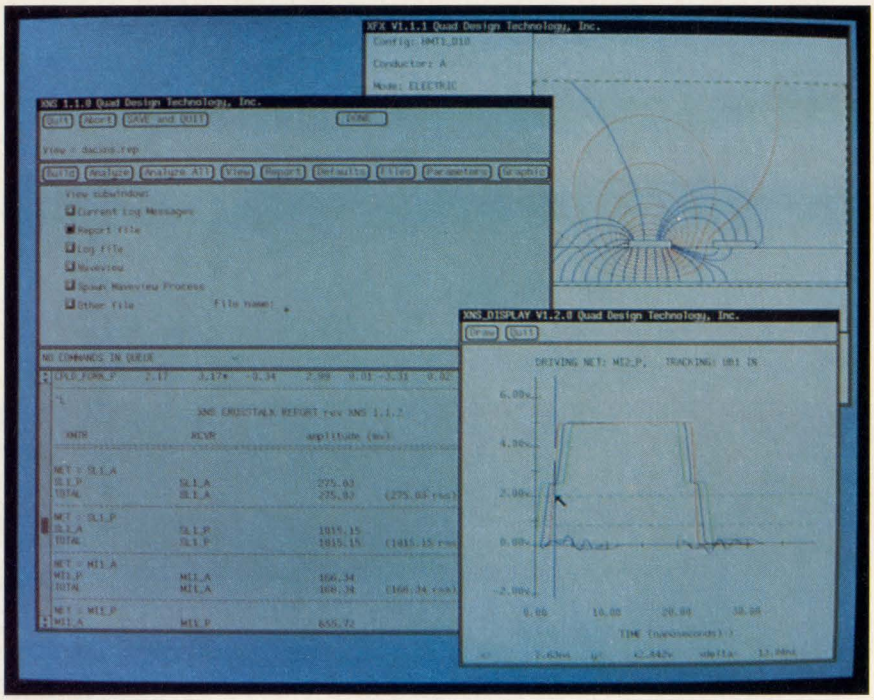
Tools like those from Quad Design have become a necessary part of high-end board design since the advent of VLSI boards with high-speed

clocks and dense packaging. While VLSI technology means higher performance, the speed and density that makes such performance possible increases the likelihood of timing-related problems. This dilemma has resulted in two basic design scenarios. First, both the number of critical timing paths in a digital design and the effects of clock signal degradation on system performance increase when clock rates exceed the 20- to 30-MHz range. As a result, signal distortions and timing errors can prevent a high-speed printed circuit board from working at all.

Second, now that designers routinely turn out ASICs with 100,000 gates and printed circuit boards populated with these devices, the idealized signals predicted by logic analysis tools are often inadequate. This is because the minute, hard-to-detect signal distortions, which logic analyzers do not calculate, can seriously degrade system performance in complex designs. Many logically correct designs fail, therefore, either because of signal distortions or because of unanticipated delays in one or more signal paths.

Quad Design's XTK predicts the effects of signal coupling or crosstalk





*The latest version of XTK, the Crosstalk Tool Kit from Quad Design, can simulate signal distortion effects for ultrahigh-frequency printed circuit board designs with operating frequencies up to 2 GHz. In the upper right of this display, the electropotentials and electric field lines of a two-conductor microstrip are displayed. At the lower right is a waveform display of a two-coupled line geometry showing the voltages of both the active and passive lines. The report on the left shows the associated noise amplitudes in millivolts.*

resulting from the use of parallel signal traces on high-density digital designs. The tool uses the designer's conductor geometry data to calculate signal line characteristics for all traces in a given configuration. It also determines the degree of crosstalk and other distortions that will affect each set of parallel traces in a circuit network. The crosstalk network simulator portion of the tool then uses this information to simulate the network waveforms that designers can expect when the printed circuit board is built. Using a mouse or cursor, designers can manipulate the waveforms to determine precisely where signal distortions occur.

"People who use our product are looking at an entire printed circuit board design and validating every net," says Chuck White, vice-president of engineering at Quad Design. "They can make sure that the signals will propagate without a lot of ringing, noise or undershoot. After they simulate the transmission lines, designers get a report that gives pin-to-pin delays, and backannotate them to our timing verification tool that contains a signal integrity flag that points out which nets can be problems."

The report can be simple, White explains, such as telling which nets go beyond a certain maximum amount of delay, or very complex, such as pointing out when a signal is not monotonic. A clock signal with a positive slope, for instance, might go negative for an instant and cause a timing error. By examining the waveform for that net, a designer can analyze and correct the factors that caused the glitch.

## Analog complicates prediction

In analog and mixed-signal component layout, the transmission line effects and parasitics get even harder to predict. Component layout and trace length, width and spacing become even more critical. "Analog designs are difficult because there are so many unknowns and variables," says Shiv C. Tasker, director of product marketing in the printed circuit board division at Valid Logic Systems (Chelmsford, MA). "Stray capacitance, for instance, can be either a bad or good effect. Some designers might put a ground shield under a portion of a circuit because the increased capacitance is desirable. Other times the effects can be detrimental. Designers also want to keep traces short and compact, but they might end up designing a product that's not manufacturable. The disciplines of design, test and manufacturing must be tightly knit when you're dealing with analog circuits."

Though in the past there have been tools that predicted circuit behavior, they were based on theoretical data gleaned from a schematic. "Most timing analysis tools on the market look at schematics and use gate delays between components to try and define the critical paths," says Tasker. "That approach doesn't take into account other elements that affect timing. In addition to gate delay, there's etch delay and settling time, each of which must be taken into account for accurate timing analysis."

Once this timing information is defined, it can be used to set limits on a postlayout simulation before the critical prototype stage. In a circuit where a driver goes from zero to one, for instance, the receiver should be ready after a certain amount of etch delay. But if there isn't sufficient drive, a signal might go halfway and linger before it ramps up. If designers know this ahead of time, they can adjust the circuit to ensure adequate drive—something that is easily done in software but expensive in a postprototype situation.

To solve these high-speed signal delay problems, Valid has unveiled SigDelay, a timing analysis tool that's part of its Allegro printed circuit board design system. SigDelay works directly with Valid's Signal Noise Analysis Tool, which lets users make simultaneous detailed analyses of high-speed board characteristics such as crosstalk, thermal shift, reflections, and ohmic loss. It uses the transmission-line simulation results provided by the Signal Noise Analysis Tool to analyze the speed and smoothness of the signal. SigDelay then verifies length and delay constraints that may have been established on the signal, and uses RapidSim, Valid's high-speed digital simulator, to extract the minimum and maximum pin-to-pin delay data for postlayout timing simulation.

## Placement is key

Tools such as those from Quad Design and Valid are giving designers and layout engineers more data

## *Thermal considerations can no longer be ignored*

The ongoing pursuit of faster, more-reliable and less-expensive electronic products is making thermal performance an increasingly "hot" topic. Efficient board layout techniques can play a role in tackling this problem, producing better products and reducing the need for fans and other supplemental cooling systems. As a result, design teams are adopting two kinds of tools—thermal modeling systems and thermal imaging systems—as effective ways to improve thermal performance.

In pursuit of higher performance, circuits keep getting smaller and faster. Surface-mount technology, fine-pitch geometries and larger scale integration are all attempts to pack more electronic functionality into less space. Unfortunately, faster performance usually generates more heat, and smaller surface areas dissipate less. The result: higher internal operating temperatures.

To the engineer, this is a fundamental problem because heat degrades performance and accelerates the aging process for most components. Heat is often cited as the leading cause of premature failure in electronic products. A common rule of thumb is that a 10° increase in temperature will cut the expected life of a component by one-half. Heat, therefore, becomes a balancing factor in the trade-off between performance and reliability.

### Layout makes a difference

Changing a board's layout may not change the total heat it generates, but it can have a significant impact on peak temperatures of specific devices. Temperature ranges of 50°C or more are not unusual on an operating circuit board. Some components, such as electrolytic capacitors, switches, relays, and active ICs, are more sensitive to heat than others. Putting these components in the cooler zones can increase the reliability of the whole board.

Some layout rules seem obvious, but—in the absence of good thermal data—designers often make simple mistakes such as inadvertently clustering all the hottest components in one small area of the board.

Other improvements are more subtle. Heat does not necessarily dissipate uniformly in all directions. Natural convection, for instance, causes heat to rise toward the top of a vertical board. Just putting the hottest components at the top of a board instead of the bottom can extend its life. And a capacitor next to a hot IC may last longer if it's placed below the IC, rather than above it.

Even ground plane design can be important. A typical copper ground plane makes an efficient conductor for moving heat from the devices out to the board's edges. By dividing the ground plane into segments, the designer can actually control these heat patterns, in effect "directing" heat away from some components.

***Heat is often cited as the leading cause of premature failure in electronic products.***

Another subtlety involves the physical stresses on components and solder joints created when different areas of the board expand at different rates due to temperature differences. Some engineers have found they can reduce these problems by orienting components parallel to rather than across the thermal gradients on the board.

Although all of these changes are simple, they're often overlooked if the designer isn't paying attention to thermal issues. On the other hand, when designers have good information about potential thermal problems, they can often deal with them easily during the layout process.

### Thermal design tools

The key, of course, is having good information. Fortunately, better tools to provide good thermal data are becoming available. Thermal modeling systems are being adopted to generate predictive data so some thermal issues can be dealt with at an early stage in the design process. Thermal imaging systems are being used to improve both the quantity and quality of data about actual thermal performance.

Computerized thermal modeling is a developing technology with potential for great improvement in dealing with thermal problems. An increasing number of these products have been released by established vendors of CAE tools. Some are stand-alone products, but the latest generation is integrated with the electronic design environment. These produce a color display showing the expected thermal performance of a particular design, allowing the user to quickly and interactively test the thermal impact of different layouts.

Although still limited in their functionality and not yet widely used, the quality of thermal modeling systems is improving rapidly. Not only can they improve the designer's efficiency, but they also bring thermal issues into the mainstream of the design process.

### Looking at temperature

Thermal imaging systems use sophisticated infrared scanning techniques to create thermal pictures or temperature maps (thermograms) of operating boards. Although different types of thermal imaging systems vary in their resolution and scanning speeds, all can generate a complete thermogram of an operating circuit board consisting of thousands of data points in less than a minute. Displayed graphically, the data is quickly obtained and easy to interpret visually. This is the only practical way an engineer can be confident there are no hidden thermal flaws in the product.

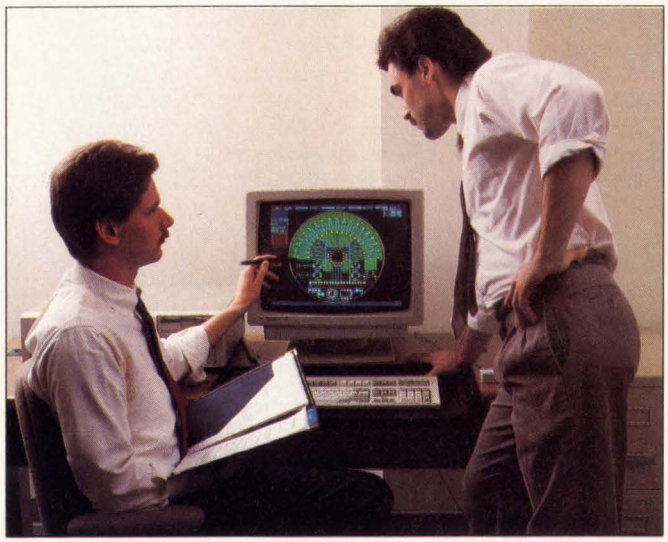
Since this is a noncontact technique, thermal imaging is particularly good for surface-mount technology, fine-pitch, hybrids, and other advanced technology products where thermocouples can be both difficult to use and potentially less accurate. And because the analytical process is so fast, the designer can easily evaluate a wide variety of alternatives without slowing the design process.

The link between product quality and thermal performance is more important than ever before to the electronics industry. Experience has shown that better thermal management can be achieved through intelligent layout decisions based on data from thermal modeling and thermal imaging systems. This not only produces better products, but it also can reduce engineering costs and accelerate development schedules.

**William T. Johnson,** president, Compix

than ever to guide them through a successful component placement. And because it's such an important element, component placement is time-consuming and demands human expertise, in spite of the number of automatic placement tools on the market.

"Component placement can make or break a router, and ultimately the finished product," says Steven Smith, operations manager at Praegitzer Design (Beaverton, OR), a printed circuit board design bureau. "Because of that, you won't find many designers using an autoplacement tool. Good designers can look three or four moves ahead and see the effects of what they're doing. A machine is constrained by some rules, such as trace length, but doesn't have the intuitive sense of a good designer."



*With the advent of high-speed microprocessors and extended memory capabilities, personal computer-based tools are boasting features once reserved for high-priced workstations. The Pads-2000 printed circuit board design suite from CAD Software, for instance, features parts rotation in 0.1-degree increments and supports circuit boards of any shape.*

Most autoplacement tool vendors are quick to point out that the purpose of their products is to provide an interactive environment for the layout engineer and not to serve as an autonomous tool. Autoplacement software can lead the designer through the layout process and relieve the drudgery associated with placing hundreds of components on a board.

"Placement tools are good at deciding what component to place next," says Steve Chidester, product manager at Teradyne EDA (Santa Clara, CA), "but they aren't very good at deciding where the components should go. A couple of hundred components with a rat's nest on the screen can be intimidating, and a designer might wonder where to start. But because the placement tool has connectivity data from the schematic, it can coach the layout engineer on what to place, and the designer can fiddle around with where to put it."

Because automatic placement tools are limited in their capabilities and therefore generally not trusted or used by layout engineers, EDA vendors are turning their attention to improving these tools in the future. But why have improvements been so slow in coming? Most tool vendors cite the more immediate need to improve routing algorithms rather than emphasize placement. Routing, tool vendors say, has been the real bottleneck in printed circuit board design and thus the most appropriate place to put their resources. And though routing tools are still evolving to keep pace with complex designs, most commercially available routers, whether personal computer- or workstation-based, are adequate for the majority of printed circuit board designs. Component placement, especially on highly populated boards, is the next logical step in improving printed circuit board layout tools. But if autoplacement tools are to improve, they will have to get more intelligence designed into their algorithms.

## Considering alternatives

Currently, printed circuit board placement tools work on a limited set of parameters to make decisions on where a component should go. They work on a user-defined grid, which is often much coarser than the grid the router will use, so the placement tool is more limited in its capabilities. These limitations might make the tool too slow, or restrict its ability to rotate parts. In addition, the placement tool makes choices based on parameters such as line length or some user-defined constraints, and then places components. If the tool tries to place a component and the result is favorable according to those guidelines, then the component is placed—if not, the tool tries again.

To overcome these limitations, tool vendors might consider using techniques that ASIC tools use, such as simulated annealing. This technique operates on the assumption that sometimes a decision has to be made that makes things worse before they get better. If the design doesn't improve after a certain amount of degradation, then everything is undone and the tool tries again.

The stumbling block, of course, is that there are more factors to consider when laying out a complex printed circuit board, and if a tool slows to a crawl when faced with intricate decisions, most engineers will jump in and take over. Even if placement tools improve, they will have the same uphill battle that routers faced in the past. "Probably 80 percent of our customers still place by hand," says Matt Whitcomb, Scicards product manager at Harris (Fishers, NY). "It's hard to get an experienced engineer to trust a machine, even if the machine does a good job. It's a cultural as well as technical issue."

Still, EDA vendors know that a tool that promises to free engineers from the drudgery of component placement is popular enough to warrant continued research and development. "It would be nice if an engineer could just floor plan a board and let the tool take it from there," says Keith Felton, technical product marketing manager for CAD products at Racal-Redac (Westford, MA). "If enough design rules were built into an autoplacement tool, then an engineer could just design the printed circuit board with groups of components as subcircuits or functional blocks. The tool would know that components in these blocks must stay together, but aside from that it would intelligently place the components on the board taking into account design rules, parasitic effects and manufacturability."

The amount of factors that such a tool would have to take into account is staggering, a drawback that may

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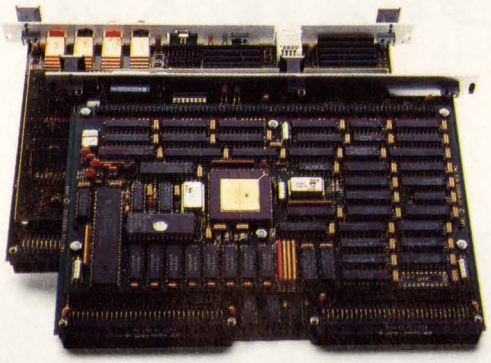

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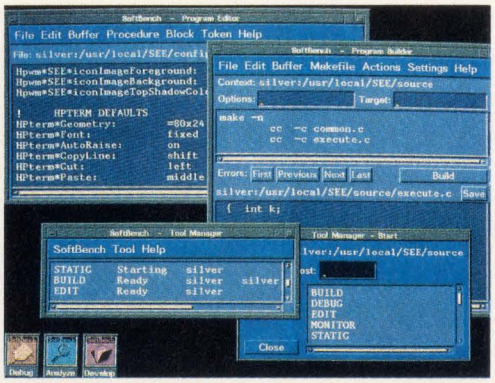


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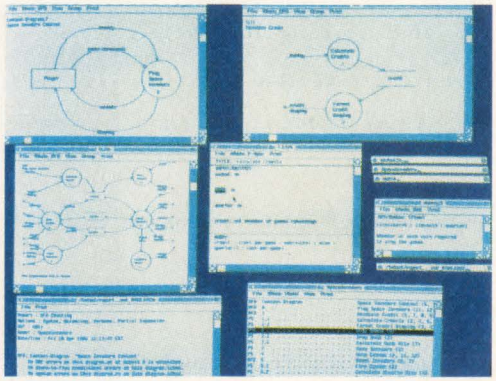

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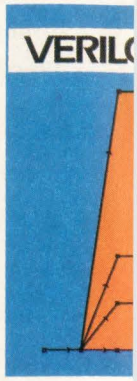


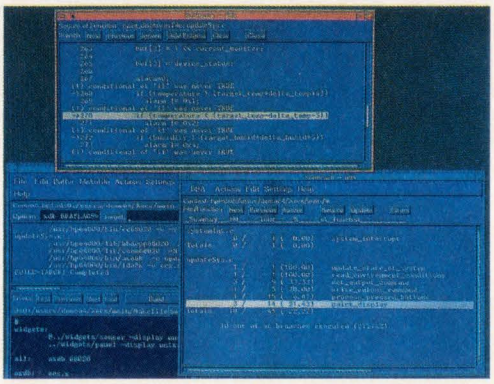

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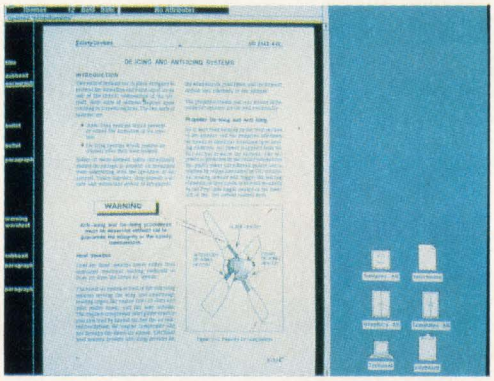

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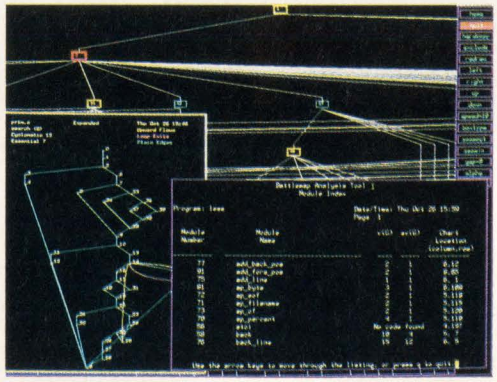

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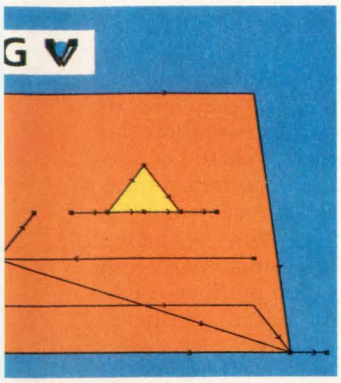

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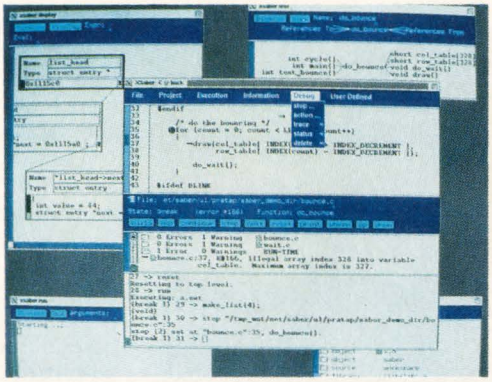

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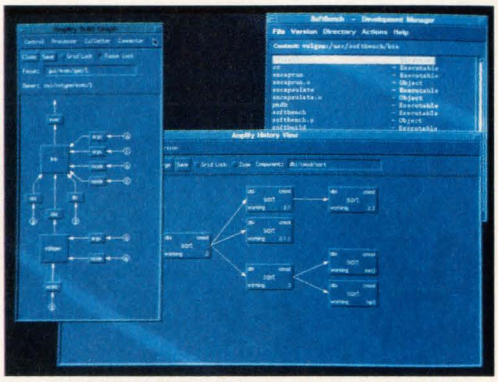

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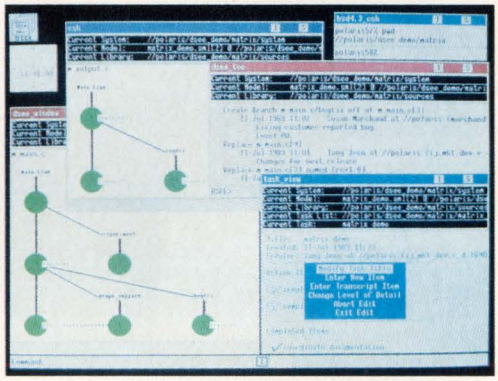

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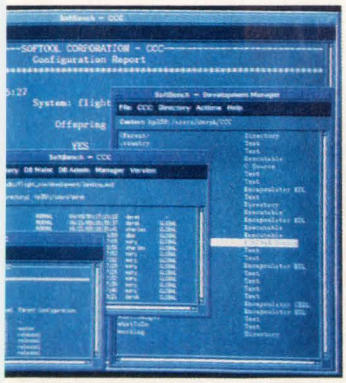

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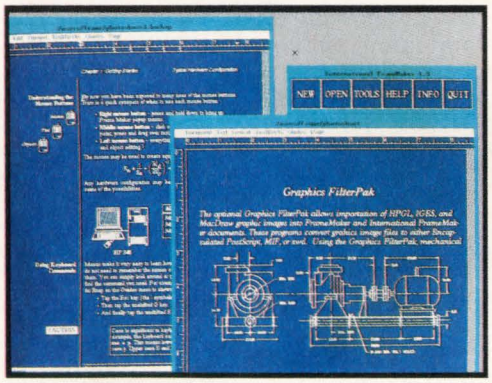


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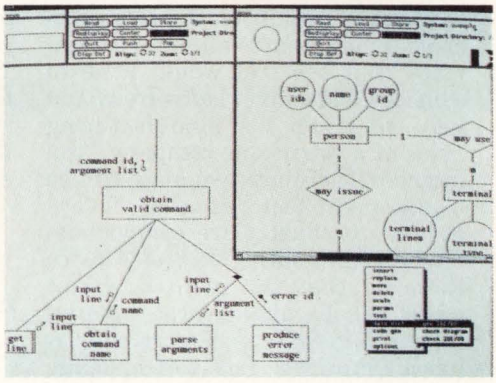


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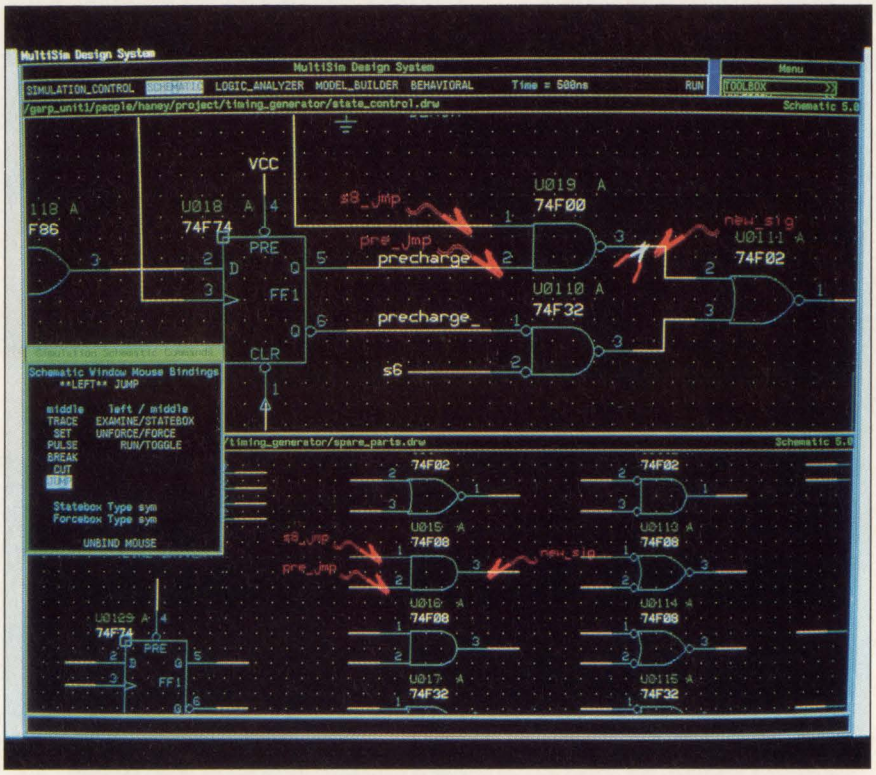


*Teradyne's MultiSim interactive designer uses on-screen icons and mouse-driven controls to let designers modify schematics. In this software cut and jump operation, changes are made to selected circuits, with no need for recompilation and resimulation.*

well keep the ultimate placement tool out of reach for some time to come. In addition to all the electrical rules that the tool would have to consider, placement software would need to grasp the manufacturing rules of a particular company. "Remember, there are two main things a placement tool has to do, " says Felton. "It must place components for efficient routing and also place them so that the printed circuit board can be automatically manufactured. If, for example, a company has an automatic insertion machine on the factory floor that's going to place diodes on the board, they'd want a design that has all or most of the diodes facing the same way. The tool could make exceptions for good reasons, but the end result can't be a printed circuit board that's only 70 percent manufacturable with automated equipment. Hand insertion at the end of the assembly line is expensive."

## Temperature a factor

In addition to all of the aforementioned layout considerations, thermal effects are becoming more critical in tightly packed printed circuit boards. One of the more recently developed tools that design and layout engineers have in their arsenal is thermal analysis capabilities. Traditionally, thermal analysis has been left until after the prototype stage of board development, when thermocouples could be used to assess the thermal behavior of a printed circuit board. Though an experienced designer and a seasoned layout engineer could estimate thermal performance and design the board accordingly, they were hard pressed to outguess the way air would flow across the surfaces of the various components.

***"It's hard to get an experienced engineer to trust a machine, even if it does a good job. It's a cultural as well as technical issue."***

*—Matt Whitcomb, Harris Scientific Calculations*

Thermal analysis tools, which present graphical representations of temperature gradients across the board, have been adopted by most of the major EDA vendors to allow designers to examine "what if" scenarios after initial component placement. The most advanced tools let users define an air flow boundary around a printed circuit board and specify any number of flow inlets (with inlet speeds and air temperatures) and flow outlets. By using potential flow analysis, the tool can determine convection velocity at any point in the enclosure. While most tools come with a library of thermal models for components, thermal rails and heat sinks, they are often dependent on users supplementing these libraries with their own frequently used parts. To do this, however, a user must have accurate thermal data for the part in question, a task that's not always easy.

"The thing we've discovered is that there's not much thermal information on a number of parts," says John Durbetaki, CEO at OrCAD (Hillsboro, OR), a vendor of PC-based EDA tools. "A lot of standard parts have been well documented, but there's not much thermal data on analog parts and the newer components. Information on what kind of plastic is used for packaging and the die size of the device are all important, and it's very hard to get. Modeling airflow is also difficult. At best, these tools give designers a close approximation of a board's thermal behavior. But they shouldn't design too close to the edge of those parameters."

For those printed circuit boards that need accurate real-world evaluation of a board's thermal behavior, there are postprototype thermal imaging systems that capture and store an infrared image of a completed board. Until recently, these systems have been prohibitively expensive, with price tags that ranged from $50,000 to $100,000. But innovations in thermal camera technology have let products such as the model 6000 from Compix come down to below $20,000. Though these systems can only affect layout after a prototype is made, the critical thermal information that they provide can be used to redesign the board before production if unacceptable hot spots are detected on the printed circuit board.

A critical aspect of placement is, of course, its effect on routing of the

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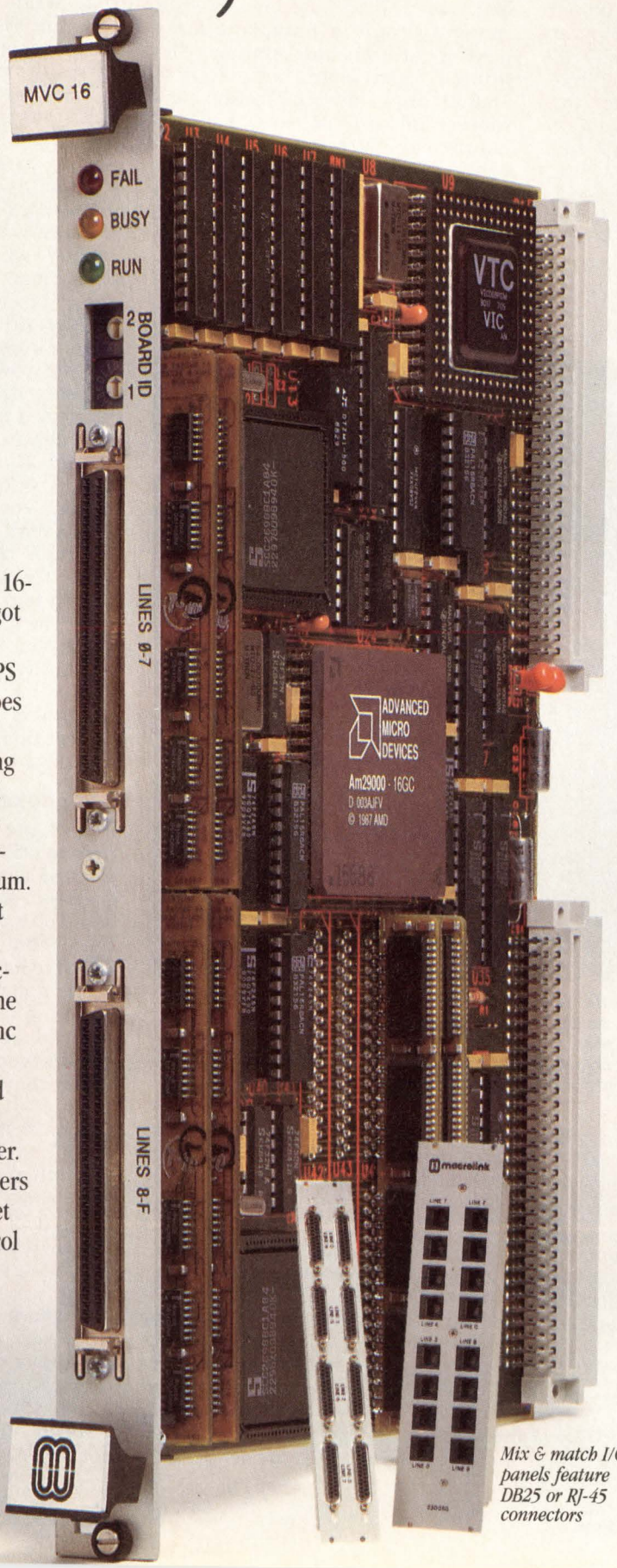


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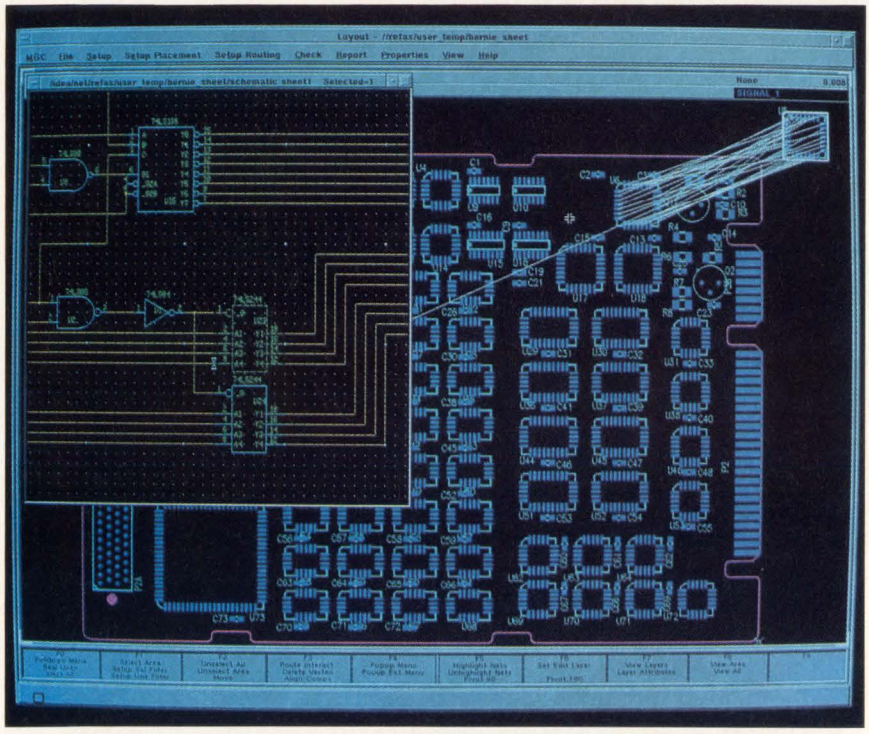
board. Today's autorouters are powerful enough to handle the majority of circuit board designs, and most finish an average design to 100 percent completion. Even though many engineers still prefer to tweak the route for greater efficiency or to reduce layers or vias, the fact that most of the route can be done automatically can shave precious time off design cycles.

Time, however, can be sacrificed if it means saving expensive layers. "The router in our Amadeus Prance product uses several routing strategies to find the most-efficient paths," says Cadence's Perry. "While it's important to show a customer that our product can route a board in 12 hours rather than 20, that's not a big cost saving in the overall design cycle. But if we can do it somewhat faster and save 2 to 4 layers, then that translates into big money. I'm sure that printed circuit board manufacturers are willing to sacrifice a little speed for accuracy, reliability and manufacturability."



*Though automatic placement tools are available, most designers prefer an interactive approach, which combines the power of the computer with a designer's expertise. In this split-screen view of Mentor Graphics' Board Station, a schematic and the associated printed circuit board layout let the user keep track of connectivity requirements to ensure better placement for routing.*

## Choice eases complexity

Because the more advanced routers have a range of algorithms to choose from, depending on the problem at hand, they're finding their way into more-complex design projects. Recently, Data General (Westboro, MA) used Racal-Redac's Visula router to route a backplane for a next-generation workstation. The printed circuit board had a total of 16,000 pin-to-pin connections (or routes) and was 243 in.$^2$ (approximately 15.25×16 in.), with 1,259 equivalent ICs and surface-mount technology components on both sides. The traces were 6-mil line widths, with 6-mil spacings through 6 layers. To get 100 percent completion, the router took approximately 40 hours on the Data General 18-Mips Aviion workstation.

To complete the route, the Visula tool provided a number of "tuning knobs" for each path. This capability lets a user select a routing strategy for each pass. The user can direct the router, for example, to first complete only those pin-to-pin connections that can be made with a straight line. Alternately, the router can be directed to make its connections only within a specified rectangular area, and so forth. A typical strategy, and one that was used on the Data General backplane, would direct the router to make the easy connections in the initial passes and to attempt progressively more difficult connections in each successive pass. While it operates automatically, the Visula router offers a reentrant capability that will report the results of each successive routing pass, and let the user intervene with a new routing strategy.

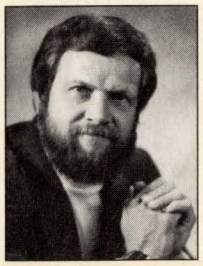
Although routing tools are improving to accommodate challenging designs like the Data General motherboard, most engineers will still intervene at the end, either to complete what the tool couldn't do or to optimize the route to eliminate vias or layers. To meet these needs, EDA vendors are giving their routers interactive capabilities that use the power of the computer to eliminate drudgery, while giving the engineer a free hand to improve the final design. Mentor Graphics' Advanced Dynamic Editor, for instance, offers a sketch mode for manual routing, which lets users draw a path of the trace to be routed. The tool then dynamically completes the trace routing and intelligently moves existing good traces out of the way. For the time being, it seems that most engineers will prefer this type of interactive routing tool, which lets them decide which portions of a board can be left for automation and which areas are best done by hand.

## To grid or not to grid

One of the ongoing debates about routers still centers on gridded versus gridless routers. The makers of gridless routers (which usually are based on a grid, albeit a minute one) claim that their tools are better suited to handle the unusual pin and trace spacings that occur when mixed packages are used on a printed circuit board. "Gridded routers were designed for and work well with printed circuit boards with a lot of ICs of similar sizes and shapes running in nice columns and rows," says Racal-Redac's Felton. "But when you have a complex fine-line design with a mix of pin-pitch components such as metric and imperial, and a lot of variances in track widths, gridded routers get bogged down."

Vendors of gridded routers counter such claims by citing the speed advantages that their routers have over the gridless ones. "So far the gridless technology hasn't beat a gridded router in a fair fight," says Teradyne's Chidester. "It's impor-

## *Adapt your engineering process*



Printed circuit board design and manufacture has traditionally been performed by groups operating relatively independently of one another. Each group in the line has been charged with finding a way to implement the decisions of the previous group, often without an opportunity to influence the design process. In most cases this has worked, even though the designs might not have been completed as rapidly, error free or cost-effectively as they could have been with a well-coordinated effort.

In our capacity as a printed circuit board service bureau, we've seen many internal problems that companies have been forced to face as a direct result of a lack of communication and/or a lack of expertise. Following are some notable examples.

### The process is the problem

In the first case, a major computer manufacturer was confronted with the need to quickly develop a new, higher-performance CPU to maintain a competitive edge. Even though the company owns the most up-to-date simulators and layout tools, six months elapsed after completing the schematic without a successful printed circuit board layout.

The primary reason for this problem was that the design engineers prepared a nonnegotiable design specification requiring routing that couldn't be achieved using any automatic tools. Because the in-house layout group failed to achieve a successful route to specification, the company searched for a highly skilled and cooperative outside layout group. The outside group spent many additional months attempting to route the unroutable design. This is one instance of a practice that could well cost this company its very life, yet the design group refuses to change its methodology.

In a second example, a CAD group within a company functioned independently of both manufacturing and engineering. In order for the company to stay abreast of technology, it had to develop a new product line that included ECL, high-speed TTL, and high pin count pin grid arrays. Moreover, the designs required both timing and coupling control, and the resulting printed circuit boards required 12 layers with 4 power planes.

When the engineering group turned to the CAD group for layout support, it was informed that it would have to redesign the product to fit 4 layers, because that was the capability limit of both the CAD tools and the printed circuit board designers. In order to save the project, the program manager was forced to look outside for layout help. The good news in this case is that the program succeeded in spite of the in-house CAD group. The bad news is that the in-house CAD group was bypassed, lost valuable experience designing complex printed circuit boards and is now gone.

***The problems in these examples could have been avoided if internal communication had been better.***

The last example involved a high-density, high-speed project that was to be an upgrade to an existing installed base of computers. The installed base had edge connectors that required printed circuit boards of 0.062 in. or less in thickness. The upgraded circuit boards were designed using 12 layers, the very least that would hold the wire and distribute the power.

When the printed circuit boards were sent to fabrication, it was learned that the materials available to build them successfully would produce a board of at least 0.085-in. thickness. By the time this was discovered, more than 12 months and uncountable amounts of money had been consumed. The market window was gone and the project was canceled, leaving the computer users with no upgrade path.

### Communication is vital

The problems in each of these examples could have been avoided if internal communication was better and if internal expertise and tools matched the company needs. These two must go hand in hand, because merely providing new tools definitely will not solve any problems.

One popular solution for companies facing these dilemmas is to purchase an integrated system that has the "know how" built in. This system is expected to tie together all the steps in the process as a way to improve the design process—the concurrent engineering approach.

The system, however, isn't likely to improve the overall design process by itself, even if it's truly integrated. The reason is simple: new tools and training are not enough. The only way the problem can be solved is if the organization is correspondingly changed.

Each group within the company must agree to a consistent set of design rules and adhere to them. Equally important, communication lines must stay open. When the overall design process is spread through several independent groups, communication often suffers. Each group must become a part of a team that works together to make the project succeed.

### Groups must cooperate

Even major investments in tools and training can't help unless the groups cooperate. Without cooperation, it's likely that these investments will actually slow the process because the players will be struggling with new tools in addition to their other duties.

In most cases, cooperation requires reorganization, and that means traditional groupings of players must change. Printed circuit board design, for example, must be tightly coupled into the engineering group.

As the first stage, or lead group, in the design process, engineering must take responsibility for understanding and providing for the needs of other groups. The upper levels of engineering must take responsibility for all the operations in the process and develop specifications that are consistent with the capabilities of each.

**Lee W. Ritchey,** BSEE, vice-president of marketing and engineering, Shared Resources

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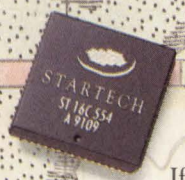


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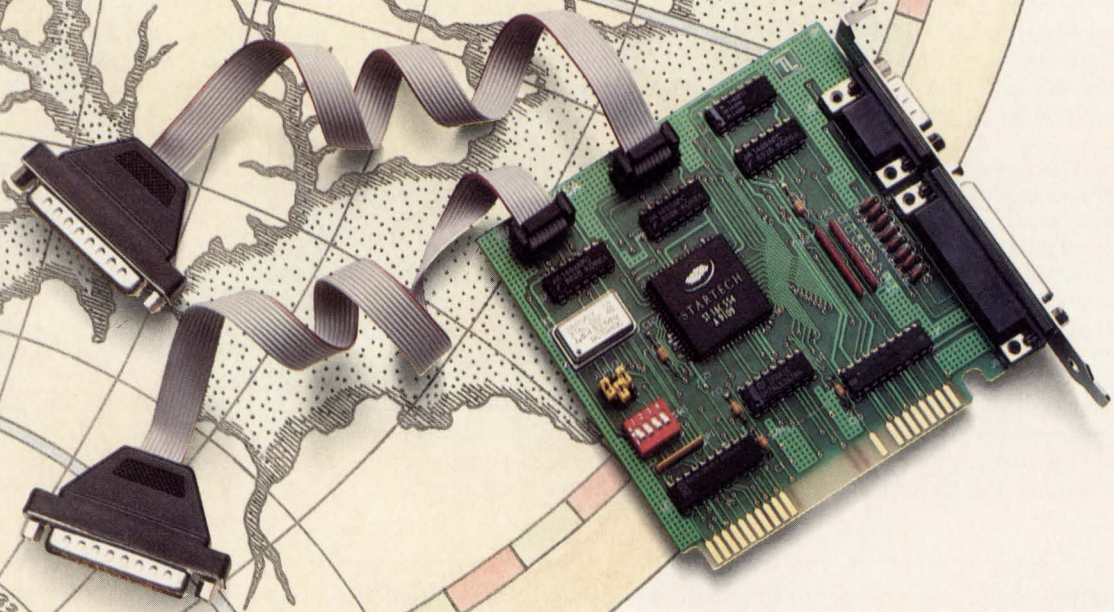

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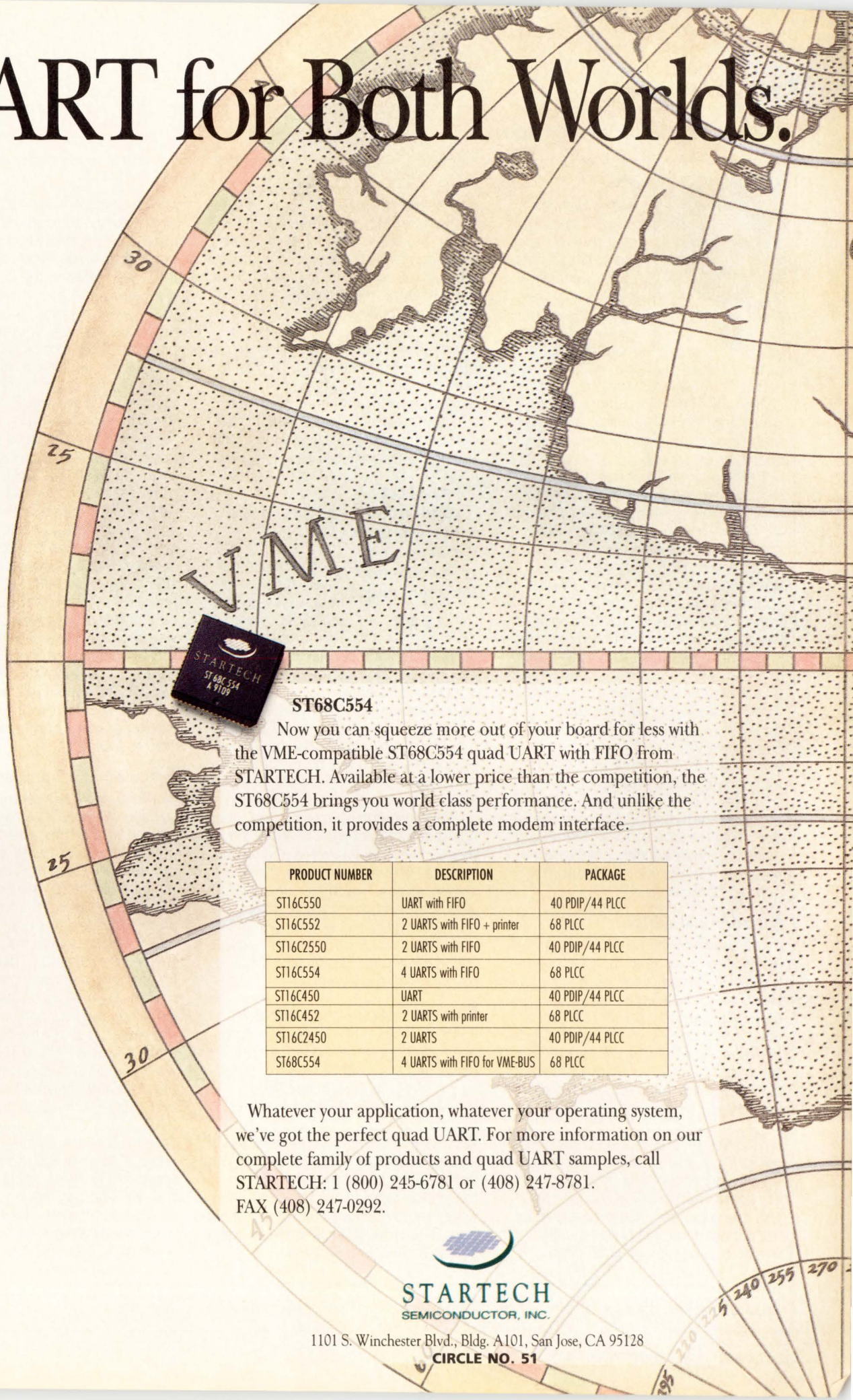


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| ST16C2550 | 2 UARTS with FIFO | 40 PDIP/44 PLCC |
| ST16C554 | 4 UARTS with FIFO | 68 PLCC |
| ST16C450 | UART | 40 PDIP/44 PLCC |
| ST16C452 | 2 UARTS with printer | 68 PLCC |
| ST16C2450 | 2 UARTS | 40 PDIP/44 PLCC |
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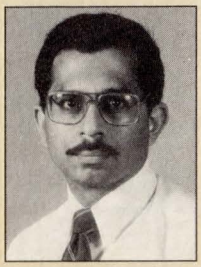
**CIRCLE NO. 51**

# Trends in analog design tools



Curved lines, complex spacing rules, multiple spacings between nets, arbitrary copper shapes, and rules regarding placement make analog board design the toughest challenge for a designer. Added to these considerations are the challenges of manufacturing, testing, packaging, heat dissipation, and a host of other aspects of the printed circuit board layout process.

To the uninitiated, it might appear that analog layout is a far simpler process than layout of a digital board. After all, analog boards usually have fewer components, are generally smaller, have fewer connections, and are typically 1 layer, double sided or 4 layers. Digital boards, on the other hand, have far more components, range from small to very large, can have thousands of connections, use multiple signal layers, and, in the absence of good autorouters, can take a long time to route.

Yet it's analog boards that go through, on average, 10 prototypes compared with 3 to 5 prototypes for digital boards. To complicate matters, most board vendors agree there's a shortage of good analog engineers. The question is whether EDA companies are delivering the kind of tools that analog engineers and designers need to compress the design cycle and reduce the number of prototypes.

## Traditional design

In the traditional design process, a specification stage is followed by a selection of the basic topology of the solution path, which is then detailed in a circuit diagram. At this point, simulation may or may not be used to verify the functional performance of the circuit. In fact, it's common to lay out a circuit and then complete the schematic as a manufacturing/field service document after developing a working board. Breadboards and prototypes are put on a lab bench with the basic premise that either the board won't work and let's figure out why, or the board won't work as required and let's figure out the changes needed. In the digital world, the board usually works, especially if simulated; it just may not work all the time or in all cases.

The reason for this difference in the design process is because of the schematic diagram's inadequacies in fully describing the circuit. (In an analog circuit, the schematic alone does not fully describe the electrical behavior of the circuit.) The schematic diagram, with its emphasis on components and interconnections in the ideal world, ignores implied components such as line inductance, impedance, mutual inductance, and coupled crosstalk. So the engineer doesn't know, except by looking at the layout, where the cross-coupling will occur. It's impossible, therefore, to predict and analyze the condition as part of the simulation process. And every time the layout is even slightly modified, these parasitic parameters and their effects on circuit behavior change. Recognizing the impact of layout on circuit behavior is critical to the development of EDA systems for analog designs.

***Are EDA companies delivering tools that analog engineers and designers need?***

Existing printed circuit board CAD systems focus exclusively on the physical aspects of designs. With the low complexity of most analog circuits, a low-end personal computer-based printed circuit board design package can address most of the core requirements of the analog designer. The next step up is the workstation version, which includes at the very least component placement at any angle, design rule checking for multiple trace widths and spacings, intelligent shape generation and fill, and test and manufacturing checks.

## Prototyping analog designs

Point solutions that focus only on the physical design aspect don't address the issues described earlier that are the major cause of long prototype cycles. While simultaneously creating the best tool for the designer, EDA companies have to look at creating the best design process environment. For analog design, this means that some method has to be found that replaces the high-cost "hardware" prototype loops with "soft" iterations where the impacts of layout are analyzed cheaper and faster.

One of the major reasons why analog engineers spend so much time specifying the layout, verifying that it has been done to their specifications and even doing it themselves is the lack of an easy mechanism to transfer design intent from the front-end to the layout. Rules regarding layout might involve the description of component placement. Placement might be prioritized, for example, by net, as in "keep these connections as short as possible to maximize the signal-to-noise ratio." Or, components might be clustered as a functional group. And groups of components might be placed either close together or as far from each other as possible.

Placement rules must be specified at any level of detail. Once that has been done, if the rules are automatically adhered to in the layout system, the design has a much better chance of being correct. Similar decisions can be made at the interconnect level. At this level design decisions include trace widths for varying voltage levels, spacing checks based on the potential difference between nets, impedance requirements, even minimizing resistance through the increased use of copper on high-voltage connections.

## Analog in a framework

In a framework environment, power dissipation of the various components calculated by the stress analysis can be used as the input for an accurate thermal analysis. Once the case and junction temperatures have been calculated, they can be sent to the simulator for a more accurate stress analysis and to recheck functional performance.

Once the parts have been placed and routed, layout parasitics such as line inductance and mutual capacitance are extracted and included in a postlayout simulation to check the functional performance. Since a 2-pF capacitance between a pair of lines is insignificant in one case and important in another, determining which layout parasitics have to be included in the simulation is a critical problem. And because of the time it takes to do an analog simulation, it's unrealistic to feed each parasitic back into the simulation. A one-hour simulation run compared with a week-long hardware test on a bench is, however, a much more cost-effective alternative.

**Shiv C. Tasker,** director of printed circuit board product marketing, Valid Logic Systems

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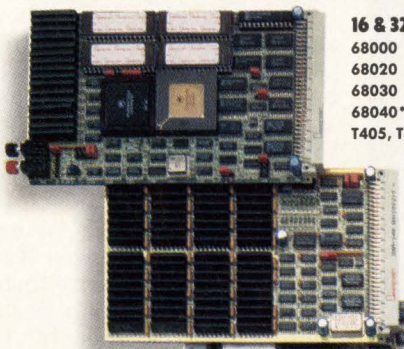

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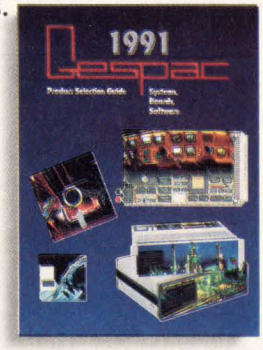


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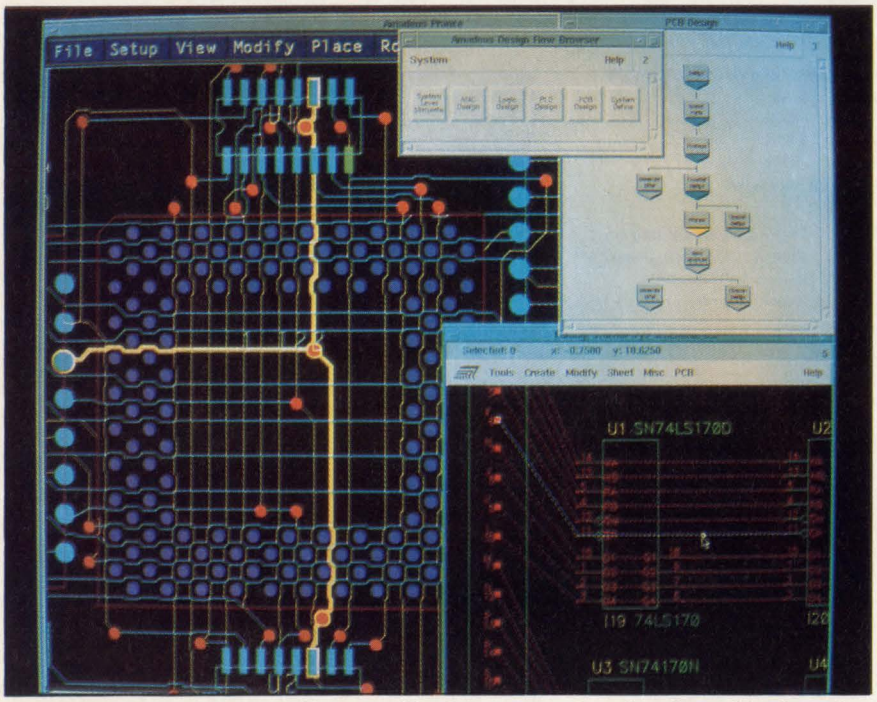


*Framework technology is making possible tight integration of tools. In this view of Amadeus Prance from Cadence Design Systems, cross-probing of a signal in the schematics highlights the associated trace in the board layout. The windows in the upper right display design flow information.*

tant when comparing autorouters to make sure that both tools are working on the same design. Some board designs are more suited for gridless and others for gridded routers. We feel that overall, our router wins more often than not."

Gridded router vendors are also making their tools more flexible by letting them switch to special grids when the design dictates. Almost everyone agrees, however, that as designs shrink, almost all routers of the future will be gridless.

## Power of the PC

Because of the time-saving nature of routers and placement tools, it's no surprise that they're becoming increasingly popular. One of the drawbacks to such tools, however, is that they're expensive and run only on high-priced workstations. Lower-cost PC-based tools have been around for a while but until recently haven't had the ability to handle large designs. In addition, compute-intensive tasks such as routing often slowed PCs to a crawl. But with affordable high-performance microprocessors and extended memory capabilities coming on the market, today's PC-based tools are rivaling the workstations for all but the most-sophisticated printed circuit board designs.

"There are a lot of reasons, besides price, why people are using PC-based tools," says Ray Schnorr, vice-president of marketing at Accel Technologies (San Diego, CA). "The workstation-based tools are great for complex, high-speed designs, but because they have so many features, they're harder to use than PC-based tools. For many designs, an engineer just doesn't need all that power. And because PC-based tools are easier to use, the designer is getting involved in printed circuit board layout."

***"The disciplines of design, test and manufacturing must be tightly knit when you're dealing with analog circuits."***

*—Shiv C. Tasker, Valid Logic Systems*

But while price and ease of use are two reasons why PC-based tools are becoming popular, their advanced feature sets have really fueled their acceptance. Most PC-based tools on the market, for instance, can handle surface-mount technology components as well as large multilayer designs and odd-shaped printed circuit boards. And because many of these tool suites have expanded to wider database structures, they can offer component rotation and greater library support.

The Pads 2000 printed circuit board design suite from CAD Software (Littleton, MA), for example, can access up to 2 Mbytes of memory and handle designs with up to 2,000 ICs. Text and components can be rotated in 0.1-degree increments, and the tool's design-oriented database lets users access any page in the schematic from anywhere in the layout environment.

PC-based tools, such as the Ultiroute from Ultimate Technology, are also offering sophisticated routing features, such as full support of blind and buried vias and rip-up-and-retry to 100 percent completion. With features such as these, even large printed circuit board design houses are turning to PC-based tools for quick turnaround on many designs.

"A lot of customers use our tools rather than wait for system time on one of the large workstations," says Carl Droste, engineering manager at Omation (Richardson, TX). "Why should an engineer wait to get his design in the workstation queue when he can lay it out, simulate it and route it on a PC? With a 33-MHz 386 PC, our tool can get a board design completed in an amount of time that rivals workstation-based tools."

Because the PC-based tools are getting so powerful, many systems houses are using them in an integrated environment, where basic design chores are done on the PC, with the workstations waiting in the wings for more compute-intensive tasks. Tool sets like those from P-CAD let users start a design on a PC and port the files to a larger system further down in the design cycle.

## Integration is key

No matter what the application or environment, one of the key traits that a printed circuit board layout tool suite must have is tight integration of individual tools. Though by itself any EDA tool might help a board designer get the job done, without tight coupling between tools it's easy for users to get lost if they have to leave one environ-

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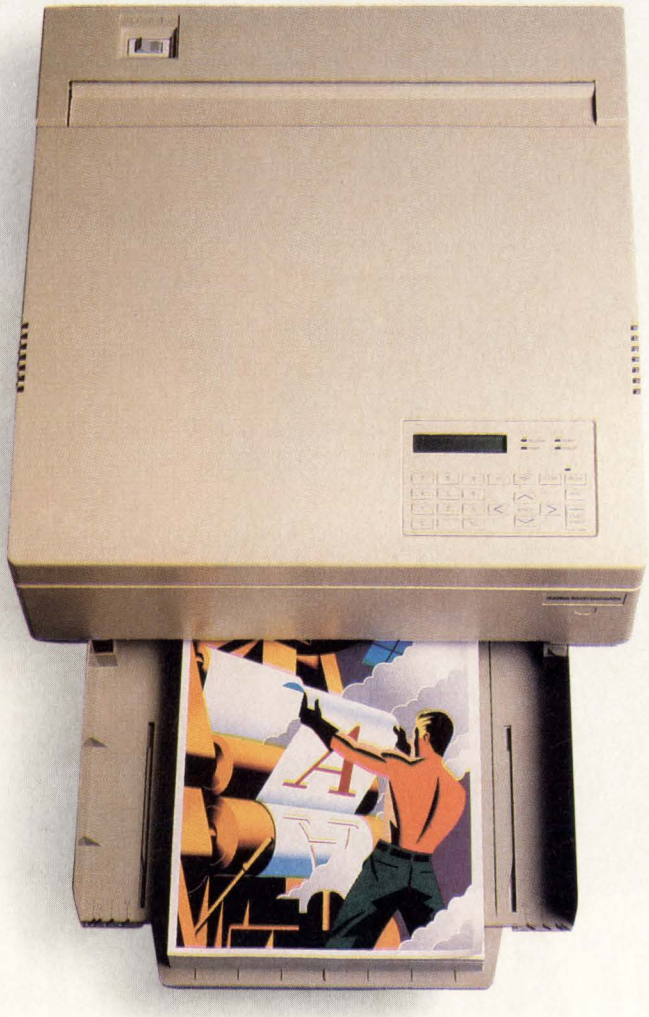

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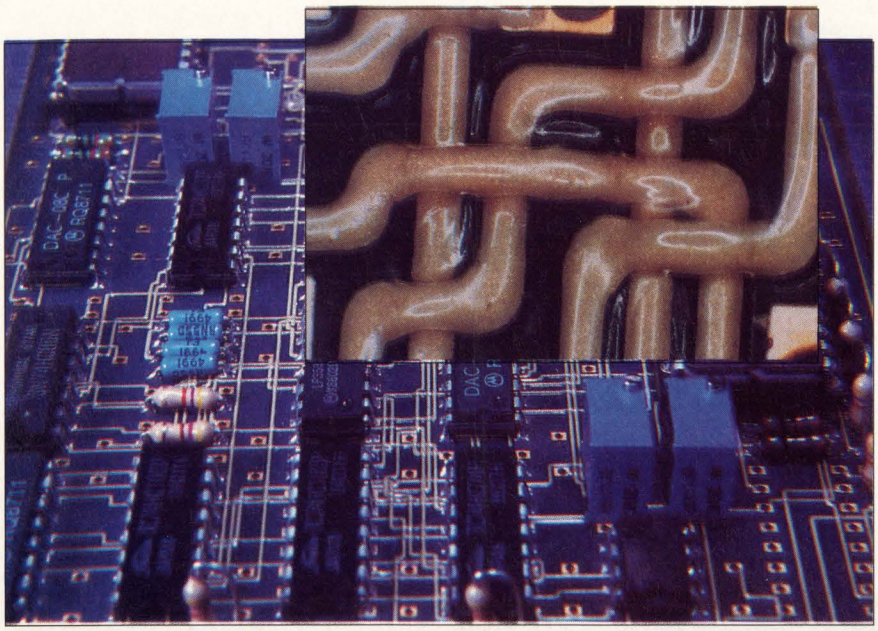

*Fast return of a prototype can shorten a printed circuit board's design cycle by weeks. The CircuitWriter system from Ariel Electronics can produce a prototype from a user's netlist and placement data in one day. Using a proprietary polymer thick-film technology, the system can create circuits equivalent to 6-layer, and even some 8-layer, copper circuit boards. Such densities are possible because the system allows trace crossovers and multiple traces between pads.*

ment to get into another. EDA vendors, therefore, have spent considerable time and money ensuring that a user can move easily between schematic and component layout, as well as libraries, to examine alternative packages or modify existing parts.

Most of the workstation-based products use frameworks as a means to achieve this end, and at least one PC-based tool set from OrCAD boasts a framework backbone for its design suite. Other PC-based tools simply rely on expanded databases to ensure some form of integration. "One of the true tests of integration is cross-probing," says Cadence's Perry. "If a user can point to a signal or component in a schematic and highlight the associated device in the layout, then that's a sign of real integration. This kind of integration allows forward and back annotation of design changes and simulation results, and ensures that all members of a design team can get their hands on the latest version of a design."

## Eliminating prototype iterations

All of the tools mentioned so far have one thing in common: Their purpose is to give both design and layout engineers a better shot at producing a working, manufacturable prototype. Unfortunately, the traditional methods of prototyping (wire wrap, for example) have been made obsolete by high-speed, controlled-impedance designs requiring multilayer boards and surface-mount components. Engineers are reluctantly turning to the full printed circuit board fabrication process to achieve their first design verification. Doing this, however, either freezes the design process while everyone waits for the prototype, or makes the prototype obsolete before it returns (if enhancements are made to the design while the printed circuit board is being made). Some innovative technologies hold promise that help is on the way.

The CircuitWriter from Ariel Electronics (Sunnyvale, CA) is a system that fabricates a fully functional circuit board directly from a user's design generally in less than one day, by extruding polymer thick-film (PTF) traces for the prototype. The system, which is in beta test now, can produce boards that would require up to 6 and, under certain conditions, even 8 signal layers on a conventional multilayer copper board. Prototypes are made on base panels—either standard copper etch or custom drilled—directly from the circuit design data. The system then extrudes PTF directly on the base panel to create the desired circuits. First, a conductive PTF is extruded between the base panel's prefabricated copper pads. Then a nonconductive PTF insulating layer is extruded to overcoat the conductor. The combined extrusions create a total physical trace height of about 8 mil. The CircuitWriter can produce boards up to 12×16 in.

According to Ariel, the transmission impedance and transmission speeds of the trace material are within 10 percent of copper traces under the same conditions, and measured performance at 50 MHz in a PTF circuit is the same as a comparable copper circuit.

With capabilities like those from Ariel on the horizon, printed circuit board designers will have more tools than ever at their fingertips to reduce time-to-market and to lower costs. And as printed circuit board layout tools get more sophisticated, even more information will be brought to the front end of the design cycle. It's unlikely, however, that the time is near when human expertise isn't needed.

"Humans have a wonderful sense of what looks good in a design," says OrCAD's Durbetaki. "And if a design looks good and clean, chances are that it will work better, too. So even though today's placers and routers are quite good, for the time being at least, an experienced person can always do better." ■

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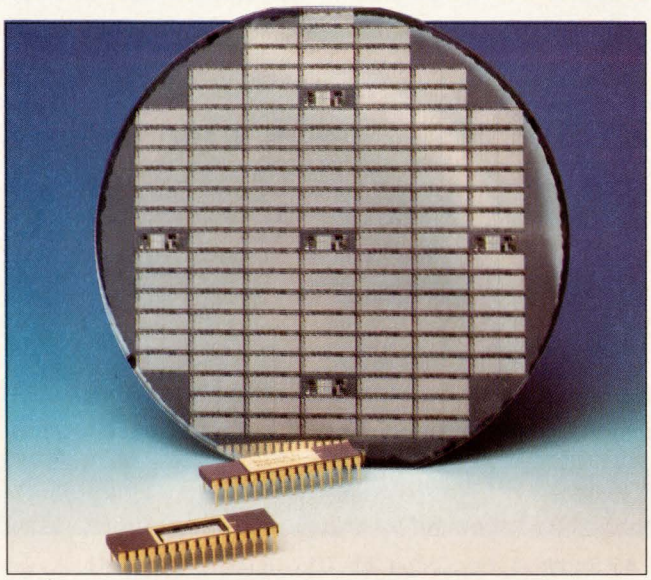
# 256-kbit SRAMs provide many choices, while 1-Mbit chips gain speed

Jeffrey Child, Associate Editor



*Built with a proprietary dual-well 0.8-μm CMOS technology, a 128k×8-bit SRAM from Paradigm Technology offers access speeds down to 20 ns. The company uses a self-aligned process that's designed to eliminate empty space in the cell, enhancing density and speed.*

As long as microprocessor cycle times continue to outpace the access speeds of DRAM-based main memory, computers will need cache memory to achieve optimum performance. Running at 33 MHz and higher, with cycle times of 30 ns and less, today's high-performance processors must operate with banks of zero-wait-state memory if they are to deliver top performance. With access times far below those of the fastest DRAMs, SRAMs continue to be the mainstay of cache designs and are keeping pace with the progress in processors by steadily increasing in speed and density.

To meet the speeds of today's lightning-fast microprocessors, SRAM designers are constantly refining their process technologies. Most SRAM vendors envision a day when BiCMOS will become mandatory for high speed, and some have upgraded to BiCMOS. Other vendors have been squeezing an astonishing amount of speed from existing CMOS processes—256-kbit CMOS parts have dropped below 15 ns.

The basic challenge faced by SRAM designers is getting high-density devices to meet these ever-increasing speeds. As prices fall, 1-Mbit SRAMs have climbed to useful speed levels, but not enough to encroach on the 256-kbit SRAM's market share in cache memory, the primary application for fast SRAMs. The best combination of speed and density is still found in 256-kbit SRAMs. These chips, unlike 1-Mbit SRAMs, offer a broad range of memory configurations and speed choices, though fast 1-Mbit SRAMs are being used as secondary cache in some designs.

## Cache design critical

In the fast-growing personal computer market, designers are finding that their choices in cache designs are important competitive decisions. The cache configuration must be large enough to offer added performance, but the amount of SRAM used must be small enough to accommodate the tight cost constraints of PC systems.

"Most secondary caches don't need to be much more than 128 kbits deep," says Robert Tabone, tactical marketing manager for SRAMs at Hitachi America (Brisbane, CA). At the speeds currently available, the most useful factor a 1-Mbit SRAM offers is its width. Wider devices can reduce both the parts count and the cost of small SRAM arrays.

"For a 32-bit machine, you could use eight 256k×4-bit parts to make your secondary cache," Tabone says. "But 256 kbits is more depth than is required for most cache designs. With a 128k×8-bit SRAM, you could offer a more-reasonable depth and use only four parts." To the dismay of cost-sensitive designers, however, few vendors supply 128k×8-bit SRAMs.

A 32k×32-bit high-speed SRAM would be ideal as a single-device, 32-bit cache for small computer systems. It would be difficult to create, though, because of the noise that can inhibit speed in such a wide memory organization on a single chip.

Another factor driving the demand for fast, high-density SRAMs is the growing interest in RISC and digital signal processing systems. A RISC processor's pipelined structure and higher instruction bandwidth require a substantial cache. In a DSP system, where one program is run all the time, it makes sense for that program's code to be stored in fast SRAM. This focus on memory architecture has let system designers differentiate their designs on more than just raw CPU speed. "There's a lot of elegance that you can lend to a design with a good caching scheme and the way you control your instruction flow," says Tabone.

## CMOS or BiCMOS?

As the accompanying tables indicate, most SRAM vendors are staying with CMOS for now, although a handful have switched to BiCMOS. Hitachi is one vendor that switched, and the company's products include a 20-ns 256k×4-bit SRAM. The device comes in a 32-pin separate I/O package or a 28-pin common I/O package.

Despite industry predictions that the next jump in SRAM speed would require switching from CMOS to BiCMOS, many manufacturers have been successful in squeezing more performance from their existing CMOS processes. Paradigm Tech-

| Model | Organization (bits) | Access time (min/max ns) | Process | Power dissipation (active/inactive in mW) | Supply voltage | Package | Availability | Price | Comments |
|---|---|---|---|---|---|---|---|---|---|
| **AT&T Microelectronics** Two Oak Way, Berkeley Heights, NJ 07922 (800) 372-2447 | | | | | | | | | **Circle 301** |
| ATT7C196 | 64k×4 | 15/25 | CMOS | 500 | 5 | DIP, SOJ | now | $46 | common I/O, output-enable pin, 2 chip-enable pins |
| ATT7C191/192 | 64k×4 | 15/25 | CMOS | 500 | 5 | DIP, SOJ | now | $46 | separate I/O, transparent write |
| ATT7C194/195 | 64k×4 | 15/25 | CMOS | 500 | 5 | DIP, SOJ | now | $46 | output-enable version available, common I/O |
| ATT7C197 | 256k×1 | 12/25 | CMOS | 500 | 5 | DIP, SOJ | now | $46 | separate I/O |
| ATT7C199 | 32k×8 | 15/25 | CMOS | 700 | 5 | DIP, SOJ | now | $46 | common I/O |
| **Cypress Semiconductor** 3901 N First St, San Jose, CA 95134 (408) 943-2600 | | | | | | | | | **Circle 302** |
| CY7C157 | 16k×16 | 20/33 | CMOS | 1,250 | 5 | LCC, PLCC | now | $156 | for glueless cache in Cypress Sparc systems |
| **Electronic Designs** 42 South St, Hopkinton, MA 01748 (508) 435-2341 | | | | | | | | | **Circle 303** |
| EDI88128CS | 128k×8 | 25/45 | CMOS | 1,000 | 5 | SOJ | 4-6 weeks | $74 | 1 chip-enable pin |
| EDI84256CS/8CS | 256k×4 | 25/45 | CMOS | 1,000 | 5 | SOJ | 4-6 weeks | — | common or separate I/O |
| EDI811024CS | 1M×1 | 15/35 | CMOS | 1,000 | 5 | DIP, SOJ | 4-6 weeks | — | — |
| EDI8832CA | 32k×8 | 15/25 | CMOS | 1,000 | 5 | DIP, SOJ | 3Q91 | $20 | — |
| EDI8465CA | 64k×4 | 15/25 | CMOS | 1,000 | 5 | DIP, SOJ | 3Q91 | $12 | — |
| EDI81257CA | 256k×1 | 15/25 | CMOS | 1,000 | 5 | DIP, SOJ | 3Q91 | $14 | — |
| **Fujitsu Microelectronics, IC Division** 3545 N First St, San Jose, CA 95134 (800) 642-7616 | | | | | | | | | **Circle 304** |
| MB82B001 | 1M×1 | 25/35 | BiCMOS | 660/138 | 5 | SOJ | 4Q91 | — | — |
| MB82B005/6 | 256k×4 | 25/35 | BiCMOS | 660/138 | 5 | SOJ | 4Q91 | — | output enable, separate I/O |
| MB82B88/9 | 32k×8<br>32k×9 | 15/20 | BiCMOS | 715/83 | 5 | DIP, SOJ | 4Q91 | — | output enable |
| MB82B81 | 256k×1 | 15/20 | BiCMOS | 660/82.5 | 5 | DIP, SOJ | 2Q91 | — | — |
| MB82B84/5 | 64k×4 | 15/20 | BiCMOS | 660/82.5 | 5 | DIP, SOJ | 2Q91 | — | output-enable version available |
| MBM101C500-15 | 256k×1 | 15 | BiCMOS | 1,040 | 5.2 | flatpack | now | $46.25 | ECL I/O |
| MBM101C504-15 | 64k×4 | 15 | BiCMOS | 1,300 | 5.2 | DIP, flatpack | 2Q91 | — | same as above |
| MBM101C510-15 | 1M×1 | 15 | BiCMOS | — | 5.2 | DIP, flatpack | 3Q91 | — | same as above |
| MBM100C514 | 256k×4 | 15 | BiCMOS | — | 4.5 | DIP, flatpack | 4Q91 | — | same as above |
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| HM6707A | 256k×1 | 15/20 | BiCMOS | 350/50 | 5 | DIP, SOJ | now | $18 to $32 | — |
| HM6708A | 64k×4 | 15/20 | BiCMOS | 350/50 | 5 | DIP, SOJ | now | $18 to $32 | — |
| HM6709A | 64k×4 | 15/20 | BiCMOS | 350/50 | 5 | DIP, SOJ | now | $18 to $32 | output-enable version available |
| HM624256A/7A | 256k×4 | 20/25/35 | BiCMOS | 350/0.1 | 5 | DIP, SOJ | now | $85 to $150 | low-power versions available |
| HM62832H/UH | 32k×8 | 15/25/35 | CMOS | 400/0.2 | 5 | DIP, SOJ | now | $10.75 | same as above |
| HM621100A | 1M×1 | 20/25/35 | CMOS | 350/0.01 | 5 | DIP, SOJ | now | $76 | same as above |
| **Integrated Device Technology** 1566 Moffett St, Salinas, CA 93905 (408) 424-7726 | | | | | | | | | **Circle 306** |
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| IDT71B259 | 32k×9 | 12/20 | BiCMOS | 350/— | 5 | DIP, SOJ | now | $65 | — |

| Model | Organization (bits) | Access time (min/max ns) | Process | Power dissipation (active/inactive in mW) | Supply voltage | Package | Availability | Price | Comments |
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| IDT71258 | 64k×4 | 20/25 | CMOS | 350/0.1 | 5 | DIP, flatpack, LCC, SOIC, SOJ | 3Q91 | — | chip-select pins |
| IDT71B258 | 64k×4 | 12/20 | BiCMOS | 450/— | 5 | DIP, flatpack, LCC, SOIC, SOJ | 2Q91 | — | same as above |
| IDT61298 | 64k×4 | 20/25 | CMOS | 350/0.1 | 5 | DIP, SOJ | 3Q91 | $56 | output-enable and chip-select pins |
| IDT61B298 | 64k×4 | 12/20 | BiCMOS | 450/— | 5 | DIP, SOJ | now | $56 | same as above |
| IDT71256 | 32k×8 | 20/25 | CMOS | 350/0.015 | 5 | DIP, flatpack, LCC, SOIC | now | $14.65 | same as above |
| IDT71B256 | 32k×8 | 15/20 | BiCMOS | 450/— | 5 | DIP, flatpack, LCC, SOIC | now | $14.65 | same as above |
| IDT71024 | 128k×8 | 25/30 | CMOS | 500/0.2 | 5 | DIP | 4Q91 | — | output enable, 2 chip-select pins |
| IDT71B024 | 128k×8 | 15/20 | BiCMOS | 500/— | 5 | DIP | 3Q91 | — | same as above |
| IDT71028 | 256k×4 | 25/30 | CMOS | 500/0.2 | 5 | DIP | 4Q91 | — | output-enable and chip-select pins |
| IDT71B028 | 256k×4 | 15/20 | BiCMOS | 500/— | 5 | DIP | 3Q91 | — | same as above |
| **Logic Devices** 628 E Evelyn Ave, Sunnyvale, CA 94086 (408) 720-8630 | | | | | | | | | **Circle 307** |
| L7C197 | 256k×1 | 12/15 | CMOS | 210/100 | 5 | DIP, LCC, SOIC, SOJ | now | — | — |
| L7C191/2 L7C194/5/6 | 64k×4 | 15/20 | CMOS | 265/100 | 5 | DIP, SOIC, SOJ | now | — | — |
| L7C199 | 32k×8 | 15/20 | CMOS | 380/100 | 5 | DIP, LCC, SOIC, SOJ | now | — | — |
| **Micron Technology** 2805 E Columbia Rd, Boise, ID 83706 (208) 368-3900 | | | | | | | | | **Circle 308** |
| MT5C2561 | 256k×1 | 15/20/25 | CMOS | 580/140 | 5 | DIP, SOJ | now | $15 | — |
| MT5C2564/5 | 64k×4 | 15/20/25 | CMOS | 580/140 | 5 | DIP, SOJ | now | $15 | output-enable version available |
| MT5C2568 | 32k×8 | 20/25/35 | CMOS | 580/140 | 5 | DIP, SOJ | now | $15 | — |
| MT5C1001 | 1M×1 | 20/25/35 | CMOS | 660/140 | 5 | DIP, SOJ | now | — | — |
| MT5C1005 | 256k×4 | 20/25/35 | CMOS | 660/140 | 5 | DIP, SOJ | now | — | — |
| MT51008 | 128k×8 | 20/25/35 | CMOS | 660/140 | 5 | DIP, SOJ | now | — | — |
| **Mitsubishi Electronics America** 1050 E Arques Ave, Sunnyvale, CA 94086 (408) 730-5900 | | | | | | | | | **Circle 309** |
| M5M5257B/8B | 256k×1 64k×4 | 15/20 | CMOS | 120/30 | 5 | DIP, SOJ | June '91 | $21 to $25 | — |
| M5M5278/9 | 32k×8 32k×9 | 15/20/25 | CMOS | 300/1 | 5 | DIP, SOJ | June '91 | $17 to $25 | — |
| M5M51001 | 1M×1 256k×4 | 25/35/45 | CMOS | 100/20 | 5 | DIP, SOJ | 35-ns, 45-ns now | $55 to $85 | configurable organization |
| M5M51004/14 | 256k×4 | 25/35/45 | CMOS | 100/20 | 5 | DIP, SOJ | 35-ns, 45-ns now | $55 to $85 | separate I/O version available |
| **Mosaic Semiconductor** 7420 Carroll Rd, San Diego, CA 92121 (619) 271-4565 | | | | | | | | | **Circle 310** |
| MSM11000 | 1M×1 | 35/45/55 | CMOS | 600/0.5 | 4.5 to 5.5 | DIP, flatpack, LCC | — | $295 | vertical inline package available |
| MSM8128 | 128k×8 | 45/55/70 | CMOS | 150/0.05 | 4.5 to 5.5 | DIP, flatpack | — | $210 | same as above |
| MSM4256 | 256k×4 | 45/55/70 | CMOS | 350/0.01 | 4.5 to 5.5 | DIP, flatpack, LCC | — | $245 | same as above |

| Model | Organization (bits) | Access time (min/max ns) | Process | Power dissipation (active/inactive in mW) | Supply voltage | Package | Availability | Price | Comments |
|---|---|---|---|---|---|---|---|---|---|
| **Mosel** 914 W Maude Ave, Sunnyvale, CA 94086 (408) 733-4556 | | | | | | | | | **Circle 311** |
| MS621002 | 256k×4 | 20/25/35 | CMOS | 500/0.5 | 5 | SOJ | now | $78 | — |
| MS621008 | 128k×8 | 20/25/35 | CMOS | 600/0.5 | 5 | SOJ | now | $84.50 | — |
| **Motorola** 3501 Ed Bluestein Blvd, Austin, TX 78721 (512) 928-6000 | | | | | | | | | **Circle 312** |
| MCM6207 | 256k×1 | 15/20 | CMOS | 750 | 5 | DIP, SOJ | now | $30 | — |
| MCM62982 | 64k×4 | 12/15 | CMOS | 850 | 5 | SOJ | now | $44 to $64 | — |
| MCM62940 MCM62486 | 32k×9 | 14/19 | CMOS | 900 | 5 | PLCC | now | $41 to $63 | burst mode for 68040 or i486 |
| MCM62990 | 16k×16 | 17/20 | CMOS | 1,800 | 5 | PLCC | now | $35 to $40 | — |
| MCM62995 | 16k×16 | 17/20 | CMOS | 1,800 | 5 | PLCC | now | $32 to $40 | internal address/data latches |
| MCM62980 | 64k×4 | 15/20 | CMOS | 850 | 5 | SOJ | now | $33 to $41 | internal registers on address bus |
| MCM62950/60 MCM62110 | 32k×9 | 15/17/20 | CMOS | 875/1,250 | 5 | PLCC | now | $30 to $66 | processor-specific versions available |
| MCM6205/6 | 32k×8 32k×9 | 12/15/17/20 | CMOS | 775/— | 5 | DIP, SOJ | now | $17 to $42 | — |
| MCM6208 | 64k×4 | 15/20 | CMOS | 775 | 5 | DIP, SOJ | now | $40 | 12-ns available 2Q91 |
| MCM6226 | 128k×8 | 25/30 | CMOS | 750 | 5 | SOJ | now | $77 | — |
| MCM6228 | 256k×4 | 25/30 | CMOS | 725 | 5 | SOJ | now | $75 | — |
| **Panasonic Industrial, Semiconductor Division** 1616 McCandless Dr, Milpitas, CA 95036 (408) 946-4311 | | | | | | | | | **Circle 313** |
| MN441008 | 128k×8 | 35 | CMOS | 770/0.55 | 5 | DIP, SOJ | now | $60 | — |
| MN441004 | 256k×4 | 35 | CMOS | 770/0.55 | 5 | DIP, SOJ | May '91 | $60 | — |
| MN441001 | 1M×1 | 35 | CMOS | 770/0.55 | 5 | DIP, SOJ | May '91 | $60 | — |
| MN44251 | 32k×8 | 20 | CMOS | 660/0.55 | 5 | DIP, SOJ | now | $20 | — |
| MN44252 | 64k×4 | 20 | CMOS | 660/0.55 | 5 | DIP, SOJ | now | $20 | — |
| MN44251 | 256k×1 | 20 | CMOS | 660/0.55 | 5 | DIP, SOJ | now | $20 | — |
| **Paradigm Technology** 71 Vista Montana, San Jose, CA 95134 (408) 954-0500 | | | | | | | | | **Circle 314** |
| PDM41257 | 256k×1 | 12/45 | CMOS | 400/350 | 5 | DIP, LCC, SOJ | now | $16.48 | — |
| PDM41258/98 PDM41251/52 | 64k×4 | 12/45 | CMOS | 400/350 | 5 | DIP, LCC, SOJ | now | $14 to $17 | available with output-enable pin |
| PDM51256 | 32k×8 | 12/45 | CMOS | 400/350 | 5 | DIP, LCC, SOJ | now | $16.48 | — |
| PDM41027 | 1M×1 | 20/25/35 | CMOS | 400/350 | 5 | DIP, SOJ | now | $127.16 | — |
| PDM41028/22 | 256k×4 | 20/25/35 | CMOS | 400/350 | 5 | DIP, SOJ | now | $127.16 | available in separate I/O and with output enable |
| PDM41024 | 128k×8 | 20/25/35 | CMOS | 400/350 | 5 | cerpack, DIP, LCC, SOJ | now | $127.16 | — |
| **Performance Semiconductor** 610 E Weddell Dr, Sunnyvale, CA 94089 (408) 734-8200 | | | | | | | | | **Circle 315** |
| P4C1256 | 32k×8 | 20 | CMOS | — | 5 | DIP, LCC, SOJ | 2Q91 | — | — |
| P4C1258/98 | 64k×4 | 20 | CMOS | — | 5 | DIP, LCC, SOJ | 2Q91 | — | output-enable version available |
| P4C1257 | 256k×1 | 20 | CMOS | — | 5 | DIP, SOJ | 2Q91 | — | — |

| Model | Organization (bits) | Access time (min/max ns) | Process | Power dissipation (active/inactive in mW) | Supply voltage | Package | Availability | Price | Comments |
|---|---|---|---|---|---|---|---|---|---|
| **Sharp Electronics** 5700 NW Pacific Rim Blvd, Camus, WA 98607 (206) 834-8700 | | | | | | | | | **Circle 316** |
| LH521008 | 128k×8 | 25/35 | CMOS | 700/5 | 5 | SOJ | now | — | no-connect on pin 32, per JEDEC |
| LH521002 | 256k×4 | 25/35 | CMOS | 600/5 | 5 | SOJ | now | — | — |
| LH52253 | 64k×4 | 20 | CMOS | 600/5 | 5 | SOJ | now | — | output enable |
| **Silicon Connections** 16868 Via Del Campo Ct, San Diego, CA 92127 (619) 674-1050 | | | | | | | | | **Circle 317** |
| SC5100 | 256k×1 | 12/15 | BiCMOS | 1,100 | 5.2 | flatpack | now | $60 | — |
| SC5104 | 64k×4 | 12/15 | BiCMOS | 1,100 | 5.2 | flatpack | now | $75 | 8-ns 2Q91 |
| SC5200 | 1M×1 | 8/10 | BiCMOS | 1,400 | 5.2 | flatpack | 3Q91 | $255 | — |
| SC5204 | 256k×4 | 8/10 | BiCMOS | 1,600 | 5.2 | flatpack | 3Q91 | $330 | — |
| **Sony Component Products** 10833 Valley View St, Cypress, CA 90630 (714) 229-4197 | | | | | | | | | **Circle 318** |
| CXK58258A/B | 32k×8 | 15/20/25/35 | CMOS | 770/11 | 5 | DIP, SOJ, SOP | 3Q91 | — | — |
| CXK59288 | 32k×9 | 15/20 | CMOS | 500/425 | 5 | DIP, SOJ | 2Q91 | — | — |
| CXK581020 | 128k×8 | 35/45 | CMOS | 660/11 | 5 | DIP, SOJ | now | $116 to $150 | — |
| CXK541000 | 256k×4 | 25/30/35 | CMOS | 660/11 | 5 | SOJ | 3Q91 | — | — |
| **Toshiba America Electronic Components** 9775 Toledo Way, Irvine, CA 92718 (714) 455-2000 | | | | | | | | | **Circle 319** |
| TC55328 | 32k×8 | 17/35 | CMOS | — | 5 | DIP, SOJ | now | $20 | output enable |
| TC55329 | 32k×9 | 17/35 | CMOS | — | 5 | DIP, SOJ | now | $22 | same as above |
| TC55464 | 64k×4 | 17/35 | CMOS | — | 5 | DIP, SOJ | now | $14 | — |
| TC55465 | 64k×4 | 17/35 | CMOS | — | 5 | DIP, SOJ | now | $19 | output enable |
| TC551664 | 64k×16 | 15/25 | CMOS | — | 5 | SOJ | 3Q91 | $200 | — |
| **United Microelectronics** 3350 Scott Blvd, #48-49, Santa Clara, CA 95054 (408) 727-9239 | | | | | | | | | **Circle 320** |
| UM61256 | 32k×8 | 20/25 | CMOS | 600/25 | 5 | DIP, SOJ | 2Q91 | $17 | — |
| UM61257 | 32k×9 | 20/25 | CMOS | 600/25 | 5 | DIP, SOJ | 3Q91 | $20 | — |
| UM61464 | 64k×4 | 20/25 | CMOS | 600/25 | 5 | DIP, SOJ | 3Q91 | $16 | — |
| UM611256 | 256k×1 | 20/25 | CMOS | 600/25 | 5 | DIP, SOJ | 3Q91 | $15 | — |
| **White Technology** 4246 E Wood St, Phoenix, AZ 85040 (602) 437-1520 | | | | | | | | | **Circle 321** |
| WS-128K8-45CM | 128k×8 | 45 | hybrid | 300 | 5 | JEDEC | 6-8 weeks | $275 | TTL compatible |

## INTEGRATED CIRCUITS

nology (San Jose, CA), for example, while investigating BiCMOS, prefers to put off the expense of switching to BiCMOS.

"There's added cost with BiCMOS in terms of actual material as well as yields," says Steve Taylor, Paradigm's vice-president of sales and marketing. "It requires extra mask steps, which adds cost. In addition, you must build BiCMOS on epitaxial wafers. Not only are these more expensive than the silicon wafers used in CMOS, they're also more prone to defects." BiCMOS does have its place in the ECL I/O environment, Taylor adds, though the majority of the SRAM business is in the CMOS TTL I/O environment.

### CMOS advantages

While the expense of switching to BiCMOS remains an important concern, reasons for remaining with CMOS for the present have as much to do with the advantages CMOS offers. "CMOS is a highly reproducible, high-volume, and low-cost process," says Gene Cloud, vice-president of semiconductor marketing at

***"Most secondary caches generally don't need to be much more than 128 kbits deep."***

*—Robert Tabone, Hitachi America*

Micron Technology (Boise, ID). "We can achieve the performance with our CMOS process that many people tout for BiCMOS." Micron is researching a BiCMOS process, but doesn't plan to implement it in production until necessary.

Moving from the 256-kbit to the 1-Mbit generation of SRAMs didn't involve any drastic change at the cell level, according to Cloud. "We've advanced the design for the basic 4-T (four transistor) cell each generation," he says. "Part of that progress involves making higher value resistors for each generation. So the cell does evolve over time, but it's still basically the same 4-T cell. That's the most cost-effective structure that produces high performance." Micron's latest offerings include a 20-ns, 32k×8-bit SRAM and a 20-ns, 128k×8-bit SRAM.

Toshiba America (Irvine, CA) also has found a respectable kick left in CMOS technology, using it to produce a 15-ns, 1-Mbit SRAM. Built with a 0.7-μm CMOS process, the chip integrates some 6.3 million elements. Samples of the device are available in 16-bit-wide organizations. Because noise can be a problem at wider organizations, the

chip's layout was designed to reduce noise generated by its ground pins and voltage supply pins. These pins were moved to the middle of the pin rows to reduce the wiring lengths between the die and the pins, thus diminishing noise.

Motorola (Austin, TX) is another company that's stayed with CMOS, using a conventional 0.8-µm process to produce a 10-ns, 64-kbit SRAM and a 12-ns, 256-kbit SRAM. The company's long-term strategy, however, includes a move to BiCMOS. "Starting in 1992, everything that we introduce at speeds of 12 ns and faster is going to be BiCMOS," says Motorola marketing manager Curt Wyman.

Motorola does plan to continue a line of slower CMOS SRAMs at densities of 1 Mbit and higher. This, Wyman notes, is in response to an emerging demand for moderate speed, high-density SRAM for use as secondary cache or main memory, where speeds around 25 ns are sufficient and CMOS is preferable.

### Smaller cell boosts speed

At least one company, Paradigm Technology, uses its proprietary design technique to push the envelope of CMOS performance limits. Paradigm's dual-well 0.8-µm CMOS technology uses a self-aligned process designed to eliminate empty space in the cell. "When most people think of the 4-T cell in a an SRAM, they consider only the four transistors and the two resistors," says Paradigm's Taylor. "At a closer look, you notice that there's a lot interconnect between those elements. We figured out a way to do the interconnect without wasting space. That gave us a very tight cell. With higher-speed products you tend to waste more die space. But, with our inherently small cell, we can use the same size die or smaller as our competition and yet offer more speed."

Paradigm's 0.8-µm memory cell measures 32 µm square, which the company claims is the smallest cell size in the industry at any equivalent lithography. The technology is scalable to 4 Mbits, according to Paradigm. In its current SRAM family, Paradigm offers a 12-ns, 256-kbit chip in a 32k×8-bit organization. At the 1-Mbit density, the company has a 20-ns 128k×8-bit SRAM.

As vendors continue to defy the expected limits of CMOS, SRAMs at all densities are gaining speed. The extensive choices among commodity 256-kbit SRAMs have a lot to offer today's systems designers. Fast 1-Mbit SRAMs are finding new applications. Until a broader choice of organization and speed for 1-Mbit SRAMs is available, many designers will be satisfied with lower-density parts for their caches. ■



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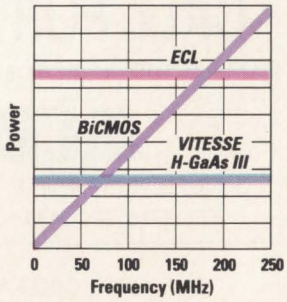


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CIRCLE NO. 59

SOFTWARE

# Toolset offers embedded object-oriented development based on Smalltalk

An object-oriented team programming environment and configuration management system allows development of embedded systems based on the Smalltalk language. Envy/Developer by Object Technology International supports the software manufacturing life cycle including prototyping, interactive debugging, performance analysis, and maintenance of applications.

The Envy/Developer toolset is aimed at realizing the benefits of object-oriented software development such as reuse of existing software components, improved reliability and lower maintenance costs over the life of the product. A windowed graphical user interface provides browsing tools for navigation through existing code, programming, testing, and debugging.

Envy/Developer can be used by programming teams in heterogeneous computing environments consisting of Apollo or Sun-3 workstations, personal computers and embedded target systems using the Motorola 680X0 family of processors. It's integrated to work as a configuration, library and version control system along with the Smalltalk/V programming language and development environment from Digitalk. All source and object code is kept on-line in a shared library that provides editions, versions and releases of applications. Complete source and object code version control is also provided for classes, methods and associated persistent objects.

All programming team members have instant access to updates and the complete version history of all components to avoid delays and unnecessary load builds. Change browsers let programmers compare different component versions and track changes down to a single line of source code. Run-time analysis tools let them identify potential performance bottlenecks. For those developing embedded MC680X0 systems, tools are provided for ROM applications written in Smalltalk.

One of the major advantages of object-oriented programming is the ability to reuse code. Developers may view and edit all available code, including the entire development history of each application, class or method. Applications, classes and methods can be loaded directly from the library into the image. Object code, for example, can be linked automatically without recompilation.

## Embedded options

In embedded application development, the Envy development tools and the Smalltalk/V environment run on the target system, while the graphics interface runs on the host system. That also means the target development environment needs sufficient extra memory to hold the Smalltalk/V system along with the Envy development environment.

A final production version of the target product would need considerably less memory than the development version. Envy/Developer can reduce that amount even further. Smalltalk has a reputation of being a memory glutton because of difficulty separating the development environment from the delivery environment, or the executable code. Envy/Developer includes a product packaging tool that allows production of small, stand-alone executables of applications.

Embedded Smalltalk can be used with commercially available real-time executives. Time-critical routines that might be hampered by the Smalltalk byte interpreter's garbage-collecting operations can be hand-coded in assembler and linked to the run-time package. Memory can be statically allocated for these routines and can guarantee setup so that garbage collection will not run while critical primitives are executing.

Envy/Developer supports Unix TCP/IP, Novell Netware, Sun PC-NFS, Banyan Vines, Digital PCSA, IBM PCLAN, and LAN Manager.

Configurations are available from three-user systems up to site or special corporate licenses. Prices start at $4,000 per user and can drop to as low as $500 per user depending on volume purchase.

*— Tom Williams*

**Object Technology International**
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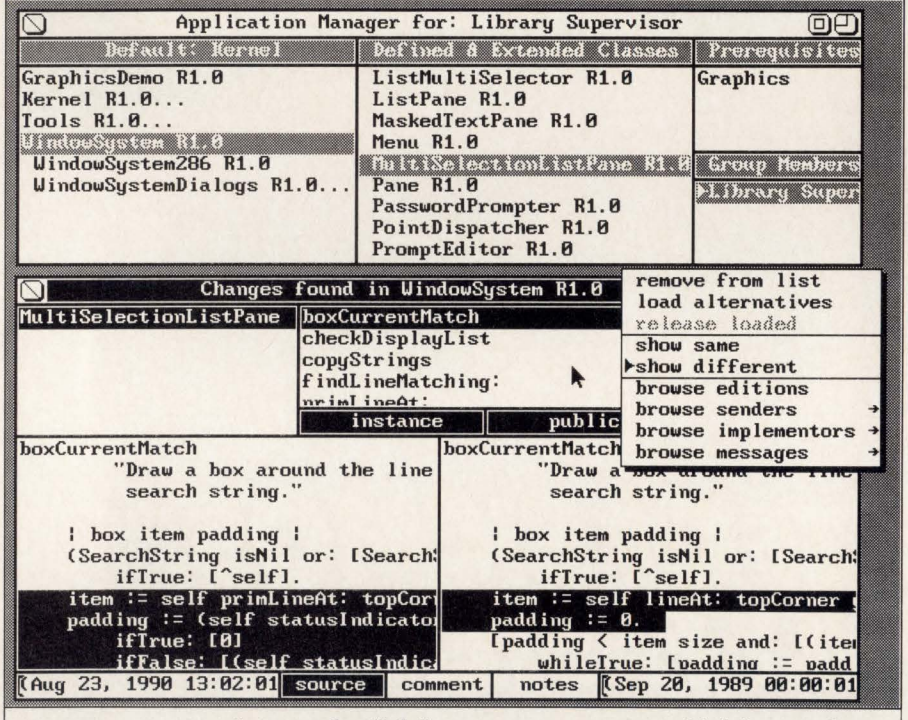
Ottawa, Ontario K2C 0P9
(613) 228-3535

*Circle 353*

**ENVY/DEVELOPER PROGRAMMING ENVIRONMENT**



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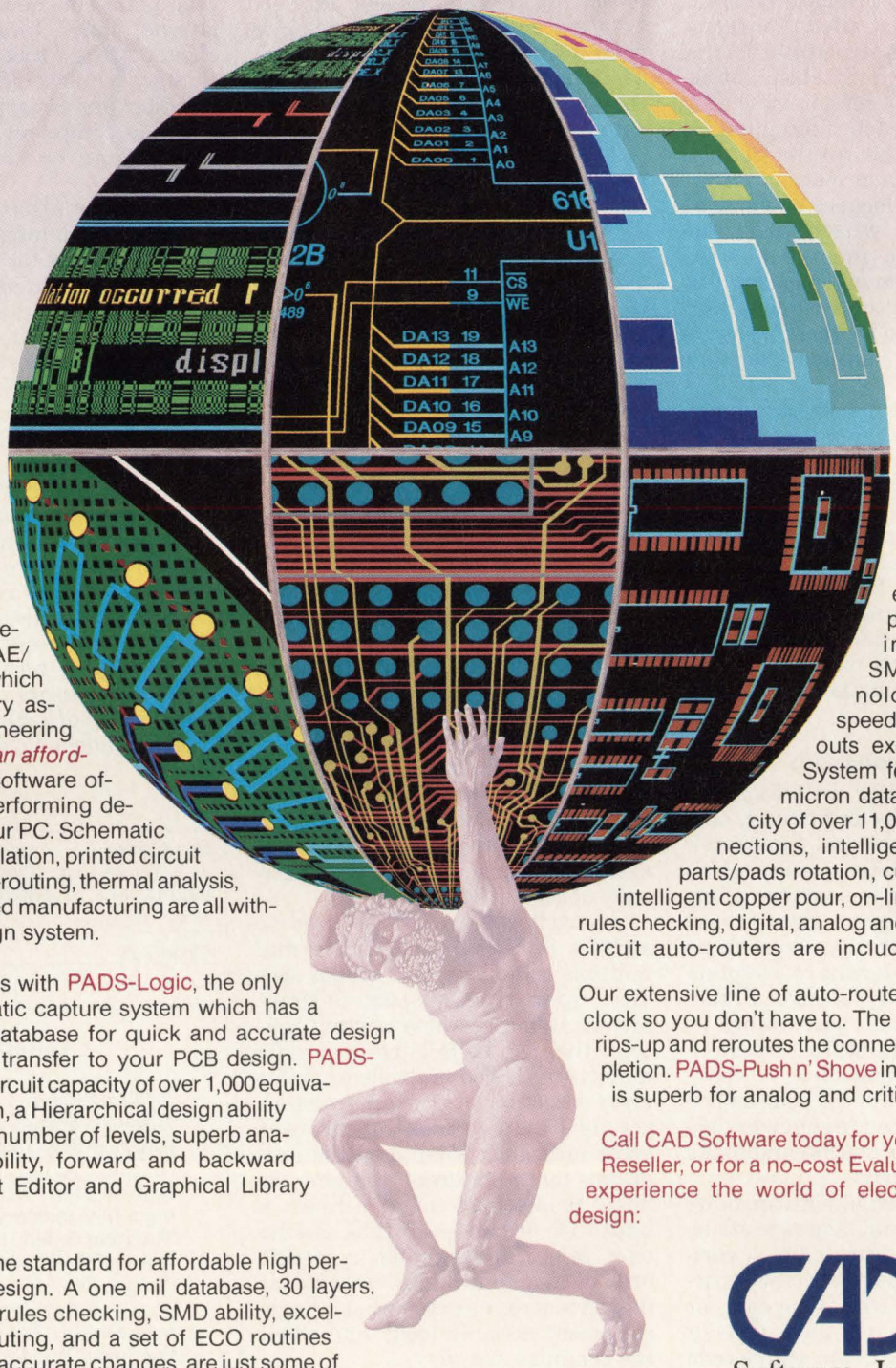


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**CIRCLE NO. 60**

SOFTWARE

# Programming environment improves reengineering and code maintenance

A new programming and software maintenance environment from ProCase helps programmers comprehend, reengineer, develop, and maintain C programs. Called Smartsystem, the toolset is structured around an object-oriented database. It includes a flexible user interface that can be customized for individual users, yet stores the results of their work in a common format.

Smartsystem focuses on existing code, the area where programmers spend the most time. Existing code is often difficult to understand because of poor documentation, often compounded by the absence of the original programmers from the organization.

Smartsystem consists of five major modules—the view, graph, store, check, and make/debug facilities—each beginning with the word "smart." These modules are sandwiched in a layer between the user interface manager and the database manager layers. Layering provides portability, configurability and separation of application code from both user interface and management issues. Modularity makes the system easily extensible.

## Editor with graphic aids

Smartview includes an editor and text-based facilities for filtering, navigation and formatting. Smartview is assisted by Smartgraph, which can graphically represent the calling structure of a program. Smartview's filtering facility lets users zero in on the code that's relevant to the problem they're trying to solve. Filters can be set based on such things as error and exception status, cross-references, pattern matching, or changes. Filtered views of the code can be edited so that software engineers can find the right information and make changes on the spot.

Smartview's navigation capability understands file and language structure and lets the user follow a variable or any language-specific structure through the code. One can, for instance, select a variable, type or function anywhere in the source code and navigate to its next or previous occurrence or to its declaration.

Smartview also contains an editor that includes text-based and mouse-based point-and-click functions. The formatting capability lets developers view and edit code according to their own formatting preferences. The final versions of their work can then be stored according to a corporate coding standard.

Another tool that can be used for navigation and for producing documentation is Smartgraph. It displays a graphical view of the calling structure of a program. The user need not view the entire structure; graphs can be produced for all or parts of a program and can be started at any point in a program's calling sequence. Filters can also be applied to the graph to allow the programmer to view only relevant parts of the calling structure.

## No surprises

Modifying poorly documented code produced by someone else can have unexpected results. Smartsystem's Smartcheck module provides multiple levels of checking the ramifications of changes. At the lowest level it performs incremental semantics and syntax checking. At the next level, it performs system-wide consistency checking that enables it to detect when a seemingly simple change might have ripple effects that must also be checked. Anytime even a small change is made, any existing dependencies are automatically checked.

Smartcheck can also be used to address issues of portability across multiple compilers and vendor-specific operating system environments. It incorporates parsing routines that can be tailored to specific dialects of C. The multiple compiler error detection lets the programmer set up filters to look for relevant error messages when creating programs for a different compiler or host. Smartcheck also includes a built-in C preprocessor that lets the user select and expand a specific area of code to look, for example, at nested macros or to see what a single statement actually looks like when the compiler sees it.

Smartmake supports fine-grained incremental compilation of the smallest units of code possible. It's aware of the modifications to code, the data dependencies of each function and the source dependency of programs, so that only those portions of programs affected by changes will be recompiled. Programmers can maintain their own altered source files while sharing object files that haven't been changed, thus avoiding needless recompilation. Smartmake supports multiple compilers and easily ties into remote or cross-compilation systems.

Finally, Smartstore is a C++ object-oriented database that provides the foundations for all of Smartsystem's other modules. It provides for multiple users to have controlled access to common data and also maintains a consistent view of the database for each programmer. Each programmer can make changes to objects without affecting the work of others. When one programmer's changes are checked in, that programmer's workspace is updated to reflect the changes made by other programmers on the team.

Smartsystem is available now. Individual modules are priced at $1,750, and the entire system sells for $8,750. A network license is available for users to purchase only the quantity of each module needed for simultaneous use.

*—Tom Williams*

**ProCase**
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(408) 727-0714

*Circle 355*

### Correction

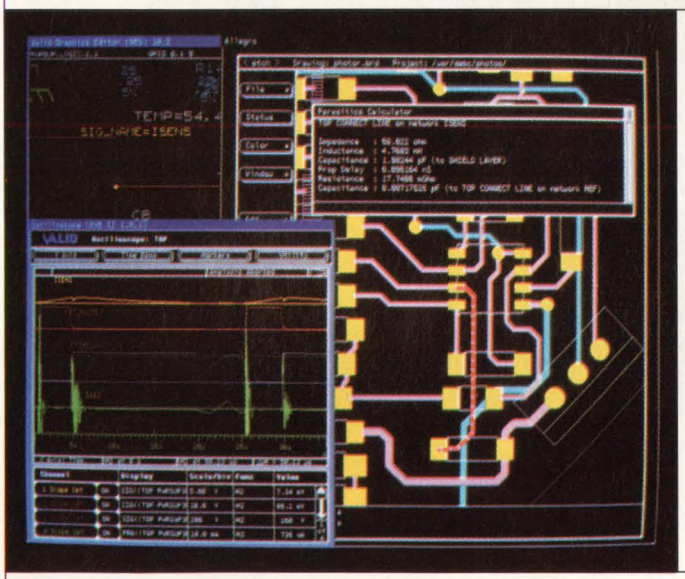
A "News Brief" in our February 1 issue reported that Toshiba America Electronic Components (Irvine, CA) developed a prototype 64-Mbit DRAM incorporating a new memory cell structure. The item failed to credit Toshiba's ULSI research center (Tokyo, Japan), where the device was developed. Readers interested in further information about the device should call Toshiba America Electronic Components at (714) 455-2000.

# Integrated environment targets analog PCB design problems

The Analog Systems Lab (A/S Lab) from Valid Logic Systems offers an integrated, front-to-back environment for the design of board-level analog systems. Designed to address the complex electrical and physical interdependencies typical of the analog design process, A/S Lab supports the use of curved traces and shapes with curved boundaries to minimize signal discontinuity (signal reflections) and maximize signal-to-noise ratios. The tool works within the ValidFrame framework to integrate Valid's Analog Workbench II with the 5.0 release of Valid's Allegro printed circuit board engineering system.

## Automated analog routing

"Traditionally, most analog boards have been routed by hand," says Shiv C. Tasker, director of printed circuit board marketing at Valid.



*Valid's Analog Systems Lab is an integrated environment for front-to-back design. The windowed display allows multiple simultaneous views of data. Here the circuit layout window (right) is overlaid with a parasitic calculator window. On the left an oscilloscope window is superimposed on the graphics editor.*

A/S Lab features any-angle placement capability that lets users place parts at any rotation to optimize printed circuit board real estate. In addition, users can create and visualize split power or ground planes on the same layer in different colors to accommodate multiple voltages and clearly identify areas of high potential differences. On-line access to alternate symbols for different packaging technologies lets the analog designer immediately address component placement restrictions imposed by electrical power, physical space, manufacturing technology, and parts-availability constraints.

Design rule checking capability has been enhanced to include checks for mechanical packaging restrictions, such as placing tall components in different areas of the board, and the unusual size, shape and insertability requirements of analog components. Automatic or user-directed line fattening is also provided to minimize trace resistance. The tool's autorouting capabilities support difficult two-layer routing strategies.

"This is a result of the sensitive nature of analog designs and the limitations of automated routing tools that don't consider the complex spacing, net impedance and capacitance requirements of analog circuits. A/S Lab uses rules-driven routing and gridless push-and-shove capabilities while following all the complex design rules of line widths and voltage-dependent spacings."

A/S Lab uses this rules-driven design methodology to let analog engineers incorporate specific performance considerations into their designs before the physical design process. Engineers can assign groups, component weights and net weights to keep interconnect distances short; specify net length to reduce stray capacitance or inductance; assign delay rules for matched lines; and specify rules regarding thermal or impedance considerations. Net layer, net spacing and line width rules designated at the schematic level guide the autorouting process and control layout-induced parasitics.

The tool also features an electrical parameter calculator that automatically extracts impedance, capacitance and other electrical values from the physical design and passes them to the circuit design for postlayout simulation. In addition, a variety of optional analysis capabilities, such as Monte Carlo statistical analysis, worst-case analysis, sensitivity analysis, and parametric plotting, are available to evaluate and optimize designs for reliability, cost and manufacturability considerations.

## Thermal analysis

For thermal analysis, actual component power dissipation information is calculated by the Analog Workbench's Smoke Alarm module and fed forward to the physical design phase. Optional thermal analysis software, ThermoStats, calculates junction and case temperatures and feeds these back to the Workbench for resimulation to converge on an optimum power dissipation and thermal management balance. Based on the simulation-analysis results, designers may choose to make component selection and placement adjustments.

A/S Lab can be equipped to analyze reliability tolerances to determine analog component failure rates. An optional reliability analyzer provides mean time between failure data for system assemblies and absolute failure rates for all design components.

Production shipments of A/S Lab are scheduled for May. The system is available as a network-sharable resource on Sun, Digital and IBM workstations and is priced at $45,000. — *Mike Donlin*

**Valid Logic Systems**
2820 Orchard Pky
San Jose, CA 95134
(408) 432-9430

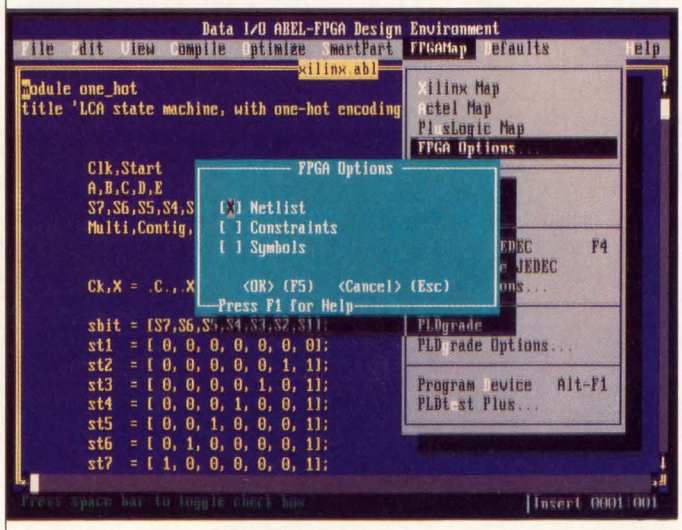
*Circle 352*

## DESIGN AND DEVELOPMENT TOOLS

# Design environment supports FPGA architectures

Data I/O's Abel-FPGA, a front-to-back solution for designers using field programmable gate arrays (FPGAs), provides design entry, optimization, device fitting, and logic synthesis for FPGAs. The tool, based on Data I/O's Abel Design Software, provides a familiar design path when moving to FPGAs.

Abel-FPGA has a DOS extended parser and reducer for handling the larger logic modules of FPGAs, as well as Abel-HDL capabilities, including constraints-generation for placement and routing of FPGA architectures. Optimization features include new criteria for netlist generation based on the details of specific FPGA architectures. In addition, menu features have been included to support FPGA design flow.




Several forms of behavioral entry are supported by Abel-FPGA, including state machine, high-level equations and truth tables. The tool also features an integrated design environment with an interactive user interface and context-sensitive help functions. Designers can enter and verify designs prior to specifying a target device or architecture. Design simulation can be performed before the target device is selected, and output can be viewed in multiple forms, including waveforms. Designers can also use Abel-FPGA to write high-level language test vectors for both design and device testing. In addition, placement and routing constraints can be entered as part of the Abel-HDL source description.

Output from Abel-FPGA includes vendor-specific netlists and vendor-specific constraint files. This allows the same design to be migrated between multiple FPGA vendors. Designers can also migrate existing programmable logic device designs to FPGAs, or design FPGA prototypes and migrate to gate arrays.

Abel-FPGA is priced at $7,995 and runs under MS-DOS on IBM XT/AT, PS/2 Model 70/80, Compaq 386 systems, and compatibles.

*—Mike Donlin*

### From descriptions to devices

Abel-FPGA device fitters are optimization programs that manipulate logic descriptions to most efficiently use specific device characteristics. FPGA device fitters automatically perform logic transformation, logic partitioning and some aspects of

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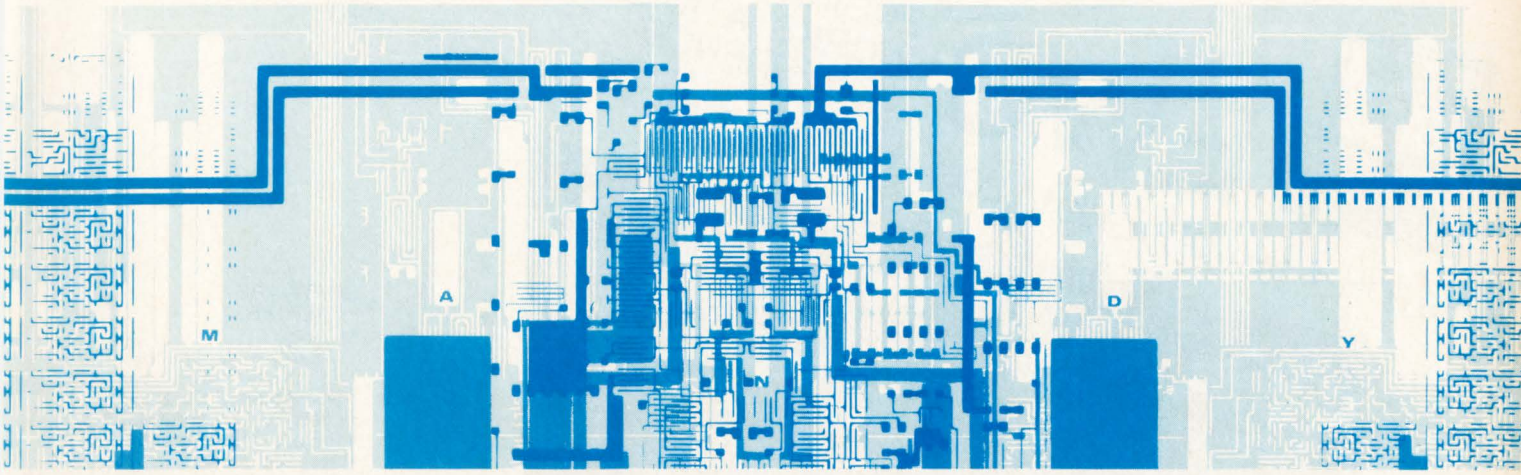

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DESIGN AND DEVELOPMENT TOOLS

# Cadence integrates PLD solution for systems design into toolset

Amadeus PLD, including the industry-standard Abel 4.0 PLD design tool from Data I/O, has been integrated with Cadence's design synthesis tools and Amadeus Systems Design Series. With Amadeus PLD, users can create a design at the gate level using schematics, describe a design in Verilog HDL, or use Boolean, truth-table or state-machine syntax descriptions in Abel. Linked to the new Cadence Improvisor front-end synthesis tool, Amadeus PLD allows users, after creating a design with Verilog HDL, to analyze technology alternatives prior to implementing the design as an IC, ASIC or PLD.

"Increasing design complexity and time-to-market pressures have increased the use of PLDs in board- and systems-level designs, calling for a new wave of PLD design capabilities," says Prabhu Goel, president of Cadence's Systems Division. "With the introduction of Amadeus PLD, Cadence is now providing the HDL-based design automation solution that will help designers handle today's complex designs."

The Amadeus toolset allows PLD users to migrate PLD designs described in Verilog HDL, or as schematics, to customized ASICs, and to prototype PLDs for future ASIC designs. Design migration through HDL-based synthesis, according to Cadence, eliminates manual translations and reduces errors. And to simulate PLDs in the context of the entire system, board-level designers can use PLD models from Logic Automation, or they can create structural Verilog models with a PLD modeling capability built into Amadeus. Cadence claims that automatic device selection, design partitioning, and Verilog-XL model generation increase a PLD designer's productivity.

Amadeus PLD is scheduled to start shipping next month, and pricing for the toolset begins at $12,000.

*— Barbara Tuck*

**Cadence Design Systems**
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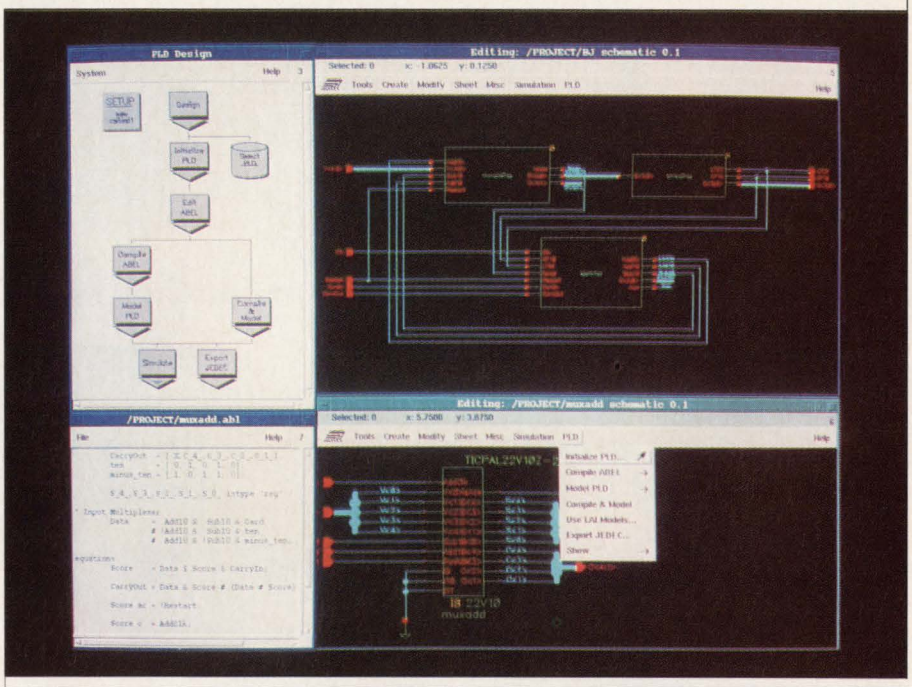

# Count On IDT

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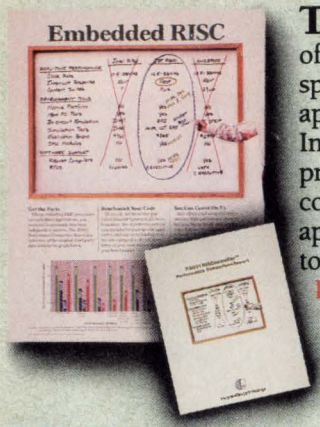


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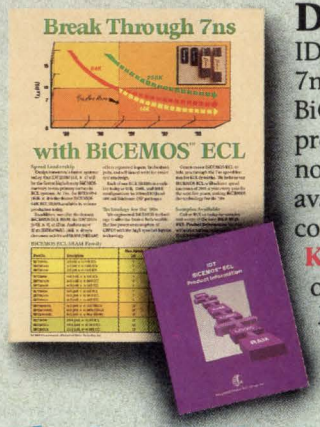


Design the fastest systems with IDT's BiCEMOS ECL family. At 7ns, the IDT10494 is the fastest BiCMOS 64K ECL SRAM in production. 256K and synchronous self-timed SRAMs are also available in 10K/100K/101K configurations. Call and ask for **KIT CODE 0091B** to get a copy of the ***BiCEMOS ECL Product Information*** booklet.

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## The SyncFIFO™ Family: Double Your FIFO Performance


SyncFIFOs offer leading-edge performance that is 50% faster than other FIFOs. The synchronous architecture is easy to implement and reduces chip count 9-to-1. SyncFIFOs have 18-bit buses and are ideal for 32-bit systems. Ask for **KIT CODE 0091D** to get ***AN-60: Designing with the IDT SyncFIFO™***.

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INTEGRATED CIRCUITS

# PLD for state-machine designs features low-power operation

The National Semiconductor MAPL128 Multiple-Array Programmable Logic device is the first in a new family of PLDs aimed at state-machine designs. An active partitioning architecture with a paged configuration, like that used in memories, sets the MAPL128 apart from other logic devices.

User-defined product and sum terms are dynamically allocated, depending on the logic design requirements. Macrostate registers with fixed feedback paths to a global bus determine which of eight PLA pages on the MAPL128 is enabled. Since only necessary logic terms are active, the MAPL128 draws just 140 mA max. from the supply. A worst-case system speed of 45 MHz, with feedback, is guaranteed across the MAPL product line.

The MAPL128—available in a 28-pin PLCC with JEDEC-standard power, ground, and clock pin placements—is functionally equivalent, according to National, to a large, continuous field-programmable logic array. Eight independent PLA planes each have the same 58×16×54 configuration. Each electrically erasable, programmable AND array has a total of 58 true and complementary inputs. The 16 product terms, which provide inputs to the electrically erasable, programmable OR array, can be programmed and interconnected to any of the 54 OR terms.

Either input or state variables can actively allocate the required terms for the additional logic arrays with zero performance delay, National claims. The same product terms required for normal output and state transitions are also used to control the PLA allocation or loading of the next PLA array. An extension of each PLA is used for interconnecting the partitioned PLAs and for driving the global macrostate registers.

## State-machine architecture

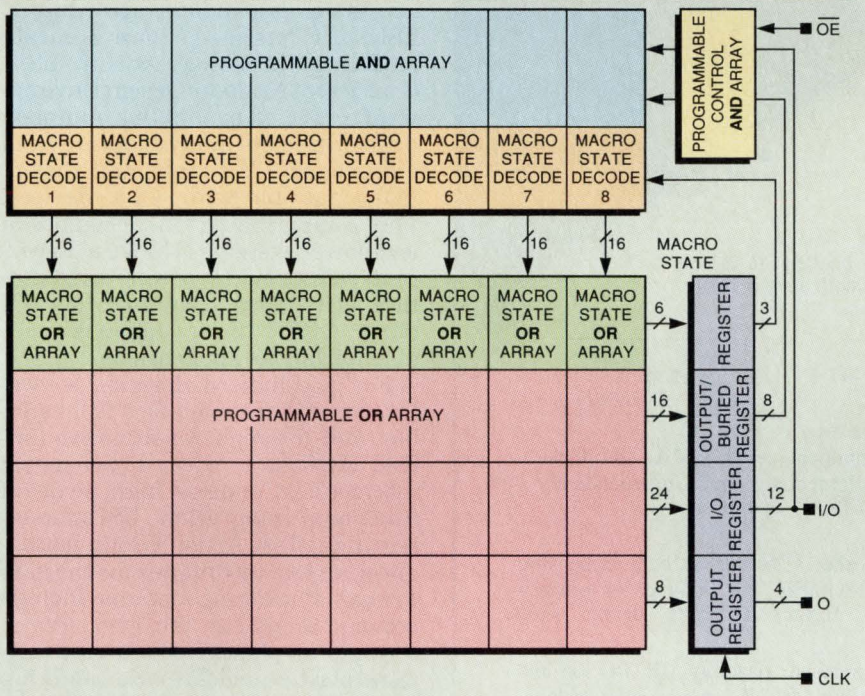
"We see our architecture as the ultimate solution for state-machine designs," says Jay Kamdar, National's director of programmable products. The company claims that the MAPL family offers considerable performance advantages over other programmable solutions for Mealy and Moore state-machine applications. A multiway branch capability lets input or state variables shift to any one of 65,536 possible states.

The MAPL128 has programmable output macrocells that can be individually configured to act as either D-type flip-flops with clock enable, or J-K flip-flops. That flexibility, National claims, eliminates the need for software transformations or for additional product terms to implement those functions.

A second 44-pin device, the MAPL144, will have the same structure and size as the MAPL128 but will allow for eight additional dedicated output pins as well as a dedicated output-enable pin. National supports MAPL family members with its Open Programmable Architecture Language software package, which accepts Boolean equations, truth tables, or state-machine language. An embedded Berkeley PLA interface provides a link to third-party PLD design tools.

In 100-unit quantities, the MAPL128 is $21.80. —*Barbara Tuck*

**AN ACTIVE PARTITIONING PLD ARCHITECTURE**

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*Circle 358*

INTEGRATED CIRCUITS

# Submicron arrays offer metalized memories and megafunctions

The LSI Logic Compacted Array Turbo series of gate arrays, having 20,000 to 200,000 usable gates (30,000 to 307,000 total gates), offers designers the ability to integrate up to 36 kbits of SRAM and 160 kbits of ROM. The 0.7-μm CMOS LCA200K gate arrays, available with both two- and three-layer-metal interconnects, offer a 25 to 30 percent performance boost over LSI's 1-μm LCA100K Compacted Array Plus gate array series.

The LCA200K library includes over 400 SSI/MSI functions or macrocells; over 300 macrofunctions for distinct architectural solutions; over 300 Intel, Motorola and Advanced Micro Devices industry-standard functions; and Sparc and MIPS Computer Systems microprocessors and peripherals. Among specialized library elements is a phase-locked loop cell that reduces system skew by compensating for chip clock skew, clock trunk ramp time, and process effects.

A critical step toward achieving the high performance of the LCA200K gate arrays, according to LSI Logic, has been a more accurate modeling technology within LSI's Concurrent Modular Design Environment, expected to ship this summer.

The new gate arrays operate from a standard 5-V supply, and they're I/O-compatible with 3.3-V devices. This compatibility lets designers of low-power systems achieve a 55 percent reduction in power consumption, LSI claims, compared to a 5-V buffer. A 3.3-V library option is available for laptop applications.

For pad-limited designs, a two-layer-metal interconnect is available, and for high-density, core-limited ASICs, a three-layer-metal interconnect enables high levels of functional integration. LSI also offers Joint Test Action Group boundary-scan test techniques for the gate arrays. Packaging options include ceramic or plastic pin grid arrays, ceramic or plastic leaded chip carriers, plastic quad flatpacks, and chip on tape (tape-automated bonding or wirebonding).

LSI's Modular Design Environment toolset, as well as the enhanced Concurrent Modular Design Environment toolset, supports the LCA200K gate arrays. Customer prototypes will begin shipping this month, with production shipments beginning two months from now. NRE charges start at $75,000. *—Barbara Tuck*

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Perhaps a good way to view the differences between American and Japanese business strategies is to consider the games of chess and go. In chess, the object is to capture individual pieces and corner the king. In go, the object is to occupy strategic positions to control territory. The acquisition of MCA by Matsushita serves as an example of the devastating effects of a go mentality vs. a chess mentality, and bodes ill for the future.

The first reactions in the press were that the U.S. culture was so lucrative that the Japanese probably would not block the release of films like *Tora! Tora! Tora!* This is the judgment of a player who thinks he has just lost a rook when in fact he has lost half of his maneuvering area. The MCA acquisition, along with the earlier acquisition by Sony of CBS Records, is really about digital audio tape and high-definition TV—and even more ominous issues beyond those.

*Around 1993 or 1994, the VME base will be able to cross the bridge into VFE territory.*

The situation leaves the impression that the U.S. government and business elite is a confederation of fools—fools who treat employees like the enemy; who measure success in three-month increments; who can't bear to invest in research without assurance of an immediate return.

In the past few years the recording industry was obsessed with defending its queen—an outmoded revenue and royalty

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In the past few years the recording industry was obsessed with defending its queen—an outmoded revenue and royalty






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CIRCLE NO. 614

## Staff Written S-bus Keynote Feature

Warren Andrews
Senior Editor

*VMEbus and Multibus II link up with Futurebus+, bringing new architectural dimensions to the open-bus playground.*


Whatever the term "bridging" the buses" comes up, the subject invariably turns to Futurebus+. In fact it seems that using the word "bridge" for a communication scheme between buses first became popular around last February when excitement over Futurebus+ popularized the concept of a bus hierarchy. Almost all the major players of VITA (VMEbus International Trade Association) and the VMEg (Multibus Manufacturers Group) banded together in a herculean effort to finalize the Futurebus+ specification and to develop bridges between it and the other major 32-bit buses.

Now, only a year later, the specification is complete and will soon see its formal debut at Buscon/90 West to be held Feb. 13-16. At the same time the first of the Futurebus+ bridge specifications—Futurebus+ to VMEbus—will be unveiled. But even though Futurebus+ and its bridge to VMEbus and Multibus, and a reported effort to bridge to IEEE 1014/Extended Industry Standard Architecture, are receiving a lot of publicity, they are by far not the only ongoing effort to tying the same or different buses together with some sort of bridge. Bridges exist, or are under development, for VMEbus to VMEbus, Multibus II to Multibus II, VMEbus to S-bus, and even VME bus to Multibus II.

Though at its most complete, a bridge is little more than a communications scheme allowing two buses to talk to each other, the more widely accepted definition states that a bridge allows two buses to operate as if boards of both buses were on the same backplane. A tall order.

At this level of complexity, there's a lot more going on than just the simple exchange of data. The bridge must take into account the transfer of control signals, addresses, block or burst transfers, interrupts, priorities and other bus signals in addition to transferring data in bits, bytes or blocks. And when the bridge interconnects different buses, each bus must be capable of operating independently at its own maximum performance while being able to communicate with the other bus.

Theoretically a bridge shouldn't tie up one bus while waiting for the other. In addition, it would be desirable for the transfer rate to at least equal that of the slower of the two buses. In theory, perhaps transfers between identical buses can be managed by a simple extension of the backplane—adding a few buffers and high-speed transceivers, matching the timing and interconnecting them with a length of cable. This approach is taken in some cases, but it's usually limited to tying only two systems together.

In most cases, though, bridging buses isn't that easy, and trade-offs have to be made. Obviously, when designers are interconnecting different buses, backplane control logic and data organization are different. But even when bridging the same bus, they must take some special considerations into account—particularly if high transfer rates are to be sustained and if the bridge is to interconnect multiple systems.

One of the highest-speed VMEbus-to-VMEbus bridge schemes that's available comes from Ironics (Ithaca, NY). The firm's high-performance Multi'rate Pipeline (MPL) link can transfer information among up to 12 VMEbus systems at rates exceeding 22 Mbytes/s (see "VME-to-VME bridge achieves 32-Mbyte/s transfers," p. 77).

"To get the fast transfer rate, we traded off some of the software transparency to achieve the increased performance and interconnect flexibility," says Ed Schulman, vice-president of marketing at Ironics. While the programming changes have to control the interface function, Ironics has developed some software routines that permit the programming changes to be made at the application level rather than the interface level.

**Bridging to S-bus**

While VMEbus-to-VMEbus bridges offer one set of problems, bridges to other buses pose yet other problems, as Performance Technologies (East Rochester, NY) is discovering. The company is currently developing a bridge for VMEbus and the Sun Microsystems (Mountain View, CA) S-bus. The introduction of Sun's SparcStation with only a limited number of S-bus slots has led many users to seek out ways of expanding their systems, according to Don Turrell, vice-president of marketing and sales at Performance Technologies. One of the most logical approaches, he says, is to have a bridge from S-bus to a separate VMEbus chassis, where a number of readily available VMEbus cards can be added.

"When we were putting together our S-bus to VME bridge, we went from the concept of a logical connection to the idea of an independent link connecting a board of one bus to



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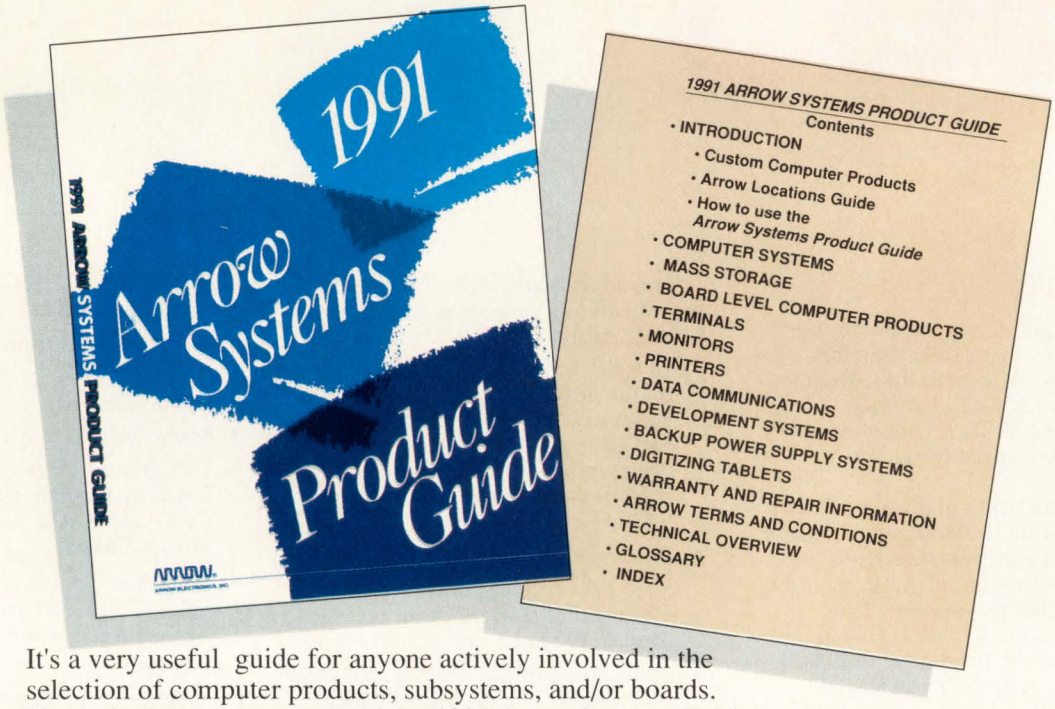


It's a very useful guide for anyone actively involved in the selection of computer products, subsystems, and/or boards. If you don't have your copy of the *1991 Arrow Systems Guide*, or someone has "borrowed" it, fill out and return the card below to receive your own copy of this important product resource.

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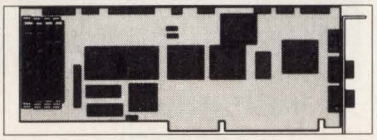

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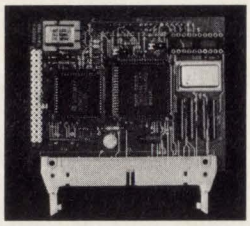

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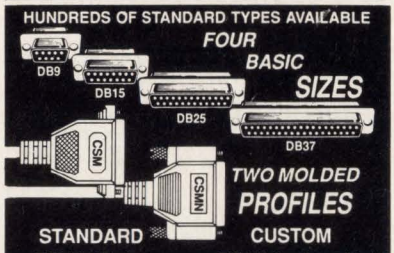


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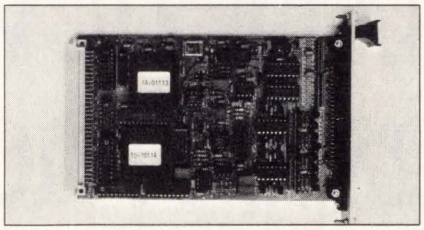

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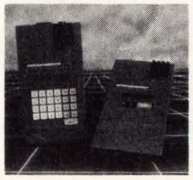

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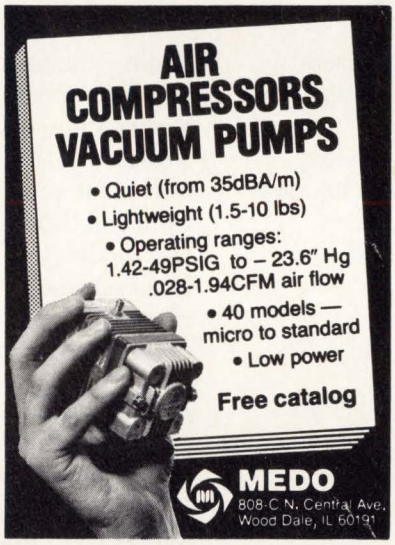


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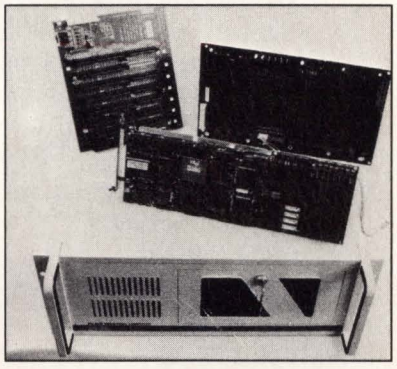

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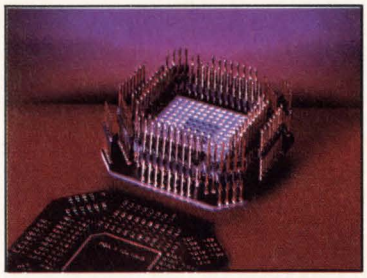

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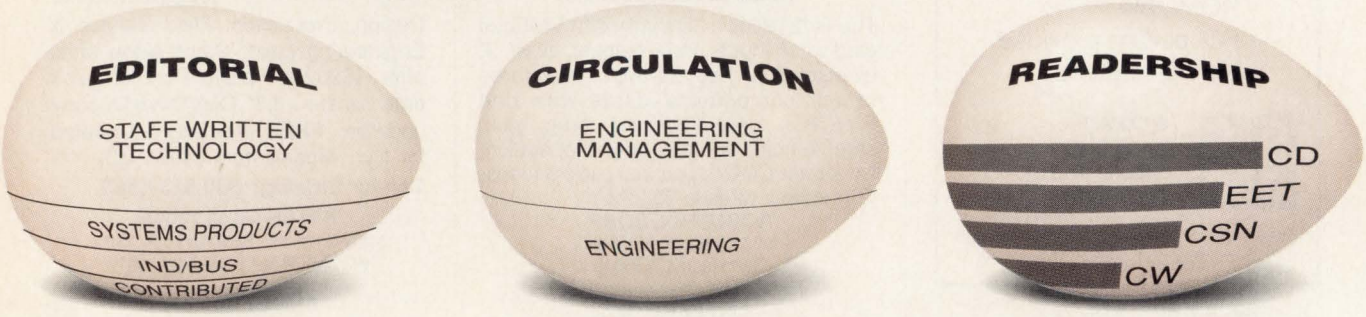


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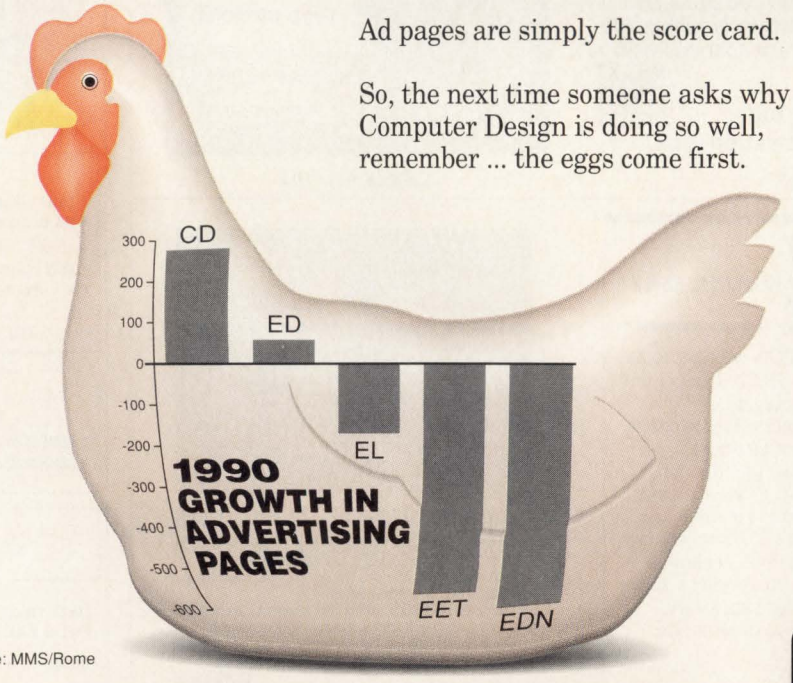


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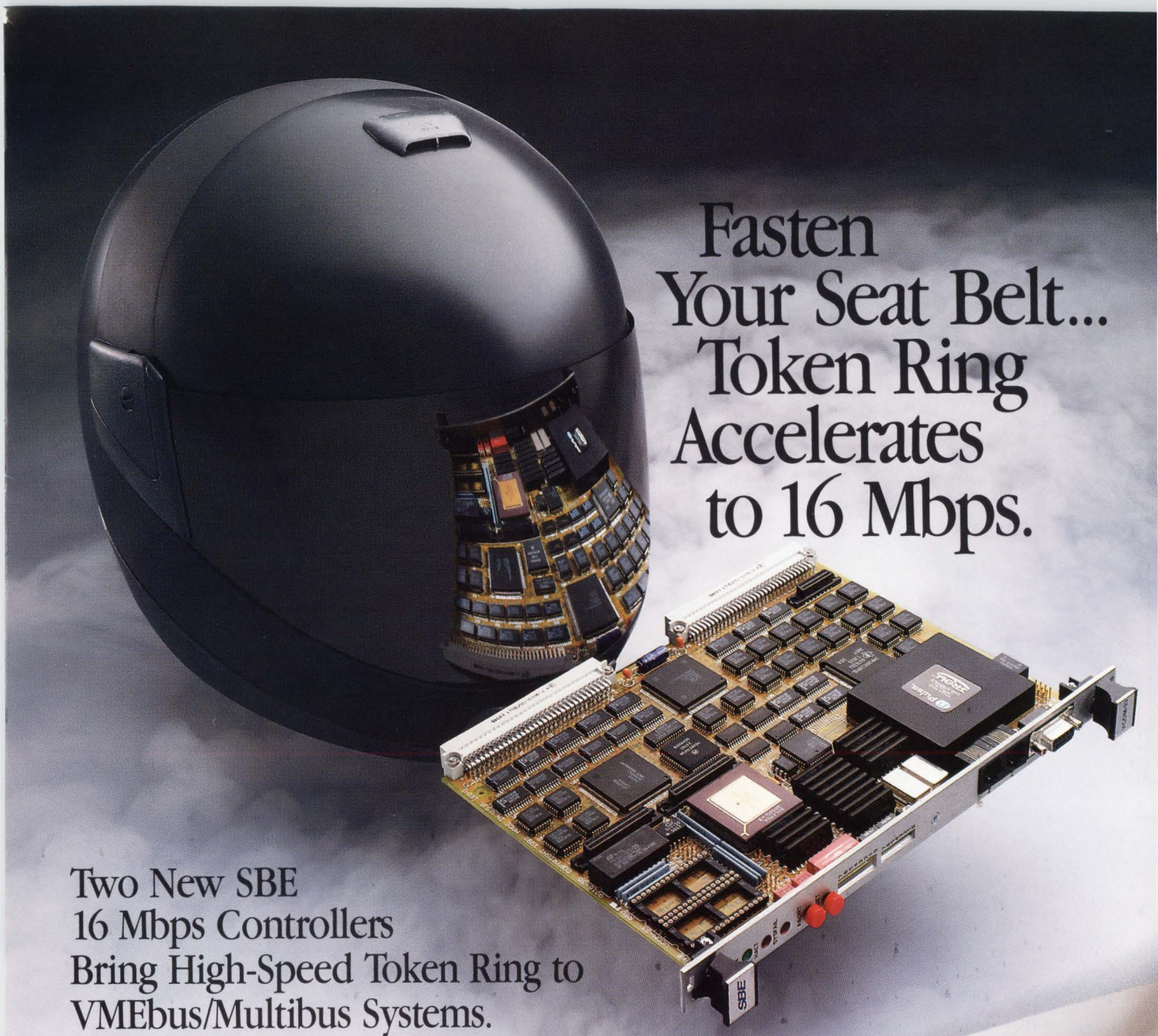

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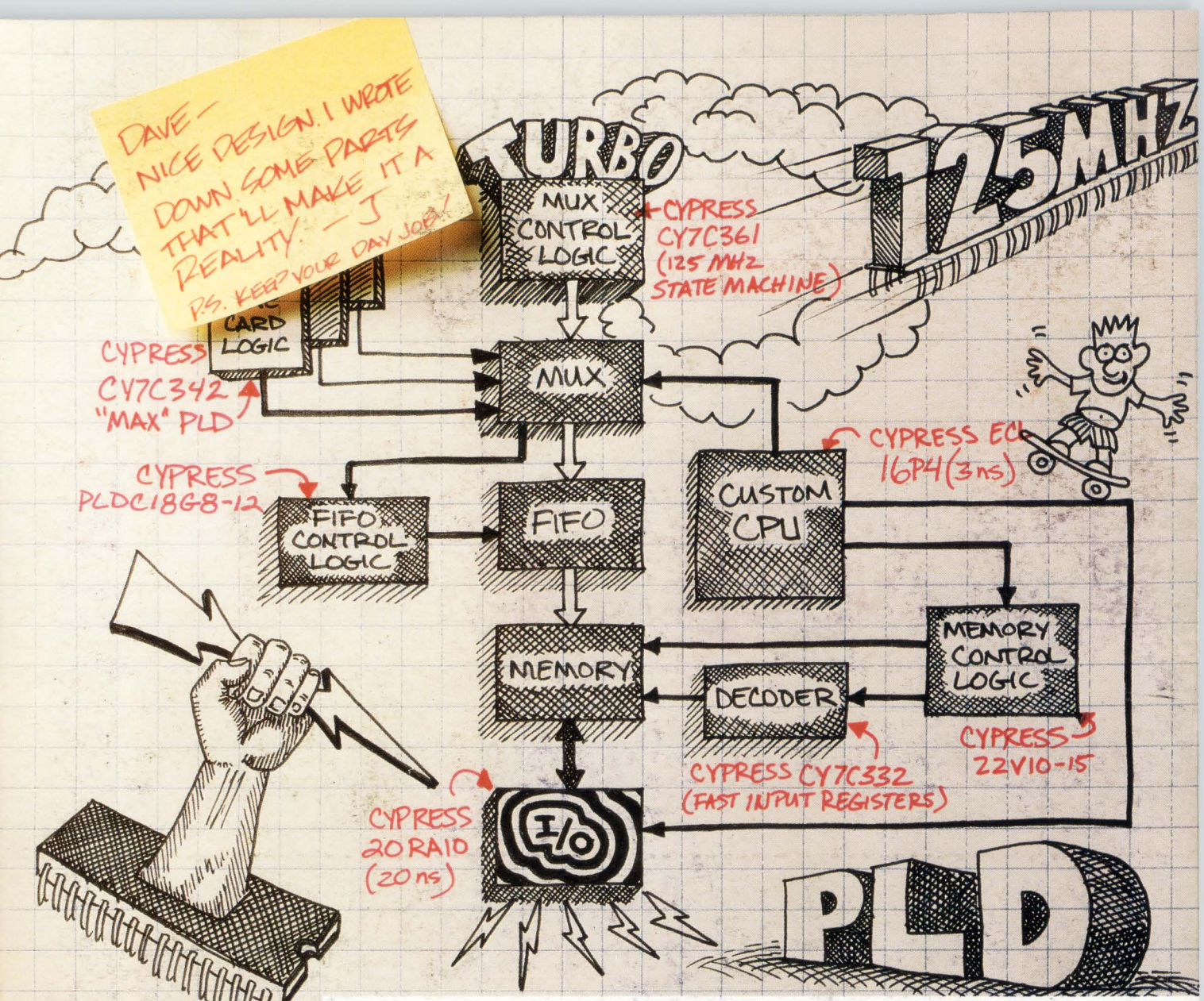


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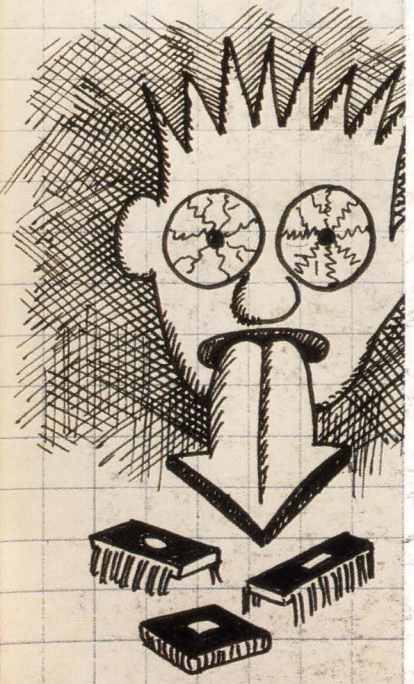


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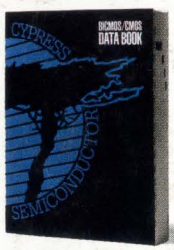


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