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COMPUTER DESIGN®

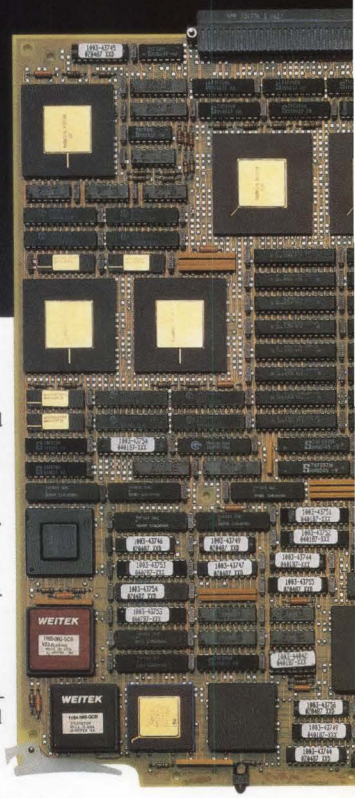
OCTOBER 1, 1988

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

ASIC memories: bigger, faster, and customized

- Innovative packages emerge to carry faster, denser chips *Page 35*
- Automated optimization refines SIMD microcode *Page 67*
- Linear power supplies survive in low-power applications *Page 100*

This year, you'll hear a lot of claims that "systems" design automation has arrived.



This 32-bit processor board was designed and simulated on Mentor Graphics workstations by Sequent Computer Systems for its multi-processor Symmetry computer system. It contains over 175 IC components including 80386 processors, a 14,000-gate standard cell and two 10,000-gate arrays.

At Mentor Graphics, we know better. And so do our customers.

They preach. We practice.

Skeptical about "systems" electronic design automation?

You should be. Because in many cases, it's a triumph of form over content. In the end, there's only one practical yardstick for evaluating a systems design solution. And that's how many successful products it has produced.

Apply this measure and the field narrows dramatically. Essentially, down to a single vendor.

Mentor Graphics.

For over five years, our customers have been turning out sophisticated board products with our EDA tool set.

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Are your tools capable of managing over 1000-page product documentation projects from start to finish?

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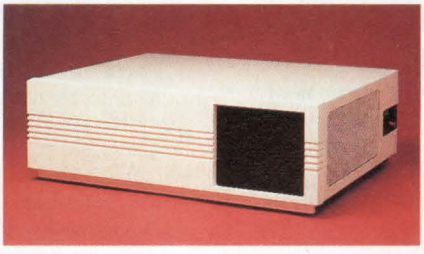

You do get a choice between two multiple-output power supplies: 190 Watts with 19A at +5V or 270 Watts with 30A at +5V. You can also choose a J2 backplane for VME extended addressing or iLBX II for a Multibus II system.

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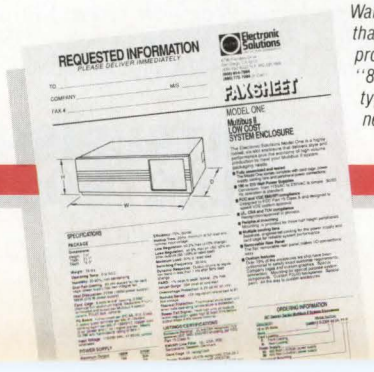

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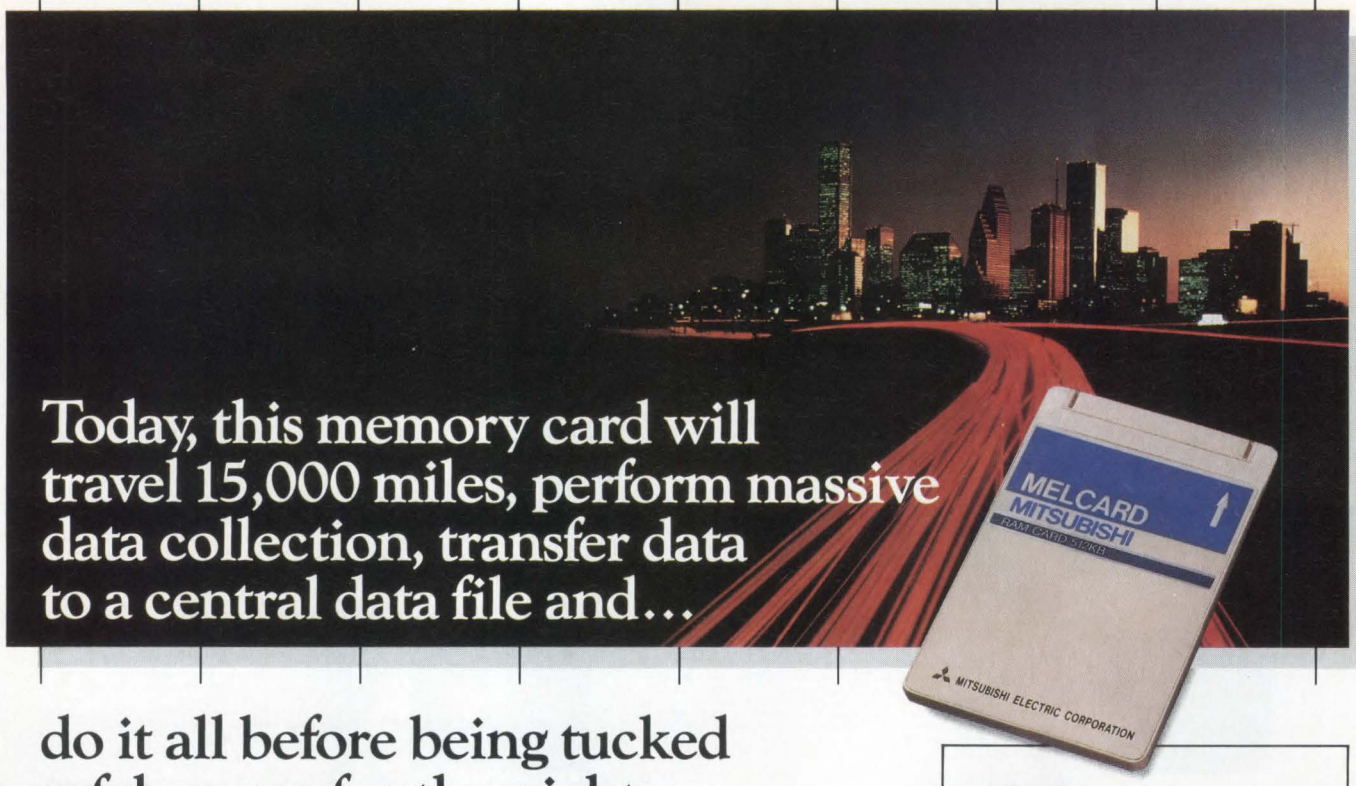


Today, this memory card will travel 15,000 miles, perform massive data collection, transfer data to a central data file and...

do it all before being tucked safely away for the night.

Now, with Mitsubishi's transportable memory cards, you can have the flexibility of carrying 32K Bytes to 2M Bytes of SRAM, OTPROM or masked ROM in your pocket. That means read/write capability (without a disk drive), remote from central data storage, plus the flexibility to interchange memory types (SRAM, OTPROM, masked ROM), upgrade and downgrade memory density, and change data width (8 bits, 16 bits). All with an extremely rugged device that's the size of a credit card (86mm x 54mm x 3.4mm).

The Applications Are Virtually Endless.

From personal computers to printers, portable equipment to telecommunications, the applications are as creative and endless as the imagination. Anywhere transportable memory and massive data storage are required, Mitsubishi's transportable cards offer the highest memory densities available on a device this small.

Save On Systems Design Costs.

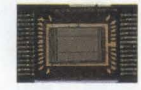
Mitsubishi's transportable memory cards offer standardized card connectors and pin assignments for easy memory interchange and density upgrade, without designing multiple host system models. Plus, future system redesign is simplified or eliminated.

Extremely High Density Memory.

The key to Mitsubishi's extremely high density memory cards is the VSOP (very-small-outline-package). Pioneered by Mitsubishi, the VSOP is over four times smaller (in overall volume) than its equivalent pin count, standard surface mount package. In fact, the VSOP is smaller than the footprint of the equivalent chip-on-board technology making it possible to pack up to 16 memory ICs, plus standard interface circuitry on one card.

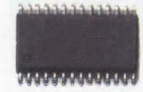
VSOP

13.8 mm x 8.0 mm x 1.0 mm = 110.4 mm^3



Chip-On-Board

15.4 mm x 9.8 mm x 1.0 mm = 150.9 mm^3



SOP

17.5 mm x 12.2 mm x 2.2 mm = 469.7 mm^3

"Transportable" Means "Rugged."

Mitsubishi designed its memory cards specifically for transportable applications. And, that means cards that are rugged and reliable. Even if a card is dropped, loss of valuable data is virtually eliminated, due to Mitsubishi's flexible, four-layer PCB and enhanced soldering techniques.

Additionally, the cards are ESD protected to 25K volts, with connectors guaranteed for 10,000 insertions.

If you want to design-in massive, transportable data storage with the flexibility to interchange memory types and densities, Mitsubishi memory cards give you the maximum memory mileage. For more information call or write today: Mitsubishi Electronics America, Inc., Semiconductor Division, 1050 East Arques Avenue, Sunnyvale, CA 94086. (408) 730-5900.

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CIRCLE NO. 3

Vol. 27, No. 18 **COMPUTER DESIGN** OCTOBER 1, 1988

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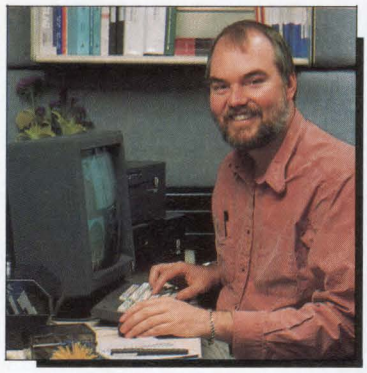
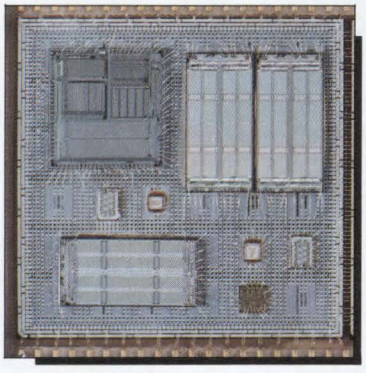


Page 20

■ TECHNOLOGY UPDATES

BUSCON SECTION



Page 35

■ TECHNOLOGY AND DESIGN FEATURES

Page 100

■ NEW PRODUCT HIGHLIGHTS

■ DEPARTMENTS/COLUMNS

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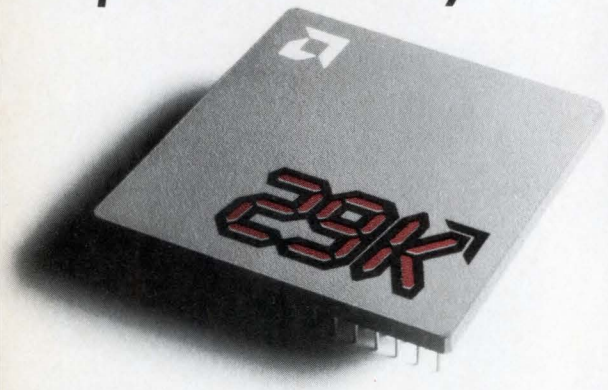

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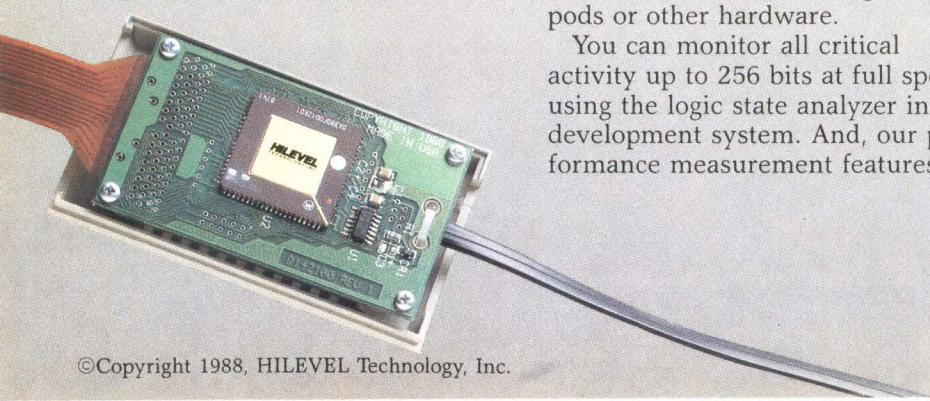

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Apple beats competition with 68030-based system

Despite the hoopla surrounding RISC-based processors, expectations have been building that Motorola's latest generation CISC processor will begin to appear in popular personal computer and workstation configurations. Steve Jobs' company, Next (Palo Alto, CA), is reportedly planning a 68030-based workstation for introduction at Comdex Fall in November, and Sun Microsystems (Mountain View, CA) is also rumored to have a system in the works.

But the first and potentially biggest splash has come from Apple Computer (Palo Alto, CA). Apple has unleashed the Macintosh IIx, a machine built around a 16-MHz 68030 and a 68882 floating-point processor. The new system executes most applications about 15 percent faster than the older 68020-based Macintosh II. Using a NuBus architecture much like the Mac II, the IIx offers six expansion slots and 4 Mbytes of on-board RAM. Only time will tell how the supercharged Mac IIx will fare when competing against Unix-based engineering workstations. Such a direct challenge to Sun and Apollo may force Apple to face issues regarding operating system, networking, system support and application software, from which the company has been shielded in the personal computing market.—*John Mayer*

Consortium challenges the Micro Channel

A consortium of more than 60 companies involved in manufacturing personal computers, mainframes, peripherals and software, including such giants as Compaq, Epson America, Hewlett-Packard, NEC Information Systems, Tandy and Zenith, has announced a direct challenge to the IBM Personal System/2 Micro Channel bus. Claiming that the Micro Channel hasn't been accepted in the PC market, the group has made a commitment to develop and use a new 32-bit PC bus structure, called the Extended Industry Standard Architecture, or EISA.

The new bus will provide the appropriate bandwidth for 32-bit CPUs, but will retain compatibility with existing PC/AT-bus cards. Amid growing concern about IBM PS/2 sales, increasing criticism of the OS/2 operating system and emerging challenges from the Macintosh family and 80386-based Unix workstations, the announcement casts grave doubts on IBM's ability to sustain its PS/2 strategy. But for the PC option card developer, the announcement may only add further uncertainty to an already risk-laden decision: which buses to support, and how many? —*Ron Wilson*

Motorola and Cypress square off over new RISC venture

Motorola Semiconductor (Austin, TX) has been granted a temporary restraining order that will bar five ex-Motorola employees, including Roger Ross and four other key members of the 88000 introduction team, from participating in the planning or development of "any semiconductor devices," pending an October hearing. The five left Motorola to form Ross Technology, a consulting firm involved in designs built around Sun Microsystems' Sparc (Scalable Processor Architecture). Cypress Semiconductor (San Jose, CA) has provided some funds to Ross Technology, and the two companies are said to be discussing licensing and foundry agreements.

Motorola's suit charges that Cypress conspired with members of the 88000 design and marketing teams to bring about the formation of Ross Technology. The suit seeks to bar the departed employees from entering Motorola's area of business, and asks for $8 million in damages from the ex-employees and Cypress. Following closely on suits regarding trade secrets and patent infringement from National Semiconductor and Advanced Micro Devices, the Motorola action leaves Cypress facing three major legal actions at once.—*Ron Wilson*

Backing into the future

With the introduction of the Personal System/2 Model 30 286, IBM (Armonk, NY) has reentered the AT market that it created and then abandoned. In April 1987, IBM claimed that it was replacing the AT architecture with the PS/2 Micro Channel bus because it offered advanced features such as multiprocessing and automatic system configuration. This move signaled the cloners to jump into the lucrative AT market and offer enhancements such as 80386 processors and increased memory speed, which dampened enthusiasm for the PS/2.

IBM's "new" Model 30 286 will be based on the Intel 80286 microprocessor but will use an impressively streamlined mother board, thanks to a five-chip logic set developed by VLSI Technology (San Jose, CA) that will reduce the chip count to about 17 percent of a standard AT's 88 ICs. The 10-MHz system will use the DOS 4.0 operating system and support up to 16 Mbytes of memory.—*Michael Donlin*

Laptops offered first 2½-in. Winchester disk drive

The pieces for low-cost, high-performance laptops continue to fall into place. Flat-panel display manufacturers are finally developing displays with high resolutions at lower prices. Now a disk drive manufacturer is introducing a significant space savings in disk storage. Prairie Tek (Longmont, CO) has unveiled the first 2½-in. hard disk drive for laptops. Occupying just 30 percent of the volume of a standard 3½-in. drive and weighing a featherlike 9 oz, the 1-in.-high Prairie 220 packs 20 Mbytes and an AT-compatible or SCSI controller into its compact footprint. Average seek time is a respectable 28 ms, and power consumption averages 1.5 W. That's a 25 percent improvement in power usage over the low-profile 3½-in. Winchesters available from Conner Peripherals (San Jose, CA) and Seagate (Scotts Valley, CA).

The success of the Prairie Tek

(continued on page 10)

drive will hinge on its ability to hurdle two obstacles: convincing the industry to follow the company to the new 2½-in. format and making sure the drive proves to be reliable. Prairie Tek is attempting to address the reliability issue with a couple of design innovations. A unique ramp-loading mechanism ensures that during an unintentional power-down the disk heads are safely unloaded and locked on the ramp structure. The design helps eliminate stiction, a common mode of failure for plated media drives. The company claims that its drive will withstand a 100-g force at 11 ms in a nonoperating environment. Adding to the drive's reliability is an actuator roughly one-half the mass of a typical coil actuator on a 3½-in. drive.—*John Mayer*

Imaging and neural nets to jointly attack machine-vision problem

For years, companies in the image-processing arena have tried to solve the problem of machine vision, with varying and less-than-satisfactory results. Imaging systems have been very good at enhancing image quality and extracting important features for the recognition process. But they've failed in establishing sets of rules by which objects can be recognized, and they've generally been limited to template-matching techniques, which limit the vision process to a very small subset of problems.

Now, however, two imaging companies, Datacube (Peabody, MA) and Imaging Technology (Woburn, MA), have joined forces with a neural network company, Nestor (Providence, RI). The Nestor Development System neural network software can be used to create intelligent pattern-recognition systems that can learn to recognize images presented to them by example rather than trying to classify them according to a set of rules dictated by a programmer. The imaging equipment will enhance and filter images to present a set of features on which the system can base its recognition decisions.—*Tom Williams*

Board maker doubles as vendor of Micro Channel ASICs

Forced to design its own application-specific IC to overcome the size constraints of its Personal System/2 board, which is 38 percent smaller than the IBM PC AT boards it had been designing for several years, Data Translation (Marlboro, MA) now has decided to market the device to other board manufacturers. A complete Micro Channel controller for either memory or I/O adapters, this CMOS ASIC also helps to overcome the limited power that's available per expansion slot for the PS/2.

The device will support multifunction I/O controllers, programmable option select, two DMA channels for multifunction interfaces, simultaneous dual controllers (either input or output or both), and continuous data transfers across DMA block boundaries. It meets all IBM-specified timing and drive specifications. Although designed for 84-pin plastic leaded chip carrier sockets, the ASIC can also be used in surface applications so that users will be able to inventory only one chip for both interface board designs.—*Sydney Shapiro*

IBM to employ Next's user interface

IBM has reportedly licensed a user interface system from Steve Jobs' company, Next (Palo Alto, CA), for use on a forthcoming version of the RT PC RISC-based Unix workstation. The interface software was developed by Next for use in its as-yet-unfinished 68030-based desktop computer, running under the Unix-like Mach operating system. IBM will presumably use the interface design to construct a user-friendly front-end for its new RISC workstation, which is reportedly taking shape under the guidance of RISC pioneer John Cocke at the company's Austin, TX facility. If nothing else, the agreement, with its reported $10 million in licensing fees to cash-hungry Next, should temper Jobs' renowned hostility toward IBM for a while.—*Ron Wilson*

Intel moves Multibus II to system level

At Buscon East this week, Intel (Hillsboro, OR) will introduce an extension of its Multibus II board architectural concept for system-level architectures. The Multibus II Systems Architecture (MSA) is intended not only to make it easier for designers to implement Multibus II board-based systems, but also to make the architecture available to other vendors for incorporation into their boards or firmware. MSA is also expected to help overcome the multiprocessing overhead burden inherent in some complex systems.

But not to ignore Multibus I, Intel will also introduce a second-generation series of 16- and 20-MHz, 80386-based CPU boards, several I/O boards, and additional packaging. In addition, the company will introduce a graphics subsystem that can be used in a real-time system without degrading system performance. Intel will also announce expanded networking options across the company's entire product line.—*Sydney Shapiro*

Graphics interface targets multitasking, real-time systems

Applications developers for multitasking, real-time systems now have a graphics interface based on the popular Gem Application Program Interface. Digital Research (Monterey, CA) will unite its Gem graphics development toolkit with its FlexOS real-time target operating system to provide sophisticated automation graphics for multitasking systems. "We'll do it without jeapordizing performance from a real-time perspective," claims Frank Iverson, vice-president for worldwide marketing. The multitasking version of Gem, called XGem, will be 100 percent compatible with existing Gem applications. The interface has already been submitted to the Open System Foundation (OSF) for consideration as the standard user environment for OSF's Application Environment Specification.—*John Mayer*

The P-CAD Software That Made This Famous Laptop Computer Is Now Made To Fit Your Budget.

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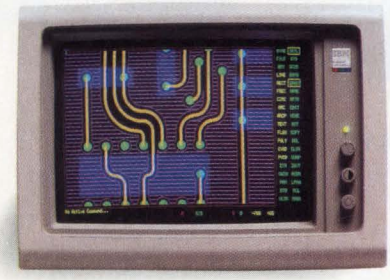

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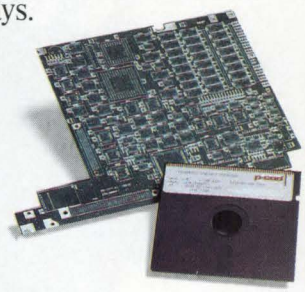

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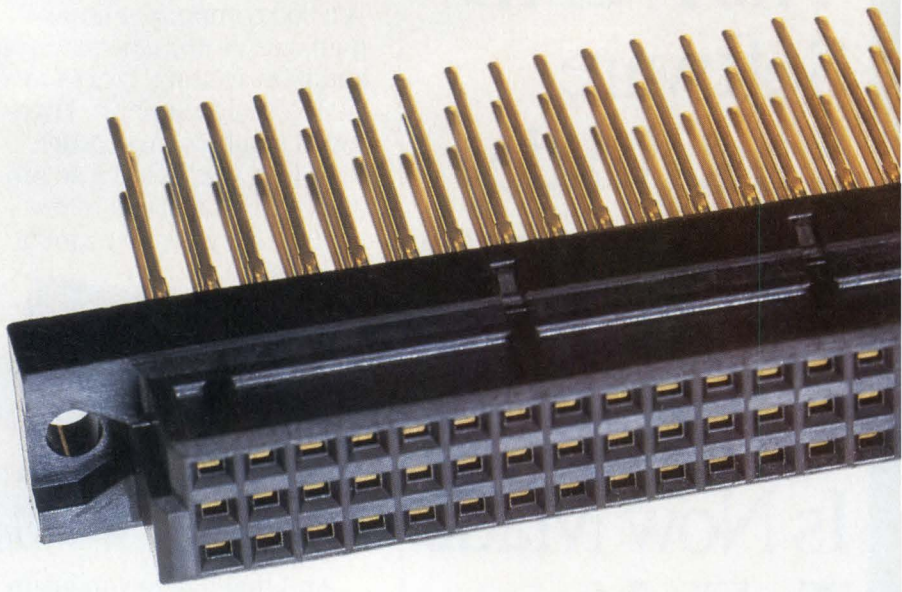

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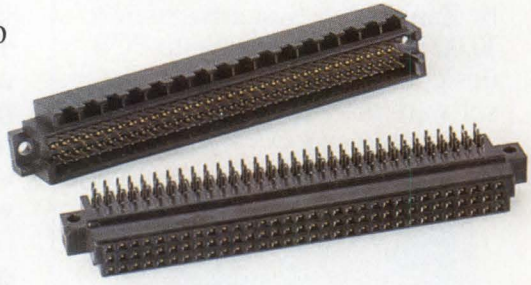

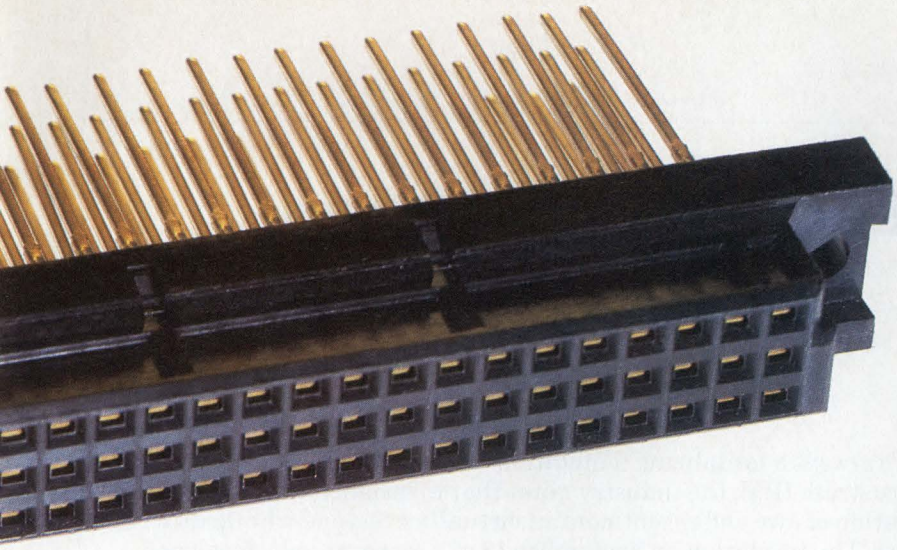

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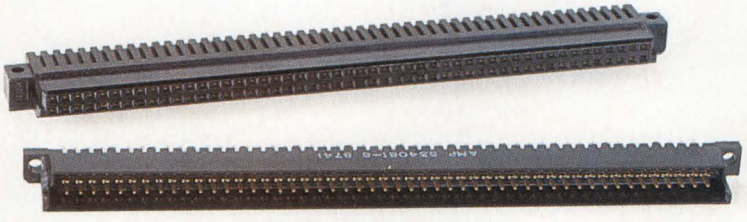

IBM takes it on the chin

When they work together, a multitude of "little guys" can have a greater impact than any one "big guy."

David Lieberman
Senior Editor

It's always a tantalizing temptation to applaud an event that's likely to frustrate IBM, the industry giant that invariably attracts a combination of awe and resentment in virtually everyone who deals with them. The revelation on September 13 of a cooperatively developed AT-compatible alternative to IBM's Micro Channel, however, was laudable for nobler reasons than for the mere bashing of Big Blue. It's a case of a number of major players in the evolution of personal computing taking control of their own destinies in a meaningful way. It's also a case of open-architecture computer companies taking the open-architecture philosophy seriously—that is, when they work together, a multitude of "little guys" can have a greater impact than any one "big guy." Though, admittedly, the PC AT bus was created by Father IBM, the kids are now completely on their own.

During the last year and a half since Micro Channel first appeared, the future of personal computing has been up in the air. With the licensing debacle, ongoing delays in OS/2, severe space and power constraints and high entry costs, Micro Channel hasn't had the look of a popular platform for tomorrow's personal machines. On the other hand, the AT's 16-bit data path plus its clumsy multimastering capabilities and other quirks made it look like a dead end. Vendors using the de facto standard 80386 microprocessor for high-end desktop systems have had to make due with proprietary solutions to make up for the AT's deficiencies—adding a private memory bus here or a kludgey facility there. The future still floated, unclear and undefined.

On September 13, Compaq, Hewlett-Packard, Tandy, Zenith, Epson, NEC, Olivetti and many others came together to direct the future toward an enhanced AT architecture based on the newly defined Extended Industry Standard Architecture (EISA) bus. Though, at press time, the technical particulars of the EISA weren't known, its intent is clear: to bridge the best of the past and future by blending compatibility with the wealth of available AT boards and the type of high-bandwidth multiprocessing capabilities that future systems will demand. Nearly simultaneously with the EISA announcement, IBM announced a new PS/2 model based on what looks remarkably like the AT bus and, in fact, uses one of the open-market chip sets. Add one more name to the list of cloners.

David Lieberman

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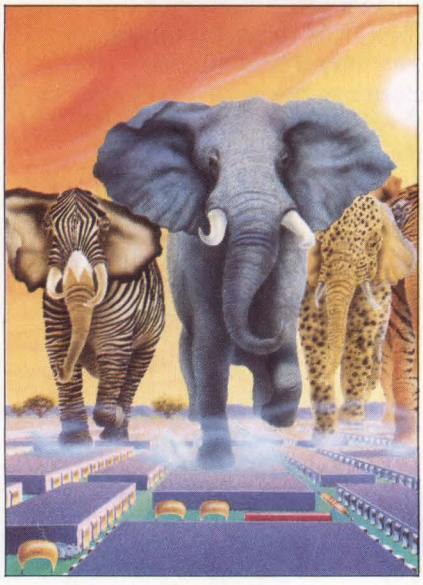

What more appropriate symbol is there for memory than the pachyderm? They're big, they're fast (despite their size), and they never forget. Who among us doesn't hold dear the childhood tale about the elephant who, about to stomp on a miniscule mouse, remembers the friend made years before when the mouse removed a thorn from the elephant's foot? Or was that a lion who had the thorn in his foot? Or a tiger? Or a leopard? It doesn't matter because our pachyderms, like ASIC memories, can be whatever we want them to be.

Cover design by Sergio Roffo

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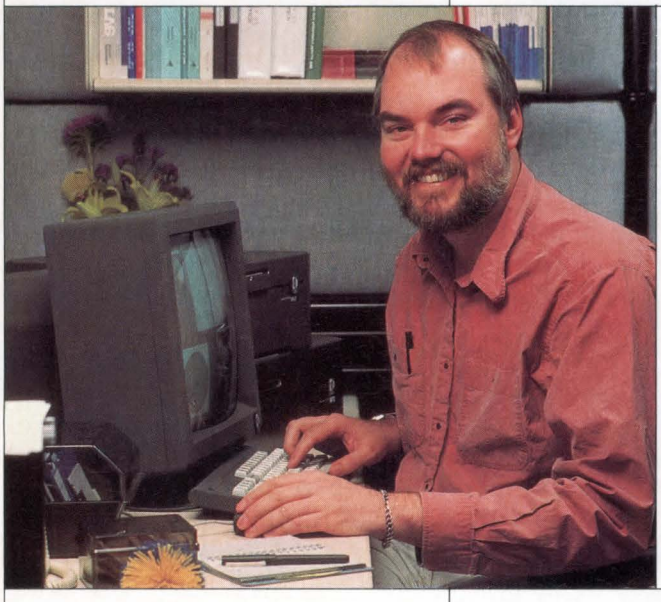
Software machine model blazes trail for parallel processing

Tom Williams, Western Managing Editor

A parallel-processing environment developed by researchers at Yale University, known as Linda, is beginning to appear in commercially available parallel-processing systems. Linda isn't a language or an operating system. It's more of a machine model and a programming methodology that could conceivably be implemented as the underlying kernel of an operating system, or built into a programming language or a hardware architecture—or some combination of the three. Linda has the added advantage of requiring relatively minor modifications to popular languages to make them Linda-compatible.

As with any maturing technology, parallel processing today is spawning plenty of activity, as well as a great deal of diversity, in terms of systems that implement parallelism. In fact, it often seems that every new idea for a multiprocessing parallel system brings with it not only a brand-new hardware architecture, but also a new software operating environment. As multiprocessing systems struggle to become commercially viable, they'll have to give an eye to standards issues to ensure portability of parallel applications.

While there are no clear-cut standards for parallelizing compilers, or even operating systems, an industry committee has been formed to address the issues of software standards for the T800 Transputer chip from Inmos (Colorado Springs, CO), an increasingly popular vehicle for implementing parallel multiprocessor systems. But it appears that before committee members can discuss language or operating system standards, they must first have an understanding of some basic underlying paradigm on which to build these standards.



One of Linda's most powerful features is its ability to replicate a process in order to create a given number of "workers," or identical processes, that can work on a large set of tuples, according to Charles Vollum, president of Cogent Research. Also, since Linda deals with processes, it can replicate as many as make sense for the application.

It could be said that the underlying paradigm on which current standards are built is the von Neumann architecture and its variations. But actually there are many approaches to hardware architectures for parallel processing, each with its own champions and detractors. The underlying paradigm for parallel systems will probably be some sort of software machine model that can find its incarnation in various forms of parallel hardware architectures. One candidate is Linda, though it's by no means the only competitor. Even those implementations of Linda that are finding their way into the market aren't yet compatible with each other.

The concept of tuple space

In addition to needing an environment that accommodates portability and can be implemented on a variety of processors and machine architectures, programmers shouldn't have to deal in detail with structural and scheduling dependencies among parallel processes. In turn, a process shouldn't be concerned with whatever other process or processes are going to use its results. And similarly, a process shouldn't have to be loaded and running at the same time results are generated in order to be able to use those results. Freed from these scheduling worries, programmers are better able to concentrate on the problem at hand.

The Linda model uncouples parallel processes from their time and space dependencies. Processes never interact directly, as is the case when messages are passed using flags and semaphores. Rather, they communicate by acting on data elements called tuples, which are kept in a conceptual shared memory called tuple space. Tuple space is accessible to all processes running on the system, and there can be as many running processes as there are physical processors. Tuples themselves are ordered sets of values that can be active data structures (processes themselves, for example) or passive data structures. Tuples are accessed by logical name rather than by address.

If a running process has data that it needs to communicate to another process, it adds that data to the tuple space. The target process need not be running at the time. When the process comes on-line, it will search tuple space for tuples that match its template. A process called (P, int I, bool B), for example, would look for a tuple with the name P that has some actual integer and some actual Boolean value.

Once the process has found the tuple, it removes it from tuple space so it can't be grabbed by any other pro-

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SOFTWARE

cess. Tuples are never altered while in tuple space. They're removed, acted upon and/or updated, and then reinserted. This makes it possible for many processes to share access to tuple space without elaborate priority or semaphore schemes to ensure orderly access to data. By definition, if a tuple is present in tuple space and a process is running that can use it, it's usable. If a running process doesn't find a tuple that matches its template, it loops until the required tuple is placed into tuple space.

■ Only four Linda operations

Linda consists of four operations: OUT places a passive tuple into tuple space; IN removes a tuple for operation by a process with a matching template; READ reads a tuple's data without removing it from tuple space; and EVAL places an active tuple (a process) into tuple space. Once the active tuple has finished evaluating, it becomes a passive tuple. By far, the most common operations are

A vehicle for parallel processing

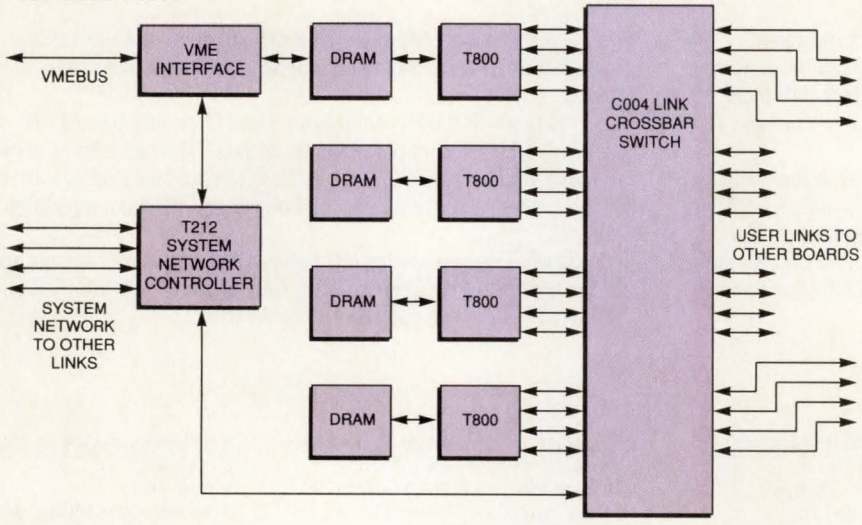
Both the Topology 1000 from Topologix (Denver, CO) and the Compute Card from Cogent Research (Beaverton, OR), which forms the basic building block of the XTM desktop supercomputer, use a similar approach in their hardware architecture. The Topology 1000, which includes four T800 Transputer chips from Inmos (Colorado Springs, CO), is based on the VMEbus. The Compute Card, with two Transputers, is based on the NuBus. But both systems can be connected and networked to an almost arbitrary number of processing nodes.

Each Transputer has its own local memory array and can communicate over the system bus as well as via serial direct memory access links that are part of the Transputer chip. Requests for data or for communications linkups are usually sent via the system bus. For data transfers between the local memories of different processors, the system establishes a DMA link by means of the crossbar switch.

The main difference between the two approaches is that the Cogent system uses a separate processor called an operator to service communications requests and set up links automatically. In the Topology 1000, on the other hand, the user has direct access to the network links via a graphics display and a mouse. The Topology 1000 user, therefore, can set up different interconnect topologies before or at run time and experiment to find the most efficient interconnect scheme for the application. In addition, the Cogent XTM is a stand-alone system, while the Topology 1000 is designed to run under Unix on a Sun-3 workstation.

In the Linda system as implemented on the Cogent system, each local processor keeps a complete copy of the list of requests for tuples, which each processor broadcasts on the bus every time it looks for a tuple. If a local processor finds that a tuple on the request list is in its local memory, it signals the operator to establish a DMA link with the requesting processor, and the data flows over that link. Similarly, if a processor stores, or OUTS, a tuple to its local memory, it checks the request list to see if there's a request pending from another process. In this way, tuple space is maintained on a conceptual and functional level even though actual tuples may be stored in separate physical locations.

TOPOLOGY 1000



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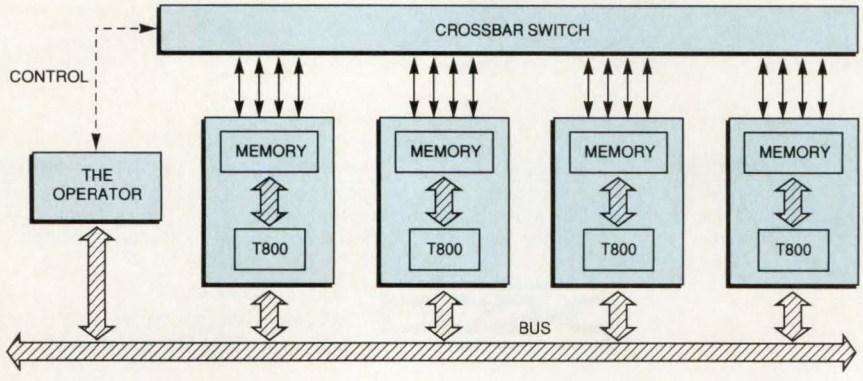

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OUT and IN.

One of Linda's most powerful features is its ability to replicate a process in order to create a given number of "workers," or identical processes, that can work on a large set of tuples, says Charles Vollum, president of Cogent Research (Beaverton, OR). Since Linda deals with processes, it can replicate as many as make sense for the application. "You can have 100 processes on one processor or 100 processes on 100 processors," says Vollum. In the former case, only one process would run at a time; the others would be blocked and pending. In the latter case, all processes could run, and the speedup would be almost linear.

"Linda is certainly the cleanest parallel software paradigm that I've seen."

—Jack Harper, Topologix

■ ■ ■

Vollum cites as an example of how replicated workers can attack a highly parallel task a ray-tracing program that computes pixel values in terms of scan lines. If each scan line is a tuple in tuple space, then a given number of copies of the scan-line ray-tracing algorithm can arbitrarily IN scan lines, compute their pixel values and OUT them back into tuple space. The master process would then IN the computed scan lines and send them to the frame buffer.

"When a worker does an IN, he doesn't know which scan line he's going to get," Vollum says. "With many processors, the easy scan lines will be done first. One processor may do only one scan line, if it's a difficult one to compute, while another may do 100." The resulting image will appear on the screen line by line in a seemingly random fashion until the entire image is completed.

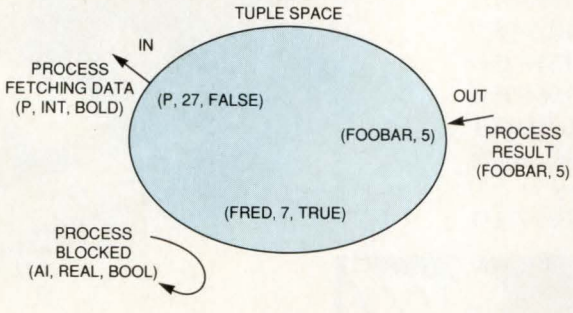
■ Two approaches to Linda

Implementations of Linda are beginning to make their way into commercial products, albeit in varying forms. Two approaches are the Cogent XTM desktop parallel supercomputer and the Topology 1000 from Topologix (Denver, CO), a plug-in board for use with Sun workstations. These approaches use similar hardware architectures based on the T800 Transputer chip, but their Linda implementations reflect different views of what users need.

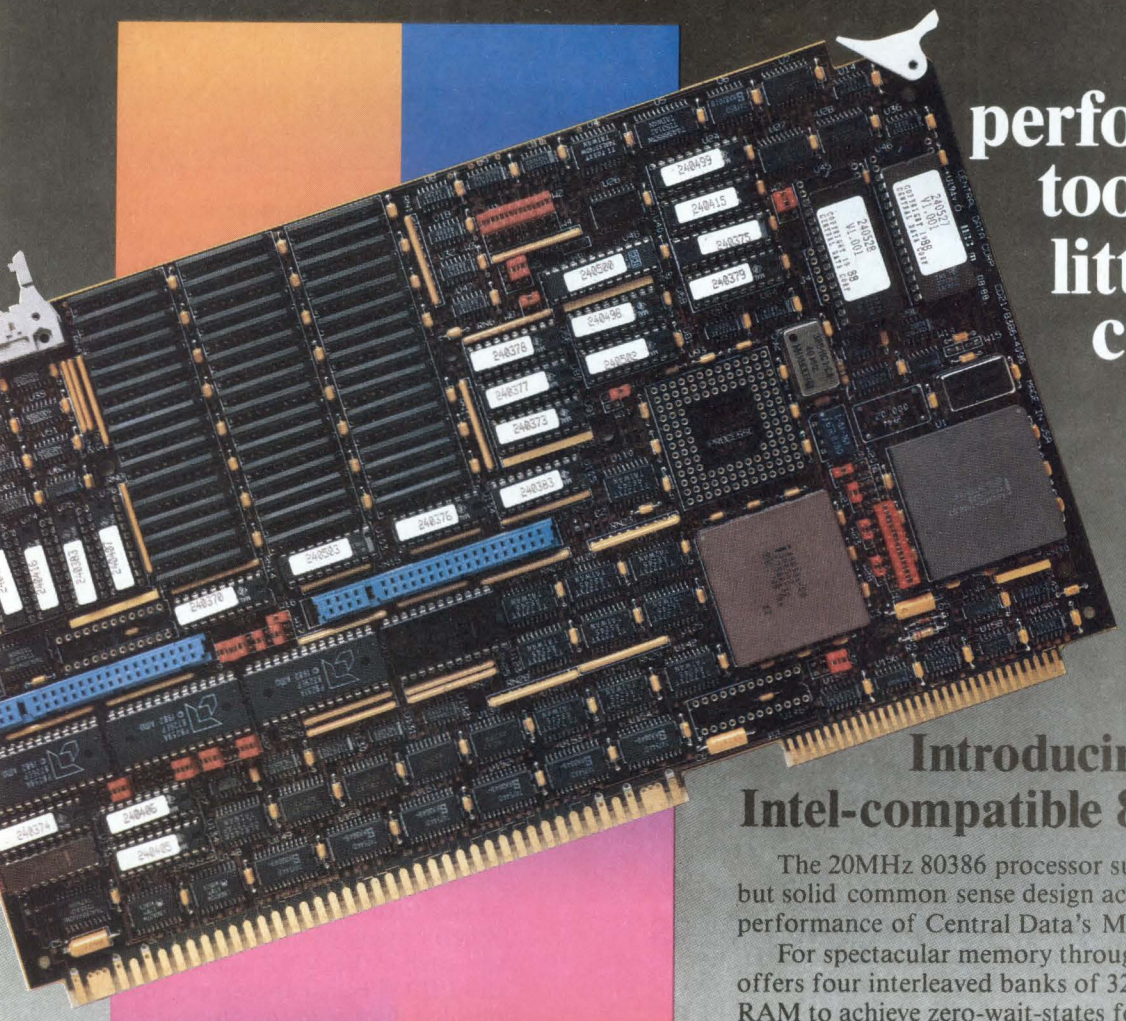
In the Cogent XTM, according to Vollum, "We pushed Linda right down to the bottom," building it into the Unix operating system kernel. Topologix took a different approach altogether in its plug-in board by embedding Linda into the Common Lisp programming language as an option. "We want to market a general-purpose machine that's not restricted to one paradigm," explains Jack Harper, president.

Embedding Linda in the operating system kernel tends to make the system a Linda-only machine, but it distributes operating system services over as many processors as are available. A request for a disk read, for example, is dropped into tuple space and is immediately grabbed by the file-server process. The file-server

THE CONCEPT OF TUPLE SPACE



All Linda processes have access to tuple space. The IN operation removes the tuple data structure from tuple space. The process storing a result has previously performed an IN on a tuple, updated it, and is OUTing it back to tuple space. The blocked process is looping because there's no matching tuple in tuple space.



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process pulls the requested data off disk and puts it into tuple space, where it's available for the requesting application process or processes. "Linda makes the operating system a distributed program that runs on all these processors, but what the user sees is old, familiar Unix," according to Vollum.

■ Built-in commands for Linda

In the Topologix approach, the Linda mechanisms for creating tuples and managing tuple space are built into the language, along with a variety of commands to invoke Linda functions. Lisp is expected to be available in the near future, to be followed by a version of C with embedded Linda functionality.

When creating Linda-capable languages (Fortran and C++) for the XTM, Cogent built in elements that fit with the syntax of the language but invoke the Linda functionality embedded in the operating system kernel. OUT in Fortran, for example, is CALL OUT. By embedding statements to do IN, OUT, READ and EVAL into what is otherwise standard source code, programmers can define tasks and tuples, and create parallel programs. Programmers can also decide exactly how many worker tasks, or copies of a task, they want to create. The number can be changed without having to recompile the program.

While keeping a range of options open for his customers to configure the Topology 1000, Harper confesses to being a real Linda fan. "When I first looked at it, I thought, 'This is ridiculous. It's too simple,'" he says. "To my mind, it's certainly the cleanest parallel software paradigm that I've seen. Linda's ability to distribute itself over an arbitrary number of processors is vital to ease of program development and debugging.

"The key is that I can build software with Linda, run it on a single processor, debug it and make it work, and then turn it loose," he continues. "And it will propagate into the parallel-processing world and will work. To me, that's just astonishing." □

COMPUTERS AND SUBSYSTEMS

Cache board delivers turbocharge to VMEbus systems

David Lieberman, Senior Editor

One of the most popular means of charging up performance in new-generation microprocessors, CPU boards and assorted controller boards is cache memory, which reduces the need to access data and/or instructions from an external source, and eliminates the wait states induced by doing so. Although caching gives a real boost to memory-intensive and/or time-critical applications, it typically increases system cost and complexity as well.

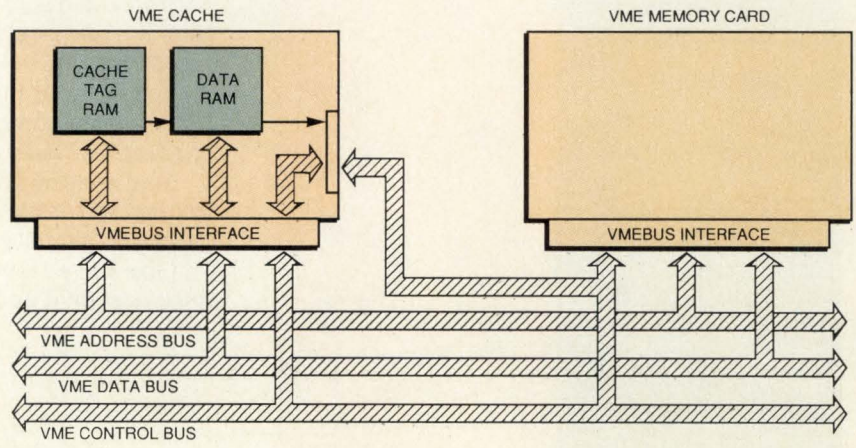
A new caching board, however, gives a cost-effective, transparent turbocharge to existing VMEbus systems without requiring CPU upgrades, hardware redesign or software reconfiguration. The VMEcache board from Ovation Systems (Great Milton, Oxfordshire, UK) provides a simple direct-mapped write-through cache system consisting of 8 kbytes of 32-bit, 35-ns cache tag static RAM and either 16 or 32 kbytes of 35-ns data cache SRAM.

The VMEcache board is installed by removing an existing dynamic RAM board and inserting the board in its place. The DRAM board is then reinserted between the slots of a backplane and reconnected through the VMEcache to the VMEbus via a special flex-circuit minibackplane. The interim position of the VMEcache lets it monitor certain signals on the bus to determine, for example, if a data request can be serviced from its own cache SRAM or if it must be passed through to the DRAM board. When requested data is resident in the cache, the VMEcache disables the DRAM board and drives the requested data onto the bus.

■ Cache doubles peak performance

The VMEcache doesn't rest content with mere caching; it also ensures that its own operations don't add delays to memory accesses and, there-

THE VMECACHE BOARD ARCHITECTURE



The VMEcache board connects an adjacent dynamic RAM board to the VMEbus via a special flex-circuit minibackplane. The VMEcache intercepts control signals to the DRAM board in order to satisfy requests out of fast cache memory whenever possible.

fore, undermine its benefits. "Very high-performance cache-tag memory lets a cache-hit detection occur within the address set-up portion of the VMEbus cycle," says Ovation's technical director, R.P. Gregory. "As a result, the data is ready to be driven onto the bus before the cycle strobes have even been asserted." The board can provide a 40-ns access to data on a cache hit, according to Gregory. "For a 16-MHz 68020, this removes three wait states involved in accessing system memory and gives the potential of one-wait-state access to memory over the bus—as fast as many CPU cards can execute from on-board memory.

"This will almost double peak performance and provide a 50 percent typical performance improvement to systems using VMEbus memory, and up to 200 percent speed improvement to systems where the bus bandwidth becomes limited by DRAM cycle time rather than by its access time," Gregory continues. "This is particularly noticeable in multiprocessor systems where total memory bandwidth becomes just as limited by the DRAM's intercycle recovery period as by the access period."

The VMEcache board maintains entries of the most frequently and most recently read memory locations. When a data request must be serviced by the DRAM board, VMEcache stores the new data for subsequent accesses. Cache entries are also made during long-word write cycles and during write cycles to previously cached locations, automatically updating previously cached data. All cache entries in the VMEcache are cleared on VMEbus reset and may also be cleared if a read-modify-write cycle occurs within the cacheable address range. "This gives the CPU the option of clearing the cache when it's using memory that's actively dual-ported independently from the cache," says Gregory. VMEcache provides hardware selection of the cacheable address range to prevent caching of noncacheable locations.

The VMEcache board, however, has no practical effect on the efficiency of write cycles. A typical CPU spends only about 20 percent of its time performing write operations, according to Gregory. "And many DRAM boards provide their own write-cycle buffering, which inherently improves write access time."

Applications for many systems

Despite its virtues, the VMEcache isn't for every system. It won't, for example, operate with VMEbus block transfer cycles and may cause coherency problems when used in conjunction with dual-ported boards. Improvements in access time will be limited for systems using memory-management units, since MMUs im-

COMPUTERS AND SUBSYSTEMS

pose an extra wait state for all accesses.

But for many existing systems, the board avoids the wait states imposed when a CPU needs to go off-board for data or code. "Since most software routines spend considerable time in loops, it's very likely that previously accessed program data will be found in the cache," says Gregory. "Studies have shown that such a cache will typically achieve a 70 percent hit rate for program execution."

The VMEcache also offers comparable performance for applications that recurrently access a limited amount of data, such as data base manipulations, according to Gregory. These applications result in more effective bus utilization—a major benefit for multiprocessing systems. The board can also benefit those CPU boards that are based on the newer microprocessors with their own on-chip caches, says Gregory, since these caches are so small that they seldom contain all the program or data space the processor requires.□

DESIGN AND DEVELOPMENT TOOLS

Standardization effort targets data management for CASE

Richard Goering, Senior Editor

Users of computer-aided software engineering (CASE) tools have a severe problem managing data when tools from different vendors are combined. An emerging standardization effort spearheaded by Atherton Technology (Sunnyvale, CA) and Digital Equipment Corp (Marlboro, MA) may soon alleviate this problem by defining a way for CASE tools to link into a consistent data-management system.

Initiated by Atherton and DEC in May, this standardization effort has since attracted participants from Apollo Computer, Cadre Technologies, Ford Aerospace, Hewlett-Packard, IBM, Index Technology, Interactive Development Environments, Interleaf, RCA, Rockwell and Sun Microsystems. The group met for the third time at the recent conference of OOPSLA-88 (Object-Oriented Programming: Systems, Languages and Applications).

The standard under discussion has been given the temporary name Atherton Tool Integration Services (ATIS). Its starting point was Atherton's Software Backplane, an integrated project support environment that provides such features as a consistent user interface, management services, a common data base and a portable operating system. ATIS focuses on management services such as version control and on data-storage issues such as concurrent data access.

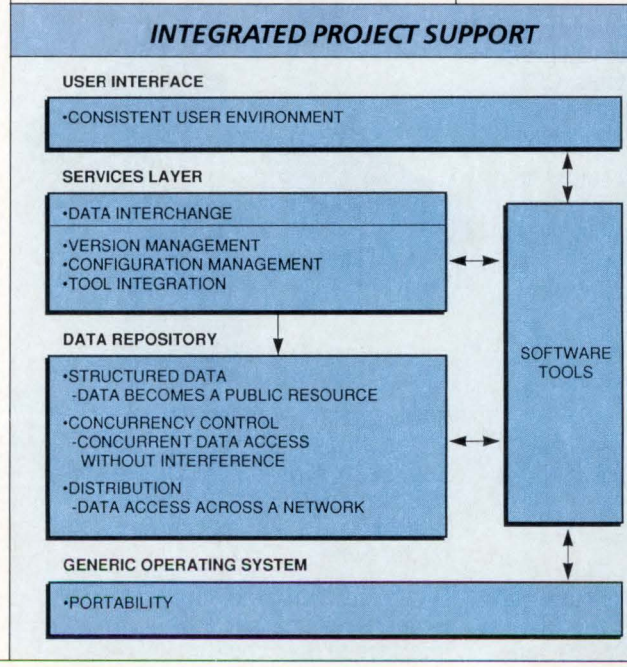
Due to input from DEC and other vendors, ATIS has evolved to the point where it now varies considerably from Atherton's Software Backplane. ATIS will be a public-domain, nonproprietary standard, and so the group that's guiding it is now looking for a name that doesn't include Atherton in the title.

■ ATIS goes beyond EDIF

The ATIS effort parallels an attempt to adapt the Electronic Design Interchange Format (EDIF) to CASE tools. By providing a neutral interchange format, EDIF will let CASE tools from different vendors exchange data. ATIS, however, allows a deeper level of integration by defining a common way of managing multivendor data.

"We're not talking about merely the ability to interchange data," says Bob Abramson, senior product manager of CASE tools at DEC. "You want to implement version control for the output of tools in a common fashion and establish relationships between the data produced by different tools. You want to go back and have an audit trail of changes made to data. And, ultimately, you want to tie in source-code modules and test programs as well."

Although not a data base standard, ATIS represents a move toward a common data-storage methodology for CASE tools. "Most previous propo-



The starting point for the standardization effort was Atherton Technology's Software Backplane, an integrated project support environment that provides a consistent user interface, a management services layer, a data repository and a portable operating system. The proposed standard addresses management services such as version control and data repository issues such as concurrency control. It does not, however, mandate a specific type of data base.

sals for integration have been at the file level," says Tony Wasserman, president of Interactive Development Environments (San Francisco, CA). "That's okay, but it's a very passive way to link tools. Here we have the idea of a shared repository through which tools can communicate."

Object-oriented approach

As currently conceptualized, ATIS fulfills two functions. First, it defines an object-oriented methodology that provides an interface between CASE tools and data-management services. Second, it establishes models for such procedures as version control, security and access control, and transaction control.

The tool interface is based on a predefined, single-inheritance hierarchy of data types. As is typical in object-oriented programming, each type has associated messages (such as open, merge and check-in), methods (pieces of code that implement messages) and properties (such as child and parent). To add a new tool, the tool integrator can either use existing types or add a new subtype. A subtype can inherit existing methods and messages, or new methods and messages can be added.

"If ATIS moves into a nonproprietary format and Sun and Apollo contribute, we'll have the best of all worlds."

—Lou Mazzucchelli, Cadre Technologies

Once a tool is added to this hierarchy, it can use an ATIS-compatible project support environment. Since ATIS manipulates objects rather than files, integration can take place at a deep level. An ATIS-based management system could, for example, define a relationship between a bubble in a diagram and a paragraph in a document.

The ability to add new types, messages and methods lets most existing tools use management services without modifying the tool. "The tool is completely blind to the fact that it's being controlled on the outside," says Bill Paseman, Atherton vice-president of technology. "The tool vendor doesn't have to make any changes." But the tool integrator must understand the interface the tool uses to communicate with the outside world.

Tool integration won't be automatic for all vendors, however. "If you don't have concepts such as object relationships, object management and navigation, there's no problem," says Lou Mazzucchelli, chairman of the board at Cadre Technologies (Providence, RI). "But if you do have these concepts, you have to figure out how your object management affects the integration tool."

In any case, a new tool that's designed with ATIS in mind can be integrated more efficiently than an existing tool. By supporting the predefined types, the tool can exchange data more efficiently and avoid duplicating storage, notes Paseman. Whatever evolves from ATIS will thus affect future tool development, and tool vendors may someday wish to label their tools as "ATIS-compatible."

Management models

ATIS doesn't mandate a specific system for implementing management services, nor does it dictate a specific type of data base. It does, however, set forth some conceptual models that describe the execution of messages. Under the current version-control model, for example, two users can open a file concurrently and update it locally. After the files are checked in, the management system merges them into a new version.

ATIS also provides several other types of models, including those for security and access control, which determine who has clearance to access data; those for naming services, which establish a file-naming methodology; and those for transaction control, which guarantee data base consistency during concurrent multiuser access. All ATIS models are under development and are subject to change.

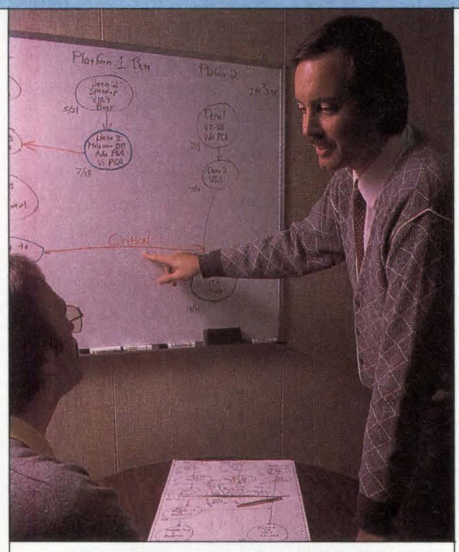
One area that the ATIS group plans to address is correspondence control, which establishes relationships between objects in the data base. Another area that will be considered is data access and communications across a network.

To develop data-management mod-

DESIGN AND DEVELOPMENT TOOLS

els, the ATIS group can draw not only on the Software Backplane experience, but on data-management systems such as the Domain Software Engineering Environment (DSEE) from Apollo Computer (Chelmsford, MA) and the Network Software Environment (NSE) from Sun Microsystems (Mountain View, CA). "If ATIS moves into a nonproprietary format and Sun and Apollo contribute their ideas, then I think we'll have the best of all possible worlds," says Cadre's Mazzucchelli.

In any case, ATIS should be able to fit on top of NSE or DSEE and provide a way for tools to use these systems. "ATIS is defining a consistent tool interface. It doesn't add functionality NSE doesn't have," says George Simons, CASE product line manager for Sun Microsystems. Since NSE, DSEE and the Software Backplane are all competing products, Simons believes that the ATIS group now needs an independent third party to assume the leadership role.



The emerging standardization effort lets existing tools use management services without being modified, claims Bill Paseman, Atherton Technology's vice-president of technology. "The tool is completely blind to the fact that it's being controlled on the outside," he says. "The tool vendor doesn't have to make any changes."

■ Other standardization efforts

The ATIS effort may complement other standardization efforts. The Portable Common Tool Environment (PCTE), which is strong in Europe, is an attempt to develop a portable environment in which software development tools can operate. The Information Resource Dictionary Standard (IRDS), a project of the National Bureau of Standards, concerns a common tool interface to data dictionaries. Now established as a standard in electronic CAE/CAD, EDIF will probably define the data-interchange standard for CASE. And the prevalence of the X Window System will help set a user-interface standard.

The net effect of all these standards will help create truly integrated software development environments. But standards only work if there's widespread cooperation among tool vendors, workstation vendors and users. "For a standardization effort to succeed, people need to talk to each other," says Atherton's Paseman. □

Frame builder and back annotator link CASE to development tools

Richard Goering, Senior Editor

Because computer-aided software engineering (CASE) tools are seldom linked to code development or testing, the transition from CASE to compiled code is usually tedious and error-prone. Two new products from Microcase (Beaverton, OR) attack this problem, however, by tying the Teamwork CASE tools from Cadre Technologies (Providence, RI) to the rest of the software development cycle.

The first of these tools is the Source Frame Builder, which can automatically translate a Teamwork structure chart's module specifications into C source file frames. The other tool, the Back Annotator, attaches performance parameters from Microcase's Software Analysis Workstation to design objects in Teamwork SD (Structured Design). "We're unifying the front-end design tools, which were islands of automation by themselves, into the microprocessor development environment," says Caine O'Brien, Microcase CASE products marketing manager.

Since late September, Microcase has been a value-added reseller of Cadre Technologies' Teamwork tools. Microcase also sells compilers and source-level debuggers from Microtec Research (Santa Clara, CA) and in-circuit emulators from Microtek International (Hsinchu, Taiwan).

> ***"We're unifying the front-end design tools into the microprocessor development environment."***
>
> *—Caine O'Brien, Microcase*

■ ■ ■

Microcase's Software Analysis Workstation is a nonintrusive analysis tool that's hosted by the IBM PC. By combining all these tools with the Source Frame Builder and the Back Annotator, Microcase is able to offer an end-to-end solution to embedded software developers.

■ Not code generation

The Source Frame Builder shouldn't be confused with automatic code generation, which is available only in a very limited sense. A source frame is a building block into which the user can later enter the code body. To build the frame, the Source Frame Builder first examines the data flows in the structure chart constructed with the Teamwork SD tool. It looks up these data flows in the data dictionary and translates them into C declarations.

The Source Frame Builder creates a header for each module in the structure chart, and it then inserts the declarations according to the user's instructions. The header coupled with the declarations constitute a frame. If a user describes his modules in C, as opposed to pseudocode, that code will be installed in the frame

automatically.

The user can keep the code in the module specifications to ensure that the design matches the code. "But," says O'Brien, "if the customer is already using version control, he probably won't choose to keep his code in the module specification because, at this time, we don't have hooks into version control."

priate objects—which could be module specifications or data dictionary entries—in Teamwork SD. This lets a user, for example, select a module specification in Teamwork SD and review the performance characteristics of that module.

Since code has already been developed, back annotation is valuable primarily for documentation and maintenance. "Test information is available in the same data base as the design itself. This enhances some of Teamwork's traceability features," says O'Brien.

"If you choose to maintain code in Teamwork module specifications, you can have the design, the source code and the performance information all in one data base," he adds.

The Source Frame Builder and the Back Annotator are sold as a package for $1,995. They'll be available on Sun-3 workstations at the end of this month and on Sun 386i workstations in December. □

SOURCE FRAME

```
#define MAXVAL = 100;

typedef double        operand_t;

static int            stack_pointer = 0;

static operand_t      stack_values[MAXVAL];


/*
 ************************************************
 *   Procedure: pop
 *   Synopsis:
 *      Remove the top value off the stack and return that value.
 *   Attributes:
 *      DEFN_FILE = calc_stack.c[File];
 *      STRUCTURE_CHART = /mdt1/calc_example/calc_main[SC];
 ************************************************
 */
pop ()
(
      operand_t                  operand;

      if (stack_pointer > 0)
      (
          return (stack_values[--stack_pointer]);
      )
      else
      (
          fprintf (stderr, "error: stack empty \ n");
          clear ();
          return (0);
      )
)
```

The Source Frame Builder from Microcase converts data dictionary definitions into C declarations, as shown in the top portion of this source frame. The comment following the /* designator is taken from the module specification. If the user describes modules in C, that code can be installed in the source frame automatically, as shown in the bottom portion of the frame.

■ Documenting test data

The Back Annotator comes into use after code has been compiled and is running on the target system. It takes advantage of two capabilities of the Software Analysis Workstation: code coverage and performance analysis. Code coverage defines the portions of a program that have been executed in real time during dynamic test runs. Performance analysis measures how much time has been spent executing various software modules.

The Back Annotator lets users attach code-coverage and performance-analysis measurements to the appro-

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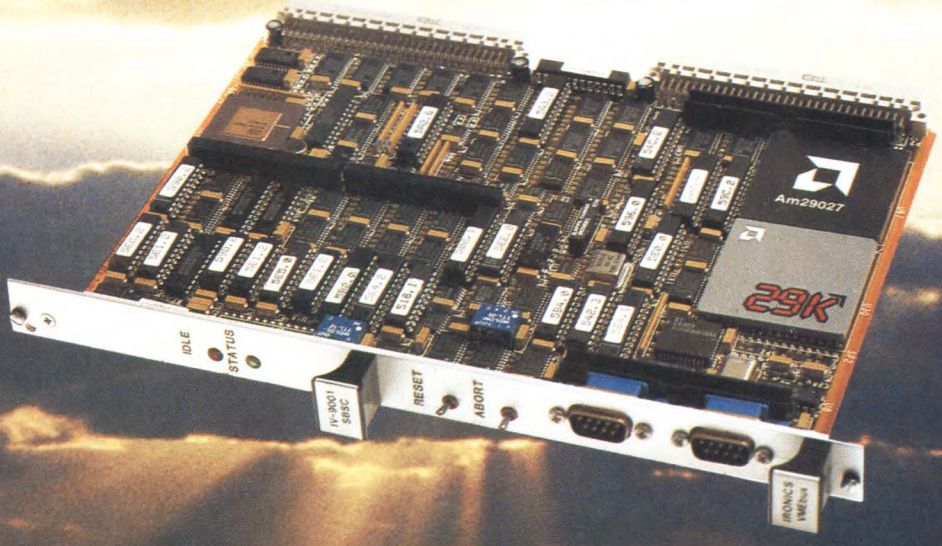

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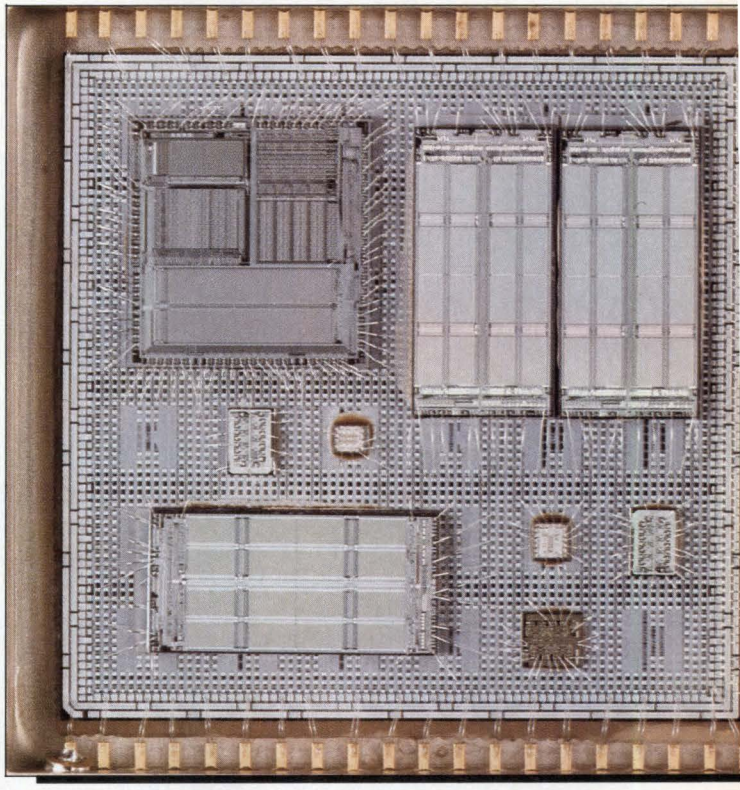
CIRCLE NO. 20

Innovative packages emerge to carry faster, denser chips

Designers turn to VSOPs, TAB-based packages, multichip modules and programmable connection networks to support today's increasingly complex ICs.

Art DeSena
President, ADS Associates



Mosaic Systems developed its 1-in.² Programmable Silicon Circuit Board (PSCB) to handle today's speed and density requirements. An electrically programmable silicon substrate and connection network, the PSCB can mount components at 10 times the density of a two- to four-layer printed circuit board.

During the past decade, the role of electronic packaging in most engineering organizations has grown from a relatively minor support function to a major area of responsibility. A decade ago, the packaging effort accounted for about 5 percent of the total component design effort. But with today's technology advances, packaging design accounts for as much as 30 percent of the total effort.

"Building 25-mil packages and developing a family of products to go into fine-pitch packages entails extensive package design effort. The materials used in the package, the handling equipment from lead trim all the way out through the test area, and even the manner in which devices are packaged for shipping are becoming more and more critical," explains Charlie Hewitt, director of domestic assembly operations at Harris Semiconductor (Melbourne, FL).

At the system level, more complex functional and performance requirements dictate the need for more advanced microelectronic technology, which results in an increase in speeds, component densities, interconnect densities, power densities and design costs. To keep pace with these higher speed and higher power devices, the development of more sophisticated packaging techniques is necessary; thus, the success of future systems depends largely on the competence and forcefulness of device and system packaging engineers.

These advanced technologies require new chip carriers that can handle increased IC pin counts. They also require structures that can accommodate the smaller 3- to 5-mil spacing between pins. Manufacturers of multilayer interconnect substrates and/or printed circuit boards are developing new manufacturing techniques that use new materials to produce assemblies that can cope with the smaller, higher density, higher speed and higher power devices. Techniques for dissipating the heat generated by these high-speed and high-power components must be considered early in the design cycle.

Furthermore, the industry's move from LSI to VLSI to the Department of Defense's VHSIC (Very High Speed IC) I and II programs has brought

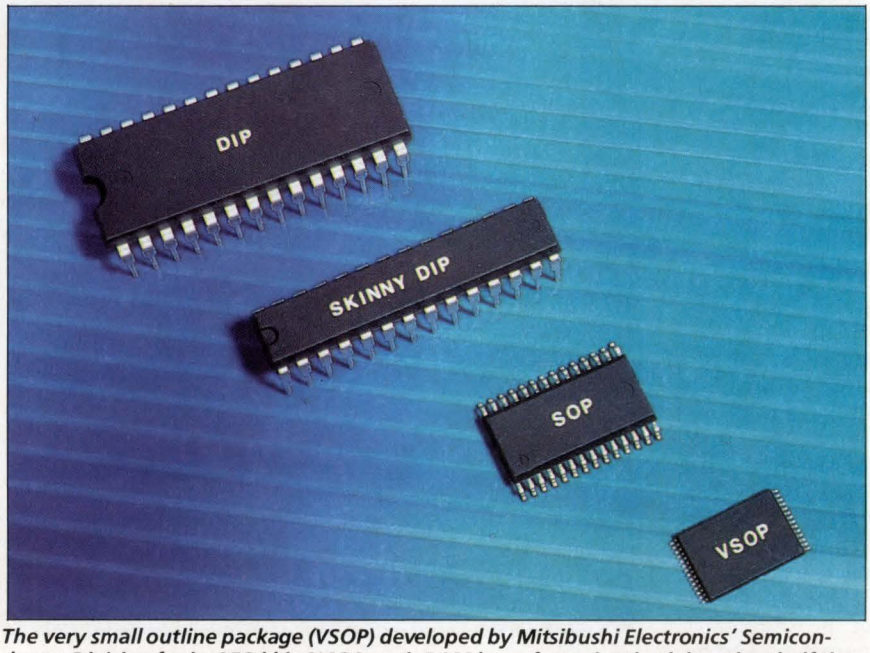
about an even greater increase in packaging requirements. The equivalent-gate count per chip has gone from 1,000 for LSI to over 50,000 for the VHSIC II program and is still increasing. Similarly, the die size has increased from LSI's 100 mils to 500 mils for VHSIC. There are typically 16 to 28 I/O pins for LSI chips, 28 to 60 pins for VLSI and 200 to 400 pins for the VHSIC program. Clock rates have also seen a dramatic increase, from 1 to 5 MHz for LSI to 50 to 100 MHz for VHSIC. In addition, the typical power dissipated in an LSI chip is between 0.5 and 1 W, while the power that must be dissipated in a VHSIC chip ranges from 4 to 6 W.

"We're still looking very heavily at 68-, 84-, 120- and 144-lead pin counts on pin grid arrays. And it's going to jump up to 180," notes Norm Allard, manager of marketing and sales at General Electric Ceramics (Chattanooga, TN). "We're also looking at 220- and 240-lead pin counts, which seem to be the next group coming." GE Ceramics produces multilayer ceramic packages, substrates and chip carriers. The chip carriers are available in multilayer and single-layer designs with standard lead counts from 16 to 84 I/O pins and centerline lead spacing of 40 and 50 mils.

Recently, the Semiconductor Division of Mitsubishi Electronics (Torrance, CA) announced a very small outline package (VSOP) version of its high-performance, 256-kbit CMOS static RAM. With the VSOP having a footprint less than half the size of a standard 28-pin small outline package (SOP), designers can pack twice as much memory into system packages in which space is critical. The VSOP also comes in a reverse version, which is a mirror image of the normal pin-out and allows for ease of design for double-sided boards.

■ New package concept uses TAB

A new package concept, Tapepak, uses tape automated bonding (TAB) technology. Tapepak has been developed by National Semiconductor (Santa Clara, CA) to meet the needs of very high density packaging. Two major innovations in packaging technology account for Tapepak meeting the latest requirements, according to Jim Walker, surface-mount packaging marketing manager at National. "The first innovation is a protective carrier ring that surrounds the leads outside the actual device," claims Walker. "It's molded at the same time as the package body and provides protection for the leads through handling and board manufacturing processes. The carrier ring also supports the outer test points of the package. The second innovation is a metal tape that's used for the leads attached to the die, the external leads and the expanded center test points at the edge of the outside ring."



The very small outline package (VSOP) developed by Mitsibushi Electronics' Semiconductor Division for its 256-kbit CMOS static RAM has a footprint that's less than half the size of a standard SOP and is drastically smaller than a Skinny DIP or standard DIP. This reduced size lets designers pack much more memory into a system package.

The Tapepak component packaging technique was developed to satisfy the technology demands of existing and future surface-mount devices, with their smaller dimensions and higher densities. It uses TAB technology to produce a low-cost, high-density and highly damage-resistant package with improved reliability and testability features not found in present-day surface-mount devices. Existing surface-mount devices, mainly SOPs and PLCCs, provide solutions for lead counts up to 84 leads. But above 84 leads, the large size of the PLCC presents difficulties in surface-mount assembly.

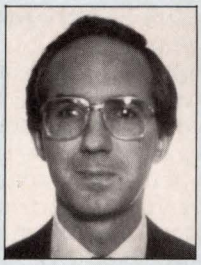
Other high-density packaging alternatives, such as chip-on-board, are space-effective but difficult to automate. The plastic quad flatpack has handling and test problems, while the pin grid arrays are large and can't be surface-mounted.

Tapepak evolved as the logical way to use die-on-tape in a testable, highly reliable configuration in which the attachment to the board didn't depend upon the die-bonding process. Tapepak uses tape to connect to the die, provides the leads to be attached to the printed circuit board and provides test points in a ring surrounding the package.

Tapepak uses a 2-oz (56 gm), 0.028-in. (0.07 mm) thick, etched single-layer copper tape as the leadframe, bonding medium and test point medium. During preparation, the copper tape leadframe is etched to produce bumped fingers on the inner lead area that correspond to the bonding pads on the target die. A finished wafer is prepared for Tapepak by forming a multilayer metallic cap over the bonding pads on the dice. The copper tape leadframe is then thermal-compression-bonded in a single "gang-bonded" step. This die-on-tape strip is molded to produce the package and its protective outer ring simultaneously.

Very high lead counts are possible with Tapepak. Existing packages have a 20-mil pitch and can accommodate 220 leads. National is planning future packages that have 15-mil and 12-mil pitches that can accommodate up to 284 and 360 leads, respectively. Also significant are the test points on the outer protective ring. These test points flare out from the 20-mil centers of the internal device leads to 50-mil centers, making

How to select the right heat sink



High-speed ECL gate arrays, dissipating approximately 1 mW/gate, have required heat sinks for a number of years. Even a 2,500-gate device, which dissipates 2.5 W, needs a heat sink. And now high-performance CMOS gate arrays, with their increased size, density and speed, are also requiring heat sinks. A 10,000-gate CMOS device dissipates 2 W at 16 MHz, and a 50,000-gate device dissipates 10 W at the same frequency—and the heat generated in each device increases proportionately as the operating frequency increases.

ECL and CMOS gate arrays with high gate counts are generally packaged in pin grid arrays (PGAs), which provide a large number of I/O pins per printed circuit board surface area. Heat sinks are either adhesive-bonded or mechanically attached to the top mounting surface of the PGA. The power dissipation level, the airflow and the physical volume available determine the heat sink's configuration. In most low-power cases, a heat sink with a wide margin of safety is selected, since it will easily fit into the space available.

But as power dissipation increases, designers must select a heat sink that will dissipate the required wattage within the space and airflow constraints. By examining the thermal performance of heat sinks in various mounting, space and airflow configurations, the right heat sink can be selected. Three types of aluminum heat sinks were evaluated by the test lab at Thermalloy (Dallas, TX): round and square multi-fin omnidirectional heat sinks; extruded heat sinks; and pin-fin heat sinks.

The thermal performance of a heat sink is its thermal resistance value, generally given in °C per watt (°C/W) dissipated from the heat sink. A lower resistance value indicates better thermal performance.

A 149-pin ceramic, cavity-down PGA (15-× 15-pin array) with appropriate heat sinks was selected by Thermalloy as the thermal model because it's the most commonly used PGA that requires a heat sink, particularly at high-power levels. The range of heat sink thermal resistance requirements for low power (1 to 2 W) is 76° to 36° C/W; medium power (2 to 8 W) is 36° to 2.4° C/W; and high power (8 to 18 W) is 7.4° to 0.8° C/W.

Comparing heat sinks

Omnidirectional heat sinks with various configurations of fin spacing were evaluated. Since wider fin spacing improves performance in natural convection or lower air speeds, the heat sinks with only two or three fins and 0.125-in. fin spacings had the better performance. The heat sinks with four fins had more surface area, but because they had smaller (0.031-in.) spacings between fins they didn't have the better performance until the air speed was increased to 600 ft/min.

For high-power levels, a pin-fin heat sink with impingement cooling is needed for most applications.

Another factor to consider with small fin spacings is blocking of airflow to downstream heat sinks or components. In cases where it matters how much airflow is being blocked, wider fin spacings should be used regardless of the air speed.

Comparisons of round and square omnidirectional heat sinks revealed that a square heat sink will provide a 5 to 10 percent improvement in performance over a round heat sink with similar dimensions.

An extruded heat sink and a pin-fin heat sink were also tested in various configurations, each one having a mounting base of 1½ × 1½ in., a height of 0.65 in. and a base thickness of 0.2 in. The extrusion had 10 fins; the pin fin was formed by milling cuts in the extruded heat sink, making a 10- × 12-pin array.

The heat sinks were tested in natural convection, conventional flow and impingement. (In impingement cooling, the airflow is into the face of the heat sink in a direction perpendicular to the mounting surface.)

The pin fin had better thermal performance in all configurations, with the greatest percentage increase over the extrusion occurring in impingement cooling. Comparisons to omnidirectional heat sinks, meanwhile, revealed that while the pin-fin heat sink had only slightly better performance in convection and conventional forced convection, it had 40 to 50 percent better performance with impingement cooling.

Selection criteria

For low- or medium-power dissipation levels, an omnidirectional heat sink or an extruded heat sink is adequate. Natural convection may be used for the low-power levels, while forced convection is needed for most medium-power levels. But for high-power levels, a pin-fin heat sink with impingement cooling is needed for most applications. The size of the heat sink depends on the semiconductor junction temperature and the ambient temperature as well as the power level to be dissipated.

There are many trade-offs that a designer should consider when selecting a heat sink. For example, a pin-fin heat sink is more expensive than both omnidirectional and extruded heat sinks, so it should be chosen only when the additional cooling performance is needed. An omnidirectional heat sink has an advantage over an extruded heat sink, since the orientation of the airflow isn't critical in omnidirectional heat sinks. And because a round omnidirectional heat sink is less expensive than a square one, a square omnidirectional heat sink should be used only when the performance requirements warrant it.

Since heat transfer depends on many variables in a packaging system, designers are advised to use heat sink thermal resistance values as only a first step in determining the thermal performance of their systems. A thermal test performed under actual operating conditions is essential before committing to a final heat sink design and cooling configuration.

Marvin Moore, MME, chief engineer, Thermalloy

them compatible with existing surface-mount equipment such as that used for SOPs and PLCCs.

The interconnection package

As VLSI and VHSIC technology find their way into system designs, the chip carrier and other component packages such as multichip modules and multilayer printed circuit boards will play an ever-increasing role in the size, speed and performance of electronic systems. With rise times in the sub-picosecond range for ECL and low nanosecond range for high-speed CMOS, interconnecting signal paths between ICs can no longer be treated as a simple mechanical connection. They must be considered as transmission lines, where characteristic impedance, crosstalk and propagation delay become essential parameters determined primarily by the geometric layout of, and the materials used to construct, the interconnection assembly and package.

Ever-increasing demands, therefore, have been placed upon interconnect manufacturers to develop new packaging techniques. Because of the emergence of gallium-arsenide, microwave and ECL technologies, controlled impedance matching is required to ensure the integrity of high-frequency performance.

A typical method of accomplishing a high-density design is to eliminate the relatively bulky IC package. Bare chips are combined with other active and passive components on a substrate to form a compact custom hybrid circuit. Thick- or thin-film interconnections are used to interconnect these circuits, providing a high level of interconnection density. And recent developments in polyimide/copper interconnection substrates have provided the ability to interconnect several high-lead-count VLSI chips while still maintaining signal and noise integrity.

In the late 1970s, the Microtec division of Augat, which has since been purchased by Rogers (Chandler, AZ), made a major commitment to serve the high-frequency performance needs of the packaging interconnect industry. Based upon polyimide multilayer technology, an additive process from Microtec gives the design engineer a degree of performance in interconnect circuitry that works well with high-frequency devices, such as GaAs and ECL. The process that Rogers uses to build its Microtec Multichip Modules is unique, based upon fully sequential lamination of polyimide and the electroplating of conductors. The electroplating of conductors is different from the thin-film polyimide process that uses sputtering or vacuum deposition of copper, according to Steve Lockard, market development supervisor at Rogers.

A typical method of accomplishing a high-density design is to eliminate the bulky IC package.

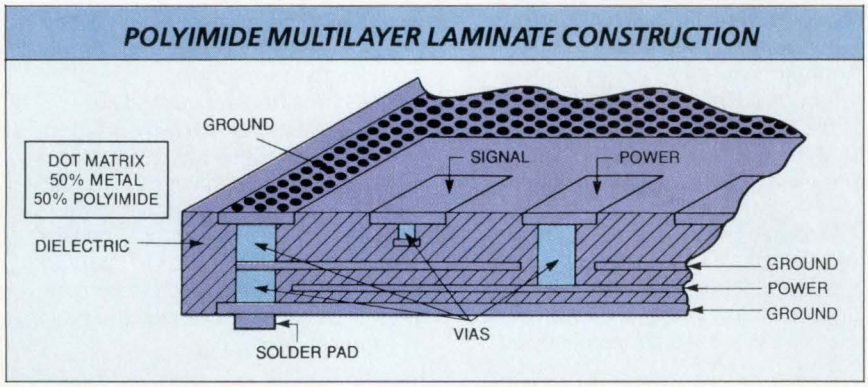
■ ■ ■

"It's not that we're using polyimide that's unique; it's the combination of sequential laminating and the electroplating of copper," says Lockard. "It offers us the ability to create very fine lines while still being able to use thick copper, which means that in ECL applications, resistive drop through conductors aren't too severe, making the electrical characteristics better. It also helps the heat-transfer capabilities of the module."

Vias (through-holes that interconnect various layers in a multilayer printed circuit board) can be created that start and stop anywhere as required within the multilayer structure. Some of those vias can go from the top to the bottom of the module and can be thermally conductive vias to a metalized backer for better control of heat management. Heat transfer is especially critical in high-speed CPU modules that use a lot of ECL circuitry and produce very high wattage per module. One very important heat-transfer issue is how to efficiently dissipate the heat generated.

The Microtec process involves combining sequential layers of polyimide (insulating layers) with plated fine line copper conductor and via interconnect layers, which requires special high-resolution artwork to photoimage the complex multiple patterns. Conductors are then electroplated to specific line widths and thicknesses, and locating copper via layers are created for layer interconnect and/or thermal heat sinking. The materials are permanently fused by heat and pressure at each added layer (lamination). Extremely fine traces can be developed using the Microtec process, where 0.002-in. lines with 0.003-in. spaces can be made for surface layers and 0.004-in. lines with 0.006-in. spaces can be made for buried layers, permitting substrate miniaturization and reduced crosstalk.

Another unique feature of Microtec's additive process is that conductive walls can be built to surround a signal line. According to Lockard, these walls can be brought up to the ground plane layers and can create a rectangular coax around the signal line, insulating the signal from any outside interference.



Using Microtec's additive process for constructing polyimide multilayer laminate boards, vias can be developed that start and stop between any combination of layers. Selected vias that go from the top to the bottom of the module are thermally conductive for better control of heat management.

Multichip modules improve ICs

Constantly seeking ways to increase the functionality and shrink the size of the products they build, designers are exploring the use of multichip modules to interconnect ICs. The ICs are then mounted on a printed circuit board to achieve smaller size and improved functionality. "Many designers have incorporated multilayer, dual-sided, surface-mounted boards

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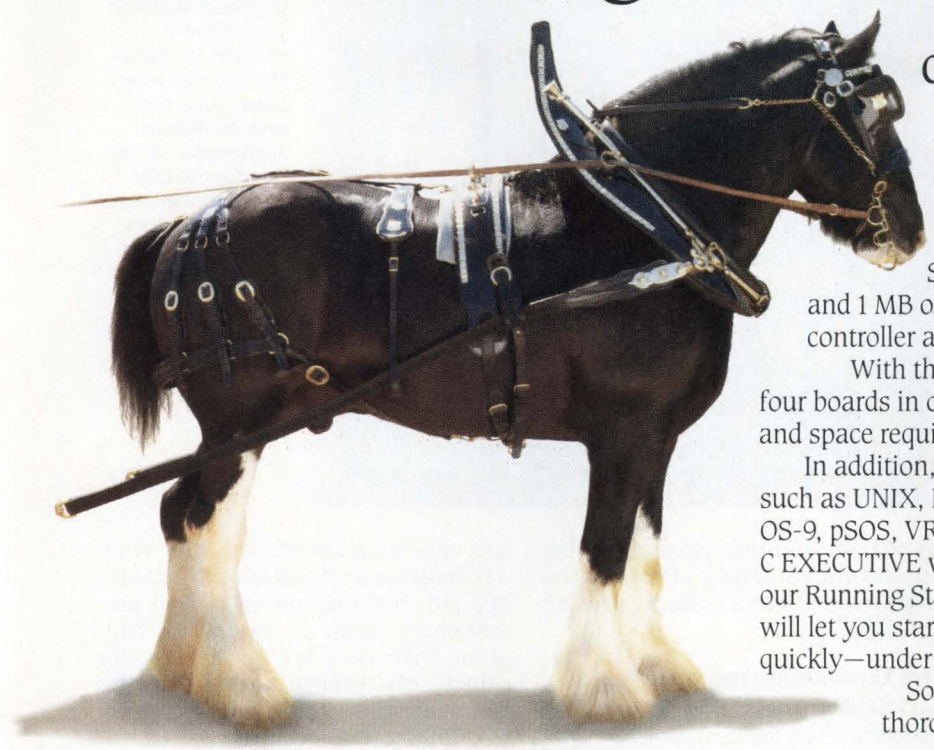

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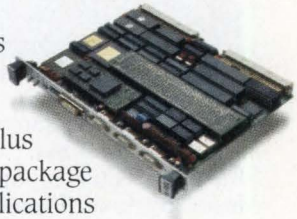

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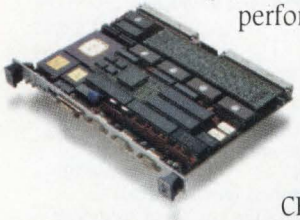

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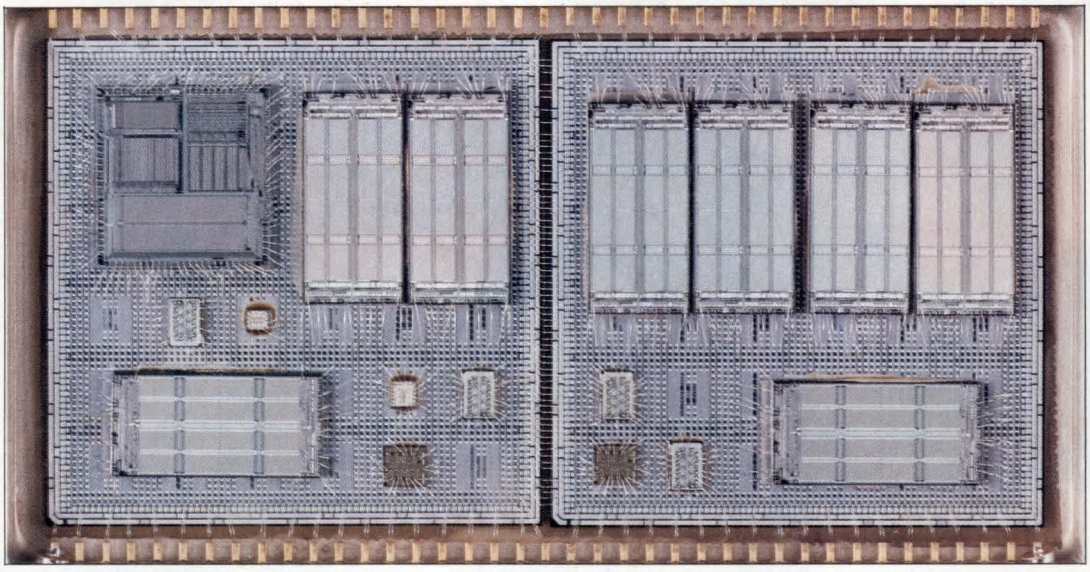

By connecting two of its 1-in.² Programmable Silicon Circuit Boards through its multichip module interconnection technology, Mosaic Systems has developed a memory board that includes 1 Mbyte of cache memory, a 32-bit microprocessor and memory control chips.

as the solution for some of their interconnect problems," notes Steve Sharp, director of applications at Mosaic Systems (Fremont, CA). "The cost for these boards can be from $10 to $20 per square inch and the development cycle can be very long. The use of multilayer ceramic hybrids is a possible solution, but they're also costly, have long manufacturing cycles and can't realize the component densities needed."

Mosaic Systems has developed the Programmable Silicon Circuit Board (PSCB), a proprietary high-density interconnect system, to replace printed circuit boards, hybrid circuits, surface-mount interconnect technology and other interconnect solutions. The PSCB is an electrically programmable 1-in.² silicon substrate and connection network. The small size and high density of the PSCB make it ideal for applications where size and speed are critical. "In fact, the PSCB can mount components at 10 times the density of a conventional two- to four-layer printed circuit board and three times the density of a six- to 10-layer ceramic substrate," claims Sharp.

In addition, the PSCB lets manufacturers drastically reduce high start-up costs and lengthy turnaround times, since customized boards are created by electrically programming off-the-shelf parts.

Mosaic's PSCB eliminates up to 95 percent of the discrete wiring and mechanical connections required by conventional circuit boards, since the PSCBs replace the fixed wire connections within the silicon and eliminate the need to add distributed high-frequency decoupling capacitors because of the dielectric effects of the insulation between voltage, ground and signal planes.

■ No termination resistors

The PSCB's use of "lossy lines" eliminates the need for termination resistors. Under the lossy line principle, the inherent line resistance is used as a built-in series terminator, eliminating the need to include separate resistors for termination. For the short distances across PSCBs (a few millimeters), attenuation effects are insignificant, so signal propagation delays are effectively the same as for loss-less lines. The elimination of ringing and signal reflection compensates for any additional delays.

The PSCB's substrate consists of four internal metal layers and a surface layer of bonding pads, with each metal layer separated by an insulating dielectric layer of silicon dioxide. The two bottom layers are solid power and ground planes permanently connected to corresponding power and ground pads on the substrate surface. The interconnection network is formed by depositing a matrix of microscopic signal lines on the silicon substrate, with the two layers of signal lines at right angles to each other. The points where the two meet are potential vertical signal paths.

These crossover points are called programmable vias because designers can change their conductivity from open circuit to short circuit by applying a programming voltage. Each 1-in.² PSCB contains 101,061 programmable vias composed of amorphous silicon, a material that has very high resistance. But when a voltage above a certain threshold is applied, the amorphous silicon permanently forms a crystalline filament with very low resistance. By selectively programming specific vias, electrical paths can be created to implement a circuit.

Bare dies, rather than packaged ICs, are then bonded to the surface with epoxy and connected to the board with traditional ultrasonic wire-bonding techniques. The bonding pads on the PSCB let the designer cluster ICs, reducing signal-line delays and increasing circuit speed. After wire bonding, the PSCB can be bonded into an industry-standard, large-cavity package. □

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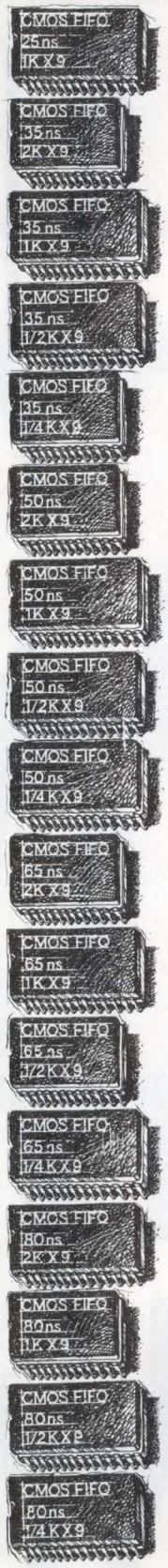

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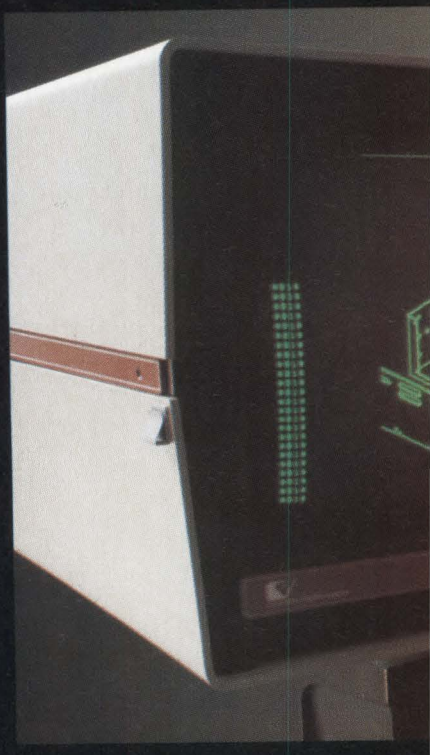

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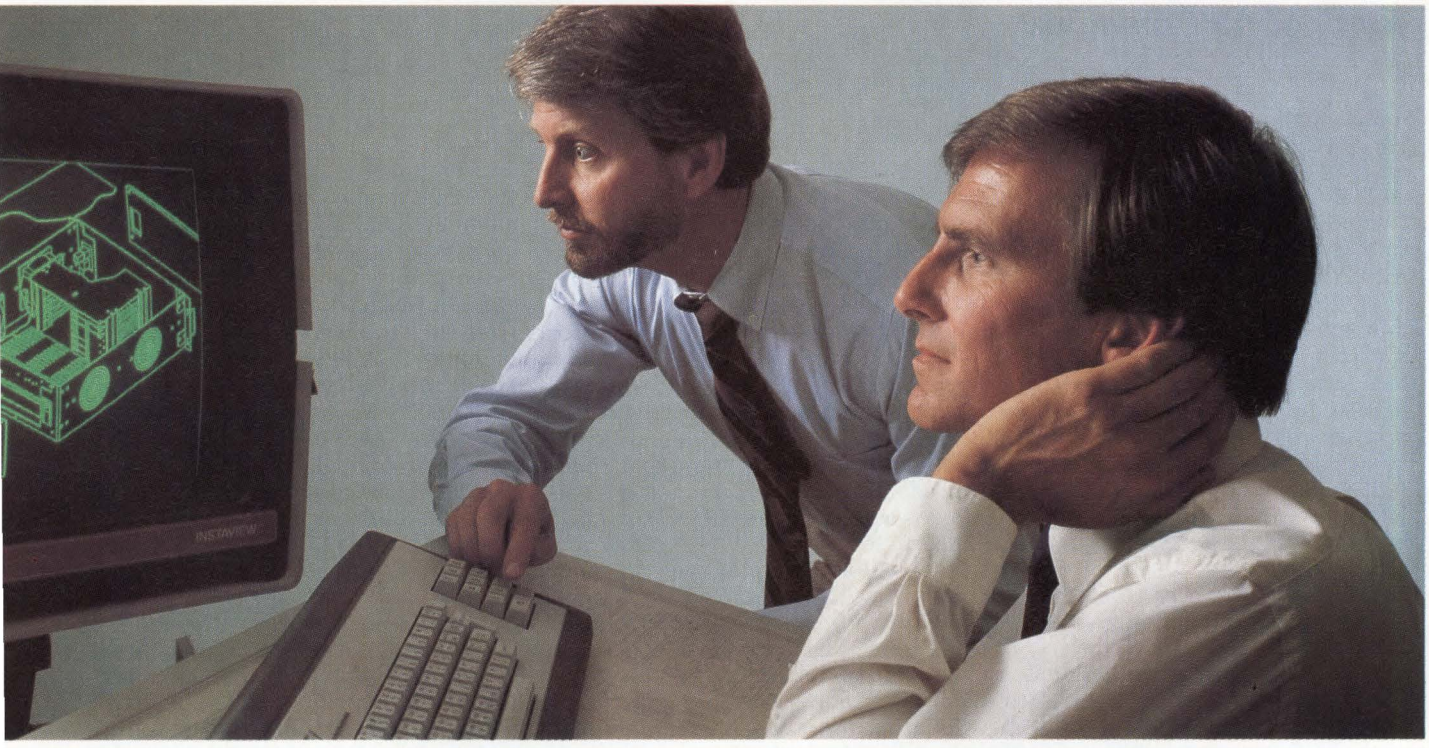

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ASIC memories: bigger, faster, and customized

Warren Andrews, Contributing Editor

The goal? Develop super-performing specialty memories. The strategy? Revamp cache, FIFO and SRAM architectures, and design entirely new forms of ASIC memory.

Memory architecture and the associated processor-to-memory interface are rapidly becoming the most critical aspects of system design. Driven by increasingly faster microprocessor cycle times, by a wide spectrum of reduced-instruction-set computers advancing system performance, and by the use of multiple processors to speed up applications, memory subsystems have taken on a totally new complexion. In a time when many hardware designs—buses, operating systems, peripherals and interfaces—are becoming standardized, memory architecture is one of the remaining few areas where designers are still able to differentiate their products from the masses. As a result, new, clever architectural innovations in the process-to-memory interface are providing significant performance boosts for users.

Fueling the need for new memory architectures, entire families of application-specific or specialty memory chips are emerging. These include memory with on-chip intelligence and control logic; multiported memory; and buffer memory that resembles a bus interface. The rule behind the design of these specialty memory chips is simple: The faster, the better. In some cases, entire memory subsystems have been defined on a single chip. And to provide flexibility, designers are also beginning to incorporate programmable features into these subsystems.

Heading the list of new specialty or ASIC memory products are cache tags; first-in, first-outs (FIFOs); data caches; dual and multiported RAM; and registered or synchronous static RAM. Though the names of these products sound familiar, today's versions bear little resemblance to their precursors of only a few years ago. FIFOs, for example, are no longer simple shift registers, but have evolved into complete storage subsystems. They'll soon be available with bidirectional ports, programmable depth and status flags, wide word lengths, and other control functions. In addition, entirely new types of application-specific memory are starting to emerge, ranging from digital-to-analog converters with RAM (RAMDACs) to complete, programmable memory subsystems.

Speed requires new architectures

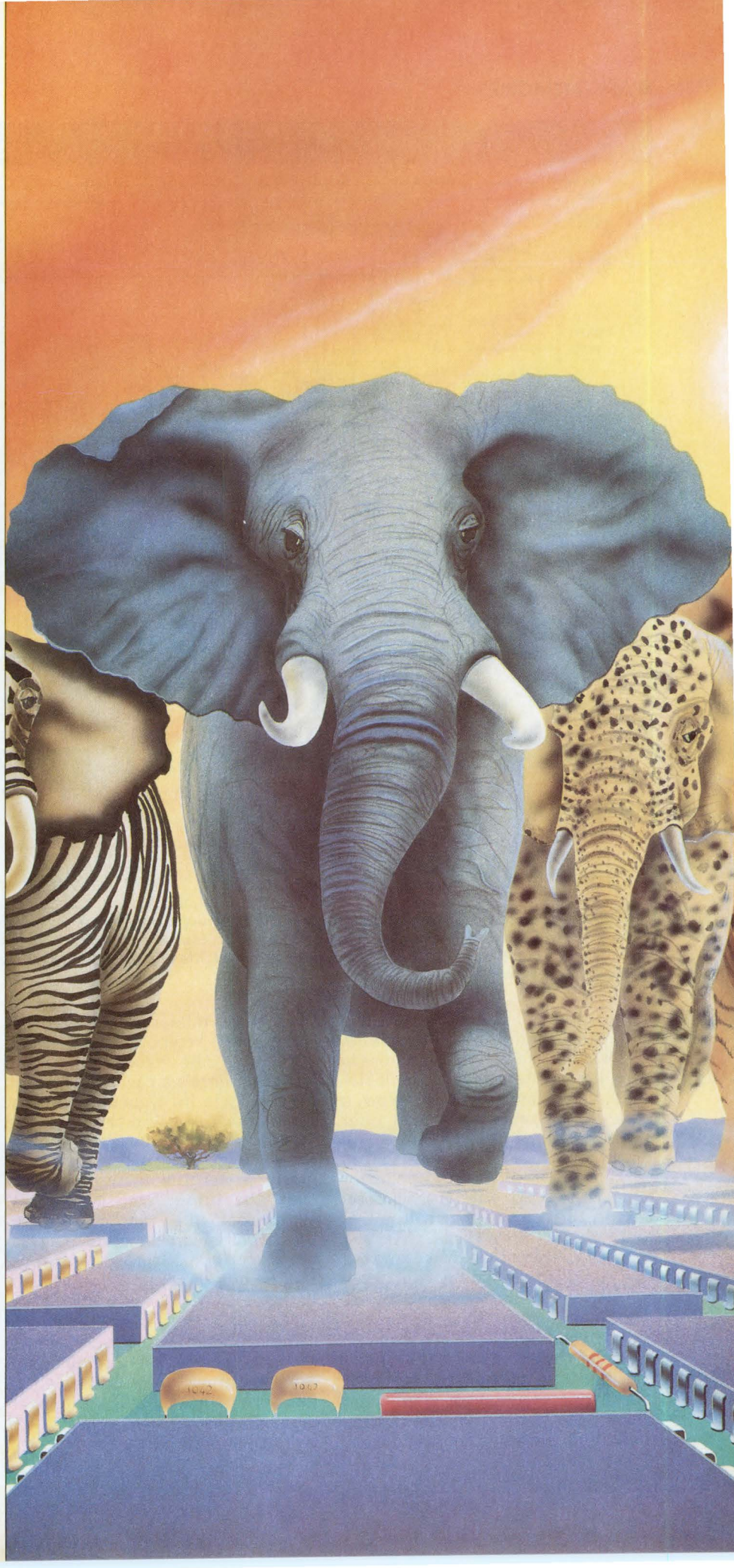
ASIC memory is a relatively recent phenomenon. Less than a half-dozen years ago, Texas Instruments (Houston, TX) rocked the dynamic RAM boat when it introduced the industry's first dual-ported DRAM, known as video RAM (VRAM). This device consisted of conventional DRAM cells with two ports: a parallel port that lets data be written to and read from the device normally, and a second port that's connected to a high-speed internal shift register so the chip can turn out serial data at video rates. The success of TI's VRAM can be measured by its number of imitators—almost every major DRAM manufacturer now makes some form of VRAM. VRAMs are widely used in almost every advanced graphics system, as well as in a host of other applications requiring the high-speed serial transfer of stored data.

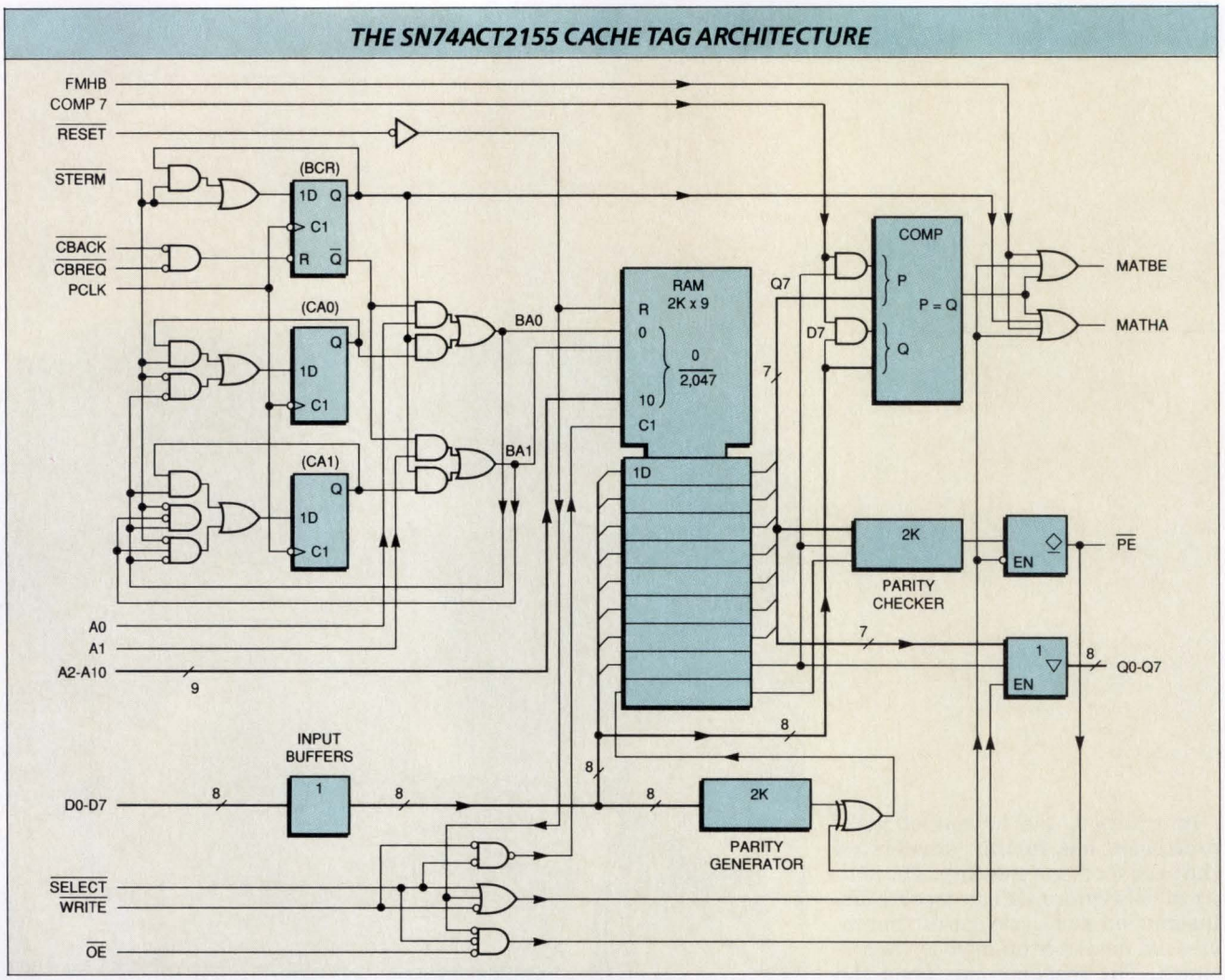
Though VRAM and other specialty DRAM products such as static-column RAM continue to proliferate, rapidly increasing processor speeds have begun to dramatically outpace DRAM access times. Inherent limitations in DRAM technology, particularly regarding refresh times, severely curtail system performance. Microprocessor clock rates have increased from only 1 MHz or so to the 25-MHz range in current generations. Devices clocking at speeds in excess of 30 MHz are already in sampling stages, and 40- and 50-MHz machines are just around the corner.

In addition, the advent of RISC processors has further accelerated the need for faster memory. The ability of RISC processors to execute one instruction each cycle has further increased demands on memory access times. The response has been the emergence of innovative memory architectures, often borrowed from minicomputer and mainframe designs and built for speed.

High-speed cache tags

One innovative memory architecture is caching, the technique in which part of the data and/or instruction information in main memory is temporarily stored in very fast SRAM while the bulk of the data is stored in relatively slow DRAM. Cache approaches use a high-speed storage medium to record the addresses of the data stored in the cache memory and to determine whether a particular address called for by the program resides in cache memory or in main memory. This function has become known as tagging, and the devices that implement it are cache tags, also referred to as tag RAMs. Cache tags are made up of a limited amount of very fast SRAM, control logic and a comparator to determine matching addresses. If a cache tag finds a





The SN74ACT2155 cache tag from Texas Instruments is designed to provide a direct interface with the Motorola 68030 microprocessor. It combines 2 kwords of 9-bit memory, a comparator and necessary cache logic. The interface and handshaking functions let it take advantage of the burst-mode capability of the processor. In addition, it has specific handshaking logic, including a pair of match outputs that speed cache operation.

match, it's called a cache hit; if a match isn't found, it's a cache miss.

TI was one of the first companies to offer a cache-tag device, the TMS-2150, about four years ago. Now, a number of competitors also offer cache-tag products, including Integrated Device Technology (Santa Clara, CA), Saratoga Semiconductor (Cupertino, CA), Vitelic (San Jose, CA), VLSI Technology (San Jose, CA) and Fujitsu (Santa Clara, CA).

A key characteristic of a cache tag is speed. If the cache tag can't keep up with the processor speed, there's little benefit from the faster processor—or from the faster cache memory. "A cache tag simply tells the CPU if the data or instructions the processor wants are resident in high-speed cache," says Steve Lau, marketing director for Saratoga Semiconductor. "But how it tells it is another story. 'How' really refers to speed."

Because the processor knows whether there's a cache hit or miss very early in its cycle and, in turn, knows where to find the data, the cache tag is located on a very timing-critical loop. In turn, designers generally prefer the fastest products since the timing loop is so tight. While companies that make memories traditionally have had to scramble to keep up with processor speeds, Lau claims Saratoga's product is a little ahead of processor speeds.

The industry is just starting to sample 33-MHz processors, which call for cache tags with a 15-ns address-to-output time. Saratoga offers four such cache tags: two 4-kword×4-bit devices with a 15-ns response and two wider-word parts, measuring 2 kwords×9 bits, that offer a 20-ns access. While there's only a 5-ns difference between the parts, that small difference could be critical. The 20-ns parts, says Lau, can accommodate 25-MHz processors and even those close to the 30-MHz level. Integrated Device Technology (IDT) offers one of the largest caches, measuring 8 kwords×8 bits, but its speed will fall short of next generation's demands.

Saratoga increased both the speed and density of its cache tags through its proprietary BiCMOS process. On the CMOS side, the process incorporates 1.5-micron drawn-channel lengths. The company is now shrinking the channel lengths to 1.2 microns, which will reduce cell and die sizes by about 35 percent, according to Lau. While the shrink in the CMOS size provides a gain in density,

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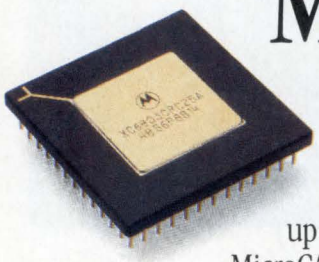

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the increased speed is achieved in the bipolar side of the process.

On Saratoga's self-aligned bipolar CMOS (SABiC) process, the base width measures a scant 0.15 microns, resulting in a cut-off frequency of 6.5 GHz. Bipolar devices are used throughout most of the chip's high-speed paths and serve as line drivers for the CMOS memory array. A die shrink that's underway for the bipolar devices (similar to the die shrink of the CMOS part of the process) is expected to raise the cut-off frequency to around 10 or 12 GHz.

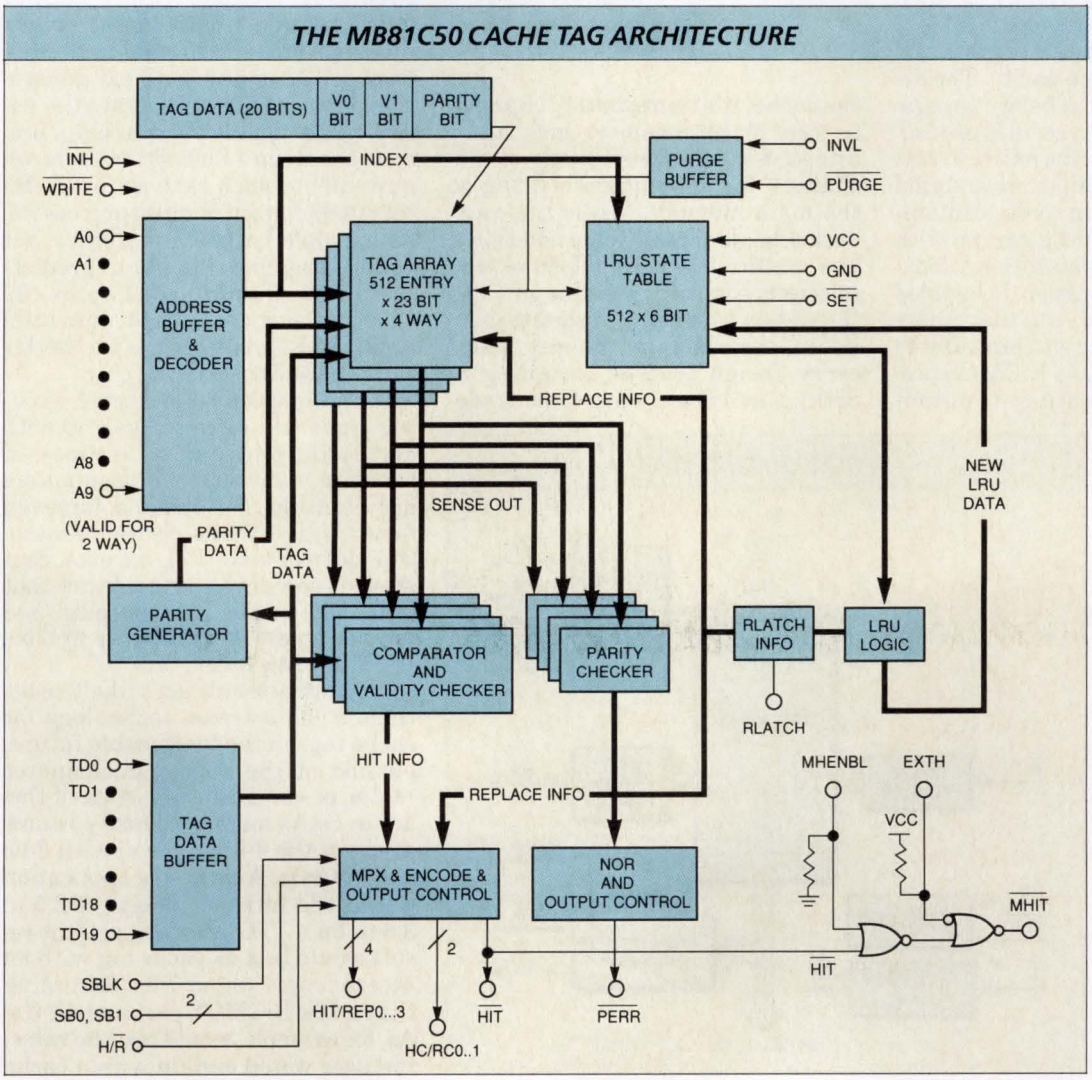
■ Desirable features a plus

With cache tags, speed itself may not be enough. Designers are also looking for deeper caches, wider word widths and more control logic—all on a single chip. Saratoga's 2-kword× 9-bit part, for example, while not keeping up in speed with the company's smaller device, offers parity check generation. This on-chip circuitry can eliminate a number of external devices that are not only more costly, but chew up valuable time with internal propagation delays and on-and-off chip delays.

In addition to speed and density, the quest to include other desirable characteristics in their cache tags has sent vendors scrambling in every direction. Since different processors tend to have different ways of implementing caching, a processor-specific cache tag—although limited in range of usability—attains the highest possible performance, according to TI's Chris DeMonico, strategic marketing manager for VLSI products. TI's SN74ACT2155 cache tag, for example, is specific to the Motorola 68030. By incorporating such features as burst-mode addressing and specific processor handshaking logic, the SN74ACT2155 is able to perform far faster than if the same functions were implemented in discrete logic, even though the raw device speed may be somewhat slower.

Various differences in processors, particularly between the Intel and Motorola architectures, make for a wide range of cache-tag designs. Motorola's processors, for example, call for a deep but relatively narrow cache, while Intel's family of processors work better with a shallower but wider cache. To complicate the issue even more, there are a variety of cache controllers available, each with its own caching algorithm, and handshake and control logic. In addition, many designers have elected to design their own ASIC cache controllers, which demand even more flexibility from cache-tag chips.

"While there's a tendency for cache tags to be processor-specific," says DeMonico, "there's also a need for them to offer the system designer complete flexibility. Ask 100 design-



Fujitsu's MB81C50 cache tag is designed to be relatively processor-independent, unlike Texas Instruments' SN74ACT-2155. It's designed as a two- or four-way set-associative device, also unlike the TI device. Twenty of the cache tag's 23 bits are address bits, and the remaining three are for validity and parity.

ers how to design a cache, and you'll get at least 100 different answers. Much of a system designer's time is spent designing the memory interface." DeMonico sees a need to maintain a flexible building-block approach to cache tags so that designers have a range of alternatives. To respond to the need for flexibility, TI offers around a dozen different cache tag products.

A processor-independent device

Fujitsu took a somewhat different path from TI by providing a more processor-independent cache tag that's designed to be more specific in the type of caching technique. The company's premier cache tag product is a four-way, set-associative cache providing a 2-kword×23-bit organization and a 25-ns address-to-output time, says Ravi Sethi, product marketing engineer. Used as a four-way cache, each set would have a maximum of 512 bits, and 1,000 bits when used as a two-way device.

The 23 bits include 20 tag bits and 3 bits for validity and parity. The device includes internal parity generators and uses a least recently used algorithm as 6 bits by the entire array. It also includes a chip-enable signal to permit daisy-chain configurations.

Though barely off the ground with its first part, Fujitsu is already looking to the next generation. Scheduled to appear early next year, the second-generation cache tag will probably be fabricated in Fujitsu's BiCMOS process and will drop access-to-output time from 25 ns to around 15 ns. The basic chip architecture is relatively well suited to a write-through scheme, says Sethi, and Fujitsu is planning to add other features including a copy-back function.

While Fujitsu's approach is perhaps not the most efficient, techniques such as write through and copy back are easy to use, and make it simpler to maintain coherency between the data sets. In a copy-back scheme, if something is changed in the cache, it's immediately changed in the main memory, making it unnecessary to keep track of the changes for subsequent writing to the main memory. While the copy-back scheme creates some additional bus traffic, it's both effective and relatively easy to implement provided the system isn't being pushed to maximum performance. In just about every design process, according to Sethi, there are always some trade-offs that have to be made.

"While there's a tendency for cache tags to be processor-specific, there's also a need for them to offer the system designer complete flexibility."

—Chris DeMonico, Texas Instruments

■ ■ ■

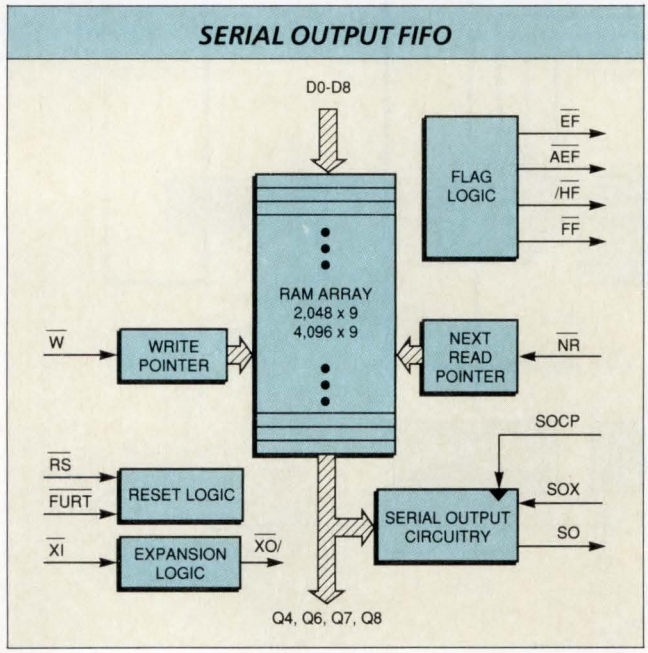
According to Sethi, it's easy to end up with a cache tag that has all kinds of cache-controller and bus functions. Many of the decisions regarding how many functions will be included on-chip are influenced by package constraints, price and the economics of die size. Fujitsu plans to create at least two other chips, therefore, to handle additional features such as controller functions, bus monitoring and bus-transfer schemes. Such control chips could eliminate much of the glue logic associated with processor interface, direct memory access control and cache interface.

Future cache tags

While there's little agreement on exactly what functions will be included in future cache tag architectures, there is consensus that the parts will continue to increase in speed and density. Typical cache designs for a 68030, for example, require three or four 4-kword×4-bit devices to make up the total cache-tag size of 4 kwords×12 or 16 bits. Next-generation devices will incorporate the entire cache tag on a single chip, predicts Saratoga's Lau. Other cache requirements, such as those for the Intel 80386 family of microprocessors, for example, call for a shallower, but wider, organization. Lau predicts that chips measuring 512 words×39 or 60 bits wide will fit the Intel processor's architecture far better than cascading existing chips.

As far as speed is concerned, existing parts will have to keep up with decreasing processor cycle times. In addition, some superminicomputers are creating the demand for even faster times. While current-generation devices have TTL outputs, Saratoga is now developing a device that will incorporate ECL outputs and provide access times that are well below the 10-ns level.

Gallium-arsenide isn't likely to become a mainstream technology for cache tags in the foreseeable future, outside of the superminicomputer realm, predicts Lau. The state-of-the-art in GaAs memory density is now at about the 4-kbyte level with 3-ns access times. A cache-tag application would add intrinsic delays of 2.5 to 3.5 ns for a TTL interface, and the result would be a 4k cache tag with an access time of about 7 ns. Assuming that a 16k BiCMOS part and 4k GaAs, for example, would cost the same, the user would end up with a cache



Variation on a theme is one of the tenets of specialty memory. In its family of parallel-in, serial-out first-in, first-outs, Integrated Device Technology converted a conventional ×9 FIFO into a serial output device. In addition, it included flags for empty, full, almost empty and almost full.

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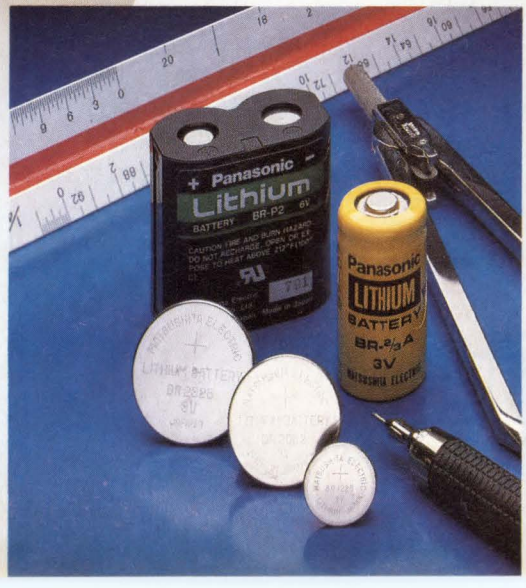

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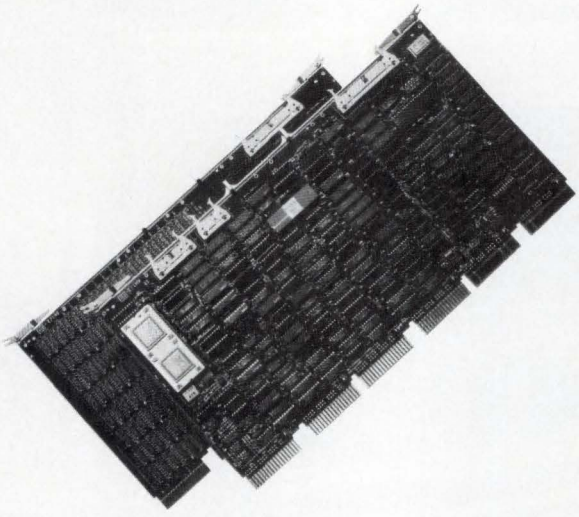

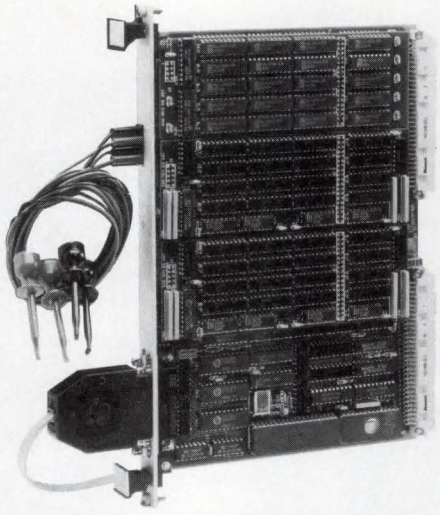

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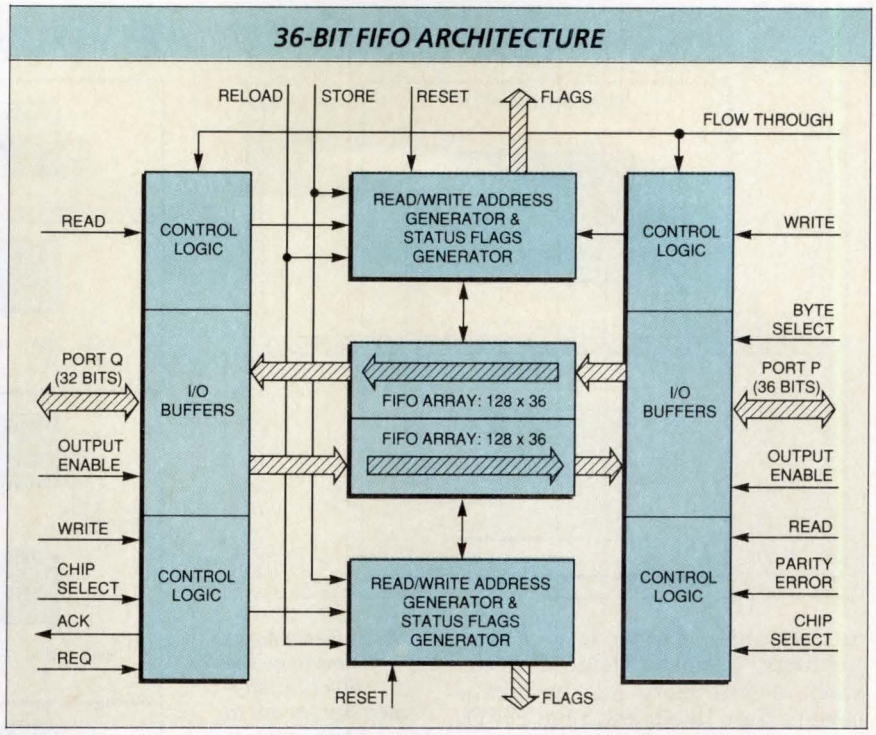
with one-quarter the density and only twice the speed. In the meantime, BiCMOS devices are rapidly increasing in speed and will soon reach the 12-ns access time range. GaAs cache tags with ECL I/O will probably find limited application in superminicomputers, Lau predicts.

Although cache tags and cache RAMs could benefit from some tight coupling, the number of different cache approaches dictates that the SRAM used for data memory be more flexible. Therefore, designers of cache tags and cache RAMs use more conventional SRAM. Fujitsu had originally planned to introduce a specialized cache data RAM along with its cache tag, until the company realized that designers required more flexibility. For the same reason, single-chip approaches incorporating cache RAM and cache tags are unlikely to be integrated on the same device in the near future, with the exception of some low-performance systems. However, cache subsystems including cache tags, cache RAM, other logic control functions and perhaps even a cache controller will start appearing on modules.



Saratoga Semiconductor plans to introduce a new 36-bit first-in, first-out buffer incorporating 36-bit-wide bidirectional ports. The proprietary architecture includes a variety of control logic functions, such as parity error and status flags.

The evolution of FIFOs

Faster processors and new processor architectures are putting demands on more than just cache tags and main memory. FIFOs, for example, are becoming widely used for a number of applications. As newer system architectures require processor-to-processor and processor-to-peripheral communications, they create the demand for some kind of buffer device. The answer has been a large FIFO.

The FIFOs of the early 1980s consisted of a simple shift register of 16 words×4 or 5 bits, says Jeff Hall, FIFO marketing manager for IDT. Their function was that of a very simple buffer, and they were mostly used in telecommunications, data communications and some data-acquisition systems. But the advent of high-speed processors and multiprocessing has created a demand for high-speed interprocessor communications and a high-speed processor-to-peripheral interface. And the approach to FIFOs has taken a new turn.

The newest breed of FIFOs, which started appearing in 1984, offer increased density with from 512 bits to 4 kwords×9 bits. Such parts are parallel-in, parallel-out standard FIFOs with no addressability. Based on an SRAM-type pointer architecture, they use read and write pointers, resulting in a very fast fall-through time—after a word is written in, it can be read out with only a simple delay. This has represented a shift in the way systems can be designed. With the smaller, shift-register-based FIFOs, the designer had to worry about the serial delay as data bubbled through the shift register. Now, with the more flexible, pointer-based FIFOs, data can appear almost immediately at the output with close to zero fall-through time.

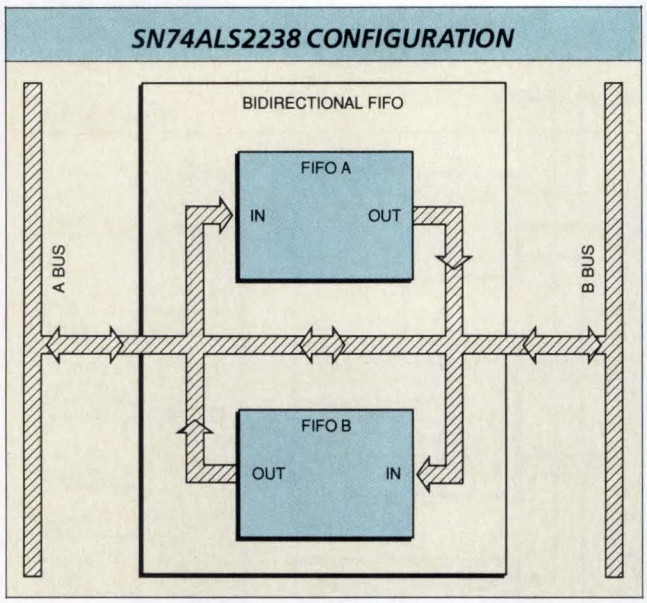
In addition, the latest generation of FIFOs contain other logic functions, such as expansion logic to increase their depth and width, parity bits and parity generation, checking logic, and an assortment of other control logic to make the parts easier to use. One of the most useful recent innovations in FIFO functions is the half-full flag, introduced less than two years ago. Before the introduction of the half-full flag, the system would only know if the FIFO was empty or full. Now, the chip can give the processor warning when the buffer approaches either under run (empty) or over run (full).

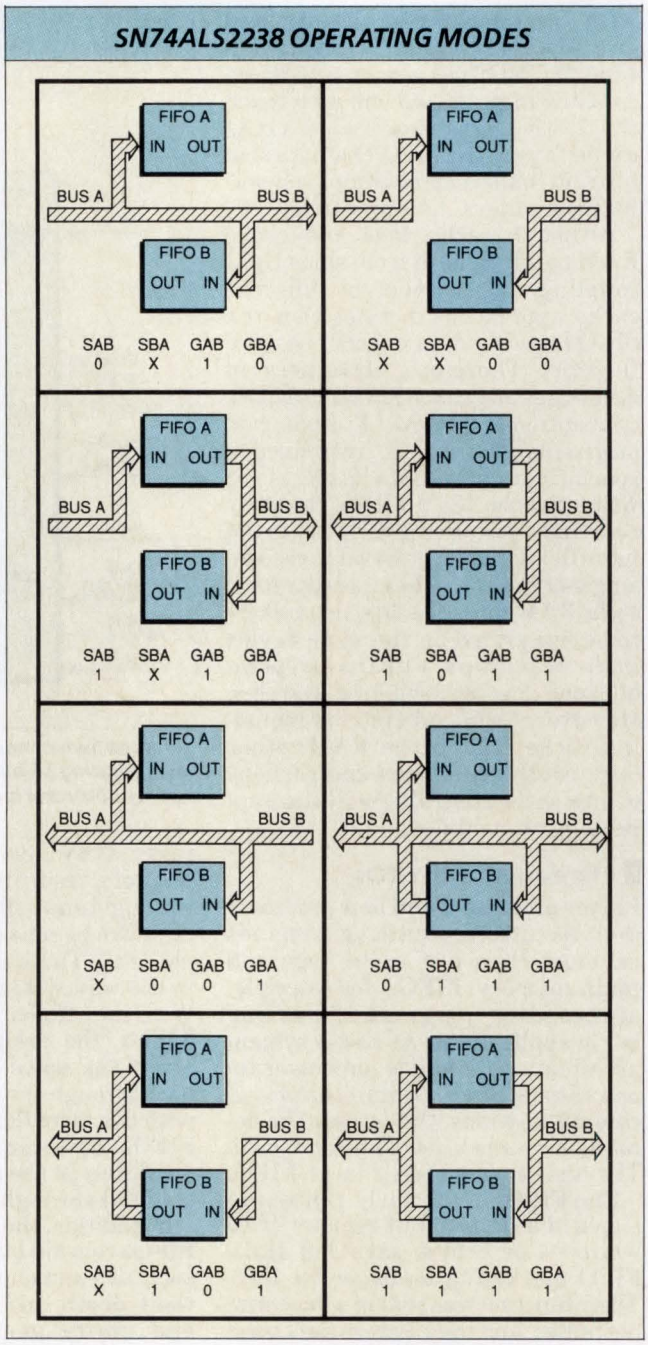
FIFOs, like cache tags, cache RAMs and other specialty memory, reside in speed-critical microprocessor loops. Performance, therefore, is one of the key parameters. Saratoga is the current speed leader, claims Lau, with FIFOs capable of steaming along at a swift 50 MHz.

New applications, architecture

FIFO architectures are about to make another major transition, perhaps as great as the move from shift-register-based parts to SRAM-based devices. This change will be both in architecture and in applications. Applications will expand from largely telecommunications, data acquisition and some data communications to become a more integral part of the central processing system. The move to multiprocessors mandates the design of FIFOs capable of processor-to-processor communication with speeds compatible with the latest generation of processors. Such mailbox-type functions will call for brand-new architectures and organizations, and increased flexibility.

At present, most FIFOs are characterized by a largely generic architecture and pinout supported by the three or four top vendors in the industry. According to TI's DeMonico, the new breed of FIFOs will incorporate such features as bus-control logic, bus drivers and other logic to eliminate the collection of programmable array logic that normally surrounds them





Texas Instruments claims to be the first specialty-memory vendor to offer a first-in, first-out with either bidirectional I/O or programmable depth—the SN74ALS2238. The simplified flow diagram (top) depicts how the device is configured. The flow chart (right) shows the different operating modes of the chip.

as bus interface devices. Future products, predicts DeMonico, will start to look more like bus transceivers than like traditional FIFOs.

■ Shift to wider word widths

One of the keys to FIFOs tackling new applications will be a shift to wider-word devices, says Saratoga's Lau. Currently, the widest word width is 9 bits. Saratoga is designing a family of FIFOs with word widths as large as 36 bits, providing 32 bits of data plus 4 bits for byte parity. The company's philosophy, says Lau, is to attack the 32-bit processor world and reduce chip count. In addition to wider word widths, this ambition requires that Saratoga add such features as bidirectional ports and programmable flags.

Saratoga used its BiCMOS process to create these wide word widths. Using a straight CMOS process to implement a 36-bit word width would have been suicidal, says Lau, since the classic concern of ground bounce becomes critical as more outputs are added to the circuit. Another consideration is that straight CMOS drivers become larger as speed is increased, until the point of diminishing returns. Bipolar drivers, on the other hand, require no such size increase and can also be made to sink up to 64 mA if required for bus driving. Also, bipolar devices drive memory bit lines and word lines, thus speeding memory-array access.

Newer systems frequently incorporate a 32-bit processor, which must talk to a microcontroller that may be only 8 or 16 bits. This requires more than a handful of conventional logic and control devices. Saratoga, however, has identified this application as a major area for FIFOs, and is developing devices that can interface to a 32-bit processor on one side and an 8- or 16-bit device on the other.

Another new FIFO architecture offered in low-density devices provides a parallel port on one side and a serial port on the other. When called for, such applications are now handled with more generic FIFOs and additional components such as a shift register and control logic. The integration of a serial interface to conventional FIFOs will benefit many LAN applications, according to Lau. Most of these applications will be in smaller LANs rather than in the larger, more complex schemes such as Ethernet. LANs operating through phone lines at distances of perhaps only 100 ft, for example, could make significant use of such FIFOs.

The new generation of FIFOs is still lacking in the type and number of flags they offer. At present, status flags indicate empty and full, and, as pioneered by IDT, half empty and

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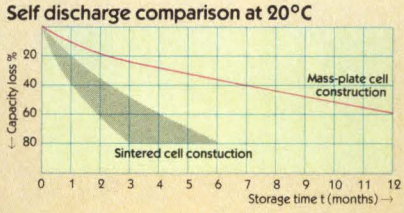

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half full. Recently, devices have emerged with additional flags indicating almost empty and almost full. Even so, many designers find that even these flags are inadequate to handle many newer applications. What's really required, say system designers, are flags that can be programmed to represent whatever status is needed.

■ Need for programmable flags

Users may desire flags that come up when the read counter reaches a particular number, for example, rather than a fixed or predetermined number. Saratoga calls such flags programmable break points. Future products, says Lau, will contain a number of flags, though not all will be reprogrammable. These flags will be programmable at reset, since the FIFO is essentially a serial device, and it's hard to halt the device and reprogram it on the fly.

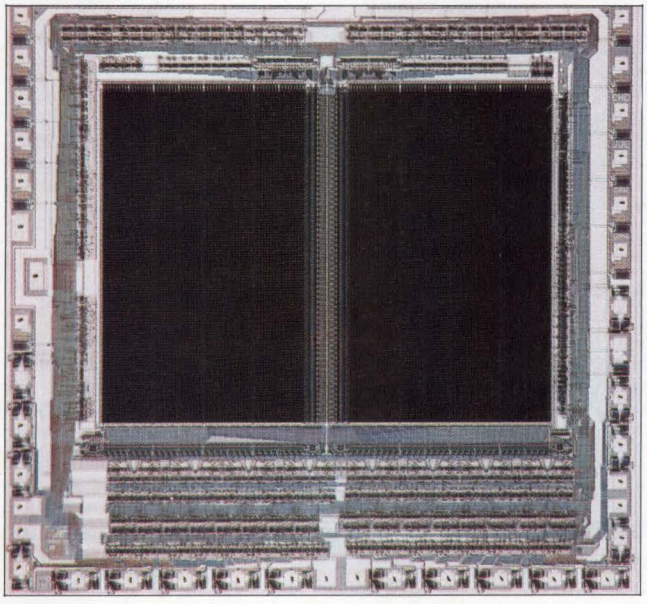
The serial nature of FIFOs requires that events such as parity error are signaled by a separate status flag. Generally, such an error causes a transmission to be restarted. By providing an error flag, however, the user can opt for an alternate course of action. Other control functions in addition to flags, such as the ability to change parity schemes (even or odd) on reset, will also be built into future-generation chips.

While Saratoga, IDT and others are racing to incorporate such features as programmable status flags into FIFOs that are due out within the next six months, TI claims to have a jump on the industry with its 74ALS2238. The part, which is currently being sampled by the company and will soon be offered in production, is the first FIFO to include bidirectional ports, a programmable depth and programmable flags, according to DeMonico.

The programmable-depth option lets designers program the depth or number of words required to fill the device, offering the flexibility of a programmable delay line. While the part is currently fabricated in the company's EPIC CMOS process, DeMonico agrees with Lau that a BiCMOS process is preferable for future FIFO architectures."If you begin to look at a FIFO as a bus transceiver—not much different from our recently introduced NuBus transceiver chip—it immediately becomes apparent that BiCMOS is the obvious process choice," he says.

■ Dual-ported SRAMs

While FIFOs will undoubtedly see broad applications in multiprocessor systems, some competition is expected from dual-ported SRAMs. As dual-ported SRAMs increase in flexibility and speed, incorporate extra bits and circuitry for byte parity, and provide separate read and write ports capable of independent operations, they'll find an increasing number of applications in interprocessor communications. FIFOs call for a sequential stream of data, while dual-ported SRAMs offer random access to stored memory. In applications such as an arithmetic logic unit register file, therefore, a FIFO can't be used because the processor has to select random bytes of information.



Many of the new breed of specialty-memory devices are take-offs of high-speed static RAM. Integrated Device Technology's user-configurable registered RAM is an example of special features surrounding a high-performance RAM. In this 4-kword x 16-bit device, IDT included its proprietary serial shift register system, allowing serial load and readback of the RAM data.

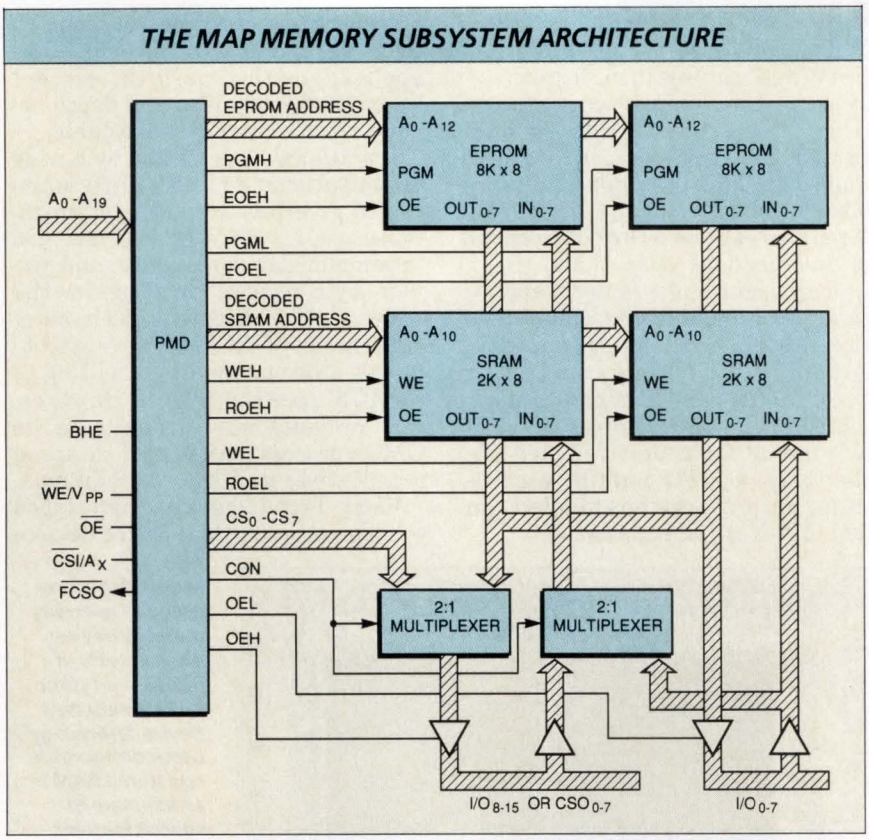
Dual-ported SRAMs are progressing on a number of other fronts. Devices are being developed, for example, to complete a read and write within 10 ns. These super-fast devices will find applications in the minicomputer arena, where they'll replace relatively low-density ECL RAMs, and provide a significant reduction in power and increase in performance. Many of the parts presently available, or under design, incorporate dual ECL I/O ports with dense CMOS SRAM arrays.

In addition, dual-ported SRAMs now require such features as interrupt signals, semaphores and parity for easy hookup with microprocessors. Like FIFOs, dual-ported SRAMs are used mostly in telecommunications and data-communications applications. However, in time, according to a spokesperson from Vitelic, designers will develop novel applications that push the present limits of speed, width and depth beyond what's currently available.

Traditional bit-wide and byte-wide organizations (×1 and ×8) are starting to give way to wider organizations such as ×16, ×18, ×27 and ×36 to accommodate wider buses and provide byte parity. Once again, the wider word widths will likely mandate the use of BiCMOS process technology since users aren't willing to sacrifice speed in return. However, IDT provides a ×16 device in its CMOS process with very little speed penalty over its 2-kword×8-bit part.

VLSI Technology has developed some proprietary dual-ported devices in addition to providing second-source and enhanced second-source devices from other manufacturers. One of its most unique dual-ported devices, which is the first of its kind with two different-sized ports, is a 16k device with a 1-kword×16-bit port on one side and a 2-kword×8-bit port on the other.

On devices that it second sources, the company tries to add embellishments to the parts to differentiate them from their competitors, says Richard Eiler, strategic marketing manager. In some cases, this simply involves offering faster versions; in others, it requires adding functions. In its 7132A/42A dual-ported SRAM devices, which are basically second sources for IDT's parts, VLSI Technology has included contention-ignore circuitry and provided two



Waferscale Integration takes the concept of specialty memory beyond conventional approaches by integrating an entire memory subsystem on a single chip. Its Mapped Address Programmable (MAP) memory subsystem, designed for digital signal processing and microcontroller applications, combines program EPROM and data static RAM on a single chip. In addition, it provides a programmable mapping decoder that lets the memory be configured in various ways, and be mapped anywhere within a 2-Mbyte address space.

interrupts.

As dual-ported SRAMs get faster, there's a trend toward a synchronous, or self-timed, architecture. This structure adds registers or latches to the RAM's I/O to hold address, data and read/write function-control information. These latches eliminate setup problems in very fast systems, letting an address be quickly latched into the RAM and then ignored.

■ Other specialty memories

Though cache tags, data caches, FIFOs and multiported SRAMs take up a good share of the specialty-memory business, other approaches are starting to emerge. The underlying trend in the specialty-memory business is to put more of a complete memory subsystem on a single chip. An example of such an approach comes from Waferscale Integration (Fremont, CA) in the form of a programmable memory subsystem for digital signal processing applications, which can serve equally well in many microcontroller-based systems.

Waferscale Integration's Mapped Address Programmable (MAP) memory combines high-speed UV-EPROM, six-transistor SRAM cells, a programmable mapping decoder and a pair of multiplexers. Internally, the memory arrays are organized as two 8-kword×8-bit EPROMs and two 2-kword×8-bit SRAMs. The chip can be configured for byte-wide or word-wide operation by programming the configuration bit on the Programmable Mapping Decoder (PMD). The memory size for the first products of the MAP family was selected based on the needs of many DSP and real-time embedded-control applications, says Jerry Banks, Waferscale Integration product marketing manager. Most applications require less than 8 kbytes of instruction EPROM and less than 2 kbytes of data storage.

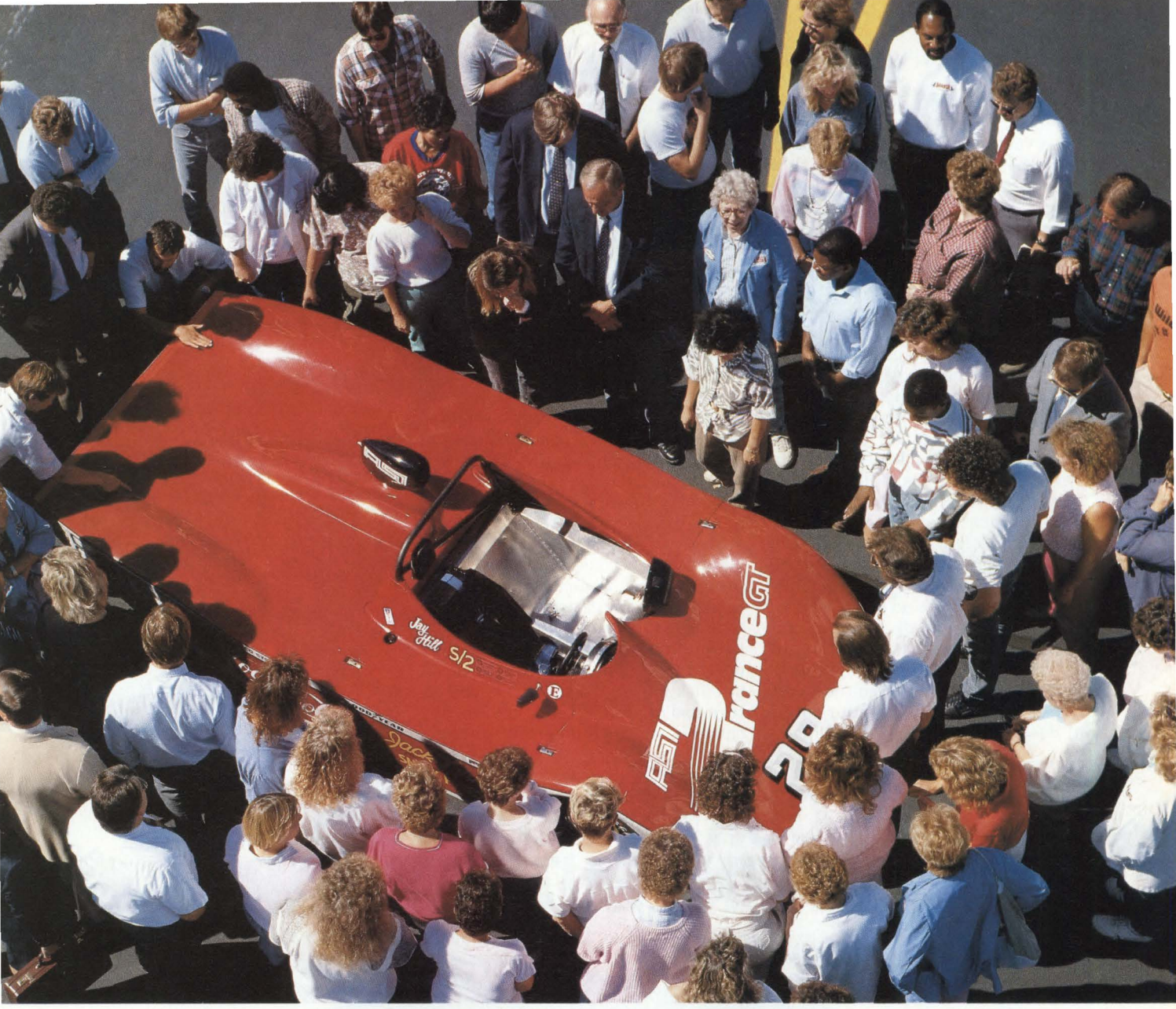
The on-chip PMD allows the placement of the physical 16 or 8 kwords of EPROM and the 4 or 2 kwords of SRAM anywhere in the total address space of 2 Mbytes or 1 Mword. In the byte-wide configuration, it's possible to subdivide and selectively access eight blocks of EPROM, each configured as 2 kwords×8 bits. Any of the eight blocks can be mapped into any of the 1,024 available 2k-deep blocks in the 2-Mbyte address space. Similarly, the two blocks of SRAM configured as 2 kwords×8 bits can be mapped into any of the 1,024 2k blocks in the 2-Mbyte address space not occupied by the EPROM.

In the word-wide operation, the I/Os of the two EPROMs and two SRAMs are common and are brought out in parallel. In byte-wide operation, however, the eight most significant bits of the I/O are multiplexed with the least significant bits using the on-chip multiplexers controlled through one of the address lines. This leaves the eight most significant I/O bits to be replaced by eight individual chip-select outputs, which can be programmed to select and control other devices in the system, such as I/O, additional SRAM or other peripheral devices.

While Waferscale Integration's MAP device is targeted for DSP applications, such as those utilizing TI's 320C25 signal processing chip, it's equally at home with high-performance 8- or 16-bit microcontrollers, such as the Intel 80186 and National HDC16000 families. The chip is fabricated in a 1.2-micron CMOS process, which supplies the memory with 40-ns access time for both EPROM and SRAM (including decode time), and provides chip-select outputs in 22 and 17 ns. Banks points out that the MAP device is the first product of the WSMAP168 family. In addition to a forthcoming die shrink from 1.2 to 0.8 microns, the company plans different programmable memory configurations and organizations.

Other specialty memories are also starting to surface, one of the latest being the RAMDAC family, pioneered by Brooktree (San Diego, CA). Designed for high-speed, high-resolution graphics systems, the two chips combine a RAM-based color palette with one or more high-speed digital-to-analog converters. The chips, which are designed to facilitate tying high-speed CRTs with slower display memory, serve as a speed buffer between standard memory chips and high-speed CRT signals.

RAMDACs also have a microprocessor unit interface that lets a graphics processor update and control the graphics memory. One of the



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Tweaking increases performance

New specialty-memory products and enhancements to existing ones will continue to surface with increasing frequency. "The designer will have an entire repertoire of application-specific memory products to select from, including both generic devices such as FIFOs and cache tags, as well as highly specialized memory subsystems," says IDT's Hall.

At least for this generation and the next, application-specific memory devices will remain largely standard, vendor-designed devices. Despite the availability of high-speed memory cells in gate arrays and cell libraries, and of sophisticated memory-cell compilers, the selection of standard application-specific memory products is still dictated by performance, cost and design turnaround. "Our internal design tools permit us to make modifications and additions to our basic design relatively quickly. However, to get the type of performance designers are looking for, chip designs have to be critically tweaked," says Waferscale Integration's Banks. It's this tweaking process that keeps memory subsystems out of the user-designed chip area.

Following the normal evolution of semiconductor integration, the first step in the development of user-designed memory subsystems will most likely be the emergence of modules or hybrids incorporating standard devices. This undoubtedly will be followed by large memory-subsystem cells appearing in cell libraries and perhaps subsystem compilers, such as a FIFO compiler.

However, the constant pressure to provide next-generation's performance with this generation's product will probably inhibit the widespread use of such approaches. Memory vendors have demonstrated that by tweaking designs, both in architecture and in process refinements, they can gain significant performance advantages. Furthermore, user-designed process technology usually remains almost a generation behind that of standard components. □

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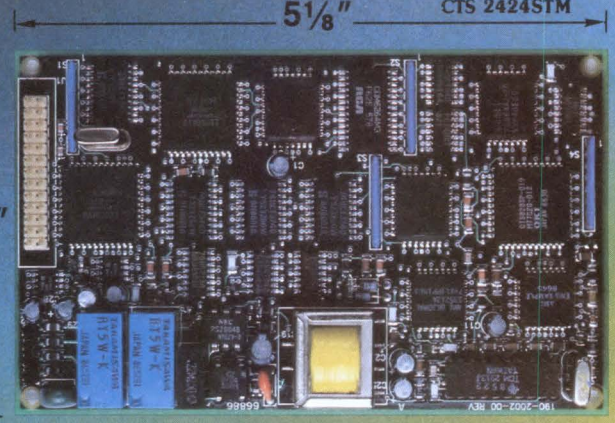

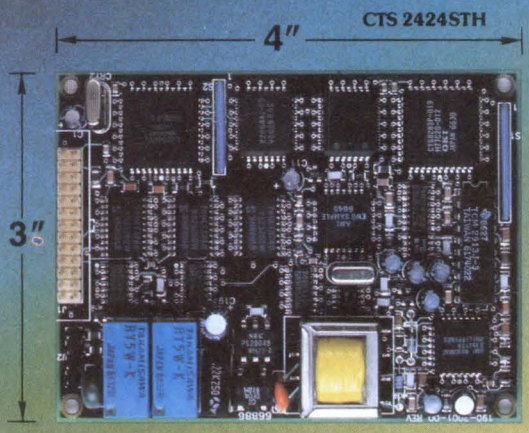

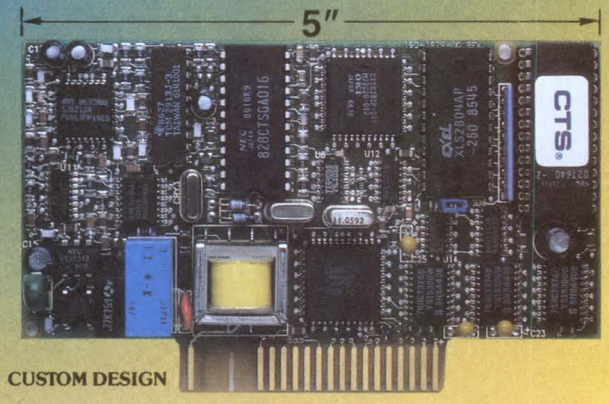

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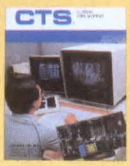

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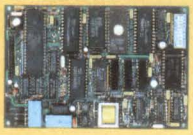

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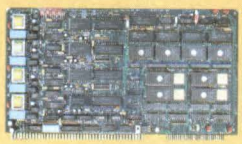

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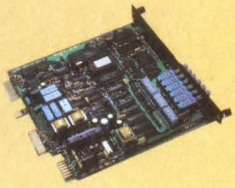

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Automated optimization refines SIMD microcode for efficient programming

Microcode development tools cut the cost and time to market for sophisticated SIMD computing architectures.

Robert A. Mueller and Dan Budge

Until recently, microprogramming was used predominantly for instruction-set emulation on general-purpose computers, and the microprograms required to implement typical machine instructions were relatively small and straightforward. As a result, only a small number of expert microprogrammers were needed to develop and optimize the microcode, which generally required only simple tool support. Today, however, a new microprogramming culture has developed that has more demanding goals and development tool requirements.

This culture has emerged from the large and growing number of applications for which execution speed is the most important requirement—applications such as signal processing, image processing, graphics and flight simulation. Computers for these applications use a single-instruction, multiple-data (SIMD) processing architecture. These computers may contain many functional elements—such as adders, multipliers, address generators, and multiple memory and data bus resources—all operating simultaneously on many streams of data.

Characterized by very wide (from 64- to over 1,000-bit) instruction words that permit a high degree of concurrent operation among independent subsystems, SIMD processing handles large quantities of data in one operation. Large, complex programs are being implemented entirely in microcode on SIMD processors. Due to this complexity, SIMD processors are extremely difficult to program efficiently. Each instruction word is composed of numerous instruction fields that control various hardware elements, and each field must be programmed in each instruction clock cycle. Moreover, many hardware elements may be pipelined, so an operation can take several instruction cycles.

Although designers of SIMD architectures have powerful chip families with which to configure high-performance systems, it's difficult to develop software to exploit the extensive concurrency and pipelining in these architectures. The software development process thus consumes the lion's share of the product development budget and greatly increases time to market.

There's a myriad of factors that contribute to this software bottleneck. To begin with, there's the inherent complexity of programming parallel

Robert A. Mueller is director of research and Dan Budge is a senior software engineer at Quantitative Technology Corp (Beaverton, OR).

How common subexpression elimination works

Unoptimized Program

```
A[i*n+j] = (X+Y)/2;
if X>0
   then Z = A[i*n+j] - 1;
   else Z = B[i*n]
```

Optimized Program

```
t1 = i*n;
t2 = t1+j;
A[t2] = (X+Y)/2;
if X>0
   then Z = A[t2] - 1;
   else Z = B[t1]
```

One common form of coarse-grain optimization, common subexpression elimination, replaces multiple occurrences of a common expression with one occurrence, a store of the expression result, and multiple accesses of the register in which the result is stored. In the unoptimized program, there are two common subexpressions—[i*n] and [i*n+j]—both of which occur in the statement A[i*n+j] = (X+Y)/2. In the optimized program, the expression results are stored in two new variables, t1 and t2. Variable t1 is assigned [i*n], and variable t2 is assigned [t1+j]. Each subsequent occurrence of the subexpressions will be replaced by the assigned variable.

processors. Unusual timing relationships, resource conflicts and large-scale concurrency create complex programming problems. In addition, the designer tends to embed obtuse hardware features in very application-specific ways, making programming at the microcode level a slow, tedious, exacting task.

Most application microcode is developed in assembly code with limited simulator and debugger support, and virtually all code optimization is performed manually, which is a time-consuming and error-prone process. In terms of cost, writing and debugging code on wide-word SIMD architectures is estimated to run between $1 and $2 per bit. An application requiring 100,000 microinstructions, where each microinstruction is 100 bits wide, might cost $10 million to $20 million to develop using today's software development tools. This situation is likely to get even worse, since the volume of application software migrating to these high-performance processors is expected to double about every year for at least six more years.

More powerful programming tools can simplify the problem considerably. It's much easier, for example, to write microcode with a state-of-the-art relocatable assembly language than to assign bit patterns to instruction fields. The use of a high-level, machine-independent language is a further step toward simplifying programming and improving reliability and maintainability. Automated code optimizers, simulators and symbolic debuggers also bring powerful capabilities to the microcode development environment.

Automated code optimization

Code optimization is one of the most critical, and perhaps the most difficult, aspects of programming SIMD processors. Most optimizations attempt to make code more efficient by reducing a program's execution time, and some focus on reducing code space. Still others try to do both.

Optimization can be either coarse-grain or fine-grain. The goal of the former, which transforms large parts of programs, is to eliminate inefficient code created through poor programming or compiler-generated code. One example is common subexpression elimination, in which multiple occurrences of a common expression are replaced by one occurrence of the expression, a store of the expression result in a temporary register, and multiple accesses of that register.

There's a common misperception that automated optimization complicates debugging.

■ ■ ■

There are many well-established coarse-grain optimizations, and a few are routinely included in higher quality workstation compilers. A more extensive collection of coarse-grain optimizations is included in most supercomputer and multiprocessor computer compilers, which are among the most sophisticated compilers.

Fine-grain optimization, in contrast, is more unusual. Fine-grain optimization manipulates low-level operations (called micro-operations) to exploit the low-level parallelism in wide-word SIMD processors by carefully scheduling micro-operations, optimizing critical program paths and concurrently executing multiple stages of a program loop. Fine-grain optimization is too complex to integrate into a high-level compiler, and a traditional compiler targeted to an SIMD processor will typically produce grossly inefficient code. An automated fine-grain optimizer can, however, reorganize compiler-generated code to eliminate inefficiencies. By programming in a high-level language that can be translated into efficient microcode, SIMD processor programmers are freed from having to hand optimize code.

Automated fine-grain optimization also enhances hardware design options, managing system complexity and exploiting parallelism that would be beyond the range of even the most experienced microcoder. Further, it helps reduce design costs and time to market. An experienced microcoder can generally write 1,000 to 10,000 lines of highly optimized wide-instruction SIMD code per year. Given a simple sequential form of an SIMD program, an automated optimizer running on a high-performance workstation can produce 1,000 to 10,000 lines of code per hour.

There's a common misperception that automated optimization—both fine- and coarse-grain—complicates debugging. Since an optimizer inserts, deletes, replaces and reorganizes code, localizing an error in the optimized source code can, indeed, be very difficult. But optimization shouldn't be performed until code has already been debugged and validated. Since an optimizer improves program performance without altering its functions, correctness is preserved. In practice, in fact, an optimizer can actually aid in debugging, since undetected bugs in a source program often become evident during the optimization process.

Automated fine-grain optimization does have some drawbacks, however.

The process limits the degree to which code can be optimized. Most fine-grain optimization problems are inherently intractable, so there are no efficient algorithms that will consistently produce optimal solutions. Nevertheless, good heuristic algorithms, evolved over many years of experience and experimentation, can produce excellent, if not ideal, results for fine-grain optimization. In situations requiring the highest possible degree of optimization, it may be necessary for critical code sections to be hand optimized by an expert microcoder. In these cases, a semiautomatic tool that verifies programmer-controlled optimizations is most effective.

There are also other drawbacks involved, such as the large amount of time required to develop a new optimizer for each new target architecture and the high cost associated with the development effort. Fine-grain optimizers are highly machine-dependent, since they require an intimate knowledge of processor resources, timing and instruction word encoding. Consequently, each new machine requires a new optimizer. Since a good heuristic optimizer is a complex piece of software, it could take longer to develop and validate the optimizer than to manually optimize the microcode it was designed to automate. This means that one-of-a-kind, throwaway optimization tools are almost always impractical. A retargetable tool that can be readily ported to different target architectures is a far more effective alternative.

Three principal fine-grain techniques are commonly used to improve code efficiency: code compaction, software pipelining and trace scheduling. Code compaction schedules a straight-line sequence of micro-operations into the fewest possible instructions without changing the sequence's function. Software pipelining, which is used for machines with pipelined architectures, reschedules loop micro-operations to concurrently execute loop stages. Trace scheduling moves micro-operations around program branches to streamline high-traffic program paths.

Code compaction is typically performed in two phases. In the first phase, data dependencies are computed for the variables in each basic micro-operation block, ensuring that a micro-operation that reads data

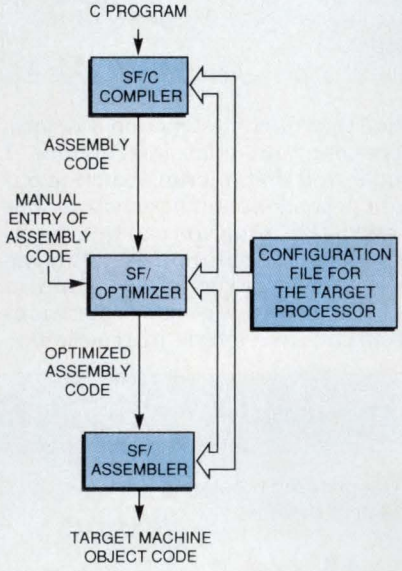
Development tool family can be targeted to SIMD processors

The Software Foundry from Quantitative Technology Corp is an integrated family of retargetable software development tools for wide-word, single-instruction, multiple-data (SIMD) processors. The tools can be targeted to a particular SIMD target architecture through the construction of a configuration file that includes those machine-specific details necessary to let machine-independent algorithms perform machine-dependent tasks. The tools are particularly well suited to wide-instruction-word SIMD processors built from VLSI components such as bit-slice processors, digital signal processors, floating-point arithmetic chips, sequencers, address generators and application-specific ICs.

The Software Foundry includes a relocatable meta-assembler (SF/Assembler), linker (SF/Linker), object-code librarian (SF/Librarian), optimizer (SF/Optimizer), ANSI C compiler (SF/C Compiler), simulator (SF/Simulator), and symbolic debugger (SF/Symbolic Debugger), in addition to a configuration processor (SF/Configuration Processor) that configures the tools to target processors from a machine description.

The SF/Assembler lets programmers efficiently program wide-instruction-word SIMD processors with pipelined resources. A programmer configures the SF/Assembler to a target processor by describing the syntax and semantics of micro-operations in the assembly source code.

Fine-grain optimizations on straight-line assembly code are done by the SF/Optimizer. Performing code compaction, software pipelining and trace scheduling, it has both automatic and semiautomatic operation modes. The configuration support needed to make the SF/Optimizer retargetable includes processor timing, instruction-word field descriptions, conflict information and micro-operation resource usage.



Once a configuration file has been constructed, QTC's Software Foundry can be used in a variety of ways. An assembly language program, for example, can be manually entered to the SF/Optimizer, which performs fine-grain optimization and sends the results to the SF/Assembler. The SF/Assembler, in turn, translates the symbolic assembly language code into target machine object code. Alternatively, C programs can be input to the SF/C Compiler for translation.

The SF/C Compiler is a full ANSI C compiler with extensions designed for SIMD processor programs. It performs extensive program analysis, including interprocedural data-flow analysis, symbolic evaluation and memory reference disambiguation, and a full spectrum of coarse-grain optimizations, including copy propagation, common subexpression elimination, dead code removal and so forth. The designer must provide the SF/C Compiler with the assembly language instructions it needs to generate to move data between machine resources, map from C data types to machine resources and from C operators to assembly code, and create an activation record.

The SF/Simulator provides an interactive environment in which code can be executed and debugged independent of the hardware. It's configured to a target processor by associating a data transformation with each target instruction.

With the SF/Symbolic Debugger, the programmer can examine and modify the contents of program variables by referencing them by name. It uses the SF/Simulator to simulate the execution of the program and thus needs only the configuration support provided to the SF/Simulator.

An example of software pipelining

Software pipelining schedules the micro-operations in a loop to concurrently execute pipeline stages. A simple program loop that sums the elements of a vector might be expressed in the following four-microinstruction straight-line pseudocode:

```
loop
1. calculate memory address in ALU;
2. read memory to memory data
   register;
3. add memory data register to
   accumulator;
4. loop till done.
```

Since all the operations in the loop can be concurrently executed and still produce the desired result, the loop can be reorganized to improve efficiency. Specifically, a single-instruction loop that concurrently adds the memory data register to the accumulator, reads memory to the memory data register, calculates a new memory address in the ALU, and conditionally loops can replace the four-instruction loop.

At this point, however, optimization isn't complete. When the loop is initially entered, it's assumed that a previous memory read has copied a value into the memory data register and that the correct memory address has been calculated for the current memory read operation. The potential problem here can be eliminated by adding a loop preamble, yielding the following pipelined loop:

```
preamble:
1. calculate memory address in ALU;
2. read memory to memory data
   register #
   calculate memory address in ALU;

loop:
1. add memory data register to
   accumulator #
   read memory to memory data
   register #
   calculate memory address in ALU #
   loop till done.
```

The original loop requires 4N cycles to execute N iterations. The pipelined loop, in contrast, requires two cycles before entering the loop and N cycles to execute N iterations for a total of N + 2 cycles.

follows the micro-operation that wrote it. In the second phase, micro-operations are scheduled in the shortest sequence of instructions within the constraints of particular data dependencies, timing issues, machine resource dependencies (a machine resource can typically hold only a single value at once) and field-encoding conflicts that may exist when several micro-operations are sharing an instruction field.

Consider a hypothetical machine with independent arithmetic, floating-point add, memory and sequencer units. In this machine, a program that performs two additions, stores the results in two memory words, and then branches might be expressed as seven microinstructions in the following straight-line pseudocode:

```
loop
1. calculate memory address in ALU;
2. r1 = r1 + r2;
3. store r1 in memory;
4. calculate memory address in ALU;
5. r2 = r2 + r3;
6. store r2 in memory;
7. branch.
```

Note that microinstruction 3 is data-dependent on microinstructions 1 and 2, and that microinstruction 6 is data-dependent on microinstructions 4 and 5. The program can thus be reorganized to obtain the following three-microinstruction program (a "#" separates distinct operations occurring in a single instruction):

```
1. calculate memory address in ALU #
   r1 = r1 + r2;
2. store r1 in memory #
   calculate memory address in ALU #
   r2 = r2 + r3;
3. store r2 in memory #
   branch.
```

Unlike code compaction, software pipelining algorithms produce results in stages that can execute concurrently. For example, while our hypothetical machine is performing a memory read using the current memory address, a new memory address that becomes valid in the next instruction can be computed concurrently. A memory read copies data from memory to a memory data register. The memory data register can be read in the same instruction cycle. In such a case, the memory data register is always read before being written in that instruction cycle.

■ Trace scheduling

Trace scheduling optimizes the most frequently used program paths. The path to be optimized is known as the trace: the term "on-trace" refers to those parts of the program that will be optimized, and "off-trace" refers to instructions in less frequented program paths. Basically, trace scheduling moves code around branches to reduce the number of instructions in the on-trace path, possibly at the expense of adding instructions in the off-trace parts of the program.

There are three main steps in a trace schedule optimization of a program: trace selection, trace compaction and bookkeeping. Trace selection, which identifies frequently executed program paths, can be per-

An example of trace scheduling

Unoptimized program
(3 units of time to execute):

```
C = A*B;
if D > 0
   then X = X + 1;
   else Y = Y + 1.
```

Optimized program
(2 units of time to execute):

```
if D > 0
   then X = X + 1
        C = A*B;
   else Y = Y + 1
        C = A*B.
```

Trace scheduling optimizes a program's most frequently used paths. Consider, for example, a single-instruction, multiple-data processor with independent adder and multiplier units. In the absence of data dependencies and shared resource dependencies, the processor can perform an add concurrently with a multiply. For simplicity, assume that multiplies, adds and compares each take one unit of time to execute. Trace scheduling can exploit the processor's concurrency.

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CIRCLE NO. 40

formed automatically by a compiler or a simulator, based on benchmark estimates of relative path execution frequency. Traces can also be explicitly identified by the programmer.

In trace compaction, the entire sequence of instructions on a program trace is treated as a straight-line sequence of instructions with one entry point, one exit point and no embedded branches. Code compaction can then be used to pack the instructions on the trace. Bookkeeping, the final major phase of a trace schedule optimization, compensates for the movement of operations around branches to preserve a program's semantics.

Automatic and interactive modes

Automatic code optimization is essential when programs are written in a high-level language. A compiler will translate the high-level language program into assembly code, which the optimizer then reorganizes and streamlines. The entire operation is transparent to the programmer.

The automatic mode can also be useful when a program is developed in assembly language. With an optimizer available, a programmer can write sequential (straight-line) code, generally with one micro-operation per line. Since it's much simpler and faster to write and debug straight-line code, as opposed to parallel operation code, development time can be reduced dramatically.

Semiautomatic optimization, a mode in which the programmer shares micro-operation scheduling decisions with the optimization program, is necessary when the microcoder needs to participate in the optimization process to ensure that performance demands are met. Semiautomatic operation is most effective when the microcoder can guide the optimizer through an interactive editing facility. Using displayed information on data dependencies, the programmer can visually identify opportunities for applying special coding tricks. In addition, program transformations can be easily edited. When these transformations violate resource usage constraints or create other detectable errors, the optimizer notifies the programmer, who can then make the necessary adjustments interactively.

Wide-instruction word SIMD architectures offer great potential for meeting rapidly escalating performance demands. But these architectures are limited by their requirement for reliable, efficient and expeditious programming. This capability can only be achieved through the use of powerful software development tools. Good automated program optimization tools are among the most difficult tools to design and implement, and the most effective tools in support of parallel programming. □

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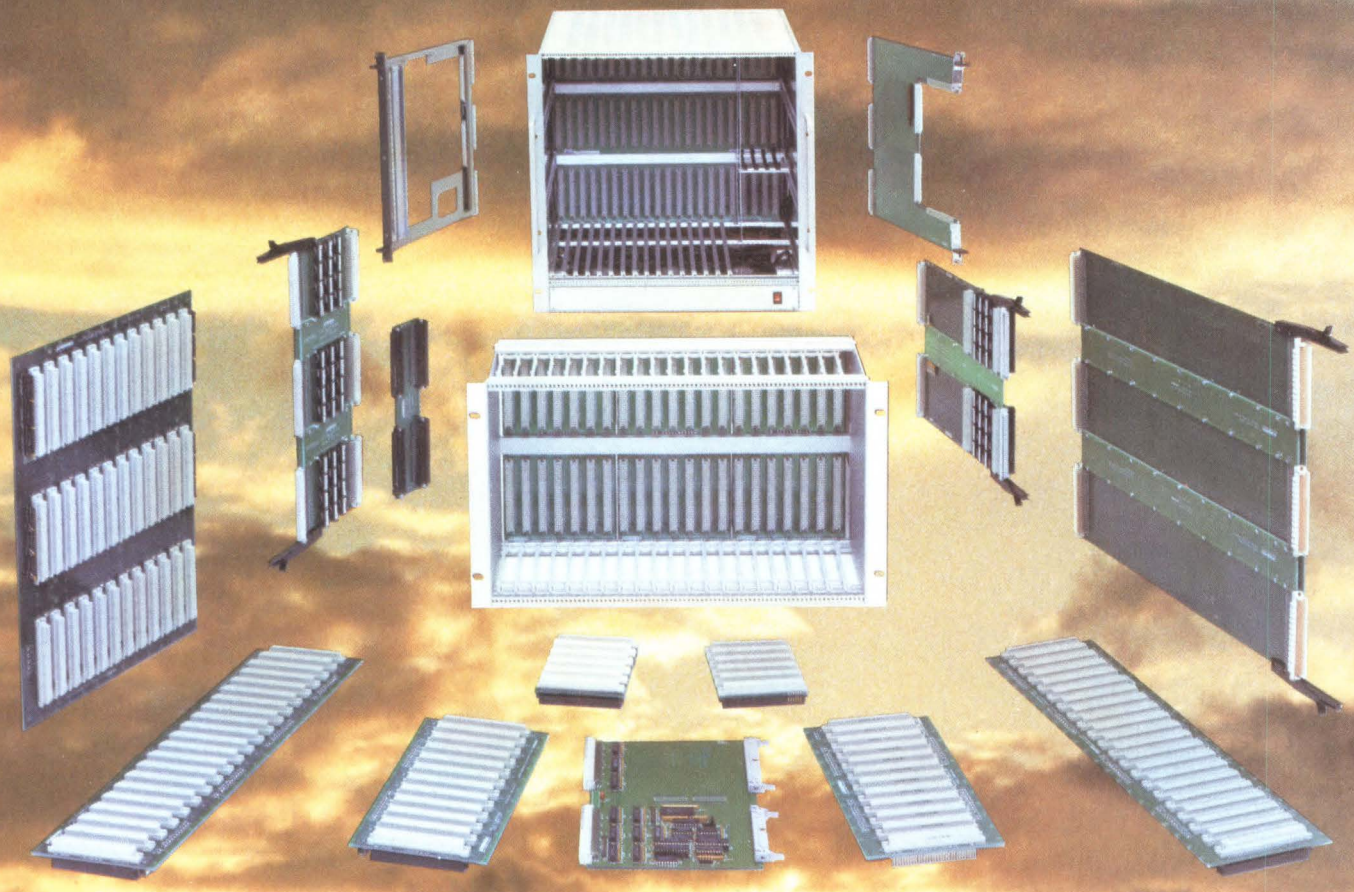

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CIRCLE NO. 44

The open-architecture bus world: too many choices?

David Lieberman, Senior Editor

Many people are surprised to learn that the old Chinese saying "May you live in interesting times" is, in fact, a curse. Someone must have wished this curse on today's open-architecture bus world, because it's suffering from an overabundance of interesting possibilities. OEMs and system integrators seem to be torn between alternative processors, buses, architectures, software strategies and networking techniques.

The future success of vendor and customer alike is likely to hinge on the decisions made today, on the forks in the crossroads that are taken and whether the timing is right. There's danger in taking a fork in the road too early and developing a technology that serves no current need. Taking a fork too late, on the other hand, can result in me-too products and a me-too company image—certainly not the road to success. Then, too, there's the danger of taking a fork that turns out to be a dead-end technology. And some will be tempted to not choose at all, to just sit at the fork and wait to see where the industry heads.

As the Buscon conference and exhibition winds up its third year this month at Buscon/88-East in New York City, most of the principal participants in the bus industry will air both their latest wares and their views on the critical topics facing the industry today. The following pages give a preview of many of the issues that will be discussed, as well as a look at some of the more noteworthy products that will make their debut at the show.

Today's hot issues

Perhaps the two issues generating the greatest interest today, and causing the greatest consternation, are reduced-instruction-set computing and real-time computing. Is the time right to take on a RISC processor? If so, which one? And can one really assume an essential performance differential between RISC and complex-instruction-set computing? What types of architectural twists, memory hierarchies and I/O structures will be effective in balancing the processing performance of new multi-Mips chips and, as a result, turning potential into usable power? How do you handle the software burden of dealing with a new type of instruction set? And what do you do with existing applications software?

As for the issue of real-time computing, one of the main questions is, Exactly what does it mean in terms of real-world applications? It clearly doesn't mean a minor tweaking of existing design and development habits. How do you provide deterministic operation in a cost-effective way? How does real-time computing affect the traditional approach to device drivers? What type of real-time development platform makes the most sense? Which of the many real-time operating systems and kernels is most appropriate for a task at hand? And what about development tools?

Then, too, there are the buses themselves—always an area of debate. It appears as if Multibus II is about to leave its cocoon and fly—but nobody knows how far. NuBus is on the verge of becoming a true open-architecture bus. But what about Micro Channel? And the ever-popular PC AT bus?

Elsewhere, the on-board power of STD Bus boards is exploding, but can STD fight off the challenge of the European standard STE Bus on the one hand, and the 16- and 32-bit buses on the other? Do 16- and 32-bit STD extensions make sense? Will the AMS Eurocard version of Multibus make a dent in the market? Or the recent rash of Multibus extension schemes? How open will Q-bus remain? Does VMEbus have the legs to carry it into future generations of high-performance systems? Will there ever be a real future for Futurebus? And how long can the old Unibus, Exorbus, Versabus and S-100 hang on?

Perhaps the most dramatic controversy in the bus world today, however, centers around software-standardization issues. Although virtually everyone in the business has a good word to say for standards, it seems as if everyone wants his own version of them. As many see it, the future success of the open-architecture bus world as a whole will depend on individual players' willingness to develop and adhere to software standards for the hardware standards that are already in place—thus enticing the OEM and system integrator to buy, rather than build, by offering quicker time to market, easier integration and surer interoperability. For individual vendors, the trick here is to achieve distinctiveness despite the commonality: to make one product stand out among a slew of near equivalents. □

■ Contents

THE BUS PLATFORM

Bringing software expertise in-house: why it works

Chris Priebe, President, Heurikon, Madison, WI

With time-to-market windows continuing to shrink, system designers and integrators are beginning to evaluate more than Mips ratings when choosing a CPU board vendor. And with competition in the board business stiffening and more vendors offering comparable products, they're becoming more choosy. Increasingly today, they're looking for a complete system solution, not just pieces of the puzzle, and they expect board vendors to assume more and more of the system-integration role. Increasingly, too, the successful board vendors will be those who are willing to take their customers by the hand and guide them through the entire system-integration process. The vendors will have to provide device drivers for the customer's choice of hardware; support and fine tune a variety of operating system and communications packages; help integrate other vendors' boards; and provide expertise in the customer's target application.

In many respects, software support has come full circle. In the CP/M days, board vendors almost universally offered operating system and driver support. Later, as Unix began to predominate and the variety of hardware configurations expanded, vendors began to rely increasingly on third-party porting houses. Today, however, heavy reliance on outside software expertise is beginning to create serious problems for board vendors. In addition to the expense involved, turnaround time can cause delays. With more and more vendors turning to outside porting houses, a considerable backlog is developing, which is being exacerbated by the proliferation of new system architectures and processors.

The advent of reduced-instruction-set processors, in particular, has created quite a dilemma. Until recently, designers of high-performance CPU boards opted primarily for one of three processor families—Intel's 80X86, Motorola's 68000 or National's 32000—and upgrades were implemented as the IC vendors introduced next-generation processors. Because these processors were object-code compatible with previous-generation family members, there were minimal porting difficulties associated with upward migration.

The move to RISC has changed that, though. Because these processors aren't object-code compatible with previous-generation processors, it's a considerable effort to port new operating systems, write new device drivers and port application programs—which, even if written in C, often require more than simple recompilation. This, coupled with the large number of RISC offerings, has created a deluge of requests for outside porting services that's outstripping the supply.

■ ***Designers expect board vendors to assume a greater role in system integration.*** ■

In effect, this reliance on scarce outside porting services makes the porting house a board vendor's business manager, with turnaround time depending on the degree to which the porting company values the board company's business. Quality can also be a problem. The rush to handle the backlog of porting assignments, as well as a lack of familiarity with new RISC architectures, could cause an increase in driver and kernel bugs. The quality of optimizing compilers could also degrade, as third-party compiler writers must quickly cope with a wider range of unfamiliar architectures.

■ In-house source code

Some vendors are trying to bolster support by strengthening their in-house software capabilities. Instead of relying on outside porting houses to handle their software needs, board vendors are purchasing the source code for the operating systems and communications packages they support, and they're adding internal programming staff to manage them.

Heurikon, for example, has found that having in-house system programmers can provide a several-month advantage over the competition in porting new Unix releases. In addition to porting operating systems, writing device drivers and debugging system interfaces, these programmers can customize an operating system and fine tune the compiler so that both work efficiently in the target environment. This capability can prove especially valuable in real-time applications.

In-house support for compilers is also proving valuable. While writing a new compiler is beyond the capabilities of most board companies, purchasing the source code and understanding the operation of a compiler can provide several advantages. If a customer uncovers a bug, for example, the board vendor can identify the bug, get the patch from the compiler vendor and implement the patch directly. By having the source code in-house, the board vendor doesn't have to wait for the compiler vendor to recompile and test the updated compiler, which may take months.

■ Putting it all together

Designers of real-time systems are increasingly opting for combinations of Unix and real-time kernels in which a Unix host serves as the development environment. In this arrangement, the final code is downloaded to the real-time kernel on the target for execution.

The problem with complex operating system interconnections, however, is that their various components—operating systems, cross-compilers, drivers and TCP/IP software—were designed by multiple vendors. Consequently, it may be difficult to isolate bugs to a particular component or obtain timely support from the vendor who designed the component. Again, by bringing the source code for these communications packages in-house, board vendors can respond more quickly to customer requests. □

Real-time computing demands standards

Wayne Fischer, Director of Marketing, Force Computers, Campbell, CA

The continuing drive for performance at all levels of the computer industry speaks well for the future of real-time operating systems and embedded computers. True, most of the action appears to center on industrial, scientific and military applications—the traditional hotbeds of deterministic computing. But new computing needs entering the scene are likely to offer unprecedented opportunities and rapid market expansion for real-time solutions. Even the desktop personal computer is approaching deterministic behavior as workstation demands for multidimensional color graphics and zero-latency I/O increase unabated.

Designers of real-time systems are focusing more on off-the-shelf board-level products and "canned" operating systems as routes to shortened development cycles and reduced architectural risks. The board and operating system markets have been moving in lockstep for several years, though in 1988 the sales growth rate for software vendors in the real-time embedded computer market has surged ahead of the hardware side. It's safe to predict that both markets can anticipate healthy growth rates as more OEMs and integrators decide to buy rather than build.

One of today's most vigorous trends—the demand for application portability—is likely to affect board-level hardware and real-time software vendors in new ways. System users want application transparency, the ability to port the capabilities of an integrated system to a new environment without reinventing the hardware and software. Users are asking difficult questions about the new generations of reduced- and complex-instruction-set computer (RISC and CISC) processors and about the impact of new instruction sets on programmers writing or rewriting application code.

The board-level industry is responding with both fresh hardware and software and fresh insight. It appears certain that the industrial world has standardized on C as the development language for new applications, in part because it allows application portability. Of the available high-level development languages, C is the closest to assembler without actually being a machine language.

Compared with machine code, however, C doesn't lock users into specific architectures, and C programs can move among CISC and RISC processors with minimum effort. Today's C compilers impart only a minor penalty over machine language—about 20 percent in execution speed and code size. Thus, it doesn't pay to write in anything but C except for the most time-critical applications.

System users want to be able to port the capabilities of an integrated system to a new environment.

Like the industrial world as a whole, the VMEbus industry is recognizing the need for a portable application language and is moving to C as a standard development language. For this purpose, The VMEbus International Trade Association (VITA) has formed a committee of hardware and software vendors. The committee expects to develop an interface definition written in C and adaptable to any computer language. Meanwhile, the IEEE-sponsored Posix (Portable Operating System Interface) subcommittee of the Unix standards committee is developing a portable interface in C.

Driver-level standardization

The development of software drivers is particularly important in embedded real-time systems because the driver code usually has to operate without latency or overhead. Progress is being made toward standardization, which will sharply reduce the level of effort needed to prepare custom drivers.

The solution to driver development has been, and still is, tight cooperation between hardware and software vendors. Board buyers, for example, have relied on their hardware supplier to recommend a vendor of real-time operating systems who also has a reputation for driver support.

Now, however, the task is being split into two parts. Hardware makers are beginning to supply drivers for their boards using a provisional standardized driver interface written in C. (The Posix committee is still working on the exact definition.) The vendor's basic drivers, each unique to a particular board, marry those boards to the standard interface.

Real-time operating systems

At the real-time operating system level, software suppliers serving a market that has adopted a standard interface will provide an operating system that exercises drivers via that interface. This will eliminate user frustration from having to write unique drivers. Given the task's complexity for most system integrators, the new methodology provides a very attractive quick start to system development.

Today's real-time operating systems use a wide range of languages, most of them machine-based, which has always been perceived as the route to performance. In time, however, these languages will probably be rewritten in C or will at least get a C interface to gain portability and machine independence. Operating system vendors may argue that their current products have kernels that accommodate C, but the interfaces are unique for each kernel, however, which is hardly the way to achieve portability.

As we move into the 1990s, sales of high-performance boards and real-time operating systems will swell rapidly as more markets discover the virtues of off-the-shelf hardware and software. The continuation of today's trends—standardized interfaces and prepackaged driver code, plus the rapid increase in board-level functionality—will weigh heavily in the designer's decision to buy, rather than build, a real-time solution. □

THE BUS PLATFORM

Real-time development tools come to life

Jennifer F. Maher, Marketing Manager, Wind River Systems, Emeryville, CA

Ten years ago, when system performance hovered around 0.1 Mips, on-board memory capped out at 64 kbytes, and application programs had around 750 lines of assembly code, traditional real-time development environments proved adequate. Current technology, however, has brought processor performance ranging from 5 to 100 Mips, on-board memory of up to 16 Mbytes and programs with up to 100,000 lines of C code. With this evolution in technology, one would expect parallel advances in development software. While this may hold true for those developing for Unix-based environments, real-time designers have been left with seemingly archaic tools and methods for developing their applications.

Until recently, designers have been faced with two equally unsatisfactory development environments for real-time applications. While Unix development environments are rich in tools, networking capabilities and user friendliness, they're unfit to meet the stringent demands of real-time systems. At the same time, the highly optimized architecture of a real-time kernel makes it ill-suited as a development platform.

As a result, designers of real-time systems have been faced with a two options: develop systems under a Unix environment and sacrifice real-time target performance, or develop on the real-time target and bear an increased burden on human and financial resources, as well as longer product development cycles. Although vendors have offered real-time Unix or Unix-like real-time solutions, many designers have been unwilling to accept millisecond solutions over the microsecond performance achieved by true real-time kernels.

After selecting a real-time solution, developers were forced to combine the hardware and software themselves. To do this, they had to integrate the Unix host and the real-time target, as well as each target software module (kernel, file manager, I/O system and debugger) to form a complete real-time system—at best, a difficult and time-consuming process. After the modules have been integrated, development has been typically done on the Unix host, with the code downloaded over a serial link—a very noninteractive and error-prone process. Once the system is complete, the developer has had to connect a terminal to the real-time target and begin debugging with the limited tools that are available in the ROM monitor.

Although this development process achieved the desired real-time performance, these rudimentary development tools can no longer meet the needs of today's high-speed systems and complex topologies. The tools lack three important features to meet the demands of state-of-the-art computer technology: extensive networking facilities, sophisticated debugging tools and a friendly user interface.

■ ***Yesterday's development tools can no longer meet the needs of today's systems.*** ■

■ Tooling up for real time

Software vendors have recently developed methods that take advantage of Unix as the development environment, while at the same time achieving the high-performance, tightly coupled solutions required by demanding real-time applications. Typically, Unix is used as the host development platform, with facilities to edit, compile and store real-time code that can run and be debugged under the real-time target. As with previous methods, the real-time software resides on each real-time processor and handles the debugging, testing and running of real-time applications.

The newer solutions offer networking capabilities, high-level source-level debugging tools, and support for remote file access and remote procedure calls. These additional facilities allow for faster, more efficient development and run-time performance. With them, for example, an engineer can develop software at a workstation under Unix and download code over a single Ethernet connection to a remote server. To the developer, the real-time target appears in a window as yet another network resource.

During development, Unix host systems are connected to real-time servers on high-speed networks or through shared memory on a common backplane. Development can be done from any number of hosts to any number of targets, with crashes on the real-time server being completely isolated from Unix and its resources. At run time, real-time targets can continue to share the network, be accessed as network resources or be removed from the network entirely. When software modifications are required, the developer simply remotely logs in to the server through a window on the Unix host.

With these new real-time solutions, developers are finally offered powerful and sophisticated real-time development environments equal to today's hardware technology. In the future, it's likely that application development tools will continue to expand in capability and performance along with hardware technology. Debugging tools must become even more sophisticated as real-time applications become increasingly complex. Software vendors must provide solutions to take advantage of the hardware characteristics of high-performance RISC, multiprocessing and parallel-processing architectures.

In the not-so-distant future, we can look forward to 100-Mips hybrid systems offering both Unix and real-time functionality in a single desktop enclosure and networked to other powerful resources perhaps thousands of miles away. With real-time software tools hot on the heels of microcomputing technology, developers may finally have access to real-time software that will no longer be overshadowed by the hardware it's designed to support. □

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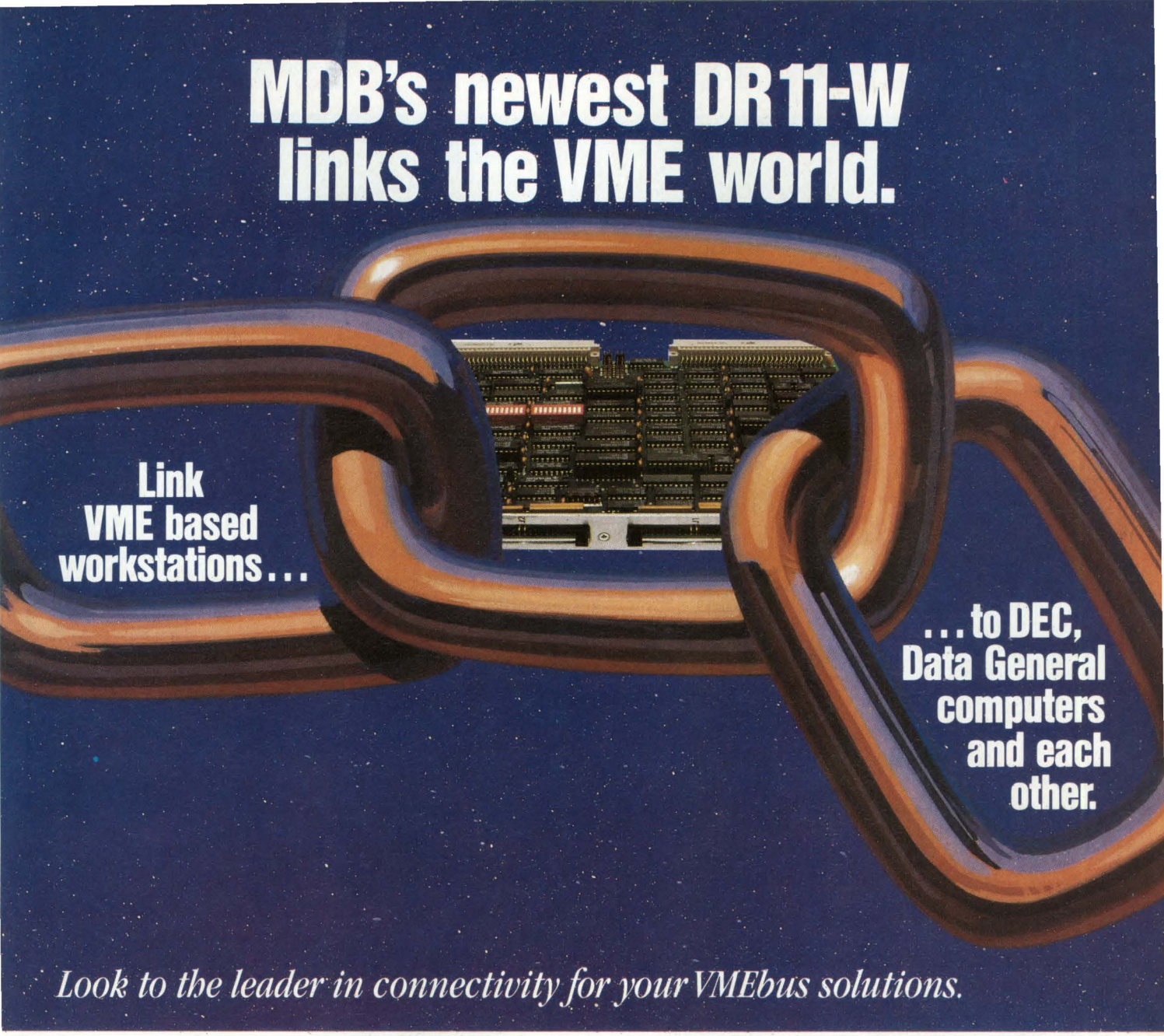

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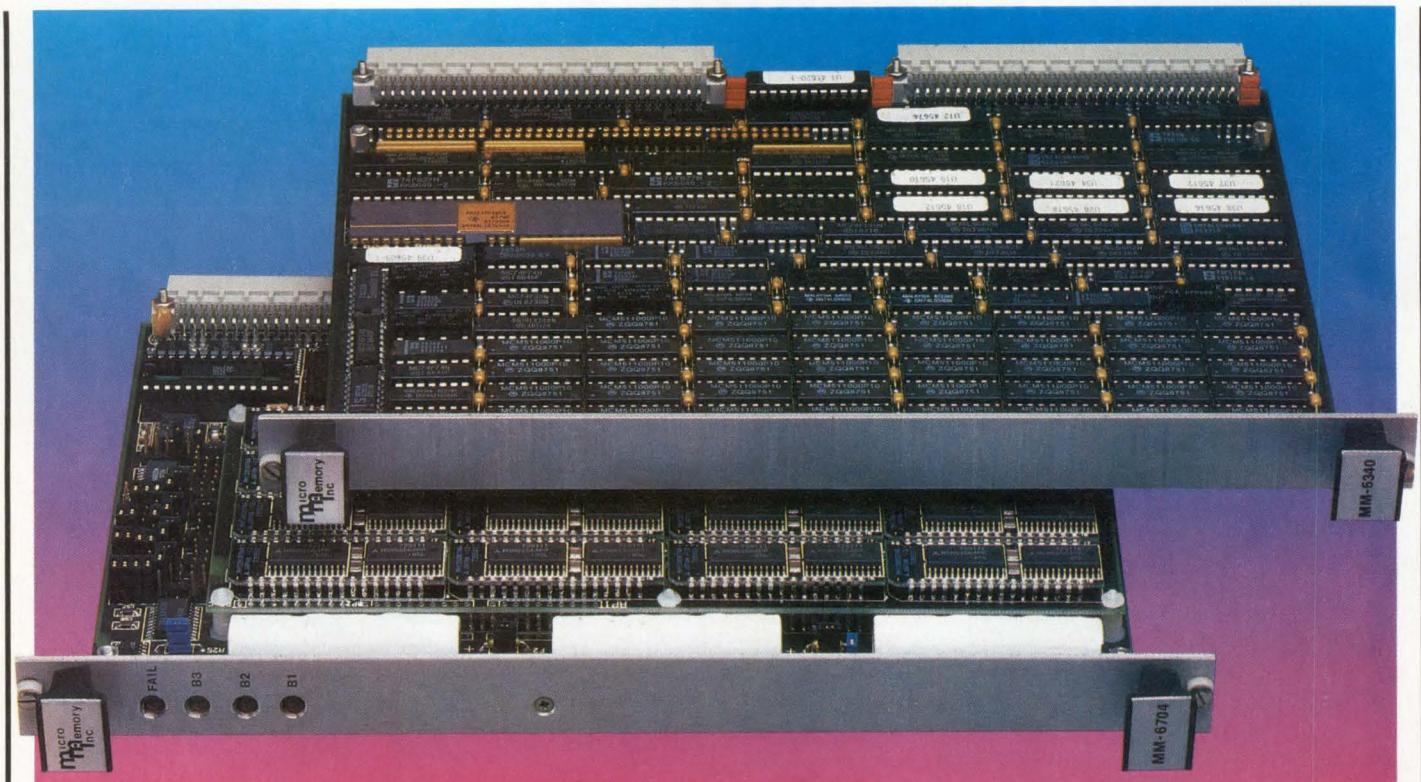

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CIRCLE NO. 45

THE BUS PLATFORM

Bus architectures shift to real-time multiprocessing

Tom Willis, Software Product Marketing Manager, Intel/OEM Modular Systems Operation, Hillsboro, OR

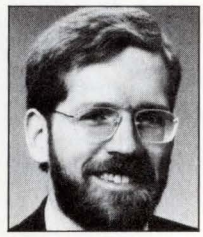
The dominance of Multibus and Q-bus—the open-architecture buses that have enjoyed the greatest success in real-time markets—is primarily attributable to the buses' real-time software support: RSX-11M system software from Digital Equipment Corp (Maynard, MA) for Q-bus, and Intel's iRMX for Multibus. In contrast, the lack of comparable real-time system software support for other buses has prevented them from making effective inroads in this market.

In the next few years, industry-standard bus boards will be used more extensively in real-time applications as they replace more expensive minicomputer-based systems. Single-board computers alone—representing $0.6 billion of 1987's $4 billion real-time OEM market—are expected to enjoy 20 percent annual growth over the next few years to represent a $1.24 billion share of 1991's almost $8 billion OEM market. Of 1987's $600 million OEM market for bus boards in real-time applications, Multibus captured a 36 percent market share, Q-bus 35 percent, STD Bus 8 percent, VMEbus 7 percent and Multibus II 4 percent.

Although Multibus and Q-bus will show continued strength in real-time markets, Multibus II and the IBM AT bus will also capture a significant share of the market. By 1991, it's projected that Multibus will shrink to a 26 percent market share, Q-bus to 24 percent, VMEbus to 5 percent and STD Bus to 4 percent, while Multibus II reaches a 20 percent share and the AT bus 12 percent. The success of Multibus II in the real-time market will be based on its sophistication, support for multiple operating systems within the same backplane, and suitability for multiprocessing. Multiprocessing, in fact, will play an increasingly important role in real-time systems. The success of the AT bus will be a function of its low entry costs.

The main handicap of AT bus systems for real-time applications has been the lack of a widely accepted real-time operating system. But, recent support for iRMX on the AT bus, will result in rapid growth of AT-based real-time systems as the bus gains credibility as a very low cost alternative to minicomputers or more functional open-architecture buses.

This new low cost point will increase the growth of the real-time market in two ways. The low cost of the AT bus solution will enable the implementation of real-time applications that were formerly too expensive. Perhaps more important, the low cost will make it possible for more entrepreneurs, until now frozen out by the high cost of entry, to get started in real-time markets.



The success of the AT bus will be a function of its low entry costs.

More processing power

Perhaps the most important reason for the overall growth of multiprocessing is that it reflects the multitasking nature of the real world itself. In addition to giving more processing power to an application, multiprocessing also allows the use of simpler, faster synchronous software solutions. But real-time multiprocessing poses some problems that are different from those of multiprocessing in other applications. Unlike other types of computing, real-time systems cannot be satisfied with good average response, but must specify and meet a worse-case response time.

Multiprocessing on a shared-memory bus such as Multibus has been successfully implemented in real-time systems, but limited numbers of interrupts and limited bus bandwidth have prevented expansion much beyond two or three bus masters. The design of multiprocessing applications on Multibus has also required special—and rare—expertise. As a result, most Multibus systems have been implemented with a single master CPU and intelligent I/O on the other cards.

In contrast, Multibus II was designed to make real-time multiprocessing easier and more powerful. Its key advantage for real-time multiprocessing is its dependence on message passing, rather than shared-memory message processing, for interprocessor communications. Message passing lets the bus support up to 20 bus masters yet still guarantee that an interrupt message from any master will reach its destination within 20 μs. If one CPU is given priority, Multibus II can guarantee a 1-μs transfer time for an interrupt message.

Message-passing multiprocessing has also allowed a dramatic expansion in the number of interrupts that a bus can support: Multibus II can support up to 255 different interrupt sources. The standardization of Multibus II communications makes it easy to ensure that all the processors on the bus are communicating together efficiently.

Micro Channel stays put

What about the Micro Channel system bus? It's not likely to gain significant market share in the real-time market over the next three years. The AT bus will represent a superior solution for several reasons. First, with its many suppliers, the AT bus will cost less. Second, the AT bus will continue to have a much wider variety of third party add-in boards suitable for real-time applications.

Third, about 50 percent of OEMs in the real-time market build at least one custom expansion board for their systems and, because Micro Channel boards require an IBM license, most OEMs will resist making this extra effort as long as the AT bus remains a viable alternative. Fourth, the lack of real-time software support for the Micro Channel and of a fully functional real-time operating system will hinder the development of real-time applications on Micro Channel bus systems. □

THE BUS PLATFORM

VMEbus gears up for 1990s computing

Shlomo Pri-Tal, Manager, VME System Technology, Motorola/Microcomputer Division, Tempe, AZ

Revolutionary advances in microprocessor technology, coupled with advances in packaging technologies, make today's board-level products deliver functional complexity and performance that were the exclusive domain of yesteryear's mainframes. As a result, the VMEbus community is rapidly refocusing to address system-oriented, rather than board-oriented, strategies. To address these issues in the context of the continuing joint and open development of the VMEbus, the technical committee of the VMEbus International Trade Association (VITA) has formed three subcommittees and a working group.

The VITA Software Subcommittee (SWSC) is working on creating specifications that will let software components interoperate in a system environment. In today's systems, the software—rather than the hardware—has a more significant impact on the interoperability of system components. The SWSC will identify interfaces that affect the interoperability of the system's software and will develop suitable specifications to be proposed as VITA standards.

The major task of the SWSC is to develop the Open Real-time Kernel Interface Definition, which has the initial purpose of allowing the development of portable drivers. The SWSC subcommittee will also look at common object file formats, as well as common media formats that will allow media transport among the various manufacturers' systems.

Another subcommittee is charged with identifying and pursuing potential areas of further specification for backplane-related issues. Since many backplane-related areas have already been addressed in other documents, the Backplane Subcommittee will take such documents into account to eliminate potential incompatibilities with approved practices.

A third subcommittee will study proposals to standardize a command and status register (CSR), possibly in the VMEbus short addressing range. On a more general level, the CSR Subcommittee's efforts are directed toward finding a more flexible way of configuring VMEbus systems.

A long-range strategy

To study the issues associated with the future evolution of VMEbus, VITA has established the Next Generation Architecture Working Group (NGAWG). VITA recognizes that VMEbus is the predominant 32-bit microcomputer architecture and that to maintain that position, a

The VMEbus community is rapidly refocusing to address system-oriented strategies.

long-range strategy that will let the VMEbus industry accommodate new microcomputer technologies must be developed.

The activity of this working group—drawn from the ranks of VMEbus users, vendors of VMEbus board-level products, vendors of VMEbus systems and platforms, as well as vendors of VMEbus software—is motivated in large part by the advent of very high performance reduced-instruction-set processors from such companies as Motorola, Sun Microsystems, MIPS Computers, Advanced Micro Devices and others. While VMEbus does provide a system environment for these processors, they stretch its capabilities. Further, it would be somewhat naive to assume that current offerings of RISC and CISC (complex-instruction-set) processors represent the absolute maximum in achievable performance.

Recognizing that VMEbus can't optimally provide a system interconnect for these ultrahigh-performance engines, the members of VITA have agreed to jointly, openly and in a timely manner develop a long-range strategy that will let the VMEbus industry take advantage of these new and exciting technologies. The NGAWG will initially articulate market requirements and formulate a business plan for the organized introduction of a next-generation VMEbus architecture, as well as identify the features that such an architecture must provide. These features will then be studied by the VITA Technical Committee, which will formulate an appropriate solution.

Possible new transactions

Various proposals for defining the use of the VMEbus reserved line have been made but, until recently, the VITA technical committee has "jealously guarded" (as some users termed it) the line's reserved nature. However, the demands placed upon VMEbus board-level products to provide building blocks in sophisticated computer systems require that the alternative uses for the reserved line be carefully studied.

The committee is looking into using the reserved line as an open-collector inverse response strobe (RS*) driven by slaves. This will accommodate two frequently requested new types of data transfers: a broadcast transfer to support message-oriented and cache-based architectures, and a cycle-retry request to resolve access deadlocks in multicrate architectures (those where multiple VME chassis are interconnected to form a single system). The major challenge in defining the reserved line is to maintain compatibility with existing VMEbus products. The board must be able to coexist with new boards in the same backplane without having or suffering an adverse impact due to the new protocols.

The joint development of VMEbus standards has established an unmatched tradition of cooperation among several competing companies to openly develop specifications that promote interoperability among high-performance board-level products. Through joint and open technical cooperation in the VMEbus community, the VITA technical committee is responding to the needs and the technological advances of an ever-changing industry to ensure that the VMEsystem remains the predominant open system architecture. □

High-performance processors pose new challenges

Richard Billig, Director, Series 32000 Value-Added Programs, National Semiconductor, Santa Clara, CA

Balancing the performance of tomorrow's microprocessors may not be possible within the constraints of today's bus board sizes and technologies. Without some system architecture changes, upgrading a board design from a 2-VAX-Mips microprocessor to a 10-VAX-Mips model could result in substantially less than the expected factor-of-five increase in performance. With processors at 50+ VAX Mips expected around 1990, this problem is likely to become more acute.

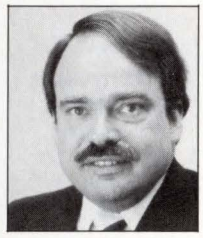
The key to balancing microprocessor performance is to provide adequate memory and efficient I/O. But memory and I/O developments aren't keeping pace with the rapid evolution of microprocessors. While 4-Mbit dynamic RAMs are appropriate for the the performance level of today's CPUs, for example, they aren't yet shipping in volume—not surprising, considering the expense and limited availability of 1-Mbit devices. Also, although disk drives are evolving to higher densities, mechanical positioning techniques keep their data-access times at tens of milliseconds.

Because microprocessor performance has increased rapidly, multiuser/multiprocess operating-system environments such as Unix have become increasingly popular in bus-based designs, even in embedded control applications. This sophisticated software affects both the memory needs (due to virtual memory) and the I/O requirements (because of the design of the Unix disk I/O subsystem) of a system.

More memory needed

Before the advent of virtual memory, balanced configurations typically contained at least 1 Mbyte of main memory per VAX Mips of CPU power. With virtual memory, however, that number has increased to 2 to 4 Mbytes per VAX Mips. Experience has shown that, whether for a micro or a mainframe, adding physical memory is often the best way to improve virtual memory performance. Based on these guidelines, a 2-VAX-Mips workstation would be fine with 4 Mbytes of DRAM on-board, but a 10-VAX-Mips design would be underconfigured even with 16 Mbytes.

The new-generation processors will thus need more than the 4 to 8 Mbytes of memory that represents the current packaging limit for a single-board computer. But going off-board for main memory fetches, even on the fastest of dedicated memory buses, significantly degrades performance. As a result, the latest CPUs



The latest CPUs use high-speed, on-board cache to mask the slower bus memory.

use high-speed, on-board cache to mask the slower bus memory and allow graceful expansion to very large memory.

With the increasing interest in efficient shared-memory multiprocessing, the caches used must become more sophisticated to maintain consistent data in each CPU's cache despite the independent actions of other CPUs. Up to a certain level of performance, data consistency can be achieved with a bus-watching subsystem and write-through cache design. However, very high-performance CPUs and efforts to put large numbers of CPUs into a single system demand different caching disciplines (such as copy-back or ownership-based designs) that buses such as VMEbus and Multibus II can't accommodate. To meet these growth needs, more advanced system buses such as Futurebus will be required.

Addressing I/O bottlenecks

Even with adequate memory, I/O bottlenecks must also be addressed. Similar guidelines for balancing I/O needs can be derived. Most Unix I/O operations are a sequence of short 1- to 4-kbyte transfers. As a result, each request may require a large number of implicit seek operations and, consequently, many milliseconds of positioning time to complete.

The I/O performance of a system is best characterized not by I/O bandwidth in Mbytes per second, but by total I/O operations required per second. Experience with Unix on superminis has shown that ten to twenty 4-kbyte I/O operations/s per VAX Mips yields a reasonably well-balanced system.

How many I/O operations per second can one 5¼-in. disk drive provide? Even with fast-access drives, the number is surprisingly small. With 2 or 3 ms for a SCSI (small computer system interface) command transfer, for example, plus a 16-ms average seek time and an 8-ms rotational latency, today's better drives have a 27-ms positioning overhead for each random operation.

Ultimately, only the actual 4-kbyte data transfer is affected by the I/O channel's speed. For example, at 1.5 Mbytes/s, an asynchronous SCSI will transfer the data in 2.7 ms, while a 4-Mbyte/s synchronous SCSI will take 1 ms. The difference is so small that positioning overhead still dominates performance. Since an average operation requires roughly 30 ms, each drive can perform approximately 33 I/O operations/s.

The average 2-VAX-Mips system would thus need about 20 to 40 I/O operations/s, and one drive would suffice. But at the 10-Mips performance level, which requires 100 to 200 I/O operations/s, three to six drives would be required. At these levels of activity, the use of multiple SCSI channels can also contribute significantly to total I/O performance.

Getting the most out of the latest high-performance board-level CPUs will require some experimentation and system tuning, adjusting physical memory and I/O configuration to optimize speed and cost. This can best be done while operating the proposed system under a test suite that creates a meaningful multiprocess and multiuser system load. Only with this type of experimentation can the whole promise of the new CPU technology be realized. □

THE BUS PLATFORM

IPI could do for I/O what RISC did for CPUs

Ernest Godsey, Director of Product Marketing, Interphase, Dallas, TX

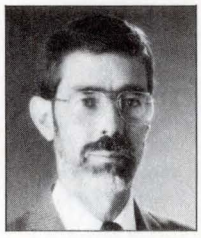
CPU vendors toss around Mips these days as if the ratings were wooden nickels. It has reached the point where system designers have to wonder how meaningful Mips ratings really are when it seems as though new super-Mips RISC chips are announced every week. What these announcements don't address, however, is the very practical question of how the system designer can increase I/O subsystem performance to balance the performance of a new high-performance processor. After all, even the fastest CPU can be slowed to a crawl by its I/O subsystem. The Intelligent Peripheral Interface (IPI) could increase I/O subsystem performance just as reduced-instruction-set computing (RISC) has increased the performance of CPUs.

Until the recent crop of high-performance microprocessors so dramatically increased the Mips ratings of CPU boards, high-performance peripheral interfaces such as storage module drive (SMD), enhanced small device interface (ESDI) and small computer system interface (SCSI) were quite adequate for configuring high-performance open-bus systems. High performance, however, is a relative term. While SMD has the highest performance capabilities of these three interfaces, the performance of the emerging IPI standard begins where SMD's performance leaves off.

IPI's higher speed

Today's advanced SMD-E drives can achieve data-transfer rates of up to 2.4 Mbytes/s, which matches the rate of the first-generation IPI drives. As it stands, however, the IPI specification can support rates up to 10 Mbytes/s, and drive manufacturers intend to extend that specification well past this rate. The speeds and storage capacities of IPI mass-storage subsystems will continue to improve as more advanced drives and controllers are introduced, bringing continually improving price/performance ratios.

Even the current IPI specification defines transfer rates that are well above the rates of available drives using a single read-write head for each disk data surface. Future plans by the ANSI committee that's refining the specification could significantly expand the capabilities of the parallel data path. This kind of expansion capability could provide future transfer rates that will be fast enough to accommodate the I/O needs of the next several generations of advanced computer systems. It's only a matter of time before IPI becomes the dominant factor in high-performance I/O subsystems.



From a performance standpoint, IPI begins where SMD leaves off.

The parallel advantage

Perhaps the most obvious technical distinction that IPI has is its parallel 16-bit data path. Earlier device-level interfaces such as SMD and ESDI use a serial data path, which necessarily limits the data-transfer rate to the signaling rate of the interface itself. An SMD-E interface that's operating at 24 MHz, for example, transfers 1 bit of data at a time and—taking disk formatting into account—will achieve approximately 2.4-Mbyte/s transfer rates for usable data. Because an IPI drive transfers 16 bits of data simultaneously, in contrast, it need only operate at about 1.5 MHz to achieve the same data-transfer rate.

SCSI also specifies a parallel data stream: in this case, an 8-bit path. But while SMD, ESDI and IPI Level 2 are all device-level interfaces between a disk drive and controller, SCSI is a system-level interface that's most commonly used between a system-resident host adapter and a drive with its own embedded controller. It's thus more aptly compared to IPI Level 3, which functions as a 16-bit system-level interface.

No free lunch

Although IPI certainly has the performance potential to interest system designers, it also has a price: greater complexity in the disk drive and the disk drive controller. The IPI disk drive, for instance, performs data serialization/deserialization, which was formerly handled by the controller. The IPI controller, in turn, must have hardware components with adequate processing capabilities to manage the protocols of the new interface, plus an architecture that's efficient enough to maintain the higher speeds that IPI allows. An internal bottleneck in the architecture of an IPI controller can erode any speed advantage that's inherent in an IPI disk drive.

No matter which interface is being used, a disk controller must perform a certain amount of processing for every block of data transferred. Because of the increased speed of IPI drives, more data blocks will be transferred to the controller per unit time than would be the case with another interface. The increased data rates will require that the processors used on disk controllers become faster, perhaps even rivaling the speed of the host system's CPU. The controllers will also need larger cache memories to accommodate the larger track sizes of IPI drives. In addition, a high-speed interface to the host will be needed to quickly transfer data to host memory.

The availability of high-performance IPI drives and controllers for use with powerful VMEbus-based computer systems will accelerate the acceptance of the new interface. With the performance enhancements that are expected from future versions of IPI, however, it's conceivable that an IPI I/O subsystem could be capable of swamping any of today's open-architecture buses. The full advantage of IPI thus may not be realized until the data rates of existing buses are increased beyond today's performance levels. □

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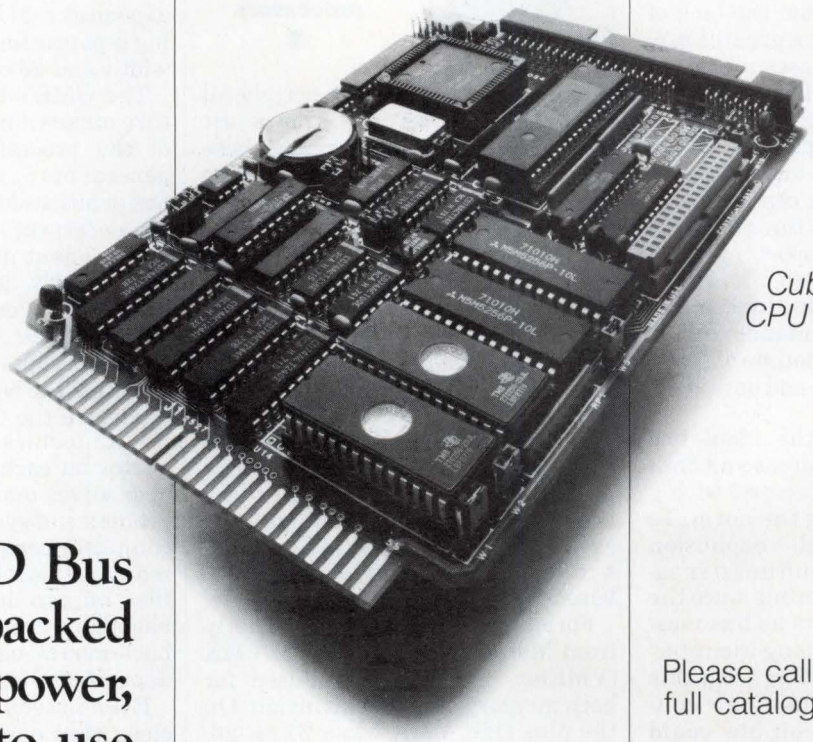

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CIRCLE NO. 46

THE BUS PLATFORM

The search for a better expansion bus

Michael Curran, President, Micro Industries, Westerville, OH

Good, bad or mediocre, a local expansion bus affords the most effective way to implement greater board functionality. By providing a secondary path, the expansion bus lets a processor board access additional memory and I/O without using the system bus. Yet every local bus places certain constraints, whether mechanical or electrical, on system expansion.

Paralleling the trend toward highly integrated boards, the number of local expansion buses on the market has soared. In fact, Multibus and VMEbus each have their own family of local expansion buses. Multibus uses one expansion bus for I/O expansion, one for memory expansion and still another for DMA functions; VMEbus, suffering from the lack of a standard, has an even greater profusion of expansion buses.

With so many buses to choose from, what's the optimum combination of features for system expansion? From experience, we know an expansion bus should provide a cost-effective way of adding various functions to a system and should support high-performance processors with a simple interface. At the same time, maximum performance demands a wide address range, vast amounts of memory, DMA capabilities and optimized interrupt capacity.

More specifically, the ideal bus should support the address and data widths of today's processors, with a 32-bit data path being the norm. To simplify interfacing, this expansion bus should relegate multimaster capabilities to the system bus since the host board usually acts as bus master. The cost of developing the interface is noticeably smaller with this approach. For mechanical convenience, the expansion bus could provide a method for mounting more than one module per host board. Furthermore, the expansion bus, like the system bus, should permit insertion of any board into any slot.

Comparing existing buses

Just how well do existing expansion buses measure up to this hypothetical expansion bus? The archetypical expansion bus—iSBX (single-board expansion bus) from Intel (Portland, OR)—provides a simple interface, 16-bit transfers and 16 address locations. Intended specifically for parallel, serial and other I/O functions, SBX quickly won widespread acceptance. Nevertheless, SBX has its drawbacks. Besides a limited data path and address range, it has inadequate DMA and interrupt capabilities for high-performance peripheral devices. Moreover, SBX allows just one module per connector, and these modules—though small to save space—are limited in functionality.

The ideal bus should support the address and data widths of today's processors.

Intel's LBX (Local Bus Expansion), which is strictly for memory expansion in Multibus systems, features 8- and 16-bit data transfers, 24 address lines and up to five agents with primary and secondary master support. But with only 24 address bits, LBX restricts memory to a 16-Mbyte direct address range. Similarly, it has too few data bits for 32-bit processors. Instead of connecting directly to a host board, LBX modules require an extra backplane in the card cage. As a result, boards become slot-sensitive based on the expansion bus they use.

Foremost in the VMEbus family from Motorola (Phoenix, AZ), VMX (VMEbus Expansion), is used for both memory and I/O expansion. On the plus side, VMX has a 24-bit address path and a 32-bit data path. It can also handle block transfers, up to six expansion modules, and both primary and secondary masters. On the minus side, multiplexed addressing slows data transfers because each transfer takes two cycles. And, like LBX, VMX extends memory to only 16 Mbytes. The extra cable connected to the backplane for the VMX is physically inconvenient because it makes slot positions within the card cage bus-specific.

A new European bus

A new expansion bus concept from Europe incorporates the best features of existing buses with some innovative features of its own. Known as OME (On-board Module Expansion), this expansion bus from Siemens (Munich, West Germany) offers compatibility with Multibus and VMEbus architectures on a Eurocard format. Not only does OME support both memory and I/O functions, but it also supports dual-port RAM expansion to 64 Mbytes without adding a dynamic RAM controller. In addition, OME expedites rapid data transfers by using separate lines for a full 32-bit data width and 26-bit address width.

The OME's less formal bus structure makes it more like an extension of the processor bus than like a general-purpose system bus. Neither bus arbitration nor DMA controllers are necessary since modules on this independent monomaster bus function strictly as slave boards. However, OME does provide four DMA request lines, three address spaces, and interrupts vectored and cascaded across the bus by an interrupt controller on the OME module.

With a stackable 96-pin DIN connector on each OME module, OME also solves many of the mechanical problems of system expansion. This connector permits the stacking of as many as four 160- or 220-mm modules on one host board. An extra backplane is unnecessary with piggyback mounting, and modules are independent of the backplane.

Even in such a small sampling, it's clear that each expansion bus has distinct advantages and disadvantages. Considering that there are as many expansion buses as there are architectures, it would be surprising if a perfect solution for system expansion existed. Certainly the OME bus, with its stackable connectors, DRAM expandability and multifunctionality, deserves serious attention. □

Militarized vs. mil-spec: appreciating the difference

Doug Patterson, Marketing Manager for Military Products, Radstone Technology, Pearl River, NY

In the VMEbus board industry, there are fundamentally three build levels: commercial, true mil-spec and everything in between. The expected operating parameters of a commercial board are fairly consistent throughout the industry, and the characteristics of true mil-spec boards are laid out in full detail in volumes of military specifications. There's much confusion, however, in the area in between, which includes the many VMEbus boards with such labels as ruggedized, temperature-hardened, extended temperature, militarized and even mil-qualified.

This gray area contains the potential for expensive yet avoidable system design crises. One recent government contract recipient, for example, was assured by a board vendor that commercial boards could be used for system development and later militarized to meet the system's military specifications. This approach didn't work, and the company is spending a bundle to redevelop the system using true mil-spec boards.

Boards built to commercial standards can indeed be ruggedized after the fact to withstand environments more demanding than the general commercial target environment. But a standard commercial board can't be postmilitarized up to true mil-spec standards. This capability must be designed in from the bottom up.

Commercial characteristics

Commercial boards and systems are designed to operate under controlled conditions in relatively benign environments, such as laboratories, offices and some shop-floor applications. These systems are expected to operate in temperatures from 0 to +55 °C and to withstand mechanical shock of up to 10 g and vibration of 2 g at 5 to 100 Hz. Little attention is paid to the ability to withstand severe atmospheric effects such as salt spray or dust.

At the system level, a commercial chassis most often provides convenient board interconnections, accommodations for storage devices, interconnecting wire harnesses and, possibly, a power supply. Commercial systems are normally convection-cooled by forced air blown across the active subassemblies.

Temperature requirements for commercial systems can be easily met by using readily available active and discrete components and plastic-packaged ICs. Card-edge connectors, IC sockets and push-on links are acceptable and often advantageous at the commercial build-level because they allow for easy component replacement and other modifications.

A standard commerical board can't be postmilitarized up to true mil-spec standards.

True mil-spec boards

At the other end of the spectrum are true mil-spec boards, designed to work reliably in hostile environmental conditions such as wide temperature extremes, air density fluctuations, shock, vibration, salt spray, dust, sand and water immersion. For the system designer, the combined effects of multiple military design specifications complicates the issue exponentially, which makes attention to board-level detail increasingly important.

To meet full military specifications, a board must be operational in temperatures from −55 to +85 °C and withstand thermal shock of up to ±25 °C/min. It must remain operational in 100 percent condensing conditions at altitudes from 1,000 ft below sea level to 70,000 ft above. The system should continue to operate while being vibrated at up to 2,000 Hz at 10 g. And the list goes on.

Building a board that can survive in this kind of environment requires focusing from inception on mechanical issues and durability. Boards for these types of applications must use only military-qualified, high-reliability, hermetically sealed ICs and screened high-reliability active and passive components. To meet the temperature requirements, low-power CMOS components are generally used wherever possible, and the components that run the warmest are placed nearest the board's edge.

Furthermore, conduction cooling schemes must be used, which usually involve a thermal management layer (TML): a thin layer of metal, usually an aluminum alloy, attached to the top of the printed circuit board, with cut-outs through which component pins pass so that the device package rests directly on the TML. When the board is mounted in its enclosure, the TML makes solid contact with the wall of the metal box, conducting heat from the components and transferring it to the inner walls of the system enclosure.

Other requirements of full mil-spec boards include multiple layers and increased line widths to minimize the detrimental effects of shock and vibration, and the use of shielded and mechanically sound connectors, usually with either a pin-and-socket or fork-and-blade contact design.

Ruggedizing sometimes works

To be fully militarized, a board clearly must be designed that way from the start. Of course, some aspects of a fully militarized board may be implemented after the fact to give a commercial board added sturdiness for certain niche applications. This is often an efficient way to meet specific environmental conditions, particularly when one considers that a full mil-spec board generally costs at least seven times more than a commercial version of the same board.

These gray-area, ruggedized boards might be used in applications such as pipeline-sensing equipment in weatherproof enclosures or sheltered air traffic control equipment. The operating specifications for such systems are defined by the application and usually involve an environment somewhere between the relatively gentle commercial environment and the hostile military environment. □

THE BUS PLATFORM

Buses vie for data-acquisition applications

Audrey F. Harvey, Engineering Manager, Data Acquisition Div/National Instruments, Austin, TX

Designers choosing a bus for use in personal-computer-based data-acquisition applications will soon have just three major buses to consider. Of the three, the IBM AT bus is now the most popular for such applications. But the NuBus and the Micro Channel are fast becoming established as platforms for data-acquisition, test, and measurement applications. In the case of the AT bus, the popularity is largely due to improvements over the PC and XT buses: a faster processor, larger card size and an increase in data bus width to 16 bits. For the other two buses, the introductions of the Apple Macintosh II computer (based on the NuBus) and the IBM Personal System/2 computers (based on the Micro Channel, except Model 30) represent significant advances in PC technology and pushed both buses off to strong starts.

When comparing these three buses for laboratory data-acquisition applications, one must consider bus bandwidth and size, memory-addressing capability, plug-in board size, power budget and multiple-processor support. Data-acquisition applications are typically I/O-intensive and consume lots of bus bandwidth and memory. The more sophisticated applications require multiprocessor systems for real-time data processing. Standardization and legal constraints on bus use are also pertinent issues.

One of the most significant improvements in PC technology is an increase in address and data bus width to 32 bits, coupled with an increase in raw data-transfer rates. The NuBus and Micro Channel have 32-bit data buses and 32-bit addressing capability, although the only PS/2 models with 32-bit slots are models 70 and 80. The Micro Channel and NuBus support burst transfers of 20 and 37.6 Mbytes/s, respectively. The AT bus can transfer 1.6 Mbytes/s, but achieving this rate has been very difficult for board manufacturers.

The data-transfer capacity of a bus determines the data-acquisition system's overall throughput. For example, the NuBus can support a 12-bit, 10-MHz analog-to-digital converter, and the Micro Channel can achieve about half that performance. The AT bus is limited to sub-1-MHz 12-bit A-D converter boards unless the manufacturer provides on-board memory.

The AT bus advantage

Two of the significant advantages of the AT bus for data acquisition are its large card size, approximately 56 in.², and a total computer power budget of 19.8 A at +5V, providing approximately 2 A per slot. Board size has a direct effect on the amount of functionality that can be provided by the board vendor. The NuBus has a similar card size, approximately 52 in.², but the Micro Channel limits the plug-in board manufacturer to an approximately 36-in.² card. The net result is that the Micro Channel board manufacturer must reduce functionality, invest in gate array technology (which increases the development time and cost per product), or invest in surface-mount technology (which remains quite expensive).

One important strength of the new buses is the provision for multiple processors.

The Micro Channel has also severely reduced the power budget. Per plug-in board, for example, 1.6 A at +5 V is alloted. This limits the number of high-speed analog and digital components that can be used, requiring that the manufacturer use CMOS technology for most of the design implementation. The Macintosh II NuBus power budget is similar to that of the AT Bus, alloting 2 A at +5V per slot.

The biggest and most far-reaching strength of the NuBus and Micro Channel specifications is the inclusion of protocols and mechanisms for multiple processor use of the bus. Both buses provide fair arbitration mechanisms that let a plug-in board gain control and use the bus to access other boards and/or system memory. These buses will, therefore, promote PC-based data-acquisition systems that provide high-speed, background processing of incoming data, while the main processor is used for running the user interface and other operating system tasks.

The Macintosh II implementation has the advantage here in that its 68020 consumes any NuBus bandwidth when talking to its program memory, thus leaving the bus free for board-to-board communications. Unfortunately, the PS/2 processors use Micro Channel cycles when communicating with program memory. Boards using the Micro Channel for board-to-board communication have adverse effects on main processor computation time, and vice versa.

NuBus is IEEE standard

Another advantage of the NuBus is its status as an approved IEEE standard bus. Manufacturers may build NuBus boards or use the bus in their own PCs for a nominal licensing fee. In contrast, IBM has kept tight hold of the patented Micro Channel and has only recently announced plans to license it to PS/2 clone makers.

Although the AT bus has some advantages in the area of plug-in board size and power provided, its severe limitations in bus bandwidth and multiple processor support limit growth for data-acquisition applications. The Micro Channel has successfully addressed the bus bandwidth and multiple processor support issues but has placed severe limitations on manufacturers of plug-in boards by reducing available space and power. This limitation may, however, be only temporary as component size, component power and manufacturing technology advances are made. The NuBus, on the other hand, gives the best of both worlds, providing the highest bus bandwidth with almost negligible compromises in board size and power. □

Omnicomp™

High Performance OEM Graphics Solutions

High Performance

Omnicomp designs and manufactures high performance graphics subsystems for a wide variety of applications. Addressable resolution is 1 to 2 million pixels while viewable resolutions are typically 1 million pixels, or greater. I/O speeds range from 1.2 MBytes to upwards of 40 MBytes per second. Vector drawing rates normally exceed 1 million pixels per second and, for the OMNI 2000/2400 GDS approach 10 million pixels per second. Graphics computing speeds range as high as 7 mips for integer operations and 7 megaflops for floating point computations.

Flexible Interfacing

In addition to bus-based configurations, each Omnicomp graphics display product can be supported using a wide variety of industry standard interfaces. Omnicomp manufactures a series of these interfaces for the IBM PC/XT/AT/RT, iSBX, and VME which emulate the DEC User Peripheral Interfaces; DR11-W, DRV11-WA, and DR11-C, DRV11. When installed in an appropriate host, these interfaces provide communication with DR11/DRV11 compatible peripherals, such as graphics display controllers.

Compatibility Plus

Whether your system uses the PC bus or the advanced architecture of MULTIBUS II, Omnicomp can provide a graphics display solution to meet your needs. Additionally, our products support DEC DMA interfaces to provide bus independent compatibility with many other computing platforms.

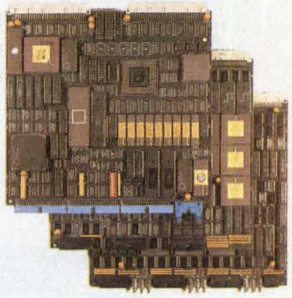
Software compatibility is maintained across the Omnicomp product family lines via our OMNI • KERNEL SYSTEM (OKS) which provides easy access to on-board graphics functionality using FORTRAN and "C".

Custom Service

Supplying reliable, well engineered graphics subsystems at a competitive price is important. Even more important is providing an extra measure of commitment to insure our customer's success. Omnicomp makes that commitment with Custom Service.

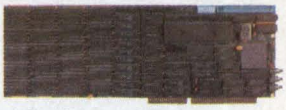
Our Custom Service is an attitude that emphasizes doing whatever is necessary to accelerate the integration of our products into your end-user solutions and to shorten your time-to-market. This includes providing application specific firmware, special interfaces, on-site engineering support and training, one-off packaging; almost anything that contributes to your success!

OMNI 2400 GDS



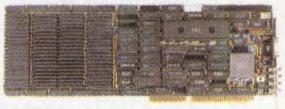
- MULTIBUS II 6U x 220 mm
- DEC DMA Compatible
- Up to 52 Planes with 4 Overlays
- 1280 x 1024 Resolution
- Hardware Cursor, Zoom, Pan
- GKS Display List Processing
- 10 Mega Pixels/Second
- Up to 3 Graphics Channels
- 2D & 3D Wireframe
- 70 MIP Image Processing
- Local Input Device Support

OMNI 1600 GDC



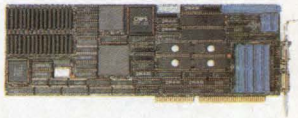
- GKS Display List Processing Via OMNI 1500 DLP
- Up to 256 Simultaneous Colors
- PC/AT Compatible
- Hardware Cursor, Zoom, Pan
- Palette from 4096 to 16.7 Million Colors
- Viewable Resolution 1280 x 1024 x 8, Plus 4 Overlays
- Addressable Resolutions 2048 x 1024 x 8, Plus 4 Overlays

OMNI 1400 GDC



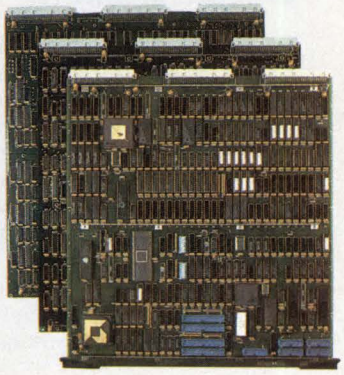
- PC/AT Compatible
- Up to 256 Simultaneous Colors
- Palette: Up to 16.7 Million Colors
- GKS Display List Processing Via OMNI 1500 DLP
- Hardware Cursor
- Viewable Resolution: Up to 1280 x 1024 x 8, Plus 2 Overlays
- Addressable Resolution: Up to 2048 x 1024 x 8, Plus 2 Overlays

OMNI 1500 DLP/OMNI 1500 GDS



- PC/AT Compatible
- DEC DMA Compatible
- GKS Display List Processing
- 80386/80387 Display List Processor
- 1 to 4 Megabytes of DLP Memory
- 4 RS-232-C Serial Ports
- OMNI 1500 GDS is an OMNI 1500 DLP plus 1 to 8 OMNI 1600 GDC's

OMNI 2000 GDS



- MULTIBUS II 9U x 400 mm
- DEC DMA Compatible
- GKS Display List Processing
- Viewable and Addressable Resolution: 1280 x 1024
- Hardware Cursor
- 2 Overlay Planes
- Modular Configurations
- Multiple Processors
  - Geometry Processor: Am29116
  - F.P. Coprocessor: Am29325
  - Graphic Coprocessor: Discreet
  - Peripheral Coprocessor: 80188
  - Display List Processor: 80386/80387

Omnicomp™ Graphics Corporation

Omnicomp™ Graphics (UK) Ltd.

Optimizing Computer Graphics . . . by Design.

1734 West Belt North • Houston, Texas 77043
713/464-2990 • Telex 285801 OMNICO UR
Fax 713/827-7540

PRODUCT DEBUTS

DSP system accepts variety of I/O modules

A family of digital signal processing (DSP) boards, modules and software for IBM PCs and compatibles, the DSPro line lets users tailor the I/O characteristics of each system. The flagship of the family is the PCI-20202C-1 DSP carrier board, which contains the TMS320C25 DSP chip from Texas Instruments. The board accepts a broad range of I/O modules that already exist as part of the manufacturer's PCI-2000 family. In addition to the DSP chip, the carrier

contains up to 96 kwords of zero-wait-state memory, interface circuitry for the I/O modules, and direct memory access capability for transfers to and from the PC's memory. A broad line of software is available for the DSPro line. DSP Library Plus offers a large selection of software routines that are callable from programs running on the PC.

Burr-Brown
1141 W Grant Rd
Tuscon, AZ 85705
Circle number 150

Booth #555

80386 single-board computer targets Multibus I

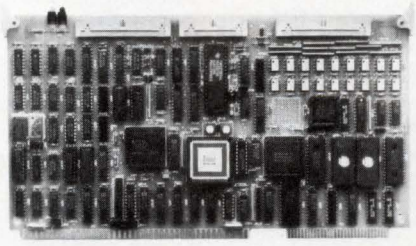
Based on a 20-MHz 80386 microprocessor, the CD21/8386 is a single-board computer for Multibus I applications that's hardware and software compatible with the Intel 386/3X series. The board features 1 or 4 Mbytes of dual-ported dynamic RAM and uses four double-word interleaved banks of fast-page RAM to achieve zero wait states for most accesses, while eliminating the need for caching. Sockets are provided for the 82380 32-bit direct memory access controller, the 80387 numeric processor and the Weitek 1167 numeric processor. Two SBX connectors and one RS-232 serial I/O port are offered, as well as full Multibus interface logic. The single-board computer is designed to accept 256-kbit, 1-Mbit or 4-Mbit DRAMs, providing on-board potential of up to 16 Mbytes of memory. With 4 Mbytes of RAM, the board is priced at $5,900.

Central Data
1602 Newton Dr
Champaign, IL 61821
Circle number 151

Booth #226

Multibus I adapter offers 5-Mbyte/s transfer rate

The Rimfire 1500 Multibus I small computer system interface (SCSI) host bus adapter uses a first-in, first-out architecture with a 1-kbyte buffer to decouple the SCSI and Multibus I. Supporting up to four 5¼- or 3½-in. single-, double- or quad-density drives, the board features a maxi-



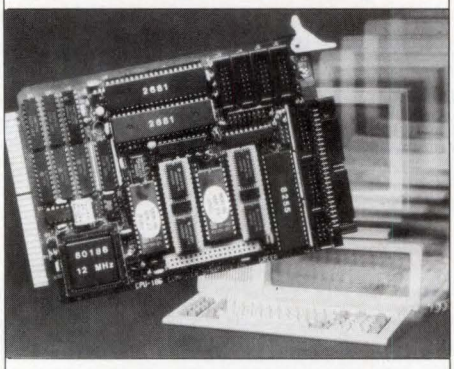
mum transfer rate of 5 Mbytes/s. Western Digital controller chips have been adopted on the device to provide the choice of either differential or single-ended SCSI bus options. Providing maximum asynchronous and synchronous transfer rates of 2 Mbytes/s and 5 Mbytes/s, respectively, the chips also support the disconnect/reconnect feature of SCSI. Single-piece price is $1,195.

Ciprico
2955 Xenium Ln
Plymouth, MN 55441
Circle number 152

Booth #449

STD bus SBC speeds to 12 MHz

Designed for reliable 16-bit performance in the industrial and OEM environments, the CPU-186 is a 80C186-based STD bus single-board computer with clock speeds of up to



12 MHz. The board lets system design engineers use an IBM PC-compatible computer to develop software for applications such as data acquisition, robotics control or automated testing. Supported by software tools for MS-DOS-compatible, ROM-based environments, the board hosts four serial ports and 24 parallel I/O lines for added industrial functionality. It also features up to 512 kbytes of battery-backed static RAM, up to 256 kbytes of EPROM, an SBX interface and CMOS construction. An on-board watch-dog timer lets the system recover if environmental situations force it off track, while a battery-backed real-time clock and four counter/timers complete the device's on-board functions.

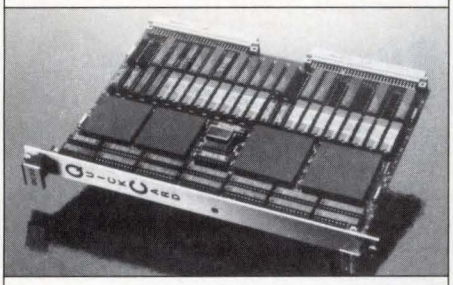
Computer Dynamics
107 S Main St
Greer, SC 29651
Circle number 153

Booth #447

VMEbus array processor delivers 32 MFlops

A dual-height, dual-depth 6U VMEbus board, the Quickcard is an array processor that provides 32 MFlops. The board fits into any VMEbus backplane without overloading existing power supplies, since it consumes only 25 W (5 A at +5 V dc) of power. Up to four processors can plug into

a system, permitting configurations with computation rates of up to 128 MFlops and 32 Mips. The board is available with 128 or 512 kbytes of dual-ported static RAM to allow concurrent I/O and processing. High-speed VMEbus peripherals transfer directly into the processor's memory



without host CPU intervention, permitting operation at full speed without waiting for data transfer. The Quickcard seamless programming environment offers both C and Fortran programmers a hand-coded scientific subroutine library. The board is priced at $9,500.

CSPI
40 Linnell Cir
Billerica, MA 01821
Circle number 154

Booth #330

PS/2 data-acquisition board provides 50-kHz throughput

Two data-acquisition boards for the IBM Personal System/2 Models 50, 60 and 80, the DT2901 and DT2905 permit simultaneous analog input, analog output and digital I/O operations. Designed for applications in temperature and pressure measurement, scientific research and process automation, the boards feature gap-free analog input and output data transfers, programmable gain, 12-bit analog resolution, and 16 lines of digital I/O. Two custom ICs arbitrate data flow between simultaneous 50-kHz analog input/output operations, as well as provide an interface to the Micro Channel bus. Each board contains an error-detection circuit, as well as two direct memory access channels for defining two data buffers in system memory. The dual DMA channels and buffers permit instantaneous chaining from one buffer to another, letting one buffer be filled by the board while data in the second buffer is being processed or stored.

Data Translation
100 Locke Dr
Marlboro, MA 01752
Circle number 155

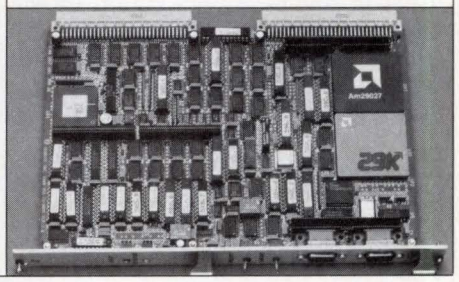
Booth #540

SBC uses RISC chip for 17-Mips performance

Based on the Am29000 reduced-instruction-set computer microprocessor from Advanced Micro Devices, the IV-9001 VMEbus single-board computer provides a sustained execution rate of over 17 Mips from 16 kbytes of cache and up to 16 Mbytes of dynamic RAM. The board utilizes a unique memory architecture that lets local buses achieve 200-Mbyte/s transfer rates through interleaved DRAM memory, same-page algorithms and a coherent cache design. The base system consists of a 6U VMEbus board with the Am29000 25-MHz microprocessor, a 16-kbyte data cache, two single serial I/O ports, local board control, and the VMEbus interface and debug monitor in ROM.

Ironics
798 Cascadilla St
Ithaca, NY 14850
Circle number 156

Booth #110



PRODUCT DEBUTS

STD bus SBC speeds to 20 MHz

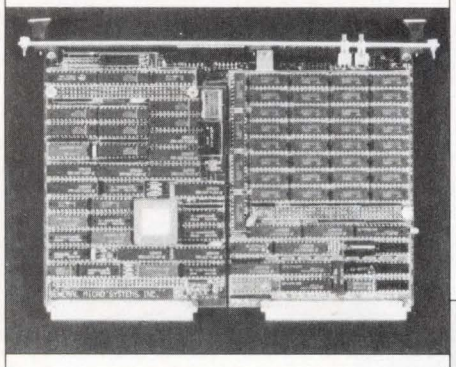
An IBM PC AT-compatible single-board computer, the LPM-286AT uses an 80286 microprocessor and a new enhanced AT (NEAT) chip set to achieve speeds up to 20 MHz. The board features 512 kbytes of RAM, an 80287 coprocessor socket, two RS-232 serial ports, a Centronics parallel port, a real-time clock, a keyboard controller and a speaker. Fully buffered to the STD bus, the processor can operate at either 10, 12, 16 or 20 MHz, and requires a single +5-V supply. The NEAT chip set can work from different CPU speeds up to 20 MHz, while still using lower cost, slower memories.

Win Systems
PO Box 121361
Arlington, TX 76012
Circle number 157

Booth #317

VMEbus SBC expands to 1 Mbyte

A VMEbus single-board computer based on a 32-bit 68030 microprocessor, the GMSV17 features up to 1 Mbyte of dual-ported, zero-wait-state static RAM. A memory-management unit boosts CPU clock speed to 25 MHz, while the dual cache memory provides an instruction cache and a



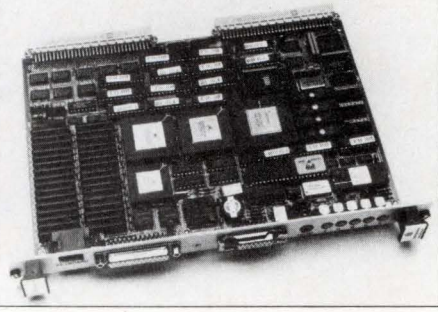
data cache with Harvard architecture. A 68882 floating-point coprocessor further supports full 32-bit processing. Local memory can be protected from unwanted writes, yet can still provide dual porting to the rest of the multiprocessor system. Up to 512 kbytes of EPROM or 128 kbytes of EEPROM can reside on the board with an additional 1 Mbyte of dual-ported SRAM or 4 Mbytes of dynamic RAM. The board both originates and services interrupts on the VMEbus, while a location monitor/mailbox interrupt technique allows real-time multiprocessing. The double Eurocard device is available for extended temperature applications.

General Micro Systems
4740 Brooks St
Montclair, CA 91763
Circle number 158

Booth #417

SBC functions as real-time target or Unix platform

Based on the Motorola 68020 microprocessor, the Liberator-SBC is a VMEbus single-board computer designed for use as a Unix platform or as a real-time target in one of the manufacturer's Optimum Series systems. The board houses a high-resolution graphics controller, two serial ports, an EPROM for storing real-time software, logic to provide direct memory access and a floating-point coprocessor. Direct connection to disk or tape is achieved via twin synchronous or asynchronous small computer system interfaces, while networking is accommodated on Ethernet. The architecture of the single-board computer combines the 32-bit microprocessor with a closely coupled 16-Mips, reduced-instruction-set-based peripheral processor. Operating at speeds of 16 or 20 MHz, the system can detect a peripheral interrupt, reschedule and carry out a task in approximately 100 ns. The processor, the VME interface and a DMA processor act as three bus masters that connect to the primary bus and can access each other, the



main memory, the firmware EPROM or the video storage.

Integrated Solutions
1140 Ringwood Ct
San Jose, CA 95131
Circle number 159

Booth #511

Memory board expands STD DOS applications

The ZT 8825 memory system expands memory capabilities to the STD bus. For STD DOS applications with solid-state mass-storage requirements, the board provides a potential of 2 Mbytes of PROM or RAM disk in a single backplane slot. For STD DOS applications that require a large amount of main memory, the board functions as expanded memory. For STD bus OEM applications without STD DOS, the board can be used as a standard 1-Mbyte memory board. The board uses the expanded memory specification developed by Lotus, Intel and Microsoft to expand the 640-kbyte conventional capacity of a PC in the DOS environment.

Ziatech
3433 Roberto Ct
San Luis Obispo, CA 93401
Circle number 160

Booth #441

VMEbus mother board hosts eight Transputers

The IMS B014 module mother board is a VMEbus-compatible device with slots for eight size 1 Transputer modules. The standard-depth, double-height card uses two link crossbar switches to change the Transputer link connections running between modules, letting any network be configured. In addition, 24 links are brought to edge connectors, with eight on the back P2 connector and the remaining 16 arranged on the front connector as two pairs of eight. The board has a slave interrupting interface to the VMEbus that provides a single bidirectional link and a subsystem port. The interface appears as a number of registers in the A16 address space on the bus, which

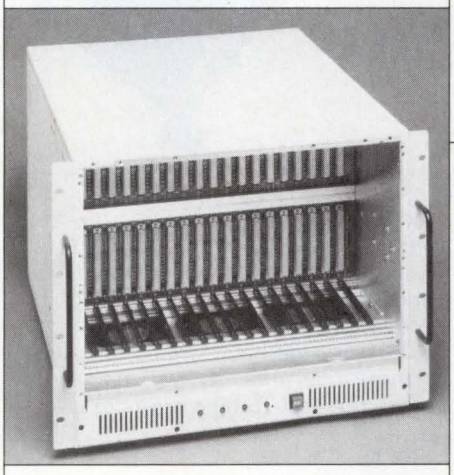
may be accessed by any VMEbus master. These registers are then used to program and interact with the board. The mother board conforms to VMEbus specification Rev C.1.

Inmos
PO Box 16000
Colorado Springs, CO 80935
Circle number 161

Booth #341

System enclosures house Multibus and VME systems

The 509 Series of enclosures for Multibus I, II and VMEbus systems are built of aluminum and can be configured with a variety of power supplies from 160 to 700 W. The enclosures feature a removable fan/cooling plenum, easy access to the J2/P2 sections of backplanes, light-emitting diodes to warn of power-supply trouble and interconnect I/O panels for system customization.



Mupac
Mupac Dr
Brockton, MA 02401
Circle number 162

Booth #507

IPI host interface adapter addresses VMEbus systems

A host interface adapter for VMEbus-based systems and intelligent peripheral interface (IPI) level 2 disk drives, the V/IPI 4260 Cougar is capable of data-transfer rates in excess of 36 Mbytes/s. The device, which can interface to as many as eight different IPI-2 disk drives, incorporates a proprietary Buspacket Interface for high-speed control. Other features include a 256-kbyte data buffer that's expandable to 512 kbytes, a Unix-optimized caching algorithm and a VMEbus master with 8-, 16- or 32-bit transfers.

Interphase
2925 Merrell Rd
Dallas, TX 75229
Circle number 163

Booth #118

VMEbus CPU hosts 16-MHz 68020

A single-board computer based on a 16-MHz 68020 microprocessor, the MS-CPU220 is a universal server platform that provides the basic intelligence, memory and control needed for a server architecture system. The VMEbus board features an interface chip with multiprocessing capabilities, two 32-pin ROM/EPROM sockets, 1 Mbyte of zero-wait-state dynamic RAM, an EEPROM for storing configuration information and an optional MC68881 floating-point coprocessor. Personality modules can be added to the board to provide peripheral functions such as network interfaces, disk controllers and serial ports. Interface with standard or thin Ethernet-connected systems is also possible. Software support includes Vxworks, a real-time Unix-compatible operating system featuring sockets and Transmission Control Protocol/Internet Protocol.

Matrix
1203 New Hope Rd
Raleigh, NC 27610
Circle number 164

Booth #210

PRODUCT DEBUTS

Memory I/O board features 16 byte-wide sockets

The VME-9100D multifunction memory I/O board features 16 battery-backed byte-wide memory sockets that accept JEDEC standard RAM, ROM, EPROM or EEPROM devices in virtually any combination. The board is available with 0 to 512 kbytes of static CMOS RAM or can accept up to 1 Mbyte of ROM/EPROM/EEPROM. Three parallel ICs provide 60 TTL I/O lines with automatic handshaking and pattern detection, along with nine 16-bit counter timers. Single-unit pricing with no memory installed is $1,200.

Logical Design Group
6301 Chapel Hill Rd
Raleigh, NC 27607
Circle number 165

Booth #252

68030 VMEbus SBC targets real-time applications

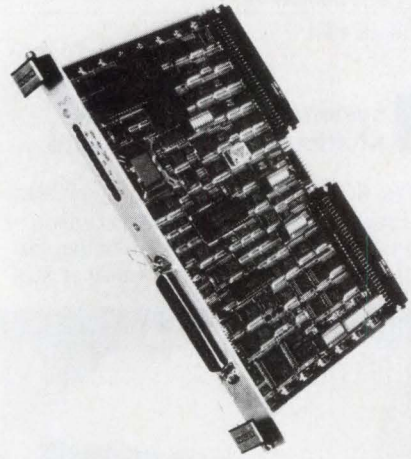
A single-height VME single-board computer, the MZ8130 incorporates a Motorola 68030 CPU along with 1 Mbyte of dynamic RAM and 1 Mbyte of EPROM for real-time applications. The board features two RS-232 serial ports, an interrupt handler and mailbox interrupt support, as well as an optional time-of-day clock with battery back-up. A master/slave interface to the VMEbus is included, while an optional MXbus expansion interface allows connection of standard and custom expansion modules for enhanced memory, I/O and other functions. With 1 Mbyte of DRAM, the price is $2,495.

Mizar
1419 Dunn Dr
Carrollton, TX 75006
Circle number 166

Booth #316

Intelligent adapter connects VMEbus to SCSI

The NCR ADP-33 is an intelligent VME host adapter that lets a VMEbus-based host processor access peripheral devices and communicate with other host processors on the small computer system interface (SCSI). The adapter boasts a guaranteed SCSI transfer rate of 2.6 Mbytes/s in asynchronous mode and 4 Mbytes/s in synchronous mode. Compatible with industry-standard SCSI ANSI X3.131-1986, the implementation parameters of the board include arbitration, reselection and parity. Data path is selectable for either 16 or 32 bits with I/O management for up to 64 concurrent SCSI operations. The device supports the SCSI initiator mode for host-to-target communications, as well as target mode for host-to-host transfers.



NCR
3718 N Rock Rd
Wichita, KS 67226
Circle number 167

Booth #426

I/O subsystem family connects 128 analog devices

An expandable I/O subsystem family lets up to 128 analog inputs and outputs be attached to any STD bus system through a single STD bus card. The family includes the SB8280 single-slot STD bus card and a series of interface racks that are chassis- or panel-mounted adjacent to the STD bus card rack, then connected to the card through a 34-pin ribbon cable daisy chain. All interface racks provide terminal strips for connection to sensors and controls in industrial measurement systems. The APB16 analog I/O rack provides 16 sockets

for installation of various signal conditioning modules, each providing 1,500-V isolation and direct connection to field sensors and controls, while the AIN16 analog input rack hosts 16 single-ended or eight differential nonisolated analog inputs. Any combination of up to eight of these racks can be attached to the STD bus. Single-quantity pricing starts at $375 for the SB8280, $250 for the APB16 and $335 for the AIN16.

Micro/Sys
1011 Grand Central Ave
Glendale, CA 91201
Circle number 168

Booth #421

Software package allows VME code portability

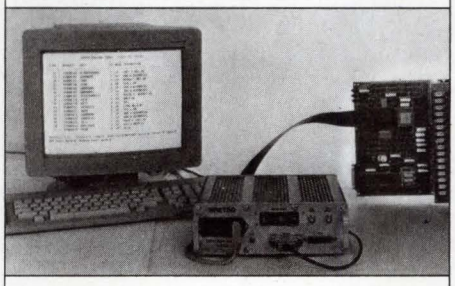
The VMEexec is a collection of support packages integrated to provide real-time performance within a Unix System V environment. The base package consists of download and start utilities, C bindings, make files, an assembler, a linker and a debug extension. These software interfaces let VMEbus developers design an application code that's directly portable between projects, regardless of the real-time kernel, and to combine software products from various vendors that conform to the standard interfaces. The executive of the package is based on the real-time executive interface definition, which defines a core set of operating system kernel services. Source code that conforms to these interfaces will execute as defined in all real-time executive environments, facilitating the development of application source code that's directly portable across all real-time executive implementations.

Motorola Microcomputer Div
2900 S Diablo Way
Tempe, AZ 85282
Circle number 169

Booth #406

Personal Micro Analyzer targets 68020 systems

The Personal Micro Analyzer is a stand-alone development tool intended primarily for testing, debugging and performance measurements in Motorola 68020-based, 32-bit systems. The device features a disassembler for 68020 program code, a cache



hit-rate indicator, 2 kwords of program trace or processor bus trace and a time tag.

Vmetro
2500 Wilcrest
Houston, TX 77042
Circle number 170

Booth #414

VMEbus 80386 processor runs PC AT software

A two-card PC AT processor module for the VMEbus, the XVME-683 combines the processing power and rugged mechanical packing of the VMEbus with the application software available for the PC AT. The module hosts a 16-, 20- or 25-MHz 80386 processor, a cache controller and 32 kbytes of zero-wait-state memory. Additional features include 1 or 4 Mbytes of dual-ported RAM, ROM-resident BIOS, a battery-backed clock, two serial and one parallel port, and a keyboard interface. The module will accept either the 80387 or the Weitek math coprocessor.

Xycom
750 N Maple Rd
Saline, MI 48176
Circle number 171

Booth #324

PRODUCT DEBUTS

Synchronous controller transfers 12 Mbytes/s

Based on the 68020 microprocessor, the PT-VME330 is a 16-port high-speed synchronous communication controller for the VMEbus. The board uses a split-bus architecture built around a 1-Mbyte dual-ported dynamic RAM data buffer. Up to eight dual-channel Z8530 serial communications controllers are coupled to the DRAM buffer by a proprietary 32-channel direct memory access controller configured to support one channel for transmit and one for receive, providing up to 16 full duplex serial communications ports. The DMA controller offers an aggregate bandwidth of 4 Mbytes/s, which lets 16 ports operate concurrently at 56 kbits/s, or one port operate at 1.5 Mbits/s. The 68020 microprocessor supervises all communication protocol on the board and moves data to and from the VMEbus at over 12 Mbytes/s. A variety of communications interface options are supported, including RS-232C, MIL-STD-188C, RS-422 and RS-485.

Performance Technologies
435 W Commercial St
Rochester, NY 14445

Circle number 172

Booth #256

RISC VMEbus SBC offers 6 MFlops at 20 MHz

Designed around the Motorola 88000 reduced-instruction-set computer microprocessor, the TP880V is a VMEbus single-board computer that boasts 17-Mips, 6-MFlops performance at 20 MHz. The CPU is interfaced to dual 88200 cache memory-management devices for the instruction and data buses, each providing 16 kbytes of zero-wait-state memory. Standard memory size of 4 Mbytes can expand to 16 Mbytes, is parity protected, and is accessible from the 88000, the VMEbus interface and the I/O subsystem. An I/O processor/direct memory access controller combination offloads I/O overhead from the main RISC CPU and provides diagnostic capabilities as well as a programming interface. The 53C90 enhanced small computer system interface provides asynchronous or synchronous data transfers occurring into main dynamic RAM in 32-bit hardware-controlled operations. Two RS-232 ports, a battery-backed real-time clock, 128- kbyte to 1-Mbyte EPROM and 64 kbytes of static RAM complete the on-board I/O facilities.

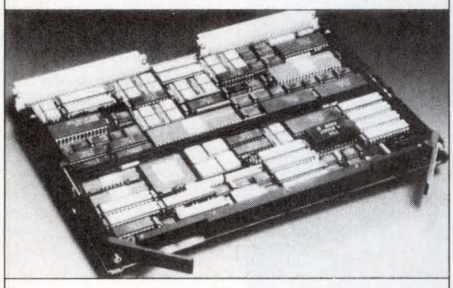
Tadpole Technology
1601 Trapelo Rd
Waltham, MA 02154

Circle number 173

Booth #426

SCSI/VMEbus interface built to military specs

An intelligent VMEbus/small computer system interface (SCSI) board for military or ruggedized environments, the PMV 68 SCSI-1 uses a 68000 processor for high-speed data transfers. All local resources are



managed by the microprocessor, including direct memory access and SCSI control, operating under the direction of 16 kbytes of EPROM resident firmware. The board also provides 16 kbytes of static RAM that's dual ported to the VME and local system bus. Configurable as a target or initiator, the device provides sustained asynchronous SCSI transfer rates of up to 1.5 Mbytes/s, with DMA transfers of up to 32 bits over the VMEbus. The board can be connected either to another SCSI controller to which multiple mass-memory peripherals are connected, or directly to a mass-storage device.

Radstone Technology
One Blue Hill Plaza
Pearl River, NY 10965
Circle number 174

Booth #218

Multibus I processor board expands to 8 Mbytes

A Multibus I processor board based on the 68020 microprocessor, the MPU-28 combines 32-bit operation at 20 MHz with up to 8 Mbytes of onboard dual-ported RAM for real-time applications in data acquisition, image processing and robotics. When configured for 1, 2, or 4 Mbytes of dual-ported RAM, the board occupies a single Multibus slot, while the 8-Mbyte configuration occupies two slots. An optional memory-management unit (MMU) is available, as well as a 68881 or 68882 floating-point math coprocessor. With the MMU, the CPU can be operated at 20 MHz with one wait state. Other features include parity protection of onboard dynamic RAM, one 8- or 16-bit iSBX connector and two multiprotocol full-duplex serial ports capable of synchronous operation at up to 64 kbytes/s. A mailbox lets other Multibus masters reset, interrupt and, via a status register, monitor the CPU.

SBE
2400 Bisso Ln
Concord, CA 94520
Circle number 175

Booth #229

Real-time software supports SPARC

The Vxworks real-time operating system is available for all implementations of Sun Microsystems' SPARC technology. The SPARC port will provide all of the real-time features of Vxworks, including a fast multitasking kernel with pre-emptive scheduling, fast interrupt response, intertask communications and synchronization facilities, and Unix-compatible memory management. Multiprocessor facilities and a user interface shell are also featured, as well as an I/O and a file system. A complete implementation of the 4.3 BSD version of the Unix O/S network package, including Transmission Control Protocol/Internet Protocol as well as Sun's Network File System and Remote Procedure Calls, will also be supported.

Wind River Systems
1316 Sixty-Seventh St
Emeryville, CA 94608
Circle number 176

Booth #321

MAJOR SYSTEM COMPONENTS

Linear power supplies survive in low-power applications

John H. Mayer, Senior Associate Editor

Although they don't offer the efficiency of switchers, industrial linear power supplies like Lambda's LN Series offer output ripple and noise as low as 5 mV peak-to-peak. Available in five single-ouput and five dual-output packages up to 48 V dc, this series meets MIL-STD-810 environmental conditions.

Few would disagree that over the past decade switch-mode power supplies have virtually usurped the role of linear power supplies. By operating at continually higher frequencies and taking full advantage of evolutionary improvements in ICs and printed circuit board design, switchers are now offering highly efficient, yet lightweight, power sources in smaller, cooler running packages. Not surprisingly, these developments have led many designers to consider linear supplies outdated in electronic system design. "It's our feeling that linear supplies for new designs are pretty much a dead animal," observes Fred Heath, president of the Power Systems Division of Valor Electronics (San Diego, CA).

But judging by the actions of some vendors, linear power supplies aren't yet extinct. A number of vendors, led by Power-One (Camarillo, CA), are offering broad product lines of linears in a wide range of configurations, while other companies are continuing to add to their existing product lines. Late last year, for example, Deltron (North Wales, PA) added 10 new models to its World Series line in single-, dual- and triple-output configurations. And the company introduced 30 single-output industrial linears with output voltages from 5 to 28 V. The Q series also supplies total output power from 15 to 260 W.

Another manufacturer, Sola (Elk Grove Village, IL), unveiled this summer a 25-model series with outputs ranging from 15 to 90 W in single-, dual- and triple-output configurations. Dubbed the Silver line, the open-frame units are UL (Underwriters Laboratories) recognized and CSA (Canadian Standards Association) certified.

The size, efficiency and weight disadvantages of linear power supplies vis-a-vis switchers are most acute at higher power levels. The dissipative regulating element in a typical linear supply offers about 50 percent efficiency, compared to the 75 percent efficiency of many switchers. In addition, the linear supply demands a heavy 50- to 60-Hz transformer, while a switcher rectifying the ac directly from the power line and operating at high frequencies can retain its small size and weight. With these liabilities, few manufacturers are building linears at over 300 W.

But linears still have a role to play, particularly in low-power applications (under 50 W). At that level their drawbacks are less acute—their line frequency transformers are still relatively small and their dissipated power isn't as significant—and they still cost less than switchers.

■ Low-noise applications

For excellent line and load regulation, a linear power supply is still the answer: regulation on a linear is often an order of magnitude better than comparable switchers. Lower noise is also an asset. Many linears generate less than 1 mV peak-to-peak (p-p) of noise, compared to 10 mV p-p for a high-performance switcher.

Given these advantages, it's not surprising that linear supplies are still used in applications requiring well-regulated voltages with extraordinarily low ripple. Some of these applications include precision laboratory equipment demanding very stable outputs or sensitive data-acquisition circuits using sensors, amplifiers, sample and holds, or analog-to-digital converters to convert dc voltages to digital form. Linears are also found in highly regulated automatic test equipment systems, as well as in some low-voltage signal-processing circuits, where unwanted noise can play a destructive role. "Analog circuitry can't tolerate the higher noise of the switching power supply," says John Haines, technical support specialist for Power-One.

In low-power medical equipment, for example, supplies such as those from Power-One, built with split-bobbin transformers that separate and isolate the primary and secondary coils, minimize leakage to power lines. In systems that monitor patients and need to keep leakage current under 10 μA, these design characteristics are mandatory. Some power-supply manufacturers add a Faraday shield between the windings in the transformer to reduce capacitive coupling between the primary and secondary windings.

Model	Max power output (W)	No. of outputs	Output range	Output ripple (mV p-p)	Transient response (μs)	Dimensions (L×H×W in.)	Price	Comments
AAK 747 River St, Haverhill, MA 01830 (508) 373-3769								**Circle 100**
MT series	5 to 40	3	2V to 60V @ 3A to 0.1A	0.5 to 1	50	3.5×5×0.9 and up	$31.90 to $152	fold-back and current limit
SM, SD series	1 to 30	1,2	2V to 60V @ 3A to 0.1A	0.5 to 1	50	2.5×3.5×0.9 and up	$38 to $91	adjustable in 1 V increments
MM, MD series	0.9 to 3	1,2	5V to 24V @ 0.1 to 0.03A	1 to 1.5	50	2×2×0.9	$31.90 to $152	low priced minis
CM,CD series	1 to 30	1,2	2V to 60V @ 3A to 0.1A	0.5 to 1	50	2.5×3.5×0.9	$38 to $91	same as above
ALT, LT series	5 to 40	3	2V to 40V @ 4A to 0.3A	0.5 to 1	50	3.5×5×0.9 and up	$62 to $145	miniature bench type
LM, LD series	5 to 25	1,2	2V to 40V @ 3 to 0.1A	0.5 to 1	50	2.5×3.5×0.9 and up	$62 to $145	miniature bench type
ACDC Electronics 401 Jones Rd, Oceanside, CA 92054 (619) 439-4200								**Circle 101**
ECV family	15 to 115	1,2,3	5V to 24V	3	30	varied	$32.95 and up	open frame
OEM family	15 to 260	1,2,3	5V to 28V	20	50	varied	$158 and up	open frame, cover opt
Acme Electric 20 Water St, Cuba,NY 14727 (716) 968-2400								**Circle 102**
SPS 15	12	1	5V to 28V @ 1.5A to 0.4A	5	50	4×4.8×2.3	$37.44	open frame, UL, CSA
SPS 30	30	1	3V to 250V @ 3A to 0.05A	5	50	4×4.8×2.5	$41.60	same as above
SPS 40	40	1	5V to 28V @ 5A to 1.6A	5	50	4.9×5.7×3.3	$75.95	same as above
SMP50-2	30	4	5V to 12V @ 3A to 0.4A	5	50	3.4×4.3×6.8	$130.00	open frame, UL, CSA; for μPs
SMP60-1/2	40	3,4	5V to 12V @ 5A to 0.4A	5	50	3.4×4.3×6.8	$147.68	open frame, UL, CSA; for μPs
SPS 30TA	17	3	5V to 15V @ 2A to 0.25A	5	50	3.4×4.8×3.9	$90.48	open frame, UL, CSA
SPS 50TA	40	3	5V to 15V @ 3A to 0.7A	5	50	4.9×7.5×4	$124.80	same as above
SPS 40T	35	3	5V to 15V @ 2.5A to 0.75A	5	50	4.8×5.5×2.9	$94.64	same as above
SPW-1	22.5	1	5V to 28V @ 3A to 1A	5	50	4×4.9×2	$36.33	open frame, worldwide design
SPW-2	45	1	5V to 28V @ 6A to 2A	5	50	4.9×5.6×3	$55.07	same as above
SPW 15D –0.8	24	2	12V to 15V @ 1A to 0.8A	5	50	4×6.5×2	$47.35	same as above
SPW 16WT	24	3	5V to 15V @ 2A to 0.4A	5	50	4×6.5×2	$60.58	same as above
SPW 40WT	41	3	5V to 15V @ 3A to 0.8A	5	50	10.3×4×3	$83.73	same as above
Acopian PO Box 638, Easton, PA 18044 (800) 523-9478								**Circle 103**
E series	—	1,2,3	1V to 75V @ 30 mA to 2.5A	0.5 to 1	—	2.3×1.8×1 and up	—	miniature regulated, short-circuit protected
EB series	—	1,2	1V to 75V @ 0 to 2.5A	1	—	3.5×2.5×0.2	—	terminal strip connectors
A series	—	—	1.5V to 150V @ 32A to 0.2A	0.25 to 1.5	—	6.6×5.1×3.4 and up	$95 to $555	regulation of ±0.005%. OVP opt
B series	—	—	3V to 200V @ 4A to 0.1A	0.25 to 1.5	—	3.7×1.6	$95 and up	general purpose, ±0.1% reg., OVP opt
NT/TN series	—	—	1V to 150V @ 0 to 3.5A	0.25 to 1	—	6.6×3.8 and up	$125 to $195	narrow profile
MX/HX series	—	1	0 to 150V @ 0 to 16A	0.25	—	6.6×5.1×3.4 and up	$155 to $475	adjustable current limiting

KEY: CSA = Canadian Standards Association; IEC = International Electro-technical Commission; OVP =over volt protection; UL = Underwriters Laboratories; VDE = Verband Deutscher Electrotechniker

■ LOW-POWER LINEAR SUPPLIES

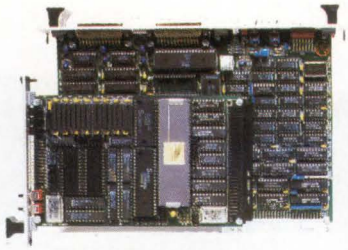
Model	Max power output (W)	No. of outputs	Output range	Output ripple (mV p-p)	Transient response (μs)	Dimensions (L x H x W in.)	Price	Comments
Calex Manufacturing 3355 Vincent Rd, Pleasant Hill, CA 94523 (415) 932-3911								**Circle 104**
1.5.2000	10	1	5V @ 0 to 2000mA	2	50	3.5×2.5×1.5	$125	encapsulated, short circuit, OVP
2.12.360	8.7	2	±12V @ 0 to 360 mA	2	50	3.5×2.5×1.5	$125	same as above
3.15.1000	8	3	5V @ 0 to 1000 mA; ±15V @ 0 to ±100 mA	2	50	3.5×2.5×1.5	$150	same as above
Computer Products 2900 Gateway Dr, Pompano Beach,FL 33069 (305) 974-5500								**Circle 105**
PM 300 series	2.5 to 15	1,2,3	5V to 24V @ 2A to 100 mA	1 to 2	50	2.7×4×1.5	$63.36	encapsulated, chassis mountable, split-bobbin wound
PM 500 series	1 to 10	1,2,3	5V to 24V @ 2A to 25mA	2 to 5	50	1.8×2.3×1; 2.5×3.5×0.9	$41.76	encapsulated, PC mountable, split-bobbin wound
World Std series	15 to 125	1,2,3	5V to 28V @ 9A to 0.8A	1	50	1.6×4.9×4; 2.5×5.6×4.9; 2.8×7×4.9	$29	open frame, world wide input
Deltron Box 1369, Wissahickon Ave, N Wales,PA 19454 (215) 699-9261								**Circle 106**
World series	15 to 240	1,2,3	5V to 48V	5	—	4×5×2 to 4×5×15	$31 to $153	open frame, VDE, UL, IEC, CSA
Elpac Electronics 3131 S Standard Ave, Santa Ana, CA 92705 (714) 979-4440								**Circle 107**
SOLV 15	15	1	5V to 24V @ 3A to 0.75A	—	50	4.9×2.1×4	$30	output ±5% adjustable, OVP std
SOLV 30	30 to 48	1	5V to 48V @ 6A to 1A	—	50	5.6×3×4.9	$50	output ±5% adjustable, OVP opt
SOLV 45	45 to 72	1	5V to 24V @ 9A to 3A	—	50	7×2.9×4.9	$80	same as above
UPS 14	12	2	12V @ 0.5A	0.1	50	3.3×2.3×4.4	$50	±5% V adjustable, OVP opt
UPS 30	30	2	5V to ±15V @ 3A to 1.2A	0.1	50	7×3×4.9	$65	same as above
UPS 45	45	3	5V to ±15V @3A to 1.2A	0.1	50	10.5×3.2×4.9	$90	same as above
Kepco 131-38 Sanford Ave, Flushing, NY 11352 (718) 461-7000								**Circle 108**
OPS 500B	20	1	0 to 500V @ 0 to 0.04A	—	500	12.9×8.3×5.2	$881	programmable voltage amplifier
PAT 7-2	14	1	0 to 7V @ 0 to 2A	0.5	50	3.3×6.4×4.9	$301	programmable voltage stabilizer module
PAT 15-1.5	22.5	1	0 to 15V @ 0 to 1.5A	0.5	50	3.3×6.4×4.9	$301	same as above
PAT 21-1	21	1	0 to 21V @ 0 to 1A	—	50	3.3×6.4×4.9	$301	same as above
PAT 40-0.5	20	1	0 to 40V @ 0 to 0.5A	0.5	50	3.3×6.4×4.9	$301	same as above
PAT 72-0.3	21.6	1	0 to 72V @ 0 to 0.3A	0.5	50	3.3×6.4×4.9	$301	same as above
PAT100-0.2	20	1	10 to 100V @ 0 to 0.2A	0.5	50	3.3×6.4×4.9	$301	same as above
PCX7-2 MAT	14	1	0 to 7V @ 0 to 2A	3	50	14.9×2.8×5.2	$486	programmable voltage stabilizers
PCX21-1 MAT	21	1	0 to 21V @ 0 to 1A	—	50	14.9×2.8×5.2	$486	same as above

Model	Max power output (W)	No. of outputs	Output range	Output ripple (mV p-p)	Transient response (μs)	Dimensions (L × H × W in.)	Price	Comments
Lambda Electronics 515 Broad Hollow Rd, Melville, NY 11747 (516) 694-4200								**Circle 109**
LX series	20 to 225	1	5V to 28V @ 4A to 1A, 45A to 17A	5	50	6.5×3.8×3.2 to 16.5×7.5×4.9	$389 to $1,723	ruggedized, enclosed
LD series	15 to 125	1,2,3	5V to 28V @ 3A to 0.8A, 25A to 9.3A	5	50	4×1.6×4.9	$74 to $296	open frame, 110/220
LZ series	2.25 to 4.5	1,2	5V to 28V @ 0.45A to 0.08A, 0.9A to 0.3A	5	50	2.5×3.5×0.9	$75 to $186	PC board mountable, plastic cover
LN series	15 to 110	1,2	5V to 28V @ 3A to 0.8A, 22A to 8A	5	50	4×1.8×4.9 to 11×4.9×4.4	$118 to $326	enclosed, ruggedized, Mil-Std
LD series	27 to 110	1	5V to 150V @ 5.4A to 0.4A, 22A to 1.1A	1	50	5.6×4.9×2.6 to 11×4.9×4.4	$247 to $466	enclosed, ruggedized, Mil-std
LC series	13.5 to 80	1	5V to 150V @ 2.7A to 0.12A	1	50	6.5×3.8×3.2 to 9.4×4.9×4.9	$378 to $812	enclosed, ruggedized, Mil-Std
Maxim Integrated Products 120 San Gabriel Dr, Sunnyvale CA 94086 (408) 737-7600								**Circle 110**
Max666	0.5	1	1.3V to 16V @ 0 to 40 mA	1	—	0.2×0.24×0.06	$2.45	micropower, 5μV quiesent current
Max667	2.5	1	1.3V to 16V @ 0 to 250 mA	1	100	0.2×0.24×0.06	$3.50	250 mA output
Max663	0.5	1	1.3V to 16V @ 0 to 40 mA	1	—	0.2×0.24×0.06	$2.15	micropower, 5 μA quiesent current
Max664	0.5	1	–1.3V to –16V @ 0 to 40 mA	1	—	0.2×0.24×0.06	$2.63	micropower, 6 μA quiescent current
Max600 series	0.5	1	1.3V to +10V @ 0 to 50 mA	1	—	0.2×0.24×0.06	$0.95 to $2.75	AC to DC regulator
Power One 740 Calle Plano, Camarillo, CA 93010 (800) 235-5943								**Circle 111**
HB5-310VP-A	15	1	5V @ 3A	5	2	4.9×4×2.1	$31.96	open frame, auto foldback/current limit
HC12 3.4-A	40.8	1	12V @ 3.4A	5	2	5.6×4.9×2.9	$48.45	remote sense
HC15-3-A	45	1	15V @ 3A	5	2	5.6×4.9×2.9	$48.95	same as above
HB2-3-A	6	1	2V @ 3A	5	2	4.9×4×2.1	$33.90	open frame, auto foldback, current limit
HE2-18-A	36	1	2V @ 18A	5	2	14×4.9×3.4	$116.35	same as above
HB250-0,1-A	25	1	–250V @ 0.1A	3	2	4.9×4×2.1	$38.75	open frame, auto foldback, current limit
HA5-1.5/OVP-A	7.5	1	5V @ 1.5A	5	2	4.9×4×2.1	$27.11	open frame, OVP, auto foldback, current limit
HC5-6/OVP-A	30	1	5V @ 6A	5	2	5.6×4.9×2.9	$53.30	same as above, remote sense
HB120-0.2-A	24	1	120V @ 0.2A	3	2	4.9×4×2.1	$38.75	open frame, auto foldback, current limit
HTAA-16W-A	20	3	5V to –15V @ 2A to 0.4A	5	2	6.5×4×2.1	$53.30	open frame, auto foldback, current limit
HB24-1.2-A	28.8	1	24V @ 1.2A	3	2	4.9×4×2.1	$31.96	open frame, auto foldback, current limit
HC48-1-A	48	1	48V @ 1A	3	2	5.6×4.9×2.9	$53.30	open frame, auto foldback, current limit

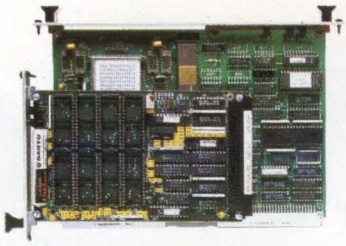
■ LOW-POWER LINEAR SUPPLIES

Model	Max power output (W)	No. of outputs	Output range	Output ripple (mV p-p)	Transient response (μs)	Dimensions (L×H×W in.)	Price	Comments
Power Switch 50 Graphic Pl, Moonachie, NJ 07074 (201) 641-4544								**Circle 112**
PLS series	15 to 45	1	5V to 28V @ 1A to 9A	3	50	4×4.9×1.6 to 7×4.9×2.8	$24 to $67	OVP std on 5V output
PLD series	24 to 45	2	±12V to ±15V @ 1A to 1.5A	3	50	6.5×4×1.6 to 7×4.9×2.5	$39 to $49	open frame
PLT series	20 to 40	3	5V to ±12V @ 3A to 0.4A	3	50	6.5×4×1.6 to 10.3×4×2.5	$45 to $69	OVP std on 5V output, open frame
Powertec 20550 Nordhoff St, Chatsworth,CA 91311 (818) 882-0004								**Circle 113**
2CC5-9B	45	1	5V to 6V @ 9A to 7.5A	2	—	4.9×3.2×7	$90	open frame, optional OVP
2K15D-1.3B	36	2	12V to 15V @ 1.5A to 1.3A	2	—	4×3×7.9	$82	same as above
2P30-TB	30	3	5V to 6V @3 to 2.5A	2	—	4×2.7×8	$92	same as above
RTE Power/Mate 2727 Kurtz St, San Diego, CA 92110 (800) 843-8544								**Circle 114**
IMA Case B	28	1	5V to 24V @ 3A to 1.2A	3	50	4.8×4×1.6	$32	split bobbin on transformer
IMA Case C	50	1	5V to 24V @ 6A to 2.4A	3	50	5.6×4.8×2.5	$50 to $52	split bobbin on transformer
ITA Case C	44	2	12V @ 1.8A	3	50	7×4.8×2.5	$53	split bobbin on transformer
Sola 1717 Busse Rd, Elk Grove Village, IL 60007 (312) 439-2800								**Circle 115**
Silver line	15 to 90	1,2,3	5V to 28V	—	—	—	—	25 models, OVP std on 5V, 0.05 percent line, load reg.
Sorensen Company 5555 N Elston Ave, Chicago,IL 60630 (312) 775-0843								**Circle 116**
QSA Case I	26	1	0 to 10V to 35 to 60V @ 0.44 to 1.5 A	3	—	3.3×3.9×6.3	$390	enclosed, remote programming & control
QSA Case II	50	1	0 to 10V to 35 to 60V @ 0.5A to 4A	3	—	3.3×5.1×6.3	$450	enclosed, remote programming & control
PTM Case I	20 to 39	1	4.5V to 29V @ 1.4 to 4A	5	2	3.3×3.9×6.5	$310	enclosed, OVP, remote sense & control
PTM Case II	35 to 56	1	4.5V to 29V @ 2A to 7A	5	—	3.3×5.1×9.5	$350	same as above
PTM (dual) I	25	1	±12V to ±15V @ 0.8A to 3A	5	2	3.3×3.9×6.5	$315	same as above
KMS Case J	1.25	1	5V to 28V @ 40 mA to 250 mA	1	2	1.8×1.8×1	$58	encapsulated, PC mount
NMS Case B	10	1	5V to 28V @ 250 mA to 2000 mA	1	2	2.5×3.2×0.9	$69	encapsulated PC mount
NMD Case B	3	2	±15V @ 30 mA to 100 mA	1	2	2.5×3.2×0.9	$75	encapsulated, PC mount
Tamura 1150 Dominguez St, Carson, CA 90746 (213) 638-1790								**Circle 117**
OLS-XB series	15 to 28.8	1	5V to 24V @ 3A to 1.2A	5	—	4.9×4×2.1	$29.50	open frame
OLS-XC series	30 to 45	1	5V to 15V @ 6A to 3A	5	—	5.6×4.9×2.9	$45 to $49.50	open frame

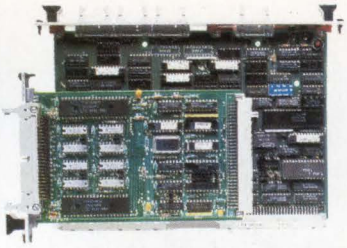
Model	Max power output (W)	No. of outputs	Output range	Output ripple (mV p-p)	Transient response (μs)	Dimensions (L×H×W in.)	Price	Comments
Tamura 1150 Dominguez St, Carson, CA 90746 (213) 638-1790								**Circle 117**
OLS-5NV	45	1	5V @ 9A	5	—	7×4.8×3.2	$67.50	open frame
OLD-5AAV	15	2	+5V to −5V @ 1.5A	5	—	6.5×4×2.1	$45	open frame
OLD-5BBV	30	2	+5V to −5V @ 3A	5	—	7×4.9×3.0	$58.50	open frame
OLD-12/15AA	24	2	+12V to ±15V @ 1A to 0.8A	5	—	6.5×4×2.1	$38.50	open frame
OLD-12B/15B	9.6 to 12	2	±12V to ±15V @ 0.4A	5	—	4.9×4×2.1	$33.50	open frame
OLD-24AA	28.8	2	+24V to −24V @ 0.6A	5	—	6.5×4×2.1	$38.50	open frame
OLD-512AA	17.5	2	+5V to +12V @ 2A to 0.5A	5	—	6.5×4×2.1	$45	open frame
OLT-522 AA	22	3	+5V to ±12V @ 2A to 0.4A	5	—	6.5×4×2.1	$49.50	open frame
Valor Electronics 6275 Nancy Ridge Dr, San Diego, CA 92121 (619) 458-1471								**Circle 118**
Series I Micro-reg	15	1,2,3	5V to 24V @ 2.2A to 0.5A	3	30	1.8×2.8×1.1 to 3.2×4×1.7	$31 to $55	open frame
OEM III	45	1,2,3	5V to 24V @ 9A to 2.1A	3	30	4×6.5×1.6 to 4×7.9×2.5	$44 to $83	open frame w/OVP all outputs
floppy disk	29	2	5V to 12V @ 3A to 1.8A	3	30	4×5×1.6 to 4×6.5×1.6	$62 to $72	open frame
μP supplies	29	2,3	5V to 15V @ 3A to 0.5A	3	30	4×6.5×1.6	$61 to $69	open frame



Processor Modules



Memory Modules

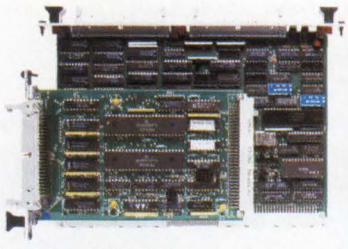


Peripheral Modules

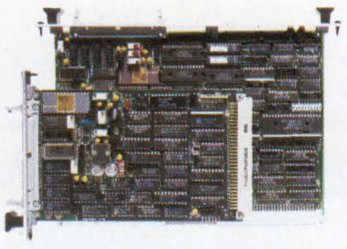
NEW!

XVME-683 VMEbus PC/AT Processor Module

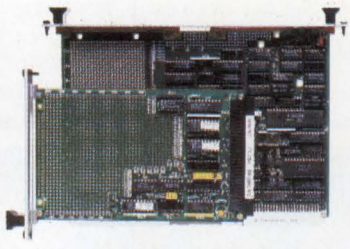
- Fully IBM PC/AT Compatible
- 20 or 25 MHz 80386 Processor
- 32 Kbytes of cache memory
- 1 or 4 Mbytes of dual-ported RAM
- 32 bit VMEbus Interface



Digital I/O Modules



Analog I/O Modules



Prototyping Modules

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Memory Products	BITBUS Controller	VME Terminal Products	PDOS*
Digital I/O	PAMUX Controller	Servo Controller Module	PSOS*
Analog I/O	1553 Interface Module		UNIX V/68K*
SCSI Controller	Thermocouple Input Module		SUN Workstations*
Winchester/Floppy Controller			VERSAdos*
			MTOS*

*Trademarks are acknowledged to: Microware Systems Corp. (OS-9); Eyring Research Institute, Inc. (PDOS); Motorola, Inc. (VERSAdos); V/68K Motorola, Inc. (UNIX); Software Components Corp. (PSOS); SUN Microsystems, Inc. (SUN Workstations); Industrial Programming, Inc. (MTOS).

CIRCLE NO. 54

MAJOR SYSTEM COMPONENTS

■ International market beckons

Like many arenas, the linear power-supply market has grown increasingly international over the past decade. Most linear supply manufacturers are attempting to meet that demand with product lines capable of accommodating electronic systems and instruments used around the world. To do that, manufacturers try to design products that will meet the most stringent requirements postulated by each of various regulatory agencies or organizations. For the most part, that implies meeting VDE (Verband Deutscher Electrotechniker) standards. "All the UL and the CSA worry about is whether there's a certain isolation voltage," says Heath. "VDE specifies the transformer construction technique and the distances between the layers of the windings of the primary and secondary."

Six years ago, Power-One introduced its International Series, the first linear supplies to meet virtually all international standards. Each unit meets the safety requirements of UL, CSA, IEC, VDE, BPO (British Post Office), ECMA (European Computer Manufacturers Association) and CEE (International Commission of Rules). They also provide worldwide ac input capabilities—100, 120, 220, 230 and 240 V ac from 47 to 63 Hz—letting customers stock a single supply regardless of destination.

"Analog circuitry can't tolerate the higher noise of the switching power supply."

—John Haines, Power-One

■ ■ ■

Since then, most major vendors have offered competitive product lines. The World Standard Series from Computer Products (Pompano Beach, FL), for example, offers input ac line voltages of 100, 115, 220, 230 and 240 V at 50 and 60 Hz. The supplies are UL-recognized and CSA-certified, and meet VDE and IEC safety standards. The power transformer is of VDE construction, with an enclosed split-bobbin and 3,750-V ac minimum isolation. The company also builds customized versions of the series with output voltages between 2 and 32 V dc and output power levels from 15 to 150 W.

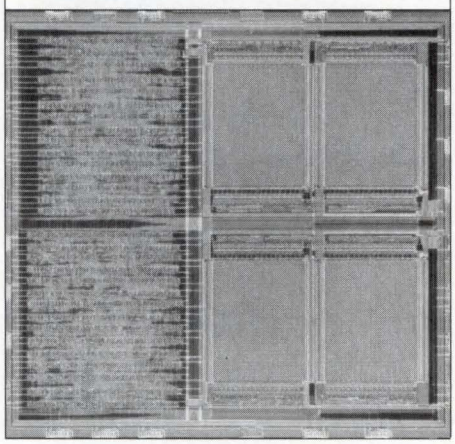
In a similar vein, Deltron's World Series line covers outputs from 15 to 240 W at 5 to 48 V. The single-, dual- and triple-output units boast an output ripple of only 5 mV p-p. Like its competitors, Deltron's linears meet virtually all safety specifications. □

INTEGRATED CIRCUITS

Bidirectional FIFO eases data exchange, enhancing system throughput

Designed to facilitate the exchange of data between devices with different transfer rates, the 67C4701 is a 512-word×8-bit bidirectional first-in, first-out (BIFIFO). The device provides an asynchronous full-duplex connection between two CPUs working in a multiprocessing mode, or between a CPU and a peripheral device.

Based on a dual-port RAM cell, the CMOS BIFIFO contains two 512-word×9-bit FIFOs (the ninth bit is reserved as a parity bit), which can be read and written to simultaneously. All necessary control and multiplexing logic circuits, plus a variety of features, are located on a single 28-pin chip. A byte-detect mode allows a comparison between the values of bytes being read and an 8-bit value preprogrammed into the internal register. When the specified value is read from the FIFO, the device generates an interrupt to tell the host that a byte detect has occurred.

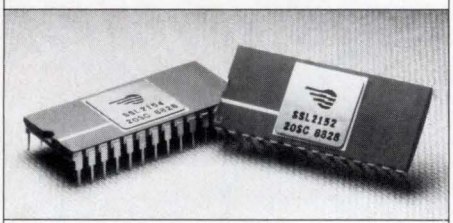


The device also generates framing bits as a means of identifying specific data or command blocks, eliminating the need to search the entire FIFO to locate desired information. Programmable almost full and almost empty flags let users tailor flag positions to the unique requirements of individual systems. Additional status flags indicate full and empty conditions. The 28-pin BIFIFO is priced at $42.50 each in 100-piece quantities.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94088
Circle number 120

Cache tag memories match output times of 17 ns

Fabricated with the manufacturer's proprietary BiCMOS technology, the SSL2152 and SSL2154 are 2k×9-bit cache address comparators with address compare to match output times as fast as 17 ns. Both devices have



TTL-compatible inputs/outputs, are cascadable in memory depth and word width, and feature a ninth bit to handle parity checking. To accommodate different system requirements, the SSL2152 has totem-pole "Match" output, while the SSL2154 has open-drain "Match" output for OR-tying with an external pull-up resistor. Both parts feature on-chip parity-generation and -checking capability, parity-error output, and forced-parity-error input. Prices for both devices start at $56.

Saratoga Semiconductor
10500 Ridgeview Ct
Cupertino, CA 95014
Circle number 121

Chip set pushes transfer rate to 40 Mbytes/s

A two-chip set for VMEbus boards, the AVICS (Advanced VMEbus Interface Chip Set) addresses the task of building high-performance multiprocessor systems for military and large civil/commercial applications. The chip set supports a sustained memory-to-memory data-transfer rate approaching the VMEbus specification of 40 Mbytes/s. The use of built-in RAM buffers for address and data information eliminates the need to handle data twice when passing messages from one intelligent card to another. A three-stage pipeline is used to maximize the transfer rate and minimize the VMEbus hold times, while a built-in direct memory access controller handles transfers from on-board RAM to the VMEbus.

DY-4 Systems
21 Credit Union Way
Nepean, Ontario K2H 9G1
Circle number 122

PLD features 22-ns propagation delay

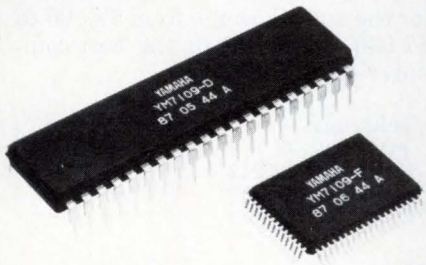
A high-speed programmable logic device, the PLHS473 offers a worst-case propagation delay of 22 ns. The device's 11 outputs can be configured to accept up to 24 product terms, while a verified lock fuse ensures design security after the device has been programmed. Because both the AND array and the OR array are programmable, common product terms (from the AND array) can be shared with any of the 11 output pins, letting a designer implement OR gate functions with up to 24 inputs. In 100-piece quantities, the plastic 24-pin dual in-line model is priced at $5.70, while the 28-pin plastic leaded chip carrier package costs $6.40.

Philips Components Div
PO Box 523, 5600 AM
Eindhoven, The Netherlands
Circle number 123

Signetics
811 E Arques Ave
Sunnyvale, CA
Circle number 124

Single-chip modem boasts 9,600-bit/s speed

A single-chip modem that operates at 9,600 bits/s, the YM7109 offers full compliance with telecommunications and industry standards. In addition to its modem capabilities, the chip is suited for Group 3 FAX in any personal computer, letting users send facsimile documents from PC to PC, from PC to facsimile machine, or from facsimile machine to PC. Built-in programmable double-tone generation is featured, as well as a scrambler and descrambler, programmable tone detection, a transmission filter, a programmable transmission level from 0 dBm to −15 dBm and a fixed-link equalizer. The device comes in either a 40-pin dual in-line package or a 64-pin quad flatpack, and runs on a 5-V, type D power supply. In quantities of 100, the modem chip is priced at $100.



Yamaha
6600 Orangethorpe Ave
Buena Park, CA 90620
Circle number 125

24-pin PLD lowers delay to 12 ns

A programmable logic device (PLD) with a worst-case propagation delay of 12 ns, the Plus173D is constructed with two arrays (AND and OR). The device supports programmable output polarity (active high or low) for each bidirectional I/O, making it suitable for applications ranging from simple cross-coupled latches to parity checkers and generators. Design, simulation and device programming support for the chip are provided by the manufacturer's Amaze PLD design software, which includes Boolean logic and direct state-equation entry, as well as functional and ac timing simulation models and an automatic test vector generator. In production quantities, the Plus173D is priced at $10.50.

Signetics
811 E Arques Ave
Sunnyvale, CA 94088
Circle number 126

DSP chip executes 400 million operations/s

Designed for applications where video signals are processed in real time, the IMS A110 digital signal processing chip can execute more than 400 million calculations/s on video data at speeds of up to 20 MHz. The chip's raw numeric processing power is derived from a parallel-processing architecture in which digitized data flows through a pipeline of 21 multiplier/accumulators. Besides the multiplier/accumulator array, the device incorporates three 1,120-stage shift registers of programmable length, each of which can hold a line of video data. The 8-bit-wide signal path is compatible to the grayscale output of most video systems. In sample quantities, the chip is priced at $500.

Inmos
1000 Aztec W
Almondsbury, Bristol, U.K.
Circle number 127

Coming October 15
Watch for Bill Harding's Special Report on LAN strategies for CAE/CAD.

DESIGN AND DEVELOPMENT TOOLS

68000 development and debug software targets VAX and Macintosh platforms

A complete integrated software development and debug package for the Motorola 68000 microprocessor family, Toolware runs on Digital Equipment Corp's VAX and Apple Computer's Macintosh series. Under the VMS operating system, designers can use the VAX series for the 68000/008/010/020 microprocessors. With the Macintosh II, SE and Plus, new designs can be developed for 68020-based systems under the Apple operating system.

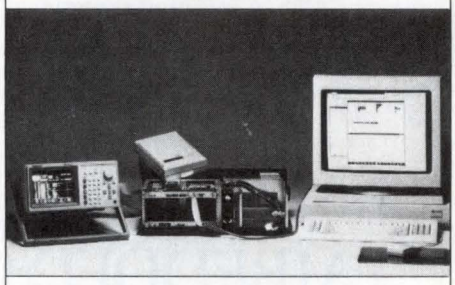
The development package lets VAX and Macintosh users interface with Motorola's HDS-300 development system, a platform that supports application development for 68000 microprocessors. A cross C compiler is included in the package, as well as an assembler/linker and source-level debugger with a special feature that allows for quick code compilation. This feature, called Make File, eliminates the need to specify parameters for each compilation, thus shortening program time.

Instead of working in assembly language, users of the source-level debugger can work in C language, which facilitates debugging. The package is priced at $11,200 for the VAX and $2,800 for the Macintosh. Individual components can be purchased separately.

Motorola Microprocessor Group
6501 William Cannon Dr W
Austin, TX 78735
Circle number 128

Development system applied to 68000 family

A logic-analysis-based development system for the Motorola 68000 microprocessor family, the TekDB Monitor integrates C source-level debuggers, a logic analyzer and an embedded debug monitor. The system provides three basic functions: download of object code into the target; program control; and a C source-level debugger. By combining these functions with the 1241 logic analyzer, real-time trace and hardware breakpoints are available. The package consists of an integrated C source-level debugger (TekDB) and debug monitor software that's burned into an EPROM and loaded into the user's prototype via an RS-232 port. Prices for the system range from $2,500 to $7,000, depending on the host computer's configuration.



Tektronix
PO Box 12132
Portland, OR 97212
Circle number 129

Engineering tools adopt Sun and Apollo platforms

An engineering tool for the specification and analysis of complex, real-time systems is available on the Sun-3 series and Apollo 3000 and 4000 series, as well as on DEC VAX systems. The Stalemate system also includes a prototyper package for rapid prototyping in Ada, a documentor for automatic documentation in Department of Defense 2167A or custom formats, and kernel/analyzer upgrades. Pricing for all of the system packages is uniform for Sun, Apollo and VAX workstations. The kernel is $10,000 per user; the analyzer is $25,000 per user; the prototyper is $25,000; and the documentor is $15,000. The software runs in standalone or networked mode.

i-Logix
22 Third Ave
Burlington, MA 01803
Circle number 130

PCB design tool enhances layout process

An enhancement to the Mentor Graphics Idea series of schematic capture and simulation tools, Protoview lets printed circuit board layout and manufacturing considerations be specified much earlier in the design process. By focusing on design flow from the logical/schematic level to the physical packaging stage, the

option lets the design engineer specify the placement of critical components and view printed circuit boards completed by CAD groups prior to delivery to manufacturing. The tool provides simultaneous two-sided placement; handles mixed technology such as surface-mount devices, through pin devices and mixed analog and digital components; and can view both the schematic and resulting layout graphically on a split screen. The option is priced at $14,900.

Mentor Graphics
8500 SW Creekside Pl
Beaverton, OR 97005
Circle number 131

ASIC verification system delivers 100-MHz clock rates

The Logic Master XL2 Verification System provides 896 individual pattern-generation and acquisition channels, or up to 448 bidirectional I/O channels, to verify application-specific ICs with over 600 pins. Featuring 100-MHz clock rates and up to 80-MHz data rates across all 896 channels, the system provides 48 timing edges, with 24 edges available to

each pin. Timing is assigned on a per-pin basis so that measurements can be made for each individual device pin. Accuracy of ±1.75 ns across all 896 channels is maintained by auto-calibrating each driver edge to match the threshold level of the corresponding device pin. Configurations begin at $470,000 for a 480-channel system.

Integrated Measurement Systems
9525 SW Gemini Dr
Beaverton, OR 97005
Circle number 132

CAD tool expands to IBM PC ATs

A high-end computer-aided drafting tool, the Plot 10 TekniCAD has been expanded for use with IBM PC ATs and compatibles. The TekniCAD/PC requires a system running MS-DOS 3.1 or higher, with a floating-point coprocessor, an Enhanced Graphics Adapter (EGA) display, a minimum of 2 Mbytes of extended memory and a hard disk (20 Mbytes minimum). A serial port and a mouse are also recommended.

The tool recognizes points, lines, arcs, arrows, dimensions and notes as separate items, letting the user specify constraints, limit searches and pinpoint a specific item in a crowded drawing. Any function can be performed on an entire body of items. Drawing data may be organized into several different levels, line styles and pen colors. Crosshatching functions include solid panel fill, line fill and fill with any user-generated pattern. Construction lines and grids can be created or removed to facilitate location selection. The price for the tool is $2,995.

CAD Associates
5840 W Interstate 20
Arlington, TX 76017
Circle number 133

Addendum

In our August 15 issue in the article "Unix performance merits extra design effort in SBC implementations" (p 54), we listed David L. Barker of Motorola's Microcomputer Division as the sole author. Two of Barker's colleagues—Paul S. Raynoha, system software architect, and Patricia A. Whitehurst, technical writer—also contributed to the article.

PRODUCT BRIEFS

Surge protector
The ITW Linx High-Speed Data Transmission Protector safeguards T1 multiplexers and other twisted-pair communication equipment against power surges that are caused by lightning and other transient voltages.
ITW Linx ***Circle 190***

VMEbus-to-Unibus link
The Model 600 VMEbus-to-Unibus link provides a bidirectional data path between a VME-based processor and a Unibus-based computer. $1,500.
Jorway ***Circle 191***

Bit-error-rate tester
The "Pocket Bert" handheld bit-error-rate tester, combined with a breakout box, is a battery-powered test set capable of testing synchronous data at rates up to 72 kbaud and asynchronous rates up to 38 kbaud. $550.
International Data Sciences ***Circle 192***

Desktop power systems
The VIP Executive Desktop Series 400 VA, 800 VA and 1250 VA uninterruptible power supplies are designed for PCs, small business computers, LANs and POS applications.
ITT Power Systems ***Circle 193***

TMS320 macro assembler
Designed for use with the Texas Instruments TMS32020 or TMS320C25 digital signal processing chips, the ASM-320 Macro Assembler generates Hex files that are suitable for uploading to the manufacturer's DSP-16 data-acquisition processor. $49.95.
Ariel ***Circle 194***

HP Laserjet to DEC interface
The Switchmate II intelligent printer switch makes Hewlett-Packard Laserjet printers compatible with DEC systems. $1,295.
Gold Key Electronics ***Circle 195***

Menu-driven CAD interface
Based on PC-like windowing technology, the MDI software provides functional groupings of menus and keywords, eliminating the need for memorizing command mnemonics.
Calma ***Circle 196***

Switching power supplies
The MDT-160 160-W, the MDT-220 220-W and the MAX-350 350-W switching power supplies are all designed in the same package size, allowing upgrades without system redesign.
Todd Products ***Circle 197***

PRODUCT INDEX

PRODUCT BRIEFS

Macintosh II color system
The Colorboard 108 and a 16-in. Trinitron monitor compose a color system for Macintosh IIs that matches Apple Computer's 72-dot/in. standard and displays images the same size as they appear in output form. $4,590.
Rasterops *Circle 198*

UPS remote signal package
The MM-Series uninterruptible power supply package is available on the manufacturer's 600-, 1,200- and 1,600-W models. An external remote signal port links the supply to the host computer's operating system via the remote operating cable.
Sutton Designs *Circle 199*

Enhanced LAN software
The Rabbitgate II product platform lets a user at a single DOS workstation on a LAN connect to SNA, X.25, BSC and DFT Coax mainframe sessions simultaneously from multiple windows with concurrent DOS and notepad.
Rabbit Software *Circle 200*

38.4-kbaud async modem
The Accelerator 2938 is an asynchronous dial modem that provides error-free file transfer rates up to 38.4 kbits/s and interactive mode rates up to 9,600 bits/s.
Telcor Systems *Circle 201*

OS/2 LAN manager
The company's OS/2 LAN Manager Arcnet driver incorporates a high session-level Protected Mode Netbios Protocol, which is at level five of the seven-layer OSI model, for higher throughput.
Standard Microsystems *Circle 202*

Display terminal
The ImageTerminal displays both text- and photograph-quality images that are stored on a computer data base.
Image Data *Circle 203*

12-bit, 2-MHz A-D converter
The ADC-00300 is a 12-bit, 2-MHz A-D converter and track/hold amplifier packaged in a single 40-pin TDIP hybrid.
ILC Data Device *Circle 204*

EPROM emulator with Mbit support
The E102 EPROM emulator is independently powered and can emulate EPROMs from 2,716- up to 27,512- and 271,024-Mbit support with optional 32- or 40-pin probe assemblies. $825.
Adams-Macdonald Enterprises *Circle 205*

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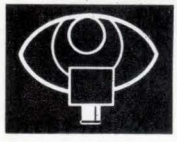
PERSONAL DEVELOPMENT

CONFERENCES

Oct 30-Nov 4
Ninth Int'l Conference on Computer Communication

Hilton Hotel, Tel Aviv, Israel. Sessions will cover local area, wide area, dedicated, special and personal networks; data transmission; and communications aspects of expert systems, office and factory automation, and the man-machine interface.
Information: J. Kella, ICCC, PO Box 50006, Tel Aviv, 61500 Israel, 03-654571. **Circle 180**

Oct 31-Nov 2
Autofact
McCormick Place, Chicago, IL. Dedicated to aiding technical managers and engineers, this conference will contain sessions on the multitude of technical topics involved in the automated, integrated factory, including AI and expert systems, CAE/CAD/CAM, CIM, MAP/TOP and other LANs, IGES, robotics, sensors, vision and simulation.
Information: Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48121, (313) 271-1500. **Circle 181**



Nov 6-11
Advances in Intelligent Robotic Systems

Hyatt Regency Cambridge, Cambridge, MA. Concurrent conferences will provide a forum for technology/scientific interaction among attendees on computer vision, expert industrial robots, sensor fusion, optics and image sensing, automated inspection and mobile robots.
Information: Society of Photo-Optical Instrumentation Engineers, PO Box 10, Bellingham, WA 98227, (206) 676-3290. **Circle 182**

Nov 8-10
GOMAC-88
Riviera Hotel, Las Vegas, NV. International Competitiveness—Its Impact on Government Electronics is the theme for this year's Government Microcircuit Applications Conference, which will address the impact on weapons systems and government electronics as a whole caused by the erosion of U.S. industrial leadership in semiconductors and related industries.
Information: Jay Morreale, Palisades Institute for Research Services, 201 Varick St, Room 1140, New York, NY 10014, (212) 620-3371. **Circle 183**

Nov 15-17
Neural Networks and Their Applications
Nanterre, France. This workshop will provide a focal point for discussing and evaluating the reemergence of neural networks and their industrial prospects, surveying international applications that are under development or already operational, and presenting commercially available products.
Information: EC2, Neuro-Nimes, 269, rue de la Garenne, 92000 Nanterre, France, (1) 47 80 66 29. **Circle 184**

Wescon/88®

Nov 15-17
Wescon
Anaheim Convention Center, Anaheim, CA. In conjunction with a 36-session applications- and user-oriented professional program that will cover application-specific ICs, systems and software, peripheral devices, and neural networks, this year's western electronics conference will stress automated design tools and engineering workstations.
Information: Garry Reeves, Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045, (213) 772-2965. **Circle 185**

SEMINARS

Oct 31-Nov 1, Dec 5-6
Making Software Engineering and CASE Happen
Chicago, IL and Washington, DC, respectively. This seminar will supplement a manager's base of experience in computer-aided software engineering with emphasis on qualitative and quantitative assessment, methods and tool selection, and methodology guidelines for installation and evaluation.
Information: Digital Consulting, 6 Windsor St, Andover, MA 01810, (508) 470-3880. **Circle 186**

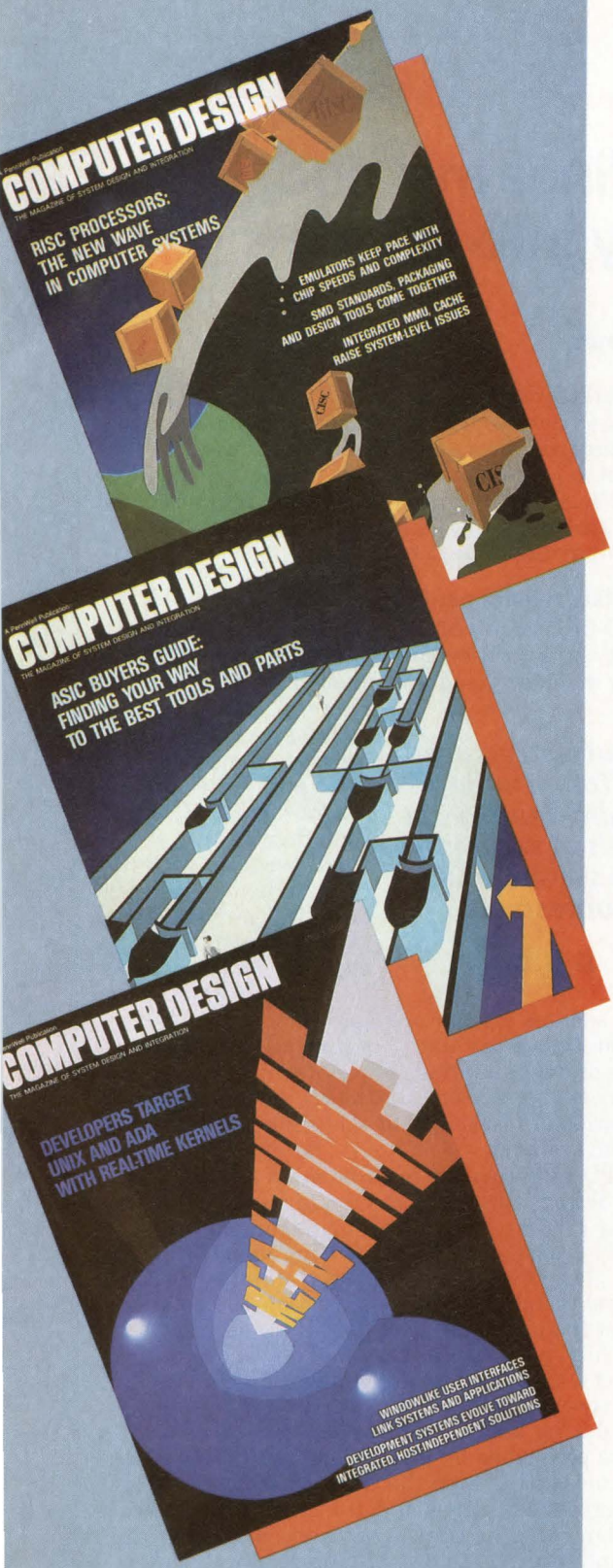
MICROPROCESSOR REPORT
THE NEWSLETTER OF MICROPROCESSOR-BASED DESIGN

Nov 3
Microprocessors '89
Red Lion Inn, San Jose, CA. Symposium featuring all of the latest major high-performance microprocessors will be on designing systems with those microprocessors. Representatives from each microprocessor vendor will participate.
Information: MicroDesign Resources, 550 California Ave, Suite 320, Palo Alto, CA 94306, (415) 494-2677. **Circle 187**

Nov-Jan
Image Processing and Machine Vision
Various locations. Seminar will provide an understanding of the fundamentals of image processing and machine vision, including techniques for implementation and integration in cost-effective applications.
Information: John Valenti, Integrated Computer Systems, 5800 Hannum Ave, Culver City, CA, 90231, (800) 421-8166. **Circle 188**

CASSETTE COURSES

Introduction to MC88100/MC88200 Instruction Set Computer
This self-paced, modular, audio cassette course (MTTA6) for designers with expertise in using 32-bit processors contains three tapes with approximately 4½ hours of material, fully illustrated notes, and related support literature. The course sets the foundation for the M88000 family of RISC microprocessors and covers the features of the MC88100/MC88200 RISC. Each module provides clearly stated objectives, comprehensive exercises and evaluations.
Information: Motorola, Literature Distribution Ctr, PO Box 209243, Phoenix, AZ, (602) 994-6561. **Circle 189**



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Military standard defines method of designing testability into systems

Art DeSena
President, ADS Associates

Plagued by a lack of adequate testability features designed into systems, subassemblies and line-replaceable printed circuit boards, the military has expended a tremendous amount of effort and funds designing and implementing specialized test systems to accommodate its depot and field repair sites. In earlier systems, controllability and observability of circuits were relatively easy to achieve. Manufacturers simply designed testability features into these systems to meet mean-time-to-repair (MTTR) requirements imposed by the military. But these testability features were usually incorporated at the system level, since the MTTR requirements typically applied to system-level operation; thus, very little attention was given to including testability features in subassemblies.

But over the past decade, military system designs have been using state-of-the-art technology. Without a structured plan for including testability features at all levels of assembly, these systems may be untestable in some instances and, at the very least, will incur horrendous test problems and high costs when test solutions are implemented.

Confronted with such a scenario, the Department of Defense (DOD) has taken great strides toward the inclusion of design-for-testability techniques. The VHSIC (Very High Speed IC), IDSS (Integrated Diagnostic Support System) and GIMADS (Generic Integrated Maintenance and Diagnostics) programs key heavily on design for testability, but they aren't all-inclusive from a system viewpoint. So the DOD issued MIL-STD-2165, "Testability Program for Electronic Systems and Equipment," in 1985, which defines a systematic method of ensuring that appropriate testability features are designed into its systems.

The intent of MIL-STD-2165 is similar to that of MIL-Q-9858, which required that suppliers to the military establish the separate Quality Control department that had total responsibility for ensuring that systems meet the required reliability and quality specifications. Although it took a few years for manufacturers to properly implement MIL-Q-9858, once it became the normal structure within a company, it was extremely successful. MIL-Q-9858 let the DOD deal exclusively with the Quality Control department in resolving quality and reliability problems.

Many companies that build systems for commercial applications have successfully used the guidelines set down in MIL-Q-9858. Similarly, the guidelines and intent of MIL-STD-2165 should be applied, where appropriate, by companies building commercial products. If these companies do so, they will benefit from the many years of coordinated efforts of the military joint services and their contractors in the electronics industry. Military suppliers, meanwhile, won't have any choice but to implement MIL-STD-2165, since it will probably become a common requirement imposed on all systems, such as MIL-Q-9858 is a requirement of all DOD equipment programs.

Testability requirements

MIL-STD-2165 requires that the contractor set up a testability organization that will be responsible for creating, managing and implementing a testability plan for the system to be produced. This organization must be defined and functioning in the very early stages of the program. For a small program with little complexity, such an organization may simply comprise one design engineer and one testability engineer. A large program such as a sonar or radar system, for example, might have a testability organization consisting of dozens or even hundreds of people, most of whom are engineers responsible for the review and implementation of testability at all levels of assembly within the system.

Without a structured plan for including testability features at all levels of assembly, these systems may be untestable.

MIL-STD-2165 consists of three main sections. Section 100 defines the program monitoring and control tasks that relate to the overall management of the testability program, including setting up a testability program plan, testability reviews, testability data collection and testability analysis. Section 200 defines tasks that include detailed testability requirement trade-off analyses, preliminary and detail design goals, and testability and assessment efforts. And Section 300 covers the test and evaluation of testability features during maintainability demonstrations, which are performed by introducing faults into a system and measuring both the time it takes for the system's diagnostic routines or self-test features to locate the problem, and the time it takes to then repair the system and return it to its normal operating status. Maintainability demonstrations are conducted to verify that the system can meet the MTTR requirements.

MIL-STD-2165 also has two appendices. Appendix A provides guidance for implementing and tailoring a testability program and contains information regarding the purpose, selection and timing of testability requirements. Appendix B provides a methodology for evaluating the testability of a design in the early stages of system conception and development and de-

fines general design-for-testability rules that are applicable to a broad cross-section of systems.

A success story

Properly evaluating the effectiveness of MIL-STD-2165 will take many years, since new system designs can take that long from inception to completion. One company, however, has already witnessed the standard's effectiveness. Subcontractor Resdel Engineering (Arcadia, CA), with help from ATE Solutions (Westlake Village, CA), a consulting company, successfully implemented MIL-STD-2165 in a sonobuoy receiver system for the military.

The stringent requirements for the sonobuoy receiver design included that redundancy be designed into the system to ensure that no single-point failure would prevent the system from performing to specifications, as well as sufficient built-in-test (BIT) and built-in-test-equipment (BITE) to detect 98 percent of all failures in the system. The BIT/BITE capability replaced the typical system test and had to be structured so it could run in a continuous background mode. False alarms from the BIT/BITE had to be kept to less than 1 percent.

Since there was no system test, BIT/BITE had to be able to isolate a failure to a single shop-replaceable assembly (SRA) in 90 percent of the cases, to one of two SRAs in 95 percent of the cases and to one of three SRAs in 98 percent of the cases.

In a report presented at the recent ATE and Instrumentation Conference, Louis Unger, president of ATE Solutions, and Michael Englehart, project manager of the P-3 Update IV Sonobuoy Receiver at Resdel Engineering, described the steps taken to successfully implement MIL-STD-2165.

The first step was to set up a testability program plan that identified and integrated testability management tasks needed to accomplish the program requirements. The testability program plan documented the tasks to be accomplished, the schedules by which those tasks were to be accomplished and the manner in which the results of the tasks were to be used. The plan was laid out very early in the development cycle—and was enforceable. Resdel Engineering included the testability plan as part of the system engineering plan and coordinated it closely with the maintainability program plan.

The next step was to set up a testability organization, and Resdel created a department called Testability Engineering, which reported to the manager of the Product Support Group. The Product Support Group integrates the disciplines of logistics support, configuration management, reliability, maintainability and testability engineering. In addition to the product-support disciplines, Testability Engineering interfaces directly with System Engineering, Design Engineering and Test Engineering. "Testability Engineering plays the role of system integrator in examining requirements and providing trade-offs for the other disciplines to apply in creating testable dsigns," Unger and Englehart reported.

To fully integrate system testability requirements into development activities, channels of communication must be established between the project organization and its outside subcontractors. Resdel not only established these channels of communication, but also provided a means for testability engineers to work with designers "on-line," to define, implement and decide on the most effective trade-offs for the testability circuits that they would include in all levels of design. By doing so, the problems encountered and solutions needed were tackled in the early design stage, when they could solve them easily, and a proper balance was reached between performance, cost and supportability of system assemblies. The open lines of communication allowed testability engineers to become members of the design team rather than just being post-design critics.

Resdel also developed tutorial materials on testability requirements and techniques, which were issued to the development team. Supplementing these documents was a series of miniseminars on testability and the requirements of MIL-STD-2165 as they applied specifically to the sonobuoy program and its governing equipment specification.

Testability given full support

Communication and education are important if testability is to be effectively implemented in a complete program, such as Resdel's sonobuoy program. But if certain testability requirements bring about an undesirable solution, such as a larger printed wiring board, a trade-off must be made. However, the designer and the testability engineer probably won't agree on the same solution; so a compromise must be reached. The most important element in reaching a compromise is a respect for each other's perspective. Traditionally, this is a stumbling block because design engineers don't understand testing and test engineers seldom communicate their needs to designers. Often, when designs are disapproved for lack of testability, the designer doesn't know why it lacks testability or how to avoid the problem in the future.

"Designers quickly realized that no matter how much they objected, testability was here to stay."

—Louis Unger, ATE Solutions, and Michael Englehart, Resdel Engineering

Resdel resolved this problem by bringing testability in-house and using ATE Solutions as consultants. The consultants brought with them the respectability necessary to be able to tell designers how to design.

"Resdel management respected testability and gave it its undivided support, and designers quickly realized that no matter how much they objected, testability was here to stay. The moans and groans gave way to real solutions," Unger and Englehart reported.

The DOD will soon release a testability analysis handbook, which is intended as a vehicle for implementing the structured design-for-testability methods defined in MIL-STD-2165. The testability handbook will assist research, development and acquisition managers and system contractors in achieving testability requirements and in predicting and assessing the test effectiveness of the system design. The handbook will also contain data sources and tools to assist design engineers. □

Military lowers its computer requirements

Sydney F. Shapiro
Senior Editor
Research/Special Projects

Across-the-board reductions in Department of Defense budgets over the past two years—item-by-item paring that probably will continue for the next several years—make discussions about the potential dollar value of the DOD electronics market impractical. Because belt tightening in all areas of this market will lower actual dollar values, discussions in terms of proportions of dollars spent are more reasonable.

Actually, electronics portions of the DOD budget, particularly those involving computers, aren't likely to be cut as drastically as other areas, such as weapon systems. Even so, the Electronics Industry Association has predicted that DOD spending on electronics will be 4 percent less this fiscal year than last year and will be even less in 1989. Therefore, to meet its increasing demand for computers, the DOD is being forced to lower some of its environmental requirements and purchase less rugged and less expensive computers for applications that don't require fully militarized machines.

DOD computer classifications

The DOD classifies its computer and peripherals requirements as militarized, ruggedized and commercial. Militarized computers are full-mil-spec devices qualified for operation in harsh or combat conditions. In such conditions, computer failure could result in harm or even death to personnel and possible loss of critical battlefield actions. Often these computers are based on a commercial architecture, such as that of Digital Equipment Corp's PDP-11 or Data General's Eclipse, on the premise that software won't have to be developed again. But the hardware in these militarized versions is completely redesigned to meet military specifications in all areas.

Redesigning a commercial computer for the battlefield environment is difficult, expensive and timeconsuming. Very often the redesign period is so lengthy that a full-mil-spec computer will fall several years behind its commercial counterpart in technology. And then the designers may discover that the original commercial software intended to be used has been so modified through several updates that it's no longer compatible with the militarized computer. In addition, militarized computers frequently are embedded in systems and therefore can't be used for other purposes.

Ruggedized computers, on the other hand, are basically the same as commercial computers. But they've been modified and often repackaged as protection against the environmental parameters of noncombat-related military applications. Some components in ruggedized computers are replaced with "hardened" equivalents that can withstand wider ranges of temperature, shock and relative humidity than can those in commercial equipment. And temperature control and larger power supplies may be included. Usually, these computers are used for such operations as rear-echelon command and control, analysis of intelligence, and communications.

Although more expensive than commercial computers, the ruggedized versions are far less costly than their militarized counterparts. This becomes increasingly important when purchasing authorities try to fill larger quantity requirements with fewer dollars.

Commercial computers—the same computers sold by most retail distributors—meanwhile, are purchased in large quantities by DOD agencies for routine applications. These computers are used in military offices as well as in all other normal operating environments.

Ruggedized computers okayed

Despite the rivalry between the U.S. Army and the Marine Corps, their operations and equipment requirements are quite similar. Market research firm Frost & Sullivan (New York, NY) indicates that both services buy three types of computers: transportable, portable and handheld. All hardware and software are nondevelopment items (NDIs)—items that have full environmental capabilities for their class but are stock items that have been modified.

Actually, some of the NDI computers purchased by military agencies in the past several years do meet military specifications. To save the cost of testing and documentation, several major suppliers of such NDI products have marketed them to the military specifications. They work just as well, with or without pedigree papers.

The Army has now determined that corps and division echelons don't need militarized computers.

■ ■ ■

Transportable computers, classified as computers capable of being lifted by two persons, are stand-alone, 32-bit CPUs with up to 8 Mbytes of RAM, a built-in display, both floppy and hard disks, and a keyboard. Fifty percent are militarized, 36 percent are ruggedized, and 14 percent are commercial.

Portable computers use the same 32-bit architecture as the transportable versions, include up to 2 Mbytes of RAM and display monochromatic images on built-in displays. Optional external displays provide color graphics. Of this processor group, 71 percent are militarized, 24 percent are ruggedized and only 5 percent are commercial.

Handheld computers weigh less than 10 lb each and

include a keyboard, a small graphics display, 256 kbytes of RAM and two communications channels. They're based on either 16- or 32-bit architectures. All of these computers are militarized because of the conditions under which they must operate.

Frost & Sullivan's findings illustrate the shift from expensive militarized computers to the ruggedized counterparts in the Army's attempt to automate tactical command and control operations, operations that have been going on for over 25 years. This program, which will provide automated battlefield information at corps, division, brigade and battalion echelons, originally was to be supported by militarized computer equipment at every level.

But the Army has now determined that corps and division echelons don't need militarized computers and has changed its purchase plan to include a large number of ruggedized computers as well as NDI commercial computers that have been repackaged to meet ruggedized requirements. An estimated cost reduction of over $76 million will result from this one change in procurement requirements. The Army will gain further cost reductions by delaying meeting its battalion-level needs, about 54 percent of the total program, until at least 1990, when the equipment will become available through another procurement plan.

Future even brighter

Today's capacity to ruggedize a commercial computer results in part from the manufacturing techniques and process technology that weren't available even a few years ago. Computers can now be protected more easily from harsh operating environments. And—by means of VLSI circuitry, smaller components and improved materials—commercial electronics as a whole and, thus, commercial computers have become more rugged and reliable.

Further improvements in the reliability of commercial electronics and in the relative ease with which commercial computers can be ruggedized, plus the need to meet increases in required quantities with fewer dollars, will expand the use of such ruggedized computers in future years. And, at the same time, increased functional requirements for equipment will necessitate improved sophistication of the computers purchased.

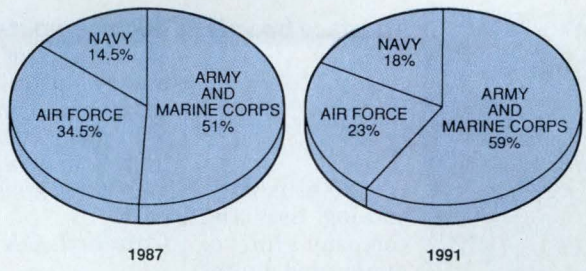
Some of the likely capabilities that will be added to ruggedized computers in the next few years will include large flat-panel color displays, high-speed three-dimensional pictorial graphics, helmet-coupled displays and improved bus architecture. But foremost among the necessary improved sophistication will be embedded expert systems and speech recognition and synthesis. Advances in commercial developments in these latter areas will unquestionably be built into ruggedized computers for military applications.

Frost & Sullivan predicts that the 1987 DOD market for ruggedized computers was almost 15 percent greater than that of 1986 and forecasts that the fiscal year 1991 market will be more than 47 percent over 1987's market. That amounts to an increase of about 69 percent over 1986's market.

The largest military service user of ruggedized computers is the Army/Marine Corps combination, followed by the Air Force. These two groups also spend the most for development of non-mil-spec computers. Development forecasts in this area for the Army/Marine Corps will increase by 24.5 percent in the 1987 to 1991 period. The Air Force will increase expenditures by nearly 13 percent in the same period. Other DOD agencies are expected to increase their research and development expenditures by over 46 percent.

Actual purchases of rugggedized computers will also increase, but in different proportions. The Army/Marine Corps combination is expected to increase its ruggedized computer purchases by nearly 91 percent from 1987 to 1991, while the Air Force will increase its purchases by only slightly more than 8 percent. In the same period, the Navy will double its purchases of similar computers. □

MARKETS FOR RUGGEDIZED COMPUTERS



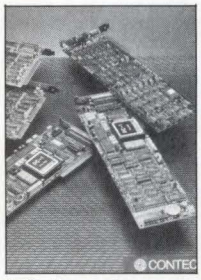
Although there will be only an 8 percent increase in overall military services expenditures for ruggedized computer production equipment and systems, the Army and Marine Corps in 1991 will spend a total of $1.7 billion, nearly double its $886 million expenditures in 1987. The Air Force, on the other hand, will increase its expenditures in this area from $602 million in 1987 to $652 million in 1991, but the overall percentages will drop from 34.5 percent in 1987 to 23 percent in 1991. One reason for this shift may be a greater need for full-mil-spec computers by the Air Force.

For more information . . .

Market data referenced in this column was based upon information from the following source:

The Military Ruggedized Computer Market in the U.S., $1,950. Frost & Sullivan, 106 Fulton St, New York, NY 10038.

LITERATURE



Interface boards

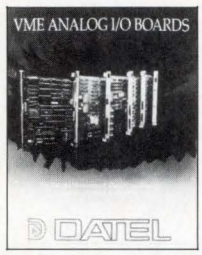
A 100-plus-page catalog lists the company's lines of analog and digital I/O boards, communications interfaces, counter/timers, memory and disk cards, motion-control interfaces, signal monitoring and control boards, accessories and software.
Contec Microelectronics
Santa Clara, CA **Circle 134**

PC instrumentation

The updated, 144-page summer edition of *The PC Systems Handbook for Scientists and Engineers* includes over 1,000 products for turning 8088-, 80286- and 80386-based PCs into data acquisition and control systems; products have been organized by compatibility.
CyberResearch
New Haven, CT **Circle 135**

HP-UX software

This catalog covers 400 technical and commercial proprietary-software solutions running on the HP-UX operating system, which adheres to AT&T's Unix System V Interface Definition Issue 2. It also contains 200 pages of software for HP 9000 workstations and servers.
Hewlett-Packard
Cupertino, CA **Circle 138**



VME analog I/O boards

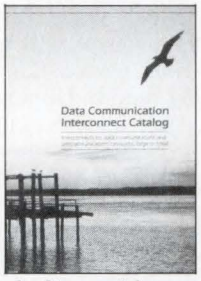
A six-page brochure covers the company's lines of high-performance analog input/output boards for VMEbus, including 12-, 14- and 16-bit analog-to-digital and digital-to-analog boards. Full technical specs and configuration and interface diagrams are included.
Datel
Mansfield, MA **Circle 136**

Microcomputer boards

This catalog of Multibus I and VMEbus products includes single-board computers, communications processors, memory boards, interface modules, firmware, software, enclosures and integrated system packages.
SBE
Concord, CA **Circle 139**

MIL-STD-1553 multiplexer

This information booklet contains 30 pages of explanation on BUS-61553, a stand-alone, dual-redundant MIL-STD-1553 integrated multiplexer hybrid interface that contains a dual transceiver, a bus controller, a remote terminal unit and bus protocol, and static RAM.
ILC Data Device
Bohemia, NY **Circle 140**



Data communications

This 20-page catalog describes a diversified line of interconnects, including cables, switch boxes, fiberoptic data links and accessories for large and small data communications networks.
Harbor Electronics
Ridgefield, CT **Circle 137**

Networking solutions

A six-page brochure describes the Passport ISDN terminal adapter, INM integrated network manager and LAN Span remote LAN bridge for global networking solutions.
Infotron Systems
Cherry Hill, NJ **Circle 141**

MIL-STD-1553B components

A range of interface transformers, data bus couplers and data bus terminators meeting the full spectrum of MIL-STD-1553B requirements are described in catalog 2001-A, with specs, schematics and package configurations included.
Technitrol
Philadelphia, PA **Circle 144**

Data acquisition

A 256-page color handbook includes data on the company's complete line of data acquisition, industrial control and monitoring, signal conditioning, and communications products for the IBM PC, PC XT, PC AT and Personal System/2, Apple Macintosh II, and VMEbus computers.
Metrabyte
Taunton, MA **Circle 143**

Data converters

This 384-page catalog features data sheets on 29 analog-to-digital converters, 20 digital-to-analog converters and 13 voltage references, with details on product features, electrical characteristics and applications.
Maxim Integrated Products
Sunnyvale, CA **Circle 142**

Power supplies

This brochure describes switched-mode power supplies and dc-dc converters, from 1 to 600 W and with up to six outputs; many models are UL/CSA/TUV- or VDE-approved and meet I/O leakage current requirements.
Total Power International
Lowell, MA **Circle 145**

Logic analyzer

This brochure describes ML4400, a 400-MHz logic analyzer that includes user-selectable input cards for the simultaneous analysis of up to four individual 8-, 16-, and 32-bit microprocessors.
Arium
Fountain Valley, CA **Circle 146**

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THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

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LAST BITS LAST BITS LAST BITS LAST BITS LAST BIT

Joint venture targets military smart power

Teledyne Semiconductor (Mountain View, CA) and Omnirel (Leominster, MA) have entered an agreement to jointly develop and market CMOS smart-power devices for the military. Under the agreement, both companies will develop products incorporating Omnirel's proprietary high-density military power packages and discrete power MOSFETs with Teledyne's CMOS ICs, MOSFET drivers and switch-mode power-supply controllers. The initial product will combine CMOS logic and power MOSFETs in a single package for switching power-supply and motor-control applications.

Partnership ports ASIC tools to workstations

An agreement between Micro Linear (San Jose, CA) and Viewlogic Systems (Marlboro, MA) will let the companies offer Micro Linear's analog application-specific IC design library as an integrated part of the Viewlogic workstation system. The library, which consists of symbols, subcircuits, component models and worst-case design-verification utilities, will be ported to the Workview stations for use on IBM PCs and DEC VAX systems.

Superworkstation developers choose Sparc

The increasingly popular Scalable Processor Architecture (Sparc) reduced-instruction-set computer engine will soon show up in superworkstations from a couple of vendors. Metaflow Technologies (Vancouver, BC, Canada) has licensed the processor from Sun Microsystems (Mountain View, CA), and will manufacture it in an advanced ECL process as the foundation for its own future supercomputing-class systems. Metaflow's Sparc-based systems, performing in the range of 100 Mips and 100 MFlops, will debut in the second quarter of 1989.

Solbourne Computer (Longmont, CO) will also license the Sparc and will design a 64-bit ultra-LSI implementation of the processor for its planned superworkstation. The Solbourne implementation will integrate a floating-point processor, memory-management unit and cache memory with the Sparc CPU on a single chip.

Pact signed to produce EPLDs

A seven-year technology exchange and supply arrangement between Altera (Santa Clara, CA) and Texas Instruments (Dallas, TX) targets high-density erasable programmable logic devices. Under the terms of the agreement, Altera will provide architecture, circuit design and software technology, while TI will supply worldwide manufacturing capabilities and its high-voltage, enhanced-performance, implanted CMOS process.

Genrad endorses VXIbus standard

A major test systems vendor is joining the VXIbus consortium. Genrad (Concord, MA), an active member of the IEEE-P1155 working group, has officially announced its support for the VXIbus standard by joining the consortium. An enhanced version of the VMEbus, VXI is specifically tailored for instrument applications. The bus will ensure compatibility between modular instrumentation products and let them interact on the same chassis.

Allegro CL selected for MIPS RISC processor

Franz (Berkeley, CA) has signed a contract with Synthesis Software Solutions (Sunnyvale, CA) to port its Allegro Common Lisp to the reduced-instruction-set computer from MIPS Computer Systems (Sunnyvale, CA). Common Lisp is a Lisp dialect combining features necessary for symbolic processing with features for traditional computing. All MIPS RISC-based computer manufacturers will have the opportunity to offer Allegro CL on their products on either an OEM basis or as a software product sold and supported by Franz.

IC vendors to share DSP, controller technologies

A five-year agreement between Harris Semiconductor (Melbourne, FL) and Zoran (Santa Clara, CA) will help each vendor develop digital signal processing and real-time control products. Under the agreement, Zoran will second source Harris' RTX 2000 16-bit microcontroller, while Harris will second source Zoran's digital signal and vector signal processors. Harris will also function as a foundry resource for Zoran in support of its commercial and military-qualified products. In return, Zoran will gain CAD technology and equipment for future joint product-design activities.

EDA vendor to use new Apollo workstations

Look for the Idea series of electronic design automation systems from Mentor Graphics (Beaverton, OR) to soon include the Series 3500 and 4500 personal workstations from Apollo Computer (Chelmsford, MA). The two platforms will deliver performance enhancements over previous Mentor Graphics systems built around the older Apollo 4000 series. The 7-Mips 4500 and the 4-Mips 3500 use Motorola's 68030 processor and are available with enhanced color graphics capabilities.

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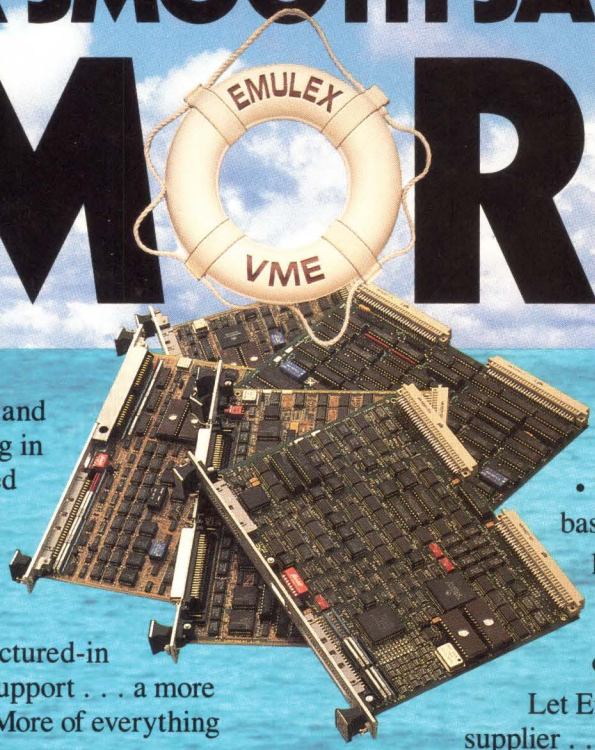

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