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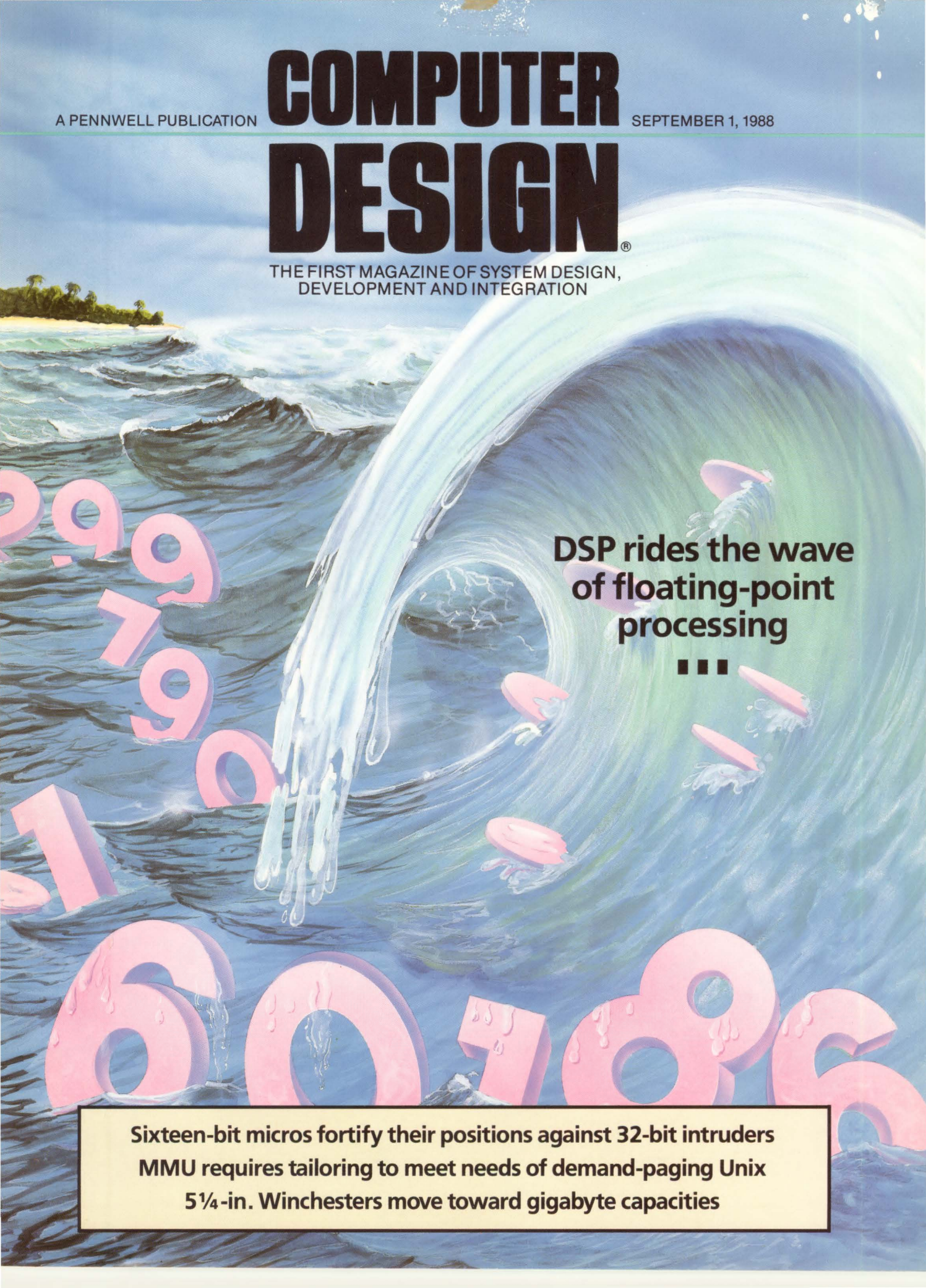
COMPUTER DESIGN®

SEPTEMBER 1, 1988

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION



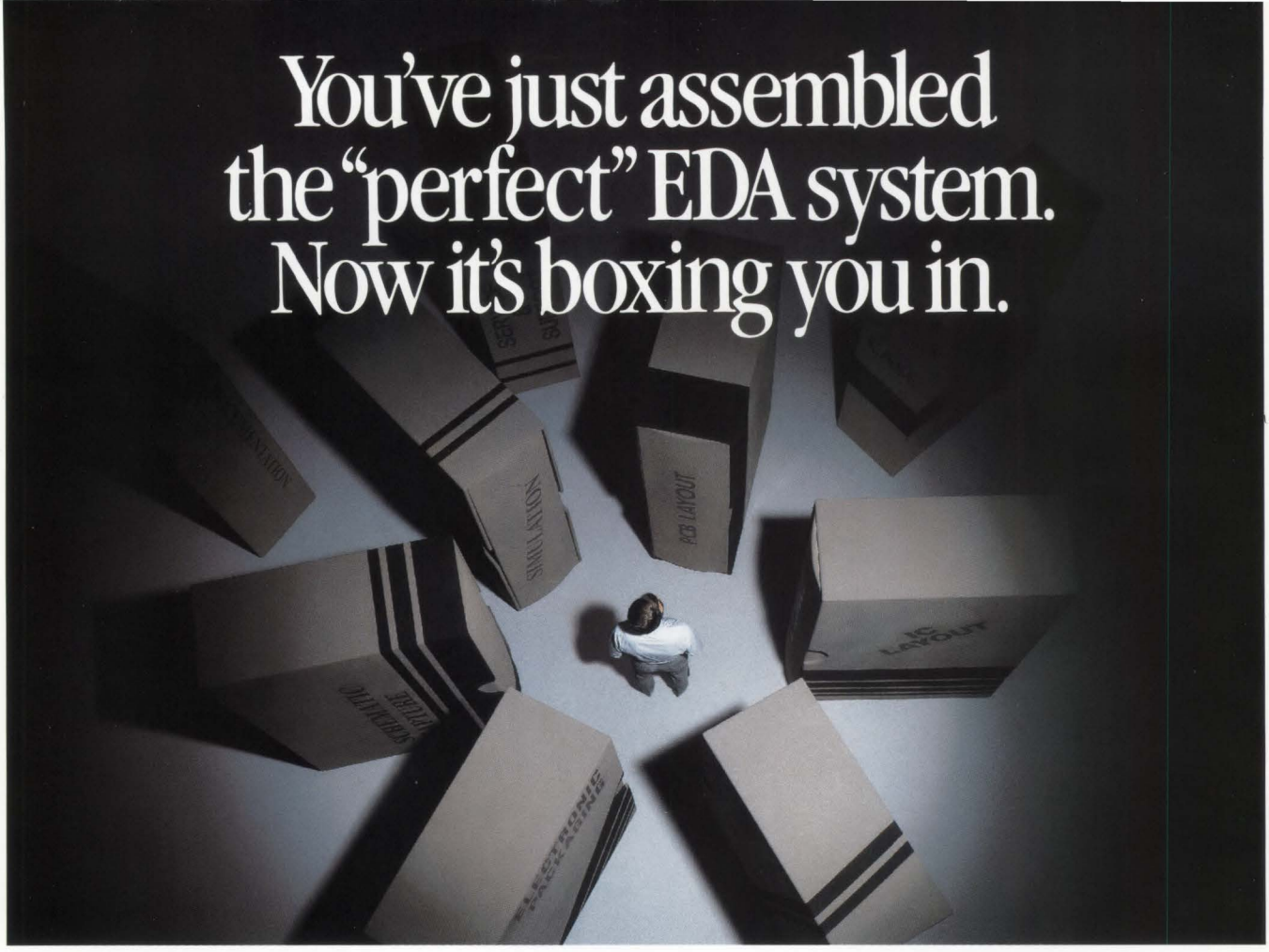
DSP rides the wave of floating-point processing

Sixteen-bit micros fortify their positions against 32-bit intruders

MMU requires tailoring to meet needs of demand-paging Unix

5¼-in. Winchesters move toward gigabyte capacities

You've just assembled the "perfect" EDA system. Now it's boxing you in.



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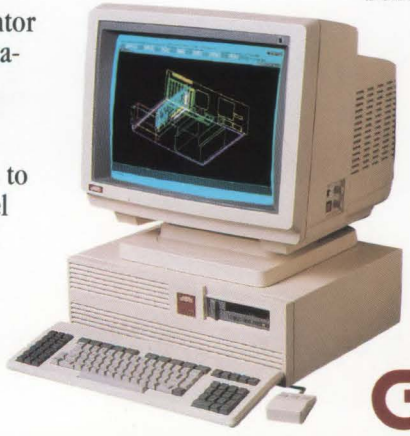

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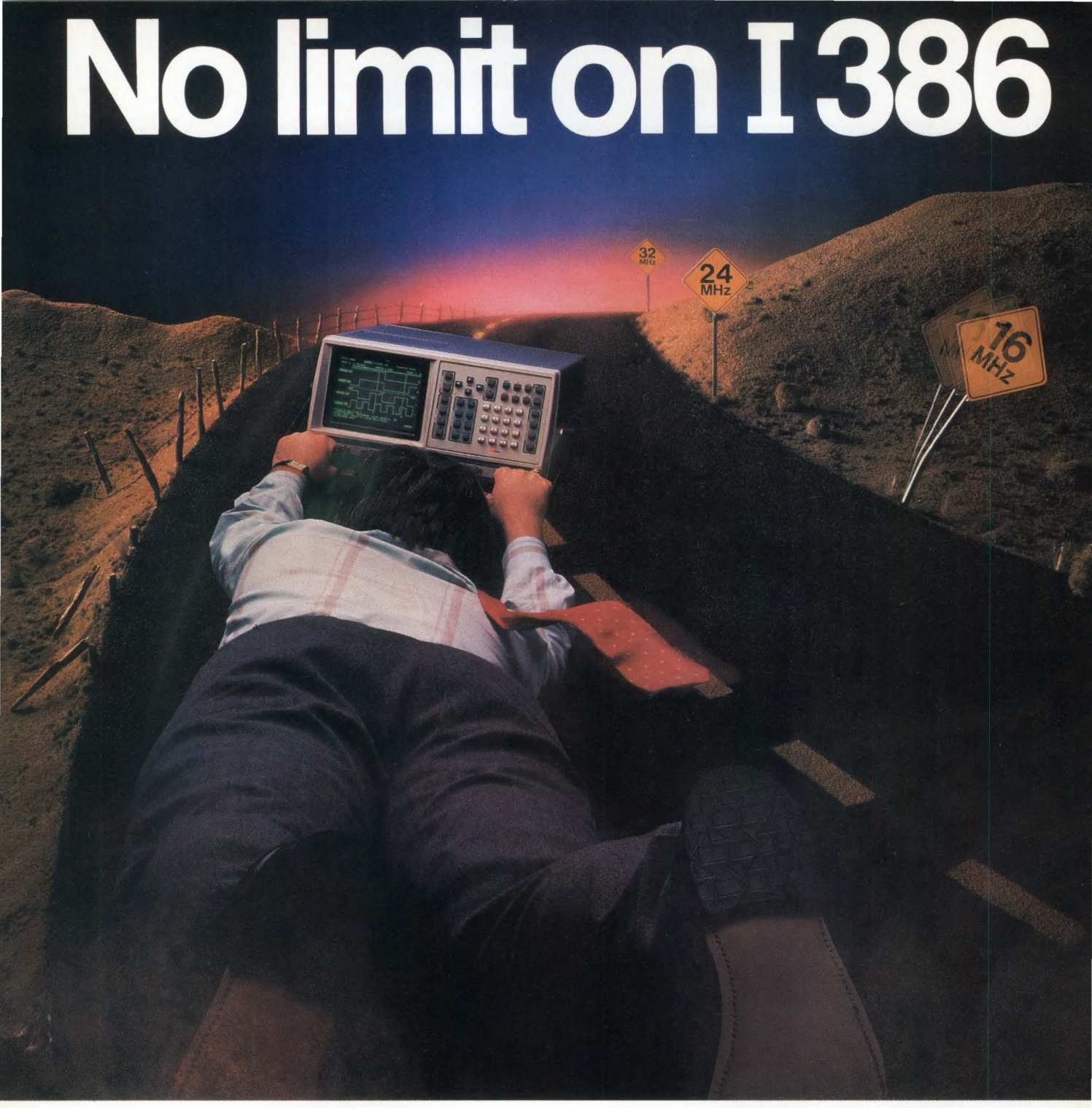

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Vol. 27, No. 16

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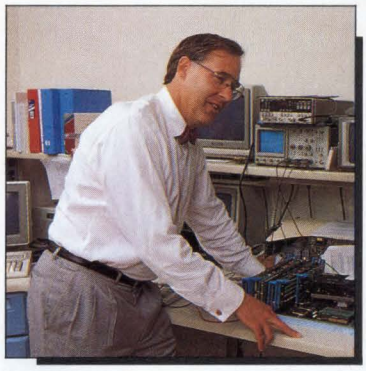

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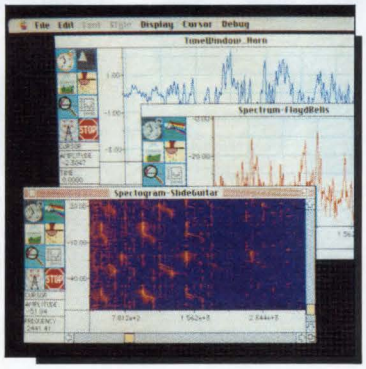
Buscon/East coming to New York October 3 to 6

To help you plan your visit, we've included a show preview and guide with this issue of Computer Design. There's a lot happening that you shouldn't miss.



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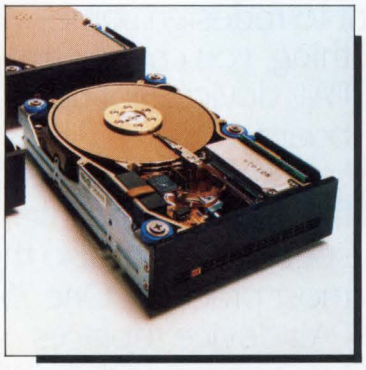

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How the fa

Our new 7.5ns PAL® device is fast enough to prove that standard logic shouldn't set the standard anymore.

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Combinatorial				
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74151 Mux	tPD	11.0	15.0	7.5
Register/Latch				
74374 Octal Register	tCO	10.0	9.0	6.5
74373 Octal Latch	tPD	8.0	6.0	7.5
	tLEO	13.0	11.5	7.5
Counters				
74161 Four bit Ctr	tS	5.5	8.0	7.0
	tCO	11.0	13.5	6.5
74269/869 Eight bit Ctr	tS	2.5	5.0	7.0
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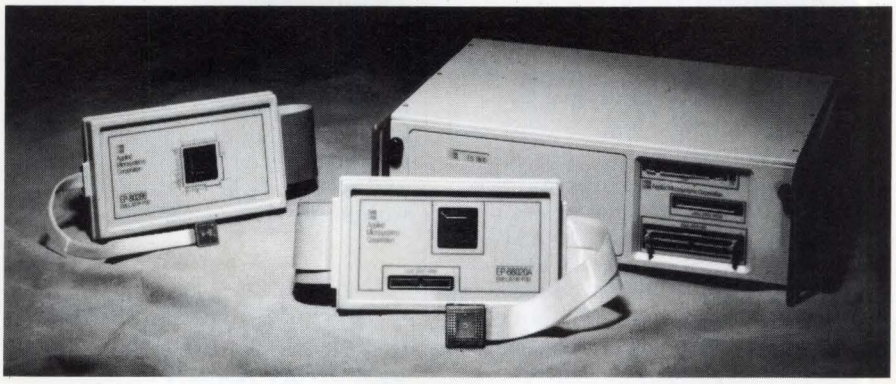

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MicroVAX	ULTRIX	8048 family, 8051 family	**Pascal**	Assemblers	(16 & 32-bit)	and other soft-
Apollo	UNIX®	8080, 8085, 8086/8,	**FORTRAN**	Linkers	**EC 7000**	ware products
Sun	MS-DOS	80186/188 and 80286	**PL/M**	Locators	(8-bit	for source
PC		**Motorola:**	**Assembler**		microcontrollers)	and symbolic
PC XT		68HC11, 6800/2/8,	**Jovial**		**EM Series and**	debugging
PC AT		6809/9E, 68000/08/10	**ADA (VERDIX)**		**EL 800**	
PC Compatibles		and 68020			(8-bit	
		Zilog:			microprocessors)	
		Z80, Z80H, MK 3880/4				
		and Z8001/2				
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CIRCLE NO. 3

Shrink in logic brings embedded DOS to portable systems

All the core logic contained on the 48-in.² PC XT mother board has been reduced to an 8-in.² circuit card on the Wildcard 88 from Intel (Santa Clara, CA). The card contains a socket for ROM BIOS supplied by Phoenix Software (Norwood, MA) and Award Software (Los Gatos, CA), a CMOS 80C800 processor, and an application-specific IC that combines a counter/timer, dynamic RAM refresh and peripheral control. The latter two chips are bonded directly to the circuit board and covered with epoxy. All memory, I/O, power and control lines are brought to a 68-pin edge connector that fits into a high-density, single in-line module (SIM) connector.

The card, which will sell for $50 in OEM quantities, will let designers add embedded DOS functionality, programmability and user interface capabilities to real-time control, instrumentation and consumer products. It isn't intended as a real-time controller in its own right. Intel hasn't included on-card system RAM, although there's space on the back side of the board for SIM memory modules. The company is also offering a prototyping board that has extra SIM slots and regular XT card slots. —*Tom Williams*

Logic synthesis moves to engineer's desktop

Logic synthesis is the hot new buzzword for application-specific IC design, but to be useful it must be available and affordable. By introducing the Ascyn-View Logic Synthesizer last month, Viewlogic (Marlboro, MA) and Algorithmic Systems (Braintree, MA) have brought behavioral logic synthesis to the desktop faster than almost anyone imagined.

Algorithmic Systems' Ascyn product can automatically synthesize a gate-level net list from an algorithmic description in a Lisp-based input language. The net list is then mapped into an ASIC cell library. Ascyn-View is integrated with Viewlogic's schematic entry and simulation tools, letting designers mix Ascyn-designed cells with cells designed using more traditional methods. Although logic synthesis is usually thought of as a high-end tool, Ascyn-View costs just $10,000 and runs on IBM PCs and VAX workstations. —*Richard Goering*

Zendex and BIRD alliance develops Multibus I 286 PC AT board

Zendex (Dublin, CA) and the BIRD (Bi-National Industrial Research and Development) Foundation have concluded funding agreements for the development of a Multibus I 286 PC AT board. The BIRD foundation is chartered to assist with joint ventures between U.S. and Israeli high-technology companies. Programs for the industrial environment will be developed on the 12-MHz single-board computer and downloaded to a Multibus I industrial control system via floppy disk. The search for beta sites began in August, with production models available by the end of the year. Founded in 1977, BIRD's funding derives from the interest on an original endowment provided equally by the U.S. and Israeli governments. —*Michael Donlin*

Clearinghouse plans to simplify military software development

The Defense Advanced Research Projects Agency (DARPA) has awarded three five-year contracts aimed at finding better ways of developing military software. The contracts are part of a DARPA plan to develop a public domain defense software repository. The repository will let developers of weapons systems software easily determine whether the software they need already exists, according to Jackson R. Ferguson, director of command, control, communications and intelligence technology at the Air Force Systems Command's Electronic Systems Division (Hanscom AFB, MA). Although similar efforts have been made for data processing software development in the private sector, Ferguson says that those efforts don't suffice for weapons systems.

The three DARPA contracts were awarded to Boeing Aerospace (Seattle, WA), IBM Federal Systems Division (Gaithersburg, MD) and Unisys (Reston, VA). —*Sydney Shapiro*

Could fiberoptics breathe new life into terminals?

The main reason for the demise of terminals has been the fact that they represent an I/O bottleneck between the host CPU and the user. With the advent of low-cost, high speed microprocessors, integrated workstations have offered users CPU, memory and display in one high-bandwidth package. But even workstations are networked, so that one may take the larger view that a system—be it terminals connected to a mainframe or workstations in a LAN—represents a computing resource with a given total bandwidth available to users.

In introducing its 4211 two-dimensional graphics terminal, Tektronix (Beaverton, OR) appears to be bucking the trend away from terminals. But by including a Fiber Distributed Data Interface, Tektronix hopes to take advantage of the I/O bandwidth offered by fiberoptics and offer an option with suitable price/performance for those times when local processing power isn't needed, but where high-speed I/O is essential for downloading and for viewing graphics displays to interact with a host computer. Tektronix, by the way, is still very much in the workstation business. —*Tom Williams*

Manufacturers of real-time computers join forces

The merger of real-time computer vendors Masscomp (Westford, MA) and Concurrent Computer (Tinton Falls, NJ) will help them stay afloat against larger, well-established rivals such as Hewlett-Packard (Palo Alto, CA) and Gould (Cleve-

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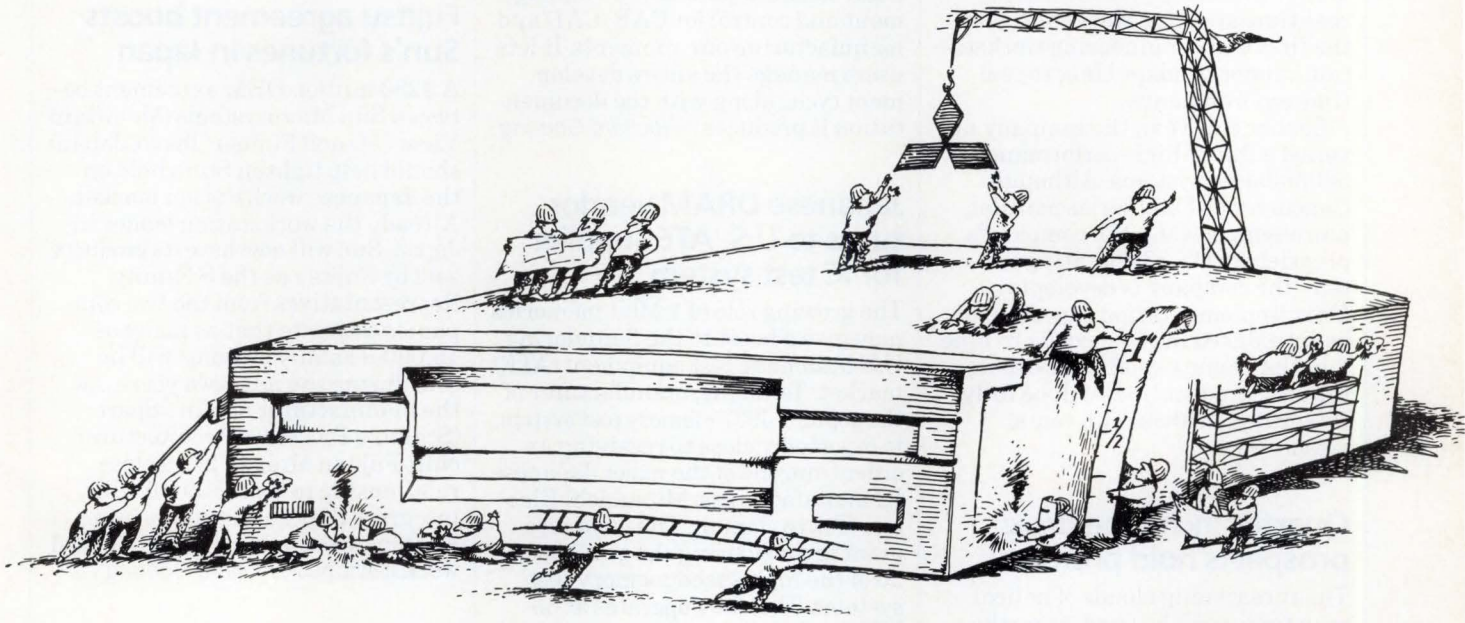

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MF353C	3½″	1″	1MB	+5V
MF355C	3½″	1″	1MB/2MB	+5V
MF501B, C	5¼″	1.61″	0.5MB	+5V and +12V
MF504B, C	5¼″	1.61″	0.5MB/1MB/1.6MB	+5V and +12V
M2896	8″	2.25″	1.6MB	+5V and +24V

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CIRCLE NO. 4

land, OH). Under terms of the agreement, Masscomp will be merged into Concurrent. Analysts expect that Concurrent's worldwide distribution system will improve Masscomp's ability to deliver its Unix-based real-time systems. Masscomp was the first Unix engineering workstation vendor to adapt Unix to real-time environments.

Earlier this year, the company unveiled a line of high-performance, 68030-based systems. Although Concurrent's 3200 series parallel processors now use the company's proprietary OS-32 operating system, the company is developing a Unix implementation expected to be introduced in the next six to nine months. Company officials expect that the product lines will be fully integrated in about two years. *—John Mayer*

Quarter-inch tape drive prospects hold promise

The threatening clouds of helical scan tape won't be shadowing the horizons of data cassette and cartridge tape drives for some time to come, according to the tape industry gurus at Freeman Associates (Santa Barbara, CA). Cassette and cartridge drives will grow at a 9 percent compounded rate through 1993, according to Freeman's latest study. Quarter-inch cartridges are expected to lead the way as quantity shipments move to the 125-/150-Mbyte range and later to the 320-Mbyte range. Manufacturers' concerted efforts to band together under the auspices of the Working Group for Quarter-Inch Cartridge Compatibility and establish standard and interchangeable recording formats and interfaces will continue to spur growth. *—John Mayer*

Data-management tools enhance CAD offerings

Data base management has long been a sore point for CAD managers. That's why third-party suppliers of engineering data-management systems, such as Sherpa (San Jose, CA), have emerged. Now Hewlett-Packard (Palo Alto, CA), active in mechanical and electrical CAD, will take an active role in engineering data management by selling Sherpa's Design Management System (DMS) on HP 9000 workstations. Sherpa's DMS software provides file management and control for CAE, CAD and manufacturing environments. It lets users manage the entire development cycle, along with the documentation it produces. *—Richard Goering*

Japanese DRAM vendor turns to U.S. ATE supplier for IC test system

The growing role of 1-Mbit memories may give a boost to the floundering U.S. automatic test equipment (ATE) market. Teradyne, manufacturer of the popular J937 memory test system, is reportedly close to receiving an order from one of the major Japanese IC manufacturers, Mitsubishi Electric (Tokyo, Japan). The Japanese giant is considering the purchase of 26 of the high-speed memory test systems. The J937 operates at 50 MHz and can test up to 16 devices in parallel—capabilities highly applicable for testing 1- or 4-Mbit dynamic RAMs. The system's low capacitive loading, about 35 pF, and its 750-ps system accuracy are designed to meet the demands of high-speed static RAMs. *—John Mayer*

Pace quickens in development of thin-film superconductor

A superconductor with 10 times the current density of existing high-temperature superconductors? That's what researchers at Sumitomo Electric Industries (Tokyo, Japan) say they've developed using a bismuth-type high-temperature ceramic super conductor. Discovered last January, bismuth-type ceramics offer a higher critical temperature (110°K), better chemical stability and lower cost.

The superconductor developed by Sumitomo researchers yields a current density of 1.9 million A/cm² at liquid nitrogen temperatures. Previously developed products only reached 200,000 A/cm². The 0.2-micron film consists of a bismuth-strontium-potassium-copper oxide over a substrate of single-crystal magnesium. *—John Mayer*

Fujitsu agreement boosts Sun's fortunes in Japan

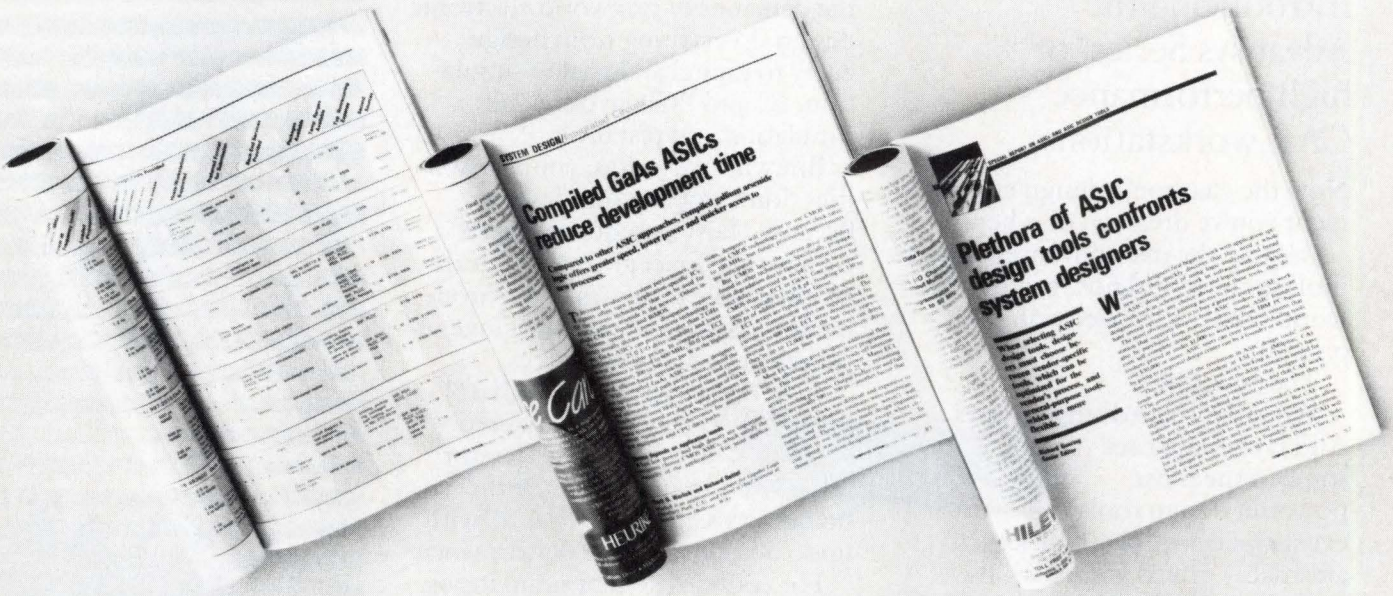
A $280 million OEM agreement between Sun Microsystems (Mountain View, CA) and Fujitsu (Tokyo, Japan) should help tighten Sun's hold on the Japanese workstation market. Already the workstation leader in Japan, Sun will now have its products sold by Fujitsu as the S Family. Representatives from the two companies estimate that as many as 15,000 S Family systems will be sold during the next two years. As the manufacturer of Sun's Sparc (Scalable Processor Architecture) chip, Fujitsu already has a close relationship to Sun. Fujitsu will integrate Sun workstations into Fujitsu's existing line of Unix-based workstations. *—Richard Goering*

NuBus moves toward open-architecture status

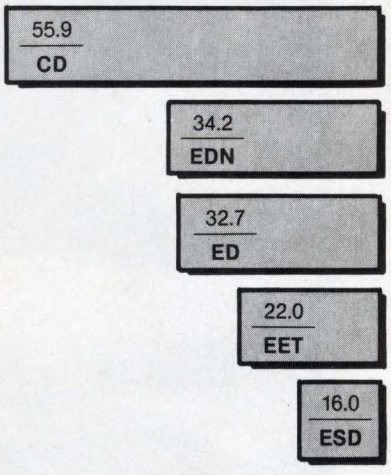
When is a computer enclosure news? When it's the first such product available for the NuBus. The appearance of an eight-slot NuBus chassis from Second Wave (Austin, TX) at last month's MacWorld Expo supports predictions that the bus will not just be an add-in vehicle for Apple's Macintosh II, but a full-fledged open-architecture bus that will find use in computer systems from multiple vendors. In these, the early days of NuBus, however, the Mac II is most likely to be the undisputed development platform for the bus.

MacWorld also witnessed a number of new hardware and software products for NuBus and the third, most populous meeting of the NuBus Manufacturers and Users Group. According to Joe Ramunni, the group's promotional director and president of Mizar, NuBus is uniquely positioned as a "crossroads bus that can blend the power expected in the industrial and OEM worlds with the plug-and-play compatibility expected in the commercial world." *—David Lieberman*

We define the market...



for ASICs.



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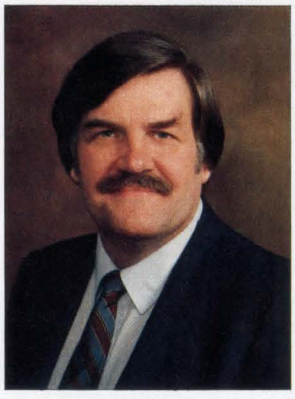

John C. Miklosz
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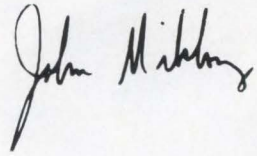
Reading Irwin Feerst's unrelenting attacks on the IEEE, it's hard to believe that the two might be in agreement, however slight, on any issue. But incredulous as it seems, the giant and the giant killer have come to similar conclusions—well, almost—about Section 1706 of The Tax Reform Act. Most of us aren't affected by Section 1706, although we all felt the impact of The Tax Reform Act in the days leading up to April 15 of this year. In brief, one provision of Section 1706 denies the tax status enjoyed by self-employed, independent contractors (such as doctors, lawyers, freelance writers, interior decorators and real-estate agents) to independent engineering, computer and scientific professionals. Technical professionals, it seems, must be considered no more than wage hands who can earn a livelihood only by working as someone else's employee.

The most obvious, and onerous, ramification of being treated as an employee, rather than as an independent, is that the "employer" must withhold income tax and social security, no matter how large or small the job performed or the amount paid for the work. The difference in status between an employee and an independent contractor is also crucial when it comes to pension planning, IRAs and Keoghs. Going out on your own and hitting it big—a dream that probably every engineer and computer specialist has had—is hard enough. There's no need for the Feds to make it harder by denying the tax status enjoyed by all other self-employed individuals.

Fortunately, some members of Congress weren't blind to the discriminatory nature of Section 1706, and the Senate Finance Committee is now looking at redressing this inequity, along with several others such as the tax on employer-provided educational assistance (which affects *every* employed professional). So far, it looks as if the exclusion from taxable income of employer-provided educational benefits will be restored through 1990. The part of Section 1706 affecting independent engineering and computer professionals is going through some rough sledding, however, and as it now stands, anyone hiring an independent engineering or computer professional will be required to withhold 10 percent for taxes.

Irwin Feerst has been bombarding members of the committee about the inequities of Section 1706. The IEEE also is supporting the redress of these inequities. We'd make at least one further recommendation: while the members of the Senate Finance Committee are considering the 10 percent withholding provision, perhaps they should also consider inclusion of payments made for speaking engagements. Politicians are a different class of professional from engineers and computer specialists. But they shouldn't be different when it comes to tax treatment. And neither should technical professionals.



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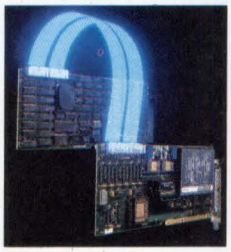

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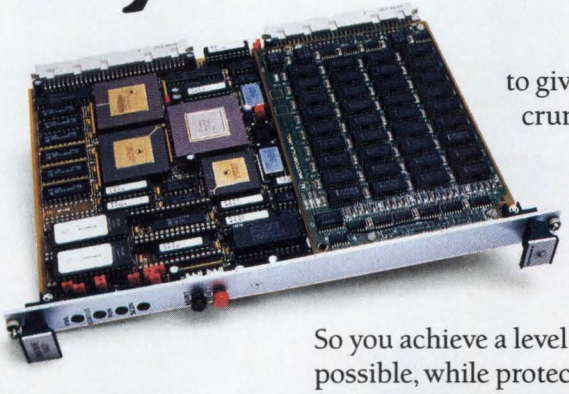

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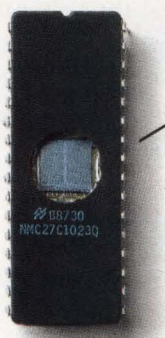

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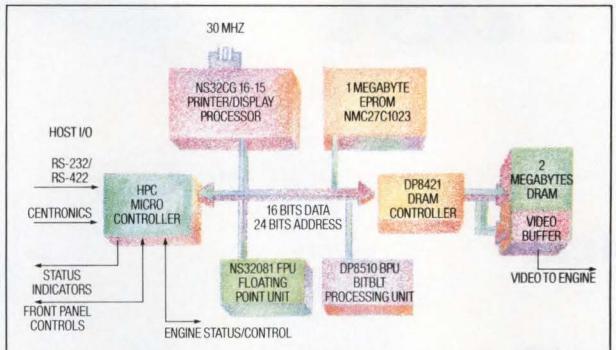

The NS32CG16 is the heart of a high-performance, cost-effective systems solution for applications like this page-printer controller.

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The NS32CG16 combines the programmability of a high-performance 32-bit microprocessor with the power of a specialized graphics coprocessor. It includes 18 dedicated graphics instructions for:

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- supports CCITT Group III and IV protocols for facsimile transmission
- on-chip clock generator
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- on-chip DMA support circuitry.

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INTEGRATED CIRCUITS

Functionality and partitioning distinguish Micro Channel chip sets

S. Louis Martin, Contributing Editor

Although similar, the available PS/2 Micro Channel chip sets—three from Western Digital's Faraday division (Sunnyvale, CA), two from Chips and Technologies (San Jose, CA), and one from Intel (Folsom, CA)—are sufficiently different to make choosing one difficult. What's more, new entries, such as the one from G-2 (Milpitas, CA), are appearing (see "Newest PS/2 chip set first to include BIOS", p 22). Designers can, however, simplify the decision by carefully comparing features.

The comparison involves a lengthy list of functions that must be incorporated into Micro Channel chip sets to provide compatibility with the various IBM Personal System/2 models. Compatibility is a big issue with such chip sets. Intel's implementation, for example, is "100 percent register-compatible with IBM's implementation," says Rajiv Sachdeva, Intel marketing product line manager. "We implemented that by using gate-level extraction." Though much rhetoric has been traded on this issue, all three vendors claim to have done a gate-level extraction and to have full knowledge of the PS/2's mysterious "undocumented" registers.

Basic functions to compare include DMA, Micro Channel control, memory control, system peripheral control/support, address bus buffers, data bus buffers, address bus control, data bus control and Video Graphics Array (VGA) support. Additional functions in the sets include various peripheral support functions such as an interface for a floppy disk controller and a keyboard, clock/timing generation, central arbitration, programmable option selection, wait-state control, coprocessor interface logic, a watchdog timer, an interrupt controller, cache support or interface, and so forth. And the list goes on.

The sets and their processors

Designated the 82310, Intel's five-chip set is aimed directly at clones of the PS/2 Model 80, but the set can be used for Model 50 and 60 clones as well, since the feature sets are the same for all three models. Normally, Model 50/60 designs use an 80286 processor, but Intel uses the 80386-SX, the 16-bit-bus version of the 80386, with the 82310 chip set to implement the Model 50/60. With a little extra logic, an actual 80286 can be used with the Intel set, though that isn't what Intel is promoting.

Intel achieved register compatibility for its 82310 Micro Channel chip set by doing a gate-level extraction, according to Rajiv Sachdeva, Intel marketing manager. IBM compatibility is key to the success of such chip sets.

Two chip sets are available from Chips and Technologies: the Chips/250 for the PS/2 Model 50/60, and the Chips/280 for Models 80 and 70. Chips and Technologies isn't bending over backwards for the 80386SX, claiming that it can be used with the Chips/250 set with very little extra logic. Each set contains seven chips, with three of the seven in common.

The third vendor, Western Digital, offers the 5400 four-chip set for the Model 50/60 using an 80286 processor. In October, the company will introduce two new sets: the four-chip 7400 for a Model 50/60 using an 80386SX, and the five-chip 6500 for the 80386-based Model 80.

DMA combined or separate

In its 82310, Intel combines the DMA function with the Micro Channel controller in the 82307—the same as in the IBM implementation—as does Western Digital in the 5010, part of the 5400 chip set. Chips and Technologies takes a different approach, separating the DMA function from the Micro Channel function in both of the chip sets. The 82C223 handles the DMA function in both, while the 82C221 handles the Micro Channel (and CPU control) function in the Chips/250 set and the 82C321 handles the Micro Channel (and CPU control) function in the Chips/280 set.

While Western Digital stayed with the IBM partitioning in the 5400 set, for the 7400 and the 6500 the company made DMA a completely separate function, as Chips and Technologies did. Western Digital, however, combined the Micro Channel function with the memory control function. (The 7030 combines these two functions in the 7400, while the 6030 combines these functions in the 6500.)

"Because it's a 32-bit processor we're dealing with, the architecture needed to be substantially larger. And with the number of available pins, we had to move the channel controls out," explains Collier Buffington, vice-president and general manager at Western Digital. He indicates that another deciding factor in this departure from the IBM/Intel partitioning was that Western Digital has implemented a 32-bit DMA controller in the 6010.

Chips and Technologies provides data bus buffers and control via the 82C225 for the Chips/250 and 82C325 for the Chips/280. There are no address or data bus buffers on the Intel chip set, but Intel does provide a data bus controller in the form of the 82308. Western Digital provides both address and data bus buffers for the 5400 and the 7400 in a single chip, the 5020. For the 6500, Western Digital provides another chip, the 6022. But two 6022s must be used for separate address and data buffers, hence raising the number of chips in the 6500 set to five.

One aspect of the memory control-

INTEGRATED CIRCUITS

lers is confusing at first. While all three vendors put memory address decoding on a single chip (the memory controller), I/O address decoding is handled differently by all three. Intel follows the IBM approach and uses two chips—the 82309 and the 82306—for most of the I/O address decode. One other chip, the 82307, also does I/O address decoding. Chips and Technologies does the complete I/O address decode on a single chip, the 82C222/322 memory controller. And Western Digital spreads the I/O decode over the entire chip set (although most is on the 6000 peripheral control chip).

■ Cache support

All three vendors are offering cache support for at least the 80386-based machines, or will be shortly. Intel offers an interface to its own cache controller, the 82385, while Chips and Technologies will soon offer cache controllers built into its memory controllers. The cache controllers from both Intel and Chips and Technologies are intended for cache sizes up to 32 kbits. But according to Tom Heil, technical marketing engineer at Intel, "Although the 82385 is designed as a 32-kbit cache controller, it can support larger cache sizes, as evidenced by the fact that IBM's 25-MHz Model 70 uses an 82385 and supports 64-kbit cache." There is some extra logic required, however.

Western Digital is touting that all three of its memory controllers, the 5030, the 7030 and the 6030, have unlimited cache size. But there appears to be a catch. Western Digital achieves unlimited size by not including the cache tag hardware, an item included in the the Intel and the Chips and Technologies controllers. At least one extra chip is thus required, and both Intel and Chips and Technologies question what's gained by slightly increasing the hit rate while requiring at least one other chip—a cache tag chip—and thus possibly adding wait states.

Western Digital's memory controllers support page mode, static column mode, four-way interleaving and LIM EMS (Lotus-Intel-Microsoft extended memory specification) 4.0 when not using the cache. The controllers offer page mode with caching when the cache is used. The integrated cache controller from Chips and Technologies will offer only basic dynamic RAM controller operation with the cache. For page and static column modes, interleaving and LIM EMS 4.0, a nonintegrated memory controller must be used.

Concerning the motivation for the integrated Western Digital con-

Newest PS/2 chip set first to include BIOS

The most recently announced Micro Channel chip set comes from G-2, an affiliate of LSI Logic (Milpitas, CA). Billed as the Universal PS/2 Chip Set, this newest entrant is the only one with BIOS software. G-2 is offering a single BIOS that's "self-scaling" to accommodate the variety of processors that can be used with IBM's Personal System/2.

Designed by Bull Micral (Roseville, MN), the chip set consists of seven application-specific IC gate arrays that support 80286-, 80386- and 80386SX-based systems. These are the GC181 CPU and Micro Channel Controller, the GC182 Memory Controller, the GC183 DMA Controller, two GC184 Address and Data Buffer/Controllers, the GC186 Peripheral and I/O Controller and the GC205 Video Graphics Array (VGA) Controller. The set will support the current Models 50, 60, 70 and 80 of IBM's PS/2, and "whatever PS/2 machine is next in line," according to Bert McComas, marketing manager at G-2.

Compared to the other vendors of Micro Channel chip sets, G-2 is taking a somewhat different approach to DMA timing and hence the Micro Channel. Timing of the DMA associated with the Micro Channel can be done in two ways. It can be done synchronously, with a divide-by-two clock derived from the CPU clock, or timing can be done completely independent of the CPU with a separate clock input to the DMA. "We supply a half CPU speed clock for convenience, but we can time the DMA from any source," says McComas. G-2 timing can thus be synchronous or asynchronous.

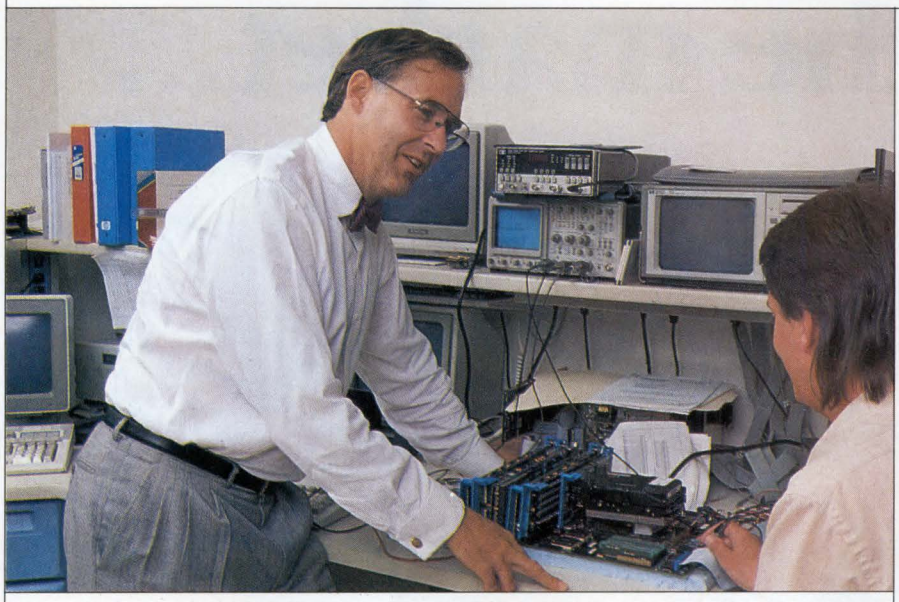
The VGA chip supports both VGA and Enhanced Graphics Adapter standards, but not some of the standards that Intel, Chips and Technologies, and Western Digital support, such as the Color Graphics Adapter, Monochrome Display Adapter, and Hercules graphics array standards. While G-2 chose not to offer the range of backward compatibility the other vendors offer, the company appears to have gone to great lengths to speed up graphics operations by including dual-port video RAM in its VGA chip. "There are a lot of little things that can be done to speed up graphics, but they add up to maybe two times the performance of the IBM product," says McComas. "With video RAMs, performance can be increased as much as six times that of IBM's VGA."

G-2 has a single BiCMOS device that includes address and data buffers and the associated address and data control. Other vendors, such as Intel, don't offer address and data buffers at all. No universal asynchronous receiver-transmitter, such as is in the Multi-Function Controller from Chips and Technologies, is included but pins have been reserved for one. G-2 includes interfacing for a floppy disk controller but has none of the support circuitry, recommending the use of the floppy disk controller (the 57C65) from Western Digital. Two bus options are available for placement of main memory, allowing use of slower dynamic RAMs if desired.

Matched memory cycles are supported for faster operation, but the memory controller supports only page mode and two-way interleaving. No cache support will be offered initially, but an interface, probably to the Intel 82385 Cache Controller, will be available in samples (25-MHz version) early next year.

The total system chip count, excluding memory and processors, is 54 chips—for a Model 50, 60, 70 or 80 mother board. For more than four expansion slots, two to four additional buffers may be required, according to McComas. A single chip count for all models is unique, since all other vendors come up with different chip counts depending on the model.

The G-2 chips operate in systems up to 20 MHz, and the price is $222 for quantities of 100 to 999. Samples will be available in September; full production will be in fourth quarter of this year.



Western Digital pulled the Micro Channel controls out of two of its DMA chips. Collier Buffington, vice-president and general manager of the company, says that the 32-bit processor needed a larger architecture and the channel had to be moved out because of the limited number of available pins.

troller, Buffington says, "After January, there probably aren't going to be any more 20-MHz 80386s; everybody's going to 25 MHz as fast as Intel can build them." Moreover, Buffington maintains that everyone will be running caches because there won't be memory fast enough to exploit the speed of the 80386 at 25 MHz without cache. "The most important thing was to give optimum performance for the 80386 at 25 and 33 MHz—so we designed our cache controller to simultaneously support page mode and caching," he says.

Partitionings differ

Like cache strategy, the placement of various functions within the chip set changes from vendor to vendor. All six of the chip sets provide a system peripheral support/control chip. In the case of Intel, the chip is the 82306 (partitioned exactly the same as IBM); in both Chips and Technologies sets, it's the 82C226; and Western Digital uses its 6000 chip across all three sets.

Western Digital and Chips and Technologies put two interrupt controllers on their peripheral chips; Intel puts one interrupt controller on the combined DMA and Micro Channel controller chip, the 82307. Intel puts the floppy disk subsystem support here; Chips and Technologies puts that function on a supplementary peripheral chip, the 82C607 Multi-Function Controller; and Western Digital appears to have omitted the floppy disk subsystem support, counting on the use of its 57C65 floppy disk controller chip. Western Digital includes the coprocessor interface logic on this chip, while Intel places that logic back on the DMA and Micro Channel Controller chip, and Chips and Technologies puts the coprocessor interface on its Micro Channel (and CPU) controller, the 82C221/321.

Another important difference involves bus timing. Both Intel and Western Digital have followed IBM's lead in deriving the 10-MHz Micro Channel DMA clock from the CPU clock. The result is a somewhat reduced ability to accommodate processor speed upgrades. Chips and Technologies, on the other hand, provides

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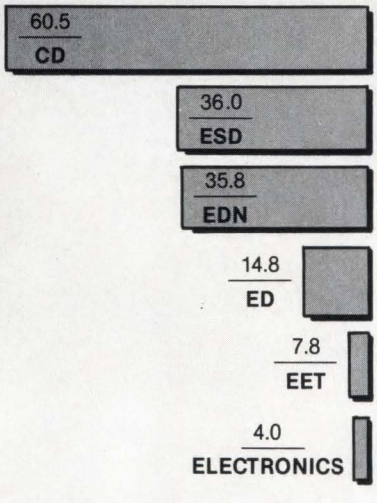

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INTEGRATED CIRCUITS

PARTITIONING OF PS/2 FUNCTIONS

Function \ Chip Set	Intel	Chips and Technologies		Western Digital		
	82310	Chips/250	Chips/280	5400	7400	6500
DMA	82307	82C223	82C223	5010	6010	6010
Micro Channel Control	82307	82C221	82C321	5010	7030	6030
Memory Control	82309	82C222	82C322	5030	7030	6030
System Peripherals	82306	82C226	82C226	6000	6000	6000
Address Buffer	—	82C225	82C325	5020	5020	6022
Data Buffer	—	82C225	82C325	5020	5020	6022
Address Control	82309	82C221 & -225	82C321 & -325	5010	7030	6030
Data Control	82308	82C221 & -225	82C321 & -325	5010	7030	6030
VGA	82706	82C451	82C451	*	*	*
Multi-Function	—	82C607	82C607	—	—	—

*offered through the PVGA1 from Western Digital's Paradise division

what it calls a dual asynchronous bus structure, in which the timing over the Micro Channel is completely independent of the CPU bus timing. Consequently, processor speed upgrades do not alter DMA timing for the company's chip set.

"Our chip set doesn't have to be changed when you go from 16 to 20 MHz or from 20 to 25 MHz. That's because of the architecture we've implemented," says Sikander Naqvi, marketing manager at Chips and Technologies.

"Intel and IBM run the DMA at the same fraction of the processor clock," says Michael Slater, editor and publisher of the *Microprocessor Report* (Palo Alto, CA). "Because of that, as they increase the speed of the processor clock, they sometimes have to actually decrease the speed of the DMA if they have to jump to a divide-by-3 instead of a divide-by-2." This difference boils down to the fact that Chips and Technologies can hold the DMA speed at its maximum specified value, independent of the processor clock frequency.

■ Varied coprocessor support

There are differences in coprocessor support that go beyond partitioning issues. Intel supports only its own coprocessors, the 80387 and the 80387-SX, whereas Western Digital claims to support a variety of coprocessors, such as the Weitek 3167 and the Texas Instruments 8847. Chips and Technologies appears to be supporting only the Intel 80287 or 80387 coprocessors. Western Digital also offers, in the 7400 and the 6500, 32-bit addressing for DMA (in the 6010, common to both sets), whereas Intel and Chips and Technologies are limited to 24-bit DMA addressing. The principal architect for the Micro Channel family at Western Digital says that the 32-bit addressing lets the company run faster DMA operations. The 6010 also has the required pins to provide 32-bit data, but it's not set up internally to handle 32-bit data, according to Larry Jones, chief scientist at Western Digital.

The chips also differ in their approach to graphics support. The VGA chip from Intel (the 82706) is functionally the same as the VGA chip in

the IBM systems. Intel offers backward compatibility to Enhanced Graphics Adapter (EGA), Color Graphics Adapter (CGA) and Monochrome Display Adapter (MDA) graphics standards. Chips and Technologies, meanwhile, claims to offer superior graphics support with the 82C451, which has backward compatibility to EGA, CGA, MDA and Hercules graphics array standards. While Western Digital doesn't offer a VGA chip with its set, the company recommends the PVGA1 from its Paradise division, which offers the same backward compatibility as the Chips and Technolgies VGA. The PVGA1 and the Chips and Technologies VGA chip offer a 16-bit data interface to VGA, while the Intel/IBM chip has an 8-bit interface.

All three vendors offer some level of cache support, I/O recovery timers and EPROM shadowing, which are extra features implemented discretely in the IBM systems. And while Intel is positioned to provide high IBM compatibility—three Intel chips (82306, 82307 and 82706) have identical functionality to IBM chips—and isn't making noise about performance improvements, others are. In fact, Chips and Technologies claims that its architectural improvements increase Micro Channel throughput by as much as 30 percent. "This has to do with functionality because on the Micro Channel you can't just increase speed to increase throughput, since Micro Channel speed is fixed at 10 MHz," says Naqvi. "You have to add functions that let you run at higher bandwidth."

Differences of omission

Some features are included in some sets and not others. For instance, Intel doesn't offer either address or data buffers because it thinks that buffers, though inexpensive, add a lot of pins when integrated. Chips and Technologies and Western Digital do include buffers. Similarly, Chips and Technologies includes a universal asynchronous receiver-transmitter on its Multi-Function Controller, while Intel and Western Digital omit this function. Chips and Technologies also includes a complete analog data separator on the same chip, whereas Intel only includes the digital portion of a data separator on the company's peripheral support chip.

Chips and Technologies offers an option of placing the DRAMs on either the local bus or the memory bus, allowing the use of slower and hence less expensive DRAMs in the former case. (Western Digital offers the same option.) Chips and Technologies offers registers for setting noncachable regions in the main memory. "Noncachable regions become very important for compatibility issues where you're in a LAN en-

vironment, or where you have dual-port memory or a video RAM that you don't want cached," says Nelson Chan, product manager at Chips and Technologies.

Chips and Technologies provides four areas that can be designated as noncachable via four mapping registers. The company also offers error detection and correction hooks, which Western Digital doesn't.

Cost and total chip count

Finally, there are two crucial differences—the cost of the chip sets and the total number of chips required to build Micro-Channel-compatible computers with them. Pricing is as follows: In quantities of 1,000, the Intel set sells for $250 for the 20-MHz version and $205 for the 16-MHz version. The Intel 82385 cache controller is a somewhat expensive addition at $95 in quantities of 1,000. In the same quantities, Western Digital's 5400—integrated cache controller included—sells for $155 for the 16-MHz version and $165 for the 20-MHz version.

In thousands, the Chips/250 set goes for $169.50 for the 16-MHz version; the Chips/280 goes for $239.50 for the 20-MHz version. (These prices from Chips and Technologies are for the current version of the product that doesn't include the integrated cache controller. Samples for the integrated version, designated the 82C327, will be available this month. No price is available, but Chips and Technologies says that the price will be less than the price for Intel's nonintegrated cache controller.)

While some vendors seem to regard the chip count question as a tactless invasion of privacy, the question is a fair one: If I buy your chip set, how many other chips will I have to buy to put together a complete PS/2 mother board?

For Chips and Technologies, the count—excluding processors and memory—is 66 chips for a Model 60, 63 chips for a Model 50, and 64 chips for a Model 80. For Intel, the count is 65 chips for a Model 50/60, and 92 chips for a Model 80. (This Intel count is for a new version of the 82306, yet to be christened but available soon, that will offer higher integration over the current version. The current count without this chip is much higher.)

For Western Digital, the count is 46 chips with the 5400, and 55 chips with both the 7400 and the 6500.

Making a final choice

While a comparison of function partitioning is useful in deciding among chip sets, factors such as availability can determine the actual choice. Intel's chips are available now, and that's probably the main reason that Dell Computer (Austin, TX) and Tandy (Fort Worth, TX) chose Intel over Chips and Technologies and Western Digital for the first PS/2 clones. Chips and Technologies is now in production with the Chips/250 set and very close to production with the Chips/280 set. The 5400 from Western Digital will be in production by the end of this month, while the 5400 and the 6500 will be announced with samples available by October.

At the same time, price and chip count put Intel's set at a disadvantage. On the bases of chip count and price, Western Digital appears to be the winner. Assuming that the 7400 and the 6500 become available on schedule and that price structures don't change (in particular, that Chips and Technologies doesn't slash prices), the only other question is the quality of the functions provided. Here, Chips and Technologies would seem to have the lead with its dual-asynchronous architecture, while Western Digital might have an edge with its cache controller, which offers unlimited cache size and page mode operation as well. At the same time, unlimited cache size can be viewed as a liability because of the omission of the cache tag chip. Moreover, the performance improvements offered by Chips and Technologies probably deserve more analysis and comparison to the improvements claimed by Western Digital in the 32-bit DMA. □

INTEGRATED CIRCUITS

VGA chips look beyond IBM spec in search of new features

Ron Wilson, Senior Editor

After a year of competing to be more IBM-compatible than the next guy, designers of the VLSI chips used to implement IBM's Video Graphics Array (VGA) have pushed compatibility into the region of diminishing returns. The most recent chip sets represent a gate-level reverse engineering of IBM's hardware. They run with virtually all personal computer applications that support the VGA and even respond correctly to command sequences that aren't documented in IBM's technical manuals.

"We've taken a very careful approach to designing VGA hardware," says Keith Angelo, product manager for graphics operations at Chips and Technologies (San Jose, CA). "We looked at the IBM hardware at both the register level and the gate level. And we found that IBM has embedded features in its own implementation that aren't currently used. Some are below the register level."

Once vendors have satisfied the need for strict IBM compatibility, they begin to look for other areas in which to pursue differential advantages. In the current generation of parts, there are four such areas: backward compatibility, more resolution and more colors, higher performance, and new functionality. While each area offers practical benefits to end-users, each also includes the risk of creating a feature incompatible with the IBM hardware—one that, therefore, won't be used by mainstream application software.

More adapter operating modes

The first two categories of added features in VGA chips concern the operating modes of the adapter. Graphics adapters generally offer a number of operating modes, each with a different combination of screen resolution and number of bits/pixel, as well as a choice of character-only or graphics operation. Each mode usually has its own way of using display memory to store image data and refresh the display screen.

In its own VGA, IBM chose to provide an entirely new set of modes, incompatible with those it had defined for the earlier Color Graphics Adapter (CGA) and Enhanced Graphics Adapter (EGA) cards. The company then provided software that could adapt the BIOS calls of applications written for the earlier cards to work with the new hardware.

The problem with this approach is that most popular PC software doesn't use BIOS calls to handle the display, because the way DOS handles the system calls is too slow. Instead, most applications write directly to the graphics adapter hardware. Most existing applications, therefore, are incompatible with IBM's VGA until their display drivers have been modified.

To solve this problem, chips like Cirrus Logic's GD510A/520A take a different approach. "What users need is hardware-level backward compatibility with earlier graphics adapters," says George Alexy, vice-president of marketing at Cirrus. "So we provided the hardware registers for the EGA, CGA, MDA (monochrome display adapter) and Hercules boards in our chip. And we provided the display logic to produce correct images for each of these devices on any of the monitors we support, including the new analog IBM Personal System/2 monitors."

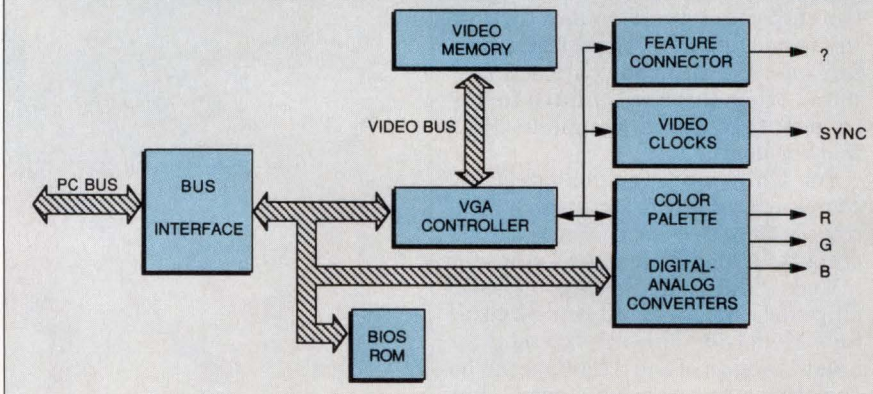
Many chip designers are also looking to the abilities of new analog multisync monitors. The Cirrus chip set, for instance, provides a 320-×200-pixel mode, an 8-bit/pixel mode and an 800-×600-pixel higher resolution mode. The high-end 82C452 chip from Chips and Technologies offers an 8-bit, 640×480 mode; a 4-bit, 960×720 mode; and a 1,280×960 monochrome.

These higher resolutions have implications not just for the VGA controller chip, but also for the Palette DAC (the chip containing the VGA's color lookup tables and video digital-to-analog converters). To produce higher resolutions, pixels have to come out of the VGA at a higher rate. To meet this requirement, Inmos and Triad Semiconductor (both of Colorado Springs, CO) created Palette DACs that operate at up to 65 or 66 MHz, sufficient speed for 1,024-× 768-pixel, 60-Hz displays.

CPU-VGA bandwidth increased

In the pursuit of speed, designers can increase two parameters: bus width and memory availability. Of the two, bus width is most easily changed. Most early VGA boards, including those by IBM, used an 8-bit connection to the system bus. Several of the new chips, such as the 82C450 family from Chips and Technologies and the GD510A/520A chip set from Cirrus Logic, use a 16-bit bus interface.

VIDEO GRAPHICS ARRAY SYSTEM



Each module in a Video Graphics Array system offers the opportunity for performance and feature enhancement. Chip vendors are focusing increased attention on the controller chip, the Palette DAC and the major data paths.

Potentially, the increase from 8- to 16-bit bus interface could double the bandwidth between the CPU and the VGA, except for a couple of limiting factors.

The first limitation is software. Applications must have new, non-IBM drivers in order to use the 16-bit interface. In reality, the wider interface will only benefit applications for which the chip or VGA board vendor supplies new driver code.

Another limitation is a hardware bottleneck. The CPU can change display memory only when the memory isn't busy refreshing the screen. So the availability of display-memory cycles is a key to performance, particularly for window-management packages that must move huge numbers of pixels interactively.

Expanding display memory

One technique for increasing display-memory availability is a 32-bit interface between the VGA controller chip and the display memory. Since the controller can read more pixels on each display-memory cycle, there are more cycles left over after screen refreshing for the PC CPU. A related technique is to use display-memory dynamic RAMs with faster cycle times, again reducing the percentage of total cycles needed by the display refresh circuitry.

Either of these techniques requires that thought be given to the arbitration scheme that grants a cycle to the CPU or to the display. "IBM uses a fixed interleaving," explains Cirrus' Alexy. "The CPU gets one cycle out of every seven. Our new chip set, depending on the screen resolution in use, can provide 1:7, 1:4 or 1:1 interleaving, making the display memory more available to the CPU."

Chips and Technologies' approach is somewhat different. Its 82C452 chip frees display-memory bandwidth by placing a first-in, first-out register between the memory and the video circuitry. Then the addition of arbitration logic in place of a fixed interleaving scheme makes the display memory available just about every time the CPU requests a cycle. "With the arbitration scheme, the CPU will get immediate access to video memory on seven out of 10 tries," says Viren Shah, technical marketer at Chips and Technologies.

A similar memory-access bottleneck occurs at the other dual-port memory in the VGA, the Palette DAC's color lookup table. In order to change the color mapping—or the relationship between a pixel value

"What users need is hardware-level backward compatibility with earlier graphics adapters."

—George Alexy, Cirrus Logic

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and a screen color—the CPU must be able to write new values into the lookup table. Some chip vendors suggest that this be done only during horizontal or vertical blanking to avoid noise on the screen. But the TR9C1710, a new part from Triad, uses its own arbitration scheme to avoid snow on the screen during lookup table accesses.

Moving beyond VGA

Beyond bandwidth improvements, there isn't much that can be done within the bounds of strict software compatibility to improve the speed of the VGA. But under pressure from performance-hungry window managers, chip vendors are looking beyond those bounds for solutions.

An example of an effective solution is the hardware support for bit block transfers (bitblts) in the 82C452 chip from Chips and Technologies. "The chip doesn't actually support a bitblt command. There are extra write modes to cut the number of instructions the CPU must execute during nonaligned blts," says Shah. The company estimates that when a window manager is moving a block of

pixels that aren't aligned with a byte boundary in display memory, the new modes can reduce the number of CPU instructions per byte moved from 64 to six or seven.

Another area for extensions is cursor support. On the standard VGA, complicated cursors will have to be moved around in display memory by CPU reads and writes, at a large cost to CPU time and memory bandwidth. Chips and Technologies' 82C452 lets the application define a cursor of up to 64×512 pixels in display memory. Then the program can command the VGA chip to move the cursor, instead of having to move each pixel of the cursor. The company claims that this capability can reduce the CPU load for cursor control by 96 percent.

■ Vendor relationships critical

Such functional enhancements to the VGA standard can make a big difference in application performance. But like changes in screen resolution, pixel depth or CPU bus width, these features require a reworking of the application software, at least at the driver level. This makes the relationship between chip vendors and application vendors even more critical.

It's clear that major software vendors aren't going to produce versions of their code for any display hardware other than IBM's. Realistically, chip vendors must learn from software vendors how to write a driver for their new VGA and then plan on providing the driver to chip customers. Since no two PC applications do their graphics the same way, this process will have to be repeated for each important software package the chip vendor wants to run fast.

Eventually, the push for greater speed and more features in VGA chip sets could have an ironic effect. By making chip vendors' ability to offer better performance dependent on their ability to deliver driver code, the trend to depart from VGA could result in a shakeout. A few vendors with excellent software relationships may be able to consistently offer better performance to end-users, despite continued hardware innovations by smaller vendors. Then the VGA, like the CGA and the EGA before it, will have become so mired in compatibility issues that it will be unable to evolve further. □

INTEGRATED CIRCUITS

Smart card development expands as standard nears final approval

S. Louis Martin, Contributing Editor

In the nearly eight years of work on smart cards, some companies have gone ahead and developed products based on a still-forthcoming standard. But now, with the first two parts of the smart card international standard (ISO 7816) approved and published and with part three being circulated for approval, those companies that have been holding back may find that the time is right to shift into gear.

Smart cards basically consist of a processor and memory embedded inside a plastic card. The processing tends to be low-powered. Motorola (Austin, TX), for example, uses its 6805 8-bit microprocessor; Siemens (Munich, West Germany), at the high end, uses the Intel 8051 microcontroller. The processor and memory tend to be put on a single chip, but that's not a requirement. The cards also include a set of contacts—somewhat akin to the edge connector on a printed circuit board—for communication with the card reader.

Companies that have been holding back on smart cards may find that the time is right to shift into gear.

■ ■ ■

Motorola and Siemens are big players in the smart card chip game. Motorola supplies microprocessors with on-chip memories that have capacities of between 1 and 8 kbytes. The most popular memory types are ROMs, EPROMs and EEPROMs, all available from Motorola, according to Paul Grimme, smart card product engineer at the company.

Siemens offers two main families of IC products for smart cards. One, for small applications, includes nonvolatile memories with pseudo-intelligent features, according to Roman Aragay, product marketing manager at Siemens. The intelligence is in the form of hardware that can protect the contents of the memories from unauthorized access.

The other Siemens IC family consists of 8051 microprocessors with on-chip, nonvolatile memory. Siemens uses EEPROM for its 1- to 10-kbit nonvolatile memory.

■ Credit card companies involved

While development of the ICs for smart cards has made a lot of progress, there has been less activity in development of the cards themselves. Some of the delay involves the major difference in strategy between the two biggest prospective customers of the cards, Visa and Mastercard.

Visa (San Francisco, CA) has come out with a somewhat extravagant design: a card that has a keyboard, a display and a magnetic stripe emulator. Visa calls it super-smart card. Aside from such "trinket value" of being a pocket calculator with a clock and storage capability as a notepad, the card is a secure device in that it requires the entry of a personal identification number. In addition, more than one account can be run on it, and it translates to different currencies.

The card's patented magnetic stripe emulator lets the card be used with a very large installed base of magnetic stripe card readers. U.S. Visa employees are testing the card for durability. Assuming all goes well, the card will be distributed to a select group of consumers at the end of this year. But with a manufacturing cost of possibly $15, the card will be an expensive item for the consumer.

Mastercard continues to research and test cards, but isn't working on fancy cards like Visa's. Mastercard is also involved with the standards committees. But Larry Ladouceur, vice-president of Mastercard (New York, NY), expresses some skepticism about the timely emergence of those standards.

U.S. government plunges in

One company that isn't waiting for a final standard is Micro Card Technologies (Dallas, TX). Paul Wittfeld, vice-president of the company, points out that while the card companies and the banks sort out their differences, it's the U.S. government that's a prime pusher of smart card usage in the United States. The U.S. Department of Agriculture, for example, is sponsoring the use of cards by peanut and tobacco farmers, and the Department of Defense is giving smart cards to recruits to pay their bills at the Parris Island (South Carolina) Marine training facility.

Micro Card, which primarily uses chips from Motorola and SGS-Thomson, is selling into all these markets. Wittfeld maintains that the infrastructure of the federal government is less resistant to change than that of the U.S. banking community.

A new Micro Card product in the general consumer area is the Smart Shopper Card. This card holds user checking account numbers, retail credit numbers, and Mastercard or Visa numbers. Users can select the account from which they want to pay. Now in the testing stage, the Smart Shopper Card also lets users store information such as clothing sizes and key dates. A card that will combine medical records and payment information will go into testing later this year, according to Wittfeld.

NEC (Tokyo, Japan), on the other hand, is taking a "wait-and-see approach," according to Toshihiko Ono, NEC assistant manager for memory marketing. The company has decided to wait for the standard before producing any cards, but it is doing engineering development work on ICs for the cards.

Meanwhile, NEC is producing memory cards, which have memory but no processing capability. The main application for memory cards is data storage for computers, and thus NEC is supplying fairly large amounts of memory. NEC's cards are credit-card size but thicker and contain up to 2 Mbytes of nonvolatile memory—currently ROM and, in the future, battery-backed static RAM.

Standard nearing completion

The international standard for smart card, ISO 7816, is in an interesting stage. Two parts have been signed off—part two was just published—and part three is now circulating for approval, according to Dorothy Hogan, vice-president of ANSI.

The first vote on part three failed, according to Pamela Marks, ISO secretariat for 7816. Only 52 percent voted approval, and 76 member countries must sign off with 75 percent in favor for the draft to pass. The negative votes included those from the United States, West Germany, Japan, the United Kingdom and the Netherlands. But modifications have been made, and the draft document should go back out to the member groups within a month or two. Voting should be completed within two months of that time. The likelihood of approval is great this time around, according to Marks. A complete specification for smart card thus could be available within three or four months.

Although some are skeptical about how long it will take to sign off part three, once this part is signed off there will be no more excuses for not making the cards and pushing them into service. □

Trying to find the right ICs?

Turn to the Integrated Circuits section in New Product Highlights. You might find just what you need.

DESIGN AND DEVELOPMENT TOOLS

Emerging EDA applications transform the Macintosh into a serious engineering tool

Richard Goering, Senior Editor

Many engineers have an IBM PC or a workstation in the office, and an Apple Computer (Cupertino, CA) Macintosh at home. The workstation is for work, and the Macintosh is for fun. But now that electronic design automation (EDA) applications are showing up on the Macintosh, that platform could become a serious engineering tool as well.

Applications such as schematic capture, gate-level logic simulation and printed circuit board layout are now available for the Macintosh family. What's more, two recent announcements could help make the Macintosh a strong platform for analog circuit simulation. One is this month's introduction of MacSpice from Deutsch Research (Palo Alto, CA); the other is the porting of PSpice to the Macintosh II by Microsim (Irvine, CA).

With 2-Mips performance, a Motorola 68881 floating-point coprocessor, up to 8 Mbytes of RAM and up to 80 Mbytes of hard disk, the Macintosh II is the strongest EDA platform in the company's product family. Apple provides a 12-in. monochrome display or a 13-in. color 480-×640-pixel display. With prices ranging from $4,000 to $8,000, the Macintosh II is competitive with low-end workstations from Apollo Computer (Chelmsford, MA) and Sun Microsystems (Mountain View, CA). The Macintosh Plus and Macintosh SE are less powerful but are still used for some EDA applications.

Many users have fallen in love with Apple's graphical user interface. "The Macintosh offers a consistent user interface no matter what package you're running," says Neil MacKenzie, engineering vice-president for Capilano Computing (Vancouver, B.C.). "If you're used to it, you can pick up a CAD package and learn it very quickly." MacKenzie also notes that the Macintosh supports a variety of desktop publishing software that can be used for engineering documentation.

■ Bargain-priced software

So far, the EDA applications on the Macintosh are low-cost packages, most costing less than $1,000. With the exception of one logic-synthesis program, application-specific IC library support isn't available.

Macintosh EDA applications also lack such features as behavioral logic simulation, hardware modeling, simulation acceleration and timing verification. But the Macintosh may be ideal for designers just starting out with EDA tools.

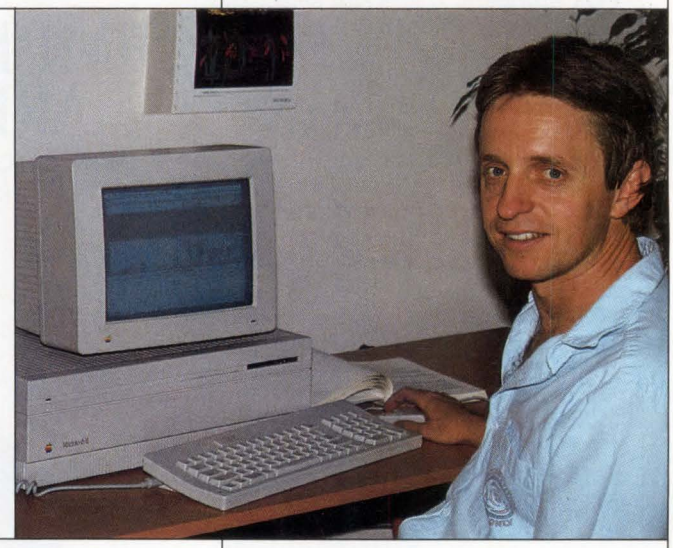
Although the Macintosh II supports A/UX, a multiuser implementation of AT&T's Unix System V, today's EDA applications use the native Macintosh operating system. "It's clear that most users want the Macintosh operating system," says Paul Tuinenga, executive vice-president of Microsim. "A/UX is a very expensive option that requires a hard disk, and people don't want to buy it for a $4,000 machine."

Users who want to run schematic entry on the Macintosh can choose Capilano's Design Works product or the McCad Schematics package from Vamp (Los Angeles, CA). With the introduction of Vamp's Digsim software in August, both schematic packages are now integrated with logic simulation. Both Design Works and McCad Schematics support such basic features as rubberbanding, rotation, panning and zooming, and they also support color.

Capilano and Vamp provide symbol libraries for common TTL, CMOS and analog components. Interfaces to printed circuit board CAD systems from such vendors as Calay (Irvine, CA) and Cadnetix (Boulder, CO) are available with both systems. While Vamp offers an interface to the Macintosh version of PSpice, Capilano provides schematic entry for Deutsch Research's MacSpice.

The digital simulators from Capilano and Vamp are fully integrated with schematic entry so that changes in the schematic are reflected in the simulation immediately. There's no need to compile net lists for either simulator. Simulation is built into Design Works, which is now priced at $685. Vamp, in contrast, provides Digsim as a $200 option for its McCad Schematics package, which costs $495.

A $200 simulator can't provide the features of a $50,000 workstation-based simulator, but it can offer some useful analysis for relatively simple



The Macintosh's graphical user interface makes it ideal for electronic design automation applications, according to Neil MacKenzie, engineering vice-president for Capilano Computing. Capilano offers the Design Works schematic entry package, integrated with logic simulation, for the Macintosh.

boards with standard parts. The simulators from Capilano and Vamp are essentially gate-level, functional simulators with very limited timing-analysis capabilities. Users can assign unit delays, but the simulators don't evaluate rise and fall times or setup and hold values. Simulation runs are generally limited to a few thousand gates.

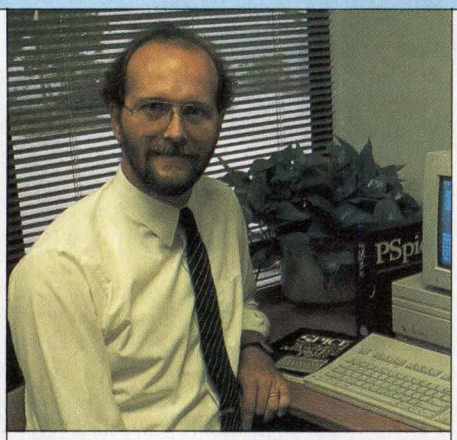
As a supplement to the Design Works package, Capilano offers a program called LPLC that generates fuse maps for programmable logic devices from Boolean equations, truth tables or state transition descriptions. Similar in concept to the Abel compiler from Data I/O (Redmond, WA), LPLC provides logic minimization and generates standard JEDEC-format fuse maps.

Macintosh as a Spice machine

Although digital simulation capabilities on the Macintosh are fairly limited, two implementations of Spice—the industry-standard analog circuit simulator from the University of California at Berkeley—are now available on the Macintosh. "I've done a lot of work with Spice over the years, and the Macintosh is a perfect Spice machine," says Jeff Deutsch, president of Deutsch Research. "The graphics are intuitive and easy to use. Someone who's never used Spice before can learn to use it easily."

Deutsch Research's MacSpice, which will be distributed by Capilano, is a full implementation of the Spice 3 standard. According to Deutsch, this version offers better speed, convergence and modeling capabilities than did earlier Spice versions. MacSpice was specifically designed for the Macintosh, and it uses the standard Macintosh user interface. But this $1,500 package (it will be available for $995 until Oct 1) doesn't include a model library, so users must either purchase a library or build their own.

Microsim's PSpice is an improved version of the Spice 2 standard that runs on IBM PC, VAX and Sun platforms. "Since we ported PSpice to the Macintosh, the Macintosh has been our most popular non-IBM-PC platform," says Microsim's Tuinenga. Because the Macintosh II includes a floating-point coprocessor, it was a natural for the PSpice port, and Tuinenga says that platform runs PSpice at about the same speed as a Sun-3 workstation.



Since being ported to Microsim's PSpice, the Macintosh II has been Microsim's most popular non-IBM-PC platform, claims Paul Tuinenga, executive vice-president of Microsim. According to Tuinenga, the Macintosh II runs PSpice, an improved version of the Spice 2 standard that also runs on VAX and Sun platforms, about as fast as a Sun-3 workstation. The Macintosh version of PSpice includes a library of approximately 250 devices.

Priced at $1,450, the Macintosh version of PSpice includes a library of approximately 250 devices. A $700 Probe option provides a graphical postprocessor. A Monte Carlo option and a parameter estimator are also available.

An analog circuit simulator from Spectrum Software (Sunnyvale, CA) has also been ported to the Macintosh. While not a Spice derivative, Spectrum's MicroCap II provides many of the same functions, including ac, dc, transient and Fourier analyses. This $895 program includes a schematic-entry capability and a library of 50 transistors.

A collection of specialized analysis programs are available on the Macintosh from BV Engineering (Riverside, CA). That company's Signal Processing Program, for example,

DESIGN AND DEVELOPMENT TOOLS

analyzes the impact of linear and nonlinear systems on user-specified, time-domain waveforms. Other programs can solve equations for filters, analyze ac and dc characteristics of passive and active circuits, and determine closed-loop system stability.

■ Laying out the boards

When the logical design of a board is complete, users can place and route boards on the Macintosh. Printed circuit board layout with automatic routing is available with the Douglas CAD/CAM system from Douglas Electronics (San Leandro, CA) and with several programs available from Vamp. Douglas provides an OEM version of Capilano's Design Works for schematic entry.

Douglas' $1,500 Professional Layout package provides interactive placement and accommodates user-definable grids, line widths and pad sizes. A $700 Autorouter option provides true multilayer routing, with up to 16 layers routed simultaneously. Dana Dotson, Douglas marketing manager, recommends a Macintosh II with 2 Mbytes of RAM for multilayer work, and suggests a 19-in. color monitor, available from several third-party suppliers.

The McCad PCB-1 program from Vamp is an interactive printed circuit board layout program that's not net-list-driven. The McCad PCB-ST program is net-list-driven, and it provides interactive placement and routing. Grids, line widths and pad sizes are user-definable, and a point-to-point router will automatically draw a route if two endpoints are defined.

The McCad Autorouter is a multilayer router than can handle up to 32 layers. "In essence, it offers 100 percent completion, and when it's done, it will show problem areas," says Vamp president John Soluk. "There will be a small percentage of routes that will be too close or will cross." Vamp offers all of its tools, including schematic entry, digital simulation and autorouting, in a bundled package called EDS-II for $1,695.

While most EDA tools on the Macintosh are low-end tools, the Ascyn logic-synthesis program from Algorithmic Systems (Braintree, MA) doesn't fit that distinction. With prices starting at $5,000, this program can automatically generate a gate-level net list for an ASIC from a high-level algorithmic input language. It works with a 2-micron gate array library from California Devices (Milpitas, CA). It's clear that if a tool as sophisticated as logic synthesis can work on the Macintosh, then almost any type of EDA tool should be appropriate for this increasingly popular platform. □

COMPUTERS AND SUBSYSTEMS

IBM forges on with 8514/A standard: But who wants it?

Tom Williams, Western Managing Editor

With the inexorable force of flowing lava, the 8514/A graphics standard oozes from the depths of IBM—regardless of whether the world wants it. The questions "Is it good? Is it appropriate?" pale next to the fact that it's there and third-party graphics hardware and software manufacturers are rallying to support it. They're also working to improve its performance and price.

Conceived by IBM as an option that would allow the high resolutions needed by CAD applications to run on its Personal System/2 family, the 8514/A offers 1,024×768 pixels at either 4 bits (16 colors) or 8 bits (256 colors) per pixel. The 8514/A chip set makes up a drawing processor that takes commands from the host CPU to update pixels in its frame buffer. This is a departure from earlier IBM graphics modes—Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA) and Video Graphics Array (VGA)—in which the host had direct access to the frame buffer's memory map.

In addition, the 8514 display specification has two modes: 1,024×768 pixels interlaced, and the VGA display mode of 640-×480-pixel noninterlaced scan. Although the 8514/A controller doesn't run VGA graphics software, it can input VGA signals via a special-feature connector and display them on a multiple-frequency monitor at the VGA resolutions.

> ***"Hardware compatibility—is it useful? Maybe, but probably not."***
>
> *—Walt Penny, Media Cybernetics*

■ ■ ■

IBM hasn't released specifications on its controller hardware but has published a document describing the Adapter Interface, or AI, the software interface to the 8514/A silicon. The AI is the interface to which IBM recommends all third-party software developers write their code. IBM's stance forces hardware and software developers who want 8514/A functionality to make an important decision: do they follow IBM's recommendation and write to the AI, or do some daring hardware companies try to reverse engineer the silicon so that software can be written directly to hardware registers? Additional issues revolving around 8514/A involve devising ways that let the earlier applications written to EGA and VGA work with 8514/A hardware and lowering the cost of high-resolution monitors needed to meet the display requirements.

■ Reverse engineering tempting

The question of writing directly to the hardware is probably the most crucial. Reverse engineering worked well with EGA and VGA, and a large number of companies are building boards using register-compatible chips supplied by five or six IC manufacturers. It appears tempting on the surface. "In all cases, you'll get better performance by writing to

the hardware," says Walt Penny, vice-president of engineering for Media Cybernetics (Silver Spring, MD), maker of a graphics toolkit called Halo, which has found wide acceptance on current graphics hardware. The only problem is that IBM has warned that it may change the silicon underlying the 8514/A AI at some time in the future, in which case software written to earlier silicon wouldn't work.

"IBM said that about everything—CGA, EGA and VGA," asserts Greg Reznick, director of marketing for Video Seven (Fremont, CA), whose company currently provides a VGA board using a register-compatible chip and is now developing an 8514/A chip set. Video Seven is banking on the assumption that IBM's warnings will turn out to be as empty as they've been in the past.

Others, however, aren't so sure. Media Cybernetics' Penny, for example, says that this time he's taking IBM seriously, noting that the Entry Systems Division—producers of PCs and PS/2s—has recently been more closely tied to the corporate center. And IBM's corporate tactic for dealing with plug-compatible manufacturers that are trying to emulate its hardware has been to keep changing the hardware.

Verticom (Sunnyvale, CA), which is readying a family of 8514/A-compatible products, is also being cautious. "We're probably at a point where the warning is going to go from a set of words to having some

F. Stephen Andes (center), president of Enertronics Research, discusses an image generated by the company's Aurora 1024 graphics board that implements the IBM 8514/A Adapter Interface (AI). Enertronics is circumventing the AI's limitations by writing its own hardware drivers for popular graphics interfaces.

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teeth in it," says Robert Dickenson, president and chief executive officer at Verticom.

AI has serious flaws

Despite disagreement over whether IBM will change the silicon underlying the 8514/A AI, just about everyone agrees that the AI as it currently stands is seriously wanting. Video Seven's Reznick calls it a "not-too-far-removed plotter driver." Indeed, while the 8514/A AI specification does include bit block transfer (bitblt) commands, it's heavily oriented toward line drawing and has quickly gained a reputation for being poor at large block transfers.

Furthermore, some criticize AI's lack of a full suite of graphics commands. "AI isn't full-featured," claims F. Stephen Andes, president of Enertronics Research (St. Louis, MO), producer of the Aurora 1024—one of the first 8514/A boards for the AT bus. "Even in CAD/CAM applications, we wish it had an arc routine and a circle routine." And Media Cybernetics' Penny, comparing the AI to Hitachi's HD 63484 advanced CRT controller and Intel's 82786, says, "The AI doesn't do a lot of the things that are native instructions in other graphics processors. We wrote the Halo toolkit to the AI because we had no choice."

Given such dissatisfaction with the features and functions of the AI, it's no wonder that third-party vendors are divided into two camps. One camp is trying to improve the AI while staying within the safe fold of interface compatibility. The other is striking out to reverse engineer and write directly to the hardware, the risks be damned. Indeed, Microsoft (Redmond, WA) itself has gotten the 8514/A hardware specifications from IBM. Its sole purpose is to write Windows and Presentation Manager drivers—*not* drivers for application programs—to the 8514/A silicon because the performance simply wasn't acceptable when the drivers were written to the AI.

But what happens if IBM does change the hardware? "The driver for Presentation Manager [and Windows] will have to change," says Verticom's Dickenson.

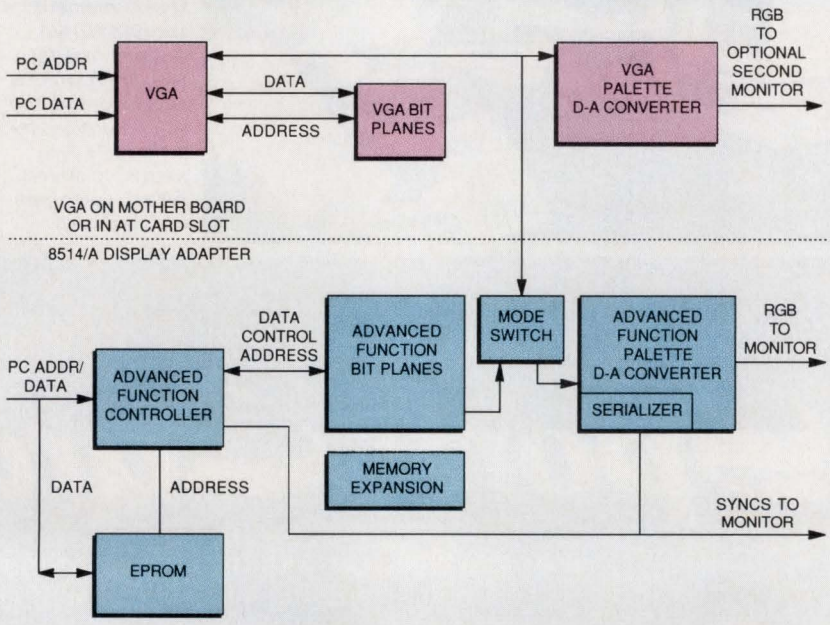
Video Seven, which claims to have successfully reverse engineered the 8514/A chip set, will be offering the specifications under nondisclosure to selected software companies so they can write both to IBM's present hardware and to Video Seven's yet unannounced hardware. This news hasn't exactly set off a chorus of cheers, however. "Can Reznick prove it's 100 percent compatible? It can't be 99 percent," cautions Kathleen Hunter, marketing communications director for Enertronics. And Media Cybernetics' Penny wonders, "Hardware compatibility—is it useful? Maybe, but probably not."

Working around compatibility

Graphics-based user environments, such as Windows and Presentation Manager, and toolkits for building graphics applications, such as Media Cybernetics' Halo, have already adapted to a lack of hardware compatibility. Media Cybernetics has written a version of Halo to the AI, but is also preparing a version that directly accesses not the 8514/A hardware but the TMS34010 graphics processor from Texas Instruments (Dallas, TX). This is significant because the initial third-party 8514/A products appearing on the market—such as the Aurora 1024 from Enertronics, the Cobra/2 from Vermont Microsystems (Winooski, VT) and the MX series from Verticom—implement a version of the AI but use the 34010 as the underlying hardware.

Large software vendors who provide system-level graphics environments such as Halo and Windows want to get as close to the hardware as possible because most application developers will want to use a toolkit of some kind rather than writing in terms of low-level graphics primitives. This makes it vital that such toolkits be as efficient as possible. Media Cybernetics, for example, worked hard to write Halo to the AI because there were certain things that Halo does that aren't directly supported by the AI's functions. These Halo operations had to be worked out by the CPU in terms of the limited AI command set rather

THE VGA-8514/A CONNECTION



The Video Graphics Array (VGA) either occupies its own IBM PC AT bus slot or, increasingly, is incorporated on the system mother board. In Personal System/2 systems, it's always on the mother board. A monitor attached to the 8514/A can display graphics from either the VGA or the 8514/A. If the VGA is being displayed on the 8514 display monitor, its palette contents are loaded into the 8514/A's palette via the mode switch. It's also possible to attach a lower resolution VGA monitor directly to the output of the VGA palette.

than by direct calls.

According to Penny, Media Cybernetics is also preparing a version of Halo that directly accesses the 34010 hardware, which would mean that applications written with the Halo toolkit could run on 8514/A boards based on the 34010 without having to go through the AI.

Even if software vendors cover both 8514/A and 34010 bases, hardware compatibility may win in the long run. For instance, Verticom has let it be known that while its initial hardware offerings will use the 34010, the company will be offering a higher performance version of its boards, which it will call the HX series. The HX series will incorporate the AI but will use proprietary VLSI—not a reverse-engineered 8514/A chip set—to carry out 8514/A functions. Verticom will supply drivers for Windows and several other programs written directly to this hardware, but will rely on both its AI implementation and its special chips to increase performance of other software applications written to the AI.

Adding 8514/A to the AT

IBM intended that the 8514/A display adapter be used only on its PS/2 line of computers with the Micro Channel bus. Third-party vendors are producing 8514/A display cards for both the Micro Channel and the AT bus. This clearly shows the intention of third-party vendors to preserve the ability of the installed base of 80286- and 80386-based, AT-bus machines to run graphics applications intended for the PS/2 and its OS/2 operating system.

But this raises a partitioning issue. The PS/2 implements VGA on its mother board, and future models are expected to have the 8514/A migrate to the mother board as well. And the newer versions of AT clones and 80386-based AT-type machines are beginning to show up with VGA on the mother board too. For such machines with VGA on the mother board, adding 8514/A capability is a matter of plugging in the card and cabling between the VGA feature connector on the mother board and the 8514/A card. The 8514/A card contains a mode switch that can pass VGA graphics through to the monitor, where they're displayed at 640-×480-pixel resolution.

For older machines, though, it will usually be necessary to take up two bus slots: one for the VGA card and one for the 8514/A. Enertronics offers an optional VGA card bundled with its Aurora 1024 for those who don't already have VGA. And Video Seven is looking at the possibility of a VGA daughter card that could attach to the 8514/A without taking an extra slot. Verticom's entry-level MX cards for the AT bus will include VGA

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capability on the card, but are viewed as transition products.

Another issue regarding the 8514/A is that of cost for the required high-resolution monitor. When one moves from 640-×480- to 1,024×768-pixel resolution, the price of the monitor needed for display takes a quantum jump from less than $1,000 to around $3,000. This price differential represents a barrier to wider acceptance of 8514/A, although there are indications that prices will soon come down. For this reason, says Vericom's Dickenson, "For the next 12 to 24 months, the high-resolution market is still a vertical one."

It's possible to use a multisynchronous monitor such as the NEC Multiscan with an 8514/A card and get the graphics performance it offers (a definite improvement over VGA) but at the VGA screen resolution. This may provide an impetus for the three-element feedback loop that Dickenson sees as essential for lowering prices: standards, software and low-cost monitors. "The critical thing for something being mainstream is that it has to be accepted as a standard, and then it feeds on itself," he says. Software developers have something to write to, and the existence of applications presents a market to which monitor manufacturers can sell at higher volumes and, hence, reduced unit prices.

"The 8514/A isn't the ideal controller for shading operations, and it's not very fast."

—George Krucik, Autodesk

■ ■ ■

Whatever criticism one may have of the 8514/A, it still represents a defined standard, if only because it comes from IBM. Large software vendors such as Autodesk (Sausalito, CA), which produces the AutoCAD drafting program, are supporting it, but they're also trying to influence IBM to extend the AI. "The 8514/A still isn't the ideal controller for shading operations, and in its current incarnation, it's not very fast," says George Krucik, manager of future development for Autodesk. But he adds that IBM has solicited comments from Autodesk about improving performance characteristics and may implement some of those suggestions.

The big question is, Will those improvements come in the form of extensions to the AI, changes in the silicon or both? Until an answer begins to emerge, the prudent software developer would do well to stick with the AI, for all its present faults. □

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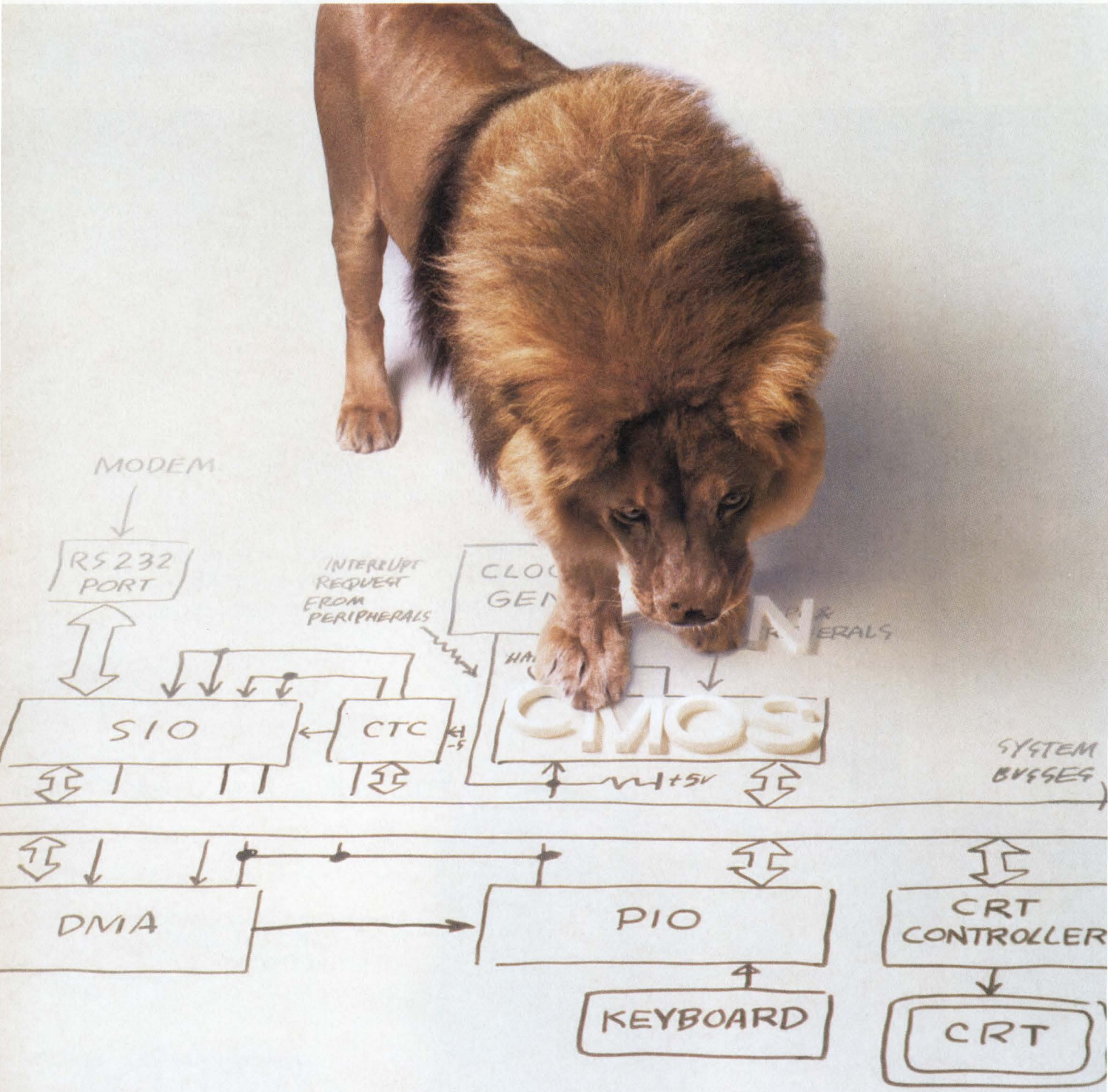

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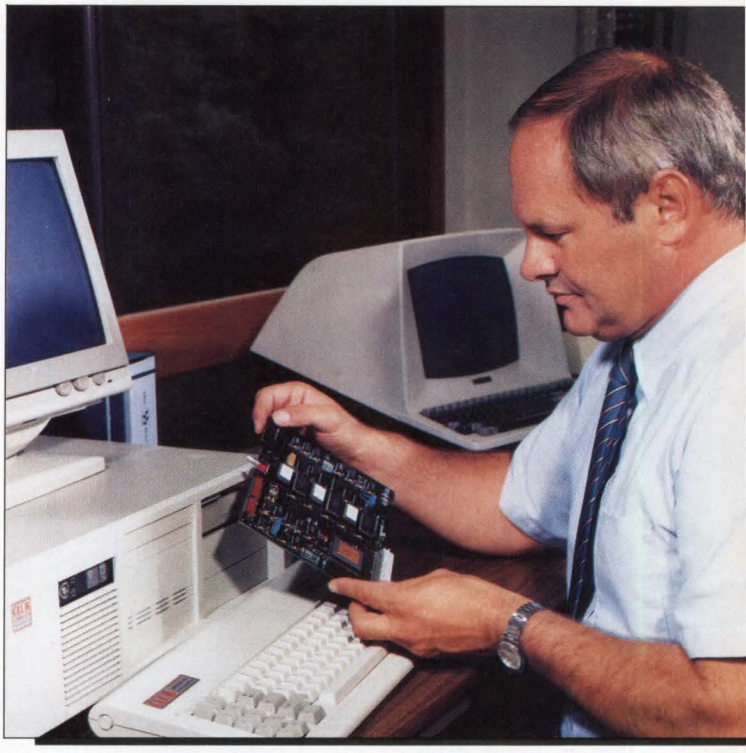
CIRCLE NO. 23

Sixteen-bit micros fortify their positions against 32-bit intruders

Marshalled against the assault of 32-bit chips, 16-bit microprocessors are relying on economy, performance and users' loyalty to hold their ground.

Ron Wilson
Senior Editor



The system designer's decision whether to stay with a 16-bit CPU or move to a 32-bit architecture is often made for the wrong reasons, according to Ed Rathje, vice-president of JMI Software. Since most senior engineering managers come from a hardware background, he says, decisions are often based strictly on hardware.

Most designers will agree that there's one fundamental reason to choose a 16-bit microprocessor over a 32-bit one: cost. But on closer examination, this single issue resolves into a wide variety of considerations, involving not just microprocessor price, but performance, total system cost, development expense and time to market.

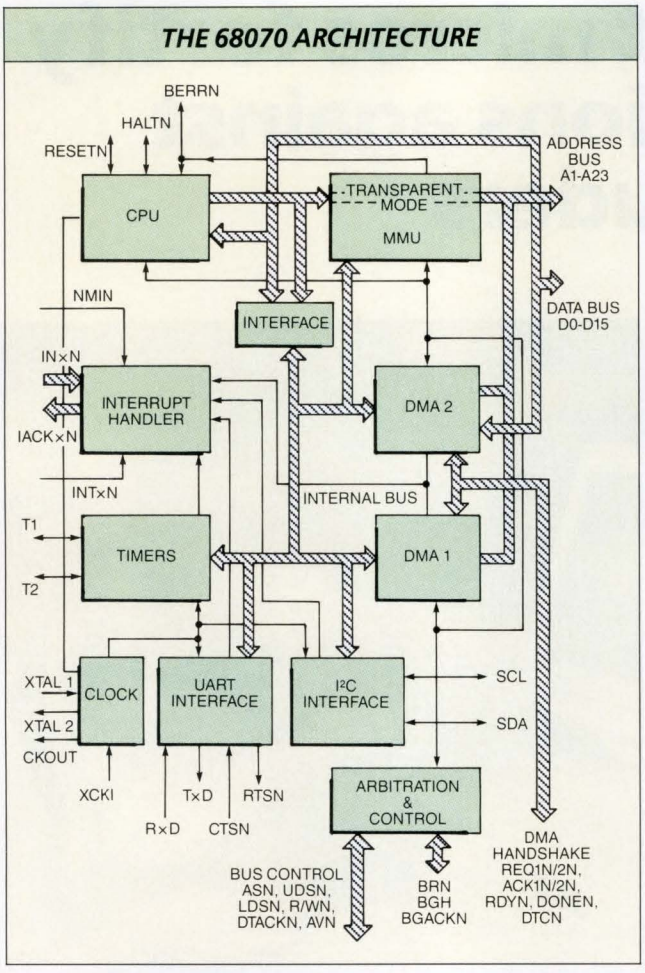
In the personal computing market, where the IBM PC AT's use of the 80286 and the Macintosh's reliance on the 68000 have made 16-bit processors the kings of the jungle, volumes are enormous. Consequently, a project's success depends much more on the cost of parts than on development or tool cost.

"Price is the biggest factor right now," says Glen Burchers, 286 marketing manager at Advanced Micro Devices (Sunnyvale, CA). "Customers are putting together 16-bit PCs with our 16-MHz 286 and running DOS or OS/2 as fast as a 16-MHz 386 would, but for $1,000 to $1,500 less." One reason for the big cost difference is the price of the CPU. "At the moment, the 16-MHz 286 is going for $127 in 100 quantities; in volume it's below $100," says Burchers. "We expect to see that price drop below $80 by the end of this year and below $50 by the end of 1989. The 386 hasn't been declining much. It started out at about $290 and is still selling at around $220."

Another reason for the cost advantage of 16-bit chips is the number of supporting chips they require. "Essentially, with a 32-bit chip you'll have twice as many components in the data path," points out Wayne Fischer, director of marketing at Force Computer (Campbell, CA). "Taking all those components into account, you can save from one-third to one-half the parts cost by staying with 16 bits."

A PC performance debate

While the cost advantage of a 16-bit PC implementation is quite clear, arguments rage over the relative performance of 16- and 32-bit PCs, at least within the IBM world. These arguments concern not so much the raw computing speed of the chips as the importance of speed to end-users.



CPU cores of 16-bit processors are small, leaving lots of room for expansion on the chip. The 68070 microprocessor from Signetics uses this extra real estate to augment its 68000-compatible CPU with a memory-management unit, a direct memory access controller, a timer and two types of serial interfaces. The chip includes most of the nonmemory hardware found on 68000 board-level computers.

"I know of no application where a 16-bit architecture can run faster than a 32-bit architecture if each is executing native code," says Burchers. "But on 286 code, a 16-MHz 286 runs somewhat faster than a 16-MHz 386." This seemingly unfair comparison is very much to the point, PC experts point out, because the bulk of PC software, including the new OS/2 operating system, is written in 8086 or 80286 instructions. There are very few packages written for the 386 architecture's more sophisticated instruction set.

"The reason for the 286 advantage is quite fundamental," says Walt Niewierski, product marketing manager for the 20-MHz 80C286 at Harris (Melbourne, FL). "Because of the additional memory management and housekeeping circuitry in the 386, the 32-bit chip requires more clock cycles to execute some instructions. So whether the 386 and the 286 are running at 16 MHz or 20 MHz, the 286 will run 16-bit code faster."

Some observers, though, argue that performance has to be more than a matter of execution speed. Intel (Santa Clara, CA), for instance, points to the growing body of applications code written specifically for the 386 that isn't executable on 16-bit architectures. The company's solution is the 80386SX—also called the P-9—a 386 processor with a 16-bit external bus, offering both 32-bit software compatibility and some of the economies of a 16-bit system.

But 16-bit chip vendors aren't quick to agree with Intel's point of view. "Yes, there will be 32-bit software out there in the future," says Burchers. "But users have to be careful. If you buy a 386 machine today, you may find that when the 32-bit software finally gets here, your 1988 PC won't have the performance—or the address range, if it's 80386SX-based—to run the stuff."

Henry Eng, V-series marketing manager at NEC Electronics (Mountain View, CA), is equally unwilling to assume a blanket replacement of 16-bit PCs. "A big part of this market doesn't need 32-bit machines," he says. "There's a fundamental split between the coming OS/2 environment—with its mainframe connectivity, elaborate multitasking and high cost—and the DOS world of the small-business user. The OS/2 environment is specifically for big corporate users who need to talk to mainframe computers and who can absorb the high cost of big memories and expensive software packages.

"After all," Eng continues, "most people aren't power users, and they don't need all the features of OS/2." This is the audience Eng identifies for NEC's new V-33 processor, the design of which seems to reflect the needs of these noncorporate PC users.

Architecturally, the V-33 lies midway between 8088 and 80286 CPUs. Like the V-30 before it, the V-33 supports the original 8086 instruction set without the 286's extensions and memory manager, making the chip incompatible with OS/2. But like the 286, the V-33 has nonmultiplexed 16-bit data buses and 24-bit address buses and is available in a 16-MHz version. And the chip also offers features beyond those of the 286.

"We speeded up instruction execution tremendously. It's four times faster than on the V-30," claims Eng. "One reason is that the instruction logic is hardwired, not microcoded. Another reason is that we've added hardware to speed up address generation. The V-33 generates effective addresses in one clock cycle, as compared to two cycles for the 286 and up to 12 cycles for the 8088."

All that hardware shows up in benchmarks, where NEC claims a Gibson benchmark result of 3.6 at 16 MHz, compared to 3 for the 16-MHz 286 and 0.5 for the 8-MHz 8088. Equally important for PC users who need large memory capacity, the V-33 supports the Lotus-Intel-Microsoft convention for extended memory, EMS 4.0, with on-chip hardware.

It seems evident that NEC focused the V-33 on the needs of demanding PC users who wouldn't be moving to OS/2. By doing so, the company defined a 16-bit market niche and tuned its architecture to defend the niche against 32-bit intruders.

■ The cost of an embedded CPU

In the embedded-computing market, cost is important but difficult to estimate because of the small manufacturing volumes of most embedded systems. Since relatively few units will be built—perhaps a few thousand a year for a few years—development

expense and tool costs can be at least as important as parts cost in the economics of a new product. To successfully defend their turf against 32-bit CPUs, 16-bit chips will have to prove their superiority in all three areas, and observers seem confident they'll do exactly that.

In controlling parts cost, the 16-bit chips have the advantage of a smaller CPU core. This leaves more room on the die for peripheral circuitry that might otherwise require extra packages and a greater design effort. The quintessential example of such a highly integrated 16-bit chip is Intel's 80186, which combines an 8086 CPU with many of the supporting chips found on 8086-based single-board computers, but on a single die. The on-chip features include a clock generator, two direct memory access channels, an interrupt controller, three 16-bit timers, chip-select logic and a wait-state generator.

Signetics (Sunnyvale, CA) has taken a similar approach to integration, but around a 68000 processor core, with its 68070 microprocessor. The chip contains a fully 68000-compatible CPU, a 68000-compatible bus interface and an array of peripheral modules similar to those of the 80186, but including RS-232 and high-speed serial interfaces.

Philip Bourekas, product marketing engineer for Signetics, sees the 68070 as part of a natural evolution in 16-bit architectures. "We see the 16-bit 68000 family members evolving away from their original home in the workstation market."

"There are a lot of advantages to the simplicity of 16-bit architectures."

—Walt Niewierski, Harris

■ ■ ■

Most suppliers of CPU chip sets also see the embedded market as fertile ground. But one of these suppliers, Vadem (San Jose, CA), has taken the unusual step of constructing chip sets around the already highly integrated CPUs.

"We really started out as a design company," says Paul Rosenfeld, Vadem's chief operating officer. "We did some work with the NEC V-40 and liked the chip, so we designed a chip set to support it.

"Starting with a highly integrated chip leads to a different partitioning than is typical in the PC market. You can use the devices already integrated into the processor, and that gives you both a real-estate and a performance advantage."

Having met with some success in its V-40 endeavor, Vadem is now preparing a chip set for the 16-MHz 80C186. "The chip set will make up a system compatible with the Personal System/2 Model 30," says Rosenfeld. "By using the on-chip functions in the 186, we get zero-wait-state access to some key peripherals. We'll support the extended memory EMS 4.0 spec, so a system can attach up to 32 Mbytes of memory."

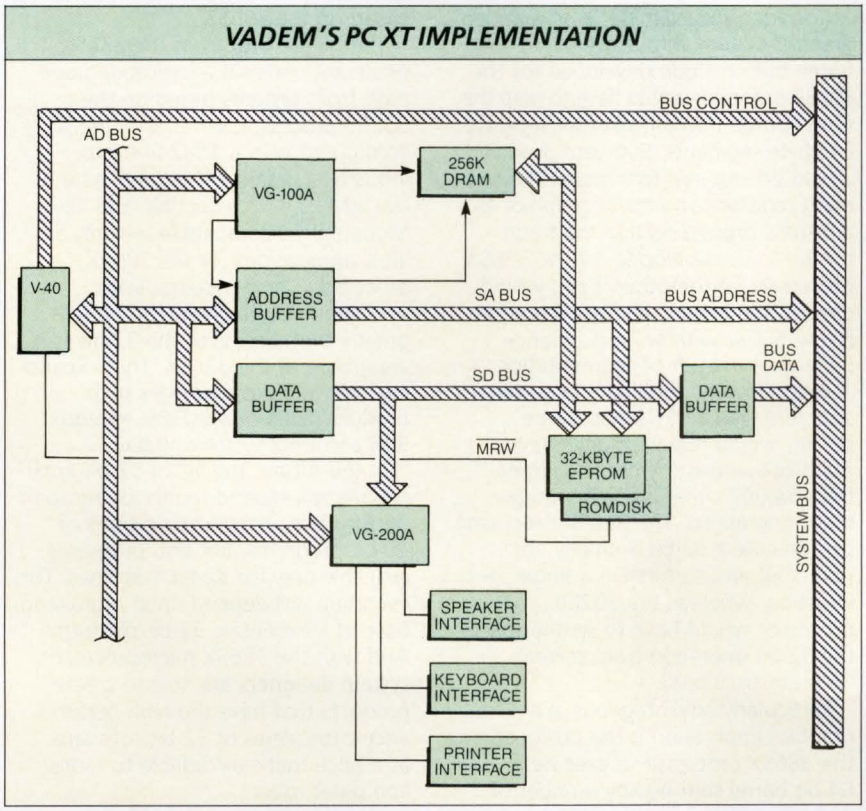
■ Development costs critical

In many low-volume applications, manufacturing cost will never be as significant as development cost in the financial analysis of a product. And in the struggle to manage engineering costs, there's both good news and bad news for 16-bit chips.

The good news comes from two characteristics in which the 16-bit chips excel: familiarity and simplicity. "One of the big advantages for a lot of our customers is their familiarity with the 68000 architecture," says Signetics' Bourekas.

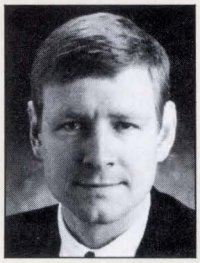
Randy Wilhelm, Intel's 16-bit focus group marketing manager, sees a similar trend for the 80C186. "We see a lot of designers migrating up from 8086 controllers," he says. "One of the big factors is the strong pull they feel from all the existing 8086 code they've developed."

Many observers also highly rate the 16-bit chips for their relative simplicity. "There are a lot of advantages to the simplicity of the 16-bit architectures. For example, the 286 in protected mode can be very effective in a real-time application with a lot of task switching. In that environment, it becomes clear that most of the 32-bit chips are more suited to data processing," says Harris' Niewierski. Intel's Wilhelm adds, "Even at the higher speeds like 16 MHz, where system cost between a 186 and an 80376 design might not be that different, the 186 may deliver a much simpler system design."



Vadem exploited the on-chip timers, interrupt controller and direct memory access logic of NEC's V-40 microprocessor in design of its IBM PC XT-compatible chip set. Using the on-chip facilities not only made access to these critical functions quicker, but also simplified the chip set and made room for a printer port.

A 32-bit micro tailored to 16-bit systems provides high performance at low cost



System designers inevitably face a trade-off between the performance and cost of the products they design. The 386SX microprocessor from Intel (Santa Clara, CA) provides the best of both worlds. It provides a 32-bit internal architecture for high performance and a 16-bit external data bus to facilitate low-cost system design.

The 16-bit bus of the 386SX processor facilitates a smaller, less-expensive system than a full 32-bit system. Fewer components such as buffers and transceivers are required. Furthermore, data paths are less narrow, resulting in fewer traces on the board. Overall, the board is smaller and often can be manufactured with fewer layers. Memory granularity is also smaller—that is, the minimum memory requirement of the system is smaller, and additional memory can be added to the system in smaller increments.

Surface-mount technology has become synonymous with low-cost system manufacturing. So the 386SX processor has been packaged in a surface-mountable, JEDEC-standard, 100-lead plastic quad flatpack (PQFP) package with 25-mil pin spacing. This package consumes very little system real estate and is optimized for low-cost, high-volume manufacturing.

Another important determinant of system cost is memory speed. The 386SX microprocessor is designed to interface easily with relatively slow and inexpensive memories. The address pipelining scheme of the 386SX lets a zero-wait-state page-mode and/or interleaved system be built with 100-ns dynamic RAMs.

This address pipelining scheme also lets the processor issue the memory address for the next bus cycle before the end of the current bus cycle, which effectively extends the memory access time of the memory subsystem. This facility provides a substantial system cost savings over other microprocessors that are in the same price and performance range and require expensive, high-speed memories, such as fast static RAMs, to avoid wait states.

■ Benefits of 32-bit architecture

The 32-bit programming architecture of the 386SX microprocessor provides three major benefits to software engineers. Most important, 32-bit code achieves high performance. Thirty-two-bit applications achieve performance that's two to five times greater than equivalent 16-bit applications running on the same system. Second, development of 32-bit software requires a smaller engineering investment than 16-bit software. Finally, 32-bit applications consume less code space than 16-bit applications.

The greater performance of the 32-bit 386SX processor over 16-bit processors like the 80286 is a result of its linear addressing capability and highly efficient 32-bit instruction/register set. Operations that are executed in one 32-bit instruction can take several 16-bit instructions to achieve the same result.

Consider, for example, a bit-mapped graphics system with a 256-kbyte-deep frame buffer. Code developed for the 80286 processor would have to map the frame buffer into at least four separate 64-kbyte segments. Software overhead would be required to manage the segment register contents as graphics algorithms process data in the frame buffer. Code developed for the 386SX processor, on the other hand, would directly and linearly address the entire frame buffer with no performance penalty as a result of segmentation.

Algorithms addressing a large data structure, like a 256-kbyte frame buffer, would require many integer math operations on integers larger than 64,000—that is, 32-bit integer math operations. The 386SX processor can execute a 32-bit multiply, addition, shift and so forth in a single instruction, whereas the 80286 processor would have to synthesize the 32-bit operation from several 16-bit instructions.

Particularly advantageous in a graphics application is the ability of the 386SX processor to execute a 64-bit barrel shift by any number of bits in three clock cycles. This capability leads to very high performance bit block transfers (bitblts) and other graphics primitives. The 80286, meanwhile, is limited to 16-bit shifts, each requiring up to 13 clock cycles.

■ Binary compatibility provided

Since the 386SX processor provides binary compatibility to the large installed base of 8086, 80186 and 80286 software, system developers have the option of preserving software investments from previous system products while providing enhanced performance and software capabilities in new systems. The Virtual 8086 Mode of the 386SX processor lets programs or even entire operating systems written for the 8086/80186 microprocessors be run as guests under new 32-bit operating systems developed for the 386 and 386SX processors. And since the 386SX processor's memory-management unit is a superset of the 80286's MMU, all 80286 software, including operating systems, is directly portable to systems based on the 386SX.

The 16-/24-bit bus of the 386SX processor makes it a logical upgrade path from systems based on the 80286 processor, which likewise is configured with a 16-/24-bit bus. Industry-standard computing systems like IBM PC AT-compatible and IBM Model 50/60-compatible systems are ideal applications for the 386SX processor. These systems, with 16-/24-bit I/O channels, can benefit greatly from access to the 32-bit software base of the 386SX. That expanding software base includes such products as Windows/386, Paradox 386 and Unix Systems V/386.

In the future, the list of 32-bit applications will expand to include not only performance-enhanced versions of 16-bit programs, but also programs available only for 32-bit machines. This evolution will depend upon a growing base of inexpensive 32-bit platforms. And with the 386SX microprocessor, system designers are able to create products that have the high-performance capabilities of 32-bit software at a price that's affordable to more computer users.

Bruce Schechter, BS, 386SX Microprocessor Product Manager, Microcomputer Division, Intel

But it's at the higher speeds that the bad news begins to show up for 16-bit economy and simplicity. "Memory speed—and cost—go up quickly with clock frequency," Wilhelm warns. "Technically, the 16-bit chips can stay with the 32-bit chips as clock frequencies go beyond 20 MHz. But in that performance range, we see most people moving to a 32-bit architecture like the 80376."

Niewierski notes that system complexity also increases with clock frequency. "At 20 MHz, you need caches to get maximum throughput out of a 286. And if you need floating-point hardware, you will also have to integrate a third-party floating-point unit; no 80287 can approach 20-MHz operation."

Harris offers a unique solution to this problem. Instead of trying to extend an existing 16-bit architecture beyond 20 MHz for higher performance, the company developed a new, Forth-executing, reduced-instruction-set-like 16-bit chip specifically for high-end embedded applications.

Dave Williams, Harris' RTX market development manager, believes that Harris' new RTX line offers the appropriate precision for most embedded applications, but without the performance limitations of conventional 16-bit architectures. "We're offering a simple chip, but an extraordinarily fast one," William claims. "In key performance specs, we're outperforming the 32-bit machines."

Software complexity an issue

As if growing hardware complexity weren't enough of a problem for high-end 16-bit designs, the chips must contend with growing software complexity as well. Traditionally, designers have fought software complexity by improving their language tools, which sometimes causes problems for 16-bit users. "The 16-bit chips just aren't as well-suited to compiled code as the new 32-bit architectures," says Intel's Wilhelm.

Other observers agree only to a point. "The biggest thing in looking at high-level languages for 16-bit chips is the problem of segmented addressing," says Ed Rathje, vice-president of JMI Software (Spring House, PA). While he feels that architectural suitability is primarily an issue for segmented-address chips rather than 16-bit chips per se, Rathje admits that, in general, the implementation of high-level languages may be better on the 32-bit chips.

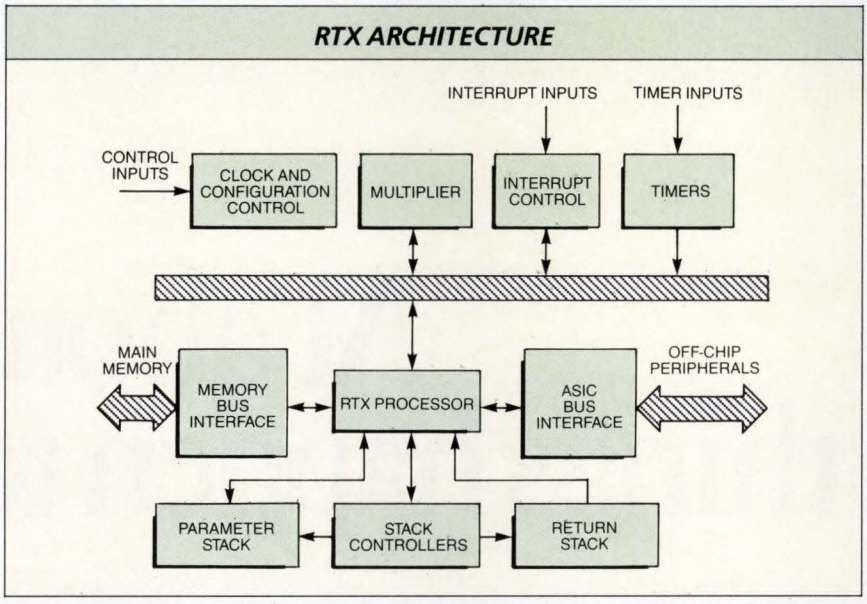
"Too often the decision of 16-bit vs. 32-bit is irrational," warns Rathje. "Most senior engineering management comes from a hardware background. These people tend to neglect software factors like language tools, operating systems and portability. They make a decision based strictly on the hardware."

As often as not, a hardware-based decision can lead to overkill. "People have been told that this faster device, in a newer technology that takes 32 bits at a time, is better for their job," says Harris' Niewierski. "But with the kind of performance we're seeing in 16-bit chips, that just isn't true for everybody."

One protection against a wrong decision is to reverse the decision process. By developing the bulk of the project code in a portable language like C—before the microprocessor is chosen—the design team can gain both a certain measure of architecture independence and an important decision-making tool.

"We're seeing a lot of applications that used to be in assembly code now written in C," says Force Computer's Fischer. "That gives the team the alternative of moving its code back and forth between 16- and 32-bit designs. It's no longer just a theory; portability is widely practiced."

JMI's Rathje agrees. "It makes sense these days to do a software prototype in C," he says. "Then you can identify some critical sections of code, extract them, and use them to benchmark several hardware configurations. It's a good investment to spend maybe $20,000 to make sure that you choose the right processor for a $500,000 project." Given the evident complexity of the decision, and the opportunity to save significant amounts of money by staying with 16-bit microprocessors whenever possible, that advice seems entirely reasonable. □



Harris chose to use silicon for speed, rather than backward compatibility, in developing the RTX 16-bit processor. Designed to directly execute Forth code, the processor offers 400-ns exception response, better than 10-Mips throughput and a specialized parallel bus intended for close integration of application-specific I/O subsystems.

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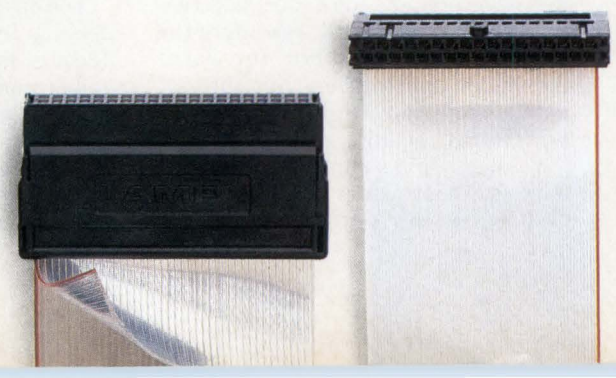

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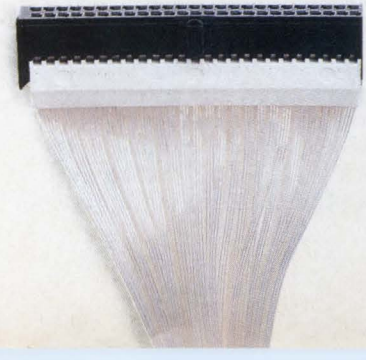


DSP applications ride the wave of floating-point processing

Warren Andrews, Contributing Editor

DSP technology is now where microprocessor technology was in the early 1970s. The scene is set for explosive growth, and much of it will be tied to the latest breed of floating-point chips.

Digital signal processing technology is branching out in two directions. For one, dramatic price reductions and the availability of powerful, single-chip DSP devices have let DSP technology invade the domain of analog signal processors as well as that of more conventional microcomputers and microcontrollers. DSP technology is now also moving upscale, exploring new frontiers in graphics, imaging, pattern recognition, instrumentation and scientific analysis.

At both the high and low ends of the performance spectrum, general-purpose, single-chip devices are making a significant impact on the design process. At the low end, prices for DSP chips have already dropped below the $5 level in volume, expanding their applications to include everything from consumer products, such as toys and automobiles, to price-sensitive commercial and industrial applications including motor servo control functions, personal computer modems and various telecommunications devices. In high-end applications, recent developments that have increased the performance and decreased the power dissipation of high-performance, single-chip devices now make them attractive alternatives to multichip, building-block solutions.

And there's an even brighter future on the horizon for DSP chips. Over the next twelve months, a number of new devices are expected to hit the market as second- and third-generation DSP chips emerge. In addition, new tools to aid the designer are beginning to surface from many third-party vendors as well as chip makers, including high-level language compilers, linkers, assemblers and emulators. In the immediate future, users can expect increasingly sophisticated software and even a DSP operating system.

Categories of DSP ICs vary

DSP ICs can be roughly divided into four categories: building-block circuits, application-specific ICs, algorithm-specific ICs and general-purpose DSPs. Building blocks are discrete chips that function as multipliers/accumulators, address generators and sequencers. While building-block solutions are the most costly DSPs in terms of printed circuit-board real estate, power dissipation, development time and programming difficulty, they offer advantages in both performance and flexibility. Discrete components such as multipliers/accumulators are now posting blazingly fast speeds. A recently introduced device from Integrated Device Technology (Santa Clara, CA), for example, boasts a 20-ns multiply/accumulate time.

Such discrete building-block approaches will continue to rule the leading performance edge of the industry in cases where designers have to squeeze every ounce of speed out of a system even if at the sacrifice of price, board space, design and programming ease. In addition, almost by definition, building-block designs provide a wide degree of flexibility in terms of being able to design a circuit to solve a particular function and of providing relatively easy, fast hardware modifications.

However, such mundane concerns as cost and board space are beginning to take their toll. Increasing pressures to cut power dissipation and reduce board space are illustrated by such designs as IBM's Personal System/2 family of computers. Add-on adapter cards in the PS/2 are only about half the size of their precursor PC AT-type boards, and power is restricted to only 1.6 W per slot.

DSP ASICs, which include both gate arrays and cell-based approaches, offer the designer a num-

The move to floating-point chips is being powered by steady improvements in performance and plunging prices. Cover by Sergio Roffo.

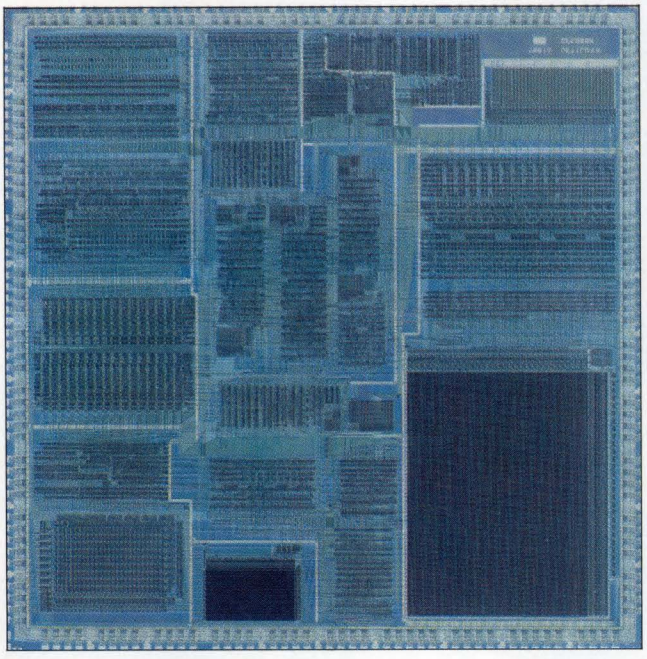
ber of advantages. Like building-block approaches, ASIC designs provide both performance and flexibility. In addition, they also provide significant reductions in board space and power dissipation over discrete ICs. At present, most DSP ASICs have to be constructed from relatively primitive building blocks, making their development both time-consuming and costly. Future development, however, may see complete DSP macrocells resident in many ASIC libraries, or as core elements diffused on gate arrays. This may turn the tables in favor of ASIC approaches for future high-volume applications. Also, DSP is very new to many application areas, and production volumes don't warrant ASIC approaches.

Algorithm-specific DSPs are a kind of extension of building-block approaches in that they perform specific DSP functions at blazingly fast speeds. Such chips are capable of delivering many times the performance of general-purpose devices for certain image-processing tasks, or when executing specific algorithms such as transforms, finite impulse response (FIR) or infinite-duration impulse response (IIR) filters. Such chips are so specialized, however, that they

can often be too application-specific. For example, two identical devices configured to execute the same algorithm won't perform equally in different applications. In fact, performance differences can be as great as two to four times.

More general-purpose DSPs

By far, the fastest growing segment of the DSP IC market is general-purpose DSPs. Since Texas Instruments (Houston, TX) started the single-chip, general-purpose DSP business with its TMS320 family, the industry has acquired a number of advocates, including AT&T Microelectronics (Berkeley Heights, NJ), Analog Devices (Norwood, MA), Motorola (Austin, TX), Fujitsu Microelectronics (Santa Clara, CA), NEC Microelectronics (Mountain View, CA), SGS Thomson (Phoenix, AZ) and Oki Semiconductor (Sunnyvale, CA).



Texas Instruments claims that its soon-to-be-released TMS 320C30 will be the most powerful and complex DSP ever made. Boasting a higher level of complexity than the Intel 80386, the 32-bit floating-point processor offers an instruction cycle of only 60 ns and a performance of 33 MFlops.

By far, TI holds the largest share of the single-chip DSP business, according to John Scarisbrick, the company's DSP department manager. Analysts confirm Scarisbrick's claim, noting that the company controls almost 70 percent of the market—six times the market share of its closest competitor. "Though most of the press attention is focused on the latest generation of 32-bit floating-point parts, almost all of the present production—and a great deal of design activity—is in the less dramatic, 16-bit fixed-point devices," says Scarisbrick.

Fixed-point DSP chips whip through integer mathematics at blazingly fast speeds. TI's latest generation part, the TMS320C25, for example, boasts an instruction cycle time of only 80 ns. But the fastest cycle time for a 16-bit, fixed-point DSP device is claimed by AT&T's DSP16. The DSP16 is available in speed versions of 75 ns and 55 ns, according to Kreg Ulery, DSP product engineer at AT&T. The part is currently undergoing some minor modifications and a die shrink from its 1-micron, double-level-metal, twin-tub CMOS process to a 0.75-micron process, adds Ulery.

In addition to the shrink, other modifications include quadrupling the on-chip RAM and increasing ROM. The new part, the DSP16A, is expected to have a cycle time of around 33 ns. The additional on-chip memory is required, explains Ulery, because at the ultrafast cycle times it's difficult to find memory fast enough to keep up with the processor.

While AT&T is stepping up the pace of its processor, unofficial word is that TI is doing exactly the same. According to sources at TI, the company will rework its TMS320C25 in a new submicron process in a program company insiders refer to as "Mosaic." TI is expected to announce the program later this year. The new part, which will probably surface sometime next year, will provide cycle times in the 25- to 35-ns range. In addition, there are hints that this part, like the announced AT&T part, will probably include other enhancements, such as additional memory. But cycle time alone may not be an accurate measurement of performance, according to David Fair, strategic marketing manager at Analog Devices. The company recently completed a die shrink of its ADSP2100 to a 1-micron CMOS process. The new version, the ADSP2100A, is the fastest general-purpose DSP available in production, according to Fair (in contradiction with AT&T's Ulery), though he says this status could change on practically a day-to-day basis. Instead of measuring performance in terms of cycle times, Fair measures performance in a benchmark where the device is running code, much like what would be used in an actual application.

DSPs lend themselves to a number of standard benchmarks, which reflect with a fair degree of accuracy how a device will perform in a system. The benchmark Fair believes to be one of the most useful and most universally accepted is the 1,024-point (often referred to as a 1k) fast Fourier transformation (FFT). The ADSP2100A whizzes through this benchmark in just under 3 ms—almost 2.5 times faster than TI's current-generation TMS320C25 and just slightly faster than Motorola's current-generation 24-bit processor, the 56000, which makes it through in 3.39 ms. Comparable benchmarks aren't available for AT&T's current-generation DSP16.

Efficiency more than cycle time

Designers often confuse cycle time with a processor's efficiency, says Fair. A number of factors, he explains, contribute to the efficiency of the ADSP2100. For one, it's the only chip that takes the Harvard architecture off-chip and uses a physical external instruction and data bus. The instruction bus goes to a program memory, which can contain either code or data. The chip can make two accesses to data in a single cycle. This compares with other approaches, such as that used by TI, in which a minimum of two cycles are required to transfer a single data bit. The I/O rate is 4:1, therefore, with that advantage alone.

In response to a need for lower system cost, Analog Devices recently introduced its ADSP2101 DSP chip. The company added on-chip memory to the ADSP2100 and multiplexed instruction and data ports to reduce package pin count. In addition, Ana-

log Devices added a pair of double-buffered serial ports as well as μ-law and a-law companding hardware.

Serial ports generally interrupt the processor when a full word is assembled either for receive or transmit, similar to the way a data-converter interrupt is treated. This requires a minimum of four instruction cycles just to service the interrupt, even if nothing is done. Even in the best conventional processor, each data point will take four data cycles to transfer a word in or out of a serial port. Analog Devices minimizes this delay through a type of cycle-stealing process called data autobuffering. When a word is ready to be transferred, a cycle is stolen, in turn letting the transfer occupy only a single cycle. On-chip data address generators are used to define the size of the buffer being transferred and to perform an interrupt at the end of the transfer.

24-bit DSP the middle ground

Motorola has taken a slightly different tact with its fixed-point DSP chip, the 56000. Instead of providing 16 bits, Motorola elected to provide 24 bits with a 56-bit accumulator. The company selected the format because 16 bits were too few for many applications, while 32 bits were overkill, says DSP major program manager Jane Bates. As an example, Bates cites digital audio, where 16-bit machines don't provide the necessary dynamic range, but 32-bit chips unnecessarily increase the price in a cost-sensitive application area.

Like others in the single-chip DSP race, Motorola also announced a second version of its device almost as soon as the first version reached

"While there are exceptions, there's a general trend toward single-chip, floating-point devices."

—Kreg Ulery, AT&T Microelectronics

production. Its initial 56001 offers a clock speed of 20.5 MHz, translating to 10.25 Mips with a 97.5-ns instruction cycle. The latest version, the 56000/1, with a shrink from 1.5 to 1.2 microns, will boost performance to 27 MHz (74.1-ns instruction cycle). Typical power dissipation of well under 0.5 W makes the 56000/1 one of the most, if not the most, power-stingy chips on the market, says Bates.

The combination of the wider word (24 bits vs. 16 bits) plus other internal resources also makes the 56000 one of the fastest devices of its type, explains Bates. Its powerful instruction set permits almost two times the performance of the TMS320C25, for example, with approximately one-half the programming code.

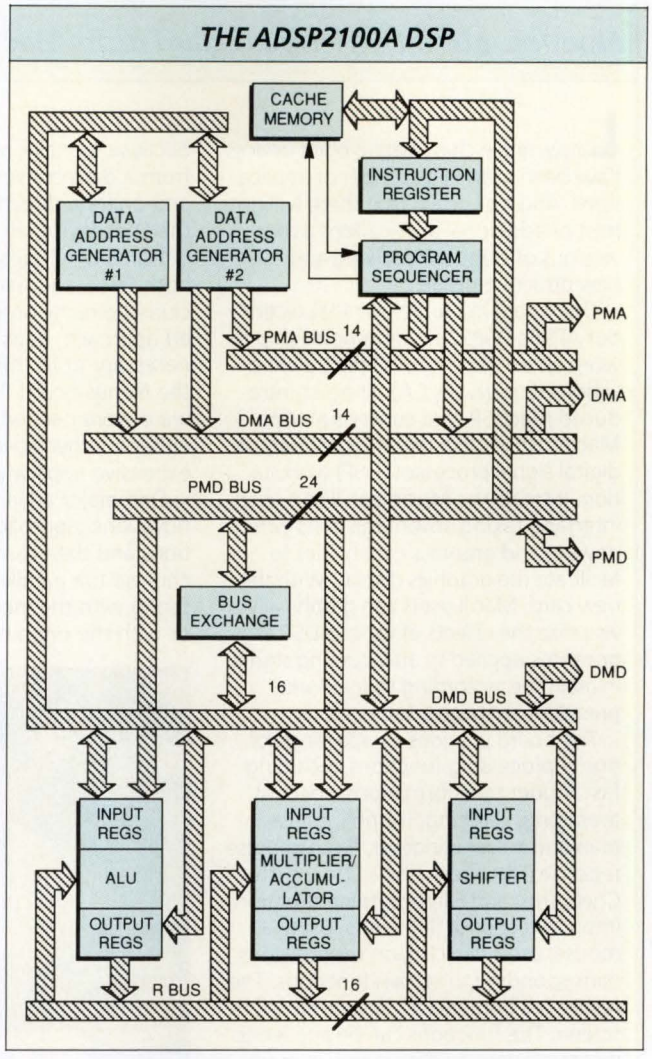
A recent development in packaging at Motorola is aimed at reducing the price of its 56000 family. The single-layer aluminized metal (SLAM) package is made of a ceramic substrate with a deposited gold pin-out pattern. The chip is bonded onto the ceramic substrate and wire-bonded to the gold conductors.

The SLAM-packaged die fits into a through-hole pinned socket that mounts directly to a printed circuit board. The size of the packaged die is too large for many surface-mount applications, thus normally calling for more expensive pin-grid array (PGA) packages. The company is able to greatly reduce the cost of the chip because the package cost itself is significantly less than that of a conventional PGA. Testing time is reduced because of the new package, and damage to the pins during insertion and release is minimized. This new packaging has permitted Motorola to lower the price of the 56001 from $125 for the PGA version to $56 for the SLAM package. Although the cost of the socket is under $5, it's expected to drop to under $2 next year.

Floating-point DSPs on the way

While fixed-point DSP chips now own the market, manufacturers are just starting to get into gear with floating-point devices. "While there are many exceptions, there's a general trend toward single-chip, floating-point devices," says AT&T's Ulery. Compared with integer or fixed-point

Taking the Harvard architecture off-chip is one of the keys to the top-level performance of the ADSP2100A from Analog Devices. Capable of whizzing through a 1k fast Fourier transformation in under 3 ms, the company claims to have the fastest DSP chip currently in production. In addition, μ-law and a-law companding hardware is on-chip to further speed many telecom operations.



Floating-point DSP Nubus board turns Mac II into real-time workstation

Lately, single-chip floating-point devices have been used in a number of applications. And it's certain that there will be a host of additional applications as early versions of chips are updated and as new devices emerge.

One board manufacturer that recently put AT&T's DSP32 floating-point chip to work on a Nubus card is Spectral Innovations (Sunnyvale, CA). The just-introduced MacDSP card converts an Apple Macintosh II into a real-time, interactive digital signal processor (DSP) workstation. It treats the Macintosh II as a user interface, taking advantage of its windowing and graphics capabilities to facilitate the graphics display. With the new card, Mac II users can graphically visualize the effects of various DSP algorithms applied to an incoming signal in real time, according to Joe Burke, president at Spectral Innovations.

The board provides a wide range of signal-processing functions, including fast Fourier transformations; spectral averaging; Hanning, Hamming, Blackman and Kaiser windows; finite impulse reponse (FIR) filters; and Butterworth, Chebyshev and Elliptic infinite-duration impulse response (IIR) filters. Using a mouse, users can click on various icons corresponding to certain functions. The results are immediately displayed on the screen. The functions can be applied to incoming data, to data stored in main memory (up to 800 ksamples/s) or to data that's been captured on disk (up to 70 ksamples/s).

■ Multiported approach is key

Burke credits the single-chip DSP used by Spectral Innovations as being a key element in packing all the functions on a single card with the real-time performance. "The processor we selected has to do a number of things. It must support data acquisition, execute the implemented signal-processing algorithms and provide graphics processing," he says. The system is designed to bring in raw data, process it, display the results in real time (that is, at a video rate so there are no perceivable jumps in the image) and update the image 30 times each second.

"We selected the AT&T floating-point processor is because it offers three direct memory access ports, an input DMA port, a parallel port and an output DMA port," Burke. "This multiported approach is critical in our application because we take raw data in directly from a data converter in serial format and operate directly on that data in the DSP device, all without any external circuitry. That's possible because both DMA and handshake logic are included directly on-chip." A multiported approach, adds Burke, is also necessary to fit the entire system on the Nubus board. If additional hardware were needed, it would require either a larger board or prohibitively expensive application-specific ICs.

One major advantage of Spectral Innovations' approach is that instructions and data can be loaded into the chip via the parallel port without interfering with the incoming data stream, or with the ongoing processing. This

Spectral Innovations found that the multiported approach of AT&T's DSP32 floating-point chip was necessary in order to be able to fit its entire MacDSP system on the Nubus board, according to Joe Burke, president.

lets the system provide a workstation environment, one that calls for both fast throughput and lots of control of the signal processor.

Another benefit of the DSP32, says Burke, is its large, 64-kbyte programming space, since both the on-board and off-board RAM are completely accessible by any program. This ample programming space permits a complete algorithm with all functions (windowing, filtering, transforms, convolutions and other DSP functions) to be loaded into the memory at one time. Once loaded, the parallel port is free to control the processor while it simultaneously takes data in through one serial port, processes it and sends it out through the second serial port.

With enough memory space, according to Burke, it's possible to let data be collected in memory, use the program to operate on that data and let it out from the serial output port. At the same time, the parallel port can be used to examine the data just processed. Data being passed through the chip can be displayed without interrupting the processor throughput.

Other chips with only a single serial port and a single parallel port have time gaps between data being input, processed and output. In addition, in these other chips, data must be output in two modes, according to Burke. And to display the data, it must first be rasterized, or perform a number of operations so that it fits within the pixel boundaries of the screen. Then, other algorithms must also be performed on the data before it can exit to an audio port.

With the full 64-kbyte address space, however, the DSP32 chip can buffer a number of data samples and write the operating parameters into the software. This pipelined process lets the main code shell run the same regardless of the settings on the Macintosh controller. The system can operate on 32 data samples just as quickly and easily as it can handle 4-kbyte samples. Without the large available memory space, other processors would have to take in smaller amounts of data, process it and then put it aside whenever they brought in another sample. The processors would subsequently have to reassemble the samples into a larger unit, which takes time and reduces the integrity of the display.

Spectral Innovations' board performs quite a few operations on the data. It can window it, filter it, run off a spectrum of it, save a linear representation and a log representation of the spectrum, and save both real and imaginary parts of the spectrum. With the chip's large memory space, for example, it's possible to build up graphics buffers to perform various tasks, such as graphics operations on the time data.

The same functions are repeated for the time data, the windowed output, the filtered output and the transform output, leaving a lot of graphics buffers inside the memory space each time data is collected. As a result, each time

a user selects between a time and a frequency mode, the data has already been calculated and can be instantly downloaded to the host for display.

Without that capability, the device would have to be reprogrammed and would have to recalculate new graphics vectors and processing steps each time the mode was switched. Not only would the response be slowed, but programming complexity would increase because the program would have to be multimode. In the case of Spectral Innovations' processor, only a single program resides in memory, and it's simply a matter of looking at a different address areas of the memory to get the different display.

Floating point vs. fixed point

A significant advantage in comparing floating- and fixed-point processors has to do with the amount of code space available, according to Burke. Using the floating-point device, code can be compacted. In fact, it was possible to squeeze all of Spectral's program code into the chip's on-board RAM, according to Burke. Fixed-point, in comparison, would use considerably more code to implement the same operations. A simple FFT, for example, requires almost three times the amount of code as the same operation performed in floating point.

The FFT has a lot of gain on the signal, and it's easy to quickly go beyond the fixed-point boundaries. Users with frequent operations must adjust data so it doesn't overflow. As the signal increases in frequency, more code must be added to do all the overflow checking.

Fixed-point operations also make it very difficult to write FFT algorithms for very large transforms. For example, in a fixed-point operation it's much more difficult to write a 1,000-point FFT algorithm than it is to write a 128-bit algorithm. The longer the transform, the more checking must be done for overflow. With the floating-point chip, very generic software can thus be used regardless of which mode the MacDSP is running.

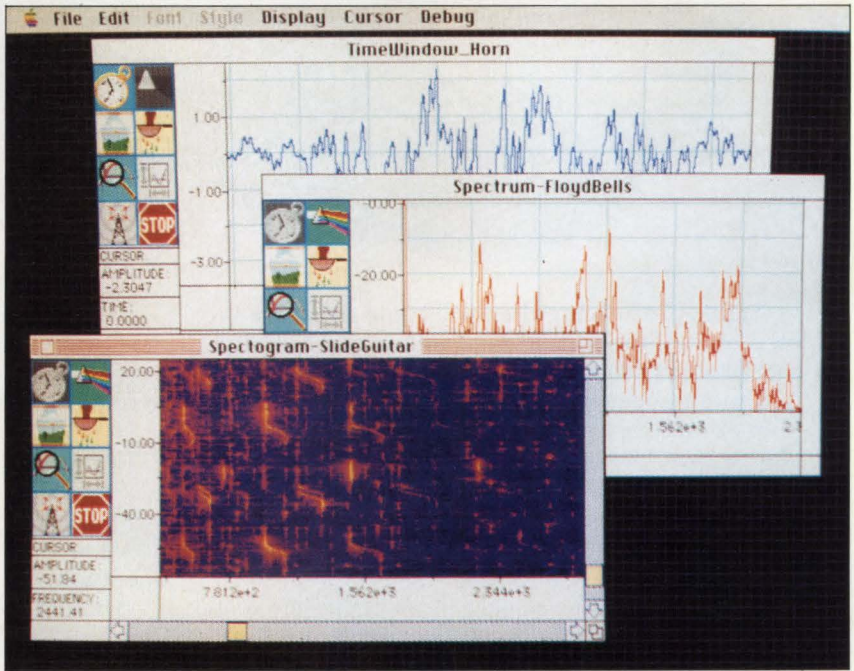
The byte-operation capability of the DSP32 also played a significant role in Spectral Innovations' selection of the chip. Working with graphics on a color screen is a byte-oriented task, as opposed to monochrome, which is frequently bit-oriented. Using the byte operations on the DSP32, it's possible to quickly and easily compress all the floating-point results into byte results and pack them into a pixel map. Such manipulations save memory space once the processor reduces the result to a byte structure.

When the DSP32C becomes available, says Burke, its larger, 16-Mbyte address space will further simplify design. The entire pixel map can then be performed in the processor, stored in the memory space and, when required, transferred directly to the screen. Using the memory space as specified, the processor can be used as a graphics driver for the screen as well as a signal-processing device, permitting much faster updates to the screen. The expanded memory will let images be built in the device memory, instead of building part of them in the processor and having to transfer them to the host (Macintosh) for completion.

Quick retrieval of data essential

Processing data is only one aspect of the function of a DSP device. According to Burke, getting the data out of the device is equally important. "Something that people don't think too much about when considering the selection of a DSP device is how information is input and output from the chip," says Burke. "Looking at a spec sheet, a designer's interest is often focused more on performance—cycle time or MFlops—than on other factors. But those numbers are meaningless unless it's possible to get the data out of the device fast enough."

A 1-kbyte transform, for example, results in an answer with some real and imaginary parts in some kind of floating-point format. Most people don't realize that quite a few operations have to follow the transform in order to use the data. These operations include such things as a magnitude square, a logarithmic algorithm to compress the data for display purposes, and a procedure to scale the data so it can be plotted on a screen. Such functions take a significant amount of time—and a lot of number crunching. A more accurate spec for a DSP device, concludes Burke, would be a throughput rate—rather than a cycle time—or such benchmarks as a 1-kbyte transform time.



The MacDSP board from Spectral Innovations uses AT&T's DSP32 floating-point chip to turn the Macintosh II into a DSP workstation. By selecting an icon on the screen, users can view the effect of different algorithms on an incoming signal in real time. Because the entire program is resident within the DSP's address space, switching requires only pointing to a different address space.

This chip enabled us to process signals of the past.

The Rosetta Stone, discovered in 1799, was the key to deciphering the hieroglyphics that had been incomprehensible for centuries.

Signal processing, when you come right down to it, is multiplication, addition, subtraction and storage. Doesn't sound very exciting.

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chips, floating-point devices provide a far greater dynamic range, simpler programming and greater resolution.

Because of the difference in complexity, fixed-point devices will always be faster, guaranteeing them a place in the spotlight for a long time to come. And often applications simply don't call for anything more than fixed-point processing.

Cost, economy of scale, and nonrecurring engineering expense considerations are crucial factors in selecting DSP chips. In very high volume applications, manufacturers can benefit by spending additional time and effort up front to achieve the lowest component cost. In many cases, this may call for additional programming effort and time in order to make a fixed-point chip perform the necessary functions.

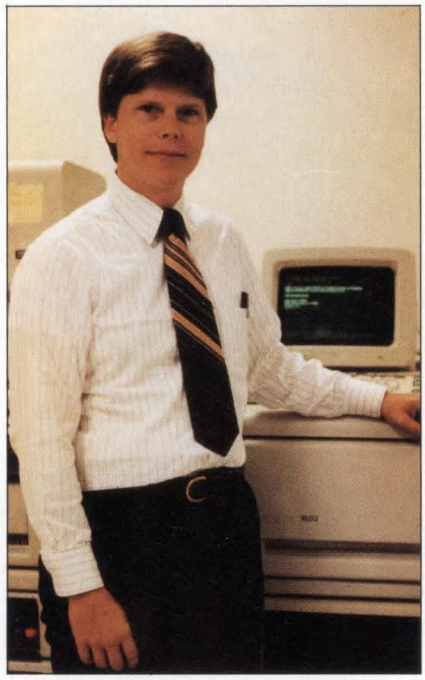
In lower volume applications of perhaps a few thousand systems per year, Scarisbrick suggests that floating-point approaches may well be warranted. While they're more expensive (floating-point chips are running relatively high in price and will probably always command at least twice the price of fixed-point in terms of hardware cost), they can offer significant savings in up-front programming and low-volume assembly costs. Other considerations when selecting DSP chips include available board space, time to market, power dissipation and, of course, function.

NEC entered the floating-point DSP market with its 32-bit μPD77230, which boasts a 150-ns cycle time. There are many functions that can't be done using fixed-point arithmetic, according to NEC's DSP hardware development engineer, Alvin Linell. In the absence of floating-point chips, certain routines must be discarded and more cumbersome code can be written to accommodate the fixed-point devices on hand. This frequently not only results in costly and time-consuming programming, but also chews up processing time, thus eroding the speed advantages of many high-performance devices.

First 32-bit floating-point DSP

AT&T was the first to reach the market with a commercial 32-bit floating point part, the DSP32, which still remains one of the only devices in volume production. The device was developed and first released internally at AT&T in January of 1985. In the fall of 1986, the company went commercial with it, becoming the first to offer a production part. The time delay, according to Ulery, was the result of AT&T management's reluctance to bring a commercial chip to market without the proper support.

DSP devices, unlike other standard ICs, require significant customer hand-holding, according to Ulery, so the company held off introduction until such support was in place. However, the DSP32 has been widely used within AT&T since its development, in such products as its 5ESS digital switch. The DSP32's solo slot will soon be challenged, however, since TI, Motorola, Fujitsu, NEC and others have announced new products, some of which are already in the sampling stage with volume production imminent.



Cycle time alone may not be an accurate measure of performance, according to David Fair, strategic marketing manager at Analog Devices. The company recently completed a die shrink of its ADSP2100 to a 1-micron CMOS process. Fair claims that the new ADSP2100A is the fastest general-purpose DSP now available in production.

The DSP32 is fabricated in 1.5-micron, depletion-mode NMOS with 250- and 160-ns cycle-time versions. Though relatively slow compared with the proposed introductions from other manufacturers, the DSP32 offers a number of features that make it ideal for certain applications.

In addition, according to Ulery, AT&T will soon release a faster, CMOS version of the chip, the DSP32C. Fabricated in a 0.75-micron CMOS process, the new chip will increase memory addressing from 16 to 24 bits and will provide a number of features requested by DSP32 users. Cycle time for the improved, CMOS version of the chip is expected to be 80 ns.

One novel feature of the DSP32 is that the memory can be used for either program or data; it doesn't have a strictly defined program or data section. There's a separate parallel port on-chip that lets one program load via DMA into the address space while the chip is still executing another program. This feature is used to dynamically download a different application while the first application is still running (see "Floating-point DSP Nubus board turns Mac II into real-time workstation" on page 54), permitting close to real-time context switching.

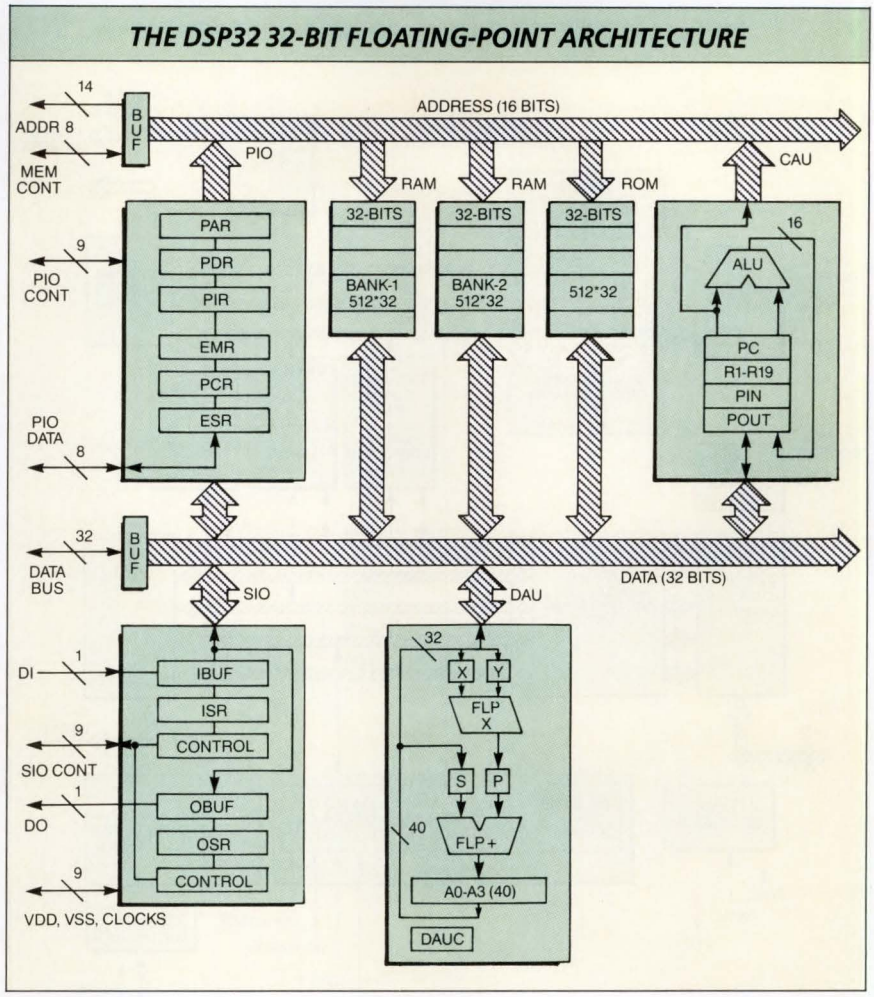
Another feature of the DSP32 that's preserved on the DSP32C is the byte-addressable address space, which makes it unnecessary to waste a complete 32-bit location to store an 8-bit pixel value or, in telecommunications, an 8-bit word as used in companded μ-law or a-law calculations. The byte addressability can be of particular importance in graphics applications and image processing where images can be processed, stored and then retrieved one pixel at a time.

Enhancements in DSP32C

In addition to having a larger address space than that of the DSP32, the DSP32C's memory interface is further enhanced by a flexible wait-state mechanism permitting the chip to talk to slower memory. The typical way to do a wait state on a DSP is to add an entire instruction cycle to the normal memory access time for each wait state. For example, in the case of a conventional DSP chip, the memory access time might be 35 ns while the instruction cycle time might be 100 ns. Thus, the access time would run 135 ns for memory that needed only slightly more than the 35-ns access. In the DSP32C, wait states are segmented into one-quarter of a cycle. A single wait state of the DSP32C, therefore, is only 20 ns (80 ns total cycle time). Wait states can be incremented in quarters of an instruction cycle.

Another modification to the DSP32 that AT&T developed as a result of customers' needs and incorporated into the DSP32C is the ability to use more than one type of external mem-

Two serial ports, one parallel port, a 64-kbyte program/address space and byte addressability give AT&T's DSP32 the flexibility to provide a number of real-time DSP solutions. A second generation in CMOS will offer a number of additional benefits, including a 24-bit (16-Mbyte) address space and a more flexible memory-addressing scheme.



ory. The DSP32C was designed with two independent speed partitions, so it's possible to run part of the memory very fast, while running other parts of the memory at a much slower rate. This is advantageous in programs where speed is critical for most of the program, but where there's some data that's only accessed every few instructions. In such a case, adding wait states to the regular program execution could drop throughput below acceptable levels. However, adding one or two wait states only every few instructions doesn't cause any major performance problems and permits the use of slower, less expensive memory.

The DSP32C is also improved in the way it handles interrupts. In real-time environments, there's a need to interrupt the device as quickly as possible, to process the interrupt, and to get back to the main program with as little loss of time as possible. There's no time for long context switches, which require the processor to save all the accumulators, registers and other values separately, then process the interrupt and restore the information again.

With the DSP32C interrupt, the state of the data-arithmetic unit, the accumulators, the multiplier inputs, the product register, all the flags and any other critical information is automatically saved when going into an interrupt-service routine. This doesn't happen sequentially, but in parallel. The overhead latency to get into the interrupt-service routine is only two instruction cycles. Getting back into the main program requires only a single cycle, making the context switch transparent to the operation. In a conventional processor, a single register is usually saved per instruction cycle, which makes getting into and out of interrupt routines a major time-consuming project.

Competition on the way

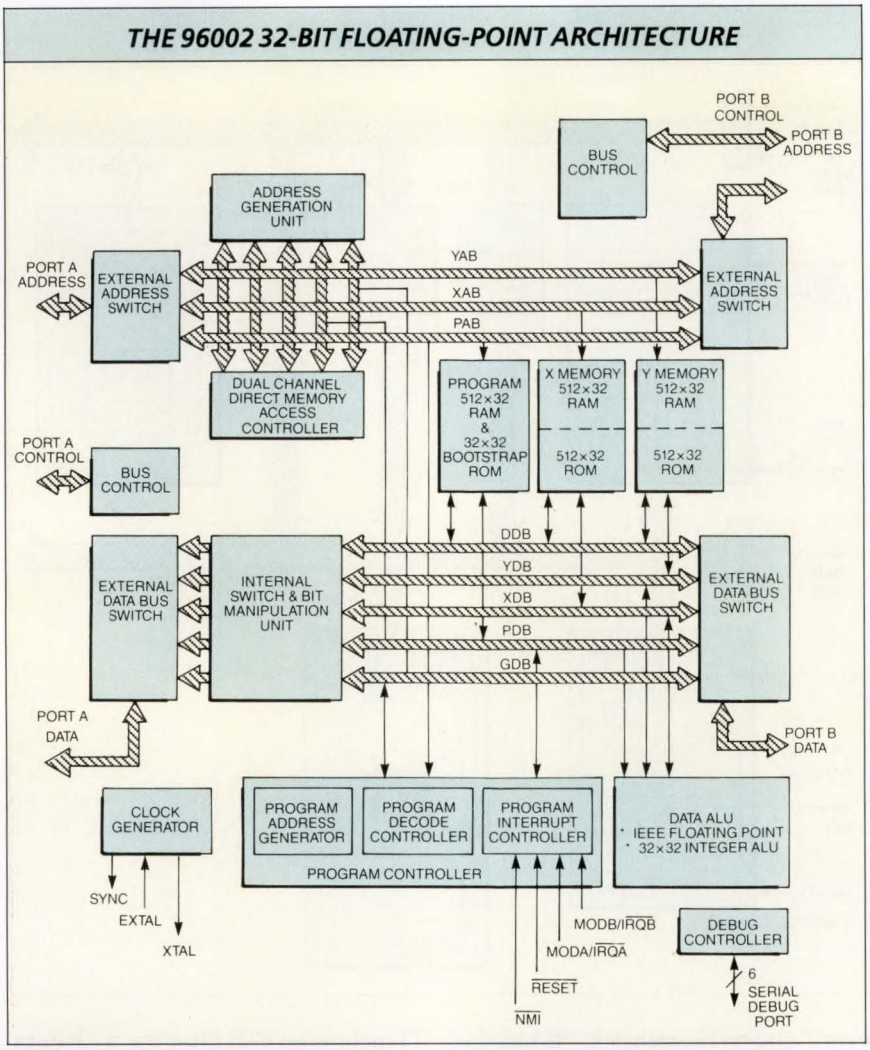
The 320C30, TI's flagship DSP product, "is unequivocally the highest performance DSP, or for that matter microprocessor or microcomputer, ever," claims Scarisbrick. "It has the highest integration level of any existing processor, and is considerably more complex than an Intel 80386." TI has been sampling the part for some time now and will be moving very rapidly into volume production.

TI's 320C30 has 33-MFlops performance, which translates into a 60-ns cycle time. Key features of TI's 320C30 include a pair of 1k×32-bit single-cycle, dual-access RAM blocks, a 4k×32-bit, single-cycle dual-access ROM block, a 64-×32-bit instruction cache, 32-bit instructions and data words, a 24-bit address space, a 32- to 40-bit floating-point integer multiplier, a 32-to 40-bit floating-point integer, a logical arithmetic logic unit, eight extended precision registers, a pair of 32-bit address generators with eight auxiliary registers, and an on-chip DMA controller for concurrent I/O and CPU operation.

Fabricated in a 1-micron CMOS process, the 320C30 gets through the 1,024 FFT benchmark in only 1.67 ms. Other benchmarks released by TI include an FIR filter tap with data shift in 60 ns and a cascaded IIR biquad filter element with five coefficients, which can be performed in only 360 ns.

Regardless of the performance of the 320C30 and TI's major share of the market, the company is unlikely to rest on its laurels. The rumor among TI insiders is that a fourth-generation DSP (a 320C40 perhaps?) will be disclosed sometime early next year. A shrink to submicron geometries (in the 0.8- to 0.9-micron area) will dramatically increase speed. Word has it that the advanced part will be targeted at applications in systems that call for performance somewhere in the 100-MFlops to 1-GFlops range. While geared for real-time, high-speed applications, sources indicate the chip will have explicit support for both double-precision and IEEE-formatted mathematics.

Fujitsu also has plans to introduce a pair of floating-point DSP devices, one a 24-bit device aimed at price-sensitive applications and the other



Motorola's 96002 32-bit floating-point DSP will include a pair of buses to facilitate anything from graphics processing to a dual-port memory interface. Samples of the 80-ns CMOS part are expected by mid-1989, with production parts to follow.

a 32-bit device aimed at high-performance applications. The 24-bit MB86220 is expected out any day, according to John Reimer, Fujitsu's manager of microcomputer and communications products. It's expected to provide an 80-ns cycle time resulting in about 12.5-Mips operation. The 32-bit MB86232 will boast a 75-ns cycle time and feature concurrent execution of ALU and transfer operations. The MB86232 offers three data formats, floating point (24-bit mantissa, 8-bit exponent), integer (24-bit without sign) and fixed point (32-bit 2's complement).

Fujitsu's 24-bit part, aimed at cost-sensitive applications, will carry a price tag of only about $30. Somewhat intimidated by TI's overwhelming dominance of the DSP market, Fujitsu is attempting to position both parts as microcontrollers rather than strictly DSP devices, according to Reimer. "We're trying to position our products as being able to do much more than standard DSP functions," he says. "Clearly TI has a stake in the ground, and by positioning the parts as reduced-instruction-set-type processors, we may get people to look at our parts who are currently looking at microcontrollers. Manufacturers of RISC machines are looking at doing stripped-down versions of their processors for embedded microcontroller applications. We're starting to see an overlap of the capabilities of those processors with those of DSP devices." Perhaps TI's Scarisbrick sums it up best by pointing out that a DSP device is, after all, nothing more than a highly efficient, well-tuned RISC processor.

Reimer's view of the overlap of microcontrollers and DSPs isn't unique. Already, many DSP devices are widely used in various controller applications. Some DSP applications, on the other hand, have been swallowed up by more conventional high-performance microcontroller products, according to Dave Whetstone, director of microcontroller marketing at National Semiconductor (Sunnyvale, CA).

Many traditional controller applications, such as certain types of positioning algorithms, are particularly math-intensive. These applications are far better suited to DSP-type processors than more conventional controllers, according to TI's Scarisbrick, and can speed applications such as a complete proportional integral divergence algorithm far faster than a conventional controller can perform a single multiply. Noting Scarisbrick's view of the microcontroller market, it wouldn't be surprising to see TI introduce a DSP product aimed at the high end of the controller business (such as Intel's 80C196 microcontroller) in the near future. TI sources hint that such a product is already under development and is expected to surface as early as this year.

■ Motorola also has floating point

Not to be left out of the fray, Motorola has announced its 32-bit floating-point part, the 96000, although samples aren't expected to emerge until late in the second quarter of next year. Although Motorola has a firm grasp on the microcontroller market, the company has been slow in initiating its DSP family. Motorola is expected to bring out two versions of the 96000: the 96001, a single-bus version aimed at high-performance, cost-sensitive applications and the 96002, which incorporates dual buses for high-performance applications. Such applications require a high bandwidth and access to large memory subsystems such as graphics, and image and numeric processing. The two independent bus ports on the 96002, which can be assigned to any of X, Y or program-memory spaces, effectively double off-chip bus bandwidth. In addition, the dual ports facilitate interfacing to page-mode and video RAMs.

The parts will be manufactured in Motorola's 1.2-micron HCMOS process with a resultant cycle time of 75 ns (13.33 Mips). By letting the ALU, address generator unit and program controller operate in parallel with the CPU, up to three floating-point

operations, two data moves and two address pointer updates can be executed in a single instruction cycle. This parallelism lets peak performance on the chip reach 40 MFlops. Twin DMA controller channels operate in parallel with the CPU to provide memory-to-memory and memory-to-peripheral transfers. Benchmark results for a 1,024-point complex FFT, says Motorola's Bates, comes in at less than 2 ms. The chip can process over 2 million interrupts/s.

DSP ASICs or ASIC DSPs?

Many DSP system makers have found shortfalls in both the performance and functionality of existing general-purpose, single-chip DSP devices and have thus vied to develop their own DSP ASICs. However, relatively low volume requirements and the lack of availability of specialized DSP cells in ASIC cell libraries have restricted most of these approaches to gate arrays. Most special DSP applications are addressed either by custom implementations of standard DSP chips, or by using discrete building-block approaches. Where manufacturing volumes make it economical, chip makers are providing customized versions of their standard parts. Chip makers are also broadening their array of standard product lines to encompass an increasing sphere of applications.

AT&T's DSP16 and DSP32 have been modularly designed for efficient customization for larger volume applications. This lets the silicon be tailored to specific customer needs. This approach is quite different than a standard-cell approach, according to Ulery. The company uses what it calls a symbolic layout, which lets a computer lay out the chip in much the same way as would be done by hand, only much faster. The technique, according to Ulery, is far more efficient than conventional cell-based design where rails are laid out and macrocells are laid out around them and interconnected via computer.

AT&T is in the process of converting the main processing block of the DSP16 into a form that's compatible with the company's CMOS standard-cell library. This will let users build standard cells around the core processor and develop a custom part within a reasonable turnaround time.

TI is also not ignoring the ASIC market. The company is expected to offer some kind of ASIC implementation of its 320C25 family, but it's not known whether it will be a library cell, a core DSP surrounded with a gate array configuration, or both. It does seem somewhat logical, given the volume requirements of many DSP applications, that a gate array approach offering a customizable I/O surrounding a core processor might well be in the cards. Such an approach would offer users quick turnaround, relatively low NRE and a flexible architecture.

Just about every manufacturer wants to get into the business of catering to the specialized needs of higher volume DSP chip users. Fujitsu is currently working on a couple of custom versions of its 24-bit floating-point device. The ASIC-like design of Fujitsu's 24-bit and 32-bit devices lends them to efficient customization with relatively fast turnaround, according to Fujitsu's Reimer.

"To conjecture that floating-point chips will do anything but dramatically drop in price is heresy."

—John Scarisbrick, Texas Instruments

New applications surface

It seems clear that there's a rosy future for general-purpose DSP chips. Still, such devices will probably never completely replace discrete building blocks in traditional DSP applications. Continued growth of general-purpose, single-chip DSPs is likely to be more of a factor in new applications rather than simply an expansion in traditional markets.

As DSP technology continues to mature, even potential users can't agree on what type of part, what functions or even what performance levels are required. A casual survey of potential users would reveal that some who are involved in PC add-in cards are more interested in cost, power and space savings than building-block approaches. Other potential users who are involved in military and other flat-out performance applications seek the ultimate in performance and are willing to sacrifice many of the convenience features. Still others want features like double-precision (64-bit) arithmetic and IEEE-formatted numbers.

Customization is only part of the solution. Many of the applications don't have sufficient volume to warrant custom approaches, or even ASIC standard-cell or gate array approaches. So DSP chip makers are trying to carefully carve out large niches with standard products, while leaving enough flexibility to accommodate a variety of applications.

And new applications are surfacing almost daily. "Customers, in their infinite wisdom, continue to come up with new and different applications we've never even conceived of," says AT&T's Ulery. Adds Motorola's Bates, "DSP technology is now about where microprocessor technology was in the early 1970s—in a period of explosive growth."

It's anticipated that much of this future growth will occur around the latest breed of floating-point chips. However, price tags for these new chips are almost universally topping the $1,000 mark in small volumes. "To conjecture that these chips will do anything but dramatically drop in price is heresy—and ignoring the history of the semiconductor business," says TI's Scarisbrick. "Remember, the TMS32010 sold for $500 when it was first introduced in 1982. Now you can buy a better part for under $5." □

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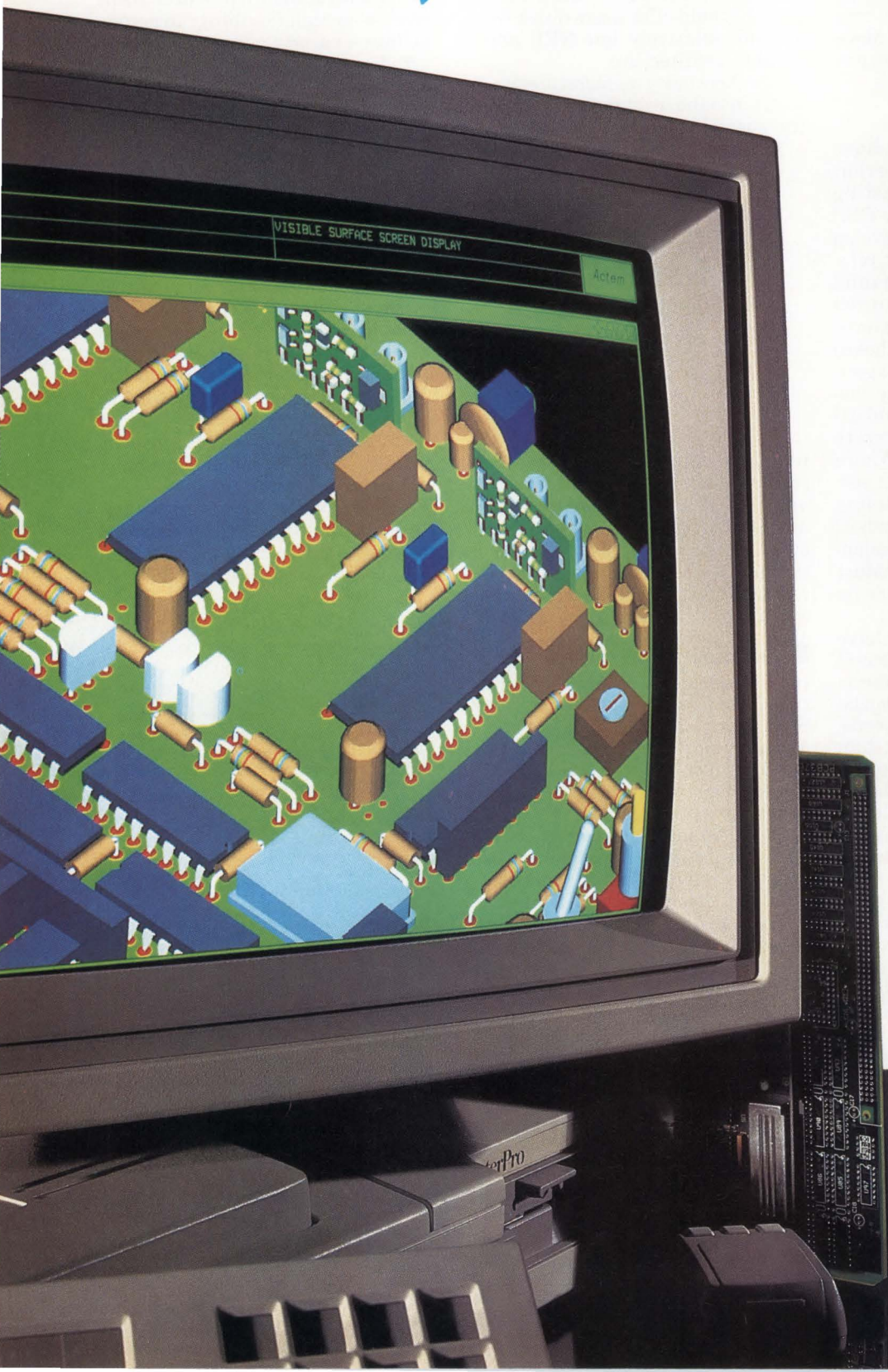

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MMU requires tailoring to meet needs of demand-paging Unix

A proposed MMU design strategy overcomes the bottlenecks and inefficiencies associated with virtual-to-physical address translation in demand-paging Unix systems.

Andreas Meyer

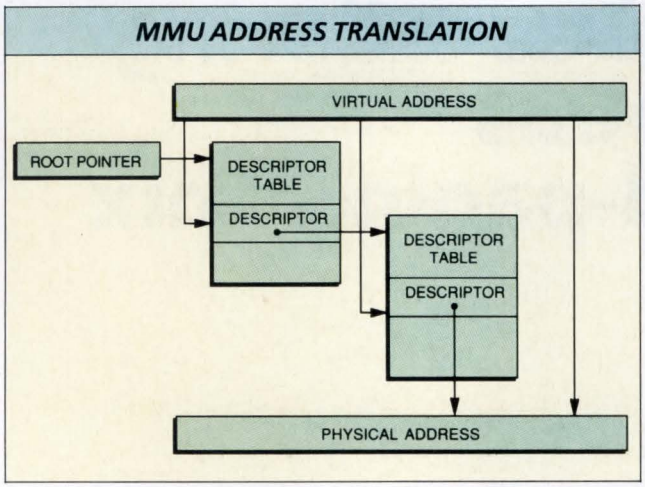
Designers hate having to deal with memory-management units—they're huge, they slow down the CPU and they're mysterious to program. For a computer system using AT&T's Unix, though, the designer has no choice but to use a memory-management unit (MMU) to perform virtual-to-physical address conversion and to handle the system's storage strategy. Although commercial MMU ICs weren't designed especially for Unix, they nonetheless fulfill its requirements quite well. Unix Version 5.3, however, adds the requirement of demand paging—a performance enhancement that many MMU designs don't serve as well.

For a running program, there's practically no difference between demand paging and the older swapping mechanism. In either case, the application program is always looking into a clean virtual address space and doesn't know, or care, where programs and data reside in memory. When all the factors are considered, however, it's clear that demand paging has several advantages over the old swapping mechanism.

To begin with, paging makes storage management much simpler, faster and easier to understand. Some frequently used Unix functions—exec and fork, for example—run considerably faster. Also, because of the way paging manages memory, the virtual address space seen by the application program can be larger than the available main memory. But don't expect miracles from demand paging. It can't make up for an inadequate amount of main memory, and the administrative demands that it places on a Unix kernel can be substantial.

Unix programs are usually logically partitioned into variable-sized segments, visible to the programmer and available to multiple processes. Since a nonpaging Unix kernel puts segments into contiguous memory areas, the MMU's job is relatively easy. It extracts a segment number from certain bits of the virtual address and, based on the contents of a base register, derives the physical address. If processes require more main memory than is available, the kernel swaps out whole segments to the "swap space," a partition of the system disk that also holds the Unix file system.

Andreas Meyer manages the Unix port department at Stollmann GmbH (Hamburg, West Germany).



To translate a virtual address to a physical location, an MMU must walk through a sequence of descriptor tables, which adds substantially to MMU overhead.

■ Swapping is now impractical

Although suitable for 1970s computing performance and memory densities, the swapping mechanism is extremely impractical and inefficient for today's machines, which are best served by demand-paging Unix. With demand paging, the available memory in the disk swap space and in main memory are combined to form the total "swappable memory." Because the memory is organized this way, a system with 5 Mbytes of main memory and 3 Mbytes of disk storage designated as swap space, for example, can run an 8-Mbyte program.

Demand paging splits main memory into many physical pages, or "frames," of equal size—typically 1, 2 or 4 kbytes each. Segments are also split into equal-sized virtual pages. A CPU programs an MMU by sending it a root pointer (which directs it to a particular table) and a virtual address (part of which designates one particular descriptor in the table). The descriptor typically points the MMU to another table that contains additional information—about validity and protection mechanisms, for example. A virtual address provided by the CPU designates the appropriate descriptor in subsequent tables. The final table contains the page descriptors that point to the actual physical page frames.

Although a segment's virtual address space remains contiguous with demand paging, the segment itself may be scattered all over main memory. And, since there's a page descriptor for each virtual page, some pages may still reside on the disk. When the CPU tries to access such a page, the MMU must interrupt the CPU and generate a bus error. The bus error service routine can then load the missing page into main memory and, if necessary, other pages can be swapped out.

■ MMU designs differ

It's difficult to pinpoint the requirements for the optimal MMU for a demand-paging Unix machine because many different solutions have worked. Storage-management designs vary considerably in how they link virtual addresses to page tables, but none of the existing MMU ICs handles segments as known under Unix. Since the MMUs all look at the user's virtual address space as if it were linear and unstructured, it's up to the Unix kernel to map the segments to a linear address space for the MMU.

In today's MMU designs, the descriptor tables are located in main memory. The MMU must fetch the descriptors, performing a "table walk," which slows down overall system operation. To minimize MMU overhead, however, MMU ICs typically have internal address-translation caches, which contain the most recently used virtual addresses and their page descriptors.

Most MMU designs split the linear address space into two or three consecutive MMU tables. The three-level solution is slower than the two-level one, since the MMU needs three memory cycles instead of two for a table walk, but the two-level solution needs much more memory space. Most MMUs can handle only a fixed page size. Two-level MMUs require a page size of 4 kbytes to accommodate the tables. Smaller pages make better use of memory, but they need more MMU table walks and CPU overhead. Longer pages are useful when there's plenty of main storage and a fast disk. With longer pages, there are also fewer page faults and table walks, but if there's too little memory available, the lengthened execution time wipes out this relative advantage.

■ A review of existing MMU ICs

The available MMU ICs—many of which are companion parts for particular microprocessors—are typically general-purpose MMUs that can run virtually any operating system. They differ in their page sizes, translation

A REVIEW OF EXISTING MMU ICs

	Motorola	Motorola	National	Intel	Fairchild	AT&T
CPU	68020	68030	32332	80386	Clipper	32100
MMU	68851	integrated	32382	integrated	CAMMU	32101
Page size (bytes)	256 to 32k	256 to 32k	4k	4k	4k	2k
Level 0	3 root pointers supervisor/ user/ DMA	2 root pointers supervisor/ user	2 root pointers supervisor/ user	segmentation unit 1 root pointer	1 root pointer	4 root pointers
Level 1	1 to 4 levels 1 to 15 bits each	1 to 4 levels 1 to 15 bits each	10 bits	10 bits	10 bits	13 bits
Level 2	—	—	10 bits	10 bits	10 bits	6 bits
Address translation cache (descriptors)	64	22	32	32	64	level 1: 32 level 2: 64
Organization	full associative	full associative	full associative	four-way set associative	two-way set associative	two-way set associative

levels and address-translation cache organizations (see "A review of existing MMU ICs," p 64).

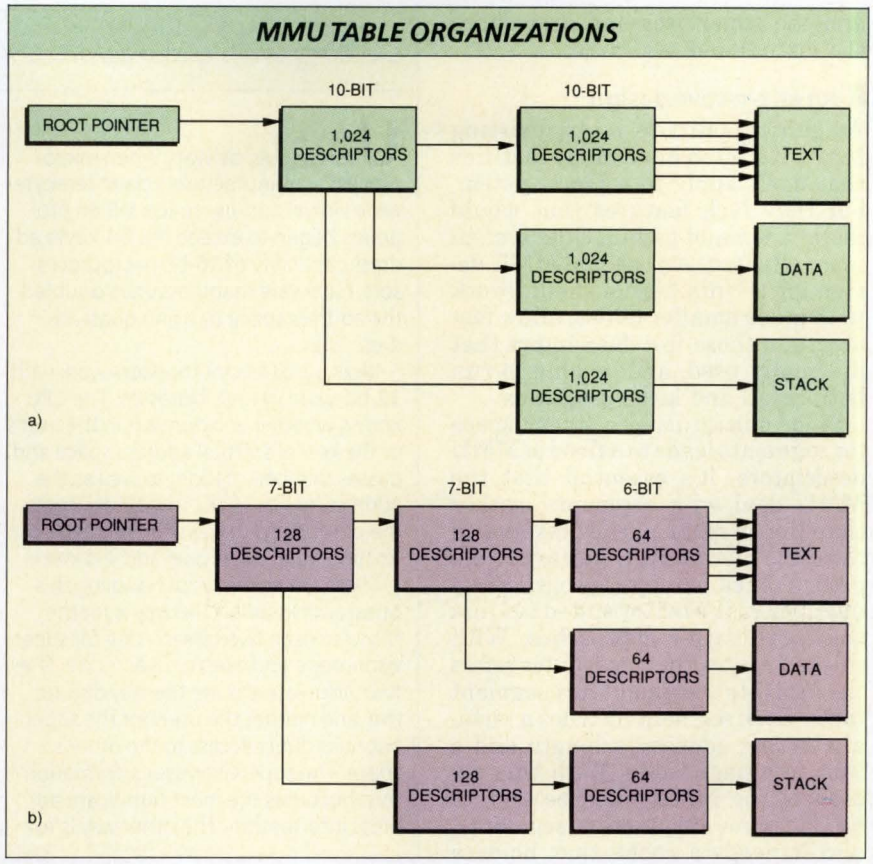
The MMU with the widest range of features is the 68851 from Motorola (Austin, TX) for the 68020 microprocessor. Page sizes for the 68851 can range from 256 bytes to 32 kbytes. The chip has root pointers for supervisor, user and direct memory access modes that can refer to an optional descriptor table. The part can provide one to four levels of MMU tables and can handle both short (32-bit) and long (64-bit) descriptors. The long descriptors include a field that gives the size of the subsequent table. After a bus error occurs, the MMU returns neither the address nor an explanation of what caused the error. This is an inconvenience, since that information is difficult to get from the 68020.

The Motorola 68030—the successor to the 68020—has an integrated MMU with nearly all the 68851 features, except that the size of the address-translation cache has been reduced from 64 to 22 entries. Two transparent windows in the 68030 let the MMU be bypassed, giving direct access to main memory.

While the Motorola MMUs can handle a variety of page sizes, the 32382 from National Semiconductor (Santa Clara, CA) for the NS32332 microprocessor handles only 4-kbyte pages. The 32382 has two root pointers (called page table base registers)—one for supervisor mode and one for user mode. Both pointers refer to a level 1 MMU table; level 2 is the page tables themselves. The rough splitting of the virtual address produces MMU tables too long for typical Unix programs.

The 80386 microprocessor from Intel (Santa Clara, CA) includes as an MMU a segmentation unit and a paging unit. With this processor, a segment can be selected by the context of the instruction (instruction fetches always access the code segment) or explicitly by a prefix instruction. A process has up to six segments, but only three of them—code, stack and data—are obligatory.

In the 80386, the segmentation unit checks the validity of the virtual address and outputs a linear address for the paging unit. If the kernel uses the segmentation unit, it has to add segmentation information to each virtual address. It's possible, however, to bypass the segmentation unit, in which case the paging unit acts as the MMU.



For a sample Unix program with a 4-kbyte page size, a two-level MMU table organization (a) with 10 bits of virtual addressing provides 4,096 descriptors, only 10 of which (0.24 percent) are essential. A three-level organization (b) with 7-bit virtual addressing at levels 1 and 2 and 6-bit addressing at level 3 provides 576 descriptors, of which only about 12 (2.1 percent) are really needed.

The paging unit of the 80386 handles 4-kbyte pages. As with the National part, a root pointer refers to level 1 tables, while level 2 is the page tables. Since the paging unit has only one root pointer, the supervisor and the user must share the virtual address space. Here, too, the rough splitting of the virtual address produces MMU tables that are too long for typical Unix programs. The page descriptor also lacks "cache inhibit," a useful feature for an external cache.

As general-purpose parts, existing MMU ICs often have many features that don't apply to a Unix system.

■ ■ ■

A simple MMU, the CAMMU (cache/MMU) from Intergraph (Palo Alto, CA) for the Clipper microprocessor handles only 4-kbyte pages and includes two root pointers—one for supervisor and one for user address space. The virtual address is split by two levels and produces MMU tables too long for typical Unix programs. The CAMMU also includes a data cache. The Clipper requires a pair of MMUs: one for instructions, another for data.

Compared to those in the other MMUs, the tables used by the WE32101 from AT&T (Holmdel, NJ) are relatively small. The first level of MMU tables is addressed by 13 bits of the virtual address and may, therefore, become as long as 32 kbytes—a somewhat clumsy feature since MMU tables must be stored in physical memory and contiguous physical memory longer than 2 kbytes isn't directly available. Like the 80386, the second level of MMU tables is the actual page tables. The WE32101 (for the WE32100 microprocessor) has 2-kbyte pages and four root pointers,

and the supervisor and user share the virtual address space.

An alternative design

As general-purpose parts, existing MMU ICs often have many features that don't apply to a Unix system, but they lack features that would make a demand-paging Unix system more efficient. An optimal MMU design for a Unix kernel should work with much smaller tables, allow fast access to those few descriptors that are really used, and be able to run both small and large programs.

Since substituting a linear space for segments leads to a flood of MMU descriptors, it's essential that the MMU deal with segments, rather than linear space, at the first level of the table hierarchy. Because this approach takes account of program segmentation, it's better suited to Unix than alternative approaches. With this technique, the root pointer refers the MMU to a segment in a segment table. Each segment includes a virtual starting address, a length and a link to a page table. With this approach, the MMU must be able to handle some disjunctive segments, and it needs a cache that holds a descriptor for each program segment. With this cache filled, however, a table walk will require only one memory access in most cases. If the MMU can't find the appropriate descriptor in the cache, it can then search a linear table in memory.

With this scheme, the MMU recognizes the right segment by comparing the given address to the virtual base and length of the segment descriptor. This table search and compare is slow, and it's more difficult to implement in hardware than extracting bits from the virtual address. Nevertheless, this process occurs only for a table walk, and it drastically reduces the size of subsequent descriptor tables.

For small segments, the second-level table is the page table itself; very long segments require a third-level table and a second cache for least recently used page descriptors. Supervisor segments and special I/O segments may even work without page tables. In this case, the segment table would point directly to the contiguous physical memory. □

Dealing with quasi address lines

Users should be wary when microprocessor manufacturers claim terabyte-wide virtual address space. When programs began to exceed the 64-kbyte address capability of 16-bit microprocessors, hardware manufacturers doubled the address space by using quasi address lines.

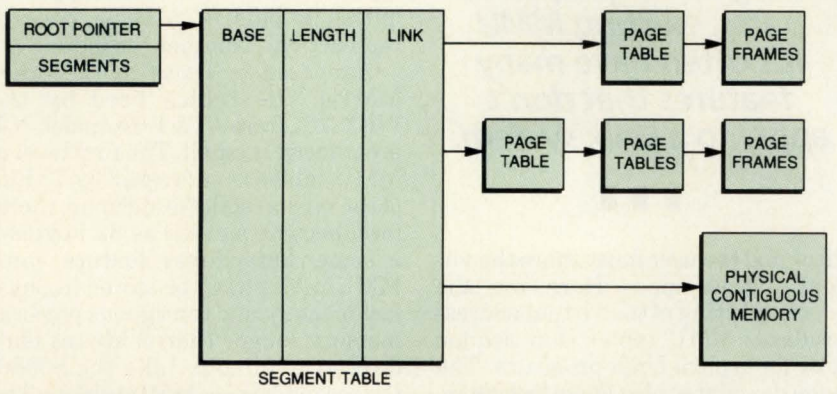
Most 32-bit microprocessors work with 32-bit-wide virtual addresses. The CPU knows whether an address is in the user's or the kernel's virtual address space and passes this information, as well as the address, to the MMU. The MMU treats the pin conveying this user/kernel distinction as an additional address line.

There are two ways of handling this quasi address line. One way is for the MMU to keep two tables—one for supervisor mode and one for user mode. The two virtual spaces are thereby disjunctive, and neither the user nor the supervisor has direct access to the other's space. The supervisor/user information thus becomes the most significant address information. The other way is for the supervisor and the user to share one virtual space, with one common MMU table for both. The MMU then compares the supervisor/user information to correct information that will go into the MMU tables.

Both of these methods are widely used. When separate tables are kept for the supervisor and user modes, some Unix kernel addresses will have 33 bits if it can't be contextually determined whether the address is a user or a supervisor address. When the supervisor and the user share one virtual space, the user's virtual space shrinks. This factor is barely a disadvantage in a 4-Gbyte-wide space, but it doesn't let user programs start at address 0. On the other hand, the address itself identifies the virtual space to which it belongs.

Nearly all microprocessors offer other quasi address lines (segments, program/data/stack, and so forth) that are passed to the MMU. If the kernel treats these as address lines, it needs additional administrative facilities to handle them.

A PROPOSED UNIX MMU



Demand-paging Unix requires special features in an MMU. If segments, rather than linear descriptor tables, are used for the first-level MMU table, table-walk overhead is diminished and the ability to keep table size down is enhanced.

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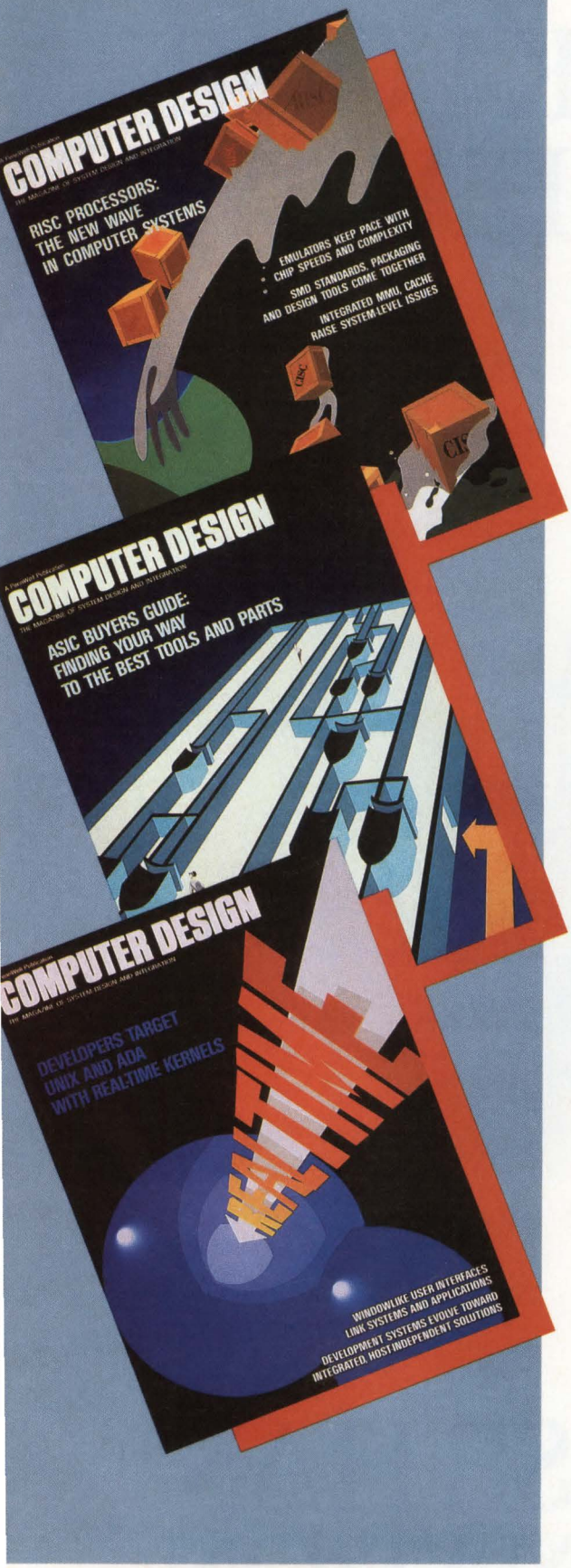

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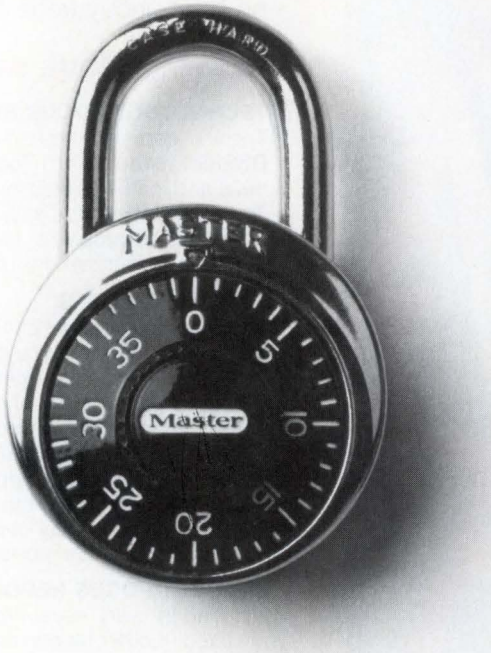

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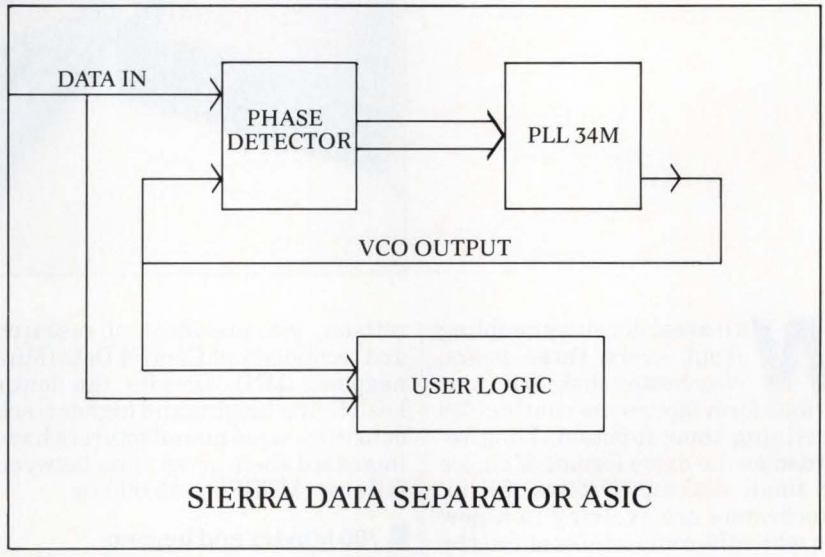

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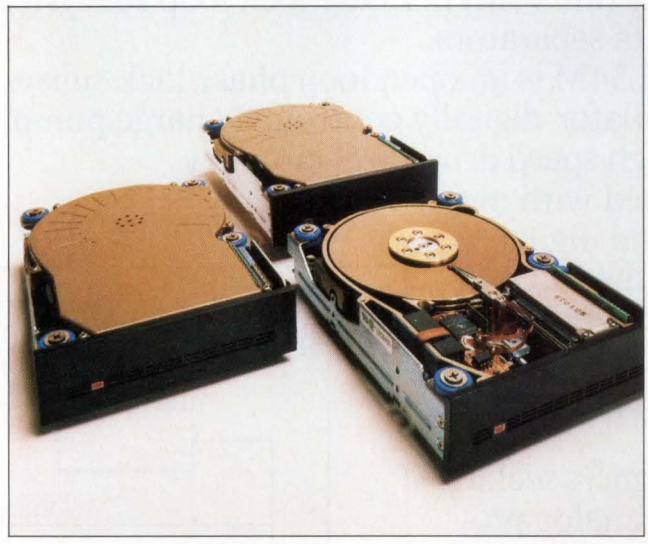
CIRCLE NO. 28

PERIPHERALS AND MEMORY SYSTEMS

5¼-in. Winchesters move toward gigabyte capacities

John H. Mayer, Senior Associate Editor



Half-height 5¼-in. Winchester disk drives such as these from Microscience provide up to 150 Mbytes of storage in a 1.6-in.-high box. Microscience was the first manufacturer to use voice-coil motors in the half-height form.

With areal densities doubling about every three years, Winchester disk drives at various form factors are continually redefining their function. Long regarded as the drive format of choice for small desktop systems, 5¼-in. Winchesters are evolving to a new role while the compactness offered by smaller 3½-in. hard drives provides an irresistible lure to small-systems manufacturers. Today's 5¼-in. Winchesters are increasingly found in relatively higher performance desktop personal computers and workstations and are slowly usurping the role of larger 8-in. units in file server and multiuser applications.

Driving this transition are steady advances in head and disk technology. Today's state-of-the-art drives are moving from minicomposite to thin-film heads and from particulate to plated and sputtered media. Head flying heights are dropping as low as 9 μin. and are expected to go to 6 μin. by the early 1990s. The extensive use of CMOS in drive control electronics and the design of lighter, more accurate actuators has helped lower power consumption and increase track densities.

But the real success of disk drive designers has been their ability to implement these performance increments without reducing drive reliability. "As areal density increases and as margins shrink, the major challenge is maintaining the reliability of the unit," says Garrett A. Garrettson, vice-president of research and technology at Control Data (Minneapolis, MN). Despite the lower head flying heights and higher track densities, some manufacturers have increased their mean time between failures (MTBF) to 35,000 hr.

■ 700 Mbytes and beyond

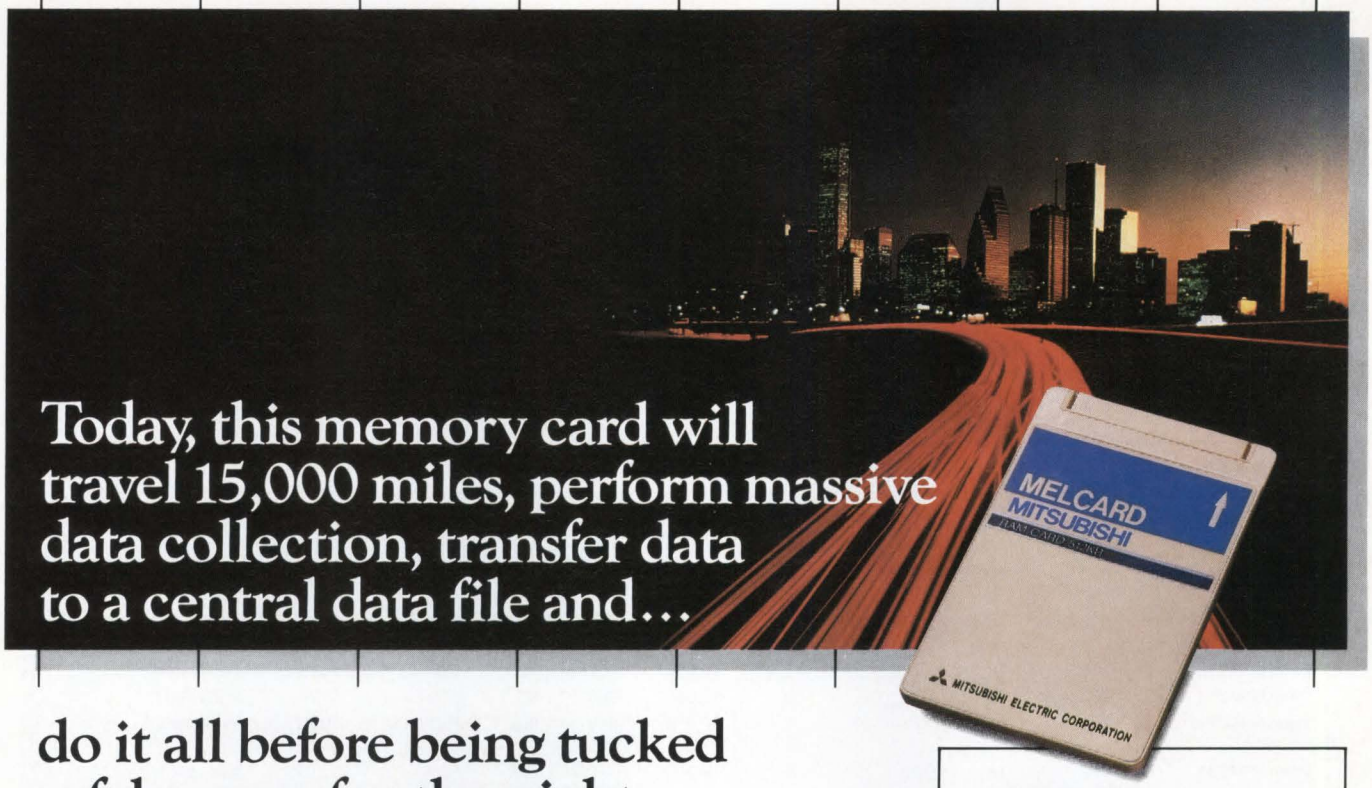
The highest capacity 5¼-in. Winchesters presently available manage to deliver well over 700 Mbytes of storage capacity by packing up to eight platters in a box and making extensive use of thin-film heads. Drives at these densities can offer a lower price per Mbyte than many 8-in. storage systems. Maxtor (San Jose, CA) introduced the first 5¼-in. drive with more than 700 Mbytes over two years ago. The XT8760 delivered 765 Mbytes of capacity and added an unprecedented 15-MHz data-transfer rate. A new actuator design helped push track densities to 1,376 tracks/in.

One of the first 5¼-in. Winchesters to follow Maxtor over the 700-Mbyte barrier was the Megafile 5000 series from Siemens Information Systems (Newbury Park, CA). Using thin-film heads and high-resolution media, the drives store up to 777 Mbytes. The eight-platter drives have a recording density of 30,825 bits/in. and an average seek time of 16 ms. Track density is 1,476 tracks/in. The drives come with either an enhanced small device interface (ESDI) or a small computer system interface (SCSI) and claim an industry-standard 30,000-hr MTBF.

Micropolis (Chatsworth, CA) added its own high-capacity 5¼-in. Winchester last fall. Like the Siemens and Maxtor drives, the 1560/1580 series transfers data at 15 MHz, with either a SCSI or an ESDI. The SCSI supports either single-ended or differential interconnection. Average seek time on the drive is 16 ms.

In the last six months, both Fujitsu America (San Jose, CA) and Control Data have added 700-Mbyte drives to their product lines. Fujitsu uses thin-film media platters to push the capacity of its M2263E drive to 778 Mbytes unformatted. The unit features a spindle synchronization capability designed to adapt it to drive clustering and disk array applications. Control Data extended its Wren V line to 702 Mbytes last May. The high-capacity drive uses data caching and a read-lookahead function to increase data throughput. With a SCSI, the drive delivers data-transfer rates as high as 16 Mbits/s and an average seek time of 16 ms.

The 5¼-in. Winchesters at these lofty capacities are typically resorting to servos with dedicated surfaces or hybrid dedicated/embedded positioning systems. Rich Freedland, president of Helios (Sunnyvale, CA), a supplier of servowriters to disk drive vendors, predicts that as capacities increase drives will continue to migrate to a hybrid servo solution. "You need the bandwidth of a dedicated servo system to get to the



Today, this memory card will travel 15,000 miles, perform massive data collection, transfer data to a central data file and...

do it all before being tucked safely away for the night.

Now, with Mitsubishi's transportable memory cards, you can have the flexibility of carrying 32K Bytes to 2M Bytes of SRAM, OTPROM or masked ROM in your pocket. That means read/write capability (without a disk drive), remote from central data storage, plus the flexibility to interchange memory types (SRAM, OTPROM, masked ROM), upgrade and downgrade memory density, and change data width (8 bits, 16 bits). All with an extremely rugged device that's the size of a credit card (86mm x 54mm x 3.4mm).

The Applications Are Virtually Endless.

From personal computers to printers, portable equipment to telecommunications, the applications are as creative and endless as the imagination. Anywhere transportable memory and massive data storage are required, Mitsubishi's transportable cards offer the highest memory densities available on a device this small.

Save On Systems Design Costs.

Mitsubishi's transportable memory cards offer standardized card connectors and pin assignments for easy memory interchange and density upgrade, without designing multiple host system models. Plus, future system redesign is simplified or eliminated.

Extremely High Density Memory.

The key to Mitsubishi's extremely high density memory cards is the VSOP (very-small-outline-package). Pioneered by Mitsubishi, the VSOP is over four times smaller (in overall volume) than its equivalent pin count, standard surface mount package. In fact, the VSOP is smaller than the footprint of the equivalent chip-on-board technology making it possible to pack up to 16 memory ICs, plus standard interface circuitry on one card.

VSOP

13.8 mm x 8.0 mm x 1.0 mm = 110.4 mm^3

Chip-On-Board

15.4 mm x 9.8 mm x 1.0 mm = 150.9 mm^3

SOP

17.5 mm x 12.2 mm x 2.2 mm = 469.7 mm^3

"Transportable" Means "Rugged."

Mitsubishi designed its memory cards specifically for transportable applications. And, that means cards that are rugged and reliable. Even if a card is dropped, loss of valuable data is virtually eliminated, due to Mitsubishi's flexible, four-layer PCB and enhanced soldering techniques.

Additionally, the cards are ESD protected to 25K volts, with connectors guaranteed for 10,000 insertions.

If you want to design-in massive, transportable data storage with the flexibility to interchange memory types and densities, Mitsubishi memory cards give you the maximum memory mileage. For more information call or write today: Mitsubishi Electronics America, Inc., Semiconductor Division, 1050 East Arques Avenue, Sunnyvale, CA 94086. (408) 730-5900.

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CIRCLE NO. 29

Model	Unformatted Capacity (Mbytes)	Average Access Time (ms)	Data Transfer Rate (Mbits/s)	# of Data Surfaces	# of Read/Write Heads	Record Density (bits/in.)	Track Density (tracks/in.)	Encoding Scheme	Interface	OEM Price	Comments
Century Data 2055 Gateway Pl, San Jose, CA 95110 (408) 298-5756											**Circle 100**
14404	140	20	10	4	4	21,000	1,450	RLL	ESDI/SCSI	$1,130	MTBF 30,000 hr
14405	170	20	10	5	5	21,000	1,450	RLL	ESDI/SCSI	$1,250	MTBF 30,000 hr
14406	210	20	10	6	6	21,000	1,450	RLL	ESDI/SCSI	$1,450	MTBF 30,000 hr
Control Data 8100 34th Ave S, Minneapolis, MN 55440 (612) 853-5795											**Circle 101**
Wren II 94205-51	51	28	5	5	5	9,535	960	MFM	ST506	$415	half height
Wren II 94205-77	77	28	7.5	5	5	13,680	960	RLL	ST506	$455	half height
Wren II 94205-71/65	85.8	28	7.5	5	5	13,680	960	RLL	ST506/ PC AT	$675/ $645	half height
Wren II 94155	86/135	28/28	5/7.5	9/9	9/9	9,274/ 14,043	960/ 960	MFM/ RLL	ST506	$625/ $695	two encoding schemes, full height
Wren III 94216	106	18	10	5	5	19,058	960	RLL	ESDI	$695	half height
Wren III 94211	106	18	10	5	5	19,058	960	RLL	SCSI	$755	half height
Wren IV 9416X	182	16.5	10	9	9	19,058	960	RLL	ESDI/SCSI	$960/ $1,030	full height
Wren V 94221	209	18	9-15	5	5	19,500	1,280	ZBR	SCSI	$1,095	half height
Wren IV 94171	375	16.5	9-15	9	9	19,500	1,280	RLL	SCSI	$1,495/ $1,595	Zoned-Bit Recording
Wren V 94186-383	382	19	10	15	15	19,800	1,280	RLL	ESDI	$1,495	full height
Wren V 94186-383H	382	14.5	10	15	15	19,800	1,280	RLL	ESDI	$1,595	full height
Wren V 94186-442	440	16	10	15	15	19,800	1,280	RLL	ESDI	$1,695	full height
Wren V 94181-638	702	16.5	9-15	15	15	19,800	1,280	RLL	SCSI	$1,995	Zoned-Bit Recording
Fujitsu America 3055 Orchard Dr, San Jose, CA 95134 (408) 432-1300											**Circle 102**
M2242A52	54.9	30	5	4	7	—	760	MFM	ST506	$950	—
M2243A52	86.3	30	5	6	11	—	760	MFM	ST506	$1,000	—
M2243R	129.6	25	0.9*	4	7	—	1,226	RLL	ST506	$1,150	half height
M2246	172	25	10	6	10	20,400	850	RLL	ESDI/SCSI	$1,200/ $1,320	ESDI or SCSI
M2249	389	18	10	8	15	20,400	850	RLL	ESDI/SCSI	$1,975/ $1,930	ESDI or SCSI
M2263	778	16	1.87*	8	15	—	—	RLL	ESDI	$3,170	—
M2243T	864	25	5	4	7	—	1,226	MFM	ST506	$1,000	—
Hewlett-Packard 11413 Chinden Blvd, Boise, ID 83714 (208) 323-3290											**Circle 103**
HP97530E	130/195/ 389	17	10	4/6/12	4/6/12	20,500	1,590	RLL	ESDI	—	wide environmental specs
HP97530 S/T/D	136/204/ 323	17.5	2/4/4*	4/6/12	4/6/12	20,500	1,590	RLL	SCSI	—	same as above
HP7962B/HP7963B	152/304**	17	1.25*	6/12	6/12	20,500	1,590	—	HP-IB	—	HP systems only
HP795XB	81/152/ 304**	17	1.25*	4/6/12	4/6/12	20,500	1,590	—	HP-IB	—	HP systems only
Hitachi America, Computer Div 950 Elm Ave, Suite 100, San Bruno, CA 94066 (415) 872-1902											**Circle 104**
DK514-38	382.3	16	14.5	14	14	26,000	1,033	RLL	ESDI	—	10-W power
DK514S-38 S/D	382.3	16	14.5	14	14	26,000	1,033	RLL	ESMD	—	single- or dual-port
DK514C-38	382.3	16	12/32	14	14	26,000	1,033	RLL	SCSI	—	supports SCSI
Maxtor 211 River Oaks Pkwy, San Jose, CA 95134 (408) 432-1700											**Circle 105**
XT-1085	85.3	27	5	9	8	9,110	1,070	MFM	ST506	—	—

Key: * = Mbytes/s; ** = formatted; ESDI = enhanced small device interface; ESMD = enhanced storage module drive; MFM = modified frequency modulation; MTBF = mean time between failures; RLL = run length limited; SCSI = small computer system interface.

Model	Unformatted Capacity (Mbytes)	Average Access Time (ms)	Data Transfer Rate (Mbits/s)	# of Data Surfaces	# of Read/Write Heads	Record Density (bits/in.)	Track Density (tracks/in.)	Encoding Scheme	Interface	OEM Price	Comments
Maxtor 211 River Oaks Pkwy, San Jose, CA 95134 (408) 432-1700											**Circle 105**
XT-1120R	128	27	7.5	9	8	13,665	1,070	RLL	ST506	—	—
XT-1140	143.4	25.8	5	15	15	8,525	1,070	MFM	ST506	—	—
XT-4170S/E	179.4	14	10	9	7	21,064	1,070	—	SCSI/ESDI	—	—
XT-2190	191.2	28.9	5	15	15	10,470	1,070	MFM	ST506	—	—
XT-1240R	240	27	7.5	15	15	13,665	1,070	RLL	ST506	—	—
XT-4280S	302.7	16	10	11	11	21,064	1,070	—	SCSI	—	—
XT-4380S/E	384.5	16	10	15	15	21,064	1,070	—	SCSI/ESDI	—	—
XT-8380S/E	410.1	14.5	15	9	8	31,596	1,376	—	SCSI/ESDI	—	—
XT-8760S/E	768.9	16.5	15	15	15	31,596	1,376	—	SCSI/ESDI	—	—
Micropolis 21211 Nordhoff St, Chatsworth, CA 91311 (818) 709-3300											**Circle 106**
1325	85	28	5	8	8	10,416	960	MFM	ST506	—	rotary voice coil
1355	170	23	10	8	8	19,804	1,055	RLL	ESDI	—	same as above
1375	170	23	5	8	8	19,804	1,055	RLL	SCSI	—	supports 1:1 interleave
1654-7	182	16	10	7	7	21,185	1,100	RLL	ESDI	—	rotary voice coil
1674-7	182	16	15	7	7	21,185	1,100	RLL	SCSI	—	same as above
1578-15	382	18	15	15	15	21,231	1,075	RLL	SCSI	—	supports 1:1 interleave
1558-15	382	18	10	15	15	21,231	1,075	RLL	ESDI	—	rotary voice coil
1568/1588	765	16	15	15	15	31,846	1,440	RLL	ESDI/SCSI	—	same as above
Microscience International 305 N Mathilda Ave, Sunnyvale, CA 94086 (408) 730-8989											**Circle 107**
HH1050	53.3	28	5	3	5	9,957	960	MFM	ST506/412	$430	half height
HH1090	95.8	28	5	4	7	9,840	1,250	MFM	ST506/412	$675	half height
HH2120	149.3	28	10	4	7	16,969	1,250	RLL	ESDI	$835	half height
Miniscribe 1861 Lefthand Cir, Longmont, CO 80501 (303) 651-6000											**Circle 108**
3650	50.5	61	5	3	6	10,124	763	MFM	ST506/412	—	half height
3053	53.3	25	5	3	5	10,200	1,033	—	ST506/412	—	half height
3675	75.8	61	7.5	3	6	15,186	763	RLL	ST506/412	—	half height
6085	85.3	28	5	5	8	9,950	1,000	MFM	ST506/412	—	full height
3085	85.3	22	5	4	7	10,298	1,100	—	ST506/412	—	half height
6128	128	28	7.5	5	8	14,925	1,000	RLL	ST506/412	—	full height
9380E	382	16	10	8	15	20,388	1,100	RLL	ESDI	—	full height, fast access
9380S	382	16	10	8	15	20,388	1,100	RLL	SCSI	—	full height, fast access
Mitsubishi Electronics America, Computer Peripherals Div 991 Knox St, Torrance, CA 90502 (213) 515-3993											**Circle 109**
MR535	50.8/76.3	28/28	5/7.5	5/5	5/5	9,358/ 14,037	1,028/ 1,028	MFM/ RLL	ST506/412	—	half height, two encoding schemes
NEC Information Systems 1414 Massachusetts Ave, Boxboro, MA 01719 (508) 264-8000											**Circle 110**
NEC D5655	179.8	18	10	4	7	19,610	1,240	RLL	ESDI	$855	—
NEC D5662	385.4	18	10	8	15	19,660	1,240	RLL	ESDI	$1,820	dedicated servo
Priam 20 W Montague Expwy, San Jose, CA 95134 (408) 434-9300											**Circle 111**
V160	60.7	28	5	5	5	10,526	1,047	MFM/ RLL	ST412/ ST506	$525	closed loop servo
V185	85	28	5	7	7	10,526	1,047	MFM/ RLL	ST412/ ST506	$575	closed loop servo
519	191.2	22	5	15	15	10,924	1,070	MFM/ RLL	ST412/ ST506	$1,150	dedicated servo
638/738	382.7	18	10	15	15	21,848	1,070	RLL	ESDI/SCSI	$1,495	dedicated servo

Model	Unformatted Capacity (Mbytes)	Average Access Time (ms)	Data Transfer Rate (Mbits/s)	# of Data Surfaces	# of Read/Write Heads	Record Density (bits/in.)	Track Density (tracks/in.)	Encoding Scheme	Interface	OEM Price	Comments
Quantum 1804 McCarthy Blvd, Milpitas, CA 95035 (408) 432-1100											**Circle 112**
Q250	58**	26	10	2	4	20,000	876	RLL	SCSI	$595	Discache buffer mgmt
Q280	80**	26	10	3	6	20,000	876	RLL	SCSI	$895	same as above
Rodime 901 Broken Sound Pkwy NW, Boca Raton, FL 33431 (407) 994-6200											**Circle 113**
RO5090	89.2	28	5	7	8	10,024	1,100	MFM	ST412	$705	half height
RO5125S	126.9	24	10	5	6	20,050	1,100	RLL	SCSI	$850	half height
RO5125E	127.4	18	10	5	6	20,049	1,100	RLL	ESDI	$850	half height
RO5130R	133	28	7.5	7	8	15,036	1,100	RLL	ST506/412	$765	half height
RO5180S	177.8	24	10	7	8	20,050	1,100	RLL	SCSI	$995	half height
RO5180E	178.4	18	10	7	8	20,049	1,100	RLL	ESDI	$995	half height
Seagate Technology 920 Disc Dr, Scotts Valley, CA 95066 (408) 439-2276											**Circle 114**
ST225N	21.3**	65	5	2	4	9,827	588	MFM	SCSI	—	half height
ST225	25.6	65	5	2	4	9,827	588	MFM	ST412	—	half height
ST4038	38.2	40	5	3	5	9,617	750	MFM	ST412	—	full height
ST238R	38.4	65	7.5	2	4	14,740	588	RLL	ST412	—	half height
ST251N	43.1**	28	7.5	2	4	14,902	777	RLL	SCSI	—	half height
ST4053	53.3	28	5	3	5	9,792	1,031	MFM	ST412	—	full height
ST277N	64.9**	28	7.5	3	6	14,902	777	RLL	SCSI	—	half height
ST296N	85**	28	10	3	6	19,869	777	RLL	SCSI	—	half height
ST4096	96	28	5	5	9	9,792	1,031	MFM	ST412	—	full height
ST4144R	144	28	7.5	5	9	14,688	1,031	RLL	ST412	—	full height
ST4192N	168.5**	17	10	5	8	20,078	1,047	RLL	SCSI	—	full height
ST4192E	191.1	17	10	5	8	20,078	1,047	RLL	ESDI	—	full height
Siemens Information Systems, Memory Products Div 1077 Business Ctr Cir, Newbury Park, CA 91320 (805) 375-2500											**Circle 115**
1300	310	25	10	14	13	19,331	1,207	RLL	ESDI	$1,995	rotary voice-coil actuator
2300	310	25	10	14	13	19,331	1,207	RLL	SCSI	$1,995	same as above
4410	382.6	18	15	12	11	26,907	1,207	RLL	ESDI	$2,300	same as above
4420	382.6	18	15	12	11	26,907	1,207	RLL	SCSI	$2,300	same as above
5810	777	16	15	16	15	30,825	1,476	RLL	ESDI	$2,995	same as above
5820	777	16	15	16	15	30,825	1,476	RLL	SCSI	$2,995	same as above
Syquest Technology 47923 Warm Springs Blvd, Fremont, CA 94539 (415) 490-7511											**Circle 116**
SQ-555	55	25	10	2	2	23,642	1,086	RLL	SCSI	$995	removable cartridge
Toshiba America, Disk Products Div 9740 Irvine Blvd, Irvine, CA 92718 (800) 456-3475											**Circle 117**
MK-53FB	43.2/64.8	25-30	5/7.5	5	5	9,383	900	MFM/ RLL	ST506/412	$735	dedicated servo
MK-54FB	60.5/90.8	25	5/7.5	7	7	9,383	900	MFM/ RLL	ST506/412	$835	same as above
MK-153FA	86.5	23	10	5	5	18,766	900	RLL	ESDI	$1,100	same as above
MK-153FB	86.5	23	15	5	5	18,766	900	RLL	SCSI	$1,195	same as above
MK-56FB	86.5/ 129.8	25	5/7.5	10	10	9,383	900	MFM/ RLL	ST506/412	$975	same as above
MK-154FA/154FB	121	23	10/15	7	7	18,766	900	RLL	ESDI/SCSI	$1,255	same as above
MK-156FA	172.9	23	10	10	10	18,766	900	RLL	ESDI	$1,255	same as above
MK-156FB	173	23	15	10	10	18,766	900	RLL	SCSI	$1,330	same as above
MK-250F	382	18	15	10	10	31,248	1,223	RLL	ESDI/SCSI	$2,235	center stack hybrid servo

extremely high 2,000-track/in.-and-above densities," he says. "And when you get to those levels, you need something on the disk surface itself in the loop, kind of like a coarse and fine adjustment."

But despite this challenge that higher density drives present to head-positioning systems, servo technology won't inhibit capacity drive development, claims Freedland. "We've been shipping servo writers with positioning capability that would allow a manufacturer at least 3,000 tracks/in.," he says. "The densities are such that we can handle another couple of iterations of head-media technology."

380-Mbyte competition hot

By general consensus, the money-making segment of the 5¼-in. Winchester market in the near term will be in the 380-Mbyte range. Driven by the growing popularity of 80386-based machines and associated software, as well as by the established workstation and multiuser markets, sales of 5¼-in. Winchesters in this capacity range are growing at the highest rates. Just last spring, Dataquest (San Jose, CA) doubled an earlier sales forecast for worldwide shipments of 5¼-in. Winchesters in the 200- to 500-Mbyte range.

Product maturity has also driven demand. Over the past year, most major drive vendors have proven they can deliver reliable 380-Mbyte drives in high volumes. Maxtor (San Jose, CA) introduced the world to the 380-Mbyte 5¼-in. drive three years ago and claims to have shipped well over 20,000 units. Today, Maxtor's competitors read like a who's who of the disk drive industry, with names such as Control Data, Fujitsu, Hewlett-Packard (Boise, ID), Hitachi (San Bruno, CA), Micropolis, Miniscribe (Longmont, CO), NEC (Boxboro, MA), Priam (San Jose, CA), Siemens and Toshiba (Irvine, CA).

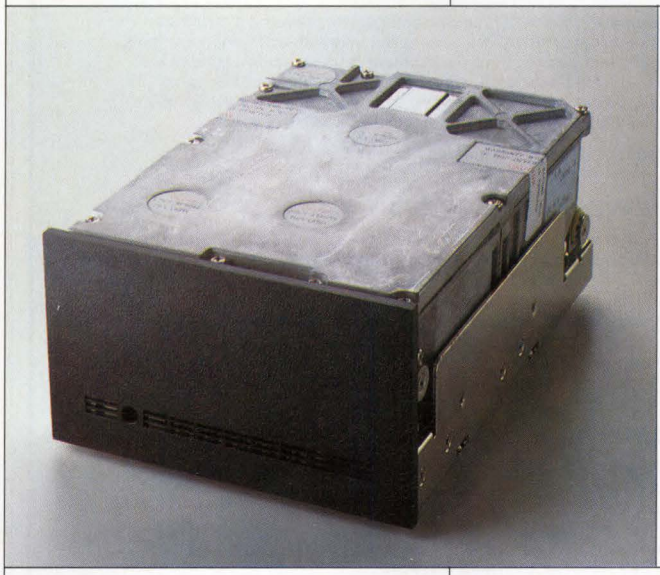
"In 5¼-in. Winchesters, 300 to 400 Mbytes is our hottest form factor," confirms David Ujita, assistant manager of Hitachi's Peripheral Systems Marketing Group. The company's 382-Mbyte DK514 delivers double the capacity of the older 170-Mbyte DK512 by using oxide-coated media and adding two platters. Average access time is 16 ms, and data-transfer rate is 1.8 Mbytes/s. The DK514 offers three interface options: an ESDI, a SCSI and an enhanced storage module drive (ESMD). Ujita sees a slow but steady migration to SCSI, especially as interface standards settle down. "SCSI has definitely proven to be a very strong player in the interface arena," he says.

Lower access times have also spurred 380-Mbyte design-ins. With the latest iteration of its product line, Maxtor cut the access time on its drive from 26 to 16 ms. Fujitsu's M2249 drive offers 18-ms access, and Control Data claims 14.5-ms access on the 383-Mbyte Wren V drive. The company's unique low-mass, straight-arm actuator helps achieve that fast access. The Wren V SCSI models feature Control Data's proprietary Zoned-Bit Recording, a formatting technique capable of enhancing areal density by 30 percent by recording more bytes on the longer outer tracks than on the shorter inner ones.

As higher capacity 5¼-in. Winchesters move to graphics-intensive applications, users will demand higher data-transfer rates. Toshiba targeted that requirement with its 382-Mbyte MK-250. The drive features a 15-Mbit/s data-transfer rate, 50 percent faster than many of its competitors. The Toshiba drive also revealed a new "center-stack" hybrid-servo design that integrates elements of a dedicated servo with advanced sector servo techniques. The company claims the servo reduces the drive's susceptibility to environmental extremes.

Half heights popular

A growing need for compact, reliable storage systems in lower cost personal and portable computers, CAD/CAM systems and low-end workstations is increasing the demand for 1.6-in., half-height 5¼-in. Winchesters. These units are filling a niche between the less-than-40-Mbyte commodity end of the Winchester market now being dominated by 3½-in. drives and the higher capacity, full-height over-300-Mbyte 5¼-in. products.



Using eight sputtered thin-film media platters and 15 ferrite read/write heads, Fujitsu's M2263E is one of the highest capacity 5¼-in. drives available, with 778 Mbytes of unformatted capacity. The M2263E transfers data at 1.87 Mbytes/s. Initially fitted with an ESDI, a SCSI version will be available later this year.

Present state-of-the-art drives in the 5¼-in. half-height arena offer 170- to 200-Mbyte capacities, use a dedicated closed-loop servo and come in ESDI or SCSI configurations. Besides their obvious space benefits, half heights offer a number of design advantages over their full-height counterparts, including greater shock tolerance, significantly lower weight, better thermal conductivity and lower power consumption.

According to Kai C.K. Sun, vice-president of engineering at Microscience (Mountain View, CA), low power consumption was one of the primary design goals in his company's Model HH2120. The 149-Mbyte half-height drive dissipates a mere 12 W thanks to extensive use of CMOS in the drive control electronics. A low-mass carriage and a

low-power, high-energy magnet in the drive's spindle motor also help keep power consumption down.

Miniscribe, generally known for its fairly slow but inexpensive, low-capacity full-height drives, entered the high-performance, high-capacity half-height arena last year with a 53-Mbyte unit called the 3053. In that drive, Miniscribe moved from a traditional linear actuator to a rotary voice-coil actuator to improve shock and vibration specs. This year, Miniscribe added a second drive to that line, the 71-Mbyte Model 3085. Like Micropolis' 1650/1670 series, the 3085 has a 35,000-hr MBTF.

A move to higher capacity

As full-height 5¼-in. Winchesters push to higher capacities and high volume, and as 3½-in. high-volume production moves into the 100- to 200-Mbyte range, 5¼-in. half heights will be forced to evolve to higher capacities. A number of vendors already offer 180-Mbyte units, and Control Data sells a 209-Mbyte unit in its Wren V line. Others, like Microscience, expect to unveil a unit with over 200 Mbytes by year's end.

But pushing far beyond that capacity in the tight half-height form factor will require some significant design changes. "I think we can push the present design to 240 Mbytes," says Sun. "Designing a 380-Mbyte half height is equivalent to developing the technology of a 750-Mbyte full height. A lot will depend on the supply of heads and media."

Sun sees future 380-Mbyte half heights using the same servo circuits as present models. But the thermal and vibration penalties from stacking four disks in a half-height box may force designers to complement the dedicated servo with some embedded servo information to correct top surface positioning errors. He expects designers to turn to some form of constant density recording to extend capacities and to turn to a look-ahead cache to boost throughput.

Price squeeze at low end

Seagate (Scotts Valley, CA) continues to dominate the low-end of the 5¼-in. Winchester market with a wide range of full-height and half-height models. Recently, the company took an aggressive price stance on its 85-Mbyte, full-height 4096, lowering prices by $50. The 4096 family features a 28-ms access time with a linear voice-coil actuator, a dedicated closed-loop servo system and the company's own sputtered thin-film media.

That price trend may be short-lived, however. Pressured by the increasing devaluation of the dollar in Europe and the Far East and rising domestic costs, disk drive vendors expect across-the-board price increases in the latter half of 1988. □

COMPUTERS AND SUBSYSTEMS

VME single-board computers pack 88000 RISC processor

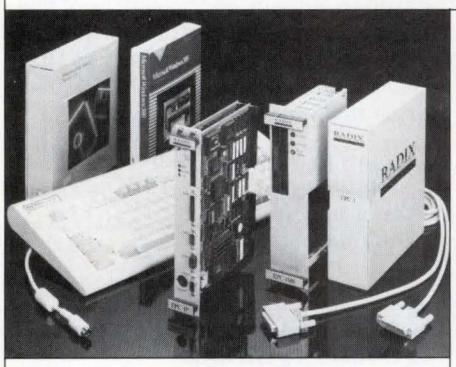
The first single-board computers out of the chute to be built around Motorola's 88000 reduced-instruction-set computer processor family are, not surprisingly, offerings from the company's own microcomputer division. The 20-MHz MVME181 and 25-MHz MVME181-1 processor boards for the VMEbus represent the minimal configuration for an 88000 system, with a single 88100 CPU and two 88200 cache memory management units—one for instructions and one for data. These entry-level RISC engines are being targeted at real-time control applications and small Unix machines serving up to about four users.

Beyond the high-performance interface that lies between the CPU and its caches, the boards optimize the data paths to their 8 Mbytes of parity-protected dynamic RAM and 512 kbytes of EPROM. The four on-board nonvolatile memory chips are accessed as individual bytes of a 32-bit word, for example. Two-way page-mode interleaving combined with a four-word state machine enhances the high-speed burst-mode capability of the DRAM. A burst-mode transfer between cache and DRAM requires between one and three wait states. The boards' DRAM is situated on a double-socketed daughter board, which prevents use of the adjacent slot in a VMEbus backplane. Future memory capacity improvements will place the DRAM on the single-board computer proper.

Both boards are capable of performing 8-, 16- and 32-bit data transfers and 16-, 24- and 32-bit addressing, and they include a level-3 bus requester and a seven-level interrupt handler. System controller functions are also provided, but can be jumper disabled. These include a four-level bus arbiter and a bus release on request mode. The boards also contain a system control register for control of board-level events such as interrupt masking. A read-only system-status register contains information on various board-level events.

The 6U-size MVME181 and MVME181-1 also come equipped with a battery-backed clock calendar and a pair of asynchronous RS-232C ports with modem control and programmable speeds from 50 bits/s to 38.4 kbits/s. Pricing is expected to be in the $9,000 to $10,000 range in as-yet-undetermined quantities.

Motorola Microcomputer Div
2900 S Diablo Way
Tempe, AZ 85282
Circle number 118



Embedded 80386 PC interfaces with VMEbus

A personal computer-compatible 80386-based computer, the EPC-1 is a two-module system with a full 32-bit VMEbus interface. An embedded PC, the system lets OEMs and system integrators take advantage of existing PC software while providing access to VMEbus memory, I/O and auxiliary processor products. The VXI modular instrumentation bus standard is also supported.

The system includes a processor module with a 16- or 20-MHz 80386 microprocessor and up to 4 Mbytes of dual-ported 32-bit zero-wait-state RAM. Built into the device are an Enhanced Graphics Adapter (EGA) controller with full support of a 640×480 Super EGA; floppy and small computer system interface hard-disk controllers; two RS-232 serial ports; a parallel printer port; and a keyboard port.

The disk module contains a 1.4-Mbyte, 3½-in. floppy disk drive and a ruggedized 40-Mbyte hard disk. Both modules fully comply with the IEEE-1014-87 VMEbus specification. The VXIbus extensions to VME include hardware support for geographical addressing, module configuration and description, and message passing. Both VXI and VME interfaces are implemented with proprietary gate arrays.

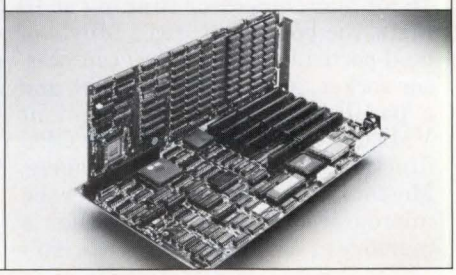
A companion software package serves as an interconnect between application software and the VMEbus, and provides device drivers for commonly used I/O boards. This interface allows programs running on an auxiliary processor, such as a 68020 single-board computer, to create, read and write DOS-compatible files on the disk modules, and to display data in Windows/386 through the CPU module. The software package also provides graphical, interactive configuration and verification capabilities for the user's system. The package is priced at $7,950.

Radix Microsystems
19545 Von Neumann Dr
Beaverton, OR 97006
Circle number 119

Baby 80386 mother board expands to 10 Mbytes

Offering direct compatibility with small- and full-sized IBM PC AT-type systems, the Baby 80386 mother board features zero wait states and a memory bus expandable to 10 Mbytes. The board is available in 16- and 20-MHz speeds with a choice of basic I/O system software and is socketed for an 80387 numerics coprocessor. The landmark benchmark performance rating for the 16-MHz model is 20.5, while the rating for the 20-MHz version is 25.5. A four-way associative cache memory expansion board provides enhanced processing speeds for memory-intensive programs such as the OS/2 and Unix operating systems. Prices start at $2,100.

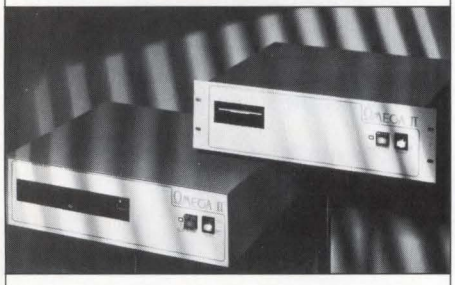
Micronics Computers
935 Benecia Ave
Sunnyvale, CA 94086
Circle number 120



COMPUTERS AND SUBSYSTEMS

68020-based workstation hosts 2 Mbytes of SRAM

Designed for the educational and OEM target system market, the Omega workstation supports a range of I/O cards and expansion options. The basic system incorporates a 12.5-MHz MC68020 microprocessor, 512 kbytes of zero-wait-state static RAM, five RS-232C serial ports and a parallel printer port. A small computer system interface and a floppy disk drive interface are included, as well



as a choice of professional or industrial operating systems. The top-of-the-line 16-MHz model features a 68881 math coprocessor and includes a 40-Mbyte Winchester hard disk with a 30-ms seek time; a 1-Mbyte, 3½-in. floppy drive; a 150-Mbyte, ¼-in. tape streamer; and 2 Mbytes of SRAM.

Windrush Micro Systems
North Walsham
Norfolk NR28 9SA, U.K.
Circle number 121

VMEbus CPU card functions as master/slave

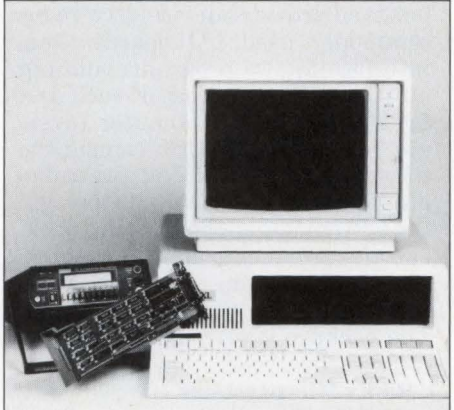
The VME-0286AT is a microprocessor module designed to function as a stand-alone microcomputer, as a single CPU system controller in a VMEbus system, or as one of several elements in a multiprocessor VMEbus configuration. Based on an 80286 16-bit microprocessor running at 10 MHz, the board features 1 Mbyte of dual-ported RAM, an 80287 coprocessor socket, a serial RS-232 port and a parallel port. A fully compliant VMEbus C.1 interface lets the CPU function as both master and slave. Mastership is acquired whenever the microprocessor generates either a memory or an I/O address that isn't mapped to the on-board memory and I/O devices or the IBM Personal System/2 bus, or the IBM PC AT bus. Slave mode is initiated whenever another VMEbus master generates an address that's mapped into the on-board RAM.

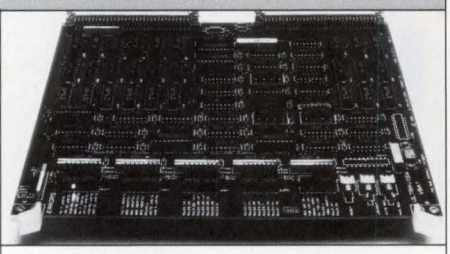
Logical Design Group
6301 Chapel Hill Rd
Raleigh, NC 27607
Circle number 122

Printed circuit board interfaces PS/2 to IEEE-488

Designed around an NEC 7210 interface chip, the uCMBC-488 interface board uses a single I/O card slot to provide IEEE-488/general-purpose interface bus talker/listener/controller capabilities on the IBM Personal System/2 Micro Channel bus. The board handles all system timing for up to 15 devices (a controller and 14 talker/listener devices) over a maximum bus length of 20 m. Data transfer is accomplished at speeds of 2 kbytes/s under normal mode operation and 400 kbytes/s for direct memory access mode. A resident DOS driver is supplied with the board, providing an interface to high-level languages such as Basic, Fortran, Turbo-Pascal and C. The board costs $299.

Metrabyte
440 Myles Standish Blvd
Taunton, MA 02780
Circle number 125





Bus and logic analyzers diagnose VMEbus faults

Used in conjunction with the manufacturer's logic analyzer, the VMEbus Analyzer identifies, automatically recognizes and triggers on 104 different bus timing faults in 27 classes. Faults, which illuminate a light-emitting diode (LED) on the analyzer, are timing violations of the VME protocols, including the specifications for signal stability during required intervals. After faults are discovered, the logic analyzer is triggered to determine the source of the fault. The board is a double-height VME board, made extra long so that the LEDs are easily observed. The price is $2,000.

Gould Electronics
3631 Perkins Ave
Cleveland, OH 44114
Circle number 124

VMEbus CPU boasts 15 MFlops

Using a pipelined coprocessor interface to achieve 8 million Whetstones/s for double-precision operations, the VME532 board-level computers come in 20-, 25- and 30-MHz versions. The manufacturer's NS32532 CPU is coupled with a Weitek WTL3164 floating-point data-path component through a 1-micron, double-metal CMOS floating-point controller that implements the Series 3200 instruction set. This interface allows full-speed operation of up to 15 MFlops without stalling to synchronize with the CPU. Five stages of instruction pipeline and a 20-stage first-in, first-out buffer let the CPU run in parallel with the floating-point unit.

National Semiconductor
2900 Semiconductor Dr
Santa Clara, CA 95052
Circle number 123

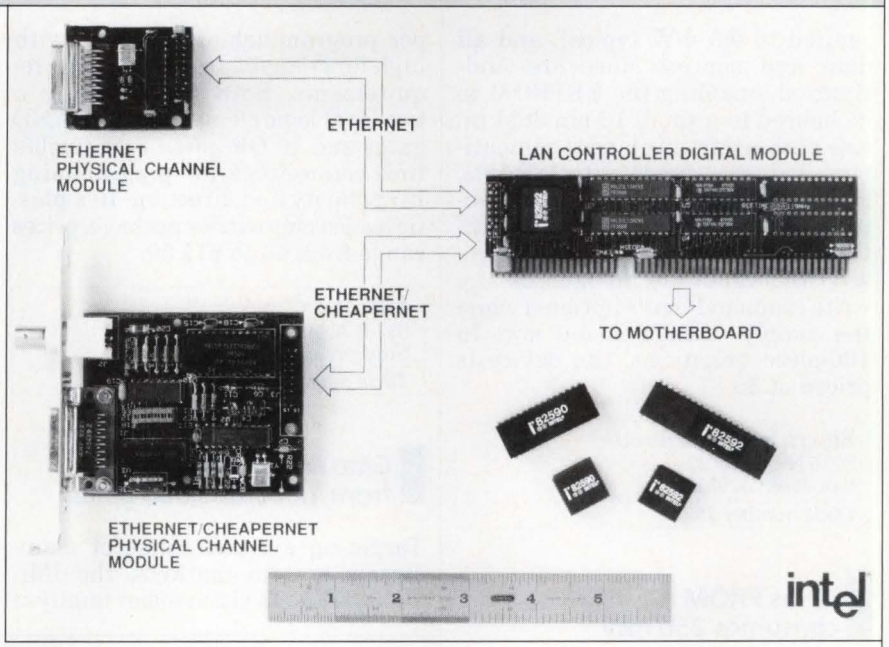
INTEGRATED CIRCUITS

LAN controller chips provide 20-Mbit/s serial bit rate

Two CHMOS LAN controller components, the 8-bit 82590 and the 16-bit 82592, are designed to implement LANs in personal computers. Requiring less than 5 in.^{2} on the mother board, the controllers provide serial bit rates of up to 20 Mbits/s for higher speed LANs.

The chips support a full range of existing and emerging industry-standard LANs including Ethernet, Cheapernet and twisted-pair Ethernet (TPE). Also included on each controller are 64-byte first-in, first-outs specifically designed for mother-board LAN solutions, and a deterministic collision resolution (DCR) mechanism for industrial and process-control networks. In distributed processing-type environments, such as factories and industrial settings, the DCR mechanism satisfies both peer-to-peer (or multistation-access) communication and real-time control.

The components support office LAN applications, such as add-in boards and low-cost LAN adapter products, and can also be used in proprietary LANs and other specialized areas. Both devices can be coupled with the manufacturer's Ethernet serial chip for an all-CHMOS solution for Ethernet and TPE applications. The 82592 is independent of local buffer memory, letting the controller use the host system's direct memory access for data transfer. As a result, a LAN solution based on the chip occupies less than 5 percent of the total mother board. In quantities of 1,000, the 8-bit controller is $31.25; the 16-bit version is $37.50.



Intel
3065 Bowers Ave
Santa Clara, CA 95052
Circle number 151

16-bit microsequencer supports 50-ns cycle time

Designed to control the execution of microcode in high-speed systems, the SN74ACT8818 is a TTL-compatible, 16-bit microsequencer that can address up to 64 kwords and perform various sequencing operations such as multiway branching and conditional subroutine calls. The device can be used in conjunction with array processors, high-speed I/O controllers and graphics-engine, display-list processors in high-end CAD/CAE workstations. In addition, the chip can support a 50-ns system cycle time, and has applications in accelerator boards, superminicomputers, LANs and interface devices. The device's three-I/O architecture facilitates three-way branches. Its dual register/counters support nested looping, as well as a single-cycle decrement and branch loop. In 1,000-piece quantities, the price is $48.40.

Texas Instruments
PO Box 809066
Dallas, TX 75380
Circle number 153

Low-power gate arrays have 10-ns propagation delay

The uPD65000 series of low-power gate arrays provides between 858 and 5,632 gates for applications in industrial and consumer products. The CMOS series includes the 65007 with 858 gates, the 65014 with 1,656 gates, the 65026 with 2,457 gates, the 65033 with 3,360 gates, the 65045 with 4,320 gates and the 65052 with 5,632 gates. Propagation delays average 10 ns, and quiescent voltage is 0.01 μA, typical. Prices range from $1.70 to $11 each.

NEC Electronics
401 Ellis St
Mountain View, CA 94039
Circle number 154

EEPROM boasts 1 million write/erase cycles

A 5-V programmable, 32-×8-bit EEPROM, the SC22100 offers an endurance specification of 1 million write/erase cycles and a data-retention reliability figure of 25 years. Processed with a proprietary 2-micron CMOS floating-gate technology, the 256-bit device operates completely from a single 5-V supply and requires no external high-voltage source for programming. Power dissipation is

INTEGRATED CIRCUITS

limited to 0.5 mW typical, and all data and address lines are multiplexed, enabling the EEPROM to be housed in a small 18-pin dual in-line package that is pinout-compatible to industry-standard static RAMs, as well as to 8- and 16-bit microcontrollers. To prevent data modifications during power up or power down, a write-lockout circuit ignores any write command that's initiated while the supply voltage is too low. In 100-piece quantities, the device is priced at $5.87.

Sierra Semiconductor
2075 N Capitol Ave
San Jose, CA 95132
Circle number 152

40-ns PROM consumes 250 mW

A 16-kbit×8-bit CMOS PROM, the WS57C51B is a 40-ns device that's only 0.3 in. wide. Depending on performance requirements, the chip is available in three access times: 40, 45 and 55 ns for commercial versions; and 50, 55 and 70 ns for military parts. The PROM is MIL-STD 883C compliant and uses 250 mW of power at 10 MHz. Manufactured with a split-gate technology, the device lets users program with a specific code, and then erase and reprogram when necessary with a new code. This reprogramming capability is used for fine tuning and field updating systems. The price is $70.

Waferscale Integration
47280 Kato Rd
Fremont, CA 94538
Circle number 155

PAL chips boast 10-ns propagation delay

Two high-speed programmable array logic-type (PAL-type) families and a fast programmable logic array (PLA) device feature propagation delays of 10 ns and 12 ns, respectively. Each PAL-type family contains four devices, one with eight combinatorial outputs and three that offer a choice of eight, six or four on-chip registers. The PLAs come in 20- or 24-pin versions and specify a 6-ns propagation delay per programmable logic level with high functionality to meet special requirements. Both PLAs feature a two-level logic element with 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction. In a plastic leaded chip carrier package, prices range from $5 to $11.50.

Signetics
811 E Arques Ave
Sunnyvale, CA 94088
Circle number 157

Gate array family ranges from 1,600 to 8,000 gates

Targeting a broad range of mainstream system markets, the IMI-7000 series is a six-member family of 1.5-micron CMOS gate arrays covering applications from 1,600 to 8,000 gates. The double-metal, oxide-isolated silicon gate arrays are fully autoroutable with up to 100 percent utilization guaranteed. For military uses, the arrays span the full MIL ambient temperature range of −55° to +125° C, with complete MIL-STD 883 screening available for all six devices. The devices come in a wide package selection including epoxy and side-brazed dual in-line packages (22 to 64 pins), leadless chip carrier, plastic leaded chip carrier and J-leaded chip carriers. Prices range from $3 to $38.

International Microcircuits
3350 Scott Blvd
Santa Clara, CA 95054
Circle number 156

DESIGN AND DEVELOPMENT TOOLS

Digital signal processing development tool offers nonintrusive operation

An in-circuit emulator designed specifically for digital signal processing (DSP) systems, the Model E-232-DSP-10 is nonintrusive and completely emulates the target system. Under interactive control, the system provides real-time transparent emulation of TI's TMS320C10 family of DSP microcontrollers at 32 MHz, including EPROM, universal asynchronous receiver-transmitter (UART) and extended-address internal RAM, without any restrictions.

The emulator offers sophisticated event definitions that can be used as breakpoints or trace controls. Three simultaneous sets of events are defined in terms of any or all of the following parameters: addresses; CPU operations including read, write, I/O, direct memory access and opcode fetch; data patterns; and external inputs. In addition, events can be counted and/or delayed by the use of two 16-bit pass counters. An eight-level hardware sequencer is available to sequentially trigger to, from, or between any breakpoint event sets or pass counter values. Other breakpoints can be triggered in the event of a trace-full condition, a watchdog timer out or an illegal opcode fetch.

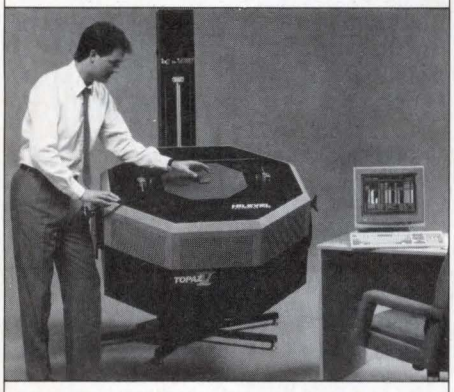
Other important features of the DSP emulator include in-line symbolic assemblers and disassemblers, two banks of 8-kbyte overlay program memory for virtual memory operation, and an eight-channel user logic state analyzer. Performance-analysis hardware and software allow the target system designer to evaluate the target code's efficiency, with both graphic and tabular displays. Various windows may be called up to display internal registers, internal and external memory, source code with single step, breakpoints, fast calls and skip calls, as well as user-defined setups. Single-unit price for the emulator is $5,995.

Signum Systems
1820 14th St
Santa Monica, CA 90404
Circle number 135

DESIGN AND DEVELOPMENT TOOLS

ASIC verifier features 110-MHz test rate

An application-specific IC verification system offering tester-per-pin architecture, the Topaz-V uses a proprietary function called virtual vector memory to test devices requiring over 1 million test vectors. Fifth-generation architecture allows individual software control of each I/O pin with test rates of 110 MHz and clocking to 220 MHz. Initially, the system will provide up to 320 I/O pins with expansion to 544 pins as a scheduled option. Pin-to-pin skew is



guaranteed less than ±500-ps across all pins, and driver-slew rate is over 1.5 V/ns. The tester-per-pin architecture allows individual pin control of I/O direction, data format, logic levels, compare thresholds and masking. Providing a 16-Mbyte RAM interfaced to pin electronics, the virtual vector memory feature shows a depth of 28 million vectors divided by the number of pins used. The system price ranges between $1,000 and $1,600 per I/O pin.

Hilevel Technology
31 Technology Dr
Irvine, CA 92718
Circle number 136

Micro analyzer supports 68020

The Vmetro personal micro analyzer (PMA) is a stand-alone development tool designed for the testing, debugging and performance measuring of 68020-based systems. A compact logic analyzer, the device features a disassembler for 68020 program code, a cache hit-rate indicator, address distribution of program and data references, and time-tag functions for performance measurement. The PMA includes logic-state analysis on the microprocessor, providing 2,000 words of program trace or processor bus trace (88 signals) with triggers and store qualifiers.

Vmetro
2500 Wilcrest
Houston, TX 77042
Circle number 137

Development tool system provided by emulator

An addition to the manufacturer's HP 64700 series of emulators/analyzers, the Logic-Analyzer-on-a-Chip is part of a development tool system for the Intel 80C196-KA microcontroller. The development tools consist of a stand-alone emulator and emulation bus analyzer, and offer an optional 16-channel analyzer that functions as a 100-MHz state analyzer as well as a 25-MHz timing analyzer. Special features include real-time, no-wait-state execution of up to 12 MHz in emulation or target memory; 64 kbytes of dual-ported emulation memory; analysis trace displays of bus-cycle activity; and tracing capabilities on data, address, status, ports and I/O. Prices for the tools start at $13,200.

Hewlett-Packard
3000 Hanover St
Palo Alto, CA 94304
Circle number 138

CAE/CAD/CAM system runs on Unix workstation

Operating on a Hewlett-Packard 32-bit Unix workstation, the CR 3000 CAE/CAD/CAM system offers comprehensive digital, hybrid and analog design capabilities with a unified data base structure. The system features mouse input with multiwindowing, pop-up menus, C software and a LAN architecture. A gridless electrical design system, the software lets designers inscribe true arcs and curves with up to 1 micron of accuracy without vector lands. Prices range from $70,000 to $140,000.

Zuken America
24 New England Executive Park
Burlington, MA 01803
Circle number 139

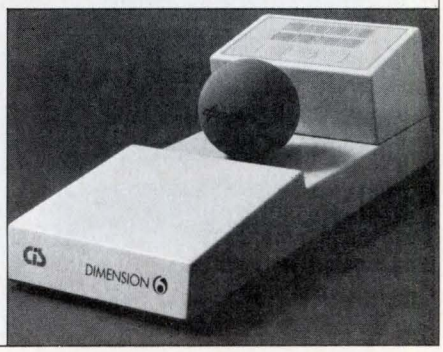
MAJOR SYSTEM COMPONENTS

Graphics control device uses optical sensor technology

A graphics control device that uses optical sensor technology, the Dimension 6 Control Ball allows manipulation of real-time or graphically simulated three-dimensional objects by the user with one hand.

Designed to overcome the 3-D limitations of conventional graphics tablets, mice, trackballs, knob boxes and joysticks, the device lets the user judge the screen object's X, Y and Z coordinates, as well as rotate the object on each axis. In all, the control ball contends with six total "degrees of freedom," including the X, Y and Z coordinates, roll, azimuth and elevation. Function buttons for rotation, translation and domination motion directions are provided, along with user-programmable settings for object sensitivity and speed control. In addition, the device allows the generation of "mixed motions" instead of simply controlling the areas around or along the main axis.

The principal part of the control system is an optically working force/torque sensor integrated in a sphere. This sensor measures forces



MAJOR SYSTEM COMPONENTS

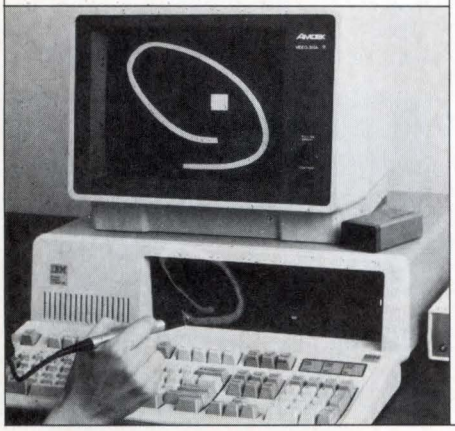
and torques applied to the sphere and converts the resulting analog values to a digital format, which is then sent to the host system via an RS-232 interface. A keypad with 11 buttons permits the selection of different operating modes, while a daisy chain function makes it possible to connect different types of input devices in one serial line. Other features include a built-in power supply, selectable baud rate and software protocols.

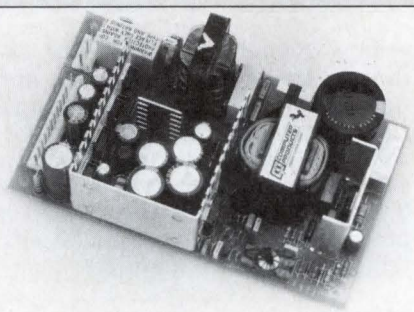
CIS Graphics
Two Robbins Rd
Westford, MA 01886
Circle number 158

Remote-cursor control system has no desktop footprint

The Optimouse remote-control cursor system consists of a miniature real-time digital image processor that automatically tracks the position of a handheld pointer in two dimensions. The pointer position may be directly interfaced to any computer for cursor control on a system VDT. A miniature two-dimensional imaging sensor is positioned near the computer terminal, viewing the area around the operator. The sensor is linked to a real-time digital imaging processing system that tracks the pointer and maps the movement onto the coordinate system of the terminal screen. Command entry is accomplished via a push button built into the pointer.

Iscan
125 Cambridgepark Dr
Cambridge, MA 02238
Circle number 162





110-W switchers combine power density and high MTBF

A family of 110-W universal input switching power supplies, the NFS110 series will accept any input voltage from 85 to 264 V_{ac} without jumper wires or switches. Calculated mean time between failures is 125,000 hours with power density exceeding 2 W/in³. Total output power at 50° C ambient temperature is 80 W with convection cooling and 110 W with forced air cooling. Typical efficiency is 70 percent, and line regulation is ±0.1 percent max, with total regulation typically better than ±3 percent. Seven models are offered with outputs ranging from −15 to +24 V. Prices start at $141.

Computer Products
2900 Gateway Dr
Pompano Beach, FL 33069
Circle number 160

500-V MOSFET boasts 50 A of usable current

Based on the manufacturer's Power MOS IV technology, the APT5010 is a 500-V MOSFET with 50 A of usable current and 0.1Ω of "on" resistance for power supply and motor-control circuits in military and commercial systems. The device has an input capacitance (Ciss) of 6,000 pF and is built on a 338-×588-mil die in a hermetically sealed 0.33-×1.125-×1.625-in. package. Designed for easy manufacture and assembly, the MOSFET can be mounted directly to a heatsink without isolation requirements. The price is $149.88.

Advanced Power Technology
405 SW Columbia St
Bend, OR 97702
Circle number 163

LCDs offer near-CRT quality

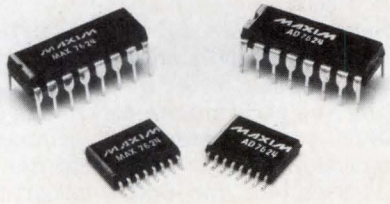
Two liquid crystal displays (LCDs) use chip-on-flexible circuitry and super-twisted nematic fluid for near-CRT quality. Both have a thin profile and come in multiple sizes for a variety of applications. The first, Model EG7005, has a resolution of 640×200 pixels and is designed for medical instrumentation and process controls. A higher resolution of 640×400 pixels is offered by Model EG8001, which can be used as a CRT replacement for computers or other sophisticated displays. Features include large-capacity graphics type capable of displaying alphanumerics, special characters, graphs, charts and patterns, and a 4-bit parallel chip.

Epson America
3814 Kashiwa St
Torrance, CA 90505
Circle number 159

Multiplying D-A converter works with TTL inputs at 15 V

A CMOS 8-bit buffered multiplying digital-to-analog (D-A) converter, the MAX7624 works with TTL or +5-V CMOS-level digital inputs when operating from a +12-V or +15-V supply. The device features a data latch to simplify microprocessor interfacing and uses thin-film resistors to achieve ±½ least significant bit relative accuracy with guaranteed monotonicity over temperature. Applications for the chip include digitally programmed gain or attenuation, microprocessor-controlled function generation, and automatic system calibration of gain and offset. Prices start at $3.15.

Maxim
120 San Gabriel Dr
Sunnyvale, CA 94086
Circle number 161



PC-to-FAX system sends full-size CAD drawings

CAD-Fax is a personal computer-to-FAX hardware/software package designed specifically for CAD environments. The system transmits CAD drawings (A to E or nonstandard formats) and design data directly from a PC to a FAX machine. A high-speed data-transfer capability lets users transfer CAD and other files between PCs over ordinary phone lines at up to 10 kbits/s.

Consisting of software and an add-in FAX modem board for the IBM PC, IBM Personal System/2 and compatibles, the system transmits any CAD file written in Hewlett-Packard Graphics Language or AutoCAD to any Consultative Committee on International Telephone and Telegraph Group III FAX machine. Plot files are automatically converted to FAX format and transmitted over ordinary phone lines at 9,600 bits/s. If line quality is poor, tranmission rate is dropped to 7,200, 4,800 or 2,400 bits/s. By avoiding a FAX machine's scanner, which frequently can't detect the fine detail common to CAD drawings, CAD-Fax takes advantage of the receiving machine's 200-dot/in. printer, letting users send plotter-quality documents via facsimile.

Drawings that are too large for a FAX machine to print are divided into 8½-in. strips and sent with alignment markers letting the recipient reconstruct the original full-sized drawing. Header messages of up to 400 characters may also be sent, eliminating the need for separate cover sheets. By effectively turning any FAX machine into a medium-resolution plotter, the package lets engineers ease plotter bottleneck by using the the office FAX machine as a standby plotter with the same scale as the original drawing. The price is $1,995.

Gammalink
2452 Embarcadero Way
Palo Alto, CA 94303
Circle number 126

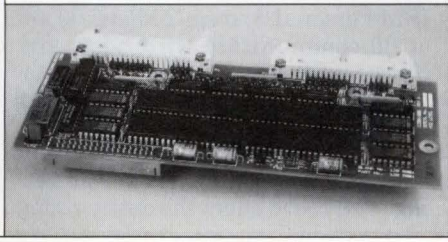
SNA gateway communicates with DSA network

The Open System Facilities/SNA gateway is an SNA facility that will let computers on Honeywell's Distributed Systems Architecture (DSA) network communicate with IBM SNA host computers. The gateway will offer a range of interoperability capabilities with IBM mainframe computers, including high-speed file transfer and terminal-access support. The product consists of optional software modules that reside on Honeywell Bull's Datanet 8 series. The communications link between the Datanet 8 and the IBM 37X5 front-end processor may be either a direct link or via an X.25 packet-switched public network. The gateway lets users of bisynchronous terminals or personal computers emulating these terminals on a DSA network access IBM host applications across an SNA network, including time sharing, transaction processing and network management.

Honeywell Bull
300 Concord Rd
Billerica, MA 01821
Circle number 130

iSBX communications board hosts eight channels

The CCSBX/008 is a serial communications iSBX board that provides eight RS-232 asynchronous ports with full-duplex operation, modem control and interrupt generation on each channel. Baud rates are independently software-programmable within the range of 110 to 19,200 baud. Unix and iRMX drivers are also supported. The board costs $495.



Concurrent Technologies
25401 Cabot Rd
Laguna Hills, CA 92653
Circle number 128

Correction

On page 117 of our July issue, we gave the incorrect model number and output drive specifications for VME Microsystem's analog output board. The correct model number is VMIVME-4101, not VMIVME-4100. The new product will drive up to 16 channels of analog output at maximum load current of 10mA simultaneously. We regret the error and apologize for any inconvenience it may have caused.

DATA COMMUNICATIONS

LAN server based on 80386 processor

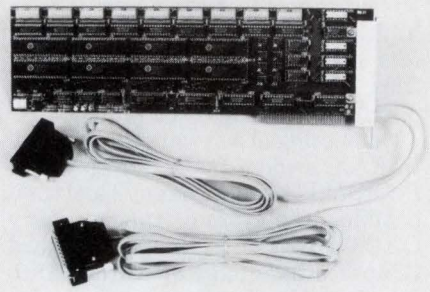
Offering a choice of hard disk sizes (170, 310 or 600 Mbytes), the Lifeserver is a LAN server based on a 20-MHz 80386 micrprocessor. The AT-compatible tower system features 2 Mbytes of RAM (expandable to 16 Mbytes), two floppy disk drives (360 kbytes or 1.5 Mbyte), a 60-Mbyte streaming tape cassette, a monochrome monitor and a hard disk drive. Prices start at $18,170.

Univation
Gibraltar Court
Milpitas, CA 95035
Circle number 127

Fiberoptic module connects to EIA-530

A pair of fiberoptic communications modules, the Micro M6110/M6120s can connect two EIA-530 compatible devices over a 2,000-m fiberoptic link. The device multiplexes clock, data and all control signals for transmission on the link, making it transparent to any variation of EIA-530 control implementation. Companion modules with RS-232, RS-499, V.24 and V.35 interfaces allow conversions across the link. Available with data-terminal equipment and data-circuit-terminating equipment connectors, the device measures 0.8× 2.1×3.4 in. and can be supplied in a suppressed electromagnetic and radio-frequency interface configuration for applications such as Tempest.

Versitron
9005-8 Junction Dr
Annapolis Junction, MD 20701
Circle number 129



PC board provides eight RS-232 channels

An eight-channel serial RS-232 board for IBM PCs, PC XTs, PC ATs and compatibles, the MS-100 communications card utilizes eight 16450 universal asynchronous receiver-transmitters to provide eight independent channels. Each channel is capable of 19.2 kbaud and can be individually addressed, allowing installation without conflicting with additional peripheral devices. The board, which takes one expansion slot in the PC, is capable of two interrupt configurations. With the first option, all eight signals are sent to a control register, which in turn sends one interrupt signal to the computer. This register is then read to identify the channel that generated the interrupt. With the second option, six of the eight interrupt lines are configured the same as the first option. The additional interrupt lines are configured as IRQ3 and IRQ4 to provide COM1 and COM2 compatibility. The price is $595.

Qua Tech
478 East Exchange St
Akron, OH 44304
Circle number 133

Workstation controller combines PS/2 and Netware

The NI9210 is a workstation controller that permits up to 16 connections to a variety of hosts, letting any IBM Personal System/2 Model 50, 60 or 80 communicate with hosts and Netware file servers using the Transmission Control Protocol/Internet Protocol (TCP/IP). The product is supplied with either 16 or 64 kbytes of dual-ported RAM for packet buffering. The board offers the entire range of TCP/IP protocol capability including remote log-on, file-transfer capabilities, electronic mail, network testing and back-up utilities. The address description file virtually eliminates the configuration process, while on-board diagnostics verify proper operation. The price is $895.

Micom Systems
155 Swanson Rd
Boxborough, MA 01719
Circle number 131

Internal modem for PCs sends 9,600 bits/s

Compatible with IBM PCs, PC XTs, PC ATs and IBM Personal System/2 Model 30, the Hook-Up 9600 is an internal 9,600-baud modem that's compatible with the Hayes command set. Other supported standards include the Bell 103 J and 212A, as well as Consultative Committee on International Telephone and Telegraph V.29 in half-duplex form. The device operates in either synchronous or asynchronous modes, using the Microcom Networking Protocol's error-control algorithm up to level 6. Diagnostics provide remote digital loopback and analog/digital loopback. Standard features include auto-dial, auto-answer and auto-redial, as well as remote operation and automatic fallback capabilities. The board costs $795.

Computer Peripherals
667 Rancho Conejo Blvd
Newbury Park, CA 91320
Circle number 134

Trademark Information

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PAL and PALASM are registered trademarks of Monolithic Memories Inc.

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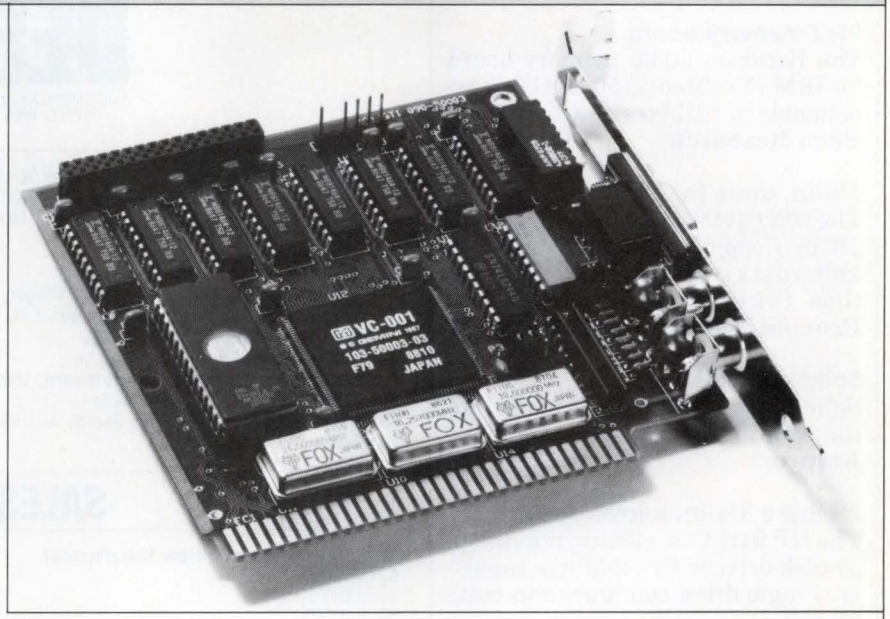
386, 386SX, 376, Intel386, iRMK, iRMX, and ICE are trademarks of Intel.

Enhanced Graphics Adapter card achieves high-level integration



The Omega 800 Plus Enhanced Graphics Adapter (EGA) graphics board for IBM PCs, PC XTs, PC ATs and compatibles uses the manufacturer's VC-100 multistandard video controller chip to achieve a high level of integration. The board is complete with utilities and drivers for popular graphics and text application programs including Autocad, Pagemaker, Lotus 1-2-3, Symphony, GEM, Exel, Ventura Publisher and Wordperfect. The controller offers all standard EGA, Color Graphics Adapter, Monochrome Display Adapter and Hercules text modes, plus 24 enhanced combinations from 80 to 132 columns ×21 to 74 rows.

Along with standard graphics resolution, the following enhanced graphics resolutions are available in all 16 of 64 colors: 960×350, 1,056×350, 640×480, 752×420 and 800×600 pixels.

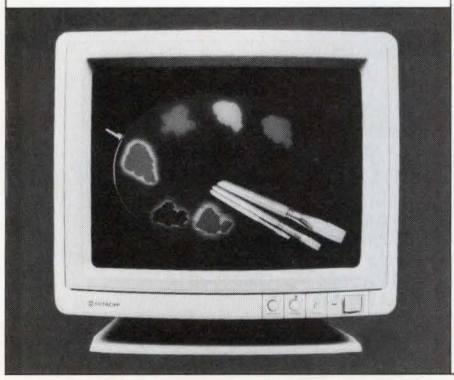
The VC-100 custom controller chip, around which the board is built, is a 160-pin device with all registers in all modes fully implemented in hardware. Built-in auto-mode switch logic with software-selectable video modes and five software-addressable clock signals of up to 34 MHz are featured.

The board costs $299 and supports virtually all monochrome, enhanced color and multifrequency monitors.

Gemini Technology
11-11151 Horseshoe Way
Richmond, B.C. Canada V7A 4S5
Circle number 140

Processor boasts a 100,000, 20-pixel vector/s speed

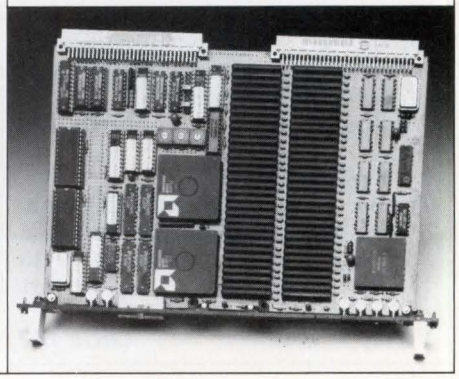
Advanced graphics processors for the IBM Personal System/2 Models 50, 60 and 80, the Spectra series is based on Advanced Micro Devices' Quad Pixel Dataflow Manager chip to give a 100,000, 20-pixel vector/s drawing speed. The series has full Video Graphics Array compatibility using a pass-through mode with a multisync or an IBM 8514 monitor. Resolutions of 1,024×780 pixels, interlaced or noninterlaced, are featured, with a screen-refresh rate of 60 kHz (noninterlaced). Screen flood is at 35 million pixels/s with 16 or 256 colors available from palettes of 4,096 or 16.7 million colors, respectively. The utilities diskette supplied with the series includes drivers for application programs such as Autocad's Release 9 and Computervision's Personal Designer series. Prices start at $1,999.



Vermont Microsystems
29 Church St
Hungerford, Berks RG17OJH, England
Circle number 142

Graphics board brings high performance to VMEbus

Based on two Quad Pixel Dataflow Manager chips from Advanced Micro Devices, the OPAC graphics board houses a 2-Mbyte frame buffer with a dotclock of up to 125 MHz. Text-update rates above 10,000 characters/s are featured, as well as a bit block transfer speed above 16 Mpixels/s, a refresh rate of 1,280-×1,024-pixels at 60 Hz, and 256 software-selectable colors out of 16.8 million. Up to three of the boards can be cascaded for color resolution of up to 24 bits/pixel. The device can process command sequences stored locally anywhere in its frame-buffer memory, and offers drawing functions such as arc, point, circle, line, string, filled rectangle and triangle, and flood fill, along with software-selectable antialiasing. Prices for the board start at $3,100.



American Eltec
569 S Marengo Ave
Pasadena, CA 91101
Circle number 143

PRODUCT BRIEFS

PS/2 memory board
The Bocaram 50/60 memory board for IBM PS/2 Models 50 and 60 is expandable to 4 Mbytes. Starts at $645.
Boca Research *Circle 171*

5¼-in. drive for PS/2
The PXF1200 1.2-Mbyte external 5¼-in. floppy for PS/2s features 500 kbit/s data transfer and 3-ms access time. Price is $450.
Procom Technology *Circle 172*

Solid-state disk
Solid State Disk can be plugged into the Ampro single-board computer.
Ampro *Circle 173*

2-Mbyte 3½-in. microfloppy
The HP 9122C is a 3½-in. microfloppy disk drive with a 2-Mbyte capacity. Single-drive configuration costs $1,150.
Hewlett-Packard *Circle 174*

High-resolution display controllers
The UDC-3400 series of high-resolution display controllers features up to a 1,280-×1,024-×34-bit/pixel display for Sun-3 workstations. Prices start at $3,995.
Univision Technologies *Circle 175*

Optical storage for Unix systems
LaserBank optical Winchester WORM storage systems offer capacities of up to 1.6 Gbytes for Unix- and Xenix-based systems.
Micro Design International *Circle 176*

Tape coupler for Q-Bus
The DQ153 tape coupler can interface up to four ½-in. start/stop, streamer or cached streamer tape drives to Q-Bus systems. Price is $1,200.
Dilog *Circle 177*

17-bit A/D converter
The AH30217 A/D converter features 17-bit resolution, provides 300 conversions/s and has differential linearity of ±0.2 ppm FSR.
Analogic *Circle 178*

1.5 kVA on-line UPS
The Benchmark UPS Model 15A uninterruptible power supply serves a 12-A load and accommodates 90- to 140-V input fluctuations. Prices start at $1,795.
Viteq *Circle 182*

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Seoul, Korea
Tel: 776-2096 Telex: K27117 DOOBEES
Fax: 755-9860

CALENDAR

CONFERENCES

Oct 3-5
IEEE International Conference on Computer Design
Rye Town Hilton, Port Chester, NY. Conference will focus on the design and use of VLSI in computers and processors, with particular emphasis on interactions among system, logic circuit, memory and physical designs; architecture; software; CAD; testing; and VLSI technology.
Information: Michael R. Wayne, IBM, Box 390 D/B34 B/901-3, Poughkeepsie, NY 12602, (914) 432-5211.
Circle 195

Oct 3-6
Electronic Imaging '88
World Trade Center, Boston, MA. Presenters of papers at this conference will discuss advances in the technical state-of-the-art or unique applications for electronic imaging components and devices in imaging systems and products.
Information: Richard Murray, Institute for Graphic Communication, 375 Commonwealth Ave, Boston, MA 02115, (617) 267-9425.
Circle 196

BUSCON ***Oct 4-6***
Buscon/88-East
Javits Convention Center, New York, NY. Specifically targeted at system-backplane and integration issues, sessions at this conference will stress board design and integration, as well as matching bus, microprocessor and peripheral-chip performances to various boards, operating systems and real-time software.
Information: Buscon/88-East, Dave Caplin, Project Director, Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06854, (203) 838-3710. **Circle 197**

Oct 4-6
International Display Research Conference
Hyatt Islandia, San Diego, CA. Sponsored by the IEEE Electron Devices Society, the Society for Information Display and the Advisory Group on Electronic Devices, with rotating locations among Asia, Europe and the United States, this meeting will emphasize research and early development aspects of display technology.
Information: Palisades Institute for Research Services, Attn: IDRC, 201 Varick St, New York, NY 10014, (212) 620-3388. **Circle 198**

Oct 9-13
Chautauqua on Productivity in Engineering and Design
Newport Marriott Resort Hotel, Newport, RI. "CAE, the promise and the reality" is the theme of the fifth annual international conference for the computer-aided design community. Conference participants—software and hardware developers, CAE managers and CAE integrators—will present 12 technical sessions, panels and roundtable discussions.
Information: Stephen Jordan, Jordan, Apostal, Ritter Associates, Administration Bldg 7, Davisville, RI 02854, (401) 884-3014. **Circle 199**

ISA ***Oct 16-21***
ISA International Conference
The Astrodome Complex, Houston, TX. More than 100 two-hour technical sessions plus additional panels, roundtable discussions and tutorials will be presented at this annual Instrument Society of America conference on instrumentation and control. Topics will include CAE/CAD, intelligent automation, knowledge-based systems, real-time expert systems, CIM and human interface.
Information: Meetings Dept, ISA, PO Box 12277, Research Triangle Park, NC 27709, (919) 549-8411.
Circle 200

MILCOM 88 ***Oct 23-26***
Milcom '88
San Diego, CA. "Twenty-first century military communications—what's possible" is the theme of this year's IEEE Military Communications Conference. The conference will stress emerging challenges, architectural concepts, techniques and technologies in MIMIC/RFLSI, VHSIC/UHSIC, wafer-scale integration, GaAs, HEMT, fiberoptics, optical computing, communications and artificial intelligence. Some sessions will be classified as DOD Secret.
Information: Milcom '88, PO Box 2568, Redondo Beach, CA 90278, (213) 297-8774. **Circle 201**

Oct 25-28
Systec/88
Munich, Germany. This conference and trade fair will cover technical and scientific applications of computer integration in manufacturing, including CIM, CAE/CAD, process computer control, robot control, data acquisition and expert systems.
Information: Munchener Messe- und Ausstellungsgesellschaft mbH, Messegelande Postfach 12 10 09 D-8000 Munchen 12, Germany, (089) 51 07-0.
Circle 202

SEMINARS

Oct 4-6, 17-21
Neural Networks
UCLA, Los Angeles, CA. Separate courses—Optical Neural Computers and Neural Networks: Translating Theory to Real-World Applications—will deal, respectively, with optical implementation of neural net models and with pattern recognition, image processing, surveillance, multiple-target-tracking autonomous vehicles and massively parallel processing.
Information: UCLA Extension, PO Box 24901, Los Angeles, CA 90024, (213) 825-1047. **Circle 203**

Oct-Nov
Data Acquisition and Analysis Using Next-Generation Personal Computers
Apple Training Centers in various U.S. and Canadian cities. In addition to hands-on instruction, free seminars will include presentations on elements and selection criteria for a personal computer-based data-acquisition system; hardware; data-capture, analysis and presentation software; and the selection of software to match the application.
Information: Cindy Bamsch, National Instruments, 12109 Technology Blvd, Austin, TX 78727, (512) 250-9119. **Circle 204**

Electron-beam probing now viable for VLSI diagnostics

Art DeSena
President, ADS Associates

Despite the exceptional promise of electron-beam (E-Beam) probing technology for device diagnostics, it's just now starting to make its way out of the laboratory. E-Beam probing is based on the principle that a finely focused beam of electrons can be used to measure the voltage waveform on an interconnecting conductor inside a VLSI device. One significant problem that's kept E-Beam probing off the production floor has been that to function properly, the device-under-test (DUT) must be in a vacuum so that the electron beam can travel unimpeded by gas molecules. Engineers have had difficulties introducing electrical signals into the vacuum chamber to exercise the DUT. Now, however, the IDS 5000 E-Beam probing system from Schlumberger/ATE (San Jose, CA) directly addresses the issue of exercising devices while they're in a vacuum chamber.

The IDS 5000 probing system is a traditional E-Beam technology, with additional features, that operates in the familiar workstation environment. The key element in the IDS 5000 is an electron optical system, which includes a scanning electron microscope (SEM), a probe card and a vacuum chamber. This system is packaged to include a high-speed (100-ps) beam-blanking unit and a high-accuracy magnetic collimation electron energy filter, neither of which is customary in standard SEMs. The electron optical column was designed specifically for the needs of voltage contrast probing (for which a very low voltage beam is required), rather than for the more general requirements of scanning electron microscopy. The column is a two-lens design that measures only 14 in. long, compared to the 40-in. columns of most SEMs. Far from cumbersome, the column is packaged out of sight beneath the workstation tabletop.

The electron optical system allows convenient and reliable device setup and high measurement accuracy with wafers and packaged parts. The lens system produces a focused electron beam small enough to probe the advanced device geometries, and it incorporates an accurate secondary electron energy analyzer, which eliminates the local field effect. The ability of the analyzer to operate without a strong extraction field makes measurement through passivation or through a dielectric both routine and reliable. The column is located beneath the DUT vacuum chamber on a precision positioning stage, giving the user direct access to the DUT. There are no mechanical adjustments necessary, since all alignment is performed electronically.

The benefits of E-Beam probing

Shrinking device geometries are making conventional debug techniques both inadequate and cumbersome. With the IDS 5000, however, engineers can probe submicron geometries, make voltage measurements, display waveforms, and then compare voltage-contrast images and layouts. The system's automatic beam alignment gives precise measurements that can be repeated without user intervention.

The IDS 5000 effectively links electron-beam testing with existing CAD/CAE tools. Integrating CAD/CAE information into the E-Beam probing environment lets design engineers use design information to evaluate the performance characteristics of silicon prototypes. A CAD layout and a schematic net list can each be displayed as a separate window on a single high-resolution color graphics monitor, while a third window displays a corresponding real-time image of the chip itself. A fourth window provides an oscilloscope tool that displays waveforms corresponding to the node being probed. The system uses signal-averaging techniques to improve the signal-to-noise ratio, ensuring high-integrity waveforms that may be stored for later retrieval and compared against live waveforms on another device under analysis.

The IDS 5000 effectively links electron-beam testing with CAE/CAD tools

■ ■ ■

The system includes tools that make use of CAE/CAD data developed on an engineering workstation. Noncontact E-Beam probing, in which no contact with the device being probed is necessary, offers design, production and test engineers significant advantages for debug, characterization and failure analysis. The nondestructive E-Beam probe, which uses low voltages, also eliminates the capacitive loading problems associated with mechanical probes and doesn't alter the device characteristics or destroy the device.

Diagnostic tools aid in probing

The IDS 5000 includes four diagnostic tools: a net-list (or schematic) tool, a layout tool, an SEM tool and a scope tool. The net-list tool, which lets designers scan through a net-list text file, is interactively linked with the layout tool and contains the CAD data on circuit connectivity and cell hierarchy. This tool can save significant time in locating the net of interest

without the need to refer to paper schematics. Input formats such as Spice, SDL (system descriptive language) and EDIF (Electronic Design Interchange Format) are supported, making it easy to interface with popular CAE systems such as those from Daisy Systems, Mentor Graphics and Valid Logic Systems.

The layout tool provides a display of the chip's CAD data base. In conjunction with the SEM tool, the layout tool is a powerful navigational aid that lets designers locate a specific signal. Designers can highlight a particular net or device within the chip on a cell-by-cell basis, eliminating the need for hard-copy plots. Panning and zooming capability in the system allows complete control over the displayed layers.

The principle of voltage contrast causes differing surface potentials to result in light and dark areas in an SEM image. Simple faults stand out clearly, thus aiding the debug process. Zooming in on a faulty portion of the device with the SEM tool alerts the layout tool to the same area in the data base so the designer can easily find the name of the signal or cell affected.

Through automated control of the E-beam pulsing circuits, the scope tool permits straightforward waveform acquisition. Accurate digital time-delay circuits provide a low jitter time base. The combination of a 100-ps rise time and automatic signal averaging results in high performance measurements. With the scope tool, a designer can display and store waveforms for submicron geometries, and thus facilitate the debug process.

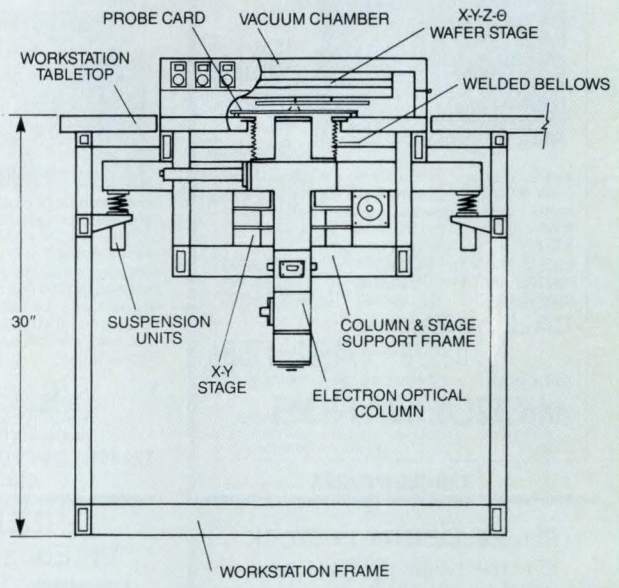
Design debug more efficient and accurate

The IDS 5000 is a versatile tool that lets VLSI diagnosis, characterization and failure analysis take on entirely new forms. It allows observation of the real chip in action and real-time voltage measurement of its activity. Since the electron beam is loadless and noncontacting, and because it doesn't alter device characteristics, it provides accurate measurements.

In addition to observing circuit behavior in real time, designers can navigate through the CAD layout and net list simultaneously, and observe and store waveforms for detailed circuit analysis. The IDS 5000 lets design and test engineers go beyond simply locating a faulty node to uncover the cause of the problem. They can then modify the design as necessary.

When conducting failure analysis, the electron optical system design lets the IDS 5000 make extremely accurate measurements on buried conductors, including those buried under a layer of passivation. As it's often impractical to remove passivation, the ability to probe through layers of nitride, oxide, polymide and other passivation materials is critical in failure-analysis applications. The dynamic fault imaging application tool acquires a sequence of stroboscopic images (snapshots of the state of the chip at fixed points in time) from a known good device and automatically compares these images with a similar sequence acquired from a failing part.

The IDS 5000 can fine tune simulation models of individual gates and entire cells by precisely measuring the timing of unloaded signals on the internal nodes of ICs. Accurate standard-cell characterization is particularly important in the application-specific IC industry. Performance enhancement is achieved by simply increasing clock speeds until the device starts to fail and then comparing the signal measurements at the various clock speeds.



The electron optical system, the key component of the IDS 5000 E-Beam probing system from Schlumberger/ATE, consists of a scanning electron microscope, a probe card, a vacuum chamber and a precision positioning stage that lets all alignments be performed electronically. The electron optical column, designed for the needs of voltage contrast probing, is a two-lens design that measures 14 in. long.

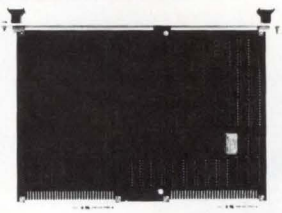
Interactive positioning of the E-Beam in the SEM tool and of the links to waveform measurements in the scope tool transform the design debug process into a technique that's similar to using an oscilloscope and a guided probe to debug a printed circuit board assembly. CAE/CAD navigational tools (net list, layout and schematic) facilitate backtracking techniques and eliminate the time-consuming and error-prone process of manual signal tracing, thus making design debug more efficient and accurate.

E-Beam probing gains acceptance

Many key companies in the industry have begun to use the Schlumberger/ATE system for design debug, failure analysis and device characterization, and to enhance the performance of VLSI designs. To date, Schlumberger/ATE has installed 26 E-Beam probing systems at an average price of about $500,000.

Companies that have already installed IDS 5000 E-Beam probing systems include IBM, AT&T, VLSI Technology, LSI Logic, Delco Electronics, Sandia Labs, Philips, SGS Thomson, and Oki Semiconductor. A few of these companies have already added an additional system to their initial purchase. This seems to be a good indicator that E-Beam probing for design debug, failure analysis, device characterization and performance enhancement is gaining acceptance. And as the technology advances, we can expect to see even more companies using E-Beam probing technology. □

SYSTEM SHOWCASE



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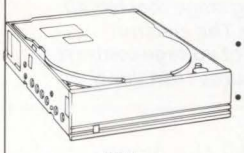
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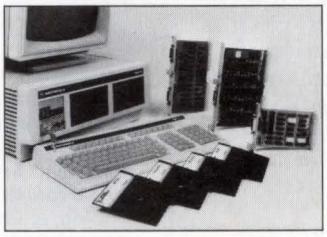

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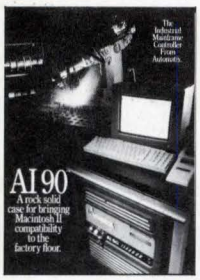
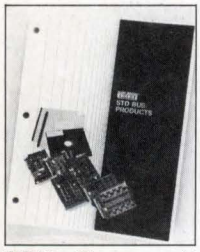


Industrial PC controller

This brochure on the first Macintosh II-based industrial personal computer controller for manufacturing applications includes full product specs on processors, memory, enclosures, operational range and options.
Automatix
Billerica, MA **Circle 205**

Surface-mount ICs

This 32-page brochure describes the company's range of small outline, very small outline and plastic leaded chip carrier surface-mounted ICs, with detailed outlines and dimensions, mounting procedures and comparisons with DIL-packaged counterparts.
Philips
Eindhoven, The Netherlands
Circle 206



STD Bus products

Over 40 high-performance boards as well as software and firmware for STD Bus applications—including analog-to-digital and digital-to-analog converters, CRT, disk controllers and IEEE-488 interfaces—are described in this eight-page brochure.
Burr-Brown
Tucson, AZ **Circle 207**

ASIC production technology

This brochure outlines the company's turnkey design and fabrication system that lets system designers design and fabricate application-specific ICs in-house quickly and inexpensively.
Lasarray
Irvine, CA **Circle 208**

Switching power supplies

This bulletin provides details on standard single-output, switch-mode dc power supplies rated from 60 to 384 W; all are UL-recognized, CSA-certified and VDE-registered.
Tamura
Carson, CA **Circle 209**

Fiberoptic multiplexer port cards

A six-page brochure lists and describes 15 different fiberoptic multiplexer port cards and typical application configurations to interface with RS-232, RS-449 and V.35 links.
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Annapolis Junction, MD
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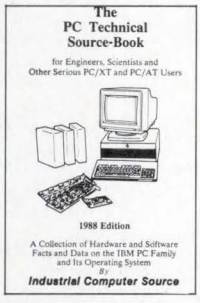

PC technical fact book

Intended for engineers and scientists who use IBM PC, XT and AT computers, this 76-page, pocket-size booklet contains hardware and software facts and data on the IBM PC family and its operating systems.
Industrial Computer Source
San Diego, CA **Circle 211**

SAA/SNA products

A series of data sheets highlights SAA/SNA protocols and SAA/SNA compatibility for the company's family of software and hardware communications products.
Network Software Associates
Laguna Hills, CA **Circle 212**

Government technical reports

This catalog describes a central source for obtaining specialized technical reports and services—such as patents, software, translations, environmental impact studies and CCITT regulations—from U.S. government and worldwide research and development programs.
National Technical Information Service
Springfield, VA **Circle 213**

IEEE-488 products

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Ziatech
San Luis Obispo, CA **Circle 214**

In-circuit emulation

An overview brochure of the company's in-circuit emulation products and software development tools offers development tool solutions for embedded processor designs.
Applied Microsystems
Redmond, WA **Circle 215**

CMOS switches and multiplexers

This catalog provides 16 pages of product and reliability data and block diagrams on the company's line of analog CMOS switches and multiplexers that operate in the 10- to 15-V single- or dual-supply range and are manufactured with a proprietary L^2 CMOS process.
Analog Devices
Canton, MA **Circle 216**

Interconnection system

High-density connectors and headers described in this 16-page catalog can be combined to form board-to-board interconnects with as many as 65 (single) or 130 (double) connections based on a 0.100-in. grid.
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Interconnect Products Div
Rolling Meadows, IL **Circle 217**

Monitoring/ control software

This brochure contains detailed descriptions of LT/Control, an integrated software package for IBM PC-compatible industrial monitoring and control systems. It includes technical specs, system benchmarks and application examples.
Laboratory Technologies
Wilmington, MA **Circle 218**

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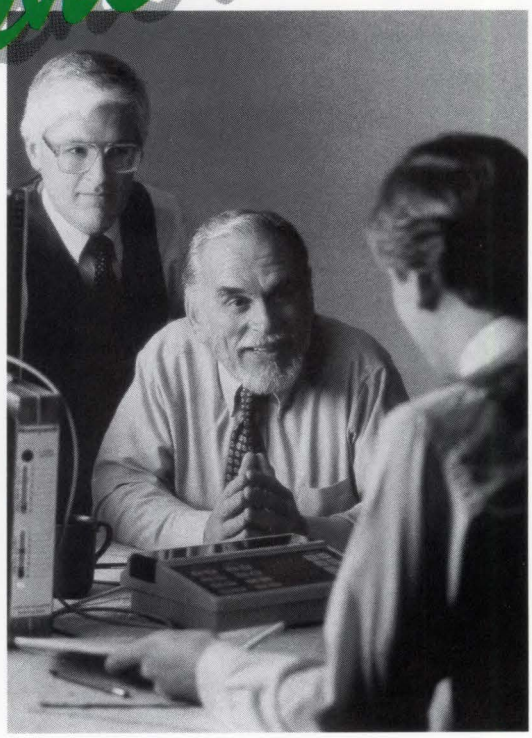

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