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COMPUTER DESIGN

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

JUNE 1, 1988

AUTOMATING DESIGN: A BUYERS' GUIDE TO CAE/CAD TOOLS

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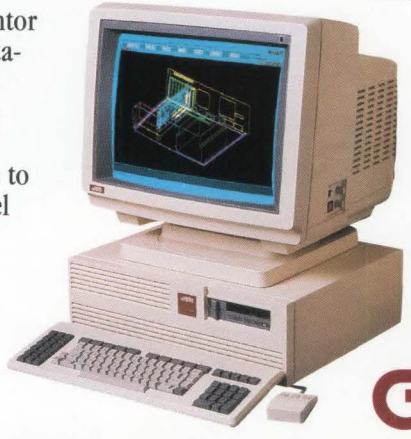

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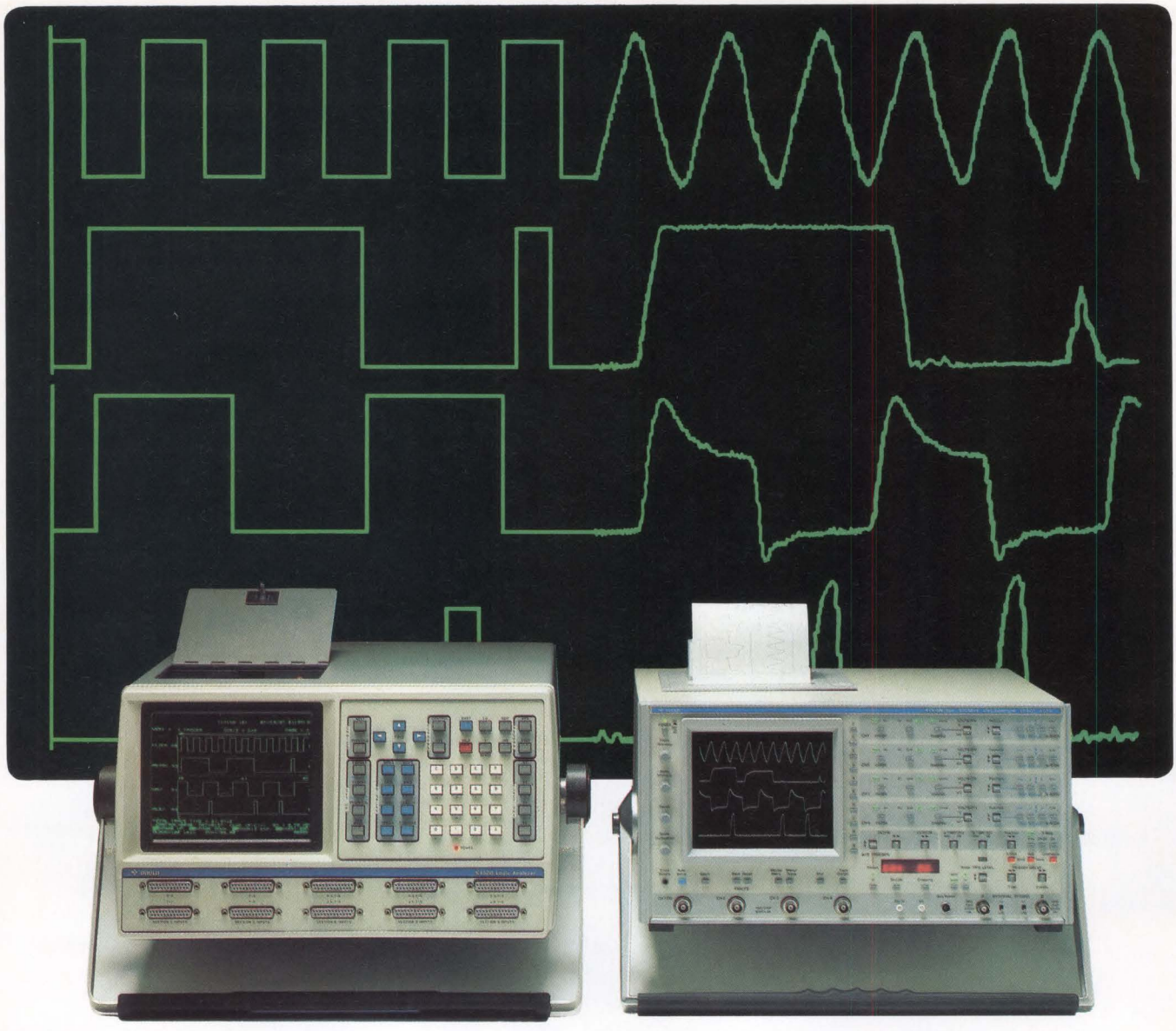

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Vol 27, No. 11 June 1, 1988

COMPUTER DESIGN®

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

This issue's cover was designed by John Bonner.

DEPARTMENTS

DAC Special Product Preview

This month's Design Automation Conference will spotlight the major technologies and products of the ever-growing electronic design automation industry. Our special four-page section highlights some of the industry's hotter areas—logic synthesis, simulation, CASE tools and products that support the VHSIC Hardware Description Language. We also preview some of the more outstanding product introductions. **Page 160.**

DESIGNERS' BUYING GUIDE TO CAE/CAD TOOLS

Special Report

SYSTEM TECHNOLOGY

Integrated Circuits

Peripherals and Memory Systems

Design and Development Tools

Technology Focus on Graphics Subsystems

Technology Focus on 8-bit Microprocessors

SYSTEM PRODUCTS

Design and Development Tools

Computers and Computer Subsystems

Data Acquisition and Control

Peripherals

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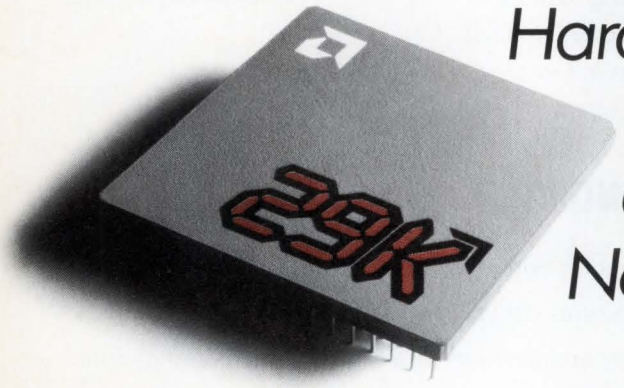

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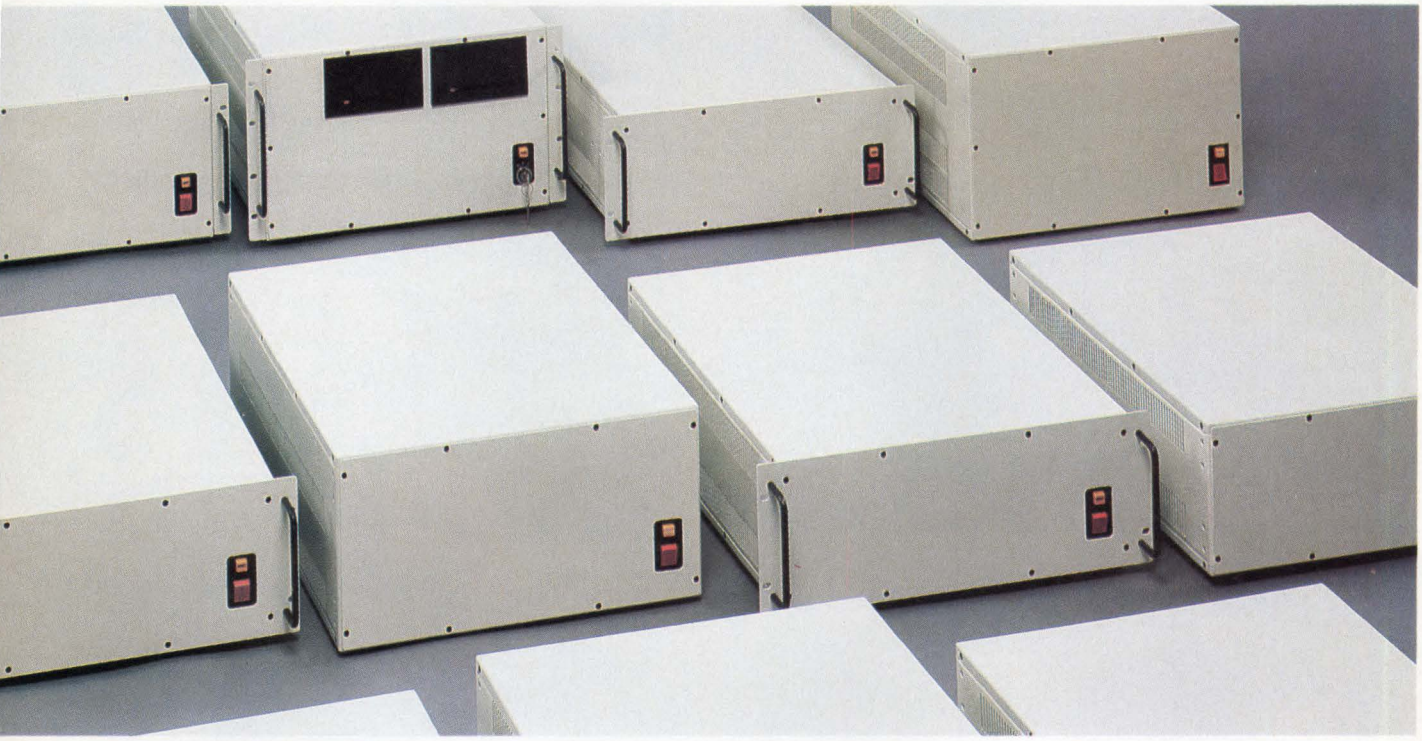

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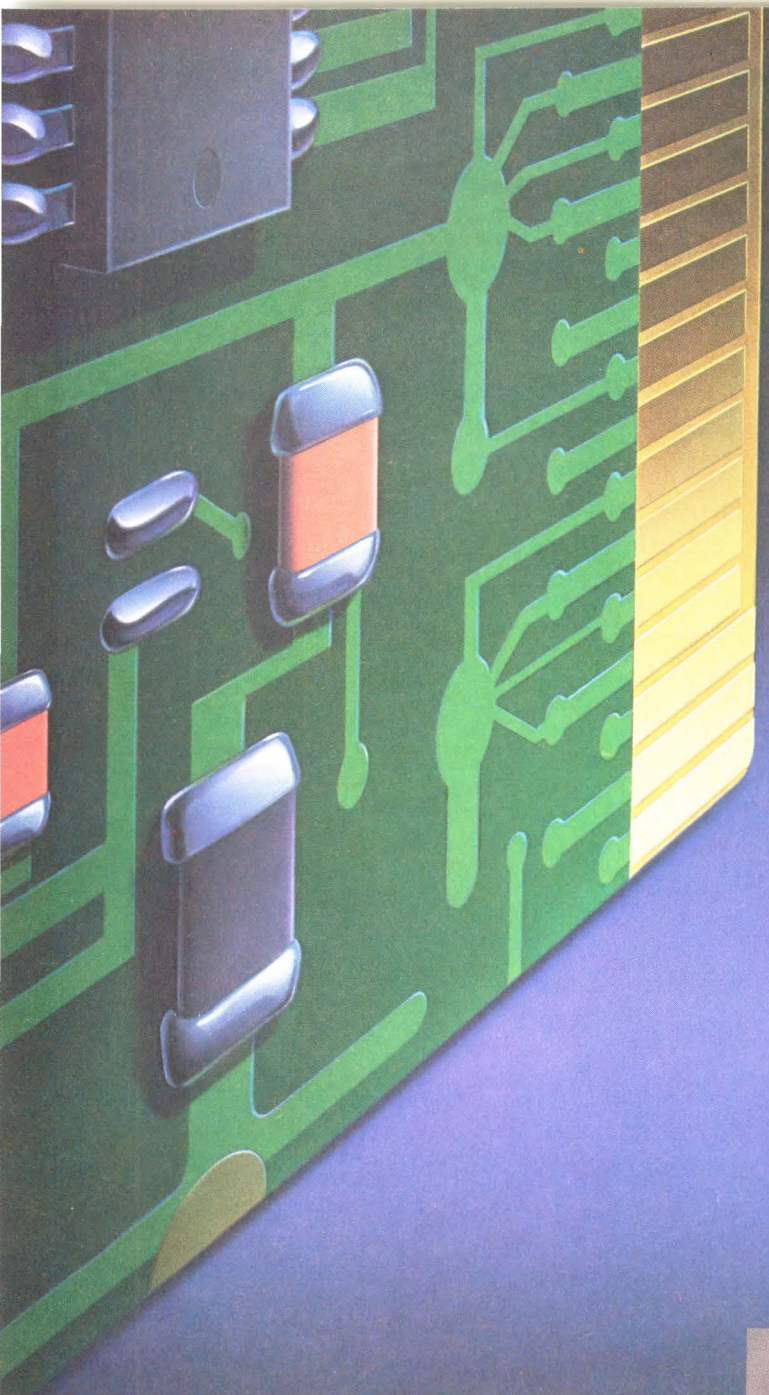

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CIRCLE NO. 6

UP FRONT

IBM-led consortium challenges AT&T domination of Unix

Seven top U.S. and European computer manufacturers have formed the international Open Software Foundation (OSF) as a direct challenge to the AT&T-Sun Unix alliance. Initial members of OSF are Apollo, Digital Equipment Corp, Groupe Bull, Hewlett-Packard, IBM, Nixdorf and Siemens, but membership is open to all organizations around the world. Starting with a new version of IBM's AIX Unix operating system, the foundation will build application interface, user interface, networking, data base and other standards to let applications move freely among the hardware and software environments of the member companies. Such existing specifications as X/Open and Posix will be incorporated in the new standard. In addition, each OSF member will contribute its own software expertise. Apollo's Network Computing System, Groupe Bull's Open System Interconnection (OSI) support, DEC's X-Window-based user interface toolkit, HP's NewWave graphics interface and Nixdorf's distributed SQL data base technology are among the items cited as specific contributions to the foundation. Given the scope of its charter and the technological strength of its participants, establishment of the foundation may have permanently deprived AT&T of the power to dictate the future of Unix.—*Sydney Shapiro*

1-Mbit static RAMs hit market

One-Mbit static RAMs, long the stuff of conference papers and market research reports, are finally being announced as real products. Among the first is a 128k × 8-bit configuration introduced at Electro '88 by Toshiba America (Irvine, CA). With an operating power consumption of 350 mW and a not-exactly-blazing access time of 70 to 100 ns (depending on the version), the new part seems typical of the introductions expected from active high-density SRAM vendors in coming months. Dense enough for main memory applications, these new SRAMs may help take the pressure off some customers suffering in the continuing dynamic RAM squeeze.—*Ron Wilson*

Electroluminescent prototype first to display full color

No flat-panel display technology will replace CRTs until it can deliver inexpensive, comparable, full color. Developments at this year's Society of Information Display conference, held in Anaheim last week, brought flat-panel displays closer to that goal. General Electric (Schenectady, NY) exhibited the highest resolution color LCD to date, a thin-film transistor-driven panel with a 1,024- × 1,024-pixel matrix. The show also featured the first full three-color electroluminescent display. The prototype, from Planar Systems (Beaverton, OR), has a 320-(× 3 phosphors) × 240-pixel matrix over a 4.8- × 3.6-in. active display area. The company developed two-color (red and green) prototypes last year but had difficulty developing a blue phosphor that's bright enough.—*John Mayer*

Logic checker brings artificial intelligence to CAE tools

A rule-based design checker running on workstations from Sun Microsystems (Mountain View, CA) offers one of the strongest applications to date of artificial intelligence in electronic design automation. The

(continued on page 10)

(continued from page 9)

Yoda product from start-up Orcas Systems (San Jose, CA) is a batch program that checks logic entered with various schematic-capture programs. Users can add their own rules for detecting structural errors, finding timing problems and enforcing testability. A similar product is available from NCR Microelectronics (Fort Collins, CO) for its standard-cell customers, but Yoda appears to be the first such tool that's foundry-independent.—*Richard Goering*

Hewlett-Packard makes 100 percent commitment to MAP

Although in the past each division of Hewlett-Packard (Palo Alto, CA) used its own proprietary network in its systems, all HP divisions are now committed to the Manufacturing Automation Protocol interpretation of the Open System Interconnection model. The only exception will be for some instrumentation. The announcement was part of the company's unveiling of plans for several MAP and OSI products to be introduced over the next three years. HP OSI Express, a new technology that implements Layers 1 through 7 of the OSI model, will be implemented first on a board called MAP 3.0 MMS (Manufacturing Message Specification). Software and a device-interface system toolset will be available by the end of the year. A MAP 3.0 protocol analyzer and MAP 3.0 file-transfer, -access and -management (FTAM) software will be available by mid-1989.—*Sydney Shapiro*

Sony makes serious play in high-speed logic

Sony's recent foray into the bipolar market is only a hint of things to come, according to J.P. Laussade, director/general manager of the company's Component Products Division (Cypress, CA). The company's new logic family achieves speeds of up to 4 GHz while keeping power consumption well under 1 W. That performance comes from Sony's ECL III technology, a 1-micron process with a 10-GHz transition frequency and an 80-ps gate delay at 300 μA. "Transmit time from pin-to-pin is faster than gallium arsenide," says Laussade. And that's only the beginning. ECL IV, a submicron process twice as fast as ECL III, lurks just around the corner, according to Laussade.—*John Mayer*

Daisy ports CAE tools to Sun 80386-based workstations

After years of offering its proprietary workstations, Daisy Systems (Mountain View, CA) will announce this month that it plans to port its CAE/CAD software to 80386-based workstations from Sun Microsystems (Mountain View, CA). The move should considerably strengthen Daisy, which recently experienced two bad years largely because of its exclusive reliance on proprietary hardware. By this fall, Daisy will port its schematic-entry and simulation tools to the Sun 386i family and will later offer printed circuit board and IC layout tools. Daisy has already begun porting its tools to the SunOS Unix environment. For the foreseeable future, Daisy will continue to offer its proprietary Personal Logician and Logician workstations, and its proprietary Dnix operating system.—*Richard Goering*

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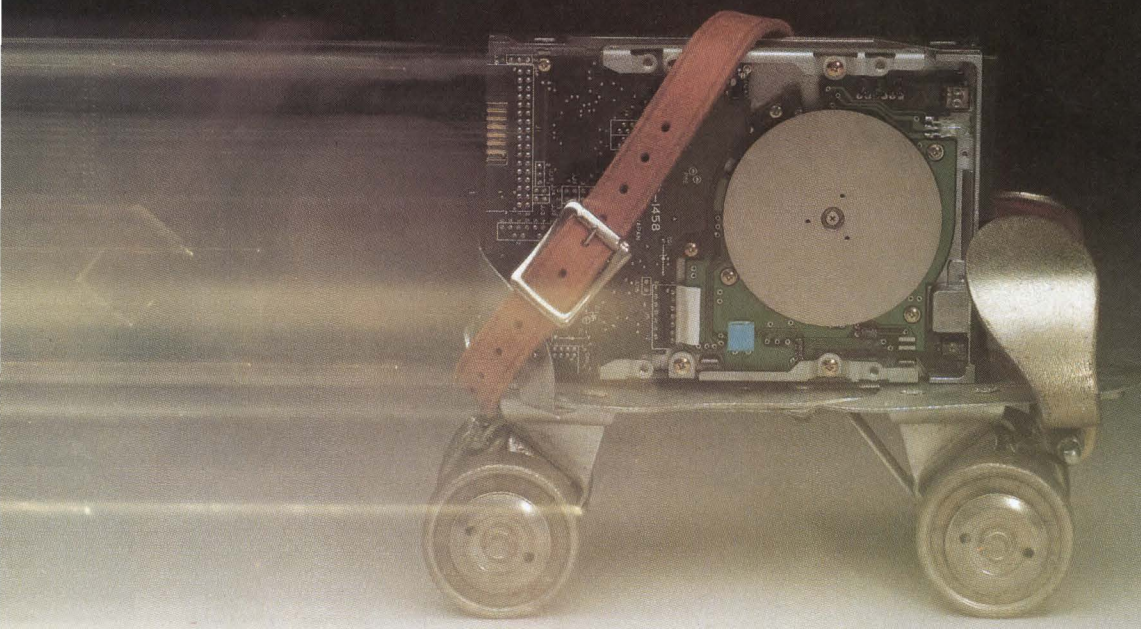

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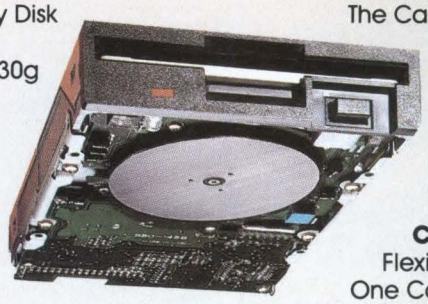

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CIRCLE NO. 7

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	XC1429C	31.5
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	FG6600	60–65
	HL/FL6605	30 ~ 64*
19" CAD/PC CAD	C3920/21/22	15–24
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MITSUBISHI ELECTRONICS

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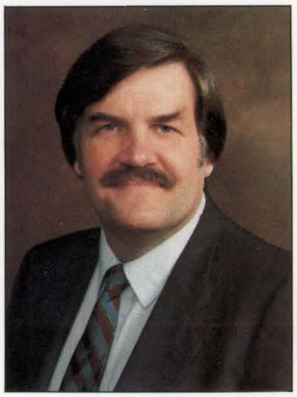
New Models Now Available



Chips vs. chips

It wasn't a world-shaking international incident. It only warranted a 30-second spot on the nightly news. The Associated Press wire service picked it up, so it made its way into a few newspapers. What was the incident? You might call it the second battle of Midway. But this time around, it was fought by Japan, some sailors aboard the USS Midway anchored at the Navy Air Station in Atsugi, Japan, and the Girl Scouts of America. It was all about 400 boxes of cookies.

As the story goes, these young men, doing what a lot of good young American men have been doing now for nearly 75 years—namely helping to defend the world against tyranny—also tried to help the Girl Scouts by buying some cookies. The news stories didn't mention whether the cookies were peanut butter or shortbread or chocolate chip. But no matter. Whatever they were, they cost only $2 a box. The Japanese, true to form in their dedication to protect their markets and their culture from intrusion by everything from beef and oranges to microprocessors, cellular telephones and American construction workers, classified the cookies as an agricultural product and slapped on a tariff of $5 a box. Not 5 cents, or 50 cents, but $5. The sailors finally got their cookies, but only after surrendering to this extortion.

What happens to $400 worth of Girl Scout cookies is infinitesimally inconsequential in comparison to the multibillion-dollar U.S.-Japanese trade imbalance. The significance of the incident is far from inconsequential, however. It underscores, once again, the myth of free or even fair trade as far as the Japanese are concerned, as well as their gross insensitivity to their trading partners. More than that, it once again focuses the spotlight on the true protectionists.

The time has come for us to wake up to the realities that few, if any, of our trading partners believe in free trade, that fair trade is open to as many interpretations as there are trading partners, and that protectionism, in one form or another, is the rule. The game of international trade isn't being played for the fun of playing; the game is being played to be won. Our trading partners, and the Japanese perhaps more than anyone else today, want to go to the Super Bowl, and they want to win. As noted in Warren Andrews' article on the current dynamic RAM shortage (see page 19), we should take whatever measures are needed to reestablish our position in the semiconductor industry, and the same holds true for a host of other industries.

I'm not big on sports analogies, but if you have to beat the Green Bay Packers to make it to the Super Bowl, you don't cry about the subzero weather, the raging snow or the muddy field. You strap on your padding, go into the mud and do whatever it takes to win. Winning in domestic and international markets requires the same grit and strategy.

John C. Miklosz
Associate Publisher/Editor-in-Chief

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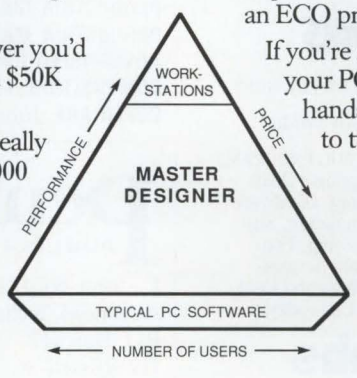

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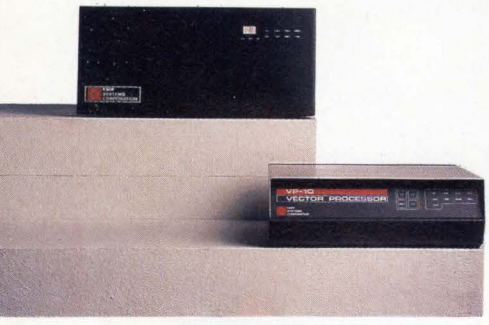

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The VP-10's pen plotter emulation feature allows compatibility with hundreds of graphics software packages, including VersaCAD, AutoCAD, and SAS. The VP-30 can be used with such popular packages as CADAM, CADS4X and Scicards/Quickplot.

The VP-10 supports electrostatic plotters from Benson, CalComp and Versatec, as well as small color raster devices from Seiko and Mitsubishi. Input data formats include KMW.PLT, HPGL (HP pen plotters), and CalComp 906/907. The VP-30 supports Versatec, Benson and CalComp electrostatic plotters – including color – and drives them at full speed. It accepts CalComp 906/907, 925, 960 and KMW.PLT data formats.

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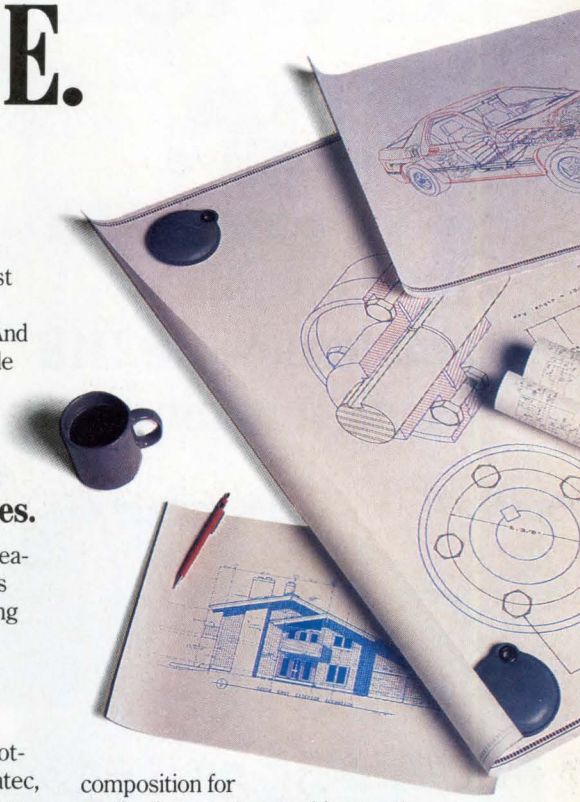

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CIRCLE NO. 13

DRAM shortage holds computer makers hostage

Dynamic RAMs are the oxygen of the computer business, and the industry is experiencing some breathing problems because of the recent shortages. The DRAM shortage that began late last year is beginning to cast a pall over the near-term—and perhaps long-term—future of the computer business. Initially, the scarcity of parts was attributed to four factors: a glitch in a large Japanese fab line, a delay in coming up to speed on 1-Mbit parts, unprecedented demand, and restrictions imposed by the Semiconductor Trade Agreement that the U.S. signed with Japan.

"All of these factors may have contributed to the disaster in the memory market," comments one major DRAM buyer, "but there seems to be something more organized about it. The disaster is turning into a pogrom." This same sentiment has been echoed by numerous vendors (who don't wish to be identified) in the board-level business, as well as elsewhere. "We're facing a major problem, and a lot of people believe that it's just going to go away," comments a prime semiconductor maker.

"The large horizontally aligned Japanese companies don't want to buy just the chip business or, for that matter, the semiconductor business. They want the whole thing—chips, boards and computers," emphasizes another industry executive. "And they're going to get it," he adds, "unless U.S. companies, the government and industry trade associations cooperate to stave off this disaster."

By constricting the supply of memory chips, offshore vendors not only drive prices up, but get their foot in the door as suppliers of other semiconductors, such as application-specific ICs, by leveraging their "allotment" of memory chips. In addition, they bite off chunks of the board, subsystem and system business by being able to provide timely delivery of completed assemblies.

Forecasts for the next few years don't look bright. Japanese vendors say they'll increase production (and exports), but even the figures they quote won't fill the shortfall (see table below). U.S. vendors (the two still in the business) can't make up the difference, and even with an all-out effort and an investment estimated at close to $2 billion, other U.S. semiconductor manufacturers could only meet about 40 percent of the estimated demand by 1991.

How it happened

How the U.S. semiconductor industry got to this point is an oft-repeated story. In the late 1970s and early 1980s, there were almost a dozen U.S. DRAM vendors. Low-priced Japanese imports drove all but two—Texas Instruments (Dallas, TX) and Micron Technology (Boise, ID)—out of the business. TI, for its part, has retained its DRAM facility, but primarily as a proving ground for new technology. Micron has had to struggle to stay above water in the price wars.

In their aggressiveness to capture the DRAM market, Japanese vendors flooded the U.S. market with cheap chips, driving out U.S. competitors. Semiconductor industry experts estimate that the chief Japanese DRAM vendors lost about $4 billion on sales of DRAMs to the United States. Charges of dumping were levied against the Japanese manufacturers, and were upheld, resulting in the 1986 Semiconductor Trade Agreement. This agreement amounted to locking the barn door after the horse has escaped. In addition, the agreement invited the offshore DRAM manufacturers to reduce exports to force prices up.

With virtually no U.S. competition, Japanese vendors are free to charge whatever price they want. The trade agreement seems to assure a shortage, and vendors are free to allocate relatively scarce parts.

As DRAMs started becoming scarce, computer makers were quick to blame the trade agreement and vented much of their anger at semiconductor manufacturers for initiating the agreement. This resulted in antagonism between the American Electronics Association—largely composed of system manufacturers—and U.S. chip makers. Though that squabble isn't yet over, most of the systems houses agree that the real problem isn't the trade agreement—rather, it's the fact that U.S. vendors were driven out of the market by the price wars with Japan.

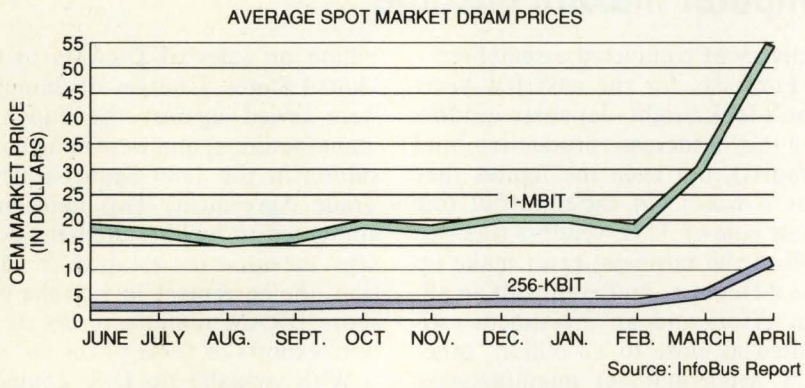
"The real problem has its roots in the U.S. semiconductor sector's almost nonexistent capacity to turn out DRAMs," system makers claim.

Japanese Production Forecast

	Density	Quarter (1988)	Production (units in thousands)	Export (units in thousands)
DRAMs	64-kbit	2	21,200	12,900
		3	18,900	11,900
	256-kbit	2	159,300	90,500
		3	155,100	88,600
	1-Mbit	2	43,600	28,300
		3	56,000	35,000
SRAMs	16-kbit	2	40,800	16,200
		3	42,200	16,500
	64-kbit	2	46,800	21,000
		3	50,600	22,200
	256-kbit	2	22,500	10,000
		3	26,000	11,800

Source: Ministry of International Trade and Industry

Warren Andrews
Contributing Editor



With virtually no U.S. competition for the dynamic RAM market, Japanese vendors were free to reduce exports to force prices up. When the supply of memory chips was constricted, spot market prices rose sharply, resulting in steep increases in board-level and system prices.

As mentioned, only Micron Technology and Texas Instruments survived to have any capacity to produce DRAMs. And though Micron is doubling its present capacity, it represents only a very small drop in the bucket. TI is reportedly beefing up its U.S. capability—even to the extent of bringing key personnel back from its Japanese facility.

It's also reported that other U.S. semiconductor vendors may be reentering the DRAM business. Motorola will be setting up a fab line for memory, but it isn't yet clear how committed the company is the task of taking on the offshore competition. National Semiconductor, too, is reported to be investigating prospects of surfacing with memory products. But such moves are at best risky ventures. The large Japanese chip makers could easily open the flood gates and release large volumes of parts just as U.S. semiconductor vendors have made a significant investment in tooling up and are getting up to speed.

"Without some kind of protection, either in the form of meaningful trade agreements or a managed trade policy," says a major chip maker, "such a major investment could backfire." System makers and chip builders are attempting to come up with some reasonable formula. Suggestions include long-term purchase contracts and even a co-op of system makers building their own DRAM factory.

Rough times ahead

Even if U.S. manufacturers find some potentially feasible solutions, the going will be rough because the foreign chip makers are the same companies that are also in direct competition with the U.S. system makers. These include all the broadly horizontal companies making all types of computers from micros to mainframes, communications equipment from desktop consoles to central offices, and instrumentation from automatic test equipment to lab equipment. Such companies include NEC Electronics, Fujitsu, Toshiba, Hitachi, NTT, Oki Semiconductor and Mitsubishi.

In addition, many other Japanese companies such as Ricoh, Seiko-Epson and others are using DRAM availability (from internal DRAM capacity and from other Japanese sources) to leverage their market position in everything from FAX machines to personal computers.

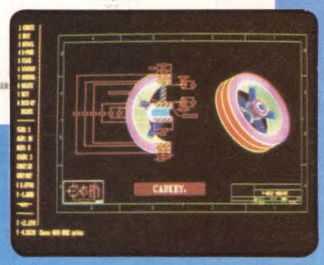
To make matters even worse, potential problems aren't being aired. Many DRAM customers are intimidated about screaming too loud, lest suppliers freeze them out. Even in interviews with the press, buyers and users tread very gently—often even after being guaranteed anonymity. "We're being blackmailed and have no choice but to give in," says one frustrated business owner. "If, for any reason, our supply of memory is cut off, we're out of business." Even in cases where vendors blatantly sidestep the law—such as when they demand tie-in sales—customers are hesitant to complain, afraid of possible repercussions.

What can be done?

Problems with shortages, and the movements of systems business abroad that such shortages produce, will recur as offshore vendors alternately tighten and relax their stranglehold on the market. Each time the hold tightens, a little more U.S. semiconductor, board and system business moves abroad. Aside from the loss of business, there's an even greater loss in terms of a transfer of technology to other shores. And national security becomes an issue when those shores are unfriendly.

Some industry experts believe steps can be taken to both lessen the immediate burden and plan a long-term strategy to preclude the problem from recurring. Certainly a key element in both a short- and long-term effort will include decisive government action. The following remedies have been suggested by various industry spokespeople.

- Strictly ration imports—many propose that for every bit of memory exported to this country as a system or board, some minimum number of bits must be exported as chips that are put on an open market, not just imported and sold to U.S.-based Japanese companies.
- Eliminate the bundling of other products (particularly semiconductors) as a condition of sale. (This practice was used inversely when memory prices were low, but is a violation of antitrust legislation in either event.)
- Continue (or increase) the executive order placing a 100 percent duty on any 16-bit or greater microprocessor- or processor-based imported product.
- Tighten loopholes that have traditionally let Japanese vendors sell to U.S. companies or to their own



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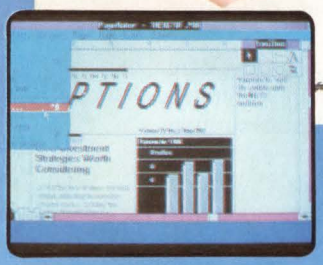

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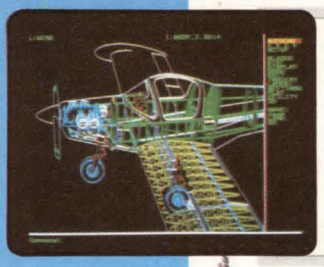

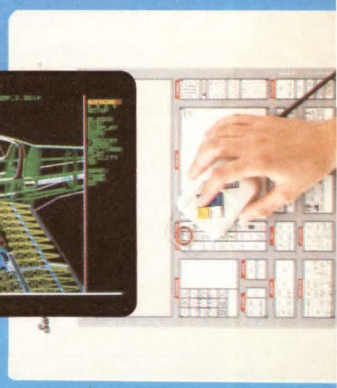

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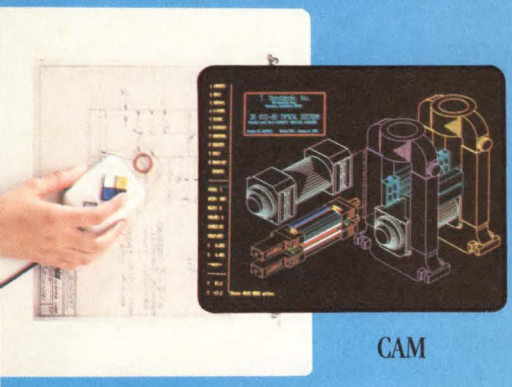

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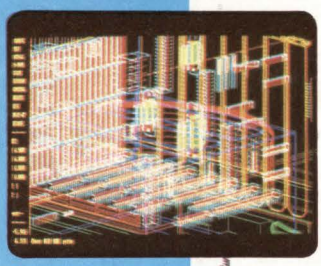

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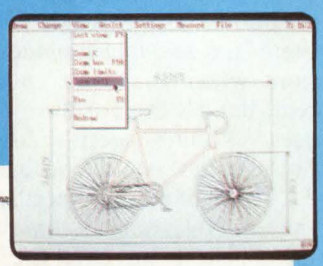

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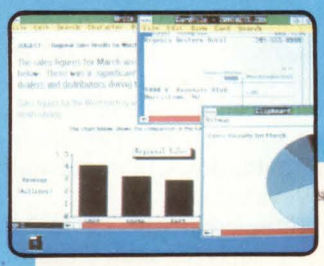

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U.S. subsidiaries through other trading nations.

- Make it mandatory for any company that's dealing in interstate trade to seek a domestic supplier first or offer a reasonable excuse for purchasing foreign parts. Such legislation could be accompanied by perks for compliance, such as tax incentives—not just punishment for noncompliance.

Legislators concerned with the general economy, the total federal budget, U.S. employment and employment opportunities, and the trade balance should be studying these issues, rather than how the United States can be "nice" to its international trading partners. For the long term, there are other issues that must be addressed to see that the DRAM fiasco isn't repeated with other products or in other industries.

> *"We're being blackmailed and have no choice but to give in. If, for any reason, our supply of memory is cut off, we're out of business."*
> *—Name withheld*

The situation demands that U.S. manufacturers be able to deal on an equal footing with their counterparts in trading nations. For them to do so, steps must be taken to manage trade policy; revise antitrust legislation; initiate tax incentives and low-interest loans; sponsor (or at least participate in) cooperative research groups; and put a mechanism in place for rapid response to industry complaints of unfair trade practices. If these suggestions and others proposed by semiconductor leaders and system makers alike are put into action, the result might well be the beginning of a new era of prosperity for the U.S. semiconductor manufacturing sector. **CD**

New PLD architectures deliver needed flexibility

New programmable logic device architectures have been coming out of the woodwork lately. First there were generic versions of standard PALs. Then there were devices that looked suspiciously like gate arrays, or like application-specific products with some programmable logic built in. Now, there are so many architectural alternatives that even vendors admit it's hard to make the right choice.

But the confused market seems to be gradually segmenting itself into three clumps. One clump focuses on the 20- to 24-pin devices used primarily in state machines. At the opposite extreme, a second group of products emphasizes high pin count and great circuit flexibility. In between these two poles, a third market segment seems to be emerging, combining some of the characteristics of both the low-pin-count and high-end devices.

Of the three areas, the 20- to 24-pin device group is certainly the most traditional. These devices almost all have a PAL architecture—a programmable AND array, a fixed OR array and highly configurable output macrocells. The flexibility of the macrocells lets one part substitute for a wide variety of older parts with essentially the same AND array layout but with different buffer, register or latch configurations.

Parts with up to 24 pins seem to be used predominantly for implementing state machines. So the operating frequency of the state machine necessarily influences the way these PALs are designed. For the most speed-critical state machines, vendors have successfully assailed the 10-ns propagation delay barrier in both bipolar and CMOS technologies. But for the less speed-driven applications, virtually every vendor has moved to CMOS.

One such vendor is Signetics (Sunnyvale, CA), which announced a family of four 20V8-style CMOS parts in May. The devices are available in quarter- and half-power designs, with propagation delays ranging from 45 to 35 ns. Signetics points out that, unlike many fractional-power CMOS parts, the PLC20V8 family has 24-mA outputs.

Advanced Micro Devices (Sunnyvale, CA) recently introduced a 20-pin part, the CMOS 18U8Q, that uses a similar idea. A quarter-power device, this implementation of the 18U8 offers either 25- or 35-ns propagation delays.

Pushing CMOS logic to these speeds raises a new issue for PAL designers: switching noise. "At 25 ns, a switching noise in a CMOS PAL can get pretty bad," warns Andy Robin, AMD director of marketing for programmable logic. "We control the problem in the 18U8 by limiting the output current to 8 mA. Of course, there are some backplane applications where that isn't enough current, but it's fine for the majority of uses." Robin suggests that switching noise issues could confine CMOS PALs to moderate speeds, leaving the sub-10-ns range to bipolar chips. "We believe we have the problem under control down to 7 ns, or maybe 5 ns, in TTL devices. But at these frequencies, where CMOS and

Ron Wilson
Senior Editor

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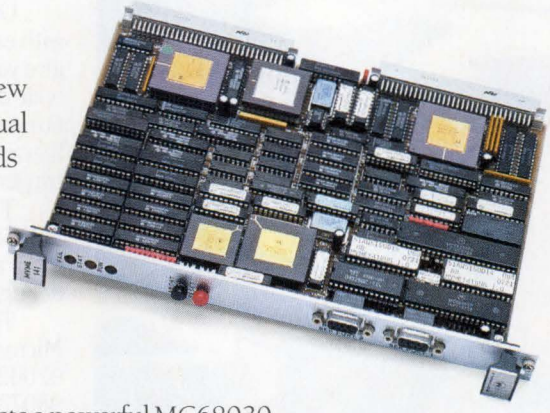

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CIRCLE NO. 16

TTL power consumptions are about the same anyway, CMOS may just not be an amenable technology."

Struggling for flexibility

The mass migration to CMOS has meant more than power savings for vendors. Greater CMOS densities mean the possibility of packing more complexity into the 24-pin devices. And that added complexity could serve customers building more complex state machines. But how to add flexibility, maintain a fixed I/O pin count and still make the device useful has been a puzzling problem.

One vendor, Lattice Semiconductor (Hillsboro, OR), has taken a cue from customer feedback on that quintessential PAL, the 22V10. "It's been an evolutionary development," says Lattice applications engineering manager Rodney Strange of his firm's new 24-pin chip, the 39V18. "Everyone loves the 22V10 until they try to use the top and bottom terms. Then they want more flexibility in allocating product terms."

To beat the allocation problem, Lattice took a page from the history of programmable logic: the page that describes PLAs. "We put both a programmable AND array and a programmable OR array into the 39V18," explains Strange. "That lets the designers who are working out really complex state machine designs allocate the product terms exactly as they need.

"The industry moved away from AND/OR programmability because it was too slow. But with our hot CMOS process and our inherently fast EEPROM fuses, we can make up most of the speed difference. The technology is really a key here—I don't think many vendors could build this part in an EPROM process," says Strange.

Taking additional steps to tailor the 39V18 to difficult state machines, Lattice worked out an unusual set of storage features. All 20 input pins are latchable, and all outputs are driven by sophisticated macrocells. Perhaps more important for machines in which not all state variables need to be observable, the chip provides eight buried-register macrocells.

Of course, all this capability in a 24-pin device comes at a price, and for the 39V18 that price is complexity. "This is not a part you'd give to a designer right out of college," Strange says candidly. The complexity of the chip also raises the ever-popular PAL testing issue: with this much going on in the chip, how do you know it's working?

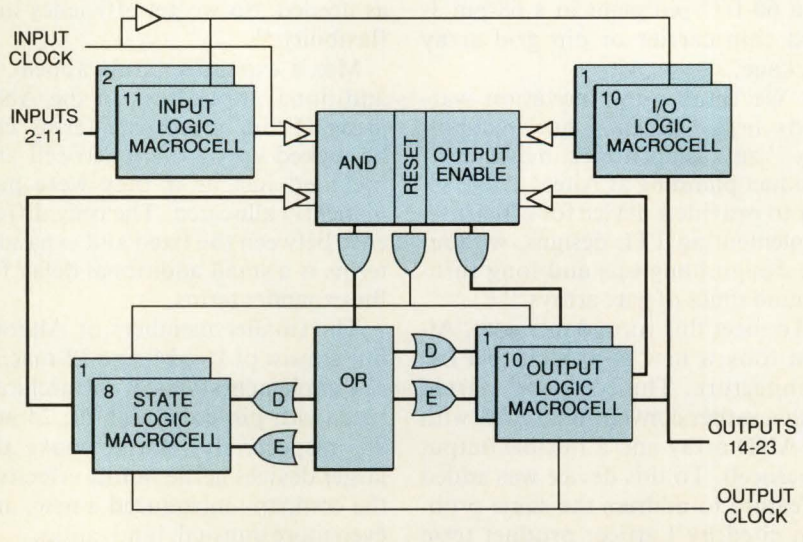
> *"There's no question that what this market wants is a programmable gate array."*
> *—Andy Robin*
> *Advanced Micro Devices*

The dependence Lattice has on EEPROM technology comes to the rescue here, according to Strange. Since the part can be programmed, tested, erased and reprogrammed in a matter of seconds, Lattice can feed combinations of programs and test vectors through the device to test all signal paths and all fuses before shipment. "For many of our customers, that's the biggest single point—that we guarantee 100 percent reprogrammablity so our customers can solder down the parts without testing them," Strange says.

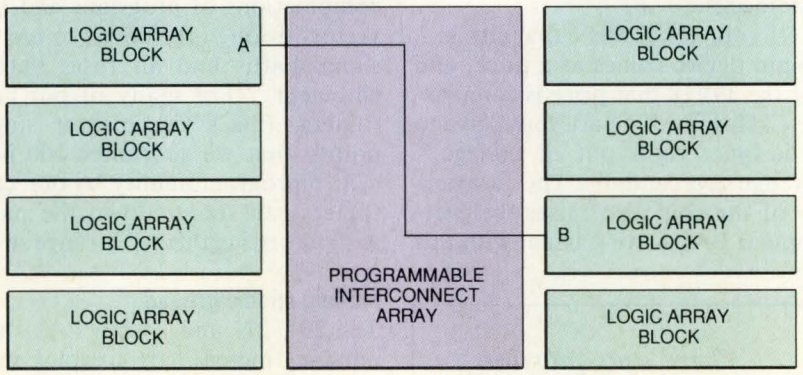
Finding middle ground

The 20-, 22- and 24-pin PALs are pursuing increasingly complex state machines with relatively conventional architectures. But at the high end, the PLD market is dominated by an entirely different idea of architecture. "There's no question that what this market wants is a programmable gate array," claims AMD's Robin. And obliging vendors, such as Xilinx (San Jose, CA), AMD and new entrant Actel (Sunnyvale, CA), are working to provide just that.

But there's still a lot of unclaimed ground left over. "There's also a need for mid-range parts, something between a 22V10 and a Logic Cell Array," observes Robin. Such a part would need the flexibility to handle



Lattice Semiconductor's 39V18 returns to a programmable-AND, programmable-OR architecture to optimize product term allocation. The 24-pin PLD's input latches, I/O macrocells and buried registers can reduce the number of packages required to implement complex state machines.



Altera's Max PLD architecture attempts to find some middle ground between conventional PALs and gate arrays. Each chip consists of a number of logic array blocks (LABs), essentially conventional PALs. The LABs are interconnected by a programmable interconnect array: a big, fixed-delay programmable version of a routing channel.

designs other than state machines, so it would need gate-array-like interconnect flexibility. But ideally it would have an understandable, predictable architecture that would look familiar to experienced PAL users.

Altera (Santa Clara, CA) thinks it has hit on this combination with its Max (Multiple Array Matrix) architecture. The architecture is provided in a family of devices, ranging all the way from a 16-I/O-pin device to a 60-I/O-pin giant in a 68-pin J-lead chip carrier or pin grid array package.

"We think our innovation warrants being called a new technology," says Stan Kopec, manager of product planning at Altera. "We set out to provide a device for efficiently implementing TTL designs, without the design hang-ups and long turnaround times of gate arrays."

To meet this formidable goal, Altera took a new approach to PLD architecture. The company started with a rather conventional PAL with an AND array and a flexible output macrocell. To this device was added a feature to address the same problem cited by Lattice: product term utilization.

"Between 70 and 80 percent of designs use only three product terms per output macrocell," explains David Laws, vice-president of marketing. "That means that more product terms permanently assigned to the cell are usually wasted. But in a fixed-allocation system, those product terms have to be there to meet worst-case needs.

"What we do in the Max," Laws continues, "is provide three product terms per macrocell. Then we have a pool of uncommitted product terms, called expander product terms, that can be assigned to any macrocell as needed. So we get efficiency and flexibility."

Max's expander terms appear as additional input lines in the AND array. From there, the terms can be picked up by the macrocell and included just as if they were permanently allocated. The only difference between the fixed and expander terms is a small additional delay for the expander terms.

The smaller members of Altera's line consist of 16-, 24- and 32-macrocell implementations of the architecture, with pin counts of 20, 24 and 28, respectively. But to make the larger devices in the family effective, the company introduced a new, and even more unusual, innovation.

Larger versions of the Max are configured not as a single big PAL with expander terms, but as a cluster of identical 16-macrocell PALs on a single chip. Chips are available with either four or eight of these logic array blocks (LABs), as they're called. To interconnect the LABs, Altera decided against the traditional gate array routing schemes used by programmable gate array vendors.

"The problems with the usual point-to-point routing," explains Kopec, "are that you can run into bottlenecks and that you can't predict what your routing delay is going to be. Some devices can have routing delays as high as 50 ns. We felt that was inappropriate."

Altera's solution is known as a Programmable Interconnect Array (PIA). Essentially, it's a set of uncommitted routing lines running down the center of the chip. From each routing line, connecting lines run through programmable fuses to each LAB. Consequently, the internal feedback signals and I/O signals from any macrocell on the chip can be connected to a PIA line and appear in the AND array of any other macrocell. The delay involved in traversing the PIA is a fixed 15 ns.

Altera's determination to make Max useful for TTL designs extends beyond the architecture to the design tools. Consequently, the design tools for the Max can work with schematic editor input as well as state machine, Boolean expression or truth table forms. Further downstream, tools extract a net list from the design data and then automatically map functions onto Max's architecture, very much in the fashion of a gate array design package.

Though Max's PIA is functionally and conceptually quite different from the variable-delay routing channels on a gate array, there's something about the analogy that sticks. In some sense, the new Altera part represents a synthesis of the well-understood but inflexible 24-pin PAL and the highly flexible but more demanding gate array. Similarly, the design problems Max serves contain both elements of the state machine approach served by PALs and the random logic approach served by gate arrays. There may indeed be a fertile middle ground between the extremes. **CD**

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CIRCLE NO. 29

Intelligent memory architectures attack real-world computation

Intelligent memory systems, which integrate some specific computational function into a memory device, have for years suffered exile in the halls of academia, barred from the industry because of their heretical, non-von-Neumann approach to computing. But recent increases in VLSI densities make these unique architectures technically feasible. And the continued intractability of some computing problems is making these systems more attractive to designers.

Two recent announcements illustrate the application of intelligent memory systems in real-world problems. The first, a content-addressable memory from Advanced Micro Devices (Sunnyvale, CA), deals with data-management problems such as sorting and indexing. The second example, a memory-based matrix multiplication device from Oxford Computer (Oxford, CT), finds application in areas as diverse as matrix algebra, image processing and neural network research.

Ron Wilson
Senior Editor

AMD's 95C85 Content-Addressable Data Manager (CADM) is essentially a 1-kbyte array of static RAM with the ability to sort its contents and to match them against a key. This capability lets the CADM act as a sort coprocessor in a system, able to achieve speeds far in excess of those attainable with conventional computing equipment. "AMD has benchmarked the CADM against a Cray X-MP on a number of sorting tasks," claims Dave Horton, strategic development manager at AMD. "While the sort performance is very data-dependent, we found that at worst the CADM was more than 1.3 times faster than the Cray."

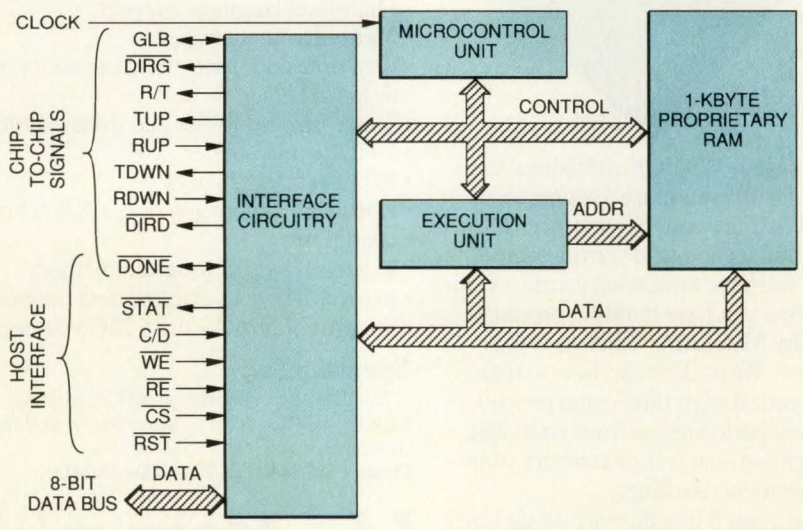
The chip has similar performance gains on content addressing. In this mode, the memory stores pairs of fields: a key field and a data field for each record. When the system sends a key to the CADM, the chip must respond with the corresponding data. The speed of this operation is also quite data-dependent, although it isn't influenced much by the total number of records in the memory. Typically, an array of CADM chips can respond to an 8-byte key in about 10 μs. AMD observes that this can be up to 500 times faster than software search algorithms.

These speeds aren't due to any breakthrough in process technology, but rather to the internal organization of the CADM chip. Inside, the CADM is essentially a very flexible 1-kbyte first-in, first-out register, surrounded by a bank of specialized comparators and controlled by a proprietary microcontroller.

The design of the FIFO permits two very special operations. First, the width of the register is programmable; hence, you can command the CADM to accept key and data fields of any length up to 255 bytes each. Second, the FIFO performs insert and delete operations very quickly. For instance, the CADM can insert a key/data record into the middle of memory, making room for it by moving all subsequent records down one space, thereby preserving the sequence of the records.

The bank of comparators is closely integrated with the memory array. Consequently, when the CADM is presented with a key, the comparator bank can establish within a matter of microseconds whether that key is present in the memory and where in the sequence of records it belongs. Meanwhile, the microcontroller is kept busy managing all of the pointers necessary for correct operation of the chip.

For cases in which the file does not fit into 1 kbyte, two alternative approaches are available. First, CADM chips can be cascaded to form one very long intelligent memory. Since all of the chips' on-board comparators and controllers will operate at once, the processing speed of the system actually increases as the number of chips increase. Thus, a file that requires a large number of chips will be handled in nearly the same amount of time as a file that fits in one chip. If the files are too big to fit into a bank of chips, search operations may be done by paging the file through the available chips.



Advanced Micro Devices' Content-Addressable Data Manager, which deals with such problems as sorting and indexing, integrates comparator and control logic into a 1-kbyte memory array. Interface circuitry connects to a host computer and enables efficient daisy chaining of the chips.

Similarly, large files can be sorted in pages and then merged. In either case, the total time required will be considerably shorter than for a software-only approach.

"Originally, we thought of the CADM as a sort engine for data base machines," explains Horton. "But as we started taking the design out to customers for feedback, they began to find new applications. Designers suggested things such as a network bridge, where the CADM could map packet addresses from one network to another without introducing large delays. Other customers suggested hidden-surface removal in graphics systems, disk caching and pattern-recognition uses.

"In one way, the part really challenges designers because it's an inexpensive hardware solution to a problem people are used to solving with software at much lower speeds. We are still finding out ourselves what you can do with a chip that can sort and search this fast."

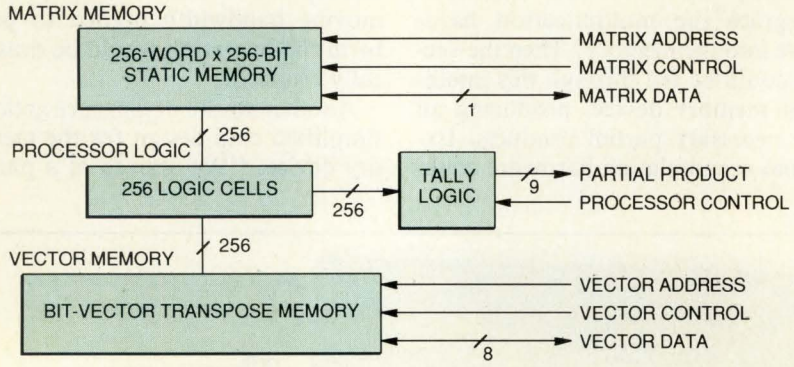
Multiplying matrices

The integration of processing logic with memory arrays has taken quite another direction at Oxford Computer. Here, the emphasis has been on another time-consuming problem that arises frequently in computing: multiplying a vector by a matrix. "We wanted to drive the cost of a vector-times-matrix multiplication into the ground," says Steven Morton, Oxford founder and chief technical officer. "Then we could look at the applications that the low cost made possible."

Oxford's approach involved first rearranging the steps in a matrix multiplication and then designing an intelligent memory system to implement them. Morton points out that the primary problem in performing the multiply isn't the arithmetic so much as moving all the data around.

Ordinarily, each element in the vector has to be multiplied by each element in the matrix, so the whole matrix gets shuffled through a vector processor once for each vector element. Oxford's idea was elegantly simple: why not put the matrix in a memory and leave it there, and then integrate the multiplication hardware into the memory? Then the vector could be fed through this intelligent memory device, producing all the necessary partial products. External accumulating hardware could add up the results. The total data-moving bandwidth needed to perform the operation would be drastically reduced.

Another stroke of elegance greatly simplified chip design for the memory device. "We arrived at a parti-



Oxford Computer's Intelligent Memory Chip integrates a RAM array with a matrix multiplier. The matrix is stored in a set of the chips, and the vector to be multiplied is fed through the chip set.

tioning where instead of each processor handling an entire large word, each processor handled one bit of each word," explains Morton. The number of chips that are required to perform an application, therefore, is determined by both the size of the matrix—each chip can hold a 256 × 256 segment—and the precision of the numbers in the matrix, as one set of chips is required for each bit of precision. Like a conventional by-1 memory chip, the intelligent memory chips are put in an array in which each chip holds 1 bit of each number from the matrix.

Inside the chip is the 256-word × 256-bit matrix memory. There's also a memory for holding and reorganizing the vector as it's passed through the chip. "Enough vector memory is provided to double-buffer a 16-bit vector," Morton says.

Bits from the matrix memory and the vector memory come together, 256 at a time, in a bank of 256 1-bit multipliers. These 1-bit results are fed to a block of tally logic that begins the accumulation process, keeping track of which 1s go where in the resulting vector.

From the tally logic, results are clocked into a vector accumulator chip that brings the products from all the memory chips together and assigns weights to them, forming a fully significant product vector.

As in the case of the CADM, enlarging the matrix increases the number of chips and, therefore, the number of processing elements. Hence, the matrix's size and precision have only a second-order effect on the time required for an operation. In fact, a user could intentionally partition a relatively small matrix among numerous banks of intelligent memory chips just to increase throughput, Morton notes.

Applications for the part include signal processing, for which matrix multiplication is an important operation. Many similar engineering applications are not targets, however. "This is basically a fixed-point machine," explains Morton. "I'm not sure whether it makes sense in applications that are tied to IEEE floating point. Most of these applications can be done with block floating-point techniques, but right now we've decided to concentrate on fixed-point applications."

Beyond simple matrix multiplication, the flexibility with which Oxford has designed the part opens a spectrum of other alternatives. For one, the intelligent memory chips can be used in a slightly different mode to do convolution for image processing. In convolution operations, pixels get loaded into the matrix memory, and the convolution coefficients are loaded into the vector memory. If the pixels are ordered correctly in matrix memory, the chip will then proceed to convolve the pixels with the coefficients, each clock producing 1 bit's worth of a 256 × 256 convolution.

Another interesting possibility arises in neural network applications. The operation performed by the resistors and summing amplifiers in a Hopfield network is essentially an analog matrix multiplication. Using the speed of a number of Oxford's chips, the same operations can be performed digitally, with elements in the matrix representing resistor values. By using additional external chips, the simulated network can be made to settle at various speeds, or nonlinear operations may be included in the network's feedback paths.

A powerful but delicate tool

In both of these instances, designers have taken an almost self-evident step toward improving system performance. Identifying a task that requires the movement of very large amounts of data through a relatively simple processor, these teams have simply integrated the processor into memory, eliminating the data movement. As a result, one of the most critical of system resources, memory bandwidth, is conserved.

But, in both cases, another important effect occurred. Integrating the processor into the memory resulted in not one processor, but in an array of parallel processors: comparators in the CADM, and 1- × 1-bit multipliers and tally logic in the Oxford chip. The proliferation of these parallel processing units has at least as much effect on system performance as the elimination of unnecessary data movement.

It's clear that for some applications, this intelligent memory approach can yield enormous speed improvements while actually reducing demands on the rest of the system. But finding the susceptible applications can be tricky. Obviously, they must involve large amounts of data and they must be inherently parallel at some level. Beyond these simplistic observations, it's not clear what, if any, additional intelligent memory applications are out there waiting to be exploited. **CD**

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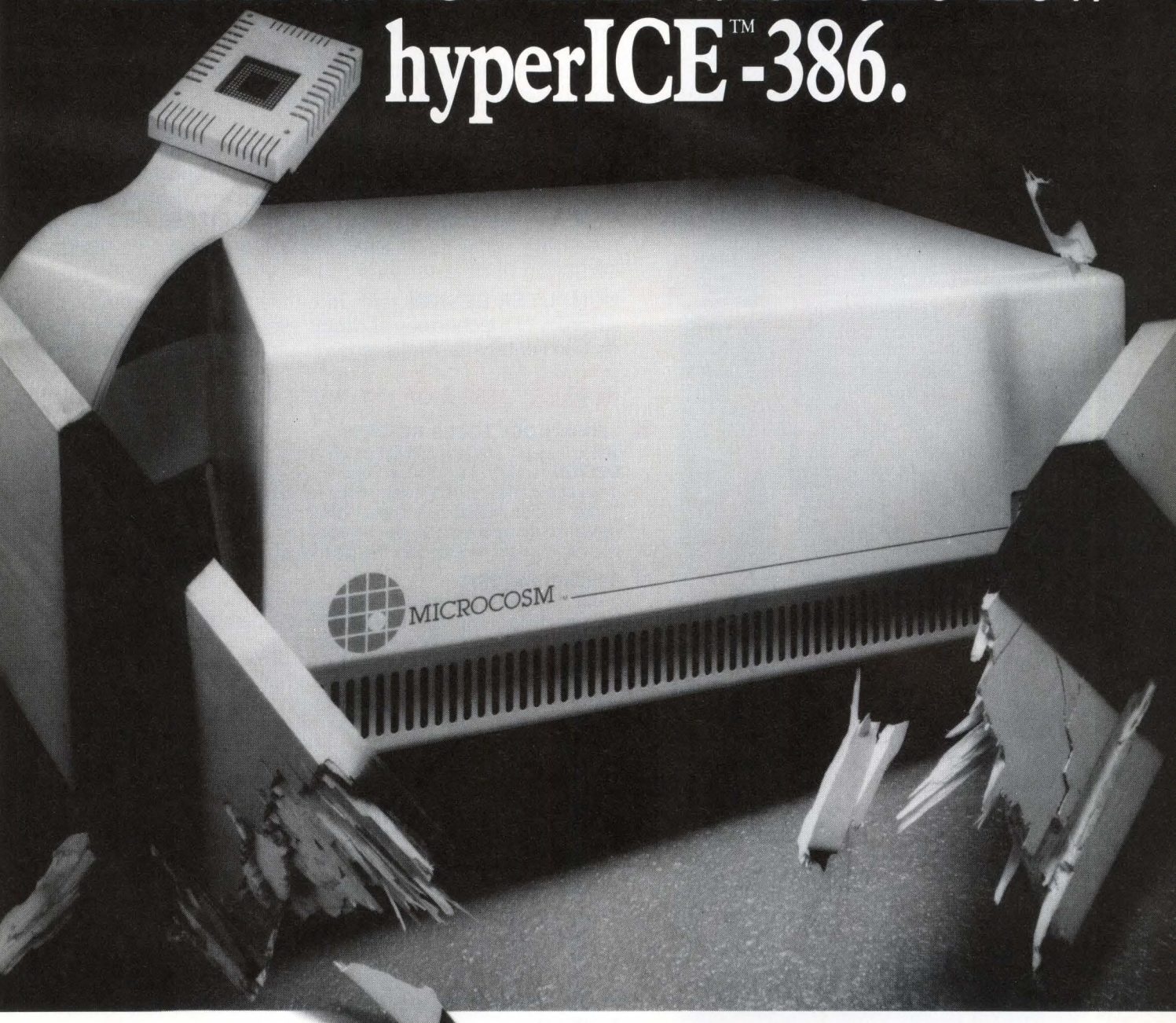

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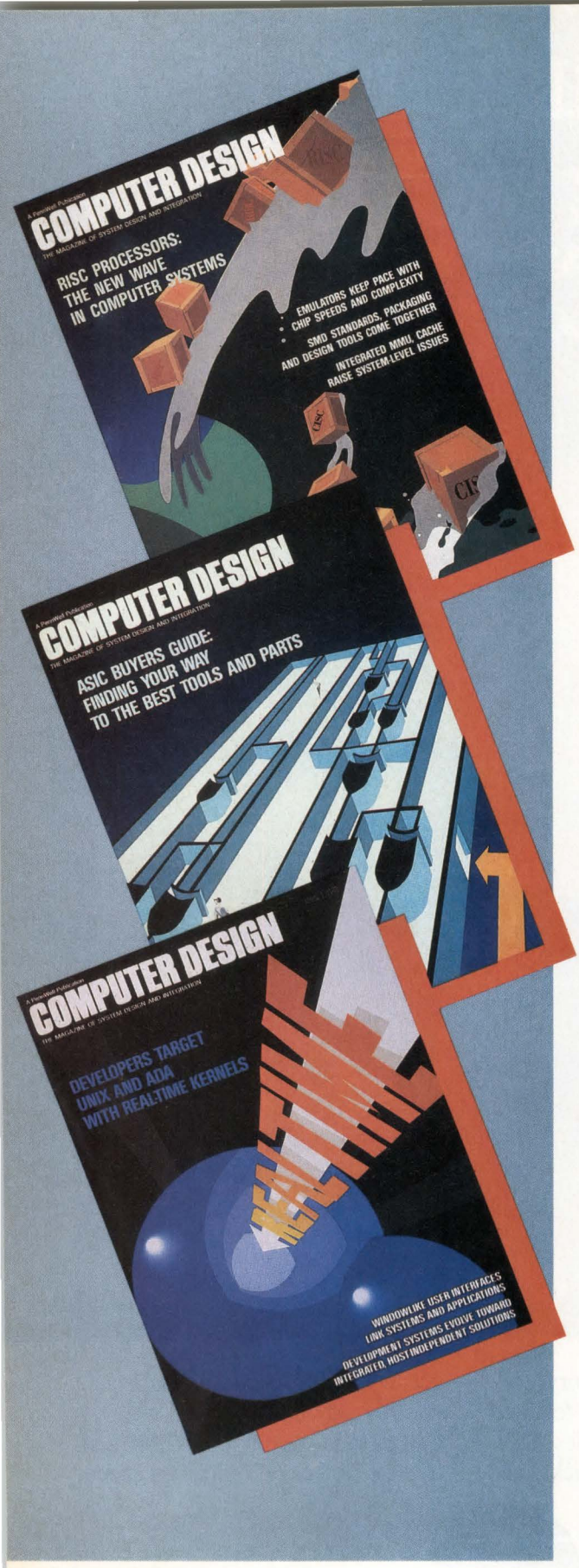

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Erasable optical media promises data-storage breakthroughs

The Holy Grail of data storage may have been found. Tandy (Fort Worth, TX) has announced the development of erasable optical media. No, it's not magneto-optic technology; it's a technology that can, for instance, be read by existing compact disk (CD) players. But it's a basic new form of optical media that can also be produced in sizes and formats other than CD-ROM. Called Tandy High-intensity Optical Recording, or Thor, the technology is based on a type of dye polymer used in the recording surface, described as "our special sauce" by Lynn Haley, Tandy's marketing information representative. The recipe, of course, isn't for public consumption.

Tandy's Thor technology is built upon media technology developed by and licensed from Optical Data (Beaverton, OR). A laser beam of a specific wavelength heats the two-layer media, causing the lower layer to expand and push up the top layer. The top layer cools faster than the lower layer and retains the raised shape until heated by a beam of a different wavelength, which causes it to flatten out. A laser beam striking these bumps is reflected differently than when hitting the smooth surface, thus letting photodetectors distinguish between data bits in exactly the same manner as with other optical media in which pits are permanently burned.

One key concern with erasable media is its robustness, or how many read/write cycles it can sustain without deteriorating. Tandy is trying to establish some data on the robustness of its new media. So far, there has been no noticeable degeneration of the media for up to about 100 cycles, says Haley, adding that the company "doesn't know yet" what the media is really capable of. The media has proven, however, to be fairly resistant to the environment.

Another question of primary interest for data storage is how data can be overwritten. In write-once media, the bumps, of course, are permanently burned into the media and data can't be overwritten. In magneto-optic technology, an entire track must be erased on one rotation of the disk and the new data written on the next rotation. Even to update one sector, magneto-optic recording requires two rotations of the disk. Tandy is closed-mouthed about the actual method of rewriting data in a data-storage context.

Tandy director of marketing Mike Grubbs did indicate, however, that the bumps in Thor media are analogous to flip-flops in that they change state each time the proper wavelength and energy of laser light strike them. And the material is known to change state in response to the wavelength of laser light: one wavelength creates a bump, another flattens out a bump. In addition, the wavelength that flattens a bump doesn't affect the surface if it's already smooth.

Data, therefore, can theoretically be overwritten on a single revolution if media passes under the laser that smooths the bumps just before the laser that writes new data bumps. Donald Mattson, Optical Data president, emphasizes that this lead/lag method hasn't yet been perfected, but the company is reasonably confident it can be.

Thor-based products

Since the technology is so basic, Tandy is interested both in developing its own products and in finding partners to develop and produce products based on Thor technology. The first product from Tandy will be an audio CD recorder/player that will sell for less than $500. The recorder/player will be able to play commercially available CDs as well as record on Thor CDs, making it a clear rival to digital audio tape. The price of media is predicted to be about $12 to $20 per disk.

Tandy is also working on a data-storage product that will employ the CD-ROM format but will be erasable. CD-ROMs currently store 600 Mbytes on one side, but Tandy believes its Thor technology has the potential to go to higher recording densities. Just how high, no one knows—or no one will say. The audio product will be the first out the door and is expected to be available in 18 to 24 months. The data-storage product will require more development because it will require higher precision and error checking. It's also possible that the aforementioned erase-before-rewrite problem may be complicating the design. A CD disk drive product, therefore, is projected to be available in about three years.

The matter of access time

Access times for CD-ROMs are comparable to those of floppy drives, rather than of Winchesters, due mainly to the mass of the laser heads. This isn't a problem for an audio product that tracks continuously inward, but a data-storage product requires rapid acceleration of heads among randomly selected tracks, and the mass of the heads affects the ability to accelerate them. But there are hopes that low-mass holographic heads will be developed that will dramatically reduce access times by eliminating most or all of their glass optics.

When asked about the laser energy required to create bumps as opposed to that used in write-once media, Grubbs became circumspect. "Media characteristics will let us do it [reduce laser energy] with reasonable confidence" is all he would say. Reducing laser energy requirements is crucial, of course, to reducing the mass of the laser heads and improving access time. **CD**

Tom Williams
Western Managing Editor

Coming June 15

Look for Contributing Editor Art DeSena's technology focus report on IC testing.

Analog/digital simulator tackles board-level designs

Although there have been numerous solutions for mixed-mode, or analog/digital, simulation, most are limited to either specific types of problems or to small amounts of analog circuitry. The Saber/Cadat product announced in late May by Analogy (Beaverton, OR) and HHB Systems (Mahwah, NJ) may be the first mixed-mode solution capable of handling a wide range of board-level designs.

Saber/Cadat brings together two popular simulators—the Saber analog simulator from Analogy and the Cadat digital logic simulator from HHB Systems. Unlike most other analog simulators, Saber permits modeling from the circuit level to the behavioral level and can model non-electrical devices such as servos and motors. Cadat provides a range of modeling levels and supports hardware modeling and acceleration.

What really makes Saber/Cadat an asset to board-level designers is its ability to model analog and digital components at a behavioral level. Most existing mixed-mode simula tors, in contrast, support analog modeling at only the transistor level. "By using the Saber/Cadat system, you can extend a mixed-mode capability across chips, boards and systems. You can go all the way down to the circuit or gate level and all the way up to the behavioral level," says David Smith, engineering vice-president at Analogy.

Richard Goering
Senior Editor

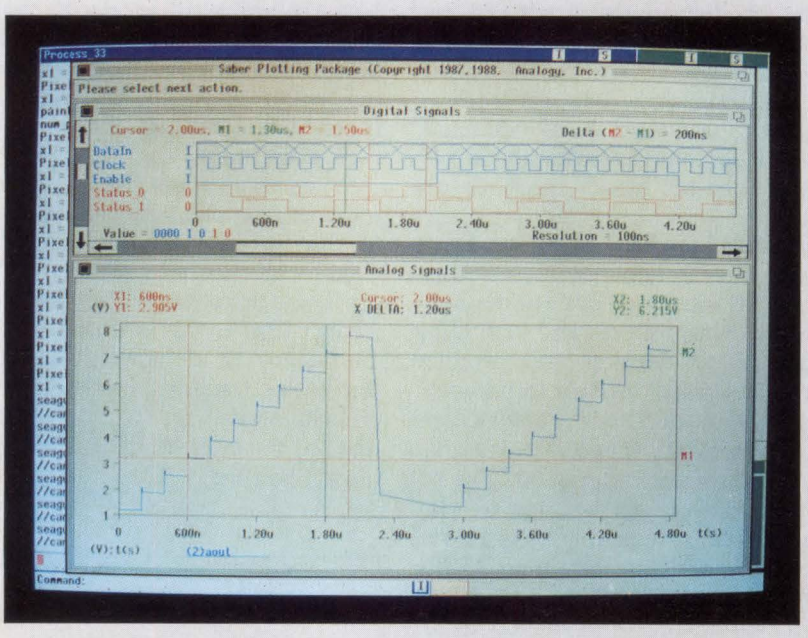
Limits of Spice

Most mixed-mode environments today use analog simulators that are based on Spice, a public-domain simulator developed at the University of California at Berkeley. The Viewsim A/D product from Viewlogic (Marlboro, MA), for example, links the company's digital simulator to PSpice from Microsim (Laguna Hills, CA). Because Spice uses built-in, transistor-level models, products such as PSpice are effectively limited to small chunks of analog circuitry.

Another approach to analog simulation is relaxation, which attempts to find solutions within localized portions of circuitry. In contrast, Spice provides a direct solution for the entire matrix of nodes in the circuit, so it's more computationally intensive. Relaxation doesn't work well for tightly coupled circuits, however, and it's generally aimed at MOS circuitry.

Saber is unique in the analog world because it provides a direct solution and still allows modeling up to the behavioral level. Instead of using built-in models, Saber solves differential equations that can model any type of physical phenomena. According to Analogy, not only is Saber typically 10 times faster than Spice, but the increase in CPU time is linear as circuit size grows.

In the digital world, Cadat has been used extensively to simulate complex boards. Hardware modeling simplifies the modeling issue for board-level designs, and the simulator's worst-case timing verification lets it check various combinations of minimum and maximum component values. Although HHB doesn't provide a behavioral language, behavioral models can be written for Cadat in C.



Saber/Cadat from Analogy and HHB Systems lets board-level designers simulate both analog and digital components up to a behavioral level. This display shows the output from an adaptive-gain stage, illustrating the simulator's ability to handle feedback between analog and digital circuitry.

Synchronization is critical

One of the most difficult problems of mixed-mode simulation is synchronizing the time steps of the analog simulator with the event queue that drives the digital simulator. Only with such synchronization can the mixed-mode simulator handle feedback between analog and digital. In A/D Lab from Daisy Systems (Mountain View, CA), for example, although signals can be fed between Daisy's DSpice simulator and the Daisy Logic simulator, the system can't handle feedback because synchronization isn't provided.

Both Viewsim A/D and Saber/Cadat provide specialized models that synchronize analog and digital

simulators and pass information between them. "The net list inserts what we call 'hypermodels,' which correspond to the interface points between analog and digital," explains Carl Melone, vice-president of product engineering at HHB Systems. "These models can be looked at as behavioral models that have interprocess communications capabilities built into them." Analogy will provide a library of hypermodels that work with the standard digital parts supported by Cadat.

A new technique, the Calaveras algorithm, provides Saber/Cadat with time-step synchronization. "Instead of providing a traditional lockstep algorithm, where the simulators have to go to a certain point in time before they can continue, we let the analog simulator run as far ahead in time as it needs to," explains Analogy's Smith. When a digital event occurs that requires analog processing, Saber can reevaluate its solution and either continue forward in time or adjust backwards in order to maintain accuracy.

Handling X states issued by digital simulators is another problem that occurs in mixed-mode simulation. Instead of attempting to propagate X states through analog models, Saber/Cadat assigns them to their last known value. If there is no last known value, it assigns an arbitrary 0 or 1. Analog models can pass X states to digital models if it's likely that the analog output will cause an oscillation.

To go from analog to digital, thresholds are used to map waveforms into 0, 1 or X states. To go from digital to analog, states such as weak 0s or 1s, strong 0s or 1s, or high-impedance 0s or 1s are mapped into the appropriate waveform. A new technique known as time-domain modeling lets Saber represent discrete state information in analog models.

Integration with CAE/CAD

Since both Analogy and HHB Systems have OEM relationships with many CAE/CAD vendors, Saber/Cadat will be integrated into existing CAE/CAD environments. Its ability to read Electronic Design Interchange Format (EDIF) net lists will facilitate the development of interfaces. Initially, Saber/Cadat will be integrated into the Visula design environment from Racal-Redac (Westford, MA).

Rockwell International (Cedar Rapids, IA), which has helped define Saber/Cadat's specifications, will be the first beta site for the product. Priced from $35,000 to $67,000, Saber/Cadat will be available on Sun, Apollo and VAX platforms in the fourth quarter of this year. **CD**

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CIRCLE NO. 30

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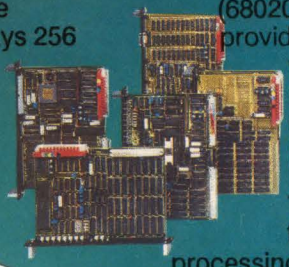

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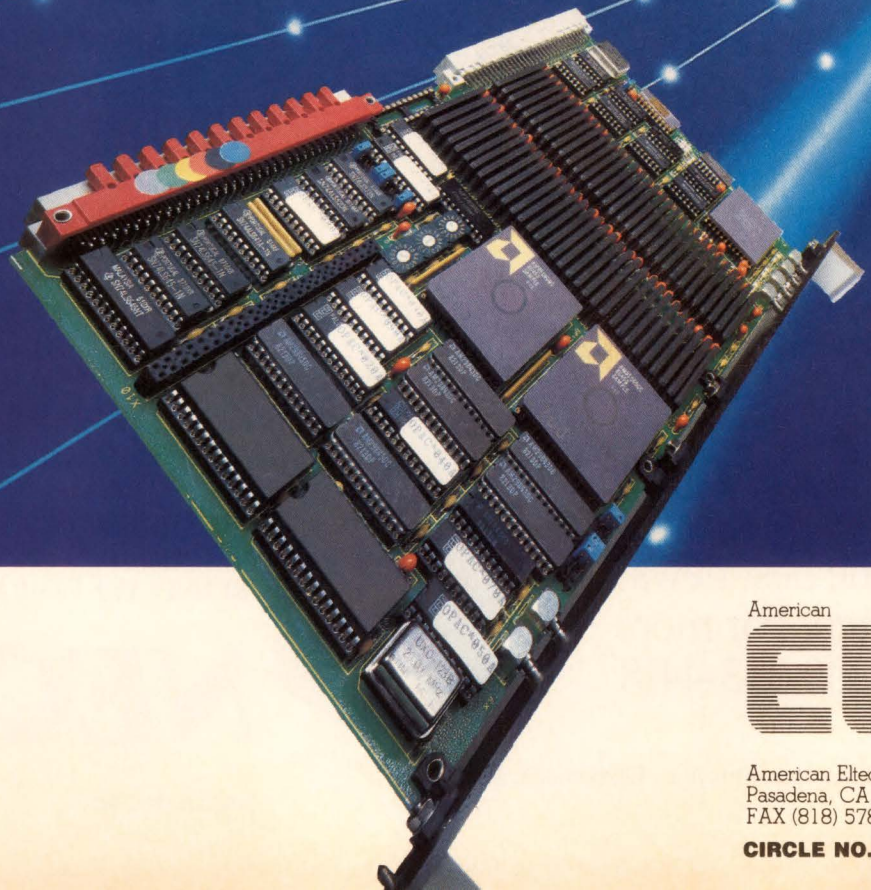

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CIRCLE NO. 21

PCs crack the barrier to high-powered graphics

The ever-blurring line that has existed between personal computers and engineering workstations has recently been all but obliterated by high-performance systems based on the Intel 80386. The introduction of the Sun386i, Models 150 and 250, by Sun Microsystems (Mountain View, CA), and the SYP302 by Intel (Santa Clara, CA) has brought systems that perform in the 3- to 5-Mips range yet retain a link back to the IBM AT bus with a vast array of plug-in modules and to DOS with a myriad of DOS-compatible applications. In addition, the new machines can already run various versions of Unix, including Xenix by Microsoft (Redmond, WA) and SunOS by Sun, as well as the new OS/2 multitasking operating system targeted for IBM's Personal System/2 family. The 80386 seems to stand at the crossroads of all these capabilities.

In terms of CPU power, 80386-based systems that use the AT bus compare quite favorably with other microprocessor-based workstations that use the VMEbus and Multibus. But there's still a major gap in terms of graphics capability available on AT cards that's also accessible to a wide range of DOS applications. All the major workstation manufacturers, including Sun, Apollo and Hewlett-Packard, have invested a great deal of effort in incorporating high-resolution, high-performance graphics into their systems, usually in the form of plug-in graphics boards using commercial or proprietary specialized graphics coprocessors. Most graphics cards for the AT bus, however, were designed for the DOS world, where fairly modest graphics standards were set by IBM. And PC controllers are characterized by the fact that the CPU and the application, rather than dedicated graphics hardware, handle graphics and drawing computations.

On the workstation side, the many controllers available have differing degrees of local graphics intelligence and varying physical architectures. This diversity has pushed users to demand the adoption of graphics standards that can work across all the various hardware. A set of software standards is beginning to gel, including the Graphical Kernel System (GKS) and the Programmer's Hierarchical Interactive Graphics Standard (PHIGS) and its extension for three-dimensional graphics, PHIGS+. In addition, there's a move to standardized, window-oriented user interfaces such as the X Window System, developed by the Massachusetts Institute of Technology (Cambridge, MA), and the Network extensible Window System (NeWS) from Sun. The highest performance systems using advanced and proprietary hardware are, of course, the ones with the least support of graphics standards.

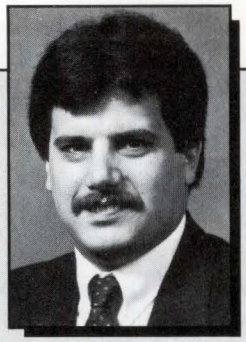
Enter the 80386-based workstation with its array of 16-bit AT card slots. Very little exists for the AT bus in the way of workstation-class graphics controllers that are also in a position to attract graphics standards, and there's even less that adheres to the kinds of graphics standards being adopted by workstations, and still less that's both high-performance/high-resolution and

Meeting the need for higher graphics capability in the OEM workstation market, the Intel SYP302 is a 25-MHz 80386-based system that uses the IBM AT bus. It's fully FCC-certified so that system designers can begin adding value with software innovations and plug-in AT modules.

Tom Williams
Western Managing Editor

accessible by the existing base of installed DOS applications. This isn't to say that there aren't higher performance board-level graphics controllers for the AT bus. But in terms of workstations, some of which support interactive 3-D solids modeling with smooth shading, surface rendering, lighting models and even ray tracing, they would be at best classified as mid-range performance controllers. Examples are the SM-1281 visualization engine from Matrox (Dorval, Quebec), which controls a 1,280-×1,024-pixel display, runs at 90,000 3-D vectors/s and includes hardware Gouraud shading and 16 light sources. There's also the Pro 1280 from Number Nine Computer (Cambridge, MA), which displays 1,280×1,024 4- or 8-bit pixels.

The companies that produce higher performance graphics boards for the AT platform have had to leave the safe world of DOS graphics standards and target specific applications such as desktop publishing systems or Autocad, the PC-based computer-aided drafting package from Autodesk (Sausalito, CA), or some other set of specific applications large enough to reward their efforts. They also have had to supply application-specific drivers for their own boards and provide backward compatibility to an IBM standard, usually the Color Graphics Adapter (CGA), to let standard DOS applications run.



Greg Reznick
Director of Marketing
Video Seven

IBM's 8514/A can give PCs workstation-level graphics

In many ways, personal computers have become powerful enough to compete with workstations. But there's at least one area where PCs still can't match the power of workstations—graphics. This shortcoming limits the design work that can be performed on PCs.

The level of graphics available for PCs still doesn't offer enough resolution, color selection or processing speed to let serious design work such as computer-aided design and drafting (CADD) migrate downward from workstations to PCs. Many graphics pundits would argue that PC graphics require a minimum resolution of 1,024×768 pixels, while simultaneously offering 256 on-screen colors, to effectively compete with workstation-quality graphics.

The prevailing PC graphics standard, the Video Graphics Array (VGA)—introduced by IBM with the Personal System/2—offers 640-×480-pixel resolution with 16 simultaneous on-screen colors. But beyond VGA is 8514/A, an advanced PC graphics adapter also announced by IBM with the PS/2. As offered by IBM, the 8514/A provides 1,024-×768-pixel resolution and 256 on-screen colors, thus providing an adequate solution for workstation-quality graphics on a PC. But the 8514/A offers more than just high resolution and many colors: It provides a significant increase in graphics processing speed—perhaps its most attractive feature.

To fully utilize the power of advanced 80286- and 80386-based machines, graphics adapters—the boards that control the information flow from the processor to the monitor—must be fast enough to keep up with the lightning-quick CPU. But most of today's VGA boards are too slow to let PC graphics compete with workstation graphics.

The 8514/A architecture is that of a graphics engine rather than of a video controller. Because it isn't a graphics engine, the VGA requires the host CPU to manage the display memory. If the program needs to draw a line on the screen, for example, it must compute which pixels

The importance of VGA compatibility

Since IBM's introduction of the Video Graphics Array (VGA), which supports a display of 640×480 4-bit pixels (16 colors), board makers for the AT platform are starting to produce boards that are first and foremost VGA-compatible. The board makers then add value by including the ability to drive displays at higher resolutions. For this higher resolution capability, they must supply their own drivers to run specific applications, as before. To date, the most popular applications to support are Autocad, Xerox Ventura Publisher from Xerox (Rochester, NY), Microsoft Windows from Microsoft, and the Graphics Environment Manager (GEM) from Digital Research (Monterey, CA).

An ever-increasing number of board manufacturers are making VGA cards, and some of them have done their own chip designs. In addition, four or five chip makers are supplying VGA ICs, including Chips and Technologies (San Jose, CA), Tseng Laboratories (Newtown, PA), Cirrus Logic (Milpitas, CA) and Paradise Systems (Brisbane, CA). A fifth player, Trident Microsystems (Santa Clara, CA) is expected to announce a VGA chip soon.

George Alexy, vice-president of marketing for Cirrus Logic, feels that VGA will become the basic display standard in AT bus systems. If this happens, manufacturers of compatibles will need to gear up quickly to meet the demand. Award Software (Los Gatos, CA) has put together a manufacturer's kit designed to help manufacturers of AT compatibles include VGA capability with virtually no design effort on their part. The kit includes the Cirrus VGA chip, a fully functional VGA board using a basic I/O system developed by Award, negatives for making the PC board, a bill of materials for the parts, a complete user's manual that can be relabeled and reprinted, photos, and spec

to turn on and then access display memory directly to effect the change. This doesn't create much overhead in a low-resolution system, but in a system with 256 kbytes or more of memory in the display buffer, the computation and manipulation time can be quite significant. A graphics engine, on the other hand, controls the display memory independently of the CPU. To draw a line, the CPU need only specify the endpoints of the line, and the graphics engine does the rest. Such capabilities let the graphics engine offload a tremendous amount of work from the host CPU while simultaneously displaying graphic images much more rapidly.

The 8514/A also uses powerful video RAM (VRAM)—memory specifically designed for video controllers—as a way to speed PC graphics performance to near the level of workstation graphics. By contrast, nearly all PC VGA boards use dynamic RAM—which was designed for system memory, not video memory—thereby creating a bottleneck in advanced 80286- and 80386-based PCs.

VRAM chips, although basically a superset of DRAMs, provide dual data ports that let information flow to or from two different sources at the same time. DRAM has a single port to receive data from the processor and send it to the monitor. VRAM features a serial port, in addition to a parallel port, letting one data port receive information from the host processor while the other port is already transferring data to the screen. The dual-port design of VRAM lets the 8514/A perform screen updates in CADD applications up to 10 times faster than a VGA board that uses DRAMs only.

As PC software vendors design more and more CADD applications for 80286- and 80386-based PCs, graphics boards must provide the resolution, color selection and, most important, the speed needed to do serious design work on a PC. The 8514/A, with its graphics engine and VRAM, provides a graphics platform that meets these requirements.

sheets and marketing materials. It's priced at $7,500.

Competition in the VGA arena is mainly in three areas: compatibility, performance and extra features. Everyone seems to agree that hardware compatibility is extremely important. "One hundred percent compatibility is an absolute must before you can do the other things," says Johanna Ohlson, product marketing engineer for graphics at Chips and Technologies. "You've got to start from a baseline of gate-level compatibility." The "other things" to which Ohlson refers are features that enhance performance and allow greater resolutions than what has been defined by IBM.

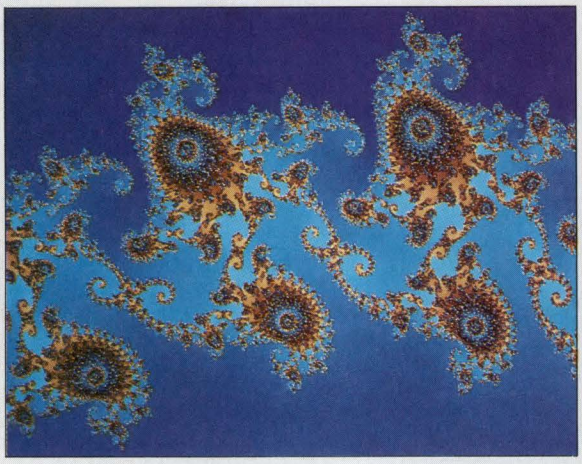
One such extended feature, a hardware cursor, is built into VGA chips made by Chips and Technologies and by Video Seven (Fremont, CA), which uses the chip in its own board-level products. Implementing the cursor in hardware saves 30 percent in software overhead, according to Ohlson, because the cursor is a 32- × 32-pixel graphics cursor. Without this feature, the CPU has to save the display pixels from the new location, write the cursor pixels to the frame buffer at the new location and also write the previously saved pixels back to the old location no longer occupied by the cursor. With a hardware cursor, all that saving and writing is done by the VGA chip. The CPU simply specifies the location of a single point of the cursor.

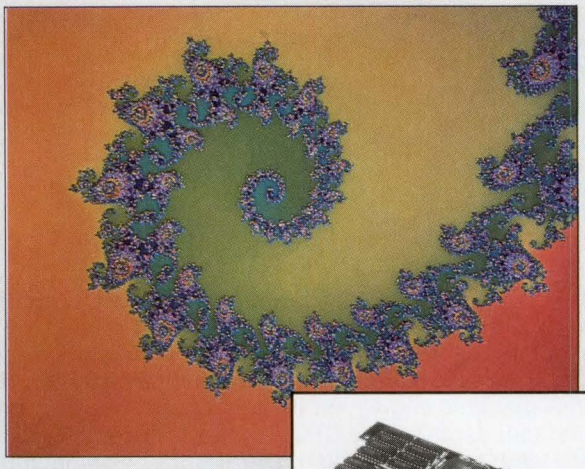
Previous IBM graphics standards use digital monitors. VGA, however, specifies an analog monitor, so upgrading from EGA to VGA often requires purchasing one of the newer multisynch monitors. The Designer VGA by Orchid Technology (Fremont, CA), however, provides a TTL port as well as an analog port so that as long as one sticks to the strict VGA specification, one can upgrade using an existing Enhanced Graphics Adapter (EGA) monitor. Video Seven recently announced a V-RAM VGA card that uses video RAMs in its frame buffer to give the CPU almost no-wait-state access to video memory.

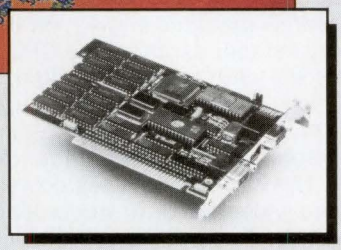
All the IBM graphics standards through VGA, however, predate the appearance of 80386/AT systems. According to Walt Penny, vice-president of Media Cybernetics (Silver Spring, MD), these systems are facing a "price/psychology barrier that must be broken." On the one hand, he says, people need to realize that these relatively inexpensive systems aren't just superfast DOS machines, but are platforms fully capable of running Unix and Unix applications. On the other hand, the Unix world needs to become friendlier in terms of standard applications and user interfaces that can migrate to 80386/AT systems. And in between these two, says Penny, there's a need for a graphics standard that can reside on the AT bus and be compatible with at least some Unix standard, such as the X Window System. Such a standard hasn't yet been clearly identified.

PC graphics beyond VGA

While the competition and innovation in the VGA arena is fierce, VGA doesn't appear to satisfy the performance and resolution needs of certain applications such as CAD. IBM apparently recognized this when it introduced, in addition to the VGA standard that's implemented on the mother board of the PS/2, the







Courtesy: Orchid Technology

IBM's Video Graphics Array (VGA), now available on AT-compatible systems from many manufacturers, defines a 16-color, 640-×480-pixel display. Most board manufacturers, such as Orchid Technology with its Designer VGA, also offer extended colors and resolutions. The fractals in these displays are rendered at 640×480 pixels with 256 colors.

8514/A, a higher resolution display adapter card.

The 8514/A has a resolution of 1,024×768×8-bit pixels and can display 256 colors from a palette of 260,000. As implemented by IBM, the 8514/A uses a monitor with interlaced scan, which lets it run at lower frequencies than noninterlaced monitors. As resolution increases, however, so does the processing burden. The 8514/A has over 2½ times the number of pixels as a 640-×480-pixel display (VGA). Because of this increase, the CPU must be relieved of the computation burden and an intelligent graphics coprocessor must be used.

Given the fact that VGA is on the mother board of PS/2, and given the fact that OS/2 will also run on AT machines, VGA will be "a fundamental display capability that comes...as a part of the basic system architecture" of 80386-based platforms on the AT bus, according to Cirrus Logic's Alexy. He also predicts that the 8514/A will then be an enhanced capability for specific applications that need it. But, unlike before, this enhanced display will have IBM's blessing, forming a "center of gravity for software," or a standard to which third parties can confidently write applications.

So far, no 8514/A products have been announced for the AT bus, but Compaq Computer (Houston, TX), Verticom (Sunnyvale, CA) and a number of other companies are reported to be readying board-level products. And Chips and Technologies and Video Seven—and probably others—are busily reverse engineering the 8514/A chip set. Thus, it appears that the 8514/A is in line to be the next AT-bus graphics hardware standard. The question is, will the 8514/A be able to boost graphics performance of 80386/AT platforms into the workstation arena? In other words, will it be able to run at least an X Window graphic user-interface efficiently?

Stages of emulation

The 8514/A is really three things: It's the type of interlaced-scan monitor introduced by IBM; it's the application interface (AI), the software interface defined in England by IBM; and it's the chip set developed by IBM upon which the standard is built. "The first level of 8514/A boards is going to be using the Texas Instruments 34010 and emulating 8514/A," says Craig Lynar, vice-president of marketing for Orchid Technology. The next level, he says, will be the hardware with custom VLSI chips.

The TI 34010 appears to be the graphics coprocessor of choice for 8514/A emulation because of its programmability. This level of emulation will, of course, be at the AI level since it's in software. But software emulation of the 8514/A AI isn't going to satisfy the performance demands of most manufacturers, no matter how fast TI can clock the chip, even though TI is sampling a 60-MHz version.

Media Cybernetics' Penny points out that 8514/A emulation in software requires "a very large investment in software resources." You have to either port your software into TI's native code, or implement the interface by means of calls to subroutine libraries supplied by TI—a method that has serious effects on performance, he says.

Greg Reznick, director of marketing at Video Seven, agrees. "The penalties are still too high to emulate 8514/A with a software interface," he says. Besides, one must differentiate between what's needed for line drawing, where the software emulation appears to do fairly well, and managing a window environment,

where, according to Reznick, 8514/A emulation falls on its face. Not only do the bit map and bitblt (bit boundary block transfer) operations represent a lot of overhead, but the application is looking at two layers of software—the window layer and the AI layer.

But Ahmed Nawaz, graphics marketing manager for TI's microprocessor products, disagrees with Reznick. "We've found that compared to Autocad running on the IBM 8514/A on a Model 50, our 34010 emulation is at equal or faster speed." Of course, Autocad is primarily a line-drawing program. TI supplies an 8514/A emulation library, which Nawaz says lets current 34010-based boards upgrade to 8514/A AI emulation with no hardware change.

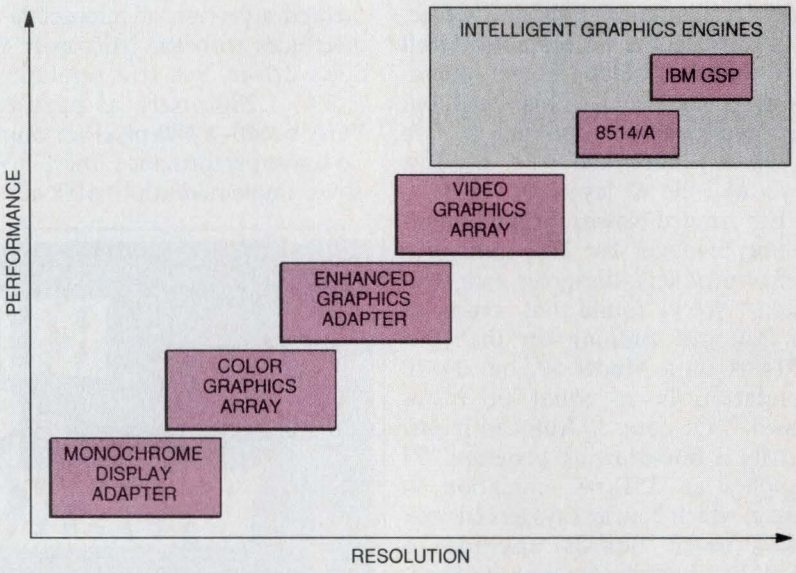
Interestingly, in the process of reverse engineering the 8514/A silicon, some people have discovered that, as Reznick says, "8514/A is more powerful than IBM is letting on, and being AI-compatible isn't the same as being 8514/A-compatible." For instance, the silicon can drive noninterlaced displays and support higher resolutions, he says. Video Seven discovered the chips had additional address lines that weren't even hooked up, so the full possibilities of the silicon haven't been unraveled.

A bridge to Unix

Already, there are efforts underway to build bridges to the kinds of user interfaces that are gaining acceptance in the Unix world, mostly the X Window environment. Microfield Graphics (Beaverton, OR) appears uniquely positioned to track the moving targets of AT-based graphics interfaces. Because Microfield's T-8 controller uses a microcodable bit-slice processor, the board can be programmed in microcode to look like any of a number of hardware engines, or to interface directly to a chosen software driver. "It's about the softest piece of hardware anyone's come up with," says Sam Mallicoat, Microfield president.

Microfield is looking at supporting window environments with the T-8, and the company has implemented a version of microcode that interfaces with the Microsoft Windows driver, but at a resolution of 1,024 × 1,280 pixels, as opposed to VGA's 640- × 480-pixel resolution. To boost performance, the T-8 Windows implementation offloads the cursor control to the microcode, thus relieving the CPU overhead in much the same way as the hardware cursor that was implemented by Chips and Technologies and Video Seven in their VGA chips.

Microfield has also done a microcoded X-server for the Unix-based X



Each successive graphics standard defined by IBM has brought higher resolution and more colors—and a demand for higher performance. Beyond the Video Graphics Array (VGA) at 640 × 480 pixels, IBM has already defined the 1,024- × 768-pixel 8514/A display adapter card, which takes over much of the graphics processing from the CPU. To go beyond that in resolution and performance, IBM has already talked about developing a true 32-bit graphics system processor (GSP), the details of which are still unknown.

Window user interface. A server is the piece of code that presents a standard interface between Unix applications and different display hardware, letting applications running on remote systems on a network be displayed via the local workstation's X-compatible server Such a microcoded X-server can display DOS applications—running on a remote DOS machine or locally within the X environment—by trapping VGA code, for example, and sending it to a DOS window running under X. Even those "badly behaved" applications that write directly to hardware registers could be handled and displayed, according to Mallicoat. Beyond that, he says, there could conceivably be a DOS that could run X Windows and have access to remote Unix applications on the network. Thus, while the key to bringing 80386/AT systems into the Unix workstation world is partly an issue of graphics performance, it's at least equally an issue of compatibility with accepted Unix network user-interface conventions.

While the microcode approach appears to offer great promise for a seamless path of continuity between DOS and some level of Unix graphics applications, there's still a possibility that independent manufacturers could build on the yet untapped capabilities of the 8514/A silicon. Should it turn out that the 8514/A chip set has the hardware capability to run efficient bit-map control and windowing functions, it could also provide a basis for an X-server.

But, as Orchid Technology's Lynar points out, "What's still missing here is the VGA side," meaning that an AT board should incorporate both VGA and 8514/A so that all applications could run on a single monitor and occupy only one card slot. If that happens, and if it turns out that window environments can run efficiently on the 8514/A hardware at high resolutions, the 80386/AT connection might make an elegant bridge between DOS and Unix and between their two universes of applications and plug-in hardware functionality. **CD**

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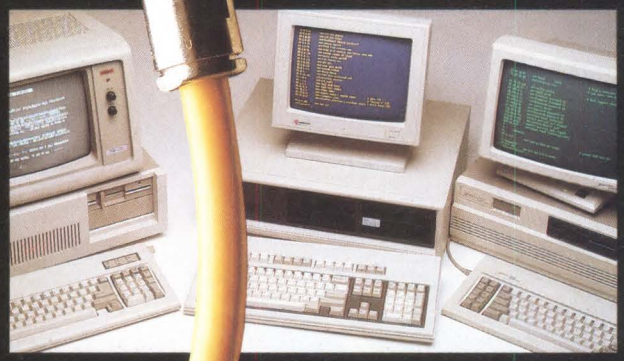

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8-bit processors demand attention as integration, speed evolve to new levels

Revolution always seems to get the front-page headlines; evolution, meanwhile, gets buried far back in the science section. So it hasn't been very easy to notice the evolutionary changes sweeping the 8-bit microcomputer world. But the changes are there—slowly paced, perhaps, yet in their aggregate they're profound enough to alter the way managers must approach these essential chips.

In the case of 8-bit microprocessors and microcontrollers, evolution is driven by improving silicon process technology. As geometries shrink, simple microcontrollers become cheaper and move into new applications. Mid-range microcontrollers absorb many of the devices that used to require additional chips. High-end 8-bit parts blur the lines between microcontrollers and microprocessors, as well as the lines between 8- and 16-bit applications.

To take optimum advantage of today's 8-bit processors, a manager needs to rethink some of the fundamental ideas about parts choice, system partitioning and performance requirements.

Logic replacement rides again

Perhaps the most profound, and most easily overlooked, change in the 8-bit world is the collapse of prices for simple 8-bit single-chip microcomputers. High-volume rates for mask-programmed parts are below $1, and even EPROM-based parts in quantities of one or more can drop below $5. These prices reopen a whole arena of applications that long ago gave microprocessors their start: logic replacement.

Because the big change has been in price rather than in functionality, its implications may have gone unnoticed by some designers. "We may have overlooked the ability of these parts to do noncomputing chores," speculates Mitch Little, product marketing manager for VLSI products at SGS-Thomson Microelectronics (Phoenix, AZ).

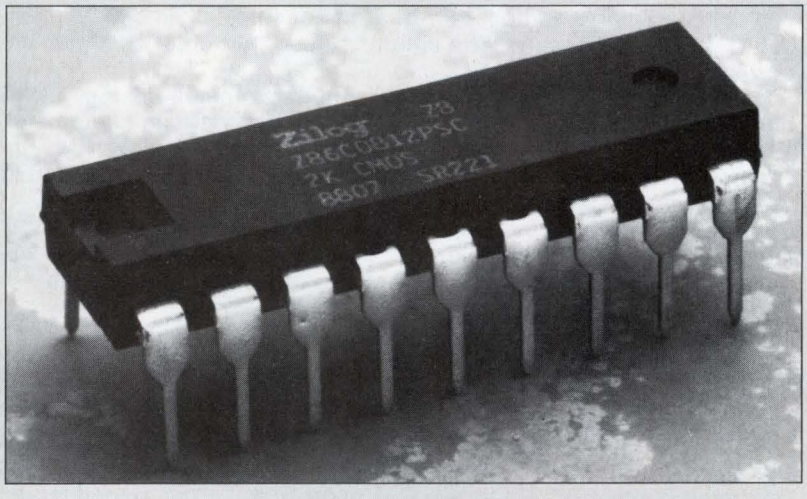
Steve Marsh, manager of MCU marketing at Motorola (Austin, TX), agrees. "At low data rates, even a basic first-in, first-out register may be more expensive than a microcontroller chip," he says. "We're starting to see more microcomputers used as state machines, but engineers still seem surprised by the idea when you first mention it. Still, when you can get an HMOS version of the 6804 in quantity for 49 cents, it's an option you have to look at."

Integrating functions

Advances in process technology can make a microcontroller die smaller, which reduces cost. They can also make room for additional functions on the chip. This aspect of improving technology—the opportunity to integrate more devices—is now being exploited by virtually all vendors of 8-bit microprocessors and microcontrollers.

Added devices on the microcontroller chip can be useful to the system designer in either of two ways. If the system is size-critical, the microcontroller may be able to absorb some peripheral equipment that used to require additional chips. Specialized memories, serial bus interfaces, universal asynchronous receiver/transmitters (UARTs) and analog-to-digital converters are recent examples of such additions.

In speed-critical systems, hardware features may be added not to reduce chip count, but to accelerate critical code paths. Virtually all microcontrollers use counter/timers in this capacity. But some newer chips add hardware with a more subtle effect on system performance, such as data pointers and direct memory access controllers to speed data movement.



One of the features of Zilog's newest Z-8 product is its package. The Z86C08 fits a 12-MHz Z-8 CPU, 2 kbytes of ROM, 124 registers, dual counter/timers, dual analog comparators and 14 I/O lines into an 18-pin DRAM-style package.

Ron Wilson
Senior Editor

Compilers for single-chip microcontrollers?

Conventional wisdom has it that 8-bit microcontrollers and high-level languages are fundamentally incompatible. The chips have irregular instruction sets and lots of specialized hardware, both of which make life difficult for a compiler's code generator. The applications typically involve logic replacement, not the sort of thing for which C or Pascal was intended. And the relatively tiny memory spaces of the single chippers simply don't have room for a big compiled object module. So says conventional wisdom.

But a pair of trends are gradually undermining this view of microcontroller programming. First, traditional microprocessor architectures are showing up in single-chip parts, opening the microcontroller arena to high-level languages originally developed in the CPM world. Second, as average program sizes continue to grow, conventional single-chip parts are showing up with more on-board memory, and use of off-chip memory is increasing.

The 64180 family of processors from Hitachi America (San Jose, CA) illustrates the first point. While the original 64180 was a highly integrated microprocessor, the addition of on-chip RAM and EPROM in the newer 647180 series clearly places this family in the single-chip microcomputer category. The architecture, however, using a superset of the Z-80 instruction set, has brought existing high-level language tools along with it.

"Support software for the family includes the usual assembler and simulation tools," explains Bob Sandler, Hitachi America's multichip microcomputer product marketing manager. "But there are also C and Pascal compilers, a compiled Basic and numerous other third-party offerings. The variety of language options no doubt is helped by the ability to migrate Z-80 tools to the 64180. In addition, the developer needn't be too concerned about the code efficiency of these high-level tools, since the 16 kbytes of on-chip EPROM can be supplemented with up to 1 Mbyte of off-chip memory."

In conventional single-chip architectures, though, memory size and architecture are constraints on compiler design. One company that has taken on these challenges is Micro Computer Control (Hopewell, NJ). MCC has developed a C compiler specifically for the 8051 architecture. "Both chip architecture and efficiency are issues when you're developing a compiler for this kind of chip," claims MCC president Edward Thompson. "The architecture in particular becomes important in a number of ways.

"To begin with, single-chip microcontrollers weren't designed with high-level languages in mind. So the constructs that compilers need, and find in the instruction sets of 16- and 32-bit chips, have to be invented from scratch. Also, in single chippers it's vital to stay close to the hardware. You have to add extensions to C to do assembly-level things such as writing interrupt routines and allocating memory. A typical 8051 user these days will have several memory maps, some on-chip and some off-chip, frequently with overlapping address ranges. The C compiler has to keep track of all of these."

Thompson makes an analogy between the 8050 family and the personal computer, on which his tools run. "In a way, the success of the 8051 has created a de facto standard, just as the success of the IBM PC has. That gives us a stable architecture for which to build tools."

MCC's optimism about the use of compilers in microcontrollers is being echoed in many other areas of the industry. NEC Electronics (Mountain View, CA), which has C support from Lattice (Lombard, IL) for its 7800 and 78300 architectures, certainly concurs. "We believe that a vendor won't have success in highly integrated devices without high-level language support," asserts P.K. Dubey, NEC Electronics' business operations manager.

Sophisticated communications

UARTs were the first complex peripherals to show up on-chip, usually supporting one relatively slow asynchronous line. But the sophistication of integrated serial communications controllers has grown to the point where in some new parts it's difficult to decide whether the chip is a microcontroller with a communications port or a communications interface with an added microcontroller.

One example is the 180-NPU from Hitachi America (San Jose, CA). The chip contains a 64180 microprocessor CPU—essentially a greatly enhanced Z-80, one normal asynchronous serial interface and one sophisticated multiprotocol interface. The latter can be initialized to operate in asynchronous mode or to handle either character-oriented (such as bisync) or block-oriented (such as HDLC) synchronous protocols.

The combination of protocol controller and programmable microcontroller lets several layers of communications protocol be handled in one chip. To keep I/O from being a bottleneck at the relatively high data rates involved in synchronous communications, Hitachi has equipped the chip with dual DMA controllers.

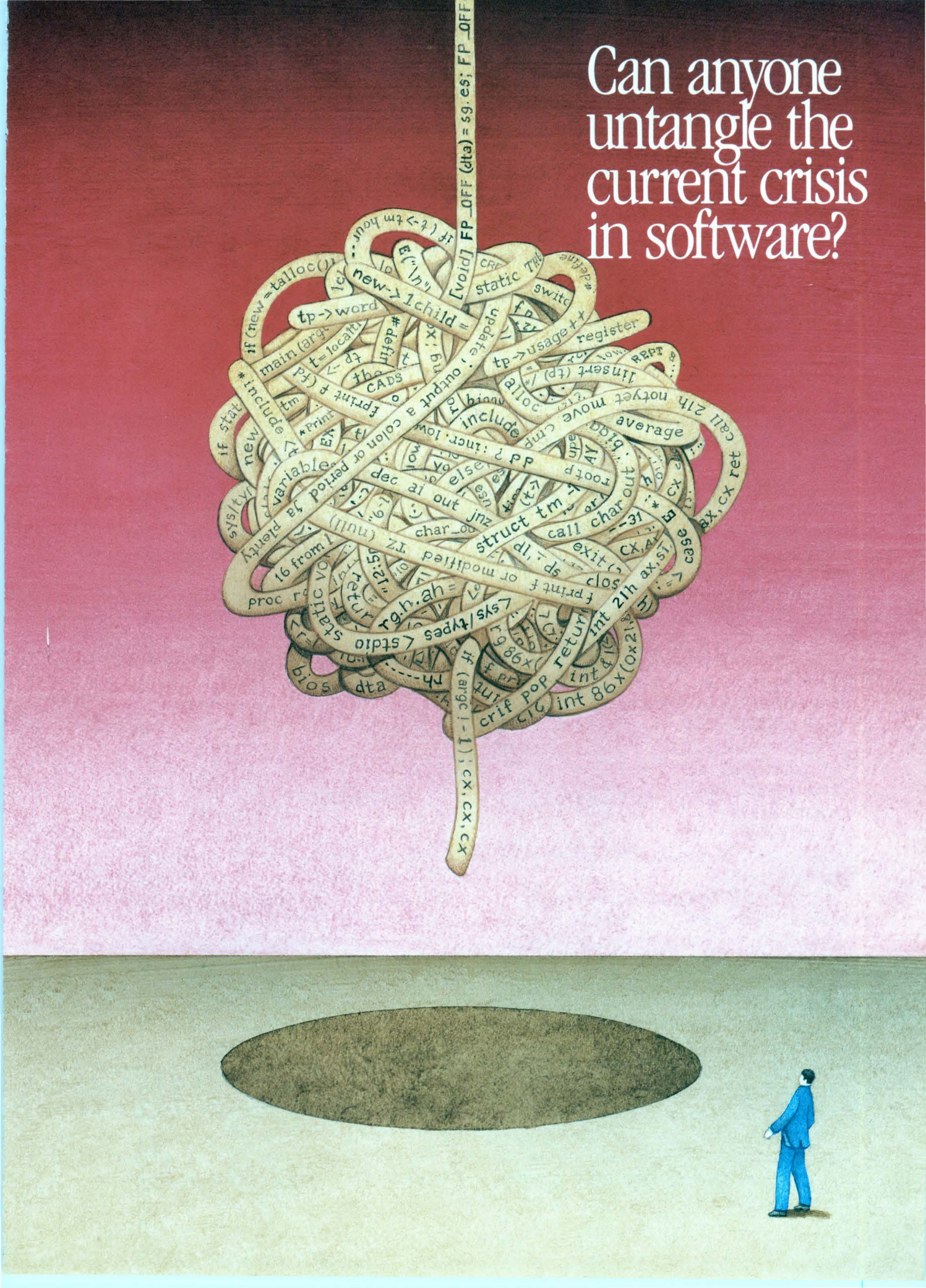
Intel (Chandler, AZ) has provided a sophisticated communications controller on a member of its 8051 family as well. The 83C152 communications controller provides capabilities for HDLC and SDLC, but also supports CSMA/CD, the carrier-sensing and collision-detecting lower protocol layers for LAN use. At a sustained 1.5 Mbits/s, the 83C152's interface won't keep up with Ethernet networks, but it's intended for low-cost proprietary networks, ISDN applications and serial bus schemes inside systems.

Serial buses proliferate

Serial buses are becoming much more common in 8-bit microcomputer systems. "We originally introduced a serial bus for our 4-bit product line in 1976," claims Richard Sessions, marketing manager for 8-bit products at National Semicon-

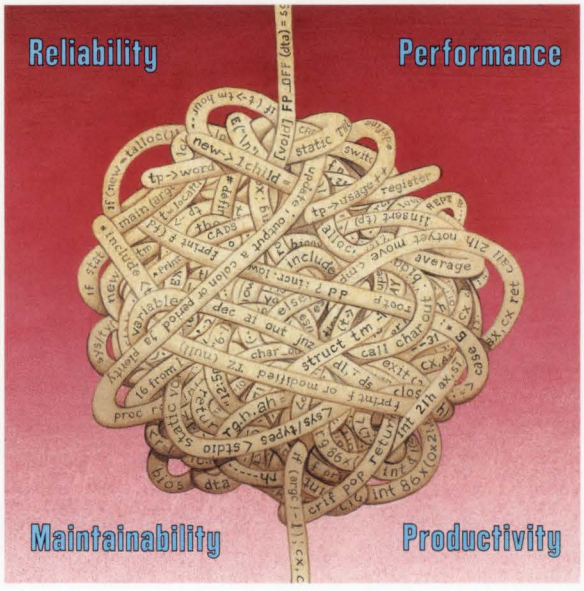
(continued on page 55)

Can anyone untangle the current crisis in software?



Yes! NWIS is renamed MicroCASE and integrates a microprocessor-CASE tool set as global as the crisis itself.

Software engineering is now experiencing a crisis of growing proportion. In order to perform increasingly sophisticated tasks, embedded microprocessor software is expanding geometrically and becoming more complex. Meanwhile, time-to-market demands call for shortened development cycles. The entire crisis is amplified by the latest wave of 16 and 32-bit microcomputer technology now finding its way into more and more products.



At a global level, this crisis involves the entire software development process, from front end analysis and design, through debug and test in the target environment.

But upon further probing, the key concerns quickly subdivide into four major issues: Development productivity, embedded system performance, verifiable software reliability, and long-term software maintainability. All have become tangled in a complex web of costly and oftentimes risky realities.

In response to these single issues, vendors of software engineering tools offer a variety of single solutions. But that is not what's needed. The crisis is global in nature, so it demands global solutions. Only MicroCASE™ offers a global tool set which spans the entire software development cycle. Formerly known as Northwest Instrument Systems (NWIS), the new MicroCASE name more accurately reflects a strategic focus on integrating a complete set of tools aimed at the needs of the microprocessor software engineer.

Probing the four crucial issues.

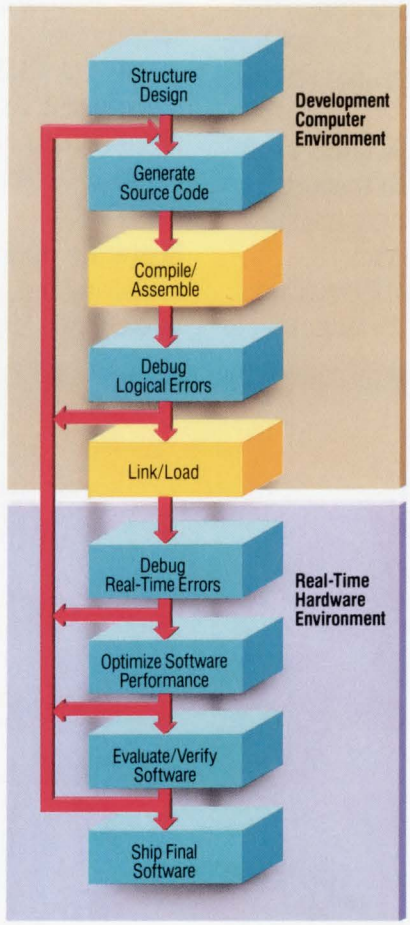
The first issue in embedded software engineering is productivity. Productivity's primary concern is the growing complexity of writing larger and larger embedded programs. 200,000 to 400,000 lines of source code, once beyond imagination, are now commonly found in a single product. And there is no end in sight to this explosive trend. As a result, engineering labor requirements are massive. Writing a 400,000-line program might typically take more than 150 man-years. Without new, automated tools, software engineering productivity will ultimately collapse of its own weight.

The second issue, performance, reflects the growing demand for real-time responsiveness in embedded systems. Here software encounters innumerable "real world" situations which require near-instantaneous reactions. But as embedded software grows in size and becomes more complex, it also tends to run slower. More features require more code. More code means reduced real-time responsiveness. In an unforgiving jet aircraft travelling at Mach 2, this may prove calamitous.

Reliability, the third issue, reflects the growing recognition that embedded software must meet the

same fail-safe level of execution historically expected from hardware. More and more, this operation level must be guaranteed to meet military specifications, FAA standards or other proofs of reliability. But the demand for reliability isn't limited to the military or government. Reliability is equally important in something as common as a late-model car. In just one example, a firmware error could shut off headlamps as you speed down a deserted road at night. This kind of potential threat can become dangerously real. Thus, engineers are commonly faced with the troubling task of assuring that there are zero bugs in a given piece of code, regardless of the code's complexity. Yet, by its very nature, software is difficult to verify in terms of reliability. Complex programs may follow immeasurable numbers of execution paths, depending on external input.

The final issue, maintainability, acknowledges the need for a method of tracking, up-dating and improving software, regardless of its complexity. The time will undoubtedly come to modify those hundreds of thousands of lines of source code written by engineers who have long since moved on to other assignments. Will someone new to the project be able to understand and work with the code as originally written? If the answer isn't "yes," up-dating and improving software will be excessively costly, time consuming, and prone to error.



In a limited response to these four key factors in the embedded software crisis, many individual tools address isolated issues. But that isn't enough when software development is becoming more complex and the risks are growing even greater. What's needed today is an all-encompassing, global Computer Aided Software Engineering (CASE) tool set which efficiently integrates and automates all phases of microprocessor development.

Meeting the crisis head on.

Today only one company, MicroCASE, has assembled a comprehensive, integrated tool set which fully satisfies computer aided software engineering needs in microprocessor development. Building on the proven nucleus of Northwest Instrument Systems, MicroCASE offers individual tools and global systems which meet these needs on a fully integrated basis.

The MicroCASE system is the first to span the entire embedded software development process. It includes tools for software design, coding, real-time debug, integration, performance analysis and verification. These instruments reside within an open architecture which lets the user extend tools already running on mainframes, workstations and personal computers.

Multidimensional solutions are the key.

Untangling the crisis in software has to begin at a practical entry point. For this reason, MicroCASE employs established software development tools for its base. These traditional tools are then complimented and expanded with an overlay of proprietary tools. The proprietary tools can be added to your existing system, piece by piece. Or you can choose a fully integrated system for the entire microprocessor development cycle, as shown on this page. By spanning this entire development cycle, MicroCASE helps you meet all four key microprocessor software development issues.

Responding to the issue of productivity, MicroCASE is working with CADRE, the leader in real-time structured analysis and structured design (SA/SD) tools. As a result, CADRE tools will soon be exclusively integrated into the comprehensive MicroCASE system. Historically, prior failures to integrate SA/SD tools with code generators, compilers, debuggers and non-statistical analysis tools inhibited the use of computer aided software engineering (CASE) systems in microprocessor development. With CADRE, MicroCASE is committed to evolving a practical tool set that integrates front end design tools with back end implementation tools.

In source code development, MicroCASE supplies Pascal and C language cross-compilers and assemblers for a wide range of popular microprocessors.

These are hosted on VAX™ IBM® PC, Sun™ and Apollo™ computers. MicroCASE tools are also tightly coupled with leading Ada cross compilers.

MicroCASE offers XRAY™ to begin source code debug before the program leaves the host development environment. This debugger simulates the execution of the compiled code so engineers can isolate and correct basic structural flaws in the program.

But debugging in the host development environment isn't enough. New problems often arise when code is integrated into target hardware. This is where the specific problems of real-time embedded software development begin to surface.

To solve these problems, MicroCASE offers a comprehensive series of linked tools which support every aspect of integration, debug, performance optimization and verification for real-time systems.

This tool set features a wide range of emulators. They provide object code download, execution control and real-time source and assembly level trace for 8-bit, 16-bit and 32-bit microprocessors.

Finally, the MicroCASE Software Analysis Workstation™ (SAW™) provides a unique, high-level system for code trace, performance analysis, and code coverage test. The SAW allows engineers to specify and trace real-time events including procedures, functions, modules, code ranges and global variables defined in the original high-level source code.

The SAW non-intrusively traces code in the real-time environment. This takes place at the procedure level without missing a single specified event. Code can also be traced for specified segments (i.e., local trace) at the instruction level. And two processors can be traced and time aligned concurrently for sophisticated multiprocessor applications.

Using advanced, non-statistical techniques, the SAW easily isolates performance bottlenecks. Proper validation of test suites is insured with real-time code coverage.

The entire MicroCASE tool set uses the same high-level source code constructs during each phase of development. The original source code serves as a basic reference all the way from programming to software test.

All MicroCASE tools are host and microprocessor independent. As a result, software development environments can be continuously modified to reflect advances in workstation and microprocessor technology.

Real-time operation is a must.

Solving the software crisis could never take place without two features pioneered by MicroCASE. First, all MicroCASE debug, integration, optimization and verification tools operate in real-time. This allows them to faithfully reconstruct events in the target system.

Second, the fact that these tools are non-intrusive means that they have no impact on the operation of a target system. Thus they assure undistorted performance. And data that is always accurate.

An important step you can take right now.

Solving the crisis in software development is going to take new knowledge about new tools. You can start now by exploring the global tool set with your local MicroCASE field application engineers. It's as easy as calling 1-800-547-4445 toll free.

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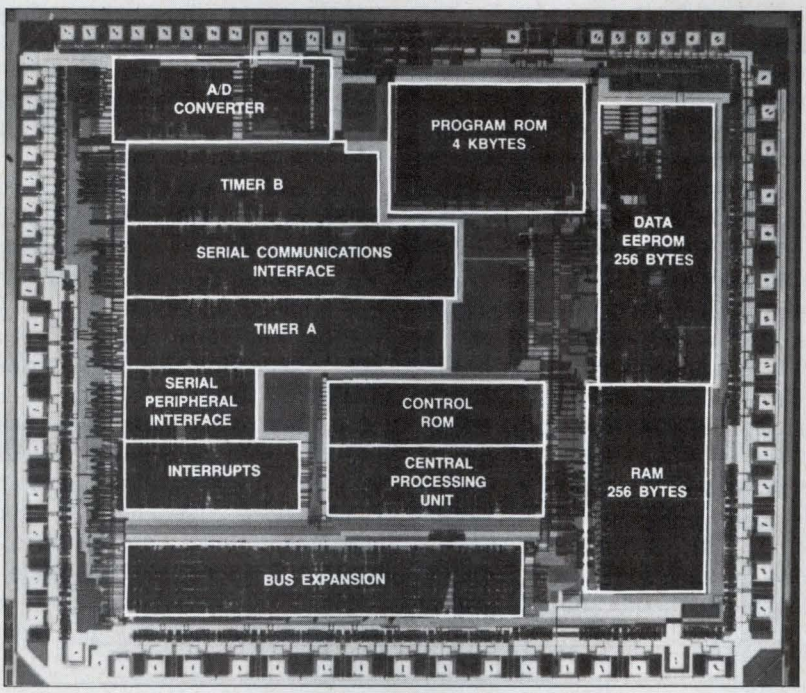


The TMS370C050 microcontroller, like the rest of the new TMS370 family of microcontrollers from Texas Instruments, was designed as a system-on-a-chip solution. The on-chip memory and peripheral modules attach to a silicon bus, providing the flexibility of an application-specific IC in an off-the-shelf product.

8-bit Microprocessors...

(continued from page 50)

ductor (Santa Clara, CA). "But we found that even in 8-bit systems our customers wanted to have the ability to interconnect microcontrollers, displays, specialized memory devices like EEPROM, and external A-D converters with a bus that could run long distances without additional components. So we've stayed with the Microwire bus concept, and it's widely used."

Most vendors have their own serial bus schemes now, including National's Microwire, Intel's Bitbus, and Motorola's Serial Peripheral Interface. These interfaces use a simple synchronous protocol to establish communications between microcontrollers and their peripherals. While slower than an external 8-bit parallel bus, the serial bus provides adequate speed for virtually all I/O transactions, reduces the total number of interconnect lines to two or three, and can be run over reasonable distances. These attributes have made serial buses important to the aircraft and automotive industries, where wiring harnesses for low-speed signals are heavy, labor-intensive enemies of the system designer.

One class of external components often connected to a serial bus is itself being absorbed into the microcomputer. Analog devices, whether comparators or full A-D converters, are showing up on-chip, and they're sporting increased speed and resolution. Integrating the analog parts has required careful blending of vendors' digital and analog CMOS processes, as well as close attention to the needs of particular customers.

Zilog (Campbell, CA), for example, focused on a combination of very low cost, small physical profile and high computing performance for the newest member of its Z-8 family. This focus, dictated by the needs of customers who must execute fairly complex algorithms on a budget, led to the inclusion of a pair of analog comparators along with 14 I/O pins, 2 kbytes of ROM and two counter/timers within the dynamic RAM-style 18-pin package.

"So far, we're seeing reasonably complex applications," says Brady Williams, Zilog's Z-8 product line director. "Customers are employing the inherent speed of the Z-8 architecture with the comparators and a minimum number of external components to solve some interesting control problems."

In spite of the flexibility of comparator-based parts, some applications demand full A-D converters, so these devices are moving on-chip too. In most cases, the on-chip converters will have 8-bit resolution.

"We were driven to move A-D conversion on-chip by specific customer needs," says Mike Polen, 8-bit microcontroller marketing manager at Texas Instruments (Houston, TX). "We codeveloped the TMS370 microcomputer family with Delco Electronics, which can be extremely sensitive to parts count. One more chip in the radio can make the radio case larger. That can force a car's instrument panel to be larger, which in turn can increase the width of the car, making the body heavier. A heavier body requires a larger, less efficient engine to meet performance goals. Thus, eliminating a separate package for the A-D converter can be a big deal for Delco."

TI and Delco (Goleta, CA) chose to make an 8-bit A-D converter one of the many I/O modules that can be configured onto a TMS370 chip. While 8-bit A-D converters are the most common on microcontrollers at the moment, a whole range of analog-input devices is available, from comparators through full 10-bit converters. But as vendors drive for more precision and speed, they begin to encounter complications.

"The majority of controller applications can be handled by 8-bit converters," says P.K. Dubey, product marketing manager for microprocessors at NEC Electronics (Mountain View, CA). "But lately, some vendors have moved on to 10-bit. A 10-bit A-D is feasible with the technology we have now, but the difference in die size between microcon-

trollers with 8-bit and 10-bit converters is phenomenal."

National's Sessions sees other limitations to on-chip A-D converters at the moment. "With some processes, there can be interference between the analog and digital circuits at resolutions over 8 bits. Sometimes you have to shut down the microcontroller during a conversion to get accurate results. The on-chip parts are useful within their limitations, of course, but we're a ways away from being able to handle engine control or digital audio applications with integrated A-D converters."

Building in speed

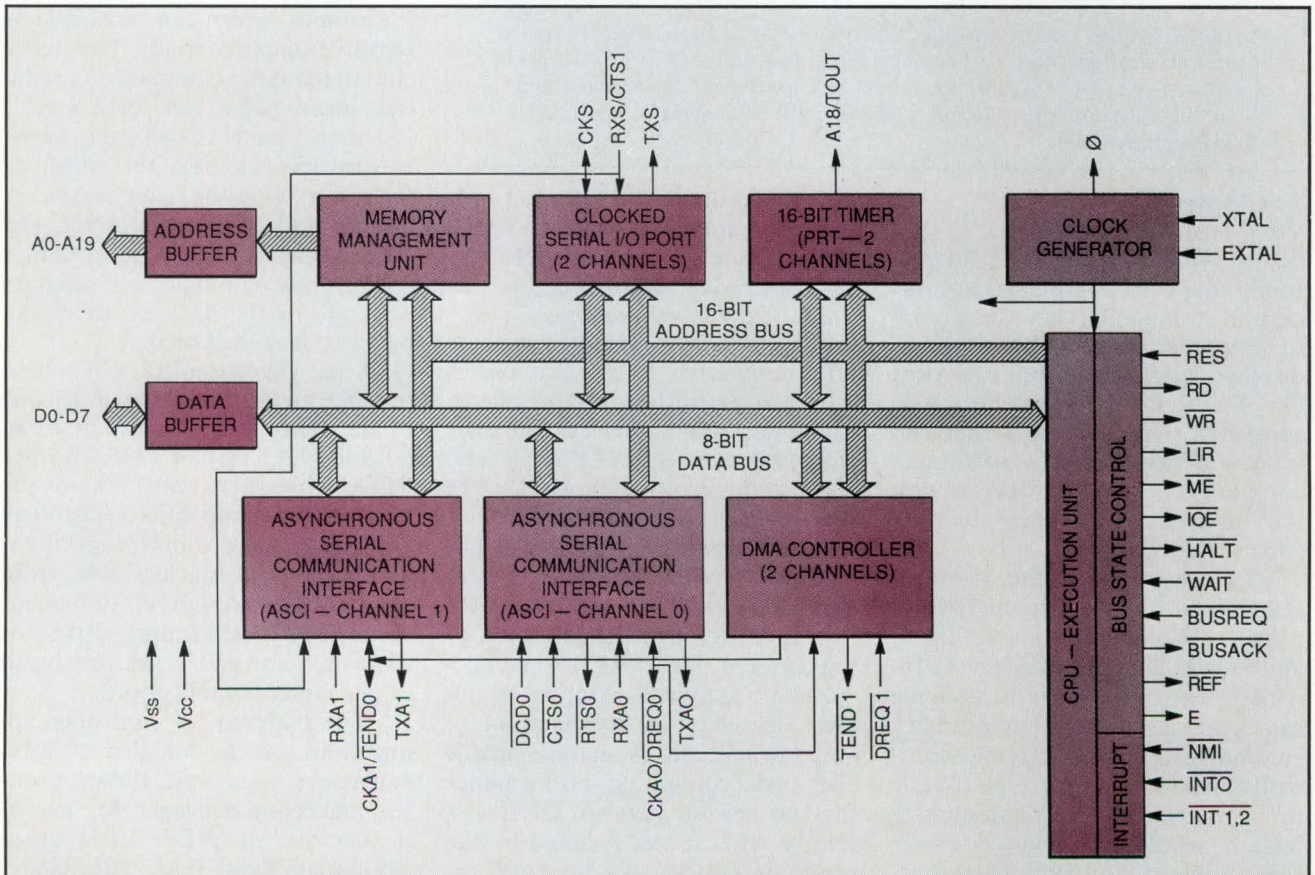
A focus on speed is characteristic of an entire category of new 8-bit parts. Like their analog-laden relatives, these chips have added I/O devices. Here, however, the motive is higher throughput rather than lower chip count. And the devices added to the microcontroller can be as simple as a data pointer or as complex as a DMA controller.

Advanced Micro Devices (Sunnyvale, CA) has added speed-enhancing peripherals to its 8051-based family of microcontrollers. AMD's current flagship, the 80C521, offers both expanded on-chip memory and dual data pointers. The dual pointers, used during data movement sequences, address a particular bottleneck in the original 8051 architecture, according to AMD. Using one pointer to hold a source address and the other pointer to hold a destination address, block moves in external memory can be accomplished at twice the speed of a conventional 8051, and with only about 65 percent of the code.

When systems call for large external memory and correspondingly large block-move operations, the vendor may choose to devote even more hardware to the problem. Hence, some 8-bit devices now have DMA hardware on-chip.

One example is the Hitachi HD-64180 family. The base part in the family is actually a microprocessor, not a microcontroller, in the sense that it has no on-chip memory. "We saw the Z-80 moving to a new market," says Bob Sandler, product marketing manager. "Once it had been used primarily in CPM-based PCs. But with the advent of the IBM PC, the Z-80 was used primarily in embedded controllers. So we decided to start with the Z-80 and tailor a part for embedded computing."

Hitachi's tailoring started with the execution unit and bus interface of



Hitachi started with a Z-80 and built around it an 8-bit microprocessor for big, speed-conscious applications. The 64180 processor chip includes a 1-Mbyte memory manager, a two-channel direct memory access controller and a selection of frequently used peripherals.

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The Z80 Family: Still growing strong.

The Z80 remains the most commonly used 8-bit microprocessor in the industry. No wonder. As the family has continued to develop, so have the advantages: the familiarity of working with devices you know and trust, the tremendous value of being able to use software you've already developed, and, of course, there's the impressive Z80 performance.

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- **Z80180** *the Z180 8-bit MPU combines a Z80 CPU, MMU, 2 UARTS, DMA, a C/T and more, with no extra logic needed for Z80 peripherals*
- **Z84C01** *combines a Z80 CPU with an on-board oscillator*

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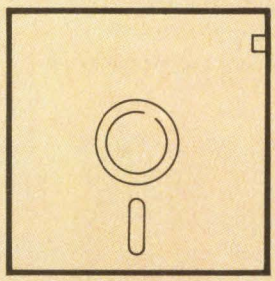

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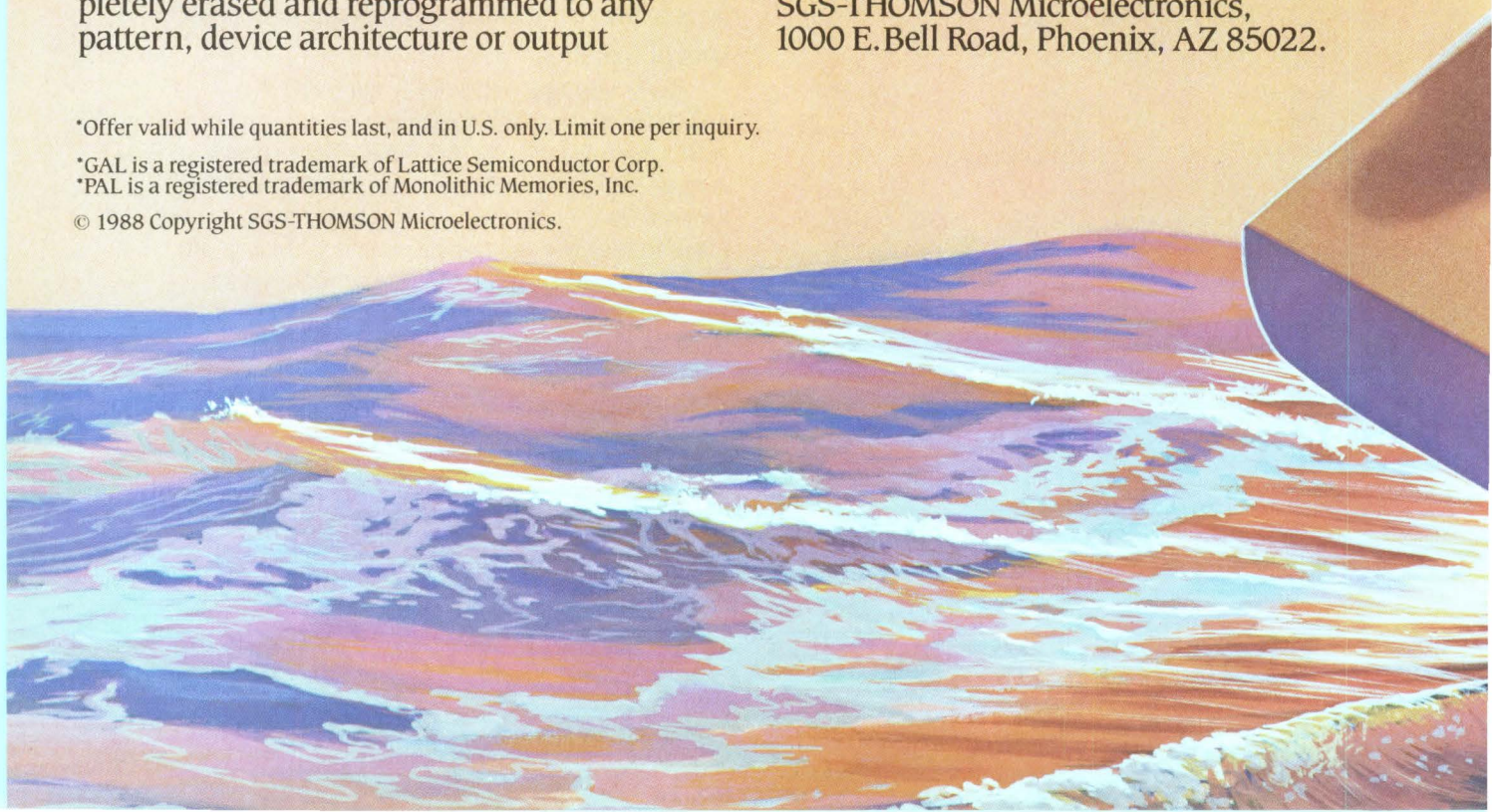

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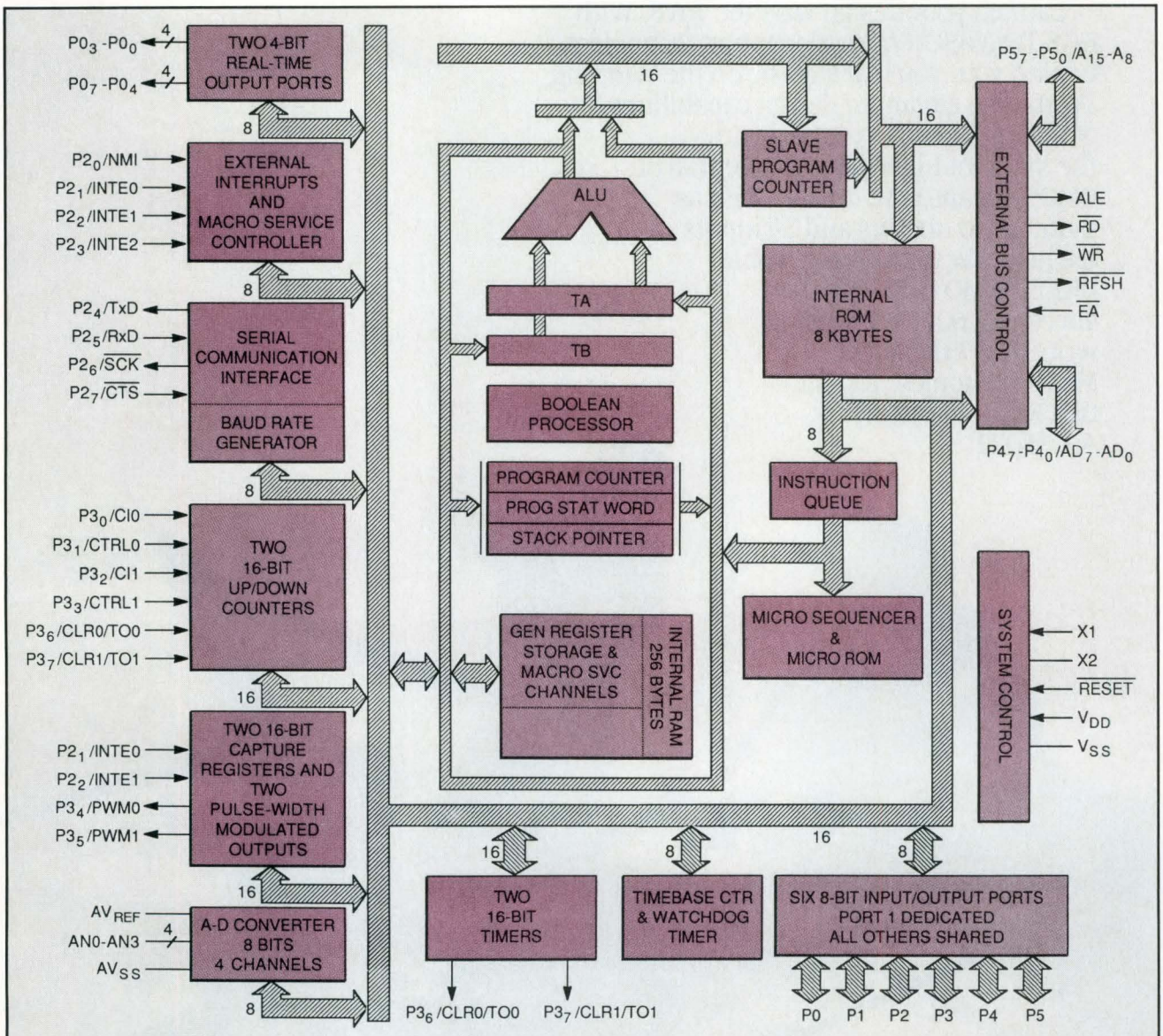

NEC's μPD78310 is a highly integrated 8-bit microcontroller aimed at 16-bit applications. The array of on-chip peripherals rivals that of any compact 8-bit microcontroller, but the 16-bit execution unit benchmarks well against full 16-bit processors.

the Z-80. Then the design team added a number of commonly used peripherals, including an interrupt controller, three serial interfaces and a two-channel timer. The bus controller was altered to support either Motorola- or Intel-style peripherals.

But Hitachi felt the Z-80 could reach more embedded applications if it could accommodate larger, more speed-critical programs. So the team included an 8×8 multiply instruction that required only 17 clocks. It then gave the 64180 an on-chip memory management unit (MMU) that expanded the address range from the Z-80's 64 kbytes to 1 Mbyte. And it added a two-channel DMA controller, capable of moving data across 64-kbyte boundaries at high speed without CPU intervention.

The new microprocessors

Hitachi's 64180 processor chip is an example of an 8-bit CPU with hardware extensions to enhance speed. It's also representative of a new generation—in a way, a new concept—of 8-bit microprocessors. These new chips are like traditional microcontrollers in that they have on-chip peripherals and, sometimes, on-chip memory. But they're philosophically quite different from traditional microcontrollers in that they're intended for use with external memory, running extremely large and demanding programs written in a high-level language.

Hitachi's fullest expression of this concept comes in the HD64180 ZTAT (for zero turnaround time). The part includes the same Z-80 core, system expansions and on-chip peripherals as the other 64180 products, but adds 512 bytes of RAM and 16 kbytes of EPROM—enough to make compiler use practical in a one-chip system. "We're offering a new path for traditional 8-bit microprocessor users," comments Hitachi's Sandler. "They can sharply reduce their parts count but get the kind of clock rate and addressing range normally associated with 16-bit CPUs. You don't have to throw away your 8-bit code just because it has outgrown 64 kbytes."

In its efforts to break into 16-bit performance territory, Zilog has gone a step beyond the 64180 with its Z-280 microprocessor. The Z-280 straddles the 8- and 16-bit barrier in both architecture and performance. On one hand, the chip is upward-compatible with the Z-80 instruction set and provides an 8-bit, Z-80-style bus interface. On the other hand, the Z-280 has features that are unheard-of in 8-bit machines: a 16-bit external bus, an on-chip MMU with a 16-Mbyte address range, 256-byte instruction and data caches, and a 20-MHz clock.

One vendor of in-circuit emulation and compilers, Softaid (Columbia, MD), believes the Z-280 is a significant step in the 8-bit evolution. "Right now, there are a lot of 32-bit machines doing jobs an 8-bit chip could handle," claims Jack Ganssle, Softaid president. "The 32-bit architecture lets the designers be sloppy and still get the program to fit. But a chip like the Z-280, with its new, more orthogonal instruction set and an incredibly good MMU, could turn that picture around for some people."

Even chips clearly identified as single-chip controllers are taking aim at 16-bit performance. That's certainly the case with Motorola's flagship, the 68HC11F1. The part, a member of the 68HC11 family, is configured with 1 kbyte of internal RAM, no internal ROM and a non-multiplexed bus. "With the faster bus and the large number of 16-bit instructions in the 68HC11 set, the F1 benchmarks in the same range as many 16-bit microcontrollers," asserts Motorola's Marsh. "Using National's benchmark numbers, we're faster than the 8096 and near the speed of National's 16-bit HPC."

Another vendor that's drawing a bead on 16-bit controllers is NEC Electronics. Its 78310/78312 microcontrollers integrate the usual 8-bit bus and full set of peripherals—including four-channel, 8-bit A-D and large memory (256 bytes of RAM and 8 kbytes of ROM, in this case)—with a full 16-bit execution unit. The 16-bit registers and data paths give the 78310 benchmarks that are clearly in the range of 16-bit machines, as well as some unusual features such as a 3.2-ms 16×16 multiply and an 8.4-ms 32×16 divide. With C compiler support and an external address range of 64 kbytes, NEC's chip is all ready to take on some rather formidable processing tasks.

The ASIC alternative

The newest 8-bit microprocessors have the speed and address range to challenge 16-bit CPUs for many jobs. And they can boast compiler and in-circuit emulator support to back up their speed. When the system requirement is compactness instead of speed, the latest single-chip microcontrollers and their supporting chips have unprecedented levels of integration, often making possible one- or two-chip systems with successive-approximation A-D conversion and pulse-width-modulated D-A conversion. In addition, prices of all the parts in quantity can be extremely low: simple chips under $1 and highly integrated parts for a few dollars aren't uncommon.

With all these strengths, it might seem that the future in embedded systems belongs to the 8-bit standard products. But there's another issue: semicustom ICs. For the most part, 8-bit CPU vendors have been liberal with their design licensing policies, the result being that most aggressive standard-cell libraries contain at least one 8-bit CPU core cell. While they may not be widely used yet, these CPU cores may be the most important alternative to off-the-shelf 8-bit processors in moderate- or high-volume applications.

The advantages of a standard-cell approach are obvious. The designer can pick a CPU core and configure around it precisely the system-on-a-chip required for the specific application. The chip gets just the right amount of memory, just the right number of I/O pins, just the right width counters and so forth.

The value of providing this flexibility to customers isn't lost on the companies providing both standard parts and ASIC services. "When 1- and 1.2-micron processes get into full-scale production, the idea of a system-on-a-chip becomes really important," explains NEC's Dubey. "At that point, the ASIC alternative becomes absolutely necessary for some high-volume customers, such as the auto industry. NEC doesn't intend to fight against the trend; we offer our 78000 CPU as a core."

For vendors without ASIC businesses, the picture may be less clear. For now at least, the enormous volumes of some off-the-shelf parts may keep them ahead of ASIC alternatives. "The ASIC cores do provide a more highly integrated solution, but when the Z-80 is around a dollar at high volumes, the ASIC just can't be cost-competitive," says SGS-Thomson's Little.

And so the evolution of the 8-bit CPU continues. At each step along the way, this 20-year evolution has created a set of cost-effective alternatives for a particular set of design problems. Some customers still use the earliest microprocessors and microcontrollers. Others go for more recent parts that carry sophisticated I/O devices on-chip. Still other designers are learning that the latest 8-bit high-end products can beat out 16-bit alternatives on many tasks. Clearly, 8-bit CPUs make up not a page of industry history, but a continuing, evolving portfolio of design alternatives for today's systems. **CD**

(Forward Thinking, Re

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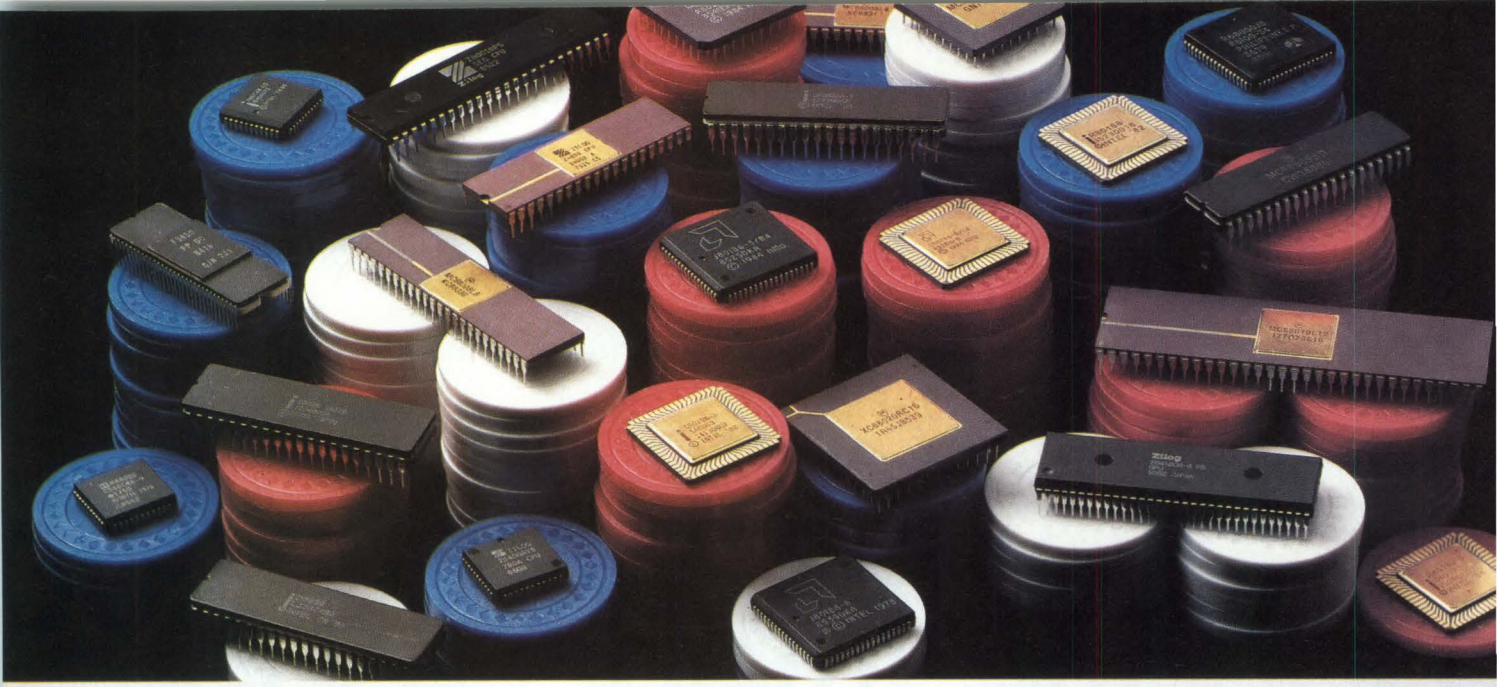

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Logic-synthesis tools forge link between behavior and structure

A new generation of electronic design automation tools can automatically generate structural descriptions from high-level inputs.

Richard Goering
Senior Editor

Today's electronic design automation (EDA) tools provide little help for one of the toughest parts of the design cycle—converting a high-level design specification into a low-level logic network. Logic-synthesis tools can now automate that process by mapping logic descriptions from one level of abstraction to a lower level. Some tools can also optimize designs for area or timing, thus generating better designs as well as boosting productivity.

Because so many engineer-hours are spent manually generating low-level schematics, logic-synthesis tools could increase engineer productivity more than any other EDA tool that's appeared so far. With the tools' potential for such great utility, the logic-synthesis market will grow from around $5 million in 1987 to over $200 million in 1990, according to the Technology Research Group (Boston, MA). "Logic synthesis will be especially important for the computer market because the need to optimize timing is so strong," says Jean-Noel LeBrun, system design marketing manager for Daisy Systems (Mountain View, CA).

Logic-synthesis tools that convert Boolean equations into programmable logic device (PLD) fusemaps have been around for some time. What's new is the extension of logic synthesis to a much broader range of designs. Two new companies, Silc Technologies (Burlington, MA) and Synopsys (Mountain View, CA), recently introduced toolsets that can map optimized logic into commercial application-specific IC libraries. Toolsets from these companies support high-level language inputs and can optimize both sequential and combinational logic.

Logic synthesis is also showing up in silicon-compilation tools, and it may restore the original promise of silicon compilation—the ability to generate IC layouts from behavioral descriptions. Today's silicon compilers are actually module generators that con-

vert structural design descriptions into full-custom layouts. Logic synthesis, on the other hand, generates no layout but converts high-level design descriptions to structural design descriptions. While silicon compilation is best suited for regular structures like RAMs and programmable logic arrays (PLAs), logic synthesis can handle a broad range of random logic.

Like silicon compilers, today's logic-synthesis tools are aimed at chip design, and they still require some knowledge of the structural implementation of the chip. "Logic-synthesis tools today can deal effectively with only relatively small blocks of random logic," says Jim Solomon, chairman of SDA Systems (San Jose, CA). As such, synthesis tools are aimed at designers who have some ASIC design expertise. Within a few years, however, board-level synthesis tools that can map high-level descriptions into standard parts will probably emerge.

The first commercial logic-synthesis tools, such as Palasm from Monolithic Memories (Santa Clara, CA), simply generated PLD fusemaps from Boolean equations without attempting to reduce that logic. Algorithms for minimizing Boolean equations into a reduced form became part of the synthesis process in the early 1980s. The Presto and Espresso-II algorithms from the University of California at Berkeley, for example, are widely used to reduce two-level, combinational logic for PLDs or PLAs. These algorithms accept sum-of-products Boolean equations and output another set of equations with a reduced set of product terms.

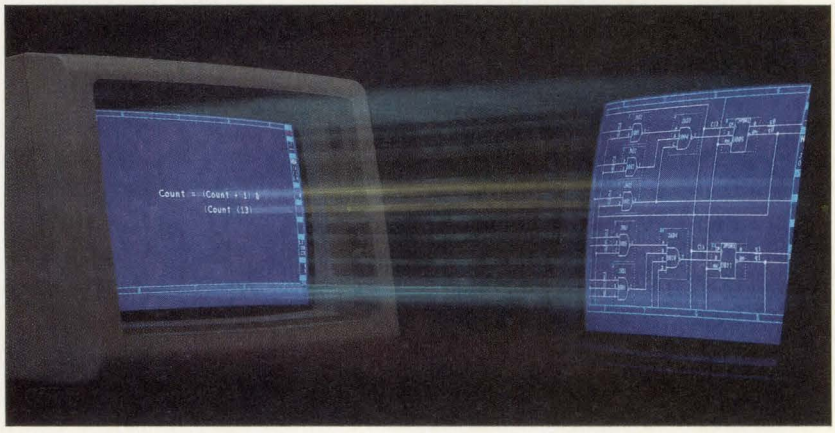
The Abel PLD compiler from Data I/O (Redmond, WA) feeds the output of Presto into a fusemap generator that can build a JEDEC standard file for a PLD programmer. Abel also adds a front-end to Presto that can accept logic equations, truth tables or a state-machine description language as input. The state-machine language, which supports case statements and if-then-else constructs, provides a way of inputting sequential logic, but this logic isn't minimized.

The logic equations in Abel allow for arithmetic and relational operators in addition to Boolean expressions. While this lets designers describe logic at a higher level, the system can't fill in structural information that's missing. "If you describe an adder by writing 'A = B + C,' you've defined nothing structurally," says Michael McClure, product manager at Data I/O's Futurenet subsidiary. "You'll get a brute-force adder. You won't end up with a ripple adder or a carry look-ahead adder unless you write the equations to define one."

Future Designer, an IBM PC-based logic-synthesis tool from Data I/O Futurenet, uses the Espresso algorithm. It can generate net lists and schematics for gate arrays as well as PLD fusemaps. Because gate arrays use more than two stages of logic, Future Designer provides a factoring technique called weak division that can decompose two-level logic into multilevel logic. Factoring sorts out the common product terms used in equations, and it can be invoked after Espresso completes the two-level logic minimization.

Future Designer not only provides all the input methodologies supported by Abel, but also supports schematic entry through Futurenet's Dash product. "All of the input methods are useful," says Larry Siebert, a member of the technical staff at Opus Systems (Cupertino, CA) and a Future Designer user. "State-machine language is helpful any time you're using a state machine. Before, we had to go in by hand and do Karnaugh mapping to create the next-state equations."

Although Future Designer supports a number of gate array libraries, it doesn't take timing into account, so it can synthesize macrocells at a func-



Logic synthesis maps high-level design descriptions into low-level schematics. Futurenet's Future Designer can synthesize programmable logic device fusemaps and gate array net lists from logic equations, state-machine descriptions, truth tables or schematic entry.

Aart J. de Geus
Vice-President of Research and Development
Synopsys

Circuit quality drives adoption of logic synthesis

Before adopting logic synthesis, designers and CAD managers should ask three key questions: Are synthesized circuits competitive in speed? Are they competitive in area? Does synthesis fit with my present way of doing things? The adoption of logic synthesis hinges on how well these questions are answered.

Synthesizing circuits to suit a designer's timing constraints is the most important and the most difficult requirement to meet. Since timing-critical modules often cause major unexpected and unpredictable schedule slips, the ability to automatically generate logic under user-specified timing constraints is extremely important. For a synthesis system to do this, it needs to master the same tricks a designer uses, such as signal phase selection, buffering, pin selection, load splitting and gate sizing. The capability to perform these tricks automatically while simultaneously verifying that a circuit meets specifications with built-in timing verification gives a state-of-the-art synthesis system the power to create competitive circuits.

In terms of area, the size of a circuit has a direct impact on its cost effectiveness. Decreasing the gate count by a few percentage points can save thousands of dollars in product costs. While designers often use only the subset of gates with which they're familiar, a synthesis program uses all the gates available in a chosen library. The resulting implementations are, therefore, often 10 to 30 percent more efficient than hand design.

After the exaggerated promises of silicon compilation, designers are rightly suspicious of radical new design approaches. Changes to the proven design methodology add an unacceptable risk to schedules that are already tight. Compatibility with existing design descriptions, CAE systems and application-specific IC libraries, therefore, is a must for synthesis. Because about 80 percent of all design work involves the redesign of existing circuitry, optimizing to satisfy the many implicit setup and hold constraints that are typical for large sequential networks is also essential to integrating logic synthesis into mainstream production design environments.

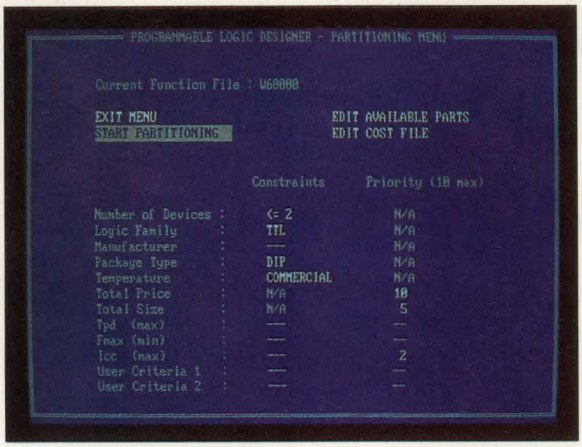
State-of-the-art logic-synthesis systems now satisfy all three of the requirements discussed above. Many computer designers are already active users of automatic synthesis, and many ASIC design groups are beginning to introduce logic synthesis into their design methodologies. Similar to CAD tools moving designers from polygons to transistors in the 1970s and CAE tools rising from the transistor level to the gate level in the early 1980s, logic synthesis brings about the next major step upward in design productivity.

tional level only. Moreover, Future Designer does not map logic into existing macrocells when it generates schematics. "The behavioral capabilities of Future Designer are best suited for generating macrofunctions that don't already exist," says McClure. "Otherwise, it's best to just use schematic entry along with the vendor's library."

One advantage of Future Designer is that the engineer can describe logic before selecting the actual device implementation. The input to Future Designer is device-independent, and the system assists with device selection by providing information about the type and number of outputs needed. If the user specifies which outputs are assigned to which devices, Future Designer can partition the design into multiple PLDs.

Two new PLD design systems—one from Hewlett-Packard (Palo Alto, CA) and one from Minc (Colorado Springs, CO)—provide, according to their manufacturers, fully automatic device selection and partitioning, which will be necessary when board-level synthesis tools emerge. HP's PLD Design System takes device-independent input and attempts to find the best fit for the design. The system selects and ranks possible devices that could fit the design. "We try to fit the design into one device, but we can also partition it into multiple PLDs," says HP marketing engineer Dan Schmauch.

In addition to providing automatic device selection and partitioning, the PLDesigner from Minc has a capability not offered by HP's PLD Design System: it lets designers specify such constraints as preferred manufacturers, package type, cost, propagation delay and maximum number of devices. Designers then have the capability to give these constraints relative priorities, and the system discovers the 10 best solutions and displays them in order. Unlike Future Designer, both the HP and the Minc PLD design systems let the user enter designs by drawing waveforms.



The PLDesigner from Minc provides automatic partitioning and device selection for programmable logic devices. Partitioning is based on user-determined priorities such as the number of devices, cost and electrical characteristics. The system then selects and ranks possible implementations.

While logic synthesis can generate fusemaps for PLDs, it can also be used effectively to generate logic for PLAs in a silicon-compilation environment. Silicon Compiler Systems (San Jose, CA), for example, has a PLA synthesis package that uses Espresso and lets users enter PLA designs using Boolean equations. And VLSI Technology Inc (San Jose, CA) offers a state-machine compiler that can generate either a PLA layout or a portable net list for its gate arrays and standard cells.

The Finesse program from Seattle Silicon (Bellevue, WA) can synthesize logic and generate layouts for on-chip controllers, state machines or combinational logic blocks. A structured input language offers a choice of truth-table definitions, Boolean equations or state definition statements. Following synthesis and optimization, Finesse can generate layouts in the form of PLAs, folded arrays with internal registers, random logic, decoders and combinations of these elements. Finesse can place and route flip-flops to implement sequential logic.

To synthesize logic, Finesse first compiles the input language into a two-level symbolic representation. It then generates a two-level Boolean representation and uses Espresso to minimize combinational logic. If a block is to be mapped into a PLA, two-level minimization is sufficient; if it's to be mapped into gates, weak division and multilevel minimization are done. A technology mapping algorithm then selects the most appropriate standard cells from the company's Concorde compiler.

Finesse is too new to have meaningful user feedback, but benchmarks run by Seattle Silicon indicate that considerable savings in both area and time are possible. Finesse is aimed at specific types of blocks rather than entire chips. "We've never done a complete chip with Finesse, and I wouldn't expect any of our customers to do so," explains Karen Bartlett, CAD engineer at Seattle Silicon. "It makes more sense to generate your control logic with Finesse and then use the data path primitives in Concorde to design the data path."

The Logic Compiler introduced recently by Silicon Compiler Systems is broader in scope than a state-machine synthesizer or a PLA generator tool. The company claims that it optimizes logic and generates layouts for a variety of circuit blocks, including first-in, first-outs; data paths; state machines; and random logic. It doesn't support behavioral input, but it can work from a net list or a design description in the company's FCX functional modeling language. As such, the Logic Compiler is more of an optimization tool than a logic-synthesis tool.

FCX is a procedural, structural language that serves as a net-list generator. Silicon Compiler Systems can take a high-level structural description from this language and compile it into a detailed, gate-level net list. Then, optimization is handled with rule-based techniques rather than algebraic methods such as Espresso or factoring. Rules for functional optimization provide logic minimiza-

```
addcard:    {
                ADDCARD;
                if (isace & ~ace){
                  ace: = ON;
                  state: =add10;
                }
                else
                  state: =wait;
}
add10:      {
                ADD10;
                state; =wait;
}
wait:       {
                if (cardout)
                  state: =test17;
}
test17:     {
                if (lt17){
                  disp: = HIT;
                  state: = showhit;
                }
                else
                  state: =test22;
}
```

Seattle Silicon's Finesse program can synthesize control logic from state-machine descriptions. These conditional statements form part of the design description for a Blackjack controller.

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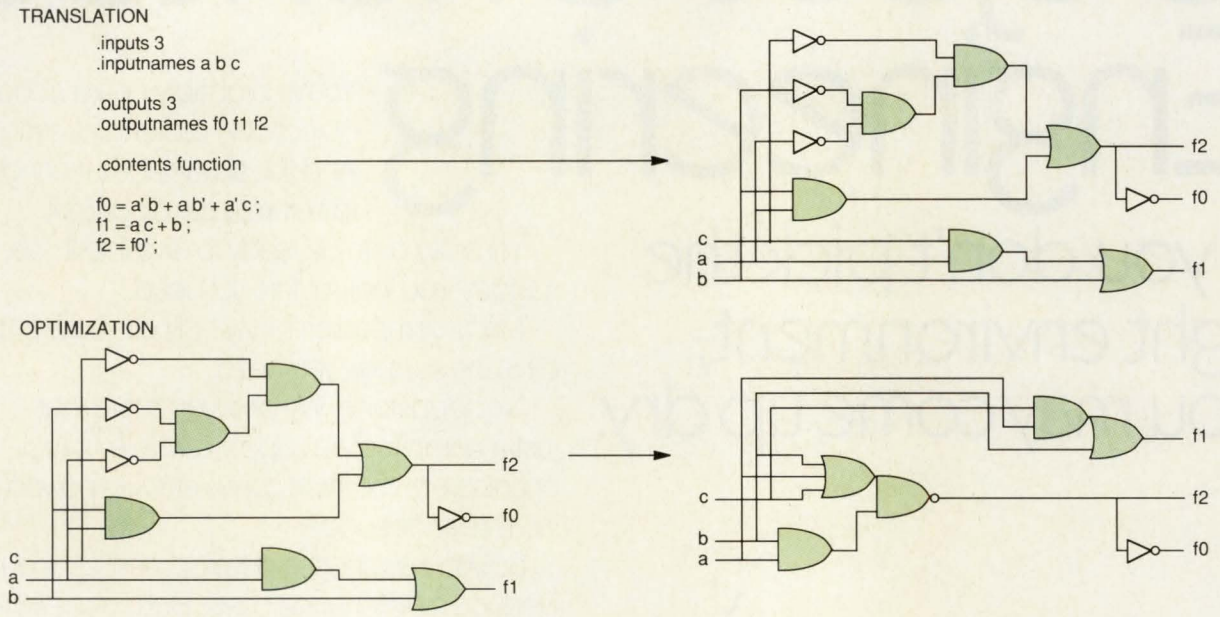

The Logic Compiler from Synopsys includes two steps—translation and optimization. The translation step, which corresponds to what is traditionally called logic synthesis, minimizes equations and converts them to a low-level net list. A rule-based optimization step then improves the design to meet area and timing constraints, ultimately mapping the design into an application-specific IC cell library.

tion, while rules for physical optimization map the minimized logic into the parametized standard-cell library of the company's Genesil silicon compiler.

To guide this rule-based process, users prioritize constraints for speed, area, aspect ratio and pin location. Because the Logic Compiler goes all the way to layout, it can trade off between functional and physical optimization to meet these constraints. "We know that certain kinds of layout structures mesh well together, and we can develop special cells and rules to take advantage of that," explains Misha Burich, engineering vice-president at Silicon Compiler Systems.

VTC (Bloomington, MN) has used the Logic Compiler in support of customer designs, as well as for in-house designs for floating-point applications. "It's a very helpful tool for random blocks of control logic," says principal research engineer Jim Joseph. "But I wouldn't use it to design at the chip level. If you try to run a data path through it, the final result won't necessarily be an improvement."

Silicon Compiler Systems' ultimate goal is behavioral logic synthesis, and the company is examining behavioral languages that could be used for synthesis, including the IEEE-standard VHSIC Hardware Description Language (VHDL). Burich believes that the early behavioral synthesis tools will be aimed at specific architectures, and he says that Silicon Compiler Systems is targeting certain digital signal processing and data path architectures that might be good candidates for synthesis.

Logic synthesis may play a growing role in silicon compilation, but it will have greater appeal to system designers if it can be used with commercial ASIC libraries. The Logic Compiler from Synopsys and the Logic Consultant from Trimeter (Pittsburgh, PA) were the first tools to provide a rule-based mapping into ASIC cell libraries. The Logic Compiler hasn't been marketed as a commercial tool, but it has been used by several large customers, and it's the forerunner of the Design Compiler, just introduced by Synopsys. Trimeter's Logic Consultant, which is marketed as a commercial tool, runs on workstations from Mentor Graphics (Beaverton, OR).

The Logic Compiler is based on the experimental Socrates synthesis system from General Electric (Research Triangle Park, NC). Although the Logic Consultant isn't a direct descendant of Socrates, it's very similar to the Logic Compiler. Like Socrates, both the Logic Consultant and Logic Compiler accept Boolean equations or net lists as input and provide synthesis and minimization for combinational logic. They both have a rule-based

(continued on page 79)

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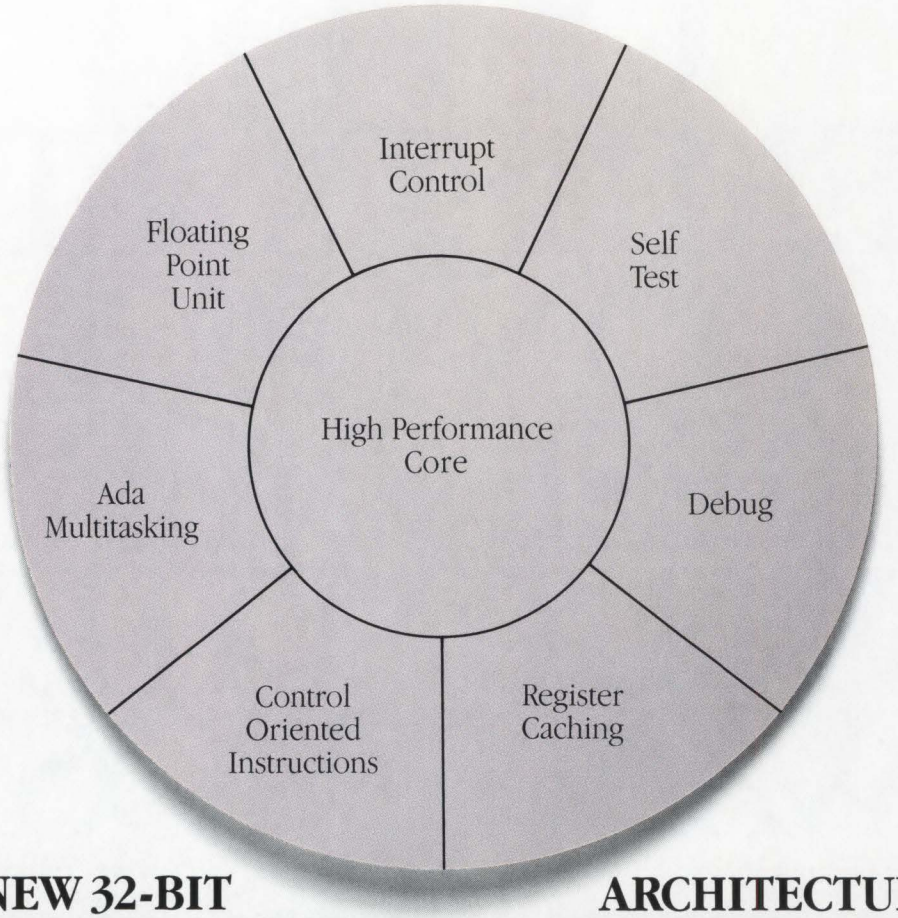

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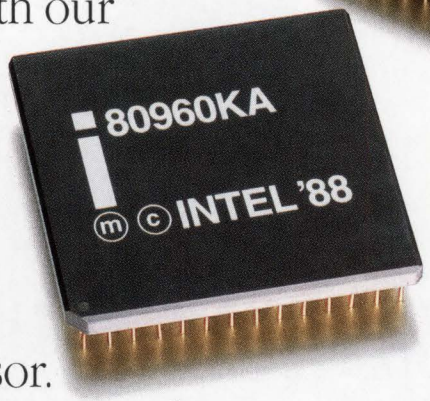

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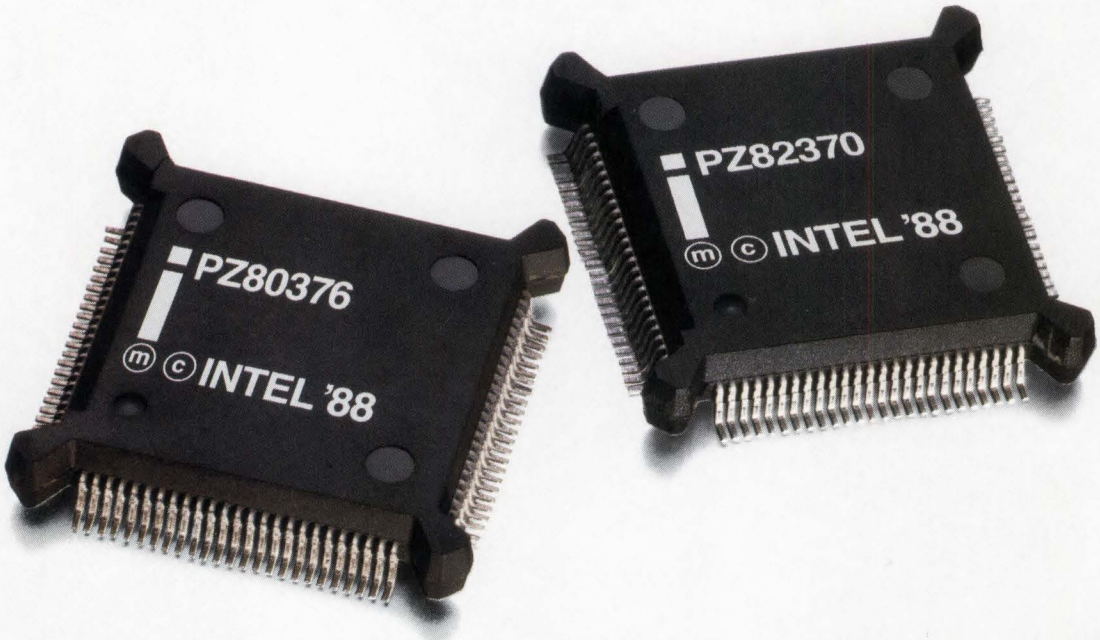

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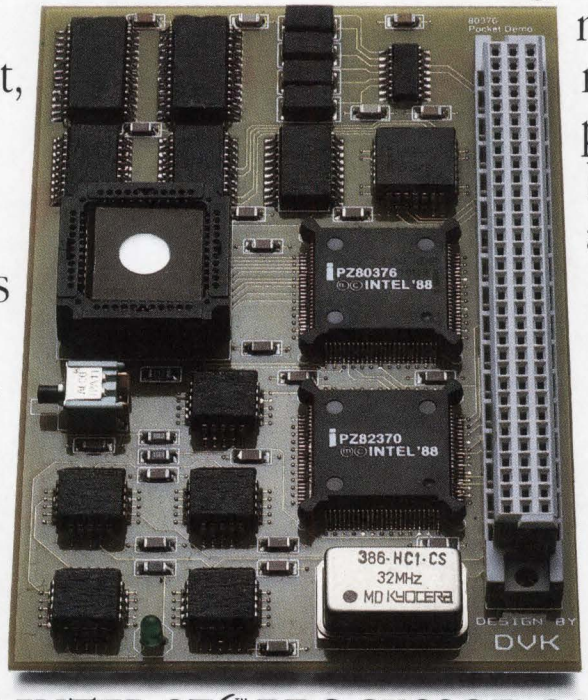

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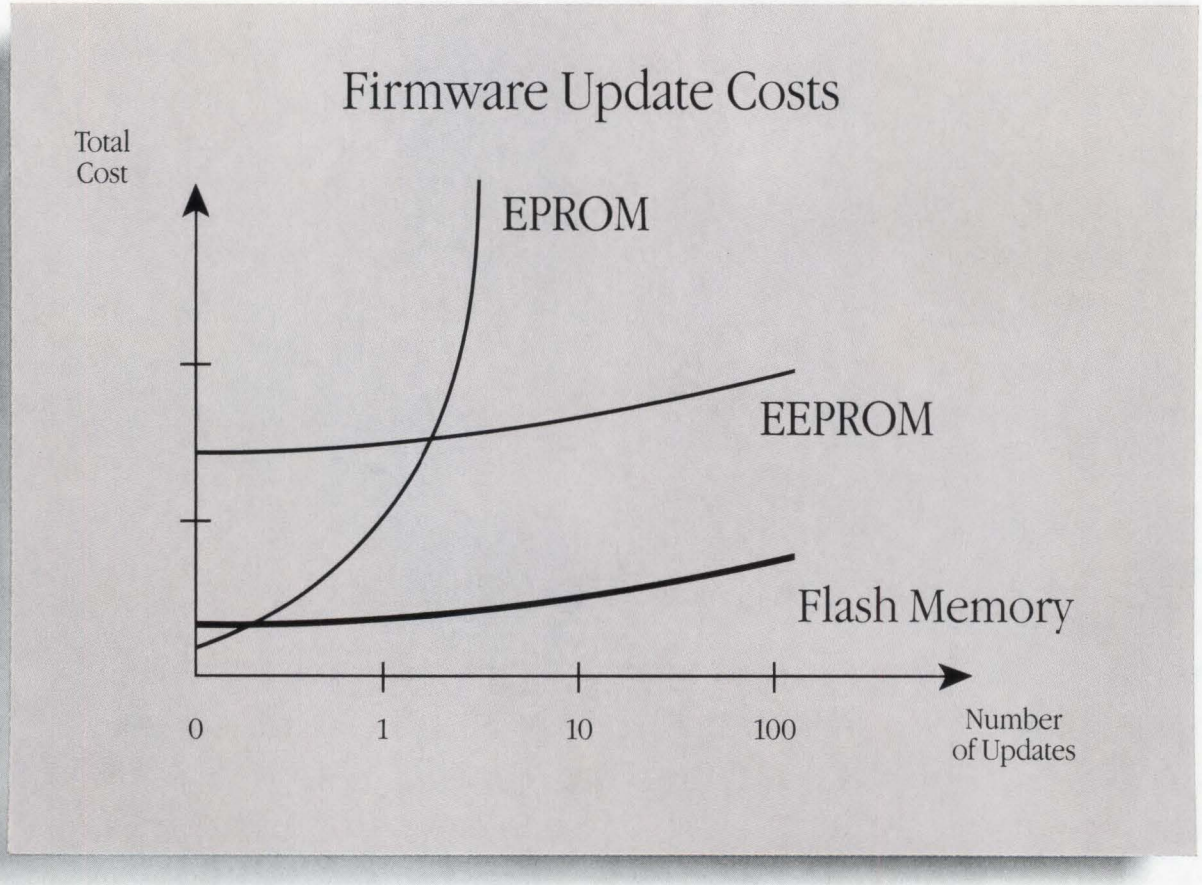

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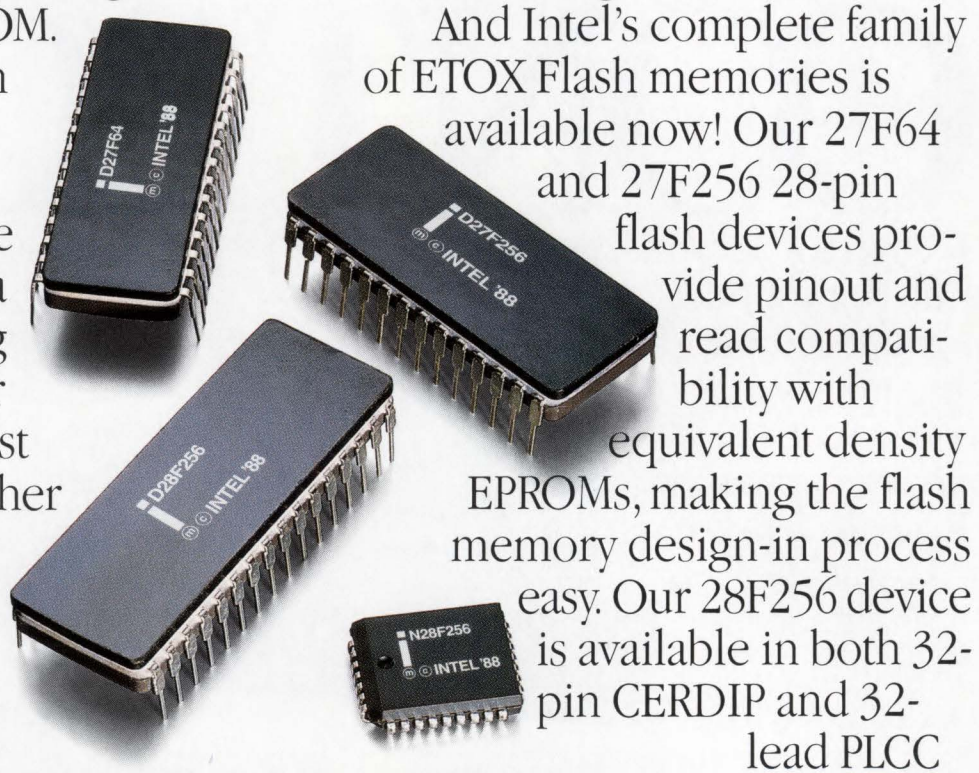

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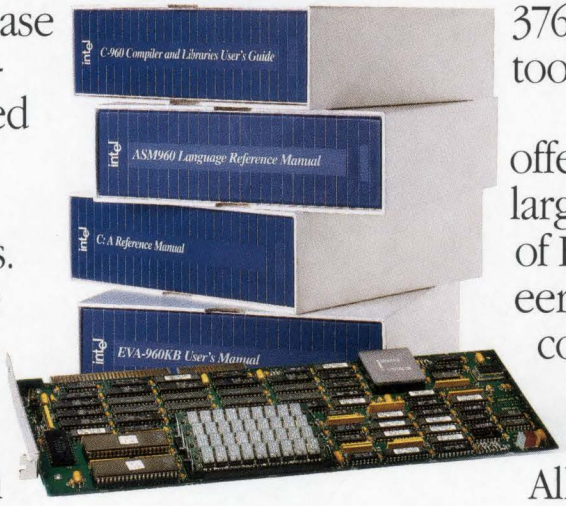

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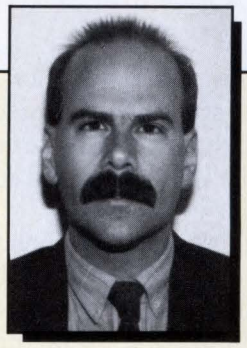


Scott H. Cravens
Consulting Engineer
NCR Microelectronics

Logic synthesis boosts ASIC design productivity

The idea behind logic synthesis is to describe a system's function at a high level, verify its function through conceptual simulation and get a physical implementation in silicon as output. The design-synthesis tools now becoming available are not quite that simple or general, but they can provide significant advantages over traditional design methods (and NCR labels its tools Design Synthesis to reflect that they encompass more than just pure logic-synthesis functions). Input descriptions may be truth tables, Boolean equations, state diagrams or high-level design languages. The outputs may be encoded in programmable logic arrays or devices, net lists of gate arrays or standard-cell elements—or even inputs to compiled functions.

The Design Synthesis system from NCR Microelectronics (Fort Collins, CO) is based on the Silcsyn logic-synthesis product recently announced by Silc Technologies (Burlington, MA). NCR has added knowledge-based features to the original toolset, integrated the tool into its Visys Design System, and now offers it as a highly flexible alternative to conventional design methodology. It will be offered initially as an optional front-end to logic design and schematic capture on a workstation from Mentor Graphics (Beaverton, OR), providing customers with a complete engineering environment on a workstation.

Logic synthesis has already demonstrated the capability of significantly enhancing engineering productivity. A 10-times improvement in design time is realistic, and an experienced user could, in the future, approach a 100-times improvement.

Synthesis may be used for a complete application-specific IC design—or it can be used to create major blocks of a design that's completed using traditional schematic capture. The initial Design Synthesis system won't include analog functions, high-level functions such as core microprocessors, or compiled functions such as memory. These functions will be integrated using schematic capture. The initial system will support the synthesis of blocks to about 2,500 gates; later releases will expand this limit substantially.

Synthesis doesn't impose a particular design style and can be used for a wide variety of applications. The design language provides constructs for both combinatorial and sequential logic. In addition, it allows the description of both synchronous and asynchronous systems, with constraints on asynchronous data to help ensure that timing requirements are met. "What if" iterations may be made to analyze different architectures.

Logic can be optimized for timing constraints through user-defined implementation rules contained in an implementation file. Also, the cell-level implementation is controlled by a part of the synthesis tool called the builder, which is driven by rules developed by NCR to ensure functionality, good design practice and efficient cell utilization.

By using different builders, alternative implementations such as gate arrays and standard cells are possible, in addition to technology migration as new fabrication technologies become available. NCR will also use the system to create macro functions that will be available for customer designs.

Die sizes resulting from design synthesis will be as small as an efficient cell-level design if the designer considers the implementation implied by various language constructs. Die size can also be affected by performance constraints defined in the implementation file. These constraints allow the definition of timing restrictions for the whole design, or for certain critical sections or paths.

Training and experience will help users become comfortable as they gain an understanding of the physical implications of a particular high-level description. NCR sees design synthesis as a significant step forward in ASIC design and believes it will play a major role in future IC design systems.

Special Report...

(continued from page 70)

optimization step that provides cell mapping based on area and timing constraints set by the user.

Because they require Boolean equations or net lists, the Logic Compiler and the Logic Consultant don't synthesize logic from high-level descriptions. Both tools, in fact, have been used most extensively to improve existing net lists. "The Logic Consultant is really a logic optimization tool with just a touch of synthesis," says Gary Holcomb, Trimeter's marketing vice-president. But both the Logic Compiler and the Logic Consultant have built a strong base for high-level synthesis by demonstrating the power of rule-based optimization.

Both systems provide a selection of algorithms for two-level logic minimization, multilevel logic minimization and factoring. The minimized equations are then synthesized into a net list. What's really distinctive about these tools, however, is the

rule-based optimization that occurs after the net list is generated. In this step, selected logic configurations are recognized and mapped into better ones. Two smaller gates might be replaced by a larger gate, for example, or two inverters could be rearranged to eliminate one of them.

Rules are invoked according to the area and timing constraints set by the designer. Cell mapping takes place during optimization, but part of the optimization can occur before an ASIC library is chosen. To improve timing, for example, the optimization phase might add more inputs to a critical path. Cell mapping requires an extensive knowledge base for each ASIC library, so only a small number of libraries are available. Trimeter's Logic Consultant, for example, now has knowledge bases for LSI Logic, Toshiba and Hughes gate arrays.

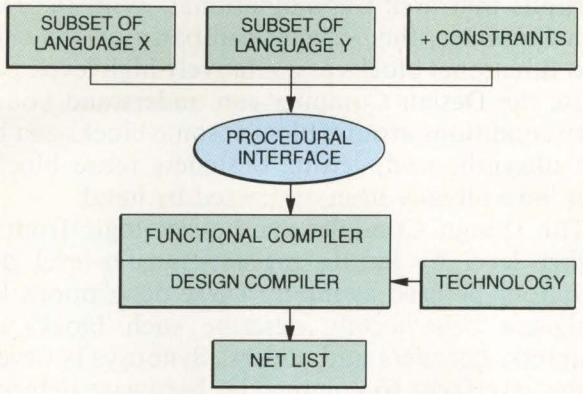
The Synopsys Logic Compiler has been used extensively at Harris Semiconductor (Melbourne, FL) and has considerably improved many combinational circuits. The tool has always produced faster circuits than those designed manually, with an average improvement of 30 percent. The area efficiency matches that of senior-level IC designers, and when those designers are factored out of the statistics, the area improvement averages 40 percent. Speed is another advantage—one circuit that took nine engineer-weeks to design manually was redesigned completely by the Logic Compiler in two hours.

"The tool produces its highest payback when you design ICs from scratch," notes Michael Bohm, section head of semicustom product development. "We've designed circuits in hours that would otherwise have taken weeks. The Logic Compiler also makes it easy to go from one technology to another, such as from CMOS to gallium arsenide." Harris generally uses the Logic Compiler on blocks with 200 to 500 gates.

Both the Logic Compiler and the Logic Consultant have been benchmarked by Larry Drenan, manager of the advanced design methodology product at Hughes Aircraft (El Segundo, CA). "These tools all approach what the designer can do by hand, and in some cases the tools might do better," he says. To provide behavioral input into the Logic Consultant, Hughes is prototyping a link to the Verilog hardware description language from Gateway Design Automation (Westford, MA).

The Synopsys Logic Compiler is limited because it handles only combinational logic, requires Boolean or net-list input, and doesn't support hierarchical design. The Design Compiler overcomes these limitations and provides a more user-friendly interface. A fully commercialized product, the Design Compiler offers interfaces to CAE environments from Cadnetix (Boulder, CO) and SDA Systems, and Synopsys is working to sign up other CAE vendors. Trimeter will also announce a second-generation synthesis tool this month, but details aren't available yet.

Unlike the Logic Compiler, the Design Compiler can optimize such components as storage elements and sequential feedback loops. Sequential optimization is allowed by an ability to work with implicit timing constraints. "The minute you throw in sequential logic, you have to deal with many more constraints," says Aart de Geus, vice-president of research and development at Synopsys. "You need to derive internal setup and hold constraints from global constraints, and that implies an ability to trace through clock networks." It should be noted, however, that little or no minimization is performed on the sequential logic.



The Synopsys Design Compiler accepts high-level inputs by providing a procedural interface that can accept subsets of hardware description languages. The Design Compiler can now accept register-transfer-level inputs, and the company is developing interfaces to commercial and in-house languages.

Hierarchy is another concept behind the Design Compiler. The Logic Compiler essentially flattens

out designs, works at the gate level, and cuts out portions that aren't combinational. With the Design Compiler, the designer can partition the chip into functional blocks at a relatively high level. Because the Design Compiler can understand boundary conditions around blocks, some blocks can be left unsynthesized, letting designers reuse blocks that have already been optimized by hand.

The Design Compiler synthesizes logic from a higher level by letting register-transfer-level descriptions be used as input. These descriptions let designers behaviorally describe such blocks as counters, decoders and adders. Synopsys is developing interfaces to commercial hardware description languages that support register-transfer-level descriptions and include a simulation capability.

Two new companies that are grappling with behavioral synthesis are Silc Technologies and Algorithmic Systems (Braintree, MA). Both have their intellectual roots in the MacPitts silicon compiler project from the Massachusetts Institute of Technology (Cambridge, MA). Silc is a spin-off of GTE Laboratories (Waltham, MA), and its Silcsyn system is a continuation of research that began with GTE's Silc silicon compiler. Algorithmic Systems is largely the work of its founder and president, Jay Southard, a co-developer of MacPitts.

The MacPitts compiler was perhaps the first truly behavioral silicon compiler, but its silicon implementation was inefficient. Silc and Algorithmic Systems have stripped away the silicon-compilation aspect and introduced toolsets that map logic into commercial ASIC libraries. The algorithmic input languages offered by these companies bear a resemblance to MacPitts' Lisp-based input language.

The extent to which Silc and Algorithmic Systems are "behavioral" depends on how one defines this elusive term. "What we have is a microarchitectural behavioral language," says Jeff Fox, Silc engineering vice-president. "It's not a behavioral simulation language like VHDL or Verilog, and it's not a register-transfer-level language, which is a structural language. We came up with a hybrid—a behavioral domain language where the constructs have very clean semantics for synthesis."

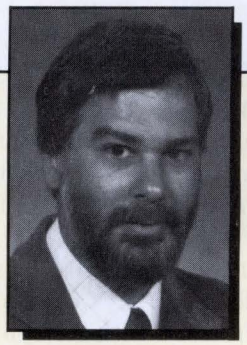
Writing a design description in Silc's Lisp-based language is much like programming in a high-level language, but there's a much closer relationship between the behavioral description and the resulting architecture. "If you want an efficient chip, you have to understand the implications of what you're writing," says Fox. A case statement, for example, might clearly imply a priority encoder if it's executed in a given state. Such implications wouldn't exist in VHDL or C.

The Lisp-based Ascyn language from Algorithmic Systems represents a purely algorithmic approach that distances the user from structure. "Any algorithm can be implemented," says Algorithmic Systems' Southard. "It doesn't matter what type of architecture the silicon uses. Ascyn generates a hierarchical cell net list, and the implementation is left to the ASIC vendor." Originally developed on the Macintosh, Ascyn is primarily aimed at relatively small ASIC designs.

Both languages can handle arithmetic as well as Boolean expressions, and they can synthesize both

```
;;Combinational Logic Machine
 (clm output-segments
   (set segments (encode display connect
            (0 #b0111111)
            (1 #b0000110)
            (2 #b1011011)
            (3 #b1001111)
            (4 #b1100110)
            (5 #b1101101)
            (6 #b1111100)
            (7 #b0000111)
            (8 #b1111111)
            (9 #b1100111))))

;;Data and Control Machine
 (dcm derive-su-clock
   (declare (clocked-by ref))
   (set clock-su-source pre-div.bitlout)

 (dcm output-digits
   (declare (clocked-by ref))
   (par (set digits 1)
     (set display-connect seconds-units))
   (par (set digits 2)
     (set display-connect seconds-tens))
   (par (set digits 4)
     (set display-connect minutes-units))
   (par (set digits 8)
     (set display-connect minutes-tens)))

 (dcm seconds-units
   (declare (clocked-by clock-su))
   (set clock-st-source seconds-units.boolean))

 (dcm seconds-tens
   (declare (clocked-by clock-st))
   (set clock-mu-source seconds-tens.boolean))

 (dcm minutes-units
   (declare (clocked-by clock-mu))
   (if minutes-units.boolean
     (incr-counter minutes-tens))))
```

Silc Technologies' Lisp-based Silcsyn language lets designers describe chips as combinational logic machines (CLMs) and data and control machines (DCMs). To implement this description of a 60-min. timer, the designer defined I/O pads, chip clocks, chip resets, chip counters and variables. The CLM here is a seven-segment decoder. The DCM is a four-state machine, and the par construct specifies parallel execution.



George Bouhasin
Director of Corporate Advanced Development Systems
Mentor Graphics

Board-level synthesis requires multivendor cooperation

Until now, most logic-synthesis efforts have concentrated on chip-level logic design. Yet board-level logic synthesis is just as feasible, and the market for the technology is many times larger. In both cases, synthesis tools are needed that automate the now tedious process of partitioning a high-level logic description into lower and lower functional blocks.

Board-level synthesis is a broader challenge than chip-level synthesis because more suppliers play a role in board- and system-level design. These suppliers include commercial device manufacturers, application-specific IC vendors, bus developers and the software vendors that supply niche tools such as behavioral models. The rapid evolution of logic synthesis, therefore, will require the emergence of a standard electronic design automation (EDA) platform for logic synthesis that all suppliers can confidently support. This platform will be defined by the market's acceptance of the data base structure it uses.

Board designers are now the primary users of programmable logic devices (PLDs)—the first board-level proving ground for logic-synthesis tools. Since the advent of PLDs, synthesis tools have been in high demand because designers want to use the devices without delving into the details of chip-level logic. They want a system that can automatically evaluate the high-level functions to be accomplished and then partition them into a fewer number of readily available parts.

Companies such as Minc (Colorado Springs, CO) answer this demand with synthesis tools that translate conceptual design descriptions into files that can be downloaded to a PLD programming box. These tools represent the described functionality using only PLDs. Eventually, however, synthesis tools won't only partition a design into PLDs—they will select from many standard parts. Designers will be able to program these synthesizers to make selections according to vendor, cost or performance requirements.

While PLD synthesis tools are generating interest in logic synthesis among board designers, there are a few pieces of the synthesis puzzle that must be developed before the technology makes a more complete transition to the board level. First, a front-end description language is needed to input desired functional and performance requirements. The IEEE-1076 standard hardware description language, VHDL, has been proposed as a possible textual input format. But the platform that becomes the industry's de facto standard for logic synthesis will probably incorporate a front-end description language that allows both textual and graphical input formats.

A second issue is model availability. To make the best parts selection, the synthesizer will need access to an extensive library of models, including semicustom, semistandard (PLDs) and standard parts libraries supported by the semiconductor manufacturers, as well as behavioral language models and hardware models for microprocessors and other complex parts. Because board designers will need to simulate what has been synthesized, the models should accommodate both tasks.

Today, EDA vendors must work closely with ASIC foundries to provide ASIC designers with fully qualified standard cell and gate array libraries. In the future, similar relationships will be forged between EDA vendors and commercial semiconductor houses to provide the parts models needed for board-level logic synthesis. In fact, it will become a practice for IC manufacturers to release models qualified for specific EDA systems when they release a new chip. This trend is already under way, as evidenced by the recent simultaneous release of the 80960 microprocessor from Intel (Hillsboro, OR) and the hardware model of the chip from Mentor Graphics (Beaverton, OR).

The pieces needed to put together an effective board-level logic-synthesis system can't be supplied by a single vendor. To ensure quick distribution and accuracy, commercial IC vendors and ASIC foundries will probably develop and market synthesis models in tandem with new devices. There's also a great opportunity for niche software developers to market alternative models, algorithms and knowledge bases for synthesis. All of these suppliers, however, need a reliable target system on which to base their tools. A standard EDA system platform with an open data base architecture must emerge, therefore, before board-level logic synthesis truly gains momentum.

sequential and combinational logic. These languages don't depend on limited architectures such as PLAs or finite-state machines, and they can handle both data path and control logic. Silc's language introduces the concept of data and control machines (DCMs), which provide a unified description of control and data flow and can be clocked synchronously or asynchronously.

To use Silcsyn, the designer first writes a design file that describes the circuit in terms of DCMs and combinational logic machines (CLMs). This behavioral description is verified with a functional simulator. The designer then creates a corresponding implementation file with specifications and constraints that describe the area and timing tradeoffs for the gate-level implementation. Here, the designer might specify such structural details as fan-out rules, depth of Boolean logic and number of look-ahead bits for arithmetic units.

The designer's behavioral description provides high-level partitioning for the chip. Silcsyn can then partition and allocate control logic and data path logic, producing a structural description that identifies such blocks as ALUs, counters and registers. A variety of algorithms are used for two-level and multilevel logic minimization. Then the description is mapped into the target cell library, using rules that are encoded algorithmically.

One attractive aspect of Silcsyn is its ability to automatically synthesize built-in testability structures. Silcsyn provides a register-transfer-level scan capability that lets designers specify the allowable sequential depth of the circuit.

Silcsyn runs on Apollo and VAX workstations and offers an interface to Mentor Graphics' schematic entry and simulation tools. It now supports a 2-micron standard-cell library from NCR Microelectronics (Fort Collins, CO). Algorithmic Systems' Ascyn runs on the IBM PC, VAX and Macintosh and supports a 2-micron gate array library from California Devices (San Jose, CA). Prices for Ascyn start at just $5,000.

While behavioral synthesis is everybody's long-range goal, it raises a lot of questions today. "When you're operating at a higher level of abstraction, what do you do with all the information you're not representing?" asks Geoff Bunza, Mentor Graphics' director of engineering. "The tool can fill in assumptions, but will designers trust it?" To gain that trust, Silc and Algorithmic Systems must now demonstrate that their tools can produce efficient silicon.

NCR Microelectronics has used Silcsyn in-house and will add it to the ASIC design system it now supports on Mentor Graphics workstations. But Silcsyn represents a radically new approach to design, and it will require a learning process. "It takes at least a design or two to get an intuitive feel for the tool," says Harold Crasts, NCR manager of strategic technology. "Most designers will have to spend six months practicing designs to really get into it."

With assistance from Silc engineers, NCR was able to generate a 500-gate functional block in one-and-a-half days. But a complex SCSI (small computer system interface) macro that involved asynchronous design was a much tougher challenge. "So long as the design is synchronous, it's like rolling off a log. But we had a problem getting the asynchronous signals to interface with the synchronous internals of the design," says Crasts.

Hughes' Drenan was impresssed with Silcsyn but didn't want to add another proprietary design language to those now in use at Hughes. "Silcsyn seems to work fairly well if you're willing to describe the whole design in their language, but it's not worth it for us to use another language. We already have a setup using Mentor workstations and Verilog," he says.

Drenan's concern indicates that an industry-standard behavioral input language could substantially increase the appeal of logic synthesis. Since VHDL is on its way to becoming an industry standard, it's an obvious target for logic-synthesis companies. VHDL wasn't designed for synthesis, and it's a very broad and complex language where one can express the same concept in many different ways. Nevertheless, Synopsis and Trimeter are including VHDL in long-range plans.

Once logic synthesis is established in the ASIC industry, the next frontier will be board-level synthesis using standard components. "There's no reason multilevel logic algorithms can't select components from TTL libraries," says George Bouhasin, Mentor's director of corporate advanced development. "The problem today is that there really aren't enough models for all the standard components."

In addition to providing a huge standard component library, a board-level synthesis tool would have to assist with partitioning and device selection. The PLD design systems from Minc and HP are perhaps forerunners of board-level tools that will provide such capabilities. Board-level synthesis tools will also have to deal with complex timing relationships between components and provide a worst-case timing analysis that can examine a range of minimum and maximum component values.

Eventually, an engineer will be able to describe a design using a high-level behavioral language and then plug that description into a tool that produces a structural design for a complete chip, board or system. The progress toward this goal will be incremental rather than revolutionary, and designer acceptance may be slow at first. In the long run, however, the move from low-level schematics to logic synthesis may be as significant as the software industry's leap from assembly-language programming to high-level languages. **CD**

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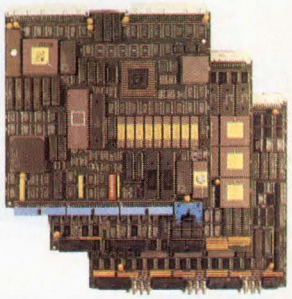

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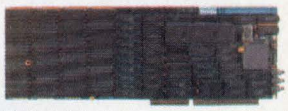

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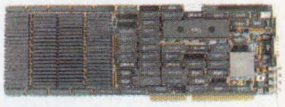

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- Palette: Up to 16.7 Million Colors
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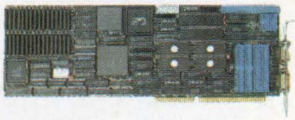
- Addressable Resolution: Up to 2048 x 1024 x 8, Plus 2 Overlays

OMNI 1500 DLP/OMNI 1500 GDS



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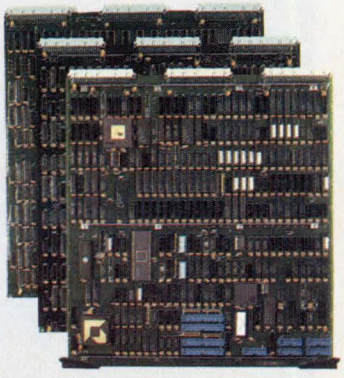
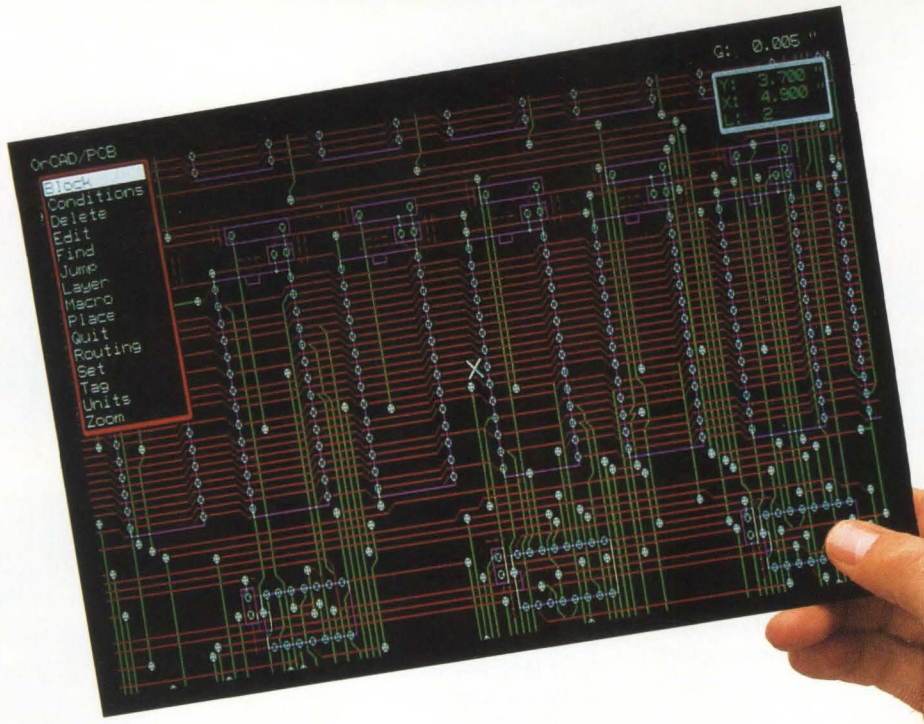
- 4 RS-232-C Serial Ports
- OMNI 1500 GDS is an OMNI 1500 DLP plus 1 to 8 OMNI 1600 GDC's

OMNI 2000 GDS



- MULTIBUS II 9U x 400 mm
- DEC DMA Compatible
- GKS Display List Processing
- Viewable and Addressable Resolution: 1280 x 1024
- Hardware Cursor
- 2 Overlay Planes
- Modular Configurations
- Multiple Processors
  - Geometry Processor: Am29116
  - F.P. Coprocessor: Am29325
  - Graphic Coprocessor: Discreet
  - Peripheral Coprocessor: 80188
  - Display List Processor: 80386/80387



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- Ratsnest and force vector placement.
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   Seltech, Inc.
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14. E. PA, NJ, NY
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    416-475-6730

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503-640-5007

CIRCLE NO. 37

DESIGNERS' BUYING GUIDE

Model	Platforms: Operating Systems	Printed Circuit Board CAD Interfaces	Component Libraries	ASIC Libraries	Options	Price
A B Associates PO Box 82215, Tampa, FL 33682 (813) 932-9853						**Circle 251**
CF/IG-Spice	IBM PC/AT	I-G Spice	200 analog discrete devices: CMOS, TTL, ECL, digital blocks	—	I-G Spice circuit sim. pkg	$990
Accel Technologies 7358 Trade St, San Diego, CA 92121 (619) 695-2000						**Circle 253**
Tango-Schematic	IBM PC: MS-DOS	12 interfaces	3,100+comp. in each of 16 lib.	—	all inclusive	$495
Advanced Microcomputer Systems 2780 S W 14th St, Pompano Beach, FL 33069 (800) 9PC-FREE						**Circle 255**
Cell	IBM PC/AT/XT, PS/2 (OS/2): DOS	outputs netlists in 9 formats	1,000+ SSI/MSI: TTL, ECL, IC fam.	—	std. opt.: interface to PCB layout PC-Pro and autorouter PCRoute	$100 sw only
Aldec-Automated Logic Design 3525 Old Conejo Rd, #111, Newbury Park, CA 91320 (805) 499-6867						**Circle 257**
Slav	IBM PC/XT/AT: PC-DOS	Pads, P-CAD, Futurenet	3,000+: CMOS, TTL, ECL, PLDs, memories	Fujitsu	sim. block diagrams and schematics (interactive)	$995 incl. interactive simulator
Digi-Lab	same as above	—	200+: CMOS, TTL, controllers	—	same as above	$1,995 educat. site license
Altera 3525 Monroe St, Santa Clara, CA 95051 (408) 984-2800						**Circle 258**
Logicaps	IBM XT/AT	—	7400 Series TTL, Adlib	—	additional lib.	$650 sw
Analog Design Tools 1080 East Arques Ave, Sunnyvale, CA 94086 (800) ANA-LOG4						**Circle 259**
Analog Workbench Circuit Editor	Apollo Domain: Aegis; HP 3000, 320, 350: HP-UX; DEC VAXStation II, II/GPX, 3200 & 3500: VMS; Sun -2, -3, -4: Unix	—	over 1,400 analog devices	6 lib.	Spice 2G.6 & Spice plus and others	$14,500 sw only $24,100 to 61,800 turnkey
PC Workbench Circuit Editor	IBM PC/AT & Compaq 286 w/opus coproc.: Unix	—	same as above and std. device lib. of 500	same as workstations	same as workstations	$8,000 sw only $15,800 turnkey
Aptos Systems 5274 Scotts Valley Dr, Suite 107, Scotts Valley, CA 95066 (408) 438-2199						**Circle 262**
Criterion I	IBM: DOS	Cadnetix, Calay, Sicards	1,200: CMOS, TTL, ECL, SMD, analog μP	—	—	$495
Automated Images 500 W Cummings Park, Woburn, MA 01801 (617) 933-1731						**Circle 263**
Ideel-ESD	80286, 80386-based PCs: MS-DOS	—	—	—	reliability & maint., wiring cabling & harnessing design, Pspice	$7,500 sw; $14,000 EGA 386/workstation; $17,500 hi-res 386/workstation

Model	Platforms: Operating Systems	Printed Circuit Board CAD Interfaces	Component Libraries	ASIC Libraries	Options	Price
Automated Images 500 W Cummings Park, Woburn, MA 01801 (617) 933-1731						**Circle 263**
Ideel-EDM	80286, 80386-based PCs: MS-DOS Apollo, DEC, Sun	–	–	–	program. & graphical interface, eng. data mgr report apps.	$25,000 sw only
Cadam 1935 N Buena Vista St, Burbank, CA 91504 (818) 841-9470						**Circle 267**
CADex	IBM mainframe, VM and VMS, IBM PC	IPC	14,000+user-definable also: discrete & digital CMOS, TTL, ECL	user-definable	sim. to Cadat	$25,000
CADdy 3401 Algonquin Rd, Suite 340, Rolling Meadows, IL 60008 (312) 394-7755						**Circle 268**
CADdy Electronics	IBM XT/AT, 386, PS/2, w/math coproc.: MS-DOS	CADdy	1,000: CMOS, TTL, analog, schematic and layout incl.	–	–	$1,895 incl. layout pkg
Cadnetix 5775 Flatiron Parkway, Boulder, CO 80301 (303) 444-8075						**Circle 269**
CDX-3000 software CDX-9500 turnkey CDX-9600 turnkey CDX-8101 software	IBM PC/AT: DOS 3.0 or higher (HP, Wyse, AT&T); Sun-3, -4: Unix	EDIF, IGES 3.0, Mentor, Redac, Scicards, Valid	3,000+: CMOS, TTL, ECL, CAD & CAE symbols	15+ASIC design kits	digital, analog and fault sim., physical modeling, CAD tools	$4,950 sw (PC); $7,000 turnkey (CDX-5000A); $10,800 sw (Sun); $15,900 turnkey (Sun)
CAECO 2945 Oakmead Village Court, Santa Clara, CA 95051 (408) 988-0128						**Circle 270**
CAECO Schematic	Sun -3, -4, Apollo: Unix 4.2	–	–	–	sim. interface to Verilog, Hilo-3, Silos, Hspice, Spice	$10,00 sw only
Calay Systems 16842 Von Karman Ave, #100, Irvine, CA 92714 (714) 863-1700						**Circle 271**
Prisma	Sun-3: Unix	Calay, CV, Recal-Redac, Scicards	5,000 SSI/MSI parts: CMOS, TTL, ECL, PAL	–	sim. interface to Cadat	–
Calos 3419 Edison Way, Fremont, CA 94538 (415) 657-4430						**Circle 272**
Calos 6000-sch	80286 & 80386: PC-DOS	Cadnetix, Calay, Calos, CV, Pads PCB, Racal-Redac, Scicards, Telesis	6,000+: CMOS, TTL, ECL, PAL, analog	–	sim. (analog, digital) interface to 8 PCB design systems, auto. ECO to Calos 6000 PCB	$4,000 sw only
Case Technology, Div. of Teradyne, 2141 Landings Dr, Mt View, CA 94043 (415) 962-1440						**Circle 273**
Vanguard Stellar Schematic Design System	IBM PC/AT, PS/2 50, 60, 80: DOS; Sun-3: Unix, VAX, μVAX2000, VSII/6PX: VMS	Cadnetix, Calay, CV, CBDS, Racal-Redac, Scicards, Telesis	5,000+: CMOS, TTL, ECL, ASIC, PLD, μP devices	20+ASIC design kits	sim. logic & circuit, interfaces to Interleaf & Venture Publishing, Ask's Manman manufact., timing verifier	$5,700 to $15,000 PC; $7,400 to $10,000 Sun & DEC sw

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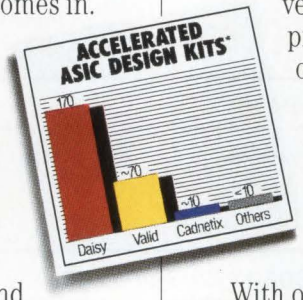
Not long ago, designing ASICs wasn't even part of your job. Now it's the part everyone's counting on.

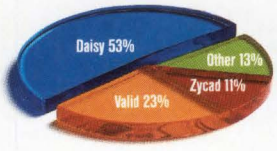
That's where Daisy comes in.

Daisy CAE tools are used by more ASIC designers than any other CAE workstations.



Because from schematic creation through post-layout simulation, Daisy has what it takes to keep ASICs on time and on budget.

For example, our MegaLOGICIAN™ simulation accelerator is seamlessly integrated with the schematic, so



Simulation accelerator market share. Source: Prime Data, 1985 and 1986 unit shipments

you can locate and correct design problems interactively. That means faster debugging and more time to improve the quality of your design.

Plus no other accelerator is as well supported, with more than 170 design kits supplied by 70 different vendors. So you can build productivity instead of libraries.

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*Based on minimum 10x performance improvement compared to 32-bit workstations. Source for design kit estimates: VLSI Systems Design's Semicustom Design Guide, 1987.

Model	Platforms: Operating Systems	Printed Circuit Board CAD Interfaces	Component Libraries	ASIC Libraries	Options	Price
Computervision, Div. of Prime Computer, 100 Crosby Dr, Bedford, MA 01730 (617) 275-1800						**Circle 274**
Schematic Design	Sun-3: Unix Sun-4: Spare CV's CADDStation version	Autoboard SMT, CADDS 4X	3,000+ SSI/MSI/LSI, TTL, ECL, PAL, memory, VLSI	—	Cadat6-HHB Systems, Saber-Analogy, Spice 26.6, Hilo-Genrad, Gards-Silvar-Lisco	$7,500 sw
Personal Engineer	IBM PC and compat., CV386	Autoboard SMT	3,500+ SSI/MSI/LSI, TTL,ECL, PAL, memory, VLSI	—	—	—
Control Data 2800 Old Shakopee Rd, Box 0, Minneapolis, MN 55440 (612) 853-3117						**Circle 275**
Midas	Apollo, Mentor	—	SSI/MSI: TTL	CMOS, VLSI-6000, VLSI-7118, VL-5000	interface to system-level Cyber-based Midas system	$60,000 to $285,000 workstation lib. $2,000, sw Cyber 180 family
Daisy Systems 700 E. Middlefield Rd, Mountain View, CA 94039 (415) 960-6674						**Circle 276**
ACE	Personal Logician 386 and Logician 386: Daisy-Dnix; Sun 386, Compaq Deskpro 386 and IBM PC AT: Daisy-Dnix	18 interfaces	4,500+ digital parts: CMOS, TTL, ECL, HCMOS, PLD, RAM, ROM, μP; 1,300+ analog parts: discretes, ICs, converters, power devic	170+ASIC design kits	sim., PLD design, PCB interfaces, procedural interface to database	$6,000 sw (PC) $25,000 turnkey (EGA/Color)
Dasoft Design Systems 1827-B Fifth St, Berkeley, CA 94710 (415) 486-0822						**Circle 277**
Project: PCBC+	IBM PC/XT/AT, PS/2: DOS	Project: PCBC+	CMOS, Hitachi, Intel (optional), 74xx/ 74LSxx	—	PCB Layout, EGA opt.	$1,500 sw
Data I/O 10525 Willows Rd N E, PO Box 97046, Redmond, WA 98073 (206) 881-6444						**Circle 289**
Dash Schematic Designer	IBM AT, PS/2, Compaq 386	Applicon, Cadam, CBDS, CV, Redac, Scicards	CMOS, TTL, ECL, discrete, memory, Intel, Motorola, Xilinx, ANSI IEEE	Gould, Hitachi, Motorola, National, Toshiba	Logic Synthesis for ASICs & PLDs, sim. interfaces, translator toolkit for custom trans.	$3,990
Design Computation Sherman Square, Route 33, Farmingdale, NJ 07727 (201) 938-6661						**Circle 278**
Draftsman-EE	ICM PCs and compat.: DOS, 640K & hard disk required	netlist input opt.: Futurenet, OrCAD, (EDIF), Scicards, Racal-Redac, HP	4,000: CMOS, LS, ALS, AS, 5, HC, HCT, memory, RCA-linear	—	foreign netlist, convert HP Ljet output	$395
Draftsman EE-II	same as above	same as above	same as above	—	same as above, hi-res. video	$695
Douglas Electronics 718 Marina Blvd, San Leandro, CA 94577 (415) 483-8770						**Circle 279**
Douglas CAD/CAM Schematic	Apple Macintosh Unix compat.	prop. CAD pkg, others planned for future	500+ parts: CMOS, TTL, PALs, PROMs, unlimited user-definable devices	—	sim. interface to Douglas CAD/CAM professional layout	$700 sw only

Model	Platforms: Operating Systems	Printed Circuit Board CAD Interfaces	Component Libraries	ASIC Libraries	Options	Price
ESP 18013-C Skypark Circle, Irvine, CA 92714 (714) 261-1777						**Circle 285**
Lognet	IBM PC and compat.: MS-DOS	Racal-Redac	HCA6000, MCA600ECL, MCA1200ECL, TTL	10+ var. lib. avail.	all interfaces incl.	$650
Europe Silicon Structures Hollybank House, Mount Ln, Bracknell, Berks, RG12 3DY, United Kingdom, (034) 452-5252						**Circle 288**
Solo 1000/Solo 1200	Apollo: Aegis DEC: VMS IBM PC/AT: DOS Sun: Unix	—	350+ SSI/MSI: CMOS, TTL, I/O pads, 7400 series, system cell	Tool is tied directly to US2/ES2 Silicon	part of integrated Solo IC generation tool	$22,500 bundled
Harris Scientific Calculations 7796 Victor-Mendon Rd, PO Box H, Fishers, NY 14453 (716) 924-9303						**Circle 322**
Scidesign	IBM PC/AT & compat.: DOS	Scicards, μ cards CV, Simulation Spice, Cadat	600+ SSI/MSI: CMOS, TTL, ECL	—	standard, CAE program. lang.	$3,000 sw
Harris Semiconductor/Semicustom Products PO Box 883, Melbourne, FL 32901 (305) 724-7000						**Circle 294**
Optilogic.F	Sun-3: Unix	—	HHB std. parts lib.	100+ basic cards, 10 megacells, RAM, ROM compiler	Cadat logic/fault sim. std.	$47,000
Optilinear.F	Sun-3: Unix	—	no	bipolar, PJfet, thin filmR, parameterized cells	circuit sim., movie carlo, ERC std.	$43,000
Hewlett-Packard 1820 Embarcadero Rd, Palo Alto, CA 94303 (415) 857-1501						**Circle 295**
Design Capture System	HP9000 series 300: HP-UX	HP Printed Circuit Design System, Calay, CV, Racal-Redac, EDIF200, Scicards	5,000+: CMOS, TTL, ECL 2,200+ analog, microprocessor	10+ ASIC design kits	sim., interfaces to layout systems, libraries, HP Logic Analyzer link	$8,000 sw $25,000+ turnkey
IBM 2077 Gateway Place, San Jose, CA 95110 (408) 288-4100						**Circle 297**
Computer-Integrated Electrical Design Series (CIEDS)	IBM PC/AT, PS/2 (model 50 and above): DOS; RT PC: AIX-System/370: VM	CIEDS/CBDS	2,500+: TTL comp. and discrete dev.	—	interface to CIEDS/behavorial, logic, A/D, and switched capacitor simulators, Hilo3, Spice 2G, CIEDS/CBDS	$2,900 sw (PC and PS/2) $8,000 sw (RT PC) $75,000 sw (S/370)
IC Designs 12020 113th Ave NE, Kirkland, WA 98034 (206) 821-9202						**Circle 298**
Desedit Design Editor	IBM PC/AT: MS-DOS	—	—	IC Designs 2-μm CMOS standard cell lib.	front-end to ASIC design, analysis, and verification system	$10,000 bundled into IC Works desktop ASIC design system
Intergraph One Madison Industrial Park, Huntsville, AL 35807 (205) 772-2000						**Circle 305**
Designer Engineer Hierarchical schematic design pkg	Clipper-based workstations: Unix System V.3	Intergraph PCB Eng. pkg, Hybrid Engineer pkg, Telesis, EDIF, SDL	3,000+ symbols: CMOS, TTL, ECL, memory, μP, peripheral devices	5	Intergraph Digital Analysis Tools (DAT), interface to Hilo-3, Analog Analysis Tool (AAT) interface to CSpice	$5,000 sw

Model	Platforms: Operating Systems	Printed Circuit Board CAD Interfaces	Component Libraries	ASIC Libraries	Options	Price
Intergraph One Madison Industrial Park, Huntsville, AL 35807 (205) 772-2000						**Circle 305**
Design Engineer PC, Hierarchical schematic design package	IBM PC/AT and compat.: DOS	Intergraph PCB Eng., Hybrid Eng., EDIF	3,000+ symbols: CMOS, TTL, ECL, memory, μP, peripheral devices	5	Hilo and Cspice netlist interfaces	$3,000 sw
Interactive CAD Systems 2352 Rambo Ct, Santa Clara, CA 95054 (408) 970-0852						**Circle 304**
ProCAD Xtra	IBM PC/AT: DOS VAX: VMS	Futurenet, rat's nest	1,000+ SSI/MSI: CMOS, TTL, linear	—	—	$695 sw (PC) $2,500 sw (VAX)
LSI Logic 1551 McCarthy Blvd, Milpitas, CA 95035 (408) 433-8000						**Circle 306**
LSED	Sun: SunOS	—	—	LSI Logic, channel-free array cell-based	interfaced to LSI logic simulation environ.	—
Matra Design Semiconductor 2895 Northwestern Parkway, Santa Clara, CA 95051 (408) 986-9000						**Circle 307**
GateAID (modified OrCAD/SDT)	PC/XT/AT, 386, PS/2, OS/2: DOS	—	SSI/MSI parts: PALs, gates, FFs, I/O buffers	same as comp. lib.	std. w/GateAID Plus/PC design system, incl. sim. and testability analysis	$945.00 incl. sim. and testability analysis tools, design lib. and documentation
Mentor Graphics 8500 S W Creekside Pl, Beaverton, OR 97005 (503) 626-7000						**Circle 308**
Neted	Apollo: Aegis, Unix	Calay, CV, EDIF 2 0 0, Redac, Scicards, Telesis	5,000+: CMOS, TTL, ECL, PLDs, memories, analog	100+ ASIC Design Kits	Integration w/Quicksim, QFault, Board Stn, Chipgraph, Gate Std. & Cell Std.	$16,900 hw & sw
Mietec Westerring 15, Oudenaarde, Belgium, 9700, (322) 242-5010						**Circle 310**
SDS	VAX: VMS	—	digital and analog lib.	1.5- to 3-μm CMOS	sim. (analog, digital, mixed aid) layout	—
Motorola, ASIC Div., 1300 N Alma School Rd, Chandler, AZ 85224 (602) 821-4426						**Circle 311**
MDS (Modular Design System)	Apollo, Mentor	—	—	HCA62A, MCA2 & MCA3 bipolar BiMOS, 2M and 3M std. cells	sim. interface to Motorola, IBM mainframe CAD systems	$500
National Semiconductor 2900 Semiconductor Dr, Santa Clara, CA 95051 (408) 721-5000						**Circle 312**
Faircad	Apollo: Aegis IBM PC: DOS all VAX VMS platforms, Sun: Unix	CBDS, Racal-Redac, Scicards, Semai	—	ECL, Aspect, CMOS 1.5-μm gate array, CMOS 2-μm std cell	sim., place & route	—
Oki Semiconductor 650 N Mary Ave, Sunnyvale, CA 94086 (408) 720-1900						**Circle 313**
—	Daisy, Futurenet, Mentor, Valid	—	4,000 SSI/MSI: CMOS, TTL	250	netlist sim.	no charge for lib.
Omation 1210 E Campbell Rd, Richardson, TX 75081 (800) 553-9119						**Circle 314**
Schema II	IBM PC/AT, PS/2, 386 and compat.	30+ supported	3,600 SSI/MSI: CMOS, PAL, VLSI, μP, IEEE, IEC	Intel: EPLD LSI Logic, Xilinx	sim., PCB Layout	$495 sw (PC) (schematic only)

Model	Platforms: Operating Systems	Printed Circuit Board CAD Interfaces	Component Libraries	ASIC Libraries	Options	Price
OrCAD Systems 1049 SW Baseline St, Suite 500, Beaverton, OR 97123 (503) 640-5007						**Circle 315**
OrCAD/SDT	IBM PC/XT/AT, PS/2 and compat.	25 interfaces	3,700+: CMOS, TTL, ECL, MPU, discrete, analog, RF	—	pkg complete	$495
Personal CAD Systems 1290 Parkmoor Ave, San Jose, CA 95126 (408) 971-1300						**Circle 316**
PC-Caps	IBM PC/AT: DOS	Calay, CV, P-CAD, Redac, Scicards	5,500 parts: CMOS, TTL, ECL, memory, linear, μP	11 lib.	sim. interface to Hilo, Cadat, Tegas, Spice	$1500+ sw only
Phase Three Logic PO Box 985, Hillsboro, OR 97123 (503) 640-2422						**Circle 317**
Capfast CF1000, CF3000	IBM PC/AT, PS/2: DOS	Cadnetix, CADDS4X, Pads, Racal-Redac, Scicards	2,000+ parts: CMOS, TTL, ECL, EM, linear, memory, μP	Fujitsu	program., netlist lib., simulator interfaces, sim. grapher	$395 (EGA) $1,295 (EGA) incl. simulator interfaces & sim.grapher
Capfast CF5000, CF6000	Sun workstation, mono (CF5000), color (CF6000): Unix	Cadnetix, CADDS4X, Racal-Redac, Scicards	2,000+ PARTS: CMOS, TTL, ECL, EM, linear, memory, utility	Fujitsu	same as above	$2,950 (mono) $4,950 (color)
Capfast CF3550	IBM PC/AT: DOS 1024×768 graphics card incl.	Cadnetix, CADDS4X, Pads, Racal-Redac, Scicards	same as above	Fujitsu	same as above, DOS extender version	$2,950 incl. graphics board, simulator interface, sim. grapher
PRO.LIB 624 E Evelyn Ave, Sunnyvale, CA 94086 (408) 732-1832						**Circle 318**
Autoschema	Apollo: Aegis IBM PC/AT: DOS Sun 3: Unix	Auto PCB	5,000 parts: CMOS, TTL, ECL, analog, PALs, Micro (Intel)	—	—	$495
Racal-Redac Westford Regency Park, 238 Littleton Rd, Westford, MA 01886 (617) 692-4900						**Circle 319**
VDC	Apollo: Unix DEC: VMS Sun 3: Unix	Racal-Redac, EDIF in development	4,000+ SSI/MSI/LSI parts: CMOS, TTL, ECL, PAL	10+ in development	sim., PCB layout, CAM output, waveform analysis	$10,000 to $100,000 sw; $15,000 to 150,000 turnkey
Schlumberger CAD/CAM 4251 Plymouth Rd, PO Box 986, Ann Arbor, MI 48106 (313) 995-6000						**Circle 321**
Bravo3 Design Capture	Sun: Unix VAX: VMS	Bravo3, others via user-config. netlist converter	4,000 SSI/MSI/LSI/analog: CMOS, MOS, TTL, ECL	—	extended comp. lib.	$2,500 sw
SDA Systems 555 River Oaks Parkway, San Jose, CA 95134 (408) 943-1234						**Circle 323**
SDA Schematics	Apollo: Domain/IX DEC: Ultrix Sun: SunOS	—	std. and complex gates	—	interfaces to HILO3, SILOS, Verilog, Spice	$5,000 schematic capt. sw $8,000 design framework sw
Silvar-Lisco 1080 Marsh Rd, Menlo Park, CA 94025 (415) 324-0700						**Circle 327**
SDS	Apollo: Aegis IBM PC/AT, PS/2: DOS; IBM RT PC, Sun: Unix; Mainframe: VM/CMS; VAX, VAXStation: VMS	Cal-PC, CBDS	4,500+ SSI/MSI: CMOS, TTL, ECL, PLD, memory	10+ lib.	behavioral, logic, mixed A/D, switch cap. filter sim., gate array, std. cell, PCB, full custom layout	$9,000+ (workstation sw only)

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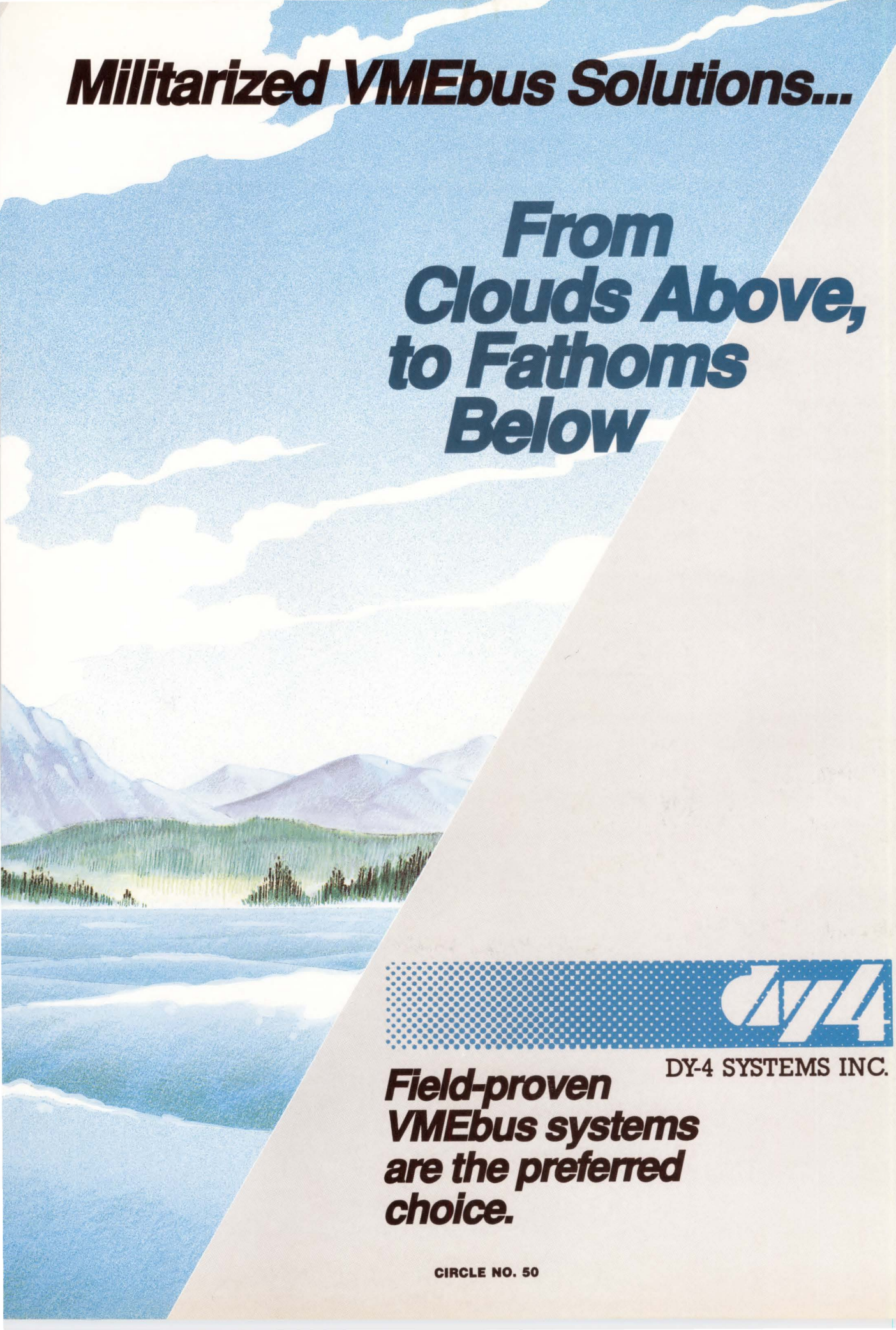
From Clouds Above, to Fathoms Below



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High performance, industry standard, multiprocessing architectures, applicable to Mil-Spec applications, field-proven ... DY-4's VME solutions satisfy the most stringent performance issues, regardless of the environment.

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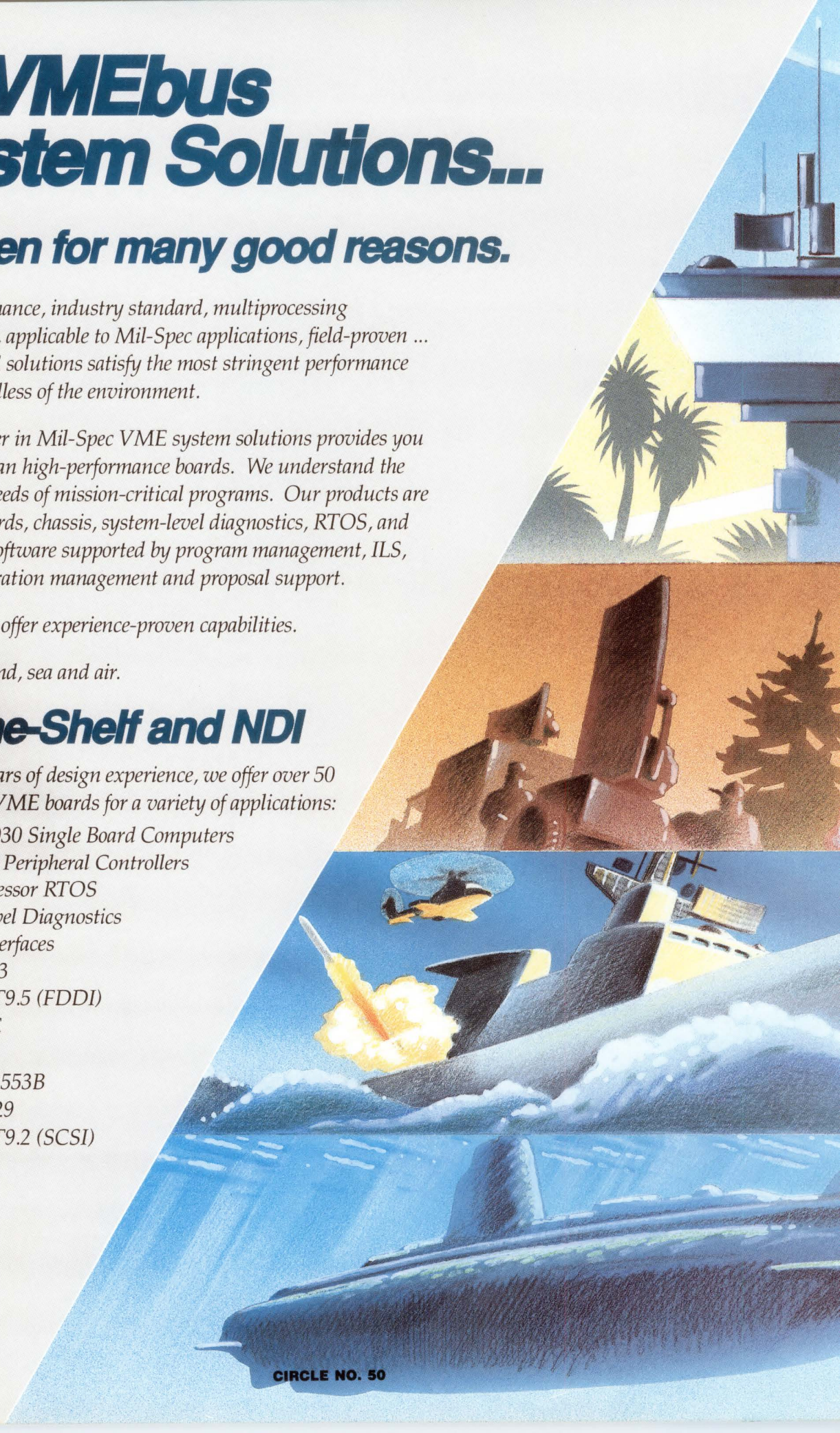
- *ANSI X3T9.5 (FDDI)*
- *SDC/DSC*
- *Graphics*
- *MIL-Std 1553B*
- *ARINC 429*
- *ANSI X3T9.2 (SCSI)*
- *Memory*
- *Chassis*



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Withstanding shock and vibration. *Our system solutions are working in helicopter navigational systems, navigational in-flight trainers, flight management systems and in-flight test and telemetry systems.*

ATC

High reliability in demanding situations. *DY-4 solutions are at work in radar data processing systems and display site equipment in major air-traffic control centers across North America.*

Ground Tactical

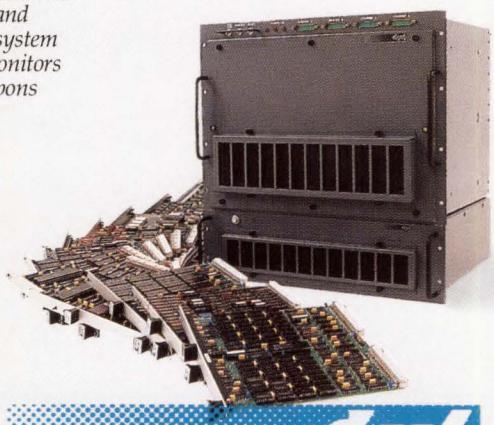
Field maintainable under the toughest conditions. *DY-4 has solutions applicable to fire control computers, tactical communications and display, system status monitors and weapons control.*

C^3I

When there's a need to know, DY-4 is there. *In naval plot data systems, naval tactical data systems, short-range air defense systems, electronic surveillance measures and ground and naval C^3 displays.*

Combat

When a timely response means survival. *From submarine combat systems to mobile X-ray units, DY-4 VME system solutions are meeting the challenge.*



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DY-4 Systems Inc.
21 Credit Union Way
Nepean, Ontario
Canada K2H 9G1

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FAX: (613) 596-0574
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Campbell, California (408) 377-9822
Los Angeles, California (714) 549-2559
Washington, D.C. (301) 964-5554
Boston, Massachusetts (617) 692-9308
Denmark (06) 96-3624
Ferranti Computer Systems, England 011 44 6333 71111

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CIRCLE NO. 50

Model	Platforms: Operating Systems	Printed Circuit Board CAD Interfaces	Component Libraries	ASIC Libraries	Options	Price
The Great Softwestern 207 Hickory St, Suite 202, Denton, TX 76201 (800) 231-6880						**Circle 293**
The Auto-Board System	MS-DOS	Futurenet, OrCAD, Schema	2,000+: CMOS, TTL, RCA, Intel, etc.	5+ lib.	sim., interface to Spice, PSpice, Berkley Spice	$750
United Silicon Structures (US2) 1971 Concourse Dr, San Jose, CA 95131 (408) 435-1366						**Circle 332**
Solo 1000/Solo 1200 (Draft)	Apollo: Aegis DEC: VMS DEC: VMS IBM PC/AT: DOS	—	350+ SSI/MSI: CMOS, TTL, I/O, pads, 7400 series, system cell	tool is tied directly to US2/ES2 silicon	part of integrated Solo IC generation tool	$22,500 (bundled only)
Valid Logic Systems 2820 Orchard Parkway, San Jose, CA 95134 (408) 432-9400						**Circle 334**
Entry Design System (ValidGED)	VAX, μVAX, 3000s: VMX; Sun 3,4: Unix; PCs: Unix, MS-DOS	12 interfaces	4,000+: TTL, ECL 30+ PLDs 60+ memories 100+ LSI/VLSI parts	97+ ASIC Design Kits	Validsim, -time, -flat, -packager, -compiler; simulator and ATE interfaces, hardware modeling, schematic flattener	$14,745 turnkey $8,800 sw
Vamp 6753 Selma Ave, Los Angeles, CA 90028 (213) 466-5533						**Circle 335**
Schematics V3.0	MacPlus, Macintosh SE & II	Calay, CV, Gerber, McCAD, Scicards	1,000+	—	digital and analog sim.	$495 sw only
Viewlogic Systems 275 Boston Post Rd W, Marlboro, MA 01752 (617) 480-0881						**Circle 337**
Workview	DEC VAX: VMS 286/386 compat.: DOS, native mode Sun: Unix	18 interfaces	3,000+ SSI/MSI: CMOS, TTL, ECL, PAL	California Devices, LSI Logic, Micro Linear, Standard Microsystems, Toshiba	sim., waveform analysis, document processor, terminal emulation, interfaces to PCB	$5,000 to $14,000 sw only
Visionics 343 Gibraltar Dr, Sunnyvale, CA 94089 (800) 553-1177						**Circle 338**
EE Designer	IBM PC/XT/AT, PS2: DOS	EE Designer (II, III)	500+: CMOS, TTL, analog	—	integrated w/logic simulation and PCB layout	$995
EE Designer II	same as above	same as above	1,000+: CMOS, TTL, SMD, analog	—	same as above	$1,895
EE Designer III	same as above	same as above	1,500+: CMOS, TTL, SMD, analog	—	integrated w/analog & sim., PCB layout, autorouting	$3,995
VLSI Technology 1109 Mckay Dr, San Jose, CA 95131 (408) 434-3100						**Circle 339**
Entry Express	Apollo, Sun, DEC, HP, Aegis, Unix, VMS	—	—	2-μm std. cell gate array 1.5-μm std. cell gate array	sim., test sw compilers, ASIC layout verification	$7,000 sw
Wintek 1801 South St, Lafayette, IN 47904 (800) 742-6809						**Circle 340**
HiWire-Plus	IBM PC/XT/AT, PS/2: DOS	Smartwork	950+: CMOS, TTL, ECL, μP, ladder, discrete, PCB: SIP, DIP, SMD, TO, PGA, Conn	—	—	$895 sw

Model	Platforms: Operating Systems	Schematic/Netlist Entry Supported	Minimum Grid Size	Design Rule Checking	Automatic Placement	Automatic Routing
Academi Systems 379 Earhart Way, Livermore, CA 94550 (415) 449-3294						**Circle 252**
Solution 6000	Micro PDP II (DEC) prop. graphics hierarchical file struct.	Case, Futurenet, Gerber Capture	1 mil	batch	region, gate & pin real-location, 2-sided	gridless, up to 20 layers simultaneous, regions, user-defin. parameter
Solution 8702	μVAX II CPU w/prop Graphics hierarchical filing	ASCII Data I/O, Gerber	var., fixed in. or metric, 2 mils	angles, clear-ance, gaps, open & short circuits w/ error marker	same as above	same as above
Accel Technologies 7358 Trade St, San Diego, CA 92121 (619) 695-2000						**Circle 253**
Tango-PCB	IBM PC: MS-DOS	Tango-Schematic, OrCAD, Schema	1 mil	connectivity check, batch	no	Tango-Route, Optional autorouter
Advanced Microcomputer Systems 2780 S W 14th St, Pompano Beach, FL 33069 (800) 9PC-FREE						**Circle 255**
PC-PRO	IBM PC/AT/XT, PS/2 (OS/2): DOS	Cell, OrCAD, Schema	1 mil	—	predefined placement in order of parts	Lee's Enhancement Algorithm
Aptos Systems 5274 Scotts Valley Dr, Suite 107, Scotts Valley, CA 95066 (408) 438-2199						**Circle 262**
Criterion II	IBM: DOS	Aptos, Cadnetix, Futurenet, P-CAD, OrCAD, Schema	1 mil	batch	no	bus maze strategy
RGraph	IBM: DOS	same as above	0.1 mil	batch	no	same as above
ASI Automated Systems 1505 Commerce Ave, Brookfield, WI 53005 (414) 784-6400						**Circle 264**
Prance	IBM Mainframe MVS & VM	—	1 mil	on-line batch, interactive	min crossing counts, min line lengths, thermal opt.	maze, layer pair true multilayer, rip-up & rerouted interactive
Automated Images 500 W Cummings Park, Woburn, MA 01801 (617) 933-1731						**Circle 263**
Personal 870	80286- & 80386-based PCs: MS-DOS/ PC-DOS	Applicon Automated Images	no min	batch spacing violation, report & graphical location ident.	placement aid using fast interactive rat's nesting & rubber-banding software	interactive on-line routing, interface to ASI Prance
Bishop Graphics CAD Systems 5388 Sterling Center Dr, Westlake Village, CA 91359 (818) 991-2600						**Circle 265**
Schematic Layout & Autorouting PCB Design Software	Macintosh and Macintosh SE & II	professional CAD/CAM schematic design & sim.	1 to 1,000 mils	intersilk online design rule checking	manual and corrective interactive parts place-ment	multilayer, maze
Cadam 1935 N Buena Vista St, Burbank, CA 91504 (818) 841-9470						**Circle 267**
Interactive Prance Cadam	IBM MVS, MUS XA & VM	Cadex and open arch. allows many netlists to be imported	as small as 1 mil	on-line, batch	prop. Automated Systems Inc. (ASI), Prance placement	multilayer, layer-pair, rip-up and retry, ASI Prance

Maximum Board Size, Layers, Components	Component Libraries	Surface-Mount Devices Supported?	Back Annotation Supported?	Options	Price
32.7 × 32.7 in., 64 layers, 2,000 IC equip., w/4 Mbytes of RAM	8,192 parts, 1,024 physical shapes	yes	no	schematics, gate, swap, Gerber Artwork input ASCII Data I/O, Digitize	$39,500 sw $62,500 integrated system
32.7 × 32.7 in., 64 layers, 2,000 IC equip.	same as above	yes	no	same as above	$43,500 sw $69,000 integrated system
32 × 19, 6 signal layers plus true power and ground planes, solder mask and silkscreen overlay	std., high density, SMD	yes	no	Tango-Route (autorouter), Tango-Tools (utilities)	$495
32 × 32 in., 255 layers, 5,000 nets	1,000+ parts: std. IC fam., DIP pkgs	yes	no	std. opts.: Gerber Photoplot	$250 sw only
64 × 64 in., 50 layers, 5,000 comp., 2,000 nets	1,200: CMOS, TTL, ECL, analog digital, SMD, μP	yes	yes	—	$1,500
same as above	same as above	yes	yes	—	$6,700
limitation is 1,000 × 1,000 grid size	1,000+ mechanical via AutoCAD; 5,000+ electrical all logic families	yes	yes	all AutoCAD thermal placement	lease-one-time fee of $41,000 plus $4,000 to 5,000/mo.
unlimited drawing file size, 16 layers, 32 × 32 in., 1 mil res; 64 × 64 in., 2 mil res. unlim. comp.	automated images	yes	—	full app. suite for schem., PCB, hybrids and masks, misc. outputs	$10,000 sw only; $16,500 EGA 386/ workstation; $20,000 high-res. 386/workstation
32 × 32, 24 signal layers, no limit of comp. or connect.	500+ parts: CMOS, TTL, analog connectors, discrete, PROMs, PLAs, user-definable custom built comp.	yes	no	autorouting, Gerber out, NC drill out	$700 schematic $1,500 PCB Layout $700 Autorouter $250 Gerber out $150 NC Drill out all software only
size is unlimited	1,200+: CMOS, TTL, ECL, discrete	yes	yes	thermal analysis component & board, HHB Cadat sim. Cadam 2-D, 3-D, solids	$60,000 to $250,000

Model	Platforms: Operating Systems	Schematic/Netlist Entry Supported	Minimum Grid Size	Design Rule Checking	Automatic Placement	Automatic Routing
CADdy 3401 Algonquin Rd, Suite 340, Rolling Meadows, IL 60008 (312) 394-7755 **Circle 268**						
CADdy Electronics	XT, AT, 386, PS/2, w/math co-proc.: MS-DOS	CADdy only	1 mil	batch in autorouters	—	orthogonal & maze, 2 layer, 16 layer and 24 layer rip-up
Cadnetix 5775 Flatiron Parkway, Boulder, CO 80301 (303) 444-8075 **Circle 269**						
CDX-56000SP	Sun-3: Unix	schematic entry/ design capt., EDIF, Scicards netlist format	up to 1μm	on-line, batch	constructive placement algorithm, gate and pin reallocation program, template placer	costed maze
Route Engine III-CDX-75000XP	prop. bit-slice accel.: microcoded software Unix	—	less than 1μm	on-line	—	100% rip-up and reroute, flex. field, true multilayer
Calay Systems 16842 Von Karman Ave, #100, Irvine, CA 92714 (714) 863-1700 **Circle 271**						
Prisma	Sun-3: Unix	Daisy, Futurenet, Mentor, Valid	1 mil	on-line DRC, and/or batch ERC	by comp, comp. type group all, gate and pin swap	rip-up and auto. reroute
Calos 3419 Edison Way, Fremont, CA 94538 (415) 657-4430 **Circle 272**						
Calos 6000-PCB	80286, 80386, PS/2: PC-DOS	Calos, Futurenet, OrCAD, Redac, Schema	1 mil	—	Matrix, comp. swap, auto. gate & pin swap, length min	Lee's costed maze, layer-pair, opt., rip-up and reroute, multilayer
Case Technology, Div. of Teradyne 2141 Landings Dr, Mt View, CA 94043 (415) 962-1440 **Circle 273**						
Vanguard Stellar PCB Design System	IBM PC/AT, PS/2 50, 60, 80: DOS; Sun-3: Unix; VAX, μVAX, 2000, VSII/GPX: VMS	CBDS, CV, EDIF, Futurenet, Mentor	1 mil	batch hierarchical	speeding algorithms min rat length, filtering by part, type and pincount var. grid	rip-up & reroute manufacturing clean-up
Computervision, Div. of Prime Computer 100 Crosby Dr, Bedford, MA 01730 (617) 275-1800 **Circle 274**						
Autoboard SMT	Sun-3: Unix Sun-4 SPARC CV version called CADDStation	schematic design; ELF, EDIF any ASCII netlist	no limits, 0.001 to 7 decimal places	on-line, batch	constructive initial placement, Steinberg algorithm, gate & pin swap, 2-sided	extended Lee for multilayer routing and for trace via repositioning
Daisy Systems 700 E. Middlefield Rd, Mountain View, CA 94039 (415) 960-6674 **Circle 276**						
Boardmaster	Personal Logician 386 and Logician 386: Daisy-Dnix, Unix μVAX II, VAX: VMS Sun-4: Unix autoroute	Ace, DED II (Daisy schematic editors)	1 mil "off-grid" increments	on-line batch, LVS, keepout areas	force directed; user-definable density, fixed placement; pairwise swaps; rat's nest display	signal & ECL prerouting; reentrant maze routing on 16 layers simultaneously
Dasoft Design Systems 1827-B Fifth St, Berkeley, CA 94710 (415) 486-0822 **Circle 277**						
Project: PCBC+	IBM PC/XT/AT, PS/2: DOS	included	20 mils	on-line	—	maze, modified Lee's, 5-segment memory router

Maximum Board Size, Layers, Components	Component Libraries	Surface-Mount Devices Supported?	Back Annotation Supported?	Options	Price
autorouter #1, 7×7 ft, EMS limit; autorouter #2, 31×31 in., EMS limit	1,000 incl. CMOS, TTL, analog, schematic and layout symbols	yes	yes	mechanical design Excelan NC Drill interface	$1,895 w/o autorouters and opts., incl., schematic pkg
34×48 in., multilayer, 24 signal layers, 10,000 comp., 100,000 connect., digital, analog, ECL, 2-sided SMT	3,000+ parts: CMOS, TTL, (mil & comm), ECL, CAD & CAE symbols	yes	yes	thermal analysis, tech pubs, sim., panel editor, ATE/CAM interfaces	$87,900 turnkey w/graphics accelerator (Sun)
same as above	—	yes	—	memory expansion	$89,900 hw accel.
32×32 ft, 256 layers, comp. not limit, connect. not limit	all	yes	yes	HHB sim. thermal analysis	—
32×32 in., 30 layers, 900 comp., 5,000 connect.	6,000+ parts: CMOS, TTL, ECL, SMD, analog	yes	yes	bidirectional, unidirectional	$2,825 sw only
IBM: 12 signal layers, 20×20 in., 16 Mbytes of memory, 1,000+ comp., 10,000 connect.; Sun & DEC: 20 signal layers, 32×32 in., 4,000 comp., 10,000 connect.	150+: CMOS, TTL, ECL, digital, analog	yes	yes	design rule checker, Gerber NC Drill, auto place & route, timing ver., digital & analog sim.	$5,500 IBM PC sw only $7,900 9500 Sun & DEC sw only
39×39 in., 20 signal layers, 10 power and ground	CMOS, TTL, ECL, SMD, analog	yes	yes	thermal analysis, electromechanical design	$34,000 for sw w/place, route
32×32 in., 255 layers (basic Boardmaster), 16 signal & 16 power (autorouter	2,500+ parts: CMOS, HCMOS, TTL, ECL, PLD, microprocessor, ASICs	yes	yes	star autorouter, 2-D drafting (MDP), NC drill & multiwire interfaces	$10,500 Boardmaster sw only $22,500 to 28,500 Boardmaster & autorouter sw only
32×32, 4 layers	Hitachi, Intel, CMOS, 74xxx/74LSxx (opt.)	yes	no	comp. libs., mfg-layout enhancement pkg, autoCAD interface, Gerber output	$1,500 sw

Model	Platforms: Operating Systems	Schematic/Netlist Entry Supported	Minimum Grid Size	Design Rule Checking	Automatic Placement	Automatic Routing
Design Computation Sherman Square, Route 33, Farmingdale, NJ 07727 (201) 938-6661 **Circle 278**						
DC/810	IBM PC & compat. w/hard disk & 640k: DOS	Design Computation EDIF, Futurenet, HP, OrCAD, Racal-Redac, Scicards (opt.)	1 mil	on-line, batch	avail. Q3 88	multilayer hugging
DC/CAD	same as above	same as above	1 mil	on-line, batch	avail. Q3 88	multilayer hugging
DC/810 II	same as above	same as above	1 mil	on-line, batch	avail. Q3 88	multilayer hugging
DC/CAD II	same as above	same as above	1 mil	on-line, batch	avail. Q3 88	multilayer hugging
DC/CAD II+	same as above	same as above	1 mil	on-line, batch	avail. Q3 88	multilayer hugging
Douglas Electronics 718 Marina Blvd, San Leandro, CA 94577 (415) 483-8770 **Circle 279**						
CAD/CAM Professional Layout	Macintosh Unix compat.	Douglas CAD/CAM prop. schematic	1 mil	no	no	maze, true multilayer (not pair)
ECAD 2455 Augustine Dr, Santa Clara, CA 95054 (408) 727-0264 **Circle 281**						
OmiCards, OmiRoute II	OmiCards, Sun, Apollo, GPX; OmiRoute II, Sun, Apollo, GPX, Mips, HP	Futurenet, Viewlogic	1 mil, 0.01 mm	on-line, batch	corrective placement, gate & pin reallocation program, 2 sided	maze, 16-layer simult., rip-up & retry, PC board & hybrid routers
EIE Electronic Industrial Equipment SA 15 rue Eugene-Marziano, CP 140, 1211 Geneva 24, Switzerland, (022) 423-260 **Circle 284**						
EIE Maestro, board designer PCB CIM pkg	DEC VAX, DECnet, PCs as workstations	EE Designer, Futurenet, P-CAD, EDIF	1 mil	on-line, batch, design and manufacturing rule checking	yes, with optimization by auto. swapping	maze, layerpair, plus user-defined algorithm
Harris Scientific Calculations 7796 Victor-Mendon Rd, PO Box H, Fishers, NY 14453 (716) 924-9303 **Circle 322**						
Scicards	VAX: VMS VAXStation II: GPX VAXStation 2000 SCX-20: Unix	Daisy, Mentor, Scidesign, Valid	0.001	on-line	auto-swap, gates, pins and comp., auto digital and analog, auto top & bottom SMD placement	channel, maze, cost-table flood and rip-up/reroute on up to 32 layers
Hewlett-Packard 1820 Embarcadero Rd, Palo Alto, CA 94303 (415) 857-1501 **Circle 295**						
HP Printed Circuit Design System	HP 9000 Series 300/800: HP-UX	HP Design Capture System, EDIF	1 mil	on-line, batch	constructive, force-directed, placement by device classification, 2-sided, rat's nest display	signal prerouting, maze, reentrant, 4-layer, 45-deg. routing, keepout zones
IBM 2077 Gateway Place, San Jose, CA 95110 (408) 288-4100 **Circle 297**						
CIEDS/Circuit Board Design System (CBDS)	IBM System/370: VM/CMS (9370, 43xx, 30xx); IBM RT PC: AIX	Lokl, CIEDS/Design Capture, other input formats	1 mil	on-line, real-time	algorithm based on logic length (least), auto. improve placement, pin swap, gate swap, 2-sided	costed maze, multilayer (up to 4 layers), and layer-pair
Interactive CAD Systems 2352 Rambo Ct, Santa Clara, CA 95054 (408) 970-0852 **Circle 304**						
ProCAD/ Proroute	IBM PC/AT: DOS VAX: VMS	Futurenet, OrCAD, Rat's nest	1 mil	on-line, batch	—	lookout, layer-pair

Maximum Board Size, Layers, Components	Component Libraries	Surface-Mount Devices Supported?	Back Annotation Supported?	Options	Price
8 × 10 in., 10 layers, 8 common	4,000: CMOS, LS, S, ALS, HC, HCT, memory, XCA linear	no	no	alien netlist converter	$1,395
32 × 32, 32 layers, 8 common place	same as above	no	no	same as above	$2,395
8 × 10 in., 10 layer, 8 common	same as above	yes	no	high-res. video, alien netlist converter	$1,995
32 × 32, 32 layer, 8 common	same as above	yes	no	same as above	$2,995
32 × 32, 32 layers, 8 common	same as above	yes	no	—	$3,495
32 × 32 in., unlimited multilayers, comp.limited only by memory	unlimited user-definable parts	yes	no	drall tape creator, Gerber file creator	$1,500 sw only
32 × 32 in., 32 layers, 3,000 comp. 12,000 connect., expandable	3,100+ parts: CMOS, TTL, SMD, analog	yes	yes	ASCII interface provided	$25,000 w/o router $40,000 w/router sw
65 × 65 in., 32 signal layers, 10,000 comp., 100,000 connect.	1,000 parts: additional parts under development	yes	yes	thermal analysis	$50,000 sw only
60 × 60 in., 32 layers, 2,500 comp., 150,000 connect.	user parts lib. 2,400 records: TTL, ECL, SMD	yes	yes	everything is incl. as std. part of product incl. drafting; thermal is an opt.	$25,00 sw
32 × 32 in., 99 circuit layers, 128 total layers, unlimited comp. & connect.	7,000+ parts: MOS, TTL, ECL, PLD, SMD, analog	yes	yes	—	$20,000 to $80,000 hw & sw
64 × 64 in., 99 conductor layers, unlimited comp. and connect.	10,000+ parts: CMOS, TTL, SMD, analog, connectors, DIPs, SIPs, ZIPs	yes	yes	interface to mechanical apps.: Catia, Cadam, Caeds	$22,000 sw (RT PC) $48,600 sw (S/370)
64 × 64 in., 40 signal layers, 5,000 connect.	1,000+ parts: CMOS, TTL, analog, PCB	yes	yes	—	$795 w/o autorouting $1,595 w/autorouting

Model	Platforms: Operating Systems	Schematic/Netlist Entry Supported	Minimum Grid Size	Design Rule Checking	Automatic Placement	Automatic Routing
Mentor Graphics 8500 S W Creekside Pl, Beaverton, OR 97005 (503) 626-7000 **Circle 308**						
Board Station	any Apollo color workstation	Mentor Graphics (others via netlisters)	0.01 metric μm	on-line, correct by construction	fully auto., mixed, constructive placement, interactive	global, rip-up-retry maze, shove-aside manufacturing
Omation 1210 E Campbell Rd, Richardson, TX 75081 (800) 553-9119 **Circle 314**						
Schema-PCB	IBM PC/AT 386, PS/2 and compat.	ASCII, Futurenet, Recal-Redac, Schema	1 mil	on-line and space check connectivity batch, net comparison	2-sided rat's nest, min connection length calculation autoplace based on placement matrix	3 heuristic, power/GND maze (9 pass) and rip-up/reroute opt.
OrCAD Systems 1049 SW Baseline St, Suite 500, Beaverton, OR 97123 (503) 640-5007 **Circle 315**						
OrCAD/PCB	IBM PC/XT/AT, PS/2 & compat.: DOS 2.0 or later	OrCAD/SDT	1 mil	on-line	—	maze, layer-pair
Personal CAD Systems 1290 Parkmoor Ave, San Jose, CA 95126 (408) 971-1300 **Circle 316**						
Master Designer	IBM PC/XT/AT and compat.: MS-DOS 2.0 or higher	ASCII netlist, Futurenet	1 mil, 0.01 mm	batch	constructive placement, placement improvement w/auto. gate and comp. swap, 2-sided	maze, layer-pair & multilayer, 45-deg. routing
PRO.LIB 624 E Evelyn Ave, Sunnyvale, CA 94086 (408) 732-1832 **Circle 318**						
AutoPCB	Apollo: Aegis PC/AT: DOS Sun-3: Unix	AutoSchema, Cadnetix, Calay, Case, CV, Futurenet, Intergraph, Mentor, P-CAD, Redac, Scicards, Valid	1 mil	batch	interactive only	costed maze, pattern recog., rip-up/reroute, simult. multilayer routing to 24 layers
Racal-Redac Westford Regency Park, 238 Littleton Rd, Westford, MA 01886 (617) 692-4900 **Circle 319**						
Visula PCB Designer	Apollo: Unix Sun-3: Unix VAX: VMS	Daisy, EDIF, Mentor, Redac (CADStar), Valid	0.001 μm	on-line, batch (manufact. and technology)	auto. gate/pin swap, 2-sided, auto. interactive template placement	multilayer, rip-up & reroute, push aside, gridless
Schlumberger CAD/CAM 4251 Plymouth Rd, PO Box 986, Ann Arbor, MI 48106 (313) 995-6000 **Circle 321**						
Bravo3 PCB layout	VAX: VMS	Bravo3 Design Capture, any other via user-config. netlist converter	1 mil	on-line, batch	multiple advanced algorithms incl. multiple trials, 2-sided, gate/pin allocation (based on Algorex)	multiple advanced algorithms incl. multilayer rip-up/reroute, (based on Algorex)
Shared Resources 3047 Orchard Parkway, San Jose, CA 95134 (408) 434-0444 **Circle 325**						
Koloa PCB Design System	Apollo: Aegis, Domain IX IBM: VM/CMS Sun-3: Unix	Aida, CAE, Case, CBDS, Daisy, Futurenet, Mentor, OrCAD, P-CAD	0.1 mil	on-line, batch	—	var. channel, multilayer, blind vias, transmission line
Crystal Router	same as above	same as above	0.1 mil	on-line, batch	—	var. channel, multilayer, blind, segmented, diagonal, buried via, diagonal routing, trans. line

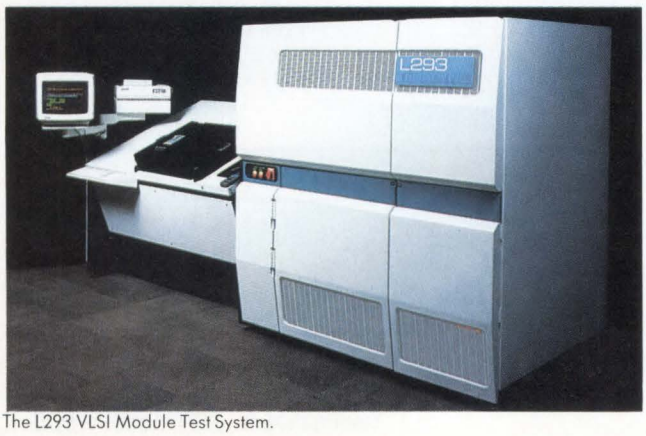
Maximum Board Size, Layers, Components	Component Libraries	Surface-Mount Devices Supported?	Back Annotation Supported?	Options	Price
40 × 40 meters, 256 layers, 32,000 comp., no limit to connect.	3,000+ parts: CMOS, TTL, ECL, PLD, μP, HCMOS, analog	yes	yes	thermal analysis, post-layout logic simulation	$45,000 sw
32 × 32 in., 30 signal layers, 450 comp.	2,000+ parts: CMOS, TTL, ECL, SMD, analog, mechanical VLSI	yes	yes	—	$975 PCB layout $850 autorouting
32 × 32 in., 16 signal layers, 130 comp. w/o EMS	—	yes	no	—	$1,495
60 × 60 in., 100 layers, 1,300 comp., 2,500 nets, 32,000 pins	4,000+ parts: CMOS, TTL, ECL, SMD, discrete, linear, memory, μP	yes	yes	CAM interface for board drilling & autoinsertion, ECO processing	$16,980 incl. extended warranty
60 × 60 in., 24 signal layers, 10,000 comp., 100,000 connect. (from-to's)	5,000 parts: CMOS, TTL, ECL, analog, micro(Intel) PALs	yes	yes	documentation incl. 3-D views w/AutoCAD	$1,995 to $4,295 DOS $7,500 Unix, Aegis
5 × 5 m, 250 electrical layers, 2,000 modes per tree, system limit on pins per comp.	4,000+ parts: CMOS, TTL, ECL, SMD, hybrid, LSI, VLSI, analog, discrete	yes	yes	MCAD, ECL, Hybrid, thermal analysis, sim., 2-D drafting, schematic capt., CAM	$30,000 to $100,000 sw
no board limits, 32 layers, no comp. limits	comprehensive generic lib.; ref. by Bravo3 Design Capt., analysis vendor-specific lib.	yes	yes	mechanical pkg, temp. and vibration analysis solids modeling, NC drill, photoplot, autoinsertion	$17,500
100 × 100 in., unlimited layers, 2,000 comp.	CMOS, TTL, ECL, SMD, analog, PGA	yes	yes	wirewrap, test fixture, drill tape	—
same as above	CMOS, TTL, ECL, SMD, analog, PGA	yes	yes	same as above	—

Model	Platforms: Operating Systems	Schematic/Netlist Entry Supported	Minimum Grid Size	Design Rule Checking	Automatic Placement	Automatic Routing
Silvar-Lisco 1080 Marsh Rd, Menlo Park, CA 94025 (415) 324-0700 **Circle 327**						
CAL-PC	Apollo: Aegis VAX: VMS Sun: Unix	Mentor, Silvar-Lisco schematic	1 mil	on-line, batch, user-definable	auto. place, 2-sided, auto. and interactive comp., placement by class	rip-up and reroute maze, prerouting
The Great Softwestern 207 W. Hickory, Suite 202, Denton, TX 76201 (808) 231-6880 **Circle 293**						
The Auto-Board System	MS-DOS	Futurenet, OrCAD, Schema	1 mil	batch	gate & pin, swapping, true interactive parts placement	prop., rip-up and reroute, layerpair, var. grids
The Auto-Board System 386 version	same as above	same as above	same as above	same as above	same as above	same as above
Valid Logic Systems 2820 Orchard Parkway, San Jose, CA 95134 (408) 432-9400 **Circle 334**						
Allegro PCB Design System	Sun-3, -4: Unix VAX GPX II & 3000 Series: VMS	Case, CV, Daisy, Futurenet, Redac, Scicards, Valid	sub-mil res.	on-line and batch DRC for auto. and interactive routing and placement	comp. floorplanning is driven from the Valid schem., auto. place. is complemented by gate/pin swap	expert, multilayer routing system consisting of costed maze, rip-up, and clean-up algorithms
Vamp 6753 Selma Ave, Los Angeles, CA 90028 (213) 466-5533 **Circle 335**						
PCB-1	MacPlus, Macintosh and Macintosh SE & II	one	1 mil	by default	manual	manual
PCB-ST	same as above	McCAD schematics, EDIF (Q4 88)	1 mil	by default	auto./manual	prop./gridless (maze opt.)
EDS-1	same as above	same as above	1 mil	by default	auto./manual	same as above
Visionics 343 Gibraltar Dr, Sunnyvale, CA 94089 (800) 553-1177 **Circle 338**						
EE Designer	IBM PC/XT/AT, PS/2: DOS	EE Designer, Futurenet, OrCAD, Schema	12.5 mils	batch	yes, algorithm min rat's nest trace length	multilayer, 25 or 50 mil basis, maze and channel
EE Designer II	same as above	same as above	5 mils	same as above	same as above	same as above
EE Designer III	same as above	same as above	1 mil	same as above	same as above	same as above
Wintek 1801 South St, Lafayette, IN 47904 (800) 742-6809 **Circle 340**						
Smartwork	IBM PC/AT/XT, PS/2: DOS	Futurenet, HiWire, OrCAD, Schema, Tango	50 mils	on-line, continual	—	Lee's (maze), layer-pair & single-layer rip-up and reroute
HiWire-Plus	same as above	HiWire-Plus	1 mil	utility program, your rules	—	—
Wire Graphics 95 Sherwood Ave, Farmingdale, NY 11735 (516) 293-1525 **Circle 341**						
Pen-entry PC	IBM PC/XT/AT or clones	interface to all schematic CAE databases is supported, Daisy, Futurenet Dash, OrCAD, Schema	—	wire-wrap wiring implementation ECL design rule observance	auto. placement via download of schematic netlist data, manual placement via lightpen or mouse	for wire-wrap in shortest path optimization; or x-y coordinate wiring

Maximum Board Size, Layers, Components	Component Libraries	Surface-Mount Devices Supported?	Back Annotation Supported?	Options	Price
32 × 32 in., signal layers, 8,000 nets, 1,000 comp., 20,000 pins	4,500 parts: CMOS, TTL, ECL, analog schematic capt., sim. models	yes	yes	sim., 2-D drafting	$47,000 incl. schematic entry sw
no limit, 16 signal layers	2,000+: CMOS, TTL, SMD, analog, RLA, Intel	yes	yes	Gerber photo plotting, $500 USD	$3,000/$3,500 sw
same as above	same as above	yes	yes	same as above	same as above
no limits to board size, pins, nets, comp.	4,000+: TTL, ECL, PLD, memories, LSI/VLSI logic parts, ASIC design kits	yes	yes	thermal & reliability analysis, multiwire interface	$20,000 interactive sw $30,000 auto. tools $40,000 and up turnkey
32 × 32 in., 9 layers, 10,000 elements per Mbyte of RAM	3,000+ footprints	yes	no	Gerber Translator, Gerber View	$395 sw only
32 × 32 in., 32 layers, 8,000 elements per Mbyte of RAM	3,000+ footprints plus user-definable	yes	no	Gerber Translator, Maze AutoRouter, Gerber View	$995 sw only
same as above	same as above	yes	no	Maze Router, Gerber View	$1,495 sw only
24 × 24 in., 26 layers, 1,000 comp.	1,000+: CMOS, TTL, analog	no	yes	autorouting netlist utilities additional lib.	$995
24 × 24 in., 26 layers, 1,000 comp.	1,000+: CMOS, TTL, analog, SMD	yes	yes	same as above	$1,895
32 × 32 in., 36 layers, 64,000 connect., 10,000 comp.	same as above	yes	yes	additional lib.	$3,995
10 × 16 in., 2 signal layers, no comp. restrictions, 4,000 connect. of autorouting	built-in commands	no	no	drill-tape utility photoplotter-driver	$495 w/o autorouter $895 w/autorouter sw only
60 × 60 in., 256 signal layers, no restrictions	800 schematic parts: 150+ SIP, DIP, SMD, TO, PGA, edged D connect.	yes	no	—	$895 sw only
42 × 42 in., wire-wrap, 1,000 comp.	yes, CMOS, TTL, ECL, SMD	yes	no	—	$5,995 sw

If you're testing complex boards,

You're facing one of test engineering's toughest challenges. VLSI boards like this one. But with a Teradyne L200 board tester on your side, complex test problems can be conquered quickly.



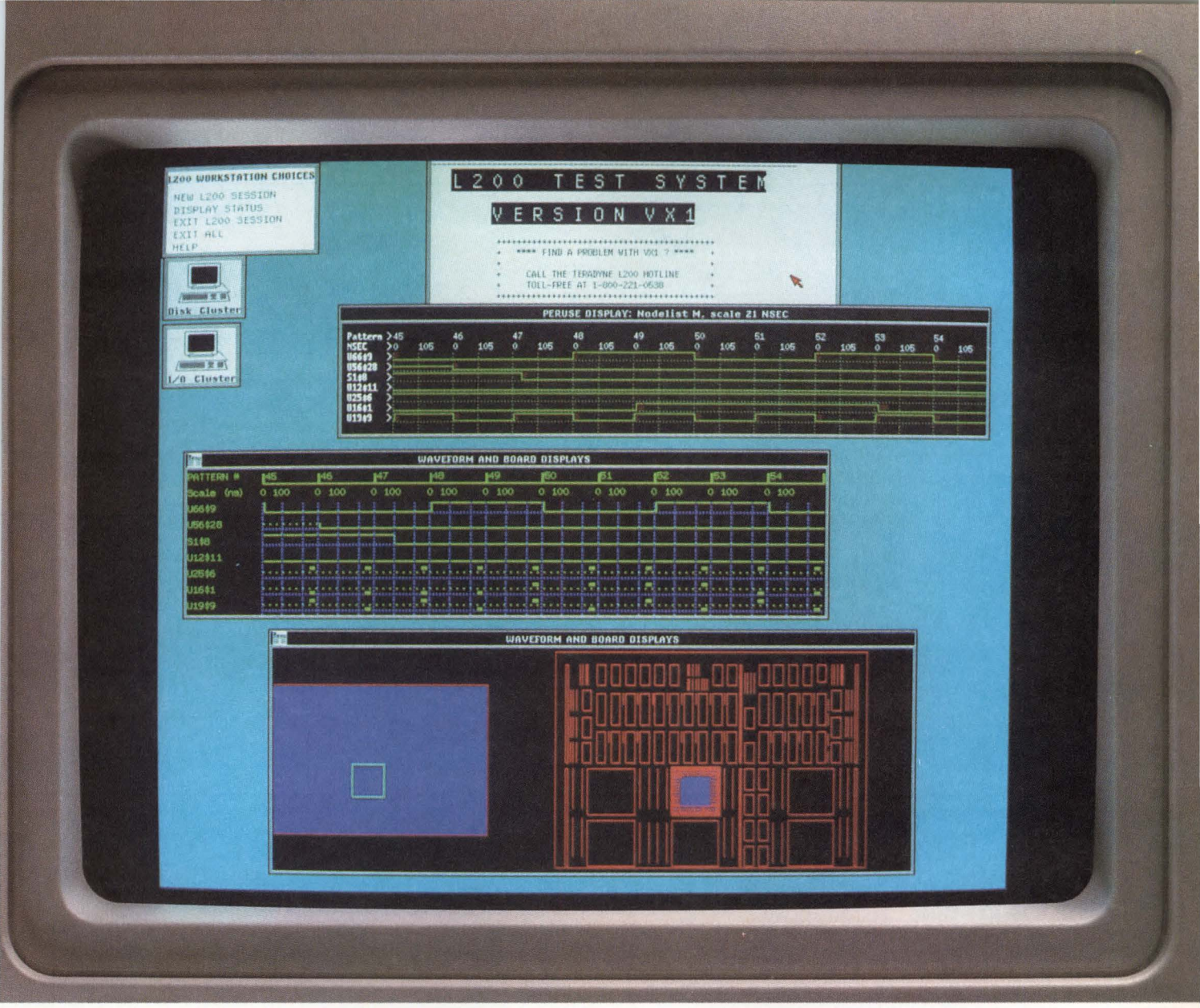
The L293 VLSI Module Test System.

Stay in front of VLSI/VHSIC advances.
Start with the most advanced hardware for analog and digital testing. An L200 fires functional test patterns at 40 MHz rates. At up to 1152 test channels. Top speed is 80 MHz. That's 4 to 8 times faster than any competitor can deliver.

And the L200 hits test signal timing precisely. With up to 32 timing sets for drive phases and test windows. Its 250 ps programming resolution with zero dead time puts signal edges right where you want them.

Divide and conquer.
VLSI/VHSIC boards demand large, complex test programs. But the L200's distributed computer architecture simplifies matters.

Testing is controlled by a VAX computer. It sends tasks to specialized processors for rapid deployment of analog, digital, and memory tests.



here's a simple plan of attack.

Programmers will appreciate clustered VAX workstations. Graphics, like waveforms and shmoo plots, make heavy debug and analysis light work.

Simulation and other tactics.

High-powered software tools tailor L200 test development to modern design techniques and test strategies. Precisely the caliber of tools you need to get tests up and running fast.

	Test Channels	Maximum Pattern Rate	Channel Skew
L297	1152	80 MHz	±1.5 ns
L293	576	80 MHz	±1.5 ns
L280vx	1152	10 MHz	±10 ns
L210vx	576	10 MHz	±10 ns

Take our LASAR simulator. It works closely with the L200 for both cluster and board-level testing. LASAR accurately predicts VLSI circuit responses and reports test program fault coverage.

Significantly, LASAR simulates L200 characteristics. So test programs automatically include when to test board responses. And what response is expected. The result is uncompromising go/no go tests as well as precise guided probe or fault dictionary diagnosis.

A powerful ally.

L200's have proven themselves under fire at hundreds of advanced manufacturing sites worldwide. So if you're about to take on a new VLSI/VHSIC project, find out how to launch a winning test strategy. Call Daryl Layzer at (617) 482-2700, Ext. 2808 without delay.

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CIRCLE NO. 38

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
Aida 5155 Old Ironsides Dr, Santa Clara, CA 95054 (408) 980-5200							**Circle 256**
Aida Logic Simulator	Apollo: Aegis, Unix Sun-3: Unix	Case Vanguard, Aida design language	gate, behavioral, Mentor, Tegas and Hilo files	0, I, X, Z	C	—	Aida Cosimulator processor
Aldec-Automated Logic Design 3525 Old Conejo Rd, #111, Newbury Park, CA 91320 (805) 499-6867							**Circle 257**
Susie-3	PC/XT/AT	any netlist: Futurenet, P-CAD, OrCAD, Schema	12 integrated input signals	0, I, Z active, passive	Mobie expert system (opt.)	—	—
Susie-4	PC/XT/AT	same as above	12 has input signal integrators	same as above	same as above	—	—
Susie-5	PC/XT/AT, 386 PC	same as above	12 has signal integrators	same as above	same as above	—	—
Fast-Guide	PC/XT/AT: PC-DOS	Aldec	12	0, I, Z, active, passive, unknown	Mobie expert system	—	—
Altera 3525 Monroe St, Santa Clara, CA 95051 (408) 984-2800							**Circle 258**
PLFSIM	IBM XT/AT	Jedec file	—	—	—	—	—
Analog Design Tools 1080 East Arques Ave, Sunnyvale, CA 94086 (800) ANA-LOG4							**Circle 259**
Spice 2G.6 and Spice Plus	Apollo: Aegis; H-P: HP/UX; Compaq, IBM PC/AT, Sun: Unix	Analog and PC workbenches, Circuit Editor	transistor and funct.	analog sim.	—	—	—
Saber	Sun and Apollo	same as above	behavioral, transistor, funct.	analog sim.	Mast	—	—
Pacsim	same as above	same as above	transistor and funct.	analog sim.	—	—	—
Analogy PO Box 1669, Beaverton, OR 97075 (503) 626-9700							**Circle 260**
Saber	Alliant: Unix Apollo: Aegis Sun: Unix VAX: VMS	Spice 2G.6 netlist, Analog Design Tools, Cadnetix, CV, Racal-Redac, Viewlogic, Mast	behavioral, funct., and primitive analog	can model digital devices with states and events	Mast, subroutines in C, Fortran, Pascal	—	Alliant, Sun-4
Vanguard Stellar CAE Design System	IBM PC/AT, PS/2, 50, 60, 80: DOS; Sun-3: Unix; VAX, μVAX 2000, VSII/6PX: VMS	Case Schematic Editor, prop., CSDF, EDIF 2.0	behavioral, gate, mixed switch	0, I, X, Z	models in C, Aida design system	—	Aida Cosimulator family prop.
Bishop Graphics CAD Systems 5388 Sterling Center Dr, Westlake Village, CA 91359 (818) 991-2600							**Circle 265**
Professional CAD/CAM schematic capt. and sim.	Macintosh, Macintosh SE & II	prop. schematic capt.	gate	0, I, Z	user-define	—	—

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
Aida System Timing Verifier	—	Aida, fault simulator	generic	CMOS, TTL	LSI Logic, Toshiba, ICs	Aida Cosimulator, Aida ATPG accel.	$80,000
—	—	APFS (Aldec), runs on parallel PCs	Daisy, Teradyne	3,500+: CMOS, TTL, ECL, PLD, MPUs, memories	Fujitsu	TIM: .01 ns interactive simulator	$495
TIM-4/.01 ns interactive	—	same as above	same as above	same as above	Fujitsu	same as above	$995
TIM-5/.01 ns interactive	—	same as above	same as above	same as above	Fujitsu	same as above	$1,995
TIM	—	—	accepts logic analyzer data as input test vector	CMOS, TTL, ECL	verifies any ASIC using logic analyzer captured I/O signals	guides hardware debugging from schematic	$1,995 educational, sw
—	—	yes	Data I/O	7400 series, TTL	—	—	$750 sw
—	Spice 2G.6 and Spice Plus prop.	—	—	sample device lib., general device lib., basic device lib.	Datalinear, Linear Lib., Microlinear, National, Plessey, VTC	advanced analysis tools, statistics, parametric plotting	$8,000 PC Workbench; $14,000 Analog Workbench
—	Saber, OEM agree.	—	—	same as above	—	same as above	$15,000 to $20,000 sw
—	Pacsim, OEM agree.	—	—	—	—	same as above	—
—	Saber	real-time failure, effects modeling	—	560 std. comp., 100 templates, std. spice models	—	spectral analysis, time domain modeling	$15,000 sw
setup/hold, rise/fall, min/max delay	Atap prop.	fault simulator prop.	Teradyne	—	1500+TTL, LSI, NEC, Toshiba	Mentor interface, logic design rule checker, static timing analyzer, and others	$100,000 sw
setup/hold, rise/fall, min/max delay	—	—	—	500+ CMOS, TTL	user-definable	—	$700 sw

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
CAD Group 3911 Portola Dr, Santa Cruz, CA 95062 (408) 475-5800							**Circle 266**
Salt	Apollo: Aegis, Domain IX; DEC VAX: Unix, VMS; IBM PC/AT: DOS; Sun: Unix	Scientific Calculations capt.	mixed behavioral, funct., gate, macro, switch, system	0, I, H, L, Z, W, X, active, passive, indeterminate	SHDL	—	sclip accel., (5-Mips Clipper 3rd party-runs Salt on PC/AT)
Cadam 1935 N Buena Vista St, Burbank, CA 91504 (818) 841-9470							**Circle 267**
Cadam Cadat Digital Sim.	IBM mainframe: VM, MVS	integrated with Cadam Cadex	gate level w/ hierarchical definition	active, passive	Cadat language is generated auto. from a schematic	—	no, but runs in mainframe background
Cadnetix 5775 Flatiron Parkway, Boulder, CO 80301 (303) 444-8075							**Circle 269**
CDX-9510, -9610, -9640 turnkey CDX-8110 software	Sun-3, -4: Unix	schematic entry/ design capt., prop. software, EDIF 2.0	behavioral, gate, physical, switch	0, I, X, Z, active, passive, floating, indeterminate	behavioral modeling	CDX-7950	CDX-770, (200k eval/s)
Calos 3419 Edison Way, Fremont, CA 94538 (415) 657-4430							**Circle 272**
Calos 6000	IBM AT, 386: DOS Sun: Unix	netlist Calos 6000 schematics fully integrated	switch, gate, funct., behavioral and hardware	21 states, 3 strengths	BDL and C	Cats	Mark 1000 accelerator
Computervision, Div. of Prime Computer, 100 Crosby Dr, Bedford, MA 01730 (617) 275-1800							**Circle 274**
Cadat	all CADDStation	CV shematic design CADDS4X	behavioral, gate, primitive	0, 1, X, active, passive, float, indeterminate	MDL, BML, RDL and schematic design model input	Cats modeler	Cats accel., Lana Cadat, third party
Saber	same as above	same as above	behavioral, comp., inner-switch	phase, magnitude, DB, real, imaginary	Mast	—	—
Dynamic Timing Verify	same as above	same as above	comp., primitive	0, I, unknown, stable/change, rise/fall	graphical (schematic design)	—	—
Control Data 2800 Old Shakopee Rd, Box 0, Minneapolis, MN 55440 (612) 853-3117							**Circle 275**
Midas	CDC Cyber	Apollo, Mentor/Daisy schematic capt., logic interconnect lang. prop.	macro, mixed, timing	0, I, X, Z tristate	prop.	—	Zycad
Daisy Systems 700 E. Middlefield Rd, Mountain View, CA 94039 (415) 960-6674							**Circle 276**
VSS (Verification Support System)	Personal Logician 386, Logician 386: Daisy-Dnix; Sun 386, Compaq DeskPro 386, IBM PC/AT: Daisy-Dnix	Ace, Ded II, Daisy schematic editors	mixed: behavioral, funct., gate, physical, switch	0, I, unknown, forcing, resistive, high Z, indeterminate	DABL, (behavioral), DML	PMX (Physical Modeling Extension)	Megalogician, Personal Megalogician, 100k eval/s

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
setup/hold, rise/fall, min/max delay	Salt A/D (prop.), A/D mixed-mode sim.	DTA, DFS	Sentry	1,500+ SSI/ MSI/LSI/VLSI: CMOS, TTL, ECL, PAL, 100+generic behavioral	LSI Logic	translators for other simulator pkgs, time-sharing Salt on supercomputers	$3,500 sw, IBM PC; $15,000 sw, Apollo, μVAX, Sun; $20,000 sw, IBM PC w/5 Mips hw; $60,000 sw, supercomputer
worst case and nominal delay	—	single and concurrent fault	no interfaces are sold w/ product	user-definable, Cadat supplied, approx 1,800 comp.	Cadat supplied	—	$97,500
funct., worst case, set-up/hold, rise/fall, pulse width	CDX-9630 turnkey CDX-8130 sw only	CDX-8120	Factron, Genrad, Zehntel	3,000+: CMOS, TTL, ECL, analog, PAL, PLD, μP	15+ ASIC design kits	Sun-4 workstations and servers for accel. A/D compilation and sim.	$26,700 sw (Sun) $42,900 turnkey $19,700 sw (Sun) $32,900 turnkey
setup/hold, min/pulses, width change	PSpice, 3rd party	Cadat, 3rd party concurrent	Eaton, Factor, Sentry	3,000+ SSI/ MSI: CMOS, TTL, ECL, 150 models	7 lib.	hardware modeling	$3,000
worst case, rise/fall, delay, loading	—	concurrent fault OEM-HHB Systems	TSSI links Factron, Teradyne	3,500+ SSI/ MSI: CMOS, TTL, ECL, μP SMD, memory,	7+ ASIC libraries	logic design, logic design w/fault analog designer	—
ac, dc, transient, noise distortion	OEM-Analogy	—	—	500+analog diodes, transistors, op amps, MOSFETs	—	—	—
race conditions static/dynamic hazards, setup/hold, min pulse width recon fanout	—	—	—	3,500+ SSI/ MSI: CMOS, TTL, ECL, μP SMD, memory,	—	part of schematic capt. system	free with schematic design system
path trace, min/max delay, setup/hold	Spice, stand alone	Stafan, Zycad FE	neutral test file	MSI/SSI, TTL	VLSI 6000, 7118, 5000, CMOS	—	—
DTV: min/max, min/nom, nom/max, setup/hold, min pulse width, rise/fall	DSpice/ virtual lab prop.	Megafault prop./concurrent	IMS, Sentry	4,500+ digital: CMOS, HCMOS, TTL, ECL, PLD, RAM, ROM, μP/; 1,300+ analog: discrete, ICs, converter, power device	170+ ASIC design kits	PMX, DSpice/ Virtual lab, Megafault, Megalogician	$15,000 sw $40,000 turnkey

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
Douglas Electronics 718 Marina Blvd, San Leandro, CA 94577 (415) 483-8770							**Circle 279**
Douglas CAD/CAM Schematic Designer	Apple, Macintosh, Unix compat.	prop. Schematic, (Douglas CAD/CAM)	gate level w/ timing	O, I, X, Z active, passive, unknown and combinations	—	—	—
E/Z CAD 5589 Starcrest Dr, San Jose, CA 95123 (408) 972-0782							**Circle 280**
Plogic	IBM PC/XT/AT, PS/2: MS-DOS 2.1 and above	OrCAD SDT and Omation's Schema	FF, gate, mixed switch	O, I, indeterminate, active, passive, HI-Z	prop.	—	—
ECAD 2455 Augustine Dr, Santa Clara, CA 95054 (408) 727-0264							**Circle 281**
Simon	Apollo: Aegis; Sun-3, -4: Unix; VAX: VMS, Ultrix; MIPS	netlists, Hspice, Spice	circuit level	continuous voltage, current	std. Spice	—	—
Ella	Apollo, Sun, VAX: VMS, Ultrix	Ella language, Mentor	behavioral, mixed gate	user-defined	Ella	—	—
EEsof 5795 Lindero Canyon Rd, Westlake Village, CA 91362 (818) 991-7530							**Circle 282**
Microwave Spice	MS-DOS, Aegis, VMS, HP-UX	netlist, schematic capt.	rf/microwave nonlinear time domain	active, passive, rf/microwave circuits	—	—	—
Libra	same as above	same as above	rf/microwave linear, nonlinear, frequency domain	same as above	—	—	—
Touchstone	same as above	same as above	rf/microwave linear, freq. domain	same as above	—	—	—
Electrical Engineering Software 4675 Stevens Creek Blvd, Suite 101, Santa Clara, CA 95051 (408) 296-8151							**Circle 283**
Precise	Apollo: Aegis Sun-3, -4, VAX, VMS, Unix, IBM, Cray	Mentor, Racal-Redac, Valid, Viewlogic, Spice compat., netlist input	analog circuit, behavioral funct.	—	—	—	—
Endot 11001 Cedar Ave, Suite 500, Cleveland, OH 44106 (216) 229-8900							**Circle 286**
N, 2	Apollo: Aegis; Sun-3, -4: Unix; VAX, μVAX: VMS, Unix	Mentor, Valid	mixed system: queuing, architectural, funct., RTL, gate	O, I, X, Z	ISP, VHDL 1076 (Q4 88)	—	—
Epic 3080 Olcott St, Suite 203-B, Santa Clara, CA 95051 (408) 988-2944							**Circle 287**
Timemill	Sun, Apollo, Valid, μVAX, HP, DEC, PC/AT: Unix, Domain IX, VMX, Ultrix, MS-DOS	prop. can translate from Spice, Verilog, Silos, Hilo, Tegas	mixed-level, behavior/funct., register transfer, logic gate, trans. switch	3 states O, I, U, continuous strength	C	—	—

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
setup/hold, min/max delay	–	–	–	500+: CMOS, TTL, PAL, PROM, ECL in future	–	PLD compiler	$700 sw
rise/fall	–	–	–	1,000+ SSI/MSI: CMOS, TTL, AS/ALS, HC/HCT	–	–	$495 complete sw w/lib. and graphics
stimulus-dependent rise/fall	Simon prop.	–	–	std. Spice elements	–	–	$16,000 sw
–	prop. Analog Modeling	–	–	user-defined	user-defined	–	$20,000 sw
rise/fall delay	Spice prop.	–	–	GaAs FET	–	–	$8,400
–	Harmonic Balance prop.	–	–	GaAs FET	–	Triquint Lib.	$23,500
–	Spara-meter prop.	–	–	GaAs FET	–	Triquint lib.	$9,900
–	Precise	–	–	750 analog op amps, comp., transistors, diodes, FETs	–	–	$9,500 to $70,000
–	–	–	–	some μP, std. ISA, bus interfaces	–	Mentor interface, VHDL 1076 output, VHDL 1076 sim (Q4 88)	–
Timemill timing sim., ver., critical path analysis	–	–	Sentry	generic random logic CMOS, ECL, FF, RAM, ROM, PLA, FSM, MSI	LSI Logic 7000 series HCMOS, Raytheon CMOS, ECL	–	$20,000

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
ESP 18013-C Skypark Circle, Irvine, CA 92714 (714) 261-1777							**Circle 285**
VSpice	PC: DOS VAX: VMS	Spice std., via Lognet capt.	analog	—	—	—	—
Europe Silicon Structures Hollybank House, Mount Ln, Bracknell, Berks, RG12 3DY United Kingdom 034 452-5252							**Circle 288**
Solo 1000/Solo 1200 (exert)	Apollo: Aegis DEC: VMS IBM PC/AT: DOS Sun: Unix	Case, Daisy, HDL netlist schematic, Mentor	RC level	O, L, X, Z driven, charged, glitches	HDL	—	—
Gateway Design Automation PO Box 573, Westford, MA 01886 (617) 692-9400							**Circle 290**
Verilog, Verilog-XL	Apollo: Aegis; IBM: VM/CMS; Silicon Graphics, Masscomp, Elxsi, Sun: Unix; VAX: VMS	interfaces to Caeco, Daisy, Mentor, SDA, TDL, Valid, Verilog HDL	complete mixed-level behavioral, funct., gate, switch	120 internal states	Verilog HDL	—	Verilog-XL software acceleration
GE Solid State Rte 202, Somerville, NJ 08876 (201) 685-6000							**Circle 291**
Mimic	Apollo: Aegis IBM: VM Sun: Unix VAX: VMX	Daisy, Futurenet, Mentor, P-CAD, Valid	behavioral, funct., gate, switch	15 states and 32k resistive depths	VHDL, C, Pascal, Fortran, PL1	—	—
Genrad 510 Cottonwood Dr, Milpitas, CA 95035 (408) 432-1000							**Circle 292**
System Hilo	Apollo: Aegis, Unix; DEC: VAX/VMS/Ultrix	Case, CV, Daisy, Futurenet, and others	integrated switch, gate, behavioral	1, 0, X, Z, plus 10 internal ambiguity states and stored charge levels	GHDL	Hichip physical modeling system	Zycad interface supplied by Zycad
Harris Scientific Calculations 7796 Victor-Mendon Rd, PO Box H, Fishers, NY 14453 (716) 924-9303							**Circle 322**
Cadat	Sun: Unix VAX: VMS	SciDesign, schematic capt., EDIF 2.0	behavioral, funct., gate, hardware, switch	I, O, X, active, passive, floating, 21 states	behavioral design	Cats modeler	Cats accelerator
Hewlett-Packard 1820 Embarcadero Rd, Palo Alto, CA 94303 (415) 857-1501							**Circle 295**
Hilo-3	HP 9000, 300/800: HPUX	HP design capt. system, HP PLD design system, EDIF 200	behavioral, gate, funct.,	O, I, X, Z, strengths (strong and weak)	funct. modeling language	Hichip	—

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
—	Spice	—	—	var. lib. avail.	—	—	$800 PC $10,000 VAX
setup/hold, timing diagrams, min/max delay	prop.	prop. statistical	Sentry	350+ SSI/MSI: CMOS, TTL, I/O pads, 7400 series, system cell	tied directly to US2/ES2	part of integrated Solo IC generation tool	$22,500 bundled
timing checks	—	testgrade, testgrade A, concurrent, prop.	through TSSI	SSI/MSI, TTL, logic auto., Quadtree for VLSI	—	—	$25,000 sw
setup/hold, rise/fall, min/max delay	—	mimic fault, simulator, prop.-GE	Sentry, Teradyne, Trillium	—	GE, LSI Logic, VLSI	—	$15,000 (Apollo, Sun) $25,000 (IBM, VAX) sw
setup/hold, rise/fall delays, min/max delay	—	Hifault, prop., PVL algorithm	Genrad and others	6,000+ SSI/MSI/LSI: CMOS, TTL, ECL, PLD	20+ lib.	Hitest test generation systems, Higen ASIC library generation	$10,000 sw base
setup/hold, min pulse width, worst case, min/max	Spice	concurrent fault sim.	Genrad, Teradyne, TSSI chip-tester, Vectron	4,000+ SSI/MSI: CMOS, TTL, ECL, PAL	4,000+ ASIC lib.	accel., modeler, ATG, PAL generator model, hardware modeler toolkit	approx. $30,000 sw
min/max/nom, worst-case, setup/hold, violations	analog workbench	parallel value list algorithm, prop. OEM	HP 3065 board test system, Genrad GR16, GR18, 227X series	5,000+ MOS, TTL, ECL, μP, PLD, 2,000+ analog, R, L, C, and analog ICs	10+ ASIC design kits	Hichip, Hilo fault	$5,000 to $50,000 sw

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
HHB Systems 1000 Wyckoff Ave, Mahwah, NJ 07450 (201) 848-8000							**Circle 296**
Cadat	Apollo: Aegis, Unix; DEC VAX, μVAX: VMS, μVMS; Sun-3, -4: Unix	CV, Futurenet, Mentor, EDIF 2.0	multilevel behavioral, funct., gate, switch	O, I, X, active, passive, floating, indeterminated	BDL, C	Cats hardware modeler	Cats accel. 300X the performance of a VAX 11/780
Silos	Apollo: Aegis; DEC VAX: VMS, VAX, Unix 4.2; IBM: MVS and others	Case, Futurenet, Xilinx	mixed behavioral, funct., gate, switch	12 + 5 logic states, high, low, unknown supply, driving, resistive	SBL, C, funct.	–	–
Pacsim	Alliant: Unix Apollo: Aegis and others	Spice I/O compat., analog workbench, MSpice	circuit	–	Spice netlist with enhancements, prop., C program. environ.	–	multi-processors (Alliant, Sequent, prop. Simucad SX system)
IBM 2077 Gateway Place, San Jose, CA 95110 (408) 288-4100							**Circle 297**
CIEDS/behavioral simulator	IBM System 370: VM/CMS IBM RT, PC: AIX	CIEDS/design capt., SDL inputs	behavioral	user-defined	HHDL	–	–
CIEDS/logic simulator	same as above	same as above	gate	O, 1, H, Z, unknown	models supplied	–	–
CIEDS/analog-digital simulator	same as above	same as above	mixed-mode	analog outputs	models supplied	–	–
CIEDS/switched capacitor simulator	same as above	same as above	time and freq. domain, sensitivity analysis of switched capacitor circuits	analog outputs	models supplied	–	–
IC Designs 12020 113th Ave NE, Kirkland, WA 98034 (206) 821-9202							**Circle 298**
QSim interactive logic simulator	IBM PC/AT: MS-DOS	Desedit (IC designs prop.), OrCAD/SDT	switch-level logic simulator (no timing)	3 states:, 1, O, and X	–	–	–
QRNL	same as above	same as above	switch-level event-driven logic simulator	–	–	–	–
Ikos Systems 145 N Wolfe Rd, Sunnyvale, CA 94086 (408) 245-1900							**Circle 300**
Ikos simulation system	Apollo: Aegis IBM PC/AT: DOS Sun-3: Unix	translators for Case, Daisy, Futurenet, Mentor, P-CAD, Valid	gates level, mixed switch	O, 1, X, N, high Z, resistive, driving, hard driving	–	–	Ikos 800, 1900
Intergraph One Madison Industrial Park, Huntsville, AL 35807 (205) 772-2000							**Circle 305**
Hilo-3	Intergraph Interpro, Interact: Unix	design engineer, prop. schematic capt.	funct., mixed gate	5 logic states, 15 logic values	HDL	Hichip	5-Mips Clipper engine

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
setup/hold, min pulse width, rise/fall, min/typ/max, load dependent delays	—	Cadat fault sim. prop., concurrent	Genrad, Teradyne, TSSI	SSI/MSI: TTL, ECL, PAL library elements	—	Cats hardware modeler, Cats accel.	$20,000
setup/hold, rise/fall, min/max delay	—	Silos integrated statistical and concurrent fault sim.	Sentry	TTL, ECL	—	—	$995 PC $20,000 workstation
—	Pacsim	—	—	supported through Contour	—	user modeling opt., waveform analysis pkg	$20,000 workstation
setup/hold, pulse width, clock freq.	interface to Spice 2G simulators	—	—	2,500+: TTL comp., discrete devices	—	supports hierarchical designs and user-created behavioral models	$75,000 sw s/370 $20,000 sw RT PC
same as above	same as above	—	—	2,500+: TTL comp.	—	optimized comp. models for fast sim.	$50,700 sw s/370 $13,500 sw RT PC
—	mixed mode supported, interface to Spice 2G simulators	—	-	60+ analog and digital primitives	—	linear approx., for nonlinear devices	$45,000 sw s/370 $12,000 sw RT PC
—	piecewise-linear approx. of nonlinear devices to perform analog sim.	—	—	12 analog primitives	—	multiple analysis modes to solve switched capacitor design problems	$37,500 sw s/370 $10,000 sw RT PC
QTim interactive timing ver.	—	—	IMS	—	IC Designs, 2-μm CMOS, std. cell lib.	—	$10,000 bundled
QTim	—	—	IMS	—	same as above	—	$10,000 bundled
50-ps lib. res.	—	prop., high-speed serial, incl. w/base system	generic output, user formatable	TTL, ECL	40+ ASIC libr.	16,000 evaluator boards netlist translators, ASIC libraries, memory	$46,500 base system for PC/AT platform
setup/hold, rise/fall, min/typ/max delay, min pulse width	Cspice prop.	Hilo fault simulator	Genrad Hilo	3,000+ SSI/MSI: CMOS, TTL, ECL	5	fault simulator ATG, Hichip	$5,000 sw

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
Integrated Silicon Design Pty Ltd PO Box 99, Rundle, 230 North Terrace, S Australia, 5000, Australia +61 82 23 5802							**Circle 301**
USA	Apollo: Aegis; HP 9000: HP/UX; IBM PC/AT: MS-DOS, Xenix; Sun: Unix; VAX: VMX, VMS	Modula 2	functional	–	ISDL	NIL	–
Probe	same as above	Spice or internal format from extractor	circuit	–	internal	–	–
Intel 3065 Bowers Ave, Santa Clara, CA 95051 (408) 765-8080							**Circle 303**
Intel's Design Environment	Daisy: Dnix Mentor: Aegis VAX: VMS	Daisy, Mentor	behavioral, gate, physical	O, I, X, Z active, passive, indeterminate	–	Zycad	1M events/s
LSI Logic 1551 McCarthy Blvd, Milpitas, CA 95035 (408) 433-8000							**Circle 306**
Silicon Integration	IBM: VM/CMS Sun: Domain IX Sun-3, -4: Unix VAX, μVAX: VMS	LSED-prop. schematic capt., NDL netlist format translator	gate	O, 1, X, Z, 3 strengths	NDL	–	Zycad interface (opt.)
System Integrator	same as above	same as above	behavioral, gate	same as above	NDL, BSL	–	same as above
Matra Design Semiconductor 2895 Northwestern Pkwy, Santa Clara, CA 95051 (408) 986-9000							**Circle 307**
Gateaid Plus/PC	IBM PC/XT/AT, PS/2, OS/2, 386: DOS	modified OrCAD/SDT	gate-level: funct. and timing	strengths: forcing, resistive, high impedance, spike, 5 levels	Boolean equations	–	–
Mentor Graphics 8500 S W Creekside Pl, Beaverton, OR 97005 (503) 626-7000							**Circle 308**
Quickfault	Apollo: Aegis, Unix	neted, prop. schematic capt.	mixed behavioral, gate, hardware, switch, compiled logic Quickparts	3 levels, 4 strengths, strong, resistive, indeterminate, high Z	–	HML	LAN accel. (Zycad/SSC interface)
Analog	–	–	–	–	–	–	compute engine accel. prop.
Quicksim	Apollo: Aegis, Unix; Mentor Graphics compute engine	neted, Mentor Graphics, schematic capt.	combination of uni- and bi-directional switches	O, X, 1, strong, resistive, high impedance, fixed, charged, wired forces	BLM, based on C or Pascal	HML	compute engine (prop.) interfaces to Zycad LE/FE and Mach Series

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
delay	—	—	—	—	—	none	$12,000 PC/AT $30,000 VAX
full circuit simulation	prop.	none	—	—	—	none	—
setup/width rise/fall, min/max delay, prelayout timing est., post-layout sim.	—	Zycad-based	Teradyne J841, Trillium micromaster	std. cell CMOS 150+ cells, UC51 cells, 82xx peripheral fam., gate arrays 150+cells	—	—	$125,000 design entry pkg $3,000 timing pkg
LCAP, setup/hold, rise/fall	—	opt. concurrent and serial via Zycad	Sentry and Ando	—	LSI Logic	single chip behavioral sim., accel. sim., fault sim.	$75,000 sw
—	—	—	—	—	—	hardware accel. sim.	$110,000 sw
Arcis (timing analyzer), wave (waveform display utility), prop.	—	Arcop testability analyzer prop.	IMS, Sentry	SSI/MSI, RAM blocks, PALs	same as std. comp. lib., plus basic gates, FFs, I/O buffers	—	$945
yes	—	concurrent	—	—	200+ ASIC technologies, 120+ ASIC design kits, 70+ ASIC foundries	—	$16,000 sw
—	prop. MSpice, MSpice Plus, MSimon	—	—	approx 1,200 analog lib.	same as above	Analog lib. MSimon, MSpice Plus	$9,900 MSpice $23,800 MSimon $19,800 MSpice sw
setup/hold, min/max pulse width and freq., spike, race, hazards	—	—	—	4,000+ SSI/MSI/VLSI	same as above	—	$33,900 sw & hw

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
Microsim 23175 La Cadena Dr, Laguna Hills, CA 92653 (714) 770-3022							**Circle 309**
Pspice	IBM PC, Macintosh II, Sun-3, -4, μVAX, VAX, Supermini & mainframe	Berkely std. netlist	dc or bias point, transient, ac or freq., noise behavior, temp.	–	–	–	–
Mietec Westerring 15, Oudenaarde, Belgium, 9700 (322) 242-5010							**Circle 310**
Made	VAX: VMS	Anasim, Digsim, Mixsim formats	circuit, gates, mixed analog/ digital/behavioral	Digsim: 15, Anasim, Mixsim	Daml, behavioral Pascal type	–	–
Motorola, ASIC Div., 1300 N Alma School Rd, Chandler, AZ 85224 (602) 821-4426							**Circle 311**
Modular Design System	Apollo-Aegis, Mentor: Unix	Mentor-Symed and neted	behavioral (Mentor Quicksim)	O, I, X, strong, resistive, high impedance, indeterminate	Mentors behavioral modeling language	–	–
Modular Design System	Daisy	DED II, font & vector, ace schematic capt. pkg	gate level modeling	O, I, X, forcing, resistive and tristate strengths	–	–	Megalogician 80k gates/s
Modular Design System	Valid	Valid Ged	gates (Valid Sim)	O, I, X, Y, Z	–	–	–
Modular Design System	Futurenet	strides from DC plus	behavioral dash, Cadat w/acculib. library	O, I, X, 2T	behavioral model descript. language	–	–
WACC timeshare	IBM/CMS via remote EWSterms	Logcap, EDIF	gate	O, I, X, Z	–	–	Motorola prop.
National Semiconductor 2900 Semiconductor Dr, Santa Clara, CA 95051 (408) 721-5000							**Circle 312**
Faircad	Cray: Cray OS VAX: VMS	Daisy, Futurenet, Mentor-MIF, Silvar-Lisco-SDL, Valid	gate	O, H, I, X	SCL	–	Cray support
Oki Semiconductor 650 N Mary Ave, Sunnyvale, CA 94086 (408) 720-1900							**Circle 313**
–	Amdahl: MVS VAX: VMS	Daisy, Futurenet, Mentor, Valid	behavior, gate	1, O, X, E, Z	Oki prop.	–	–
Omation 1210 E Campbell Rd, Richardson, TX 75081 (800) 553-9119							**Circle 314**
Schema-Silos	IBM PC/AT/XT, 386 and compat.	Schema II netlist	gate	O, I, X	–	–	–

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
–	Pspice prop.	–	–	240+, bipolar transistors, diodes, power MOSFETs, volt. comp., op amps	–	device equation source code, probe graphics, part parameter est., Monte Carlo, Digital files	$950 sw
setup/hold, rise/fall, min/max	Anasim (Spice like prop.)	Fault.sim (prop.)	Sentry, Teradyne	digital and analog lib.	1.5- to 3-μm CMOS, 3-μm SbiMOS	–	–
setup/hold, rise/fall, pulse width/fanout, capacitance/back annotation	behavioral level approx.	–	–	–	2-μm DLM std. cell 3-μm SLM std. cell	BiMOS macrocell arrays	$7,500 sw
–	A/D Lab	DFS, MDFS, concurrent	VLA IF conversion to Logcap format and TIC (tester Indepen-dent code)	–	same as above	PMX, fault grading, μVAX engine, Mega accelerator	$7,500 sw
setup/hold, rise/fall, pulse width/fanout, metal/ext capacitance	–	–	Logcap for-mat, tester Indepen-dent code	std. cell, 2-μm DLM, 3-μm SLM, 62A to 2-μm, BiMOS MCA 3	–	–	$7,500 sw
setup/hold, rise/fall, epitaxial cap.	–	single fault concurrent fault	–	HCA62A series, 2-μm macrocell arrays	–	fault Able hardware synthesis	–
setup/hold, rise/fall, prop. delays, capacitive loads delay (worst-case)	–	–	tester inde-pendent codes	–	120 ECL/TTL arrays, 120 BiMOS arrays, 118 CMOS arrays	91 software cells for CMOS arrays	$1,400 per 1000 gates (typ.) timeshare
min/max, rise/fall, indust/mil. tester, setup/ hold, environment	–	Fair fault concurrent	Sentry	–	as per timing sim.	schematic capt., place and route	–
Oki prop.	Spice	Oki prop.	Ando, Sentry	4,000 SSI/MSI: CMOS, TTL	250	–	–
loading, delay, dmin/dmax, setup/hold, spike	–	–	–	under development	under development	–	$995 5,000 gate $2,500 16,000 gate

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
OrCAD Systems 1049 SW Baseline St, Suite 500, Beaverton, OR 97123 (503) 640-5007							**Circle 315**
OrCAD/VST	IBM PC/XT/AT, PS/2 and compat.: DOS 2.0 or later	OrCAD/SDT, EDIF	gate	12 states, 4 strengths	primitive based modeling lang. incl. VHDL, PLO compiler	—	—
Personal CAD Systems 1290 Parkmoor Ave, San Jose, CA 95126 (408) 971-1300							**Circle 316**
Hilo & Cadat & Tegas interfaces	—	—	—	—	yes	Hilo & Cadat support	—
PC-Logs	IBM PC: DOS	PC Caps prop.	behavioral, gate	O, I, X; supply driving, resistive, high impedance	prop.	—	—
Racal-Redac Westford Regency Park, 238 Littleton Rd, Westford, MA 01886 (617) 692-4900							**Circle 319**
Cadat 6.1 (digital)	Apollo: Unix Sun-3: Unix VAX: VMS	Visula design capt. (VDC), prop. schematic capt.	behavioral, gate, mixed switch	21 states, 3 logic levels, 3 logic strengths, 12 intermediate	BDL	Cats	Cats accelerator
Saber (analog)	same as above	Visula design capt., Mast modeling lang.	behavioral, mixed circuit	analog signals	Mast	—	—
Roche Systems 1705 N Rankin St, Appleton, WI 54911 (414) 733-6077							**Circle 320**
Sim Good	Apollo: Aegis IBM PC: MS-DOS	Dsim netlist	same as above	O, I, X, driven, resistive, floating, indeterminate	Dsim macro lang.	—	—
Schlumberger CAD/CAM 4251 Plymouth Rd, PO Box 986, Ann Arbor, MI 48106 (313) 995-6000							**Circle 321**
Bravo3 Logic Analysis (based on Cadat)	Sun: Unix VAX: VMS	Bravo3 design capt.	behavioral, mixed: gate, structural comp.	O, 1, X, Z, active passive	Cadat behavioral modeling	Cadat Cats modeler	Cadat Cats accelerator
Bravo3 Analog Analysis (based on Spice)	same as above	same as above	hierarchical gate/structural	—	Spice	—	—
SDA Systems 555 River Oaks Parkway, San Jose, CA 95134 (408) 943-1234							**Circle 323**
SDA timing analyzer	Apollo: Domain IX DEC: Ultrix Sun: SunOS	SDA schematics, EDIF 1.1	block, gate, mixed electrical, switch	3 logic, 4 states	SDA prop. (IL)	no	—
Hilo3 simulation interface	same as above	same as above	funct., gate, mixed switch	3 states, 3 strengths	Hilo HDL	Hichip	—
Silos simulation interface	same as above	same as above	same as above	3 states, 4 strengths	C language	no	—
Verilog Netlister	same as above	same as above	same as above	6 states, 8 strengths	verilog	no	—

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
propagation delay setup/ hold time, removal time & min, pulse widths	Pspice, third party	—	—	1,200 SSI/MSI: CMOS, TTL, ECL	—	VHDL and PLD modeling software	$995 complete
—	interface to Spice	interface to Cadat, Hilo	interface to Cadat, Hilo	—	—	—	$800
rise/fall	—	—	—	—	—	—	$2,750, $4,000 w/schematic capt.
worst case, setup/hold, min pulse, common mode ambiguity	—	Cadat fault	Factron, Sentry	2,000 SSI/MSI, 200 LSI	10+ in development	schematic capt., waveform analyzer, hw modeler, plagen, BDL	$25,000 sw
time domain modeling	Saber	—	—	20+ model templates, 500+ std. analog	—	schematic capt., spectral analysis	—
setup/hold, rise/fall, spike analysis	—	—	—	—	CMOS semi-custom	—	$995 IBM PC $15,000 Apollo
Cadat	—	Cadat concurrent fault sim.	Schlumberger ATE, (Factron/ Sentry), others	approx. 5,000 SSI/MSI: CMOS, MOS, TTL, ECL	—	worst-case timing, models, hardware modeler, accel.	$20,000 sw
Spice	enhanced Spice, prop.	—	—	approx. 200, varies	—	—	$5,000 sw
setup/hold, rise/fall, short/long path	Metasoft-ware Hspice, Spice 2G.6	Hilo, Silos, Testgrade	—	—	—	Metasoftware Hspice, Spice 2G.6, SDA testability analyzer	$7,000 sw
setup/hold, rise/fall, min/max	same as above	Hilo, prop., parallel value list	Advantest, Genrad, SDA STL, Sentry,	—	—	Hspice, Spice, SDA testability & timing analyzer	$5,000 sw
same as above	same as above	Silos, prop., concurrent	same as above	—	—	Silos fault sim., Hspice, Spice, SDA testability analyzer	$5,000 sw
same as above	same as above	concurrent, prop., test grade	—	—	—	Textgrade fault sim., Hspice, Spice, SDA testability & timing analyzer	$3,000 sw

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
Silicon Compiler Systems 2045 Hamilton Ave, San Jose, CA 95125 (408) 371-2900							**Circle 326**
Lsim	Apollo: Domain IX DEC: Ultrix Sun: Unix	EDIF 1.10, Spice, Lsim netlist, formats, GDT schematic capt.	analog, behavioral modeling, circuits, fault, funct., gate, switch	H, L, X, 4096 strengths per state	M language	—	—
Silvar-Lisco 1080 Marsh Rd, Menlo Park, CA 94025 (415) 324-0700							**Circle 327**
Helix	Apollo: Aegis Sun-3: Unix VAX: VMS	Cass-prop. schematic capt., SDL netlist	mixed behavioral, register, gate, switch	user defined (integer, real, enumerated, complex) 0, I, X, Z	HHDL	—	Zycad interface
Cadat-6	same as above	same as above	gate, mixed switch	0, I, X, 4 strength, 21 state	C, BML	Cats	Mach 1000
Simucad 1040 Marsh Rd, Suite 200, Menlo Park, CA 94025 (415) 321-2350							**Circle 328**
Silos	Apollo: Aegis DEC: VAX/VMS Sun: Unix 4.2	Case, Futurenet, Xilinx	behavioral, funct., gate, mixed switch	12 + 5 logic states, high, low, unknown, supply, driving, resistive, high impdence	SBL & C-funct., Simucad behavioral language	—	—
Pacsim	same as above	Spice input and output compat., analog workbench, MSpice	circuit	—	Spice netlist with enhancements	—	multi-processors
Simulog 3211 Scott Blvd, #104, Santa Clara, CA 95054 (408) 727-8272							**Circle 329**
Supersim	stand alone w/interfaces to mainframe host system	Silos compat. netlist	gate level only w/software interface to behavioral levels	0, 1	Sial, simulog interactive language	avail. via external bus	hardware accel., models systems at 3 to 5 kHz clock speeds
Teradyne Design & Test Automation Group, 321 Harrison Ave, Boston, MA 02118 (617) 482-2700							**Circle 331**
Lasar Version 6 simulation system	DEC: VAX/VMS Valid: Unix	Vanguard Stellar, netlist converters	behavioral, hardware, gate, switch	15 logic states, 256 signal strengths	Label, TML	Datasource physical modeling system	Teradyne, Dataserver sim. server
The Great Softwestern 207 Hickory St, Suite 202, Denton, TX 76201 (800) 231-6880							**Circle 293**
The Auto-Board Simulation Interface	MS-DOS	Auto Board interface to Pspice	Pspice	Pspice	Pspice	Pspice	Pspice
United Silicon Structures (US2) 1971 Concourse Dr, San Jose, CA 95131 (408) 435-1366							**Circle 332**
Solo 1000/Solo 1200 (exert)	Apollo: Aegis DEC: VMS IBM PC/AT: DOS Sun: Unix	Case, Daisy, HDL netlist schematic capt., Mentor	RC level	0, L, X, Z driven, charged, glitches	HDL	—	—

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
Ltime critical path analysis, transistor optimization, power estimation	Adept circuit, Lspice analog, prop.	probabilistic fault sim.	Sentry, advantest, IMS	—	—	GDT, Ltime, Lspice	$49,500 sw
setup/hold/freq./pulse width	Andi (mixed A/D), Swap (switched capac.), Spice	—	interface to TSSI = Genrad, IMS, Sentry, Teradyne	4,000: CMOS, TTL, ECL, PDL, memory	—	Andi, Swap, Spice	$35,000 sw
setup/hold, min/max delay, worst case timing	—	Cadat-6, concurrent	—	—	10+	—	$20,000 sw
setup/hold, rise/fall, min/max delay	—	Silos integrated, statstical and concurrent fault sim.	Sentry	TTL, ECL	—	—	$995 PC 20,000 on workstation
—	Pacsim	—	—	supported through Contour	—	user modeling opt., waveform analysis pkg	$20,000 workstation
—	—	Future	—	—	—	capacity expansion to 10M gates	$250,00
true worst-case timing analysis	—	concurrent fault sim.	Computer Automation, Genrad, Teradyne, others	4,000+ SSI/MSI/VLSI: CMOS, TTL, ECL, PLD	6 ASIC design kits	auto. test pattern generator, auto. PLD test generator	$15,000 sw $40,000 hw & sw
Pspice	Pspice	Pspice	Pspice	Pspice	Pspice	the Auto-Board System	$500 sw
setup/hold, timing diagrams, min/max delay	prop.	prop. statistical	Sentry	350+SSI/MSI: CMOS, TTL, I/O pads, 7400 series, system cell	tied directly to US2/ES2	part of integrated Solo IC generation tool	$22,500 bundled

New high performance PC-based emulators from HP.

Introducing the HP 64700 Series emulators. Low-cost, entry-level, PC-based emulators with features you won't find with any others in the price range—or even higher. The HP 64700s deliver unmatched capability, ease-of-use, measurement power, flexibility, and reliability . . . plus HP support.

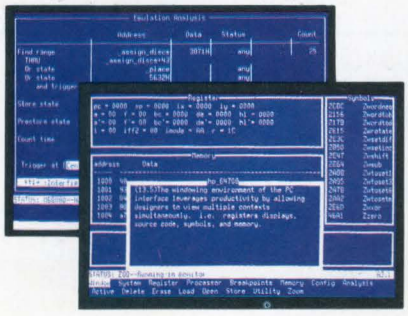
While the HP 64700s are tailored to meet the needs of individual engineers and small design teams, they'll perform equally well for large teams working on complex projects.

The rapidly expanding family of HP 64700 emulators provide real-time, transparent emulation at full processor speeds with no wait states. The PC user interface gives a new meaning to the term "friendly" with features like multiple windows, single-letter keystroke command entry, access to symbols for powerful debugging capability, timing diagrams, and on, and on, and on. The experienced user as well as the beginner will appreciate how easy these emulators are to work with.

In addition to the features shown above, there are lots of others that put the HP 64700s in a class by themselves. To name a few: function with IBM-PC, HP Vectra and compatibles, RS-422 high-speed serial

we never stop asking "What if...

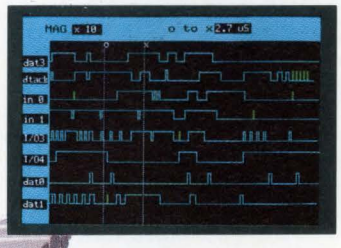
You could spend a lot more and get a lot less.



Multiwindow viewing allows up to eight displays on-screen simultaneously.

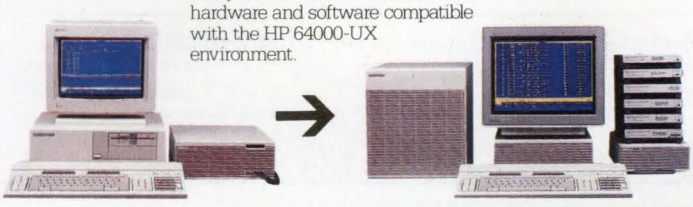
"Sky-hook" handles plus flexible 2- to 3-foot cables and low-profile probes allow easy access into target systems.

Powerful emulation bus analyzer with 8-level sequencing and optional 16-channel, 25 MHz state & 100 MHz timing analyzer available.



Up to 32 emulators can be interconnected, synchronously started, cross armed, cross triggered, and halted.

Entry level HP 64700 emulators are hardware and software compatible with the HP 64000-UX environment.



interface for superior download and upload speed, code coverage analysis for efficient software testing and design, host-independent portability, and compatibility with popular absolute file formats such as Tektronix and Intel hexadecimal and Motorola S record.

Once you get your hands on an HP 64700 emulator, you'll agree that this is the new standard in the field. Especially at a starting price of $8,900.

Free demo disc.

For a free demo disc that gives you the "hands-on" feel for HP 64700 Series capabilities, call HP at 1-800-752-0900 ext. 786E, or mail the attached business reply card.

HEWLETT PACKARD

CIRCLE NO. 40

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
United Technologies Microelectronics Center 1575 Garden of the Gods Rd, Colorado Springs, CO 80907 (800) MIL-UTMC							**Circle 333**
Highland	VAX: VMS	Daisy, Mentor, Valid, netlist	gate	O, I, X, Z	VHDL 1076B	–	Zycad
Valid Logic Systems 2820 Orchard Parkway, San Jose, CA 95134 (408) 432-9400							**Circle 334**
Validsim logic simulator	PCs: Unix Sun-3, -4: Unix VAX, μVAX, 3000: VMS	ValidGED graphics editor, EDIF 2.0	switch (MOS pass transistor), gate, behavioral	20 state sim., incl., 3 logic levels, 4 signal strengths	Pascal and C	Realship, Realchip II and Real model	Realfast, 500k events/s (max)
Validtime timing verifier	same as above	same as above	–	24 states, 8 values	–	–	–
Vamp 6753 Selma Ave, Los Angeles, CA 90028 (213) 466-5533							**Circle 335**
DSIM	MacPlus and Macintosh SE & II: Macintosh	McCAD schematics, EDIF (Q4 88)	gate	O, 1, X, Z, active, passive, indeterminate	–	–	–
ASIM	same as above	–	analog models, Spice	from command file	Spice	–	–
Vantage Analysis Systems 42840 Christy St, Fremont, CA 94538 (415) 659-0901							**Circle 336**
Vantage Spreadsheet	Apollo: Aegis	Mentor Graphics, direct database access	full multilevel, gate through architecture	user-definable	full VHDL IEEE 1076 spec.	–	–
Viewlogic Systems 275 Boston Post Rd W, Marlboro, MA 01752 (617) 480-0881							**Circle 337**
Viewsim	286/386: DOS, native mode Sun: Unix VAX: VMS	Viewdraw, prop. schematic capt.	behavioral, circuit, funct., gate, switch	O, I, X, Z, driving weak, capacitive	VHDL 1076	–	Zycad interface
Visionics 343 Gibraltar Dr, Sunnyvale, CA 94089 (800) 553-1177							**Circle 338**
EE Designer	IBM PC/XT/AT, PS/2: DOS	EE Designer	gate, behavioral	O, 1, T, active, passive	VHDL	–	–
EE Designer II	same as above	same as above	same as above	same as above	same as above	–	–
EE Designer III	same as above	same as above	same as above	same as above	same as above	–	–
VLSI Technology 1109 Mckay Dr, San Jose, CA 95131 (408) 434-3100							**Circle 339**
Logic Express	Apollo, Sun, DEC, HP, Aegis, Unix, VMS	prop. EDIF 2.0, Daisy, Mentor	mixed, switch, gate, behavioral	O, I, X, LL, nodes states are continuous in 0.1 V	VTIModel	–	Mach 1000
Concept Express	same as above	same as above	behavioral, gate, mixed, switch	O, I, X, LL node states are continuous in 0.1 V	VTIModel	–	Mach 1000

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
setup/hold, min pulse width, min/max delay	prop.	prop., concurrent, Zycad	Genrad, Trillium	100+ SSI/MSI/ LSI from UTMC, ASIC lib.	UTMC	bus contention check, rad hard current density analysis	—
min/typ/max delays, comp. & wire, input-pin to output-pin delays, rise/fall, setup/hold	Precise	Faultfree	Genrad HP, IMS, Sentry, STS, Teradyne, Trillium,	4,000+ TTL,ECL, PLDs, memories, LSI/VLSI logic auto. behavorial models, analog lib.	97+ ASIC design kits	Realchip, Realchip II, Realfast, Realmodel, Validtime, Faultfee	$12,500 sim. $27,950+ turnkey
rise/fall, recovergent, fanout, wire delays, global default, estimated, specified	—	—	—	same as above	same as above	—	$6,250 sw $27,950+ turnkey
min/max delay	—	—	—	1,000+	—	—	$295 sw
—	Spice	—	—	std. models	—	—	$1,995 sw
incl. as part of VHDL modeling environment	—	—	tester-independent ASCII format	4,000+ SSI through VLSI avail. Q4 88	avail. starting Q4 88	hardware analyst, system analyst, model lib.	$30,000 to $60,000 sw
setup/hold, rise/fall, fanout, pulse, clock skew	Viewsim/ Ad, prop.	—	TSSI	3,000+ SSI/MSI: CMOS, TTL, ECL, PAL	—	—	—
rise/fall, min/max delay, spike analysis	prop.	prop. conncurrent	—	1,000+: CMOS, TTL	—	—	$995 w/integrated system
same as above	prop.	same as above	—	same as above	—	—	$1,895
same as above	prop.	same as above	—	same as above	—	—	$3,995
setup/hold, clock skew, min/max delay, pulse width, critical path	Opt. VTISpice	Mach 1000	sentry/STS Magaone	—	1.5- & 2-μm std. cell gate array	compilers, ASIC layout verification	$30,000 sw
same as above	opt. VTISpice	Mach 1000	sentry/STS Magaone	—	same as above	ASIC layout ver.	$70,000

DESIGNERS' BUYING GUIDE/Simulation Systems

Model	Platforms: Operating Systems	Design Entry Formats	Levels of Analysis	States and Strengths	Modeling Languages	Hardware Modeling	Acceleration Support
XCAT 2855 Anthony Lane S, Minneapolis, MN 55418 (612) 789-2050							**Circle 342**
MXT-100	Apollo: Aegis/Unix IBM PC/AT: DOS	Futurenet, Mentor, OrCAD, Viewlogic	gate, switch	O, I, X, Z, 4 strengths	Silos, Tegas, Hilo, Verilog	—	XCAT prop., 1 to 2M events/s
Zycad 3900 Northwoods Dr, Suite 200, St Paul, MN 55112 (800) 631-5040							**Circle 343**
Logic Evaluator	Apollo: Aegis Sun: Unix IBM VAX: VMS	interfaces to over 70 design environ.	mixed transistor, gate, behavioral (opt.)	O, I, U, supply, driving, resistive, high impedence	—	—	Zycad
Magnum II	Apollo: Aegis Sun: Unix VAX: VMS	same as above	mixed transistor, gate, behavioral	same as above	—	—	—
System Development Engine	VAX: VMS	vendor supplied and prop. interfaces to over 25 design environ.	mixed transistor and gate	same as above	—	—	—
Mach 1000	Apollo: Unix Sun: Unix	Mach Tools prop., HX - Hilo interface, MX Mentor Graphics interfaces	mixed transistor, gate, behavioral	O, I, X, N, rail, forcing, driving, active, passive, tristate, large/ small capacitive	Mach Tools, EDIF	HHB Cats	—

DESIGNERS' BUYING GUIDE/ASIC Layout Systems

Model	Platforms: Operating Systems	Design Entry Formats	Gate Array Tech. & Max. # of Gates	Std. Cell Tech. & Max. # of Transistors	Placement Capabilities	Routing Capabilities
Advanced Micro Devices 901 Thompson Pl, PO Box 3453, Sunnyvale, CA 94088 (408) 732-2400						**Circle 254**
XACT	IBM PC: MS-DOS	netlist	CMOS, LCA 2000	—	interactive or auto., sim. annealing algorithm	interactive or auto.
Aptos Systems 5274 Scotts Valley Dr, Suite 107, Scotts Valley, CA 95066 (408) 438-2199						**Circle 262**
Cell Pro	IBM PC: DOS	Aptos Schema, Futurenet, OrCAD, PCAD	CMOS	CMOS 25,000	interactive	interactive
ICD-One	IBM PC: DOS	same as above	CMOS	CMOS 25,000	interactive	interactive

Timing Analysis	Analog Simulation	Fault Simulation	Test Vector Output	Standard Component Libraries	ASIC Libraries	Options/Upgrades	Price
setup/hold, rise/fall, glitch detection	—	parallel	generalized output data	Mentor Genlib	NCR, SMOS	—	$60,000 to $80,000 turnkey
rise/fall delay, input delay	—	prop. accel. concurrent	—	6,000 SSI/MSI	LSI	fault evaluator for concurrent fault sim., Zilos software interface, eventlink	$125,000 accel.
same as above	—	same as above	—	same as above	LSI	concurrent fault, Zilos eventlink	$38,000 accel.
O, I	—	—	—	same as above	—	—	$1,500,000 accelerator
rise/fall, min/max, propagational delay, input pin delay	—	prop., concurrent accelerated	Sentry	2,000+	8 ASIC - vendor supplied	concurrent fault, cluster opt.	$70,000 accel. and internal host system

Qualified Vendor Libraries	Design Verification Supported	Extraction Capabilities	I/O Formats	Options/Upgrades	Price
AMD logic cell array	on-line DRC, in-circuit ver.	—	—	—	$3,600 sw only
—	—	connectivity	GDSII	—	$1,995
—	—	connectivity	GDSII	—	$6,700

Model	Platforms: Operating Systems	Design Entry Formats	Gate Array Tech. & Max. # of Gates	Std. Cell Tech. & Max. # of Transistors	Placement Capabilities	Routing Capabilities
CAECO 2945 Oakmead Village Court, Santa Clara, CA 95051 (408) 988-0128						**Circle 270**
Blocks	Apollo: Aegis Apollo: Domain IX Sun -3, -4: Unix	CAECO schematic prop. format	—	CMOS, NMOS, ECL, unlimited	interactive and/or auto. min cut algorithm, pair-wise interchange, sim. annealing, row balancing	auto. global preroute channel
Control Data 2800 Old Shakopee Rd, Box 0, Minneapolis, MN 55440 (612) 853-3117						**Circle 275**
Midas	CDC Cyber	Apollo/Mentor, or Daisy schematic capt., logic interconnect lang. prop.	CMOS, 2,000,000	CMOS	interactive (Apollo workstation)	auto. (Cyber-Midas)
Daisy Systems 700 E. Middlefield Rd, Mountain View, CA 94039 (415) 960-6674						**Circle 276**
Gatemaster	Logician 386: Daisy-Dnix Personal Logician 386: Daisy-Dnix	ACE, DED II (Daisy schematic editors)	CMOS 6,200, bipolar 2,700	—	interactive or auto., sim. annealing algorithm, accel. opt.	interactive or auto., channel, maze, rip-up and reroute, accel. opt.
ECAD 2455 Augustine Dr, Santa Clara, CA 95054 (408) 727-0264						**Circle 281**
Symbad	Apollo, DEC, μVAX, Sun, Tektronix, VMS, Aegis, Unix	Mentor, Silos, Tegas	—	CMOS, bipolar, GaAs, no software limit.	clustering, partitioning, geometric fitting full auto. pad, terminal placement opt., and others	global, channel, switch box
Dracula	μVAX: VMS, Ultrix, Apollo, Sun, Mips, IBM	netlists, Spice, Hspice, Simon, Tegas, Hilo, Silos, and others	no software limit.	no software limit.	—	—
Emerald Design Systems/Andrew Tickle Associates 1043 N Shoreline Blvd, Mountain View, CA 94043 (415) 965-3300						**Circle 261**
LSG/Turbo CAD	Apollo and PC 286/386's, Silicon Graphics, Sun, VAX	SDS, Silos, Spice	—	auto. CMOS cell layout, design rule driven	interactive or auto.	interactive or auto.
Europe Silicon Structures (ES2) Hollybank House, Mount Ln, Bracknell, Berks, RG12 3DY, United Kingdom 34 45 25252						**Circle 288**
Solo 1000/Solo 1200 (place, gate, route, draw)	Apollo: Aegis DEC: VMS IBM PC/AT: DOS Sun: Unix	Case, Daisy, HDL netlist, Mentor, schematic capt.	gate arrays not supported	CMOS 64,000	auto. logic is placed based upon design entry hierarchy structure	auto. channel, critical paths can be tagged to have routing priority
GE Solid State Rte 202, Somerville, NJ 08876 (201) 685-6000						**Circle 291**
Vital	Apollo: Aegis IBM: VM Sun: Unix VAX: VMS	GE netlist, Tegas (TDL)	—	CMOS 120,000	auto. std. cell and block p/r, partitioning based algorithms, sim. annealing	global, channel, maze routing, auto. routing and sizing or power and ground buses

Qualified Vendor Libraries	Design Verification Supported	Extraction Capabilities	I/O Formats	Options/Upgrades	Price
–	batch, DRC	resistance, capacitance, R/C	CIF, GDSII	layout synthesis, schematic capt., custom layout	$35,000
CDC, Honeywell, VTC	batch Cyber, Dracula OEM	–	GDS2, PG (ALF)	–	$85,000 to $435,000 sw Cyber 180 family
CDI, Datalinear, Exar, GE, Matra Harris, Microlinear, Philips, Siliconix, UTMC	on-line, batch, DRC	connectivity, transistor (wire delays)	GDSII	foundry-defined autolayout runs incl.	$22,000 layout sw only $58,500 turnkey system
–	batch, on-line verification, symbad symbolic	connectivity, parasitic capacitance and resistance	GDSII, Applicon, Symbad ASCII, PG, Dracula, E Beam	symbolic layout and compaction, polygon editor, auto. floor planner	$50,000 to $100,000
–	batch, on-line, incremental, hierarchical	CMOS, MOS, bipolar, GaAs, connectivity, w/R and C parameters	GDSII, CIF, Applicon	–	$25,000 sw
design role independent lib. supplied w/system	Emerald's Jade-Batch and incremental, also interface w/ECAD and Maskap	–	APL, CIF, EDIF, GDSII	Emerald's editor and plot driver	$28,000 module gen. $22,000 place and route
US2, ES2	built in ERC, correct by design layout	gate loads, net interconnect, loading capacitance	CIF, GDSII	part of integrated Solo IC generation tool	$22,500 (bundled only)
GE Solid State	ECAD, Enlave-GE, Concert-GE	connectivity, transistor, R&C	Apple, CIF, EDIF, GDSII	mixed digital/analog placement	$70,000 sw only

Model	Platforms: Operating Systems	Design Entry Formats	Gate Array Tech. & Max. # of Gates	Std. Cell Tech. & Max. # of Transistors	Placement Capabilities	Routing Capabilities
Harris Semiconductor/Semicustom Products, PO Box 883, Melbourne, FL 32901 (305) 724-7000						**Circle 294**
Optilogic.B	Sun-3, -4: Unix	Optilogic.F, Daisy, EDIF netlist, Mentor	CMOS 100,000 (1/89)	CMOS 100,000	std. cell, macrocell	SDA router, power options, contour routing
Optilinear.B	same as above	Optilinear.F	—	bipolar, to 200 V, to 1.2 GHz	interactive	interactive
IC Designs 12020 113th Ave NE, Kirkland, WA 98034 (206) 821-9202						**Circle 298**
IC Works Desktop, ASIC Design System	IBM PC/AT: MS-DOS	Desedit design editor (prop.) or CAD/SDT	—	2μm CMOS, up to 20,000 transistors	auto. std. cell placement, Mason, global interactive block placement tool	auto. channel and river router, std. cells, Mason, global interactive block routing tool
IC Editors PO Box 5938, San Jose, CA 95150 (408) 971-2422						**Circle 299**
Iced Graphics Editor	IBM PC and compat.: MS-DOS, PC-DOS	—	—	—	interactive (70,000 transistor chips have been designed)	interactive
Intergraph One Madison Industrial Park, Huntsville, AL 35807 (205) 772-2000						**Circle 305**
Tancell cell-based IC Design	Intergraph Clipper based workstations	EDIP, Hilo, TDL, Silos netlists, GDSII, EDIF physical descript.	—	10,000+ cells, CMOS, GaAs	auto. cell, macro-block, digital/analog cell segregation, timing-driven placement of cells	auto. single/double metal, 2 half-layer, power routing, macro-block, gridless
Integrated Silicon Design Pty Ltd PO Box 99, Rundle, 230 North, Terrace, S Australia, 5000 +61-8-223 5802						**Circle 301**
Phase One	Apollo: Aegis; HP 9000: HPUX; IBM PC/AT: MS-DOS Xenix; Sun: Unix; VAX:VMS	mask level geometrical descriptions	full custom CMOS, NMOS, (GaAs Q4 88)	—	interactive and auto.	manual
Phase Two	same as above	symbolic layout	same as above	—	same as above	manual
Phase Three	Apollo: Aegis HP 9000: HPUX Sun: Unix VAX: VMS	schematic, symbolic, geometric	same as above	—	interactive or auto. from floorplan	manual, channel, river
Integrated Silicon Systems (ISS) PO Box 13665, Research Triangle Park, NC 27709 (919) 361-5814						**Circle 302**
LTL-100	IBM PC/AT: DOS	—	CMOS, NMOS, bipolar, (analog), 10,000	CMOS, NMOS, bipolar, (analog), 20,000	interactive	—
LTL-100/386	Compaq 386: DOS	—	CMOS, NMOS, bipolar, (analog), 100,000+	CMOS, NMOS, bipolar, (analog), 150,000+	interactive	—

Qualified Vendor Libraries	Design Verification Supported	Extraction Capabilities	I/O Formats	Options/Upgrades	Price
Harris CMOS, (VLSI 1/89)	DRC, LVS	parasitic C	Stream, PG tape	RAM, ROM compilers foundry	$137,000
Harris Analog	DRC, LVS	parasitic C	Stream, PG tape	auto. device gen., circuit sim. w/mome Carlo, foundry	$104,000
IC Designs, 2-μm CMOS std cell lib.	QERC (prop.), ADRC (prop.)	connectivity, transistor, R&C (prop.)	CIF, GDSII	IC Designs, cell editor, ($5K)	$10,000 sw only
—	—	—	GDSII, CIF	—	$995 sw only
Motorola, NCR, Standard Microsystems, SMS, Waferscale, VTC	DRC, ERC, timing analysis	interconnect delay, layer, capacitance	EDIF, Hilo, TDL, Silos netlist, GDSII, EDIF physical decript. ASCII reports	Tansure timing-driven layout, Tantest auto. scan test synthesis, auto test pattern gen.	$55,000 sw
Orbit, AWA (Australia)	on-line, batch, DRC, ERC	transistor, capacitance	CIF	—	$5,000 for PC $30,000 for VAX
Orbit	on-line, batch, interactive	same as above	CIF	—	$12,000 for PC $40,000 for VAX
none	same as above	same as above	CIF	—	—
any GDSII Stream compat.	any GDS II compat.	—	GDS II, CIF and Applicon	CCC/200 cell compiler, plotting software, networking, C data base access	$15,950 w/high-res. monitor and cont.
same as above	same as above	—	same as above	same as above	$19,750 w/high-res. monitor and cont.

Model	Platforms: Operating Systems	Design Entry Formats	Gate Array Tech. & Max. # of Gates	Std. Cell Tech. & Max. # of Transistors	Placement Capabilities	Routing Capabilities
Mentor Graphics 8500 S W Creekside Pl, Beaverton, OR 97005 (503) 626-7000						**Circle 308**
Gate Station	Apollo DN3000, DN4000: Aegis/Unix	neted, DDF	MOS channeled & sea of gates, bipolar unlimited capacity	—	interactive & auto. global & detail	interactive & auto. channel, maze, rip-up & retry, overall routing
Cell Station	same as above	neted, DDF	—	MOS, bipolar, 7,500 placeable objects/hierarchy level	interactive & auto. constructive initial placement - pair wise interchange, net priorities	interactive & auto., interactive power & signal routing, batch & interactive
Chip Station	same as above	neted	unlimited	—	interactive	interactive
Mietec Westerring 15, Oudenaarde, Belgium, 9700 (322) 242-5010						**Circle 310**
MADE (Mietec analog and digital eng. supt.)	VAX: VMS	Silvar-Lisco SDL	—	1.5- to 2.4-μm CMOS, 3-μm SBiMOS	Calm P (Silvar-Lisco), auto. or interactive	Calm P (Silvar-Lisco), auto. and distributed delay extract. (back annotation)
National Semiconductor 2900 Semiconductor Dr, Santa Clara, CA 95051 (408) 721-5000						**Circle 312**
Faircad	Apollo: Aegis Sun: Unix VAX: VMS	Daisy, Mentor MIF, Silvar-Lisco SDL, Valid/Futurenet	CMOS 15,000 ECL 6,300 Aspect 15,000	—	interactive or auto. seeded auto., scatter auto., on-line rule checking, critical-path ident.	interactive or auto., on-line rule checking, maze and Manhattan routing
Oki Semiconductor 650 N Mary Ave, Sunnyvale, CA 94086 (408) 720-1900						**Circle 313**
Calma 5280	VAX: VMS Amdahl: MVS	Daisy, Futurenet, Mentor, Valid	CMOS 10,000	CMOS 30,000	interactive and auto.	interactive and auto.
Racal-Redac Westford Regency Park, 238 Littleton Rd, Westford, MA 01886 (617) 692-4900						**Circle 319**
ISIS/Visual Silicon	VAX: VMS	schematic capt., ISIS adv. HDL, ISI forms	—	CMOS 500,000+	std. cell min-cut., complex arrays, interactive	auto. channel route, interactive
SDA Systems 555 River Oaks Parkway, San Jose, CA 95134 (408) 943-1234						**Circle 323**
SDA ASIC layout	same as above	Silvar-Lisco SDL, Mentor MIF, EDIF	—	CMOS, NMOS, bipolar, GaAs, over 13,000 cells	interactive or auto., clustered placement algorithm	interactive or auto., gridless 90 and 45 deg. contour routing, interactive global router
Seattle Silicon 3075 112th Ave N E, Bellevue, WA 98004 (206) 827-4224						**Circle 324**
Chipcrafter	Apollo: Aegis, Unix	Mentor schematic, logic synthesis lang.	—	CMOS, 100,000 to 450,000	fully auto.	fully auto.
Concorde	same as above	same as above	same as above	same as above	same as above	same as above

Qualified Vendor Libraries	Design Verification Supported	Extraction Capabilities	I/O Formats	Options/Upgrades	Price
Gould/AMI, NEC, Siliconix	correct by construct., error prevention, Dracula II/III opt.	wire length delays	DGSII Stream, Applicon, gate lister, EDIF, DDF	logic sim., circuit sim., fault sim.	—
MOSIS	same as above	same as above	GDSII Stream, Applicon, Cell Lister, DDF	same as above	—
—	interactive DRC, Dracula II/III, Remedi-debugger	Spice for circuit sim.	GDSII Stream, Chip Lister	same as above	—
MTC CMOS 3-, 2.4- and 1.5-μm, MTC SBIMOS lib.	DRC, ERC, (Maskap, Calma)	connectivity, transistor maskap & back annotation	GDSII	spec, sim. netlist, GDSII	USD $20,000 w/netlist USD $30,000 w/spec
Fairchild/National	on-line, batch, DRC, NRC, ECAD	full wire and via analysis	GDSI and APL	schematic capt., timing sim., fault sim.	—
Oki	on-line, batch, DRC, ERC, Dracula	connectivity	GDSII	—	turnkey only
SMS multifoundry cells	interactive DRC hierarchical, connectivity check	signal loads	GDSII I/O optical and E-beam P.G.	full custom layout, layout compactor interface to Spice Cadat and Ella sim.	$70,000 sw only
—	on-line, interactive, hierarchical, incremental, DRC, ERC, Extract, LVS	all schematic devices and interconnect as well as most parasitic	GDSII, EDIF	—	—
Seattle Silicon, std. cells and compilers	provided as service	provided as service	prop.	add. rules sets, application specific lib.	$59,000 w/full compiler-based design system
same as above, GDSII format cells	batch, Dracula II and LVS interface	interface to std. programs for connectivity, transistor R&C	GDSII, CIF	same as above	$125,000 w/full compiler-based design system

Model	Platforms: Operating Systems	Design Entry Formats	Gate Array Tech. & Max. # of Gates	Std. Cell Tech. & Max. # of Transistors	Placement Capabilities	Routing Capabilities
Silicon Compiler Systems 2045 Hamilton Ave, San Jose, CA 95125 (408) 371-2900						**Circle 326**
GDT	Apollo: Domain IX DEC: Ultrix Sun: Unix	EDIF 1.10, GDT schematic capt., Mentor	—	CMOS, NMOS, bipolar, more than 1 million transistors	auto. or user guided-loose routing, mincut & sim. annealing algorithms	block, channel, power & ground, auto. & procedural
Genesil	same as above	Silicon Compiler Systems: forms, Mentor: neted (opt.)	—	CMOS 50,000+	interactive blocks or auto. std cells	auto. w/control of channel assign. and net prior., algorithms for block, clock, power & pad routing
Silvar-Lisco 1080 Marsh Rd, Menlo Park, CA 94025 (415) 324-0700						**Circle 327**
CAL-MP, SCII	Apollo: Aegis IBM: VM/CMS VAX: VMS	Silvar-Lisco schematic, SDL textual format, netlists via translators	—	BiCMOS, CMOS, NMOS, bipolar, GaAs, 100,000+ transistors	floorplanning, interactive and auto., cluster-based intitial placement and others	global, channel routing, 2-, 2 1/2- and 3-layer interconnect, routing over/thru/into cells
Gards, Gards-XL, Avant Gards	same as above	same as above	CMOS, NMOS, BiCMOS, bipolar, GaAs, 150,000+	—	floorplanning, interactive and auto., force-directed pairwise interchange, and others	interactive and auto., line-search & maze algorithm, 1, 2, and 3-layer interconnect, and others
Tangent Systems 2840 San Tomas Expwy, Suite 200, Santa Clara, CA 95051 (408) 980-0600						**Circle 330**
Tancell	Apollo: Aegis Intergraph: VMS,μVMS, Unix Sun: Unix VAX: VMS,μVMS	netlists EDIF, Hilo-3, Silos, physical design data: EDIF, GDSII Stream	—	15,000+ cells: CMOS, GaAs, BiCMOS	auto. floorplanning, incl. both cells and funct. blocks	completely auto., gridless, 2.5 layer, auto. power w/multiple styles
The Great Softwestern 207 Hickory St, Suite 202, Denton, TX 76201 (800) 231-6880						**Circle 293**
The AutoBoard System	MS-DOS	Futurenet, OrCAD, Schema	1 to 4,000 nets	1 to 4,000 nets	manual or interactive	auto. rip-up & reroute, prerouter, stop & restart, grid & gridless
United Silicon Structures (US2) 1971 Concourse Dr, San Jose, CA 95131 (408) 435-1366						**Circle 332**
Solo 1000/Solo 1200 (place, gate, route, draw)	Apollo: Aegis Dec: VMS IBM PC, AT: DOS Sun: Unix	Case, Daisy, HDL netlist, Mentor, schematic capt.	gate arrays not supported	CMOS 64,000	auto.: logic is placed based upon design entry hierarchy structure	auto.: channel, critical paths can be tagged to have routing priority
United Technologies Microelectronics Center 1575 Garden of the Gods Rd, Colorado Springs, CO 80907 (800) MIL-UTMC						**Circle 333**
Highland	VAX: VMS	Daisy, Mentor, Valid, netlist	CMOS 40,000	—	auto., interactive	auto., channel
VLSI Technology 1109 Mckay Dr, San Jose, CA 95131 (408) 434-3100						**Circle 339**
Silicon Express	Apollo, Sun, DEC, HP, Aegis, Unix, VMS	prop. EDIF	CMOS 65,000	CMOS 100,000	auto. w/placement improvement	interactive channel w/compaction
Design Express	same as above	prop. EDIF	CMOS 65,000	CMOS 100,000	same as above	same as above

Qualified Vendor Libraries	Design Verification Supported	Extraction Capabilities	I/O Formats	Options/Upgrades	Price
Lcompilers-process, portable silicon compiler lib.	Lsim mixed-mode analog & digital sim., batch or interactive ERC/DRC, fully integrated in GDT	connectivity, transistors, parasitic, capacitances areas	GDSII, EDIF 1.10 Spice	Lcompilers-process, portable silicon compiler lib., Lspice analog sim., Ltime crit. path analyzer	$88,000 sw only
20+ fabline vendors	static timing analysis funct. sim., logical design rule checking, and others	auto. models for transistor, gate, funct., power, and parasitics	GDSII, CIF	Genesil ATG, Lcompilers, Geneport, and others	$99,500 sw only
Exar, Fairchild, Marconi, Mietec, Racal, SGS-Thomson, Siliconix, TI	correct-by-construction, batch, DRC, ERC, NCC, EPC	RC delay analysis, interconnect capacitance extract.	GDSII, CV, Applicon, CIF	3-layer routing pkg	$57,000 w/ schematic entry, sw
AMD, Fairchild, Racal, SGS-Thomson, TI	on-line DRC, NCC, batch DRC, ERC, NCC, EPC	same as above	Applicon, CIF, CV, GDSII	1-layer routing pkg, open system-access routines	$60,000 w/ schematic entry, sw
Motorola, NCR, SMOS, SSI, Standard Microsystems, Waferscale, VTC	ERC, DRC, timing analysis	interconnect delay, layer, capacitance	netlist, EDIF, Hilo-3, TDL, Silos, physical design, EDIF, GDSII Stream, ASCII	Tansure: timing drive layout	$70,000 w/tansure on workstation
generic	batch netlist only	connectivity netlists, parts list, wire wrap, etc.	—	autorouting	$750 sw only
US2, ES2	built-in ERC, correct-by-design layout	gate loads, net interconnect, loading capacitance	GDSII, CIF	part of integrated Solo IC generation tool	$22,500 (bundled only)
UTMC	ERC, DRC, ECAD	connectivity, transistor	GDSII, prop.	—	incl. in design NRE
VLSI	—	—	—	interactive layout & verification	$140,000 sw
VLSI	on-line, batch, ERC, prop.	connectivity; transistor, R&C	—	—	$195,000 sw

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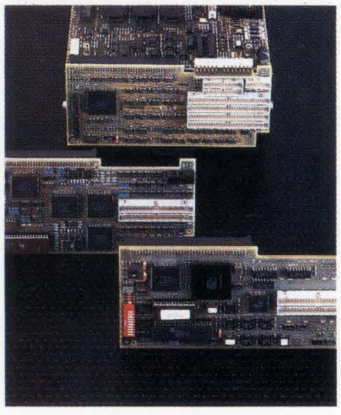

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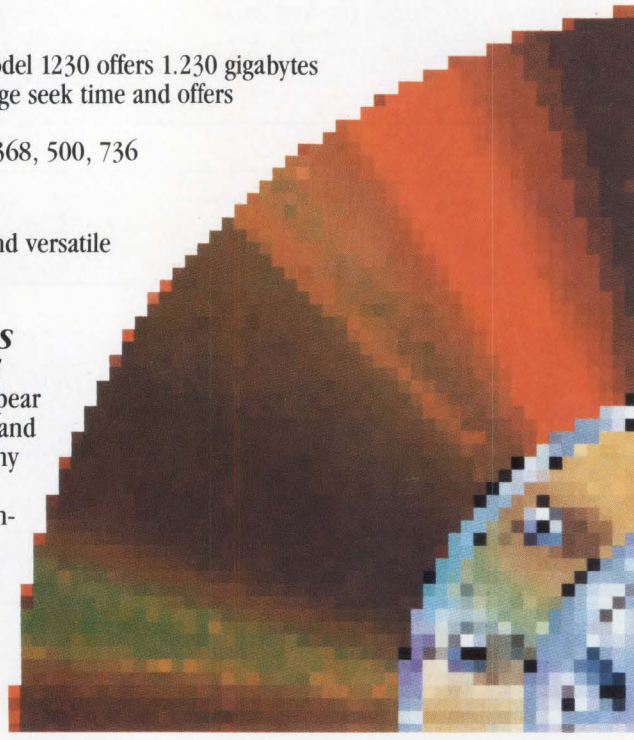
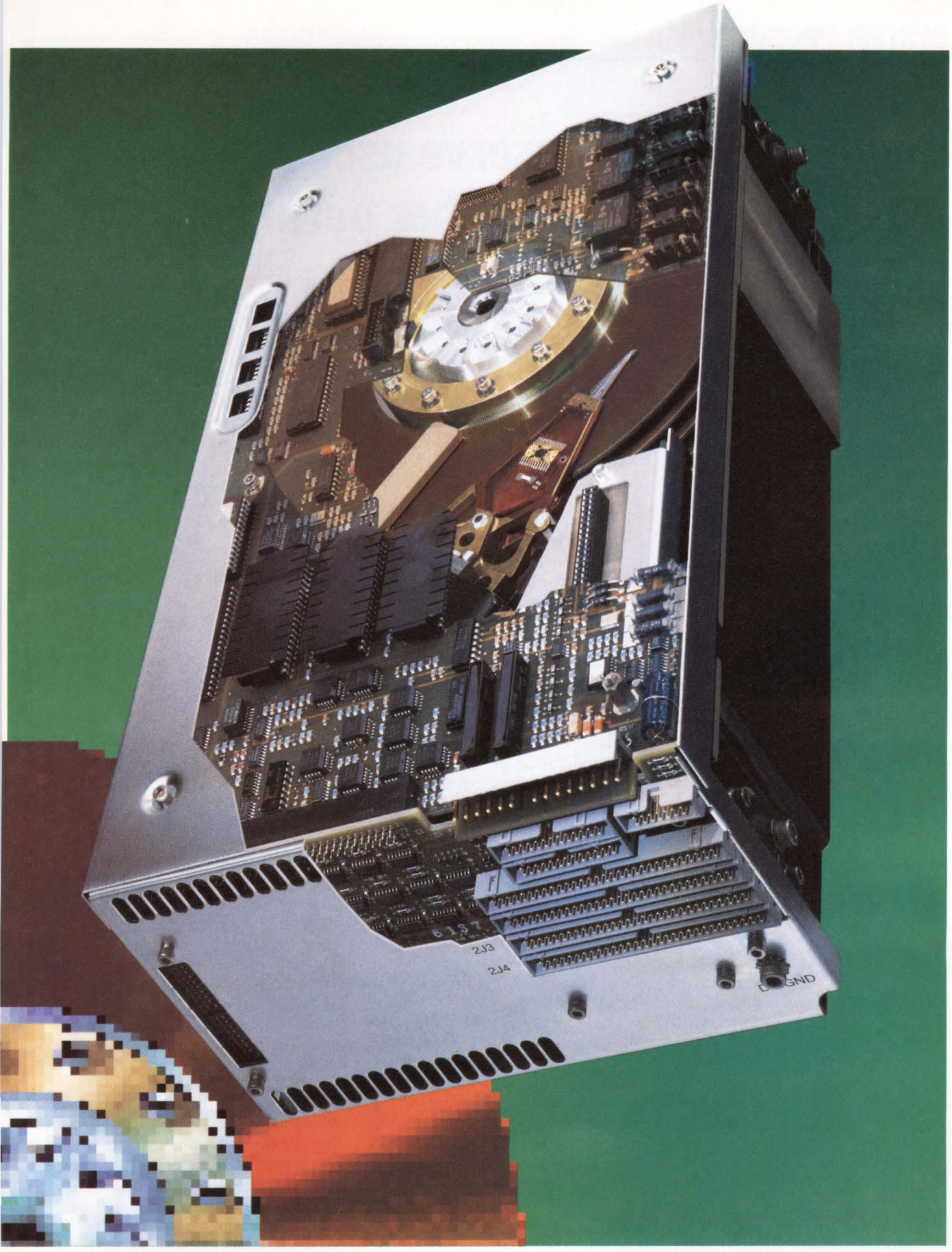


CONTROL DATA

CIRCLE NO. 41


2J3
2J4
GND

Logic analyzers preserve user investment with expandability, higher performance

Not long ago, designers looking at logic analyzers priced under $4,000 found products primarily targeted for education, field service and simple bus troubleshooting. If they needed to analyze an 8- or 16-bit microprocessor's I/O activity, they probably had to spend close to $10,000. And when their designs began integrating higher speed 32-bit parts, they were forced to move to another logic analyzer and a higher price bracket.

High performance was available at low cost, but users typically had to make a sacrifice. One way that vendors typically cut cost was by trading clock speed for channels. A low-end analyzer might offer 16 channels at 25 MHz, eight channels at 50 MHz or four channels at 100 MHz. Even on some higher speed instruments, memory or sampling speed was cut in half if glitch capture was used. On other units, the use of multiple clocks significantly cut state acquisition speed.

Certainly, products offering these trade-offs are still available at the lowest price ranges. But a dramatic effort to bring down the prices of general-purpose logic analyzers has effectively lowered the entry costs of relatively high performance analysis and, to some extent, has eliminated the need for these performance trade-offs. Designers can now buy a 100-MHz logic analyzer with close to 100 channels for under $10,000. And if they don't require that level of performance for their current design, the modular architectures of the latest instruments let them invest now in a lower performing, less costly configuration and upgrade later as needed.

Logic analyzer prices have been dropping for some time, but the introduction of the HP 1650A and HP 1651A by Hewlett-Packard (Palo Alto, CA) last August revised user expectations. With a design that integrated a complete 16-channel logic analyzer and acquisition memory onto a single chip, the 1650A delivered 80 channels of 100-MHz transitional timing and 25-MHz state analysis for under $8,000. At less than half that price, the HP 1651A supplied 32 channels of 100-MHz transitional timing and 25-MHz state analysis. Both units also offered dual time-base operation for multi-CPU applications.

PRODUCT FOCUS

The significance of the HP announcement wasn't lost on the market. The 1651A delivered a complete package for the design and test of 8-bit microprocessor-based systems for under $4,000, an unprecedented price/performance achievement. At 80 channels, the 1650A targeted 16- and 32-bit systems. A simplified front panel on both instruments, freed from clutter by the use of a single knob and keypad, amplified the importance of ease-of-use.

The latest logic analyzers to hit the market deliver a competitive jump in performance. Introduced this month and marketed by John Fluke Mfg (Everett, WA), the Philips PM 3655 can tackle the latest 32-bit, bit-slice and reduced-instruction-set computer processors—and, at a price of less than $10,000, it costs about $5,000 less than its predecessors of equal capability. The user-configurable analyzer packs up to 96 channels in its box on optional 24-channel cards. Each channel is backed by twice the memory (2 kwords) found in the HP 1650A.

Unlike many other analyzers—including the HP unit—that only offer 25-MHz state analysis, the PM 3655 provides full 100-MHz operation across all channels for both state and timing analysis. There's no trade-off between number of channels and clock rate. Nor is there any loss of speed or memory when implementing the unit's 5-ns glitch capture. "Every spec point is aligned with 100 MHz," emphasizes Hans Binnerts, international product manager for Philips T & M (Eindhoven, The Netherlands). "Our setup and hold times are corresponding with 2-ns setup time and 2-ns hold time. It's really 100 MHz."

The analyzer uses a four-level triggering scheme, with up to three trigger words definable at each level. With this scheme, the PM 3655 can track four nested branching levels in a program with an if-then-else statement at each level, so any one of three actions can be taken. The system is effectively equivalent to a 12-level trigger sequence.

The PM 3655 also offers full personal computer functionality. An on-board 8088 microprocessor lets users take full advantage of the open architecture of the MS-DOS environment. A floppy disk supplies adequate storage for setups and data, while expansion slots let users add more storage, a mouse or another pointer device.

Analyzers that grow

Modularity is a key feature to preserving user investment in sophisticated test instrumentation. Manufacturers of most product lines expect users to purchase higher performing instruments as their needs grow. A new low-cost logic analyzer from Tektronix (Beaverton, OR) at-

(continued on page 153)

John H. Mayer
Senior Associate Editor

WITH THE WRONG ASIC DESIGN TOOLS, YOU COULD BLOW THE WHOLE PROJECT.

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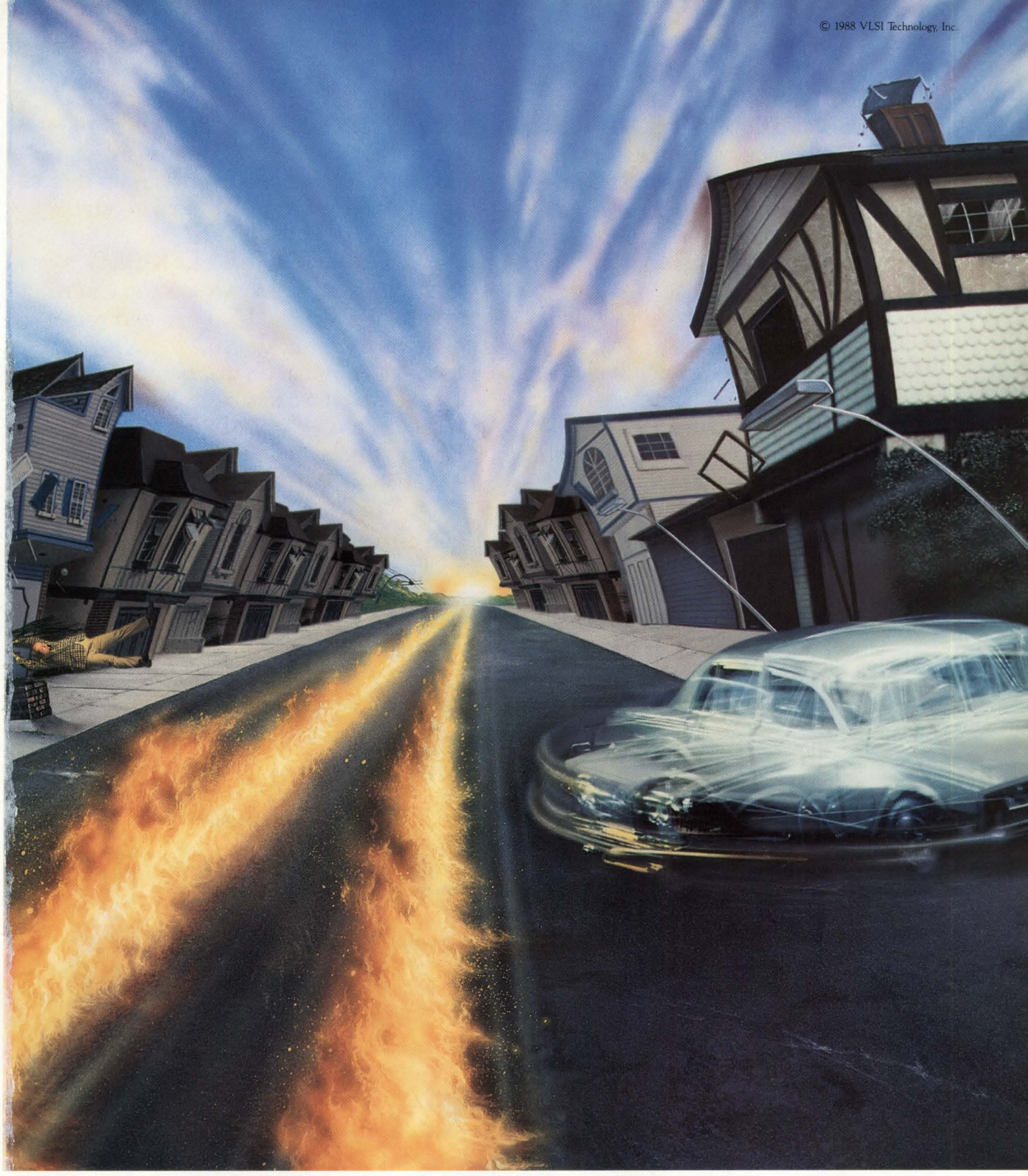

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tion, and packaging possibilities. In short, it tells you the best silicon solution to your problem.

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Gate array, standard cell or cell-based.

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And we've got a couple of "expert" compilers for cell-based or gate array designs that think exactly the way you do.

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Only our Portable Library lets you choose gate array or cell-based, 1.5μ or 2μ, *after* you've completed your logic design.

It can allow you to do that because your library always remains stable. No matter what process you use.

Process obsolescence is now obsolete.

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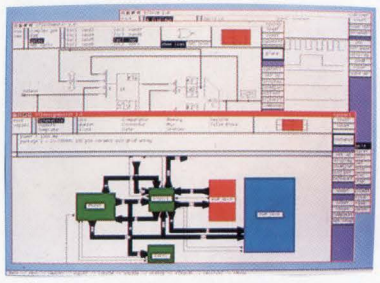
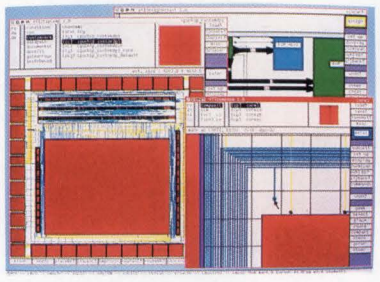


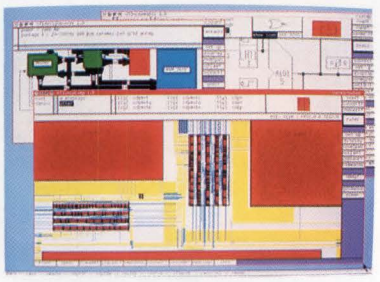
The Concept Express Design System's highly productive logic tools and silicon compilers were used to develop this very-large-scale ASIC. It incorporates a 2901 datapath, RAM, ROM, and over 3,400 gates of random logic.

DESIGN EXPRESS™:



This highly-integrated design combines control logic, a register file, a refresh counter, and five peripheral chips onto a die size of 275x315 mils. The logic design, layout, and verification were completed in only 12 weeks.

SILICON EXPRESS™:



This design integrates all the peripheral chips for an AT computer with six megacells and control logic. Using the Silicon Express Design System, logic and physical designs like these can be implemented in under two man months.

VLSI TECHNOLOGY, INC.

Using ECL technology, the Philips PM 3655 logic analyzer delivers 100-MHz performance on up to 96 channels. The analyzer, which is marketed by John Fluke Mfg, uses a high-speed instrumentation bus for logic analyzer functions and a standard PC XT bus for data processing and interface operations.

Logic analyzers...

(continued from page 146)

tempts to circumvent that expense. Targeted to such divergent needs as those of educators, service technicians and development engineers, the 1230 brings the modular architectures found in Tektronix's high-level logic analyzers down to the $3,000 level.

A basic 1230 is a self-contained, portable unit with 16 acquisition channels. By simply plugging in additional 16-channel cards, users can increase their system to 32, 48 or 64 channels. "For users expecting to move from 8- to 16-bit analysis, the 1230 makes that move a lot less painful," explains Chuck Wiley, marketing manager for Tektronix. Triggering is provided in two forms. In "basic" mode, the unit supplies 14 levels of if-then statements. For more sophisticated routines, an "advanced" function lets each of the 14 levels use if-then-else statements to track branching in real time.

The instrument's feature set simplifies the process of searching for intermittent system faults. Each channel is backed by four 2-kword-deep memories. An auto-compare mode lets users make single or repeated comparisons between any two memories and automatically identifies discrepancies between expected and acquired values. In addition, the availability of up to four time bases lets users observe data from different parts of a system, with each clocked separately.

Ease-of-use becomes critical

Just as modularity has attracted logic analyzer users, ease-of-use has become a critical feature in any low-cost instrument. Simplified operation has contributed significantly to the popularity of logic analyzers such as the ML4100 from Arium (Anaheim, CA). That instrument's menu-driven, coordinated display formats and single-key access to all screens let users easily switch between timing, state and disassembly modes while maintaining the same position in the data buffer relative to the trigger event.

Those same features are found in the company's new ML4400. To the original feature set, the ML4400 adds the ability to analyze up to four different processors, as well as supply disassembly and time-align functions. Built in a modular chassis, the ML4400 can be configured to provide up to 16 channels at 400 MHz, 64 channels at 100 MHz (synchronous) or 160 channels at 50 MHz. Prices start at $4,995.

Another new low-priced ($2,995) unit comes from Gould (Cleveland, OH). Designed for users of 8- and 16-bit microprocessors and TTL, Gould's K25 delivers 32 channels with internal and external clock rates to 25 MHz. Memory is 1-ksample deep per channel. The logic analyzer features four levels of triggering with restart, plus event and delay count. In addition, disassembly support is available for virtually every major microprocessor.

The K25 uses a softkey-controlled display to ease first-time use. In timing mode, the analyzer displays any 17 channels or scales and lets users label each channel. In list mode, up to 32 channels can be grouped together and given a single character label and name. The analyzer also offers search, compare and find-difference features.

PC compatibility common

Links to the open architecture of the MS-DOS world and its access to software for data analysis and word processing, not to mention CAE systems, are becoming virtually mandatory on logic analyzers. Few, if any, analyzers go as far as the Philips PM 3655 with its two-bus architecture, one for high-speed instrumentation and the other for a standard PC. But a number of analyzers provide a closer integration to the PC environment than the performance-restricted PC cards found at the lowest price levels.

The PLA-286 line from Kontron Electronics (Mountain View, CA) integrates the functionality of a 10-MHz 80286-based PC into its logic analyzer. The PLA-286 provides either 48 or 96 state channels at 20 MHz and 8 or 16 timing channels at 100 MHz, depending on configuration. Dolch American Instruments (San Jose, CA) ventures a step fur-

Low-cost logic analyzers

Model	Maximum Synchronous Clock Rate (MHz)	Maximum Asynchronous Clock Rate (MHz)	Maximum Number of Channels (State/Timing)	Number of Channels at Maximum Sample Rate (state/timing)	Memory Depth/Channel (bits)	Triggering Levels	Minimum Glitch Capture (ns)	Price ($)	Comments
Arium 1931 Wright Cir, Anaheim, CA 92806 (800) 562-7486									**Circle 100**
ML4400	100	400	160/320	80	2k to 32k	8	5	$4,999	cross trigger, time stamp
ML4400S	50	100	80	40/20	8k	8	5 (opt)	$4,995	expandable to multicards
ML4400/L	71	100	32	32/4	1k to 8k	4	5 (opt)	$2,495	μP support opt.
ML4100/X	71	100	32	32/4	1k to 8k	4	5 (opt)	$3,295	nonvolatile setup, search, compare
ML4100/8	71	100	32	32/4	1k to 8k	4	5 (opt)	$3,685	supports 8-bit μPs
ML4100/16	71	100	62	62/4	0.5k to 8k	4	5 (opt)	$4,850	supports 16-bit μPs
Array Analysis 200 Langmuir Lab, Brown Rd, Ithaca, NY 14850 (800) 451-8514									**Circle 101**
System A	25	25	32/32	32	1k	1	—	$2,985	standalone modules
System H	50	50	96	96	2k to 8k	14	—	$6,270	expands to 1,536 channels
GFT-2E	200	25	128	64	1k to 8k	14	3	$8,712	diagnostic expert system
Bitwise Designs 297 River St, Suite 501, Troy, NY 12180 (518) 274-0755									**Circle 102**
System-40	25	125	40/40	40/8	4k	16	—	$2,995	PC XT-compatible
System-80	25	125	40/40	80/16	4k	16	—	$6,000	PC AT-compatible
Dolch American Instruments 2029 O'Toole Ave, San Jose, CA 95131 (408) 435-1881									**Circle 103**
Cobra PA480	25	100	48/48	12/12	4k	16	5	$5,365	built-in 286 or 386 PC
El Toro Systems 23702-B Birtcher Dr, El Toro, CA 92630 (714) 770-1474									**Circle 104**
PC-29	50	50	24/24	24/24	1k	1	—	$749	PC card, software
PC-52	25	100	24/24	24/6	1k to 4k	1	—	$1,299	variable threshold
PC-27200	50	200	24/24	24/6	4k to 16k	16	—	—	same as 27100, 200 MHz
Gould, Test & Measurement 19050 Pruneridge Ave, Cupertino, CA 95014 (800) 538-9320									**Circle 105**
K25	25	25	32/32	32/32	1k	4	—	$2,995	16 setups, ref. memory
K50	50	100	32/32	16/8	1k to 4k	4	5	$3,995	16 setups, active probes, ref. memory
K115	70	200	64	16/8	1k	8	5	$9,995	ref. memory
Hewlett-Packard 1820 Embarcadero Rd, Palo Alto, CA 94303 Call local sales office.									**Circle 106**
HP 1651A	25	100	32/32	32/32	1k	8	5	$3,900	disk drive, time tagging, supports 8-bit μPs
HP 1650A	25	100	80/80	80/80	1k	8	5	$7,800	disk drive, time tagging, supports 8-, 16-, 32-bit μPs
Iwatsu Instruments 430 Commerce Blvd, Carlstadt, NJ 07072 (201) 935-5220									**Circle 107**
SL4121	20	100	16	16/16	8k	4	3	$4,200	saves 10 setups, compact
SL4620	10	200	95	80/8	2k	4	3	$10,400	10 setups; μP disassembly
John Fluke Mfg, Philips T&M Products PO Box C9090, Everett, WA 98206 (800) 443-5853									**Circle 108**
PM 3655	100	100	96/96	96/96	2k	4	5	$9,950	built-in PC, 24-channel expansion cards

Key: ch.=channel; gen.=generation; opt.=optional; ref.=reference

Now benchpress 400 MHz. Easy.

Arium introduces The Tool for your bench. The 400 MHz logic analyzer at a price you can handle as easily as the ML4400 handles multiple pods simultaneously . . . starting at $4995.

Arium does it again.

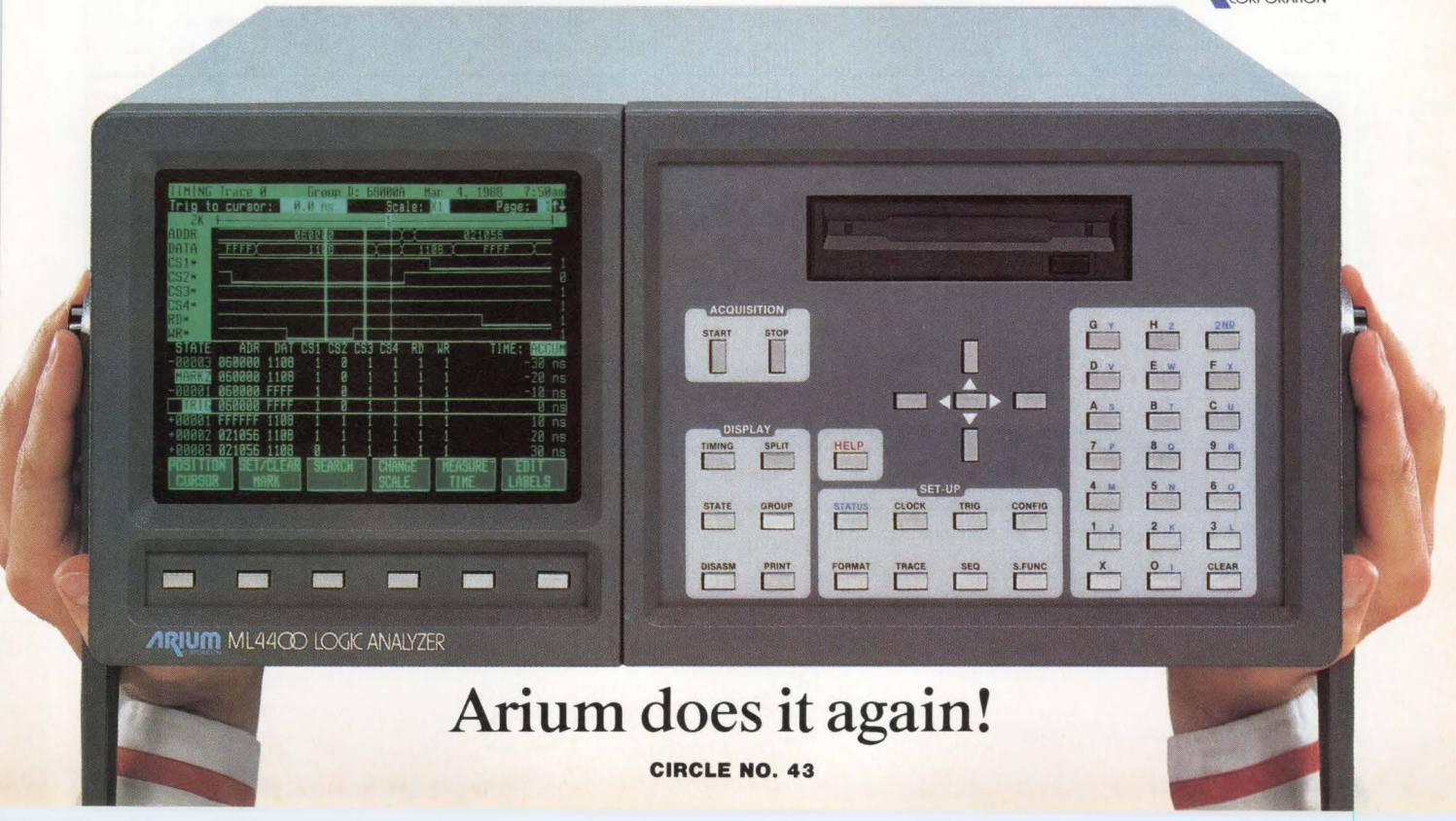
We just redefined high-end logic analyzers in terms of low-end cost. With the 8/16/32-bit ML4400, you can combine up to four independent-clock cards (user-selectable) to get 16 channels at 400 MHz, 64 channels at 100 MHz (synchronous), or 160 at 50 MHz (synchronous). That means you can now handle full-speed 68030s or 80386s, as well as 68020s and 8086s. And, uniquely, up to four different microprocessors, simultaneously. That's speed our competition can't catch up with. Now for ease of use.

Easy. Redefined. What does ease of use mean to you? If it means: Single key menu access to all screens. Complex triggering (Boolean, multilevel, repeat functions) with cross-triggering between state and timing, and between pods. Cross-time stamping. Transitional timing. All software resident . . . Then, you'll find them all, and more, in the ML4400.

Why Arium? How can Arium be the first to put this much low-cost power on your bench? Because we've always been first, ever since we redefined performance/price logic analyzers with our ML4100. When will the competition catch up with the performance/price of our new ML4400? Don't hold your breath.

For more data on the new ML4400, as well as on our family of Arium 8/16/32-bit logic analyzers at prices as low as $2495, contact ARIUM CORPORATION, 1931 Wright Circle, Anaheim, CA 92806-6052. Telephone 800/TO-ARIUM (800/862-7486), (714/978-9531 in CA).

ARIUM CORPORATION



Arium does it again!

CIRCLE NO. 43

Model	Maximum Synchronous Clock Rate (MHz)	Maximum Asynchronous Clock Rate (MHz)	Maximum Number of Channels (State/Timing)	Number of Channels at Maximum Sample Rate (state/timing)	Memory Depth/Channel (bits)	Triggering Levels	Minimum Glitch Capture (ns)	Price ($)	Comments
Kontron Electronics 630 Clyde Ave, Mountain View, CA 94039 (800) 227-8834									**Circle 109**
PLA286-01	20	20	48	48	4k	14	—	$7,400	built-in PC AT, disassembler, pattern gen.
PLA286-02	20	20	48	48	4k	14	—	$9,900	built-in PC AT, 20-Mbyte hard drive
PLA286-03	20	100	48/8	48/8	4k/8k	14/2	10	$9,300	built-in PC AT, dissemblers, pattern gen. opt.
Microcase PO Box 1309, Beaverton, OR 97075 (800) 547-4445									**Circle 110**
LAN-AIU	10	100	32/16	32/16	4k	15	5	$6,450	PC-controlled, time aligned state & timing
LAN-16IU	10	100	48/16	48/16	4k	15	5	$7,985	same as above
LAN-32IU	10	100	80/16	80/16	4k	15	5	$9,370	same as above
Orion Instruments 702 Marshall St, Redwood City, CA 94063 (415) 361-8883									**Circle 111**
Omnilab 9210	34	204	48	8	4k	—	5	$5,800	combined PC-based analyzer/stimulus
Omnilab 9240	34	680	48	2	4k	—	5	$8,900	combined analyzer/scope/stimulus
Panasonic Factory Automation 2 Panasonic Way, MS 7G-1, Secaucus, NJ 07094 (201) 392-4050									**Circle 112**
VP-3621P	20	20	32/16	32	1k	4	10	$5,200	8-, 16-bit μP disassembly
VP-3663P	100	100	48/32	16	1k	4	5	$9,800	same as above
Rapid Systems 433 North 34th St, Seattle, WA 98103 (206) 547-8311									**Circle 113**
R3000	20	20	16	16	1k	6	10	$1,995	PC-based, pattern gen. opt.
R3020	10	10	32	32	0.5k	6	10	$3,495	PC-based, pattern gen. opt.
Soltec Sol Vista Park, San Fernando, CA 91340 (800) 423-2344									**Circle 114**
PLA 3300	10	10	16	16	0.256k	16	15 ms	$2,495	battery-powered, timing, state & signature analysis
PC-27100	50	100	24/24	24/6	4k to 16k	16	—	—	expansion boards to 72 ch
Tektronix PO Box 500, Beaverton, OR 97077 (503) 629-1359									**Circle 115**
1205	9	100	24/8	2	2k to 24k	3	10	$2,495	video out
1230	25	100	64/64	16	4×2k	14	5	$2,795	user-installable modules, video out, auto-compare
1240	50	100	72/72	72/36	0.5k to 2k	14	6	$7,450	supports 45 μPs, μCs, DSPs
Total Logic 585 Burbank St, Unit A, Broomfield, CO 80020 (303) 460-0118									**Circle 116**
LA-200	100	100	32/32	4/4	1k to 8k	8	—	$1,995	PC card

Key: ch.=channel; gen.=generation; opt.=optional; ref.=reference

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CIRCLE NO. 44

ther and houses its single-card unit in a portable PC powered by a 20-MHz 80386. The company's Cobra 386 is reputed to be one of the fastest portable 386s on the market. Long a major supplier of digital test equipment, Dolch offers a range of instrumentation modules for the PC's six slots, including digital pattern generators and oscilloscopes.

For designers working with hybrids or mixed-signal ICs, the Omnilab 9240 from Orion Instruments (Redwood City, CA) combines the resources of a 200-Msample/s logic analyzer with a 100-MHz digital oscilloscope and synchronized analog and digital stimulus generators. The instruments are packaged in a foot-high, 5- × 17-in. box that carries its own power supply and I/O channels. Multiple instruments can reside on a proprietary O-bus that links to a PC via an interface card and ribbon cable.

Besides its unique architecture, the Omnilab adds an innovative triggering scheme. Called Select, the synchronized system combines conventional oscilloscope and logic analyzer triggering with RAM truth tables. The configuration is particularly useful for finding rarely occurring events such as buried noise glitches or missing pulses.

For test-monitoring environments or performance testing of a microprocessor-based system over long periods of time, Bitwise Designs (Troy, NY) offers a logic analysis system that collects up to 64 kwords of data. The system features 25-MHz state and 125-MHz timing analysis, 16-level trigger sequencing, memory-mapped word recognition and 256-state pass counting. The IBM PC AT-compatible system comes in a basic configuration of 80 channels with 4 kwords of memory per channel, but can expand to 320 channels and 64 kwords of memory. A menu-based, multitasking, windowing environment, based on Microsoft Windows, simultaneously displays multiple timing diagrams, state tables, performance histograms, disassembled code, trigger setups and system configuration. **CD**

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CIRCLE NO. 46

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Design Automation Conference reflects explosive industry growth

The Design Automation Conference (DAC), which is celebrating its 25th anniversary this year, has undergone dramatic changes in recent years. The premier trade show of the electronic design automation (EDA) industry was originally just an academic conference. But exhibits began to appear in the early 1980s with a handful of companies displaying plans for future products. Today, the DAC is a burgeoning trade show. Over 100 companies will exhibit real products at this year's show, to be held June 12-16 in Anaheim, CA.

While the EDA industry has been marked by a growing number of suppliers, the impact of recent mergers and acquisitions will also be evident on the exhibit floor. Case Technology (Mountain View, CA) and Aida (Santa Clara, CA), for example, for the first time will be exhibiting as subsidiaries of Teradyne (Boston, MA). The acquisition of Simucad (Menlo Park, CA) by HHB Systems (Mahwah, NJ) and the recent merger of ECAD (Santa Clara, CA) with SDA Systems (San Jose, CA) will also be reflected in the exhibits.

New technologies featured

Logic synthesis, a new technology that maps high-level design descriptions into low-level schematics and net lists (see "Logic-synthesis tools forge link between behavior and structure" on p 65), will be a hot topic at the DAC. Two new companies, Synopsys (Mountain View, CA) and Silc Technologies (Burlington, MA), will introduce commercialized toolsets for logic synthesis. Both Synopsys' Design Compiler and Silc's Silcsyn accept inputs from high-level design descriptions, synthesize combinational or sequential logic, and use rule-based algorithms to map logic into commercial application-specific IC cell libraries.

Another logic-synthesis company, Trimeter (Pittsburgh, PA), will also introduce a high-level synthesis tool at the DAC. And NCR Microelectronics (Fort Collins, CO) will demonstrate its own version of Silcsyn, enhanced with rules for NCR's standard-cell libraries.

The VHSIC Hardware Description Language (VHDL) is another key topic this year, and Vantage Analysis Systems (Fremont, CA) will exhibit its Vantage Spreadsheet, a simulator that fully implements the IEEE standard VHDL 1076. Endot (Cleveland, OH), meanwhile, will introduce a VHDL system design and analysis toolset, similar to its N.2 product. VHDL support tools will also be exhibited by Intermetrics (Cambridge, MA) and Cad Language Systems (Potomac, MD).

A number of simulation tools will also be introduced. Among them is System Hilo, the successor to the Hilo-3 simulator from Genrad (Santa Clara, CA). Enhancements over Hilo-3 include an expanded hardware-description language, a new stimulus programming language and a new timing-analysis module. Hewlett-Packard (Palo Alto, CA) is among the OEM vendors that will announce support for System Hilo.

As a supplement to its Quicksim simulator, Mentor Graphics (Beaverton, OR) will introduce Quickpath, a critical path analyzer that provides worst-case timing verification for ASICs and printed circuit boards. And in a joint effort, Analogy (Beaverton, OR) and HHB Systems will demonstrate Saber/Cadat, a mixed-mode simulation environment that can handle behavioral modeling for both analog and digital components. Valid Logic (San Jose, CA) will introduce a new analog simulation environment that emulates common laboratory instruments.

Stressing the importance of design/test integration, Gateway Design Automation (Westford, MA) will introduce its Verifault-XL fault simulator, which is based on its Verilog hardware-description language. Valid Logic will introduce a fault simulator too. Its fault simulator lets users vary the fault coverage, trading off execution speed for accuracy.

To make prototype verification easier, Integrated Measurement Systems (Beaverton, OR) will announce a Characterization and Timing Analysis software package that lets users control IMS' Logic Master testers from a spreadsheet environment. This tool provides menu-driven routines for propagation delay, setup time, hold time and Shmoo plotting.

A new company, Descartes (Santa Clara, CA), will demonstrate a sea-of-gates layout system aimed at large gate arrays. The system is primarily sold through foundries and is customized for each user.

CASE tools too

Although the DAC has traditionally been aimed at hardware designers, software-development tools are beginning to appear. Cadre Technologies (Providence, RI) and Interactive Development Environments (San Francisco, CA) will show their structured analysis and design tools for computer-aided software engineering. I-Logix (Burlington, MA) will display its Statemate system, a graphical tool for real-time system specification. And Hewlett-Packard will introduce in-circuit emulators for digital signal processors from Texas Instruments (Austin, TX).

Following is a closer look at a few of the products to be introduced at, or just before, the trade show. For more information on any of these products, circle the reader service numbers provided. **CD**

Richard Goering
Senior Editor

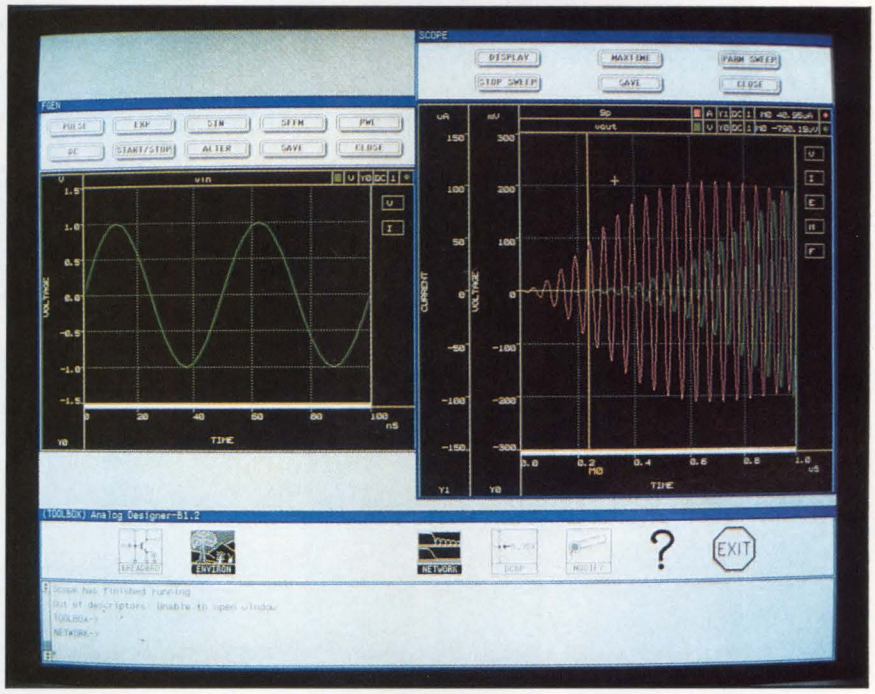
Analog design toolset features open architecture

A second-generation enhancement of Valid Logic's Analog Designer uses an open architecture that will let Valid add new tools and capabilities. Called Advantage, the system also provides an enhanced user interface, includes more library development tools, and offers a new documentation capability that lets users print schematics and waveforms.

Like the Analog Designer, Advantage uses the Precise circuit simulator from Electrical Engineering Software (Santa Clara, CA). Based on the Spice circuit simulator from the University of California at Berkeley, Precise offers improved convergence and up to three times the speed of standard Spice.

The user interface emulates common laboratory instruments, such as a function generator, an oscilloscope and a network analyzer. Designers use Valid's GED schematic editor to create a schematic, which is compiled for simulation. A function generator icon lets users apply different types of stimulus to the circuit, such as pulse, exponential, sinusoidal, single-frequency, frequency-modulation and piece-wise linear.

A scope icon lets users generate plots and measure the time-domain response of a circuit. The network



icon can be used to measure the frequency-domain response of a circuit. And a dc-operating-point icon can find the dc operating point of a given node and evaluate the proper biasing for the circuit.

A probe function lets users point at nodes in the design and get information. A new feature, the expression probe, lets users assign mathematical expressions to probes.

The open architecture will let Valid add such tools as mixed-mode analog/digital simulation in the future. Advantage will be available in July at an average price of $50,000 on Sun or VAX workstations.

Valid Logic Systems, 2820 Orchard Pkwy, San Jose, CA 95134.

Circle 155

Emulators support digital signal processors

By providing in-circuit emulation for the Texas Instruments TMS-32020 and TMS320C25 digital signal processors, the HP64786A/AL and 64787A/AL products are among the first emulators to break into the DSP arena. The HP64786 supports the TMS32020 up to 20 MHz with no wait states, while the HP64787 runs at 32 MHz with no wait states for the TMS320C25.

These host-independent emulators are members of the HP64700 series, which are normally controlled by an IBM PC or compatible. The emulators have 64 kwords of high-speed, dual-port emulation memory. This dual-port memory allows emulation displays and modifications of the emulation memory without having to halt the processor during emulation. Memory can be mapped in 1-kbyte blocks.

Each emulator has an internal logic analyzer for tracing DSP code flow. The 64786AL and 64787AL models also include a 16-channel external logic analyzer that can be configured for asynchronous 100-MHz timing analysis, 25-MHz state analysis, or slave analysis coupled with the emulation analyzer. The external analyzer has full triggering and storage qualification capabilities.

For designs that involve multiple processors, a Coordinated Measurement Bus permits synchronization and cross-triggering of up to 32 HP-64700 series emulators. Prices range from $13,300 for the HP64786A emulator to $16,500 for the HP64787-AL emulator.

Hewlett-Packard, 3495 Deer Creek Rd, Palo Alto, CA 94034.

Circle 156

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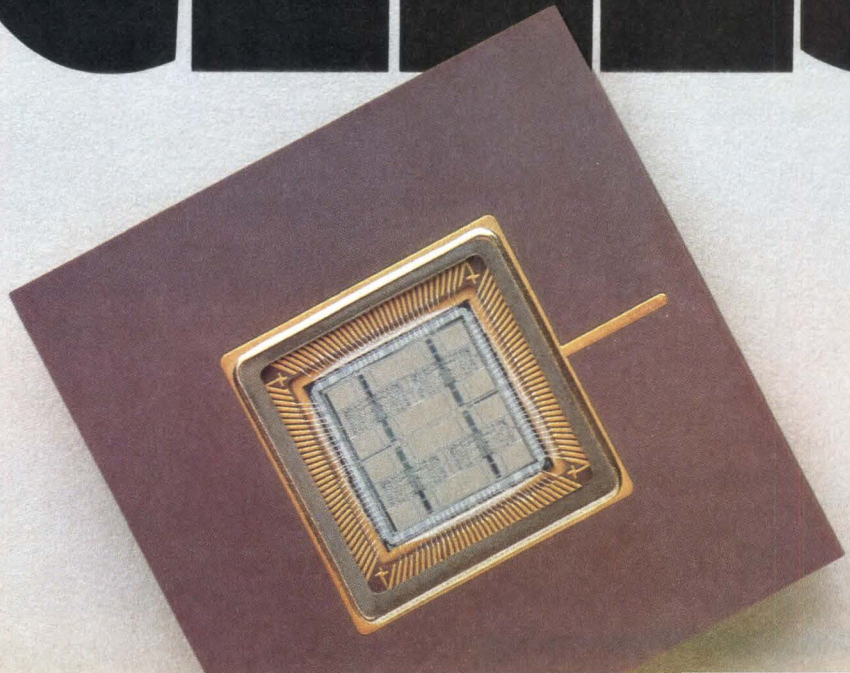

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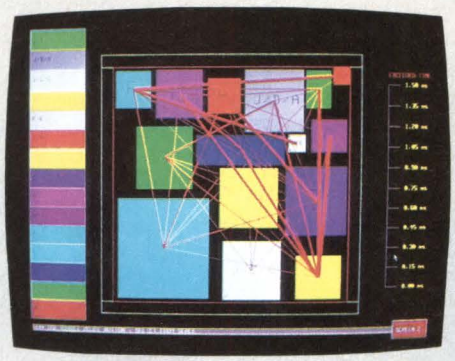

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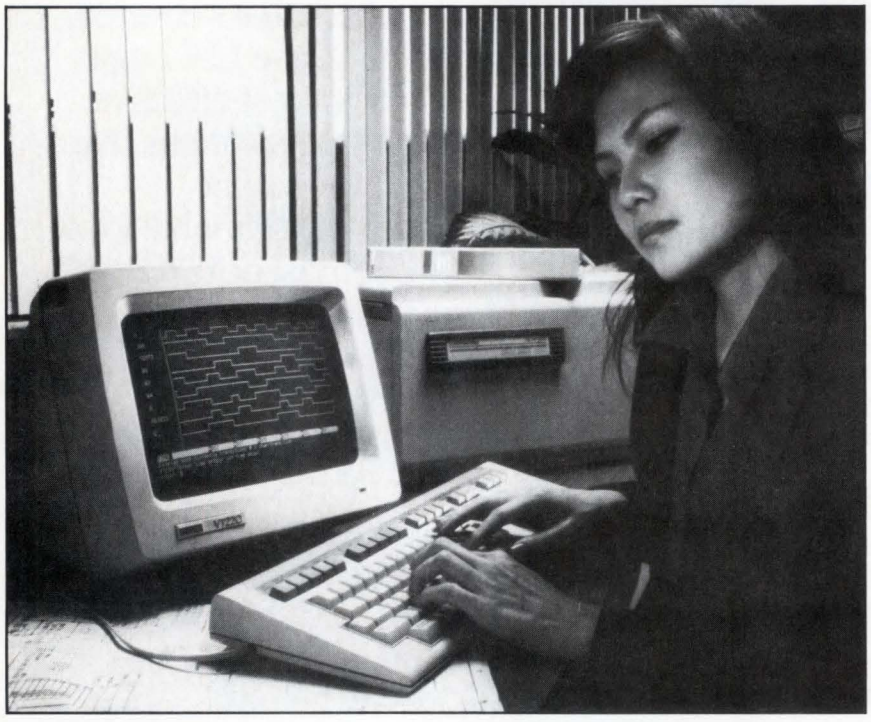
CIRCLE NO. 47

Modular simulation toolset provides flexibility

A next-generation successor to the Hilo-3 simulator, System Hilo provides a broad toolset for design verification, fault simulation, timing analysis, test generation, simulation modeling and library access. The modular architecture of System Hilo lets users mix and match specific capabilities, while all tools run under a common user interface and support common hardware- and waveform-description languages.

The Hisim logic simulation and Hifault fault simulation modules are essentially the same as their Hilo-3 counterparts, although the company claims a performance increase for both modules. The Hitime module provides a dual-delay (minimum/maximum) timing verifier that finds potential problems caused by component timing variations. A trace-back option lets users determine the stimulus vector causing the error.



Hitest provides automatic test-pattern generation when built-in testability structures are used; otherwise, it provides interactive test development. Hipost provides postprocessors for Genrad test equipment.

The GHDL hardware description language enhances its Hilo-3 predecessor with additional primitive elements at the switch, gate and functional levels. A new waveform description language, DWL, provides high-level stimulus programming for System Hilo. DWL is a block-structured language that supports basic looping and conditional branching, as well as parametized procedures and concurrent processes.

The Hilib component library includes over 6,000 parts, and the Higen library generation tool supplies parametized component modules to help users build application-specific IC libraries. Additional modeling capabilities are available through the Hichip hardware modeling system, as well as through an external modeling interface that lets users import third-party behavioral models. Available in July, System Hilo runs on workstations from Apollo Computer, Sun Microsystems, IBM, Digital Equipment Corp, Hewlett-Packard and Intergraph. Prices start at $10,000.

Genrad, 300 Baker Ave, Concord, MA 01742. **Circle 157**

Critical path analyzer displays timing violations

A graphical critical path analyzer provides a true worst-case, minimum/maximum timing analysis for application-specific IC and board designs. An addition to Mentor Graphics' Quicksim simulator, the Quickpath timing analyzer detects any path that's too fast or too slow, highlighting violations directly on the schematic for easy recognition.

Quickpath automatically calculates delays along paths between clocked elements, compares the path delay with clock specifications, and identifies all setup and hold violations. It also supports multiphase and multifrequency clocks, and removes common ambiguity to avoid overly pessimistic simulation results. Unlike most minimum/maximum timing simulators, Quickpath finds all possible setup and hold violations without stimulus vectors.

Quickpath can identify areas where the ASIC's performance can be optimized. Slow paths are identified and highlighted directly on the schematic. On the board level, Quickpath provides a worst-case analysis based on the minimum and maximum timing specifications for each component on the board. All setup and hold violations caused by combinations of fast and slow components are highlighted.

Available by the end of the year, Quickpath works with all modeling types, including gate-level, behavioral and hardware models.

Mentor Graphics, 8500 SW Creekside Pl, Beaverton, OR 97005. **Circle 158**

Revisions enhance PCB design package

A new revision improves the simulation and printed circuit board routing capabilities of the electronics design software of Computervision. Enhancements of Revision 3.3 include a new timing verifier, the integration of third-party analog and digital simulators, and the repositioning of algorithms for printed circuit board layout.

Part of the schematic design module, the dynamic timing verifier locates timing errors such as race conditions, static and dynamic hazards, setup and hold violations, reconvergent fan-out problems and minimum pulse-width violations. Further verification is provided with the Cadat digital logic simulator from HHB Systems (Mahwah, NJ) and the Saber analog simulator from Analogy (Beaverton, OR).

New routing algorithms in the Autoboard SMT module provide dynamic recursive repositioning of traces and vias. During interactive editing, the software will automatically reposition traces as new circuitry is added. Layout enhancements for analog circuits are included, and a new drafting package is available.

Computervision, 100 Crosby Dr, Bedford, MA 01730. **Circle 159**

Fault simulator uses hardware description language

A fault simulator based on the Verilog hardware description language from Gateway Design Automation can propagate faults through behavioral models created with this language. The Verifault-XL simulator also uses Gateway's XL algorithm, which claims significant speed advantages without using special-purpose hardware.

The Verilog language supports design descriptions from the architectural level to the gate and switch levels. Passing faults through behavioral models is much faster than passing faults through gate-level or switch-level models. Other fault simulators that offer behavioral propagation generally use the C language for building behavioral models. But this approach is more difficult than using a hardware description language, and it limits the behavioral fault simulation to serial processing.

Verifault-XL is a concurrent fault simulator that uses the XL algorithm, which is said to produce speed increases three to 25 times over other software simulators. The XL algorithm uses an adaptive behavioral recognition technique that's an advanced form of clock supression. For a further speed increase, Verifault-XL can be distributed over a network of workstations, where runtime speedup is directly proportional to each additional workstation.

Available in July, Verifault-XL will be sold in conjunction with the Verilog-XL logic simulator. Prices start at $30,000 for existing Verilog-XL users.

Gateway Design Automation, 6 Lyberty Way, Westford, MA 01886. **Circle 160**

Coming June 15

Look for Contributing Editor Steven Martin's technology focus report on peripheral controller ICs and for Contributing Editor Art DeSena's technology focus report on IC testing.

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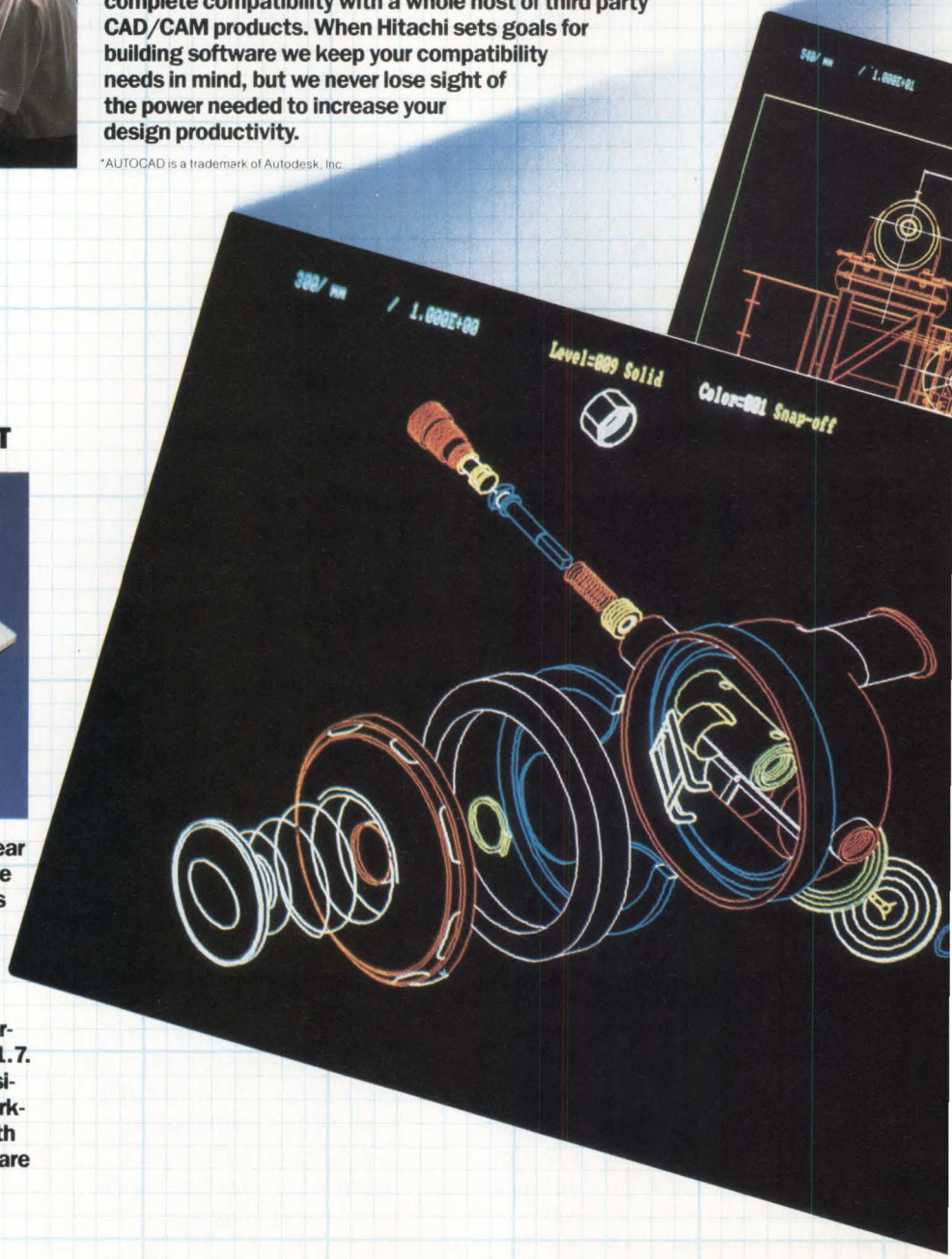
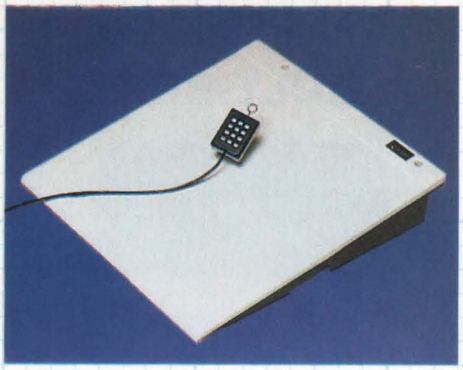


HDG-1212D DIGITIZER TABLET



The new Puma Pro comes with a 10 year warranty, as a sign that this product is the ultimate in reliability. Over 200,000 hours MTBF, high accuracy of ± 20 mils and standard features like a 1 button stylus pen, AC adaptor, 4 button or 12 button cursor, cable and RS232C interface make it one of the leading tablets in America. The actual digitizing area is 11.7 × 11.7. You'll undoubtedly find this one of the easiest, most convenient and pleasurable working tools in your office. It's compatible with Hitachi's software and all Hitachi tablets are supported by most programs.

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HITACHI®

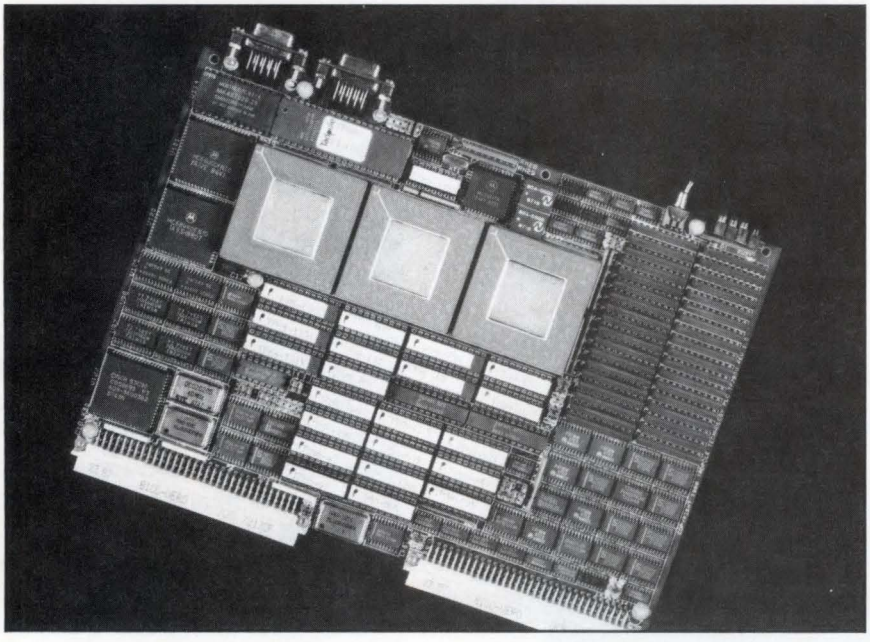
CIRCLE NO. 53

Single-board computer uses Motorola RISC processor

Two single-board computers based on the Motorola 88000 come complete with an optimizing C compiler. The TP880V is based on a VMEbus architecture, while the TP880M supports Multibus II.

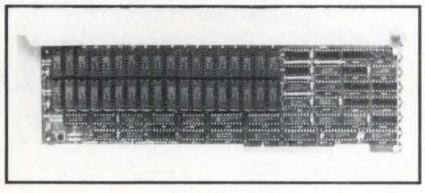
Two 88200 cache memory management unit devices are implemented on the TP880V, one for the instruction bus and one for the data bus, providing an environment suitable for implementing Unix. The TP880V, which has 4 Mbytes of on-board memory, is byte-parity protected and is ported between the main processor, the VMEbus and the on-board I/O subsystem bus.

The memory interface uses nibble-mode dynamic RAMs to support burst fill of the 82000 cache line. A subsystem bus is provided to offload most of the I/O requirements from the 88100 processor. Featuring an MC68000 CPU and an MC68440 direct memory access controller, the bus provides a small computer system interface (SCSI) to support a range of peripheral devices. Other facilities include two RS-232 ports; 128-kbyte EPROM; battery-backed, real-time clock; and 16-kbyte static RAM accessed with zero wait states. The SRAM and EPROM spaces let the I/O executive operate without access to the main on-board system memory, while the subsystem interfaces to the host through a dual-ported area of main system memory.



The functionality of the TP880M is similar to that of the TP880V. The I/O subsystem is provided with Ethernet, a SCSI, four RS-232 ports, up to 128 kbytes of EPROM and 64 kbytes of SRAM accessed with zero wait states. The Multibus II iPSB interface is implemented using the Intel Message Passing Coprocessor at up to 32 Mbytes/s.

Both products are supported by the Tadpole C Development System, a C compiler for Unix and standalone environments designed for the 88100 processor providing Kernighan and Ritchie and ANSI C support. The benchmark performance of the TP880V using fully optimized code exceeds 45,000 Dhrystones at 20 MHz. The TP880 runs the Unix System V.3.1 operating system. **Tadpole Technology,** 6747K Sierra Court, Dublin, CA 94568. **Circle 134**



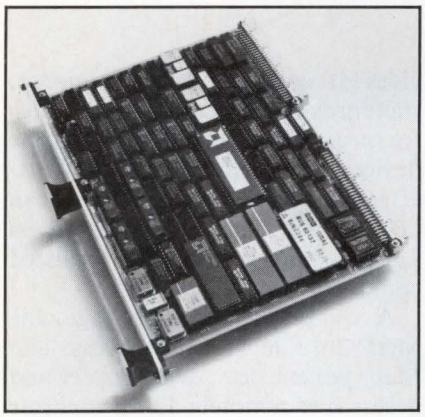
Memory board for IBM PS/2 expandable to 4 Mbytes

The BocaRAM 50/60 is a microchannel-architecture memory board that supports OS/2 multitasking features with up to 4 Mbytes. The 1- and 2-Mbyte configurations are expandable to 4 Mbytes by adding 1-Mbit, 120-ns dynamic RAM chips. A menu-driven installation program and diagnostics package are included to provide proper board functioning. Prices are $645, $995 and $1,695 for the 1-, 2- and 4-Mbyte versions, respectively. An unpopulated version is available for $295. **Boca Research,** 6401 Congress Ave, Boca Raton, FL 33487.

Circle 135

Intelligent VMEbus I/O processor runs at 25 MHz

The GMSV07-SYS-G is a 32-bit, intelligent I/O processor board running at 25 MHz with a direct memory access driven IEEE-488 interface, a small computer system interface port, a parallel port, two serial ports and a real-time clock. The board uses a 68020 processor and a 68881 coprocessor, a Z8536 programmable configuration controller and a 68155 bus-interrupt manager, and features 1 Mbyte of on-board RAM augmented with 1 Mbyte of dynamic RAM. Optional memory configurations can include up to 1 Mbyte of EPROM or 128 kbytes of EEPROM. Operating systems available with the V07 include PDOS, PSOS, VRTX and OS-9. Prices begin at $2,692. **General Micro Systems,** 4740 Brooks St, Montclair, CA 91763. **Circle 136**

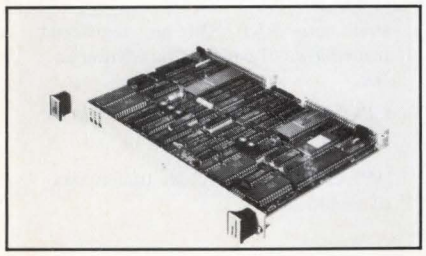


Intelligent MIL-STD 1553B interfaces with VMEbus

The SVME-653 offers dual-redundant 1553-bus interfaces, a bit-slice microprocessor and 64 kbytes of dual-ported memory. VME host software can select either bus control or remote terminal operation by initializing the SVME-653 as one type or the other. The dual-ported memory is accessible to the on-board processor and the VMEbus. Separate data-exchange areas are allocated within this memory for the transmit and receive directions of each 1553B subaddress. The location of data-exchange areas can be programmed by the host, along with the size and number of buffers in each area. **DY-4 Systems,** 21 Credit Union Way, Nepean, Ontario, K2H9G1. **Circle 137**

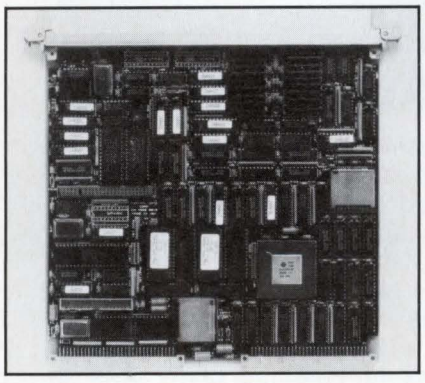
Interface board provides 4-Mbyte transfer rate

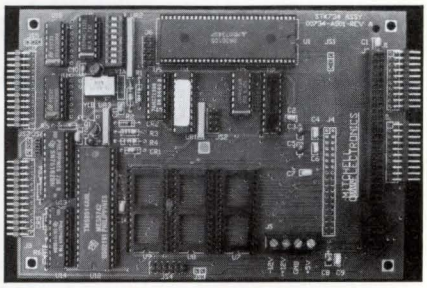
The PME SCSI-1A interface board is fully compatible with the ANSI X3T9.2 small computer system interface (SCSI) and can provide asynchronous data transfers at up to 4 Mbytes/s. The SCSI-1A handles up to 16 concurrent tasks, simultaneous VME/SCSI transfers, and direct memory access transfers up to 32 bits wide over the VMEbus via a dual-ported RAM for full protocol handling. All data transfers between VME and SCSI pass through a first-in, first-out buffer store of 512 longwords for maximum throughput and minimum VMEbus loading. A completion bit is set in the command parameter block, which raises a VMEbus interrupt. Interrupt level and vector are software-selectable and can be disabled, with the host polling the "host adapter status word" for completion. The price is $1,495. **Plessey Microsystems,** One Blue Hill Plaza, Pearl River, NY 10965. **Circle 138**



Controller board features CPU and 2-Mbyte RAM

The CD22/4500-2048 controller is a SCSI/ANSI- and SASI-compatible device with a 12.5-MHz, 80186 CPU and 2 Mbytes of parity-protected RAM. Communicating with up to seven SCSI host/peripheral adapters and up to 56 possible devices, the controller delivers maximum data transfer rates of 1.5 Mbytes/s asynchronous and 4 Mbytes synchronous. Four disk-sorting algorithms (first-in, first-out; shortest seek first (SFS); SCAN; and CSCAN) are provided to offload the host disk-processing tasks. The board is priced at $2,400 for quantities of 100. **Central Data,** 1602 Newton Drive, Champaign, IL 61821. **Circle 139**





Single-board computer offers 36 programmable I/O lines

Based on the Mitsubishi M50734 single-chip microcomputer, the Model STK734 single-board computer features an RS-232 port with RS 422 and IEEE 488 offered as options. The device offers 36 programmable parallel lines—some of which also serve as serial I/O—stepper-motor control, pulse-width modulation and an 8-bit analog-to-digital converter, as well as counters and timers that may be used with interrupts. Prices start at $320. **Mitchell Electronics,** 8481 Rock Riffle Road, Athens, OH 45701. **Circle 140**

DSP designed for Sun-3 workstations

Powered by two Texas Instruments TMS32020 chips, the Sky Challenger-S is a single-board arithmetic digital signal processor designed for high-speed applications on Sun-3 workstations. The two chips are configured in a master/slave arrangement, letting the host simultaneously move and process integer data with no wait states. On-board memory, available from 64 to 256 kbytes, is a multiported static RAM mapped into the Sun-3's VME address space, letting the VMEbus and both chips access memory simultaneously. Additional features include a C compiler and a flexible, 16-bit parallel I/O interface. Price is $5,200. **Sky Computers,** Foot of St. John St, Lowell, MA 01852. **Circle 141**

Coming June 15

Look for the Product Focus Report on fiberoptic devices.

HP networking products meet MAP 3.0 specs

Conforming to the Manufacturing Automation Protocol (MAP) 3.0 specifications for factory communications, five manufacturing networking products help Hewlett-Packard computer users communicate with multivendor devices.

The first product, the MAP 3.0 Manufacturing Message Specification (MMS) software package, provides HP users with an international, standards-based command language for programming MAP-compatible devices on the factory floor. Cost-effective, carrier-band cabling can be used with the MMS software in factory subnetworks for localized communication.

A second software package, the MAP 3.0 File Transfer, Access and Management, lets users transfer and access files remotely across multiple computer systems.

For computer-to-network connection, a VLSI card provides a full MAP interface via either broadband or carrier-band cabling. The OSI Express implements all seven layers of the OSI protocol stack. The card is accompanied by the MAP 3.0 Nodal Management Facility for local computer configuration.

To connect HP products to any non-MAP, RS-232 device on the factory floor, HP's Device Interface System, in conjunction with MAP 3.0 MMS software, provides complete device compatibility.

Finally, a MAP 3.0 Protocol Analyzer monitors network traffic online. When integrated with HP's Openview network-management product, it enhances user control and management of multivendor computer communications on the network. **Hewlett-Packard,** Information Networks Group, 19490 Homestead Rd, Cupertino, CA 95014. **Circle 142**

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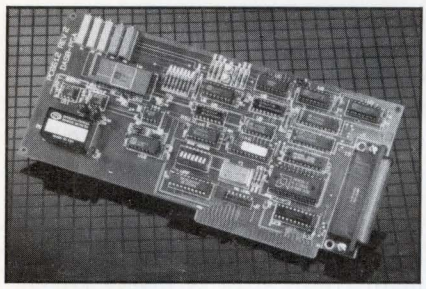


Analog input board offers software-selectable input

An eight-channel, 12-bit analog input board for the IBM PC AT offers nine software-selectable input ranges. These include bipolar ranges of ±10 V, 5 V, 0.5 V, 0.05 V and 0.01 V and unipolar ranges of 0 to 10, 1, 0.1 and 0.02 V. The DAS-8PGA board provides four digital-output bits and three digital-input bits. A three-channel counter/timer can operate as an analog/digital pacer clock or can be used to measure or generate frequency, measure pulse width, or count events. Utility software provides a complete assembly driver for Basic, installation, calibration and example programs, as well as a few operational data-acquisition programs. Price is $560. **MetraByte,** 440 Myles Standish Blvd, Taunton, MA 02780.

Circle 143

Portable computer acts as mobile measuring system

The Portax-AT system is a portable/AT-compatible system designed for analog data acquisition and test measurement. Built for net-independent operation, the system features a +12 V_{dc} or optional 115 V_{ac} power input, and is available in a 19-in. rack-mount or tabletop format. It comes with 8- or 12-MHz versions of the 80286 with up to 1 Mbyte of RAM. An 80386 model with up to 16 Mbytes of RAM is also available. The system offers multiple options for mass storage, including 3½-in. and 5¼-in. floppy and Winchester drives, and a 60-Mbyte cartridge tape drive. It comes with a 7-in. CRT or an electroluminescent display. **Stemmer Personal Computer Systems GmbH,** Boschstrabe 12, 8039 Puchheim, Munich, W Germany.

Circle 144

Cassette memory card inserts into STD bus board

Available for either the STD TTL bus or the STD CMOS bus, the 234/334C cassette memory card offers large-scale data acquisition and transfer capability for the STD bus. The credit card-sized cassette can either be inserted into a socket mounted on the STD card or used with an extension cable and remote panel socket. The cassettes feature CMOS static RAM, a write-protect switch and a replacement lithium battery. Single-unit pricing is $285. **Enlode,** 1728 Kingsley Ave, Orange Park, FL 32073. **Circle 145**

GPIB controllers provide integrated DMA control

The GPIB-232CT and the GPIB-422CT turn any computer or terminal with a RS-232 or RS-422 serial port into a general-purpose interface bus (GPIB) controller, or make any RS-232 or RS-422 device look like a GPIB device. Both boards feature microcomputers that include built-in direct memory access control and a 64- or 256-kbyte RAM buffer. The controllers are fully programmable via an on-board IEEE-488 Bus Control Language (IBCL) operating system. The DMA controller allows data transfer to the memory buffer from the GPIB port at speeds of up to 900 kbytes/s. Price is $595 for the 64-kbyte version; $795 for the 256-kbyte version. **National Instruments,** 12109 Technology Blvd, Austin, TX 78727. **Circle 146**

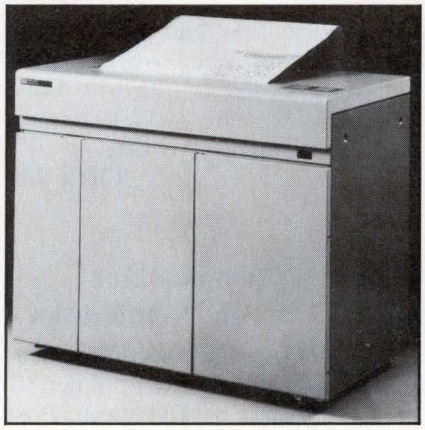
Peripherals

Electrostatic plotter offers high throughput

Hewlett-Packard has expanded its line of CAD/CAE output devices with the introduction of the HP 7600 series electrostatic plotters. Two models of the high-throughput, monochrome plotter are available, the D and the E size. Resolution reaches 406 dots/in.

Although lower cost pen plotters produce color images, they operate at slower speeds and offer limited unattended operation, since pen and paper condition must be monitored regularly.

The 7600 series features built-in



Hewlett-Packard Graphics Language (HP-GL), as well as HP-GL/2, which the manufacturer says will offer enhanced performance for the future. The plotter is mobile, with a footprint of 35×55×23 in., and connects to RS-232-C, HP-IB (IEEE-488) and Centronics parallel interfaces. Data flow from the host will be faster with the use of the parallel interface, providing reduced plotting time.

A built-in vector-to-raster converter with 40-Mbyte storage holds up to 3 million vectors and off-loads

the host CPU. Plotting speed is constant after this conversion at .64 in./s in normal mode and .32 in./s in high-density mode for the Model 240D, and .86 in./s and 43 in./s for the Model 240E.

Available media are report- and premium-grade opaque paper, as well as vellum. Translucent paper will be available this fall. Prices for the series are $22,900 for the 240D and $27,500 for the 240E. **Hewlett-Packard,** 19310 Pruneridge Ave, Cupertino, CA 95014. **Circle 147**

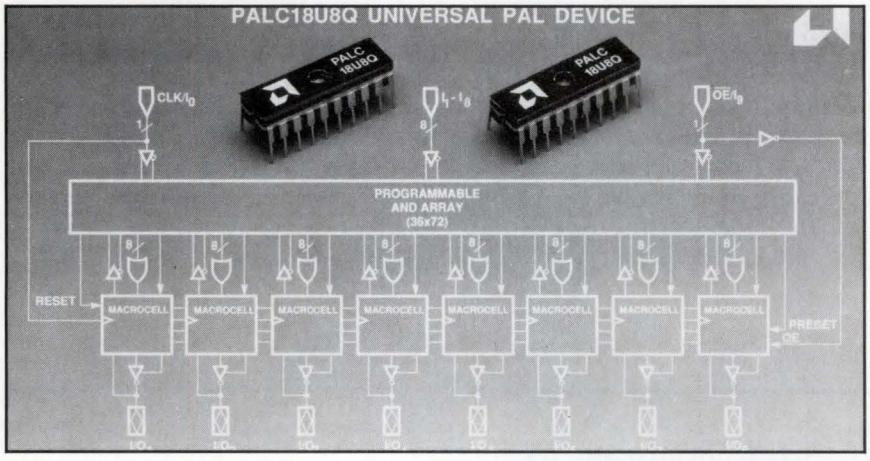
Plotting software rasterizes data for direct output

Users running Autocad on IBM PC ATs or compatibles can use their systems as rasterizers and controllers with Versatec's Autocad Autodesk Device Interface plotting software. When installed as a driver, users can call the software directly from within Autocad, for convenience and speed. When installed as a utility, the software plots from an Autocad disk file, conserving RAM space. The software features 127 definable pens and selectable pen widths (from 1 to 15 points wide), as well as multiple document sizes, eight line colors and multiple copies. A hard disk, DOS version 3.1 or higher, and a Versatec model 110 interface board and device driver (version 1.2) are required. In addition, a math coprocessor is highly recommended. The price for Autodesk Device Interface plotting software is $250. **Versatec,** 2710 Walsh Ave, Santa Clara, CA 95051. **Circle 148**

Integrated Circuits

Programmable array logic family features 10 dedicated inputs

Using UV-erasable CMOS technology and consuming 55 mA of power, the PALC18U8Q series of programmable array logic (PAL) devices allow design flexibility through 10 dedicated input lines and a macrocell. Each macrocell is configurable in one of eight combinatorial or registered options.



The series includes the PALC-18U8Q-25, with a 25-ns, propagation delay and the PALC18UQ-35, with a 35-ns delay. Both are available in 20-pin plastic and ceramic-windowed, dual in-line packages.

Applications include sequencing and prototyping, as well as traditional PAL device tasks in the computer, telecommunications and industrial markets. In quantities of 1,000, the PALC18U8Q-25 costs $4; the PALC18U8Q-35 costs $2.75. **Advanced Micro Devices,** 901 Thompson Place, Sunnyvale, CA 94088. **Circle 149**

Controllers let two microprocessors access RAM

The 74F1764/1765 and the 74F1764-1/1765-1 dynamic RAM dual-ported controllers are timing generators and arbiters that let two microprocessors, microcontrollers or other memory-accessing devices share the same block of DRAM. The devices perform signal timing, arbitration, address multiplexing and refresh address generation. The 1764-1/1765-1 reduce the row-address hold time by half a clock cycle, and their outputs permit first-reflected wave switching, as opposed to incident wave switching. **Signetics,** 811 E Arques Ave, Sunnyvale, CA 94088. **Circle 150**

Chip set communicates with T1 or CEPT networks

A four-chip set lets telecommunications engineers convert to either T1 or Conference of European Post Telecommunications (CEPT), the respective North American and European standards, without extensive modification. The T1/CEPT line card is switched from one standard to the other by interchanging a single chip. It is used by the 1.5-Mbit/s computer-to-computer communications market, private automatic branch exchanges, channel banks and multiplexers. The price is $98 in 5,000-piece quantities. **Dallas Semiconductor,** 4350 Beltwood Pkwy S, Dallas, TX 75244. **Circle 151**

RISC chip set has 25-MHz clock rate

With a 25-MHz clock rate, the IDT-79R3000 microprocessor, the IDT-79R3010 floating-point accelerator and the IDT793020 write buffer chip set operate at 20 Mips. The microprocessor includes a programmable CPU, a memory-management unit, a cache controller, 512 kbytes of instruction and data caches, and a floating-point coprocessor interface. The accelerator performs floating-point calculations in parallel with the execution of program instructions, while the write buffer allows write operations during run cycles. Lots of 100 are priced at $795 for the microprocessor, $875 for the accelerator and $45 for the write buffer. **Integrated Device Technology,** 3236 Scott Blvd, PO Box 58015, Santa Clara, CA 95052. **Circle 152**

Single chip moves 33 million pixels/s

The HD63487, or Memory Interface and Video Attribute Controller (Mivac), is a single chip with all the circuitry needed to control graphics memory and display attributes. An engineer can build a graphics system in the space of a business card using Mivac with existing CRT controller chips and dynamic RAMs. Mivac can draw images into its memory at 2 million pixels/s, and transfer them to a CRT at 33 million pixels/s. Programmable parameters include resolution, number of colors, pixel shift rate and frame buffer size. The price is $25 in 5,000-piece quantities. **Hitachi America,** 2210 O'Toole Ave, San Jose, CA 95131.**Circle 153**

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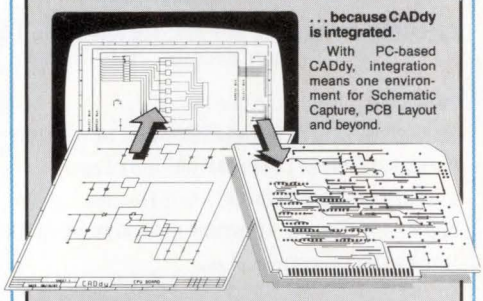

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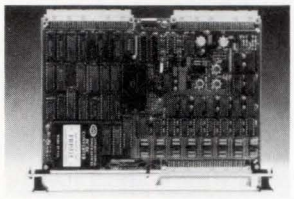
CIRCLE NO. 222

VMEbus
HIGH RESOLUTION ANALOG-TO-DIGITAL CONVERTER

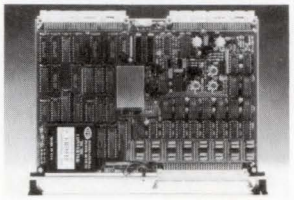


VMIC announces a VMEbus High Resolution Analog input board VMIVME-3116) that features built-in-test and auto-calibration. The new product is designed with 32 single-ended/16 differential front panel inputs with a wide variety of input filter options. The ADC board features a resolution of 16 bits and a conversion time of less than 20 microseconds. The price is $2,595.00 with all options; however, lower priced options are available.

Contact VMIC,
12090 South Memorial Parkway,
Huntsville, AL 35803-3308,
(205) 880-0444

CIRCLE NO. 223

VMEbus
HIGH SPEED ANALOG-TO-DIGITAL CONVERTER



VMIC announces a high speed VMEbus, 12-bit analog-to-digital converter (VMIVME-3101) with 32 single-ended/16 differential front panel inputs. The new product is designed with builtin-test, auto-calibration, and a wide variety of input filter options. The product is designed with a provision for simultaneous settling and conversion which gives A/D conversion throughputs to 200 kHz. The A/D converter conversion time is 3 μs. The price is $2,895.00 with all options; however, lower priced options are available.

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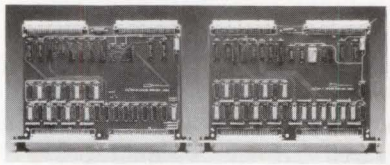
CIRCLE NO. 224

VMEbus REPEATER LINK



VMIC announces a software transparent high performance (32-bit) multidrop longline (R485) differential VMEbus Repeater Link (VMIVME-Repeater-485/32) that supports the interconnection of up to 16 VMEbus chassis in a system configuration where a "Master Chassis" contains all master/slave controller boards and the extended chassis (slave chassis) contains only slave boards. The price of the master multidrop board (VMIVME-Repeat M-485/32) is $895.00 and the slave multidrop board (VMIVME-Repeat S-485/32) is $1,095.00

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Huntsville, AL 35803-3308,
(205) 880-0444

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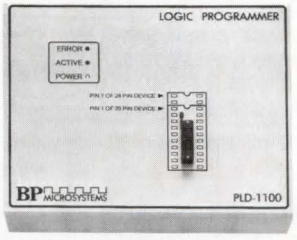

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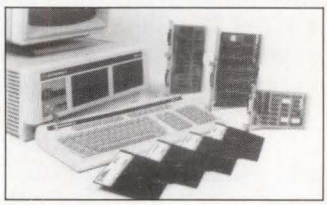

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