

# COMPUTER DESIGN

MAY 15, 1988

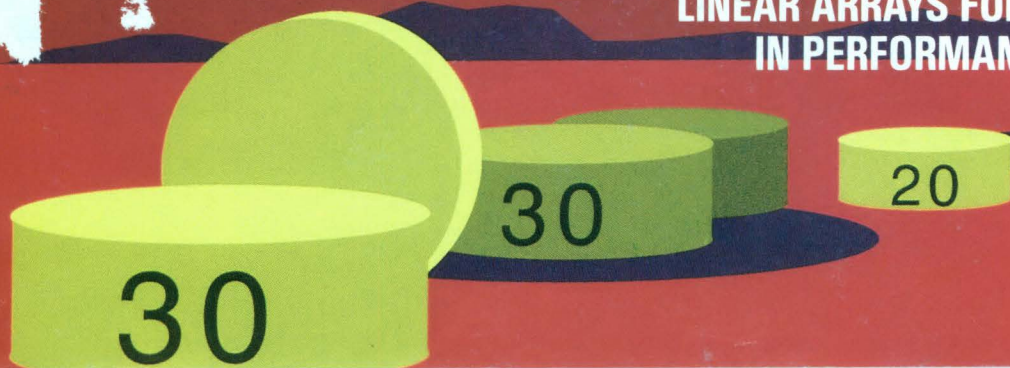
THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

## RISC ARCHITECTURES TAKE ON HEAVYWEIGHT APPLICATIONS



**LINEAR ARRAYS FORGE IMPROVEMENTS  
IN PERFORMANCE AND FLEXIBILITY**

**ISDN PIECES BEGIN  
TO FALL INTO PLACE**





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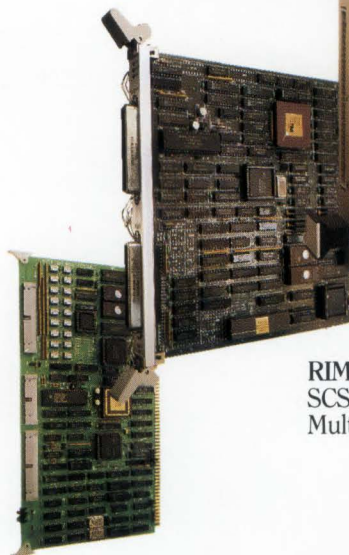
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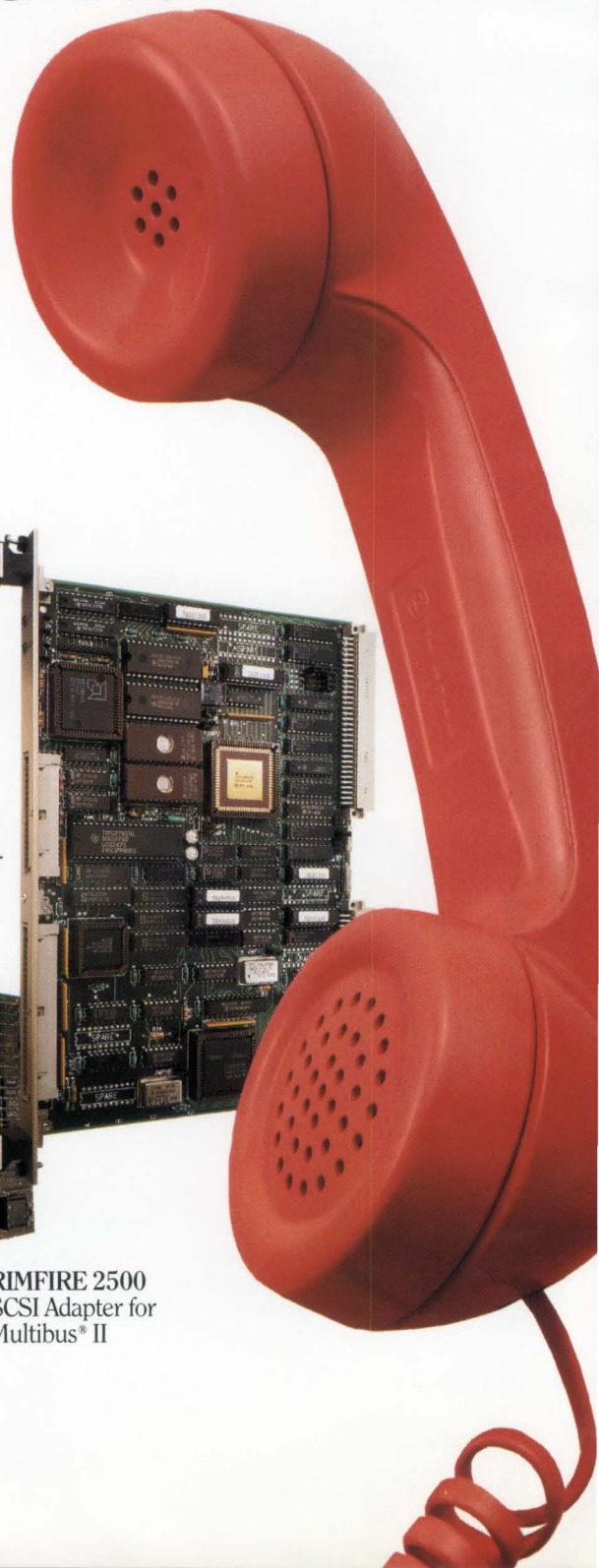
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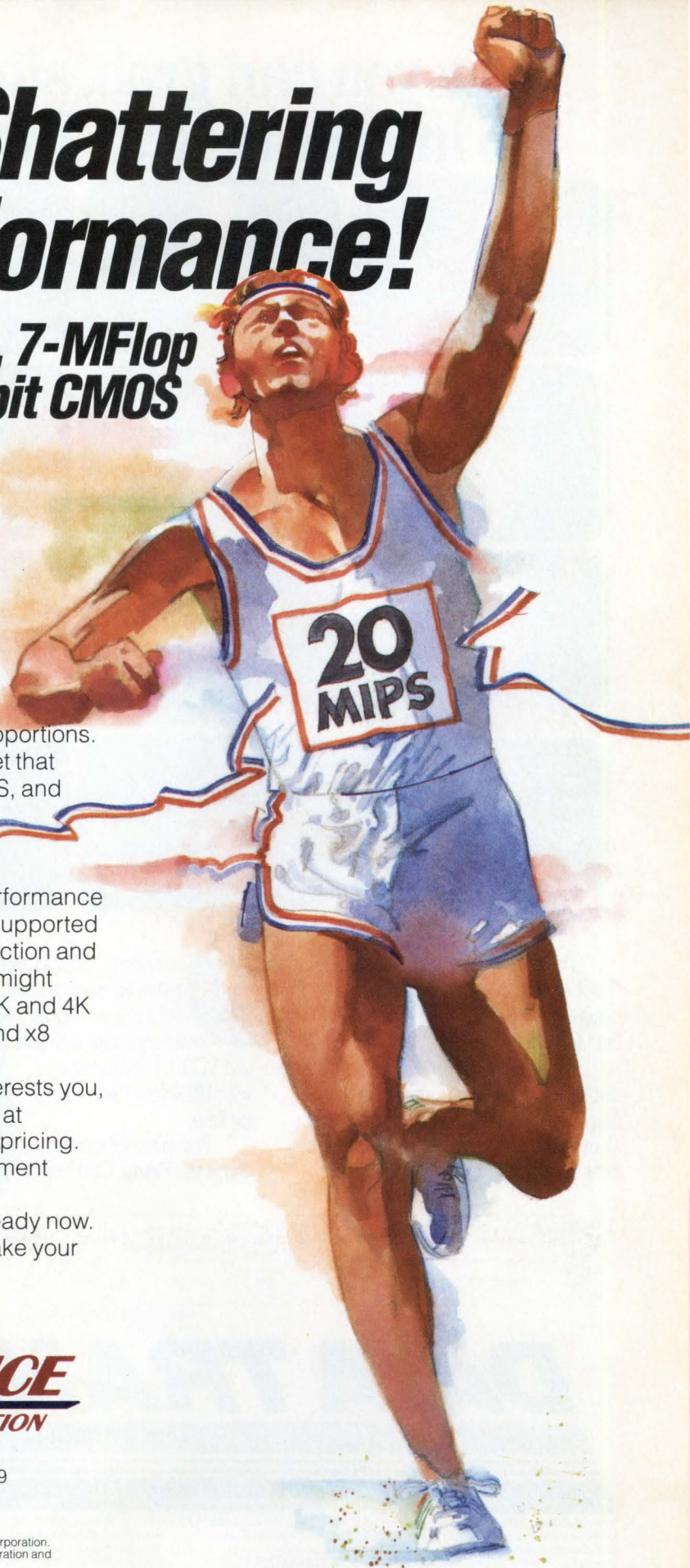
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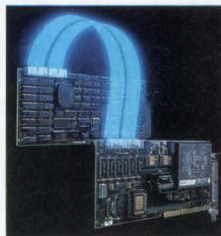


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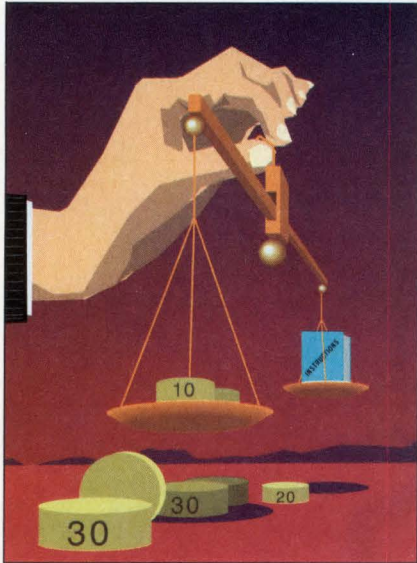
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**CIRCLE NO. 3**





This issue's cover was designed by John Bonner.

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*Within the last year, linear arrays have begun to catch up to their digital counterparts. Developments in base silicon, array architecture and CAD environments are combining to give the analog designer higher performance and more flexibility.*

### Technology Focus on Communication ICs

- 48 The ISDN puzzle takes shape as the pieces fall into place. Recent announcements indicate an industry-wide commitment to ISDN. Vendors are integrating higher levels of performance into new S and T interface chips while expanding their offerings to support other points in the network. Even more significant, development boards are starting to appear.

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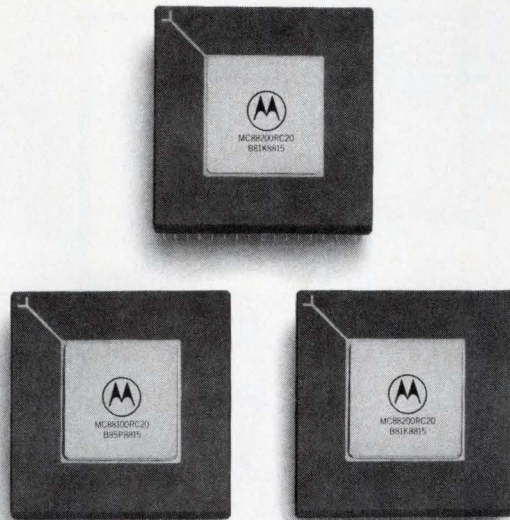
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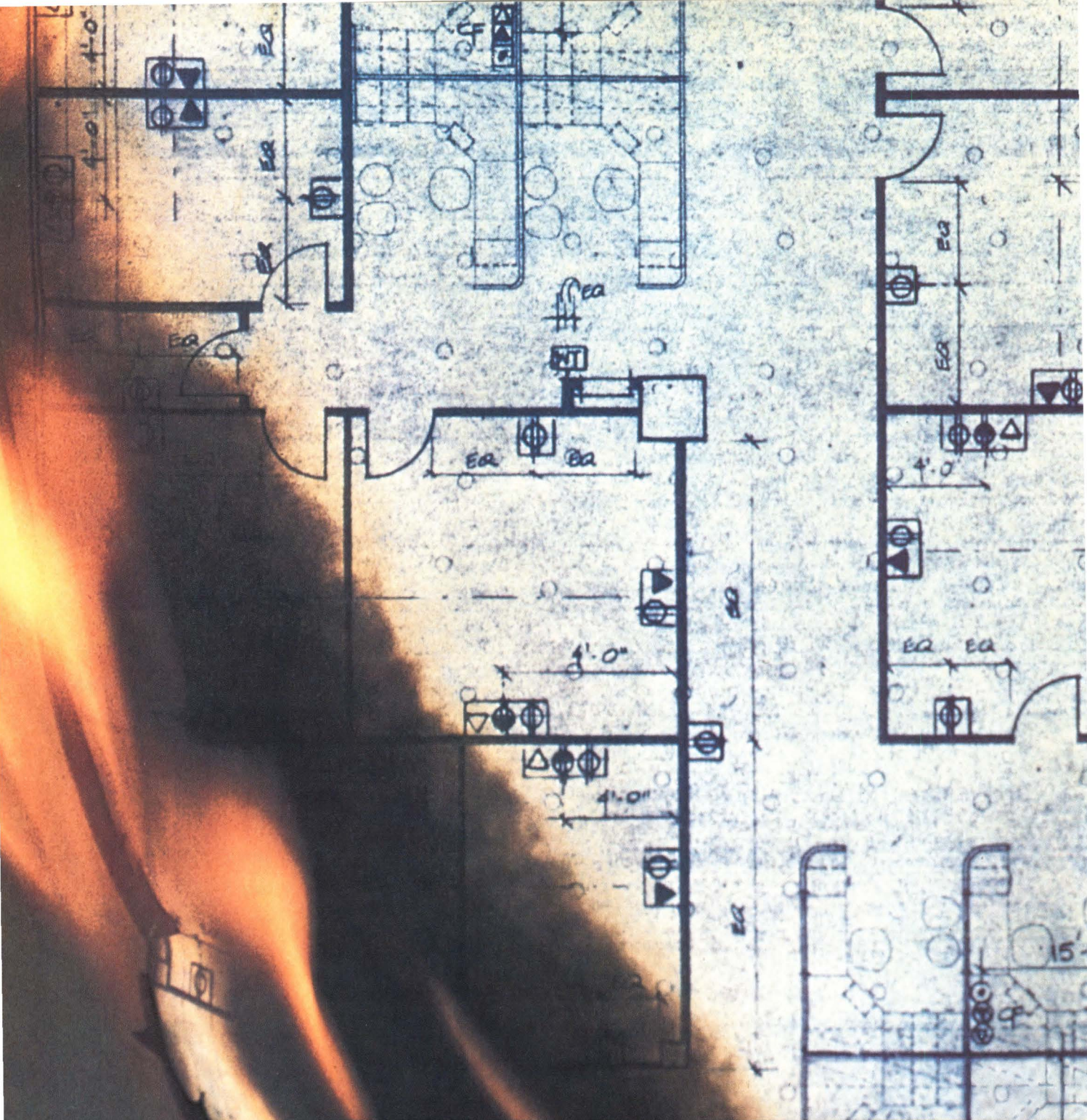


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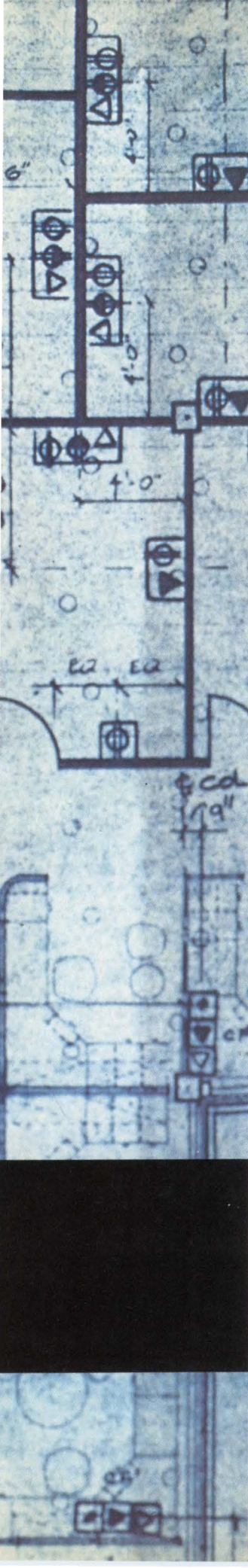
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Unless you're using  
AT&T data cables, the 1988 fire codes  
could be cause for alarm.





Rest assured, AT&T is ready now with a complete line of UL-listed data cable products that conform to the new National Electrical Code.\*

Whether you're concerned with building installations, or the interconnection of computer components, don't risk being burned by the new NEC fire safety standards, effective July '88.

The revised NEC specifies that only listed cable may be placed in buildings for data communications circuits. Yet many suppliers have been slow to respond to the stricter standards.

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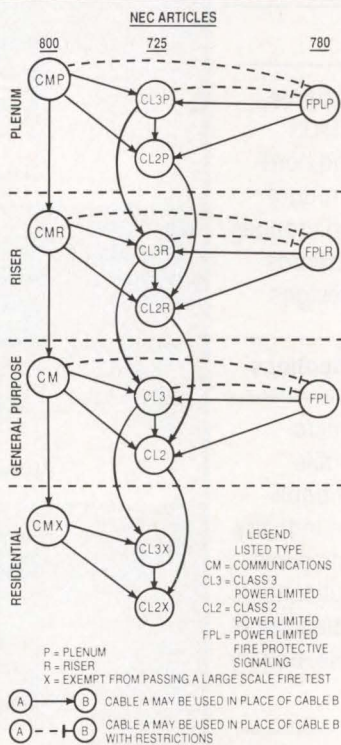
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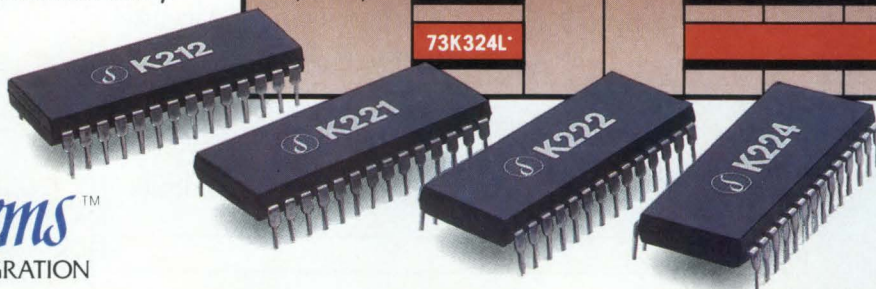
The family includes an easy-to-use micro-processor control interface, and versatile features suitable for a wide variety of applications. The "U" versions integrate an industry standard UART with the modem function in a design optimized for integral bus applications, and the low-power "L" versions operate from a single + 5 volt supply, making portable, battery, or line powered designs possible.

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MODEM IC SELECTION CHART								
APPLICATIONS	PRODUCTS	OPERATING MODES						PRODUCT FEATURES
MARKETS SERVED	SSI DEVICE NUMBER	103 0-300 BPS	212A 1200 BPS	V.21 0-300 BPS	V.22 600/ 1200 BPS	V.22 bis 1200/ 2400 BPS	V.23 0-1200 BPS	
<b>UNIVERSAL APPLICATIONS</b> Stand-Alone or Integral Modem Designs	73K212	█						High performance single-chip modems with easy-to-use cost-effective features.
	73K221			█				
	73K222				█			
	73K224					█		
<b>LOW POWER APPLICATIONS</b> • Lap Tops • Portable Terminals • Line Powered Modems • Battery-Powered Units	73K212L	█						High performance single-chip modems providing low-power operation from a single + 5 volt supply.
	73K221L			█				
	73K222L				█			
	73K224L					█		
<b>DEDICATED INTEGRAL APPLICATIONS</b> • Bus-Oriented Systems • Credit Verification • Automatic Teller Machines • Pay Telephones • Diagnostic Equipment	73K212U	█						Enhanced single-chip modems with a fully integrated 16C450 UART function, and added circuitry to simplify integral designs.
	73K221U			█				
	73K222U				█			
<b>EUROPEAN DATA COM APPLICATIONS</b> Multi-standard modems requiring videotex compatibility	73K322*			█				Single-chip modems add V.23 and special features to standard operating modes; available in + 12 volt or + 5 volt versions. * Available 1988
	73K322L*			█				
	73K324*				█			
	73K324L*				█			

CIRCLE NO. 6 FOR PRODUCT INFORMATION  
CIRCLE NO. 7 FOR CAREER INFORMATION

*"Where we design to your applications."*



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# UP FRONT

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## **Tandy announces breakthrough in erasable optical media**

The search for truly erasable optical media may have ended with an announcement by Tandy (Fort Worth, TX) of a new media technology called Thor (Tandy High-intensity Optical Recording). While the company won't disclose the details, the media is written by laser heating, which causes the layered material structure to buckle inward, forming a small depression on the surface that can be read by the read laser. Re-heating causes the depression to flatten out again, leaving the surface in its original form. Tandy's plans are for erasable audio recording on the same format as compact disks, but data storage—using CD ROM format and larger platters—is also feasible. If the technology proves workable, it could compete with CDs and digital audio tape in the consumer arena and with CD ROM, write-once optical and magneto-optical recording in the computer industry.—*Tom Williams*

## **Behavioral logic synthesis joins EDA marketplace**

A long-standing dream of electronic design automation (EDA) vendors—the ability to translate behavioral inputs into gate-level schematics and net lists—is closer to being reality. Silc Technologies (Burlington, MA) is introducing Silcsyn, a logic-synthesis tool that can map behavioral descriptions into commercial application-specific IC libraries. Silcsyn includes an input language based on Lisp, a functional simulator and a static timing verifier. Initially available on workstations from Mentor Graphics (Beaverton, OR), Silcsyn can synthesize sequential or combinational logic. At least two other vendors will introduce commercial logic-synthesis toolsets within the next four weeks.—*Richard Goering*

## **Electroluminescent displays pare power, boost brightness**

Planar Systems (Beaverton, OR), the market leader in thin-film electroluminescent displays, has now cut power consumption to make its displays more competitive with twisted liquid crystal displays. Using power recovery circuitry and more efficient drivers, Planar has reduced the maximum power rating on its 640- $\times$ 400-pixel display to 14 W—still three times the power needed for a comparable backlit supertwisted LCD. To help make the trade-off more palatable, the company has also increased brightness by 50 percent from 20 to 30 fL, or about four times that of the backlit supertwisted LCD.—*John Mayer*

## **Texas Instruments plans CASE tools for embedded systems**

Having had some success with its Information Engineering Facility (IEF), a computer-aided software engineering (CASE) system designed to develop information systems, Texas Instruments (Dallas, TX) hopes to be among the first to deliver a completely integrated system for real-time embedded systems. Like IEF, the proposed system would automate software design, from planning and analysis to code generation. But don't look for it any time soon. "By the early 1990s, we expect to have a product...that takes the IEF approach," says Michael Watters, TI's manager of advanced information management. With such a product, developers of embedded systems might find benefits similar to the 4:1 productivity enhancements over conventional system development methods already provided by implementations of IEF.—*John Mayer*

*(continued on page 10)*



## High-performance real-time system abandons Multibus for VME

The recently unveiled 68030-based computer systems from Masscomp (Westford, MA) provide the company with a formidable weapon in its attack on the real-time scientific market. But one of the more intriguing aspects of the product line is the company's decision to move from the Multibus I-based designs of earlier products to a VMEbus-based architecture rather than to Multibus II. "Looking at industry trends, we saw that the direction was toward VME," says product manager Judith LaRocque. "VME has much more support than Multibus II. Upward compatibility with our Multibus I-based systems is retained by supporting up to six Multibus-to-VME interface modules."—*John Mayer*

## Valid Logic to become largest full-custom IC CAD supplier

By acquiring the IC layout product line from Calma (Milpitas, CA), Valid Logic (San Jose, CA) will soon become the industry's largest full-custom IC CAD supplier. The acquisition agreement, which effectively removes Calma, a subsidiary of General Electric, from the electronic design automation market, brings Valid an installed base of more than 2,700 users. When the agreement is complete, Valid will assume all sales and development responsibilities for the GDS-II (Graphics Design System) and EDS-III (Electronics Design System).—*Richard Goering*

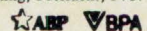
## Trade association promotes Nubus for industrial applications

Claimed to be a cost-effective alternative to both the low-end STD Bus and Multibus I but having performance capabilities comparable to the high-end VMEbus and Multibus II, Nubus is potentially the bus-of-choice for many industrial applications, according to its supporters who met earlier this month in Atlanta during Comdex/Spring. The group will develop a charter, objectives and membership requirements prior to a full promotional effort for Buscon/East in October, according to Jennifer Maher, marketing project manager at Mizar (St. Paul, MN), who led the meetings. Seven companies are involved in the association, including Apple Computer (Cupertino, CA), which chose Nubus for its Macintosh II; Texas Instruments (Austin, TX), an early developer of the bus; and Mizar. For more information on the association, contact Anne Weber at (714) 669-1201.—*Sydney Shapiro*

## ASIC microcontroller cores grow to 16 bits

National Semiconductor (Santa Clara, CA) has announced the conversion of its HPC 16-bit microcontroller to an application-specific IC megacell. The company claims the HPC Core is the first 16-bit microcontroller to be made available in a cell library. The cell, which National says can be tailored to suit the needs of individual designs, already includes a variety of memory and peripheral blocks, including RAM, timer/counters, an interrupt controller and a Microwire/Plus serial interface. The speed of the CPU core and the variety of included devices make the HPC Core a significant advance over existing 8-bit cores, according to sources at National.—*Ron Wilson*

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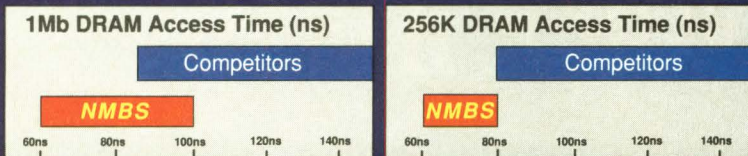




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			SOJ	Production
			ZIP	Production
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			SOJ	2Q88
			ZIP	2Q88

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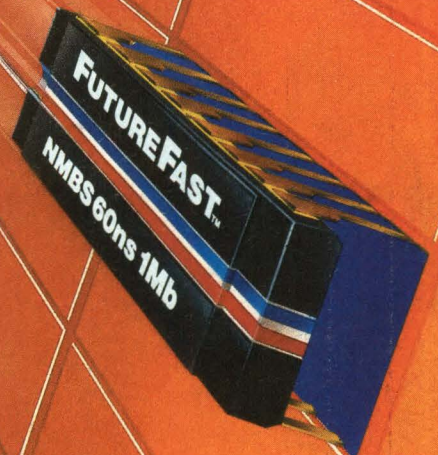
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## **To be continued.**

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## Putting their houses in order

**O**n a whirlwind tour of the Midwest and Southwest last month, I visited a variety of board and computer houses, from small companies that ship a few hundred pieces a month to large operations crunching through tens of thousands of products every 30 days. All the trends we've read about were evident in varying degrees at one company or another: design for testability and manufacturability, "soft" prototyping through design simulation, sophisticated materials-management systems, highly automated assembly equipment and so forth. What struck me most on my plant tours, though, was the excellent use of computers in the coordination and integration of all the parts of an operation and, in a few select places, the impressive use of Japanese principles to turn out better products by more highly motivated manufacturing personnel.

Two of the companies I visited had recently completely revamped their manufacturing operations. At both, operations managers steeped in the assembly-line tradition had thrown much of their training and experience out the window and enthusiastically embraced a foreign approach. In terms of job lots, "the bigger the better" is no longer the rule at these companies. In terms of work flow at individual manufacturing stations, "the quicker the better" no longer holds. As for component suppliers, "the more sources the better" has also become a part of the past. And no longer do these companies, or their customers, want to maintain large inventories of component products when just-in-time deliveries provide a much smoother manufacturing flow.

Virtually all the companies I visited have been willing to pay the up-front costs of producing a more efficient operation and a more reliable, more competitive product. The capital equipment costs can, of course, be staggering, the time and energy required to make major transitions are great, and the early stages of the learning curve can be very disruptive. Yet, not one company has failed to perceive a payback or, at least, clear indications that a payback is on its way.

At those companies where the Japanese influence is most apparent, one of the biggest up-front costs seems to be time. It takes time, first of all, for assembly personnel to make the psychological transition from being anonymous cogs in a machine to being, in essence, their own manufacturing managers, quality-control supervisors and, in some cases, maintenance personnel. And even once this transition is made, volume is typically below what it was. Yet even in the early stages, the beginning of the payback can be seen in the state of the products at the end of the manufacturing cycle. Despite the initial reduction in the volume of products produced, there's also typically a substantial reduction in both the number of products that require time-consuming in-house rework and the number that fail in the field.

A handwritten signature in cursive script that reads "David Lieberman".

David Lieberman  
Senior Editor



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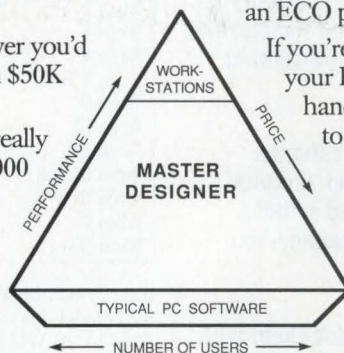
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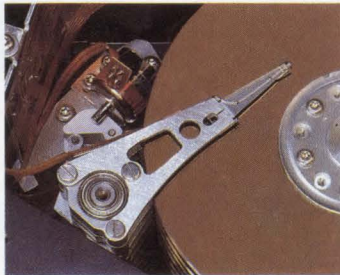


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Wren V	442	16	ESDI	10
Wren V	383	14.5	ESDI	10
Wren V	344	16.5	SCSI	10-15
Wren V H.H.	190	18	SCSI	10-15
Wren IV	307	16.5	SCSI	10-15
Wren III	182	16.5	ESDI	10
Wren III	160	16.5	SCSI	10
Wren III H.H.	106	18	ESDI	10
Wren III H.H.	91	18	SCSI	10
Wren II	96	28	ST506,ESDI	5
Wren II H.H.	51	28	ST506	5

H.H. = Half High Models

SCSI models list usable capacity formatted in 1024 Byte sectors.

Wren III, IV, V-344 Mb SCSI models have 40,000 Hr. MTBF (others: 30,000 Hr. MTBF).

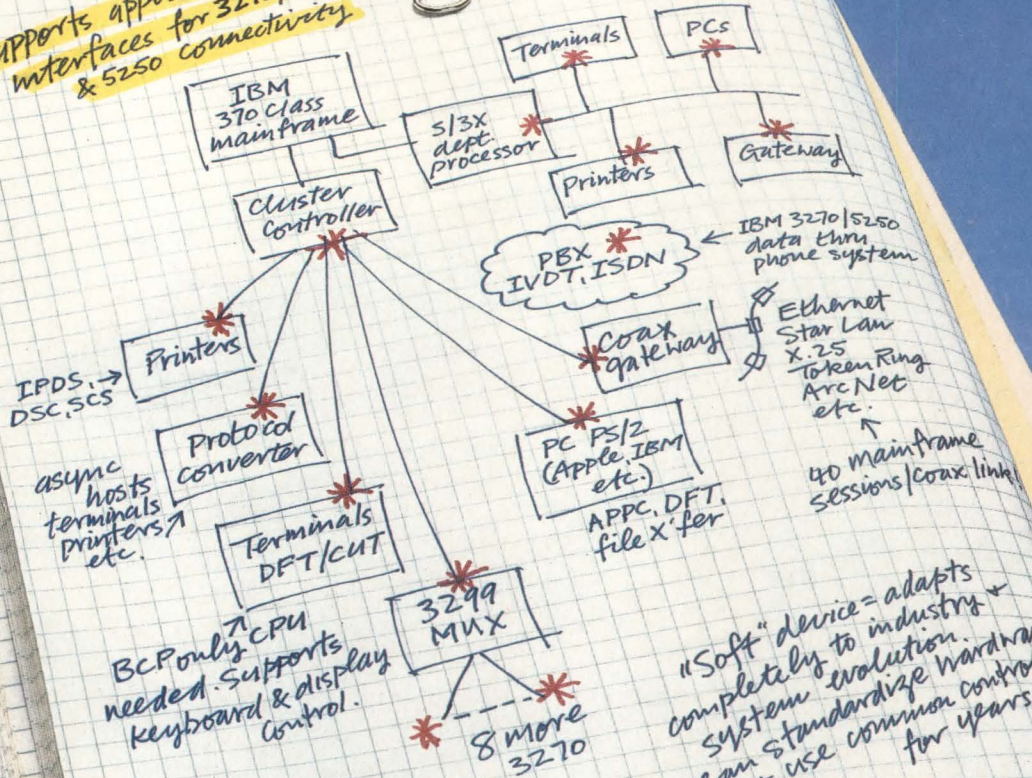
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\* DP8344 BCP



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## INTRODUCING THE DP8344 – THE EASY, AFFORDABLE WAY TO IBM CONNECTIVITY

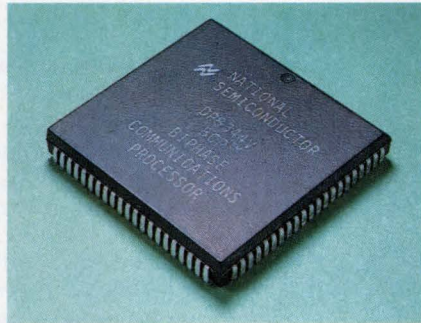
At last there's a one-chip solution to processing IBM 3270, 3299 and 5250 communication protocols – the programmable DP8344 Biphasic Communications Processor.

The BCP™ is easily integrated into cluster controllers, PCs, terminals and printers, so now anyone can design a plug-compatible interface for IBM mainframe and departmental processors.

You can also use the DP8344 in a PBX or to build a gateway to various local- and wide-area networks.

You can use it in a protocol converter to give inexpensive peripherals access to the power of the mainframe. Or in a PC or IBM PS/2 to provide 3270 or 5250 terminal emulation.

In fact, providing IBM connectivity is now so simple and inexpensive that a host of new applications are being developed. The BCP has been designed in by more than 100 companies – including Hewlett-Packard, Local Data, Pathway Designs, Lee Data, Centronics, and Memorex.



## IT GIVES YOU A LOT OF POWER IN A VERY SMALL SPACE

A full system, supporting all three IBM protocols can be implemented in an area not much larger than a credit card.

The BCP integrates an intelligent transceiver and a high-performance CPU on the same low-power CMOS chip.

Powerful enough to operate as the sole system processor, the BCP also incorporates a flexible bus interface with on-chip arbitration logic, enabling communication with other processors.

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## IT COULDN'T BE MORE FLEXIBLE

The BCP features a software-configurable transceiver that supports not only IBM 3270, 3299 and 5250 protocols but also general eight-bit protocols.

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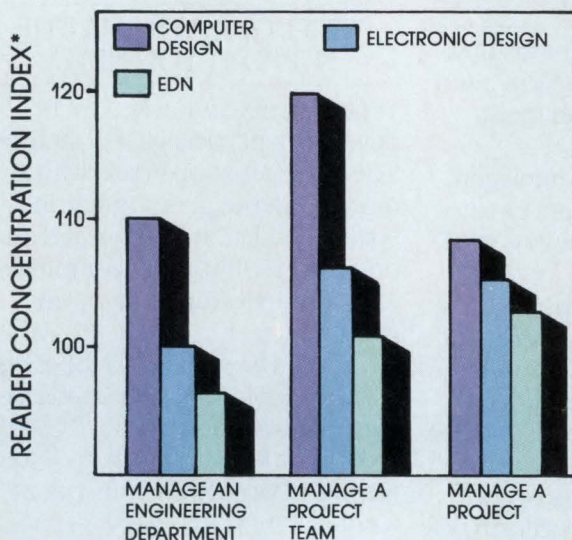


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THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

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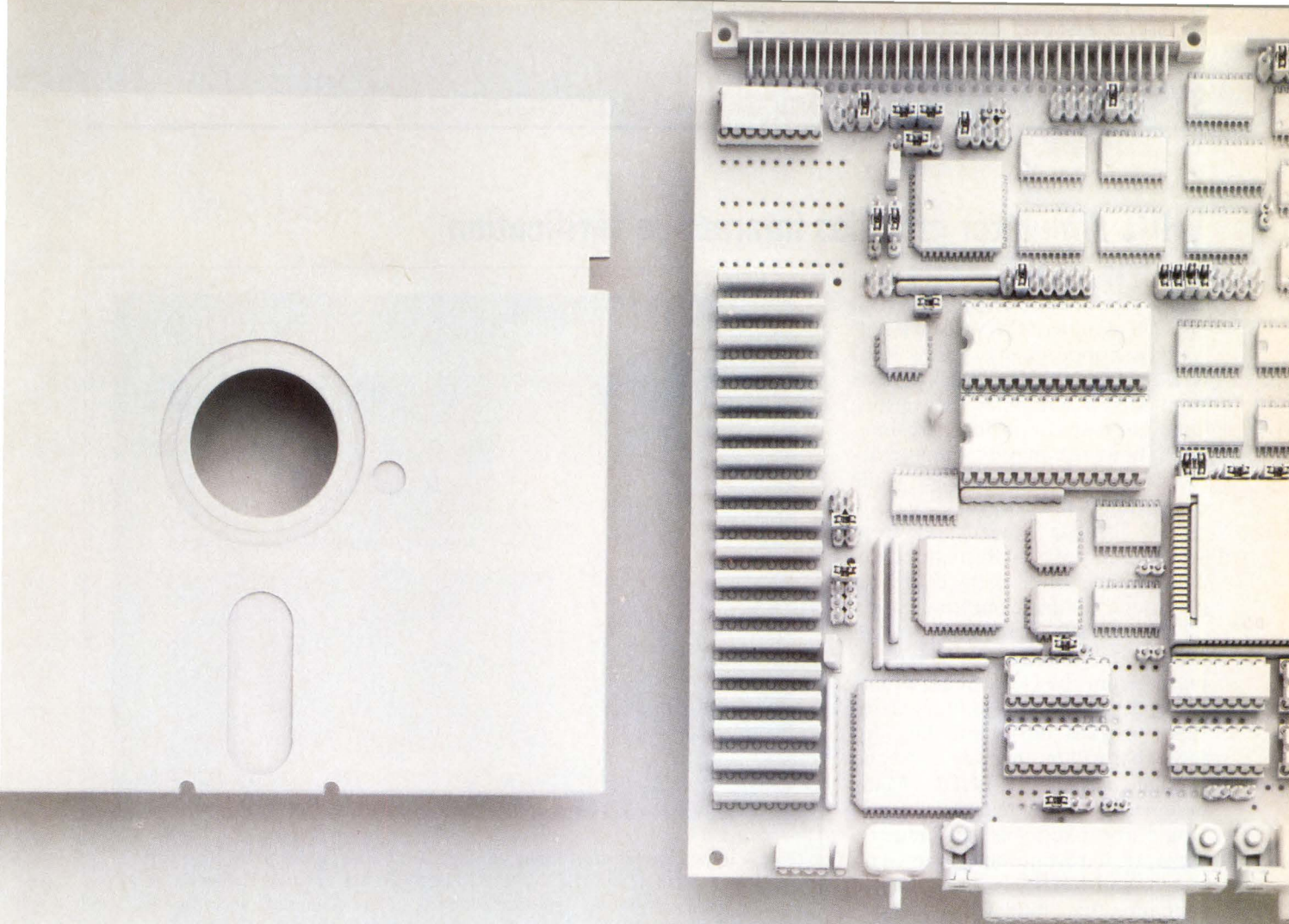
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## VHDL simulator provides interactive verification

What may be the first commercial logic simulator to provide a full implementation of the VHSIC Hardware Description Language (VHDL) is now available on workstations from Mentor Graphics (Beaverton, OR). The real story behind the simulator, however, may be the interactivity it allows the designer while simulation is underway.

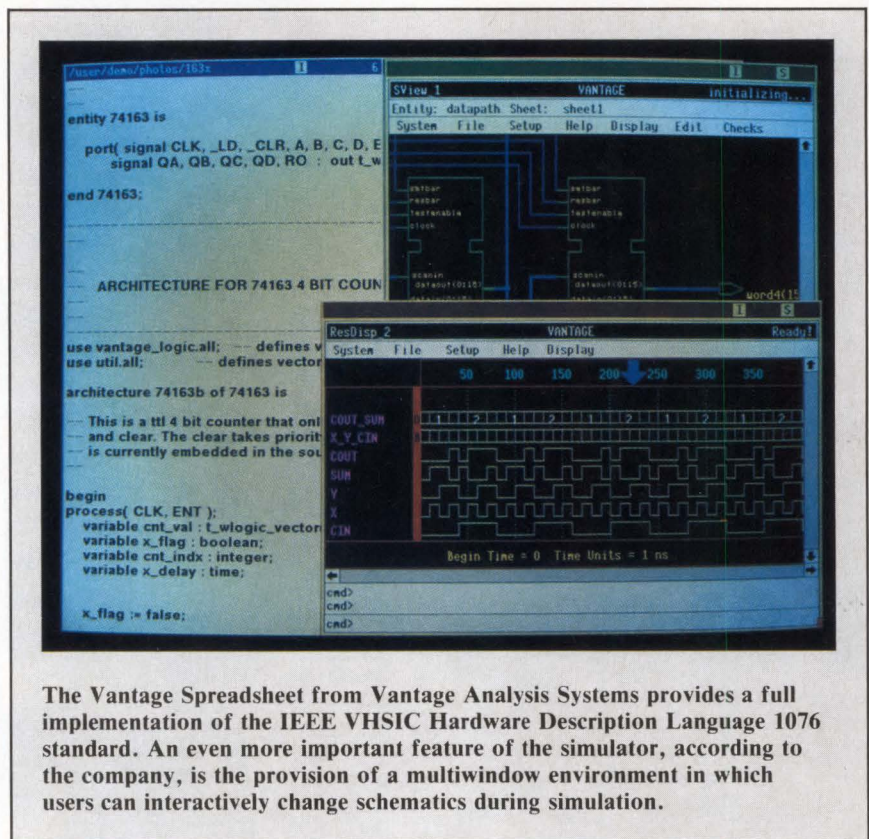
The Vantage Spreadsheet from Vantage Analysis Systems (Fremont, CA) is newsworthy because it provides a complete implementation of the new IEEE standard, VHDL 1076. With a mandate for VHDL expected from the Department of Defense, designers in the military/aerospace market are scrambling for tools that will let them describe and simulate designs in VHDL. Many designers in the commercial world would also like to use an industry-standard hardware description language, and VHDL is on its way to becoming that standard.

But David Coelho, executive vice-president of Vantage, has more than VHDL on his mind. "The most important thing we're bringing to the marketplace is the ability to make real-time changes to the schematic during simulation," he says. "This lets designers do a what-if analysis they never could do in the past. VHDL is just an opportunistic thing that we're leveraging."

### Compilation bottleneck

One of the most frustrating aspects of logic simulation is the time it takes to change a design and then resimulate it. Designers usually must stop the simulation, return to the original schematic, change that schematic, and then recompile it into a net list for simulation. If a large design is involved, this process can take hours. Incremental compilation techniques may let designers recompile just a portion of the design, but they still have to get out of simulation and go back to the original schematic.

Richard Goering  
Senior Editor



The Vantage Spreadsheet from Vantage Analysis Systems provides a full implementation of the IEEE VHSIC Hardware Description Language 1076 standard. An even more important feature of the simulator, according to the company, is the provision of a multiwindow environment in which users can interactively change schematics during simulation.

Vantage provides a specialized schematic editor that lets the engineer make on-the-fly changes to the design. The original schematic data is moved from Mentor Graphics' Neted editor into Vantage's SView schematic viewer. Once the schematic data is in SView, users can zoom and pan within the schematic, probe signals and make design changes without exiting the simulation. Vantage's net-list generator adds the changes to an existing net list, compiling only the new data that's added.

This ability to make rapid design changes makes the Vantage Spreadsheet analogous to the spreadsheets used for financial analysis. "Simulation is no longer a batch verification capability; it's a real-time tool," says Coelho. "We're predicting a one- to two-minute turnaround for most design changes. This capability could change the way designers feel about simulation."

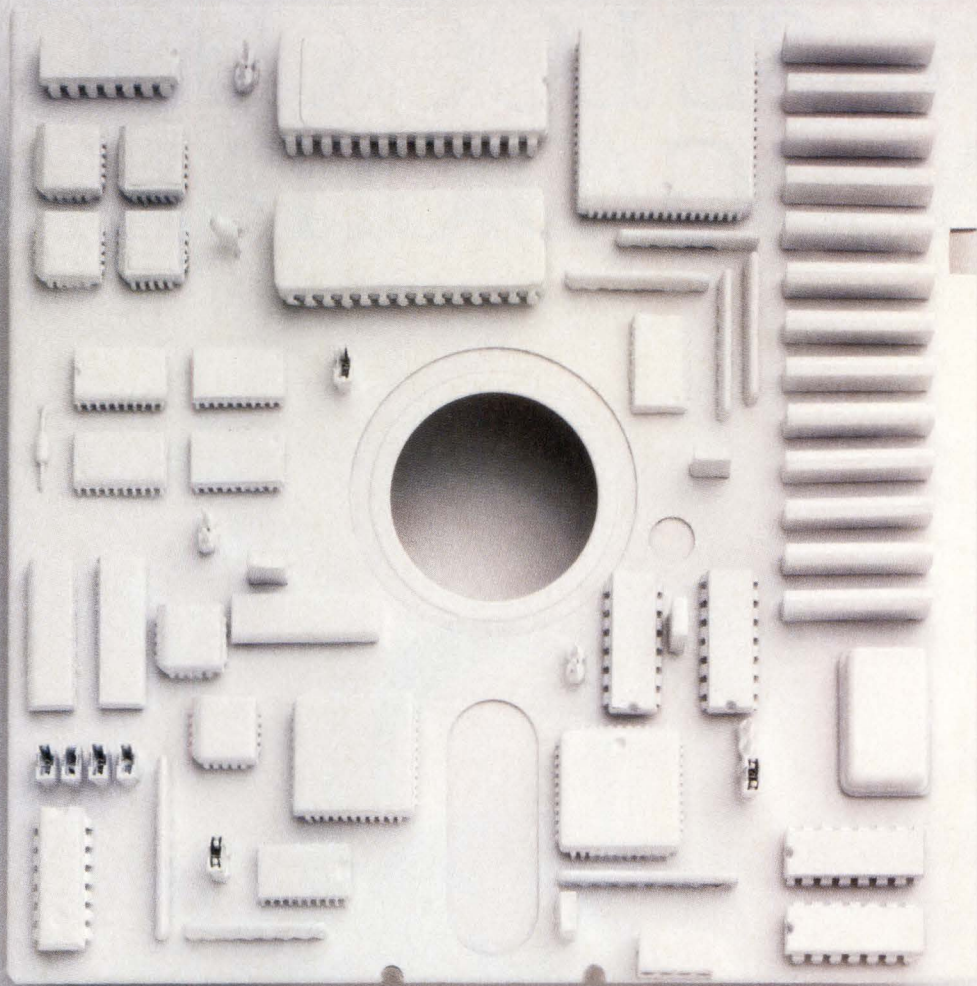
Vantage's interactive capabilities

will attract many designers, although in the short run, VHDL is likely to be its strongest selling point. By supporting the full VHDL standard, the Vantage Spreadsheet permits a mix of behavioral- and gate-level models. VHDL models are difficult to find, but as the standard becomes more widespread, a number of VHDL libraries should become available. Any model that conforms to the standard should run on the Vantage Spreadsheet.

VHDL doesn't currently support fault simulation, and neither does the Vantage Spreadsheet. That could pose a problem for military/aerospace companies, since they're the biggest consumers of fault simulation. The Vantage Spreadsheet also lacks an automatic worst-case timing verification capability, and the initial release doesn't support hardware modeling. But these limitations may be overshadowed by the simulator's interactivity and its complete support of VHDL.

CD





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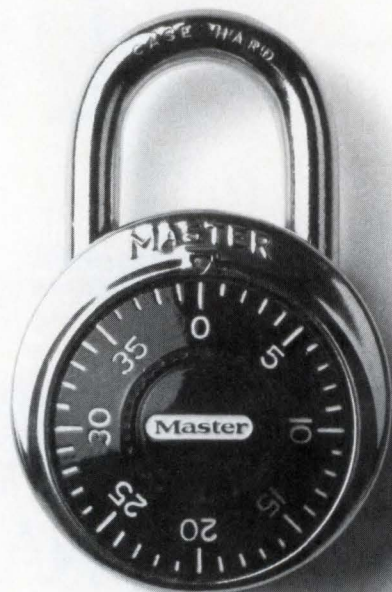
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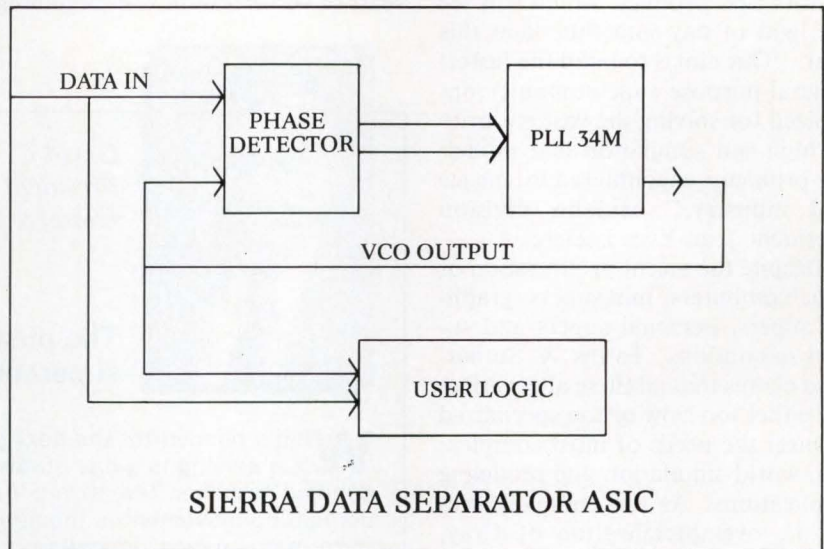
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## Moderately parallel supercomputer avoids vector hardware

About 18 months after the separation of Evans & Sutherland Computer (Salt Lake City, UT)—a leading vendor of high-end graphics, modeling and simulation products—into multiple divisions, the new computer division (Mountain View, CA) has revealed some details about its mission and its first product, which will see the light of day sometime later this year. “Our aim is to build the fastest general-purpose supercomputer optimized for solving the vast majority of high-end simulation and modeling problems encountered in science and industry,” explains division president Jean-Yves Leclerc.

Despite the recent proliferation of supercomputers, minisupers, graphics supers, personal supers and superworkstations, Evans & Sutherland claims that all these alternatives are either too slow or too specialized to meet the needs of most complex, real-world simulation and modeling applications. As the company sees it, the overspecialization of Cray, Cray-like and mini-Cray-type machines lies in their vector orientation.

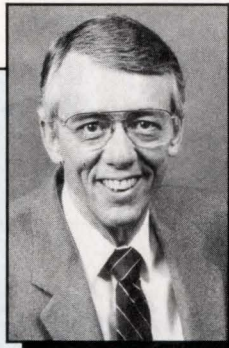
Vector processing has been the mainstay of supercomputing since the early 1970s—long enough, according to Evans & Sutherland, to firmly establish its limitations. “The key to attaining high performance in vector-processing supercomputers is the ability to vectorize the bulk of application code—say, 85 to 95 percent,” says Leclerc. “But scientists and engineers have found that typically they’re able to achieve this level of vectorization for only a handful of problems and in a narrow range of applications, and there’s a significant performance penalty when a vector machine has to handle unvectorized code. As a result, the sustained performance rates of the machines average only 5 to 20 percent of the peak performance potential.”

Evans & Sutherland has gathered an impressive array of user testimony on the vectorization problem.

The company cites, for example, studies conducted at the Los Alamos and Lawrence Livermore National Laboratories, which show that, on the average, the labs have been able to vectorize only 70 percent of their code. “Faced with this sobering assessment of where we stand after 10 years of vectorization, I’m beginning

to wonder whether vectorization has a substantial place in future supercomputer architectures,” says Los Alamos spokesman Olaf Lubeck. He estimates that Cray machines used at Los Alamos achieve only 12 percent of their potential performance.

Leclerc admits, however, “Vector math is useful for such applications as weather mapping and fluid dynamics, where a data set is subdivided and a number of calculations



*David C. Evans  
President  
Evans & Sutherland Computer*

### The push for interactive supercomputing

What’s needed for the next giant step forward in scientific problem solving is a mix of raw horsepower, interaction and tightly coupled graphics. The driving force behind today’s high-performance computing movement is the need of scientists and engineers to perform mathematical modeling: simulating with a computer the way complex processes or devices will behave in real life. The ability to model these phenomena with computer tools represents a qualitative leap forward in science and engineering—a leap that will have a major impact on every technical discipline from drug research to integrated circuit design. The potential benefits are enormous: faster time to market, reduced reliance on costly prototyping, better quality and, most importantly, the ability to solve previously unsolvable problems.

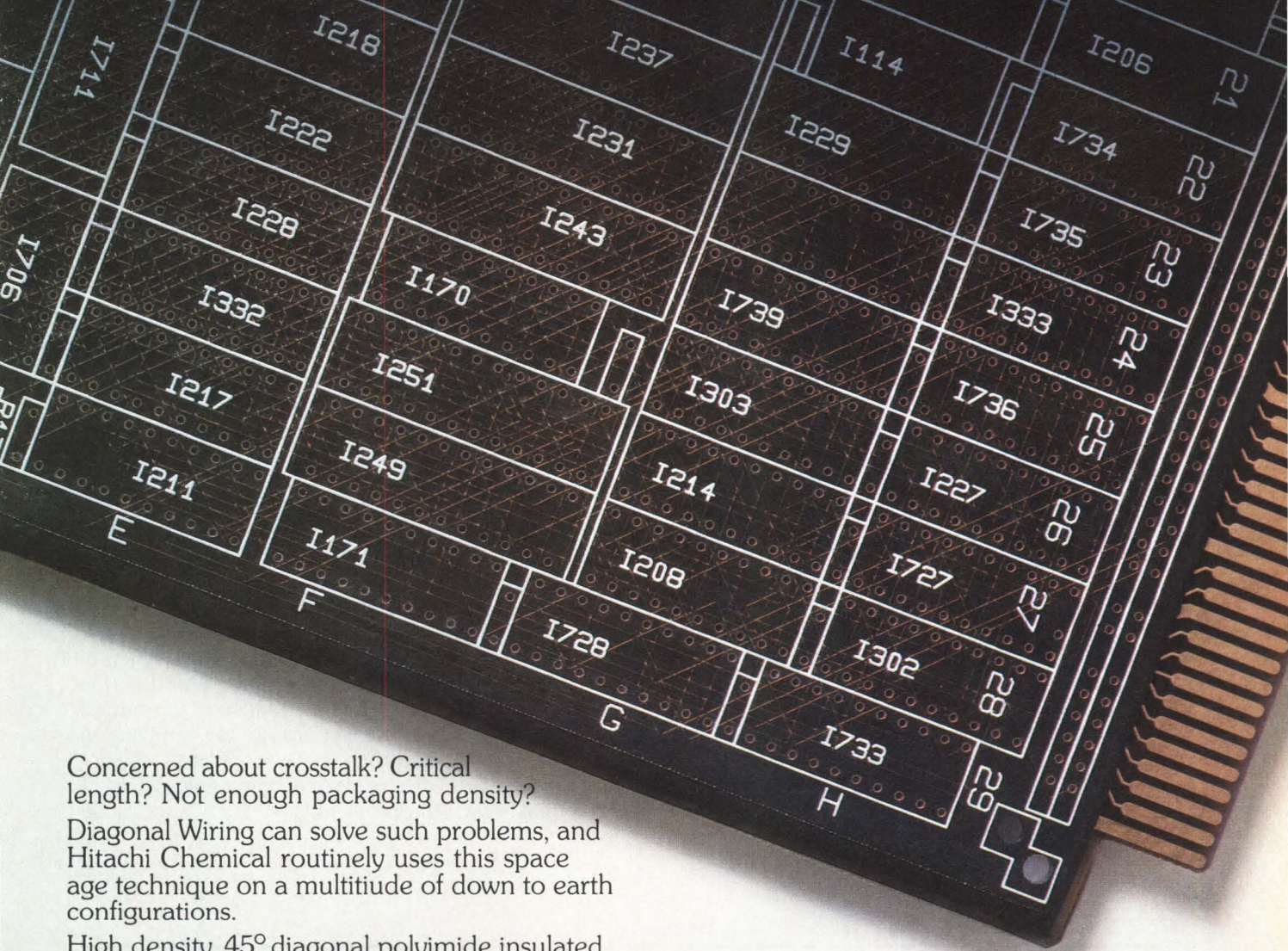
Through modeling and simulation, computers offer a much more efficient and productive alternative to conventional means of testing ideas and designs, such as manual calculation, experimentation and observation, or prototyping. Furthermore, computer-based modeling and simulation can provide the only practical way to test theories about problems beyond the scope of actual physical modeling or trials—problems raised in such diverse fields as astrophysics, cosmology and molecular dynamics.

Computer modeling and simulation has been the enabling factor for ground-breaking developments in a wide range of scientific and engineering fields, encouraging the vanguard of commercial suppliers to continually push out the bounds of visualization technology. Where chemists were once content to model molecules statically, they now want to view such simulations in real time, interactively manipulating data and watching the results. And where mechanical engineers have modeled individual parts of larger systems, they now want to simulate entire large-scale, supercomplex systems under dynamic real-world conditions and interactively adjust design parameters. Interactive modeling and simulation lets the user visualize the results of complex calculations, make intuitive judgments during processing and perform modifications to programs on the fly. The more interactive the dialog between man and machine, the more intuition, human judgment and experience can become an integral part of the computational process.

**David Lieberman**  
Senior Editor



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are applied uniformly to each section." The architecture of the coming Evans & Sutherland machine, thus, will provide for high-speed vector-type processing as well as scalar power but won't use dedicated vector hardware to balance its Mips/MFlops performance.

Evans & Sutherland's machines will consist of two to eight processors, each with 16 computational units. Each of these units can run an application on its own or with other computational units, or it can manage a segment of an application that has been parallelized and assigned to multiple units. Each computational unit contains three functional units: one for handling floating-point adds, one for floating-point multiplies and one for integer operations. "This approach will let the machine provide a high number of both Mips and MFlops without actually using vector-processing hardware," says Leclerc. The range of expected machine configurations will deliver from 300 Mips/MFlops to over 1 Gips/GFlops. Pricing will be from \$3 million to \$8 million.

While it's clear that the ability to assign tasks to the computational units as befits the application provides for a lot of flexibility, Evans & Sutherland has yet to explain the architectural wrinkles that will manage

the overall process. The heart of the system, though, will be three types of semicustom CMOS VLSI chips residing in 340-pin packages and configured in six-chip sets. The system will include a large shared memory (256 Mbytes per processor) and will provide a 10-Gbyte/s I/O bandwidth between computational units. It will be, as one might expect, a highly pipelined machine that, when desired, can be moderately parallel.

### Against the grain

Evans & Sutherland has a second major objection to vectorization, which it perceives as a form of fine-grain parallelism. In both vector machines and the so-called massively parallel computers, restructuring existing code to take advantage of fine-grain parallelism and, hence, get the most out of the machines is a difficult and time-consuming chore, and one that's often beyond the programming expertise of the ultimate user, claims Leclerc. "Machines with the power for complex problems—such as Cray-type vector machines and massively parallel machines—are of limited, special-purpose use due to the magnitude of programming effort required to tap their power," he says.

Evans & Sutherland, therefore, has opted to implement only very

high-level, coarse-grain parallelism in its new machines. "That doesn't require going deeply into the fundamental structure of existing code," Leclerc explains. Taking advantage of the machine's parallelism still requires conversion of a small amount of code, however. But, Leclerc says, "The conversion is much more intuitive because it takes place logically at a higher, more natural level for the application, using larger portions of the existing code." By the time the machines are introduced, an application development environment will be available to aid in parallel programming.

The Evans & Sutherland machines will use an operating system based on Unix 4.3 BSD with Mach extensions. Optimizing C and Fortran compilers will also be available, as will an object-code generation facility, a source language debugger, performance profilers and other development tools. "Scientists and engineers shouldn't be required to understand the details of computer science to vectorize programs at the lowest level of parallelism," comments Leclerc. "Rather, they should define the high-level modules of the natural parallelism within the application and then let development tools implement the computer science part of the problem." **CD**

## Peripherals and Memory Systems

### Erasable optical drives ready to move in on Winchester turf

**A** family of erasable optical disk drives with removable media is poised to challenge the performance of mid-range Winchesters while at the same time topping the capacity of high-end hard disks. The first members of the line from Maxtor (San Jose, CA) are Tahiti I, a 5¼-in.

drive offering up to 600 Mbytes of on-line total storage, and Fiji I, a 3½-in. drive with 160 Mbytes of on-line unformatted storage. Average seek times for the two drives are 30 and 100 ms, respectively. Tahiti I's data transfer rate of 10 Mbits/s is comparable to rates found on many Winchester drives. Fiji I has a data transfer rate of 1.9 Mbits/s.

The capacities are quoted as for-

matted or unformatted, depending on whether a drive's small computer system interface (SCSI) controller is embedded or separate. The controller on the 5¼-in. drive is embedded on the drive, while the 3½-in. drive has a separate SCSI controller, making it easy for designers to integrate different controllers and data formats. One recommended use for the Fiji I is as a floppy replacement for backup in laptop systems. Its capacity has been tailored such that it can back up a full disk of Maxtor's 170-Mbyte (unformatted) 3½-in. Winchester drive.

**Tom Williams**  
Western Managing Editor

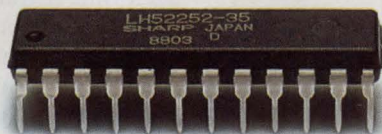




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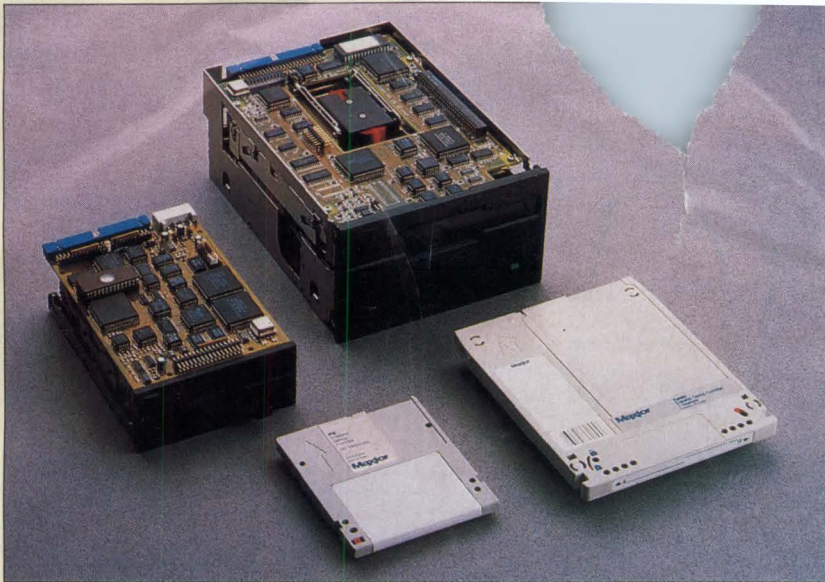
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**CIRCLE NO. 19**





Two drives from Maxtor's erasable optical disk drive family have attained Winchester-class performance. The 5 1/4-in. Tahiti I provides 1 Gbyte of formatted data storage as well as seek times of less than 30 ms. Fiji I is a low-cost-per-Mbyte 3 1/2-in. drive that provides 160 Mbytes of storage and an average seek time of 100 ms. Both drives use removable media and feature the small computer system interface.

According to Skip Killsonk, vice-president of marketing at Maxtor, the two drives represent an advance in that they have caught up with Winchester-class performance. Optical drives have long been characterized by slower seek times and data transfer rates due to the mass of laser heads and the time needed to deliver enough laser energy to the media to write data. Apparently, Maxtor has sufficiently finessed the parameters to approach low- to mid-range hard disk performance in its 5 1/4-in. offering.

Erasable optical recording uses magneto-optic technology: the heat of a laser beam is used to orient the magnetic polarization of the media to that of an ambient magnetic field. The polarity of the media then affects the polarization of an incipient laser read beam, thus determining whether a spot on the disk is a one or a zero. This means that to write a track on the disk, the track must first be erased by switching the ambient field coil to zero polarity and writing all bits, which become zero. Then the field coil is switched to one polarity for the write operation, and the laser is turned on for only those bits that are to be written as ones. Magneto-optic technology, therefore, will always write more slowly than

comparable Winchester technology because it takes two revolutions to do a write. Read operations, however, don't have this restriction.

#### Media options

The 5 1/4-in. Tahiti I has taken advantage of the intelligence that can be built into an embedded SCSI controller to offer a range of media options. Not only can users set the sectors at either 1,024 bytes or 512 bytes per sector, but they can also choose between an ANSI standard cartridge (for easy portability between drives of different manufacturers) and a special higher-capacity media cartridge. The standard cartridge offers a 600-Mbyte (300 per side) capacity, while the special higher-capacity media cartridge developed by Maxtor offers a 1-Gbyte (500 Mbytes per side) capacity.

The higher capacity is achieved by formatting the disk for zoned, or constant density, recording. Zoned recording takes advantage of the fact that the outer tracks of a disk have more linear room for data than the inner tracks. In the past, linear bit densities have been limited by the capacity of the inner tracks, which also have the highest linear velocity and, hence, the highest data rate. Intelligent buffers on the SCSI con-

troller let a drive vary the data rate of the read/write channel and match that rate to the constant data transfer rate of the host interface. Thus, as one moves out from the center, each time a track is able to accommodate an additional full sector, one is added and the data rate increases accordingly. With this method, Maxtor has managed to achieve a 40 percent capacity increase.

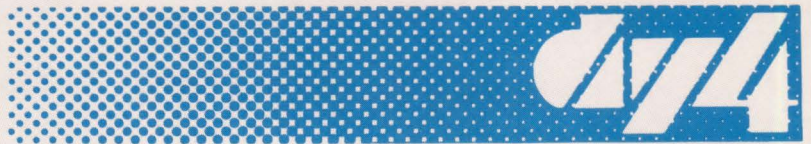
According to Killsonk, the 5 1/4-in. Tahiti I will find a home in such applications for storing drawings as desktop CAD stations and network file servers as well as in image archiving systems. The security advantages of removable cartridges will be a plus, as will be the fact that removable media effectively increases the overall capacity of a drive, if not the instant availability of that capacity.

Despite the power demands of the motor and the actuator and the additional need for the field coil, maximum power consumption for the two drives is quoted as 35 W for Tahiti I and 17 W for Fiji I. Both drives are expected to begin shipping early this fall, with volume pricing around \$2,500 for the 5 1/4-in. drive and less than \$1,000 for the 3 1/2-in. drive. Volume prices for media for the 5 1/4-in. Tahiti I and the 3 1/2-in. Fiji I are \$175 and \$49, respectively. **CD**



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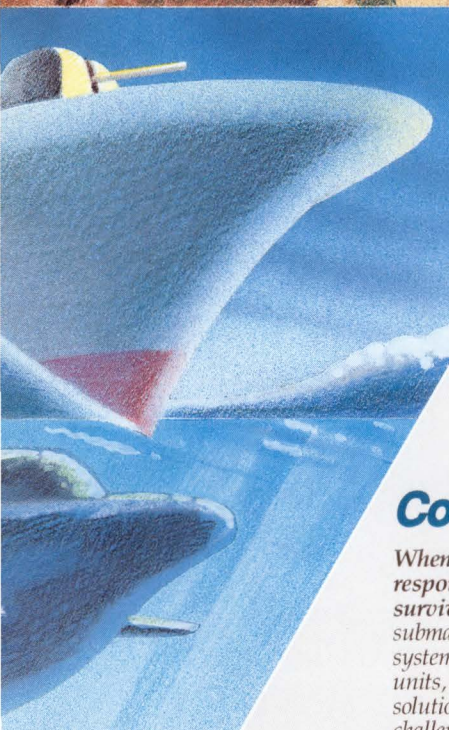
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# Linear arrays forge improvements in performance and flexibility

Until very recently, analog, or linear, arrays have been mired in the "dark ages" of the application-specific IC business compared with mushrooming developments of their digital brethren. Within the last year or so, there has been a surge in activity that promises to continue for the next several years. Developments in base silicon, array architecture and CAD environments are combining to bring new levels of performance and flexibility to the analog designer. In addition, relatively low cost, fast turnaround times and novel approaches to a migration to full-custom design hold promise for a widening base of applications.

And just beyond the horizon, new waves of technology are forming. Faster and better bipolar technologies are emerging with improved techniques for including high-voltage and high-current transistors as well as implanting high-quality resistors and other components. Analog CAD tools are maturing, gradually weaning analog designers from the breadboard to the terminal. And even a little further in the future—perhaps a couple of years away—combined analog bipolar and digital CMOS devices on the same semicustom chip may become a reality, resulting in a true bridge from high-quality, high-resolution, high-voltage and/or high-current analog circuits to the microprocessor-based systems of today.

Primarily designed for use where high operating voltages, high drive currents and/or high-performance (frequency) linear functions are required, analog arrays are perhaps one of the oldest commercial semicustom IC technologies around.

Early analog arrays consisted of a random placement of transistors,

resistors, capacitors and diodes diffused on a die and connected with a single personalizing metal layer. Compared with the evolution in digital ASICs, the development of linear arrays has been relatively slow.

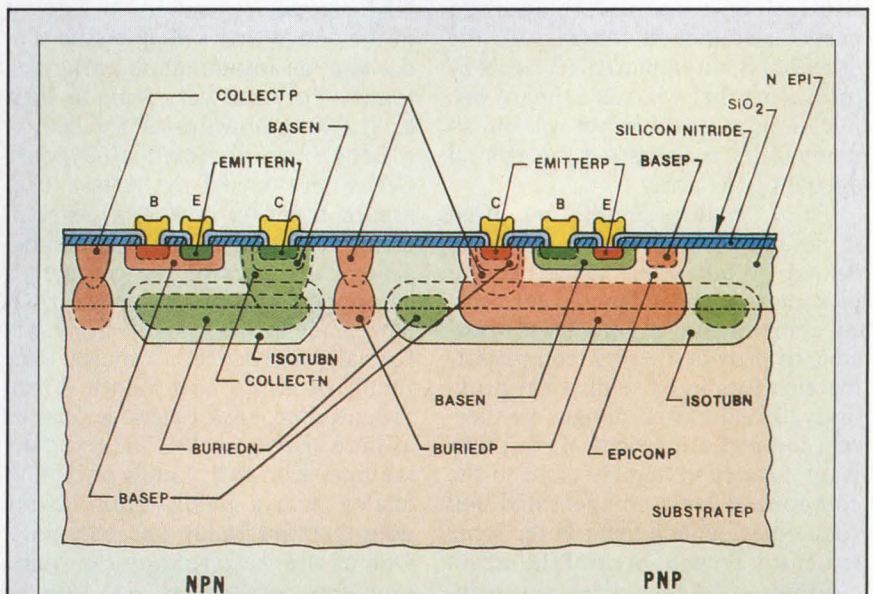
New design tools from third-party vendors—such as the Analog Workbench from Analog Designs and P-Spice from MicroSim (Laguna Hills, CA), as well as integrated schematic capture and net-list programs from Viewlogic (Marlboro, MA) and Futurenet (Redmond, WA)—are rapidly smoothing out the design environment. And many of these bring analog design to the personal computer.

## Design considerations

Many design considerations remain fundamentally the same for both digital and analog design, says David Guinther, vice-president of Custom

Silicon Inc (Lowell, MA), an independent vendor of both analog arrays and standard-cell-based products. According to Guinther, the analog ASIC designer must consider six fundamental issues (see "Designers contend with an explosion in ASICs," *Computer Design*, Apr 15, p 57): function (what the chip will do); functionality (what discrete functions will be included); ac parameters; dc parameters; packaging; and preconception (who's going to do how much of a design?).

In addition to these fundamental considerations, analog array design requires careful attention to other critical areas. In straightforward digital designs, the key elements are usually the availability of macrocells and compilers rather than the base silicon process. The raw gate speed is determined by the minimum transis-



AT&T's complementary bipolar IC process results in one of the fastest arrays available. The NPN transistors have a beta of about 100 and an  $f_T$  of 4 GHz; PNP transistors have a beta of 40 and an  $f_T$  of 2.5 GHz. The N-type collector of the NPN transistor is surrounded by P-type material on the sides and bottom. By keeping the substrate at the most negative circuit potential, the collector-substrate PN junction is always reverse-biased.

Warren Andrews  
Contributing Editor



tor dimensions and process. Other variables such as transistor sizing for higher fan-out is managed in software. In analog design, there are many more variables—components are not all created equal. Factors to consider include transistor sizes and types, transistor performance, resistor and capacitor types, thermal effects, total power dissipation, and the amount of circuit that must be breadboarded.

Cost, volume and the possibility of alternative approaches are also more significant with analog arrays than with digital circuits. With digital circuits, for example, there are often only two alternatives—ASIC parts or standard parts. Virtually no handcrafted, full-custom digital VLSI design activity is going on.

Many analog circuits, however, can still benefit from careful handcrafting. There are a number of reasons for this, the first being that the total number of devices on a chip is usually somewhat limited, making hand-drawn circuits possible. Second, clever designers can take advantage of flexibility in transistor size to optimize the performance of a particular function. Arrays, on the other hand, attempt to offer a mix of transistors that will suit as many applications as possible, yet without so many types as to restrict the general appeal of the array.

Third, analog circuits are often somewhat fussy if they're unevenly heated. While some arrays try to provide thermal balancing for critical components, it's not always possible to provide thermal compensating elements in close physical proximity. Handcrafted designs let thermal compensating elements be physically located extremely close to the component being compensated and sometimes include them in the same structure. Fourth, none of the arrays currently available offer any technique for trimming once a device is made. With handcrafted designs, zener-zapping or even laser-trimming can be incorporated such that dice can be adjusted before packaging—or after, depending on the type of package.

Finally, there are cost considerations. Significant die area—as much as 50 percent—can be saved in handcrafted circuits over array circuits. Depending on the circuit, this could shift the price/volume crossover point to considerably lower volumes for custom parts than might traditionally be expected.

#### **Fast turnaround**

A key benefit of analog arrays—similar to that enjoyed by their digital counterpart, gate arrays—is very fast turnaround time. “Most analog arrays require at least a couple of revisions before they go into production,” claims Charles Gopen, vice-president of marketing for Micro Linear (San Jose, CA). The large number of parameters makes it far more complex than designing a digital circuit. It's also difficult to predict the exact performance of a completed device; the tools just aren't as good as digital design tools, he says.

Turnaround times for analog arrays range anywhere from two to eight weeks, depending on the vendor and the complexity of the chip. NRE charges depend on the amount of the design that's done by the vendor and the amount done by the customer. They can vary from as little as \$1,000 to upwards of \$30,000.

Sony Corp of America (Cypress, CA) offers one of the fastest turnaround times for prototype development, claims Jean-Pierre Laussade, general manager of the company's component products division. A newcomer to the market, Sony will formally introduce its master-slice family of arrays next month. Turnaround time, says Laussade, can be as little as two weeks. The company is about to bring its family of bipolar analog arrays public after having used them internally for some time. One of the reasons Sony can quote such fast turnarounds, he says, is that it runs a batch of wafers every two weeks—combining wafers for internal use with those of customers.

Also, Sony uses an approach in which a large block, or master chip, on a wafer contains five different array types in a 4- $\times$ -4-chip array with

one test chip and one dummy. “This way, the customer doesn't have to pay for a whole wafer full of prototypes, which significantly lowers NRE charges that typically run from \$2,000 to \$5,000 for a design,” comments Laussade.

Micro Linear's Gopen sees linear array products characterized by certain attributes of performance, supply voltage, drive current, flexibility and design-tool support. “To some extent, there are some distinct categories,” says Gopen. “For example, in the very high end, devices operate in the multiple-GHz range. These devices emerged from the internal needs of equipment manufacturers who took their proprietary technology out to the marketplace.”

#### **High-end solutions**

The high end has, for the most part, limited applications—primarily in government, instrumentation and aerospace—where performance, not cost, is the predominant consideration, according to Gopen. High-end analog array solutions are provided by Tektronix (Beaverton, OR), VTC (Bloomington, MN) and AT&T (Allentown, PA).

Tektronix's QC-4Quickchip addresses the high-end market. The company used its proprietary technology employed in developing its 1-GHz scope to create the Quickchip. The semicustom array offers almost 300 NPN transistors with a typical  $f_T$  of 6.5 GHz and about 175 PNP transistors with a much lower cut-off frequency of 20 MHz. It also includes more than 1,200 resistors and about 30 capacitors. In addition, the array provides almost 300 equivalent ECL gates with typical delay times of under 400 ps.

VTC, a division of Control Data Corp, offers a relatively small array comprising close to 100 NPN transistors (72 medium size and 24 low noise) with a typical  $f_T$  of 6 GHz. Its 48 PNP transistors fabricated as vertical rather than substrate transistors provide an  $f_T$  of 1 GHz. In addition, VTC's array includes 24 Schottky diodes, 120 resistors and 26 capacitors located around the periphery of the



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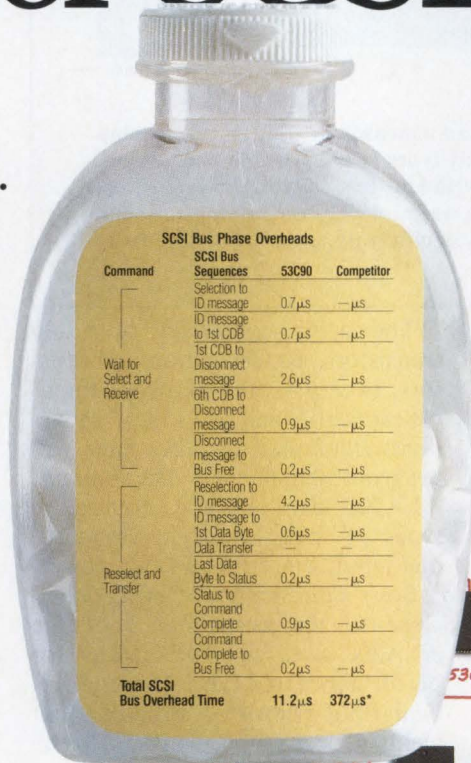
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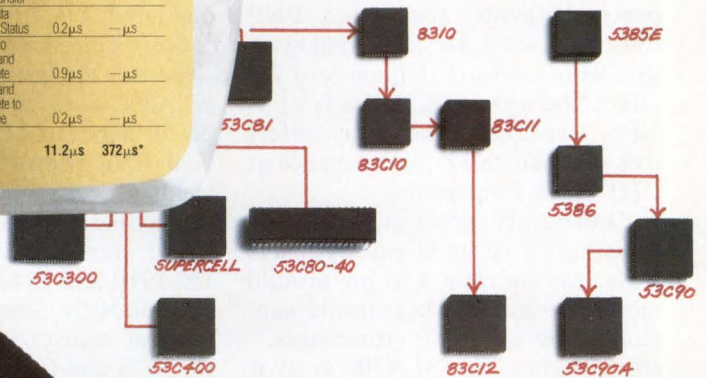
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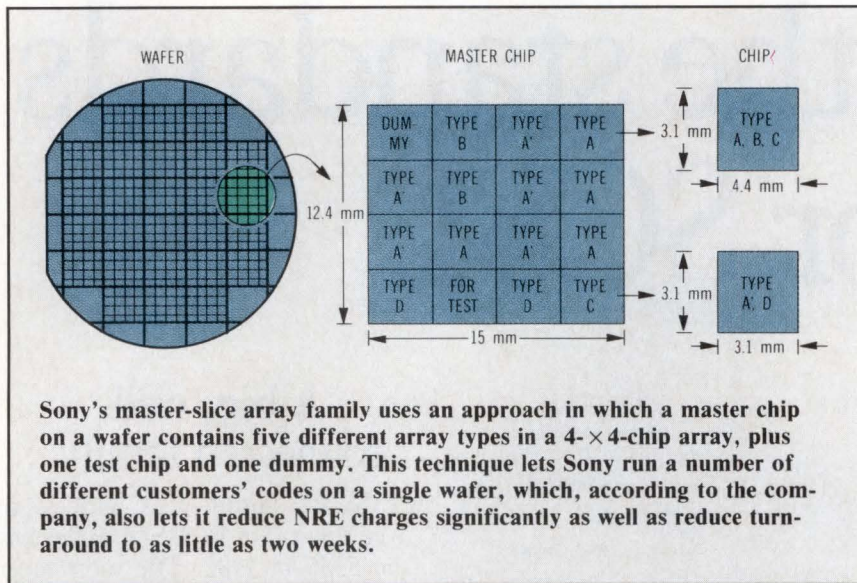


NCR Microelectronics Division

CIRCLE NO. 20

\*Electronics Magazine August 20, 1987 Pg. 65





die. The chip is divided into 12 blocks, or tiles, to help simplify the layout of macrocells.

AT&T's high-performance offering, the ALA200, is fabricated in what AT&T calls its complimentary bipolar (CBIC) process. According to senior engineer Ren Jenkins, the process provides the fastest PNP transistors available on an analog array, with a cut-off frequency of 2.5 GHz. And with the 4.5-GHz  $f_T$  of its NPN transistors, the array offers true complimentary performance at UHF/VHF frequencies.

"Inherently good-quality PNP transistors free up circuit designers from wasting time working around more conventional lateral and substrate-collector PNP transistors," says Jenkins. The ALA200 array is designed on a regular grid pattern that provides clearly defined routing channels, which the company claims simplifies design and makes it easy to implement macro functions.

In addition to conventional dual-metal layers, AT&T offers a single-metal option as well as a thicker gold layer option the company calls thick metal. This interconnect material is available with very low sheet resistance for higher-current applications. The conventional metal has a current capacity of 2 mA/micron of metal width, while the thick metal has a current capacity of 14-mA/micron metal width.

The array comprises over 200 transistors, almost a thousand resistors, twenty 1- to 5-pF programmable capacitors and two 150-pF capacitors. Implanted resistors have values from 50 to 6,000  $\Omega$ . The standard ALA200 array includes four basic types of modules; eight standard, one input, one trim and two power.

Sony's masterslice offering comes close to the performance of the ALA200 with an NPN transistor performance of 3 GHz. It uses a vertical PNP transistor structure that yields a performance of 350 MHz. Depending on which chip type is selected, transistor count varies from 180 PNP and 274 NPN to 384 PNP and 530 NPN. Sony also offers a variety of transistor types, including six NPN and three PNP types.

Devices are interconnected by two layers of metal. The total resistance available on chip ranges from 2.4 M  $\Omega$  to 17.2 M  $\Omega$  depending on the chip version selected. Similarly, capacitance varies from 358 pF to 744 pF.

#### Minitile architecture

Micro Linear is also getting into the high-performance end of the analog array business with its recently released FB3600 array family. The 12-V array includes 1-GHz NPN transistors, but with relatively low-performance PNP transistors. "But the slower PNP transistors don't present any real performance problem. In

designing a performance system, you don't put the PNP transistors in a critical speed path," says Gopen.

The FB3600 varies significantly from other high-performance arrays and from its precursor, the FB300, in the architecture of its tiles. On most conventional arrays, tiles are relatively large, permitting the inclusion of an entire macrocell on a tile. Also, tiles are separated by dedicated routing or wiring channels.

In the FB3600, Micro Linear divided its array into smaller sections, or minitiles. The company has defined five basic minitiles; they vary from general-purpose tiles to high-precision tiles with precision resistor links. Other tiles contain low-noise transistors and output transistors that are capable of driving up to 100 mA. "Each of the three members in Micro Linear's FB3600 family—the FB3310, the FB3620 and the FB3630—contains a mixture of different minitiles carefully selected by the company to reflect the most frequent usage," says Gopen. "The selection of minitiles and components within the tiles is based on Micro Linear's design experience and is organized to permit both high component use and the inclusion of complex functions."

In addition, the tiles are butted against each other, minimizing routing channels. "The array resembles the sea-of-gates approach that's used in digital gate arrays," notes Gopen. With the two layers of metal interconnection, instead of one layer, signal lines are routed on top of the minitiles.

"One of the major objectives in developing the 3600 family—aside from performance—was to provide a very cost-effective array," continues Gopen. The combination of the minitile architecture and the elimination of most of the routing channels has resulted in a die almost 50 percent smaller than that used in the FB300 arrays. "The overall cost of integrating a system," says Gopen, "can run anywhere from 10 percent to as much as 50 percent less than integrating the individual functions in discrete ICs."

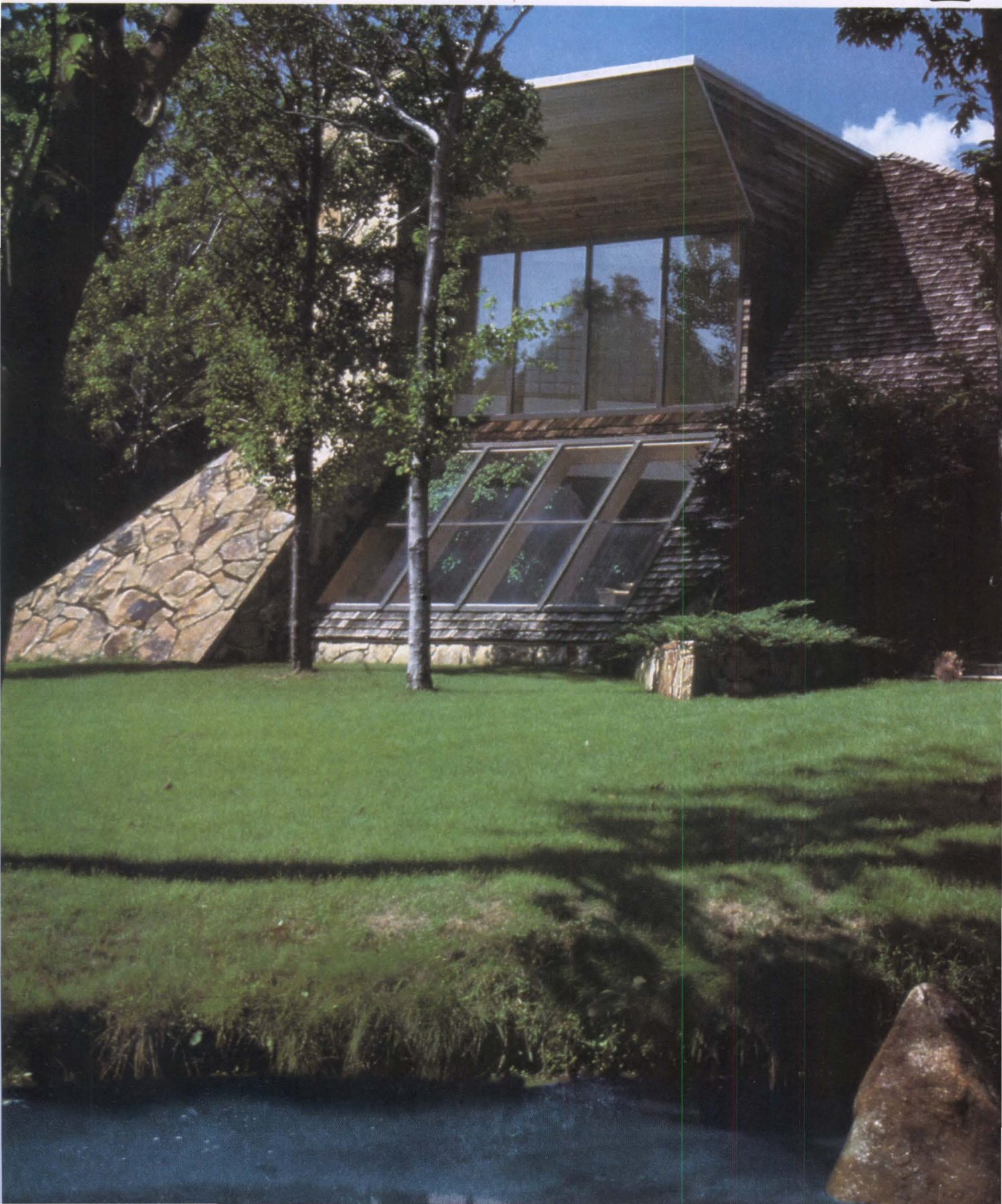


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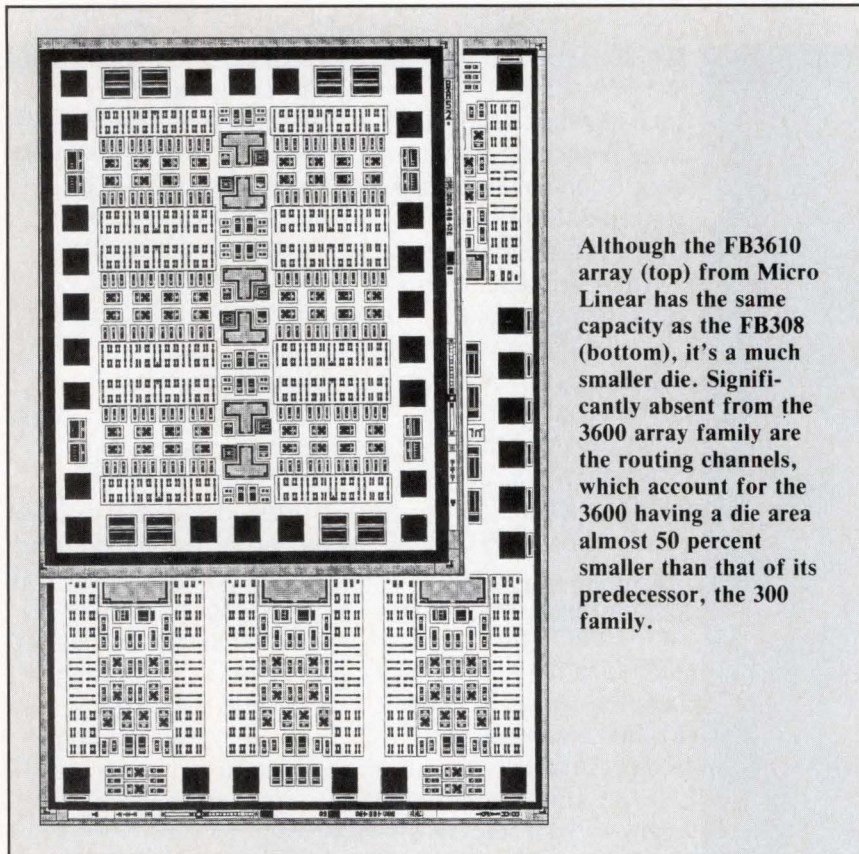


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Although the FB3610 array (top) from Micro Linear has the same capacity as the FB308 (bottom), it's a much smaller die. Significantly absent from the 3600 array family are the routing channels, which account for the 3600 having a die area almost 50 percent smaller than that of its predecessor, the 300 family.

Another benefit of Micro Linear's architecture, says Gopen, is a relatively quick and painless migration from an array to a full-custom part. In making the conversion, the same parts are used in the custom version as in the array, only unused parts are eliminated. "The technique has been so effective," says Gopen, "that the company is using it in the development of some of its standard parts."

A high-performance array family from Plessey Semiconductor (Scotts Valley, CA) is in the 300- to 400-MHz range, with high-performance NPN transistors and lower performance PNPs. Richard Padovani, Plessey's strategic marketing manager, claims the company's gridded tile-array structure eases layout and becomes a correct-by-construction technique. Further, he says, the tile architecture allows the definition of a wide range of macros through the use of the process's single-metal interconnection scheme.

The family of nine arrays comprises a variety of densities, transis-

tor types and component assortment to suit almost any array configuration. "With over 3,000 integrations," Padovani claims, "Plessey has more experience in designing and knowing what components are called for on arrays than just about anyone else in the business."

Meanwhile, Exar (Sunnyvale, CA) has forged out in yet another direction with its Flexar (Flexible Array) architecture. Instead of diffusing a particular type of transistor on its base substrate, it diffuses sexless transistors that can be tailored, at the time of metalization, to be either PNP or NPN types. Called Twinstors, the configurable transistors provide an  $f_T$  of 500 MHz as an NPN transistor, dropping to only 5 MHz as a PNP.

While Twinstors can act as either an NPN or PNP transistor, when not used, it can serve as either a 90- $\Omega$  crossunder or as a pair of 500- $\Omega$  resistors. This further eases designing because these resistors are located near active elements.

The company's Beta Flexar arrays are currently available in three different densities with 100, 180 and 240 Twinstors, respectively. Also, a smaller, 66-Twinstor version will be released soon, according to Surjit Nijjer, Exar's custom linear products marketing manager.

Nijjer also hints that Exar will be coming out with a new family of arrays—the Gamma series—perhaps as early as next month. Though he didn't reveal all the details of the new series, he claims the new arrays will be much denser, with a different structure than the Beta series. They will also have an upper frequency limit of 1.5 GHz.

### Higher-voltage arrays

Many analog array applications call for supply and operating voltages above the 20- to 25-V range. Many standard devices such as op amps, digital-to-analog converters and analog-to-digital converters operate at  $\pm 15$  V. AT&T's ALA400 family of arrays fall in the mid-voltage area with a 33-V capacity. This is a family of general-purpose arrays offering high-performance NPN and PNP transistors, a limited number of power outputs and some JFET modules for high-input-impedance applications, says Jenkins.

Like the ALA200, the ALA400 is fabricated in AT&T's CBIC process, yielding PNP and NPN transistors of almost equal performance. The  $f_T$  for NPN types is 350 MHz, degrading to only 300 MHz for the PNP transistors. The ALA400 uses two layers of metal interconnect, and like the ALA200, is available with an optional high-current thick metal.

Plessey's 40-V MV series of arrays is also targeted at the general-purpose market. "In the MV family," says Plessey's Padovani, "the company has also incorporated MOS capacitors on-chip. These are far less sensitive to voltage than the easier-to-build junction capacitors. In addition, the arrays incorporate implanted resistors that offer linear high-value resistances, letting the chip operate at lower currents."

The MV arrays also use a config-



urable transistor, something similar to the approach used by Exar, Padovani adds. He points out, however, that extreme care must be used in designing any device where the transistor is configured in the final metalization, or else there can be some catastrophic problems. There is a tendency to develop an "EPI shift," which can result in a mismatch of base and emitter contacts. For its part, Plessey has developed a technique that provides the tight matching required in many analog circuits. "Plessey loosely refers to its single-transistor structure as a Monistor," says Padovani. The company may back away from the use of the trademarked name in favor of simply calling the device a universal NPN/PNP device, however.

The universal NPN/PNP device lets many circuits be easily configured that would be difficult to design if only fixed transistors were available. "Not every design uses PNPs and NPNs in a fixed, or even predictable proportion," says Padovani. "Frequently, much real estate is chewed up getting the right combination of transistors."

### Still higher voltage

Many applications for these analog arrays—such as smart-power or telecommunications applications, or those used in an inductive environment—require a more robust technology. AT&T's ALA300 family has a 90-V capability. Once again, AT&T's CBIC technology is used, resulting in NPN transistors with an  $f_T$  of 350 MHz and PNPs with a 300-MHz  $f_T$ . The ALA300 consists of two device parts, the 300 and the 301. Both are relatively small in terms of device count: the ALA300 has 13 NPN transistors, 15 PNPs, 108 resistors, three capacitors, a single diode and 30 bonding pads. The 301 has four times the components of the 300 with the exception of bonding pads, of which it has 32.

Other high-voltage arrays include the 50-V Genesis from Cherry Semiconductor (East Greenwich, RI), a 65-V version of the Quickchip from Tektronix and the 100-V MPD-8020

from Micrel (Sunnyvale, CA). Designed for a variety of high-power, high-voltage applications including switching power supplies, motor control, lamp drivers, printer solenoid drivers, relay drivers and a host of other switching applications, the 8020 combines CMOS, DMOS and bipolar components.

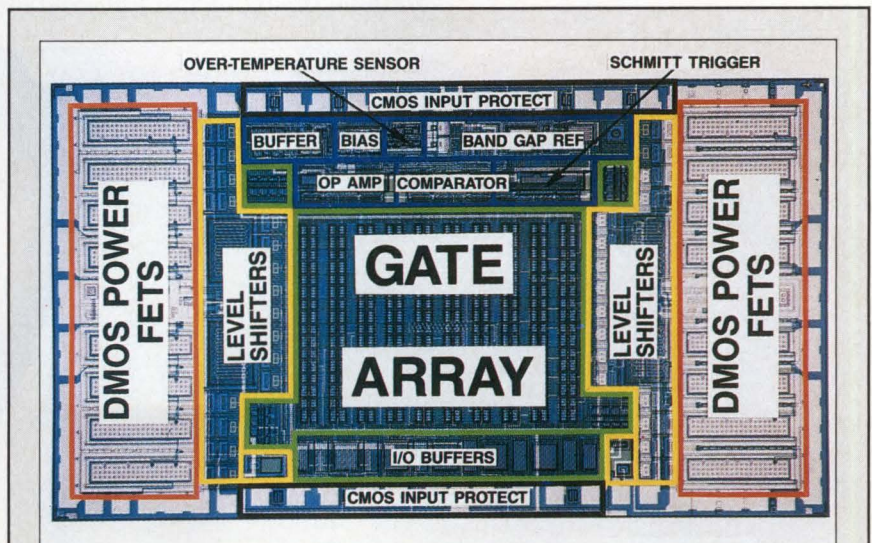
At the power ends (located at either end of the 256-mil-long chip) are 16 N-channel DMOS power FETs, each of which is located in its own isolated tub. Because each device is fully floating (sources, gates and drains), there's no restriction on their use and they can be used for push-pull drivers and in H-bridge designs. The DMOS FETs are rated at 100 V and 200 mA, with an on-resistance of 10  $\Omega$ . The company claims that the FETs can be paralleled, resulting in a 100-V, 3.2-A configuration with 0.625- $\Omega$  on-resistance for single, half-bridge, full-bridge or bilateral switches.

In addition to the rugged outputs, the array contains an uncommitted array of 200 CMOS gates, a dozen TTL/CMOS I/O buffers, three op amps, three comparators, three Schmidt triggers, a unity gain analog

buffer, a band-gap reference, an over-voltage sensor, a voltage pump to drive the high side of gates above  $V_{DD}$ , 16 medium-current sink pre-drivers, and 16 high-voltage, level-shifting, high-side pre-drivers. And, there's a zener diode and a collection of resistors and capacitors. In addition, the surrounding pads leave room for plenty of high-voltage and logic I/O as well as  $V_{CC}$  and  $V_{DD}$ .

Turnaround time for Micrel's array is nine weeks from initial customer interface to the test and delivery of 25 prototype chips, according to Micrel. The 8020 is packaged in a 44-lead plastic leaded chip carrier; however, either 11 or 22 pins are fused together and attached to an on-board heat sink. Micrel says its array is designed to satisfy designers who are champing at the bit to develop smart-power systems yet can't find ICs to suit their applications.

Most forecasters see commercial mixed-mode arrays appearing in about two or three years. "There's still a lot more to be done with bipolar devices," says Micro Linear's Gopen. Device sizes are shrinking, parts are moving faster and supply voltages are going down, he adds. **CD**



The MPD-8020 high-voltage semicustom array from Micrel incorporates a dense CMOS gate array in its center, 16 fully floating N-channel DMOS power FETs, and a variety of other functions. Each DMOS FET is fully floating, so there's no restrictions on their use. At 100 V, the array has the highest operating voltage of any commercial array.



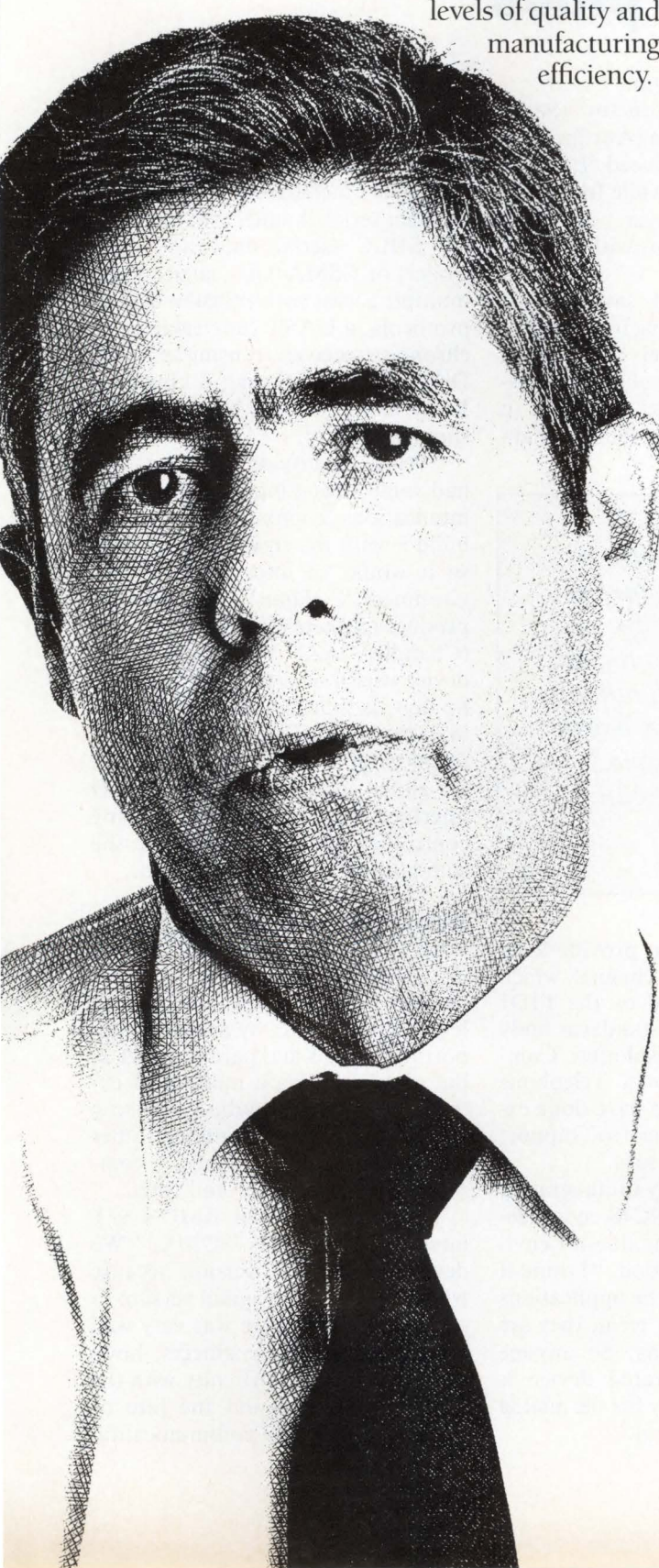
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# The ISDN puzzle takes shape as the pieces fall into place

This year may just be the first year of significant silicon for the Integrated Services Digital Network (ISDN). Last year, chips emerged to support the S and T interface reference points in the ISDN network, prompting a lively debate about what layers of the ISDN specification should be supported by the hardware. This year, vendors are revising last year's offerings, including moving toward higher levels of integration. Support for other points in the network, notably at the R and the U interface points, is also starting to appear. And there's a sure sign that the industry is getting serious about ISDN: development boards are beginning to appear.

Furthermore, one of last year's problems—the inability of chip sets to communicate with each other because of differing bus structures—has even been partially solved, at least in Europe, where the four major European telecommunications companies have agreed upon one bus structure. Unfortunately, however, that problem still remains in the United States.

## The S/T interface

Most of the S/T interface chips introduced last year supported only Layer 1, but some offered higher levels of integration, and that trend toward integration has been apparent this year.

Siemens (Munich, West Germany) has offered ISDN chips since 1986. The earliest chips were the 2080 S/T interface chip, a Layer-1-only device, and the 2070 controller for the link access protocol in the D channel (LAPD). These two devices are now also available on a single chip, the 2085. Also available from Siemens is the 82520, which incorporates two

2070s on the same chip.

National Semiconductor (Santa Clara, CA), Motorola (Austin, TX), and Siemens introduced Layer-1-only chips last year, while Intel (Folsom, CA) offered Layer 1 as well as partial Layer 2 support with its chip, the 29C53.

Available only in samples last year, the 29C53 is going into production now. And Intel has already made changes to the chip. The majority of the changes, according to Pat Weston, strategic planning man-

*“The U interface has massive potential if at some stage all phone lines go digital. There are 200 million phone lines in North America alone.”*

*—Pat Weston  
Intel*

ager at Intel, were to provide logic for the S bits in the Q channel, which were recently defined by the T1D1 committee, the U.S. standards body of the CCITT (Consultative Committee of International Telephone and Telegraph). “We have done extensive modifications to support those bits,” Weston says.

As to the possibility of integrating the 29C53 and the 29C48 coder/decoder (codec), Weston doesn't envision that happening soon. “I think if you look at most of the applications for ISDN in the near term, they are data-only applications. So anyone who buys an integrated device is probably going to pay for the analog function and not use it.”

Intel also introduced last year a device that can handle LAPD and more. The 83C152, which Intel labels as a universal communications controller, includes an 80C51 CPU, a global serial channel that can handle SDLC (serial data link controller) or CSMA/CD (carrier sense multiple access with collision detect) protocols, a UART (universal asynchronous receiver/transmitter), two DMA channels, timers, 8 kbytes of ROM and 256 bytes of RAM, and standby control.

“When specifying the part, we had some strong input from a communications company on how to build it with the right peripheral set so it would fit into the ISDN environment,” claims Tom Alberts, product marketing engineer at Intel (Chandler, AZ). What makes the device useful as a terminal adapter, he says, is that data can be brought in from a terminal on the UART (local serial channel) and sent out on the global serial channel to the SLD interface of the 29C53. The standby control lets the 80C51 be halted; the standard 80C51 can't be halted.

## Higher levels of integration

With the introduction last year of its 79C30, Advanced Micro Devices (Austin, TX) offered the highest level of integration by not only supporting Layer 1 and part of Layer 2, but also including a number of extras, such as an audio-processing block that includes, among other telephone-related functions, a combined telephone codec and filter.

The new version of AMD's S/T interface chip is the 79C30A. “We developed this new version because when we took the original version to market, the hardware was very well accepted; software engineers, however, found some difficulty with the protocol software and the rate of interruption of the communication

Steven L. Martin  
Contributing Editor



CPU," says John Landau, directorate marketing manager at AMD. Both AMD chips use a local CPU for B and D channel processing.

Based on feedback from software engineers, AMD has added to the chip transmit and receive first-in, first-out (FIFO) memories and has altered the interrupt structure, making interrupts maskable. The FIFOs can handle back-to-back packets before the FIFO has to be emptied. Thus, the FIFO doesn't have to be emptied when the packet processing on one packet is complete; rather, processing on the next packet can begin with the first packet still in the FIFO. "All of these things were done to minimize the burden on the CPU and to allow it to be used for other functions in the terminal," Landau says. The 79C32A is the equivalent revised chip without the audio block.

A new chip from AMD, due out in samples this summer, is the 79C401, which offers partial LAPD support. This is a data link controller similar to the one in the 79C30/32, but is "much enhanced," says Landau. Defined by AMD in conjunction with AT&T (Holmdel, NJ), the 79C401 was designed from the software perspective. "We found that in the design of ISDN equipment, 90 percent of the investment is in the software; so we're trying to minimize CPU intervention," Landau says. With this chip and a local processor, entire packets of any HDLC (high-level data link controller) type of protocol can be processed transparent to the host system, thus leaving the host system free for higher level communications tasks. The device is designed to go in terminal equipment and can process up to 2 Mbits/s. It has a 32-byte receive and 16-byte transmit FIFO, a DMA interface and a USART (universal synchronous asynchronous receiver/transmitter). It allows stacking of up to four back-to-back packets.

Earlier this year, NEC Electronics (Mountain View, CA) introduced its LAPD chip, the 72305, which handles all of Layer 2, according to Phil Lim, product marketing manager.

"Some people are using HDLC controllers coupled with software; some are combining all the Layer 2 functions in software," explains Lim. "We've decided to implement all of Layer 2 LAPD protocol in hardware because it off-loads the host processor and lets it handle higher layer functions." The 72305 handles both basic and primary rates. Like the AMD 79C401, it requires a local processor, which the Intel 83C512 does not. NEC Electronics also offers a separate LAPB (link access protocol in the B channel) controller, the 72107.

The company plans to introduce by mid-1988 an S/T interface chip, the 98201, that supports only Layer 1. A second-generation device will integrate the S/T interface and the 72305 LAPD controller, says Lim. An optional 2-wire interface (ping-pong transceiver) is available now.

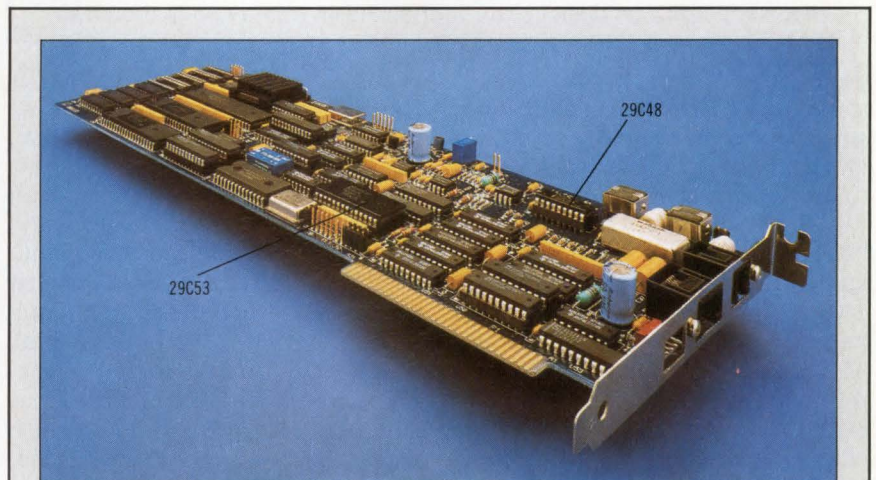
#### Missing links, bottlenecks

One of the biggest gaps in the ISDN picture is the U interface, the 2-wire, basic-rate connection from the customer premises, home or business, to the central office. Until recently, this interface hadn't been defined. "Certainly, U-type transceivers are not available, and there's a lot of fuzziness about when they will be available, and even more fuzziness

about whether they are going to be cost-effective," notes AMD's Landau. AMD sees more promise in T1 and CEPT (Conference of European Post Telecommunications) primary-rate interfaces.

Others, however, think differently. While Intel declined to comment specifically on U interface development, the company does admit an interest. "The U interface has massive potential if at some stage all phone lines go digital," Intel's Weston claims. "There are 200 million telephone lines in North America alone." On the negative side, says Weston, it isn't clear how fast ISDN is catching on. Although the U specification isn't entirely complete yet, Weston maintains that it's sufficiently well defined now to begin developing products.

Like most others, NEC Electronics is awaiting final definition of the U interface from the T1D1 committee before bringing out a device. "We're going to come out with a U interface device, but we want to make sure that it's 100 percent compliant to the standards," Lim says. One of the remaining problems is the definition of the line length. A previous problem has been the line code definition, but it seems quite certain that 2B1Q will be the chosen line code for the North American stan-



The IDK 29C53 ISDN development kit from Intel includes two PC-compatible boards with the 29C53 S interface and the 29C48 codec and filter for voice support. The kit, priced at about \$5,000, includes software.



## The basics of ISDN

The Integrated Services Digital Network (ISDN) is an all-digital communications network. It applies not only to data but to voice and video as well. When fully installed, it will provide a global connection of telephones, computers, facsimile machines, and so forth, that could well justify the use of that popular word, connectivity.

In discussions of ISDN, two fundamental concepts arise: reference points and layer support. There are four reference points in the network: R, S, T and U. R is the interface from older, non-ISDN equipment, which requires an adapter to become compliant with ISDN standards. The S interface point is where ISDN terminal equipment on a customer premises can connect to network termination equipment. When multiple terminal equipment is connected to a single network terminator, that network terminator is then connected to another network terminator that provides the transmission out of the customer premises. The interface between those network terminators is the T reference point. The transmission line out of the customer premises is the U reference point. The U reference point is a two-line connection, whereas the S and T reference points are four-line connections.

There are seven layers to the Open System Interconnection model of the International Standards Organization. Layer 1, the Physical Layer, deals with the physical transport of the bit stream. Layer 2, the Data-Link Layer, deals with the link access protocol on the D channel (LAPD). To get access to the B channels, which carry the actual user voice or data communication, certain protocols must be adhered to; the D channel handles these formalities. Layer 3, the Network Layer, provides routing and relaying through intermediate systems. Layers 1 through 3 are the layers of primary interest to IC manufacturers.

Layer 4 is the Transport Layer, which provides transparent, error-free transmission between end systems. Layer 5, the Session Layer, handles the dialogue between communicating processes. Layer 6, the Presentation Layer, is concerned with standard presentation of information. And Layer 7, the Applications Layer, provides the user with network services via application programs.

ISDN transmission begins at the end-user location at the application level and proceeds through the layers to the Physical Layer on which the communication is transported. From there, it travels through the network, which might involve several switching stations for long-distance transmission, to the targeted end-user, where the transmission then climbs its way back up the various levels to the application level.

tem #7, which specifies how ISDN switches must communicate signaling information, is used for signaling between central offices and is related to call setup and teardown. "One of the big issues that needs to get sorted out before the tidal wave of ISDN hits is Signaling System #7," says Intel's Weston. "Until then, the best we can do is have islands."

Signaling System #7 involves all seven layers of the Open System Interconnection (OSI) model for ISDN. Although Signaling System #7 isn't completely defined for all layers, NEC Electronics is providing full support to Layer 2 with a new IC, the 72307. It's identical to the company's 72305 LAPD chip, except for a firmware change that makes it compliant with Signaling System #7. This is the first Signaling System #7/Layer 2 chip on the market, according to Lim. Production will begin in July.

### Chip talk

A year ago, bus structures for inter-chip communication seemed to be proliferating. It appeared quite certain that different chips from different vendors wouldn't be able to talk to each other—despite the fact that the overall goal of ISDN is global communication. But this situation has somewhat improved recently—at least in Europe. An enhanced version of the IOM (ISDN Oriented Modules) bus from Siemens has been adopted by four West German telecommunications companies—Alcatel, Italtel, Plessey and Siemens. The enhanced IOM bus, as does the original IOM bus, transports B and D channel information and includes a monitor channel. The enhancement adds no lines. The bus consists of receive and transmit lines, a clock, and a frame signal.

"This is now a quasi-standard of the European telecommunications industry," notes Siemens' Lerach. "We defined that interface together. We improved the IOM in a way that, over the monitor channel, a more enhanced protocol allows better communication between components connected to the bus."

dard. In addition to line length, some issues related to maintenance still need to be resolved, says Lim. Nevertheless, NEC Electronics plans to introduce a U interface next year.

Mitel (Kanata, Ontario) also believes the U interface shouldn't be ignored. In fact, the company has a 2-wire transceiver, the 8972, that partially meets the U specification. Moreover, Mitel claims to be working on a new version—the 8910 Digital Subscriber Line Interface Circuit—that will meet the complete U specification. The part will be announced around November, when samples will become available.

While others are still only talking about the U interface, Siemens now

claims to have one, the 2090—at least for the German standard using the 4B3T line code. A two-chip set, the 2090 is available in samples. "This is a two-wire transmission over the public U interface," says Lothar Lerach, manager of communications products at Siemens. "It meets the severe distance requirements of a public network. I think we have met here the most challenging requirements." A modified version of the 2090 for the 2B1Q line code, which will be a single chip, should be available in mid-1989.

Another problem that must be solved before ISDN can be fully implemented, according to some, is Signaling System #7. Signaling Sys-



### Development boards mean business

A sure sign that things are beginning to move with an emerging technology is the appearance of development boards. And with development boards being introduced by such major vendors as AMD, Intel, NEC, Mitel, Motorola, and Siemens, ISDN seems to be gaining considerable momentum. AMD, in fact, has been selling a board for over a year. It contains the 79C30A, is IBM PC-compatible, and sells for less than \$2,000, including software. A new-generation board will include both the 79C30A and the 79C401.

Intel has also introduced a PC-compatible ISDN board. This board provides the customer with the 29C53 for the S interface, the 29C48 for voice support, an 80188 microprocessor for D channel processing, and an 82530 for B channel processing, along with memory and software. "It lets the user convert a regular PC into a full-fledged, ISDN-compatible integrated voice/data workstation," says Weston. The price is about \$5,000 for the IDK 29C53 kit, which includes two Intel ISDN boards and software.

By mid-1988, NEC Electronics will also have two IBM PC-compatible development boards for ISDN. One board will include NEC's Digital Line Interface Controller chip (2-wire connection) along with an LAPD chip; the other board will include the S/T interface chip with the LAPD chip.

Mitel introduced last year an ISDN PC card, the 59500 Express Card. This comes as a single board with software and sells for \$1,500.

Motorola will introduce a PC board along with software in July. The board will have Motorola's S/T interface chip, the MC145474 (a Layer-1-only chip), Motorola's dual data link controller for LAPD and LAPB, the MC145488 (operating both at basic and primary rates), and an MC145000 series codec and filter. The board and software implement ISDN protocols through Layer 3 and will cost around \$1,500.

Various companies, such as Dallas Semiconductor (Dallas, TX), Exar

(Sunnyvale, CA), Mitel, and Crystal are offering chips supporting T1 (1.544 MHz) or CEPT (2.048 MHz) lines. A relatively new offering, the SSI 233 line interface chip, comes from Silicon Systems (Tustin, CA). A corresponding CEPT line interface chip is due out in August. The

primary function of these chips is clock recovery (once the clock is recovered, the data can be extracted). The chips' receive section extracts clock and data and outputs them in standard TTL format. The transmitter section accepts TTL clock and data from the digital circuitry and



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40 percent then means that the clock edge has progressed  $\pm 20$  percent over the sequence of those 15 bits.

"This is a scientific, lab-measured jitter; real-world jitter is never that way, but every piece of test gear in the world is written for sinusoidal jitter, because that's what you can measure in the lab," Bridge says.

Real-world jitter is the subject of debate in the industry right now, he notes. The T1X1 committee of the Exchange Carrier Standards Association (charged with writing North American telecommunication standards) has been studying jitter for a long time. "I don't think they've finished their work, but it may be true that 62411 is overly demanding," Bridge says. But if you want to get any equipment certified for use in the AT&T network, you have to meet 62411. And Crystal's new chip will do that for you. Samples of the CS61574 are now available; full production will commence this summer. The device uses mixed analog/digital CMOS process, dubbed smart analog by Crystal. In quantities of 100, the price is \$22.

### Digitizing voice

On the user end of ISDN, voice needs to be digitized. Various techniques based on PCM have been applied. (The codecs mentioned earlier, such as the 29C48 from Intel and the integrated codec in the 79C30 from AMD, use standard PCM technique.) The latest wrinkle in the world of voice encoding/decoding is adaptive differential PCM (ADPCM), which allows greater compression of data in digital transmission of voice or analog signals. Dallas Semiconductor introduced an ADPCM chip awhile back. Now Sierra Semiconductor (Sunnyvale, CA) has also introduced one.

The chip from Sierra is the SC-11360. "What you get in the ISDN area is 2B+D, which is two 64-kbit/s data paths plus a 16-kbit/s data path," says Bill Nicholson, director of standard products marketing at Sierra. "A codec actually samples a voice-band channel at a rate of 8 kbits/s and converts that to

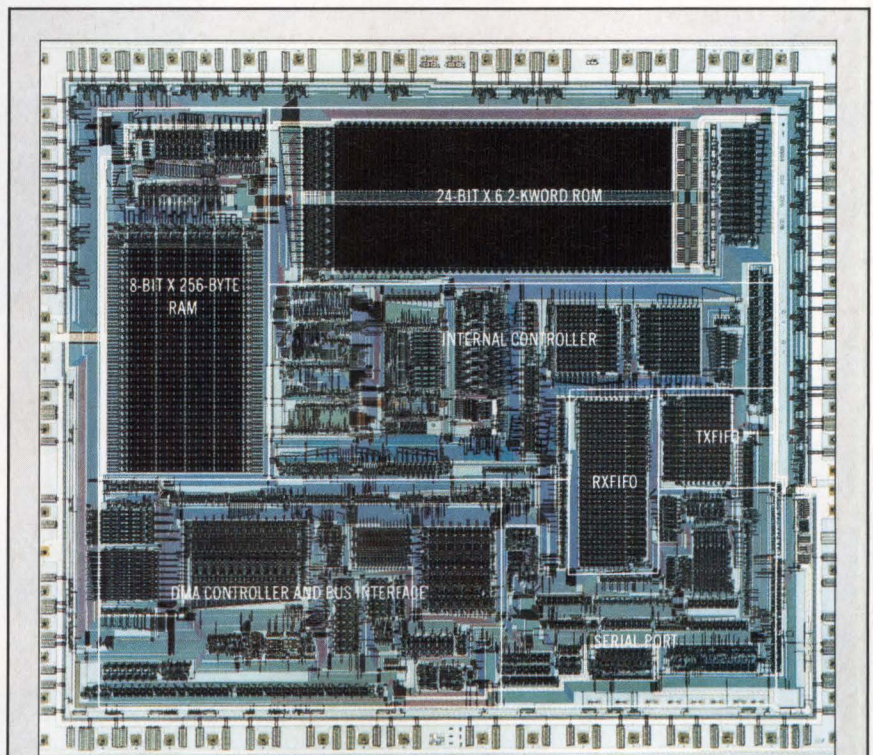
a PCM 8-bit word." That PCM 8-bit word is then interfaced at a serial bit rate of 64 kbits/s. With the compression capability of ADPCM, data can be compressed so that more than one voice channel can be transported on a single 64-kbit/s channel.

"This is used today in point-to-point private line systems," Nicholson says. "Through this ADPCM transcoder [the SC11360], you can double the channel capacity at no additional cost." There are three different modes that can be used, depending on the required quality of voice transmission. In one mode, capacity is doubled, as mentioned; in a second mode, three channels can be transported at 24 kbits/s with some degradation in quality; and in a third mode, four channels can be transmitted at 16 kbits/s with additional degradation in quality.

"When you end up with these two ISDN 64-kbit/s pipes into your

house from the ISDN drop point, it sounds like a lot of capacity, but it's really not," Nicholson says. "The SC11360 could be used to interface to one of the 64-kbit/s 2B channels, doubling its capacity." Increasing the capacity of the standard systems of today has been of considerable concern, and it may well become a concern with ISDN when it's finally installed as standard equipment.

Clearly, ISDN is a long-term project with plenty of remaining problems, such as the need for final bit definition in Signaling System #7 and the lack of the U interface for the North American standard. In addition, in some countries encouragement by government or a push by private enterprise seems to be necessary if the ball is really going to roll. Nevertheless, the pieces are starting to fit together and the outline of the ISDN puzzle is finally beginning to appear. **CD**



The 72307 Signaling System #7 chip from NEC Electronics provides the signaling for call setup and teardown between central offices, which allows users to dial out of their local areas. The company claims that the chip, which fully supports Layer 2, is the first Signaling System #7/Layer 2 chip on the market.



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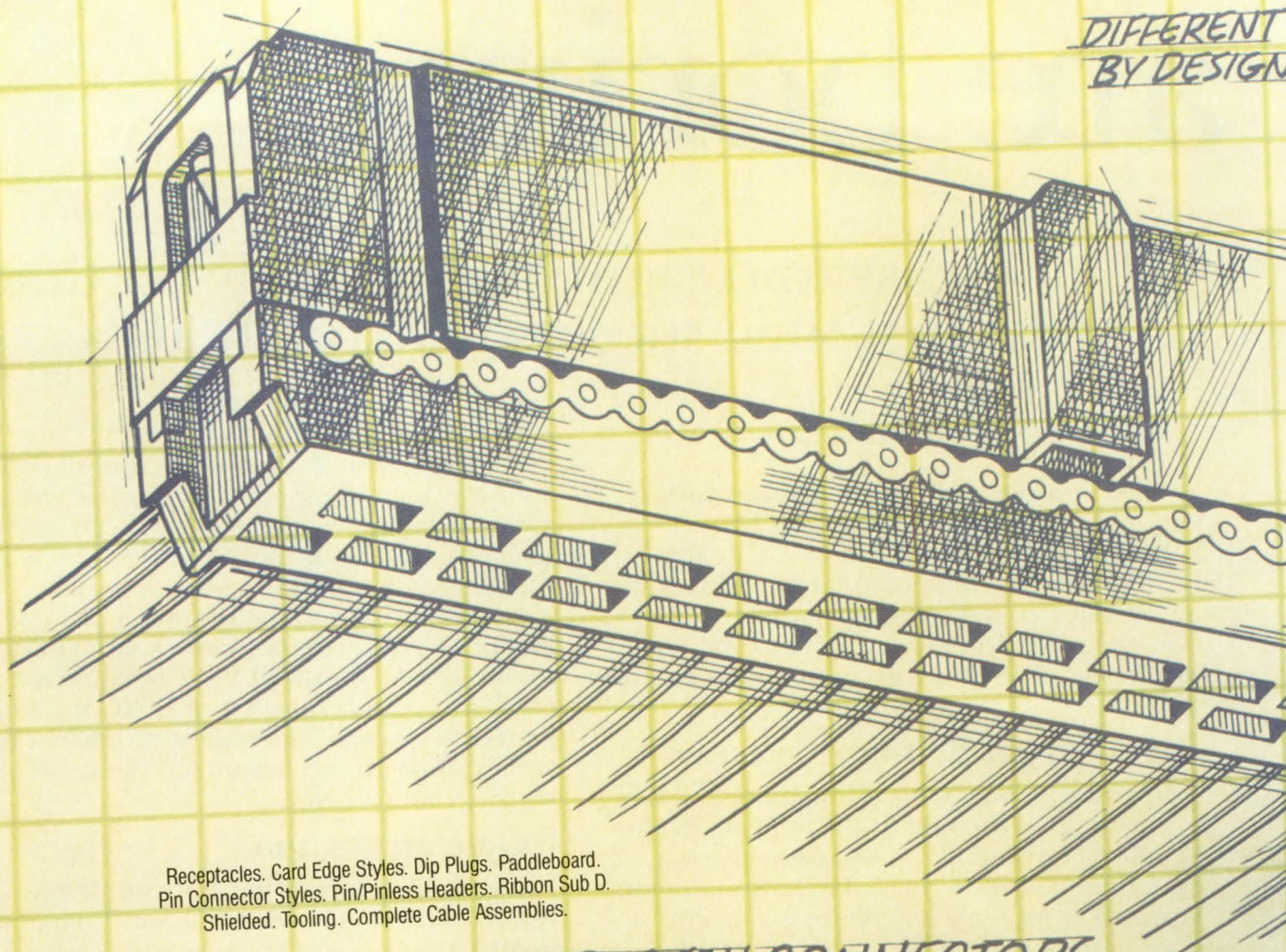
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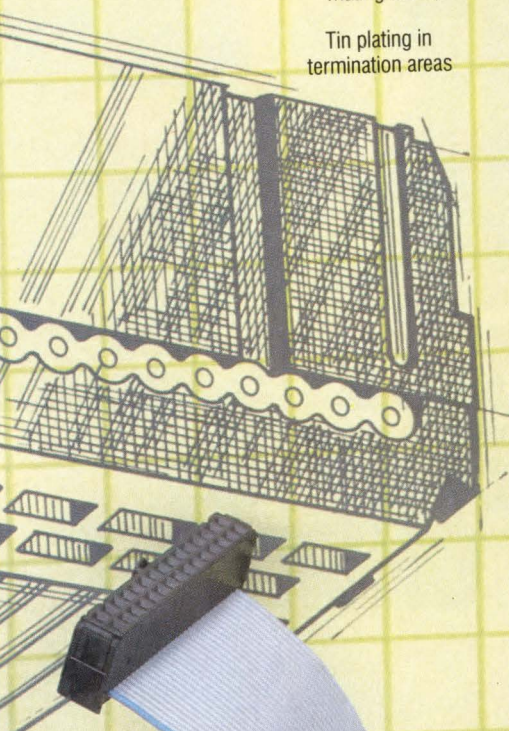
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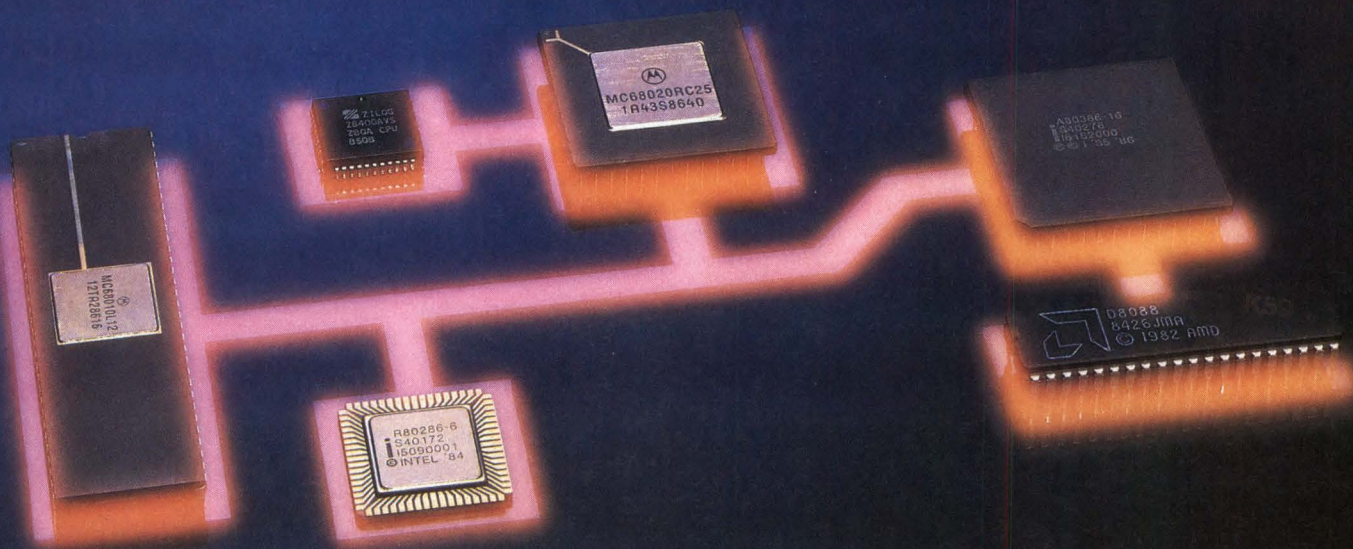
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# RISC architectures take on heavyweight applications

**The concepts that define RISC architecture have left the lab and are working their way into superminis, workstations and embedded computers.**

**Ron Wilson**  
Senior Editor

**T**he question isn't whether you're working on a reduced-instruction-set computer: everyone is. The question is whether you're willing to admit it." Thus one manager describes the pervasiveness of the RISC phenomenon. Born in 1960s supercomputers, nourished in IBM's 801 project and brought to fruition in the halls of Stanford and Berkeley, RISC architecture is moving from research to industrial application with startling speed.

Some of the initial concepts for simple, register-intensive CPU design came from Seymour Cray's work for Control Data Corp in the 1960s. But the modern notion of a RISC architecture emerged from John Cocke's 801 project at IBM in the late 1970s. Cocke's team brought CPU architects and compiler gurus together, asking what would be the best CPU architecture for an optimizing compiler, rather than for an assembly-language programmer.

The IBM group developed a RISC dogma consisting of two key ideas. First, instructions should execute in one machine cycle whenever possible. Second, the machine should have a load/store architecture. In other words, load and store instructions should move data in and out of registers, and computational instructions should only work on data already in the registers. This rule helped keep instructions fast, and it let the optimizing compiler control register allocation.

The new dogma represented a departure from the prevailing attitude, perhaps best represented by DEC's VAX family. The VAX architecture used a highly complex, microcode-driven CPU to execute long, complicated instructions. In a way, the ideal was to find an instruction for every frequently used subroutine in a computer language. But the RISC approach took the complex instructions apart so the optimizing compiler could get at their components. In the process, the architecture eliminated microcode and microse-



quencers in favor of a simple, pipelined, one-instruction-per-cycle CPU design.

The IBM work defined the RISC architecture. But the 801 team had only 1970s ECL technology in which to implement its ideas. And the compiler technology necessary to exploit the RISC concept was hardly known outside IBM. Some technological advances had to occur before the RISC idea could move out of well-funded laboratories.

For one thing, the idea needed an implementation technology that could really exploit the simplicity of the RISC CPU. That technology was rapidly developing in CMOS VLSI. For another thing, RISC concepts waited on the dissemination of compiler technology outside the walls of IBM. As the 1970s came to a close, that technology was appearing in universities and software houses in the United States and Europe.

Finally, RISC technology needed to solve some serious architectural problems: chief among them, memory bandwidth. Simplifying the instruction set had created many opportunities for CPU architects, but it had created an almost insatiable demand for memory speed as well. The faster a RISC CPU went, fetching a new instruction every CPU cycle, the more memory speed it demanded. The 1970s approach of meeting this demand with huge static RAM arrays was an economic impossibility outside the supercomputer market.

The answer to the problem came from another new idea in mainframe architectures: cache memory. If architects could keep the cache hit rate high enough, they could keep a RISC CPU running at nearly full speed, yet they would have to buy only a small SRAM cache to support a large main memory of DRAMs.

With inexpensive VLSI, improving compiler technology and the appearance of affordable caches, all the pieces were in place for a surge in RISC development. That surge started not at IBM, which seemed to lose interest in the RISC concept, but at the two towers of West Coast computer science, the University of California at Berkeley and Stanford University.

**T**he RISC story is next picked up by David Patterson, professor of computer science at UC Berkeley. "In 1980, we began investigating RISC architectures. Our interest was primarily in using the simpler RISC CPUs to exploit VLSI." The Berkeley team sought to demonstrate that the inherently smaller CPUs of RISC systems would make possible very small, and hence very fast and economical, single-chip 32-bit microprocessors.

The Berkeley team was able to exploit the sim-

licity of the RISC CPU to fit an entire processor onto one chip, with space left over. Patterson's people decided to use the extra real estate to solve one of the lingering problems inherent in RISC architectures: task switching time.

Because RISC's load/store architecture is naturally register-intensive, changing tasks can mean swapping a lot of register contents in and out of memory. In a multitasking environment like Unix, all that swapping can hurt performance. So Patterson's group developed the idea of a register set much bigger than any one task could use. The register set would have one area of global registers available to all tasks, and one area for local registers. Within the local-register area, a pointer would indicate the start of a task's local register set, or register window. So when a new task was started, the operating system just had to change the pointer to point at the new task's register window. No swapping would take place until all the local registers were in use.

Patterson's team demonstrated the feasibility of a single-chip, 32-bit RISC microprocessor. The team also demonstrated an important characteristic of such a simple CPU. As Patterson points out, "Because of its simple design, the RISC CPU can track VLSI technology very successfully. As geometries shrink, RISC CPUs get faster. The result is that RISC machines have been getting faster more quickly than CISC machines."

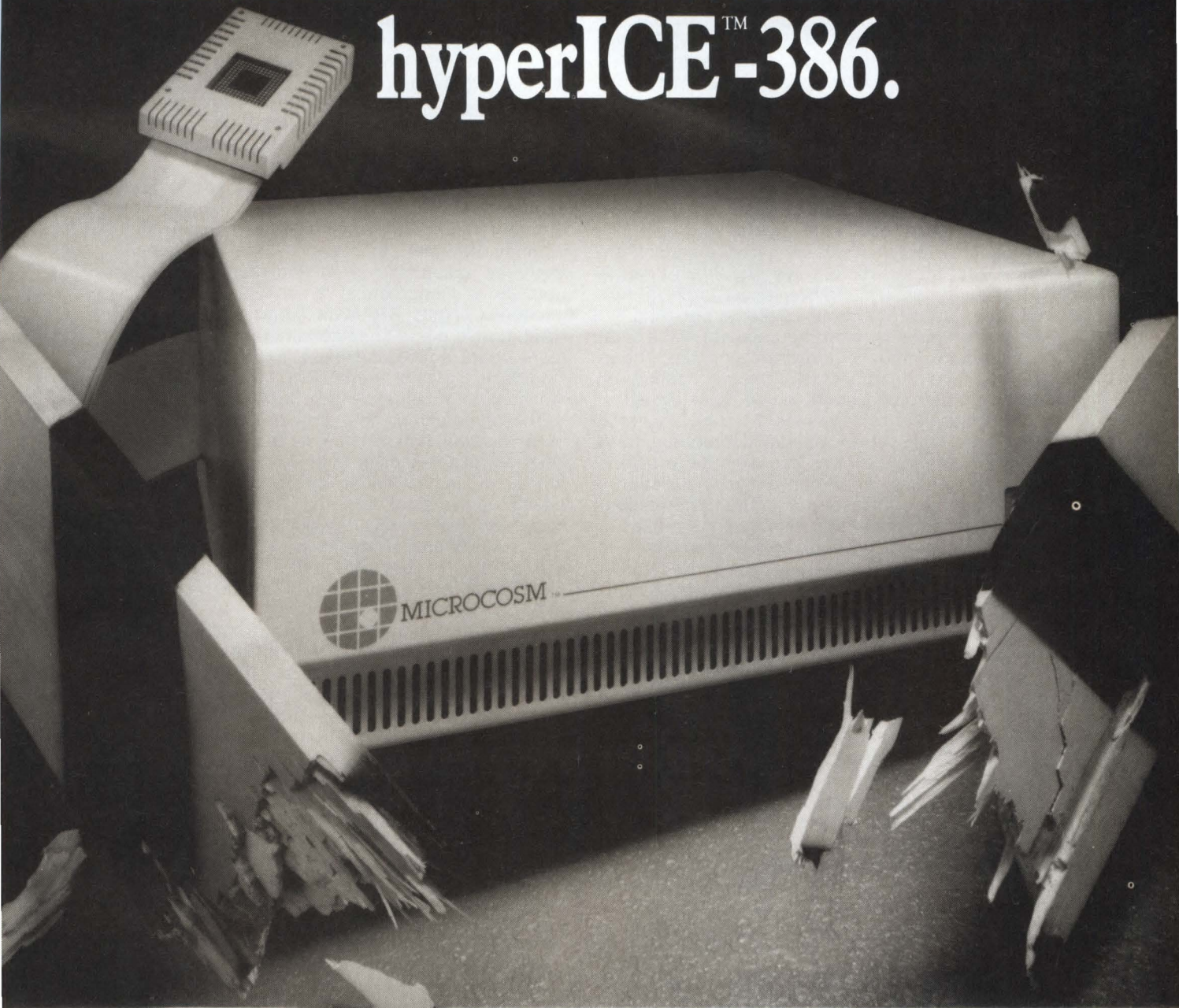
About a year after Patterson's work began at UC Berkeley, a team under John Hennessy, professor of computer science and electrical engineering at Stanford University, began to investigate RISC machines from a slightly different viewpoint. "One of the key ideas for us," Hennessy remembers, "was that you can make trade-offs between what you do in hardware and what you do in software in a RISC machine. Because we had optimizing compiler expertise in the group at Stanford, we did some things differently than they were being done at Berkeley."

One difference involved instructions that required more than one cycle for execution. Examples were branch and load instructions. Earlier RISC machines had introduced the idea of a delayed branch. The idea is that if the branch instruction takes two cycles, the CPU, which fetches a new instruction every cycle, would execute the instruction after the branch instruction before the new program counter could take effect. RISC compilers had been adjusted to compensate for this.

But the earlier machines had not extended the delayed action concept to other multicycle instructions, such as load instructions. They tended to



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CIRCLE NO. 28



## A RISC chip for embedded applications

The 80960KB from Intel (Chandler, AZ) differs from other 32-bit microprocessors based on reduced-instruction-set computer (RISC) technology in that it was designed specifically for embedded applications, where power consumption, integration, cost and ease of use are as important to a product's success as processor performance.

Like other RISC-based machines, the 80960KB has a load/store architecture: all instructions operate on registers except for the load and store instructions, the only instructions that reference memory. It also has a large register set. A program has access to sixteen 32-bit global registers, sixteen 32-bit local registers and four 80-bit floating-point registers. Furthermore, it has simple instruction formats (all instructions are 32 bits long and must be aligned on word boundaries) and a small but useful number of addressing modes. The instruction set is compact, and the most commonly used instructions execute in one clock cycle.

To achieve its performance (7.5 VAX Mips at 20 MHz), the 80960 uses register scoreboarding so that multiple instructions can execute in parallel with load operations. When a load instruction is executed, the processor marks the target register as busy. While the load completes, the processor can continue executing an unrelated series of instructions that don't reference the same register. By using two arithmetic logic units, the 80960KB can calculate the effective address of a branch instruction in the instruction decoder while the integer execution unit completes another instruction.

Unlike other RISC machines, the 80960KB has a control-oriented instruction set. It includes a comprehensive set of Boolean, bit and bit-field instructions, which simplify the task of programming embedded applications. And the 80960KB is highly integrated, including an on-chip interrupt controller, an integrated floating-point unit, a 512-byte instruction cache and a register cache that can hold up to four sets of local registers.

Some RISC purists might object to the fact that the 80960KB has an on-chip microcode ROM. Although the 80960KB doesn't use microcode for its basic instruction set, it does use microcode for several functions rarely found in RISC machines, which make the 80960KB easier to use in embedded applications. For these functions, a hard-logic implementation wouldn't have been cost-effective because it would have made the chip impractically large and difficult to manufacture.

One example where using microcode is more cost-effective is in floating-point operations. Other examples abound: software tracing, support for in-circuit emulation, interrupt handling and automatic procedure calls. Most users would agree that these functions greatly enhance the usability of the processor, and including them doesn't hurt the processor's overall performance.

Some RISC theorists might argue that these functions would be faster if they were implemented in software, but that isn't the case. By giv-

ing these functions access to private hardware resources on-chip, such as additional registers and special microinstructions, they execute much faster than they would if they had to be implemented in software. The same resources couldn't be made available to software because they're highly implementation-dependent and making them visible to the programmer would cause compatibility problems between generations.

Many of the new RISC microprocessors require extremely fast memory systems—usually in the form of large static RAM caches—to deliver their promise of higher performance. This requirement might be acceptable in an engineering workstation, but it's impractical in most embedded applications. While SRAM is faster than dynamic RAM, it also costs considerably more, consumes more board space and uses much more power. One design goal of the 80960KB was high performance with only inexpensive DRAM.

The key to achieving that goal is the 80960KB's burst bus, which can read or write up to four words (16 bytes) in one access. In the first cycle of a transfer, the processor issues an address, followed by one to four words of data, and ends with a recovery cycle. In other words, the 80960KB can transfer four words in only six cycles, while even machines with a two-cycle transfer require at least eight cycles. The 80960KB has a maximum bus bandwidth of 53.3 Mbytes/s at 20 MHz.

A burst bus is an excellent fit for static-column and nibble mode DRAM. In the first access, there's a delay to charge the row address (RAS precharge time), but once that's done, the next three accesses can proceed quickly. Static column mode allows fast access to the bits located in the selected row of DRAM simply by toggling the column address strobe (CAS) signal. In nibble mode, a multiplexed address is applied to the DRAM; then, as in static-column mode, up to 4 bits of data can be quickly transferred by successively toggling the CAS. By completing the RAS precharge during the burst bus's address and recovery cycles, it's possible to get performance that rivals SRAM performance without even using memory interleaving.

With its burst bus, register scoreboarding and extensive use of internal caching, the 80960KB is relatively insensitive to memory wait states. In fact, the processor loses only 7 percent of its performance for each wait state, in contrast to a performance loss of 35 percent or more for other RISC-based machines. This low percentage gives designers of embedded applications a tremendous advantage in that they can use inexpensive DRAM instead of large SRAM caches. They can achieve high performance yet stay within their cost, space and power consumption constraints.

—Mike McGowan  
Product Manager for the 80960K series  
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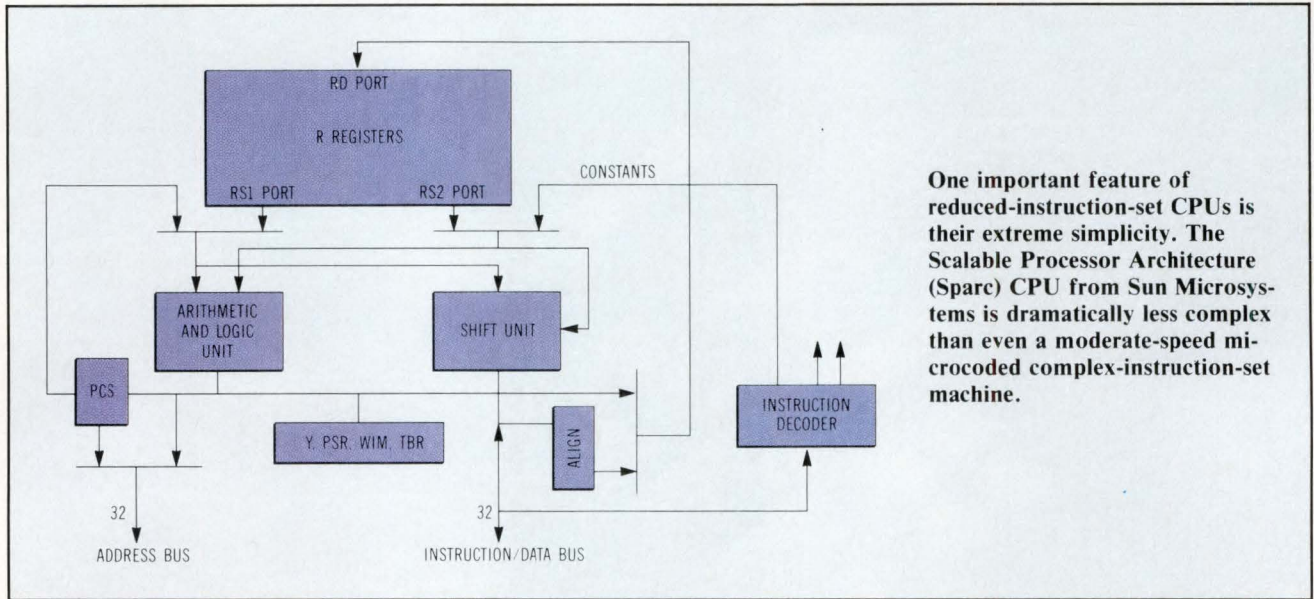
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CIRCLE NO. 29





One important feature of reduced-instruction-set CPUs is their extreme simplicity. The Scalable Processor Architecture (Sparc) CPU from Sun Microsystems is dramatically less complex than even a moderate-speed microcoded complex-instruction-set machine.

freeze the entire pipeline while a load instruction was executing, just to make sure that the data actually got into the register before some other instruction tried to use it.

Hennessy's team recognized that with a clever compiler, freezing the pipeline wasn't necessary. The compiler simply had to make sure that the instruction directly after the load didn't try to use the new data. And if this were the responsibility of the compiler, rather than hardware interlocks in the CPU, useful work could be done in parallel with the load instruction. Not only would the CPU be simpler, but it could do more in a given number of cycles. The Stanford group referred to this architecture as a Microprocessor without Interlocked Pipeline Stages, or, reaching a bit for a pun, MIPS.

Hennessy's team also relied on its compiler expertise to solve the procedure-switching problem. "The Berkeley group found that procedure calls were very expensive, and responded by implementing a large register set," explains Hennessy. "We chose instead to have a smaller register set and get the compiler to minimize the amount of loading and storing that went on during calls. We've found that there's little difference in overall performance, but the smaller register set produces a slightly smaller die, which can be important for people working in technologies like gallium arsenide."

The two university teams took a concept from mainframe architects, applied it to VLSI processors and refined it for use with the latest compiler technology. In the process, the RISC CPU became a compact, manufacturable and understood one-chip microprocessor capable of several Mips 32-bit computation. What had been an interesting idea for

architects was suddenly a potential competitive advantage for microprocessor-dependent 32-bit workstation vendors.

Certainly problems remained. While the Berkeley and Stanford teams concentrated on an integer CPU, little was done to address some of the other needs of high-performance workstations, such as memory management and floating point. But the university work triggered a race to produce a RISC workstation microprocessor.

**W**orkstation vendors quickly recognized the implications of the RISC work at Berkeley and Stanford. If a simple microprocessor could run at 10 Mips, 32-bit workstations could challenge the fastest superminicomputers on compute-intensive applications. Three microprocessor design efforts in industry—one following the Berkeley ideas, one growing out of the Stanford research and one adding RISC ideas to its own unique concepts—have pursued the goal of the 10-Mips workstation.

Each vendor has had to fill in some blanks to translate the university designs into workstation products. Floating-point hardware, memory management and cache designs have proved essential to a successful 32-bit workstation, and none of these elements was specifically addressed in either the Berkeley or the Stanford work. Not surprisingly, each of the early RISC microprocessor vendors has taken a different approach to filling these gaps.

Sun Microsystems (Mountain View, CA) chose to follow Patterson's work at Berkeley in at least two important respects. Most obviously, Sun adopted Patterson's register window approach to manage procedure call delays. But perhaps more

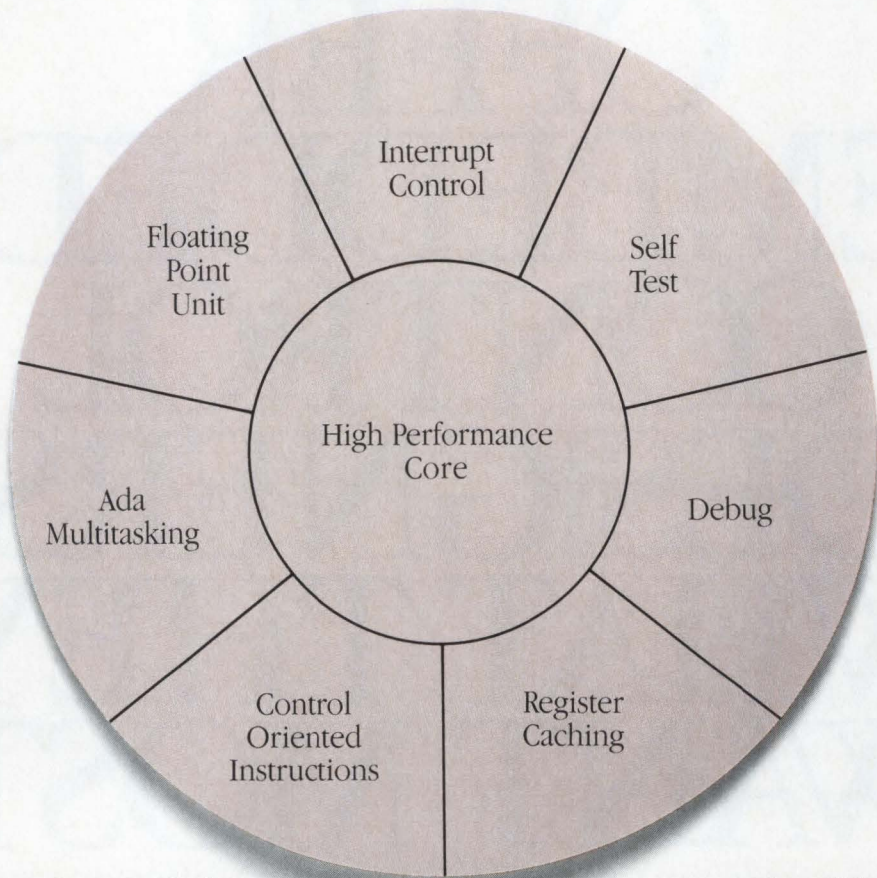
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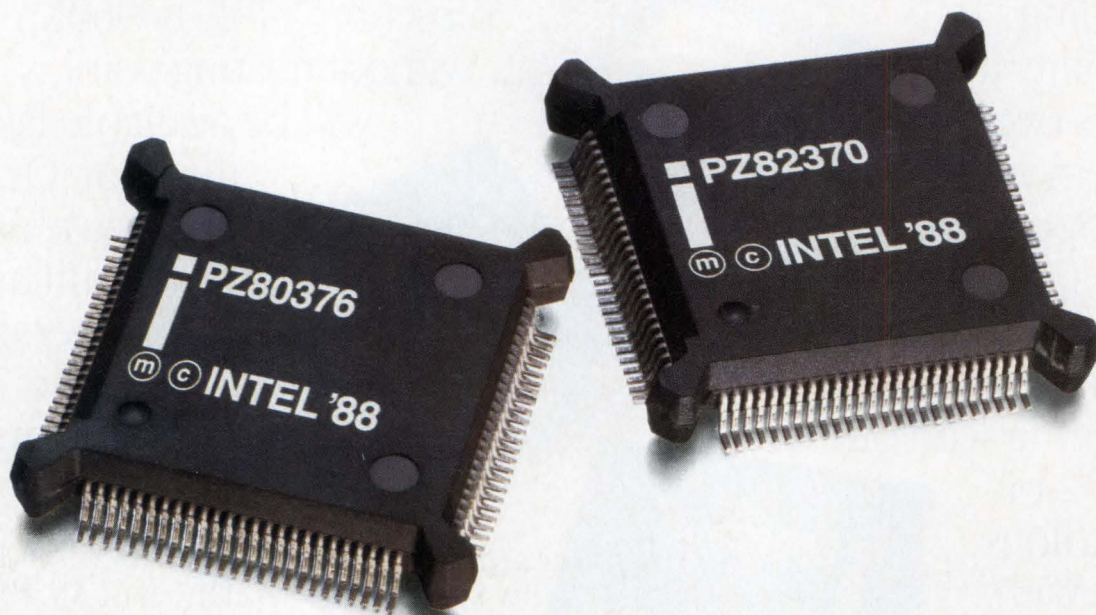
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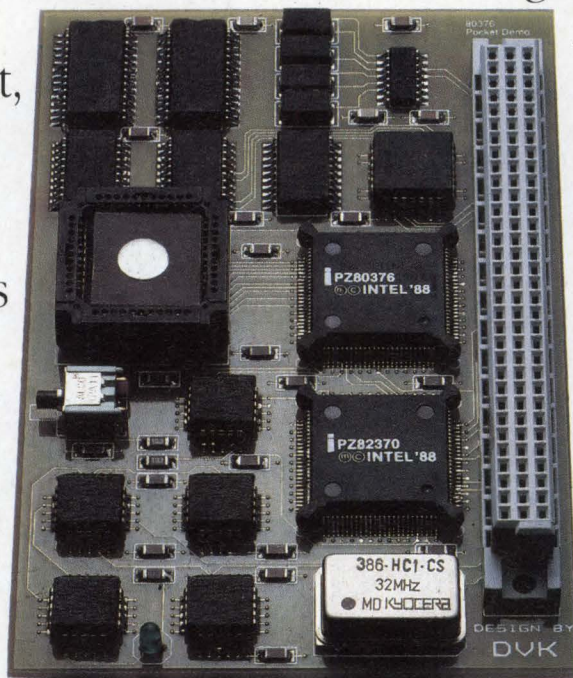
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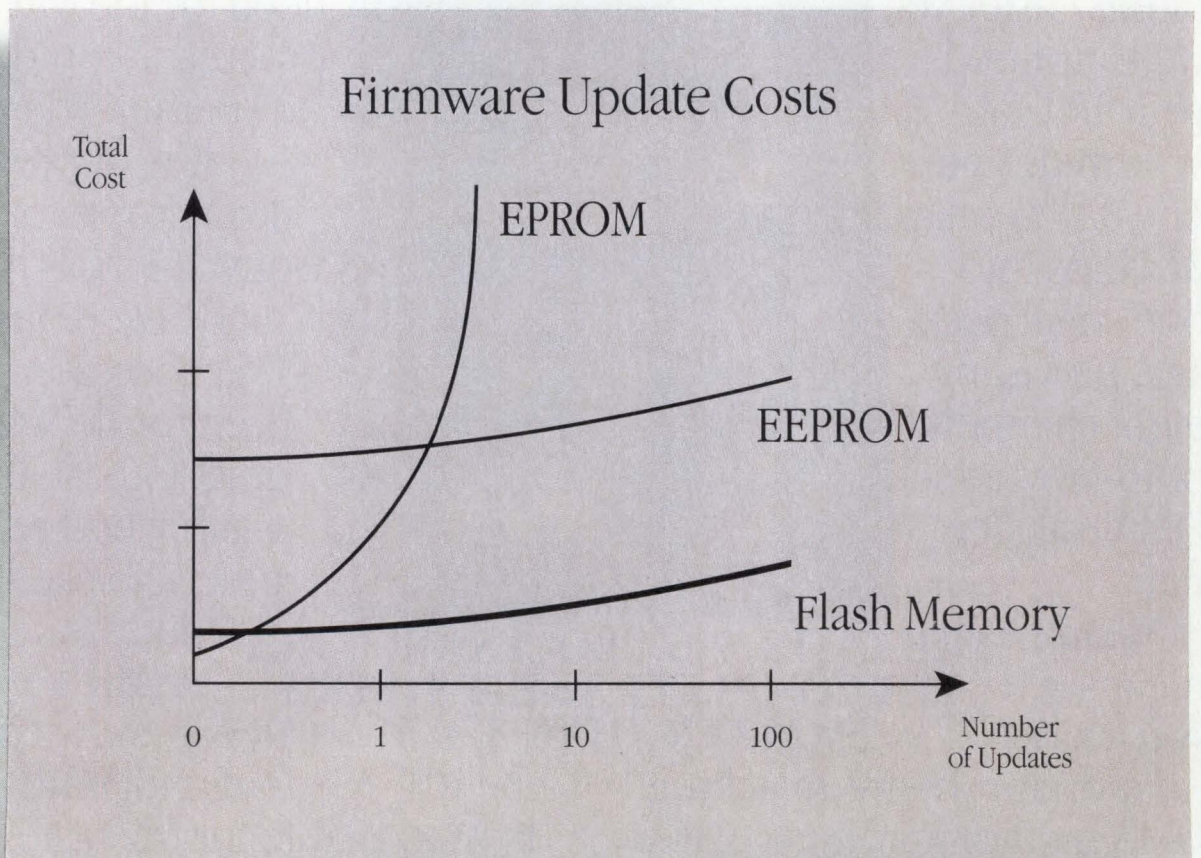
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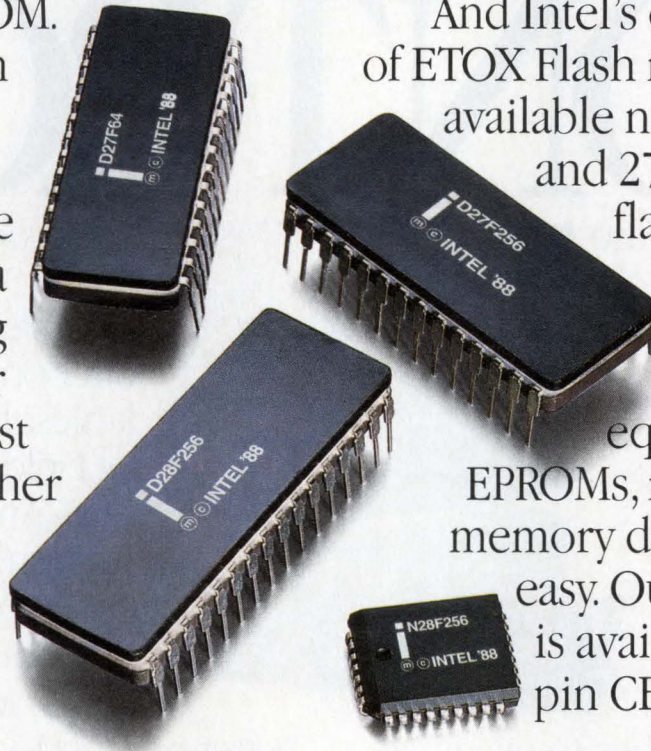
The ETOX process breaks through the technology barrier between low-density, high-cost EEPROM and dense, low-cost EPROMs. It combines the electrical erase capability of an EEPROM with the single transistor cell of EPROM.

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Reprogramming Failure Rate		
Technology	100 Cycles	10,000 Cycles
Flash Memory	<.01%	.1%
EPROM	2%	—
EEPROM	—	5%

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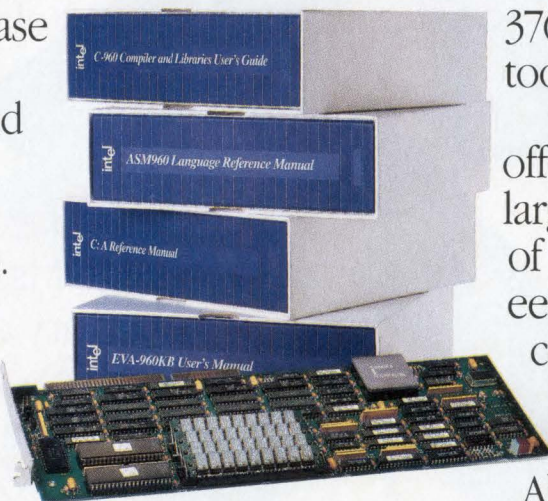
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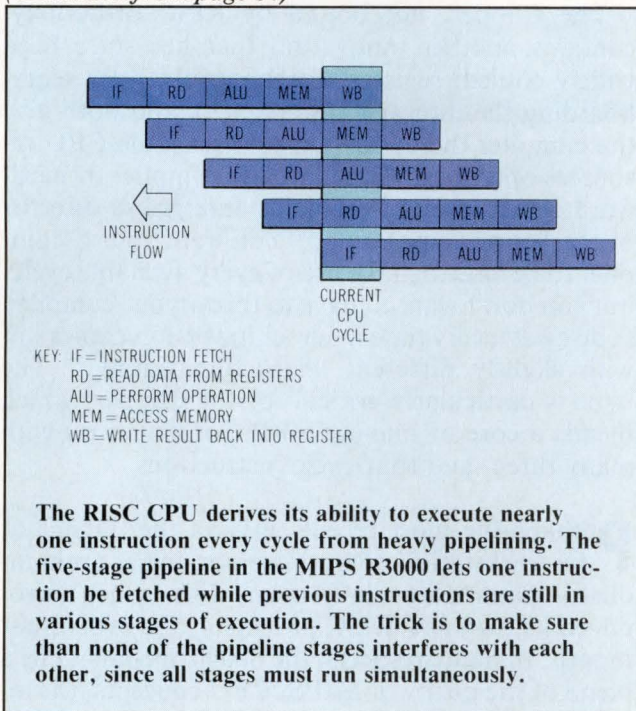
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**CIRCLE NO. 34**



(continued from page 64)



important, Sun took to heart the Berkeley team's notion that a simple CPU design could easily be moved from one implementation to another, turning each new technology into an increase in speed. So Sun's RISC microprocessor was designed from the outset to be portable between implementation technologies: hence, the Scalable Processor Architecture, or Sparc.

Simplicity for the Sun team meant keeping the component count on the CPU low enough that the CPU could be implemented on a single chip in a whole range of technologies, from CMOS gate arrays to handcrafted ECL. This restriction forced Sun to partition the floating point, memory management and cache hardware off-chip.

The result is generally a less compact design than can be achieved with other RISC chips. But for many system designers, the scalability—and hence the wide choice of vendors and cost/performance points developing for Sparc—clearly outweighs chip count as a consideration. "Customers are looking at Sparc as an instruction-set definition, with many implementations available," points out Susan Mason, marketing development manager for Sparc supplier Fujitsu Microelectronics (San Jose, CA). "We'll have customers in production this year with our 16.6-MHz gate-array implementation of the chip. We have announced a 25-MHz standard-cell implementation and expect to make another significant increase in speed by going back and handcrafting some of the cells."

Parallel computer vendor Arix (San Jose, CA)

also cites vendor flexibility as a key issue in its selection of Sparc. "RISC isn't a religious issue for us, just a means of providing performance and portability," points out Bruce Sawyer, Arix director of RISC development. "Sparc offered an open architecture, so we could benefit from competition among the chip vendors but stay with one instruction set and binary interface standard."

While the Sparc instruction-set architecture seems to be developing into a de facto standard, there has been confusion about floating-point, memory management and cache support. Since these items aren't included in the chip definition, implementers have taken something of an every-man-for-himself approach. Sun has developed its own solutions, including a third-party floating-point processor, the 9947 from Texas Instruments (Dallas, TX). Fujitsu plans its own set of support chips. "We intend to find a customer with whom we can develop a cache controller for productization," says Mason. "We will also look at floating-point units, and will take on a memory manager as soon as we see AT&T's specification for Unix memory management."

While Sun exploited Patterson's ideas, a company spun off from Stanford to turn that team's efforts into products. MIPS Computer Systems (Sunnyvale, CA) absorbed Hennessy's philosophy of extremely fast hardware and heavy dependence on optimizing compiler technology. The MIPS processor chip retained the Stanford design's delayed loads and branches, and focused on a single high-speed implementation rather than scalability.

The result is a CPU that, in its most recently announced incarnation, the R3000, is claimed to yield 20 VAX Mips: that is, 20 times the integer performance of a VAX-11/780. This compares to claims for the initial Fujitsu Sparc implementation ranging from 6 to 10 Mips.

The R3000 CPU contains a four-stage noninterlocked execution pipeline, a Unix-capable memory manager and cache control circuitry (but not the cache RAMs themselves). Like the Sparc, the MIPS chip relies on an external floating-point coprocessor, but there's a major philosophical difference between Sun and MIPS in the way the external FPU is designed. While Sun chose to interface a third-party FPU to its chip, MIPS designed its own closely coupled coprocessor.

The MIPS designers felt strongly that the key to performance was the ability of the compiler to manage the CPU pipeline, during floating-point as well as integer operations. "It's absolutely essential that there be a seamless coupling between the coproces-



sor and the CPU,” argues Tom Riordan, MIPS director of CMOS systems. “The floating-point unit must understand the state of the integer unit’s pipeline at all times.”

These considerations led the MIPS team to develop the R3010 coprocessor for use with the R3000. The company feels that its performance results—7 single-precision Linpack MFlops—more than justify its belief in seamless coprocessing to maintain the integrity of the pipeline.

The Berkeley and Stanford heritages are clearly evident in Sun’s and MIPS’ products. But a third vendor, Fairchild Semiconductor, also benefitted from the university work. The Fairchild team did not attempt to reimplement either research chip. Instead, the team absorbed the RISC concepts into its own somewhat CISC-like architecture and added some innovations that would heavily influence later RISC designs.

The Fairchild Clipper, now available from Intergraph Advanced Processor Division (Palo Alto, CA), was the first microprocessor design to recognize the growing memory bandwidth problem RISC chips were causing. As CPU speeds moved from 10 to 16 to 25 MHz, it became impossible to service the CPU bus—not only from a conventional DRAM main memory, but even from many cache memories. The Clipper’s solution was to separate the relentless demand of instruction fetches from load/store activity by providing separate instruction and data buses.

The Clipper supports the dual buses with a pair of integrated cache and memory-management chips. Combining the two functions provides considerable efficiencies in the way caching and address translation can be overlapped and frees considerable space on the CPU die. The Clipper designers use this space for an FPU that has been growing in sophistication and speed through succeeding generations.

The Clipper, not bound by RISC orthodoxy, contains another innovation that has since been widely copied: register scoreboarding. “By scoreboarding the integer registers, we could both give the compiler the opportunity to schedule CPU resources optimally and relieve the compiler of hardware dependencies,” explains Intergraph director of marketing Gary Baum. “You want your C compiler to be able to make use of every available cycle, but you don’t want to have to throw your compiled code away every time a new chip version comes out with slightly different instruction timing.” The issue is particularly critical for the Clipper, which blends a core of one-cycle RISC instructions with many three- and four-cycle instructions.

Perhaps the most recent entry in the pursuit of the workstation microprocessor comes from industry giant Motorola (Austin, TX), which introduced its own new RISC processor, the 88000, last month. In many respects, the 88000 appears to be a blend of the purity of MIPS’ CPU concepts, the innovations of Clipper’s bus architecture, partitioning and scoreboarding, and the strength of Motorola’s own superb CMOS fabrication technology.

The 88000 CPU sticks to the dogma of simple, one-cycle, fixed-length instructions and a load/store architecture. Like Clipper, the 88000 is a dual-bus, three-chip layout with register scoreboarding. But the 88000 FPU is unlike that in either the MIPS or Clipper designs and may well point to the future direction of RISC architectures.

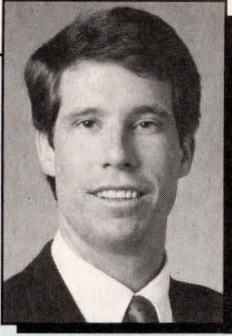
Inside the CPU chip, the 88000 architecture isn’t so much a pipeline as a collection of buses serving a cluster of execution units. A load/store unit handles memory reference instructions. An integer execution unit handles integer and logical operations, and a floating-point execution unit handles IEEE floating point. All the execution units work

Machine	Clock MHz	Cycles/Instruction	Native Mips
MIPS R3000	25	1.25	20
MIPS R2000	16.7	1.4	12
AMD 29000	25	2.0	12.5
Sparc	16.7	2.1	8
IBM RT PC	6	3.0	2
Clipper	33	6.6	5
80386	20	6.0	3.5
68020	16	7.0	2.3
VAX 8550	22.2	7+	3.0
VAX-11/780	5	10	0.5

Source: MIPS Computer

**RISC CPUs are coming consistently closer to the goal of one cycle per instruction averaged over an entire program. Progress is made both by clever definition of instructions and by hardware speedups for such tough nuts as floating-point multiplies and divides. Since the average number of cycles per instruction so dramatically affects speed, it’s a disputed measure.**





*Jim Hughes  
Manager, Product Marketing  
Pyramid Technology*

## **Expandable configurations let manufacturers fine tune for performance**

**R**educed-instruction-set computers are now firmly accepted in most segments of the computer industry. RISC technology is being applied in two key user applications: single-user systems and commercial workstations; and multiuser environments. Commercial users, such as those in financial services, telecommunications or government applications, can choose from a wide variety of RISC products, ranging from the microprocessor-based IBM RT PC and chip sets from companies such as MIPS Computer Systems (Sunnyvale, CA), to supermini-based offerings such as the single-processor Spectrum Series from Hewlett-Packard (Palo Alto, CA) and the symmetric multiprocessor Series 9000 product line from Pyramid Technology (Mountain View, CA). As RISC gains popularity, users are demanding performance improvements beyond raw single-CPU power. The needs of the commercial environment require expandable systems that provide a balanced architecture to solve large general-purpose application demands.

To meet users' needs for system size, application complexity and so forth, computer manufacturers must provide an easily expandable capacity and an easy-to-implement, predefined upgrade path, including all areas of system performance: I/O capacity and throughput, memory capacity and access, and CPU performance. Feedback from the installed customer base in data base applications, on-line transaction processing and communications can provide the basis from which to incorporate improvements in bus utilization, caching algorithms, operating system performance and basic system design required to enhance system throughput.

Manufacturers of RISC-based systems that adhere to open-system standards while still retaining a proprietary-based system architecture have an advantage because they can fine tune their system design implementation to increase balanced performance. Balanced system performance optimizes system throughput among CPU, memory and I/O accesses. The key is having the ability to enhance overall system performance beyond what can be achieved if only raw CPU power is increased. Indeed, users who consider only the CPU Mips specification when outlining system requirements are making a mistake because system bottlenecks can be caused by one or more of the other functional areas of the system—specifically, I/O

channels or memory access.

With a proprietary-based architecture, a manufacturer isn't dependent on the design trade-offs of a third-party supplier, so enhancements can be incorporated into the system implementation without changing the architectural definition of the product. Performance enhancements beyond the CPU architecture for a RISC-based application include implementing such things as symmetric multiprocessing; high-speed system buses; large data and instruction caches; fast, high-capacity block and byte multiplexer channels; a diagnostic/service processor; and a large, high-speed memory subsystem. These system enhancements need to be provided in a modularly expandable package so that the system configuration meets the demands of the application environment while retaining the best price/performance profile. The key for the manufacturer is understanding the system requirements from a total application environment, so that the system can be fine tuned to meet the user's needs. Examples include the incorporation of special instructions to improve operating system performance with data base products and I/O fine tuning for applications with long-running processes and/or large working sets such as software development environments and communication networks.

In evaluating application requirements, today's users must look beyond raw CPU performance to overall system throughput. Most traditional benchmarks measure single-threaded performance, in which transactions are handled serially. This measurement ignores potential I/O bottlenecks in a multithreaded environment, in which more than one transaction is active at a time. For example, the Dhrystone benchmark is a single-threaded benchmark designed to measure raw CPU power and compiler efficiency. This is contrasted with the AIM Suite 3 benchmark, which is multi-threaded and measures the ability of a system to provide CPU, I/O and memory to many processes (or users) simultaneously. Neither of these is a completely accurate predictor of performance, but a benchmark such as AIM 3 evaluates the needs of today's computing environments much better than the Dhrystone benchmark. Benchmarks must simulate intended use and evaluate CPU, I/O and memory access as a complete, integrated system so that the prospective customer can make a more intelligent purchasing decision.



over the same two source buses and single destination bus to a common, scoreboardd register file.

This type of organization allows for concurrency between the execution units. "The scoreboarding hardware in the register file takes care of data dependencies," explains Roger Ross, manager of advanced microprocessor operations at Motorola, "so the compiler is free to start concurrent instructions on the available execution units without having to predict when each operation will finish."

The most important characteristic of the 88000, beyond Motorola's ability to attract software to the architecture through sheer marketing muscle, may be the system's ability to incorporate new, specialized execution units. "We can put about eight execution units on the current internal buses," comments Ross. "As we implement the chip in finer geometries, that starts to make room for some really interesting special-purpose things, like vector processors and graphics engines."

**S**un, MIPS, Intergraph and Motorola all have taken different architectural approaches to a common goal: a fast Unix workstation. But in focusing on their various schemes to implement memory management, floating point and efficient caches, these four companies have been pulled further and further away from the needs of another large microcomputer market: embedded computing. And while the workstation companies were holding the attention of these early entrants, other powerful CPU vendors began to think of RISC not in terms of Unix, but as an embedded computing breakthrough.

Vendors of embedded computing processors are well aware of the RISC revolution, but they also know that they must meet a set of needs quite different from those of the workstation vendors. Embedded processors generally must be able to respond to events very quickly: in microseconds rather than the milliseconds typical of workstation response times. In addition, embedded processors usually must be very compact and must make code debugging easy, even during real-time operation.

In the past, these needs have been met by microcontrollers at the low end and bit-slice designs at the high end. But a multi-Mips RISC microcontroller can challenge the bit-slice dominance in many applications. Rick Rasmussen, microprocessor marketing manager at LSI Logic (Milpitas, CA), says, "We've seen the demand for 32-bit embedded controllers build up first in military applications, where tasks keep getting bigger. Now designers need something more powerful than the 1750. It's too early to say what will happen next, but it looks like

the demand will spread to commercial avionics, then to systems like laser printers."

Jim Ting, product marketing manager for the VRTX real-time operating system at Ready Systems (Palo Alto, CA) agrees that RISC speed can attract embedded system designers. "We see customers looking for a big performance increase, to let them take on new tasks. But designers are very careful about system cost in embedded systems. With RISC CPUs, people are particularly skeptical about the cost of the memory systems."

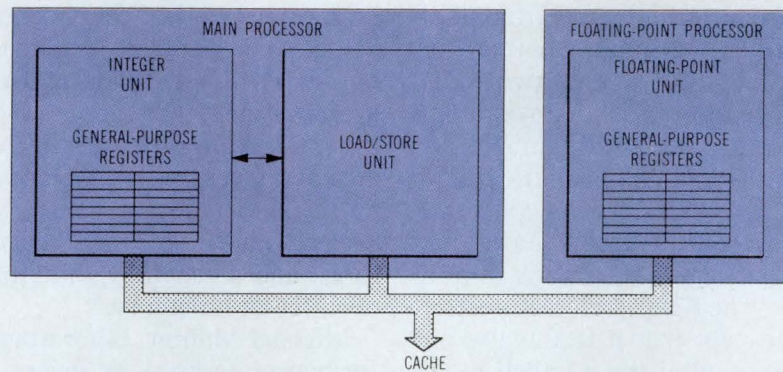
One of the first vendors to respond to this finicky appetite for low-cost power was Advanced Micro Devices (Sunnyvale, CA). While AMD's Am29000 CPU can be outfitted as a workstation microprocessor, it has some features particularly appealing to embedded computer designers.

AMD constructed a very fast integer CPU, currently running at a sustained 17 Mips at 25 MHz. (A 30-MHz part is being sampled.) To improve response time, AMD innovated a register architecture similar to the Berkeley register window approach. The 29000 CPU has a total of 192 registers, of which 64 are always-available global registers. The 128 local registers may be addressed either in bank-switched groups of 16, or relative to a register stack pointer. Either method lets most context switches occur without swapping registers into memory.

The company apportioned space on its CPU chip with embedded systems in mind, too. John East, senior vice-president for AMD's Logic Group, explains, "The things you put on the CPU chip should be the things most embedded designs can use. So we put a branch-target cache and a memory manager on-chip. We kept the floating-point unit and data cache off-chip and optional." The branch target cache is a specialized instruction cache that prevents the CPU's four-stage pipeline from emptying during repeated branch instructions.

The 29000 has also tried to minimize the RISC CPU's hunger for memory bandwidth. Recognizing that many embedded designs had room for neither elaborate caches nor large SRAM memory arrays, the chip's designers have done their best to keep the chip operating at full speed with simple DRAMs or video RAMs. Their measures include a three-bus architecture in which separate instruction and data paths share a common set of address lines. The bus can operate in a simple address-then-data mode, or in a pipelined mode where address is provided on one cycle and data on the next. Also, the bus has a burst mode in which one address triggers a burst of data cycles. The company claims that the CPU can reach peak transfer rates of 100 Mbytes/s in burst mode.





Instructions	Sequential	Parallel*
FMPY	4	1
LOAD	2	1
ADD	1	1
STORE	2	1
INC	1	1
<b>Total Number of Clocks</b>	10	5

\*Assumes no register conflicts

Multiple execution units are an increasingly common feature of RISC CPUs. In the Ridge 5100 multicyle integer instructions, load/store operations and floating-point calculations can proceed in parallel once they have started.

The 80960 microcontroller recently introduced by Intel (Santa Clara, CA) also shows specialization for embedded control applications, but through a different set of choices. Like the Motorola 88000, the Intel CPU is actually a cluster of execution units served by a common fetch unit, a register file and a silicon bus. This permits the company to offer versions of the CPU with and without floating point or memory management, and to vary the amount of on-chip cache.

Intel chose to implement an instruction cache on-chip in the 80960 and to provide a register banking scheme similar to that of the 29000. The 80960 provides a mix of global and local registers. Rather than the local registers being in fixed banks, as in the 29000, they're held in a register cache, from which they may be used or swapped as needed.

Another adaptation of the Intel chip for embedded control is the provision of some complex instructions, particularly for floating point. Instructions for such things as transcendental functions, which the Intel designers felt were helpful to some embedded system designs, are decoded into RISC instructions within the CPU chip.

In this regard, the 80960 team has started with a RISC core and then left the RISC philosophy behind to pursue its own ideas about embedded computing. Other recent CPU designs have started with the same set of concepts but wandered even further afield from the original notion.

One example is a MIL-1750-compliant CPU from United Technologies Microelectronics Center (Colorado Springs, CO). According to UTMC applications engineer Lance Flake, "Another division needed a 1750 engine capable of meeting peak performance requirements beyond the current range of 1750 speed. Our design team decided to meet the requirements with a RISC processor that could emulate the 1750 instruction set."

The resulting design is a RISC machine with added hardware to map some of the more arcane MIL-1750 features onto the simple instruction and register layout of the reduced architecture. Perhaps the largest hardware item outside the RISC core is a universal asynchronous receiver-transmitter used to implement the 1750 console mode.

UTMC claims 6 RISC Mips for the machine, and Flake says, "We were able to emulate the majority of the 1750 instructions at about three RISC instructions per 1750 instruction. When we run the standard instruction mixes, we show about 600 kips running 1750 code."

While UTMC targeted the 1750 architecture for the company's RISC-based design, Harris Semiconductor (Melbourne, FL) has used RISC concepts in an entirely different approach to embedded computing: to create a highly integrated Forth-executing microcontroller. The RTX 2000 combines the notions of one-cycle execution and a simple instruction set with a stack-based architecture



intended to directly execute Forth code.

The new Harris processor integrates its small CPU with a 16- $\times$ 16-bit multiplier, an interrupt controller, three counter/timers and two stack memory structures. The chip uses a conventional 16-bit bus to access memory and an additional high-speed bus specifically to attach application-specific I/O devices to the processor. George Nicol, president of Silicon Composers (Palo Alto, CA) has had some experience now packaging the Harris chips in board-level products. "The RISC architecture itself isn't really the issue, except that it lets us use our compiler technology to exploit the parallelisms of the CPU," he observes. "On the sieve benchmark, for instance, our compiler is able to combine the simple instructions until we're running 16 Mips average with only a 10-MHz clock."

While some vendors are borrowing RISC concepts in the design of their CPUs, it's becoming increasingly possible for system designers to borrow the RISC CPU itself for inclusion in their ASIC designs. Two major ASIC vendors, VLSI Technology (San Jose, CA) and LSI Logic (Milpitas, CA) have announced RISC CPU cores. Both companies will offer the products as off-the-shelf processor chips and as elements in their ASIC design libraries.

While VLSI Technology's part is a proprietary design, LSI Logic has chosen to go after commercially available CPUs from MIPS and Sun. LSI's Rasmussen explains one advantage of the CPU core approach to system design. "As speeds increase, it takes closer and closer integration of the CPU, cache and coprocessors to keep the system operating. Eventually, RISC architectures will move from collections of separate chips to on-chip integration of cache, memory management and coprocessor control functions. We will be able to provide a range of these functions from our cell library."

**T**he fundamental concepts of RISC computing, perhaps a decade in formation, have been quickly molded to the needs of workstation and embedded computing markets. To see the likely future of these microprocessor-based RISC products, we can turn to the vendors who have the longest history with the architecture: minicomputer vendors. Companies like Ridge Computers (Santa Clara, CA) and Pyramid Technology (Mountain View, CA) brought board-level RISC processors onto the market as early as 1983 and have been evolving their architectures ever since, free from the constraints of silicon real estate.

One evident trend in these larger machines is the elaboration of memory and I/O architectures. "We're coming to a point in time when the perfor-

mance of a particular execution unit will be only an important detail of the system design," claims H. William Gimple, vice-president of systems technology at Pyramid. "The real question will be aggregate system throughput. We worked out most of the instruction set issues in the '70s, and now the area of concern will be memory architectures. We'll be seeing much larger caches, multiple layers of caches, multiport and tagged memory architectures, and a general rethinking of the partitioning of CPU and memory."

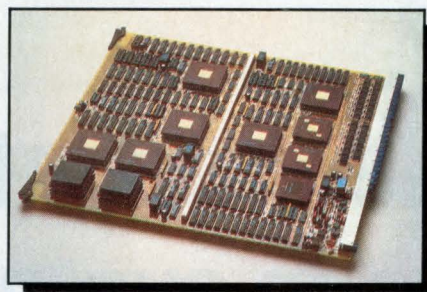
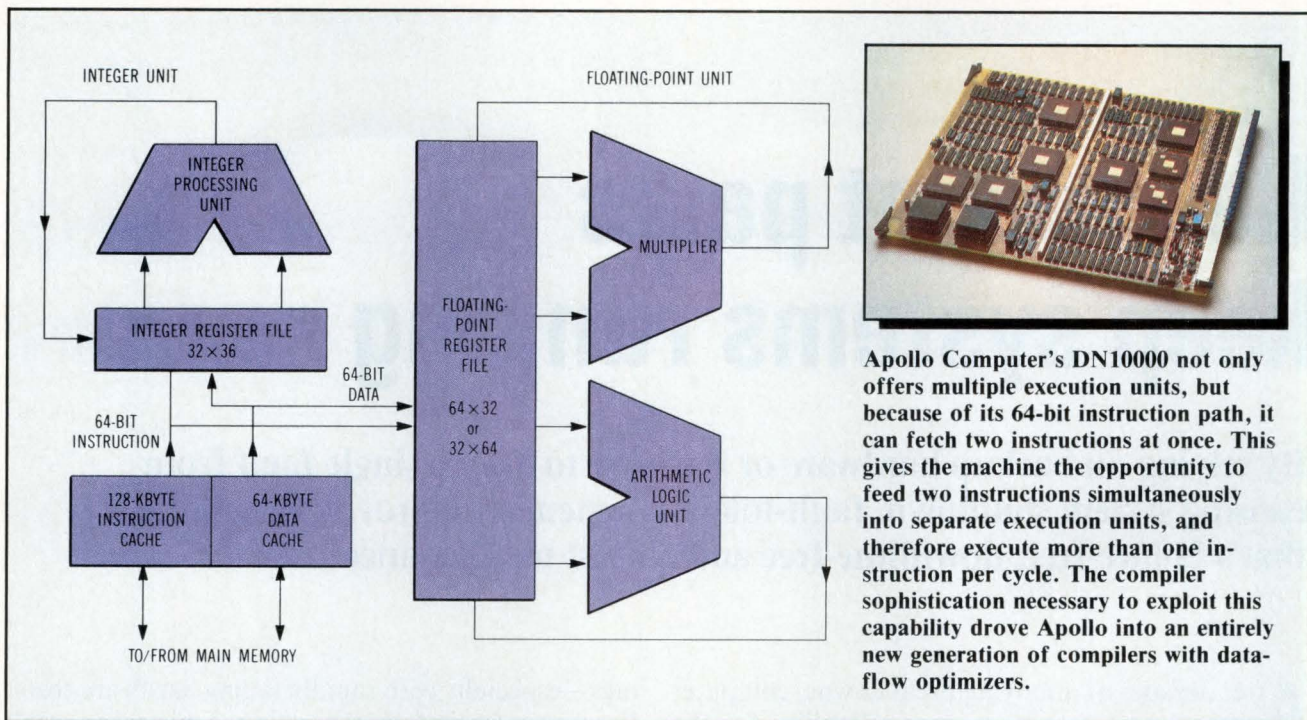
Michael Mahon, laboratory manager of the information technology group at Hewlett-Packard (Palo Alto, CA), cites I/O architectures as another area of current work. "I/O architectures have become extremely important. We see systems developing hierarchies of buses that all share common protocols."

As memory and I/O systems grow, the RISC instruction sets are feeling the tug of evolution as well. Perhaps an example of the force applications can exert on architecture is the HP Precision Architecture, as Mahon explains. "We started with code samples from all kinds of applications. We would postulate an architecture based on the instruction load, then mock it up and get feedback from the software tool and hardware design groups." HP's process not only reproduced the basic outlines of a RISC machine; it also added an array of new instructions, including floating-point, string and binary-coded-decimal operations.

Apollo Computer (Chelmsford, MA) also found it necessary to add instructions, in this case in pursuit of speed in floating-point-intensive engineering codes. Not only can the DN10000 perform floating-point instructions (in one cycle except for divide and square root), but it has some instructions especially adapted for the needs of analytical codes. "For our applications, the choice of instructions was critical," claims senior product manager Paul Bemis. "For instance, we have a five-operand multiply-add instruction. The machine can do a floating-point load on one execution unit while it's doing a multiply-add on another. This capability virtually lets the compiler configure the CPU as a vector processor."

As vendors, driven by new applications requirements, have added new instructions to basic RISC execution units, they have relied on partitioning to fight complexity. Many microprocessor and board-level designs have relied on coprocessors to handle floating-point computations. As cycle times decrease, designers are moving from coprocessors to separate execution units on an internal bus. This concept was apparent last fall in the latest Ridge





Apollo Computer's DN10000 not only offers multiple execution units, but because of its 64-bit instruction path, it can fetch two instructions at once. This gives the machine the opportunity to feed two instructions simultaneously into separate execution units, and therefore execute more than one instruction per cycle. The compiler sophistication necessary to exploit this capability drove Apollo into an entirely new generation of compilers with data-flow optimizers.

CPU, the 5100, and has since appeared in micro-processor designs from both Intel and Motorola.

"In the short term, we'll see machines break the one-cycle-per-instruction barrier," conjectures MIPS' Hennessy. "The new Apollo DN10000 seems to be heading in that direction." The 10000 attacks the barrier with 64-bit instruction and data paths. The wide instruction paths let the Apollo fetch unit load two instructions at once. If the instructions happen to be for different execution units, the machine will proceed to execute the two simultaneously.

"Further out," Hennessy continues, "we should see a cluster of processors driven off of a single instruction queue, under control of a combination of hardware interlocks and compiler intelligence. Essentially, these RISC architectures that can present a number of instructions at once to a number of execution units are moving toward very-large-instruction-word machines."

As the ability to handle multiple dissimilar execution units from one fetch unit increases, there will be more variety in the types of execution units vendors can provide. Chip vendors, with characteristic optimism, are already discussing coprocessors for signal processing, message handling and graphics. In the near future, a RISC CPU core may be added to all manner of specialized devices, from digital signal processors to three-dimensional graphics engines, as a simple matter of convenience.

And then what happens? Again Hennessy: "By 1992, the insights we've gained from the RISC con-

cept will start to play out. At that point, we'll need to find another new idea to put us back on a steep improvement curve. This time the breakthrough could come in multiprocessing, and again it could be led by software. Just as RISC technology let compilers make the CPU pipeline more efficient, perhaps a new technology will let compilers make a cluster of CPUs more efficient." **CD**

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# Redundant parts keep systems running

**By relying on backup hardware or software to keep a single fault from causing system shutdown, fault-tolerant systems can provide computing that's failure-free, downtime-free and almost maintenance-free.**

**A**fter decades of annoying breakdowns, computer systems now require greater reliability for the on-line computerized applications of the 1980s. System failures are, at the very least, time consuming and expensive, since they require system shutdown and restart, and they often have catastrophic results. They could idle a production line, damage the environment or even result in loss of life. In fact, applications such as nuclear reactor control systems haven't been fully computerized because of the potential impact of computer failures.

But there's a way to avoid such failures. Fault-tolerant computers—also known as redundant, survivable, robust, fail-safe or nonstop computers—provide failure-free computing with low maintenance and no downtime. They do so by detecting faults automatically and prompting immediate system reconfiguration.

Unlike more conventional, single-processor systems, fault-tolerant computers incorporate extra hardware, usually in the form of multiple processors, so a system can continue to operate despite the failure of any system component. Redundancy rarely calls for complete duplication of hardware, however; often it requires only a small amount of extra hardware or additional software. Even though the redundant parts represent an added expense for a system, it's a small investment compared to a fault-tolerant system's potential sav-

ings—especially with rapidly falling hardware costs. In some cases, in fact, the savings achieved by using a fault-tolerant computer can surpass initial system cost. The cost of a single computational failure can be extremely high for applications such as order-entry, financial transaction and data base on-line processing; nuclear, hazardous material and environmental control systems; life-support systems and critical medical electronics; and communications, surveillance and security systems.

Maintenance costs are also lower in fault-tolerant systems. Fault-tolerant computer systems containing ordinary commercial components allow fewer failures and cost much less than conventional systems with more expensive parts that have been screened for high reliability. Fault-tolerant systems feature fully automated diagnostics for maintenance and repair. Because maintenance costs often exceed a conventional system's original purchase price, these diagnostics are valuable.

Besides being cheaper to operate, fault-tolerant systems are more reliable. Minimizing downtime increases system availability, defined as the total time the computer is operational divided by the total time it's needed. In conventional systems, this number is often between 95 and 98 percent, a level that's inadequate for some applications. Fault-tolerant systems can be much more reliable, however. A fault-tolerant system designed recently for the U.S. Department of Transportation and the Department of Defense, for example, achieved a predicted availability of 99.999999 percent.

Fault tolerance is valuable in both transaction-processing applications and general-purpose com-

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## Gary Kravetz

*Kravetz is vice-president of engineering at Fail-Safe Technology (Los Angeles, CA).*

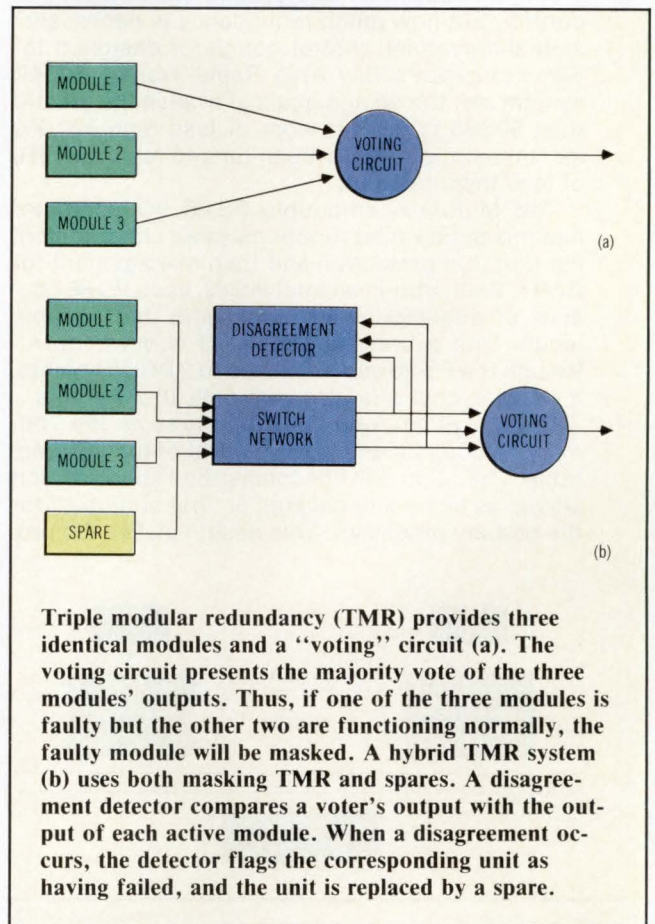


puting applications, such as process control, that are extremely sensitive to downtime. Transaction-processing applications encompass on-line inquiries of and updates to information stored in a large, shared data base. Each transaction—a complete task such as entering an order, reducing cash balance, moving goods from work-in-progress to finished goods, and so forth—is discrete, making fault tolerance easy to achieve. Transaction-processing applications typically use two processors that run separately. If the results agree, the transaction is considered valid. If they disagree, the processors both run self-tests. If one processor fails the self-test, it's locked out and manually repaired.

In the other category—general-purpose computing—applications are continuous rather than discrete, so fault tolerance isn't as easy to achieve. In general-purpose computing applications, fault-tolerant computers have traditionally used a triple modular redundancy (TMR) technique. To protect the system against failure, TMR uses three identical modules—such as a processor or a power supply—and a “voting” circuit that presents the majority vote of their outputs. A voter is much less complex than the modules it monitors and so is much less likely to fail.

Despite their relative simplicity compared to the modules they monitor, the voters in a system with TMR are complex enough to be difficult to design. Consequently, even though hardware costs have decreased in the last three years, systems with TMR have typically cost five times as much as nonredundant systems. Because such systems proved too costly and too difficult to maintain for most control applications, a lower-cost solution was needed.

To determine how much reliability most control systems require, a Fail-Safe Technology (FST) development team surveyed a number of general-purpose applications in aerospace, office automation and industrial automation industries and found that 21 percent would benefit from fault tolerance. Of this group, over 20 percent required dual-redundancy fault tolerance, but less than 1 percent required triple redundancy. In fact, the only systems FST identified as needing triple redundancy were aircraft fly-by-wire flight-control systems. Since dual redundancy (DR) sufficed for most of the systems, FST concluded that DR solutions needed to be developed. The company proceeded to develop a DR version of an IBM PC com-



patible. IBM PCs are used for aerospace, office and industrial applications, and the DR version can use all the existing software.

### Detecting and pinpointing a fault

Since the earliest digital systems, on-line testing has generally been done with hardware. Fault-tolerant computers make use of traditional techniques implemented with hardware: error checking (parity, Hamming and checksums, for example), logic duplication and comparison, majority voters with disagreement detectors, watchdog timers, and special circuitry to monitor critical elements such as power supplies and clocks.

Although testing with hardware is still the more familiar approach, software can also be used for on-line testing. By providing both self-test diagnostics and reasonableness checks on the outputs, such software can detect more than 99 percent of the on-line faults. In a fault-tolerant system, the data base is stored redundantly. After a potential



## Fault-tolerant microcomputing

The critical signals that run a high-speed train system require redundant I/O to ensure that a single subsystem failure can't cause a loss of control. But how much redundancy is necessary? A dual-redundant control computer designed for San Francisco's Bay Area Rapid Transit (BART) system met the design goals of availability greater than 99.986 percent, a cost of less than \$20,000 (per installation), and a mean-time-to-repair (MTTR) of less than one hour.

The Multibus-compatible FS-86 I/O computer handles such varied functions as air conditioning, lighting, fire protection and train management for BART. Built around an Intel 80386, each FS-86 consists of dual-redundant processors that communicate over a cross-strapped I/O subsystem. Although the FS-86 can handle up to 2,048 I/O points, it remains cost-effective with only 16 I/O points.

In the system, one CPU functions as the "primary" processor and takes control of the I/O functions. The other CPU becomes the "shadow" and serves as an on-line backup, or "hot standby," for the primary processor. This design makes the pro-

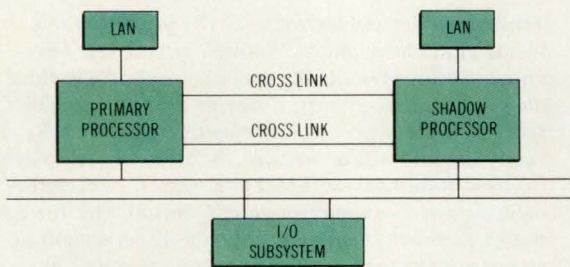
cessors available almost continuously and facilitates repair.

The primary processor communicates control information to the central operator's console and keeps the shadow processor current, using a loosely synchronized timing scheme and the periodic exchange of check data. The exchanged data consists of device-status tables, system-control parameters, and self-testing information. Optical isolation maintains electrical separation between the primary and shadow processors and between the processors and the I/O units.

The primary and shadow processors are connected by a dual-redundant serial communications path. The serial link is used to exchange and cross-check critical parameters. If an error is detected, further analysis determines the source of error. Because the FS-86 design permits hot sparing, virtually any component in the CPU or the I/O subsystem can be tested or replaced while the system is operating.

The FS-86 conducts self-diagnosis, involving a nondestructive processor, memory and I/O subsystem checks. Fault masking will find most faults before they affect an output. Redundancy also plays a part in the FS-86's dual-redundant power supplies, which ensure uninterrupted power.

The FS-86 software is organized as a collection of independent tasks. The operating system software schedules tasks in response to real-time events, such as interruptions from external devices, clock pulses or messages from other tasks. Semaphore and mailbox constructs in the real-time operating system provide task synchronization and resource sharing.



fault is detected, the system is tested again; if the fault no longer exists, all the copies of the data base are restored. Because they don't need extra hardware, software fault-tolerance methods save hardware costs but can slow down the applications software and take longer to detect the fault.

After a fault has been detected by either hardware or software, fault-diagnostic software is used to locate the source of a fault to the smallest replaceable unit—a component, circuit or subsystem. In general, diagnostics in fault-tolerant systems involve both hardware and special test software. In the simplest cases, the detection hardware points directly to the faulty unit, so additional isolation isn't required. But sometimes the detection hardware can only indicate several potentially faulty units, and additional hardware and software diagnostics must be used to isolate the fault.

### Recovering from a fault

A fault-tolerant system must be reconfigured after a fault has been detected. If possible, the recon-

figuration process restores the system to normal operation; otherwise, it may allow degraded operation or even invoke a systematic shutdown. In full recovery, a system returns to normal operation with its usual processing power and memory capacity, and any information damaged from the fault is restored to its fault-free values. In degraded recovery, also known as "fail-soft," a system returns to a fault-free state but loses some processing or memory capacity because the faulty unit has been switched off-line.

Recovery for fault-tolerant systems is automatic and can be either static or dynamic. Static recovery attempts to instantaneously hide, or mask, the effects of a fault, and dynamic recovery substitutes spares for faulty units. Fault-tolerant systems can combine static and dynamic techniques to suit reliability and availability requirements. The main criteria for determining whether recovery should be dynamic or static is how quickly the fault must be handled. For example, a nuclear reactor would need immediate recovery and so would have to use



mainly static techniques. A communications controller, on the other hand, can request a retry of transmission after a failure, so it could use dynamic recovery.

Fault masking prevents the effects of the fault from spreading beyond the replicated module. The faulty output of a module protected by fault masking doesn't propagate beyond the masking device—a voter, for example—so operation can continue. The masking device handles masking, testing, diagnosis and recovery, so additional diagnostics aren't needed. Error-correcting codes, replicated hardware and redundant software can be used to implement masking. But successful masking can only handle one fault at a time, and the redundant units must always be powered and ready.

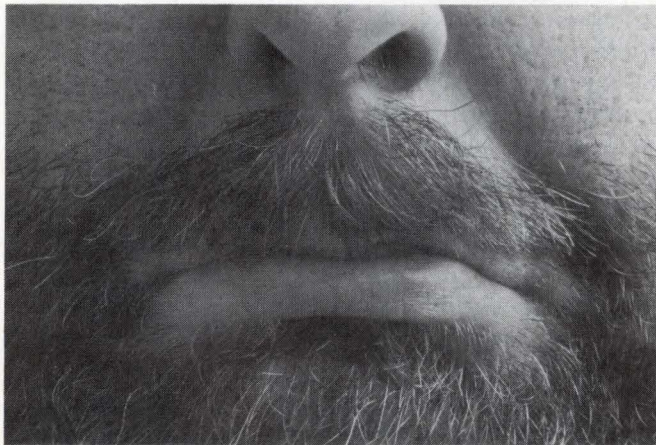
One of the most fundamental questions about masking is whether it should be implemented at the component, gate, module, subsystem or system level. At each level, masking has different costs and benefits. Use of masking, however, is always based on the low probability of correlated faults occurring in a redundant module and causing that module to fail. This assumption implies that masking

probably isn't feasible for protecting an IC package because if one component in the masking scheme fails, another will be similarly faulty.

Masking is most often implemented at three of those levels: component, gate and module. Two diodes in series that are parallel to two other diodes in series can achieve masking at the component level. This arrangement prevents one diode's failure from causing an open or a short circuit between the input and output. This four-diode scheme can be used as a fault-tolerant replacement for a single diode.

At the gate level, a masking scheme called "quadded" logic can protect both combinatorial and sequential networks. With this scheme, a logic network exists in quadruple redundancy. Quadded logic should be used when gates occupy different packages because it reduces the probability of common faults. An error resulting from a faulty network element will get corrected downstream from the error's origin, and fault-free neighboring signals will provide the means for correcting the fault. Quadded logic, popular in the days of discrete logic, is less suited to IC implementations, however, because designers can't change available ICs.

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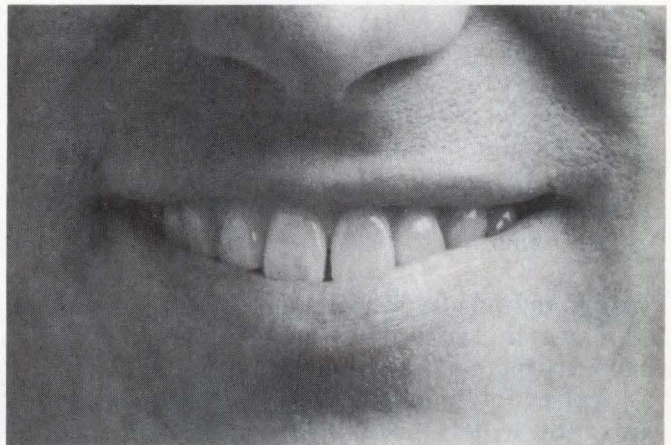
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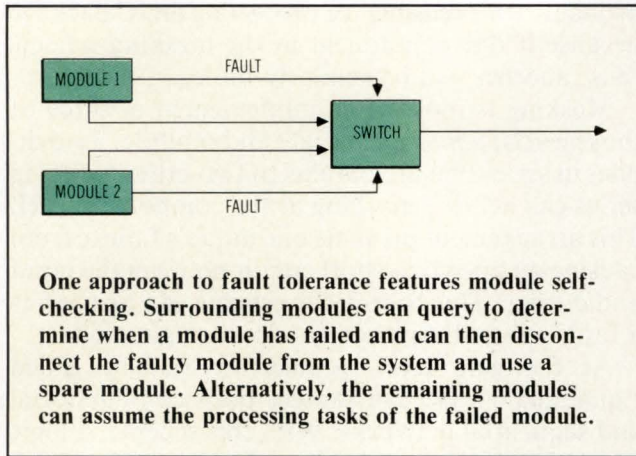


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Voting is a common form of masking at the module level. A three-input voter is used in TMR. The TMR technique can also be extended to include more modules, in which case it's referred to as N-modular redundancy (NMR). With NMR, additional faulty modules can be tolerated; in a five-module system, for example, NMR tolerates two faulty modules. The number of modules must always be odd so that a majority vote can exist.

The concept of NMR masking also extends to software. So-called N-version programming uses multiple, concurrently executing programs that have been independently designed, coded, tested and maintained. The N-version software system on which the programs run contains voting procedures and drivers that implement program-output comparisons and majority voting. N-version programming is able to mask the effects of a software fault because the probability of two independently generated software programs containing the same bug is very small.

### On-line redundancy switches units

Unlike static methods such as masking, dynamic recovery methods switch in on-line redundant units to replace faulty units in a system. Spare hardware units can be left in standby mode or left off until needed. The critical component in dynamic recovery is the switching mechanism. After diagnostics identify a faulty module, the switching mechanism must disconnect the failed unit and substitute a spare. If the switching mechanism functions incorrectly, the system can't recover.

There are at least two ways to switch to a spare unit. In one approach, the system removes power from the faulty unit and applies power to the replacement. The design of interface logic among units in such a system must disable the outputs when power is removed. Furthermore, the power switch's design must guarantee that the switch

won't fail. These switches frequently contain dual-coil relays in a series-parallel masking configuration. Since the switches use masking to guarantee that they'll perform correctly, the approach is a combination of dynamic and static methods.

A second approach to switching spares is to disconnect a faulty unit's outputs from the system and connect the spare's outputs to the system. Called cross-strapping, this technique uses ultra-high-reliability switches in a masking configuration.

In an implementation of a switch with a hybrid TMR system, which combines three active modules and one standby module, a disagreement detector compares the voter's output with the output of each active module. When a disagreement occurs, the detector flags the corresponding failed unit, and the unit is replaced by a spare. The approach can also be extended to a hybrid NMR system.

In another possible architecture—one that's more complicated and more difficult to implement—each module performs internal self-checking and records its own failure. Through a query mechanism, surrounding modules can determine when a module has failed. These modules can then agree to disconnect the faulty module from the system and replace it with a spare module. Alternatively, the remaining modules can assume the processing tasks of the failed module.

Software-module spares can also be used. This approach structures the software into blocks, each containing a spare module and a conventional non-redundant module that can detect errors. Acceptance testing, which determines whether the software modules are running correctly, is critical to the recovery-block methodology. When the test indicates a problem in the block being executed, a redundant block gets selected and run. The recovery-block technique can protect against software errors by requiring that each block be independently coded.

Fault tolerance is the key to the reliable use of computer power in downtime-sensitive applications. Each application of fault tolerance is unique, however; there's no such thing as a fault-tolerant computer for all applications. The implementation of fault tolerance must take into account many parameters, including initial cost, life-cycle cost, performance, reliability, the faults expected in the system, response to faults, and expected system use. **CD**

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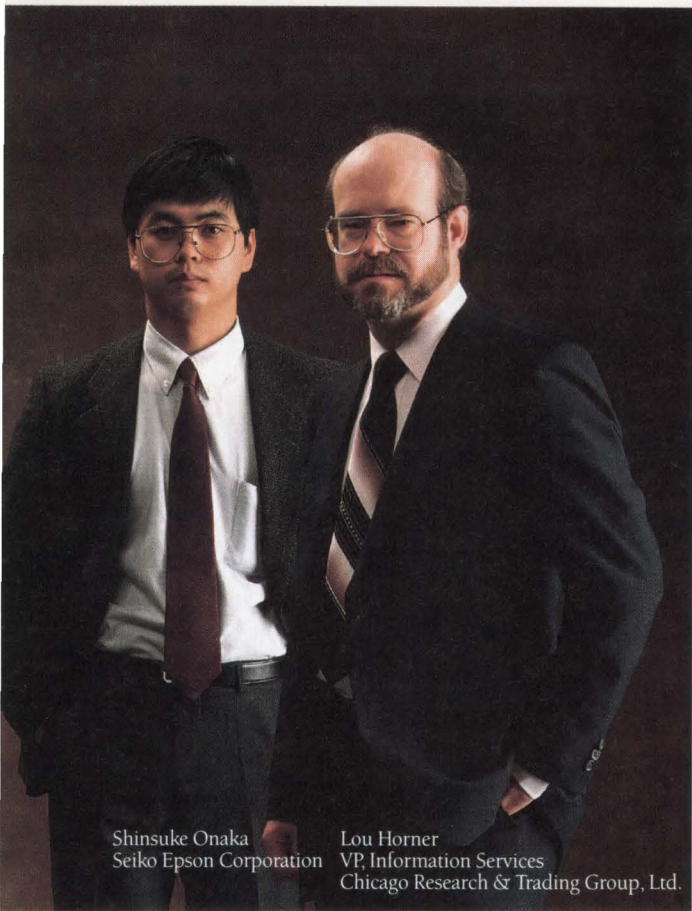
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# 1/4-in. tape drives follow desktop directions

Since 3M (St. Paul, MN) introduced it in 1971, 1/4-in. tape has been fighting an uphill battle for market acceptance. Initial reactions to the technology were less than enthusiastic, particularly since the backup needs of early desktop systems could be easily met by less expensive floppy disks. A continuing failure by manufacturers to provide standardized, interchangeable products did not help win design-ins. And recently, the promise of newer technologies like optical memory, digital audio tape (DAT) and 1/2-in. tape cartridges has cast doubt on the future of 1/4-in. tape.

But those days may be over. For backup applications in the low to mid-range (20 to 150 Mbytes), 1/4-in. tape has clearly emerged as the technology of choice for small system designers. In 1987, 1/4-in. cartridge drive manufacturers for the first

**John H. Mayer**  
Senior Associate Editor

## PRODUCT FOCUS

time shipped over 1 million units, over 30 times the volume of units shipped just five years ago, according to Raymond Freeman, president of Freeman Associates (Santa Barbara, CA).

The technology's success is attributed to a number of factors. Certainly the ability of manufacturers over the last few years to band together under the auspices of the Working Group for Quarter-Inch Cartridge Compatibility (QIC) and establish standard and interchangeable recording formats and interfaces has played an important role. Just as critical, however, has been vendors' ability to quickly deliver

the performance levels and capacities demanded by desktop systems in suitable formats and at reasonable prices. As high-performance desktop systems have added higher capacity Winchester's first in 100-Mbyte, and now in 200- and 300-Mbyte, capacities, tape drive vendors have quickly brought comparably high-capacity tape drives to the marketplace. At the low end, DC-2000 minicartridge drive vendors have moved quickly to accommodate the emerging 3 1/2-in. Personal System/2 format.

### Workstation-type capacity

Keeping pace with the frantic growth of memory capacity in small systems has played a pivotal role in the continued success of 1/4-in. tape. As capacities of 5 1/4-in. Winchester's have risen, the demand for comparable backup on a single tape has grown as well. Most major cartridge drive manufacturers now offer 1/4-in. tape drives in 60-, 120- and 150-Mbyte capacities. Typical of many vendors, for example, Cipher Data (San Diego, CA) has added 150- and 125-Mbyte drives to its product line.

At the highest performance levels, tape drive designers have been pushing beyond the 300-Mbyte plateau. Siemens-Tandberg Data (Newbury Park, CA), Archive (Costa Mesa, CA) and Wangtek (Simi Valley, CA) have all announced QIC-320 compatible units. The industry-standard QIC-320 recording format records data on 26 tracks at a density of 16,000 bits/in. Formatted capacity for a typical 600-ft 1/4-in. tape is 320 Mbytes, but it expands to 500 Mbytes with an extended-capacity cartridge. Although announced at Comdex last November, all three vendors are only now offering evaluation units. "I would expect units to be available in the market in the



QIC-40 compatible minicartridge tape drives like Colorado Memory Systems' Jumbo use Reed-Solomon error correction to achieve error rates as low as 1 in  $10^{14}$  bits read. This unit further ensures high reliability by integrating most drive functions into five custom ICs.



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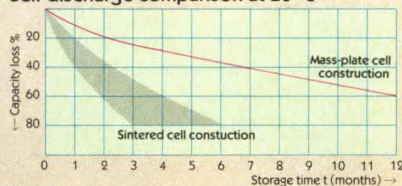
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Model	Capacity (Mbytes)	Recording Format	No. of Tracks	Density (kbits/in.)	Tape Speed (in./s)	Transfer Rate (kbytes/s)	Interfaces	Media	OEM Price	Comments
<b>Advanced Digital Information Corp</b>										<b>Circle 100</b>
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634	134 to 536	HCD-134	32	10	120	70	AT/SCSI	DC600XTD/HK	—	—
532	67 to 268	HCD-75	16	10	60	35	AT	DC600HC	—	—
400	40	—	24	12.5	60	2	SCSI	DC2000	—	—
<b>Algo 9198-C Red Branch Rd, Columbia, MD 21045 (800) 225-2546</b>										<b>Circle 101</b>
1200S	5.3	PE	4	1.6	30	6	RS-232	DC300XL, DC600A	\$1,995	intelligent stand-alone
1200i	5.3	PE	4	1.6	30	6	RS-232, IEEE-488	DC300XL, DC600A	\$2,170	same as above
1600	20	PE	4	6.4	30	24	RS-232	DC300XL, DC600A	\$2,995	same as above
ST1060	60	QIC-24	9	8	90	86.7	QIC-24	DC600A	\$1,595	external streaming
ST1060EG24	60	QIC-24	9	8	90	86.7	QIC-24	DC600A	\$1,980	same as above
ST1125	125	QIC-120	15	10	72	86.7	QIC-120	DC600XTD	\$2,180	same as above
<b>Alloy Computer Products 100 Pennsylvania Ave, Framingham, MA 01701 (617) 875-6100</b>										<b>Circle 102</b>
TS/2	40	QIC-40	20	10	50	500*	floppy	DC2000	—	PS/2-comp.
RET/40	40	QIC-40	20	10	50	500*	floppy	DC2000	—	PC-, XT, AT-comp.
RET/120	120	MFM	20	10	50	500*	—	DC600XTD	—	PS/2- & PC-comp.
<b>Analog &amp; Digital Peripherals 251 S Mulberry St, PO Box 499, Troy, OH 45373 (513) 339-2241</b>										<b>Circle 103</b>
Feedback 344	18	—	4	6.4	45	38.4	RS-232	DC600	\$2,195	RS-232 interface
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<b>Archive 1650 Sunflower Ave, Costa Mesa, CA 92626 (714) 641-0279</b>										<b>Circle 104</b>
5945	60	QIC-11 & QIC-24	9	8	90	90	QIC-36, QIC-02, SCSI	DC300XL, DC600A/XTD	—	5¼ in., half, full height
FT60	60	QIC-11 & QIC-24	9	8	90	90	QIC-02 4	DC300XL, DC600A/XTD	—	external
2060	60	QIC-11 & QIC-24	9	8	90	90	QIC-02, SCSI	DC300XL, DC600A	—	5¼ in., half height
2150	150	QIC-150	18	10	90	112.5	QIC-02, SCSI	DC600A/XTD	—	5¼ in., half height
2320	320	QIC-320	26	16	90/120	180/240	QIC-02, SCSI	DC600XTD	—	5¼ in., half height
60e	60	QIC-24	9	8	90	90	QIC-02, SCSI	DC300A/XL, DC600XTD	—	external
150e	150	QIC-150	18	10	90	112.5	QIC-02, SCSI	DC600A/XTD	—	external
5220/5520	20	QIC-40	10	10	25/50	250/500*	floppy	DC2000	—	5¼ in., half height
5240/5540	40	QIC-40	20	10	25/50	250/500*	floppy	DC2000	—	5¼ in., half height
3030	40	QIC-40	20	10	50	500*	floppy	DC2000	—	external for PS/2
3550/60	40	QIC-40	20	10	50	500*	floppy	DC2000	—	3½ in., PS/2-comp.
3580/3580e	80	QIC-80	28	14	35	500*	floppy	DC2000	—	internal/external
5580	80	QIC-80	28	14	35	500*	floppy	DC2000	—	3½ in.

Key: comp. = compatible; FAD = file access device; GCR = group code recording; MFM = modified frequency modulation; NTDS = Navy Tactical Data System; PE = phase encoded; prop. = proprietary; SCSI = small computer system interface; serp. = serpentine; XTD = extended; \* = kbytes/s.



Model	Capacity (Mbytes)	Recording Format	No. of Tracks	Density (kbits/in.)	Tape Speed (in./s)	Transfer Rate (kbytes/s)	Interfaces	Media	OEM Price	Comments
<b>California Peripherals</b> 955 Francisco St, Torrance, CA 90502 (213) 538-1030										<b>Circle 105</b>
CP-60	60	QIC-24	9	10	90	90	QIC-02, QIC-36 SCSI	DC600A	\$265	loading door
CP-125	125	QIC-120	15	12.5	72/90	90/112	QIC-36, QIC-02, SCSI	DC600A	\$340	loading door
CP-150	150	QIC-150	18	12.5	72/90	90/112.5	QIC-36, QIC-02, SCSI	DC600A/XTD	\$340	loading door
<b>Cipher</b> 10101 Old Grove Rd, San Diego, CA 92138 (800) 424-7437										<b>Circle 106</b>
540/540+	60/150	QIC-24/ QIC-150	9/18	8/10	90	87	QIC-02, QIC-36, SCSI	DC300XL, DC600A/XTD	\$500	two models, full height
ST150S	150	QIC-150/ QIC-120	18	10	72/90	87	SCSI, SCSI-2	same as above	\$510	half height
<b>CMS Enhancements</b> 1372 Valencia Ave, Tustin, CA 92680 (714) 259-9555										<b>Circle 107</b>
T160/T160EXT	45/60	serp.	9	8	90	90	QIC-36	DC300XL, DC600A	\$995/ \$1,095	internal/external, IBM PC-comp.
<b>Colorado Memory Systems</b> 800 S Taft Ave, Loveland, CO 80537 (303) 669-8000										<b>Circle 108</b>
Jumbo	40	QIC-40	20	10	90	250/ 500*	floppy	DC2000	\$250	3½ in., dual speed
QIC-60	60	QIC-24	9	10	90	720*	QIC-02	DC600	\$695	internal/external
QIC-125	125	QIC-120 & QIC-24	15	10	90	720*	QIC-36	DC600	\$595	internal/external
<b>Data Track USA</b> 9451 Sohap Ln, Columbia, MD 21045 (301) 992-9143										<b>Circle 109</b>
Tracker 1600	5.5	PE	4	1.6	30/90	19.2	RS-232	DC300, DC600	\$2,100	stand-alone
Tracker 1700	40	MFM invert	4	1.7	30/90	38.4	RS-232, RS-422, Centronics	DC300, DC600	\$2,495	same as above
<b>Emerald Systems</b> 4757 Morena Blvd, San Diego, CA 92117 (619) 270-1994										<b>Circle 110</b>
60-2000 series	60	QIC-24	9	8	90	75	QIC-02	Lifetape 60	\$1,495	internal, 5¼ in.
60-9000 series	60	QIC-24	9/18	8	90	75	QIC-02	Lifetape 60	\$1,795	5¼ in., PS/2-comp.
150-9000 series	150	QIC-150	18	8	90	75	QIC-02	Lifetape 150	\$2,695	external, PC bus
150-9107 series	150	QIC-24	18	8	90	75	QIC-02	Lifetape 150	\$2,695	5¼ in., PS/2-comp.
150-2000 series	150	QIC-150	18	8	90	75	QIC-02	Lifetape 150	\$2,395	5¼ in., PC bus
<b>Genisco Peripheral Systems</b> 10874 Hope St, Cypress, CA 90630 (714) 220-0720										<b>Circle 111</b>
Cart. Drives	3	ANSI, serp.	4	1.6/ 6.4	30/90	6,24	custom, RS-232	—	\$3,500 to \$21,000	ruggedized subsystems
<b>Hewlett-Packard</b> Computer Peripherals Bristol, Filton Rd, Stoke Gifford, Bristol, BS12 6QZ, UK (Call local sales office.)										<b>Circle 112</b>
HP7946A	67	prop.	16	10	60	—	HPIB	DC600	—	disk & tape combined
HP9144A	67	prop.	16	10	60	—	HPIB	DC600	—	tape drive only
HP35401A	536	prop.	16	10	60	—	HPIB	DC600	—	autochanger



# SYSTEM PRODUCTS/Memory Systems

Model	Capacity (Mbytes)	Recording Format	No. of Tracks	Density (kbits/in.)	Tape Speed (in./s)	Transfer Rate (kbytes/s)	Interfaces	Media	OEM Price	Comments
<b>Irwin Magnetic Systems</b> 2101 Commonwealth Blvd, Ann Arbor, MI 48105 (313) 996-3300										<b>Circle 113</b>
110	10.4	MFM	8	6.4	39/70	250*	floppy	DC1000	\$399	5¼ in., half height
120	19.5	MFM	14	6.4	39/70	250*	floppy	DC2000	\$499	5¼ in., half height
125	21.6	MFM	12	10	50/70	500*	floppy	DC1000	\$499	5¼ in., half height
145	40.6	MFM	20	10	50/70	500*	floppy	DC2000	\$699	5¼ in., half height
220	19.5	MFM	14	6.4	39/70	250*	floppy	DC2000	\$499	3½ in., half height
225	21.6	MFM	12	10	50/70	500*	floppy	DC2000	\$499	3½ in., half height
245	40.6	MFM	20	10	50/70	500*	floppy	DC2000	\$649	3½ in., half height
265	64.5	MFM	24	13.2	38/63	500*	floppy	DC2000	\$849	3½ in., half height
<b>Miltope</b> 1770 Walt Whitman Rd, Melville, NY 11747 (516) 420-0200										<b>Circle 114</b>
CR300	46	PE	4	1.6/ 3.2	30/90	384	TTL, NTDS, RS-232	DC300	\$17,250	meets MIL-STD
<b>Mountain Computer</b> 240 Hacienda Ave, Campbell, CA 95008 (408) 379-4300										<b>Circle 115</b>
TD4000	60	QIC-40	20	10	50/90	62.5	SA450	DC2000	\$300	5¼ & 3½ in.
<b>Siemens-Tandberg Data</b> 1077 Business Center Cir, Newbury Park, CA 91320 (818) 706-8872										<b>Circle 116</b>
3610/20	60	QIC-24	9	8	90	—	SCSI/QIC-02	DC300XLP	\$785	5¼ in., half height
3630/40	120	QIC-120	15	10	72	—	SCSI/QIC-02	DC600A	\$860	5¼ in., half height
3650/60	150	QIC-150	18	10	72	—	SCSI/QIC-02	DC600XTD	\$860	5¼ in., half height
3800	320	QIC-320	26	—	120	—	SCSI/QIC-02	DC600XTD	\$995	5¼ in., half height
<b>Stream Technology</b> 556 Gibraltar Dr, Milpitas, CA 95035 (408) 263-4411										<b>Circle 117</b>
3208	72	GCR	26	10	72	90	SCSI, QIC-24	DC2000	\$300	3½-in. streaming
<b>Sysgen</b> 556 Gibraltar Dr, Milpitas, CA 95035 (408) 263-4411										<b>Circle 118</b>
Streamtape	72	GCR	26	10	72	90	QIC-36	DC2000	\$450	subsystem
QIC-file	60	GCR	9	8	90	90	QIC-36	DC600A	\$430	same as above
Bridge-Tape	42	MFM	24	8.6	90	250/ 500*	QIC-40	DC2000	\$350	same as above
Net-file	120	GCR	15	10	90	90	QIC-120	DC600XTD	\$900	same as above
<b>Tallgrass Technologies</b> 11100 W 82nd St, Overland Park, KS 66214 (913) 492-6002										<b>Circle 119</b>
TG-1020i	20/30	QIC-100	12	10	75	750*	QIC-103	DC2000	\$495	external
TG-1020e	20/30	QIC-100	12	10	75	750*	QIC-103	DC2000	\$795	external
TG-1040i	40/60	QIC-100	24	10	75	750*	QIC-103	DC2000	\$695	5¼ in.
TG-1040e	40/60	QIC-100	24	10	75	750*	QIC-103	DC2000	\$995	external
TG-4060	60/100	QIC-100	11	8.2	75	750*	QIC-103	DC600A	\$1,295	5¼ in., external only
TG-4120	120/ 200	QIC-100	22	8.2	75	750*	QIC-103	DC600XTD	\$1,595	5¼ in., external only
<b>Tecmar</b> 6225 Cochran Rd, Solon, OH 44139 (216) 349-0600										<b>Circle 120</b>
QT40i	40	QIC-40	20	10	50/90	500*	floppy	DC2000XTD	\$595	5¼ in., internal
QT40e	40	QIC-40	20	10	50/90	500*	floppy	DC2000XTD	\$795	PC, XT, AT-comp.
QT Mac40	38.5	QIC-100	24	10	75/90	750*	SCSI	DC2000XTD	\$1,395	Macintosh-comp.
QT125i	125	QIC-120	15	10	72/90	90	PC-36	DC600XTD	\$1,895	5¼ in., internal
QT90i	90	QIC-120	11	10	72/90	90	PC-36	DC600XTD	\$1,695	5¼ in., internal





# Unhitch Your VME CPU From Analog I/O

Until now you've probably had to contend with excessive Analog I/O overhead on your VME CPU. Start and stop... a few bytes at a time... hurry up and wait... and grit your teeth!! Why? Because conventional VMEbus I/O boards have to empty after *every* sample. These interrupts can choke even the fastest CPU. But, there is a cure.

## Memory Buffering Makes the Difference

Just look at our MPV952 High-Speed VME Analog I/O Board. We think you'll find the relief you're looking for. It samples from eight input channels to convert 12-bit data in just 1.5 $\mu$ s. Fast? Yes! And the results are stored in onboard data buffers. That's the secret. These buffers are 36k words of RAM that work in unison. The host processor can now unload a block of data from one buffer while the other is being filled with new data. Less interrupts, faster acquisition. Just right for those high-speed 32-bit UNIX<sup>®</sup>-based system such as the Sun<sup>™</sup> workstation. But, there's more. To free the CPU even further, the size

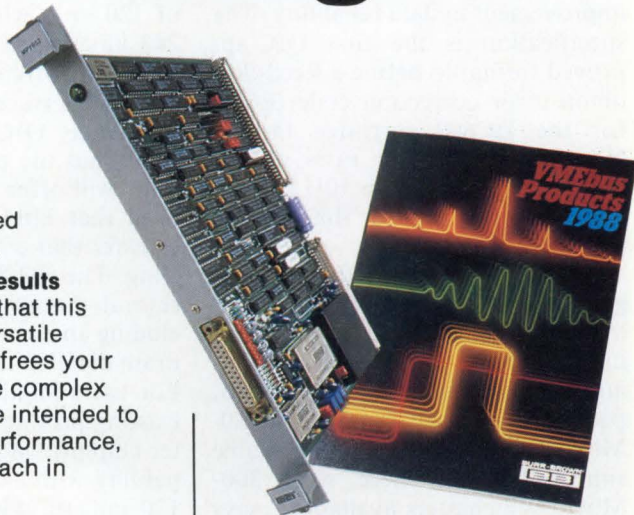
of the data blocks to be gathered, the sampling rate, and the number of channels to be sampled are all programmable.

## Look Closely at the Results

We think you'll agree that this is the fastest, most versatile board around. And, it frees your workstations to do the complex calculations they were intended to do. Excellent price/performance, too! Just over \$2500 each in quantities of 10.\*

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UNIX<sup>®</sup> AT&T, Bell Laboratories; Sun<sup>™</sup> Sun Microsystems, Inc.



\*U.S. prices only.



# SYSTEM PRODUCTS/Memory Systems

Model	Capacity (Mbytes)	Recording Format	No. of Tracks	Density (kbits/in.)	Tape Speed (in./s)	Transfer Rate (kbytes/s)	Interfaces	Media	OEM Price	Comments
<b>Tecmar</b> 6225 Cochran Rd, Solon, OH 44139 (216) 349-0600										<b>Circle 120</b>
QT60i	60	QIC-120	9	10	72/90	90	PC-36	DC600XTD	\$1,365	5 1/4 in., internal
QT125e	125	QIC-120	15	10	72/90	90	host	DC600XTD	\$2,295	external, IBM-comp.
QT90e	90	QIC-120	11	10	72/90	90	host	DC600XTD	\$1,845	external, IBM-comp.
QT60e	60	QIC-120	9	10	72/90	90	host	DC600XTD	\$1,495	external, IBM-comp.
<b>3M, Magnetic Media Div.</b> Building 223-5N, 3M Center, St Paul, MN 55144 (612) 733-5454										<b>Circle 121</b>
MCD-40 FITD	40	QIC-40	24	8.6	29/58	250/ 500*	SA450/475	DC2000	\$545	—
MCD-40 SCSI	40	QIC-100	24	10	60	21	SCSI	DC2000	\$795	—
HCD-75	67	—	16	10	60	35	SCSI	DC600	\$1,150	—
HCD-134	134	—	32	10	120	70	SCSI	DC600	\$1,295	—
<b>Wangtek</b> 41 Moreland Rd, Simi Valley, CA 93065 (805) 583-5255										<b>Circle 122</b>
5125	125	QIC-120	15	10	72	90	QIC-02	DC600	—	5 1/4 in., half height
5150	150	QIC-150	18	10	72	90	SCSI	DC600	—	5 1/4 in., half height
5320	320	QIC-320	26	16	120	240	SCSI	DC600	—	5 1/4 in., half height
FAD 3500	40	QIC-40	20	10	25/50	250/ 500*	FAD, QIC-40	DC2000	—	3 1/2 & 5 1/4 in.

third or fourth quarter," speculates Bob King, director of marketing and sales at Wangtek.

Besides increased capacity, the QIC-320 drives offer a formidable improvement in data reliability. The specification is the first QIC-approved format to define a Reed-Solomon error correction code (ECC) for the DC600 cartridge family. Nonrecoverable error rates are no more than one error in  $10^{14}$  bits, or about 100 times better than typical rigid disk drive rates.

The target for these drives is the growing number of 300-Mbyte and higher Winchester drives designed into higher-performing workstations and desktop systems. "A year ago, people would have gone with a 320-Mbyte tape drive if it were available simply because there were 300-Mbyte Winchesters available," says King. One of the first models announced, the Model 3800 from Siemens-Tandberg Data backs up 320 Mbytes in 27 min. The half-height, streaming tape drive features a 64-kbyte buffer, operates at 120 in./s

and uses Series 600XTD media. The 3800 will also read 60-, 125- and 150-Mbyte tapes.

Wangtek's 320-Mbyte drive, the Model 5320ES, operates at a speed of 120 in./s with a transfer rate of 240 kbytes/s. Like its competitors, the drive offers a small computer system interface (SCSI). "You may see some QIC-02 interfaces out there, but the predominance of the units will offer a SCSI because you need that kind of performance to transfer that amount of data," says King. The 5320ES also incorporates several custom-developed ICs, including an error correction chip that dramatically improves reliability. For users looking to upgrade from existing products, a custom formatter chip provides backward read capability with existing QIC-24, QIC-120 and QIC-150 recording formats.

Archive's 320-Mbyte unit is part of the company's Viper product line. The Viper 2320 is a half-height, 5 1/4-in. streaming drive available with SCSI and QIC-02 interfaces. Extensive use of highly integrated parts

and surface-mount technology lets Archive pack the drive into a compact box. Like its competitors, the 320-Mbyte Viper reads tapes written on 150-Mbyte and 125-Mbyte drives.

Of course, the 320-Mbyte drives would hardly be viable without complementary media. Both 3M and Data Electronics Inc (San Diego, CA) have developed high-capacity cartridges in parallel with the new drives. QIC-150 drives typically use 3M's DC600XTD cartridge, which is capable of 12,500 flux reversals/in. at 90 in./s over an 18-track scheme. The DC600XTD+ contains 600 ft of 1/4-in. tape designed to record and read data in a 26-track serpentine format with 20,000 flux reversals/in. The cartridge operates in drives running at 120 in./s.

The key to achieving higher data recording densities is repeatability. Lateral tape movement in both 3M's and DEI's cartridges is minimized by one-piece tape guides. To limit the distance that the tape travels freely, an additional post is added near the read/write head. "The DC600-



XTD+ will exhibit virtually no perpendicular variation— $\pm 1/2$  mil across the 5-mil read width of the QIC-320 track,” says James Milligan, business development manager for 3M’s magnetic media division.

#### **QIC-40 drives proliferate**

Despite the excitement surrounding the higher-capacity units, the fastest-growing market lies in those drives backing up ever-popular personal computers. Cartridge drives built around the QIC-40 recording format are finding broad appeal as low-cost, highly interchangeable backup. QIC-40 specifies 40 Mbytes of data stored on 20 tracks at 10,000 flux reversals/in. The standard lets users freely exchange files in standard DC-2000-type minicartridges across a wide range of drives from a variety of manufacturers and backed by various application programs and operating systems.

QIC-40 offers significant advantages over earlier formats. Unlike previous standards that failed to specify important compatibility factors, QIC-40 provides interchange compatibility at the format, file and operating system level. As a result, the specification supports popular operating systems, including DOS and Unix, making it ideally suited for IBM PS/2 and PC products.

In addition, the specification significantly reduces tape format time by relieving users of the need to servo-write-pass or bulk-erase a tape prior to formatting. To speed access of reader files, the format supports direct track stepping, an approach that lets the drive jump directly to a specific track rather than search for a file sequentially through all previously recorded data.

QIC-40 drives are presently available from most major vendors, including Alloy Computer Products (Framingham, MA), Archive, Colorado Memory Systems (Loveland, CO), Mountain Computer (Campbell, CA), Tecmar (Solon, OH), 3M and Wangtek. Virtually all the units are targeted at the PC market and come in either half-height 5/4- or 3/2-in. formats. Many of the newer

units, such as Archive’s ArchiveXL, for example, are PS/2-compatible and come in both internal and external versions. One attraction of the QIC-40 format is its use of the PC’s floppy disk interface. Running off the floppy disk interface offers a significant cost savings to the system integrator, but limits data transfer to 250 kbits/s for an IBM PC XT-type controller, or 500 kbits/s for the IBM PC AT- or PS/2-type.

One QIC-40 drive accommodates either controller automatically. Introduced in January, Jumbo from Colorado Memory Systems samples the data transfer rate and automatically defaults to the fastest available speed. “Most backup manufacturers require a different model tape drive from the XT- or AT-/PS/2-type controller,” claims William T. Beierwaltes, president of Colorado Memory Systems. “Our unit permits dense migration as computers are upgraded or when a drive is shared among different computer models in the office.”

Colorado Memory Systems has also implemented a number of design features to improve reliability. The unit uses durable dc brushless motors and eliminates all adjustment pots on the printed circuit boards. IC component count was reduced to roughly one-third that of competing models by integrating multiple functions into five ASICs. “Circuit-wise, it’s the simplest, lowest parts count circuit on the market,” Beierwaltes claims.

#### **Other DC2000-type options**

Despite the claim by some vendors that QIC-40 is the standard of choice, other DC2000-type options do exist for the PC user. In fact, the market leader in the minicartridge market, Irwin Magnetic Systems (Ann Arbor, MI), uses a proprietary formatting technique. The company offers both 5/4- and 3/2-in. models ranging in capacity from 10 to 65 Mbytes. All models feature embedded servos and dedicated software designed to position the heads in the center of each track.

Another option comes from Tall-

grass Technologies (Overland Park, KS). The QIC-100 format, originally developed at the company and then adopted early on by Apple Computer (Cupertino, CA), is used in the Tallgrass TG-1020 and TG-1040 models. Ranging in capacity from 20 to 60 Mbytes, the drives conform to either 5/4- or 3/2-in. formats in either internal or external units.

A subsidiary of Sysgen, Stream Technology (Milpitas, CA) is marketing the first commercial streaming tape drive using the DC2000 minicartridge in the 3/2-in. form factor. The Model 3208 records data in a 32-track serpentine format that yields a 72-Mbyte capacity. Tape speed is 72 in./s. In addition, the company claims to be the first in the industry to introduce ferrite heads into a 3/2-in. minicartridge drive.

Stream Technology hopes to get a head start on the competition as desktop systems using the 3/2-in. format move to higher performance levels. By using an embedded SCSI or a QIC-36 interface rather than the floppy interface, the 3208 can transfer data at up to 5 Mbytes/s. “The nonstreaming drives are geared to people who don’t want to buy a controller,” claims Doug Bercow, director of marketing at Stream Technology. “We wanted to have a higher-capacity drive because as hard disk capacities grow, tape capacity needs grow. Users won’t want to wait for data to pass through their floppy disk controllers.”

In the meantime, movement is afoot to develop QIC specifications that accommodate higher storage capacity and data transfer rates with the DC2000 cartridge. Adopted by QIC in February, QIC-80 supports twice the capacity of QIC-40 using the same interface. To meet the higher data transfer needs of higher-capacity drive users, a standard has also been developed around the SCSI interface. Dubbed QIC-110, the standard defines a recording format for the DC2000 minicartridge that will provide 110 Mbytes and will be backward-read compatible with QIC-40 tapes. QIC-110 was formally adopted in April.

**CD**

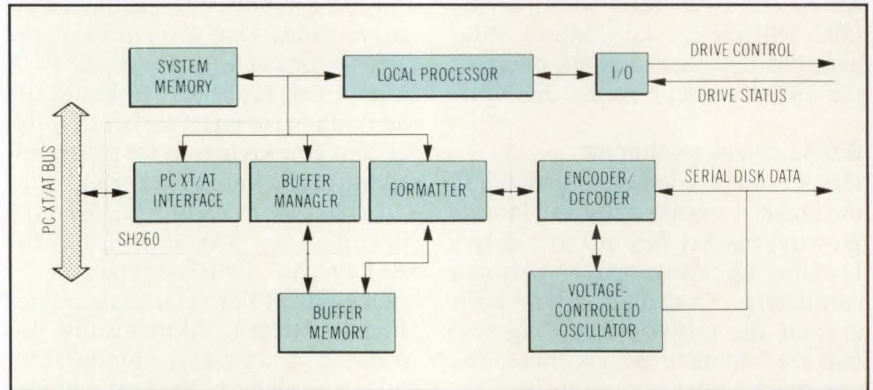


## Chip integrates XT/AT Winchester disk control functions

Designers building 80286- and 80386-based systems now have a single-chip solution to hard disk control. The CL-SH260 is the first IC to integrate a formatter, a buffer manager and IBM PC XT/AT bus controller functions onto one chip.

Manufactured in an advanced CMOS process, the chip consumes less than 500 mW, making it extremely applicable to the power-conscious portable computer market. Replacing up to eight current VLSI or MSI chips, the highly integrated solution lets designers of embedded intelligent drives install multiple drives on the same PC bus in a master/slave configuration.

The chip can handle data rates up to 20 Mbits/s. Unlike the 3:1 sector interleave common on most control-



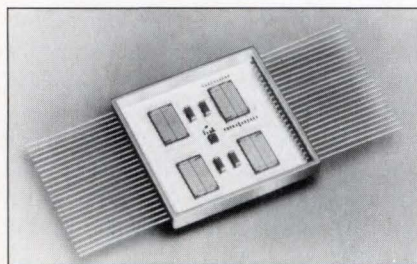
lers, the CL-SH260 supports a 1:1 interleave with a concurrent sustained transfer rate of 2 Mbytes/s on the disk and 4 Mbytes/s on the host bus. Data throughput is increased by a factor of three. Automatic wait-state generation on the host bus in-

terface provides compatibility with speed grades of host processors ranging from a 6-MHz 80286 to a 20-MHz 80386. In volume quantities, the chip sells for under \$30.

**Cirrus Logic**, 1463 Centre Pointe Dr, Milpitas, CA 95035. **Circle 125**

## Compact megabit SRAM hybrid suits military systems

Packaged in a 1.25- $\times$ 1.25- $\times$ 0.15-in. 46-pin hermetic flatpack, the MEM-84000 is a 1-Mbit full-MIL static RAM hybrid. Access time is 100 ns. Organized as 64k $\times$ 16 bits, the SRAM is designed to support 16- or 32-bit processors in military applications. The hybrid combines four TTL-compatible 32k $\times$ 8 RAM chips and transfers data using 16 address lines, 16 data lines and standard read, write and enable lines. With external decoding, the part is expandable to any memory width and depth. Pricing starts at \$750. **ILC Data Device**, 105 Wilbur Place, Bohemia, NY 11716. **Circle 126**



## CMOS GAL devices offer 15-ns access

A family of E<sup>2</sup>CMOS Generic Array Logic (GAL) devices provide reconfigurable logic with bipolar speed at low power levels. Maximum operating currents for the GAL16V8 and GAL20V8 parts range from 45 to 90 mA. Access times run from 15 to 35 ns. The devices include test circuitry and reprogrammable cells that allow extensive testing during manufacture. A minimum of 100 erase/write cycles is guaranteed. Prices in quantity range from \$3.75 to \$10.35. **National Semiconductor**, 2900 Semiconductor Dr, PO Box 58090, Santa Clara, CA 95052. **Circle 127**

## Octal register improves system debug

The IDT49FCT818 is the first CMOS octal register with a Serial Protocol Channel feature, which lets designers perform scan techniques at the component and board level to improve system debug in the devel-

opment phase. With 12.5-ns propagation delays, the part can be used in any data path, control path or pipelining application and is easily paralleled in a single serial loop. Like other devices in the company's FCT family, the IDT49FCT818 features the drive of bipolar registers ranging from 32 mA for commercial applications to 24 mA for the military market. Available in plastic and sidebraced dual in-line packages and leadless chip carriers, the octal register sells for \$3.35 and up in quantities of 100. **Integrated Device Technology**, 3236 Scott Blvd, Santa Clara, CA 95054. **Circle 128**

### Trademark Information

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GEOMETRY ENGINE is a trademark of Silicon Graphics Inc.

APLEX and UTX/32 are trademarks of Gould Inc.



## DSP chip delivers general-purpose IEEE floating-point performance

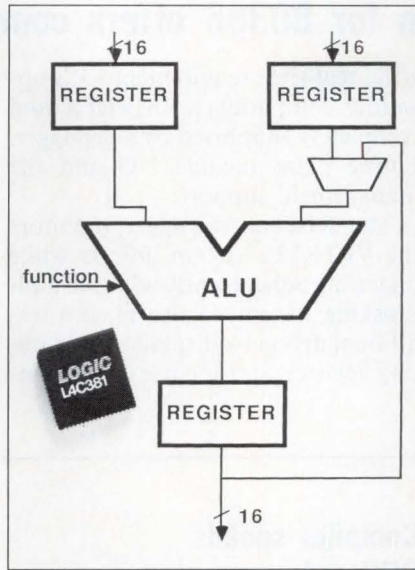
Software-compatible with the fixed-point DSP 56001, an off-the-shelf DSP chip provides general-purpose IEEE floating-point performance for real-time applications such as high-speed control, digital audio, numeric processing, speech and image processing and spectral analysis. Claiming a peak performance of 40 MFlops, the DSP 96001 is the first of a family of single-chip HCMOS digital signal processors. The chip offers 512 words of on-chip program RAM, two preprogrammed data ROMs, on-chip bootstrap hardware to speed loading of user programs and program RAM, and on-chip debug circuitry to provide access to internal resources in support of circuit emulation. The CPU comprises three 32-bit execution units operating in parallel—a data ALU, an address generation unit and a program controller. The DSP96001 has MCU-style on-chip peripherals (serial communication interface, synchronous serial interface and 32-bit host interface), program and data memory, and a memory expansion port to simplify interfacing to page mode and video RAMs. **Motorola**, Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735.

Circle 129

## Converter serves synchro control systems

Offering an accuracy of 6 arc-seconds, the SD(RD)570 synchro-to-digital 20-bit converter has a resolution of 1.24 arc-seconds. Features include built-in test, an anti-180° false lock-up circuit, and a reference synthesizer and analog velocity output. The device uses high accuracy precision transformer-isolated inputs configured for either synchro or resolver inputs. Tracking rate is 720 degrees/s. **Natel Engineering**, 4550 Runway St, Simi Valley, CA 93063.

Circle 130



## CMOS 16-bit ALU hits high speed

Combining the functionality of several chips in digital signal processing or image-processing systems, the L4C381 CMOS 16-bit ALU can perform any of five arithmetic or five logical functions on two 16-bit inputs in 26 ns in flow-through mode. In registered-add mode, the new part completes a function in 20 ns. Each of two 16-bit inputs on the device has a register. Users can load two data values simultaneously from a 32-bit bus or one data value at a time from a 16-bit bus. A register on the 16-bit output, along with a feedback path, lets the chip recycle an output result back to an input. Price in quantity for the 26-ns part is \$24. **Logic Devices**, 628 E Evelyn Ave, Sunnyvale, CA 94086.

Circle 131

## Single-chip 64-bit floating-point processor supports multiple formats

The Am29C327 is the first floating-point processor to support IEEE-754, DEC D, F and G, and IBM floating-point formats. Performing arithmetic and logic operations on both 32- and 64-bit integers, the part includes an instruction set with more than 70 instructions. The 1.2-micron CMOS chip is available at either 100

ns or 120 ns and operates in either a flowthrough or pipelined mode. Packaged in a 169-pin grid array, the device sells for \$595 in its 100-ns version. **Advanced Micro Devices**, 901 Thompson Pl, PO Box 3453, Sunnyvale, CA 94088.

Circle 132

## CMOS FIFOs boost 40-MHz data rate

Using an HCMOS process, the 74HC/HCT40105 and 74HC/HCT7030 first-in, first-out (FIFO) registers. The parts are 4 bits  $\times$  16 words and 9 bits  $\times$  64 words. Both parts claim a typical 40-MHz burst-in/burst-out data rate without flags. Operating temperature range is -40 to 125°C. Independent shift-in/shift-out controls allow high-speed synchronous or asynchronous data transfers, while input-ready and output-ready status indicators indicate the full or empty condition of the FIFO. Both units are cascadable in depth and expandable in word width. **Signetics**, 811 E Arques Ave, PO Box 3409, Sunnyvale, CA 94088.

Circle 133

## Complex multiplier offers high precision

A DSP building block for the Complex Datapath family will multiply two complex words, each with 16-bit real and imaginary parts, every 100 ns and output the complete 32+32-bit result within a single cycle. The PDSP16116 complex multiplier contains four 16  $\times$  16 array multipliers, two 32-bit adder/subtractors and complete control logic required for high-precision DSP applications. Packaged in a 144-pin grid array, the device dissipates 1,000 mW. Price is \$586 in quantity. **Plessey Semiconductor**, 9 Parker, Irvine, CA 92718.

Circle 134

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### Real-time operating system for 80386 offers comprehensive solution

A real-time operating system for the Intel 80386 microprocessor includes the Ready Systems VRTX32/386 multitasking kernel, the RTscope 386 real-time debugger and the VRTX32 system monitor.

The kernel is a real-time executive designed for use in security applications for communications, instrumentation, aerospace, military and factory automation that must meet

strict real-time requirements. It's upwardly compatible with VRTX and completely supported by a debugger. Future plans include I/O and file management support.

The RTscope debugger monitors the VRTX32's system objects while operating concurrently with the multitasking system. It also plays a traditional debug by displaying and setting register and memory functions

for the 386. Besides performing both board-level debug and monitoring functions, the unit displays the contents of local and global descriptor tables and sets and removes 386 hardware breakpoints.

The VRTX32/386 sells for \$6,775, and the RTscope 386 costs \$3,000. **Ready Systems**, 449 Sherman Ave, PO Box 61029, Palo Alto, CA 94306.

**Circle 135**

### Integrated development toolkits available for 80386

A family of native and cross development tools offer full support for the 80386 microprocessor. The integrated toolkits are available on VAX, SUN and other 68000-based systems, IBM PC, Compaq Deskpro 386 and compatible 386-based systems. The 80386 compilers use extensive global optimization techniques and generate extremely dense code. They support two floating-point units: the Intel 80387 and the Weitek 1167. Each compiler has interlanguage calling capability. **Oasys**, 230 Second Ave, Waltham, MA 02154.

**Circle 136**

### Optimizing Pascal compiler speeds execution for 8051

The AVPAS51 3.0 optimizing Pascal compiler produces code efficiently enough to virtually eliminate the need for assembly code for the 8051 microcontroller family. The compiler's programs use all 8051 memory spaces and support interrupt handling, special function registers and internal bit operations. The compiler also includes a feature to declare individual subroutines static, thereby reducing code size and improving execution speed. Price is \$795. **Avocet Systems**, 120 Union St, PO Box 490, Rockport, ME 04856.

**Circle 137**

### Compiler speeds DSP code execution

The LSI C compiler is a complete MS-/PC-DOS facility for writing digital signal processing software in C and compiling that software into executable object code for the Texas Instruments TMS320C25 processor. The processor includes a preprocessor and linking assembler, represents a full implementation of C as defined by Kernighan and Ritchie, and supports all integer data types. Interrupts are handled using the standard C signal function, and five auxiliary registers are provided for use in assembly language routines. The compiler requires two disk drives, 512 kbytes of RAM and an IBM PC, PC XT, PC AT or compatible running MS-DOS 3.1 or later. **Spectrum Signal Processing**, Suite 301, Discovery Park, 3700 Gilmore Way, Burnaby, B.C. V5G 4M1.

**Circle 138**

### Diagrammer/formatter automates system design in Unix environments

Designed to eliminate many of the manual aspects of system design in Unix-based systems, an interactive diagrammer and code formatter lets developers build programs in the structured environment of the Warner open-brace notation and then recast the program diagram into C,

Pascal and Cobol for compilation. Called Sourceview, the development tool lets developers view documentation through their design notation. As users create, change, move, delete, expand or import components into a design, Sourceview automatically alters the design diagram to reflect the changes. It runs in all Unix environments that support the standard C library. Future versions will support MS-DOS and VAX/VMS environments. **Heartland Systems**, 1601 Kasold Dr, Lawrence, KS 66046.

**Circle 139**

### Compiler improves embedded application development

The iC-86 R4.0 is a C compiler designed for code development in Intel's 8066/186/286/386 family of microprocessors. Built-in functions maximize programming efficiencies, reduce development time and simplify maintenance. Single-unit price with preproduction libraries is \$750. Upgraded libraries will be sent to users at no extra cost. **Intel**, 3056 Bowers Ave, Santa Clara, CA 95052.

**Circle 140**

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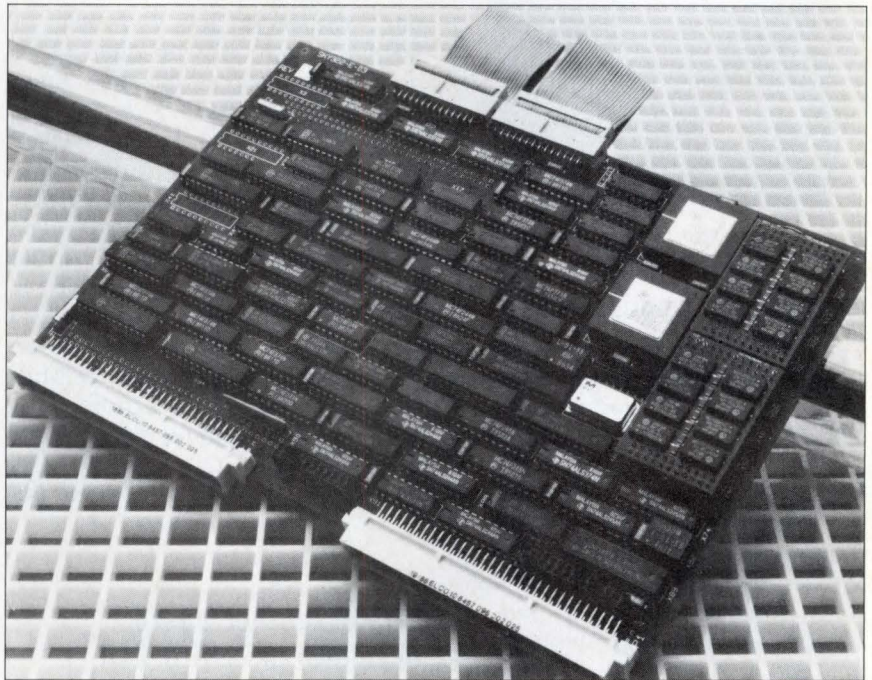


## Low-cost DSP board supports popular workstations

Delivering 10-Mips performance, the Challenger-S is a low-cost digital signal processor (DSP) for the Sun-3 family of workstations. The board is supported by a C compiler and cross development tools, relieving users of the need to program in time-consuming assembly language. A pre-processor, a 32020 assembler, a linker and a debugger are available for application development.

The board uses two Texas Instruments TMS32020 chips to address the high-speed processing requirements in applications like speech or image processing, vibration analysis, real-time control and digital filtering. The two chips are configured in a master/slave arrangement that lets the master control all operational functions, while the slave is devoted to arithmetic processing. With the board in place, the Sun-3 host can simultaneously move and process integer information with no wait states.

Available in options from 64 to 256 kbytes, on-board multiported static RAM matches the instruction speed of the processor chips. The

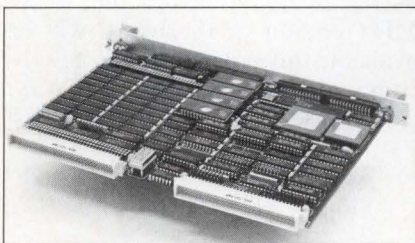


memory is mapped into the host's VME address space, letting the VMEbus and both TI chips address the memory simultaneously. A 16-bit parallel interface connects custom devices, such as analog-to-

digital converters, or links multiple Challenger-S boards.

In single quantities, the board sells for \$5,200. **Sky Computers**, Foot of John St, Lowell, MA 01852.

**Circle 141**



### CPU board adds daughter-board expandability

The V68/32 is a VMEbus board incorporating a 68020 processor at up to 25 MHz. The board also features a 68881 floating-point coprocessor, 1 Mbyte of no-wait-state dynamic RAM, 512 kbytes of EPROM and two serial I/O ports. Memory can be extended to 4 Mbytes. An I/O daughter-board interface delivers direct memory access to the on-board

DRAM and interrupt support. Daughter boards provide a VME Subsystem Bus interface, a combined SCSI/clock/printer, a 10-MFlops math coprocessor and a high-resolution graphics display. Price for the CPU board is \$1,950. **I/O**, 2430 N Huachuca Dr, Tucson, AZ 85745.

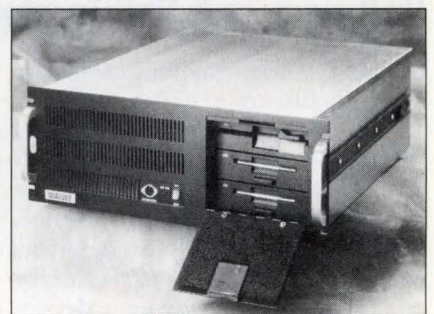
**Circle 142**

### AT-compatible computer housed in durable package

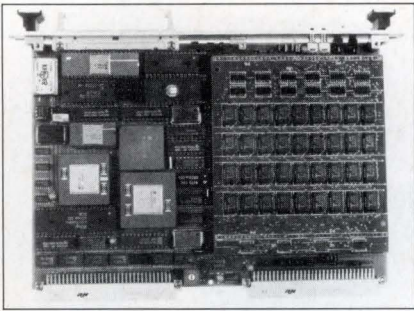
The QPC-7000 is a rack-mount IBM PC AT computer designed for rugged environments. Targeted for data acquisition, process control and distributed control, the computer fills one slot of its 12-slot backplane with the QPC-5121 single-board computer. The system features an 10-

MHz Intel 80286, 1 Mbyte of RAM, a socket for an 80287 coprocessor, a floppy controller, a SCSI Winchester controller, a serial port, a parallel port, and a clock/calendar with battery backup. It also adds a disk carrier assembly, a drive-area cover door with security lock, a system reset button and a 200-W power supply. **Qualogy**, 2241 Lundy Ave, San Jose, CA 95131.

**Circle 143**







## VME SBC suits Unix or real-time applications

The XVME-650 CPU board, built around a 15-MHz 32332 microprocessor, is equally at home in embedded, real-time control or Unix applications. Implementing full 32-bit VMEbus master/slave capabilities, the board includes an MMU, a floating-point coprocessor, 1 or 4 Mbytes of dual-ported, zero-wait-state dynamic RAM, a pair of JEDEC sites for nonvolatile memory and two RS-232 serial ports. Mailbox operations are supported. **Xycom**, 750 N Maple Rd, Saline, MI 48176. **Circle 144**

## CPU for Multibus II packs SCSI and Ethernet

The 68020-based TP23M2 SBC packs SCSI and Ethernet interfaces, a Local Bus Extension (LBX) and 16-bit single branch exchange extension bus and six serial ports on a Multibus II board. The board is available in versions for Unix and

real-time applications: the former include 4 Mbytes of dynamic RAM and a paged memory-management unit; the latter has 1 Mbyte of DRAM. Both provide dual 32-bit direct memory access channels, up to 256 kbytes of EPROM, a real-time clock, 2 kbytes of battery-backed static RAM, a pair of programmable counter/timers and, optionally, a floating-point coprocessor. The boards run a demand-paged, virtual implementation of Unix V.3 and the VRTX-32 real-time kernel and I/O extensions. A Unix-to-VRTX communications package using the Multibus II message passing protocols is also available. **Tadpole Technology**, 6747-K Sierra Ct, Dublin, CA 94568. **Circle 145**

## 80386 mother board accelerates Zenith 248

An add-on mother board for the Zenith Model 248 provides 32-bit performance and zero-wait-state operation. Available in 16- or 20-MHz versions, the board uses an Intel 80386 CPU, a Chips & Technologies chip set, an Advanced Micro Devices Basic I/O System (BIOS) and an 80387 math coprocessor. Price for the 16-MHz version is \$2,595, while the 20-MHz board sells for \$2,995. A piggyback board provides up to 8 Mbytes of 32-bit memory. **American Micronics**, 18005 Skypark Cir, Suite A, Irvine, CA 92714. **Circle 146**

## No-frills J2 VME backplane offers two power options

The P/N 024-245-01 is a low-cost, six-slot VME J2 backplane. The center row of pins on the 96-pin connectors are bussed for VME's 32-bit expansion and have shorter pin lengths (6 mm), except for the two end connectors. All other pins are 17 mm. Outside rows are left unbussed for user I/O connections. Unlike the premium series VME J2 backplanes, this solution doesn't offer auxiliary ground pins bordering each socket slot for selective signal/ground. Two power options are available: Mate-N-Lok connectors and Quick Disconnects. **Hybricon**, 12 Willow Rd, Ayer, MA 01432. **Circle 147**

## VMEbus CPU board offers balanced design

The MVME141 is a high-performance computing engine that optimizes access to external memory and peripherals to prevent I/O bottlenecks. Built around a 25-MHz 68030 CPU and 68882 floating-point coprocessor, the board includes a 64-kbyte set-associative cache, a VME Subsystem Bus interface, and a cache monitor application-specific IC that ensures cache coherency for multiprocessing systems. Pricing is \$4,122 in quantities of 100; a 30-MHz version of the board will be available this fall. **Motorola**, Microcomputer Div, 2900 S Diablo Way, Tempe, AZ 85282. **Circle 148**

## Design and Development Tools

### Software and library simplify programmable gate array use

Opening its user-programmable gate array family to a wider audience, Xilinx is supporting its 2000 and 3000 series programmable gate arrays with logic synthesis software and a TTL library. These two tools offer an opportunity for designers using traditional logic ICs to easily migrate to high-density logic devices

rather than risk custom solutions or learn a new design methodology.

Based on the Espresso program developed at the University of California at Berkeley, Xilinx's logic synthesis software offers algorithmic modifications optimized for the company's Logic Cell Array architecture. Users can specify either min-

imum logic resources or maximum performance as the primary goal in designs. Although applicable to any logic network, the software is primarily directed at designs using programmable logic device techniques. Included in the DS23 Automated Design Implementation System, the logic synthesis software is part of a



package that adds software capable of converting schematic netlists and PLD equations into a programmable gate array netlist, eliminates unused logic, and automatically places and routes programmable gate arrays. The package sells for \$1,500.

The TTL library complements the standard XACT library of over 100 counters, decoders, multiplexers, and registers. Adding over 40 common MSI functions, the TTL library is priced at \$500.

**Xilinx**, 2069 Hamilton Ave, San Jose, CA 95125. **Circle 149**

## Modeling software speeds network design

Opnet is an integrated modeling and simulation package for digital communications networks. Acting as a testbed for network protocols and architectures, the package lets users predict the effects of design and operating parameters on network performance. Models are specified graphically, and event-scheduled simulations are compiled from the models. User-specified procedures, written in C, can be linked into the simulation. Opnet offers a variety of postprocessing tools, including plotting and statistical functions, for simulation result analysis. **MIL 3**, Washington Harbor, Suite 350, 3050 K St NW, Washington, DC 20007.

**Circle 150**

## Integrated microprogram design tool speeds process

In an attempt to simplify and accelerate the design of microprogram-based systems, the Step-50 Microprogram Development System offers a set of integrated hardware and software tools that support the Microsoft Windows Operating Environment. The toolset includes a 160-bit  $\times$  4-kword-deep Writeable Control Store with 25-ns RAM devices, a real-time trace memory of 4k  $\times$  80 bits that supports an operating speed of 25 MHz, and a built-in logic state analyzer that offers sophisticated clock and breakpoint

controls with multiple trigger levels. Executing under the Windows environment, the system's operating software supports five levels of user control. An IBM PC AT or compatible acts as a user console. Step-50 also supports the company's Meta-step language system, a high-level

language definition, design, programming and debugging system for custom language development. Price for the development system without Metastep or the AT is \$15,000. **Step Engineering**, 661 E Arques Ave, PO Box 61166, Sunnyvale, CA 94088.

**Circle 151**

## SOFTWARE ENGINEERS

Northrop Corporation's Defense Systems Division develops embedded, real-time software for airborne radar and electro-optical/infrared countermeasure applications. In addition, we conduct independent research and development in software development techniques and artificial intelligence control concepts.

Emphasis is on programming in the "C" and Ada languages following a structured design methodology and supported by graphics-based interactive development tools. Our state-of-the-art software development environment is implemented on a VAX cluster configuration, running under VMS, connected to SUN workstations on an Ethernet LAN, running under UNIX. Each software engineer has a terminal or workstation providing access to all computing resources on the network.

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### Software Architects

To initiate design projects and perform requirements analyses, algorithm development, and high-level design. Requires an advanced technical degree with formal computer science training and five years experience in the development of large-scale real-time embedded software. Experience in structured design methodology in a military standards environment and exposure to knowledge-based expert-systems and object-oriented programming techniques desired.

### Software Systems Development Engineers

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### Software Tools Development Specialists

To evaluate and/or develop tools to enhance software development productivity. Requires BSCS, or equivalent, and three years experience in software tools development. Experience with the Unix operating system, bit-mapped graphics displays, graphics standards, and windowing environments desired.

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**CIRCLE NO. 44**



## VME controllers optimize Ethernet performance

Two VME controllers address high-performance processing applications by supplying linking and front-end solutions for Ethernet networks. The two boards include the LC202 Ethernet link board and the EXOS

302 Ethernet controller board.

Built around an 80186 microprocessor, the LC202 achieves link speeds of up to 9 Mbits/s. By designing the board for the link environment, the LC202 boosts perfor-

mance when running host resident protocols such as 4.2 BSD and other Unix derivatives. The on-board processor and firmware provide network management functions and an optimized path to Ethernet. Typical applications include distributed file systems such as Sun's Network File System. The LC202 sells for \$1,495.

The Exos 302 is an intelligent Ethernet front-end processor board. Using Intel's 80286 processor, it pushes performance up 70 percent over preceding boards in the Exos family, while retaining full compatibility with existing software. The board costs \$2,495.

**Excelan**, 2180 Fortune Dr, San Jose, CA 95131. **Circle 152**

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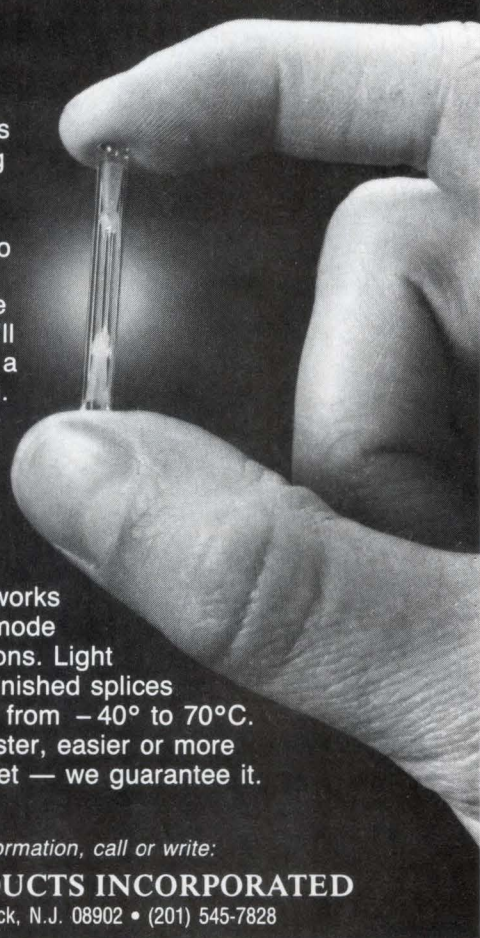
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### High-speed processor connects diverse systems

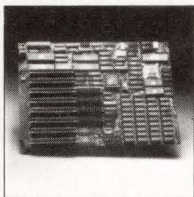
Linking a diverse collection of computers and operating systems at very high speed, the Hyperchannel-DX units let systems on a network move data at speeds up to 100 Mbits/s. The networking products handle up to eight concurrent sessions on different networks, including networks using different protocols or media. Transmission is supported on coaxial cable, fiberoptic cable, twisted-pair wire, high-speed telephone lines and global communications links. In addition, the architecture complies with Ethernet and Transmission Control Protocol/Internet Protocol and will comply with future definitions of Fiber Distributed Data Interface and Open Systems Interconnection. The Hyperchannel-DX is built around a 16-MHz 68020 processor, a 1- to 16-Mbyte shared central memory and a 400-Mbit/s backplane. The system accepts data from one system, manages buffer-memory allocation for host and media interfaces, selects the proper route for data movement and passes pointers between the various interfaces to direct traffic. **Network Systems**, 7600 Boone Ave N, Minneapolis, MN 55428. **Circle 153**

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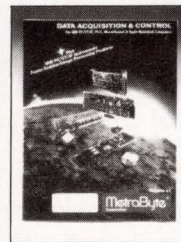
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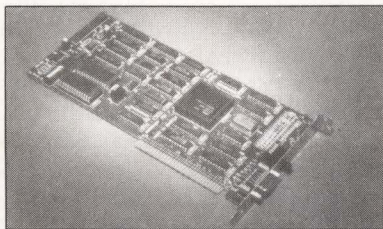
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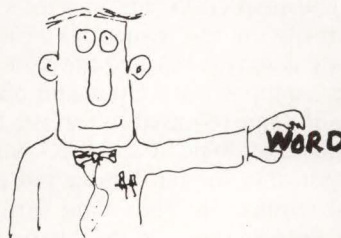


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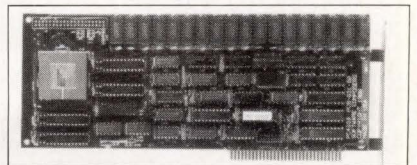
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**CIRCLE NO. 226**



A specification for a four-wire serial interface to incorporate boundary-scan cells for standard ICs and application-specific ICs is being finalized by the Joint Test Action Group (JTAG), an international ad hoc group of companies promoting standardization of design-for-testability techniques. The interface will enhance testability of printed circuit board assemblies and can virtually eliminate the need for bed-of-nails fixtures, especially critical when boards are designed using surface-mount components.

A key feature of the JTAG 2.0 standard is a four-pin implementation with a clock, a single-mode input and serial I/O lines. It also has a small state machine to decode the mode input and generate control and clock signals, and it includes serial path shifts for instructions or data. Multiple parallel data paths are available, including a bypass path and a boundary-scan path.

The JTAG, which was originated by Philips in 1985, has endorsed a proposed design-for-testability interface standard that uses the boundary-scan implementation. The interface specification has been adopted by the IEEE PLM 1149 Test Bus Standards Group as well.

## IC test architecture

When first formed, the JTAG moved in the direction of a simple boundary-scan test architecture and scan interface for support of board-level test. But as other test structures, such as hybrid components, ASICs and surface-mount technology, were identified that needed support, the JTAG expanded the original boundary-scan architecture to support these additional test structures, according to Lee Whetsel, member of the Group Technical Staff at Texas Instruments (Plano, TX) and a key technical person involved in designing the new interface for the JTAG.

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## Interface brings standardized DFT closer to reality

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*Art DeSena  
President  
ADS Associates*

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The IC test architecture interface using boundary scan adopted by the JTAG is readily expandable to accommodate other IC test structures such as built-in-self-test and internal core scan design. Development of software support tools is simplified because there's a distinct separation between instruction and data scan operations. The architecture of the four-wire interface consists of an instruction register, a data register, a 2:1 serial data output multiplexer and the JTAG interface port.

The instruction register selects and controls the test structures residing in the data register, and the data register contains the control and observation logic required to test the IC's application logic. The JTAG port is responsible for the timing and control required to shift data through the data register or the instruction register. The interface defined by the JTAG requires four dedicated test pins: a serial data input, a serial data output, a test control input (mode) and a scan clock input.

The serial data input is a unidirectional input coupled to the serial data inputs of the instruction and

data registers via the 2:1 multiplexer. The external serial data is fed into the serial data input and shifted into the selected data path, instruction register or data register during the low-to-high transition of the scan clock input. Similarly, the serial data output is a unidirectional output coupled to the serial data outputs of the data or instruction register via the 2:1 multiplexer. The serial data is shifted out of the selected data path, data register or instruction register on the low-to-high transition of the scan clock input.

Also a unidirectional input, the test control input is coupled to the control input of the JTAG port with the external serial test control input shifted into the the port controller on the low-to-high transition of the scan clock input. The scan clock input, defined as a free-running 50 percent duty cycle clock input, is a unidirectional clock and is coupled to the clock input of the JTAG port.

Satisfying the test interface requirements identified by the JTAG for boundary scan, the JTAG port design also meets the interface requirements of both the military and commercial sectors of the electronics industry. Requirements met by the JTAG port include synchronous operation, reset capability, support ring or star scan configurations, selection of data and instruction scan operations and use of a dedicated four-pin test port baseline.

Since synchronous operation is more easily supported by automatic test generation toolsets, it's preferred over asynchronous operation. The synchronous operation requirement specifies that the operation of a standard test port should be synchronous to a free-running scan clock, with the control input and the transfer of serial data synchronous to the scan clock input. To satisfy the reset capability, the test port provides a means to continuously force a reset (strap) condition on the test



logic so it will go to and stay in a reset condition. This ensures that the test logic won't inadvertently become active and impede the operation of the application logic.

The test port supports both ring and star scan configurations. In a ring configuration, multiple ICs are interconnected serially on one continuous scan data path so that the primary scan interface shifts data through the scan path to access one or more of the ICs in the ring. In a star configuration, multiple ICs are interconnected so that one can be directly accessed by the primary scan interface. To satisfy the selection of data and instruction scan operations, the test port can efficiently direct scan data through the instruction or data register scan paths.

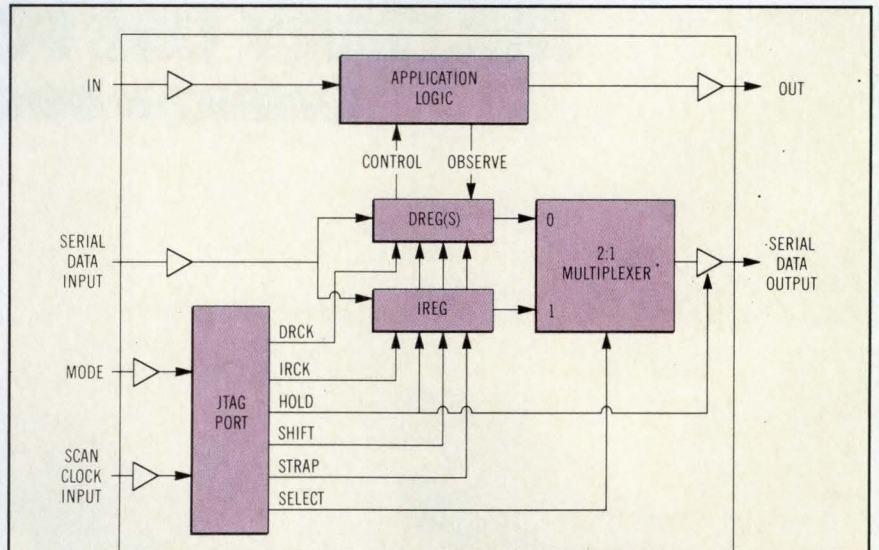
The dedicated four-pin baseline lets scan operations occur concurrently with normal operation of the IC and simplifies the bus interconnect. An advantage of the four-pin baseline is that the package size increases only to the next package size when a standard part is retrofitted with boundary scan.

#### Port meets interface needs

Requiring two dedicated inputs, a scan clock input and a test control input, the JTAG port is a state machine design that decodes a stream of serial bits (serialized commands) entering the JTAG port through the test control input. The decoding takes place during the low-to-high transition of the scan clock input.

Responding to the serialized test control command inputs by activating its internal control outputs, the JTAG port sends control signals to the instruction and data registers.

These controls consist of an instruction register scan clock, a data register scan clock, and hold, shift, select and strap commands. The instruction register scan clock transitions with the scan clock when enabled, and the first low-to-high in-



The JTAG standard 2.0 serial interface for testability consists of an instruction register (IREG), a data register (DREG), a 2:1 serial data output multiplexer and the JTAG port. Consisting of a four-pin implementation with a clock, a single test control (mode) input and serial input and output lines, the interface also has a small state machine to decode the mode input and generate control and clock signals.

struction register scan clock transition preloads the instruction register, while the second and subsequent low-to-high instruction register scan clock transitions cause the instruction register to shift. The data register scan clock also transitions with the scan clock when enabled and preloads the data register with the first low-to-high data register transition. Similar to the instruction register scan clock, the second and subsequent low-to-high data register scan clock transitions cause the data register to shift.

The hold command is an active low output from the JTAG port that forces the boundary and instruction register output latches to hold their present state during shift operations and also enables the serial data output tristate buffer when active low. The shift command is an active high output from the JTAG port that puts the boundary or instruction register into shift mode. The select command output from the JTAG port

selects the output of the instruction register (if select is high) or the data register (if select is low) to be connected to the serial data output buffer. The strap command is an active low output from the JTAG port that forces the test logic into a reset mode that doesn't interfere with the operation of the application logic.

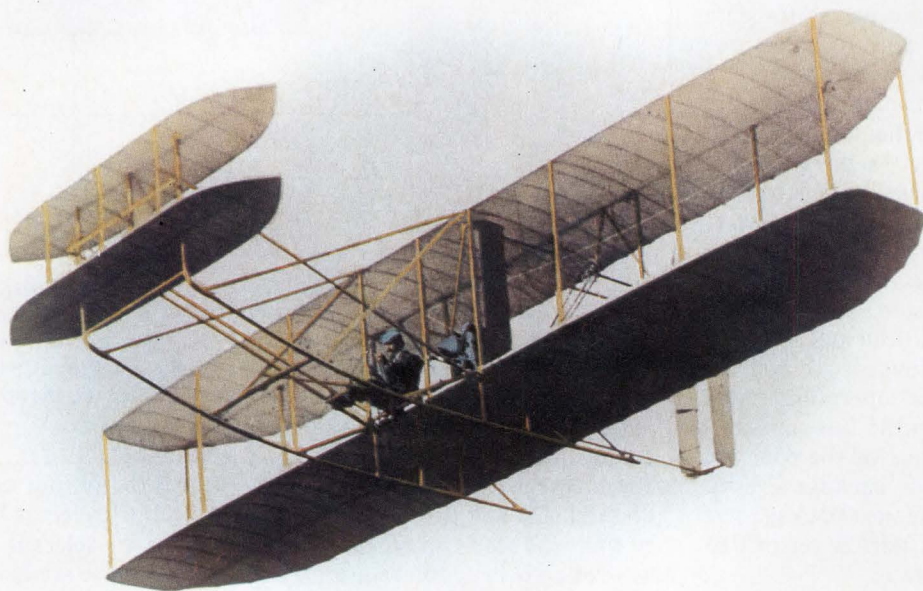
During operation, the JTAG port goes through various states and always returns to the strap (reset) state if the test control input is high, which satisfies the requirement of forcing a reset condition on the test logic through the interface port.

The JTAG port meets the needs of a serial test interface, and the architecture is flexible enough to support test structures ranging from simple boundary scan to the sophisticated maintenance and support structures required in military electronic systems. Support is growing for the JTAG port and architecture, and some companies already plan to install the port in new IC designs. **CD**



**"WITH THE EXCEPTION  
OF OBSERVATION, I SEE NO  
MILITARY USE FOR IT."**

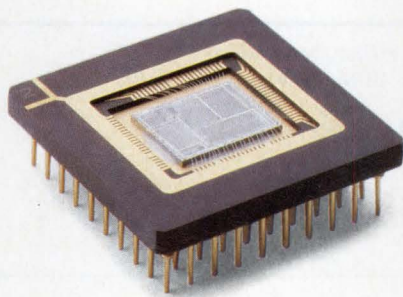
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