A PennWell Publication

OCTOBER 15, 1984

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

DIGITAL SIGNAL PROCESSING

CONTROLLER
DISK INTERFACING

DISTRIBUTED MICROS BOOST POWER OF TEXT/GRAPHICS SYSTEMS

STD BUS BOARD CUTS DATA ACQUISITION COSTS

IN OUR MEMORIES.

NEC
NEC Electronics

CIRCLE 1

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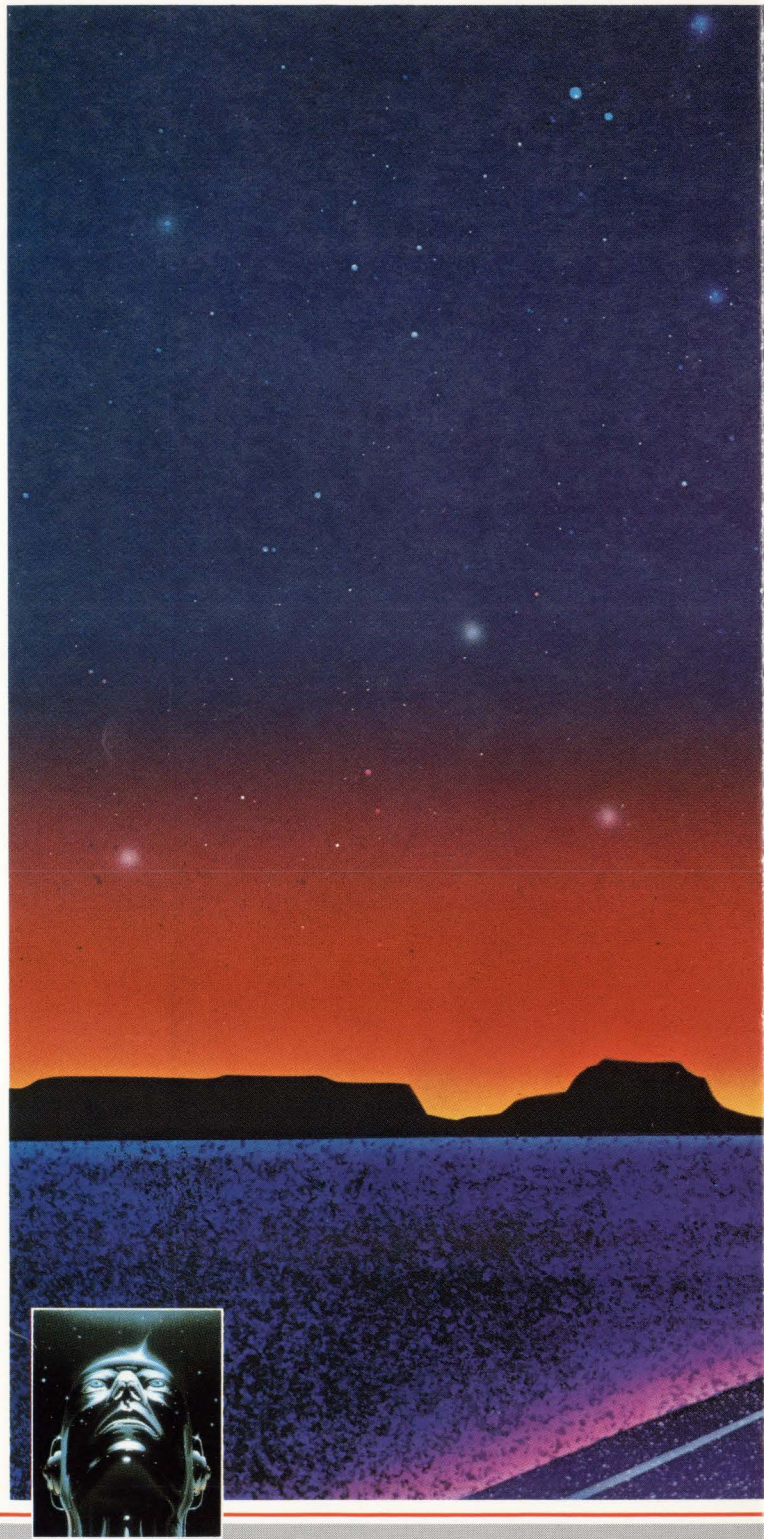
Static RAM[2]	•	•	•						•		•			
Dynamic RAM		•	•						•		•		•	
ROM	•		•							•	•	•	•	•
PROM				•	•		•	•	•					
EEPROM			•						•					
UV EPROM	•		•						•	•	•	•		

[1]MMOS refers to Mixed-MOS technology (CMOS and NMOS).
[2]High speed 4K and 16K devices available.



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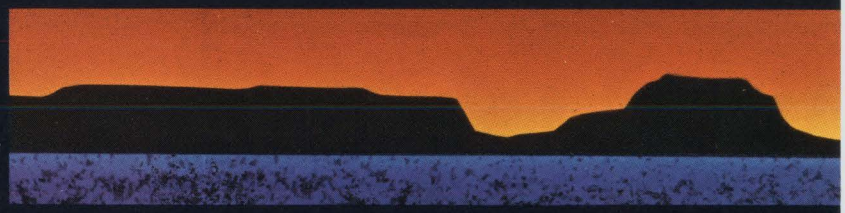
MEMORIES OF THE FUTURE



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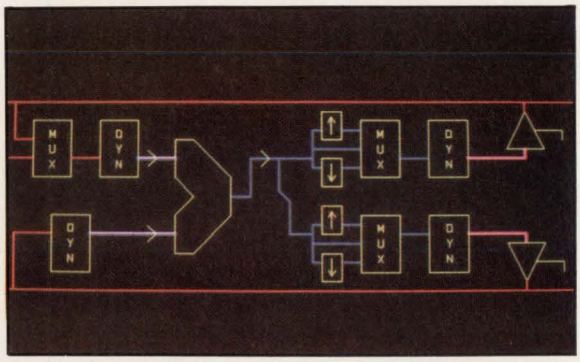
CIRCLE 2

COMPUTER DESIGN®

This month's cover was designed and created by Mary Codd and Steve Branch at Coddbarrett Associates, Inc. It was illustrated by Steve Branch and based on an idea from Advanced Micro Devices.

SPECIAL REPORT ON DIGITAL SIGNAL PROCESSING

SYSTEM TECHNOLOGY



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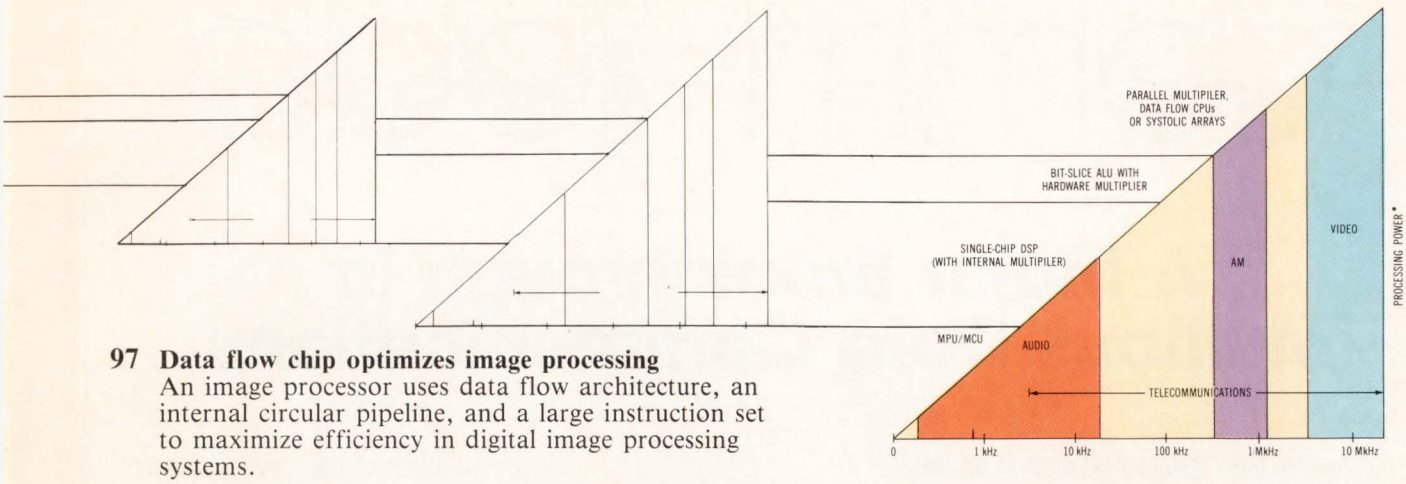
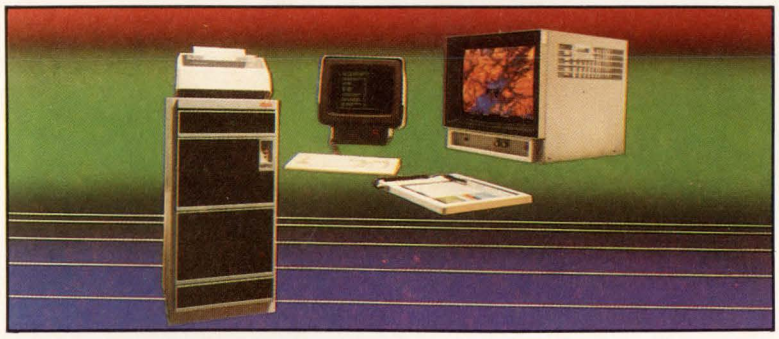


SYSTEM COMPONENTS



DEPARTMENTS

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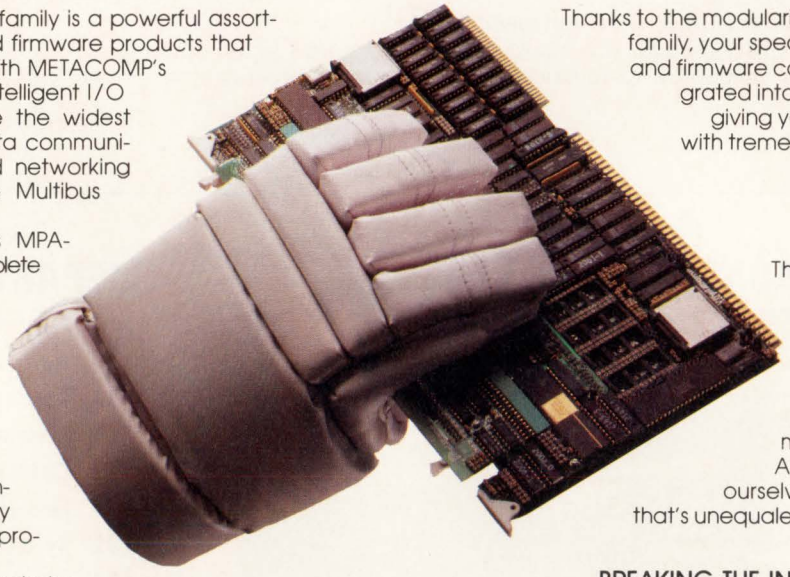

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THE MULTIBUS BREAKTHROUGH PEOPLE

CIRCLE 3

UP FRONT

Intergraph workstation joins the 32-bit list

The 32-bit workstations announced by Tektronix (Beaverton, Ore) in September will have competition. Intergraph (Huntsville, Ala), is also introducing a 32-bit Unix-based workstation for computer aided design/computer aided engineering applications. In addition, the Intergraph workstation—Interpro 32—can be used as a personal computer when running an MS/DOS. It can also be a terminal emulator, and functions as a Digital Equipment Corp DT200, Tektronix 4014, or IBM 3270 Series terminal. Interpro 32 has a 15-in. color monitor with 1184- x 884-pixel resolution. Price tag is approximately $20,000 per workstation.—*R.G.*

Team work speeds integration of design and debug tools

The union of designing and testing will move ahead as more makers of digital test tools join forces with workstation vendors. For example, Dolch Logic Instruments' (San Jose, Calif) recent unveiling of its CAESAR—short for computer aided engineering system analyzing resource—might not have drawn attention if it had not been coupled with the announcement of the firm's joint technology agreement with CAE Systems (Sunnyvale, Calif). Under the agreement, Dolch will provide its CAESAR tools (a variety of in-circuit emulation, logic analysis, and pattern generation hardware developed for Dolch's Atlas logic analyzer system) to CAE Systems on an OEM basis.

Since Northwest Instruments (Beaverton, Ore) announced an OEM agreement to supply its μAnalyst logic analyzer to its Beaverton neighbor, Mentor Graphics, such workstation vendors as Valid Logic, Daisy, and CAE Systems have been scurrying around for suppliers of similar tools. The two major makers—Hewlett-Packard (Palo Alto, Calif) and Tektronix—would have no reason to strengthen competitors who will make the same kind of integrated design and test systems.

As a result, the candidates for joint agreements or acquisition are not many. Gould's Biomation/Millenium group of Santa Clara, Calif is an obvious possibility, but that firm is having problems keeping up with the competition and is looking at disappointing sales. An OEM agreement with a major workstation vendor would give it a shot in the arm, however. With Northwest Instruments already linked to Mentor (and developing a high channel count pattern generator expressly for Mentor), it is out of the running. An even closer link between Northwest and Mentor in the near future would be no surprise. One remaining candidate appears to be Nicolet/Paratronics of Fremont, Calif teamed with Applied Micro Systems (in view of the latter's recent acquisition by Nicolet). The two have had a relatively close and informal relationship for more than two years to promote an inexpensive system based on Paratronics' logic analyzer and Applied Micro Systems' emulator. Another possible candidate, Hilevel Technolgoy (Irvine, Calif), is known for its Emulyzer product. This firm is hot at work developing a pattern generator, and exploring the possibilities of acting as an OEM supplier of logic analysis, emulation, and pattern generation tools—*J.M.*

UP FRONT

Tektronix throws monkeywrench at Northwest

Dark clouds may be looming on the horizon for Northwest Instruments and in turn, for Mentor Graphics. The growth of several Beaverton-based design and test tool companies has been stoked with Tektronix alumni. Tektronix has treated its graduates with benign neglect because they did not present direct competition. But Tektronix has just filed suit against Northwest Instruments to restrain its new vice president of engineering, James Cavoretto, from (presumably) taking up where he left off at Tektronix. Since Cavoretto was involved with the company's oscilloscope effort, Tektronix' suit does not make sense. It appears to be a warning of Tektronix' future action, allowing the company to keep its integrated designs and test tool plans under wraps a little longer. Some key Tektronix people have joined the competition in this area, including Larry Sutter, president and CEO of Northwest (from Tektronix Design Automation Div) and Peter Strong, the new group vice president for test and measurement at Gould's Biomation/Millenium organization, also from Tektronix' design and automation group.—*J.M.*

Converter chip marries 80286s to 8088s

Designers of PC AT compatible systems, as well as those designing 80286 expansion boards for the standard PC, face a time-consuming technical problem—how to control slow 8-bit circuitry with a fast 16-bit processor. Help may be on the way. The EL-286-88 processor converter chip from Edsun Labs, Inc (Wayland, Mass) is an application-specific VLSI IC that converts 80286 processor signals into the equivalent signals of an 8088. It solves the bus interfacing problem by allowing an 80286 to drive circuitry design for the 8088 and will, according to the manufacturer, save the designer up to 9 months of product lead time. The EL-286-88 is scheduled to appear in Jan 1985, but a board version will be available to OEMs in Nov 1984 for prototyping—*J.H.*

Opening up ARCnet for the PC deluge

A line of products just announced by Datapoint Corp (San Antonio, Tex) includes a networking package for the IBM PC, a direct ARCnet interface for Datapoint's Vista-PC system, and a CP/M software support package for the ARCnet. The PC connection package is based on an Intelligent Network Executive interface card that connects to the PC. Card and software are priced at $770. Datapoint was one of the first into the local area network fray, and first to offer LAN functions on a chip, via the ARCnet VLSI controller from Standard Microsystems Corp, (Hauppauge, NY). Claiming 6000 installed LANs, Datapoint can win a numbers game with any LAN vendor. But offering connection for PC-DOS and other environments—in essence opening up its formerly proprietary network—has become a prime goal for this manufacturer.—*J.V.*

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ELECTRONICS MAKES THE DIFFERENCE

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CIRCLE 4

UP FRONT

Touchscreen computers tie to IBM PCs via an Ethernet

Up to 50 networked Hewlett-Packard (Palo Alto, Calif) Touchscreen computers and IBM PCs now can share such peripherals as ThinkJet and LaserJet printers through a local area network provided for HP by 3Com Corp (Mountain View, Calif). Dubbed EtherSeries/150, the LAN requires that at least one Touchscreen computer with a 15-Mbyte hard disk (Touchscreen MAX personal computer) to act as a file server. Each server can accommodate from two to eight users. EtherSeries/150 consists of four elements: EtherLink accessory board for accessing Ethernet; EtherShare/150, for allowing multiple users to share data and fixed disks; EtherPrint/150 for sharing printer facilities; and EtherMail/150 for providing fast electronic mail service. In addition, HP has expanded its mass drive offering to include double-density, double-sided 3½-in. drives for a total storage capacity of 1.4 Mbytes.—*N.M.*

Waiting in the wings...a Brown Trout

Industry watchers have stepped up the scan rate in anticipation of the debut of a new high end processor from IBM. Much speculation has surrounded this machine series. Some believe this "Sierra" series will be delayed some six months beyond its previously expected January arrival because of the lack of aggressive high end competition. Others say that this is contradicted by recent price reductions in the 3080 line—usually a sure sign of imminent unveiling. In any event, it is anticipated that when the machine is unveiled, it will come in within the $200,000/MIPS window. The first introduction in the series should provide 28.5-MIPS performance. Code-named Morgan, or Brown Trout, the dual-processor machine will act as a pivotal point for the series, with further announcements to come in on both the upper and lower performance sides.—*P.K.*

Artificial intelligence for the masses

Texas Instruments (Austin, Tex) is about to enter the artificial intelligence field with a dedicated Lisp processor for symbolic processing applications. The TI "Explorer" establishes new ground in price and size at the low end of the market. Explorer is NuBus-based and is a result of collaboration between TI and LISP Machine, Inc (Culver City, Calif). It is software-compatible with LMI's Lambda series machines. The microprogrammed 32-bit Lisp processor has 16- x 56-kbits of writable control store and a tagged architecture. Along with the Lisp compiler, numerous program development tools and toolkits are to be either provided or are already available.—*J.B.*

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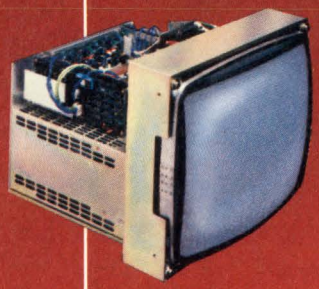

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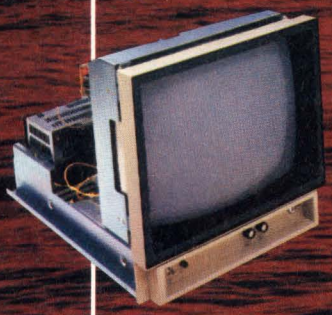

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CIRCLE 7

FEEDBACK LOOPS AND QUALITY CIRCLES

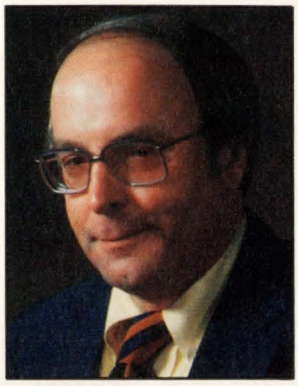
Most comparisons of Japanese and American management styles concentrate on the differences—as I did in my editoral, "Wa versus the Gunslingers" (*Computer Design*, Oct 1983, p 11). However, the real secret of the Japanese and Silicon Valley miracles may lie in a single feature that characterizes the most successful high technology companies. No matter where they are located, the best companies seem to have effective communication between management and the people in various departments and plant locations. This, in turn, leads to a common bond of trust within the organization and to a unified sense of purpose and direction.

In a small entrepreneurial company, internal communication occurs naturally because the founders begin with a common purpose and a small group of employees at a single location. As the organization grows, however, communication breaks down because people start to pull in different directions. It then becomes necessary to restore communication via some strategy such as the Japanese "quality circles."

When scanning a recent issue of the *Quality Circle Digest* recently, I was surprised to learn that about one million U.S. employees are already involved in quality circles or other problem solving groups. Until I read that, I had a lukewarm interest in the concept. To begin with, the topic of quality control—though important—tends to be boring. Also, I have an inherent distrust of organizations run by "facilitators and coordinators" because they usually turn out to be excessively bureaucratic. What finally aroused my curiosity, however, was a Quality Circle Institute survey of U.S. quality circles. This survey revealed that the major benefits of these groups were improved communications, teamwork, morale, and attitude—in addition to the expected quality and productivity benefits.

Once my interest was stirred, I became aware of other proponents of similar management styles. A source that convinced me that I had stumbled upon something significant was the testimony of Charles E. Sporck, president and CEO of National Semiconductor Corp. In his address to a local hearing of the Joint Economic Committee of the U.S. Congress held in Sunnyvale, Calif, Sporck described how his company had instituted a Quality Enhancement Strategy program (QUEST), which involves "techniques that somewhat resemble quality circles."

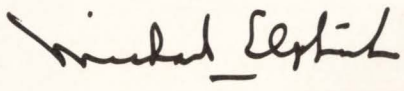
The QUEST program is not the only strategy National uses to encourage employee communication and involvement. Open offices, with shoulder-high, movable partitions and no doors, focus on the essentials for doing the job rather than nonessential trappings. "Answer line" forms placed throughout the buildings allow any employee to send managers direct, confidential messages and receive prompt responses.



National's Santa Clara, Calif headquarters has a closed-circuit television network that allows Sporck to speak directly to employees about key issues and give immediate answers to questions. Also, Sporck says that when serious issues affecting the company are in the news, National sends letters to each employee's home. All this is in addition to Sporck's regular talks to large groups and frequent informal breakfast or dinner meetings with small groups of employees.

Of course, these strategies are not unique to National. In fact, most of the successful computer and semiconductor companies I have visited—especially those in Silicon Valley and on the Route 128 belt around Boston—have similar programs to ensure communication. Perhaps where Sporck differs from other high technology managers is in his giving such high priority to communication versus other strategies for innovation. He explains, "If I were to isolate the human factor for this analysis, and boil it down to one essential element, it would be the necessity to establish trust with employees. On that foundation of trust, the rest of the business structure can be built. Trust means there is a common understanding and agreement about the mission of the enterprise. That is achieved through continual communication. . . with a significant level of participation from employees in the definition and execution of that mission, and with employees sharing the results of the success of that mission."

[To learn more about quality circles and to get a copy of the magazine, call or write Janice Minch, Circulation Manager, *Quality Circle Digest*, PO Box Q, Red Bluff, CA 96080-1335. Tel: 916/527-6970 ext 103.]



Michael Elphick
Editor in Chief

MEET THE STRONGEST

here's a lot more to a Fujitsu gate array than glass, gold, and aluminum; it's the human element that really sets our product apart.

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That's how you get numbers like these:

CMOS

TECHNOLOGY	GATE LENGTH	PROP DELAY TIME*	GATE COUNT
STD CMOS	3.6 μ	7.0 ns	700-3900
H CMOS	2.8 μ	5.0 ns	440-3900
VH CMOS	2.3 μ	2.5 ns	2600-8000

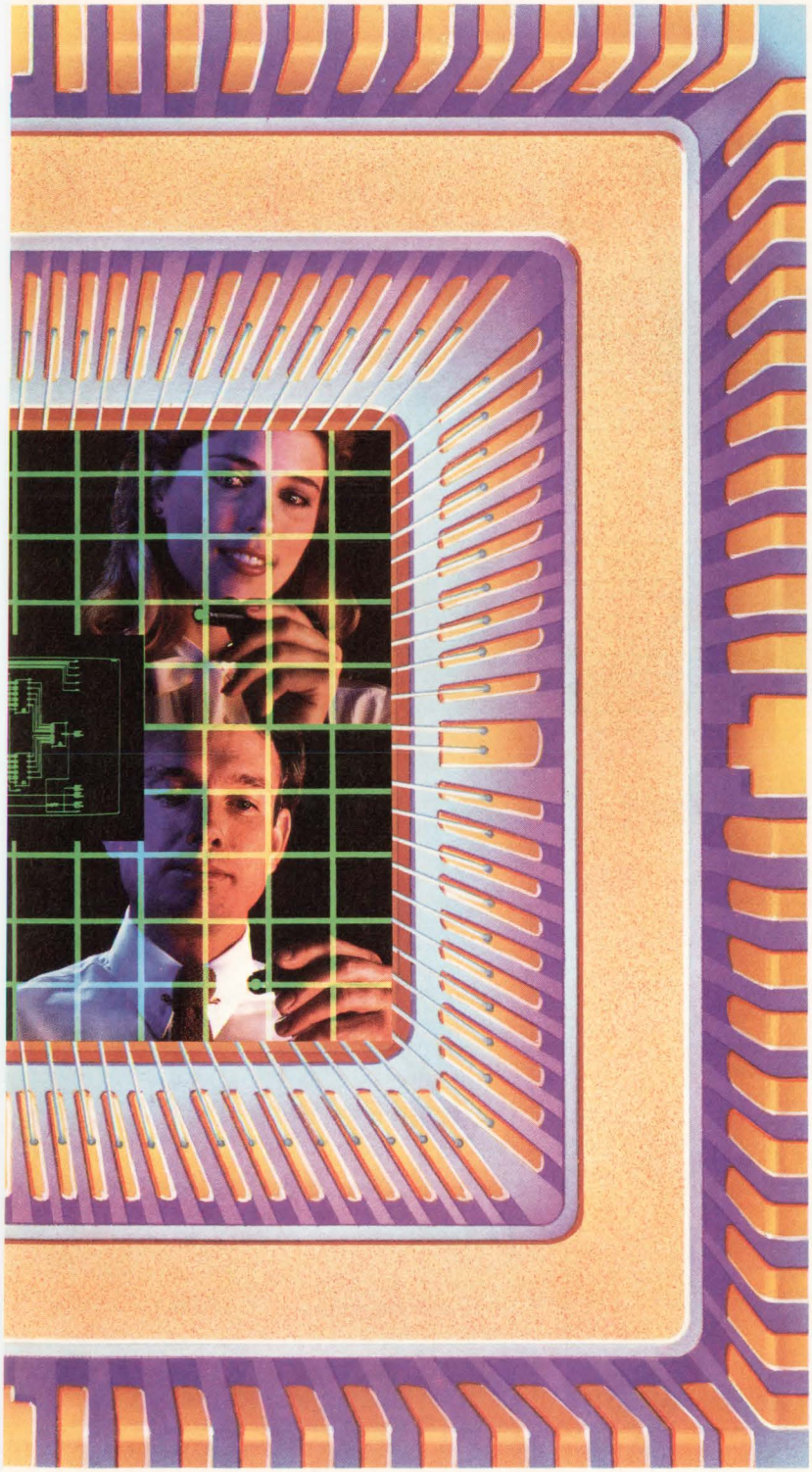
*2-Input NAND Gate, F/O = 2

BIPOLAR

TECHNOLOGY	PROP DELAY TIME*	GATE COUNT	POWER DISSIPATION PER GATE
LSTTL	1.8 ns	500	2.3 mW
LSTTL	1.9 ns	240-1100	0.8 mW
LSTTL	0.95 ns	2000	0.65 mW

*3-Input NAND Gate, F/O = 1

TEAM ON THE CIRCUIT.



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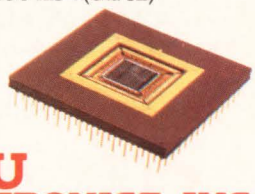

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CIRCLE 8

COMPUTER DESIGN

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CIRCLE 9

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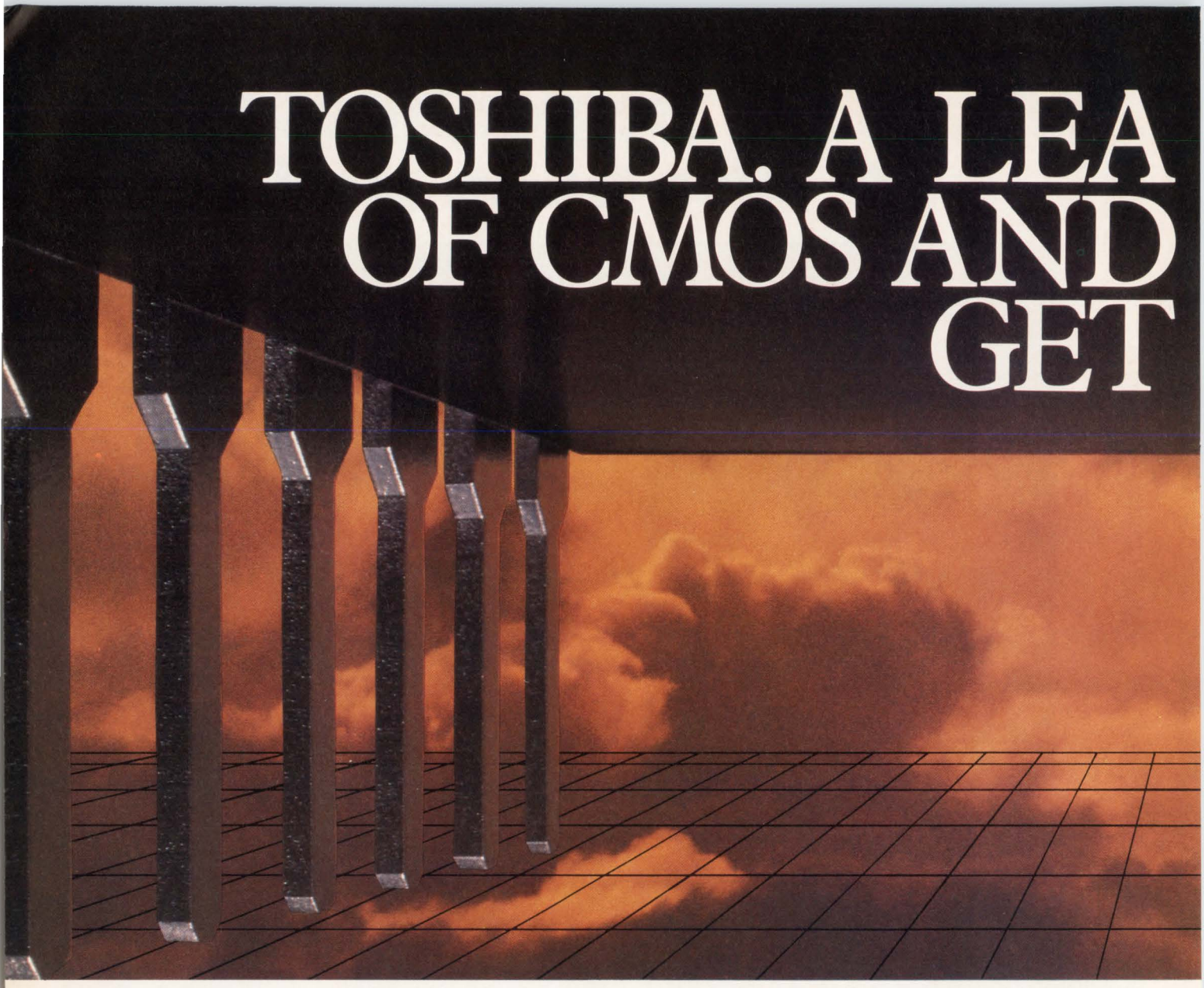

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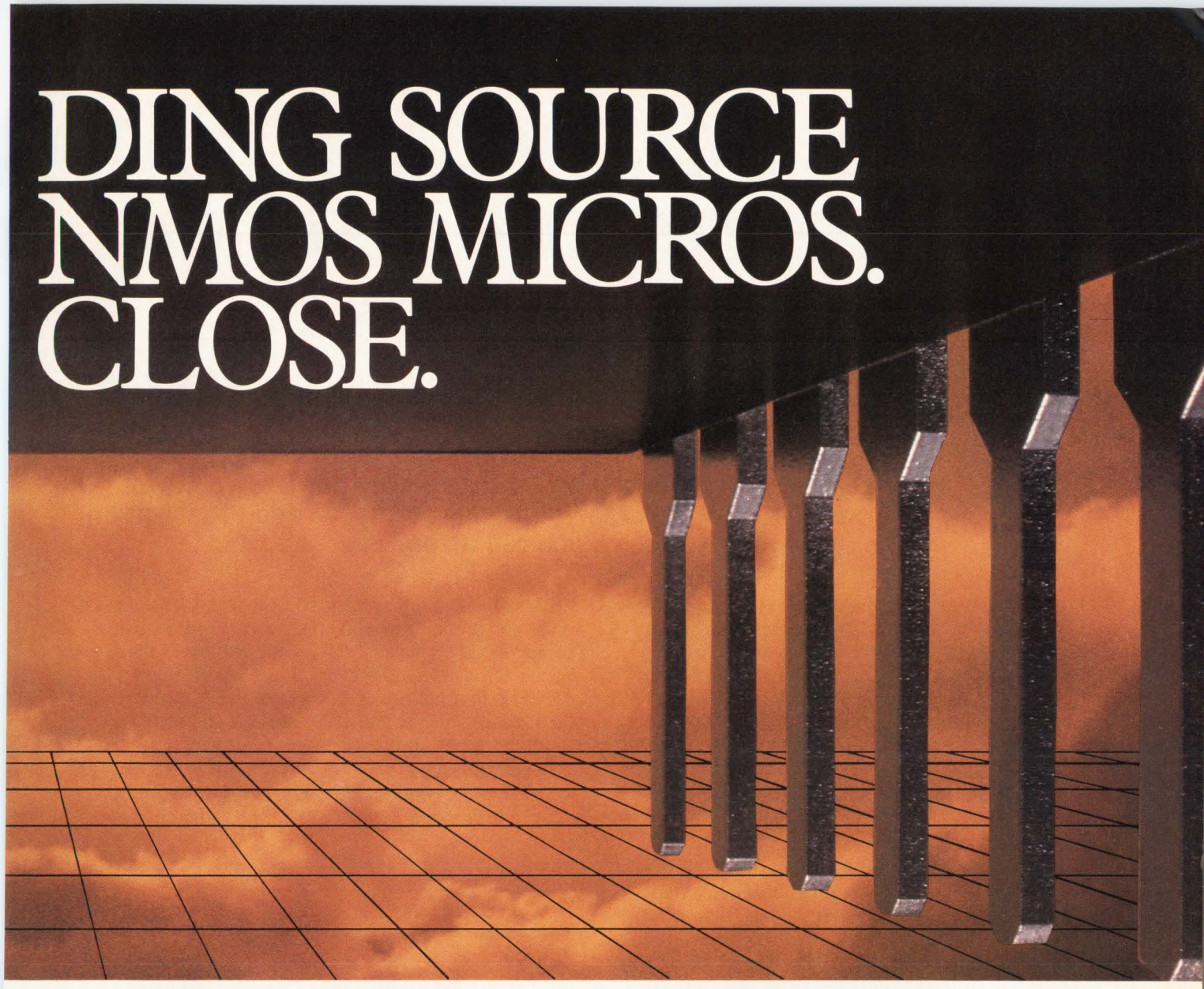

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Device	Technology	ROM (Bytes)	RAM (Bytes)	Speed	Operating Current (Max)	Standby Current
TMP8048	NMOS	1K	64	6MHz	135mA	15mA
TMP80C48	CMOS	1K	64	6MHz	10mA	10μA
TMP8049	NMOS	2K	128	6MHz/11MHz	170mA	50mA
TMP80C49	CMOS	2K	128	6MHz	10mA	10μA
TMP80C50	CMOS	4K	256	6MHz	15mA	10μA

8-BIT MICROPROCESSOR—CMOS Z80A FAMILY

Device	Description	Technology	Operating Current	Power-Down Current
TMPZ84C00	4MHz Z80A CPU	CMOS	15mA (@ 4MHz)	10μA

Also available are the popular Z80 peripherals in CMOS including P I/O, CTC, CLOCK, DMA & S I/O.

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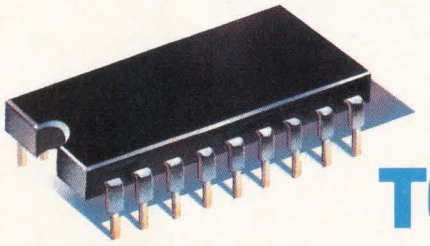

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CIRCLE 11

In 64K DRAMs, INMOS high performance and flexible ...including 8K x 8.

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8K x 8 — The cost and space saver. This newest member of the INMOS 64K DRAM family, available in a plastic package, offers access times of 120 and 150ns. The by-8 organization is a natural for microprocessor designs and other applications that require word width rather than memory depth...in process controllers, intelligent terminals, and buffer memories for example. And its pin 1 refresh makes it a very attractive alternative to 8K x 8 static RAMs. Because it combines low power and low cost with minimal support circuitry.

16K x 4 — The performance chip. With 100, 120, and 150ns access times, this organization makes a lot of sense in high-performance systems, such as high-resolution graphics, where high data rates are required. Packaged in plastic DIPs, the IMS2620 also gives you the right combination of cost, organization, and speed for microprocessor systems, terminals, and even arcade and home games. If you're upgrading from 16K x 1 chips, it provides a factor of four reduction in chip count. And its "$\overline{CAS}$ before $\overline{RAS}$" refresh assist function minimizes required support circuitry for cost and space savings.

64K x 1 — The big-system choice. This DRAM also gives you a choice of 100, 120, and 150ns access times. What's more, it includes "Nibble Mode," which allows effective cycle times below 85ns. Available in a variety of packages, including plastic DIPs, ceramic DIPs, and chip carriers, it's ideal for systems requiring lots of memory depth.

Check the chart. You'll find the industry's broadest family of 64K DRAMs...and the right device for your requirements. Then call an INMOS distributor for all the details.

Organization	Access Time (ns)	Cycle Time (ns)	Part No.
8K x 8	120	190	IMS2630-12
	150	240	IMS2630-15
16K x 4	100	160	IMS2620-10
	120	190	IMS2620-12
	150	240	IMS2620-15
64K x 1	100	160	IMS2600-10
	120	190	IMS2600-12
	150	230	IMS2600-15

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CIRCLE 12


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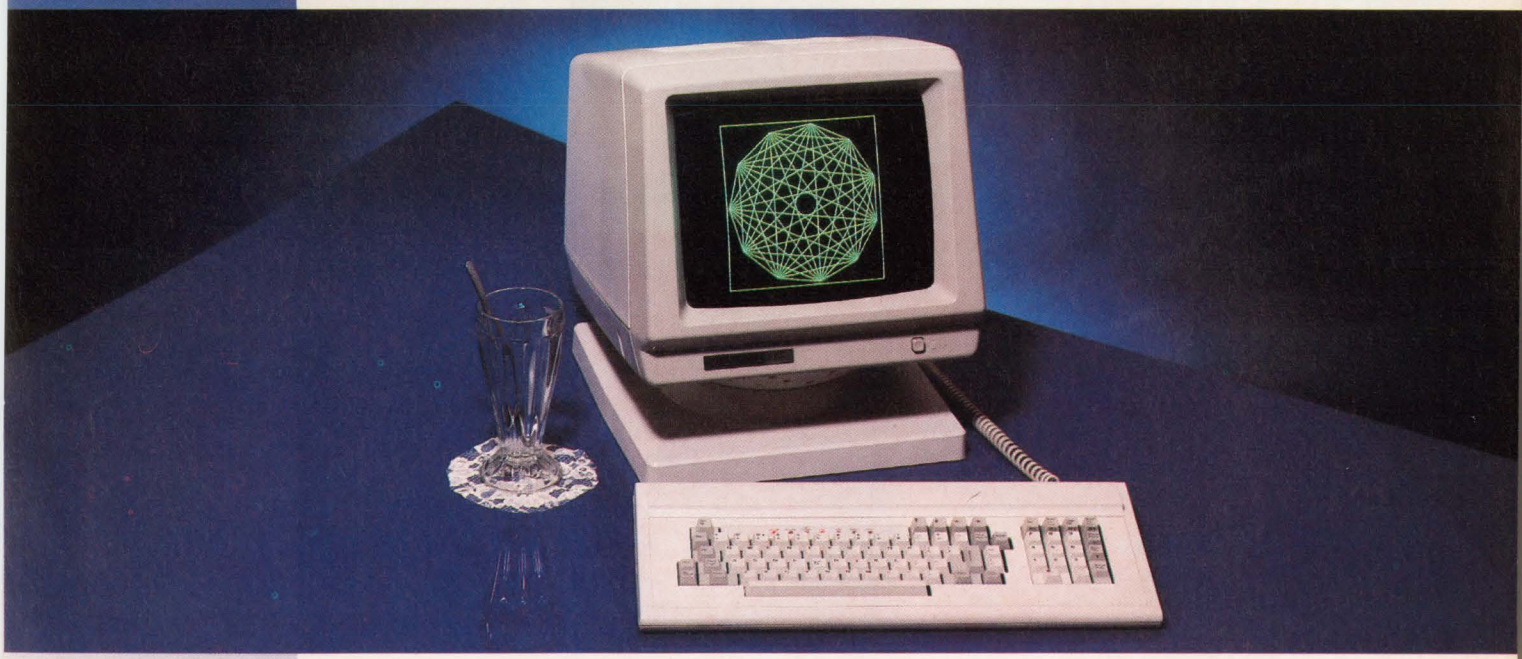

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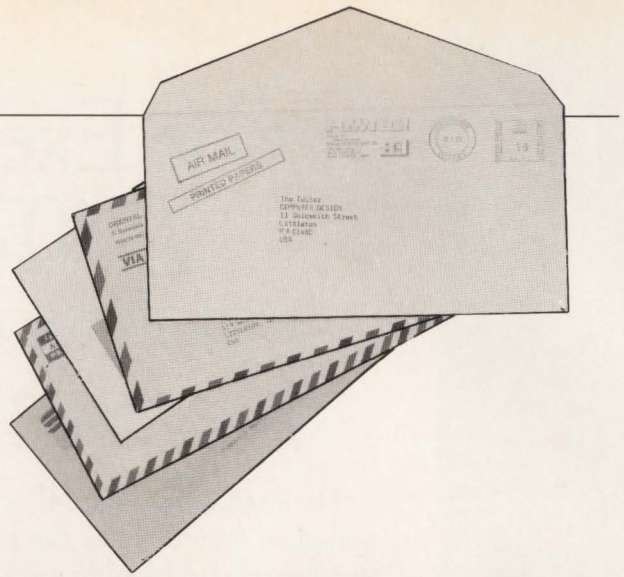
PEACE OF MIND TECHNOLOGY

CIRCLE 13

LETTERS TO THE EDITOR



Where were you?

Reading your editorial of August 1984, I wonder if we went to the same National Computer Conference. The temperature was indeed 110 degrees, but I did not notice any undue stress. In fact, I was still able to wear my suit all day (it is my office and I am lost without the pockets) and still remain comfortable. My second comment is, with all those free shuttle buses, why did you need to take a cab anywhere? I brought my wife along to Las Vegas and we went to shows in the evening, notably Gallagher, and were able to walk to the many attractions on the Strip near our hotel. After the fiasco at NCC in Anaheim, I would think Las Vegas would have been thought a blessing. Everything seemed to go quite well there this year. I believe the "Great Olympics Scare of '84," of course, had something to do with lessened travel in general, but was not a factor in the lower attendance at NCC.

To be frank, in your editorial there was no reference to what you consider more tolerable. Did you mean better climate, better facilities, less expensive accommodations, or what? Maybe we should have an NCC East and an NCC West. I do not have answers, but would be interested in other observations.

Richard Rorex
Ampex Corp
200 N Nash St
El Segundo, CA 90245

Yes, we did go to the same National Computer Conference, and I agree with Mr Rorex that the show itself was quite well organized—especially when compared to last year's Anaheim fiasco with the overheated tents and the converted basement of the Disneyland Hotel. However, members of the trade press are expected to attend all sorts of other functions scattered throughout the city, in addition to the conference. That is why I directed my criticism primarily at the city of Las Vegas and not at the NCC organizers.

The windstorm and power failure occurred just after I arrived at a press reception in the Hacienda casino. One of the more serious cab problems occurred after a business luncheon at a restaurant called The Library. Like Mr Rorex, I did use the shuttle buses whenever possible, and they were much more plentiful than at the Interface Conference earlier in the year. I heard that at that conference, the city restricted the number of shuttle buses to appease the cab fleet owners.

Like Mr Rorex, I do not claim to have all the answers. Perhaps, however, if we compare our experiences and state our personal priorities, the organizers will learn how to please more of the people more of the time. And, we may be able to accelerate the learning process if—as proposed in my editorial—we start to vote with our feet. Incidentally, AFIPS still has not announced the official attendance figures for NCC, so one can only assume that they were embarrassingly low.

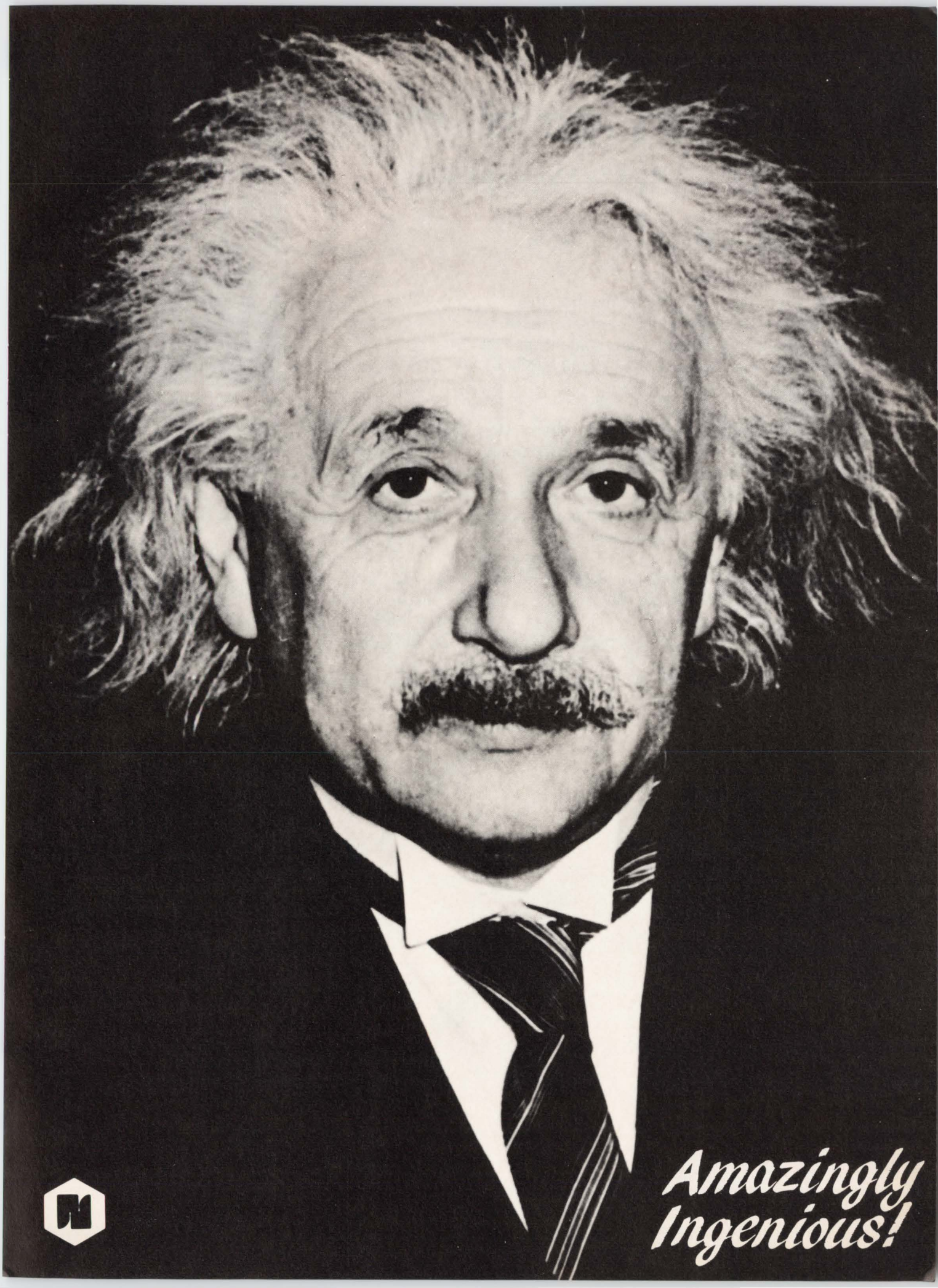
Michael Elphick
Editor in Chief

Reader comment

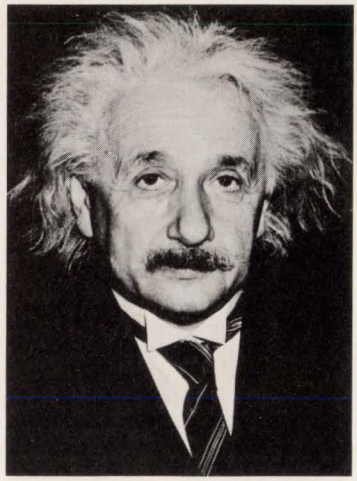
Congratulations on an excellent June 15, 1984 issue. I have browsed/read six articles, and they all scored "high" value to me. Outstanding! I only regret that there is generally so little time to learn and read.

I'm passing on my *Computer Design* magazine to a number of colleagues. Eventually, it lands in the local library of my technology group.

Bjorn T. Cronhjort
Ericsson Information Systems AB
Bromma Sweden


Amazingly
Ingenious!

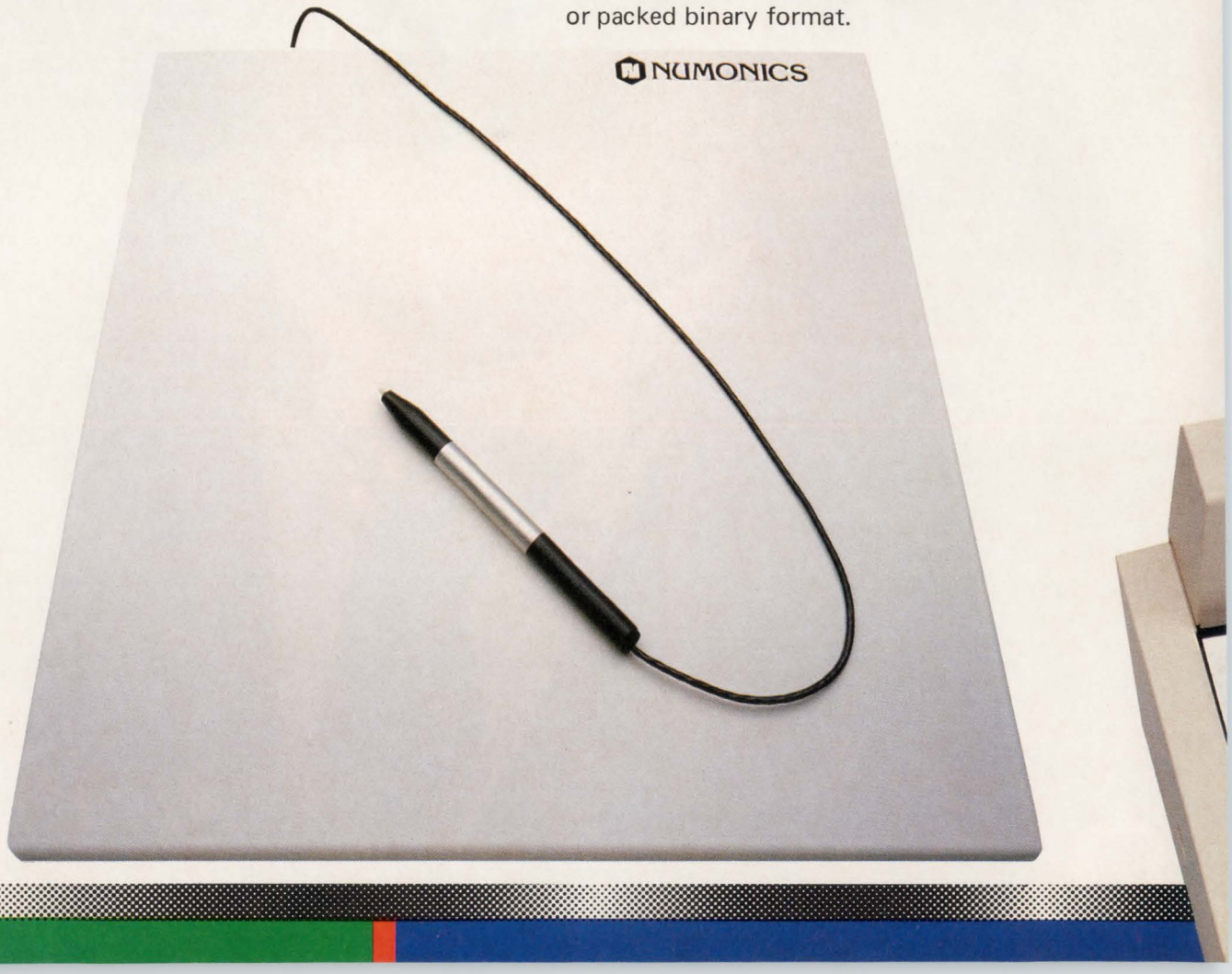
"Frankly, gentlemen, their capabilities astound me."

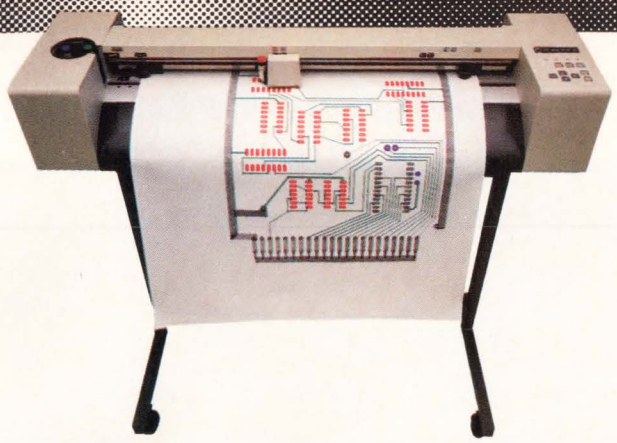


"Thank you, sir. We'd like to mention their reliability as well; Numonics is rather famous for that. And their high resolution. And the flexible range of sizes and capabilities. Would you like to know more?"

The # 2200 Tablet has a user-specified resolution as high as .001", with standard features including versatile firmware for self diagnostics, HOST override of switch-settable functions, and matrix menuing. It operates in six programmable modes: point, stream, switch-stream, incremental, polled, or timed, and interfaces in RS232, IEEE, or byte parallel, with packed binary or standard format. Sizes range from 6" x 6" to 36" x 48".

The # 2210 Tablet is a simplified version of the 2200 and also comes in sizes from 6" x 6" to 36" x 48" and, like the 2200 all sizes have identical control electronics. A single card works for all. It digitizes up to 200 points per second, in the 6 programmable modes. It accepts down-loads for changing default operating conditions. Standard pen; optional 1, 4 or 16 button cursors. This low-profile, self-diagnostic tablet interfaces with RS232, IEEE, or byte parallel, in standard or packed binary format.





The # 5424 Plotter with stand, also uses the grit-roller system, is a lower cost, single pen plotter that accepts non-sprocketed cut-sheet paper or mylar, 22" to 24" wide. Plots at almost 6" per second, is extremely accurate and has a similarly comprehensive command structure. It is designed and constructed for high durability.

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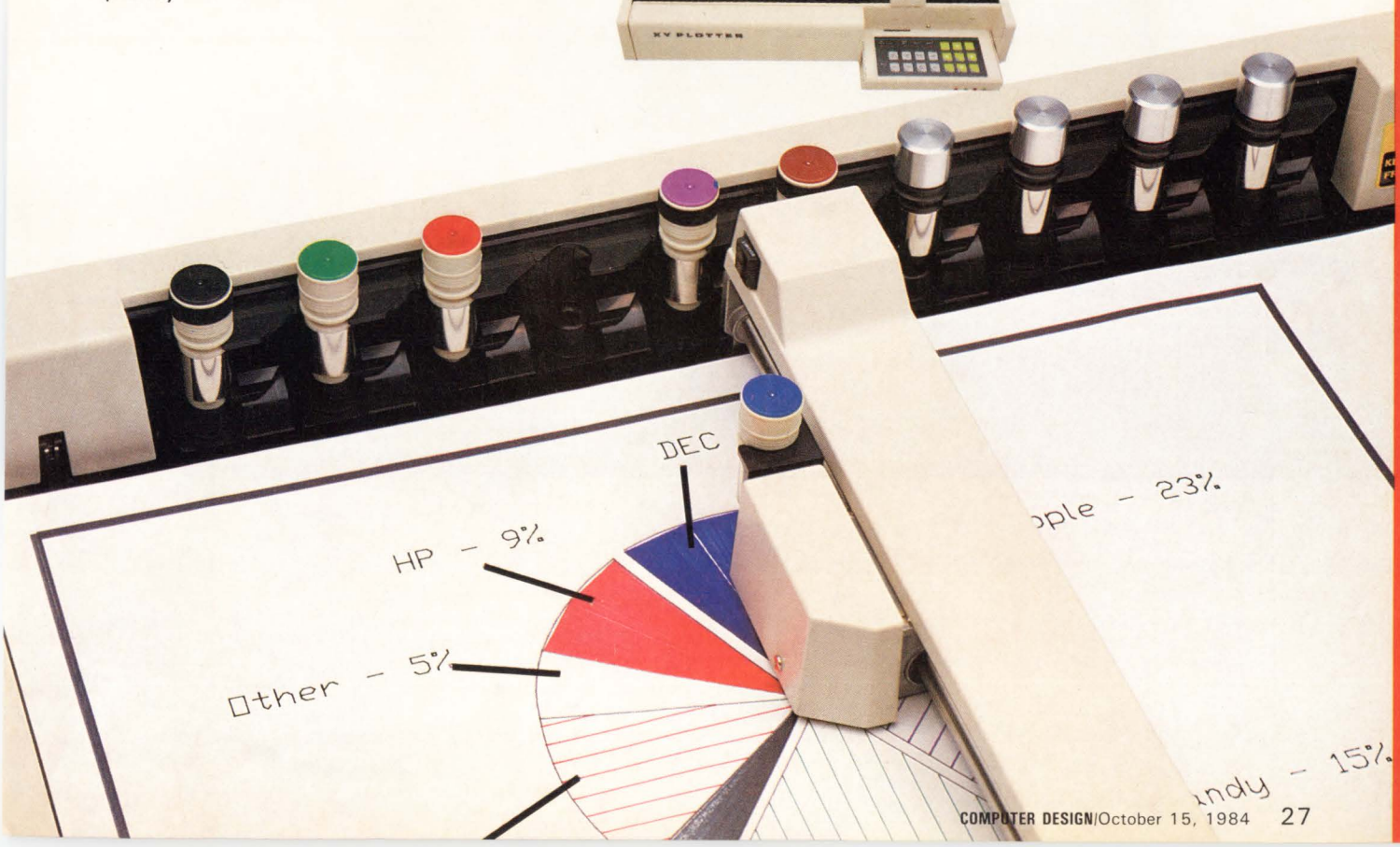
CIRCLE 16



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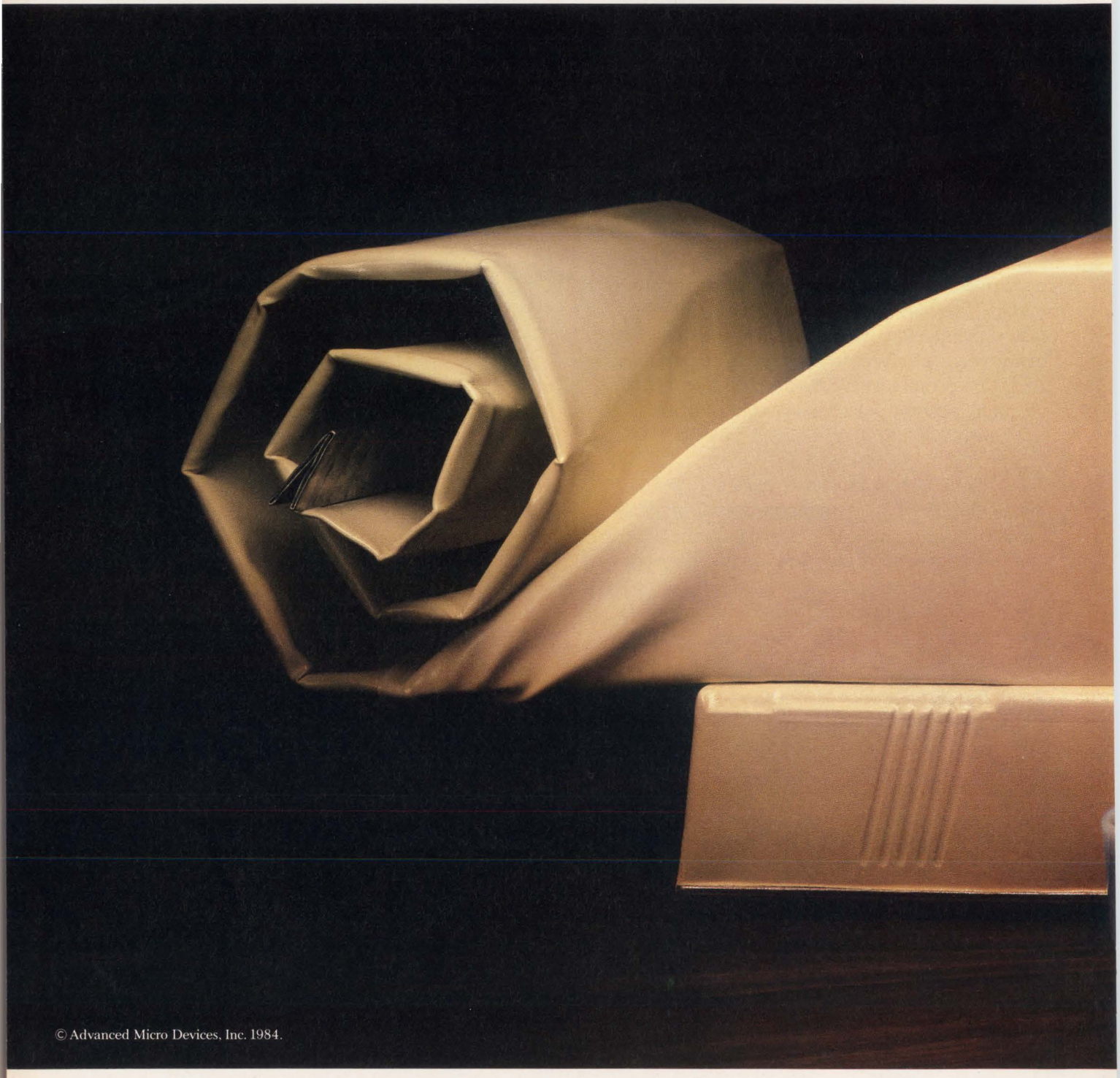
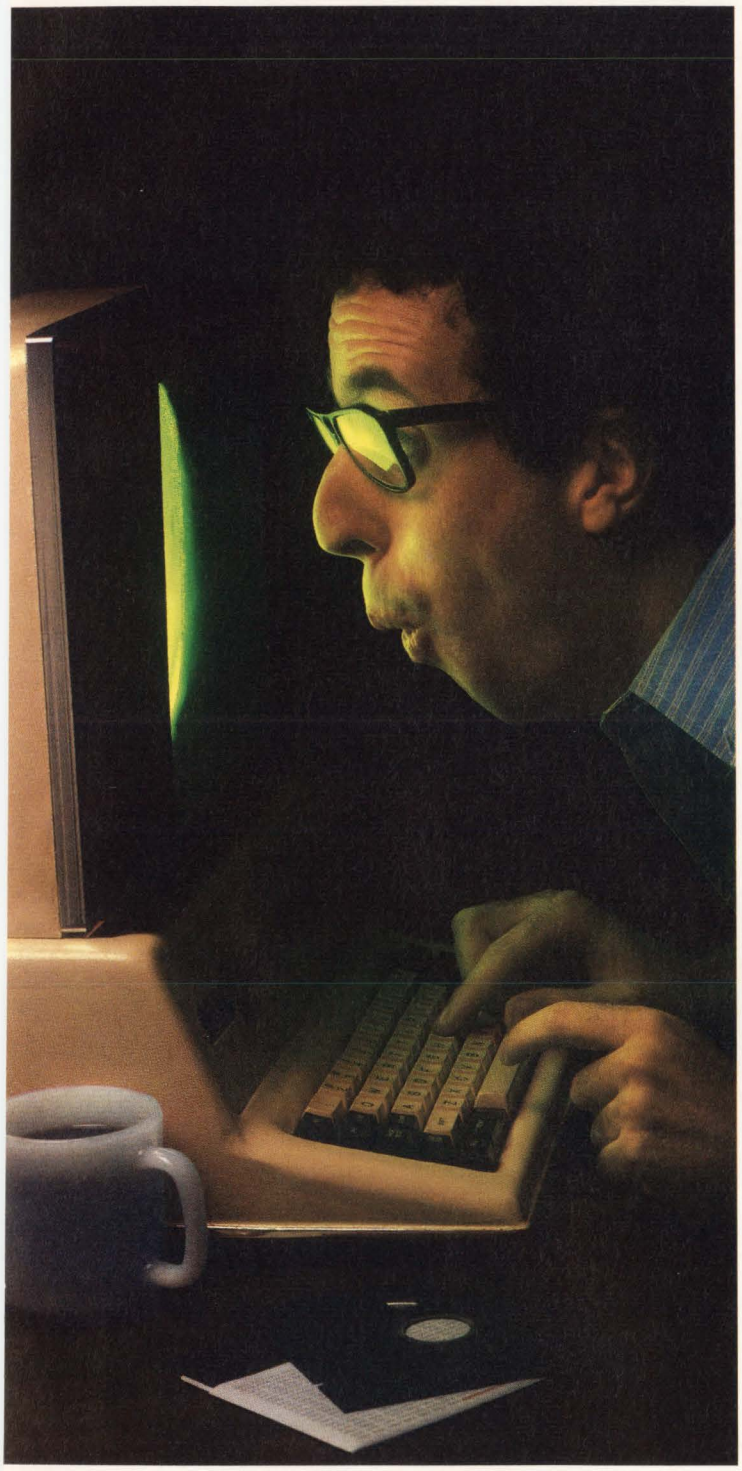


MORE OUT OF THE TUBE.



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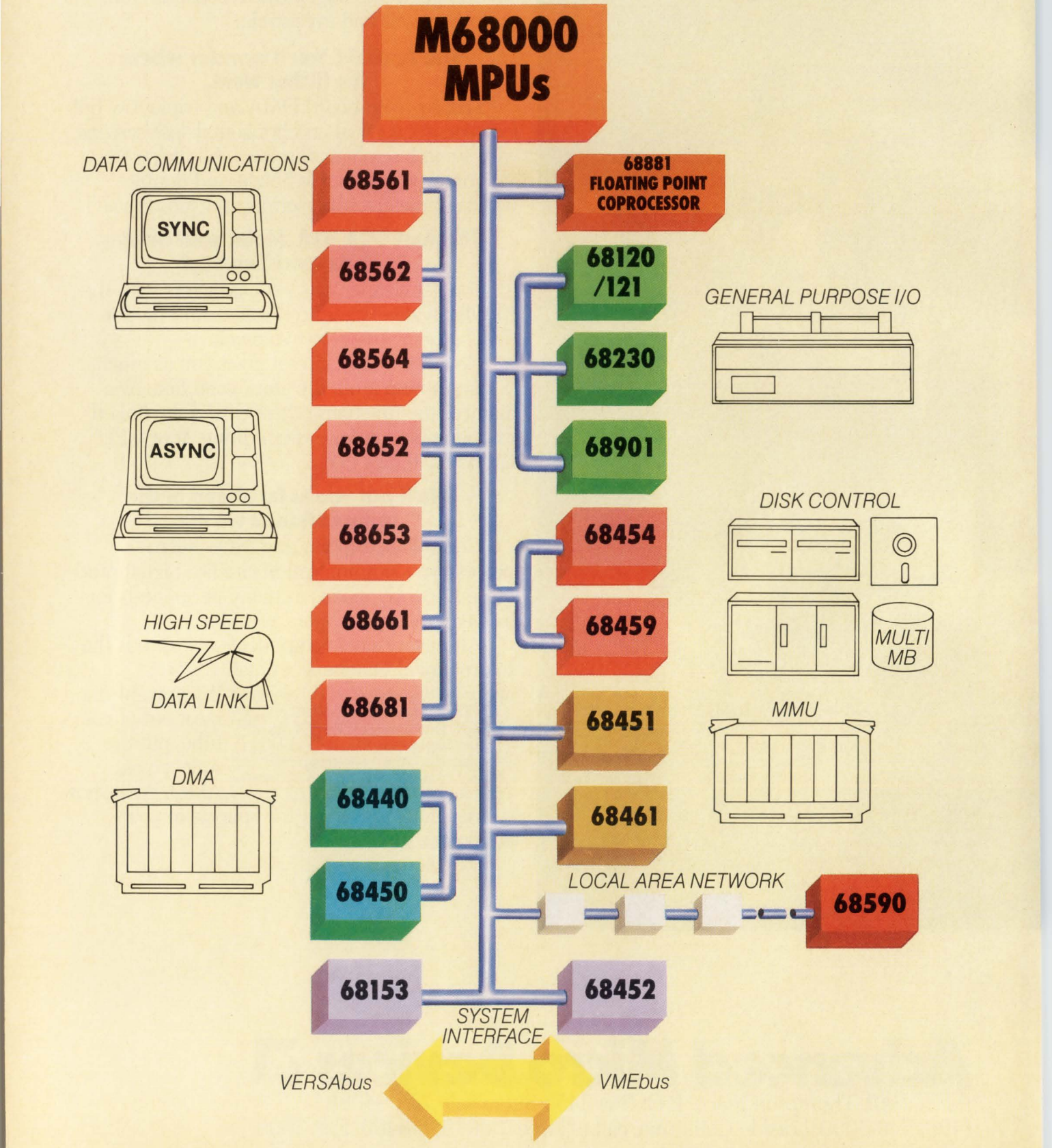
CIRCLE 17

For all these reasons, should be your next



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Data Comm, DMA Control, Local Area Network Control, Parallel, Serial and General Purpose I/O, Memory Management, Bus Control: all are there and more, to raise your systems above the competition in a hotly-competitive marketplace.

Critical for high-performance systems-DMA.

Moving data around fast, with minimal intervention from the processor is the responsibility of the 68440 Dual DMA and the 68450 DMA Controller. The 68440 is a two-channel high-speed solution, capable of a 5 Mbyte/sec transfer. The 68450 offers four independent DMA channels and extensive support for the movement of complex data structures.

Link your system to the outside world.

Whether to a terminal, a transmission line or another system, M68000 Family data communication devices link up your system efficiency and free the processor for more important work. The family offers one of the most popular data comm parts available—the 68661 Enhanced Programmable Communications Interface. It's a universal synchronous/asynchronous comm chip that interfaces easily to M68000 MPUs and directly to most 8-bit MPUs.

The 68681 Dual UART is another important available family peripheral. It provides two completely independent full duplex receiver/transmitter channels in a single package.

A Multi-Protocol Communications Controller, the 68652, contributes extensive flexibility, and basic microcomputer functions are provided by the 68901 Multi-Function Peripheral.

Still other aspects of M68000 Family data comm functionality available from Motorola include a Polynomial Generator Checker, a Parallel Interface/Timer, and two Intelligent Peripheral Controllers.

Additional 68000-compatible data communication parts are available and under development by other leading VLSI manufacturers.

Network and bus control.

Network and bus control requirements expand as multiple-processor operations increase and networking grows in popularity. The M68000 Family grows to meet these requirements with circuits like the 68590, scheduled for introduction this year. It's designed to meet all IEEE Ethernet™ specifications for M68000 systems. And, with the VMEbus becoming a standard, a new VME Controller will be added to the family as well.

Disk control and memory management.

Management of data storage devices is the domain of the 68454 Intelligent Multiple Disk Controller. The extremely flexible IMDC can control any combination of up to four single- or dual-density floppy and hard disks of various formats.

Our 68451 is now seasoned by years of experience with multi-user, multi-task systems, because memory management was one of the first peripheral functions identified in processor systems. UNIX™ System V/68™ fully supports operation of the 68451 MMU. Now, the requirements of 32-bit demand-paged virtual environments are immediately satisfied by the MC68461 Memory Management Controller.

Floating point.

The Motorola 68881 Floating Point Coprocessor is a companion processor to the 68020 scheduled for sampling within the next few months. It's designed to provide support for the latest revision of the IEEE specification for floating point high-level calculations, and also can be used as a peripheral with the 16-bit M68000 Family processors.

For additional information on the entire M68000 Family, write or fill out the coupon, and send it to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, Arizona 85036. Do it today.

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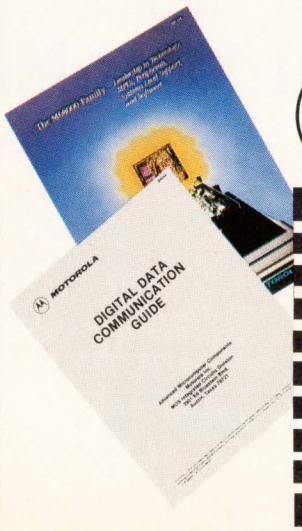
M68000 FAMILY

Function	Designation	Device No.
16-bit Microprocessor	MPU	68000
8-bit Microprocessor	MPU	68008
16-bit Virtual Memory Microprocessor	MPU	68010
16-bit Expanded Virtual Memory Microprocessor	MPU	68012
32-bit Virtual Memory Microprocessor	MPU	68020
Floating Point Coprocessor	FPC-P	68881
Dual Direct Memory Access	DDMA	68440
Direct Memory Access Controller	DMAC	68450
Multi-Protocol Communications Controller	MPCC-2	68561†
Dual Universal Serial Communications Controller	DUSCC	68562
Serial I/O	SIO	68564†
Multi-Protocol Communications Controller	MPCC	68652
Polynomial Generator Checker	PGC	68653
Enhanced Programmable Communications Interface	EPCI	68661
Dual Universal Asynchronous Receiver Transmitter	DUART	68681
Intelligent Multiple Disk Controller	IMDC	68454
Disk Phase Lock Loop	DPLL	68459†
Memory Management Unit	MMU	68451
Memory Management Controller	MMC	68461
Intelligent Peripheral Controllers	IPC	68120/121
Parallel Interface/Timer	PI/T	68230
Multi-Function Peripheral	MFP	68901
Local Area Network Controller—Ethernet	LANCE	68590
Bus Interrupter Module	BIM	68452
Bus Arbitration Module	BAM	68153

†Alternate source available only



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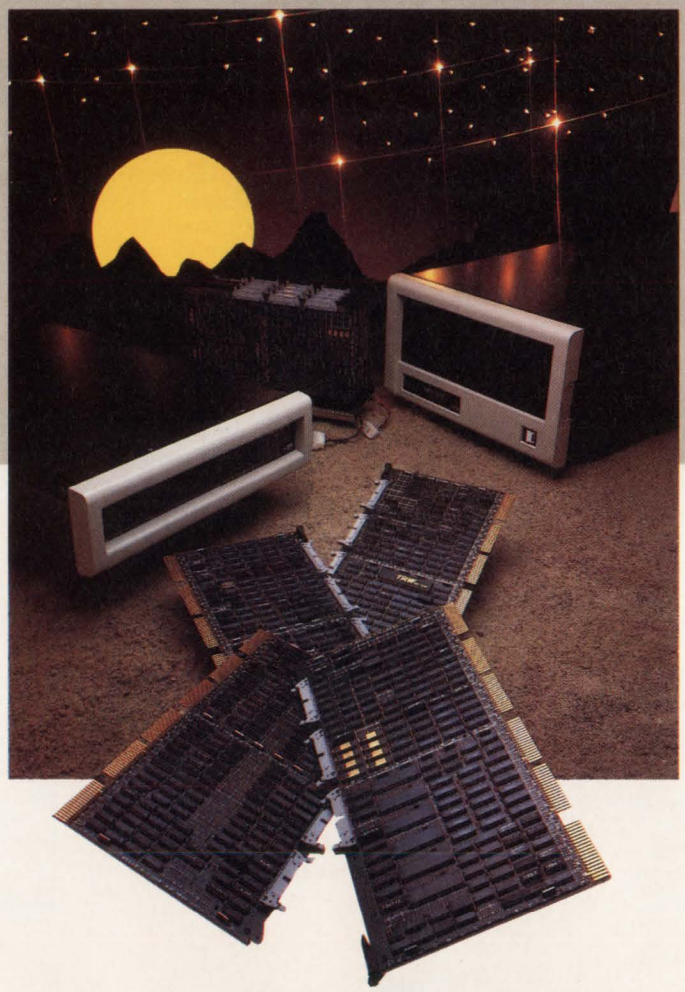

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CIRCLE 18

Data bases add function to meet computer aided design needs

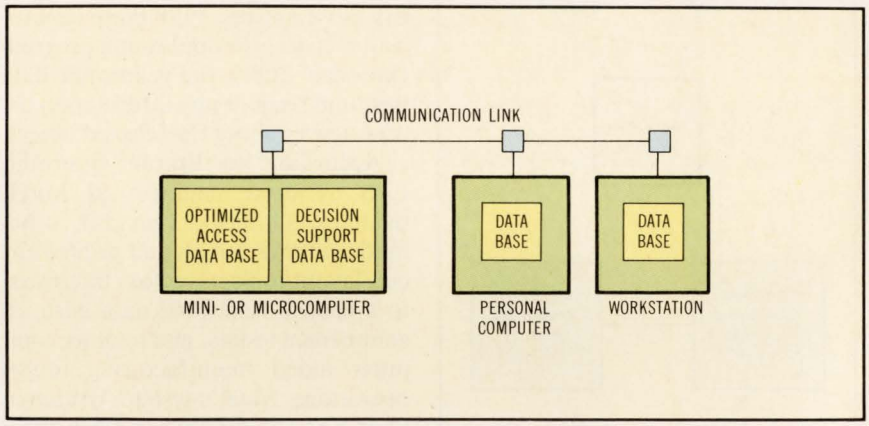
Developments now underway promise more advanced relational data bases capable of handling optimized access "production" tasks and flexible access decision support. Until these more efficient data bases appear, a variety of database techniques are being used.

Considerable design effort has already been expended on specialized data bases to store graphical data for rapid display. Manufacturers of engineering workstations have developed such data bases to support their equipment; for example, Apollo Computer's (Chelmsford, Mass) Graphic Metafiles for use with its engineering workstations. Similarly, Computervision (Bedford, Mass), a complete computer aided design (CAD) manufacturer, treasures its proprietary in-house graphics data bases.

Database developments are also driven by the needs of the even larger management information sector which seeks better ways to combine the data storage needs of executives and clerks. Database experts agree that the best long range solution for this type of storage will be universal data bases that can handle a variety of data at the same time. Such research is underway at companies like Computer Corp of America (Cambridge, Mass), Mitel (Ottowa, Canada), and in several university campuses.

With the spreading use of data bases, it has become apparent that computers perform two different types of activities: optimized access and decision support. High production data processing and engineering design graphics image displays require optimized access. Decision support systems aid management decision making and support basic engineering design procedures.

If the data base is for decision support, relational access is exceptionally capable and flexible. However, where optimized access is necessary, existing relational data bases cannot satisfactorily handle many data processing production and graphics storage problems. Several different techniques are currently used to allow data bases to provide decision support and optimized access. Since relational data bases are frequently unable to handle optimized access, other more conventional or more specialized data bases are used for these activities. But relational types remain the best choice for decision support.



Separate data bases may be located within a single computer or in individual computers. Concurrent access for multi-user data bases and outside access through communication links are possible.

Separate data bases

It is common in business applications to maintain completely separate data bases for decision support and optimized access. Separate, independent data bases may occupy space in the same disk storage unit under the control of one computer, or they may each be in separate storage units attached to different computers. When computers or workstations are connected, separate data bases can be accessed by multiple users, sometimes concurrently. In many cases the same or similar information is stored in the separate data bases, especially when access to individually compiled data bases is through personal computers.

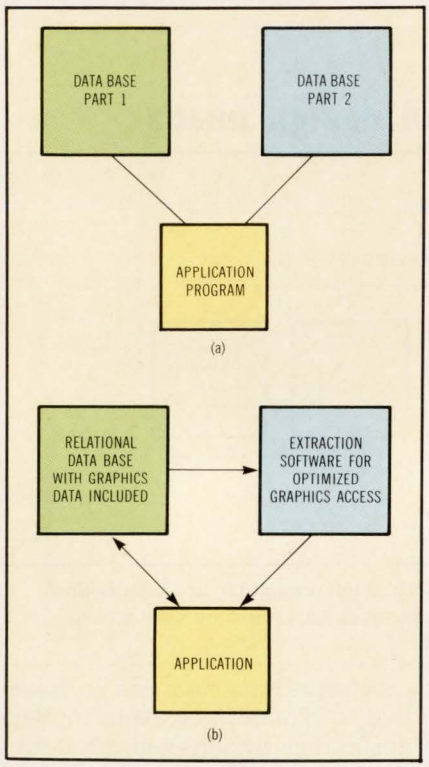
Separate data bases can be organized to minimize or eliminate data duplications by partitioning and storing all similar information in one data base. For example, Mentor Graphics (Beaverton, Ore) uses a specialized data base optimized for graphics presentations. Jack Bennett, a project leader at Mentor, explains that in this database scheme for computer aided engineering (CAE) circuit design applications, a separate relational data base stores supporting information about circuit properties and connections between components. This information can be readily accessed.

The relational data base stores circuit-related items such as net lists, components, pin configurations, and properties. Some applications must start with specific components, find all the pins attached to them, and then all the nets attached to those pins. Other applications start at the nets and work their way to the components. Still others allow users to browse through a circuit and randomly change individual component properties. Relational flexibility allows all these procedures to be followed with ease.

(continued on page 34)

Data bases add function

(continued from page 33)



When stored information can be cleanly divided, the data base can be partitioned into separate parts, and only the appropriate part is accessed (a). Extraction software can provide optimized access to data stored in a relational data base. Decision support data is obtained directly from the data base, while optimized access is through the extraction software (b).

The basic requirement for a graphical data base is more straightforward—the stored information has to be put on the screen as quickly as possible. Suppose the components for a computer aided printed circuit board design are to be purchased from outside vendors. A relational data base can store needed information on component suppliers.

If the designer needs to know the total cost of the parts on the printed circuit, however, the graphics data must be correlated with costs and other project information. Graphical and nongraphical information must then be merged from the separately partitioned data bases. The two can be tied together through design application programs that access both data bases. From a graphical display, the user may select objects of interest. The application program can then query the graphics data base to identify those objects. With those identification codes, the application program can then query the relational data base and retrieve any information the user desires about the selected object.

According to Emran Quereshi, CAD database engineer at Mitel, (Kanata, Ontario, Canada), schematic entry terminals and printed circuit layout tools have been interfaced to a central relational data base, to commercial testers, and to other computer aided manufacturing (CAM) operations. Mitel's system, written in C, is VAX-compatible and is now in the testing stages.

Extraction techniques

Michael Stonebraker, a professor and database expert at the University of California at Berkeley, has proposed another way to tackle CAE data storage problems. Both the graphics and the supporting information would be kept in a relational data base. This provides an efficient way to extract the graphics data and allows fast display.

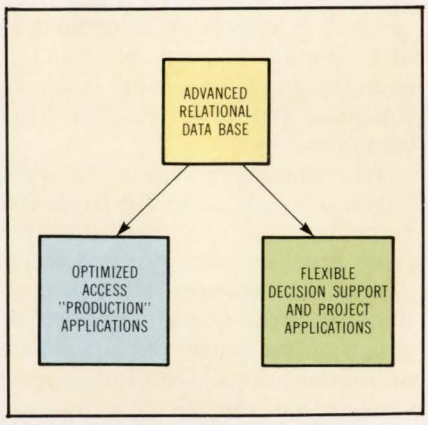
Take a data base designed specifically for graphics storage. Discard concurrent access, crash recovery, and other database controls and services. What remains is the access structure—the way that data is handled between main memory and disk storage so as to optimize movement of data between the two. In other words, the result is optimized extraction software.

Equipped with this extraction software, a relational data base can store information for graphics display, as well as for decision support. When displays are needed, the database stored graphics information is extracted and transformed into the most efficient form for main memory storage and use. For example, a designer may wish to browse through the portion of a design of an aircraft wing between the wing tip and the engine. To do that without suffering long waits for display changes, all the needed graphics data must be moved into main memory. Using the extraction capability, the revised main memory contents are quickly retransformed into database format once the design has been reviewed. Then, the memory contents are moved back into the relational data base.

Relational access

Decision support can also be effectively combined with optimized access by superimposing a relational "front end" on a nonrelational data base. A relational data base's flexibility in handling unpredictable inquiries is due to operations like Join. With this operation, users can tie together two groups of records, when no tie was planned. This makes possible the kind of queries needed for decision support.

By combining a query language that includes Join and other operations with an optimized access data base, decision support and access functions are possible. Where "production" activities are a primary concern, priority arrangements can be added to keep decision support queries from interfering with production schedules. Security aspects and access restrictions can also be handled at the relational front end. This is the



Advanced relational data bases are expected to provide a single unified basis for both optimized access and flexible decision support. Such data bases are not yet available.

approach used in such database products as RQL/32 from Perkin Elmer (Oceanport, NJ) and ENFORM from Tandem Computers (Cupertino, Calif).

These techniques for linking optimized access and decision support database uses involve extensive specialized software design efforts. General-purpose relational data bases that can handle both types of requirements would be a better solution. These new data bases are already under development. They will need new capabilities, including massive main memory buffer storage, multidimensional indexing, and a rich selection of primitive objects that includes geometrics, as well as familiar alphanumerics. Developments along these lines are being stimulated by the needs of CAD activities.

Most general-purpose data bases are best suited for accessing data residing on a disk. Thus, there are no commercial data bases designed to make full use of 5-Mbyte main memory buffer storage areas. But, CAD applications require the prompt display of massive amounts of data. Consequently, main memory buffer storage must be very large. This capability is currently under development.

Existing relational data bases use one-dimensional indexing. This serves well where the items to be indexed are dollar figures or words. For example, a typical computer stored table contains columns with names, ages, salaries, and departments for each employee. Access is gained through a one-dimensional index of the selected key column.

In contrast, graphics require two- and three-dimensional indexing. This allows the software to rapidly identify those objects whose coordinate positions are pointed to by the cursor, as the user pans the display. For graphics, it would be helpful to be able to index rectangles. A relation containing various rectangles would be most efficiently accessed by indexing the rectangles in such a way that each index entry takes account of all four corner points.

A new generation of programming tools is emerging from artificial intelligence research. Lisp and other similar AI languages support the building of abstractions and hierarchies, which are the kind of tools needed to handle graphics along with other types of information in a data base. In the near future, we can expect to see designers blend these AI tools with relational data bases. Work on this approach is now underway at MIT and companies such as Symbolics, Inc (Cambridge, Mass). Howard Shrobe, a technical director at Symbolics, is building a CAD system in which all the data management facilities are written in Lisp.

Objects in CAD data bases include cylinders, polygons, groups of lines, and solid shapes. Primitive objects currently available for use in data bases are integers, slopes, character strings, and packed decimals. Simulating the graphical objects using these alphanumeric primitives is inefficient. Primitives that directly represent geometric shapes would be more useful. A relational data base typically represents a rectangle by four floating point numbers. A data base designed to handle graphics efficiently, would represent this rectangle by a "box" code.

Just as higher level languages allowed programmers to work much more effectively than they could with assembly languages, these new representations will open up more powerful database capabilities. The Daplex Adaplex data base, now operating in prototype form at Computer Corp of America, is able to provide more direct representation of objects and hierarchies along these lines. Still in development, this is a post-relational data base based upon, but going beyond, relational techniques. After further development, relational data bases with greater speed and efficiency should accommodate a wider range of needs.

—Howard Falk, Contributing Editor

SYSTEM TECHNOLOGY

(continued on page 42)

Announcing the arrival of the world's first universal

Standard Microsystems' HDC 9224 is so advanced it controls hard disks, floppy disks and even tape back-up.

The new addition to Standard Microsystems' magnetic controller family is a single chip that controls Seagate-compatible hard disks, as well as IBM®-compatible single- and double-density floppy disks.

A single chip that allows you—for the first time—to include tape back-up in a small computer without adding a lot of costly hardware and software.

A single chip so advanced its built-in DMA controller and ECC detect and correct errors with absolutely no processor intervention.

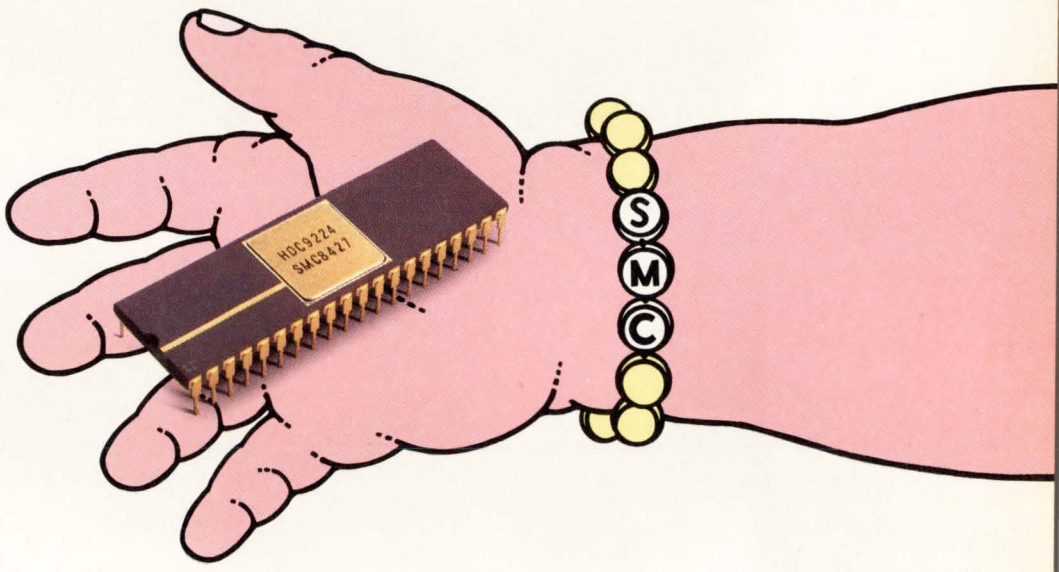
We've named this new addition the HDC 9224 Universal Disk Controller. But, you may call it one of the biggest breakthroughs in IC performance in a long, long time.

The cornerstone of an intelligent subsystem.

The HDC 9224's ultraflexible architecture makes it the true "next generation Winchester disk controller." With the addition of a few simple parts, you can use the HDC 9224 to build a high-performance, low-cost subsystem that not only controls hard and floppy disks, but cartridge or cassette back-up, too.

The HDC 9224 easily interfaces to all popular ST506-

disk controller.



compatible hard disk drives with up to 16 heads. Its flexible format command lets you select hard disk sector lengths up to 16 kilobytes and can be used with both interleaved and non-interleaved sector formats.

What's more, the HDC 9224 controls up to four disk drives of all sizes—8-inch, 5.25-inch and the new 3.5-inch—and it can read and write a wide variety of single- and double-density floppy formats, including such standards as IBM's 3740 and System 34.

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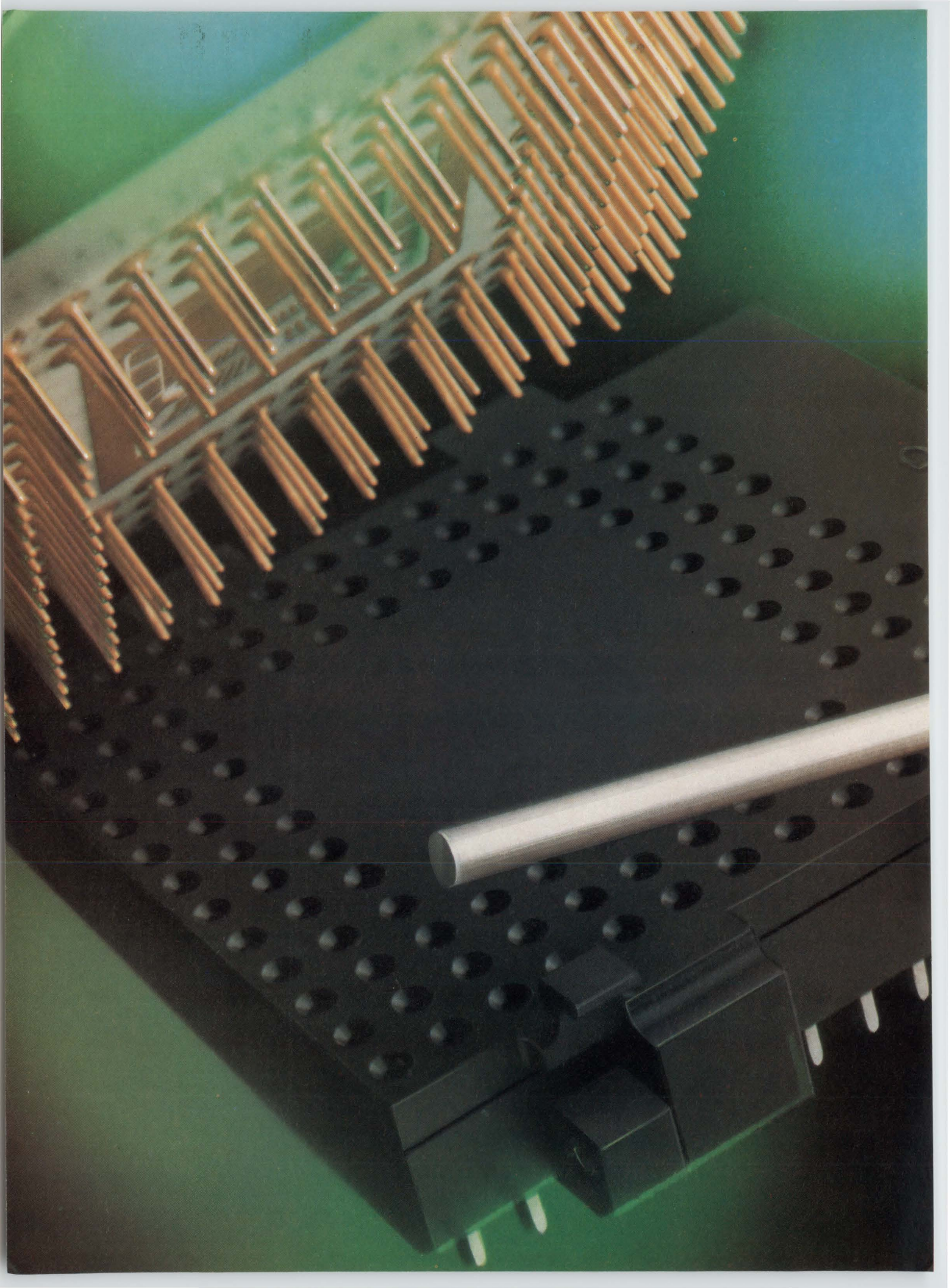
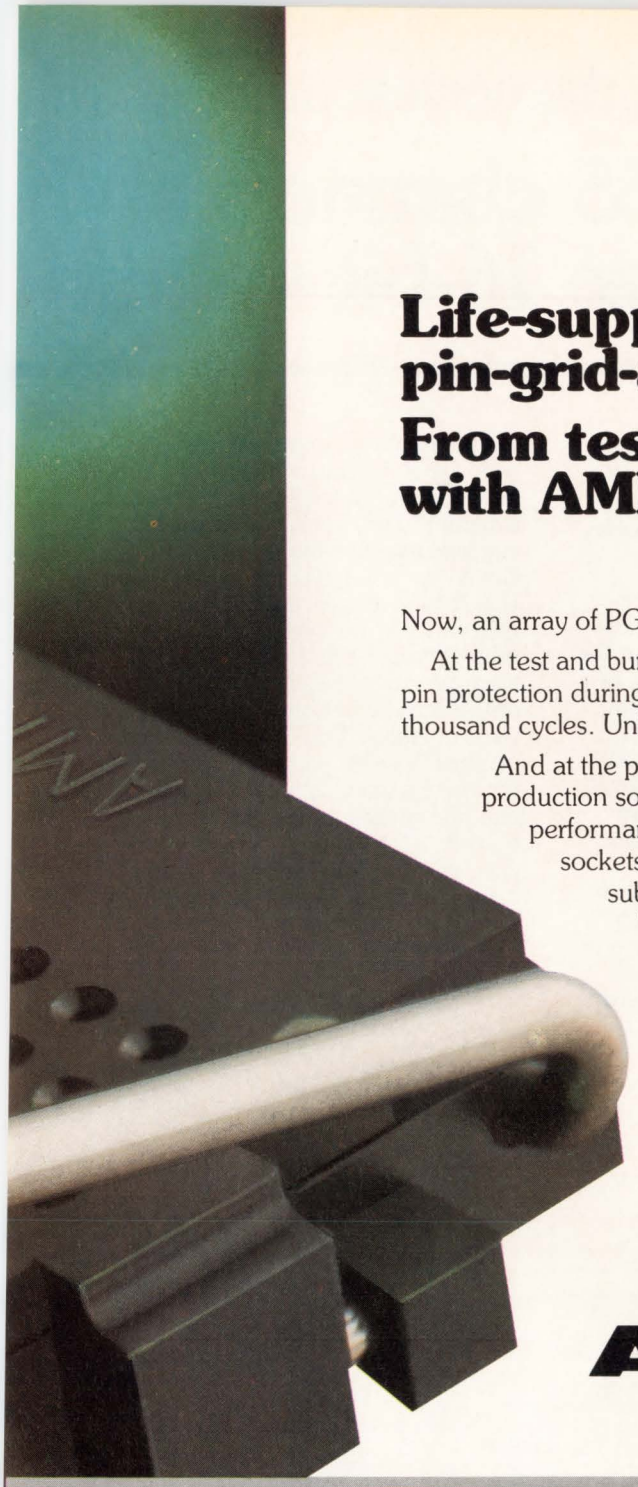
CIRCLE 20





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CIRCLE NUMBER 10

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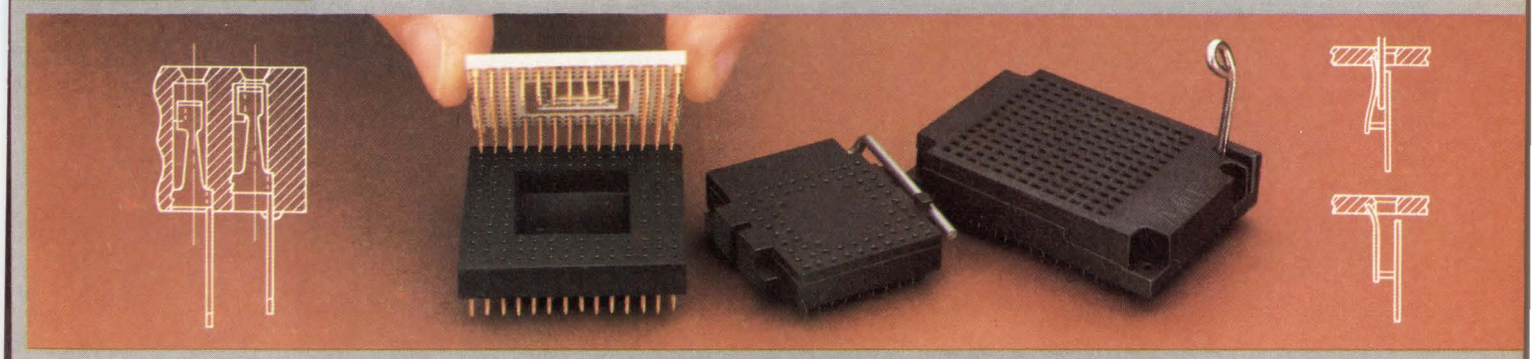

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The HP 1630G...65 channels and maximize 16-bit system

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Three new software overview modes let you nonintrusively monitor software performance and hardware/software interactions in real time.

The HP 1630G significantly expands on the software performance capabilities already introduced in the HP 1630A/D family members. In addition to time histograms that show execution-time distribution, and label histograms that show address activity, the HP 1630G gives you three new modes: program flow, time positional, and linkage measurements. *Program flow measurement* lets you monitor program activity based strictly on op-code accesses. This can help resolve confusions which may occur when histogramming by address, especially if the program generates inline code or if memory blocks are interspersed between sections of the program. *Time positional measurement* lets you measure the number of occurrences of an event per unit time. Use this to better understand the behavior of your system under a time-varying load. *Linkage measurement* measures the relative frequency of the activity between specific software modules. You'll find this mode invaluable when you want to monitor the transfer activity between a main program and a series of subroutines, for example. Take advantage of all these software performance analysis modes to rapidly

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Floppy disc interface and popular 16-bit microprocessor support.

On-board non-volatile memory keeps one instrument setup and your current disassembler instantly available at power-up. For even greater storage, the HP 1630G features direct compatibility with a number of HP disc drives such as the HP 9121S/D (the HP 9121D is illustrated). In one convenient 3 1/2" floppy you can now store data, state listings, timing diagrams, alternate disassemblers, and instrument setup configurations. For added flexibility, the HP 1630G supports all popular 8-bit, as well as the following 16-bit microprocessors: 68000, 8086, 8088, 80186, 80286, Z8001 and Z8002.

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HP 1630G

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CIRCLE 21

Artificial intelligence concepts are being put to practical use

The list of participants in the world of artificial intelligence keeps growing. Offerings from pioneers Symbolics and LISP Machines have been joined by IBM's Lisp/VM, an AI software tool that took over 10 years of internal research to develop. Tektronix, Digital Equipment Corp, Data General, and Texas Instruments have ventured into the field of knowledge engineering also. Development programs from several startups, written in Prolog, Lisp, Fortran, and C, bring AI to the personal computer (see Table, "New Entries in AI").

IBM's Lisp/VM is written for a machine configuration that will support both VM/SP and CMS program environments. It is not available for the PC. To execute, these programs require a VM/SP virtual machine with a minimum of 1 Mbyte of virtual memory. Actually, Lisp/VM consists of a programming language and a unified program development environment. Its programs and data are accessed through a program editor (LispEDIT) or through the VM/SP editor (XEDIT).

LispEDIT requires a minimum of 4 Mbytes of virtual memory for execution. It provides a split screen interface to the system in which the top portion shows the Lisp expression currently under consideration, formatted for the Lisp language. The lower portion shows the most recent user input and system messages. This software uses the CMS file organization to support its library functions. The program librarian allows a collection of programs to be stored in one file, and individual access to and updating of each program. The compiler, interpreter, editor, and loader all interact through these files.

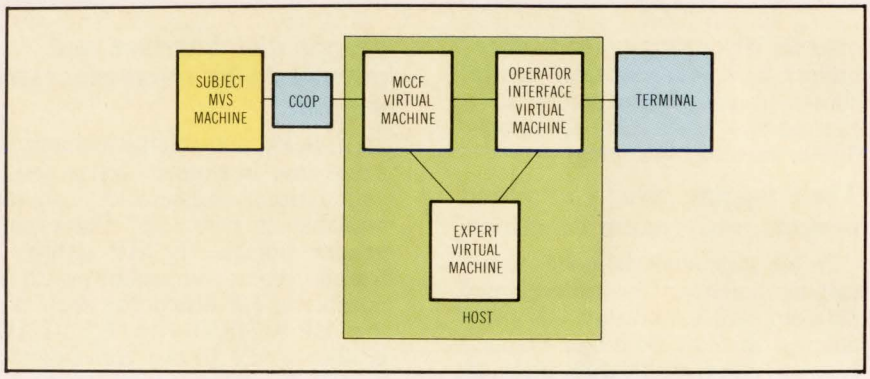
IBM uses this software to design expert systems. One such system is the Yorktown Expert System for Multiple Virtual Storage (YES/MVS). This system is essentially a software watchdog that aids computer operators in controlling an operating system.

Unlike "static" systems, which can solve the problem separate from the operation, this system responds to changing computer system conditions in real time by keeping the large computers operating. While watchdogs for realtime systems are nothing new in the electronic transaction industry, this is believed to be the first system that applies expert rules to keep systems online.

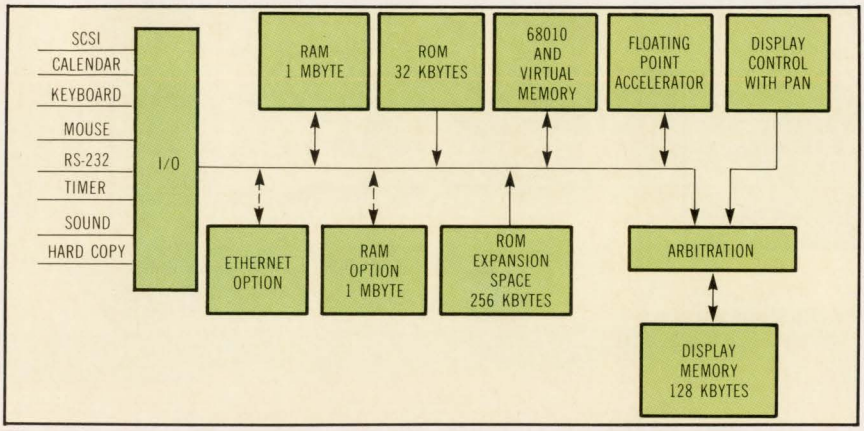
Trained operators are needed to control large, multimillion-dollar installations that handle such applications as banking transactions, reservations, and credit verifications. As computers become more sophisticated and fully trained operators become less able to handle them, more powerful installation management tools are needed.

YES/MVS was developed for managing MVS operating systems, IBM's most widely used operating system on its large mainframe computers. Currently, the expert system is experimental and being applied to

(continued on page 44)



YES/MVS runs under the VM/370 operating system on an IBM 3081 computer. Currently, the system is partitioned into three virtual machines for speed and efficiency: the MVS operator system, the MVS communications control facility (MCCF), and a machine to control the display console. Communication to the MVS machine is via centralized control of processors (CCOP), which provides centralized control and filtering of messages between various computers at an installation.



The entire 4404 architecture fits on two boards, with one handling all the I/O functions and the other handling the rest of the circuitry. While this is a complete development system, a built-in ANSI X3.64 terminal emulator allows it to act as a terminal attached to a mainframe computer through an RS-232 port. An optional Ethernet is also available.

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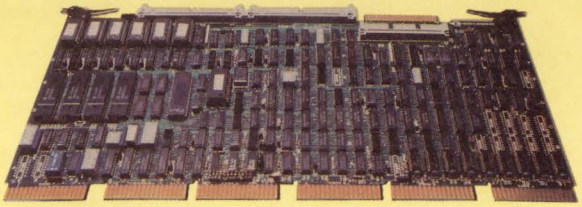

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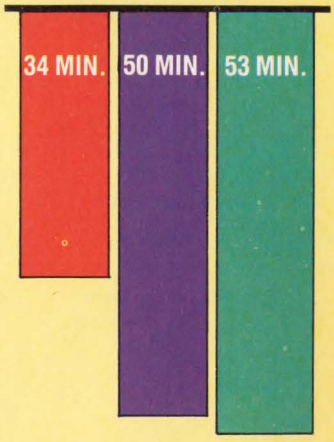

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AI concepts

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New Entries in AI

Company	System Name	Application	Configuration	Price
Tektronix (Beaverton, Ore)	4404 AI systems	Development system using Smalltalk-80, Franz Lisp, and Prolog options.	Self-contained desktop terminal with 10-MHz 68010 and common interfaces.	$14,950 per unit
Data General (Westboro, Mass)	Common Lisp	Software package for AI applications.	Used on DG's 32-bit ECLIPSE MV superminis and DS workstations	$8000 lic. on MV $2000 lic. on DS
Digital Equipment Corp (Maynard, Mass)	Numerous AI software packages from independent producers	Development tools including Inference's ART, Gold Hill's GCLISP, ISI's Interlisp, Prologia's Prolog II, Carnegie Group's SRL+ and PLUME.	Used on DEC VAX and personal computers.	Based on package
	VAX Lisp	Development tool based on Common Lisp.	Used on VAX/VMS machines.	$8000
	OPS5	Knowledge-encoding language to derive production rules.	Used on VAX/VMS machines.	$5000 $3000 lic.
Teknowledge (Palo Alto, Calif)	M.1	Development tool for microcomputers.	Used on IBM PC.	$12,5000 includes 4-day training and 1-year maintenance $2500 lic.
Symbolics (Cambridge, Mass)	3670	Symbolic processor for AI applications.	Self-contained computer with 30 Mbytes of memory.	$84,500
Logicware (Toronto, Canada)	MProlog	Prolog-derived development language.	Used on IBM VM/CMS, DEC VAX/VMS, and IBM PC.	$300 to $40,000 depending on machine used.
IBM (Kingston, NY)	Lisp/VM	Development tool for Lisp-based applications.	Used on IBM's System 370 processors.	$6500 lic.
Texas Instruments (Austin, Tex)	Personal Consultant	Development tool for Lisp-based applications.	Used on TI's Professional Computer under IQLisp.	$3000
Gold Hill Computers (Cambridge, Mass)	Golden Common Lisp (GCLisp)	Development tool for microcomputers.	Used on IBM PC with at least 256 Kbytes of memory.	$495
Jeffrey Peronne and Associates (San Francisco, Calif)	Expert-Ease	Development tool for microcomputers.	Used on IBM PC with at least 128 Kbytes of memory.	$2000
Metacomco (Monterey, Calif)	Cambridge Lisp 68000	Development tool for 68000-based systems.	Used on SAGE computers under TRIPOS operating system.	$750
LISP Machine, Inc (Los Angeles, Calif)	4 x 4	Four-user Lisp machines for development of Lisp applications.	Four self-contained Lisp processors that can share common resources.	$45,000 per user
	PICON	Realtime expert system for process control.	Used on LMI's Lambda/ PLUS machines.	N/A
Production Systems Technologies, Inc (Pittsburgh, Pa)	OPS83	Refined compiler-based programming language to develop production rules.	Used on VAX 11/750 and VAX 11/780.	$10,000

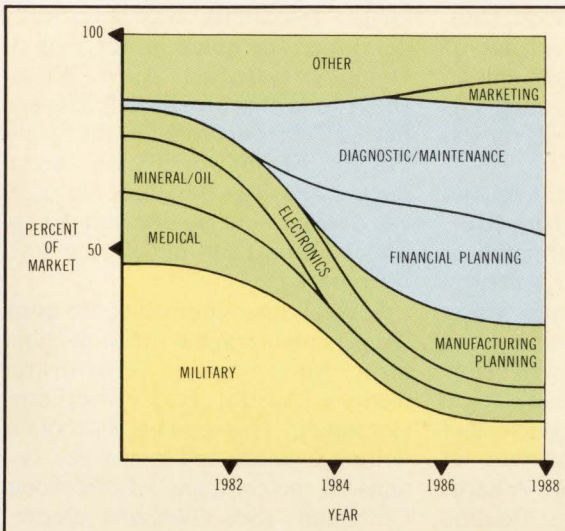
large mainframes at the company's research facilities in Yorktown Heights, NY.

The software running in a large computer installation represents hundreds of man-years of development and comprises many interacting subsystems. Each installation has a different configuration and different local policies for computer operations, both of which change over time. Thus, the tools that manage a computer installation must be tailored and modified to meet changing conditions. A realtime expert system becomes a natural choice for this task.

The challenge to a realtime expert system is somewhat bigger than for systems that primarily serve a consultative role such as MYCIN or CASNET, both used in medical settings. These static expert systems make conclusions based on user-interpreted inputs, while YES/MVS bases its conclusions on primitive facts obtained directly from the system being monitored. Making the proper choice is challenging since, by the time conclusions are to be put into effect, many facts may have changed. The dynamic character of the system makes it difficult to model, to develop, and to debug.

The software runs under the VM/370 operating system on an IBM 3081 computer. Because the subject MVS system and the YES/MVS reside on different computers, problems on one will not interfere with the other. Currently, the software is partitioned into three virtual machines for speed and functional separation. Because of its flexibility, the OPS5 language was chosen for the MVS environment. Intelligence, in the form of OPS5 rules, is distributed between the expert virtual machine and the display controller.

The IBM researchers fine tuned the OPS5 rules to the point where modified versions run significantly faster than other Lisp implementations of OPS5. Most of the expertise for keeping computers running is encoded in over 500 OPS5 rules. In addition, system programmers, manuals, and even the MVS designers were consulted. Despite these efforts, researchers found many important pieces of knowledge during online testing that the experts did not mention.



At least one research firm predicts a decline in mainstay AI applications for the military. DM Data, Inc predicts a rise in commercial and industrial applications, specifically in financial planning and in diagnostic/maintenance. It projects the expert system software market to reach over $10 billion by 1990, up from $30 million currently.

The capabilities of YES/MVS will be expanded in the future. Other possible subdomains that may be incorporated are help for the operator during initial program loading, planned and emergency shutdown, capacity planning, configuration, and installation. Another company entering the AI

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AI concepts

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market is Tektronix (Beaverton, Ore). Capitalizing on their knowledge of Smalltalk-80, these designers built an AI development system around this icon-based language that sells for less than $15,000.

The company claims that its 4404 workstation provides a higher performance for developing such applications as expert systems, natural languages, intelligent robotics, vision systems, automatic programming, and theorem proving at a cost well below that of existing AI machines.

The 4404 is a desktop system that runs on the 68010 processor at 10 MHz with no wait states. A hardware accelerator supports floating point operations. Its user memory is 1 Mbyte of RAM, expandable to 2 Mbytes, while its page-on-demand management provides an 8-Mbyte virtual memory space that permits development of complex programs without segmentation or overlays.

This system's roots go back to 1980, when Xerox, the original developer of Smalltalk, chose Tektronix as one of four major companies to help evaluate the new programming language. (Smalltalk was specifically developed for quick prototyping of complex systems.) Allen Wirks-Brock, one of the original developers, helped Tektronix to tailor the Smalltalk for the 4404 workstation's architecture. Besides Smalltalk-80, users can develop applications with the optional Franz LISP and Prolog software packages.

Several other companies are using the personal terminal for AI development. An example is Texas Instruments's (Austin, Tex) Professional Consultant. This terminal is a tool for writing financial and legal expert systems on the company's Professional Computer. (See *Computer Design*, Aug 1984, p 8.) It has both a development engine and an inference engine. With these tools, the designer can develop an expert system incorporating as many as 400 production rules on the TI personal computer.

This development tool can handle uncertain and imprecise data. For each application, there are certain factors that determine the degree of confidence for a particular conclusion. These factors allow the user to ask why a particular question was asked or how the system reached its conclusion. Presented as numerals, the factors can be used as a basis for accepting or rejecting system recommendations.

This concept was adopted from the MYCIN system, an early AI effort. Intelligence gathering operations basic to MYCIN were later extracted for use in EMYCIN, which can be applied to AI applications such as those targeted by the Personal Consultant.

In general, current development activity is moving toward such commercial and industrial areas as financial planning and analysis. In *AI Trends 1984*, a recently released report by DM Data Inc (Scottsdale, Ariz), the research firm predicts that during the next several years, the major AI applications will be for diagnostic and maintenance aids, and financial and manufacturing planning. While it is hard to predict if this trend will continue, the recent entries listed in the Table certainly confirm the research firm's current prediction.

—Nicolas Mokhoff,
Senior Editor

MICROPROCESSORS/MICROCOMPUTERS

Multi-user systems prepare to do battle with PC AT

The challenge facing multi-user systems after the introduction of the IBM PC AT and the PC network is formidable. PC-compatible multi-user systems are responding by citing cost and performance advantages in the 2- to 12-user range. These systems also stress MS-DOS compatibility, while the multi-user PC AT is Xenix-compatible.

Two multi-user systems competing with the IBM PCs are the Dimension from North Star Computers (San Leandro, Calif) and Mega PC from Corona Data Systems (Thousand Oaks, Calif). These IBM-compatible systems consist of workstations, dedicated workstation processors, a centralized server, and shared peripherals. Both systems claim a cost and efficiency advantage by housing processors and server in one backplane.

North Star's Dimension system includes up to 12 workstations, while the Corona Mega PC system, introduced the same week as the IBM PC AT, supports up to eight. Both use a 7-MHz, 8088-2 processor (compared to the PC's 4.77-MHz processor). The Dimension server uses an 80186 processor, while the Mega PC server uses an 8088-2 processor augmented with a hard disk controller.

Each workstation functions as a single-user system with its own operating and file system, much like an independent IBM PC or XT. The workstations can also transfer data to one another, and share peripherals such as disk drives, printers, and streaming tape drives.

The Mega PC system runs under MS-DOS. The Dimension system uses an MS-DOS emulation, NS-DOS, which was recently revised for compatibility with 3Com semaphores. This compatibility allows users to take advantage of applications written for the 3Com/Ethernet marketplace. A

(continued on page 48)

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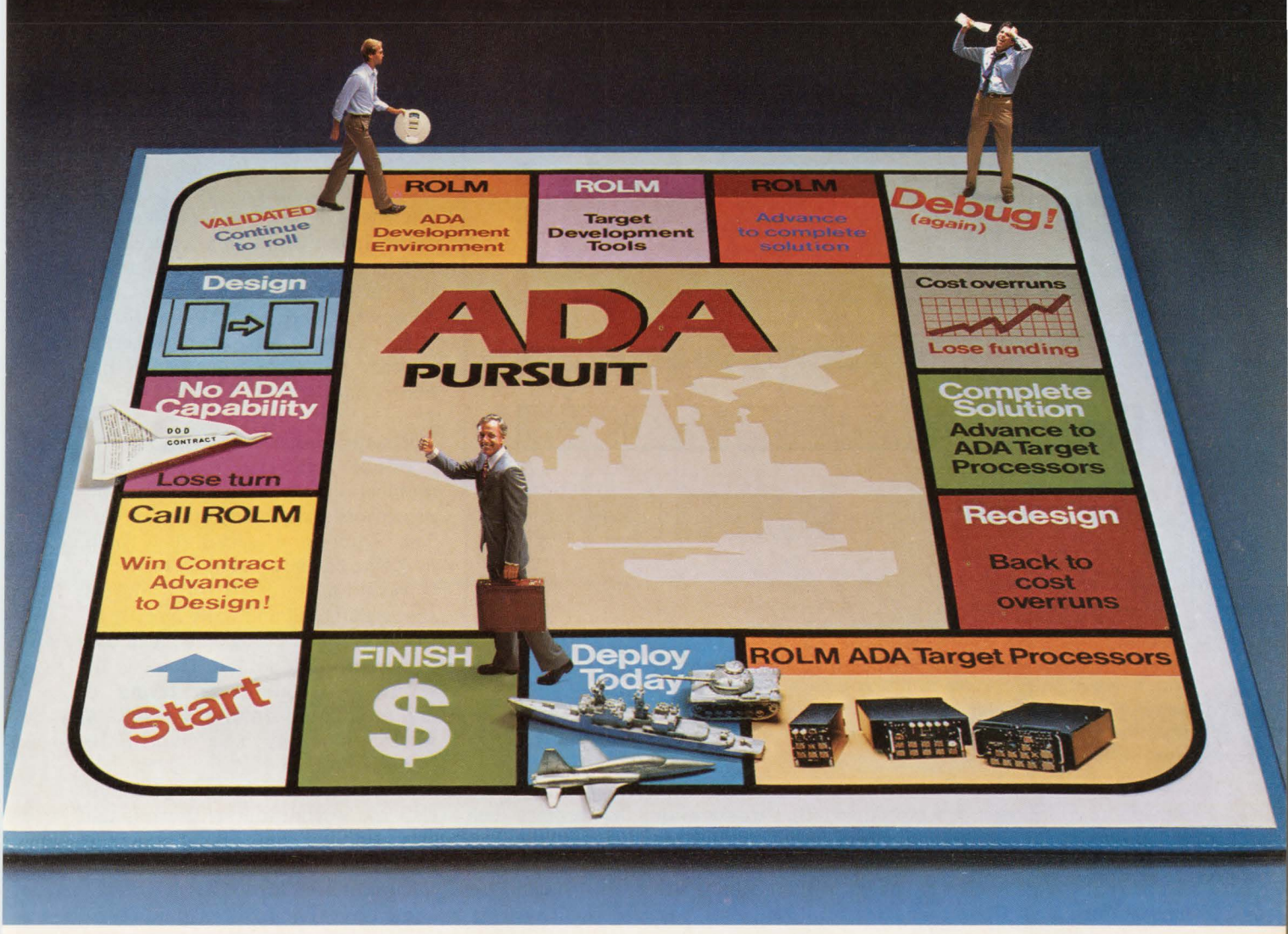

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Multi-user systems

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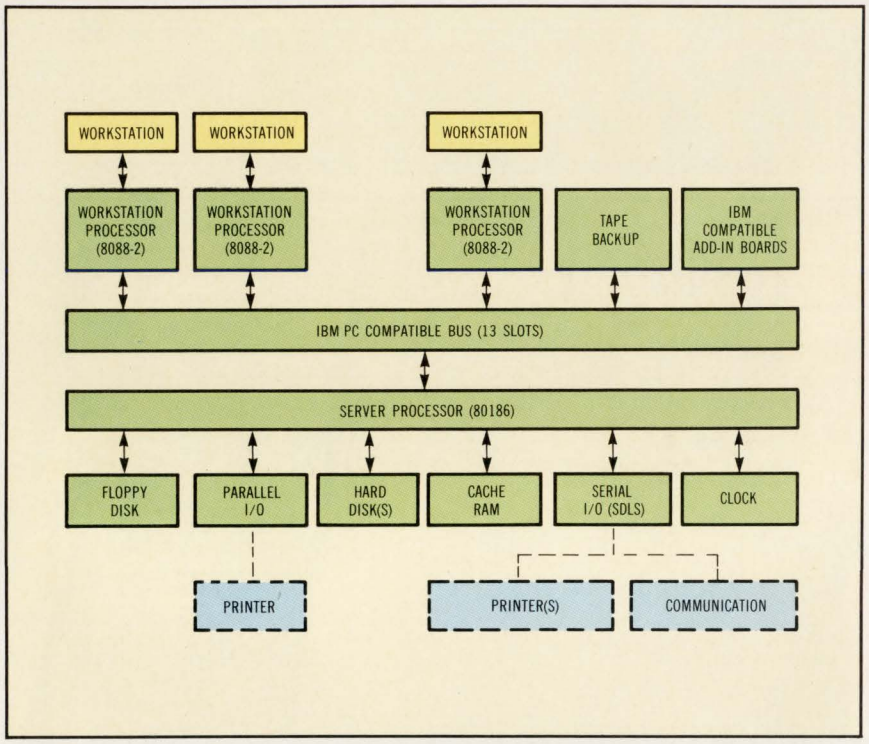


North Star's Dimension system allows workstation processors to communicate with a server processor via an IBM PC-compatible bus. The processors and the server are located in one backplane, and workstations are connected to processors with coaxial cable. IBM-compatible boards can be plugged into spare slots in the bus.

semaphore coordinates processes that run at the same time and share information. A number of multi-user database software packages, including Ashton-Tate's dBase II and Software Connections' LAN:Datastore, are written to take advantage of 3Com semaphores.

Closely coupled network

By housing the processors and the server in one backplane, the IBM compatibles minimize the need for shared communication lines. This makes it unnecessary to transmit data in packets, gain access to a LAN bus, and cope with collisions and retries. However, the processors and the server use arbitration to gain control of an IBM-compatible bus. Since the bus has a higher bandwidth than cable, communication between the workstation processors and the server is rapid. North Star calls this architecture a "closely coupled network." The trade-off for this approach is that workstations do not have their own local memory. In addition, the server is the linchpin of the system—if it goes down, the entire system goes down. However, for small systems, the savings in cost and overhead may well compensate for these disadvantages.

Both systems allow the user to plug IBM-compatible cards into spare slots in the IBM bus. A Corona spokesman commented that one could plug a LAN card into the bus, and run 256 users off the card. He did not see this as a common application of the Mega PC, however.

Both systems use a polling scheme to determine the priority of workstation requests. In the Dimension system, for example, the 80186 polls each processor on a regular basis and queues up requests. Service requests from processors are handled on a first come, first served basis. Preemptive scheduling allows higher priority tasks, such as requests from the disk drives, to claim the server processor when necessary.

A copy of MS-DOS runs on a virtual machine in the server. This operating system adds a named file system to the Dimension's electronic mail and spooling functions, and makes a set of generic subroutines available to any task. A realtime, multitasking kernel in the Dimension reduces idle time in the server processor. If a task that currently has control of the 80186 becomes blocked while waiting for an event, such as disk I/O, the kernel releases the server processor and allows another task to run.

Workstation communication

In both multi-user systems, communications between workstation processors are handled by the server. The Dimension server can map 64-Kbyte blocks of memory from any workstation into its own address space, and read and write directly to this memory. Using this method, communication is rapid. However, if several workstations are trying to communicate simultaneously, a workstation may have to wait to transfer data.

Workstations in both systems consist of keyboard/CRT terminals. Workstations are connected to the processors with coaxial cable, with separations of up to 300 ft. In the Dimension system, workstation processors have 128 Kbytes of RAM, expandable to 256 or 512 Kbytes. Mega PC workstation processors have 256 Kbytes of RAM, expandable to 512 Kbytes.

Until recently, caching of any kind has been uncommon on the microcomputer level. However, the Dimension and Mega PC systems both speed disk access time by caching data from the disk. These multi-user systems offer either 256- or 512-Kbyte RAM in server memory. In North Star's Dimension system, about 156 Kbytes are required for overhead. Thus, about 100 Kbytes are available for caching with the 256-Kbyte RAM. When a request for disk access comes in, the server checks to see if it can be handled from cache. If it can, disk access is

about 1 percent of the time required to go to hard disk.

The Dimension system caches one track of 17 sectors (8½ Mbytes) at a time, on the theory that a program that uses one sector is likely to use adjacent sectors. When the cache is full, the server clears out the least recently used track and makes room for a new track. Corona's Mega PC system provides caching only if 512-Kbyte RAM is provided in the server. In this case, a separate disk cache board is provided. According to Corona, average disk access time is four times faster if the board is installed.

Both systems claim a substantial price advantage over IBM PC networks. Both cost less than $8000 for a basic, two-user system, with additional workstations available for about $1500. For a Mega PC system, $7805 buys a two-user system with 256-Kbyte RAM per user, and a 10-Mbyte hard disk drive. Each additional workstation costs $1495. Thus, a three-user system would cost around $9300. A PC AT with two additional terminals can be purchased for less than this. However, in this situation, users are time-sharing one 80286 processor. Also, the applications are different because the multi-user PC AT uses a Xenix environment.

Weighing the advantages

IBM's PC network, which can accommodate up to 72 PCs, XTs, or ATs, requires about $700 worth of hardware for each node. The cost of each computer is added to this. Of course, each workstation has its own local memory, a feature that is lacking in the North Star and Corona schemes.

Corona and North Star claim a performance advantage too. Corona claims its benchmarks show the Mega PC to be twice as fast as a comparable network of IBM PCs. Comparisons to the PC AT and the IBM PC network are not yet available. Despite the cost/performance claims of North Star and Corona, IBM will be a tough competitor in the multi-user market.

In fact, IBM's entry into this market is expected to set a number of *de facto* standards (see *Computer Design*, Oct 1, 1984, p 27). The question facing vendors like North Star and Corona is whether users will seek the security of the IBM label, or consider the alternatives that may not conform to future standards set by IBM.

—by Richard Goering, Field Editor

SYSTEM TECHNOLOGY

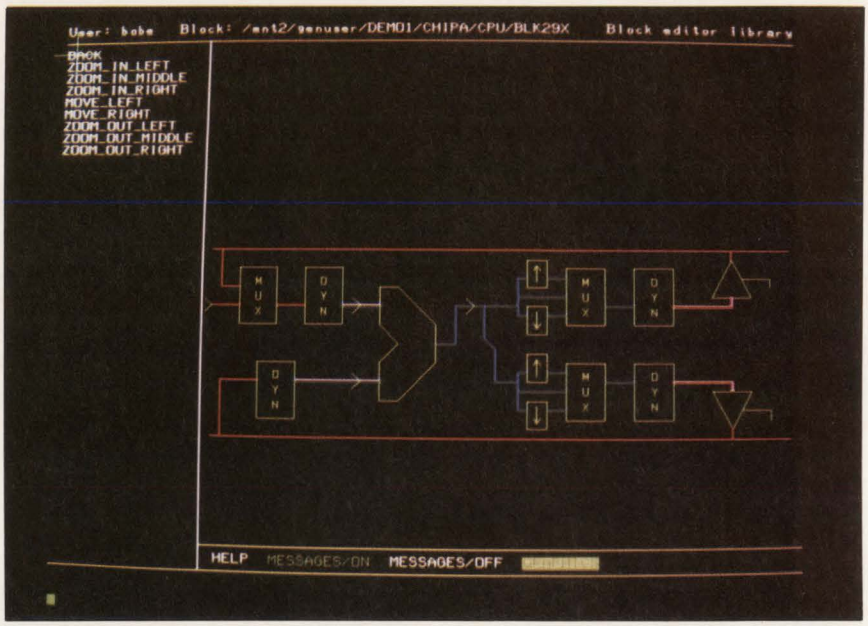
(continued on page 50)

Silicon compilation cuts costs of custom VLSI

There was a quiet revolution at work in the semiconductor industry last year, and its culmination was the MicroVAX computer chip introduced by Digital Equipment Corp. Although it was not widely known at the time, MicroVAX I was the proof-of-concept for a new design tool now known as "silicon compilation."

The MicroVAX design work was done at Silicon Compilers, Inc (Los Gatos, Calif) on its, at that time, unannounced Genesil system. The system, with its silicon compilation capability, enabled designers to complete the MicroVAX in six months. This is much less time than it takes designers of competitive microprocessors such as Intel's iAPX 80286. This chip was introduced at the same time as MicroVAX, but took several years to design.

Silicon compilation uses massive computing power to replace many of the semiconductor designer's skills. Thus, it allows a system designer, who has no specialized knowledge of IC design, to define a system that will eventually be reduced to one or more custom ICs. It allows calculation of IC size and production costs without circuit redesign. In addition, each design can be modified to fit because the design rules of several foundries can be input to the system.



The silicon compiler's block editor permits top-down design of onchip logic beginning with simple block diagrams, if that is where the designer chooses to start. Graphic representations are automatically translated into required geometrics for VLSI fabrication, and there is a library of functional cells that can be called. Each design level has preselected default circuits that the designer can optimize, discard, redesign, or use without modification.

Saving skilled labor

Companies that do not convert to silicon compiling are going to be at a serious disadvantage in the near future. Custom VLSI designs are becoming too expensive to be approached any other way. The final development stage of a custom IC, the layout phase, is the most labor-intensive. Constant reiterations of the timing and logic simulations required to verify each "tweak" of the chip are a huge drain on most projects.

Heavy demand for skilled labor time has forced many companies to use the standard-cell or gate-array approach of semicustom ICs. This choice is not always best, but it provides chips faster than the fully custom approach. Many experts feel that if layout could be automated, then custom ICs could become a more viable development tool. Most skilled IC designers agree that compilation of a system or circuit design directly to silicon will happen eventually.

The Genesil system supports four designers from first concept through silicon layout in a hierarchical system design. In addition, it checks each design step for correctness. This makes it practically impossible to design a bug into the system because each step is checked for its impact on other parts of the system.

Design rule verification

During layout, a complete set of design rules for the specific process and IC manufacturer is used. Violation of the design rules is not allowed. Up to four processes can be verified simultaneously, allowing the designer to check between them to see which system allows the smallest die size.

The Genesil system is not restricted to designing one IC at a time. Designers can begin with the complete system, regardless of the number of chips required for a full implementation. In the event that more than one chip is required for the system, designers are able to continue interactive design of the entire chip set. Thus, system partitioning (interconnections between the chips and other optimizations) can be done during the early design phase and monitored or changed at any point in the design cycle.

Genesil is aimed at all system designers (not specifically IC designers) and has a Digital VAX-11/750 with a 1600-bit/in. tape drive, 450 Mbytes of disk storage, up to four color graphics stations (1025- x 768-pixel resolution), and design automation software packages. These packages include IC definition, functional simulator, timing analyzer, place and route, testout, and tapeout.

Currently, the software package only supports NMOS chip designs. In the first quarter of next year, a CMOS function set that will be directly

(continued on page 52)

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Silicon compilation

(continued from page 50)

interactive with the NMOS function set, is expected. This will permit conversion of NMOS designs into CMOS circuits. IC design functions for both systems fall into six categories: memory, complex logic, data path, random logic, pads, and test. Memory functions offer blocks including RAM, ROM, first in, first out buffers, and stacks. Complex logic functions include PLAs, decoders, and encoders, while data path functions allow parallel data paths from 4 to 32 bits wide.

Top-down design

Compared to previous approaches, Genesil is a more hierarchical design environment. Designers can start at any design level. Logic and timing can be verified at any stage through more and more detailed iterations. A system architecture can be developed during the design process. This is different from the method used at VLSI Technology. That company's method provides cell compilers to assist in detailed layout of silicon patterns but requires that most of the system design be completed prior to the start of the IC design. Treating the IC as a subsystem does not allow the same design freedom or rapid movement from system-level design to completed silicon.

Random logic functions allow the user to compose lower level functions such as NAND and NOR gates or flip-flops for simple signal inversions, gate buffering, or control signals. This provides direct access to the design's gate level, which is normally hidden in the other Genesil functions' block level design.

The Pad function is used to construct the pad blocks that provide offchip connections. Test functions allow designers to include test blocks within the IC design. Two separate functions are provided—level-sensitive scan device (LSSD) and Interblock Scan Path. In LSSD, users create a test strategy that converts sequential circuits into combinatorial circuits by setting all of the sequential nodes so that test vector generation can be used. The Interblock Scan Path improves the controllability and observability of the internal paths. This yields a built-in test strategy in which the interblock registers are configured as linear feedback shift registers. These registers translate incident test patterns or compress test results into a signature that can be scanned.

Proven concept

How well does all this work? Over the last few years, Silicon Compilers has proved its methodology in a series of projects. The first was the Ethernet datalink controller now being used by Seeq Technology. Silicon Compilers claims that this is the first such product on the market, despite the fact that Intel spent two years on its version before Seeq work even began. The second was a dynamic raster controller chip now used in Sun Microsystems, Inc's engineering workstations. The third, and probably most impressive project was the MicroVAX I. This 32-bit VLSI computer system chip has 98 to 99 percent of Intel 80286 chip's density.

Yet, designers are not apt to rush out and buy a Genesil system without some serious consideration. It is priced at $545,000, or close to $140,000 per user. This is almost 50 percent higher than other workstations presently on the market. However, the capabilities and labor savings are also higher than other workstations intended for gate-array or standard-cell VLSI design (eg, those from Daisy, Metheus, and Mentor). But, when many designers are literally betting their company's future on the next product line, the corporate decision makers may be forced to pay the higher price.

—Bill Furlow, Senior Editor

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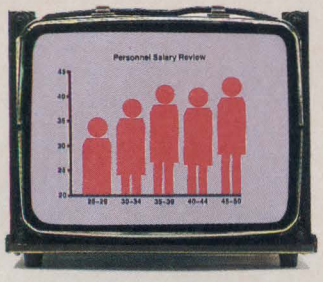

Administration

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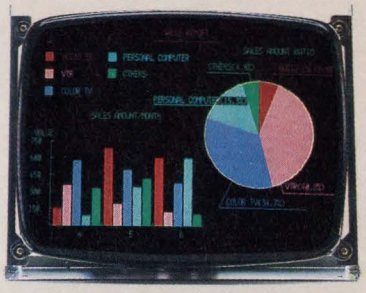

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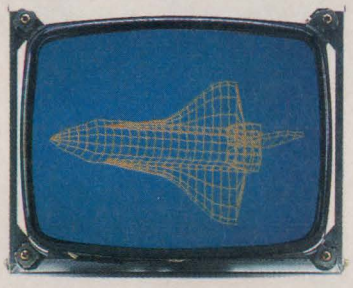

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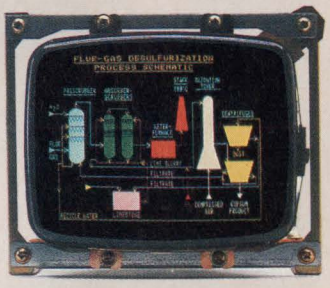

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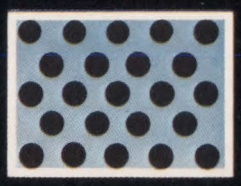
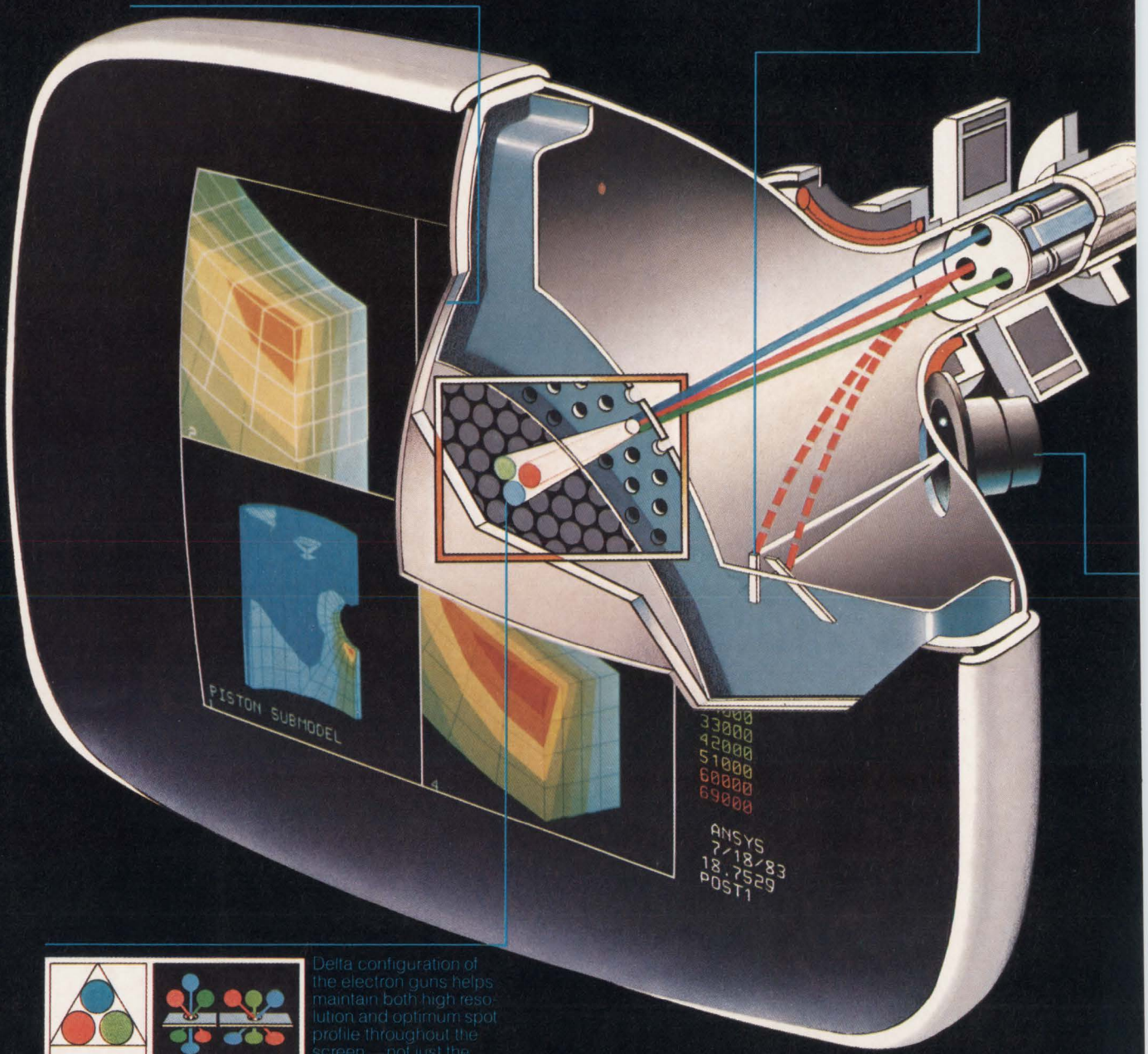
An aluminum layer between the shadow mask and the screen reflects light from the phosphor dots out toward the viewer and at the same time prevents errant screen light from reaching the photodetector.



The 4115B's patented AutoConvergence is accomplished by applying non-parallel indexing phosphors at precise angles and positions at the rear of the CRT shadow mask, detail at left.



Delta configuration of the electron guns helps maintain both high resolution and optimum spot profile throughout the screen — not just the center.

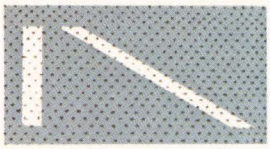
Tektronix.

The higher the visual resolution of a color display, the more difficult it becomes to converge the color beams at a precise point.

Yet, without precise control of convergence, productivity gains promised by high resolution graphics simply can't be realized.

That's why Tek designed the 4115B with AutoConvergence as our engineering prerequisite.

The engineering work environment is tough on high resolution displays. A shift in display angle for better viewing. Mild vibration from a stray elbow. Minor temperature change. Circuit drift. Tube aging. The earth's magnetic field.



A photodetector picks up light from the indexing phosphors. A microcomputer then compares instantaneous beam positions with factory specifications. Convergence corrections are generated to make the two coincide.

They all can cause the color line blurring effects commonly called *misconvergence*.

Loss of detailed information, especially in corners. Fuzzy, fringed colors. And visual ambiguity. All of which can lead to user fatigue, error and loss of productivity.

Until the 4115B, manual reconvergence was typically up to an hour-long task for a service technician—resulting in even more lost time.

No wonder most display manufacturers won't talk about the problem. But Tek will. Because we solved it with our exclusive AutoConvergence.

Push one button on the 4115B and all three electron guns are converged automatically. In 20 seconds. Not just in the screen center but from corner to corner.

Convergence accuracy is within .25mm, as compared to the 0.3mm to 1.0mm achievable by manual or other techniques. There's no interruption to work, so there's no loss of productivity.

The 4115B's high performance doesn't stop with AutoConvergence. It just begins there. You can apply its 60 Hz non-interlaced, 1280 x 1024 display, 50,000 vector/second redraw speed and user selectable 32-bit coordinate space to optimize productivity on any application.

Large area fills are accomplished at 125 million pixels per second. Standard host communications is 19.2K baud.

So if you want to start with the highest resolution and work at your best all day, every day, call your Tek Sales Engineer. For literature or the location of your local Tek sales office, call toll-free:
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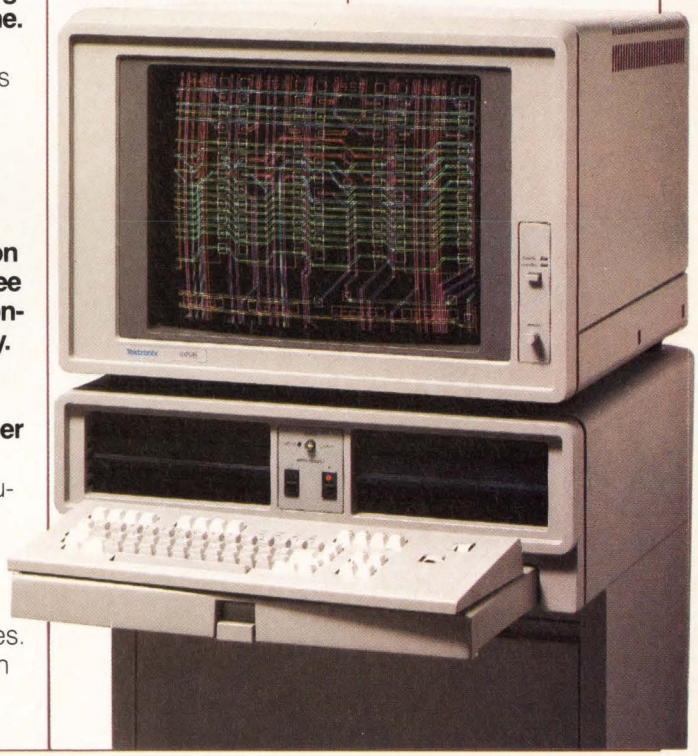

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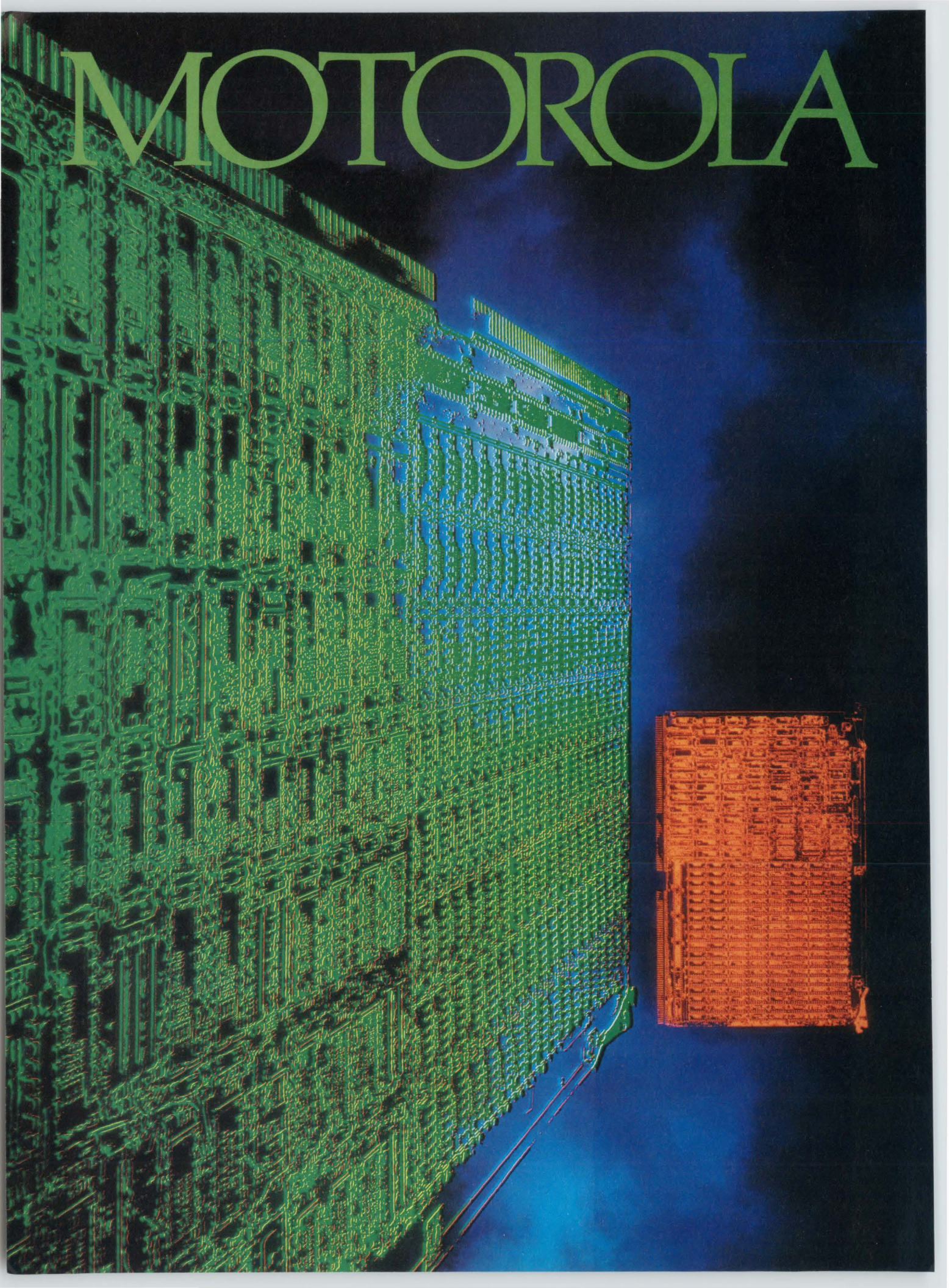
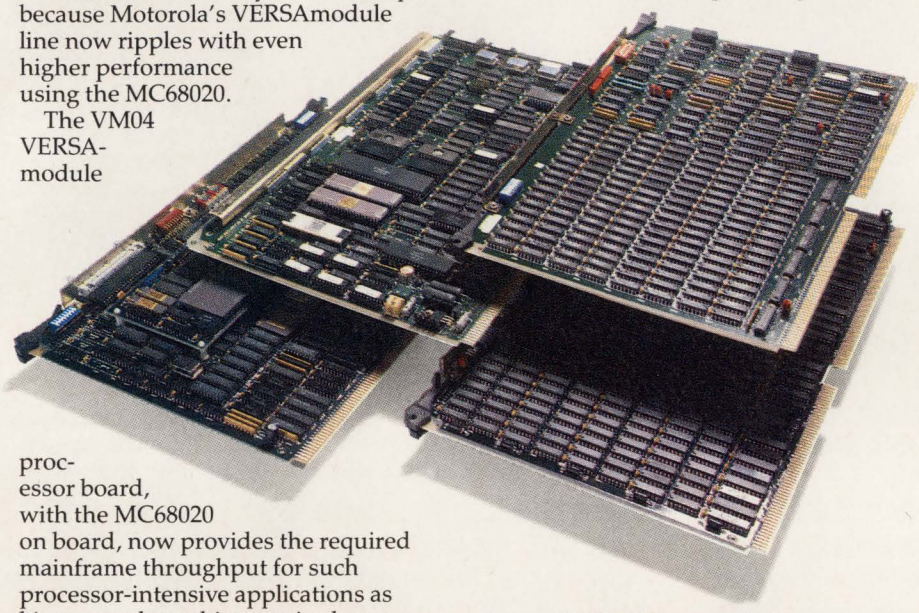

MOTOROLA

Challenge the mainframes.

VERSAmodules™ now run the MC68020, true 32-bit performance standard.

VERSAmodule microcomputer boards have already proven themselves in performance-demanding communication, industrial, laboratory and imaging applications. You knew these boards were powerful workhorses before, but hold on to your bootstraps, because Motorola's VERSAmodule line now ripples with even higher performance using the MC68020.

The VM04 VERSAmodule processor board, with the MC68020 on board, now provides the required mainframe throughput for such processor-intensive applications as bit-mapped graphics manipulators, scientific data acquisition systems and artificial intelligence machines. Applications that, before this, required mainframe machines.



Gaining speed, adding power, lowering overhead.

The new VERSAmodule VM04 processor board can access more than 4 billion bytes of data and manipulate or process 32 individual pieces of information every 180 billionths of a second (180 nanoseconds). Measured in millions of instructions per second (MIPS), the VM04 operates at a sustained rate of 2 to 3 MIPS, with burst rates exceeding eight MIPS, challenging the speed of some mainframe computers.

16K bytes of instruction/data cache on-board help reduce off-board memory accesses to ensure top performance. When off-board access is needed, the VM04 calls on the interface capabilities of Motorola's MC68020-specific RAMbus™ to eliminate most arbitration overhead and speed memory transfers.

The VM04 monoboard is the first MC68020 processor board to offer paged memory management hardware, plus an interface to support the soon available MC68881 floating point math co-processor.

These new modules add to a broad offering of board-level products including processor, memory, controller and communication modules with complete evaluation and development systems.

Broad VERSAmodule line.

Two new high density memory boards have been added to the line to complement the MC68020-based monoboard.

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The VM13 dynamic RAM module provides 1 or 4 Mbytes of random access memory dual ported to both RAMbus™ and VERSAbus.™ A perfect system mate for the VM04 32-bit monoboard, the VM13 has error detection and diagnostic capability.

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A choice of real-time and whose-time-has-come operating systems.

The VERSAmodule Family is supported by both of Motorola's M68000 operating systems: the VERSAdos™ operating system for real-time applications, and the SYSTEM V/68™ operating system where a UNIX™ operating system environment is desired.

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Continued Motorola support.

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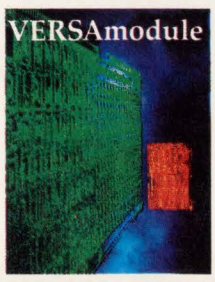

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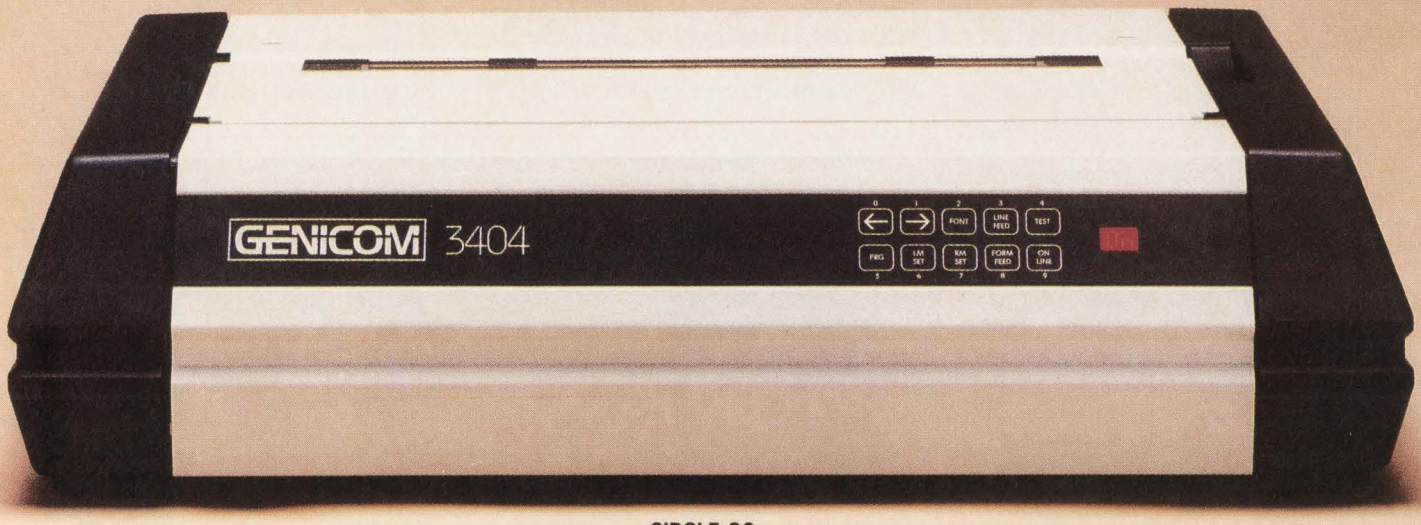


CIRCLE 30

SPECIAL REPORT ON

DIGITAL SIGNAL PROCESSING

Real-world signals are analog in nature. Unless quantum theory is considered, these signals are well represented by continuous waveforms whose Fourier transforms are also continuous functions. In recognition of this relationship in the 1920s, the first filters developed for removing unwanted signals from telephony transmissions were analog devices. Some of the first practical computers that Massachusetts Institute of Technology researchers and others experimented with in the 1930s and 1940s were also analog. These computers depended on variable resistors, inductors, and capacitors, as well as on tube-based amplifiers to simulate differentiation and integration.

Today, digital computers perform most calculations, even though analog technology still provides a great deal of the filtering functions that most practical communication and computer systems need. Matters are changing rapidly, however. For example, digital filters are replacing the basic analog signal processing device—the analog filter. Filtering is the most rudimentary signal processing chore that is, nevertheless, a kind of signal processing. It consists of the conversion of a signal or waveform, regardless of its nature or shape, from one amplitude and phase distribution as a function of time—or frequency—to another, usually more desirable distribution.

In a practical system, filters and other kinds of signal processing elements combine to perform certain chores. These may be mathematical in nature, including correlation and multiplication. The mathematical chore may be part of the implementation of some algorithm for speech recognition, image enhancement, spectrum analysis, high speed calculations, and a host of others. Limitations of analog technology, including precision, reproducibility, price flexibility, reliability, size, and power consumption, have prevented widespread adoption of such systems, however.

Spurred by the development of VLSI technology, digital signal processing is making its mark in the electronic systems world. VLSI-based DSP is combining with a wide variety of algorithms and their software implementations to perform signal processing chores uniformly among processing units and without analog's disadvantages. Development tools are also appearing, with the personal computer functioning as a design aid.

The industry is working overtime to develop the chips, algorithms, software, and subsystems that computer designers link together to make DSP-based systems. Standards are being discussed, new applications are evolving, and the industry is realizing that DSP need not be solely the expert's domain—even though it requires a degree of mathematical precision to use properly.

The following article provides an overview of these developments. It is geared to the novice because most computer designers are unfamiliar with DSP technology. But it also covers much material for the initiated. The overview lays the groundwork for the contributed articles that follow. These concentrate on recent and anticipated product introductions. They offer computer system designers and integrators a good idea of what to expect for their DSP designs during the next couple of years.

Harvey J. Hindin

Harvey J. Hindin
Special Features Editor

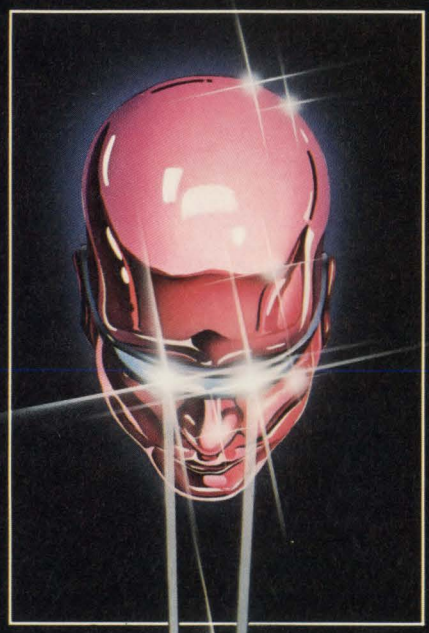
The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance.

Without complex adjustment electronics . . . and none of the convergence drift inherent in active correction systems. At last, high resolution in-line tubes with stable performance that stands up to the ravages of time and tough office/industrial environments.



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The achievement of Panasonic high resolution in-line color CRTs.

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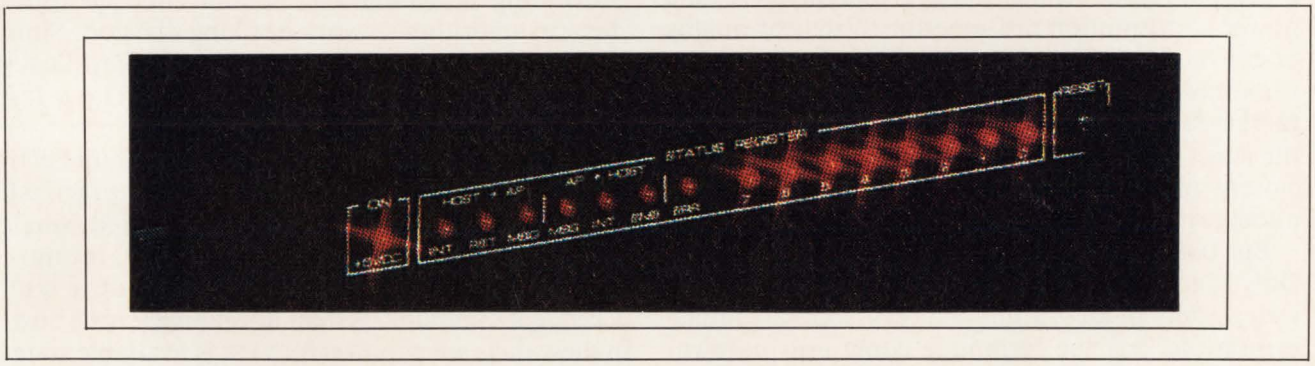
CIRCLE 31

DIGITAL SIGNAL PROCESSING MOVES INTO HIGH GEAR

VLSI chips, software development tools, and algorithms now handle a variety of computer design applications.



Harvey J. Hindin,
Special Features Editor

Software, algorithms, development tools, VLSI, and subsystems are combining to speed the use of digital signal processing techniques. This acceleration is especially apparent in such compute-intensive chores as image enhancement, speech recognition, and spectrum analysis. And, they are all available at ever-lower cost and offer higher reliability.

Many, if not most, designers are far more familiar with analog technology or the digital VLSI chips and general-purpose microprocessors at the heart of today's computer systems. The world of special-purpose microprocessors oriented to digital signal processing (DSP), and the realm of support chips geared to implementing some compute-intensive function by means of a specially designed mathematical algorithm, is strange to them. To do their jobs properly, however, computer systems designers and integrators need to know that DSP is, and what it can do for their systems. Then they need to know what new DSP functions they can expect in the next year or two.

As DSP becomes more flexible and widespread, both analog and digital designers will have to make more choices between different DSP components and subsystems. They will also have to decide, early on, if they should opt for the DSP approach.

Getting started

Today, digital computers perform most calculations; but analog technology still provides a great deal of the signal processing functions that most practical communications and computer systems need. However, matters are changing rapidly. For example, the basic analog signal processing device—the analog filter—is being replaced by digital filters. Filtering is the most rudimentary signal processing chore but it is, nevertheless, signal processing. It is the conversion of a signal or waveform, regardless of its nature or shape, from one amplitude and phase distribution as a function of time (or frequency) to another, usually more desirable distribution.

A great part of DSP technology depends on the use of a variety of digital filters. For example,

practical implementation of most algorithms requires a number of filters. In a practical system, filters and such other signal processing elements as microprocessors, multipliers, address generators, A-D and D-A converters, and correlators combine to perform most chores.

These chores, often highly mathematical in nature, include waveform correlation, matrix inversion, Fourier transforms, multiprecision, and floating point arithmetic. The mathematical chore may be part of an algorithm for speech recognition, image enhancement, spectrum analysis, or high speed calculations, for example. Some of these applications are suitable for single-chip DSP implementations that use a dedicated microcomputer. Others are geared more to subsystem or system implementations in the form of DSP units known as array processors.

As the experienced designer expects, overlap exists between the various design approaches—dependent upon the application and its specification. DSP is chosen for all the applications, however, because its precision, reproducibility, price, reliability, size, and power consumption are superior to that of analog or conventional digital systems. Most important, in some cases, DSP technology is the only way the job can be done. And, DSP has an added benefit. Unlike the case with many analog systems, DSP theory closely predicts what happens in actual systems undergoing tests.

But DSP has harbored these advantages for years. Only since VLSI-based DSP has combined with a wide variety of algorithms and their software implementations has the technique come into its own. DSP development tools are also appearing, with the personal computer functioning as the heart of the design support system.

Since the swing to DSP started, designers have been working overtime to develop even more of the chips, algorithms, software, and subsystems that comprise DSP-based systems. The industry is discussing standardization, and is pioneering applications. And it is finding that DSP can be used by novices as well as experts. One aspect of DSP that remains primarily in the expert's domain, however, is algorithm development. Computer scientists and mathematicians are cooperating more and more to overcome the limitations algorithms present.

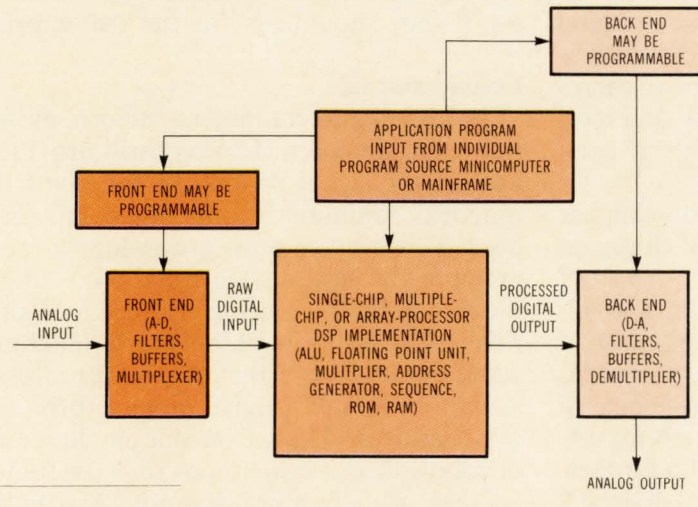
How to calculate

Algorithms provide the mathematical structure at the heart of DSP. The word itself derives from the name by which ninth century Arab scientist/mathematician/astronomer Mukhammad ibn Musa was known—al-Khorezmi. (This name was taken from the empire northeast of modern day Iran from which he came.) Because of his work with mathematics, "al-Khorezmi" became the name for the procedure called an "algorithm."

An algorithm is simply a mathematical rule for performing a calculation. School children use a classical algorithm to work out long division. Similarly, computer designers use the Cooley-Tukey algorithm—developed in 1965—to calculate a fast Fourier transform.

The recent strides in constructing ever-more efficient algorithms have helped make DSP practical. When coupled with the ability of dedicated, single VLSI-based chips to implement algorithms, the most complex calculations can become part of a DSP-dependent computer system at relatively little cost. In these days when powerful VLSI is available so inexpensively to all comers, the superiority of any one system design is often a matter of algorithm design.

Calculations that can be performed more efficiently provide benefits including faster realtime systems and better image enhancement, for example.



Depending on its functions, a digital signal processing (DSP) system usually has an analog input subsystem (front end), a back end, and a processing unit. The latter contains a dedicated computer implemented in a single- or multiple-chip, or a multiple printed circuit board design.

TABLE 1

Applications of Digital Signal Processing

Numeric processing	Signal processing	High speed control
Fast multiply/divide	Digital filtering	Servo links
Double-precision operations	Correlation	Position and rate control
Fast scaling	Hilbert transforms	Motor control
Nonlinear function computation (ie, sin X, e^x)	Windowing	Missile guidance
	Fast Fourier transforms	Remote feedback control
Instrumentation	Adaptive filtering	Robotics
Spectrum analysis	Waveform generation	Telecommunications
Digital filtering	Speech processing	Adaptive equalizers
Phase locked loops	Radar and sonar processing	μ/A law conversion
Averaging	Electronic countermeasures	Tone generators
Arbitrary waveform generation	Seismic processing	High speed modems
Transient analysis	Speech processing	Multiple-bit rate modems
Image processing	Speech analysis	Amplitude, frequency, and phase modulation/demodulation
Pattern recognition	Speech synthesis	Data encryption
Image enhancement	Speech recognition	Data scrambling
Image compression	Voice store and forward	Digital filtering
Homomorphic processing	Vocoders	Data compression
Radar and sonar processing	Speaker authentication	Spread spectrum communication

The bible on algorithms for computer use is, of course, Donald E. Knuth's (of Stanford University) *The Art of Computer Programming, Volume 2: Seminumerical Algorithms* (Addison-Wesley, 1981). The latest words are found in research journals and company memoranda and these publications show that even classic algorithms get better.

Algorithm applications

The digital filters seen so often in DSP systems are either nonrecursive digital filters—known as finite impulse response (FIR) filters, or recursive digital filters—known as infinite impulse response (IIR) filters. The FIR is the most commonly used design. It may be implemented as a straightforward tapped delay line in which the input data stream is convolved with data from weighted filter taps. The appropriate configuration of delays and taps implements the filter I/O relationship needed for a particular DSP system; the output signal can be expressed as various sums and products of the input signals.

Such a straightforward design approach is valid when the number of taps and delays is of no concern. Other designs, keeping half or more of the number of parts (a typical FIR filter may have hundreds of taps), are based on approximations of the very long string of input and output digital signal samples.

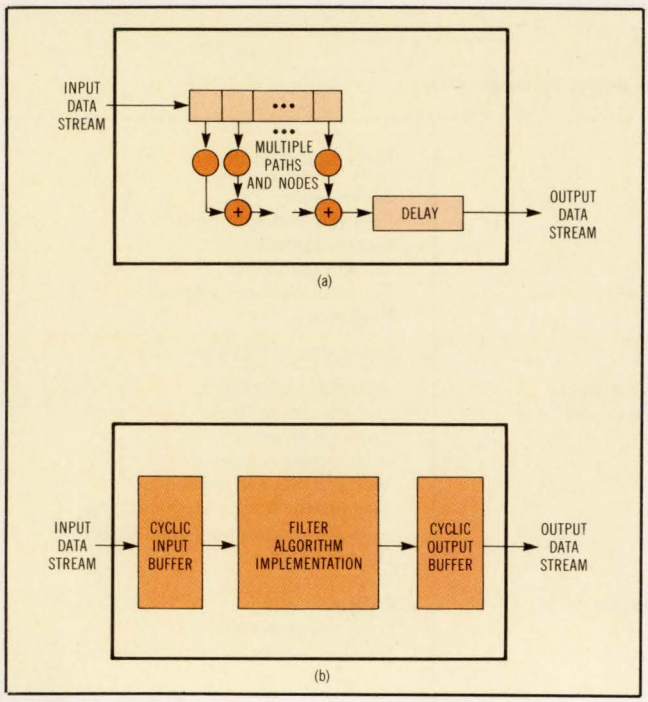
These result in "fast" algorithms for implementing FIR filters. They are fast because their implementation substitutes additions for multiplications. A complex number multiplication such as $(A + jB)(C + jD) = E + jF$ can be calculated as $E = AC - BD$ and $F = AD + BC$, or as $E = (A - B)D + A(C - D)$ and $F = (A - B)D + B(C + D)$. The first requires two additions and four multiplications, while the second uses four additions and only three multiplications. Note that an elaborate, fast algorithm may represent a nonrecurring design expense which may or may not be justified for a particular DSP application. The DSP computer designer must ponder this and make a judicious trade-off between cost and efficiency.

Algorithms are also used in the actual implementation of FIR filters. For example, the equiripple approximation is known to result in the lowest order filter able to meet a given I/O specification. The Parks-McClellan algorithm allows for equiripple FIR designs that may be implemented on mainframes. Or, the designs may even be done on an IBM or Texas Instruments (Dallas, Tex) personal computer using DOS operating system-based software.

In Atlanta Signal Processors'(Atlanta, Ga) design approach, the filter order and the edges of the passband and stopbands are fixed. Moreover, the FIR filter coefficients are systematically varied so that an equiripple behavior is achieved in each approximation band. The algorithm terminates when this is achieved. An alternative algorithm is the so-called Kaiser-window method. It trades off filter order, ripple magnitude, and the filter passband-to-reject-band transition region size. It is important that a wide variety of algorithms and computers handle the design of both IIR and FIR filters since they are the basis of most DSP systems.

Faster and faster

The classic continuous Fourier transform is in the repertoire of every electrical engineer who ever needed to find the frequency domain equivalent (magnitude and phase) of a time domain signal, and



Trellis searching is an important DSP task with many applications in computer-based systems. Functionally, the trellis is a finite impulse response filter with thousands of taps (a). It has many applications (b)—tracing the signal flow is the problem.

vice versa. It has a discrete analog—it is both meaningful and possible to find the alternative domain equivalents of discrete time or frequency signals.

The discrete Fourier transform is the most performed DSP operation, and processors of all sizes attack it in every DSP application. It used to be a costly (in computer time) operation. But, matters improved greatly in 1965 when the fast Fourier transform (FFT), a quick algorithm for computing the discrete Fourier transform, was developed by Cooley and Tukey. Depending on the application, a transform could be done in .01 of the time it took before. This made practical some Fourier transform-intensive systems that could not be designed before.

Other recently developed algorithms have reduced the time even more. All are rather complex. And, as in the case of fast FIR algorithms, an engineering design trade-off must be made between whether or not to use them. Certain systems for national defense, for example, will use the brand-new Winograd algorithm for FFTs to gain that last extra rush of speed. Under certain conditions it is particularly good at reducing the number of multiplications needed in a transform. But it is difficult to understand and use in designs.

Other algorithms

A wide variety of specialized algorithms exist for particular DSP problems. For example, the so-called trellis searching is a useful technique for decoding convolutional codes, demodulating signals with intersymbol interference, and is good for text, character, and voice recognition. Such algorithms as the Viterbi algorithm, used to implement trellis searching in FIR filters, require the efforts of mathematicians, computer scientists, and DSP designers to understand, implement, and use.

The purpose of a trellis search is to define the path through a digital network or filter that most closely approximates how a given set of discrete network input signals is converted into an output signal set. The straightforward "method of exhaustion," wherein every possible path "through the trellis" is tried, simply uses too much processor time (growth is exponential with trellis size). Again, a "fast" algorithm is needed and the Viterbi algorithm is a practical one.

Experts needed

Algorithm research is making its mark in more efficient DSP systems, but there is much to do. The problem, says IBM fellow Richard E. Blahut at IBM in Owego, NY is that "algorithm understanding is not widely disseminated." Blahut is the author of the basic work *Fast Algorithms for Digital Signal Processing* (Addison-Wesley, 1984). Moreover, other industry gurus say, algorithm work is just plain difficult, requiring high level skills not seen in the average engineer. Key algorithm work and much algorithm development is going on in the general categories of data compression, compaction, encryption, transmission encoding, and translation to meet the needs of a variety of DSP applications, according to Blahut. For example, new vector quantization algorithms can now compress speech to a few hundred bits per second. And, Blahut maintains, modern data compaction codes are such that neither the encoder or decoder needs any knowledge about the information to be compacted.

There are many algorithms for computer data transmission. For example, the Reed-Solomon code (also an algorithm) corrects data errors due to noise or purposeful interference. The military and commercial applications are vast. A computer-controlled communications system can operate in a hostile environment with minimal degradation and a DSP-based computer system can be sure of the purity of its input data. Reed-Solomon data decoders depend on, among other algorithms, the FFT. Finally, note that many data transmission codes used by computer designers for secure or low noise transmissions require trellis searching with the Viterbi algorithm.

The "regularity" of an algorithm is as important as its low number of multiplications. In other words, for cost-effectiveness in algorithm implementation it is best to implement the algorithm structure on a VLSI chip. This means that both the chip and algorithm architectures must be regular and matched.

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CIRCLE 32

Algorithms that require substantial internal chip variations are expensive, if not impossible, to implement in silicon.

Industry experts agree that the most significant advances in fast algorithms will come when DSP chip architectures are developed jointly with algorithm architectures. This is no easy chore. It requires marrying two formerly separate technologies.

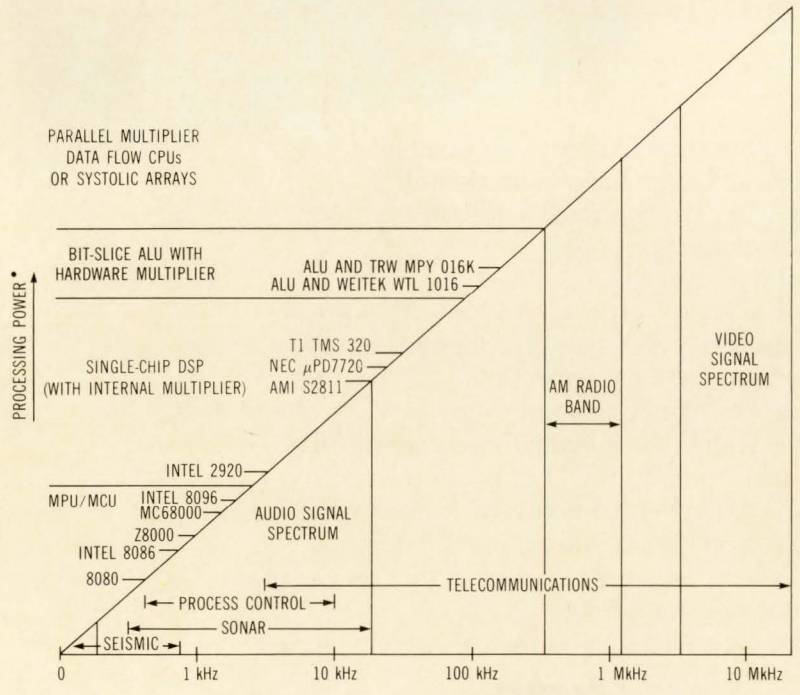
Matters are made even more complicated by the development of new DSP chip architectures. For example, the data flow architecture in the NEC (Natick, Mass) μPD7281 DSP chip—with its advantages over the traditional von Neumann computer architecture—should stimulate the development and implementation of some novel algorithms. These algorithms could speed some of the chip's chores including image and numerical processing (see "Data Flow Chip Optimizes Image Processing," p 97 in this issue). And, the systolic arrays that will ultimately appear in DSP design will also need their own brand of algorithms (see "Paralelism Makes Strong Bid for Next Generation Computers," *Computer Design*, Sept 1984, p 104).

Silicon riches for DSP

There is a wide variety of VLSI-based chips suitable for signal processing applications, some of which have been around for several years. Only now are their applications showing rapid growth, however, as the various DSP factors come together. It is difficult to classify the niches into which these chips fit, largely because many trade-offs exist between applications served, processing power, speed, and other DSP system design parameters specific to a particular case.

At the low end of the signal frequency spectrum, standard microprocessors are being designed to serve as DSP devices. There is no magic to this. A DSP chip is a microprocessor (microcontroller) dedicated to the DSP function. It usually has onchip RAM, ROM, an ALU (and perhaps hardware multipliers), registers that allow repetitive calculations much faster than processors not similarly equipped, and other DSP-oriented features. But, the general-purpose processor that is not similarly equipped can be used with auxiliary chips if medium to high end operation is not needed. Moreover, they may be easier to program since designers and software developers are more familiar with them. Motorola's 6800 and 68000 families seem to be a favorite among software designers. According to one study, they compete with TI's dedicated TMS32010 for the designer's attention—as do custom or proprietary designs geared for a specific application (often for the military).

A variety of chips such as the NEC device mentioned previously have been introduced recently or within the last year or so. Some are available as samples, some are in production, and others are in the planning stages. Where a particular chip fits in this categorization is a function of the size of the potential order, the customer's clout, and other variables



Some of the more readily available DSP chips based on a measure of processing power. Parallel multiply, data flow, and systolic architecture chips are starting to appear.

* BASED ON RAM MULTIPLY SPEED FOR 50-COEFFICIENT FINITE IMPULSE RESPONSE FILTER AND SAMPLE RATE OF 2x FREQUENCY

that the design engineer needs to investigate on a case-by-case basis. The new chips range from full-blown microprocessors and support chips dedicated to DSP applications through to multipliers which can be used for DSP or other chores, and to the A-D and D-A converters essential to getting the real world of analog signals into and out of a DSP system.

There are also a variety of "glue" chips. These provide the support details of a DSP system that a VLSI chip geared to some major function does not have room for. No nontrivial system calculates anything without them; and the designer cannot afford to ignore them. Fairchild Semiconductor Div (Mountain View, Calif) has made a name for itself by providing the DSP industry with fast glue chips. As almost always in the VLSI business, however, there are many suppliers.

Speed is most often the watchword in DSP systems. Either full-width microprocessors or bit-slice designs, in either MOS or bipolar ECL process technologies, respectively, have offered designers a choice. Of course, for highest speed applications, bipolar bit-slice design is the only way to go—and Advanced Micro Devices (Sunnyvale, Calif) makes what amounts to the industry standard (see "General-Purpose Board is Designer's First Step into DSP," p 81 in this issue. A variety of other firms provide such elements as support chips and pin-for-pin compatible chips.

Where a single chip implementation is called for, the NMOS process technology of TI's TMS320010 reduced instruction set architecture seems to be a favorite (see "Parallelism Makes Strong Bid for Next Generation Computers," *Computer Design*, Sept 1984, p 104). It blazes along at 5 million instructions per second (MIPS). It has plenty of competition from such Silicon Valley firms as Intel and American Micro Systems, Inc (Santa Clara, Calif), and such Japanese firms as Fujitsu Microelectronics, Inc (Santa Clara, Calif) and NEC. Many of these companies are traveling the low power consuming route offered by CMOS. In any case, everybody watches everyone else—for example, TI is looking into bit-slice designs and AMD is checking out CMOS.

Roughly speaking, MOS devices are superior to bipolar in component density and power consumption but inferior in speed. Today, CMOS is comparable to NMOS in both density and speed and superior in power consumption. As a result, it is getting a lot of attention (see "Circuit Density and Speed Boost Tomorrow's Hardware," *Computer Design*, Sept 1984, p 210). Gallium arsenide (GaAs), promising the highest speed of all, has yet to make its mark after years of advance publicity. Production samples of various GaAs-based DSP devices will not be available for some time. And, it will be years before GaAs devices appear in real DSP systems in quantity—assuming they do not have major cost, reliability, flexibility, specification, or other problems. Eight-bit GaAs devices will appear first.

Lately, power saving CMOS has begun to make its speed mark. For example, Analog Devices, Inc (Norwood, Mass) has come up with a set of four chips that together act as a 10-MHz, 16-bit slice, DSP system. For designers who need floating point calculations conforming to the IEEE's proposed standard for such matters, two new chips are available for 10-MHz fixed or floating point (single and double precision) arithmetic.

The differences between fixed point, floating point, or block floating point arithmetic in DSP systems are a major concern for DSP designers. The proper arithmetic choice is critical to system accuracy and precision, requiring a study of numerical approximation subtleties. These are thoroughly discussed in the proposed IEEE floating point standard. Although benchmarks are subject to the limitations of design and interpretation, they at least provide a starting point for the designer.

More on chips

The Analog Devices DSP chip set consists of a program sequencer chip, an address generator, an ALU, a multiplier-accumulator, and a floating point multiplier and ALU. General-purpose in design, none of the first four mentioned chips have architectures geared to specific algorithms, allowing designers to "roll their own." Although geared to 16-bit DSP, the chips can be cascaded to handle 32-bit applications.

As one representative of the latest in chip design, the set sports a high degree of integration of ancillary functions. In the past, these functions had to be furnished by glue chips in a real DSP system. Eliminating glue chips cuts down on board space and power requirements. It also speeds DSP algorithm implementation since chip-to-chip communication overhead is reduced. Analog Devices hopes that its CMOS set will be a tough competitor against the bipolar bit-slice architecture that has dominated high speed DSP applications. Other CMOS DSP chip manufacturers have the same goal.

The firm will not depend on speed alone to promote its products, however. For example, designers will be able to implement a so-called radix-4 FFT by using the chip set. This algorithm for the FFT has, to a large extent, been ignored by DSP designers. They have used the lower throughput radix-2 FFT for several reasons. For one, it is more well known and designers tend to lock themselves into using familiar or less complex algorithms. (Radix-2 is complex enough for most designers.) For another, it has been difficult to implement the radix-4 algorithm's complex computations in systems where cost is a major factor. Only the highest speed systems—for military applications in sonar and radar signature

TABLE 2

Benchmarks of Floating Point Arithmetic Processors

	Analog Devices ADSP-3210 ADSP-3220	Intel 8087
Effective throughput rate (Single precision floating point)	100 ns	19 μs (multiply)
Multiply/accumulate throughput rate	100 ns	37 μs
Input-to-output time	200 ns	19 μs
Power dissipation for multiply and ALU	800 mW	3 W
Double precision multiply throughput	500 ns	27 μs
Double precision add throughput	200 ns	18 μs
32-bit fixed point multiply throughput	100 ns	19 μs
32-bit fixed point add/subtract throughput	100 ns	18 μs
Package	96-lead PGA	40-pin DIP

analysis—have gone to radix-4 with its complicated, expensive, dedicated printed circuit boards full of silicon parts.

Designers continually face the problem of making the most clever choice of algorithms. Not only is the radix-4 method not used as much as it might (even with bipolar bit-slice logic), but some designers believe that FFTs must use multiples of 1024 data points in their calculations. This is just not true, however, as an analysis of the transform itself shows. A myth has developed that all calculations must be based on data block lengths with multiples of two.

Basic DSP

The DSP goal is to implement some algorithm as quickly as possible. The algorithm performs a repetitive calculation defined by some instruction set stored in the chips implementing the algorithm. The chips also hold the originally analog data that has been converted to digital by an A-D converter and whatever data (coefficients) are needed to implement the algorithm. To perform these chores, regardless of a chip set's process technology or its manufacturer, certain identical functions must be carried out.

The first chore—the calculations themselves—is performed by the ALU and a multiplier-accumulator (onboard or as a separate chip). The ALU might be aided by a fixed or floating point coprocessor and the multiplier-accumulator must be dedicated to multiplying (the DSP time-consuming operation) as fast as is practical.

These chips are controlled by a program sequencer that controls the flow of instructions to the calculating chips. Instructions handle the flow of addresses to the program memory, the program branching, interrupts, and all the functions common to any microprocessor system. The difference is that the sequencer must be fast—its overhead must be minimal when it does its assigned chores. This explains why a dedicated sequencer is often seen in DSP.

Finally, a typical DSP system algorithm requires rapid reads and writes of data and coefficients and a method for performing this chore with minimal overhead is necessary. Thus, most DSP systems need a dedicated address generator that specifies where data and coefficients are in memory.

Note that both high speed operation and high throughput are required and that the two figures of merit are not the same. The raw rate at which a calculation (or part of a calculation) may be performed must be tempered by how much useful work can be gotten through the DSP system. Once the chips in a system are put together, the needed glue chips added, and all the intra- and inter-chip communications and overhead taken care of, system throughput will decrease. So, mere reference to a faster process technology for chip construction, for example, is not the whole story; nor is raw instruction execution speed.

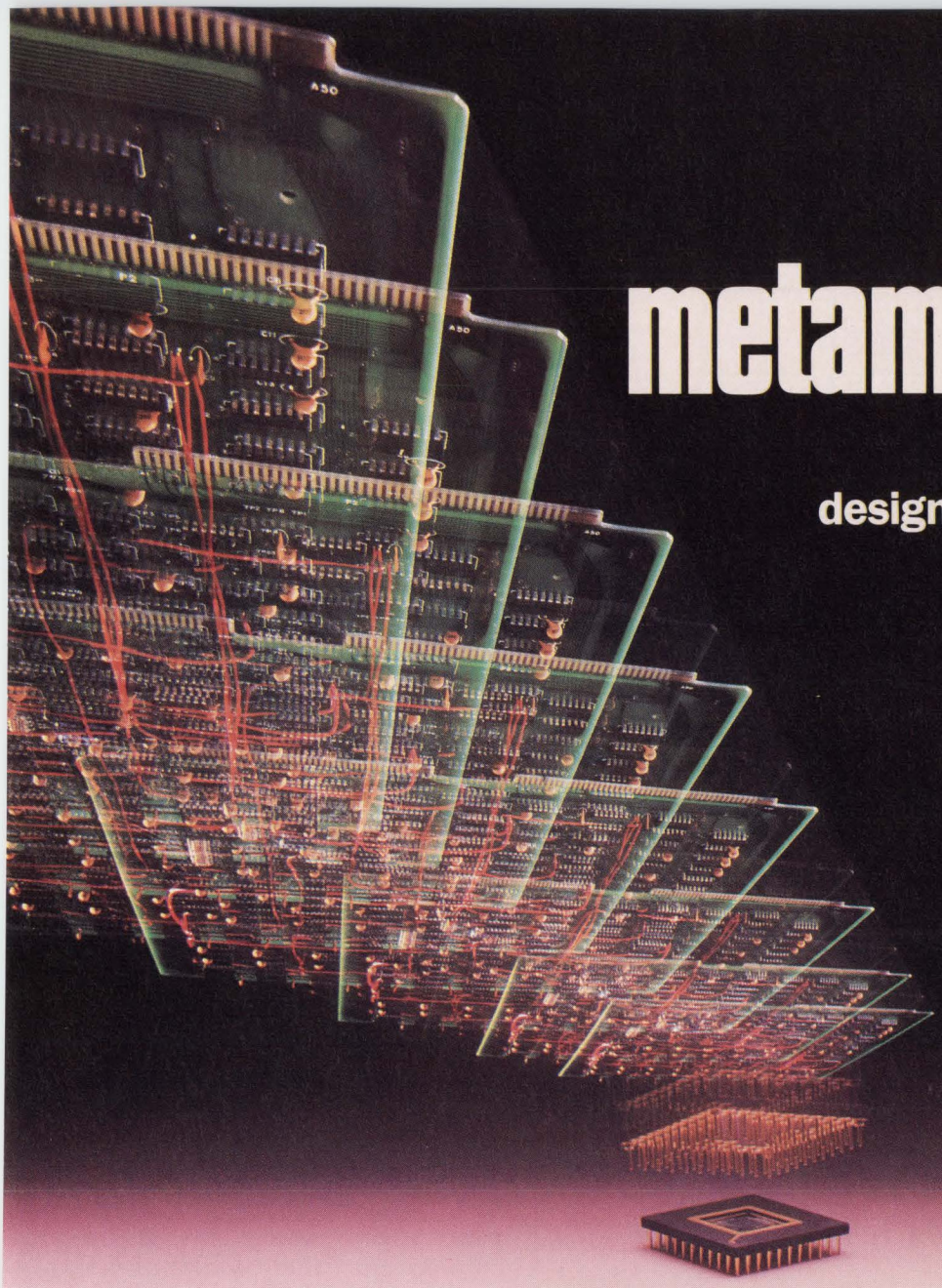
More problems

There are many other trade-offs that determine system throughput. For example, large data words may be handled by the DSP system. But, if they are handled in two or more parts because some system chip (or chips) cannot deal with them directly, a communication and overhead bottleneck may occur, wiping out the anticipated high throughput. (This would result from taking apart and restoring the large word.) Moreover, I/O bottlenecks or other inefficiencies could emerge in any design, regardless of its architecture.

DSP computer designers need to consider these bottlenecks carefully when configuring their systems. It is particularly important to make fair comparisons between alternative system designs. For example, dedicated DSP microcomputers, with all the mentioned functions on one chip, may indeed save power and board space and have the usual benefits associated with a single-chip implementation.

Compromises in the chip design may exist that allowed all the DSP functions to be put on one chip in the first place, however. These compromises might affect system throughput, the impact of which would depend upon the application. Thus, no substitution can be made for intelligent system design; relying on chip manufacturers who might not know about system problems can be dangerous.

Similarly, high performance bit-slice architectures (bipolar) are fast and flexible, but have their own set of trade-offs. Such trade-offs might include whether the DSP system must be general-purpose or algorithm-specific. For example, a bit-slice address



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Equivalent Gates	3500	1700	1500	1000	500	250
Typ. Gate Delay (ns)	.3 - .7*	.9	.9	.9	.9	.9
Typ. Power (W)	3.5	2.8	2.5	2.0	1.2	.6
I/Os	120	120	84	76	56	36
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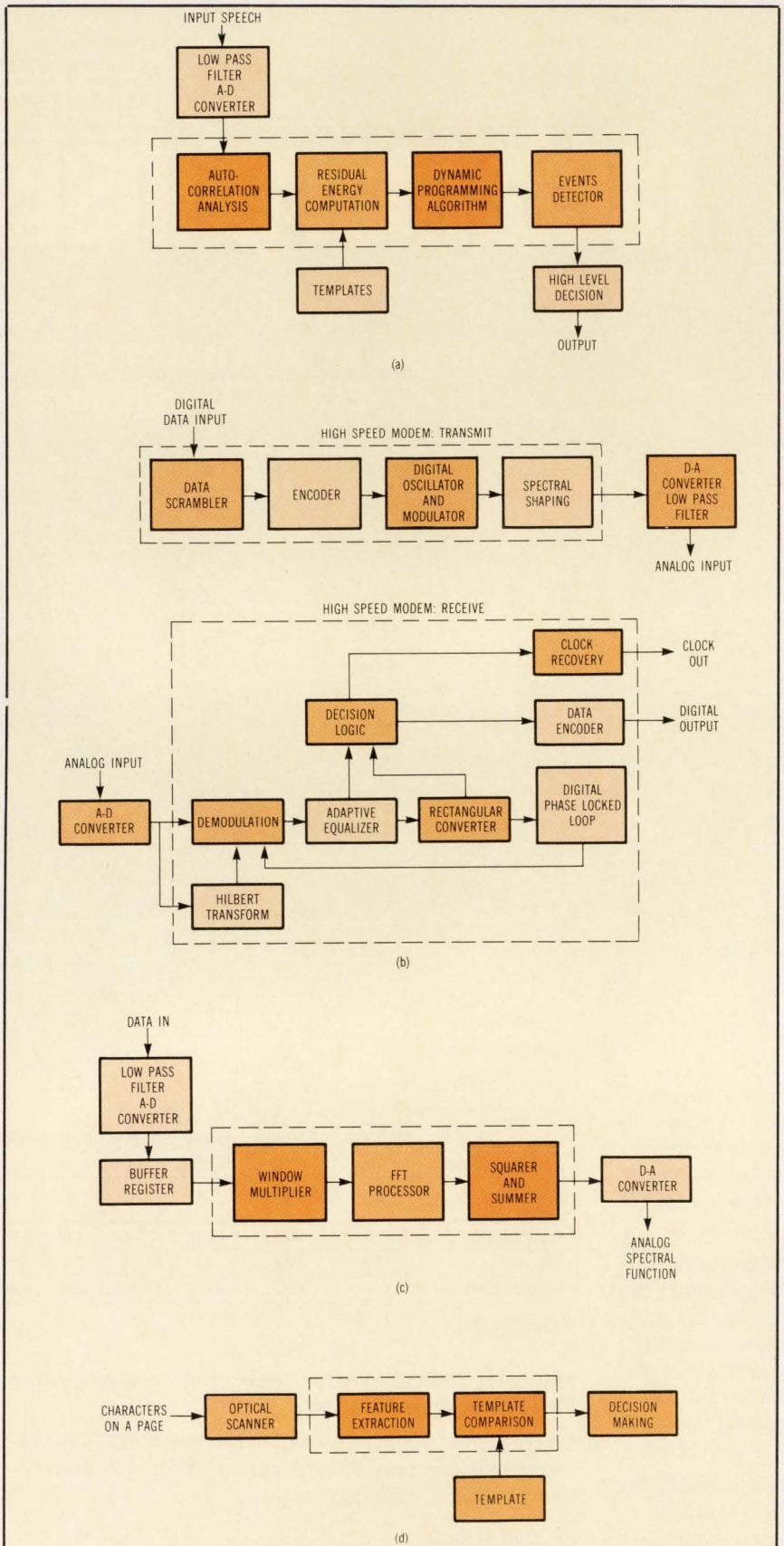


Single-chip DSP devices (denoted in figure by dotted lines) have a variety of applications in speech (a), high speed modems for transmit and receive (b), fast Fourier transform (FFT) based spectrum analysis (c), and optical character recognition. These systems are built around Texas Instruments' TMS320, but other processors may be used.

generator is often dedicated to one algorithm while implementing a general-purpose bit-slice address generator might require multiple chips. A full bipolar system might also consume too much power or space for the system designer's taste.

Current thinking has it that, for the ultimate in high end, high speed DSP applications, bit-slice is the only way to go. However, designers had better track closely such new architectures as the NEC data flow chip. Nevertheless, AMD is enjoying great success with its bit-slice set. AMD's set offers a multiport pipelined processor, and an FFT address sequencer for data and coefficients. It also has a single-clock 16 x 16 parallel multiplier with registers, two multilevel (dual two-stage or single four-stage) pipeline register (four 8-bit registers) devices, and a 16 x 16 parallel multiplier-accumulator. Many vendors are trying to improve on one or more of these designs or offer variations.

The designer with savvy knows that even DSP benchmarks are not the whole story. For example, a given FFT may be performed by one chip set as quickly as another. But, considerations including board space, power, cost, glue-chip count and availability, programming ease, upgradeability, availability, and the completeness of the vendor's line will swing the decision one way or the other. In fact, depending on what is important in the design, what can be tolerated, and what is just plain unacceptable, designs might call for a slower chip set. In the real world of computer design, the fact that a radix-2, 1024-point FFT may be completed in some number of milliseconds (or less) may not be the most important consideration.

Low electric bill

CMOS process technology is making its mark in a variety of DSP chip applications. And, as CMOS technology becomes more

pervasive in the VLSI world, DSP computer designers wonder if its low power consumption benefits will come to all the DSP chips. Since most DSP algorithms require multiplication and addition, and since fast multipliers based on bipolar process technology use up power, many designers could opt for CMOS—if the equivalent performance (or even close) was available.

One of the many firms looking into CMOS multipliers is Integrated Device Technology of Santa Clara, Calif. It has come up with a 200 mW, 16- x 16-bit multiplier pair that does its job in 65 ns. The chips can be set up in large multiplication arrays and are quite typical of what CMOS can offer.

IDT is by no means alone in this field. And, DSP designers need to carefully examine the trade-offs to be made in opting for a new vendor. For example, IDT's delivery capabilities may not be the same as those of another company having a complete DSP line. On the other hand, designers might be interested only in multipliers or IDT's other products and designers may be willing to mix and match vendors to supply parts for the system. Certainly, IDT's claim that its multiplier is as fast as the traditional bipolar design while consuming only half the power is a strong selling point. Designers concerned with supplying system power, coping with temperature rises in confined spaces, and other practical problems of a real system design will be listening.

Along with multipliers, there are a number of chips that satisfy the needs of a complete DSP system. Most of these are made by a variety of vendors. For example there are many possibilities for D-A and A-D converters. One of the latest of these geared to display applications is from the TRW LSI Components Div (La Jolla, Calif). Such chips are less glamorous than the elaborate and complex chips designed to implement algorithms. They are a necessary, indeed critical, system component, however. They can limit a DSP system's speed, throughput, signal-to-noise ratio, accuracy, precision, and more.

TI now offers a D-A and A-D converter set also able to perform such signal conditioning functions as anti-aliasing and sin(x)/x corrections. It also has such functions as control logic, serial data I/O and, first in, first out (FIFO) memory. The set can be used with most DSP processors. When it is used with TI's, however, it provides a programmable front end and back end for a DSP system. One reason for this is that its filters can be adjusted.

Still other DSP chip types have unique applications. For example, Logic Devices, Inc of Sunnyvale, Calif has a multiport register file. The firm offers a CMOS register file featuring eight, 8-bit registers (that can be combined for wider words), accessible by five parallel ports (to get at any register when the designer wants to). It is ideal for bit-slice devotees who are frustrated with a bit-slice architecture's relatively small external memory-to-ALU bandwidth (which limits the number of DSP operations that can occur in a given time period) and looking for a single-chip solution. It allows external data to be put into an ALU simultaneous with DSP algorithm operations and can speed DSP throughput.

As might be expected, AMD has a similar chip. Still another chip Logic Devices offers is a 16-bit CMOS microprocessor slice. It was designed to replace the comparable AMD chip with onboard multilevel lookahead carry generation capability. In fact, it is meant to use the same application software as the AMD chip.

Data flow moves in

A DSP chip that is radically different will be available soon from NEC Electronics Inc (Natick, Mass). NEC has eschewed convention and gone to the so-called data flow architecture for its design (see "Parallelism Makes Strong Bid for Next Generation Computers, *Computer Design*, Sept 1984, p 104). This design speeds image and numeric processing and allows chip cascading for even faster speeds. It is fully described in "Data Flow Chip Optimizes Image Processing," in this issue on p 97.

Along with multipliers, there are a number of chips that satisfy the needs of a complete DSP system.

The NEC design uses pipelining but abandons the classic von Neumann architecture for its calculating engine. In the von Neumann architecture, the CPU fetches instructions from ROM, and data from memory, for example. Each of these acts must wait until the previous acts are completed. In contrast, with the data flow architecture the CPU is data-driven. It responds to data's arrival by attaching it to instructions waiting for it in the CPU. Moreover, every instruction that needs the data is given it so no more than one fetch is necessary for a data "piece."

With this design, it is possible to perform a lot of parallel processing because events do not have to wait for previous events. As a bonus, up to a point that can be calculated, it is possible to speed matters linearly by cascading data flow chips. NEC claims 5 MIPS per chip and minicomputer performance for its chip in certain DSP applications. As is the case with other DSP chip architectures, however, careful system consideration determines the chip's practicality in a given application.

With a new architecture like data flow, the availability of software both for software development and algorithms is particularly important. NEC is well aware of this and is addressing the problem directly

with software aids. All major vendors, regardless of the kinds of chips or systems they offer, provide a variety of such aids. These include canned programs, third-party vendor-developed applications, detailed manuals, development toolkits, seminars, and emulators. They realize that DSP designers know that a "better" chip or system does no good unless designers can program them.

In a systolic array, an array has dozens, or ultimately hundreds, of identical processing elements that are hooked together for shifting data.

Taking a more traditional tack, but continuing the trend toward CMOS, another Japanese firm, Fujitsu Microelectronics has come up with a DSP engine. As one of the latest DSP engines, it features more onboard ROM and RAM memory, adjustable I/O, higher speeds rivaling bipolar devices, and all the evolutionary goodies expected from a VLSI firm's latest and greatest. The chip is not a bit-slice design, but is a rather complete DSP microcomputer.

Many vendors

There are many other firms in the DSP chip business. Some of them produce parts for another part of their firm (for example, Hewlett-Packard of Palo Alto, Calif and Rockwell of Culver City, Calif). Others are second sources, such as General Instruments (Hicksville, NY) for the TI chip. Still others are geared to specific applications (Hughes of El Segundo, Calif) for missile guidance, AT&T Technologies of Basking Ridge, NJ for satellite link echo cancellation). Lastly, AMI, Intel (Santa Clara, Calif), Monolith Memories, Inc (Santa Clara, Calif), Hitachi (San Jose, Calif), and others produce for the merchant market. Intel was an early leader with its 2920, and says it is working on new DSP chips but could provide no information about them for this report.

In all, some thirty firms worldwide make DSP chips for their own or external use. Some make just a few pin-compatible chips, hoping they will tap into the market of a major vendor who has already prepared the market for alternate sources. Others provide complete families and software support.

Some firms are devoting much effort to figuring out what DSP designers will need in the future—and they are getting ready to provide it for them. Certainly GaAs is one such area of research and development. The theory says that GaAs chips should allow faster speeds at much the same power consumption as CMOS. First chips to appear will probably handle such 8-bit arithmetic as multiplication.

While NEC is the first firm with a data flow architecture chip, others are coming into the non-von Neumann world. Of course, TI already has its modified Harvard architecture, as do several other firms. This architecture is not a radical departure from existing structures, however.

Several radical departures in architecture were recently described at the premier DSP conference—The 1984 International Conferences on Acoustics, Speech and Signal Processing held in San Diego, Calif. IBM's Federal Systems Divison (Manassas, Va) briefly described its so-called bimultiply accumulate chip. Still experimental, the 12.5-MHz, pipelined, NMOS, 144-pin chip is the basis for a kind of systolic array. It is implemented as an FIR building block. Another chip mentioned at the conference was from France's Ecole Nationale Superieure des Telecommunications. Also a kind of systolic array, it is an NMOS device geared to speech recognition and implements one of that field's algorithms.

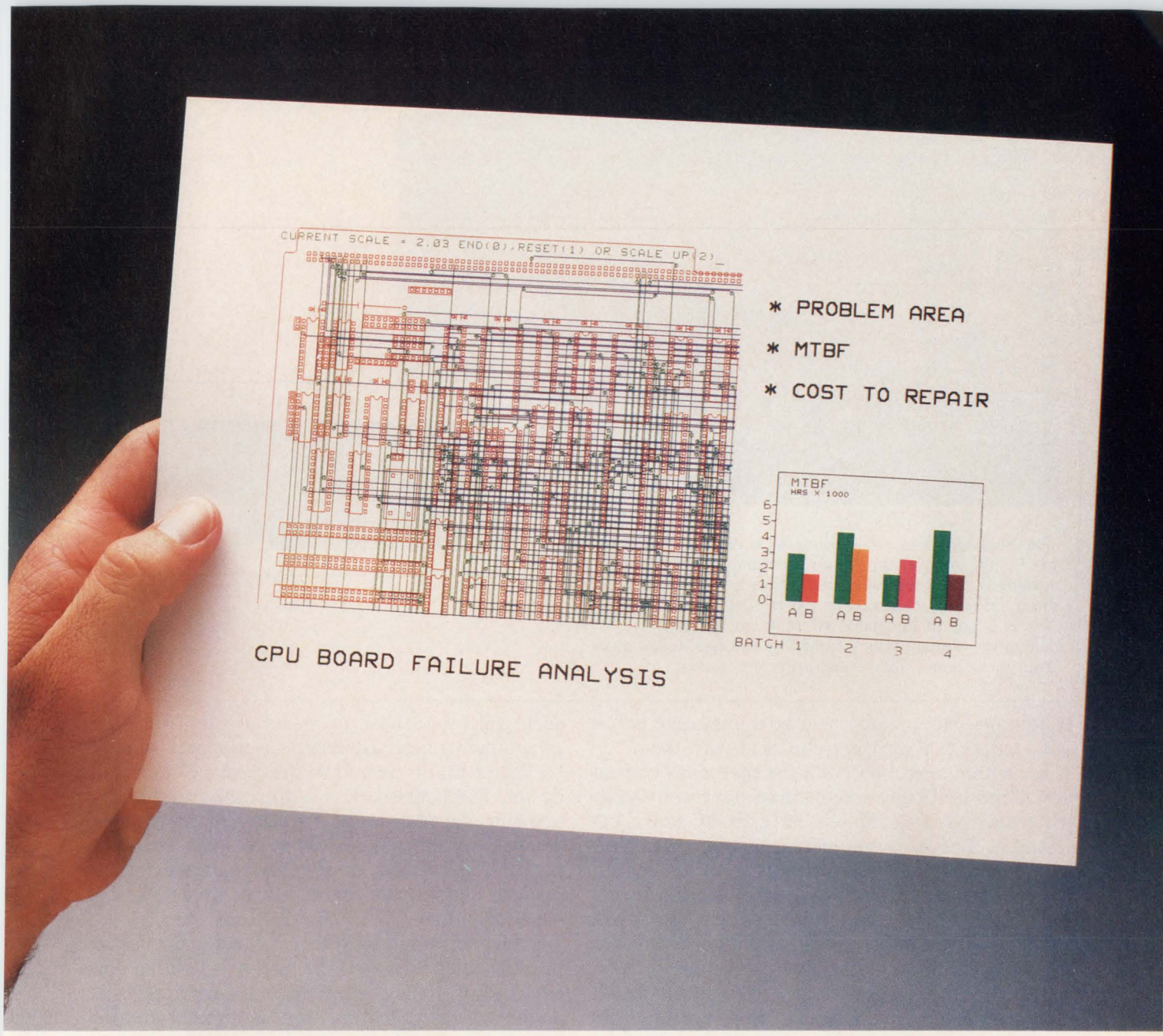
In a systolic array, an array has dozens, or ultimately of hundreds, of identical processing elements that are hooked together for shifting data around. These arrays were first introduced at Carnegie-Mellon University (Pittsburgh, Pa) in the late 1970s. They execute the same instruction in parallel on multiple data words. The array elements share control lines, timing and program instructions.

Many systolic array design problems limit its use in DSP and other applications. One is designing a systolic array chip that can connect efficiently to many neighbors without bogging down in overhead. Construction is also a problem and wafer scale integration is being considered. Other problems plaguing systolic array designers include how to know when a chip has failed and determine which one it is (they all seem the same) in order to reconfigure the system and bypass the offender. Then there is the question of how a systolic array is packaged. Conventional packaging requires just too many pins.

Nevertheless, preliminary systolic array designs for DSP are on the way. For example, systolic arrays may be seen to some extent in INMOS's (Colorado Springs, Colo) transputer (a 32-bit microprocessor) and TRW's yet-unavailable chip for FIR filters. MIT is also looking into them, as are General Electric Company of England, and several other British-based division of U.S. companies, including Hewlett-Packard, Ltd.

New software too

Radical architectures require radical software algorithms. Conventional DSP algorithms are geared to von Neumann designs (see "Fifth Generation Computing: Dedicated Software is the Key," *Computer Design*, Sept 1984, p 150) and are often not suited to data flow or systolic designs. Given that von Neumann algorithms are difficult enough to deal with, it seems clear that algorithms for NON-VON architectures, as they are known, will be a long time



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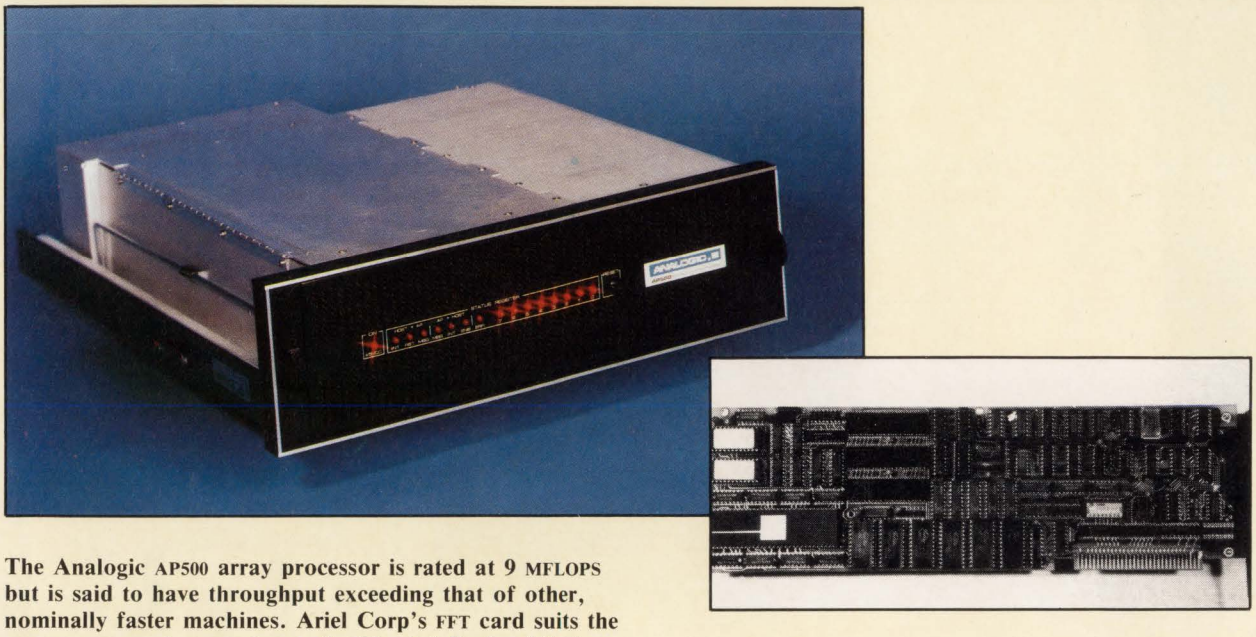

The Analogic AP500 array processor is rated at 9 MFLOPS but is said to have throughput exceeding that of other, nominally faster machines. Ariel Corp's FFT card suits the IBM XT personal computer or the Hewlett-Packard Series 200. It is one of the many DSP tools for personal computers that are taking some low end DSP design away from mainframes, minis, and array processors.

in coming. Moreover, it will be a long time before the average DSP designer can deal with them.

Algorithm reserchers point out that many conventional and well known algorithms have to be recast for NON-VON DSP. This is an area of active DSP research, but it is hampered by the difficulties inherent in NON-VON algorithms.

Array processors are a major application for the wide variety of chips and algorithms discussed. These DSP subsystems, either as standalones or as add-ons to micro, mini, or mainframe computers (used to speed algorithm-based repetitive calculations), represent a lucrative market. They are made by nearly a dozen firms in the United States alone. These include both established firms and the start-ups that are appearing too fast to list them all.

A partial listing includes Analogic Corp (Wakefield, Mass) (see "Array Processor Doubles As DSP Engine," in this issue, page 89), Ariel Corp (New York, NY), CSP Inc (Billerica, Mass), DSP Systems (Ottawa, Canada), Floating Point Systems (Beaverton, Ore), Numerix Corp (Newton, Mass), Sky Computers (see "DSP/Development Board Offers Host Independence," in this issue, p 109), Star Technologies Inc (Portland, Ore), and Systolic Systems (San Jose, Calif).

The range and diversity of applications of array processors is quite amazing. For example, array processors from Analogic Corp are not only found embedded in such dedicated system applications as a nuclear magnetic resonance machine where it helps sharply define the inside-the-human-body "picture" the NMR machine generates. But, they are also in such general-purpose products as the firm's APL programming language-based, overlapping-windows computer that is geared to inexpensive computing power. The field is fiercely competitive and there is one rule the DSP designer must remember—what you get is proportional to what you pay. For example, at the low end, a lot of array processors are made as plug-in, add-on boards for the IBM XT personal computer (Ariel, Systolic, Marinco).

Even lower on the cost scale of personal computer plug-ins made for DSP is the Intel 8087 floating point coprocessor. It may be plugged into an empty socket in the XT or TI Professional Computer motherboard. And, IBM's brand-new multi-user personal computer—the AT—has a spot for the even more sophisticated Intel 80287 floating point coprocessor (see "Multi-user AT Computer Creates Standards Overnight," *Computer Design*, Oct 1, 1984, p 25).

Price/performance trade-offs

At the other end of the price spectrum are boards made by such firms as Floating Point Systems for high end applications. These involve six-figure costs and 10 to 15 MFLOPS or more speed, depending on the application. Better yet, array processor capabilities have been upgraded so much by their chips that some of them achieve a percentage of supercomputer performance (or even better) at a price that justifies the buy.

For example, Floating Point System's FPS-164/MAX can hit 331 MFLOPS (when it is coupled with a mainframe) for certain algorithms. It's a steal at $300,000 if you are running one of those algorithms.

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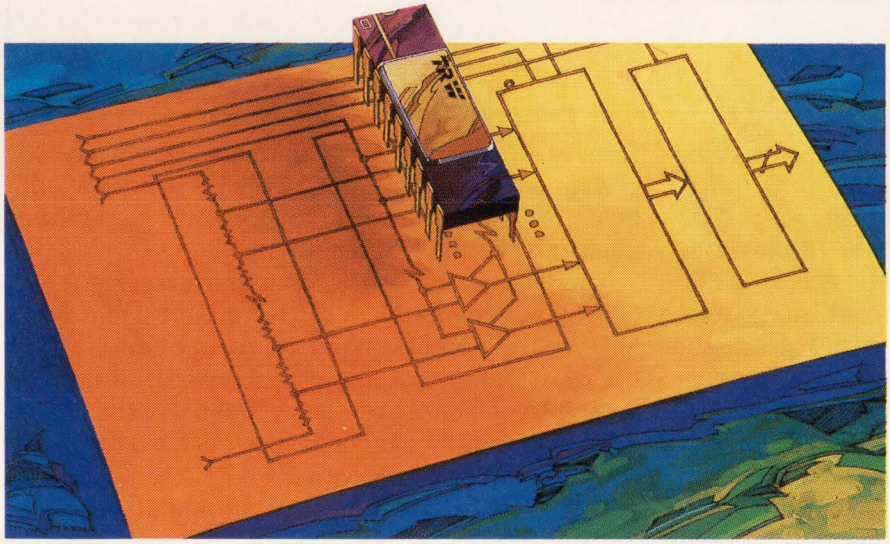

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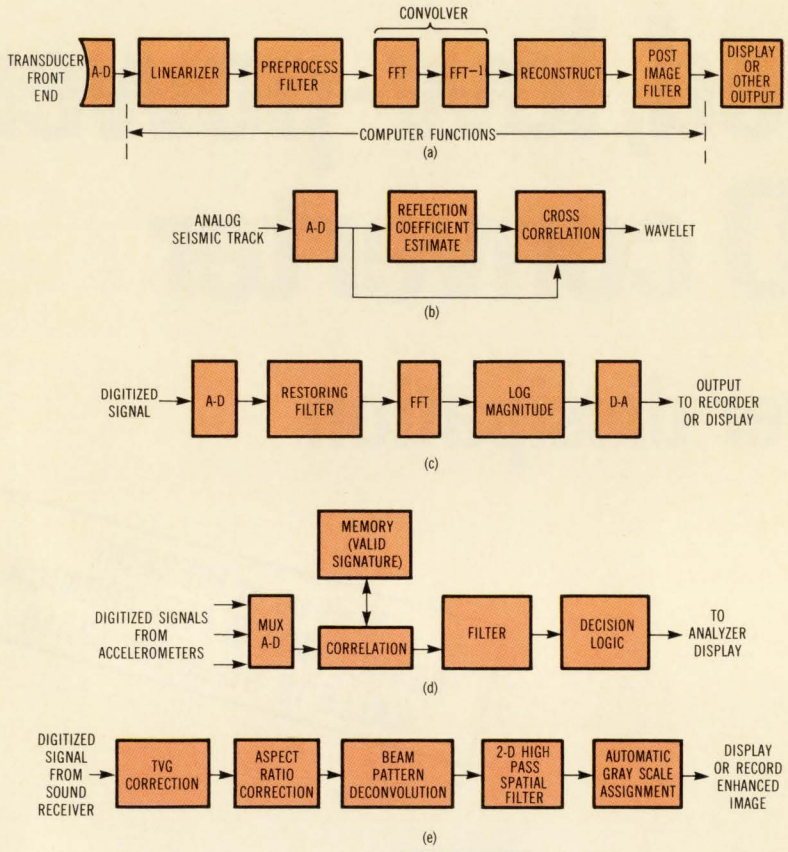
CIRCLE 34



Applications of array processors include general signal processing (a), seismic exploration (b), spectrum (c) and vibration analysis (d), and side scan sonar processing (e). Configurations appear different but comprise a small number of the same digital filter-like components.

The alternative, a Cray-1 supercomputer, may be slower for that algorithm and cost $5 to $10 million. Also consider the fact that newcomer Star Technologies says it will soon deliver 100 MFLOPS at 32 bits. It uses ECL gate arrays whose heat is said to be blown away by a novel forced air system. Finally, Analogic Corp's AP-500 array processor is making a strong DSP mark in many applications areas. It is an outgrowth of the firm's successful AP-400.

The high end 64-bit array processors are not every DSP designer's cup of tea, however. A strong 32-bit market served by "lesser" machines for many applications also exists. For both of these bit sizes, the second key to success, after speed, is applications software. This is written by the DSP designer, third-party gurus, or the board vendor. In any case, it is a major problem even with the traditional von Neumann architectures these processors enjoy.

Trying to get an exotic, nonconventional algorithm implemented quickly for 64-bit machines (let alone cheaply) can give the designer a lot of grief. Even 32-bit machines are difficult to supply with special software. Sometimes DSP designers are the only ones sufficiently interested and they are not sufficiently skilled to do the job. Compilers that transform existing software to run on an array processor present one partial solution. Even these are not adequate, however, since the processor's capabilities might not be used efficiently.

The large array processor manufacturers try to help by making as much software as possible available for their processors in the form of application libraries. But algorithms are a very special thing—subject to personal preference much like the choice of a programming language. So it is hard to satisfy everyone's specific interests.

Although the DSP world will ultimately go to 64 bits for the scientific calculations that are the mainstay of the array processor field, 32-bit machines are most common today. They range in price from hundreds of thousands to tens of thousands of dollars, with throughputs ranging from 100 MFLOPS to 5 or 10 (which is a function of price). Typical machines in this range made by Sky and Analogic Corp are discussed in detail in the articles on p 109 and p 89 in this issue. They are good representations of state-of-the-art technology for different types of array processors.

The coming 64-bit array processors offer more than precision. They make it possible to accommodate DSP applications not otherwise achievable. The

reason is simple. At 32 bits, for certain algorithms and calculations, round-off errors make results worthless. The 64-bit array processor does not have such a problem for a large additional number of applications and algorithms. As such, when coupled to an existing mainframe, it may substitute for supercomputers in, for example, certain simulation applications.

DSP designers may use a DSP board or an array processor in an IBM XT, or they may hook it to a DEC minicomputer or an IBM mainframe. Array processor subsystems cannot replace these machines—nor are they intended to—because they are too limited in application. The goal is to complement the larger machine's capabilities for DSP. As such, the boards are designed to easily interface. For example, Sky provides Multibus, VMEbus, and S100 bus connections for its boards. In fact, many of Sky's boards and those of other manufacturers in the 16- and 32-bit DSP world are directly set to plug in workstations and minicomputers to increase their floating point calculation capability.

DSP design comes to PCs

Serious practitioners of the DSP art who need to be able to design complete systems must rely on such gear as Digital Equipment Corp's (Maynard, Mass) PDP-11 and VAX minicomputers for their programming environments and DSP programming tools. They use these machines along with the software design tools provided by many of the VLSI chip manufacturers who serve the DSP market.

The surprise low end design tool of the 1980s—the personal computer—is getting its share of DSP software, however. The personal computers (usually from IBM in Boca Raton, Fla or Texas Instruments often need an Intel 8087 mathematics coprocessor (for floating point arithmetic) as their only nonstandard hardware—and then only if the designer cannot wait for the 8088 or 8086 to chug along and come up with the needed DSP numbers.

Many of the personal computer software packages are geared to TI's TMS320 DSP microcomputer chip. This is because TI realized early on that application software would be invaluable to designers involved in signal processing, and its availability would help sell chips. For example, Alembic Systems (Santa Monica, Calif) sells a speech sciences development package and cross assembler/loader for the TMS320 and Computalker Consultants (also in Santa Monica) has an assembler and simulator for the same product. DSPS, Inc in Ottawa, Canada, offers a TMS 320 cross-assembler among other DSP products.

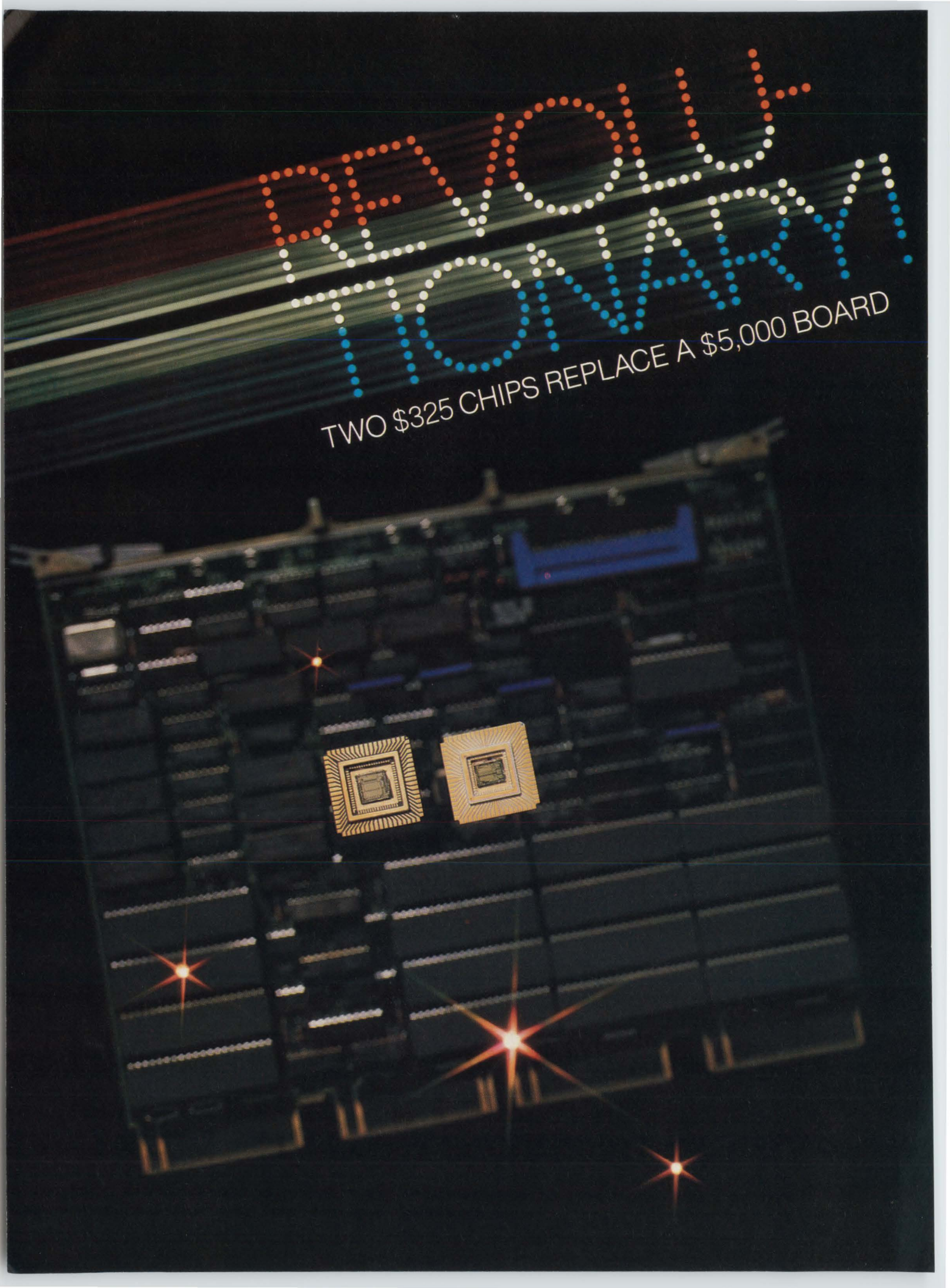
Some of these firms are moving beyond mere software and offering plug-in PC boards. For example, Alembic has a board geared to the Advanced Micro Devices DSP telephony chip known as subscriber line audio processing circuit (SLAC). This high speed MOS chip offers DSP-based, programmable filters at the central office interface with each telephone subscriber line as well as A-D and D-A conversion. It is designed to tailor the specific subscriber line connection for either voice, data or teletext transmissions from the computer-controlled, networked business office. To do this chore, it adjusts the parameters of the communications link so whatever data is transmitted (or received) can be optimally handled as far as noise, error rate, and other factors are concerned. SLACs may appear in many computer systems of the future.

The surprise low end design tool of the 1980s—the personal computer—is getting its share of DSP software.

The fast Fourier transform is widespread in DSP and a variety of software packages implement it in software. One for the PC is offered by Whitman Engineering, Inc (Maitland, Fla). Still another commonly performed function is digital filter design. Software packages for this chore are offered by various firms including Signix Corp (Wayland, Mass) and Atlanta Signal Processors, Inc.

Atlanta's software package is geared for the IBM PC or XT or the TI Professional Computer. An 8087 speeds up calculations (the filter design programs recognizes its presence automatically) but it is not necessary. Not only does the program come up with a digital filter's parameters, it automatically generates the assembly code to implement the parameters on the TI TMS320 DSP chip.

DSP design software for personal computers makes advances in VLSI and algorithms even more significant for the designer. In the coming years, DSP will be applied to an increasing number of computer design problems not only because DSP produces better-specified computer systems, but because it is easy to use.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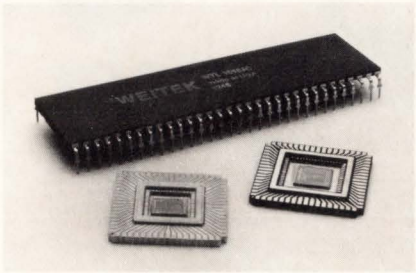

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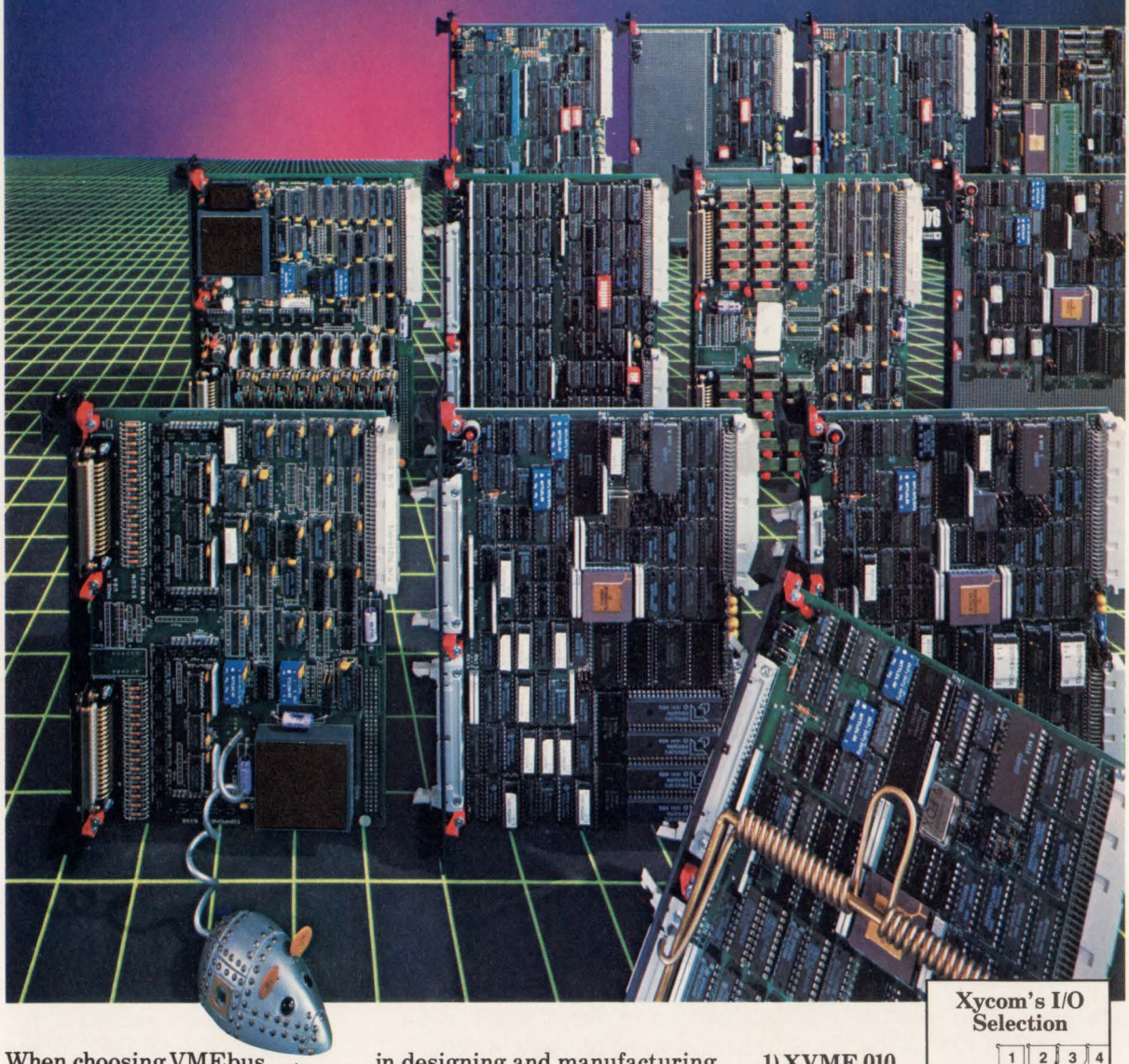

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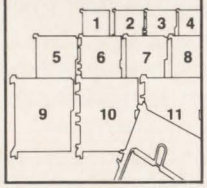

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CIRCLE 36

GENERAL-PURPOSE BOARD IS DESIGNER'S FIRST STEP INTO DSP

An entry-level, single-board computer performs 1-K complex point fast Fourier transforms, matrix operations, and filters.

by Rajesh Tanna

Digital signal processing technology has been available for a number of years. But new PCs have forced designers looking at the technology's problems to continually update their solutions. Before this can be done, however, the basic principles of digital signal processing design must be understood. One of the best ways the designer can learn these principles is to review an actual design of a high speed, single-PC board, digital signal processing computer suitable for repetitive calculations.

One way to explain the design process is to state the typical system requirements and describe the appropriate design. The fast Fourier transform (FFT) is the central algorithm in signal processing. Its implementation is the basic design requirement. Note, however, that the architecture to be described lends itself to any algorithm that requires high speed number crunching. These include filters and matrix multiplications, additions, and subtractions.

The architecture chosen for the digital signal processing (DSP) board must support the designer's specific goals. For example, the arithmetic architecture must support the speed requirements of the processes to be run. The memory architecture must be properly chosen to support realtime applications. In addition, the architecture of the addressing section can be straightforward. This section needs different address generators to support different DSP algorithms. The microword width for the control section would be decided by the rest of the architectures. Finally, the section should be designed based on the data acquisition method and the nature of the host.

After the design is completed on paper, a thorough timing analysis makes sure that speed goals are achieved. More processing power may have to be added if the goals are not achieved and cannot be relaxed. Finally, the code is written. Ideally, it should be thought of during the design phase. This ensures that all resources can be used efficiently for the particular algorithms for which the board is designed.

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Fundamental considerations

The basic component of the FFT computation is the "butterfly"—named after the shape of its graphic representation. A butterfly requires computation of one complex multiplication and two complex additions. DSP system throughput is the rate function at which these calculations are performed.

Assume that the input signal only contains frequencies below 500 kHz, which are to be separated into spectral components with a 500-Hz bandwidth. Assuming both in-phase and quadrature signals are available and no guard band is necessary, aliasing

is avoided by digitizing at a 500-kHz sampling rate. If 1024 is selected as a suitable memory size, real-time operation requires a dual-memory bank and that a 1-K FFT be performed every 2 ms. Thus, data acquisition can continue while the FFT is performed on the previous data batch.

A 1-K FFT contains 10 columns of 512 butterflies each, for a total of 5120. This figure translates to 5120 x 4 real multiplications and 5120 x 6 real additions. Since the FFT algorithm consists of short loops that are highly repetitive and multiply-intensive, a micro-programmable, pipelined architecture is best. Included in this architecture are a micro program control section, an arithmetic section, a data memory section, an addressing section, and an I/O section. Hardware must be capable of 10-MHz operation so that a single multiplier performs all required multiplications.

The butterfly performance for architectures with a differing number of resources that are potential bottlenecks has been calculated. To accomplish a 1-K FFT in 2 ms at 10 MHz, each butterfly can take no more than 400 ns (4 cycles). A two-bus, two-ALU, one-multiplier architecture may be chosen for the DSP computer board design. Note that the multiplier and the two buses are occupied 100 percent of the time, and the ALUs 75 percent of the time. Fig 1 shows a block diagram of the board architecture.

The arithmetic section, including ALUs and multiplier (Fig 2), performs all number crunching. The three ports and six registers of the Am29501 ALU are a good choice for pipelined operations. The Am29517 16 x 16 multiplier is also suitable because of its single clock requirement. The butterfly equations for radix 2 DIF transforms are $A' B = A + B$, $B' = (A - B)W^k$; the DIT transforms are $A' = A + BW^k$ and $B' = A - BW^k$. A and B are complex input data points and W (superscript k) is the complex coefficient.

As seen from these equations, multiplication always involves one coefficient (constant) and one data point. So for the FFT algorithm, the coefficient is the multiplier and the ALUs furnish the multiplicand. Squaring to form a magnitude requires multiplication between data inputs. For this computation, a multiplexer switches the multiplier input from the coefficient source to the ALU. Also, complex arithmetic requires that data be able to flow from either ALU to the other. Finally, the product from the multiplier flows back into the ALU to continue through the pipeline.

All these data paths can be achieved using the ALUs and the multiplier. A transceiver allows data flow between ALUs and prevents bus contention. A carry lookahead generator connected between ALUs allows double-precision arithmetic.

When a fixed point system is designed, data scaling must be considered so that results do not overflow. Although scaling can be on the input data or on the results, a shifter at the input to the pipeline serves the function without restricting the input data. When the shifter is at the output, input data is restricted, to ensure that no overflow occurs on the first pass through the pipeline.

Memory is important too

Data memory must be designed to support the high speed architecture. The minimum requirement is one memory bank, toggled between the host system and the DSP processor. But this design causes the DSP processor to be idle for the time data is unloaded and new data reloaded. Realtime applications typically sample data continuously at a fixed rate. Results of the process are read continuously from the data memory. Thus, with two memory banks, one can be unloaded and reloaded, while the other is processed by the DSP.

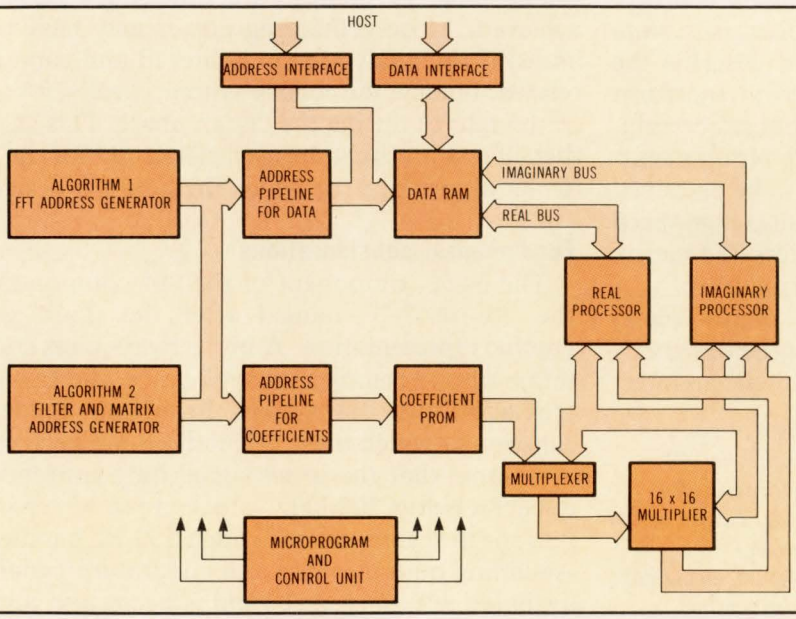

Fig 1 A single-board, digital signal processing (DSP) system under microprogram control handles a variety of computer-intensive chores. This design is an entry-level computer for the DSP beginner. It handles fast Fourier transforms (FFTs), filters, and matrix operations under host control.

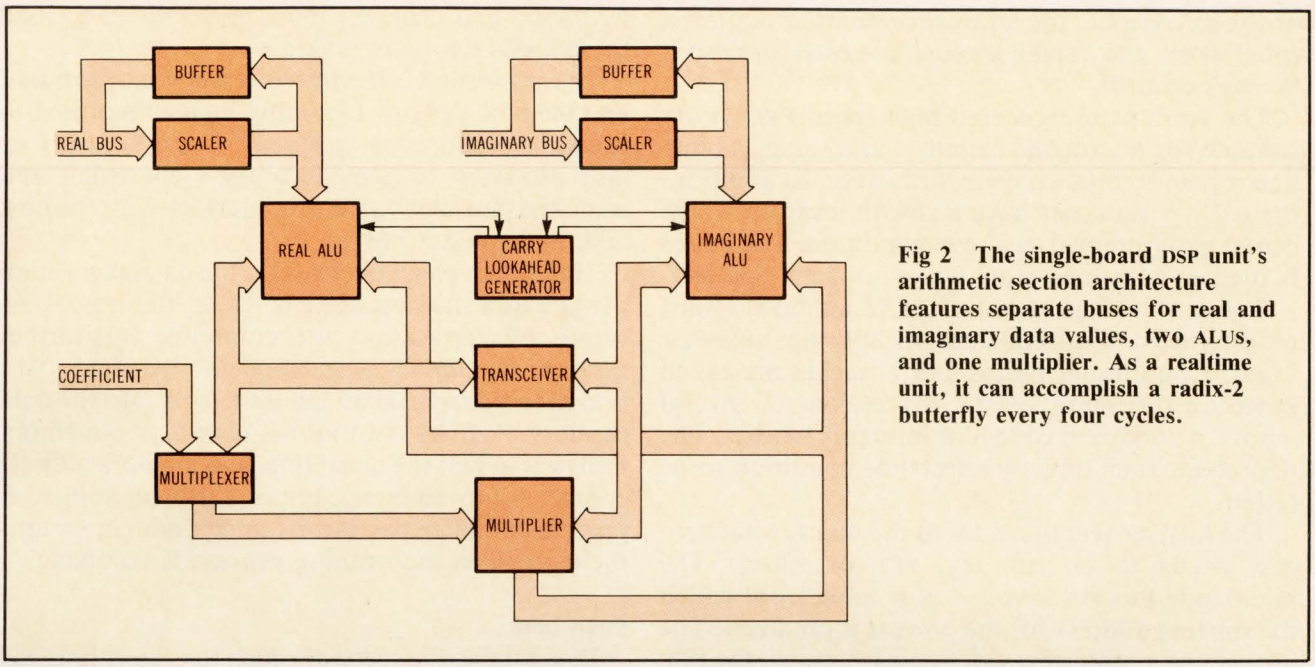

Fig 2 The single-board DSP unit's arithmetic section architecture features separate buses for real and imaginary data values, two ALUs, and one multiplier. As a realtime unit, it can accomplish a radix-2 butterfly every four cycles.

A typical dual-memory architecture has two address buses supplying addresses to the two banks (Fig 3). One supplies data addresses for the DSP process and the other supplies addresses for loading of data and unloading of results. The memory needs to be arranged so that complex numbers can be easily stored and accessed. Assuming that the design calls for a 16-bit DSP system, each memory bank must be 32 bits wide and 1-k deep to hold 1024 complex data points. This restricts the designer to in-place FFTs.

Separate data buses from the memory to the ALUs allow all 32 bits of data to flow in unison into both ALUs. However, the host system might be 8 or 16 bits wide. The complex number would then be loaded in two or four parts. Three transceivers interfacing the host system data bus to the memory must be controlled to ensure correct sequence data flow.

The transceivers between the memory and ALUs must also be controlled to prevent bus contention. Transceivers between the memory and host system are controlled for the same reason. Finally, memories must be high speed to support the realtime architecture (45-ns RAMs in this design).

To achieve parallel operation, both memory banks are addressed simultaneously. One is handled by the host for data unloading and reloading. The other is handled by the DSP address generator (Fig 4). The Am29540 FFT address sequencer, which can generate data and coefficient addresses for all combinations of in-place/non in-place, radix 4/radix 2, and DIT/DIF FFTs, supports transform lengths of 2 to 65,536 points.

The Am29116 controller is suited for address generation for other DSP processes (matrix arithmetic and filters). This is because it takes care of all addressing, and board space is usually critical. Because the board runs one process at a time, the two address generators are never used simultaneously. Therefore, microcode bits for the two parts can be overlaid.

To synchronize the arrival of addresses and data at the memory, there is a pipeline register between the address generators and the data memory. The Am29520 pipeline register must also be used to make the microcode efficient and allow butterfly completion every four cycles. This part has four registers and can serve as a dual two-level pipeline register. Two source addresses for the data inputs for one butterfly are saved in one level. The two destination addresses for the results of the previous butterfly are saved in the other level.

The FFT process needs coefficients or constant values that are PROM-programmed. These PROMs, can be addressed by the Am29540 address generator. The filter process also needs coefficients programmed into a separate PROM and addressed by the filter address generator. A separate pipeline register holds coefficient addresses for each FFT butterfly.

Addressing from the host side for data is provided at high speed to make the application real time. The best way to achieve this is through a DMA scheme. Finally, the design requires four, tri-state buffers to switch buses when memories are toggled.

Stay under control

Because microcode controls the system, the control section is the heart of the design. Microcode width must be decided during this design phase and a microprogram sequencer must be selected to execute the microcode. Microcode bits need a pipeline register so that the sequencer can fetch the next microinstruction while the present one is executing. Note that the arithmetic section requires the bulk

of the microcode, the addressing section requires a small share, and a small amount is needed for miscellaneous control.

The Am27S45A registered high speed PROMs are suitable for microcode memory, and serve as pipeline registers, thus saving board space. In addition, these 2-K x 8 PROMs have a 2049th location which can be programmed as a reset condition. The board is then in a defined state when power is applied.

A way of testing the board for "conditions" must be provided. The sequencer usually has one test input. Conditional jumps and branches are taken based on this input's state. To test one of several inputs, a condition code multiplexer is needed. The microcode then directly selects the condition to be tested.

The host system indicates to the board what process needs to be run (eg, FFT or filter). The microcode PROMs have a vector table from which the starting address for the process is obtained. The instruction register provides a link between the DSP board and the host, and indicates the FFT or matrix size to the address generators. With this design, the same microcode serves any size FFT or matrix.

The host interface also has a flipflop, indicating on which memory bank the board is to work. The host sets or resets this flipflop, turning on the switching logic for either one memory bank or the other.

The designed board does not have writable control store. In other words, the microcode is programmed into PROMs and cannot be changed unless the PROMs are changed. However, writable control store can be added. The PROMs have to be replaced by RAMs, and a means must be provided to load these RAMs with microcode.

The I/O section is the interface between the board and the host system. Decoding logic is required to decode I/O addresses reserved for the board. It is also necessary to provide a DMA controller and some registers and buffers to interface with the host address and data buses.

This design phase depends on the data acquisition method and the host system. Here, the host is assumed to be an AmSys 29/10 computer. It is further assumed that data is host supplied. Therefore, DMA is used to transport data from the host into the data memory. A flyby DMA allows memory-to-memory transfers in half the usual time and an extra address counter (flyby counter) supports this capability. A process-complete flag (set by microcode) interrupts the host when the running process is complete.

Keep time

Determining the speed at which the algorithms will run is the most critical design phase. The designer starts out with a set of goals divided into two categories. Category 1 lists the different algorithms that the design has to process; Category 2 lists how fast they must run.

The design must begin with Category 1, and the architecture must be designed so that all algorithms run. The designers then write microcode for these processes. Knowing the architecture, and having written the microcode, they can easily evaluate worst-case data paths. They then compute process times and compare them with the Category 2 goals.

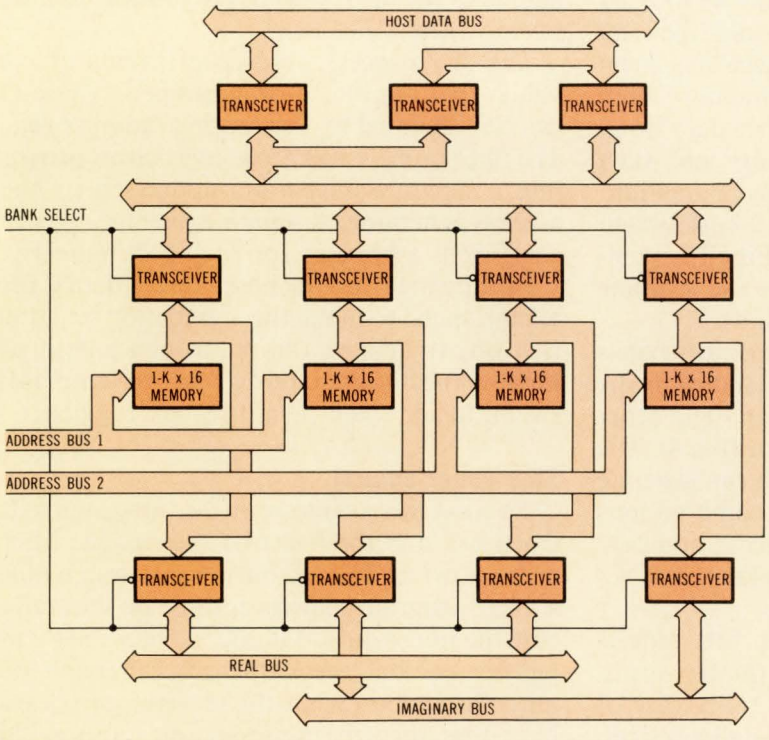

Fig 3 The DSP memory section has two address buses that enable simultaneous addressing of its 1-K x 32 double memory banks. The many transceivers make the connections to the host data bus and to the DSP system's real and imaginary data buses.

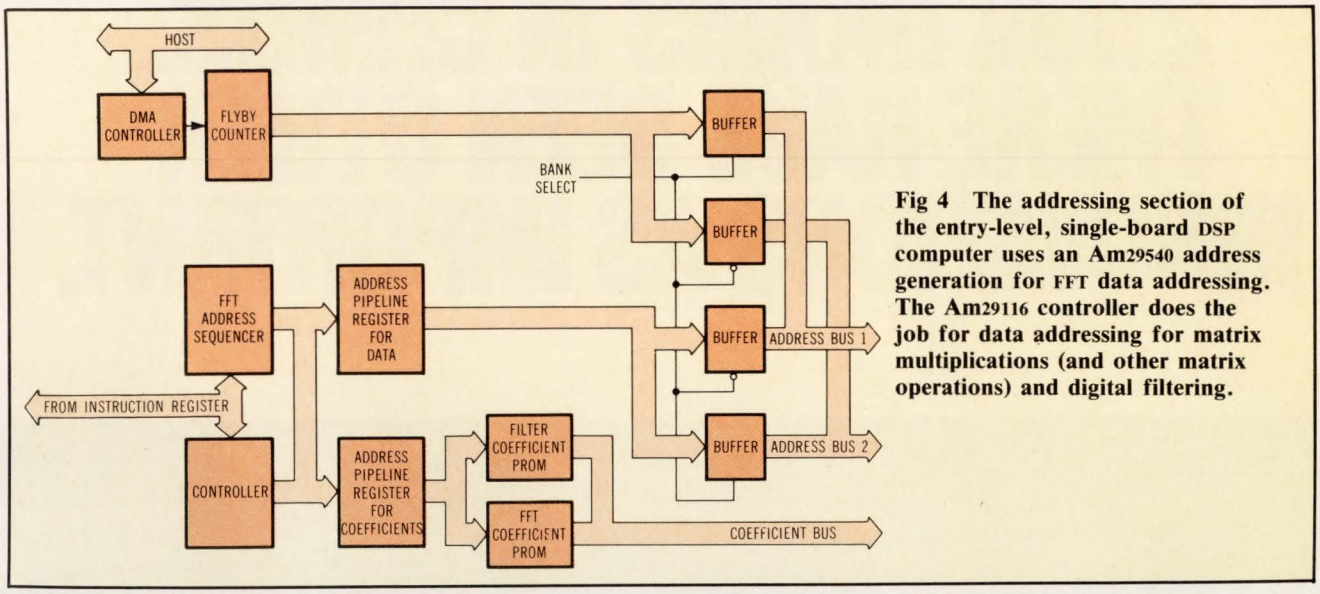

Fig 4 The addressing section of the entry-level, single-board DSP computer uses an Am29540 address generation for FFT data addressing. The Am29116 controller does the job for data addressing for matrix multiplications (and other matrix operations) and digital filtering.

All is well if the criteria in both categories are met. If not, trade-offs must be made. If the designer cannot write more efficient microcode, the architecture must be changed or goals relaxed.

Changing the architecture implies adding hardware for more processing power. Because of board space and cost limits, this is not always possible. The alternative solution (relaxing goals) means either eliminating some algorithms (thus reducing hardware, eliminating propagation delays, and increasing speed), or accepting slower speeds.

A data path time is the total of all setup and hold times, propagation delays, and access times that data encounters between two registers. One example is the path time from when the pipeline register emits an address to when the ALU's register clocks the data in. This includes the clock to output of the microprogram pipeline register, access time of the pipeline register, propagation delay through bus switching buffers and transceivers, data memory access time, delay through shifters, data setup time for the ALU's register, and the data hold time for the ALU's register.

All possible data paths should be considered. Usually, the longest one is the path for testing conditions. The longest data path determined the best possible cycle time. One way to improve performance is to control clock cycles with a clock generator. Long paths can use a slower clock and short paths a faster one. Careful data path analysis leads to significant performance gains—especially when only a few paths are slow.

Microcoding made easy

Microprogramming involves writing a coherent sequence of microinstructions to execute commands required by the machine. A microinstruction usually has two primary parts: the definition and control of all elemental microoperations, and the definition and control of the next-executed microinstruction's address.

Various microoperations include controlling the ALUs, multiplier, data address generator, data memory, address pipeline registers, shifters, and condition code multiplexer. Defining the next microinstruction includes spotting the source selection for the next microinstruction address. Two principles help when writing efficient microcode for these chores. Parallel execution of different operations is the most efficient technique; maximum resource use is gained via a pipelined architecture.

The arithmetic section should be programmed first. Then, the code for the rest of the system should be mapped into the code for this section. This approach is best because the arithmetic section is the bottleneck and the available resources need to be used as efficiently as possible.

Writing the code is made much easier with the AMDASM meta-assembler. This is because it lets the designer create a symbolic language. First, instructions are user defined—each instruction defines a bit pattern for a microword section. These instructions are then grouped, in the second phase, to write the microcode. Microcode debugging can be a costly and time-consuming process if PROMs are burned every time code is changed. The writable control store in the host replaces the microcode PROMs during the development phase. In order to aid debugging, the host enables single-stepping through the code. After the code is debugged, a PROM fuse map can be created.

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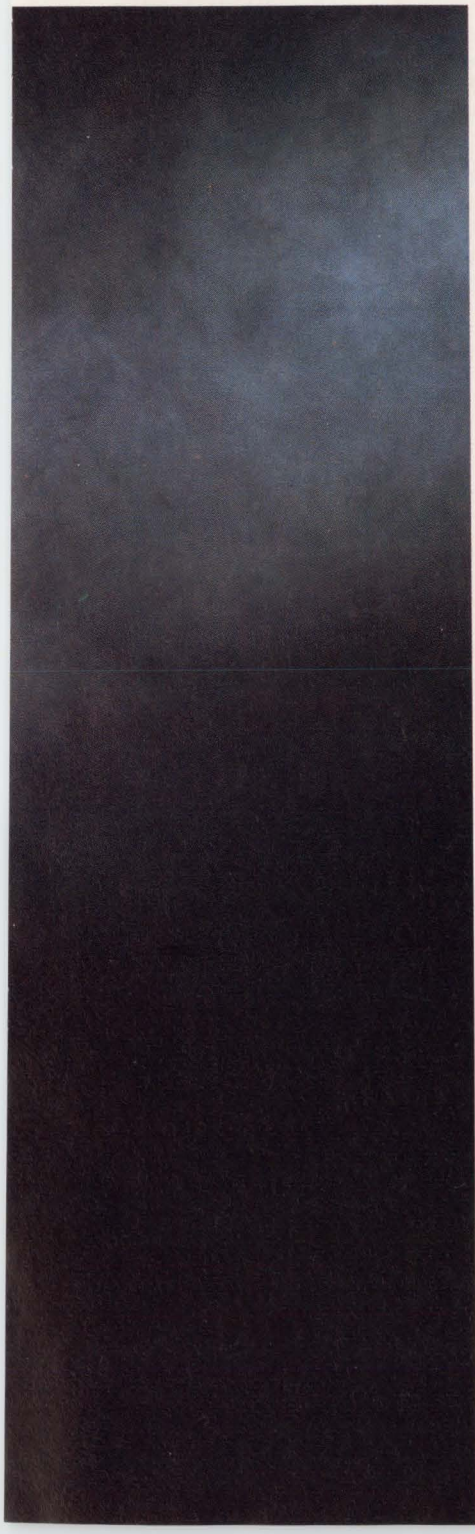

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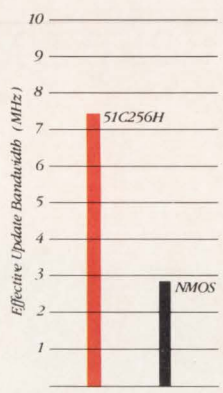

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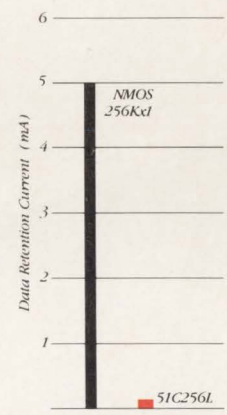

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CIRCLE 37

ARRAY PROCESSOR DOUBLES AS DSP ENGINE

Almost host independent, an application software-driven subsystem solves a wide range of design problems.

by Bruce R. Mackie

Computer designers are adopting digital signal processing techniques at an ever-increasing rate. Unlike analog systems, digital systems are fairly immune to time and environmental variations. They are also easily changed via software modification.

Analog system changes often require hardware design modifications. However, for many realtime processing applications, continuous analog processing techniques remain dominant due to the speed and power limits of the array processors performing realtime calculations. One of the latest industry steps to overcome this bottleneck is the AP500.

The AP500 is an array processor based on distributed processing (Fig 1). Its 12.5-MHz Motorola MC68000 executive processor supervises, schedules, and monitors each of the array processor's discrete processors. Moreover, its 384-Kbyte maximum program memory can host a sophisticated array processor executive program. This allows many array processor control tasks to be user transparent.

The prime responsibility of the array processor's CPU is I/O operation control between the minicomputer or mainframe host and the array processor. But, the array processor is designed to be as host independent as possible in performing its application program chores. Equally important tasks for the MC68000 are the setup, control, and monitoring of the array processor's various supplementary (dedicated) processors.

One such device, the peripheral interface adapter (PIA), works with the array processor's optional AMA-500 Multibus adapter (through an independent DMA controller). Using the PIA, the computer system designer can connect any peripheral device, such as monitors, disks, tapes, local networks, and graphics controllers. In addition, these devices are array processor-dedicated and put no burden on the host.

There is an alternative to the PIA in the array processor's dual auxiliary I/O ports. These are high speed (6-MHz), 16-bit, bidirectional data paths directly into or out of the large (1 megaword, each word 32 bits) AP500 data memory. Here again, the MC68000 is responsible for setting up and monitoring an independent DMA controller for each I/O port.

The final element in the array processor distributed processing environment is an arithmetic pipeline controller. As with the previously mentioned elements, the array processor's MC68000 sets up and monitors the pipeline controller. Detailed control of the pipeline and its associated data memory is reserved for a dedicated pair of processors. The first, the address generator, is responsible for information movement into or out of data memory to various array processor locations. The second, the pipeline

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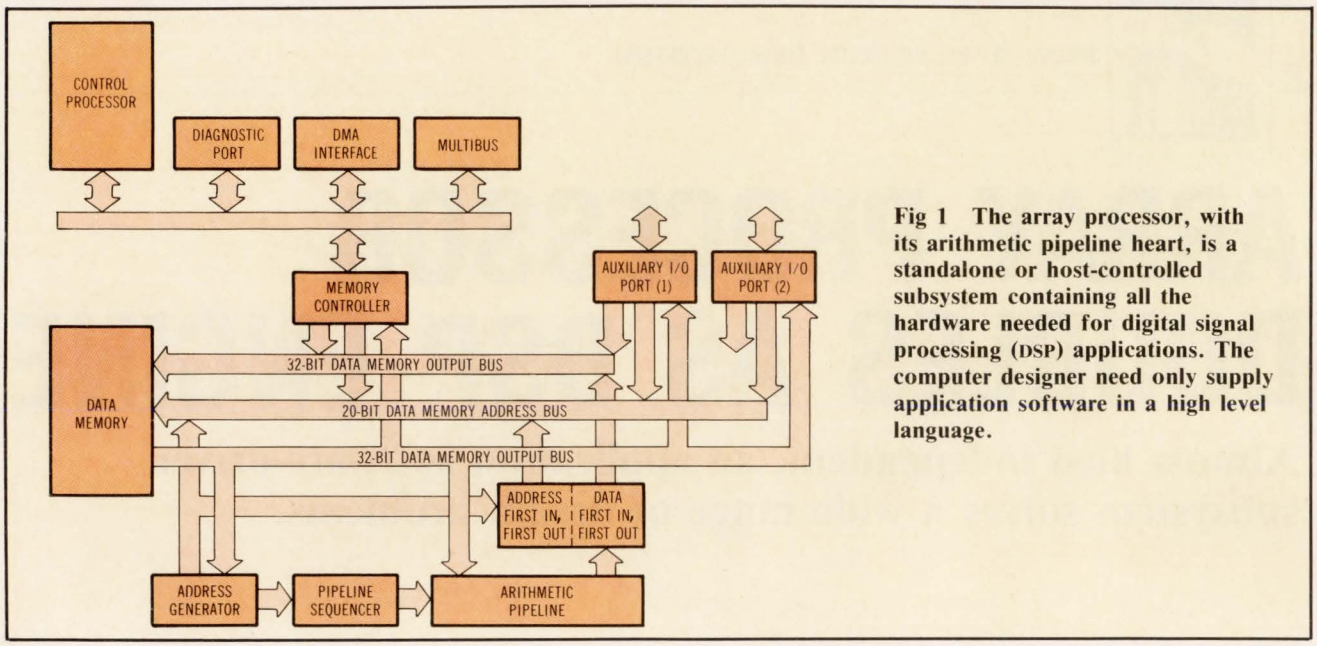

Fig 1 The array processor, with its arithmetic pipeline heart, is a standalone or host-controlled subsystem containing all the hardware needed for digital signal processing (DSP) applications. The computer designer need only supply application software in a high level language.

sequencer, controls all the pipeline functions. This distributed, discrete processing capability under CPU control characterizes a fourth-generation array processor (see Panel, "Array processors evolve").

The pipeline approach

The AP500's arithmetic pipeline (Fig 2) is key to its performance. For example, internal registers ("M" and "Z" files) utilize memory bandwidth resources better than nonbuffered pipelines. In addition, various bypass and feedback paths maximize memory bandwidth resources and the array processor's arithmetic resources, by eliminating static passes through unused memory elements.

Although most array processors perform data-dependent addressing, they must perform these operations from system data memory. This procedure absorbs limited data memory bandwidth. In contrast, the AP500 allows data-dependent addressing directly from the pipeline to its address generator—eliminating usage of scarce data memory and bandwidth resources.

The pipeline design allows an array processor that is raw speed rated at 9 million floating point operations per second (MFLOPS). But, its practical throughput can outperform processors initially rated at 12 to 13 MFLOPS. Similarly, the computation-only, extended-precision nature of the pipeline (40 bits with a 32-bit mantissa and an 8-bit exponent) allows a 32-bit data memory, not the usual 38 bits. This feature reduces costs without a negative impact on the resolution of computed results.

When configured as an attached array processor, the AP500's number-crunching facility is accessed by host-based, high level language application programs. However, the array processor's software functions almost as a standalone device. Host program and array processor communication is initiated by calls to host K-functions. These user-written or Analogic-supplied routines initiate the construction of data structures known as function control blocks (FCBs). Ultimately, they direct array processor operation.

K-functions provide rudimentary parameter checking before invoking the array processor manager. Together with the array processor driver, this controls the host side of all transactions with the AP500. The manager reports errors encountered in array processor operations or during host/array processor communications. It also handles host-initiated requests to report on or change the array processor's operational status. Furthermore, the manager answers requests to stop or reset the array processor. It also sets up the common variables to be used in array processor calls.

Unlike the manager, the array processor driver is host-specific and considered part of the host's operating system. The driver has many functions. It directs host to array processor data, array processor control/status, and message registers; and handles array processor-requested host interrupts. The driver also maps host memory, when necessary, for host to array processor DMA transfers.

Executive forms operating system

The array processor counterpart of the driver is the array processor executive, which resides in the array processor's program memory. It monitors and controls all of the processor's resources. Together with service subroutines, the executive forms an elementary, realtime, single-user array processor operating system. Interrupts can be sent to the arithmetic pipeline and any array processor peripheral device. Once it has appraised a critical situation, the executive can stop and redirect array processor activities

almost immediately. Most often, it initiates host to array processor DMA transfers and presides over all other I/O functions. One of its most important duties is acquiring host-constructed FCBs.

After obtaining one or more FCBs, the array processor executive calls one of a set of array processor Q-functions. These generate FCBs. Some K-functions simply make calls to the array processor manager and have Q-functions associated with them. Written in MC68000 assembly language (supplemented with Analogic-written macros), array processor Q-functions check the parameters contained in the FCBs. K-function parameter lists refer to data buffers, rather than absolute data memory addresses. (Data buffer ID numbers are all that the user need supply.) Therefore, Q-functions will ensure against any discrepancies between the amount of data processing requested and the amount of data present.

Q-functions also call executive service subroutines to organize and manage data memory buffers as specified by the original K-function calls. Q-functions set up small structures in data memory containing the initial values to be loaded into the address generator's registers. These consist of data buffer first-word addresses and the number of points to be processed. The final array processor Q-function duty is to start address generator execution.

Having been started by the array processor executive as the result of a call by an array processor Q-function, the address generator loads its 16 registers from data structures set up in data memory by the Q-functions. Arithmetic unit control is then passed to a function subroutine. These programs consist of address generator and pipeline sequencer microcode. The address generator sections of function subroutines contain instructions to start and stop the arithmetic pipeline. They also direct data flow to the arithmetic pipeline by supplying data memory with addresses. The address generator directs processed result flow back to data memory by entering write addresses in the first in, first out (FIFO) buffer.

The issuing of a read address also starts the pipeline if it is not running. Once started, the pipeline runs synchronously with the address generator. Data flow through the pipe is controlled by the pipeline sequence microcode section of the function subroutine. (As noted earlier, a function subroutine may have more than one section of pipeline sequence code.) In addition, the address generator may call other function subroutines or simply execute the pipeline sequence code associated with some other function subroutine.

AP500s with auxiliary I/O ports have additional executive software known as the auxport driver. This code controls communications between the array processor and data acquisition hardware (for example, A-D converters). It checks the state of the FIFOs that buffer data in and out of the auxiliary I/O ports and issues priority interrupts to the array processor's control processor.

The auxport driver sets up and switches data flow to and from buffers in the array processor's data memory. It also requests an interruption of the data flow into the array processor by changing the auxport's message register state. Similarly, an external device signals the beginning or end of a data transmission by manipulation of the auxport control/status register. A set of special K- and Q-functions, for user interface with the auxport driver, makes it possible to design an AP500 application involving

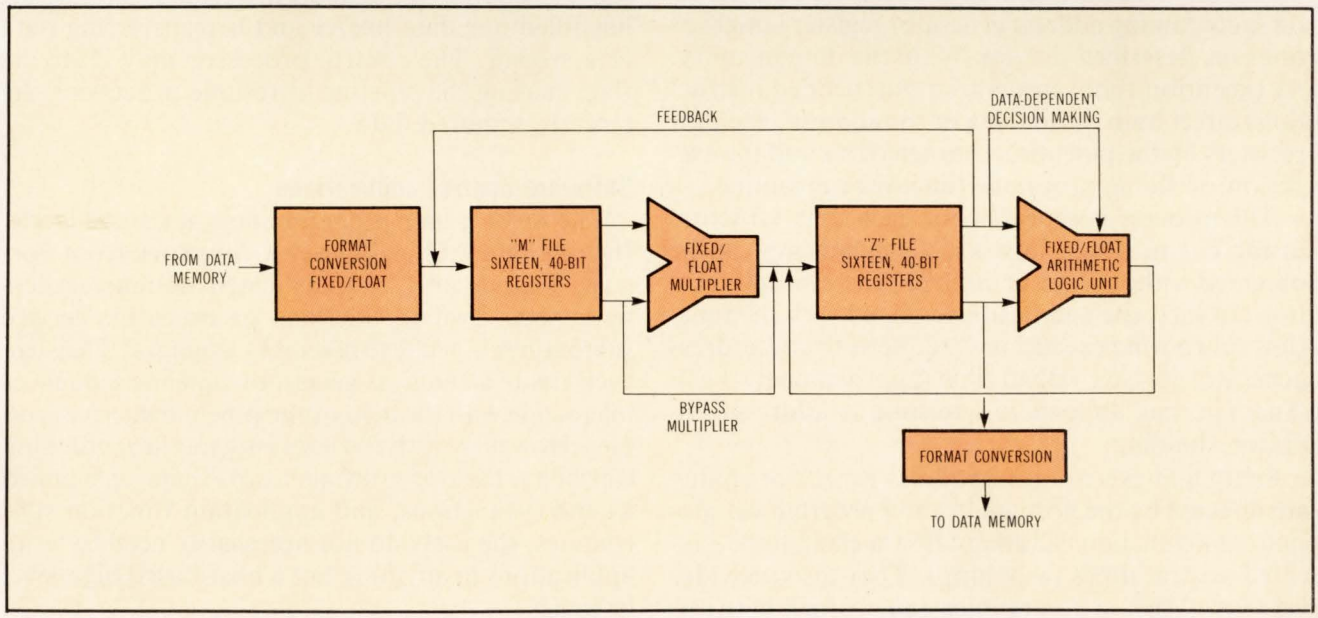

Fig 2 The arithmetic pipeline of the array processor sports both "M" and "Z" files (each with sixteen, 40-bit registers), with both feedback and data-dependent, decision making. It performs operations on up to 4096 Kbytes of onboard data memory.

realtime data acquisition, and code the application in a high level language such as Fortran.

A new hookup

Computational throughput rates for complicated application programs can be greatly enhanced by concatenating array processor directives in data structures (chains). Two chaining types are supported by the array processor's system software. A sequence of FCBs can, by suitable K-calls to the array processor manager/driver, be set prior to execution. Thereafter, they can be executed as a group.

Array processor chain execution may proceed from the host or may be down-loaded into the array processor's program memory. The latter option improves array processor efficiency by reducing the amount of host-array processor communication needed to carry out a sequence of high level calls. Thus, a series of Q-function calls can be executed repeatedly without host intervention. However, FCB chaining does not eliminate the need for the MC68000 to check parameter lists each time a Q-function call is issued. This and other service duties by the array processor executive consume approximately 500 μs for each Q-call. This form of chaining, however, eliminates the 1.7 ms of overhead that is incurred by each K-call.

To eliminate the overhead burden associated with FCB chaining, Analogic has developed a proprietary chaining capability. This design allows the results of several Q-function calls to be collected prior to the start of actual pipeline operations. Once pipeline execution has begun, pipe control can be passed directly from one function subroutine to another—without control processor intervention. The array processor executive sets up a string of data structures containing address generator register initial settings (as described previously) in the data memory. At execution time, specialized microcoded instructions direct both the loading of the address generator registers by the pipeline's characterizers and the execution of the appropriate function subroutine.

This process is repeated for each data structure in the chain. Thus, host K-call sequencing can be obtained without host or control processor intervention. In fact, the overhead associated with the function subroutine execution is reduced to the address generator register reload time (approximately 5 μs). Analogic has dubbed this technique address generator chaining.

Setup and execution of address generator chains are directed by the host application program via specialized K-function calls that allow a chain to be executed several times (as a loop). They also provide, via event flags, a communication channel between a pipeline chain and some related process executed by the control processor. For example, chain execution may be halted by an event flag. This remains set until the control processor is notified (by an interrupt passed from the auxport driver) that the auxport has filled one data buffer and is transferring data to a second. The control processor may clear the flag, causing the pipeline to resume processing the recently acquired data.

Array processors evolve

By today's standards, the first array processors of the late 1960s were primitive. In fact, these processors were nothing more than combinations of fast adders and multipliers, very tightly coupled to a host processor's CPU and core memory. Not widely used, they were research curiosities created at great cost.

The emergence of minicomputer technology in the early 1970s ushered in the commercial array processor market. Again, by current standards, these second-generation devices were still primitive machines. Discrete digital signal processing functions like fast Fourier transforms (FFTs), filters, and the like, could be performed on these early devices. But, they were still intimately coupled to their heavily burdened hosts and inefficient in performing their main computing chores.

Increased array processor competition in the mid to late 1970s featured third-generation devices that broke the tight coupling bottleneck. Third-generation array processors are characterized by several factors. For one, they contain enough intelligence to completely absorb an entire multistage mathematical task (auto-correlation or power spectrum density calculations), and leave the host free for other chores. For another, they control the data flow to and from the host processor. This again relieves the host of tedious overhead tasks. And finally, they contain varying amounts of data memory to release the host's memory.

The next step in the evolution of host-independent array processors is well represented by the AP500. It is characterized by more extensive local intelligence and varied I/O capabilities. Other attributes the computer designer should look for in a state-of-the-art array processor are low cost, small size, and broad functionality.

Software control applications

The AP500 is user-programmable at several levels. In addition to calling library K-functions from Fortran, Pascal, or C, sophisticated designers/users write their own Q-functions or executive service subroutines in MC68000 assembly language. They can even create an address generator-pipeline sequencer microcode with the help of the pipeline microassembler. However, with the address generator chaining capability, the ever-growing list of Analogic-supplied K- and Q-functions, and application function subroutines, the users do not necessarily need to write applications in anything but a host-based high level language.

Automatic testing is a prime application of the array processor. For example, communication equipment often has a high digital signal processing

(DSP) content. The production testing of such gear requires test signals to be input and device responses be analyzed. An array processor with optional auxiliary I/O ports forms the kernel of such a test system. The unit accommodates digitized test signals stored in its memory or on a standalone disk. These signals are transmitted to the equipment under test through one of the auxports and a D-A converter. Response signals are digitized by an A-D converter and shipped back to the array processor through the other auxport.

If a fast Fourier transform (FFT) is applied to the received signal, its power spectrum can be calculated and matched to templates stored in the array processor's data memory. The pipeline then determines the quality of fit between the observed and expected power spectra. The control processor, in turn, uses the analysis results to decide if the unit has produced a signal within tolerance. If not, it is subjected to further tests to determine, via signature analysis, where the problem lies. No host computer is required for this application.

In a similar application, the processor can be part of the test equipment contained in a jet engine test cell. Here, output signals of several accelerometers are attached to various sections of the engine, digitized, time multiplexed, and input to the array processor through auxports. The array processor demultiplexes the digital signals and performs an FFT on each of them.

The next procedural step is the power spectrum computation. The array processor compares the intensities at various frequencies to preloaded threshold values. Should a situation arise where the vibrational amplitude at a particular frequency exceeds the threshold, the array processor's control processor transmits a signal (through the serial port or a host computer) causing the engine to shut down gracefully.The threshold values are recomputed at each engine speed change. The AP500's ability to compute FFTs quickly (4.7 ms for a 1024-point complex FFT) allows the analysis to be repeated frequently enough to prevent engine vibration damage.

The unit can also aid in robotics applications. For example, in addition to performing DSP chores, it can perform high speed execution of image processing algorithms. This capability, coupled with those of the control processor, is valuable in object recognition and positioning.

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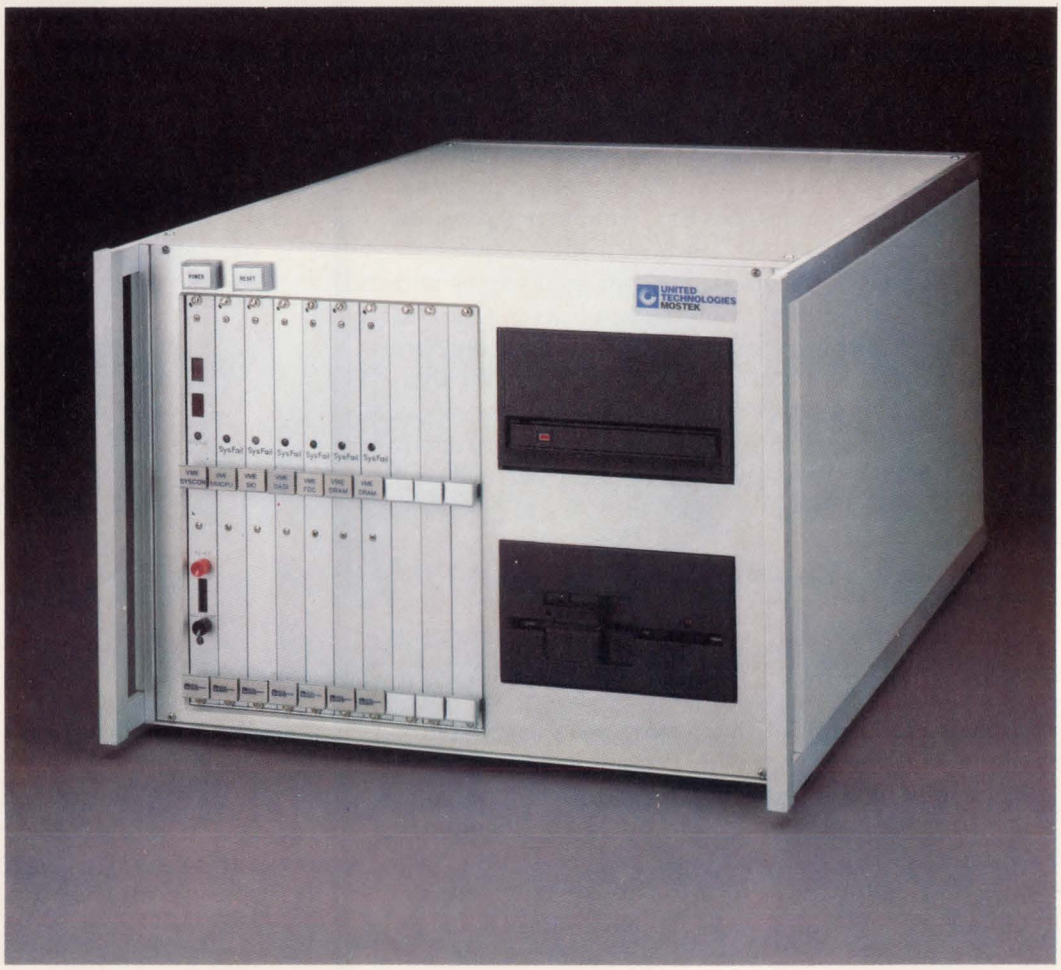

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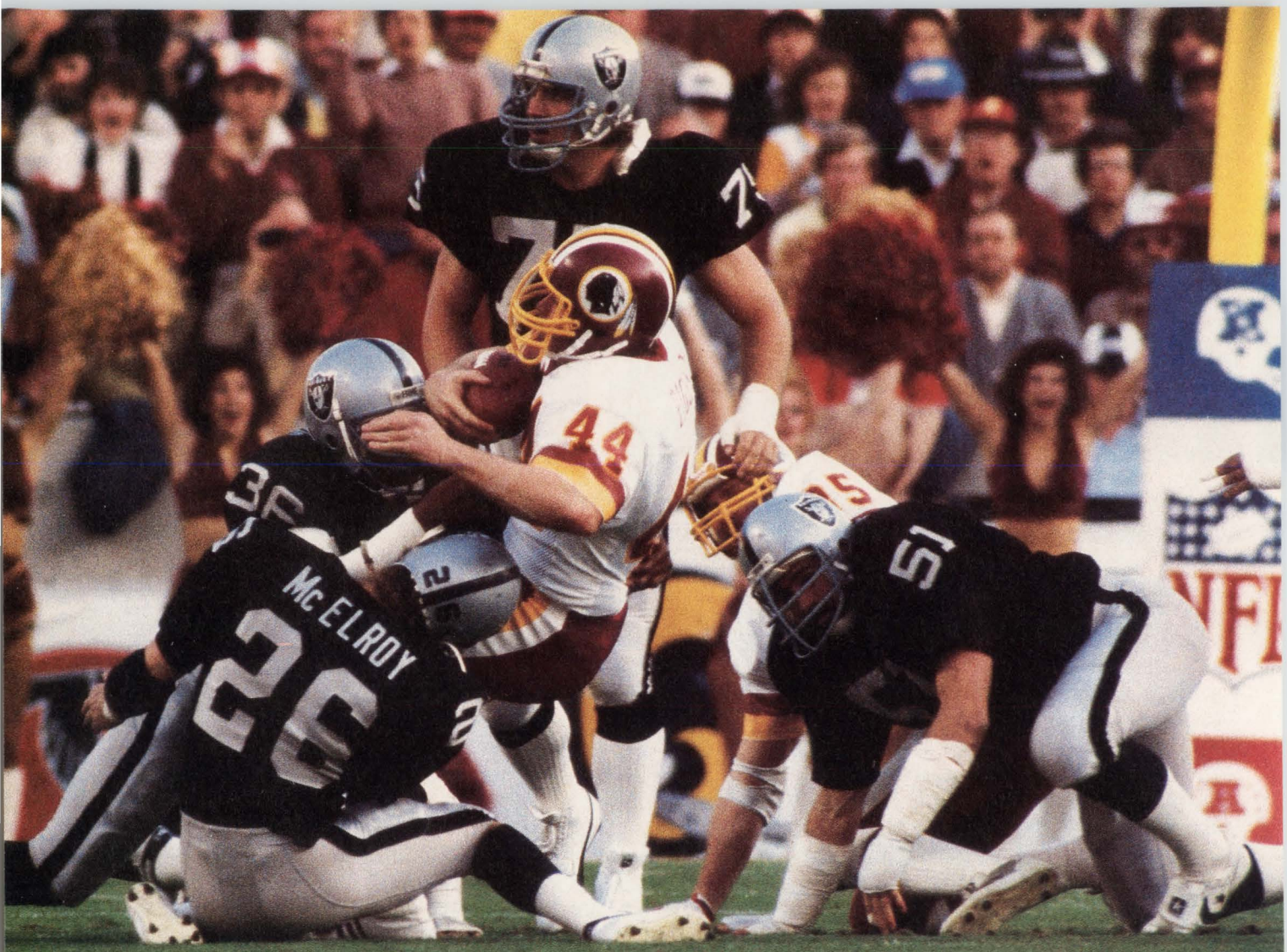

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CIRCLE 40

DATA FLOW CHIP OPTIMIZES IMAGE PROCESSING

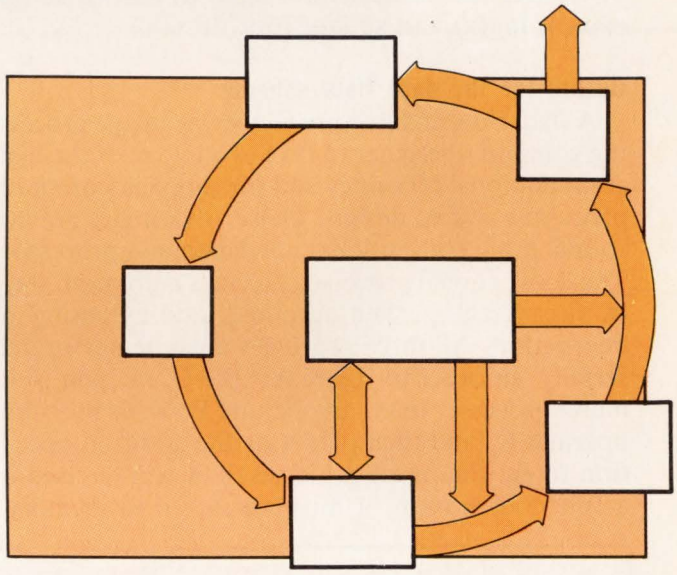
An image processor uses data flow architecture, an internal circular pipeline, and a large instruction set to maximize efficiency in digital image processing systems.

by Yong M. Chong

Image processing system designers must typically make a trade-off between speed and flexibility. If a minicomputer is used for image processing and memory storage, the system will be too bulky and slow for dedicated, realtime applications. If dedicated hardware is added to the system, very high processing speeds can be achieved, but the hardware must be redesigned if a small program segment is changed.

A dedicated, programmable image processor that features data flow architecture can help resolve this trade-off (Fig 1). The NEC μPD7281 image processor uses an internal circular pipeline and a powerful instruction set to allow high end image processing. As a data flow processor, the μPD7281 does not fetch instructions; it processes "tokens" that represent operand data. A data flow architecture allows the processor to maximize efficiency in a variety of multiprocessing applications.

The μPD7281 can be used in design efforts for image analysis, and in pattern recognition for artificial intelligence applications. Its internal circular pipeline allows the processing unit to operate nonstop at a 5-MHz rate. The processing unit contains a 17- x 17-bit (including the sign-bit) multiplier, and an ALU that performs normal arithmetic, logical, barrel-shift, comparison, and bit-manipulation operations. The chip, the first VLSI device on silicon to use data flow architecture, has a more extensive instruction set than conventional von Neumann processors.



The chip is well-suited for image processing applications using algorithms involving two-dimensional convolution, enlarging, shrinking, and rotation. In addition, this digital signal processor is suitable for realtime signal processing applications, since most

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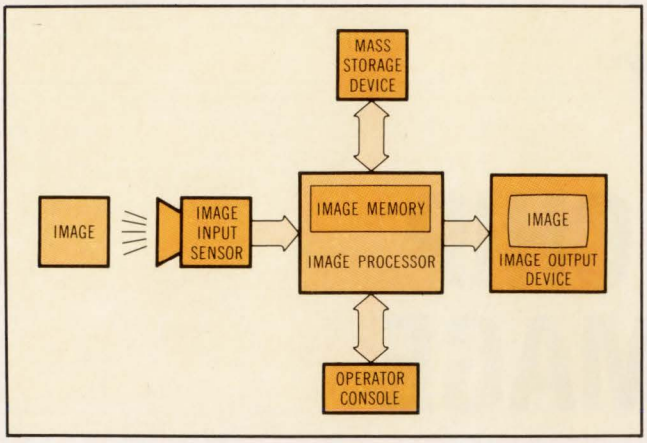

Fig 1 A typical image processing system, regardless of its application, has the same basic parts. Minicomputers and dedicated hardware have been used for such processing. One recent implementation involves NEC's data flow architecture-based VLSI chip.

signal processing algorithms contain large amounts of concurrencies. Finally, the processor is available for numerical processing applications such as matrix-matrix multiplications, matrix-vector multiplications, floating point arithmetics, and realtime evaluations of transcendental functions such as cos(x), sin(x), exp(x), log(x) and square root of x.

Opting for the data flow scheme

A data flow architecture allows the image processing computer designer to take advantage of the high computational efficiency and the simplicity of multiprocessor system design. These advantages are not found in the conventional von Neumann processor. The conventional processor executes a program step, by first fetching, then decoding, and executing an instruction. All three processes must be performed serially. In order to figure A = B + C, the von Neumann processor loads an operand B, loads the other operand C, and then performs the addition operation to get the result A. If result A will be used in a future operation, it must be stored in memory.

A data flow processor does not fetch instructions. It has a program store that represents a form of data flow graph. Each operand data is represented by a "token." This token contains a processor address field, a control field, an identifier (or tag), a data field, and other control fields. During program execution, the data flow processor learns exactly what type of operation will be performed on a token by referring to the data flow graph image in its program store. It can also recognize whether or not all tokens are available for instruction. When all operands or tokens are available, the data flow processor sends the tokens and instructions to the processing unit. The processor also contains local memory to store the tokens (with intermediate results) during computations. Writes and reads to/from local memory are performed concurrently while the processing unit executes an instruction.

A typical data flow processor in a multiprocessing system is shown in Fig 2. In such a design, the only way the processor communicates with the outside world is through the I/O switch. When the host processor wants to communicate with the data flow processor, the host sends a token.

When a token enters a data flow processor, the processor address field of the token is examined to determine whether or not the token is for the particular processor. If it is for that particular processor, the token is accepted. Otherwise, it is sent to the next data flow processor. Clearly, tagging a data token with a specific address enables many data flow processors to be connected in a cascade configuration for multiprocessing.

A data flow processor is data driven. In other words, in each data flow processor, program execution is driven only by the available data needed to execute the program. For example, for a data flow processor to perform the A = B + C operation, the processor must receive a token with the data B and a token with the data C before the addition operation can be performed. These two tokens may arrive in

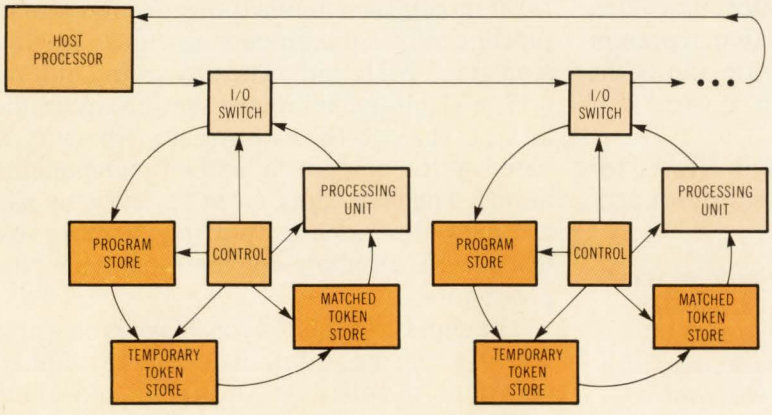

Fig 2 Data flow-based image processors are suitable for a multiprocessing system. The generic design shown provides the basis for the data flow architecture-based image processor that, among its other chores, simulates the I/O switches.

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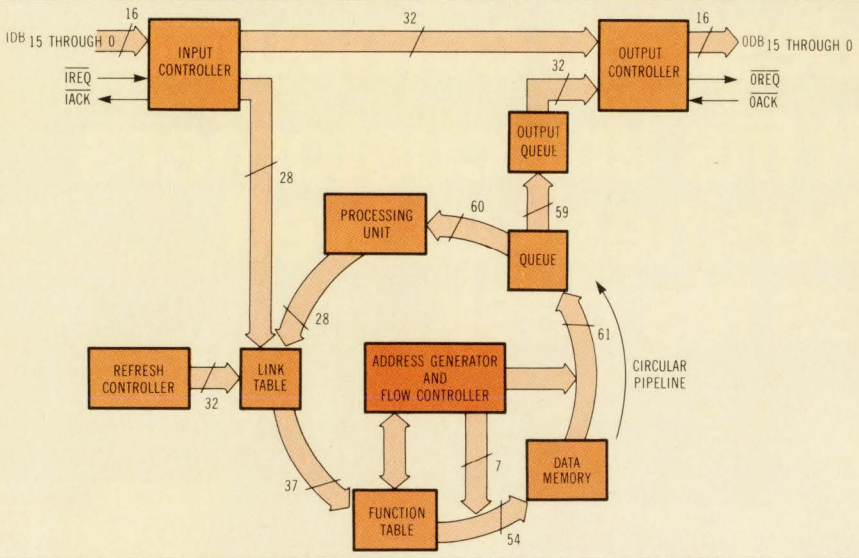

Fig 3 The image pipelined processor is a 40-pin device that can be cascaded to operate in a multiprocessing environment in a variety of image processing systems. Multiple chips can be used in two different basic configurations.

any order due to the data flow processor's token-matching capability.

Token matching for token B and token C can be done by examining each identifier field. From the object code previously down-loaded into it, the processor knows that tokens B and C are to be matched together to form token A. Once the tokens B and C are matched, they are sent to the processing unit for an addition operation. The resulting data is then tagged by the identifier A. If token A is to be matched with another token within the same processor, token A is stored in the temporary token storage memory until the partner token enters the processor. The processing unit can operate nonstop, assuming there are many operations other than $A = B + C$ to be performed.

Achieving multiprocessing power without the need for complex control hardware gives the data flow architecture a major advantage over the conventional von Neumann architecture. Data flow machines do not waste time fetching instructions. Nor do they load and store intermediate results to/from memory during computations.

The image processor's architecture (Fig 3) is based on the architecture in Fig 2. The link table and the function table store object code, while the data memory temporarily stores the tokens to be matched. The address generator and flow controller match two tokens, and the queue temporarily stores the matched tokens before they are processed by the processing unit. The output queue temporarily stores outgoing tokens, and the refresh controller generates refresh tokens. These refresh tokens refresh the chip's dynamic RAMs. The link table, function table, data memory, and queue are configured using DRAMs.

Theme and variation

The input controller and the output controller are equal to the I/O switch in Fig 2. The input controller studies the incoming token's processor address fields. If the processor address matches with an incoming token's processor field, the token is directed to the link table. However, if the processor address does not coincide, the incoming token is directed to the output controller.

There are two basic system configurations for multiple μPD7281s. These are the cascade [Fig 4(a)] and the ring [Fig 4(b)]. A cascade configuration requires that one or more processors feed the input data tokens in from one end, and receive output data tokens from the other end. In a ring configuration, there is an image memory, a host processor, and hardware logic to multiplex data from the host processor and the image memory.

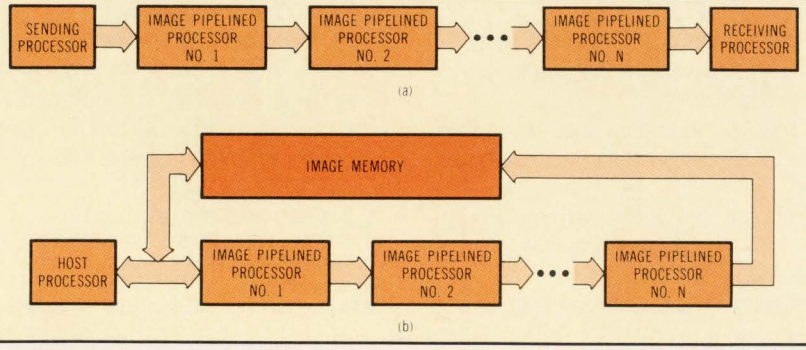

Fig 4 Either the cascade (a) or the ring (b) configurations are useful architectures for systems requiring multiple image signal processors. An additional chip for memory access and bus interfacing is under development to support the ring configuration.

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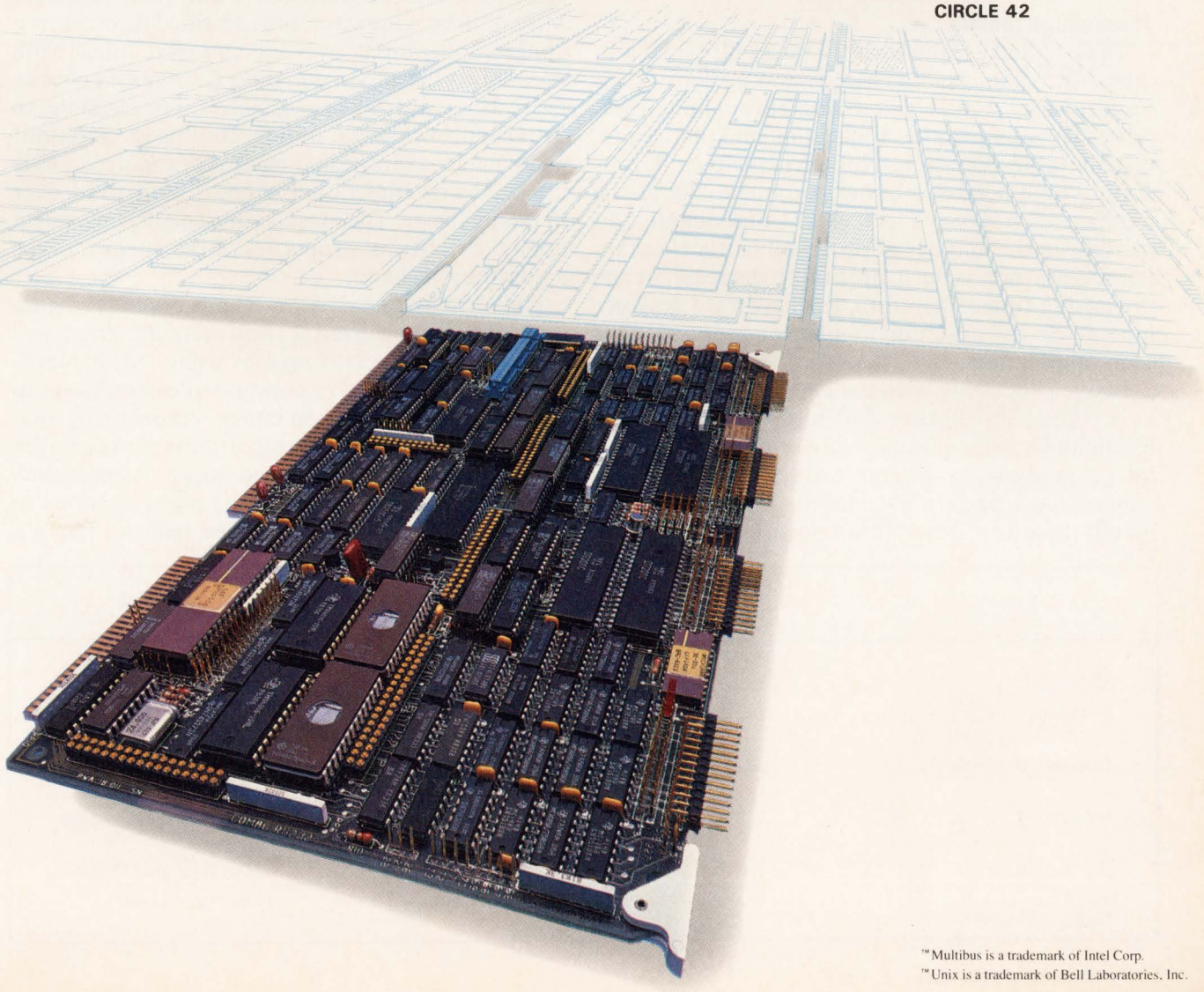

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TABLE 1

Execution Times in a Cascade System

Operation	One Image Pipelined Processor	Three Image Pipelined Processors	Note
Multiplication	22 μs	8 μs	48- x 48-bit = 96 bits
3 x 3 matrix multiplication	24 μs	18 μs	17-bit fixed point
64-stage finite impulse response filter	50 μs	18 μs	17-bit fixed point
Floating point multiplication	4.6 μs	1.8 μs	17-bit mantissa 17-bit exponent
Cosine (x)	40 μs	15 μs	33-bit fixed point

For the ring configuration architecture, NEC is developing a support chip known as the Memory Access and General bus Interface Chip (MAGIC). It handles all token flows between the image processor, the image memory, and the host processor. The MAGIC chip can support up to four image processors. Its other capabilities include self object-code loading and DMA between the image memory and a display processor.

Throughput results

Tables 1 and 2 show what the image pipelined processor chip can do in a cascade and a ring system, respectively. Actual processing throughput rates differ depending on the application and the specific system implementation. However, the overall processing time decreases almost exponentially as the number of processors increases. Consequently, an increase in the number of processors after a certain point does not yield a profitable decrease in the processing time. Therefore, the hardware designer must select the optimum number of processors for each application.

Image processing with the μPD7281 will be useful in artificial intelligence (AI) and other advanced technologies. AI applications are often dependent on image analysis to extract certain features from images; and pattern recognition to classify and match these features with a known pattern. While there are many image analysis techniques and pattern recognition algorithms, not all of these methods work well in each application. Therefore, it is often necessary to modify existing algorithms or write new algorithms for a certain application.

The purpose of image analysis is to divide images in some "meaningful" regions and then analyze these regions for more information. When dividing images, gradient and directional edges, texture, color, and contrast parameters may be considered. Most of these parameters are identified through convolution operations over the complete image with one- or two-dimensional masks. These masks characterize different feature parameters. For example, to extract edges that run only in southwest directions in an image, a directional mask that can detect only the southwest directional edges is convolved over the entire image. The mask's size is highly dependent upon the statistical properties of the image and the application at hand.

Other image analysis methods include region growing, region clustering, and merging. After segmenting an image into regions using various techniques, the shape and orientation of each region can also be analyzed. Once an image is thoroughly analyzed, pattern recognition algorithms are employed to "understand" the analyzed image. As in speech recognition, image pattern recognition attempts to match the extracted and analyzed features (from a

TABLE 2

Execution Times in a Ring System

Operation	One Image Pipelined Processor	Three Image Pipelined Processors	Note
Rotation	1.5 s	0.6 s	512 x 512 binary image
One-half shrinking	80 ms	30 ms	512 x 512 binary image
Smoothing	1.1 s	0.4 s	512 x 512 binary image
3 x 3 convolution	3.0 s	1.1 s	512 x 512 gray image
1024 complex fast Fourier transform	60 ms	24 ms	17-bit fixed point

segmented image region) to a set of features previously stored in the processor's memory. The set of features previously stored in the memory includes the features extracted and analyzed from many known image patterns or objects to be recognized. To obtain such feature parameters from known image patterns, the patterns undergo the same image analysis techniques applied to the image to be recognized. In speech recognition, this process is called "training."

Pattern recognition accuracy

As with speech recognition, it is impossible to exactly match an input pattern to one of the reference patterns. Therefore, a typical result from a pattern recognition attempt is given in a probabilistic manner, such as "76 percent match with pattern number 4." The pattern recognition accuracy depends on how good the feature extraction procedure is, how many feature parameters are used, how many image pattern trainings are performed, and how much of "percent match" is a match.There are many more factors that could be analyzed. But, since the recognition time is directly proportional to the number of parameters to be matched, the parameter number should be as small as possible when a pattern recognition system is utilized.

In medium-level pattern recognition schemes, the designer can develop a pattern description language with a set of primitives and a grammar set. Such a language is useful in describing many interconnected regions within an image. In fact, it may be possible to describe an image with several sentences. This feat is called syntactic pattern recognition. In the syntactic pattern recognition scheme, the designer has to cope with incorrect syntax embedded in the input picture because of noise, perspective distortions, and image patterns that are not in the language dictionary.

In high level pattern recognition schemes, the recognition system has a broad knowledge base on which to call. Moreover, the system can learn from past experience. Learning from past experience means that after a scene is analyzed and recognized, the data and data structures obtained from the scene are stored in a knowledge base's data bank for later use. This type of learning ability is used in AI-based expert systems currently used in defense, medical, and commercial applications.

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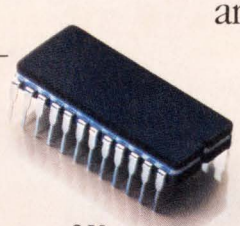

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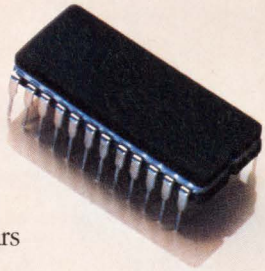

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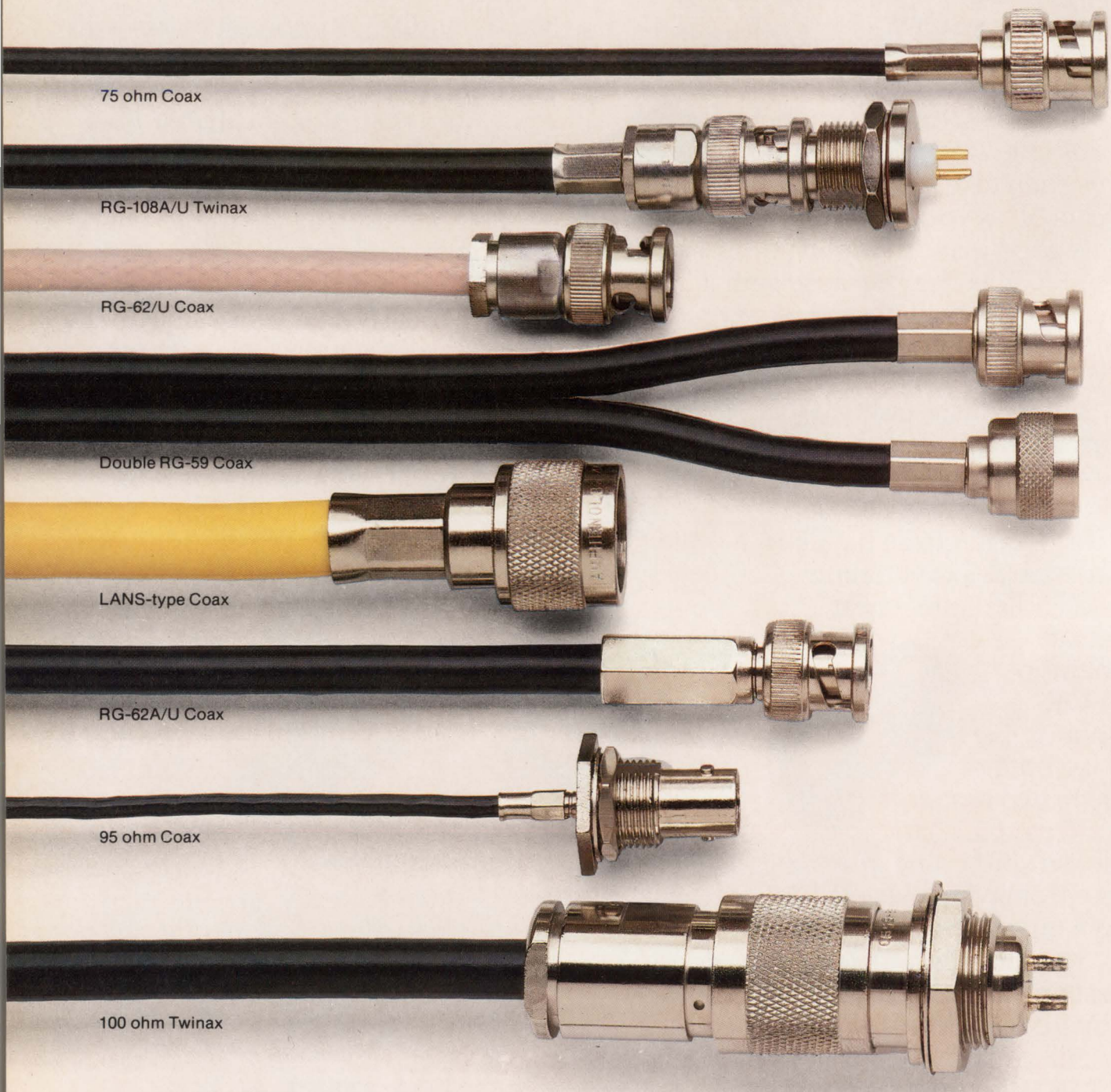

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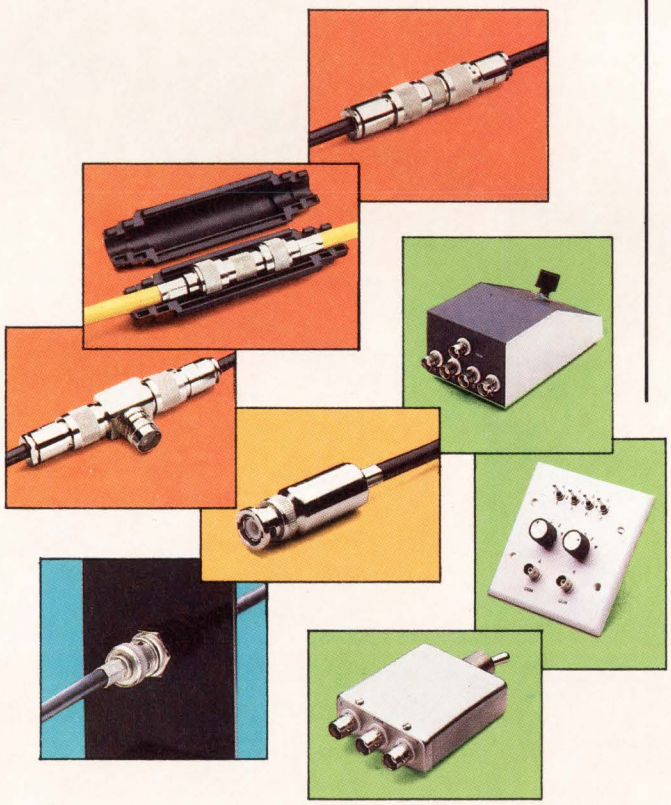

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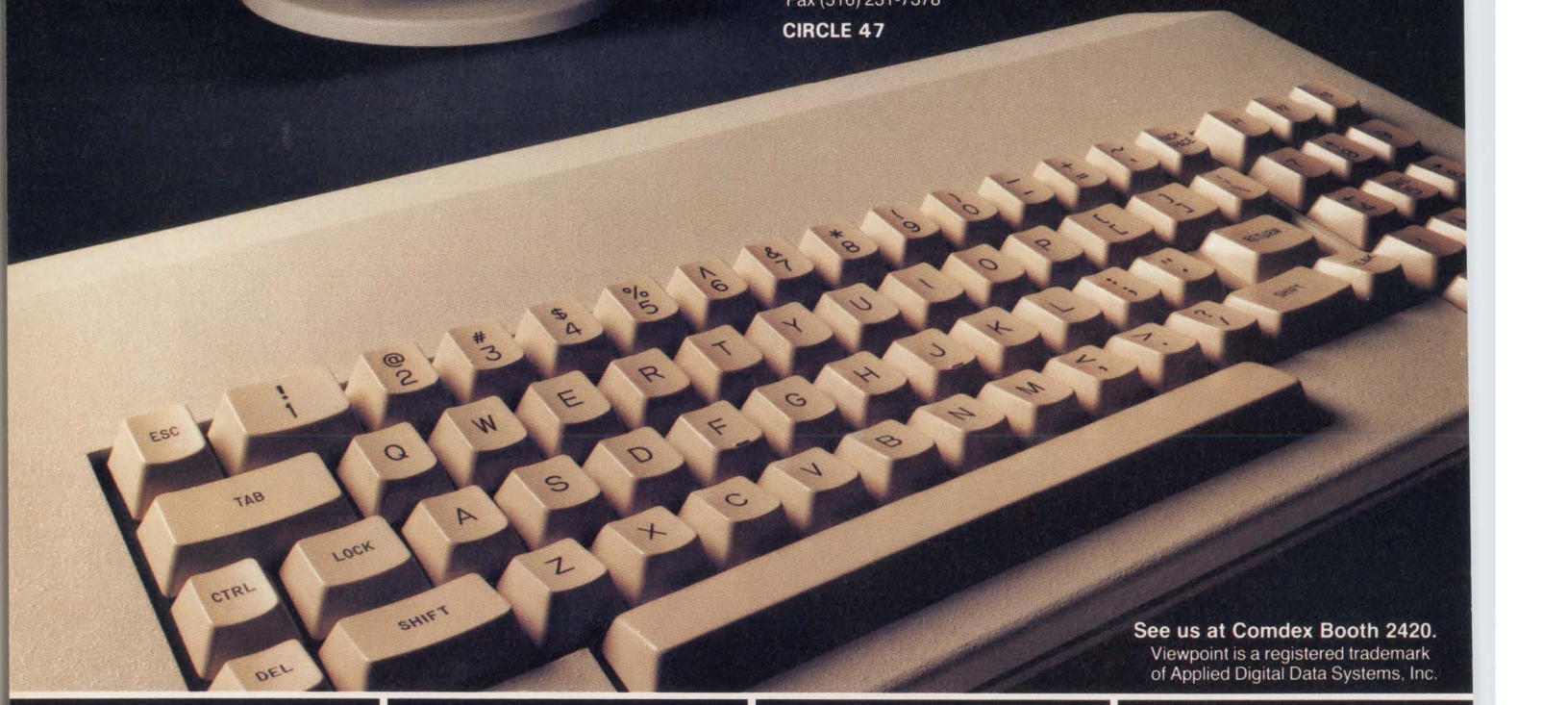

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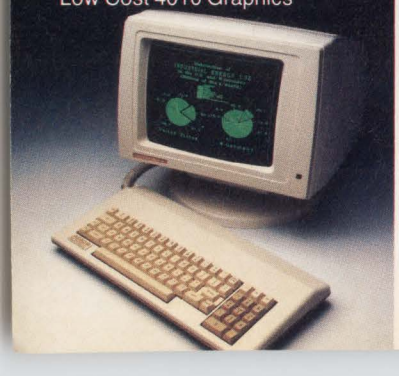

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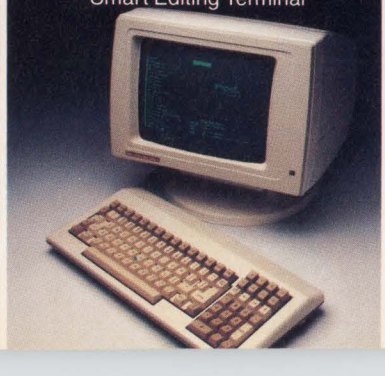

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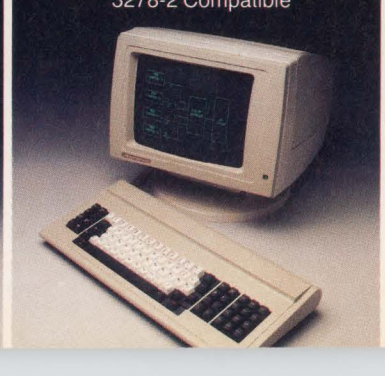

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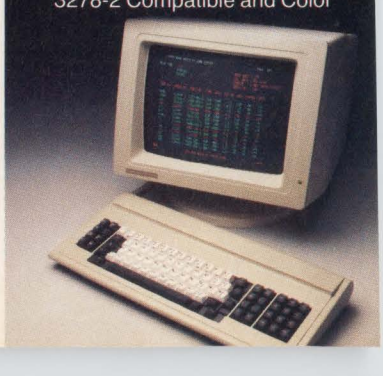

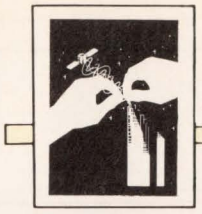

DSP/DEVELOPMENT BOARD OFFERS HOST INDEPENDENCE

The application is programmed, the board is plugged into a Q-bus, and the designer enjoys virtually host-independent digital signal processing.

by George Pawle and Tom Faherty

Designing a digital signal processor that offers the throughput advantages of parallel arithmetic and 32-bit accumulation is not easy. This is because there are few low cost, efficient, single-PC board digital signal processing systems. A processor designed with these concerns in mind would, for example, be able to run at 5 million instructions per second and need only application software to do its job. All the necessary hardware would be in place to fit many applications at the low end of array processor capabilities. These capabilities include speech, image, and communication processing; vibration analysis; realtime control; and digital filtering.

George Pawle is a senior product development engineer at Sky Computers, Foot of John St, Lowell, MA 01851, where he is responsible for the SKY320 digital signal processor. He holds a BS in chemistry from Tufts University.

Tom Faherty is a system engineer at Texas Instruments, Inc, 504 Totten Pond Rd, Waltham, MA 02154, where he is responsible for application/sales of semiconductors. He holds a BS in physics from Holy Cross College.

Such a processor, the SKY320, is now available and can be plugged into Digital Equipment Corp's popular PDP-11 minicomputer-based Q-bus. Its board is also capable of standalone operation. Moreover, by redesigning its onboard modular bus interface, it can be made compatible with virtually any mini- or microcomputer.

Central to the board's hardware architecture is its fast, four-port data memory. All the board's major buses have access to this memory. With a fast, static RAM, the board also provides the maximum program memory space that its onboard TI TMS320 digital signal processing (DSP) chip can address.

A major part of the SKY320 (Fig 1) is its Q-bus interface that connects the host computer with the processor. The interface (Fig 2), consisting of a transceiver set (a DEC-provided chip set), detects the address and data sent from the Q-bus to the processor, and vice versa. It also includes a status control register for operation control such as status reports. A general-purpose, 16-bit wide communication register, with no specified hardware function, is software controlled for transferring data words between the board and the Q-bus.

The Q-bus is connected to a tri-state bus known as the Q-bus interface bus (QBI bus). This bus connects the Q-bus to the status control register, communication register, the P-(program) memory address, the P-memory data register, the D-(data)

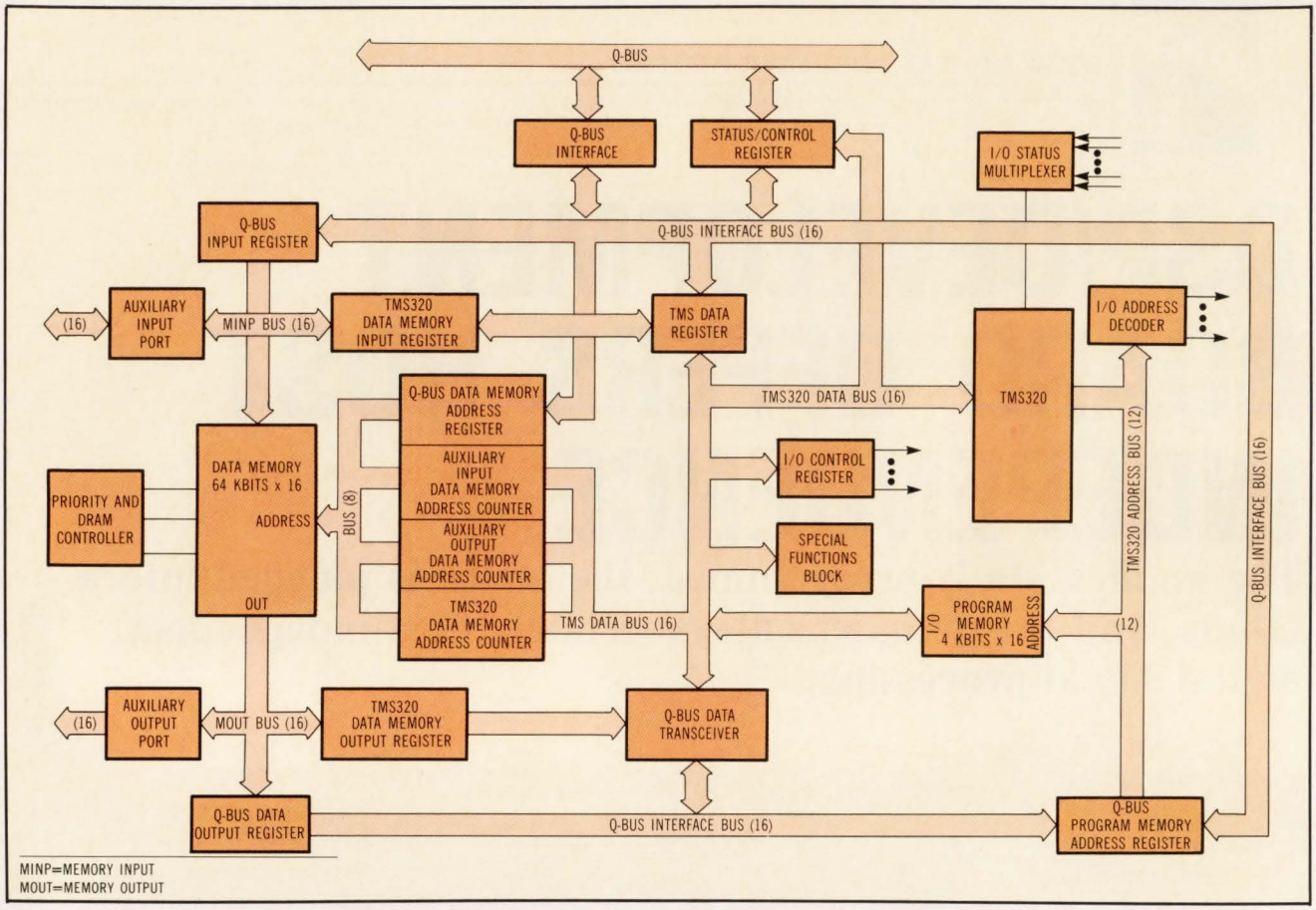

Fig 1 The SKY320 application processor/development board is centered around the TMS320 digital signal processing (DSP) chip. Designed for connection to the Q-bus and other host buses, the board operation is almost host independent. Only application software need be written.

memory address, and the D-memory data register. It incorporates interrupt control that allows the board to interrupt its host on two independent channels. The interrupt control also permits the Q-bus to interrupt the board on two interrupt channels. From the host side, the Q-bus interface uses four words in four consecutive addresses in the I/O page of the Q-bus to transfer data to and from the board.

The first word is incorporated in a 16-bit wide status control register, while the next word is allocated to the communication register. The third word is assigned to the address for the D-memory transfer. Finally, the fourth word is allotted to the data that handles transfers to or from the D-memory.

The status control register is used to start and reset the DSP chip. This register also determines whether or not a data transfer corresponds to data in the board's P-memory or D-memory. As might be expected, an interrupt-enable signal prevents the processor from interrupting the host. Furthermore, six programmable status lines (with no hardware definition) are used to provide information on either the interrupt type or board processor status.

The communication register allows a 16-bit data word to be transferred between the board and the host without an address register. Since data organization on the board is by word (16 bits/word), it is convenient to be able to send 16 bits of data directly, without having to use an address. Otherwise, the bits would have to be controlled by the 6 bits in the status register. Or, they would have to be put into the D-memory. This latter procedure requires an address from both the DSP "side" and the Q-bus "side," (and is useful for interrupt routines). When an interrupt to the board occurs, data can be quickly sent to and from the host with little overhead.

Inside story

A look at a realtime board application shows the relationship among the various board function blocks. A loosely coupled application like a finite impulse response (FIR) filter requires that a program be loaded from the host onto the board. This starts the DSP chip. Then, without host intervention, the board will take a word in continuously from its auxiliary input port, process it through the filter, and send a single word out through its auxiliary output port.

Another example is a realtime spectral analysis with a 1-Kbyte complex fast Fourier transform (FFT). The FFT operates in the same way as the FIR

filter except that it works on data blocks, and its output is displayed. For a loosely coupled system like this, only downloading is necessary. In contrast, a tightly coupled system requires that data be brought in from an auxiliary input port to the D-memory to have a signal processing operation done (eg, edge enhancement). Once the edge enhancement is performed, the host is notified to save that data. The host picks the data out of D-memory and stores it on a disk, one line at a time, if necessary.

The DSP is a fixed point arithmetic chip, and block scaling is needed to handle wide dynamic range data. The amount of shift in the chip's barrel shifter is fixed, making dynamic scaling difficult. So, the board designers opted for a register checker on the DSP's data bus. This register looks for the maximum absolute value bit transferred on the bus in a given time period. It can be reset to zero and read back, and turned on and off.

As stated above, the register checker tells the board user the maximum value transferred on the bus in a given time period. Thus, computer designers need not do any internal testing (through DSP-based software) to find the largest magnitude of transferred data. Since the register automatically reports, a single chip can handle all dynamic scaling—a useful feature for high dynamic range FFTs.

The board interrupt consists of a single programmable logic array (PLA) that can handle six interrupts. The reason for such complex interrupt logic is simple. Such logic allows the designer to expand the DSP's single interrupt line to accommodate six possible interrupts. Two come from the host, and four are generated by the auxiliary I/O ports. Of these six interrupts, five are maskable. These have enable bits that prevent or enable an interrupt under application software control. The sixth interrupt (from the host) is nonmaskable. Thus, if the DSP is ready for interrupts, it can receive one from the host regardless of other events.

Interrupts are gated with an AND gate with the enable. Then, all of the interrupts which pass through the gate are ORed together and sent to the DSP's interrupt line. The interrupts, as they come into the PLA, are saved in a recommended standard flipflop that holds the data until the interrupt is acknowledged. Finally, the PLA allows the designer to clock the output of the interrupt line with the chip's system clock.

The operational key

The heart of the SKY320 board is the TMS320 DSP chip (Fig 3) and its associated circuitry. Since the board sports two separate tri-state buses for address and data, the DSP chip presents both address and data to the board simultaneously to speed data transfer.

The board's P-memory is 4-Kbit x 16 static RAM with a 70-ns access time. It is connected to the address bus. Also connected to the address bus is the chip's port selection circuitry for its eight I/O ports. The P-memory address bus uses the Q-bus address register to access the P-memory that initializes the DSP's application program. There is a connection to the

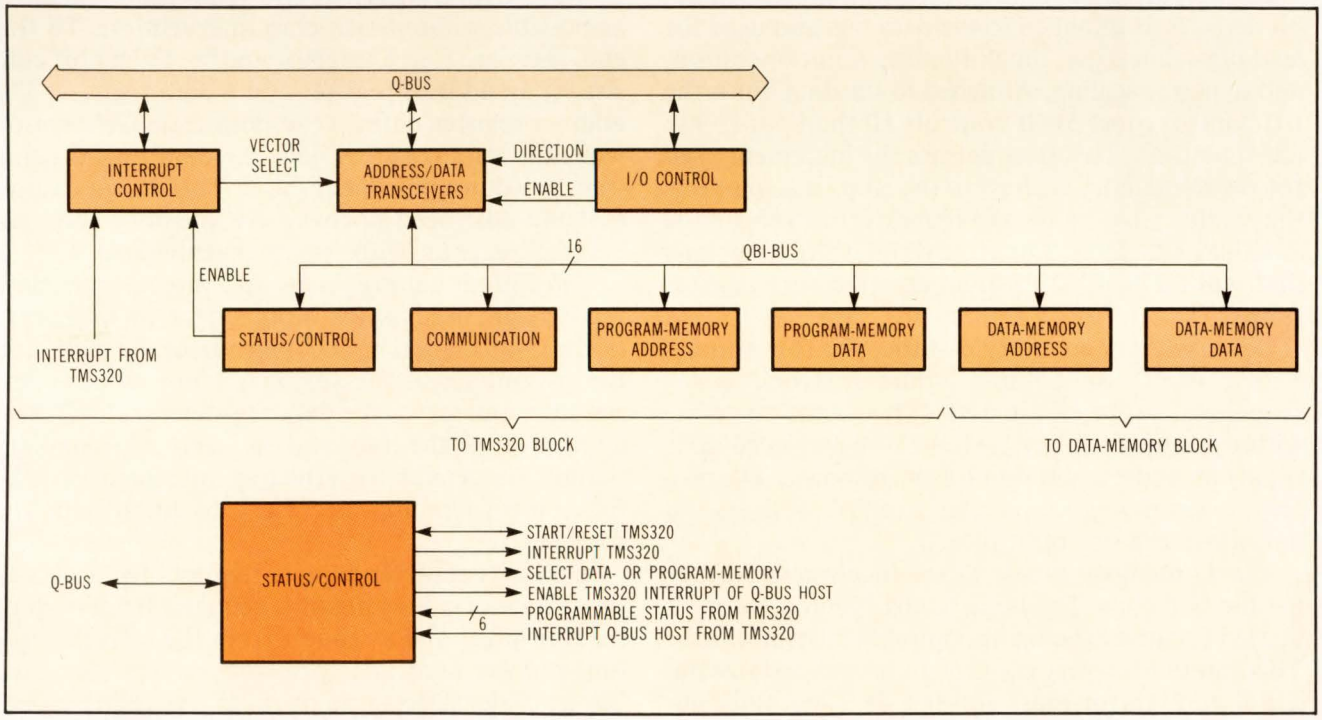

Fig 2 The Q-bus interface of the board depends on address/data transceivers built from a DEC-provided chip set. Interrupts may come from either the host computer or the DSP chip and the board's data and addresses are divided into two parts as shown.

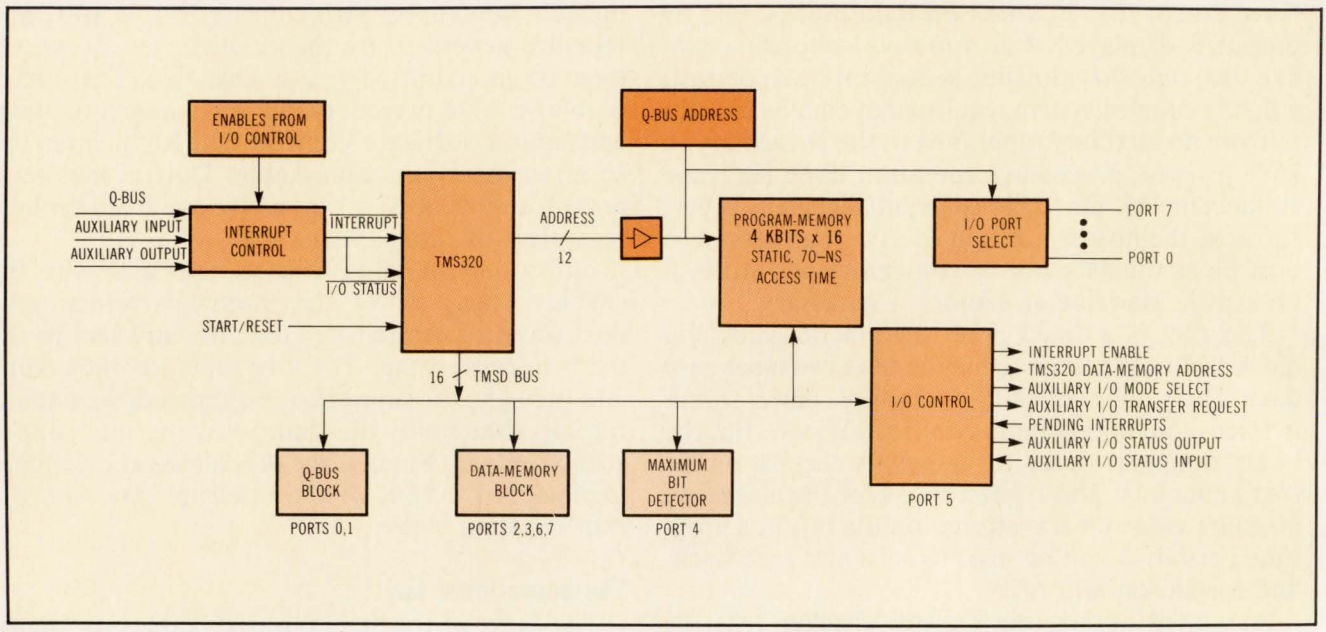

Fig 3 The board's chip block is key to the application processor/development board operation. Eight I/O ports handle the board's Q-bus, data-memory, I/O, and maximum bit detector. The DSP chip can be interrupted from the Q-bus, the auxiliary input, or the output.

Q-bus block (on the data bus attached to the chip) that allows the Q-bus to transfer data to and from the communications and status register.

A connection to the D-memory block uses ports 2, 3, 6, and 7 of the DSP chip's I/O space. This design helps define the address registers used for transfers to and from the D-memory to the DSP chip's and the auxiliary I/O ports. Actual data transfer occurs via a separate data register.

For its part in the board operation, the maximum bit detector is attached to the data bus and used for lead digit detection, block floating point operation, and dynamic scaling. Attached to the data bus is the I/O control (port 5). It controls all the board/chip I/O functions. This port defines the increment used for the D-memory address to the chip. It also selects the auxiliary I/O mode and requests transfers on the auxiliary I/O ports. Lastly, it defines the interrupts that will be enabled to input the interrupt register status.

Because the P-memory is static, the row address strobe (RAS) or column address strobe (CAS) sequences can be eliminated. (This cannot be done with dynamic memory.) All the designer need do is supply an address and wait for the response. The procedure is simple since the TMS320 chip's address and data lines are not multiplexed.

The D-memory block allows local mass storage for the DSP chip. The large board-based memory is needed because the chip has only 144 internal words. This amount is a very convenient scratchpad size but is not enough for mass storage. It is certainly not enough for data processing, or DSP.

The 100-ns access time, dynamic RAM-based D-memory is organized into 64,024, 16-bit words. Such speed is necessary to keep pace with the chip's cycle time. The chip itself is a dynamic device. Thus, the designer has to keep its clock constant. In other words, to achieve the maximum transfer rate (in and out of the chip), the 200-ns cycle time must be matched to that of the chip.

Four ports needed

The D-memory organization is designed to allow as much data transfer to and from the D-memory as possible without DSP chip intervention. To this end, there are four D-memory ports. Each port consists of an address register and a data register. The address register defines the data transfer location while the data registers hold the data that is being transferred in a pipeline fashion. This design ensures that the port need not wait for memory response before it gets on with its other activities.

Three input data registers and three output data registers are used on the input side. One takes care of the Q-bus, another accommodates the chip, and the last one serves the auxiliary input. On the output side, one serves the data register for the Q-bus, another serves the chip, and one serves the auxiliary output. Associated with the dynamic memory is all the control circuitry necessary to implement the four ports.

A priority resolver accepts requests for access to the D-memory. Five possible requests from each of the four ports and a request from the refresh clock time-out are used. The priority resolver (for each 200-ns cycle) selects one of these five requests and gives it to the dynamic RAM controller. The DRAM controller provides the signals to the D-memory needed to define the address. It also handles the data

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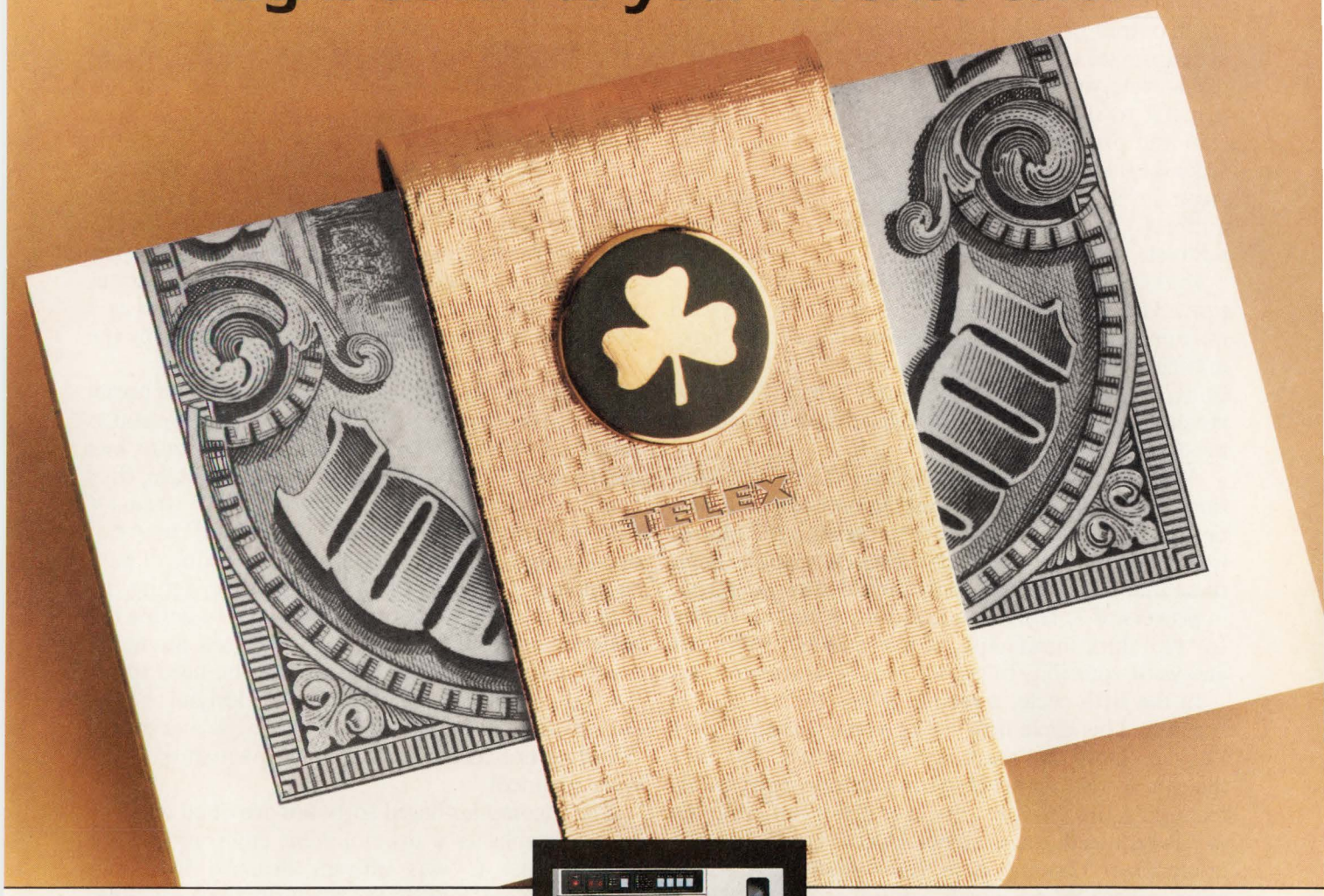

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CIRCLE 48

as it goes into the memory or comes out of it. The signals are the standard signals for dynamic memory—the RAS, CAS, and write enable.

The chip communicates with the external D-memory in several ways—all based on the system clock output provided by the chip (Fig 4). This clock synchronizes the entire board and chip. In the first clock cycle, an instruction defines the address of the transfer to the D-memory. This is an OUT instruction and proceeds through port 2 of the chip. The second cycle is used to output data and transfer data from the chip to the register used for the D-memory address. The D-memory actually stores a new address.

In the third cycle, the chip initiates an IN instruction. This instruction starts a read from the data memory. In this cycle, the D-memory has now automatically (as a result of the previous OUT instruction), already been read from the D-memory. This means that during the third cycle, data is ready to be clocked into the chip.

After data is clocked, the address associated with the D-memory transfer is incremented, and a new data transfer from D-memory to the output data register is started. This data transfer is a variable increment that can be added to by the I/O control register in powers of 2, from 1 to 128. This feature is useful for FFT data interlacing. It can also be useful for arrays or rotations in two-dimensional transforms.

In the fifth cycle, a second IN instruction is performed. This cycle now looks exactly like the first IN cycle. Note that the board can transfer data into the chip as fast as this chip can generate instructions to initiate the transfer. So, if a 256-point complex FFT is required, the designer has to set up that FFT in blocks of 32 points each. Each block of 32 points must consist of 64 words—one word for the real part, and one for the imaginary part of each complex point. The transfer is accomplished by a series of 64 consecutive IN instructions. This minimizes the overhead needed to transfer data in and out of the chip.

Once the block of 32 complex points has been operated on, it is again output to the D-memory. Now a sequence of 64 consecutive OUT instructions is in order. The overhead is just a single OUT instruction to define an address at the block transfer beginning.

The auxiliary I/O ports transfer real-world data into and out of the SKY320 board; they are directly connected to data memory. This design allows data to be transferred into the board at rates up to 5 MHz/word. This rate is possible only if one port at a time is active. If additional ports are active at the same time, they can each achieve a throughput rate of 2.5 MHz/word.

Keep in step

The board operates synchronously for two reasons. First, the chip is a synchronous device. Second, to achieve very fast processing speeds, the designer should stay away from asynchronous operation and its processor wait states. Once wait states are available, there is a tendency to use them as a design convenience, thereby letting speed fall by the wayside.

Speed also plays a part in the auxiliary I/O ports. Each of these ports has eight programmable status bits (four input and four output). These status bits can be used for several purposes. For example, they can modify or define the type of "data" transfer that is occurring on the port. The "data" may not necessarily be actual data. It might be control data to set the clock rate of the transfer, to define the number of words to be transferred, or to define the address and D-memory where the data might be transferred. The "data" could also be used to set up a special software protocol. This design is necessary if there is an external device with a protocol that does not correspond to the implemented hardware protocol.

The C compiler-based software provided with the board establishes a development environment for applications. C was chosen because it allows designers to get closer to the hardware than any other high level language. To optimize time-critical parts of the designer's application program, facilities for generating inline assembly language code are part of the C compiler. There is also a macro-expander that generates the chip's inline code. Finally, an "include facility" provides a set of library routines.

A linker is not provided. The "facility" differs from a linker in that it actually incorporates assembly language programs into another assembly language

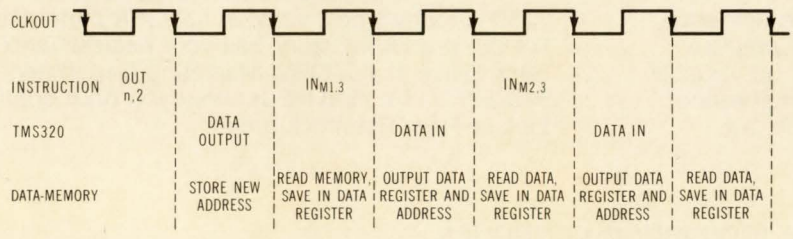

Fig 4 Data-memory timing is accomplished for a two-word read with all operations in either the DSP chip or the data-memory are controlled by the DSP chip-furnished CLKOUT signal. This signal also synchronizes all other DSP board operations.

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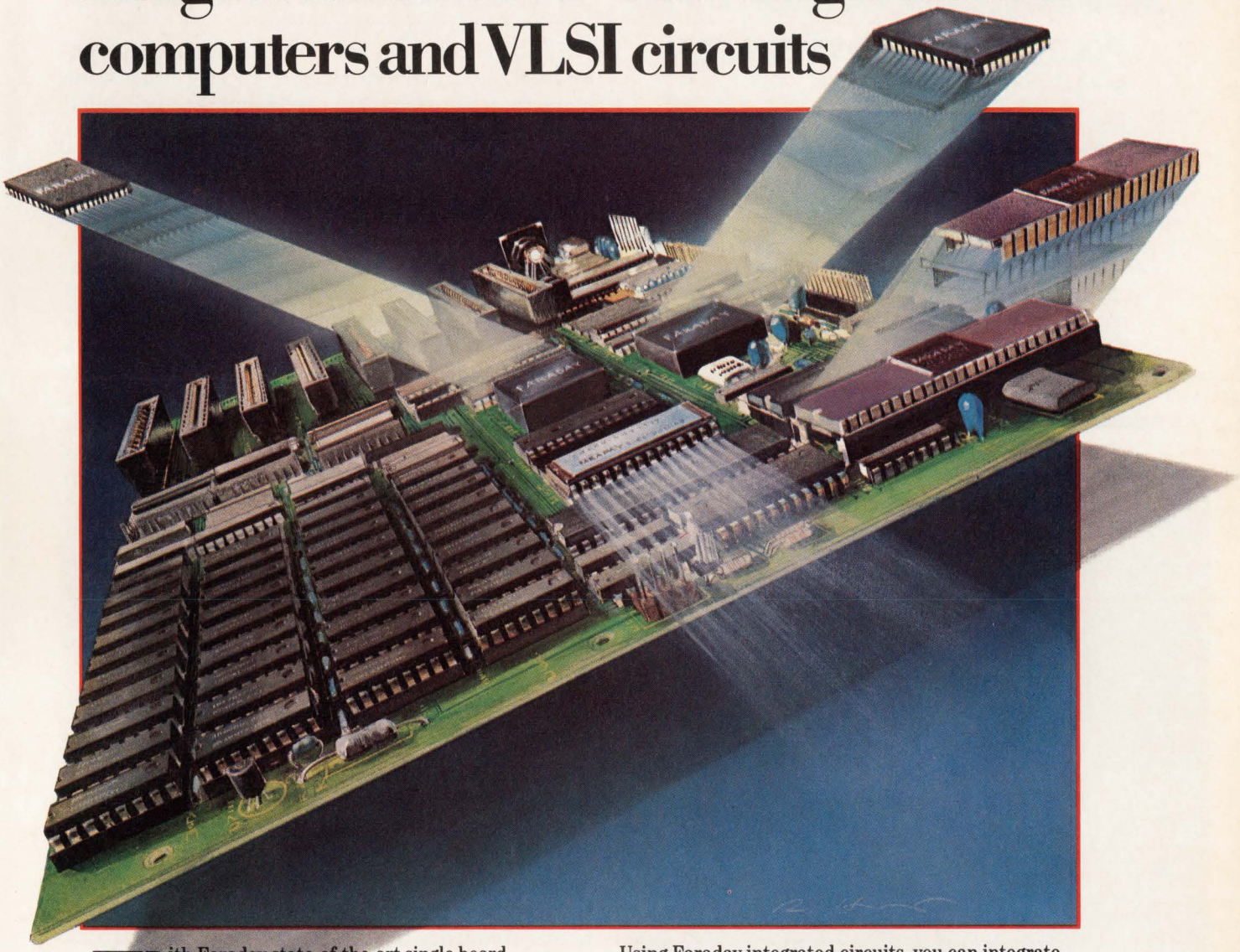

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program before the assembly state. In contrast, a linker adds programs after the assembly state. Or, in other words, a linker ties "everything" together after "something" is assembled.

Since only 4 Kbytes of program space are available on the TMS320, there is no need for a linker with the facility. The assembly language code is either generated directly, or through an absolute assembler that converts the assembly language code into machine code. This code can be directly downloaded into the chip. The generated machine code is loaded into the chip through a set of software routines from the host (the host operating environment).

The high level language subroutines have parameters that allow the board user to specify either a file name for a file of machine code that is to be loaded into program memory, or a file name of data that is to be loaded into the data memory. The host operating environmental control also allows the designer to easily start and stop the chip, transfer data directly from arrays, and look at the chip's D-memory.

Spectral analysis is a software-intensive application for the board. In this application, data is read in through the auxiliary input port in blocks of 1-K real points. This data comes into one area of the data memory. When the block is full, it is then Fourier transformed, using a 1-K complex FFT. A complex FFT is done on real data by zeroing all the imaginary points. By incrementing the data memory address by two, the board zeroes out the imaginary part and uses the complex FFT to transform real data.

Once it is transformed, the data is put in a third area of data memory and output through the auxiliary output port to an X-Y display. An X-Y display is handled by requiring that every other point (in this third area of data memory) correspond to a fixed X coordinate. The output of the FFT then becomes a variable Y coordinate. This output comes directly out of the output port to an X-Y scope. Actually, it goes through a D-A converter and then goes to the X-Y scope where the realtime display of the FFT of, for example, voice data, is observed.

Note that the 1-K complex FFT takes 30 ms. But, the display refresh rate is such that 50 ms is needed for each data block. These figures allow 20 ms for software manipulation (such as looking for a particular frequency or looking for frequency errors). Clearly, sufficient time is left to do a realtime analysis of the problem at hand.

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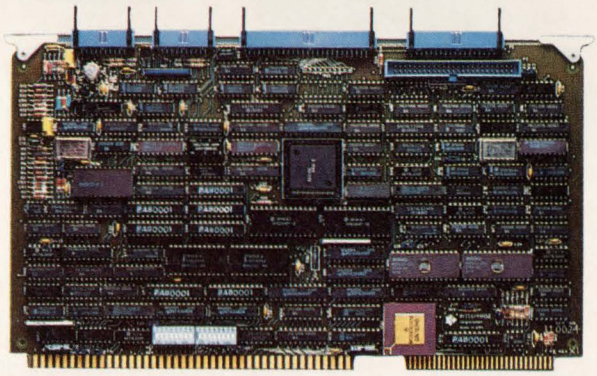

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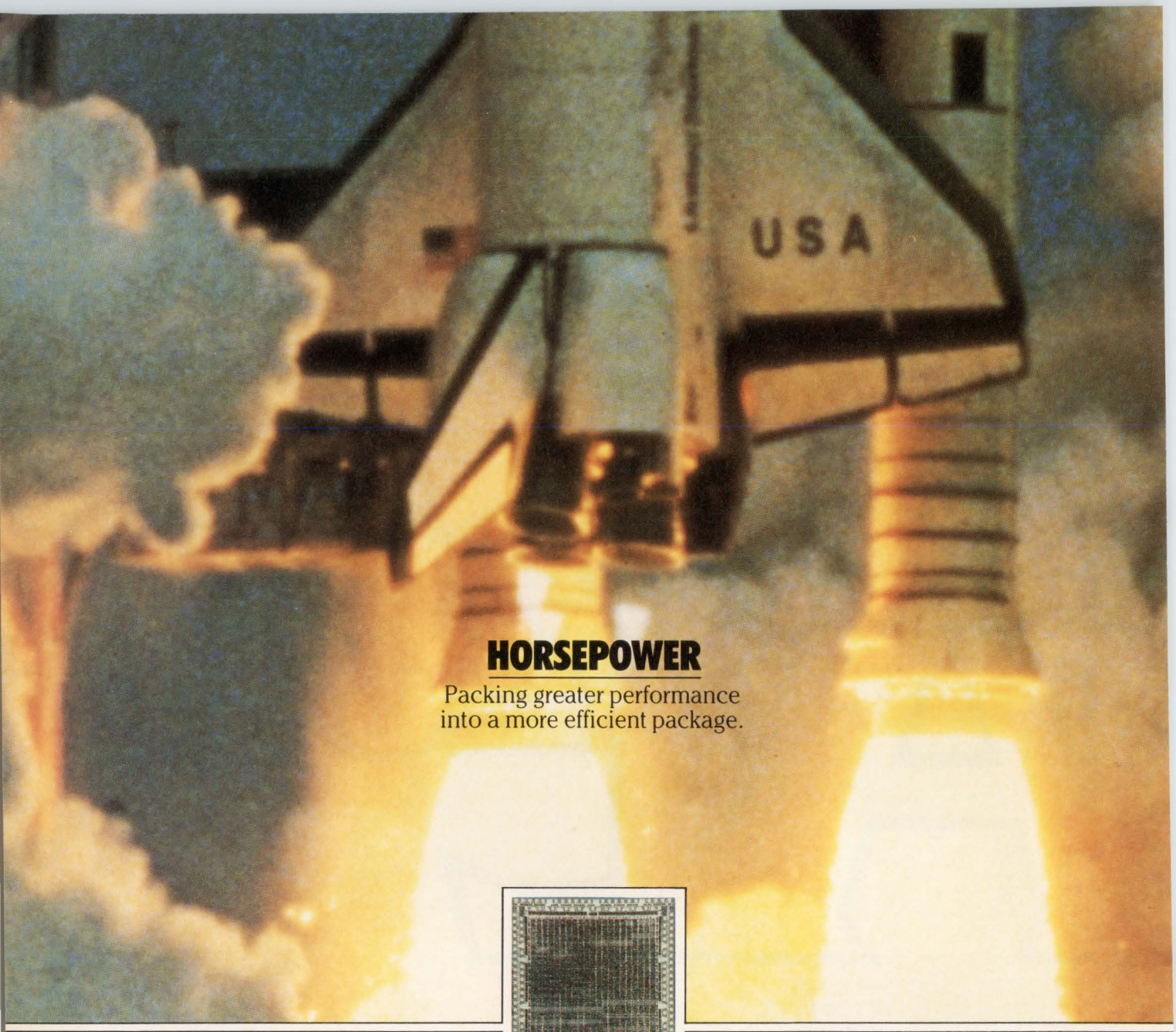

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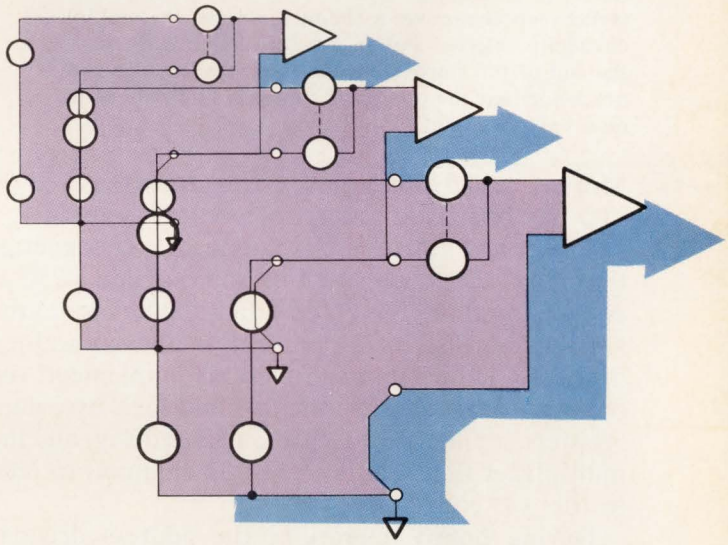
ANALOG BOARD CUTS DATA ACQUISITION COSTS USING STD BUS

In computer-based industrial measurement and control environments, an STD bus-compatible analog input board can cut data acquisition cost per channel by 60 percent.



by Andrew Davis and Steve Connors

To effectively serve industrial control applications, data acquisition boards must be able to withstand harsh environments while allowing system designers sufficient flexibility. Environmental considerations dictate that the boards must withstand high temperatures as well as electrical and magnetic interference and noise. Furthermore, the products must deal with the low analog-signal levels typical of industrial sensors, and they must be able to reject the common-mode voltages that often appear between sensor ground and A-D converter ground. They should be available in several configurations to permit precise system tailoring to user needs.

It should be easy to design such data acquisition boards into industrial control systems. After all, system designers should concentrate on the process being controlled, not on the electrical and mechanical nuances of the analog input board that interfaces a controlling computer with the process. Therefore, data acquisition devices should easily interface with other functions within the process control system.

Andrew Davis is vice president of sales and marketing at Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. He holds a BS and an MS in materials science from Cornell University and an MBA from Harvard University.

Steve Connors is director of analog devices at Data Translation Inc, where he is responsible for analog designs for I/O boards and data acquisition modules.

In addition, they should be low cost, giving designers more money to spend on such critical process control system components as transducers and actuators, whose mechanical nature precludes the cost reductions typical of solid state electronics products.

An analog input board for the STD bus

An example of such a board-level data acquisition product is the model DT2712. This 32-channel, 3330-sample/s analog input board for STD bus systems is compatible with 8- or 16-bit CPUs. The STD bus, a microcomputer bus based on a modular, small board format (in contrast to the large board format of the Multibus), lends itself to low cost systems. Its bus structure is straightforward to simplify system design, and its modular architecture permits design flexibility. The various STD bus boards available allow a system to be tailored to user needs. No performance shortcuts need ever be taken, but no expensive, unnecessary extras need be included either.

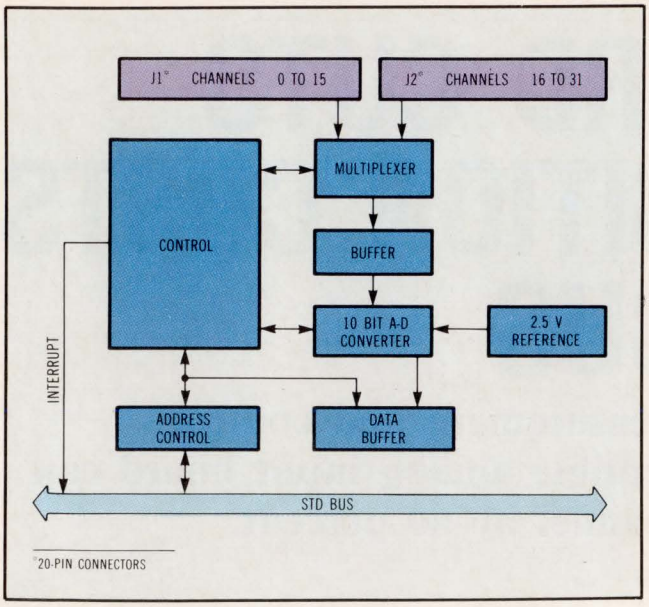


Fig 1 The analog input board multiplexes 32 analog inputs to a 10-bit A-D converter. When the control and status register receives a channel address, the multiplexer channel is selected and an A-D conversion is started. At the end of the conversion, the interrupt line signals the processor that the process is complete and data at the data buffer is valid.

Moreover, the 8-bit microprocessors often used on STD bus boards are ideal for control systems.

The board's structure includes an A-D converter that is a CMOS IC with 10-bit resolution and a 250-μs conversion time (Fig 1). The digital interface to the STD bus consists of a data buffer and an address decoder. Other board functions implement the control/status register, the low and high byte data registers, an interrupt control, a 50-μs delay, and the multiplexer that selects one of 32 channels to feed to the A-D converter.

During board operation, the address decoder looks for valid commands sent to the board, and controls the tri-state data buffer's mode. If a received command is a read operation, the data buffer writes to the bus. If the command is a write operation, the buffer reads from the bus. During other operations, the data buffer is placed in a high impedence mode. Writing a valid channel address to the control/status register triggers the 50-μs delay. This gives the selected channel time to settle before conversion begins. After the conversion is complete (as signaled by an interrupt or by the control/status register's A-D done bit), the data register's low and high bytes must be read, in that order, to clear the board. Once the board is clear, it is ready for another conversion.

To furnish its cost/performance features, the board includes numerous circuit design innovations. For example, to operate the A-D converter over a 0- to 5-V input range requires that it operate from an 8-V supply. Because the STD bus's supply is 5 V, an onboard charge pump is included to boost the STD bus to the 8-V level. A charge pump, however, can introduce noise problems. These are avoided by synchronizing A-D conversions so that they occur between the charge pump's noise spikes.

The sample/hold function, which maintains a constant input-signal level during the A-D conversion process, is another problem. Most sample/hold chips require bipolar supplies—they will not work with the unipolar supply available on the board. Using the multiplexer along with a capacitor as the sample/hold results in sample/hold performance specifications that include a 1-mV/ms droop rate, a 200-ns aperture delay, a 50-ns aperture uncertainty, and a feedthrough attenuation of -66 dB at 1 kHz.

The board's CMOS components also contribute to its low cost and interfacing simplicity. The components' low power consumption allows the board to derive its power—250 mA at 5 V—from the STD bus. This eliminates the need for an expensive external power supply. To ensure flexibility, the board can be mapped into either the memory or I/O space of the CPU, and can support either software-polled or vectored interrupt schemes.

Interfacing considerations

A host CPU communicates with the board via a command/status register. Writing a channel to this register initiates a conversion. The host then reads two data registers when a bit in the command/status register indicates an end of conversion or when the board generates an interrupt to signal that data is ready. In keeping with its low cost and interfacing simplicity, the board has no error bits that must be monitored by the host CPU before the host inititates a conversion or reads results. However, the host's software must ensure that all old data is read before requesting a new conversion.

Optional screw-terminal panels simplify connections to transducers while providing designers with sufficient flexibility to adapt the board to user needs. These panels can accommodate active and passive components for signal conditioning and input protection to ± 100 V. Contributing to its low cost, the analog input board accepts 32 single-ended inputs. However, adding two fully populated boards allows the input board to digitize 32 differential inputs. Unpopulated versions can accept 250-Ω resistors to convert the 4- to 20-mA signals typically found in process control applications to the 5-V, full-scale level.

The board can operate with Z80, 8080A, 8085, 6800, 6802 or 6809 microprocessors serving as the host CPU. An onboard jumper allows synchronization differences between these two groups of processors: the Z80, 8080A, and 8085 in one group; the 6800, 6802, and 6809 in the other.

The host processor treats the unit as either a memory or an I/O device. The board can be

memory mapped with 16-bit addressing or I/O mapped with 8-bit addressing (onboard jumpers select either memory or I/O mapping. It occupies 4 bytes—the base address plus the next 3 bytes—within the memory or I/O space. The factory-assigned base address is FFFC(hex); other addresses [from FF00(hex) to FFFC(hex) in the memory space and from 0 to FC(hex) in the I/O space] are jumper selectable.

The system CPU communicates with the board via the board's read/write, control/status register, located at the base address, and two read-only data registers, located at the base address plus one and plus two (Fig 2). Triggering an A-D conversion on a specific channel involves writing that channel's address to bits 4 to 0 of the control/status register. These bits are read/write bits; reading them indicates the channel on which a conversion is in progress or the channel on which conversion last took place.

One method of obtaining the converted data involves the host computer's monitoring of the control/status register until the A-D done bit (bit 7—a read-only bit) is set and reading the data from the two data registers. As an alternative, the host CPU need not monitor the control/status register for assertion of the A-D done bit. Instead, the CPU can program the board to furnish an interrupt when conversion is completed. The CPU can select this interrupt operation by asserting bit 6—the interrupt enable bit—of the control/status register. This is a read/write bit that indicates whether an interrupt has been requested.

Interrupts can occur in two modes, as determined by onboard jumpers. In the first mode, the board pulls the STD bus's interrupt request (INTRQ) line low when a conversion ends. To determine which board initiated the interrupt request, the host CPU must read the board's control/status register to see if the A-D done and interrupt enable bits are set.

The second interrupt mode requires a priority interrupt controller (PIC) card. Then, all devices able to generate interrupts must be connected to the PIC, each by two wires external to the STD bus. The PIC monitors all interrupt-generating peripherals and arbitrates interrupt requests based on user-assigned priority levels.

As mentioned, the board accepts 32 single-ended analog inputs and does 10-bit A-D conversion at a 3330-sample/s throughput rate. It supplies a straight binary output code directly proportional to the input. In keeping with the board's cost goals, it contains no onboard digital offset circuitry. Therefore, if connected to a 4- to 20-mA current loop, it never generates the lower fifth of its output-code range.

The analog-input range on each channel is 0 to 5 V. Inputs can swing to ±20 V (with board power on or off) without damaging the board. A selected channel presents a 10-mΩ, 1000-pF input impedence

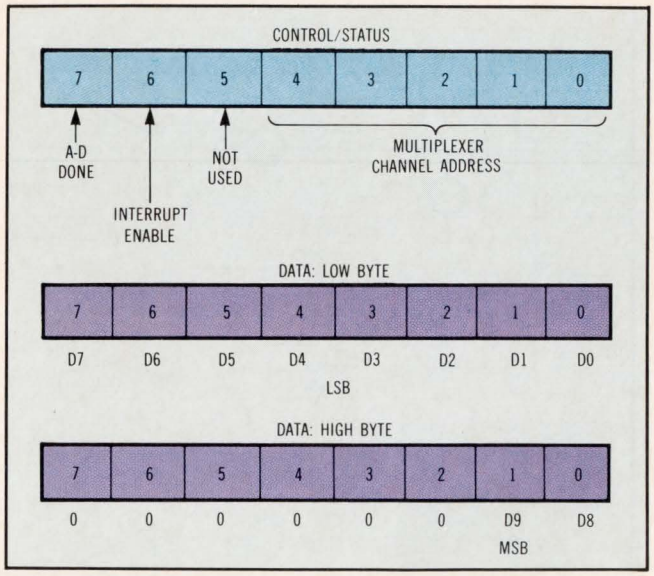


Fig 2 The board appears to a CPU as a read/write, control/status register located at the selected base address. Any write to this address will start an A-D conversion. When the A-D done bit is set in the control/status register, the data can be read from the read-only data registers. At the base +1 address the data low byte is read, followed by the high byte at the base +2 address.

to an input signal, while input impedence on non-selected channels is 100 mΩ, 10 pF. Channel cross-talk is −66 dB at 1 kHz, and channel-to-channel input voltage error specs at ±1 mV. Nonlinearity specs at ±0.5 LSBs, while noise equals 0.2 LSB rms. System accuracy is ±0.12 percent. Gain and zero error are adjustable to zero.

Measuring 4.5 x 6.5 x 0.37 in. (11.43 x 16.51 x 0.94 cm), this board weighs 4.4 oz (124.7 g). It operates from 0 to 70 °C, and its A-D converter is monotonic over that temperature range. Storage temperature specs at −25 to 85 °C. Connections to the board can be made via two 20-pin connectors. These include one pin for each of the 32 analog-input channels (16 channels per each connector). Each connector also includes analog and digital common pins, an amplifier-low pin for remote-ground sensing (over a ±0.1-V range), and a 5-V output pin for use with the screw-terminal board.

Analog input characteristics

The board can be used in three input schemes (Fig 3). Used without the screw-terminal panel, it can accept 32 single-ended inputs (a), or can be used in pseudo-differential input mode (b). In the normal single-ended mode, the board's amplifier-low pin connects to analog common, and any common-mode voltages between sensor common and board common appear as part of the input voltage. These common-mode voltages can thus contribute errors to the converted output.

In contrast, the pseudo-differential input mode allows the amplifier-low (sense) pin to be separated

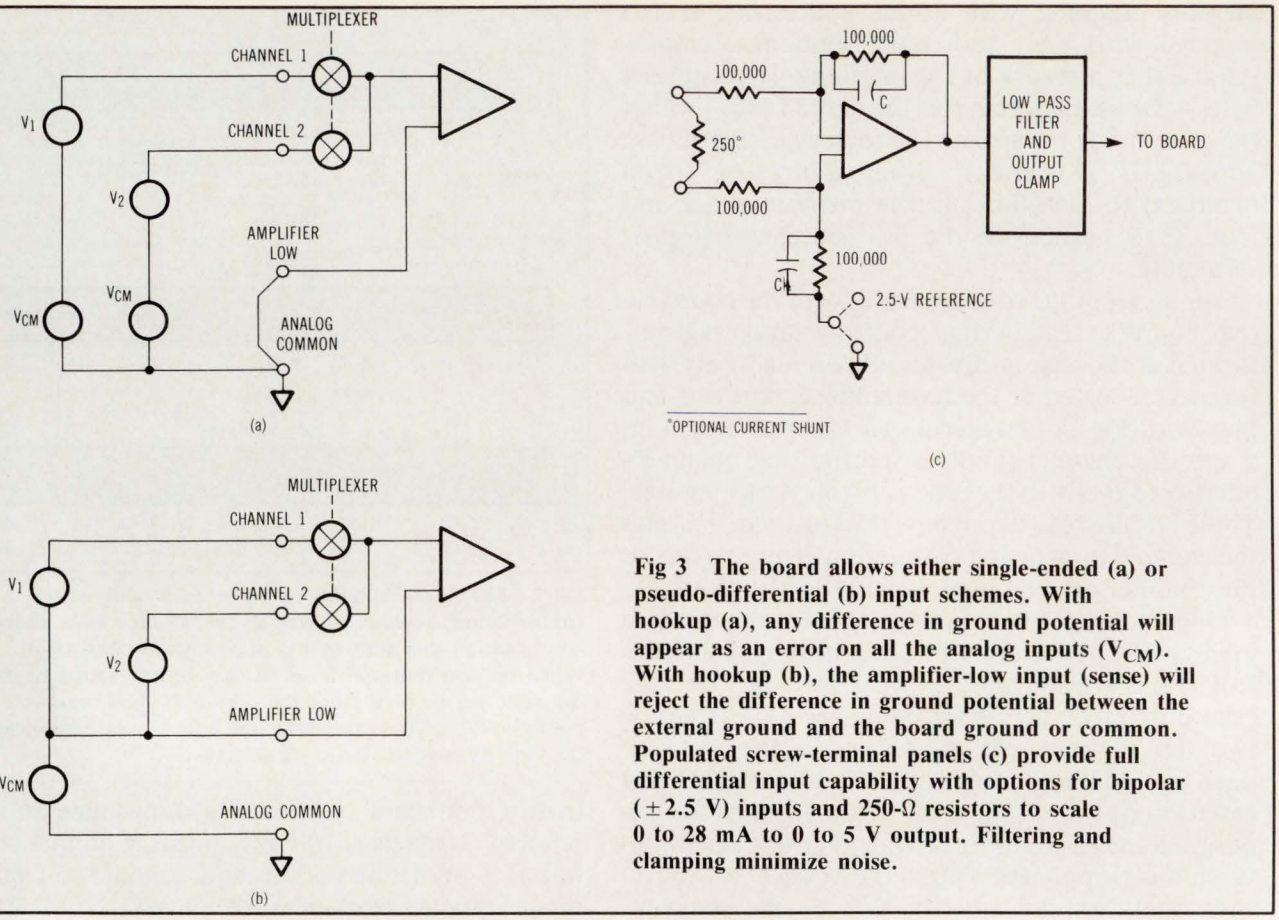


Fig 3 The board allows either single-ended (a) or pseudo-differential (b) input schemes. With hookup (a), any difference in ground potential will appear as an error on all the analog inputs (V_{CM}). With hookup (b), the amplifier-low input (sense) will reject the difference in ground potential between the external ground and the board ground or common. Populated screw-terminal panels (c) provide full differential input capability with options for bipolar (±2.5 V) inputs and 250-Ω resistors to scale 0 to 28 mA to 0 to 5 V output. Filtering and clamping minimize noise.

from the board's analog common and connected directly to sensor common. This allows rejection of the common-mode voltage common to all input signals. The connection minimizes ground problems and acts as a remote ground sense. In either of these modes, the board requires a 0- to 5-V input. The addition of 250-Ω resistors panel converts 0- to 20-mA current signals to this level.

Adding one or two fully populated screw-terminal panels allows yet a third input scheme (c). These versions contain true differential input amplifiers, and each can convert 16 differential input signals to the 0- to 5-V level. Each input channel has a 200 kΩ input impedance. The required ±15 V power supply is derived either from the STD bus (5 V at 250 mA) by version with an onboard dc to dc converter, or from an external ±15 V, 30-mA supply for versions without a dc to dc converter. These versions have an onboard 2.5 V reference source that converts −2.5- to 2.5-V signals to the 0- to 5-V level.

These boards also include 15- or 35-Hz low pass output filters. They achieve better than 60 dB of common-mode rejection at 60 Hz. Moreover, a balanced 20 V peak-to-peak common-mode input voltage at frequencies to 1 MHz typically yields only an LSB of output flicker. This performance stems from the amplifier's common-mode rejection at low frequencies and the low pass filter's normal-mode rejection at higher frequencies.

These populated boards are also available with 250-Ω current shunts to convert 0- to 20-mA current-loop signals to voltage signals. An additional feature is the voltage-clamping function, which protects inputs. If one DT709 amplifier saturates due to an overvoltage input (perhaps resulting from an open 4- to 20-mA current loop, which can result in application of the loop supply voltage—typically 24 V—to the board input), the board's multiplexer is protected, and the board can continue acquiring data on other channels.

Hence, the flexibility and ease with which the board can interface analog sensor outputs with the STD bus make it a suitable data acquisition product for use with STD bus based process-control systems. This board/amplifier combination should prove valuable in industrial markets where price sensitivity and human engineering play important roles.

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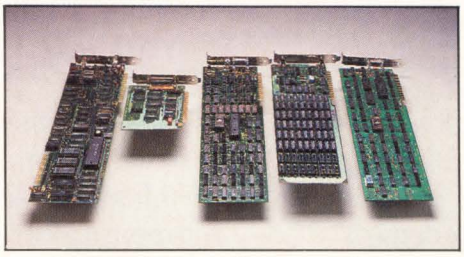

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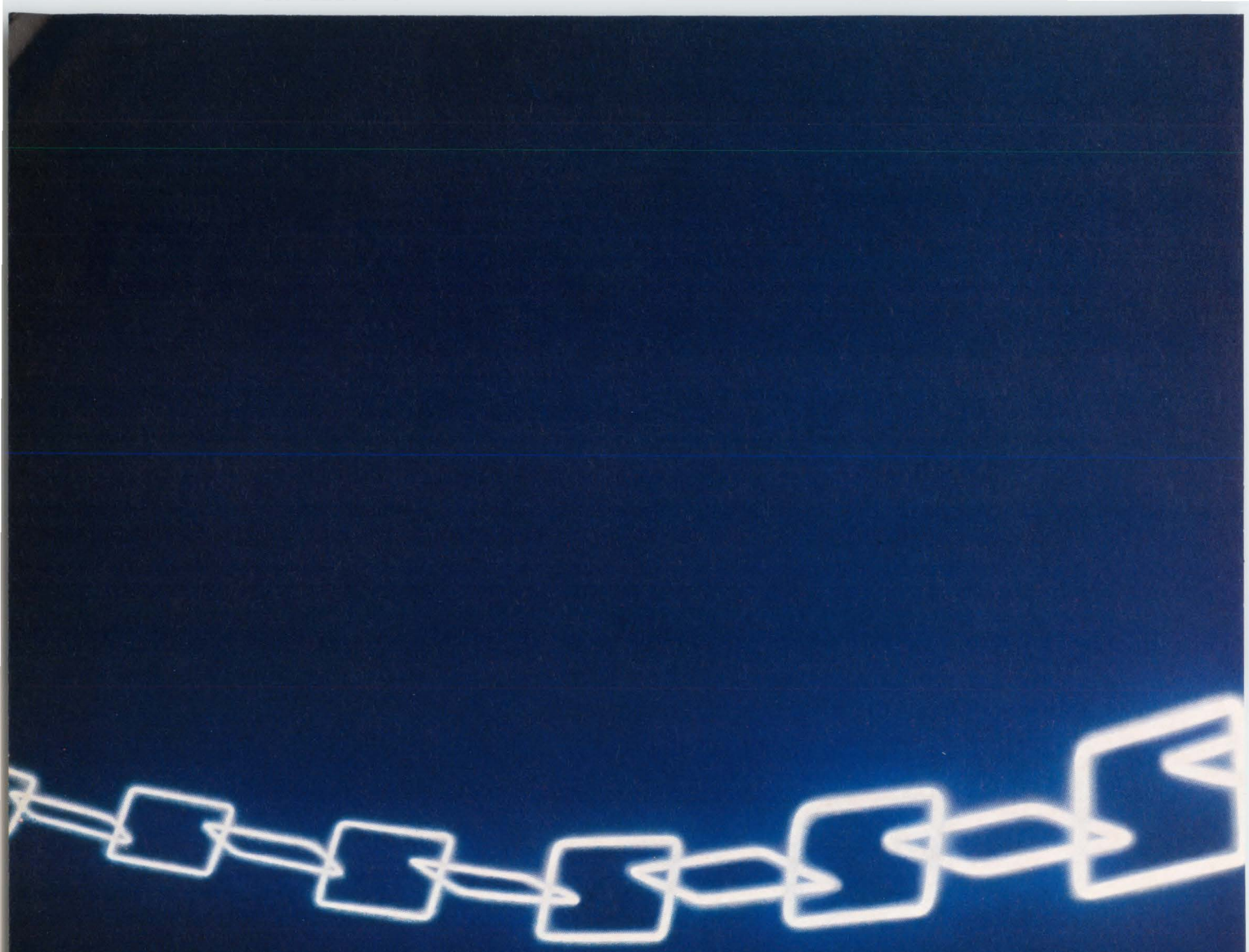
CIRCLE 55



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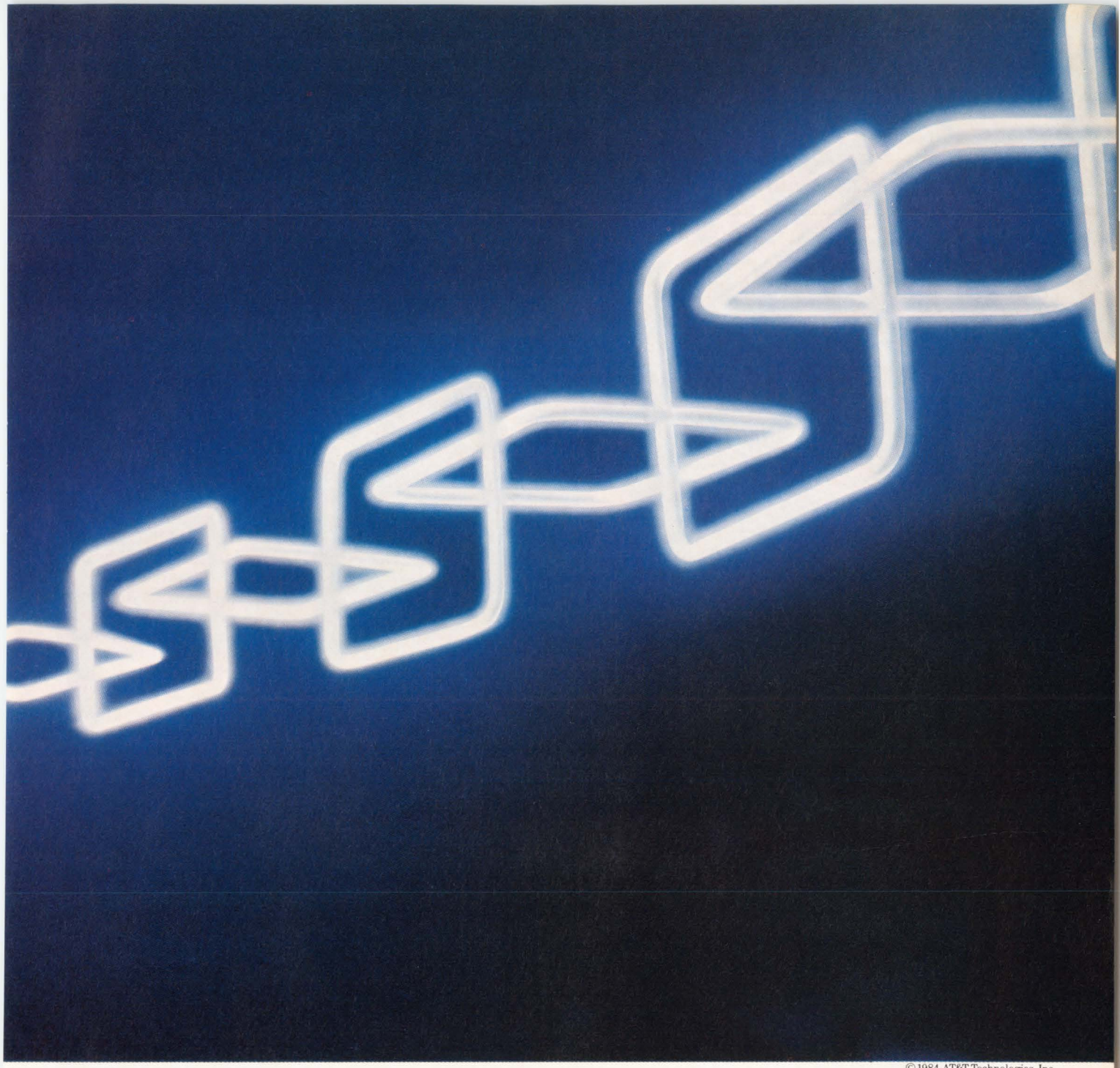

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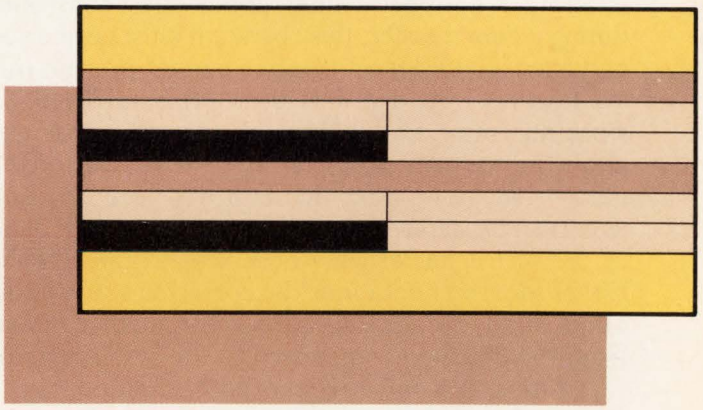
CIRCLE 57

WINCHESTER/FLOPPY CONTROLLER EASES DISK INTERFACING

Chip performs seek overlaps and interleaved data transfers for high performance disk control. Other techniques such as disk caching and elevator sorting are easily supported.

by Mark S. Young



Forming a reliable interface between a serial disk and its parallel computer processing data represents the main problem integrators face. Unique requirements of disk/drive system integration such as disk control, data transfer, data reliability, and error handling demand costly hardware and extensive software support. Also, coupling an asynchronous, serial data channel to a synchronous, parallel computer data channel can prove to be a difficult hardware task. Data buffering, data blocking/deblocking, bus usage, and system interface timing require extra system logic. Finally, making the disk conform to the operating system's data handling needs requires development of additional software.

Creating disk directories, addressing disk memory, optimizing disk access, and using the controller disk I/O commands all combine to make interfacing difficult. One chip set that addresses these concerns is the Am9580 hard disk controller (a Winchester/floppy controller) and the Am9581 disk data separator. The set is ST506/412 compatible, but it can be made to conform to Enhanced Small Disk Interface or Small Computer System Interface by adding several other chips.

One of the disk controller's primary tasks is coupling the serial disk bus from the parallel system bus. Even though such peripherals as modems and printers allow the user to stop a transfer after each character by using a ready/not ready signal line, halting a disk is not as easy. The nature of disks prevents such a data transfer interface; once it starts transmitting data from a sector, the operation must either finish or abort. Because data transfer cannot be stopped, the controller and the system must deal with complex data buffering and transfer over the system bus.

A typical Winchester drive sends data serially at 5 Mbits/s. If the data is moved directly to the system bus in 16-bit blocks, the disk controller must hold the bus for more than 800 μs to complete a 512-byte transfer. Because data leaves the disk at a relatively

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slow speed (but not so slow that the bus can be shared among different masters), the disk controller can easily become a system bottleneck. This is especially true in multi-user or multitasking environments.

Several different data buffering methods are commonly used to prevent this bottleneck. The first in, first out (FIFO) buffer provides a simple, and generally effective, method of buffering disk data in low performance systems that use floppy disk drives. In the higher data speed environments of Winchester drives, however, a FIFO does not provide sufficient bus buffering. Moreover, the FIFO does not free the bus from the problem of long accesses by the disk controller—it only decouples the disk from the CPU bus timings. If the FIFO is not sufficiently deep (256 bytes or more), the bus buffering only provides longer lag between the time disk transfer begins and the time it takes to obtains access to the bus through arbitration. In the mean time, the controller still needs to use the bus for long periods.

Buffer dilemmas

A FIFO buffer may also encounter data underflow and overflow. These problems are especially prevalent in systems with high bus loading or with multiple bus masters that require frequent servicing. Usually, if another peripheral interrupts a disk controller during a data transfer, this operation must be aborted and tried again. FIFO buffering cannot prevent this event, unless the depth of the FIFO is sufficient to store an entire sector. Finally, the FIFO does not allow the controller to determine the validity of the data—that is, whether the data has been certified as correct by the error detection circuitry—until most of the sector has already been sent to the system. Either incorrect data must be corrected using additional bus cycles, or the entire sector must be reread from the disk and transferred to the system again.

A full sector buffer is another technique that is commonly used in Winchester controller designs. The single sector buffer normally uses a single static RAM chip. The size of the buffer is limited only by the SRAM devices available. With 2-Kbit x 8 SRAMs widely available today, and the newer 8-Kbit x 8 SRAMs starting to appear, just about any size buffer can be easily built. Multiplexing the address, data, and control lines between the controller and the system requires a minimum of extra hardware with this buffer.

The full sector buffer approach avoids many of the problems associated with the FIFO approach. Overflow and underflow are no longer a problem, and data integrity is ensured, because the entire sector is stored in the buffer before it is sent out to the system. However, the single sector buffer cannot perform zero interleaved data transfers between the system and the disk controller—data cannot be loaded into the buffer until the previous sector has been fully emptied. As a result, single buffer disk I/O can be at least 25 percent slower than zero interleaved sector operations, depending on how much interleaving is required.

The dual sector buffer approach used on the hard disk controller has the advantages of single sector buffering, while it greatly increases disk I/O throughput. These integrated dual sector buffers allow the user to select data sector sizes of 128, 256, or 512 bytes. The dual sector buffer system employed by the hard disk controller always has one buffer available to the system and the other buffer available to the disk [Fig 1(a)].

When both the system and the disk are finished using their respective sector buffers, the buffers are switched (or toggled) so that the former disk buffer is now available to the system and the former system buffer is available to the disk [Fig 1(b)]. This buffer toggling method allows the hard disk controller to transfer data continuously from the disk without any sector interleaving, even at disk speeds of 20 Mbits/s. Besides allowing complete decoupling of the disk and the system bus from each other, the dual sector method maximizes data throughput as it minimizes system bus use. Because each data sector on the disk is stored entirely within the hard disk controller, the

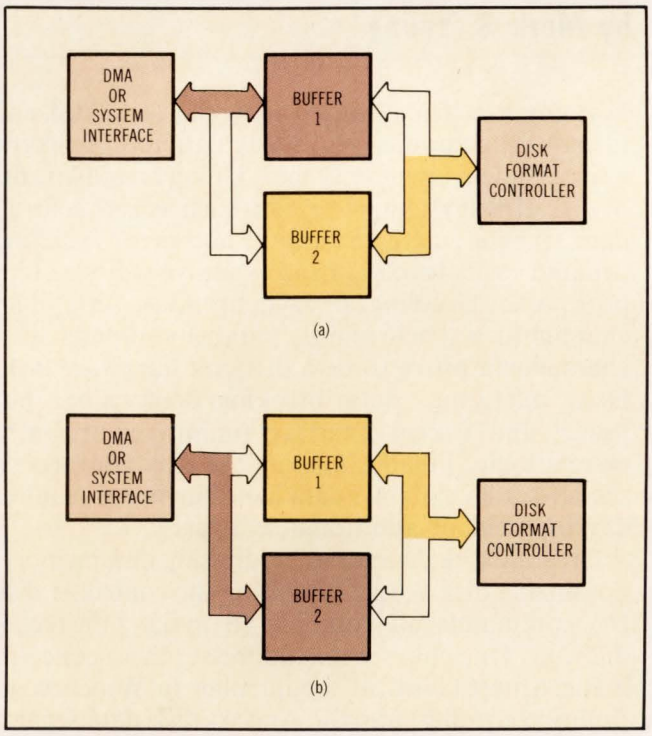

Fig 1 The dual sector buffer approach illustrates how data can be transferred between the disk and the system simultaneously. Buffer No. 1 is allocated to the system/DMA while the other buffer is used by the disk formatter (a). When the system and formatter are finished, the buffers are switched (b). In this manner, the system empties one buffer while the disk formatter fills the other (or vice versa), thus continuously moving data to and from the disk.

system bus is not tied up continuously during the physical transfer of the data to and from the disk.

The controller's bus use can be limited to short, fast data transfers without the danger of data underflow or overflow. In addition, the controller can be interrupted by more important activities for much longer periods than allowed by FIFOs, without sacrificing any disk data transfers. And because the sector is fully loaded onto the controller and checked for errors before it is transferred to system memory, the data need only be sent once. Erroneous data is never transferred out of the controller unless the system specifically requests the controller to do so. Full sector buffers allow the Winchester/floppy controller chip to gather from diverse memory locations on-the-fly, instead of assembling contiguous data blocks before the transfer occurs.

To adjust overall bus performance, the system can alter burst and dwell values on the hard disk controller.

All disk controllers, especially Winchester controllers, must perform data transfers efficiently between the disk and system memory. Usually, this requires that a DMA device or DMA channel be dedicated to the disk controller. From a design viewpoint, a compromise is made when an external DMA controller operates with a disk controller. This is because an external DMA controller is usually slower than a custom, integrated DMA unit.

In order to make the DMA control handshake work properly, the DMA must receive high priority in the system bus hierarchy. At the same time, the interface must be generalized to handle the different DMA devices. Extra software is also required by the system to set up the DMA controller for each disk transfer. From a controller design point of view, interfacing to an external DMA unit requires a tradeoff in disk controller performance. If the controller has to handle commands, status, and data without constant system intervention, at least three DMA channels have to be dedicated to the disk controller.

The fully integrated DMA controller on the hard disk controller eliminates all external system hardware support functions. Thus, system interface requirements are reduced to bus drivers, bus receivers, and a disk driver software routine. The Winchester/floppy controller chip's DMA controller can handle an 8- or 16-bit data bus and up to 32 bits of addressing. The hard disk controller's DMA unit can transfer data at up to 5 Mbytes/s.

An extra strap option allows the system interface to support either synchronous or asynchronous memory transfers. The user can also extend the basic four-clock transfer cycle with either the READY line or with programmable wait-state insertion. A failsafe measure ensures that a faulty memory board will not cause the hard disk controller to stall the system bus. A time-out counter releases the system bus, thus ensuring that the hard disk controller aborts any memory transaction taking longer than 5 ms.

The Winchester/floppy controller's DMA bus activity can be determined by setting the burst and dwell characteristics in one of its control registers. The burst characteristics indicate how many bytes of data are transferred every time the DMA unit uses the system bus. This number can be programmed from 1 byte to as many bytes as are required in a single transfer request of the hard disk controller. The dwell characteristics determine the amount of time the DMA unit stays off the system bus between bursts. During a multibyte DMA transfer, the DMA unit will release the bus. This occurs only after the number of bytes indicated by the burst count have been transferred. After waiting the amount of time specified in the dwell count, the hard disk controller will request the bus to continue the DMA transfer, as necessary.

To adjust the overall system bus performance, the system can alter burst and dwell values on the hard disk controller. These burst and dwell characteristics allow other peripherals in the system to use the bus and to prevent "lockout" of lower priority peripherals. Because the DMA unit can transfer data to and from the buffers much faster than the disk can, the onboard sector buffers give the system plenty of time to move data in and out of the controller. The buffer will maintain maximum disk throughput, even with the use of burst and dwell.

Controlling the bus

In the event of a system emergency, the DMA unit can be forced to abort the current DMA transfer. A two-wire handshake scheme is used on the Winchester/floppy controller chip interface to gain control of the system bus. The hard disk controller asserts the bus request line and waits for the bus acknowledge (bus grant line) to be asserted by the system arbiter. When the DMA unit is finished transferring data on the bus, it de-asserts the bus request line. This indicates to the arbiter that the bus is now free. If the system needs to force the hard disk controller off the system bus, all it has to do is de-assert the bus acknowledge line. The hard disk controller will cleanly finish the current word or byte transfer, and then get off the bus. This is called preemption. Even in an emergency, none of the data transfers to or from the hard disk controller are affected. The hard disk controller will continue to request the bus as it would normally and attempt to finish the interrupted transfer as though nothing unusual happened.

The system has access to seven 16-bit control/status registers, as well as to an onboard DMA unit.

These registers allow the system to keep track of the hard disk controller while the chip is operating. The command/status register allows the system to start, stop, or resume a command chain operation. A software "reset" is also provided. Its function is equivalent to that of the hardware reset pin. Software reset allows users to reset the chip without actually using the reset pin, which can be tied to the system reset line. This causes the chip to immediately abort the current command operation.

The system has access to seven 16-bit control/status registers, as well as to an onboard DMA unit.

The stop chain command forces the hard disk controller to abort the current chain at the end of the current command. The resume command allows the hard disk controller to pick up where the interrupted command left off without restarting the command. This is possible when a noncatastrophic error is the cause of the interruption. The upper byte in the register contains the current chip status—information about certain types of errors are reported in this field whenever the hard disk controller halts.

The mode register determines bus activity by using the burst or dwell fields. In addition, a programmable interrupt option allows users to enable or disable interrupts from the hard disk controller. The number of wait states inserted into each memory transfer (0, 1, 2, or 3) can be specified to allow the hard disk controller to accommodate slow memories and the memory transfer acknowledge line. A register lock bit freezes the register set. This allows the system to monitor all the registers while the hard disk controller is running, without the danger of having them altered during a read access. Finally, the disk control interface is specified in this register by the seek mode field. It determines whether implied and overlapped seeks, implied seeks only, no seek operations but disk status (restricted), or no seeks or disk status (buffer mode) will be performed by the hard disk controller.

The next block pointer always points to the current command being executed in the command list. The status result pointer always points to the next status block to be written. The status result length specifies how much memory is allocated for status results information. The next block pointer is initialized before each go command; it points to the beginning of the command chain. Then, the hard disk controller automatically fetches commands and reports their status to the area specified by the status result pointer and status result length registers. The status result pointer and status result length registers only need to be updated when they overflow. By monitoring these registers, the system can determine what the hard disk controller is doing while this chip is executing a command list. The next block pointer and status result pointer are both 32-bit pointers, accessed as two 16-bit registers.

Among the most poorly implemented features on many disk controllers are the command set, status information, and the mechanism for transferring these between the system and the controller. The small, primitive disk I/O commands in many controllers force the system to build up more powerful macro commands just to facilitate the writing of the disk driver software routines.

A typical controller might have read, write, and verify sector commands. It would also have a seek, a load/dump buffer, a format track command, read error correction code syndromes, and read ID. These primitive commands usually require a separate seek command before any track can be accessed. They also require the system to monitor the position of the read/write heads. In many controllers, the drive parameters must be loaded every time the drive is accessed, or the flexibility of the user is limited by fixed drive control parameters. Additionally, the system must continuously feed all commands to the controller, keep track of errors, and control the data transfers to and from the disk.

An indirect software cost associated with a simple disk controller design might result from interfacing a typical Winchester with a personal computer. This would require a complex software I/O driver to

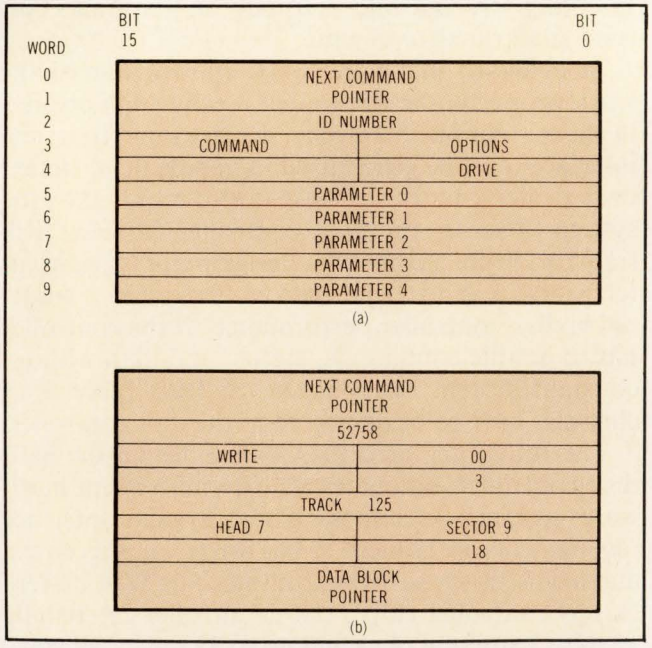

Fig 2 The I/O parameter block (IOPB) command structure is a 10-word block containing all the data needed to allow the hard disk controller to move data to and from the disk (a). The write command will transfer 18 sectors from a contiguous block of system memory indicated by the data block pointer (b). The read/write heads will be moved to track 125, head 7, and start in sector 9.

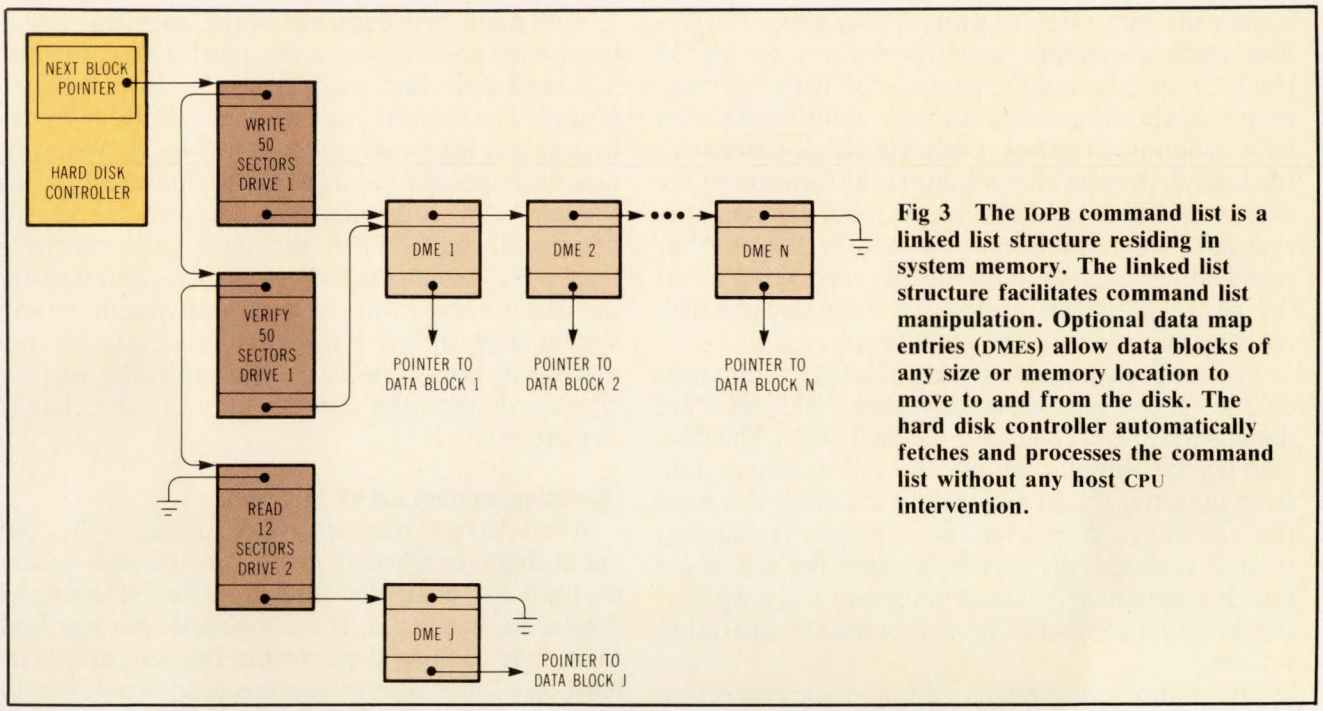

Fig 3 The IOPB command list is a linked list structure residing in system memory. The linked list structure facilitates command list manipulation. Optional data map entries (DMEs) allow data blocks of any size or memory location to move to and from the disk. The hard disk controller automatically fetches and processes the command list without any host CPU intervention.

perform simple disk read and write operations. For example, when an operating system requests 10 disk sectors, the CPU must issue a seek command and 10 groups of alternating read sector and dump buffer commands. Besides issuing these 21 commands to the controller, the external DMA controller must be set up for the data transfer. At the same time, the CPU becomes responsible for monitoring the controller's progress after each of these commands has been completed. The hard disk controller, on the other hand, could complete such an operation in a single command and alert the system via interrupts if any problems requiring intervention of the operating system arose.

The basic command structure of the hard disk controller is the I/O parameter block (IOPB), shown in Fig 2. All disk-specific parameters are obtained from the individual drive parameter RAMs that are stored on the hard disk controller. Only parameters for executing the command are required. The first two words of the IOPB contain the 32-bit pointer to the next IOPB in the command chain; the IOPB equals 0 when it is the last command in the chain. Finally, a 16-bit ID value is provided to help the system identify errors.

When the hard disk controller issues status result block commands, the ID field of the IOPB is put into the status result block to indicate which IOPB caused the error or had a problem. The command byte says what command the IOPB gave. The operating system has 16 different IOPB commands. The options byte allows users to specify both command-independent and special command-dependent control options. The command-independent options allow users to stop on any status result block, on fatal errors only, or at the end of each IOPB. The command-dependent options include track verify after a seek, data map control enable, user-defined data marks, error location information, and location of specific disk ID fields.

Up to six 16-bit parameters are provided with each IOPB. Typically, the drive's starting track number, starting head number, starting sector number, and the number of sectors to be transferred are required in each command. In addition, options such as user-defined data marks, format patterns to be used, and relocated track information are needed. A 32-bit data pointer is also needed to specify the beginning of the data to be transferred, or to point to the data map indicating how the data is transferred.

Each of the controller's primary commands—read sector, write sector, and verify sector—can handle from 1 to 256 sectors. Specific user-programmable bytes in the drive parameter RAMs indicate how the controller will respond to multihead and multitrack overflows. All commands on the hard disk controller automatically seek the track specified in the parameters and perform any multiple track seeks the command requires. A separate seek command is not required for any disk I/O command. Each command also has a pointer or pointers to the data needed for write or verify operations, including pointer or pointers to memory space in the case of read operations. This allows the hard disk controller to perform all buffer read and write operations automatically between the controller and system memory without using separate load and dump buffer commands.

Other commands such as load disk parameters, restore drive, and format track allow the user to

initiate the controller for normal operation. The format track command specifies from 1 to 65,535 tracks. It also formats the entire disk with one command, again using the mutlitrack, multihead policy byte to handle overflow. Once the disk is initialized, the hard disk controller monitors the location of the current read/write heads' tracks, thus relieving the system of the responsibility. Moreover, a seek command allows users to move the disk read/write heads to any track. This is useful, for example, if a disk is to be accesssed in the near future.

The read data absolute and read ID commands enable recovery of data from disk fields that are damaged by head crashes or media defects. The relocate track command allows the user to move data from defective tracks and re-map the new track onto the old track. Whenever the damaged (relocated) track is accessed, the hard disk controller will detect this. It automatically moves to the new track without stopping the command or burdening the operating system.

The dump sector buffer, dump error correction code syndromes, and correct buffer commands allow the system to examine disk data error before correction. If necessary, the hard disk controller can perform error correction automatically, without system intervention. The load sector buffer, load error correction code syndromes, and dump drive parameter commands, in conjunction with the other load and dump command, allow onchip diagnostics of the Winchester/floppy controller chip's degree of function.

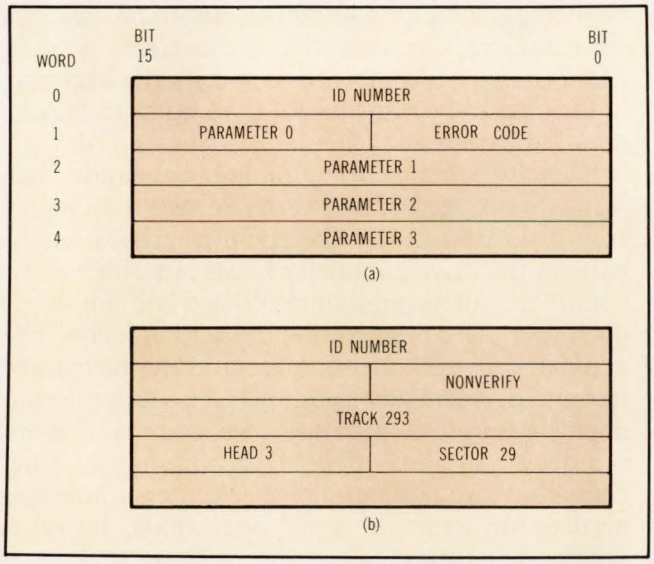

Fig 4 The status result block reports complicated disk I/O errors to the system. Each five word status result block has an ID value and up to four parameters (a). A typical status result block illustrates the type of status information given to the CPU (b). In this case, the data specified by a verify command was not the same as data found on the disk's track 293, head 3, and sector 29. The drive number is specified in the IOPB with the appropriate ID number.

With many disk controllers, the operating system must issue commands to the hard disk controller. The hard disk controller fetches its own command instead. The operating system arranges the command in a linked list command chain (Fig 3). When the next block pointer points to the beginning of the list, the hard disk controller is ordered to execute the command chain. Then the hard disk controller fetches the commands, processes them, and transfers the data to and from the disk and system without system intervention. Using the link pointer in command will cause the hard disk controller to fetch commands until the last command in the chain is executed.

Operating system stays informed

When the hard disk controller completes the command chain, or when an error/control fault occurs, the hard disk controller interrupts the system to tell it what has happened. If a correctable error or fault caused the command execution, the system tells the hard disk controller to resume processing, but instructs it not to restart the command. Other options allow the hard disk controller to interrupt the operating system whenever data is transferred and is therefore available.

The linked list command structure eases the implementation of the overlapped seek routine. A special software routine handles the command chain in the hard disk controller chip. When the operating system enables this routine, the hard disk controller follows the command chain via the linked pointers, and looks for commands ahead of the command being executed. Whenever it finds a command involving an inactive drive, it calculates the necessary seek information. It then issues the seek command to this drive, well before the command is actually executed. And when a previously busy drive finishes its current command, the hard disk controller starts to look farther down the chain for a command that involves some seeking for that drive. In this manner, time-consuming head positioning is executed in parallel, providing a dramatic improvement in disk I/O performance.

In addition to fetching and processing its own commands, the hard disk controller issues status result blocks to indicate when certain events occurred while disk data was being processed. The status result block is a five-word unit (Fig 4). Each block contains a 16-bit ID number to say which IOPB issued the status result block, an error code to explain the error, and up to 7 bytes of parameters to indicate other error-specific information. For memory efficiency, status result blocks, unlike IOPBs, are stored in consecutive order in the status result area specified by the status result length register.

By examining the status result area after a command chain has been executed (or halted because of

Introducing the VP-10 Graphic Element Processor

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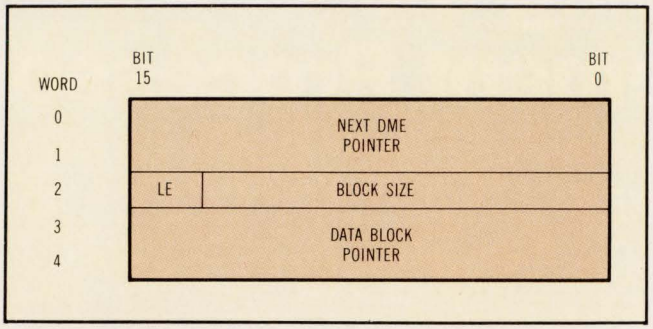

Fig 5 The DME uses a linked list structure similar to the IOPB command list. Each DME can handle up to 32,768 bytes. The load enable (LE) bit determines whether the data specified by the DME will be skipped. This option specifies what data in each sector will be downloaded, thus avoiding unnecessary data transfer on the system bus.

errors), the system can determine what has happened on the disk. When the status result area becomes full or overflows during a normal hard disk controller operation, the hard disk controller ceases operation and alerts the system. Then, the system can either increase the area allocated for status reporting or analyze the status and reset the status result pointer and status result length to the beginning of the status area. It performs one of these functions before telling the hard disk controller to resume operation.

Optional stops

Status reporting is an important function of a peripheral that controls the system's primary mass storage device. Many errors can occur in a typical disk subsystem during normal processing; each affects the system, controller, or disk to a different extent. For example, upon detecting an incorrect seek operation, the hard disk controller will automatically attempt a re-seek operation. If the second attempt is successful, the hard disk controller issues a nonfatal status result block to alert the system of the disk error. If the reseek attempt fails, however, the hard disk controller automatically issues a status result clock and ceases operations. The system should have the option of specifying whether or not the controller will stop on any error (fatal or not) or only on the fatal errors.

It may be unwise to abort a disk operation even for a fatal error in some cases. Consider a zero interleaved multisector read operation. In the process of transferring the disk data to the system, a flaw might be noticed by the error detection unit. Because few error correction codes can correct the error and physically continue reading the sectors in sequence, a typical controller would abort the read operation and immediately initiate data recovery operations. However, since data errors are relatively rare in most drives, it would be wiser for the controller to indicate the sector that is damaged, prevent the error from being transferred to the system, and continue reading the remaining sectors. Once the last of the data has been transferred, the system has the controller recover sectors that had problems. In this scenario, the controller avoids wasting time caused by stopping and starting the read procedure or resulting from introduction of extra rotational latencies into the disk I/O operation.

The status result system in the hard disk controller handles errors in many different ways. Users are given maximum flexibility in deciding what errors are to be aborted automatically and which errors are merely informational. Users of most small personal computers probably do not want to halt the controller every time an error is detected—especially if the controller can be programmed to perform retry operations automatically and to use the onboard error correction codes. These users are only interested in being alerted when the data cannot be recovered automatically. Users of minicomputer systems might want to examine the status result information for system maintenance logging. Users of such error-sensitive systems as fault-tolerant computers have a greater investment in detecting errors, no matter how minor. The hard disk controller allows these users to tailor the status system to support their applications.

Data in a computer system's memory is represented by groupings of bytes or words of various sizes that, on a disk, are divided into groups of bytes called sectors. Although sector sizes vary from disk to disk, and sometimes from track to track, they are always the same size on a given track. Sectors on a disk usually come in 128, 256, or 512 bytes; less frequently in 1024, 2048, or 4096 bytes. Unfortunately, computer data and disk data rarely agree on sizes. The controller must usually divide all system data into blocks equal to the sector size on the disk. The reverse operation is required when data is read off the disk.

The embedded control algorithms in the Winchester/floppy controller chip allow this common data preprocessing task to be offloaded onto the controller. The hard disk can automatically fit data into sector blocks for writes and into continuous data for read operations. It can also perform data blocking and deblocking for any other size of data.

The hard disk controller allows the user to specify an optional data map whenever disk data is transferred between the disk and system memory. With this data map, users can fetch data from the system memory in any size block (1 to 32 Kbytes/block) and pack the data into the required number of sectors. Conversely, when data is being read from the disk, the data mapping option allows users to deblock the data into any size block and store it in widely dispersed, noncontiguous memory locations. Users also have the option of reading only certain fields from each sector and transferring only that data into the

system. Thus, bus bandwidth is saved from unnecessary data transfers.

Data in system memory is not always arranged in continuous blocks that are easily moved, as units, to the controller and onto the disk, however. Increasingly, users are creating complex data structures in Pascal, C, and Ada to store data in a form that can be easily manipulated. It is very inefficient to store data in blocks of memory that encompass the data structures themselves. It is also wasteful to have the CPU gather the data and transfer it to a temporary buffer for the disk controller. The same applies when the data needs to be read back into the system. Having the CPU perform the data packing and unpacking requires extra system memory for buffers and increased system overhead because all data needs to be transferred twice in system memory to be read from, or written to, the disk.

The data map structure used by the hard disk controller is a block of five 16-bit words (Fig 5). It consists of a 32-bit pointer to the next data map block, a byte count word with a load flag, and a 32-bit pointer to the actual system memory location where data is to be read or written. Data map blocks can be strung together just like IOPBs to create a data map as large as needed for the data blocking/deblocking task. Because the DMA unit is much better at handling data transfers than the CPU, the data map is considerably more efficient than having the system perform the task.

As disk controller peripherals become more sophisticated, the system interface must also progress. Although it is impractical to provide users with every permutation in hardware and software, the hard disk controller design allows for a large degree of flexibility and programmability. At the same time, the disk controller should not overwhelm the system with a design so flexible that it is unusable. System integrators need a controller that can be easily integrated into today's standards and upgraded to future requirements without complete redesigns or compromises in performance.

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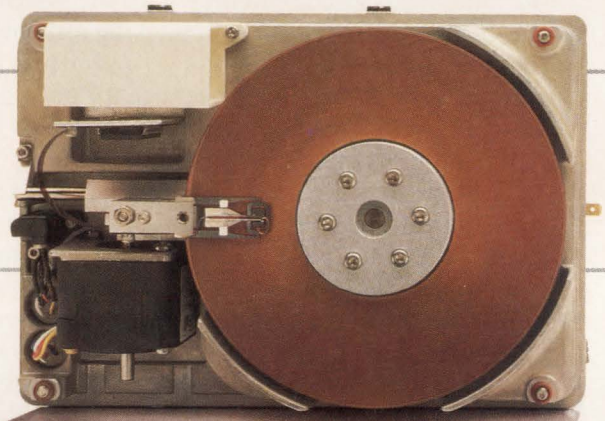
There Are Only Two Things New Tested Pairs

The Testing.



OEMs face major problems trying to decide which hard disk drives to build into their microcomputer systems. What with the wide range of drives, and so many hidden costs associated with evaluation, testing and integration, the process becomes a time-consuming and costly hassle.

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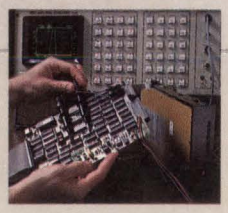

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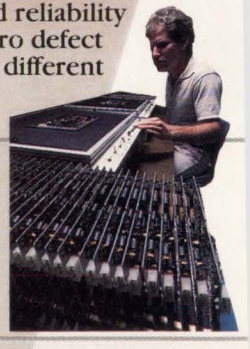

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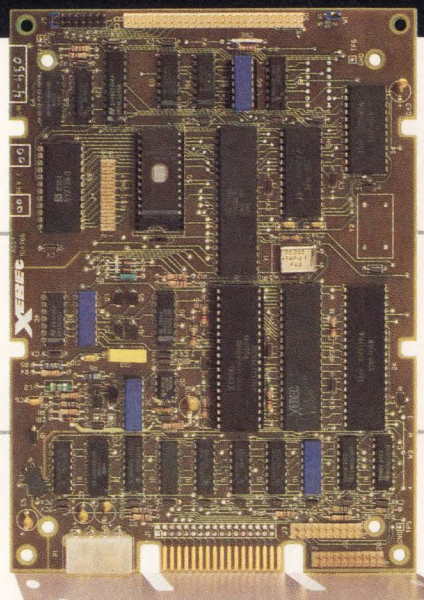

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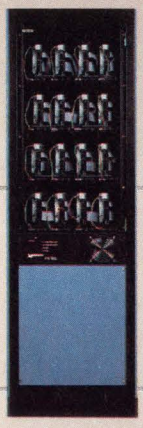

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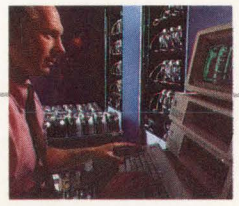

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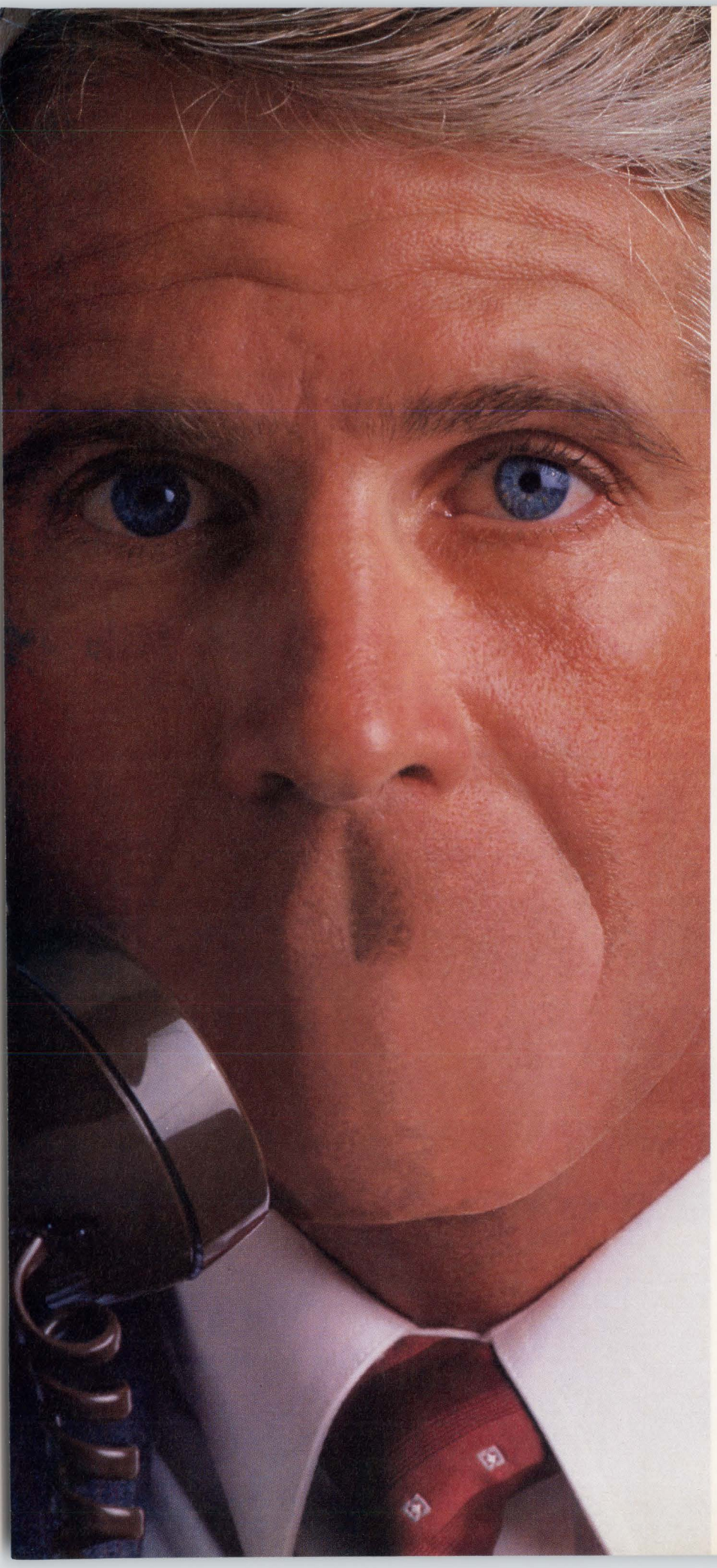

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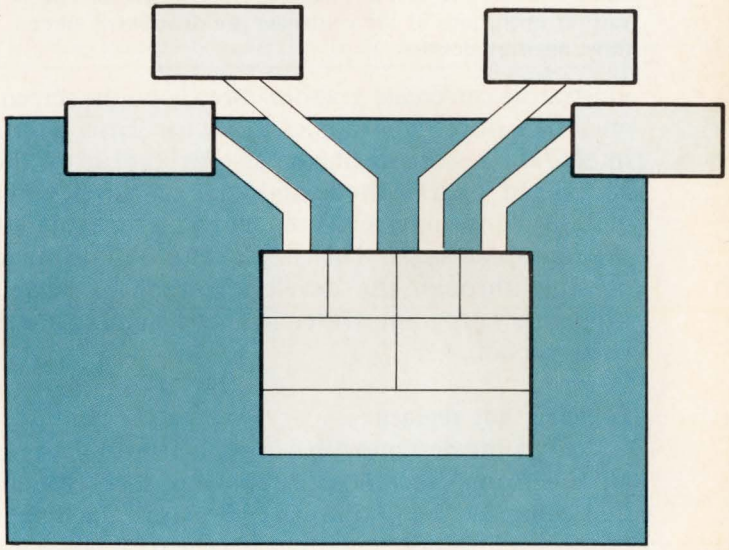
MULTIPLE MICROS DISTRIBUTE TEXT AND GRAPHICS FUNCTIONS

An integrated system distributes design and editing work load of technical publishing across multiple microprocessors. This architecture automates document production by enhancing traditional methods.



by Robert S. M. Wulff

Computerized technical publishing presents special problems for system designers because there are many kinds of users with different needs—authors, editors, layout artists, illustrators, drafters, and production managers. Editors, for example, must be able to see the interrelationship of art and text, and illustrators and artists must be able to easily create and modify art. A graphics text system to satisfy the needs of these users requires an easy-to-use interface that is "transparent" to the complex operations being performed. This interface must also have the same "feel" as manual methods of illustration, page layout, and typography.

One way to accomplish this is to use a multiprocessor architecture that combines an interactive graphics processor to support the user interface; a special purpose graphics processor to handle realtime zooming, scanning, and scrolling; and text and graphics that are integrated into the same data base. In a single integrated system developed by Qubix, the graphics editing and manipulation capabilities of a computer aided design (CAD) system are combined with word processing functions, text editing, pagination, and composition. With a large landscape display incorporating 2240 x 1680 viewable elements, the system can generate type fonts in a wide range of styles and sizes. To drive the display, the company has designed a proprietary video board that operates much like a stored logic computer.

Graphics and text are combined into a single data base that lets the user view and interactively edit pages containing both text and art on a screen prior to output. Input can be accepted directly from word processors or personal computers (text) and CAD systems (art), as well as from any workstation, keyboard, and/or graphics generator. In addition,

Robert S. M. Wulff is vice president of research and development at Qubix Graphics Systems, 1255 Parkmoor Ave, San Jose, CA 95126, where he is responsible for the graphics capabilities of the Qubix system. He holds a BS in mathematics from California State University, Fresno.

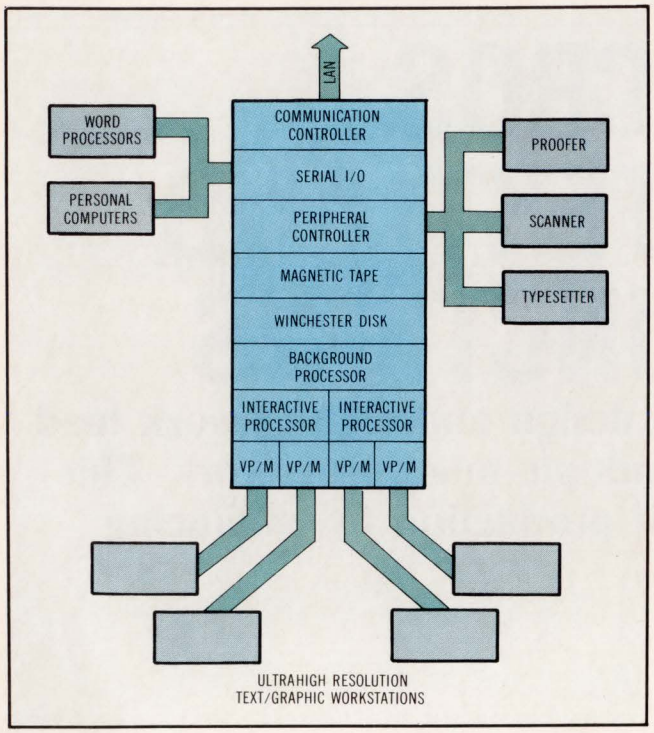


Fig 1 The system consists of four graphics workstations and up to 320 Mbytes of Winchester mass storage. The various operations of the controller are distributed among three microprocessors.

illustrators can create graphics directly on the screen, and then store the graphics in vector form. Fonts in actual sizes are displayed as they appear on the completed page, edited, and sent to a typesetter without any intermediate manual makeup or photographic steps. This single data base is made possible through the development of a special, proprietary program written in C and running under Unix version 4.2.

Enhance, not replace

One of the designers' basic goals was to develop an Electronic Technical Publishing (ETP) system that enhanced the traditional methods of document production, rather than replacing them. While present computer aided publishing (CAP) systems have increased the efficiency and productivity of the publishing process, they have eliminated a powerful spatial and visual problem-solving methodology, replacing it with a more limited linear thinking style. This new style is similar to the way programmers think and work. However, editors must be able to see the interrelationship of art and text in real time on the screen. Illustrators and artists must be able to create new art easily, as well as to edit and to modify old art quickly and easily. For this, an easy-to-use graphics text interface similar in "feel" to manual methods of illustration, page layout, and typography is needed.

The results of actions taken by the editor/designer/illustrator in the production of a document must be immediately perceptible. Yet, this is one aspect of document production that current approaches to CAP have done little to resolve. Final decisions as to type size, layout, the relationship between art and text on a page, and the style of a document can only be made when an actual document is produced, in either page, spread, or complete form.

The operator must have interactive realtime feedback, even for a small change such as correcting a single mistake in one illustration in a large document. While implementing global changes, eg, reorganization of the outline of the document, the results of those changes should be immediately seen on the screen, in the actual fonts and type sizes of the final document. Users interact with the system in a direct, visual manner by pointing at objects as they are displayed on the screen. The user tells the system what to do by touching and selecting first the object to be acted upon, and then touching a menu button representing the action to be performed.

This straightforward "object/action verb" grammar is consistent across the entire system, independent of the application being run. For example, the user activates all editing functions in an identical manner, regardless of the environment. First, the object—a word, a sentence, an illustration, an entire document, a page layout—is selected. Then the verb performs the actual change. While the process by which underlying programs actually accomplish their internal editing functions varies from view to view, the method by which the user initiates the edit operation is identical.

The actions to be performed within a particular view (the verbs) are selected from a menu in the command pane. Because of the object/verb structure of the command language, all operations (editing of text, graphics, layout) are initiated by a concise command set found in a command pane menu. The user is never locked out or "mode bound." As users select an object, the system ensures that the correct menu is displayed. For example, all text objects are manipulated using the same familiar text edit menu, regardless of surrounding context or task. A strength of this visual/gestural grammar is that users do not generally need to spend their time typing. None of the manipulation involved in page layout, selection of correct type face and size, or creation and revision of illustrations requires any use of the system keyboard.

The system is built around a distributed function architecture consisting of multiple MC68010 microprocessors. These share up to 8 Mbytes of internal RAM, and are linked by an internal Ethernet-based bus. A single full function cluster (Fig 1) can have up to four graphics workstations and up to 320 Mbytes of Winchester mass storage. An unlimited number of nodes can be linked using an external Ethernet local area network interface.

Each cluster has a multitasking controller comprised of three MC68010s and attendant memory, and interface circuitry. Various controller operations are distributed among the CPUs. Central to the design is the interactive processor, which handles all functions relating to graphics processing, drives the screens, and, most importantly, coordinates all of the activities of the multiple-view user interface.

In raster scan systems, the graphics processor's function is to furnish information in bit-mapped form.

The background processor functions as a file server for the 80- to 320-Mbyte Winchester disk drive, coordinating all batch operations and various system data management functions. A third CPU handles all demand publishing functions. All disk management functions are under the control of a single MC68010 with 2 Mbytes of internal RAM. It also controls the system's archival tape backup (nine-track, 1600 byte/in. standard and streaming tape).This processor's basic function is to act as the system file server and task manager.

Distributed function multiprocessor architecture

Since the rest of the processors in the system do not have their own disk drives, the background processor handles program storage for the graphics. It also performs the batch operations associated with scanning and publishing documents sent to the phototypesetter and proofreader. It can handle all of these functions because many publishing functions are nonrealtime, batch processes, and are not high priority operations. Their output can stretch over several minutes to several hours. Consequently, these low priority functions can be performed in the background and can be interrupted for several seconds or several minutes to access the disk.

Word processors or personal computers are linked to the background processor via a serial octal interface board, while communications with the other processors in the system use an internal Ethernet interface. To avoid any unnecessary overloading of the microprocessor, the disk control, tape control, and serial octal interface boards are configured for DMA; that is, they reference memory without going through the CPU. Additional space in the eight-slot Multibus rack is available for interface boards to the proofreader, phototypesetter, and scanners.

Contained in the same chassis are multiboard backplanes for the interactive graphics processor and the demand publishing CPU, each of which incorporates its own MC68010 and 1 Mbyte of RAM. The graphics processor contains these things plus interface boards for the internal Ethernet bus, serial processor I/O ports for the keyboard, and digitizers for each of the graphics terminals. Whenever the interactive processor needs anything from the Winchester, it accesses the disk via the internal 10-MHz Ethernet bus.

The interactive processor also contains a video memory board with 2240 x 1872 bytes (4 Mbytes) of bit-mapped image RAM, and a 155-MHz raster generator capable of generating 2240 x 1680 viewable elements on a 19-in. landscape display. Thus, the system can produce any font style sized between 4.5 and 72 point. A 64-bit word and access times ranging from 0.775 to 1 μs allow for many user interface operations.

For many applications, there is enough processing power available in either the graphics or data management processors to handle the scan input and raster output print functions. However, to further ensure that neither the graphics nor the data management processors are overloaded by unnecessary batch-oriented nonrealtime functions, each of these incorporate dedicated microprocessors. Physically, the two are very similar, each contains 1 Mbyte of RAM, and an internal Ethernet interface. However, each has different interface boards and translation software. The demand printing processor performs raster-image processing, translating the vector images into the appropriate raster output.

Four functions, performed in what appears to the user to be real time, enable user interaction with screen elements. This interaction is similar to the intuitive spatial/nonlinear process that the majority of ETP system users are most comfortable with. The system is designed so that panning (moving the screen view horizontally), scrolling (moving the screen view vertically), zooming (increasing and

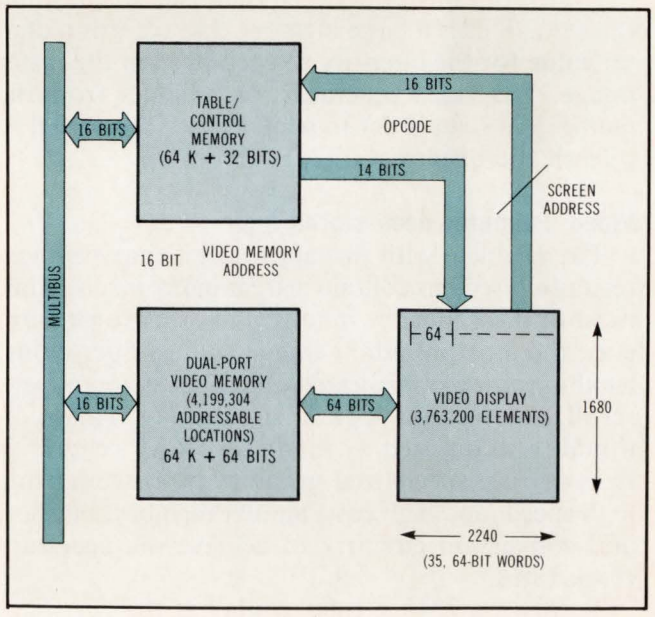


Fig 2 The use of dual-ported display and logic design allows high speed video processing without impacting the performance of the video processor.

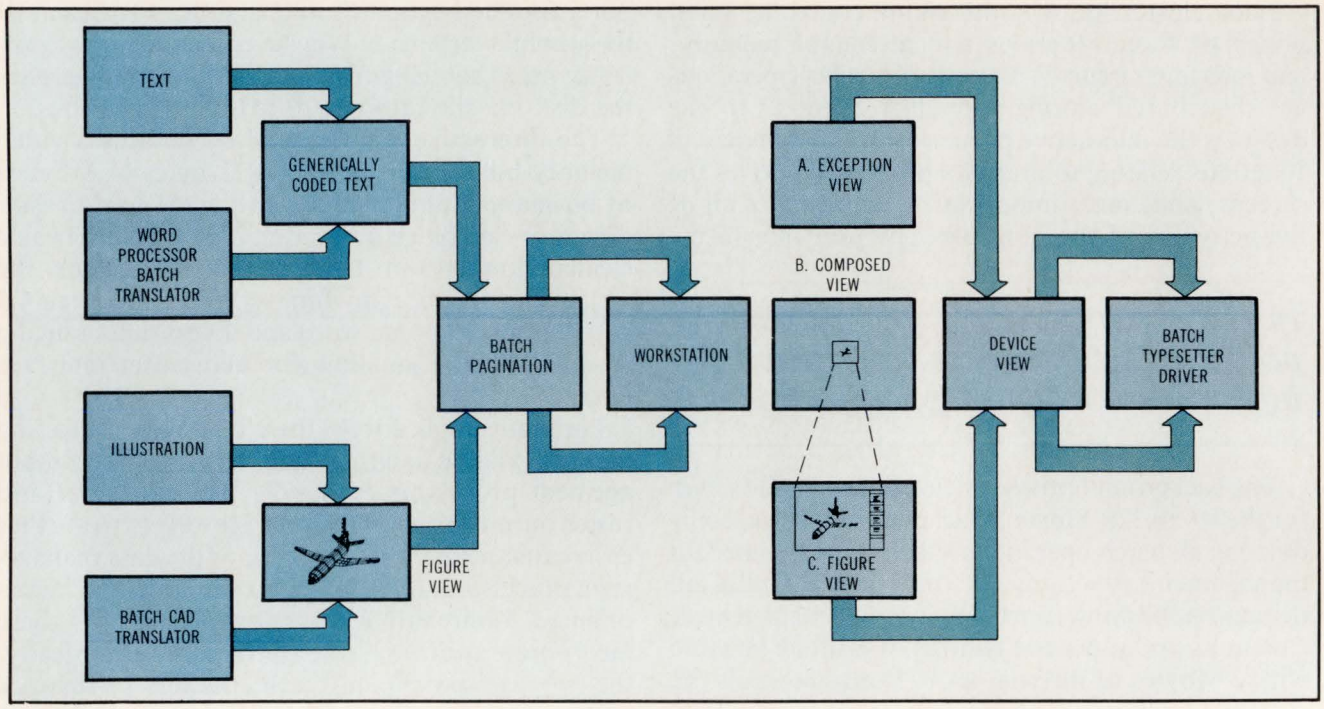


Fig 3 The chart shows the flow of a technical document as it passes through the system. Integration of text and graphics into the same data base is done using a proprietary integrated text/graphics database program. This program is written in C.

decreasing the size of the view on the screen), and, instantaneous recall and display of various dynamic menus can be performed without impact on the interactive processor's performance.

In raster scan systems, the graphics processor's basic function is to furnish information in a bit-mapped format that may bear no relation to the order of the lines, points, and characters in the system file. The most common solution is to insert a refresh display memory buffer between the raster display and the CPU. This is a large memory that records a digital value for the intensity of each pixel in the raster image. The video generator reads values from the memory in scan order to generate a video signal to refresh the display.

Video computer uses stored logic

The problem with this approach is that even low resolution screens contain a great many pixels. And, most of these must be modified in order to perform even the most mundane image change operations, let alone more sophisticated ones such as zoom, pan, scroll, and instantaneous menu display. The traditional solution used by many CAD/CAP vendors is to construct specialized graphics processors using high speed (and high cost) bipolar memory, bit slice, and conversion circuitry to achieve the necessary clock rates.

To drive a 2240 x 1680 display at the necessary 155-MHz rate, without overloading the interactive processor and without depending on high speed bipolar memory and bit slice components, Qubix has designed a proprietary (patent pending) video board that operates much like a stored logic computer. This board uses a dual-ported refresh memory architecture and a special video address lookup table to map a window in the 64-K words x 64-bit image memory into video values (Fig 2). Each entry in the table memory is viewed as a binary number. These numbers are used to index a table of video values represented as 64-bit raster words.

The 2240 visible pixels are scanned horizontally in 64-bit chunks for a total of 35 raster words per line. As each 64-bit word is scanned, the lookup table counter is incremented and, at the end of a complete screen, a clear signal is sent to the counter. By scanning in 64-bit raster words, the video memory need only operate at 1/64th the clock rate of the screen's 155-MHz raster generator. This is about 2.2 MHz or 800 ns, or about one-half the speed at which the memory can be driven. This allows the memory array to be dual-ported, with interleaved cycles, some going to the interactive processor CPU via the 16-bit wide Multibus, and some to the 64-bit wide video bus.

Zoom operations with the system are relatively straightforward. They involve only the addition or deletion of address lines in the lookup memory's address table. For example, to double the size of a character that is 16 bit lines high without losing definition, the address of each line must be reloaded, each one drawn twice. Similarly, to double the size of the image in the horizontal direction, a control signal from the control portion of the lookup table

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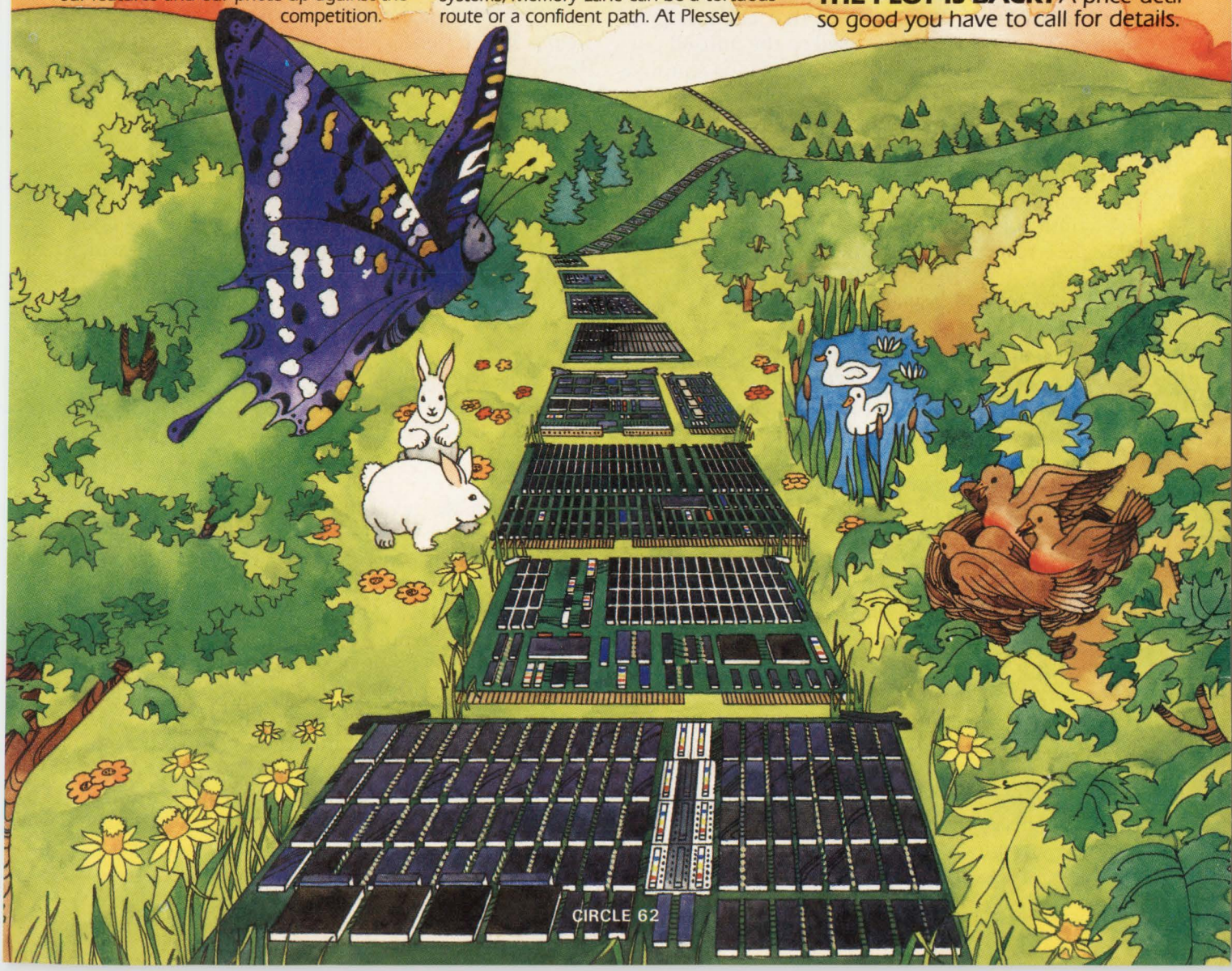

CIRCLE 62

memory must be sent to the video display. This cuts the clock rate in half. Thus, instead of shifting 64 bits out in 64 clock states, 32 bits are shifted out. The result is a bit transition every two clock states. In effect, this stretches each pixel in the designated area to twice its original width.

To perform pan and scroll operations, the system uses a 36th 64-bit word. Rather than incrementing all of the display addresses by one, the system loads and displays the invisible 36th word in 8-bit byte amounts. Since this is a table update, pan and scroll operations require only 1/36th as many memory location writes in the horizontal direction and 1/72nd as many in the vertical direction.

Finally, a variety of dynamic menus and other displays can be removed from the display and returned in microseconds and nanoseconds. Such "instantaneous" operation takes advantage of the fact that only 90 percent of the display memory (2240 x 1680 bits versus a total of 64-K x 64 bits) to address the raster display at any one time. Other systems with similar capabilities must erase the display completely, then recreate it. Similar operations in this system are nondestructive. That is, when a particular display is removed from the screen all that changes is its address location, from the used to the unused portion. With the Qubix system, redisplay is simply a matter of accessing the correct locations in memory rather than recreation of the needed image. Because the lookup table memory is only one-fourth the size of the video memory (64-K words x 16 bits versus 64-Kwords x 64-bits), such operations are usually four times faster than those systems which require complete recreation of an image.

Integrate text and graphics

The final element in the design of an ETP system that meets user needs is the integration of text and graphics into the same data base (Fig 3). This is achieved through the use of a proprietary integrated text/graphics database program, written in C, and running under a ported implementation of the multiuser Unix version 4.2.

Graphics information entered via the screen is processed through a figure translation program and entered into a figure data base stored on the Winchester hard disk. Scanned art is also entered into the figure data base after being converted from raster into vector form by passage through the graphics workstation and ghosted. Photographs are scanned and stored directly in rasterized form in a separate disk location. Graphics information from external CAD systems is passed through a graphics translator, then entered into the same figure data base. At the same time, a generic coded text data base is built on the disk. This consists of input accepted directly from text entry terminals and standard word processing input that has been passed through a text translator.

Also on the disk is a style data base, consisting of a set of rules to define the style for a particular user of the system (eg, a technical publishing department). It usually has specifications for column size and length, figure size, and the relation of figures to text and pages. This information is entered into the data base in two ways—it is either coded from the terminal keyboard or via a style editor. A style editor allows the user to layout the page directly on a workstation CRT and performs all the exception processing related to the data base.

Redisplay is a matter of accessing the correct memory locations rather than recreating the needed image.

Once the style, figure, and generic text are entered into the system, the user simply invokes a batch composition command from either the keyboard or the screen. During the first pass through the batch composition and pagination process, the style and text is passed through a generic translator. This generates a logical data base on the disk in which the two are combined. On the second pass, the logical data base goes through a pagination process. At this time, the figures in the figures data base are combined with the style and textual information. On the last pass, a physical data base that combines all three elements is generated.

Exception processing best illustrates the system's ability to respond to and interact with users. Exception processing involves determining the location of stylistic, artistic, and textual errors, cataloging and bringing them to the user's attention. In this system, the process is performed in parallel with batch pagination and composition. All exceptions generated during graphics, text, and generic translation are sent to an exceptions file on the disk. Then, during the last pass of the batch pagination and composition process, all of the exceptions—textual, graphics, and generic—are tagged to a specific page and/or line. Then, an exception list is generated and sent to the screen.

Manipulating the text/graphics data base

The process by which the operator interacts with the various elements of the integrated text/graphics data base to produce a completed document is similar to manual page layout and typesetting. In the manual process of layout, the editor takes a piece of paper, a pencil, and a ruler, and constructs a blue line with the appropriate column widths indicated. Next, the various components are listed: headlines, subheads, text, italics, and footnotes. Next, the editor selects the various type styles. Then, the actual typewritten copy is marked with the appropriate symbols, indicating where each type style is to be used. This marked up copy is then sent to a typesetter who selects or creates the hot type in the correct styles.

This is then put into a large wooden frame, called the mold.

In many semi-automated systems, the marked up copy is given to a computer operator who translates the copy editing instructions into a code the computer understands. In the more automated systems, which merge text and graphics in batch mode, the editor must abandon traditional copy editing instructions and enter the computer commands directly into the text.

In the Qubix system, instead of drawing on a piece of paper with a ruler and a pen, the editor takes a pen-like sonic stylus and draws the layout on the outline of a piece of paper on the screen. As the editor draws in the vertical and horizontal directions with the stylus, the appropriate lines are drawn with their measurements in picas shown in small windows on the side and at the bottom of the screen. Once the lines are drawn, the system understands that those are the boundaries of the columns on the page. It is not necessary to type in the appropriate computer instruction to indicate the measurement in picas, since it is already drawn on the screen.

Instead of looking up the typestyles and writing down the appropriate symbols, the editor goes to the command window on the screen, which contains all of the major 20 or so subelements of a page layout. The editor points to the appropriate subelement with the stylus and moves to another window on the screen. This allows the user to scroll through a list of all the existing fonts. At the top and bottom of this window are arrows. Pointing to the top arrow scrolls the window up. Likewise, pointing to the bottom arrow scrolls the window down. Once the correct font appears, the editor points to it with the stylus and then at the execute command. The computer interprets this as the type style for the particular subelement selected.

A system that integrates hardware and software to make even the most complex operations as transparent as possible to the nonexpert user enhances the creative process involved in technical publishing. This requires a powerful system architecture that allows users to interact in real time, to switch between simultaneous activities quickly and easily, and to transfer data between interdependent activities in a consistent manner.

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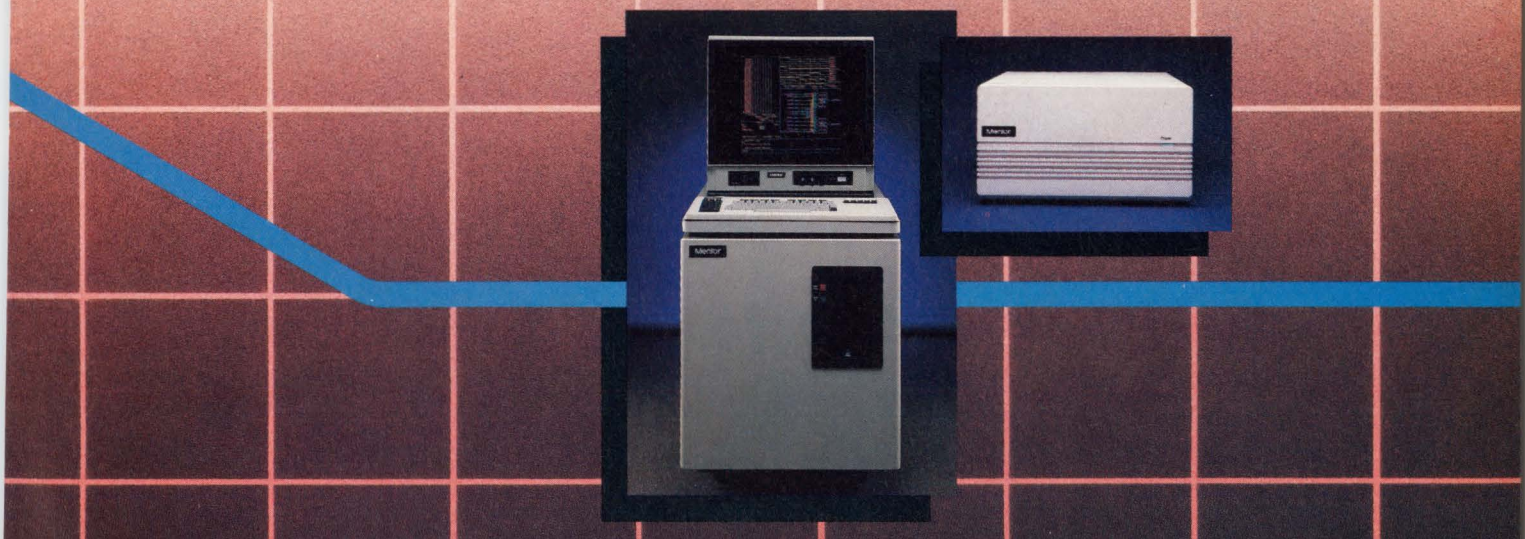

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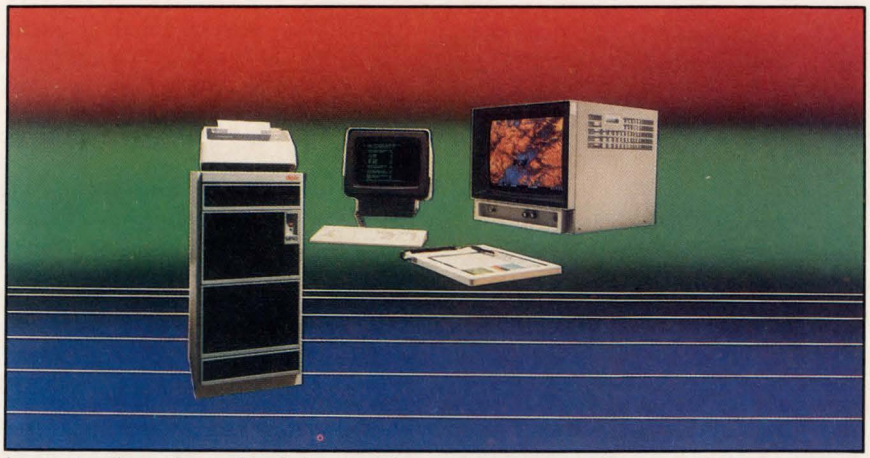
CIRCLE 65

Image processing vaults beyond the world of 512 x 512 pixels

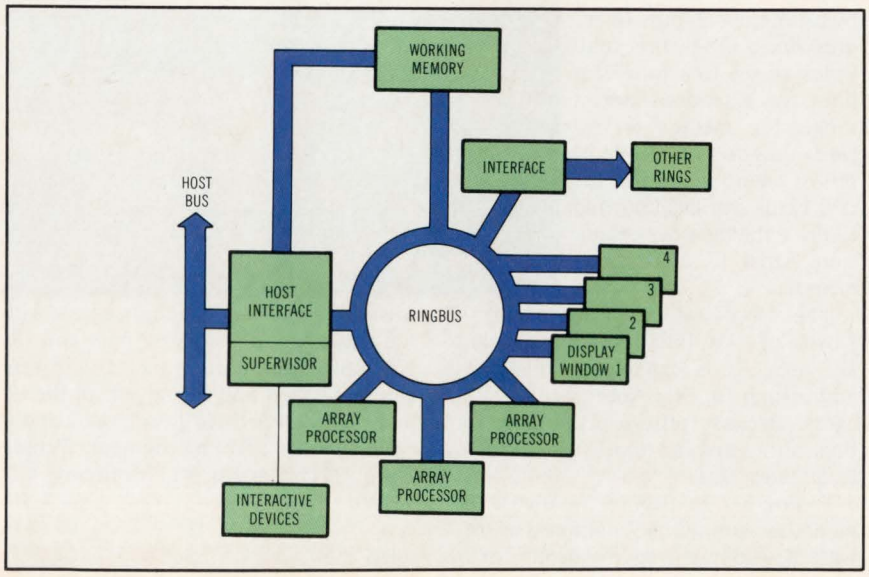


The MPX-3 provides the system integrator with a potent image processing subsystem for high resolution, large image display. Built around a unique Ringbus architecture, the MPX-3 offers versatile, "image crunching" capabilities for applications that match imaging with computer power. Remote sensing applications stand out when considering this system, but geophysical, medical, simulation, graphic art, and picture archiving applications are other areas likely to be pursued.

Rather than using a bit-plane memory structure, the MPX-3 uses a dynamically reconfigurable memory format. This means that images being processed can take any arbitrary rectangular shape or can consist of several hundred overlaid sections viewed in parallel. For example, three-dimensional seismic data and magnetic resonance imagery can be viewed. The three-dimensional data set may be scanned along any of its three principal orthogonal axes without further processing. Diverse image formats can be loaded, combined, extracted, and overlaid with this system. In mapping applications, Landsat and radar data can be overlaid. In medical settings, cardiographs and X-rays can be simultaneously viewed.

At the center of the MPX-3 is a Ringbus that allows data exchange among system components at a 40-Mbyte/s rate. Memory is dynamically allocated according to the dimensions of each image. The Ringbus supports a supervisory processor, a working memory, an integer processor, and a display window capable of feeding data to four independent workstations. The 32-bit wide Ringbus can accommodate up to 16 parallel processors. It can also connect to other Ringbuses.

Working memory board capacity measures 2 or 8 Mbytes. Cycle time for a 64-bit word hits 208 ns. Maximum system capacity is 128 Mbytes. A fully configured system can hold over 500 images, each 400 lines x 300 pixels x 16 bits/pixel. The tri-ported working memory provides program incremented access to the Ringbus, a DMA port to the supervisory processor for host image loading, and random access to the supervisory processor.



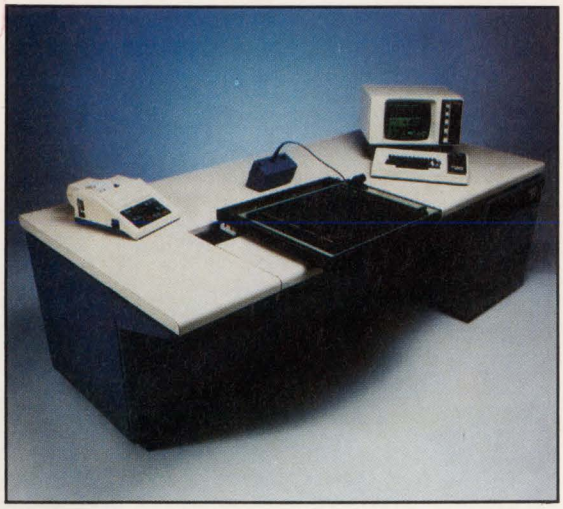
The NS32016-based supervisory processor operates at 10 MHz and features 512 Kbytes of RAM and 128 Kbytes of ROM. Through the supervisory processor, the MPX-3 links to the host. Currently, DEC VAX 700 series machines represent typical hosts, but MPX-3 designers indicate other hosts can be efficiently connected. The host to working memory data transfer rate hits 1.5 Mbits/s in the burst mode.

Realtime display features offer dynamic operating range. Synoptic overview allows zoom from a large image overview to a single pixel and back without reloading the image. A "filmloop" feature provides dynamic assignment of image memory to create full color film loops (at rates approaching realtime video) across more than 500 image sections. Images can be moved around the screen, stacked according to priority, peeled to uncover the image beneath, or expanded in either axis.

The system's multiple display capability supports up to four screens, each with numerous display windows of any rectangular shape. An overview reference display can be held on one screen, while other screens undergo image processing activity. Formats include 512 x 512 or 484 x 512 (selectable), or 1024 x 1024 pixels. Display buffer D-A converters offer full 8-bit resolution. Shipments of the MPX-3 are scheduled for the second quarter of 1985. **Dipix, Inc**, 10220 Old Columbia Rd, Columbia, MD 21046. —*J.V.*

Circle 260

In-circuit testers expose device timing errors



Designed for LSI and VLSI testing, the series 700/730 are in-circuit testers that can detect device-data timing errors. Devices that function—but perform outside the desired range of specs—can be identified during in-circuit testing. The result is an improved yield at the next test station. The Flexpin hybrid architecture allows the flexible programming and easy debugging found on nonmultiplexed systems—all while maintaining low cost per pin of multiplexed in-circuit testers.

The testers consider the time and relational specs from a manufacturer's data book. Standard tests include fixture verification, shorts, and continuities, analog components, SSI, and VLSI.

Conventional in-circuit testers have clock generators that only produce control signals. These signals determine whether the device under test (DUT) works. The 730 tester offers timing and format control of the DUT input stimuli, at pattern speeds to 10 MHz.

The 730 tester has a feature called the Protector. Automatic back-drive time and duty cycle control sets back-drive time according to manufacturer's specs or user's standards.

Flexpin architecture, like multiplexed systems, packages its hybrid pins in groups. Any pin in the group can be designated the dynamic pin. Using a multiplexed system, once all dynamic pins are assigned, the remaining pins become unavailable. Using Flexpin architecture, the remaining pins are controlled by their own drivers, which can be set high or low.

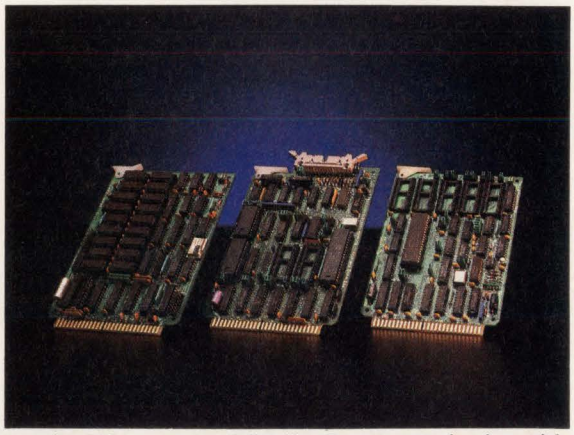
This whole process eliminates pin contention when the need for extra guarding arises during debug and change. Other benefits of the scheme include reduced board programming times and eliminating fixture rewiring.

Behind the pin is a RAM that can be configured in two ways depending on the device being tested. The 4-K x 4-pin RAM used together with the sequence processor, the Accelerator, introduces algorithmic pattern to devices such as microprocessors and dynamic RAMs. The 16-K pin configuration tests custom and semicustom devices (gate arrays and devices that use LSSD test techniques) where long linear pattern depths are needed.

Also included is a diagnostic software package that analyzes the initial results and removes potential ambiguities resulting from a fault message. This helps the user to spot the causes of failure. For bus-related faults, a software feature will automatically pinpoint a failing device. For time-related bus faults, a current probe pinpoints the failure at speed. Price is $150,000. **Factron/Schlumberger**, 299 Old Niskayuna Rd, Latham, NY 12110. —*M.B.*

Circle 261

Card family puts 8088 on STD bus



In order to bring 16-bit processing to the 8-bit STD bus domain, a family of STD cards arrives supporting the Intel 8088 processor. The 8088 not only brings a 16-bit internal architecture to the STD bus, but also allows code to be developed on IBM PC or PC-compatible computers, then down-loaded to the STD environment via an RS-232 channel.

The card family consists of two 8088 CPU cards and a 512-Kbyte dynamic RAM card. The new memory board takes advantage of many 8088 features, but the CPU boards can also work with the vast number of existing STD boards from more than 100 different manufacturers.

The two CPU cards are the 7861 multifunction CPU card and the 7862 8088 processor card. The 7861 has 136 Kbytes of onboard addressing capability in five byte-wide JEDEC sockets and can address the 8088's full 1-Mbyte memory address space. The 7862 accommodates up to 64 Kbytes of onboard erasable PROM and 8 Kbytes of onboard RAM. Both CPU cards address the 20-bit memory address space by using the STD bus, 16 address lines, and by time multiplexing the first four data lines for extended address range. For memory or I/O cards that do not decode 20 bits of memory address, the CPU cards can be jumpered to drive the memory expansion signal to bank select memory.

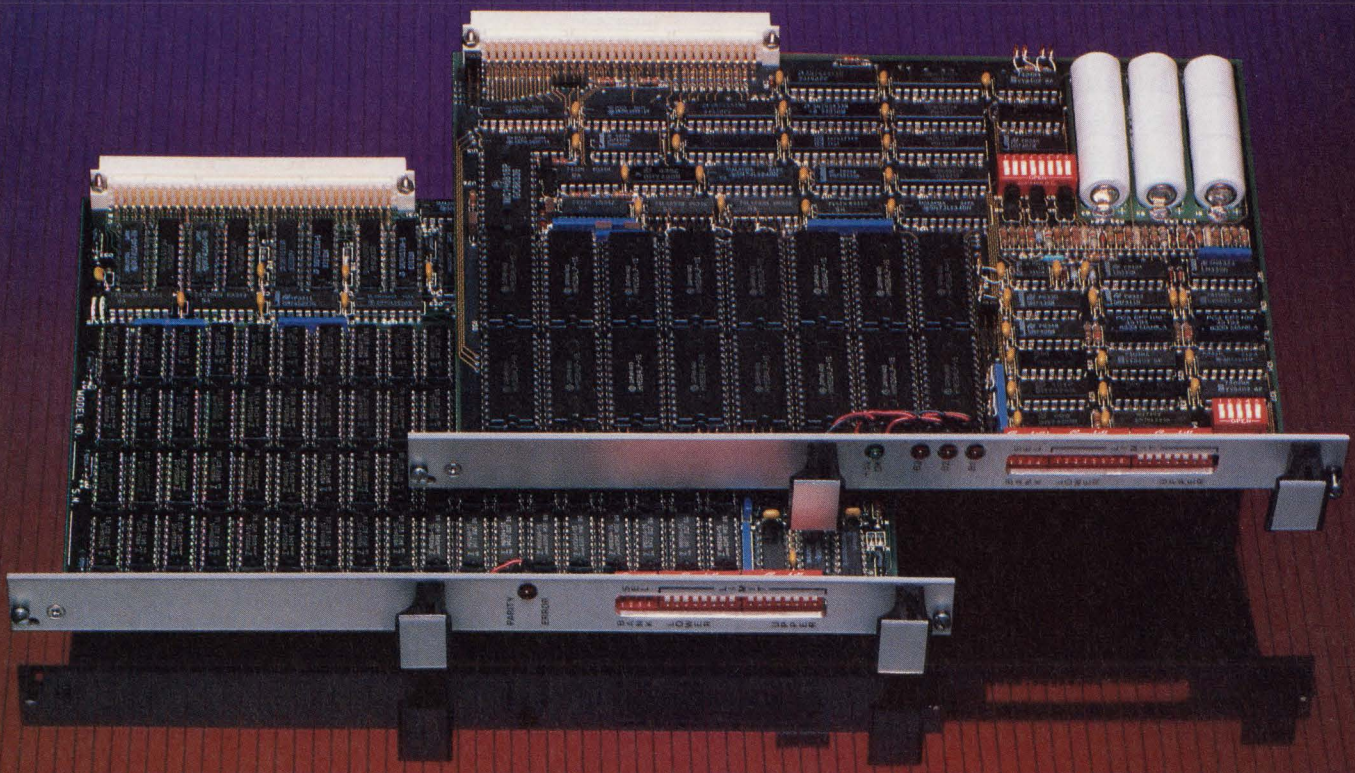
The 7712 DRAM card can contain 512 Kbytes of RAM, if 256-Kbyte DRAM chips are used. It is capable of full 20-bit addressing for use with the 8088 CPU cards. Because refresh takes place onboard, the card can appear to the system as a static RAM.

Prolog has envisioned the use of IBM PC and PC-compatible computers as software development environments for its 8088 card family. By communicating with the 8088 CPU via the RS-232 port and the communication port on the PC, software can be written and debugged on the PC and down-loaded for testing and application to the STD environment. **Prolog Corp**, 2411 Garden Rd, Monterey, CA 93940. —*T.W.*

Circle 262

VMEbus MEMORIES

High Speed DRAM — Non-Volatile CMOS



Micro Memory boards allow you to take advantage of VMEbus reliability in your business and industrial control systems. Our VMEbus family includes both high-speed DRAM and non-volatile CMOS memories that are compatible with the VME/10 microcomputer.

Our MM-6000D and MM-6200D are high-speed DRAM memories that provide 2M bytes and 4M bytes, respectively... the highest in the industry. Both boards have parity generation and checking that is indicated on a front panel LED.

If you need non-volatile memory, the MM-6500C and MM-6600C CMOS memories have redundant on-board batteries. Data retention is five years for the lithium version and three months for the NiCad version. The boards are also versatile because you can mix EPROMs and CMOS RAMs. And, the capacity of these two boards is the highest in the industry.

All boards are burned-in for 48 hours during memory diagnostics and there is a one-year warranty on parts and labor.

Model No.	Capacity	Cycle/Access, nsec	Type	Word Length
MM-6000D	256K, 512K, 1M, 2M	330/210	64K or 256K DRAM	16-bit
MM-6200D	512K, 1M, 2M, 4M	350/220	64K or 256K DRAM	32-bit
MM-6500C	32K, 64K, 128K	200/200	CMOS w/Calendar-Clock	16-bit
MM-6600C	64K, 128K, 256K	200/200	CMOS	16-bit

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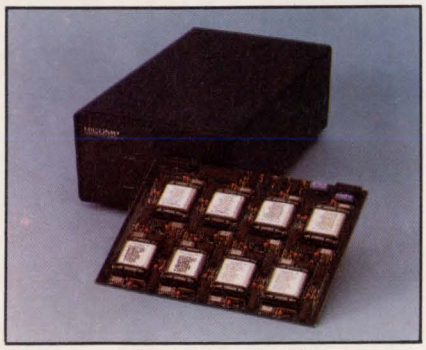
CIRCLE 66

Bubble memory serves well in tough settings



The MBM-1A is a rugged bubble memory system built to withstand the effects of hostile environments. Available with either 500 Kbytes or 1 Mbyte of nonvolatile solid state memory, the unit resides in an enclosure the size of an 8-in. floppy disk drive.

This unit links to a host as a floppy disk drive or as a block access peripheral. In the floppy emulation mode, the MBM-1A emulates up to four 5¼- or 8-in. drives, supporting varied single- and double-density formats. This mode requires a Shugart-compatible controller. No additional software development is needed. The MBM-1A's write-protect feature allows each emulated drive to be write-protected by setting a front-panel switch.

In the block access mode, individual blocks of bubble memory can be randomly accessed in 512-byte segments using simple software commands. Commands include Write, Dump and Read Data Status Read, and Abort. The interface required here is an RS-232-C serial I/O port.

The enclosure measures 8.55 x 14.6 x 4.62 in. (217 x 370 x 117 mm). Track-to-track access time hits 6 ms in the 5¼-in. floppy emulation mode—3 ms for 8-in. emulation. Block access mode transmission ranges from 300 baud to 9.6 kbaud. An internal switching power supply handles line surges and dropouts.

Bubble technology provides reliable operation. Bubble memory is nonvolatile, so data remains intact when the system loses power. Battery backup is not required. Because the MBM-1A is based on solid state technology, it is not subject to problems associated with electromechanical devices.

The 1-Mbyte version of the MBM-1A costs $4950, while the 500-Kbyte model sells for $3450. **Hicomp Computer Corp**, 5016 148th Ave NE, Redmond, WA 98052. —*J.V.*

Circle 263

Printer uses binary charge technology to combine text/graphics

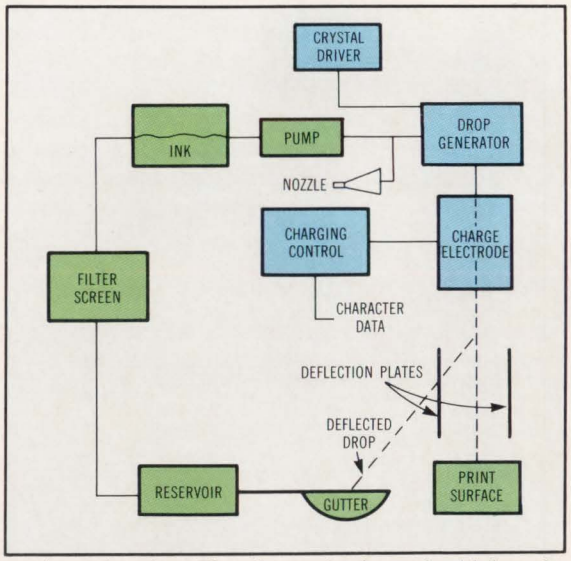
This multifunction ink-jet printer offers full-page, all points addressable printing. It combines graphics and text at 300-dot/in. resolution and prints up to 18 pages/min. Standard features include 128 Kbytes of internally buffered RAM storage, a resident multipurpose font set, automatic two-sided printing, Centronics interface and Xerox 2700 emulation, and self-test and operator diagnostics.

The printer can operate in two modes. Quality mode prints letter quality at a 300- x 300-dot/in. resolution. Alternate mode prints draft quality at high speeds. The host terminal controls formats with automatic subscripts and superscripts. The device prints in portrait or landscape modes or a combination of both. Many type fonts are available, including logotype.

Using multiple array ink-jet technology as an approach to binary continuous-flow ink-jet printing, the printer permits all points addressable direct imaging for custom graphics, mixed type fonts, and logos. The continuous flow approach creates individual drops by pressure waves. Then, the drops are charged selectively, adopting particular trajectories.

The charges determine which drops hit the page and which go to a special ink catcher. Two types of deflection techniques are available: multideflection and binary. The binary approach leaves droplets charged or uncharged. If uncharged, they travel on a direct path to the paper. If charged, they are deflected into a catcher system where the ink is recycled.

The printing process begins when ink, under pressure, is forced through an opening, while the ink chamber is stimulated at a particular frequency in the printhead by a piezoelectric crystal. The ink stream breaks into precisely spaced, uniform drops. As each drop breaks off, it passes through an electrical charging zone that imparts a control charge on the drop.



The binary system requires an opening for each dot position. In the company's patented approach each position in the array matrix corresponds to an individual jet. The closer the jets, the higher the resolution, and with multiple jets, higher throughput is available. The printer will sell for $5000 to $7000. Deliveries begin first quarter of 1985. **Diconix, Inc, div of Eastman Kodak Co.** 3800 Space Dr. PO Box 3230, Dayton, OH 45431.

Circle 264 —*M.B.*

Hardware/software standards merge in design workstation

The C1200 workstation is specifically designed for engineering applications in the office environment. Performing at 1½- to 2-times the speed of a VAX-11/780 for engineering work loads, the unit executes 2-million single-precision and 1.5-million double-precision Whetstone instructions/s. The system architecture allows single- or multi-user systems, either standalone or networked for peripheral access and sharing data.

Combining high performance with industry standards in hardware and software, the deskside unit offers a large virtual address space, full 32-bit data paths, and the Unix operating system. In addition, it can be configured with up to 24 Mbytes of memory.

On the hardware side, the workstation uses a proprietary ACCEL processor—a true 32-bit computer. The architecture is optimized for high performance on computationally intensive tasks and supports flexible bit-mapped display generation. To advance the hardware standards approach, the units incorporate an integrated network, called Accelenet. It can communicate with other systems connected in IEEE 802.3 (Ethernet) LANs. The I/O subsystem is compatible with the IEEE 767 (Multibus).

The processor has separate registers and processing units for both integers and floating point numbers. Basic trigonometric and arithmetic functions are microcoded in the FPU. The workstation along with demand-paged virtual memory, supports individual program address spaces of up to 2 Gbytes. The file system automatically optimizes file placement and performs operations in large blocks to minimize disk access overhead.

The operating system is based on 4.2 BSD Unix, and software is optimized with extensions to support bit-mapped graphics, multiple window displays, distributed files, and communications. Optimizing compilers are available for Fortran 77, Pascal, and C.

The unit has two different color graphics display subsystems, both available with tablet or mouse. One display uses a 19-in., 60-Hz, noninterlaced refresh monitor to provide 1280 x 1024 resolution, eight-bit planes for color selection, and vector writing speeds of 60,000 one-cm vectors/s.

Basic configuration includes the 32-bit ACCEL processor, the extended FPU, 56-Mbyte disk drive, streaming cartridge tape drive, 2-Mbyte ECC memory, and a system software license. In quantity, the price for the basic unit is $45,000. The high resolution color display is $27,600. **Celerity Computing**, 9692 Via Excelencia, San Diego, CA 92126. —*M.B.*

Circle 265

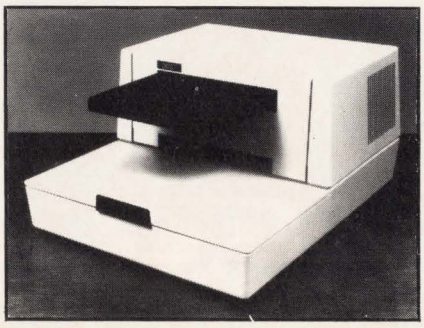
Scanner digitizes graphics and reduces storage requirements

Typewritten pages that include graphics can be scanned and read into a host computing system with series 100 image scanners. In addition, an optional series 4400 character recognition controller reduces data storage requirements by transmitting text as ACSII character codes.

Series 100 image scanners can read a typewritten page, including logos, charts, or signatures, and transmit a bit-mapped image to the host. They can also be programmed to recognize typewritten text only. These desktop scanners come in three models with scanning resolutions of 200, 240, or 300 pixels/in. Scanning speeds range from 9 to 13.5 s/page.

The character recognition controller is a board located in the host system. Character recognition can reduce data storage requirements by as much as 10 to 1. Only the graphic information is retained as bit-mapped data.

By converting text to character codes, the controller lets users edit, merge, or manipulate text. For example, documents can be filed and retrieved by keyword, and word processing applications can be developed by the user.



The combination of the series 100 image scanner and the series 4400 character recognition controller allows the creation of documents with text and graphics. For example, a manual where schematics and text are scanned, manipulated, and merged could be produced.

All series 100 models include an automatic stack feeder that hooks up to 75 pages. Page sizes can range between 6 x 6 in. and 8½ x 14 in. The scanner will automatically adapt to paper with varying color and contrast.

Prices for the scanner and controller should range between $7000 and $10,000, depending on quantity and configuration. Product shipment is scheduled for the fourth quarter of 1984. **Dest Corp**, 2380 Bering Dr, San Jose, CA 95131.—*R.G.*

Circle 266

New SKY WARRIOR

15 MFLOP Array Processor cuts through $1,000/MFLOP barrier!

At $14,900*, it's the most economical way yet to put mainframe number crunching into your microcomputer.

The 15 MFLOP SKY WARRIOR isn't simply a minor technological advance. It's nearly a revolution, fully twice as cost effective as anything else on the market. Capable of performing 15 million 32-bit floating point operations per second. And ½ million operations per second on 64-bit data.

Use it for 2-D Fast Fourier Transforms in imaging systems, in on-site seismic analyses, in 3-D graphics workstation transformations, in real time laboratory signal processing systems, or anywhere else requiring fast interaction with lots of data.

We're experienced veterans at porting hardware. We'll adapt SKY WARRIOR to your custom bus the same way we've adapted our other SKY products to many custom buses already. SKY WARRIOR is compatible with the VME bus, and will soon be compatible with other standard bus structures, too.

SKY WARRIOR's tightly coupled architecture gives you speed as well as easy access to maximum system memory. And remains invisible to your end user in the process.

This easy-to-use, plug-in processor comes fully software supported by a rich library of user-callable subroutines.

All software developed for our popular, field proven Micro Number Krunchers will run on SKY WARRIOR, too.

You don't have to worry about delivery, performance or backup when you deal with SKY. We specialize in floating point products. Our customer list reads like a scientific and engineering Who's Who. Ask and we'll give you references. They'll tell you what they tell us, things like *rock solid engineering*, *instant responsiveness*, *super technical support*, and *total product reliability*.

For detailed technical information on our exciting new SKY WARRIOR or any of the other products in our LEGION of arithmetic processors, contact SKY Computers, Inc., Foot of John Street, Lowell, MA 01852, telephone (617) 454-6200.

SKY

SKY COMPUTERS

*Quantity 1. OEM discounts available.

CIRCLE 67

Supercomputer gets a four-processor adaptation

The four-processor X-MP/48 with 8 million words of central memory and the X-MP/1 with 1, 2, or 4 million words highlight the Cray X-MP series. Additionally, redesigned X-MP/2 models are available with reduced size and power requirements. A DD-49, which is a 1200-Mbyte high performance disk drive, and a model of the solid state storage device featuring 1 Gbyte of semiconductor memory. All models in this series are in production, with first deliveries scheduled for the fourth quarter of this year. Mainframe prices range from $5 million to $14 million. **Cray Research, Inc**, 608 Second Ave S, Minneapolis, MN 55402.
Circle 267

Hardware virtual memory distinguishes 32-bit machine

MegaMicro computers incorporate the NS16032 CPU for 32-bit internal logic with an internal data path configured on the Multibus 16-bit interface. Demand-paged virtual memory is used in hardware, as is 64-bit double-precision floating point arithmetic. The hardware virtual memory provides up to 16 Mbytes of address space per process. Systems can include 1 to 16 Mbytes of RAM, an intelligent disk controller supporting four Winchesters and two floppies, and a 1-Mbyte floppy drive with cartridge and nine-track tapes. A reconfigurable Berkeley 4.1 Unix (with 16-user license standard), plus C and Fortran 77 compilers are available. A unit with 512-Kbyte RAM and 33-Mbyte Winchester, costs $20,000. **Logical MicroComputer Co**, 4200 W Diversey Ave, Chicago, IL 60639.
Circle 268

Entry-level supercomputers achieve 28-MFLOPS performance

Five IBM-compatible supercomputers form the AS/91XO series, which aims at providing low cost vector processing. Machines in this series can typically perform at 28 MFLOPS. Users of existent AS/90X0 computers can upgrade to AS/91X0 performance levels. The AS/91X0 computers include a software tool called VAST (Vector and Array Syntax Translator). With these units, users can run 370 software on a machine running vector-processing applications. Prices in the series range from $2.1 million for the AS/9140 to $5 million for the AS/9180. Upgrades are priced at $300,000 for uniprocessor systems, and $600,000 for multiprocessor models. **National Advanced Systems**, 800 E Middlefield Rd, Mountain View, CA 94040.
Circle 269

Realtime 3-D color images join artificial intelligence line

A LISP machine line adds the IRIS system for realtime 3-D color graphics. IRIS includes a 1024 x 1024 raster image memory, currently displayed on a 1024 x 768 RGB monitor. The system has 12 bits of image memory (expandable to 24 bits) and yields over 16 million colors. A proprietary VLSI circuit—the Geometry Engine—allows high speed display processing and realtime manipulation of 3-D shapes. IRIS has computer-generated animation rates exceeding 65,000 3-D transformations/s. Ten Geometry Engines handle object rotation, translation, scaling, four-plane clipping, and perspective. A graphics library has over 150 subroutines. Price is $40,000; deliveries start in the fourth quarter. **LISP Machine Inc**, 6033 W Century Blvd, Los Angeles, CA 90045.
Circle 270

Supermini employs ECL and supports 4-Mbyte memory

The 9750 midrange supermini melds high speed ECL circuitry to a five-stage pipelined CPU architecture. It supports up to 128 terminals and 255 interactive processes simultaneously, and is available for extant system upgrade. The system supports all series 50 communication and peripheral devices. Cost of a typically configured 9750 (including 4 Mbytes of memory, two 315-Mbyte fixed media disks, a 1600-bit/s streaming magnetic tape subsystem, a CRT console, and Primos operating system) is $251,500. Upgrade pricing starts at $98,000. Another model, the 9650, supports 96 terminals and has 2 Mbytes of memory. The 9650, using a custom gate array-based processor and two-stage pipeline, costs $146,500. **Prime Computer, Inc**, Prime Park, Natick, MA 01760.
Circle 271

Workstation can stand alone or support 3270 host access

Designed to run most PC software, the 1186 intelligent workstation operates as a standalone local processor or as an online 3270 display station. As a standalone unit, the 1186 uses MS-DOS. An 80186 microprocessor speeds program execution. The 1186 comes with either two dual-sided, double-density floppy disk drives, each with 360 Kbytes of formatted memory. Or, a 10-Mbyte hard disk and single floppy can be used. The unit is priced at $3025 for the two-floppy disk model, and $4980 for the hard disk. **Telex**, 6422 E 41st St, Tulsa, OK 74135.
Circle 272

Multi-user graphics system turns terminals into workstations

The GC-1000 graphics series converts D-Scan GR-1100 or GR-2400 terminals into workstations for high resolution graphics applications. This multitasking, multi-user unit is based on the 16-bit 8086 with local RAM and mass storage, and runs the concurrent CP/M operating system. The GC-1000, model 1020, consists of 256 Kbytes of RAM , one 5¼-in. 655-Kbyte floppy disk, a bidirectional Centronics parallel interface and four serial I/O ports, plus RS-232 and RS-422 ports. Languages include C, C-Basic and Fortran-77. The Graphics System Extension is supported. Prices start at $4950. **Seiko Instruments U.S.A, Inc**, 1623 Buckeye Dr, Milpitas, CA 95035.
Circle 273

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Molded construction highlights assemblies that surpass emi standards

A series of D-subminiature assemblies exceeds all electromagnetic compatibility standards. Dubbed the Ulti-Mate-D, the series is rated at 60 to 70 dB. Its general-purpose shielded style meets RS-232 and RS-449 standards. Thumbscrew/nut retention systems are optional on all three models. Contacts are C77000 nickel silver with optional selective gold finish. Single-conductor or twisted-pair cables may be specified, UL-Style 2464 and UL-Style 2448. It includes three basic models with four sizes (9, 15, 25, and 37 positions), each in male and female types. **Symbex**, 72 Corwin Dr, Painesville, OH 44077.
Circle 274

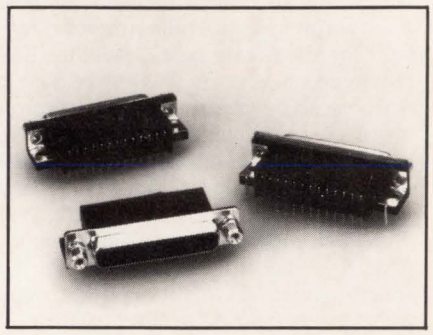
Dvorak format unit is replacement for PC keyboard

An IBM PC replacement keyboard features the Dvorak format. Such keyboards in the Maxi-Switch 8500 series feature improved tactile feel. Also distinguishing this product are built-in palm rest and adjustable support legs. The replacement keyboard, housed in a white molded case that matches the standard IBM PC cabinet, is available from stock at a price of $149.95. **Century Research & Marketing**, 10800 Normandale Blvd, Bloomington, MN 55437. **Circle 275**

Solderless LED device provides simple electrical connections

Conxrite CNX 310 series has a molded plastic body with a self-contained interchangeable ¼ W resistor. The connector can be used on circuits from 3 to 28 V with wiper type contacts compensation for varying sizes of LED leads. It requires no tools for assembly, while providing a simple fast press fit connection. Price is $0.34 each in quantities of 10,000. **Visual Communications Co**, PO Box 986, El Segundo, CA 90245. **Circle 276**

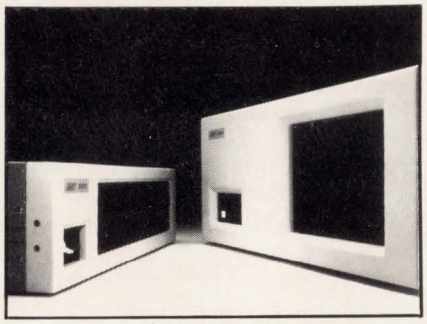
Connectors suppress emi/rfi leakage



The Metal Shell "D" subminiature connector has a tin-plated metal shield design to suppress emi/rfi leakage. Grounding integrity derives from a threaded rivet and diverse grounding brackets, including a wraparound version that passes under the mounting flange to the PC board. Users can choose either molded and threaded inserts or jackscrews. These connectors ensure a closed entry interface and positive pin protection. Devices are available in 9, 15, 25, and 37 contact sizes. **Burndy**, Richards Ave, Norwalk, CT 06856.
Circle 277

MICROPROCESSORS/MICROCOMPUTERS

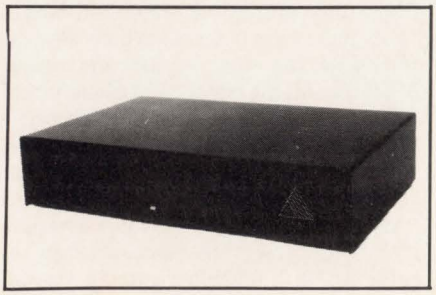
Memory management enhances 68000-based system



The Multibus-compatible SBE 300 line of 16/32-bit computer systems executes at 10 MHz without wait states. The SBE 300 line combines a 68000 or 68010 MPU with the Unix-like Regulus operating system and features memory management circuitry that contains 32 independent maps. Each map can support a realtime task of 4 Kbytes to 8 Mbytes in size. Up to 8 Mbytes of hardware refreshed, no-wait-state dynamic RAM can be accessed by the CPU, which interfaces with a disk controller through the SBEX-SASI multimodule interface. Mass storage includes a 10-Mbyte, 5¼-in. hard disk. The system has 10 Multibus slots, (eight available for expansion). Quantity-100 price is $5795. **SBE, Inc**, 4700 San Pablo Ave, Emeryville, CA 94608.
Circle 278

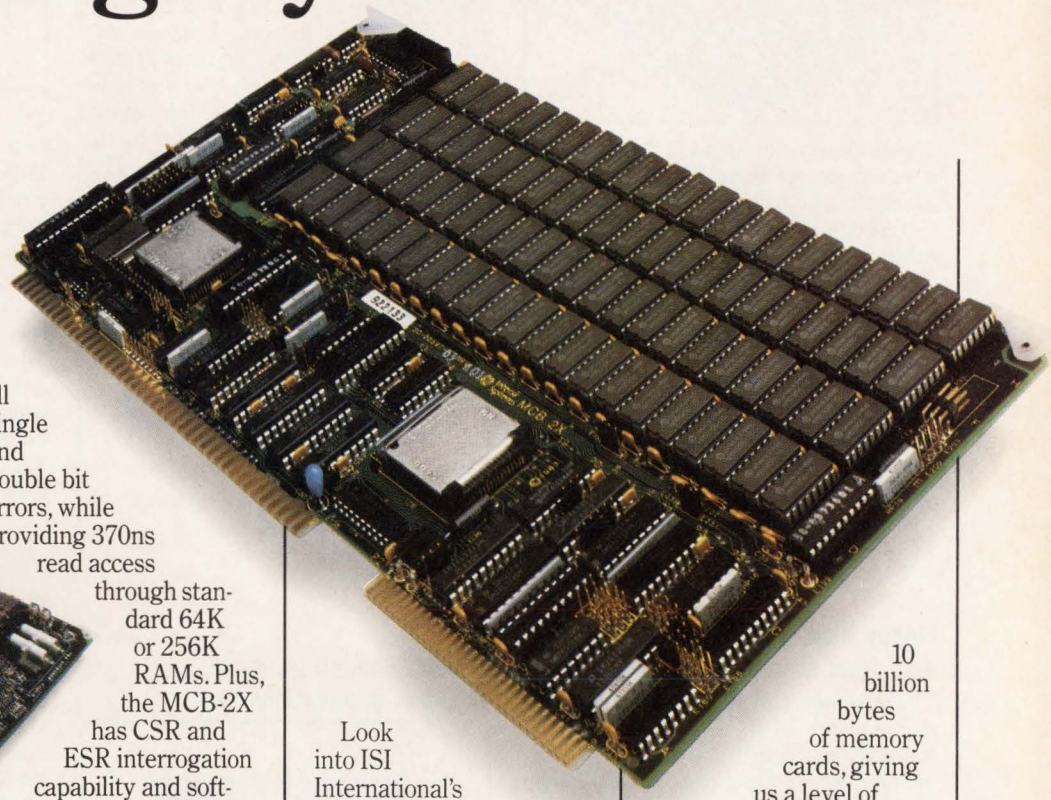
Multi-user system based on 68000 sports 3-MIPS rate

The Pinnacle is a 12-MHz 68000 microcomputer executing at a 3-MIPS rate. RAM size reaches 8 Mbytes. Part of RAM is used as a "RAM disk" that emulates floppy and Winchester activity (eg, storing often used programs). The Pinnacle uses a portable UCSD p-System operating system. Seven RS-232 ports mean seven users can simultaneously use the machine. The hard disk system starts at $5995 and the dual floppy at $3895. **Pinnacle Systems**, 10410 Markison Rd, Dallas, TX 75238.



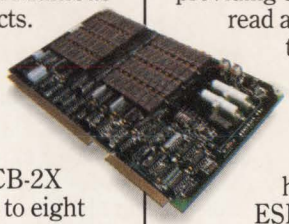
Circle 279

The first thing ISI International put on this new Multibus® card was 2 megabytes...



And that was just the beginning.

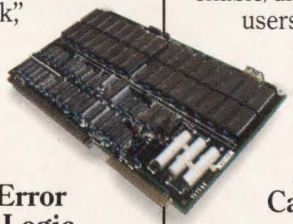
Squeezing 2 megabytes of memory onto a single Multibus* card is quite an accomplishment in itself. But we believe it takes more than just memory to meet the increasing needs of today's systems. That's why our new MCB-2X Multibus card is designed with a number of significant special features. And why ISI International is truly a leader in Multibus memory products.



MCB-364

Superior Dynamic Memory Relocation.

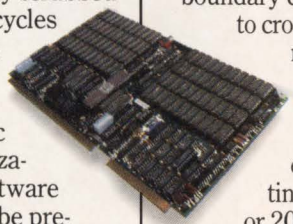
The new MCB-2X can relocate up to eight 64K or 256K blocks independently—making it a very powerful tool for "RAM disk," graphics display or multiple table look-up applications.



MCB-332

Expanded Error Correction Logic.

All single bit errors are automatically scrubbed during refresh cycles without system interruption. And thanks to the automatic memory initialization feature, software doesn't have to be pre-conditioned.



MCB-512

On-board ECC detects all single and double bit errors, while providing 370ns read access through standard 64K or 256K RAMs. Plus, the MCB-2X has CSR and ESR interrogation capability and software control of ECC enable/disable, allowing users to provide comprehensive system-level diagnostics.

Flexible Addressing Capabilities.

Board addresses starting on any 4K boundary can be mapped to cross 1 and 4 megabyte boundaries. The MCB-2X can also occupy a continuous 512K or 2048K memory space within its 16 megabyte range.

Look into ISI International's new MCB-2X. You'll find all the features you need... plus up to 2 megabytes of memory for the largest capacity available on a single card. Or, for non-volatile CMOS requirements, see our MCB-364 and MCB-332 modules. For simpler dynamic requirements, investigate our MCB-512.

Since 1970, ISI International has shipped over 10 billion bytes of memory cards, giving us a level of experience that's hard to match. Put it to work for you. For systems needs just call us in the West at (408) 743-4442, in the East (201) 272-3920, or in the Midwest call (513) 890-6450. For off-the-shelf products, contact your nearest ISI International distributor: Alliance, Anthem, Arrow, Future Electronics, R.A.E., Quality Components or Schweber.

*Multibus is a Trademark of Intel Corp.

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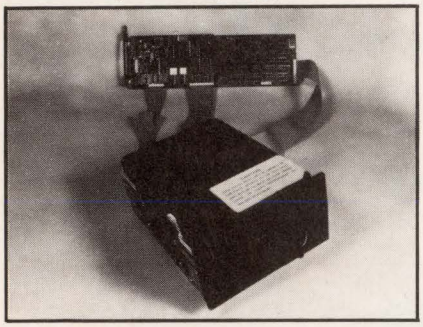
ISI International Corporation
1275 Hammerwood Avenue, Sunnyvale, CA 94089 • (408) 743-4443

CIRCLE 68

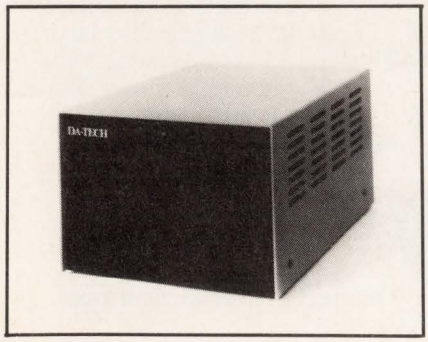
Conversion of PC to XT enabled by memory upgrade



The Gemini is an upgrade that converts a PC to an XT-type machine. Located internally and using available power, the system combines a 10-Mbyte, half-height hard disk drive and a half-height floppy disk drive. The Gemini comes with a SandStar floppy drive controller card and a hard disk controller module. It will also work with the SandStar hard disk controller card or memory card with hard disk controller modules. Features include 10-Mbyte formatted capacity, low power draw, MTBF of 14,000 h, and four-point shock mounting. **Maynard Electronics**, 430 Semoran Blvd, Casselberry, FL 32707. **Circle 280**

Floppy disk systems provide high level data file management

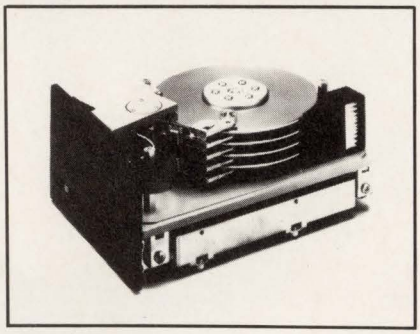
The 2000 series features 1600 Kbytes of storage and an RS-232-C interface. The standalone, file-oriented disk subsystems include two or more 5¼-in., 400-Kbyte floppy drives, disk controller, power supply, and interface. Onboard firmware uses CP/M structured commands, operations, and formats. Features include directory controlled file allocation, file and disk copy capability in the subsystem, 8 baud rates to 19.2 k, and optional current loop interface. Prices range from $2600 to $5500. **Da-Tech Corp**, 92 Steamwhistle Dr, Ivyland, PA 18974.



Circle 281

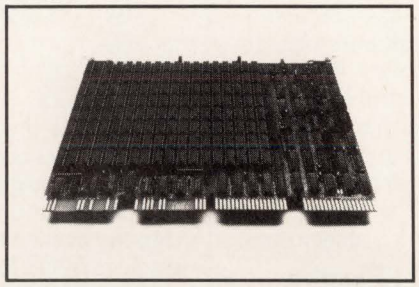
Winchester drives offer 85-Mbyte capacity

The 85-Mbyte V185 disk drive extends the V100 series of Winchesters. These models offer 30-ms average access times and incorporate standard ST412/ST506 interfaces. The V185 uses four platters. Increased capacity is achieved via higher track density and the use of the landing zone for recording data. Track density is increased from 960 tracks/in. to 1000 tracks/in. The drive's four metallic disks have a sputtered, hard carbon protective overcoat. Volume production should begin during the fourth quarter of this year at $695. **Vertex Peripherals**, 2150 Bering Dr, San Jose, CA 95131.



Circle 282

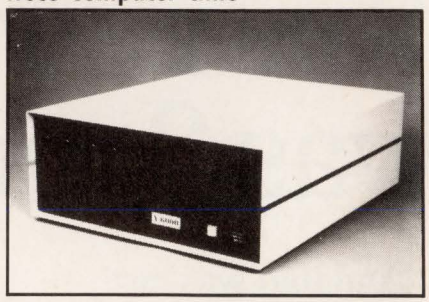
Memory modules aimed at Q-bus applications



The CI-1173 ranges in size from 128 Kbytes to 4 Mbytes on a single card. Access and cycle times are 130 and 300 ns, respectively. The memory is user configured to start and stop addresses on any 16-Kbyte boundary in the 0- to 4-Mbyte address range. Extended addressing allows expansion to 32-Mbyte memory. An onboard control status register, addressable at any of 16 reserved locations in the I/O map, gives instant status of the memory and exact location of any failing RAM. Single-quantity prices range from $1695 to $7995. **Chrislin Industries, Inc**, 31352 Via Colinas, Westlake Village, CA 91362.

Circle 283

Disk duplicator frees computer time

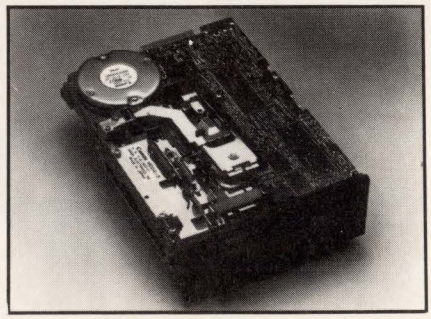


The Victory Duplicator produces 100 percent flawless copies. It will copy up to three disks at a time from an original diskette or up to four disks at a time from a built-in Winchester. An auto-feed option will be available soon for unattended operation. The unit has dozens of formats to choose from and will match the protocol of almost any current computer. The company will provide custom formatting, serializing, or copy-protection where required. **Victory Enterprises Technology, Inc**, 8910 Research Blvd, Austin, TX 78758.

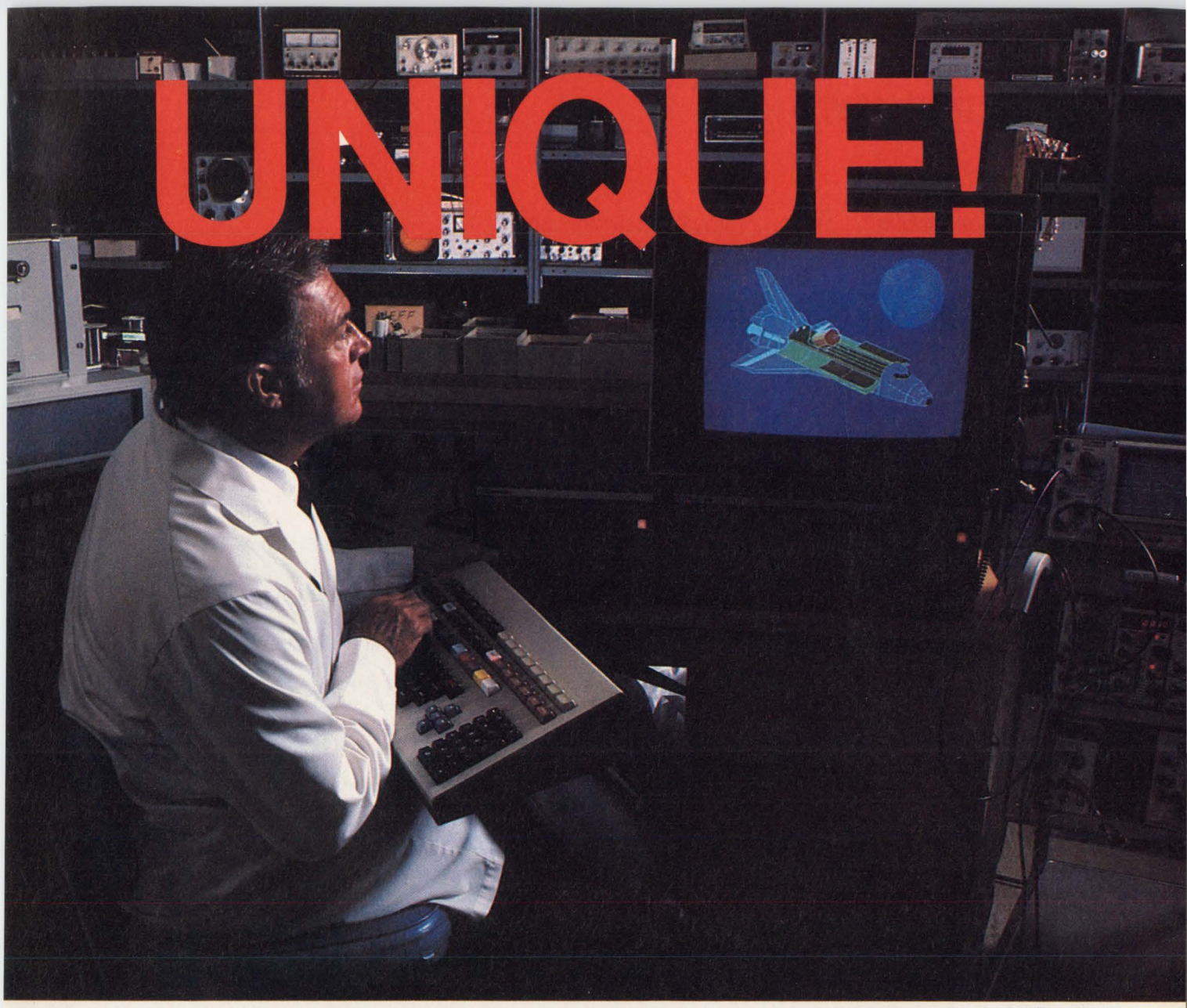
Circle 284

Disk drives offer 48- and 96-track/in. operation

The MDD413 and the MDD423 disk drives have a single drive motor for each disk with two stepping motors that enable independent disk access. The MDD413 is a low profile, dual 5¼-in. disk drive running at 48 tracks/in. with an unformatted capacity of ½ Mbyte per disk and a 1-Mbyte total. Track-to-track access time is 6 ms. The model MDD423, with 3 ms track-to-track access time, is a low profile dual 5¼-in. disk drive operating at 96 tracks/in. with an unformatted 1-Mbyte per disk capacity and a 2-Mbyte total. **Canon, U.S.A., Inc, Disk Drive Div**, One Canon Plaza, Lake Success, NY 11042.



Circle 285



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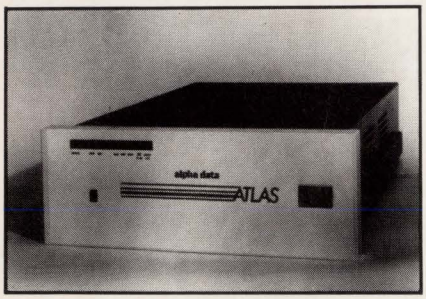
Fast disk drive contains 160 Mbytes of memory



With an average online access time of 18 ms under normal demand conditions, the Atlas disk drive incorporates 50 read/write heads on three platters. They can be stepped to a total of 160 cylinders or 8000 individual tracks. Each cylinder provides instant access to a full megabyte of data. The system is interfaces and format compatible with ANSI/SMD specs. The 50-head configuration reduces the amount of arm movement, accommodates more than 70 percent more user requests, and maintains acceptable response times even under high demand. **Alpha Data, Inc**, 20750 Marilla St, Chatsworth, CA 91311.
Circle 286

Increased capacity resides in half-height form factor

A 25-Mbyte, half-height drive is designated the 3425. The unit meets standard half-height dimensions and weighs 4 lb. It uses a two-disk, four-head design with 612 cylinders, track capacity of 10.4 Kbytes, and ST412 interface. In addition, the 3425 has an average access time of 85 ms, 14-W heat dissipation, and a head shipping zone in a nondata area. **MiniScribe Corp**, 1861 Lefthand Cir, Longmont, CO 80501.
Circle 287

Disk drives feature capacities up to 1 Mbyte

The two TM65 family models focus on portable and desktop applications. These 5¼-in., half-height flexible disk drives feature storage capacities up to 1 Mbyte. Model TM65-4 is a 96 track/in., double-sided drive that offers 1 Mbyte of storage. It features an onboard microprocessor that controls spindle speed, positions the heads to achieve minimum hysteresis, switches the write current for optimum recording quality, and provides a programmable ready signal. Track-to-track access time hits 3 ms. The TM65-2L is a 48-track/in., double-sided drive offering ½ Mbyte of storage and track-to-track access of 6 ms. The TM65-2L costs less than $125, while the TM65-4 is under $150. **Tandon Corp**, 20320 Prairie St, Chatsworth, CA 91311.
Circle 288

Universal memory board features 32-bit transfers

Designed for the VMEbus, the V-1612 offers 24 universal 28-pin memory sockets. Chip sizes can be configured at 2-K, 4-K, 8-K, 16-K, or 32-K x 8 bits. The board handles 8-, 16-, and 32-bit data transfers, and has jumper programmable DTACK delay. Features include write protection and power up/down protection for battery powered CMOS RAMs. Price is $695. **Ironics Inc**, 117 Eastern Heights Dr, PO Box 356, Ithaca, NY 14850.
Circle 289

DATA COMMUNICATIONS

Device offers low cost entry to packet switching network

The TX-700 series X.25 PAD is a multiple microprocessor-based packet assembler/disassembler. It assembles data for transmission over telephone lines and reassembles it at the receiving end of a network. The device can support data throughput of 160 packets/s. Each unit can concentrate up to 32 data channels, operating as fast as 9.6 kbits/s onto a single phone line. All data programming is done from a standard terminal connected to the system's supervisory port. Pricing starts at $1950. **ComDesign, Inc**, 751 S Kellogg Ave, Goleta, CA 93117.
Circle 290

Micro-to-mainframe SNA interface available in custom version

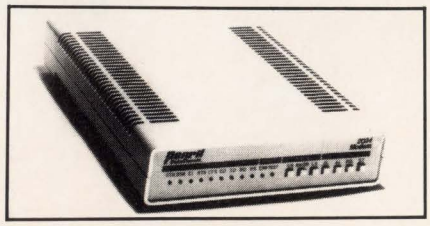
The NSA-SNA series is a family of flexible communication emulators allowing small computers to talk to mainframes. The emulators provide a multiprogramming environment on the PC. Thus, PC-DOS programs can run concurrently with the SNA emulator. The user can switch between the two tasks at will. Written in C, they are easily ported to other systems. System requirements are PC-DOS 2.0, 128 Kbytes of memory, and the IBM SDLC card. **Network Software Associates, Inc**, 19491 Sierra Soto, Irvine, CA 92715.
Circle 291

Fiber optic interface beefs up VAX and PDP-11 communications

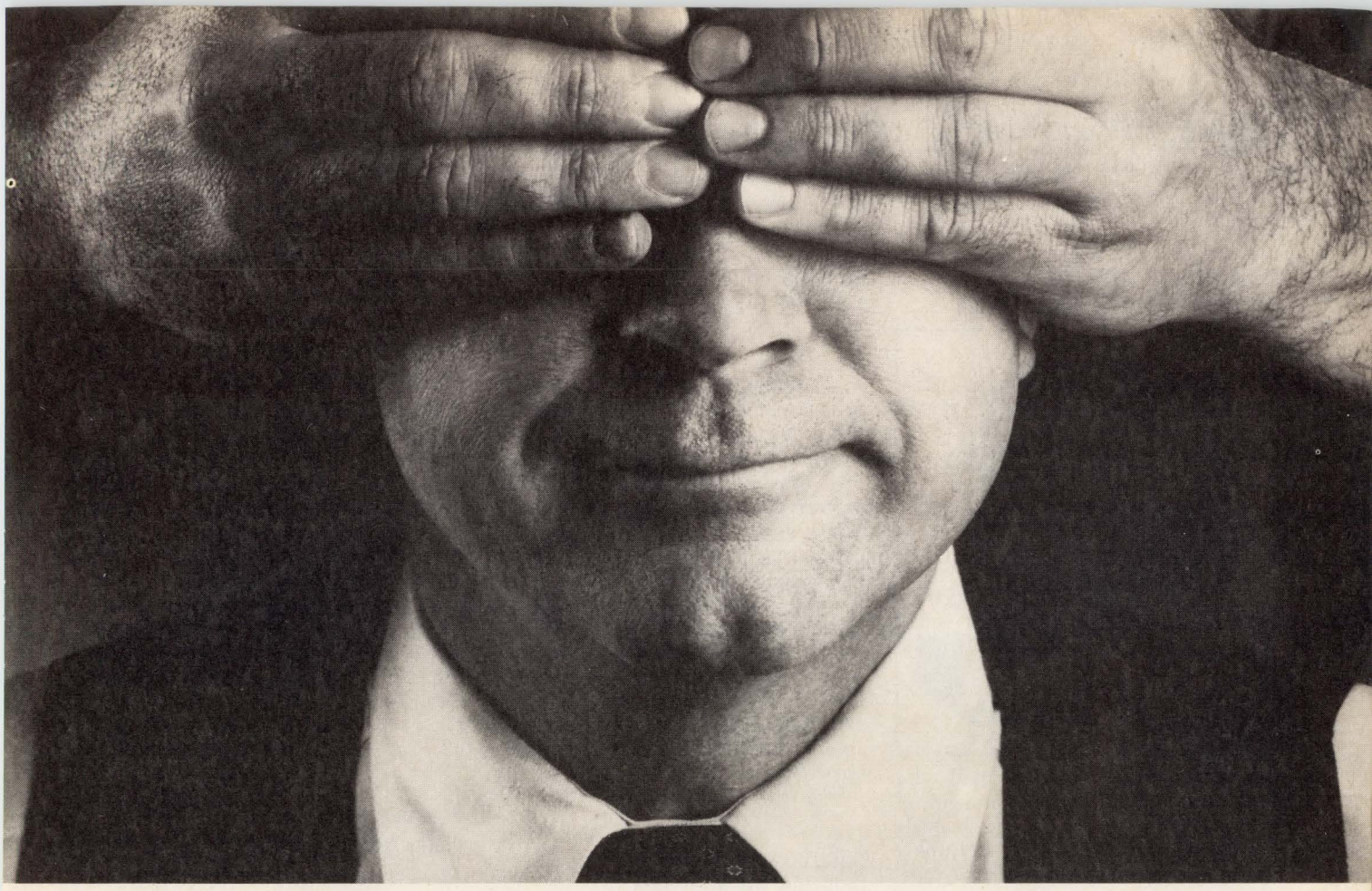
A high speed fiber optic modem, the DC100, sports compatibility with DEC VAX and PDP-11 machines, as well as DEC-compatible peripheral devices. The DC100 permits fiber optic interconnection of DR11-W and DR11-B interfaces at distances up to 3300 ft (1006 m.) The DC100 is a two-modem system. It converts the parallel DR11 interface to a 60-Mbit/s serial optical bit stream that is reconverted into parallel electrical signals at the far modem end. **Artel Communications Corp**, PO Box 100, West Side Station, Worcester, MA 01602. **Circle 292**

Full-duplex modem features adaptive equalizer

Communicating at 2.4 kbits/s, the 2024 modem operates in either asynchronous or synchronous mode and has an external switch that selects the data format. A 1.2-kbit/s rate is automatically adaptable in answer mode, and is switch selectable in call-origination mode. In asynchronous mode, character length can be 8, 9, 10, or 11 bits, including start and stop bits. Synchronous transmission permits clocking via modem internal clock, DTE external clock, or transmit clock slaved to the receive clock. The 2024 has a built-in autodialer and an automatic adaptive equalizer, which adjusts the 2024 receive circuitry for optimal data reception. **Penril, Data Communications Div**, 207 Perry Pkwy, Gaithersburg, MD 20877.



Circle 293



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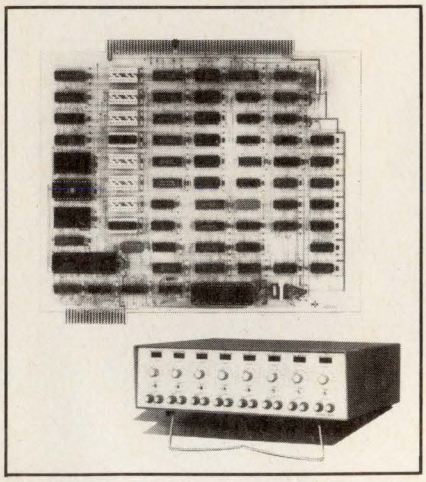
CIRCLE 70

Data output card allows realtime digitized data transfer



A data output card—called the SP800—provides full transfer of digitized realtime values from up to 16 channels (eight per card). This optional, microprocessor-controlled card is compatible with the ES1000B electrostatic chart recorder. Model 23-2101-23 transfers data unidirectionally to an external IEEE 488 controller (or other bus listener) and plugs into the SP800/3600 interface. The SP800 digitizes data from each input channel at a 10-kHz sample rate with 10-bit resolution. Through the card, the minimum and/or maximum of any channel's data can be transferred along a bus to the system controller. Price is $1200. **Gould Inc**, 3631 Perkins Ave, Cleveland, OH 44114. **Circle 294**

Network processor emulates DMF-32 controller operation

The System 207 network processor represents a Unibus interface network processor that emulates the asynchronous controller operation of the DEC DMF-32. Both character and DMA-mode output capabilities are included. Working with other DCA equipment, this device supports a remote terminal cluster. The System 207 consists of a single hex-sized circuit controller board that plugs into a Unibus small peripheral controller slot. It supports two point-to-point trunk links, each of which can communicate at rates of up to 19.2 kbits/s. Also, the System 207 supports up to 16 emulated DMF-32 controllers for up to 128 virtual circuit connections. Prices start at $4950. **Digital Communication Assoc, Inc**, 303 Technology Pk, Norcross, GA 30092.
Circle 295

Auto-dial modem has two-level security system

The AJ 1212-AD2 is a multispeed, synchronous/asynchronous modem compatible with Bell 212A and 103/113 operation. Speeds supported range from 0 to 300 bits/s. It can also operate as a 1.2-kbit/s modem. Sophisticated security features mark this auto-dial unit. The 1212-AD2 protects data at two independent levels. When an operator tries to access a protected field, the modem requests the security level and the appropriate password. It quickly checks protected passwords and log-on sequences. It also requires a second-level password before allowing access to the modem's memory. The device is priced at about $695. **Anderson Jacobson, Inc**, 521 Charcot Ave, San Jose, CA 95131.
Circle 296

Data bus transceiver improves bit error rate

The MIL-STD-1553 device, BUS-63104, is a form-fit-function replacement for CT3231 and is TTL compatible. The receiver section accepts Manchester phase-modulated bipolar data at the input and produces a biphase TTL signal at the output. The transmitter section accepts biphase TTL data at the input and produces a 30-V nominal peak to peak differential signal across a 145-Ω load. Measuring 32.0 x 32.0 x 5.1 mm and weighing 11 g, the device is packaged in a 24-pin square hybrid. Price is $295. **ILC Data Device Corp**, 105 Wilbur Pl, Bohemia, NY 11716.
Circle 297

Telecomm software enhances smart modem

Smartcomm II 2.0 software includes the Xmodem Protocol, VT52 and VT102/100 terminal emulation, and batch commands for auto-data transmission at specified times. The software protects passwords, tests the modem without going online, and lets users switch between voice and data. It includes a batch command set directory for storing up to 26 command sequences that automatically perform any Smartcom function. A macro security feature protects passwords and account numbers. Price is $149. **Hayes Microcomputer Products, Inc**, 5923 Peachtree Industrial Blvd, Norcross, GA 30092.
Circle 298

INTERFACE

Plug-in board provides text/graphics overlays for IBM PC

The PC-MicroKey System is offered at two levels. Level I is a low cost RGB only system, requiring a Sony KX series monitor or its equivalent. It sells for $900. Level II offers RGB plus NTSC composite video output. It can not only overlay the output of a video disc player, but also any video tape player, still-frame video tape, or camera. This combined display can be broadcasted and recorded for use in interactive training development. Level II is $1895. **Video Associates Labs, Inc**, 3933 Steck Ave, Austin, TX 78759.
Circle 299

Reduced parts count marks analog multiplexers

Two analog multiplexers—the DG526 and DG527—are compatible with TTL and CMOS devices. They perform 16-channel and dual 8-channel multiplexing, respectively. Combining analog switch and data latch functions on a single chip, these devices reduce interface hardware between the microprocessor system bus and the analog system under control. Available in 28-pin DIPS (plastic or ceramic), the DG526 and DG527 are priced from $11.37 to $27.93 (depending on package and grade specified) in lots of 100. **Siliconix, Inc**, 2201 Laurel Rd, Santa Clara, CA 95054. **Circle 300**

Dichroic LCD driver chip enhances display contrast and viewing angle

The S4520 dichroic LCD driver chip can supply 30 V, providing wider viewing angle and high color contrast for displays. Operating from a logic supply of 4 to 16 V and a display supply as low as −29 V, this CMOS device allows drive voltage swing of up to 32 V, while drawing as little as 400-μA current. An onchip oscillator generates the ac backplane signal, with the frequency determined by an external resistor and capacitor. Users can bypass the internal oscillator with an externally generated backplane signal. Plastic DIP S4520S are $12.60 each in quantities of 1000, or $22.85 for ceramic leadless chip carriers. **Gould AMI Semiconductors**, 3800 Homestead Rd, Santa Clara, CA 95051.
Circle 301

Integrated manufacturing system adds two interfaces

Information can be passed directly from semiconductor fabrication equipment to the CTX4000 data base with two interfaces. The first, the Interface Manager, provides an enhanced operating system environment for running CTX interfaces. It allows starting, stopping, and monitoring of up to eight interface tasks running on a CTX4000 task processor or series 1000 data concentrator. The second, the CTX Xincom interface, provides for data capture directly from the Xincom 5540. It allows data from the Xincom to be reformatted and transferred to the CTX4000 data base. Interface Manager price is $2000; the Xincom interface costs $15,000. **CTX International**, 575 N Pastoria Ave, Sunnyvale, CA 94086.
Circle 302

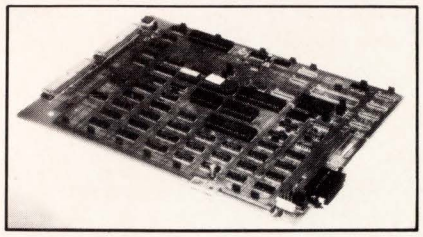
Hard disk controller fits 3½-in. form factor

The DJ210 connects micros that use SASI or Konan DJ interfaces to ST-506/412 Winchesters. The 124-pin chip performs the entire set of disk drive controller functions with the exceptions of the firmware, processor, drivers, receivers, and data clock separator. The chip does control the bus, 256- or 512-byte state machine, CPU control, I/O decode, I/O registers, data conversion, RAM control, shift register, and error correction, among others. Price, in quantity, is $150 each. **Konan Corp**, 1456 N 27th Ave, Phoenix, AZ 85009.
Circle 303

Power line current transceiver handles 16 BSR X10 house codes

The 410 model is a microprocessor power line current carrier transceiver. This device resides on a standalone 4½- x 6-in. (115- x 152-mm) card containing a Z8 microprocessor. BSR modules need not be ganged together for multichannel control because the 410's two-way transmission feature provides confirmation that commands are properly received. The 410 can transmit and receive any of 16 house codes used by the BSR X10 system, simply by setting DIP switches. It is also field selectable for either of two I/O configurations. A model 420 represents an RS-232 version that can handle 256 channels and 96 commands. **Hydrus Corp**, 6218 Cedar Springs, Dallas, TX 75235.
Circle 304

Interface links half-inch tape transports with computers



Designed to couple RS-232 serial data to half-inch tape drives, model IN-210 serial communication interfaces support both asynchronous and synchronous protocols and operate in remotely or locally programmable modes. Most standard baud rates are selectable up to 28.8 kbaud. The IN-210 interface is packaged on a 10- x 13- x 0.5-in. (25.4- x 33- x 1.2-cm) PC card. It requires 5 V at 2.5 A and 12 V at 100 mA. Operational temperature range is 0 to 50°C. The IN-210 sells for $1360 in quantities of 100. **Telebyte Technology Inc**, 148 New York Ave, Halesite, NY 11743. **Circle 305**

Sixteen shades of gray are available with upgrade

The Grayscaler converter upgrades an IBM or compatible color graphics card to full gray scale operation. It provides 16 distinct brightness levels of composite video. Driven from the RGB port, this adapter delivers RGB crispness to green, white, or amber screen monitors. The Grayscaler generates a distinct brightness level for every color and eliminates color grain found when operating directly from the color card. The Grayscaler costs $59.95. **Avocado Computer**, 17352 Yorkshire Ave, Yorba Linda, CA 92686.
Circle 306

Analog ouput board supplies two channels for the IBM PC

The DAC-02 allows direct connection to four 20-mA proportional control valves and other output devices. The board contains two double buffered 12-bit D-A converters plus interface circuitry with output ranges of ±10 V, ±5 V, 10 V, and 5 V. The D-A converters are also multiplying D-A converters for ac measurements and resolver/synchro conversion applications. All connections are made via a 25-pin female D connector located at the rear of the PC. Price is $240. **MetraByte Corp**, 254 Tosca Dr, Stoughton, MA 02072.
Circle 307

Intelligent disk controllers offer additional features

Three enhancements for the 8890 Sybercache include: up to 18 Mbytes of cache memory, an 8-channel switch, and a dual-frame configuration that combines two units. The 18-Mbyte memory, a field installable option, supports the 8380, 8350, 8360, and 8650 drives. The switch feature allows eight channels to be connected to the unit so the controller can be shared by multiple processors. The dual-frame option lets one controller take over for another during a power interruption. **Storage Technology Corp**, 2270 S 88th St, Louisville, CO 80028.
Circle 308

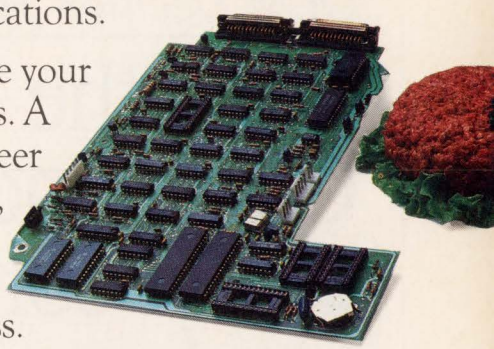
Low cost CRT controller is STD bus compatible

The ANC-7345H provides a completely programmable character display format and a user alterable 256-char font. The font includes ASCII chars, upper/lower case, and semigraphics. The independent, memory mapped, 1024-char controller has cursor control and hardware scrolling, as well as character by character inverse video. RS-170 level composite video is available at the rear mounted 10-pin ribbon connector. In addition, 12 V can be obtained from this connector to power the video display. Cost is $119. **Antona Corp**, 13600 Ventura Blvd, Sherman Oaks, CA 91423.
Circle 309

Comm controller board furnishes eight channels

Featuring the 80186 CPU, the Am96/3500 intelligent interface board can operate as a slave controller or bus master. It relieves the system CPU and software of the overhead associated with serial I/O service, allowing higher data rates for Multibus compatible systems. It has eight channels based on the Z8530 serial comm controllers and is compatible with RS-323-C and RS-423 protocols. The board is software selectable for asynchronous operation at up to 76.8-kbaud, and for higher synchronous rates. With asynchronous operation at up to 38.4 kbaud, price is $2795 each in quantities one to nine. **Advanced Micro Devices, Inc**, 901 Thompson Pl, PO Box 3453, Sunnyvale, CA 94088.
Circle 310

Qume can give your system extra appeal—with terminals made to order to your exact specifications.



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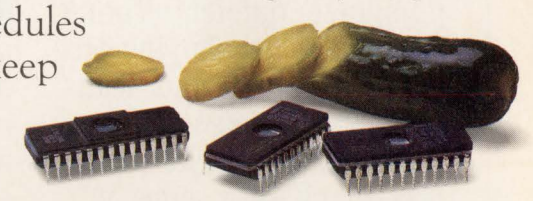

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CIRCLE 72

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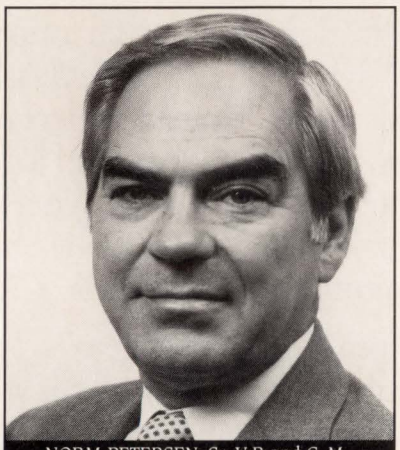

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CIRCLE 73

Cached disk controller enhanced with firmware

Firmware for the ASC-525 cached disk controller allows it to run in Unix and multi-user environments. It complements the 320-Kbyte, onboard cache and is a full implementation of the SCSI bus interface. Simultaneous SCSI data transfers from cache and overlapped disk seeks on all supported drives increases the SCSI bus bandwidth. With a high hit ratio, disk access time can be reduced from 85 to under 10 ms. The unit is $1995 and fits the 5¼-in. form factor. **Advanced Storage Concepts, Inc**, 9660 Hillcroft, Houston, TX 77096.

Circle 311

Two I/O modules are available for data acquisition systems

The 32-bit, Unix-based MC-500 system now has a SC-16F 16-channel conditioning module and a TC-16F thermocouple input module. The signal conditioning module contains 16 independent differential input instrumentation amps for use with low level sources, current loop interfaces, and bridge type transducers. The thermocouple module contains 16 independent amps for use with J, K, S, or T thermocouples. Cold junction compensation is provided. Each module costs $2500. **Masscomp**, One Technology Pk, Westford, MA 01886.

Circle 313

Add-on board turns IBM PC into realtime multitasking computer

Called the RC/VRTX, the board concurrently manages and processes all tasks associated with the execution and performance of the user's application programs. It supports the DOS operating system concurrently with its realtime operating system, allowing access to BIOS functions. The board requires about 250 μs to switch from one task to another. Dedicated memory space stores the specific parameters for location, size, and status of each task. Cost is $1495. **Dyad Technology Corp**, 4040-G Sorrento Valley Blvd, San Diego, CA 92121.

Circle 315

Address extension module supports the 11/73 processor

Compatible with the Q-bus, the MSC 8904 can combine 18- and 22-bit controllers with a 22-bit memory bus to configure systems with 4-Mbyte memory and 18-bit peripherals. The hex-wide board translates 18-bit addresses to 22-bit ones. A subsystem version includes the PAE module, a power sequence/line, time clock module, backplane, and 300-W power supply with fans. The module is $1600, the backplane is $850, and the subsystem is $5300. **Monolithic Systems Corp**, 84 Inverness Cir E, Englewood, CO 80112.

Circle 312

Long distance channel extender handles IBM mainframe peripherals

The model MBX-T101 provides block multiplexer channel communications at 1.544 Mbits/s over distances of more than 25 mi. The extender is transparent to host software and allows placement of plotters, laser printers, and other output devices. Compatible with Bell T1 carrier digital communication circuits, this channel extender requires no procedural changes, additional programming, or software modification. **Megabit Communications, Inc**, 90 West County Rd C, St Paul, MN 55117.

Circle 314

Printer adapter provides interface for IEEE 488 devices

The GPAD-C allows printers with a Centronics interface to connect to any computer or controller with an IEEE 488 (GPIB) interface. The GPIB address is selected by a five-position DIP switch. No special software is required. Without cables the GPAD-C measures 3.5 x 5.75 in. (8.9 x 14.6 cm). Two cables and a power supply are included. The cables allow 6 ft between the printer and the GPIB connection. The printer adapter costs $179. **Connecticut microComputer**, 150 Pocono Rd, Brookfield, CT 06804.

Circle 316

SOFTWARE

Second-generation design language handles diverse target devices

The CUPL design language for programmable logic enters its second generation with CUPL Version 2. Version 2 lets the designer describe logic in any of three ways: state diagrams, Boolean equations, or function tables. State machine coverage includes D, JK, and RS flipflops. The language runs on CP/M and MS/DOS-based PCs as well as Unix systems. It automatically converts design logic descriptions into the appropriate fuse pattern data for the target device. CUPL 2.0 is available for $895. **Assisted Technology**, 2381 Zanker Rd, San Jose, CA 95131.

Circle 317

Geometric transformation power gained by image processor

Fast Image Warp is a software program added to the Trapix series of realtime image processing systems. It is a general, "6 degrees of freedom," geometric transformer that includes image warp, image rotation, and continuous image magnification and reduction. Modular design allows warping of subimages with user-specified dimensions, and of whole images up to 1024- x 1024- x 32-bit pixels. Execution time for the package is about 1 s for a 512 x 512 array. Fast Image Warp costs $1200. **Recognition Concepts, Inc**, PO Box 8510, Incline Village, NV 89450.

Circle 318

Fortran-77 now runs under the RT-11 operating system

A PDP-11 Fortran-77 implementation is targeted for RT-11 users, with applications in the development and execution of analytical programs. The compiler will run under Version 5 or 5.1 of RT-11 on any PDP-11 or Professional 300 configuration with 48 Kbytes of user memory, 1 Mbyte of available disk space, and an FPP Features include the support of precision and complex arithmetic, virtual arrays, encode/decode statements, formatted and unformatted sequential and direct access I/O, and runtime formatting. Price is $950. **Digital Equipment Corp**, 10 Main St, Maynard, MA 01754.

Circle 319

System/370 processors gain Lisp capabilities

A version of Lisp includes Virtual Machine (VM) capability and runs on the IBM System/370 processor line. It provides tools to ease creation, debugging, maintenance, and execution of Lisp programs. The product is interactive and display oriented. Known as Lisp/VM, the system lets users observe an executing program and specify, as each semantic unit is reached, what debugging information should be displayed. Lisp/VM consists of a programming language and development environment. Lisp/VM programs and data are accessed through the system editor, or through the VM/SP editor. The product is available for a $6500 one-time license fee. **IBM**, Dept 68Y PO Box 152750, Irving, TX 75015.
Circle 320

Programmer's workbench tools aid software development

Dubbed the software development environment (SDE), this collection of tools eases program writing. SDE tools generate test data and programs, provide control for auditing purposes, and merge, rearrange, and reformat files. An SDE training course, online help, and a library storage facility are provided. Within SDE, an access manager (which handles SDE file security) controls file access. License for the program is available for $265 per month. **NCR Corp**, Dayton, OH 45479.
Circle 321

Programming accelerated with preprogrammed C language functions

Preprogrammed C language functions and subassemblies, dubbed C-Power Packs, save programming time and simplify debugging. They feature six libraries of preprogrammed functions and subassemblies that easily integrate into software to enhance code uniformity. The more than 600 functions can be mixed and matched. Interfacing with DOS 2.0 and earlier DOS versions, C-Power Packs include code for communications, mathematics, utilities, as well as database and building block functions. Operation is on Microsoft and Lattic C compilers, and assorted PC-compatible devices. C-Power Packs are priced from $99. **Software Horizons, Inc**, 165 Bedford St, Burlington, MA 01803.
Circle 322

Signal processing software available for the IBM PC

A compatible subset of the ILS software runs on the PC and XT. Called the ILS-PC 1, it offers over 30 integrated programs for data acquisition support, waveform display and editing, digital filtering, and spectral analysis. Data aquisition includes support of A-D and D-A hardware; waveform features include graphical display (single or multichannel) and cursor editing of signals. It requires 256 Kbytes of memory and a graphics board running DOS 2.1. An 8087 is recommended for running the software at close to minicomputer speed. License fee is $1495. **Signal Technology, Inc**, 5951 Encina Rd, Goleta, CA 93117.
Circle 323

Software moves programs between micros, minis, and mainframes

The 2.0 release of the Network DataMover software includes features for full partitioned data and library support, remote unattended operation, and improved security and audit capability. The software lets the user manipulate data or programs via menus from a personal computer, instead of a mainframe. It runs on the MVS mainframe operating system and moves data throughout the network. Applications can be as diverse as Cobol or Lotus programs. **Systems Center**, 2988 Campus Dr, San Mateo, CA 94403.
Circle 324

Multilingual word processor mixes languages in one document

The ML.WP word processing package offers standard word processing features and accepts any language or combination of languages. The system displays help messages, prompts, error messages, and other interfaces in the user's choice of languages, and can accommodate left-to-right and right-to-left languages on the same line. The software is available on VAX systems to support single or multiple user systems. **Compulex, Inc**, 188 Middle St, Lowell, MA 01852. **Circle 325**

Let's hear from you
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INTEGRATED CIRCUITS

Modem chip set provides token-passing performance

The NE5080 high speed FSK modem transmitter and NE5081 receiver offers phase continuous modulation and demodulation of a digital bit stream in various architectures. The chip set conforms to the IEEE 802.4 standard, yet permits the designer to tailor performance in data rate, carrier frequency, and cable type. Carrier frequency is adjustable between 50 kHz and 20 MHz. A modem built with this set offers a range exceeding 30 dB. Price for each chip in the set is $15.50 in 1000s. **Signetics Corp**, 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086.
Circle 326

Floating point chip set achieves high speed and precision

Offering 2 to 8 megaflop performance, the WTL 1064 and 1065 handle single (32-bit and double (64-bit) precision formats, while taking care of 32-bit two's complement integers. The array flowthrough time for the WTL 1064 is under 360 ns for single precision multiply and 600 ns for double precision. The array can be divided into stages separated by pipeline registers so that an operation can begin before a previous operation is finished. With 2-micron NMOS technology, the devices dissipate 2 W typical and measure approximately 300 mils on a side. They are housed in standard 144-pin grid array packages. **Weitek**, 501 Mercury Dr, Sunnyvale, CA 94086.
Circle 327

Universal disk controller combines hard disk, floppy, and tape features

The HDC 9224 offers transparent error detection and correction, programmable automatic retry option, precompenstation logic, and 24-bit DMA controller. Detection and correction of disk data errors occurs with no micro intervention or interrupt servicing requirements. It interfaces to ST506-compatible hard disk drives with as many as 16 surfaces/drive. Flexible format command allows the user to select hard disk sector sizes of up to 16 Kbytes in length. The chip can control both streaming and start-stop tape drives. **Standard Microsystems**, 35 Marcus Blvd, Hauppauge, NY 11788.
Circle 328

Universal digital loop transceivers combine data and voice

The MC145422 and MC145426 are universal digital loop transceivers (UDLTs) that can combine digital and voice band communications. These devices move data over digital PBXs using twisted-pair wire, transmitting and receiving voice data at 64 kbits/s and signaling data at 16 kbits/s. With two operating modes—master and slave—they consist of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and Tx and Rx data registers. They operate on a single, 5- to 8-V supply, and can be driven by TTL or CMOS logic. Production quantities are planned for the fourth quarter, with a 1000-piece price of $20.23 for the 422 and $18.95 for the 426. **Motorola Inc, Logic and Special Functions Products Div**, 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 329

Nonvolatile 256-bit memory has onchip voltage generator

A 256-bit serial EEPROM chip is dubbed the NCR 59306. This 16- x 16-bit device uses a single 5-V power supply. An onchip voltage generator allows programming without the need for external high voltage supplies. In standby mode, power consumption is only 25 mW. Fabricated with the firm's n-channel silicon-nitride-oxide-silicon process, the NCR 59306 is pin compatible with the NMC9306 from National Semiconductor. Other characteristics include a 500-kHz clock rate, TTL compatibility, and eight-pin DIP. The price is $4.52 each in quantities of 100. **NCR Microelectronics Div, Product Marketing**, 8181 Byers Rd, Miamisburg, OH 45342.

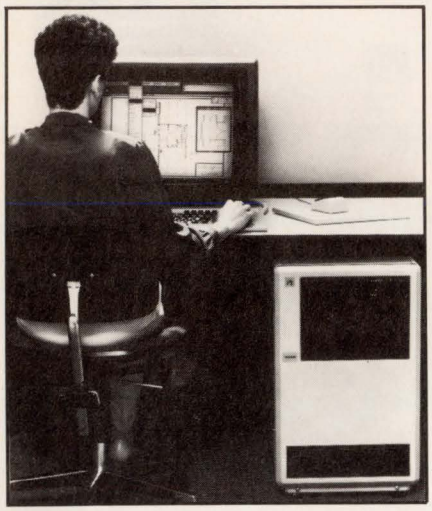
Circle 330

Quad op amp is plug-compatible with industry standard devices

LT1014, a 14-pin DIP, is compatible with the LM124, LM148, OP-11, and RC4156. The LT1013 is packaged in an 8-pin mini DIP and in TO-5 configurations and is compatible with the MC1458 and LM158. The LT1014 has a maximum offset voltage of 180 mV, maximum drift is 2 μV/°C, and it has 0.8 nA maximum offset current. It delivers more than 20 mA load current with no crossover distortion while dissipating less than 500 μA per amp. In 100s, the devices are priced between $2.95 and $5.35. **Linear Technology Corp**, 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle 331

Management projects run on Formtek workstations as well as PC/XT



The Facilities Management System enables automated planning and design of facility projects. The package runs on both Formtek workstations and IBM PC/XT microcomputers. A key feature is space programming, which manages spatial standards and determines building or layout program. Other features include spatial stacking, which provides evaluated alternatives, and allocates different functions or departments to different floors of multifloor buildings; and space projections, which assesses different growth scenarios of layout alternatives. **Formative Technologies Inc**, 5001 Baum Blvd, Pittsburgh, PA 15213.
Circle 332

Turbo Pascal made easy with Toolbox programming aid

Where search and sort capabilities are important, programmers writing software in Pascal can use the Turbo Toolbox to save time. Designed to complement the Turbo Pascal compiler for Z80 and 8088/8086 systems, Turbo Toolbox offers solutions to basic programming tasks. In the Toolbox are tools such as Turbo-ISAM on a disk, Quicksort, and the GINST (general installation program)—which is a terminal installation module that automatically gets Turbo Pascal programs up and running on Z80- and 8088/8086-based microcomputers. The package allows users to access file records on key searches. With this feature, direct access is available to records in a sorted sequence. Price is $49.95. **Borland International**, 4113 Scotts Valley Dr, Scotts Valley, CA 95066.
Circle 333

Level/noise/frequency test set comes in compact package

The LNF-3 test set measures noise, level, and frequency. It measures transmission traits of VF lines in accord with BSTR41009. Control of 829 loopback sets is provided by a 2.7-kHz loopback tone controlled by a momentary action switch. Designed to mount in a 19-in (48.2-cm) relay rack, the LNF-3 takes up only 1.75 in. (4.4 cm) of vertical space. The unit contains an audible monitor, a variable fixed signal generator, dual level and frequency display; plus auto-ranging digital readout. **Atlantic Research Corp**, 5390 Cherokee Ave, Alexandria, VA 22314.
Circle 334

Design tool family expands with PC-based workstation

Simulog logic simulator and Symgraph schematic capture system provide designers with tools for logic design and verification. Simulog is a nine-state, event driven device with a set of 20 logic primitives. Both TTL and MOS circuits can be simulated. It displays the state of the logic signals as waveforms in color on the high resolution workstations. Symgraph allows logic designs to be entered as multiple sheet schematic diagrams and to extract a netlist for simulation. Simulog is $2500 per copy, while Symgraph is an integral part of the graphics subsystem. **Chancellor Computer Corp**, 1101 San Antonio Rd, Mountain View, CA 94043.
Circle 335

Workstation meets needs of analog design engineering

The Analog Workbench is a standalone for the analog circuit designer. It consists of a 32-bit computer, mass storage, display, and software. The product features a menu-driven scheme and mouse pointer. A circuit can be modified (for example, the value of a collector resistor can be changed from 50 to 100 Ω), and the effect on the rest of the circuit quickly analyzed. Three setups are provided: a time-domain setup, with multichannel function generator and multichannel oscilloscope; a frequency-domain setup, with sweeper and multichannel network analyzer; and a dc setup with dc multimeter. A compiler for the C language is included. Workbench price is $74,800. **Analog Design Tools Inc**, 800 Menlo Ave, Menlo Park, CA 94025.
Circle 336

Logic analyzer combines with microcomputer

A logic analyzer capable of timing, state, and signature analysis integrates with a CP/M microcomputer to form the Omni 4. Housed in a rugged 27-lb package, the Omni 4 can collect 1000 data samples on each of 16 channels or 500 samples on up to 32 channels. Four channels of glitch detection are provided with a minimum detectable pulse of 10 ns. The system uses qualifiable internal or external clocks as fast as 20 MHz. The CP/M computer uses a Z80A CPU and 64 Kbytes of RAM. Two 5 ¼-in. disk drives provide 760 Kbytes of storage. The Omni 4 is priced at $4495. **OmniLogic, Inc**, 350 Sunset Blvd N, Renton, WA 98055.
Circle 337

Portable standalone emulators designed for 8- and 16-bit micros

The Sophia SA700 is a family of compact emulators that provide full symbolic debugging capability—independent of the host development system. The emulators are self-contained with a CRT, ASCII keyboard, 8-in. floppy drive, PROM programmer, logic state analysis probes, and an in-circuit emulator. Programs to be debugged can be entered directly from the floppy, which can directly read executable object files from Intel's MDS series II and III, iRMX-86, CP/M-86, and CP/M 2.2. The systems are priced at less than $10,000. **Sophia Computer Systems**, 3337 Kifer Rd, Santa Clara, CA 95051.
Circle 338

Graphics software release increases system speed

A hardware and software combo for Telesis engineering design workstations increases system speed by two to six times. Addition of a high resolution monitor, expanded pixel memory, filled line graphics, dynamic rubberbanding, plus color priority and blank-by-color capabilities enhance system performance. A 2000- x 2000-pixel memory plane option equips the graphics processor with roam and zoom functions that are free of flicker. The 50 Hz, noninterlaced monitor has a 1000- x 900-pixel count. Blank-by-color lets the user remove a class of items designated by color. **Telesis Systems Corp**, 21 Alpha Rd, Chelmsford, MA 01824.
Circle 339

Package for CAD is computer independent

Super-CADS is 3-D full-function software for the IBM XT, VAX, and ELXSI. Features include dynamic interactive menus and relational database support. The data base stores design data and generates reports and interactive queries. The mechanical software has more than 1000 commands in construction primitives and unlimited viewing in 3-D space. Scaling is from 1 to 1 million. Six standard orthographic views, a standard isometric view, and some user-defined views are available. **Tasvir Corp**, 2490 Charleston Rd, Mountain View, CA 94043. **Circle 340**

Bit-map color graphics station shows true memory device topology

With the capacity to display 1 Mbit of data simultaneously on the 19-in. high resolution color moniotr, this portable station is designed for testing semiconductor memories. Bit manipulation capabilities are accessible through keyboard and joystick controls. The system stores up to 8 planes of 1 Mbit each and, when coupled with the choice of 256 colors, allows single-level or composite bit-map display. It can also zoom and pan individual segments of the device. Used in conjunction with the Q2/52 memory test system, it is priced at $60,000. **Megatest Corp**, 1321 Ridder Park Dr, San Jose, CA 95131. **Circle 341**

Prolog and programming tools run on DECsystems 10/20

Based on the high level logic programming language Prolog, Dec-10/20 Prolog is aimed at development work in advanced applications. It consists of an incremental compiler, an interpreter, and a runtime and debugging system. It runs under TOPS10 and TOPS20. Also included is a library of public domain utilities such as a natural language geography query program called CHAT. License is $10,000 per CPU. It is distributed on a nine-track, 1600 bit/in. TOPS20 dumper format mag tape and includes documentation. **Quintus Computer Systems Inc**, 2345 Yale St, Palo Alto, CA 94306. **Circle 342**

Let's hear from you

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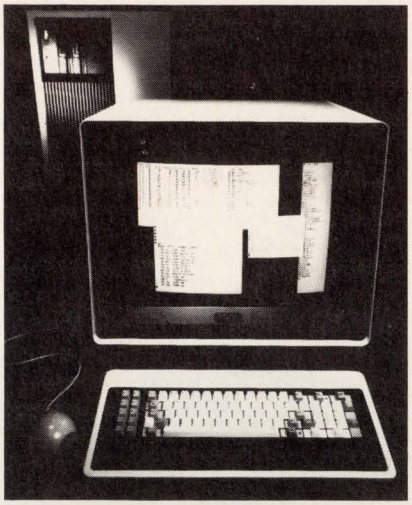
Graphics workstation combines multi-user Unix with high resolution



Graphics workstations in the 80/G line match Unix with a graphics processor and an ultrahigh resolution raster-scan display. Aimed at graphic design, document composition, scientific modeling and CAE, the machine's display resolution lists at 200 lines/in. (2180 x 1728 pixels) with the 15-in. portrait mode, and 150 lines/in. (2304 x 1728 pixels) with the 19-in. landscape mode. High resolution interactive composition is supported by a writing speed of less than 0.5 s. The unit is designed around the 68000 processor. **Pixel Computer Inc**, 260 Fordham Rd, Wilmington, MA 01887. **Circle 343**

Schematic designer allows fast product turnaround

The Dash-2 schematic designer adds mouse-driven editing features to the Dash-1. Dash-2 capabilities include Tag and Drag, which enables the user to pick a symbol, drawing area, or alphanumeric field and then drag the targeted selection across the screen; Snap, which allows the user to position a cursor in the vicinity of a pin and "snap" the connection in place; and Realtime Orthogonal Rubberbanding, in which all connecting lines move as symbols or areas move. Three zoom levels and onscreen help further enhance operation. The Dash-2 for the PC/XT costs $6280 for the add-on package, and $12,980 for a whole system. Upgrades for Dash-1 systems cost $250. Dash-1 packages now cost $600 less than corresponding Dash-2 models. **FutureNet**, 6709 Independence Ave, Canoga Park, CA 91303. **Circle 344**

System supports three users for CAD applications

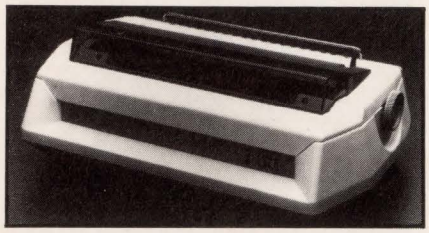
Designer V-X series M represents a multiuser, multi-application system for CAD/CAM. Series M supports four 300-Mbyte disk drives along with a standard system 300-Mbyte disk. It also supports CADDS 4X software, which can be used for applications such as electronic and mechanical design and drafting. The system manages three interactive users simultaneously and is compatible with systems including the Series V-X (which can be upgraded to Designer M operation) and CDS 4000. Basic system is approximately $250,000 with a CGP 200 X processor, CADDS 4X software, one 300-Mbyte disk, tape drive, two high resolution color graphic terminals, and an application pack. **Computervision Corp**, 100 Crosby Dr, Bedford, MA 01730. **Circle 345**

Channel simulator tests systems including IBM 360 and 370

The Channel Simulator is a testing device that simulates standard I/O operation on IBM 360, 370, 4XXX, or 30XX systems. Testing can be completed from one location in both the automatic and manual modes. A built-in modem connection allows remote testing. Interactive manual mode gives the user realtime logical control of the IBM bus and tag line levels, so a user can single-step through an interface or command sequence. The unit is packaged in an aluminum flight case. **Comcheck International, Inc**, 8711 E Pinnacle Peak Rd, Scottsdale, AZ 85255.

Circle 346

Daisywheel printer runs at quiet 55 dB

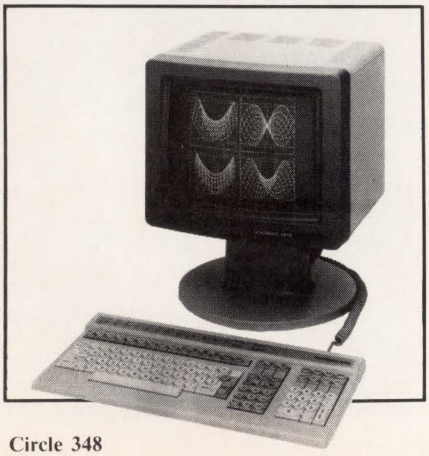


Featuring a reliable hammer assembly, improved motion control systems, and acoustic mufflers, the M45 QuietWrite offers a choice of eight different interchangeable interface modules. Bidirectional printing occurs at 45 chars/s on average English text. Interfaces include RS-232 with current loop, Centronics, Dataproducts, IEEE, HP, Qume Sprint3, and IBM systems 34, 38, and 5200. The multistrike ribbon is driven by a separate motor to optimize ribbon life. **Daisy Systems Holland BV**, 279 Nieuweweg, PO Box 125, 6600 AC Wijchen, The Netherlands.

Circle 347

Bit-mapped raster graphics enhance terminal alphanumerics

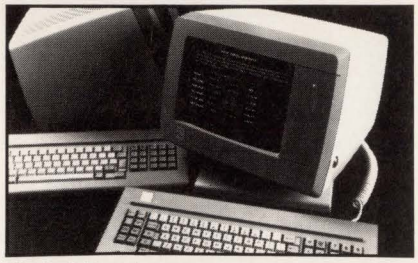
A plug-in board option transforms the 2200S terminals into a direct bit-mapped raster graphics system with 720 x 336 view area. In enhanced alpha/graphics mode, the 2200S will generate characters from up to eight character sets. In a vector mode, primitive graphics are produced as solid or dot/dash lines. In point and interactive graphics modes, the unit emulates the Tektronix 4010. The 2200S features a 70-Hz refresh rate, can be equipped with up to 56 Kbytes of memory, and can transmit by character, page, block, or line/field. The terminal costs $1395, with an optional graphics board at $729. **Tandberg Data, Inc**, PO Box 99, Labriola Ct, Armonk, NY 10504.



Circle 348

Ergonomic display family designed for IBM 3270 users

The displays include a low cost 12-in. monochrome version, model 078, and a color model, the 079. Both models are plug compatible with IBM's 3178 and 3179, respectively. They feature a two-piece, low profile design with tilt and swivel capabilities; and a coil cable, adjustable keyboard. Both display 1920 chars and attach directly to either the 3274/3276 controller or the Telex 174/274C/276 control unit. The 078 is priced at $1550, including a choice of keyboards with a numeric or program function pad. The 079 is $2195. **Telex Computer Products, Inc**, 6422 E 41st St, Tulsa, OK 74135.



Circle 349

High density monochrome displays incorporate switching power supply

Series HF monochrome displays come in 15-, 17-, and 20-in. sizes. They operate in noninterlaced mode for a flicker-free display. Video bandwidth is set at 80 MHz. MTBF is specified, according to MIL-217-C, at 12,500 h. Series HF displays incorporate a switching mode power supply that reduces unit weight. Input voltage can vary from 85 to 133 Vac or 47 to 63 Hz, without degradation of performance. A field-selectable strap sets the displays for 168- to 265-V operation. The HF series also incorporates a regulated high voltage supply for stable dynamic graphic display. **Ball Corp, Electronic Systems Div**, PO Box 43376, St Paul, MN 55164.

Circle 350

Magnetic nonimpact unit represents downsized version of MP 6090

Resolution of 240 x 240 dots/in. and speed of 50 pages/min are achieved on the MP 6050. Using proprietary perpendicular magnetographic technology, this unit sports an MTBF rate set at 1 million pages. Typical monthly print output of the MP 6050 exceeds 300,000 pages. Basic model with logic architecture includes a video interface and a power stacker. It also allows operator- and host-selectable densities, and its interface is monodirectional on a character line transfer basis. This unit is a downsized version of the MP 6090. Options include four additional sets of 96 chars and a vertical format unit tape reader. **Cynthia Peripheral Corp**, 766 San Aleso Ave, Sunnyvale, CA 94086.

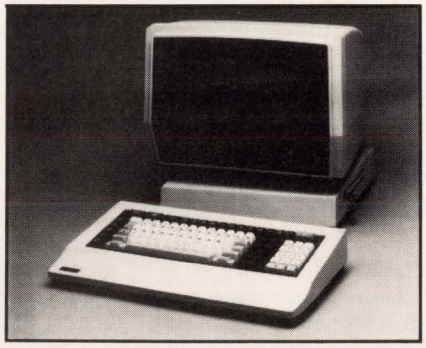
Circle 351

Matrix line printer furnishes bit-image graphics plotting

The MVP 150C offers increased plug compatibility for IBM PC and most other micro users. In addition to correspondence and draft print modes, data processing, and condensed printing, the printer offers elite printing and bit-image graphics plotting. In the elite mode, fully formed character printing occurs at 12.5 chars/in. The unit can be used as a shared resource printer for workstation clusters or as a system printer for microcomputer-based LANs. Price is $2995. **Printronix, Inc**, 17500 Cartwright Rd, PO Box 19559, Irvine, CA 92713.

Circle 352

Data terminals are controlled by microprocessors



Model 8015S uses Bell 8A1 protocol to send and receive asynchronous data at speeds up to 1800 bits/s and synchronous data at 4800 bits/s. With multiple format storage, it offers 8 memory pages with cursor selectable page number, line, and column position. Command mode permits a host or terminal to download time, data, and passwords to all terminals on a network. The 8022S model uses the Univac protocol or synchronous transmission to 9600 bits/s. Both terminals provide one EIA RS-232 port and one Centronics printer port. **Racal-Milgo**, 8600 NW 41st St, Miami, FL 33166.

Circle 353

Laser printer also configures as scanner and copier

The M3071 combines printing, scanning, photocopying, and optical image overlay in one machine. For letter-quality printing it uses laser electrophotography, and for copying it uses a halogen lamp. At a resolution of 240 x 240 dots/in., the M3071 prints 20 pages/min. It performs scanning by transforming data from hard copy to dot data that is sent to the host computer for further processing. The unit sells as a printer only, or can be configured with all or some of the above features. With all options, the M3071 is $7340. **Fujitsu America**, 3055 Orchard Dr, San Jose, CA 95134.
Circle 354

Color monitor displays text, graphics, or video recorder output

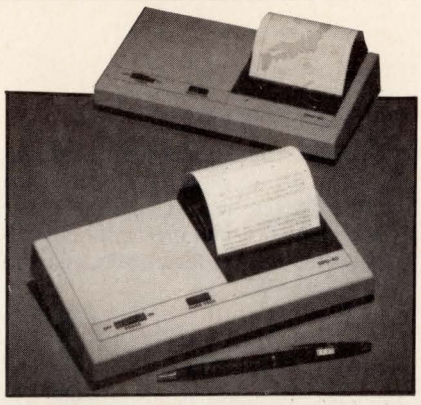
The Color 500 displays text or graphics from microcomputers with NTSC composite or RGB video outputs. Additionally, the monitor provides an auxiliary mode to display inputs from a video recorder. Resolution is rated at 460 (H) dots x 240 (V) lines in the RGB mode and 320 (H) dots x 240 (V) lines in the NTSC composite mode. Dark bulb CRT provides high contrast display. Optional tilt-and-swivel base improves viewer comfort. The Color 500 monitor price is $525. **Amdek Corp**, 2201 Lively Blvd, Elk Grove Village, IL 60007.
Circle 355

Color light pen serves demanding applications

The 260 HP has high sensitivity and functions when illumination is as low as 0.2 ft-L. The pen features push-tip actuation, an electronic assembly with an MTBF over 183,000 h, and high electrooptical performance. The actuation mechanism has a life expectancy in excess of 2 million operations. A light pulse output is produced in less than 0.5 μs in response to a 0.2 ft-L input. Completely self-contained, the pen operates from a single 5-V source. **Interactive Computer Products, Inc**, 23951 El Toro Rd, El Toro, CA 92630.
Circle 356

November Preview
Watch for a special article on memory systems

Transportable printer features high reliability



A DPU-40 printer offers silent thermal operation and interfaces with host via a parallel port. This compact unit weighs 14.1 oz (400 g). Print speed is about 0.6 lines/s. An onboard character generator produces the 96-char ASCII set. The unit uses standard heat-sensitive paper that is 80 mm wide. Friction feed advances the paper. Using an ac adapter, the DPU-40's reliability is set at 500,000 lines MTBF minimum. Unit costs $86.25 in quantities of 1000. **Seiko Instruments**, 2990 W Lomita Blvd, Torrance, CA 90505.
Circle 357

Medium speed printer runs with IBM System 34, 36, and 38

The dot-matrix TX5180 interfaces directly to the IBM systems via a standard twin coaxial cable and is a plug-compatible replacement for the IBM 5256, 5224, and 5225 printers. It supports cable through and terminate features for use as a terminating printer on a chain of seven or as an immediate device. Push-button control panel can access over 50 printer features that can be programmed by the user and stored in nonvolatile memory. Operating at 180 chars/s, the printer generates output ranging from 74 to more than 400 lines/min. Price is $2995. **Datasouth Computer Corp**, 4216 Stuart Andrew Blvd, Charlotte, NC 28210.
Circle 358

Fiber optic light pen handles medium-resolution tasks

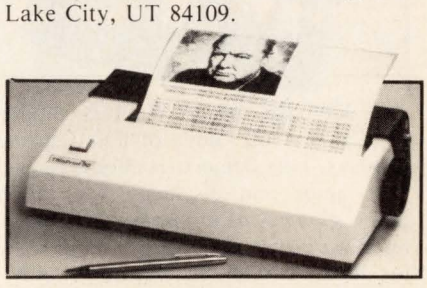
A fiber optic light pen for medium-resolution applications consists of a 5.7-in. pen, 4 ft of fiber optic cable, and a 3.7-in. fiber optic link that plugs into a computer. The pen features color compensation, low light level sensing, error fault rejection, and ambient light rejection. The light pen needs only three lines for operation: V_{cc}, ground, and output. It displays maximum propagation delay of 1 ms. Operating supply voltage is 4.75 to 5.25 V, with an output sink/source current of 1.75 mA. Anticipated price for the pen is $20 each in quantities of 10,000, plus modification costs. **Honeywell Optoelectronics Div**, 830 E Arapaho Rd, Richardson, TX 75081.
Circle 359

Printer can intermix fonts for word processing stations

Laser technology is at the heart of the Smart Writer. This printer is designed for a duty cycle of up to 3000 pages per month. It can print up to eight pages/min. MC68000 processor-based firmware includes Qume, Diablo, and Epson simulation, four standard fonts (three portrait, one landscape), plus capabilities to intermix fonts on one line. Fonts can also be down-loaded. Centronics interface is standard; RS-232 is optional. A user-replaceable cartridge includes toner and a photoreceptor drum. **Quality Micro Systems, Inc**, PO Box 81250, Mobile, AL 36689.
Circle 360

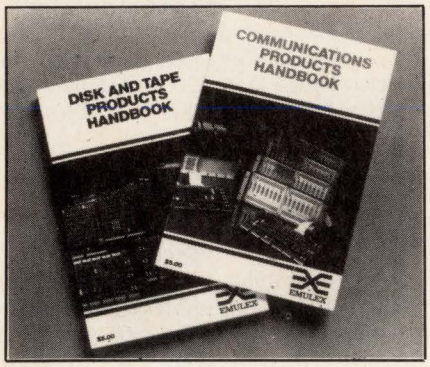
Battery-powered printer incorporates impact printing mechanism

ThinType 80 letter-quality printers use an internal rechargeable power system. A spin-wheel impact printing mechanism is also used. True logic-seeking, bidirectional printing at 15 chars/s is complemented by a long-life ink roll that prints over 1 million chars. The self-contained charger and battery pack give the flexibility of continuous ac and portable dc operation. NiCad charge controller and auto-turn-off/on features further enhance operation. The ThinType 80 weighs under 7 lb (31.7 kg). Centronics interface is standard, with other ports optional. The unit costs $395. **Axonic Corp**, 417 Wakara Way, Salt Lake City, UT 84109.



Circle 361

Controller handbooks

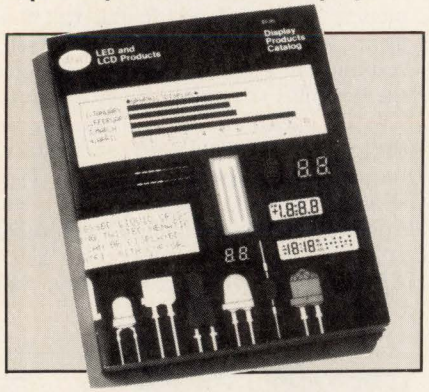


A disk and tape products handbook and a communication products handbook contain systems integration data for DEC-connection of Emulex mass storage and data comm peripherals. **Emulex Corp,** Costa Mesa, Calif.
Circle 410

Shielding windows for emi

A 40-page brochure studies transparent barriers for viewing as well as emi shielding of large window areas. Specific treatment of emi shielding performance, optical performance, optically clear window substrates, contrast enhancement, plus assembly and mounting techniques stand out among topics covered. **Technit,** Cranford, NJ.
Circle 411

Liquid crystal and other displays



The 320-page display product catalog spotlights a full family of liquid crystal displays, LCD dot matrix modules, and LED lamps and displays. Application notes, glossary of terms, industry cross-reference information, and other data are included. **A.N.D.,** Burlingame, Calif.
Circle 412

Surface-mount chips

A 303-page catalog describes chip resistors for surface mounting, resistor networks, discrete leaded resistors, power semiconductors, and magnetic materials. **Allen-Bradley Electronics Group,** Milwaukee, Wis.
Circle 413

Control on the Q-bus

Line of Q-bus data acquisition and control systems, enclosures, monitors, interface modules, wiring accessories, and I/O software gets full treatment in a 64-page catalog. **ADAC Corp,** Woburn, Mass.
Circle 414

Thermal printer/plotters

Revised brochure reports on line of 44- and 80-col thermal printer/plotters. Individual dot addressing, enhanced vector plotting, plus programmable and manual format selection stand out among capabilities. **Gulton Industries, Graphic Instruments Div,** East Greenwich, RI.
Circle 415

Circuits in CMOS

Describing a family of CMOS ICs, a 24-page directory provides detailed descriptions and technical data. Series G65SC00 microprocessors, G65SC150 microcomputers on a chip, and the CFT (customer furnished tooling) program get special attention. **GTE Microcircuits,** Tempe, Ariz.
Circle 416

Resistor networks

Ladder, chip carrier, and custom networks implemented through thick- and thin-film resistors are profiled in a 15-page bulletin. Cutaway and dimensional specification drawings, circuit schematics, and surface temperature graphs are included. **TRW Electronic Components Group, Resistive Products Div,** Philadelphia, Pa.
Circle 417

Memory card for the STD bus

Model 70128 STD bus cards are described in a product bulletin, which includes detailed block diagrams showing the circuitry of these 8085-, 8088-, and Z80-compatible units. **I/O Controls Inc,** Newtown, Pa.
Circle 419

Vision system

Eye vision system is explained in this 4-color brochure, which details the applications and theory underlying the IVS-100. A software and hardware data sheet provides complete specifications. **Analog Devices,** Norwood, Mass.
Circle 418

Multiplexers, LANs, and more

Data communication products from over 70 manufacturers are detailed in a 184-page catalog. Information on multiplexers, LANs, fiber optic equipment, switching and patching systems is included. **Glasgal Communications, Inc,** Northvale, NJ.
Circle 420

T-1 transmission

This technical backgrounder examines digitized voice and effective use of T-1 1.544 Mbit/s transmission facilities. The 16-page booklet presents issues involving the T-1 network's application in mixed data, voice, and video. **Timeplex, Inc,** Woodcliff, NJ.
Circle 421

Test system for telecomm

Twenty-page pamphlet outlines the A360 telecommunications test system. Capable of testing mixed signal telecomm ICs, system allows complex signal generation and signal processing functions in parallel. **Teradyne, Inc,** Boston, Mass.
Circle 422

Design workstation

A full color, six-page brochure profiles an integrated application module set for schematic design, logic simulation, placement, and routing for printed circuit board layout and drafting. **Versatec,** Santa Clara, Calif.
Circle 423

Portable regulators

Twenty-page, illustrated brochure details an expanded line of power conditioners designed to protect sophisticated electronic equipment from voltage irregularities. Portable and hardwired micro/minicomputer regulators, as well as constant voltage transformers, are featured. **Sola Electric,** Elk Grove Village, Ill.
Circle 424

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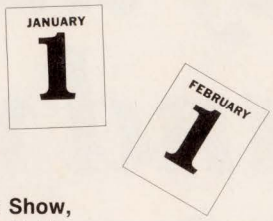

CONFERENCES

NOV 2-4—Autotestcon, Sheraton Washington Hotel, Washington, DC. INFORMATION: M.D. Myles (Code Air 552), Naval Systems Command, Washington, DC 20361. Tel: 202/692-3146

NOV 4-8—Int'l Congress on Advances in Nonimpact Printing Technologies, Stouffer's Concourse Hotel, Arlington, Va. INFORMATION: Richard C. Beach, Itek Graphic Systems, 811 Jefferson Rd, Rochester, NY 14692. Tel: 716/475-9050

NOV 12-15—IEEE Int'l Conf on Computer Aided Design, Santa Clara, Calif. INFORMATION: John A. Domiter, Bell Telephone Labs, 4K523, Holmdel, NJ 07733. Tel: 201/949-6675

NOV 13-17—Elektronica, Munich, W Germany. INFORMATION: Kallman Assoc, 5 Maple Ct, Ridgewood, NJ 07450. Tel: 201/652-7070

NOV 14-18—Comdex/Fall, Las Vegas Convention Center, Las Vegas, Nev. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600

NOV 16-17—Forth Interest Group Convention, Hyatt Palo Alto, Palo Alto, Calif. INFORMATION: Forth Interest Group, PO Box 1105, San Carlos, CA 94070. Tel: 415/962-8653

NOV 27-30—Conf on Magnetism and Magnetic Materials, Town and Country Hotel, San Diego, Calif. INFORMATION: Alex P. Malozemoff, IBM Research Center, PO Box 218, Yorktown Heights, NY 10598. Tel: 914/945-2154

NOV 28-30—Winter Simulation Conf, Sheraton-Dallas Hotel, Dallas, Tex. INFORMATION: Udo W. Pooch, Dept of Computer Science, College of Engin, Texas A&M Univ, College Station, TX 77843. Tel: 409/845-5498

DEC 3-9—Int'l Microcomputer Conf & Display 1984, China, The Guangdong Scientific Hall, Guangdong, PRC. INFORMATION: Meridian Technology Exhibitions Ltd, Rm 1201 Kai Tai Commercial Bldg, 317 Des Voeux Rd C, Hong Kong

DEC 4—Detroit; **DEC 7**—Houston; **DEC 11**—New Orleans; **DEC 14**—New York—**Lotus 1-2-3.** INFORMATION: Software Institute of America, Inc, 8 Windsor St, Andover, MA 01810. Tel: 617/470-3880

DEC 4-6—Western Design Engin Show, Moscone Center, San Francisco, Calif. INFORMATION: David J. Caplin, Clapp & Poliak, 708 Third Ave, New York, NY 10017. Tel: 212/661-8010

DEC 5-7—Conf on Artificial Intelligence Applications, Sheraton Denver Tech, Denver, Colo. INFORMATION: R. Haralick, Dept of Elec Engin, VPI & SU, Blacksburg, VA 24061. Tel: 703/961-6819

DEC 5-7—Fiber Optics Communications, Washington, DC. INFORMATION: Merril A. Ferber, The George Washington Univ, School of Engineering and Applied Science, Washington, DC 20052. Tel: 202/676-6106

DEC 6—California Computer Show, Hyatt Hotel, Palo Alto, Calif. INFORMATION: Norm DeNardi Enterprises, 289 S San Antonio Rd, Suite 204, Los Altos, CA 94022. Tel: 415/941-8440

DEC 6-8—Realtime Systems Symposium, Hyatt Regency Hotel, Austin, Tex. INFORMATION: Miroslaw Malek, Dept of Computer Science, Univ of Texas at Austin, Austin, TX 78712. Tel: 512/471-5704

DEC 9-12—IEEE Int'l Electron Devices Meeting, San Francisco Hilton and Towers, San Francisco, Calif. INFORMATION: Melissa M. Widerker, Courtesy Associates, Inc, 665 15th St, NW, Suite 300, Washington, DC 20005

DEC 10-11—IEEE Computer Society Computer Networking Symposium, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Computer Networking, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

DEC 10-11—Micro/Personal Computer Operating Systems, Boston, Mass. INFORMATION: Software Institute of America, Inc, 8 Windsor St, Andover, MA 01810. Tel 617/470-3880

DEC 10-14—Hands-On Programming in Ada, Washington, DC. INFORMATION: George Harrison, The George Washington Univ, School of Engin and Applied Science, Washington, DC 20052. Tel: 202/676-6106

DEC 10-14—Modern Digital Signal Processing, Washington, DC. INFORMATION: Shirley Forlenzo, The George Washington Univ, School of Engin and Applied Science, Washington, DC 20052. Tel: 202/676-6106

DEC 11-13—Fifth-Generation and Supercomputer Symposium, Rotterdam, The Netherlands. INFORMATION: Rotterdam Tourist Office, Stadhuisplein 19, 3012 AR Rotterdam. Tel: 010/14 14 00

JAN 24-26—Modeling and Simulation on Microcomputers, Bahia Hotel, San Diego, Calif. INFORMATION: Ray Swartz, Berkeley Decisions/Systems Inc, 730 Park Ct, Santa Clara, CA 95050. Tel: 408/984-6397

FEB 5-7—Mini/Micro West Computer Conf and Exhibit, Anaheim Hilton Hotel, Anaheim Calif. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-1965

FEB 13-15—Int'l Solid State Circuits Conf, New York Hilton, New York, NY. INFORMATION: Lewis Winner, Almeria, Coral Gables, FL 33134. Tel: 305/446-8193/4

Feb 25-28—Compcon Spring, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SHORT COURSES

NOV 26-27—Personal Computers/ Worcester Polytechnic Institute, The Hilton, Natick, Mass. INFORMATION: Kathy Shaw, WPI, Office of Continuing Education, Worcester, MA 01609. Tel: 617/793-5517

NOV 28-30—Engineering Use of Lotus 1-2-3/Worcester Polytechnic Institute, Int'l Management Services Computer Lab, Framingham, Mass. INFORMATION: Kathy Shaw, WPI, Office of Continuing Education, Worcester, MA 01609. Tel: 617/793-5517

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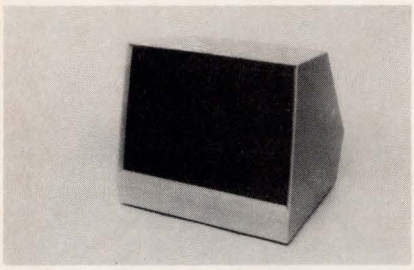

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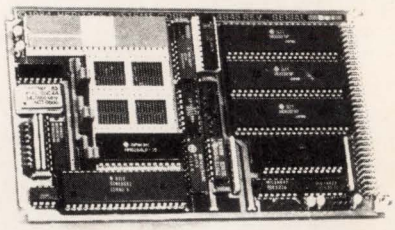

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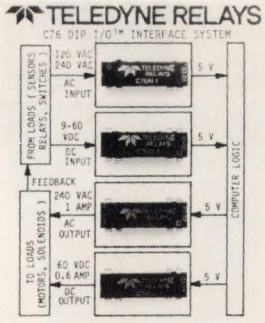

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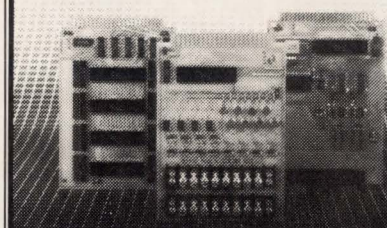

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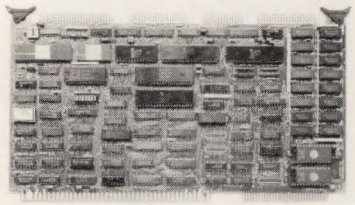

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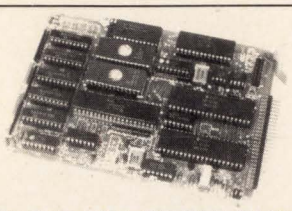

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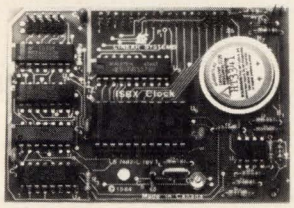

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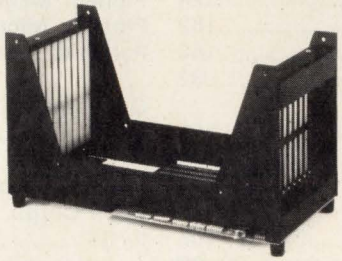

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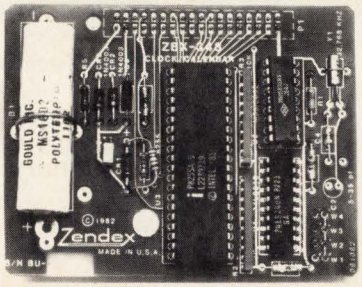

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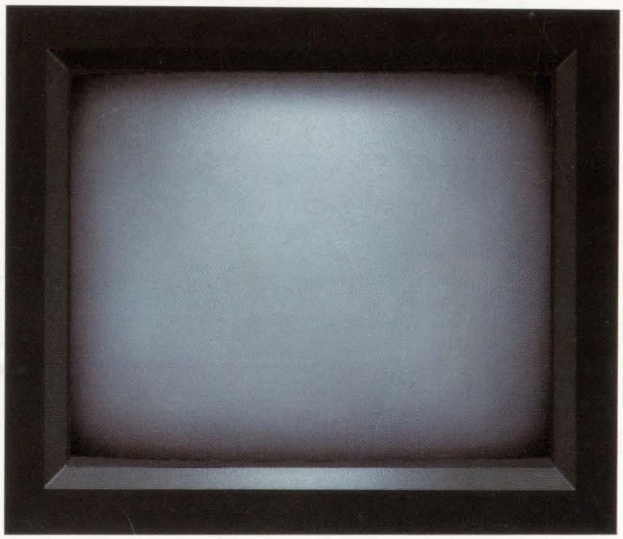

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