A PENNWELL PUBLICATION

FEB. 1982

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

SPECIAL REPORT:
INNOVATIONS IN SYSTEMS ARCHITECTURE

COPYING ROMS: RIGHT OR WRONG

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THROUGH ROTATING HEAD TECHNOLOGY

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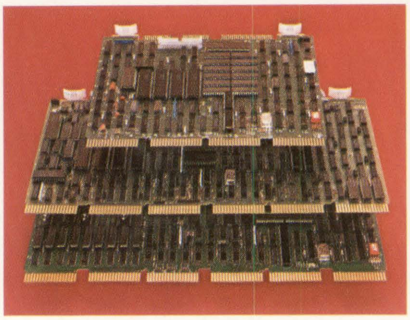
Now there's an advanced technology family of single board controllers for DEC* computers from Western Peripherals—the number one name in controllers.

The TC-131 (for PDP-11s*) is the first TM-11 emulating controller to combine PE and NRZ on one standard hex board. It lets you mix 9-track, PE, NRZ or dual density tape units in any combination up to 125 ips. A 64 byte data buffer allows installation at any point on the unibus without consideration of NPR priority.

The TC-151 single board NRZI tape controller interfaces any industry-standard drive to the LSI-11.* Add a dual width Phase Encode Board for the same performance as the TC-131.

The DC-231 accommodates up to four SMD disc drives of 40 to 600 mb each with RMO2 emulation. Its four sector (2048 bytes) data buffer makes "data-late" errors a thing of the past. The advanced technology "micro-engine" allows a complete track to be written on a single drive revolution. A measurable performance advantage for your PDP-11.



All three controllers are software compatible. All have self test. All are backed by one of the best factory service organizations in the business. And all can be delivered in 30 days.

For more information, call or write today: Western Peripherals Division, Wespercorp, 14321 Myford Road, Tustin, CA 92680, U.S.A. (714) 730-6250. TWX: 910 595-1775. CABLE: WESPER

Number 1 in controllers for DEC and Data General computers.

western peripherals™
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*Trade name of Digital Equipment Corporation.

CIRCLE 1 ON INQUIRY CARD

When you ask some people about backup — they back off.

And for good reason. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer.

Kennedy is the only company that can offer an SMD compatible, 8" 40 MByte disk drive (Model 7300) and an 80 MByte 14" Winchester disk drive (Model 5380). To back them up, Kennedy has a ¼" cartridge recorder (Model 6450), and Model 6809, ½" Data Streamer Tape Transport.

Kennedy was the first to utilize the ¼" 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

Kennedy has always backed its products. That's why we're No. 1. Call or write us about your problem.

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CIRCLE 2 ON INQUIRY CARD

New Cromemco System One shown with our high-capability terminal and printer.

A new small computer that won't limit you tomorrow

Here's a low-priced computer that won't run out of memory capacity or expandability halfway through your project.

Typically, computer usage tends to grow, requiring more capability, more memory, more storage. Without a lot of capability and expandability, your computer can be obsolete from the start.

The new System One is a real building-block machine. It has capability and expandability by the carload.

Look at these features:

- **Z80-A processor**
- **64K of RAM**
- **780K of disk storage**
- **CRT and printer interfaces**
- **Eight S-100 card slots, allowing expansion with**
  - **— color graphics**
  - **— additional memory**
  - **— additional interfaces for telecommunications, data acquisition, etc.**
- **Small size**

GENEROUS DISK STORAGE

The 780K of disk storage in the System One Model CS-1 is much greater than what is typically available in small computers. But here, too, you have a choice since a second version, Model CS-1H, has a 5'' Winchester drive that gives you **5 megabytes** of disk storage.

MULTI-USER, MULTI-TASKING CAPABILITY

Believe it or not, this new computer even offers multi-user capability when used with our advanced CROMIX* operating system option. Not only does this outstanding O/S support multiple users on this computer but does so with powerful features like multiple directories, file protection and record level lock. CROMIX lets you run multiple jobs as well.

In addition to our highly-acclaimed CROMIX, there is our CDOS*. This is an enhanced CP/M† type system designed for single-user applications. CP/M and a wealth of CP/M-compatible software are also available for the new System One through third-party vendors.

COLOR GRAPHICS/WORD PROCESSING

This small computer even gives you the option of outstanding high-resolution color graphics with our Model SDI interface and two-port RAM cards.

Then there's our tremendously wide range of Cromemco software including packages for word processing, business, and much more, all usable with the new System One.

ANTI-OBSOLESCENCE/LOW-PRICED

As you can see, the new One offers you a lot of performance. It's obviously designed with anti-obsolescence in mind.

What's more, it's priced at only $3,995. That's considerably less than many machines with much less capability. And it's not that much more than many machines that have little or nothing in the way of expandability.

Physically, the One is small — 7'' high. And it's all-metal in construction. It's only 14⅛'' wide, ideal for desk top use. A rack mount option is also available.

CONTACT YOUR REP NOW

Get all the details on this important building-block computer. Get in touch with your Cromemco rep now. He'll show you how the new System One can grow with your task.

*CROMIX and CDOS are trademarks of Cromemco Inc.
†CP/M is a trademark of Digital Research

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CIRCLE 3 ON INQUIRY CARD

UP FRONT

IC device reliability report offered by DoD

Digital Failure Rate Data 1981, containing over 400 pages of data on the reliability experience of thousands of SSI and MSI devices currently in use in active government and industry programs, is available from the Reliability Analysis Center (a Department of Defense Information Analysis operation), Griffiss AFB, NY 13441, at $60/copy prepaid in the U.S. ($70 non-U.S.). Ordering number is MDR-17. Data in the book have been analyzed and evaluated for reliability by experienced RAC staff engineers, and cover a broad range of device technologies, including TTL, CMOS, PMOS, NMOS, Schottky, and ECL.

All information necessary for individual device failure rate computation per MIL-HDBK-217C prediction models is provided: operational type, device manufacturer and part number, complexity, screens, environmental stress, operational life or test hours, number of units stressed, and number failed. Over 90 pages cover generic failure rates, observed failure rates vs MIL-HDBK-217C predictions, and field replacement rates.

Draft standard on local computer networks published

A 400-page "Draft B" of the IEEE 802 Local Network Standards Committee is now available from the IEEE Computer Society, PO Box 639, Silver Spring, MD 20901 (request IEEE 802 Draft Standards), or 10662 Los Vaqueros Circle, Los Alamitos, CA 90720 (specify order number 905). Cost is $9 prepaid for Society members or $12 for nonmembers.

Inventory of available software packages being compiled

Software producers or vendors who have not yet registered with the National Center of Scientific and Technological Information (COSTI) may still do so in time to be included in the international survey being conducted under authorization of UNESCO. An inventory of software packages (only those that will be operational by Dec 1982) available for mainframes, minicomputers, and microcomputers is scheduled for publication by the end of 1982. For details, contact COSTI, PO Box 20125, Tel-Aviv 61 200, Israel.

Agreements

Under terms of agreements between GenRad, Inc, and Cirrus Computers, Ltd, 25% ownership of the British advanced software consulting group's holding companies in the U.K. and the U.S. will be sold to the Concord, Mass, test equipment manufacturer through an exchange of common stock. GenRad will also have an option to purchase the remaining 75%.

CTS Corp has purchased for cash the shares of Fabri-Tek Inc owned by M. F. Mickelson, chairman of the board and president of the latter company. A tender offer will be made for all of the remaining 62% of Fabri-Tek shares at the same cash price ($6/share).

Pretriggers

Integrated circuits

A bipolar LSI microcontroller from Signetics called the 8X305 can fetch, decode, and execute instructions in one 200-ns machine cycle. The Schottky device is a speedier version of the previously announced 8X300. It is supported by a host of new products including the 8X310 interrupt controller coprocessor, the 8X355 32-deep LIFO stack, the 8X360 memory address director, and four faster and easier to program I/O devices.

Pretriggers

Microprocessors/microcomputers

The first two members of Texas Instruments' TMS99000 family of third-generation 16-bit microprocessors consist of "the world's first floating point microprocessor," and of a baseline CPU with an 84-instruction set.

Interface

A standard interface that boasts low power, low cost, and small size, the Hewlett-Packard Interface Loop (HP-IL) enables HP-41C and -41CV handheld computers to control and read data from digital multimeters and to interact with a digital tape cassette drive and thermal printer/plotter.

Storage Technology's 8890 intelligent disk controller is said to reduce sequential I/O times by 40% to 75% over standard controllers, thereby significantly improving batch throughput.

System elements

Piezoelectricity's recently recognized ability to produce discrete and controlled motions has been put to use by Piezo Electric Products, Inc as the basis for devices that replace common mechanical and electromechanical switches, valves, and relays.

An optoelectronic keyboard from Optical Techniques International detects key movement through the interruption of light beams, enabling a device with one-third the parts of a standard keyboard.

Computers

Britton Lee's IDM 200 relational database management system can be used in medium or large scale applications as a standalone system supporting intelligent terminals, or as a central resource for several mini- or microcomputers.

A triple symmetric multiprocessing configuration for Digital Equipment Corp's DECsystem-10 mainframes enables three central processors to support up to 250 active jobs.

Data acquisition

Two high resolution data acquisition subsystems introduced by Analog Devices, Inc provide 14- and 15-bit resolution with maxiumum linearity of ±0.005% and ±0.003% of full scale.

Data communications

The transmission rate of Micromation's M/LINK intelligent modem board, which links S-100 microcomputers to mainframes at 2400 baud over standard Bell 201C phone lines, supports voice and data transmission using SDLC or bisync protocols.

Memory systems

Less than half the height of standard 8" drives, two of the single- and double-sided floppy disk drives introduced by Shugart Associates can fit into the space previously used by a single drive.

Peripherals

Look for a 50M-byte, 4-platter, 5.25" Winchester disk drive from EVOTEK at NCC. Use of plated media results in low error rates and high signal resolution.

Recently announced OEM graphics products from Metheus Corp include a display controller, a graphics subsystem, and a software package that supports development of systems for the other devices and includes 51 FORTRAN-callable subroutines.

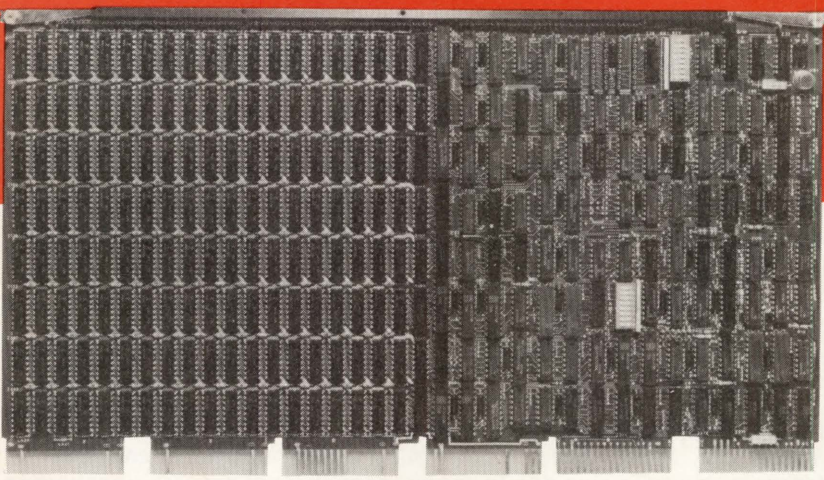
When installed in the card cage of a DEC VT-100 or C. Itoh CIT-101 terminal, the Selanar Corp SG200 graphics retrofit board adds Tektronix 4014 emulation capability.

Software

Two more versions of the VRTX realtime silicon 16-bit operating system kernel have been released by Hunter & Ready. Now, in addition to a version for the Z8002, there are versions for the 68000 and for the 8086 and 8088. VTRX extends the architecture of its companion microprocessor by adding a set of 22 operating system instructions for task management, message passing, memory management, interrupt handling, and character I/O. Except for a small configuration table, program functionality is identical across architectures. Programs written in C and compiled are identical and portable between the different processors.

Postmaster: CHANGE OF ADDRESS—FORM 3579 to be sent to Computer Design, Circulation Dept, PO Box 593, Littleton, MA 01460. (USPS 127-340)

DEC®-COMPATIBLE SEMI ADD-INS



FROM THE LEADER

Look to the leader — Dataram — for your DEC-compatible semiconductor add-in memory. Offering not only the broadest, most complete line of semi add-ins, but the most capable...no matter what your yardstick. Compatibility, throughput, cost, power efficiency, size...no matter how you measure capability, Dataram DEC-compatible semi add-ins are the clear leader.

A leadership position earned by improving on DEC's price and delivery...and then adding features available from no one else in the industry.

The chart provides a glimpse at the industry-pacesetting family of DEC-compatible semi add-ins. Circle the reader service number below or, better yet, call us today at 609-799-0071, and we'll give you a close-up look at the products that have made us the leader.

DEC Mini	Dataram Add-In	Board Size	Maximum Capacity
LSI-11®	DR-115S	dual	64 KB
LSI-11	DR-215S	dual	256 KB
LSI-11	DR-113S	quad	256 KB
LSI-11	DR-213S	quad	1.0 MB
PDP®-11	DR-114S	hex	256 KB
PDP-11	DR-114SP	hex	256 KB
PDP-11	DR-214SP	hex	1.0 MB
PDP-11	DR-144S	hex	256 KB
PDP-11	DR-244S	hex	4.0 MB
VAX®-11/750 PDP-11/70	DR-175S	hex	256 KB
VAX-11/780	DR-178S	extended hex	512 KB
DECSYSTEM 2020®	DR-120S	extended hex	512 KB
PDP-8/A	DR-118S	quint	128 K x 12

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Dataram also provides core add-ins, core and semiconductor add-ons, memory system units, memory management, and a wide range of memory-related accessories for DEC users.

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CIRCLE 4 ON INQUIRY CARD

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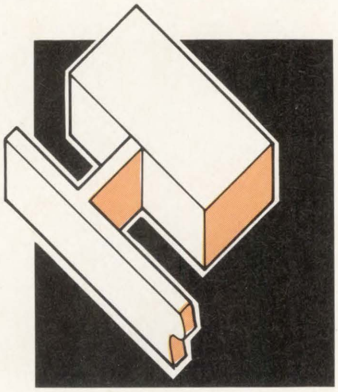
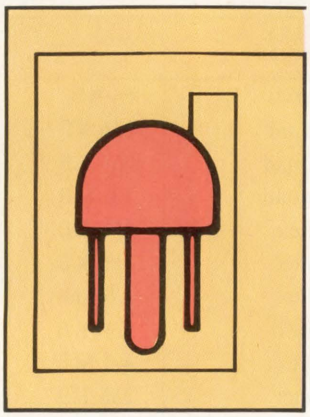
System technology



50 *Distributed hardware architecture of multiple-microcomputer transaction processor virtually eliminates computer downtime*

System design



149 *Equipment designers control all factors in their systems—except the quality of commercial power lines; the responsibility for conditioning those lines falls to the system user*

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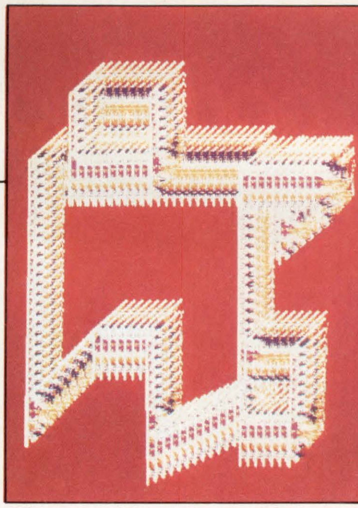
BPA ABP

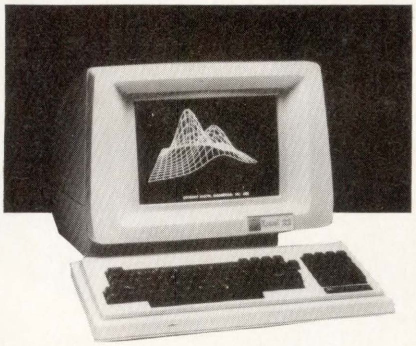
Vol 21, No 2
Feb 1982

Special report on innovations in systems architecture



This month's cover, entitled "Systems architecture," was created by Larry Gartel with the Images system at the New York Institute of Technology

System components



229 *VT-100 compatible, monochromatic graphics terminal offers 12" or 14" nonglare screen and detachable typewriter style keyboard*

Departments

Designers' Preference Survey*

*Appearing in Domestic issues only

Editorial reviewers for this issue:

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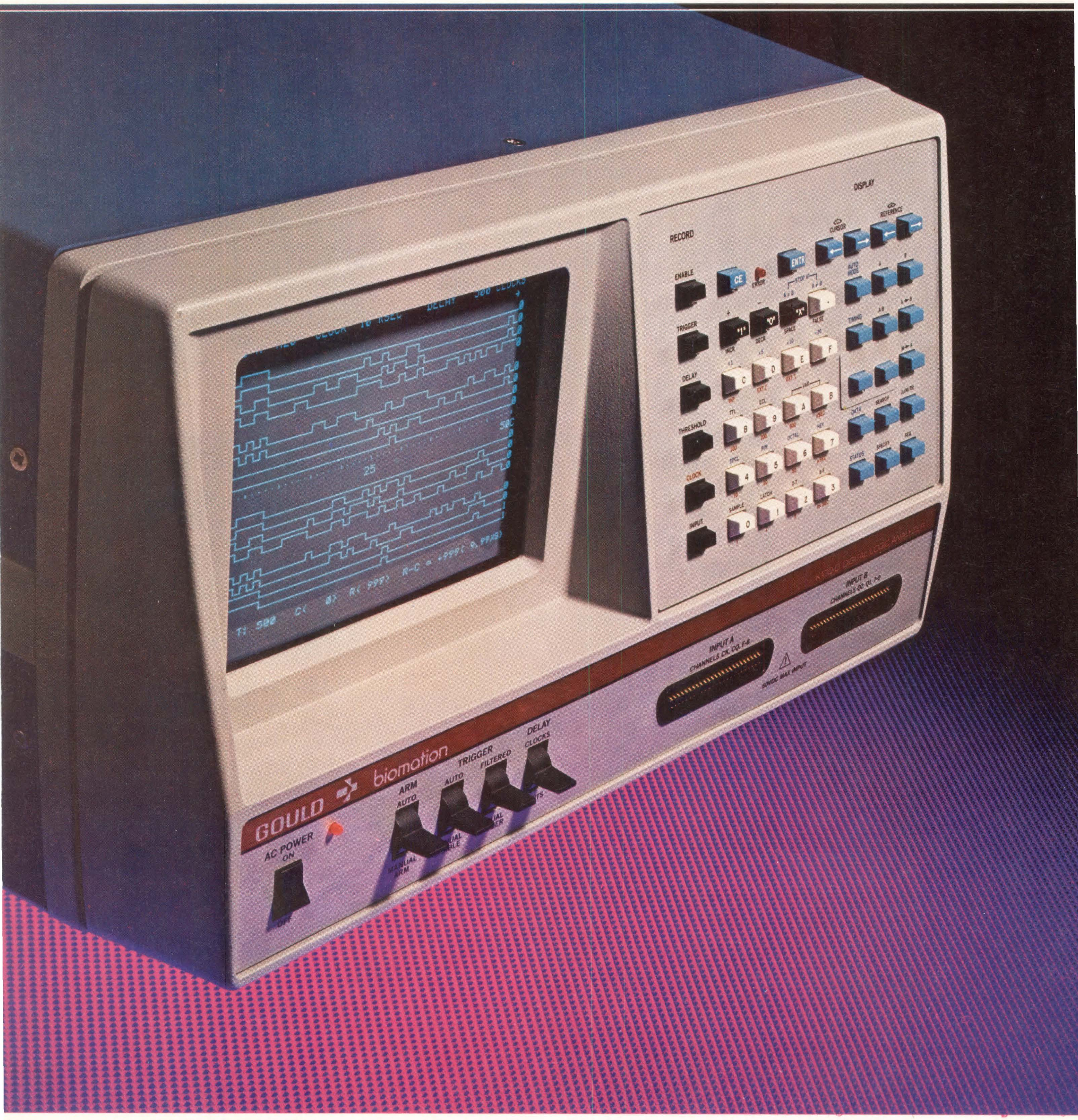
GOULD BIOMATION K100-D



7 reasons why the K100-D is now the world's best-selling logic analyzer.

How the general-purpose K100-D beat out H-P to become #1.

Not so long ago, Hewlett-Packard logic analyzers were the industry standard. We asked digital designers to compare the K100-D with H-P's popular 1610B and 1615A logic analyzers before making any buying decision.

In head-to-head comparison, the K100-D came out looking so good, it's now the best-selling logic analyzer in the world. Here's why:

1. It's easy to systematize.

For automated troubleshooting and production ATE, the K100-D features a fully-programmable GPIB interface.

To help you support a wide variety of bus-oriented systems, there are standard high-performance probes, specialized probing accessories and detailed application notes available on all the popular microprocessor systems currently in use.

2. It's concise.

The K100-D monitors 16 channels in time domain, 32 in data domain, so you can probe enough points to pin down problems at their source.

3. It's fast.

A 100 MHz clock rate resolves signals to 10 nanoseconds. The front end is also sensitive enough to capture glitches as narrow as 4 ns.

4. It's deep.

1024 words deep in memory—for faster, more accurate debugging. The K100-D extends the length of data you can trap from your system at any one time.

5. It's clear.

The K100-D has a large keyboard and interactive video display, a comprehensive status menu, highly useful time domain display, and data domain readout in user-specifiable hexadecimal, octal, binary or ASCII.

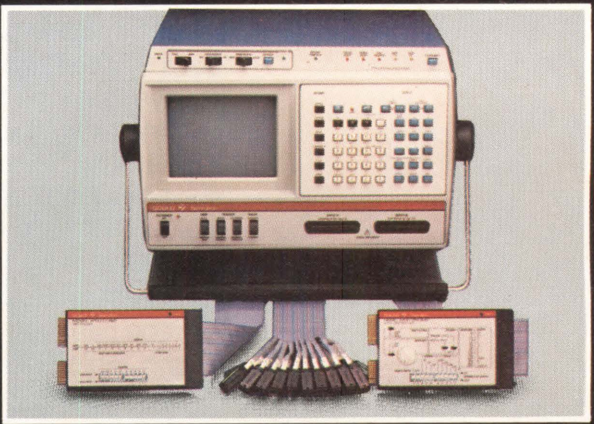
6. It has remote diagnostics.

A new T-12 communications interface option lets your field troubleshooters share their system observations with the best engineers back at headquarters. Remote diagnostics provide faster debugging and save a lot of time and travel for your most valuable people.

7. It's well supported.

You get full applications support from the experts in logic analysis.

For a free copy of our "Logic Analyzer Comparison Guide," request card for microprocessor system application notes, and T-12 Communicator information, just circle the appropriate reader service numbers. Or contact Gould, Inc., Instruments Division, Santa Clara Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050, phone (408) 988-6800.



The T-12 "top hat" for the K100-D provides logic analyzer remote diagnostic capability. Other options include the GPIB Analyzer and RS232 Serial Data Analyzer.

Circle 5 for Comparison Guide
Circle 6 for App. Note request form
Circle 7 for T-12 communicator data

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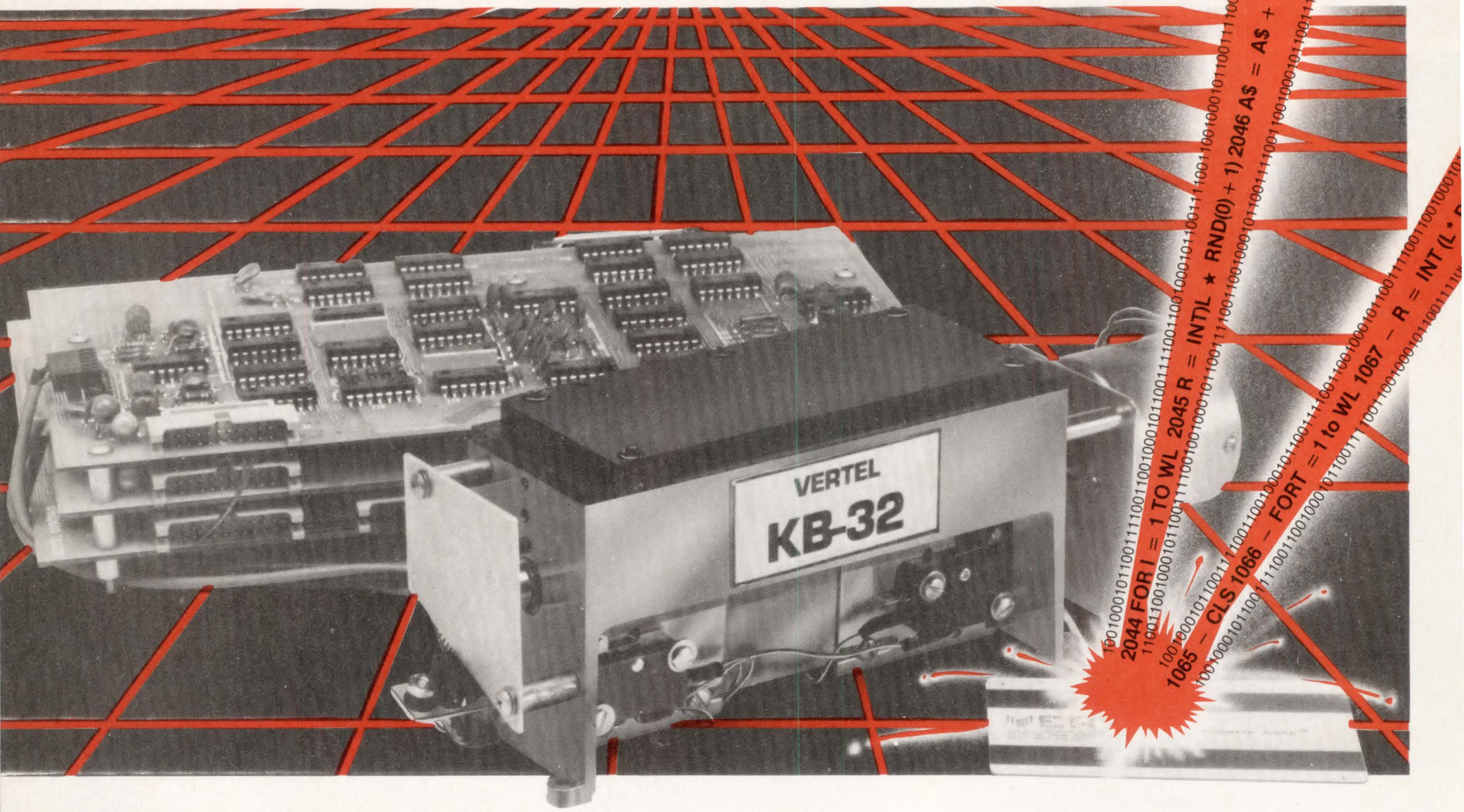
At VERTEL, we just can't leave well enough alone.



We've doubled storage capacity and reduced reading time...simultaneously

Introducing the KB-32 Magnetic Card Reader/Writer. At Vertel we're always looking for ways to improve parameter loading. With our new KB-32 Card Reader/Writer, we have even outdone the KB-31 system...a system that has become an industry standard.

For example, we've doubled the storage capacity of our Kilobyte card™, which now means you can record over 2176 8-bit bytes on one card. And our new reader/writer has an improved head that reads all 4 tracks simultaneously...providing twice the amount of information in one-half the time, thereby improving reading time by a rate of 4.

Designed for microprocessor-based systems, the new KB-32 is ideally suited as a low cost peripheral for parameter loading and/or data storage in process control systems, medical data systems and other similar applications.

Call us today to see how the Kilobyte™ system can benefit you!

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ON THE QUALITY OF PROFESSIONAL LIFE ACCORDING TO OUR READERS

☐ Salary ☐ Fringes ☐ Location

Our research department just finished tabulating an interesting survey that is somewhat connected with my December '81 editorial and contains some intriguing information. Although our readers span the gamut of executive engineering management to design engineers, our average reader is a senior engineer, whether in software or hardware. This average reader is 30 to 39 years old and has from one to three years of experience in his current job assignment. Asked to rank in order of overall importance what most people look for in a job, it's not hard to guess that salary is most important. That has been the goal of every struggling engineering student I've ever met. It's also not surprising that the tenor of the times—inflation—has taken its place in importance for our average engineer in the form of desire for extended medical and retirement benefits, and in that order. Almost equal in rank to retirement benefits are vacation benefits. Also not really surprising, work hard/play hard is very much in keeping with the tempo of the times.

What is surprising, to some extent, is that as many respondents are satisfied with their current salaries, as are dissatisfied. That, perhaps, is a more accurate measurement of the toll being taken by inflation and their confidence in any forthcoming prospects for reduction in inflation. Even more surprising, but perhaps linked to the desire for more direct compensation, is that twice as many respondents are unsatisfied with growth potential in their current positions as are satisfied. If we actually look at the average respondent (our senior engineer), three times as many felt dissatisfied with present growth opportunities as those who were satisfied.

Despite all of the flak offered by the sunbelt, the bulk of the software-involved respondents currently work in the mid-Atlantic states, while the bulk of hardware-involved respondents work on the West Coast. When asked where they would like to be, most software-involved respondents said the mountain states, while hardware-involved respondents still prefer the West Coast. Without casting any aspersions, neither hardware nor software respondents listed the Midwest as their favorite prospective place to work. Not surprising, however, since there is a universal primary interest in salary and benefits, is that almost everyone would consider any location if the compensation package was right.

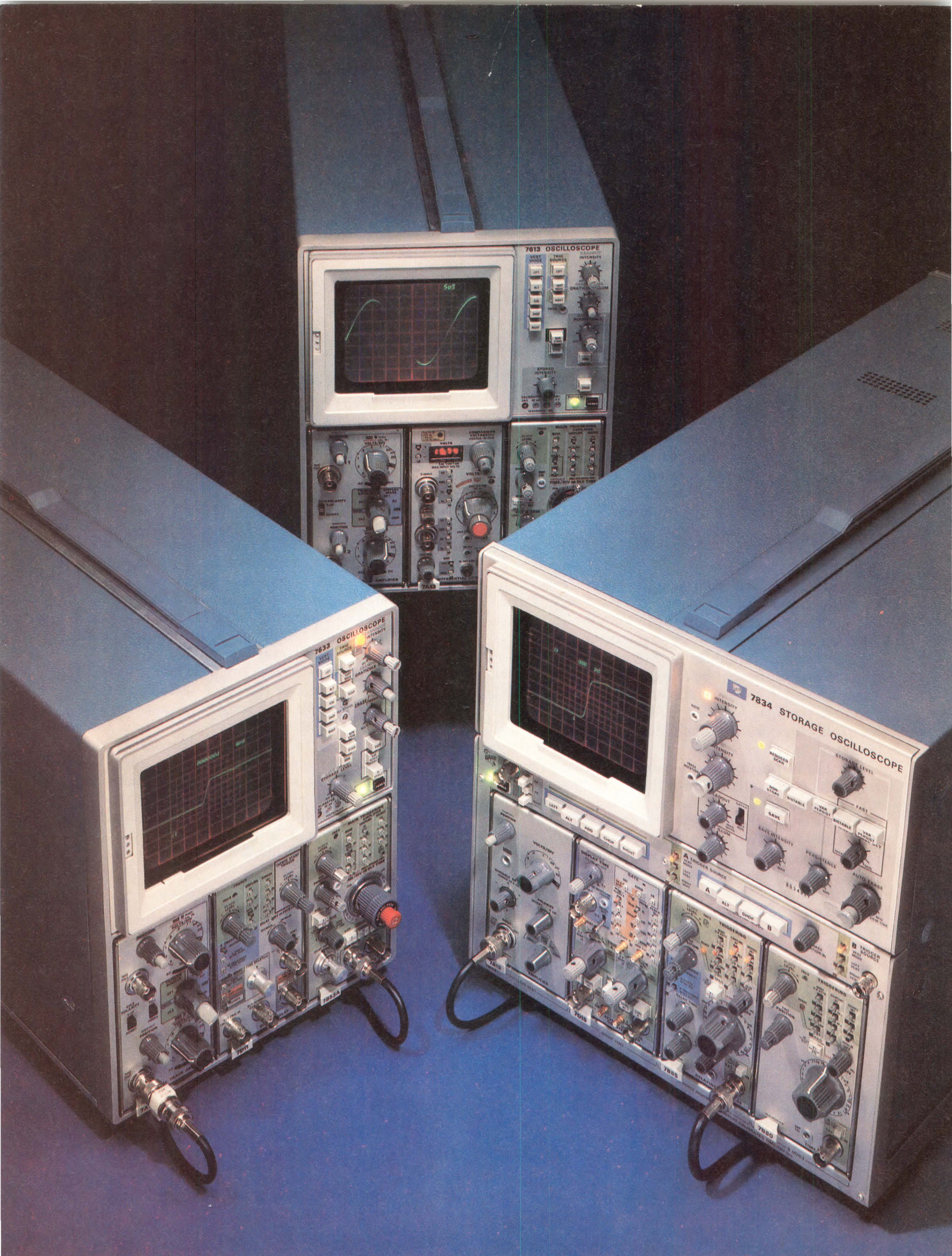
The last item I gleaned from the compilation will probably come as a surprise to the current administration in light of its intentions to crank up defense spending; our average respondent would prefer not to work in defense oriented industries. Going back to the bulk of the people who constitute our average respondent—the senior engineer—and realizing that the number of years out of school for these people is 10 to 19 years, that places them right in the middle of the generation of students that sweated the Viet Nam war out in college. Perhaps all of you in that age bracket who protested, and demonstrated, and felt that you had no effect on the overall scheme of things, may just get your retribution yet—10 to 20 years after the fact.

Saul B. Dinman

Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—September
"Designing Software for Maintainability"
Judith A. Clapp, The MITRE Corporation

This article will now compete with other monthly winning articles for the 1981 Windjammer cruise award.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CONFERENCES

MAR 3—California Computer Show, Marriott Hotel, Anaheim, Calif. INFORMATION: Carol Reimer, Norm De Nardi Enterprises, 289 S San Antonio Rd, Suite 204, Los Altos, CA 94022. Tel: 415/941-8440

MAR 15-17—Human Factors in Computer Systems/NBS, Gaithersburg, Md. INFORMATION: Wilma Osborne, A265 Technology Bldg, Nat'l Bureau of Stds, Washington, DC 20234. Tel: 301/921-3485

MAR 19-21—Computer Faire, San Francisco Civic Auditorium and Brooks Hall, San Francisco, Calif. INFORMATION: Laurie McLean, Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: 415/851-7075

MAR 22-25—Interface Nat'l Conf and Expo for Data Communications/ DDP/Networking, Dallas Conv Ctr, Dallas, Tex. INFORMATION: The Interface Group, PO Box 927, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

MAR 23-25—Southcon, Sheraton Twin Towers Hotel, Orlando Hyatt Hotel, and Holiday Inn International Drive, Orlando, Fla. INFORMATION: Robert Myers, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAR 23, MAR 25, AND APR 14—Invitational Computer Confs, Dallas Marriott, Dallas, Tex; Adam's Mark Hotel, Houston, Tex; and Sheraton Southfield, Southfield, Mich. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

MAR 30-APR 1—INFOCOM '82, Joint Conf of the IEEE Computer and Communications Societies, Las Vegas, Nev. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

APR 4-7—SOUTHEASTCON '82, Sandestin Conv and Resort Ctr, Destin, Fla. INFORMATION: Carolyn Schauble, Conv Chairman, U.F. Graduate Engineering Ctr, PO Box 1918, Eglin Air Force Base, FL 32542. Tel: 904/882-5614

APR 5-7—Office Automation Conf, Moscone Ctr, San Francisco, Calif. INFORMATION: Betty Lou Cooke, American Federation of Information Processing Societies, Inc, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/558-3600

APR 14-16—Local Networks and Distributed Office Systems, Business Strategy Conf and Expo, London Tara Hotel, Kensington W8, England. INFORMATION: Online Conferences Limited, Argyle House, Northwood Hills, Middlesex, HA6 1TS, UK. Tel: (09274) 28211; Telex: 923498

APR 15-18, APR 22-25, and MAY 6-9—Computer Show and Office Equipment Expo, Dallas, Tex; Uniondale, NY; and Los Angeles, Calif. INFORMATION: National Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

APR 21-28—Hanover Fair, Hanover, West Germany. INFORMATION: Hanover Fairs Information Ctr, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

MAY 3-5—Acoustics, Speech and Signal Processing Internat'l Conf, Paris, France. INFORMATION: Prof Claude Gueguen, Dept Systemes et Communications, Ecole Nationale Superieure des Telecommunications, 46 Rue Barrault, 75634 Paris, Cedex 13 France

MAY 10-12—IEEE Symposium on Circuits and Systems, Rome, Italy, INFORMATION: Institute of Electrical and Electronic Engineers Inc, 6411 Chillum Pl, NW, Washington, DC 20012

MAY 11-13—Society for Information Display Internat'l Sym, Town-Country Hotel, San Diego, Calif. INFORMATION: L. Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

MAY 18-20—Northcon, Seattle Ctr Coliseum, Seattle, Wash. INFORMATION: Robert Myers, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAY 25-27—Electro, Sheraton-Boston Hotel, Hynes Auditorium, and Commonwealth Armory, Boston, Mass. INFORMATION: Robert Myers, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

SEMINARS

Computer Technology and Requirements for Federal Electronic Regulatory Compliance Seminars, various U.S. cities and dates. INFORMATION: Don White Consultants, Inc, International Training Ctr, State Route 625, PO Box D, Gainesville, VA 22065. Tel: 703/347-0030; Telex: 89-9165

Network Protocols Seminars, various U.S. cities and dates in March. INFORMATION: American Institute for Professsional Education, 100 Kings Rd, Madison, NJ 07940. Tel: 201/822-1230

MAR 9-11—Internat'l Zurich Seminar on Digital Communications, Swiss Federal Institute of Technology, Zurich, Switzerland. INFORMATION: Secretariat 82 IZS, Miss M. Frey, EAE, Siemens-Albis AG, CH-8047 Zurich, Switzerland. Tel: +41-1-247 51 20

SHORT COURSES

MAR 2-5—Packet Switching Networks for Modern Data Communications, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: 202/676-6106; 800/424-9773 (outside DC)

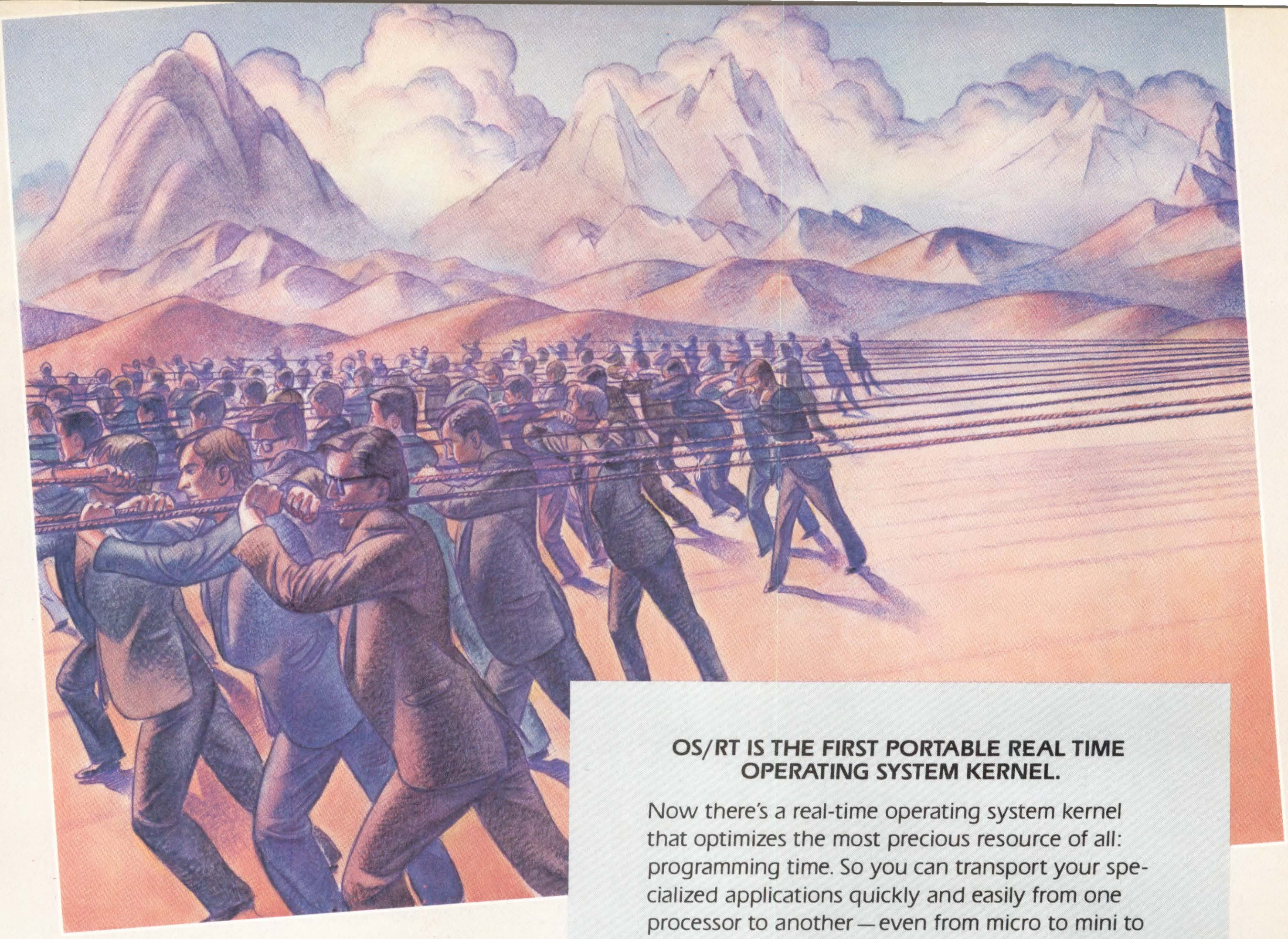
MAR 9-12 and APR 20-23—VIO-Voice Input/Output for Computers, Los Angeles, Calif; Boston, Mass. INFORMATION: Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405. Tel: 213/450-2060

MAR 15-17—Fiber Optical Communications, Arizona State Univ, Tempe, Ariz. INFORMATION: Ctr for Professional Development, College of Engineering and Applied Sciences, Arizona State Univ, Tempe, AZ 85287. Tel: 602/965-1740

MAR 15-19—Structured Programming and Software Engineering, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 22052. Tel: 202/676-6106; 800/424-9773 (outside DC)

MAR 22-23 AND MAR 24-26—Review of Pascal and Introduction to Ada, Univ of Wisconsin-Extension, Madison, Wis. INFORMATION: Avinash Vaidya, Program Director, Dept of Engineering and Applied Science, 432 N Lake St, Madison, WI 53706. Tel: 608/262-8592

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last minute changes.



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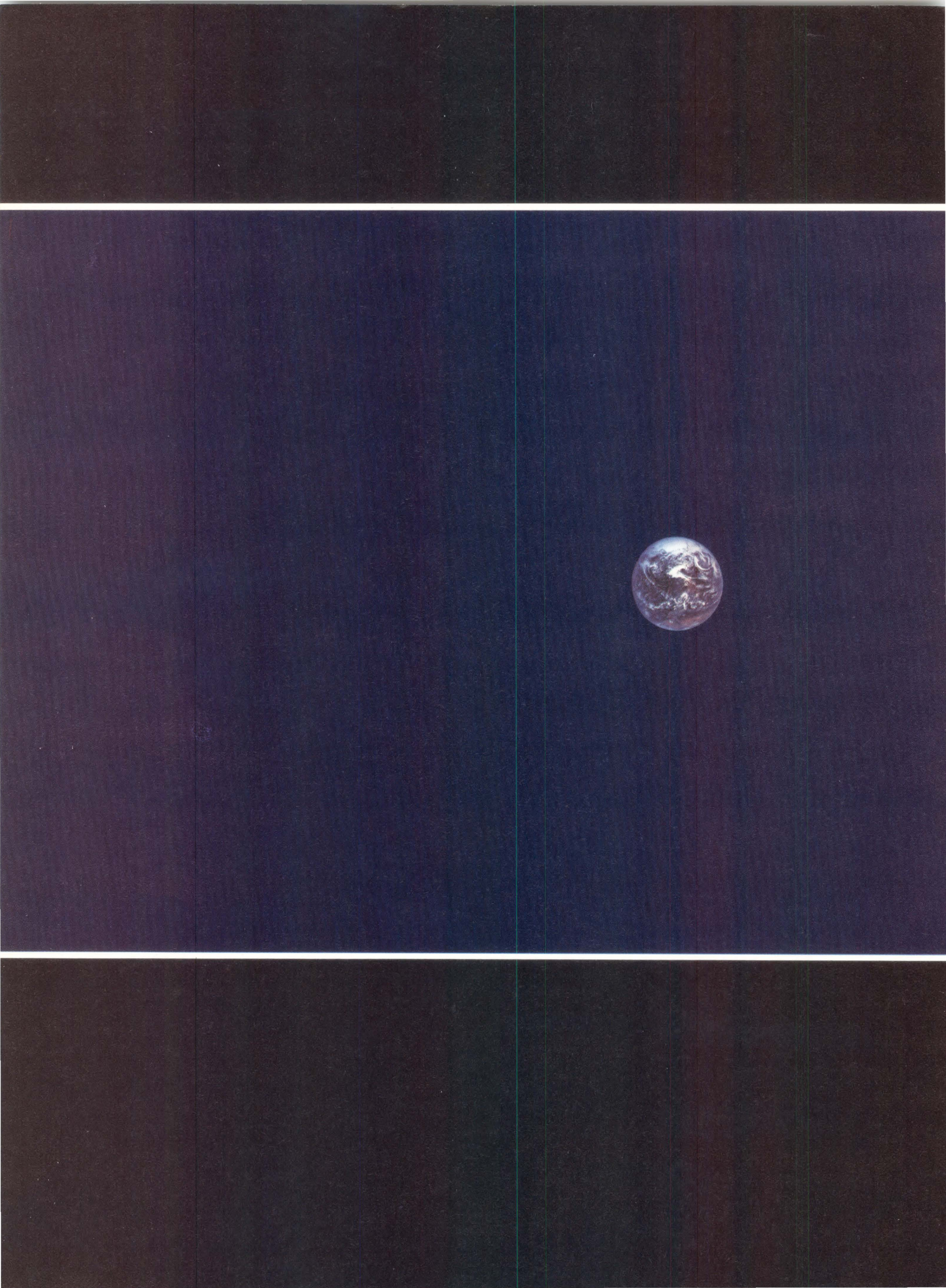
CIRCLE 16 ON INQUIRY CARD



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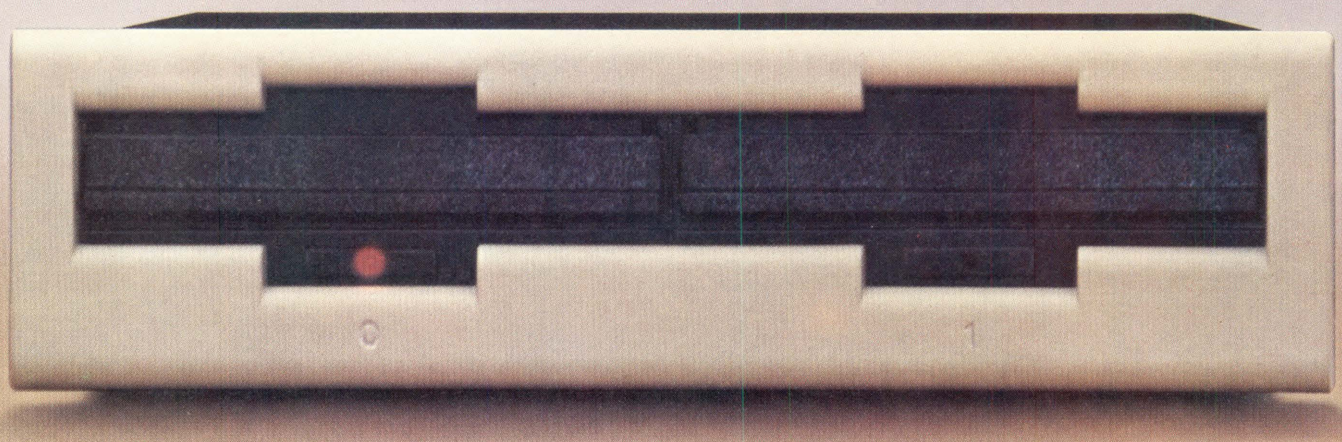

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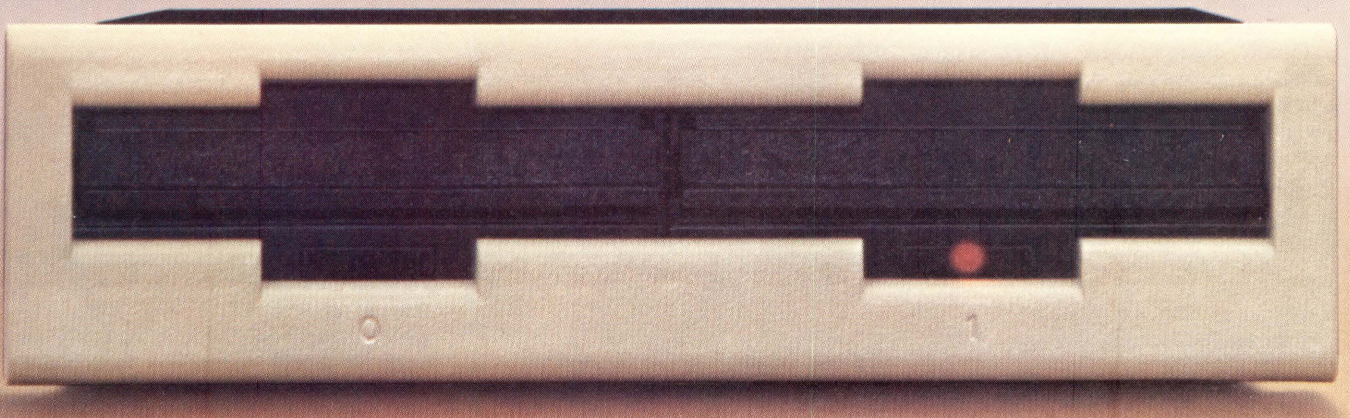

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CIRCLE 18 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

"Automated Design of Computer Based Systems" by Shawn Spilman (Nov 1981, pp 161-174), was exceptional but for one detail. Mr Spilman states that only raster displays can perform rubber banding.

We use the DVST display in the refresh mode to perform rubber banding as well as other functions generally attributed only to raster display performance. Arguments over this application vary. However, the fact is that it can be done successfully.

Henry Schoenemann
Gerber Systems Technology, Inc
South Windsor, Conn

To the Editor:

I feel I must point out the misleading aspects of the article, "Cartridge Transport Disc Backup," (Oct 1981, pp 141-146) by Darell Meyer. The most eye-catching piece of the article is Fig 5, a graph of dump time vs record size, using a single-record buffer. Why anyone would use a single-record buffer with a streaming tape drive is beyond me. Even a simple 2-track buffering scheme would permit Mr Meyer's chosen disk-tape combinations to keep the tape busy, and avoid repositioning completely. This would permit 30-ips backup in file management mode in 6 minutes, and 90-ips backup in mirror image mode in 2 minutes.

The memory requirement for this is 20k to 30k bytes, which would certainly be available on any system I can think of that would be likely to have a 10M byte Winchester disk.

Finally, many low cost start/stop tape drives have start and stop times significantly faster than 60 ms (or 0.60 ms, as given in Fig 4!), while retrieval requirements may demand the tape block size to be much smaller than a full track. These two factors can considerably increase dump time for a start/stop tape drive.

Glen Seeds
Systemhouse Ltd
Advanced Technology Div
Ottawa, Canada

The Author Replies:

Thank you for the opportunity to respond to the letter from Glen Seeds of Systemhouse Ltd. The point which Mr Seeds raises is exactly the message of the article. The article was intended to highlight problems that system designers need to be aware of, so that they can address them intelligently. In the text preceding the reference to Fig 5, it is pointed out that several buffering schemes, such as ring buffers, can be used to minimize dump time. Fig 5 was used to illustrate the effect of lack of sufficient buffering.

The start/stop time for quarter-inch cartridge uses DEI, PEREX, Tandberg, and Kennedy product specs as a reference. These vendors represent the majority of products offered in this class of products.

Hopefully this information will help to clarify Mr Seeds' comments.

Darell L. Meyer
Pertel Computer Corp
Woodland Hills, Calif

To the Editor:

Mr. Pasika's letter and Peter Rony's reply in the October 1981 issue (p 28) remind me of a recent experience with the 8255 in a multi-microprocessor system. I had used the 8255 in single processor systems for some time, but in this case I was caught by an 8255 idiosyncrasy. First, when the 8255 is reset, the ports are all switched to inputs, forcing the port pins to a high impedance state. At this time the output latches are cleared to logic zero. Second, if a port is subsequently programmed to be an output, the pins will go to logic zero.

If some other device is monitoring an 8255 pin during a local reset, it will see the high impedance state (equivalent to a logic 1) followed by the logic 0. This caused a problem in our system because the device connected to the 8255 output pin was not "informed" of the local reset and merely responded to the logic 1 seen during the reset period. The particular task was moved to an ordinary latch which could be maintained in a known state during reset time.

Bob Schuchman
Datagraphix, Inc
San Diego, Calif

To the Editor:

Mr Dmoch's comments (Letters, Nov 1981, p 24) on Terence M. Davis's article, "Powerful Graphics Tool Combines Refresh and Storage Capabilities," July 1981 pp 105-108, are well founded. I agree that raster, DVST, and refresh vector technology should be viewed as coexisting—not competing—technologies. Each will have optimum application niches for many years to come. Raster will dominate those applications demanding moderate resolution with lots of solid colors. Refresh vectors are best suited for moderately complex line drawings with lots of dynamics. DVST displays are best for very complex drawings with moderate dynamics.

Mr Dmoch is victim of a common error when he states that "vector refresh terminals can generate high resolution (4096 x 4096) displays." Resolution is defined as the ability to resolve adjacent points by some criterion, such as Rayleigh's. Mr Dmoch is probably referring to 12-bit DACs used both in the vector refresh terminals and in DVST terminals. While this is an important characteristic of terminals (it defines the quantization error and hence the jagginess of, say, a circle), it has nothing to do with resolution. The true resolution of vector refresh terminals is closer to 1000 x 1000. DVSTs operated in the storage mode have much higher resolution. This is due to the bistable nature of the device, which enhances the Gaussian spot into a sharp edge similar to a printed page. This, together with the absence of flicker inherent in DVSTs, leads one to speculate that storage displays should be superior, in terms of user fatigue, to both raster and vector refresh displays. Experiments designed to address this issue are underway at Tektronix and elsewhere.

Dr Carlo Infante
Tektronix, Inc
Beaverton, Ore

To the Editor:

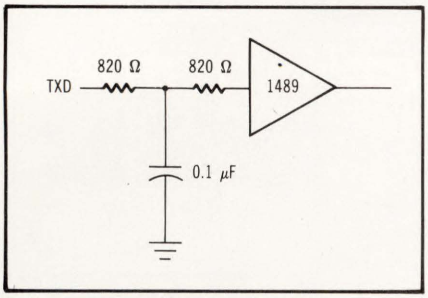
The article on LM-2, "the LISP machine" (Oct 1981, pp 38-40) was interesting, especially since this is obviously not a very accurate machine. The article says that in reply to 50!, it "fills the screen with hundreds of digits." Since 50! has only 65 digits (actually it equals 30, 414,093,201,713,378,043,612,608, 166,064,768,844,377,641,568,960, 512,000,000,000) there appears to be something wrong. Maybe it was printed out in binary? That would take 215 digits (I won't write it out).

Mark A. Sicking
Monsanto
St Peter's, Mo

To the Editor:

The article by L. T. Pearson, "Extending the Limits of an RS-232 Interface" (Sept 1981, pp 163-166) is good but neglects the effects of filter elements added by the manufacturers of RS-232 devices, who may have looked at that same capacitance limit. For example, the "simplified EIA" interface on the Teletype model 40 printer uses a 1200-pF capacitor on the RS-232 signal line. This cuts the available cable length in half unless the data speed is also kept down.

Several months ago I had a similar problem with a modem, even though my cable was only a few feet long. I was developing a box to use a Racal-Vadic VA3451P modem with an Apple II+ and an SSM AIO interface board with automatic origination capabilities. When I tried to test by accessing a local computer dial-up facility at 1200 baud, the responses indicated that the system received garbage and refused the logging information. I then tried the analog loopback feature of the VA3451P. At 300 baud there were no errors in a test of an hour or so, but at 1200 baud errors in each line exceeded correct data returned. In order to check the modem, a factory test was run using the internal remote-controlled digital loopback with the report of perfect operation. Finally I looked at the transmit data line with my oscilloscope. I found the data integrated to a triangular waveform. Tracing the input circuit of the modem, I found that the data are received in the modem by a 1489 but that there is a low pass filter made up of a pair of 820-Ω resistors and a 0.1-μF shunt capacitor. Another call to the factory disclosed that the capacitor is correct. (See the Figure.)



The RS-232 drivers in the SSM AIO card are the same as Pearson's Fig 2. At 1200 baud the input filter integrated the signal to the extent that the voltage swings at the 1489 barely exceeded the standard ±3-V thresholds at the extreme peaks. The transition times (see Pearson's Fig 1) were the same as the bit length at 1200 baud—much greater than 0.04 T_{PD}. For driving true RS-232 inputs with cables there is nothing wrong with the circuit shown in Pearson's Fig 2, but it won't drive the VA3451P modem. At the expense of greater power dissipation, I shunted the 3.3-kΩ collector resistor with 2.7 kΩ; the errors at 1200 baud disappeared, but with little margin. Having both a 1489 and a 1488 in my control box I used a section of each to make a data signal buffer. With the totem pole output of the 1488 supplying charge to that 0.1-μF capacitor, operation has been fine for several months (with the exception of other modem failures).

I would term the driver circuit of Pearson's Fig 2 to be a "gentle" driver, in that it is current limited to have no more output capability than the RS-232 specification requires. That limited output might be a problem if an attempt were made to drive more than one RS-232 load at a time or a nonstandard input like the VA3451P. I believe one of the design features of the RS-232 standard is the slower transition, which is an effective limiter of radiated rf noise from the connecting cable. Conversely, using a power driver (such as the 1488 with a large capacitance in the receiving device) will accentuate the transition signal currents and accentuate the radiated rf interference. Since my clients and I tend to use computing devices at the same time we use radios and TVs, limiting the rfi makes us all happier. And we're even happier when the data transmissions are accurate!

Dr Gerald N. Johnson
Electrical Engineer
Ames, Iowa

The Author Replies:

Regarding Mr Johnson's question about the possible omission of filter element (ie, 1200-pF capacitor) in the cable length calculation, this capacitance would fall under the category of driver or termination capacitance. On p 166 I write, "Of course, driver and terminator capacitance must be *subtracted* from the total capacitance before determining the capacitance to be allocated for the cable." The article goes on to say that internal capacities of the driver or terminator are small enough to be considered negligible. However, designers or manufacturers can add any number of capacitor values at their discretion. Each value will modify the results, but the above sentence specifies how they are to be accounted for. They cannot be (and were not) neglected!

Other engineers have designed their own interfaces (drivers and receivers) with no capacitance added, and have exceeded the values stated in the article. This is possible; however, it is pointed out that though their interface worked, they were running outside the RS-232 standard and taking their chances—in this case on crosstalk between lines.

Any article has greater value when it provides a solution to a wide range of problems or is directed towards a large scope of applications. Thus, the intent behind my article was not to emphasize one particular design case, though one was used to serve as an example (no filter capacitors). The equations are general and handle the filter capacitor situation as described in the article. However, the addition of sophisticated filtering, beyond a simple capacitor, requires redefining the circuit model. This is an *exception* to normal use and beyond the intended scope of the article. Mr Johnson even states in his letter that the VA3451P is a *non-standard* input.

L. T. Pearson
Federal Aviation Administration
Pomona, NJ

To the Editor:

In your Nov 1981 editorial (p 11) you mentioned direct execution of high level languages, but forgot to add "user friendly" and "nonprocedural" to the qualifying adjectives. These adjectives represent a basic requirement for untrained computer—or maybe "information machine" is more appropriate here—users. With the advances in hardware and the concepts of dynamic machine architecture through accessible microcode, such languages are already on the way. PROLOG is an excellent example (a brief description appears in the article "PROLOG, in the Nov 1981 issue of *BYTE* magazine).

Keep up the good work with *Computer Design*—it's an excellent publication.

George J. Freidkin
Cord Consulting Co
University, Ala

The Editor Replies:

You are quite correct in calling attention to the "user friendly" requirements. I'm afraid I made the tacit assumption that "user friendliness" is a foregone requirement even for high level systems and languages designed for the accomplished programmer. There is nothing more frustrating to the experienced programmer than to have to wade through someone else's undocumented idiosyncrasies. Hopefully those days are drawing to a close and self-documenting and auto-prompting techniques will become the rule rather than the exception.

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CIRCLE 21 ON INQUIRY CARD

CAD/CAM systems and software supply cost-effective tools to keep pace with growing design automation needs

Today's products and production technologies require more complex design and design documentation for manufacture. As a result, the production cycle is stretched. Since getting products to market rapidly is the key to a company's economic success, automation of the design process has become essential. CAD/CAM equipment manufacturers are filling this need.

Two factors have been primarily responsible for the development of CAD/CAM systems as cost-effective tools for industry. These are lower cost, high performance computer hardware and sophisticated turnkey software packages for specialized applications. Some of the trends showing potential for the future are lower priced systems that provide all current capabilities, in addition to more powerful systems that will support all processing and data management requirements for product design, engineering analysis, and manufacturing operations.

Turnkey systems

CADMAX-1, from **Vector Automation, Inc**, Village of Cross Keys, Baltimore, MD 21210, combines vector stroke refresh display techniques with bit slice processor technology in a design and drafting system for electrical schematics. The system results from the company's attempt to produce a state of the art system at a price within reach of small and medium sized users.

The $66,200 turnkey standalone CADD system uses a 21" (53-cm) vector stroke refresh display with 4096 x 4096 resolution as its graphics terminal. A bipolar bit slice processor gives interactive users instantaneous response and can operate up to 56 workstations without degradation. Optional multicolor plotter and digitizer are also supported.

A data tablet enables entry of design and drafting commands; a separate 95-key ASCII keyboard allows text entry. Online storage is provided with a Winchester disk; a magnetic tape cartridge maintains a duplicate set of drawing files for backup, and is used to install software and communicate drawings to other like systems.

Another multistation system priced under $70,000 from **Drafting Dynamics, Inc**, 4615 Industrial Ave, Suite H, Simi Valley, CA 93063, the ON/LINE provides high performance CAD/CAM for PC boards and schematics. With this system, one drawing can be digitized, while another is being edited or designed on the CRT and the pen plotter is producing a third.

The minicomputer based system automatically produces drill tapes, photoplot tapes, wire lists, and parts lists. It can also perform schematic to PC board continuity checks. Software and symbol chip libraries are supplied with the basic system.

In addition, a bit slice graphics processor used within its Systems 52 and 54 has allowed **Nicolet CAD Corp**, 2450 Whitman Rd, Concord, CA 94518, to significantly cut prices of these systems. The multiprocessor systems use a 16-bit DEC LSI-11/2 controller and the Tektronix 16-bit bit slice processor with 128k bytes of onboard memory.

System 52, built for high speed digitizing, is constructed around the Tektronix 4052 desktop computer with a high resolution 11" (28-cm) direct view storage tube display, integral keyboard, magnetic tape cartridge drive, and joystick. A DEC LSI-11/2 processor, two dual-density floppy disks with DMA controller, and 36" x 48" (91- x 123-cm) digitizing tablet complete the $37,465 system.

Built around a Tektronix 4054 with 19" (48-cm) display and thumbwheel driven crosshair cursor, the System 54 has been reduced in price to $44,965. The high resolution screen on this unit allows complex drawings to be panned or specific details to be zoomed in. Layout elements are automatically positioned on the grid as specified, permitting rapid, accurate component by component design. Layers of the drawing can be displayed together or separately; all layers are corrected simultaneously when a change is made.

Graphics processors

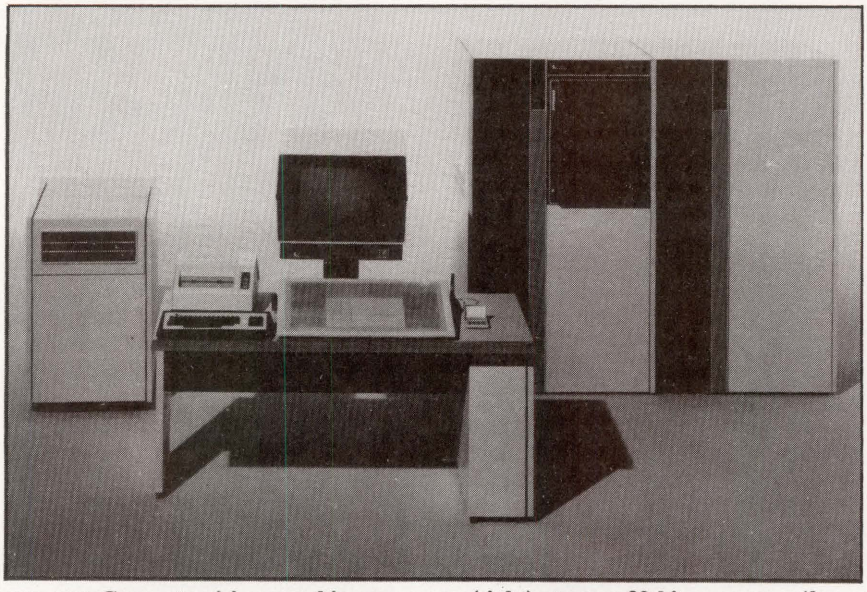
Claiming to extend turnkey CAD/CAM systems into interactive engineering analysis, analytical processing unit (APU) from **Computervision Corp**, 201 Burlington Rd, Bedford, MA 01730, supplies computer power and processing architecture necessary for execution of computationally complex analytic programs such as finite element analysis, kinematics, and advanced printed circuit and integrated circuit routing packages.

An extension of the distributed processing architecture used in the Designer V, the 32-bit cache based processor has an integral floating point accelerator. It supports interactive analysis functions without degrading graphics performance.

Running the CVMOS virtual memory operating system, the processor supports programming languages that include FORTRAN 77/66, PL/1, and Pascal. Thus, users can integrate existing analysis programs and develop their own analysis software. Hardware and software elements of the system are fine tuned to specific CAD/CAM requirements.

The APU can be shared by up to eight CGP-200X central processors. This multiple

(continued on page 32)



CGP-200X Computervision graphics processor (right). APU, a 32-bit processor (far right), attaches to the CGP-200X, and provides computer power and processor architecture necessary for complex analysis programs. Both are integral part of Designer system that includes monochromatic and color raster workstations (center) and disk storage modules (left).

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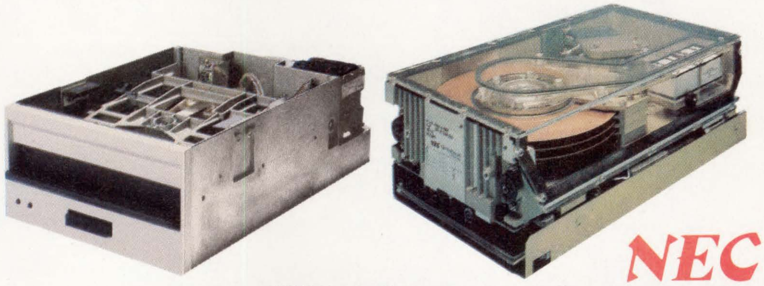

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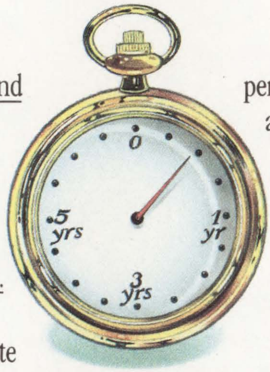

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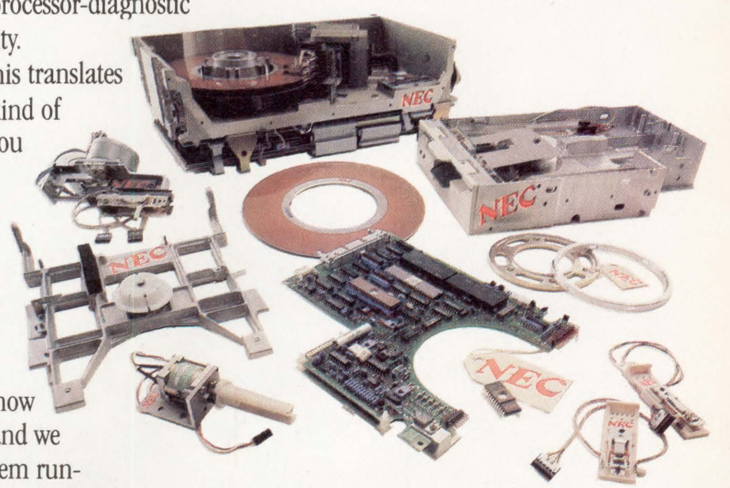

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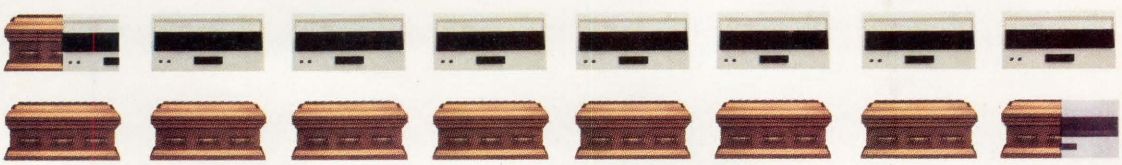
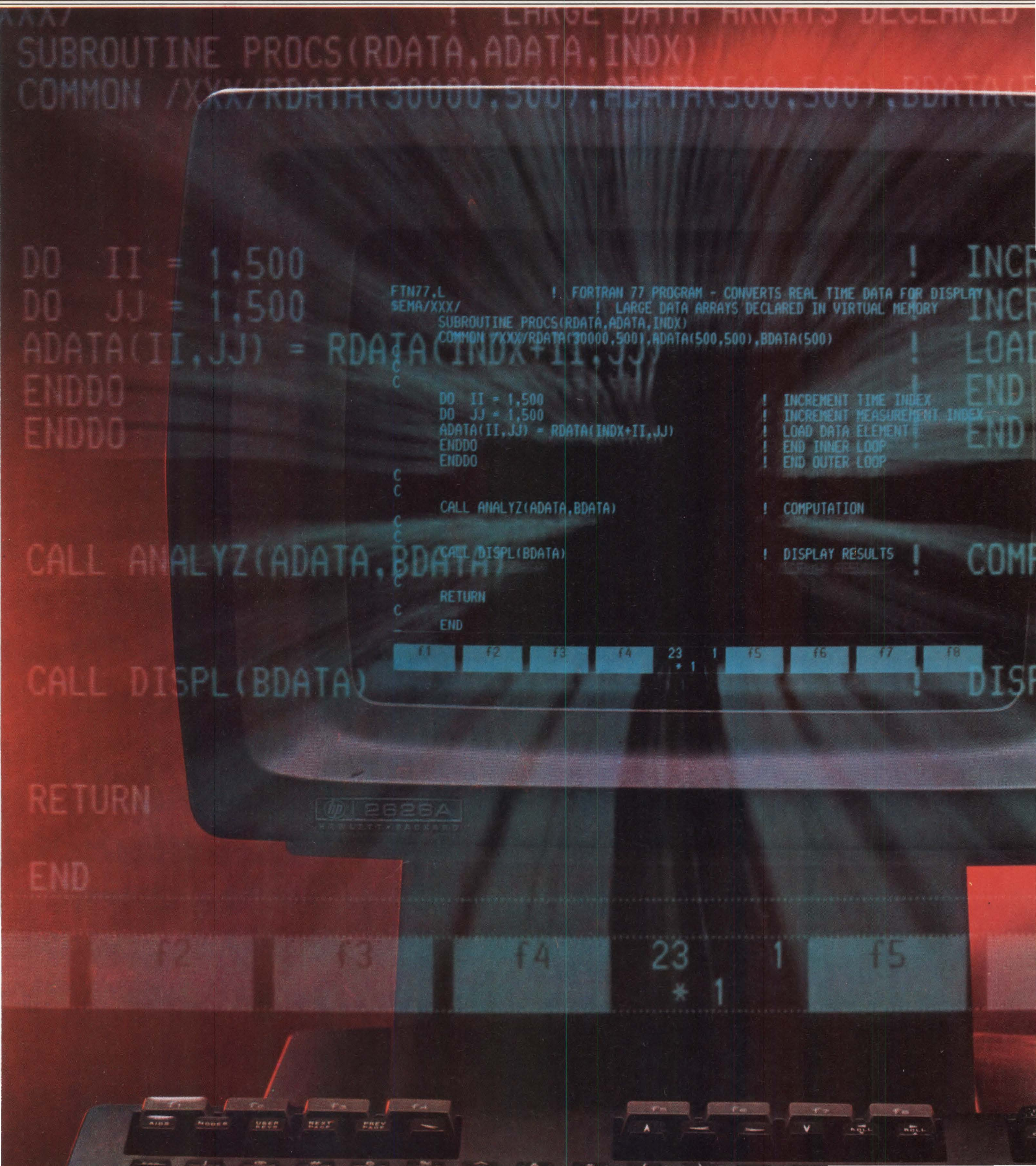
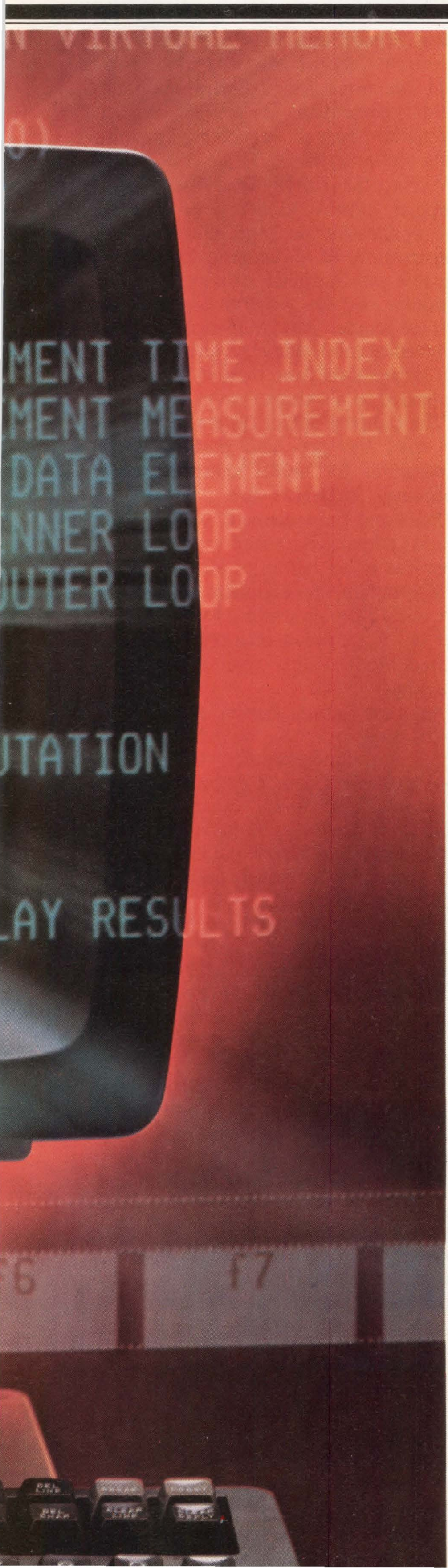


CIRCLE 22 ON INQUIRY CARD

The new HP you'd think you were



1000 Model 65: sitting at a mainframe.



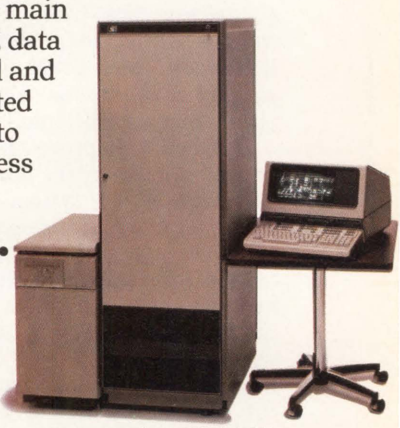
Now you can tackle your large applications without breaking your budget. That's because our new HP 1000 Model 65—with a powerful real-time operating system and advanced memory management scheme—can handle jobs that previously required a mainframe computer. And do it at a minicomputer price.

Extended code space for programs. Virtual memory for data.

The key to the Model 65's new power is our enhanced RTE-6/VM operating system. Using an Extended Code Space segmentation scheme, RTE-6/VM lets you compile, load and execute large programs (approaching 25,000 lines of FORTRAN code), or convert them from other computers. And because RTE-6/VM uses a virtual memory design, these programs can access a huge 128 megabytes of data—transparently. So your programs can virtually be as large as the application requires.

Getting a head start on development.

A Model 65 development system gives you maximum HP 1000 power in one fully-configured package. You start with RTE-6/VM, floating point hardware and one megabyte of high-performance main memory. You also get our award-winning IMAGE data base management system; FORTRAN 77, Pascal and Macroassembler; a 16 Mb fixed disc with integrated tape cartridge; and a powerful graphics terminal to use with our Graphics/1000-II software. All for less than $65,000.



A one megabyte Model 65 development system is priced at under $65,000.

Third parties play a part.

If you're a software supplier, just picture *your* big applications on the Model 65. The cost of the "total solution" to your customer will be significantly lower. Which means more systems can be sold. And that's just the idea behind our new HP PLUS program, where selected software suppliers team up with HP to bring competitively priced, quality solutions to the marketplace. And if you're an OEM, our volume discount schedules make these systems even more attractive.

For more information, call your local HP sales office. Or write Hewlett-Packard, Attn: Joe Schoendorf, Dept. 12128, 11000 Wolfe Rd., Cupertino, CA 95014.

You can see the HP 1000 working on factory applications at Productivity '82. Watch your newspaper for more details.

When performance must be measured by results.

HEWLETT PACKARD

Price U.S.A. list; subject to change without notice.

22201
HPTC-70

CIRCLE 23 ON INQUIRY CARD

processor architecture allows configuration of systems having more than 50 workstations. The processor is priced at $150,000 and will be available in the second quarter of 1982.

In addition, CGP-200X extends the CGP-200 functionally distributed processing computer to improve performance and functionality without making existing hardware, software, and data bases obsolete. The machine quadruples the size of the virtual memory space, supplies eight times the physical memory capacity (8M bytes), and expands the amount of microcode devoted to CAD/CAM. Online disk capacity and disk channel bandwidth have also been increased. Integral remote diagnostic capability allows system problems to be diagnosed from remote sites.

Applications software

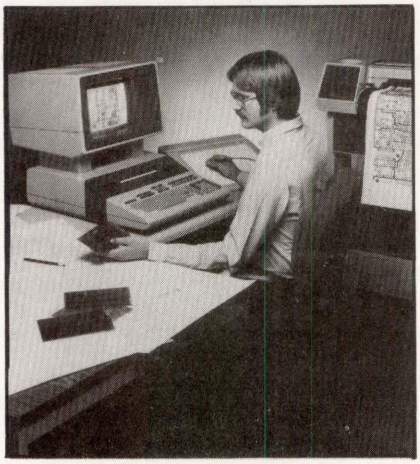
Among recent software releases aimed at the CAD/CAM area are automated packaging and placement and 3-dimensional geometrical design packages that unite design and manufacturing through a common data base. Also available from **Applicon Inc**, 32 Second Ave, Burlington, MA 01803, is a CADAM package that runs on a minicomputer rather than a mainframe.

Designed to improve routine completion of printed circuit boards designed on a CAD/CAM system, Applicon's packaging and placement program automates the time consuming, error prone tasks of packaging and placing components and back annotation. This significantly reduces keying errors, since schematic text associated with a design need not be manually entered. It also cuts the time required using manual methods.

Back annotation, the process of recording pin and component assignments back to the original schematic drawing, is also handled automatically. This cuts the time required from hours to minutes.

Compatible with 9845 desktop computer systems, EGS/45 software from **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303, offers general drawing, PC board layout, and schematic drawing capabilities. The package, created for use by electronic circuit and PC board designers, increases individual productivity, saving up to 50% of the time required using manual methods, and is a key element in HP's concept of a manufacturer's productivity network.

General drawing core, schematic drawing, and PC board layout modules are available individually or as part of



PC board schematics can be generated using the Hewlett-Packard EGS/45 engineering graphics system. Saving up to half the design time required for manual methods, the system runs on an HP 9845 desktop computer.

the package. Required to use the other modules, the general drawing core is used to create engineering drawings from primitive elements. Primitives and library parts are viewed on the CRT. Screen editing commands allow objects to be copied, moved, or repeated.

Interactive layout or digitizing of 32″ x 32″ (81- x 81-cm) multilayer boards with 0.001″ (0.025-mm) resolution is supported by the PC board layout module. Tooling outputs for use in manufacturing are automatically generated, and users can obtain plots to verify layout accuracy, paper tapes to feed NC controlled drilling machines, and magnetic tapes to drive photoplotters.

The schematic drawing module produces electronic schematics and automatically generates materials lists. Appropriate library symbol modification also enables this software to produce other types of diagrams.

Modular structure of the system allows BASIC routines to be developed to process drawings created with any module in the package. Routines fit into the program structure and appear as just another module.

Hardware recommended for use with the package includes HP 9845C, assembly execution ROM, graphics tablet, drafting plotter, and mass storage device.

To extend graphics capabilities of its 4300 and 3081 computer systems in engineering and manufacturing areas, **International Business Machines Corp, Data Processing Div**, 1133 Westchester Ave, White Plains, NY 10604, offers two CAD programs and support for the CADAM system under the VM/370 operating system. The CAD packages, developed by Dassault Systemes of Paris, France, and Structural Dynamics Research Corp of Milford, Ohio, provide functions for 3-dimensional and solid geometrical conceptual design evaluation, as well as engineering modeling and analysis.

CATIA, Dassault Systemes' computer graphics aided, 3-dimensional interactive application package, allows direct construction of 3-dimensional objects on IBM 3250 graphics display systems. Modules include wireframe geometry, surface geometry and numerical control, polyhedral solid geometry, and kinematics. Design data from these modules can be passed to a CADAM system.

The CAEDS graphics system developed by SDRC has pre- and postprocessing capabilities for model generation and checking. Interfaces are provided to CADAM and finite element analysis programs; graphics output of user models is provided either before or after analysis. The program can significantly shorten the overall design process by evaluating key structural points on a computer generated model rather than a full scale mockup.

Another CADAM system allows users to offload work from mainframes onto midrange minicomputers. Offered by **Perkin-Elmer Corp, Computer Operations**, 2 Crescent Pl, Oceanport, NJ 07757, for use on its 32-bit minicomputers, this system, developed and used by Lockheed, has previously been available only on mainframes.

CADAM (computer graphics augmented design and manufacturing) is an interactive general purpose design and drafting system containing analytical design aids for use in 3-D design, design drafting, and NC parts programming. The system enables engineers to work in an interactive environment. Designs can be enlarged 100 times or more to permit the smallest details of a complex structure to be examined.

CADAM software ties design and manufacturing disciplines together through a common data base, thus permitting better communications between those functions. Perkin-Elmer's use of midrange computers in the distributed graphics system enables the full attributes of the system to be placed at the designer's desk, thereby enhancing engineering/design productivity.

Upcoming distributed graphics products supporting and enhancing CADAM

(continued on page 33)

will provide sufficient processing power to supply rapid interactive response. Both hardware and software products will be fully supported by the company.

Integrated service networks

Taking the user from concept to finished product, the ICEM approach from **Control Data Corp,** Box O, Minneapolis, MN 55440, integrates engineering and manufacturing products and services. It includes a library of engineering oriented application packages ranging from design, modeling, analysis, and drafting to mechanical and structural analysis and on to numerical control of machine tools.

Control Data's Integrated Computer Aided Engineering and Manufacturing (ICEM) program takes users from beginning concept to finished product. Here, CD/2000, an ICEM program, is used to create a crane gear for display on the terminal screen.

Integration of programs within a data library system serves as the "missing link" to CAD/CAM by allowing online storage and retrieval of huge volumes of data. Access to the data is provided through a workstation based on the Tektronix 4114-30 graphics terminal. Also important to the package is an initial graphics exchange specification (IGES) program developed to provide a common file structure for data generated by interactive design drafting systems. With IGES, all automated drafting systems have access to a shared data base maintained on computers at Control Data's Cybernet services network or on Cyber 700 series computer system.

In addition, a link has been established between Synthavision—the company's geometric modeling product—and CD/2000—its automated design and drafting system. This link facilitates online transfer of modeling data to the design and drafting function.

A joint venture involving General Electric Co and Structural Dynamics Research Corp, **GE-CAE International, Inc,** 300 Techne-Center Dr, Milford, OH 45150, aims to "close the loop" between technology and industry to increase productivity. Offering various CAE related computer services through a network of service centers, SDRC will provide the software link which, coupled with GE automation products, will provide an integrated system of design, analysis, and processing planning automation.

As the focal point of the SDRC computer aided engineering software system, SYSTAN automates the system analysis process. Allowing easy extraction of component and connector data from test results, finite element analysis results, and data banks, the software handles units and coordinate system compatibility automatically. Graphics capabilities, including color display, provide versatility in displaying verifying components and system models. Forced response results and animated mode shapes can also be displayed.

Other products in the software system are the graphics system for finite element model preparation and results display, FRAME for general finite element analysis, IMP for analysis of mechanisms, MODAL-PLUS for modal analysis from experimental data, and FATIGUE for fatigue life estimation from experimental or analytical strain data.

System elements are available on DEC and IBM systems and those of some other manufacturers. Products will be distributed through General Electric Information Services Co and through a network of Productivity Centers where users will be able to experiment with CAD/CAM and CAE.

—Peg Killmon, Senior Editor

Vector Automation, Inc	—Circle 240 on Inquiry Card
Drafting Dynamics, Inc	—Circle 241 on Inquiry Card
Nicolet CAD Corp	—Circle 242 on Inquiry Card
Computervision Corp	—Circle 243 on Inquiry Card
Applicon Inc	—Circle 244 on Inquiry Card
Hewlett-Packard Co	—Circle 245 on Inquiry Card
IBM Corp	—Circle 246 on Inquiry Card
Perkin-Elmer Corp	—Circle 247 on Inquiry Card
Control Data Corp	—Circle 248 on Inquiry Card
GE-CAE International, Inc	—Circle 249 on Inquiry Card

INTEGRATED CIRCUITS

Products and services offered for voice synthesis applications

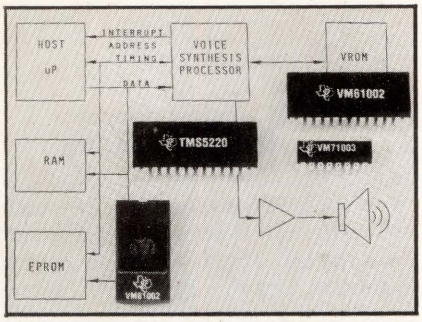
Texas Instruments Inc has announced several additions to its line of speech technology products, including a speech development system (SDS), a speech evaluation board, upgrades in its existing TMS5100 and TMS5200 series voice synthesis processors (*Computer Design,* July 1980, p 166), and three additional speech ROMS.

SDS is intended for OEMs who wish to design synthesized speech vocabularies into their proprietary products. The system enables users to develop, analyze, and edit custom vocabularies. Two major hardware components are used. The MultiAMPLUS™ development system is a high performance, general purpose minicomputer that provides a computing environment for speech-data processing and utility execution. The second component is the data collection processor. It is an intelligent slave to the minicomputer, and provides linear A-D and D-A conversion of 12-bit accuracy. It also includes the necessary anti-aliasing and signal reconstruction filters that are required to collect and play back speech signals.

Users of SDS can record, store, and edit any kind of linear predictive coding (LPC) speech. The system has complete facilities for both analysis and constructive synthesis, and can interactively edit text, phoneme, allophone, and LPC data. It will generate speech from text, phoneme, or allophone inputs. Friendly system software leads users through the vocabulary generation process. SDS allows users to control every step of vocabulary development from initial script generation to programming EPROMS.

System pricing varies, dependent on the hardware included. A typical configuration including the development system, data collection processor, and SDS software costs $97,630, with delivery 60 days ARO. Companies who cannot justify the cost of SDS, do not have staff or experience, or do not have extensive requirements in vocabulary development, can avail themselves of SDS capabilities at Regional Technology Centers (RTCs) established by the company in Chicago, Ill; Boston, Mass; Los Angeles and Sunnyvale, Calif; and Atlanta, Ga. Another RTC is scheduled for opening in Dallas, Tex early in 1982.

(continued on page 34)



TMSK202 speech synthesis evaluation kit is used to evaluate TI's speech synthesis products for 8- and 16-bit microprocessor based systems. Voice synthesis processor can produce male, female, and children's synthesized speech as well as variety of sound effects. EPROM and two VROMs store total of 256 words, phrases and sounds. These can be linked together by user and output to amplifier as synthesized speech.

TMS5100 series evaluation board is a handheld battery operated unit designed for engineers and customers who want a standalone demonstration of synthesized speech quality. Through its integral speaker it can produce one to eight phrases, selectable via a rotary switch, at the touch of a button. The board is used to evaluate and demonstrate the 4-bit 5100 series voice synthesis processors and to provide a basic understanding of the company's voice processors.

Except for a power supply, the board does not require any external hardware or software. Components include the TMS5100 voice synthesis processor and the TMS2532 32k-bit EPROM that stores eight phrases of synthesized speech, each of about 3-s duration. A wide range of phrases can be selected from TI's speech library and stored in EPROM. Suggested single-quantity price of the evaluation board is $99. It is available from authorized distributors.

Additional ROMs and larger vocabulary have expanded the TMSK101A and TMSK202 speech synthesis evaluation kits. Increasing the number of ROMs from one to three offers a larger choice of words. The TMSK101A contains 289 words or phrases, and the TMSK202 has 241 words or phrases plus 15 sounds.

Compatible with control logic or most 4-bit microcomputers, the TMSK101A contains a TMS5100 voice synthesis processor. This single-chip synthesizer produces good quality speech at a low (1200-bps) data rate. The kit also includes a VM61001 vocabulary ROM (VROM) containing 204 phrases, a VM71001 with 50 phrases, and a VM71002 with 35 phrases. Each item in the EPROMs can be individually accessed and concatenated to form phrases and sentences.

Kit TMSK202 evaluates voice synthesis capability on 8- or 16-bit microprocessor based systems. It contains a TMS5220 voice synthesis processor, VM81002 EPROM with 15 sounds, VM61002 ROM with 206 phrases, and VM71003 with 35 phrases. The latter ROM incorporates female synthesized speech. The kit's onchip FIFO buffer allows speech to be held in the host microprocessor or stored in a custom ROM.

Both kits use the LPC technique; both speech synthesis processors incorporate a 10-stage lattice filter that electronically simulates the human vocal tract. The kits implement the filter with an array multiplier that performs 200k multiplications/s to accurately generate up to 10k speech samples/s. Furnished with documentation for implementation into various applications, the kits are available for authorized distributors. Prices in quantities of one to four are TMSK101A, $45, and TMSK202, $60. Discounts are applicable for larger quantities.

Three devices have been added to the company's series of VROMs, which store standard synthesized speech vocabularies. VM61003 stores weather related words, VM61004 words dealing with military applications, and VM61005 words relating to avionic equipment and conditions. Suggested distributor pricing for each of the three VROMs in single quantity is $11.65. **Texas Instruments Inc, Central Literature Response Center (SC-346)**, PO Box 202129, Dallas, TX 75220.

—Jim Hughes, Senior Editor

Circle 250 on Inquiry Card

Bipolar linear arrays handle high output current

A series of 14 bipolar linear array devices was recently introduced by Micro-Circuit Engineering (MCE). Called UniRAYs, the devices are fixed component arrays, to which metal interconnect is added, producing a custom circuit. Arrays are supported by a design program that enables a circuit designer with little or no IC design experience to design a custom IC. These designs are completed in a few weeks at a cost lower than that of a full custom circuit. Preprocessed arrays are stocked in the factory with transistors, resistors, capacitors, and gates defined. MCE then connects these components as indicated in the customer's layout. Normally, the customer does the design and layout, but if requested, the company will do both (or just the layout) at a nominal charge. Ten of the recently announced parts are improved 20-V versions of A20 standards. One part is an improved version of Interdesign's 40-V MOD. Three of the devices, one 20-V part and two 40-V parts, are proprietary linears.

The company is claiming a significant performance increase as a result of N+ sinker diffusion fabricating. This process results in a low-value saturation resistance that gives the user a choice between higher output current or lower saturation voltage and reduced power dissipation.

With the increased capacity for output current, typically 50% greater than that offered by industry standard parts, the series meets industrial/process control, instrumentation, medical electronics, and military equipment requirements.

The three unique and improved bipolar arrays are the 20-V A20WS, and the 40-V A40AS and A40BS. The 20-V array has 464 components on a 117- x 102-mil (2.97- x 2.59-mm) die and 24 bonding pads. Active components include small signal and medium current npn transistors, in addition to lateral dual-collector and vertical pnp transistors. Total diffused resistance is 443 kΩ with 200-Ω to 3.6-kΩ capacities. There are also ten 30-kΩ pinch resistors. The 40-V A40BS has 218 components, including small signal, medium current, and common-collector npn transistors; lateral single-collector and vertical pnp transistors; and Schottky diodes. Total diffused resistance onchip is 161 kΩ. The 40-V A40AS has 245 components, including small signal and medium current npn transistors; lateral quad-collector, lateral 6-emitter, and vertical pnp transistors; and diffused and pinch resistors. The total diffused resistance is 237 kΩ.

These semi-custom ICs can be packaged in a variety of housings. Offerings include ceramic and plastic DIPs, ceramic side-brazed DIPs to TO-92 plastic, ceramic flatpacks, metal flatpacks, multilead metal cans, TO-66, TO-3, and T-220 power packages. The package variety covers 3- through 40-lead requirements.

UNIDES is the company's array development and evaluation system. UNIDES is a self-prompting IC design program. For example, a UNIDES breadboard consists of a printed circuit board mounted in a supported fixture. It contains a silk screened geometrical layout that corresponds to a particular worksheet. The breadboard has monolithic IC components in discrete form ready for interconnection by the user with a set of patch cords provided. It also has an onboard tester to check performance of the kit parts. **Micro-Circuit Engineering Inc**, 1111 Fairfield Dr, West Palm Beach, FL 33407. Circle 251 on Inquiry Card

Vincent van Gogh would have given his left ear for an AED512 graphics terminal.

To impress his young paramour, van Gogh cut off a piece of his right ear. He simply couldn't live without love. Nor could he live without the vibrant colors of his craft—which is why he'd have given his *left ear* for the powerful graphics and imaging capabilities of the AED512.

This intelligent, full-color raster graphics terminal would have given van Gogh the purity and intensity of color he demanded—with a palette of 16.8 million hues. The ability to display 256 colors simultaneously. *Plus* two serial interface ports. Half-second image transfers by DMA. Emulation of the Tektronix 4010 family. And a price tag even an artist could afford.

Besides the striking self-portrait displayed here on the '512 screen, van Gogh would have been able to produce equal masterpieces in CAD/CAM, animation, business graphics, cartography and TV production.

He would certainly have joined our Graphics User Group to trade techniques with others in this growing colony of AED graphics masters.

You, too, can join the AED colony and create your very own masterpieces. With the AED512. Call or write us today for a free brochure, full technical specifications, and information about our 16 demo diskettes. Advanced Electronics Design, Inc. 440 Potrero Avenue, Sunnyvale, CA 94086. Phone 408-733-3555 TELEX 357-498

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ADVANCED ELECTRONICS DESIGN, INC.

CIRCLE 25 ON INQUIRY CARD

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IMOX™ is our advanced ion-implanted, oxide-isolated process. It shrinks the space between transistors, cuts capacitance, and decreases size.

Thanks to IMOX we've got 16K PROMs that can do 35ns, very fast registered PROMs that use a third of the space and half the power of two-pack solutions, the industry's first 4Kx4

CMOS double-metal level array fabricated in 5″ wafers

SLX 6320 and SLX 6360 are 2000- and 6000-gate arrays, respectively, fabricated in 2-level metal N-well silicon gate CMOS technology. The first of National Semiconductor's SLX family, the devices are designed to replace bipolar TTL parts. More than TTL compatible, the arrays have ac and dc characteristics that match or exceed the performance of the 74LS family. Output buffer current and capacitive drive (8 ns for 50 pF) characteristics are the same as for the 74LS family. The input buffer, with its 4-ns propagation delay, performs better than the input buffers on the 74LS parts.

The first members of the new gate array family will be fabricated with 3-μm line widths. The 2000-gate 3-μm array with an internal propagation delay of 2 ns is due for sampling in the first half of '82; the 6000-gate 3-μm array, also with a 2-ns delay, should be available in the second half of this year. A 2000-gate 2-μm part with a 1-ns delay is due the latter part of this year. Fifty-six 3-state I/O buffers and 56 input buffers are onchip. Packaging options include 124-pin plastic and ceramic area-grid pinned packages, with leads on a 100-mil (0.3-cm) grid.

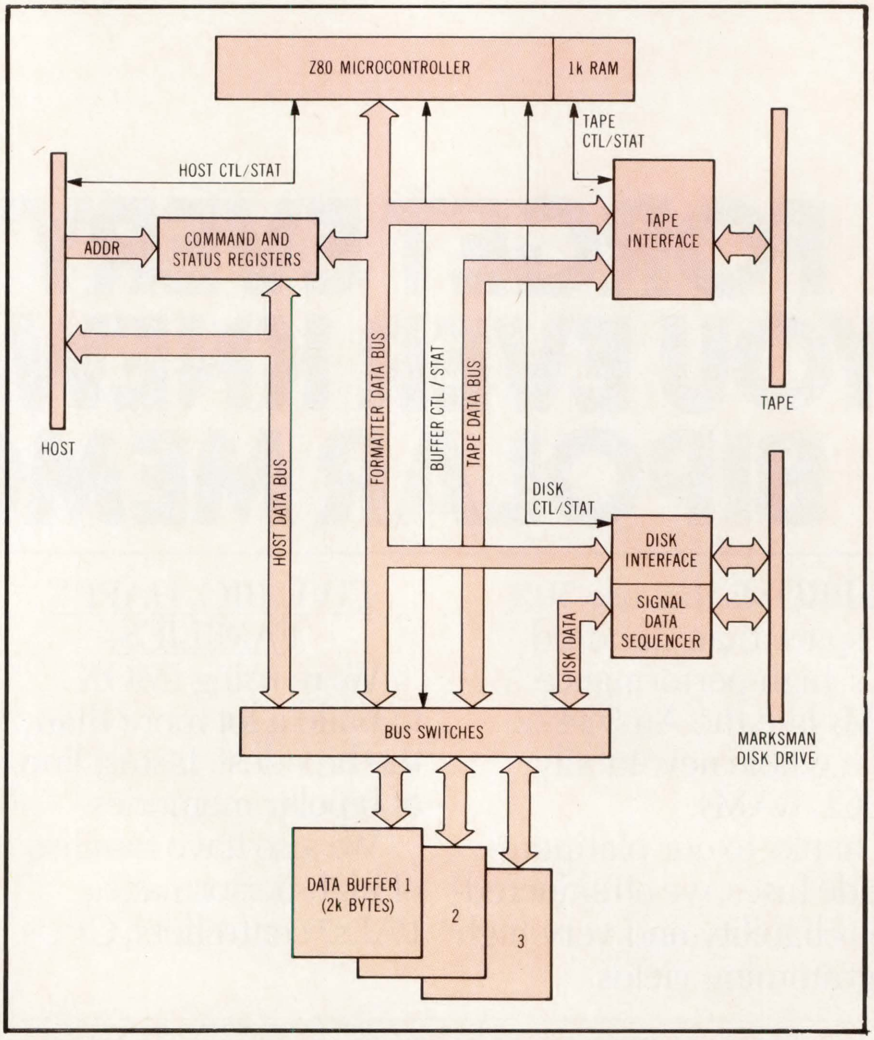
Power dissipation in the gate arrays is a function of the average switching frequency of the gates used. With these arrays, the typical internal gate power dissipation is 20 μW/MHz of switching frequency. The resulting power dissipation is typically under 400 mW for the 2000-gate array and under 900 mW for the 6000-gate array. Standby power will be less than 1 mW.

Array performance is a result of the processing technology: CMOS, double-metal, and 3-μm line widths. CMOS means low power. The two layers of metal maximize circuit speed by eliminating delays associated with poly interconnect resistance. Dry plasma etch techniques, which are used extensively throughout the process, achieve the 3-μm line width. Small line widths are necessary to make the high current and capacitive drive output buffers practical. Previously, they were impractical because the transistor area required to obtain a given transconductance is proportional to the square of the gate length, ie, a 5-μm gate length transistor is three times as large as a 3-μm gate length transistor. An integrated CAD system including logic simulation, test generation and grading, and automatic placement and routing will support the gate arrays. Turnaround time from logic design to sampling is estimated to be 12 to 14 weeks.

To produce the gate arrays, the company is installing two 5″ (13-cm) VLSI lines for wafer fabrication. One of the new 5″ wafer fab lines will be used for the fabrication of CMOS gate arrays; the other will be a 5″ bipolar line to manufacture ECL arrays. **National Semiconductor**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

MEMORY SYSTEMS

Disk/tape formatter with selective file backup allows host access



T series disk tape formatter. Host interface for single-board device requires eight data lines, four address lines, and three control lines (read/write/reset).

Century Data System's Marksman T series formatter controls one or two Marksmen disk drives of 20M to 160M bytes and up to four 30- or 90-ips Archive, Cipher or DEI intelligent 0.25″ tape drives. The disk controller, tape controller, and host interface are on one PC card. Combining these features on one card benefits the host system in three ways: increased data transfer rates, offline backup and restore capability, and simplicity in the host interface.

The formatter can support data rates to the host of up to 2M bytes/s burst and 500k bytes/s continuous. 10M bytes can

(continued on page 42)

8-CHARACTER DRIVER/DECODER.

FIRST 8-CHARACTER ALPHANUMERIC LED DRIVER/DECODER.

There's an exciting new attraction in single-chip display drivers: the ICM7243. The first 14/16 segment alphanumeric 8-character LED display driver/decoder.

The ICM7243 has the award-winning features you expect from Intersil. Like an on-board ROM for generation of 64 characters (eliminating additional PROMs and ROMs). Full microprocessor compatibility, accepting the popular six-bit ASCII input. Elimination of external components for direct driving of multiplexed displays. Cascadability to 16 or 24 characters without additional hardware. And, of course, at a matinee price — only $8.25 in 100s.

FIRST TRIPLEXED LCD DRIVERS.

Intersil has an LCD show-stopper too: our ICM7231 series: The world's first family of single-chip, multiplexed alphanumeric LCD display drivers. The ICM7231 series uses Triplex technology to drive three segments per pin instead of just one. So it outputs much more information — controlling four or five alphanumeric characters or eight to ten numbers, plus 16 to 20 addressable indicators. Starting at just $5 in 100s.

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LED Display Driver/Decoders				
Multiplexed	ICM7243A/B	8-Character	16/14 Segment	6-Bit ASCII Input
	ICM7218	8-Digit	7 Segment	Parallel Entry Hexadecimal or Code B
Direct	ICM7212	4-Digit	7 Segment	Parallel Entry Hexadecimal or Code B
LCD Display Driver/Decoders				
Triplexed	ICM7231	8-Digit	7 Segment 16 Indicators	Parallel Entry
	ICM7232	10-Digit	7 Segment 20 Indicators	Serial Entry
	ICM7233	4-Character	18 Segment	Parallel Entry 6-Bit ASCII
	ICM7234	5-Character	18 Segment	Serial Entry 6-Bit ASCII
Direct	ICM7211	4-Digit	7 Segment	Parallel Entry Hexadecimal or Code B
Vacuum Fluorescent Driver/Decoders				
Direct	ICM7235	4-Digit	7 Segment	Parallel Entry Hexadecimal or Code B

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Dear Intersil:

Put my name in lights!

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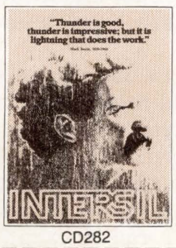


☐Also, please send me a Mark Twain poster from your "famous quotations" ad series.

CD282

be backed up in less than 2 min. The formatter offers true offline data backup and restoration through its transparent commands. Even with a previously commanded transparent backup or restore operation in progress, depending on user defined priorities, the host can access a disk. The host interface requires only eight data lines, four address lines, and three control lines (read, write, and reset). In addition, the formatter provides all signals necessary to support DMA and other control features for high performance systems.

The T series formatter has six basic functional blocks. The six blocks include an onboard microcontroller, a serial data sequencer, three floating data buffers, a host interface, a disk interface, and a tape interface.

A Z80 CPU, EPROM, RAM, and I/O control circuitry are included in the onboard microcontroller. It reads the command register, initiates host commands, and updates the status register at command completion. Because of the very high data transfer, the microcontroller does not transfer data, but initiates the transfer sequences through its I/O circuitry.

The serial data sequencer performs serial to parallel data conversion for disk data, and also does a CRC for errors on the serial data stream. It works together with the disk interface to handle disk data transactions.

With the three floating data buffers, the microcontroller handles all data transactions. To execute a data transfer in "bucket brigade" fashion, it can assign them individually to any of the host, disk, or tape data buses. First, it assigns an empty buffer to the source device. When the buffer is full, the microcontroller assigns it to the destination device and assigns the next empty buffer to the source device. The buffers rotate in this fashion, full ones from source to destination device, and empty ones back in a rotary fashion, until the transfer is complete.

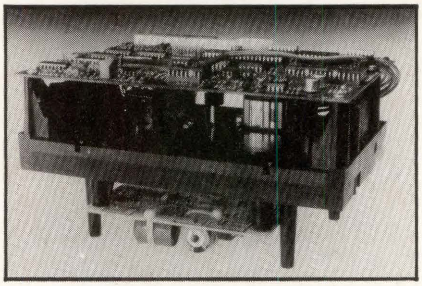
In addition to generating the necessary interface signals for the disk, tape, and host, the three interface blocks also provide terminations for inputs and drivers for outputs. Each interface includes a data bus.

The host interfaces to the formatter via a 16-byte command register, and a high performance discrete signal set. The host writes commands, command execution parameters, and data into the command register, but cannot read back what it has written. All read operations are from the status register, which transfers status information from the formatter to the host.

For high performance systems that require DMA and overlapped command capability, the formatter provides six additional status signals, which are the high performance signal set. These discrete signals include two direct command status signals, two transparent command status signals, and two DMA transfer signals. With these, the host can monitor and direct the transparent command status without reading the status byte. It can also generate interrupts upon command completion, and set up multiple-sector DMA transfers that will carry through to completion without further host processor intervention. The price of a formatter with cables, accessories, and a single 40M-byte disk drive is $3370. **Century Data Systems,** 1270 N Kraemer Blvd, Anaheim, CA 92803.

Circle 252 on Inquiry Card

45M-byte 0.25" streaming tape drive provides low cost Winchester backup

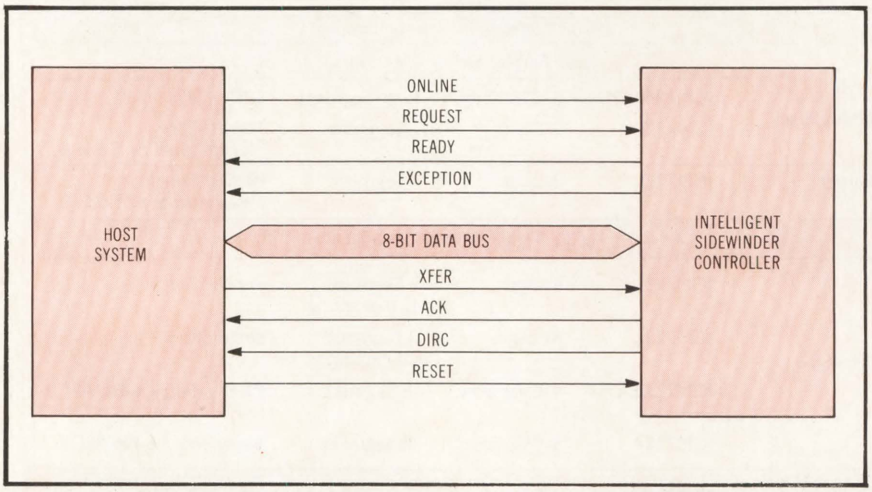


The Super Sidewinder 45M-byte (formatted) 0.25" streaming cartridge tape drive with a transfer rate of 90k bytes/s provides 8" and 14" Winchester backup at $20/M byte. Manufactured by Archive Corp, it can back up 160M bytes in 33 min with three media changes. Two models are available: basic and intelligent. Both provide high streaming at 90 ips and eliminate the inter-record gaps associated with traditional start/stop tapes. The drives use a serpentine recording technique that allows nine tracks of data to be written in both forward and reverse directions, without the need for rewind at the end of each track.

The recording head has two channels and a separate erase. Each channel has both write and read functions. The Super Sidewinder and the previously announced plug compatible Sidewinder are claimed to be the only 0.25" drives that erase with an ac signal, permitting light writing and high density recording with existing head technology. This advanced tape recording technique is usually found only in high performance 0.5" reel-to-reel tape drives.

The intelligent drive has a microprocessor based controller that relieves the host CPU of overhead functions such as buffering, tape positioning, error detection, rereading, tape formatting, file searching, and determining read status. The intelligent unit also minimizes the engineering hardware and software efforts required to interface the drive with the

(continued on page 44)



Intelligent 0.25" tape drive interface to host. Tape controller relieves host of such functions as tape formatting, data interrupt, error and file mark processing, and tape positioning. Automatic read-after-write error detecting, block buffering, and read retries are transparent to host. Should host be unable to meet streaming rate, drive will stop, reposition, and start again.

host. Multiple file marking allows the drive to be used for more than backup. The intelligent drive has been designed for a streaming environment at a recording density of 8000 bpi. The drive will fit into the same form factor as an 8" floppy disk drive.

Other key specifications of the drive include hard error rates of one in 10^8 bits (recoverable) and one in 10^{10} bits (nonrecoverable), commensurate with those of Winchester drives; a start/stop time of less than 300 ms; and a MTBF of 3500 power-on hours of typical usage. **Archive Corp**, 3540 Cadillac Ave, Costa Mesa, CA 92626.

Circle 253 on Inquiry Card

5.25" Winchester drive has fixed and removable disks

DMA Systems' Micro-Magnum 5/5 is a 5.25" Winchester with fixed and removable hard disks designed to meet OEM mass storage, I/O, and backup requirements. Both disks have a capacity of 6.75M bytes unformatted and 5M bytes formatted. The system is claimed to be the first 5.25" Winchester with fixed and removable disks. The removable disk is contained in a self-sealing cartridge. When the cartridge is inserted, a door actuator mechanism opens ports to allow the heads access to the media, and to filter the air in the cartridge. The sealing and air recirculation systems are so effective the air filter should never need to be replaced. The dual-drive cross-section is shown in Fig 1. Heads are positioned by a track following servo and linear motor positioning system. Notice that the heads are retracted into the head positioning system when not in use. The heads never touch the medium; they are retracted when the drive is not operating and float above the medium when the drive is operating. When the disk cartridge is removed the door automatically closes.

The disk in the cartridge contains prerecorded servo data that positions the heads when writing or reading. Regardless of temperature variations that can cause expansion or contraction of the mechanical portions of the storage system, positioning accuracy is maintained. This feature allows reliable data interchangeability/transportability and eliminates the need for mechanical alignment. The positioning system, the fact that the disk and heads never make contact, and the patented magnetic recording head assembly mean that the drive does not require any preventive maintenance.

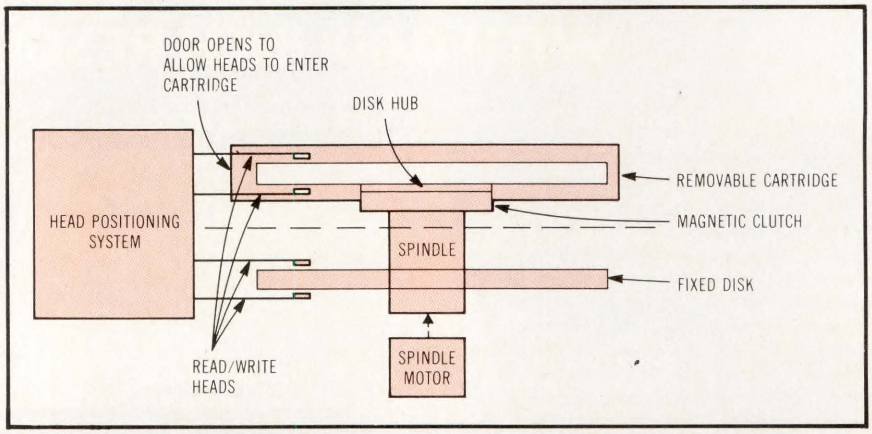


Fig 1 Cross-section of DMA System's Micro-Magnum fixed/removable drive. 0.75" (1.9 cm) high cartridge is removable medium for system I/O and file backup. Removable cartridge and drive compartment are automatically sealed. Servo information is embedded on disk, providing reliable cartridge interchange.

Along with Dysan and Seagate, the company has applied for an ANSI standard to cover the cartridge's mechanical characteristics. The cartridge is basically a standard 5.25" oxide disk clamped to a hub and enclosed in a plastic housing. The cartridge is designed, in conjunction with the receiving mechanism, to be loaded in only one orientation. It weighs 11 oz (0.312 kg) and is 5.394" x 5.551" x 0.748" (13.70 x 14.09 x 1.89 cm).

The form factor and mounting holes of the drive conform to the front panel

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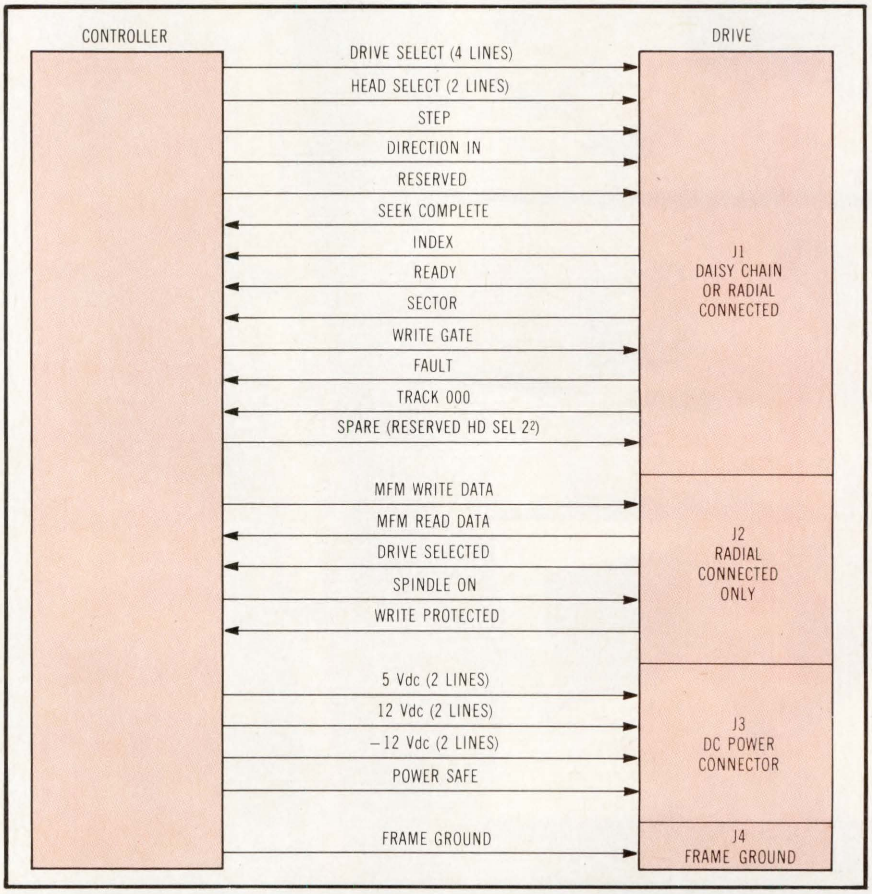
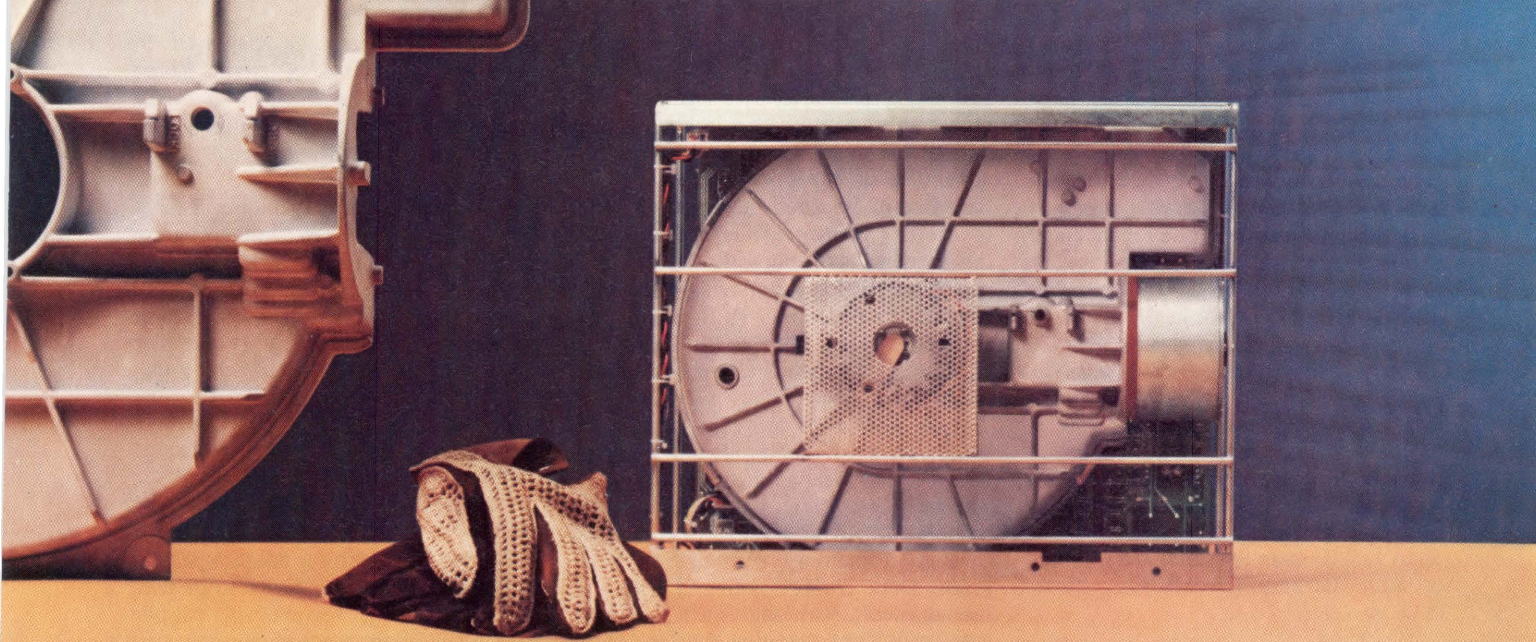


Fig 2 5.25" Fixed/removable hard disk drive controller interface system requires one standard controller. Drives can be daisy chained with other 5.25" Winchesters.

SYSTEM SUPERCHARGER



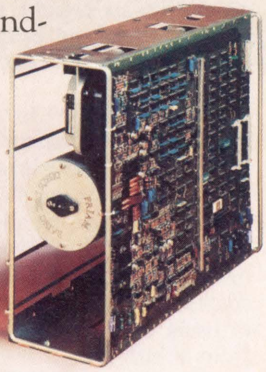
PRIAM's 158-megabyte Winchester Disc Drive

Supercharge your system performance with the 158-megabytes-per-unit capacity and fast voice-coil head positioning of PRIAM's DISKOS 15450. Multi-user and multiprocessor systems put demands on database size and response that only a high-performance Winchester disc drive like the DISKOS 15450 can satisfy.

PRIAM's 14-inch disc drive design has been proved in thousands of units shipped. It weighs only 38 pounds, and its brushless DC motor drive makes the DISKOS 15450 as mechanically simple as the turbocharger it resembles. No belts, no pulleys, no mechanical brakes. Compare the low price of the DISKOS 15450 with comparable drives. You'll agree that its cost/performance is far ahead of the pack.

All three PRIAM 14-inch drives, with capacities of 34, 68 and 158 megabytes, are only 7" x 17" x 20" in size, including the optional power supply. They all have the same 1.04 megabyte/second data rate, and operate from the same interfaces. Standard PRIAM or optional SMD, ANSI or SMART/SMART-E Interfaces make integration of these high-performance drives into your system quick and easy.

PRIAM 8-inch drives have capacities of 11, 35, and 70 megabytes, with the same interfaces and the same grand-prix performance characteristics as PRIAM's 14-inch models.



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CIRCLE 29 ON INQUIRY CARD

of a mini-floppy. At a length of 10.5″ (26.7 cm), it is longer than a mini-floppy drive, however. The added length is required to accommodate the linear motor. The drive is shock mounted horizontally, and requires only one controller. Other fixed/removable systems require two controllers; one for the fixed disk and another for the floppy, tape, or separate removable disk. The controller drive interface is shown in Fig 2.

Both disks have capacities of 454 tracks/in and 8617 bpi. Sector density is 256 bytes/sector. There are 32 sectors/track plus one spare. Transfer rate is 5M bps. Access times are 3 ms track to track, 40 ms average, and 10 ms settling. The disks rotate at 3443 rpm. Operational temperature range of the drives is 50 to 115 °F. **DMA Systems,** 325 Chapala St, Santa Barbara, CA 93101.

Circle 254 on Inquiry Card

MICROPROCESSORS/ MICROCOMPUTERS

Handheld computer packs desktop power in portable unit

Handheld, like a programmable calculator, Quasar's HHC (handheld computer system) contains a processor equivalent in power to that of a desktop computer, yet weighs less than a pound with keyboard and display. A built-in nickel-cadmium battery powers the unit, which with six peripherals including optional modem and printer fits comfortably in an attache case. Total weight is 22 pounds.

Based on the 1-MHz 6502 microprocessor, the system accommodates up to three 16k-byte plug-in ROMs or 4k-byte EPROMs, and 2k or 4k bytes of CMOS RAM. The I/O adapter allows users to add up to 48k more nonvolatile RAM. The basic unit and optional peripherals and adapters can operate from NiCd batteries, or using an external adapter/recharger, from ac current.

With optional adapters, the unit plugs directly into a television receiver for color graphics capability; connects with larger computers and data bases over telephone lines through an acoustic coupler; and attaches a 15-column thermal printer, additional memory, or RS-232-C compatible devices.

Design of the unit incorporates an advanced bus structure with extended addressing to 256 16k-byte segments. All peripherals work together in any combination. Use of interrupt driven I/O takes advantage of the processor's capabilities. Use of vectored interrupts instead of device polling techniques eliminates the burden that keyboard, display, and peripheral device monitoring tasks impose on the processor. Thus, the microprocessor can handle sophisticated applications programs and execute multiple tasks concurrently.

A memory bank switching technique supplies extensive read only and random access memory capability and flexibility. The technique permits the computer to combine data from both ROMs and RAMs through a memory continuation program. Data compression and memory management techniques such as Huffman coding and mapping and the use of permutation algorithms significantly extend capacities of the 160k ROM and 73k RAM. The mapping algorithm also permits the computer to use bidirectional data access to speed computing.

The TV display monitor adapter allows the computer to attach to any standard TV receiver. Sixteen lines of 32 characters each can be displayed in several combinations of color. Three color graphics modes display 64 graphics dots by 32 lines, 64 dots by 48 lines, and a selection of black and eight other colors.

Providing 65 keys including 3 programmable function keys and 4 program definable keys, the keyboard supplies 2-key rollover, auto repeat keys, and full cursor control. Function keys perform uniformly no matter what program is running. The three programmable function keys can be assigned to perform any sequence of keystrokes. Functions are selected through a series of nested menus; interactive prompts appearing on the 26-character LCD display guide users through the process.

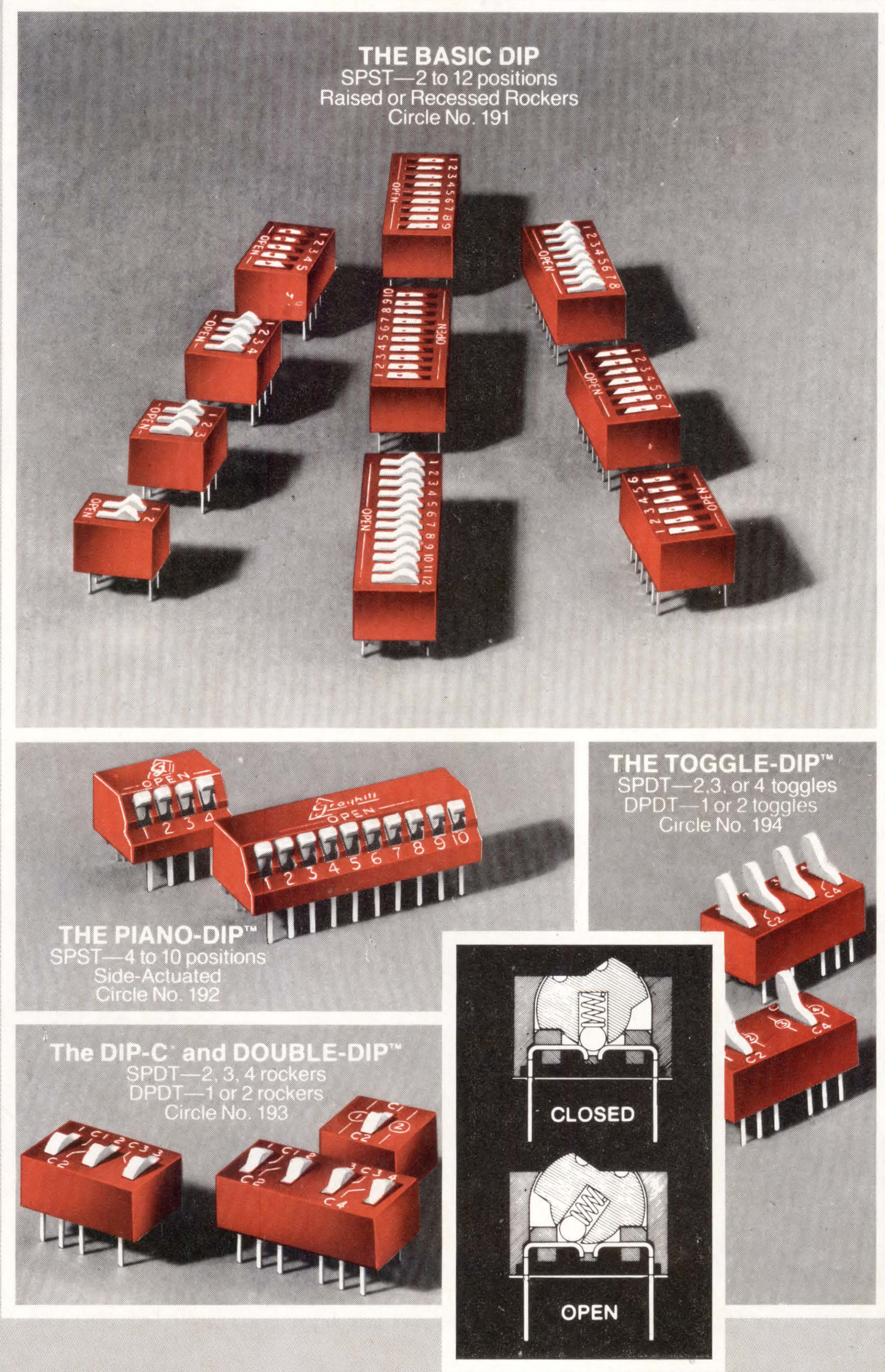
The RS-232-C interface adapter permits any RS-232 compatible device to be used with the system. An acoustic coupler with integral data modem gives the computer full communications capability from any telephone. The modem's options—110 or 300 bps, full- or half-duplex transmission, answer or originate mode, number of start or stop bits, and parity—are set and controlled by software. An automatic handshake routine used with the host allows users to regulate the rate of display.

The unit has a fully developed operating system and built-in applications.

(continued on page 50)

Handheld computer from Quasar puts processor, memory, printer, modem, and battery pack in an attache case. Programmable in SNAP and BASIC, unit connects to mainframes over telephone lines and to TV for local display.

GRAYHILL DIP SWITCHES: THERE IS A DIFFERENCE!



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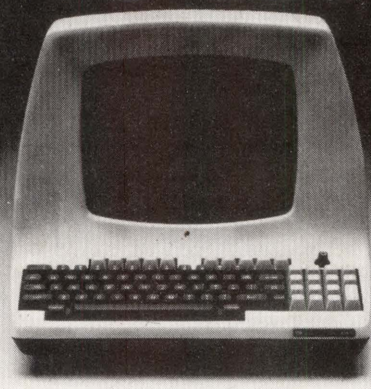

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Standard software includes a calculator, clock/calendar, and flexible file system. The system's programming languages include SNAP and Microsoft BASIC. SNAP, a Forth-like threaded language, can call any 6502 instruction allowing critical subroutines to be written in assembly language for fast execution. BASIC gives users access to existing programs.

A basic 4k-byte unit retails for $595. $150 buys an I/O peripheral device adapter; $55 an ac adapter. The acoustic coupler with integral modem sells for $275; the TV display interface for $295; and the RS-232 for $250. Additional memory is available at $225 and $325 for 4k and 8k modules, respectively. **Quasar Co, Div of Matsushita Electric Corp of America**, 9401 W Grand Ave, Franklin Park, IL 60131.

Circle 255 on Inquiry Card

Continuous processing system reduces programming costs by automating software development

Claiming to virtually eliminate computer downtime through its architecture, and to reduce the cost of programming with an automated software development system, DOSC designed the FailSafe system to provide fast response time and high throughput in an online transaction processing environment. This is achieved using a distributed microprocessor architecture that dedicates individual application processors to each function or task, and supplies a high speed data bus to link each processor to a shared data base.

Implemented in hardware as a distributed multiprocessor with continuous processing capability, the MT-85 computer contains multiple microcomputers that perform assigned tasks in parallel. Parallel organization supplies high processing capacity and rapid response time while simplifying system support software.

A large shared data base is accessible to each processor through the database manager, a 1.25-MIP processor running the FailSafe operating system that works concurrently with a 5-MIP database controller processor to provide controlled access to the data base. A second database manager, used only for backup, can be switched online automatically or manually.

The intelligent database controller processor supports CDC cartridge module drives (16M to 300M bytes) or any SMD type disk interface. The system contains two such controllers, both online, and provides for mirrored imaging of all writes, automatic

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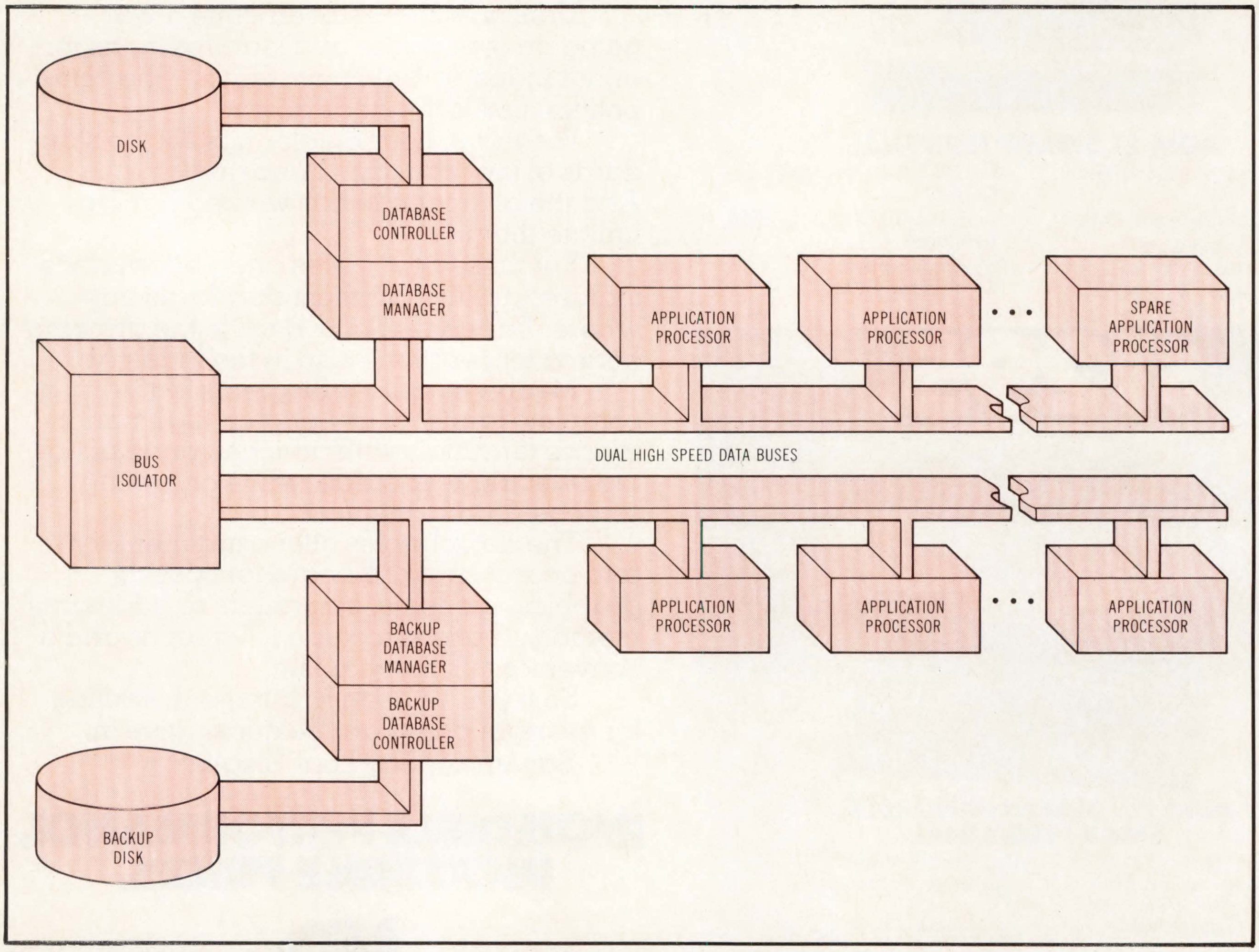
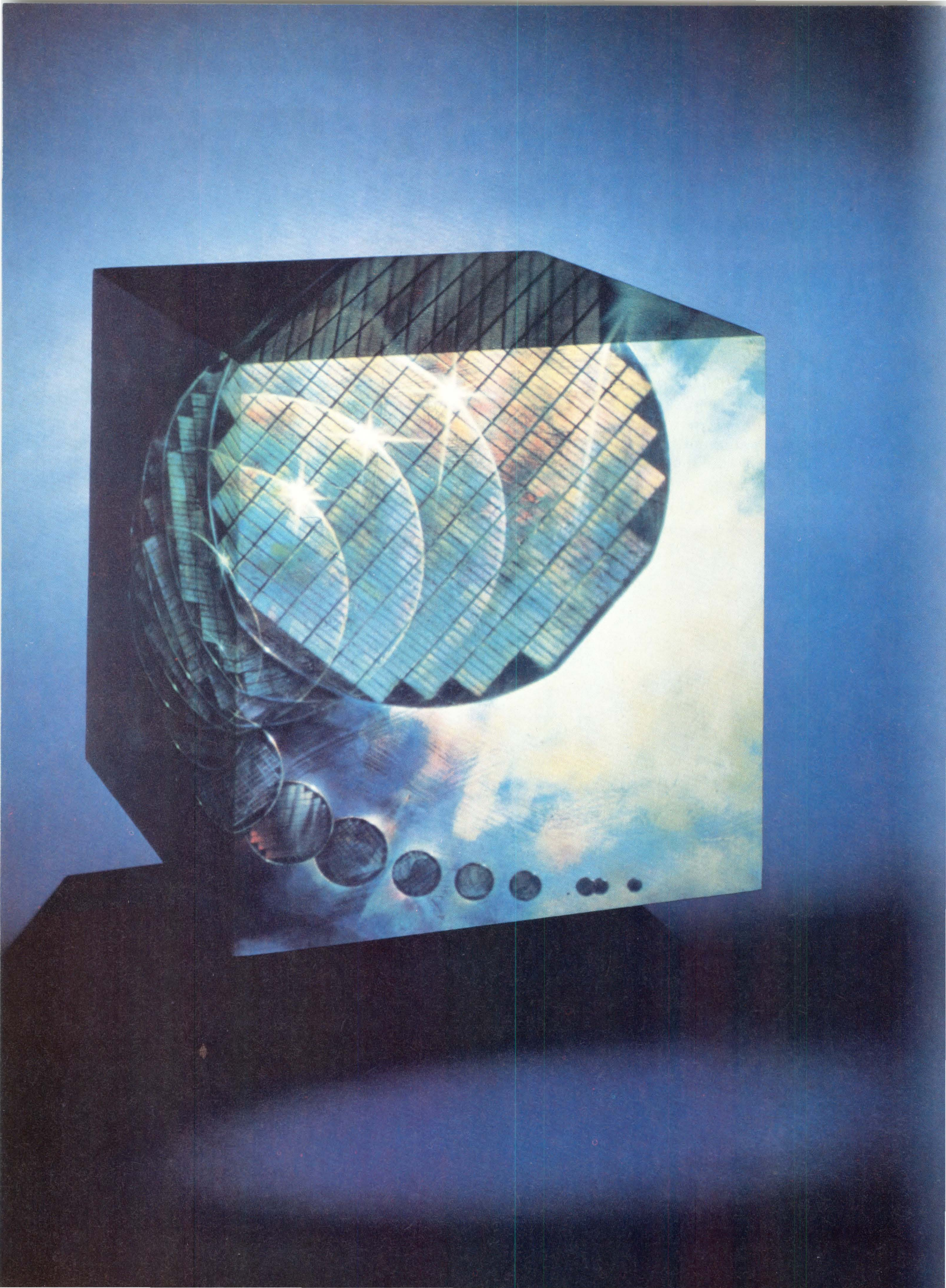


Hardware architecture of DOSC FailSafe computer includes microprocessor based application processors associated with each of up to 32 workstations. All are connected to central database unit through high speed data buses. Central unit includes dual database disks, dual database managers, dual disk controllers, and dual power supplies for failsafe operation.



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The IMS1420: High Speed. Low Power. Available Now.

The VLSI technology leader in 16K static RAMs introduces another industry first. Organized 4K x 4, the IMS1420 offers a chip enable access time as fast as 45ns.

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IMS1420-55	4K x 4	55ns	50ns	600mW	165mW
IMS1421-40	4K x 4	30ns	40ns	600mW	NA
IMS1421-50	4K x 4	40ns	50ns	600mW	NA
IMS1400-45	16K x 1	45ns	40ns	660mW	110mW
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CIRCLE 33 ON INQUIRY CARD

The Lexidata System 3400 Display Processor and full line of interactive peripheral devices are designed specifically for OEMs and sophisticated end-users. The System 3400, rapidly becoming the leader, with over 1,000 units shipped to date, possesses the product characteristics required by this demanding customer group.

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CIRCLE 34 ON INQUIRY CARD

diagnostics, error logging, automatic error correction, and automatic read to verify for all writes.

Up to 32 application processors are included in the central processor system. Each is a single-board computer using Intel's 8085A-2 microprocessor, 16k bytes of EPROM for resident system programs, and 48k bytes of RAM for user programs. Use of a p-code interpreter multiplies effective physical memory by a factor of two or three.

Standard peripherals supported independently by each microcomputer include a CRT, keyboard, floppy disk, parallel printer, and serial communications interface. Use of an MID interface board permits these computers to communicate with various nonstandard parallel and serial interfaces.

The parallel processing architecture simplifies support software and permits efficient operation of structured application programs. Using structured design techniques, the application is decomposed into separable tasks that are assigned to individual microcomputers. These computers process assigned tasks in parallel, providing high computational throughput and user response time.

Software is developed on the computer using the FailSafe Software Development System. The system is based on the automation of structured programming techniques in a disciplined programming environment. Techniques used in the system include creation of a data dictionary, structured data flow analysis, structured English language definition of functional specifications, and top-down testing procedure. Automation techniques include the use of simple paper forms to define system inputs and outputs, generation of a central data dictionary from variable definition forms, and translation of structured English specifications into program code. System and user documentation are generated as an output of the translation process.

Price for the basic system is $79,400. This configuration provides two 80M-byte disks, two 16M-byte disk cartridges for database backup, two database managers, two database controllers, and two 200-char/s printers. The system also has dual power supplies, supervisor station, one workstation, and FailSafe operating system and printer spooler software. **DOSC**, 175 I. U. Willets Rd, Albertson, NY 11507.

Circle 256 on Inquiry Card

Low cost, disk based microcomputer systems run UCSD Pascal

With prices that start at $5195, microcomputer systems store up to 14M bytes of data online. Designed for industrial users and third party OEMs, the systems run the UCSD Pascal operating system.

A number of features have been designed to adapt the units to commercial and industrial environments. Dependability is enhanced by electronic soft head load, automatic disk drive power-down, low operating temperature rise, and rugged all-metal enclosure.

Standard configurations are based on a 500-ns processor with 64k bytes of RAM. Six serial I/O ports and a realtime clock/calendar with battery backup are also provided. Expansion cards meet special requirements for parallel I/O and EPROM programming.

Model ONE supplies 2.2M bytes of online storage using two double-sided, double-density 8" diskettes. An integral DMA channel ensures high throughput in disk intensive applications. Model TWO provides 5M- or 14M-byte capacity using a Winchester disk drive. Its single 8" diskette offers backup capacity of 1.1M bytes. Both models are available with either desktop or rackmount cabinets.

Software support for the systems is provided by UCSD Pascal versions II.0 and IV.0, with optional FORTRAN 77 and BASIC compilers, as well as assemblers for 6800 and 8080 microprocessor families. Virtual disk and recursive editing capabilities are obtained with an ASE text editor.

During software development, the systems offer a workstation environment for Pascal and assembly language programmers. Applications packages in Pascal are available from several sources for business as well as other uses.

Prices for a complete system start at $5195. A 5M-byte unit with Pascal installed sells for less than $7000. OEM discounts are available. **Scenic Computer Systems Corp**, 12314 Scenic Dr, Edmonds, WA 98020.

Circle 257 on Inquiry Card

DATA COMMUNICATIONS

Local area network transmits at multiple speeds

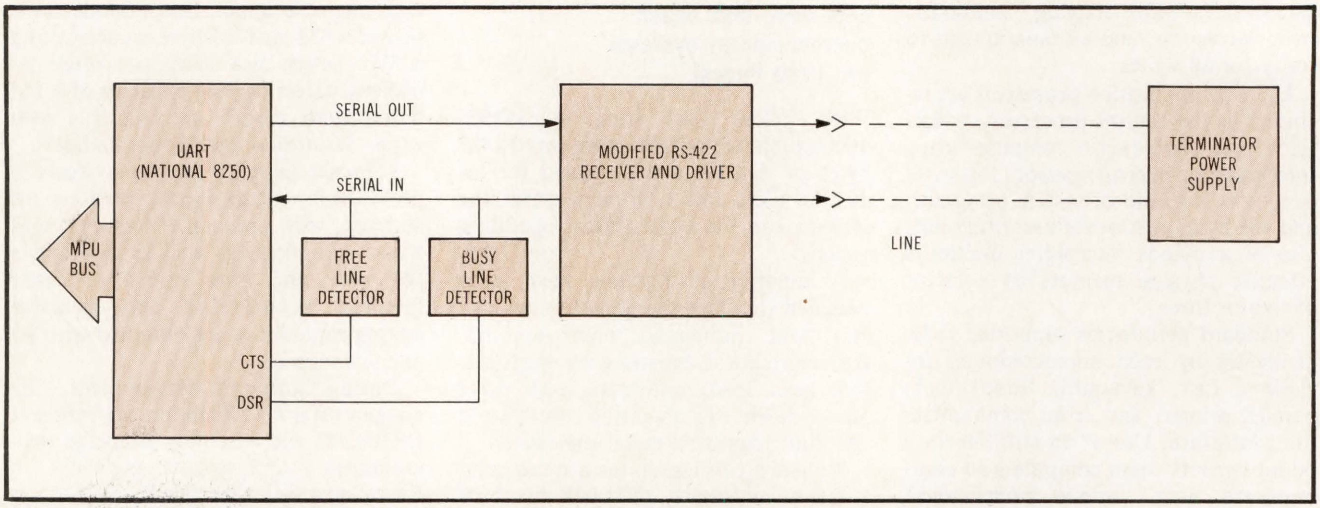
A local area networking system ZEDA Computers' InfiNet allows individual microcomputers to process local tasks in parallel with other processing. Two to 30 computers can be networked and up to 60 operations can be simultaneously performed. Along with microcomputers, the system allows the networking of hard disks, printers, mag tape, clocks, and terminals via a 2-connector cable; all run under a C/PM subset.

User sharing of resources, such as printers and disks, is a cost advantage obtained by networking. When a node or processor is added to the network, the system power does not degrade as it does in distributed systems. With networking, however, there is a degradation in the average network response time. At a conservative 24,000-baud transmission rate, response time for 2 stations transmitting simultaneously is 122 ms; 5 stations, 249 ms; and 10 stations, 1.25 s. Typically, 25 stations simultaneously transmitting require 3.12 s for network response. When 25 stations are transmitting, the rate slows to 939 baud. One way of improving response time is to increase the baud rate. The company feels many networks will be able to transmit at 100,000 baud. In most applications, however, stations spend more time executing programs locally than transmitting data. All or even most stations in a network would rarely transmit simultaneously. Response time and transmission rate degradation are not as debilitating as appear at first glance.

Several organizations, including the International Standards Organization (ISO), have proposed methods to divide various modules of local area networks into logical "layers." The ISO model consists of seven layers. InfiNet has dealt with the lower three levels (physical, data link, and network) of the ISO model and has maintained compatibility with the others.

The physical layer consists of a single twisted pair cable, less than 5 km long, which connects the transceivers in parallel. Differential voltage levels on the cable conform to the conventions of RS-422. Characters are placed on the cable in UART fashion by asynchronous

(continued on page 56)



InfiNet hardware implementation. Network "free" and "break" conditions are detected by pair of binary 16-counters clocked at 25,000 bps. One counts sequential ones and the other zeros. Overflow of ones counter generates "free" interrupt. Overflow of zeros counter generates "break" interrupt.

MOS communications chips using one start bit, eight data bits, and one stop bit per character.

The data link layer is responsible for construction of data packets. This layer accepts data from higher levels, delivers formatted packets to the physical layer, and awaits acknowledgments. When receiving, this layer acknowledges formatted packets from the physical layer, removes framing information, and delivers the contents of the data field to higher levels. Routines implementing this layer have been embedded into the ZEDOS (CP/M compatible) operating system, and could be buried within virtually any other DOS. The company's ZBASIC programming language also implements commands for communication with other stations.

The network layer divides outgoing messages into packet sized data fields, and assembles incoming data fields into complete messages for higher levels. Several utility programs for transmission of disk files, printing files, and sharing disk drives, have been written for systems at this level. Hooks for the MDBS data base manager have also been written into utilities at the network layer level, as well as for applications programs written in ZBASIC.

Information in the network is transmitted in packets; regardless of length and data rate, all packets begin with a preamble of nine character times. One character time is the time required to transmit a byte on the network, including the start and stop bits. The preamble is always transmitted at 25,000 baud, and consists of the following fields

Char time	Field name
0 to 1	Break char (marks beginning of each packet)
2 to 4	3-byte destination address
5 to 7	3-byte source address
8	Command byte (any 8 bits for arbitrary use)
9	Length of data field (in bytes)
10 to end-2	Data field (as many bytes as desired, containing data to be delivered to destination)
Last 2 chars	16-bit checksum char

Any two network stations can, by mutual agreement, use the command byte to switch to a higher data rate and/or lengthen the data field of the packet. The basic network can drive a 5-km cable with packet communication established at nine character times at a 25,000-bps rate. Individual applications can control the speed/cost/distance tradeoffs to increase the effective communication rate when appropriate. A packet cannot exceed 125 ms in length, which prevents any one station from dominating the bus. Also, a new packet cannot be placed on the cable until 16 bit times (at 25,000 baud) of silence have followed the previous packet. However, an exception to these restrictions is useful in optimizing data flow and reliability. When a receiving station wishes to acknowledge receipt of a packet from a transmitter, it can place up to three characters of data on the bus immediately after receipt of the last character of the packet, without waiting for the cable to become available to the other stations on the network. In this way, packet acknowledgment (or lack thereof) can be added to a data exchange without the delays inherent in cable arbitration and collision resolution.

A typical hardware implementation of the network is based on National Semiconductor's 8250 serial communications chip. Like many others, this chip interfaces directly to the microprocessor bus for parallel data transfers, and provides flexible serial input and serial output pins for connection with the network cable through the driving and detection circuitry. Collision detection is accomplished by transmitting stations that monitor their own transmissions and compare received data with transmitted data on a character by character basis. Differences are interpreted as a collision. **ZEDA Computers International Ltd,** 1662 West 820 North, Provo, UT 84601.

—Douglas Eidsmore, Senior Editor

Circle 258 on Inquiry Card

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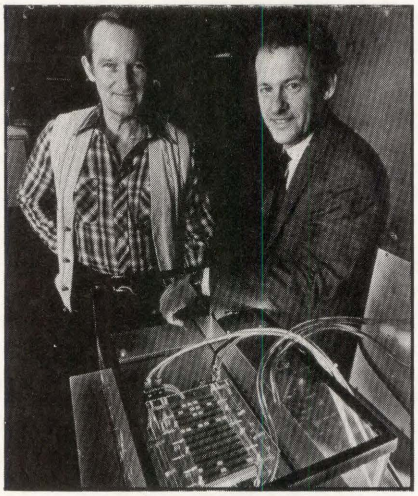
Liquid immersion technology cools supercomputer's circuits

A technological advance will permit development of a computer 6 to 12 times more powerful than today's machines. Performance goals for this machine require extremely dense packaging to reduce the length of connecting wires and achieve the 4-ns cycle time desired.

Plans for the CRAY-2 computer under development call for a 32M-byte memory size and a CPU having a 4-ns cycle time. In contrast, the existing CRAY-1 has a 4M-byte memory and a cycle time of 12 ns. In designing the machine, Seymour Cray, founder of Cray Research, Inc, has used ECL chips housed in tightly packed modules. They are immersed in an inert liquid for cooling.

Most large scale machines relay on freon or circulating water for cooling, with the cooling liquid flowing through a heat sink to which the circuits are attached. However, Cray has totally immersed the circuit card modules in the cooling liquid. Fluorinet, the inert fluorocarbon cooling liquid, is supplied by 3M Co for this and other electrical applications.



3-Dimensional module provides circuit density necessary to achieve CRAY-2's supercomputing speeds. Seymour Cray and John Rollwagen are shown with tank of inert liquid containing prototype module. Liquid immersion technology efficiently cools circuits within the module.

Immersing the circuits in the liquid eliminates the need for heat dispersing elements within the modules, enabling circuits to be more densely packaged into the 3-dimensional modules. This dramatically reduces the length of connecting wires—from 48″ (123-cm) in the CRAY-1 to 16″ (41-cm) in the machine under development—and provides far greater speed potential.

Development of the system will continue over the next few years. It is expected to be phased into production before 1985. **Cray Research, Inc,** 1440 Northland Dr, Mendota Heights, MN 55120.

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CIRCLE 36 ON INQUIRY CARD

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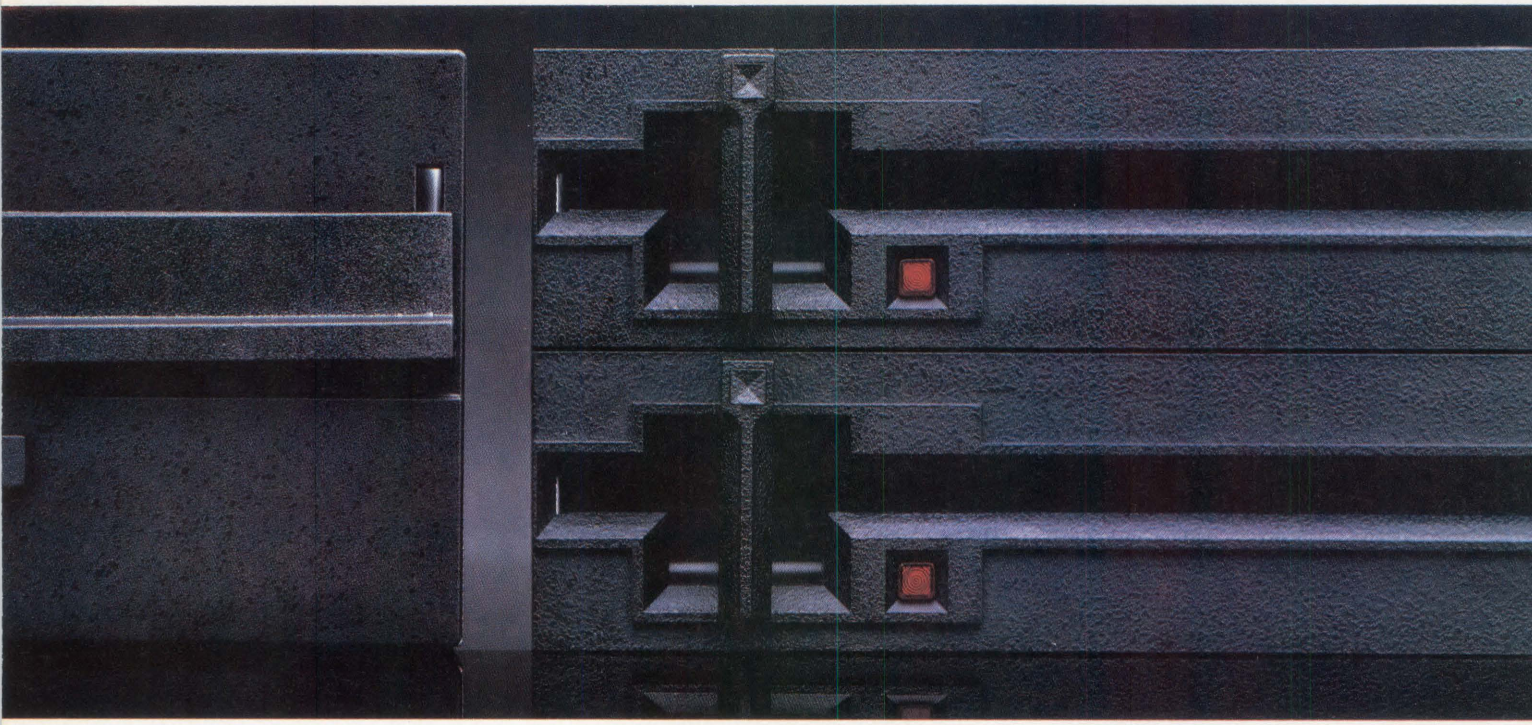

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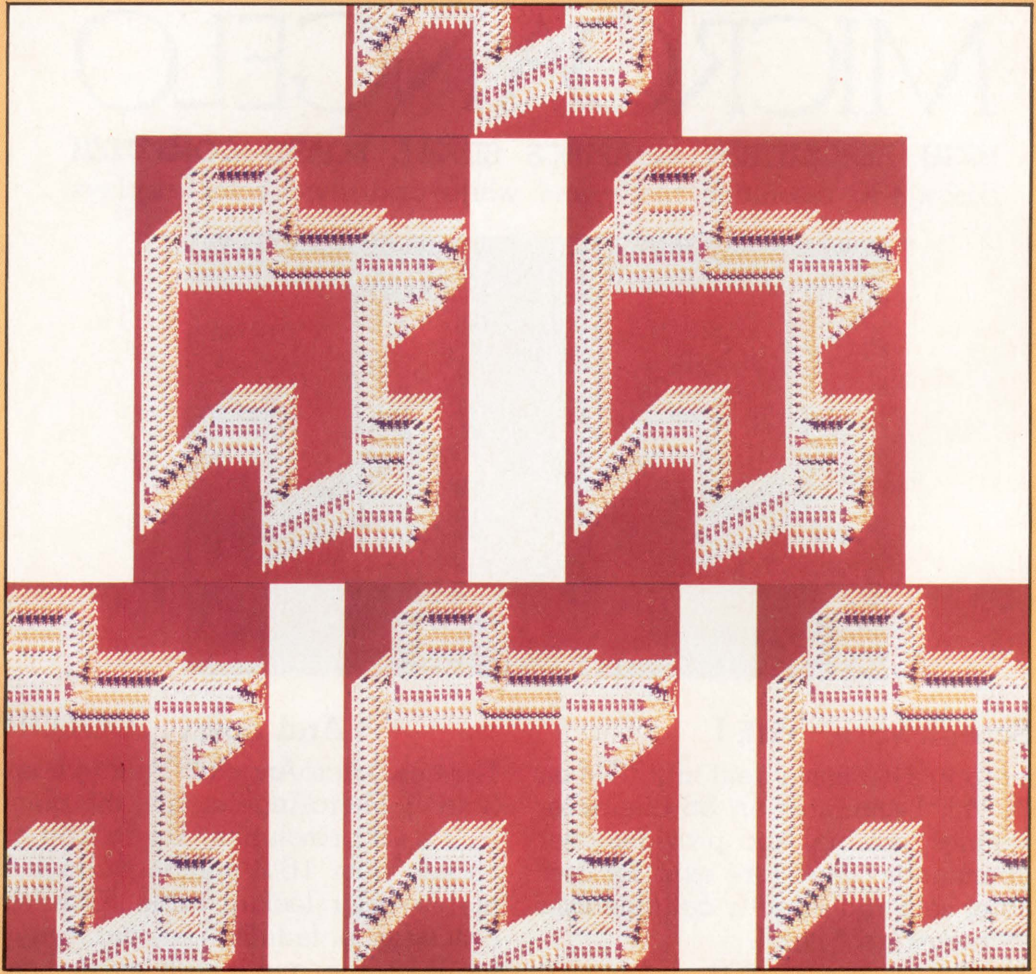
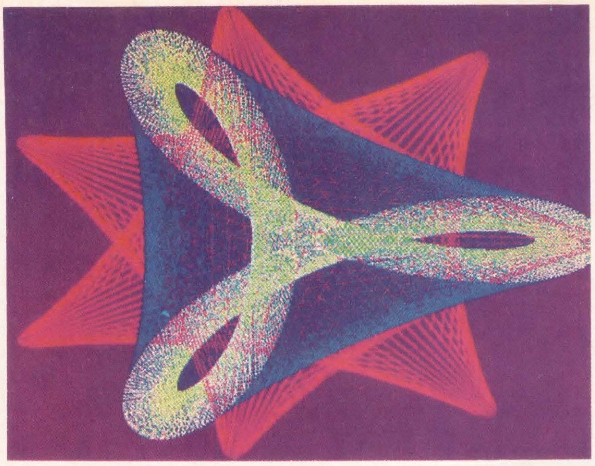
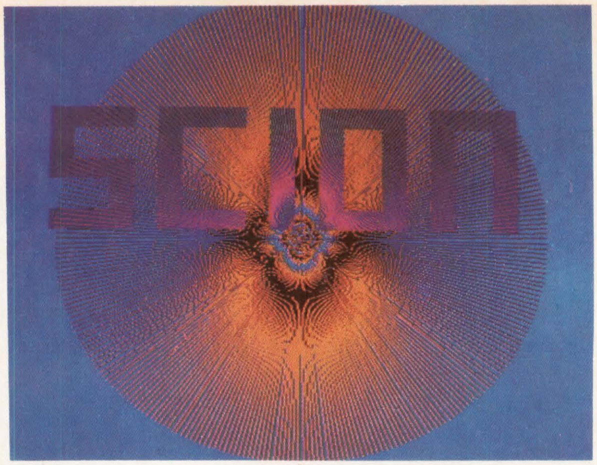
SPECIAL REPORT ON

INNOVATIONS IN SYSTEMS ARCHITECTURE







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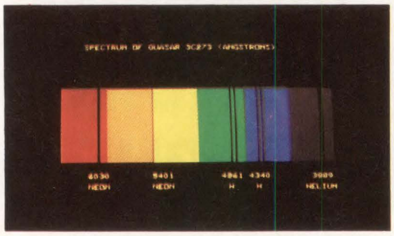
BYTE, Product Review



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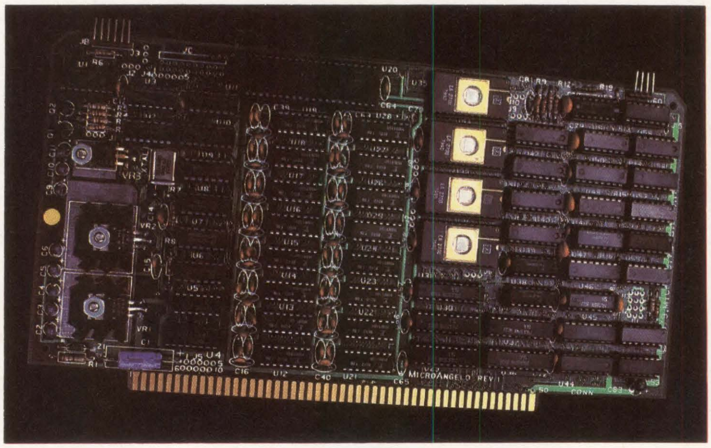

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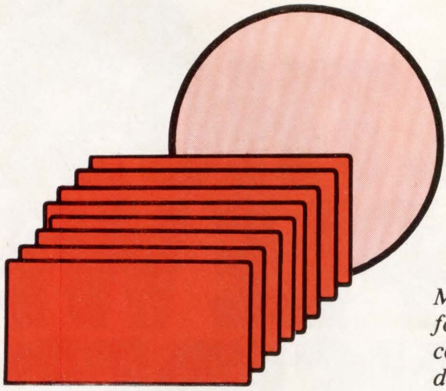
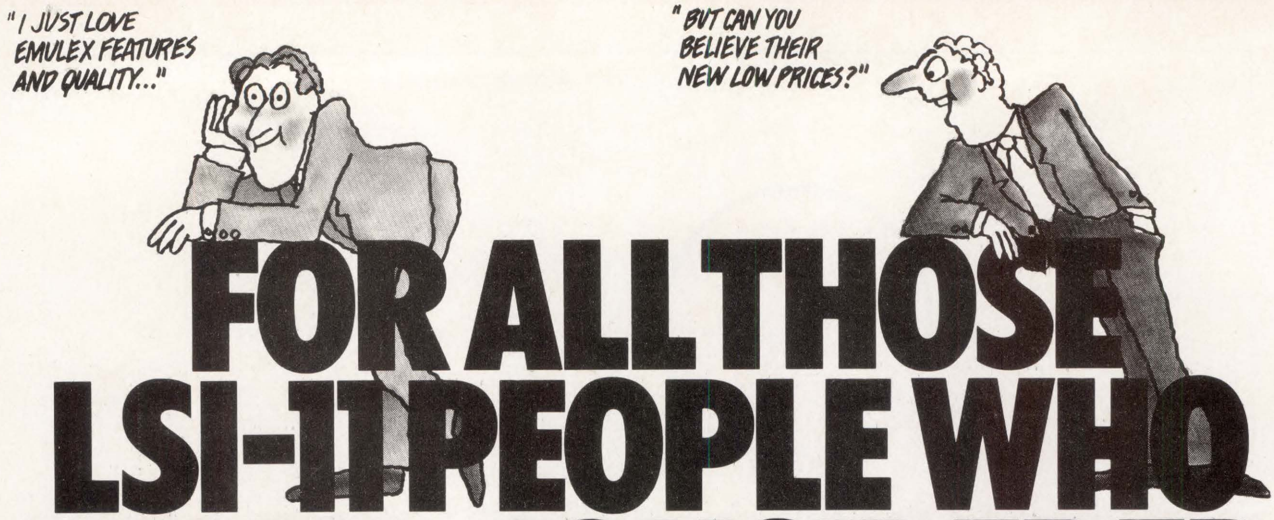


Minicomputer designed specifically for the UNIX operating system communicates with its I/O device controllers via IEEE 796 bus **87**

Special report on innovations in systems architecture



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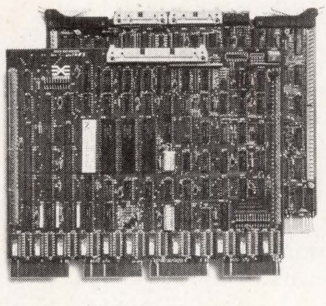

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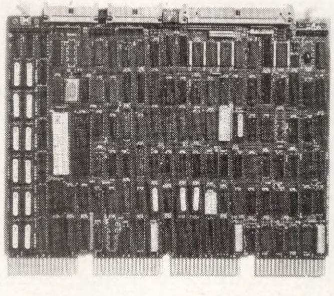

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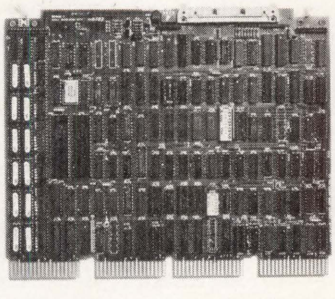

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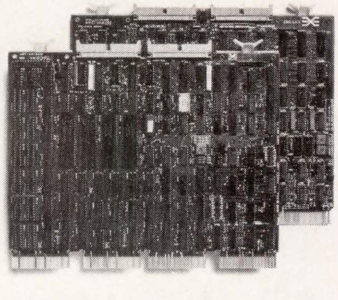

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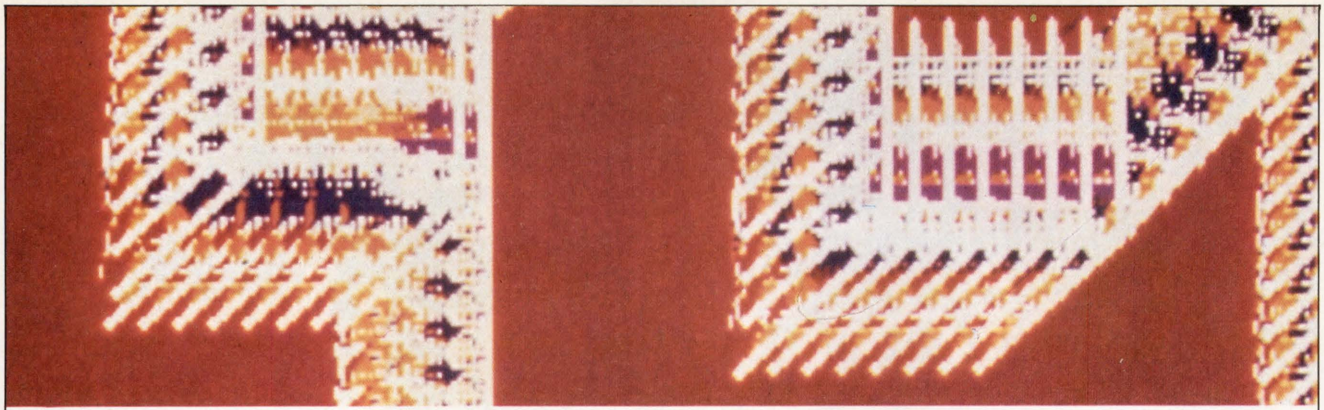

INNOVATIONS IN SYSTEMS ARCHITECTURE

have been few and far between in recent years. In a sense, the microprocessor revolution and the drive for lower priced computing power has more or less stifled most CPU architects, except for those involved in mainframe architecture and military or highly specialized systems. The era of designing minicomputers at the average computer company that couldn't support its own custom LSI designs ended several years ago, and with it came an innovation drought in system architecture. The microprogrammable bit slice chip offered somewhat of a resurgence in innovation architectures, particularly where 8-bit micros simply couldn't offer the functional performance features required in high speed applications such as array processing, graphics systems, and high end or super minicomputers. Many minicomputer companies were afforded reprieves from "death by microcomputer" competition through bit slice components, simply redesigning their multi-board SSI/MSI minis into single-board CPUs that were fully upward compatible with all of their previous software. Incidentally, the act of taking an off the shelf bit slice chip set and warping its preconceived purpose to emulate anyone's existing architecture is, indeed, a feat of sheer innovation in microcoding, as well as logic design.

For the time being, the upswing in 16-bit microcomputer chips is again going to put somewhat of a crimp in architectural innovation. The difference this time around, however, is that the host of smart support chips now available, and growing, is allowing system architects to do lots of innovative things with overall system structure, even though they are using somewhat mundane CPU chips as components. Multi-CPU and locally distributed functional system architectures are becoming commonplace. Now the system architect's challenge has become one of not being boxed in by a particular IC manufacturer's concept of what a computer system should look like.

The real renaissance in smaller CPU architectures is just within grasp as the VLSI gate array moves into the realm of the smaller computer manufacturer with the advent of the silicon foundry. Once again the CPU architect can return to innovations in internal CPU structures and still come up with a commercially feasible, competitive design.

Saul B. Dinman

Saul B. Dinman
Editor in Chief

A FLOATING POINT MODULE FOR MILITARY COMPUTERS

An extended arithmetic unit attains performance goals through its architecture and its approach to generating the algorithms that support floating point calculations

by Robert L. Cassola

The AN/AYK-14(V), designated as the U.S. Navy standard airborne model, is a variable configuration, general purpose 16-bit computer with a performance range of 400k to 800k operations/s. It is functionally partitioned into pluggable modules, the basic building blocks from which a variety of computer configurations can be constructed. Intermodule communications are standardized via uniform internal bus structures which permit reconfiguration and the addition of new modules without impacting the architecture. (See Fig 1.)

In order to broaden the capabilities of the computer, a special module has been designed to perform the floating point calculation of nine frequently encountered special mathematical functions: square root, exponential, natural logarithm, sine, cosine, tangent, inverse sine, inverse cosine, and inverse tangent. When configured with this module, called the extended arithmetic unit (EAU), the computer becomes well suited for performing mathematical calculations requiring high precision, such as those arising in navigation, guidance, and signal processing applications.

Basic design considerations

The design of the EAU began with the specification of the floating point word format, as well as the requirements for execution time, accuracy, module size, weight, and power. To maintain compatibility between AN/AYK-14(V) and AN/UYK-20(V) (U.S. Navy standard shipboard computer) software, the floating point word format for the unit was chosen to consist of a 24-bit fractional mantissa, a 7-bit exponent, and a sign bit denoting whether the value of the mantissa is positive or

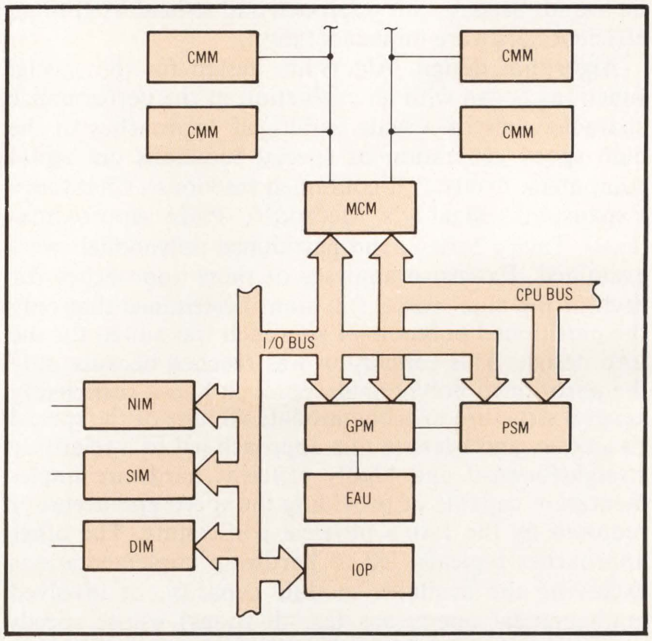

Fig 1 Block diagram of EAU in typical AN/AYK-14(V) configuration. Memory subsystem comprises four core memory modules (CMMs) and memory control module (MCM). I/O subsystem includes I/O processor (IOP) and three I/O channel types: Navy Tactical Data System, serial, and discrete interface modules (NIM, SIM, and DIM). CPU consists of general processor module (GPM), processor support module (PSM), and EAU, which interfaces directly with GPM. Instructions and floating point operands are transferred to EAU via 16-bit bidirectional bus. Floating point results are returned via same bus.

Robert L. Cassola is manager of technical resources for Government Systems operations at Control Data Corp, 8100 34th Ave South, Minneapolis, MN 55440. Previously, he taught physics at Ohio State University and was a research physicist at Battelle Memorial Institute, Columbus, Ohio. He holds a BS from the Polytechnic Institute of New York and a PhD from Ohio University. He is also a lecturer in physics at the University of Minnesota.

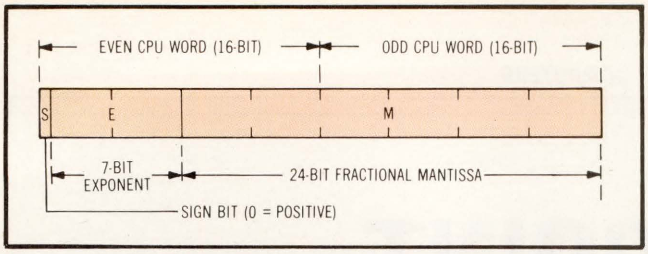

Fig 2 EAU floating point word format. Sign magnitude format with sign bit, 7-bit biased hexadecimal exponent, and 24-bit fractional magnitude mantissa is used. Positive and negative infinity values are defined and processed uniquely when detected. Floating point words must be located in even-odd pairs of AN/AYK-14(V) 16-bit registers or memory locations

negative. A hexadecimal representation is used and exponents are biased by 40_{16}. (See Fig 2.) Execution times for the nine special functions were targeted to be less than 30 μs, and the accuracy of the special function calculations was specified to be within one bit of the true value. The size of the unit was to be limited to that of the standard, double-sided, AN/AYK-14(V) module, whose dimensions are 6.5" x 9.0" x 0.80" (16.5 x 23 x 2 cm) while the weight was to be less than 2.3 lb (1 kg), and the power dissipation was not to exceed 50 W.

Next, attention as focused on the tradeoffs between the various approaches to generating the special mathematical functions and on the supporting architecture. It was concluded that the EAU performance goals could be realized only if two criteria were met. First, a unified mathematical approach that would apply equally well to the generation of each of the required algorithms had to be found. Second, this approach had to lend itself to an efficient hardware implementation.

Algorithm design. Algorithm design for the special functions began with an evaluation of the performance characteristics of a wide variety of approaches to the high speed generation of special functions on digital computers. CORDIC[1, 2], continued fractions[3], Chebyshev Expansion[4], Maehly's Method[5,6], Padé Approximations[3], Taylor Series[7], and partitioned polynomials were examined. Extensive analyses of these approaches for each of the nine special functions determined that only the partitioned polynomial approach was suited for the EAU design. This conclusion was reached because only the partitioned polynomial approach had a sufficiently general structure to accommodate all nine of the special functions, and because this approach led to a relatively straightforward and highly efficient hardware implementation capable of providing the speed and accuracy required by the EAU's physical constraints. The other approaches typically led to hardware implementations exceeding the available module capacity, or involved mathematical operations (eg, divisions) whose speeds were inconsistent with the required execution time of 30 μs.

The partitioned polynomial approach to the generation of the special functions divides the range over which a given function is to be determined into a small number of contiguous intervals. The function is then approximated within each of these intervals by a rational polynomial whose coefficients are optimized to provide the best fit to the desired function. A complete approximation for a given function thus consists of a set of polynomials which span the entire range of function arguments and can produce values that agree with the true function values to the desired level of accuracy.

For example, suppose that the function f(x) is to be approximated over the interval $x_i \leq x \leq x_f$. The partitioned polynomial approach divides the interval (x_i, x_f) into a number of intervals, n, such that

first interval:	$x_i \leq x < x_1$
second interval:	$x_1 \leq x < x_2$
.	.
.	.
.	.
j^{th} interval:	$x_{j-1} \leq x < x_j$
.	.
.	.
.	.
n^{th} interval:	$x_{n-1} \leq x < x_f$

For each of these intervals an approximating polynomial is generated. Thus, for the j^{th} interval the approximating polynomial $f^{(j)}(x)$ is generated, where

$$f^{(j)}(x) = \sum_k a_k^{(j)} x^k \qquad x_{j-1} \leq x < x_j$$

and the coefficients $a_k^{(j)}$ are determined to reduce the difference between f(x) and $f^{(j)}(x)$ to some acceptable level. The complete partitioned polynomial approximation to f(x) over the entire interval $x_i \leq x \leq x_f$ thus becomes

$$f(x) = \begin{cases} f^{(1)}(x) & x_i \leq x < x_1 \\ f^{(2)}(x) & x_1 \leq x < x_2 \\ \vdots & \vdots \\ f^{(j)}(x) & x_{j-1} \leq x < x_j \\ \vdots & \vdots \\ f^{(n)}(x) & x_{n-1} \leq x < x_f \end{cases}$$

The key considerations in using partitioned polynomials involve the number of intervals into which the total function range is to be divided and the complexity of the approximating polynomials employed in the various intervals. As a general rule, the number of intervals should be kept as small as possible, consistent with speed and accuracy requirements, and the complexity of the approximating polynomials should be essentially equal for each interval, thus ensuring that execution time will be relatively constant over the entire range of function arguments.

Architecture design. As already noted, the partitioned polynomial approach to approximating the special functions leads to a relatively straightforward and efficient

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architecture. This is because each of the expressions to be evaluated is a polynomial of the general form

$$p(x) = p_0 + p_1x + p_2x^2 + p_3x^3 + p_4x^4$$

where, as an illustration, a 4th-order approximating polynomial has been assumed. Such a polynomial can be rewritten in the equivalent form

$$p(x) = \{[(p_4x + p_3)x + p_2]x + p_1\}x + p_0 \quad (1)$$

consisting of a sequence of repetitive operations involving a multiplication followed by an addition. Because this process is repetitive, an architecture can be specifically developed to perform this multiplication/addition sequence efficiently.

Such an architecture, shown in Fig 3, contains the elements of the EAU directly involved in the polynomial expansion process. Other elements (not shown) include exponent handling hardware, additional registers for floating point scaling and for interfacing to other AN/AYK-14(V) central processing unit modules, and a 2048-word x 40-bit control memory (containing built-in test and operational sequences) and supporting addressing structure. Command word sequences called *controlware* regulate this architecture. Commands are read from the control memory, and one command is used to control each machine cycle. Cycle times range from 156.25 to 343.75 ns, depending on the function performed. Commands are used to initiate the serial multiply/add operations, which then proceed independently, under control of a 16-MHz clock. Additional commands may be executed during a serial multiply/add operation.

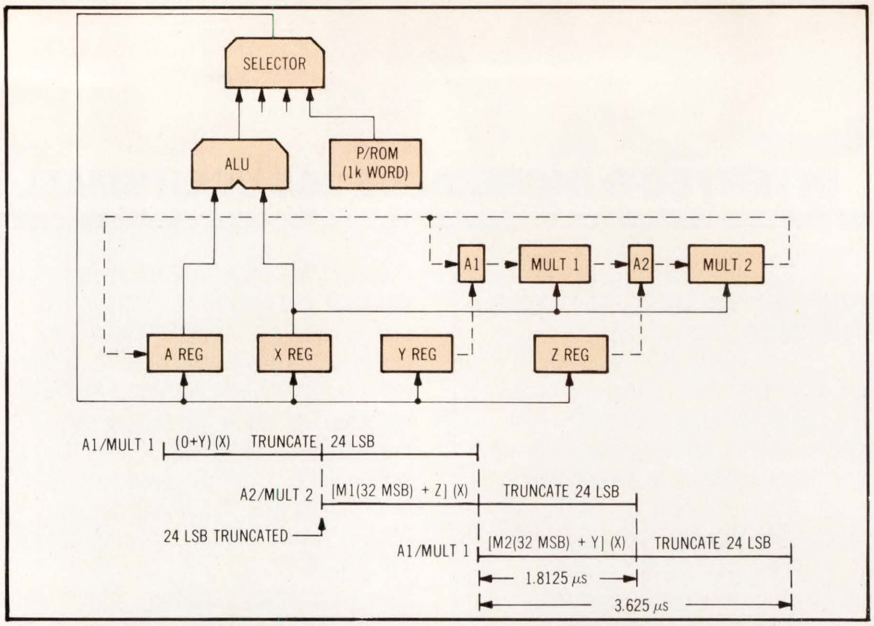

Fig 3 Polynomial expansion architecture. EAU elements directly involved in polynomial expansion process are dual, serial, and overlapped adder/multipliers. Architecture is controlled by command word sequences, and each machine cycle by one command.

In order to illustrate the use of the architecture for polynomial expansion, the general 4th-order polynomial of Eq (1) will be assumed. If m represents the 24-bit mantissa, then p(x) becomes

$$p(m) = \{[(p_4m + p_3)m + p_2]m + p_1\}m + p_0$$

The controlware steps and serial multiplier/adder operations required to evaluate p(m) are

(1) Y = p_4: Transfer the 32-bit p_4 value from the programmable read only memory (PROM), via the selector, to the Y register.

(2) Initiate MULT 1 for p_4m: Load serial multiplier 1 with the value m which is contained in the X register, and multiply by p_4 (contained in the Y register). The serial adder 1 (A1) is disabled for this multiply, thus disregarding multiplier 2 output.

(3) Z = p_3: Transfer the 32-bit p_3 value from the PROM, via the selector, to the Z register. This transfer occurs during the first part of the previously initiated multiply operation.

(4) Initiate MULT 2 for (p_4m + p_3)m: Load serial multiplier 2 with the value m from the X register, and multiply by the sum of p_4m (from multiplier 1) and p_3 (from the Z register). The EAU hardware initiates this multiply at the midpoint of the multiplier 1 operation. At this point, the 24 least significant bits (LSB) of the multiplier 1 product have been discarded, and the 32 most significant bits (MSB) of the product are serially added to the Z register contents for the multiplier 2 operation. The first half of the multiplier 2 is thus overlapped with the last half of the multiplier 1 operation, as illustrated in Fig 3.

(5) Y = p_2: Transfer the 32-bit p_2 value from the PROM, via the selector, to the Y register.

(6) Initiate MULT 1 for [(p_4m + p_3)m + p_2]m: Load multiplier 1 with the value m from the X register, and multiply by the sum of p_2 (Y register) and the 32 MSBs of the multiplier 2 product.

(7) Z = p_1: Transfer the 32-bit p_1 value from the PROM, via the selector, to the Z register.

(8) Initiate MULT 2 for {[(p_4m + p_3)m + p_2]m + p_1}m: Load serial multiplier 2 with the value m from the X register, and multiply by the sum of the 32 MSBs of the multiplier product and the p_1 value (Z register). This final product is serially transferred into the A register such that when the multiply operation is complete, the product is contained, appropriately scaled, in the A register.

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(9) $X = p_0$: Transfer the 32-bit p_0 value from the PROM, via the selector, to the X register.

(10) $X = A + X$: Transfer the sum of the p_0 value (X register) and the A register contents back into the X register. The EAU hardware delays this operation until the final multiplier 2 operation is complete. This final addition is performed in the 32-bit parallel arithmetic logic unit (ALU) and transfers the value

$$\{[(p_4m + p_3)m + p_2]m + p_1\}m + p_0$$

to the X register. This value is the fractional mantissa of the final polynomial result. Additional EAU commands are required to appropriately normalize the final result, combine the mantissa with the final exponent value, and transfer the floating point number to the central processing unit.

It was recognized early that the effects of finite word length, rounding and truncation operations, resolution, etc, would strongly influence overall algorithm accuracy.

The polynomial expansion process uses the overlap feature of the dual, serial multiplier/adders to perform an n^{th} order polynomial expansion in $(n + 1) \cdot 1.8125\ \mu s$, as illustrated in Fig 3. Each serial multiplier uses three AMD 25LS14 multiplier circuits to obtain a product in $a + b + 2$ clock cycles, where a is the number of bits in the multiplier and b is the number of bits in the multiplicand. Since 32-bit (p_n) by 24-bit (m) products are required, and a 16-MHz clock is used, the total multiply time is (58) (62.5 ns), or 3.625 μs. The overlap feature effectively reduces this time to one half, or 1.8125 μs, for each multiply in the polynomial except for the last, which requires the full 3.625 μs.

The exponents of the floating point operands can be accommodated using the same general approach by expressing the approximating polynomial in the form

$$p(x) = p_0 + p_1(m16^k) + p_2(m16^k)^2 + p_3(m16^k)^3 + p_4(m16^k)^4$$

where $x = m16^k$ is a floating point number whose fractional mantissa is m and whose unbiased hexadecimal exponent is k. This expression may be expanded and rewritten

$$p(x) = p_0 + p_1 16^k m + p_2 16^{2k} m^2 + p_3 16^{3k} m^3 + p_4 16^{4k} m^4$$

or

$$p(x) = \left(\{[(p_4 16^{3k} m + p_3 16^{2k})m + p_2 16^k]m + p_1\}m\right) 16^k + p_0$$

which possesses the same general form as Eq (1), and reduces to Eq (1) for the case $k = 0$.

For $k \neq 0$, the polynomial expansion proceeds as already described, except that the values of p_0, p_1, $p_2 16^k$, $p_3 16^{2k}$, etc, are now read from the PROM instead of the p_n values. This technique requires multiple tables of coefficients to be stored in the PROM for each function, but eliminates the need to perform a multiply (or scaling) operation on the p_n values. The quantity (16^k) factored from the expression

$$p(x) = \left(\{[(p_4 16^{3k} m + p_3 16^{2k})m + p_2 16^k]m + p_1\}m\right)(16^k) + p_0$$

represents the exponent of the operand and does not require a multiplication in the polynomial expansion process.

Tables for exponent values $k = 1$, $k = 0$, $k = -1$, $k = -2$, $k = -3$, $k = -4$, $k = -5$, and $k = -6$ are normally required. For $k > 1$, an input operand reduction is performed to reduce the operand to the primary range of the function and allow use of the appropriate table. Tables for $k < -6$ are not required, since function calculations become unnecessary for these small values (for example, $\sin x = x$ for very small numbers). For negative k values, the tables (and the corresponding number of terms in the polynomial) become smaller as k increases, since the 32-bit coefficient $p_n 16^{(n-1)k} = 0$ when $(n-1)k < -8$. Thus, the unnecessary multiplications by zero are eliminated, and execution times are reduced for operands with negative exponents.

Detailed design considerations

Once partitioned polynomials had been chosen as the preferred mathematical approach, and the basic architecture had been established, the detailed design of the algorithms for the nine special functions began. The principal goal was to develop specific algorithms.

The first step was to develop an EAU simulation which would permit an accurate evaluation of the performance of various candidate algorithms. It was recognized early that the effects of finite word length, rounding and truncation operations, resolution, etc, would strongly influence overall algorithm accuracy. It was also recognized that once a suitable algorithm structure had been established, a number of iterations would be required to refine it into a form optimized for speed and accuracy. The simulation was therefore carefully constructed to faithfully represent the actual EAU hardware to the bit level, ensuring that the simulated performance

Other special purpose calculations, such as Kalman filtering, readily suggest themselves as candidates for EAU functions.

of a candidate algorithm would be identical to its performance in an actual EAU. In addition, it was designed to efficiently accommodate modifications to candidate algorithms, thus permitting a wide variety of algorithm implementations to be fully explored in a relatively short time.

After developing the simulator, detailed algorithms for each of the nine special functions were specified, programmed, tested, evaluated, and refined. During the evaluation, several observations about the detailed structure of the algorithms emerged. First, it became

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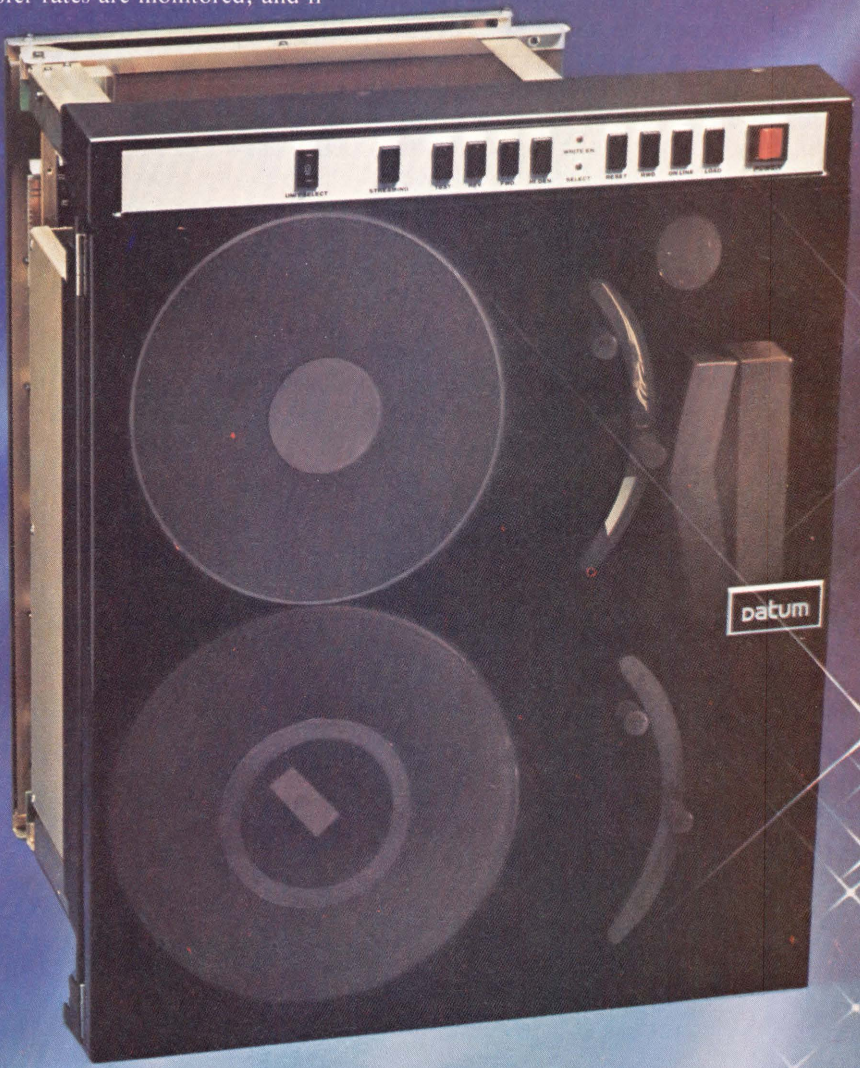

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apparent that any reasonable partitioned polynomial representation of the inverse sine and inverse cosine functions would require the evaluation of a square root. It was therefore essential to develop an algorithm for the square root function which not only provided the requisite accuracy, but whose execution time was significantly less than 30 μs. Careful analysis led to an approach based on a 3-term Taylor expansion of the square root function within a number of relatively narrow intervals which span the range of argument values lying between 0.25 and unity. A scaling technique was then used to expand this reduced range to the full range of argument values, which extends from zero to infinity. The resulting algorithm for the square root function is able to provide an average accuracy in excess of 23.5 bits and requires an execution time of 13 μs. This latter figure is sufficient for evaluating the inverse sine and cosine functions within the desired 30 μs.

Second, it was observed that the accuracy of an algorithm suddenly and unexpectedly deteriorated in certain regions. This aberrant behavior was usually subtle so that it was hard to detect. Such behavior typically arises not because of any *mathematical* flaw in the algorithm design, but because of the errors introduced by certain *digital* operations used by the algorithm. Considerable effort was required to locate these trouble spots, and much ingenuity was needed to eliminate them.

Third, it was noted that an efficient procedure for performing angle reduction was needed. Angle reduction is required to calculate the trigonometric functions for argument values exceeding 2π radians, thus reducing a large input argument to one that lies within the principal range of the trigonometric functions. The procedure requires considerable care to ensure that the reduced angle contains sufficient precision to yield a function value with the desired accuracy. Furthermore, the process must be accomplished as rapidly as possible, since computational speed is of utmost importance. A series of tradeoff analyses led to a procedure in which a complete angle reduction process typically requires 20 μs. Its accuracy is evidenced by the computation of the sine and cosine functions with an error that does not exceed 4 bits for argument values as large as 10^7 radians.

EAU performance

The performance of the EAU's nine special functions was verified by comparing the calculated results with those of a standard, taken to be the CDC 6600, whose accuracy significantly exceeds that required for EAU verification. For each of the special functions, at least 10,000 random numbers were used to sample the range of function argument values. Care was taken to ensure that adequate sampling was provided for all ranges of the function and that potential trouble spots were identified and examined in detail.

The Table summarizes the results of the accuracy and speed evaluation for the nine special functions. It shows that for all of the functions the EAU results are either identical to, or within one bit of, the true value in over 95% of the cases tested. Also, the typical execution times for each of the special functions are less than 30 μs over the principal range of argument values. Only when the trigonometric functions are evaluated for arguments exceeding 2π radians does the average execution time exceed 30 μs.

Conclusions

The EAU provides the AN/AYK-14(V) with the capability to perform floating point arithmetic as well as highly

Accuracy and Typical Execution Times of EAU Special Functions

		Percent Occurrence of n-bit Error*					
Function	Range	n = 0	n = 1	n = 2	n = 3	n > 3	Typ Execution Time (μs) (incl CPU and EAU times)
Square root	$0 \le x \le +\infty$	70	30	-	-	-	13
Exponential	$-\infty \le x \le +\infty$	45	50	5	0.01	-	26
Natural logarithm	$0 \le x \le +\infty$	50	50	-	-	-	26
Sine	$-2\pi \le x \le +2\pi$	77	23	-	-	-	24
	$-10^7 \le x \le +10^7$	31	56	13	-	0.01†	45
Cosine	$-2\pi \le x \le +2\pi$	68	32	-	-	-	24
	$-10^7 \le x \le +10^7$	31	55	13	-	0.04†	45
Tangent	$-2\pi \le x \le +2\pi$	68	31	1	0.09	0.04	28
	$-10^7 \le x \le +10^7$	40	35	20	3	2	50
Inverse sine	$-1 \le x \le +1$	79	21	-	-	-	26
Inverse cosine	$-1 \le x \le +1$	60	40	-	-	-	26
Inverse tangent	$-\infty \le x \le +\infty$	56	44	-	-	-	23

*Fractional percentages have been suppressed except for values less than unity
†Corresponds to a 4-bit error

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accurate and rapid floating point calculations of nine frequently encountered mathematical functions. This capability, unique in a general purpose tactical processor, makes the computer particularly attractive for guidance, navigation, signal processing, and similar applications requiring rapid, high precision, floating point calculations.

Also provided by the unit is the potential for evaluating other special functions that might be encountered in certain applications. This added feature stems from the EAU's ability to accommodate additional special purpose controlware, which can be tailored to the requirements of specific problems. For example, a particular guidance application might use linear regression to estimate current position from a series of prior position measurements. By adding appropriate controlware to the unit, the calculation can be incorporated directly into the EAU's list of standard functions, thereby significantly increasing the speed at which the linear regression is calculated. Other special purpose calculations, such as Kalman filtering, readily suggest themselves as candidates for additional EAU functions.

Acknowledgments

Derald Pedersen was responsible for the definition, design, and verification of the EAU architecture. Generation of the unit's controlware was the responsibility of Larry Brezinski. Bob Pedersen designed the EAU simulation, while Marion Klockeman performed the preliminary coding of the various algorithms. Finally, the formulation of several of the algorithms is due to Juris Ozols, whose many suggestions were influential in improving the overall performance of the entire EAU algorithm package.

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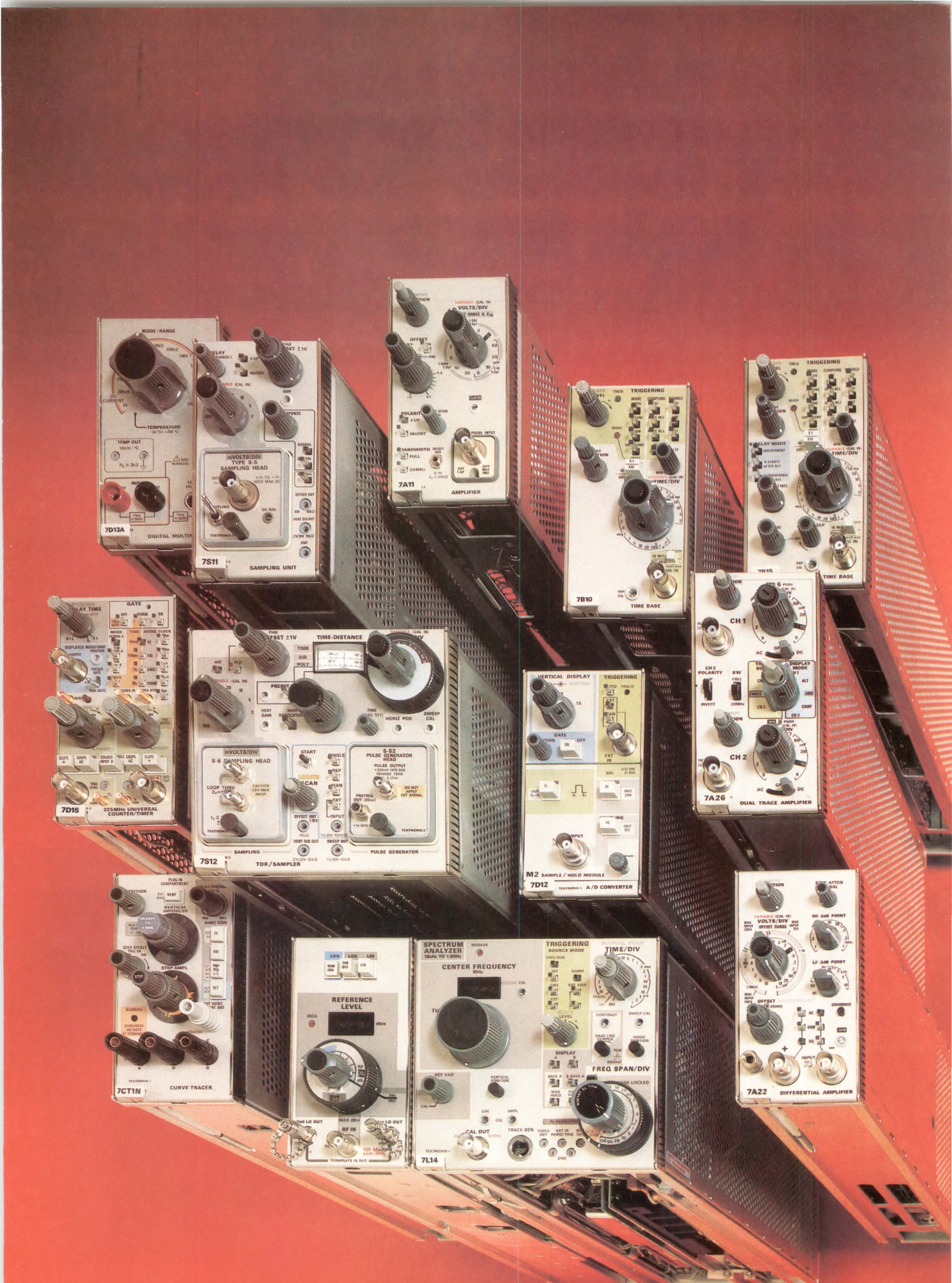
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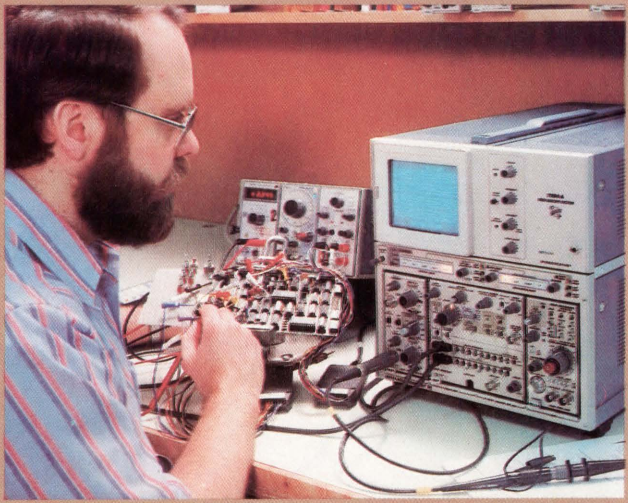

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Executing special functions in external hardware, interlaced with but not controlled by the microcomputer, offers speed advantages

by Meir Lahat

Being integral components, microcomputers have instructions that cannot be modified from outside. To enable the processors to execute additional instructions, sequences are conventionally formulated by means of routines (eg, multiplication in the 8085 or floating point in the 8086). For greater speed, connecting external hardware permits various functions to be executed under processor control. In this case, operands are transferred from the processor to the external device and the results are read back; this is accomplished under computer control using conventional input/output techniques.[1, 2] Controlling execution of such functions with the processor, however, requires that the processor be interrupted to handle functions such as operand transfer. Additional speed can be obtained more efficiently without processor intervention by using specialized high speed hardware[3-5] in combination with a technique that executes functions interlaced with the processor but independent of it.

The interlacing technique provides a higher execution speed and exploits up to 50% of the special hardware's capacity. Flexibility in addressing the operands is preserved on the level of the microcomputer itself.

Interlacing functional hardware

Key to the technique is conversion of a complete instruction in the fetch phase to a different instruction (usually a NOP or relative JMP). This converted instruction, instead of executing a function within the microcomputer, results in activation of the special hardware function that connects directly to the memory. This function, in turn, extracts operands, performs required operations, and returns results to memory.

The technique, illustrated in Fig 1, uses as special instructions either unused instructions or existing instructions that are blocked in the microprocessor. The address multiplexer and the data buffer remain transparent as long as they do not execute special function instructions. When a special function instruction is reached, the special instruction switching unit decodes it during the fetch phase and blocks the data buffer and address multiplexer with the aid of the special instruction line. The special instruction switching unit sends a short "dummy" instruction to the data input bus of the microcomputer. Although no function is executed by the microcomputer (similar to a NOP or JMP instruction), the special hardware function unit is instructed to begin independent operation. The special hardware function unit extracts addresses of the operands from memory, executes necessary operations, and returns results to memory.

Since the functional hardware can execute functions at a very high speed, and since memories currently in use are very fast compared with the execution speed of even short instructions in the microcomputer, the entire process can be completed during the time the dummy instruction is being executed in the microcomputer. Depending on the specific processor used, its speed, and the interlaced function implemented, extra wait cycles can be added to the dummy instruction to ensure that the interlaced hardware can complete its function before the dummy instruction is completed.

The interlaced technique can be implemented for any microprocessor. With pipelined central processing units based on sophisticated microprocessors, it is only necessary to ensure proper synchronization and to add wait cycles as required. The technique easily addresses operands in memory; however, addressing information in

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the microprocessor is more difficult and may require additional instructions to accommodate information exchange with the processor.

Depending on required functions and on the structure of the microprocessor system in use, the technique can be implemented in various ways. Therefore, this discussion will be limited to implementation of a high speed interlaced multiplication function for the TMS-9900 microcomputer by connecting an external TRW MPY-16 multiplier.

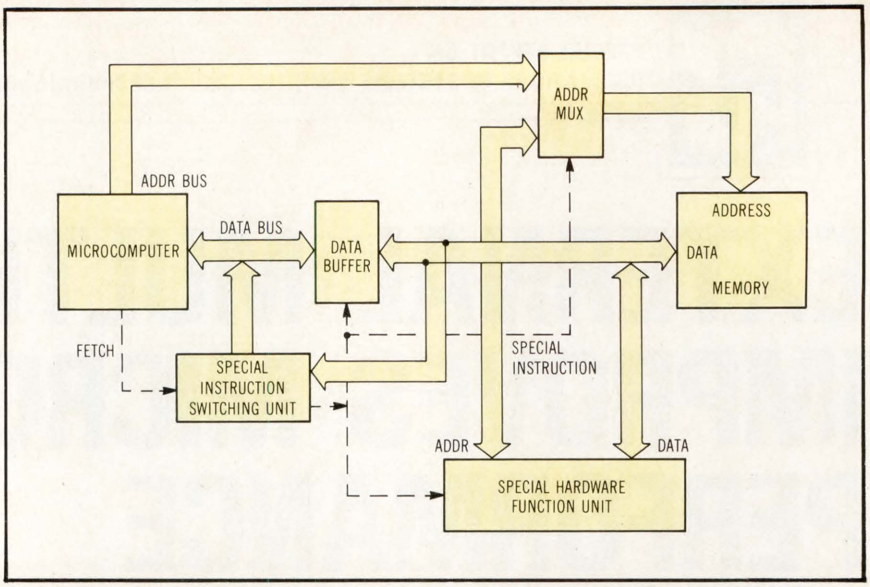

Fig 1 Interlaced special hardware technique. System is designed to switch special hardware instructions during fetch cycle and to block data buffer and ADDR MUX using special instruction line. Dummy instruction, sent to microcomputer's data input bus, performs no function, but instructs special hardware function unit to begin independent operation.

Realization

A 16-bit microcomputer with a memory to memory architecture, the TMS-9900 is distinguished by having only three onchip registers: program counter (PC), status register (ST), and workspace register (WH).[6] The workspace register indicates the memory address that is assigned to the first of 16 registers; the remaining 15 registers are sequential to the first.

In the 9900, the multiplication instruction takes about 20 μs and is performed only on unsigned operands. The interlaced technique reduces the execution time to 2 μs, and allows multiplication of signed operands. The interlaced multiplication function is transparent to the programmer. When a multiplication instruction is fetched from memory, it is converted to a short dummy instruction for the processor. The interlaced hardware performs the multiplication function during dummy instruction execution. The result is obtained as if the multiplication function were performed by the microcomputer, but faster than the processor could do it. The multiply instruction consists of one or two words, as shown.

0	1	2	3	4	5	6–9	10–11	12–15
0	0	1	1	1	0	D	TS	S

Second word	(only in TS = 10)

D—operand in register (1 of 16 registers)
TS, S—source

Symbolic and index addressing modes use two words for instruction execution. The second word is the operand or the address of the operand. In the remaining three modes of addressing, one word is sufficient.

TS	S	Addressing mode
00	0 to 15	Workspace register
01	0 to 15	Workspace register indirect
10*	0	Symbolic
10*	1 to 15	Indexed
11	1 to 15	Workspace register indirect autoincrement

*Not used

Only three addressing modes are used in this system. One word mode is used only for multiplication; the remaining two modes are not used, saving hardware and preventing execution of the two dummy instructions that are required to complete the process and set the program counter for continuation of the run.

The multiply instruction (op code 001110) is decoded during the fetch phase (instruction acquisition—IAQ) by the special instruction switching hardware. Then the data buffer is blocked, and code 0000 is instead sent to the microcomputer. This code is not used by the processor and results in no function execution or status alteration. Decoding is completed within six cycles; after decoding, the PC is incremented in preparation for the instruction that follows.

The special hardware function receives the multiply instruction at the same time. Depending on the addressing mode, as specified by TS, the unit extracts addresses and operands from memory, and executes up to six additional memory accesses (mode 11) to complete the connection and return the result. The multiplication itself is executed in the fast multiplier; results are obtained in 200 ns. The entire process, from beginning to end, is performed in less than 2 μs.

If a memory with a 200-ns cycle time is used, and if allowance is made for the additional 50-ns propagation time in the system, the process can be completed within 1.9 μs. Execution of the dummy instruction in the processor will take 2 μs. If the process requires more than 2 μs, the system must be switched to hold to complete the process.

The system reduces execution time for a multiplication by a factor of 10 for unsigned operands and by a factor of 20 for signed operands. In systems operated under microcomputer control, the corresponding acceleration factors are 2 and 4, respectively.

Functional multiplication circuit

When the special instruction signal is sent from the special instruction switching unit, the functional multiplication circuit (Fig 2) is activated. Changes to the workspace register made during programming require an update. This can be accomplished by means of routine

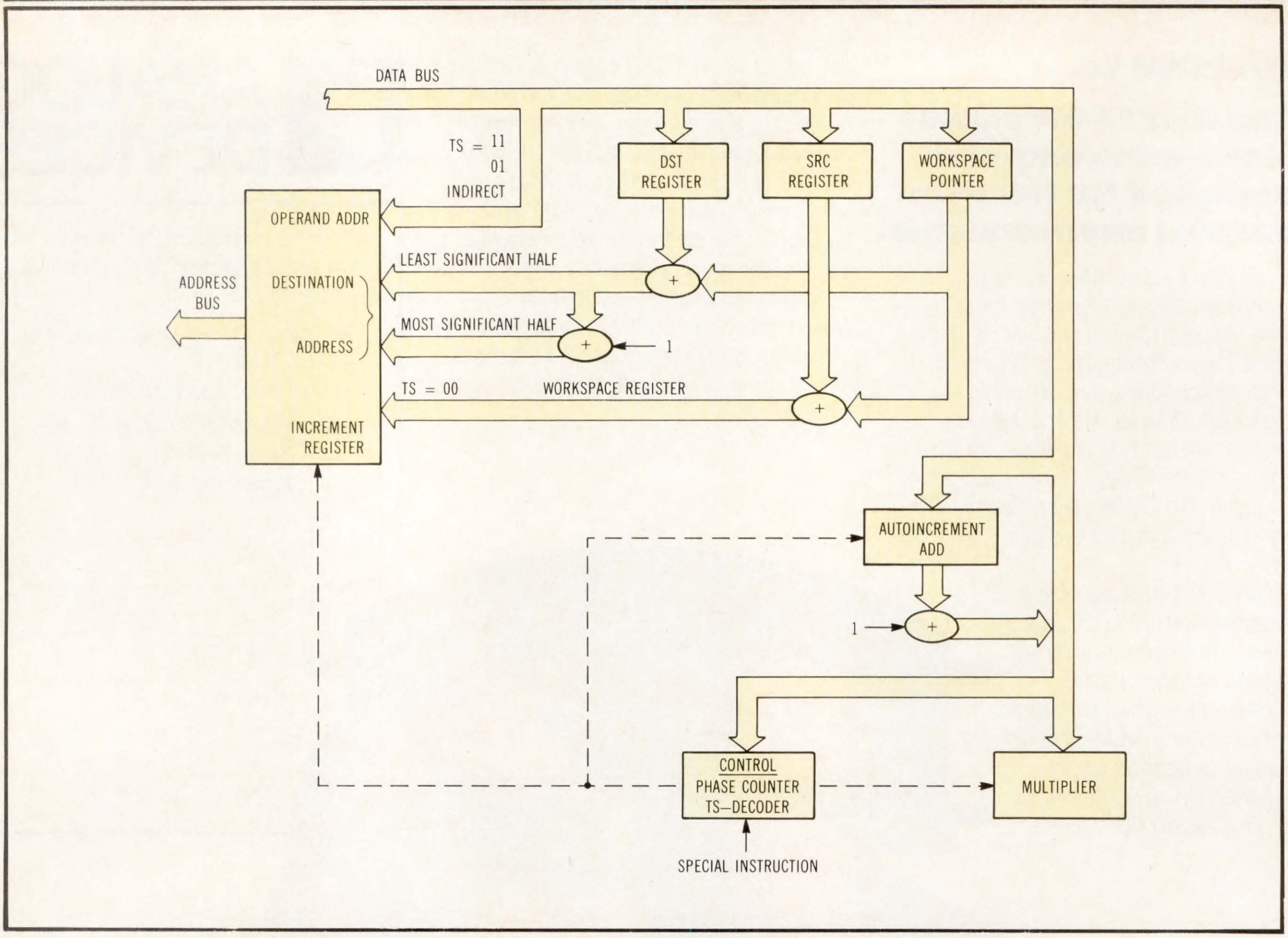

Fig 2 Functional multiplication circuit. Activated when special instruction signal is sent from special instruction switching unit, control unit decodes addressing mode and actuates phase counter. Workspace registers are updated by means of routine I/O instructions or by direct decoding of two instructions affecting registers.

input/output instructions or by direct decoding of the two instructions affecting the workspace register.

The control unit decodes the addressing mode according to TS, S, and D, and activates the phase counter. The system contains up to 10 phases, two of which are optional and depend on the addressing mode.

Phase	Function	Cycle (ns)
1	Fetch	
	(WH) + SRC → ADDR BUS	350
	(Memory) → data bus	200
2*	(Data bus) → ADDR BUS (mode TS ≠ 00)	50
3	(Memory) → multiplier	200
4**	(ADDR BUS) + 1 → memory (mode TS = 11 only)	200
5	(WH) + DST → ADDR BUS	50
6	Memory → multiplier	200
7	Multiplication	200
8	(Multiplier most significant half) → memory	200
9	(WH) + DST + 1 → ADDR BUS	50
10	(Multiplier least significant half) → memory	200

*Active only if mode is not workspace register, WH (TS ≠ 00)
**Active only in autoincrement mode (TS = 11)

Durations of all cycles are integral multiples of 50 ns. Execution time of the multiplication operation will be 1.9 μs using the longest addressing mode.

Summary

Accelerating microcomputer performance through external functional hardware, this technique overcomes delays encountered using conventional techniques. By eliminating the need to use the computer to move operands to external hardware, the technique supplies speed and flexibility advantages. In addition, it can be implemented in most existing systems without internal modifications.

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A MULTIPROCESSOR MINICOMPUTER DESIGNED FOR UNIX

Using industry standard design, challenging memory requirements of the UNIX operating system are met by a multiprocessor equipped minicomputer

**by Curtis Myers
and Grant Munsey**

A multi-user minicomputer designed specifically for the UNIX operating system incorporates industry standard design elements. The architecture's sole purpose is to optimize UNIX by exploiting its strengths and designing around operating system characteristics that hinder performance in multiprocessing environments.

Designing system hardware for a specific operating system is not a new concept; neither is designing according to readily available and understood industry standards. However, a number of factors, such as the growing cost of software development for both the system integrator and the end user, have combined to make these two design criteria essential for future systems. Additional factors include the falling price of hardware, standardization of buses and interfaces, leveling of technical capabilities, and growing availability of special purpose integrated circuits. These factors have diminished the advantages of proprietary architectures and operating systems.

In short, market forces have played the largest part in system design. Providing high system performance and throughput was the first design criterion. The second was to provide interfaces for the widest range of peripherals possible, and the third was to provide a growth path through a regular, uniform architecture.

The strengths of UNIX

UNIX is a clean, simple operating system with comprehensive capabilities. Highly modular, it consists of many separate processes that could fit within a limited hardware address range. Program development consists of small single-task modules that are later linked together; its interprocess controls allow very large applications to be developed and tested in modules. While a full UNIX system occupies up to 6M bytes of secondary storage, most modules are very compact.

Because the total UNIX system is large, it must be disk resident, and the system designer must provide fast and efficient disk access for the required memory swapping. This is particularly important in view of the tree structure of the UNIX file system which involves many indirect accesses. In a multi-user commercial environment dominated by file transfers and inquiry/response tasks, this directory structure poses a challenge. As system loading increases, the performance of an unaided central processing unit (CPU) quickly degrades with the overhead of handling interrupts and the associated

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memory swapping; this results in response times that suffer dramatically. Intelligent input/output (I/O) controllers and an efficient common memory manager can address some of these problems.

Design overview

The Plexus P/40 is a 16-bit multiprocessing minicomputer designed to rapidly integrate hardware and software. Its hardware essentially consists of off the shelf microprocessors, while its system design is a proven, high performance minicomputer architecture. Moreover, the I/O design, based on Intel's MULTIBUS, is easily understood and interfaced. Using industry standards, including the MULTIBUS backplane, the device has a storage module disk (SMD) interface, UNIX, and supports asynchronous, bisynchronous, and high level data link control/synchronous data link control (HDLC/SDLC) communications (Fig 1).

In addition, the P/40 provides intelligent I/O controllers, an efficient common memory manager, fast access through fast disks, and an intelligent SMD type disk controller supported by a direct memory access (DMA) channel to main memory. The technical design goal in using multiprocessors was to eliminate traditional bottlenecks on data transfer rates and interrupt handling so that the system performance would have only two technical limitations: disk access time (20 to 40 ms) and overall main processor performance.

The main processor, designated the job processor, is built around a 16-bit microprocessor and is responsible for executing user programs. Because its shorter instructions meant fewer fetches per instruction and in most cases faster execution, the Z8000 series was chosen over other microprocessors with larger address space. The nature of the design is such that, by distributing processing power throughout the system, a job processor can be chosen for its efficiency at particular tasks. The system's 8M-byte physical address space was considered more than sufficient for the initial markets; the present model supports 4M bytes.

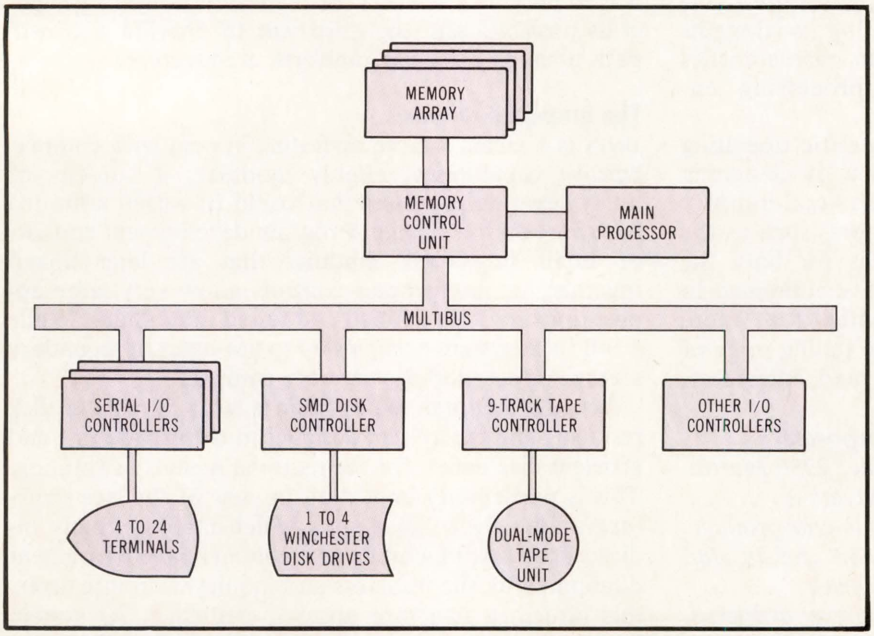

Fig 1 Plexus P/40 block diagram. System relies on IEEE 796 bus (MULTIBUS) to communicate with its I/O device controllers. For greater speed, system memory is on separate bus.

At least two other types of processor, also built around Z8000 microprocessors, assist the job processor—the intelligent communications processor (ICP) and a mass storage controller. These peripheral processors handle all interaction with terminals, printers, and disk and tape units independent of the main processor. Information is transferred between the peripheral processors and main memory using DMA techniques. Since each processor has its own DMA channel, the job processor is rarely interrupted. Multiple ICPs, job processors, and/or mass storage processors can be plugged into the MULTIBUS backplane.

The major issues affecting system design were how and what the auxiliary processors would communicate with the job processor, and how memory management would efficiently maintain control. UNIX made it fairly easy to resolve these issues since it is built on a set of small, relatively independent modules.

Job processor

Nearly all features of the Z8001 are used, including separate instruction and data spaces, user and system modes, and vectored interrupts. With 16 general purpose registers and 110 distinct instruction types, the job processor uses four address spaces. The normal I/O space is used to communicate with I/O ports on the MULTIBUS while special I/O space (SIO) is used to control the processor. Memory instruction and data spaces are used to access the corresponding locations in main memory.

An intelligent controller helps maintain high rates by offloading the main processor.

The job processor maps all normal I/O references to the MULTIBUS. When executing an I/O instruction, the processor requests control of the MULTIBUS through its bus arbiter. When control is granted, the processor places the port address on the lower 16 address lines (A0 through A15) and asserts the appropriate read or write control line (IORC or IOWC). After the addressed MULTIBUS port executes the command, it returns an acknowledge (XACK) to the processor, which allows the I/O instruction to complete execution and releases control of the MULTIBUS. If either the MULTIBUS is busy when the processor tries to execute a normal I/O instruction or if the port is slow in returning its acknowledge signal, wait states are automatically inserted to extend the I/O instruction. The job processor uses only word I/O instructions when accessing MULTIBUS ports. If the port only supports byte operations, the high order byte is undefined when the port is read and ignored when the port is written.

Job processor's SIO is used for system control, diagnostic, and housekeeping functions. Because efficient diagnostics are critical in a multiprocessor design, a special serial I/O port is used to connect a diagnostic terminal directly to the processor. A universal asynchronous receiver/transmitter (UART) with a programmable baud rate generator is used to create a single vectored interrupt to the job processor. To aid in software debugging, the job processor has a trace mode capability that generates a vectored interrupt whenever the processor fetches the first word of an instruction and is in normal mode. This feature can be used to single-step through programs.

In addition, the job processor has access to a counter/timer circuit (CTC). In normal operation, the CTC is used to divide the system clock down to 50 Hz to provide the job processor with realtime clock interrupts. A battery powered clock/calendar gives the job processor access to the time of day in hours, minutes, and seconds and will operate up to forty days without system power. This feature is critical as many UNIX utilities require the time of day to be correct. Additionally, the clock/calendar allows the system to go from power-up to a fully operational state without operator intervention. Power-up sequences are automatic and are initiated with an on/off switch.

To augment its capabilities, the job processor also contains an arithmetic processing unit (APU), which performs floating point addition, subtraction, multiplication, and division on 32- and 64-bit numbers in American National Standards Institute (ANSI) standard format. Software options are being explored for even greater speeds.

The job processor uses two Intel 8259A programmable interrupt controllers (PICs), each with eight interrupt request lines. The PICs are cascaded together in a master/slave configuration to give a total of 15 interrupt lines with distinct vectors. This may seem extremely low for a processor of this size, but only a few interrupts per second actually reach the job processor—the intelligent communications processors handle the rest locally while the DMA techniques further reduce job processor involvement in interrupt handling. When considering the auxiliary processors and the MULTIBUS interrupts, the system has hundreds of distinct interrupt vectors.

Here, a small design problem had to be overcome. Because the processor requires that all vectors be on an even boundary (bit 0 must be 0), the PICs cannot be connected in a normal manner. Instead, data line 0 from the PIC is connected to data line 1 of the job processor bus, and so on with PIC line 7 to processor line 8. Processor data line 0 is pulled low, which means that data must be shifted one line to the right when the PIC is read or written to.

Memory control unit

Efficient and proven memory management and error handling and correction are critical in a multiprocessor system, particularly since UNIX is rather intolerant of errors. To break a large amount of memory into small segments that enable the processors to find information faster, and to include error checking and correction is the system's concept. The memory control unit (MCU) takes requests for main memory, from both the job processor and the peripheral processors, and generates the proper signals to the memory array boards. Controlled by the job processor with SIO instructions, the MCU contains address mapping circuitry (Fig 2), error correction logic, and the dynamic random access memory (RAM) controller.

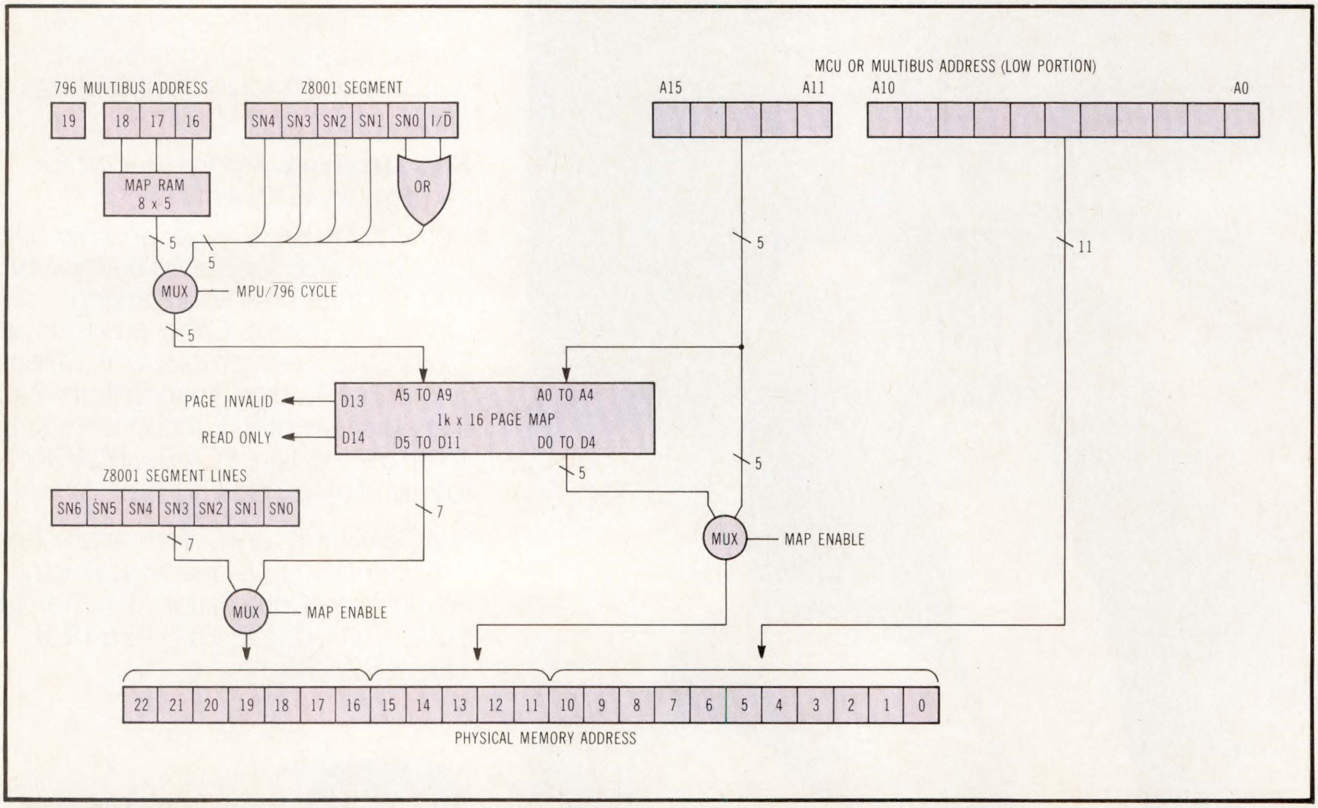

Fig 2 Memory control unit translates MCU and MULTIBUS logical data addresses into physical memory addresses.

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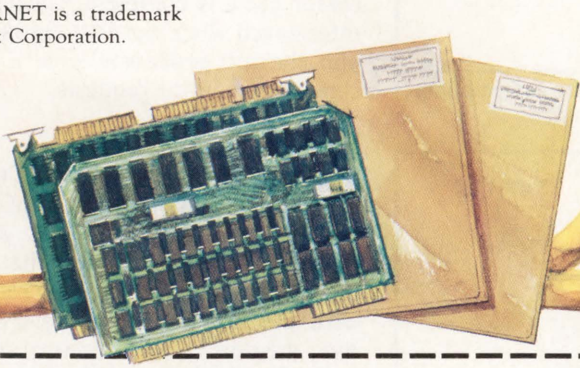

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In normal operation the MCU takes 21 address lines from the job processor or the MULTIBUS, then maps them into a 23-bit (8M-byte) physical address space. When the job processor accesses memory, five segment address lines and the 16 address lines form the address to the MCU. Segment line 0 is ORed with the instruction/data (I/D) line; this implies that the job processor can access data memory in segments 0 to 31, but instruction references can be made only to odd numbered segments (I/D bit = 1). Thus, running in segmented mode, the operating system has access to all memory segments, whereas user programs, which run in unsegmented mode, have access to one code and one data space.

Logically, the five highest MCU address lines select 1 of 32 map sets (Fig 3). A map contains from 1 to 32 2k-byte pages of memory. A typical process or program requires one map set for instructions and one for data. Minimum memory for a single program is 4k bytes, and the maximum is 128k bytes. Therefore, maps for up to 16 processes can be simultaneously resident in the mapping RAM, and if a process is resident in memory without a map slot, only one map slot for that process must be changed for the process to run. In other words, frequently called processes can be stored in memory without occupying map slots and be run very quickly without swapping the process itself in from secondary storage.

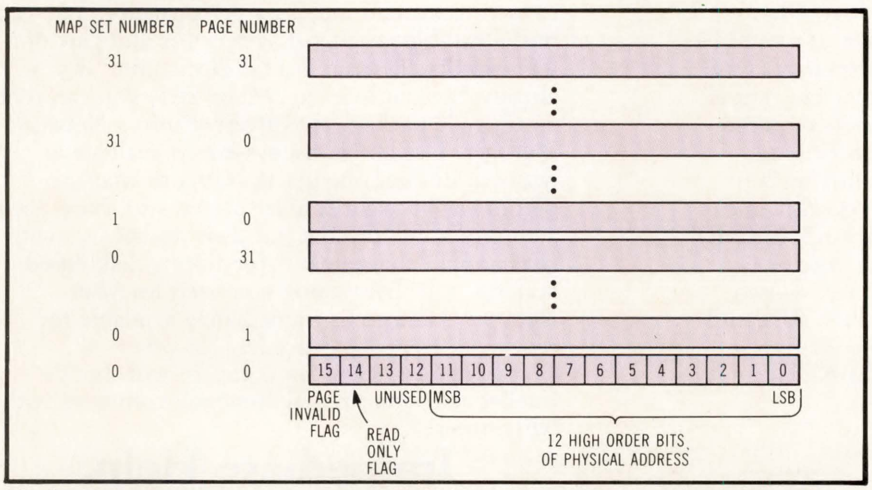

Fig 3 Page map RAM consists of 1024 16-bit entries. Map contains information used to translate between logical and physical memory addresses.

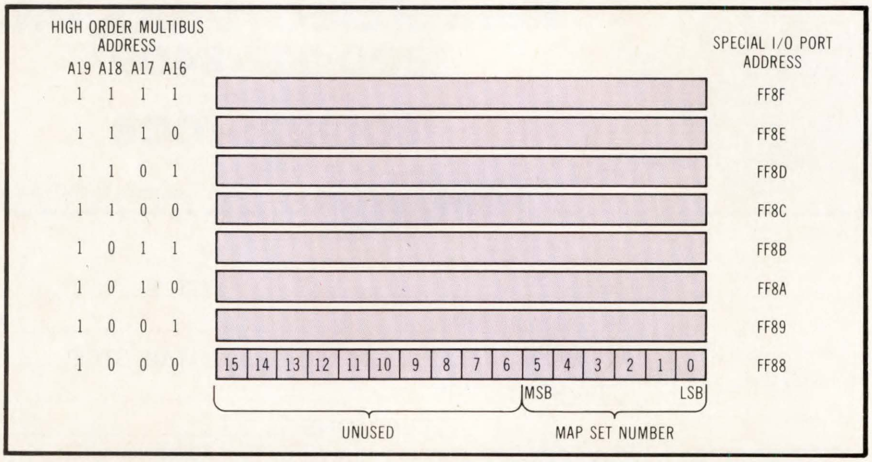

Fig 4 796 bus map contains eight 16-bit entries. Map translates data addresses on MULTIBUS into system memory addresses.

In addition to the page map, a MULTIBUS map RAM allows processors on the MULTIBUS to access memory through the MCU (Fig 4). This RAM can store eight map set numbers, allowing processors to simultaneously access eight of the 32 map sets.

Moreover, the MCU is responsible for error handling, checking each reference to memory for consistency with the attribute bits assigned to each page. Each page can be assigned a read only or invalid status. When a violation occurs, the MCU latches the address and map set number that caused the violation; the status information; and, for an error generated by the job processor, the address of the first word of the last instruction fetched before the error. The MCU determines whether the job processor or a peripheral processor generated an illegal reference and takes appropriate actions. If the job processor caused the violation, the MCU asserts the job processor segment trap line. For a MULTIBUS processor error, the MCU enables the job processor to take control of the MULTIBUS and notify the processor that an error occurred before the processor tries to transfer another block.

MCU arbiter

The MCU arbitrates between MULTIBUS processor and job processor requests for main memory. When a device wants to request a memory cycle, it asserts its memory request line to the MCU arbiter, which, in turn, asserts the memory grant line to the winning device. The grant line enables the device's address, data, and control lines, using a first come, first serve protocol when memory is not in use and interleaving requests when memory is active. For example, if the memory is inactive and the job processor requests memory, it immediately receives a grant and the cycle begins. If a MULTIBUS processor requests a cycle during the job processor cycle, it will not receive a grant until the job processor cycle is complete. Cycles are interleaved when the MULTIBUS port and the job processor issue a continuous stream of requests.

MULTIBUS memory port

The MULTIBUS memory port maps the upper half of the 1M-byte MULTIBUS memory address space through the MCU. When the port detects a MULTIBUS memory request with the high address bit (A19) active, the port requests control of the MCU through its arbiter. Then the port initiates the memory cycle and generates the acknowledge signals (AACK and XACK) when the cycle is complete. Generated a fixed time before the cycle finishes, the AACK is used by the peripheral processors to increase throughput. The port supports both word and byte memory accesses.

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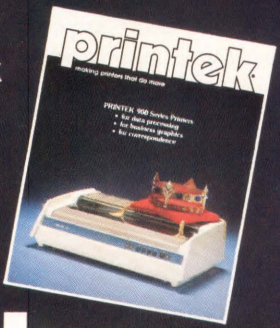

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Certain measures are taken when the job processor and the MULTIBUS processors share buffers in memory, because addressing conventions used by the job processor and the MULTIBUS byte are different. The job processor expects the high order byte in a word to be at an even address, while the MULTIBUS uses the opposite convention. Data can be accessed from the MULTIBUS or by the job processor without further consideration, provided they use independent sections of memory. When main memory is used as a common area for passing data between MULTIBUS devices and the job processor, data are stored in memory. (See Table, "Memory addressing.")

Memory addressing

	Even address	Odd address
MULTIBUS	RAM low bank data (0 to 7)	RAM high bank data (8 to F)
Job Processor	RAM high bank data (8 to F)	RAM low bank data (0 to 7)

When the job processor writes a byte into a location using an even address (eg, 1000H), it is placed in the high bank. If data from the same location are read from the MULTIBUS, low bank data are actually read. To read the correct byte, the next address location (1001H) is read from the MULTIBUS.

Dynamic RAM array. The dynamic RAM boards contain 128k or 512k 22-bit data words, each logically made up of a 16-bit data word and a 6-bit error correction field (modified Hamming code). The error correction scheme detects and corrects single-bit errors and detects double-bit errors. In addition, the arrays contain basic support functions such as address decoders, buffers, and row address strobe/column address strobe multiplexers. All control, address, and data lines come from the MCU over a dedicated bus, taking power and ground from the MULTIBUS connector.

Intelligent communications processor

A powerful, intelligent device, the ICP contains a processor, memory, eight serial ports, one parallel port, and DMA channels associated with each port. Typically, it handles all low level buffering and processing necessary to support a variety of terminals, modems, and printers. The eight RS-232 serial ports are implemented with universal synchronous/asynchronous receiver/transmitters (USARTs). Asynchronous baud rates from 50 to 38.4k are selected for each channel by programming a CTC counter/timer. Character length, parity, and the number of stop bits are also programmable. Each serial port can support asynchronous, bisynchronous, and HDLC/SDLC protocols.

The ICP communicates with the job processor using command and status blocks located in main memory. Data transfers between the ICP and main memory are controlled by the ICP's processor, thus further freeing the job processor of any time-critical interrupt handling.

The ICP uses a Z8000-series 16-bit microprocessor. Always operated in the system mode, there is no separation of instruction and data or special and normal I/O spaces. The ICP contains 16k bytes of programmable read only memory and 32k bytes of RAM with parity arranged in two 16k x 9 banks. The processor can directly address 64k bytes of memory, with the lower 48k resident on the ICP and the upper 16k mapped into main memory via the MULTIBUS and the system MCU. Parity generation and checking are enabled or disabled by the processor.

DMA techniques. The ICP uses a combination of software and hardware to simulate a DMA. Data are moved to and from main memory via block move instructions executed by the ICP processor. Since the upper 16k bytes of the ICP's address space are mapped into main memory, the ICP processor executes a block move from the middle 32k bytes of memory to the upper 16k bytes when it wants to move data into main memory. It programs a CTC channel to provide a pulse every n seconds, nominally 1 to 2 ms but tunable, depending on the application. This pulse goes to the MULTIBUS arbiter and causes it to request the bus. When control is obtained the arbiter sends an interrupt to the ICP processor, which initiates a block move of approximately 32 words. The size of the block is also tunable depending on the application. After the move is complete the processor signals the arbiter to release the bus. When no blocks remain in the DMA queue, the ICP processor disables the CTC channel so that no more interrupts are generated.

The nature of the design is such...that a job processor can be chosen for its efficiency at particular tasks.

This technique moves 64k characters/s, or the equivalent of eight terminals running in burst mode, and uses less than 10% of processor bandwidth. It allows a DMA task to run in the background without monopolizing either the MULTIBUS or local bus, and it leaves a great deal of the ICP processing capabilities free for tasks such as executing segments of UNIX, table conversions for data communications protocols, terminal handling programs, and other local processing tasks.

Port handling is also done with DMA channels within each ICP, which allows all eight ports to output simultaneously at a 19.2k-baud maximum asynchronous rate. The DMA function is provided by three Intel 8237 DMA chips, which are programmed by the processor to transfer one byte, then release the local bus to the processor. This ensures that the ICP processor will get at least every other memory cycle.

Based on the Z80A PIO, the parallel port is also DMA supported. Control logic associated with the port generates all control and handshake signals necessary for the DMA to transfer data to a line printer without processor intervention. The port sends a vectored interrupt to the processor if the printer asserts the fault line.

MULTIBUS arbiter and interface. Using the parallel arbitration technique, the MULTIBUS arbiter on the ICP requests the MULTIBUS every time a processor controlled timer circuit reaches a 0 count. When control of the MULTIBUS is obtained, the arbiter locks BUSY and interrupts the ICP processor, informing the processor that it can begin a transfer to main memory. The processor

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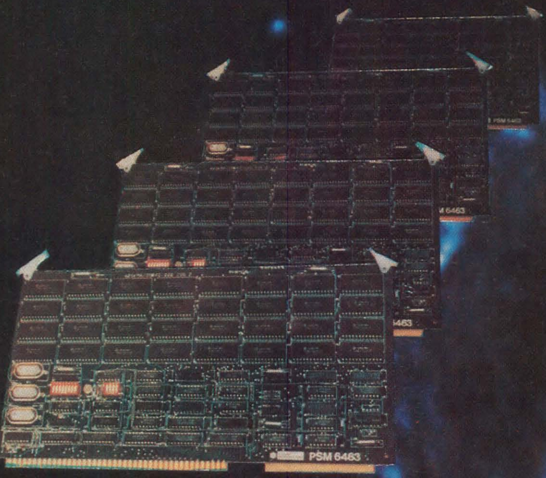

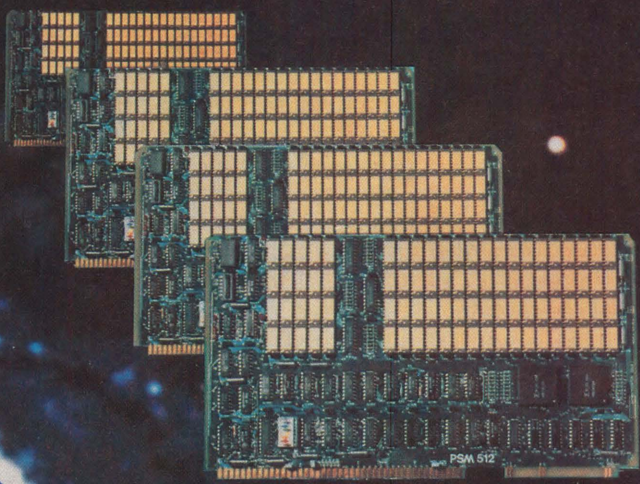

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resets the arbiter and releases the MULTIBUS when the transfer is complete.

A master that supports only 16-bit memory read and write operations, the MULTIBUS interface allows the processor to assert one of the eight MULTIBUS interrupt lines (INT0 to INT7). It initiates a MULTIBUS memory cycle when the processor performs a memory operation in the upper 16k bytes of its address space, which are mapped into the system's main memory. Addresses are formed by linking a 6-bit port with the 14 least significant processor address lines, forming the 20-bit MULTIBUS address. Nine peripheral chips in a daisy chain generate vectored interrupts. A translation circuit makes the interrupt vector produced by the peripheral chips compatible with the ICP processor.

Disk and tape controllers

The disk controller is an intelligent device that supports up to four drives. High performance SMD disks were chosen for the system because a wide range is available from many vendors (20M bytes to 1G byte), allowing systems integrators to precisely match disk capacity with applications, and also, because of its size and flexible file system, UNIX requires frequent disk accesses. As the UNIX file system is tree structured and file space is not preallocated, most accesses consist of several indirect accesses through directories. Thus, a very fast disk and disk controller supporting high transfer rates are desirable for UNIX based minicomputers. DMA channels provide the 3-MHz bandwidth for these rates.

An intelligent controller helps maintain high rates by offloading the main processor. The job processor simply sends the disk addresses and lengths of the blocks to be transferred; the controller's intelligence allows it to send a very large number of blocks, provided the MULTIBUS is not busy.

Built around an Intel 8089 16-bit I/O processor with 10k bytes of memory, the controller is capable of performing multiple-sector operations that span tracks, as well as automatic error detection and correction. It uses a 32-bit fire code to detect 22-bit burst errors and correct 11-bit errors in a way that makes its operation transparent to the job processor. Like the ICP, the controller receives commands from the job processor by reading a control block in main memory. But unlike the ICP, which controls the MULTIBUS for transfers of about 32 words, the disk controller can be interrupted after each word by higher priority MULTIBUS interrupts. While preventing data transfers from tying up the MULTIBUS, it allows the full 1.2M-byte transfer rate of the SMD disks.

The technical design goal...was to eliminate traditional bottlenecks on data transfer and interrupt handling.

The magnetic tape controller supports up to four industry standard 9-track, 0.5" tape drives. These are dual-mode units to support streaming as well as start/stop operation. Like the disk controller, it uses an 8089 I/O processor and has its own local memory. Since it maintains record buffers in main system memory, there is no limitation on tape block length.

Conclusion

While the job processor can be expanded from 256k bytes to 4M bytes and beyond, up to eight job processors, ICPs, and mass storage controllers can be configured in a single system. This results in a mid-range minicomputer with expansion to 24 terminals and 580M bytes of disk storage. Another growth path is through networking—not by adding even more power to the processor, but by adding another processor. This multiprocessor approach of using industry standards makes networking extremely easy. Since the ICP is a general purpose computer in its own right and can be downloaded, it can be programmed to handle Ethernet, X.25, or other network protocols. Its overall performance is roughly that of a PDP-11/70 or the high end of the 16-bit Eclipse systems, at approximately one-third to one-half the cost.

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High 707 *Average 708* *Low 709*

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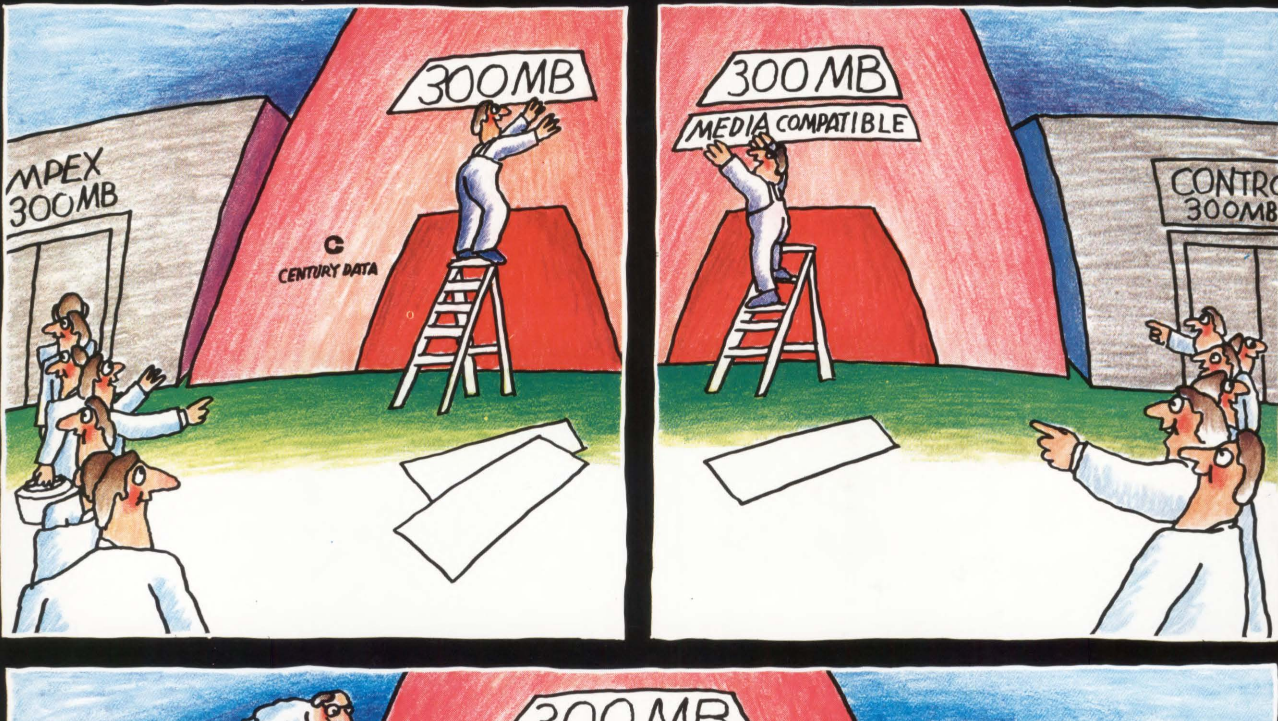
Drives for the 80's



Century Data's new T306 disk drive: It's what a lot of 300 MB-removable users have been waiting for.

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Continued on next page

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Needless to say, Mr. Amerson likes our Tridents a lot. We think your customers will like them, too. Why not give us a call, today, and get the details.

T306 *Continued from first page*

a catamaran head shape significantly improves aerodynamic performance.

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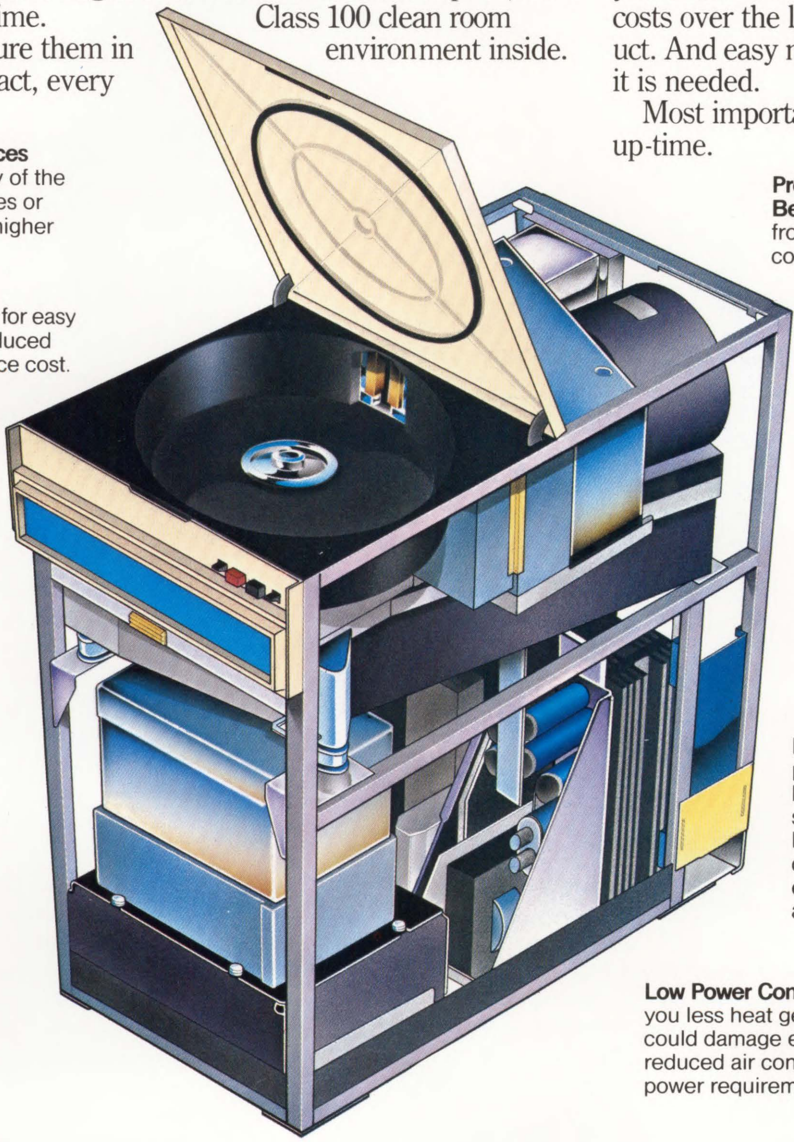

Parallel Disk/Head Surfaces assure far greater stability of the head over uneven surfaces or dust particles, providing higher data integrity.

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Plug our system into your system for mass storage that gives you extreme reliability, has the highest cost efficiency, and Winchester/tape file loading and unloading without downtime for the operator.

The secret is transparent, prioritized commands. While our new T-Series Marksman is fully or selectively backing up data onto ¼″ streaming tape, direct requests from the CPU for access to data files on the disk can be given higher priority. The user is unaware of any time lapse as the back-up function is interrupted, the user's data need is fulfilled, and the back-up function is resumed, without further host system intervention.

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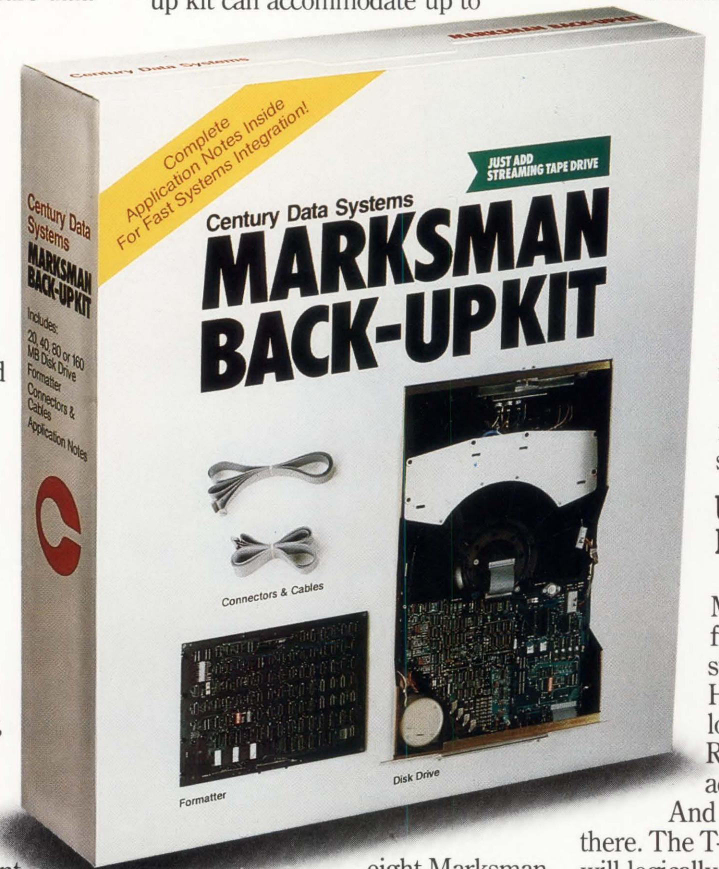

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MAKING THE MOST OF MULTIPROCESSING FOR MICROCOMPUTERS

Microprocessor system performance limitations can be minimized through use of multiprocessing techniques

by W. Y. Yue and R. P. Halverson

Design for maximum efficiency of the most expensive resources has been a prime directive in design of computer systems. But now, the era of the multiprocessor has arrived, and with it have come changes in the traditional manner in which engineers approach design considerations. Although the assumption that greater utilization of resources yields greater gains is still valid, the relative cost of system building blocks has changed drastically in recent years. Today, peripherals—not processors—represent the most costly design element.

Advances in semiconductor technology have inverted the cost of the central processing unit, local read only memory and random access memory, and input/output modules with that of the higher cost of peripherals, making relatively cheap computing power available. However, to design for maximum efficiency and economy, the engineer must keep the expensive peripherals busy. The design consideration today lies with the speed of the multiprocessing unit (MPU). Many fast peripherals that interface directly to local storage through direct memory access (DMA) could be used to the limit of performance if the overall data transfer rate were not compute-bound.

Unfortunately, many applications are compute-bound, and the least expensive resource, the MPU, limits performance. Furthermore, MPU speeds have not kept pace with local storage speeds. Although they may require fast access storage devices, none of the currently popular MPUs can effectively utilize data transfer rates possible with even the lower cost members of today's read only memory (ROM) and random access memory (RAM) families. Multiprocessors can serve to answer these needs, improving performance (for small added cost) by sharing high bandwidth RAM and ROM among two or more MPUs.

Most widely employed MPUs are able to support shared bus multiprocessor systems. For example, Intel's 808X family uses HOLD and HLDA or RQ and GT signals to provide orderly bus control switching. Zilog's Z8X family has similar signals, BUSRQ and BUSAK. But use of these signals for shared bus operation does not accomplish the multiprocessing objective, since only one processor at a given time is active on the bus. The timing of these MPUs is such that simple bus control and arbitration logic can mesh bus transactions of two or more MPUs together. They become transparent to each other with little degradation in performance.

Fig 1 illustrates the timing diagram for the Intel 8086 MPU. Each bus transaction requires at least four clock pulses, called timing states. Timing state T1 is used to issue and latch address values. Write data out and control signals (not shown) become stable during state T2 and remain so until state T4. Data in lines are sampled near the trailing edge of either the T3 clock or, for slower devices, the last of the wait (TW) clocks which are inserted between T3 and T4.

The address latch enable (ALE) signal issued during state T1 begins every bus transaction; it is, in effect, a bus request signal. Read transactions end 10 ns after the trailing edge of the T3 clock. Bus writes could end during state T2, since all needed data are then available.

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R. P. Halverson is staff consultant for Data Flo Corp, 1301 Cambridge Ave, Hopkins, MN 55343. Mr Halverson was formerly an associate professor in the electrical engineering dept of the University of Minnesota, where he also received his PhD degree, and has served as a consultant to several computer systems design firms.

Total time for all four states in a 5-MHz 8086 is 800 ns—more than twice the cycle time of a typical dynamic RAM. Thus, most memory chips are less than half-utilized when running with a 5-MHz microprocessor. On the bus, states T2 and T3 are active; and states T4 and T1 represent wasted time which could be well used by another MPU.

A practical example

Employing two microprocessors is the system design depicted in Fig 2. The two 8086s each have fully buffered address, data, and control access to the system bus. A single 8284 clock generator circuit provides 15-MHz clock (OSC) to the bus arbitration logic, 5-MHz clock (CLK) to both microprocessors, and 2.5-MHz clock (PCLK) to peripherals and RAM refresh counter. Local storage uses both 2716 electrically programmable read only memory (EPROM) and 4116 RAM. Peripheral chips include an 8253 programmable interval timer (PIT) and several 8251 universal synchronous/asynchronous receiver/transmitters (USARTs). Each microprocessor has its own 8259 programmable interrupt controller (PIC) connected to the MPU side of the bus buffers.

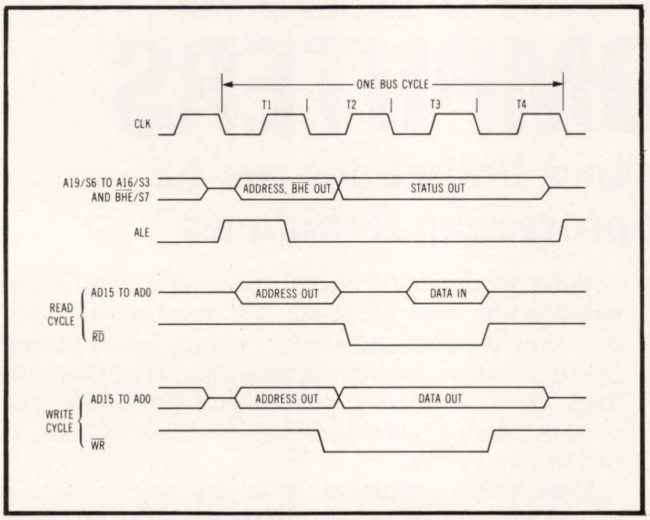

Fig 1 Timing diagram for 8086 microprocessor. Since at least four timing states (800 μs at 5 MHz) are required for each bus transaction, typical RAM chip operates at half speed when used in conjunction with single 8086 processor.

Bus control logic arbitrates requests from three sources—the two MPUs and the RAM refresh logic, as shown in Fig 3. Priority order is MPU 1 first, refresh second, and MPU 3 third. This order ensures that distributed RAM refresh can never be locked out for more than two or three states. Since the RAM refresh occurs approximately every 13 μs, the possible preemption of the MPU 2 bus cycle only slightly degrades the MPU 2 performance. DMA request arbitration logic could be added in a similar way. If DMA transfers always reference 256 or more successive RAM addresses (128 words) within 2 μs, the transfers could replace the RAM refresh request.

A timing diagram of several bus transactions is shown in Fig 4. The bus grant latch is clocked by a signal derived from the clock generator and driver's OSC and CLK signals and the bus busy (BBSY) flipflop, so that bus grants change soon after CLK. BBSY ensures that each bus transaction takes at least two clock periods. The WAIT flipflop inserts one wait state for bus requests to EPROM or input/output (I/O) devices, thus ensuring adequate access time to these slower devices. The dynamic RAM's row address strobe (RAS) and column address strobe (CAS) timing is also shown in Fig 4.

Hardware semaphore

Multiprocessors contending for shared resources can interfere with each other unless a semaphore mechanism exists to lock others out while a processor executes critical code. In maximum mode configuration, the 8086 features a lock prefix instruction to drive a signal line that hardware can use to prevent bus access by other devices during a "locked exchange." However, this mechanism does not exist in minimum mode 8086, or in most other microprocessors.

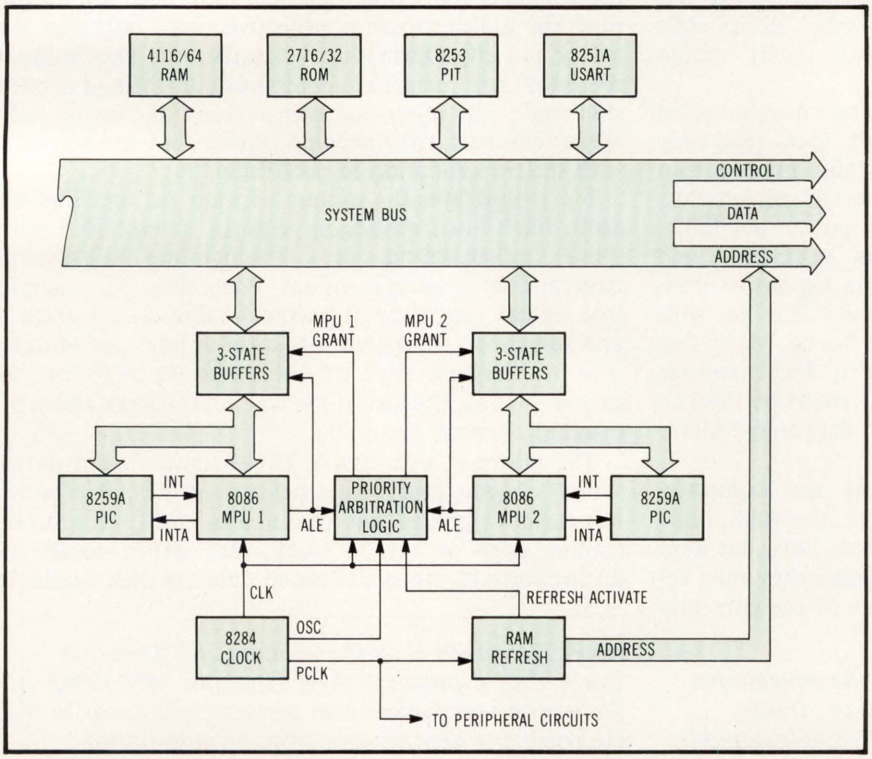

Fig 2 Dual processor system. Performance increases when more than one processor shares memory. In system depicted, external clock provides timing signals for bus arbitration logic.

A simple lock flipflop is used in this microprocessor system to accomplish the same purpose. Second rank of this double-rank flipflop is one bit of the status word read by instructions IN 00 or IN 02. The bit indicates whether the system is locked or unlocked. IN 00 clears, and IN 02 sets the first rank; transfers from first to second rank occur at the end of each bus transaction. A processor that reads the status (with IN 00) and finds the system unlocked can then manipulate semaphores in memory associated with the critical resources or code. Further status inputs (even on the next bus transaction) will find the system locked. After testing

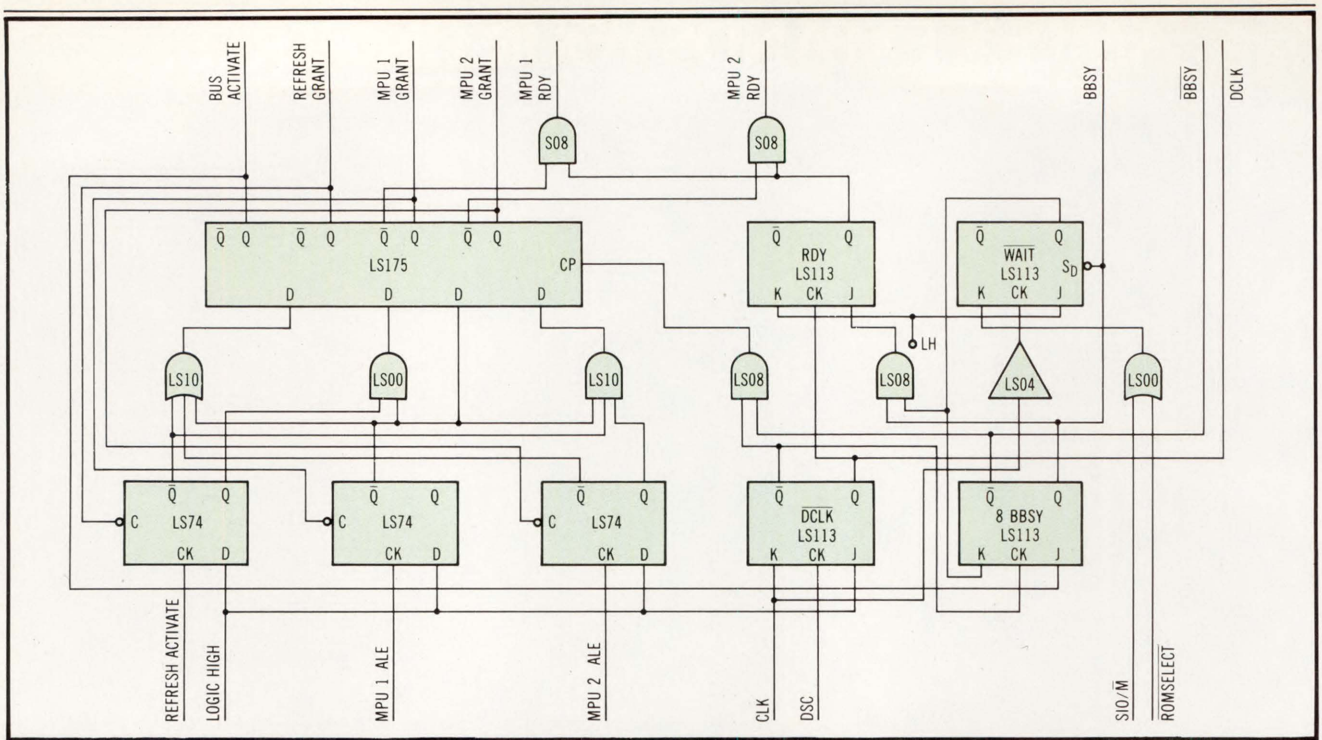

Fig 3 Bus arbitration logic diagram. All important RAM refresh takes place between MPU bus requests and overrides MPU 2 when necessary.

or setting the memory semaphores, the first processor executes an IN 02 instruction, which again unlocks the system for other processors. Another bit of the status word is an "identity" bit derived from the grant logic, which identifies the processor (0 or 1) so that decision branching is possible during interrupt controller initialization.

Since a concurrent coprocessor conceptualizes a multiprocessor system, it is important that the interrupt structure be provided for smooth efficient task switching. Some hardware interrupts that may occur in a multiprocessing system include

- realtime clock "tick" interrupts, used by the operating system to reallocate processor resources equally among several users;
- I/O interrupts such as ready/requests from slow peripherals that avoid time-wasting busy/wait loops; task completion and error exception interrupts from peripheral controllers or DMA devices that are capable of substantial independent activity before requiring processor service;
- event notification interrupts that require immediate processor attention, such as "power is failing."

In addition, a software interrupt scheme, if available, can be used for system resource calls or job termination notification to the operating system.

Ideally, an interrupt in a multiprocessor system should be serviced by the processor that is executing the lowest priority task. In a multitasking operating system with symmetrical treatment of processors, any given processor may be executing the lowest priority task at the instant of interrupt.

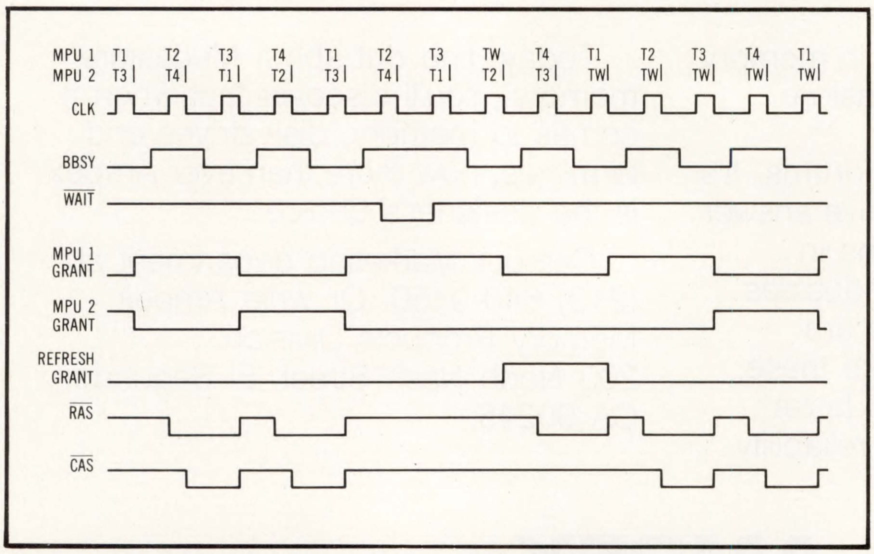

Fig 4 Dual processor bus timing diagram. Wait states are inserted when necessary to allow slower system elements and procedures to catch up with processors.

To communicate task priority to interrupt controllers complex hardware must be used. Also, the required handshaking signals (INT and INTA) between the 8086 MPU and, for example, the PIC make a fully symmetrical dual processor interrupt system difficult to design. In the system described here, each processor has its own PIC, wired to the local side of its bus buffers. Judicious distribution of interrupt signals between the two controllers helps to avoid excessive interrupt service by either processor.

The 8086 employs a vectored interrupt scheme, with the interrupt vector supplied by the interrupt controller. It is permissible for both PICs to issue the same vectors, since one of the bits in a status input identifies the processor. Thus a processor

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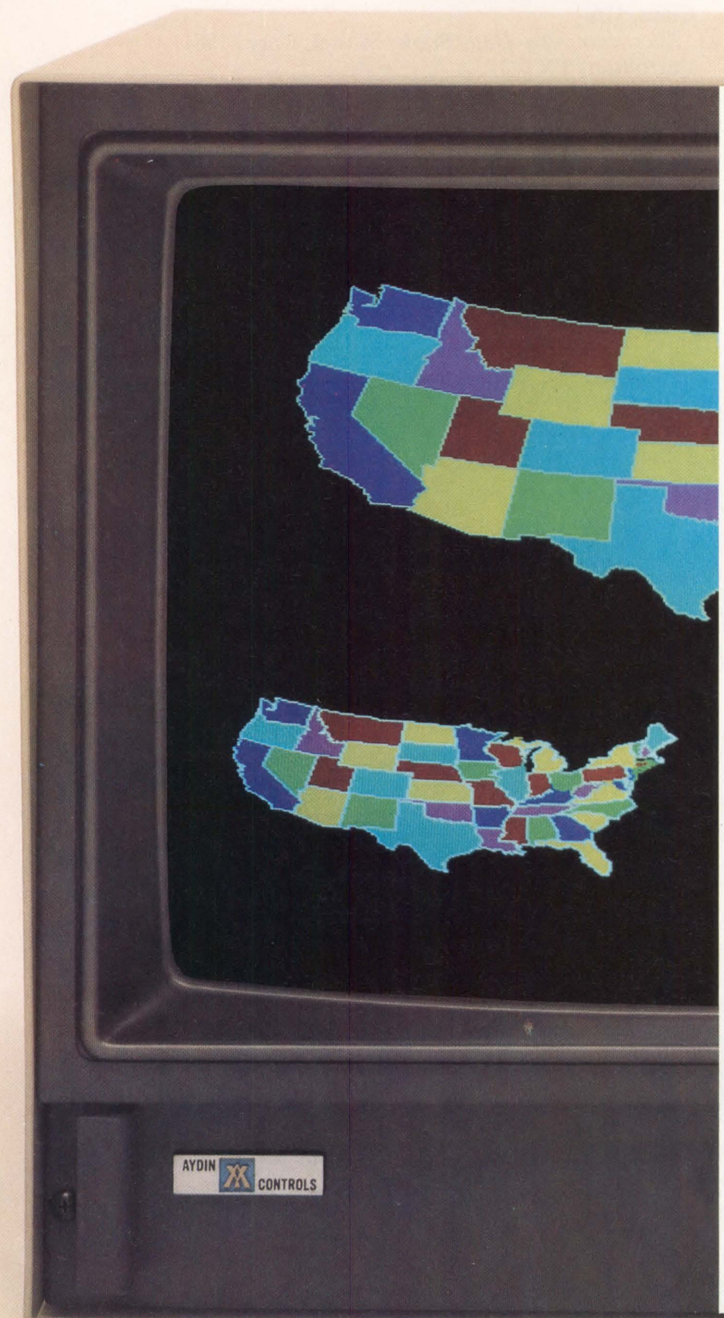

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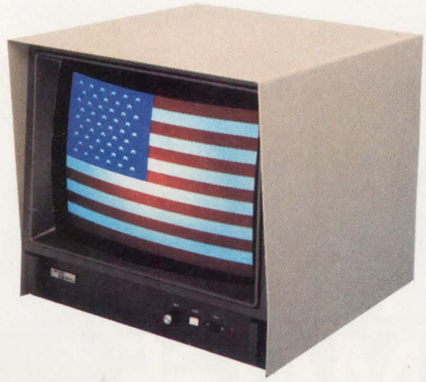

AYDIN CONTROLS

executing common code can branch to a routine unique to its interrupt. The same test can also be used to separate the code to initialize each processor's PICs for different interrupt vectors.

Software considerations

In many applications, high performance microprocessors are capable of serving several users simultaneously. Multi-user operating systems have been written to control such usage in a multiprogramming context. Software extension, however, of such operating systems to run in concurrent multiprocessors can be difficult. Since an 8086 assembler was not readily available to test the concurrent operation of the two MPUs as described here, a small operating system was modified by hand assembly to support two 8259A PICs and two 8251A USARTs. At initialization, each processor was forked to a different segment of code using the identity input to initialize its own 8259A PIC and assign nonconflicting data and stack segments in RAM. Only one MPU was allowed to initialize the 8253 PIT under locked (critical code) conditions because of chip recovery time restrictions. A fork at the entry to each I/O driver causes each MPU to control a separate USART in a unique assignment.

With these changes, two separate terminals run the same operating system independently, sharing most of the code in ROM. However, this scheme makes a fixed assignment of one MPU to each port, and does not allow a processor to handle overload computing from the other.

A better approach would be to implement an interrupt driven multitasking operating system such as that described in Intel's *8086 Family User's Manual,* application note AP-6. In this scheme, interrupts to either or both processors dispatch them to a multi-priority multiple task program which allocates processor time on the basis of user needs. If both processors execute common code, the test and lock feature described above can keep the processors from interferring with each other as task programs are assigned. Throughput of such a system should approach or exceed that of two independent microcomputer systems which duplicate the resources shared in this design.

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Z80 Microcomputer Data Book, Mostek Corp, 1981, Carrollton, TX

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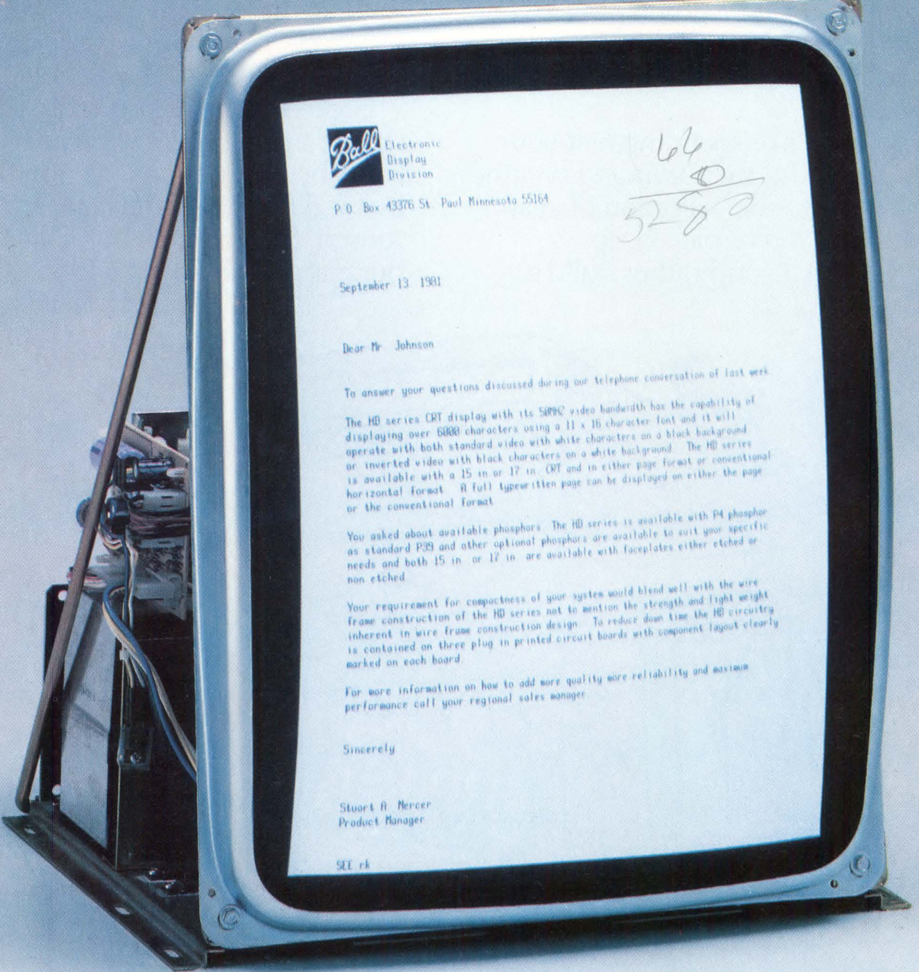

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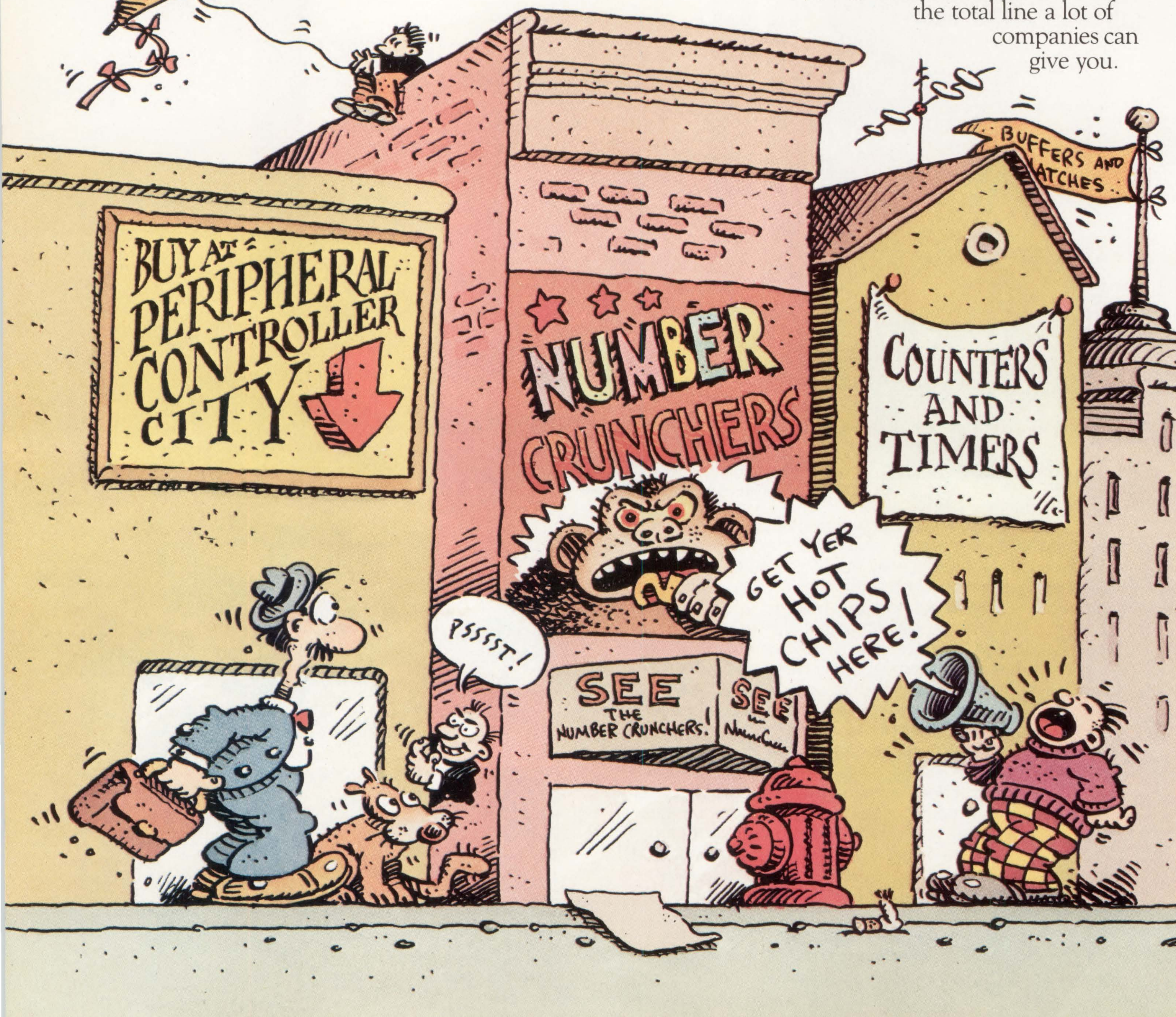

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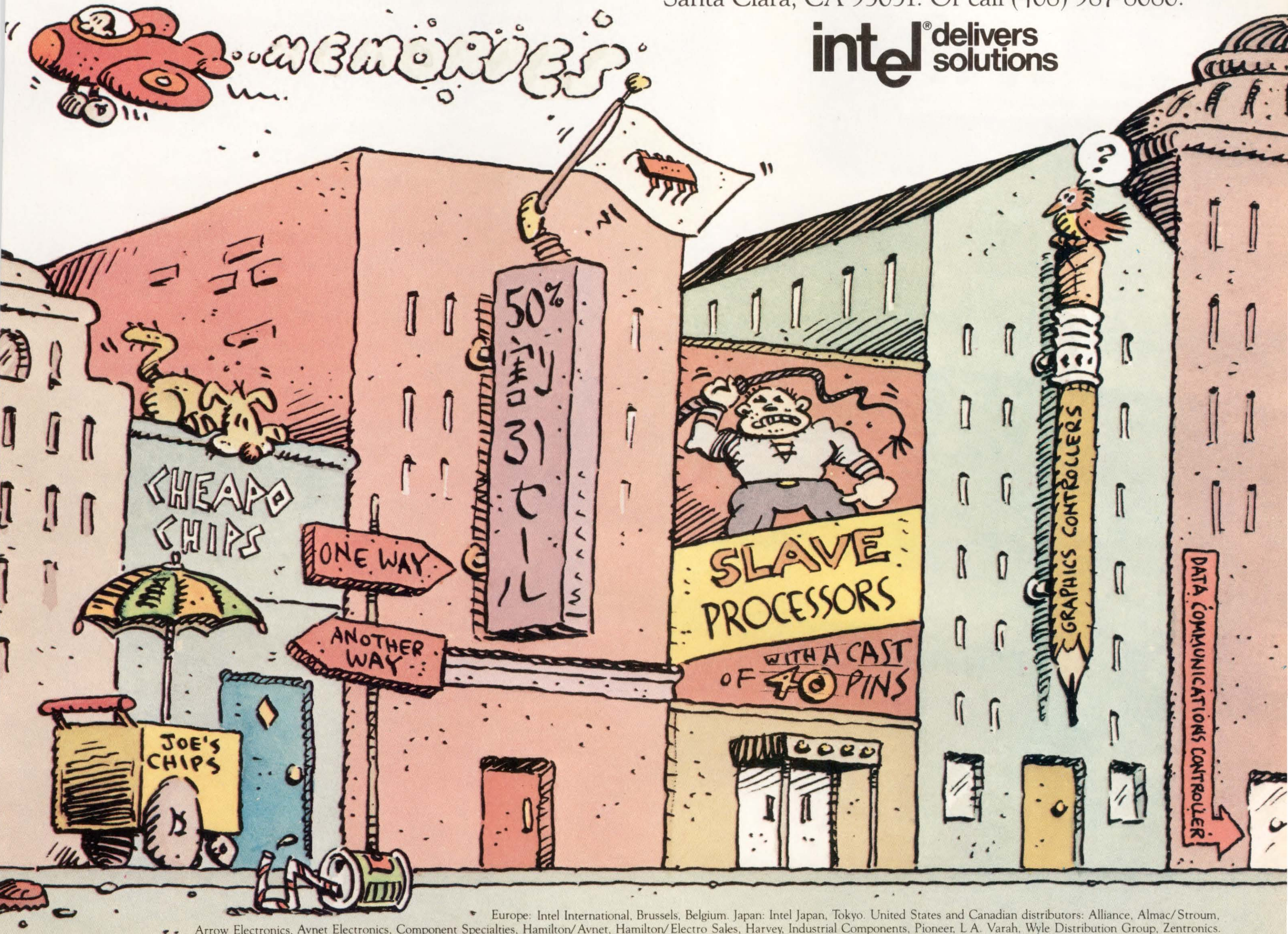

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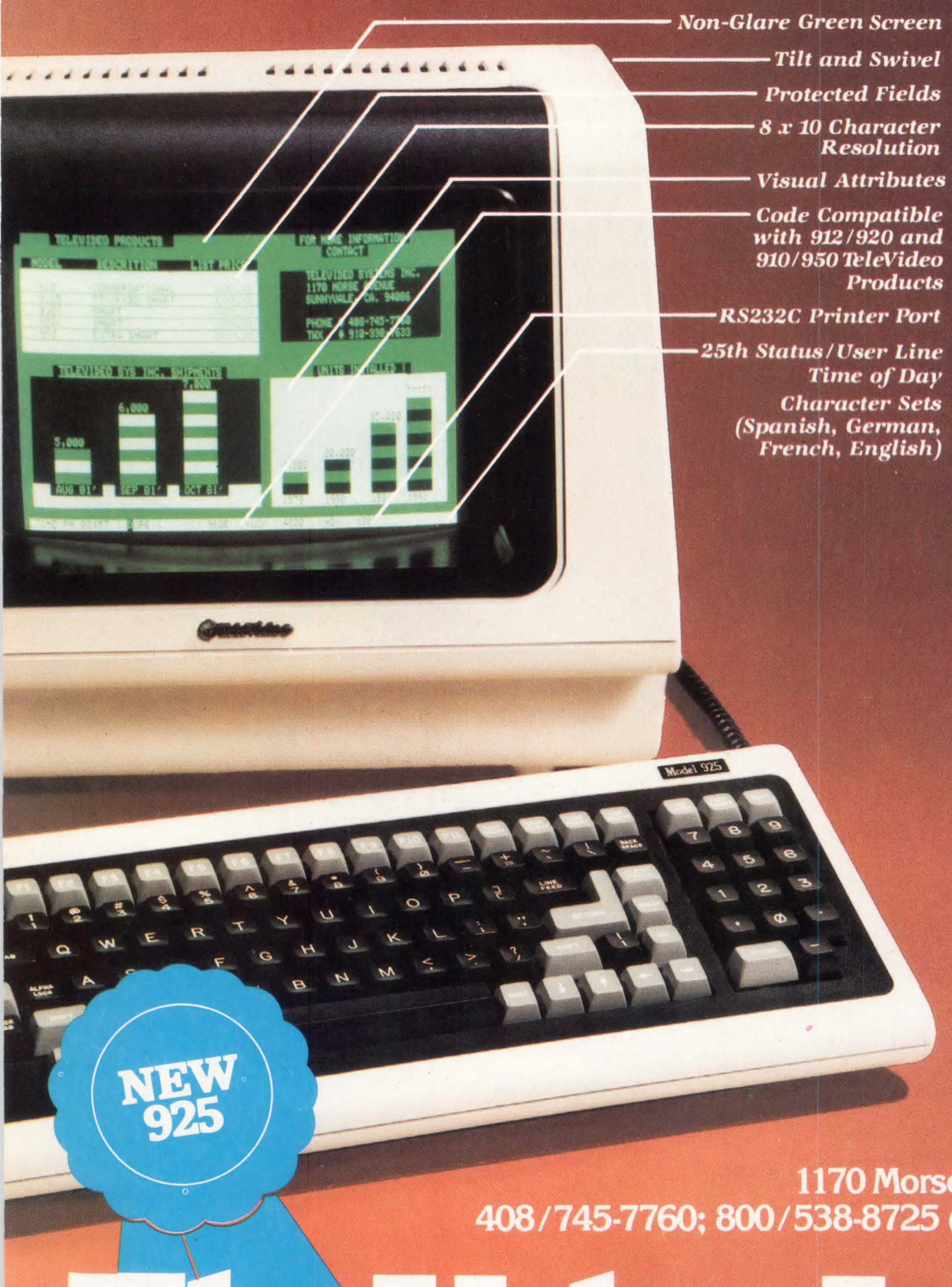

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CIRCLE 63 ON INQUIRY CARD

SERIAL BUS FOR INTRA-TERMINAL DATA TRANSFER

Use of a serial data bus concept in point of sale systems provides flexibility, uninhibited debug, uncomplicated manufacturing, and straightforward maintenance

by John E. O'Neil

Functions of intelligent terminals, especially those used in point of sale applications, have expanded beyond mere data entry sequencing and cash control. Complexity in these applications is increasing and terminals are playing a more pervasive, active role in the banking or retail business systems of which they are a part. In addition to integration of the credit authorization function, successful product lines will offer direct connection to accounting and inventory systems and access to shared data bases (Fig 1).

A terminal must be flexible because many of these systems are already in place. Varying requirements on peripheral device characteristics that a terminal must support also suggest a flexible approach. For example, a printer may or may not be required to print in two colors, print alphanumeric data or upper/lowercase characters, or print on inserted forms such as charge slips. A quiet printer may be more desirable than a fast one or vice versa; a given terminal may need one or perhaps multiple printers. This diversity is manifested by a rash of terminal hardware configurations, each of which uses the same central processing element (Fig 2).

Modularity is the recognized technique in achieving flexibility. In this case, modularity can be effected by partitioning all hardware specific to a given device onto a device controller card that can be plugged into the terminal/system when necessary. This is not a new concept; minicomputer companies have been using it for years. In general, the choice must be made between a modular, systems oriented approach to hardware design, and a customized approach using unique interfaces optimized for specific devices. In the modular approach, one must be careful to provide configurability at the proper level. The intent is to provide devices that are readily installed and removed. Losing sight of this is easy when considering how empty a given device controller may be, how easy it is to combine two controllers into one, or how much more of a given resource a controller can handle. Thus a device providing 16 control lines could be more desirable than one providing 64.

As processing power cost decreases, the modular approach becomes more attractive in applications where hardware component cost was previously prohibitive. The systems approach should also benefit with lower manufacturing and service costs; this must be weighed against component cost. Self-contained microprocessors are useful tools for modular design and are becoming comparable in price to much less intelligent devices, such as universal synchronous/asynchronous receiver/transmitter (USART) and programmable input/output (PIO) chips.

As modularity is an essential ingredient of a flexible system, this draws attention to characteristics of the backplane or bus where pluggable modules reside. The degree of flexibility a modular design offers will depend on the strength of the connection between modules, in this case printed circuit boards (PCBs). The less complex the bus used as the connection, the more flexible the resulting system.

Configuring a terminal for a specific application is simply a matter of connecting a universal main logic board to the appropriate device controller boards at final assembly. Situations in which two devices are

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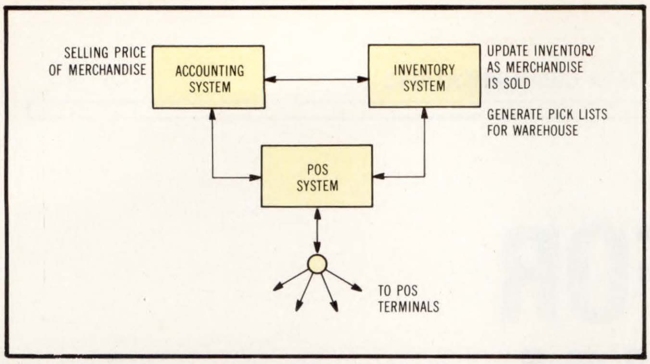

Fig 1 Functions in simple point of sale (POS) configuration. Paper paths between these systems create bottlenecks that hinder timely data transfer.

made mutually exclusive by requiring the same interrupt lines on a bus are undesirable. In order to avoid such situations, software and hardware interdependencies must be confined to individual boards. The presence or absence of any given board (with the exception of the main logic board, which must always be present) does not affect another board. Optimally, only the application program will be affected as the device configuration changes.

Flexibility within cost constraints is the design goal. Thus, a look at the required performance level is in order. The application calls for a simple I/O bus to be used for data exchange between a central processor board and device controller boards. By and large, the peripherals run by the device controller boards interact with a human terminal operator. As a result, data rates supported by what is usually thought of as a bus are not required. Speed can be traded off for simplicity, flexibility, and ease of reliable implementation as design goals.

A new approach to the I/O bus

A network approach to an I/O bus, the Intrabus™ technique uses a common 2-wire cable assembly connected to each device controller board and to the main logic board (Fig 3). One wire is a signal line; the other a common ground return. The bus is inherently serial and half-duplex. An asynchronous transmission format is used even though it is not the most efficient scheme possible. However, the simplicity it offers outweighs the better line utilization of synchronous transmission or other more complex schemes.

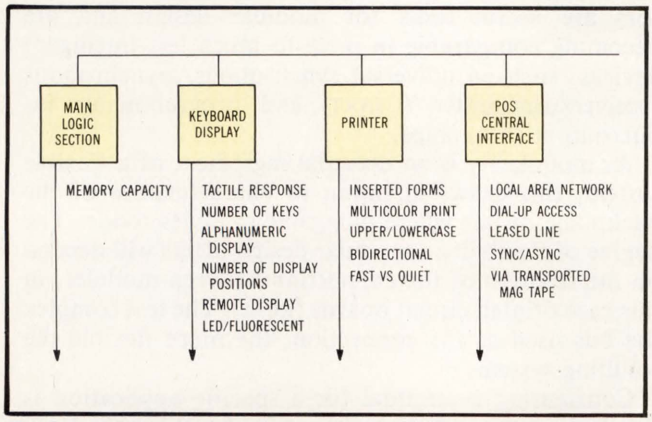

Fig 2 POS terminal hardware menu. Variety and number of options demonstrate need for design modularity and flexibility.

Data are transmitted in ASCII at 9600 bps, allowing the use of line monitors to view bus traffic. A contention protocol approach is used because of its simplicity. The excellent connectivity offered by contention has not proved to be of much significance in the application. Collision does not introduce the degradation expected in a contention environment because bus traffic arrives in sequenced, rather than in random, fashion.

Hardware component cost of the network approach is acceptable and offers free advantages, many of which derive from extending device independence to a hardware level. Usually, a device driver must be written for each device and the operating system implements device independence by invoking the appropriate driver. It should be emphasized that the benefits realized are the result of using an architecture designed to fit the application—a common, I/O channel for communication among PCBs. Many implementations of the channel are possible, such as a polled approach where the main logic board acts as the network host. As another alternative, much higher data rates can be achieved using various forms of synchronous transmission since the clocking implied allows the receiver to lock onto the beginning of each bit time with high accuracy. As synchronization occurs at the start bit which begins each character, asynchronous implementations drift at the bit level.

Bus interface

The Intrabus technique uses the Intel 8041A (UPI-41A) as the bus interface. Each connection to the bus requires this device as a bus controller. It is a convenient device to use since it is designed to be a user programmable peripheral controller that can connect directly to a master processor's bus. The 8041A contains three registers that are available both internally and to a master processor: input, output, and status. As masked for the bus, the 8041A can be thought of as a smart universal asynchronous receiver/transmitter (UART) with a built-in communications protocol.

Software in the bus controller is organized into four major sections—software UART, bus interface, protocol state processing, and main processor interface—each of which can be viewed as an independent state machine, driven by events relevant to it. The highest level control flow within the bus controller is as follows:

```
DO FOREVER
   PERFORM bus interface
   PERFORM main processor interface
ENDDO
```

The protocol state processing section is PERFORMed by the bus interface when a properly addressed error-free packet is received. Once started, the software UART section is interrupt driven. An interrupt caused by a start bit on the bus initiates the receive mode. Transmit mode is initiated on command of the protocol state processing section.

Alternative implementations

Using an entire microprocessor as a bus interface may seem unusual. Indeed, there are other possible implementations of a shared I/O channel for communication between a main logic board and device controllers. The tradeoff involves use of the central processing unit as a

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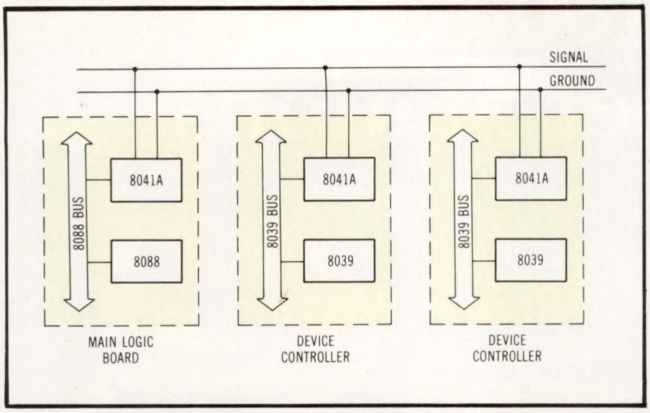

Fig 3 Architecture of Intrabus technique. Each connection to bus requires 8041A universal peripheral interface as bus controller. It converts CPU data and handles bus contention protocol.

means of simplifying interconnection, as opposed to a more complex bus where a given board connects only to the bus lines it needs. A bus controller with self-contained read only memory (ROM), random access memory (RAM), and interface hardware does not require excessive board space while the overall cost compares favorably to other methods of interfacing microprocessors.

For example, although much higher bandwidth is possible for a parallel bus with eight data lines, it is unnecessary. Some form of a byte-wide bidirectional buffer will be required at each device unless an 8041 type processor with its built-in buffering can handle the peripheral and interfacing to the bus. Ribbon cable with its relatively expensive connectors will probably be required and will introduce crosstalk problems. While a backplane or motherboard circumvents these effects to a degree, the geometry of board placement inside a cramped terminal may not permit it as a solution.

A strong argument can be made for the use of a less intelligent device, such as a UART, to serve as the bus interface device. There are advantages to the processor approach, the relative importance of which is application dependent. One advantage is that a very simple point to point protocol can be used as the data link between a main processor and its bus controller. This simplified protocol requires less memory to implement since it need not deal with the complexities of the protocol used to communicate over the bus. Also, the RAM contained in the 8041A reduces realtime constraints on a board's main processor because it buffers up to 16 characters at a time. This allows the main processor to ignore the bus controller during critical device service periods, and to catch up during less critical intervals. A self-contained microprocessor with enough RAM can buffer an entire message and thus become a store and forward device. This eliminates all bus controller imposed realtime constraints on the main processor. As a result, much higher data rates can be implemented on the bus without placing higher throughput requirements on processors that desire to use the bus.

Intrabus addressing—simplicity

Any bus on which addressing is done by message content rather than wires, by use of dedicated bus lines, offers the advantage of simplicity because the main logic board hardware remains the same no matter how many devices are connected. Though attractive at the low end, point to point approaches using dedicated unique interface electronics become cumbersome as devices are added.

A 2-wire bus reduces cabling used for the data link between boards to a minimum. As all boards share a common data link, it is possible to construct a universal test fixture. This fixture has to satisfy variable power requirements of the board under test, but can achieve a go/no-go level test by supplying the appropriate scenario on the bus.

Using a contention protocol permits identical software to run in each bus controller so that only one mask is needed for the 8041A. The excellent connectivity offered by contention, where any two nodes on the bus can directly communicate, is more important in a local area network (inter-terminal) than in the intra-terminal environment, since in the latter case traffic tends to be routed to or from the main logic board. The loss of throughput at high loading, usually suffered by contention schemes, is not experienced since bus traffic is strongly time sequenced and collisions are rare.

The Intrabus technique tolerates changes in the I/O device configuration with minimum customization. Changing or adding devices that connect to the bus will only affect the application program, as it must communicate with a device at a different address. The change is transparent to the operating system because it is capable of routing messages to any valid bus address and it does not perform message processing specific to any device.

Adopting any interface standard carries with it the benefit of reusable software. The main processor code that interfaces to a bus controller only has to be written once for each type of processor.

The less complex the bus...the more flexible the resulting system.

Intrabus processing—reliability

Most popular microprocessor bus architectures are high speed, parallel designs intended to provide a maximum data rate for general purpose distributed processing. They are capable of supporting tightly coupled microprocessors that communicate indirectly via shared memory. Attached resources may or may not be intelligent, and therefore may or may not be able to gain control of the bus. The essential architectural difference between these bus structures and a microprocessor bus is the capability for more than one bus master. As they are no more tolerant of noise than a microprocessor bus, care must be taken to isolate them from it.

Although incapable of satisfying the most demanding multiprocessing applications, a bus that requires all connections to be intelligent has reliability advantages. The protocol implemented on the bus protects all data exchanged between boards. Additional error detection/correction can be implemented between cooperating nodes. For example, data to be displayed are not as critical as transaction data being transmitted to a recording device. Errors are transient and immediately apparent in the former case but not in the latter.

Presence of a bus used exclusively for I/O tends to localize microprocessor bus runs. In the ideal case, the

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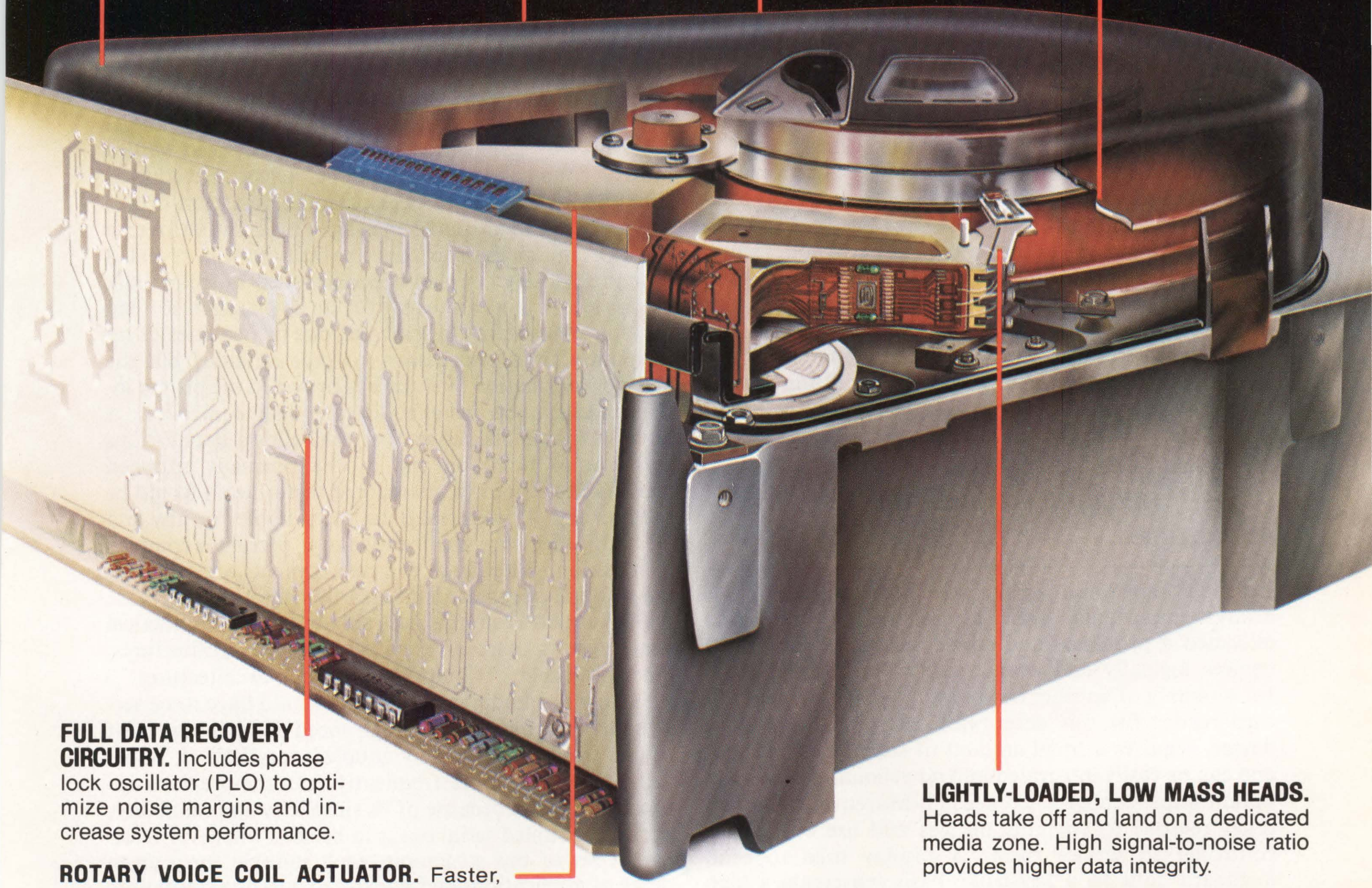

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I/O bus is the only bus not totally confined to one PCB. Unforeseen requirements for additional memory can prevent this ideal from being realized because memory must reside on the bus of the processor that needs it. Nevertheless, other than for memory expansion, an I/O bus can serve as a universal data highway. This confines processor bus runs to printed circuit etch and avoids signal quality loss caused by connectors degrading over time, a problem suffered by all expanded bus systems to some degree.

The connectivity of the Intrabus system is minimal—a signal and a ground line. This implies a long mean time between failures since so few line drivers and receivers are involved. In addition, if a bus controller or its associated support circuitry fails in a way that makes the bus unusable, this will be detected by the other connected bus controllers. Nodes can be disconnected one at a time until the remaining bus controllers can communicate; this always identifies the node with the failed components. A continuity test of the two bus lines and the successful communication between any two nodes eliminates the bus as a problem source. Therefore, the lack of any bus lines used exclusively for addressing aids troubleshooting. Because of the short bus length and relatively low transmission speed (9600 bps), transmission effects such as ringing, echoing, and line capacitance are not noticeable.

...a bus that requires all connections to be intelligent has reliability advantages.

Proper partitioning of functions among processors is always important. Each device is not necessarily allocated a processor and connected to the bus; some devices logically and economically fit as an optional subassembly of another device. A magnetic stripe credit card reader fits this description. It is an inexpensive device, requires a small amount of support electronics, and can be easily integrated into a keyboard device as an option implemented when needed. Moreover, there are other reasons to combine devices and use one device controller to service them. A display used to echo keyboard data on a keystroke basis represents a high degree of interaction between two devices. Any time two devices must communicate directly, consideration should be given to combining them. The bus is intended to support flexible terminal configuration and assembly by providing a universal link between the main logic board and device controllers. Providing all devices with intelligence and connecting them to the bus to accomplish this is unnecessary. Yet, as improper combination of devices will adversely affect modularity, each case must be carefully considered.

Conclusion

Serial data transmission has its place as a data bus architecture. When the required data rates are not demanding and flexibility is important, the serial approach is optimal. Many distributed processing applications require nothing more involved, and offering more bandwidth on a bus than will be needed is not advantageous.

Another key aspect of distributed processing is the nature of communication required between processors.

Comparison of bus architectures

Bus Architecture	Shared Memory	Noise Tolerance	Fault Detection	Cabling
Parallel Closely Coupled	yes	difficult to attain	difficult to automate	may need backplane
Parallel Loosely Coupled	no	yes	easy	average
Serial Loosely Coupled	no	yes	easy	simple twisted pair

Some applications require the very high performance offered by tightly coupled approaches, where memory is shared and communication is indirect. However, if high performance is not required, it should not be implemented. Any application that can be serviced with a loosely coupled design should be. Error detection is simplified when inter-processor communication occurs explicitly via identifiable messages transmitted over a bus. Often, analysis of an application will reveal a potential loosely coupled approach such as smart bulk memories. It is not unusual for an application to read multiple disk sectors in search of one or two lines of information. It is unnecessary to pipe anything but the desired information over the bus provided the proper intelligence can be installed in the disk controller. A down-loadable disk controller that allows applications software to build on top of the normally supplied primitive functions (read/write at sector level) would be satisfactory. A universal data bus suitable for any and all multiprocessing applications is at present a complex proposition. When high end requirements are satisfied, the low end becomes unnecessarily complex.

Backing off from this desirable but as yet impractical goal suggests a set of application-driven architectures. (See the Table, "Comparison of bus architectures".) The most demanding applications would have to be serviced by a closely coupled high speed parallel bus. Next in line would be a loosely coupled parallel bus, hopefully used much more frequently than the previous approach. Finally, because of its simplicity and reliability, a loosely coupled serial bus is to be used whenever feasible. A set of bus structures, each suitable for a given range of applications and integrated into one computing system, seems to be a reasonable design philosophy.

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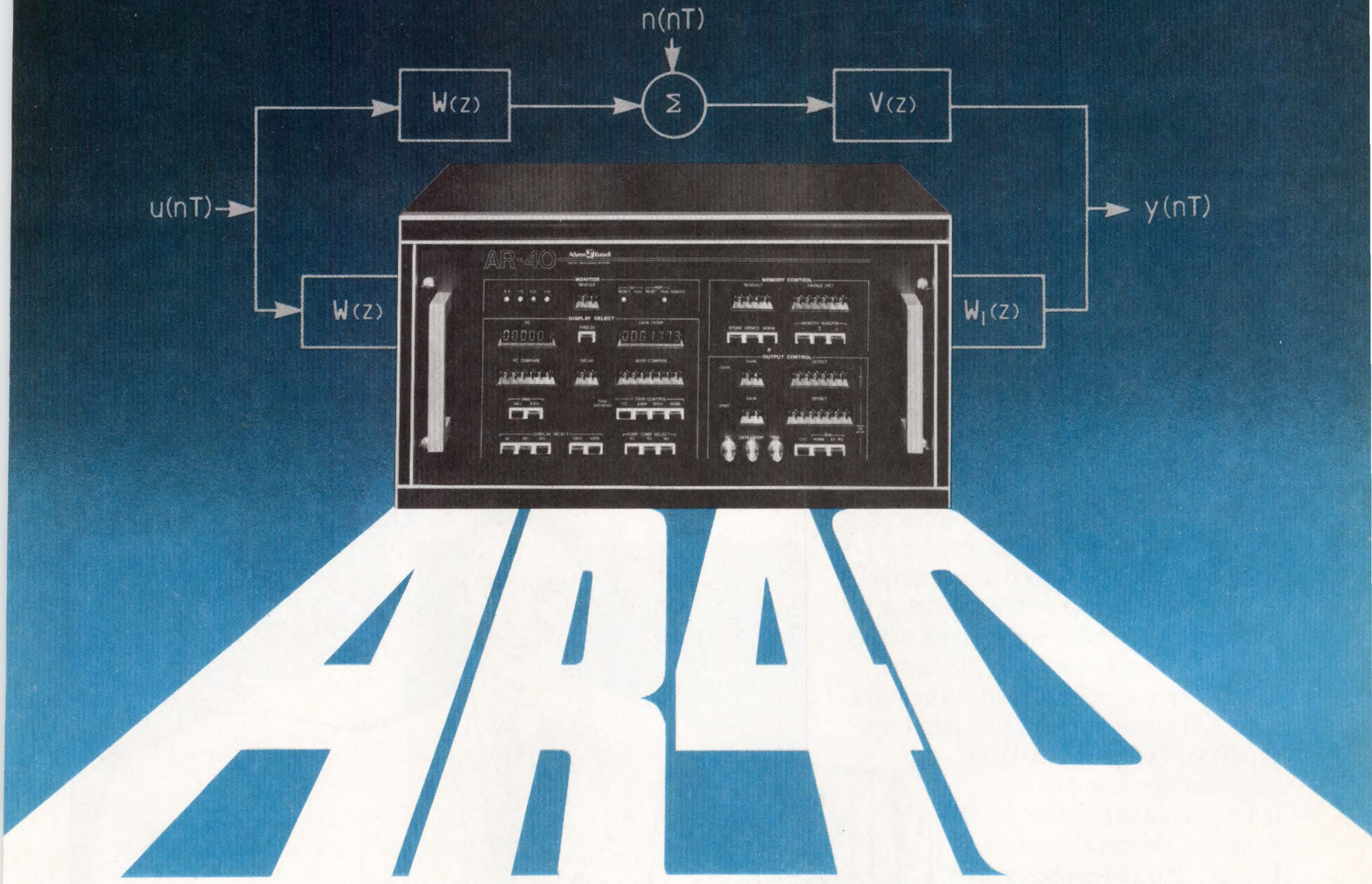

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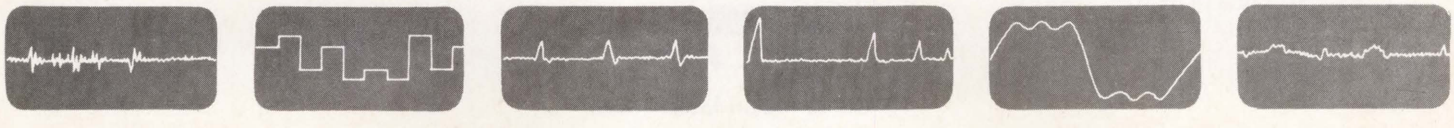

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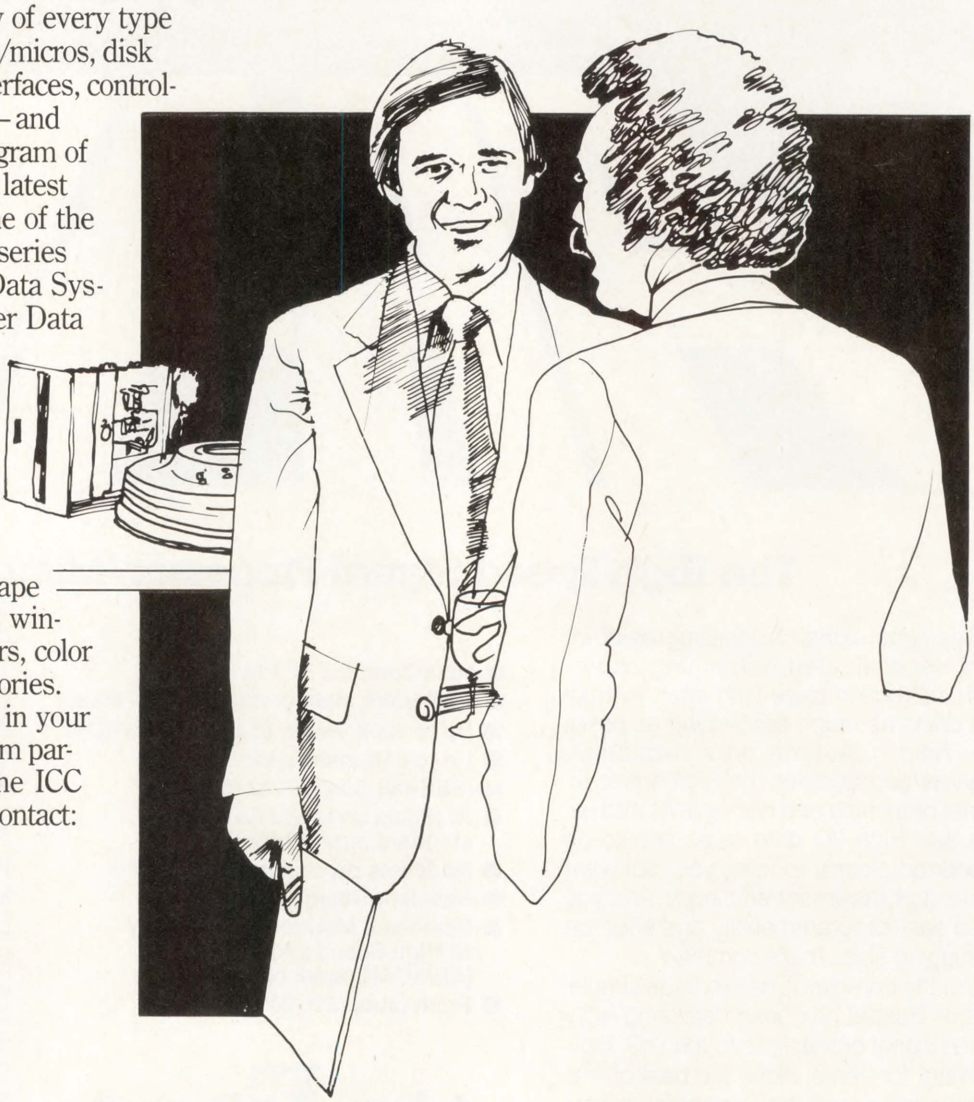

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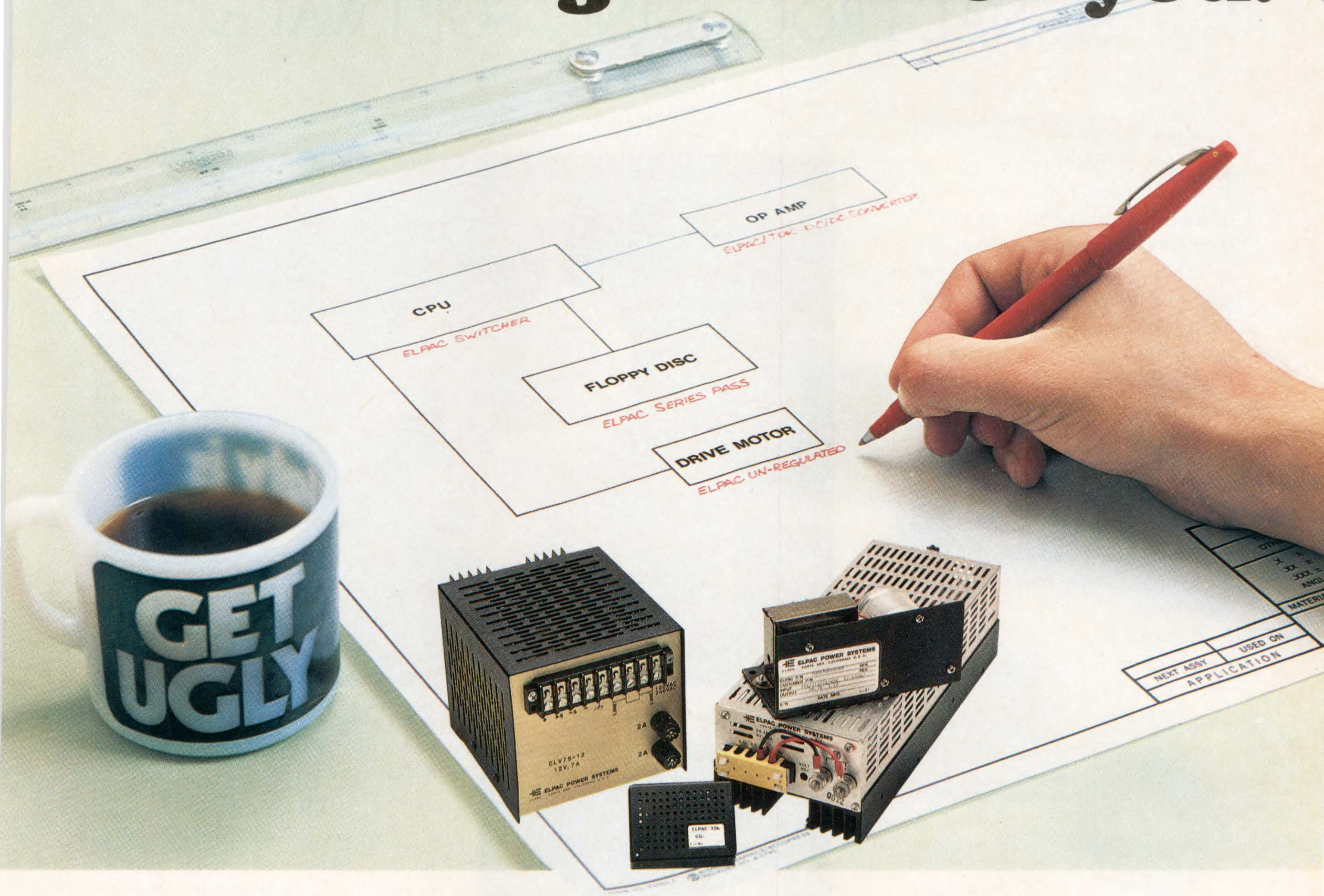

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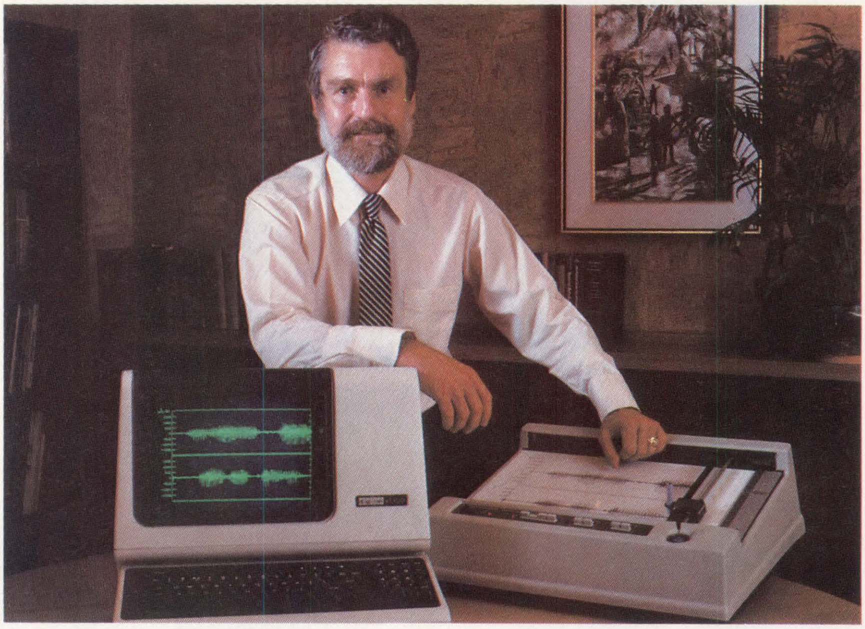
BY A.H. "STEEN" GRAY, Jr., Ph.D.
Vice President, Signal Technology, Inc.

I've been in this business long enough to know that some things never change. The "make or buy" quandary as it applies to software is a good example. "We've got some expensive programmers; let them earn their keep." How many times have you heard that when you've suggested buying a program package that seems perfectly tailored to your application?



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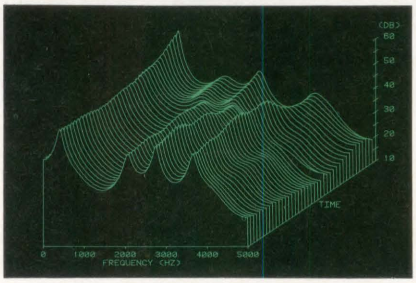

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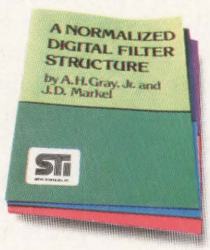

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CIRCLE 69 ON INQUIRY CARD

DUAL-BUS DESIGN FOR A MICROCOMPUTER

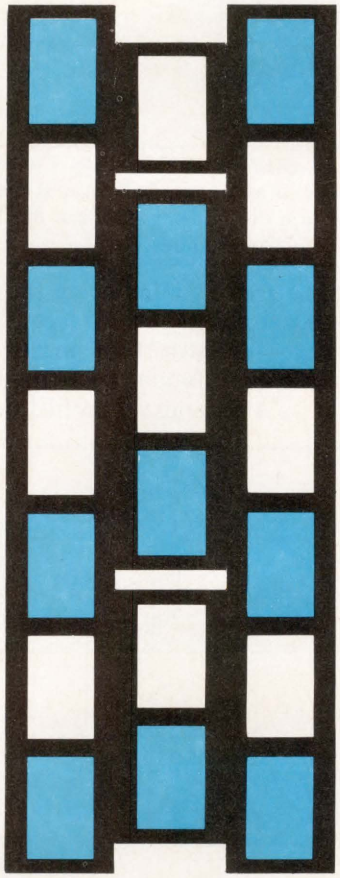
Improved performance and increased memory availability result when a microcomputer's resources are divided along common and applications lines

by Robert A. Garrow

Unified bus structures are common in most minicomputer designs. The approach combines on a single bus the support of both common primitive facilities, such as the central processing unit, and those unique to the application. However, advances in both the physical and functional density of large scale integration, together with the creation of universal bus standards for microcomputers, have made possible a dual-bus architecture that can provide several distinct advantages over a unified bus. The dual-bus approach creates a division between common and unique functions, allowing the user to economize with the available low cost computing power, while reducing the risk of hardware obsolescence.

With the dual-bus architecture, common resource functions and unique applications functions reside on separate buses. Parallel processing that matches the user's speed, increased memory capability, protection and isolation of common and application resources, and independence of application resources from common resource upgrades are all advantages innate in the dual-bus concept. In addition, application equipment does not need to be altered if common function capabilities are improved, preserving the user's engineering investment in valve added components.

Common functions of local bus architecture used in a family of workstation computers include human interface, computer mass storage interface, and input/output. These functions support the basic functions necessary for any specific application, including communication between operator and workstation, information processing, storage and retrieval of data, and communication with peripherals and networks. (See Fig 1.) Proposed IEEE bus standard MULTIBUS is the application bus illustrated with the system; the system contains from two to five MULTIBUS compatible card slots, depending on the configuration.



Dual-bus advantages

A dual-bus configuration in which the local bus supports a 16-bit microprocessor and an optional coprocessor, while the MULTIBUS supports application dependent hardware, provides significant advantages not offered by a unified bus system. Optimizing operation and speed of either the main processor or coprocessor and associated memory and peripheral capacity, the local bus masters also use a bus arbitration protocol that is more efficient than the bus request/acknowledge protocol used on the MULTIBUS. The two processors share instruction stream and use a request/grant handshake that is synchronized by a shared clock to speed processor interaction. Direct memory access (DMA) anticipates when the bus will

Robert A. Garrow is vice president of engineering and cofounder of Convergent Technologies, 2500 Augustine Dr, Santa Clara, CA 95051. Prior to the formation of the company, Mr Garrow was director of engineering at Intel's Microcomputer Development System Div, and is a codeveloper of the MULTIBUS. A holder of several patents, he is a graduate of the University of California at Berkeley with a BS degree in electrical engineering.

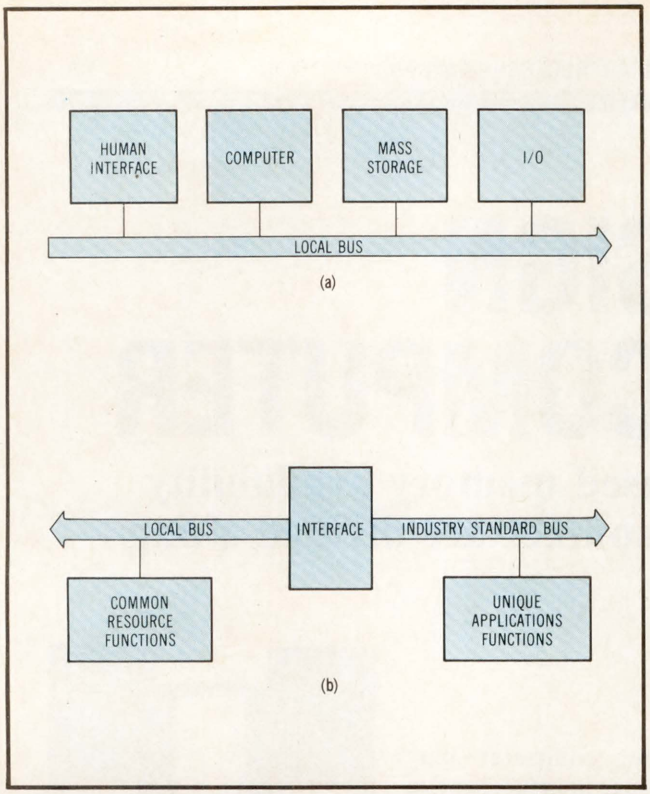


Fig 1 Dual-bus architecture. Common functions (a) can be optimized and upgraded without disturbing applications hardware on industry standard bus (b) while interfaced to the common facilities.

become free by monitoring the central processing unit (CPU) status lines. Faster access to local memory than is possible for MULTIBUS masters results. Such speed enhancements would be virtually impossible to implement on a generalized unified bus.

By controlling access of MULTIBUS signals to the local bus (a task handled by the local MULTIBUS interface), the local bus can protect itself and its memory resources from unauthorized or electrically anomalous interaction with the MULTIBUS. Although the MULTIBUS can access specifically defined local bus memory addresses, it cannot access local bus input/output (I/O) either directly or through DMA. Only five interrupt lines are shared between the two buses; all other lines are reserved for single bus intervention.

Since they remain electrically separate, the local bus and MULTIBUS support parallel processing. The local processor and MULTIBUS CPU operate simultaneously and independently, as long as neither requires access to the other's resources. In addition, the MULTIBUS effectively doubles address space to 1M byte available on the local bus.

Common facilities

Details of the common facilities are presented in Fig 2. Human interface permits interaction between operator and workstation by means of a keyboard and video display. The 16-bit processor (supported by an optional numeric processor) with random access memory (RAM) and read only memory (ROM), provides computing power. A realtime clock, interval timers, and interrupt control complete the CPU support. High speed DMA (I/O) and disk controller interface enables communication with the mass storage subsystem, while the printer and two serial communications channels provide I/O functions.

Processors, CPU, and memory. The standard CPU is a 5-MHz 16-bit processor, operated in maximum mode. Using a 6-byte instruction queue, the CPU achieves high performance through its 16-bit internal data path, 16-bit external interface, and instruction prefetch. This

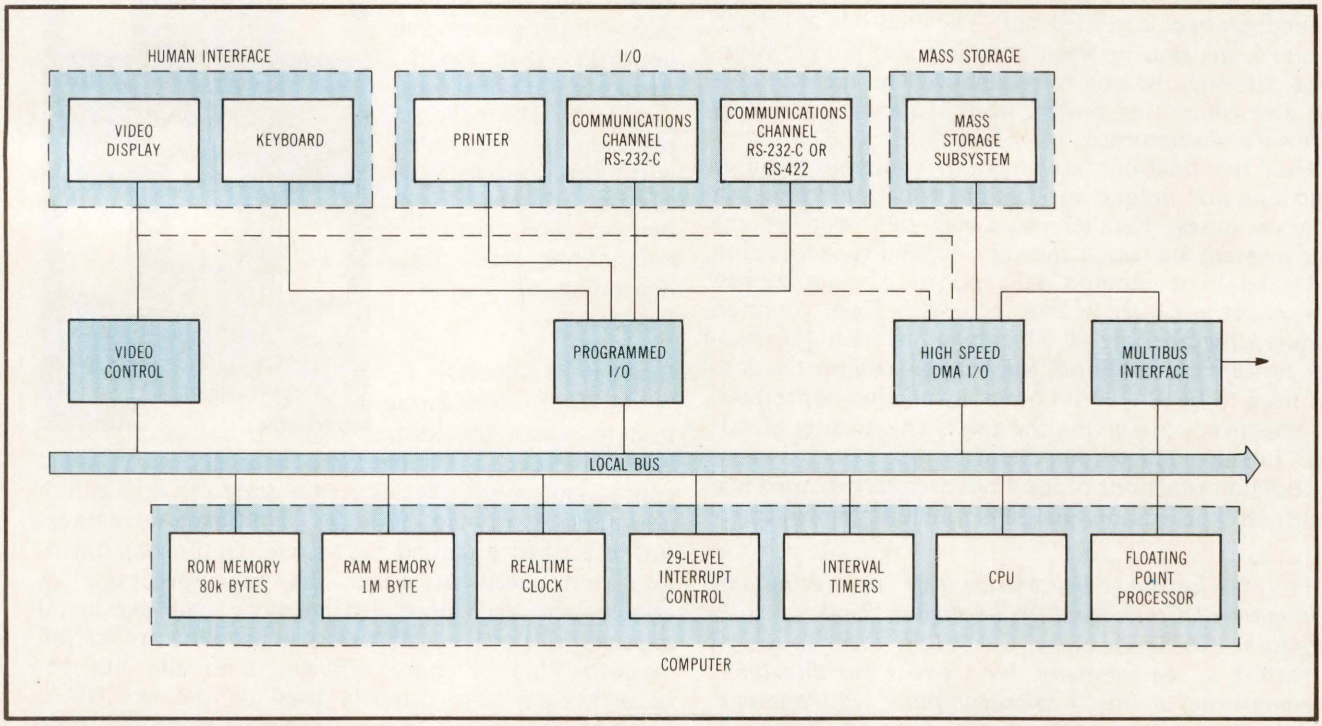


Fig 2 Common facilities. Functions supported on local bus include memory, realtime clock, mass storage, and programmed I/O. MULTIBUS interface permits communication with industry standard equipment for wide range of applications. Common and unique facilities are prevented from interfering with each other.

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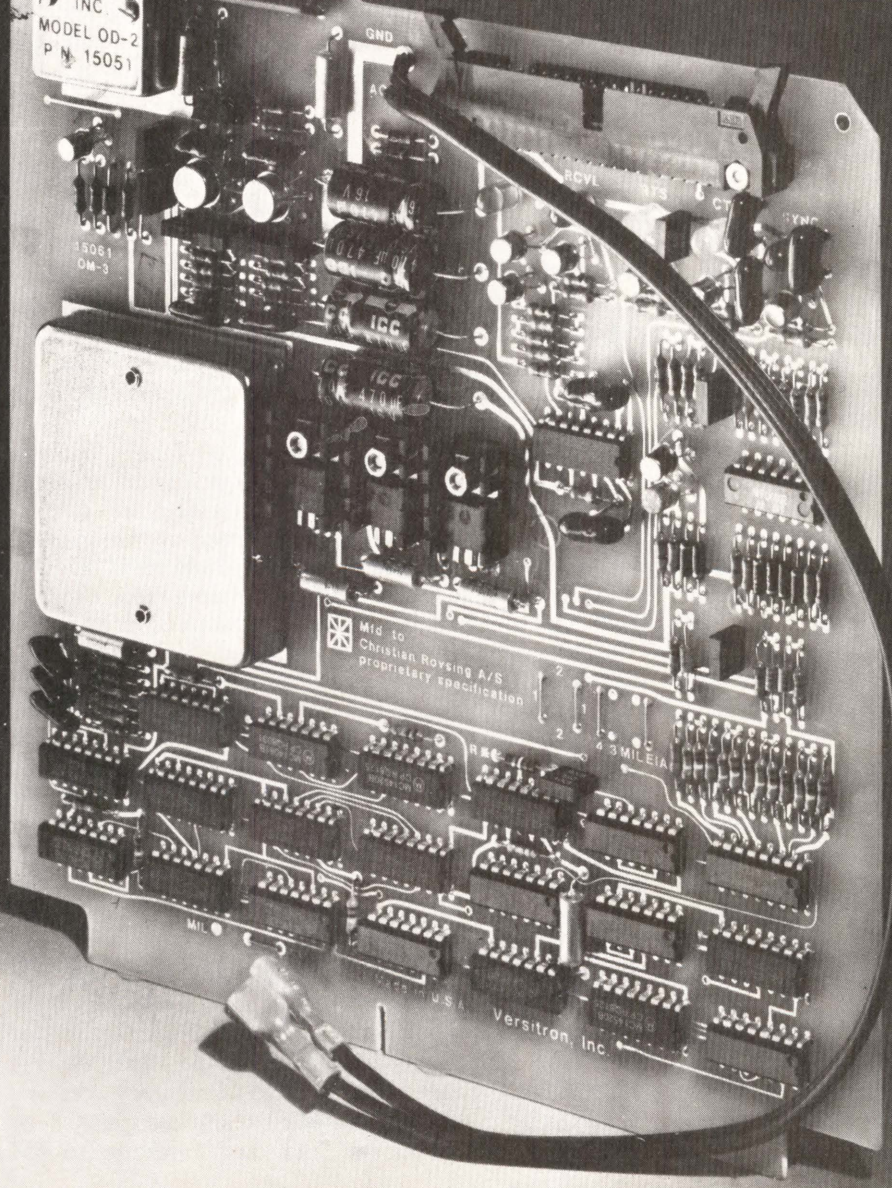

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CIRCLE 70 ON INQUIRY CARD

architecture provides high speed data movement and utilizes memory to fetch instructions during bus cycles that would otherwise go unused. The CPU executes 135 high performance instructions, contains 24 addressing modes, and operates on the contents of 14 internal registers. Since a separate bus supports the special applications related to hardware, the design can easily accommodate higher performance procesors without requiring changes in the applications hardware. Interrupt control, interval timer, and realtime clock support CPU operation.

Numeric processor. Within specific applications requirements, the optional numeric processor can improve system throughput by providing 100 times the numeric processing capabilities of the CPU. The numeric processor operates as a coprocessor with the CPU, monitoring the same stream of instructions. However, each processor is designed to execute the specific instructions that it can most effectively handle. Numeric processing extends the register resources and instruction set of the CPU, which contains a register stack of eight 80-bit, individually addressable registers. The resulting increase conforms to the proposed IEEE floating point standard—the instruction set comprises 63 instructions that operate on 16- and 32-bit integers and 32- and 64-bit real numbers.

Interrupts. Non-maskable and maskable interrupts of the CPU are supported by the local bus, with the interrupt controller providing up to 29 levels of priority interrupts. The system processes three types of interrupts—external device interrupts, internal exception interrupts, and internal software generated interrupts. I/O controllers, interval timer, realtime clock, and MULTIBUS generate maskable external interrupts. In addition, the local bus transfers four non-maskable external interrupts to the CPU—power failure, parity error, write protect, and bus timeout. Divide error, single-step, and overflow-detect generate internal processor exception interrupts. Software calls utilize the facilities through internal software generated interrupts. Application generated interrupts placed on the MULTIBUS protect the system from unwanted tampering with interrupt lines and improve system performance by providing two discrete interrupt systems.

A user accessible 16-bit timer/counter with a clock rate of 19.58 KHz provides the system's interval timer capability. The timer can be loaded or read under program control, while the counter generates a maskable interrupt. A realtime clock generates a maskable interrupt derived from the power line frequency (50 or 60 Hz).

RAM and ROM. The system supports both RAM and ROM [or programmable read only memory (PROM)] in a 1M-byte memory address space; two possible memory configurations are illustrated in Fig 3. The position of RAM and ROM within the address space, and minimum/maximum RAM and ROM sizes are indicated. (ROM occupies lower memory; RAM occupies upper memory.) RAM configurations range from a minimum of 128k bytes on the memory I/O board to a maximum of 992k bytes that is configured with 512k bytes on the memory I/O board and 480k bytes on the memory expansion board. RAM detects single-bit errors with byte parity. The first 32k bytes of RAM can be write protected to ensure operating system integrity.

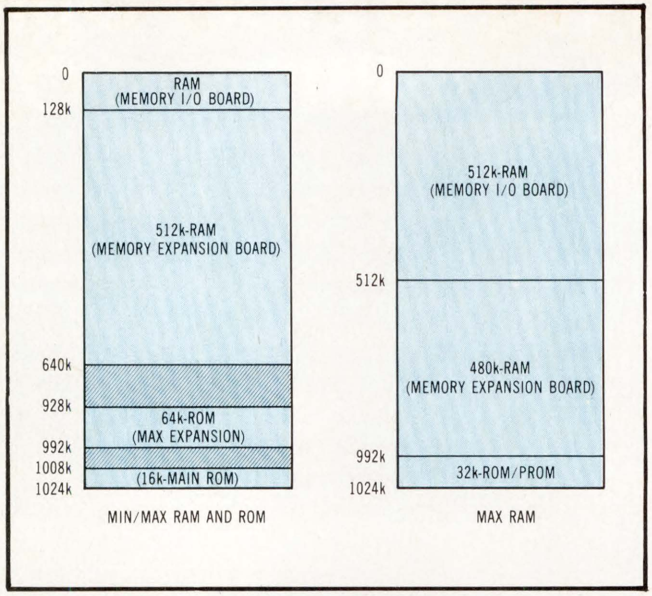


Fig 3 Memory configurations. Several memory configurations can be supported in 1M-byte address space on local bus side of system. Addition of greater memory capability on MULTIBUS side is possible.

Minimum ROM capacity is 4k bytes. Bootstrap software and system diagnostics are contained on the processor board; the processor board can contain a maximum 16k bytes. A maximum system size of 144k bytes is reached with the 128k-byte ROM expansion board.

Interface to the mass storage subsystem is accomplished through a high performance 16-bit channel. The mass storage subsystem, communicating through high speed DMA transfer, supports both floppy disk and 8″ Winchester technology. One or two 500k-byte 8″ floppy disks are included in the minimum configuration, although a system may contain a maximum of three 8″ Winchester disk drives to provide 10M-, 20M-, or 40M-byte capacity. A removable cartridge disk provides backup for the Winchester drives.

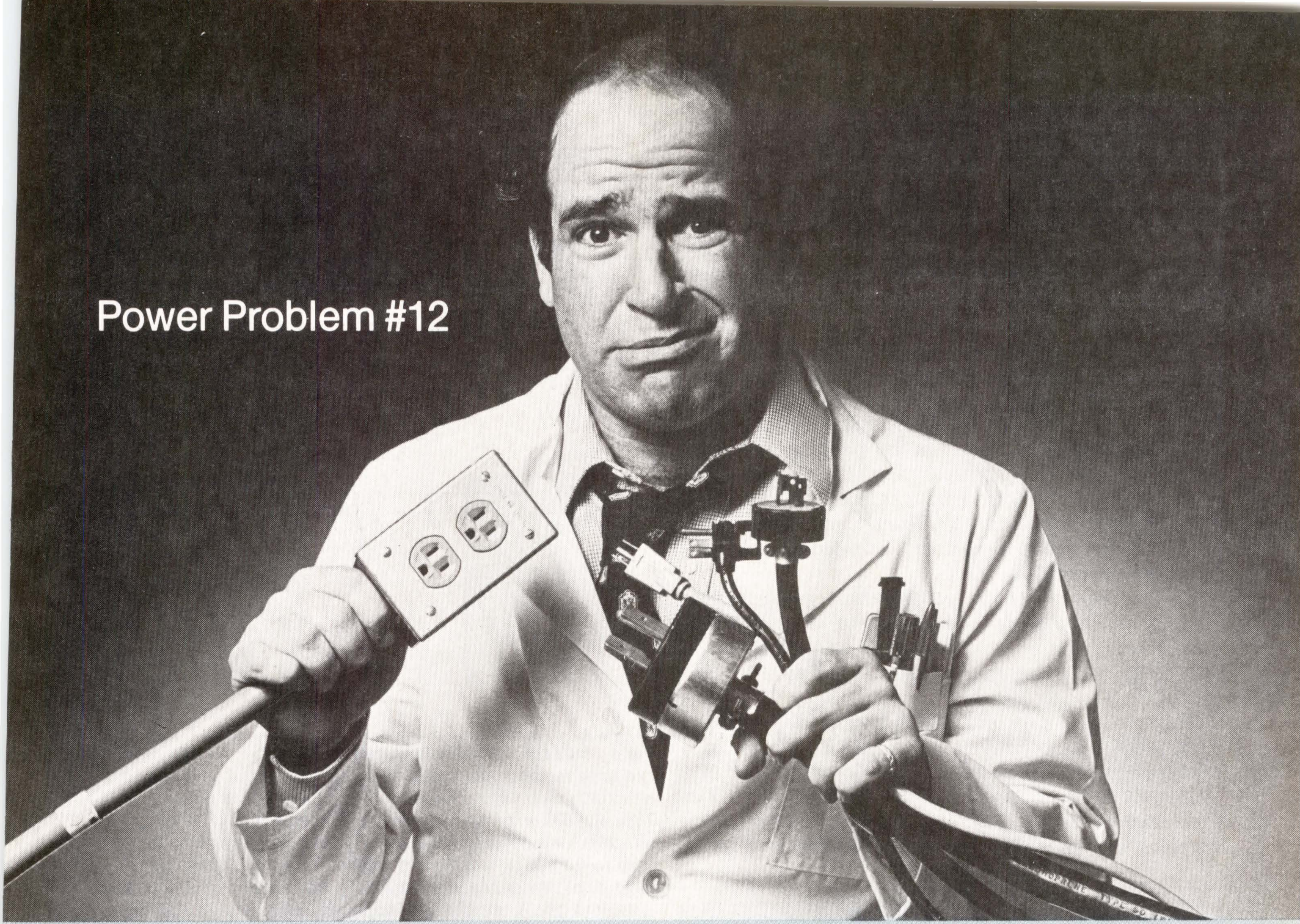
Input/Output. Two programmable serial channels perform system communications. One channel operates with either an RS-232-C or RS-422 interface, and is connected to a DMA channel for high speed operation. The second channel operates in RS-232-C mode only. RS-232-C channels have software selectable baud rates ranging from 110 to 19.2k baud. RS-422 operates via onboard DMA at up to 615k bps over balanced differential lines. Each channel is independently programmed to support both synchronous and asynchronous protocols, as well as bit-oriented protocols.

The system includes an 8-bit parallel printer interface, and outputs ASCII data to printers at speeds greater than 1200 lines/minute under interrupt and programmed I/O control. It is capable of handling either buffered or non-buffered printers.

Application bus: MULTIBUS

A master processor on the MULTIBUS has a 1M-byte address space in addition to the memory space of the local bus. Switch-selectable windows allow sections of MULTIBUS memory to be accessed by the local CPU. Fig 4 illustrates the three choices of local memory access.

The MULTIBUS supports a 64k I/O address space, 8- or 16-bit I/O data transfers, and data rates up to 5M



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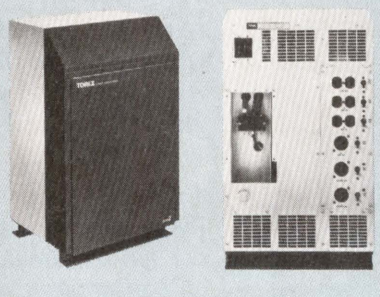

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transfers/s. The local CPU can access MULTIBUS I/O resources, although the MULTIBUS master cannot access local bus I/O resources. Of eight MULTIBUS interrupt lines, only five are shared with the local bus. Interrupts can be expanded to 29 maskable interrupts via interrupt controllers on the MULTIBUS. One channel of local bus DMA supports data transfers between local bus memory and the MULTIBUS, using the previously defined mapping scheme. DMA with local bus I/O devices occurs only to and from local bus memory.

Since the MULTIBUS can accommodate additional processors, as well as memory and I/O expansion, it provides the means to configure a system to fit a variety of specific applications. By including a single-board computer, a CPU board, or a special purpose processor within the MULTIBUS configuration, the system's processing power to perform data manipulation, data storage, or I/O control is significantly improved. Each processor operates on a separate, dedicated bus, containing its own memory and I/O.

Adding memory to the MULTIBUS increases system memory capacity using the local bus-to-MULTIBUS window. Either RAM or ROM/PROM can be placed on the MULTIBUS. MULTIBUS memory also supports MULTIBUS processors and I/O controllers.

The MULTIBUS provides I/O expansion for peripheral controllers, data communications, and interfaces; such expansion is controlled by either the local bus CPU or a MULTIBUS master. Support of a peripheral controller for magnetic tape, hard disk, printers/plotters, and graphics terminals is also provided by the MULTIBUS.

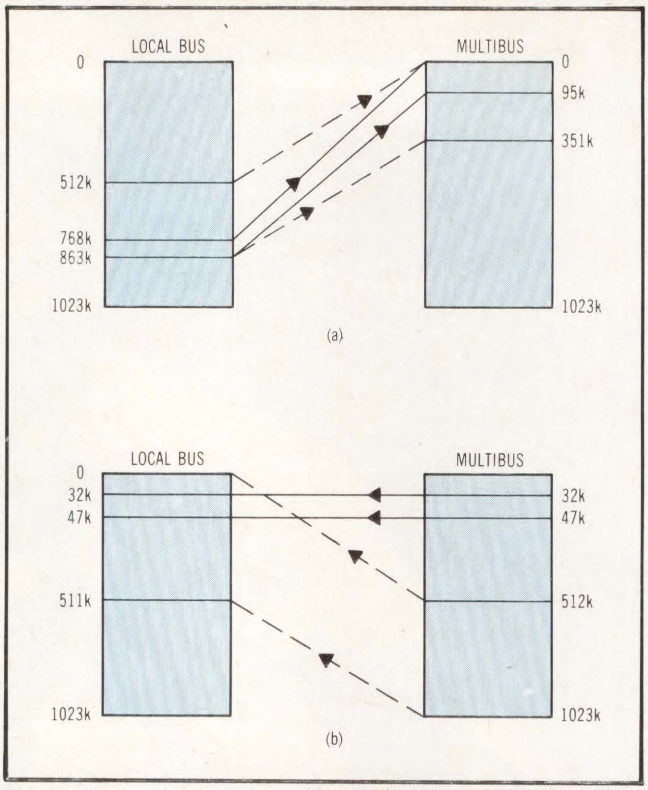

Fig 4 MULTIBUS/local bus shared memory. Switch selection can limit memory sharing accesses to either local memory or MULTIBUS memory exclusively. When local bus is master (a), 768k to 863k window of local bus can map to 0 to 95k MULTIBUS window; or 512k to 863k local bus window can map to 0 to 351k MULTIBUS window. When MULTIBUS is master (b), buses can share a 32k to 47k address window; or a 512k to 1023k MULTIBUS window can map to a 0 to 511k local bus window.

Adding data communications controllers furnishes serial ports to dumb terminals, data communications ports to networks, or communication extensions to other systems. Special system requirements, such as analog or digital I/O, or high speed local networks, are also possible by employing the MULTIBUS.

Minicomputer comparison

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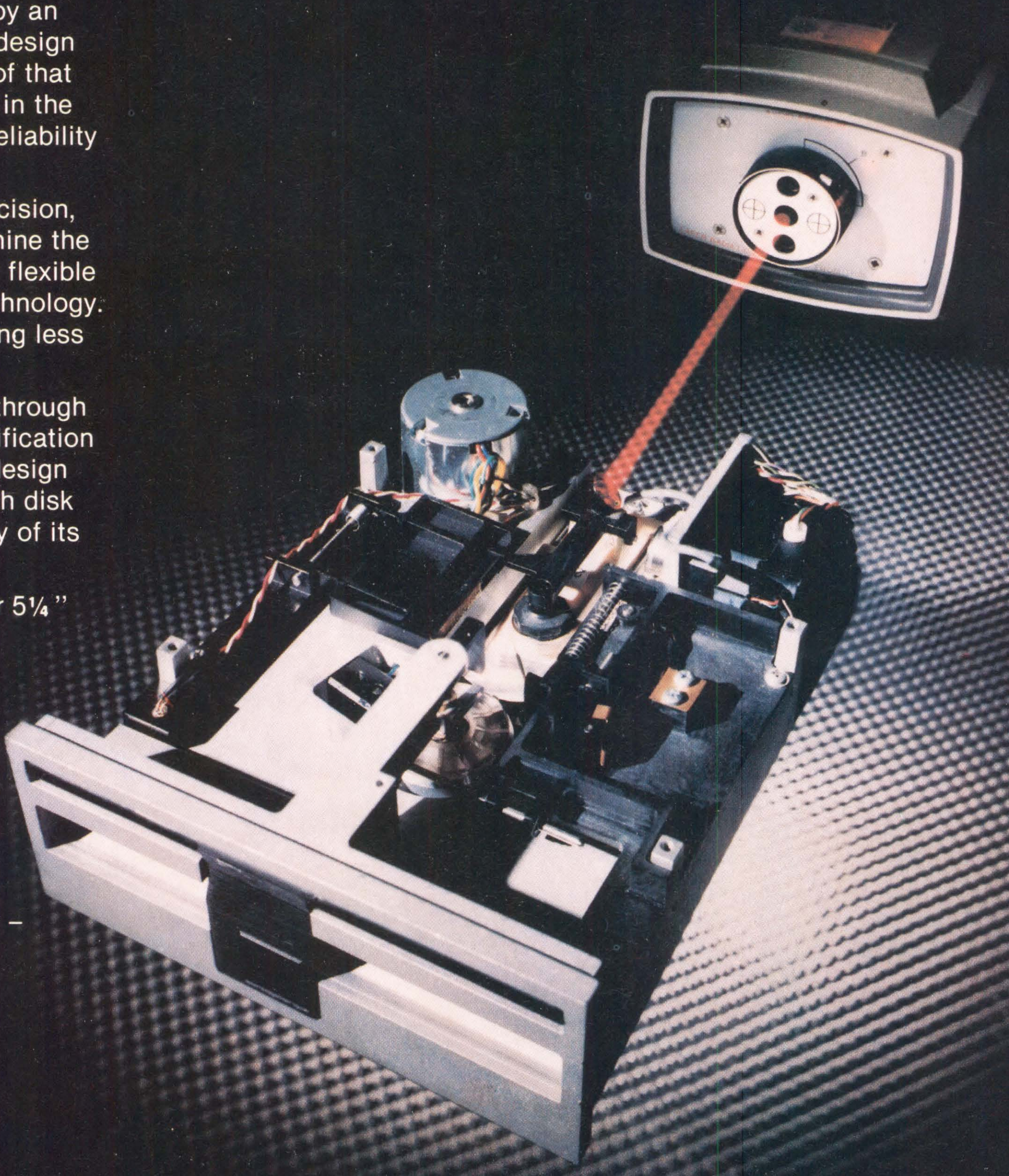

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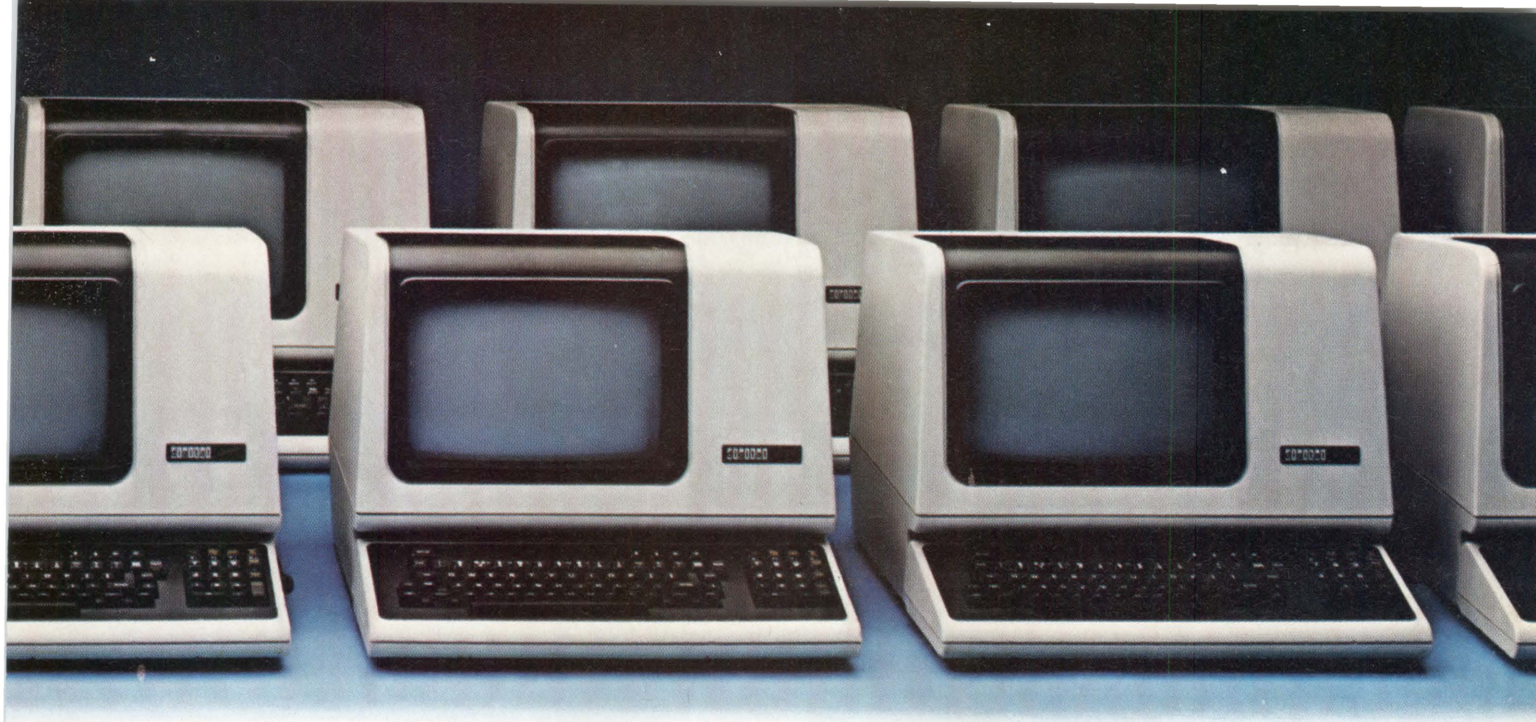

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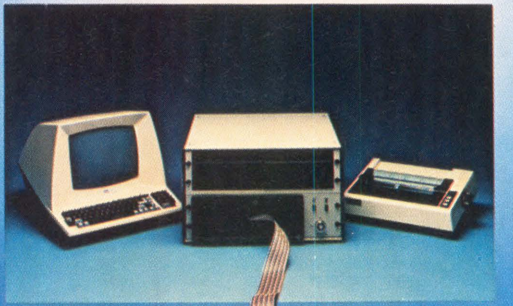

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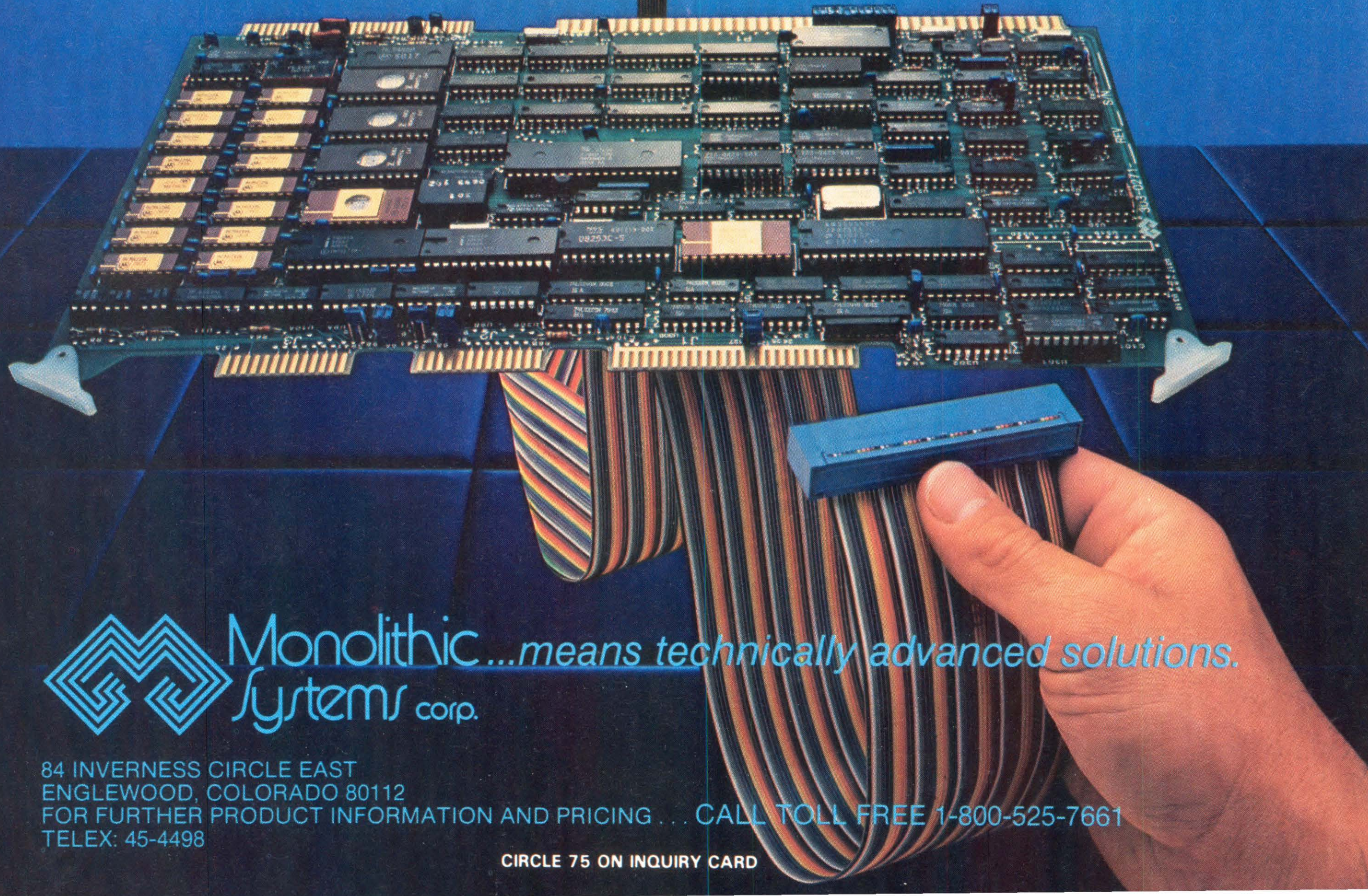

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CIRCLE 75 ON INQUIRY CARD

COPYING ROMS: RIGHT OR WRONG

When copyright laws confront object code, the outcome is unpredictable due to the random judicial process surrounding software

by Richard H. Stern

In the November 1981 issue of Computer Design, *the author discussed the legal protectability of software under the federal copyright laws and concluded that until the law is revised, domestic and foreign software pirates will continue their buccaneering ways. Moreover, object code in particular will not receive effective protection from the courts. Recently, the federal court in San Francisco published a decision protecting the TRS-80's I/O program, when embodied in a ROM as object code. The new decision now makes the score one to one on ROMs.*

The only other decision on the subject held the ROM of the CompuChess game unprotected against competitive duplication. In this article the implications of the TRS-80 decision will be discussed along with the suggestion of passing a software law that directly and expressly covers object code.

According to the San Francisco federal trial court in *Tandy Corp v Personal Micro Computers, Inc*, copying a read only memory is copyright infringement. The court expressly disagreed with the only other court opinion yet issued on this point, the 1979 decision of the Chicago federal trial court in *Data Cash Systems, Inc v JS&A Group, Inc*, in which the court decided that a read only memory is not protected under copyright law. Although software proprietors may be encouraged by the Tandy decision, the case raises perplexing questions as to statutory interpretation and the purpose of the copyright laws.

Richard H. Stern is a partner in the law firm of Baker & Hostetler, 818 Connecticut Ave NW, Washington, DC 20006, where he specializes in intellectual property, antitrust law, and computer matters. He was formerly chief of the Intellectual Property Section and Patent Section of the Antitrust Division, U.S. Dept of Justice. Mr Stern has a BSEE and an AB from Columbia University, and an LLB from the Yale Law School.

Background

Both plaintiff Tandy and the defendants manufacture home microcomputers. Tandy's TRS-80 computer includes an input/output (I/O) program; the defendants allegedly misappropriated this program which interprets BASIC source code into machine-intelligible object code. This interpretation process is essential to the use of the computer, the court noted, because while human beings cannot understand object code, machines cannot be directly operated by ("understand") human-intelligible high level languages such as source code.

Apparently, Tandy had registered the program for copyright as a source program, which is treated as a literary work under the copyright laws. Tandy discovered that defendants were using the same program in their microcomputer, and subsequently sued. When written out in source code or another human-intelligible language, Tandy's I/O program is clearly copyrightable. However, the I/O program, like other programs, must be transformed into object code before the computer can use it. By preparing a read only memory (ROM) whose physical pattern corresponded to the object code of the I/O program, Tandy transformed its I/O program into object code.

When the defendants reproduced Tandy's ROM, the question arose as to whether Tandy's or the defendants' ROM chip was a "copy" of the original copyrighted I/O program in terms of the copyright statute. The defendants moved for summary judgment in their favor, on the ground that although their ROM chip duplicated Tandy's, it was not a copy of Tandy's copyrighted I/O program. The copyright law, of course, protects and prohibits only "copies."

A new opinion

Refusing to dismiss Tandy's complaint, the court rejected the summary judgment motion. The court said that it felt convinced that a silicon chip is a "tangible medium of expression," within the meaning of the copyright statute, "such as to make a program fixed in that form subject to the copyright laws." Also, the court noted that according to the statute, works can be "fixed" in any "tangible medium of expression, now known or later developed, from which they can be perceived, reproduced, or otherwise communicated, either directly or with the aid of a machine." The court concluded from these two propositions that, "The imprinting of a computer program on a silicon chip, which then allows the computer to read the program and act upon its instructions, falls easily within this definition."

...the court badly confuses itself with its metaphors.

The court recognized that it differed from the *Data Cash* trial court, which had held that a ROM in which object code is stored is not a "copy" of the source program to which the object code corresponds, and had ruled that a "copy" of a source program is another source program rather then a mechanical device. Moreover, the San Francisco court disagreed with the reasoning in *Data Cash*.

In addition, the court noted that Tandy may be able to show that the defendants copied its I/O ROM by making a human-intelligible printout of the program (clearly a copy under copyright law) and then using it to produce the ROM. "If this method of unauthorized duplication in fact is proved," the court observed, "there can be no doubt that the unauthorized duplication of a visually displayed copy of the program would fall within the reach of the federal copyright laws."

Is a chip a "copy"?

The court's last point is well taken, but its earlier conclusion about ROMs does not follow from the two propositions on which the court relied to reach it. Imprinting a program on a chip that corresponds to the 1s and 0s of the pertinent object code does *not* "fall easily within" the statutory definition of a copy of the copyrighted source program. To be sure, the court could be correct in saying that the chip may *in some sense* be "read" and "understood" by the computer, but none of that means that the I/O program "can be perceived, reproduced, or otherwise communicated" from the chip as the statute requires. That is debatable, and the conclusion one draws depends on one's view to how many people a message must be intelligible before copyright applies. It may also depend on the intended purpose of the recording medium.

Gaps in the court's logic are filled with two unstated, and probably erroneous, assumptions. One is that the object code version of the I/O source program is a copy of the latter. The second is that the chip is a copy of the program in object code or of the program in source code. More important, the court badly confuses itself with its metaphors. When speaking of a computer "reading" or "understanding" object code, and "act[ing] upon its instructions," the court mistakes metaphor for reality. Computers do not read books or understand them in the same sense as a person does. Yet, the court's reasoning assumes this to be true and that "perception" by a machine or "communication" to a machine is covered by the statute. This is highly questionable, and possibly wrong.

Object code—written form

Object code in its written form is a string of 1s and 0s wholly unintelligible to even most skilled readers, and therefore probably not a copy of source code or of a program. This pattern of 1s and 0s is produced by a series of transformations from the other languages in which a program is written, and there is no fixed relationship between the source program and the object code. Some statements in the source program may not have counterparts in the object code, while some portions of the object code version may not have counterparts in the source program.

...stopping such action ... calls for a different legal mechanism...

Moreover, this source code/object code transformation is not readily reversible. Object code can probably be taken apart and transformed (inverse compiled or reverse compiled) into high level source code by a computer, or more readily be disassembled into comprehensible assembly code. But this can occur only when important factors are known about the prior source code/object code transformation, such as machine identity and the editor/assembler used to effect it. Even then, the product of the reverse transformation will probably be far from identical to the original source program.

Object code—chip form

Object code is even less a source program copy in physical form, and probably not even a copy of the object code in written form. The physical form of object code is a pattern of magnetized and unmagnetized domains on a magnetic tape or disk; a pattern of punched and unpunched holes on a paper tape or a set of cards; or, as it is here, a pattern of closed and open gates on a chip. Though the pattern corresponds to the written form of object code on a one to one basis, the physical object is not a copy of the pattern of 1s and 0s. Under U.S. law determined by previous court decisions, a copy of a blueprint is another blueprint, not a building or machine made from the blueprint. (The *Data Cash* court stressed this point.) Therefore, the chip is probably not a copy of the written form of the object code version of the I/O program.

For even more pervasive reasons, the chip is probably not a copy of the I/O source program. The copyright statute defines a copy as a material object from which the original work (ie, the I/O source program) "can be perceived...or otherwise communicated."[1] This raises the question of who or what is perceiving and communicating, a human or a machine.

Deceptive metaphor of computer perception

Just as a normal person cannot "perceive" the source program from the object code, whether in written or chip form, the chip cannot "communicate" the source program to a person. By speaking metaphorically of the computer as reading the chip, in some way understanding the chip's message or instructions, and then acting upon this, the court in the present case glossed over this problem. All of this is only a metaphor, as a computer is not a thinking perceiver. In the same sense that a computer cannot be murdered or have property bequeathed to it, neither can it be communicated with. Until now, copyright has been understood to refer to the subject matter of perception by a human being and communication with a human being. According to this interpretation, a copyrightable work conveys information or feeling; it must have some communicable intellectual or emotional content.

The proper interpretation of "perceive" in the statute is thus "comprehend intelligently," rather than merely mechanically record or register without intellectual appreciation. Without an explicit legislative command that "perceive" henceforth includes perception by a machine, whatever that would mean, there is no basis for concluding that otherwise imperceivable, incomprehensible object code is a copy of anything under the copyright law.

In other words, whether human intelligibility and sensibility are sine qua non for copyright is the question. The answer to that question is probably yes and the present court's judgment that a "copied" ROM is within the scope of the federal copyright infringement statute must therefore probably be rejected.

Need for specific law

This does not mean that duplicating someone else's ROM is laudable. On the contrary, it means that stopping such action is essential. However, that calls for a different legal mechanism than the one Tandy sought to use. Appropriate software legislation, designed to meet the needs of the subject matter (ie, software), is needed. Because there are varied and conflicting interests at stake, devising such legislation is no simple matter. Different types of copying may call for different remedies. Surely, more sound and productive results will be realized by undertaking to devise new legislation to cover software than by distorting existing copyright law.

Applying copyright law to software is likely to lead to unpredictable and unacceptable results. Copyright law provides remedies largely geared to preventing people from copying books. It has been extended, with questionable results, to include such things as lamp bases, fabric designs, and earrings. It has not, however, been extended to purely industrial products. Its application in this context is likely to be disastrous. Consider, for example, whether an innocent user of the defendants' microcomputer would be an infringer of Tandy's copyright. It is not clear whether Tandy should be entitled to make the user stop using the defendants' ROM and thus stop using the microcomputer, or whether Tandy could prevent him from selling or trading in the computer. What effect such action would have on the future of the home computer market is uncertain. The same questions can be applied to a commercial user of a ROM or disk with purloined object code.

...the proper way to deal with software is with a law directed to software, not...books, plays, pictures, and musical scores.

This issue remains unclear under ordinary copyright law principles. Literally, the copyright law permits the impounding and destruction of any and all infringing copies of a copyrighted work.[2] A better view is probably that a purchaser of a pirated copy of a copyrighted work is not an infringer, and that it would make no sense to impound and destroy the purchaser's copy. However, one recent court opinion conflicts with this view, stating that even an unwitting purchaser who buys an unauthorized copy in the marketplace can be held liable for infringement.[3] Because the copyright statute makes no distinction, and there are no decisions directly in point, the issue remains cloudy.

Another provision of the copyright law provides for seizure, forfeiture, and destruction of infringing products imported into the United States.[4] This could be a manufactured ROM or burned PROM that embodies the I/O program for the TRS-80. It is clear that this seizure provision applies even to innocent U.S. purchasers of a copied work. A legal rule that subjects software users to such risks would make no sense, but that may be the law if copyright is applicable to object code as the San Francisco court has held.

A proper software law

Examples could be multiplied, but the point is that the proper way to deal with software is with a law directed to software, not with one directed to books, plays, pictures, and musical scores. A proper software law should deal specifically with object code in a sensible manner, taking into account the interests of software proprietors, hardware manufacturers, programmers, data processors, machine tool users, and consumers of products that depend on software for their production. Unfortunately, present copyright law does not begin to consider these interests.

A proper software law would clearly define what is infringement of software, specifying different remedies for different types of infringement. It may well be that a proper software law would go beyond unloaded object code to protect algorithms, program concepts, and object code independently compiled from a copyrighted source program. In that case, remedies far less drastic than those applied against a ROM unloader should be used.

These issues call for public discussion, interchange of views in the software industry, and a legislative solution explicitly and clearly stating the consensus reached. The result should not depend on how different judges differently interpret the provisions of a law that was written without consideration of any of these problems.

To remedy the present legal confusion, the software industry should confer to unearth problems, reveal conflicting interests, and point toward acceptable solutions. The natural outcome of this would either be a clear statement of opposing views, or a consensus of opinion on what the industry should ask of Congress. The time has come for the democratic, legislative process to supersede the present random judicial method of resolving disputes over who owns software and to what extent.

References

1. 17 U.S. Code § 101
2. 12 U.S. Code § 101
3. Compare Jewelers' Circular Pub Co v Keystone Pub Co, 274 F. 932, 936 (S.D.N.Y. 1921), *aff'd on other grounds*, 281 F. 83 (2d Cir 1922); and Foreign & Domestic Music Corp v Licht, 196 F.2d 627 (2d Cir 1952), with American International Pictures, Inc v Foreman, 576 F.2d 661 (5th Cir 1978)
4. 17 U.S. Code § 603 (c)

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PRACTICAL BACKUP THROUGH ROTATING HEAD TECHNOLOGY

A disk backup offers adequate throughput and rapid random access without resorting to data streaming

by Bruce Manildi

A new approach is being taken to produce a low cost, high capacity, high speed disk backup and file unit. Using a removable half-inch magnetic tape cartridge, the drive stores 80M bytes/cartridge (formatted) with a data rate of 500k to 600k bytes per second. Data are formatted in 615 blocks of 131k bytes/block. During data transfer, the tape is motionless and the drive operates as a random access device within each block, using two active heads that describe 16 cylinders. A stepping motor, in conjunction with a peripheral drive system, provides block to block access.

Storage hierarchy

Since the cost/performance ratio is always a consideration, one must seek a pragmatic solution to storage needs. A hierarchy of storage devices can offer extremely fast (nanosecond) access to small amounts of data and increasingly longer access times to larger amounts of data.

Typically, there are three levels in the hierarchy: *semiconductor memory* provides rapid access but is limited in capacity due to cost; *disk drives* provide a range of access times and capacities through either fixed head/track (rapid access, higher cost) or moving head devices (slower access to data but lower storage costs); and *tape drives* meet large capacity, lower speed requirements ranging from high performance vacuum column drives (typically using 0.5" tape), to low speed, low capacity 0.25" cartridge drives.

An efficient computer system uses all three levels of the storage hierarchy as needed. Semiconductor memory provides fast computation and throughput of a relatively small amount of data at any time. A disk drive updates the data in semiconductor memory from time to time as the central processing unit (CPU) performs different functions. In addition, a tape drive fulfills backup and archival (offline) storage needs.

General description

Combining desirable features of both disk and tape drives, the Pragma 2000 direct access cartridge drive discussed here provides both rapid random access within a data block and a high data transfer rate. The drive uses 0.5" tape in a low cost, removable cartridge that can be stored offline for archival purposes. Thus, a block can be directly selected or serially sequenced like a tape drive.

The interface, and consequently the controller, are similar to those of a disk drive. In fact, one of the interfaces is hardware compatible with Shugart Associates' SA 1000 interface. Though no larger than a floppy disk drive, the unit stores 80M bytes on a single 5" x 5" x 1" (13- x 13- x 2.5-cm) removable cartridge at an instantaneous rate of 512k bytes per second.

Data are stored in blocks that are equivalent in length to half the circumference of the rotating read/write scanner. The tape remains stationary during the read/write operation while the rotating magnetic transducer scans the tape lengthwise. The rotating scanner is separated from the tape by an air bearing which protects the tape from wear while accurately centering it. This eliminates the edge guides found in most tape drives and the edge damage generated by them. In addition, interchangeability is greatly enhanced since the center of the tape is always in the center of the path, regardless of tape width or slitting problems.

Bruce Manildi is vice president of operations at Pragma Data Systems, Inc, 610 Palomar Ave, Sunnyvale, CA 94086, in addition to being one of the company's founders. Previous experience includes design of communication terminals and video recording/disk storage drives. He has also designed tape recorders for missile and space applications. Mr Manildi holds a BSEE from Stanford University and an MSEE from San Jose State University.

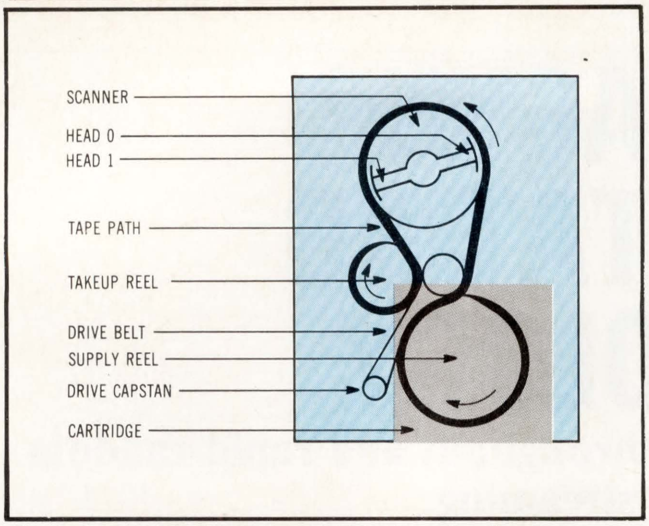

Fig 1 Tape path through cartridge. Rotating heads are separated from tape by air bearing.

With the combination of stationary tape, air bearing, and a high inertia, servo controlled scanner, data jitter caused by instantaneous speed variation of the tape is eliminated. Stability of the data read by the direct access cartridge drive is as good as that provided by most disk drives. This fact, along with the use of the same data rate as the SA 1000 type disk drives, allows use of the same data separator for both the unit and the disk drive it backs up.

A high data transfer rate is obtained without resorting to streaming. The same data are presented at the interface every revolution of the heads (18.75 ms), providing a command is not received to access the heads or tape.

Theory of operation

A rotating scanner carries a pair of magnetic transducers and provides tape guidance for the cartridge drive. The magnetic tape wraps around this scanner and is separated from it by an air bearing. (See Fig 1.) The path of the rotating heads describes a longitudinal track approximately 5.5" (14 cm) in length, parallel to the tape length. In the "home" position, head 0 writes a track next to the edge of the tape nearest the drive base plate and head 1 writes a track just above the center of the tape. To access track 2 and track 3, the heads are simultaneously positioned at the next cylinder by a linear actuator. This process repeats for each of the 32 tracks (16 cylinders) in a block. (See Fig 2.)

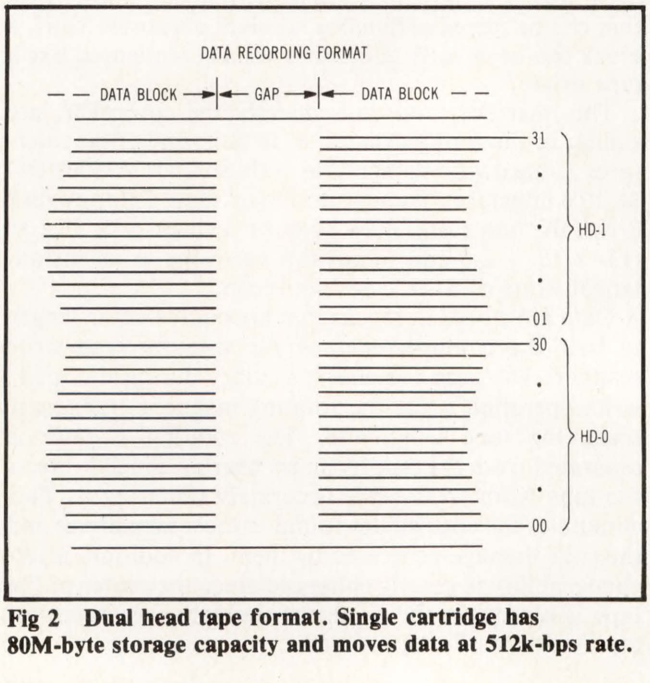

Fig 2 Dual head tape format. Single cartridge has 80M-byte storage capacity and moves data at 512k-bps rate.

To move to another block, a second stepping motor is activated. The tape moves past the scanner to the required block by driving a belt in contact with the periphery of the tape packs. Once the desired block is in approximate position, a data seeking servo precisely aligns the beginning of the block with respect to the scanner. Overlapped seeks are allowed to position head and tape simultaneously.

Data to be written on the tape are presented at the interface in the form of a pulse for every flux transition. The signal is gated internally before going through the write driver and a 2-channel (one for each head) rotary transformer. In the read mode, the signal is sent back from the head through the rotary transformer and signal conditioning circuit. Modified frequency modulation encoding is recommended, but write precompensation is not required. However, if the same data path is used for both a disk drive and the backup, it is simpler to use the precompensation. While other encoding schemes can be used, they may be less compatible and result in slightly lower capacity.

Cartridge

The cartridge contains 333' (101 m) of 0.5" magnetic tape, with a protective leader that doubles as an autoload mechanism. Once the cartridge is inserted and a load command is given, the belt rotates the reel, stripping the leader from the flanges. A guide channel forces the leader through the tape path, where the flanges of the takeup reel capture it. Since the leader is wider than the tape, the tape itself never touches any surface in the drive or cartridge.

Summary

Pertinent specifications of the direct access cartridge drive described in this article include an 80M-byte capacity, instantaneous data rate of 4.34M bps, average intra-block data rate of 2.9M bps, and an average inter-block data rate of 1.5M bps. Track to track access time is less than 9.4 ms, while adjacent block to block access time is less than 280 ms. Dimensions of the drive are 14" x 8.55" x 4.63" (36 x 21.72 x 11.76 cm) with a 4.87" x 4.87" x 1.1" (12.38- x 12.38- x 2.79-cm) cartridge. Power supply requirements are 24, 5, −5 V (or −7 to −15 V) at 80 W peak. Error rates are 1 to 10^9 hard, and 1 to 10^8 soft. This design, using rotary head technology, provides high, stable data rates without streaming, small package size, and large capacity at a low cost.

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High 722 *Average 723* *Low 724*

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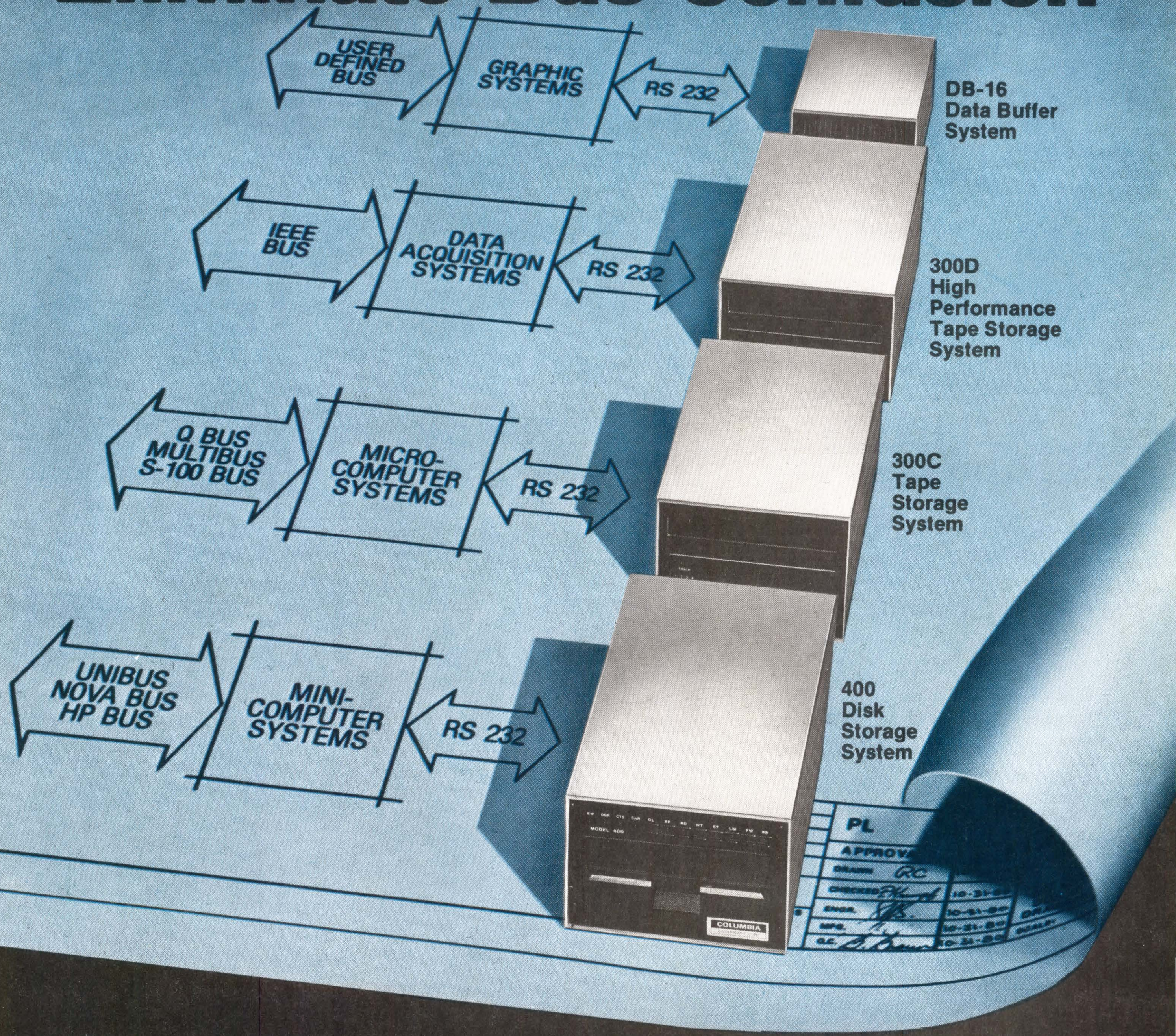

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DIGITAL TOOLS FOR ANALOG DESIGNERS

This computer language for the analog designer speeds development in signal processor applications

by Sandy Wharton

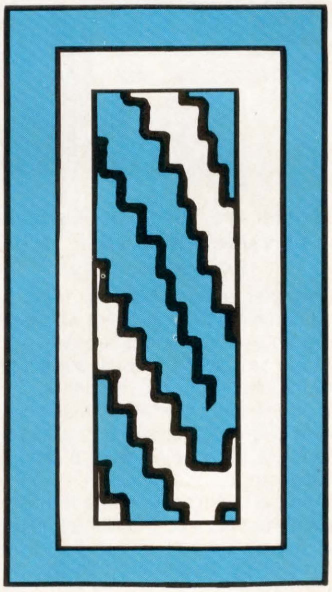
Signal processing systems are sampled systems that process analog signals using digital techniques. Because digital design techniques are new to most analog designers, tools are required to intelligently blend digital computers and analog design. Therefore, creators of the signal processor chip worked closely with software writers to design a signal processor applications software compiler. This compiler has the features and terminology needed by the analog designer and is also easy to use.

Advantages of digital signal processor chips

Even with the most careful calculations, the characteristics of the final analog circuit vary because of component tolerance deviation. Extensive redesign is required whenever changes are desired. However, by bringing the technology of the digital world to analog circuits, completed designs have now been made repeatable. Because of the crystal driven, fully programmable signal processor chip, all that is required when changes are needed is to reprogram the chip.

Using a sample and hold circuit and performing bit wise analog to digital (A-D) conversion, these chips convert analog signals to digital data. All internal computations and transfer functions are then carried out in a digital processor. Outputs are sent through a digital to analog (D-A) converter to produce analog outputs. (See Fig 1.) Applications for digital signal processors include modems, dual tone multiple frequency receivers, and spectrum analyzers.

Sandy Wharton is in charge of curriculum development for high level languages in the Customer Training Dept at Intel Corp, 1350 Bordeaux Dr, Sunnyvale, CA 94086. She has a BA in mathematics from Ripon College, Ripon, Wis, and an MS in computer science from the University of Santa Clara, Calif.



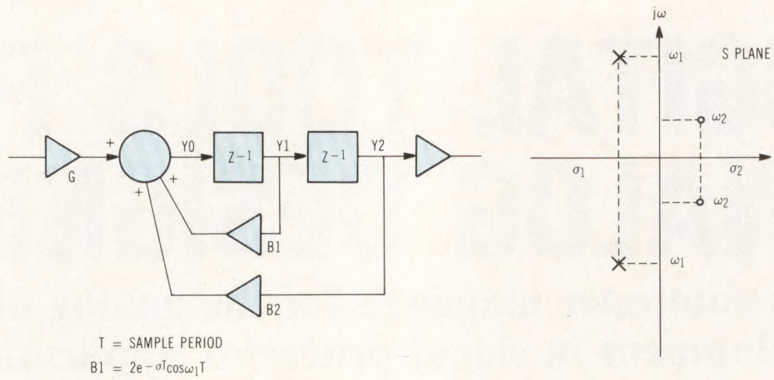
Software design tools

In the past, analog designers have used digital computers for circuit modeling and calculation. Since the signal processing chips require programming, tools are required to assist analog engineers with their design. Intel provides a software simulator to test programs and an assembler to convert a finished program to machine code. Of particular importance is a new signal processor filter design tool, the Signal Processor Applications Software package SPAS20, tailored to the needs of the analog designer. All the software tools run on an Intellec[R] microcomputer development system.

Applications compiler

The SPAS applications compiler allows the analog designer to work in either the S-plane or the Z-plane. An interactive tool with outstanding graphic capability, SPAS makes it easy to specify, alter, and review design parameters. The designer can enter filter parameters (eg, sample rate, poles, zeros) and immediately see the Bode plot of the resulting filter characteristics. To get a closer look, the plot can be blown up or expanded to

Explanation of some terminology



T = SAMPLE PERIOD

$$B1 = 2e^{-\sigma_1 T}\cos\omega_1 T$$

$$B2 = -e^{-2\sigma_1 T}$$

$$GAIN = \frac{G}{(1 + B2)\sqrt{1 + \left(\frac{B1^2}{4\,(B2)}\right)}}$$

The block diagram of this filter has two delay (memory) locations (Z^{-1}) and two feedback loops, (poles) with multipliers B1 and B2. Equations for B1 and B2 fit into the general equation for a 2-pole low pass filter.

Y0 = (G * X) + (B1 * Y1) + (B2 * Y2)

where

X — input sample
G — weighting constant of the input
Y1, Y2 — currently saved values
B1, B2 — constant weighting factors

B1 = 1.9573546 and B2 = −0.95824511 in the 50-Hz filter example. Pole pairs are reflected about the real axis in the S-plane. Points in the S-plane are ordered pairs consisting of a real coordinate and an imaginary coordinate.

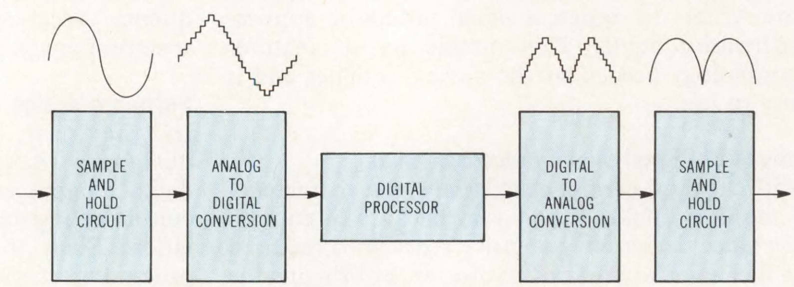


Fig 1 Converting analog signals to digital data. Processor chips convert input analog signals to digital data through A-D conversion, while analog outputs are sent through D-A converter.

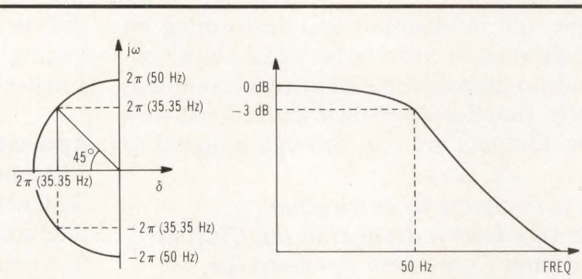


Fig 2 Butterworth filter complex pole relationships and associated attenuation curve. Circle represents filter cutoff frequency (50 Hz) with 45° pole locations coinciding with −3 db points.

display more clearly the sections of interest. A table of the exact values can also be listed.

When the designer is satisfied with the frequency response, time response, etc, of the filter, the compiler will produce commented code on command. This saves the user from writing the detailed steps in the assembly language required to implement functions. A novel feature of this compiler is that the programmer can direct it to optimize the code produced. (See the Panel, "Optimizing produced code.") Specifications for optimization include number of instructions, minimum gain error, and pole error. Code can then be stored on diskette for later use. Because of the minimal effort required to reinstate the previous status, work sessions can be as long or as short as desired.

Sample session

There are four steps to the process for developing a 2920 program that implements a 2-pole Butterworth low pass filter with cutoff frequency at 50 Hz. In the first step, the complex pole pair (2 poles) is set up at 50 Hz in the S-plane by invoking a built-in Butterworth function

```
:BUTTER (2,50)
```

The poles in a Butterworth filter lie on a 45° angle from the origin, on a circle whose radius is the cutoff frequency. (See Fig 2.) The SPAS software places the poles accordingly and reports the position of pole 1:

```
POLE 1 = -35.349369,36.275165
```

The built-in function, BUTTER, created two poles which define a filter. In the next step, some of the filter's characteristics can be looked at graphically:

```
GRAPH GAIN
```

The frequency (in Hertz) is plotted on a logarithmic scale. (See Fig 3.)

SPAS can then be directed to produce code in the third step. A variety of boundary conditions can be placed on the compiler's efforts which include directions to minimize the pole or zero position error, minimize the maximum total absolute error, or minimize the mean square error. In addition, the compiler can be given an absolute maximum number of instructions to use. If no limit is set, the compiler will test sequences of instructions up to 20 lines long. It codes the filter specified, with the stipulation that the number of instructions cannot exceed 13. When the filter has been coded it can then be stored on diskette.

```
CODE POLE 1 INST<14
```

To find the best code with the smallest error in the least possible number of instructions, the compiler tries many combinations. It begins by writing a minimal 4-instruction program, but this results in significant pole error. The best code was 13 instructions as shown in Fig 4. In each dimension, the pole error was less than 1 Hz.

Finally, in the fourth step the user adds any necessary instructions to the assembly language to complete the design, and stores this information on disk. The assembly language is translated to machine code by the assembler. This assembled code can then be tested by

Optimizing produced code

Written in FORTRAN, the compiler uses a heuristic approach to produce assembly code. It begins by trying pole or zero locations, using the fewest instructions it can. It then moves the pole or zero to a new location in the S-plane and tries to write a program to implement the pole or zero at that new location. The error for each try is tracked, and when a try with a smaller error is found, this is reported to the user as "best yet" while the code is being stored for that try. Thus the compiler tries dozens of combinations and locations to produce the best code.

The compiler uses a tree search method, exhausting all the legal combinations with 4 instructions before it allows itself to add another instruction and start again. In addition, the compiler optimizes in order to minimize the possibility of overflow and underflow error.

Code with minimum pole or zero position error in the smallest number of instructions is the result. The compiler reports the number of instructions, the position error, and the sequence of assembly language instructions with comments that tell the user how the program works. As the compiler stores the latest program in memory, information can be stored on disk at any point in the design session.

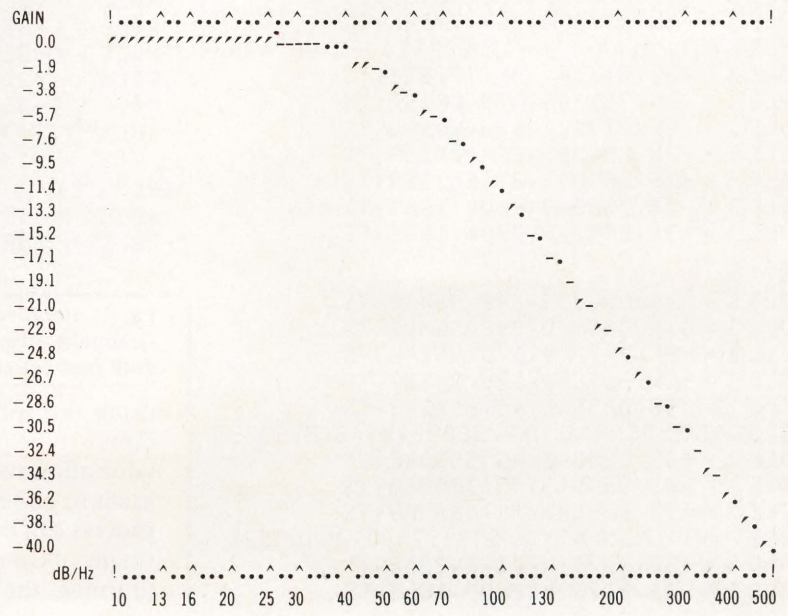


Fig 3 Logarithmic gain vs frequency curve for filter being designed

```
INST=4
 POLE 1 = 0.00000000,2604.1665,TS
  BEST YET: PERROR = -35.349998,-2568.8164
INST=5
 POLE 1 = -26.317544,2604.1665,TS
  BEST YET: PERROR = -9.0324535,-2568.8164
 POLE 1 = -26.317544,2604.1665,TS
 POLE 1 = -1147.52624,73.220191,TS
  BEST YET: PERROR = 1112.17626,-37.870193
INST=6
 POLE 1 = 0.00000000,36.634704,TS
  BEST YET: PERROR = -35.349998,-1.28470610
 POLE 1 = 0.00000000,293.45465,TS
 POLE 1 = 0.00000000,293.45465,TS
 POLE 1 = 0.40470251,36.630233,TS
 POLE 1 = 0.40470251,36.630233,TS
 POLE 1 = -33.029541,2604.1665,TS
 POLE 1 = -33.029541,2604.1665,TS
INST=7
 POLE 1 = 0.00000000,359.64285,TS
 POLE 1 = 0.00000000,328.19976,TS
 POLE 1 = -35.138202,2604.1665,TS
 POLE 1 = -34.716053,2604.1665,TS
INST=8
 POLE 1 = 0.00000000,344.27529,TS
 POLE 1 = 0.00000000,343.03845,TS
 POLE 1 = -26.317544,25.898057,TS
  BEST YET: PERROR = -9.0324535,9.4519405
 POLE 1 = -26.317544,25.898057,TS
 POLE 1 = -26.317544,207.35467,TS
 POLE 1 = -26.317544,145.385787,TS
 POLE 1 = -25.899845,26.312263,TS
 POLE 1 = -25.899845,26.312263,TS
 POLE 1 = -35.329586,2604.1665,TS
 POLE 1 = -35.138202,2604.1665,TS
INST=9
 POLE 1 = 0.00000000,342.92297,TS
 POLE 1 = 0.00000000,342.88452,TS
 POLE 1 = -26.317544,36.777538,TS
  BEST YET: PERROR = -9.0324535,-1.42753984
 POLE 1 = -26.317544,36.777538,TS
 POLE 1 = -26.317544,179.06152,TS
 POLE 1 = -26.317544,176.64541,TS
 POLE 1 = -25.691085,37.207153,TS
 POLE 1 = -25.691085,37.207153,TS
 POLE 1 = -35.316867,2604.1665,TS
 POLE 1 = -35.349369,2604.1665,TS
INST=10
 POLE 1 = 0.00000000,342.94415,TS
 POLE 1 = 0.00000000,342.96966,TS
 POLE 1 = -26.317544,176.41946,TS
 POLE 1 = -26.317544,176.34317,TS
 POLE 1 = -33.029541,40.585342,TS
  BEST YET: PERROR = -2.3204574,-5.2353439
 POLE 1 = -33.029541,40.585342,TS
 POLE 1 = -33.029541,99.320220,TS
 POLE 1 = -33.029541,94.883903,TS
  BEST YET: PERROR = 3.5974579,0.26409531
 POLE 1 = -32.187526,41.242080,TS
 POLE 1 = -35.317874,2604.1665,TS
INST=11
 POLE 1 = 0.00000000,342.92785,TS
 POLE 1 = -26.317544,176.46040,TS
 POLE 1 = -26.317544,176.51063,TS
 POLE 1 = -33.029541,36.125816,TS
  BEST YET: PERROR = -2.3204574,-0.77581787
 POLE 1 = -33.029541,36.125816,TS
 POLE 1 = -33.029541,94.459716,TS
 POLE 1 = -33.029541,94.317306,TS
 POLE 1 = -35.138202,53.646865,TS
 POLE 1 = -34.716053,58.438884,TS
 POLE 1 = -32.292720,36.773082,TS
 POLE 1 = -35.317874,2604.1665,TS
INST=12
 POLE 1 = 0.00000000,342.94900,TS
 POLE 1 = -26.317544,176.42877,TS
 POLE 1 = -33.029541,94.537765,TS
 POLE 1 = -33.029541,94.631347,TS
 POLE 1 = -35.138202,38.819107,TS
 POLE 1 = -34.716053,39.188758,TS
 POLE 1 = -34.716053,57.747837,TS
 POLE 1 = -34.716053,57.514701,TS
 POLE 1 = -35.329586,47.366230,TS
 POLE 1 = -35.138202,53.646865,TS
 POLE 1 = -35.560665,38.441642,TS
 POLE 1 = -35.560665,24.805942,TS
 POLE 1 = -35.319591,2604.1665,TS
INST=13
 POLE 1 = -26.317544,176.46971,TS
 POLE 1 = -33.029541,94.477058,TS
 POLE 1 = -35.138202,34.124813,TS
  BEST YET: PERROR = -0.21179580,1.22518540
 POLE 1 = -34.716053,34.539981,TS
  BEST YET: PERROR = -0.63394545,0.81001665
 POLE 1 = -34.716053,57.875385,TS
 POLE 1 = -34.716053,58.028068,TS
 POLE 1 = -35.329586,39.472026,TS
 POLE 1 = -35.138202,38.819107,TS
 POLE 1 = -35.138202,43.994682,TS
 POLE 1 = -35.138202,43.688228,TS
 POLE 1 = -35.316867,47.810382,TS
 POLE 1 = -35.349369,46.669281,TS
 POLE 1 = -35.666271,33.577907,TS
 POLE 1 = -35.349369,36.275165,TS
  BEST YET: PERROR = -6.2942490/10**4,-
  ; 0.92516708
INST = 13
 POLE 1 = -35.349369,36.275165,TS
  BEST: PERROR = -6.2942490/10**4,-0.92516708
```

Fig 4 Iterative attempts of compiler to optimize code. Gradually error and number of instruction steps are reduced until best yet condition cannot be improved.

using the software simulator, which allows simulated inputs to be presented to the chip. Moreover, the simulator allows the resulting outputs produced by the program to be seen in either tabular or graphic form. This process can be repeated to make desired changes, which finally allow a signal processor chip to be programmed (burning the onchip electrically programmable read only memory) and tested in the actual hardware system.

Summary

By applying digital techniques to analog circuits, the designer gains both ease of design and flexibility for

```
OUT2_P1 EQU TEMP
LDA OUT2_P1,OUT1_P1,R00
    ; OUT2_P1=1.00000000*OUT1_P1
LDA OUT1_P1,OUT0_P1,R00
    ; OUT1_P1=1.00000000*OUT0_P1
SUB OUT0_P1,OUT1_P1,R05
    ; OUT0_P1=1.00000000*OUT0_P1-
    ; 0.031250000*OUT1_P1
ADD OUT0_P1,OUT0_P1,R08
    ; OUT0_P1=1.00390625*OUT0_P1-
    ; 0.031372070*OUT1_P1
SUB OUT0_P1,OUT0_P1,R06
    ; OUT0_P1=0.98822021*OUT0_P1-
    ; 0.030881881*OUT1_P1
ADD OUT0_P1,OUT1_P1,R00
    ; OUT0_P1=0.98822021*OUT0_P1+
    ; 0.96911816*OUT1_P1
SUB OUT0_P1,OUT2_P1,R00
    ; OUT0_P1=0.98822021*OUT0_P1+
    ; 0.96911816*OUT1_P1-
    ; 1.00000000*OUT2_P1
ADD OUT0_P1,OUT2_P1,R05
    ; OUT0_P1=0.98822021*OUT0_P1+
    ; 0.96911816*OUT1_P1-
    ; 0.96875000*OUT2_P1
ADD OUT0_P1,OUT2_P1,R07
    ; OUT0_P1=0.98822021*OUT0_P1+
    ; 0.96911816*OUT1_P1-
    ; 0.96093750*OUT2_P1
ADD OUT0_P1,OUT2_P1,R09
    ; OUT0_P1=0.98822021*OUT0_P1+
    ; 0.96911816*OUT1_P1-
    ; 0.95898437*OUT2_P1
ADD OUT0_P1,OUT2_P1,R10
    ; OUT0_P1=0.98822021*OUT0_P1+
    ; 0.96911816*OUT1_P1-
    ; 0.95800781*OUT2_P1
SUB OUT0_P1,OUT2_P1,R12
    ; OUT0_P1=0.98822021*OUT0_P1+
    ; 0.96911816*OUT1_P1-
    ; 0.95825195*OUT2_P1
ADD OUT0_P1,IN0_P1,R00
    ; OUT0_P1=0.98822021*OUT0_P1+
    ; 0.96911816*OUT1_P1-
    ; 0.95825195*OUT2_P1+1.00000
/end/
```

future designs. Digital computers and sophisticated software, used as design tools, simplify the designer's task. The analog designer can use the vocabulary of filter design in the S-plane, when working with digital software tools, to specify poles and zeros and see filter characteristics (eg, gain). Thus, modern software tools can bring the advantages of digital processing to analog circuits.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 725 *Average 726* *Low 727*

THE GLITCH STOPS HERE

When it comes to power conditioning, the user must often provide his own protective devices

by Ruxton Tucker

As more shortages occur in available energy sources, power problems plaguing computers and sensitive electronic equipment are increasing. With data processing equipment operating at increasingly faster speeds, there is a corresponding need to cope with such deteriorations in power quality. Most computer manufacturers have shown concern by studying the problem and reporting the findings to customers.

It is generally concluded that various power problems cause computers to malfunction. As a result, most computer manufacturers discuss problems in site preparation guides or installation manuals. For example, one manufacturer states that designers of

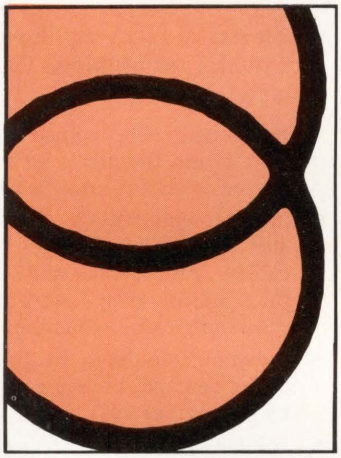
> ...sophisticated electrical and electronic equipment exercise tight control over just about every factor in their systems except the quality of the commercial power lines. Power companies are continuously making a strong effort to maintain the voltage, frequency, and waveform on their lines within acceptable standards, but practical and economic limitations degrade their performance.[1]

Another manufacturer adds that

> Power line disturbances (variations above or below the voltage available at the wall plug) can cause power variations outside the specified tolerances of data processing equipment.[2]

Such statements make it clear that the user is responsible for providing the computer with ac power that meets tolerances specified by the manufacturer. Installation and planning guides also point out that utility supplied power does not generally meet these requirements, noting that the consequences of out-of-specification power can be serious. What the manuals fail to explain is that the typical computer facility experiences an average of 128 error producing power problems each month,[3] causing equipment damage and expensive, time-consuming reprogramming.

Since 1977, Ruxton Tucker has been Director of Marketing for Topaz, Inc, 3855 Ruffin Road, San Diego, CA 92123. He has worked for 19 years in the power conditioning field, including ten years' involvement in engineering design. Mr Tucker holds a BSEE from the University of Illinois and an MBA from Loyola University.



Power problems

Basically there are three major types of power problems—power line noise, voltage fluctuations, and power outages. Power line noise is commonly experienced as static on a radio broadcast or "snow" on a TV screen. As harmless as these minor annoyances may seem, noise can cause serious problems for sensitive, computerized equipment, such as program errors, data entry errors, and system damage.

Power line noise accounts for nearly 90% of all power disturbances that can affect computer operations. (See Table 1.) Common causes of power line noise, including voltage spikes and oscillatory, decaying disturbances, are utility network switching (eg, during load-leveling operations); transients resulting from faults; lightning strikes; and turning on and off air conditioners, copiers, freezers, elevators, and other heavy equipment.

Designers of sophisticated electrical and electronic equipment exercise tight control over just about every factor in their systems except the quality of commercial power lines.

Fluctuating voltage is a common phenomenon that can momentarily dim lights or blow fuses. It also creates serious operational problems for sensitive electronic equipment. When voltage is too high, equipment damage can occur. When voltage is too low, a computer may function improperly and may lose significant portions of data. Unprogrammed data changes, as well as errors in logic and memory, can also result. Although low voltages constitute only 11% of all computer power line disturbances, estimates are that low voltages account for nearly half of the computer related power

TABLE 1[3]

Incidence of Power Line Disturbances

<table>
<tr><th>Power problem</th><th>Rate</th><th>Percent</th><th></th><th></th></tr>
<tr><td>Noise: Oscillatory, decaying transients (15% threshold)</td><td>62.6/mo</td><td>49.0%</td><td rowspan="2">Noise 88.5% of Total</td><td rowspan="3">Noise Disturbances and Voltage Variations 99.5% of Total</td></tr>
<tr><td>Noise: Voltage spikes (25% threshold)</td><td>50.7/mo</td><td>39.5%</td></tr>
<tr><td>Voltage fluctuations (10% threshold)</td><td>14.4/mo</td><td>11.0%</td><td></td></tr>
<tr><td>Power outages</td><td>0.6/mo</td><td>0.5%</td><td></td><td></td></tr>
<tr><td>Total</td><td>128.3/mo</td><td>100%</td><td></td><td></td></tr>
</table>

problems; a relatively long duration of low voltage accentuates the problem. Causes of voltage fluctuations include

- transmission line voltage drops between the utility substation and the user's service entrance caused by normal transmission line impedances.
- intra-building voltage drops between the service entrance and the point of usage. Normal impedances found in cables, connectors, and fuses exacerbate the voltage fluctuations. Heavy start-up currents or changing loads commonly cause reductions in line voltage.
- brownouts initiated by utilities during periods of high power demand. In severe cases, utilities may reduce voltage by as much as 10%.
- voltage sags and surges caused by power line faults or the resultant actions of fault-clearing devices, by sudden heavy loads on the power line (eg, machine start-up) and by the slow reaction time of utility regulating equipment.

Due to the common occurrence of voltage fluctuations, the American National Standards Institute (ANSI) specifications permit ac voltage to drop as much as 11.7% below nominal by the time it reaches user equipment. ANSI standards allow maximum partial voltage loss of −8.3% at the service entrance, and intra-building losses of −3.4%. Since most sensitive electronic equipment is designed to operate within ±10% of normal rated voltage, many serious equipment problems can occur even under normal conditions.

Power line conditioners thus protect against 99.5% of all power line disturbances.

The high demand for electrical energy is producing an increased number of power outages (blackouts). In addition, several utility companies—already supplying power at near capacity levels—plan "rolling blackouts" to guarantee power to critical areas during periods of peak usage. This plan calls for intermittent interruptions, or a timesharing approach, to utility resources. Power outages, the inadvertent loss of all power, can cause problems for computer users, the most critical of which are loss of valuable data and the need for expensive, time-consuming reprogramming. Power outages can be caused by overload of the utility system; overload of the user's power distribution system; or damage to utility generation, transmission, or distribution systems.

Protective solutions

Protection against power disturbances must be directly proportional to the need for accuracy and reliability in a computer application. The more critical the application, the greater the need for protection. Products can be used to help solve power problems and should be reviewed by users or potential users of sensitive electronic equipment. Such products include filters, ultra-isolation transformers, line voltage regulators, power line conditioners, and uninterruptible power systems.

Filters. Filters are a selective network of inductors and capacitors, which allow signals of certain frequencies to pass through while blocking or attenuating other frequencies. They are typically useful for handling frequencies above 50 kHz. However, most transient contamination of computers occurs in the 400-Hz to 50-kHz region[3]; filters are inherently inefficient at these lower frequencies. Furthermore, resistive and dielectric losses indicate that filters are not especially effective at higher power levels. Most filters are inexpensive and many computer manufacturers provide some noise filtering. Filters are only a partial solution. Nonetheless,

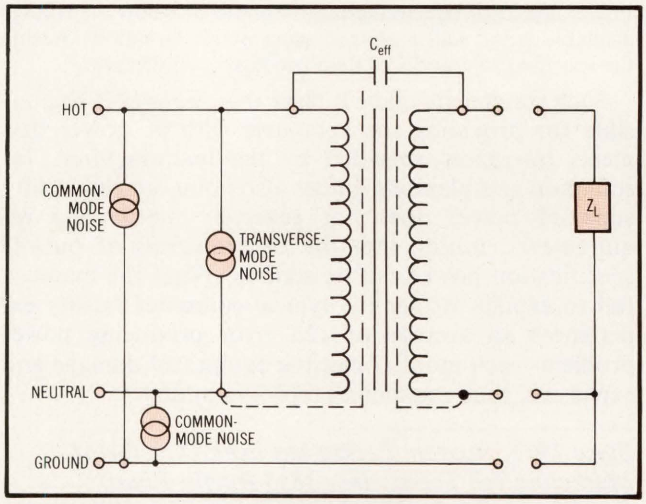


Fig 1 Ultra-isolation transformer. Two center lines represent core material or laminations. C_{eff} represents effective coupling capacitance between primary and secondary coils. User equipment is protected against electrical disturbances ranges from dc to several megahertz.

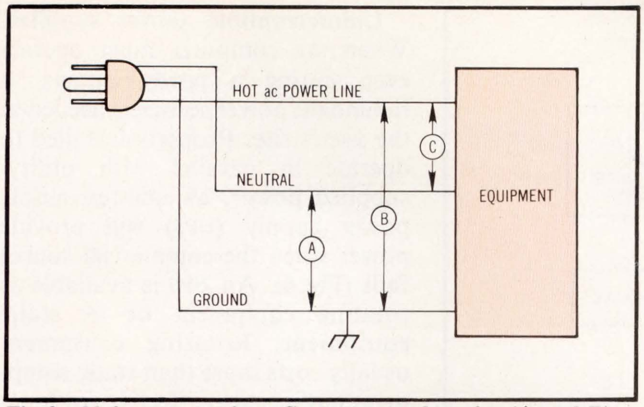


Fig 2 Noise attenuation. Common-mode noise (A and B) creates serious problems for computer equipment that uses common (ground) as a reference for logic circuitry. Internal dc power supplies, although effective at removing lower frequency components of transverse-mode noise (C), do not attenuate common-mode noise. Therefore, protection from high frequency components of transverse-mode noise and all frequencies of common-mode noise typically is needed.

the average cost of eight cents per voltampere of power handling capability (which differs from the cost of power watts consumed) is nominal.

Ultra-isolation transformers. To protect the computer from noisy power lines, an ultra-isolator is useful. An ultra-isolator is a transformer with an unusually high degree of isolation (Fig 1). This device attenuates noise in both directions—in as well as out. It also attenuates common-mode noise and transverse-mode noise. Common-mode noise occurs between the ground

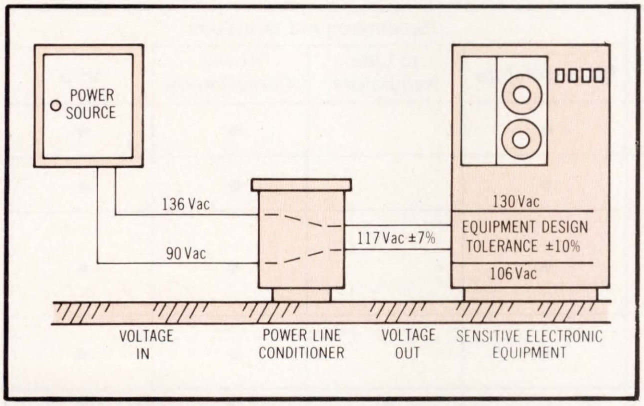


Fig 3 Power line conditioner application. Varying input voltages, as low as 90 Vac and as high as 136 Vac, are received and immediately regulated to within ± 7% of nominal. Thus, ac power is controlled within the ± 10% design limits of most sensitive equipment. Noise attenuation is also provided by its ultra-isolation transformer to protect against noise and transients in ac power source.

wire and both current-carrying conductors, while transverse-mode noise occurs between the current carrying conductors (Fig 2).

An ultra-isolator installed between the user's equipment and the power line can prevent malfunction of equipment caused by noise transients (400 Hz to 5000 Hz) and voltage spikes (10 kHz to 100 kHz) in all frequencies from dc to several megahertz. In other words, an ultra-isolator protects against 88.5% of all power line disturbances that can affect the operation of sensitive equipment. Because of its excellent attenuation of common-mode noise, an ultra-isolator also eliminates special grounding requirements. An ultra-isolator costs about 15 cents per voltampere of power handling capability.

AC line voltage regulators. If the sensitive equipment operates in low or high voltage areas, or in an area susceptible to brownouts, then an ac line voltage regulator will correct these voltage variations. A line voltage regulator can provide steady, regulated, distortion-free ac power to the computer. Regulators automatically step-up or step-down voltage to protect against variations; short- or long-term changes in the input line voltage(s) are thus regulated for single- or 3-phase operation.

To be effective now and in the next few years, a good regulator must be able to accept normal rated voltage, ranging from 15% above rated to 25% below rated voltage. The regulator must also correct these variations to within the 10% tolerance band of most computer equipment. Some computers require even tighter tolerances than 10%. For example, one processor's installation manual states,

> The line-to-line, steady-state voltage tolerances when the equipment is operating must be maintained within plus six percent or minus eight percent of the normal rated voltage, measured at the receptacle.[4]

Voltage regulation is thus needed for most of these installations. Line voltage regulators cost approximately 25 cents per voltampere.

A power line conditioner output therefore provides safety isolation and noise attenuation for all forms of noise that affect computer operation.

Power line conditioners. Power line conditioners combine voltage regulation, as described previously for ac line voltage regulators, as well as filtering and isolation, as discussed for ultra-isolators. Power line conditioners thus protect against 99.5% of all power line disturbances. The power line conditioner also protects computers from the effects of short- and long-term voltage fluctuations (Fig 3). Even when utility power strays above or below rated voltage by 20%, a power line conditioner will correct the voltage into the computer's tolerance range within 10 ms. Most computers are designed to withstand voltage fluctuations for periods not exceeding 15 to 20 ms.

To eliminate faults caused by short-term power line disturbances or transient contaminated power, a power line conditioner uses either a filtering system or an ultra-isolation transformer. Filtering uses elements in the power line circuitry to significantly reduce the amount of high frequency noise that can pass from the power line to the user's equipment. An ultra-isolation transformer magnetically couples the line power to the user's equipment. A power line conditioner output therefore provides safety isolation and noise attenuation for all forms of noise that affect computer operation. Power line conditioners cost approximately 45 cents per voltampere. Varying sizes of power line conditioners can protect the many types of sensitive electronic equipment.

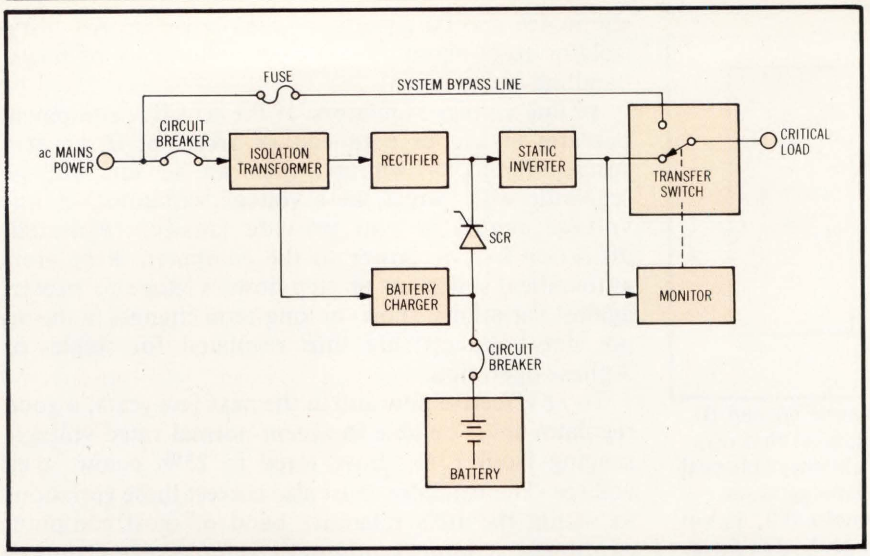


Fig 4 Online, uninterruptible power supply. If ac mains voltage falls more than 15% below nominal, the silicon controlled rectifier (SCR) turns on, connecting battery to inverter input. Stored energy at rectifier can continuously power inverter during SCR turn on. Inverter supplies stable, transient-free power to critical load until system battery is discharged. When ac mains power is restored, rectifier automatically supplies inverter with dc power. To ensure power to critical load during next ac mains outage, SCR is turned off and battery is automatically recharged. If monitor senses ac voltage loss at inverter output, transfer switch automatically transfers load to ac mains.

Uninterruptible power supplies. When the computer must operate even during a power outage, a redundant power source is needed at the user's site. Properly installed to operate in parallel with utility-supplied power, an uninterruptible power supply (UPS) will provide power when the commercial source fails (Fig 4). An UPS is available as rotating equipment or as static equipment. Rotating equipment usually costs more than static equipment but it is also effective for long-term outages of several hours. These devices may be powered by inertia, internal combustion engines, or other mechanical means. Static equipment uses electronic circuitry, which includes an inverter to generate sinusoidal ac power from a battery (dc source).

In either case, an UPS is expensive when compared to the previous solutions discussed. The installed cost of an UPS ranges from $2.50 to $3.50 per voltampere. However, an

TABLE 2

Power Problem Solver Guide

	Common Power Line Problems	Recommended Solutions			
		Ultra-isolators	ac Line Regulators	Power Conditioners	UPS
Power Line Noise	Lightning strikes causing up to 3000-V transients	•		•	•
	Spikes caused by utility network switching	•		•	•
	Transients produced by operating machine tools, air conditioners, copiers, lighting systems, and other office equipment	•		•	•
	Ringing disturbances caused by power factor correction capacitor switching carried out by utility	•		•	•
Voltage Fluctuations	Brownouts		•	•	•
	Undervoltages or overvoltages caused by faults and fault clearing devices		•	•	•
	Voltage fluctuations caused by heavy equipment using the same source		•	•	•
	Steady state voltage variations from nominal. Chronic low line voltage		•	•	•
	Voltage fluctuations caused by user owned generators		•	•	•
Power Outages	Temporary outage caused by rotary system startup				•
	Momentary power interruptions from faults or overloads on power line				•
	Blackouts				•
Other Power Problems	Ground not dedicated or isolated	•		•	•
	Shock hazard to systems, operators, or users	•		•	
	Frequency variations caused by user owned generators				•

UPS is the only available method for eliminating all power line problems, including blackouts, that affect computers. Based on a total of 109 monitor months at 29 locations across the United States, it was found that power outages lasting longer than 10 ms occur less than once a month. (See Table 1.)[3]

...the power line conditioner is the most cost-effective choice for solving computer grade power problems.

Summary

Above all, the user is responsible for protecting data processing equipment. Table 2 reveals the relative effectiveness of devices used to protect equipment from common power line problems. (Because of relatively low protective features, filters are not included in this Table.) Power line conditioners and UPS offer the most comprehensive solutions. The UPS also keeps the computer operational during power outages. But because power outages account for only 0.5% of all power line disturbances, the power line conditioner is the most cost-effective choice for solving computer grade power problems.

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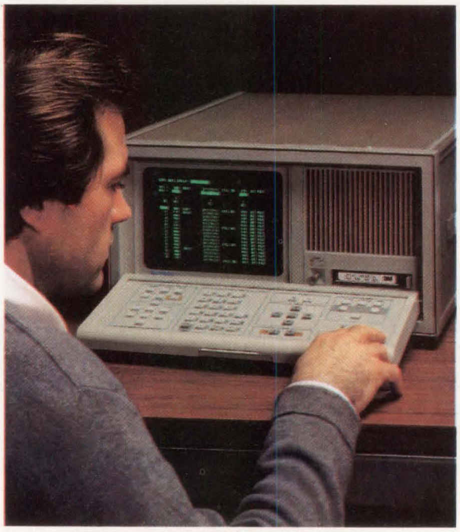

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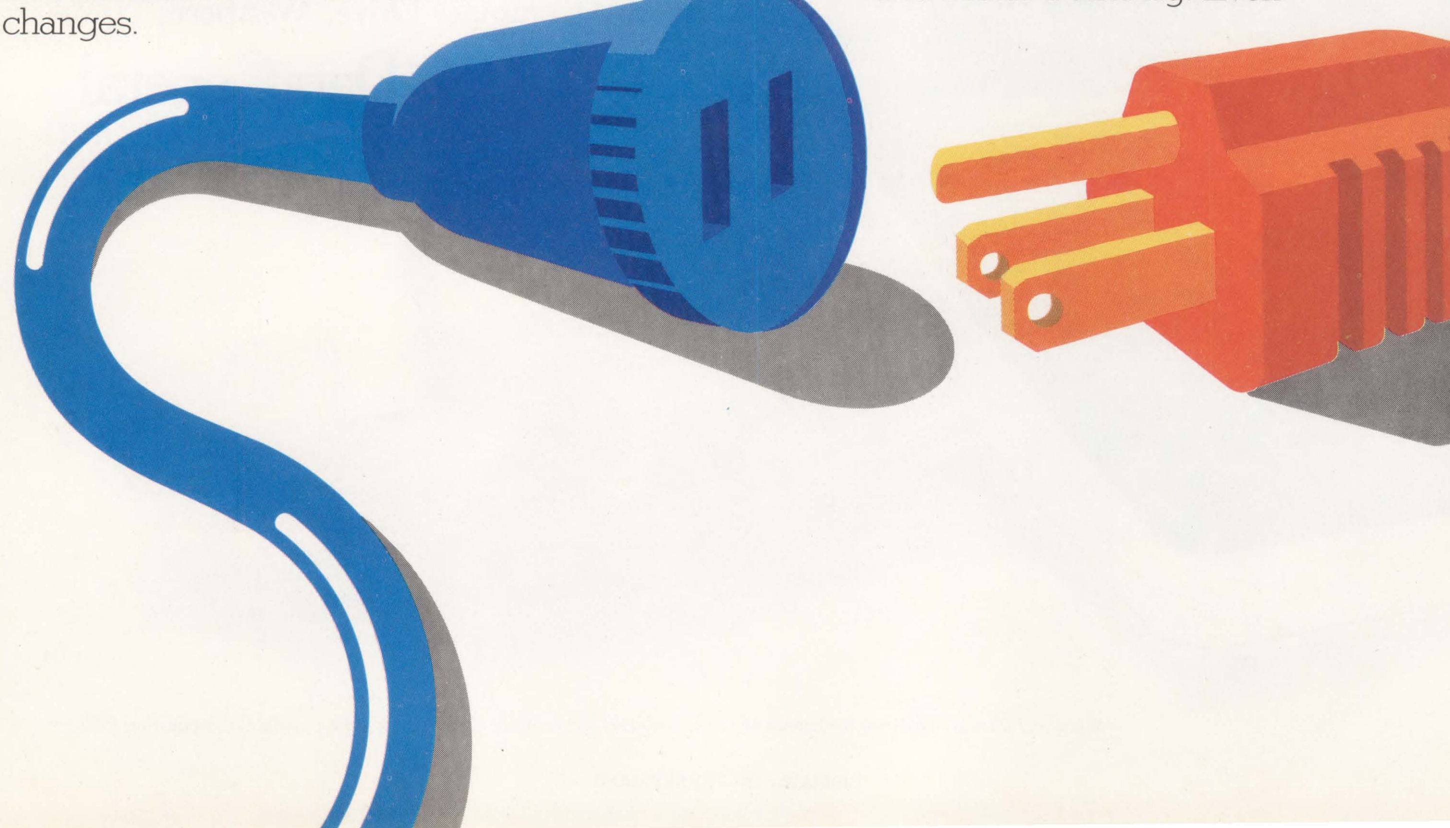

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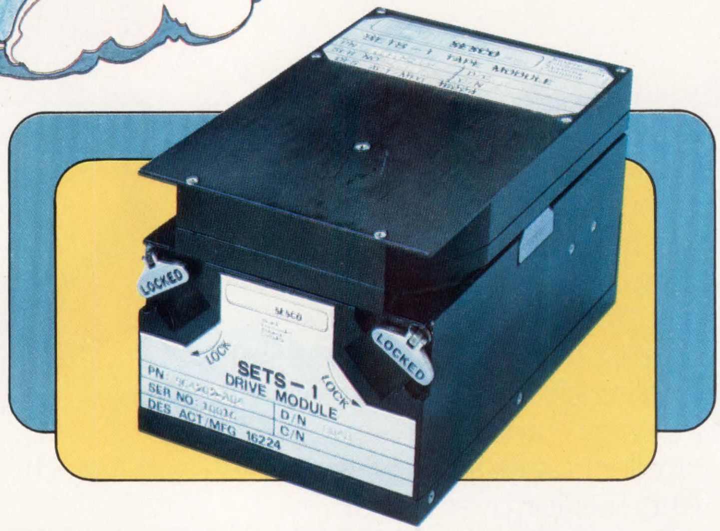

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EFFORTLESS ERROR MANAGEMENT

Basic application of error management techniques is based on error history, including the double complement error correction cycle

by Bob Nelson

When implemented only in hardware, error management is generally limited to simple error logging. In most systems, error logging hardware is designed to capture the location of one error and use this information for maintenance purposes. In more sophisticated systems, however, software extends the error management function: after hardware obtains error information, data are accumulated on disk to expand storage capacity for information relating to error locations. Beyond the error information storage function of error management, which is useful for maintenance, some systems implement a correction procedure based on error history. If two errors occur in a memory word where an error has previously occurred, it is likely that both errors can be corrected. The basic error management system described in this article will provide a high correction rate for all 2-bit errors, except when two soft errors simultaneously occur in a memory word with no error history.

Error management system

The error management system comprises the central processing unit (CPU), the system memory, an error checking and correction (ECC) device, and an error management unit (EMU). The CPU is a 16-bit machine and requires commensurate memory. Actual memory, including the six check bits that the ECC device requires, is 22 bits wide. The ECC device is based on the DP8400 monolithic ECC unit manufactured by National Semiconductor. The EMU is a hypothetical device that can be implemented in hardware, partially or entirely, depending on system requirements.

The DP8400 provides several functions and features that allow easy implementation of a minimum hardware error management system. Error indicating syndrome words must be available to the EMU directly and syndrome injection capability must exist. (See "Simplification of 2-Bit Error Correction," Jan 1982, pp 127-136, for a discussion of the DP8400's syndrome input/output ports.) The DP8400 also provides the hardware required to perform a double complement correct cycle. Error flags must be provided to discriminate between 2-bit and detectable 3-bit errors; the DP8400 provides three such flags to include this function.

Vertical columns in the matrix shown in Fig 1 represent the single data bit error indicating syndrome words. A double data bit error syndrome word results from exclusive ORing (XOR) the two single-bit error indicating syndrome words that correspond to the bit locations in error. A detectable triple data bit syndrome word is any one of the ten syndrome words, not included as part of the matrix, which contains either three or five 1s. Syndrome words that represent check bit errors contain 1s in the syndrome word bit positions corresponding to the check bits in error, and 0s in the remaining bit positions. An error condition involving the data and check bit fields provides a syndrome word that represents the data bit(s) in error, XORed with a syndrome word representing the check bit(s) in error.

Error management unit

The EMU is memory intensive and uses memory in the form of an associative stack. Three fields constitute each of the 16 words in the stack: the 8-bit address field, which is the associative portion of the word; the 2-bit

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0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
LSB						error locations									MSB		
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	LSB	0
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1		1
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	syndrome	2
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	words	3
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1		4
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	MSB	5

Fig 1 DP8400 syndrome word generator. Presenting errors to unique matrix produces syndrome words.

tag field; and the 6-bit syndrome field (Fig 2). The pointer addresses the stack. The EMU also contains a syndrome comparator, a temporary syndrome register, and a tag bit attribute register and comparator. The EMU monitors most ECC flags and provides flags of its own both to the ECC device and to the CPU; monitoring the memory address and comparing that address to the

	address	tag bits	syndromes
Word 0	7 6 5 4 3 2 1 0	1 0	5 4 3 2 1 0
•			
•			
•			
Word 15	7 6 5 4 3 2 1 0	1 0	5 4 3 2 1 0

Fig 2 Associative stack organization. Of 16-bit address, eight address bits are most significant bits. Tag bits indicate type of error, and syndrome bits contain syndrome word.

stack's address field is a major function of the EMU. When the "stack full" flag is off, however, the number of words in the match area is limited by the location of the stack pointer. If a match occurs, ie, if the current memory address is an address at which an error occurred previously, the information obtained from the previous error can be used to correct more than one error bit. Each EMU function will be defined in a subsequent section of this article.

Single-bit error: first occurrence

Absence of a match, accompanied by single-bit error indicating flags, defines the first occurrence of such an error in the current address. The error may be in the data bit or check bit field of memory. Error address, tag bits (Fig 3), and single-bit error indicating syndrome word are stored in the EMU stack. Tag bits are assigned a value of 00, indicating a soft single-bit error. The stack pointer is then incremented and the ECC device corrects the single-bit error in the usual way. Stored syndromes contain an odd number of 1s. In Fig 4, data bit 5 fails at memory address 52 HEX, check bit 3 fails at address 45 HEX, and data bit 9 fails at address C7 HEX. Since the errors have not occurred previously at these addresses, they are given a tag bit value of 00. Logging errors should not impact the speed or function of the ECC system in performing single-bit error correction.

Tag Bits	Information Status
00	soft single-bit error
01	firm single-bit error
10	hard single-bit error
11	hard double-bit error

Fig 3 Tag bit field of stack indicates error type for more efficient processing by error management system. Tag bit field could be extended in other systems to provide more error information.

Double-bit error: first occurrence

When a double-bit error occurs at an address with no error history, the EMU exercises the only available option, a double complement correct cycle. As the ECC device enters the complement write mode, the syndrome word that represents the double-bit error condition is stored in the temporary syndrome register. Then the ECC system performs a double complement correct cycle to generate a second set of error flags. If two soft errors caused the initial indication of a 2-bit error, the second set of error flags will also indicate two errors and represent a noncorrectable condition. Any double-bit error situation other than that of two soft errors will produce error flags that indicate a correctable condition at the conclusion of the double complement correct cycle.

One hard and one soft

Error flags produced after the second complement of the double complement correct cycle indicate a single error if the initial error condition was one hard and one soft. At that point, the hard error will have been "corrected" and the remaining soft error indicated. The ECC device will generate a new single-bit error indicating syndrome word, which the EMU will XOR with the previously stored double-bit error indicating syndrome word. The result, which is the single-bit hard error indicating syndrome word, is stored in the stack.

To identify the bit as a single hard error, the tag bit field is set to a value of 10. After the error information is stored, the stack pointer is incremented. The ECC device corrects the single error in the usual manner. The remaining soft error may be either a check bit error or a data bit error. Fig 5 illustrates a soft error in data bit location 2 and a hard error in data bit location 11. A double complement cycle corrects the error in location 11. Representing the soft error, a new syndrome word is then XORed with the original syndrome word to produce

	error address	tag bits	syndromes	
Word 0	1 0 1 0 0 0 1 0	0 0	1 1 0 0 0 1	data bit 5
Word 1	0 1 0 0 0 1 0 1	0 0	0 0 1 0 0 0	check bit 3
Word 2	1 1 0 0 0 1 1 1	0 0	0 0 1 0 1 1	data bit 9
Word 3	X X X X X X X X	X X	X X X X X X	
•				
•				
•				
Word 15	X X X X X X X X	X X	X X X X X X	

Fig 4 Logging errors on EMU stack. Single-bit errors occurring at addresses with no previous error history receive tag bit value of 00.

```
1st error  0010000000010000  111010  2 and 11
D → D̄      1101111111101111  000101  complement
2nd read   1101111111111111  000101  11 corrected
D̄ → D      0010000000000000  111010  complement

                             101001  new syndromes

                             010011  2 + 11 XOR 2 = 11
```

(a)

Word	error address	tag bits	syndromes	
Word 3	0 0 1 1 0 1 1 0	1 0	1 0 1 0 0 1	data bit 2
Word 4	0 1 1 0 1 1 0 1	1 0	0 1 0 0 0 0	check bit 4

(b)

Fig 5 After correcting hard error in bit position 11 (a), system stores hard error syndrome on associative stack (b) and sets tag bit field to indicate single-bit hard error.

Word	error address	tag bits	syndromes	
Word 0	1 0 1 0 0 0 1 0	0 0	1 1 0 0 0 1	data bit 5
Word 1	0 1 0 0 0 1 0 1	0 0	0 0 1 0 0 0	check bit 3
Word 2	1 1 0 0 0 1 1 1	0 0	0 0 1 0 1 1	data bit 9
Word 3	0 0 1 1 0 1 1 0	1 0	1 0 1 0 0 1	data bit 2
Word 4	0 1 1 0 1 1 0 1	1 0	0 1 0 0 0 0	check bit 4
Word 5	1 0 0 0 0 1 0 0	1 1	1 0 1 0 0 0	2 hard
Word 6	X X X X X X X X	X X	X X X X X X	
•				
•				
•				
Word 15	X X X X X X X X	X X	X X X X X X	

Fig 6 Contents of EMU's stack containing initial occurrence of each error type.

the syndrome word that represents the hard error. These hard error syndromes are stored as shown in Fig 6, which also shows the storage of a hard check bit error at address 6D HEX.

Two hard

An ECC "no-error" flag, following a double complement correct cycle, indicates an initial error condition of two hard errors. Data following the second complement are correct; since no error exists, a syndrome word of all zeros is generated. The EMU will store the error address, the tag bits, and the contents of the temporary register. Tag bits will be given a value of 11, indicating a double-bit hard error. The stored syndrome word is then XORed with the contents of the temporary syndrome register and the new syndrome word from the ECC device (as with a one soft/one hard error condition), and the stack pointer is incremented. In this example, the information obtained from a double-bit hard error at address 84 HEX, including a syndrome word of 101000, is stored. A 2-bit error indicating syndrome word provides no information regarding the location of the errors. Errors in data bit locations 13 and 15, for example, produce the stored syndrome word as would errors in check bit locations 3 and 5. Fig 6 illustrates the contents of the associative stack portion of the EMU following the first occurrence of each type of error discussed. Word 5 in the stack represents the double-bit hard error.

Logging the errors

As errors occur at new addresses, error data are stored in the stack and the stack pointer is incremented. When information is entered in stack word 15 a "stack full" flag is set. The stack full flag directs the pointer to the lowest word address location in the stack containing the value 00 in the tag bit field. After storing data, the stack pointer goes to the next highest word address location that contains a 00 in the tag bit field. The stack contains the most recent error addresses at which single-bit soft errors occurred and all addresses at which firm or hard errors occurred. When no tag bit field contains 00, the "overflow" flag is provided and no additional stack storage occurs. However, logged error information is available to the system. One of the DP8400 modes, for example, allows data to be provided to the syndrome input/output ports and output through the data input/output ports, a capability that allows the error information to be dumped to the system disk for an additional level of storage. In another mode, the DP8400 can internally transfer data from the data input to the syndrome output, allowing the stack to be loaded from the system disk via the data bus.

Error locations are stored in real time by the logging procedure. Error resolution is defined by the correspondence of the memory address bits to the EMU address inputs. The EMU described here has eight address inputs that allow chip level error resolution in a 1M-byte memory system when 64k-bit dynamic random access memories are used. Since the EMU does not monitor the least significant eight memory address lines, error information—specifically the address and syndromes as stored in the EMU—represents a memory chip location. If a "read error" match occurs, only the tag bits and/or the stored syndrome word may be updated. Therefore, each unique error address can exist in a single stack location. Each stored word location defines one defective bit (chip) location if the syndrome word indicates a single-bit error. In some cases, the error information will represent two hard errors, which normally cannot be located.

Relocating the errors

In response to new error information, it may be desirable to change the error locations as defined by the syndrome words stored in the EMU. If a single-bit error is accompanied by an address match and tag bits representing a stored single-bit soft error, but if the syndrome comparison indicates that a different bit is in error, the syndrome field of the matching stack word should be changed to the new syndrome word. The ECC will correct the single-bit error in the normal manner, and the most recent soft error information for that memory address will be maintained. Previous soft error information can be offloaded to a secondary storage device prior to the update.

Stored Error	Tags	Detected Error
1 bit, firm	01	1 soft, 1 hard
1 bit, hard	10	1 soft, 1 hard
1 bit, soft	00	1 soft, 1 hard
1 bit, soft	00	2 soft
1 bit, firm	01	2 hard
1 bit, hard	10	2 hard

Fig 7 Errors for syndrome injection in order of probability. Syndrome injection in the DP8400 allows faster correction than double complement method.

Maintenance help

Maintenance tools are a by-product of the EMU system. During the ECC procedure, error locations are identified and error types determined. EMU generated flags, which are provided when the stack contents reach a defined level, allow the error information to be offloaded to the system disk and the EMU to be cleared and reloaded with selected error information from disk. After the error information is loaded on disk, the system can be powered-down for maintenance. Following system power-up, suspect information about error location may be written to the EMU. This extended logging capability is part of the total error management system.

Redefinition

When a single-bit error occurs in a location at which a single-bit error has occurred previously, and the stored syndrome word is the same as the single-bit error indicating syndrome word generated by the ECC device, it may be necessary to redefine the error type. If the match provides tag information indicating a soft error (tag field = 00), the tag field will be changed to 01 to indicate a single-bit firm error. Such a redefinition is valid. For instance, a firm error may be an unproved hard error or an error-prone memory device sensitive to alpha particles, system noise, or both. Such an error can be treated as either a soft error or a hard error, or be given a definition based on the present error. For the purpose of this discussion, a firm error will be treated as a hard error.

With...double complement correct cycles, 100% of 2-bit errors can be corrected when...one of the errors is hard, regardless of...error history.

Although a soft error can occur in any given location within a chip, a second soft error is most likely to occur within the same chip. Error-prone chips are identified and tagged as firm error locations. In the EMU, both the syndromes and the address field are compared, providing higher error resolution within a word. In this EMU, the tag bit field is updated and the syndrome field is rewritten (if the second error is not in the same chip, the most recent single-bit error location in that word will be stored). The ECC device corrects the single-bit error in the normal manner.

Double-bit error: subsequent occurrence

When a double-bit error occurs and the EMU obtains a match, the contents of the tag bit field dictate the possible courses of action (Fig 7). If the tag bits are 11, for example, a double complement correct cycle is the only option. If the tag bits indicate a single-bit hard error location, a double complement correct cycle could be implemented. On the other hand, it is reasonable to assume that the stored syndrome word represents one of the two present error locations; in that case the error can be corrected without additional memory cycles.

One hard—one soft, one hard

If a match is obtained, tag bits are 10, and a 2-bit error has been detected, it is most likely that one error is soft and the other hard. Syndrome injection will obtain the fastest correction. The syndrome word in the stack, which usually represents the hard error location, is presented to the DP8400. There it is XORed with the internally generated syndrome word to provide the resulting soft error syndrome word, which is then presented to the syndrome decoder. After the ECC device corrects the soft error, it generates new check bits and zero syndromes. XORing the new syndromes with the still-injected hard error syndrome word, the unit decodes the hard error location and corrects the second error. This procedure allows correction of 2-bit errors without additional memory cycles, once the location of the hard error has been determined. Although a firm error is treated as a hard error, it must be given special consideration during system maintenance.

One soft—one soft, one hard

If a 2-bit error is detected and a match obtained with a tag of 01, the highest probability is that one error is soft and one is hard. The syndrome word from the stack is injected into the DP8400, where it is XORed with the internally generated syndrome word, providing the result to the syndrome decoder. Correcting the soft error, the ECC device generates new check bits and syndromes, XORs the new syndromes with the still-injected hard error syndrome word provided by the EMU, decodes the known error location, and corrects it. When the location of one error has been determined, this procedure allows high speed correction of 2-bit errors without additional memory cycles.

One soft—two soft

If a match is obtained, tag bits are 01, and a 2-bit error is detected, both errors are probably soft and can be corrected by syndrome injection. The syndrome word in the stack (which often represents one of the soft error locations) is presented to the DP8400, where it is XORed with the syndrome word, generated internally to provide the unknown soft error syndrome word to the syndrome decoder. Correcting the soft error, the ECC device generates new check bits and zero syndromes. XORing the new syndromes with the still-injected "known" soft error indicating syndrome word, it decodes the error location and corrects the second error. Thus, two soft errors can be corrected if the location of one is known.

One firm or hard—two hard

If two hard errors occur at an address where a single-bit hard error has been recorded previously, syndrome injection will usually accomplish the correction. The syndrome word in the stack, which most likely represents one of the hard error locations, is presented to the DP8400 where it is XORed with the internally generated syndrome word, providing the result to the syndrome decoder. The ECC device corrects the first error and generates new check bits and zero syndromes. XORing the new syndromes with the still-injected "known"

error indicating syndrome word, the unit corrects the second error. This procedure allows high speed correction of two hard errors when the location of one is known.

Double complement

The double complement error correction cycle is effective for locating hard errors in an error management system. This technique is effective when speed of error correction is of less concern than system integrity. Use of the double complement correct cycle following the detection of every error enhances error determination and correction. Immediate determination of single-bit hard errors improves the possibility that double-bit errors in the same defined address can be corrected. The next level of error detection and correction efficiency, using the double complement correct cycle for each detected error, includes those error types noted in Fig 8.

Stored Error	Tags	Detected Error
1 bit, soft	00	2 hard
1 bit, firm	01	2 soft
1 bit, hard	10	2 soft

Fig 8 Errors for double complement correction. When speed is of less priority, double complement method allows more precise error detection, logging, and correction.

One soft–two hard

A no-error indication from the ECC device following the double complement correct cycle will complete the definition of the error type—defined as a 2-bit error by the syndrome word stored in the temporary syndrome register—as a 2-bit hard error. If a match occurs but the tag bit field indicates a single-bit soft error, the tag bit field can be changed to 11, indicating two hard errors, and the syndrome field replaced with the contents of the temporary syndrome register. Error information can be offloaded to a secondary storage device before this update.

One firm or hard–two soft

If the ECC device generates error flags indicating a double-bit error at the conclusion of the double complement correct cycle, the 2-bit error that instigated the cycle remains and contains two soft errors. Since the only recorded error at the current memory location is hard, the errors are not recoverable and system operation terminates. In some systems, a firm error may be defined as a soft error, and data may be recovered. When offloading of soft errors is practiced, the disk or other storage mechanism can be interrogated for prior memory errors at the current address. These soft errors can be corrected if proper information is available.

Two hard–double error

When a match occurs and the tag bits indicate that an earlier 2-bit error has been recorded for the present memory address, ECC device's error flags identify the error type after the double complement correct cycle. If the present error is soft, system operation must be terminated—assuming that no additional relevant information regarding errors at this address is available from other sources. If the second set of error flags indicates that the present error is a 2-bit hard error, the errors can be corrected. Comparing the syndrome words in the temporary syndrome register and the stack will provide additional information. If the syndrome words do not match, three or four hard errors exist and system operation must be terminated.

Locating two hard errors

When the presence of two hard errors has been determined, a subsequent access at the same address will most likely indicate a single-bit error. If the single-bit error is in one of the two locations that had defined the previous 2-bit hard error, adequate information is available to locate the other error. The temporary syndrome register will store the single-bit error indicating syndrome word. Data are corrected by the double complement correct cycle, and the syndrome word in the stack can be replaced by the contents of the temporary syndrome register. The double-bit hard error indicating syndrome word can be offloaded and the word replaced. The new word will then be offloaded and XORed with the first syndrome word, keeping the result in the secondary storage element. Secondary storage is available for interrogation if additional errors occur in the same address. In more sophisticated error management systems, additional tag bits are made available in the EMU stack. One of these tag bits can be used to indicate that additional error information exists in secondary storage for that error address.

Summary

The simplified error management system presented here allows correction of double-bit errors if one of the errors has previously occurred. With the use of double complement correct cycles, 100% of 2-bit error correction is provided when at least one of the errors is hard, regardless of previous error history. Enhanced error logging is provided with error type determination capability. Maintenance aids are provided through the DP8400's bidirectional data transfer capability between the syndrome input/output and data input/output ports.

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High 731 *Average 732* *Low 733*

This is the last in a 3-part series on error management. The first part, "Error Correction the Hard Way," appeared in December 1981 and the second part, "Simplification of 2-bit Error Correction," was published in January 1982.

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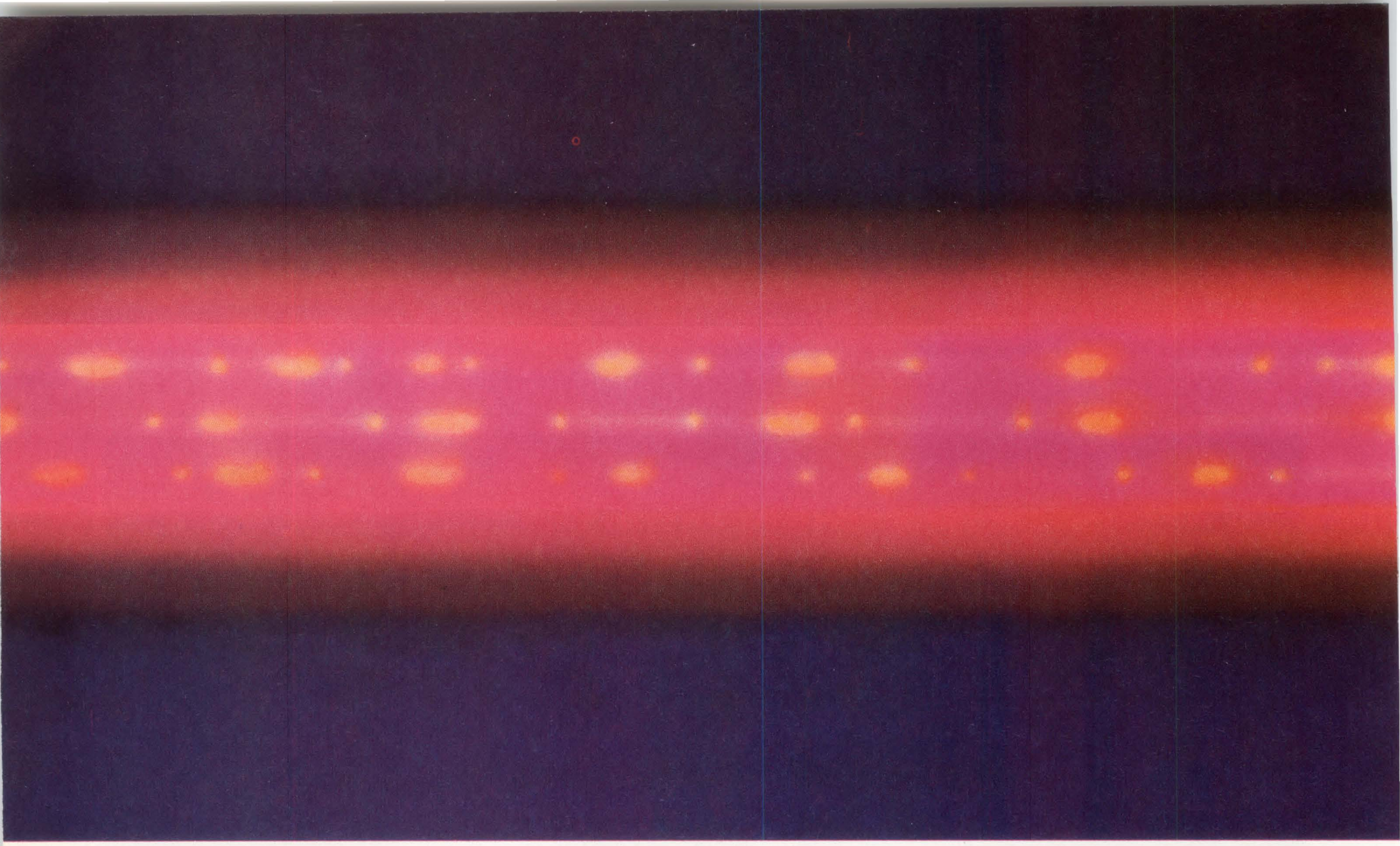

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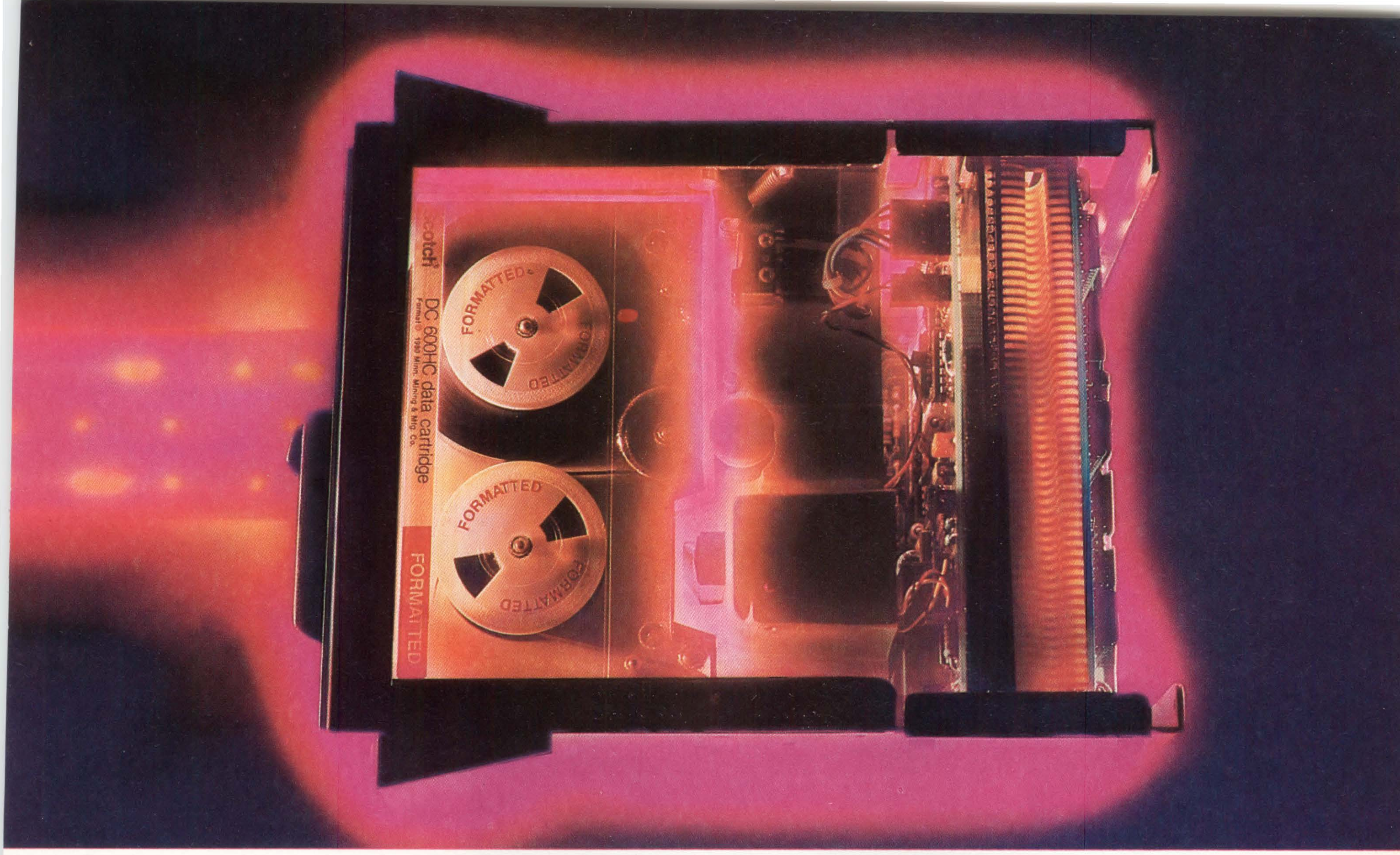

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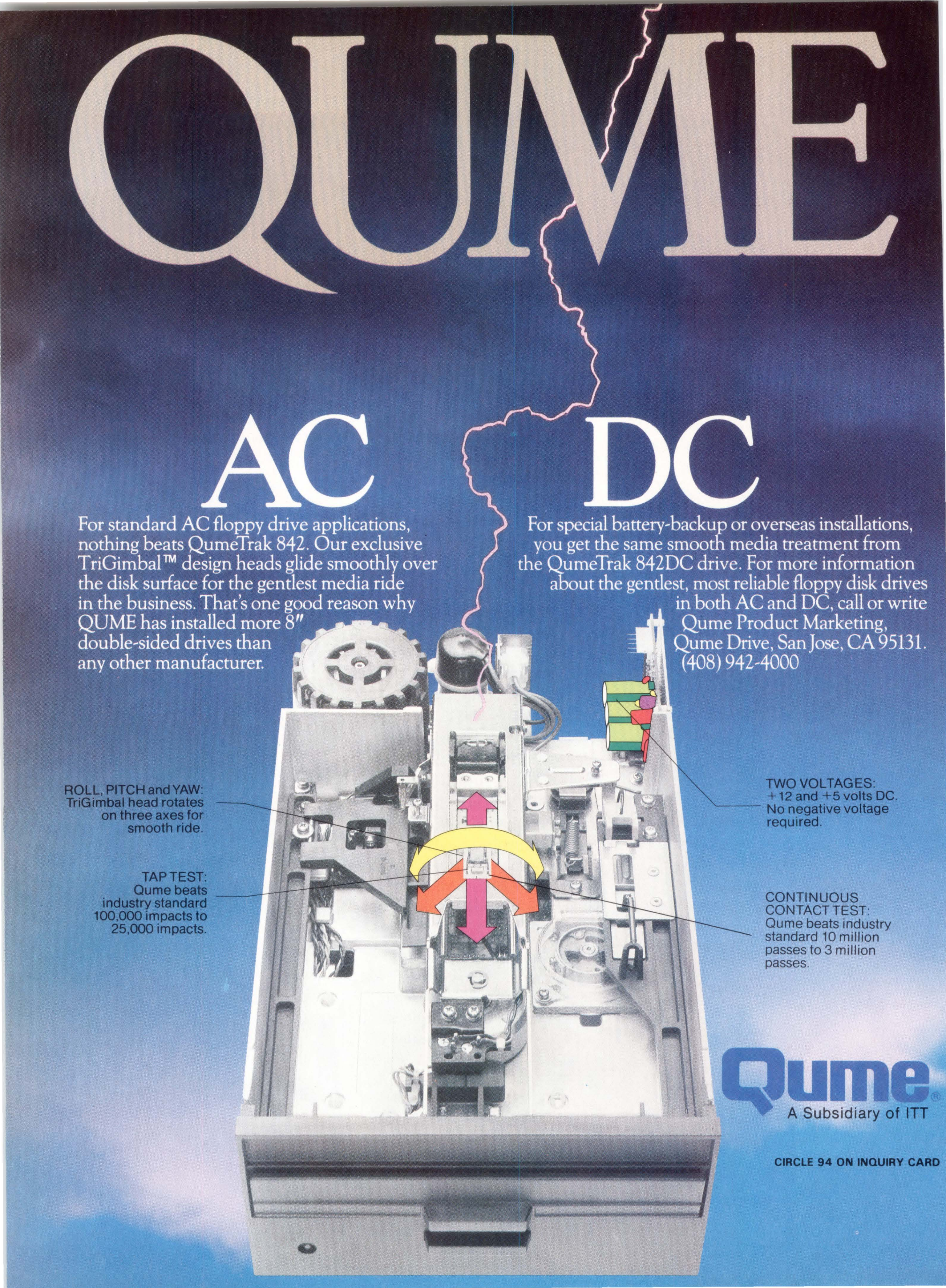
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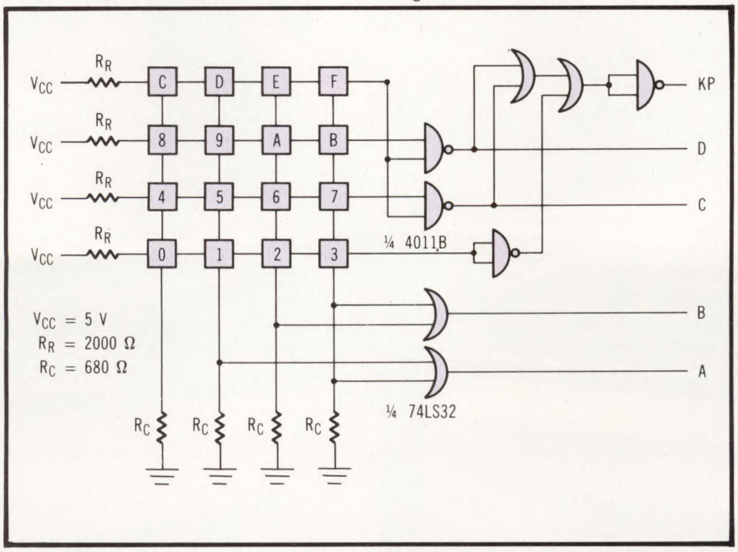
ECONOMICAL KEYPAD ENCODING

Through judicious use of biasing resistors, this 2-chip encoder circuit capitalizes on the differences between CMOS and LS/TTL

by Jeff Hurlburt

A simple circuit design can generate hexadecimal codes using inexpensive gates and a 4 x 4 matrix keypad. The Figure has a 2-family keypad encoder circuit requiring only one 74LS32 (quad OR) and one 4011 (quad NAND) integrated circuit, along with a few resistors.

Since the low power Schottky transistor-transistor logic (LS/TTL) and the complementary metal oxide semiconductor (CMOS) logic families recognize substantially different voltage levels corresponding to a 0 and a 1, a switch closure can produce a forcing condition (1 to an OR gate; 0 to a NAND gate) along both row and column lines of the matrix. The trick is to select the biasing resistors (R_R and R_C) so that the voltage divider, formed by a keypress, produces an LS/TTL 1 and a CMOS 0 output. With $R_R \doteq 2000\ \Omega$s and $R_C \doteq 680\ \Omega$s, the resulting 1.2 V represents a change to logic 1 at an LS/TTL OR gate input and a change to logic 0 at a CMOS NAND gate input.



A variety of gate configurations (AND with OR, NAND with NOR, and so forth) can be utilized; a few spare gates on a board can supply all the logic required for encoding. In the design shown, the no keypress output (lines A through D) is a hexidecimal 0. A keypress flag output (line KP) goes to logic 0 to signal any keypress.

Jeff Hurlburt is a graduate student at the University of Houston, working on his doctorate in education. His interests include microprocessor systems development and applications of computers to education of the gifted and talented. Mr Hurlburt has a BA in history from Rice University and an MA in special education from the University of Houston.

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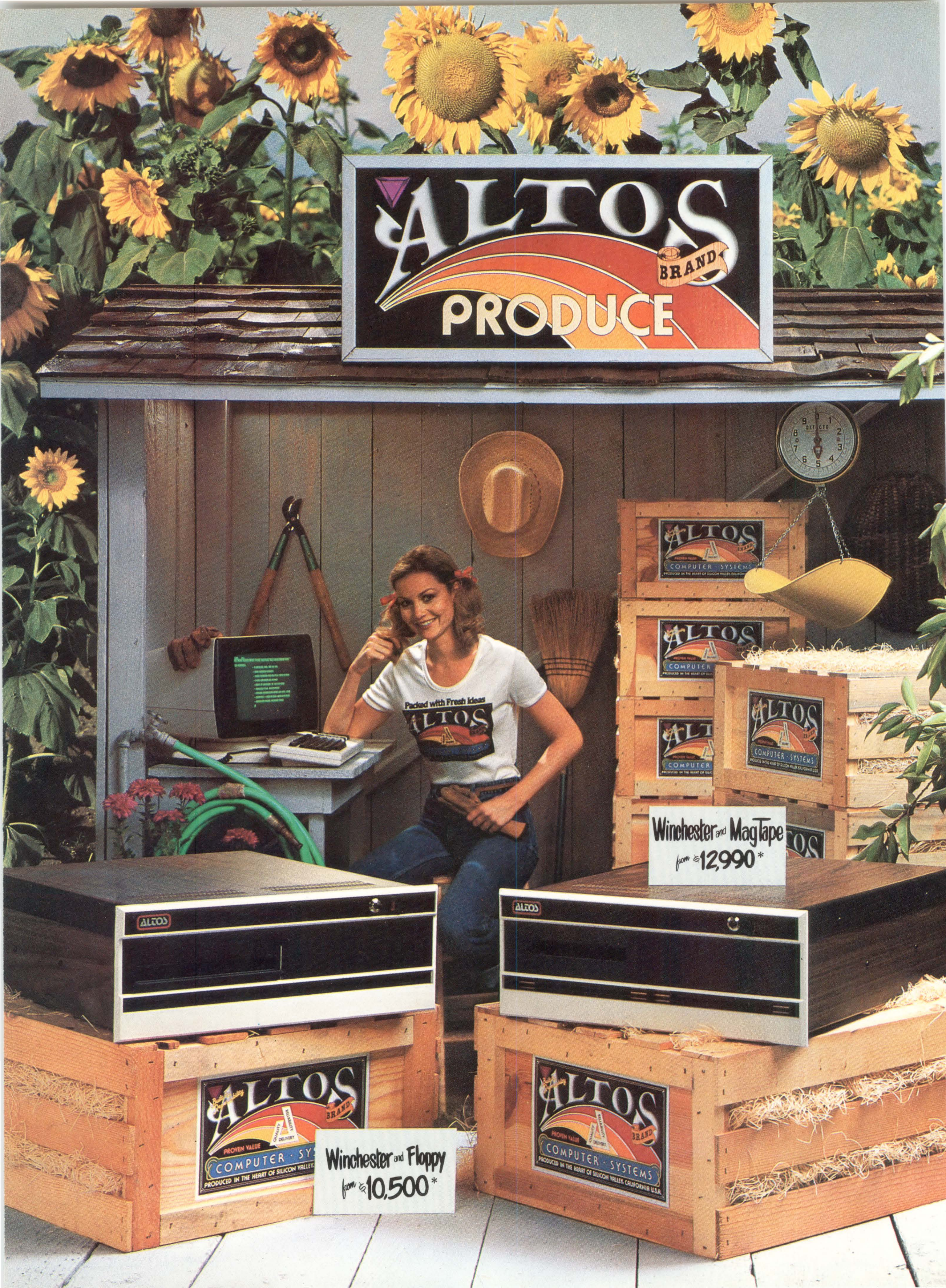
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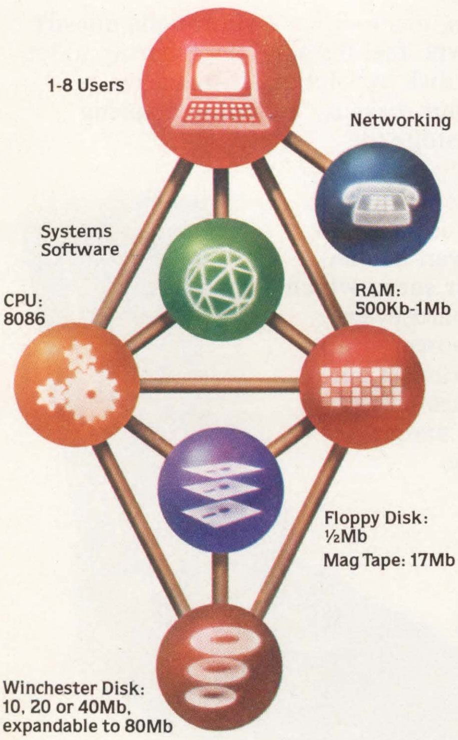

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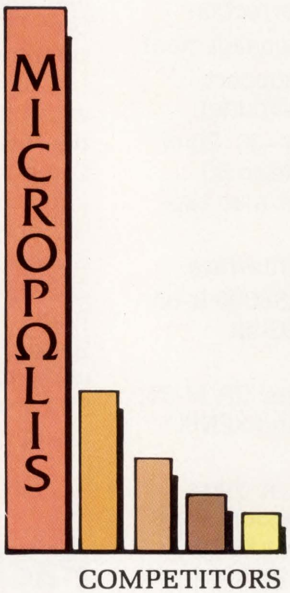


FACT: Critical components start out only in the clean room.

Recording heads, platters and voice coil positioner start out in the clean room and are never exposed to contaminated air. They're completely sealed in the lower half of the drive with pure air circulated through a 0.3 micron life-time filter. All active components are kept out of this sealed area, resulting in a clean area MTBF of 25,000 hours. Some manufacturers include active components in the sealed area, creating nightmares for field service.

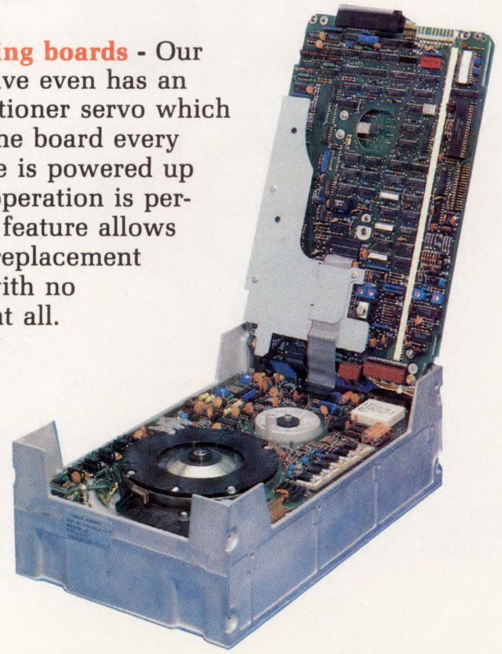
FACT: Micropolis drives are engineered for reliability, stability and performance.

We pay close attention to the clean area, but there's more. Designed in are features which make ours the most reliable, stable high performance 8" Winchester on the market.

- **Quartz locked direct drive motor** - A unique Quartz crystal speed control circuit holds rotational accuracy to better than 0.5%, which allows 5% more data on the drive. The high efficiency brushless dc motor eliminates two main shortcomings of line voltage induction motor/belt drives - excessive power and heat, and double inventorying for 50/60 Hz requirements.

- **Fail-safe braking mechanism** - Micropolis doesn't agree with those who feel it's good engineering to let the head slow the disk by friction. Instead, we extend the life of our disks by including a spring loaded brake that stops the motor in seconds.

- **Self-adjusting boards** - Our intelligent drive even has an adaptive positioner servo which recalibrates the board every time the drive is powered up or a restore operation is performed. This feature allows quick board replacement in the field with no adjustments at all.



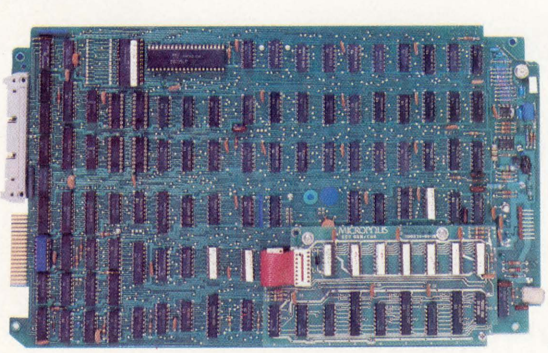
facts about 8-inch Winchesters

• **Truly balanced positioner** - A balanced rotary voice coil mechanism combines with a closed loop servo to continuously monitor head position, removing the danger of off-track writing inherent in stepping motor systems. Also, drives using non-rotary voice coils or stepper positioners are vulnerable to even very low levels of shock and vibration.

• **Latches and locks hold head in place** - Heads always land in the non-data area and are latched in a safe position even when the drive is moved from desk to desk. A special lock protects against higher shocks during shipping and is unlocked manually for installation.

FACT: Micropolis' optional Intelligent Controller can save you time and money.

Why spend valuable development time and money designing a controller from scratch when we've already done it for you. Our Intelligent Controller board fits inside the drive, gives you 922 Kbyte data transfer rate, sophisticated EPM data separation, up to 1 Kbyte of buffering and 5 bits of error correction.



Even with all of this, the controller costs less than $400 in OEM quantities. As a further economy, each master drive with Intelligent Controller can handle up to three additional slave drives. Drive interfaces are also available for SMD, ANSI and SA 1000.

FACT: Militarized computers use our drive.

Thanks to our inherent reliability, customers such as Rolm Computer and Miltope Corporation buy Micropolis drives for their militarized computer systems. Solid, rugged construction means long life and low maintenance costs in your less hostile environment.

FACT: On the horizon, 90 and 180 Mbyte 8" Winchesters.

We're at 45Mbytes and climbing. We plan to introduce three more 8" models by the end of 1982 with storage capacities of 60Mbyte, 90Mybte and 180Mbyte. The new models will help maintain our leadership position in the high capacity, high performance over-30Mbyte market.

If a solidly engineered high performance 8" Winchester plays a role in your design plans, phone or write for more "plain facts".

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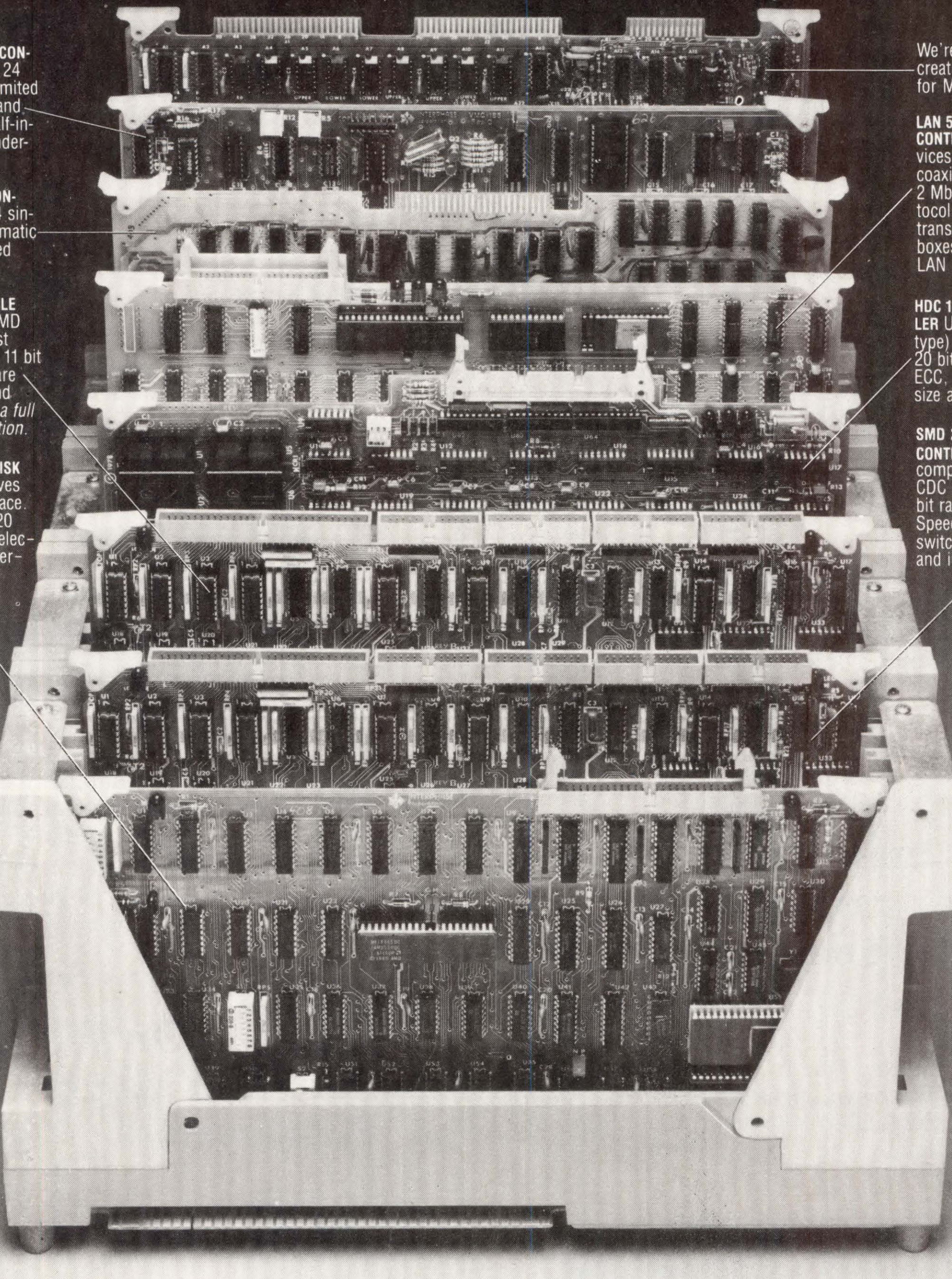

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Entire rigid disk controller family is software interchangeable. Automatic completion of simple multisector commands, automatic recovery from errors, bad track mapping, full sector buffering, extensive diagnostic reporting. Variable burst DMA in 8 or 16 bit systems. Software drivers and disk subsystems also available.

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Our "molded-in" technology produces complete one-piece jumpers without the electrical and mechanical problems associated with conventional "crimped-on" IDC assemblies.

We make it easy to choose the right connector by providing technical and design support and a wide variety of industry-compatible, UL-recognized terminations (Socket, Card-edge, PCB, DIP, D-Sub Min, DRB and Dual Row Plug), as well as headers in gold and non-gold contact options.

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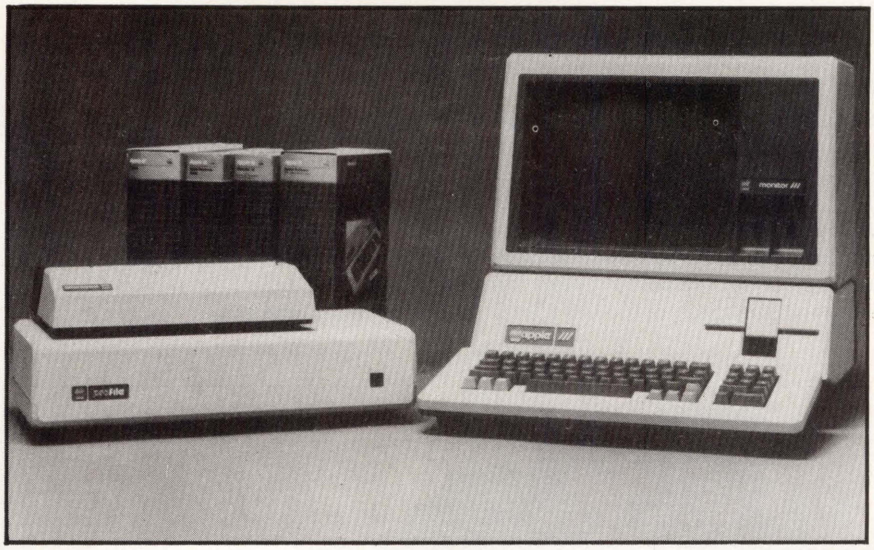
Upgraded Apple III offers expanded mass storage capability, professional application programs



A more powerful version of the Apple III personal computer features an improved operating system, expanded storage capability, and 7 new or enhanced software packages, at lower cost. In addition, this version of the Apple III supports up to 256k bytes of internal memory. Each computer is supplied with a set of system software diskettes that contain the Sophisticated Operating System (SOS 1.1), utilities file and device maintenance formatting software, and emulation mode software. This software supports up to 256k bytes of internal memory, uses no additional I/O slots, has a disk switch detect feature that protects against writing data on an incorrect disk, supports the RS-232 protocol, and provides an enhanced emulation mode that allows almost all Apple II software to run on the Apple III.

Expanded storage capability is provided by the Apple III/ProFile personal mass storage system. Designed to be integrated into Apple III systems, ProFile is a complete, self-contained unit featuring an intelligent controller, 5.25" Winchester drive, power supply, interface card, and driver software. The system accesses data 10 times faster than conventional floppy disk drives and increases the Apple III's online storage capacity to 5M bytes. Its 4 disk surfaces, 2 read/write heads, and actuator mechanism are integrated in a sealed, protected unit. To ensure data integrity, the intelligent controller automatically scans for errors and relocates marginal data blocks elsewhere on the disk. Housed in a 4.39" x 17.28" x 8.81" (1.15- x 43.89- x 22.38-cm) cabinet, the system can be used with any Apple III with 128k bytes of RAM and SOS 1.1

Seven new or enhanced application programs are available for the computer. The command oriented Business Graphics III program allows users to determine the min, max, sum, mean, std deviation, and variance when performing statistical analysis, and to project data trends through a variety of comparison methods. Written in Pascal, the program can load, plot, and analyze data from VisiCalc™, BASIC, and Pascal text files. The VisiCalc III program operates like an electronic worksheet, allowing the user to enter alphabetic or numeric information in row and column format. It features 17 new commands and operations, including edit, which allows the user to change formulas without rewriting; if, which enables the user to make decisions about what operations to perform; and choose, which allows table lookup. Boolean and mathematical functions have been added as well.

Apple Writer III is a word processing program that, used with the ProFile system, stores up to 1200 pages of copy. Included in the program are several sophisticated word processing functions such as a glossary, tab files, split screen, and a find-and-replace feature that locates and replaces words throughout the copy. The program also features formatting capabilities, such as paragraph and column tabulation, underlining, and automatic print formatting. Its Word Processing Language contains std Apple Writer III commands and allows the user to generate form letters and handle other repetitious tasks. With this program, users can transfer, copy, or delete blocks of text; chain files together; and transfer Apple II Apple Writer and Pascal files into Apple Writer III format. The program works with Apple II Mail List Manager files and can integrate VisiCalc III files into reports or documents.

The Business BASIC language for the Apple III features 2 new reserved words that facilitate formatting and printing. Several utilities have been added, including renumber and merge. Manuals and documentation have been rewritten and redesigned to emphasize ease of use and quick reference. Apple III Pascal, a new version of UCSD Pascal, includes a text editor, assembler, and a command processor that assigns only the graphics space required for each application. The language provides a software development package with an effective programming structure and many data options.

A print formatting program, Script III, takes any text written using the Pascal editor and formats it for hardcopy printouts. The program allows the user to designate line spacing, margins, page breaks, and text justifications when developing new programs; it highlights and underlines key words or phrases and paginates using headers and footers. The program works with a wide variety of Apple III compatible dot matrix and char printers, allowing the user to selectively print any portion of text and to chain files together for uninterrupted printing.

Access III general purpose communications software transforms the Apple III into a terminal that communicates with a variety of computers and timesharing systems. The software is virtually universal, facilitating microcomputer user to user and user to mainframe database communications. Users can transfer files to and from other Apple systems as well as larger computers, and can edit text on the Apple III without tying up timesharing phone lines. The program is compatible with either Apple III Pascal or Apple Business BASIC. Mail List Manager program will be available in the future for maintaining mailing lists and printing labels using an Apple III/ProFile system.

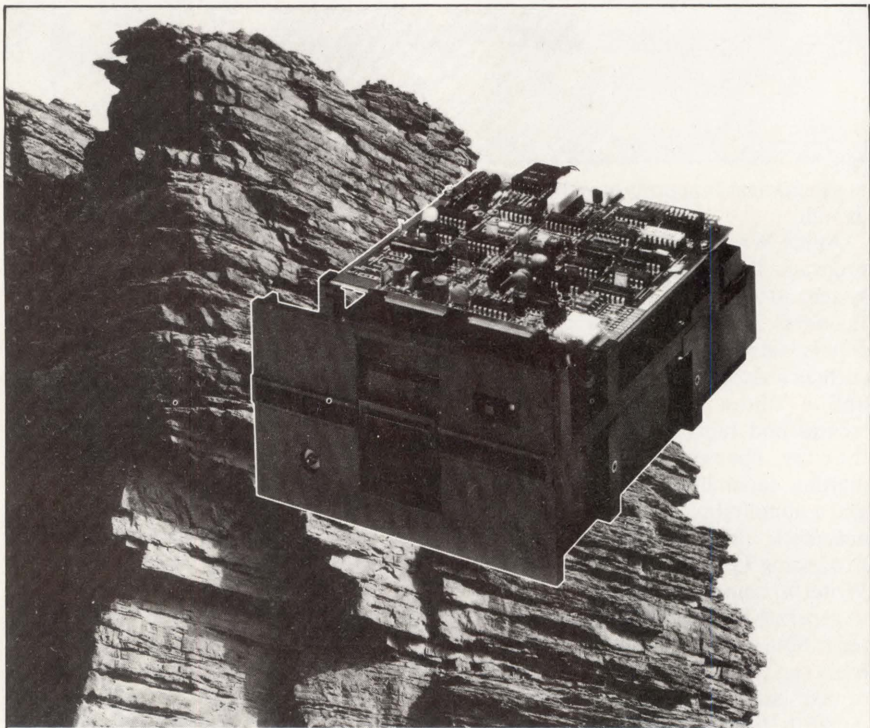
The computer supports up to 256k bytes of internal memory using 64k-byte RAMs that provide more information storage with lower power consumption. This additional memory also enables users to run larger, more sophisticated programs than previously possible. The memory enhancement is available as an upgrade kit to present owners of Apple IIIs with 128k bytes of RAM. It will be offered as a system option early in 1982.

A new Apple III with 128k bytes of memory and SOS software is priced at $3495. The complete system, with Business BASIC, VisiCalc, SOS, and Monitor III video display, is $4190. The min configuration required to operate the ProFile mass storage system includes 128k bytes of RAM, SOS 1.1 operating system, and utilities. Price of the Apple III/ProFile system is $6994. **Apple Computer Inc,** 10260 Bandley Dr, Cupertino, CA 95014. Circle 265 on Inquiry Card

MIL-STD-883B version of MC68000 processor

MC68000 16-bit processor with internal 32-bit architecture is available with full MIL-STD-883B processing. The unit offers seventeen 32-bit data address registers in addition to a 32-bit program counter and a 16-bit status register. With memory mapped I/O, the 16M-byte direct addressing range is the largest available in a 16-bit microprocessor. The processor is available in either a 64-pin hermetic side-brazed ceramic DIP or the JEDEC type C, 68-terminal leadless chip carrier. **Motorola Inc, MOS Integrated Circuits Group,** 3501 Ed Bluestein Blvd, Austin, TX 78721.

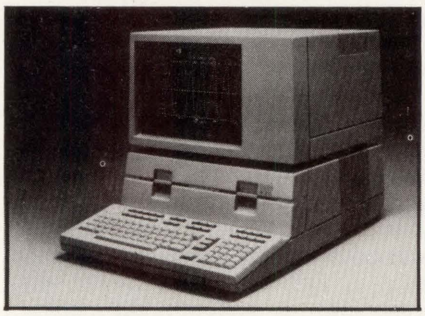
Circle 266 on Inquiry Card



Desktop computer for engineering and test applications

HP 9836A desktop computer enables the user to gather, interpret, and graphically display data, increasing the range of computer aided engineering and test application possibilities. Based on an 8-MHz Motorola MC68000 processor with 32-bit data and address registers, the computer is similar in construction to the HP 9826A. It includes a larger [12" (30-cm)] CRT screen, two 5.25" flexible disk drives, plus extended alphanumerics and graphics capabilities. Display enhancements include underlining, inverse video, blinking, and a half-bright and half-shifted dot scheme that improves character legibility.

Six new options are available for the system. The optional HP std Pascal language package includes documentation supporting the use of Pascal and Motorola MC68000 assembly language source code, and 4 mini disks containing the system software. A complete debugging package and a disassembler are included as well. The VisiCalc™ electronic worksheet is also available. It is used as a computational recalculation tool. As variables are changed on the worksheet, the software stores, retrieves, and recalculates the results; it can also print out those results on various HP-IB external printers. The HP 98627A interface card is available to support a color or monochromatic external monitor for graphic display. Consisting of a PCB and a battery, a powerfail protection option enables the system to ride out momentary glitches in line power that are transparent to the user. It also generates an interrupt to the user's program if power stays down for more than a few cycles. The HP 98256A 256k-byte RAM card uses 64k-byte RAM chips to provide up to 2M bytes of read/write memory. Optional data communications capabilities provide the same asynchronous data communications and HP data link capabilities as those available on the HP 9826A. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.



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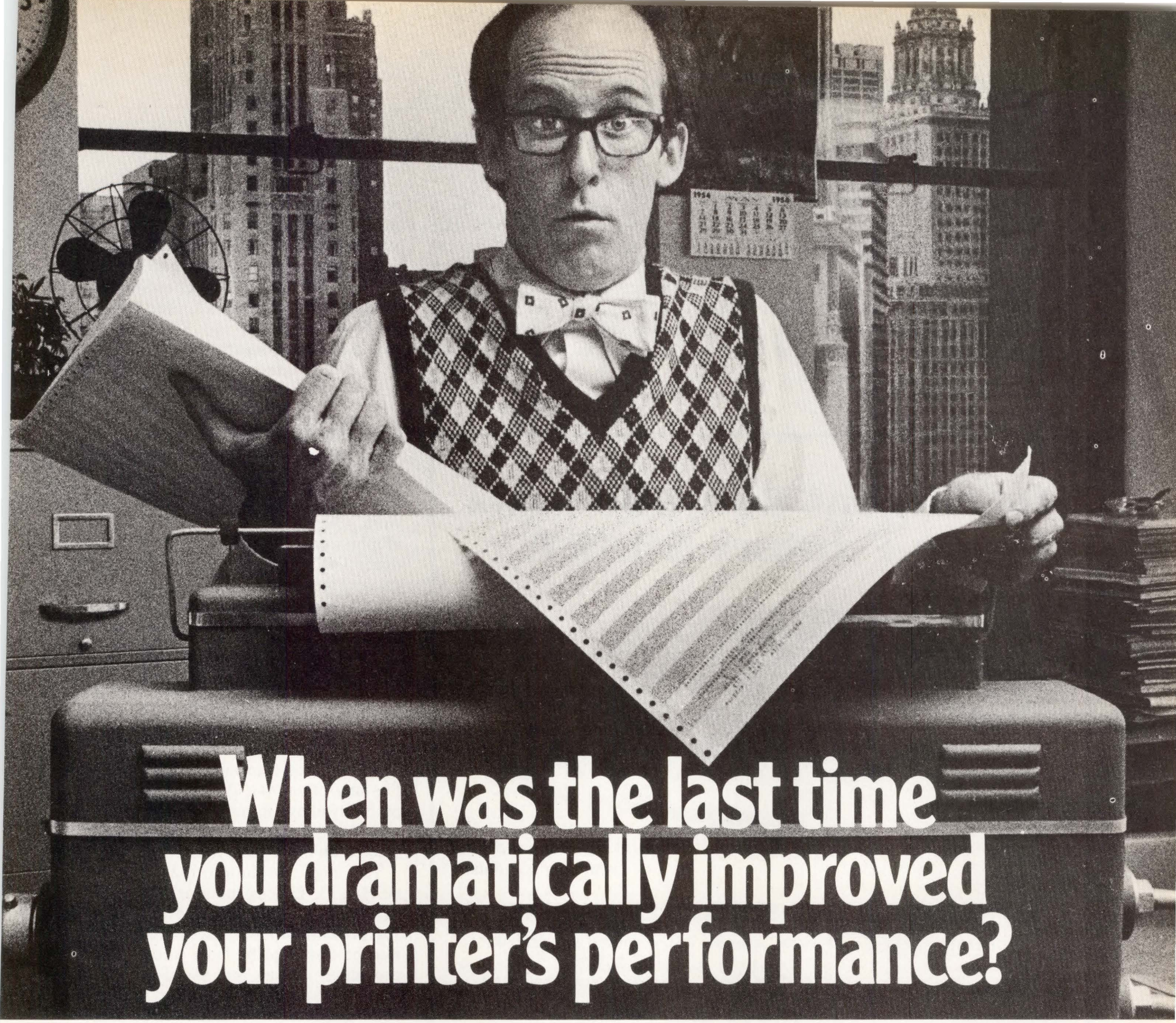
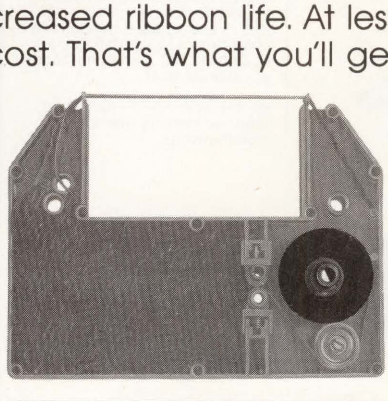


Today's measure of a printer's performance goes beyond line speed and purchase price. The true test is print quality and cost-per-character operating expense. Porelon ink rolls, designed specifically for impact printer ribbon cartridges, will dramatically improve the number of quality impressions and greatly increase the life of every ribbon.

Better impressions, increased ribbon life. At less cost. That's what you'll get every time you design a ribbon cartridge featuring Porelon ink rolls.

Find out how simple it is to add this performance feature to your impact printers. For further information, call 615/432-4134, or write: Porelon, Inc., 1480 Gould Drive, Cookeville, Tennessee 38501.



PORELON

YOUR LAST IMPRESSION IS WHERE WE BEGIN

CIRCLE 100 ON INQUIRY CARD

Desktop microcomputer system

Based on the Motorola MC68000, the Fortune 32:16 features an operating system derived from Bell Laboratories' UNIX™ system and has a full range of business application software packages including general accounting and distribution, forecasting, budgeting, and financial modeling. The basic system includes a 32-bit microprocessor with a 16-bit data path; expandable memory (128k to 1M bytes); a 1M-byte, 5.25″ floppy disk drive; keyboard; and 12″ (30-cm) video display. A Winchester disk drive, with optional 5M, 10M, or 20M bytes of storage, is available. The system supports BASIC, COBOL, FORTRAN, Pascal, and C. Its single-user configuration is expandable to a multi-user, timeshared system that can be networked using Xerox's Ethernet. **Fortune Systems Corp,** 1501 Industrial Rd, San Carlos, CA 94070.

Circle 268 on Inquiry Card

Color business graphics system added to local network system

Designed for use with the Attached Resource Computer® (ARC) local network, the turnkey 9680 color business graphics system allows network users to dynamically create, display, print, and photograph color graphic images. The system incorporates a high resolution (512 x 482) raster display monitor, a graphic input tablet with stylus, and a system controller. Graphics information can be input to the system via either the tablet and stylus or the system processor keyboard. Since graphics information is stored in the company's std disk file format, it can be transmitted and handled like any other ARC file. This file compatibility allows input from existing data and text files or from information created on other 9680 systems.

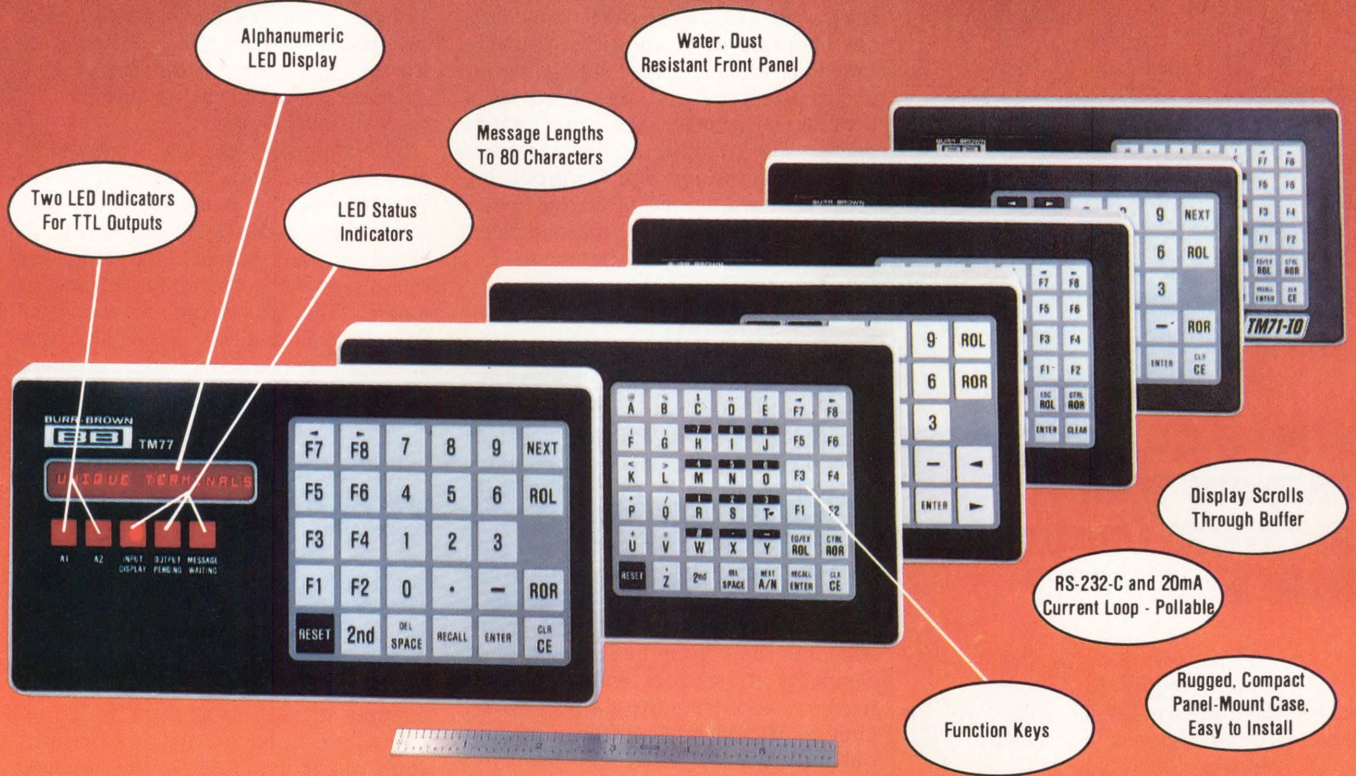
The high resolution (525 lines at 60 Hz), 13″ (33-cm) monitor can be used to retrieve a series of images from disk for presentation purposes. Images can also be displayed by large screen image projection devices and saved on video cassette recorders, allowing realtime color graphics presentations to be made for large audiences. Interfaces for various system components and peripherals, as well as the ARC local network, are provided through a system controller that incorporates a Z80A microprocessor with control memory and frame buffer storage memory. The controller accepts input from the graphics tablet and system processor and displays it on the color monitor. System commands can be invoked through the processor keyboard or by specifying functions through the use of "light keys" that can be overlaid on the monitor screen. Light keys are selectable using the tablet and stylus, and are used by the operator to create the separate picture components that combine to form a complete picture.

The operator is supplied with a 16-color palette from which the picture can be created. Also included in the light keys is a group of controls that allows the operator to adjust these palette

(continued on page 190)

SIX TOUGH TERMINALS

From $290*



Model	Alpha Display Characters	Baud Rate	Data Buffers	Keyboard	Function Keys(2)	Features	Supply Voltage
TM71	16	110-19200	320 Characters(1)	Alpha	14	Full feature	+5VDC
TM77	16	110-19200	320 Characters(1)	Numeric	14	Larger keys	+5VDC
TM71-I/O	16	110-19200	320 Characters(1)	Alpha	14	TTL I/O	+5VDC
TM77-I/O	16	110-19200	320 Characters(1)	Numeric	14	TTL I/O, larger keys	+5VDC
TM70	12	300 & 1200	36 Characters	Alpha	8	Low cost	+5VDC
TM76	12	300 & 1200	36 Characters	Numeric	8	Larger keys	+5VDC

1) Two 80-character input buffers - two 80-character output buffers.
2) User programmed.

MICROTERMINALS: The practical, easy to install, simple to operate answer for real world data entry/display: priced for OEM designs; tough, waterproof for factory floor work; pretty enough to enhance control consoles; so versatile they can often replace fragile CRT's and printers. If your man/machine communications are complex - or simple - and limited in volume, one of these compact (8.5″ x 4.5″ x 0.6″) terminals may be ready to talk to you...but talk to us first!

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D-1

CIRCLE 107 ON INQUIRY CARD

colors for their blue, red, and green components, as well as for hue, brightness, and saturation. More than 16M color choices are available; a max of 16 colors can be displayed at one time. Software functions include draw, chart, script, playback, library, and output. Optional peripherals include a color dot matrix printer and 2 models of film recorders capable of exposing film for producing slides and prints, 8 x 10 Polaroid[R] color prints, and 8 x 10 color transparencies. **Datapoint Corp**, 9725 Datapoint Dr, San Antonio, TX 78284.

Circle 269 on Inquiry Card

1M-byte memory mapping capability

TM990/102 single-board computer features 128k-bytes onboard memory with extended addressing memory mapped to 1M byte. The CPU includes power-up reset logic to delay a reset until power stabilizes after switch-on, and load after reset logic to automatically branch to the load vector and boot software. Module supports up to 16 prioritized interrupts from the system bus and capability to support onboard prioritized interrupt from the EIA port driver. Unit is offered in 3 versions—without onboard dynamic RAM, with 64k-bytes RAM, and with 128k-bytes RAM. Onboard RAM runs with zero wait states when accessed by the processor. All 3 versions can address up to 16k bytes of onboard EPROM. TM990/404 monitor is available to support debugging in extended addressing mode and is capable of expanding the command table by using the monitor's command scanner. **Texas Instruments Inc**, PO Box 202129, Dallas, TX 75220.

Circle 270 on Inquiry Card

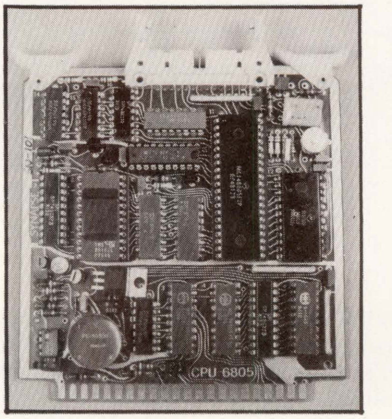
Single-board computer offered for battery based operation

CPU-6805 CMOS single-board computer is based on the 146805E2 CMOS CPU and designed specifically for battery based operation. The 4.5" x 5.25" (11.4- x 13.34-cm) board contains 1k byte of RAM, 8 lines of digital I/O, 8 analog inputs, a power switched EPROM, a realtime clock, and a switching voltage regulator. It has full C-44 bus compatibility using high speed CMOS buffer chips to access up to 128 offboard ports and 32k of offboard memory.

A powerful, controller oriented CMOS microcomputer with onboard RAM and ports, the computer's 146805E2 CPU uses a multiplexed data and address bus, making it compatible with National Semiconductor's NSC-810 and -831. A total of 1186 bytes of RAM are available on the board, including 1024 bytes in a pair of 6514s, 112 bytes in the CPU, and 50 bytes in the realtime clock. A power switched 2716 EPROM is used for program storage, giving the advantage of zero quiescent power from an inexpensive, readily available part.

The computer has 2 low power modes derived from the wait and stop modes of the CPU. In the wait mode, the processor's bus accesses are halted, but its clock is maintained, reducing the board's power consumption to approx 6 mW. The board can be awakened from the wait mode by an interrupt from its timer, an external interrupt, or a reset. A stop instruction causes the CPU to stop its oscillator; a circuit on the board senses the stopped oscillator and reduces the board's supply voltage to approx 2.8 V. In this mode, the board's power consumption is typically less than 0.5 mW. The stop mode is exited when either an external interrupt or a reset is applied. Recovery from the stop mode typically takes 5 ms.

The 146818 realtime clock used on the board can be programmed to provide interrupts at intervals as short as 3.2 ms, or as long as once a day. These interrupts can be used to wake the computer from its low power modes. **Synapse Corp**, 199 Main St, N Falmouth, MA 02556.



Circle 271 on Inquiry Card

High end version of PD?-11/23 microcomputer addresses up to 1M byte of memory

PDP-11/23 PLUS, a high end version of the PDP-11/23 microcomputer with up to 1M byte of memory, features memory expansion capabilities not available in the std PDP-11/23 packaged processor, as well as extended addressing. Fully software compatible with PDP-11 midrange minicomputers, the processor features parity memory, an extended version of the LSI-11 bus, and 7 expansion slots for adding modules. The parity memories employ 64k chips for higher memory density per board and are offered in 256k- and 512k-byte versions.

The 5.25" high processor fits in a std 19" (48-cm) industrial rack and includes a CPU module that contains the microprocessor chips, clock, bootstrap, diagnostics, and 2 serial line units. Options include floating point microcode and commercial instruction set chips. The system also accommodates the FPF-11 hot floating point option that provides 17-digit accuracy and 6 times the speed of the floating point chip option alone.

Two basic configurations are available. The entry level configuration has twin 10.4M-byte disk cartridge drives, a VT-100 family terminal, RSX-11M operating system software, and a processor with 256k bytes of memory. A second configuration has dual 10.4M-byte drives, a VT-100 family terminal, RSX-11M+ operating system software, and a processor with 512k bytes of memory. Prices for the processor start at $8500. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 272 on Inquiry Card

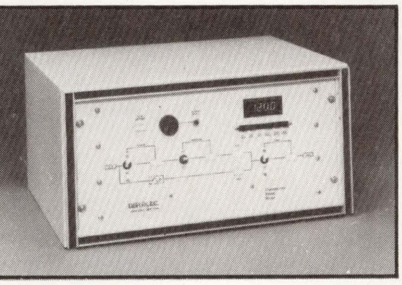
Multi-user, multitasking microcomputer system

A 32M-byte Winchester disk system that supports up to 5 workstations, 5032 MultiShare microcomputer system features a 6-MHz Z80B processor that speeds processing time by 15% to 20% over a 4-MHz system, and an extended version of the CP/M operating system. RAM memory is expanded to 128k, providing 56k per terminal for user applications. Basic system hardware includes a video console and keyboard, Megastor chassis with independent power supply, 8" Winchester hard disk drive, and a 630k-byte floppy disk. Both the hard and floppy disks utilize the company's dual-mode disk controller with automatic error detection and correction. Full system backup is available with an optional 4-track, 15M-byte cartridge tape drive. With the system's timesharing capabilities, different applications can be performed simultaneously by up to 5 operators at locations up to 100' (30 m) from the central processor. Two printers can be supported and operated simultaneously. In addition to extended CP/M, std software includes Microsoft BASIC, SCOPE editor, and ZSM assembler. **Vector Graphic, Inc,** 500 N Ventu Park Rd, Thousand Oaks, CA 91320.

Circle 273 on Inquiry Card

POWER SOURCES & PROTECTION

Switch mode line protectors provide ac power line protection



First in a series of lightweight, low cost "switch mode" line protectors, models DLP-8 and -12 combination line conditioners and uninterruptible power systems provide complete protection from all problems associated with ac power lines, including noise brownouts and full blackouts. Designed for use with small computer systems, DLP-8 and -12 handle computer ac load requirements up to 1 kVA and 1.5 kVA, respectively. All power conversion and control functions are carried out at frequencies higher than the 50/60-Hz line frequencies, eliminating line frequency magnetic chokes and transformers.

Both units are equipped with integral, built-in sealed batteries capable of 5-minute operation minimum at full power in the event of a complete power failure. Second versions of both units are available with built-in batteries for a minimum operation of 1 hour. The line protectors operate from a wide range of input voltages and frequencies. Either unit can be user selected for a center voltage of 115 or 230 Vac, and proper 1-line operation will occur as long as power line voltage stays within 30% to -20% of this level. Line frequency can be from 25 to 500 Hz.

Output voltage and frequency can be factory set to any std level. Frequency is maintained to better than 1% and voltage is regulated to ±5% over the full output range, with load power factors

(continued on page 193)

MANY PEOPLE THINK OF PENRIL AS THE HIGH PERFORMANCE DATA COMMUNICATIONS COMPANY

MAYBE that's because Penril's 2400, 4800 and 9600 bps modems include centralized diagnostic control. So your high speed network has fault isolation and diagnosis without test equipment or a remote operator. Many of those diagnostic test functions are carried out on a separate diagnostic channel so network operation is not disturbed. Maybe it's our encryptor that gives you network security. Or maybe it's our statistical multiplexer that can concentrate up to 16 lines into one... at tremendous savings in lines and modems.

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Penril

Data Communications Division
5520 Randolph Road
Rockville, Maryland 20852-2681

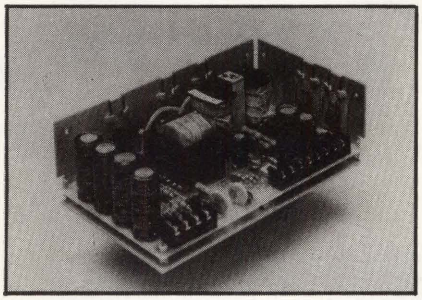
ranging from 0.5 leading to 0.5 lagging. Harmonic distortion is less than 5% for a linear load. A 200% overload can be supported for 1 full cycle, and a 150% overload for 10 s.

DLP-8 is normally supplied with a std 3-prong, 115-Vac plug, and draws less than 12 A from an ac line. DLP-12 requires up to 18 A and normally requires a special line outlet. Each unit requires 2 safe, sealed lead acid, 48-Vdc battery modules. The DLP-8 uses 12-lb (5-kg), 2.5-Ah modules and DLP-12 uses 25-lb (11-kg), 5.0-Ah modules. List prices are $2995 for the DLP-8 and $3995 for the DLP-12. Completely militarized units and custom designs are available. **Displex, Inc**, 21 Brewster St, Glen Cove, NY 11542.

Circle 274 on Inquiry Card

Open frame switching power supplies

Econoflex open frame switching power supplies are available in single- and triple-output models and meet UL and CSA requirements. The power supplies have dual inputs at 110 Vac ±20% and 220 Vac ±20%, 47 to 440 Hz, making them suitable for international equipment. Inrush current is limited to 15 A peak at 110 Vac and 30 A peak at 220 Vac. All outputs are fully regulated and floating, and incorporate short circuit and overload protection. All units carry a 1-year warranty and are isolation checked at 2500 Vrms and burned in for 24 h at full load. **Gould Inc, Instruments Div**, 35129 Curtis Blvd, Eastlake, OH 44094.



Circle 275 on Inquiry Card

Uninterruptible power source

UPS protects computers or word processors from brownouts, "noisy" power lines, and total power failures. Unit receives source power from the ac line, converts this power to 48 Vdc, and stores it in self-contained gel cells. The 48 Vdc from the storage cells is then converted back to a pure, regulated 110 Vac, 60 Hz source to run the computer or word processor. Commercial ac lines keep the storage cells fully charged, and the storage cells provide power to run the system. If commercial power sources drop below or rise above 110 Vac, the power cells maintain the proper level of power to the computer. In the case of a total, prolonged power failure, the UPS will provide at least 15 min of operating power at up to 5 A, so that the computer or word processor can be shut down in an orderly manner without loss of data. **General Interface Systems, Inc**, Hartz Plaza, Suite 358, 560 Hartz Ave, Danville, CA 94526.

Circle 276 on Inquiry Card

CIRCLE 111 ON INQUIRY CARD

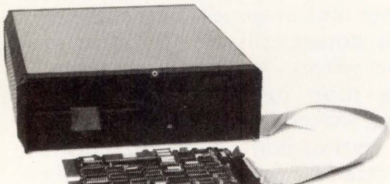
When You Need . . .

WINCHESTER DISK SYSTEMS

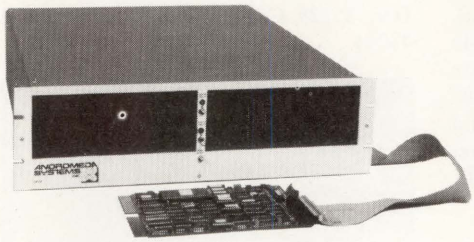
FOR THE Q-BUS

ADD-ON SUBSYSTEMS

MWDS



WDS



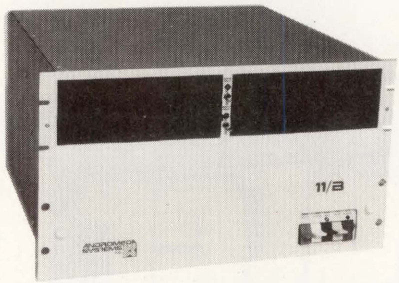
RPX60

5-1/4″ DISKS

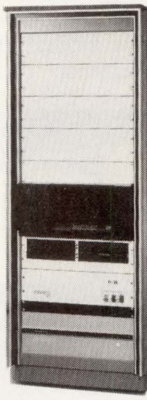
8″ DISKS

14″ DISKS

11/M-W



11/B-W



11/B-WTS

FULL TURNKEY COMPUTER SYSTEMS

. . . think of Andromeda

Andromeda Systems, Inc. offers the Q-Bus user a wide selection of Winchester disk based mass storage systems. Both add-on subsystems and full turnkey computer systems are available. Current storage capacities range from 2.5mb to 160mb. The Winchester disk controllers emulate DEC RK-05, RL-01/02, and RP-02/03 devices for compatibility with existing operating systems. Winchester disks in 5¼″, 8″ and 14″ formats are used to obtain the best possible performance in a variety of package sizes.

Back-up is to floppy disk or streaming magnetic tape. The 5¼″ and 8″ systems may be specified with an intregral floppy disk drive; these systems use the Andromeda WDC11 controller that includes an RX-02 emulating floppy disk controller on the same dual-width card. Also available for backup is a separate, high performance, non-emulating floppy disk controller, the DFDC11/DMDC11. This proprietary controller offers 25 to 61 percent more storage along with a data transfer rate 2.25 times faster than the RX-02.

We offer a complete line of Q-Bus based systems and other LSI-11 related products. For details, contact:

ANDROMEDA SYSTEMS INC.
9000 Eton Ave.
Canoga Park, Calif. 91304
Phone: 213/709-7600
TWX: (910) 494-1248

Graphic programming system aids implementation of graphics applications

Intelligent Graphics System (IGS) is an intensive graphic programming system that aids in the implementation of a wide variety of graphics applications. Its basic design is modeled after the proposed ACM Graphics Standards Planning Committee Core. The language allows users to generate, modify, store, and retrieve graphic data structures dynamically. These data may take the form of simple line drawings, bar charts, graphs, or complex interactive display sequences.

Users can design and generate color graphics displays using English language commands and coordinate systems that are relevant to their own application. Realtime displays can be designed for updating by live data from stripchart like moving displays, while static displays can pull data from disk files in the company's desktop systems. Such displays can be mixed in one application.

The language features 2 fundamental coordinate systems: the basic coordinate system including world coordinates, in which the picture for display is constructed; and the device coordinates in which data are displayed. Because of the device independent nature of the language, various color graphic displays and plotters can be used interchangeably as output devices although their resolutions may vary. In addition to flexible graphics output, the language also permits data input from several devices such as keyboards, digitizers, and lightpens.

Basic plotting capabilities include std graphic primitives, automatic labeling and scaling of grids and axes, bar charting, pie charts, multiple-curve plotting, realtime data, multiple char fonts, transformations (view port, world, rotate, zoom), and clipping. Char fonts can be displayed in any size, color, angle, and orientation. Language features include display procedure libraries, movement of displayed segments, pick and event handling with feedback, graphics data structure editing, and a simplified ASCII interface. The package runs on the company's 8000 series high resolution terminals and CP/M desktop computer systems. **Intelligent Systems Corp,** Intecolor Dr, 225 Technology Park/Atlanta, Norcross, Georgia 30092.

Circle 277 on Inquiry Card

Operating system

UNISYS, a version of Bell Laboratories' UNIX operating system, is available for the company's CTW-300 and CTS-300 series microcomputers. It can directly address up to 1.5M bytes of memory with no restrictions placed on program size, and supports 8 multitask/multi-user operations. The C language, featuring 64-bit floating point math, Pascal, ANSI std FORTRAN '77, and Assembly language programming capabilities are available. BASIC and COBOL will be available in early 1982. **Codata Systems Corp,** 285 N Wolfe Rd, Sunnyvale, CA 94086.

Circle 278 on Inquiry Card

 CIRCLE 113 ON INQUIRY CARD

CAD/CAM software package

Designer Logic™ package provides integrated circuit designers with schematic entry and connectivity extraction capabilities, extending the capabilities of the company's VLSI design system to include schematic documentation. It includes a user friendly interface, operating commands, and component libraries, as well as formattable outputs to logic simulators. The package allows the VLSI designer to automatically extract a connectivity list of all schematic information using simple commands to access the system data base. It provides formattable outputs to logic simulators including LOGCAP and TEGAS-5, two of the most commonly used simulators, eliminating the time-consuming task of manually transferring logic and circuit design information from the schematic to the simulator. The system features menus containing std commands and component symbols frequently used in the design and layout of VLSIs, and is priced at $15,000. **Applicon Inc,** 32 Second Ave, Burlington, MA 01803.
Circle 279 on Inquiry Card

Operating system on silicon

Silicon version of CP/M-86 operating system operates with Intel 8086 and 8088 microprocessors, allowing the designer to develop a diskless operating system with all the power of the disk based version of CP/M-86. The part is a complex, large scale IC containing 16k bytes of ROM plus timers and other logic. Since it does not require a disk, it is ideal for remote computers interconnected in a local distributed network sharing a large-capacity disk drive. The firmware CP/M-86 also allows the manufacture of smaller, less expensive systems. **Intel Corp,** 5200 NE Elam Young Pkwy, Hillsboro, Or 97123, and **Digital Research, Inc,** PO Box 579, Pacific Grove, CA 93950.
Circle 280 on Inquiry Card

Software package

RJE (+) Plus EDL software package is designed for distribution of host workload to remote IBM series/1s. Running in either 2780 or 3780 mode, the program supports reader and list queues, automatically routing jobs in the list queue to assigned printers of disk spool files. Data from 1 to 7 files can be transmitted to the host and merged with respective optional JCL. RJE station operator commands can be entered on the console. Printer carriage control tapes are supported via a control file. Programs include the RJE (+) Program and File Maintenance Utilities. **Carney Associates, Inc, Computer Consultants,** 3114A W Marshall St, Richmond, VA 23230.
Circle 281 on Inquiry Card

Graphics software

Offered for DEC's VAX 11/780 computer systems, DISSPLA 9.0 device independent software calls on a library of more than 700 FORTRAN subroutines to produce charts, graphs, 3-D diagrams, and highly flexible maps for business, scientific, government, education, and engineering applications. Features include a blanking system that gives users the ability to eliminate confusing and overlapping lines, sophisticated char generation and type selection for annotation of graphics presentations, and extensive mapping capabilities. In addition, a virtual storage system optimizes computer memory resources by storing data on the disk instead of in main memory. Standard interfaces are available for more than 60 output devices. **Integrated Software Systems Corp,** 4186 Sorrento Valley Blvd, San Diego, CA 92121.
Circle 282 on Inquiry Card

Disk buffering software for CP/M 2.2 systems

Cache/Q software enhances the speed of a CP/M system by up to 32 times by buffering transfers to and from the disk drives. It reduces the amount of disk activity required for any given application and is transparent to all user and system programs. No operating procedures need to be modified. The software can be installed in a CP/M 2.2 system with 64k bytes of memory or less, or can take advantage of additional bank-selected memory. It features an interactive installation program, a reconfiguration program through which a user can specify which files or class of files are to be buffered, and a display program that displays the operating statistics of the software. **Queue Computer Corp,** 75 Pelican Way, Unit F, San Rafael, CA 94901.
Circle 283 on Inquiry Card

It pays to keep your computer in tick-tock shape. And that's simple to do with our Timing Control Unit (TCU).

The TCU makes certain your computer always knows exactly what time it is—during power up, power down, or even in a brownout or blackout.

Rechargeable batteries, mounted right on the board, make the TCU immune to power failure of any sort. For as long as three months. And an on-board crystal-controlled oscillator ensures supreme accuracy at all times.

Digital Pathways' TCU clock-calendars observe the correct number of days for each month. Setting of time and date can be performed by a simple software routine. Some TCUs can be set to initiate an interrupt at a chosen date and time, or at specified intervals.

If you want to keep your computer on time, all the time, call or write us today at: Digital Pathways, 1060 East Meadow Circle, Palo Alto, CA 94303. Telephone (415) 493-5544. TWX 910-379-5034.

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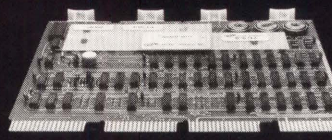
	TCU-150	*Lockheed SUE	TCU-200
*LSI-11/2 & 11/23	TCU-50D	*Naked Mini	TCU-310
*Multi-Bus	TCU-410	Any Model (RS-232/20mA)	SLC-1
*EXORcisor	TCU-68		



*PDP-11 and LSI-11 are registered trademarks of Digital Equipment Corp. Others listed are trademarks, respectively, of Intel Corp., Motorola, Inc., Hewlett-Packard, Lockheed Corp. and Computer Automation Inc.

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Circle 115 on inquiry card.

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Germany: (089) 60 60 71-72 Telex: 5216290 isio d • Switzerland: 022/310587 Telex 289191

RSX-11M compatible software for LSI-11 analog and digital interfaces

ADLIBRSX, a full library of subroutines compatible with DEC's RSX-11M multitasking, realtime operating system software, supports all of the company's analog and digital interfaces for the LSI-11 bus. It supports analog high level, low level, and thermocouple inputs, while achieving max throughput rate. The analog input routines allow the user to select sequential or random access channels, programmable gain amplifier settings, internal or external triggering, and other parameters. Digital inputs and outputs, realtime clock functions, pulse counting and generation, and the company's multiple interrupt controller are fully supported. Routines for analog and current loop outputs are also provided. The library also supports the company's analog I/O boards for the PDP-11 Unibus. Library subroutines are callable from FORTRAN, Pascal, and BASIC. I/O drivers for MACRO-11 programmers are also included. For systems with battery backed or core memory, provisions for power fail reset are included. The library is available on RX01 compatible floppy diskette, RL01 or RL02 compatible hard disk, and TU58 compatible tape cartridge. Both source and object codes are included. **ADAC Corp,** 70 Tower Office Pk, Woburn, MA 01801.
Circle 284 on Inquiry Card

Software graphics package

QPLOT graphics FORTRAN software package is designed for VAX systems and is plottable on any graphics device that can draw a vector. User needs only one graphics language, and can direct output to several graphics devices by varying a single parameter. Program can output to an intermediate plot file during application program execution, and then can be redirected to one or more graphics devices without reexecution of the application program. Routines are provided for 2-D rectangular and polar plotting, 3-D rectangular plotting with hidden line removal, flowcharting, mapping, and typesetting. **QTECH Assocs,** PO Box 952, Old Lyme, CT 06371.
Circle 285 on Inquiry Card

Line editor

Command line editor (CLE) permits rapid correction of interactive commands, customizes terminal keys, creates one-button commands, and keeps a log file of all commands issued. Issued commands are corrected in 3 steps. First, one button is pushed to back up to any previously issued command. Editing is done with a keypad editor. Pressing "return" resubmits the corrected line. To define terminal keys, one key is pushed. The user then types a text string, a DCL command, or a built-in function. Table driven software automatically assigns a help text to that key, as well as defining the one-button command. Commands can be assigned interactively, or to remain each time the user logs in. At the operator's option, a record is kept of every line issued as a command; each logged command also contains the date and time the command was issued. The editor runs on VAX/VMS systems with VT100, VT52, or hardcopy terminals. **Rubel Software, Div of Andrew Rubel & Assocs, Inc,** One Soldiers Field Park 605, Boston, MA 02163.
Circle 286 on Inquiry Card

CIRCLE 116 ON INQUIRY CARD

Interactive logic simulation program

Designed for simulation of MOS/LSI logic, ILOGS accurately models operating characteristics unique to MOS ICs. It can also simulate conventional logic elements, as well as RAMs, ROMs, and PLAs. The program features interactive program control, 9 logic states providing true wired OR logic, free-format data input/description, nested macros, extensive error checking, user definable macro library, and built-in PLA models. Capabilities include initial state verification, network timing simulation, spike detection, and delay path checking. **Circuit Simulation Sciences,** 2970 Fruitdale Ave, Suite C, San Jose, CA 95128.

Circle 287 on Inquiry Card

Operating systems

MultI/OS and I/OS operating systems provide users of Radio Shack TRS-80 model II with CP/M compatibility and other functions. MultI/OS for the model II allows 2 or 3 users with added memory of 64k, 128k, or 196k bytes in the system. A hard disk can be added for up to 40M bytes with 63,000 files allowed. Features include 5 additional user programmable function keys, auto start capability, the ability to disable user abort sequences, symbolic debugger, text editor, directory status, disk copy and file transfer programs, disk and memory diagnostics, and a printout formatting facility. MultI/OS and I/OS support up to 15 disk units and allow the mixing of 5" and 8" (13- and 20-cm) floppy and hard disks. MultI/OS allows up to 16 tasks simultaneously, any of which can run with a physical terminal or as a background job. It provides for multiple printers with automatic spooling, record lock using FMM, 48k bytes/user, and a full range of languages. The compatibility factor allows the user access to the vast amount of currently available application packages. **InfoSoft Systems Inc,** 25 Sylvan Rd S, Westport, CT 06880.

Circle 288 on Inquiry Card

BIOS conversion program

Allowing Xerox 820 to interface with virtually any communication and peripheral device, Samson program approximately triples the 820's disk reading speed. Features include keyboard setup of all hardware interface ports from the console, keyboard adjustable interconnection of peripheral devices to SAM hardware, alphabetical directory with file size indications for disk management, and a terminal program to operate SAM as a timeshare terminal. Samson allows either of 2 serial ports to be configured to run at any of the std baud rates, char lengths, parity options, or stop bits for a variety of peripherals. Two serial printers can be installed on a single 820 and selected from the console. Programs can be run automatically on system boot to allow turnkey systems to be easily built. The program makes the COMM port available to generic applications programs like Courier; it can also be used for a second printer or other peripheral. In addition, the 820 can be used as a terminal for either connection to the Source or other timesharing networks. **The Software Establishment,** 705A Lakefield Rd, Westlake Village, CA 91361.

Circle 289 on Inquiry Card

A new high resolution hard copier for DVST* displays.

Honeywell's newest member of its VGR 4000 family of video graphics recorders produces fast, clear, easy-to-read hard copy records of anything your DVST display can present.

That's because our new VGR 4000 graphics recorder for DVSTs utilizes a high resolution format with 2000 x 2000 sample points, independent of display size. And delivers a sharp looking record on dry silver paper in only 14 seconds.

You can choose from two sizes of picture formats that are switch-selectable with no board changes or complex adjustments. You can also select black-on-white or white-on-black pictures, simply by flipping a front-panel switch.

With the multiplex option, you can even mix 11-inch and 19-inch display sizes without adjustments. An optional built-in test pattern generator aids troubleshooting and verifies proper unit operation.

Arrange for a free demonstration. See for yourself what we can accomplish together. Call Durke Johnson today at (303) 773-4818. Or write for free detailed information and a sample record:

Honeywell Test Instruments Division
P.O. Box 5227
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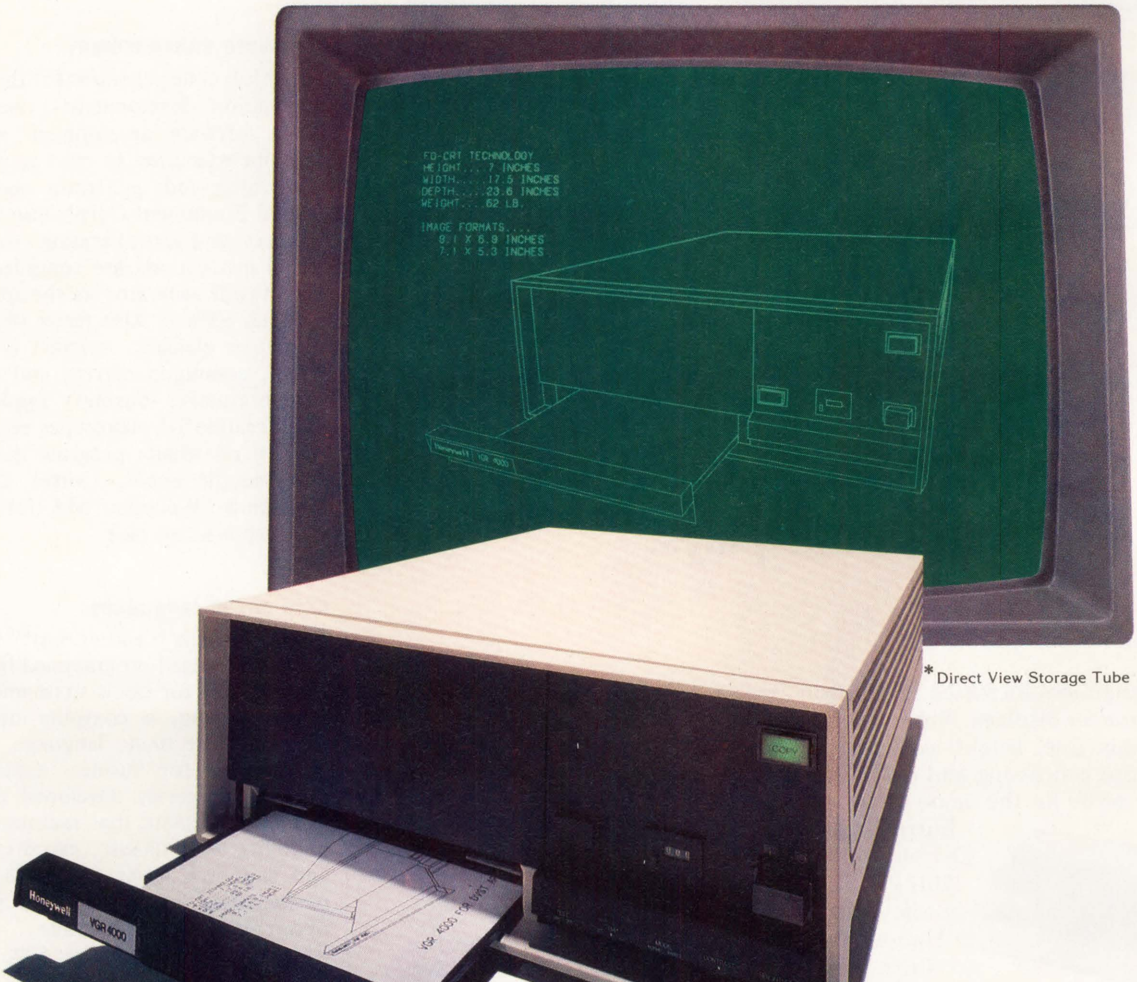


*Direct View Storage Tube

Honeywell

CIRCLE 90 ON INQUIRY CARD

Networking software

Designed as an alternative to DECNET, the CALL-11 software package is run by the user at any terminal connected to the host system. A std communication port is used to call up a second computer over ordinary business telephone lines with an existing modem or acoustic coupler. In addition, communication between 2 local computers can be achieved by a simple cable, making a direct connection between a std terminal port on each computer. Files of any type, including binary program files together with their file attributes, can be transferred in either direction between two computers. The package also does wildcard transfers with a file name inspection latch. The software need only reside on the computer that initiates the connection, freeing the user from a limited network of computers and eliminating the high cost of a license for each correspondent computer together with the cost of special hardware. The software requires no system generation. It is currently implemented on the DEC PDP-11 and VAX series of computers under the RSTS and VMS operating systems. The correspondent system may be a computer other than a VAX or PDP-11. **Clyde Digital Systems, Div of Clyde Enterprises, Inc,** PO Box 348, Bedford, MA 01730.

Circle 290 on Inquiry Card

Software enhancement

An object code generator for the INFORM application development system combines software development with fast machine execution to cut running time. The object code generator operates on Digital Equipment Corp's PDP-11s under RSX, IAS, and VMS operating systems. Internal instructions are compiled by the object code generator for the application and run 60% to 90% faster than its interpretive element. INFORM is English based, command driven, and designed for interactive business applications. The creation of prototypes enables the user to reevaluate program design and suit specific needs. **Cortex Corp,** 55 William St, Wellesley, MA 02181.

Circle 291 on Inquiry Card

CP/M based languages

CBASIC™, CB80™ and PL/1-80™ DEC formatted packaged programmed languages are available for DEC's VT180 microcomputer. CBASIC, a compiler-interpreter dialect of the BASIC language, is most widely used for business applications. CB80 is a recently developed compiler version of CBASIC that maintains compatibility with CBASIC, executes faster, and supports MP/M. PL/1-80 is an implementation of subset G of the PL/1 programming language. **Digital Research Inc,** PO Box 579, Pacific Grove, CA 93950.

Circle 292 on Inquiry Card

Coming Next Month: Designer Preference Survey on Microprocessors, ICs, and Modules

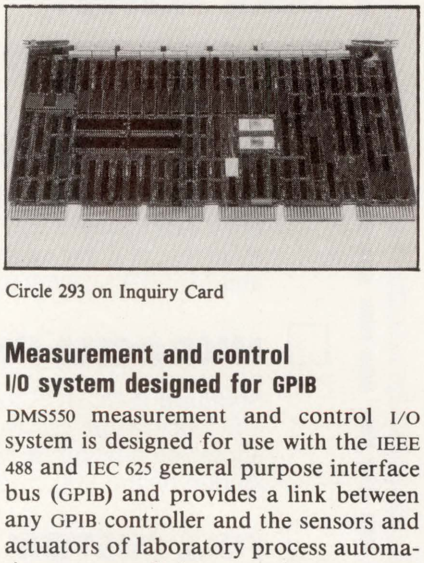
Controller interfaces combined 80M and 160M-byte drives to PDP-11

S33/A1 controller allows any combination of 80M-byte SMD and 80M/160M-byte Winchester drives (to a total system capacity of 320M bytes) to be interfaced to DEC PDP-11 minicomputers. The controller supports the Control Data Corp (CDC) 9762 80M-byte SMD, or equivalent, and 80M- and 160M-byte Winchester drives from CDC and Fujitsu. Media compatibility is maintained between DEC's RM02 SMD and 80M-byte SMDs interfaced to the controller.

The device is completely software compatible with all DEC operating systems that support the RMOS disk system. The RMO2 handler supports 80M-byte drives. When the controller is connected to 160M-byte CDC or Fujitsu Winchester drives, 2 logical 80M-byte units are mapped onto the 160M-byte Winchester.

Occupying one slot in the host PDP-11, the Unibus compatible controller operates in any hex SPC slot. It has 32-bit ECC for data, allowing correction of a single 11-bit error burst, and a 16-bit CRC for header error detection. A 4-sector (2k-byte) buffer contained on the controller eliminates "data late" errors. Self-test is std. The controller provides dual-port compatibility, enabling 2 controllers to access one or more common disks that are equipped with the dual port option.

Power requirements are 5 Vdc at 9.4 A and −15 Vdc at 0.5 A. The controller presents 1 unit load to the Unibus. Single-quantity price is $3900. **Dataram Corp**, Princeton Rd, Cranbury, NJ 08512.



Circle 293 on Inquiry Card

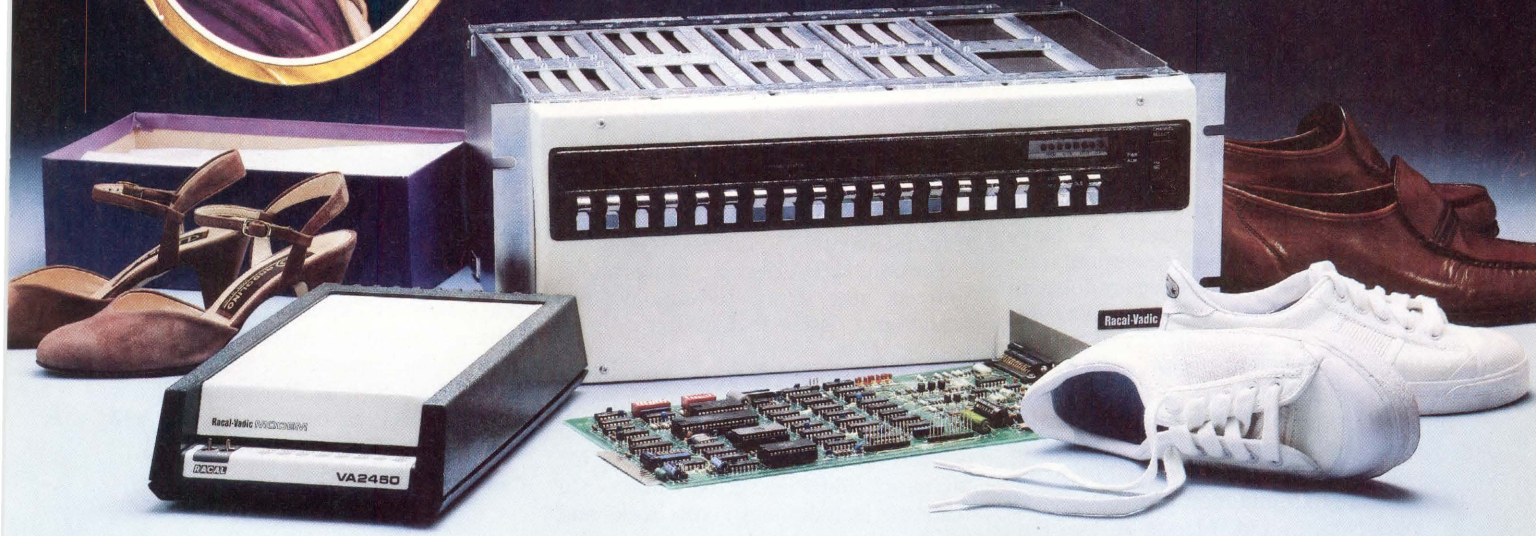
Measurement and control I/O system designed for GPIB

DMS550 measurement and control I/O system is designed for use with the IEEE 488 and IEC 625 general purpose interface bus (GPIB) and provides a link between any GPIB controller and the sensors and actuators of laboratory process automation systems. It is a complete measurement and control interface in a single, compact package that provides conditioning and conversion for any combination of analog and digital I/O signals.

User configured I/O modules allow the system to accommodate a variety of I/O signals. Currently available functions include digital input and output; analog input and output; pulse, event, and up/down counting; frequency measurement; realtime clock; and thermocouple, strain gauge, and RTD inputs. Up to 8 interchangeable I/O modules can be plugged into the single printed circuit motherboard that contains GPIB interface buffers and transceivers, as well as module address and interrupt request circuitry. Analog input multiplexers are bussed to a single, programmable gain

(continued on page 206)

Dear Ma:
For Point Of Sale applications, Racal-Vadic's 2400 bps modems are a real "shoe-in"!



Recently, three of the country's largest retail shoe chains selected Racal-Vadic modems for their Point Of Sale systems.

You see, Ma, many of the new P.O.S. terminals operate at 2400 bps; twice as fast as older 202-based systems. And, being synchronous, throughput is increased another 30% since start/stop bits aren't transmitted. This adds up to a big savings in line costs.

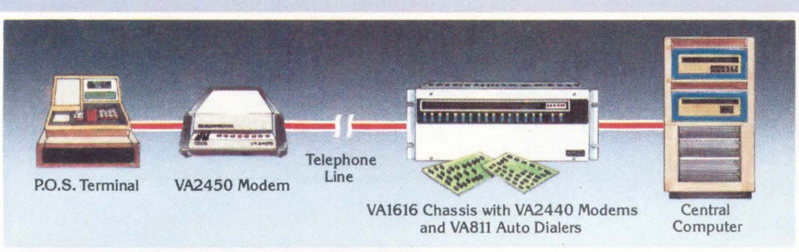
The retail stores install the VA2450 modems. They're compact, low profile and the telephone can sit on top, conserving space. An important feature of the VA2450 is the VOICE/DATA/MANUAL switch on the front panel which eliminates the need for a special telephone. During the day, the switch is positioned so the phone can be used for normal incoming and outgoing voice communication. At night, when rates are lower, the modem is engaged so the central computer site (using the VA2440 modem and VA811 dialer) can poll each retail store collecting sales, inventory and other data.

Up to eight VA2440 modems and VA811 auto dialers can be mounted in Racal-Vadic's 7-inch high rack chassis. The auto dialer(s) operate either in a singleline mode (one modem per dialer) or in Racal-Vadic's exclusive Multiline configuration where up to 60 modems can be accessed from a single RS366 or RS232C computer port. That's a tremendous savings in space and hardware.

When you sum it all up, Ma, Racal-Vadic modems are a real "shoe-in" when it comes to Point Of Sale systems for any business or industry.

Your independent thinking son,

Alexander Graham Jr.



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CIRCLE 123 ON INQUIRY CARD

A-D converter that allows high and low level signals to be mixed as required.

The I/O modules are designed as industrial grade system components. CMOS logic reduces ambient electrical noise susceptibility and power consumption. Internal shielding of the modules prevents emi/rfi interference and permits trouble-free operation within the I/O system. Input filtering is provided on certain digital I/O modules to block switch and relay contact closure transients and other high frequency noise. In addition, optional optical coupling isolates external digital inputs and outputs from the GPIB and the I/O system. The A-D conversion circuitry permits analog input signals to be digitized with minimum degradation from normal or common-mode errors, temperature drift, and ground loop problems. **DI-AN Data Systems Ltd,** Mersey House, Battersea Rd, Heaton Mersey, Stockport, Cheshire, SK4 3EA, England.

Circle 294 on Inquiry Card

Microprocessor based controller offered for 5.25″ Winchester drives

A microprocessor based controller with onboard separator logic and Shugart Associates' SA1400 series host interface, S1410 controls up to 2 Seagate ST-506 5.25″ and compatible disk drives. Completely compatible with all popular host adapters, the controller measures 5.75″ x 8″ (14.61 x 20 cm), exactly fitting the form factor of 5.25″ drives. Its compact dimensions are achieved using multisourced gate array technology that results in a design that utilizes only 56 ICs.

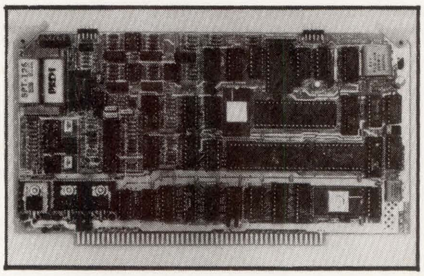
The controller features automatic error detection and correction circuitry that detects up to 22-bit burst errors and corrects up to 11-bit burst errors for increased data integrity. Other std features include automatic seek and verify, automatic fault detection, multisector transfers, selectable sector size (hardware strappable for either 256 or 512 bytes), programmable sector interleave, full onboard sector buffer, industry std host interface protocol (the Shugart Associates system interconnect bus), burst error length status reporting, fast step mode, and field proved software protocol.

Commands are issued to the controller over an 8-bit, bidirectional bus connected through an adapter to the host computer. The data separator/SERDES logic serializes bytes and converts to MFM data, and deserialized MFM data into 8-bit bytes. Programmable drive characteristics allow increased drive capacity without controller modification. Power required is 5 V at 2 A max and 12 V at 50 mA. Single-unit price is $295. **Xebec, an MSC company**, 432 Lakeside Dr, Sunnyvale, CA 94086.

Circle 295 on Inquiry Card

High speed S-100 telecommunications controller

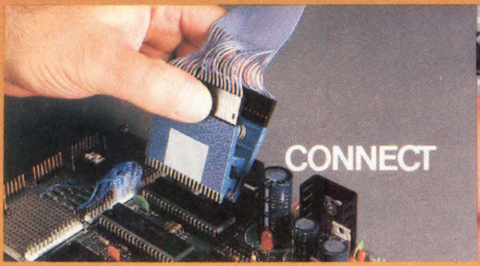
M/LINK intelligent communications interface enables a wide range of microcomputers to communicate with mainframes over a std dial-up phone line. It accommodates error-free data transmission at 2400 bps using the Bell 201C std and allows alternate data and voice communications. SDLC or BiSync communications protocols are PROM-selected at the time of installation. The device provides synchronous, half-duplex operation; throughput is optimized by firmware that incorporates routines for line handling and protocol generation. Dibit differential phase-shift keying encodes data 2 bits at a time to differentially shift the phase of an 1800-Hz carrier. Received phase shifts are decoded to recover the original data. Data input can be from an S-100 bus or from an asynchronous full-duplex RS-232 terminal. Transmit level is −9 dBm, receive level is 0 to −40 dBm, and RTS/CTS delay is jumper selected 25 or 150 ms. **Micromation, Inc**, 1620 Montgomery St, San Francisco, CA 94111.



Circle 296 on Inquiry Card

CIRCLE 124 ON INQUIRY CARD

Logic analysis this easy should be expensive. But it isn't.



Thanks to our PM3543's state-of-the-art technology, time-consuming logic analysis is a thing of the past.

Simply attach the 40 pin DIL clip to the microprocessor, select disassembly and instantly the logic analyzer is set up to look at address and data from the chosen microprocessor.

Then read.

The PM3543 has resident disassemblers for the most popular 8- and 16-bit microprocessors which are called up simply at the push of a button.

The 8-bit microprocessors include the 8048 family, 8080, 8085, 6800/02/08, Z80 and 6502/12 all in a single option. A second option includes the 16-bit microprocessors, the 8086 and Z8000 as well as the 6809, 8088 and 1802.

Using these options, data can be stored using an inexpensive cassette tape recorder. You may want to record a self-diagnostic routine in the lab and take it to the production line or into the field for servicing, or just for future reference. When loading back to the analyzer, both compare memory and trigger format are automatically set up to be the same as when the data was dumped.

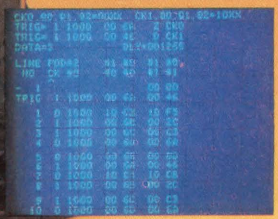
Additionally, the RS232 interface, included, permits hard copy of the collected program through the use of a printer. Just select the baud rate and print out. (IEEE 488 also available.)

The PM3543 is so easy to use and so low priced you'll wonder how you ever got along without it.

Call or write today for a free eye-opening demonstration.

For nationwide sales and service information call 800-631-7172, except in Hawaii, Alaska and New Jersey. In New Jersey call collect (201) 529-3800, or contact Philips Test & Measuring Instruments, Inc., 85 McKee Drive, Mahwah, NJ 07430.

Special menu for disassembly and serial interface options, as displayed on PM3543 screen.



Our dual clocking PM3543 demultiplexes the multiplex bus microprocessors, enabling both address and data to be sampled from a single connection. This, combined with more than 20 possible ways of triggering and sampling data, gives ultimate user flexibility.

The PM3543 Logic Analyzer. Superior Engineering.

From Philips, of course.

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☐ Call me to set up an appointment.
☐ Just send me more PM3543 literature.

Name__________

Title__________

Company__________

Street__________

City__________ State____ Zip______

Phone__________

Raster scan video controller

MULTIBUS compatible controller is capable of generating vectors, arcs, circles, and rectangles at speeds up to 800 ns/pixel, resolutions up to 1280 x 1024, and refresh rates up to 60 Hz/pixel. It supports either black and white or color graphics and integrates video refresh memory, a DMA bus interface, and video raster formatting and generation on a single board. Onboard 64k RAMs relieve the bus and main computer memory of all video refresh chores. Up to 2M pixels of screen data can be stored in 1 to 4 video planes. Access is via a high speed, bidirectional DMA channel. Output to the video monitor is via an ECL digital video channel capable of rates as high as 80 MHz (12.5 ns/pixel). **Ikier Technology, Inc**, 16 Sears St, Burlington, MA 01803.

Circle 297 on Inquiry Card

High performance controller boards

Series 200 controllers link the company's MIKRO-DISC Winchester drives to S-100, MULTIBUS, and Q-bus based computers. They support up to 4 drives, each with up to 32 heads, with a data transfer rate of 6.25M bps. The controllers also optimize the drives' seek time (28.3 ms avg) by full head-select and seek-complete handshaking. Error detection is provided using a 16-bit fire code (CRC-16). Fully buffered sectors of 256, 512, or 1024 bytes are included. Data through-checking and disk sector checking are performed on all read/write operations. The controllers also support write/verify operations and a go/no go self-test function. Firmware drivers are provided for optimum compatibility with host computer system software; custom drivers can also be supplied. All models are packaged to be embedded into the various host computers, and all feature single-board design for space efficiency and ease of maintenance. **New World Computer Co**, 2805 McGaw Ave, Irvine, CA 92714.

Circle 298 on Inquiry Card

Magnetic tape controller

Model DQ330 is a microprocessor based, single-board, 0.25″ (0.64-cm) 3M cartridge magnetic tape controller that provides interface for 1 or 2 Kennedy 6450 0.25″ DE300 type cartridge tape drives with up to 17M bytes of data storage each. The fully self-contained, quad-size controller has 30-ips read/write speed (FIFO buffer for DMA latency and memory addressing to 128k words), 6400-bpi format density, and 192,000-bps data transfer rate. It is designed for backup use with DEC LSI-11, -11/2, and -11/23 computers. The unit requires only a single CPU card slot and ribbon cable for interconnection and is compatible with DEC TM-11 and TS-03 software drivers in RT-11 and RSX-11 operating systems. In operation, the controller handles read after write serpentine head drives. It includes a diagnostic routine and automatic self-test that caused onboard diagnostics to run each time the Q-bus is initialized. An integral LED provides indication to ensure protection of critical database transfer. **Distributed Logic Corp**, 12800 Garden Grove Blvd, Garden Grove, CA 92643.

Circle 299 on Inquiry Card

Serial interface board

A 4-channel PDP-11 Unibus compatible board, DL4-11 replaces 4 DL-11A, B, C, or D ports in the same physical space of 1 card. It is compatible with both 20-mA current loop and RS-232-C/CCITT V.24; 16 baud rates, from 50 to 19.2k baud, can be selected for each port from the edge of the board without unplugging the board or changing crystals. Each port can be set via DIP switches for individual frame protocol; starting device and vector addresses are also set via DIP switches. The unit is compatible with DEC operating system software for DL-11. **Minntronics Corp**, 2599 White Bear Ave, St Paul, MN 55109.

Circle 300 on Inquiry Card

High speed, bit mapped graphics controller

FT-1024, a member of the Gateway™ series of MULTIBUS compatible boards, features a 1024 x 1024 x 1 frame buffer, with 800 x 1024 dedicated to the visible display. The additional buffer area is used as a cache for graphic symbols and fonts. Only 64 ms are required to write an entire buffer, allowing the display a 16-frame/s cinematic refresh rate that permits nonflickering moving images. Additional features include direct accessibility to arbitrary 1 x 16 rectangles, and simultaneous access to 4 different graphics objects. The board measures 12″ x 6.75″ x 0.55″ (30 x 17.15 x 1.40 cm) and has an op temp of 0 to 50 °C. **Forward Technology Inc**, 2595 Martin Ave, Santa Clara, CA 95050.

Circle 301 on Inquiry Card

Watch for March Design Frontier Report on Designing with Advanced System ICs

27 Megabytes in a 5¼" Winchester. All without plated media or thin film flim-flam.

RMS does it again. Our new series boasts capacity to 18 megabytes using conventional Winchester technology. And with our Data Express®-II data separator, capacity increases to a generous 27 megabytes. All without plated media or thin film flim-flam.

Here is the capacity you need. For multi-user systems and networks. For transaction-oriented and data base management applications. For bigger on-line programs. And that capacity is available within 70 ms (average access time).

Only RMS gives you all these features:

CHOICE OF EIGHT CAPACITIES

	STANDARD megabytes	WITH DATA EXPRESS-II megabytes
RMS 518	18	27
RMS 513	13.5	20.25
RMS 509	9	13.5
RMS 504	4.5	6.75

☐ Proprietary head positioning system with electronically dampened actuator ☐ Buffered step mode ☐ Integral microprocessor control ☐ All DC voltages ☐ Minifloppy form factor ☐ Industry-standard 5¼" Winchester interface ☐ Electrical spindle brake ☐ Landing/shipping zone outside the data area ☐ Heat dissipation of only 19.4 watts ☐ Built-in AGC ☐ Industry-standard transfer rate (5 MHz) ☐ Data Express-II transfer rate (7.5 MHz) ☐ Data Express data separators (optional)

For better cost per byte with the reliability of proven Winchester technology, talk to RMS. Circle the readers' service number for a free brochure. Better yet, call us to order your evaluation unit. We're accepting orders now.

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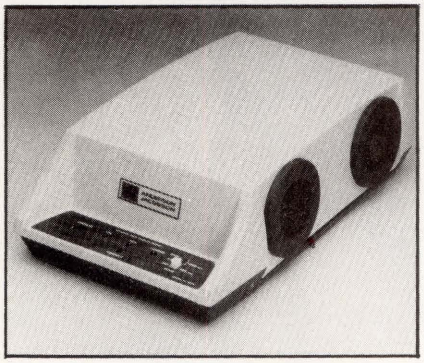
Capacity without Compromise

CIRCLE 127 ON INQUIRY CARD

Originate only, full-duplex acoustic coupler/modem



Microprocessor controlled AJ 1233 communicates with Bell 212 and 103/113 VA 3400, and AJ 1200 series modems. It is switch-selectable for communications at data rates of 1200 bps synchronously or asynchronously, and from 0 to 450 bps asynchronously. The device can be used in all modes either as an acoustic coupler or modem, directly connected to the switched network by a modular RJ-11C jack. A handset cup holds the handset firmly in place without the use of mechanical levers or springs. Vertically mounted acoustic cups ensure optimum performance at 1200 bps. A double-flanged seal provides noise isolation, and a handset to microphone coupling technique isolates vibration, as do the rugged housing and rubber footing design. **Anderson Jacobson, Inc**, 521 Charcot Ave, San Jose, CA 95131.

Circle 302 on Inquiry Card

Statistical multiplexer

DCX815 provides error-free transmission of up to 8 asynchronous data channels over a single composite link. It provides an unrestricted intermix of speeds from 50 to 9600 bps, and any 5-, 6-, 7-, or 8-bit Baudot, ASCII, or IBM code. With a max aggregate input of 19,200 bps, speeds and codes are switch-selectable on a per channel basis, or automatic baud rate can be selected. A single-digit readout provides a continuous monitor of the composite link utilization to aid in network management. Diagnostics permit the user to rapidly identify a defective channel while maintaining service on the remaining channels. The unit is available in 4- and 8-channel configurations. The 4-channel unit consists of a single PC card and is field upgradable to an 8-channel unit by the addition of a single expansion card. Lowering the hinged front panel allows access to controls and indicators for network configuration, diagnostic testing, and card removal. **Rixon Inc**, 2120 Industrial Pkwy, Silver Spring, MD 20904.

Circle 303 on Inquiry Card

High speed fiber optic system

Model 5330 consists of model 5330T fiber optic transmitter and model 5330R receiver capable of operating at NRZ data rates from dc to 100M bps. DC coupled from transmitter logic input to received data output, the system has an automatic threshold control (ATC) processor that continuously monitors the receiver output level and optimizes the discriminator threshold. An infinite hold memory circuit within the ATC is updated only if peak received power changes by 20 dB. Data inputs and outputs are ECL compatible. Completely independent of the transmitted data pattern or data rate, the system operates at 820 nm and can be used with either 100- or 200-μm diameter fiber. Transmission rates of 100M bps are possible up to 300 m using a partially graded 200-μm diameter fiber. **LeCroy Research Systems Corp**, 700 S Main St, Spring Valley, NY 10977.

Circle 304 on Inquiry Card

Communication protocol for PROM programmer

Communication protocol for the company's model MPP 80 SAM PROM programmer ensures accurate transmission of PROM data, even over poor or very long lines. Whether hardwired, microwave, or satellite linked, programming data can be transmitted over telephone lines from a computer or PROM programmer in the home office directly to a field site. Program changes do not have to be shipped in printed or punched tape form each time a product is updated or repaired in the field. The system uses a format similar to hexadecimal paper tape formats, with the addition of an acknowledgment protocol. A data record, including a 4-digit hex checksum of the single-digit values in the record, is

(continued on page 212)

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We make more variations of flat cable than any one: laminated, extruded and bonded, grey and color coded. Jacketed cable for inter-cabinet runs. Ground plane cable to reduce cross-talk. Even a twisted-pair flat cable that can be mass-terminated, so you get the performance you want and the lower costs you need.

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CIRCLE 129 ON INQUIRY CARD

transmitted to a receiver. Once each data record has been transmitted, the transmitter expects an acknowledgment from the receiver. If there are errors in the transmission, the record is sent again without the intervention of either operator. The process is repeated until either an acknowledged, correct transmission takes place or a timeout occurs. **Kontron Electronics, Inc**, 630 Price Ave, Redwood City, CA 94063.

Circle 305 on Inquiry Card

Synchronous fiber optic modem

FM-801 operates full duplex over a single optical fiber; synchronous data rates up to 19.2k bps and asynchronous transmission to 4800 bps are std. Automatic self-test features plus remote and local loopback capabilities verify link operation, and offer complete and continuous fault monitoring control. All RS-232-C handshaking features are built in. Data I/O is through a std 25-pin electrical connector. For distances up to 3 km, only 1-channel PCS fiber optic cable is required. Modem is available in rack-mount and standalone versions. **Fibronics**, 655 Concord St, Framingham, MA 01701.

Circle 306 on Inquiry Card

Intelligent, high speed synchronous modems

P-V.29/9600 and P-V.27/4800 modems are microprocessor controlled, fast train, and adaptively equalized with complete self-test and system test capabilities. P-V.29/9600 features an LSI transmitter and operates at 9600 bps with fallback rates of 7200/4800 bps. It is compatible with CCITT V.29 recommendations, operates on 4-wire, unconditioned private lines, and employs quadrature amplitude modulation. An optional multiplexing capability permits grouping of up to 4 independent data channels to form a 9600-bps data stream. P-V.27/4800 is designed to operate on either 2- or 4-wire private lines at 4800 bps, with a fallback rate of 2400 bps. Two independent 2400-bps data channels can be combined to form a 4800-bps data stream by means of an optional multiplexing feature. This unit is compatible with V.27/bis and V.27/ter. Both units operate in either point to point or multipoint, half- or full-duplex applications. **Prentice Corp**, 266 Caspian Dr, Sunnyvale, CA 94086.

Circle 307 on Inquiry Card

Modem eliminator

MOD/EM/ULATOR 402 provides local and remote loopback switches at both DTE interfaces. EIA local loopback tests can be conducted whether or not the DTE supplies the RTS and/or DTR signals. Used in conjunction with the device's self-test feature, the loopback capability eases system fault isolation. The device features asynchronous or synchronous transmission selection, synchronous data retiming to permit longer cables, 1200 to 19,200 bps selection, CTS delay selection, internal or external clock selection, local CTS control by remote DTE, active CD and RI signals, 8 EIA diagnostic indicators, and tandem operation capability. It can also be used to test any modem interfacing FDX device. **Com/Tech Systems Inc**, 505 Eighth Ave, New York, NY 10018.

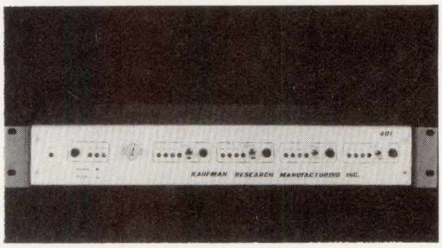
Circle 308 on Inquiry Card

Inductive coupled originate/answer modem

Using an inductive coupling technique for receiving, MFJ-1230 Bell compatible modem provides more reliable data transfer by eliminating errors caused by room noise, vibration, and other acoustic coupling problems. The modem operates at 0 to 300 baud, features half- and full-duplex operation, and is crystal controlled for very high stability. It provides TTL and CMOS I/Os as well as RS-232 compatibility, allowing easy interfacing to nearly any computer with proper software. In addition, I/O ports are provided for a cassette tape recorder. Housed in a 4" x 1.5" x 9.5" (10- x 3.8- x 24.1-cm) cabinet, the device is compatible with most std data terminals or personal computers. An Apple version, complete with software, that plugs into the game port is available for $139.95. **MFJ Enterprises, Inc**, 921 Lousiville Rd, Starkville, MS 39759.

Circle 309 on Inquiry Card

Port expander connects multiple devices to single CPU port



Model 401 port expander, capable of switching inbound clock signals and data, allows either 4 modems or 4 terminal clusters to share a single CPU port. Device synchronizes clear to send signals for outbound information before sending signal to CPU. No modem or modem eliminator is required when combining terminal clusters in local mode; internal clock eliminates the need for 1 modem/cluster. Each of the 5 ports can be configured to the modem or CPU terminal by setting front panel switches. Std RS-232-C cables are used. One cluster can be disconnected without disabling other operating clusters. **Kaufman Research Manufacturing, Inc**, 2260 Mora Dr, Mountain View, CA 94040.

Circle 310 on Inquiry Card

Personal computer modem

SIGNALMAN MK1 is a Bell 103 compatible modem designed for the personal computer user. It is completely portable, with a battery power system capable of running at least 50 consecutive hours. Built-in RS-232-C cable allows interface to any RS-232-C port. An audible carrier detect circuit replaces LEDs as confirmation of standard telephone line connections for voice and data. Automatic mode selection (originate/answer) and a talk/data switch are included. Serial, binary, and asynchronous formats operate at data rates of 0 to 300 bps, with full duplex. **Anchor Automation, Inc**, 16130 Valerio St, Van Nuys, CA 91406.

Circle 311 on Inquiry Card

Development support package

Offered for the company's series 80 family of 8-bit, CMOS, single-chip microcomputers, EASE-49™ allows users to develop 8048/8049 type circuits on any existing host computer compatible with CP/M or ISIS operating systems, including personal computers. The package is priced at $3995 and consists of the MPB-800 emulation board, development system interface software on an 8″ floppy disk, and documentation. The emulation board functions between the user's CP/M or ISIS based development system and the 80C48/80C49 socket, emulating in real time the operation of the company's single-chip microcomputer unit. Interface software is either ISIS or CP/M compatible. **OKI Semiconductor**, 1333 Lawrence Expressway, Santa Clara, CA 95051.

Circle 312 on Inquiry Card

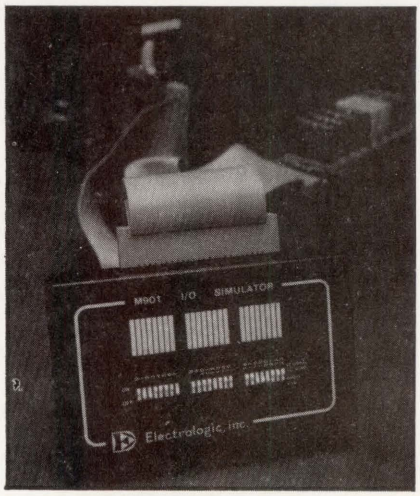
IBM 3101 emulator

DM310 display terminal emulates the IBM 3101 models 22 and 23, offering both conversation and forms mode operation in one unit. It includes an auxiliary printer port; flicker-free 60-Hz screen refresh; 1920-char screen presentation, with a 25th line for status information; 3101 compatible keyboard with 8 programmable function keys and 12-key numeric pad; P42 green phosphor display; and extensive visual and logical field attributes. The terminal is priced at $1295. **Beehive International**, 4910 Amelia Earhart Dr, Salt Lake City, UT 84125.

Circle 313 on Inquiry Card

I/O simulator

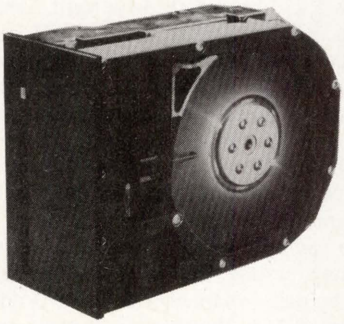
M901 I/O simulator device is edge connector compatible with industry std I/O module racks. Packaged for handheld or benchtop simulation of I/Os to a microprocessor, device can also simulate the processor to I/O devices. Features include indicators for 24 simultaneous I/O channels, cardedge connector that mates directly to I/O module mounting racks operating with 5-Vdc logic, and switches rated for 50k cycles. **Electrologic, Inc**, 1359 28th St, Signal Hill, CA 90806.



Circle 314 on Inquiry Card

5.25" thin film drives

Designed for 16- and 32-bit processors, "freedom generation" ST538 and ST706 drives utilize the same interface and power supply as the ST506 micro-Winchester. ST538 offers 38.25M bytes of unformatted storage, with 3672 tracks/drive and a track density of 540 tracks/in (212.6/cm). It features 32 sectors/track, transfer rate of 5.0M bps, 8.33-ms avg latency, 3600-rpm rotational speed, 10,202-fc/in recording density, 612 cylinders/drive, 6 heads/drive, and 3 fixed disks/drive. Formatted capacity is 30M bytes/drive. ST706 is claimed to be the first removeable 5.25" microdisk cartridge drive to use thin film heads. It offers 6.38M-byte/drive unformatted storage capacity, 270-track/in (106/cm) track density, 306 cylinders/drive, 612 tracks/drive, and 2 heads/drive. Formatted capacity is 5M bytes/drive. **Seagate Technology**, 360 El Pueblo Rd, Scotts Valley, CA 95066.



Circle 315 on Inquiry Card

Fixed media disk drive

32M-byte 8" version of the 9410 Finch drive can be mounted horizontally or vertically in the same space as an 8" flexible media drive. Data are stored on 3 lubricated disks housed in an environmentally sealed data module that also contains a rotary voice coil actuator for head positioning, accuracy, and rapid access to stored data. Information is transferred to or from the data module at a rate of 6.45M bps. Single-track and avg seek times are 10 ms and 50 ms, respectively, with an avg latency time of 8.33 ms. The unit can be configured with up to 4 drives in a star or daisy chain configuration, and, through its interface electronics, in a daisy chain configuration with flexible disk drives. All drive electronics are contained on 3 circuit boards. **Control Data Corp**, Box O, Minneapolis, MN 55440.

Circle 316 on Inquiry Card

256k-byte memory for personal computer

CI-PCM memory module is designed specifically for the IBM personal computer and uses 64k-bit NMOS dynamic RAM technology. Module requries 1 I/O expansion slot for 256k bytes of memory, and generates and checks parity with IBM compatible interrupt. Device is addressable in 64k-byte increments throughout the 1M-byte address field. Memory access time is 225 ns; cycle time is 400 ns with a current requirement of less than 1 A from the system's 5-V power supply. Modules are available in 64k-, 128k-, 192k, and 256k-byte configurations. **Chrislin Industries, Inc**, 31352 Via Colinas, Suite 102, Westlake Village, CA 91361.

Circle 317 on Inquiry Card

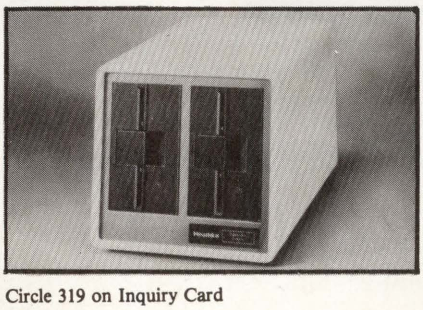
5.25" fixed disk drive

SI series M4863 drive is available with storage capacity of 3.33M, 6.66M, or 10M bytes (unformatted); each disk surface employs one movable head to service 160 data tracks. The series offers a high speed seek time of 75 ms avg, 160 ms max, including settling time. Because of its size and operative versatility, the drive can be installed either vertically or horizontally. Its narrow width permits side by side installation with most miniflexible disk drives. **Mitsubishi Electronics America, Inc, Computer Peripherals Div**, 2200 W Artesia Blvd, Compton, CA 90220.

Circle 318 on Inquiry Card

Expanded disk storage

H-37 high density disk system and Z-89-37 double-density disk controller card expands disk storage for the company's microcomputer systems to more than 640k chars/5.25" diskette. The H-37-2, available with 2 drives, increases data storage capacity to 1.28M bytes. **Heath Co**, Dept 350-335, Benton Harbor, MI 49022.



Circle 319 on Inquiry Card

Tape backup for Winchester systems

Tape streamer backup option for Chieftain and Pathfinder 8" and 5.25" Winchester systems stores up to 20M bytes on 0.25" cartridge tape. The option allows data transfer of 20M bytes in less than 5 min at 90 ips. Series also incorporates file by file or complete backup with single command as backup methods. Drive to tape and tape to drive data transfer is provided. **Smoke Signal Broadcasting**, 31336 Via Colinas, Westlake Village, CA 91361.

Circle 320 on Inquiry Card

27M-byte capacity Winchester drives

Series of 5.25" Winchester disk drives with 1 to 4 platter models delivers capacities of 4.5M- to 18M-bytes unformatted, and increases tracks per platter from 306 to 432, and tracks per inch from 255 to 270. Industry std 5.0M-bps transfer rate is unaffected. Optional Data Express™ II data separator adds 50% recording/track capacity and uses 7.5-MHz transfer rate. 27M-byte disk drive capacity is attainable using conventional Winchester technology. All models fit mini-floppy form factor, require only dc voltages, and use industry std 5.25" interface. **Rotating Memory Systems, Inc**, 1701 McCarthy Blvd, Milpitas, CA 95035.

Circle 321 on Inquiry Card

High volume recording disk drive

A double-sided, double-density 5.25" floppy disk drive, capable of recording at 96 tracks/in, the QumeTrak 592 has 1000k bytes formatted capacity, or up to 819k bytes unformatted capacity. Track to track access time is 3 ms. Designed for small system and Winchester backup applications, drive includes a head load solenoid to reduce media wear and ensure data integrity. Additional reliability is provided by brushless dc motor in a direct drive configuration. **QUME**, 2350 Qume Dr, San Jose, CA 95131.

Circle 322 on Inquiry Card

256k-byte MOS RAM

Dual-wide memory module for DEC LSI-11/23 uses 64k RAMs and is powered from a single 5-V supply. High reliability and low cost are achieved through the use of a 2-layer PCB and significantly fewer components. Addressing is switch-selectable in 32k blocks up to 2M words, and access time is rated at 150 ns. Single units are available for $1200; OEM discounts are available. **Professional Data Systems,** 2670 Walnut Ave, Suite C, Tustin, CA 92680.

Circle 323 on Inquiry Card

Mass storage system

ZRP-100 system features a 160M-byte Winchester disk drive backed with a 100-ips streamer tape drive. Fully industry compatible and using std 0.5″ (1.27-cm) magnetic tape, the streamer drive can operate in a conventional start/stop mode at 25 ips. It can store up to 46M bytes of unformatted data on 1 std reel of 1.5-mil tape. The streamer drive offers a data transfer rate of 160k bytes/s, rewind speed of 200 ips, and hard error rate of less than 1 in 10^{10}. It also provides a fully automatic loading feature and automatic diagnostics. The Winchester drive features an MTBF of 10,000 h and avg access speed of 27 ms. System is housed in a 40″ x 23″ (101- x 58-cm) steel cabinet. **ZZY Systems,** 1900 Lafayette St, Santa Clara, CA 95050.

Circle 324 on Inquiry Card

5M-byte hard disk subsystem

LS525 incorporates a Seagate Technology ST506 5.25″ hard disk drive with 2 magnetic disks, 4 read/write heads, and 6.38M bytes of total recordable storage capacity. It includes a proprietary 10-MHz microprogrammed controller that can simultaneously control up to 4 drives. The controller operates under the device independent LDOS disk operating system that permits users to carry on time saving functions such as linking, routing, setting, and filtering. The drive can be daisy chained with up to 3 additional 5.25″ Winchester drives, providing 20M bytes of online storage. It measures 12″ x 5.25″ x 13.5″ (30 x 13.34 x 34 cm) and weighs 18.5 lb (8.4 kg). Power requirements are 100/120/220/240 Vac ±10% selectable and 47 to 63 Hz, 100 W. Initially available for use with TRS-80 I and II systems, the drive will also be available for Apple II and III, Commodore PET, Atari 800, and Zenith microcomputers. **Laredo Systems, Inc,** 2264 Calle de Luna, Santa Clara, CA 95050.

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Speech for yourself. New development system from TI.

Here's the capability to develop, analyze, edit and program speech — in-house — it's new, from the first supplier of speech products and services — Texas Instruments.

It's a hardware/software system that supports the creation and design of speech synthesis products.

Vocabulary development can be totally controlled from initial script generation to EPROM programming. The Multi-AMPL* Speech Development System provides complete facilities for vocabulary production through either constructive synthesis or analysis synthesis methods.

The hardware

The two major hardware components of TI's new Speech Development System are the TMAM9080 Multi-AMPL System and the data collection processor. The TMAM9080 offers a high-performance, general-purpose computing environment for speech data processing and utility execution. The data collection processor is an intelligent "slave" device that provides the analog interface required to collect and play back speech signals. It provides 12-bit linear A/D-D/A conversion accuracy and includes necessary anti-aliasing and signal reconstruction filters.

Speech Development System Key Features

- Text-to-speech
- Interactive editing of text, phoneme, allophone and LPC data
- LPC analysis synthesis
- TMS5100, TMS5110A, TMS5200, TMS5220 VSP (Voice Synthesis Processor) capabilities
- Speech recording and play back
- Digitized speech
- EPROM programming
- User-oriented software

The software

The software packages in the Speech Development System are designed to provide you with friendly, interactive interfaces that guide you through the vocabulary generation process quickly and easily. Because speech synthesis is data-intensive, the Speech Development System uses a data base management system. This allows convenient interaction with all utilities and creates a complete speech library, with everything from simple script listings to comprehensive LPC (Linear Predictive Coding) data files.

The system

The Speech Development System uses two different methods to generate speech data. In **Analysis Synthesis,** data from natural speech is used to gauge the parameters of a time-varying linear model. Then the synthesis process creates the compressed synthetic speech signal from these parameters. In **Constructive Synthesis,** words, phrases and sounds are built from a pre-fabricated library of basic speech sounds.

The source

There's a lot to talk about. You can find out more about TI's new Multi-AMPL Speech Development System and how to create your own custom word library, a library completely compatible with TI's Voice Synthesis Processors, by writing to Texas Instruments, P.O. Box 202129, Dallas, Texas 75220.

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

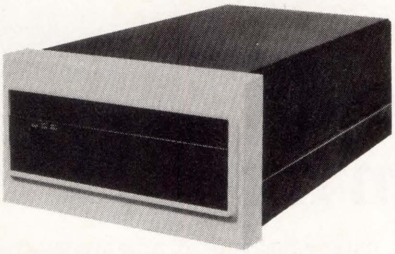
TEXAS INSTRUMENTS
INCORPORATED

85936

CIRCLE 134 ON INQUIRY CARD

160M-byte Winchester disk drive

Model 5350 is designed for cabinet mounting in the packaged Harris 80 and 300 super minicomputer systems, as well as in peripheral cabinets for the Harris 100, 500, and 800. A sealed module protects the entire recording environment from contaminants and provides a fixed head-to-media relationship that eliminates the need for head alignments. The drive has 4 disks with 5 data surfaces. Avg seek time is 30 ms, and I/O data rate is 1.2M bps. With 680 tracks/in (268/cm), the drive has a formatted capacity of 144M bytes. **Harris Corp, Computer Systems Div**, 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33310.



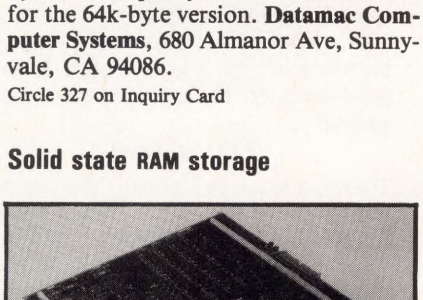
Circle 326 on Inquiry Card

High capacity memory expansion board

Containing up to 4 times the amount of memory currently available for the IBM personal computer, the board allows IBM personal computer users to directly address up to 1M byte of memory. The board can be configured in a variety of sizes: 64k, 128k, 192k, and 256k bytes—with parity. Prices start at $499 for the 64k-byte version. **Datamac Computer Systems**, 680 Almanor Ave, Sunnyvale, CA 94086.

Circle 327 on Inquiry Card

Solid state RAM storage



Lotus cache memory solid state storage device provides greater system throughput and faster user response time by reducing seek and latency wait times; associated data transfers can occur in 225 ms. A 4-layer PCB that uses 64k-bit RAM chips, the device comes in 4 sizes and plugs directly into the system backplane. Multiple boards can be used to provide up to 64M bytes of RAM storage. Memory operates in block mode, consisting of 256 words/block. One data block is transferred for each command sequence; no partial blocks can be transferred. Optional error correction and detection capability is available. **Point 4 Data Corp**, 2569 McCabe Way, Irvine, CA 92714.

Circle 328 on Inquiry Card

INTEGRATED CIRCUITS

Static MOS ROMs

The 64k 2364 (organized as 8192 x 8) and the 128k 23128 (organized as 16384 x 8) are offered in upward compatible JEDEC-B std 28-pin packages. For both devices, std worst-case access time is 300 ns. Both offer programmable chip select inputs, allowing the customer to define active high or low and set the desired logic level as part of the masking process. Fabricated with n-channel silicon gate MOS technology, the TTL compatible devices require only one 5-V power supply, offer high noise immunity, and are available in both plastic and ceramic packages screened to commercial and military temp ranges. The 23128 dissipates 450 mW max, while the 2364 is rated at 440 mW max. **Signetics Corp**, 811 E Arques Ave, Sunnyvale, CA 94086.

Circle 329 on Inquiry Card

Elastic store device and line coder

TCM2401 elastic store device provides the buffer store and pulse-stuffing (justification) functions required in a second-order pulse coded modulation multiplexer. The part can be used in either a European CCITT 2.048M- to 8.488M-bps system or in a U.S. 1.544M- to 6.312M-bps system. It incorporates onchip circuitry for a variety of complex functions, including write-clock distributor, read-clock distributor, 8-bit wide elastic store, justification-code detector, timing-clock gating, phase comparator, and binary output retimer. Fabricated using metal gate CMOS technology, the device is provided in a std 16-pin plastic DIP and has an op temp range of −25 to 70°C. Max power dissipation is 200 mW with nominal 10-V supply voltage. Specifically designed for European telecommunication systems, the TCM2201 line coder has a std clock rate of 2.048 MHz, onchip transmission coder, reception decoder, and error detection circuitry. It uses an HDB-3 (high-density bipolar-3) coding scheme that precludes strings of zeros greater than 3 bits. The transmission coder is fed by a synchronous clock and binary NRZ data, while the reception decoder is fed by a synchronous clock and a bipolar or HDB-3 coded signal externally split in 2 input signals. A "serial OP control" input allows the decoder and coder to be cascaded internally. Fabricated using metal gate CMOS technology, the part has a max power dissipation of 300 mW at a supply voltage of 12 V. It is packaged in a std 16-pin plastic DIP and has an op temp range of −25 to 85°C. **Texas Instruments Inc**, PO Box 202129, Dallas, TX 75220.

Circle 330 on Inquiry Card

MIL-STD of 64k-bit EPROM and 16k-bit static RAM

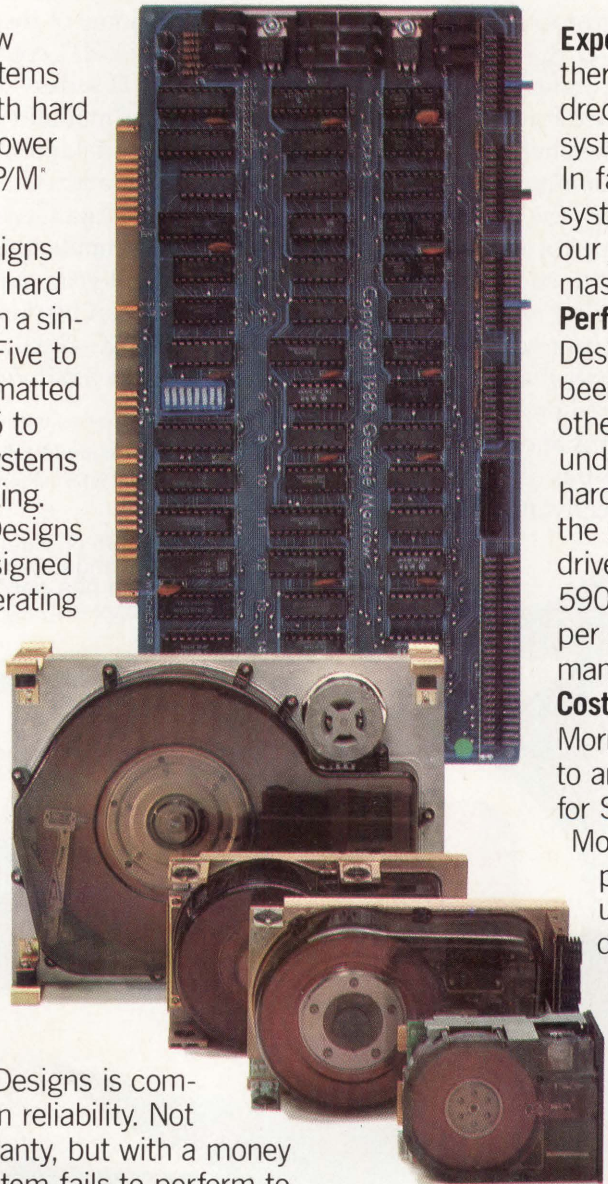
M2764 military version of the 2764 EPROM meets MIL-STD-883 class B stds and provides 64k bits of nonvolatile memory organized as 8k x 8 bits. Worst-case access time is 250 ns. The part is fast enough to eliminate program wait states and allow for max throughput in many applications. Its 28-pin configuration conforms to JEDEC stds; the pinout design permits 2-line control, and the 28-pin format is adaptable to RAMs, ROMs, EEPROMs, and EPROMs, and allows for interchangeable use of 2k-, 4k-, 8k-, 16k-, and 32k-byte memories. Fabricated using the company's HMOS-E technology for nonvolatile memories, the device offers a low active current of 100 mA that drops to 50 mA in standby mode. A 450-ns version is also available. Military M2167-10 is a fully static 16k-bit RAM with 16k- x 1-bit storage capacity and 100-ns access time. It is claimed to be the densest static RAM available that conforms to MIL-STD-883 class B. The part features an automatic power-down mode, uses a single 5-V power supply, and is TTL compatible. Both devices operate over −55 to 125°C. **Intel Corp**, 5000 W Williams Field Rd, Chandler, AZ 85224.

Circle 331 on Inquiry Card

MORROW DESIGNS

Now, Complete 5¼" System 5 Mbytes $2,495

Leading edge technology in hard disk systems.



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Widest range. Morrow Designs offers the widest range of hard disk systems available from a single supplier. 5¼," 8," 14." Five to over 100 megabytes of formatted hard disk storage. $2,995 to $17,980. Cost effective systems that work. And keep working.

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Reliable systems. Morrow Designs is committed to hard disk system reliability. Not simply with a 90-day warranty, but with a money back guarantee. If our system fails to perform to specification, send it back. We'll send back your money.

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CIRCLE 135 ON INQUIRY CARD

Synchronous Communications Interfaces with X.25 capability.

MDB makes the difference!

The industry's only DUP-11* compatible interfaces for Q-bus* (as well as Unibus*) computers are now available with support for X.25, the international data communications protocol. This means that the popular MDB DUPV-11 (Q-bus) and MDB DUP-11 (Unibus) synchronous communications interfaces are ideally suited for use in public common carrier packet-switched networks and multi-computer or terminal communications.

In addition to X.25 capability, the interfaces offer a number of significant performance advantages above and beyond their functional equivalency and software compatibility with DEC. The small size quad boards will accommodate BI-Sync and DDCMP in byte control and SDLC, ADCCP and HDLC bit-oriented protocols with programmable character lengths and complete hardware error control. For Q-bus users, this is big system protocol handling never available before.

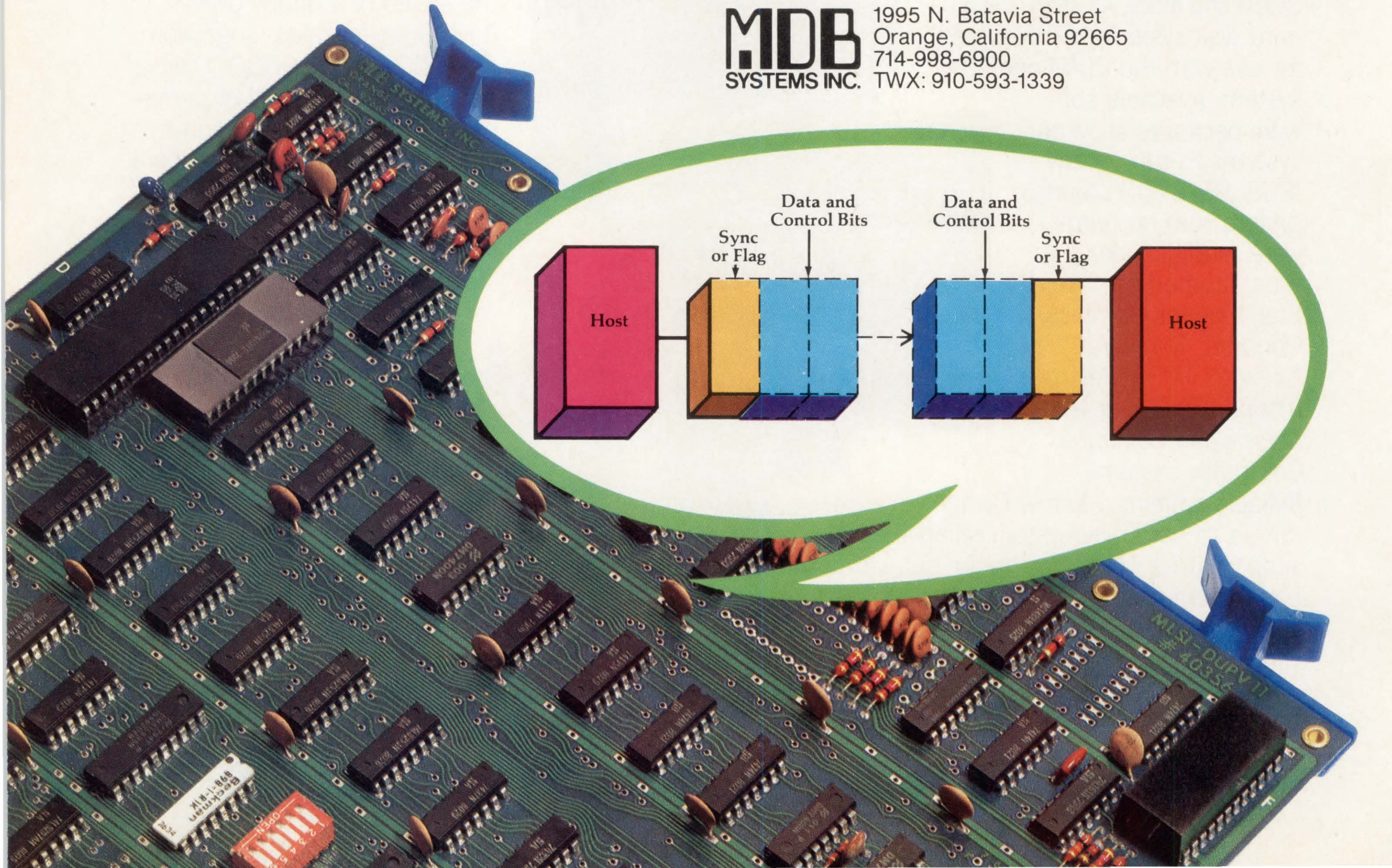
But that's not all the difference MDB interfaces can make to your system. MDB offers line printer controllers for over 100 computer/printer combinations and some of them test themselves. MDB makes the only DZ11 compatible multiplexors for DEC's LSI*-11 series—and RS-422 is available. We offer PROM modules with window mapping, asynchronous serial interfaces, LSI-11/23 box systems with 22 bit addressing, and a wide range of products for Data General, Perkin-Elmer and IBM Series/1 computers. Our boards are warranteed for a full year, many are available off-the-shelf and they can be purchased under GSA contract #GS-00C-02851.

Let MDB make a difference in your system.

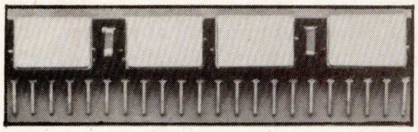
*Trademark Digital Equipment Corporation

Circle 137 for featured product data.
Circle 138 for general information.

MDB SYSTEMS INC. 1995 N. Batavia Street
Orange, California 92665
714-998-6900
TWX: 910-593-1339



High density 256k- x 1-bit dynamic RAM



EDH-4256 is offered in a 22-pin single inline package (SIP) that utilizes 4 industry std 64k RAMs in leadless chip carriers and includes two 0.1-μf decoupling capacitors. Operating on a single 5-V ($\pm$10%) supply, the SIP dissipates only 540 mW active and 110 mW standby. Data inputs and outputs are common, with separate RAS control. The chip offers std system oriented features such as direct interfacing capability with high performance logic families, max input noise immunity to minimize "false triggering" of the inputs, onchip address and data registers, and 2 chip select methods. It is useful wherever board space is at a premium, in applications that require error checking, or in systems using unorthodox bit counts. Two versions are currently available: EDH-4256-15, with 150-ns access time, and EDH-4256-20, with 200-ns access time. **Electronic Designs, Inc**, 230 Eliot St, Ashland, MA 01721.

Circle 332 on Inquiry Card

CMOS RAMs

MWS5114-3, -2, and -1 have access times of 200, 250, and 300 ns, respectively, over an op temp range of 0 to 70°C. Organized as 1024 words by 4 bits, the devices are fabricated in the company's ion-implanted silicon gate CMOS technology for low power consumption. They are specified to retain data at voltages as low as 2 V over the entire op temp range, allowing them to be applied in battery backup systems. Initial versions of the 18-pin devices are available in plastic packages; ceramic parts will be available early in 1982. **RCA/Solid State Div**, Rte 202, Somerville, NJ 08876.

Circle 333 on Inquiry Card

Programmable array logic circuits

Six members of programmable array logic (PAL^{R}) series 24 family of bipolar ICs are designed to perform combinatorial logic functions. Included are the PAL12L10, a 12-input, 10-output AND-OR-INVERT gate array; PAL14L8, a 14-input, 8-output AND-OR-INVERT gate array; PAL16L6, a 16-input, 6-output AND-OR-INVERT gate array; PAL18L4, an 18-input, 4-output AND-OR-INVERT gate array; PAL20L2, a 20-input, dual-output AND-OR-INVERT gate array; and PAL20C1, a 20-input, single-output AND-OR/AND-OR-INVERT gate array. Offered in 300-mil wide Skinnydip™ packages, the devices have the equivalent of 200 gates each, implanted with AND arrays driving fixed OR arrays. Their transfer function is equivalent to the sum of products. The circuits draw a max of 100 mA current, although the typ I_{CC} requirement is 60 mA. Input to output time is a max of 40 ns. Typ access time is 25 ns. Commercial and military op temp ranges are available. **Monolithic Memories Inc**, 1165 E Arques Ave, Sunnyvale, CA 94086.

Circle 334 on Inquiry Card

Military version 16k static RAM

Organized as 16k x 1, IMS1400S-70M meets MIL-STD-883B requirements and operates over the −55 to 125°C range. Featuring a chip enable access time of 70 ns, the device consumes a max power of 660 mW that is reduced to 165 mW when the chip is in the low power standby mode. It is packaged in a 20-pin DIP and is priced at $126 in 100-piece quantities. 55- and 45-ns versions are also available. **INMOS Corp**, PO Box 16000, Colorado Springs, CO 80935.

Circle 335 on Inquiry Card

CMOS gate arrays

The first 2 members of the SLX family of high density gate arrays, SLX 6320 and SLX 6360 are 2000- and 6000-gate high performance CMOS gate arrays, respectively. Both devices will have a typ internal gate propagation delay of 2 ns, and will be available in TTL and CMOS compatible versions. The family will be fabricated in the company's 3-μm, dual-layer metal CMOS silicon gate process (M²CMOS™) that offers significant advantages in densities and speed/power performance. Devices from the family can be used in all applications where bipolar TTL logic devices have been traditionally used. They are specified to be compatible with TTL and their ac and dc characteristics have been designed to match the actual characteristics of the 74LS logic family. Typical propagation delay of the SLX family output buffer driving 50 pF is 8 ns, while the device's TTL input buffer has a typ propagation delay of 4 ns. **National Semiconductor**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

DATA CONVERSION

16-bit DAC

PCM50 offers 16-bit resolution with a 96-dB dynamic range. Typical total harmonic distortion is 0.003% (FS input, 16 bits), typ settling time is 5 μs, and typ differential linearity error is 0.0015% of FSR. The device can also be operated as a 14-bit converter for less demanding applications and is compatible with EIAJ STC-007 specifications. Pin compatible with DAC71-COB-V, the unit's ceramic 24-pin DIP also contains an internal voltage reference and an output. The DAC is priced at $49.75 in quantities of 100. **Burr-Brown**, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734.

Circle 336 on Inquiry Card

Militarized 5-MHz word rate ADC

Constructed on a single 5" x 5.43" x 0.5" (12.7- x 13.8- x 1.27-cm) PC card, MOD-1205MB includes a track-and-hold amplifier with 25-ps max aperture uncertainty, encoder, and timing and output registers. Features include a min analog input bandwidth of 10 MHz, a signal-noise ratio of 63 dB min, and a noise/power ratio of 56 dB min. Analog input is $\pm$2.048 V full scale, $\pm$4 V max, with 400-Ω or 50-Ω input impedance pin selectable. Input offset voltage is adjustable to zero via an onboard potentiometer. Power required is 13 W. The device provides min/max limits on all specs. **Analog Devices, Inc**, Rte 1 Industrial Pk, Norwood, MA 02062.

Circle 337 on Inquiry Card

Microprocessor compatible multiplying DAC

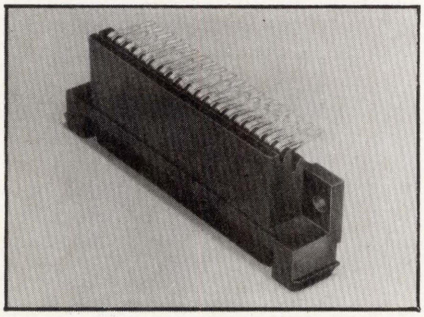
DAC-888 high speed multiplying DAC provides microprocessor compatibility for 8- and 4-bit microprocessors. Device meets the requirements of 8-bit microprocessors with no external logic requirement except address decoding. Single rank, level triggered latch, and 0-ns data hold time overcome potential for unpredictable output in double buffered D-A configurations. The converters are available in military and industrial grades (−25°C to 85°C); devices processed to MIL-STD-883B are also std products. **Precision Monolithics, Inc**, 1500 Space Park Dr, Santa Clara, CA 95050.

Circle 338 on Inquiry Card

Single-channel fiber optic connector

Designed to terminate moderate size cable with typical insertion loss of 1 to 2 dB, the 804 series molded plastic connectors accommodate a variety of industrial/commercial grade glass, plastic, or plastic coated cable in fiber sizes from 140 μm to 1 mm. In addition, molded plastic mating receptacles can be specified to accept industry std fiber optic active components such as TO-18 and TO-46 styles, as well as the Motorola Straightshooter™ and Honeywell's plastic and metal Sweetspot™ devices. Total termination time for single units is less than 10 min, after cable stripping. The connector design also enables mass termination in seconds using ultrasonic bonding or heat welding. Connectors are available in PCB, bulkhead, rack and panel, and cable to cable configurations. They can also be stack mounted for junction box applications. **Amphenol North America, a Div of Bunker Ramo Corp,**, 2122 York Rd, Oak Brook, IL 60521. Circle 339 on Inquiry Card

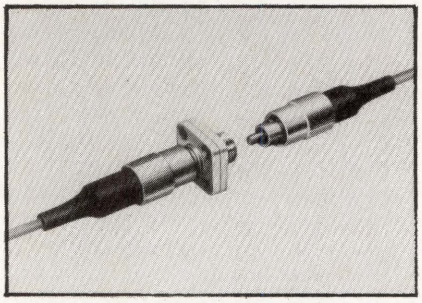
D subminiature, right-angle female receptacle



Style E2 all-plastic receptacle for RS-499 cable assemblies incorporates a pair of molded-in RS-499 latches and requires no additional hardware. The cable assembly plugs into the receptacle and is solidly retained by the latches. Receptacles are available in 9, 15, 25, and 37 positions, and mate with any type of D subminiature male plug connector. They feature large lead-ins for easy mating, 60/40 tin/lead selective plating on the tails for enhanced solderability, rigid tails requiring no plastic inserts or spacers for support, plus a double-stamping process that permits precise, selective placement of gold only where required. **Holmberg Electronics Corp**, Asheville Hwy, Inman, SC 29349.

Circle 340 on Inquiry Card

Single optical fiber connection system



The system is composed of a connector, a plug ferrule, receptacles, and a fiber polisher for single- and multi-mode signal transmission applications. Accepting a single fiber, PVC-covered, 3-mm dia cord, model SAP-2 optical fiber plug furnishes low connection loss (0.5 ± 0.2 dB) in single-mode transmission, with a 10-μm core fiber in the 1.3-μm wavelength region, when used with the ultrahigh precision ceramic plug ferrule, model SF-1. This ferrule offers high environmental reliability. Its high concentricity and capillary hole diameter tolerances permit easy connector assembly in the field and eliminate special alignment efforts. The component's high durability allows 500 or more connections. Available in 2 versions (SAR-1 and -2), the receptacle achieves high coupling efficiency between a fiber and a light sensing or emitting element. The SAP/SF/SAR connectors operate from −20 to 60°C. Completing the system, the L-1A fiber-polishing machine handles up to 12 plug ferrules. **Seiko Instruments, USA, Inc**, 2990 W Lomita Blvd, Torrance, CA 90505.

Circle 341 on Inquiry Card

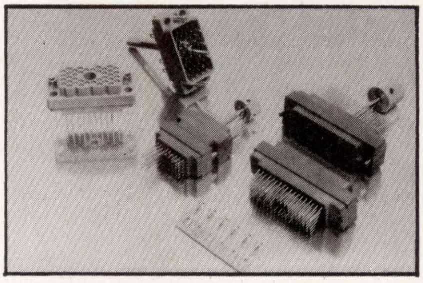
D subminiature rectangular connectors

Connectors employ a 2-piece thermoplastic insulator per UL 94V-O, and are available in E, A, B, C, and D shell sizes. Insulators have an op temp range of −65 to 300 °F (−55 to 149 °C), and accommodate contact arrangements of 9, 15, 25, 37, and 50-size #20 nonremovable (captivated) solder pot, wirewrap, or PC contacts, respectively. They accommodate up to 50 contacts (each rated at 5 A) and are capable of accepting up to #20 gauge wire. Connectors are completely intermateable with the corresponding size of all existing submin D connectors. They can be adapted to either panel or cable applications by adding the company's backshells and latching hardware. Custom configurations are available. Shells and contacts are offered in a variety of finishes. The user can also specify installation of only the contacts required for a particular application. **CD Corp**, 5855 W Centinela Ave, Los Angeles, CA 90045.

Circle 342 on Inquiry Card

Rack and panel connectors

Souriau/Connectral 816 series connectors feature hermaphroditic contacts and a center actuating jackscrew, and are completely interchangeable and intermateable with the ELCO 8016 series and EDAC 516 series. Mating halves of each contact are identical and consist of a 2-prong fork shape.The center actuating jackscrew locks mated connector halves securely together and facilitates mating and unmating. Crimp contacts are available loose or on reels for automatic crimping and can be inserted in either plug or receptacle bodies. Contacts are also available for wirewrap and solder eyelet termination. Polarizing hardware can be set to any of 6 positions at the factory or by the user. Connectors are available in glass-filled diallyl phthalate and polycarbonate with 20, 38, 56, 90, and 120 positions. **Souriau Inc**, 7765 Kester Ave, Van Nuys, CA 91405.



Circle 343 on Inquiry Card

Spring socket pins

Low cost, gold plated beryllium female connectors provide easy replacement of PCB modules and semiconductor devices. Socket portion of the pin contains 2 spring tines that accept and provide contact with either round or flat pins, or leads. The 0.230″ (0.584-cm) spring socket pin has a 0.090″ (0.229-cm) pin diameter; socket portion accepts a 0.185″ (0.470-cm) lead length inside and can be wave or hand soldered into circuits. **Auto-Swage Products, Inc**, 726 River Rd, Shelton, CT 06484.

Circle 344 on Inquiry Card

Software and microprocessor video courses

Up to 25 technical employees can be trained inhouse in software engineering for micro- and minicomputer systems and in microprocessor and microcomputer technology through software and microprocessor video courses. The scope of the software course is managerial, emphasizing skills development for managing realtime micro- and minicomputer software and hardware development projects. Course participants learn to specify system requirements, estimate costs, monitor and control project schedules, and plan for testing. The micro course is designed to introduce microprocessor technology to engineering, manufacturing, planning, and administrative personnel. A microprocessor training lab, designed to be used throughout the course for realtime hands-on experiments, consists of a portable self-contained microcomputer with a built-in keyboard and display, thermal and optical sensors, timers, motor, and communications interfaces. Both courses can be purchased or rented. **Integrated Computer Systems,** 3304 Pico Blvd, Santa Monica, CA 90405.

Circle 345 on Inquiry Card

Downloadable speech synthesizer board

Featuring high quality voice response synthesized from downloaded LPC speech parameters, SPEECH 1100 utilizes downloadable RAMs instead of programmed ROMs to temporarily store one of many 64k-bit speech data files stored externally. Each file contains approx 30 s of speech (about 40 words), compressed and encoded using linear predictive coding. Vocabulary files can be structured to contain an assortment of words or phrases suited for varying conditions or operational environments. The device does not have a permanently stored, application specific vocabulary. Additions or modifications to the vocabulary files can be made at the user's site or at the company's speech lab. Also included on the board are an 8085A microprocessor for control; a 10-bit DAC; a 7-pole, anti-aliasing, low pass filter; and a 2-W audio amplifier. Most MULTIBUS computers can be interfaced to the board; other micro/minicomputers can interface through the board's TTL parallel or RS-232-C serial ports. **Telesensory Speech Systems,** 3408 Hillview Ave, Palo Alto, CA 94304.

Circle 346 on Inquiry Card

Ternary slide switch

Switch features output code combinations of 9^3 in a package comparable to a std 2-position DIP switch. Miniaturized circuitry within the PCB DIP switch allows selection from 3 setting positions per station. The switch base has an antimigration seal to prevent flux wicking and ensure the integrity of the device during wave soldering operations. Max recommended switching load is 12 Vdc at 25 mA and max recommended nonswitching load is 50 Vdc at 100 mA. Switch operates at temperatures of −40 to 85 °C, with insulation resistance of 1000M Ω. Switch contacts are beryllium copper with 0.00001" (0.000254-mm) gold plate over nickel flash. **Stanford Applied Engineering, Inc,** 3520 De La Cruz Blvd, Santa Clara, CA 95050.

Circle 347 on Inquiry Card

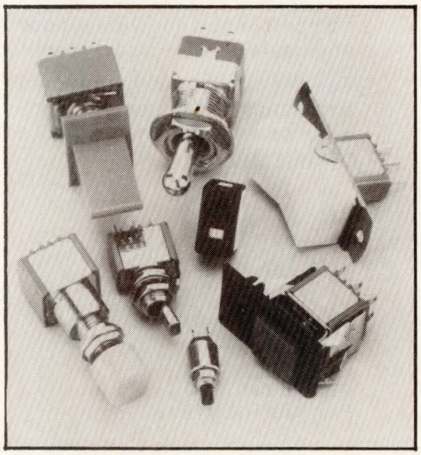
Manual RS-232 digital transfer switch

Model 1081-0005 spdt switch allows switching of modems between frontend processors, with an option for monitoring switched lines. The unit switches all 24 lines of an RS-232 connection; RS-422 switching is optionally available with appropriate hardware changes. Panel box version measures 3.5" x 2" x 4.5" (8.9 x 5 x 11.5 cm), and 3 rear 24-pin connectors and 2-screw mounting. It can be supplied as 8 units in a std 19" x 3.5" (48-x 8.9-cm) rack panel. A shelf or desk model adds 2" (5 cm) in width for stability. The monitor version adds a single RS-232 connector to the face of the unit. By cabling from this connector to any digital monitoring instrument, all switched lines can be monitored. **MarLee Switch Co,** 933-D N Central Ave, Upland, CA 91786.

Circle 348 on Inquiry Card

Miniature, subminiature, and microminiature switches

Available in toggle, rocker, paddle, pushbutton, and slide configurations, InterSpec™ switches meet International Electrotechnical Commission standards as well as UL, CSA, VDE, UTE, SEV, SEMKO, NEMKO, DEMKO, and Space Lab national certification agency requirements. Contacts on all switches are available in silver plating with various plating combinations and alloys to solid silver or gold; fine silver contacts are also available for reliability in low amperage/dry circuit applications up to 6 A, 125 Vac, or 3 A, 250 Vac. A protective shoulder at the bottom of the bushing provides a high torque load surface to protect the switch during installation. An operating lever pin in the sleeve eliminates damage in high abuse locations and prevents rotation. Sealing options are available for severe environments, including corrosion and moisture. Four basic configurations are available: 5000, 11000, 12000 and 21000 series toggles/S series immersible toggles; 7000 series rocker paddles; 8000, 9000, and 13000 series pushbuttons/micropushbuttons; and 25000 series slides. **Crouse-Hinds Co, Arrow Hart Div,** 103 Hawthorn St, Hartford, CT 06101.



Circle 349 on Inquiry Card

Metal oxide resistors

Metal oxide resistors in 1-, 2-, and 3-W capacities serve as alternatives to carbon, wirebound resistors. General purpose resistors have a resistance range from 0.22 to 150k Ω, with std tolerance of ±5%. Tempco is ±200 ppm/°C. Flameproof coating prevents burning under overload conditions. 1- and 2-W devices are compatible with automatic insertion equipment and are available on lead tape reel or cut and formed. **Stackpole Components Co,** PO Box 14466, Raleigh, NC 27620.

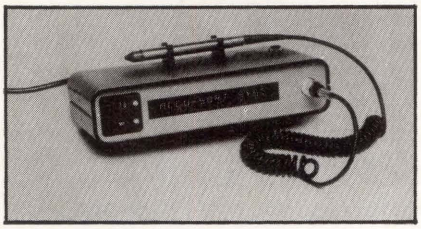
Circle 350 on Inquiry Card

Lightpen bar code reader

Model 4510 includes bar code reader, self-contained power supply, handheld lightpen and holder, and a 16-char, 0.375" (0.953-cm), alphanumeric LED display. Std features include switch-selectable baud rates, separate power-on and good read LED indicators, and a good read audible indicator with volume

(continued on page 226)

control and 2-tone selection. Bar code reader wand is supplied with 6′ (1.8 m) of coiled cable and quick disconnect, self-locking connectors. It is programmed to read codes 3 of 9 and interleaved 2 of 5, and will not smear or distort a label. Enclosed in heavy-duty plastic, the unit measures 2.25″ x 4.25″ x 9.875″ (5.72 x 10.80 x 25.083 cm) and weighs 3 lb (1.35 kg). The angle of each unit is adjustable over a 120° range to provide max visibility for all operators at distances up to 10′ (3 m) **Accu-Sort Systems, Inc,** 511 School House Rd, Telford, PA 18969.



Circle 351 on Inquiry Card

Subminiature PCB switches

Manufactured in toggle, rocker, and pushbutton versions, the Cutler-Hammer® T, Bor RK 8000 series of subminiature switches is designed for PCB use and is available in 7 circuit configurations. Terminal mounting options are available and all materials used in the switches are heat resistant, making them suitable for wave soldering operations. Toggle and rocker switches are made in either single- or double-throw with total actuator travel of 30°. Switching action is slow-make, slow-break butt contact. All conductive parts, including terminal and contact block, are silver or copper with gold plate for low contact resistance and high electrical life. **Eaton Corp,** 4201 N 27th St, Milwaukee, WI 53216.

Circle 352 on Inquiry Card

Digital delay modules

DL13 14-pin, TTL compatible, computer/military grade delay modules use a hybrid combination of passive, lumped-constant delay components, and an active input driver and output buffer. Circuit architecture also includes compensation for propagation delays and internal termination of the output. No external circuitry is required to achieve the required delay. With high delay accuracy (±5% or ±2 ns typical), and fast rise time (3 ns typical), the series can drive up to 10 TTL loads. Sixteen std delay times range from 25 to 1000 ns; others are available upon request. Op temp ranges are 0 to 70 °C (computer grade) and −55 to 125 °C (military grade). Screening options on military grade modules include IC or final product burn-in per MIL-STD-883. **Kappa Networks, Inc,** 165 Roosevelt Ave, Carteret, NJ 07008.

Circle 353 on Inquiry Card

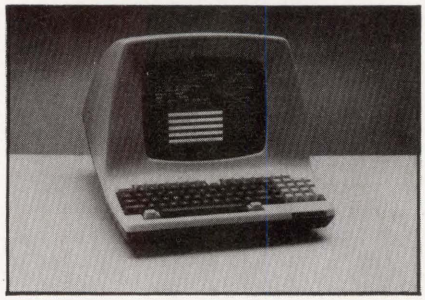
DC servo motor

Model 1410 high performance, permanent magnet dc servo motor is rated at 410 oz-in (2.87 N•m) continuous without cooling, with accelerations to 11,000 (rads/s)². Precision tolerances include output shaft to flange perpendicularity ±0.0015, encoder shaft perpendicularity ±0.0005, and end play held to ±0.0005. With 4 std motor and 3 tachometer windings, the unit is capable of high speed, low speed, plugging, and operation at stall. A tachometer option includes extended shaft and tapped holes for encoder. **Aerotech, Inc,** 101 Zeta Dr, Pittsburgh, PA 15238.

Circle 354 on Inquiry Card

PERIPHERALS

Smart video display terminal features microprocessor based design



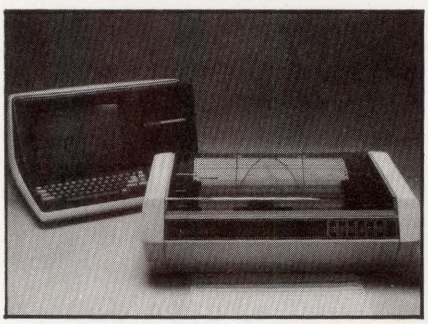
ADM 21 smart video display terminal features a microprocessor based design that allows modifications in firmware without hardware modifications. The company can tailor the terminal to meet specific functional requirements and emulate other popular video display terminals. Housed in the company's "clamshell" enclosure, the unit offers full editing capabilities, including clear screen, erase line/page, char insert/delete, and line insert/delete. Visual attributes include reduced intensity, inverse video, blink, blank, and underline. The terminal also provides conversation and block mode operation; 8 function keys with a shift capability to 16 functions; baud rates of 75, 110, 150, 300, 600, 1200, 2400, 4800, 9600, and 19,200 baud; X-ON/X-OFF; program mode; self-test; selectable steady or blinking cursor; and a combination extension/printer port.

The high resolution, 12″ (30-cm) nonglare screen features a green or white phosphor 80 x 24 display; 7 x 8 (9 x 11 field) char matrix with lowercase descenders; and user accessible contrast control. Keyboard features include Selectric typewriter layout; numeric keypad; cursor control, edit, line/page send, and auto-repeat keys; and a function mode key. A 32-char answer back memory, current loop operation, international char sets, function keycap set, and limited graphics are optionally available. **Lear Siegler, Inc, Data Products Div,** 714 N Brookhurst St, Anaheim, CA 92803.

Circle 355 on Inquiry Card

150-char/s dot matrix printer

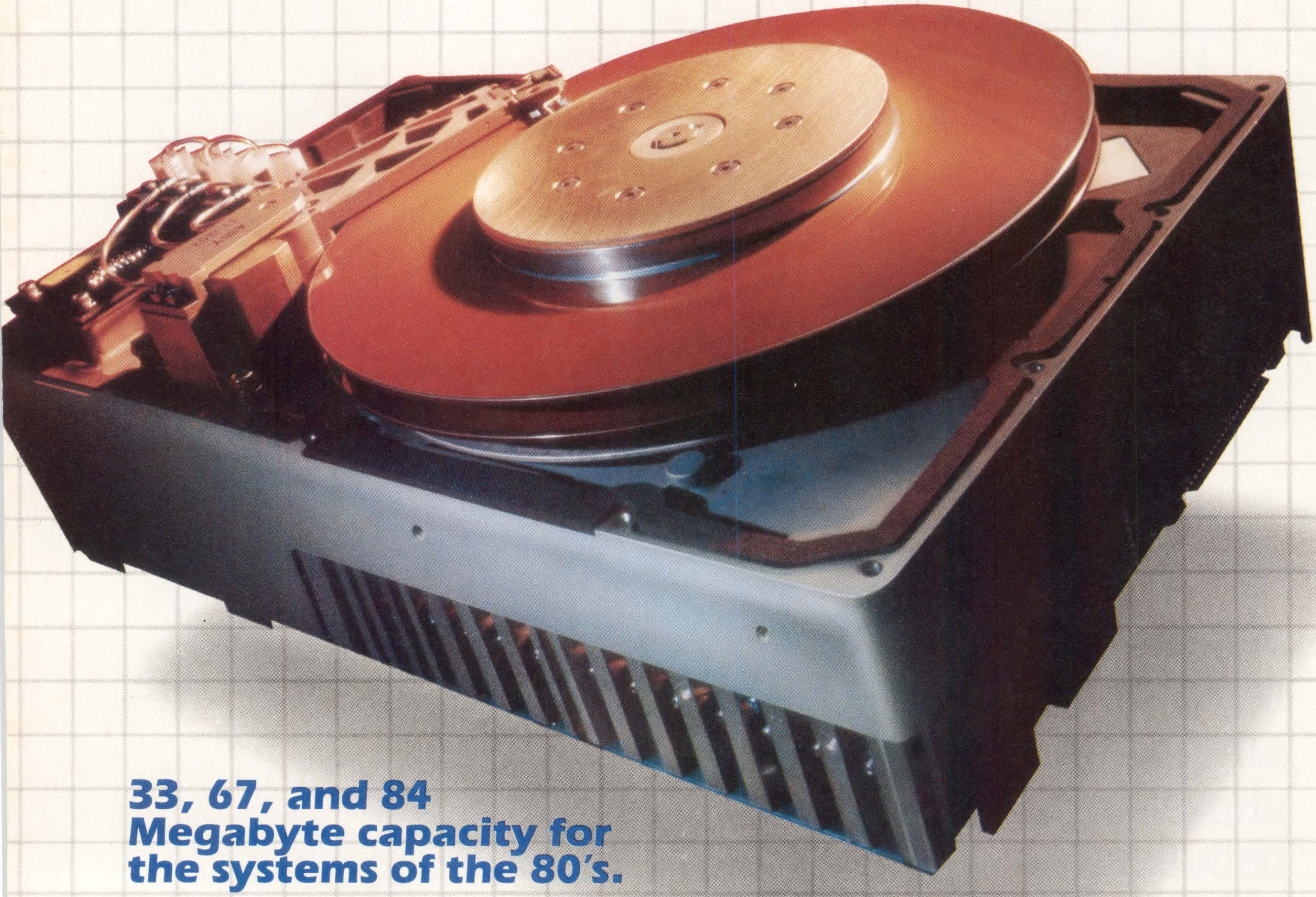
Model 4422 MPT/Printer, designed for use with the company's MPT/80 series intelligent workstations and MPT/100 technical desktop computers, features a full print line input buffer, 5-ips paper slew rate, 80- or 136-char print line lengths, and ribbon life expectancy of 3M chars. The printer's 9 x 9 pin dot matrix printhead allows the user to produce reports containing the full 96 upper/lowercase ASCII char set, with true risers, descenders, underlining, and boldface text. A printhead-to-platen distance adjustment lets users maximize print quality when using up to 6-ply print forms. An offline self-test feature allows the user to check printer operation, and isolate and correct problem sources before committing data to output. **Data General Corp, Technical Products Div,** 4400 Computer Dr, Westboro, MA 01580.



Circle 356 on Inquiry Card

Pertec's TrakStar™

a new family of 8-inch Winchester drives.



33, 67, and 84 Megabyte capacity for the systems of the 80's.

Proven design innovations make Pertec's TrakStar family of 8" Winchesters a must-see drive for business and word processing OEMs. Available now, TrakStar delivers the high performance, capacity and reliability OEMs are looking for in a compact, low-cost package.

TrakStar models offer capacities of 33, 67 and 84 megabytes so you can select the right size drive for your specific needs . . . economically, without compromise.

TrakStar offers ANSI standard interface to provide ease of integration, using industry-supported controllers. The rotary voice coil positioner, hard/soft sectoring and an 8-inch floppy form factor are part of TrakStar's unique combination of features that set it apart from the others.

Heads, disks and positioner are in the clean sealed section, with an unsurpassed 25,000 hours MTBF. The field-replaceable electronics are located outside of the sealed section, so that down time is virtually eliminated.

TrakStar is the proud result of Pertec Computer Corporation's commitment to perfecting technology. And it has a lot more to offer, because it's backed by the industry leader in OEM customer support.

For the full story, write for the new TrakStar literature.
Pertec Computer Corp., P.O. Box 2198, Chatsworth, CA 91311, or call (213) 999-2020.
In Europe, contact Pertec International, 10 Portman Road, Reading, Berkshire RG3 1DU. Tel. 734-582115.

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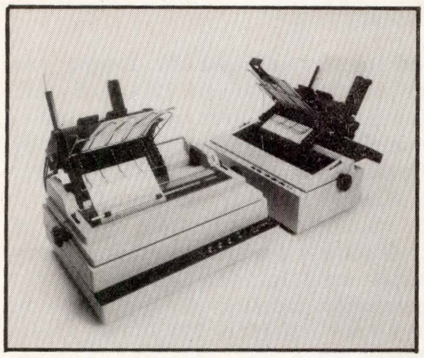
PERFECTING TECHNOLOGY

CIRCLE 141 ON INQUIRY CARD

Daisywheel printers



DY 211/ASF is a 20-char/s, low cost daisywheel printer, while DY 311/ASF is a 34-char/s high performance daisywheel printer. Both units offer bidirectional printing and an optional fully motorized feeding mechanism that loads up to 200 sheets and automatically recovers and reverses stacking. They also feature a 17" (43-cm) removable platen; 4 printing pitches; a 1k-byte buffer; and ribbon cartridges. Both have RS-232-C or industry std 50-wire interfaces; the DY 211/ASF adds 8-bit Centronics interfaces as well. **Olivetti OPE**, 505 White Plains Rd, Tarrytown, NY 10590.
Circle 357 on Inquiry Card

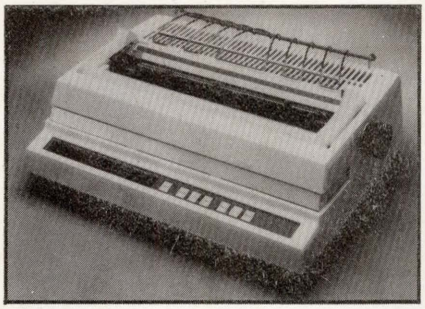
5.5" CRT monitor

VDP-572 incorporates all of the features of the VDP-58XS series. It measures 140 x 110.2 x 170 mm and weighs 1.2 kg, enabling it to fit easily into the std rack. The unit displays alphanumeric and graphics information as supplied by the 3 input signals (VS, HS, and video) that give more than 64 chars/16 lines. It also uses half the electron beam used by ordinary CRTs since it uses a large scale electronic lens. The display face can be angled from 0 to 23 degrees. A P31 green display is std; a P4 B/W display is optionally available. **Intertek, Inc**, Naito Bldg, 7-2-8 Nishishinjuku, Shinjuku-ku, Tokyo, Japan 160.

Circle 358 on Inquiry Card

Plug compatible printing system for IBM system 34/38 minicomputers

Printing system consists of a BDS LQ40 printer and a model IPI-34 interface housed in the printer. The bidirectional printer produces 40-char/s letter quality printing with 132-col spacing at 10 cpi, 158 col at 12 cpi, or 198 col at 15 cpi. Char spacing is switch-selectable. Max form width is 16" (40.6 cm); up to 6-part forms can be handled. Vertical spacing, under program control, is variable in 0.021" (0.053-cm) increments. Carriage speed is 400 ms for 132 col, while paper feed speed is 4 ips. The printer accepts interchangeable plastic and metal printwheels to provide a variety of fonts and languages. Metal wheels have 88, 92, and 96 chars, while plastic wheels have 96 chars. Options include a pin feed platen, uni- and bidirectional tractor feed, single- and double-tray sheet feed, and a dual-envelope tray. **BDS Corp**, 115 Independence Dr, Menlo Park, CA 94025.



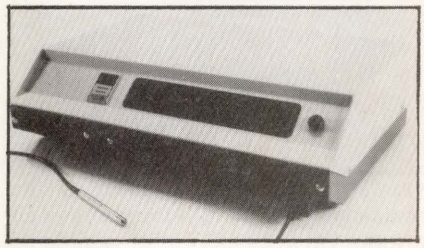
Circle 359 on Inquiry Card

Low cost desktop printer

Letterprinter 100 is the company's lowest cost desktop printer that features high speed impact dot matrix printing, draft copy mode, and graphics output, in addition to letter quality printing. Priced at $1495 in quantities of 100 and $2590 in single units, printer is targeted for OEMs using small sized systems and personal computers. It is suited as a companion printer for video terminals with local printer output facilities. Two font styles implemented in ROM are std; up to 3 ROM assemblies can be added for additional fonts. Chars/in, tab settings, printing speeds, and margins are selectable. Feed options are available. Universal power supply, EIA RS-232-C interface, and baud rates from 50 to 9600 are featured. **Digital Equipment Corp**, Maynard, MA 01754. Circle 360 on Inquiry Card

Bar code system

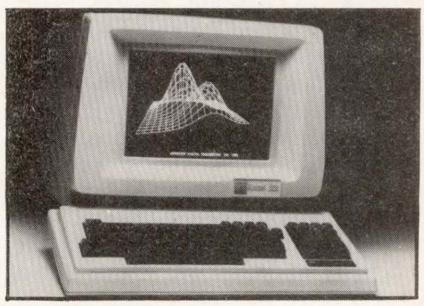
Telepen bar code system, composed of a fiber optics, bidirectional reader with std RS-232/V.24 interface, is claimed to be the only bar coding system that prints and reads the full ASCII char set. Its ability to read degraded bar codes and variable quality printing makes it effective in industrial or other applications where the printed bar code is susceptible to abuse.



Bar coded labels can be produced in the factory using simple dot matrix printers. **KPG Inc**, Cosmopolitan Ctr, Suite 204, 6075 Barfield Rd, NE, Atlanta, GA 30328. Circle 361 on Inquiry Card

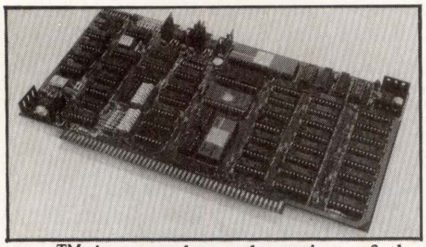
Monochromatic point to point graphics terminal

Excel 22G allows vector drawing, point plotting, arc drawing, and area fill; it also provides solid, dotted, and dashed lines and can define text by height, width, and line angle using either fixed or proportional spacing. A cross-hair cursor ensures higher accuracy in plotting points, and a lightpen is optional. The VT-100 compatible terminal offers a tiltable display, a choice of either a 12" or 14" (30- or 36-cm) nonglare screen, and a detachable typewriter style keyboard with separate numeric keypad on a 6' (1.8-m) coiled cable. Also std are split screen/regional scrolling, double-wide and double-high/wide characters, cursor addressing/sense functions, built-in self-test diagnostics, and a CRT saver that automatically shuts off the display when activity ceases. The unit's "works in a drawer" single logic board can be easily accessed without removing the enclosure hood. Terminal is compatible with most graphics software packages that utilize a Tektronix 4010 driver. **Datamedia Corp**, 7401 Central Hwy, Pennsauken, NJ 08109.



Circle 362 on Inquiry Card

Enhanced video board



VB3A™ is an enhanced version of the company's VB3 board; it incorporates all of the VB3's features plus additional operating features, as well as extended applicability to a wide variety of CRT/monitors. The board features a smaller, 6 x 7 upper/lowercase character EPROM that retains descenders while opening up the screen for more text. In one mode, the unit allows users a display of 24 lines x 80 chars on a std P4 phosphor monitor; a second mode adds a 25th line used for status updates. The EPROM also permits up to 50 lines x 80 chars to be displayed on a monitor having a P39 long persistence screen. The board provides positive-1 or negative-going horizontal and vertical synch pulses, and TTL level outputs; a 1-V pk-pk composite video signal is available as well. Level choice is jumper selectable. Software includes a CP/M compatible intelligent terminal driver (Televideo compatible) that permits the board to be used with many popular software packages. **SSM Microcomputer Products Inc**, 2190 Paragon Dr, San Jose, CA 95131.

Circle 363 on Inquiry Card

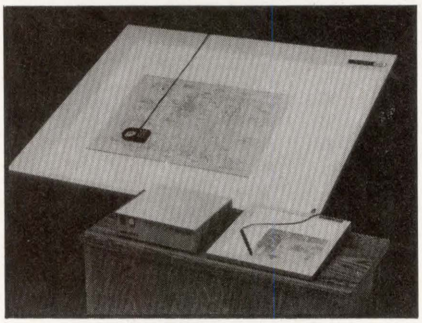
Card punch

Connecting directly to Data General's NOVA minicomputers, PC200/51 is claimed to be the fastest 80-col punch available for these systems. Card punching speeds range from 100 to 250 cards/min, based on the location of the last column punched. Card punch verification is accomplished through echo check error detection. A 100-card capacity reject stacker is provided for automatic selection of cards that do not pass the echo check verification. Control software for the unit is the same as for the Data General paper tape handler, ensuring compatibility with the company's operating systems. Included with the punch is an interface cable and controller board that plugs directly into the backplane of the NOVA. **Cardamation Co,** PO Box 746, Frazer, PA 19355.

Circle 364 on Inquiry Card

Digitizer tablets

9000 series tablets feature electromagnetic technology, allowing for digitizing from conductive material and more precise data input with greater data stability. Five tablet sizes are offered, ranging from 12" x 12" (30 x 30 cm) to 60" x 44" (152 x 112 cm). All are available in std and backlit surfaces and feature a 4-, 12-, or 16-button cursor with user definable keys or pen stylus. Digitizing accuracy is ±0.0105. The units have a resolution of 1000 lines/in (394/cm), repeatability of ±0.001, and can digitize at a rate of 200 coordinate pairs/s. The digitizer processing unit uses 8085A microprocessor technology for increased speed and flexibility. Switch-selectable output is dual-port RS-232-C or 16-bit parallel; IEEE 488 output is optional. Any or all of the interfaces can be used simultaneously. **California Computer Products, Inc,** 2411 W La Palma Ave, Anaheim, CA 92801.



Circle 365 on Inquiry Card

Programmable data entry terminal

Enabling new or existing computer systems to use bar coding for data collection and management, Series 7 terminal allows 2-way (full-duplex) communication between a mainframe and any number of remote workstations. It features a full alphanumeric keyboard, handheld stainless steel bar code scanner with either an infrared or red LED light source, 32-char dot matrix display, and std 16k storage capability. EPROMs can be programmed to perform specific task functions with screen readout. Alphanumeric bar code schemes supported by firmware include CODABAR, 3 of 9, UPC, EAN, five bar 2 of 5, and interleaved 2 of 5, MSI/Plessey. Terminal is capable of multicode or dual-code operation, uses a serial ASCII format, and has RS-232-C compatible signal levels. It operates on 115 V at 60/50 Hz or 220 V at 60/50 Hz. **Welch Allyn, Inc, Industrial Products Div**, Jordan Rd, Skaneateles Falls, NY 13153.

Circle 366 on Inquiry Card

80-col serial matrix printer

MT-120 160-char/s printer produces graphics, bar codes, and OCR, condensed or expanded characters, as well as correspondence quality text. Special plotting modes are available for both bit image control of dot placement and a selectable sequence of graphics chars for producing linear charts. The printer features interchangeable plug-in interface modules for friction, sprocket, or tractor paper drive. Operator or interface programmable functions include form feed instructions, change of line spacing or char pitch, underscoring, and horizontal/vertical tab settings. **Mannesmann Tally**, 8301 S 180th St, Kent, WA 98031.

Circle 367 on Inquiry Card

Intelligent printer

Designed to print shipping labels, std bar codes, and variable sized matrix chars, IPS-7000-A is available with parallel, RS-232 serial, and 20-mA current loop interfaces. Using a ballistic printhead,it bidirectionally prints a 64-char set in the std ASCII mode; Danish, German, Swedish, Swedish/Finnish, Spanish, and U.K. sets are optional. The printer handles forms lengths up to 12" (30 cm) through a rear or optional bottom paper feed. Paper motion is forward and backward. The unit has programmable vertical format and a dynamic platen with adjustable print density. It can print multipart forms up to an original plus 5 copies. Baud rates are available from 300 to 4800 baud. Standard features include selectable 6 or 10 lines/in (2.4 or 4/cm), self-test, and audible trouble alarm. **Dataroyal Inc,** 235 Main Dunstable Rd, Nashua, NH 03060.

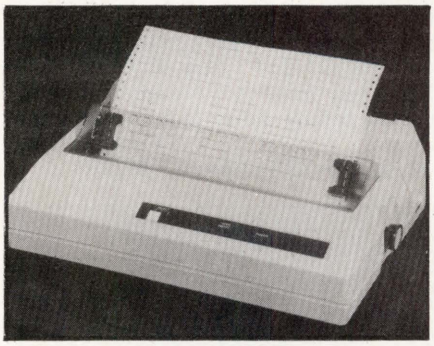
Circle 368 on Inquiry Card

Bidirectional daisywheel printer with Z80 based interface board

Combined with an Intek Integrator microcomputer based interface board, the Fujitsu SP830 daisywheel printer interfaces with Altos, Apple II, Xerox 820, TRS-80, IBM and Vector Graphic computers. The integrator board features 1k RAM (16k or 48k optional), RS-232 with 16 software or hardware selectable baud rates ranging from 50 to 19,200 baud, current loop, and Centronics parallel and IEEE ports. Software capabilities include automatic bidirectional printing, sheet feeder mode, and graphics mode. The printer is available with 127- or 96-char plastic or metal wheels. Maximum print speed is 80 char/s. **Intersell,** 465 Fairchild Dr, Suite 214, Mountain View, CA 94043.
Circle 369 on Inquiry Card

132-col desktop printer

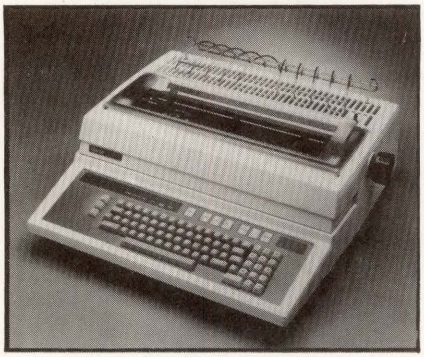
Model 152 features 150-char/s print speed; bidirectional, logic seeking printing; adjustable tractors; "clean hands" ribbon cassette; and top of form, compressed print that allows 132 cols to be printed in an 8" (20-cm) print line, or 216 columns in a 13.2" (33.5-cm) print line. It also provides self-test capability, 5-part forms capability, and a visual paper empty indicator. A complete character set modification guide is available that allows the OEM to modify or create personalized char sets on the printer. **Centronics Data Computer Corp,** Hudson, NH 03051.



Circle 370 on Inquiry Card

Computer Design invites you to write feature material about your development work. Send for our free Author's Guide. Circle 503 On Inquiry Card

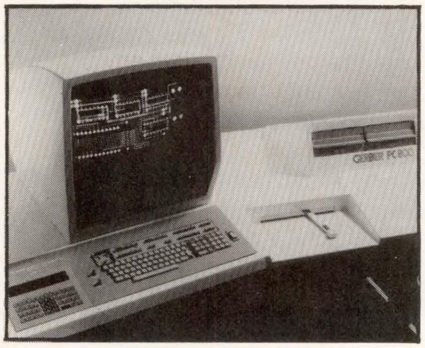
Keyboard send/receive printer/terminal



Model 630 KSR offers an RS-232-C serial interface, a 16-byte input buffer, an expanded 2688-byte print buffer, word processing firmware features, extensive diagnostics for host control, and transmission rates ranging from 110 to 9600 baud. The unit also offers 128 bytes of nonvolatile RAM with battery backup that provides up to a 31-char "here is..." message and operating parameters. Carriage and printwheel selection-related commands can be restored from the nonvolatile RAM via a remote reset. No reinitialization is required between power-offs. The printer/terminal is available with keyboards for APL, French, German, Norsk, or Scandinavian; all keyboards include a 10-key numeric pad. **Diablo Systems Inc, a Xerox Co,** 24500 Industrial Blvd, Hayward, CA 94545.

Circle 371 on Inquiry Card

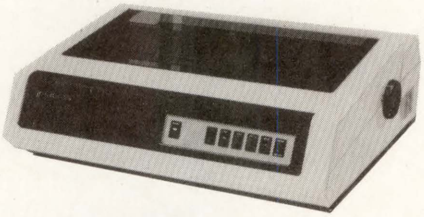
Color graphics option for PC-800 model 2 CAD system



PC-800 color graphics option is provided for creating PCB artwork and associated manufacturing aids. With the option, the PC-800 operator can work with up to 7 different colors on the system's 19″ (48-cm) color raster display. Up to 7 PCB layers can be simultaneously differentiated; each layer can be assigned a different color, and each color can be displayed independently. The designer can visually verify that feedthroughs have been correctly connected, pads and traces under a ground plane are properly placed, component outlines do not intersect, interferences do not exist, traces are centered in pads, drill holes have been properly placed, short or open circuits do not exist, and so forth. The option can be added to a PC-800 model 2 CAD system at a cost of $12,000. **The Gerber Scientific Instrument Co,** PO Box 305, Hartford, CT 06101.

Circle 372 on Inquiry Card

High speed serial matrix printer



Model 2350 prints subscripts, superscripts, and underlines, as well as 2-color printing, and operates bidirectionally at speeds of up to 350 chars/s. It combines short line seeking logic and fast horizontal and vertical slew speeds, increasing throughput to equal that of printers operating at higher char/s rates. Users with applications requiring 40 chars/line can expect a throughput of 340 lines/min. A 2k-byte input buffer is std, and a 9-pin stored energy printhead prints the full 96-char ASCII set. Two condensed and 3 double-width fonts are operator selectable. The 136-col printer accepts 6-part forms up to 15″ (38-cm) wide. The printer is offered with std Centronics and Dataproducts compatible parallel interfaces; RS-232-C and high speed parallel interfaces are also available. Options include 72- x 72-dot/in (28 x 28/cm) graphics and alternate char sets. **Okidata Corp,** 111 Gaither Dr, Mt Laurel, NJ 08054.

Circle 373 on Inquiry Card

Programmable terminals with diskette mass storage

Two 2950 models of programmable terminals offer flexible disk mass storage devices and memory extension up to 256k bytes, integrated digital cassette option, high resolution video display, national character sets, and supporting software. Disk storage options are single- and dual-drive units in 1M- and 2M-byte capacity using std 8″ media. Memory can be optionally expanded and treated as an addressable peripheral device. Communications capabilities include IBM 3270 BSC compatibility and BASIC program format. Asynchronous protocol (7-bit ASCII with strappable baud rates) and EIA RS-232-C communications are possible. A financial communication option permits device to transmit over inhouse communication link using digital concentrator protocols. Also featured are 7 x 9 matrix CRT display with 25 lines of 80-chars and character sets for 24 languages. **NCR Corp,** Dayton, OH 45479.

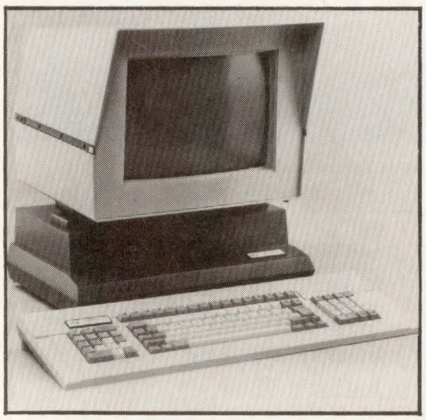
Circle 374 on Inquiry Card

Low cost, general purpose graphics terminal

Alpha Star I/O display terminal, priced at $465, is claimed to be the least expensive full-featured CRT currently available. Operator oriented features include tilting screen with a diffusing nonreflective bezel and a detachable keyboard, reverse video, foreground/background for forms, limited editing, programmable printer port, EIA RS-232-C or 20-mA current loop, built-in numeric pad, and 3 programmable function keys. **Emulog Inc,** 3730 Yale Way, Fremont, CA 94538. Circle 375 on Inquiry Card

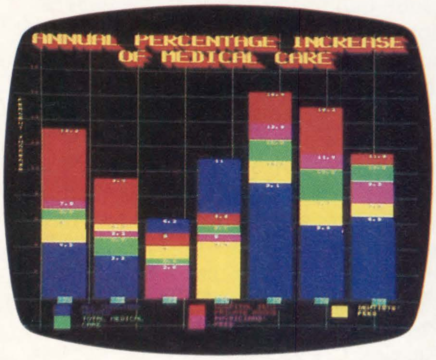
International spec CRT

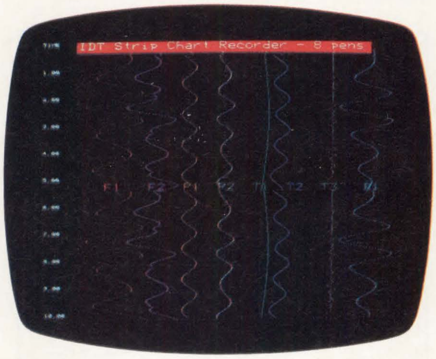
Series 80 Data Screen[R] terminal is designed to meet requirements of international ergonomics and can be customized to exact OEM specs. Display features include high resolution 15″ (38 cm) CRT screen, 256 chars displayable in 25 lines of 80 chars, horizontal and vertical split screen, and line graphics. Keyboard features include 16 programmable function keys, adjustable audible feedback, cursor editing keys, and 4 status indicators. **TEC, Inc,** 2727 N Fairview Ave, PO Box 5646, Tucson, AZ 85703.

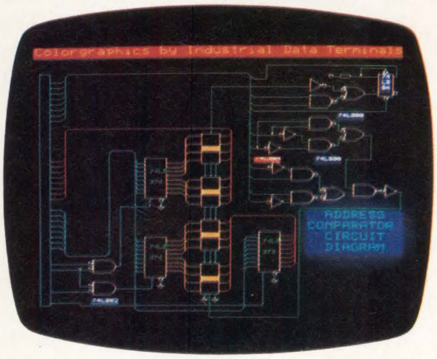


Circle 376 on Inquiry Card

Bubble Breakthrough





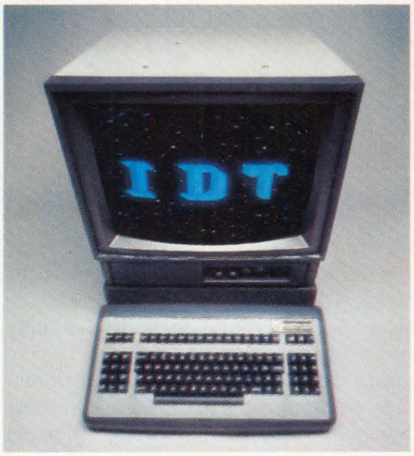


IDT 2200. First and only color graphics terminal with bubble memory!

The IDT 2200, with bubble memory storage in the terminal, establishes a new standard in color graphics capability and reliability. Non-volatile bubble memory allows you to retain permanent displays in the terminal, and ensures data integrity even in the harshest environment. Bubble memory unburdens your host computer of memory requirements and dramatically reduces transfer time to the terminal. With its increased megabit capacity, you can build and store permanently an entire library of pictures and subpictures in the terminal.

PLOT 10* software compatibility is now available. A new hardware vector generator draws vectors 10 times faster. New front access design permits easy maintenance, plus room for three full-color display memory planes.

IDT 2200 with bubble memory. The newest reason why we're earning a reputation for cost-effective performance in color graphics terminals.



- **Highly reliable. Ruggedly designed for long life and low maintenance in industrial environments.**
- **Non-volatile memory provides megabit capacity within the terminal for a library of pictures and subpictures.**
- **Rapid display of graphics with bubble and subpicture architecture stored within the terminal. High-speed, high-resolution presentation. 512 x 512 individually addressable pixels.**
- **Subpicture architecture, using BUBBLEPICS™, MACROGRAPHICS™ and VECPICS™, with auto-write and auto-erase capability, permits the creation of complex displays and high-speed animation with relatively simple programming.**
- **Terminal's intelligence allows simplified programming using high-level ASCII commands. Communications require no special handlers or drivers, just a standard RS 232 serial interface. Binary and 8-bit parallel inputs also available.**
- **Flexible packaging: rack mount, desk top or OEM configurations.**
- **Interfaces available for selected color or black and white printer/plotters.**

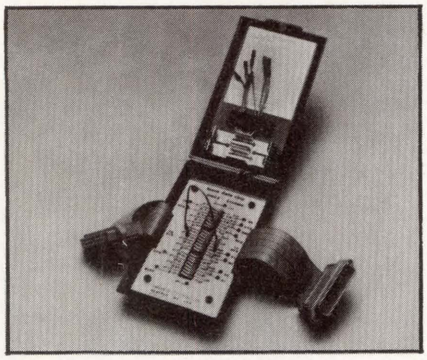
Customer-configured...performance-proven.

*A Trademark of Tektronix, Inc.

Industrial Data Terminals Corp.
173 Heatherdown Drive, Westerville, Ohio 43081 (614) 882-3282

CIRCLE 143 ON INQUIRY CARD

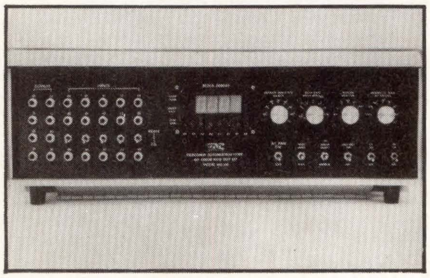
RS-232 I/O line tester



Pocket-sized device connects between the user's equipment and the communication line to differentiate 12 signals. Interface pins can be cross-patched with the tester's connection jumper wires to test and correct problems. LEDs monitor the following signals: TD (2), RD (3), RTS (4), CTS (5), DSR (6), DCD (8) TC (15), RC (17), DTR (20), SQ (21), RI (22), and busy (25). The tester uses a supplementary power supply from two 1.5-W penlight batteries to eliminate errors caused by power drain. An EIA/CCITT conversion chart is also included. **International Minicomputer Accessories Corp,** 2465 Augustine Dr, Santa Clara, CA 95051.
Circle 377 on Inquiry Card

Bit error rate test set

Model 316 bit error rate test set is designed for engineers working with optical fiber and coaxial cable data transmission systems at data rates up to 10M bps. Control ports of both transmitter and receiver allow dynamic testing of asynchronous or synchronous modems in multidrop half-duplex configurations. Networks sharing the same transmission medium can be tested while isolating system hardware and software elements. Features include RS-422 and TTL compatible I/O; NRZ formatted CCITT error codes of 63, 511, and 2047 bits; and internal transmit and receive clock generators ranging from 0.25M to 10M bps. **Telecomm-Automation Corp,** PO Box 473, Southbury, CT 06488.



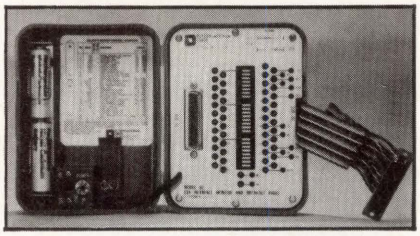
Circle 378 on Inquiry Card

ECL logic probe

LP-4 detects and indicates valid ECL logic levels using LED indicators for high and low levels. A third LED, labeled pulse, indicates the occurrence of single pulses as short as 3 ns and pulse trains with repetition rates up to 100 MHz min (150 MHz typ at 50% duty cycle). With the pulse LED on, the high or low LEDs indicate positive or negative polarity. The probe features a 2-position switch for pulse or memory (latch) mode selection. Constant input impedance is greater than 10 kΩ; input overload protection is ±100 Vdc continuous, ±220 Vdc transient, and 120 Vac for 30 s (to 1 kHz). Device measures 5.8" x 1.0" x 0.7" (14.7 x 2.5 x 1.8 cm), and is provided with a 1.5" (3.8-cm) long probe tip, 36" (91-cm) power and ground leads with alligator clips, and a series of BNC and wire wrap-in input adaptors. **Global Specialties Corp,** 70 Fulton Terr, New Haven, CT 06509.

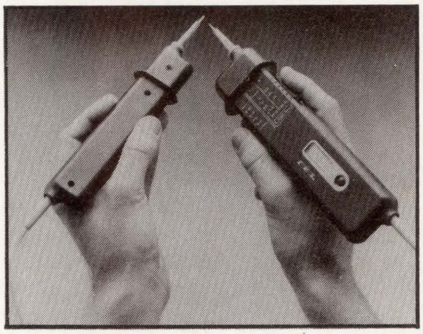
Circle 379 on Inquiry Card

Interface monitor and breakout panel



A pocket sized, portable test set rechargeable interface monitor, model 60 provides access to all 25 conductors of the EIA RS-232-C interface. Twenty-four switches allow all interface conductors except frame ground to be individually interrupted for simulating handshaking control signals and isolating terminal and modem signals. Twenty-five test points on each side of breakout panel provide access to EIA signals for test equipment probes. Twelve LEDs display key signals without interruption of signal path; 2 additional LEDs sense whether signal levels meet EIA specs. Small jumper cables are provided to allow cross patching and monitoring of signals. The self-contained monitor operates directly from 110 Vac during battery recharge. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865. Circle 380 on Inquiry Card

Handheld multimeter

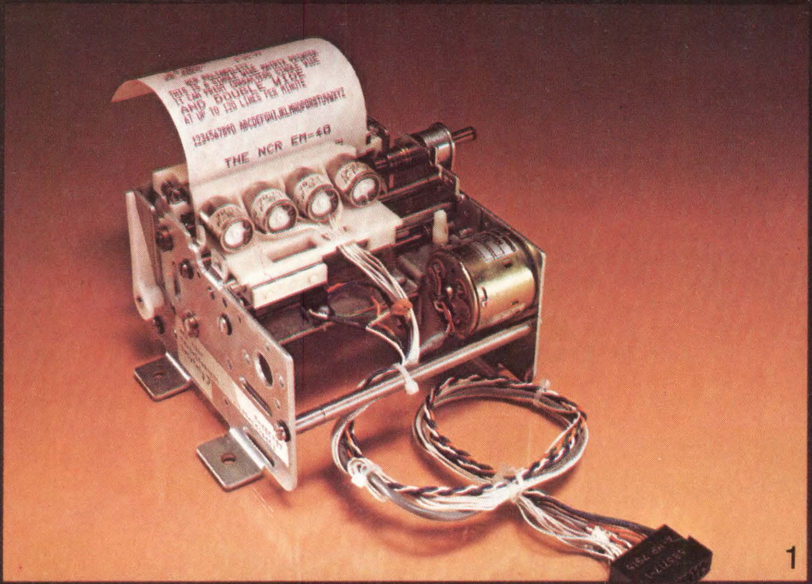


Steinel Digi-Check 3.5-digit handheld probe multimeter differs from conventional or pocket DVMs by utilizing 2 probe tips interconnected by a 1-m cable. Probes contain LCD, range and function selector slide switches, storage batteries, and battery charger. An additional pushbutton memory storage feature allows reading retention. Multimeter can be operated for 12 h max/charge, and can be recharged by any supply voltage between 110 and 240 Vac, 50 or 60 Hz. **Energy Electronic Products Corp,** 5441 W 104th St, Los Angeles, CA 90045.
Circle 381 on Inquiry Card

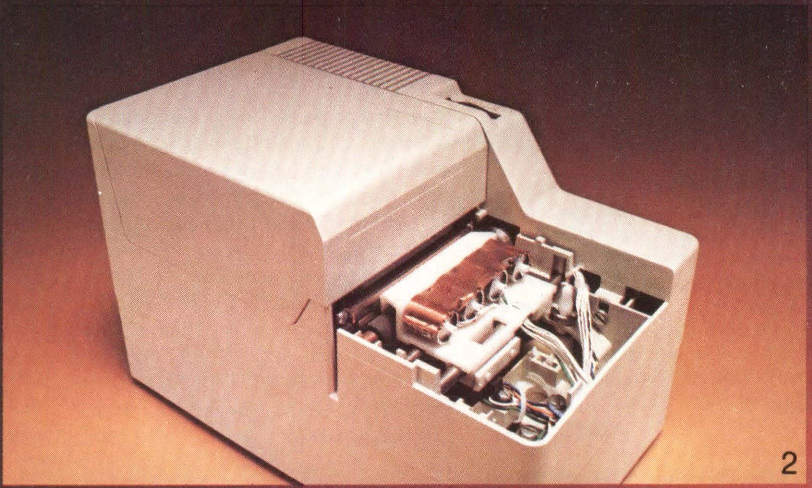
In-circuit digital PCB test system

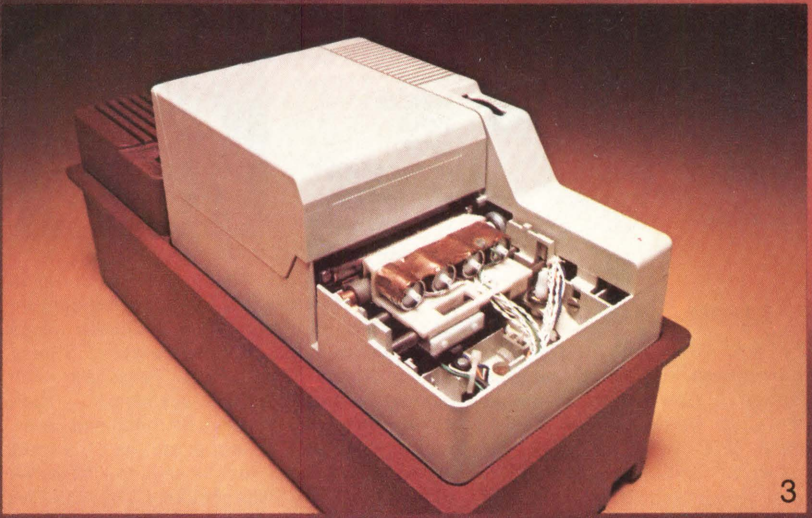
Model 3000C individually isolates and performance tests ICs installed on a digital PCB. It accurately detects marginally-operating devices, as well as shorted and defective ICs. The device automatically provides truth table function testing of discrete ICs at frequencies up to 150 kHz. Readout can be provided on a VDT, strip printer, or optional line printer. A keyboard offers operator interfacing. Driver and receivers are programmable for up to 40 test pins, permitting the testing of a wide variety of IC configurations. Driver and receivers are programmable for up to 40 test pins, permitting the testing of a wide variety of IC configurations. With the std unit, truth table functional tests can be performed on MSI and SSI devices, including TTL, RTL, DTL, and CMOS logic families. An ECL testing option is also available. **Fairchild-Testline Div,** 1400 White Dr, Titusville, FL 32780.
Circle 382 on Inquiry Card

NCR has a 40 column printer with NCR field proven reliability to match your application...



1


2


3

NCR's 40 column printers have been designed into many different products to satisfy a number of unique applications.

Shown here are:

1) the mechanism only for instrumentation data logging products *or* for those products where the printer must be totally integrated.
2) the cabinitized unit for POS systems where a mechanism is required but the product has not room for an integrated printer.
3) a freestanding unit with parallel or optional serial interface for remote printing in POS or data logging applications.

Not shown are slip printers and split platen printers similar to configuration 2. The list of options will take the standard unit and customize it to *your* specific system needs.

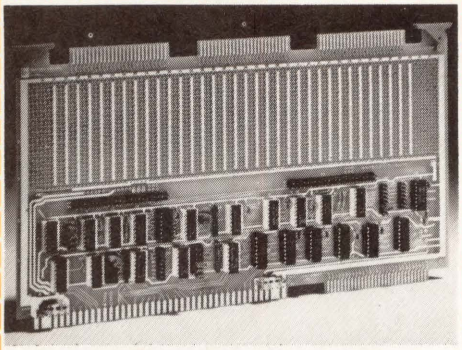
For information on 40 column printers, 80 column printers, and CRTs, contact:

NCR-OEM Marketing
P.O. Box 627
Ithaca, New York 14850-0627
Telephone: (607) 273-6066
Telex: 932406

NCR
OEM Marketing Division

...take your pick.

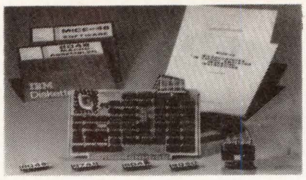
CIRCLE 144 ON INQUIRY CARD



MULTIBUS™ INTERFACE & PROTOTYPE

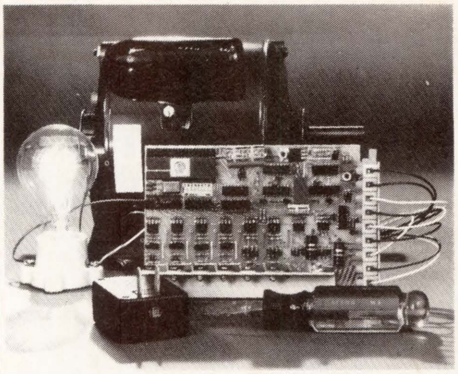
Prototype QUICKLY and EASILY. 100% of Multibus interfacing circuitry included. 20-bit Address, 8/16-bit Data. Delivery from stock. Multibus™ Intel Corp, Model# PR 80A, Price: $355 each. **ELECTRONIC SOLUTIONS,** 5780 Chesapeake Ct, San Diego, CA 92123. Tel: Toll Free (800)854-7086, In California (714)292-0242, TLX 910-335-1169

CIRCLE 475



8048 IN-CIRCUIT EMULATOR

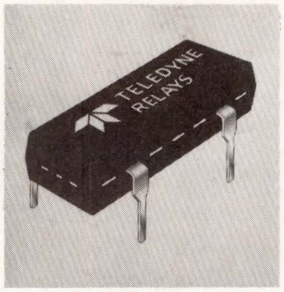
IEEE-696 (S-100), CP/M compatible. Emulates 8035, 8039, 8048, 8049, 8748, 8040, 8050, and 80C48 CMOS. Hardware Breakpoints allow Real Time Emulation up to 11 MHz. Trace includes disassembled code. Display/Modify Program & Data Memory, Registers, I/O Ports & Flags. Disassembler. Scope trigger from breakpoint locations. MICE-48 comes on one S-100 board with a 3 ft. cable and buffer assy. that plugs into the user's uP socket. The board with all supporting software is $995. For 8048 MACRO Assembler add $150. **SIGNUM SYSTEMS,** 726 Santa Monica Blvd, Santa Monica, CA 90401. Tel: (213)451-5382 **CIRCLE 478**



6801 MICRO CONTROL SYSTEM

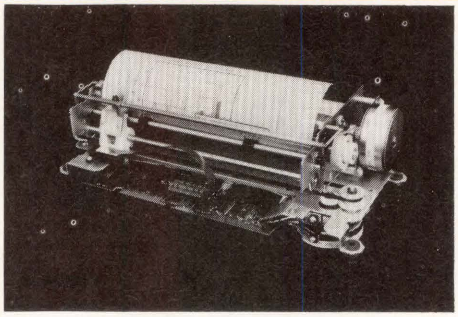
Analog and Power Control I/O.....in a Single Board Computer, 6801 or 68701 MPU with 2K ROM or EROM, 128 RAM, timer. 8 12-bit analog inputs, 8-bit analog output, 8 AC or DC inputs or outputs, serial I/O, digital I/O, watchdog timer, power supply. **WINTEK CORPORATION,** 1801 South St, Lafayette, IN 47904; Tel: (317) 742-8428 **CIRCLE 481**

SOLID STATE AC/DC RELAY



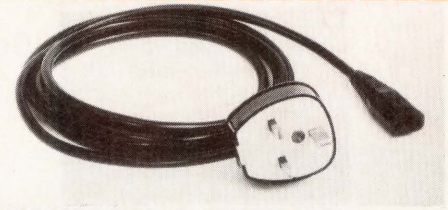
Teledyne's 640-1 is a solid state pin compatible replacement for DIP reed relays where higher reliability and long life are required. Switches AC or DC up to 50V. Low on-resistance is 2 ohms. Control voltage range is 3.8 to 10VDC. Transformer coupling provides 1500(P-P) isolation, low off-state leakage, & high switching speed. Employs hybrid microcircuits in TO-116 DIP. $6.15 ea for 5000 pcs. **TELEDYNE RELAYS,** 12525 Daphne Ave, Hawthorne, CA 90250. Tel: (213)777-0077

CIRCLE 476



QUIET & FAST

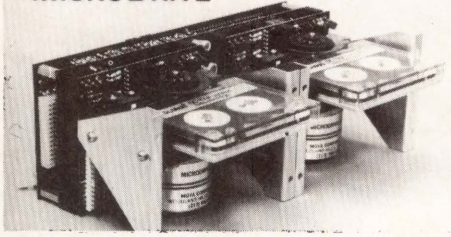
If you thought our Q3 was a durable, reliable and quiet thermal printer mechanism, just wait 'til you hear about the new Q160 ● 160 cps ● high resolution plotting ● 80/132 columns ● 2-4K buffer ● parallel/serial interface ● bidirectional printing ● upper/lower case, descenders ● APL, custom fonts ● 4½ pounds. **COMPUTER DEVICES,** 25 North Avenue, Burlington, MA 01803. Tel: (617) 273-1550. **CIRCLE 479**



INTERNATIONAL CORDS AND CORDSETS

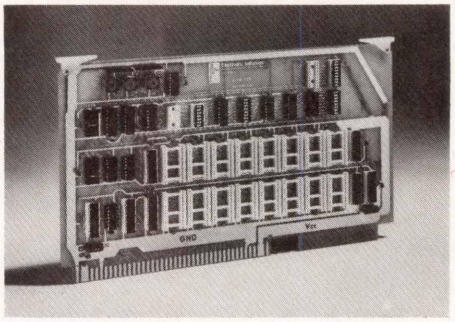
Standard cords for use in European countries, Australia, U.S. and Canada are available from stock or with shorter delivery times than custom cords. Cords have approvals at VDE, SEV, SEMKO, and other national test agencies as well as CSA certification and UL listings. Power supply cords can be installed permanently; cordsets with CEE-22 connector are detachable. Bulk cordage is available in sizes 3 x 0.75 mm², 3 x 1.0 mm², and 3 x 1.5 mm². **PANEL COMPONENTS CORP.,** P.O. Box 6626, Santa Rosa, CA 95406. Tel: (707) 523-0600. **CIRCLE 482**

MICRODRIVE



MicroDrive (TM) TAPE CARTRIDGE DRIVE SYSTEMS DESIGNED FOR OEM'S

Rugged, all metal, patented main plate assures precise head to tape interface for DC100A cartridge interchange. Compact units (2 Drives) with control and formatting circuits use only 8" by 3" of panel space. RS-232 and parallel I/O are available. Modular design allows distributed packaging in tight terminal applications. Call or write for OEM pricing and full specs. **MOYA CORPORATION** 9001 Oso Ave, Unit B, Chatsworth, CA.91311. Tel: (213)700-1200 **CIRCLE 477**

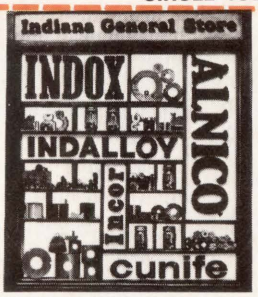


MULTIBUS™ EPROM BOARD

32k with 2716's, 64k with 2732's or 2532's. 20-bit Address, 8/16-bit Data. Easy address selection. Delivery from stock. Multibus™ Intel Corp, Model# PROM-32/64, Price: $395 each. **ELECTRONIC SOLUTIONS,** 5780 Chesapeake Ct, San Diego, CA 92123. Tel: Toll Free (800)854-7086, In California (714)292-0242, TLX 910-335-1169

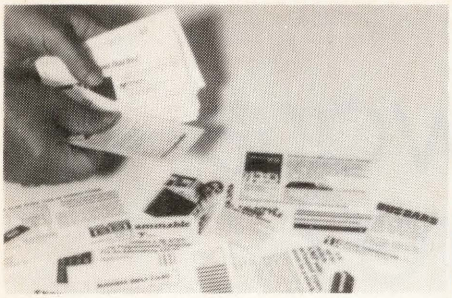
CIRCLE 480

WHEN YOU NEED PERMANENT MAGNETS



...Come to the INDIANA GENERAL STORE for high energy cast Alnico ... Sintered Alnico for small, intricate shapes ... Economical Indox® Ceramic magnets ... Cunife close tolerance stamped or formed parts ... Space-saving Incor® Rare Earth Materials with highest energy product available ... High quality Indalloy® formed or machined in intricate parts. Ask for complete file of current permanent magnet technical data. **INDIANA GENERAL — MAGNET PRODUCTS,** 405 Elm St., Valparaiso, IN 46383 (219)462-3131.

CIRCLE 483



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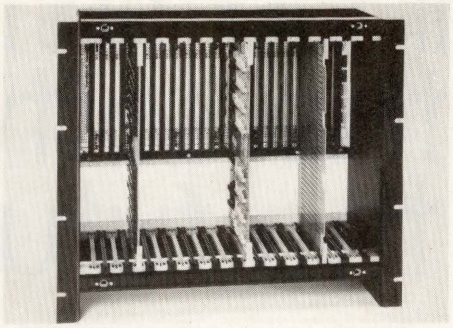
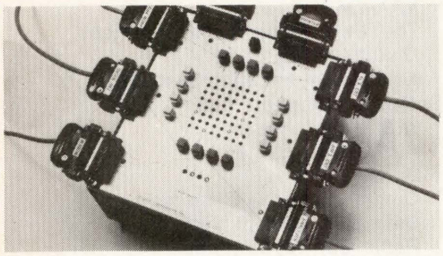
Here's a way for your company to test new product acceptance, offer catalogs, find new applications, or support ongoing product lines. *Computer Design's* POSTAL MAILERS go to our 70,000 domestic subscribers 4 times each year. Rates start at $895 per card and go down with frequency.

Contact Maureen Sebastian, **COMPUTER DESIGN,** 11 Goldsmith St., Littleton, MA 01460. (617) 486-8944. **CIRCLE 484**



RACK MOUNT MULTIBUS™ CAGES

Now you can assemble Multibus systems for rack mounting applications with a minimum of mechanical design effort. The 15.75" high units are available with up to 26 card slots complete with backplane and power supply connections. Multibus™ Intel Corporation. **ELECTRONIC SOLUTIONS,** 5780 Chesapeake Ct, San Diego, CA 92123. Toll Free: (800)-854-7086. In Calif. (714) 292-0242. **CIRCLE 487**



RS232 DATA SWITCHING MATRIX

· Implements every possible connection between Tx Data and Rcvd Data for eight I/O ports.
· Manual Control and connection monitoring via built in key array and 8 × 8 LED display.
· Non-volatile memory for 16 connection arrangements.
· 20 ma, RS232, or TTL may be mixed.
· Remote selection via parallel TTL interface.

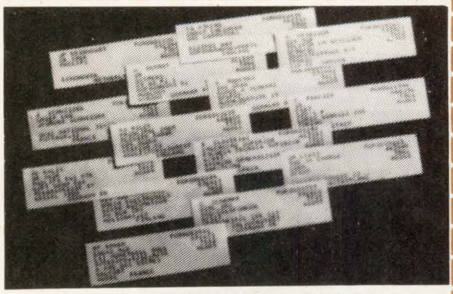
$995 (1-4, USA only), **DIGITAL LABORATORIES,** 600 Pleasant St., Watertown, MA 02172. 617/924-1680.

CIRCLE 485

Digi-Data's cartridge drive is plug compatible with DEI's funnel drive and it's more reliable at lower cost.

CONTACT: DIGI-DATA CORPORATION
8580 Dorsey Run Rd.
Jessup, MD 20794
(301) 498-0200

CIRCLE 488



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CIRCLE 489

Microcomputer analog I/O systems
Analog I/O systems for microcomputers are featured in 288-p catalog that gives specs for products from modular subsystems to fully integrated data acquisition systems. **Data Translation,** Marlboro, Mass.
Circle 390 on Inquiry Card

Matrix control and switches
Two brochures describe 3919 intelligent matrix control and direct access storage device matrix switches used with IBM or plug compatible mainframe systems. Send letterhead request to **T-Bar Inc, Sales Support Dept,** PO Box T, Wilton, CT 06897. Circle 391 on Inquiry Card

Technology overview
Publisher's 1982 catalog covers current issues in computer technology, computing for management and business, and computer applications in education. Technical books are reviewed. **Digital Equipment Corp,** Bedford, Mass.
Circle 392 on Inquiry Card

Electrostatic printer/plotter
Speed, format, resolution, character sets, and software of V-80 electrostatic printer/plotter are discussed in 8-p color brochure. **Versatec, A Xerox Co,** Santa Clara, Calif.
Circle 393 on Inquiry Card

Printer series
Brochure with data storage configurations profiles TermiNet[R] 200 printers, including line printer, keyboard send/receive, receive only, split platen, forms access, and APL/ASCII models. **General Electric Co, Data Communications Products Dept,** Waynesboro, Va.
Circle 394 on Inquiry Card

Insulation displacement connectors
Catalog lists complete line of insulation displacement connectors with performance specs, material finish, and assembly diagrams. Use of GTH™ contact system for mass storage terminations is described. **Burndy Corp, Components Div,** Norwalk, Conn.
Circle 395 on Inquiry Card

Composite product listing
Composite 200-p catalog documents DACs and ADCs, op amps, voltage references, analog switches and multiplexers, and dual transistors. **Micro Power Systems, Inc,** Santa Clara, Calif.
Circle 396 on Inquiry Card

Switching power supplies
Switching power supply catalog details electrical and mechanical specs for switching power supplies, including complete case and I/O configurations. **Power General,** Canton, Mass.
Circle 397 on Inquiry Card

Power conversion/switching products
Power conversion equipment, including high power linear voltage regulators, switching transistors, min parts count, and system applications. **Lambda Electronics,** Melville, NY.
Circle 398 on Inquiry Card

Packaging/connector system
Spec charts, diagrams, and environmental tests results detail 64-quad inline package (QUIP) that combines high lead count microprocessors and peripheral ICs on 2-sided boards. **3M,** St Paul, Minn.
Circle 399 on Inquiry Card

Power line protectors
Glitch Guard power line conditioning equipment is described in brochure that addresses power fault detection, corrective measures, and equipment installation. **TII Electronics Div,** Copiague, NY.
Circle 400 on Inquiry Card

Universal touch screen
Specs, applications, and operating principles for Touch Screen digitizer are contained in illustrated brochure; flexibility for small business and home computer use is discussed. **TSD Display Products, Inc,** Bohemia, NY.
Circle 401 on Inquiry Card

Brushless dc spindle motor
Spec sheet outlines JDBH-3250 dc spindle motor designed for 5.25″ and 8″ Winchester memory disk drives, with hubs for 1, 2, or 3 disks. **Clifton Precision, Litton Systems, Inc,** Clifton Heights, Pa.
Circle 402 on Inquiry Card

Conductor cables
Centerline round conductor flat cables in 0.050″, 0.100″, and 0.156″ dimensions are detailed in bulletin. **Panduit Corp,** Tinley Park, Ill.
Circle 403 on Inquiry Card

Display products
Applications and specs for gas discharge display systems, including std, custom, alphanumeric, and modular alphanumeric systems, are detailed in 16-p catalog. **Cherry Electrical Products Corp,** Waukegan, Ill.
Circle 404 on Inquiry Card

Current interface and modem/terminal analyzer
Wallet size cards and stick-on labels outlining Bell 301/303 current interface charts pin assignment, mnemonic names, and signal flow and function. Model 60 (Blue Box) terminal interface pocket analyzer cards are also available. **International Data Sciences, Inc,** Lincoln, RI.
Circle 405 on Inquiry Card

Electronic components
Catalog highlights complete line of electronic packaging hardware, and components, including edgeboard PC connectors, hood assemblies, Multi-Term™ connectors, IC sockets, mounting boards, emi filter, logic panels, and back panels. **Stanford Applied Engineering, Inc,** Santa Clara, Calif.
Circle 406 on Inquiry Card

Data conversion products
Hybrid and discrete data conversion products including A-D, D-A, S-D and R-D converters are cited in shortform catalog, along with bus amplifiers, transformers, and synchro instruments. **ILC Data Device Corp,** Bohemia, NY.
Circle 407 on Inquiry Card

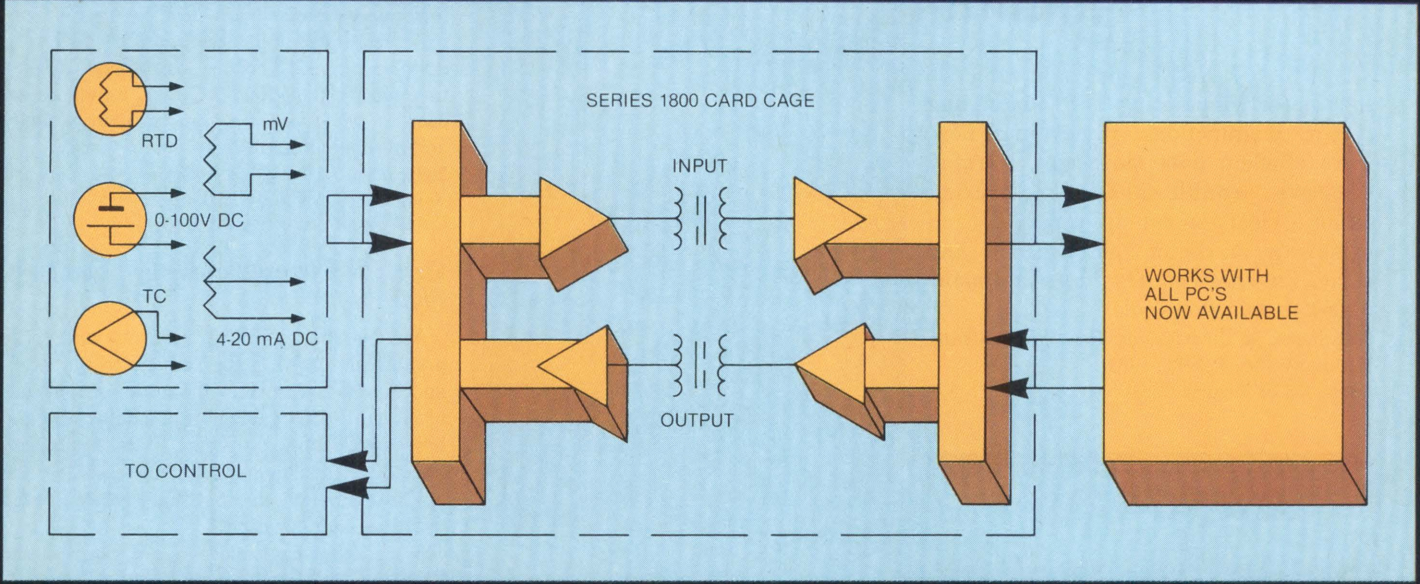
Statistical multiplexers
Brochure describes Supermux[R] 680 statistical multiplexer family, outlining cost effectiveness, diagnostic diagrams, and system specs. **Infotron Systems Corp,** Cherry Hill, NJ.
Circle 408 on Inquiry Card

Printed circuit connector series
V-CON PC connector series is described in product bulletin, detailing MIL specs, configurations, and ordering info. **Viking Connectors Inc,** Chatsworth, Calif.
Circle 409 on Inquiry Card

80M-byte Winchester drive
Brochure outlines performance, error rates, compatibility, recording specs, and positioning characteristics of model 5380 80M-byte Winchester disk drive. **Kennedy Co,** Monrovia, Calif.
Circle 410 on Inquiry Card

Power supply catalog
Full line of power supplies that provide outputs from 1 to 200 V, to 60 A and new line of redundant output systems is offered in catalog. **Acopian Corp,** Easton, Pa.
Circle 411 on Inquiry Card

PC users - Here's your economical solution to analog input problems:

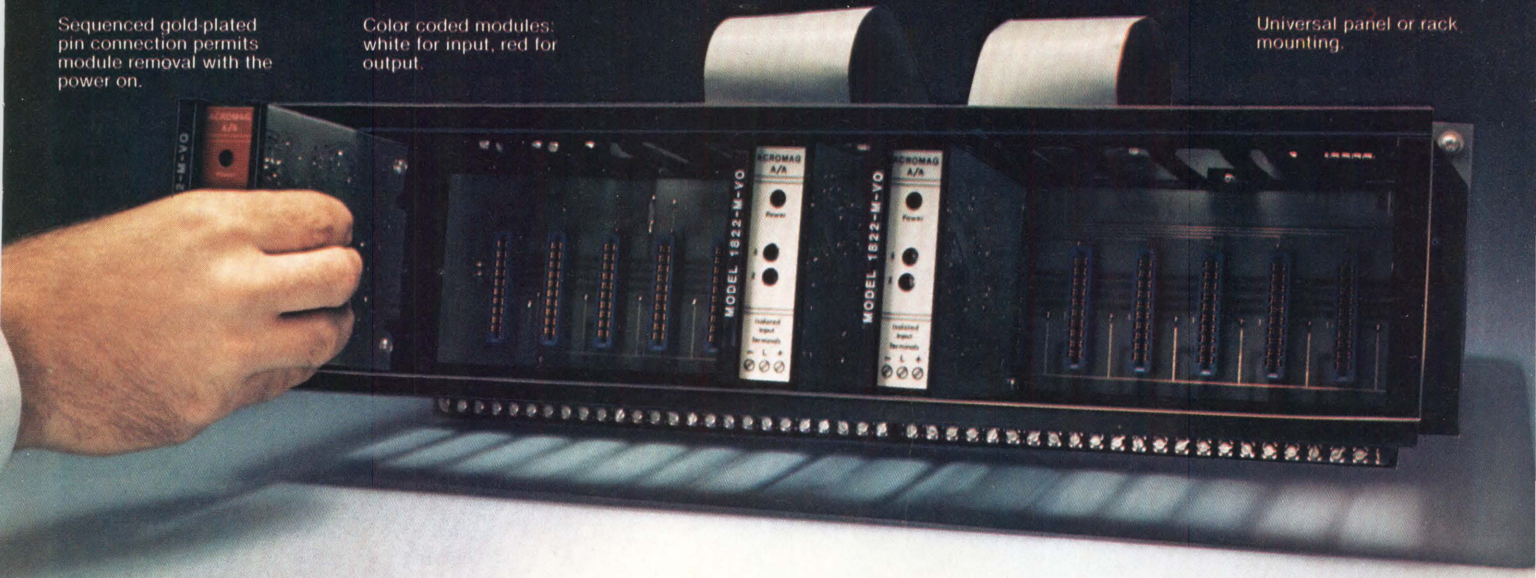


The rugged Series 1800 Signal Conditioner

Sequenced gold-plated pin connection permits module removal with the power on.

Color coded modules: white for input, red for output.

Universal panel or rack mounting.



Built-in thermocouple termperature references.

Plug-in slots provide flexibility to interchange modules with no effect on field wiring.

LED status indicators.

Rugged screw terminals for field wiring.

If your control system requires interfacing non-linear signals with your PC, or if isolation of input or output signals is causing you problems, then look into Acromag's Series 1800 System—specifically designed for PC and computer users who must marry the real world of analog signals and controls to PC's, microprocessors, and computers.

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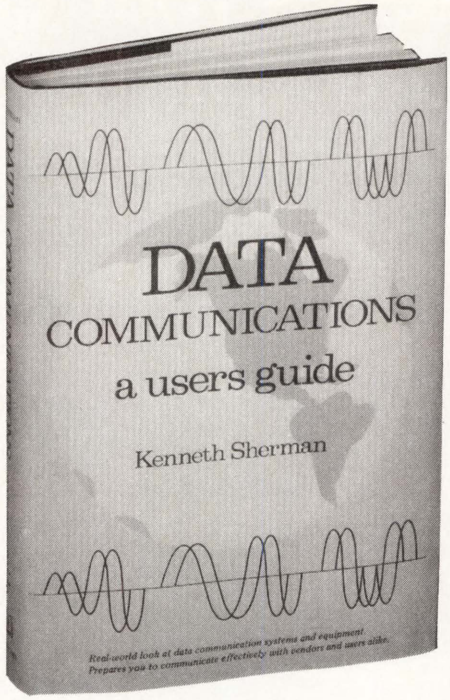

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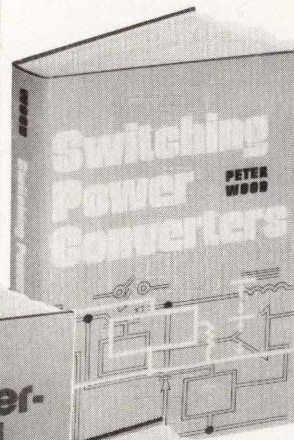

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280 pages; 6 x 9; 128 illustrations; Van Nostrand Reinhold; $24.95. July, 1981.
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Data Base Architecture by *Ivan Flores, Ph.D.*

This is the definitive guide to data base organization, giving the answers to the why's and how's. It describes the structure and use of information organized into a data base, and how application programs, data structures, data base management systems (DBMS), the operating system, and hardware relate to each data base organization.

408 pages; 295 illustrations; 6 x 9; Van Nostrand Reinhold; $26.50. July, 1981.
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464 pages; 142 illustrations; 6 x 9; Van Nostrand Reinhold; $26.50. May, 1981.
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The Software Legal Book by *Paul S. Hoffman.*

Written by a practicing attorney and CDP holder in non-legal terms. Covers: Protection of proprietary software, ownership of software and modifications, defining deliverables, basic contract provisions, warranties, excusable delays, special contract situations, bundled systems, third party leasing, arbitration, and developing software from contracts.

179 pages; L.L. bound; Carnegie Press; $59.95. 1981. Circle 459 on Inquiry Card

Computer-Assisted Data Base Design by *George U. Hubbard.*

This book not only thoroughly explains the theoretical aspects, but also provides explicit directions on all data base design procedures. In addition to a practical design methodology it discusses the ways to automate the major portions of this methodology. However, all of the techniques can be utilized without computer assistance.

320 pages; 123 illustrations; 6 x 9; Van Nostrand Reinhold Data Processing Series; $24.95. August, 1981. Circle 460 on Inquiry Card

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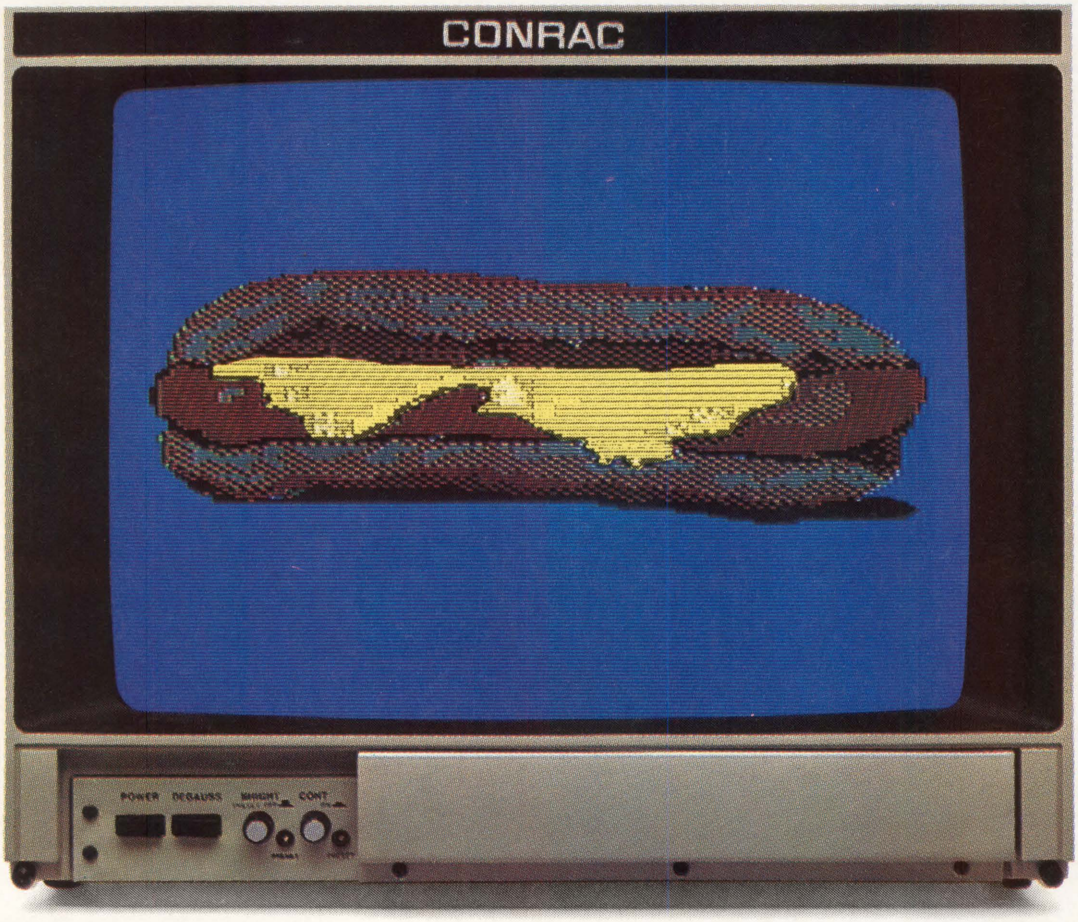

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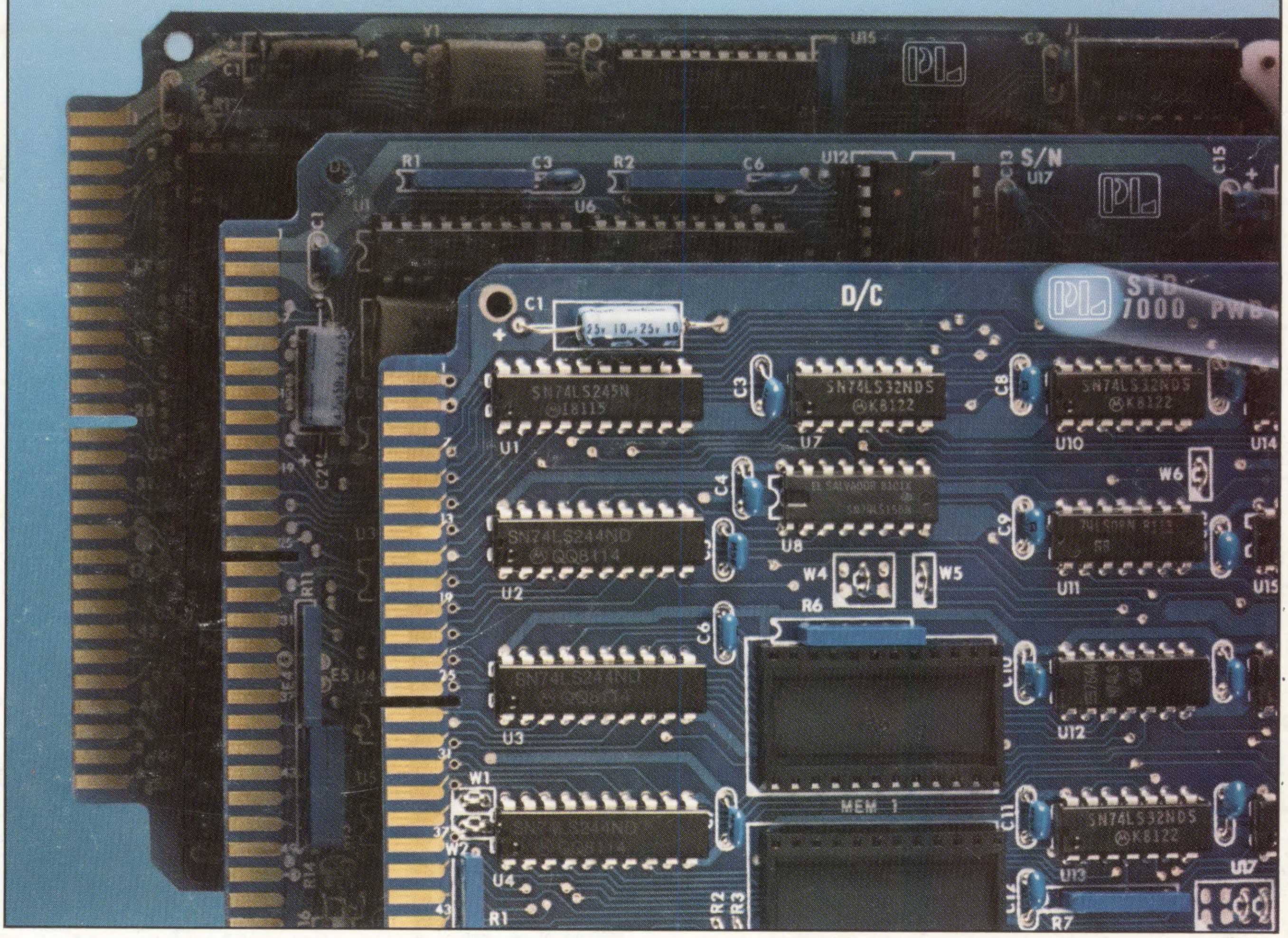

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