A PENNWELL PUBLICATION

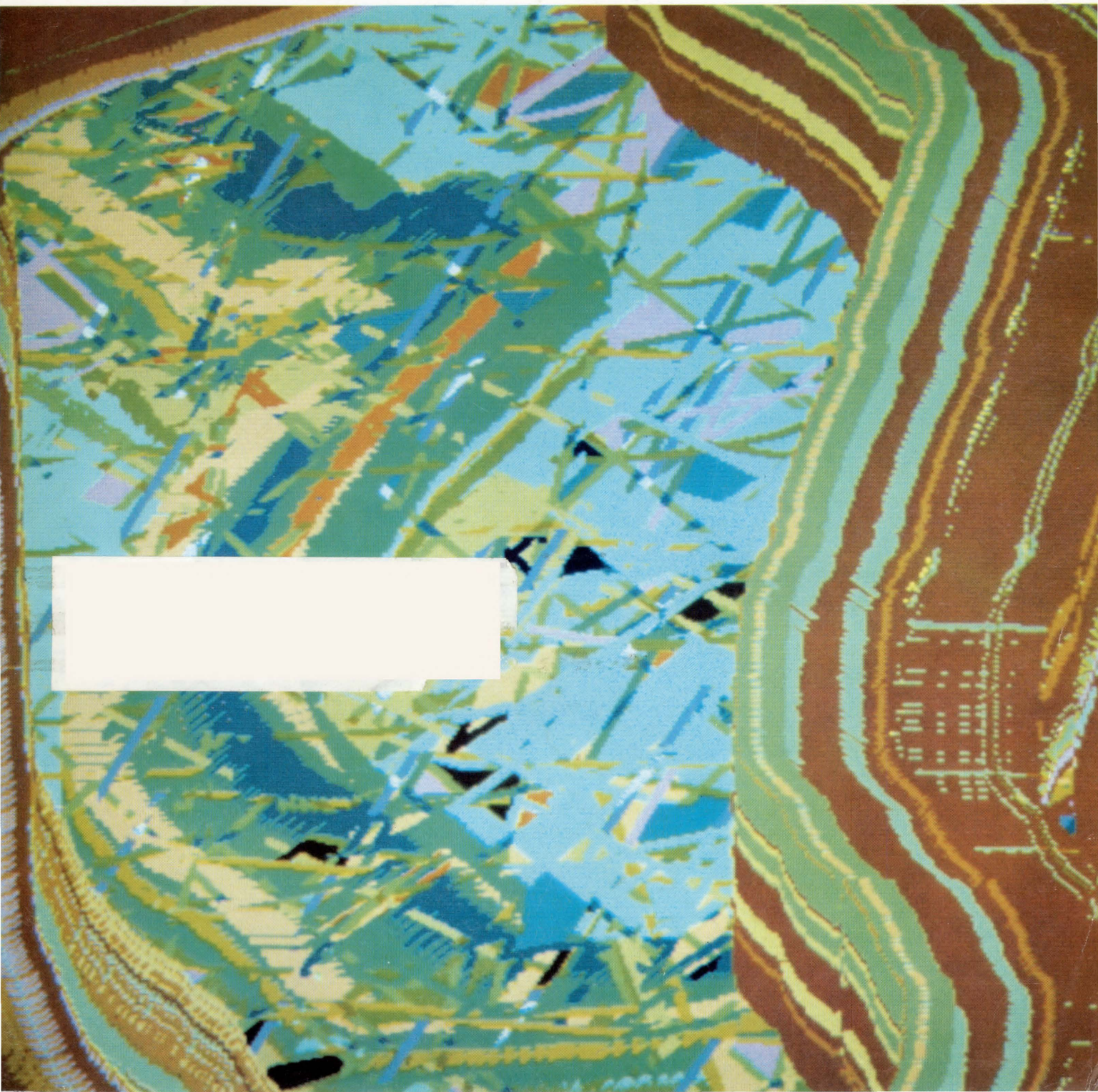
COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

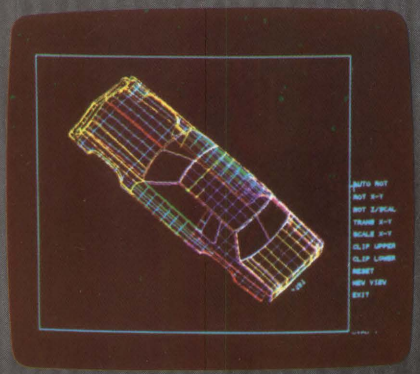
JANUARY 1981

32-BIT MINICOMPUTER ACHIEVES FULL 16-BIT COMPATIBILITY

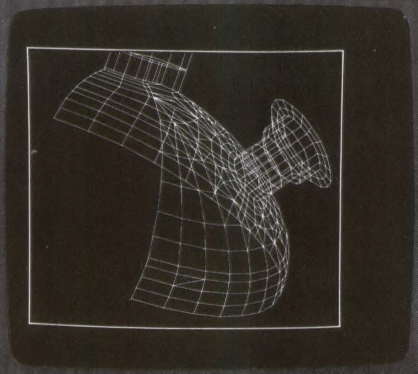
LOGIC ANALYZERS CONQUER LSI COMPLEXITY



Freedom of Expression.

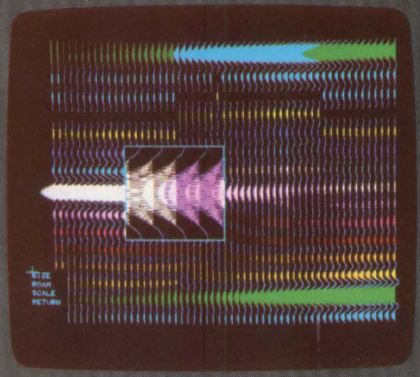


Only Megatek gives you all three, the excitement of dynamic raster color...

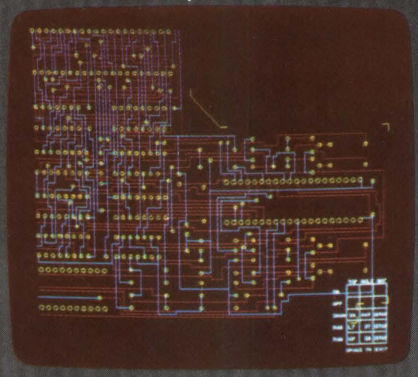


...the precision of 4096 x 4096 high resolution calligraphic Whizzard systems...

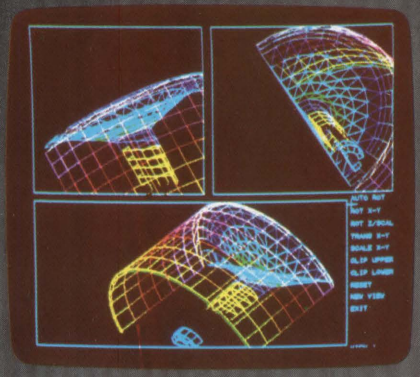
...and user-oriented software to make it easy to implement your application.



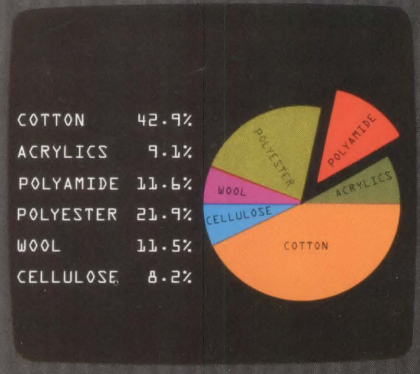
Powerful, real-time dynamics enable you to scan the display then zoom in for added detail.



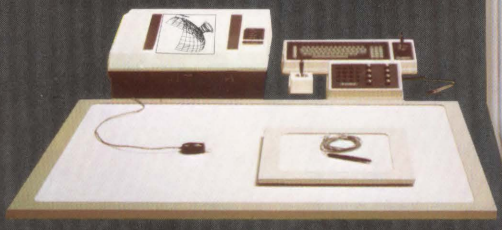
A large virtual display gives you the full picture, with the added information of up to 16 colors at a time.



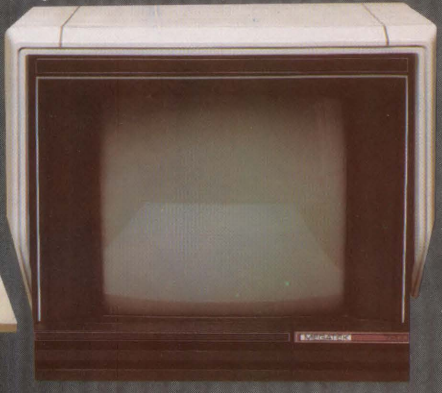
Rotations mean you can view models from any angle and segment the display into multi-viewports.



It all adds up to the capabilities you need to put your ideas into pictures.



And you get freedom of choice, too, with intelligent interactive peripherals and modular design for easy expansion.



The Megatek Whizzard. It will set you free.

Express yourself with a Whizzard computer graphics system and take advantage of our technological innovations. You get system flexibility. Easy to use, ever-expanding software support. Installation, training and service world-wide. And an inside track on the future.

We're earning our reputation in computer graphics. Count on us. For advanced hardware compatible software. And added value.

Find out more about how Megatek can give you freedom of expression. Write for up-to-the-minute details on our complete line of computer graphics products.

Megatek Corporation, 3931 Sorrento Valley Blvd., San Diego, CA 92121. 714/455-5590. TWX 910-337-1270
Megatek International/Europe, 11 Woudstraat, 4031 JA Ingen, The Netherlands, Telephone: 31 3443-2800, Telex: -70619

MEGATEK

MEGATEK CORPORATION

CIRCLE 1 ON INQUIRY CARD

New From Kennedy

Model 6450 High Density Cartridge Tape System

Low cost, flexible and reliable backup—that's Kennedy's Model 640 Cartridge Tape Drive and Model 650 Embedded Formatter—combined in one compact package—Model 6450. Model 6450 is loaded with features, such as:

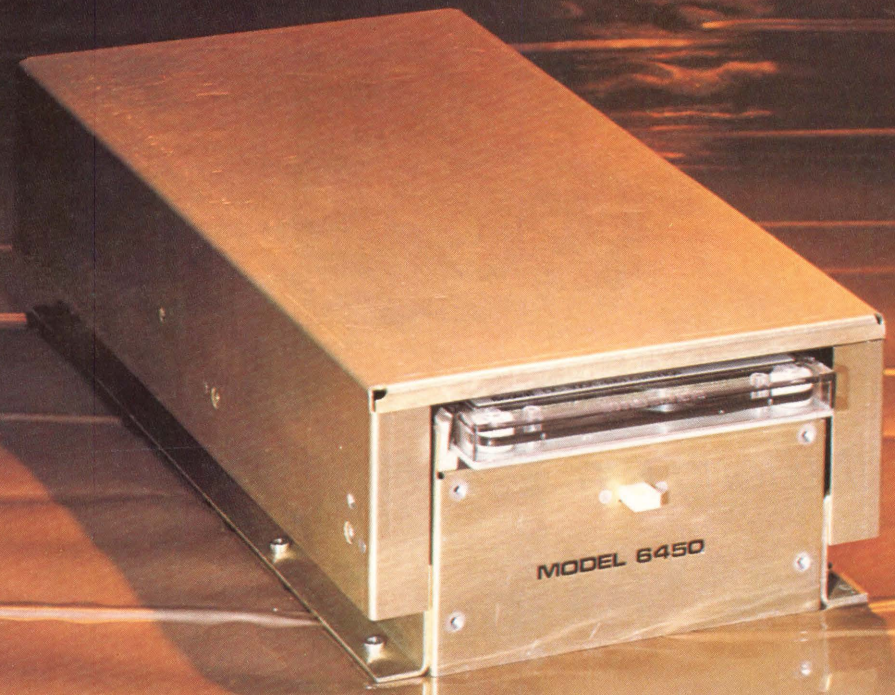
- Low power consumption—the system requires only +5 and +24 volts for a total consumption of under 40 watts.
- Serpentine recording head—eliminates time consuming rewinds between tracks during backup process.
- 6400 BPI recording density—yields up to 17 Mbytes of unformatted data capacity on a 450 ft. cartridge.
- Infrared tape position detection—virtually impervious to ambient light, a major factor in tape position sensing errors.
- Online self test—The 6450 system performs online self test before your backup operation begins.

These are only a fraction of the features that make Model 6450 the most advanced ¼" tape cartridge available. All these features, combined with Kennedy experience and reliability guarantee it.

KENNEDY
Subsidiary, Magnetics & Electronics Inc.
1600 Shamrock Ave., Monrovia, CA. 91016
(213) 357-8831 TWX 910-585-3249

KENNEDY INTERNATIONAL
Koningin Elisabethplein, 8
B-2700 Sint-Niklaas
Belgium
Tel: (031) 771962
Telex: 71870 Ken Co

CIRCLE 2 ON INQUIRY CARD



KENNEDY • QUALITY • COUNT ON IT

It Pays To Have The New Mannesmann Tally T-3000.

New features from the leader in matrix line printers.

New capabilities. Expanded versatility. The Tally 300 line per minute printer takes advantage of the inherent flexibility of matrix line printing to give you more value. Now you can beat the band with host defined **downstream font selection** and change character styles midstream. No lost time, downtime, or messing around to change fonts. Plus, you can now print **double high characters** for highlighting text. Or, for those occasions when extra special print quality is called for, a new **multi-pass** model makes a double pass to enhance character appearance.

And now you can move the printer from the computer room and locate it where the information is used. A new Asynchronous Communications Adapter gives you 300 line per minute on-line **remote printing.**

Plus, look at the standard features of every T-3000. Quiet operation. Easy, front access, straight path paper loading. A reel to reel, prethreaded ribbon system for quick and clean ribbon changing. A time saving **diagnostic status display** that reduces service calls. It tells if a fault condition is operator correctable. If a service call is needed, it tells the service man what's wrong.

Dependable and durable, the T-3000 never requires preventive maintenance. Never needs adjustment. Character formation and line registration never waver. The T-3000. High reliability. Patented **flexure technology.**

There's more to tell so contact your nearest Mannesmann Tally Sales outlet.

Mannesmann Tally, 8301 South 180th Street, Kent, WA 98031. Phone (206) 251-5524.

Printers for the long run.

MANNESMANN TALLY

CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN®

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

VOLUME 20, NUMBER 1 JANUARY 1981

DEPARTMENTS

Cover by Darcy Gerbarg
Created at the Computer Graphics Research Laboratory of the New York Institute of Technology

Number of copies printed this issue—87,770

FEATURES

CONFERENCES

STAFF

Publisher and Editorial Director
Robert Brotherston

Editorial

Editor & Vice President
John A. Camuso

Managing Editor
Sydney F. Shapiro

Technical Editor
Shawn Spilman

Senior Editor
Peg Killmon

Field Editor S. Calif & SW
(213) 824-5438
Michael Chester

Field Editor N. Calif & NW
(408) 371-8901
Douglas Eidsmore

Associate Editors
James W. Hughes **Colleen Ginchereau**

Copy Editors
Sue Paxman **Debra M. Highberger**

Assistant Editor
Jun U. Smith

Editorial Advisory Board
Brian W. Pollard **Ralph J. Preiss**
Rex Rice

Circulation and Production

Associate Publisher & Vice President
Anthony J. Saltalamacchia

Circulation Director
Robert P. Dromgoole

Data Control Manager
Wanda Holt

Circulation Manager
Alma Brotherston

Production Manager
Linda M. Wright

Production Assistant
Lou Ann Sawyer

Advertising Coordinators
Sally H. Bowers **Cherie Crosby**

Art Director
James Flora

Technical Art
Concepts Unlimited

Marketing

Vice President of Marketing
Ronald W. Evans

Marketing Services Manager
Linda G. Clark

Promotion Manager
Tom Hodges

Financial

Administrative Director
John O. McGillivray

Controller
David C. Ciommo

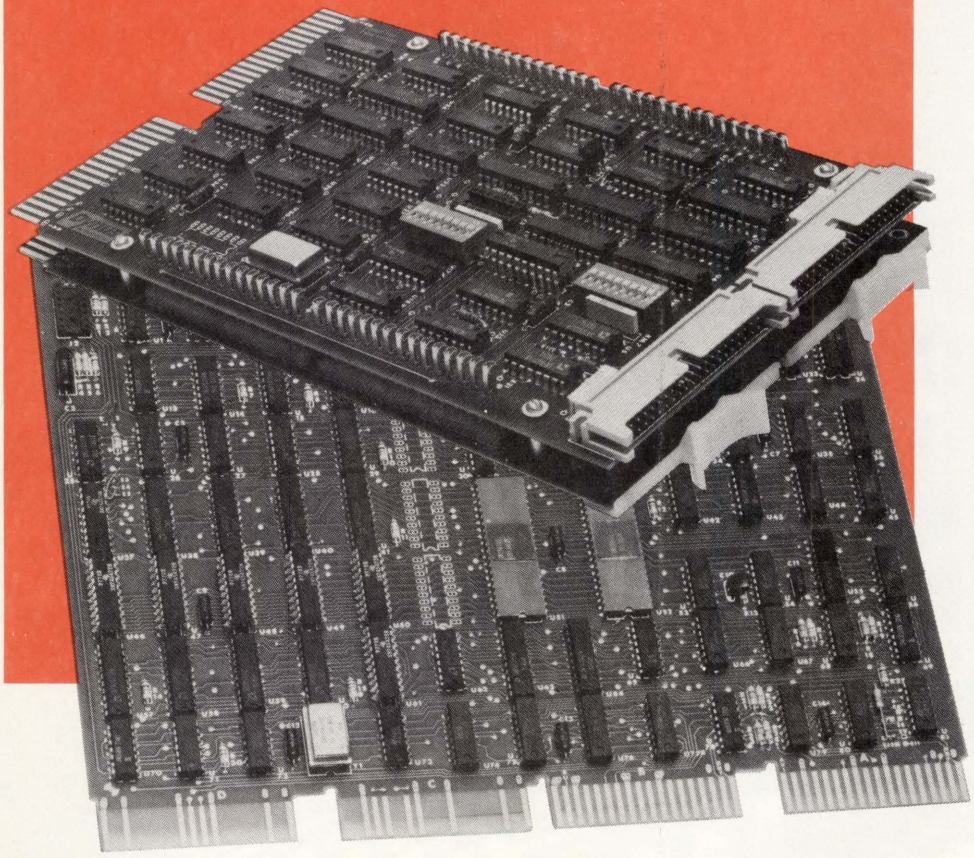
Computer System

Research Director
Wayne Newman

Editorial & Executive Offices
11 Goldsmith St, Littleton, MA 01460
Tel. (617) 486-8944/(617) 646-7872

Editorial manuscripts should be addressed to Editor, Computer Design, 11 Goldsmith St., Littleton, MA 01460. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."

DEC®-COMPATIBLE PERIPHERAL CONTROLLERS



Now, from the company that delivers the industry's widest range of DEC-compatible memory products, a family of peripheral controllers that's second to none. From comparatively simple cartridge disk controllers to complex 300MB storage module drive (SMD) controllers.

An impressive array of state-of-the-art controllers, all built around high-speed bipolar microprocessors. All software compatible with the host LSI-11® or PDP®-11 minicomputer...and all available now.

And Dataram's controllers are designed to save you money, and a lot more. Like space — our controllers typically occupy half the space required for the comparable controller from DEC. Doing it with a level of performance that makes any member of this family worth looking at.

Look at the chart of our current family of peripheral controllers, growing every day. If you don't see the controller you need, we're probably working on it right now. Call us and discuss your requirements.

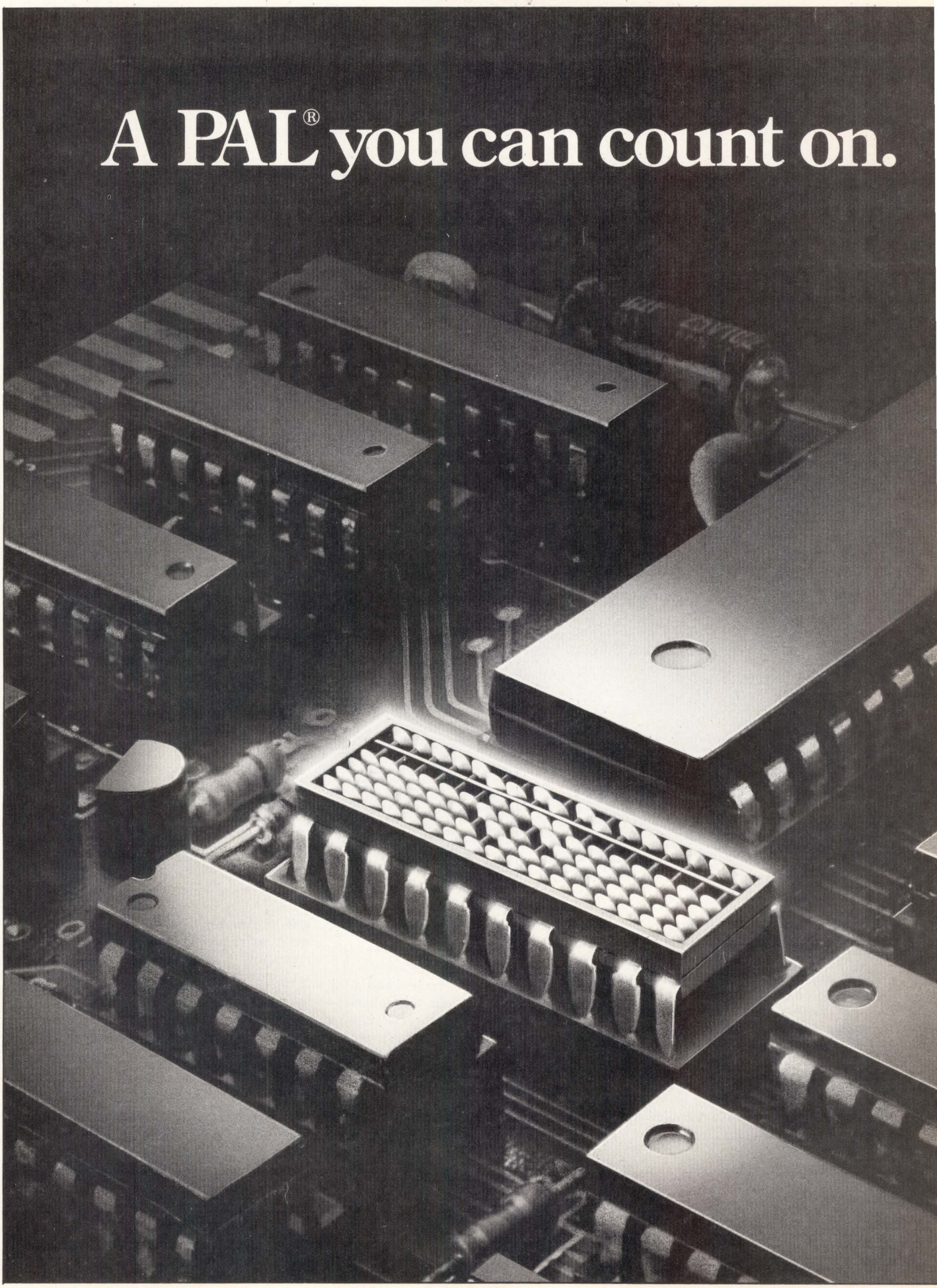
DEC, LSI-11 and PDP are registered trademarks of Digital Equipment Corporation.

DATARAM CORPORATION

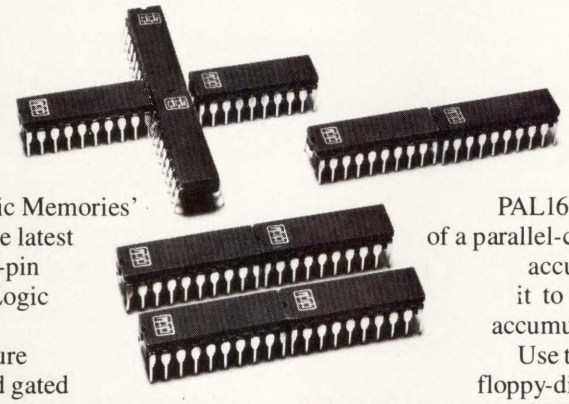
Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

DATARAM CONTROLLER	Magnetic Tape Controller			Cartridge Disk Controller		SMD Controller					
	T03	T04	T34	C03	C33	S03/A	S03/B	S03/C	S33/A	S33/B	S33/C
MINI COMPATIBILITY	LSI-11	LSI-11	PDP-11	LSI-11	PDP-11	LSI-11	LSI-11	LSI-11	PDP-11	PDP-11	PDP-11
	TM11/TU10			RK05		RM02	RK07	RP06	RM02	RK07	RP06

CIRCLE 5 ON INQUIRY CARD


A PAL® you can count on.

Announcing two new arithmetic PALs that replace ALUs and bit slices, use less space and power.



The PAL16A4 and PAL16X4 are in production now and in stock at your Monolithic Memories' distributor. They are the latest two members of the 20-pin Programmable Array Logic (PAL) family.

Both new PALs feature exclusive-OR gates and gated feedback which allow you to perform complex arithmetic functions such as addition, subtraction and counting. And both allow you to save up to 75% in parts count over old-style random logic.

New capabilities in the same 20-pin SKINNYDIP™.

PAL16X4 is an AND/NOR/Exclusive-OR array with four programmable I/O pins, four registers each with internal feedback and a three-state output. It's suitable for use as a programmable counter or a between-limits comparator.

The PAL16A4 provides the same capabilities as the PAL16X4, with the addition of a parallel-carry and an on-board accumulator which allow it to perform as an ALU accumulator.

Use them in controllers for floppy-disk systems, for hard-disk systems or for CRTs . . . wherever space and power must be conserved. Their low power dissipation and 20-pin SKINNYDIP packaging make them the board designer's dream.

Ask for complete details.

Contact your nearest Monolithic Memories franchised distributor or sales representative for full technical data on the entire 15-device 20-pin PAL family.

Monolithic Memories, Inc., 1165 E Arques Ave., Sunnyvale, CA 94086.

PAL and SKINNYDIP are trademarks of Monolithic Memories, Inc.

HOTLINE!
For express product information, call toll-free:
(800) 528-6050 Ext 131. In Arizona: **(800) 352-0458** Ext 131

Monolithic Memories MMI

CIRCLE 6 ON INQUIRY CARD

Compare our data and time domain logic analyzer with the industry's leading data-domain-only unit.

For complete analysis, the K100-D outperforms H-P's 1610B!

Before you settle for the Hewlett-Packard 1610B data domain analyzer, compare it with the general purpose Biomation K100-D, our fastest-selling logic analyzer ever.

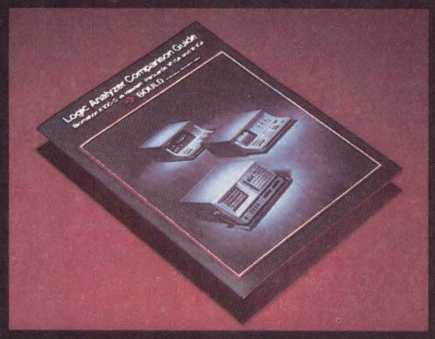
Compare depth of information.
A data domain (software) analyzer —even a unit as sophisticated as the H-P 1610B—simply does not give you all the information you need for debugging your mainframe, mini- and microprocessor-based systems. During the critical system-integration stage of a development cycle, a problem that looks like a software failure may turn out to be a not-too-obvious hardware malfunction. The K100-D's data/timing capability lets you analyze software/hardware relationships and find the problem, wherever it originates. You can display up to 16 channels of critical timing information about race conditions and phase relationships between signals.

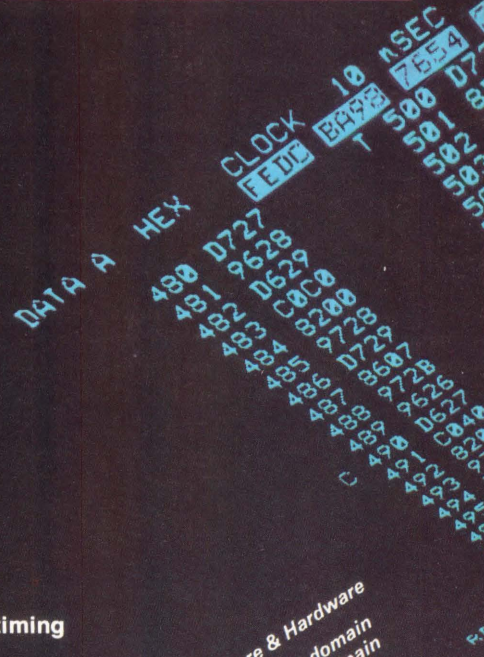
So vital is this timing information to complete problem analysis that industry trends indicate logic analyzers of the future will have both data and timing analysis capabilities—like the K100-D has today!

Compare data domain range.
The high-speed K100-D gives you data domain capability to 70 MHz —as compared with the 1610B's 10 MHz rate—for use with faster multiplexed microprocessors, computers, and ECL bit-slice processors. At 12 to 70 MHz, the K100-D gives you 16 channels of data display, with 1024 words of memory.

Operating at 0 to 10 MHz, both units give you 32 channels of data domain information. But the K100-D's memory is 8 times as deep as the 1610B's—512 words versus 64. The 1610B's 7 levels of triggering exceed the needs of most users, and those who do need this capability can generally get it from their development system. With the K100-D, you don't sacrifice vital timing information for data domain capabilities you don't need.

The final analysis.
To help you evaluate your needs before you buy, we've prepared a point-by-point competitive comparison of the Biomation K100-D and the H-P 1610B. (Incidentally, it also shows how the K100-D beats H-P's general purpose 1615A hands down.) To get your free copy, just use the reader service number or write Gould Inc., Instrument Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.

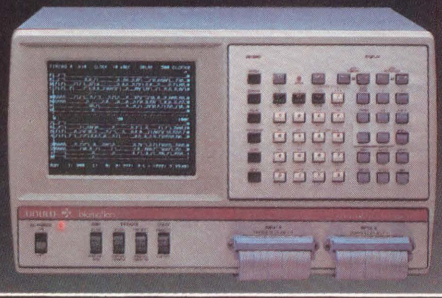




Hewlett-Packard 1610B
A sophisticated data-domain-only logic analyzer

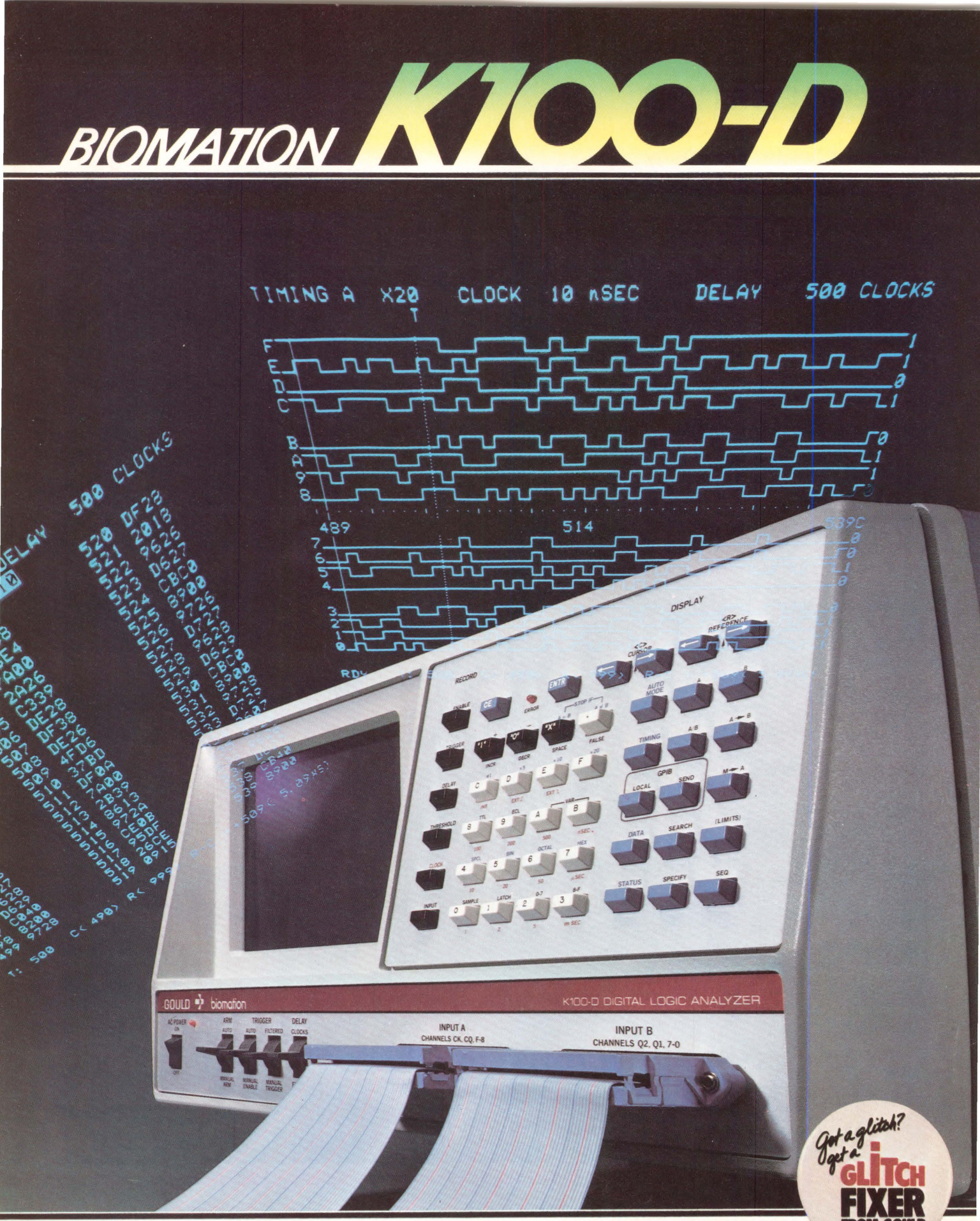
Analysis: Software
Speed: to 10 MHz
Channels: 32 data
Memory: 64 words

Biomation K100-D
The industry's finest data/timing logic analyzer



Analysis: Software & Hardware
Speed: to 70 MHz data domain
to 100 MHz time domain
Channels: 32 data to 12 MHz,
16 data to 70 MHz
16 timing to 100 MHz
Memory: 1024 words @ 16 channels
512 words @ 32 channels

BIOMATION K100-D



Got a glitch? get a GLITCH FIXER FROM GOULD

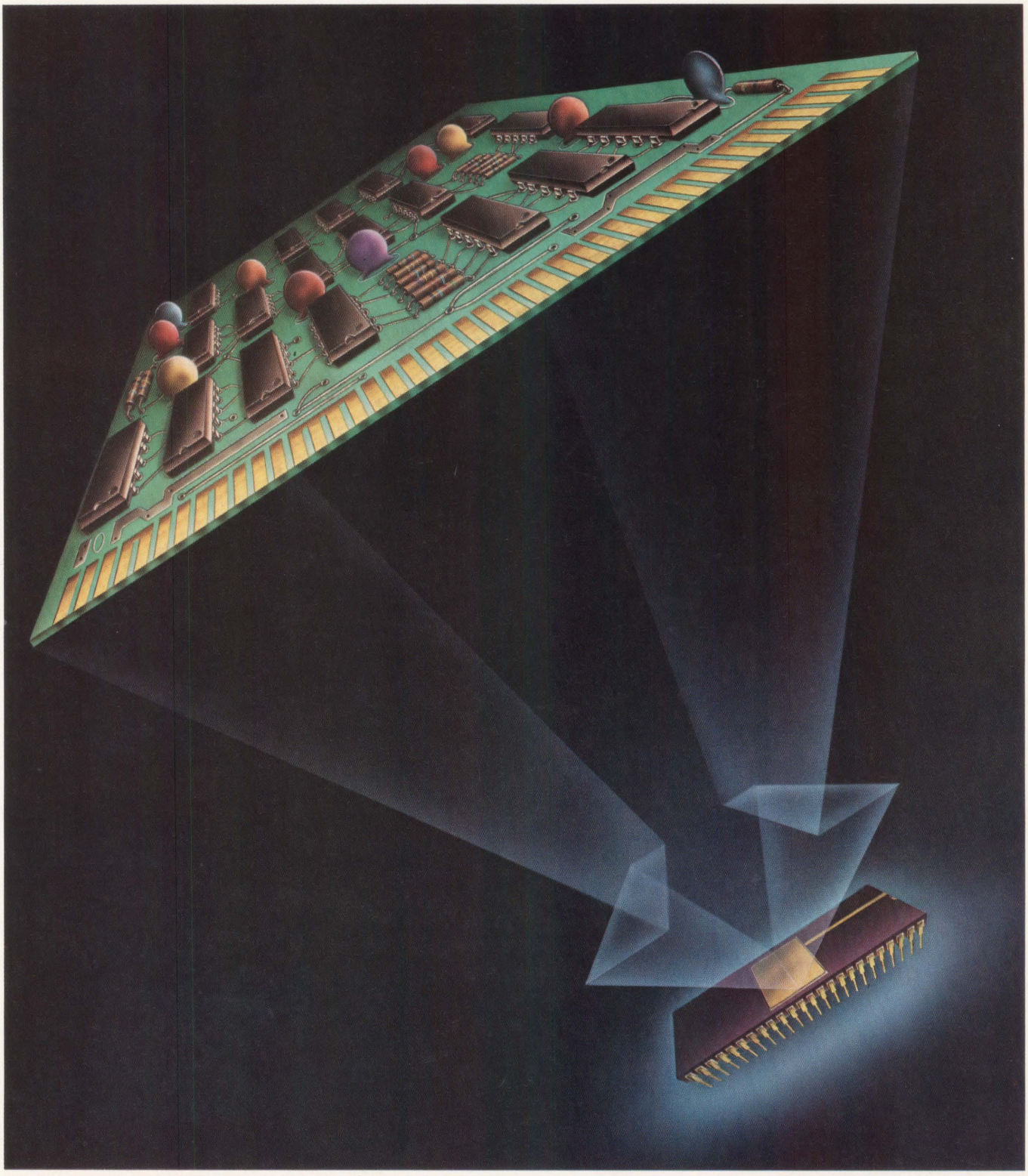
GOULD

An Electrical/Electronics Company

CIRCLE 7 ON INQUIRY CARD

FAIRCHILD

A Schlumberger Company



We just reduced your bus

Introducing the fastest single-chip IEEE-488 bus in the business.

Fairchild's 96LS488 is the first and only General Purpose Interface Bus that performs all the functions of Talker, Listener and Talker/Listener on a single low-power Schottky chip. And it's microprocessor-independent.

No one can touch the 96LS488 for speed, either. It operates at the full bus specifications of 1 MHz data rate—four times faster than its closest competition.

It drives the bus directly.

The 96LS488 contains all the termination resistors and 48 mA drivers for the management, bus handshake and parallel Poll required for the bus. It implements all IEEE-488 functions internally and features simple system handshake for ease of interface.

A bus load of features.

The 96LS488 requires only a single 5V power supply. It has:

Separate Talk and Listen address capability.

Secondary address capability.

Talk only and Listen only capability.

Source handshake delay programmable for low or high-speed data drivers.

Serial Poll and parallel Poll capability.

A device Trigger and Device Clear outputs.

The capability to implement Remote/Local function.

And all bus I/O signals comply with IEEE-488 input threshold, termination and output specs.

We'll route you an evaluation kit today.

The 96LS488E is available to you now. You can begin to design with it immediately by contacting your local Fairchild Semiconductor distributor for an evaluation kit. This kit includes:

Two 96LS488E's.

A complete data sheet describing the functions and parameters of the 96LS488.

An application guide showing information on hookup with various microprocessor-based systems.

The names of our 96LS488 applications specialists you can call to answer any additional questions.

There's no longer any need to spend extra time designing an interface logic. Our bus gets you there much faster. And much easier, too.

For more information call or write 96LS488 Bus at Fairchild Semiconductor Products Group, P.O. Box 880A, Mountain View, California 94042. Tel: (415) 962-3716. TWX: 910-379-6435.

Fairchild Camera and Instrument Corporation

interfacing problems.

CIRCLE 8 ON INQUIRY CARD

CALENDAR

CONFERENCES

FEB 2-4—Microprocessor-Based Energy Management Systems, U of Wisconsin-Madison, Madison, Wis. INFORMATION: Robert P. Madding, Dept of Engineering, U of Wisconsin Extension, 432 N Lake St, Madison, WI 53706. Tel: 608/263-7920

FEB 3-5—Aerospace and Electronic Systems Winter Conv, Sheraton Universal Hotel, North Hollywood, Calif. INFORMATION: William H. Minshull, Bldg A 107, Hughes Aircraft Corp, Culver City, CA 90230. Tel: 213/391-0711

FEB 3 AND FEB 5—Invitational Computer Conf, Pier 66 Hotel, Ft Lauderdale, Fla, and Radisson Inn Atlanta, Atlanta, Ga. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

FEB 9-12—Internat'l Symposium on Information Theory, Santa Monica, Calif. INFORMATION: Prof Izhak Rubin or Kung Yao, System Science Dept, 4531 Boelter Hall, U of Southern California, Los Angeles, CA 90024. Tel: 231/825-2240

FEB 18-20—Internat'l Solid State Circuits Conf, Hyatt Hotel, New York, NY. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 23-26—Compcon Spring '81, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 9-12—Software Engineering Internat'l Conf, San Diego, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 12—California Computer Shows, Inn-at-the-Park, Anaheim, Calif. INFORMATION: Norm De Nardi, 95 Main St, Los Altos, CA 94022. Tel: 415/941-8440

MAR 16-18—Industrial and Control Applications of Microprocessors, IECI '81, Sheraton Hotel, Philadelphia, Pa. INFORMATION: H. Troy Nagle, Dept of Electrical Engineering, Auburn U, Auburn, AL 36830

MAR 23-25—Office Automation Conf, Albert Thomas Convention Ctr, Houston, Tex. INFORMATION: Kate Frye, Office Automation Conf, PO Box 9659, Arlington, VA 22209, Tel: 703/558-3617

MAR 23-26—Internat'l Conf on Digital Communications, Congress Bldg, Internat'l Fair of Genoa, Genoa, Italy. INFORMATION: Manager, Rome Branch of Administrative Office, 5th ICDSC, Telespazio SPA, Corso D'Italia 43, 00198 Rome, Italy

MAR 24-26—FOC '81 EAST, Internat'l Fiber Optics and Communications Expo, Hyatt Regency, Cambridge, Mass. INFORMATION: Ellen M. Bond, Information Gatekeepers, Inc, 167 Corey Rd, Brookline, MA 02146. Tel: 617/739-2022

MAR 24-27—Printemps Informatique, Palais des Congres, Paris, France. INFORMATION: Kallman Assocs, 30 Journal Sq, Jersey City, NJ 07306. Tel: 201/653-3304

MAR 30-APR 1—IEEE Internat'l Conf on Acoustics, Speech, and Signal Processing, Sheraton-Atlanta Hotel, Atlanta, Ga, INFORMATION: Ronald W. Schafer, Dept of Electrical Engineering, Georgia Inst of Tech, Atlanta, GA 30332. Tel: 404/894-2917

APR 3-5—West Coast Computer Faire, Civic Auditorium, San Francisco, Calif. INFORMATION: Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: 415/851-7075

APR 7-9—Electro, Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

APR 27-29—IOOC '81 (Integrated Optics and Optical Fiber Communication), Hyatt Regency, San Francisco, Calif. INFORMATION: Barbara Hicks, Optical Society of America, 1816 Jefferson Place, NW, Washington, DC 20036. Tel: 202/223-8130

APR 27-MAY 1—Society for Information Display Internat'l Symposium, Grand Hyatt Hotel, New York, NY. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193

APR 28-30—Internat'l Telecommunications Forum, Concorde Lafayette Hotel, Paris, France. INFORMATION: Dusty Rhodes, Arthur D. Little Decision Resources, Acorn Park, Cambridge, MA 02140. Tel: 617/267-3456

MAY 4-7—NCC (National Computer Conf), McCormick Place, Chicago, Ill. INFORMATION: Gerard Chiffriller, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/558-3600

MAY 19-21—INTELEC '81 (Internat'l Telecommunications Energy Conf), Royal Lancaster Hotel, London, England. INFORMATION: INTELEC '81 Secretariat, The Inst of Electrical Engineers, Savoy Pl, London WC2R OBL, England

SEMINARS

MAR 19-20 AND MAY 7-8—Data Communications, Worcester Polytechnic Inst, Worcester, Mass. INFORMATION: Ginny Bazarian, Office of Continuing Education, Worcester Polytechnic Inst, Worcester, MA 01609. Tel: 617/753-1411

SHORT COURSES

MAR 2-4, 4-6, 5-6, 9-12, and 16-17—Microprocessor Application Design, Advanced Micro Devices, Inc, Customer Education Ctr, Sunnyvale, Calif. INFORMATION: Advanced Micro Devices, Inc, Customer Education Ctr, 490-A Lakeside Dr, Sunnyvale, CA 94086. Tel: 408/732-2400

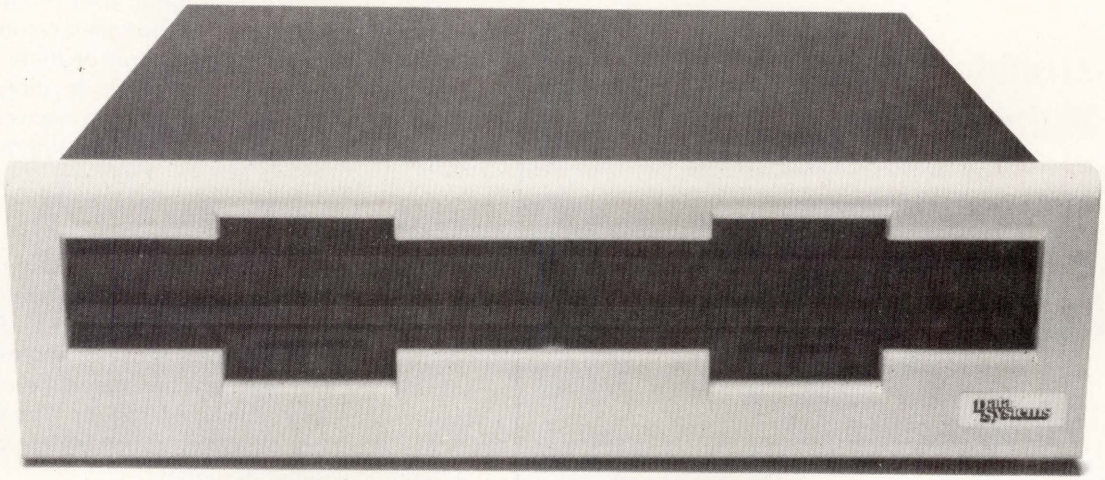
MAR 23-24—Digital Electronics for Automation and Instrumentation; MAR 25-28—TRS-80 Radio Shack Microcomputer Interfacing and Programming for Scientific Instrumentation; AND MAR 25-28—Motorola Single Chip Interfacing and Programming Using the 6801, 6809, and 6800, Virginia Polytechnic Inst and State U, Blacksburg, Va. INFORMATION: Dr Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. Tel: 703/961-5241

MAR 24-25—Custom Integrated Circuits and Integrated Circuits for Telecommunications, San Francisco Hilton, San Francisco, Calif. INFORMATION: Continuing Education in Engineering, U of California Extension, 2223 Fulton St, Berkeley, CA 94720. Tel: 415/642-3112

APR 6-10—Tutorial Week-East, Orlando Marriott Inn, Orlando, Fla. INFORMATION: Tutorial Week-East, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

Announcements intended for publication in this department of ***Computer Design*** must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.

THE DSD 440. TOTAL DEC® RX02 COMPATIBILITY,



AND MORE.

The DSD 440 is the only alternative to the DEC RX02 that's 100% software, hardware and media compatible with LSI-11, PDP®-11 and PDP-8 computers, including those with extended memory. It can be configured as an RX02 for DEC double density or IBM 3740 single density recording, or as an RX01 for backward operating system compatibility.

MORE

A 512-byte hardware bootstrap is built into all PDP-11 and LSI-11 interfaces. It loads system software automatically from either single or double density diskettes. Extensive self-testing is DIP-switch selectable with the "Hyperdiagnostics" that run without being connected to a computer. The low profile 5¼-inch DSD 440 features write protection and diskette formatting.

FASTER

The optimized DSD 440 microcode increases system throughput when using the RT-11 foreground/background monitor. In particular, the DSD 440 with an LSI-11 runs fill and empty buffer operations 20% faster than an RX02.

FOR LESS

The DSD 440 is the RX02 compatible flexible disk system that combines high performance and advanced features with fast delivery... at a lower price. For further information, call or write Data Systems Design today. A data sheet and price list will be forwarded to you immediately.

® Trademark of Digital Equipment Corporation

Data Systems

EASTERN REGION SALES
Data Systems Design, Inc.
51 Morgan Drive, Norwood, MA 02026
Tel: (617) 769-7620 TWX: 710-336-0120

WESTERN REGION SALES
Data Systems Design, Inc.
2560 Mission College Blvd., Suite 108
Santa Clara, CA 95051 Tel: (408) 727-3163

CORPORATE HEADQUARTERS: Data Systems Design, 3130 Coronado Drive, Santa Clara, CA 95051
Tel: (408) 727-9353 TWX: 910-338-0249

CIRCLE 9 ON INQUIRY CARD

A Distributed Processing System For Military Applications— Part 4: The Software

Ralph Mauriello

Litton Data Systems
8000 Woodley Ave, Van Nuys, CA 91409

The first three articles of this series described, respectively, the system overview,[1] the high speed serial interelement bus that connects the system nodes,[2] and the design approach used for the computers[3] in the distributed processing system developed by Litton Industries for military applications. This fourth and final article in the series discusses the executive software design that was created for the system.

The first three requirements listed in the Panel, "DPS Executive Software Requirements," are derived directly from the system design as described in the system overview,[1] while the last two are imposed in order to attain the goal of software development cost reduction. System initialization requirements include (a) local bootload, to load a node that has bootload media within it; (b) system bootload, to load the entire system from a single button activation; and (c) remote bootload, to load, via the serial interelement bus (SIB), a node that does not have bootload media.

Executive support of the monitoring and control functions includes SIB initiation and control, periodic status requests/responses, and the transmission of such various protocol messages as Acknowledge and Wilco. Software is also required to control system reconfiguration in the event of node or data bus failures.

The executive developed for the distributed processing system (DPS) had to support existing UYK-20 user programs in order to ensure minimum development costs for new software systems and permit applicability of existing user programs to a new system. Also, the executive must support development of new user programs that are designed for applications using DPS hardware. Since it is desirable that the new user programs serve more than one system application, the executive must provide the necessary support to permit user programs to request resources or permit calls to other user programs without knowledge of the location of the called resource or of the other user program. Combination of these last two requirements minimizes software development costs because it permits the use of many existing software modules and ensures that the development of new modules is applicable to more than one system.

DPS Executive Functions

The Panel, "DPS Executive Functions," summarizes functions resulting from the design of the software system that satisfy the requirements described above. Although the functions in this list resemble those of any executive program, the first four functions are quite different from what they would be in a centralized system. The input/output (I/O) and memory allocation functions are implemented in a fairly conventional manner.

While the conceptual design of the functions is described, not all of the features are fully implemented. The limiting factor in the implementation of the software is the hardware demonstration system (see Fig 1) that was built for software development. This system contains three nodes, each of which contains a single element, and only one of which contains a dual central processing unit (CPU). A more generalized configuration than that of the demonstration system is shown in a system that has not only elements, but nodes with multiple elements called clusters. (See Fig 2.) In a multibus system, the buses interface with each other at the clusters; eg, a 3-element cluster may be used to interconnect three SIBs, as shown in Fig 3.

With reference to Figs 2 and 3, the following definitions apply: the SIB interconnects the nodes; a node may consist of one or more elements, a multi-element node is called a cluster, and a single-element node is called an element; and an element may have one or more CPUs. Hardware development of a cluster and a dual-loop system is currently under way and verification of the software design of these capabilities awaits completion of the hardware.

Design Approach

Since the first emulator developed for DPS was a UYK-20, it was decided to take SDEX 20, existing executive for the UYK-20, and use it as the basis for the DPS executive design. Many extensions to its capabilities were added to support DPS. Significant weaknesses of SDEX 20 for this application are that the program was designed to support a single-processor system and that each of the nine different task types requires its own separate scheduling list and list maintenance routines. Modifications and/or new features were added to SDEX/20 to make it applicable to a DPS.

(continued on page 19)

NEC Trimliners. A generation ahead.

300-600 LPM band printers that set new standards.

At NEC, we've been working on band printer technology for more than seven years. While others were contemplating the possibilities of this practical, low-cost method, NEC was constructing its first units, getting the bugs out, improving the designs. Bringing state-of-the-art electronics to band printer controls. Adding serviceability. Reliability. Durability.

Today, NEC offers two band printers with speeds of 300 and 600 lines per minute. Available now, they are also reliable—now. They incorporate a technology which is now. The band technology. Low-cost, very reliable, extremely flexible.

A new enhanced-print feature allows the user to change speeds under either software or hardware controls to produce higher quality printed output. The feature reduces the 300 LPM speed to 170 LPM, and the 600 LPM rate to 350 LPM.

NEC's Trimliner printers have *never* experienced any band breakage. They have uptimes 50% higher than the competition. Trimliners average less than 30 minutes to repair. They're quiet, modular, ultra-cool and available in desktop, pedestal-mounted or two models of quiet cabinetry.

The technology of the 80s in a printer for the 80s from NEC—a company that was preparing for this decade and its band printing needs while others were just thinking about it.

NEC's Trimliner band printers. A generation ahead.

NEC. Going after the perfect printer.

NEC

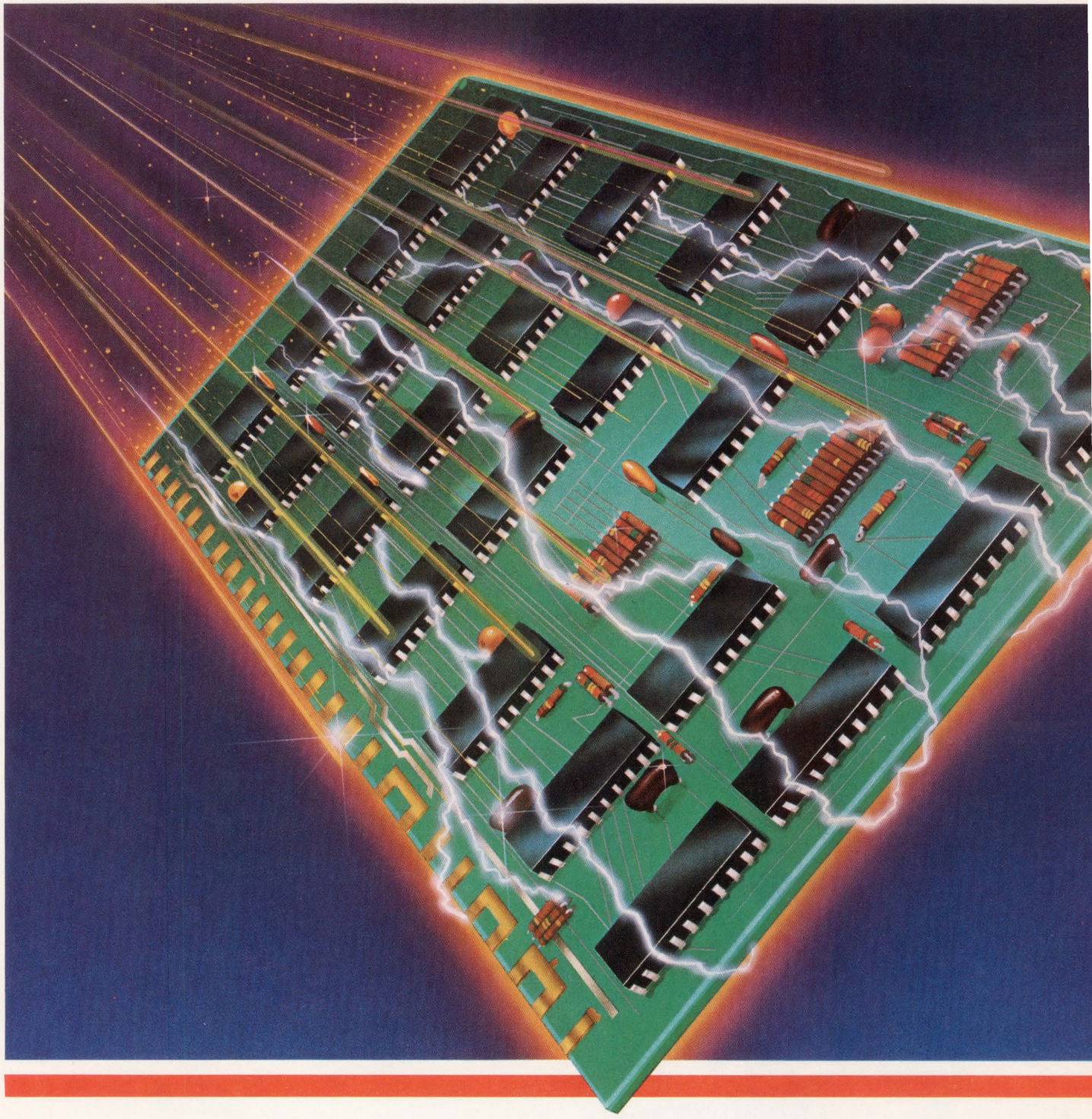
NEC Information Systems, Inc.

Head Office: 5 Militia Drive, Lexington, MA 02173, (617) 862-3120
Eastern Office: 36 Washington Street, Wellesley, MA 02181, (617) 431-1140
Central Office: 3400 South Dixie Drive, Dayton, OH 45439, (513) 294-6254
West Coast Office: 8939 S. Sepulveda Blvd., Los Angeles, CA 90045 (213) 670-7346
Southern Office: 2945 Flowers Road South, Atlanta, GA 30341, (404) 458-7014

CIRCLE 43 ON INQUIRY CARD

FAIRCHILD

A Schlumberger Company



More of the fastest circuits

For high-speed and low-power requirements, nothing comes close to our FAST registers and multiplexers.

You've already heard about the exceptional performances of Fairchild's FAST latches, flip-flops and counters. Now, here are a few FAST facts on some of our other fine devices that you can use to upgrade your logic systems.

REGISTERS

74F194 4-Bit Universal Shift Register

Shift Frequency . . 150 MHz typ
Clock-to-Output Delay . . . . . 4.0 ns typ
I_{CC} . . . . . 33 mA typ

The 74F194 is 50% faster than Schottky and requires 65% less power. It's currently available in a plastic or ceramic package. And we have three octal shift registers planned for the near future: the 74F299, 74F322 and 74F323.

MULTIPLEXERS

Data-to-Output Delay

74F153
Dual 4-input. . . . 5.0 ns typ
74F253
Dual 4-input with 3-state outputs . . . . . 4.4 ns typ
74157
Quad 2-input . . . 4.5 ns typ
74F257
Quad 2-input with 3-state outputs . . . . . 4.0 ns typ
74F158
Quad input with inverted outputs . . . . . 2.9 ns typ

Select-to-Output Delay

74F352/353
inverted versions of the 74F153/253. .6.3 ns typ

Our multiplexers are 30% faster than Schottky and require 70% less power.

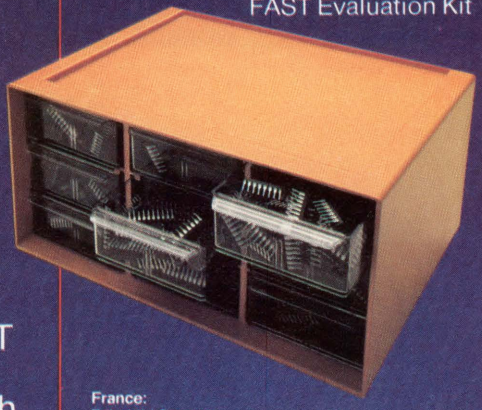
Our total FAST offering.

There is a total of 30 FAST parts available now in production quantities, with additional functions coming soon. So you can upgrade your standard Schottky system or design a new system today, with Fairchild's high-speed, low-power, improved-density devices.

Make a thorough examination.

To check our parts out further, order our evaluation kit that contains 14 different 74F Series devices. A total of 72 parts. Contact your nearest Fairchild sales office or distributor for our kit or information about our product delivery dates. Or call or write FAST, Fairchild Semiconductor Products Group, P.O. Box 880A, Mountain View, CA 94042. Tel: (415) 962-FAST. TWX: 910-379-6435.

FAST Evaluation Kit

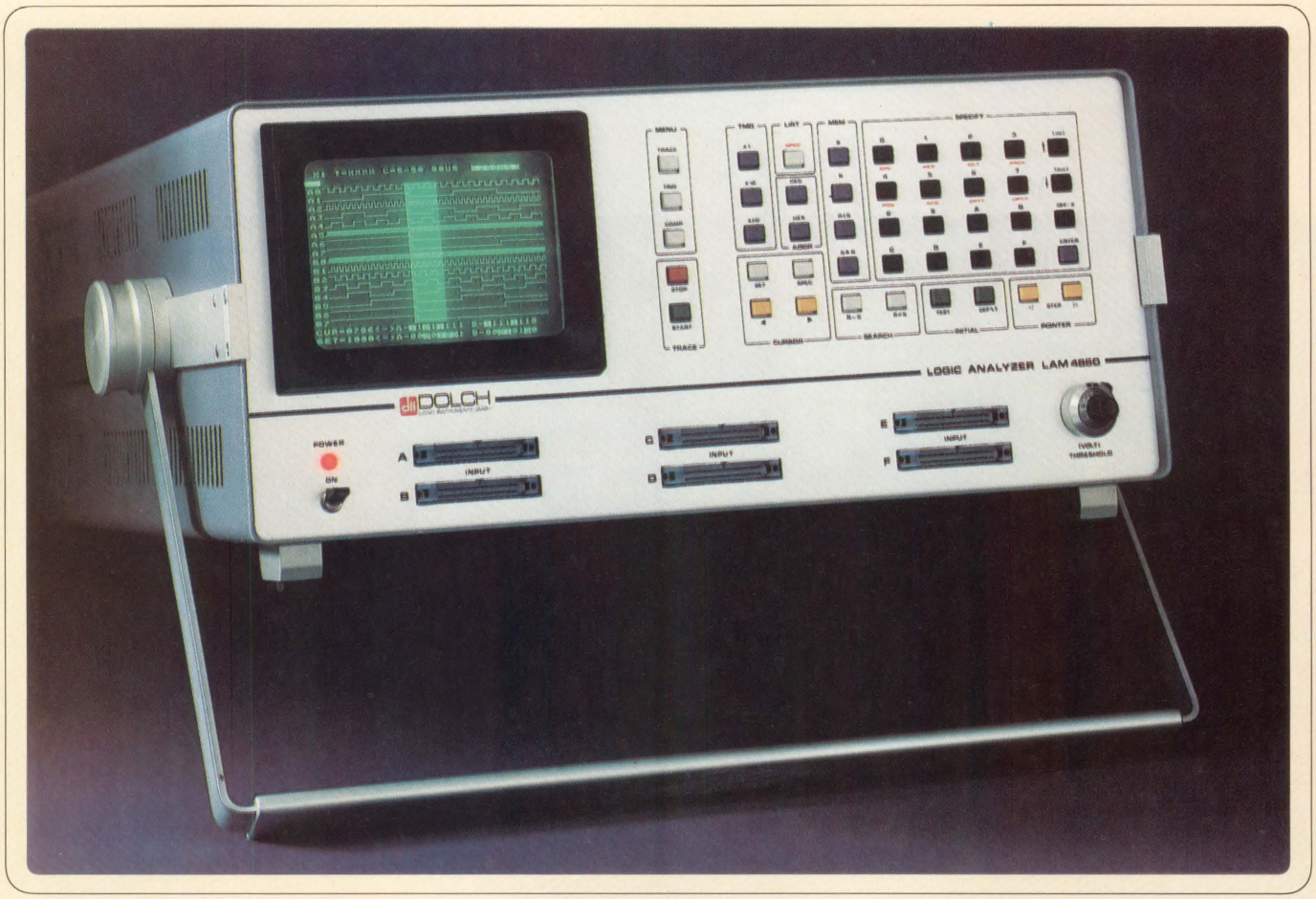


France: Fairchild Camera & Instrument S.A., 121 Ave. d'Italie, 75013 Paris. Tel: 331 584 55 66. Telex: 0042 200614. **Italy:** Fairchild Semiconduttori S.P.A., Viale Corsica 7, 20133 Milano. Tel: 02 296001-5. Telex: 843-330522. **Germany:** Fairchild Camera & Instrument (Deutschland) GmbH, 8046 Garching Hochbruck, Daimlerstr. 15, Munchen. Tel: 089 320031. Telex: 52 4831 fair d. **England:** Fairchild Camera & Instrument (UK) Ltd., 230 High St., Potters Bar, Hertfordshire EN6 5 BU. Tel: 0707 51111. Telex: 262835. **Sweden:** Fairchild Semiconductor AB, Svartengsgatan 6, S-11620 Stockholm. Tel: 8-449255. Telex: 17759. **Japan:** Fairchild Japan Corporation, Pola Bldg., 1-15-21 Shibuya, Shibuya-Ku, Tokyo 150. Tel: 03 400 8351. Telex: 2424173 (TFCTYO J). **Hong Kong:** Fairchild Semiconductor (HK) Ltd., 135 Hoi Bun Road, Kwun Tong, Kowloon. Tel: 3-440233. Telex: HX73531.

Fairchild Camera and Instrument Corp.

across the board.

CIRCLE 11 ON INQUIRY CARD



48 TO 96

Channels in One Logic Analyzer

Our LAM 4850 is the only logic analyzer that won't force you to buy, borrow or add-on to expand your analyzing capability to 96 channels. The power is already there. The flexibility is there. With a new channel expansion probe, the world's first 48-channel logic analyzer can be easily extended to an unrivaled 96 channels.

Plus multi-level clocking flexibility.

With three individual memory blocks of 16 channels by 1000 bits, the LAM 4850 allows simultaneous sampling with up to three separate clocks. This gives you a bus demultiplexing capability to independently monitor addresses and data. You can also disassemble program execution of a microprocessor into mnemonic code with this high performance instrument.

Plus sequential trigger power

The LAM 4850 has a 4 level nested recognition capability easily programmed through a separate menu. This feature simplifies debugging a faulty piece of software among several nested routines. And the LAM 4850 has the unique Dolch trigger trace monitor that gives you a real time read out of the completed routines.

Plus many other features:

- 1000 bits of recording and reference memory per channel
- Clock rate to 50 MHz
- With 96 channels—500 bits of recording and reference memory and 10 MHz clock rate
- Separate menus to set trace, trigger and compare parameters
- 5 ns glich catching
- Binary, hex, octal, ASCII, and timing display
- Programmability via GPIB and RS-232 interfaces
- Disassemblers and personality probes for all popular microprocessors

Plus sales and service nationwide.

For more information, contact your nearest representative or our manufacturing facility. Dolch Logic Instruments, Inc., 2180 Bering Drive, San Jose, CA 95131. (800) 538-7506. Inside Calif.: (408) 946-6044. TWX 910 338 3023.

dli DOLCH
LOGIC INSTRUMENTS

REPRESENTATIVES: **Austria** 02236/866310, **Belgium** 022192451-53, **Denmark** 02804200, **Finland** 08090520311, **France** 069302880, **Germany** 08931901-1, **Great Britain** 0734694944, **Greece** 0218219470, **Holland** 040533725, **Israel** 03453151, **Italy** 024158746, **Norway** 02356110, **Spain** 052213199, **Sweden** 08879490, **Switzerland** 013632188, **East Europe-U.K.** 093252121, **Singapore** 0637944, **South Africa** 01227739.

CIRCLE 12 FOR FURTHER INFORMATION. **CIRCLE 14 FOR DEMONSTRATION.**

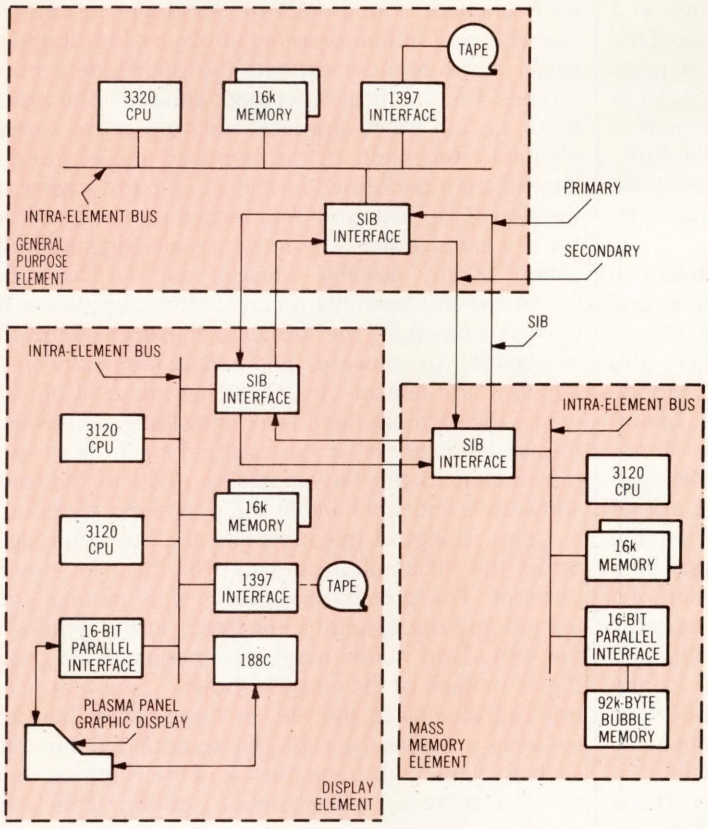


Fig 1 DPS demonstration system. Each node contains single element. Only one element contains dual CPU

Initialization

The initialization function of SDEX 20 was replaced virtually in its entirety because of a completely new set of system startup requirements. System bootload and remote bootload are entirely new. Local bootload is complicated by the multiple-CPU configuration that the UYK 20 hardware or software design does not permit.

Designed to permit initialization from any node that has bootload media, the system begins its initialization process by activating the system bootload function from the front panel of the selected element. Activation of such a node causes that node to assume the SIB controller function. In the demonstration system of Fig 1, the display element was chosen because the display is useful for system monitoring and control.

Activation of the system bootload button initiates a startup firmware routine in each of the processors within the display element. These execute a microdiagnostic and elect a master CPU to control the bootload function. The lowest numbered processor to pass its microdiagnostic test is elected master CPU, and the remaining processors become slaves. As in the SIB design, the master CPU function is reassignable to one of the other CPUs should the master fail. Firmware within the elected master then performs the bootload function and initiates tape read, computes checksums for each record to ensure correct data entry, and finally turns over control of the master CPU to software. This portion of the initialization function examines the element configuration table to determine the expected configuration of this element. Since the element configuration table of the demonstration system indicates that a second CPU is resident in this element, the next function is to start up the slave CPU.

The master CPU reserves a space for the dedicated memory of the slave CPU, places the starting address of slave CPU dedicated memory into a prespecified word in local memory (word 2), and then sets a "startup command" bit in local memory for the slave CPU. The software in the master CPU then goes into a wait loop until a "CPU up" bit is posted by the software executing in the slave CPU. After execution of its microdiagnostic (initiated by pushing the button) the slave CPU enters a loop which continually tests the startup command bit. Upon sensing the presence of the startup command bit, posted by the master CPU, the slave CPU transfers the starting address of its dedicated memory into its dedicated memory pointer register. All references to a CPU's dedicated memory are offset by the address value in the dedicated memory pointer register. This permits each CPU to have private dedicated memory for executive functions. As implemented, all CPUs execute the same code (single-copy

(continued on page 20)

reentrant) and have private control files. Firmware then passes control to software at an address contained in a prespecified location of the dedicated memory area of the slave CPU. Software now executing in the slave CPU posts the "CPU up" bit to inform the master CPU that software is up and running in the slave CPU. The display element of Fig 1 is now initiated and assumes the SIB controller function. When there is more than one slave processor in the element, the remaining slave processors are initiated by the master CPU in a similar manner.

The next function of the initialization software is bootload and initialization of the general purpose and mass memory downloop elements. Performed by the SIB controller software module within the executive, this function starts up the bus and, after ensuring enough delay for synchronization of all downloop nodes, broadcasts a remote master reset message to all of the downloop elements. The SIB interface hardware at each of the downloop elements detects the remote master reset message and resets the entire element. In the general case, the reset function, whether executed by a button activation on the front panel or the reception of a remote master reset message over the SIB, will cause all CPUs in an element to execute the microdiagnostic and then elect the master CPU of the element. In the demonstration system, the election of a master CPU is performed, and the CPU in each downloop element is the master. The firmware bootload routine in the master CPU of the downloop element then composes a status message for transmission back to the SIB controller, and prepares to receive the bootload record from the SIB. Functions described above are performed by all downloop elements. The status message contains information regarding the configuration of the downloop element.

Reception of the status messages by the SIB controller node permits it to compare the received configuration messages with the expected configuration of the system as defined by the element configuration tables (one for each element in the system). Assuming all nodes are operable and in the expected configuration, the SIB controller software now extracts the appropriate bootload records for the first downloop element and transmits them via the SIB to the local memory of the downloop element. Reception of the bootload records and error checking are performed by firmware in the master CPU of the downloop element. Any record received with an error in it is discarded. The response message indicates the action taken, thereby causing the SIB controller to retransmit the previous record. After completion of the bootload function, the firmware transfers control of the master CPU to software. The initialization software, executing in the master CPU, then determines if other CPUs within the element need to be initialized, performing the required function(s) if necessary. Finally, a message is transmitted to the bus controller node to indicate that software is initialized within the downloop element.

Upon receipt of this message, the bus controller performs the initialization function for the next downloop element. The process is repeated until all elements are loaded and the system is initialized. In the general case, the downloop nodes may contain clusters as shown in Fig 2. In each of the clusters shown, there is an element not tied directly to the SIB. In these cases, initialization software provides the capability to bootload and initialize such an element through the use of the common memory via the memory management system. The software modules that the element requires to be loaded are placed in common memory by software running in the element tied to the SIB. The firmware of the master CPU within the element to be loaded recognizes lack of an SIB connection and lack of bootload media and, therefore, goes by default to the common memory to extract the initialization routines. Control is then turned over to software.

(continued on page 27)

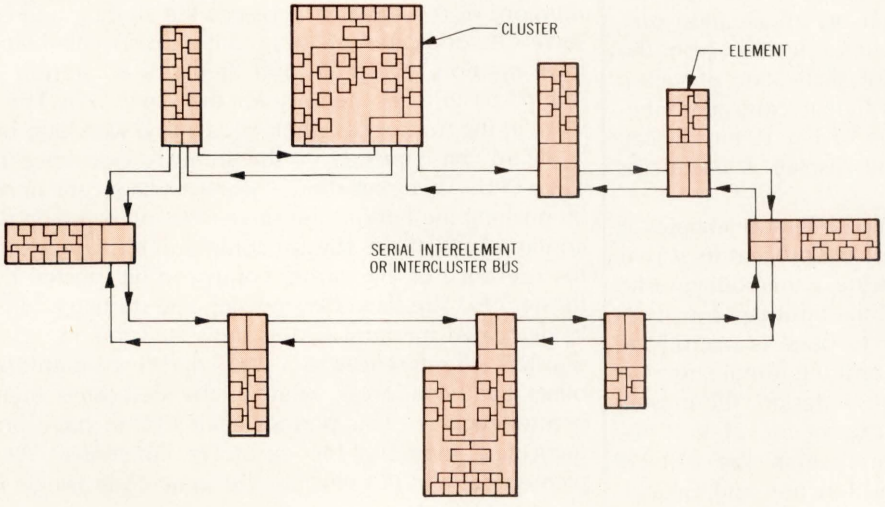


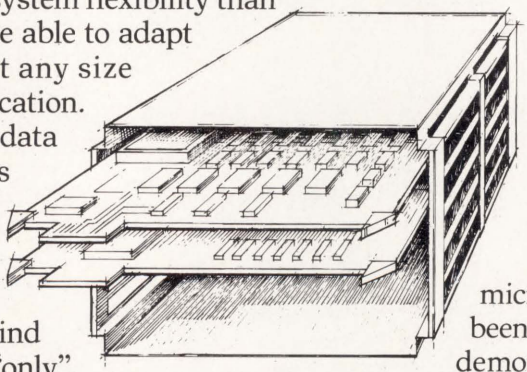
Fig 2 Generalized SIB interconnecting multiple elements and clusters. Element is single-element node; cluster is multi-element node

Hewlett-Packard announces another small breakthrough.

The two-board, 1/2 megabyte microcomputer.

Our HP 1000 L-Series now offers state-of-the-art 64K RAMs. They're the reason we've been able to put 512 kilobytes of memory on just one 6¾" x 11" board.

With the CPU on the other board, the L-Series opens a whole new dimension in microcomputers. Because with so much memory in so little space, you have more system flexibility than ever before. In fact, you'll be able to adapt the L-Series for just about any size job—and any kind of application. Including communications, data management and process control.



Big software for small hardware.

You may have to remind yourself that the L-Series is "only" a microcomputer. With powerful software features like our multi-programming, multi-user RTE operating system and language support that includes Assembler, FORTRAN 4X, BASIC and PASCAL, there's almost no limit to the high performance products you can build. Especially if you take advantage of our proven data base management system and networking software—also upwardly compatible throughout the entire HP 1000 line.

Multiple I/O processors, too.

The L-Series is designed with an innovative distributed intelligence architecture that assigns I/O traffic to separate processors located on each interface board. This means each I/O processor has its own direct memory channel—and direct access to the entire main memory. So you get exceptional I/O performance and greatly increased throughput.

Choose your configuration.

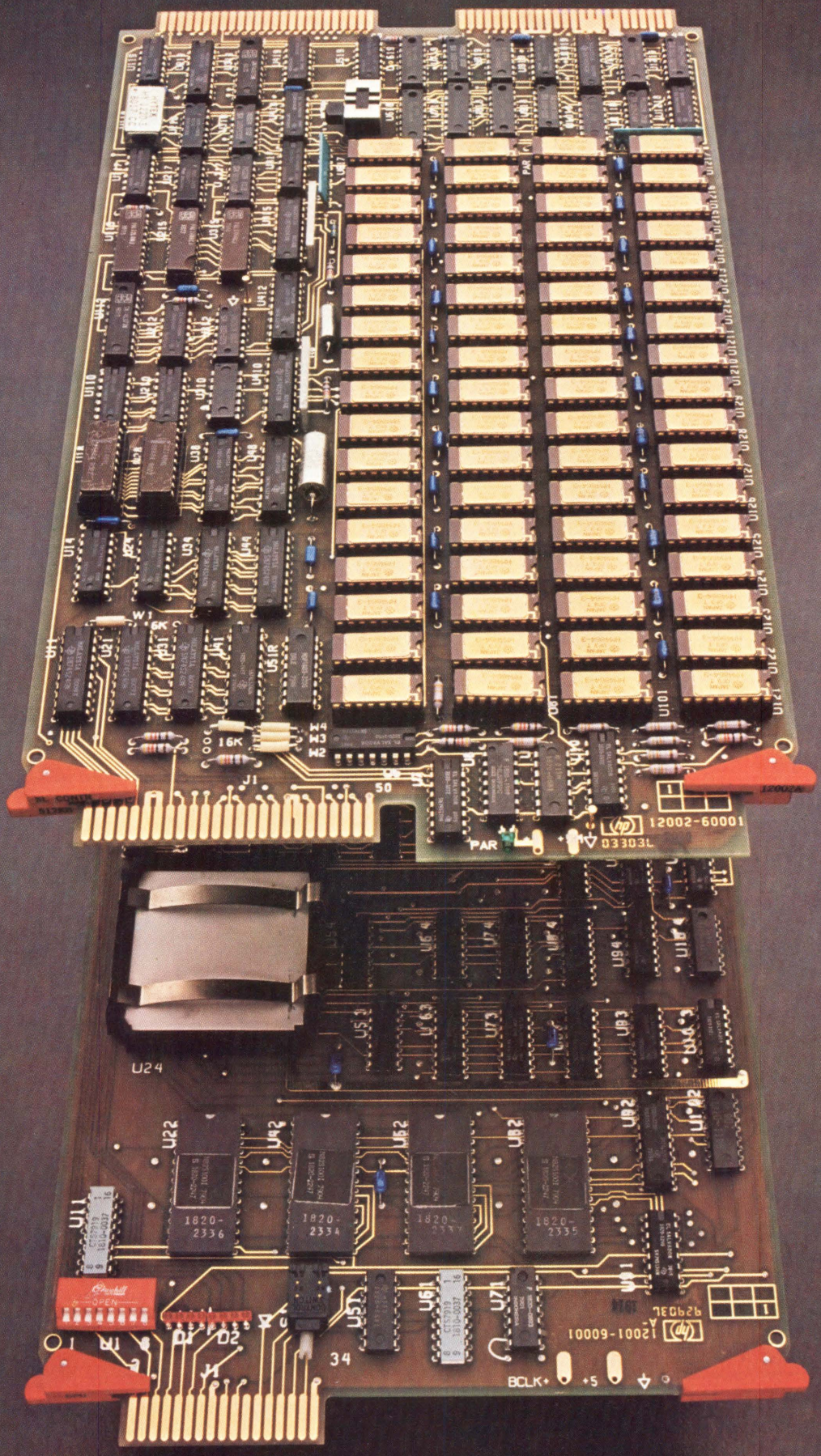
The HP 1000 L-Series comes in a wide range of board, box and system packages. Which means you'll be able to choose the configuration that's best for your application. Development units are available at $13,250* for the CPU and a full 1/2 megabyte of memory.

If a two-board, 1/2 megabyte microcomputer sounds like what you've been looking for, come in for a hands-on demonstration. Just call the nearest HP sales office listed in the White Pages. Or write for more information, and a copy of our new OEM catalog, to Hewlett-Packard, Attn: Joe Schoendorf, Dept. 1286, 11000 Wolfe Rd., Cupertino, CA 95014.

HEWLETT PACKARD

*Price is U.S. list.

22007 HPDS41


W1
16K
J1
50
12002-60001
03303L
PAR
U24
1820-2336
1820-2334
1820-2335
OPEN
D1
D2
34
BCLK+
+5

One board, one bus, one way environment for the '80s.

With Motorola MC68000 VERSAmodules, a single board offers all the functional versatility of competitive 16-bit systems at a fraction of the cost.

With VERSAmodules and the powerful VERSAbus™ interconnect, there's maximum utility, expandability, reliability and maintainability for a wide range of industrial, communication, lab automation and general business applications in one optimized system.

With the complete VERSAmodule family of circuit boards, system software, packaging and accessories the microcomputer system engineer can apply the power and versatility of the MC68000 MPU at a high level of system integration.

With VERSAmodules, you're into the '80s and beyond.

Most Powerful Microcomputer

The VERSAmodule Monoboard Microcomputer flagships the VERSAmodule family. Combining an MC68000 MPU, full VERSAbus interface, multiprocessor capability, substantial ROM/RAM, serial and parallel I/O and timer/counter functions, it's easily the most powerful single-board microcomputer yet offered. For designs requiring up to 128K bytes of ROM and RAM, plus two high-speed serial channels (up to 19.2K baud) and 40 lines of parallel I/O, this single board meets all system needs. Competitive approaches require two to four boards for the same capability, and, inevitably, more cost.

Total Software Environment

Many 16-bit applications, particularly in higher-performance, control-oriented areas, require a realtime, multitasking environment for efficient operation. By combining the ready-made RMS68K™ multitasking system software package with your VERSAmodule-based system, you can save the man-months of effort necessary to develop a system capable of managing resources efficiently in real time. Time and money saved can be used to apply your expertise to development of application programs.

to a total, 16-bit system VERSAmodules.™

New Generation Bus.

Supporting a mixture of 8- to 32-bit MPU architectures with high-speed transfer rates, VERSAbus offers a flexible, economical system bus ideal for industrial automation, communications or general business applications. VERSAbus is incorporated in the VERSAmodule chassis/card cage backplanes and willingly accomodates multiple processors. Designed-in ease-of-use for tomorrow's upgraded systems saves money by obviating major hardware and software redesign.

Inherent Reliability/ Maintainability.

VERSAmodule products support an unmatched level of system integrity. This includes reliability of the MC68000 with its advanced architectural features such as exception-processing and interrupt handling. These allow for graceful handling of common system problems such as bus error, illegal instruction, divide-by-zero, privilege violation, spurious interrupt, etc. This "soft-failure" capability alerts operating personnel and, in many cases, allows recovery before critical failure.

Reliability of VERSAbus-based systems is enhanced through power-fail detect and self-test features. AC-fail and power-down indication allow saving critical data in non-volatile memory through power outages. Self-test minimizes down-time by allowing manually-initiated self-test, when a problem is suspected, with failed boards indicated by on-board fault indication lights.

Versatile Development Support.

Unparalleled ease and efficiency in software development for VERSAmodules is yours through EXORmacs™ – a third generation 16/32-bit development system with state-of-the-art hardware architecture, advanced operating software and self-test capability. Pascal, FORTRAN and structured macro assembler allow choice of the language best suited to needs. A versatile, CRT-oriented text editor speeds up program preparation and modification. And a flexible linkage editor permits modular, top-down system development.

Again, less design time, lower cost and an earlier product operation date for a better bottom-line result.

Send for a new VERSAmodule brochure. Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036 or call (602) 244-5714.

Take a big step into the '80s with Motorola VERSAmodules.

Innovative systems through silicon.

MOTOROLA INC.

TO: Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.
73CD1/81

Please send me information on VERSAmodules.

Name _____

Title _____

Company _____

Address _____

City _____

State _____ ZIP _____

COMPARE PRINTER TERMINALS AND BE CONVINCED

After you compare* features and performance... then look at price. With the Digi-Data Model 2516 KSR printer terminal, you get more value at 16 to 30% lower cost.**

For that Receive Only application, our 2511 RO provides similar advantages. And once your Series 2510 is installed, you have the reliability of fewer components with no cooling fan required... and the serviceability of a single board controller.

After you compare, we know you'll be convinced... the Digi-Data 2516 is "FIRST IN VALUE".

DIGI-DATA CORPORATION
8580 Dorsey Run Road, Jessup, MD 20794
(301) 498-0200
... **First In Value**

*Specifications and pricing obtained from vendor literature for comparably equipped units.
**Substantial OEM quantity discounts available.

Printing Terminal
VALUE COMPARISON

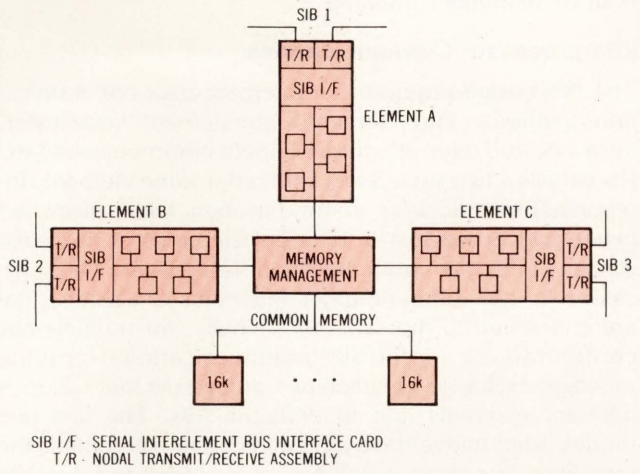
	DIGI-DATA 2516	TI 820	Tally T1612	HP 2635B
SPEED [Characters/sec]	150-200	150	160	180
SIZE Width	21.9"	26.0"	25.5"	25.2"
SIZE Depth	18.5"	21.0"	27.0"	23.0"
SIZE Height	8.5"	8.2"	8.5"	8.5"
WEIGHT [lbs]	39	40	69	56
Maximum BAUDRATE	19200	9600	9600	9600
EXTENDED BUFFER CAPABILITY	Yes	No	Yes	No
PRICE	$2150.	$2545.	$2605.	$3950.

DIGI-DATA CORPORATION
...First in Value!

CIRCLE 16 ON INQUIRY CARD

In a multibus system, the buses are tied together in clusters (Fig 3). Assuming bus 1 contains the node at which the system bootload function was initialized, element A will be bootloaded as described previously. Once bootloaded, its initialization software determines, by investigating its configuration table, that two other elements are part of this cluster and must be initialized. The other two elements in the cluster are initialized via common memory, and each of these elements in turn becomes the SIB controller for its respective SIB (element B for SIB 2 and element C for SIB 3). These elements provide the SIB controller functions which initialize their respective SIBs and bootload all their downloop nodes. Forwarding of the required programs from the bootload media at the SIB controller of SIB 1 to element A, into common memory of the cluster, and from there to the appropriate SIB for bootloading of its downloop elements follows.

A key feature of the initialization software is control and selection of which CPU (in a multi-CPU element) will handle the various I/O devices that are tied to the element. Since all I/O interface cards are tied to the intra-element bus (IEB), as are all CPUs, any of them can handle any of the I/O devices. Control is implemented by the AMD 2914 chip, which provides maskable interrupts. A new instruction was defined to permit control of this fail-safe feature.



SIB I/F - SERIAL INTERELEMENT BUS INTERFACE CARD
T/R - NODAL TRANSMIT/RECEIVE ASSEMBLY

Fig 3 Three-element cluster interconnecting three SIBs. Buses interface with each other at clusters in multiple-bus system

Interrupt Processing and Task Scheduling

In the DPS interrupt processing and task scheduling functions, all but one of the currently defined tasks in the SDEX/20 executive have been retained. The message task type of SDEX/20 has been replaced in the DPS implementation by a function entitled "standard message task." The DPS standard message task contains the SDEX/20 message task as a subset to provide compatibility with existing user programs.

The message handling function developed while implementing the standard message task is probably the most important function developed for the DPS software. It provides the major mechanism for communication between applications programs. Messages are addressed by program module number without knowledge of the physical location of the program module. Software module X can send a message to software module Y in any processor within the system.

The task scheduling function of both source and destination processors, in cooperation with the interprocessor communication functions described below, automatically routes the message to module Y. When module X wishes to send a message to module Y it uses a module number to address the message. Module Y may be assigned to the same CPU as that to which module X is assigned, to another CPU within the same element, to a CPU within a different element within the same cluster, to a CPU that is somewhere downloop, or to a CPU in a different SIB. The local copy of the executive contains tables that indicate which of the various processors in the configuration contains module Y. If module Y is not assigned to the requesting CPU, an appropriate message is composed and sent to the executive of the CPU that does control module Y.

In a multiple-loop system, all modules that are not contained within the loop are labeled as external to the loop by the module number routing table, and these messages are routed to the bus exit node. In Fig 3, for example, the cluster shows three elements, each of which operates as the bus exit node for its respective SIB. If the original request for module Y was made in SIB 1, element A extracts the message from the SIB, moves it into common memory, and, assuming that the message was for a node in SIB 2, alerts element B. The software module routing table in the bus exit node of SIB 1 need not know in which node of SIB 2 module Y resides—only that module Y is assigned to SIB 2. Element B of the cluster will have in its software module routing table the address of the SIB 2 node that does contain module Y. The multiple-loop approach is merely an extension of that which has already been implemented in the single-loop system.

The importance of this single modification, standard message task function, to the SDEX/20 executive cannot be overemphasized. The capability of user programs to call resources and/or pass messages to other user programs without knowing the physical location of the recipient of the call or message greatly reduces software development costs for all future systems. This feature also permits the partitioning of existing single-processor systems: user programs call for the executive, and the executive assigns the task to the same CPU. Standard message task function permits partitioning of such functions into physically distributed processors without modifying existing user programs. This is mandatory if move-

(continued on page 28)

ment from existing centralized systems to distributed processing systems is to proceed in an evolutionary, rather than revolutionary, manner.

Interprocessor Communications

The DPS design requires four interprocessor communication methods: intra-element, interelement/intracluster, intra-SIB, and inter-SIB. Intra-element communication exists between two processors within the same element. Interelement/intracluster communication takes place between two processors in different elements of the same cluster. Intra-SIB communication is between two processors of two different nodes (elements or clusters) that are connected to the same SIB. Finally, for multiple-bus configurations, inter-SIB communications provide message exchange between two processors that reside in different elements and in different SIBs. The first two modes listed above have already been implemented; the remaining two await development of cluster and dual-SIB configuration. Hardware and firmware design have advanced such that extensions of existing software design will permit implementation of these added capabilities.

Intra-element and interelement communication uses software to construct the messages, and firmware and hardware to interpret two new instructions: intra-element interrupt and interelement interrupt. *Intra-element interrupt* is performed by firmware that activates the intra-element interrupt line of the IEB. With the exception of the initiating CPU, all CPUs within the element are interrupted, and a 6-step 1.44-μs firmware routine examines a prespecified location in its dedicated memory to determine whether the interrupt is for its CPU. If it is, the interrupt handler is called; if not, control is returned to software without software awareness of the interrupt.

Interelement interrupt causes firmware in the source CPU to send a special code to the memory management unit indicating an interelement interrupt and specifying the element number within the cluster to be interrupted. The memory management card connected to the initiating element passes the signal via the common memory bus to the memory management card that interfaces with the destination element. The receiving memory management card activates the interelement interrupt line. Firmware in all CPUs within the element then examines a prespecified location in *common* memory to determine whether its software should be interrupted. Intra-SIB and inter-SIB processor communications are implemented by executive software use of the standard message task described earlier.

SIB Interface

Three major functions provided by the SIB handling portion of the DPS executive are SIB protocol, SIB I/O handling, and SIB controller function. The first two of these functions are replicated in every element connected to the SIB. The SIB controller function need to reside only in those nodes that are required to perform that function. If the currently assigned SIB controller fails, one of the other nodes containing SIB controller software automatically becomes the new SIB controller.

SIB protocol functions include examining the header of every received message and generating Acknowledge messages and other required responses. The received messages are then routed to the task scheduling function of the executive by the SIB protocol module. This portion of SIB executive software is also responsible for maintaining a table of messages that are to be transmitted to other elements via the bus, as well as retransmitting messages for which no acknowledgment was received. Finally, the SIB protocol software processes the configuration table update messages that are received from the bus controller, ensuring that all elements within the system have an updated status of the entire configuration.

I/O handling functions of the bus interface software are fairly conventional. They include registering tasks for all I/O interrupts received from the SIB, analyzing the status words associated with these interrupts, and sending commands to the bus interface hardware to cause messages to be received and transmitted. Additional functions consist of maintaining the buffers of the received messages and generating the checksum word for transmitted messages.

The only unconventional feature of this portion of the software is transmission of messages to the SIB interface

(continued on page 30)

The Idea:

To take the DEC™ VT100™ terminal and turn it into a sophisticated, yet economical graphics terminal.

Will wonders never cease? Not if Digital Engineering has anything to do with it. We're the pioneers in retrofit graphics. And this time we've turned DEC's VT100 alpha-numerics terminal into a full-fledged graphics terminal that features multiple character sizes, dot-dash lines, point plotting, vector drawing and selective erase for quick, easy updating of the graphics display.

We call this transformation The Retro-Graphics™ Enhancement. And while it begins with complete emulation of Tektronix® 4010 Series terminals—and compatibility with most existing graphics software, including Tektronix Plot 10™ and ISSCO's® DISSPLA® and TELLAGRAF®—there is much more to be said for this breakthrough. First, graphics are displayed on a 12" (diagonal) green-toned screen at 640 x 480 resolution. Refresh raster scan technology insures a bright, easy-to-read display. And all of the features that the DEC VT100 terminal begins with remain intact, including 96 upper/lower case ASCII characters, up to 132 characters per line, numeric and function keypads, detachable keyboard and a wide variety of screen customizing features.

The Retro-Graphics Enhancement for the DEC VT100 terminal. Whether you are looking for continuity with existing DEC products, or for a high-quality graphics terminal at hundreds less than the competition, ours is the right idea. For more information, write or call.

DIGITAL ENGINEERING

630 Bercut Drive, Sacramento, CA 95814
(916) 447-7600 TWX 910-367-2009

Retro-Graphics™ is a trademark of Digital Engineering, Inc. DEC™ and VT100™ are trademarks of Digital Equipment Corporation. Tektronix® and Plot 10™ are trademarks of Tektronix, Inc. ISSCO® DISSPLA® and TELLAGRAF® are registered trademarks of Integrated Software Systems Corporation.

hardware for reconfiguration in the event of failures in adjacent nodes or in either of the incoming links. Detection circuitry in the bus interface hardware notifies this software module whenever signal or signal synchronization is lost. The software module responds to that input, provides the software controlled reconfiguration, and permits continued operation in spite of such a failure.

System control functions reside within the SIB controller software modules, which need only to reside in those elements that contain the capability to operate as the SIB controller. However, this software may be active in only one node in any one bus at a given time. The functions of this software include initializing the bus, determining the initial status of all of the downloop elements, loading the software modules into the downloop elements, and issuing initialization orders to each of the downloop elements. Once the system has been initialized, the bus controller function periodically interrogates the status of all elements on that SIB, updates copies of the system tables that reside in the downloop elements, and reacts to various bus failures. For example, the bus controller function not only issues the initial go-ahead flag, which permits downloop elements to transmit, but also continues to monitor that flag to ensure that it is maintained within the loop. After appropriate timeouts, absence of the go-ahead flag will cause the bus controller to reissue the go-ahead in order to reestablish bus communication. Failure of the go-ahead to return indicates that there is a failure somewhere within the loop and that a reconfiguration has probably occurred.

I/O Handling

All DPS I/O devices are connected to an element via an I/O interface circuit card. Software I/O handlers are provided to deal with each of the peripherals. The I/O handlers implemented for the demonstration system (Fig 1) are tape, display, and SIB. With one exception, I/O handler functions are standard: registering tasks to handle I/O interrupts, analyzing device status words, and commanding the device. This added I/O handling function in the DPS permits communications with other software modules to perform various functions, also allowing applications programs to communicate with devices not in their element. A program may format and output data to a display in another element.

Memory Allocation

Two types of memory, local and common, are defined. As currently implemented, all local memory is accessible by all CPUs. However, hardware capability allows a mixture of shared and private memory for each CPU in a multi-CPU element. Consistent with UYK-20 and AYK-14 architecture, memory is divided into pages of 1024 words each. To maximize memory use, pages have been subdivided by the DPS memory allocation module into blocks of four words each. Any number of blocks may be assigned. Each page has eight blocks of header information and 248 blocks for storage.

Summary

Software developed for the DPS provides three new functions: complete system initialization by pushing one button, reconfiguration in the event of node or SIB failure to permit continued operation, and the ability of any user program to call any other without knowledge of the called program location. With the hardware development of the dual-SIB system, these functions will be extended to the full capability required by the system.

References

1. R. Mauriello, "A Distributed Processing System for Military Applications—Part 1: System Overview," *Computer Design*, Sept 1980, pp 14-30
2. R. Mauriello, "A Distributed Processing System for Military Applications—Part 2: The Serial Data Bus," *Computer Design*, Oct 1980, pp 14-36
3. R. Mauriello, "A Distributed Processing System for Military Applications—Part 3: The Computers," *Computer Design*, Dec 1980, pp 22-38

DPS Executive Functions

Initialization

Interrupt processing and task scheduling

Bus interface

I/O handling

Memory allocation

DPS Executive Software Requirements

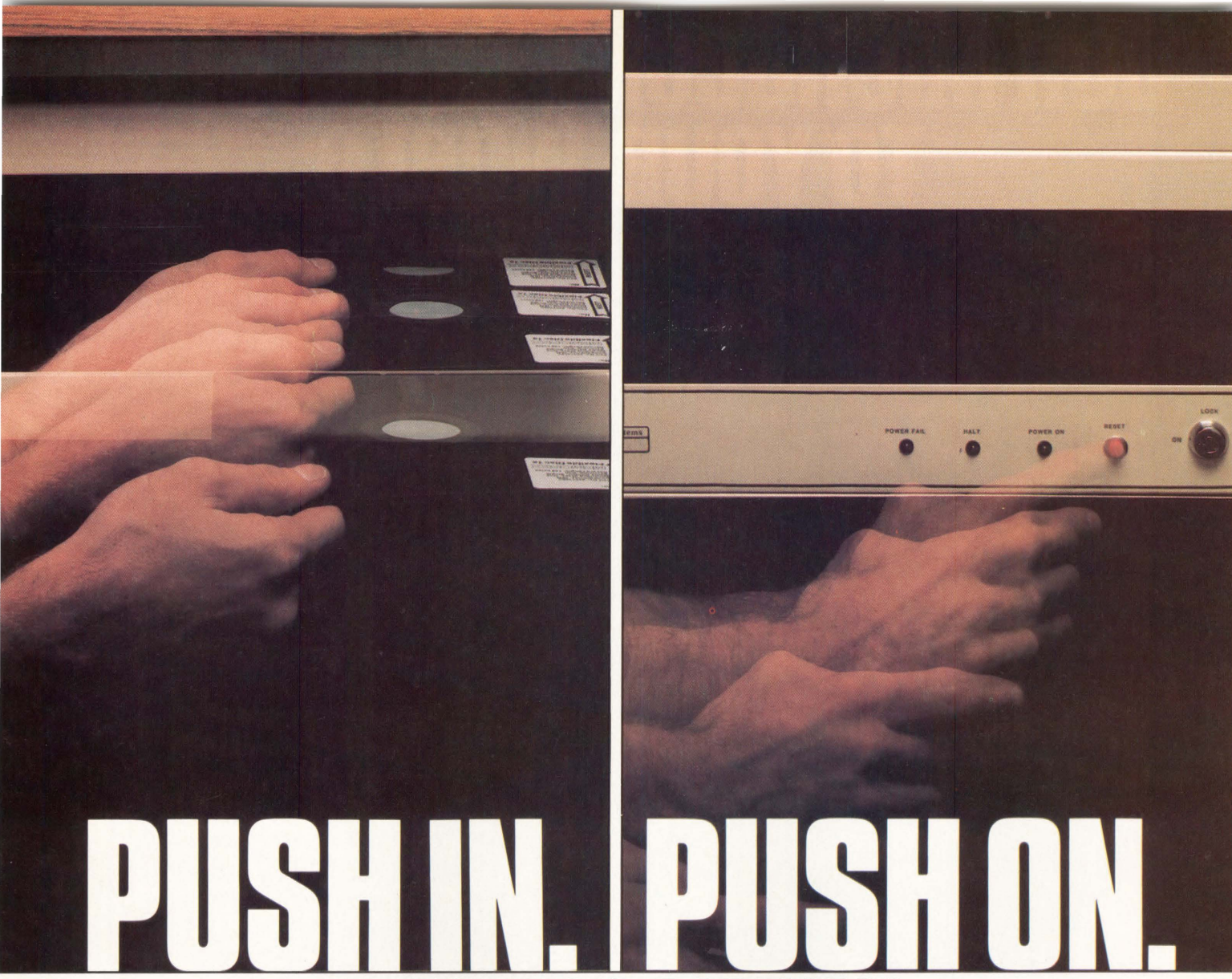
Support system initialization

Support monitoring and control

Support reconfiguration

Permit use of existing UYK-20 user programs

Permit user programs to call for resources or exchange data without knowledge of the location of the called resource or other user program



PUSH IN. PUSH ON.

MAKING MINIS OUT OF MICROS.

Here's the system builder's solution for successful computers and applications. Push in the CCS component. **Push in** the operating software. And **push on** with your application. CCS systems and components are designed to go together quickly, and to keep running reliably, with a proven return rate of less than 1%.

And you get performance. The systems deliver hardware vectored interrupts and interleaved DMA data transfers with rates as high as two megabytes per second, plus "virtual like" bank select memory of up to 512K bytes. This 8-bit system provides single user, multiuser, and multitasking capability with ample speed to prevent operator waiting or loss of incoming real-time data.

The systems are available with CP/M or MP/M operating systems. For real-time or multiuser applications, the CCS OASIS real-time multitasking operating system supports re-entrant programs and relocatable code modules, with facilities for task-to-task communication, file protection, time-of-day bookkeeping, spooling, task overlay, dynamic memory management, ISAM file structures and device-independent I/O. CCS OASIS includes debug, text editing, linkage, and file sort utilities; the system supports a host of existing languages, applications, and utilities from a range of vendors.

○ Please have a sales representative call me.
○ Please send more information on CCS Systems and Expansion Modules.

Name _____
Company _____
Address _____
City/State/Zip _____
Phone: ( ) _____

California Computer Systems
250 Caribbean Drive
Sunnyvale, CA 94086
(408) 734-5811

Powerful computer systems you can configure to your demanding requirements quickly, and with confidence. Choose from a variety of systems. Expand with CCS board-level modules for memory, disk control, high-speed arithmetic, and I/O, plus subsystems for floppy and hard disk storage.

If you sell, install, or use computer systems, you should know more about the CCS product line. **We've got a lot more to tell. Tear out and return the coupon for more information. Or call.**

CP/M and MP/M are trademarks of Digital Research. OASIS is a trademark of Phase One Systems.

CIRCLE 19 ON INQUIRY CARD

OUR MICROCOMPUTER TALKS TO YOUR WORLD.

When you need a powerful processing system that talks to your world... you need a COMMANDER COMPUTER. Four standard RS-232C ports handle serial data to 19,200 baud, allowing you to add low speed peripherals or even communicate with remote devices over a phone line. But if you need higher speed or more flexibility, use COMMANDER's parallel I/O under program control. And, if that's not efficient enough, select the optional DMA port to process parallel data on a cycle-steal basis direct to memory. COMMANDER's optional IEEE/488 controller gives you direct interface to the world of instrumentation and a host of compatible devices readily available. The optional Real Time Interface module gives you individual bit I/O to input status lines and digital sensor signals ...or to output alarms and commands. And you can use up to four independent programmable real time clocks for precise time interval control without wasted processor time. Inquiries for custom features are welcome.

BUT THAT'S NOT ALL...Select the COMMANDER configuration to fit your system need. The models 500 and 900 have an integral CRT and keyboard while the models MX and FX (not pictured) can be married to a simple terminal for operator interface. Add the optional arithmetic unit for high speed fixed point or floating point processing. And, if your application requires graphics, optional memory is added to provide 512x256 video graphics capability.

All COMMANDER models will execute higher level programs in BASIC, FORTRAN or COBOL or machine level programs in MACRO-80 Assembler. Operating programs are executed under CP/M™ FDOS, the new MP/M™ operating system or UCSD Pascal.™

COLUMBIA
DATA PRODUCTS, INC.

Computer Systems Division
8990 Route 108
Columbia, MD 21045
Tel: 301-992-3400 TWX: 710-862-1891

CIRCLE 20 ON INQUIRY CARD

™CP/M and MP/M are trademarks of Digital Research

Systems Architecture, Products Developed To Support Information Distribution Networks

Distributed systems architecture (DSA) and a set of system and hardware products designed to operate within the rules and protocols embodied in DSA have been announced by Honeywell Information Systems, 200 Smith St, Waltham, MA 02154. The architecture is consistent with the reference model of the International Standards Organization open system architecture (Fig 1) and supports X.25 and X.21 packet- and circuit-switched network protocols. DSA has been characterized by the company as a flexible open system and network architecture that eliminates the need for a hierarchical organization of processing elements in a network.

The product set includes Datanet 8, (DN8) frontend network processor (FNP); distributed network supervisor (DNS), the communications software package for the DN8; and distributed system satellite (DSS) hardware/software system that runs as a satellite processor in a DSA network.

DN8 handles communications in a DSA network for a DPS 8 or Level 64/DPS host computer using GCOS 8 and GCOS 64 operating systems respectively. Its central processor operates asynchronously under firmware control. All data transfers between elements are via a high speed bus at rates to 6M bytes/s. The DN8 can accommodate 2-, 8-, or 16-channel interface bases. Low, medium, and high speed terminals, up to 56k bits/s, can be connected. Synchronous and asynchronous and combinations of half- and full-duplex modes are also supported.

The channel interface base accepts up to four communication channel interfaces in combinations of any two transmission types: RS-232-C dual synchronous and dual asynchronous, to 9600 bits/s each; HDLC RS-232-C, one channel up to 9600 bits/s; HDLC wideband, one channel up to 56k bits/s; and HDLC wideband CCITT V.35, one channel up to 56k bits/s. The basic DN8 FNP includes 256k-byte memory, diskette, and automatic control function, and can be configured with up to two channel interface bases. One host connection and one 30- or 120-char/s communications console are required.

DNS is the communications software specifically designed for the DN8 FNP and with other DSA elements in a communications intensive data processing network. It supports up to four communications management functions in the DSA architecture as well as terminal management in a secondary network attached to the network processor. DNS also supports public data and value-added networks, including X.25 packet-switched and X.21 circuit-switched networks.

DSS hardware/software system allows a Level 6 small computer to act as a satellite processor (Fig 2) and to communicate with a host computer in the DSA network using HDLC protocol on leased lines. It can also control a local network. One leased line at a time can be used for DSS-host connection using point to point 2-way simultaneous HDLC protocol, allowing speeds up to 9600 baud in RS-232/V.24 interface mode.

Circle 321 on Inquiry Card

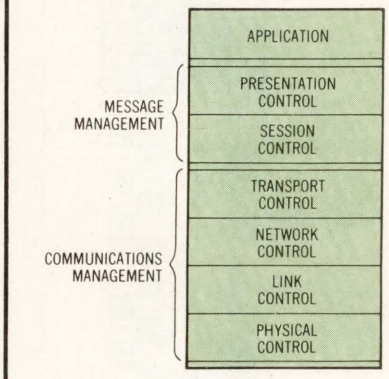


Fig 1 Layered functional structure of DSA. Four communications management layers are involved in data transfer across public or private networks. Message management layers handle logical flow of data between processes. Activities and application processes reside in application layer

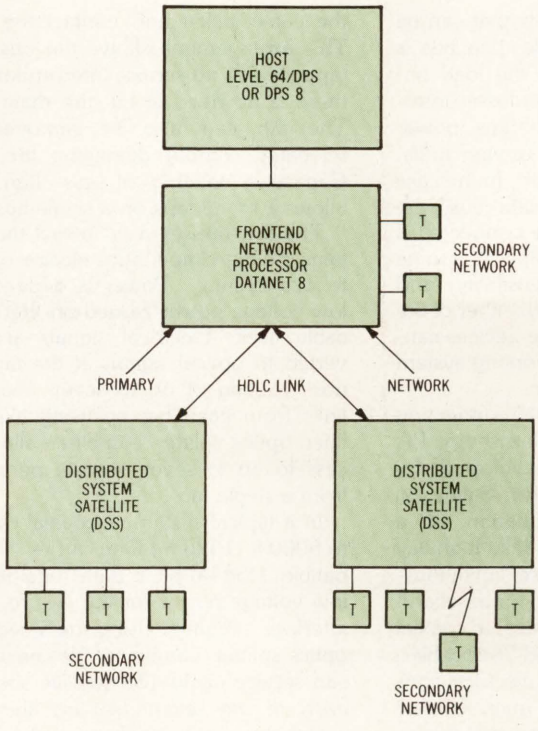
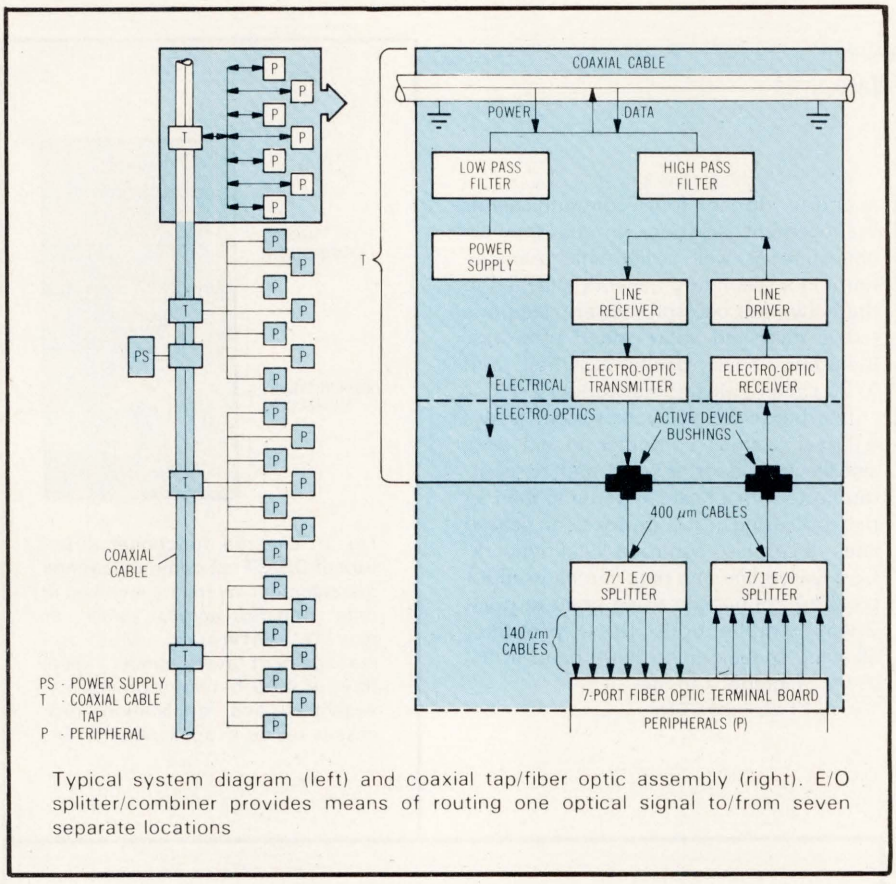


Fig 2 Example of DSA network. DSS is entry level satellite processor for use in DSA network

Hybrid Coaxial/Fiber Optic Highway Developed for Local Data Distribution



Typical system diagram (left) and coaxial tap/fiber optic assembly (right). E/O splitter/combiner provides means of routing one optical signal to/from seven separate locations

The number of remote units that can be tapped into a coaxial cable data bus is limited by such factors as the load imposed by each tap, insertion losses introduced by a large number of taps, power handling capability of the driving units, and the data speeds involved. In the case of a straight fiber optic data bus, the number of units that can be connected is similarly limited by the optical source power output, detector sensitivity, and cable/connector losses. With either of the transmission media, satellite devices cannot easily be added to a working system without interrupting service.

A combination of interconnecting hardware from AMP Inc, Harrisburg, PA 17105, and circuitry developed by Xycom Inc, 750 N Maple Rd, Saline, MI 48176, enables implementation of a hybrid coaxial/fiber optic data highway that offers relief from these limitations. The configuration, designed for baseband coaxial systems, incorporates a coaxial tap, suitable for both 50- and 75-Ω cables, that makes mechanical and electrical contact by clamping to the main coaxial cable. Spring loaded probes pierce the insulation and contact the center conductor while two sets of ground springs pierce the cable jacket and contact the braid. This arrangement allows the bus to be tapped with no service interruption since there is no need to cut the main cable. The tap can also be removed and relocated without damaging the cable. Capacitive loading of less than 3 pF allows a many taps on a single bus.

The tap houses a PC board that contains the high impedance electro-optic interface circuitry. Power is derived from low voltage power carried on the coaxial cable itself. Electrical signals are converted to optical signals at the tap location; routing of up to seven fiber optic links from each tap by using a passive fiber optics splitter/combiner allows access to up to seven remote peripherals from a single tap.

In a typical system, a coaxial cable up to 5000 ft (1525 m) long carries TTL compatible 1.544M-bit/s data together with low voltage power for the electro-optical interface circuitry. Using the 7-way fiber optics splitter/combiner, 19 coaxial taps can service up to 133 satellite sites, and each of the seven 140-μm fiber optic cables can carry signals up to 1 km from the tap location.

Circle 322 on Inquiry Card

Program 9900 µPs in half the time. AMPL lab and 16-bit Pascal. The Texas Instruments time savers.

The AMPL* microprocessor prototyping lab can shorten overall program development time by 30 to 60%. For example, correcting an error in a 1000-line program on a typical assembler can take 30 minutes. For the AMPL user: less than a minute.

The AMPL lab is a complete set of software and hardware development tools for TI's 16-bit 9900 Family of microprocessors and TM990 microcomputer modules. Pascal, Fortran and TI's Power Basic high-level languages are available as options.

Improves productivity

Carefully planned, mature and field proven, the AMPL lab boosts programming output. Contributing to its productivity:

- Programmability — Using a Pascal-like command language, the AMPL lab can be programmed with complex test and debugging sequences. Locating problems is automatic. A line-by-line assembler and disassembler make quick fixes easy.
- Real-time emulation — Checks programs on the spot, step by step. No wait states, full execution speed.
- Logic-state trace — Rapidly establishes breakpoints, traces addresses and data.
- Microprocessor Pascal — Adding TI's Microprocessor Pascal to the basic AMPL lab provides a complete system including source editor, compiler, host debugger, configurator, native-code generator, and run-time support.

The AMPL lab is also easy to use. Self-prompting, menu-driven, load-and-go.

More cost-effective uses

For even greater cost effectiveness, the AMPL lab can be used for product maintenance in debugging systems returned from the field. To help with incoming inspections. As a word processor to generate documentation.

Incorporating TI's 990 minicomputer, the AMPL lab is backed by nationwide service.

See the AMPL lab save time. Arrange a demonstration with the Distributor Field Applications Engineer at the Systems Center nearest you (see listing at left). Ask for a copy of the AMPL brochure, CL-461. Or write Texas Instruments Incorporated, Box 1443, M/S 6404, Houston, Texas 77001.

TEXAS INSTRUMENTS
INCORPORATED

85704D

CIRCLE 21 ON INQUIRY CARD

Program out a
Integrated

Signetics' new IFL Series 20 maximizes design flexibility, lowers power dissipation, and cuts parts count.

Integrated Fuse Logic is Signetics' answer to TTL logic replacement. With our versatile IFL family, you can turn almost any logic design into hardware with just a handful of programmable parts. You'll save design time, reduce inventory, and improve system performance in the process.

Our new IFL Series 20 packs superior performance into 20-pin, PAL-compatible DIPs. Besides offering I/O structures and AND arrays that are fully programmable, the IFL Series 20 gives you unique features that maximize both design flexibility and cost effectiveness with only three standard architectures: FPGA, FPLA, and FPLS.

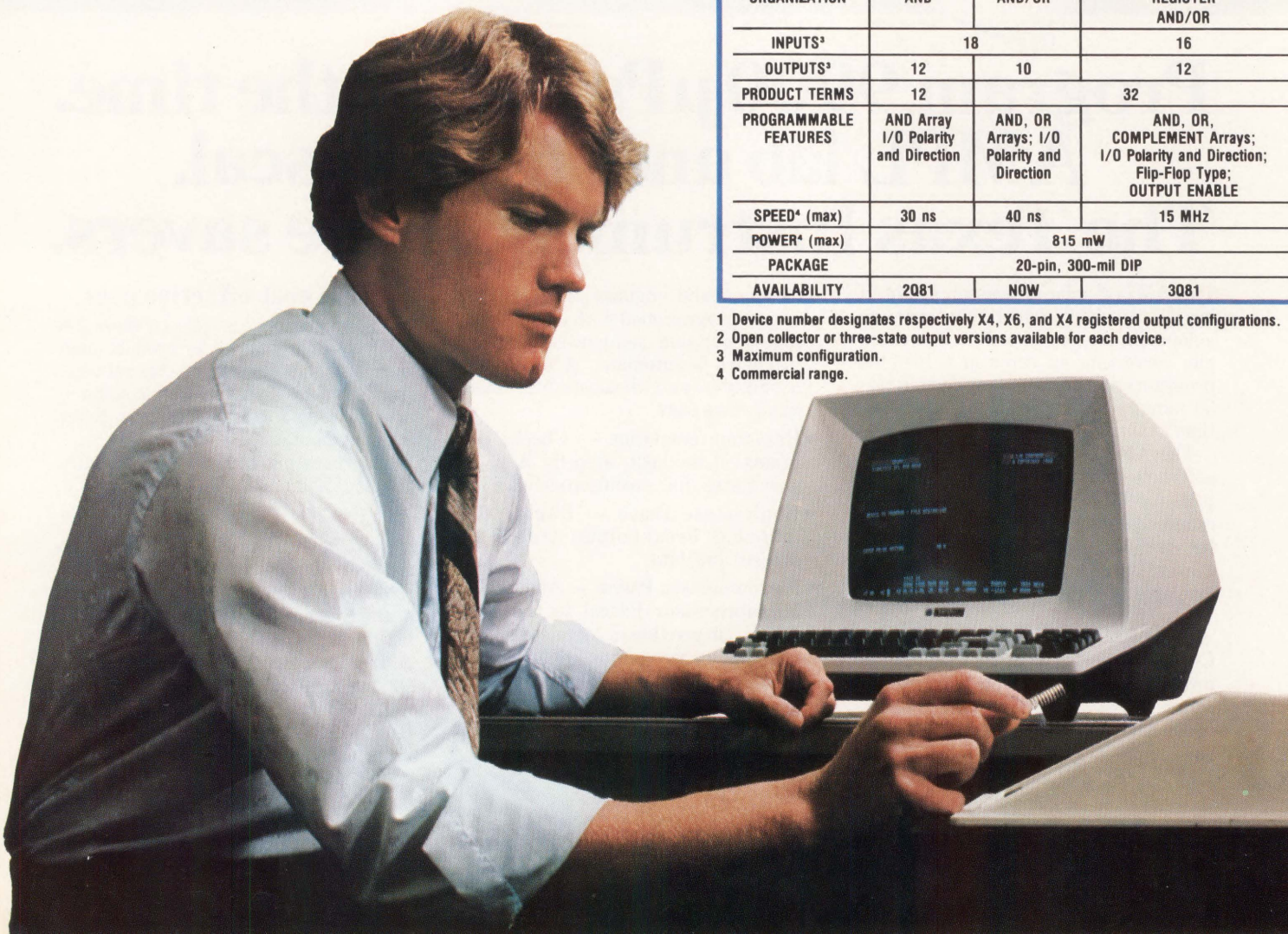
For starters, each IFL Series 20 device uses 815 milliwatts, maximum. That's 30% less power at the same speed than comparable field programmable elements. Lower power means greater reliability.

And thanks to open collector output options, IFL Series 20 lets you synthesize functions with greater complexity and faster switching speeds.

Series 20

	FPGA	FPLA	FPLS[1]
DEVICE[2]	82S150/151	82S152/153	82S154/155 82S156/157 82S158/159
ORGANIZATION	AND	AND/OR	REGISTER AND/OR
INPUTS[3]	18		16
OUTPUTS[3]	12	10	12
PRODUCT TERMS	12	32	
PROGRAMMABLE FEATURES	AND Array I/O Polarity and Direction	AND, OR Arrays; I/O Polarity and Direction	AND, OR, COMPLEMENT Arrays; I/O Polarity and Direction; Flip-Flop Type; OUTPUT ENABLE
SPEED[4] (max)	30 ns	40 ns	15 MHz
POWER[4] (max)	815 mW		
PACKAGE	20-pin, 300-mil DIP		
AVAILABILITY	2Q81	NOW	3Q81

1 Device number designates respectively X4, X6, and X4 registered output configurations.
2 Open collector or three-state output versions available for each device.
3 Maximum configuration.
4 Commercial range.



lot of TTL with Fuse Logic.

You also get programmable output polarities to eliminate the need for external parts. Because each IFL device lets you program both active high and active low outputs.

With the IFL Series 20 logic array (FPLA) and logic sequencer (FPLS), you'll achieve higher speeds and greater logic density via programmable "OR" arrays. These allow you to "edit" logic functions even after delivery of systems to the field by just reprogramming spare gates.

Series 28

FPGA	FPLA	FPRP	FPLS
82S102/103	82S100/101	82S106/107	82S104/105
AND	AND/OR		REGISTER AND/OR
16			
9	8		
9	48		
AND Array I/O Polarity	AND, OR Arrays; I/O Polarity	AND, OR Arrays; INPUT Polarity	AND, OR, COMPLEMENT Arrays; INPUT Polarity
35 ns	50 ns	70 ns	11 MHz
895 mW			945 mW
28-pin, 600-mil DIP			
NOW			

Moreover, the Series 20 FPLS allows you to:

- Save I/O pins and minimize AND gates with on-chip complement array.
- Optimize AND gate allocation in counting, shifting, and data buffering applications with programmable J/K, D, or T flip-flop options.
- Save AND gates and free package pins for control functions with bi-directional flip-flops that can handle I/O bus data, or convert to direct input mode.
- Use synchronous clocking together with asynchronous flip-flop preset and clear for clock override or initialize functions.
- Gain additional programming capabilities—including Boolean equation entry with standard programmers.

Programming the IFL family is simple. Many standard PROM programmers selectively open fusible links on our IFL parts. Intact fuses couple all logic blocks for the desired function.

IFL Series 20 now complements our field-proven IFL Series 28, specially designed for high-end applications demanding greater I/O capability.

Find out how you can program flexibility into your next logic design with IFL Series 20, Series 28—or a *combination of both*. Write us today. Or contact your nearby Signetics sales office or authorized distributor.

Signetics Corporation, 811 E. Arques Avenue, P.O. Box 409, Sunnyvale, CA 94086. (408) 739-7700.

signetics

a subsidiary of U.S. Philips Corporation

Multiple Technologies from 8 Divisions:
Analog, Bipolar Memory, Bipolar LSI, MOS Memory, MOS Microprocessor, Logic, Military, Automotive/Telecom

To: Signetics Publication Services, 811 E. Arques Ave., P.O. Box 409, MS27, Sunnyvale CA 94086

Please send me more details on your: ☐ IFL Series 20 ☐ IFL Series 28 ☐ FPGA ☐ FPRP ☐ FPLA ☐ FPLS

☐ My need is urgent; have an applications specialist phone me at once: ( )_____.

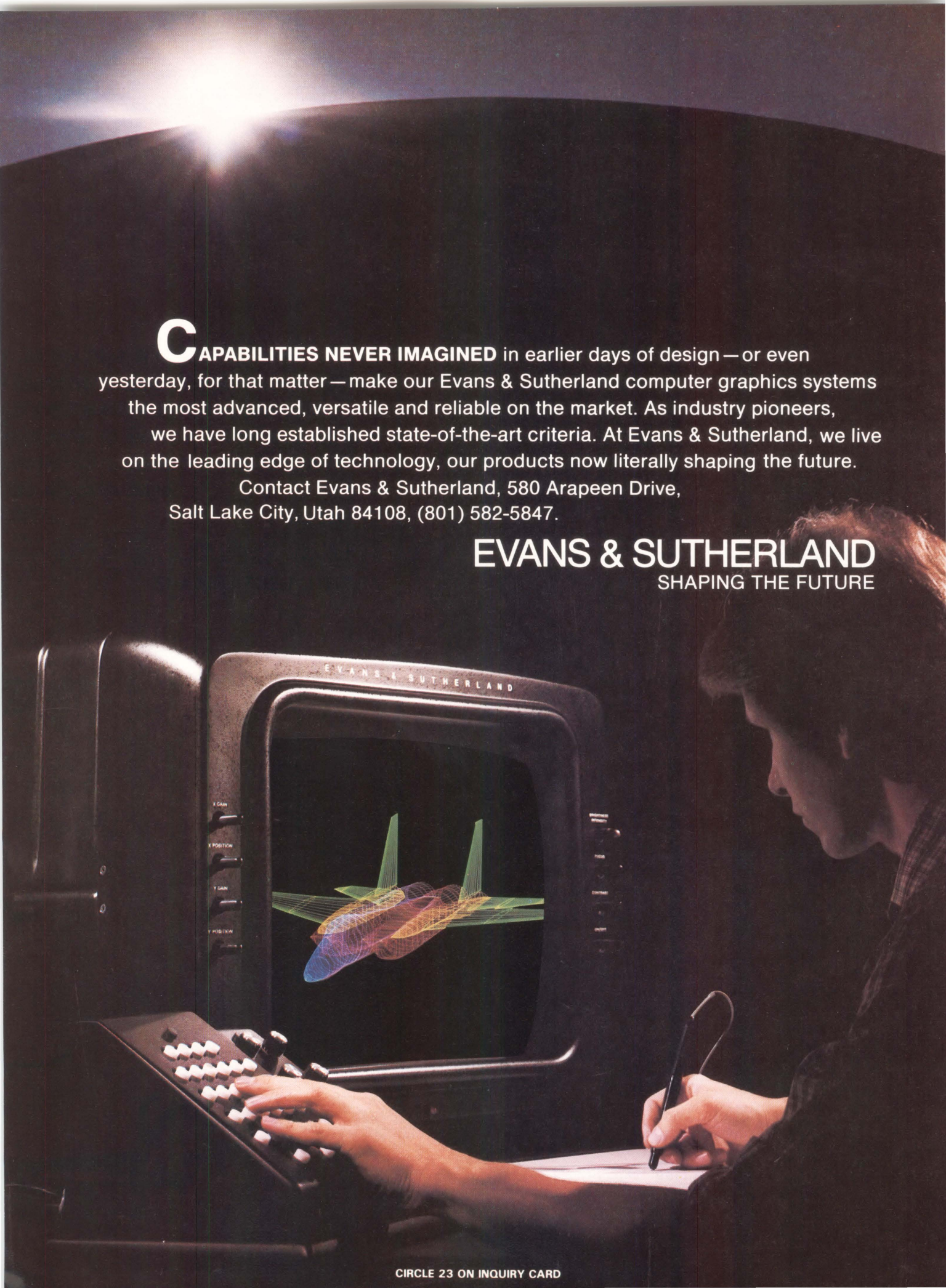
Name_____ Title_____

Company_____ Division_____

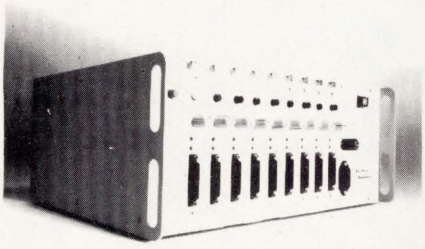
Address_____ MS_____

City_____ State_____ Zip_____

CD181


CAPABILITIES NEVER IMAGINED in earlier days of design—or even yesterday, for that matter—make our Evans & Sutherland computer graphics systems the most advanced, versatile and reliable on the market. As industry pioneers, we have long established state-of-the-art criteria. At Evans & Sutherland, we live on the leading edge of technology, our products now literally shaping the future.
Contact Evans & Sutherland, 580 Arapeen Drive,
Salt Lake City, Utah 84108, (801) 582-5847.
EVANS & SUTHERLAND
SHAPING THE FUTURE
EVANS & SUTHERLAND
CIRCLE 23 ON INQUIRY CARD

Port Concentrator Optimizes Channel Capacity Use In Univac Systems



Univac compatible true port concentrator. Device can operate in either remote or local mode for either computer port or terminal cluster

Unlike port limited time division multiplexers and statistical concentrators, model 871 true port concentrator, designed specifically for Univac computers, allows free interface with a mix of terminals, including hard copy and CRT devices, at various speeds. It enables a single Univac system port to support 31 nodes of 8 drops each, for a total of 248 devices. Data rates of the terminals can range from 110 to 19.2k bits/s, and communication with the computer system is via UTS 400 protocol.

The port concentrator is a product of Kaufman Research Manufacturing, Inc, 14100 Donelson Place, Los Altos Hills, CA 94022. It supports any number of ASCII devices, including special or nonstandard terminals. The concentrator uses three modules: controller, power, and line interface module(s) (LIM). Once the basic concentrator is in place, ports can be added by installing additional LIMs. Since no terminal interacts with any other, performance is not affected by expanding the number of terminals.

Each LIM provides selectable baud rates and line protocols. The interface is selectable, RS-232, DTE, or DCE. The concentrator chassis is 7 x 17 x 12″ (18 x 43 x 31 cm), mounts power supply and controller/converter, and has space for up to eight LIMs. Power requirement is 115 ± 10% Vac, 47 to 63 Hz, 115 W. 230-Vac operation is an option. The company has also introduced model 870 port concentrator that provides similar capabilities for IBM 3270 protocols.

Circle 323 on Inquiry Card

Interactive Test System Provides Extensive Diagnostics and Analyses

Interactive test system INTERVIEW[R] 4500 for data communications protocol diagnostics includes features designed for packet protocols and SNA, plus detailed frame analysis of HDLC and SDLC. Bisync, async, IPARS, EBCD, XS-3, Selectric, and EBCDIC are also standard in the unit. The system is from Atlantic Research Corp, 5390 Cherokee Ave, Alexandria, VA 22314, and uses an advanced version of the self-teaching trigger technique introduced in the company's INTERVIEW 3500 programmable data analyzer (*Computer Design*, Jan 1980, pp 32-33). Since it is unnecessary to learn an instruction set to program a test, minimal operator training is required.

A functionally labeled and color-coded keyboard, self-teaching menus, and training tapes facilitate operation of the system. The CRT displays all microprocessor prompted menu choices with all unnecessary or conflicting selections deleted. Major features of the system include emulation of host, terminal, and node. Network performance measurements performed by counters and timers can be viewed in real time. An integral tape stores test results plus 600k data characters. The analyzer contains a slot for an optional 128k-byte RAM capture memory for 56k-bit/s recording.

The system is capable of simultaneous search for multiple strings of 16 characters each. Four bit masks per string permit search and analysis of specific bit configurations. 16 user definable transmit messages are available.

Present users of the company's 3500 analyzer are offered a field conversion kit to change it over to a fully operational 4500 system. Data tapes are directly interchangeable.

INTERVIEW 4500. Graphic display guides user in entering timing relationship between data and interface leads

Circle 324 on Inquiry Card

Communications Processor Distributes Intelligence Throughout Data Network

A family of processors for management of remote networks, ICOT 257 series permits the distribution of intelligence and control functions via its microprocessor-per-line architecture and special bus system called ICOBUS[TM]. The bus, plus a firmware library, handles incompatibilities in code, speed, and protocol. Protocols that may currently be exchanged through the bus include Bisync, Uniscope, ASCII TTY, X.25/HDLC, SNA/SDLC, PARS, and P1024. Others are available on request.

The processor, developed by Microform Data Systems, Inc, 830 Maude Ave, Mountain View, CA 94043, performs all routine network management functions operating as a remote network processor. These functions include polling, message editing and processing, queuing, priority scheduling, diagnostics, error recovery, statistics gathering, and security.

A line concentrator function buffers data from incoming lines for retransmission at high speeds over a lesser number of designated output lines. The processor accommodates data rates to 9600 bits/s, and the standard unit can handle up to 13 full duplex I/O lines.

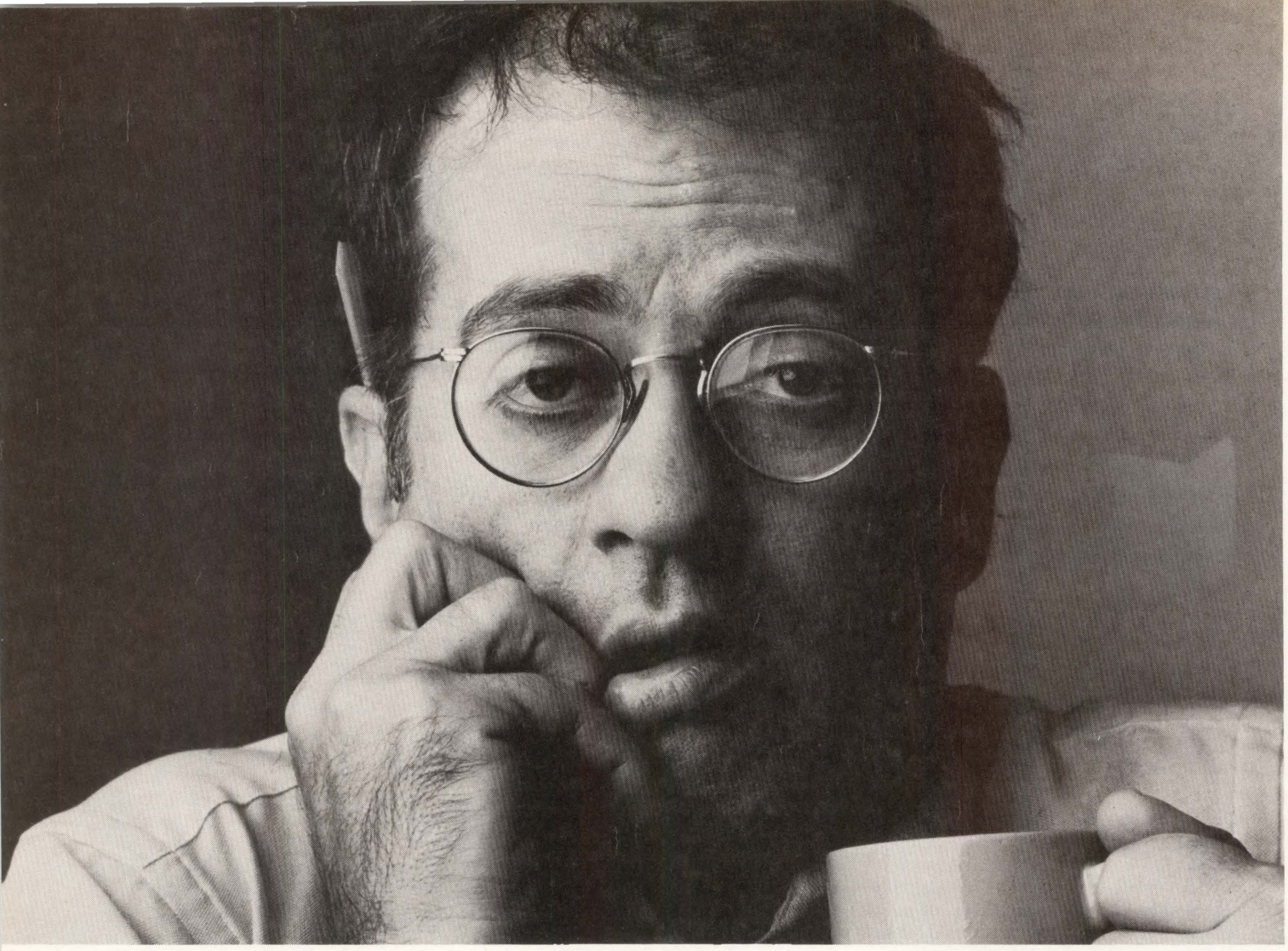
A message switching function selectively routes data to other attached terminals, any of several hosts, any other processor on the network, or to an external network. Network terminals and processors can access incompatible hosts and nodes.

Providing migration to SNA/SDLC and other integrated network architectures, the processor series supports network segments using asynchronous and synchronous protocols simultaneously with segments that have been converted to bit oriented protocols such as SDLC or HDLC. This can extend the useful life of existing terminals that are incompatible with new networks.

Series firmware is in three levels. Physical control level handles all physical character interrupts and executive functions; a second level handles message protocols; the third, or application level, is modified as needed to meet the code exchange, routing, and special processing requirements of each application.

Hardware for the processor series includes 48k RAM system memory and timing boards, and up to 13 communications processor boards. Each board has 6k to 12k bytes of P/ROM and/or ROM, 2k bytes of RAM, an interrupt processor, and a serial line interface.

Circle 325 on Inquiry Card



SOFT ERRORS CAN BE HARD ON YOUR SYSTEM.

Your RAMs are getting denser. Your soft error rate is getting higher. And you're getting a headache.

Soft errors, alpha particles, system crashes, hard errors. Take it easy. Relax. There's a simple solution.

Introducing the Am2960 Error Detection and Correction (EDC) Unit.

The Am2960 EDC corrects single-bit errors and detects double-bit errors. It's easily expandable from 16-bits wide to 32 or 64 bits. Its worst case speed is an amazing 34ns detect, 64ns detect and correct! And best of all, it's available right now.

You want byte operations? You got 'em. You need initialization, error logging and diagnostic capabilities? No problem. The Am2960 gives you all the functions of 25 to 50 TTL packages on one chip.

And if you're worried about the data path, don't be. Our slim 24-pin Am2961 and Am2962 EDC Bus Buffers solve the complete interface problem between the RAM, the EDC unit and the system data bus.

There's just no easier, cheaper, faster way to find and fix errors than the Am2960.

Bipolar LSI: The Simple Solution.

Our new Am2960 family of bipolar LSI and interface dynamic memory support devices will help you maximize your system's performance and reliability, minimize its chip count and cost.

And you won't find higher quality parts. Since the day we opened for business we've given every single part we make MIL-STD-883. For free.

Get the Am2960 Error Detection and Correction Unit. It'll be good for your system.

Advanced Micro Devices

901 Thompson Place, Sunnyvale, CA 94086 · (408) 732-2400
Right, From The Start.

CIRCLE 24 ON INQUIRY CARD

COMMUNICATION CHANNEL

Minicomputer System Adds Adapter for Communications Functions

Communications capabilities have been added to the F/4000 minicomputer system introduced last year (*Computer Design*, May 1980, p 267) by Formation Inc, 823 East Gate Dr, Mt. Laurel, NJ 08057. The F4700 communications adapter allows the computer to act either as a host or a node in a network of systems in a distributed processing environment. Functionally equivalent to IBM's 4331 communications adapter, it emulates IBM 270X SDA Type II and supports standard IBM software.

The adapter allows the movement of programs as well as data. It operates with a synchronous RS-232-C/V.24 modem, supplied by the user, on each of two 9600-bit/s ports. Switched or private line, point to point or multipoint configurations are supported. Local Bisync terminals can be attached with no need for a modem.

Each adapter allows two communication lines with an aggregate data rate of 19.2k bits/s max to be connected to the minicomputer system. Each line appears to the system as a subchannel of the byte multiplexer channel. The adapter occupies one standard slot in the minicomputer backplane, and up to eight adapters can be supported by the system. Two adapters attached to a single modem via EIA switches provide redundancy.

Single board design uses minimal hardware implementation; virtually all protocol-specific functions are microcoded, and the microcode is loaded into writable control store on power-up. Maintenance microdiagnostic is another microcode feature. Executed at system power-up under control of the system control processor (SCP), it reports any detected problems to the SCP, which takes the communications adapter offline and notifies the operator.

Circle 326 on Inquiry Card

Alarm Panel Automatically Detects RS-232 Circuit Fault Conditions

Digital alarm panel 5977 detects carrier failures in point to point networks and indicates streaming modem conditions in multipoint networks. The device allows continuous monitoring of one RS-232 type circuit from any one of 16 modems, or up to 16 circuits within a single RS-232 interface. If any of the circuit signals exceeds a preselected timeout period, an audible alarm and visual indicator alert the operator to the occurrence of a fault. The panel is available from T-Bar Inc, 141 Danbury Rd, Wilton, CT 06897.

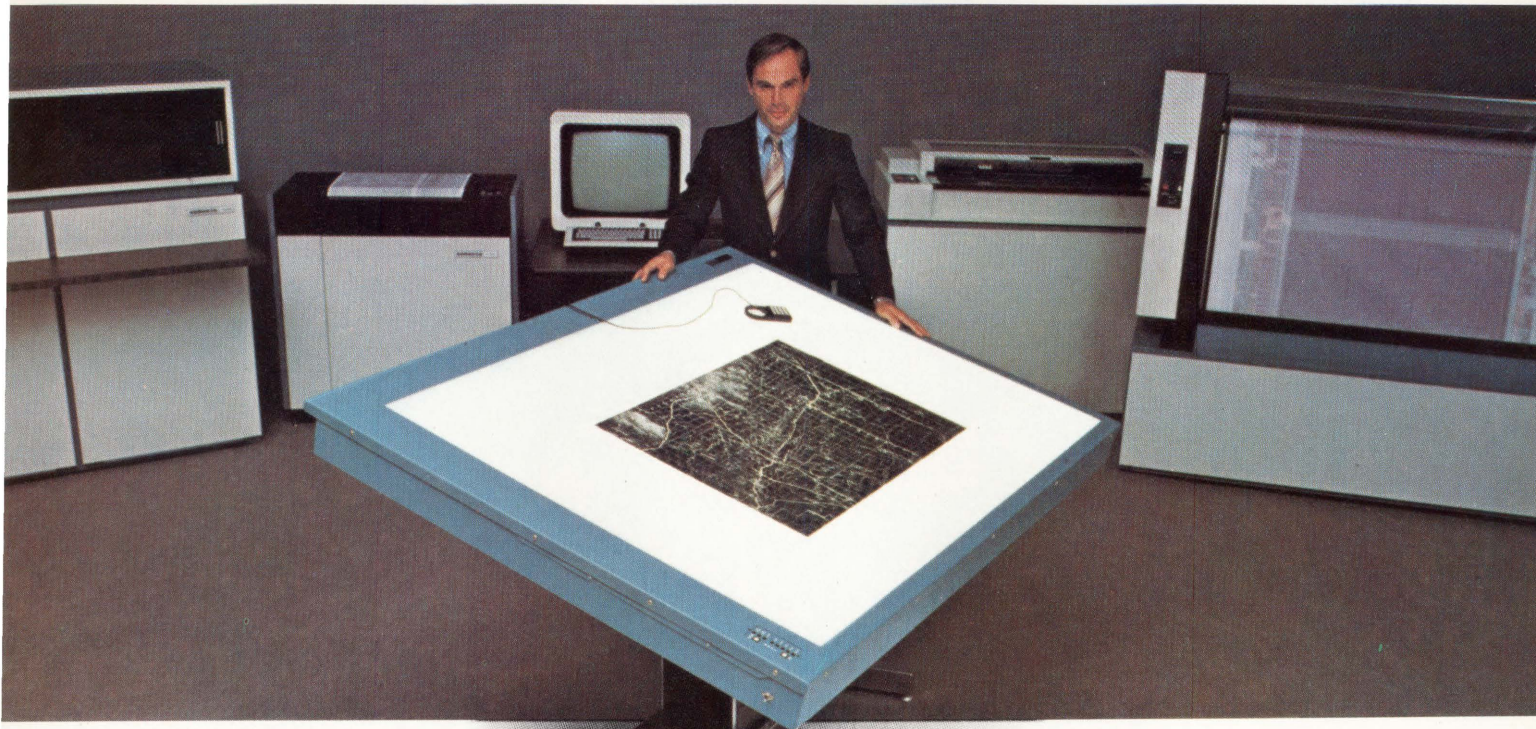
Options include selection of MARK and SPACE signals for each of the 16 circuits, with a timeout period adjustable from 1 ms to 6 min. This option allows specification of the setting of each of the alarm indicator points and of how the operator will be alerted when line conditions change. The device also allows for mixing of different data communications circuits that can be monitored from the same panel.

16-circuit complementary panel 5977R, also available as an option, allows for remoting one or a group of 16 alarm circuits from each 5977, and forwarding alarm conditions to other operator sites.

The alarm panel is furnished for rack mounting in standard 19″ (48 cm) cabinets. Interface is for RS-232 signaling (−3 to −25 V or 3 to 25 V).

Circle 327 on Inquiry Card

We've Always Offered More Graphics Solutions.



Now CalComp adds the full line of Talos digitizing tablets to what is already the most extensive line of computer graphics solutions available from any manufacturer.

Talos gives you a wide choice of digitizers in sizes from 11″ x 11″ to 44″ x 60″, with the option to back-light and rear-project images. And that's the kind of selection you need for your varied applications, including pipeline layouts, printed circuit boards and data reduction. Plus, they can accommodate conductive materials for digitizing seismographic and well-head logs.

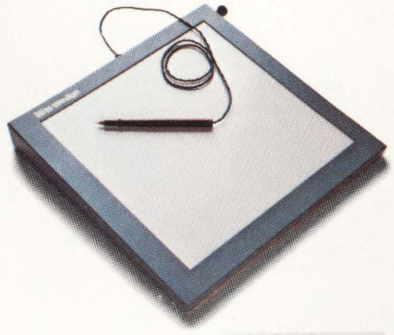
Our newest products, the 800 Series and the Wedge, both feature electromagnetic technology to allow you to digitize from conductive materials, and to give more precise data input and greater data stability.

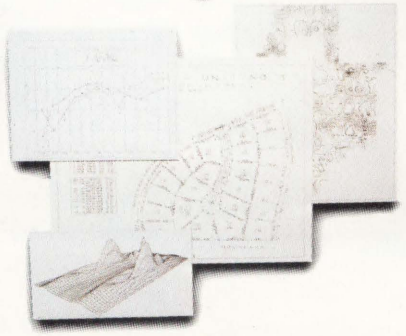
The flexible 800 Series with MULTIBUS® module lets you use dual tablets, dual cursors, and multiple interfacing for greatly expanded system capabilities.

The Wedge, designed especially for applications using small systems, offers end users and OEMs an affordable yet highly dependable alternative to traditional CRT control devices. And to aid operation ease and efficiency, the Wedge offers a unique five-degree sloped surface.

The 600 Series, using electrostatic technology and incorporating the "active inch" principle, is also available in a wide range of sizes and surface options.

With Talos Digitizers, We Offer Them All.





To further expand accuracy and high speed performance, we offer SMART software packages for the 600 and 800 Series. SMART provides local processing of digitized data to let you combine functions and calculations, and much more depending on your working requirements.

CalComp for all the alternatives in computer graphics.

CalComp offers full lines of drum, flatbed and beltbed plotters; controllers; computer output microfilm (COM) units, and electrostatic plotter/printers. And, new from CalComp, the Graphic 7 display system.

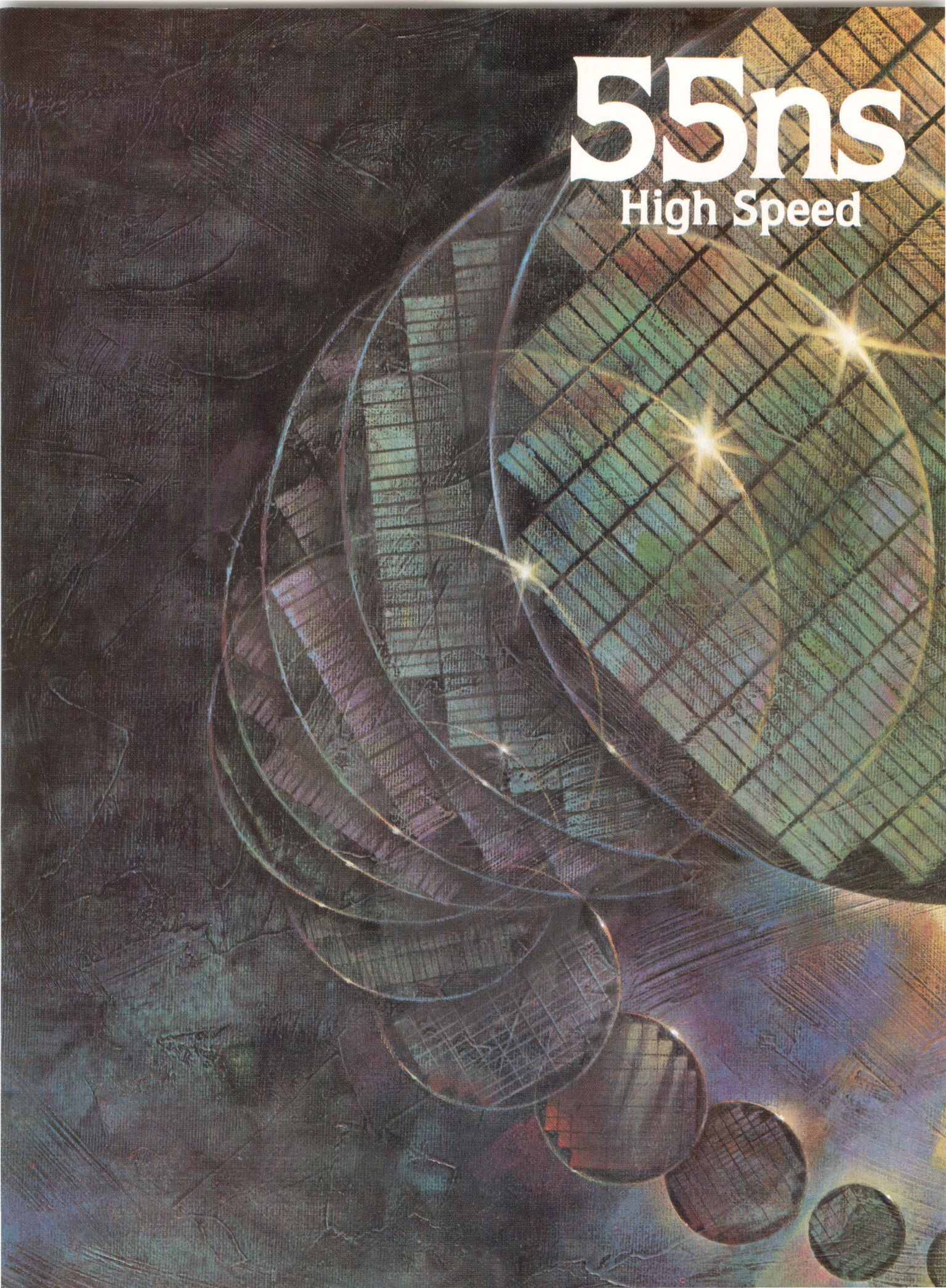
Plus CalComp support. All CalComp products — including Talos digitizers — are backed by the largest professional team of sales, systems and service people in the industry — direct from CalComp. And our worldwide service organization means we can give you fast assistance wherever you're located.

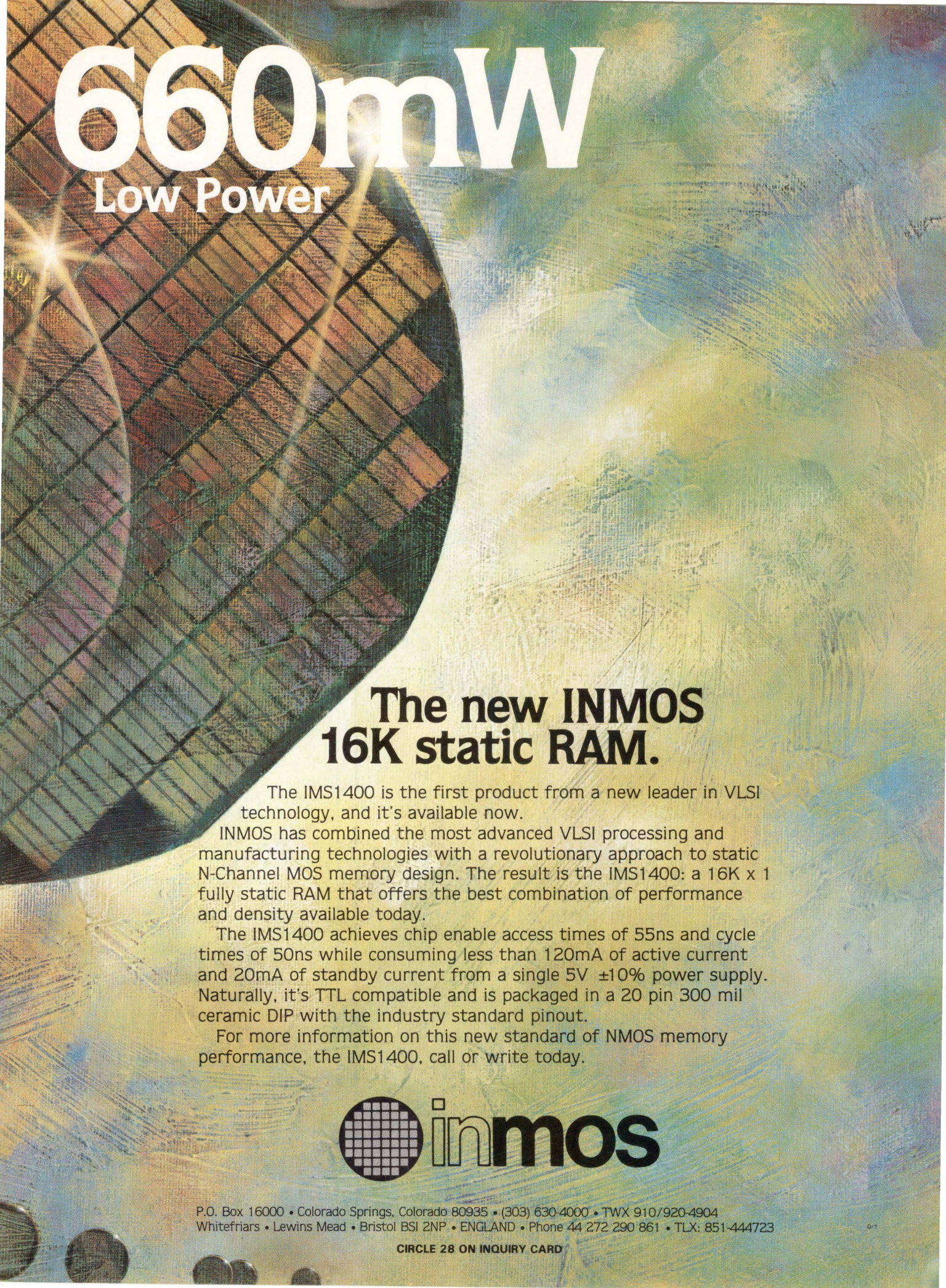
We have all the solutions to your graphics needs. Call today to see how we can find the right one for you.

CALCOMP
A Sanders Graphics Company
SANDERS

California Computer Products, Inc.
2411 West La Palma Avenue
Anaheim, California 92801
Telephone (714) 821-2011
TWX 910-591-1154

Graphics Sales Offices: Tempe, AZ: (602) 894-9468; Orange, CA: (714) 978-7111; Santa Clara, CA: (408) 727-0936; Englewood, CO: (303) 770-1950; Norcross, GA: (404) 448-4522; Schaumberg, IL: (312) 884-0300; Shawnee Mission, KS: (913) 362-0707; Metairie, LA: (504) 833-5155; Waltham, MA: (617) 890-0834; Southfield, MI: (313) 569-3123; Bloomington, MN: (612) 854-3448; St. Louis, MO: (314) 863-2711; Woodbridge, NJ: (201) 636-6500; Fairport, NY: (716) 223-3820; Cleveland, OH: (216) 362-7280; Dayton, OH: (513) 276-5247; Tulsa, OK: (918) 663-7392; Portland, OR: (503) 241-0974; Pittsburgh, PA: (412) 922-3430; Wayne, PA: (215) 688-3405; Dallas, TX: (214) 661-2326; Houston, TX: (713) 776-3276; McLean, VA: (703) 442-8404; Bellevue, WA: (206) 641-1925


55ns
High Speed



The new INMOS 16K static RAM.

The IMS1400 is the first product from a new leader in VLSI technology, and it's available now.

INMOS has combined the most advanced VLSI processing and manufacturing technologies with a revolutionary approach to static N-Channel MOS memory design. The result is the IMS1400: a 16K x 1 fully static RAM that offers the best combination of performance and density available today.

The IMS1400 achieves chip enable access times of 55ns and cycle times of 50ns while consuming less than 120mA of active current and 20mA of standby current from a single 5V ±10% power supply. Naturally, it's TTL compatible and is packaged in a 20 pin 300 mil ceramic DIP with the industry standard pinout.

For more information on this new standard of NMOS memory performance, the IMS1400, call or write today.

inmos

P.O. Box 16000 • Colorado Springs, Colorado 80935 • (303) 630-4000 • TWX 910/920-4904
Whitefriars • Lewins Mead • Bristol BSI 2NP • ENGLAND • Phone 44 272 290 861 • TLX: 851-444723

0/1

CIRCLE 28 ON INQUIRY CARD

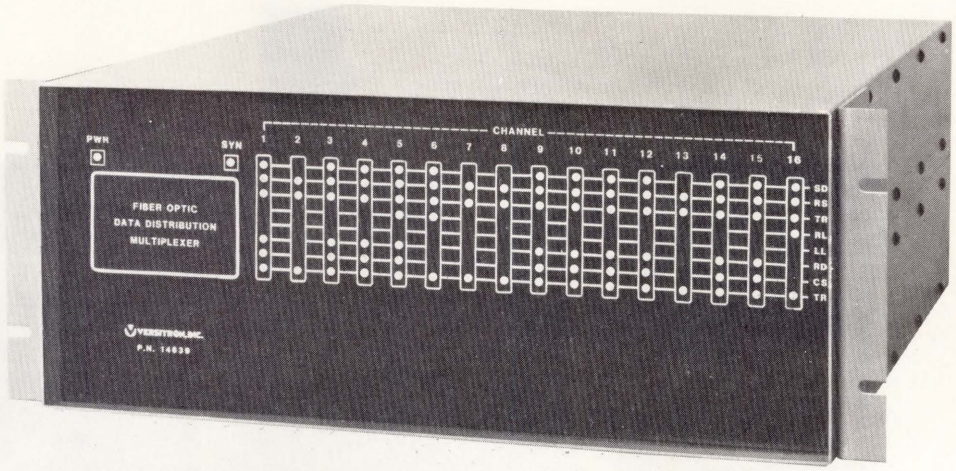
2400-Bit/s Modem Incorporates Data Concentrator and ARQ—A 4-channel concentrator and automatic retransmission on error are incorporated into the No-Frills™ concentrator modem from Micom Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311. Operating at 2400 bits/s, the modem is designed for use in a minicomputer network having three or four terminals located at a site remote from that of the computer. The device operates as a cluster controller with built-in modem for Digital Equipment, Hewlett-Packard, Data General, and other minicomputer configurations. It can be used on standard unconditioned leased telephone lines.
Circle 328 on Inquiry Card

Line Driver Provides Economical Short Haul Data Transmission—Operating in point to point and multipoint environment, synchronous line driver SLD1920 from Intertel, 6 Shattuck Rd, Andover, MA 01810, provides synchronous data transmission at speeds ranging from 2400 to 19.2k bits/s. It operates over local telephone loops or twisted pairs, error free, at distances up to 18 miles (29 km) at 2400 bits/s. The modem uses a coarse bit rate sampling technique to handle asynchronous devices to satisfy limited distance applications for both synchronous and asynchronous transmission. Multiple self-test functions include remote digital loopback for testing the total communication link.
Circle 329 on Inquiry Card

Starter Kit Offered for Basic Broadband Coaxial Network—To introduce potential users to the broadband coaxial cable transmission medium for local data networks, Amdax Corp, 160 Wilbur Place, Bohemia, NY 11716, is offering a starter kit that consists of two data exchange interface units (DAXs), two directional couplers (taps), a channel translator, and 100 ft (30 m) of broadband coaxial cable. DAX units transmit and receive digital signals and superimpose the data on an rf carrier. The couplers tap a portion of the power from the trunk cable onto a drop cable leading to a data source. The channel translator converts blocks of data transmitted at low frequencies to the higher frequencies required for reception. Kit includes a starter guide, glossary of terms, and an installation manual.
Circle 330 on Inquiry Card

Facsimile Machine Meets CCITT Group 1, 2, and 3 Specifications—Desktop digital facsimile transceiver 9136 can transmit a standard business document anywhere in the world in about 1 min, and can also communicate with other CCITT-approved analog machines operating in the 3- and 6-min mode. The device, from 3M, Business Communication Products Div, Dept BC80-22, St. Paul, MN 55133, has semiautomatic loading and connects to the dial-up network through a standard modular telephone jack. The transceiver measures 7.5 x 17.5 x 21.0″ (19.0 x 44.5 x 53.3 cm) and weighs 35 lb (15.75 kg). The system will be available sometime in 1981. □
Circle 331 on Inquiry Card

fiber optic system with multi-drop capability



handles 16 channels of local distribution data

Versitron's new fiber optic data distribution system provides all of the features of fiber optic transmission while maintaining a cost effective edge over a conventional hardwire unit. The system provides a direct full duplex link to the CPU port for 16 terminals from several different locations — all over a single fiber optic cable pair!

Multi-Drop Multiplexers The heart of the system is Versitron's new multi-drop multiplexer. This equipment consists of a central unit, located at the CPU, and several remote units located throughout the local distribution network. The central unit operates as a conventional time division multiplexer; providing an aggregate (16 channel) interface to the local distribution network over a fiber optic cable pair, and 16 EIA interface parallel data channels to the CPU. Each of the remote units is assigned a number of channels. Each unit continuously adds its assigned channels into the proper time slots on the transmit aggregate signal and withdraws the channel data from the receive aggregate signal. Once the parallel data is recovered it may be brought through an EIA connector directly to the terminal; or, for terminals located some distance away, through a separate parallel data fiber optic link.

Flexible Configuration The exact system configuration — the number of remote units and the number of channels/unit — is totally dependent on the individual site requirements. Additionally, the system configuration may be changed at any time simply by swapping circuit cards.

The system is designed to operate with any combination of synchronous or asynchronous terminals up to a maximum of 19.2 kbps for synchronous or 9600 baud for asynchronous. The built-in diagnostics include the ability of the central unit to command a remote channel loop-back without affecting traffic on the remaining channels and a complete front panel status display.

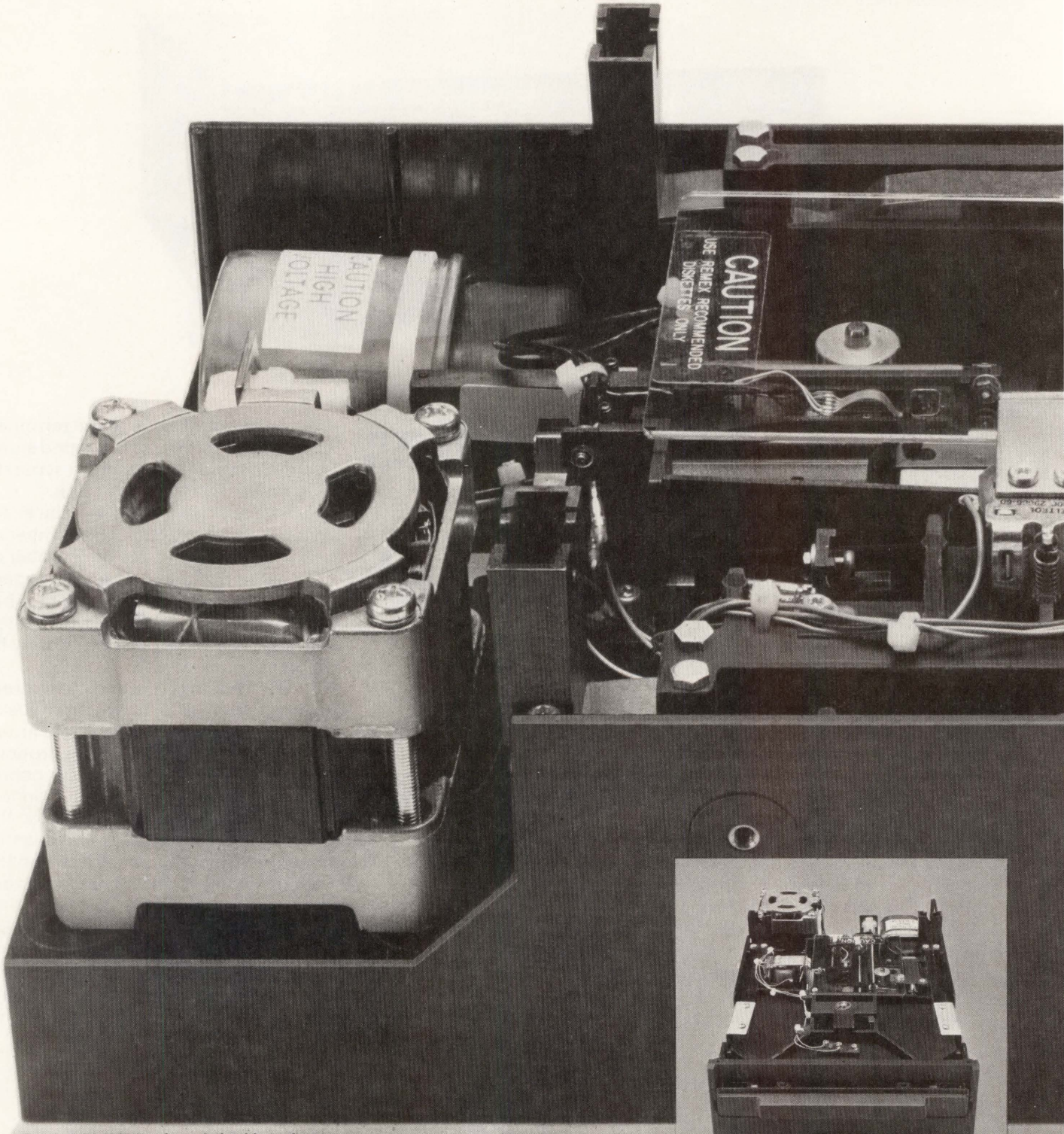
Versitron, Inc. installed its first fiber optic link utilizing a multiplexed data technique in the early 1960's. Since that time we have sold over 19,000 fiber optic links covering a wide variety of requirements for military and commercial applications.

VERSITRON

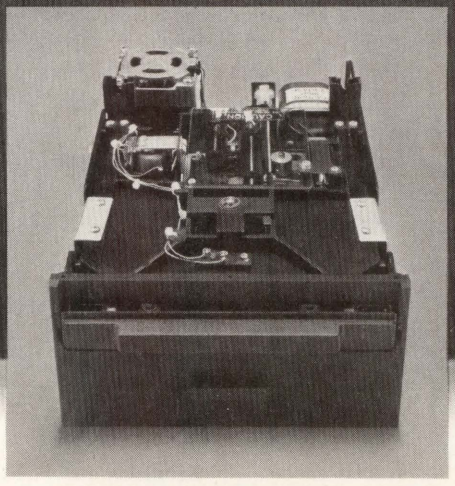
Versitron, Inc. 6310 Chillum Place N.W. Washington, D.C. 20011 (202) 882-8464

CIRCLE 30 ON INQUIRY CARD

Remex Dual Head
No Extravagant Claims.

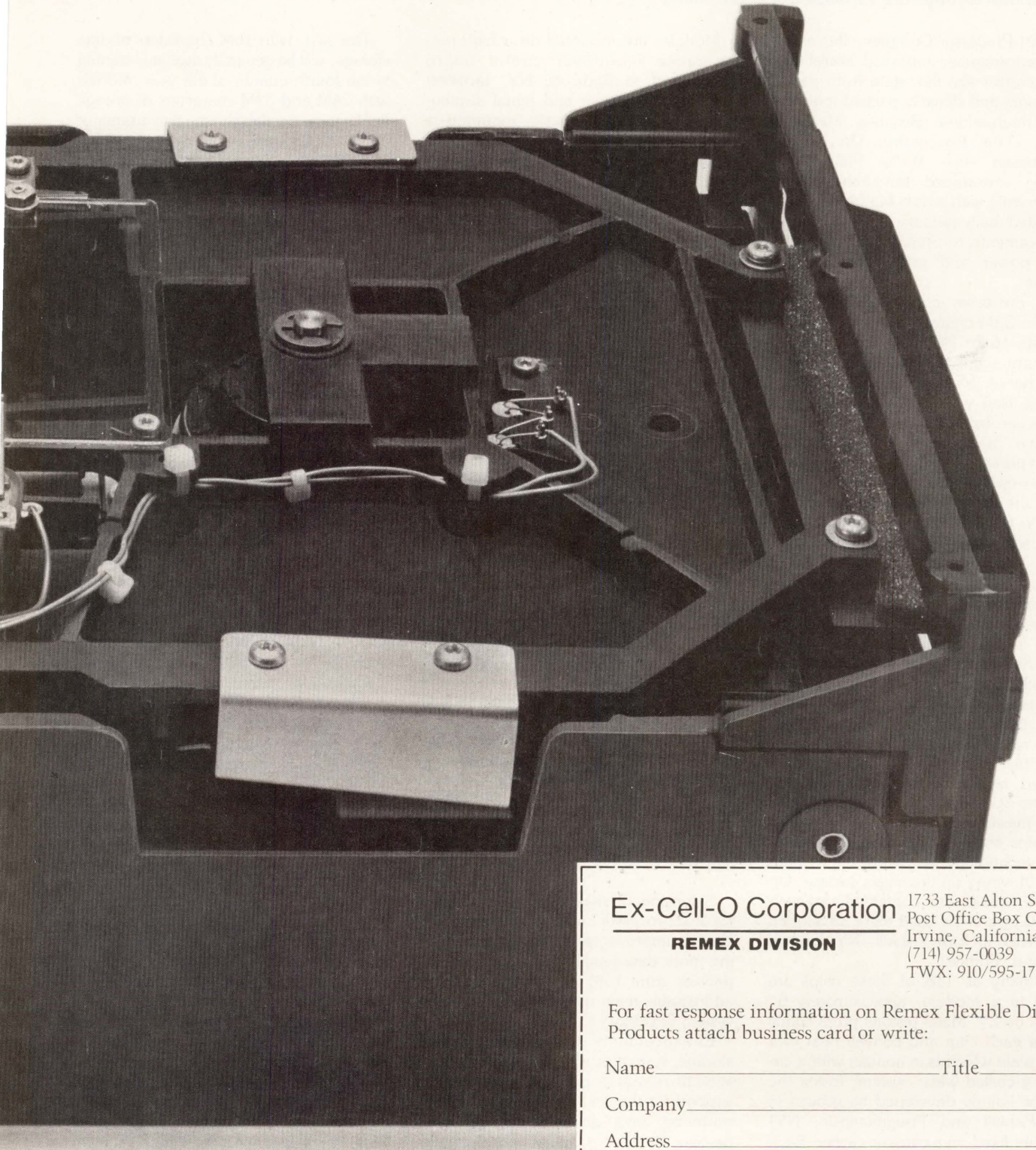


Remex RFD4000 Dual Head Flexible Disk Drive



Remex RFD2000 Single Head Flexible Disk Drive

Floppy Disk Drives.
Just Performance.



Write or Call for Specifications and Delivery.

Ex-Cell-O Corporation
REMEX DIVISION

1733 East Alton Street
Post Office Box C19533
Irvine, California 92713
(714) 957-0039
TWX: 910/595-1715

For fast response information on Remex Flexible Disk Products attach business card or write:

Name_____ Title_____

Company_____

Address_____

City_____ State_____ Zip_____

Phone_____

Dyadic Design and Dense Logic Contribute to Improve Processor Performance

The 3081 Processor Complex offers users high performance, improved availability, and compact size that stem from paired processors and densely packed logic circuits. International Business Machines Corp, Data Processing Div, 1133 Westchester Ave, White Plains, NY 10604, announced this achievement concurrently with a 3033 Model Group S, expanded main memory on the 3033, and enhancements to MVS/SP, all of which boost power and range of the large systems.

The processor complex offers 16M, 24M, or 32M characters of main storage and has 16 or 24 integrated channels. Maximum aggregate data transfer rate is 72M char/s. Most direct access storage devices used with other large IBM processors can be attached.

Within the processor complex, two distinct processors—in a dyadic or paired design—operate at a cycle time of 26 ns under the system's control program. In addition to providing high performance, the dyadic design improves availability, since either processor can assume the other's workload.

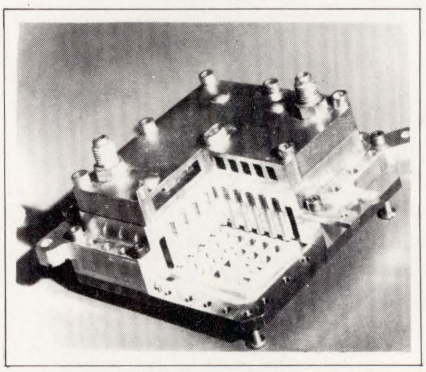
Computational functions are provided by more than 750k logic circuits contained in four compact packages, each measuring approximately 2′ square and 3″ thick. The system offers up to twice the internal performance of the 3033 and significantly reduces space, cooling, and power requirements.

The processor complex uses highly integrated bipolar logic technology that operates at speeds of 1 to 2 ns. Produced by the master slice, or gate array method, the chips are customized using electron beam technology to connect the three levels of wiring on the chip's surface. Up to 704 circuits are contained on each chip. (Logic chips used were developed at facilities in East Fishkill, NY, and in Essonnes, France.)

As many as 118 of these chips are sealed in a module, approximately 5″ square by 2″. Metal pistons press lightly against each chip and convey heat to a metal plate which is in contact with a circulating chilled water system. Inside the module (jointly developed by groups in East Fishkill and Poughkeepsie, NY) chips are fixed on a ceramic carrier. Each carrier has up to 33 layers and about 400′ of internal wiring for signal interconnection and power distribution.

Modules are mounted on a high performance multilayer circuit board (developed in Endicott, NY, facilities) that provides power and signal distribution functions previously requiring a number of separate cards, boards, and cables. For rapid servicing, modules can easily be removed from the board and replaced.

The concurrently announced 3033 processor, model group S doubles the internal performance of the 3031 processor and can be upgraded at customer's locations to 3033 models, allowing users to triple system capacity. The processor is available with six channels and 4M or 8M characters of main storage. Machine cycle time is 57 ns.



Circuit module used in IBM's 3081 processor complex contains as many as 118 logic chips providing total of 45,000 circuits. Within module, spring-loaded pistons in contact with each chip convey heat through metal plate to circulating chilled water system. Modules plug into multilayer circuit boards which permit more than 750k logic circuits to be housed in 4 ft³

Extension of maximum main storage for 3033 processor and attached processor models improves performance by keeping more data readily available. This expansion from 16M to 24M characters of addressable main memory also increases system flexibility.

Enhancements to multiple virtual storage/system product release 1 and an MVS/SP release 3 provide programming support for the 3081 and the recently announced 3375 direct access storage device. Release 3, which includes all functions available in release 2, offers improved system performance, reliability, and availability.

The 3081, with 16M characters of data storage, will be generally available starting in the fourth quarter of this year. Models with 24M and 32M characters of storage will become available in the first quarter of 1982. A 3081 processor complex, which includes processor, processor controller, power unit, coolant distribution unit, and systems and operators' consoles, with 16 channels and 16M char of main storage, has a price of $4,046,240. A 24-channel 32M-char complex has a price of $4,596,240.

Circle 350 on Inquiry Card

2.5G- and 571M-Byte Disc Drives Added to IBM Compatible Line

Large capacity direct access storage devices and a data streaming feature for solid state disc have been announced by Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027. The 8380 stores more than 2.5G bytes of data, is fully compatible with IBM's 3380, and attaches to the equivalent of any IBM 370/158, 370/168, or 303X processor. The 8370, a 571.3 M-byte drive, is fully compatible with the 3370 and requires no software migration for current users.

The 2-spindle 8380 has two independent actuators per spindle (each with its own support electronics) and provides capacity per actuator of approximately 630G bytes. A media interchange switch allows each spindle to be accessed via either set of support electronics. Data transfer rate is 3.0M bytes/s, and average seek time is 16 ms. The unit is available with optional dual-port and fixed heads.

The 8370 is a single-spindle device with two independent actuators with separate electronics. Media interchange switch allows actuators to be switched between either set of electronics. Formatted with a fixed block architecture, the unit has a data rate of 1.86M bytes/s. Average seek time is 20 ms. Units are available with optional dual ports and string switching.

The addition of data streaming channel support for the 4305 solid state direct access storage device allows its use in either data streaming or 2-byte wide transfer mode. This allows a 3M-byte/s transfer rate to be attained.

Circle 351 on Inquiry Card

EXTRA. EXTRA.

Now you get more extras when you pick the new dot matrix printers by C. Itoh. Choose the Comet 80-column printer and get the extra benefits of four character sizes and paper-saving print compression. Choose the Comet II 136-column printer and receive the added extra of a full-width computer size printer that accommodates paper widths to 381 mm (15").

Both the Comet and Comet II also offer the rare combination of low cost and high performance. Both models operate at an efficient 125 cps bidirectional print speed and in a 9 x 7 dot matrix.

C. Itoh's Comet series has the extra advantage of a unique multilingual capability with a selection of four different alphabets: English, German, Japanese and Swedish. Other special characteristics include a programmable VFU (Vertical Format Unit) plus self-test diagnostics. For your operator's convenience, there's easy bottom or back paper loading, and both Comets use a standard low-cost nylon ribbon. Plus our printers already meet 1981 Class A FCC, UL, and fire safety requirements.

If all that wasn't enough, Comet and Comet II are plug-compatible with all major printers in the industry, meeting standard parallel serial interface specifications. Our printers are backed by C. Itoh's warranty and a nationwide field service organization.

And as a final, all important extra, when you choose either printer from C. Itoh you get immediate off-the-shelf delivery.

So if you want the highest quality at the best price, look into the extras the C. Itoh Comet and Comet II printers offer. You'll get a lot more than you bargained for. For more information, contact C. Itoh Electronics, Inc., 5301 Beethoven Street, Los Angeles, CA 90066; Tel. (213) 390-7778. Chicago Office: 240 E. Lake Street, Suite 301-A, Addison, IL 60101; Tel. (312) 941-1310. New York Office: 666 Third Ave., New York, NY 10017; Tel. (212) 682-0420. Dallas Office: 17060 Dallas Pkwy., No. 108, TX 75248; Tel. (214) 596-2974.

C. ITOH ELECTRONICS, INC.

One World of Quality

CIRCLE 32 ON INQUIRY CARD

NAKED MINI® 4
EVERYTHING YOU'LL

The NM 4/10
A half-card 16-bit mini with half-cost economy. Four on-board distributed I/O channels, hardware multiply/divide and DMA are standard. Cost? Even less than many micro-computers.

The NM 4/30
A midrange beauty. Twice as fast as the 4/10 and with a larger instruction set. Double register shifts, multiple-word memory reference instructions, and more.

The NM 4/90
Twice as fast as the 4/30 and with a beefed up instruction set. With a hefty 128K byte's worth of direct addressing, it's an ideal choice for high-performance applications like industrial control and data communications systems.

The NM 4/95
Top of the line. Memory management unit for expansion to 8 megabytes. ECC RAM memory for reliability. High speed cache memory for faster throughput. And Page Protection to prevent destruction of another user's space.

The NM 4/04
SCOUT™ the little fella that's had OEM's buzzing for months. Through the wizardry of ISOLITE,™ SCOUT can test himself every time he's turned on. And a 16-bit CPU, I/O, 32K byte RAM, and card cage costs less than $1,000.

ComputerAutomation has just what you need to cut a path through to your computer solutions.

You need compatibility? We've got it, with software compatibility from SCOUT through our 4/90. And I/O compatibility across the family, from the 4/10 through the 4/95. All with up to 128K Bytes of directly addressable memory. And up to 8 megabytes of physical memory for the 4/95.

You want software and development tools? We've got all the operating software to get you up and running.

You demand reliability? We've got a track record of success in applications as diverse as automated bank tellers, aircraft control simulators, blood analyzers, laser welders and missile tracking systems.

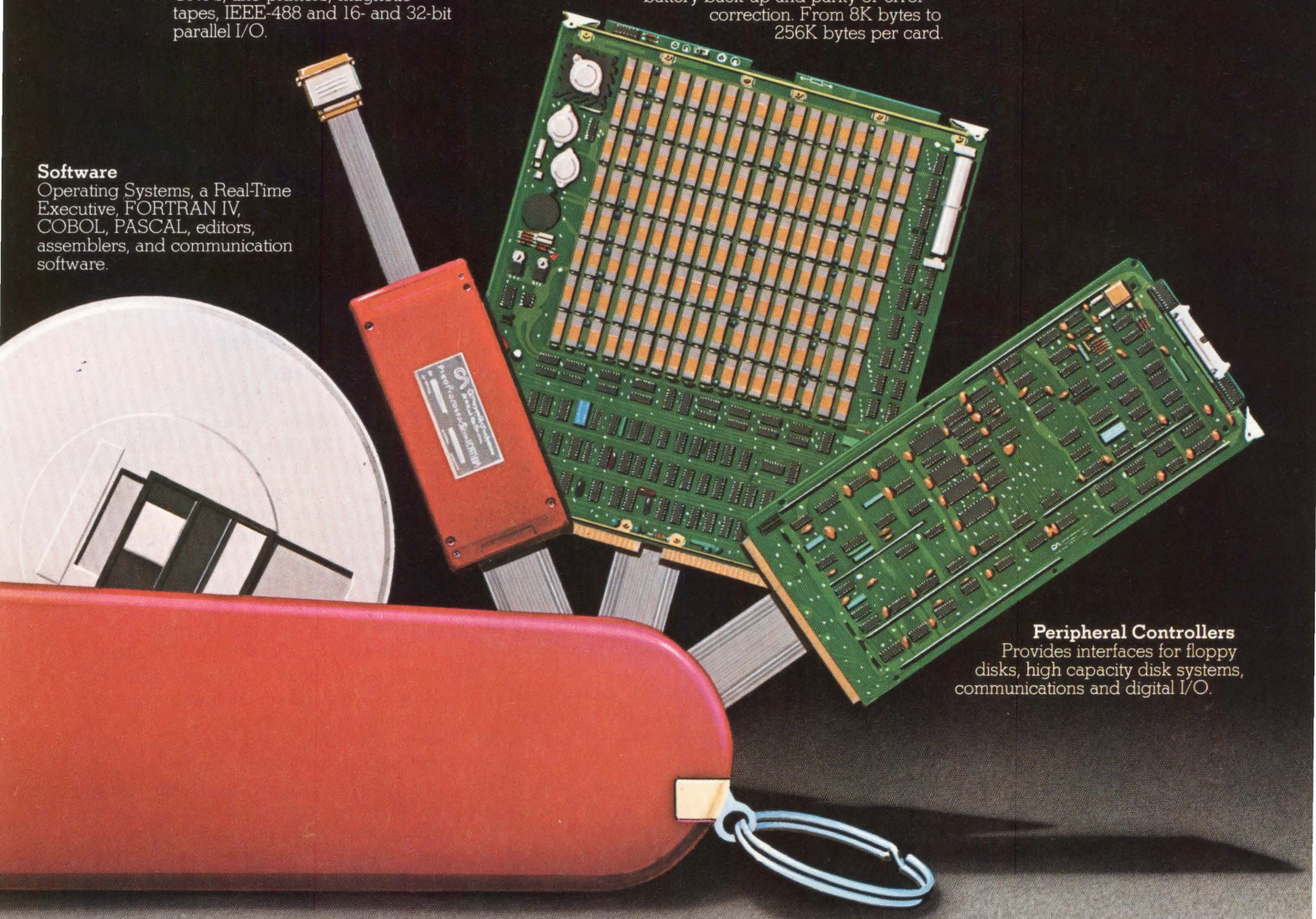
Best of all, it's all part of CA's OEM philosophy that says to protect our profitability, we've got to protect yours. Which means com-

COMPUTERS. NEED IN THE OEM JUNGLE.

Interfaces
Our famous Intelligent Cables offer low-cost interfaces for async and bisync communications, CRT's, line printers, magnetic tapes, IEEE-488 and 16- and 32-bit parallel I/O.

Memories
The family never runs short of memories. Core, RAM, and E/PROM. Plus battery back-up and parity or error correction. From 8K bytes to 256K bytes per card.

Software
Operating Systems, a Real-Time Executive, FORTRAN IV, COBOL, PASCAL, editors, assemblers, and communication software.



Peripheral Controllers
Provides interfaces for floppy disks, high capacity disk systems, communications and digital I/O.

petitive prices, a hassle-free software policy, timely deliveries and the best warranty in the business.

We've got everything you'll need to battle your way out of the OEM jungle.

And the path out begins on the right.

ComputerAutomation
NAKED MINI® Division
Where OEM's come first.
18651 Von Karman, Irvine, California 92664

Send help fast. CD 1-81

☐ Please send the latest full-color brochure on the entire NAKED MINI family.

☐ Please send a sales representative.

☐ Please call me at (____) _____

If you're really in a hurry to fight your way out, give us a call at (714) 833-8830 X455.

Name_____

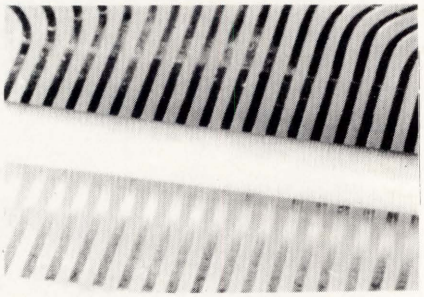
Company_____ Title_____

Address_____ City_____

State_____ Zip_____ Phone_____

CIRCLE 33 ON INQUIRY CARD

Elastomeric Connector Joins Circuit Planes Using Pressure Alone



Cambiflex, metal to metal elastomeric connector system developed by Cambion, consists of cylindrical core wrapped with thin flexible circuit which carries parallel conductors that interconnect corresponding patterns pressed against it

CAMBIFLEX is a reliable metal to metal elastomeric connector system employing microminiature connections that join two parallel or perpendicular planes of circuitry by pressure alone. Developed by Cambion, 445 Concord Ave, Cambridge, MA 02238, the connections require no soldering, bonding, or use of large space-consuming bodies and associated hardware, and can be used to maximum advantage for flat flexible cable, discrete components, thumbwheel switches, and subassembly modules.

The connection consists of a nonconducting elastomeric core with parallel lines of gold-plated copper conductors on a thin flexible film. When compressed between two parallel planes, the metallized lines around the circumference interconnect the circuitry on each plane with guaranteed contact redundancy. The main function of the elastomeric core is to provide the force for a reliable connection; a secondary function is to serve as a resilient backing to increase the contact area (when under compression) and accommodate surface irregularities.

With a vertical or horizontal housing molded in 30% glass filled Noryl, the fixed connector assembly provides a latching facility when used with the cable connector. The cable connector assembly is self-latching into the vertical or horizontal housing of the fixed connector assembly. Flat flexible polyester insulated cable is available 1″ (2.54 cm) wide with 9 or 17 conductors. Cable assemblies are available in standard overall lengths of 5.9, 11.8, 17.7, or 23.6″ (14.9, 29.9, 44.9, or 59.9 cm). Adapter boards are rigid glass epoxy, 0.063″ (1.600 mm) thick, and are patterned, drilled, and plated to accept DIL ICs up to 16 pins on a 0.300″ (7.62-mm) pitch. Working voltage is 150 dc or ac, with 1-A recommended maximum working current. Contact resistance is 20 mΩ typical, and insulation resistance is 10^5 MΩ min at 85 V.

Circle 352 on Inquiry Card

Multi-User Computer System Balances Power Using Independent Processors

ECHO system 8020 can be expanded up to 256 independent users without significant impact on system throughput. To accomplish this, Echo Communications Corp, 1708 Stierlin Rd, Mountain View, CA 94043, distributed independent microprocessor modules throughout the system to maintain an even balance of computing power.

The basic system uses three microprocessor modules. One processor module handles the mass storage functions, while pairs of processor modules perform the terminal and general computing functions for up to four users. Other features are four independent user terminals, 20M bytes of disc storage, a standard 8″ (20-cm) floppy disc drive for software interchange, and a cartridge tape backup device. User terminals feature a detached keyboard and 15″ (38-cm) video display providing over 3000 software definable characters and graphics.

System components and operating system software enable the computer to continue to operate when one or more of the system components fail. In multiple processor systems, each processor automatically assumes a portion of the work load. Multiple processors and DMA controllers operate at up to 6 MHz and transfer data in 8-, 16-, and 32-bit groups. A system supports multiple RS-232 standard data communication lines. The system bus also enables interbus asynchronous communication data rates of 1M bytes between system buses. The Echo Net provides intersystem communication via single conductor cable to remote locations.

The system is easily configurable and may be expanded by combining multiple 6-MHz Z80 processors and 16-bit 86000 processors in a single system to share the work load. A single processor can address up to 16.7M bytes of RAM in one enclosure. The Echo Bus interface controller enables each system card cage to communicate with additional cages. More than one bus interface controller can be used with an additional Echo bus to increase system reliability. Data can be transmitted through the computer at over 1M bytes/s.

The ECOS operating system allows modular expansion and fault tolerance simply by adding another processor to a system bus or multiple processors in multiple buses. Disc and tape devices can be incorporated anywhere in the system to ensure fault tolerant performance. An added benefit of the system modularity is that a failure in any user processor module will affect a maximum of four users without bringing down the entire system. Future options allow addition of redundant database modules to provide even more failure resistant operation.

Circle 353 on Inquiry Card

VLSI Tester Capable Of Handling 120 Pins At 20-MHz Rates

Offering capability for testing devices having up to 120 pins at full 20-MHz test rates, model 120 of the Sentry series 20 family is a high speed general purpose VLSI test system. In the unit, Fairchild Camera and Instrument Corp, Test System Group, 1725 Technology Dr, San Jose, CA 95110, provides comprehensive testing for a broad range of engineering and production applications.

The system is based on a multiprocessor architecture, and uses 10k and 100k ECL throughout all formatters, timing paths, and pipeline and local memory sections to enhance system speed. MOS and bipolar memories, microprocessors, and peripheral chips that run as fast as 20 MHz, and static RAMs, bit slice microprocessors, and microprogrammable controllers that run faster than 20 MHz can be fully characterized by multiplexing pins.

A 24-bit wide data bus in the system's FST-2 CPU allows communication at DMA speeds for maximum throughput. Because of its I/O speed, the computer is available for program development or data reduction most of the time. Memory capacity is 196k 24-bit words, and a fast fixed head disc is included for further program storage capacity expansion.

The 20-MHz sequence processor can generate millions of 0/1 and format control test vectors for functional testing of microprocessors and peripheral control

(continued on page 56)

HOW TO COPY THE MICROPOLIS 8" RIGID DISK DRIVE.

It's bound to happen sooner or later. Someone will decide to copy our 8" rigid disk drive. It happens to all industry-standard products.

So we're going to save someone the trouble and tell exactly how we built our 8" drive. But we're not worried. Because, frankly, we don't think anyone else will want to go to the trouble we did to give you such a product.

First of all, our family of 8" rigid disk drives (9 to 45 megabytes) comes with features you simply can't find in the competition's products. Such as our low-cost intelligent controller board, designed to allow swift integration into your existing system.

In addition to low power dissipation and fastest access time, we also included a Quartz-locked, direct-drive, brushless DC motor. We gave our rigid disk a braking mechanism, too. It extends the life of the disk by not allowing the head to act as the brake. That's a longer disk life for you, and a higher MTBF in the critical clean area. Next, we included our balanced rotary voice coil positioner, which, together with the closed-loop servo, absolutely protects against unexpected jolts, bumps, and shocks during write operations which might otherwise result in off-track writing.

We enclosed the heads, platters, and positioner assembly in a sealed clean area. No other drive has all active components outside the clean area, for easy access and maintenance. So we can offer the longest drive warranty in the business.

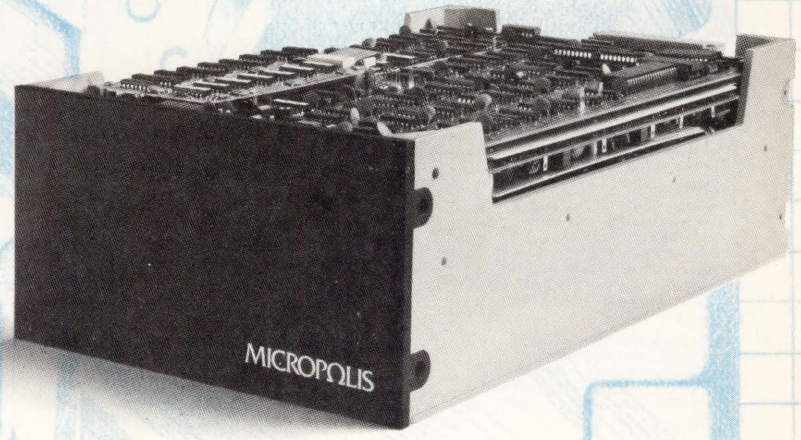
All this adds up to unprecedented quality, reliability, and stability. And our 8" rigid disk fits into the exact same space as an 8" floppy drive—they even use the same screw holes.

So if you want the best 8" rigid disk drive, call us. We deliver.

If you want to try and copy it, good luck. You'll need it.

MICROPOLIS™

21329 Nordhoff Street
Chatsworth, California 91311
(213) 709-3300. Telex 651486



CIRCLE 34 ON INQUIRY CARD

devices. Its 16 I/O registers, 16 mask registers, and 16 functional invert registers provide flexibility for exhaustive testing of future complex logic devices. 4k words of local memory allow storage of the necessary patterns without data breaks. The pattern processor also runs at 20 MHz, allowing testing of high speed memories up to 65k x 18 bits.

An enhanced timing system offers 156-ps resolution for accurate placement of edges when measuring ac parameters of high speed devices. Its 16 timing generators can program up to 32 independent edges. Each edge can be changed during test execution to any of 16 different values to provide added flexibility in measuring ac parameters.

Operating system software permits testing in foreground along with programming in the background. The FACTOR testing language can be used to write device programs, and a large library of utility programs speeds device debugging.

Circle 355 on Inquiry Card

Attached Virtual Processor Meets Growth Requirements Of VS/9 Applications

The 1100/60 attached virtual processor, a special purpose CPU that operates in the multiprocessor environment of an 1100/60, integrates VS/9 capabilities into the series 1100 line. Announced by Sperry Univac, PO Box 500, Blue Bell, PA 19424, the system is designed to execute 90/60, /70, and /80 systems without modification. An 1100/60 user program, attached processor control software (APCS), provides the I/O interface for the VS/9 operating environment with the series 1100 operating system.

Hardware on the VS/9 side consists of a central processor with a logic bus structure and microcode control similar to that of the 90/80 family. Main storage capacity of an 1100/60 attached virtual processor (AVP) ranges from 524k to 1048k words. A 32k-byte buffer storage (cache) provides for buffering of instructions and data between the 1100 main storage unit (MSU) and the AVP CPU. Buffer storage improves CPU performance and reduces the number of accesses to the MSU.

Most I/O operations are performed through I/O devices attached to the 1100/60 channels. The attached processor control software (APCS) establishes the environment for the VS/9 to operate as though it were running with its standard peripheral complement. APCS supports the 1100/60 AVP access to VS/9 random access data volumes via direct, logical, or local attachment.

Direct attachment allows disc subsystems of the 90V systems to attach directly to the 1100/60 block multiplexer channel. Data written to these volumes by the 90V will be accessed directly by VS/9 running on the 1100/60 AVP without modification of the data format. Thus, these volumes can continue to be used by a 90V for data transportability, volume, group sharing, and system backup.

With the logical arrangement, discs such as the 8470 are formatted and accessed using standard 1100 series software. This facility allows VS/9 users to benefit from current technology devices that are not included in standard configurations.

In local attachment mode, the 90V disc subsystem is attached to the AVP through an optional block multiplexer channel. This mode provides support of devices being used in the VS/9 environment for which comparable support is not available through OS 1100.

Circle 354 on Inquiry Card

IT™ is the difference between too smart and too dumb.

Just when you thought you were totally confused by all the "smart" computer terminals on the market, Lear Siegler eliminates the confusion by bringing you exactly what you need.

IT™—the Intermediate Terminal™ video display from Lear Siegler.

IT compresses the broad spectrum of "smart" terminals into ITself. Now, when you're looking for a terminal that isn't too smart but isn't too dumb either, IT is perfect for the job.

And IT is completely self-contained, with full editing, formatting and protected field capabilities.

With IT you get two pages of memory (a total of 48 display lines). A complete range of visual attributes. Blinking. Blanking. Reverse video. Reduced intensity with protected fields. And underlining.

Plus, you also get upper/lower case. A high resolution monitor. Built-in numeric keypad. Function keys. Full or half duplex. Conversation or block mode transmission. Modifiable personality. And optional business graphics.

And, best of all, you get the same high standards and solid workmanship that made the Lear Siegler Dumb Terminal® video display a legend in its own time.

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

IT, the Intermediate Terminal from Lear Siegler.

Lear Siegler, Inc./Data Products Division, 714 North Brookhurst Street, Anaheim, CA 92803 800/854-3805. In California 714/774-1010.
TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices: • San Francisco 408/263-0506 • Los Angeles 213/454-9941 • Chicago 312/279-5250 • Houston 713/780-2585 • Philadelphia 215/245-1520 • New York 212/594-6762 • Boston 617/423-1510 • Washington, D.C. 301/459-1826 • England (04867) 80666.

Intelligent Typewriter Derives Performance From Motor Control Aspects

The Qyx intelligent typewriter uses a daisywheel printing system with powerful software to provide capabilities ranging from automation of simple typing functions to sophisticated word processing. To meet the needs of these applications, the carriage and printwheel are driven by linear and rotary motors developed specifically for them, along with necessary drive and control strategies.

The basic system, developed by Qyx Div of Exxon Information Systems, Lionville, PA 19353, consists of system control module, printer, and keyboard. It provides a 1-line buffer memory, automatic erase backspace, automatic selection of 10-, 12-, or proportional-pitch styles, automatic centering, and a phrase dictionary. In higher level machines, memory capacity is increased to 10k characters for level II, with up to two removable mini-diskettes of 60k characters each for level V. Higher level machines also have extensive text editing and word processsing capability and can be equipped with a 24-char LED display as well as a communication module.

The system is controlled by a Z80 based microcomputer with various amounts of static and dynamic solid state memory. All typewriter operating functions as well as editing and other applications functions are performed there. The daisywheel printer serves as the output medium and consists of these major motion components: a linear step motor for carriage motion, rotary step motor for daisywheel motion, rotary step motor for platen motion, hammer for print execution, and solenoids for print ribbon and erase ribbon lift.

Carriage motion for the printer is derived from a 4-phase variable reluctance, linear step motor. With a basic step size of 0.0167″ (0.424 mm), the motor is configured to minimize the mass of the slider and to avoid the umbilical cord problems of transporting large amounts of power. Front and rear stators are designed to drop negligible magnetomotive force in the back iron. The magnetic structure produces a larger than normal increase in torque with 2-phase-on compared to 1-phase-on. This force differential allows continuous current control of each phase pair and ensures that equal currents flow in each of the two energized phases when the motor is run in 2-phase on energization scheme.

Overall motion is controlled through an F8 microprocessor. Motion commands are received from the operating system and appropriate phase energizations are used to initiate motion. Gross control of motion during acceleration and deceleration is provided by sequential switching of phases based on position information from the sensors and desired switching angle. An analog position and velocity loop is invoked during the last step to achieve rapid final settling and to maintain the final position accurately.

Printwheel motion is provided by a 4-phase variable reluctance step motor which uses split stators and an axial air gap construction. The printwheel has teeth embedded in it and acts as the rotor of the motor as well as the load. Motor construction minimizes inertia of the system and provides for ease of insertion and removal of the printwheel. There are 98 characters per revolution on the wheel; thus 2 motor steps correspond to 1 character motion.

With 49 rotor teeth, the motor provides 196 steps/revolution. Two quadrature sensors provide positional information during closed loop motion control and provide position and velocity information during final damping. Daisywheel petals are used with optional transducers to provide feedback signals. As in the case of carriage motion, a microprocessor controls overall printwheel motion. During long multiple-character moves, the maximum speed achieved is 1700 characters/s, which is 3400 steps/s or 1040 r/min.

Circle 356 on Inquiry Card

Test System Offers 25/50-MHz Clock Rates For Static and Dynamic RAMs

System 7800 offers 25/50-MHz testing of static and dynamic memories for incoming inspection and engineering applications. Offered by Accutest Corp, 25 Industrial Ave, Chelmsford, MA 01824, the unit can have a number of configurations and can include up to two fully loaded test heads.

The system tests virtually all static and dynamic RAMs and ROMs and all TTL/ECL and MOS technologies. With a full complement of 27 input pins and 10 output pins, it can handle RAMs up to 64k x 8 and P/ROMs to 64k x 10. It offers high functional test speeds, high throughput, and comprehensive data reduction and engineering capabilities, as well as significant operating and maintenance economies.

25-MHz clock rates are standard for all test patterns. Testing rates up to 50 MHz are achievable through the use of a split cycle technique. Overall system accuracy is better than 0.5 ns. The unit provides 1-ns I/O switching, 16 timing sets, 32 timing mask sets, programmable active loads, and pin selectable timing, formats, and levels.

Controller is a DEC LSI-11/23 computer with up to 128k words of memory. Software is based on DEC's RSX-11/M multitasking operating system. Test plans are implemented in Pascal based software to reduce programming time and offer improved program documentation. Up to 16 systems can be networked to a host computer, integrating a semiconductor production line into a central process control and management information system.

Circle 357 on Inquiry Card

Dual-Density Tape Controllers Offer Packaging Flexibility

TO4/T34 dual-density tape controllers operate with Digital Equipment Corp's LSI-11 and PDP-11 minicomputers and are TM11/TU10 compatible. In developing the controllers, Dataram Corp, Princeton-Hightstown Rd, Cranbury, NJ 08512, used a packaging approach that provides the user with maximum packaging flexibility.

For NRZI mode (either processor) one quad board is required; for phase encoded (PE) mode, a dual-size PE board is added. The PE board draws 5 V and ground from the back panel of the minicomputer but does not use any of the bus signals on the back panel. This allows the PE board to be inserted in any available slot.

LSI-11 compatible TO4 and the PDP-11 compatible T34 controllers operate with industry standard tape drives and support any combination of 7-track, 9-track, NRZI, or dual-density drives. Up to four drives can be daisy chained to one controller and 64 bytes of data buffering are provided. 7-track drives can operate with the controllers in NRZI mode at 200, 556, or 800 bits/in; 9-track drives in NRZI mode at 800 bits/in or in PE mode at 1600 bits/in. The designs incorporate an integral 16-bit bipolar microprocessor and support tape drive speeds up to 125 in/s.

Bus address and interrupt vector address assignments are switch selectable. The 5-V current requirements are 5 A for NRZI controllers; the PE option requires an additional 2.1 A for either model. Automatic self-test with LED fault indication is standard on both.

Circle 358 on Inquiry Card

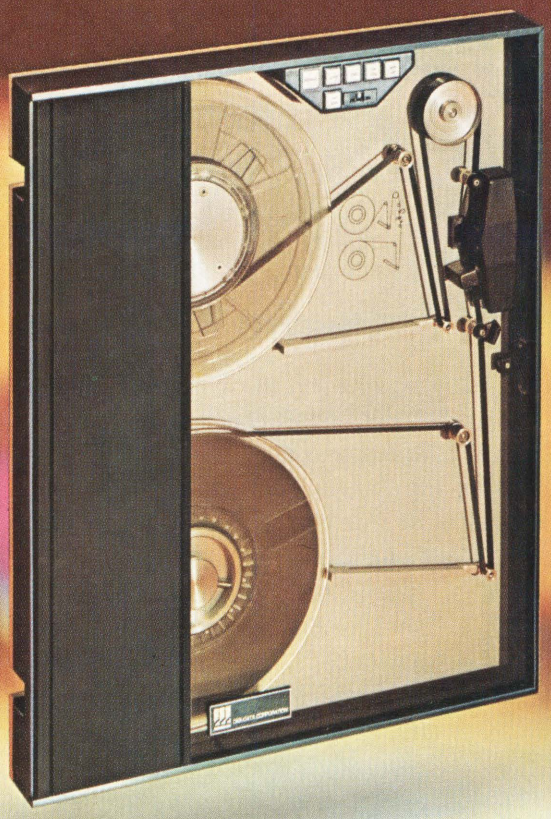
Digi-Data's Best Customers Have Switched From the Competition...

Here's Why:

- they can depend on Digi-Data's product performance and reliability . . . assured by clean, simple design and proven in over 10,000 installations.
- they choose from 192 recorder models to get the speed, format and reel size to meet their every need.
- they receive guaranteed industry compatibility at the transport, formatter and computer levels.
- and, they always pay less.

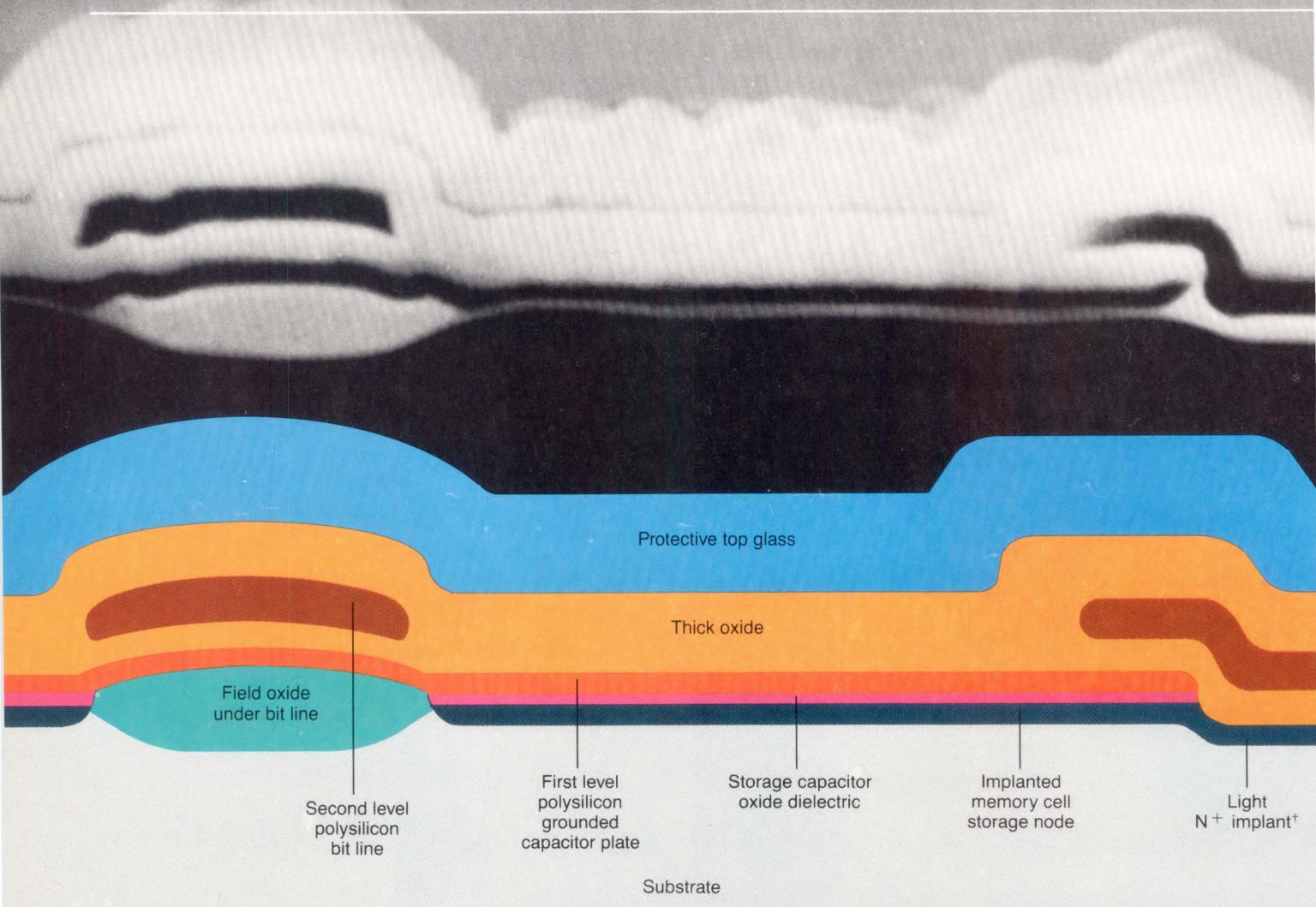
DIGI-DATA CORPORATION
8580 Dorsey Run Road
Jessup, MD 20794
(301) 498-0200

®... **First In Value**



CIRCLE 37 ON INQUIRY CARD

THE BUSINESS OF DESIGN



By now, you're probably aware that no less than 18 manufacturers have or will introduce their own version of a 64K RAM. And that each version will be at least a slightly different design. So how will you choose one intelligently? How will you base your decision knowing that each manufacturer feels strongly justified in choosing the architecture and manufacturing process it will use?

One of the best ways to evaluate any semiconductor memory is to look at a company's past experience in producing them. Look beyond the performance specifications and find out just how much they know about the business of design.

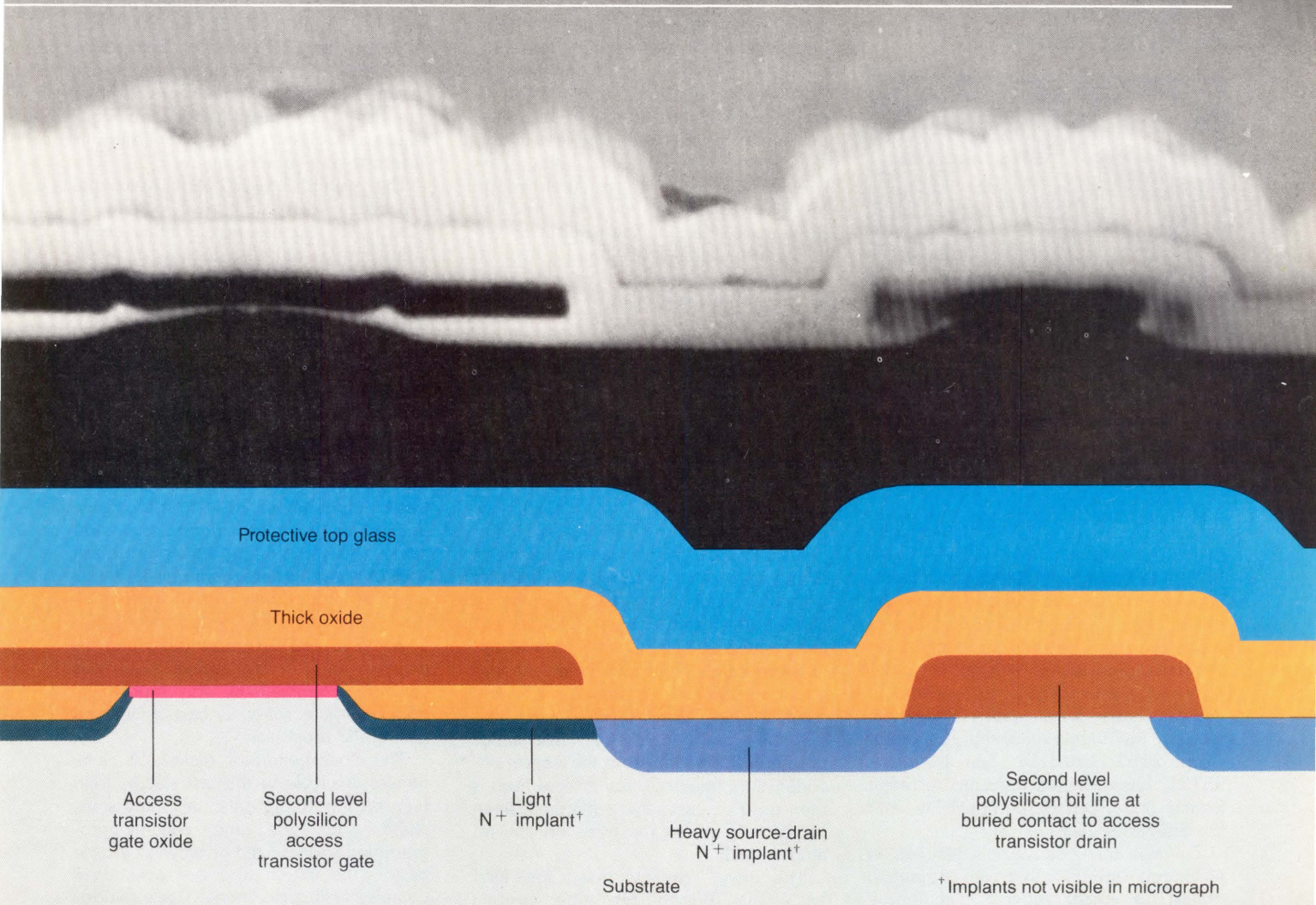
At Mostek, the business of design means that the ultimate challenge for our designers is to enhance the manufacturability of every device we make so that it can be produced reliably, in volume. It means that we incorporate and refine, wherever practical, the same proven design techniques that helped us achieve world dominance at the 4K level, and to an even greater extent, at the 16K level.

But it also means that we fully investigate and develop new approaches and new circuitry to satisfy the new constraints inherent in progressively sophisticated MOS memories.

A good example of this business-like approach to design is the use of polysilicon bit lines in our Scaled POLY 5* process.

How to choose a 64K RAM wisely after examining the specs.

MOSTEK.

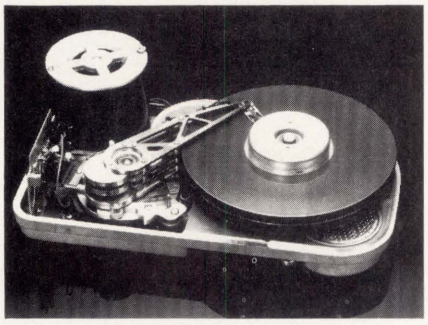


Though diffused bit lines are undeniably correct for our industry-standard MK4116, VLSI geometries precluded their efficient use in the MK4164. Consequently, we needed a new way to maximize the usable signal generated from the smaller area available for storage cells. So we switched to polysilicon bit lines. This switch significantly improved the capacitor-to-total-cell area ratio and resulted in 50% more usable signal to the sense amplifiers than if we had used diffused bit lines with the same layout rules.

Though the switch to polysilicon bit lines is just one example of numerous MK4164 design innovations, it is representative of the driving force behind all of them: Improved manufacturability. Because for us, achieving higher levels of manufacturability is not only a noble design goal, it's also smart business. It's why we make and ship more dynamic RAMs to more companies than anyone else in the world. And it's how we intend to maintain that distinction.

To find out more about the added confidence that designed-in manufacturability can give you, send for our 64K RAM brochure that explains it in detail. Write Mostek, 1215 West Crosby Road, Carrollton, Texas 75006. (214) 323-6000. In Europe, contact Mostek Brussels, 660.69.24.

8″ Winchesters Double Density Using Moving Coil Actuator



Using low mass, low load force, contact start/stop head technology, Quantum's 8″ Winchester provides SA1000 compatibility, while altering rotational speed and flux and track densities to accommodate track position servo and 10M-byte/disc capacity

Q2000 low cost 8″ (20.3-cm) fixed disc drives provide 10M-, 20M-, and 30M-byte capacities. Based on a combination of reliable technologies, the drives offer a capacity per disc that is more than double that of competitive products at costs competitive with older technology drives. While rotationl speed, flux, and track densities differ to accommodate the higher capacity, Quantum Corp, 2150 Bering Dr, San Jose, CA 95131, has designed the units to retain format and interface compatibility with the Shugart SA1000.

To raise track density to 345 bits/in (135/cm) (double that of competing drives), a rotary moving coil torque motor head actuator and temperature compensation is used instead of open loop stepper motor actuators. This solution combines attractive aspects of linear and rotary voice coil actuators in an innovative rotary actuator (patent pending) that creates pure torque with no sideways stress on actuator bearings. Balanced statically so that the drive can be rotated in any direction without head or arm movement, it allows the bearing structure to be lower in cost than those used in alternative designs.

Its construction requires only a ring magnet, two flat plate magnetic circuit elements, a single plane moving coil, and a 2-bearing structure. It is driven by a simple 2-phase electronics system, and incorporates a low inductance coil for low power consumption.

Providing an average access time of 50 ms for the 10M-byte and 60 ms for the 30M-byte drives, it is faster than stepper systems and approaches the performance of expensive voice coil systems. Positioning accuracy and timing is enhanced through the use of an optical position encoder located on the actuator. This encoder is fabricated using glass reticle/LED/photodiode technology historically used in low cost precision positioning systems. The result is an encoder system that is accurate to over 10 times the track density of present units, leaving room for growth to higher track densities.

Higher track density disc drives require temperature compensation to ensure accurate track location and reliable operation. This system, instead of the dedicated track position reference surface traditionally used, uses a direct track position feedback derived from the disc surface itself. Capable of updating track position 50 times/s, this temperature compensation servo technique uses the index timing space at the end of each track to encode track location information between the last inter-record gap and the index pulse. On initial drive power-up, and continuously thereafter, an onboard microprocessor reads actual track and head location coding once each disc revolution and compares it with actuator position information from the optical encoder. Any head position error sensed is then used to offset the actuator position to precisely center the head on any intended track.

The drives use low mass, low load force IBM Winchester type contact start/stop head technology, and 200-mm OD, Winchester type media. Maximum recording density is 6000 bits/in, maximum flux density is 6600/in, and track density is 345/in. Rotational speed is 3000 r/min. Physical interface and power supply characteristics closely match those of floppy drives. Packaging allows the drive to mount using the same attachment hardware as 8″ (20.3-cm) floppies.

Included in the family are the 10.67M-byte (unformatted) single-disc Q2010, the 21.33M-byte 2-disc Q2020, and the 32M-byte 3-disc 02030. Transfer rate is 4.34M bits/s, average latency is 10 ms, and access times are 15-ms track to track, 100 ms max, and 50-ms average (Q2010) to 60-ms average (Q2030).

Circle 359 on Inquiry Card

Automated LSI/VLSI Test System Handles Complex Chips

A 128-pin LSI/VSLI/hybrid semiconductor test system, the S-3275 has sophisticated pattern generating and timing capabilities and can handle 64 inputs and 64 outputs at up to 20 MHz. Tektronix, Inc, PO Box 500, Beaverton, OR 97077, has also included a software system that improves memory utilization and increases processing speed, and contains a networking option that permits interface to any large computer.

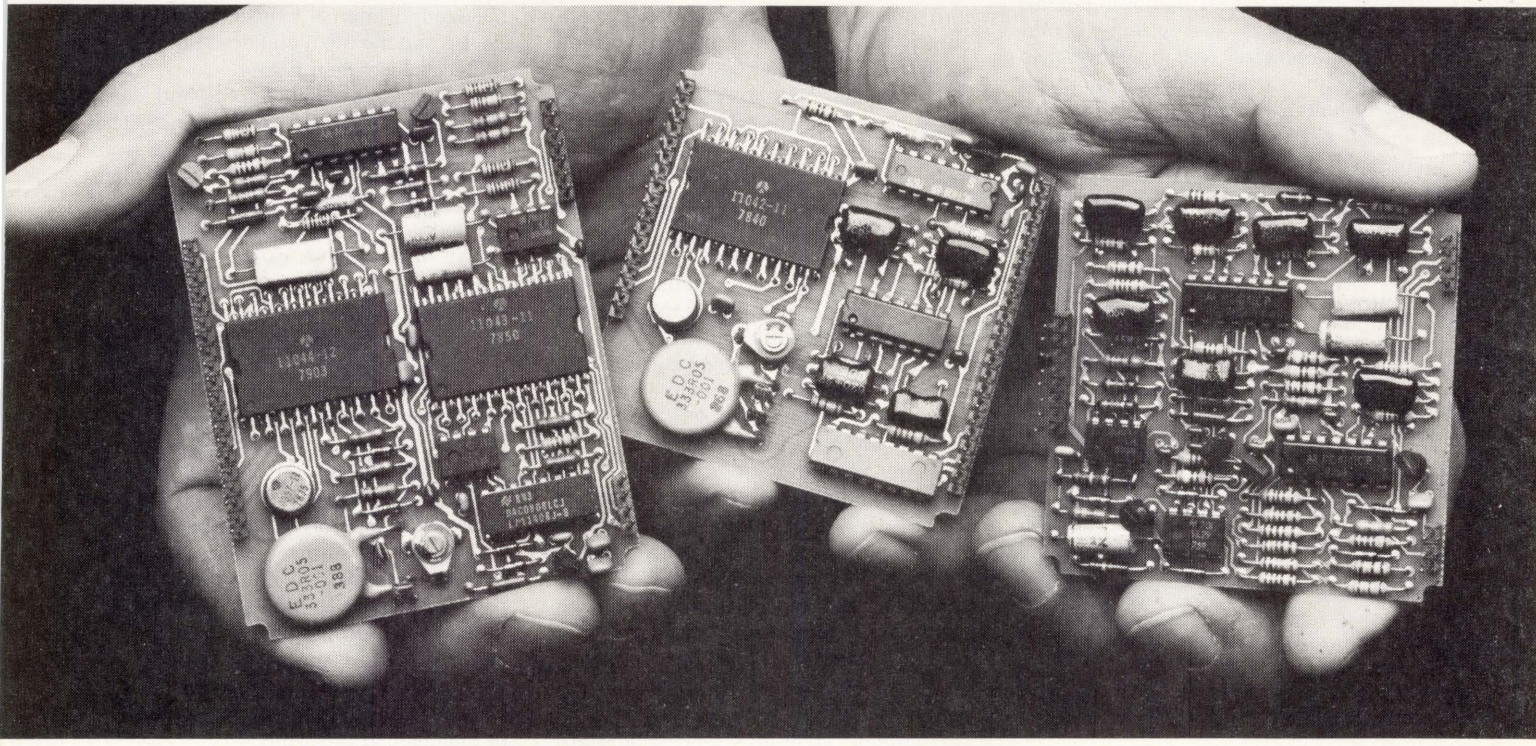
The system has 20-MHz functional capability and realtime error logging. Its 128 data channels operate either as 64 input and 64 output channels, or as 64 input/output channels. Included in the system's dual-memory architecture are enhanced pattern generator, clock generator, and pin electronics cards. Sophisticated pattern control and sequencing as well as algorithmic pattern generation are supplied by the 2952 pattern processor. Four bits of pattern data (force, inhibit, compare, and mask) are sent by the processor to each pin electronics card at the 20-MHz rate. Force and compare pattern memories are 64 bits by 4k words deep; inhibit and mask pattern memories are 64 bits by 1k words deep. In algorithmic pattern generation mode, the pattern processor generates 12X, 12Y, 12Z, 16 force data, and 16 compare bits on each cycle. Addresses can be scrambled by the topological memory (4k words by 12 bits), an integral part of the processor.

The clock generator makes 16 clock phases available to the test station. Sixteen sets of timing data, including start, width, and cycle time, can be programmed and selected on a cycle by cycle basis by the pattern processor, resulting in complex split cycle timing. Cycle periods range from 500 Hz to 20 MHz with time resolution to 8 ns. Clock generation features include 125-ps phase edge resolution and 1-ns skew and accuracy with automatic calibration. In addition, the clock can operate in a free-running mode, be synchronized to the test device, or be switched on a cycle by cycle basis.

The system's pin electronics cards have been enhanced to accept the four data bits presented by the pattern processor and have oncard shift registers (4k deep) available for auxiliary force and compare storage as well as for realtime error storage. Other card features include fixed or toggled data sources, programmable driver and comparator sample and hold circuits, and analog access to the system's 50-Ω switching matrix.

(continued on page 64)

R24. The first 2400 bps modular modem.



Rockwell's compact MOS-LSI modem gives new physical design freedom.

Micro power

Rockwell's R24 Modem is the most compact 2400 bps MOS-LSI modem available today. Its small size and modularity give designers a whole new form factor flexibility. Requiring only 25 square inches of system area, the R24 is ideal for terminals and communications equipment.

The R24 provides functional flexibility also. Of its 3 modules, one is the transmitter, two the receiver. Terminal designers can offer transmit-only or receive-only options. And, the R24 is Bell 201 B/C and CCITT V.26 and V.26 bis compatible.

With its major functions in LSI circuits, the R24 is solid-state reliable and economical. It can be configured for operation on either leased lines or the general switched network. And, each low-profile module can be plugged into standard connectors or wave soldered onto system PC boards.

A new generation of modems from the company that's delivered more high-speed modems than anyone in the world. That's Rockwell Micropower!

For more information, contact Modem Marketing, Electronic Devices Division, Rockwell International, P.O. Box 3669, RC 55, Anaheim, California 92803. (714) 632-5535.

Rockwell International

...where science gets down to business

With its optional integrated waveform digitizer, the system can perform waveform analysis. Its analog access, integral to the test station, has both parallel and GPIB interfaces. The system will perform dc parametric testing with Kelvin sensing to the device under test and can make single-shot time measurements with 50-ps resolution. All graphics generated by the system can be converted to hardcopy form.

TEKTEST III, Version IV, the system's software, is an English-like self-documenting language. It has realtime debugging and true foreground/background operation that allows up to four programming tasks to be performed while testing continues. While the software enhancement requires a minimum memory configuration of 42k words, memory management, and floating point processor, it improves memory utilization. The networking option, an extension of the operating system software, provides the interface to user defined mainframes. With it the user can interface the test system to any large computer.

Circle 360 on Inquiry Card

Memory Test System Offers Realtime Bit Mapping Option

1389 solves many problems of testing high performance semiconductor memories, including fast byte wide static RAMs, and large dynamic RAMs. The system, developed by Teradyne Inc, 21255 Califa St, Woodland Hills, CA 91367, delivers high integrity waveforms to the pins of the memory under test. It offers 0.25-ns timing accuracy at the device pins and has waveform flexibility needed for complex functional test patterns. Realtime bit mapping (RTBM) option is an interactive tool that provides a color display showing the precise location of the failing memory bits and identifying timing, voltage, and pattern conditions under which failures occur.

Consisting of mobile system controller, mainframe, one or two remote test electronics modules, and system power supplies, the unit improves memory testing through its architecture. Computing controller is an 18-bit processor that controls system instrumentation, handles test program preparation, and analyzes test results. The system is supplied with a 64k memory that expands in increments of 64k to a maximum of 256k.

The mainframe houses pattern generator, waveform generator, and analog circuits. Controlling functional testing, the pattern generator produces address sequences, input data, and expected output data for the memory under test. It also controls cycle by cycle selection of cycle times, edge delay sets, and format sets. Each functional test cycle is controlled by a 48-bit microinstruction stored in the pattern control RAM.

The realtime bit mapping option can be added to the pattern generator to identify memory cells that fail during a functional test. With the addition of a color CRT terminal, up to 100 different colors show the location of each failed cell and the conditions under which it failed. RTBM is used in production testing to identify partials and to select rows and columns of RAMs that incorporate redundancy.

The waveform generator consists of a crystal oscillator, cycle time generator, edge delay generators, and formatting circuits. Memory under test cycle times and all time functions within each memory under test cycle are derived from a single 125-MHz crystal oscillator. Cycle times can be programmed from 50 ns to 32 μs in 0.50-ns increments. Computer controlled analog delay circuits in each transmission path maintain skew and edge to edge delays at the memory under test pins to within 0.25-ns system specification.

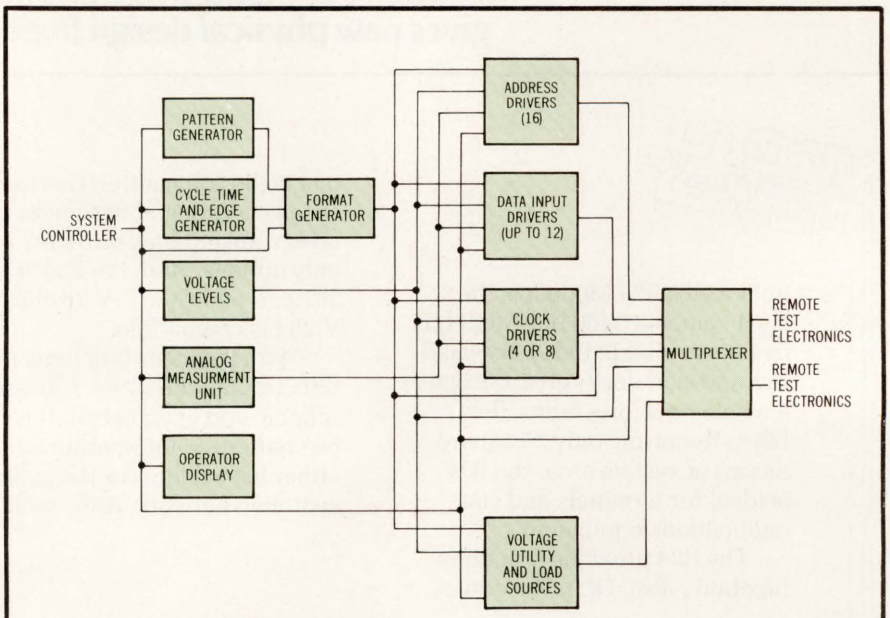
Automatic edge lock (AEL) a time domain reflectometry technique, automatically adjusts the 150 analog delay circuits to compensate for differences in path lengths between the crystal oscillator and the pins of the memory under test. In addition to maintaining timing accuracy, AEL also verifies address, data input, and clock driver levels. Calibration occurs in the few-millisecond interval between testing one device and the next, and does not require a special calibration fixture.

Each address, data input, and clock driver has a 50-Ω output impedance. This controlled impedance is maintained from driver outputs to remote test electronics to ensure high integrity waveforms at the pins of the memory under test.

The remote test electronics module contains data output detectors, I/O switching, device interface board, and load switching. Having the detectors in the remote test electronics allows accurate data output detection for devices with either low or high impedance outputs. I/O switches in the remote test electronics allow testing of devices with separate data input and output pins and those with common I/O data pins.

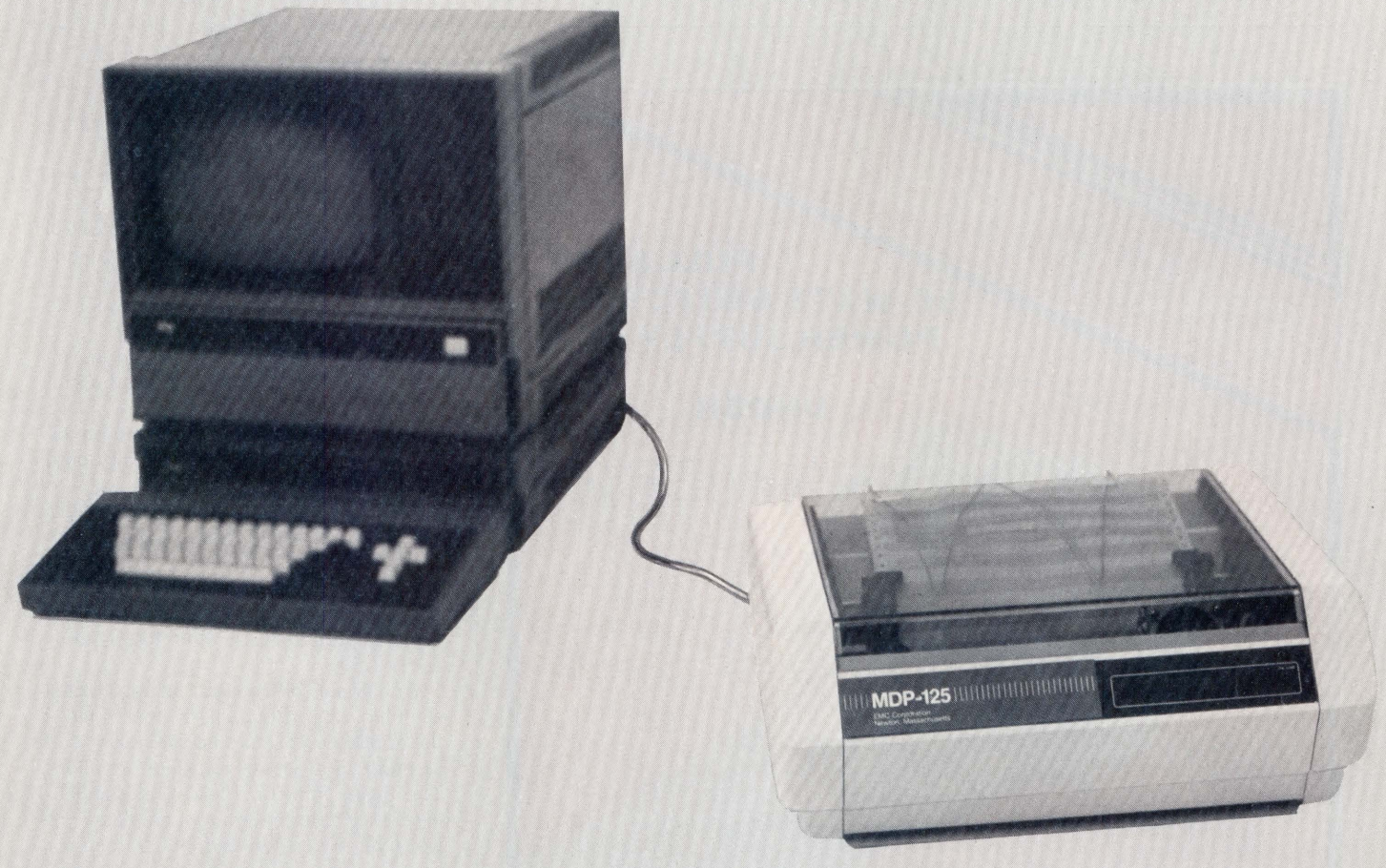
The unit is supplied with operating, utility, applications, and maintenance software recorded on data cartridges. Memory test programs are prepared using the Pascal-T programming language which simplifies the process of preparing device test programs and reduces the cost of maintaining programs.

Circle 361 on Inquiry Card



Mainframe of Teradyne's J380 memory tester houses pattern generator waveform generator, and analog circuits. Functional test cycle is controlled by 48-bit microinstruction stored in pattern control RAM. Address, data input, and clock drivers have controlled 50-Ω output impedance maintained to remote test electronics, ensuring high integrity waveforms at pins of memory under test

Reliable Hard Copy Output at Low Cost.



For your intel® Microcomputer Development System.

The Model MDP-125 from EMC Corporation is a heavy duty, hard copy printer designed especially for use with Intel Intellec* Series Microcomputer Development Systems.

The MDP-125 prints a 96 ASCII character set in 9x9 dot matrix, with true upper/lower case characters and underlining. It operates bi-directionally, for maximum throughput, at up to 125 characters-per-second. It's available in 80-column, and 136-column wide-carriage versions. And it comes with a ten-foot cable that plugs directly into your Intellec* system.

With our instruction manual, and features like automatic on/off motor control, you'll be operational in minutes. You can send information to the printer from the Intellec* system console without additional manipulation of the printer controls. An optional Control Panel provides off-line self-test.

The MDP-125 is ruggedized, for reliable performance under high duty cycles, and quietized, with sound-deadening, included as standard. Other features include a front- or bottom-loading tractor-feed mechanism, and a long-life mobius loop ribbon cartridge. The printer uses fanfold paper, and can produce up to five copies plus original.

To order hard copy output for your Intellec* system, call or write the Marketing Department:

EMC² CORPORATION
385 Elliot Street
Newton, Massachusetts 02164
TWX: 922-531 EMC CORP NEW
Tel: (617) 244-4740

* intel® and INTELLEC are registered trademarks of INTEL Corporation.

CIRCLE 40 ON INQUIRY CARD

Signature Analysis Option Allows Test System to Handle Loaded Boards

Complex circuits, ROMs, RAMs, and I/O based printed circuit boards can be completely tested even if signature analysis has not been designed into the board.

Option 100 for the model 3060A board test system from Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, dynamically and automatically tests complex digital circuits, using signature analysis, a data compression technique invented by HP in 1977. Permitting the system to test with automatic isolation capability beyond the node, even on bidirectional buses, the option simplifies production testing by using automatic probing and backtracing hardware and software, thus eliminating operator intervention.

The option provides the stimulus (up to 2-MHz rate), measurement (up to 10-MHz rate), and automatic diagnostic functions required for pass/fail testing and fault isolation. The dynamic digital functional test capability can be used on both dedicated and multiplexed bus architectures. A built-in counter, logic comparators, and high speed RAM backed drivers are included for external microprocessor stimulation, analysis, and fault diagnosis.

The stimulus is designed to interface with the typical microprocessor architecture. Stimulus interfacing with the data and control buses consists of RAM backed drivers which can create data and control signals at speeds up to 2 MHz. Dynamic stimulus, which interfaces to the address bus, is connected to a binary sequencing generator (counter). These two basic building blocks can be connected in one of four ways to stimulate the board under test.

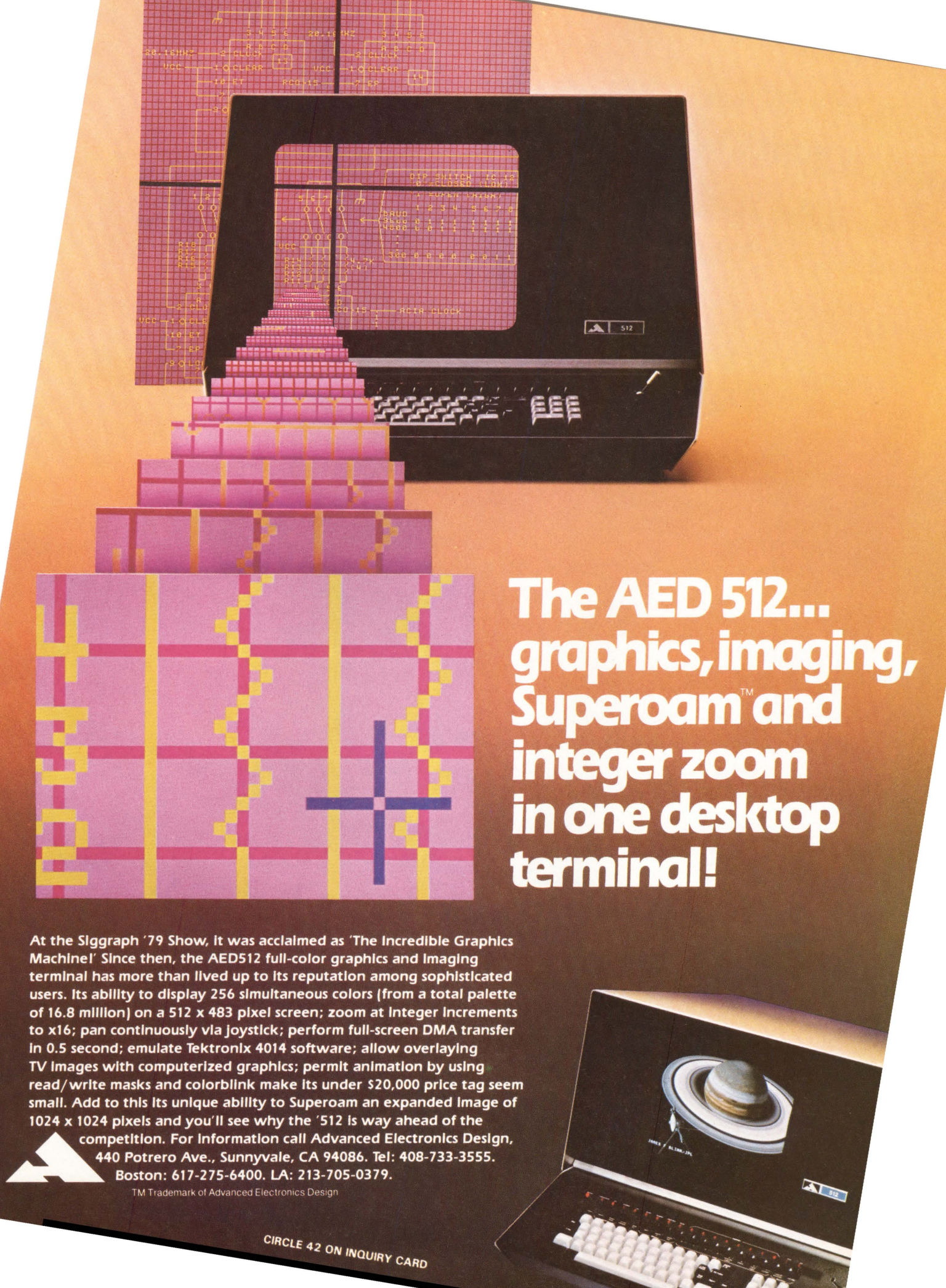
Dynamic drivers can be 3-stated on the fly by a hardware signal from the board under test. This allows the test system to interface to bidirectional data buses and to multiplexed address/data buses. To allow high speed operation, 16 of the high speed drivers have memory behind them, providing signature analysis stimulus programs and other test patterns to circuitry.

Additional electronics in the digital stimulus response analysis unit control the application of stimulus programs used in production testing and fault isolation. The digital functional test (DFT) software gives the test programmer complete control over all customized microprocessor based testing electronics to design and implement production tests for boards in microprocessor based products.

Signature analysis detection circuitry in the tester can be multiplexed through the system scanner to the bed of nails fixture to take signatures on up to 500 different nodes during any one test. If these signatures are good, the board is good. If a bad signature is found, automatic backtracing software performs fault isolation.

Automatic backtracing software is capable of handling analog signals as well as digital signatures. This is an advantage in testing hybrid circuits because backtracing software reduces the problem of designing a functional test for a printed circuit board to that of designing tests for different nodes on the board. The DFT software takes care of the organization and puts nodal tests together automatically into a functional circuit test.

Circle 362 on Inquiry Card



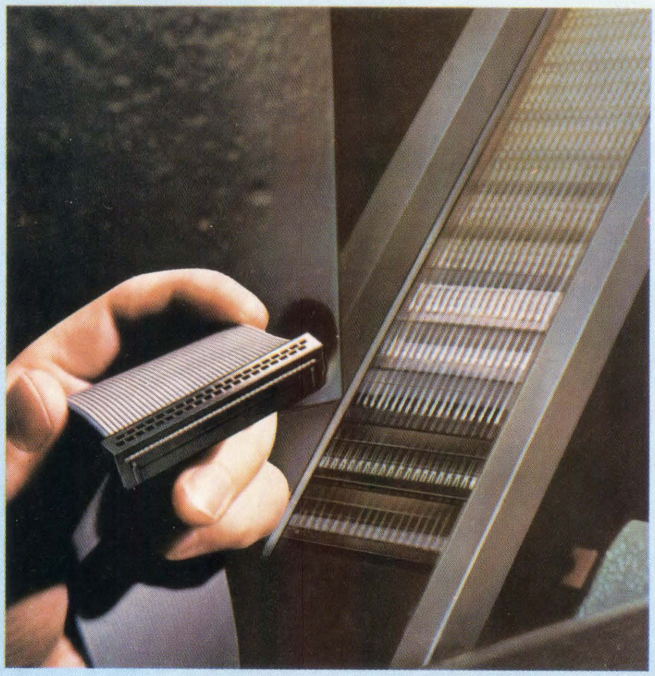
The AED 512... graphics, imaging, Superoam™ and integer zoom in one desktop terminal!

At the Siggraph '79 Show, it was acclaimed as 'The Incredible Graphics Machine!' Since then, the AED512 full-color graphics and imaging terminal has more than lived up to its reputation among sophisticated users. Its ability to display 256 simultaneous colors (from a total palette of 16.8 million) on a 512 x 483 pixel screen; zoom at integer increments to x16; pan continuously via joystick; perform full-screen DMA transfer in 0.5 second; emulate Tektronix 4014 software; allow overlaying TV images with computerized graphics; permit animation by using read/write masks and colorblink make its under $20,000 price tag seem small. Add to this its unique ability to Superoam an expanded image of 1024 x 1024 pixels and you'll see why the '512 is way ahead of the competition. For information call Advanced Electronics Design, 440 Potrero Ave., Sunnyvale, CA 94086. Tel: 408-733-3555. Boston: 617-275-6400. LA: 213-705-0379.

TM Trademark of Advanced Electronics Design

CIRCLE 42 ON INQUIRY CARD

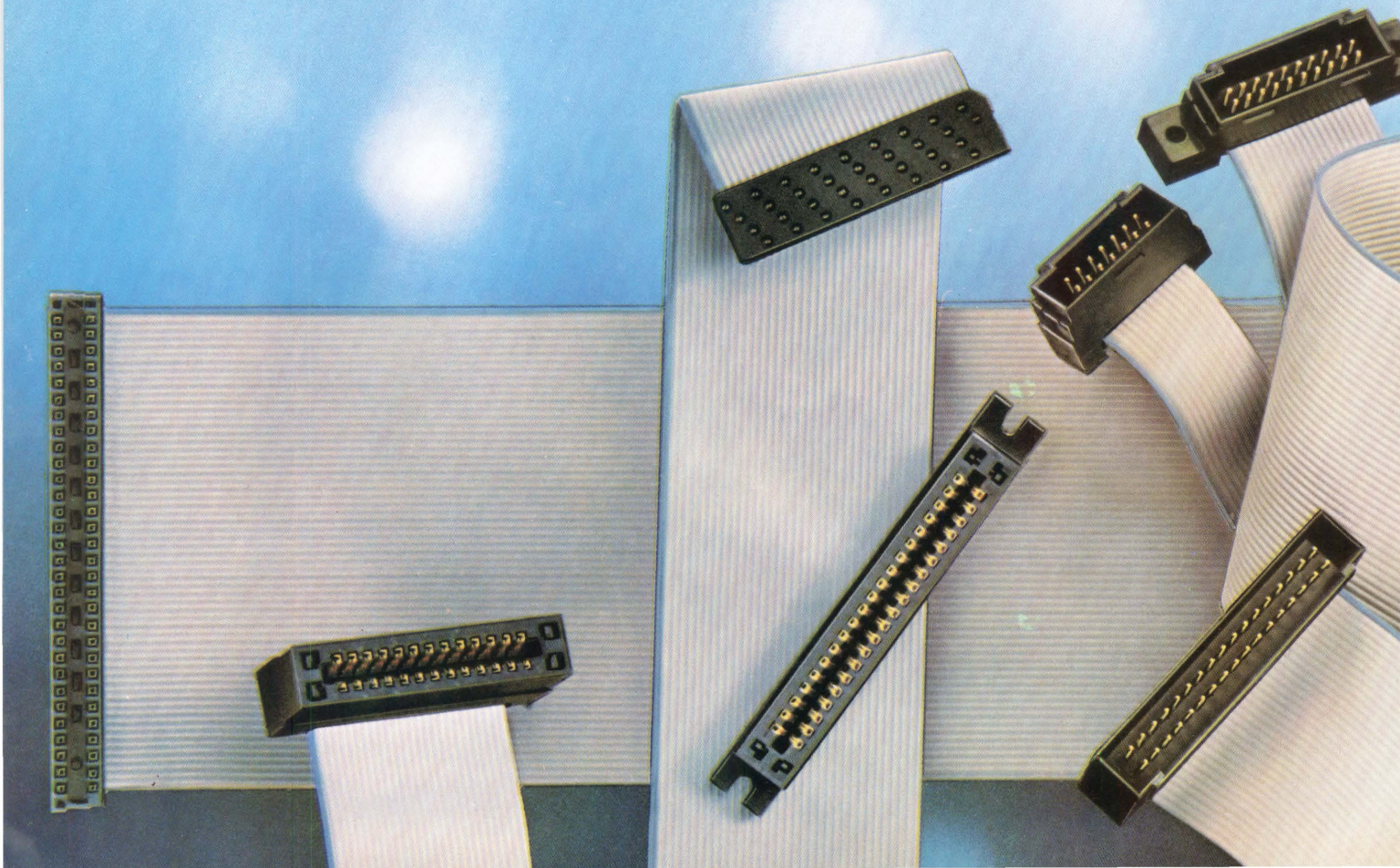
Double your production rate of ribbon cable assemblies.



Now you can terminate AMP Latch connectors at the rate of 450 an hour. That's more than double the speed of what you can do with other ribbon cable connectors.

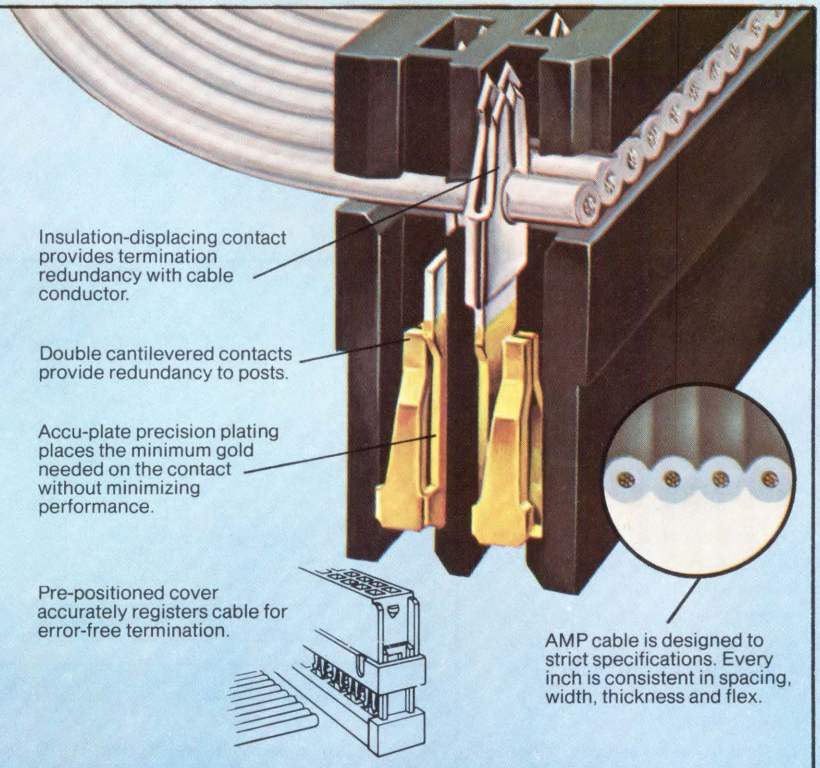
Our new semi-automatic tool makes it happen. It precision feeds, positions and terminates preassembled receptacle connectors in one step. Our precision cable further minimizes rejects, because it's designed and manufactured to strict dimensional specs. And our complete range of fully shrouded headers includes a positive locking type you can squeeze-to-release with one hand.

With these continued advancements and our wide mix of connectors, the AMP Latch system is more productive than ever.



AMP Facts

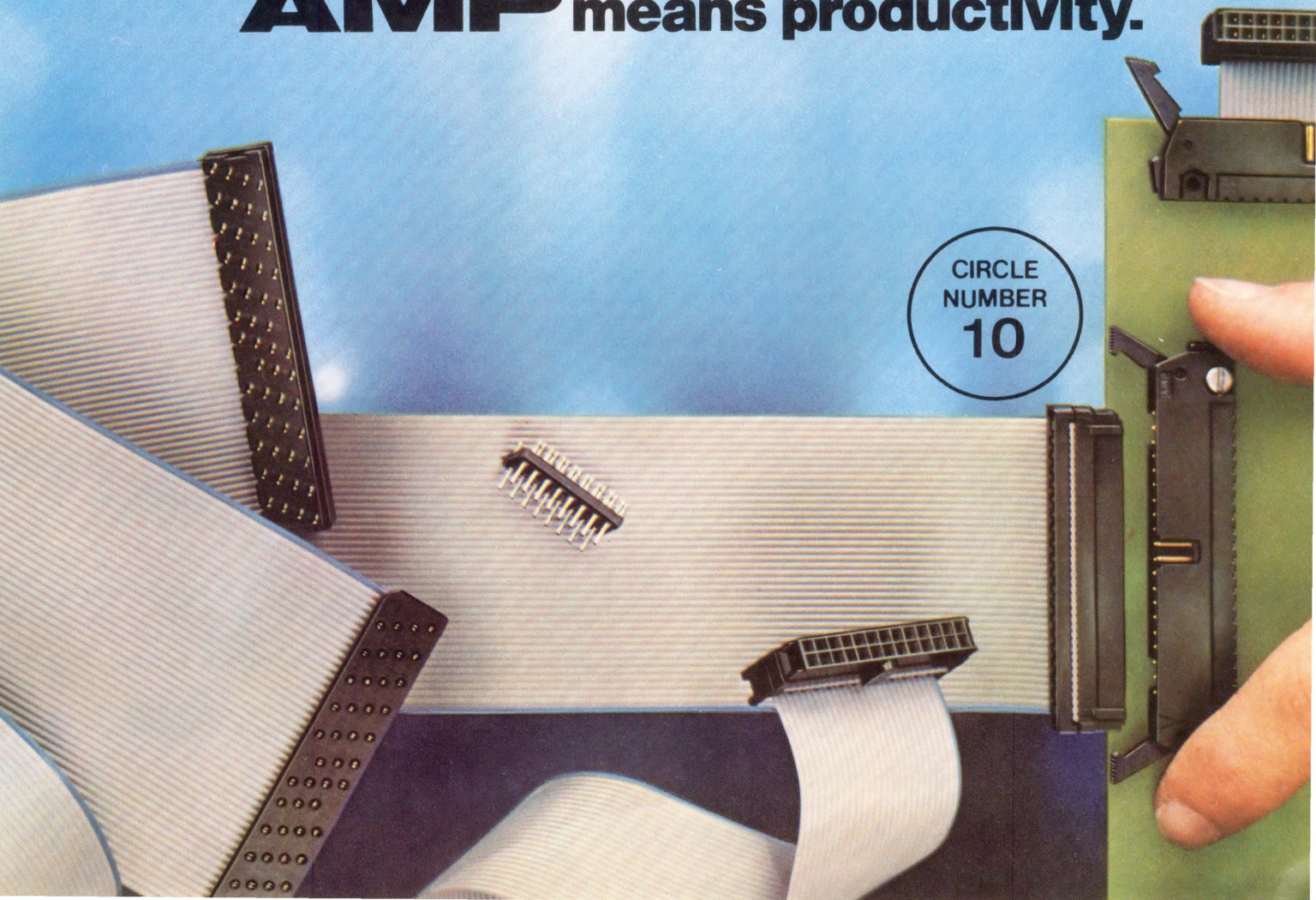
Wire Types: Small-gauge solid or stranded discrete, plus flat ribbon, woven ribbon and other types of flat cable with round conductors on .050" centers.
Size: 10 through 60 positions.
Connector Types: Wide variety of cable-to-cable, card edge, DIP and receptacle connectors available.
Electrical Current Rating: 1 ampere (continuous).
Operating Temperature Range: −55°C to +105°C
Dielectric Withstanding Voltage: 500 volts RMS.
Tooling: Pneumatic, manual and semi-automatic bench termination machines.



For a free sample, call the AMP Latch Information Desk at (717) 780-8400.

AMP Incorporated, Harrisburg, PA 17105

AMP means productivity.



Multifunction Information Processing System Uses Multiple Bus Architecture

Workstation based information processing systems do away with the traditional concept of a CPU and distribute all computing power to workstations. The Convergent family, introduced by Convergent Technologies, 2500 Augustine Dr, Santa Clara, CA 95051, extends from a standalone system with minicomputer power to a resource sharing cluster system of 16 workstations with data storage capabilities to 116.5M bytes. The systems have processing power equivalent to a large minicomputer.

Series 1000 standalone systems, each consisting of a single workstation with 128k bytes of RAM plus mass storage, are CT-1111-1 with 1M-byte dual floppy subsystem for storage and the CT-1121-1 with an 8″ (20.3-cm) Winchester subsystem along with one floppy disc for a total of 10.5M bytes. Workstation electronics consist of three to four printed circuit assemblies: processor, memory-I/O, optional memory expansion, and video display control boards. These four assemblies are linked through a proprietary CT-BUS.

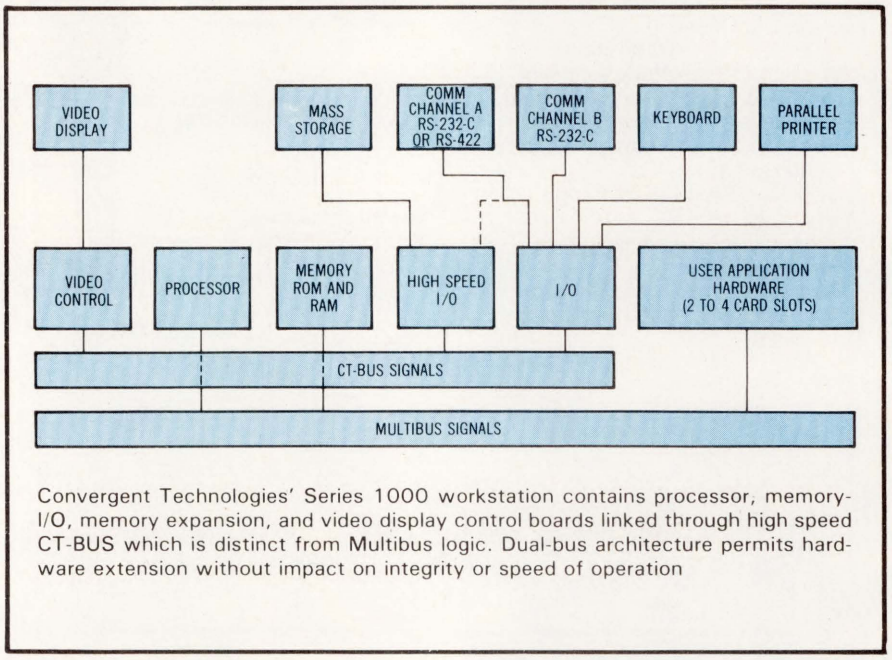
The processor board contains an Intel 8086 16-bit microprocessor operating at 5 MHz. In addition to the 8086, the board may contain an optional 5-MHz 8087 mathematics processor. Four high speed DMA channels are used for I/O and for a Multibus slave to gain access to the CT-BUS signals. These channels operate at 3.3M bytes/s and support the video subsystem, two high speed serial channels, and mass storage interface.

A programmable video display system permits development of sophisticated screen formats. The 15″ (38-cm) display at 50-MHz refresh rate is organized as 34 lines by 80 or 132 characters, with the screen divisible into virtually unlimited windows. Standard character set contains a full 256 characters, including the entire printing ASCII set, bit map graphics, and some foreign characters. Additional character sets are RAM loadable, since all characters and graphics are completely soft.

Dual-bus architecture allows addition of user hardware extensions without impacting integrity or speed of operation of workstation electronics modules. Communication between masters operating on the two buses or between the workstation processor and Multibus slave is via an over-lapped memory mapping scheme or through a DMA channel. Memory addressing, interrupt recognition and processing, as well as I/O addressing may be done completely independently in the Multibus region, or may be shared with CT-BUS logic. All interfaces between the two buses are under software control of the workstation processor.

Five programming languages support development of system and application programs. Languages include assembly language, BASIC, Pascal, COBOL, and FORTRAN. CTOS, a compact multitasking operating system, serves as a building block for development and implementation of application software.

Circle 363 on Inquiry Card



Convergent Technologies' Series 1000 workstation contains processor, memory-I/O, memory expansion, and video display control boards linked through high speed CT-BUS which is distinct from Multibus logic. Dual-bus architecture permits hardware extension without impact on integrity or speed of operation

Business Computer System Family Extended at Top and Bottom

Multiuse, entry level Datasystem 315 and top of the line commercial D750 and D780 systems are based on the PDP-11/23 and VAX processors. Introduced by Digital Equipment Corp, Maynard, MA 01754, the units extend the range of commercial capability provided within the compatible families.

Available with a choice of six programming languages and two operating systems, the 315 can be used as standalone system, network node, or store and forward terminal. Its base memory is 64k bytes (expandable to 256k bytes). It uses a VT100 video terminal and a dual RX02 double-density floppy disc drive for 1M bytes of mass storage.

The system is available with either the commercially oriented CTS-300 or RT-11 general purpose operating system. CTS-300 includes the business oriented DIBOL-11 programming language, DECform program package for video terminal screen operations, and a sort utility and file handling utility. RT-11 offers a choice of five programming languages including FORTRAN IV, BASIC, FOCAL, and APL, and can be used for realtime applications.

The D700 series contains 4.3G bytes of virtual address space and up to 2G bytes of user program space. It is capable of up to four times the performance of the Datasystem 500 series. Information management capabilities provided by the systems are compatible with other Datasystems, including the VAX RMS file management system, VAX-11 FMS forms utility, DATATRIEVE query and report writer, selection of high level languages, and extensive communications packages. VAX-11 COBOL provides fast execution of generated object code, high compilation speed, and ease of use. VAX-11 BASIC and PL/I are also available. For data exchange between Datasystems, DECnet networking facility is available. □

Circle 364 on Inquiry Card

THE LEADING MICROPROCESSOR OPERATING SYSTEMS FOR THE 1980s

MTOS 86

MTOS-80

Real-time operating system for the 8080. In service since 1976

MTOS-68

Real-time operating system for the 6800. In service since 1976

MTOS-86MP MTOS-80MP

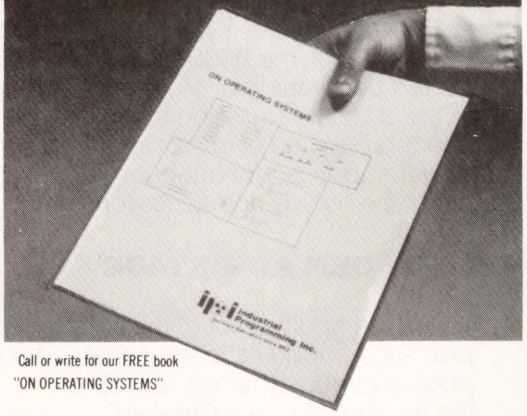
Multi-Processor versions of MTOS-86 & MTOS-80.

THE MULTI-TASKING OPERATING SYSTEM FOR THE 8086

Unlike some operating systems, the MTOS family is written in assembly language.

The result: compact, efficient programs.

MTOS is sold in source form; the user can specialize MTOS for his own applications.



Call or write for our FREE book "ON OPERATING SYSTEMS"

COMING SOON!

MTOS-68K

FOR THE MOTOROLA **68000**

Ask for a free copy of the MTOS-68K User's Guide.

These MULTI-TASKING OPERATING SYSTEMS are sold under a liberal licensing policy which allows resale of the object program, when embedded within a product, without further charge.

In Israel:
CONTAHAL, LTD.
83 Gordon Street, Tel Aviv
Telephone: 22 41 15

In Belgium:
BETEA S.A.
Chaussee de Louvain 775
B-1140, Brussels
Telephone: (02) 736 80 50

In West Germany:
ALFRED NEYE-ENATECHNIK
Schillerstrasse 14
2085 Quickborn (Hamburg)
Telephone: 041 06 / 612-240

In Scandinavia:
AB TELEPLAN
Tritonvägen 25, Solna, Sweden
Phone: 08-98 10 00 Tx. 17587

In Japan:
TOKYO ELECTRON LIMITED
Shinjuku Nomura Bldg. 1-26-2 Nishi-Shinjuku
Shinjuku-Ku, Tokyo 160
Telephone: 343-4411

In Benelux:
C.N. ROOD B.V.
Cort v.d. Lindenstraat 11-13, Postbus 42
2280 AA Rijswijk, Nederland
Telephone: 070-996360, Tx. 31238

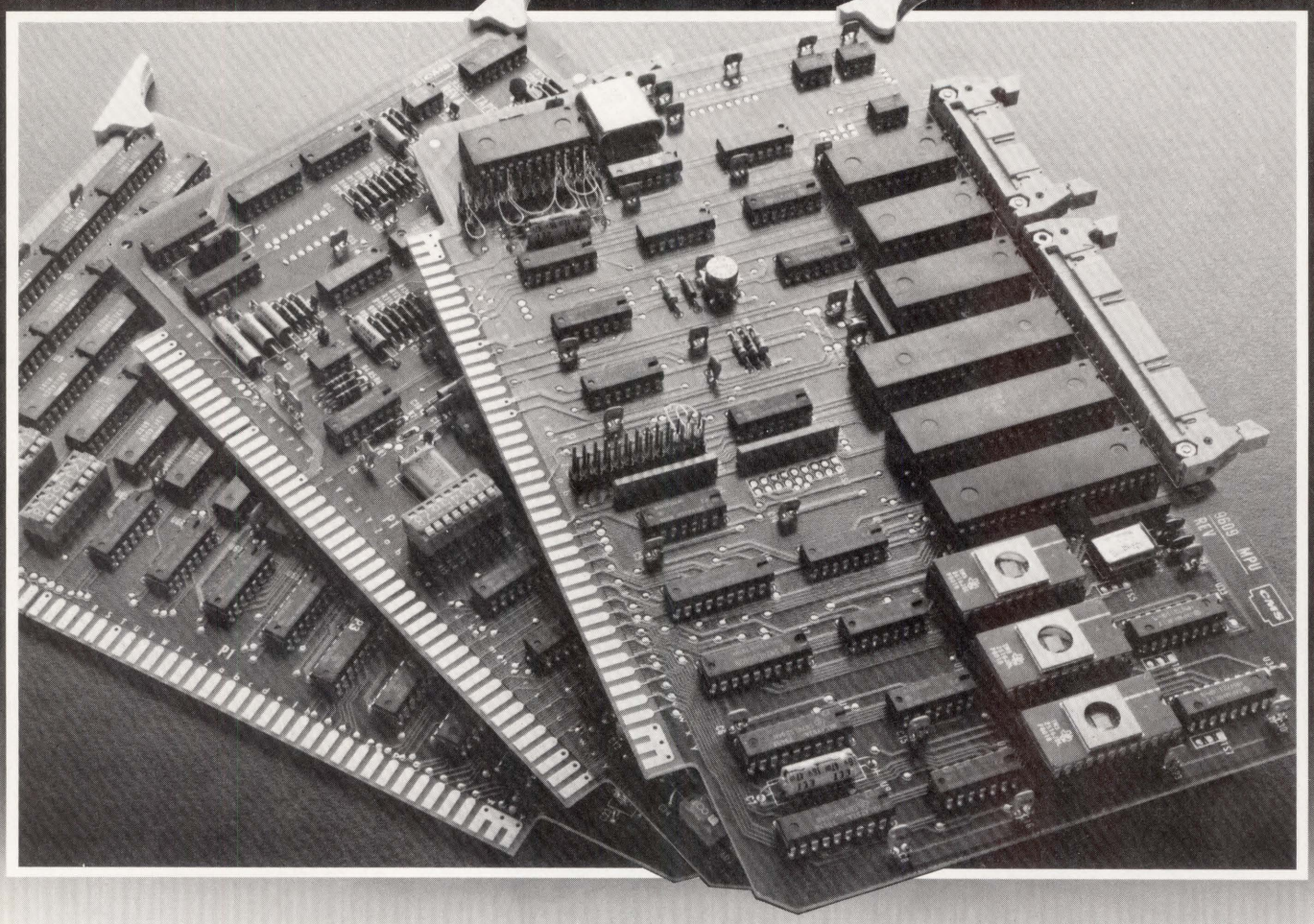
In Australia:
INDUSTRIAL COMPUTER SYSTEMS P / L
269 Auburn Rd., East Hawthorn, VIC 3123
Telephone: (03) 827-389

ipi Industrial Programming Inc.

Software Specialists Since 1963

100 Jericho Quadrangle, Jericho, N.Y. 11753 • (516) 938-6600 • Telex 429808

COMPARE
THE CMS 6809 ADVANTAGE



Creative Micro Systems is proud of its line of general purpose microprocessor support modules. These M6800/M6809 based modules are pin and outline compatible with the industry standard EXORcisor* and Micromodule* bus.

COMPARE THE CHOICE

That's why we want you to compare our products with the competition before you design your next microprocessor based system.

Each module in our product line is designed to respond to the needs of a major computer system function. Our 9609 module, featured above, is a complete microcomputer on a single board. It features the MC6809 processor, 6K of EPROM, 1K of RAM, 40 parallel I/O lines, 2 RS-232C serial ports, BREAK detect, 3 16-bit programmable timers, priority interrupt vector generator and a power failure protect/restart circuit.

*Trademark of Motorola

For more extensive system requirements, the 9609 is supported by a variety of Memory, I/O, and Data Acquisition modules, and a broad line of card cages, power supplies, mother boards, prototype boards and accessories.

THE OEM ADVANTAGE

Try to find another set of microprocessor modules in the same price and quality range with all the positive features Creative Micro Systems has to offer.

Original Equipment Manufacturers who compared our products have specified Creative Micro Systems for applications in data acquisition, data communication and encryption, materials testing, automatic test equipment, process control, energy management systems, agricultural instrumentation and small business data processing systems.

WANT MORE TO COMPARE

Once you compare you'll agree Creative Micro Systems has more to offer your application. Write or call for our new product catalog. We'll also be happy to tell you about our exciting new products in development now.

CMS

Creative Micro Systems
11642-8 Knott Street
Garden Grove, CA 92641 USA
Telephone (714) 898-9669

Find us in the 1980 IC Master Catalog on pages 2608-2609.

In EUROPE Dialogue Marketing (Electronics) Ltd. Rose Industrial Estate, Unit 11G, Bourne End, Bucks, England, Telephone 06285-26729 Telex 848080 MICRO G

CIRCLE 131 ON INQUIRY CARD

THE LATEST ADVANCE IN VIDEO GRAPHIC HARD COPY RECORDING FROM HONEYWELL

VGR 4000, Honeywell's new and advanced video graphic recorder, provides fast, crisp, 8½ x 11″ hard copies on dry silver paper from most CRT's and other video sources.

White-on-black or black-on-white images are as simple as flipping a switch. With options, images can be produced having up to 16 shades of grey or even more.

An innovative processing technique eliminates the need for large heated platens. This allows the recorder to run cool, consuming very little energy.

The VGR 4000 is the only recorder on the market available with a self-contained test-pattern generator providing a choice of formats for proper copy verification.

Rugged, yet cleanly designed for easy operation, the compact VGR 4000 can be used on a desk top or rack-mounted, taking up only 7″ of front panel space.

Honeywell's VGR 4000 is the latest advance in video-input hard-copy reproduction systems, built by the people with the most fiber-optic CRT recorder experience in the field.

To get the whole story on the VGR 4000 and how it can meet your needs, call Durke Johnson at 303/773-4700. Or write Honeywell Test Instruments Division, Box 5227, Denver, Colorado 80217.

WE'LL SHOW YOU A BETTER WAY.

Honeywell

HON-6-631

CIRCLE 45 ON INQUIRY CARD

Realtime System with Replay Capability Monitors Air Combat Exercises

Classically, air combat training has made use of simulated aerial dogfights, in which pilots maneuver to obtain positional advantages and to claim "kills." Prior to 1973, these kinds of exercises were limited in their effectiveness, since participants, training officers, and analysts had to depend on making educated guesses as to the outcomes of the simulated dogfights. However, since 1973, a computer controlled system has made it possible for viewers to obtain exact data on the relative motions of the participating aircraft, the trajectories of simulated weapons, and the occurrence of simulated hits or misses.

This still-evolving system, developed by Cubic Corp, 9333 Balboa Ave, San Diego, CA 92123, is designated as TACTS/ACMI. The term TACTS (Tactical Aircrew Combat Training System) is a designation specified by the Naval Air Systems Command, while ACMI (Air Combat Maneuvering Instrumentation) is specified by the U.S. Air Force. Both of these organizations are users of the system. Military bases where the system is utilized include Marine Corps Air Station, Yuma, Ariz; Nellis Air Force Base, Las Vegas, Nev; Naval Air Station, Oceana, Va; Tyndall Air Force Base, Fla; U.S. Air Force Europe, Sardinia, Italy; and Luke Air Force Base, Ariz.

Among the wide variety of combat aircraft that participate in the missions are the F4, F5, F14, F15, F16, F106, and A4. Prominent among the many weapons simulated are the Sidewinder (AIM-9L) and Sparrow (AIM-7F) air to air missiles.

Starting with Cubic's initial contract with the U.S. Navy in 1971, the TACTS/ACMI system has evolved through several stages. It is a system that allows training personnel to monitor the details of the combat training missions in real time and allows participating pilots to review the sequence of events subsequently in debriefing. The system depends to a large degree on visual CRT displays showing the details of the action. Four subsystems are involved: the airborne instrumentation subsystem (AIS), tracking instrumentation subsystem (TIS), control and computation subsystem (CCS), and display and debriefing subsystem (DDS). (See Fig 1.)

Airborne Instrumentation, Tracking, And Control and Computation

The AIS is mounted in a pod that, under training conditions, replaces a sidewinder air to air missile pod. Consisting of seven modules (see Figs 2 and 3), this airborne subsystem processes data descriptive of the state of motion of the aircraft and clocks the time of simulated weapon launch/firing.

(continued on page 79)

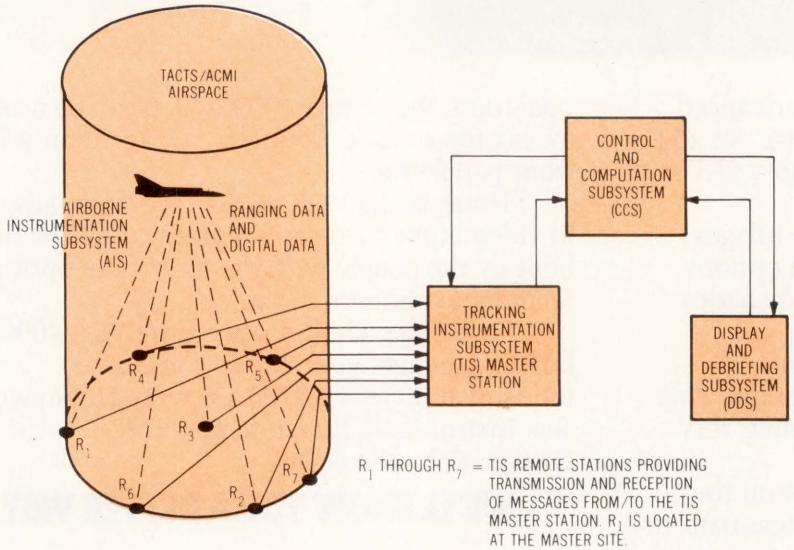


Fig 1 TACTS/ACMI system from Cubic Corp provides realtime and debriefing displays of aerial dogfight exercises. Seven remote stations track participating aircraft and receive data from airborne instrumentation. Data are processed successively at master tracking station and control and computation subsystem for use in display and debriefing subsystem

AND NOW SAMUX II!

Distributed I/O Control for the 80's from Opto 22

64 I/O Stations Per Host Computer

192 I/O Points Per Station

Simple Twisted Pair Communication To The Host and Station-to-Station

Digital and Analog I/O Modules

Efficient Protocol

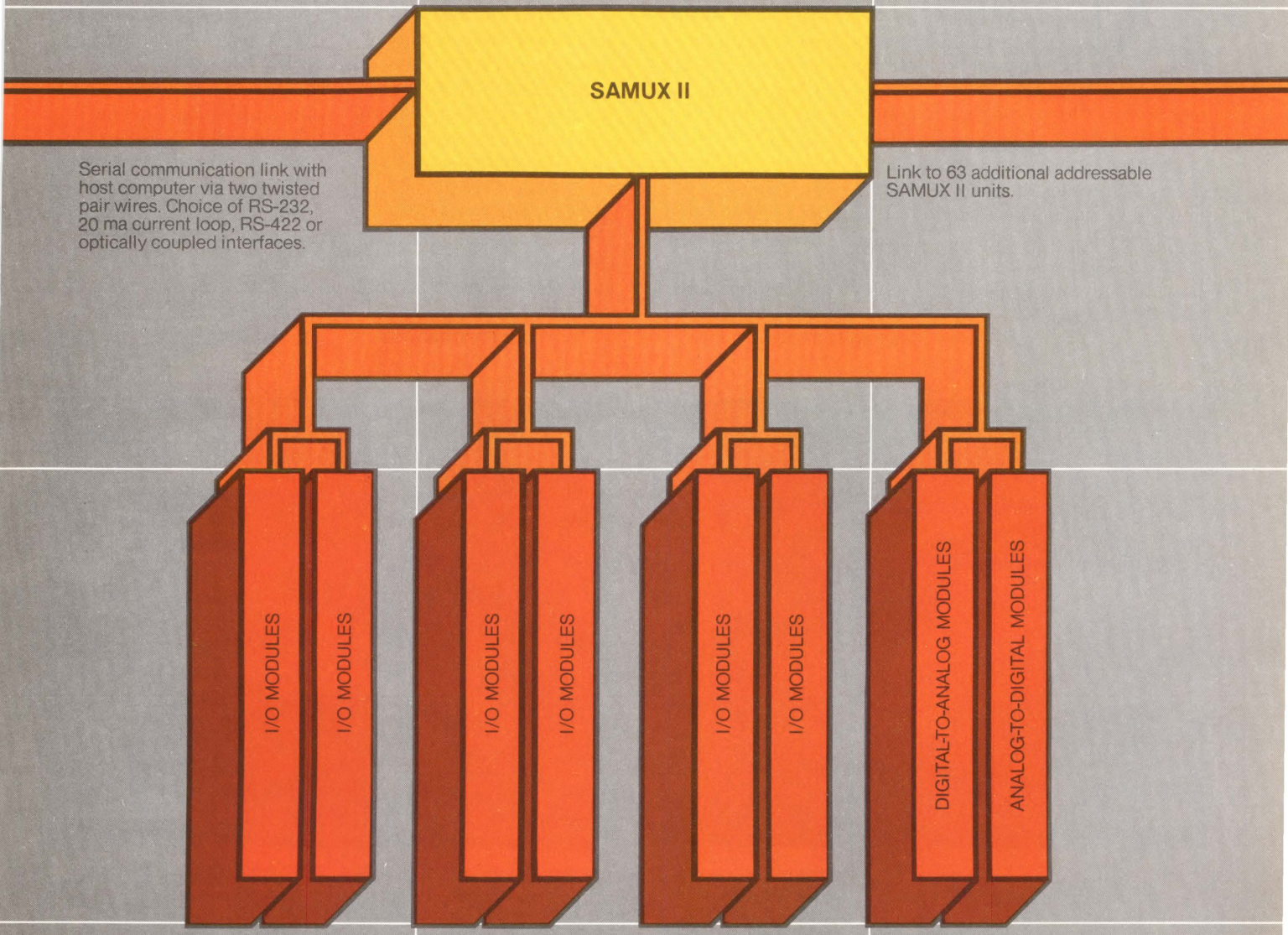
Versatile Command Set

Watchdog Timer

Latched Inputs and Time Delays

Extensive Communication Attachments

Isn't it what you expected from Opto 22?



Serial communication link with host computer via two twisted pair wires. Choice of RS-232, 20 ma current loop, RS-422 or optically coupled interfaces.

Link to 63 additional addressable SAMUX II units.

Modules per station range from 96 digital power I/O plus 48 analog to digital plus 8 digital to analog or up to 192 digital power I/O.

15461 Springdale St.
Huntington Beach,
CA 92649
(714) 891-5861
(800) 854-8851
Telex: 692386

opto 22

Distributed by Hamilton/Avnet

CIRCLE 46 ON INQUIRY CARD

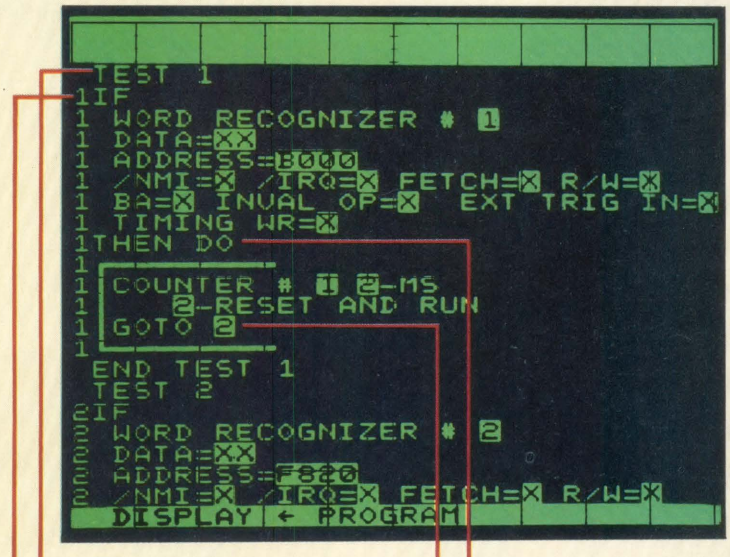
Tektronix' new 7D02. logic analyzer with the

Now, a total solution to problems encountered either on or off the bus. Tektronix' new 7D02 Logic Analyzer. Featuring a unique user language that reduces even the most complex testing to a few simple statements. You supply the overview and the 7D02 does all the detail work for you. With a sophistication never before possible.

A simple, yet sophisticated user language. Writing a test program is no more complicated than responding to a few simple prompts. A handful of basic phrases let you configure the 7D02's resources into almost any combination needed to solve the problem at hand. Often you'll find the 7D02 has an intelligence equal to the software you're integrating into your prototype.

Individualized 8- and 16-bit mnemonics. Through a series of personality modules, the 7D02 can adapt to the characteristics of specific microprocessors. Familiar mnemonics let you work faster and more accurately. Support today extends to the 6800, 6802, 8085, 8086, Z80 and Z8002 with more to come. There's also a personality module available for general purpose logic analysis.

Up to 52 channels of information. Flexibility is the key. You start with the basic 28 channels used for state acquisition, then the expansion option increases this to 44. For timing applications or wider state acquisition, there's an additional synchronous or asynchronous 8-channel timing option complete with its own memory, word recognizer and glitch trigger.

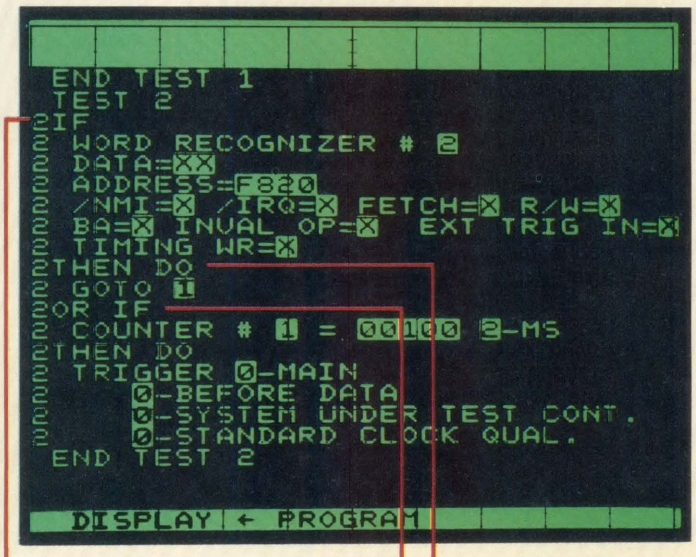


All test parameters supplied by prompts.

IF clause defines a data stream event, which may be either single or compound.

THEN clause defines a response to the event. In this case, setting counter #1 to zero and then incrementing every millisecond.

At the same time the counter is set, branch to the second test. (bracketing allows simultaneous actions).



The 7D02 now monitors the data stream for an event to satisfy the second test's IF clause.

If the event occurs, then branch back to the first test and start the program over.

Or if counter #1 has reached 100 mS, then activate the trigger.

7D02 LOGIC ANALYZER

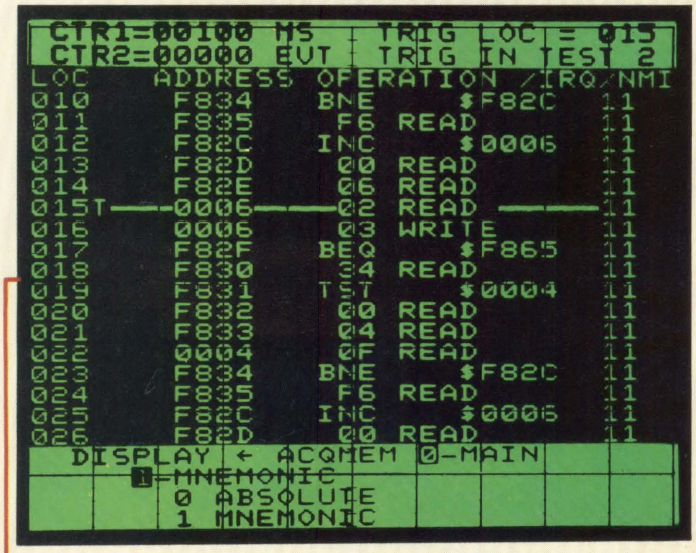
A user-programmable smartest triggering ever.

And there's more. The 7D02's user language takes advantage of four separate word recognizers, each up to 48 bits wide. Plus two counters usable in either the time or event mode. In addition to clock qualifications, there are two types of data qualification to provide selective data storage.

The Tektronix 7D02 Logic Analyzer can give you a whole new approach to μP-based design.

Locating an intermittent fault. The following program gives a limited demonstration of the simplicity and power behind the 7D02's user language. Here the object is to trigger when a second event on the bus does not occur within 100 mS of a first event.

The 7D02 is a 3-wide plug-in for the popular Tektronix 7000 Series oscilloscope. Shown above is a Tek 7603 mainframe housing the 7D02 logic analyzer with a personality module supporting the 6802 microprocessor.



By using the proper personality module, software flow can be displayed using the mnemonics of the chip under test, here the Motorola MC6802.

Tektronix®
COMMITTED TO EXCELLENCE

For immediate action, dial our toll free automatic answering service 1-800-547-1512.

For the address of your nearest Tektronix Field Office, contact:

U.S.A., Asia, Australia, Central & South America, Japan Tektronix, Inc., P.O. Box 1700, Beaverton, OR 97075, Phone: 800/547-1512. Oregon only 800/644-9051, 503/644-0161, Telex: 910-467-8708, Cable: TEKTRONIX

Europe, Africa, Middle East Tektronix International, Inc., European Marketing Centre, Postbox 827, 1180 AV Amstelveen, The Netherlands, Telex: 18312

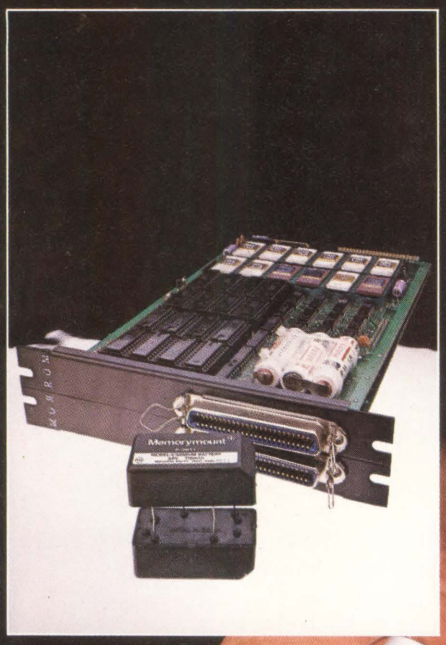
Canada Tektronix Canada Inc., P.O. Box 6500, Barrie, Ontario L4M 4V3, Phone 705/737-2700

How to improve your memory.

Worried about your product's volatile memory? Don't forget about Panasonic. Our reliable Memory-Mount™ Batteries are pin-compatible with PC-board mounts, and we offer an extensive selection of types, sizes and voltages to cover most every electronic memory support requirement.

For long-life CMOS biasing, our Memory-Mount Lithium primary batteries can keep a binary circuit energized for years. They operate in wide range of temperatures, and are designed for minimal shelf life loss (shelf life tests indicate up to 95% of original capacity after five years in some cases). Their stable, hermetically-sealed package does not generate gas or corrosives, and our Memory-Mount types are unaffected by flow soldering (available plug-in socket accepts our coin-type Lithiums for wave soldering).

For rechargeable secondary battery applications, Panasonic Nickel-Cadmium Memory-Mount batteries offer close capacity/voltage characteristics, up to 1,000 charge/discharge cycle capability, and they're factory-tested for uniformity. All Memory-Mount Nickel-Cadmiums can be delivered in discharged state, to allow flow soldering onto PC boards before charging.



Our Mercury Memory-Mount batteries combine the advantages of miniaturization with large electrical capacity and very stable working voltage. Available in both cylinder and button types, they operate in a wide range of temperatures and offer long storage life.

Most of these PCB pin-compatible batteries are also available with standard tab connections. And Panasonic can provide larger battery systems, including sealed lead-acid, for computer program transfer, hold-memory storage or orderly shutdown of computers and process controllers. For complete information, contact Panasonic Company, OEM Battery Dept., One Panasonic Way, Secaucus, NJ 07094; (201) 348-7277 or 348-7278.

Panasonic Memory-Mount™ Batteries, your reliable memory support source.

Shown: a selection of Panasonic Lithium, Nickel-Cadmium and Mercury coin-type and Memory-Mount batteries.

Panasonic®
just slightly ahead of our time

CIRCLE 47 ON INQUIRY CARD

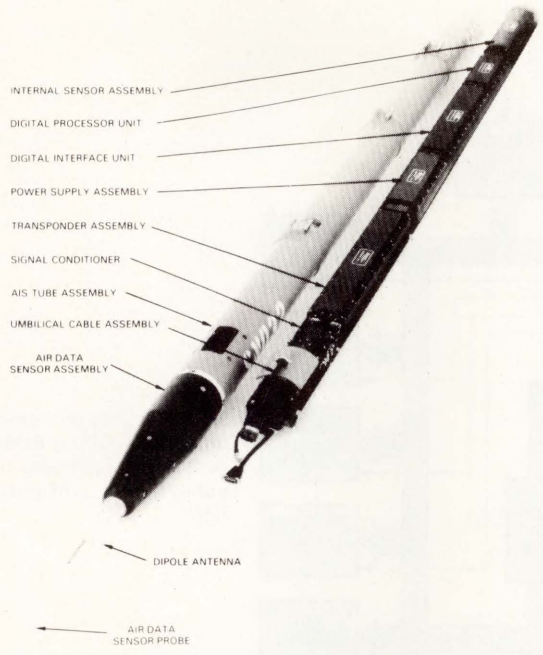


Fig 2 P-4 AIS. Subsystem is housed in pod that, in training, replaces sidewinder missile pod

Microprocessors are located in two of the seven AIS modules. One microprocessor is in the digital processor unit (Fig 4), where it integrates acceleration and angular rate data fed to it by the inertial sensor assembly, obtaining velocity vector and position as well as heading, pitch, and roll angles. It then transforms all kinematic data into an earth-coordinate frame of reference.

A second microprocessor is located in the digital interface unit. This processor acts as a communications front end, interfacing between the first (kinematic) processor and the transponder.

In an early version of the P4 pod, these two microprocessors are 8080s, but, in the more advanced P4S pod, 8085s are used. A third 8085 is present (in the digital interface module of the advanced pod) for interfacing to the serial data bus onboard the aircraft. This data bus has thus far been implemented only on the F16 and F18 aircraft, and, therefore, the P4S is initially being used only with them, although eventual upgrading will include other craft.

Kinematic data transmitted from the AIS are received at TIS tracking stations, which are the second of the four subsystems. The TIS normally consists of seven remote stations and one master station. At remote stations, 8085 microprocessors act as communications controllers, providing diagnostics, timing and sequencing, and data formatting, and responding to specific condition indicators,

(continued on page 80)

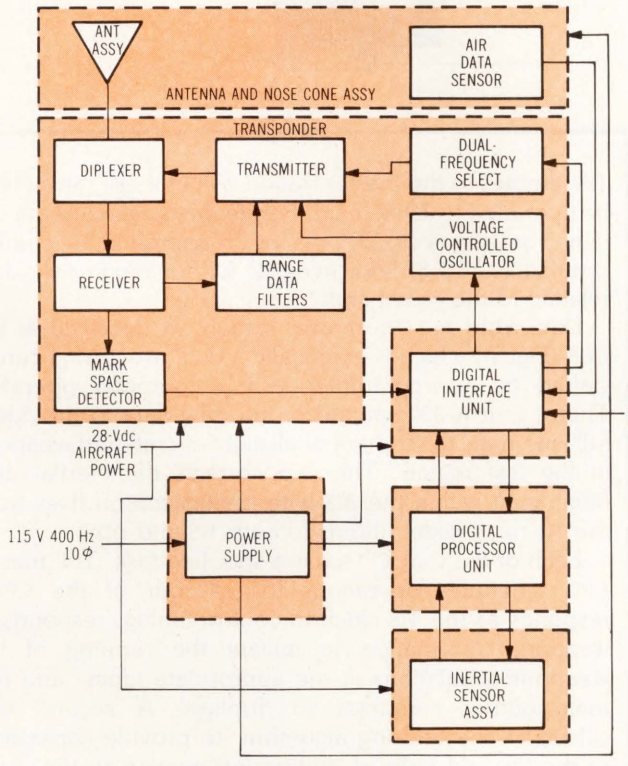


Fig 3 Block diagram of AIS. Digital processor unit operates on inputs from inertial sensor assembly to obtain aircraft stat of motion. This information and weapon simulation data proceed via digital interface unit to transponder for relay to tracking stations

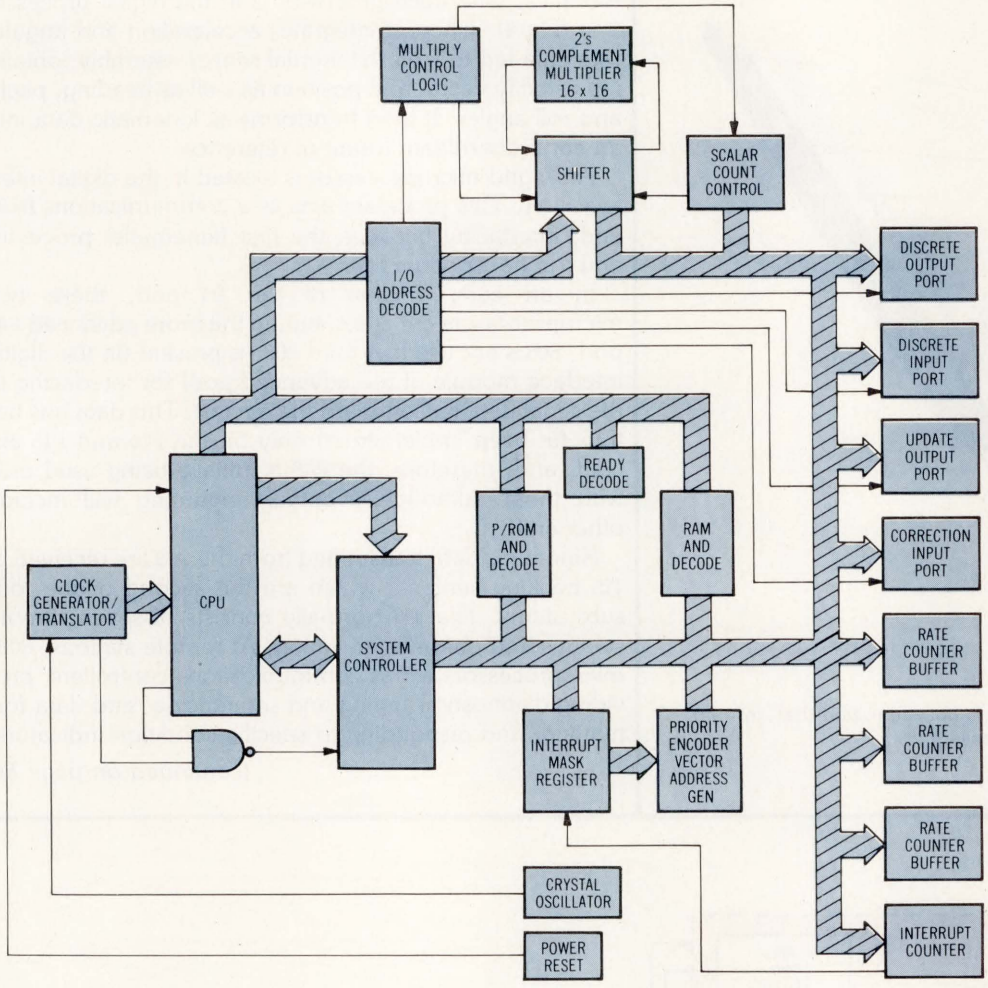


Fig 4 Digital processor unit of AIS. CPU is 8080 or 8085, depending on subsystem configuration

such as alarms. Data from these remote stations are transmitted to the manned TIS master station, where additional data communications control is carried out. Since all of the remote stations can track all of the participating aircraft, one of the tasks of the master station is to select optimum station/aircraft pairings for acquisition of data from the aircraft and retransmission to the CCS subsystem.

A Perkin-Elmer Interdata 8/32 minicomputer handles the processing requirements at the TIS master station. This situation is to be modified with the introduction of an unmanned TIS master station, in which processing will be conducted by 8086s.

The TIS provides continuous, simultaneous identification and tracking of the 8 combat planes in all attitudes, as well as the capability to track 12 additional escort aircraft by position only. (Upgrading will allow tracking of 16 combat planes plus 24 escorts.) Uplink capabilities provide for the transmission of correction signals to the onboard inertial reference unit in the AIS, while the downlink transmits all inertial and mission dependent information from the AIS. Data rates are 62k baud for ground to air, air to ground, and transmission from the TIS remotes to the master station. All of these rates are to be upgraded to 198k baud. Range measurements are obtained at least every 200 ms for the aircraft in the combat simulation and at least every 2.4 s for range-only data relating to the escort craft.

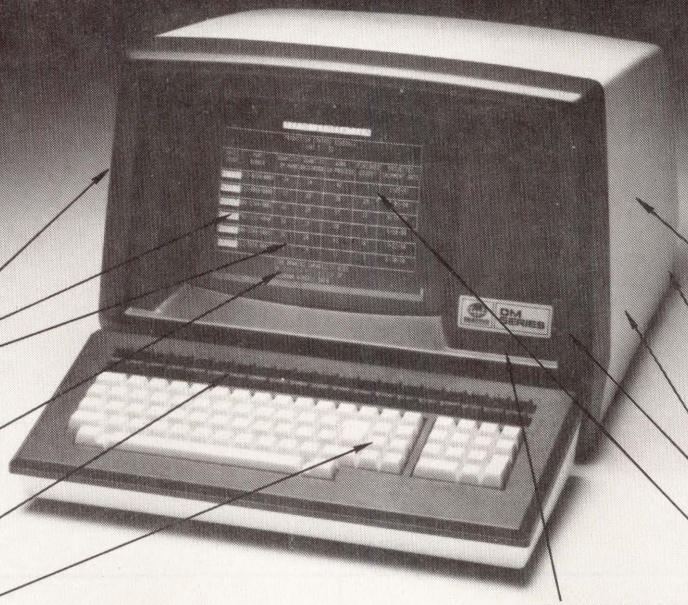
Data from the TIS master station are received at the CCS (Fig 5), which is essentially a data processing center staffed by a programmer and a computer operator. There, four 8/32s operate on the raw data to provide a full kinematic description of all eight aircraft and weapons in the test region. The CCS corrects the inertial data originating within the AIS with multilateration fixes from the TIS to provide outputs to both TIS and DDS.

Each of the four CPUs has a specified task. The master CPU schedules operations for all four of the CPUs, responds to the TIS clock to control timing, responds to weapons information to initiate the running of the weapons simulations at the appropriate times, and formats output messages to displays. A second CPU calculates the tracking algorithm (to provide corrections to the TIS and state of motion information to the DDS), and the remaining two CPUs provide the logic for the

(continued on page 82)

OEM terminals for the future...TODAY

The industry standard, smart DM terminals from Beehive



YOUR COLOR AS STATED

M-LOCK (SPLIT-SCREEN)

P4 or P42 AS NEEDED

MULTIPLE VISUAL ATTRIBUTES PER YOUR SPECIFICATIONS

FUNCTION KEYS AS REQUIRED

SPECIAL KEYS FOR YOUR APPLICATION

RAM/ROM TO MEET APPLICATION REQUIREMENTS

PRINTER/AUX PORT IF REQUIRED

SYNCHRONOUS or ASYNCHRONOUS I/O AS DESIRED

SELF DIAGNOSIS

LINE DRAWING CAPABILITY

EDITING FEATURES/ MULTIPLE PAGES

A terminal whose parameters can change with your requirements!

Now available with attractive discounts

Call for applications assistance and delivery

TOLL FREE USA **(800) 453-9454**

CALIFORNIA Costa Mesa *(714) 540-8404* • Sunnyvale *(408) 738-1560*
FLORIDA Altamonte Springs *(305) 830-4666* **ILLINOIS** Arlington Heights *(312) 593-1565*
MASSACHUSETTS Woburn *(617) 933-0202* **NEW YORK** New York *(212) 682-2760* **UTAH** Salt Lake City *(801) 355-6000*
WASHINGTON, D.C. (VA) Falls Church *(703) 356-5133*
EUROPE The Netherlands *Phone 020-451522*

BEEHIVE INTERNATIONAL

"A proven competitive manufacturer of smart terminals"

CIRCLE 48 ON INQUIRY CARD

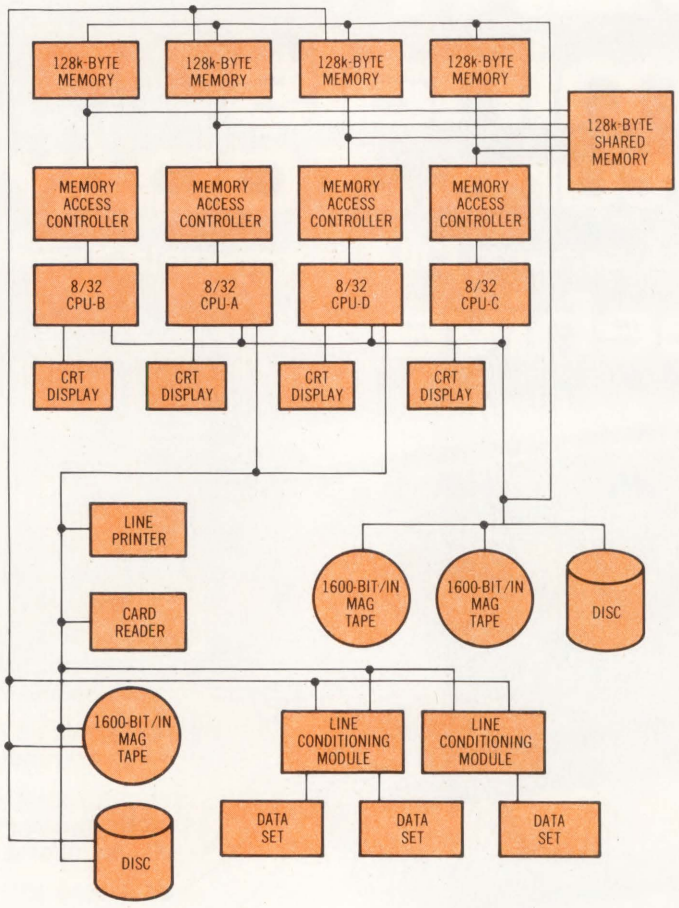


Fig 5 CCS utilizes four central processing units. Specific tasks such as tracking algorithm, weapon simulation, and timing/control are assigned to specific CPUs

weapon simulations. Weapon trajectories are simulated as a function of initial firing time, the velocity vector of the firing aircraft, and calculated tracking and homing inputs based on the updated location of the target relative to the weapon.

The four CPUs share 128k bytes of core memory, and each also has its own dedicated core memory of 128k or 256k bytes. Peripherals in the subsystem include a line printer, card reader, CRT displays, magnetic tape drives, and two disc drives.

Display and Debriefing

Located in a van or building, the DDS uses an Adage GS330 display controller to operate a strokewriter CRT and color projection displays. Each of two consoles in the trailer provides a pair of 21″ (53-cm) display screens. Typically, one screen on each console shows a graphics simulation of the aircraft that are engaged in the combat exercise, while the second screen displays tabular data relating to the performance of the eight aircraft and interactions between aircraft pairs (Fig 6).

Various graphics displays are possible. One of these, a plan view of the test range, can be set to show a square area either 40 or 100 nautical miles (74 or 185 km) on a side, including not only the aerial region within that

(continued on page 86)

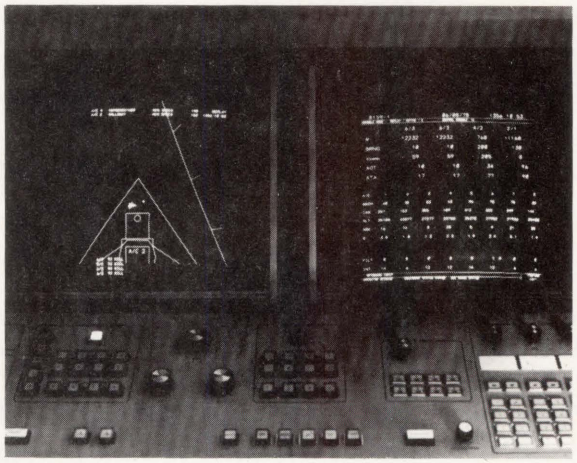
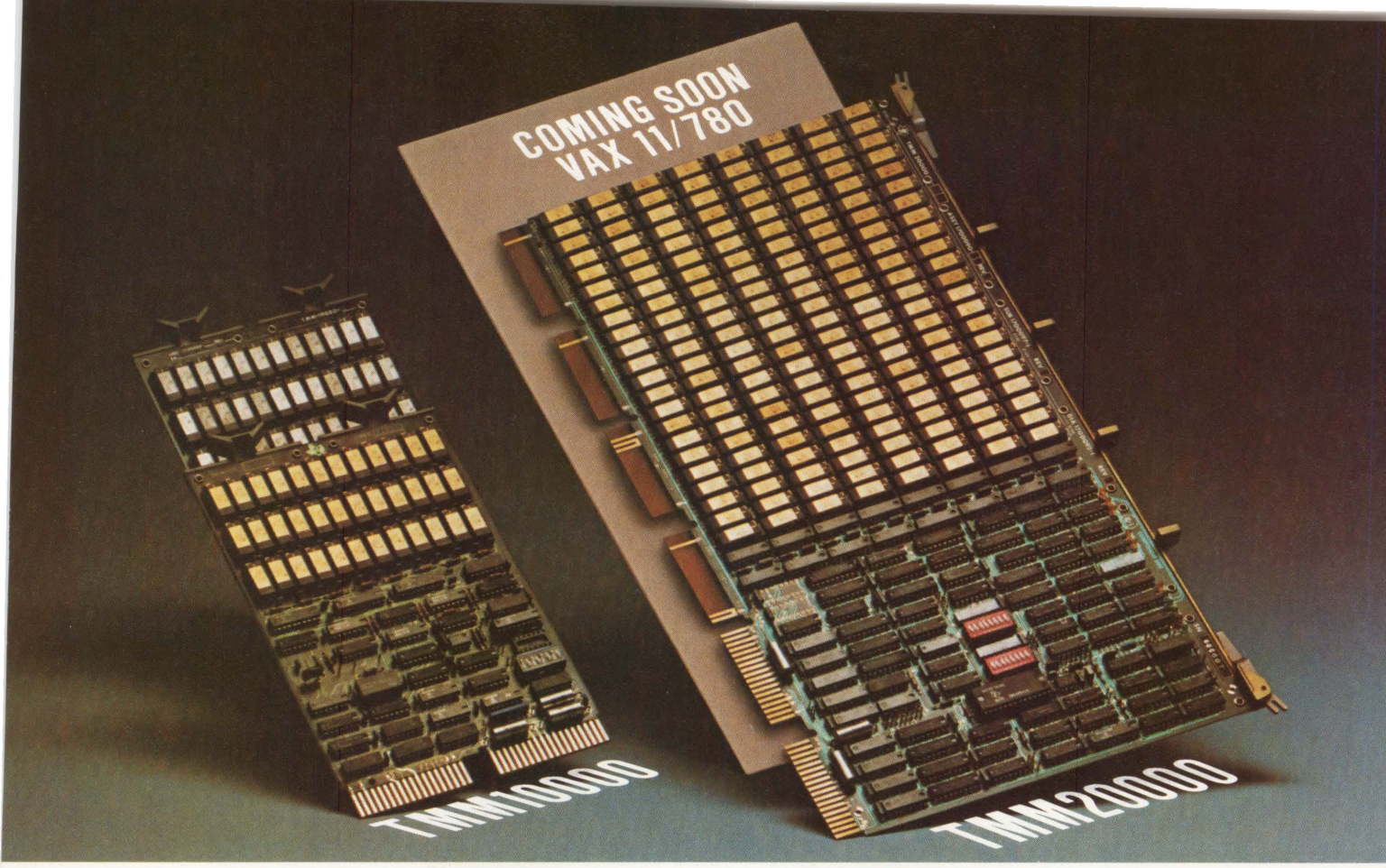


Fig 6 DDS console. On left screen is F-106 cockpit view of second aircraft. Right screen lists relative locations and velocities of aircraft pairs, right-hand column (for example) indicating aircraft #1 in coordinate system of aircraft #2, as shown by 2/1 column head. Lower part of right screen lists parameters relating to eight participating aircraft



New 96K word module. LSI-11/23 compatible. TI's growing memory systems family.

Quality. Reliability. Compatibility. And a new addition to our TMM10000 Series as the TI memory systems family keeps growing.

TMM10000 Series

- 64K words or new 96K words
- Optional parity
- Standard "dual" DEC board
- Low power

TMM20000 Series

- 256K word/128K word high-density versions
- Error detection/correction enhances system reliability
- Error correction transparent to operating system
- Fully compatible with PDP-11/34 and the recently announced PDP-11/44 UNIBUS+ computers
- Addressing capability to two megawords
- Low power
- Programming options: Modified or extended UNIBUS, I/0 page size, control status register address location and error status register.

All TI-designed add-in memory systems employ state-of-the-art 5-V MOS dynamic RAM technology.

Custom capability

If you need custom memory systems in production quantities, be sure and talk to TI. We'll custom-design modules for specific applications with the same meticulous attention to cost-effectiveness that our standard modules offer.

For immediate delivery from stock, call Integrated Memory Systems at (713) 490-3746, your nearest semiconductor distributor or TI field sales office. Or, send us the coupon for more information.

Texas Instruments Incorporated
Semiconductor Group
P.O. Box 1443, M/S 6958
Houston, Texas 77001

Before I order, I'd like to know more about:

☐ TMM10000 modules ☐ TMM20000 modules ☐ Custom memory modules

Name_____

Company_____

Address_____

City_____ State_____ Zip_____

TEXAS INSTRUMENTS
INCORPORATED

+ Trademark Digital Equipment Corp.

85214A

CIRCLE 49 ON INQUIRY CARD

Introducing the Intellec® Series III. The system for designers who want the technological heights.

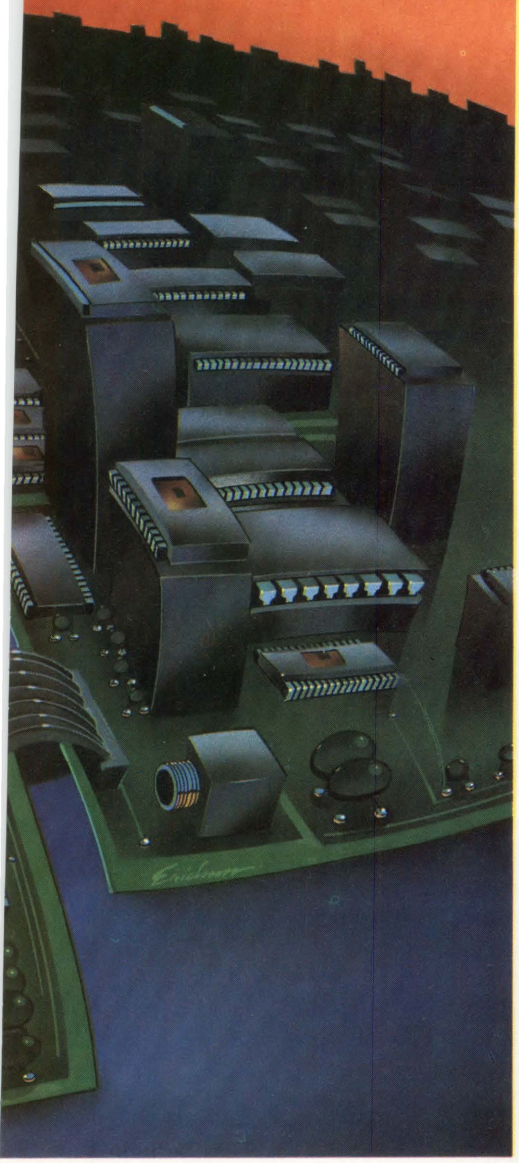
Only Intel offers both state-of-the-art microprocessors like the iAPX 86, iAPX 88 and 8051, plus development systems like our new Series III, that let you reach new highs in performance.

To reach the top of the VLSI design world, it takes technologically advanced products. The iAPX 86, the industry's highest performance 16-bit microsystem. The iAPX 88, the industry's 8-bit price-performance champion. The 8051, the industry's most powerful single-chip microcontroller. And the industry's only development system that fully supports the newest technology: the Intellec® Series III.

Get versatility *and* performance in one development system

Series III is the only development system that supports design efforts varying from signal processors, through universal peripheral interfaces and 8-bit microprocessors, to powerful, 16-bit microsystems. And does it all at either the component or single-board-microcomputer level. That's because the Series III's dual processor (8085, 8086) architecture always provides the right level of functionality for any development project. Plus, the Series III's one megabyte address space and 7.5 megabyte hard disk capacity allow you to increase compilation throughput by a factor of 5—compared to previous Intellec systems—while accommodating unusually large, stand-alone development projects.

Intellec® Series III Development System



development challenge of

Prepare now for future growth

The new Series III represents the latest —and highest—performer in Intel's line of planned development solutions. This line includes the Series II, for 8-bit development projects, and the new, *low-cost* Model 120 for smaller 8-bit projects that require an entry level development system. These systems provide a natural upgrade path for stand-alone development efforts.

For large, multi-user projects, Intel offers a second upgrade path: the new NDS-1 network development system. With NDS-1, all Intellec stand-alone models can be tied into a distributed development configuration. NDS-1 supports up to 15 megabytes of disk storage, and provides resource sharing for up to eight Intellec systems. So now you have the flexibility to use any of the Intellec system technologies in projects ranging from small, stand-alone efforts, to large, complex systems.

Get the broadest range of languages and in-circuit emulators

To shorten development cycles and get your products to market sooner, Intellec systems provide the broadest range of design/development tools in the industry. High-level programming languages, such as Pascal, our block-structured application language; PL/M, our systems implementation language; and our ANSI-compatible FORTRAN. Plus macroassemblers for every programmable Intel device. ICE™ in-circuit emulators, available at *the same time* a new Intel device is available. A worldwide training network. On-site training programs. Field maintenance, including a toll-free hotline. Plus the largest staff of field applications engineers in the semiconductor business.

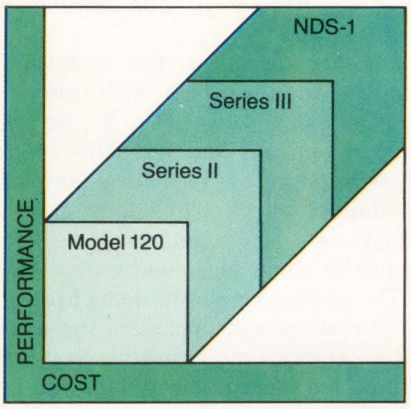
That's our full spectrum of development system solutions. And only Intel offers it.

TYPE	CPU	SUPPORT
ANALOG	2920	2920 Assembler High-Level Compiler Simulator
SINGLE-CHIP	8048, 8049	ASM48, ICE49™ Multi-ICE™
	8022	ASM48, ICE49™
	8041A	ASM48, ICE41A™ Multi-ICE™
8-BIT	8080, 8085	ASM80, PL/M Pascal, FORTRAN COBOL, BASIC ICE80™/ICE85™ Multi-ICE™
	iAPX 88	ASM88, PL/M Pascal, FORTRAN ICE88™
16-BIT	iAPX 86	ASM86, PL/M Pascal, FORTRAN ICE86™ ICE86/88™ Extensions ASM89 Real Time Breakpoint Facility (RBF)
	iAPX 86/20, iAPX 88/20 (numeric data processor)	
	iAPX 86/11, iAPX 88/11 (with 8089 I/O processor)	

Intel's Total Hardware/Software Support

Protect your development system investment

All Intellec systems delivered since 1975 can be upgraded to the latest development system technology. And they'll continue to be upgradable in the future. That's because Intellec systems are planned as a progression of products that keep pace with rapid microcomputer advances. Thus Intellec systems enable you to be first in using the latest technology. More importantly, they protect your development system investment. That's critical, both now and in the future, because today's Intellec systems will support the next generation of microprocessors: the iAPX 186 and iAPX 286. And allow you to transfer design skills from one generation of products to another, cutting down on retraining time and costs.



Intellec® Upgrade Path to Investment Protection

All of which comes down to this: Only Intel offers *both* state-of-the-art advances in microprocessors *and* the upgradable development systems to support them. They go hand in hand. So, when you're considering the problems of technology change, varying levels of project complexity, and system upgradability, remember: Intel delivers *complete* development system solutions. And only Intel.

For further information, contact your local Intel sales office/distributor, or return the coupon to Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

☐ Please send me more information on Intellec® Development Systems.
☐ I have an Intellec system. Please send upgrade information.

Processor(s) being used: _____

Language(s) being used: _____

No. of planned programmer workstations: _____

Name _____

Title/Organization _____

Address _____

City/State/Zip _____

☐ I have an immediate requirement. Please telephone me at:

( ) _____

CD1

Europe: Intel International, Brussels, Belgium.
Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A.Varah, Wyle Distribution Group, Zentronics.

intel® delivers solutions

perimeter, but also ground features including 3-dimensional contours of prominent hills or mountains on the range. Aircraft participating within the region appear as simplified shapes with attitudes, velocities, and locations relative to one another and to the range represented.

Another display is the centroid, in which a cube-shaped region is shown, measuring 2.5, 5, 10, 20, or 40 nautical miles (4.6, 9, 19, 37, or 74 km) on a side. Initially, this cube is centered at the centroid of a selected set of participating aircraft. For example, the centroid could be that of all participating aircraft, a selected pair or triplet, or a single aircraft (in which case, the centroid would be identical to the location of the specified craft).

The centroid point remains fixed in its initial position, so that all aircraft (including those used to calculate the initial centroid) move relative to this fixed point. In other words, the fixed point remains the centroid of the initial configuration, not the centroid of the updated configurations. The entire display can be rotated about an axis through the centroid. This rotation can occur about the local vertical or about a horizontal axis normal to the viewer's line of sight as he faces the display. By combining these rotations, the viewer can see the cubic region in any orientation.

Symbols (Xs) on the terrain part of the centroid display indicate the normal projections of aircraft locations onto the ground. As the cube is rotated into a plan view, these Xs fall directly below the pictorial representations of the aircraft and are no longer visible. For this situation, with tilt angle equal to 0, the centroid display becomes identical to the plan view display, except possibly for scale.

The recent path of each aircraft is indicated as a solid curve representing the locus of the left wingtip and a dashed curve representing the locus of the right wingtip. Other symbols shown in the display include dashed-line trajectories of weapons and a box symbol surrounding an aircraft that has suffered a simulated hit by a weapon.

A third mode of display (Fig 7) presents the view from the cockpit of a selected aircraft. This mode places the viewer inside the cockpit, presenting outlines of the canopy and of aircraft in the field of view. The viewed aircraft will move relative to the canopy outlines, as a function of the relative motions of the viewed and viewing aircraft.

In all modes, aircraft and weapon locations, attitudes, and states of motion are updated on the display every 100 ms. When direct communication between an aircraft and tracking station is not possible, update is based on extrapolation rather than on newly received data. Displays are not stored in memory but are based on calculations from the raw kinematic data. Therefore, upon replay, any of the display modes and parameters can be selected. Hard copies of displays are available through a printer peripheral.

Typically, two consoles are provided in the DDS station, one used by blue team members, the other by red. Each team is able to select displays independently. By delivering verbal feedback to the pilots via uhf voice radio, trainers or trainees at the console can participate in the tactics of the simulation.

For debriefing purposes, a pair of large display screens [4′ (1.2 m) square] on a wall duplicates the displays on the 21″ (53-cm) screens of one of the consoles, adding color such as blue and red aircraft symbols as programmed. These large displays make it possible for viewers in a small theater to watch the details of the simulation.

An upgrade of the existing system will make it possible for a ground controller, operating at the console, to fly a drone, which would be attacked by aircraft mounting live weaponry. The updated location and orientation of the drone would appear on the display, as would the graphical symbols of the aircraft. Placement of the drone's intelligence in the DDS station rather than in the drone offers significant savings by reducing target expenditure.

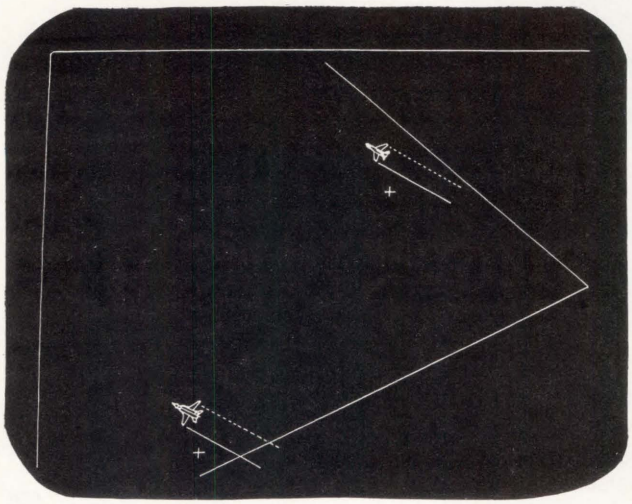


Fig 7 CRT display utilizing 5-nautical mile (9-km) centroid view shows Navy F-14 Tomcat (lower left) and A-7 Corsair II about to engage in air combat exercise. Solid trail indicates recent path of left wing tip, dashed trail of right

Summary

Combining instrumentation, data communications, display, and control capabilities, the realtime system brings an activity previously subject to limited observation into an exact, accessible format. A significant attribute of this system is its turnkey capability, allowing military pilots without special computer training to operate it after only a few hours of familiarization. The safety and effectiveness of air combat training has been greatly enhanced, with significant cost reductions, in an operation that offers insights that were essentially out of reach in previous approaches.

17+ MEGABYTE DISK BACKUP

DEI COMPATIBLE CARTRIDGE TAPE DRIVE

The Model 400 MAXIDRIVE™ packs 17.2 megabytes on a single data cartridge and is loaded with advanced features. Unique, hard mounted motor. Rugged transport mechanism. Excellent power dissipation. High, 6400 bpi density. Fast, 192,000 bps transfer rate. Four-track, read-after-write dual-gap head, with selective erase. Solid state BOT/EOT detection. Plug-in electronics. Plus more.

Contact us today for complete details —

For more information please call 800-645-5292

Qantex

Division of
North Atlantic Industries
60 Plant Avenue, Hauppauge, NY 11787
(516) 582-6060 TWX 510-227-9660

CIRCLE 51 ON INQUIRY CARD

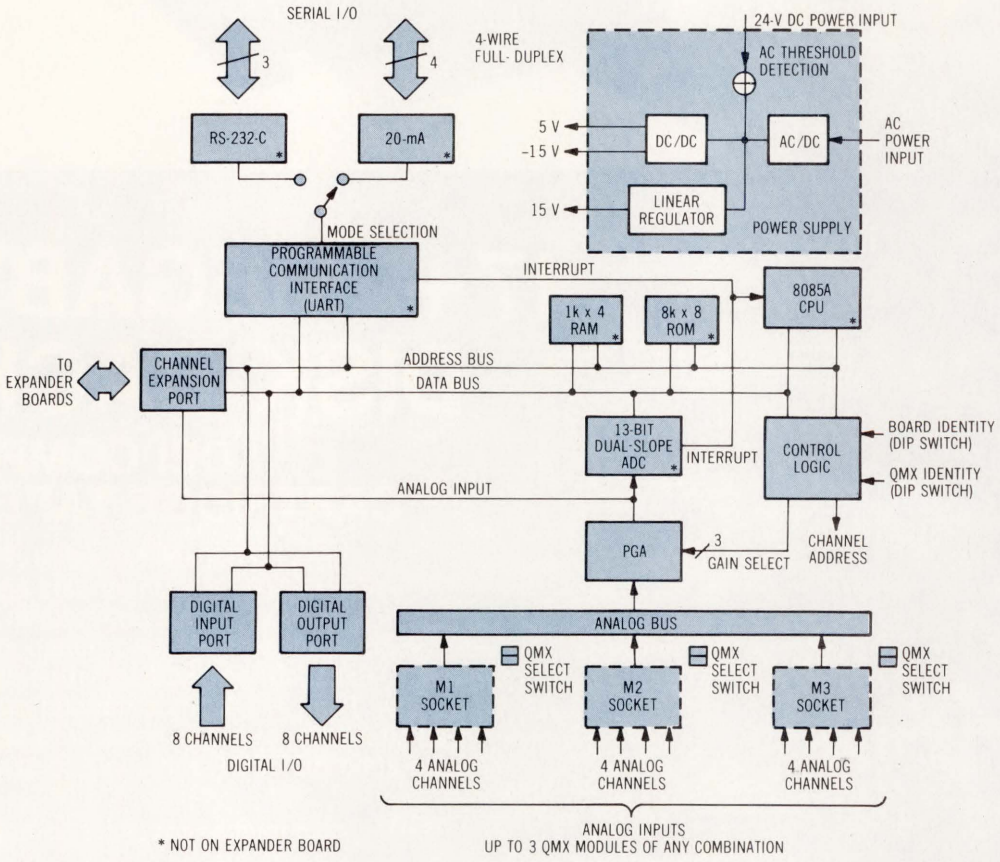
Single Board Contains Full Intelligent Measurement and Control System

Sensor signal conditioning, analog multiplexing, analog to digital conversion, digital input/output ports, power supply, and serial communications link to the host computer are all included on the single printed circuit board μMAC-4000 intelligent measurement and control system. One precalibrated master board accepts 4, 8, or 12 analog input channels; three expander boards can be added to form a cluster with a total of 48 channels; and up to 384 channels can be provided in a multicluster configuration. An onboard microcomputer scales, linearizes, and converts input data to engineering units; stores the results in random access memory; and then updates the stored data at a rate of 15 or 30 channels/s—unburdening the host of these duties.

Any computer or terminal that has a 20-mA or RS-232-C port can serve as host, with the control system used either as a local front end in the control room or remotely at a distance of up to 10k ft (3 km). Control is maintained by a command set in firmware via a serial interface bus. When commands are executed, results are sent to the host in ASCII format at speeds up to 9600 baud.

The manufacturer, Analog Devices, Inc, Rte 1 Industrial Park, Norwood, MA 02062, has introduced the microcomputer based μMAC-4000 for industrial and laboratory applications, and particularly for the factory environment in which small clusters of sensor I/O must be measured and controlled. Input protection of 130 Vrms, high channel to channel and input to output isolation common mode voltage isolation of ± 1000 Vac,

(continued on page 91)



μMAC-4000 masterboard block diagram. Input data are linearized, converted to engineering units, stored in RAM, and continuously updated by CPU. Full-duplex UART, which receives and transmits data at serial I/O port, is jumper selectable for either RS-232-C or 4-wire TTY 2-mA current loop operation. Expander boards, which increase number of available channels, contain same components as master board except for actual control and communications interface devices

Plug in to CRDS for complete LSI-11® systems

LSI-11/23 systems 30 days! a.r.o.

Software

Your choice of:

- **RT-11**
- **RSX-11M**
- **U/V6 (UNIX*)**

MF-211/411

- **LSI-11/2 with 32K words or LSI-11/23 with 64K, 96K or 128K words**
- **RX02 Equivalent Dual Floppy Systems, Single-Sided or Double-Sided, Dual Density**
- **Quad Serial Interface**
- **8 Quad Slot Backplane**

HD-11/HD-11T

- **Shugart Winchester Drive with 21 Megabyte Capacity, Software Equivalent to Four RL01's**
- **DEI Cartridge Tape Back-up (HD-11T)**
- **Controller Card with RL01 Instruction Set Compatibility**

When you plug in to Charles River Data Systems you plug in to innovative, practical solutions to your system design requirements. Solutions like our double-sided, double-density floppy disk systems—offering one megabyte of RX02 equivalent storage per drive. Or our Winchester drive with cartridge tape back-up for fail-safe reliability—in a single enclosure, with a common controller card.

You can purchase each of our compact, reliable components separately to expand or complete a system. Or combine them in your choice of configurations for powerful, multi-user, general purpose computers in a single, cost-effective package.

Equally at home as R & D systems or as the basis for business and process control systems, CRDS systems are based on the DEC LSI-11/2 or LSI-11/23, with from 32K to 128K words of MOS memory. Peripherals available include a 21 megabyte Winchester fixed disk system; single- or double-sided floppy disk drives; and a 3M cartridge tape back-up for the Winchester disk. Software systems available include RT-11, RSX-11, and U/V6 (UNIX*).

Whichever configuration you choose, you're assured of plugging in your system fast, because CRDS delivers most products in *30 days!*

For complete specifications, and to discuss the configuration or components that best meet your needs, call CRDS Marketing at (617) 655-1800. And plug in to CRDS *today.*

®Trademark of Digital Equipment Corporation.

**UNIX is a registered trademark of Bell Laboratories.*

CRDS

Charles River Data Systems, Inc.

4 Tech Circle, Natick, MA 01760 • Tel. (617)655-1800 • TWX (710)386-0523

CIRCLE 52 ON INQUIRY CARD

Short, But Not On Features.

Good things come in low profile packages.

Including tactile feedback, force hysteresis, .125″ total travel, .055″ overtravel, and many other human factor advantages normally associated with only standard-size keyswitches.

Datanetics low profile DC-60 keyswitches stand tall on quality and reliability. Sizes range from .770″ for the −01 version to .980″ for the −05 version when measured from the P.C.B. to top of the keycap. Trifurcated gold-inlayed stainless steel contacts provide the long life needed for quality terminal applications.

And the options are as long as your arm. The DC-60 is the answer to the height requirements associated with the new European regulations.

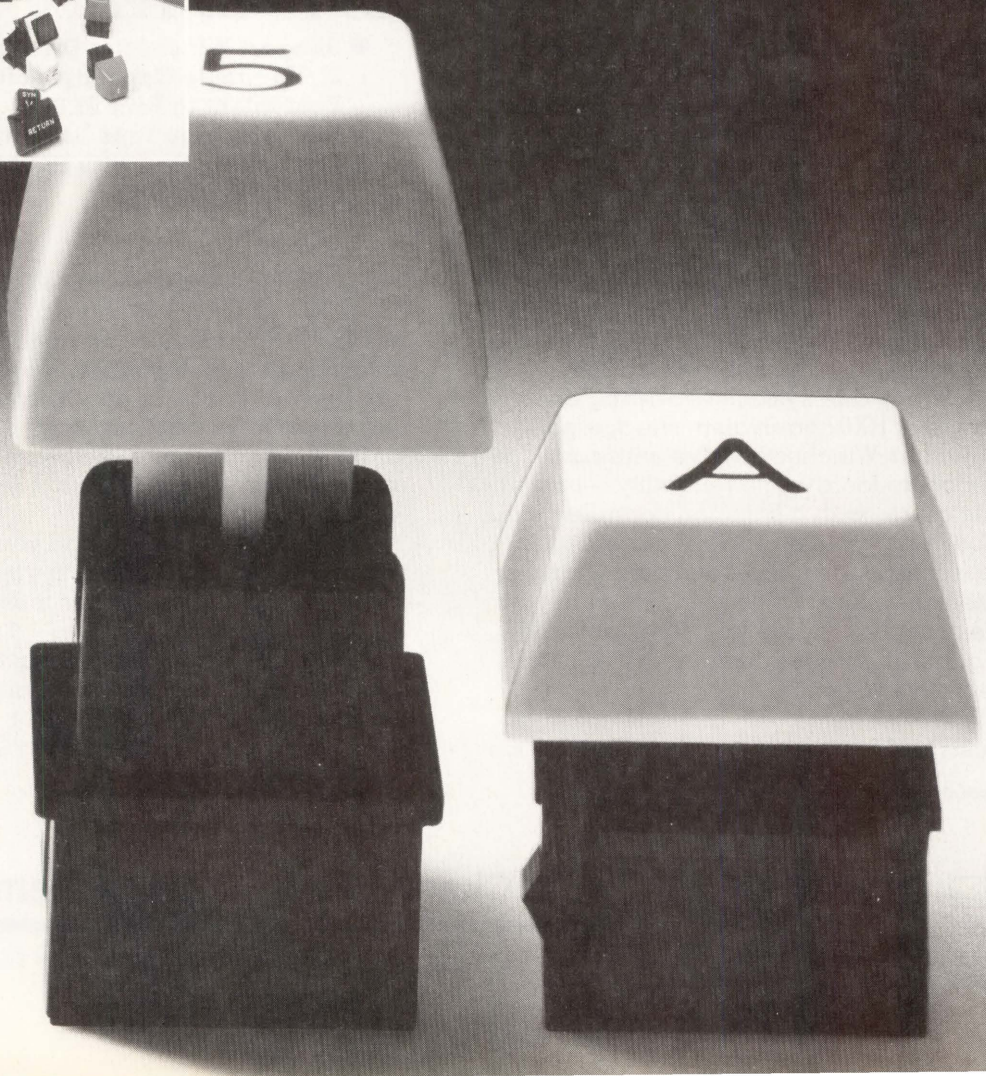
In short, they're big favorites with the world's major calculator, business machine and computer peripheral companies.

Call us today for the lowdown on low priced, low profile DC-60 keyswitches. And put quality at your customers' fingertips.

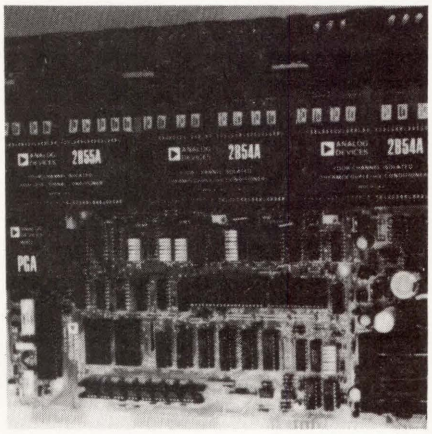
ITT Datanetics Corporation
A Subsidiary of ITT

10840 Talbert Avenue
Fountain Valley, CA 92708
Phone: (714) 549-1191
TWX: 910-596-1301

CIRCLE 53 ON INQUIRY CARD



high common mode rejection of 160 dB, normal mode rejection of 86 dB, low drift amplification, and rfi/emi immunity ensure performance. A high accuracy programmable gain amplifier and a 13-bit integrating ADC preserve signal integrity. Selection of standard signal conditioning modules enables direct connection to a wide range of sensors.

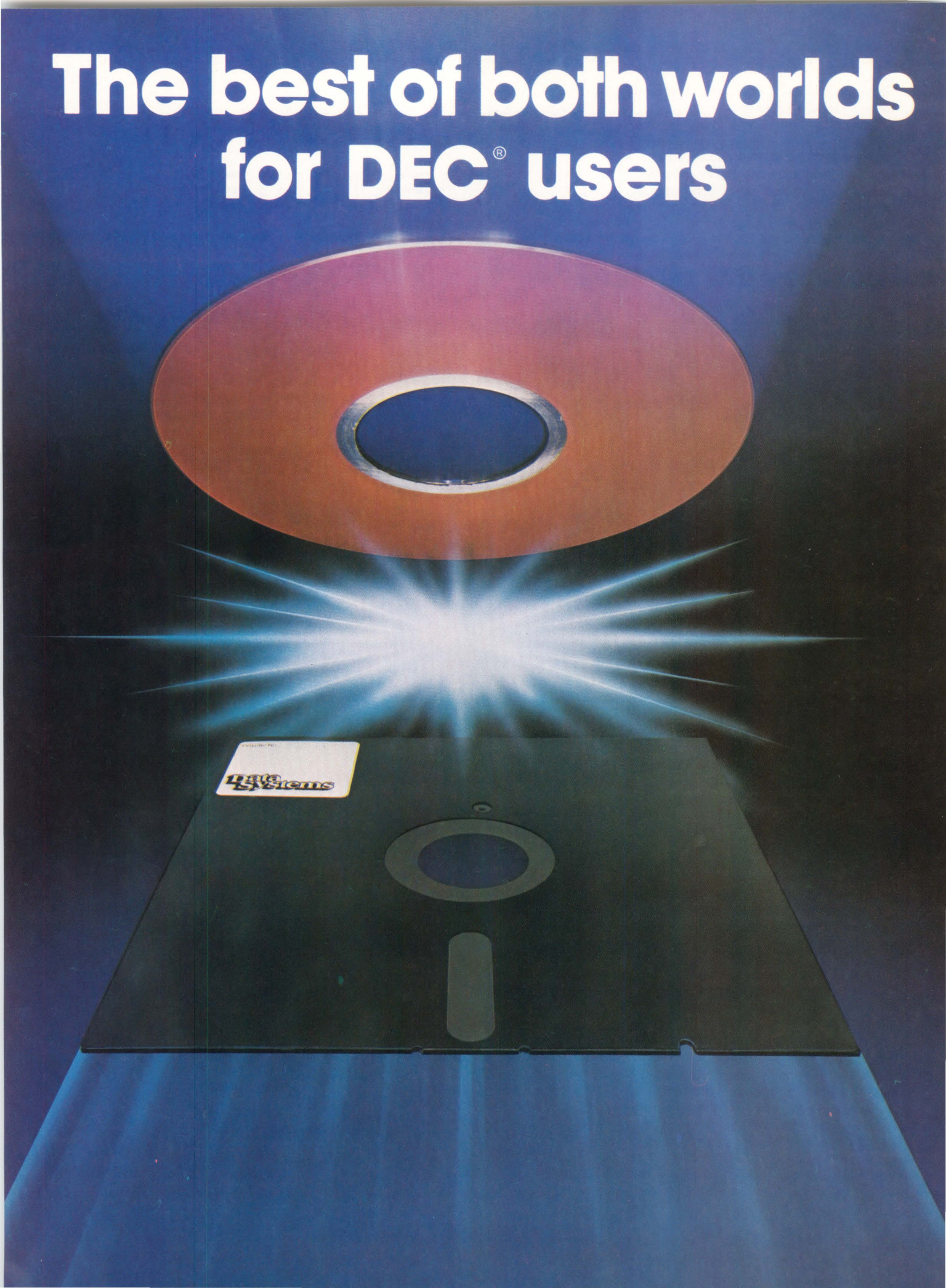


Intelligent measurement and control system. Microprocessor unburdens host computer by performing many control procedures on the board. Screw terminals are provided for direct sensor connection. Plug-in signal conditioning modules are chosen to match sensors used in specific application. DIP switches select even or odd parity and baud rates up to 9600

Expanded systems consist of a 9.5 x 13″ (24.1 x 33-cm) master board, expander boards, and a digital I/O subsystem. ADC, 8085A CPU, 4k of RAM, 64k of ROM, and universal asynchronous receiver/transmitter (UART) communications interface on the master board are shared by the expander boards. The digital I/O subsystem interfaces to the other boards through the digital I/O port and permits use of the system with the power control circuits and loads common to heavy industrial environments. Each expander board, as well as the master board, contains an onboard power supply; the I/O subsystem requires a separate 5-V source.

As many as three plug-in QMX multiplexer modules can be accommodated. (See the diagram.) Channel input data are measured, stored, and transmitted in terms of dc voltage, degrees Celsius or Fahrenheit, or 0 to ±100% of span. A QMX input multiplexer carries out transducer signal conditioning; when the proper input module is selected and the onboard DIP switches are set, the QMX module and the programmable gain amplifier are programmed to scale the analog signal to the input range of the dual-slope ADC. A factory set rate of 15 conversions/s can be increased to 30, but results in reduction of the normal mode rejection ratio. □

The best of both worlds for DEC® users



Data Systems Design's DSD 880

Introducing the DSD 880 — A DEC-compatible disk system combining eight-inch winchester and floppy disks

For DEC users who need more capacity and performance than an RX02, the DSD 880 now offers a more cost effective alternative than a dual RL01. Consider these benefits offered by the DSD 880:

- significantly lower initial and total life-cycle costs
- the reliability of a winchester, with 7.8 Mbytes, emulating RL01
- the removability of a floppy disk, with 1 Mbyte, emulating RX02
- valuable saving in rack space (5¼" vs. 21" for dual RL01)
- unique "hyperdiagnostics" enabling fast and easy trouble-shooting to the modular level
- built-in bootstrap eliminating the need for an expensive DEC bootstrap board and saving a backplane slot
- one half-quad backplane slot vs. two quad boards for the RLV11
- versatile interface card for easy integration with any LSI-11 backplane, unlike DEC's RLV11 interface that needs a special backplane and cannot be used with the VT 103 terminal

Compare for yourself and see why nothing compares to the DSD 880.

Data Systems

The Intelligent Alternative to DEC Disk Systems

To get more information on the DSD 880 call or write:

CORPORATE HEADQUARTERS:
2241 Lundy Avenue
San Jose, CA 95131
TEL: (408) 727-9353
TWX: 910 338-0249

WESTERN REGION SALES:
2560 Mission College Blvd., Suite 108
Santa Clara, CA 95051
TEL: (408) 727-3163
TWX: 910 338-0249

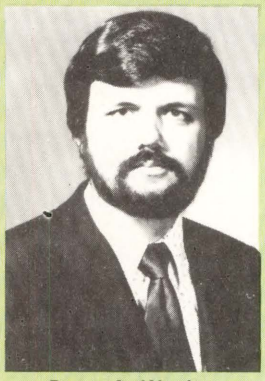
EASTERN REGION SALES:
51 Morgan Drive
Norwood, MA 02062
TEL: (617) 769-7620
TWX: 710 336-0120

INTERNATIONAL SALES: Australia, Melbourne (03) 543-2077, Sydney (02) 848-8533; Canada (416) 625-1907; Denmark 01/83 34 00; Finland 90/88 50 11; France 03/956 81 42; Israel 03/ 298783; Italy 02/ 4047648; Japan, Osaka (06) 323-1707, Tokyo (03) 345-1411; Netherlands 020/45 87 55; New Zealand 4-693-008; Norway 02/78 94 60; Sweden 08/38 03 70; Switzerland 01/730 48 48; United Kingdom 01/207-1717; West Germany and Austria (089) 1204-0.

International Solid State Circuits Conference

Grand Hyatt Hotel, New York, New York

February 18-20, 1981



Bruce A. Wooley
Program Chairman

Jerome J. Suran
Keynote Speaker

ISSCC '81, in its 28th year, will stress the new era in digital electronics, in particular the dynamic trend toward significant increases in the number of bits per chip for VLSI and related microcircuits. The program schedules more than 50 papers to be given during 15 daytime sessions, with 10 panel sessions to be held on Wednesday and Thursday evenings. Authors and presenters from the U.S. and throughout the free world will number over 300.

The formal opening of the conference, at a special double session beginning at 1:30 pm on Wednesday, will consist of welcoming remarks by program chairman Bruce A. Wooley of Bell Laboratories and by executive committee chairman J. A. A. Raper of General Electric, award presentations, and the keynote address. Among the awards to be presented are the IEEE Cledo Brunetti Award, which will go to Donald R. Herriott of Bell Laboratories, for key contributions to the development of a practical beam system for fabrication of IC masks and to other aspects of microlithography; the ISSCC Beatrice Winner Award for Editorial Excellence; and the ISSCC Best Paper Awards. Jerome J. Suran, staff executive with the technical systems and materials sector technology operations of General Electric Company, and a past president of IEEE, will deliver the keynote address, "The Technology Thrust of New Era Electronics."

ULSI and VLSI

A hierarchy of limits governing ultra-large scale integration will be defined in the invited paper opening the session on Solid State Devices (session 3, Feb 18, 9-11:45 am). This report will also describe circuit performance to project minimum dimensions for NMOS transistors, polysilicon resistors, and interconnections, and will assess possible future levels of ULSI. Other presentations during this session will concern an experimental floating gate FET with two capacitively coupled control gates for a nonvolatile and electrically alterable application (an enhanced conduction insulator under one control gate charges and/or discharges the floating gate); a merged bipolar/JFET structure with a 50-V breakdown and f_T of 0.5 GHz for a standard 5-V digital process; the saturation velocity operation of a silicon Hall device to achieve high magnetic sensitivity independent of bias voltage and temperature; and an active ballasting technique to fabricate an oxide passivated power transistor with f_T of 50 MHz and capable of continuously dissipating 250 W with collector voltages above 200 V.

VLSI Microcomputer Systems (session 9, Feb 19, 9 am-12:15 pm) will describe a fully integrated 32-bit VLSI processing system made up of six VLSI chips (with up to 600k transistors/chip), including a 32-bit CPU, I/O

(continued on page 96)

Introducing

The OP-1/15

A Unique Low-Cost Display Computer

Announcing the latest addition to the highly successful OP-1 family of display computers ... the OP-1/15.

Designed as an intelligent user-programmable work station or low-cost standalone system, the OP-1/15 is housed in an attractive desk-top enclosure. Its advanced styling includes a modern, low profile keyboard and tiltable CRT display.

A large 15 inch display monitor provides 25 lines of crisp and clear character presentation. Sophisticated video enhancements such as reverse, blink, bold, underline and suppress are standard and under program control.

The OP-1/15 is compatible with Ontel's wide selection of software. It may be configured with up to 64K of RAM and 16K of PROM storage. Integral serial and parallel adapters provide communications capabilities for cluster operation with local printing.

Optional features include a matching dual mini-diskette console with DMA-based controller for more than a half-megabyte of local storage. Most standard Ontel peripheral controllers may be used as the high speed I/O port on the OP-1/15.

Contact me today for additional information including our very attractive pricing and delivery.

Douglas Wagner
National Sales Manager
Ontel Corporation
250 Crossways Park Drive
Woodbury, NY 11797
(516) 364-2121

CIRCLE 56 ON INQUIRY CARD

processor, memory controller, 128k-bit RAM and 528k-bit ROM. An NMOS VLSI fabrication process for the chips in the 32-bit VLSI processing system just mentioned makes use of optical lithography with a 2.5-μm pitch and double-layer metallization. Another paper will cover a 16-bit NMOS microprocessor which combines a minicomputer instruction set with a microprocessor bus. Four other papers during this session will discuss a 32-bit VLSI micromainframe computer system and its components. Subjects include the architecture goals and the circuit, logic, and process technology objectives; a 335-mil square micromainframe execution unit chip that accepts, decodes, and executes the continuous stream of microinstructions received from the sequencer in the basic computer; a 320-mil square instruction decoding unit chip, containing more than 100k transistors, that decodes the bit aligned, variable-length instructions and produces the microinstructions and data necessary for execution; and the 342-mil square I/O interface processor chip.

VLSI Logic (session 16, Feb 20, 9 am-12:15 pm) will be the subject of one of the three concurrent closing sessions on Friday. Papers to be given include a description of an 8-bit single-chip microcomputer having two nonvolatile NMOS memories; the chip contains both a 1k-byte program store and a 60-byte realtime rewritable data store. Another paper will report on a 16-bit CMOS/NMOS SOS 12k-gate microprocessor which involves a barrel shifter and a multiplier; the chip features a 300-ns cycle time with only 600-mW power dissipation. A 1-μm bipolar VLSI convolution device, applicable to many digital signal processing requirements, contains 16,200 devices, operates at 30 MHz, and consumes only 700 mW. The last paper will discuss a bipolar 2500-gate subnanosecond masterslice LSI, developed for random logic; it provides an average delay time of 0.8 ns/gate and has a power dissipation of 0.5 mW/gate.

Three evening panel sessions, one on Wednesday, Feb 18, and two on Thursday, Feb 19, will be on various aspects of VLSI technology. CMOS versus NMOS for VLSI (evening session 3) will present recent developments in high density, high speed CMOS memories and the concern for lower power dissipation that makes the reexamination of the CMOS/NMOS issue timely.

Packaging for VLSI Components (evening session 7) will deal with the problems that are expected when semiconductor components with as many as 10^6 devices become feasible in the near future. Design Methodologies for VLSI (evening session 8) will examine design cost and time both of which are escalating at an exponential rate as the complexity of ICs grows likewise.

Memories and Related Techniques

RAMs and other memory technologies will receive close attention in three separate daytime sessions. Static RAMs (session 1, Feb 18, 9-11:45 am) will cover a 4k static RAM using 2-μm $MoSi_2$-gate CMOS/SOS technology with 18-ns access time, 200-mW operating power, and 50-μW standby power; an 18-ns/150-mW fully static 4096 x 1-bit RAM using double poly HI-CMOSII technology with 2-μm gate length; a 64k x 1-bit fully static MOS RAM, using 1.5-μm design rules, with multiplexed addressing, that is assembled in a standard 300-mil 16-pin DIP; another 16k x 1-bit fully static RAM using double level poly scaled NMOS technology (typical 30-ns access time and 600-mW power dissipation); and a 25-ns 16k x 1-bit static RAM using a double polysilicon/molybdenum process.

Memories and Redundancy Techniques (session 8, Feb 18, 3:15-6 pm) will investigate redundancy techniques for static RAMs; fault-tolerant VLSI memory yield improvement; a 100-ns 64k dynamic RAM using redundancy techniques; a 32k static RAM utilizing a 3-transistor cell; and a 4k x 8-bit dynamic RAM with self-refresh. On Thursday afternoon, Memory Techniques (session 12, Feb 19, 1:30-5 pm) will cover a completely TTL-compatible, single 5-V supply, nonvolatile static RAM utilizing a 3-layer polysilicon process and a low current floating-gate tunneling approach. A report will discuss a 45-ns fully static 16k MOS ROM that makes extensive use of small signal amplification and 0-V threshold devices to reduce active power to 350 mW and standby power to 75 mW. Another will describe a 34-μm^2 DRAM cell fabricated with a 1-μm single-level polycide FET. Discussed in another report will be CCD multilevel storage techniques that result in increased bit density and decreased sense signal, citing design considerations for multilevel storage. The technique of byte-wide magnetic bubble memory interfacing will also be described, along with the implementation of interface circuitry associated with a 256k-byte memory. The last paper in this session will report on the development of a high speed, split-emitter cell designed to overcome the problem of small sense signals in injector-sensed IIL/MTL memories.

Data Acquisition and Communication

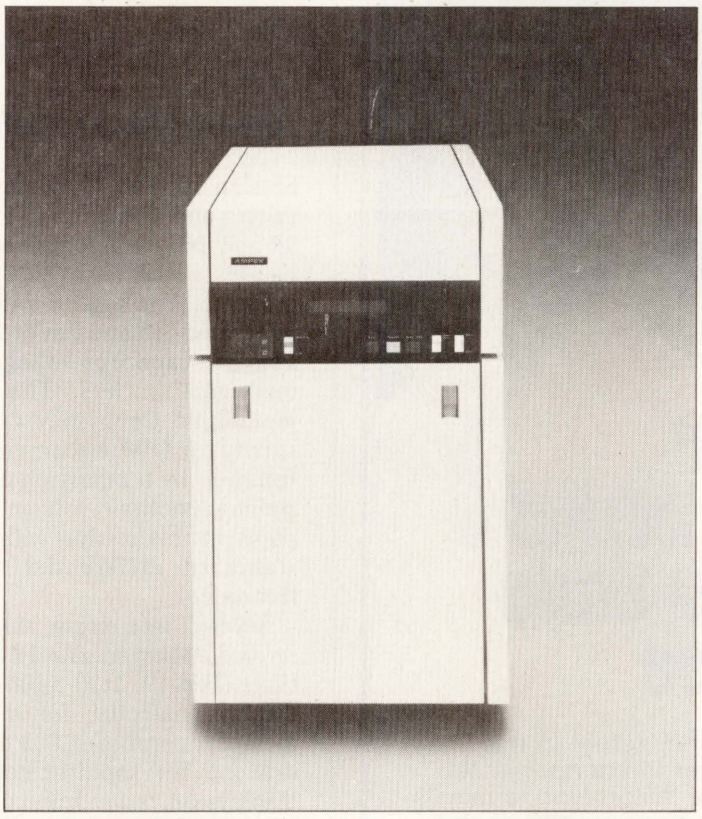
A-D converters will be the main subject of Data Acquisition Circuits (session 6, Feb 18, 3:15-6 pm). The first paper will report on a 12-bit ADC with integral track and hold fabricated in compound monolithic form. The next will describe an integrated 16-bit ADC for PCM audio systems, with an instantaneous sampling and coarse-fine integration techniques. Another paper will discuss a 2-chip CMOS ADC circuit, used in a handheld digital thermometer, that employs a compensating circuit for the reference junction of a thermocouple and a switching amplifier to resolve signals as small as 1 μV.

The subject of another report is an error-correcting 14-bit/20-μs CMOS ADC, fabricated on a 4.1 x 4.2-mm monolithic chip using a thin-film non-binary 17-bit DAC that resembles an R-2R ladder (with a radix of about 1.85 instead of 2), a conversion algorithm, and a calibration EPROM. The session will also include a paper on a curvature-corrected micropower voltage reference.

Close attention will be paid to single-chip devices in several papers in Telecommunication Circuits (session 17, Feb 20, 9 am-12:15 pm). These will include a description of an optically coupled crosspoint array with a >450-V breakover voltage, dV/dt >2000 V/μs

(continued on page 98)

TOTAL CDC COMPATIBILITY AND GREAT DELIVERY, TOO!



The only thing worse than not having enough disk storage, is not being able to get enough disk storage.

Fortunately, the Ampex DM-9300AQ solves both problems. With 300 megabytes of reliable disk pack storage and off-the-shelf delivery.

But the advantages of the DM-9300AQ don't stop with delivery. It's completely compatible with CDC's 300 megabyte drive. So disk packs can be interchanged, written on, or read by either drive. Of course, the industry standard SMD interface, and power sequencing of both units are also compatible.

DM-9300AQ disk pack swapping is as easy as using them. Its large front opening has been designed with the convenience of a top loader, and human engineered for minimal lifting. So even a 20-pound pack is easy to insert and remove. It's such a good idea, we're surprised somebody didn't think of it sooner.

But then, the DM-9300AQ is full of good ideas. Like highly reliable on-track servoing, and a single port daisy-chain interface with ribbon cable that can be converted—in the field—to an internal dual port.

And the same goes for maintenance. Service requires only front, rear, or top access. Side access is eliminated, so you can arrange the units side by side. What's more, the logic chassis in the rear of the unit swings out to provide easy access to all test points and connections. And extensive use of LEDs simplifies trouble-shooting.

The DM-9300AQ has a lot to offer. But what's even better, is that it's all offered right now. With delivery that's ready when you are.

The DM-9300AQ. Just one of a complete line of Ampex plug compatible disk drive memories for nearly any CPU.

For more information, contact Gary Owen at Ampex Memory Products, 200 North Nash Street, El Segundo, California 90245. If you're really in a hurry call him at 213/640-0150. Or contact your local sales office.

Either way, we won't keep you waiting.

AMPEX

MAKES THE DIFFERENCE.

CIRCLE 57 ON INQUIRY CARD

capability, and >5-mA gate sensitivity. One paper will describe a fully integrated CMOS filter/CODEC chip with an independent encoder/decoder, transmit/receive filters, and bandgap reference sources on the 30-mm² chip. Another will discuss a monolithic CMOS PCM CODEC with filters using charge distribution and switched-capacitor techniques on a 23.4-mm² active chip area. Still another paper will report on a PCM CODEC and filters integrated on a 30.4-mm² chip using CMOS technology, and consisting of an encoder/decoder, switched-capacitor filters, and two PLL clock generators.

Analog Devices and Advanced Circuits

Session 10 (Feb 19, 9 am-12:15 pm) will cover Analog Filters and Oscillators. The first paper will describe a 37-mW fully self-contained narrow-bandwidth recursive bandpass with passive CCD resonators for FDM channel modems. The second will present results obtained for integrated 5th and 7th order Chebyshev filters based on switched-capacitor voltage-wave design, requiring only unity-gain buffers. The next paper will describe a monolithic Chebyshev CCD wave filter with low sensitivity for FDM telecommunication systems. This will be followed by a report on a high frequency temperature-stable monolithic voltage controlled oscillator. The last paper in this session will discuss a low noise chopper-stabilized differential switched-capacitor filtering technique.

Several interesting single-chip devices will be described during session 13 on Advanced Circuit Applications (Feb 19, 1:30-5 pm). Among these are a graphic display controller for a 256k-word x 16-bit display memory, permitting 800 ns/dot address calculation and drawing for sophisticated alphanumeric and graphic displays on raster-scan color CRTs. Another single-chip device is a fiber optic receiver circuit capable of operating at 200M-bit data rates with an NEP of 36 dBm.

Also considered during session 13 will be a library of self-testing VLSI cells for both online and offline testing, citing a 16 x 16-bit array multiplier with 9300 CMOS transistors as an example. A self-testing 1k-bit ROM device that permits the test mode functional conversion of peripheral subcircuits into test aids will be discussed in another report.

Running concurrently, session 14 will cover Analog Techniques (Feb 19, 1:30-5 pm). The first paper will report on a low noise bipolar op amp with excellent characteristics. This will be followed by a description of a 30-MHz photodetector with a heterojunction preamplifier. The third paper will describe an NMOS comparator for a bubble memory peripheral support chip.

Session 14 will continue with a description of a 4-terminal wideband monolithic amplifier. A technique will then be described for a cascode amplifier

nonlinearity correction that provides compensation for the diode nonlinearity of an emitter degenerated cascode stage by using an additional emitter degenerative pair. The last paper of the session will report on an open loop programmable amplifier with a maximum gain-bandwidth product of 1 GHz.

Advanced Process Technology (session 15, Feb 20, 9 am-12:15 pm) will include a report on a bulk CMOS technology based on HMOS offering such features as a high resistivity P substrate, diffused wells, and 2-μm channel length N- and P-channel devices. A second paper will discuss the quality of silicon on spinel epitaxially grown on spinel, and the characteristics of 250-V bipolar ICs and MOS devices fabricated in the epitaxial silicon. Another technique that will be described is the numerical simulation of impurities redistribution near a mask edge in general processing conditions. In conjunction with 2-dimensional device analysis programs, the simulation is a useful tool in understanding lateral effects in small geometry VLSI devices.

The fabrication of a multiple self-aligned bipolar transistor with a sidewall base electrode will be covered in another report. A description will also be given of the super self-aligned process technology used to fabricate a static bipolar 256 x 4-bit ECL RAM (3 ns/1k bits) with typical access times of 2.7 ns at 550 mW. The final paper in the session will discuss a self-aligned source/drain planar device for ultrahigh speed GaAs MESFET VLSIs.

Informal panel discussions will be held on a variety of subjects during the first two evenings of the conference. In addition to the evening sessions previously described, one panel will assess the latest developments in power GaAs FET amplifiers, with emphasis on circuit design for performance and reliability. Concurrently, on Wednesday evening, there will be a discussion of speech synthesis techniques.

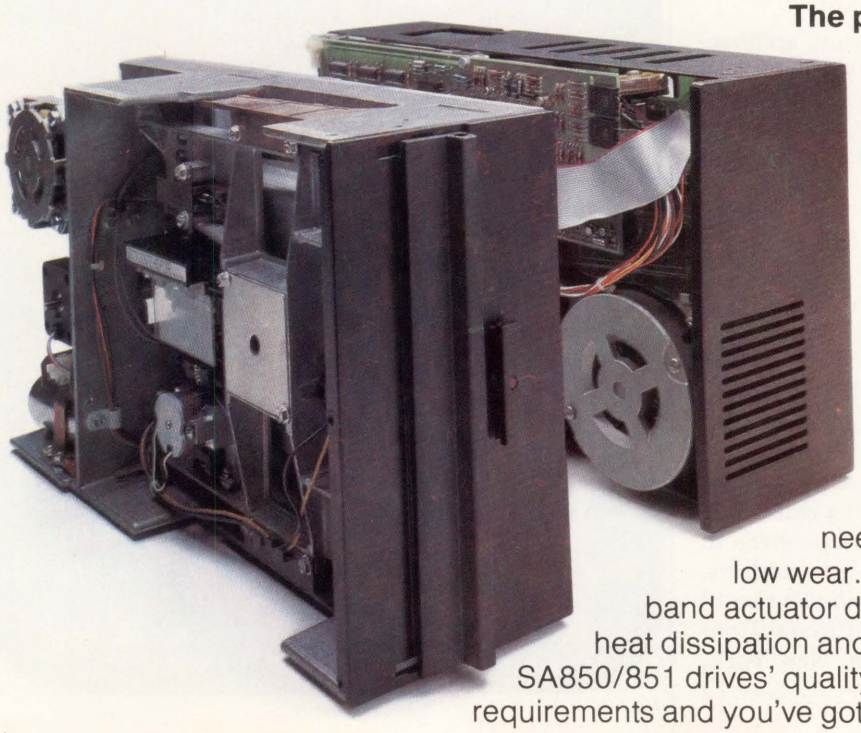
On Thursday evening, a panel will discuss architecture, bus design, software compatibility, high level language capability, and software functions to aid in the selection of microprocessor families. Concurrently, there will be panel discussions on the limits of precision analog ICs and on millimeter wave ICs.

Registration

Advanced registration (postmarked by Feb 2) is $50 for IEEE members and $70 for nonmembers. Late registration, or registration at the door, will cost an additional $10 for both members and nonmembers. A copy of the ISSCC *Digest of Technical Papers*, containing edited and illustrated condensations of all papers, will be given to all attendees. Register by sending name and address, with the proper remittance in U.S. funds (make checks payable to: ISSCC '81), to: IEEE Solid State Circuits Conference, Box 1625, Grand Central Station, New York, NY 10017. □

Now rolling on the fast track. The race is on for high volume production of double-sided eight-inch floppys. And Shugart's SA850/851 drives are widening their lead. The first OEM double-sided drives introduced in 1977 were from Shugart and since then we've continued to invest our resources in perfecting the technology. After hundreds of man/years of R & D and production engineering, we've succeeded in bringing our OEM customers the most reliable, cost-effective and manufacturable double-sided drive in the industry. With more than 70,000 SA850/851's already installed and production rolling into high gear, now's the time to get your double-sided product plans on the inside track with the Shugart Express.

SA850
The inside track



The perfect match. With 1.6 MBytes of unformatted storage, the SA850/851 drives are the perfect back-up solution for Winchester fixed disk systems. And since they're identical in size and I/O compatible with our SA800 drives, the SA850/851's are the perfect match for upgrading existing single-sided floppy systems as well. Head and media problems are a thing of the past because our Bi-Compliant™ head assembly delivers the superior media compliance needed for solid data integrity and low wear. And our famous Fasflex™ metal band actuator delivers 3 ms access times with low heat dissipation and superb reliability. Match up the SA850/851 drives' quality and performance with your system requirements and you've got a winner—on any track.

™ Trademark of Shugart Associates

/851. for OEM success.

Experience Curve Benefits. With more technological firsts and shipments of 1½ million floppy disk drives, Shugart brings unsurpassed experience to its production of double-sided floppys. And we are continuing to reinvest in R & D, manufacturing technologies and customer support programs to bring you the most thoroughly engineered, most reliable double-sided floppys in the industry. Give us a call today for your reservation on the Shugart Express at one of our sales offices, or Hamilton/Avnet outlets. □ **Shugart Associates: 475 Oakmead Parkway, Sunnyvale, CA (408) 733-0100.** *Sales & Service: Sunnyvale, CA; Costa Mesa, CA; Minneapolis, MN; Richardson, TX; Framingham, MA; Mt. Freedom, NJ; Atlanta, GA; Toronto, Ontario; Paris, France; Munich, Germany.* □

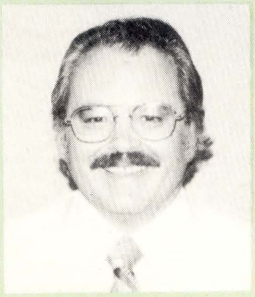
Shugart®

CIRCLE 60 ON INQUIRY CARD

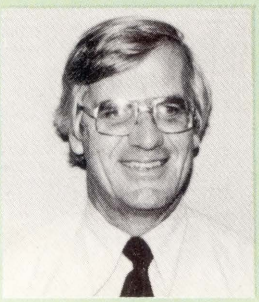
COMPCON Spring '81

Jack Tar Hotel, San Francisco, California

February 23-26, 1981



Theodore Laliotis
General Chairman



James Rudolph
Program Committee Chairman

"VLSI in the laboratory, the office, the factory, the home..." is the theme of COMPCON Spring '81, the 22nd IEEE Computer Society International Conference. A total of 36 sessions, nine in each of four areas of study—Architecture, Technology, Applications, and Software—will be held Tuesday through Thursday, February 24-26. On Monday, preceding the regular conference program, three all-day preconference tutorials will be held on Distributed System Design, Local Computer Networks, and Computer-Assisted Design and Engineering.

General Chairman Theodore Laliotis of Hewlett-Packard will officially open the conference on Tuesday, February 24, at 9:00 am. Following his welcoming remarks, he will introduce the keynote speaker, Carver Mead of the California Institute of Technology, who will address the conference on "The Next Revolution in Electronics."

A special all-conference program will be held on Wednesday, February 25, 3:30-5 pm. An invited paper, "Prometheus or Pandora: The Influence of Automation on Society," will be presented by Nobel Laureate Herbert A. Simon, professor of computer science and psychology at Carnegie-Mellon University.

Special Attention to VLSI

Particular attention will be paid to VLSI in eight sessions, as well as in specific papers to be given in a number of other sessions. VLSI Forecasting will be the theme of the panel discussion in session 2 (Feb 24, 1:30-3 pm), and the problems of VLSI packaging will be covered by three papers in session 6 (Feb 24, 3:30-5 pm). The European view of Applications for VLSI will be given by several speakers from Western Europe during session 7 (Feb 24, 3:30-5 pm). Four papers related to VLSI in Speech Processing will be presented during session 11 (Feb 25, 8:30-10 am).

VLSI Testing will be the overall subject for the three papers in session 22 (Feb 26, 8:30-10 am); and speakers from Western Europe will discuss Technological Development of VLSI during session 26 (Feb 26, 10:30 am-noon). Five papers and a panel discussion on 32-Bit VLSI Computers will take two sessions on the last day of the conference: session 29 (Feb 26, 1:30-3 pm) will cover Part I, and session 33 (Feb 26, 3:30-5 pm), Part II.

Software

Although the conference is nominally divided into four stems, many of the sessions have papers that demonstrate the effect of one stem on another. For example, four papers planned for session 4 (Feb 24, 1:30-3 pm) will focus on the impact of software on microprocessor architecture: Finding Architectural Commonality between Software and Hardware; Microprocessor Architecture Which Reflects Software Requirements; Software Impact on Microprocessor Architecture: A Case Study; and Computer Architecture in LSI: Lessons and Prospects.

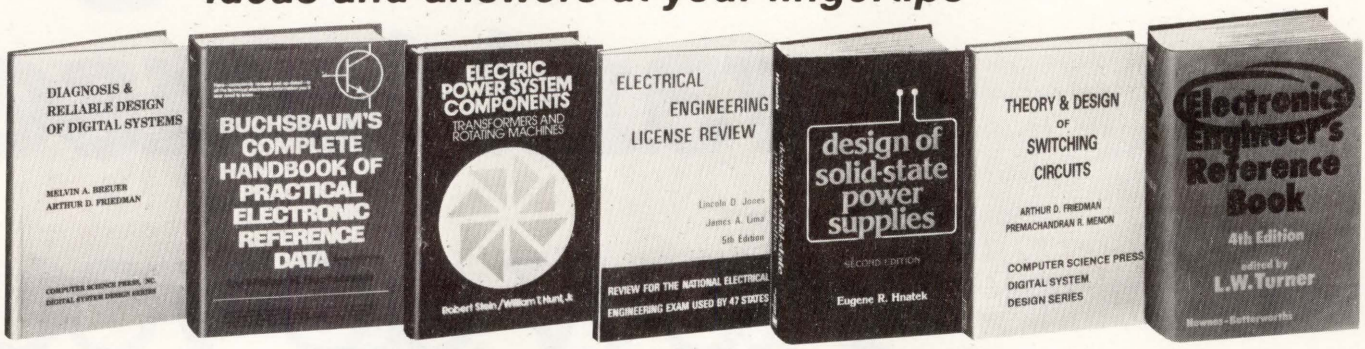
Other software topics will be covered during session 12 (Feb 25, 8:30-10 am), a panel discussion on Ada: Fear and Loathing in Programming. Session 16 (Feb 25, 10:30 am-noon) will present four papers on Operating System Topics; session 20 (Feb 25, 1:30-3 pm) will be a panel discussion on Migrating UNIX to Micros; session 24 (Feb 26, 8:30-10 am), another panel, will discuss

(continued on page 106)

INTRODUCING

Electrical and Electronics Engineering Book Club

Ideas and answers at your fingertips



Take any 3 books for only $1.00 each (values to $71.40)

if you will join now for a trial period and agree to buy 3 more books—at handsome discounts—over the next 12 months.

Now you can build a valuable professional library easily, conveniently and at great savings! Select your introductory books now and mail in the coupon today.

(Publishers' Prices shown)

42175. DIAGNOSIS AND RELIABLE DESIGN OF DIGITAL SYSTEMS. *Breuer and Friedman.* **$21.95**

36915. BUCHSBAUM'S COMPLETE HANDBOOK OF PRACTICAL ELECTRONIC REFERENCE DATA. *Walter H. Buschbaum.* **$19.95**

44080. ELECTRIC POWER SYSTEM COMPONENTS. *Stein and Hunt.* **$22.50**

44125. ELECTRICAL ENGINEERING LICENSE REVIEW. *Jones and Lima.* **$16.95**

52170. HANDBOOK OF DIGITAL IC APPLICATIONS. *David L. Heiserman.* **$21.95**

83380-2. THEORY AND APPLICATION OF DIGITAL SIGNAL PROCESSING. *Rabiner and Gold. Counts as 2 of your 3 books.* **$29.95**

69750. A PRACTICAL GUIDE TO COMPUTER METHODS FOR ENGINEERS. *Terry E. Shoup.* Lists software with guidelines for application. **$17.95**

77790-2. SEMICONDUCTOR DEVICES AND INTEGRATED ELECTRONICS. *Arthur George Milnes. Counts as 2 of your 3 books.* **$26.50**

42033-2. DESIGN OF SOLID-STATE POWER SUPPLIES. *Eugene Hnatek.* From oscillators and transistors to finished converters/inverters. *Counts as 2 of your 3 books.* **$27.50**

83400. THEORY AND DESIGN OF SWITCHING CIRCUITS. *Friedman and Menon.* **$22.95**

44155. ELECTRONIC DESIGNER'S HANDBOOK. *Thomas Keith Hemingway.* **$14.95**

62751. MINI/MICROCOMPUTER HARDWARE DESIGN. *Kraft and Toy.* **$20.95**

44900-3. THE ENCYCLOPEDIA OF COMPUTER SCIENCE. *Edited by Ralston and Meek.* Monumental 1550-page volume covers topics ranging from theory and applications to programming and Boolean algebra. *Counts as 3 of your 3 books.* **$60.00**

52214. HANDBOOK OF ELECTRONIC FORMULAS, SYMBOLS AND DEFINITIONS. *John R. Brand.* **$15.95**

73865-2. RELIABILITY AND MAINTAINABILITY OF ELECTRONIC SYSTEMS. *Edited by Arsenault and Roberts.* 597 pages. *Counts as 2 of your 3 books.* **$28.95**

84555-2. TRANSFORMER AND INDUCTOR DESIGN HANDBOOK. *Wm. T. McLyman. Counts as 2 of your 3 books.* **$35.00**

42498. DOCUMENTATION STANDARDS AND PROCEDURES FOR ON-LINE SYSTEMS. *Edited by Martin L. Rubin.* **$21.95**

62881. MODERN SWITCHING THEORY AND DIGITAL DESIGN. *Samuel G. Lee.* **$23.95**

42260-2. DIGITAL COMMUNICATIONS BY SATELLITE. *Edited by Thomas Kailath. Counts as 2 of your 3 books.* **$38.50**

78364-2. SINUSOIDAL ANALYSIS AND MODELLING OF WEAKLY NONLINEAR CIRCUITS: With Application to Nonlinear Interference Effects. *Weiner and Spina. Counts as 2 of your 3 books.* **$27.50**

42267-2. DIGITAL CONTROL SYSTEMS. *Benjamin C. Kuo.* Packed with on-the-job examples and special analytical tools. *Counts as 2 of your 3 books.* **$27.95**

57775. LASER SAFETY HANDBOOK. *Mallow and Chabot.* **$22.50**

52210-2. HANDBOOK OF ELECTRONIC DESIGN AND ANALYSIS PROCEDURES USING PROGRAMMABLE CALCULATORS. *Bruce K. Murdock. Counts as 2 of your 3 books.* **$26.50**

62651. MICROPROCESSORS AND MICROCOMPUTER SYSTEMS. *G. V. Rao.* **$24.50**

44300. ELEMENTS OF ELECTRONIC INSTRUMENTATION AND MEASUREMENT. *Joseph J. Carr.* **$17.95**

80270. STARTING AND MANAGING YOUR OWN ENGINEERING PRACTICE. *John A. Kueken.* **$13.95**

52185. HANDBOOK OF ELECTRONIC COMMUNICATION. *Gary M. Miller.* **$17.95**

79167. SOFTWARE RELIABILITY GUIDEBOOK. *Robert L. Glass.* **$18.95**

79163. SOFTWARE QUALITY MANAGEMENT. *Cooper and Fisher.* **$20.00**

57770. LASER BEAM INFORMATION SYSTEMS. *Edited by William C. House.* Job-oriented approach. **$15.00**

Membership Benefits. In addition to getting three books for only $1.00 each when you join, you keep saving substantially on the books you buy. • Also, you will immediately become eligible to participate in our Bonus Book Plan, with savings of at least 70% off the publishers' prices. • At 3–4 week intervals (16 times per year) you will receive the Book Club News, describing the coming Main Selection and Alternate Selections, together with a dated reply card. • If you want the Main Selection, do nothing and it will be sent to you automatically. • If you prefer another selection, or no book at all, simply indicate your choice on the card, and return it by the date specified. • You will have at least 10 days to decide. If, because of late mail delivery of the News, you should receive a book you do not want, we guarantee return postage.

—Special Selection—

44145-3. ELECTRONICS ENGINEER'S REFERENCE BOOK. *Edited by L. W. Turner.* Up-dated, covers electronic materials and components, solid state devices, integrated circuits, microelectronics, telecommunications and electronics in industry plus much more. 1600 pages. *Counts as 3 of your 3 books.* **$78.00**

88008. WRITING FOR RESULTS. *David W. Ewing.* **$18.95**

32265-2. ADVANCED LOGICAL CIRCUIT DESIGN TECHNIQUES. *Svoboda and White. Counts as 2 of your 3 books.* **$27.50**

00470-3. VAN NOSTRAND'S SCIENTIFIC ENCYCLOPEDIA. *Edited by Douglas M. Considine.* Outstanding reference for professional engineers with over 7,200 articles on scientific and engineering subjects. 2,382 pages; 2,500 illustrations and charts. *Counts as 3 of your 3 books.* **$69.50**

Electrical and Electronics Engineering Book Club
Riverside, New Jersey 08075

Please accept my application for trial membership and send me the three volumes indicated, billing me only $1 each. I agree to purchase at least three additional Selections or Alternates over the next 12 months. Savings range up to 30% and occasionally even more. My membership is cancelable any time after I buy these three books. A shipping and handling charge is added to all shipments.

3 books for $1 each.
Indicate by number the books you want.

A few expensive books (noted in book descriptions) count as more than one choice.

No-Risk Guarantee: If you are not satisfied—for any reason—you may return your introductory books within 10 days and your membership will be canceled and you will owe nothing.

Name_____

Address_____

City_____

State_____ Zip_____

(Offer good in Continental U.S. and Canada only. Prices slightly higher in Canada.) M-AB6

Your design want to use How do you

Ask the leader in gate arrays, International Microcircuits Incorporated.

Gate arrays are now being used for a wide variety of LSI applications. If your designers want to take advantage of gate arrays, here are the questions and answers that will help you decide.

Frank Deverse, President

Just what is a gate array?

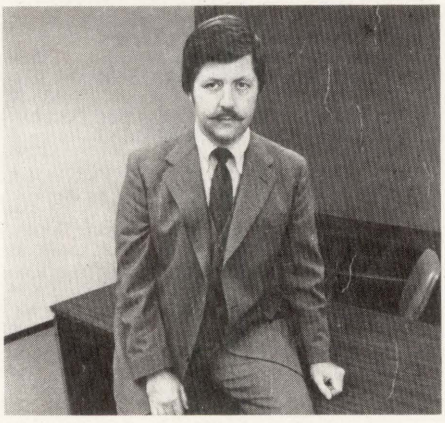
A gate array is the fastest way to get to a unique digital LSI device at low cost. We take a pre-designed, preprocessed matrix of transistors and interconnect them uniquely for each customer. The result is a **proprietary silicon solution** to your logic needs.

Why should I consider gate arrays?

Quick access to LSI, low development costs, and the opportunity to leapfrog the competition and get your product to market faster. Like IBM did with the 4300.

Are gate arrays just another niche product?

We believe gate arrays are a mainstream technology because they solve the new set of problems resulting from the push toward VLSI. High density silicon helps solve the problems of reliability, parts count, power dissipation and testing. Gate arrays solve the key problems of this density: design time and talent. They give you economical access to the benefits of LSI. The issues are universal. The gate array solution is very attractive.



Joe Kroeger, Director of Marketing

There must be some tradeoffs involved.

Sure. With gate arrays you will considerably shorten your development time and cost—translate a superior design into an IC quickly—but you may not use your chip space as efficiently as with fully custom logic. (But ask us again next year; even that difference is going away.) Corporately, this means that if you need to get your product to market quickly in moderate volume, you need gate arrays. If you have several million units that you have to shave every cent of cost from, you need custom logic.

What do the costs look like?

Since many customers make use of common background chips, the bulk of the tooling and design costs have already been amortized. To get to your proprietary circuit takes—ballpark—$10K, 7 weeks, and we do the layout. I'll give you a firm quote when we see your logic problem.

Who's using gate arrays now?

You already know about IBM. The customers who've been coming to us since 1974 are all over the industry, but they're each at the leading edge of their business. They're using gate arrays for their leapfrog generation of products. And we now see new gate array suppliers entering the market in droves.

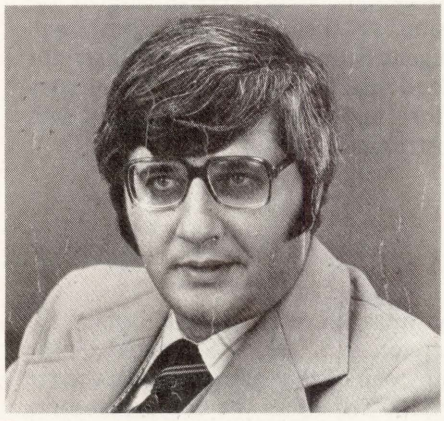
Sounds like a booming business. Why?

Three converging forces are making gate arrays more widely applicable. As standard logic becomes more dense and therefore more specialized, volumes are declining and part numbers are proliferating. Today's complexity of circuits is lengthening standard product development times. And gate arrays

engineers gate arrays. decide?

themselves are far faster and more versatile than they were a few years ago. We're delivering 2,000 gate-cells per chip now, looking at about 4,000 soon and forecasting nearly 10,000 in '82. Three years ago we were offering less than 500 gate-cells per chip.

It's not a sudden boom. It has been building for several years and we have done more than 400 circuits during that time.



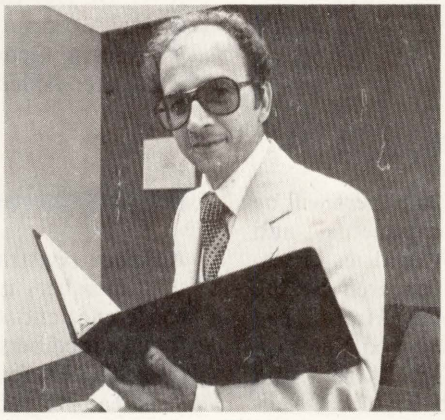
Orhan Tozun, Director of Engineering

How do we interface with you? How do we get started?

Our engineering department talks with your designer and evaluates your logic to make sure it's do-able on one of our many gate arrays. The next step is a firm quote to let you evaluate the economics of our solution. That includes both development and production costs. We can do it because our CAD system gives us consistency and our years of experience provide projectable yield information that lets us cost your job accurately in advance.

Then we send you our logic, right?

Right. We take it through a logic restructuring and minimization, block out the functions from our CAD library and lay out the interconnections between logic blocks. Then we check it. And re-check it. Only then do we commit to fabrication.



Rick Picard, Director of Operations

How do we minimize risk with gate arrays?

Let's look at each of the risk elements that apply to any development work, and see how vulnerable you are by using gate arrays.

1. Reliability. Gate arrays are no more subject to reliability failures than any IC; actually, the regularity and repetition inherent in gate arrays improves their reliability. We use all the time-tested QC technology. Standard processing is used throughout.

2. Functionality. We use CAD to convert your logic into silicon. And we have only one layer to get right. Everything else is proven. We spot any problems fast. **It will work.**

3. Reliability of supply. Gate array technology lets us inventory pre-processed, ready-to-be-personalized wafers. We keep plenty of wafers on hand to support our customers' orders both for development and for production. Personalization, packaging and test are all performed in-house. We can promise 4–6 week delivery for production quantities. And costs of $.02 a gate or even lower.

Interested? TWX us! We'll TWX you complete information right away. Or write us at 3350 Scott Blvd., Building #37, Santa Clara, CA 95051. Tel. (408) 727-2280.

TWX: 910-338-2032

INTERNATIONAL MICROCIRCUITS INCORPORATED

Gate Array Leadership

Disposable Intelligence: Hand-Held Computers; and session 28 (Feb 26, 10:30-noon) will be a panel discussion on Software Mass Marketing.

Networks and Architecture

Under the architecture stem, session 1 (Feb 24, 1:30-3 pm) will consist of five papers on Local Networks; and session 5 (Feb 24, 3:30-5 pm) will be made up of five papers discussing Local Network Standards. Session 9 (Feb 25, 8:30-10 am) on Database Machine Architecture will feature three papers: Is There an Ideal Database Machine?; Utilizing Associative Array Memories in the Design of a Database Computer; and The Architecture of the IDM 500.

The following four papers will be presented in session 13, Data Flow Architectures (Feb 25, 10:30 am-noon): A Graphical Approach to Software Development Using Function Graphs; A File-Oriented Application Program for a Data-Driven Computer System; Dependence-Driven Computation; and An Instruction Set for the Processing Element of a Multiple-Processor Dataflow Machine. Attached Array Processors, session 17 (Feb 25, 1:30-3 pm), will present A VLSI Approach to the FFT; A New Approach to Vector Instructions; and Fast Sparse Matrix Computations.

Session 21 (Feb 26, 8:30-10 am) on Multiprocessor Systems Architecture will present papers on MP/C: Multiprocessor/Multicomputer Architecture, A VLSI Interconnection Network for Multiprocessor Systems, and Architecture of a Myriaprocessor. The papers to be presented in session 25 (Feb 25, 10:30 am-noon), Memory Management, are as follows: Fourier Analysis of Software-Cache Interactions; Virtual Memory Management for the Z9000; Design Philosophy of the 68000 MMU; and Address Translation and Mapping Reduce RAM Size Requirements.

Technology and Applications

Under the technology stem, more than 20 papers will be presented on advanced circuits, components, and devices. For instance, Semiconductor Memories in session 10 (Feb 25, 8:30-10 am) will be covered by the following papers: Large ECL Bipolar RAMs; High-Speed NMOS 16k Static RAM; 64k Dynamic RAM; and New Applications with E²PROMs. Papers on Gate Arrays and Programmable Logic, session 14 (Feb 25, 10:30 am-noon), will include Gate Arrays: A User Perspective; The Impact of Customized Gate Array Families on Custom Design; The Mask-and-Field Programmable Logic Design Revolution; Computer-Aided Design—The Engineering Interphase for Macrocell Array Circuits; and Automated Logic Arrays in a Custom Interface.

Other advanced technology programs will include session 18 (Feb 25, 1:30-3 pm), The New CMOS Microprocessor Era Is Dawning, with the following papers: P²CMOS Microprocessor Provides High Performance Solution to Low Power Applications; An 8-Bit Control-Optimized CMOS Microprocessor; and New CMOS 1800 Series Processors Reduce Chip Count. Session 30, titled Computer Aided Design Philosophy (Feb 26, 1:30-3 pm), will include Digital Systems as Mathematical Expressions; PRIM: a Placement and Routing Implementation System for Master-Slice LSI Chip Design; and CAD for Signal Processing. Fiber Optic Communications Systems will close the technology stem schedule as session 34 (Feb 26, 3:30-5 pm), with the following papers: Optical Fiber Makes Research Information Processing System; Minicomputer System Distribution by Optical Fiber Data Highway; Optic Fiber Data Freeway Systems—A Loop Network for Distributed Computer Control; and Impact of Terminal Device Design on Fiber Optic Local Area Networks.

The applications stem will start in session 3 (Feb 24, 1:30-3 pm) with several speakers presenting papers on Mini Winchester Discs. Papers to be delivered in session 15 on Recent LSI Implementations of Multiple-Valued Logic (Feb 25, 10:30 am-noon) are as follows: Recent Multiple-Valued Circuits; Multilevel NMOS Circuits; Multivalued Logic LSI Implementation Transmission; Use of 4-Valued Logic LSI Implementation in the 8087 ROM Cell; and Multiple-Valued Current Mode Integrated Circuits. Session 19, Intelligent Data Entry (Feb 25, 1:30-3 pm), will include the papers Dynamic Character Recognition: An Emerging Technology; Image Processing, Where It Begins and Where It Is Going; and Distributed Data Entry Using OCR.

Other applications discussions will include High Resolution Displays, session 23 (Feb 26, 8:30-10 am), with the following papers: Distributed System Design Discipline: An Application of Tell; Computer Graphics: Hardware and Technology Directions; and The GDS-2 System for Physical Design. Papers on Intelligent Instrumentation, session 31 (Feb 26, 1:30-3 pm), will cover HP 1980 Intelligent Scope; Network Analyzer for B-767; Computerized Blood Analysis; Arbitrary Waveform Generator; and Patient Diagnostics with Computer-Aided Instrumentation.

Registration

Advance registration must be received by February 13. IEEE members may remit their fee of $75 each for the conference and/or any one of the three tutorials; the fee for nonmembers is $100 for either the conference or a tutorial ($200 for both). Late registration, accepted at the Jack Tar Hotel beginning Sunday evening, February 22, will have an additional fee of $10 for either the conference or a tutorial, or $20 for both. Tutorial registration includes luncheon and preprinted notes. Conference registration includes a copy of the COMPCON *Digest of Papers* and two complimentary drink tickets for each of the conference-hosted parties on Tuesday and Wednesday nights. To register in advance, send name, organization name, address, and IEEE or IEEE Computer Society membership number, along with the proper registration fee (checks made payable to COMPCON Spring '81), to: Robert M. Long, Lawrence Livermore National Laboratory, Box 8080, L-72, Livermore, CA 94550. □

First compare quality. Then compare cost.

Morrow Designs' 10 megabyte hard disk system: $3,695.

MORE MEMORY. LESS MONEY.

Compare Morrow Designs' DISCUS™ M26™ hard disk systems to any system available for S-100 or Cromemco machines. First, compare features. Then, compare cost per megabyte. The M26 works out to under $200 a megabyte. And the M10 is about half the cost of competing systems.

COMPLETE SUBSYSTEMS.

Both the M10 (8″), and the M26 (14″), are delivered complete with disk controller, cables, fan, power supply, cabinet and CP/M® operating system. It's your choice: 10 Mb 8″ at $3,695 or 26 Mb 14″ at $4,995. That's single unit. Quantity prices are available.

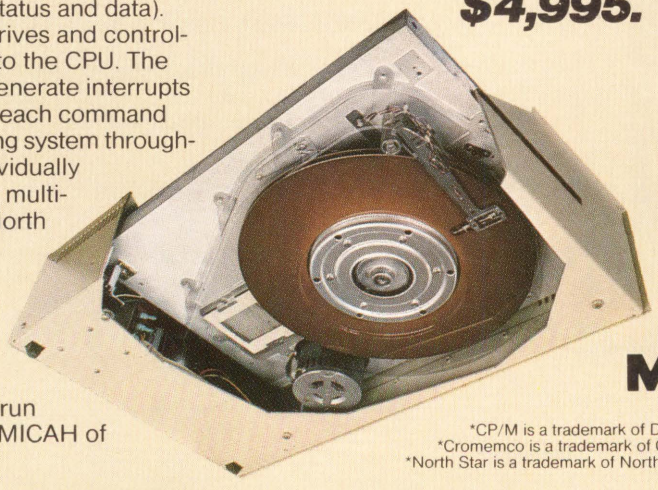
BUILD TO FOUR DRIVES.

104 Megabytes with the M26. 40+ megabytes with the M10. Formatted. Additional drives: M26: $4,495. M10: $3,195. Quantity discounts available.

S-100, CROMEMCO AND NORTH STAR.*

The M26 and M10 are sealed-media hard disk drives. Both S-100 controllers incorporate intelligence to supervise all data transfers through four I/O ports (command, 2 status and data). Transfers between drives and controllers are transparent to the CPU. The controller can also generate interrupts at the completion of each command ...materially increasing system throughput. Sectors are individually write-protectable for multi-use environments. North Star or Cromemco? Call Micro Mike's, Amarillo, TX, (806) 372-3633 for the software package that allows the M26 and M10 to run on North Star DOS. MICAH of Sausalito, CA, (415) 332-4443, offers a CP/M expanded to full Cromemco CDOS compatibility.

Morrow Designs' 26 megabyte hard disk system: $4,995.



AND NOW, MULT-I/O.™

Mult-I/O is an I/O controller that allows multi-terminal and multi-purpose use of S-100 and Cromemco computers. Three serial and two parallel output ports. Real time clock. Fully programmable interrupt controller. Designed with daisy-wheel printers in mind. Price: $299 (kit), $349 assembled and tested.

MAKE HARD COMPARISONS.

You'll find that Morrow Designs' hard disk systems offer the best price/performance ratios available for S-100, Cromemco and North Star computers. See the M26 and M10 hard disk subsystems at your computer dealer. Or, write Morrow Designs. Need information fast? Call us at (415) 524-2101.

Look to Morrow for answers.

MORROW DESIGNS

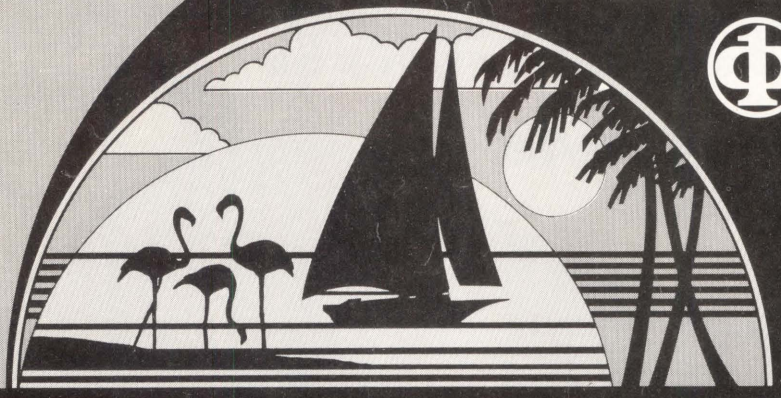
5221 Central Avenue
Richmond, CA 94804

*CP/M is a trademark of Digital Research Corp.
*Cromemco is a trademark of Cromemco, Inc.
*North Star is a trademark of North Star Computers, Inc.

CIRCLE 62 ON INQUIRY CARD

Advance Announcement . . .

Tutorial Week 81 EAST



General Chairman: Oscar Garcia, University of South Florida
Program Chairman: Russell E. Theisen, Martin Marietta
Local Arrangements: Joseph Massett, Martin Marietta
Donald Mendorf, Stromberg-Carlson
William Towles, Martin Marietta
Publicity: Louis Smith, General Telephone and Electronics
Jonathan Orlick, E Systems
Treasurer: Harry Hayman, IEEE Computer Society

A solid week of tutorials in 3 tracks • April 6–10, 1981

Attendance limited to 100 per tutorial. Advance registration only: deadline — March 9, 1981.

MONDAY, 4/6	TUESDAY, 4/7	WEDNESDAY, 4/8	THURSDAY, 4/9	FRIDAY, 4/10
① **VLSI from a User's Perspective** Rex Rice	② **Microcomputer System Design and Techniques** Carol A. Ogdin	③ **Microprocessor Interfacing Techniques** G. Jack Lipovski	④ **Interactive Computer Graphics** Herbert Freeman	⑤ **Computer-Assisted Design and Engineering** Stephen R. Levine
⑥ **An Overview of Networks and Distributed Processing** Burt H. Liebowitz	⑦ **Computer Communications Protocols** David C. Wood	⑧ **Computer Networks** Ira W. Cotton	⑨ **A Pragmatic View of Distributed Processing Systems** Harvey A. Freeman	⑩ **Local Computer Networks** Harvey A. Freeman
⑪ **Models and Metrics for Software Management and Engineering** Victor R. Basili	⑫ **Modern Programming Language Design** Anthony I. Wasserman	⑬ **System Analysis and Requirements Specification** Raymond T. Yeh	⑭ **Software Testing and Validation** Edward Miller	⑮ **Software System Design** Jack C. Wileden

ORLANDO MARRIOTT INN, ORLANDO, FLORIDA

Attendance limited to 100. Register NOW!
Select up to one tutorial per individual per day.

	Per Tutorial	All Week
FEES: Members	$85	$400
Nonmembers	$100	$475

Includes bound tutorial text and luncheon. There will be a no-host reception Monday night.

HOTEL ACCOMMODATIONS:
Reserve your room at the Marriott Inn now. Write to:

Orlando Marriott Inn
6700 Sand Lake Road
Orlando, FL 32807
Attn.: IEEE Tutorial Week

RATES: Single or Double: $50.00
with kitchen: $60.00

Mail to: Tutorial Week 81 East, Box 639, Silver Spring, MD 20901

☐ I am interested in the following tutorials (please circle numbers):
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Please mail me the complete program announcement.

☐ I want to register right now. Enclosed is $_____ to reserve space at the following tutorials (circle numbers as appropriate):
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

☐ Check enclosed ☐ VISA/BankAmericard ☐ Master Charge

Card No._____ Exp. Date_____ Signature_____

Name_____ IEEE or IEEE-CS Membership No._____

Street Address_____

City/State/Zip_____

IEEE COMPUTER SOCIETY®

CIRCLE 22 ON INQUIRY CARD

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.®

Add-in Reliability. Then Relax.

Our LSI-11* memory systems come with built-in ECC (Error Checking and Correction) circuitry. So you don't have to worry about expensive service calls, or strained relations with customers. Our 2,500 ECC systems in the field have a proven MTBF *in excess of 15 years.*

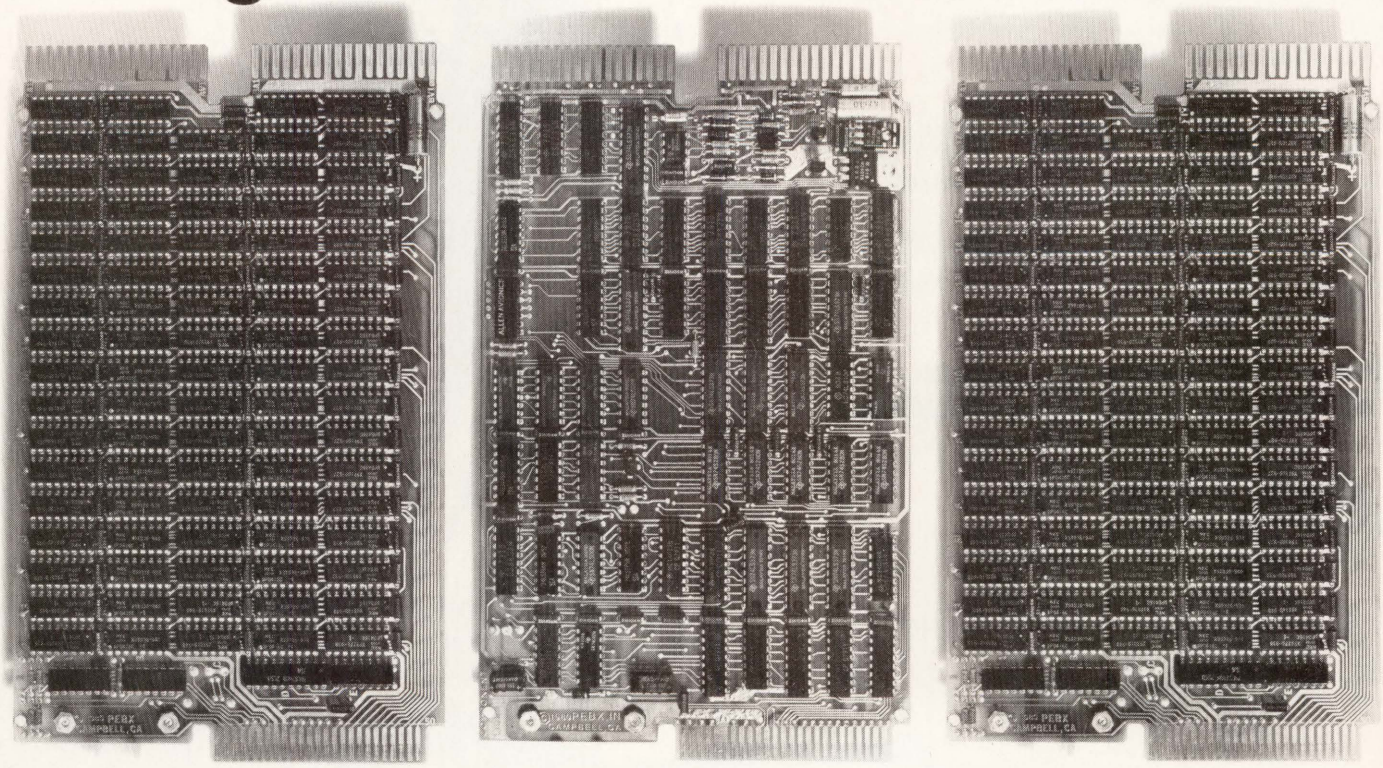
PEBX is the first to protect your LSI-11 system from failing RAMs and those random alpha particle crashes. We've also made protection from power outages as easy as hooking up a battery.

We'll give you from 32 to 256K bytes of error-correcting memory that takes care of all single-bit errors. Plus a display that points to any erring RAM, allowing *preventive* maintenance rather than finger-pointing after a system crash.

So if you're an OEM and you don't want to worry about costly service calls, find out about our add-in reliability and relax. *Contact PEBX toll-free today at (800) 538-3112. Within California phone (408) 866-7838 for full info on how you can get the best LSI-11 memory on the market.*

PEBX
501 Vandell Way
Campbell, CA 95008
(408) 866-7838

Finally: LSI–11 memories with ECC.



*LSI-11 is a registered trademark of Digital Equipment Corporation.

HERE'S WHY MONOLITHIC SYSTEMS IS WINNING THE SINGLE BOARD 8 BIT COMPUTER RACE

We make you more productive...

The MSC 8009* is a "REAL" Single Board Computer. Based on the Z80A® processor, with enough memory - 64K bytes of dual ported RAM and up to 32K bytes of EPROM - to handle most processing tasks on the internal bus. It contains a floppy disk formatter/controller, a choice of powerful APU's, prioritized vectored interrupts and extensive I/O. This total system solution is provided within a single MULTIBUS® card slot... reducing board count, increasing reliability and leaving the MULTIBUS free for system functions. And the MSC 8009 is supported by our extensive and growing line of system modules (ask for our catalog).

And, we put you on the right track for the future...

Monolithic Systems has combined industry standard elements to achieve an elegant computer system architecture... a Z80A processor, IBM floppy disk data format, a 9511/12 APU... all performing under the amazing CP/M®. This is the key to a universe of software that you can select from our catalog or from standard industry offerings. For multiuser or networking capability, MPM® and CP/NET® extends your system performance.

We respond to your needs...

We have a record of consistantly meeting the needs of our computer OEM's for over 10 years. And, when you have a special system requirement, we utilize that extensive experience to deliver a special solution. For applications assistance contact us at 14 Inverness Drive East, Englewood, Colorado 80112 or phone (800) 525-7661

Monolithic Systems means..... Technically advanced solutions

Monolithic Systems corp.

MSC Regional Sales Offices: Eastern Region
1101-B9 State Road, Princeton, NJ 08540, (609) 921-2240
Central Region 14 Inverness Drive East,
Englewood, CO 80112, (303) 770-7400
Western Region 49 South Baldwin, Suite D,
Sierra Madre, CA 91024, (213) 351-8717

*Single Unit Price $1895.00
MP/M, CP/NET and CP/M are trademarks of Digital Research Inc.
Z80A is a trademark of Zilog Corp.
MULTIBUS is a trademark of Intel Corp.

CIRCLE 64 ON INQUIRY CARD

32-BIT MINICOMPUTER ACHIEVES FULL 16-BIT COMPATIBILITY

Early architectural definition results in design of 32-bit minicomputer that offers full 16-bit compatibility without a mode bit

Steve Wallach
Chuck Holland

Data General
Route 9, Westboro, MA 01581

Designing a viable product for the competitive 32-bit minicomputer market requires a specialized approach that combines the latest semiconductor technology with a system organization capable of achieving the best possible performance. When the 32-bit minicomputer must offer full 16-bit compatibility without enforcing two distinct modes of operation, the specialized design approach becomes even more important. Conventional design techniques constrained in this way may lead to a tradeoff between performance and ease of implementation. However, by having implementers and architects interact in a top-down, goal driven design effort at the earliest phase of development, compromise of performance is avoided.

Undertaken over a 2-year period, the design of the ECLIPSE MV/8000™ involved cooperative implementation and architectural development. Critical elements of that process included the structure and functions of the design team; the basis for design decisions; an overview of the target system organization, particularly its instruction set; and the significance of specific architectural features. Important factors to be considered were the reasons for designing a 32-bit machine and the reasons for avoiding two complementary modes of operation.

As declining component costs enlarge the 32-bit technology market, other applications are developed and demand for these application systems steadily grows. The major advantage of the 32-bit machine is its ability to support a large logical address space for storing programs and data. Because of this, the design had to provide the largest possible address space constrained to 32-bit words—a 4G-byte size—and to allow use of the complete address space in the first implementation. Important to this part of the design was the concept of equating files with the address space, first developed under MULTICS[2]. Finally, because structure and organization of the address space strongly influence

system capability in a multiprogramming, multi-user environment, a major portion of the design effort dealt with the layout and management of the 4G-byte address space.

Compatibility through use of a mode bit is predicated on two mutually exclusive instruction sets with the constraint that only one instruction type can function at a time. Also, marketing considerations indicated the need for a 32-bit minicomputer that featured total compatibility with existing 16-bit software. Six years ago, instruction set extensions in the 16-bit ECLIPSE® computer achieved full binary compatibility with the 16-bit NOVA® computer, introduced more than 12 years before that, without resorting to the use of a mode bit. It therefore seemed prudent to use the same technique for extending to 32 bits. In addition, without a mode bit the 16-bit instruction set is not detachable, thus ensuring a continued commitment to software compatibility. This nondetachable instruction set results in binary compatibility with Advanced Operating System (AOS) programs based on the 16-bit ECLIPSE and allows 16-bit program development on the 32-bit ECLIPSE MV/8000 system. It also supports concurrent execution of 16- and 32-bit programs and permits mixing 16- and 32-bit subroutines (or individual instructions) within the same program.

To best accomplish the design of a 32-bit machine without a mode bit, the project team was divided into hardware and software implementation groups. Establishment of a cohesive team was just as important to the success of the project as technical judgments made during the design effort. Partitioning the design team into two groups instead of designating a committee of architects expedited definition of the overall hardware and software implementation. Since, ultimately, system implementers would have to conform to the overall hardware and software definition, design team members felt that intensive interaction at the earliest phases of the design effort was a prerequisite for implementation of the architecture. As will be shown, many architectural features of the instruction set were in fact influenced by the first implementation.

Suggestions for architectural enhancements and alternatives were evaluated as to their impact on hardware and software development schedules, the hardware resources needed to implement proposed features, their effect on performance, and perceived marketing needs. Although responsibility for final acceptance rested with the appropriate hardware or software team leader, suggestions were welcomed from all implementation team members and other technical personnel within the central engineering and software development groups.

Hardware Organization

Before final definition of the architecture, logic designers and microprogrammers on the hardware implementation team developed an overall system organization (Fig 1) based on a dual-port cache memory system, with the processor divided into four basic components handling input/output (I/O), main memory access, central processing, and system control (operator console, clock generation, etc). This system organization was chosen after a detailed system analysis had been done taking many factors into consideration. For example, handling of I/O data transfers involves block oriented (eg, disc based) operations that access main memory directly and require appropriate logic for detecting that a copy of the designated physical block resides in cache memory. It also involves single word transfers that require either buffering or partial read and write accesses to main memory. I/O buses transfer data in 16-bit words. The memory system in a 32-bit machine usually grants requests in integer multiples of 32 bits. Therefore, system organization had to make some provision for accessing data of less than 32-bit precision.

System organization also had to support extremely high bandwidth processor and I/O subsystems, both able to exceed 16M bytes/s. Furthermore, it was important to minimize the time for cache miss (cache fault) resolution. Most cache designs are optimized to give the highest possible hit rate (cache hits/attempts, or 1 – fault rate). While this is always desirable, the true measure of cache efficiency is the effective access time:

(hit rate) (cache access time)
+ (fault rate) (main memory access time)

Therefore, the interface between the cache and main memory had to be optimized to reduce the overhead associated with a cache fault. Ultimately, this goal necessitated the construction of a dual-port cache featuring an I/O port which exhibited characteristics of a general purpose 32-bit bus, and a central processor port. Other factors influencing system organization included a desire to minimize the interface between the I/O subsystem and the processor subsystem, the need to support a soft operator's console based on a video display, and the inclusion of sophisticated diagnostic subsystems.

Microsequencer Features Random Access Memory Control Store

Based on a random access memory (RAM) control store, the microsequencer contains the microcode that interprets ECLIPSE MV/8000 instructions. The microcode, which is organized as 4k by 75 bits for a 74-bit microinstruction with parity, generates control signals required by the other processor elements. Because the control store was designed using RAM, the microcode is reloaded from a 1.2M-byte diskette by the system control processor (SCP) each time the system is powered up.

The use of RAM achieves control store alterability, making microcode changes or updates easy to implement by simply replacing the diskette, and providing microdiagnostics. When a malfunction is suspected, microdiagnostics overlay the control store to give accurate fault isolation in a matter of minutes at a finer granularity than can be achieved using diagnostics based on standard machine instructions.

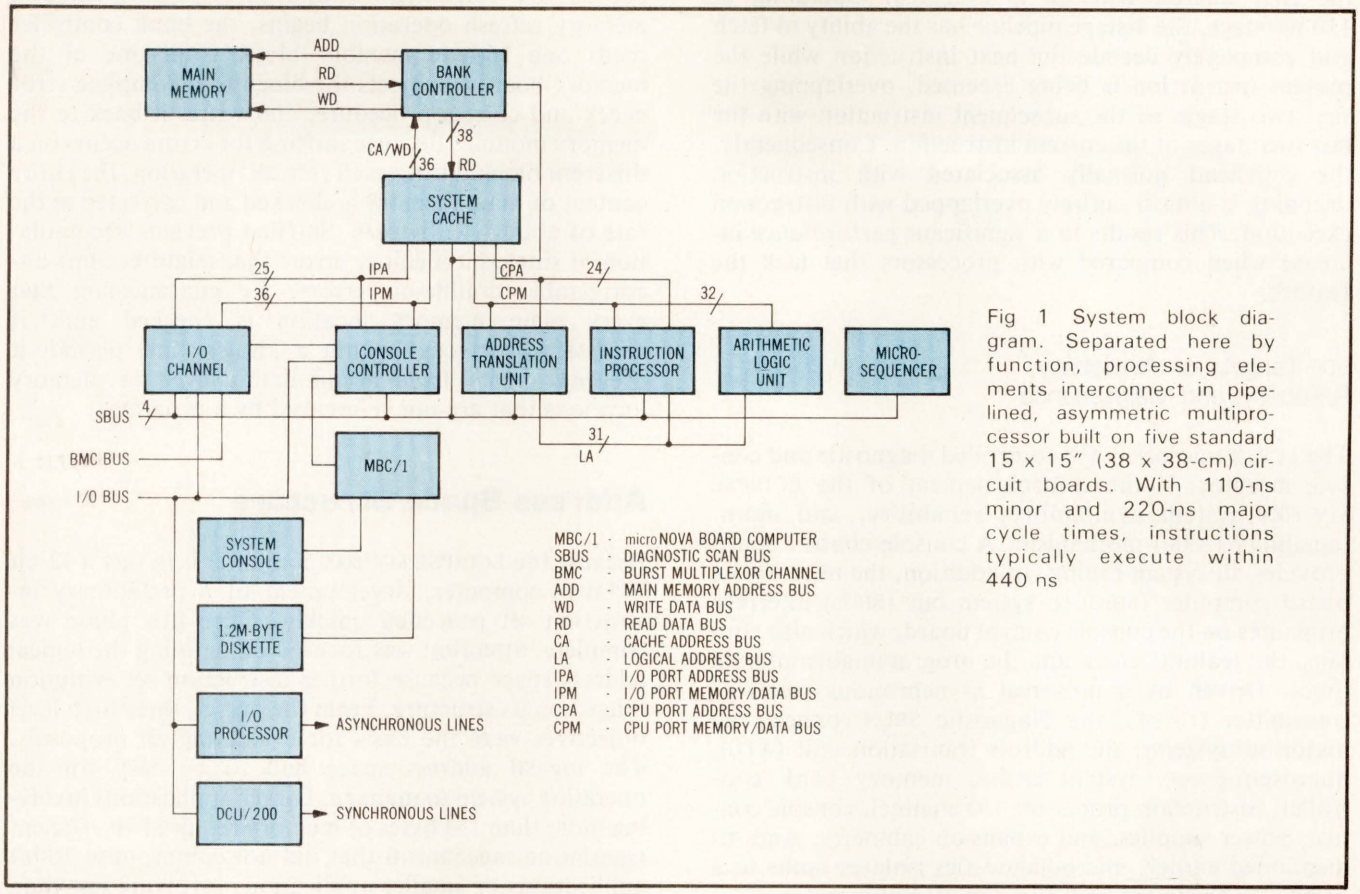


Fig 1 System block diagram. Separated here by function, processing elements interconnect in pipelined, asymmetric multiprocessor built on five standard 15 x 15" (38 x 38-cm) circuit boards. With 110-ns minor and 220-ns major cycle times, instructions typically execute within 440 ns

Programmable Array Logic Functionality Reduces Part Count

More than any other component type, programmable array logic (PAL) influenced the design, performance, and personality of the ECLIPSE MV/8000 system. This family of devices implements a programmable AND array that provides input to a fixed NOR array and has registered (D flipflop) and combinatorial versions packaged in 20-pin, 0.3" (0.8-cm), dual-inline packages. The use of PAL components began slowly. When designers started achieving a three- to fivefold reduction in parts count over the use of off the shelf, medium scale integration (MSI) components, PAL usage accelerated. Ultimately, more than 10% of all central processor parts were PAL components, distributed about 40, 30, and 30% among the 16R4, 16R8, and 16L8 part types, respectively. The ability to feed back registered PAL outputs internally motivated the high usage of 16R4 and 16R8 part types.

For the ECLIPSE MV/8000 computer, PAL proved to be the right idea at the time. Its high density package combines a high level of functionality with the potential for reduced parts count; hence, design modifications require only fuse changes and not changes to the printed circuit board etch. Additionally, PAL components are easy to use. Another interesting aspect of PAL emerges from an examination of the cases in which it was not used, cases when an off the shelf MSI design could be achieved at a lower cost, or cases when a PAL implementation would have been too slow. For example, a 16L8 has a propagation delay of 40 ns. In many cases, this was not sufficient to handle the worst case delay through the network. If PAL components with a propagation delay of 20 ns had been available, their use would have increased significantly.

Pipelined Instruction Decoding Improves Performance

Unique to the 32-bit minicomputer industry, the instruction processor, which decodes instructions for subsequent execution, contains a 1k-byte direct mapped instruction cache organized as a 64-block, high speed memory of 16 bytes/block. Because of its look ahead and look behind potential, the instruction cache speeds up program execution, particularly benefiting program loops and backward branches. Totally separate from the system cache, the instruction cache allows instructions and data to be fetched concurrently without interference.

Instruction cache output provides input to the instruction decoder. A high degree of pipelining allows instruction execution to proceed through four distinct stages. An instruction is fetched from the instruction cache, the instruction operation code is decoded to obtain the microcode starting address, the first

micro-instruction is read from this address, and finally, the first microinstruction is executed. Operating at 110 ns/stage, the 4-stage pipeline has the ability to fetch and completely decode the next instruction while the present instruction is being executed, overlapping the first two stages of the subsequent instruction with the last two stages of the current instruction. Consequently, the overhead normally associated with instruction decoding is almost entirely overlapped with instruction execution. This results in a significant performance increase when compared with processors that lack the feature.

SCP Targets on Availability, Reliability, and Maintenance

The SCP, a microNOVA™ controlled diagnostic and console monitor, is the control element of the ECLIPSE MV/8000 system availability, reliability, and maintainability (ARM) mechanism. A console control board provides all system timing. In addition, the microNOVA board computer (MBC) to system bus (SBUS) interface originates on the console control board, which also contains the realtime clock and the programmable interval timer. Driven by a universal asynchronous receiver/transmitter (UART), the diagnostic SBUS connects all major subsystems: the address translation unit (ATU), microsequencer, system cache, memory bank controller, instruction processor, I/O channel, console control, power supplies, and expansion cabinetry. And, as mentioned earlier, microdiagnostics isolates faults to a particular hardware board in a matter of minutes.

SCP power margining, used to stress logic components and isolate components that may be failing intermittently, is accomplished by increasing power by as much as 5% above normal or decreasing it by up to 10% of normal voltage. System clock margining serves three functions. By increasing the system clock to 120 ns, it permits the processor to operate reliably when logic boards are on board extenders and allows a component to function when it has degraded beyond performance specifications, a feature used by the diagnostics. By decreasing the system clock to 100 ns, it stresses logic components and helps to isolate intermittent component failures.

The SCP also regulates the ability to disconnect the instruction cache, system cache, and ATU address cache, allowing continued processing in a degraded mode of operation. In a modern, highly interactive, online application environment, ARM is as important as any of the critical system parameters, such as price or performance. To be effective, it must be tightly integrated into the design, not added at the last minute. Overall, the SCP control, diagnostic, and margining capabilities provide the required level of effectiveness and functionality to speed up maintenance and repair and minimize reasons for shutting down the system.

Sniffing Protects Memory Data

A sniffing mechanism reduces the likelihood of encountering uncorrectable multiple bit memory errors, thus greatly increasing data reliability. All memory boards are refreshed simultaneously. Each time a memory refresh operation begins, the bank controller reads one 16-byte memory block from one of the memory boards, subjects the block to a complete error check and correct procedure, and writes it back to the memory module. Because sniffing for errors occurs on a different block during each refresh operation, the entire content of main memory is checked and corrected at the rate of about 1M bytes/s. Sniffing prevents accumulation of single-bit memory errors that might become uncorrectable double-bit errors. By guaranteeing that every main memory location is checked and, if necessary, corrected within a known time period, it prevents errors from accumulating even in memory locations that are not referenced by a program.

Address Space Structure

Because the ECLIPSE MV/8000 computer is in fact a 32-bit ECLIPSE computer, development of a preliminary instruction set proceded quickly. Once this phase was complete, attention was focused on defining the logical address space because further instruction set evolution hinged on its structure. From the outset, three high level objectives were the basis for evaluating all proposals. The logical address space had to be easy for the operating system to manage. Larger applications involving more than 1M bytes of memory required an efficient translation mechanism that did not compromise 16-bit applications or smaller applications involving less than 1M bytes of memory. Sessions with customers whose needs surpassed the capabilities of a 16-bit machine revealed that relatively small programs in the 250k- to 500k-byte range were projected, especially in commonplace realtime environments. Finally, the operating system had to be embedded into the logical address space so that both systems and applications software would benefit from the address space extension.

When establishing memory management, the first step taken was choice of page size. A 2k-byte page was selected on the basis of the average file size under AOS, the page fault rates achieved by various other page sizes, the overhead incurred during page frame management, the working set size of a fixed entry ATU, and the effect of page size on the logical to physical translation mechanism. [3,4] (Fig 2 compares the page table overhead for 512- and 2k-byte page sizes.) This choice is an important one because the 2k-byte page also becomes the basic unit of memory protection. As will be shown, another consequence of this choice is that 2k bytes becomes the largest unit of contiguous physical memory under every logical address space size, which simplifies operating system design and requires maintenance of only one free page list. The selected page size immediately determines the 11 least significant bits in a 32-bit logical address, leaving the semantics of the remaining 21 bits undefined. The two fundamentally different approaches to interpreting these 21 bits were christened "flatlands" and "treelands" by the design team.[5]

The flatlands approach involved hashing the 21 high order bits of a logical address into a translation region

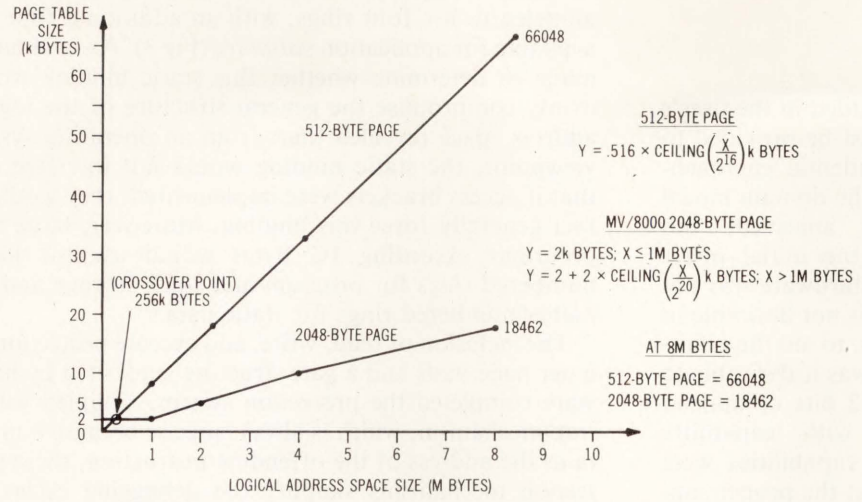


Fig 2 Page table overhead. Plot of overhead created during page frame management compares impact on performance of two candidate page sizes during logical to physical address translation

within physical memory. Acceptable performance required open addressing, linear probing with a 50% load factor on the bucket size. This would have resulted in an average of 1.5 probes for a cache hit and an average of 2.5 probes for a cache fault.[6]

The treelands technique, the one ultimately implemented, used a more traditional page table approach. In this form of logical address translation, a table constructed in main memory maps logical addresses into physical addresses. Each page table entry supplies various flags and, if appropriate, the physical address that corresponds to a logical address. With the selected page size of 2k bytes, it was assumed that four bytes would be sufficient for physical address information, and the page table, therefore, would have 512 entries.

Performance was the determining factor behind the choice of a page table approach. In view of the expected page fault rate, the two memory references needed to resolve address translation using the hashed technique, and the performance characteristics of the processor microarchitecture, the page table exhibited better performance than a hashed index. Had the logical address required a 3-level lookup, the hashed approach would have been more efficient.

Because of its structure, the page table requires a 9-bit index. Two such indexes are used to construct 18 of the 21 logical address bits that remain unresolved after taking the page offset into consideration. Since use of a third, 3-bit page index field was considered wasteful, the remaining three bits reference one of eight segment registers maintained within the processor.

The treelands approach was further optimized in two ways. One permits a 1-level translation for those programs that use less than 1M bytes on a segment basis, with a bit in the segment base register denoting either a 1- or a 2-level translation. The other adds validity bit interpretation in each page table entry for segment boundary protection against out of bounds references. Because a page is allocated to each page table, it is not necessary to define segment length registers. Instead, AOS/VS, the 32-bit operating system that manages MV/8000 resources, simply marks as invalid any page table entry that maps an undefined portion of the logical address space.

Studies by Belady and Hatfield show that complete support of referenced bits is important to the efficient management of a large virtual address space.[7,8] Three alternative locations for these bits were considered: the page table entry associated with the page in main memory, the part of the machine state attached to each page frame of the physical address space for the implementation, and a table associated with the process currently running. Each alternative was analyzed in relation to the time needed for software to access the referenced bits (ie, the work factor associated with the page replacement algorithms), the impact on the present and future implementations, and the effect on performance and design of the system data and address cache accelerators. Associating referenced and modified bits with the machine state, similar to the method used in the IBM 370, proved best.[9] The availability of high density static RAM and the ease of defining special instructions to accelerate page replacement were major determining factors, as well as the simplification of the ATU, which then need only be read with respect to main memory.

Privileged instructions were next defined to manipulate referenced and modified bits. One group of instructions permits each referenced and modified bit of a page frame to be examined individually. The other allows referenced bits to be treated as a bit string. The OR Referenced Bit (ORRB) instruction can perform the inclusive OR of a string of referenced bits and a string in main memory, resetting the accessed bits to zero. This approach helps the operating system maintain referenced bit strings easily on a per process basis, using the standard set of bit string instructions (count bits, locate first bit, etc) for string analysis. Various

algorithms maintain multiple bit strings per process to simulate reference counts greater than one.

Address Space Protection

Because the operating system is embedded in the user's context, some form of protection must be provided to detect and prevent malicious or accidental encroachment into the system address space. The domain model and the capabilities model were analyzed, but capabilities were eliminated during the initial phase because the complexity of the added hardware was not commensurate with the return.[10] It was not desirable to restrict capabilities to special segments, to aid the granting and revocation mechanisms, nor was it desirable to expand the logical address beyond 32 bits or append tags to each memory location with capability potential.[11] This is not to say that capabilities were undesirable in their own right, but that the proper support mechanism seemed to be beyond the scope and objectives of the project.

The domain model was narrowed to a hierarchical approach using one of the possible ring implementations. Since either a logical address or an integer can occupy an accumulator, and most instructions do not distinguish between integers and addresses, the MULTICS model could not be used directly. Two alternatives were considered: binding the ring number to the address space, and defining a ring register to be maintained separately. The first abstraction was chosen to eliminate the need for an extra machine state requiring protection, to permit the same instructions used for subroutine calls and returns to be used for cross-ring operations, and to add to the efficiency of Trojan horse pointer detection.

With the decision to bind the ring number in the address space, the number of rings had to be specified. In its early design phases, the operating system was modeled to use four rings, with an additional four left available for application software (Fig 3). An evaluation made to determine whether this static binding would overly compromise the general structure of the logical address space revealed that, from an operating system viewpoint, the static binding would not interfere and that if access brackets were implemented, they would in fact generally force this binding. Moreover, large user programs exceeding 1G bytes would use the lower numbered rings for program and stack storage and the higher numbered rings for static data.

The inclusion of read, write, and execute protection on a per page basis and a gate structure supported by hardware completed the protection system. Coupled with a trap mechanism, which is always precise because it maintains the address of the offending instruction, these protection mechanisms simplify the debugging cycle and generally abort runaway programs instantly. The gate array, defined for each ring, permits a called routine to designate the number of gates and an access bracket for each gate during all inner ring calls (Fig 4). Valid cross-ring calls, complete with stack switching and construction of a new frame on the target stack, take about 6.6 μs, without requiring software intervention. This level of effort directly supports the objective of processing operating system calls quickly and efficiently.

Instruction Set

Standard 16-bit ECLIPSE and NOVA computers, instructions form the basis for the ECLIPSE MV/8000 instruction

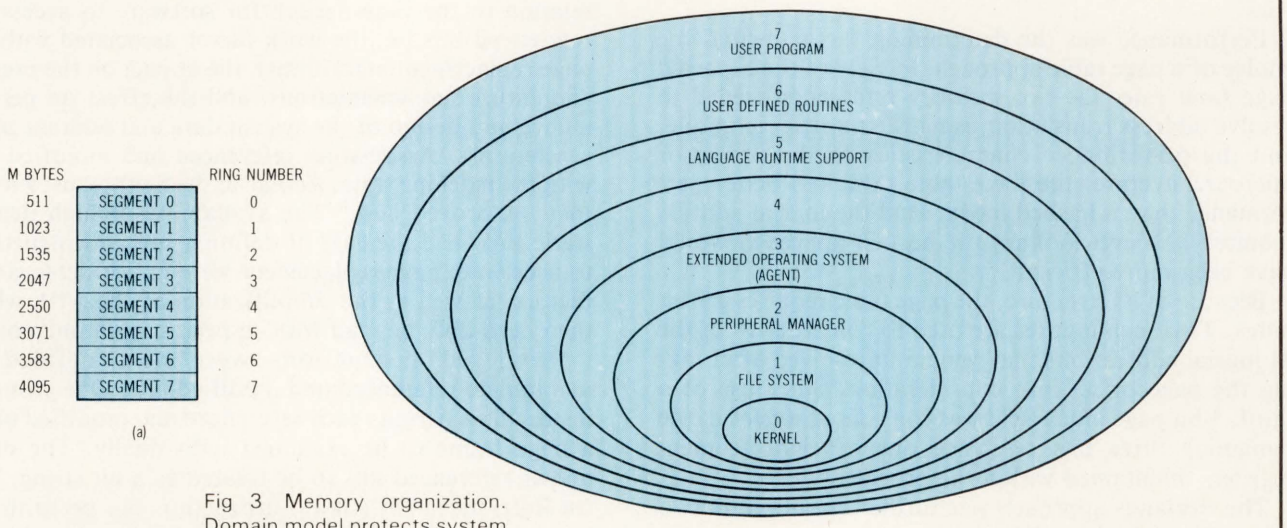


Fig 3 Memory organization. Domain model protects system address space by defining segment boundaries shown in (a). Then, in (b), AOS/VS hierarchical software system structure assigns memory segment and category or layer of software to each ring

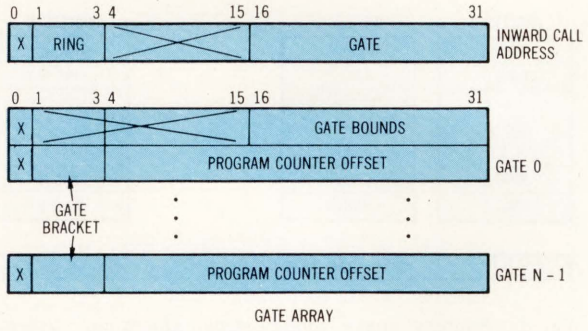


Fig 4 Gate mechanism. Called routine designates number of gates and access bracket for each gate during inner ring calls. Valid intra-ring calls execute in 6.6 μs, including stack management overhead. Both processes enhance operating system performance

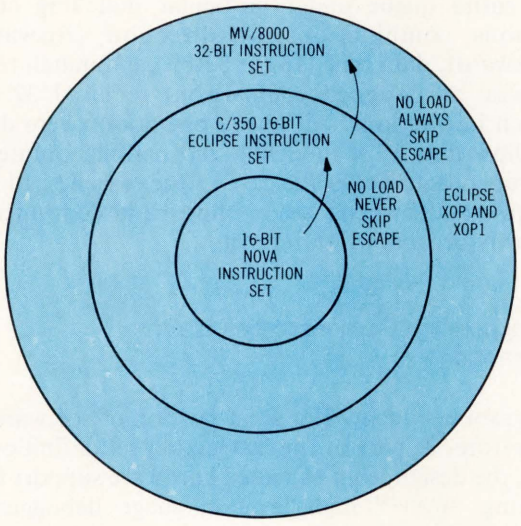


Fig 5 Hierarchical instruction set relationships. To achieve hierarchical mode-free instruction set, MV/8000 extends ECLIPSE instruction set to handle 32-bit accumulators and 4G-byte address space. New instructions use ECLIPSE no load, always skip, escape category in the same way ECLIPSE instruction extended NOVA no load, never skip, escape category

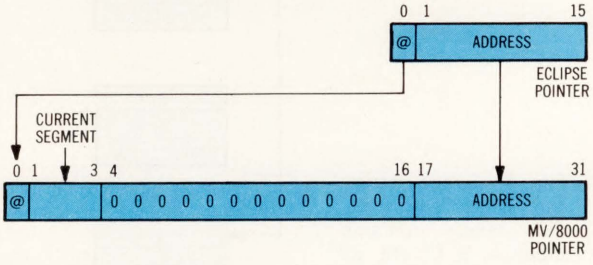


Fig 6 Pointer relationships. To dynamically map 16-bit address space into 32-bit address space without loss of performance, all 16-bit addresses are constrained to reference the first 64k bytes in segment

set. Extensions to manipulate the 32-bit address space and the 32-bit fixed point accumulators, and to expand general purpose functionality, are achieved by defining a new instruction class using the no load, always skip, binary encoding of the ECLIPSE ALC instructions (Fig 5). Four 16-bit accumulators are expanded to 32 bits, with their least significant 16 bits serving for 16-bit operations. Interpretation of fixed point data as 2's complement numbers accounts for this arrangement. Expanded to 31 bits, the program counter (PC) references memory at a 16-bit word granularity. The four 64-bit floating point accumulators (FPACs) are identical to those in the ECLIPSE computer. FPACs contain only floating point data—never addresses data—hence no reinterpretation is needed. Expanded from 32 to 64 bits, the floating point status register contains the 31-bit floating point program counter, which is a copy of the PC when a floating point fault occurs. This ensures that floating point faults are always precise and independent of the pipeline or overlapped nature of floating point computations. Two additional machine state structures enhance efficiency and fault handling capability: a 16-bit processor status register and four 32-bit stack management registers.

In the 16-bit ECLIPSE computer, a stack pointer, stack frame pointer, and stack limit maintained in hardware assigned memory locations manage the stack. Four 32-bit registers manage the ECLIPSE MV/8000 stack: a stack base register for detection of stack underflow, a stack limit register to detect overflow, a stack pointer, and a frame pointer. These parameters migrated into registers for performance reasons. The 16-bit processor status register (PSR) contains the flags used for integer overflow interpretation. One flag, OVR, signals that overflow has occurred. The other flag, OVK, is used as a mask to initiate or suppress the integer trap mechanism. Remaining bits are reserved for future hardware augmentation.

Following preliminary instruction set definition came the design of the logical address space structure; once that was completed, instruction set definition resumed. However, one final attribute of compatibility remained unresolved: mapping the 16-bit address space into the 32-bit address space. This was achieved by constraining a 16-bit address to the first 64k bytes of each segment (Fig 6), which permits efficient AOS/VS management of 16-bit processes running concurrently with 32-bit processes and allows instructions that generate 16-bit addresses to be interspersed with instructions that generate 32-bit addresses in the same program.

Language Viewpoint Attains Symmetry

Language related and system related constraints divided the instruction set definition process into two areas that were by no means mutually exclusive but are best discussed separately because each has different objectives. From a high level language viewpoint, the objective was to make the instruction set symmetrical with respect to all relevant data types. Consequently, all memory to accumulator and accumulator to accumulator instruction types apply to the baseline 16-and

32-bit integer data types and the baseline 32- and 64-bit floating point data types. Additional instructions provide a rich repertory of immediate operations, comparisons, shifts, memory to memory increments and decrements, logical and Boolean bit strings, byte and byte string manipulations, and sophisticated transfer of control (including CASE and DO WHILE constructs). Addressing uses the standard ECLIPSE computer modes: absolute, PC relative, and indexed through an accumulator.

System Viewpoint Adds Capability

From an operating system viewpoint, the most important instruction attributes are not the instructions per se but the capabilities of individual memory reference instructions to manipulate user data bases directly in a secure, efficient, and reliable manner. Once these attributes were firmly established, effort concentrated on providing instructions that could replace sequences of repetitive operations. The first step was to identify an instruction set to properly manipulate machine state constructs defined for the 32-bit logical address space. This involved the segment base registers (SBRs) and the referenced bits and modified bits maintained by the hardware.

Approached from an operating system perspective, the 4G-byte logical address space is divided into two regions: a system wide 512M-byte kernel and a process or user wide 3.5G-byte region (Fig 7). Directly supporting this abstraction, the Load All SBR (LSBRA) instruction purges the entire ATU, and the Load Some SBR (LSBRS) instruction effectively purges the ATU of entries associated with segments 1 to 7, inclusive. ATU purging is needed to avoid associating the user logical address of the currently executing process with the translation context of a previously executing process.

Another class of instructions deals specifically with the referenced and modified bits. Many iterations, some of which followed performance measurements on an engineering prototype, led finally to the concept of treating referenced bits as a group of 16-bit (rather than binary) strings. The 16-bit string structure reduces the page replacement overhead by about 70%. It is noteworthy that without the alterable RAM based microsequencer changes of this magnitude could not have been accomplished so late in the development cycle.

Once AOS/VS coding was under way, operating system designers requested a comprehensive set of queue handling instructions. Their request was based on efficiencies in code density; performance in the scheduling and resource management modules; and reduced interrupt latency, an important realtime parameter that measures the delay in honoring an interrupt request. AOS/VS uses a priority queue model. It has only one physical queue; however, areas within the queue are grouped by priority level (Fig 8). Therefore, insertions are necessary not at the beginning or the end of the queue, but only relative to a specified queue element.

Two types of queue instructions were defined to meet efficiency and performance goals. One permits queue

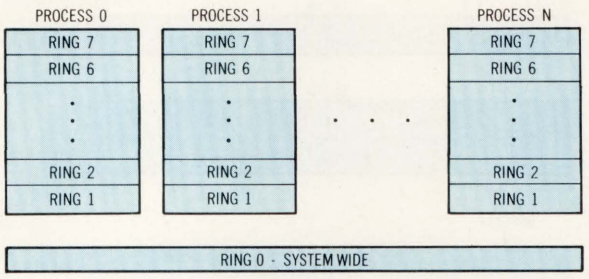


Fig 7 Address space relationships. Operating system divides 4G-byte memory space into two segments. System context occupies 512M-byte kernel region. Individual process contexts occupy remaining 3.5G-byte user region

insertions and deletions, and the other permits searching the entire queue under particular matching criteria. Various combinations of direction (forward or backward), data type (16- or 32-bit) and match relation (bitwise or unsigned comparison) required 32 queue search instructions. All queue operations were defined to allow linked list modeling and permit noninterruptible operations or, in the case of the searches, to return unique results when a search must be discontinued temporarily because of an interrupt.

Breakpointing Demonstrates Design Interaction

Program debugging is a great portion of software cost. Therefore, as part of the instruction set definition process, the design team provided hardware support for the existing SWAT™ high level language debugger, one which assumes that a breakpoint instruction can replace the first 16 bits of any other instruction. Breakpoint

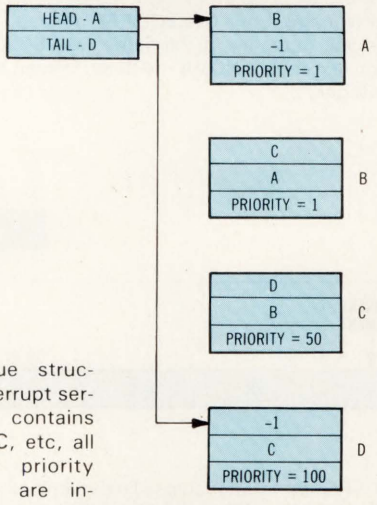


Fig 8 Queue structure. One interrupt service queue contains areas A, B, C, etc, all grouped by priority level. Items are inserted into appropriate area; therefore, they need not enter queue at beginning or end. Instead, special instructions position new items relative to queued items and also search queue under match criteria

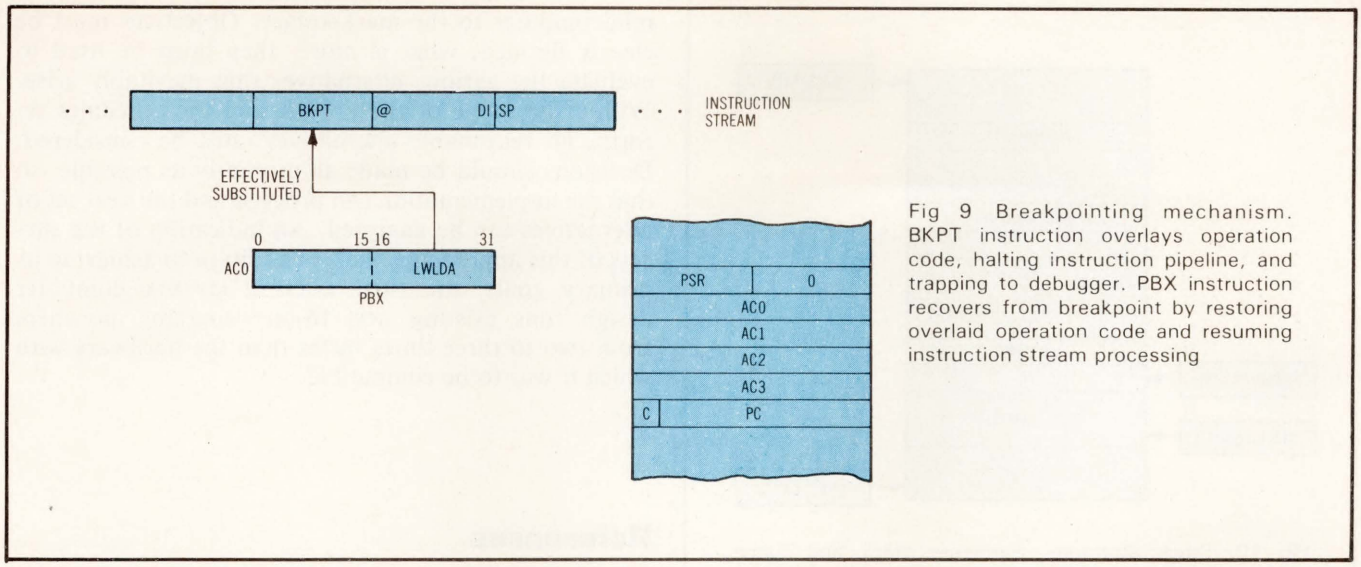


Fig 9 Breakpointing mechanism. BKPT instruction overlays operation code, halting instruction pipeline, and trapping to debugger. PBX instruction recovers from breakpoint by restoring overlaid operation code and resuming instruction stream processing

(BKPT) instructions are constrained to be exactly 16 bits long. Moreover, they must provide a trap address referencing the first instruction of the trap handler. In keeping with the overall system trap concept, a page 0 trap handler location was defined within the first 512 bytes of each segment so that each process and/or ring could have its own debugger.

Complementing the BKPT instruction, the Pop Block and Execute (PBX) instruction effectively restores the breakpointed instruction opcode, substituting it for the BKPT opcode (Fig 9). Superficially, this instruction pairing seems straightforward and easy to implement. However, during the prototype debugging phase, deleterious side effects of the initial instruction definition and implementation became apparent. One side effect was the potential to return to a deleted breakpoint: when a BKPT instruction was removed and replaced with the actual opcode, the debugger still returned to the user program by means of a PBX instruction which, of course, by then would not work. The instruction processor, being pipelined and operating asynchronously with respect to the ALU, proceeded to decode the next three macroinstructions. Thus, the 16-bit opcode was substituted over the wrong instruction. Because instruction processor interpretation of the BKPT instruction stops the pipeline, this problem was not encountered for PBX instructions correctly paired with BKPT instructions. To correct the first side effect, the PBX instruction was redefined with the restriction that the 16-bit opcode actually fetched from the instruction stream and used as the target of a PBX must be a BKPT instruction. In this way, a policy decision eliminated the problem.

A more complicated side effect involved making the BKPT and PBX instructions work properly for breakpoints that could tolerate page faults or interrupts (eg, breakpoints during string move operations). Under some circumstances, a page fault during execution of the PBX target instruction caused execution of the BKPT instruction, after the page fault was resolved, when the PBX target instruction should have been executed. This resulted from methods used to load and restore state information on the user stack.

Implementation group members who were committed to the desirability of these debugging features formed an ad hoc team that devoted considerable energy to either properly designing the microinterpreter for this instruction pair, or eliminating the pair altogether. Because these side effects were detected late in the design cycle, an immediate solution was necessary. A reasonable and effective solution was found, one that did not further affect the instruction definition process. This solution serves as a clear example of how a first implementation can and will affect instruction set architecture.

Precise and Compatible Subroutine Handling

The 16-bit ECLIPSE computer directly supported a powerful stack mechanism that handled the stack pointer, frame pointer, and stack overflow. In the ECLIPSE MV/8000 computer, the 32-bit stack was expanded to include stack overflow and underflow detection and complete cutback of a stack frame—including passed arguments—via only one instruction, a RETURN. The 32-bit stack typically supports subroutines invoked through the CALL instruction, if one or more arguments are passed, or by means of a Jump to Subroutine (JSR) instruction, if no arguments are passed on the stack. Ultimately, the same stack frame is built in each case, and the same instruction is used for the return (Fig 10).

Precise calling conventions were desirable from two vantage points. In one case, studies revealed that the execution time for subroutine call and return instructions represents a significant portion of overall program execution time, even in highly computational floating point operations, making a fast and efficient mechanism desirable. In the other case, it was mandatory to support a 32-bit common runtime library patterned after the structure successfully developed for the ECLIPSE computer. In fact, the ECLIPSE MV/8000 computer's call, save, and return mechanism supported by the hardware accurately mimics this convention.

One noteworthy aspect of stack support is the attention given to proper handling, identification, and

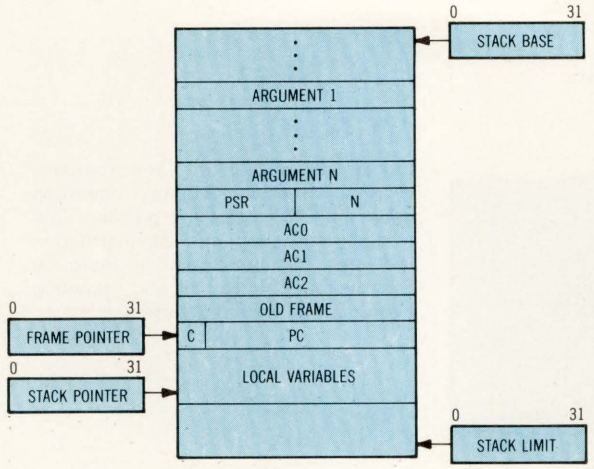


Fig 10 Stack structure. Hardware stack and frame pointers manage stack. Hardware base and limit registers detect overflow and underflow, trapping to user routine in either case. Subroutine CALL instruction passes arguments and constructs stack frame. JSR instruction builds stack frame without passing arguments. All structures support calling conventions of common runtime library

recoverability of stack faults. A test is made for stack overflow upon every operation that pushes an item onto the stack. During every operation that pops an item from the stack, a test is made for stack underflow. When a stack fault is detected, a trap occurs by vectoring through a location in page 0 of the current segment; thus, the user program—not the operating system—handles the trap.

Summary

Hardware and software implementation and architectural aspects of the ECLIPSE MV/8000 computer project give unique insights into the technical and organizational requirements for bringing a successful 32-bit minicomputer to the marketplace. Objectives must be clearly defined; what is more, they must be used to evaluate the various alternatives that inevitably arise. Within the scope of the project and the schedules set forth, all reasonable alternatives must be considered. Decisions should be made as promptly as possible, so that the implementation can proceed and the next set of alternatives can be analyzed. An indication of the success of this approach is that, in addition to achieving its primary goals, the final ECLIPSE MV/8000 computer design runs existing AOS 16-bit programs anywhere from two to three times faster than the hardware with which it was to be compatible.

References

1. ECLIPSE MV/8000, microNOVA, and SWAT are trademarks of Data General Corp, and ECLIPSE and NOVA are registered trademarks.
2. E. I. Organick, *The MULTICS System: An Examination of its Structure,* MIT Press, 1972
3. "Introduction to the Advanced Operating System (AOS)," 093-000121, Data General Corp, Westboro, Mass
4. W. W. Chu and H. Opderbeck, "Performance of Replacement Algorithms with Different Page Sizes," *Computer,* Nov 1974, pp 14-21
5. R. Morris, "Scatter Storage Techniques," *Communications of the ACM,* Jan 1968, pp 38-43
6. D. E. Knuth, *The Art of Computer Programming: Sorting and Searching,* vol 3, Addison-Wesley, 1973
7. L. A. Belady, "A Study of Replacement Algorithms for Virtual Storage Computers," *IBM Systems Journal,* vol 8, no 2, 1966, pp 78-101
8. D. J. Hatfield, "Experiments on Page Size, Program Access Patterns, and Virtual Memory Performance," *IBM Journal of Research and Development,* Jan 1972, pp 58-66
9. "IBM System/370 Principles of Operation," GA22-7000, IBM Corp, Poughkeepsie, NY
10. J. H. Saltzer and M. D. Schroeder, "The Protection of Information in Computer Systems," *Proceedings of the IEEE,* Sept 1975, pp 1278-1308
11. R. S. Fabry, "Capability-Based Addressing," *Communications of the ACM,* vol 17, no 7, July 1974, pp 403-412

About the Authors:

Steve Wallach, now the staff specialist involved with advanced system development for the ECLIPSE MV/8000 system, was principal architect for that system and manager of advanced development for ECLIPSE systems. He received a BSEE from the Polytechnic Institute of Brooklyn, an MSEE from the University of Pennsylvania, and an MBA from Boston University.

Chuck Holland, a design engineer, has headed the microcode development group for the ECLIPSE MV/8000 and participated in the development of the system's architecture and design. At present, he is working with an advanced development group. He received a BS and an MSEE from Georgia Tech.

Introducing high performance storage for any micro. Ready to roll.

Digital's new TU58-EA will change the way you use tape storage.

Because it combines the convenience and cost advantages of a ready-to-roll tape cartridge, with the performance advantages of random accessing.

The TU58-EA is a compact table-top package, complete with power supply and EIA interface, ready to hook up to any computer.

And it has a built-in MPU that makes it think like a disk. Instead of handling data serially like other tape systems, the TU58-EA reads, writes and searches for data in blocks. So you can use it in more time-critical applications.

We also offer two unpackaged versions for greater design flexibility: the single-drive TU58-AB, and dual-drive TU58-BB. Both offer universal EIA interfacing.

High performance storage is just one of the ways Digital makes microcomputers easier to work with. We offer hundreds of hardware products to choose from. Boards, boxes, and development systems. Memory and interface boards. Terminals and printers. With the widest selection of powerful, proven software in the industry.

All backed by Digital's support group of over 14,000 people worldwide.

It's the total approach to micros, only from Digital.

For more information call our toll-free LSI-11 Hotline at **800-225-9220.** (In MA, HI, AK and Canada, call 617-467-7000.) Or send the coupon.

Digital Equipment Corporation, MR2-2/M65, One Iron Way, Marlboro, MA 01752. In Europe: Digital Equipment Co. Limited, Acre Rd., Reading, RG2 OSU, England. In Canada: Digital Equipment of Canada, Ltd. Or contact your local Hamilton/Avnet distributor.

☐ Please send more information on the TU58 family.
☐ Please have a Sales Representative call.

Name_____

Title_____

Company_____

Address_____

City_____ State_____ Zip_____

Telephone_____

My application is_____

Send to: **Digital Equipment Corporation,** MR2-2/M65, One Iron Way, Marlboro, MA 01752.
DEC-C-156 O-1-O

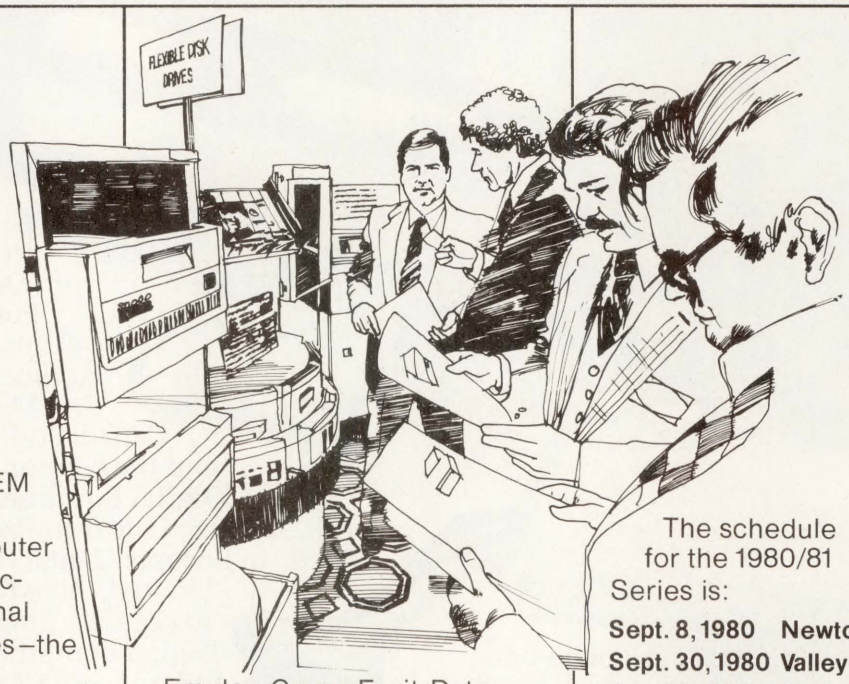
digital

We change the way the world thinks.

CIRCLE 65 ON INQUIRY CARD

OEM America Meets

At The Invitational Computer Conferences



In Boston
...in Ft. Lauderdale
...in Palo Alto and
seven other cities, OEM decision-makers meet the country's top computer and peripheral manufacturers at the Invitational Computer Conferences–the only seminar/displays designed specifically for the unique requirements of the quantity user.

In one day, at each 1980/81 ICC, guests will receive a concentrated, up-close view of the newest equipment and technology shaping our industry. Some of the companies which participated in the 1979/80 ICC Series were: ADDS; AVIV Corp; Applied Data Communications; BASF Systems; Cambridge Memories, Inc.; Centronics; Century Data Systems; Cipher Data Products; Compugraphic; Computer Devices; Control Data Corp.; Data Systems Design; Dataproducts Corp.; Dataram; Datasystems Corp.; Diablo Systems; Documation; Emulex Corp.; Facit Data Products; Florida Data; Hewlett-Packard; International Memories, Inc.; Kennedy Company; Lear Siegler; MDB Systems; MFE Corp.; Microdata; Monolithic Systems; Mostek; NEC Information Systems; National Semiconductor; Olivetti; Perkin-Elmer Memory Products; PerSci, Inc.; PCC/Pertec; Pioneer Magnetics; Plessey Peripherals; Powertec; Priam; Printronix; Remex; Rianda Electronics; Scientific Micro Systems; Shugart Associates; Siemens; Storage Technology; TEC; Tally Corp.; Teletype; Telex Computer Products; Texas Instruments; Trilog; Universal Data Systems; Versatec; Xylogics.

The schedule for the 1980/81 Series is:

Sept. 8, 1980	**Newton, MA**
Sept. 30, 1980	**Valley Forge, PA**
Oct. 22, 1980	**St. Louis, MO**
Nov. 18, 1980	**Palo Alto, CA**
Jan. 13, 1981	**Orange County, CA**
Feb. 3, 1981	**Ft. Lauderdale, FL**
Feb. 5, 1981	**Atlanta, GA**
Mar. 3, 1981	**Dallas, TX**
Mar. 5, 1981	**Houston, TX**
Apr. 2, 1981	**Denver, CO**

Invitational Computer Conferences

Invitations are available from participating companies or the ICC Sponsor.
For further information contact:
B.J. Johnson & Associates, Inc.
2503 Eastbluff Drive, No. 203
Newport Beach, CA 92660
(714) 644-6037

CIRCLE 66 ON INQUIRY CARD

A new measure of protection from AIRPAX

AIRPAX has the smallest, most compact line of magnetic circuit breakers available. They give the same ON-OFF power switching and reliable protection as much larger competitive units. PUSH-PULL and PUSH-TO-RESET designs have evolved from the well-proven SNAPAK® Circuit Protector. All have the patented snap-action mechanism which increases operational life by as much as five times. Operator "teasing" of the contacts has been eliminated and arcing is minimized.

SNAPAK Circuit Breakers will operate at either DC, 50/60Hz or 400Hz and are especially designed for panel mounting. The PUSH-TO-RESET has a position indicator and prevents accidental shutoff.

AIRPAX has a complete line of circuit breakers to serve your needs. Write or call us today for our new short form catalog. AIRPAX/North American Philips Controls Corp., Cambridge Division, Woods Road, Cambridge, MD 21613, telephone (301) 228-4600.

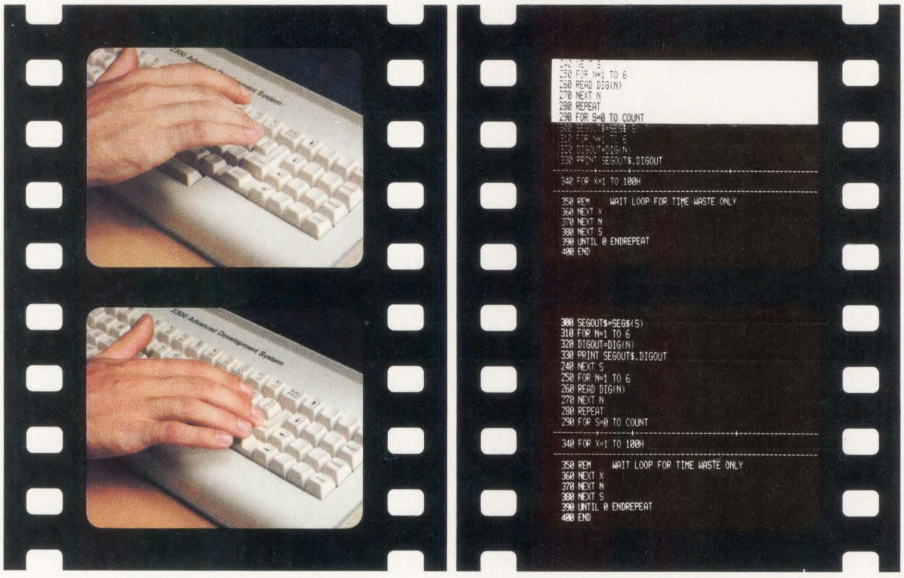
AIRPAX®

NORTH AMERICAN PHILIPS CONTROLS CORP.

Cambridge Division

CIRCLE 67 ON INQUIRY CARD

The speed of our system lowers your real product development costs...



real fast

There are many good reasons why you should consider our development systems for implementing your smart-product designs. Universality . . . compatibility with the newest 16-bit devices . . . upgradeability to multi-user networks . . . and our unexcelled slave emulation support are solid reasons why a GenRad system is your best buy. But don't overlook the speed, the ease-of-use and the versatility we've built into the 2300 series.

These are the factors that can do the most to lower your real product development costs. By speeding up the circle of design (editing, assembling, linking and debugging). Helping you bring products to market before your competitors. Helping you meet more of your design goals. Helping you work smarter, not harder. Compare us! After you've seen our demonstration, you'll know why.

You've got to see our hard disk/floppy disk manager with "wild card" file names. Our screen-based editor will astound you with its speed, full program scrolling, find/replace, block move and file merge features. Our relocatable macro-assemblers, high level languages and in-circuit emulation with symbolic debugging have to be seen to be appreciated.

We've kept things simple and fast. Easy-to-learn but sophisticated. Our operating system is menu driven. Complex commands have auxiliary "help" displays to reduce reliance on reference cards. With our command file processor you can create your own higher level operating system. With a single command you can execute the most complex programs, again and again, without repeating redundant, time-consuming instructions. It's so fast, our system will be waiting for you . . . not the other way around.

Remember this. Helping you build smarter smart products is just part of our commitment. Helping you do it faster and at less cost is just as important.

Ask for a demonstration.

Visit us at SOUTHCON Booth No. 658.

GenRad 2300 Series Stand-Alone Universal Development System. Supported processors: 8080, 8085, Z-80, 6800, 6802, 1802; the 8086, 68000, 6809 and 6502 are supported with the GenRad 2302 Slave Emulator.

GenRad
Development Systems Division

5730 Buckingham Parkway
Culver City, CA 90230
(213) 641-7200 TWX: 910-328-7202

CIRCLE 68 ON INQUIRY CARD

LOGIC ANALYZERS CONQUER LSI COMPLEXITY

Logic analyzers transcend the complexity of LSI circuits by using time and data domain recording to isolate microprocessor problems in hardware and software control

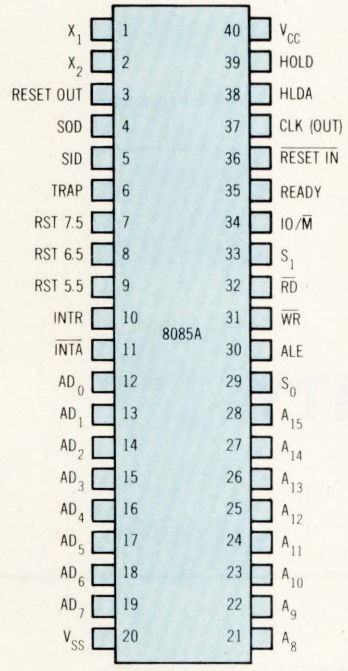
Gary Brock

Gould, Incorporated, Biomation Div
4600 Old Ironsides Dr, Santa Clara, CA 95050

Providing instrumentation suitable for debugging and troubleshooting systems based on large scale integrated circuits—such as the microprocessor—has been a major challenge to the test and measurement industry. As compared with earlier devices, the behavior of microprocessors is both complex and dynamic; problems can exist in the hardware, the software, or only in specific hardware/software interactions. Even though instruments designed for static electrical characterization can be extremely useful, electrical characterization alone is often inadequate for isolating problems or verifying proper operation. Microprocessor activity entails the complex interaction of several different signals in ways that vary over time in response to both programming and external inputs.

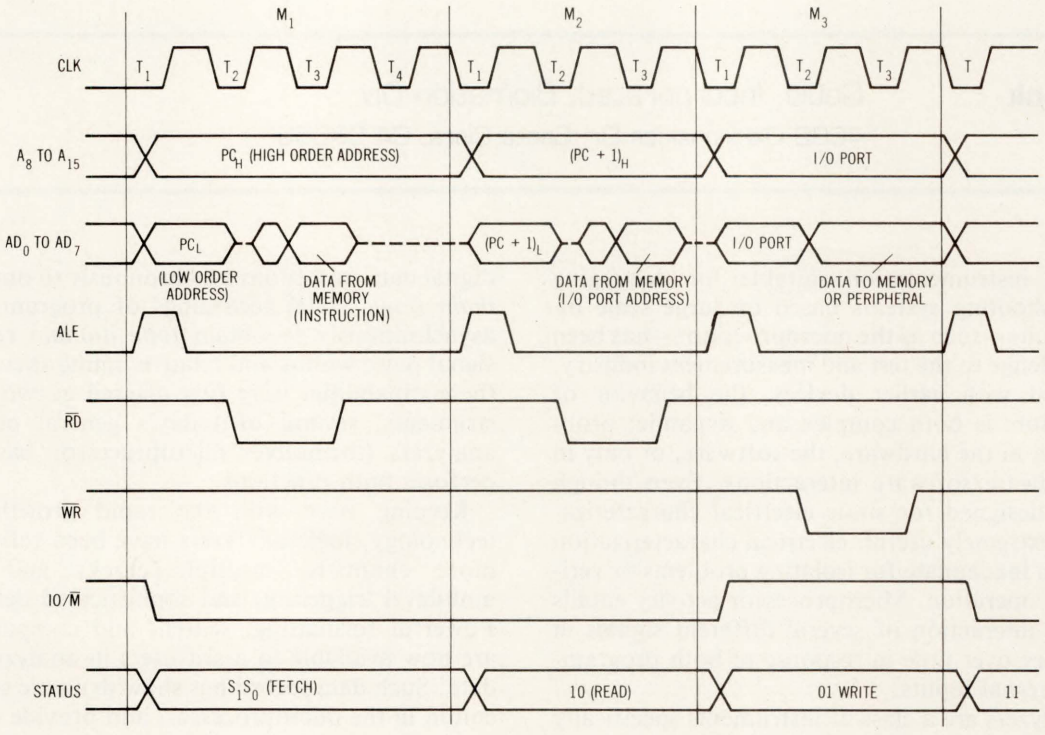
Logic analyzers are a class of instruments specifically designed to simultaneously monitor and record digital information from several different signals over a number of consecutive time periods. Originally introduced in 1973 (less than three years after the first microprocessor), these versatile instruments can sample digital data transitions synchronously to obtain *data domain* (logic state) recordings of program activity, or asynchronously to obtain *time domain* recordings of signal pulse widths and relative timing skews. Although these capabilities were first offered in two separate instruments, several of today's general purpose logic analyzers (themselves microprocessor based systems) perform both functions.

Keeping pace with the rapid growth in digital technology, logic analyzers have been refined to offer more channels, multiple clocks and qualifiers, multilevel triggering, and sophisticated delay features. Powerful formatting, search, and compare functions are now available to assist users in analyzing recorded data. Such data recordings show dynamic software execution in the microprocessor, and provide complete information on the types of instructions executed. This process zeroes in on which inputs or combination of inputs results in a system malfunction. Since they can record actual system behavior in real time, logic analyzers have become one of the primary tools of



(a)

Fig 1 Microprocessor signals and timing. In (a), 8085A multiplexing adds seven valuable signals without enlarging IC package. Three of the six possible machine cycles (b) are opcode fetch, memory read, and I/O write (Courtesy of Intel Corp)



(b)

digital designers and systems integrators. Evolution toward a systems approach in instrumentation has brought such valuable refinements as fully programmable interfaces (allowing external control of logic analyzers), desktop computers (for automated testing), and extensive, specialized data analysis.

In addition to offering powerful recording and formatting capabilities, microprocessor control of instrumentation supplies the flexibility necessary for analysis of nearly all digital circuitry. Discrete components, microcomputers, peripherals, parallel interfaces, serial interfaces, and even complex mainframes all can be evaluated and debugged quickly using these analyzers.

Popular Architecture

One widely used 8-bit microprocessor, the 8085A, is in many ways typical of a number of other microprocessors currently available. It incorporates several interesting design features, including a multiplexed address/data bus, multiple control signals, and a sophisticated interrupt structure. Using a single 5-Vdc power supply, the microprocessor occupies a 40-pin dual-inline package (DIP). With a standard 320-ms clock, it has instruction times ranging from 1.3 to 5.57 ms. Examination of the functional architecture of the 8085A provides a specific background for understanding the problems involved with measuring microprocessor behavior and for discussing the ways in which logic analyzers can provide solutions.

Multiplexed bus structure brings out both address and data information over the same lines by using separate control signals to indicate when each type of information is valid. This effectively reduces the number of signal lines coming out to the integrated circuit (IC) that are needed for a given level of operation. Consequently, the processor can be packaged in a compact 40-pin DIP to save board space while allowing the inclusion of several other signals to increase overall flexibility.

Bus Signals

Fig 1(a) maps out the 8085A pinout. Note that both the data byte and the low order address byte are brought out of the microprocessor on the same pins (12 to 19) and are labeled AD_0 to AD_7. The high order address is output separately via pins 21 to 28 as A_8 to A_{15}. 8085A signals available as a result of this multiplexing scheme that were not available on Intel's earlier 8080A include ALE, RST 5.5, RST 6.5, RST 7.5, TRAP, RESET OUT, SID, and SOD. The SID and SOD signals provide the processor with a limited serial input and output capability. RESET OUT allows synchronous reset of system support devices while TRAP, RST 7.5, RST 6.5, and RST 5.5 provide maskable and nonmaskable priority restart interrupts. ALE replaces the 8080A SYNC signal to indicate the first clock period of every machine cycle. In addition, the falling edge of ALE serves as the control signal that indicates valid address information, providing the key to demultiplexing the 8085A. Thus, by multiplexing the processor, seven signals of considerable value were added without requiring a larger IC package.

Bus Timing and Machine Cycles

Fig 1(b) shows the basic timing relationships of the 8085A as described by the manufacturer. Three typical machine cycles are shown; an operation code (opcode) fetch, a memory read, and an input/output (I/O) write cycle (as would occur during processing of the OUT instruction). Valid data for both the instruction fetch and the memory read are indicated by the rising edge of $\overline{RD}$. Valid data for the I/O write are indicated by the rising edge of $\overline{WR}$. $\overline{INTA}$, the only other control signal that indicates valid data, is not shown but has timing very similar to $\overline{RD}$. Note that the upper address bus (A_8 to A_{15}) remains valid not only for the falling edge of ALE but also for the rising edge of the data control signals. Therefore the upper address byte can be read using either ALE or the same signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$) that indicate valid data information.

There are six possible types of machine cycles during which the 8085A bus remains active. In addition to the three shown in Fig 1(b), these are memory write, I/O read, and interrupt acknowledge cycles. The type of cycle being executed is defined by states of IO/$\overline{M}$, S_1, and S_0. 8085A bus active machine cycles and the corresponding states of these status lines are listed in the Table.

Machine Cycle Chart

Machine Cycle	IO/$\overline{M}$	S_1	S_0	Octal
Memory Write (MW)	0	0	1	1
Memory Read (MR)	0	1	0	2
Opcode Fetch (OF)	0	1	1	3
I/O Write (IOW)	1	0	1	5
I/O Read (IOR)	1	1	0	6
Interrupt Acknowledge ($\overline{INTA}$)	1	1	1	7

Troubleshooting in the Time Domain

Since logic analyzers can perform timing measurements on several digital signals simultaneously, rapid comparison with manufacturer's specification tables and pinpointing of unwanted noise signals are facilitated. Typical timing problems that are handled easily using a general purpose logic analyzer include measuring signal pulse widths, determining phase relationships between signals, detecting race conditions, and finding asynchronous noise spikes ("glitches"). Current logic analyzers can record and display up to 16 channels of

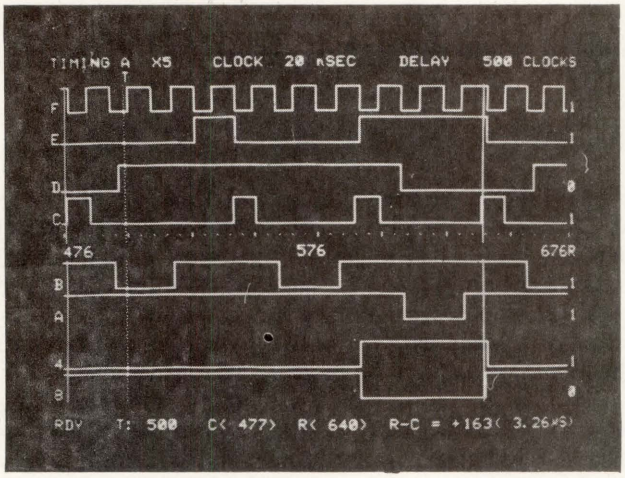


Fig 2 Time domain analysis. Same three machine cycles shown in Fig 1 appear in actual display of 8085 executing OUT instruction (note similarity). Two vertical cursors mark beginning and end of OUT execution. Data at bottom give relative cursor positions and instruction duration

high resolution timing information. Using an internal sampling clock running at a much faster rate than the system signals being examined, these analyzers provide timing resolution ranging from 50 ns (20 MHz) to 5 ns (200 MHz). Because information is sampled and stored digitally, data changes are recognized only at the active edge of the sampling clock. Several analyzers also offer latching circuitry, however, which permits the user to detect threshold crossing between samples. A variety of sophisticated triggering mechanisms is available to ensure that the time window desired is captured precisely.

Fig 2 shows an actual time domain recording of an 8085A executing an OUT instruction; the same three machine cycles are shown in Fig 1(b). This recording was made by a high performance, general purpose logic analyzer with 16-channel, 100-MHz timing resolution, 32-channel data domain recording, and a standard IEEE-488 programmable interface. After the desired resolution (sampling rate) was determined, the analyzer was programmed to trigger on the opcode corresponding to the OUT instruction. Two cursors or vertical lines—one at the far left and one toward the right side of the display—have been positioned to coincide with the beginning and the end of the OUT instruction execution, respectively. Relative positions of the two cursors are shown at the bottom of the display, and the time represented by the difference in their positions can be read directly at the bottom right side. Because of the digital nature of logic analyzers, this time measurement has an uncertainty of one sampling clock period (in this case, 20 ns).

The cursor positions help to identify the relevant portion of the recording and to illustrate the ease of making timing measurements with a modern logic analyzer. The analyzer can be programmed to capture the execution of any 8085A instruction and the cursors lined up to measure the difference between any two positions in the resulting recording. Instruction execution times, signal pulse widths, channel to channel skews, and even complex multistate dependent timing intervals can be measured easily and quickly.

Troubleshooting in the Data Domain

Data domain recordings depict the dynamic execution of software. Address and data information can be formatted and displayed in a manner very similar to that of a program object code listing. Typical formats allow binary, octal, hexadecimal, and ASCII character groupings of data channels. Instead of just recapturing the program, however, logic analyzers are also able to record every machine cycle involved in the actual execution of the program. For example, if a program calls for the execution of a loop that starts at 500 and decrements to 0 by intervals of 1, a data domain recording would capture the execution of each iteration in the loop.

In addition to capturing the address and data information, recording a variety of status and control signals is desirable. Signals can help to identify what the system was actually doing when it processed a particular address/data combination. In the case of the 8085A, each machine cycle is identified by three status signals (IO/$\overline{M}$, S_1, and S_0), as shown earlier in the machine cycle chart. Recording these signals along with their corresponding address and data provides complete identification of every machine cycle executed. Even more complete information can be recorded by also monitoring the various 8085A interrupt signals (INTR, TRAP, RST 7.5, RST 6.5, and RST 5.5).

Accurate data domain recording of program activity requires that logic status be recorded synchronously; all signals must be monitored exactly as they are handled by the processor. Since the 8085A is a multiplexed processor, its instructions can be clocked by both ALE and any of three control signals: $\overline{RD}$, $\overline{WR}$, or $\overline{INTA}$. Therefore, in order to properly monitor 8085A activity in the data domain, the logic analyzer must be equipped with both demultiplexing and OR clocking capabilities.

Although demultiplexing and OR clocking features are available in several logic analyzers, not all manufacturers' implementations are equally desirable. In some, external circuitry may be required, which introduces the possibility of loading down the system with multiple probes on individual signal lines (such as the multiplexed address/data lines AD_0 to AD_7). Excessive loading of any signal can affect system behavior and possibly cause failures. Preferably, each signal is monitored with a single probe and then buffered from internal circuitry before it is fed to other locations.

Fig 3 shows a portion of an actual 8085A data domain recording, made by the same logic analyzer that produced the time domain recording in Fig 2. Thirty-two channels of information were recorded; 16 channels were assigned to address, 8 to data, 3 to the machine cycle status signals (IO/$\overline{M}$, S_1, and S_0), and the remaining 5 to the various interrupt signals (INTR, TRAP, RST 7.5, RST 6.5, and RST 5.5, respectively). The 16-bit 8085A addresses are shown in hexadecimal on the same lines as their respective logic analyzer memory locations. Data

bytes are displayed directly beneath the 8085A addresses. Just to the right of the data bytes are the machine cycle status signals, formatted in octal to allow easy identification of the type of machine cycle executed. The five interrupt signals are each displayed sequentially in binary following the machine cycle status signals.

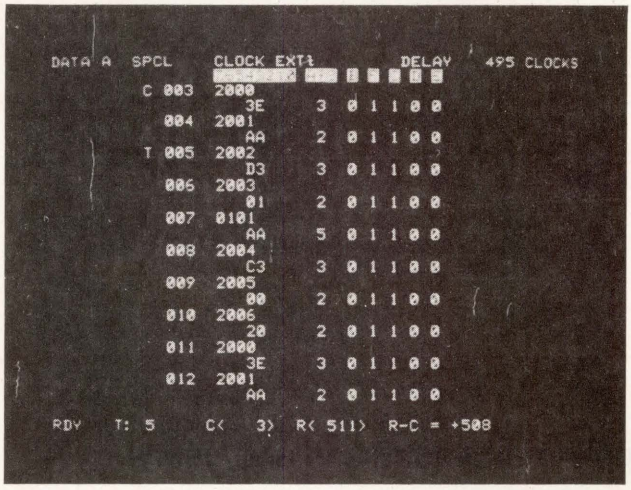


Fig 3 Data domain analysis. Display depicts software execution by presenting address and data information in various "program listing" formats. Here, each memory location corresponds to one machine cycle. Besides reconstructing dynamic programs, analyzers are capable of recording every machine cycle that occurs during program execution

Each logic analyzer memory location corresponds to the execution of a single machine cycle. All bus active machine cycles were recorded in their consecutive order of occurrence, and there is a unique memory location for each cycle to trace machine flow in real time. A number of sophisticated triggering parameters can provide precise capture of the information surrounding suspected problem areas.

Visual analysis of a recording is often supplemented by powerful analysis routines resident in the logic analyzer. Automatic search and compare features, for example, allow rapid determination of questions such as, How many instruction fetches are present in memory? How long did it actually take to execute a particular program loop? Was address OFC3 captured in memory? What differences exist between this recording and one made earlier?

Summary

Logic analyzers are an excellent answer to the problems of microprocessor debugging and troubleshooting. Particularly, the strength of the general purpose logic analyzer, itself a microprocessor based system, lies in its ability to record both in the time domain and in the data domain. Hardware faults, software faults, and specific hardware/software interactions that cause microprocessor malfunctions are easier to locate and evaluate. Data recordings show dynamic software execution in the microprocessor. By providing complete information on the types of instructions executed, the data recordings reveal which inputs or combinations of inputs caused the system's behavior.

Bibliography

Intel Component Data Catalog, 1980, pp 6-24

B. Lorentzen, "For Complete μP Design, Logic Analyzers Finish What Development Systems Start," *Electronic Design,* Mar 29, 1980, pp 81-85

B. Lorentzen, "How Much Speed is Enough for a Logic Analyzer?" *Electronic Engineering Times,* July 23, 1979, pp 48-49

M. Marshall, "What to Look for in Logic Timing Analyzers," *Electronics,* Mar 29, 1979, pp 109-114

A. Osborne and J. Kane, *An Introduction to Microcomputers, Volume 2: Some Real Microprocessors,* Osborne/McGraw-Hill, Berkeley, Calif, 1978

R. Tottingham, "Understanding Logic Analyzers," *Machine Design,* Apr 2, 1979, pp 99-104

About the Author:

A digital applications engineer for Gould Inc, Gary Brock specializes in product development, including conceptual design and new product evaluation. Gary has conducted logic analysis training seminars regarding time and data analyses of discrete logic, microprocessor, and mainframe digital systems and interfaces. He holds BS and MBA degrees from Wright State University in Dayton, Ohio.

Please rate the value of this article by circling the appropriate number in the "Comments" box on the Inquiry Card.

High 704 Average 705 Low 706

TECH NOTE

The Changing Power Supply Scene

Important implications exist for power supply manufacturers and users alike as switching power supplies become an attractive alternative to linear regulation in low output applications

Jeffrey D. Shepard

LH Research
14402 Franklin Ave, Tustin, CA 92680

Almost every electronic system uses some kind of power supply to convert raw input power from the ac line into refined electrical power that is compatible with system requirements. Because they are needed in so many systems, power supplies represent an important segment of the overall electronics industry.

Two distinct segments, one large and one small, make up the power supply market. The former (75% in 1979) incorporates a mature technology growing at 8 to 10% a year, while the latter incorporates a developing technology that is experiencing 30% annual growth and significant change. This large differential in growth rates is causing a basic structural change in the power supply industry, although external factors also contribute to the change. The latter include the quality of electric power produced by utilities, changing government regulations, and technological developments in other areas of electronics.

Developing Versus Mature Technology

Today, most power supply designs use the linear or series-pass regulation technique. Linear power supplies provide excellent regulation, but they have a number of characteristics that are increasingly becoming drawbacks to their general use. When energy was abundant and raw materials inexpensive, it did not matter that a typical linear wastes 60% of its input energy as heat; nor was the relatively large amount of copper and steel needed to manufacture linears considered a serious disadvantage. However, as concern over the relative inefficiency of linears grew, the basic technology of the power supply industry began a shift to a different and more efficient regulation technique called pulse width modulated switching regulation.

Switching power supplies, or switchers, have been used in military applications for many years. Yet, it took the development of more reasonably priced switching transistors to make switchers commercially practical. The technology used to achieve the increased electrical and material efficiency of switchers is relatively complex and quite different from that of linears. Because of their complexity, early switchers were competitive only in the higher wattage output markets; in fact, the first commercially economical switchers used transistors originally designed for automotive and television applications. To achieve acceptable performance, these

(continued on page 134)

We just delivered our one millionth

Why the celebration?

We just delivered our millionth D.C. power supply to a very happy customer. Borrowing a note from the record industry, we presented a special solid gold unit to further honor the occasion.

One million.

An impressive number in itself. But consider what it took to get there.

Electrical Wire – about 475 million feet. That's enough to wrap around the world a few times.

Sheet Metal – an estimated 820,000 sq. ft. Or enough to cover more than 17 football fields.

Transformer Magnetic Steel – around 2,200 tons. This translates into the weight of about 1,250 mid-size automobiles.

Resistors, Capacitors and Semiconductors – approximately 54 million. And each one was individually tested, along with a double in-circuit test.

Assorted Screws, Nuts and Hardware – 45 million pieces or so. Though mostly automated, it's still a lot of turns of the screwdriver.

And on and on it goes. Which leads to the reason we have become, in just a few short years, the world's largest manufacturer of open-frame D.C. power supplies.

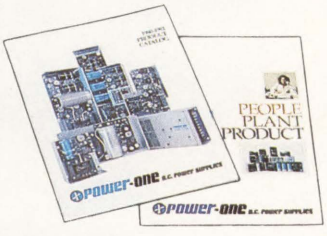
We have the experience.

We do all manufacturing in our new 100,000 sq. ft. facility. And we continue to guarantee the service, quality, and reliability you demand.

So now begins the second million. And it won't take long to get there. Not when you see our expanded line of open-frames – plus a new and growing family of switchers. **All at our same old low prices!**

See for yourself.

Send for our new 1980-81 Catalog and Power-One Tour Guide. You'll know why we reached the first million in record time.



Power-one
D.C. POWER SUPPLIES

Power-One, Inc. • Power One Drive • Camarillo, CA 93010
Phone: 805/484-2806 • 805/987-3891 • TWX: 910-336-1297

CIRCLE 69 ON INQUIRY CARD


JAPAN 0822
HM6147P-3
IR
100
WINNER

2147's Too Hot to Handle?
Now You Have A Choice!

The Award Winning HM6147

4K x 1 CMOS Static RAM From HITACHI !!!

Here's Hitachi "HI-CMOS" technology at its best: you get the high speeds of HMOS... the high bit densities of NMOS... and the low power dissipation of CMOS. This advanced technology has never been more evident than in our IR100 award-winning HM6147 CMOS memory: a unique combination of high-speed NMOS memory cells and low-power CMOS peripheral circuits yield fast 55ns access times with low-power 75mW dissipation; there's never a need for costly cooling systems and high current power supplies with the HM6147. Best of all, there's no need to wait for this advanced technology CMOS RAM: you can get all the Hitachi HM6147 CMOS RAMs you need – at a price that rivals NMOS cerdip RAMs – simply by calling your local Hitachi Representative or distributor sales office.

HM6147 CMOS RAM

Organization	Speed	Typ. Operating Power	Typ. Standby Power	Max. Power Down
4K x 1	55/70/85ns	75mW	25mW	100μW

Pin-For-Pin Replacement For 2147

Available In Volume...NOW!

Regional Headquarters

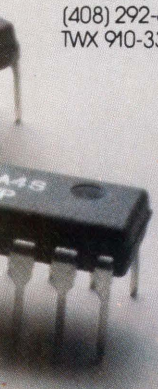
Western
1800 Bering Dr
San Jose, CA 95112
(408) 292-6404
TWX 910-338-2103

Central
6200 Savoy Dr., Suite 704
Houston, TX 77036
(713) 974-0534
TWX 910-881-7043

Eastern
594 Marrett Rd., Suite 22
Lexington, MA 02173
(617) 861-1642
TWX 710-326-1413

Stocking Distributors

Active Component Technology • Anthem • Bell • CAM/RPC • Diplomat • Future • Jaco • Marshall • Milgray • RC Components • Resco • RM Electronics • Sterling • Time • Western Micro Technology



HITACHI

Hitachi America, Ltd, Electronic Devices Sales and Service Division
1800 Bering Drive, San Jose, CA 95112 (408) 292-6404

Symbol of Semiconductor Quality, Worldwide

CIRCLE 70 ON INQUIRY CARD

transistors had to be matched individually, resulting in an extremely high and costly rejection rate.

Continued improvements in switcher technology have made the modern power supply market a dynamic one. As switching power supply sales volume increased, demand for switching transistors grew to a point where transistor manufacturers began to design and produce devices specifically for switcher applications. However, in addition to being expensive, early switchers were less reliable than linear power supplies. This lower reliability was a direct manifestation of their complexity and the lack of components designed specifically for their use.

"Today's major linear power supply manufacturers could easily be replaced by a new group of switcher manufacturers."

Increased sales volume has spurred development of integrated circuits (ICs) for use in switching regulated power supplies. These ICs significantly reduce the cost of designing and manufacturing switchers. Furthermore, use of components developed specifically for switchers, and use of ICs to reduce overall component count, together have resulted in greatly improved reliability comparable to that of linears. The next few years should see continued adoption of switching regulation by the power supply industry.

What is expected as an important result of this trend is that industry leadership will shift as basic technology changes. Today's major linear power supply manufacturers could easily be replaced by a new group of switcher manufacturers. This has happened many times in the electronics industry. Examples include the displacement of RCA, Sylvania, and General Electric as suppliers of vacuum tubes by Texas Instruments, National Semiconductor, and Motorola as suppliers of semiconductors; and the replacement of Friden, Monroe, and Victor as suppliers of electromechanical calculators by Texas Instruments, Hewlett-Packard, and Casio as suppliers of electronic calculators.

Leadership changes as technology changes. Companies that hold large shares of a market for current technology products, such as linears, have major technical and financial investments that cannot be adapted quickly or easily to changing technology, such as switcher regulation. Major suppliers must precisely time their move into a new technology. Changing before the new technology has been accepted by a wide enough segment of the market, or after competitive firms have become entrenched in the new marketplace, will cost companies a substantial portion of their market share.

In the power supply industry, the top five commercial firms are primarily manufacturers of linears. These are Lambda Electronics, ITT North Electric, Acme Electric, ACDC Electronics, and Power/Mate. All are currently at various stages of transition from linears to switchers. The second ranking five commercial power supply manufacturers consist of four switcher companies and one supplier of linears: LH Research, Power-One (linears), Pioneer Magnetics, Hewlett-Packard, and Boschert. Because the switcher companies are already strongly committed to the new technology, any of the linear companies that do not use precise timing in "hitting the window" into the switcher market can be expected to lose significant market share to the switcher manufacturers.

Switcher technology should continue to improve in the 1980s, with the replacement of bipolar transistors by power metal oxide semiconductor field effect transistors (MOSFETs) as the next major development. This change is expected to be gradual, beginning in the low power units and slowly being incorporated into higher output level equipment above the 200-W level. Designs that include power MOSFETs will yield smaller, less expensive, and more reliable switchers; therefore, to achieve long-term survival as a major power supply manufacturer, a company must adopt switcher technology and also make the transition from bipolar to MOSFET switchers, with the sizable research and development investment this entails. Again, manufacturers who cannot meet the challenge will lose market share.

Efficiency Considerations

Although initial unit price is important, the efficiency of a power supply has greater impact on the cost of ownership and is thus a critical factor in power supply comparisons. The efficiency of a power supply is often oversimplified and misunderstood. It is usually defined as the ratio of output power to input power. By this measure, the efficiency of a typical linear is 40%, and that of a switcher 70%. However, the true magnitude of the difference between 40 and 70% efficiency may not be obvious. Consider two typical 250-W power supplies: a linear and a switcher. The linear requires 625 W of input power, the switcher 357 W. Energy consumption of these units differs significantly in that the switcher wastes only 107 W of input power while the linear wastes 375 W, more than three times as much. In terms of today's energy costs, this is an expensive difference over the entire life of the systems in which power supplies are installed.

"Switcher prices, now competitive with linears at levels above 100 W, will continue to fall as the technology advances."

Another important consideration is the need to exhaust the heat dissipated by a power supply. Most modern electronic systems operate in environmentally controlled surroundings. A linear places a much greater load on air conditioning

equipment than a cooler running switcher. Therefore, although the change in moving from 40% efficiency to 70% efficiency is less than a factor of two, this translates into a fourfold decrease in wasted energy, a difference that becomes increasingly important as the cost of energy continues to rise.

"Switchers...typically provide 20 ms of carryover, adequate for the protection of digital systems against momentary dropouts."

Material efficiency is also important in the overall efficiency of a power supply. Switcher prices, now competitive with linears at levels above 100 W, will continue to fall as the technology advances. Linears incorporate large 60-Hz power transformers, which consume large amounts of steel and copper; therefore, the price of linears will increase with the rising price of materials. Besides being costly, large transformers are heavy. A linear will deliver about 5 W/lb (11 W/kg), a switcher about 20 W/lb (44 W/kg). Physical volume is another manifestation of the material efficiency of a power supply. Linears typically offer 0.33 W/in^3 (0.02 W/cm^3), switchers 1.0 W/in^3 (0.06 W/cm^3); thus, a switcher will occupy only one-third the space of a comparable linear.

External Factors

The quality of the electric power delivered on the major power distribution networks is only fair. It is quite common for ac line power to skip a cycle so that a 16-ms dropout occurs. Dropouts can also be caused by power distribution network switching or even a natural phenomenon like lightning.

Most digital systems cannot tolerate a loss of power for longer than about 15 ms, and a linear power supply cannot provide sufficient carryover in the case of line voltage dropouts. Switchers, on the other hand, typically provide 20 ms of carryover, adequate for the protection of digital systems against momentary dropouts. They also protect electronic systems from brownouts. Linears normally tolerate an input voltage range of only ±8%, whereas switchers have an input voltage range of about +10 to −20% of nominal.

It is generally accepted that rolling brownouts will occur frequently in the future and that ac line power dropouts will continue to be common. These factors, together with the increasing importance of continuous operation of digital systems, will help determine the rate at which switching regulated power supplies replace linears as the industry standard.

Changes in the scope of government regulations will also affect the transition from linears to switchers. The Federal Communications Commission (FCC) recently adopted regulations covering the emission of electromagnetic interference (emi) from electronic equipment. Linears are inherently quiet devices that produce little emi, whereas switchers are emi sources that require extensive filtering to meet FCC regulations. Most current technology switchers incorporate filter networks that reduce emi, but generally not to the extent now required by the FCC. The emi limits acceptable to the FCC are similar to those set by the German organization *Verband Deutscher Elektrotechniker* through its 0871 specification. Only one manufacturer can meet the emi requirements of VDE-0871 through internal filters, demonstrating the difficulty of conforming to strict emi requirements.

A second area of government regulation that could become important is the minimum allowable efficiency standard for electronic equipment. Efficiency requirements have already been imposed on the automobile industry and are pending for the electric appliance industry. Any reasonable standard, such as a requirement for efficiency greater than 50%, would call for use of switchers rather than linears.

The speed and direction of technical change in the entire electronics industry will affect the power supply segment, since all manufacturers will need to work harder than ever to keep abreast of their own fields. Electronics firms now producing power supplies in-house as a sideline will no longer be able to keep pace with current technology in both their primary field and the area of power supplies. The result will be the growth of the non-captive segment of the power supply market.

"A second area of government regulation that could become important is the minimum allowable efficiency standard for electronic equipment."

The increasing use of microprocessor based devices, too, will impact the industry. As compact, low power microprocessor systems replace mainframe computers and other large electronic systems, the market for high wattage power supplies will shrink, while lower power units will account for an even larger portion of power supply production. This will affect power supply manufacturers because low power switchers generally incorporate circuit configurations quite different from those of high power switchers. It is another area in which the successful manufacturer must adjust to changing conditions.

Conclusion

Switcher technology will continue to improve during the coming decade, leading to lower cost and greater reliability. In contrast, linears, because they reflect a mature technology, will continue to increase in price as labor and raw materials costs rise. Consequently, the power supply industry will be abandoning linear regulation technology in favor of switchers. For power

(continued on page 137)

Smart screen size: 15"

15-inch display heads the Executive 80™ list of smart ergonomic features.

When you look at the business end of a terminal, you expect to see a clear, crisp display. That's exactly what you'll see on the Executive 80™ standard 15-inch display. Executive 80 gives you a viewing area that's 25% larger than the competition's 12-inch screens — at no extra cost. Since a larger screen is easier to read, you can expect increased throughput, fewer errors, and greater comfort for your operators.

Hazeltine's attention to ergonomic detail doesn't stop with the larger screen. You can order the tiltable screen with detached keyboard for greater operator convenience. And the *Enhanced Video Option* features smooth scroll, selectable double-size characters, and switching between 80- or 132-column format from the keyboard.

Put Executive 80's big screen to the test. You'll agree it's the smart way to look at data.

Call today and we'll send you additional literature and pricing information. Call toll-free (800) 645-5300 — in New York State call collect (212) 752-3377.

Hazeltine Corporation
Computer Terminal Equipment
Greenlawn, NY 11740
(516) 549-8800

Hazeltine Executive 80

Answers for the Eighties

New York (212) 752-3377 • New Jersey (201) 584-4661 • Chicago (312) 986-1414 • San Francisco (415) 342-6070 • Atlanta (404) 256-5581 • Arlington (703) 892-1800 • Orlando (305) 628-0132 Dallas (214) 980-9825 • Los Angeles (213) 553-1811 • Columbus (614) 889-6510 • England 01-568-1851 Telex (851) 928572

CIRCLE 71 ON INQUIRY CARD

supply manufacturers, the changing technology could bring about a change in industry leadership. Major linear manufacturers who fail to move into switcher technology at the right time will suffer a significant loss of market share, while strong switcher manufacturers who can take advantage of the change in technology will gain market share.

During the transition period from linears to switchers, the latter will continue to be in short supply because major switcher manufacturers have not yet grown large enough to keep up with demand, while linear companies have yet to complete the transition to the new technology. Numerous small switcher manufacturers have sprung up to fill the gap between the supply of and demand for switchers. As the transition to switchers is completed, a major shakeout in the power supply industry is likely to take place. Some large producers of linears will make the change successfully; others will not.

"The transition from bipolar to MOSFET technology within the switcher industry could intensify the coming shakeout and impact power supply users as well as manufacturers."

The transition from bipolar to MOSFET technology within the switcher industry could intensify the coming shakeout and impact power supply users as well as manufacturers. Users who purchase their requirements from outside vendors must adapt their power supply specifications to switcher technology and review their qualified suppliers with an eye to switcher capability. Users who are in-house producers of power supplies will face ever increasing difficulties in manufacturing state of the art power supplies. Linears can be designed in a matter of weeks, but switcher design requires many months. This fact will encourage many firms that are now producers to turn to outside vendors to overcome the problems of efficient power supply production. Moreover, changes in government regulations will compound the problems of firms that attempt in-house production of switchers.

Finally, technology changes in other parts of the electronics industry will affect the power supply segment. Most important will be the continuing development of microprocessor based systems, which will cause the market for high output power supplies to become a smaller portion of the overall power supply market. The outcome of all these changes within the industry is that two kinds of manufacturers will most likely survive in the long term: small but technically strong companies that produce a low volume of high power units and custom switchers, and a few large companies that produce a very high volume of low power switchers for the microprocessor based products currently being developed.

Bibliography

S. Davis, "Top 10 Power Supply Makers Outpaced Industry Growth," *Electronic Business,* Aug 1979, pp 62-68

R. Hackmeister, "Power Supply Technology Advances to Meet New Market Needs," *High Technology,* Apr 1980, pp 10-12

W. Hersom and J. Shepard, "Switching Power Supplies," *Digital Design,* Dec 1979, pp 74-78

J. Shepard, "Switching Supplies: The FCC, VDE and You," *Electronic Products,* Mar 1980, pp 51-53

How valuable is this note to you?

High 710 Average 711 Low 712

Please circle the appropriate number in the "Comments" box on the Inquiry Card.

TECH NOTE

Microprocessor Controlled Digital Pulse Width Modulators

Practical, extensible circuits illustrate the advantages of digital pulse width modulation in effective, low cost, microprocessor based applications that range from signal processing to servo control

Vassilios J. Georgiou

Voicetek Incorporated
PO Box 388, Goleta, CA 93017

A pulse width modulator changes the on-off ratio of a pulse train according to a control signal. In a digital pulse width modulator, the control signal is a data word whose value determines the pulse width. Regardless of pulse width, the period of the modulated pulse train remains constant. Microprocessor control of a digital modulator is easily achieved. The microprocessor can supply a word to designate the pulse width at its output port, and the modulator can produce a train of pulses having the desired width. It is also possible to generate a pulse width modulated signal by using only software to toggle an output port bit at appropriate times. This approach has disadvantages, however. The microprocessor must be dedicated because virtually all of its time will be consumed in generating the control signal, and the speed of the microprocessor will limit the maximum pulse repetition rate.

A microprocessor controlled pulse width modulator (PWM) has many uses. It can serve as an inexpensive digital to analog converter (DAC) because the average or dc value of its output is proportional to the pulse width and, therefore, proportional to the value of the control word. To operate a PWM as a DAC, it is necessary to filter its output at a frequency below the pulse repetition frequency. Because of its modulation method, the DAC will be monotonic and will have excellent linearity.

Motor speed control is another application. The speed of a series wound dc motor—the most common small motor—can be controlled by regulating the applied voltage. When operating at low speeds with a low applied voltage, the motor torque may be less than the friction in its bearings, and the motor may stall, operate erratically, or even refuse to start. If the motor is driven by a pulse width modulated signal, it will always receive the same voltage during the times that the pulse is on, so that the starting and operating torque will suffice even at very low speeds. For example, a small motor that stalls around 600 r/min when controlled by a variable voltage source will operate smoothly down to 1 r/min or less when controlled by a digital PWM. This application does not require a low pass filter because the inertia of the motor smooths out the effect of the pulses.

Another advantage of PWM control is that power drivers will operate in the on-off mode with transistors either fully saturated or fully off, minimizing power dissipation in the driver. PWM control of other electromechanical transducers, such as loudspeakers and ultrasonic transmitters, realizes many of these same advantages.

(continued on page 140)

GET A CLEAR HONEST IMAGE THE HITACHI WAY!

Computer data and graphic displays never looked better, brighter, sharper.

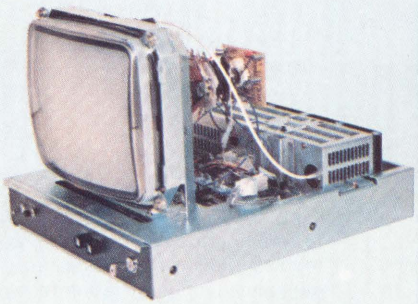
New Hitachi high resolution in-line RGB color monitors utilize wide video bandwidth and a 0.31 mm spacing between triad pairs. The result? A trio-dot density **twice that of conventional monitors!**

Look at these advanced features

Adjustment-free convergence, single PCB configuration, video amplifier bandwidth from 50 Hz to 25 MHz. Flexible frequencies range from 15 to 18 KHz horizontal and 50 to 60 Hz vertical. Monitors provide high contrast and brightness from black matrix and 85% light transmission tubes. Can any other maker match these advantages?

Variety of Screens

You can select from a wide choice of screens to meet your specific application needs: Normal phosphor; long persistence phosphor to virtually eliminate flickering, or medium resolution versions for most ambient light situations.



Unsurpassed performance

Long time convergence stability is assured due to self convergent in-line guns and **single PCB reliability.** Operator controls include power on/off, degauss, brightness, contrast.

Call or write for more information.

Hitachi America, Ltd. 100 California Street, San Francisco, Calif. 94111 Tel: (415) 981-7871

Crown Electronics, Tualatin, OR (503) 638-7561; **Quadrep, Inc.,** San Jose, CA (408) 946-4000; **Bestronics, Inc.,** Culver City, CA (213) 870-9191, Irvine, CA (714) 979-9910, San Diego, CA (714) 452-5500; **Comstrand, Inc.,** Minneapolis, MN (612) 788-9234; **Sumer, Inc.,** Rolling Meadows, IL (312) 991-8500, Brookfield, WI (414) 784-6641; **Bear Marketing,** Richfield, OH (216) 659-3131; **Robert Electronic Sales,** Pasadena, MD (301) 255-7204, Lansdale, PA (215) 855-3962, Richmond, VA (804) 276-3979; **Technology Sales, Inc.,** Lexington, MA (617) 862-1306.

CIRCLE 72 ON INQUIRY CARD

Two Design Approaches

A digital PWM can be implemented in many different ways. The two possible implementations described here represent two completely different approaches to the problem and have the advantage of requiring a minimum number of components. In Fig 1, two LS161 counter integrated circuits (ICs) form a free running divide-by-256 counter whose output is constantly compared with the microprocessor output port value using the two cascaded LS85 comparators. As long as the counter output is less than the control word at the output port, the A > B comparator output stays high. When both inputs to the comparator are equal, the A > B output goes low, to zero, and remains low until the counter overflows. Then, A > B returns high and the process is repeated.

The period of the output waveform is

$$T_{out} = 256\ T_{clk}$$

and the pulse width is

$$W = C\ T_{clk}$$

where C is the control word value. With a zero control word, this circuit supplies a zero output level, and the device that it drives will remain fully off. However, with the maximum 255 control word value, the output will not remain fully on; instead, it will drop low every 255 clock pulses and remain low for one clock period. This is not harmful in most applications.

The circuit in Fig 1 is easily expanded to use larger control words by cascading additional comparators and counters. If multiple output channels are required, additional sets of comparators can be added, and the same counter can feed the comparators on all channels. In a multichannel digital PWM using this approach, the total number of ICs required is one more than the number of channels multiplied by one-fourth of the accuracy in bits.

Preloadable up/down counters can implement a PWM as shown in Fig 2. The counter chain decrements the preloaded control word value and, when it reaches zero, generates a borrow. The JK flipflop connected

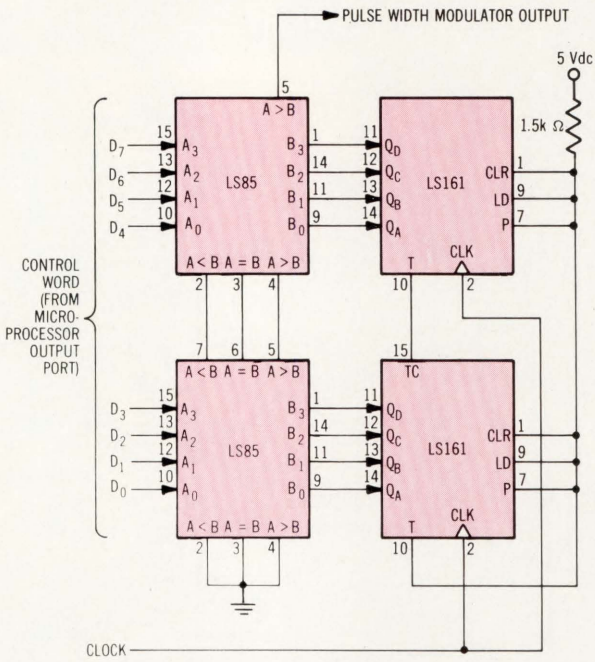


Fig 1 PWM using free running counters and comparators. Comparator output will be high as long as control word at microprocessor output port exceeds output of free running divide-by-256 counter, otherwise low. Additional components increase accuracy and allow multiple channel operation

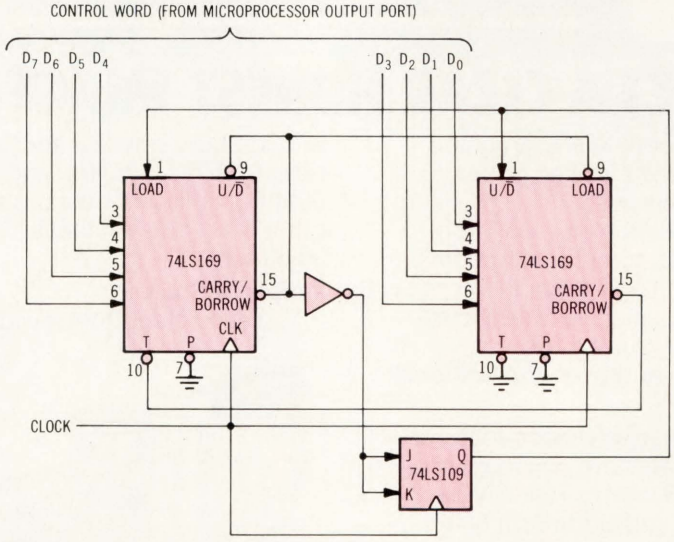
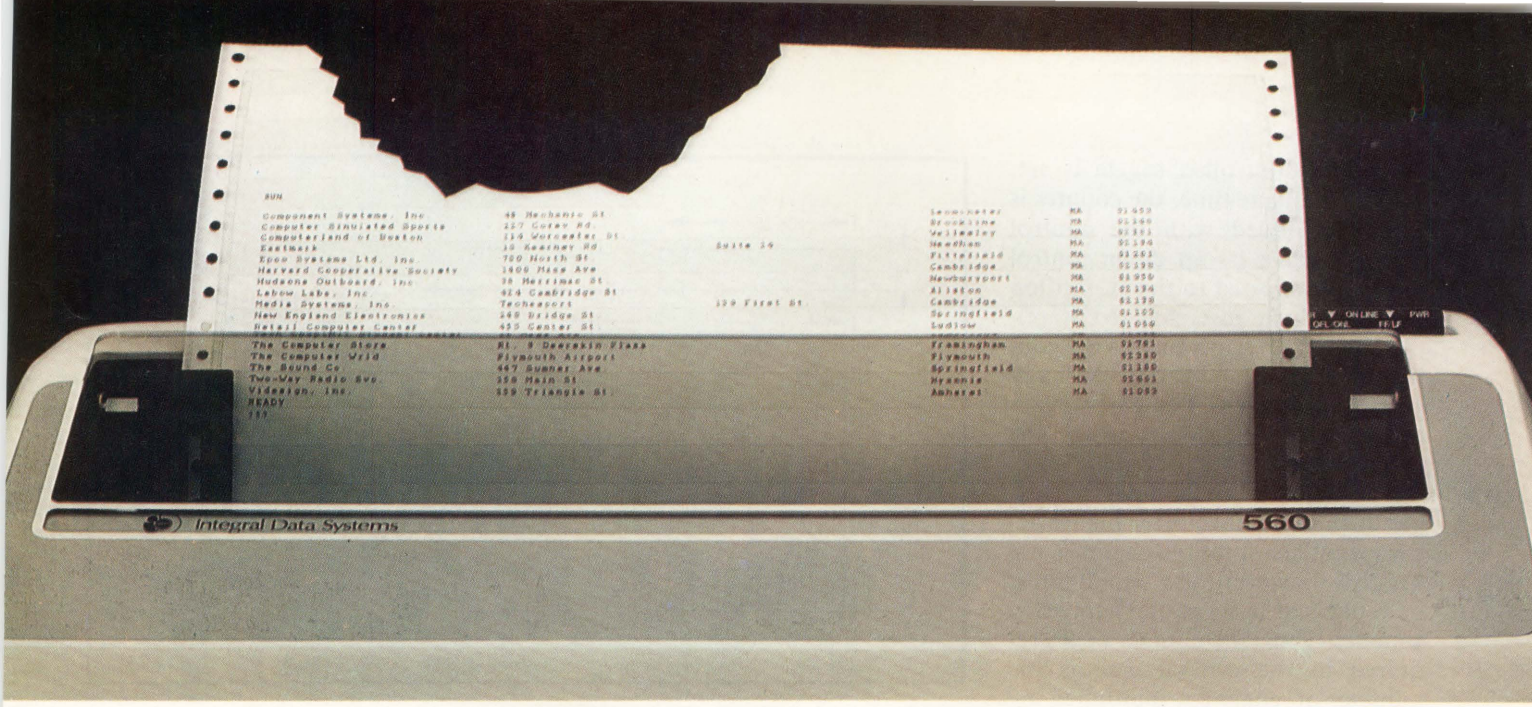


Fig 2 PWM using up/down counters. Preloaded counter decrements to zero and toggles flipflop. It next increments to overflow and again toggles flipflop. Increased accuracy is easily achieved; however, multiple channel operation requires full circuit for each channel



Meet the Tiger with a bigger bite.

Introducing the remarkable 132-column Paper Tiger™ 560. The first full-width matrix printer to give you fully formed characters for a low $1695.*

The new 560 features a staggered nine-wire ballistic type print head that overlaps dots in both horizontal and vertical planes. It bi-directionally prints up to 150 dense, text quality characters per second.

The 560 also features a reliable cartridge ribbon that lasts up to four times as long as spool and cassette ribbons, separate heavy-duty stepper motors to drive the print head and advance the paper, plus true tractor feed.

presents a breakthrough in matrix printin
ering the user excellent print quality wit
ce of a matrix printer. Employing a uniq
red column" head manufactured by Integr
creates high quality printouts by overla

Paper Tiger 560 Print Sample

And famous Paper Tiger performance comes with every new 560. Like fixed or proportionately spaced text, programmable tabbing and business forms control, automatic text justification, print formats to 220 columns, parallel and serial interfaces, self-diagnostics, and more. All inside the most compact printer of its kind.

Need more stripes? Dotplot,™ our high-resolution raster graphics package, is standard on every 560.

For data processing, word processing and small business applications, this is your Tiger. The business-sized Paper Tiger™ 560.

It's a Tiger you can count on.

Call TOLL FREE 800-258-1386 (In New Hampshire, Alaska and Hawaii, call 603-673-9100.) Or write: Integral Data Systems, Inc., Milford, NH 03055.

Paper Tiger 560

Integral Data Systems, Inc.

*Suggested single-unit U.S. price. Very generous OEM discounts available.

as a data controlled toggle is set, and, at the same time, the counter is again preloaded with the control word. Because its up/down control input is connected to the JK flipflop output (which just changed state), the counter now increments the control word value and eventually generates a carry. The carry again toggles the JK flipflop to repeat the cycle.

The addition of counter ICs expands this circuit to offer higher accuracy. When multiple channels are desired, however, the circuit must be replicated in its entirety for each channel. Thus, the number of ICs required in the general case is the number of channels multiplied by the sum of one-fourth the accuracy, in bits, and two-thirds. This number must be rounded to the nearest higher integer and cannot be less than three.

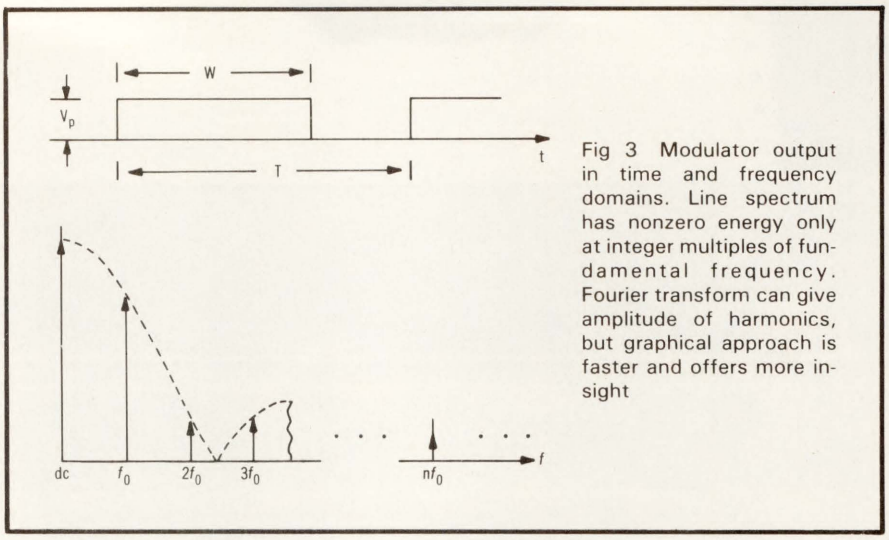


Fig 3 Modulator output in time and frequency domains. Line spectrum has nonzero energy only at integer multiples of fundamental frequency. Fourier transform can give amplitude of harmonics, but graphical approach is faster and offers more insight

Spectral Analysis

Proper use of a PWM requires an understanding of the frequency domain characteristics of a pulse width modulated signal. For a given pulse width, the signal spectrum can be found by performing a Fourier transformation on one period of the modulator output. However, the graphical approach used here is faster and allows a feel for the spectral behavior to develop. The spectrum is, of course, a line spectrum with nonzero energy only at frequencies that are integer multiples of the fundamental frequency $f_0 = 1/T$, where T is the period of the output waveform (Fig 3).

Amplitudes of the individual harmonics can be determined by noting that, regardless of the pulse width, the spectral envelope will be the rectified sinc function (sine X divided by X) shown in Fig 4. Thus, the spectrum of the PWM output can be viewed as a sequence of spectral impulses, each with amplitude 1, multiplied by a rectified sine wave that has been scaled appropriately.

The main lobe of the sinc function widens as the width of the modulated signal decreases. At the same time, its amplitude is reduced, which is to be expected because the peak of the main lobe is the average or dc value of the time domain signal. The final spectrum would look the same if the sinc function changed only in amplitude and the fundamental frequency of the line spectrum changed for each pulse width. The latter cannot occur because, by definition, the period of the modulated waveform remains constant; however, the fundamental frequency can be used to calculate the spectrum graphically in two stages.

First, determine the amplitude of the dc component in the spectrum, the average value of the time domain signal:

$$V_{dc} = (W\ V_p)\ /T$$

This scales the amplitude of the sinc wave envelope. Next, find the ration $k = W/T$. Then, using Fig 4, draw a vertical line at the X-coordinate point that has value k. The height of

(continued on page 144)

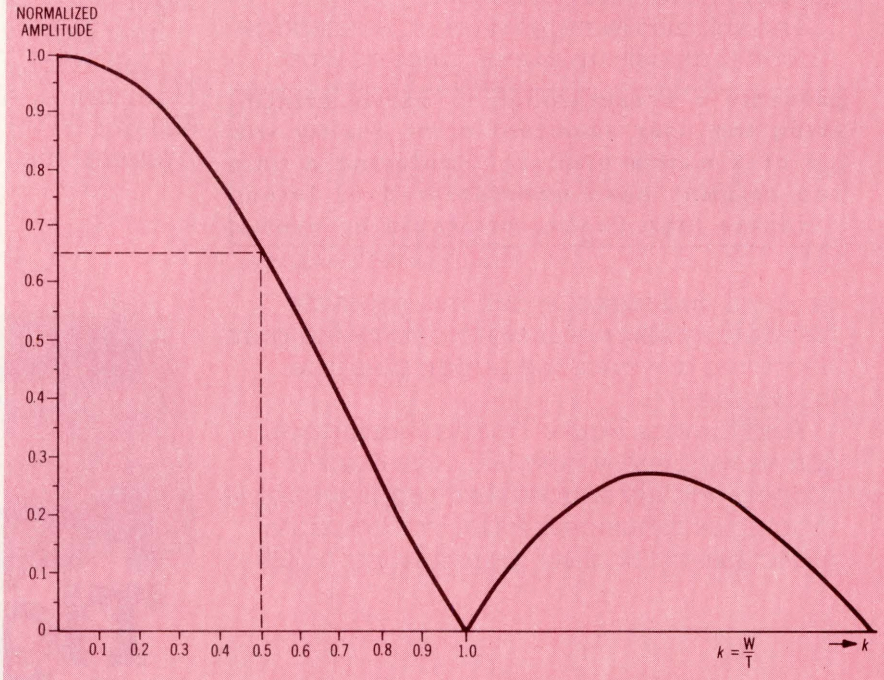


Fig 4 Spectral envelope. Visualizing spectral impulses as having unit amplitude and multiplying these impulses by scaled, rectified sinc function shown here gives true spectrum of PWM output

FAIRCHILD

A Schlumberger Company

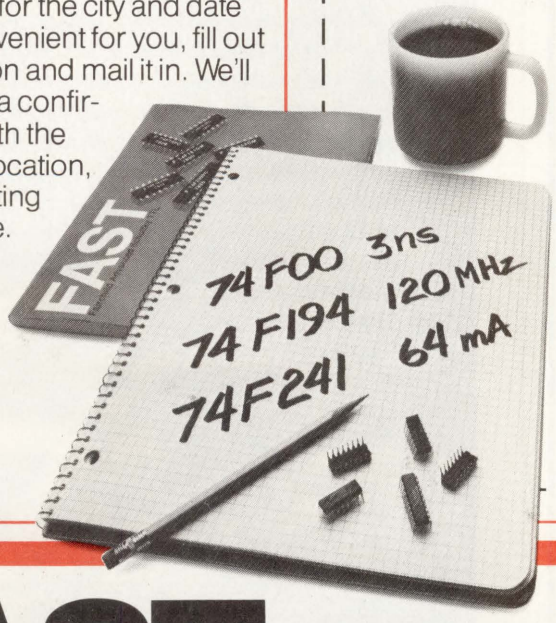
You like what you've heard about the FAST family of Advanced TTL Logic, but you want to know more, right? That's easy. Just sign up.

Announcing the new, expanded FAST Technology Seminar. Applications, comparisons, reliability, delivery, ordering information—everything you need to know, at no cost, from the people who know it best—the Fairchild FAST Marketing Application Team.

You get a FAST data book, a workbook containing all of the materials presented in the seminar, samples and availability information.

And you get all the latest input on the technology that's delivering up to 40% more speed than Schottky, with a reduction in power of up to 75%! And up to 75% more speed than low-power Schottky.

The Fairchild FAST Application Seminar. Just check the listing for the city and date most convenient for you, fill out the coupon and mail it in. We'll send you a confirmation with the seminar location, and a seating guarantee. FAST.



Where and when.

Feb. 4, 1981 —
Santa Clara, CA (408) 987-9530
Feb. 5, 1981 —
Seattle, WA (503) 641-7871
Feb. 6, 1981 —
Portland, OR (503) 641-7871
Feb. 9, 1981 —
San Fernando Valley, CA (213) 990-9800
Feb. 10, 1981 —
Los Angeles, CA (213) 990-9800
Feb. 11, 1981 —
Anaheim, CA (714) 557-7350
Feb. 12, 1981 —
Irvine, CA (714) 557-7350
Feb. 13, 1981 —
San Diego, CA (714) 557-7350
Feb. 16, 1981 —
Phoenix, AZ (602) 864-1000
Feb. 17, 1981 —
Salt Lake City, UT (801) 566-3691
Feb. 18, 1981 —
Denver, CO (303) 794-8381
Feb. 19, 1981 —
Minneapolis, MN (612) 835-3322
Feb. 20, 1981 —
Chicago, IL (312) 640-1000
Feb. 23, 1981 —
Dallas, TX (214) 234-3391
Feb. 25, 1981 —
Houston, TX (713) 771-3547
Feb. 26, 1981 —
Huntsville, AL (205) 837-8960
Feb. 27, 1981 —
Atlanta, GA (205) 837-8960
March 2, 1981 —
Detroit, MI (313) 478-7400
March 3, 1981 —
Cleveland, OH (216) 587-3600
(Pioneer Electronics)
March 4, 1981 —
Dayton, OH (513) 236-9900
(Pioneer Electronics)
March 5, 1981 —
Indianapolis, IN (317) 849-5412
March 6, 1981 —
Tulsa, OK (214) 234-3391
March 9, 1981 —
Boston, MA (617) 237-3400
March 10, 1981 —
Stamford, CT (516) 293-2900
March 11, 1981 —
New York, NY Area (516) 293-2900
March 12, 1981 —
Philadelphia, PA (215) 657-2711
March 13, 1981 —
Baltimore, MD (301) 730-1510
March 16, 1981 —
Orlando, FL (305) 834-7000
March 17, 1981 —
Fort Lauderdale, FL (305) 771-0320

And how:

Fill out and mail FAST to guarantee your reservation. Or call the local number in your area.

Name _____

Title _____ Phone ( ) _____

Company _____

Address _____

City _____

State _____ Zip _____

Seminar Location _____

Mail to: Fairchild FAST Seminar
P.O. Box 7880LSI
Mountain View, CA 94042

FAST made easy.

the intersection of the vertical line with the sinc envelope gives the normalized value of the fundamental. This value multiplied by V_{dc}, found earlier, gives the actual amplitude of the fundamental. Repeating this procedure at X-axis values that are integral multiples of k yields corresponding values for the harmonics.

For example, consider a square wave that goes from zero to V_pV. Such a square wave can be viewed as a pulse width modulated signal with period T = 2W. The ratio k, in this case, is W/2W = 0.5 and V_{dc} = $WV_p/2W$ = $V_p/2$, as it is expected. From Fig 4, the amplitude of the fundamental is 0.65 V_p, and the amplitude of the second harmonic (and that of every other even numbered harmonic) is zero, again, as expected from a square wave.

Applications

When a digital PWM is used as a DAC, its output must be filtered to remove the fundamental and the harmonics, because information in the modulated signal is contained in its dc value variations. To do this, a low pass filter is required. Practical filters, however, are imperfect and have finite roll-off; therefore, after filtering, residual noise on the signal can be calculated by using the spectral representation. The maximum bandwidth of the output cannot exceed the fundamental frequency; with practical filters, it will be considerably lower.

When a digital PWM controls the speed of a motor, it is important to have a fundamental frequency that is sufficiently higher than the mechanical resonant frequency of the motor so that the motor acts as a mechanical low pass filter. On the other hand, if the fundamental frequency is too high, the electrical inductance of the motor will filter out all of the harmonics. Then, the time domain signal seen by the motor will have dc characteristics, and the advantages of using a modulated signal during start-up and low speed operation will be lost.

Finally, high accuracy and high bandwidth in a digital PWM demand a very high clock frequency. For example, with an 8-bit modulator running at 20 MHz, the fundamental will lie around 80 kHz. For 12-bit accuracy, the fundamental drops to only 5 kHz. Therefore, although very high resolution DACs are easy to build using digital PWMs, their bandwidth is quite limited.

Bibliography

R. A. Gabel and R. A. Roberts, *Signals and Linear Systems*, John Wiley and Sons, 1973

L. R. Rabiner and Bernard Gold, *Theory and Application of Digital Signal Processing*, Prentice-Hall, 1975

The TTL Data Book for Design Engineers, Second Edition, Texas Instruments, Inc

Please rate the value of this note by circling the appropriate number in the "Comments" box on the Inquiry Card.

High 713 Average 714 Low 715

ADD-ON ADD-IN

MEMORY...FROM THE LEADER

PDP®-11/70-compatible
2.0MB ADD-ON

There's lots of good reasons to buy your ADD-ON/ADD-IN memory from the leader.

For starters, there's the wide range of core and semi mini-memories we offer. The industry's widest. In fact, Dataram is the only company in the world supplying minicomputer-compatible core and semiconductor main memory and disk emulation systems. The *only* company.

And Dataram ADD-ON/ADD-IN products do more. Like save money...as well as valuable space in your minicomputer. And they increase throughput and improve overall performance.

Just some of the reasons why Dataram is the leading supplier of ADD-ON/ADD-IN memory for the minicomputer industry...and shipping at an annual rate of $25 million.

Want more reasons? If you're using a minicomputer, and want to get more for your memory dollar, talk to us. We're very reason-able. Dataram.

DEC and PDP are registered trademarks of Digital Equipment Corporation.

DATARAM CORPORATION

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

	CORE	SEMI
DEC®	✓	✓
DATA GENERAL	✓	✓
INTERDATA	✓	✓
VARIAN	✓	
INTEL	✓	

I'd like more answers about mini-memories for my _____ minicomputer.

☐ Please send information.
☐ Please have a salesman contact me.

Name _____

Title _____ Phone _____

Company _____

Address _____

City _____ State _____ Zip _____

Canada: Ahearn & Soper Ltd., Alberta, British Columbia, Ontario, Quebec • **Finland:** Systek OY, 737-233; **France:** YREL, 956 81 42 • **Hungary/Poland/Rumania:** Unitronex Corporation, WARSAW 39 6218 • **Italy:** ESE s.r.l., 02/6073626 • **Netherlands:** Technitron b.v., 020-45 87 55 • **Sweden:** M. Stenhardt AB, (08) 739 00 50 • **Switzerland:** ADCOMP AG, 01/730 48 48 • **United Kingdom:** Sintrom Ellinor Ltd., (0734) 85464 • **West Germany:** O.E.M.-Elektronik GmbH, 07 11-79 80 47 • **Australia/New Zealand:** Anderson Digital Equipment, (03) 543 2077 • **India:** Industrial Electronic Instruments, 79281 • **Israel:** Minix Computers & Systems Ltd., 03-298783 • **Japan:** Matsushita Electric Trading Co., Ltd., 03 (435) 4501

CIRCLE 76 ON INQUIRY CARD

HOW FAST DO YOU WANT TO HIT THE STREET WITH YOUR MICRO SYSTEM?

During these last two years, thousands of companies have gone into business with the sole purpose of developing micro-based products.

And in an environment as explosive as that, you are either very quick. Or very dead.

So, although building your micro-based system from scratch could be a glorious experience, we would advise you to buy one of our single board computers. Or even better, our prepackaged systems.

If you call your local Data General industrial electronics stocking distributor* to order your development system this morning, you'll be able to start working on your software this afternoon.

And while your competition is pounding out assembly code, you'll be working with big computer languages. An MP/FORTRAN with multi-tasking. An MP/PASCAL that executes at assembly language speeds. An MP/BASIC that lets you write enormously complex programs that take up very little space. And MP/OS. A micro sub-set of AOS, the operating system anyone who knows operating systems will tell you is the most sophisticated in the world.

With system tools as powerful as these, you could be out selling your micro-based product while other guys are still trying to figure out how to use the wimpy tools that the semiconductor companies are offering.

And as you get bigger, and get into bigger systems, everything you've done will grow right along with you. Because Data General micros are compatible with every other Data General computer.

If you are still unconvinced, let us tell you a story.

A certain system house we know assigned two teams the same micro project using two different computer companies. The team using Data General finished in four months. The team not using Data General took nearly seven months.

Would you care to guess whose micros they are using now?

Data General
We take care of our own.

*SCHWEBER, HALL-MARK, KIERULLF, ALMAC/STROUM, R.A.E. in Canada.

Glitch Grabbing made easy.

When digital and analog worlds meet the relationship between state and timing analysis becomes critical. Today Philips brings you one instrument that both locates *and* analyzes digital faults. Instantaneous changeover from state to timing analysis shows instant comparison of software commands and hardware results.

If you're active in design, development, production, maintenance and service of digital systems and equipment, you'll thank Philips for bringing you the best of both worlds.

The PM3500 100MHz 16 Channel Logic Analyzer

- 505 x 16 bits memory format
- Spots 3ns glitches
- Choose binary, hex, octal, mapping or timing display modes
- Handles all logic families
- Offers compare mode facilities
- Tiny and inexpensive input probes can be grouped or used separately—even several feet apart
- Comprehensive automatic diagnostic routines

For nationwide sales and service information call 800-631-7172, except in Hawaii, Alaska and New Jersey. In New Jersey call collect (201) 529-3800, or contact Philips Test & Measuring Instruments, Inc., 85 McKee Drive, Mahwah, NJ 07430

From Philips, of course.

PHILIPS Test & Measuring Instruments

PHILIPS

CIRCLE 77 ON INQUIRY CARD

Improved Reader for Magnetically Encoded ID Cards

Hybrid circuitry accommodates variations in insertion speed, yet is simpler than an all digital version

A hybrid demodulator in an electronic card reader for magnetically encoded identification cards is simpler and less expensive than equivalent all digital circuits. In the reader, used to control access to test facilities at the Jet Propulsion Laboratory (JPL), a pickup senses the magnetic variations on the card stripe and generates a phase encoded digital signal. The card used at JPL is an identification (ID) card the size of a typical credit card.

Rate at which the user inserts the card defines the period of the clock that synchronizes the phase encoded data. Although the insertion speed (by hand) can vary by a factor of 20, the demodulator is able to extract the data from the coded signal, allowing the reader to compare the pattern with a preset recognition code. If a match is found, the reader unlocks a door or performs some other positive action for the user.

The identification code is recorded on the card in binary diphase form [Fig 1(a)]. A data 0 is recorded as a signal level transition at the midpoint of the clock period; and a data 1 is recorded as one transition at one-quarter of the clock period and another at one-half the clock period. The clock period is defined as twice the width of a 0 bit and depends on the speed at which the card stripe passes through the magnetic pickup. [Another way of looking at this code is that a string of 0s is recorded at the clock frequency (f), and a string of 1s is recorded at twice the clock frequency (2f).] This form of modulation is standard in the industry, and is of the same form as used by the credit card industry, digital recording for storage on disc or tape.

In the demodulator, shown in Fig 2, the diphase signal from the pickup is fed to a level converter, which changes the pickup pulses to levels compatible with transistor-transistor logic (TTL) circuitry. A transition detector monitors these diphase signals and detects logic level changes. Whenever a transition in either direction occurs, the transition detector produces a 6-μs pulse [Fig 1(b)].

An autocorrelation method is now used, which stores the time period of the previous bit and uses it to compare the time period of the following bit. It is implemented as follows: A clock and data converter separates the clock pulses from the

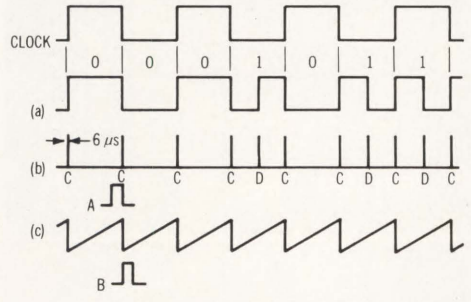


Fig 1 Diphase code (a) is used in magnetic key card reader. Transition detector in reader produces stream of clock and data pulses (b) from the coded information. Peak voltage of ramp waveform (c) is proportional to clock period and is used in demodulating coded signal. At least 10 reference clock pulses are stored in front of data on card stripe

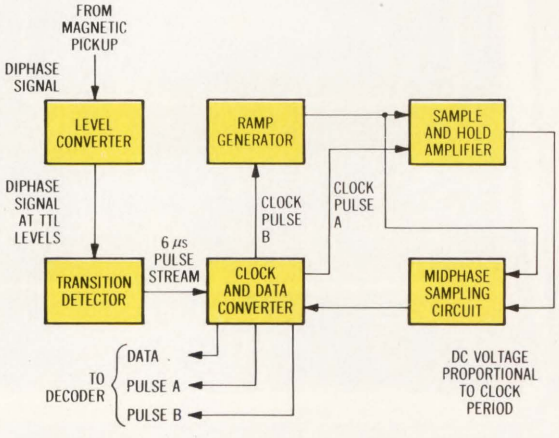


Fig 2 Demodulator portion of card reader separates data signals from clock signals. Ramp generator, sample and hold amplifier, and midphase sampling circuit—all of which are analog circuits—identify midpoints of variable length clock periods so data can be extracted

data pulses. It includes a synchronous generator that produces a 6-μs pulse (A) immediately followed by another 6-μs pulse (B) that signals the start of a clock period.

Pulse B triggers a ramp generator [Fig 1(c)] that applies a linearly rising output to a sample and hold amplifier. When the next pulse A is applied to this amplifier, the amplifier stores the terminal value of the ramp voltage, which ranges from 0.5 to 10 V, depending on the length of the clock period.

A midphase sampling circuit compares the stored voltage from the previous cycle and the voltage ramp of the present cycle to determine the midpoint of the current data period. The circuit then sends a sampling pulse to the clock and data converter so that it can check its input to determine whether a data pulse arrives within the ramp cycle. If such a pulse is received, it is recorded as a data 1; if no pulse is received, a 0 is recorded.

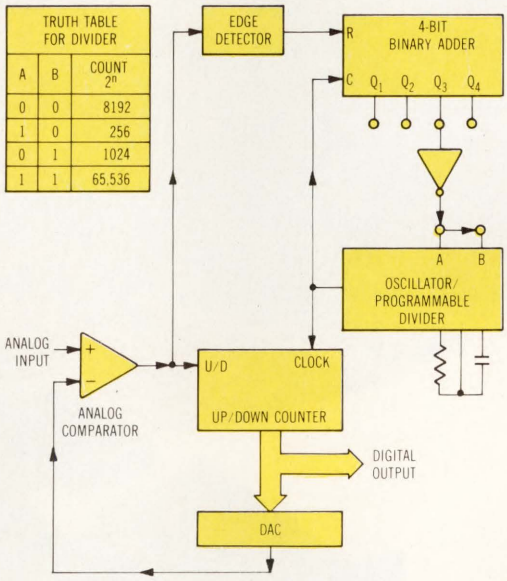
Possible variations in the clock period from one ramp cycle to the next are accounted for by generating a midphase sampling pulse of longer than the 50% midpoint window. Up to 75% of the ramp cycle can be examined for the presence of a data pulse. This information is then transmitted to the pattern decoder. On separate lines, the clock and data converter also transmits pulse A and pulse B information to the decoder.

Note

This work was done by Ta Tzu Wu of Caltech for NASA's Jet Propulsion Laboratory. Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to the California Insititute of Technology, Pasadena, CA 91109.

Variable Clock Rate ADC

Circuit uses different rates to optimize performance in both searching and tracking



An analog to digital converter (ADC) operates at two different rates so that low amplitude noise is reduced without the loss of transient response. A slow clock rate is used while the converter is tracking a signal, and a fast clock rate is used when the converter is searching for a signal. During tracking, when sensitivity is important, the slow clock reduces noise. In the search mode, when the signal may be changing rapidly, the fast clock ensures rapid response.

In previous ADCs for low frequency instrumentation, noise was reduced by adding a low pass analog filter or by permanently reducing the clock rate. However, these methods made the converter too slow.

In the new ADC (see figure), an up/down counter is forced to equal the analog input and then to track it. The slew rate, or bandwidth, of the converter is a function of the clock rate.

Transitions at the output of an analog comparator are sensed by an edge detector. Transitions at the clock rate signify that the converter is tracking, while an absence of transitions signifies searching. When the converter is tracking, a 4-bit binary adder is constantly being reset, causing the converter to be clocked by a programmable divider at f/65,536, where f is the oscillator frequency. If four successive clock pulses occur without an up/down transition being detected, the converter clock changes to f/8192, or eight times the tracking rate. Of course, many other clock rates and track/search rate ratios are possible, and the transitions from track to search can be made at absent transition sums other than four.

Note

This work was done by Phillip C. Lipoma of Lockheed Electronics Co, Inc, for Johnson Space Center.

OUR STREAMERS VS. THEIRS.

Remember all the hoopla?

Quarter inch streamer tapes were heralded as the long-awaited answer to Winchester backup.

Trouble is, they turned out to be longer-awaited than anybody anticipated.

OEM's have yet to receive a single shipment of production streamer tape units from the early suppliers who made all the fuss.

Now that the commotion has died down, Archive quietly introduces its streamers and claims technological leadership in the field.

And if it seems you've heard that song before, consider that we've already made deliveries of Sidewinder basic & intelligent ¼" streaming cartridge tape drives.

Designed specifically for Winchester backup, the Sidewinder offers 30 or 90 IPS tape speed, 10 or 20 Mbytes of formatted storage in either basic or easily integrated intelligent units.

Call us today and learn how to get your Winchester project back on target.

Archive Corporation, 3540 Cadillac Avenue, Costa Mesa, California 92626, (714) 641-0279, Telex: 683466.

ARCHIVE

Programming the 8086— Part 2: Addressing Modes

Stanley Mazor
Intel Corporation
1350 Bordeaux Dr, Sunnyvale, CA 94086

This article, second of a series discussing programming techniques for the 8086 microprocessor, builds on the explanation of register instructions presented in Part 1, and concentrates on the addressing modes available to the assembly language programmer. The conclusion, to be published in February, will cover procedures and parameter passing.

An 8086 microcomputer system can have up to 1M bytes of memory, and each byte is individually addressable via the 20 address lines. Memory is partitioned into segments; at any instant as many as four different segments can be accessed. These segments, the code segment (CS), stack segment (SS), data segment (DS), and extra segment (ES), are located when the programmer loads the segment registers with the segment starting address. (See Fig 1.) Various methods of addressing a byte of data in the current data segment can be analyzed by examining the addressing modes designated by the instruction format.

Register to register instruction format was discussed in Part 1 (*Computer Design*, Dec 1980, pp 130-136). A typical layout of the instruction (Fig 2) shows that the REG and R/M fields each designate 1 of 8 registers. The W bit selects byte mode or word mode. When data are to be accessed from the data segment of memory, the MOD and R/M fields have 24 combinations to specify memory addressing mode; these combinations are depicted in the shaded portion of the figure.

(continued on page 152)

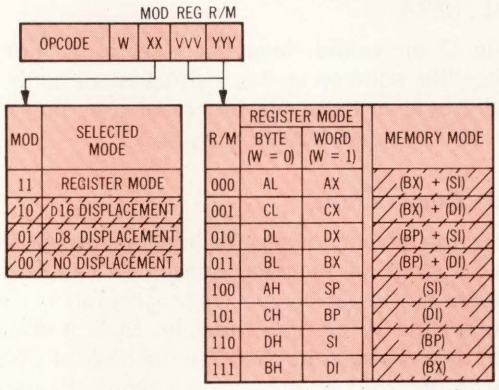


Fig 2 Register to register addressing. MOD field designates register mode, and R/M and REG field designate one of eight registers

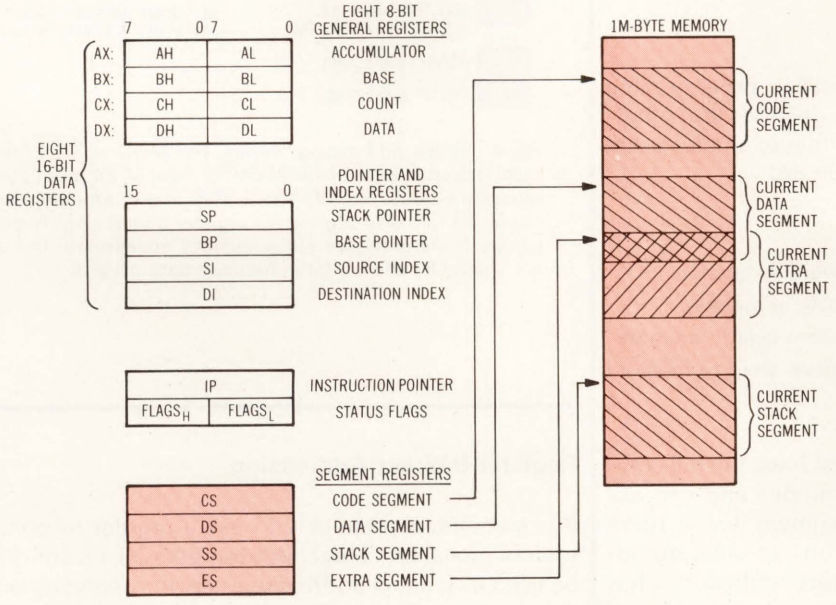


Fig 1 Segment registers address memory. Four segment registers augment general registers described in Part 1. Each receives starting address of one memory segment, allowing program to access data in any of four segments

Direct Addressing Mode

In the most common addressing mode, the memory address is contained within the instruction. For the 8086, this address is 16 bits (2 bytes) and permits addressing of any byte in the current 64k-byte data segment. The symbolic instruction for moving one byte of data in the AL register to a variable in memory (symbolically called BETA) and the assembler generated machine code are illustrated in Fig 3. This instruction occupies 4 bytes of storage and contains the 16-bit address of BETA. Note that the five addressing mode bits are set

MOD = 00
R/M = 110

for direct addressing. The W bit is set to 0 because AL register is a byte register, and the direction bit (D = 0) indicates that the register is a source of data. If the instruction had used BETA as the source, ie,

MOV AL, BETA

then the D bit would have been set to 1. For word variables, the address in the instruction designates the low order byte of data; the processor uses that byte as well as the next data byte in memory.

Variable Declarations

The 8086 assembler provides declarations for allocating a byte or a word of memory space for variables, and remembers the variable type when generating machine code to set the W bit appropriately. Size of immediate constant data is also controlled, on the basis of whether a variable is declared as a byte or a word. Examples of these declarations

```
BETA    DB    3           ; constant byte 3
WAREA   DW    0           ; constant word 0
TEMP    DB    ?           ; uninitialized byte
V       DB    50 DUP (0)  ; array of 50 zeros
```

feature "strong typing," which simplifies programming and reduces the number of symbolic opcodes that otherwise would have to be established. Other examples using these variables in direct address mode are

```
MOV BX, WAREA      ; data word to register
INC BETA           ; data byte in memory
MOV BETA, 10       ; immediate byte to memory
ADD WAREA, 50      ; immediate word to memory
```

Most 8086 instructions (including shifts) have the full complement of 24 memory addressing modes and can address any byte or word in the data segment with a 16-bit direct address. Of the 24 combinations of memory addressing, only one combination, direct addressing, has been discussed. All 24 combinations are shown in Fig 4.

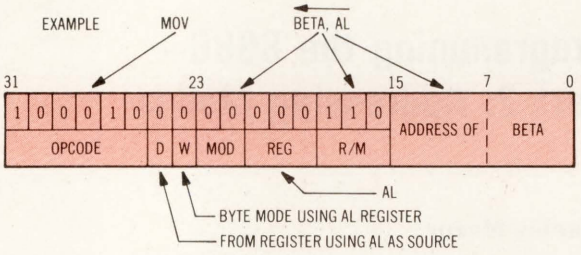


Fig 3 Direct addressing. Instruction moves byte contained in AL to data location BETA, whose 16-bit address occupies last two bytes of 4-byte instruction. Direct addressing is exception to general rule that MOD field designates number of address bytes actually contained in memory reference instruction

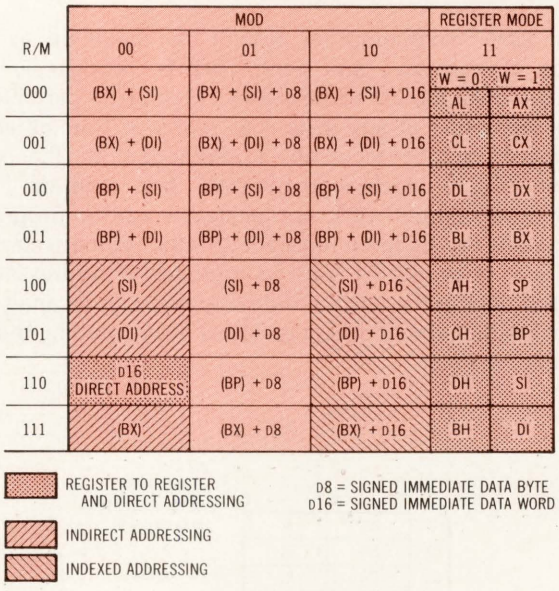


Fig 4 8086 addressing modes. For MOD = 0, 1, or 2, eight possible values of R/M define total of 24 memory addressing modes. For MOD = 3, R/M and W bit define additional 16 forms of register to register addressing. Register names in parentheses show indirect access. D8 and D16 are signed 8- and 16-bit immediate data offsets

Register Indirect Addressing

It is sometimes preferable to use a register to point to a memory location. Three 8086 registers (SI, DI, and BX) can be used as indirect address registers for operating on data in memory. When a programmer uses this mode, the

Converting Fahrenheit to Celsius Using a ROM Table

Problem

An 8-bit value representing a temperature in the range of 32 to 122 °F is a memory location symbolically called FTEMP. It is to be converted to degrees Celsius by use of a table of Fahrenheit temperature values stored in read only memory (ROM), starting at a location symbolically called CTABLE. The first table entry is the temperature value corresponding to 0 °C. Each successive entry corresponds to an integral Celsius degree 1, 2,..., 50 °C. The converted value is to be stored at a byte location called CTEMP.

```
CTABLE       DB   32  ; ENTRY FOR 0 °C, 32 °F
CTABLE + 1   DB   33  ; ENTRY FOR 1 °C, 33 °F
CTABLE + 2   DB   35  ; ENTRY FOR 2 °C, 35 °F
                .
                .
                .
CTABLE + 50  DB  122  ; ENTRY FOR 50 °C, 122 °F
```

Solution

A program loop is written to compare the value of FTEMP with each entry of the table until a corresponding value is found. The position of the corresponding table entry is used directly as the converted Celsius temperature. The positions of the entries in the table are treated as if they were numbered from 0 to 50.

The table is searched, starting with the last entry (CTABLE + 50), and ending with the first entry (CTABLE). FTEMP corresponds to an entry if it is greater than or equal to the table entry values. For example, if FTEMP is 34, it corresponds to the table entry for 1 °C at CTABLE + 1.

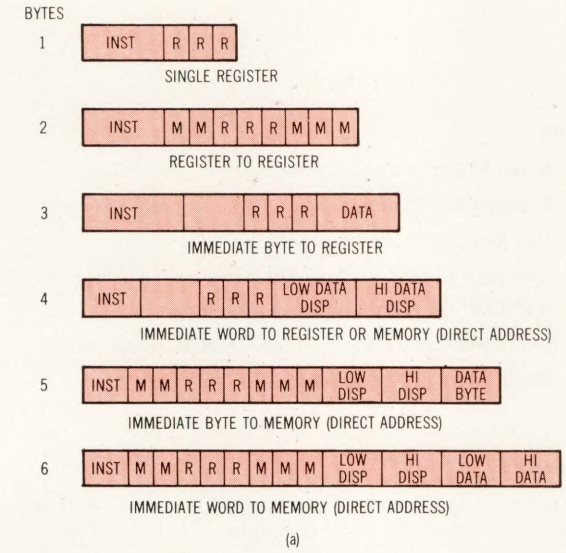
The loop instruction decrements CX by 1, and jumps (loops) if CX ≠ 0. It is convenient, therefore, to search from CTABLE + 50 to CTABLE + 1. Step 1 initializes the CX to 50, which causes it to loop 50 times and terminate when CX = 0. The count is used as an index in step 4, but first must be moved to an index register in step 3. Note that CX can be used with the loop instruction but cannot be used as an index register. Step 4 performs the comparison of FTEMP (which is loaded into AL in step 1) with the current (indexed) entry in the CTABLE. If FTEMP is greater than or equal to the value of the CTABLE entry, a jump is made to exit the loop and store the result in step 7. When CX is decremented to 0, the loop terminates and this program produces a zero result for any FTEMP value less than or equal to the first entry in CTABLE. Also, any FTEMP value greater than the last CTABLE value results in the answer 50.

Steps

(1) Move FTEMP to AL register
(2) Initialize loop counter to 50
(3) Use loop count as index [SI]
(4) Compare FTEMP with CTABLE [SI]
(5) If FTEMP ≥ CTABLE [SI], go to step 7
(6) Decrement loop count (CX); if CX ≠ 0, go to step 3
(7) Store index (CL) at CTEMP

Program

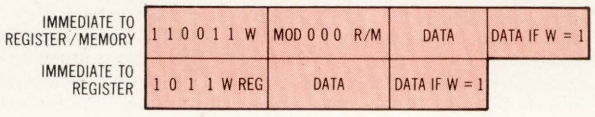
Symbolic Label	Mnemonic Opcode	Symbolic Operands	Address Type
STP 1:	MOV	AL, FTEMP	; Direct
	MOV	CX, 50	; Immediate
STP 3:	MOV	SI, CX	; Register
STP 4:	CMP	AL, CTABLE [SI]	; Index direct
	JGE	STP 7	; Relative
	LOOP	STP 3	; Relative
STP 7:	MOV	CTEMP, CL	; Direct



(a)

INSTRUCTION	BYTES USING GENERAL FORM	BYTES USING SPECIAL FORM	BYTES SAVED
PUSH/POP REGISTER	2	1	1
MOVE IMMEDIATE DATA TO REGISTER	3	2	1
ACCUMULATOR DIRECT ADDRESS MEMORY	4	3	1
INCREMENT/ DECREMENT REGISTER	2	1	1
ARITHMETIC: IMMEDIATE DATA WITH ACCUMULATOR	3	2	1

(b)



(c)

Fig 5 Instruction length. In (a), one instruction can have six different lengths ranging from 1 to 6 bytes depending on addressing mode. In (b), special form capitalizes on unused opcode bits to reduce size of certain commonly used combinations of opcode and addressing mode. For example, in (c), special form of "move immediate data to register (or memory)" instruction saves one byte of program storage

designated register is enclosed in square brackets, as follows: MOV AL, [BX], which reads, Move into the AL register the data byte in memory at the location addressed by the contents of the BX register. The instruction length for this format is 2 bytes, shorter than that of the direct address mode since no address displacement appears in the instruction stream. In this case, the operand can be a source or destination depending on the D bit, as previously discussed.

Indexed Addressing

When an element of a table or vector of data in memory is to be accessed, an index register can be effectively used to select the item. In this mode, the base address of the array is contained as a direct address in the instruction, and the subscript is located in the index register. For example, to access the 50th element of vector V, the subscript 50 might reside in the SI index register, and the instruction would contain the starting address of vector V. In writing symbolic assembler programs, the index register to be used is written in square brackets as follows: MOV AL, V[SI]. Of course, the programmer can change the subscript index value in SI dynamically and select different items from the table. There are 4 possible index registers, with short and long displacement option; double indexing simplifies complex array handling. (See Fig 4.)

Instruction Size

The number of bytes occupied by the instruction depends on the addressing mode used and whether immediate data are required. Fig 5 tabulates some of these variations in instruction lengths from one to six bytes.

In addition to these formats, the 8086 has some special but redundant forms that reduce the number of bytes required for frequently used instructions. They include the instructions shown in Fig 5(c), which generally result in one less byte of program storage per instruction. The programmer need not remember these, as the assembler automatically selects the shortest possible form.

Summary

Application programs manipulate data in memory, and the programmer allocates memory space for variables using assembly language declarations. These declarations assign symbolic names and associate a data type (byte/word) with the variable. In referring to data variables in the data segment, the 8086 assembly language programmer has many choices of addressing modes and index registers; experienced programmers appreciate the versatility of double indexing, and novice programmers will produce shorter and more efficient programs.

Complete systems for computer graphics and image processing.

And, we do mean complete! Grinnell systems can include computers, disc drives, terminals and software operating systems. Plus a FORTRAN software and driver package; high resolution TV monitor, camera, and hard copy color printer.

There are also other options to meet any special requirement you might have.

Of course, you may already have some of the necessary hardware. That's why Grinnell systems work with standard TV monitors and cameras, and why plug-compatible interfaces are available for most minicomputers.

We also give you a complete product line to choose from:

GMR 270 Series: 512 x 512 resolution frame buffers and full color pipeline image processing systems.

GMR 260 Series: 1024 x 1024 resolution frame buffers for grey scale, black and white, pseudo color and full color.

GMR 27 Series: High speed, modular graphic and image display systems.

GMR 37 Series: Low cost graphic display systems.

So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a complete system that can do it. For complete specifications and/or a quotation, call or write today.

GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920, TWX (910) 338-2145

CIRCLE 80 ON INQUIRY CARD

Whether you want streaming or start/stop, Cipher has the tape drive you need.

Cipher Data Products is the leading independent manufacturer of tape drives. That means we can give you more combinations of size, speed, capability and cost for meeting any application you can name. From our low cost and versatile streaming drives to our high performance yet cost-efficient vacuum column drives.

Take our exciting Microstreamer™ family.

Now you have a choice. You can take our famous Microstreamer dual speed streaming tape drive. Or you can order our soon-to-be-famous higher capacity Microstreamer 2. They both offer the advantages of high performance Winchester disk backup combined with effective input/output performance.

The original Microstreamer stores up to 46 megabytes of data on a single 10½" reel of tape. The new Microstreamer 2 doubles that capacity to 92 megabytes per reel. Whichever you choose, you can back up your Winchester disks in a matter of minutes, with fewer media changes.

That's exciting, but there's more.

There may be other announced streamers, but when you get a Microstreamer you get more than just backup. Take a look at all of these exclusive features:

- ☐ completely automatic tape loading and threading
- ☐ 25 ips speed for normal start/stop applications
- ☐ choice of 1600 or 1600/3200 selectable recording density
- ☐ automatic diagnostics
- ☐ smaller size
- ☐ lower cost

Catch the excitement!

Call us today at (714) 578-9100. Or write for our free product brochure—10225 Willow Creek Road, San Diego, California 92131.

cipher data products, inc.

the exciting company

COMPARE FLEXIBILITY.

Model 950

- *Advanced editing with wraparound*
- *Smooth scrolling*
- *15 baud rates (50B to 19.2kB)*
- *Protected fields*
- *Underlining*
- *Split screen with line lock*
- *Non-glare screen*
- *Programmable function keys*
- *15 special graphics characters*
- *Versatile screen attributes*
- *Self test*
- *25th status line*
- *Buffered auxiliary port*
- *14 X 10 character resolution*
- *Integral modem option*
- *Tiltable screen*

Tailor this smart CRT terminal to your particular needs and make it your own. It has the flexibility and brains to provide all the performance you need but is priced to make sense whether you need 10 or 1,000.

The TeleVideo model 950 detachable keyboard CRT Terminal has 11 special function keys—22 functions with the shift key—that can readily be programmed to your requirements using 256 bytes of on-board RAM.

You needn't stop there. You can change keys, key functions, even keyboard locations. And the 950's microprocessor based design means you can customize the firmware for your system.

Of course the 950 has premium TeleVideo performance—advanced editing with wraparound, split screen with line lock, and smooth scrolling. It also features a 25th status line, speeds to a true 19.2 kilobaud, and 15 special characters for powerful line graphics.

Contact TeleVideo for a detailed brochure, or call today to discuss how you can use these capabilities to make this terminal uniquely yours. TeleVideo, Incorporated, 2149 Paragon Drive, San Jose, CA 95131. (408) 946-8500.

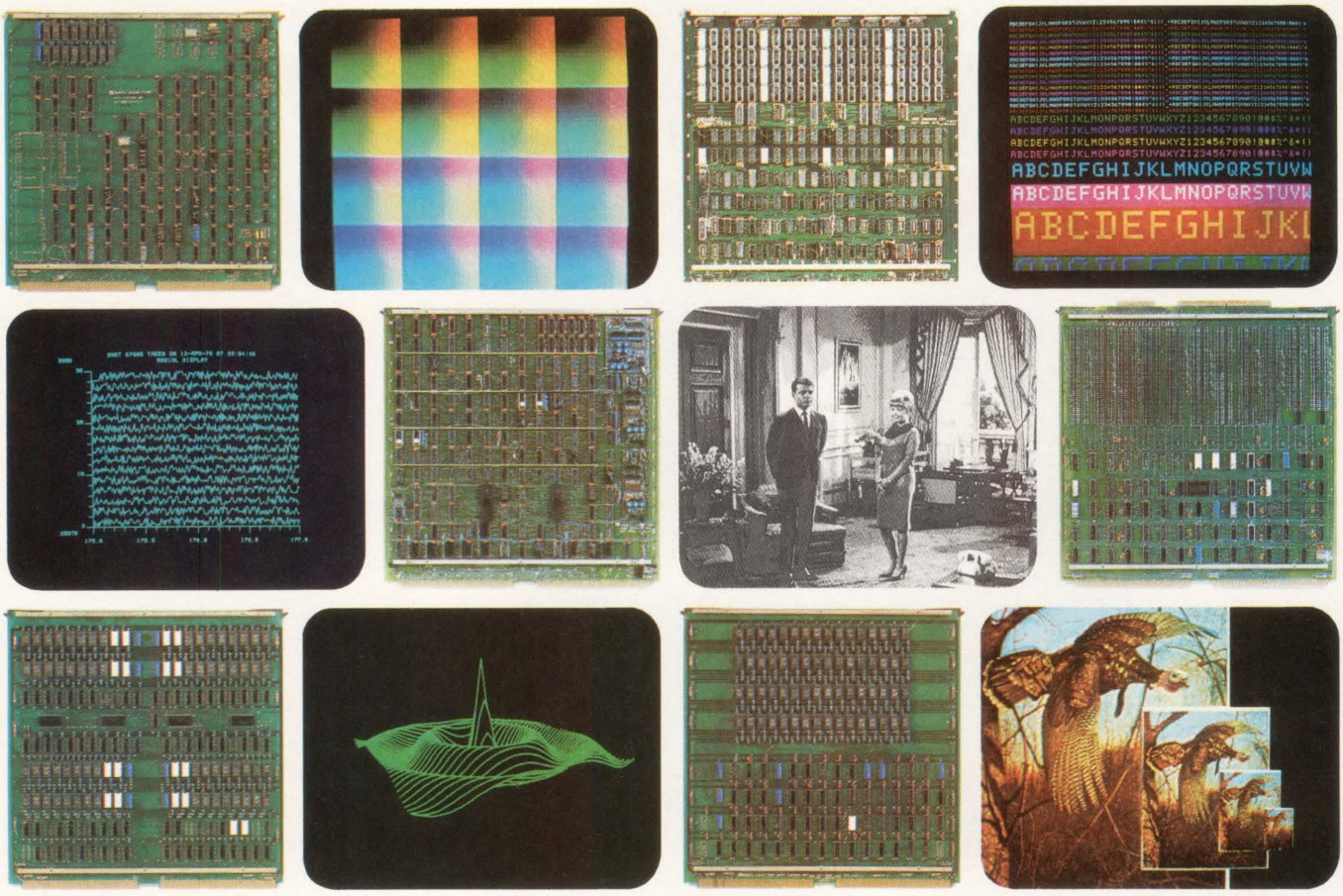
Nationwide Field Service is available from General Electric Company, Instrumentation and Communication Equipment Service Shops.

TeleVideo®

COMPARE PRICE.

CALIFORNIA Costa Mesa (714) 557-6095 • San Jose (408) 946-8500 • MASSACHUSETTS Boston (617) 668-6891
NEW YORK/NEW JERSEY Paramus (201) 267-8805 • TEXAS Dallas (214) 980-9978

CIRCLE 82 ON INQUIRY CARD



THE GRAPHIC SYSTEM DESIGNED FOR ONE APPLICATION. YOURS!

If you need high resolution (1280 x 1024) for CAD/CAM... 17 million colors and 256 gray shades for imaging... high speed line drawing for seismology and simulation... special symbols and alphanumerics for process control ... high speed data transfers for command and control... scrolling capability for data logging... and flicker-free viewing... then you've found your system.

You get all the graphics capability you need... and you don't have to buy more than you need... with Genisco's GCT-3000 raster graphic display systems. Only GCT-3000 has the unique modular design which lets you expand the capabilities of a basic four board system with a variety of optional modules, devices and software. Create low, medium or high resolution, monochrome or color, highly interactive or display only. Add high speed graphics manipulation and simplify applications programming with Genisco's package of Fortran-callable subroutines. No matter how simple or state-of-the-art your system, you'll get the best price/performance characteristics available.

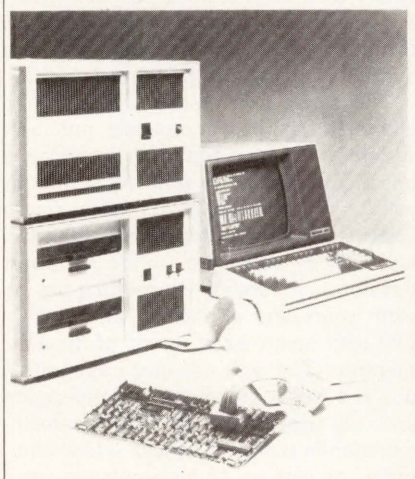
And you get all the advantages of raster scan technology.

Don't settle for a compromise. Call or write for a demonstration of Genisco's GCT-3000. We'll show you the system we've designed for you. Genisco Computers. 3545 Cadillac Ave., Costa Mesa, CA 92626. (714) 556-4916.

GENISCO COMPUTERS

A Division of Genisco Technology Corporation

Microcomputer Development Lab Emulates Range of 8- and 16-bit Microprocessors



8550 development lab offers resources for full microcomputer product design, software facilities for both assembly and high level languages, and complete incircuit emulation and hardware testing capabilities

Realtime emulation for a variety of 8- and 16-bit microprocessors, and complete design, debugging, and integration tools are provided by the 8550 microcomputer development lab. A single user system, the lab is the first in the 8500 modular MDL series. This series, available from Tektronix, Inc, PO Box 1700, Beaverton, OR 97099, provides full compatibility between systems in the series, including software support, and all of the company's multivendor, realtime emulation support packages.

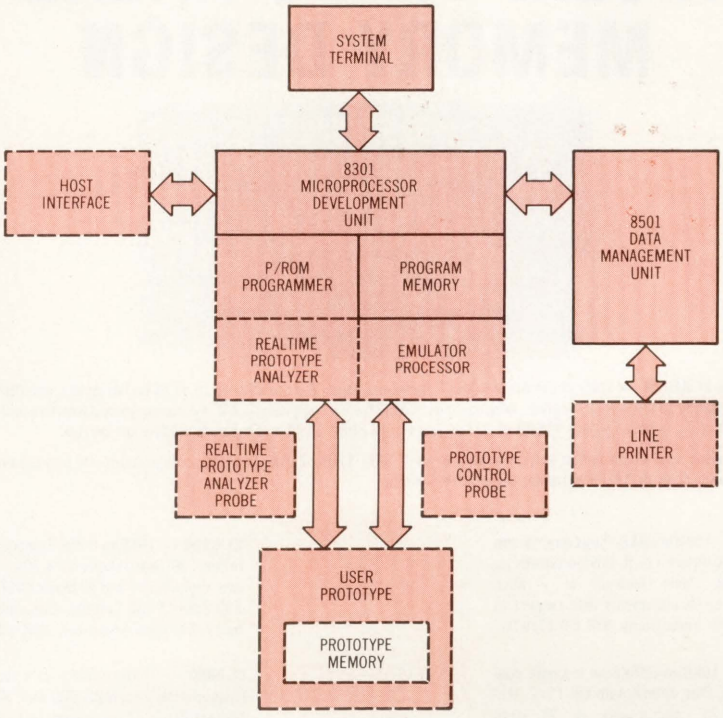
Major components of the development lab are the 8301 microprocessor development unit and the 8501 data management unit. The development unit contains the system software, DOS/50 operating system, 32k bytes of static system memory, 32k bytes of static program memory (expandable to 64k), language processor, and emulator controller. The data management unit handles files and auxiliary I/O for the operating system and manages the movement of user files between dual-sided, double-density (2M-byte capacity) floppy discs and the development unit.

8086/88, 68000, and Z8001/2 16-bit microprocessors are emulated in realtime, with support for the full address ranges of each and with use of symbolic debugging. The 8086 emulator will support the 8-MHz 8086-2, 4MHz 8086-4, and 5-MHz 8088, and is compatible with the 8087 and 8089; the 68000 emulator will provide debugging support at 8 MHz; and the Z8000 emulator will support the 4-MHz Z8001 and the 4-MHz Z8002. A personality card and probe adapter are required to switch chips.

The operating system supervises general I/O; file creation and maintenance; program assembly, compilation, execution, monitoring, and debugging; P/ROM programming; and communication. Program entry and editing are provided by a standard line oriented editor or an optional advanced CRT oriented editor that allows both line and screen oriented editing.

Assembler software packages for the system include macros, language extension, library generator, and linking capabilities. Macro capability allows the designer to access frequently used sets of code by referencing the macro by name. Assembly time string manipulation, including variable length strings both inside and out of macros, enhances code management. English language

(continued on page 160)



Basic 8550 microcomputer development lab consists of two major components: 8301 microprocessor development unit, and 8501 data management unit. Also shown are prototype board, prototype control probe, and system terminal

diagnostics provide error messages that locate the line containing an error. The completed and assembled object code is stored on disc in a binary format file; commonly used object modules may be stored in library files. The linker joins and locates multiple code segments into a complete, executable program. Additionally, the conditional assembler allows the creation of a customized final program by testing conditions to determine which code segments are assembled into the final program.

Options available for the system include Pascal, a realtime prototype analyzer (RTPA), 16-bit emulation, 16-bit analyzer, P/ROM programming, communications utilities, and emulator processors and prototype control probes for selected microprocessors.

Pascal is now available for 8080/8085 microprocessors; versions will be available for the 8086, Z8000, and 68000 16-bit microprocessors at later dates.

A trigger trace analyzer will be available as an integration tool for 16-bit emulators. This analyzer will use a 255-word x 62-bit trace buffer, four flexible event triggers, numerous breakpoint options, and high speed (125-ns/cycle) storage capability.

P/ROM programming will support the 2716/32 and 2516/32 P/ROMs and the 8748 family. The programmer can read data from a P/ROM into program or prototype memory, burn a P/ROM with data from program or prototype memory, or compare P/ROM contents with memory contents.

Extensive software and hardware communications support is available. The system can transmit and receive ASCII and binary data to or from a host computer. Along with the standard console I/O port, three RS-232-C compatible ports are available for use with peripheral devices.

This single user system will be joined within the year by a compatible, multiuser system and a host computer system, the advanced integration unit. Most options will be transportable to these future systems. The multiuser system, the 8560, will be a complete microcomputer development system supporting up to eight users and containing an LSI-11/23 CPU with up to 128k words of dynamic memory. The 8054 advanced integration unit is a self-contained peripheral station and will provide hardware/software integration in conjunction with a host computer, as well as 16-bit emulation for a single-user system. It will have a ROM based operating system, with software that allows direct access to the host computer by making the peripheral transparent to the user's CRT.

Circle 461 on Inquiry Card

Personal Computer Provides Range of Features and Capabilities

A full-featured, expandable, personal computer system, the VIC 20, available from Commodore Business Machines, Inc, 950 Rittenhouse Rd, Norristown, PA 19403, connects to any television set or monitor and provides 5k bytes of memory (expandable to 32k bytes). It uses the standard 6502 computer on a chip, as well as an MOS Technology video interface chip.

The computer offers a full range of special features and expansion capabilities. Standard features include color, full size keyboard, external expansion ports, 22-character by 23-line screen display, high resolution graphics, graphics character set, joystick/paddles/lightpen, and external plug-in memory and program cartridges. Peripherals will include a tape cassette unit, single floppy disc drive, printer, and add-on accessories to tailor the system to a variety of specific applications.

Circle 462 on Inquiry Card

"A computer system for analog measurement must be built from the ground up."

Fred Molinari, President

When analog capability is merely tacked onto a laboratory computer system, performance is predictably poor.

So when we designed LAB-DATAX, analog measurement was our primary goal.

As a result, LAB-DATAX is the highest performance microcomputer data acquisition system available today.

LAB-DATAX is designed to preserve signal integrity, eliminating noise and ground loops through a unique front connection panel.

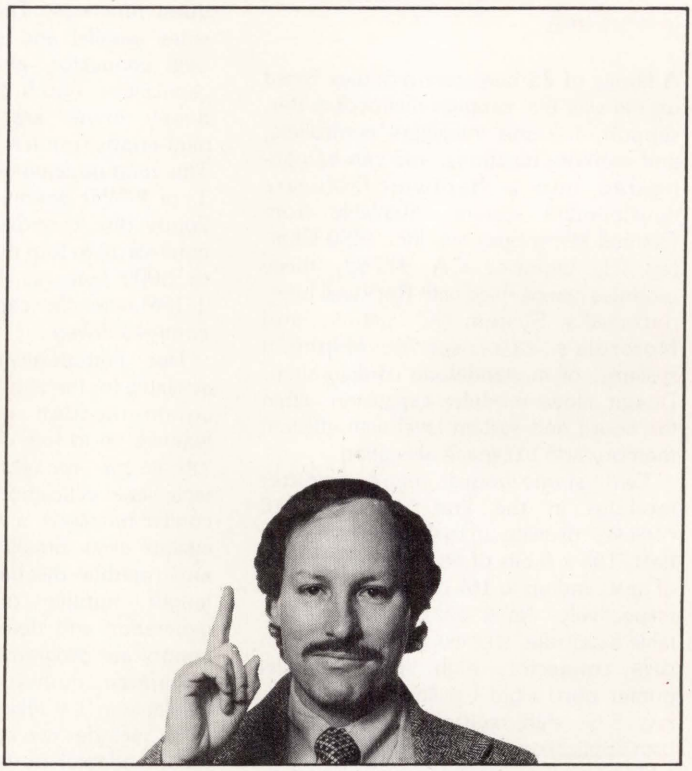
Analog problems such as wire paths, ground connections, and shielding have been met head-on and resolved.

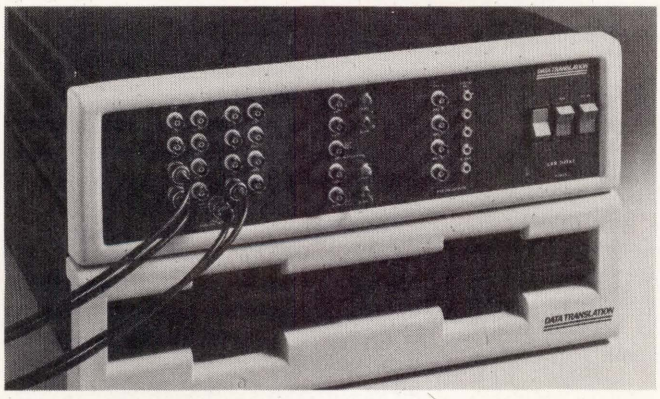
Throughput is extraordinary thanks to RT-11 FORTRAN IV software and our own DTLIB-FORTRAN callable subroutines.

In fact, the most powerful LAB-DATAX achieves continuous data throughput into memory at more than 62 times the rate of DEC's MINC-11.™

Most systems are constrained by their small selection of analog and digital I/O peripherals. They are limited in every way.

Not so LAB-DATAX. We offer you over 100 boards in configurations to ensure the performance you need.





Every model of LAB-DATAX includes an LSI 11/2™ CPU with 64KB RAM memory. A fixed and floating point instruction set. A synchronous serial interface. A bootstrap loader. A dual-drive double-density Floppy Disk. DTLIB-FORTRAN callable subroutines. And 16 slot dual-height capacity.

What's more, LAB-DATAX includes the full DEC RT-11 operating system. As well as a programmable real time clock, useful as a time base generator for analog conversions.

LAB-DATAX is even user configurable.

A broad array of analog input, analog output, and digital I/O is available for particular applications.

In all, LAB-DATAX is optimized for high performance in analog measurement. Optimized for high throughput, ease of use, and flexibility.

Proving once again that things always come out better when you start from scratch.

Data Translation, 100 Locke Drive, Marlboro, Massachusetts 01752. (617) 481-3700. Telex: 951646. In Europe: Data Translation Ltd., Rockwell House, 430 Bath Road, Slough, Berkshire/England SL1 6BB (06286) 3412. Telex: 849862.

DATA TRANSLATION

SALES OFFICES: AZ 602-994-5400; CA 213-681-5631, 415-965-9394; CO 303-371-2422; FL 305-748-9292, 813-725-2201; GA 404-455-7222; IL 312-960-4054; IN 317-788-4296; MA 617-481-3700; MD 301-636-1151; MI 313-437-0816; MN 612-441-6190; NC 919-723-8102; NJ 609-428-6060; NM 505-292-1212, 505-524-9693; NY 516-488-2100, 607-722-9265; OH 513-253-6175, 216-659-3138; OK 405-528-6071; OR 503-297-2581; PA 412-327-8979; TX 512-451-5174, 214-661-0300, 713-780-2511, 512-342-3031, 713-988-9421; UT 801-466-6522; WA 206-455-5846; CANADA 416-625-1907

LSI-11 and MINC-11 are trademarks of Digital Equipment Corp.

Hardware Modules Ease Prototyping and Product Integration

A family of 25 hardware modules based on the 6502 CPU supplies microcomputer, support, I/O and intelligent controllers, and memory functions, and can be configured into a hardware/software development system. Available from General Micro Systems, Inc, 1320 Chaffey Ct, Ontario, CA 91762, these modules can be used with Rockwell International's System-65, AIM-65, and Motorola's EXORciser development systems, or in standalone configuration. Design allows modular expansion within the board and system level with efficient memory and I/O space allocation.

Two single-board microcomputer modules in the line, GMS6506 and GMS6525, provide up to 4k x 8 bits of static RAM, 16k x 8 bits of ROM/EPROM, and 4k of RAM, and up to 16k of ROM and EPROM, respectively. An RS-232 port with selectable baud rate, IEEE 488-1975/78 port with GPIB connector, high speed parallel printer port, eight I/O lines, two timers, two 8-bit shift registers, provisions for DMA applications, and fully buffered data, address, and control lines are included on the 6506. The 6525 includes an RS-232 port with switch selectable baud rates, GPIB IEEE 488-1975/78 port, eight I/O lines, two timers, two 8-bit shift registers, and a Centronics-compatible 8-bit printer port.

GMS6508, the static memory module, is addressable in 8k x 8 arrays, and provides 24k x 8 bits of static RAM, 16k x 8 bits of EPROM/ROM, a write protect switch for each array, and base address and enable switch for EPROM/ROMs. Address and data lines are fully buffered. Dynamic memory, GMS6505, provides up to 64k of dynamic RAM, and is addressable in 4k increments. Included are onboard refresh, onboard parity generator and checker, and a write protect switch for each array. The P/ROM-ROM module, GMS6521, accepts 2708, 2716, 2758, 2316, and 2332 P/ROMs, provides up to 16k x 8 bits of RAM, and is addressable in 1k x 8 blocks. Each P/ROM-ROM also has an enable/disable switch. Featured in the nonvolatile memory, GMS6524, are up to 8k x 8 bits of EAROM with an onboard dc-dc converter, 10-year retention time (up powered), and 10-ns erase time.

Among the peripheral control modules, the GMS6512 video display generator uses a character generator ROM to produce high resolution (256 x 192) alphanumeric and graphic displays in color. Available in 4k x 8 or 8k x 8 static RAM, and in interlaced or non-interlaced modes, the module provides an onboard modulator and a programmable interrupt control on vertical retrace. GMS6514, the GPIB module, provides IEEE 488-1975/78 functions, as well as talker and listener, device clear and trigger, and serial request functions. The module also provides parallel and serial poll, onboard GPIB connector, and system controller capabilities. Two 5.25″ (13.33-cm) mini-floppy drives are controlled by the mini-floppy/printer module, GMS6519 This module features eight I/O lines and 1- or 2-MHz operation. The 8″ (20-cm) floppy disc controller module, GMS6509 controls up to four drives and transfers up to 500k bytes/s; the module features 1.18M-byte disc capacity and extensive control software.

Two communications modules are available for the line. Model GMS6511, the communication interface adapter, features up to four channels of ACIA and TTY: RS-232, -422, -423, and/or TTY; selectable serial echo mode; data set/modem control functions; a wire wrap section for custom clock circuitry; and base address and enable/disable switches. Word length, number of stop bits, parity generation and detection, and interrupt control are programmable. GMS6507, the advanced communication module, available in 1.0 MHz, 1.5 MHz, and 2.0 MHz, includes two synchronous serial interface adapter ports and two advanced data link controller ports. Three-state I/O buffers, a disable switch for each port, and a wirewrap section for custom I/O are provided.

All models have overvoltage and reverse polarity protection, emphasize noise decoupling, and have large fanout capabilities. General specifications apply to all of the modules in the series. Operating temperature is 0 to 50 °C, power requirements are 5 V ±5% and ±12 V, and edge connectors are 86 pins on 0.156″ (0.396-cm) centers. Typical dimensions are 9.75 x 6.00 x 0.60″ (24.76 x 15.24 x 1.52 cm).

Circle 463 on Inquiry Card

S-100 Bus Microcomputer Expands From Single- to Multiuser Environments

Decision I is a multitasking IEEE standard S-100 bus microcomputer that features a UNIX identical operating system that runs CP/M as a subtask. Available from Morrow Designs, 5221 Central Ave, Richmond, CA 94084, the microcomputer will sell for under $5000 in a 4-user configuration.

The UNIX operating system (functionally compatible with Bell Laboratories' UNIX) supports UNIX system calls in a manner that is source compatible with UNIX; UNIX programs compile directly, and UNIX documentation is almost totally applicable. CP/M runs as a task under UNIX and communicates with both CP/M and UNIX standard media for maximum portability.

The CPU features a 4- to 6-MHz Z80, sophisticated memory management hardware, and a floating point processor. Disc support includes dual 800k-byte, 5″ (13-cm) floppy discs mounted in the mainframe; dual 1.2M-byte, 8″ (20-cm) floppy discs; and a 26M-byte Winchester disc.

Memory management hardware includes a memory map that supports up to 16 tasks without swapping. Each task receives complete memory protection and automatic memory allocation. One task can be delegated as the supervisor to handle privileged functions forbidden to ordinary tasks. Such functions will trap to the supervisor for proper handling. A switch array on the CPU board allows turnkey configuration if the full range of supervisor functions is unnecessary.

Circle 464 on Inquiry Card

Memory Management Allows Computer System to Meet Multiuser Requirements

A flexible memory management technique supplies the DSC-4 computer system with capability to allocate up to 512k bytes of RAM. Available from Digital Microsystems, Inc, 4448 Piedmont Ave, Oakland, CA 94611, the system can handle multiuser applications with maximum efficiency at minimum cost. The system consists of a Multibus based Z80A processor; one or more 128k RAMs; four RS-232 serial ports; two 8-bit parallel ports; and two single-sided, double-density floppy disc drives. Options allow up to 28M bytes of disc storage capacity.

Features include error detecting LSI components, onboard ROM diagnostics, HiNet network connection capability, realtime clock I/O and clock interrupts, and a floppy disc controller that provides for either IBM 3740 single-density or System/34 double-density operation and uses standard CRC-16 error detection. Extra card slots allow for the addition of user specified Multibus compatible boards.

Software available includes CP/M, MP/M, and single or multiuser Oasis. Additional applications, using high level languages such as BASIC, PL/1, FORTRAN, COBOL, or Pascal may be developed.

Circle 465 on Inquiry Card

The Invisible Modem is Here!

Dear Ma:

Racal-Vadic introduces the Amazing Modemphone— World's first voice-data telephone with a built-in Bell 103/113 compatible 300 bps full duplex modem.

An invisible modem?

That's right. It's packaged INSIDE a standard rotary or tone telephone.

Now, all you need is the Modemphone and your terminal. Use it for regular voice communication, or, with a flip of a switch, transmit and receive data at rates up to 300 bps full duplex.

Bell 103/113 compatible, the Modemphone is FCC registered for direct-connect to the switched network. You can choose either manual or automatic Originate/Answer.

Racal-Vadic engineers have done a remarkable job of packaging a COMPLETE MODEM inside a conventional telephone. All standard modem circuitry is mounted on a 17.5 square inch PC board, while a 6 square inch board adds the automatic Originate/Answer option.

The Modemphone is amazingly simple to install and to operate, with instructions on a pullout plastic card.

No doubt about it — the world's first voice-data telephone is the shape of things to come, eliminating the need for a separate modem and associated wiring. At $250, the price is right, too.

For fast info call the 800 number right now.

Your independent thinking son,

Alexander Graham Jr.

Racal-Vadic Member IDCMA

222 Caspian Drive
Sunnyvale, CA 94086
Tel: (408) 744-0810 • TWX: 910-339-9297

RACAL *The Electronics Group*

PHONE: (800) 543-3000, OPERATOR 390

Racal-Vadic Regional Offices: West: (408) 744-0810 • **East:** (301) 459-7430
Central: (312) 932-9268 • **Northeast:** (617) 245-8790 • **Southwest:** (817) 277-2246

Available from these stocking reps...

Alabama: (800) 327-6600 • **Alaska:** (907) 344-1141 • **Arizona:** (602) 947-7841 • **California:** S.F. (408) 727-6491, L.A. (714) 635-7600, S.D. (714) 578-5760 • **Colorado:** (303) 779-3600 **Connecticut:** (203) 265-0215 • **District of Columbia:** (301) 622-3535 • **Florida:** Fort Lauderdale (800) 432-4480, Orlando (305) 423-7615, St. Petersburg (800) 432-4480 • **Georgia:** (800) 327-6600 • **Illinois:** (312) 255-4820 • **Indiana:** (317) 846-2591 • **Kansas:** (913) 362-2366 • **Maryland:** (301) 649-6000 • **Massachusetts:** (617) 245-8900 • **Michigan:** (313) 973-1133 • **Minnesota:** (612) 944-3515 • **Mississippi:** (800) 432-4480 • **Missouri:** (314) 821-3742 • **Nevada:** (800) 422-4591 • **New Jersey:** North (201) 445-5210, South (609) 779-0200 • **New Mexico:** (505) 299-7658 • **New York:** Binghamton (607) 785-9947, N.Y.C. (212) 695-4269, Rochester (716) 473-5720, Syracuse (315) 437-6666 • **North Carolina:** (800) 327-6600 • **Ohio:** Cleveland (216) 333-8375, Dayton (513) 859-3040 • **Oregon:** (503) 224-3145 • **Pennsylvania:** East (609) 779-0200, West (313) 973-1133 • **South Carolina:** (800) 327-6600 • **Tennessee:** (615) 269-3726 • **Texas:** Austin (512) 451-0217, Dallas (214) 231-2573, Houston (713) 688-9971 • **Utah:** (801) 484-4496 • **Virginia:** (301) 649-6000 **Washington:** (206) 364-8830 • **Wisconsin:** (414) 547-6637 • **Canada:** Calgary (403) 243-2202, Montreal (514) 849-9491, Toronto (416) 675-7500, Vancouver (604) 681-8136

CIRCLE 86 ON INQUIRY CARD

Magnetic Tape System Is Multibus Compatible

INTL-1050, an IBM/ANSI compatible magnetic tape system that is plug compatible with the Intel Multibus, consists of a single-card tape controller that connects to the model 1050 formatted tape transport. The card tape controller manages data transfers between the host CPU and the drive via direct memory access into an 8k onboard buffer.

The complete subsystem, available from Innovative Data Technology, 4060 Morena Blvd, San Diego, CA 92117, uses a dual-density, 9-track, 45-in (114-cm)/s tape transport for either 800 bit/in (314/cm) NRZI, or 1600 bit/in (628/cm), Phase Encode. Error recovery, interrupts, and status and diagnostic primitives are provided in 4k onboard EPROM. The Multibus, isolated from the subsystem, allows tape data transfer without requiring main bus cycles.

A system controller fits Multibus card cages and stores over 40M bytes of data on a full size 2400′ (731-m), 10.5″ (26.6-cm) diameter tape reel. Features include drive embedded formatter, IBM compatible 7- or 9-track, read after write, VRC and LRC checks, software controlled single- or dual-data buffering, multiple drive systems, and high speed data transfer. The system measures 24 x 19 x 15″ (60 x 48 x 38 cm), is fully integrated and tested, and is shipped in any combination of up to eight tape drives.

Circle 466 on Inquiry Card

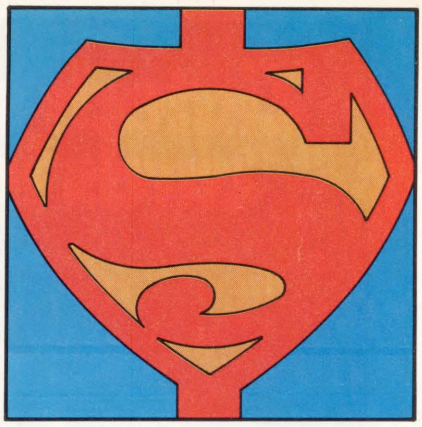
Component Configurations Extend μC Families

Four additional configurations of the LSI-11/23 microcomputer, along with price reductions from 7 to 19% on several standard configurations, are available. Extensions of the family from Digital Equipment Corp, Maynard, MA 01754, include an LSI-11/23 entry level component package consisting of the CPU, 32k bytes of RAM, two serial lines, clock and provisions for 8k bytes of ROM or EPROM.

Several price reduced (6 to 21%) configurations and an additional configuration are available for the LSI-11/2. This configuration includes the CPU, 64k bytes of RAM, four serial lines, clock, ROM/EPROM provisions, and software license for the RRT runtime system. Other memory sizes and some multifunction boards are available.

Circle 467 on Inquiry Card

VISACOM/23 GRAPHIC/IMAGE SYSTEM. SUPER CAPABILITIES, SUPER FAST, SUPER PRICE.



DeAnza's VISACOM/23 now offers you features and capabilities previously only found in large-scale systems. Features like proven and superior image and graphic display software, advanced computing capabilities and proven operating systems software.

All at a very reasonable price.

The VISACOM/23 and the DeAnza Library of Image Processing Software (LIPS) allows you to perform work you only thought possible on the large, expensive systems.

Graphic and display efforts like convolutions, rotations, classification, amplifications, addition, subtraction, image and graphic zoom and scroll as well as much more.

And, the VISACOM/23 incorporates the powerful LSI-11/23 computer so you perform graphic and image processing more easily and much faster.

It allows you to do more work in less time.

VISACOM/23 has a full 512K byte memory for dedicated computer operation or image display as well as 128K bytes of dedicated memory outside of the image memory, four independent graphic overlay channels, alphanumeric character generators, color and monochrome transformation units and cursor overlays.

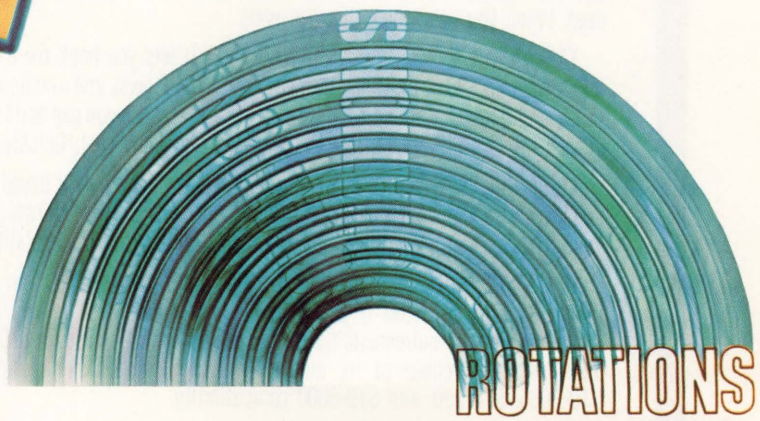
If your graphic and imaging application calls for a system that provides quality, flexibility and added capabilities all in an economical package, find out more about the VISACOM/23 today.

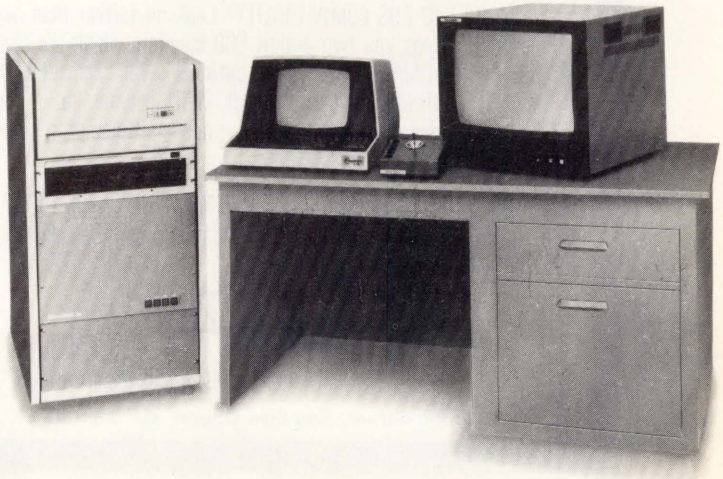
Call or write:

DeAnza Systems Incorporated

CORPORATE HEADQUARTERS: 118 Charcot Avenue, San Jose, CA 95131, (408) 263-7155, TWX: (910) 338-7656
REGIONAL OFFICES: 100 First Ave., N.E., Suite 114G, Cedar Rapids, IA 52401, (319) 364-1366 • 3918 Prosperity Ave., Suite 204, Fairfax, VA 22031, (703) 698-0600.

GIVE YOURSELF A BETTER IMAGE





CIRCLE 87 ON INQUIRY CARD

MICRO DATA STACK

Memory and I/O Boards Increase Program Storage and Serial Data Rate

Combination memory and I/O expansion boards, iSBC 108A™ and 116A™, provide users of the company's single-board computer with up to four times the program storage capacity and twice the maximum serial data rate of the original iSBC 108™ and iSBC 116™ boards. Available from Intel Corp, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123, the boards allow expanded data memory, program storage memory, serial I/O, and parallel I/O. The 108A and 116A contain 8k and 16k bytes of RAM, respectively, 48 programmable I/O lines, a programmable serial I/O port with RS-232-C drivers and receivers, eight interrupt lines, and a 1-ms interval timer.

Both boards are compatible with Multibus™ and interface iSBC 80™ or iSBC 86™ single-board computers. 20-bit memory address decoding gives compatiblity with the 1M-byte memory address space of iSBC 86 computers. 12-bit I/O address decoding is also provided. EPROM power requirements have been reduced by up to 70%.

An 8251A universal synchronous/asynchronous receiver/transmitter, USART, is provided, allowing most byte oriented communications protocols to be programmed with commands in the applications software of the system. Eight jumper selectable interrupts are available: two each on the USART and two programmable peripheral devices, and two for user designated devices, one of which can be jumpered to the interval timer to provide interrupts at 1-ms intervals.

In both synchronous and asynchronous modes, the serial I/O port features half- or full-duplex, and double-buffered transmission and reception. Circuits are provided to check parity, overrun, and framing errors. The port uses either an onboard baud rate generator, or external clock signals; in the asynchronous mode, jumper selectable baud rates range from 75 to 19,200.

Forty-eight parallel I/O lines are implemented with two 8255A programmable peripheral devices, providing a total of six 8-bit ports that can be configured with system software into bi- and unidirectional combinations. Two ports can be used as status or I/O registers. Sockets allow installation of line drivers and terminators to suit specific applications.

Circle 468 on Inquiry Card

Just think what you can do with that speed. At 240 lpm, 80 characters per line, you can copy a full 24 line CRT screen in 6 seconds... or deliver a memo by phone at 1200 baud.

No problem. Because the TH 240's clean design and unique thermal dot matrix printhead deliver that speed reliably and without a sound. With thousands installed and field proven, you can buy with confidence. What's more, the TH 240 has self test diagnostics and three easily replaceable subassemblies for the ultimate in serviceability... and you get the support of 40 service centers nationwide. You don't need to maintain a TH 240 inventory... we do it. Call or write for details today.

PRINTERS THAT PERFORM... WITH YOUR SYSTEM.

*To Qualified OEMs

PRINTER SYSTEMS CORPORATION
1 West Deer Park Road, Suite 104
Gaithersburg, MD 20760
(301) 840-1070 (800) 638-4041

CIRCLE 89 ON INQUIRY CARD

Support System Emulates CMOS MPU in Real Time

MEX146805, this company's first CMOS hardware and software support system, adapts EXORciser™ and EXORterm™ equipment to the development of systems based on the CMOS MC146805E2 MPU. Available from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix AZ 85036, the support system provides the user with a debugging repertoire and gives realtime emulation of the MPU. Included are two printed circuit board modules, one extender cable terminated by a 40-pin DIP plug, an MDOS diskette containing the MPU macro assembler and linking loader, and FIVEbug™, the MEX6805 debug/monitor program.

The development system uses a CMOS processor on the MPU module, together with an MC6800 or MC6809 MPU in the EXORciser development system. This technique isolates the CMOS processor from the development system, while allowing interprocessor communication. Existing M6800 or M6809 hardware and software is used for the development of MC146805E2-based systems.

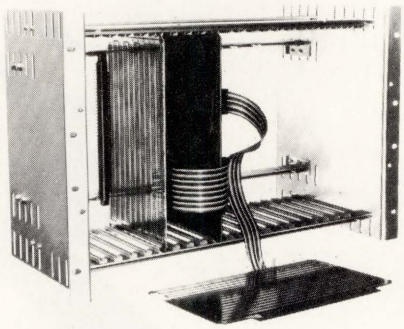
FIVEbug capabilities enhance the debugging function; multiprocessor user systems can be debugged, one processor at a time. The debug/monitor system works with MEX146805 module configuration commands, data manipulating commands, diagnostics for testing onboard RAM, processor control commands, and memory change commands.

The cross macro assembler, featuring macros, conditional assembly, relocation, and linking, and requiring 24k bytes of RAM, allows the assembly of the MPU source code and supports the CMOS MPU. The linking loader combines relocatable object modules to produce an absolute object image.

Operable in standalone mode by forfeiting interrupt-driven debug capabilities, the system allows use of all onboard RAM, EPROM, and external memory, and permits use of the single step and set breakpoint function, or halt-on-address, for programs in onboard RAM. Minimum system requirements for use of the MEX146805 are EXORciser with EXORterm 150, EXORdisk II, and 24k of memory.

Circle 469 on Inquiry Card

Prototyping Boards Have Expanded I/O Capability



4611 series prototyping boards from Vector Electronics have an 8″ uncommitted area for mounting ribbon wire connectors and hold up to 119 16-pin DIPs

A series of prototyping boards for Motorola EXORciser or Rockwell AIM 65 Expansion provides flexibility in interconnection methods and component placement. The boards, available in bare, dual-power bus, and dual-power bus plus 3-hole pad configurations from Vector Electronic Co, Inc, 12460 Gladstone Ave, Sylmar, CA 91342, have a large uncommitted pad area near the top for ribbon wire I/O connectors.

Model 4611-1 is bare except for the edge connector, is used with wrapped wire interconnections, and holds up to 119 16-pin DIPs. Power and ground buses are made with added wire. Model -2 has only interposed power and ground buses, is intended for wrapped wiring, and holds up to 80 16-pin DIPs or a mixture of sizes. Model 4611, with 3-hole pads interspersed with power and ground buses, holds up to 45 16-pin DIPs, or a lesser number of larger devices, and is designed for soldered interconnections or solder mounting of wrap post IC sockets and discrete components. All three boards have an 8″ (20-cm) long uncommitted area for mounting ribbon wire connectors with two rows of leads of LEDs on a 0.1″ (0.2-cm) grid. All boards have the standard EXORciser 48/36 contact card edge connector.

Circle 470 on Inquiry Card

Small Business Computer Combines Hard/Floppy Discs With Magnetic Tape Backup

Combining hard and flexible disc storage with a magnetic tape backup unit and providing storage for large amounts of data with economical tape backup, the ACS8000-6-MTU small business computer is available from Altos Computer Systems, 2360 Bering Dr, San Jose, CA 95131. The microcomputer system supports one to four users simultaneously, and uses a Z80A CPU, 8″ (20-cm) floppy and 14″ (35-cm) Winchester disc drives, and a 0.25″ (0.65-cm) "funnel" cartridge tape drive.

The single-board computer offers greater throughput, enhanced reliability, ease of repair, and socketed expansion areas. Single- and double-sided floppy discs provide either 1 or 2M bytes of online storage, and Winchester discs provide unformatted storage options of 14.5M, 29M, or 58M bytes. The MTU includes a 450′ (135-m) cartridge with over 17M bytes of storage capacity. Reading and writing are unidirectional on four tracks, at 30 in (76 cm)/s. The drive will search at 90 in (228 cm)/s, and packing density is 6400 bits/in (2517/cm).

Features of the system include tape initialization, verifying the cartridge by writing and reading a check code on each of the four tracks; disc to tape backup, placing user specified files onto the tape; tape to disc restore, placing user specified files from tape to a specified disc drive; disc to tape append, allowing the addition of new files into a partially used tape cartridge; and a tape directory, listing the names of all data files on a cartridge.

Data reliability is less than one error in 100M bits read by the device. Automated error recognition and correction ensure continued data integrity.

Circle 471 on Inquiry Card

Single-Board Controller Improves Microcomputer Printing Speed

Designated LPC-03, a single-board printer and controller provides serial printing capability of 180 char/s or 340 char/s, and line printing at 300 lines/min to users of DEC LSI-11, LSI-11/2, LSI-11/23, and PDP-11/03 microcomputers. The controller, available from BDS Computer Corp, 1120 Crane St, Menlo Park, CA 94025, is plug compatible with the UNIBUS and software transparent to the

(continued on page 170)

"Our new VISUAL 400 tops the industry's finest line of video terminals."

"Compare Visual's line of terminals with any other in the industry. Character or block mode. 80 or 132 columns. Black and white or green and black screens. Double high and double wide characters. Super editing. Limited graphics. Paging. International character sets. Programmable function keys. We emulate and outperform terminals from DEC®, Hazeltine, Lear Siegler and ADDS. Chances are we've got the right terminal at the right price for you. Call our marketing department and see for yourself."

Tom Foley, President

VISUAL 100 –

DEC VT100® Compatible Plus

- Advanced video package is standard
- Non-glare, tiltable screen
- Detached solid state keyboard, n-key rollover
- CRT saver feature
- Serial buffered printer interface option
- Hewlett-Packard protocol compatibility option

VISUAL 200 – Switchable Emulations

- Switch selectable emulation of DEC VT52®, Hazeltine 1500, ADDS 580, LSI ADM-3A
- Non-glare tiltable screen
- Detached solid state keyboard
- Large 7 x 9 dot matrix characters with descenders for lower case
- Background/foreground, blink, security fields, editing
- EIA-RS232-C and 20 ma interfaces, serial printer port, smooth scroll, 14 function keys
- Numeric keypad and cursor positioning keys

VISUAL 210 – Block Mode

- All the features of VISUAL 200 plus...
- 14 user programmable function keys, up to 48 codes each may be down line loaded
- Transmit line, field, page
- User programmable message framing including start of message, end of line, field separator and end of message codes
- Remote transmit
- Suspend/resume transmit
- Transmit unprotect/all

VISUAL 400 – Top Of The Line

- All the advanced video capabilities of the VISUAL 100, i.e., 80 or 132 columns, etc., plus...
- Flexible block mode transmission parameters
- Multiple field definitions including numeric only, alpha only, must fill, total fill, right justify, protect
- 8 resident national character sets & line drawing
- Programmable non-volatile function keys
- Control code display
- Printer port independent of communication interface
- 2 or 4 optional pages of memory; flip page or scroll
- Set-up modes for selection of terminal parameters, eliminating cumbersome switches

VISUAL See for yourself

Visual Technology Incorporated

Railroad Avenue, Dundee Park, Andover, MA 01810
Telephone (617) 475-8056 Telex 951-539

CIRCLE 90 ON INQUIRY CARD

MICRO DATA STACK

operating system, requiring no reprogramming or reconfiguring. The controller measures 5 x 8.5 x 0.5″ (13 x 21.6 x 1.2 cm) and occupies one quad-size slot in the chassis. Required power is 5 Vdc at 0.8 A.

Both the 340- and the 180-char/s printers are a 7 x 7 dot matrix with 64/96-char sets. The serial printers measure 8 x 26 x 23″ (20 x 66 x 58 cm) and weigh 70 lb (38 kg). The 300-line/min printers have 64 uppercase character sets with 96 upper/lower case character sets as options. The line printers measure 15 x 30 x 25″ (38 x 76 x 63 cm) and weigh 150 lb (68 kg).

Circle 472 on Inquiry Card

S-100 Bus Computer Designed for ROM Based Programs

The basic System Zero (model CS0) computer from Cromemco Inc, 280 Bernardo Ave, Mountain View, CA 94043, can be expanded by adding more memory and I/O cards to take advantage of floppy and/or hard disc systems. The S-100 bus computer system includes a Z80A-based single card computer, 1k byte of RAM memory, and 3k control BASIC in ROM memory. Three additional slots on the bus are available to tailor the system to specific applications.

Model CS0/D, a special version, is available for use with floppy discs, and includes the Z80A single card computer, 64k of fast RAM, and the 16FDC disc controller card that permits the use of high capacity disc drives storing 390k bytes on 5″ (12-cm) diskettes. The controller has an onboard resident disc operating system, RDOS-2, that provides system diagnostics, as well as the ability to read or write single-sided, double-sided, single-density, or double-density diskettes.

Circle 473 on Inquiry Card

Memory Management/Mapping Make Single-Board Computer Useful in Multitasking

Am95/4010, an 8-bit, Multibus compatible, single-board computer from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086, features memory management capabilities and an Am8085A-2 CPU with 4-MHz operation. Memory management and mapping capabilities adapt the unit to use in multi-user/multitasking designs.

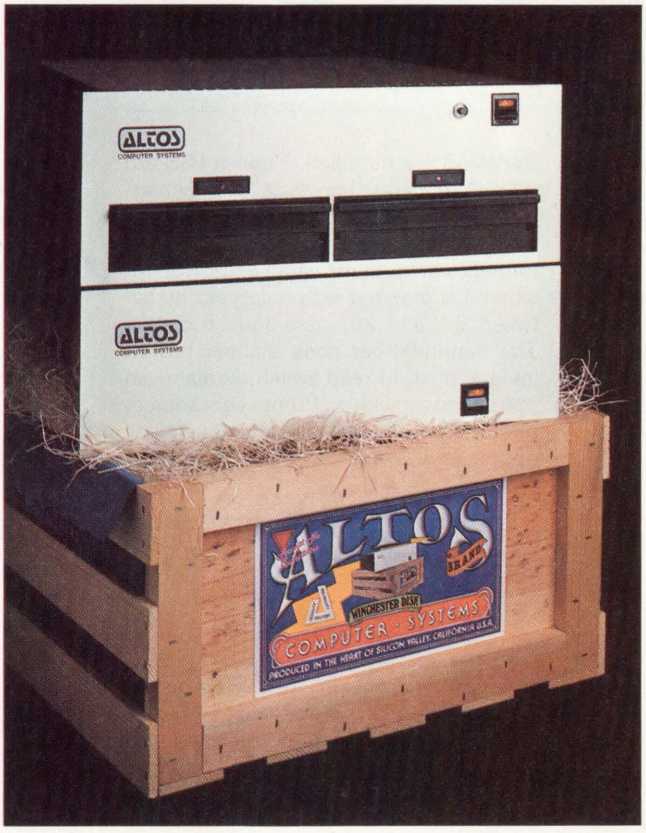
The memory management unit uses a programmable onboard mapping RAM, enabling the user to address 256k bytes anywhere in a 1M-byte address space; these 1M bytes can be divided into as many as 256 1k-byte segments with each segment independently placed anywhere in the address space. Each segment can be independently read or write protected. The user can select any RAM board that is Multibus compatible. Standard memory boards can be mixed in any combination up to 256k bytes of memory.

Four independent groupings and common blocks of memory within the memory map are allowed for multi-user/multitasking designs. Each user and the system have separate address space; only the system is allowed to execute I/O operations and similar privileged instructions. The system can trace resource availability, prevent contention, and determine priority of access.

Standard features include two RS-232-C serial ports, 24 parallel I/O lines, up to 4k bytes of P/ROM, 8-channel vectored interrupt controller, and the Am9513 with five independent 16-bit counters and multimode operation.

Circle 474 on Inquiry Card

WHY OUR WINCHESTER HARD DISK BASED SYSTEMS ARE PICKED BY GROWING CONCERNS



Growing seasons. Those fruitful times when firms often find that their applications have outgrown their systems. Yet the costs of stepping up to a minicomputer can cause growing pains for many growing concerns.

Altos Computer Systems, a world leader in single board microcomputer technology, has packages of fresh ideas designed specifically for growing OEM's, the business sector, and many other end users. In fact, they're responsible for Altos' own rapid growth in the last three years.

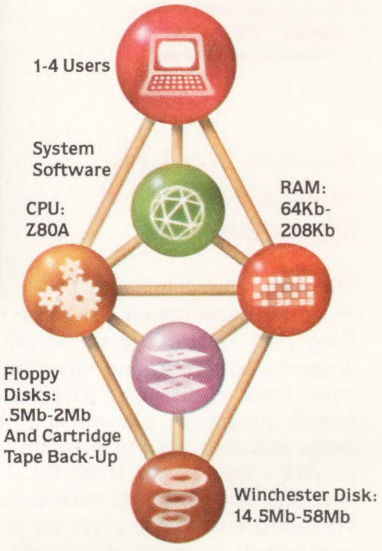
Packages like Altos' ACS8000-6 microcomputer family that's loaded with features which provide minicomputer performance at affordable microcomputer prices. The advanced, proprietary double-sized single board contains fully socketed and reliable LSI circuitry that includes: the Z80A* CPU with high speed DMA; up to 208 KBytes of RAM; the sophisticated floppy disk and Winchester hard disk controller; six RS-232C serial and two 8-bit parallel ports; and an optional floating point processor.

The Altos hard disk family will support up to four users simultaneously with 48 KBytes of RAM each, as well as up to 58 MBytes of on-line quality Shugart Winchester hard disk storage, with tape cartridge back-up. And all this at microcomputer prices.

Altos also supports three industry standard operating systems: single/multi-user CP/M,** OASIS,† and Altos' proprietary AMEX.™ Seven high level programming languages are offered which are CP/M or AMEX compatible.

Weed through the microcomputer system alternatives. No matter what your application, you'll pick Altos.

For specific details about pricing or performance, call or write: Altos Computer Systems, 2360 Bering Drive, San Jose, CA, 95131, (408) 946-6700, Telex 171562 ALTOS SNJ.



Packed with Fresh Ideas

ALTOS
COMPUTER SYSTEMS

*Z80A is a registered trademark of Zilog, Inc. **CP/M is a registered trademark of Digital Research, Inc. †OASIS is a registered trademark of Phase One Systems, Inc.

CIRCLE 92 ON INQUIRY CARD

MICRO DATA STACK

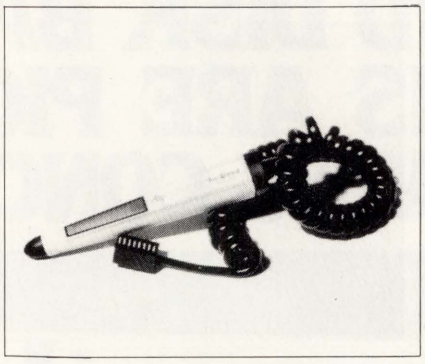
CPU Board Compatible With 8-Bit Memory and I/O Subsystems

CP88, a CPU board for S-100 machines based on the Intel 8088 microprocessor, is compatible with commonly used 8-bit memory and I/O subsystems. The board, available from Microfuture, PO Box 5951, San Jose, CA 95150, features 1M bytes of memory address space, with flexible EPROM/RAM addressing in the top 4k of address space. Provision is made for up to 3k bytes of onboard EPROM and 1k bytes of static RAM. Memory access time requirements are 450 ns using the standard 5-MHz 8088 CPU.

Full 16-bit math and extensive string handling capabilities are included in the instruction set. All S-100 edge connector pins are plated; 97 pins are brought to onboard feedthrough. Two 16-pin, three 18-pin, and one 40-pin spare sockets are provided for breadboarding.

Circle 475 on Inquiry Card

Bar Code Wand Plugs into Apple II or III Computer



BarWand, a modified Hewlett-Packard HEDS 3000 digital bar code wand, interfaces to the Apple computer line and is designed to read all common bar code formats with nominal width of 1′ (0.3 m) when it is scanned with a tip velocity between 2.9 and 29″ (7.6 and 76 cm)/s. The handheld bar code scanner has an integral push to read switch, contains an optical sensor with a 700-nm light source, photodetector, and precision aspheric optics, and is available from Advanced Business Technology, Inc, 12333 Saratoga-Sunnyvale Rd, Saratoga, CA 95070.

The wand must be held with a tilt angle between 0 and 30° with the tip in contact with the tag. Surface of the switch button must be parallel to the height dimension of the bar code. A digitizing circuit in the wand provides a TTL compatible logic high when positioned over a nonreflecting black bar and a logic low over a reflecting white space. The push to read switch energizes the 700-nm LED emitter and electronic circuitry.

Features include a replaceable, low friction scanning tip, a 7′ (2.13-m) stretch cable, and a lightweight case. Supply voltage is 3.6 to 5.75 Vdc; supply current is 50 mA. Output power is 200 mW, and switch bounce is 5 ms. The wand weighs 1.5 oz (42 g), and is 5.2″ (13.2 cm) long and 0.75″ (1.90 cm) in diameter. Assembly code subroutines are provided on 5.25″ (13.33-cm) disc media to read most common bar codes including Paperbyte, Label Code, and typical UPC codes, and are arranged in a series of application demonstrations written in Applesoft.

Circle 476 on Inquiry Card

SOFTWARE

Software Standards Established for 16-Bit Microprocessors

Standard conventions that will enable programs written in any language for the Zilog Z8000 microprocessor to call Z8000 programs written in any other language have been established. The standards specify parameter passing and register usage practices used in software written by Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014, for its microprocessor. They also enable compilers for all Z8000 languages to generate object code.

The proposed standardized calling conventions have been adopted by Microsoft and are under consideration by several other companies. They satisfy the requirements of the major programming languages, including C, PLZ/SYS, FORTRAN, and Pascal. In addition, they minimize call-return overhead, allow for passing of structured parameters by value, and add little complexity to code generators. No undue call-return overhead is introduced in code generated by one language processor at the expense of another.

Two register subsets—temporary and global—are partitioned from the microprocessor's register set. Temporary registers are not preserved by called routines, while global registers are preserved across subroutine calls; ie, they contain the same values on the return from a subroutine call that they contained on entering the subroutine.

Every member of a parameter list is assigned by an algorithm either to a register or to storage. The algorithm handles value, result, and reference parameters for both segmented and nonsegmented versions of the microprocessor.

In a related activity, the U.S. Air Force has been licensed to use the microprocessor's instruction set in defense related computer systems. According to the agreement, the Armament Division of the Air Force Systems Command may use the Z8000 instruction set in 16-bit computer based defense embedded systems, including applications in weapons, communications, command and control, and military intelligence. Such systems will be developed either by the Armament Division or its contractors. However, as part of the nonexclusive agreement, the licensee may not modify the instruction set.

Circle 477 on Inquiry Card

Industrial Version of Pascal Supports M68000 and Z8000 CPUs

Intended for OEM industrial applications, HA-Pascal/I supports all functions of PL/M compilers but has a Pascal syntax. Features include port I/O support, 32-bit arithmetic, access to memory on a byte or word basis, assembler routines callable for time critical applications, entire set of Pascal control structures, complete set of useful external functions, interrupt or realtime operations, debugging with the machine monitor, ROMable object code, high efficiency code production, and support of a separate compilation.

Hemenway Associates, Inc, 101 Tremont St, Boston, MA 02108, states that the compiler produces native code and runs under either HA-SP/68000 or HA-SP/Z8000 operating systems although the code it produces can run standalone. Operation of the compiler is edit a source Pascal program, compile the source producing macro calls, assemble the macro calls together with the supplied macro library to produce relocatable object code, and link and relocate the relocatable object code producing native machine code. □ Circle 478 on Inquiry Card

Dialight sells only used rockers and toggles.

That's because all are 100% tested. At Dialight we don't use hit-or-miss sampling to test our miniature rockers and toggles. All are 100% tested electrically and mechanically before you get them. And all are made in the U.S.A.

You can choose from thousands of different designs. Our rocker and toggle line contains countless combinations of standard colors, sizes, mountings and contact ratings. Included are dozens of front-panel and sub-panel types, plus many styles for snap-in and printed circuit board applications.

If our catalog doesn't show exactly the switch you need, we'll design and build it to order.

Next time specify only used switches—100% tested rockers and toggles from Dialight, 203 Harrison Place, Brooklyn, N.Y. 11237 (212) 497-7600.

DIALIGHT
meets your needs.
A North American Philips Company

CIRCLE 93 ON INQUIRY CARD

Memory Error Control Management

John R. Mick
Advanced Micro Devices
901 Thompson Pl, Sunnyvale, CA 94086

As the size and density of dynamic random access memories increase, so will hardware bit failures due to alpha particle impingement. Design engineers must therefore be increasingly concerned with soft errors in memory designs that include large, dense random access memories. To improve reliability it is essential that such memory systems be supported by error detection and correction. It has been estimated that system reliability can be increased by a factor of 60 or more if suitable error detection and correction methods are employed.

Memory Support Devices

The advantage of using large and very large scale integration (LSI and VLSI) random access memories (RAMs) is diminished by the need to surround them with small and medium scale integration (SSI and MSI) devices that constitute error detection and correction (EDC) circuitry and circuitry required for memory buffers, drivers, and controllers. Semiconductor manufacturers are therefore introducing LSI memory support devices that allow the designer to implement error detection and correction and to control memory in a more cost-effective fashion. In addition, EDC and lower part counts can slash field maintenance costs and allow systems to run longer, uninterrupted from soft or hard memory errors, ie, memory errors can be logged for use in detecting marginal RAM chips.

Typical of these memory support devices is the AmZ8000 family including the AmZ8160 error detection and correction unit, the AmZ8161/AmZ8162 EDC bus buffers, the AmZ8163 refresh and EDC controller, the AmZ8164 dynamic memory controller, and the AmZ8165/AmZ8166 dynamic RAM drivers. Fig 1 shows a typical microcomputer memory system in which the memory support subsystem interfaces to the central processing unit (CPU) data bus, address bus, and control signals.

Dynamic Memory Controllers

Dynamic memory controllers (DMC) are not the same as memory management units (MMU). MMUs are intelligent devices that can translate logical addresses into physical address spaces, remember memory space attributes and act accordingly to prohibit access, and allow read only access or limited access based on some code. DMCs, on the other hand, simply accept a physical address and present it in the proper sequence to the memory subsystem. For example, the AmZ8164 can accept a 16-bit address and present it to memory as two sequential 8-bit bytes with an externally specified delay between them. DMCs must also keep track of refresh count control to avoid the loss of

(continued on page 176)

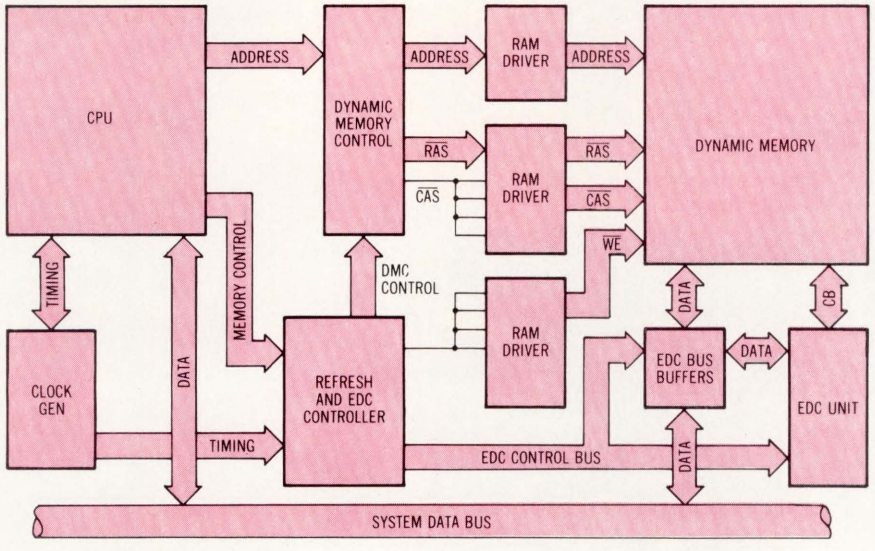
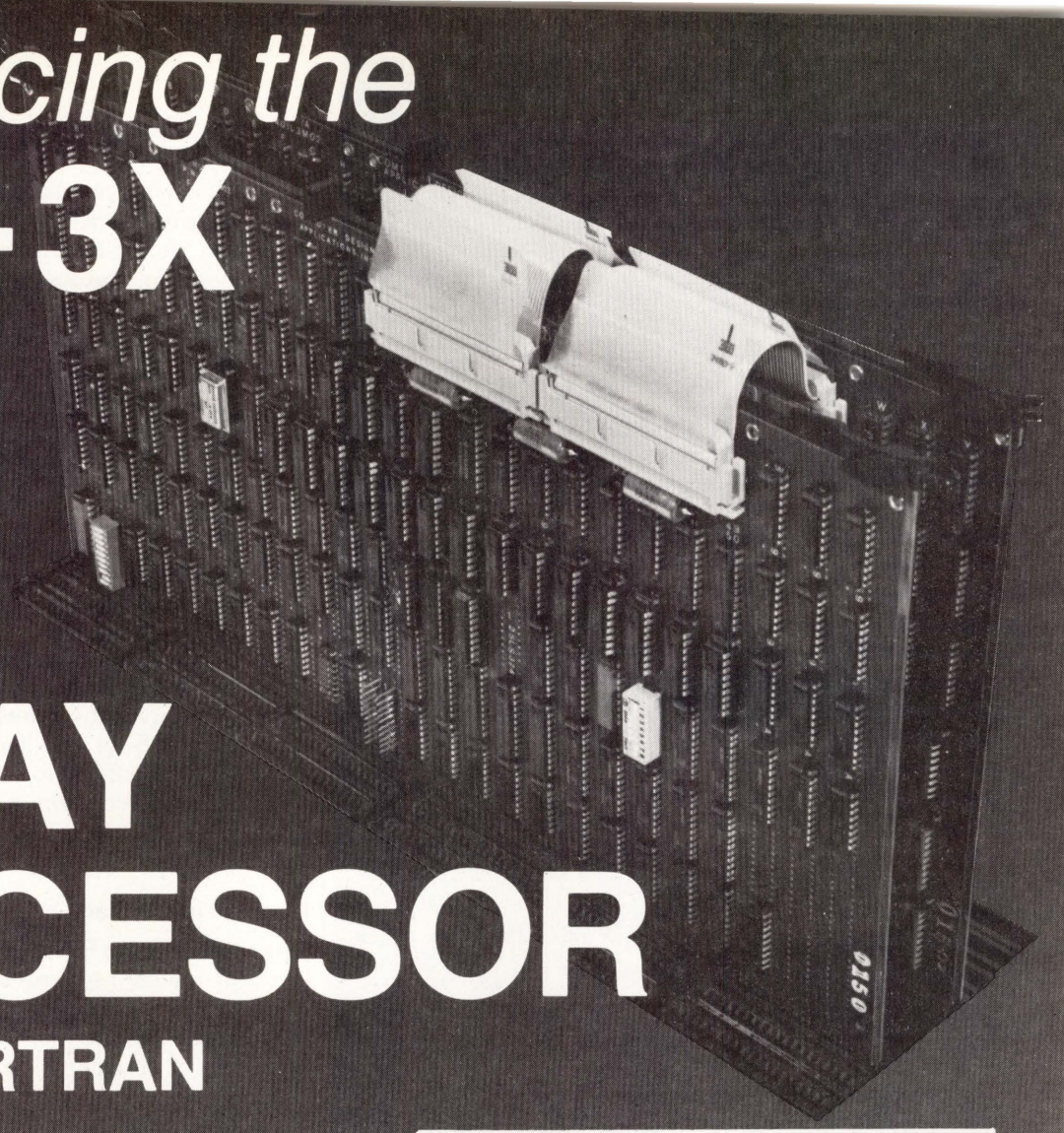


Fig 1 MOS microcomputer memory system. Memory support subsystem interface to AmZ8000 data bus, address bus, and control signals

introducing the

MSP-3X



ARRAY PROCESSOR

PDP-11* FORTRAN
For RT- or RSX

LOW COST

100 TIMES FASTER!

The MSP-3X microsignal processor performs block floating point array processing up to 100 times faster than existing PDP-11* minicomputers. The MSP-3X contains a 4K word buffer memory and an extensive FORTRAN-callable array library that includes FFTs, filters, vector/vector math functions, spectral density and lots more.

MSP-3X FEATURES

- **Convolution (1 or 2 dimensional)**
- **Spectrum Analysis**
- **Random Number generation**
  Also Filtering and Assorted Vector Operations in an Extensive Array Library.

*PDP-11 is a registered trademark of Digital Equipment Corporation.

All These Features for $5000 in Single Quantities

From Computer Design & Applications . . . a recognized leader in multiprocessing. Call or Write today for details on our complete family of analog and digital products and systems.

cda

COMPUTER DESIGN & APPLICATIONS, INC.

377 Elliot Street / Newton, MA 02164 (617) 964-4320

Telex 922521 CDANEW

CIRCLE 94 ON INQUIRY CARD

information in dynamic memories; hence, their programmability should include the selection of refresh modes, and they should be adaptable to different memory sizes.

In addition, the AmZ8164 DMC provides address handling, and row address strobe (RAS) and column address strobe (CAS) decoding and control. It contains 18 input latches for capturing an 18-bit address for memory control and is designed to operate with either 16k or 64k dynamic RAMs. As needed by the memory, the designer uses either 14 of the multiplexer address inputs and 7 of the address outputs or all 16 of the multiplexer address inputs and all 8 of the address outputs. In 16k dynamic RAMs 7 address inputs are provided to the RAM during the RAS LOW signal, and then the 8-bit multiplexer is switched so that 7 upper address bits are provided to the RAM for the CAS LOW cycle. The device provides a 3-bit input address MUX and an 8-bit refresh counter. The 8-bit refresh counter supplies the refresh address to the dynamic memory during the refresh cycle. This counter can be used in a 128- or 256-line refresh mode. The DMC also contains a RAS 2-line to 4-line decoder so that up to four rows of dynamic memories can be controlled from one device and includes a CAS buffer to inhibit the CAS output during refresh.

Using Line Drivers

As can be seen in Fig 1, dynamic RAM drivers can be used in large memory systems to buffer the address, RAS, CAS, and WRITE enable signals to the RAMs. Using standard line drivers such as the Am74S240 and Am74S244 requires the addition of an external series damping resistor between the Schottky output and the RAM to keep the Schottky HIGH to LOW transition from causing a disastrous undershoot and a slower rise time. By locating the resistor in the lower output driver, as in the AmZ8165 and AmZ8166 line drivers, the undershoot problem is eliminated while permitting the fast rise.

The AmZ8165 and AmZ8166 are pin compatible devices with the Am74S240 and Am74S244. The -65 and -66 RAM drivers are specifically designed for driving dynamic RAMs and feature high capacitance drive, guaranteed maximum undershoot of less than -0.5 V, and V_{OH} of less than $V_{CC} - 1.15$ V. Both devices feature symmetrical rise and fall times and have guaranteed minimum and maximum specifications at both 50 pF and 500 pF loads. The -65 is inverting, and the -66 is noninverting.

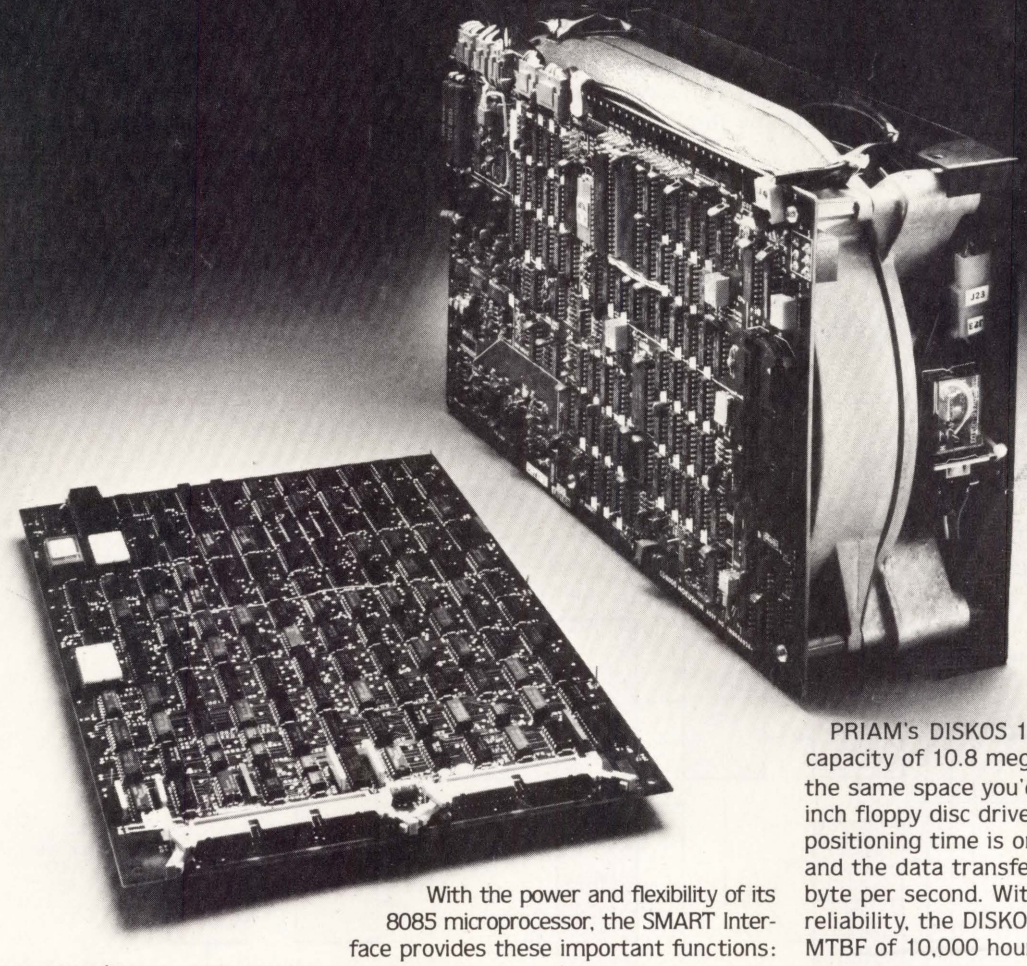
EDC Buffering

Effective use of an EDC chip requires a companion 3-bus buffer with latches. Incoming data must be fed simultaneously to the memory for storage and to the EDC unit for computation of the check bits which are stored with the data in memory. During a read cycle the buffer can operate in either of two modes. In the first mode it can pass data transparently to the data bus and the EDC unit. If the EDC unit does not find a problem with the data, nothing further happens. If the data is incorrect, the EDC must notify the system to stop and wait while the

(continued on page 178)

SMART START

WITH PRIAM'S $1995 WINCHESTER DISC DRIVE/INTERFACE PACKAGE!



Now you can upgrade your system performance easily and inexpensively with PRIAM's SMART START Winchester disc drive package. You get a DISKOS 1070 floppy-disc-size disc drive and PRIAM's SMART Interface. This SMART START combination is priced at only $1995, and its capacity is twice that of other comparable combinations.

PRIAM's SMART Interface adapts quickly and conveniently to most popular microprocessor I/O busses, and it controls up to four eight-inch or 14-inch PRIAM Winchester disc drives having capacities from 10.8 to 158 megabytes. So your systems get the benefit of Winchester technology reliability, low cost-per-megabyte, and a potential for much higher capacities and higher throughput, still using the same SMART Interface.

With the power and flexibility of its 8085 microprocessor, the SMART Interface provides these important functions:

- Serializes and deserializes data with selectable sector sizes of 128, 256, 512, or 1024 bytes.
- Full sector buffering permits data transfers at any rate up to 2 megabytes per second, with programmed I/O or DMA.
- Automatic alternate sector assignment makes disc defects transparent to the host processor.
- Overlapped-command and implied operations capability improves systems throughput in multiple-drive (up to four) systems.

These benefits and many more are packed into a single 8″ × 14″ printed circuit board that can be piggy-backed on the DISKOS 1070, or any other PRIAM disc drive, or mounted separately. PRIAM's optional power supply provides power to both the SMART Interface and the DISKOS 1070 for only $295 more.

PRIAM's DISKOS 1070 gives you a capacity of 10.8 megabytes in exactly the same space you'd give an eight-inch floppy disc drive. Average head positioning time is only 53 milliseconds, and the data transfer rate is 0.9 megabyte per second. With Winchester reliability, the DISKOS 1070 has an MTBF of 10,000 hours.

In addition to the SMART Interface and DISKOS 1070 disc drive, your SMART START package includes a drive interface terminator and an interface manual. PRIAM will also provide application notes for adapting the SMART Interface to commonly used microprocessor I/O busses.

Get Winchester technology off to a SMART START in your system now. Complete SMART Interface and DISKOS 1070 specifications are yours for the asking. This special offer is good only until March 15, 1981, so call or write today to: PRIAM Corporation, 3096 Orchard Drive, San Jose, CA 95134. Telephone (408) 946-4600 TWX 910 338-0293.

PRIAM

CIRCLE 95 ON INQUIRY CARD

data is corrected. In the second mode, read data is latched into the buffer and not released to the data bus until the EDC says to proceed. In either mode, incorrect data is corrected, and the correct data replaces the incorrect data in memory.

Data interface between the dynamic memories, the EDC chip, and the system data bus is accomplished with bus buffers. The AmZ8161 bus buffer is inverting between the system data bus and the EDC bus, while the AmZ8162 is noninverting. Both devices contain two internal latches, a multiplexer, and a RAM driver output buffer. The devices have 4-bit wide data paths to and from the RAM, to the EDC, and to the system data bus.

EDC Unit Operation

The AmZ8160 error detection and correction unit (Fig 2) will generate check bits on a 16-bit data field according to a modified Hamming code and correct the data word when check bits are supplied. Operating on the data read from memory, the device will correct a 1-bit error and will detect all 2- and some 3-bit errors. For 16-bit words, 6 check bits are used. The device is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations the device makes the error syndrome available on separate outputs for data logging. The unit includes two diagnostic modes in which diagnostic data can be forced into portions of the device to simplify device testing and to execute system diagnostic functions.

Sixteen bits of data are loaded into the data input latch from the bidirectional DATA lines under control of the latch enable input. Depending on the control mode, the input data is either used for check bit generation or error detection/correction.

In both EDC modes, the syndrome generation logic block compares the check bits read in from memory against a newly generated set of check bits produced for

(continued on page 180)

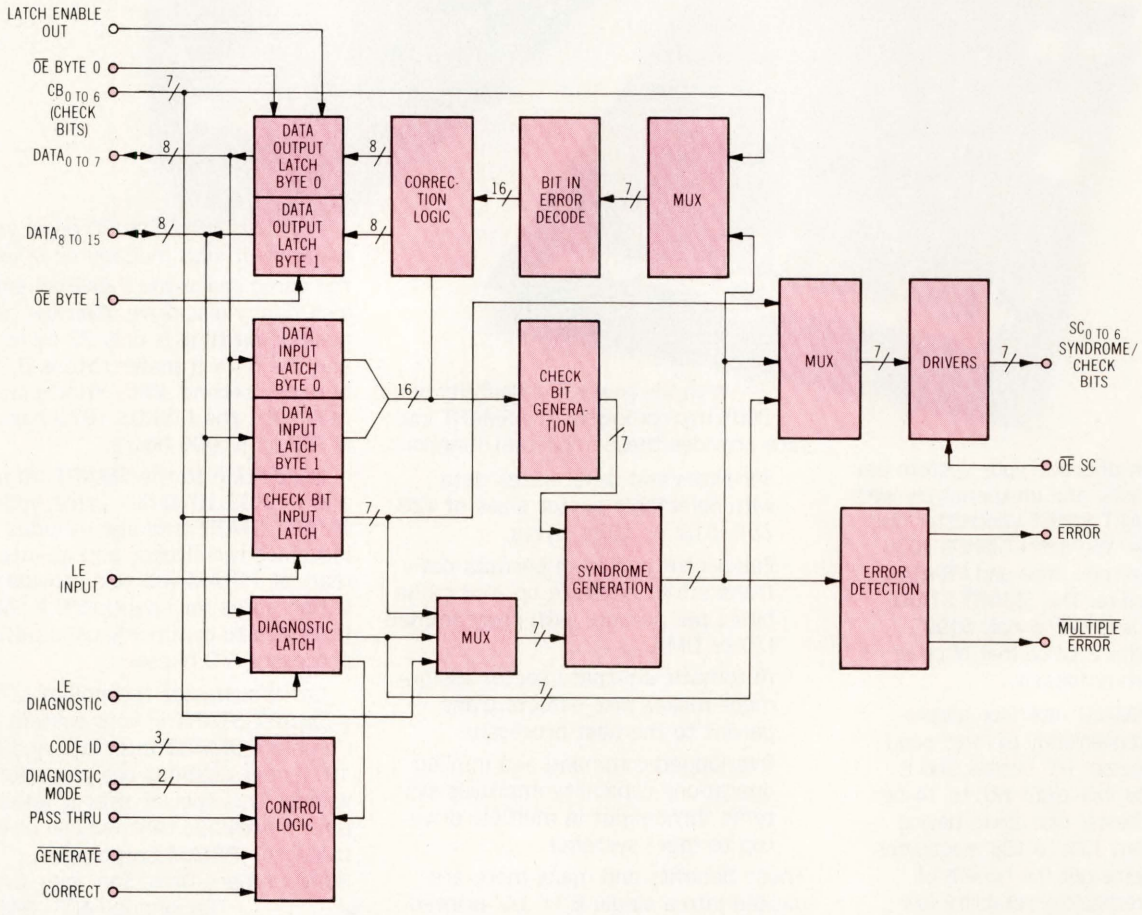
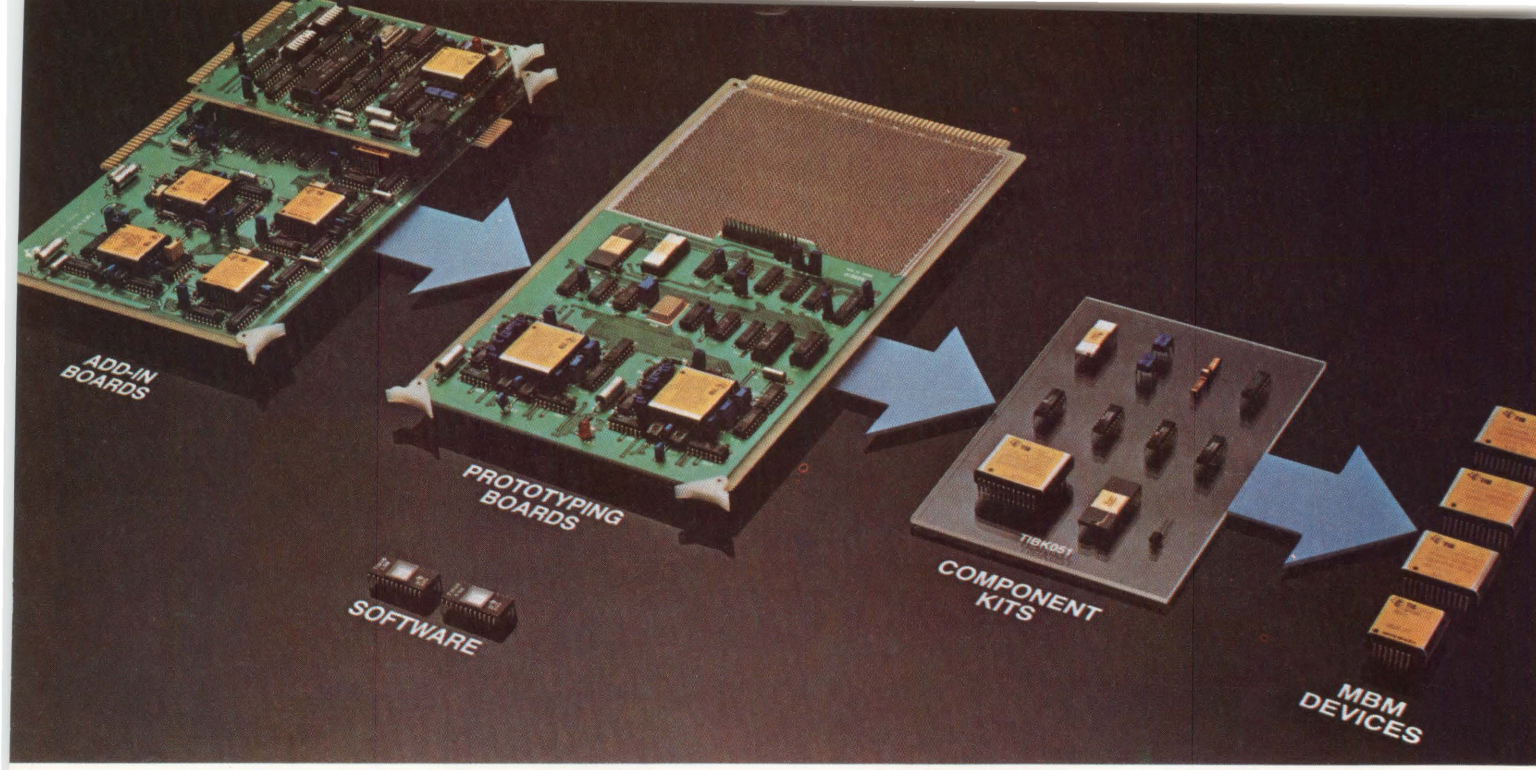


Fig 2 Block diagram of EDC unit. AmZ8160 can be run with no WAIT states when used in 16-bit wide mode shown in Fig 1



More ways to get into bubble memory. And get more out of it. From Texas Instruments.

TI's eight years of experience in bubble memory design and production have provided keen insights into customer design requirements.

So, it makes sense that only TI, the leader in bubble memory technology and products, can offer you more make-or-buy choices for more ways to get into the industry's fastest-growing technology.

It all comes down to a special sensitivity to our customer's needs — no matter what your application, level of sophistication or volume — if you want to get more out of bubble memory technology — talk to Texas Instruments.

Add-in systems

For direct plug-in to most popular microcomputer buses, including TI's TM990 bus. Fully tested, fully assembled systems with capacities ranging from 11K to 1024K bytes. All with associated support circuitry on board.

Prototyping boards

TI supplies the assembled bubble memory and support circuitry — you prototype the interface to your own system — then, when you're ready for volume production, you can build your own boards or have TI build to your specifications.

Kits and components

Design your own non-volatile memory system for your own production. *Less than $100** buys you a 92K bubble memory kit* in unit lots of 1,000, complete with all the support circuitry, including the custom controller. TI's 92K, 256K, 512 K and 1-million bit bubble memory components help optimize cost-effectiveness. Because you buy only as much memory as you need. Only when you need it.

Support, support, support

No matter which route you take. Everything from fully documented user's manuals to development software to a learning-intensive Advanced Technology Seminar at either of our Regional Technology Centers. And, for technical design help, there's our bubble memory applications lab.

Continuing commitment

To innovative, cost/performance effective bubble memory technology. For a full line of standard or custom products. And, for more choices.

For details, send for our newly updated brochure, CL-473A. Contact your nearest Texas Instruments field sales office or authorized distributor. Or write Texas Instruments, Box 225012, M/S 308, Dallas, Texas 75265.

MAGNETIC BUBBLE MEMORY DEVICES, KITS AND PROTOTYPING BOARDS			
CAPACITY (KILOBITS)	**DEVICE**	**KIT**	**PROTOTYPING BOARD**
92	TIB0203	TIBK091	TBB5990
256	TIB0250	TIBK021	TBB5902
512	TIB0500	TIBK051	TBB5905
1024	TIB1000	TIBK101	TBB5910

ADD-IN SYSTEMS		
BUS STRUCTURE	**SYSTEM**	**CAPACITY (KILOBYTES)**
TM990	TM990/210	23 to 69
TM990	TM990/211	128 to 1024
STD	TBB7090/91	11 to 104
OEM (9900,8080, Z80)	TBB5005	64
OEM (9900, 8080, Z80)	TBB5010	128
LSI-11†	MBC11*	46 to 736
MULTIBUS‡	MBB80*	92
S-100	MBB100*	46 to 736

SOFTWARE	
TM990/431	Interactive monitor to test and demo TM990/210
TM990/453	Power Basic with file management for TM990/210

*Available from Bubbl-tec Div. of PCM, Inc., 6800 Sierra Court, Dublin, CA 94566 (415) 829-8705
†Trademark of Digital Equipment Corp.
‡Trademark of Intel Corp.

TEXAS INSTRUMENTS
INCORPORATED

** U.S. prices, subject to change without notice

83744A

CIRCLE 96 ON INQUIRY CARD

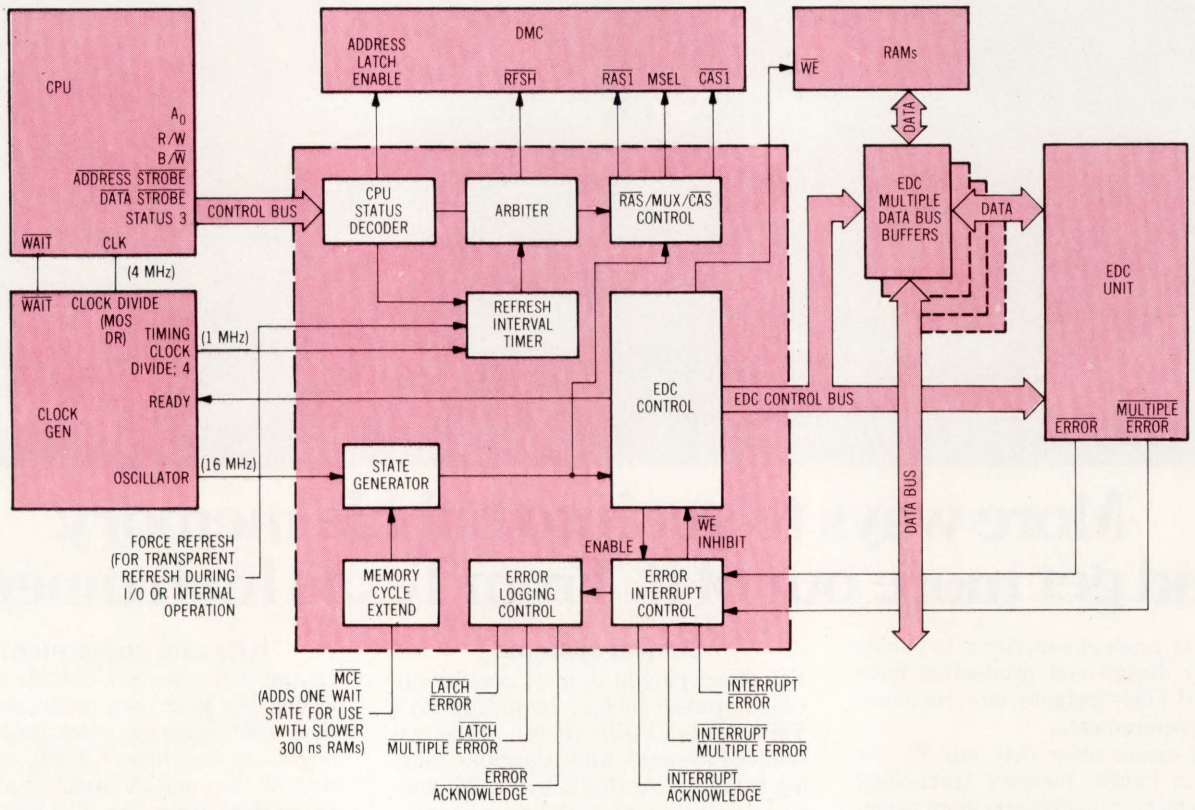


Fig 3 Refresh and EDC controller. AmZ8163 manages control bus interface and provides control signals to memory support devices. Circuitry for error interrupt control and error logging control is included

the data read from memory. If both sets of check bits match, there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

Syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors), the syndrome bits will be all 0s. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit that is in error.

The refresh and EDC controller (Fig 3), in conjunction with the microprocessor, manages the control bus interface and provides control signals to the memory support devices including refresh timing, RAS control, and MUX SELECT and CAS inputs to the DMC. The device also controls the RAM WRITE enable and manages the direction and 3-state enable control of the multiple data bus buffers and the EDC unit. In addition, the device contains circuitry for error interrupt control and error logging control if the user desires these features in the system.

AmZ8163 contains the AmZ8000 CPU status decode that determines if a memory cycle was intended. The internal arbiter monitors the refresh interval timer allowing memory refresh to occur when needed. The device has been designed so that asynchronous clocks can be involved with respect to the control bus and refresh. Thus, the arbiter eliminates metastable flipflop problems associated with asynchronous systems.

Summary

Proper memory control management can improve the mean time to failure of memory systems. By boosting memory reliability, two competitive advantages are obtained. First, the system can run uninterrupted with either single soft errors or with the loss of one memory chip. Second, field maintenance costs can be reduced and service, including replacement of faulty memory components, can be scheduled on a regular basis.

Puzzled over minicomputers?

Systems has all the pieces.

For two decades, SYSTEMS has been at the forefront in the design and manufacture of general purpose minicomputers and minicomputer-based systems. During that time our 32-bit product line and our reputation for excellence in 32-bit technology have grown. SYSTEMS has demonstrated the ability to fully satisfy the demanding requirements of high-technology, real-time scientific, industrial and government applications.

SYSTEMS experience can satisfy your needs too. We have the latest in high-performance processors, friendly software and quality peripheral devices. Our complete family of 32-bit minicomputers and systems provide the performance you need—at the right price. Our years of business experience in supplying minicomputer products, support and service to the OEM enable us to tailor our products, packaging and pricing to meet your requirements. Our commitment to advanced technology is evidenced by one of the largest development budgets in the industry. Continuous introduction of new products and system components assures our customers that SYSTEMS will continue to be one of the most technologically advanced minicomputer suppliers in the world.

SYSTEMS has all the pieces to solve your minicomputer puzzle. Call or write the company with a lifetime of real-time experience, and watch the pieces fall in place for you.

Systems Engineering Laboratories, Inc.,
6901 W. Sunrise Blvd., Fort Lauderdale, FL 33313.
(305) 587-2900, 1-800-327-9716

Argentina•Australia•Belgium•Canada•Colombia•England
France•Italy•Japan•Mexico•Sweden•Thailand•West Germany

SYSTEMS
Proven COMPUTER Performance

Byte Erasable 16k-Bit EEPROM Offers 250-ns Access Time

A 16,384-bit EEPROM that can be erased and reprogrammed on a byte basis operates from a 5-V power supply in the read mode. Writing and erasing, on a chip or byte basis, are accomplished by providing a single 21-V pulse. The 2816, from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95951, with a fast read access speed, is compatible with high performance microprocessors. Using the fast access speed allows zero wait operation in large system configurations. The electrical erase/write capability of the device makes it suitable for applications requiring insystem nonvolatile erase and write.

Memory cells in the EEPROM rely on a mechanism called Fowler-Nordheim tunneling to write and erase data. EPROMs write by attracting electrons to a polysilicon floating gate and erase by dissipating them through exposure to ultraviolet light. The 2816 EEPROM erases as well as writes by electrically causing the electrons to tunnel across a thin layer (less than 200 Å of silicon dioxide. At 125 °C, the device will retain data for at least 20 years. The chip is fully static; refreshing is never required regardless of read frequency. The standard chip has a worst-case access time of 250 ns, while the 2816-3 is rated at 350 ns, maximum, and the 2816-2 has a worst-case readout specification of 200 ns.

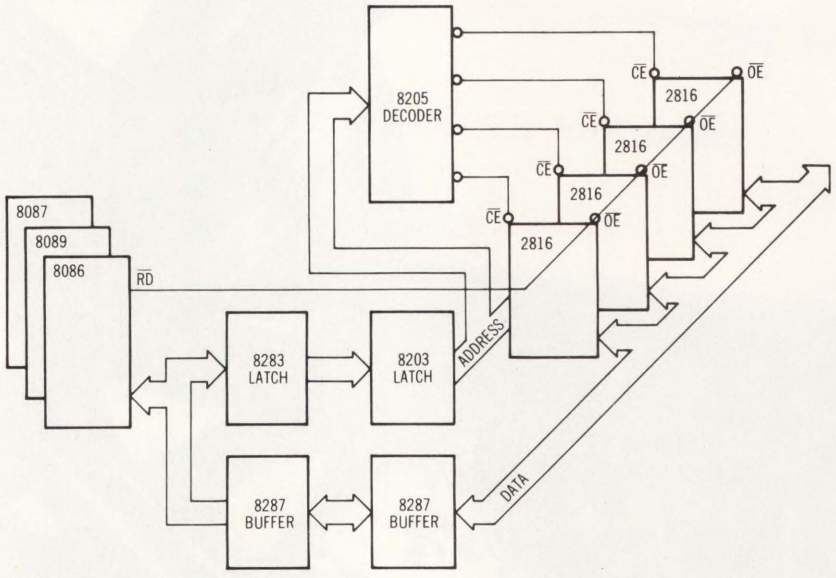
Since the device is byte erasable, a single-byte program change can be accomplished 100 times faster than it can be done on a bulk erase part. Any of the 2k bytes can be erased and rewritten in 20 ms. Rated for operation from 0 to 70 °C, the low power device dissipates 495 mW from the single 5-V supply.

The device also features 2-line control, a system control function that has become essential in large high speed microcomputer systems; 2-line control eliminates contentions between addresses and data on bus lines. The chip has separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) pins that permit the microprocessor to control when it is enabled.

Nonvolatile and fully static, the EEPROM can be reprogrammed electrically in the field, without removal from inservice equipment and also can be reprogrammed remotely, via a radio or telephone link. This flexibility permits design engineers to realize applications that were impossible to implement with less flexible program store devices or were prohibitively expensive due to the high cost of downtime or labor incurred by the user when changing the program. Some potential uses are calibration constants storage (continuous calibration); software alterable control stores (dynamic reconfiguration); remote communications programming; PC and NC industrial applications; CRT terminal configuration and custom graphic and font sets; military replacements for core memory and fuse link P/ROMs; point of sale terminals; remote alterable lookup tables; printer and communications controllers; and remote data gathering.

In addition, the EEPROM comes in a 24-pin package that conforms to the industry standard pinout for high density byte wide memories recently approved by the Joint Electron Device Engineering Council. By using the 2816 and printed circuit boards with 28-pin sockets, designers can be assured of future compatibility of microcomputer system memory components.

Circle 441 on Inquiry Card



Intel's iAPX 86/2816 EEPROM read architecture. EEPROM contains program information required by microprocessor

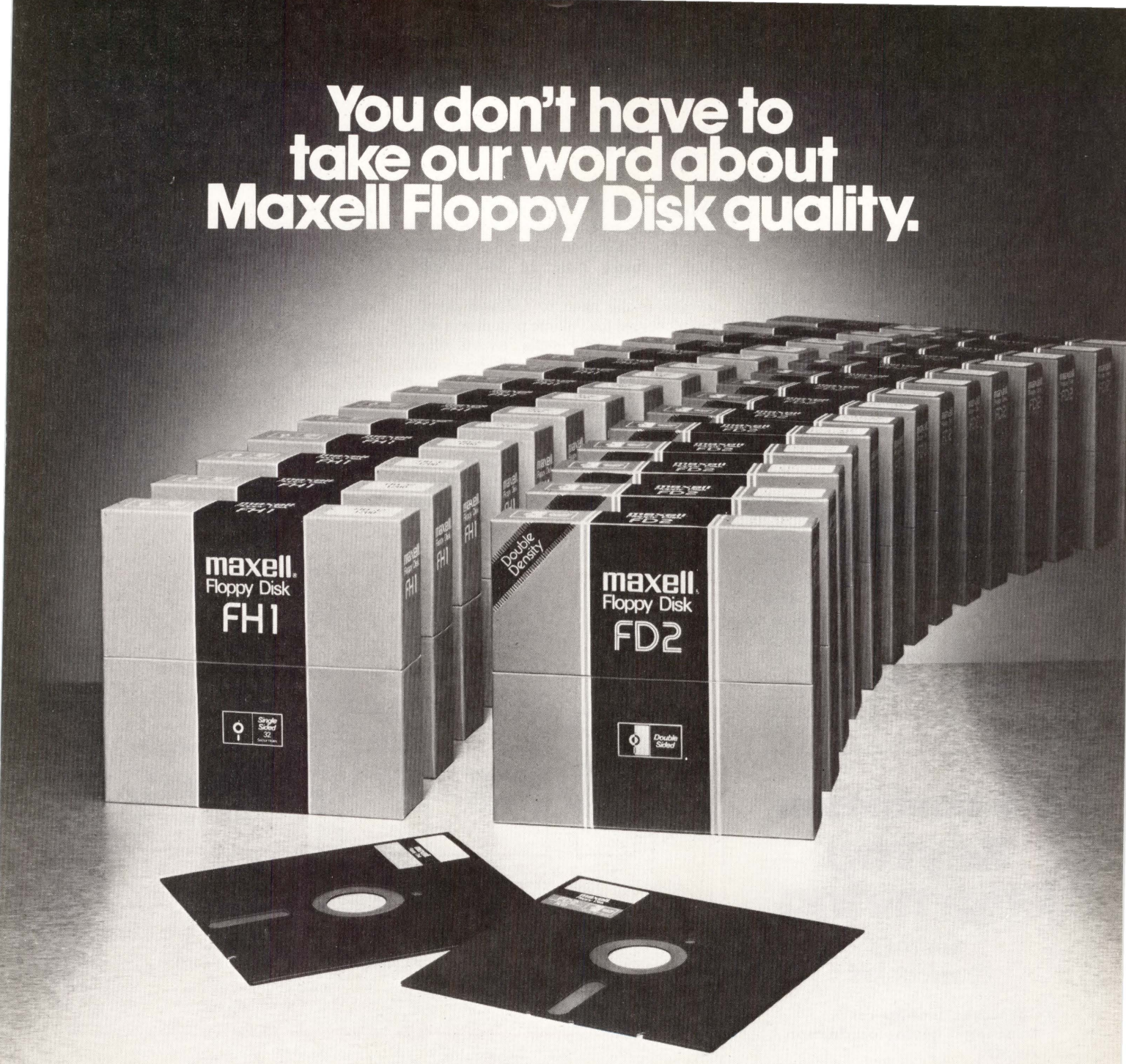
Low Power 9-Channel Data Acquisition System Operates from Single Supply

A recently announced monolithic, CMOS, 9-channel, 8-bit data acquisition system (DAS) operates from a single 5- to 15-V power supply and dissipates 0.25 W of power, maximum. Manufactured by Analog Devices, Rte 1 Industrial Pk, Norwood, MA 02062, the DAS utilizes a patented integrating technique called quad-slope. Designated AD7583, it converts an addressed channel's analog input to an equivalent 8-bit digital word in 4 ms. It is designed for battery powered systems.

AD7583 features relative accuracy, differential nonlinearity, and zero and full scale accuracy of ±1 count maximum. This accuracy is maintained over a supply range of 12 to 15 V and a temperature range of −125 to 85 °C. The device offers TTL or CMOS compatibility, requires six passive components and two general purpose op amps for operation, and interfaces directly to microprocessors.

(continued on page 184)

You don't have to take our word about Maxell Floppy Disk quality.



Ask the people who made your system.

Maxell Floppy Disks are either expressly specified or recommended by many major disk drive manufacturers. We're also relied upon by a growing number of 8" and 5¼" Floppy System owners. They find our Floppy Disks do everything possible to bring out the maximum performance of their systems. And they find our disks do this consistently.

Are we better than others? Will a box of ten Maxell Disks always contain ten disks that produce high performance results every time? We think so. We certify each one. We maintain extraordinary quality control. So they all meet or exceed the most critical industry standards.

But please ask the manufacturer of your system to double check our recommendation. See your computer products supplier. Or write to us for more information. We recommend dealers write to us about the opportunities Maxell Business Products offer.

maxell®

BUSINESS PRODUCTS DIVISION

Maxell Corporation of America, Business Products Division, 60 Oxford Drive, Moonachie, N.J. 07074 Tel: (201) 440-8020

CIRCLE 98 ON INQUIRY CARD

Designed for remote data acquisition applications requiring battery operation, the 8-bit accurate device may be applied in seismic measurements, oceanographic and weather balloon research, or anywhere remote data logging is required. Other applications include process control and, with 12-V operation, automotive data acquisition.

The ADC does not respond to analog inputs less than 0.15 or greater than 0.85 of the reference voltage. This is an advantage in single-supply applications, since buffer amplifiers driving the analog inputs can be connected to the same power supply. It also facilitates connection to ratiometric transducers whose zero output may not be at true zero.

Circle 442 on Inquiry Card

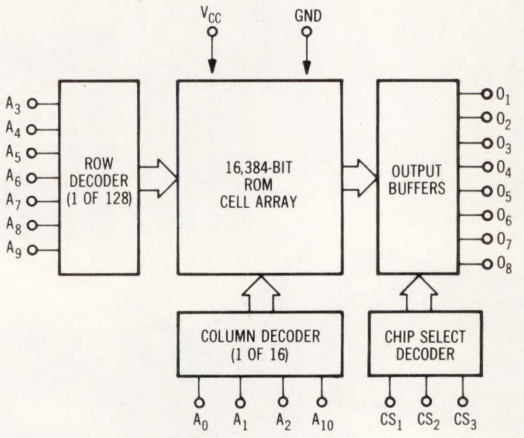
16k-ROM Is Fully Compatible with Bipolar P/ROMs

A high speed 16,384-bit static mask programmable ROM, organized 2048 words by 8 bits, is designed to be pin compatible with industry standard 16k bipolar P/ROMs, eg, 3636 or 82S191. The ROM eliminates the need to redesign printed circuit boards for volume production after prototyping with P/ROMs. SY3316 offers full TTL compatibility on all inputs and outputs and operates on a single 5-V power supply. The 3-state output buffers facilitate system expansion by allowing outputs to be wire-ORed together. These features, combined with a maximum access time of 80 ns, make the device suitable for applications where high performance, large bit storage, and simple interface are important design considerations.

Manufactured by Synertek Inc, PO Box 552, Santa Clara, CA 95052, the device utilizes fully static circuitry and operates asynchronously so that no clocks are required. The three chip select buffers are mask programmable to be any combination of high active, low active, or don't care that is desired. This allows up to eight ROMs to be OR-tied without external decoding.

Fabricated using scaled, high performance N-channel MOS technology, in combination with innovative design techniques, the device provides the high performance and ease of use features associated with nonclocked static memories.

Circle 443 on Inquiry Card



Block diagram of Synertek SY3316 high speed ROM. 16k bipolar P/ROMs are accepted as program data inputs. 3-state outputs allow wire-OR expansion

Gate Array Pair Have In-House Design And Fabrication

Two CMOS gate array devices have been introduced by Semi Processes Inc, 1885 Norman Ave, Santa Clara, CA 95050. SP7010 is a 1000-gate device with 500 device cells arranged in an array of 25 rows by 20 columns, 40 output driver pairs, and 76 bonding pads. SP7005 has 544 gates, 272 cells arranged in a 17-row by 16-column array, with 30 output driver pairs and 56 bonding pads. Each output driver on the chip can drive two standard TTL loads, or 3-state or CMOS devices. With 80% utilization, the SP7010 can accommodate 800 gates, the SP7005, 435.

Fabricated using a proprietary selective oxidation silicon gate CMOS process, the two metal mask programmable uncommitted logic arrays provide designers and OEMs with manufacturing control, design flexibility, and quick turnaround. Customers can give the manufacturer design specifications, do the design themselves, or use the company's computer aided design facilities to lay out the metal mask. According to company claim, functional device prototypes can be provided in 6 to 14 weeks and full production runs soon thereafter.

Circle 444 on Inquiry Card

Plessey Miproc 16 bit super power suits your needs!

Miproc-16 is the fastest 16-bit microcomputer card family available and has a compute-rate of 4 million instructions per second.

INSTRUCTION POWER Up to 170 instructions including multiply/divide and bit manipulation give Miproc-16 formidable processing capability.

16-BIT POWER 16-bit program words make programming easy. 16-bit data words maintain high precision in arithmetic operations.

ADDRESSING POWER 16-bit dual memory architecture gives 65k words of directly addressable program memory *and* 65k words of data memory with 8 powerful address modes.

INTERRUPT POWER Multilevel, priority vectored interrupt system handles context changes in less than 2 microseconds.

I/O POWER 256 directly addressable I/O channels with data I/O rates of up to 1.7 megabyte/s under program control, and up to 20 megabyte/s for DMA.

HIGH SPEED PROCESSING POWER The unique dual memory architecture combines with high-speed Schottky TTL technology to execute most instructions in a single 250 nanosecond machine cycle.

SOFTWARE POWER Comprehensive package available which utilises the powerful facilities of the DEC PDP11 including cross-assembler, PL Miproc high level assembly language and a full Coral package. And soon a disk-operating system with PASCAL.

HARDWARE POWER Comprehensive range of processor, memory and interface cards backed up by sophisticated hardware development aids.

RUGGEDIZED POWER Miproc can be configured to meet any known military specification.

FLOATING POINT POWER Ultrafast hardware, floating point add-on.

Available as standard commercial or full military systems.

Commercial Miproc is adaptable for various configurations and caters for up to three Miproc CPUs.

Military Miproc in a 1-ATR conduction-cooled chassis to MIL-E spec gives up to 3.3 million instructions a second, and unrivalled cost/performance.

PLESSEY MICROSYSTEMS

Plessey Microsystems Inc, 19546 Clubhouse Road, Gaithersburg, Maryland 20760 Telephone: (301) 948 2791 TWX: 710 828 9708
1641 Kaiser Avenue, Irvine, California 92714 Telephone: (714) 540 9931 TWX: 910 595 1930
France: Paris (01) 776 43 34 Holland: Noordwijk 01719 19207 Germany: Munich (089) 23 62 270
Japan: Eiji Kitahara, Tokyo 244 3782 UK: Towcester (0327) 50312.

0654 2 0122

Buffered 18-Bit Hybrid DAC Offers 16-Bit Linearity

An 18-bit DAC with true 16-bit (0.0008%) linearity, complete with storage registers, internal reference, and output amplifier, has been announced by Hybrid Systems Corp, Crosby Dr, Bedford Research Pk, Bedford, MA 01730. A single proprietary monolithic chip, in a hermetic 28-pin DIP, contains switches, storage registers, and other electronics for high resolution and low linearity error. TTL/DTL and CMOS compatibility, combined with low power dissipation, makes the DAC377 well suited for high resolution data conversion.

16-bit linearity has been attained by using an internal digital decoding technique, realized on a proprietary LSI chip, with a single-chip laser trimmed resistor network. Input registers are composed of three independent segments (two 8-bit and one 2-bit) with level triggered latches to provide compatibility with microprocessor data bus interfaces. The DAC dissipates less than 450 mW.

DAC377BO-18 operates over 55 to 125 °C and is screened to the requirements of MIL-STD-883, Method 5008. DAC377C-18 operates over 0 to 85 °C. Linearity and gain drifts are ± 1 ppm/°C FSR and ± 2 ppm/°C FSF, respectively, providing stability over the entire temperature range. Input coding is binary for unipolar operation, and offset binary for bipolar operation.

The propagation time of the DAC's input buffering circuits introduces a skewing of the digital data reaching the bit switches. The skewing causes the bit switches to operate asynchronously with each data change, producing an increase in the settling time, 1 to 2 μs, and large glitches. Dynamic performance of the DAC can be improved by using the internal latches on these units. The latches are located after the input buffer circuits and just before the bit switches. When correctly strobed, the latches present a data change to the bit switches in a synchronous manner. The latches should be closed while the input data is changing and propagating through the buffers. After the digital data has settled, the latch is loaded and the "new" data is transferred to the switches synchronously. The latch is then closed and is ready for the next data update.

Circle 445 on Inquiry Card

CMOS Gate Arrays Second Sourced For Semicustom Market

Designated NC5100, NC5150, NC5200 and NC5350, a line of semicustom gate array devices provides a direct second source for the Master Logic ML100 through ML350 devices. All products will be processed using metal gate CMOS technology, providing low power consumption, broad power supply range, and high noise immunity.

The devices range in complexity from 100 equivalent 2-input gates to 200 equivalent 2-input gates with 32 flipflops. They are a compromise between standard SSI/MSI circuits and full custom designed devices.

Nitron Inc, 10420 Bubb Rd, Cupertino, CA 95014, offers engineering and production support for its semicustom products. Pre-layout engineering consists of the processing of the first five layers of the wafer. Then, with a customer supplied layout of the sixth layer (the metal mask), the company completes the wafer processing. Prototypes of the customer's product are then supplied, and production quantities are manufactured.

Primary applications for the new devices will be as replacements for discrete logic implementation. In such applications, parts count should be reduced and reliability increased. The company's gate array products will be offered in standard plastic and ceramic dual-inline packages.

Circle 446 on Inquiry Card

Digital Multimeter IC Operates with Only 8 Components

A recently introduced digital multimeter IC, the ZN450, requires only eight external passive components for operation. Its versatility makes it suitable for a variety of measurement applications, such as voltage, current, resistance, weight, and temperature. The monolithic chip uses a delta-sigma modulation technique that not only ensures linearity but permits implementation of an auto-zero method that guarantees zero reading for 0-V input. The auto-zero function is completely digital in operation, eliminating the need for a capacitor to store error voltage.

The device, from Ferranti Electric Inc, Commack, NY 11725, needs no external active circuits and consumes less than 25 mW of power. Operating temperature range is 0 to 70 °C.

Circle 447 on Inquiry Card

Active Filter Use Seen For Three Quad Programmable Op Amps

Designed for use in active filter applications, three recently announced quad programmable operational amplifiers require no latchup, have built-in short circuit protection, and are fully programmable over a 100:1 current range. Designated TAB 1042, /43, and /44, the three devices will operate at supply voltages ranging from 1.5 to 12 V and are available from Plessey Semiconductors, 1641 Kaiser Ave, Irvine, CA 92714.

TAB 1042 and /44 are programmed by current to a common bias pin. However, the /44 has an exceptionally high short circuit current rating, which makes it ideal for driving high capacity loads. Although they both have excellent bandwidth characteristics, the /42 can be used to tailor bandwidth. Both can be used for battery powered applications because of their low power drain.

TAB 1043 is programmed through the use of two bias supply pins. It also allows users to program the first three linear amps with one voltage source, and the fourth linear amp with a different supply voltage. The /43 offers greater flexibility because the final amplifier in this IC can be programmed independently of the other three.

Circle 448 on Inquiry Card

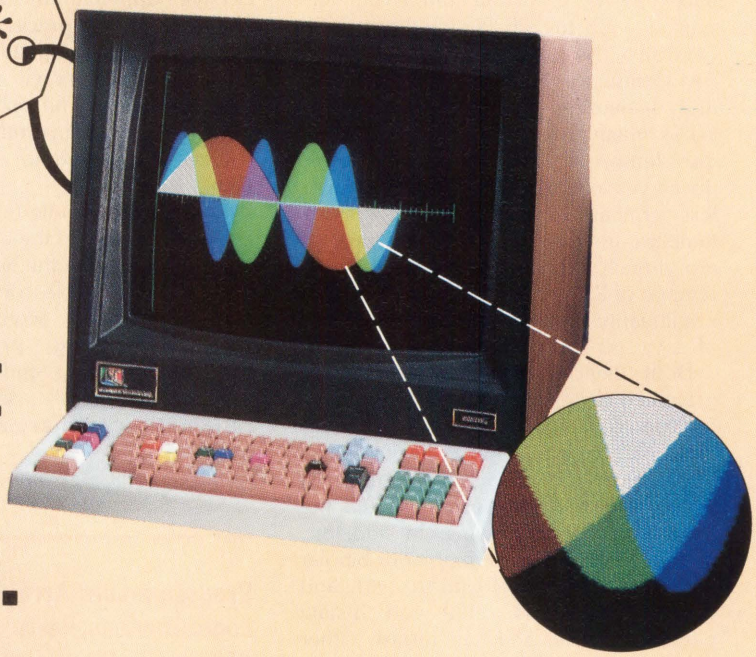
Low Power 1024-Word by 4-Bit Static RAMs Announced

A pair of 1024-word by 4-bit silicon on sapphire CMOS static RAMs, designed for use in memory systems where low standby power, low operating power, and simplicity of use are desirable, have been announced by RCA/Solid State Div, Rte 202, Somerville, NJ 08876. The RAMs, designated CDP1825 and CDP1825C, have a common data input and output and an extended temperature range of −40 to 85 °C.

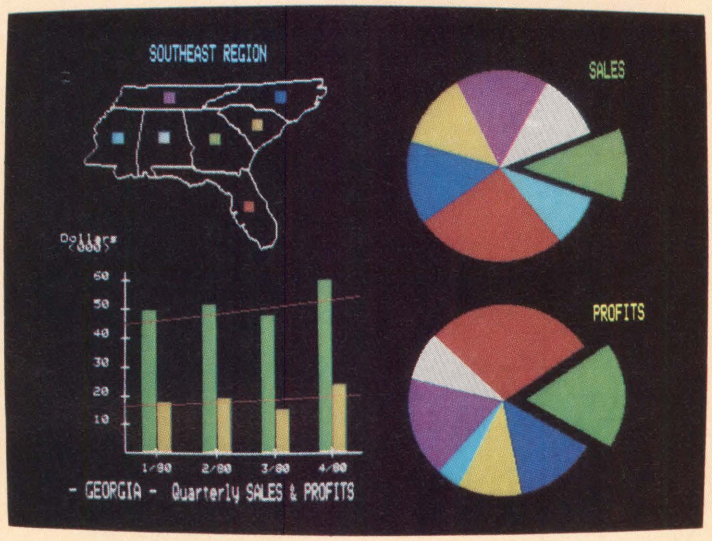
Both fully static devices operate from a single power supply with a memory retention for standby battery voltage as low as 2 V, minimum. CD1825 operates from 4 to 10.5 V. The range for CD1825C is 4 to 6.5 V. Supplied in 18-lead hermetic, dual-inline side brazed packages and in 18-lead dual-inline plastic packages, the RAMs have industry standard 1024 x 4 pinouts.

Circle 449 on Inquiry Card

Introductory Special
$3,355*
8001-I 19" CRT Terminal



Another ISC breakthrough: Affordable dot addressable color graphics.



Introducing the world's lowest priced high resolution color graphics.

Now high prices don't have to keep you from high performance graphics. ISC's new 8000 Series "I" terminals and desktop computers display color vectors and arcs with full-screen, 480 x 384 individual dot precision—note the close-up photo above. Impressive? With terminals starting at a quantity 100 price of $3,355, try incredible.

For any application requiring critical picture definition.

ISC's new "I" series is suited for process control, energy management, MIS—virtually any application needing sophisticated color graphics. Available in contemporary or industrial cabinets, each model features an 80 cpl by 48-line character format and RS-232C interface. Individual dots displayed in any of 8 colors can shade to a wide spectrum of color combinations.

ISC's "I" series desktop computers include File Control System Disk BASIC, 8K to 24K RAM, and 80K to 26-Megabyte disk. OEM prices start at $4,635, quantity 100.

With ISC's new "I" series, you can now get dot addressable color graphics for a third less than anything else on the market. And we include the keyboard! See for yourself why ISC is the world's largest manufacturer of color graphics systems—call **800-241-4310** for the name of your nearest ISC rep.

Note to current 8001G users: You can easily add ISC's dot addressable option to your unit. This is the kind of upward compatible growth you can expect from ISC! Consult our customer service department for complete details.

*Per unit. Single evaluation units sold on cash-with-order terms. Limit one per customer. Orders must be received by February 1, 1981. 30-day delivery from factory. U.S. domestic prices. Unretouched photos of screens.

Color Communicates BetterSM

Intelligent Systems Corp.®
Intecolor Drive ▪ 225 Technology Park/Atlanta ▪ Norcross, Georgia 30092 ▪ Telephone 404/449-5961 ▪ TWX 810-766-1581

CIRCLE 101 ON INQUIRY CARD

12-Bit A-D Converter Is Guaranteed over Full Temperature Range

Guaranteed at ±½ LSB maximum nonlinearity, and differential nonlinearity over 0 to 75 °C for the commercial version or −55 to 125 °C for the military version, the HI-5712A, from Harris Semiconductor Products Div, PO Box 833, Melbourne, FL 32901, features a 10 μs maximum conversion time and a gain tempco of 15 ppm/°C. A lower priced version, the HI-5712, is available for less critical applications. Except for temperature characteristics, the two ADCs are virtually identical; HI-5712 has a gain tempco of 25 ppm/°C and a guaranteed nonlinearity and differential nonlinearity of ±½ LSB at 25 °C.

Both devices can be software programmed to operate as 10-, 8-, or 6-bit converters with a corresponding reduction in conversion time. A flexible interface is provided for 8-, 12-, and 16-bit systems via the chip select line and the word length control pins. In addition, both will accept either unipolar or bipolar inputs, are compatible with DTL, TTL, and CMOS levels, offer serial and 3-state parallel outputs, and can furnish either binary or 2's complement binary output codes.

Fabricated using leadless chip carrier hybrid technology and assembled to both sides of a multilayer ceramic substrate which is part of the 40-pin DIP, the converters consist of eleven 0.02-μF decoupling capacitors and six hermetically sealed integrated circuits. The circuits comprise a laser trimmed 12-bit digital to analog converter, a 12-bit successive approximation register with 3-state latches, a precision 10-V voltage reference, a high speed comparator, a wide band operational amplifier, and a timing network. The onboard clock and reference can be overridden by external sources if required for special applications.

Designed to handle full-scale inputs of either 10 or 20 V in the unipolar mode or ±5 and ±10 V in the bipolar mode, the devices are suitable for applications in multichannel data acquisition, military, status monitoring, process control, medical monitoring, and instrumentation systems. MIL-STD-883 class B and high reliability commercial grades are available.

Circle 450 on Inquiry Card

Programmable Array Logic Devices Perform Arithmetic Operations

Latest members of the programmable array logic (PAL) Series 20 family from Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, can perform arithmetic functions such as add, subtract, greater than, less than, between limits, and equality. In combination with other members of the family, the PAL16X4 and PAL16A4 arithmetic PALs can replace 5400/7400 series TTL level functions, thereby reducing chip count and simplifying board layouts.

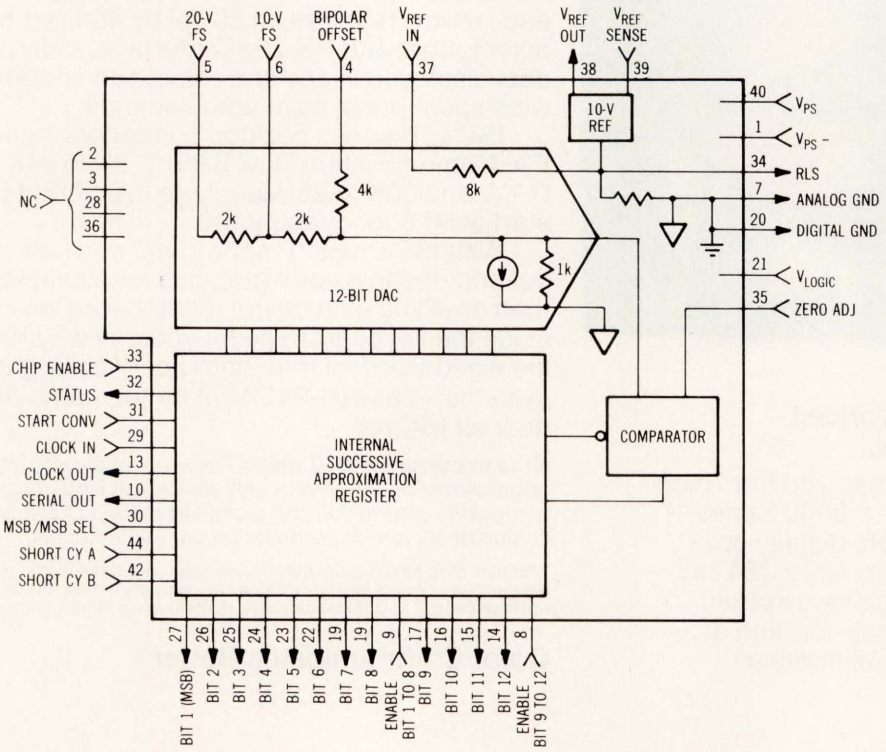
Exclusive-OR gates and gated feedback allow the devices to perform counting and logic functions without consuming an excessive number of product terms. The additional feature of a dedicated parallel carry in the PAL16A4 makes possible parallel addition and subtraction.

Arithmetic PALs are seen as basic building blocks for data path functions in computer architecture that requires arithmetic operations. Applications include 4-bit up/down counters with shift, program counters, and between limits comparators. PAL16A4 is ideally suited as an ALU with accumulator.

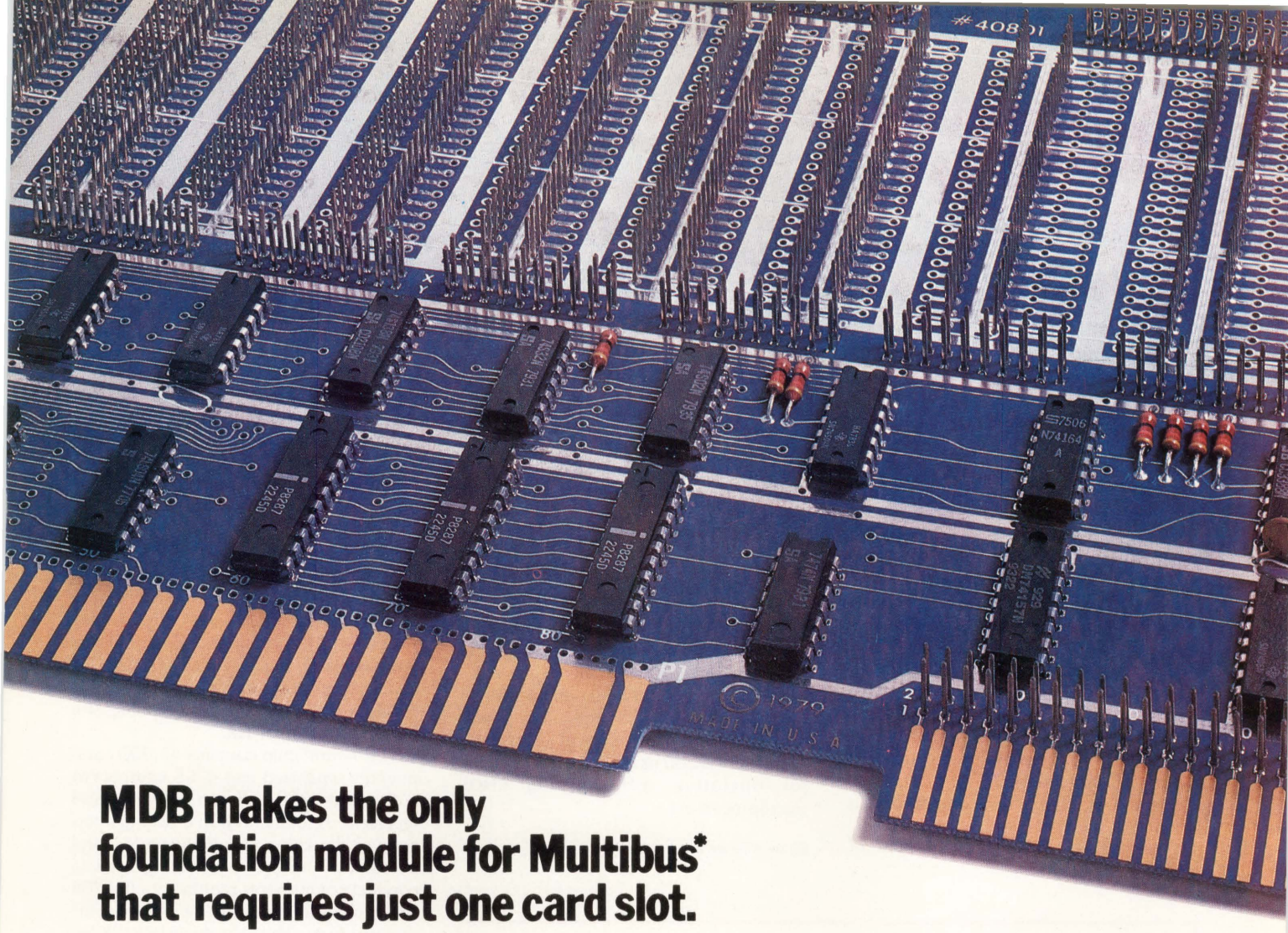
Propagation delay time of the arithmetic PALs is 40 ns maximum, specified over the voltage and temperature range. Clocked to output delay time is 25 ns maximum, also over the specified range.

The arithmetic PALs are fabricated with the company's advanced Schottky TTL process and bipolar P/ROM fusible link technology. They are housed in 20-pin SKINNYDIP packages.

Circle 451 on Inquiry Card



Functional diagram. Harris Semiconductor HI-5712/HI-5712A accepts user programmed unipolar and bipolar inputs. Output code select line and short cycle control inputs are latched internally for microprocessor compatibility



MDB makes the only foundation module for Multibus* that requires just one card slot.

Imagine what else we can do!

If you've never been excited about a foundation module before, now's the time. MDB offers the industry's first module for use with Intel 16 and 8 bit single board computers. It gives low cost Multibus-to-peripheral interface with complete address and interrupt logic, standard Intel board spacing and room for up to 38 sockets or IC devices of any size on the wire wrap portion of the board. Because all wire wrap pins and components are on the same side of the board, the module requires only one card slot. And it takes any configuration DIP package and provides three 50-pin edge connector positions. In addition, MDB makes a pure wire wrap general purpose module in a single slot configuration which has space for 60 IC positions. This is the kind of flexibility a logic designer dreams about.

If you're not an Intel user, you can still get MDB design flexibility—in single slot bus foundation and wire wrap modules for PDP**-11, LSI**-11, Data General and Perkin-Elmer computers and wire wrap boards for IBM Series/1. Even the dedicated portions of these modules are application adaptable in that they allow a change of functionality by the use of wire wrap pins.

What else can MDB do for you? Look at our line printer controllers. We offer more than 100 computer/printer combinations. If you need communications modules, interprocessor links, multiplexors and PROM boards, we've got them all with the built-in quality MDB is famous for.

MDB interface products are warranteed for a full year; most can be delivered in 30 days or less, and you can buy them under GSA contract #GS-00C-02423. What can we do for you?

*Trademark Intel Corp. **Trademark Digital Equipment Corp.

Circle 102 for Intel, 103 for LSI-11, 104 for PDP-11, 105 for DG, 106 for PE, 107 for IBM.

MDB SYSTEMS INC.
1995 N. Batavia Street
Orange, California 92665
714-998-6900
TWX: 910-593-1339

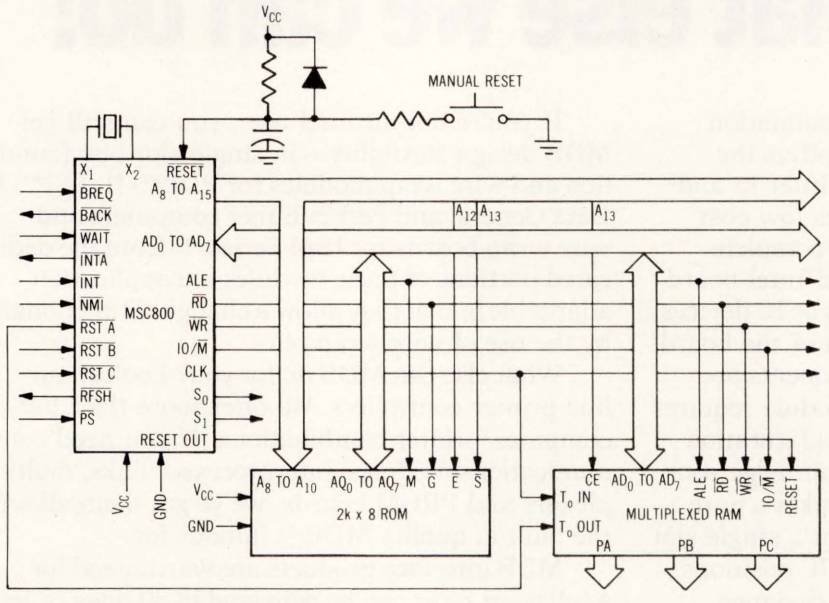
2048 x 8-Bit Multiplexed Bus ROM Is Mask Programmable

Designed for use in multiplex bus systems, a CMOS mask programmable byte organized ROM shares address and data lines and is therefore compatible with most CMOS microprocessors. The MCM65516, from Motorola Semiconductor Products Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721, is organized as 2048 bytes of 8 bits. The multiplexed bus design allows a reduction in the package size from 24 pins (used in standard NMOS ROMs) to 18 pins. Fewer external bus lines and the smaller package size mean higher board packing density.

CMOS microprocessor compatibility is enhanced by pins 13, 14, 16, and 17, which give the user the versatility of selecting active levels. Pin 17 allows the user to choose between high, active low, or a third option of programming which is termed the MOTEL mode. If this mode is selected by the user, it provides direct compatibility with either the Motorola MC146805E2 or Intel 8085 microprocessor series. In the MOTEL operation the ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle.

The ROM is designed for low active and low standby currents. An active power dissipation of 150 mW (at V_{CC} = 5 V, freq = 1 MHz) and a standby power of 250 μW (at V_{CC} = 5 V) mean low power for battery operation. Typical access time of the ROM is 280 ns, making it acceptable for operation with existing CMOS microprocessors.

Circle 452 on Inquiry Card



Typical MCM65516 connections. Data strobe (DS) on MC146805E2 and read bar ($\overline{RD}$) on 8085 control output of data from ROM but are of opposite polarity. Motorola 2k x 8 ROM can accept either polarity signal on DS input as long as signal toggles during cycle

Bipolar Logic Chip Capable of System/370 Data Flow Rate

An experimental 5000 circuit bipolar logic chip, claimed to be capable of the data flow of a System/370 Model 138 processor, has been developed by IBM Corp, Data Systems Div, East Fishkill, Rte 52, Hopewell Junction, NY 12533. Most of the chip's manufacturing processes are identical to those used for the 704 circuit transistor-transistor logic (TTL) and 1500 circuit Schottky current switch logic chips used in System/38 and 4300 series processors. The chip has an epitaxial layer, recessed oxide isolation, and three levels of metal. To facilitate manufacturing turnaround, a master slice or gate array technique was employed.

Speed of the circuit is 2.2 ns, but it is more conservatively clocked at 4 ns. This enables a machine cycle time of 100 ns, the approximate performance rating of a System/370 Model 138.

The 7-mm² chip contains 45,000 components organized into 4705 internal circuits and 218 offchip drivers and receivers. A total of 5.8 m of wiring interconnect the chip's circuit elements, compared with the 2.2 m of wiring used to connect components required by the 704 circuit chips found in the developer's current products. The chip dissipates 2.3 W, of which 1.6 W are consumed by the internal circuitry. All but 68 of the 11,000 connections were made with the automatic placement and wiring programs of the company's engineering design system.

System/370 architecture requires many active registers that could not fit on the chip, so a high speed, offchip local store is employed to contain the registers. The 60-ns access time of this local store is compatible with the 100-ns machine cycle time because of the driving power of the bipolar circuits. A 54-bit read only storage (ROS) word controls four major system components: an 8-bit arithmetic/logic unit, a 24-bit incrementer/decrementer, ROS word sequencing, and a control for two offchip memories.

A hardware forced microprogram entry system transfers control between microprograms on a microstop rather than on an instruction stop boundary. This facilitates the operation of very fast I/O devices during the execution of some System/370 instructions requiring hundreds of microinstructions. The same hardware can be expanded to solve such other difficut control programs as parity errors, push button interrupts, and memory wrap.

Circle 453 on Inquiry Card

DILOG INTERFACES DEC 11*

10 intelligent hard disc and magnetic tape controllers offer LSI-11,* 11/2, 11/23, and PDP-11* single quad slot compatibility with up to 60% power saving.

Only DILOG (Distributed Logic Corporation) exclusive automated design, common proprietary architecture and sophisticated bipolar μPs give you • all single board quad size products requiring no external power or chassis . . . just a cable to connect the drive . . . *you don't need anything else* • high reliability • automated self-test including data base protect feature and indicator. And at cost savings of 50% or more.

LSI-11 MAGNETIC TAPE CONTROLLER, Model DQ 120, interfaces 4 industry standard reel-to-reel drives • emulates TM11* • handles 7 and/or 9 track NRZI drives to 112.5 ips • selectable DEC or IBM byte order formatting • data error checking • RT-11/RSX-11* compatible • extended addressing to 128K words.

LSI-11 MAGNETIC TAPE COUPLER, Model DQ 130, interfaces dual density (NRZI/PE) formatted drives • emulates TM11 • handles up to eight 9 track 800/1600 bpi industry standard drives at speeds from 12.5 to 125 ips • "streamer" mode capability • software or switch selectable density • RT-11/RSX-11 software compatibility.

LSI-11 MASS STORAGE DISC CONTROLLER, Model DQ 200, interfaces any two SMD flat cable interface compatible hard disc drives for up to 500 MB on-line storage • mix or match compatible Winchester, SMD or CMD • variable sector size • automatic media flaw compensation with bad sector flagging • optimized logical to physical unit mapping • implements Winchester fixed head option.

LSI-11 SHUGART SA4000 WINCHESTER DISC CONTROLLER, Model DQ 201, emulates DEC RK* • runs drivers under RT-11 and RSX-11M* systems • compatible with 14.5 MB SA4004 or 29 MB SA4008 drives • automatic media flaw compensation.

LSI-11 DISC CONTROLLER, Model DQ 100, interfaces 2.5, 5, 10 or 20 MB cartridge and fixed platter drives in combinations to 80 MB • RKV-11/RKO5* emulator • handles front load (2315) and/or top load (5440) drives • automatic power fail/power down media protection • RT-11/RSX-11 compatible.

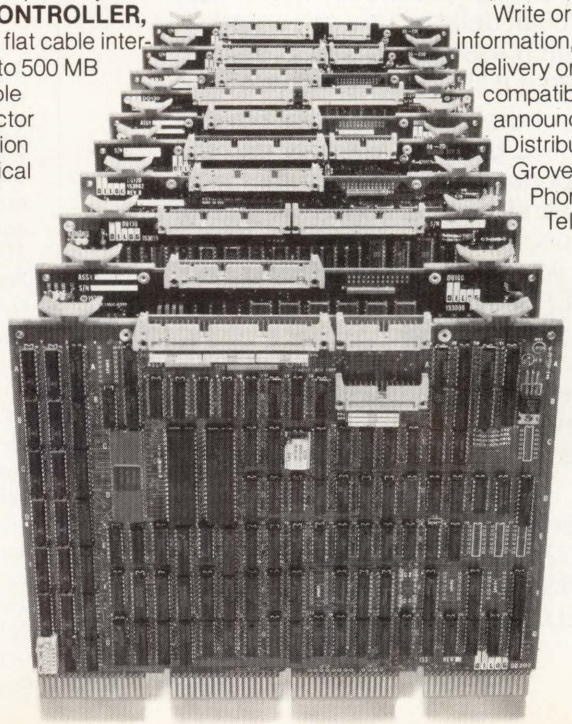
LSI-11 EMULATING MASS STORAGE CONTROLLER, Model DQ 202. Cost effective interface of two 8 and/or 14-inch Winchesters, SMD or CMD hard disc drives without changing controller . . . 8 to 300 MB capacity • RP emulator • automatic media flaw compensation.

PDP-11 MAGNETIC TAPE CONTROLLER, Model DU 120, emulates TM-11 and has same features as Model DQ 120 (LSI unit) • software compatible with RT-11, RSX-11, RSTS, IAS and MUMPS.

PDP-11 MAGNETIC TAPE COUPLER, Model DU 130, offers features of Model DQ 130 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS software compatible.

PDP-11 DISC CONTROLLER, Model DU 100 includes features of Model DQ 100 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS compatible • emulates RK-11.

PDP-11 EMULATING MASS STORAGE CONTROLLER, Model DU 202, offers same features as Model DQ 202 (LSI unit).



Write or call for detailed product performance information, OEM quantity pricing, stock to 30 day delivery or warranty data on these DEC 11 compatible products . . . or several soon to be announced new DILOG products.

Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, CA 92643
Phone (714) 534-8950
Telex: 681399 DILOG GGVE

DISTRIBUTED LOGIC CORP.
DILOG

All DILOG μP Products are Low Power, Quad Size

*Trademark Digital Equipment Corp.

CIRCLE 108 ON INQUIRY CARD

AROUND THE IC LOOP

Price of 8-Bit ADCs Reduced – Reductions of 30 to 45% in price on their line of 8-bit high accuracy ADCs has been announced by National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051. The reductions apply to ADC0801, ADC0802, and ADC0803 single-differential converters and ADC0808 and ADC0816 converters with 8-channel MUX.

Two Single-Chip Microcomputers Reduced in Price by 58% – Prices of two piggyback microcomputers, the MK38P70/02 and MK39P37/02, have been dropped by 58% (without EPROMs). The MK38P70/02 uses standard EPROMs and can emulate all 3870 microcomputers from 1k-bytes to 4k-bytes of ROM. Also using standard EPROMs, the MK39P73 has a hardware USART and emulates all of the company's 3873 single-chip microcomputers. Both devices are available from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 454 on Inquiry Card

High Speed Latch Is Compatible with Intel 3404 – A high speed latch is functionally identical to and pin for pin compatible with Intel's 3404. The 8T3404 from Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086, is designed primarily as a memory address register or data register, but can be used in any high performance storage application. Split controls allow for minimum package count in various word length systems. The data to output delay is 12 ns over 0 to 75 °C.

Circle 455 on Inquiry Card

2k x 8 CMOS RAM Is Pin Compatible with Byte Organized EPROMs – Offering HMOS speed, NMOS bit density and CMOS power dissipation, the HM6116 2k x 8 CMOS RAM is pin compatible with byte organized industry standard EPROMs. The unit has an access time of 120 ns, an operating power dissipation of 180 mW, and a standby power dissipation of 100 μW. It is available from Hitachi America Ltd, 1800 Bering Dr, San Jose, CA 95112.

Circle 456 on Inquiry Card

4k Static RAM Second Source Replacement Uses 20% Less Power – A second source replacement for the 2148 4k static RAM is pin and function compatible with the original device, yet uses 20% less power. D2148-3, from Intersil Inc, 10710 N Tantau Ave, Cupertino, CA 95014, is rated at 140-mA active current and 30-mA standby. Two versions of the device are offered. The D2148-3 has an access time of 55 ns, while D2148 has an access time of 70 ns. □

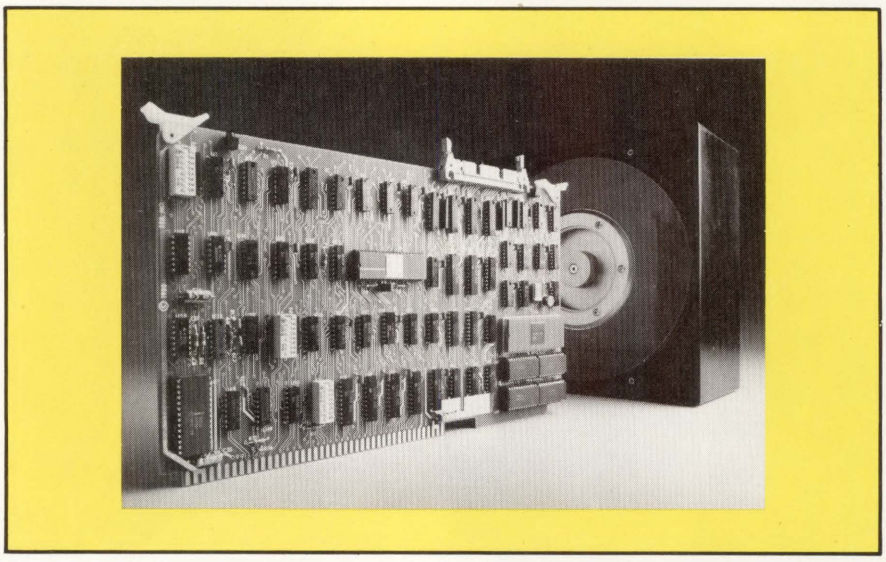
Circle 457 on Inquiry Card

CIRCLE 110 ON INQUIRY CARD

Single-Board Controller Handles Discs Complying with ANSI X3T9.3 Interface

The single-board Multibus compatible WDC 2880 controls up to eight 8″ Winchester disc drives complying with the ANSI X3T9.3 interface specification that is expected to become industry standard for 8″ Winchester drives. The X3T9.3 interface has been incorporated into disc products having capacities of from 10M to 60M bytes/unit from manufacturers that include BASF, Priam, and 3M.

Based on the 8X300 bipolar microprocessor from Signetics, the intelligent firmware driven controller manufactured by Interphase Corp uses the same basic architecture as the company's other hard disc controllers. The 8X300 acts as controlling device for all Multibus and disc activities, resulting in a design that requires only 62 ICs on a double-sided (not multilayer) board for exceptional reliability and low cost while retaining impressive performance characteristics. The controller uses a memory based I/O parameter block in combination with four switch selectable I/O registers to implement the mass memory interface.



Functional Operation

The controller has an 8- and 16-bit wide data bus, dynamically selectable under software control, and 20-bit address bus. During data transfers it operates as a true Multibus bus master and uses a variable burst length (from 1 to 256 bytes or words per burst) DMA to move data to or from anywhere in Multibus memory at maximum data rates to its onboard full-sector buffer. Sector size is selectable by onboard option switches.

During a sector write operation, the controller moves data into the sector buffer and adds the error correction code, locates the proper sector of the proper track of the proper surface of the proper disc unit, and finally writes the data plus ECC onto the disc. During sector read, the proper sector/track, surface/unit is located and data plus ECC are read into the sector buffer. The controller then checks data for validity (using the ECC code) and, if valid, moves them to the specified Multibus memory. If an error is detected, the controller decides whether to pass data through the ECC or to wait one revolution and try again. Automatic error recovery procedures include up to eight rotational retries per pass and up to five disc restores and reseeks. Hard errors up to 11 bits long can be recovered using the ECC hardware. No invalid data are passed to the Multibus, and no bus time is used for error recovery.

Multisector reads and writes are handled automatically, and the

sectors are interleaved to optimize data throughput. Track and surface boundaries can be overlapped by a multisector transaction with all implied seeks handled by the controller. Comprehensive diagnostic error reporting is provided when a transaction cannot be successfully completed.

Additional Features

A bad track mapping feature allows users to map a track with a hard error to a physically separate track (cylinder). Although all hard disc drives have a number of spare tracks intended to be used in this manner, most systems require the operating system to keep up with bad tracks; using this approach, the disc controller relieves the software operating system of that task.

Addressing modes include both absolute and relative addressing of the full 20-bit Multibus address space. This makes it fully compatible with all features of both 8- and 16-bit Multibus CPUs from Intel and others.

The unit provides true overlapped seek capability. This allows for very high performance in multiple-drive systems having operating systems capable of overlapped seeks.

Software drivers can be provided for standard operating systems such as CPM, ISIS II, MTOS 80, and MTOS 86. Compatible CPUs include 80/10, /20, /30, 86/12, and other single-board computers based on 8080, 8085, 8086, Z80, Z8000, and other devices. Two 20-bit addressing modes support both 8080 and 8086 style addressing features. Both series and parallel bus contention logic ensures operation in system environments that include those of an Intel MDS or National Starplex development system.

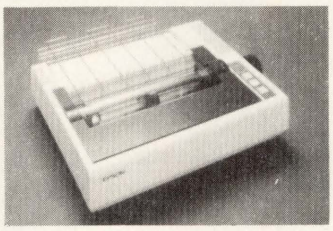
Price and Delivery

Single-unit price for the WDC 2880 is $1795. In quantities of 100, price is $1250/unit. Deliveries are 30 days ARO. Interphase Corp, 13667 Floyd Circle, Dallas, TX 75243.

For additional information circle 199 on inquiry card.

Correspondence Quality Dot Matrix Printer Uses Disposable Printheads

With life expectancy conservatively rated at 50M to 100M characters, the disposable Micro-Nine™ printhead in the MX-80 is replaced as simply as changing a ribbon cartridge. Making a clear original plus two carbons, the printer offers a choice of 40, 80, 66, or 132 columns of printing in as many as 4 distinct printing density modes: standard, double (advance paper 1/206th and repeat line), emphasized (shift right and double strike), and double emphasized (combination of double and emphasized). More than half of the 12 different combinations use multistrike or multipass techniques to generate correspondence quality printing.

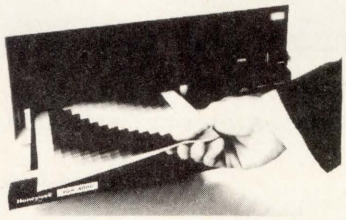


Bidirectional printing, logical seeking of shortest lines, 80-char/s capability, 64 graphics characters, and forms handling are other standard features. The unit provides the full 96-char ASCII set with descenders using the 9-pin head and a 9 x 9 matrix. Line spacing is 0.125, 0.166, or 0.097" (0.317, 0.421, or 0.246 cm), plus programmable. Throughput at 10 char/in (3.93/cm) using the logical seeking function is 105 lines/min for a 20-char line, 73 lines/min for a 40-char line, and 46 lines/min for an 80-char line. Interfaces include the standard Centronics style 8-bit parallel, and optional RS-232 or IEEE 488. A 1-line buffer is provided. **Epson America, Inc,** 23844 Hawthorne Blvd, Torrance, CA 90505.

Circle 200 on Inquiry Card

Video Graphic Hard Copier Produces High Resolution Images on Dry Paper

A fast reliable means of transferring data displayed on raster scan CRT terminal devices and other video sources, in the form of realtime images, to high resolution page sized hard copies, VGR 4000 provides photographic quality, black and white, and/or 16 shades of gray, permanent records of sketches, alphanumerics, or continuous tone images. The copier can accommodate data signals for most raster scan video sources with video line/field rates from 260 to 1329/50 to 60 Hz. An automatic lock-on feature eliminates all adjustments except those that optimize copy image.



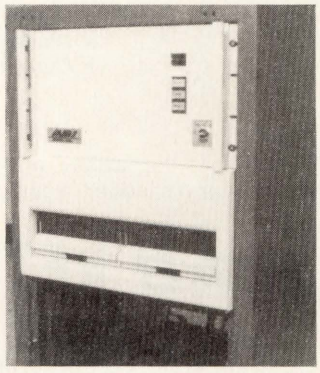
Data signals are accepted via the interface panel on the back of the recorder, processed, and applied to the fiber optic CRT. Dry silver paper is driven past the face of the CRT, exposed, developed by a temperature process, and presented as a dry permanent copy measuring 8.5 x 11" (21.6 x 28 cm). Total time is about 14 s. Two different image sizes can be printed. Changing the image from black on white to white on black requires a simple front panel switch change. Recording paper and paper cassette loading sequence are easily accomplished. Approximately 270 copies can be made from a 250' (82 m) roll of recording paper.

Basic design makes the unit desktop or rack mountable. The platenless copier runs cool, and consumes only 100 W on standby. Eliminating the platen reduces the size of the inner mechanism and paper path. The machine operates faster, and fewer moving parts make it more reliable. **Honeywell Test Instruments Div,** PO Box 5227, Denver, CO 80217.

Circle 201 on Inquiry Card

Array Processing System Handles Realtime Computation as Computer Peripheral

MARS-232 programmable array processor modules are designed for use in systems with demanding throughput requirements. In a basic configuration, the system can perform the industry standard 1k complex fast Fourier transform in 1.05 ms; multiprocessor configurations achieve higher performance levels. Floating point array processor modules typically are controlled by a minicomputer as programmable peripherals. Synchronous hardware design principles provide programming simplicity and easy interfacing of modules with each other.

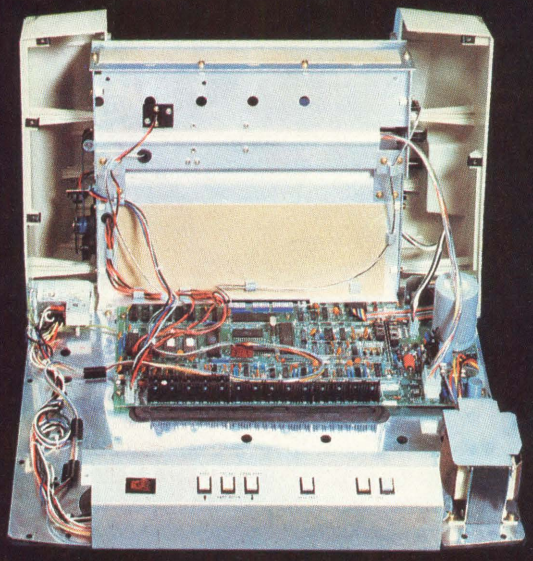


Data processor module is available in two versions: DP-R, which performs a single 32-bit multiply and two 32-bit adds in 200 ns; and DP-C, which is capable of four multiplies and six adds in 200 ns. The instruction set, involving more than 50 instructions, includes a large group of logical operations and many data dependent instructions. Architectural features include dual parallel 16-bit data paths and arithmetic units, and a set of 4 high speed memories with up to 64k 32-bit words each. Another system module, the interface processor, controls data flow in the system, handling prioritized device interrupt request arbitration and I/O transfers at a 20M-byte/s rate.

Packaging options include a midsize system consisting of two DPs and an IP integrated with power supplies and LSI-11/02 in a rack mountable 10.5" (26.7-cm) cabinet. This configuration can run standalone with use of ROM boards. **CNR, Inc, Computer Products Div,** 220 Reservoir St, Needham Heights, MA 02194.

Circle 202 on Inquiry Card

Say Ahh...



Our New grafixPLUS™ 80-column printer opens wide for easy servicing.

Introducing the newest members of our grafixPLUS™ family—the DP-9000 Series 80/132 column printers—built on the same tradition of quality printout, solid design and low cost of ownership established by our 132/220 column DP-9500 Series.

A Case for Serviceability

Not that is comes up often, but want to get inside? Simple. Just remove a few screws and the clam-shell case swings open exposing all major components. This easy access plus built-in self-test and minimum component count yields an MTTR of one-half hour. The 9-wire print head replacement's even simpler . . . two screws and it's out. Without opening the case. And without a service call.

Performance Plus

The DP-9000 Series prints the full ASCII 96 character set, including descenders and underlining, bi-directionally, at up to 200 CPS. Number of columns can go up to 80 or 132, depending on character density—switch or data source selectable from 10 to 16.7 characters per inch. And all characters can be printed double width. The print head produces razor-sharp characters and high-density graphics with dot resolutions of 72X75 dots/inch under direct data source control.

Interface Flexibility

The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

When you're ready for a printer (or several thousand), look into the grafixPLUS DP-9000 Series from Anadex—you'll find an open and shut case for quality. Contact us today for details, discounts and demonstrations.

Anadex®
...the plus in printers

...close please.

SALES OFFICES: San Jose, CA (408) 247-3933
Fullerton, CA (714) 871-0501 • Wakefield, MA (617) 245-9160 • Austin, TX (512) 327-5250

ANADEX, INC. • 9825 DeSoto Avenue • Chatsworth, California 91311, U.S.A. • Telephone: (213) 998-8010 • TWX 910-494-2761

ANADEX, LTD. • Dorna House, Guildford Road • West End, Woking, Surrey GU24 9PW, England • Tel: Chobham (O9905) 6333 • Telex: 858762 ANADEX G

CIRCLE 112 ON INQUIRY CARD

PRODUCTS

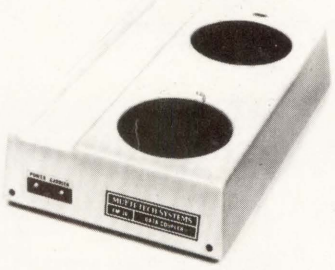
DATA COMMUNICATIONS

ASYNCHRONOUS LIMITED DISTANCE MODEM

Designed for asynchronous local data distribution of up to 9 mi (14.4 km) over private 2- or 4-wire nonloaded metallic lines at rates to 19.2k bits/s, model 6200 can be used in point to point and multidrop network configurations. Internal straps select receiver impedance, receiver equalizer, and 2- or 4-wire operation. Interface is RS-232-C/V.24. A 20 mA TTY current loop interface is also available. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865.

Circle 203 on Inquiry Card

PROGRAMMABLE ANSWERBACK ACOUSTIC COUPLER



Originate only 300-bit/s 103/113 compatible acoustic data coupler FM30AB has programmable answerback capability. Log-in code, password, or user authorization number is programmed into unit's P/ROM and code is answered back to the host on receipt of an ENQ signal by the coupler. Major application is in prevention of unauthorized access to timesharing systems, service and credit bureaus, and educational computing services. **Multi-Tech Systems, Inc,** 82 Second Ave SE, New Brighton, MN 55112.

Circle 204 on Inquiry Card

4-LINK MULTIPLEXER

Single board microprocessor based MX-4 mux allows four asynchronous data links to transmit over single synchronous composite channel full-duplex at rates to 9600 bits/s, with asynchronous option. Design features include switch programmable character formats and immediate character transmission. Composite channel loopback switch facilitates self-test. Automatic retransmission of link errors is provided. Interface is RS-232-C/V.24. Flow control is also optionally available. **Gandalf Data, Inc,** 1019 S Noel, Wheeling, IL 60090.

Circle 205 on Inquiry Card

449/422 INTERFACE FOR LIMITED DISTANCE MODEM

All standard interfaces plus EIA RS-449/422 are available with synchronous 2000 local area data distributor. Unit operates up to 10 mi (16 km) at selectable speeds from 1200 to 19.2k bits/s over unloaded lines or coax cables. It conforms to Bell Pub 43401 and operates 2-wire half-duplex, 4-wire half- or full-duplex, point to point or multipoint. High speed synchronous (to 64k bits/s) and asynchronous operation are available as options. Diagnostic capability eliminates need for external test equipment during installation and checkout. **Avanti Communications Corp,** Aquidneck Industrial Park, Newport, RI 02840.

Circle 206 on Inquiry Card

COMMUNICATIONS INTERFACES FOR PRINTER

Programmable controller on line printer INNOVATOR 202 implements numerous communication interfaces including parallel compatible with Centronics and DataProducts. It supports ASCII serial, IBM, Burroughs, and NCR protocols. The system is based on the Teletype[R] model 40 printer mechanism and uses heavy duty chain technology to print fully formed u/lc characters on up to six copies at 300 lines/min. 132- and 80-col models are available. **Innovative Electronics Inc,** 15200 NW 60th Ave, Miami Lakes, FL 33014.

Circle 207 on Inquiry Card

WHERE BUSINESS TALKS TO BUSINESS

"One Day" California Computer Shows

Norm De Nardi's *OEM and end-user* California Computer Shows... extending the limits of information between exhibitor and prospect...under one roof, in a highly charged, professional environment. In just one day, 1 p.m. to 7 p.m., as an exhibitor your company reaches more key decision makers. And that translates into lower costs of sales. As an attendee, you get a hands-on, buyer's eyeview of the latest in computer and computer peripheral products.

CAN YOU AFFORD NOT TO BE THERE?

Each show carefully focuses on a specific segment of the computer equipment market. As an exhibitor, you are virtually guaranteed a prescreened, invited audience of qualified decision makers. And the attendee can get right to their product area of interest, too.

The "One Day" California Computer Shows cut the cost of exhibiting and attending, effectively achieving the lowest-cost-per-prospect contact.

Firms typically exhibiting are Tektronix, AED, H-P, Control Data Corporation, Shugart, General Electric, Perkin Elmer, National Semiconductor, Xerox, Data General, Digital Equipment Corp., Mostek, Versatec, Lear-Siegler, Motorola, Data Products, Centronics, Intersil, Texas Instruments and Intel.

"One Day" California Computer Shows — the best investment you'll make in the future of your company.

"One Day" California Computer Shows.

March 12, 1981	**Inn at the Park Anaheim, CA**
April 23, 1981	**Hyatt Hotel Palo Alto, CA**

NDN

Norm De Nardi Enterprises

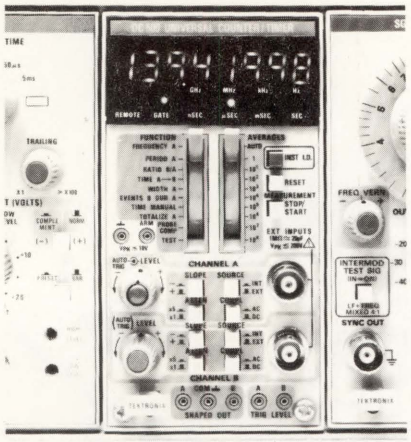
95 Main Street, Los Altos, CA 94022, (415) 941-8440.

Invitations are available from participating firms, or NDN Enterprises. Call or write today for information.

CIRCLE 114 ON INQUIRY CARD

TEST AND MEASUREMENT

UNIVERSAL COUNTER/TIMER

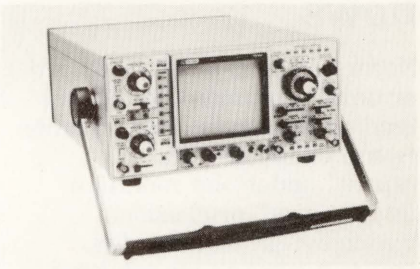


DC509, a high performance TM 500 plug-in, makes single-shot time interval measurements with 10-ns resolution. Measurement averaging permits 1-ps resolution. Frequency measurements to 135 MHz are made using reciprocal counting technique that provides high resolution of low frequency signals faster than conventional counting techniques. Auto trigger senses applied signals and automatically sets both trigger levels to optimum trigger points. Front panel monitoring jacks permit precise trigger level adjustments. Outputs of the signal shaping circuits can also be monitored helping set trigger point on complex waveforms. Probe compensation function compensates the high impedance probe to the counter. **Tektronix, Inc**, PO Box 500, Beaverton, OR 97077.

Circle 208 on Inquiry Card

100-MHz QUAD-TRACE SCOPE

Triggered sweep model 1500 features a full complement of controls for dual-trace display plus inputs and controls for two additional vertical inputs. When signals are displayed on channels 1 and 2, channel 3 may display external triggering signal applied to Channel 1, while channel 4 displays trigger signal for channel 2. Four signals not related in frequency can be displayed in sync simultaneously. Any of 4 channels can be displayed or deleted. For channel 1 and 2, vertical input attenuator offers 10 ranges in conventional 1-2-5 sequence with vernier provided. A selectable 20-MHz bandwidth limited circuit restricts −3-dB bandwidth to 20 MHz, filtering out extraneous signals at higher frequencies. **B&K-Precision, Dynascan Corp,** 6460 W Cortland St, Chicago, IL 60635.



Circle 209 on Inquiry Card

COMPUTERS AND COMPUTER SYSTEMS

ARRAY PROCESSOR

IP8500 provides realtime histogram calculations and Boolean functions, fast vector generation, 64-char font generation, and switchable synchronization. Compatible with DEC PDP-11 systems, the unit has up to 20 image memories of 512 x 512 x 8 bits, enhancing use in applications requiring high resolution color, multi-image monochrome, or pseudocolor displays. 4 output channels provide independent pan or integer zoom. Max system stores 1024 x 1024 x 32 image in 512- x 512- x 32-bit image window. **DeAnza Systems, Inc,** 118 Charcot Ave, San Jose, CA 95131.

Circle 210 on Inquiry Card

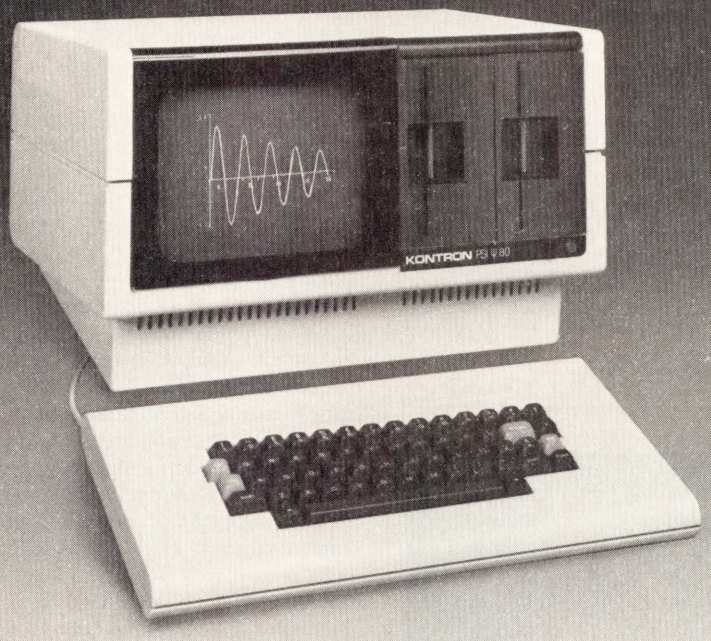
MILITARIZED MINICOMPUTER

Designed for use in rigorous airborne, shipboard, ground based, and land mobile environments, PDP-11/44M is a fully militarized version of the DEC PDP-11/44. It meets all required military specifications and carries the AN/UYK-42 (V) designation. The minicomputer can use all the software developed by DEC for the PDP-11 commercial line. Applications include tactical functions, command and control, administration, logistics, fire control, and communications. **Norden Systems,** Norwalk, CT 06856.

Circle 211 on Inquiry Card

This is Kontron's PSI80 Series Intelligent Computer/Controller

NEW



Introducing . . .
Kontron's PSI80 Series Intelligent Computer/Controller System. The new PSI80 system is designed to control most processes via IEEE 488 bus, RS 232 and parallel interfaces. Additionally, the PSI80 can be easily adapted to any analog or digital source for process control through standard ECB computer boards on a modular basis. Standard features include:

- 32/64 KByte RAM
- Single/dual minifloppies, 144 KBytes each
- Two RS 232 interfaces (synchronous and asynchronous)
- Parallel I/O, Centronics compatible
- 19-inch rack mount capability
- Full graphic video display with an extra 16 KByte video RAM, upper and lower case with extenders on 25 lines at 80 characters
- 9-inch monitor
- Detachable keyboard

Plus . . .
The PSI80 is fully expandable via Kontron's unique card cage design which accepts six Kontron ECB cards for these user-specified functions:

- CMOS RAM (ECB V)
- IEEE 488 (ECB B)
- High-speed arithmetics (ECB A)
- Analog I/O (AN-μP80)
- Digital I/O (ECB I)
- Real time clock (month, date, etc.)
- Subprocessor modules for multiprocessor applications (Z80-EML/SP)

Get complete details and the name of a Kontron sales and service organization near you.

Write or call
Kontron Electronic Inc.
630 Price Ave.
Redwood City, CA 94063

COMPUTER/CONTROLLERS:

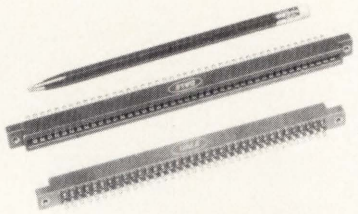
For data on Kontron® Computer/Controllers, Digital Multimeters, Counters, PROM Programmers, Logic Analyzer and Printers, call (800) 227-8834. In California call (415) 361-1012.

CIRCLE 116 ON INQUIRY CARD

PRODUCTS

PACKAGING AND INTERCONNECTION

36- AND 43-CONTACT EDGEBOARD CONNECTORS

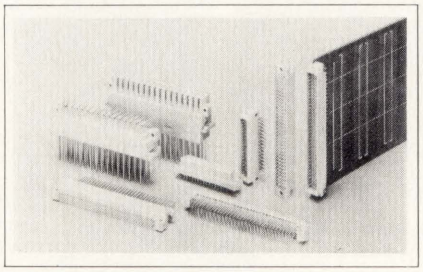


Expanded EB 7D line features 0.156" (4-mm) contact spacing and will accept 0.062" (1.6-mm) circuit boards. The UL-listed line is also available with 6, 10, 15, 18, and 22 positions. Contact plating choices include gold per MIL-G-45204, gold flash, or electro tin plate per MIL-T-10727. Wide choice of mounting variations and contact terminations is available. **Dale Electronics, Inc,** E Hwy 50, Yankton, SD 57078.

Circle 212 on Inquiry Card

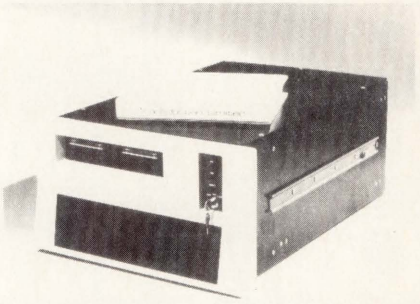
HIGH DENSITY 2-PIECE PCB CONNECTORS

Two-piece series 100 PCB connectors, available with up to 96 contacts in three row, have bifurcated female contact design with dual-wipe hard gold plated surfaces. Mating tolerances of 0.001" (0.025 mm) produce minimal abrasion. Contact resistance is less than 15 m after 100 mating cycles. Series mates with all IEC 48B- and DIN 41612-spec components. Five types offer hundreds of contact arrangements for 16, 32, 48, 64, or 96 throughlines, and are available for wave solder, wirewrap, or hand solder. **Panduit Corp, Electronic Products Group,** 17301 Ridgeland Ave, Tinley Park, IL 60477.



Circle 213 on Inquiry Card

PDP-11 COMPATIBLE ENCLOSURES



SUPERBLUE/11 combines power supplies, backplanes, card cage, front panel controls, power cord, and chassis slides in a DEC compatible package. Dual-purpose bus converter kit (Q-BUS to UNIBUS or UNIBUS to Q-BUS) and dual-drive DECtape II cartridge assembly are optional. The package accommodates both 9-hex slot LSI-11 (DEC DDV-11B) and PDP-11 (DEC DD11-DK) backplanes in any of 5 optional configurations with 18 hex slots (54-dual) max. Two independent bus structures can be used under control of one CPU with aid of the bus converter kit. Extended (board height) LSI-11 and PDP-11 bus grant cards are included with each backplane. Board insertion is from the top, facilitating access to cable connectors and allowing visual monitoring of activity lights of system controllers and interfaces. High efficiency power supplies provide 50 A at 5 Vdc, 6 A at 12 Vdc, 1 A at −12 Vdc, 6 A at 15 Vdc, and 1 A at −15 Vdc to service either CPU, memories, and controllers. **Transduction Ltd,** 1645 Sismet Rd, Unit 11, Mississauga, Ontario L4W 1Z3, Canada.

Circle 214 on Inquiry Card

10-POSITION PCB FLAT RIBBON CABLE CONNECTOR

Flat ribbon cable connector housing is made of black reinforced polyester thermoplastic and contacts are of nickel-silver alloy with tin alloy surface finish. Standard cable is 28 AWG stranded on 0.05" (1.3-mm) centers, gray or rainbow PVC. Other dielectrics such as Teflon® are available. PCB line now covers six sizes from 10- to 50-position. **The A P Great Jumper Co,** Box 938, 72 Corwin Dr, Painesville, OH 44077.

Circle 215 on Inquiry Card

THERE IS ONLY ONE 32-BIT COMPUTER WHOSE LOGIC DOESN'T DEFY LOGIC.

PRESENTING THE DATA GENERAL ECLIPSE MV/8000.

Apparently, our competitors are operating under the premise that there is no need to make their new computers compatible with their older ones. And have no qualms about rendering obsolete the years of man-hours and the hundreds of thousands of dollars you've invested in software.

At Data General, we believe this kind of logic defies logic. Which is why we designed our 32-bit MV/8000 to protect your software investment.

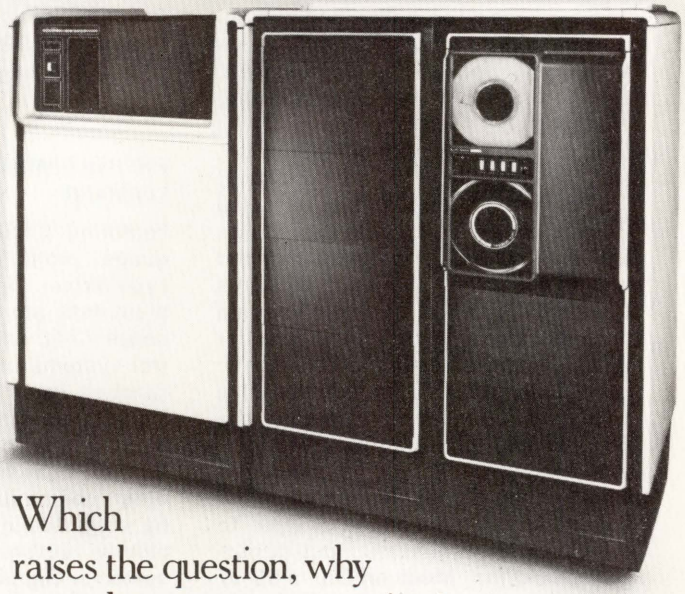
Not destroy it.

However, the MV/8000's software compatibility is only part of what places it in a class by itself. Another factor is speed. It's the fastest computer of its size on the market.

In fact, its 36.4 MB/sec memory bandwidth is at least two to four times faster than its nearest competitor.

It's also more reliable, much easier to maintain, quicker to get operational (it not only offers the widest range of software, but the widest range of languages*) and offers sophisticated security features, word processing, communications capabilities and data base management. All superior to its nearest competitor.

And while these features alone make the MV/8000 a most attractive investment, there's something else. It also costs less than its nearest competitor.



Which raises the question, why go to the nearest competitor?

If the logic of purchasing any other 32-bit computer escapes you as much as it escapes us, just fill out the coupon and we'll be happy to fill you in on the one computer that eclipses them all.

The remarkable new Data General Eclipse MV/8000.

Data General

Mail to: Data General Corporation
4400 Computer Drive, MS C228
Westboro, Massachusetts 01580

Attention: Marketing Communications Department

☐ Please send me more information on the Data General Eclipse MV/8000.

☐ Please have a sales representative call on me immediately.

Name _____ CDG-11-80

Title _____

Company _____ Tel. _____

Address _____

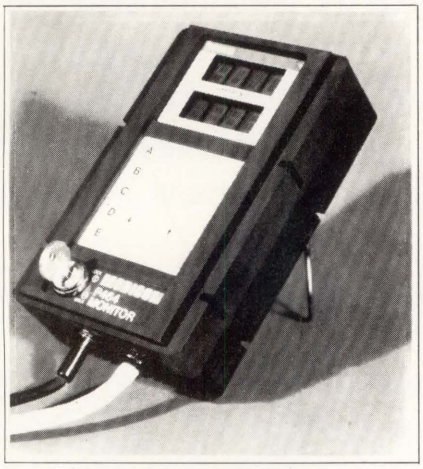
City _____ State _____ Zip _____

*Fortran 77, Cobol, Basic, PL/1 and RPG II

CIRCLE 118 ON INQUIRY CARD

DATA ACQUISITION AND CONTROL

HANDHELD PROGRAMMABLE CONTROLLER MONITOR



P464 provides an online operator interface to the 484 programmable controller for monitoring, maintenance, and debugging. It plugs directly into the controller's front panel or J470 EIA adapter. Measuring 7.5" high, 4.5" wide, and 2.5" deep (19.0, 11.4, and 6.3 cm), it has a sealed 24-position keyboard with two 4-digit LED displays and is housed in a rugged drip proof case. The unit monitors status of discrete or analog inputs and outputs, displays timer and counter values, checks results of arithmetic operations, HOLDS (on command) a displayed value, and monitors the RUN state of the controller. It also permits single-key access to important variables via 5 user defined keys. An optional model enables the user to disable or force discrete input or output. **Gould Inc, Modicon Div,** 155 W Big Beaver Rd, Suite 104, Troy, MI 48084.

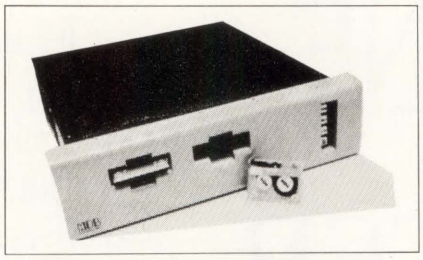
Circle 216 on Inquiry Card

FIBER OPTIC LINK FOR MULTIPLEX CONTROL SYSTEMS

Fiber optic link is offered as alternative to twinaxial wiring for Cutler-Hammer DIRECTROL® multiplex control systems. The link makes these systems inherently safe and immune in high noise and potentially explosive environments. The fiber optic link is a complete package including interface modules, cable, and an installation kit having instructions, connectors, tools, and decladding and recladding chemicals. **Eaton Corp, Cutler-Hammer Products,** 4201 N 27th St, Milwaukee, WI 53216.

Circle 217 on Inquiry Card

DATA LOGGING SYSTEM FOR HARSH ENVIRONMENTS

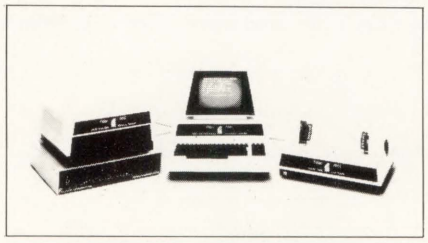


MLSI-11/03-580 incorporates an LSI-11/2 CPU, 2 TU58 cartridge tape units with 500k-byte data capacity, 2 asynchronous serial ports, line time 60 cycle clock, switching power supply, bootstrap (MXVIIAC), dual-width backplane, and 32k bytes of RAM. Chassis requires 5.25" (13.33 cm) of panel height, and may be RETMA rack mounted or configured for rolling cart or hand carry. System is equipped with self-contained power on/off and front panel control switches. **MDB Systems, Inc,** 1995 N Batavia St, Orange, CA 92665.

Circle 218 on Inquiry Card

PROGRAMMABLE DATA LOGGER

Featuring BASIC and assembly language programming, CRT display, typewriter keyboard, and program/data storage capability, FIDAC series 7240 data acquisition and control systems offer a range of plug-in function cards for analog and digital signals plus mini-disc memory and impact printer options for versatility. IEEE-488 controller capability allows other compatible instrumentation to be integrated into the system for completely automated electronic test systems. Signal linearization, averaging, multiple alarm limits, and data display on the 40-char by 24-line CRT are accomplished by std software packages. Single- or dual-data tape recorders store programs and data. Basic system incorporates 12-bit ADC with input multiplexer, digital I/O, pulse counting, and range of optional plug-in function cards. **F. I. Electronics,** 968 Piner Rd, Santa Rosa, CA 95401.



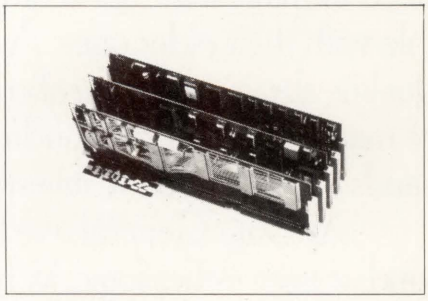
Circle 219 on Inquiry Card

FREQUENCY DOMAIN A-D CONVERTER

ADC-4450 features both −72-dB total harmonic distortion and −72-dB intermodulation distortion to meet critical frequency domain parameters; 12-bit resolution and 1.5-μs conversion time make the device suitable for digital signal analysis instruments such as spectrum analyzers, and fast Fourier transform equipment. The successive approximation design is characterized in both frequency and time domain. Packaged in a standard 2 x 4 x 0.4" (5 x 10 x 1.0 cm) discrete module, the converter is offered for external (-4450) or internal clock (-4452) applications. With pin programming, the user has a choice of 6 unipolar and bipolar input ranges. Output is 12 bits in both parallel and serial format with 5 TTL load drive capability. Operating with a 7.5-MHz clock, the converter offers full ± ½ LSB linearity and no missing codes. Gain and offset may be adjusted for system calibration. A pin programmed internal reference is provided in both models and can provide up to 0.5-mA drive to external circuits. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.

Circle 220 on Inquiry Card

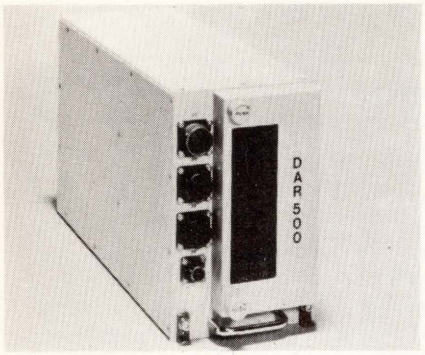
DISTRIBUTED INTERFACE SYSTEM



SAMUX II serial addressable multiplexer system is controlled by host computer via a 4-wire serial communication link; up to 64 individually addressable stations located up to 5000' (1524 m) away can be connected to the host via an asynchronous full duplex serial link. Features include expandable power I/O or combined analog and digital I/O, timing or time delay functions, latched inputs, event counters, watch dog timer, RS-232 or other communications options, selectable baud rate, and PB-24 mounting racks. **Opto 22,** 15461 Springdale St, Huntington Beach, CA 92649.

Circle 221 on Inquiry Card

DATA ACQUISITION AND RECORDING SYSTEM

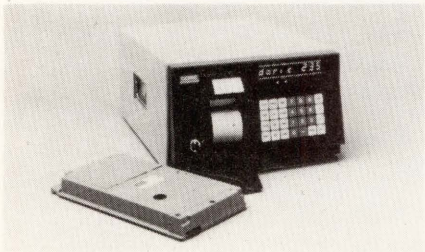


Operating with dual microprocessors, system stores 600M bytes on ANSI compatible 0.25" (0.63-cm) tape cartridge, and handles 4 channels of serial asynchronous data at 0 to 200k bits/s. 128k-bit data bursts are accommodated at megabit rates. Unit records at 7200 bits/in (2834/cm) serpentine fashion on 10 tracks over the 700' (210-m) tape length. Drive uses 10,000-h brushless dc motor with proprietary digital servo. Input power is 115 V, 47 to 440 Hz, single-phase. **Peripherals Development Associates, Inc,** 3303-B1 Harbor Blvd, Costa Mesa, CA 92626.

Circle 222 on Inquiry Card

DIGITAL DATA LOGGER

Digitrend 235 is a multitasking, multiprogramming instrument for scanning or realtime monitoring that can serve as intelligent front end for a computer. It accepts a broad range of thermocouple and other industrial sensor signals and can monitor up to 100 analog input measurements (points), including millivolts, voltage, current, and resistance inputs, and up to 96 digital inputs. It can also be used as a moderate speed data acquisition device with up to 256 separate alarm points and a max of 4 alarm setpoints/input. Std programmable serial I/O and digital I/O options permit interfacing with various computer peripherals. Based on the 6800 microprocessor, the unit can be used in harsh environments. **Doric Scientific, Emerson Electric Co,** 3883 Ruffin Rd, San Diego, CA 92123.



Circle 223 on Inquiry Card

MEMORIES

UNIVERSAL P/ROM PROGRAMMER AND ROM SIMULATOR

Including RS-232-C and TTY interfaces, to simplify downline loading from host microprocessor development system, Ariel programs any single- or triple-voltage, 256- to 128k-bit, MOS EPROM. EPROM code and type are entered through a hexadecimal keyboard. Pushbutton controls reset the unit, load RAM from master EPROM, verify RAM against master, and program or verify copy EPROM. Simulation cable allows unit to replace EPROM for system/software tests in ROM simulation mode. **American Microsystems, Inc**, 3800 Homestead Rd, Santa Clara, CA 95051.

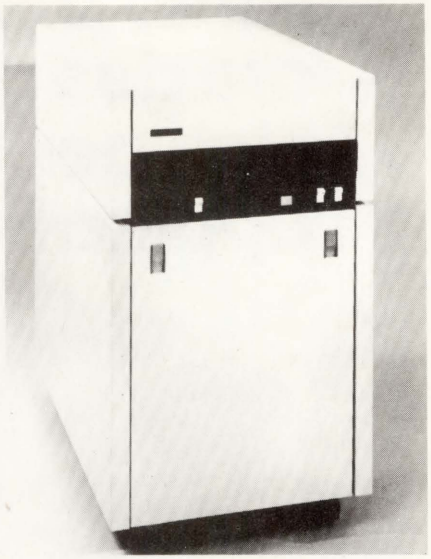
Circle 224 on Inquiry Card

MILITARY CARTRIDGE RECORDER/REPRODUCER

ECR-40 emulates capabilities of 125 in (317 cm)/s reel to reel recorders, recording up to 48M bytes of 9-track parallel phase encoded data at 6400 bits/in (2519/cm). Offering shuttle speed up to 240 in (609 cm)/s, the unit achieves data transfer rates of 200k bytes/s at 31.25 in/s within 3 ms. The unit is mounted in ½ ATR rack or front panel, and has a transport mounted on 4 vibration isolators in heavy frame. Recorder uses ANSI compatible 0.5" (1.27-cm) tape, and provides modular interface, bidirectional playback, auto locking, and self-tensioning drive. **Genisco Technology, Systems Div,** 18435 Susana Rd, Rancho Dominguez, CA 90221.

Circle 225 on Inquiry Card

CDC COMPATIBLE DISC DRIVE

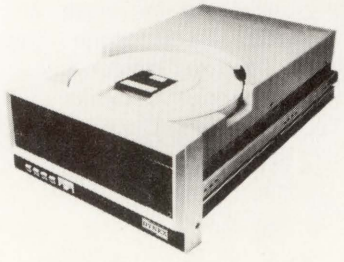


A plug compatible and media interchangeable alternative to the 30M-byte CDC 9766, DM-9300AQ uses CDC 9883-91 type 20-surface disc packs, and is housed in a foam insulated cabinet to reduce acoustical noise. Drive complies with FCC standards for electromagnetic radiation. 30" (76-cm) high unit allows front, rear, and top access, and LED indicators assist troubleshooting. Features include SMD compatible interface and single-port daisy chain version of the basic interface. **Ampex Corp, Memory Products Div,** 200 N Nash St, El Segundo, CA 90245.

Circle 226 on Inquiry Card

10M-BYTE FIXED DISC DRIVE

Series 4000 is a direct replacement, and is interface compatible with CDC, Perkin-Elmer, Dynex, and other cartridge disc drives. When combined with the 10M-byte series 6000 cartridge disc drive, system expansion to 40M bytes in any combination of fixed disc and removable cartridge drives is possible. Each drive has its own built-in backup, comprehensive documentation, and 1 yr mechanical and 90 day electronic warranty. **Western Dynex Corp,** 3536 W Osborn Rd, Phoenix, AZ 85019.



Circle 227 on Inquiry Card

STRIPPED DOWN FLOPPY DISC SYSTEM

Functionally equivalent to the DEC 11V03-L, MF-211 dual floppy disc system has either 4- or 8-quad backplane that can handle any LSI-11/2 or -11/23 series card. The controller has all necessary electronics for control, interface, bootstrap loader, formatter, and self-tester. Controller is completely RX02 equivalent including media and software compatibility. The system is mounted in a 10.5" (26.7-cm) rack mountable enclosure. A system containing two double sided 1M-byte drives is available if more storage is required. **Charles River Data Systems, Inc,** 4 Tech Circle, Natick, MA 01760.

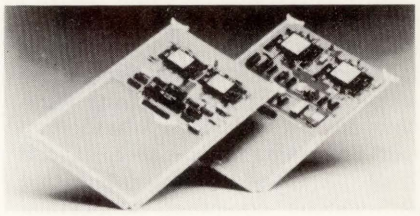
Circle 228 on Inquiry Card

WINCHESTER DISC DRIVES

Mass storage devices MSM80F and MSM80F/HPT have 67M bytes of formatted storage accessed by moving heads. Std fixed head segment of the /HPT is accessed by 96 data heads located in head/disc assembly to provide 1.6M bytes storage without repositioning delays. Programmed internal microprocessor unit initiates and controls such functions as seek, read/write, data separation, and internal diagnostics. **Perkin-Elmer Corp, Computer Systems Div,** 2 Crescent Place, Oceanport, NJ 07757.

Circle 229 on Inquiry Card

MAGNETIC BUBBLE MEMORY PROTOTYPING BOARDS



TBB5990, TBB5902-1 and -2, TBB5905-1 and -2, and TBB5910-1 and -2 provide 23k to 256k bytes of nonvolatile memory storage. Each contains 1 or 2 256k- or 512k-bit magnetic bubble memory devices and a controller, and features 85k-bits/s transfer rate. Page size is 34 bytes. Boards measure 7.5 x 13.5" (19.0 x 34.2 cm), with 100-pin edge connectors. Power supplies are 5, 12, and −12 V. Op temp is 0 to 50 °C; nonvolatile data storage temp is −40 to 85 °C. **Texas Instruments Inc,** PO Box 225012, Dallas, TX 75265.

Circle 230 on Inquiry Card

COMPONENTS AND SUBASSEMBLIES

820-nm LED IN PLASTIC FERRULE CASE

Infrared MFOE106F fits directly into AMP fiber optics connector #227240-1, and may be used with MFOD detectors. 700 μW of power are output from a 200-nm dia optical port within a numerical aperture of 0.58. Response time is 12 ns; optical rise and fall times are 120 ns at I_F = 100 mA. Op temp range is −30 to 85 °C, and storage temp range is −30 to 100 °C. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.

Circle 231 on Inquiry Card

75-W OPEN FRAME SWITCHERS

Single-, triple-, or quad-output versions of LMG-75 series have outputs regulated to 0.1% for 92- to 138-Vac, 47- to 440-Hz line input and 0.5% for 0 to 100% load changes. Efficiency is greater than 70% of full load. Ripple and noise are less than 50 mV pk to pk from 50 to 10 Hz. Units meet UL 478 specifications, feature foldback current limiting, and provide 28 ms of holdup protection for line dropout at 115-V line and full load. **Gould Inc, Electronic Power Supply Div,** 4323 Arden Dr, El Monte, CA 91731.

Circle 232 on Inquiry Card

FET INPUT POWER OP AMPS

PA07 and PA07A drive up to ±5 A into resistive and ±1.35 A into inductive loads. Max available output power is 180 W using single power supply into resistive load. Units can operate with dual supplies between ±10 and ±50 V, or single-supplies from 20 to 100 V. Current limit is externally programmable and highly linear output stage is protected against inductive kickback or back EMF. Slew rate is 4.5 V/μs, and gain bandwidth products is 1 MHz. Input offset and input bias current for PA07 and PA07A are given as ±1 and ±0.5 mV and 5 and 3 pA, respectively. **Apex Microtechnology Corp,** 1130 E Pennsylvania St, Tucson, AZ 85714.

Circle 233 on Inquiry Card

FULL KEY TRAVEL INDUCTIVE KEYBOARD

Inductric series keyboards feature reliability, long life, resistance to shock, vibration, dust, liquid contamination, humidity, or temperature extremes, and a proprietary operator adjustable touch control. Design is based on a differential transformer switching module. Etched on both sides of the PCB, coils of the transformer produce canceling signals when pulsed by a drive amplifier. To achieve switching, a ferrite core is moved into a hole in the PCB that is drilled through one pair of coils. Resulting increase in inductive coupling unbalances transformer and sense circuit receives input signal. Keyboard is virtually immune to electrical interference from external source, since key switching and interconnecting matrix operate with low impedance. All encoding is done by 8048 family microprocessors. **Mechanical Enterprises, Inc,** 7 Park Ctr, Sterling, VA 22170.

Circle 234 on Inquiry Card

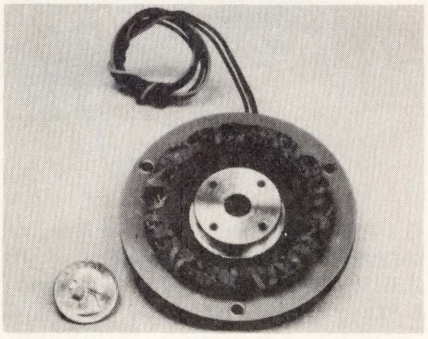
KEYSWITCH AND KEYBOARD ARRAYS

Available in molded monolithic array housings and in discrete versions, KS-200 mechanical keyswitches have twin bifurcated precious metal contacts. Momentary switches have 20M cycle life with 5M cycles for alternate action units. Available arrays range from standard 54- and 63-key layouts, custom multikey units, ancillary arrays of 2 x 1 through 6 x 5 configurations, and standard numeric pads in 11-, 14-, and 18-key formats. Units are molded in one-piece housings, and all arrays and switches can be wave soldered. Each unit is made to user specification. **Stackpole Components Co,** Box M, Farmville, VA 23901.

Circle 235 on Inquiry Card

WINCHESTER DISC DRIVE MOTOR

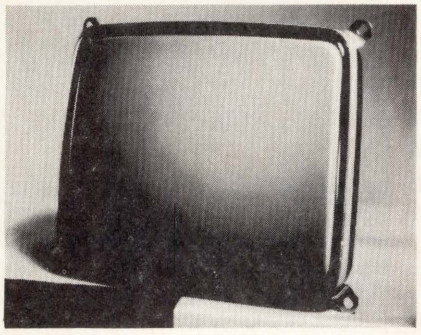
Designed for Winchester disc technology, DB-3500 brushless dc motor will direct drive a disc load from 0 to 3600 r/min in 25 ms and develop up to 30 oz-in (0.210 N·m) reserve torque. Motor uses eight ceramic magnet poles and 3-ϕ wye connected fractional slot armature winding. Units can be furnished as basic rotor/stator sets, with optional commutation encoders, or as complete ready to run drives. Motor weighs 13 oz (364 g), has 3.5″ (8.9-cm) dia and overall height of 0.75″ (1.9 cm). **Clifton Precision,** Marple at Broadway, Clifton Heights, PA 19018.



Circle 236 on Inquiry Card

PRECONVERGED COLOR DISPLAY TUBE

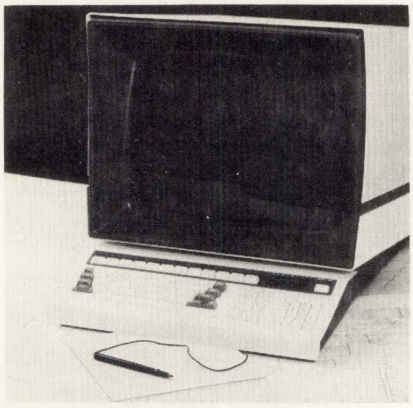
High resolution of 800 pixels/line achieved in the 14″ (35.6-cm) 370KAB22 color display tube is due to the high dot density (2070k dots) and its unitized inline gun with large aperture lens. The self-convergence system features 0.7-mm max misconvergence at any screen location. Black matrix screen offers high contrast. CRT has 90° diagonal deflection, electrostatic focusing, and magnetic deflection and convergence. Overall length is 351.1 ±9.5 mm and neck length is 149.6 ±4.8 mm. **Panasonic Co, Electronic Components Div,** 1 Panasonic Way, Secaucus, NJ 07094.



Circle 237 on Inquiry Card

INPUT/OUTPUT DEVICES

GRAPHICS PROGRAMMING SYSTEM AND TERMINAL



G-CORE, a device independent interactive system compatible with SIGGRAPH/ACM CORE standard, makes use of graphics programs residing in the intelligent GRAPHICUS-80 terminal instead of in the user's host computer. Only ANSI FORTRAN routines containing CORE compatible entry points and message formatting routines to pass user request to the terminal reside in the host. The terminal controller executes user requests, maintains the display file and other data, and controls all graphics devices including its own display. The 1000-line host package is easily learned and convenient to transport to other computers. The GRAPHICUS-80 terminal features high resolution on its 21" (53-cm) display. Features include firmware processor with 32k-byte memory, expandable to 256k bytes; state of the art architecture; and firmware and emulator packages. **Vector Automation**, Village of Cross Keys, Baltimore, MD 21210.

Circle 238 on Inquiry Card

DATA TRANSMISSION TERMINAL

Designed for high speed transmission of IBM format compatible digital magnetic tape data via DDD, WATS, leased, or private line links, the microprocessor based series 7300 is fully compatible with terrestrial and satellite channels provided by domestic and international common carriers. It provides high throughput for both satellite and conventional terrestrial links through use of ARQ procedures and by processing data in large blocks. All formatting, error protocol, modem signaling and tape transport control are directed by a single-chip LSI microprocessor. Built-in self-test validates system operation. The system's tape transport connects to a variety of data terminals via an EIA RS-232-C compatible I/O port with error protecting line protocols. Several levels of database protection are available, from simple character parity to selected repeat ARQ. Error checking is provided on both character and block basis with method and line protocol selected to match user terminal configuration. System can operate unattended in point to point or multipoint networks. **Quad Systems Inc**, 16021 Industrial Dr, Gaithersburg, Md 20760.

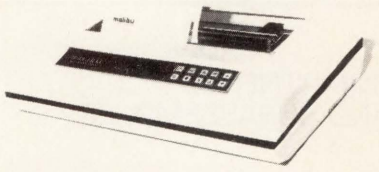
Circle 239 on Inquiry Card

2740/3767 COMPATIBLE CRT DISPLAY TERMINAL

Model 1000 provides 2740 and 3767 users with the convenience of a display in existing or planned networks with no hardware or software modification. Supporting up to 2 printers either as slaves or directly addressable by a host processor, the microprocessor based terminal features a 12" (30-cm) diagonal screen with 23 lines of 80 char. The 24th line is an operator status and diagnostic line. Print-through feature increases data throughput; up to 2 printers may be attached to the display, both addressable directly from the host. Screen formats, operator prompts, and other productivity aids can be created at a central location then downline loaded to terminals and stored locally for access by the operator. Formats can also be stored in the terminal's nonvolatile memory. **Custom Terminals, Inc**, PO Box 19906, Raleigh, NC 27619.

Circle 240 on Inquiry Card

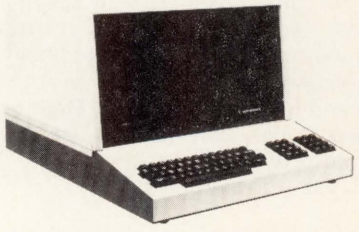
DUAL-MODE MATRIX PRINTER



Designed to serve in data processing as well as word processing applications, model 200 provides enhanced letter quality print mode and associated word processing compatible firmware. Each character font stored in the printer features both a high speed and a reduced speed version. Output speeds range from 165 to 250 char/s in data processing mode and from 42 to 60 char/s in letter quality mode. Two 10-pitch Titan fonts are std; alternate fonts include sans serif, 10-pitch, 12- and 15-char/in (4.7 and 5.9/cm), proportionally spaced, OCR-A, italics, and scientific. The printer can store up to 6 different fonts in ROM, for a total of 12 speed/font options. Touch sensitive front panel gives user control over font selection. LEDs identify fault conditions, and font selection. **Malibu Electronics Corp**, 2301 Townsgate Rd, Westlake Village, CA 91361.

Circle 241 on Inquiry Card

VIDEO DATA TERMINAL



UVT-14 universal video terminal offers 14" (35-cm) diagonal, wide angle CRT screen and green phosphor display characters for minimum eye fatigue. Command functions, such as data entry, data edit and display, preprogrammed function keys, and format protect, promote operator efficiency. Data displays can be made to blink at a defined rate or can be dimmed to attract attention. Up to 16 function keys can be selectively programmed. Information entry is speeded by transmission of data in blocks. Eleven text editing keys provide efficiency in entry or correction of information. Self-test diagnostics are operator activated to reduce maintenance time. **Motorola Inc, Communications Group**, 1301 E Algonquin Rd, Schaumburg, IL 60196.

Circle 242 on Inquiry Card

HIGH RESOLUTION METRIC PRINTER/PLOTTER

Quadramet series metric printer/plotters use the electrostatic Quadrascan writing head to produce a resolution of 100 dots/cm, compared to the conventional 78/cm. The print head contains 4 offset rows of writing styli (compared to the conventional 2). In operation each dot overlaps adjacent dots approximately 50% (compared to the conventional 10%). Model 9424 plots at 2.54 cm/s to a plot width of 59 cm. Model 9436 plots at 1.27 cm/s across an 89-cm plot width. Units output a gothic character font using the 123 ASCII character set. Character generator is a std feature and provides large or small characters. Small characters are 55 mil (1.4 mm) wide, 86 mil (2.2 mm) high, and are spaced 15.8/in (6.2/cm). Large characters are 110 mil (2.8 mm) and 174 mil (4.4 mm), and are printed 7.9/in (3.1/cm). **Benson-Varian, Inc,** 385 Raveldale Dr, Mountain View, CA 94043.

Circle 243 on Inquiry Card

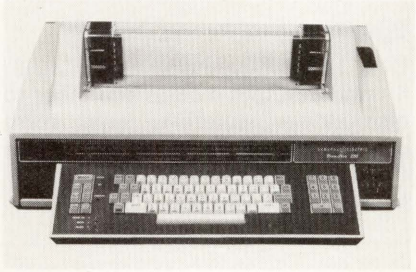
1500-LINE/MIN BAND PRINTER

Built to provide print quality and high reliability at heavy duty cycles, BP-1500 uses an interchangeable steel band, and prints 1500 lines/min with a 48-char set and 1200 lines/min with a 640-char set. Diagnostic and status indicators minimize downtime by providing detailed status on the condition of the microprocessor and system interlocks which control printer operation. Touch sensitive control panel includes built-in self-test unit which features a switch selectable 80- or 132-col multiple pattern program. Built-in sensors indicate paperout as well as paper and ribbon

motion, preventing loss of data and providing for unattended operation. **Dataproducts Corp,** 6200 Canoga Ave, Woodland Hills, CA 91365.

Circle 244 on Inquiry Card

PRINTER LINE ENHANCEMENTS

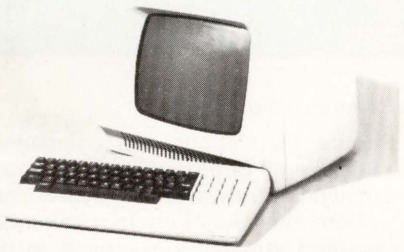


APL/ASCII keyboard layout, 9-wire printhead, and an alternate font are available options for the TermiNet[R] 200 printer line. APL/ASCII allows printing and transmission of APL and ASCII characters. Of the 188 printable characters 94 are for APL and 94 for ASCII. 20 other APL symbols can be created by overstriking. 9-wire printhead enables descenders on 1/c characters and true underlining. Alternate font allows implementation of user-definable character set(s). Options are for use with new models and not for retrofit to older units. **General Electric Co,** Data Communication Products Business Dept, Waynesboro, VA 22980.

Circle 245 on Inquiry Card

SMART TERMINAL

TERMINALSMITH-1, a compact single-board system, displays 1920 char arranged in 24 lines of 80 char on a 30-cm diagonal CRT; a 25th line displays terminal status. Inductive keyswitches are used in the detachable serial keyboard that provides 59 keys with 14-key numeric



keypad, and 12 function keys, each programmable to strings of up to 78 char. Interface is std RS-232-C at 16 rates from 50 to 19,200 baud, programmable from the keyboard. Two interchangeable I/O ports with independent interface characteristics allow simultaneous connections with computer and printer or computer and modem. Basic memory consists of 6k ROM, expandable to 16k; 1k of data RAM; and 1 page of display memory. **Falco Data Products, Inc,** 744 San Antonio Rd, Suite 4, Palo Alto, CA 94303.

Circle 246 on Inquiry Card

HIGH RESOLUTION COLOR GRAPHICS TERMINAL

A modular, interactive computer terminal that gives users full-color raster scan graphics output from the host computer, RM6212 colorgraphic computer terminal offers 8 times the color selection, 25 times the vector writing speed, and more than twice the resolution of the RM-6200A. Interfacing via serial asynchronous communications with any host computer using a std RS-232-C interface, the terminal offers resolution of 640 x 480 picture elements, with an option for 640 x 512 pixels. Four refresh memory planes controlled by a user programmable video lookup table permit display of up to 16 colors selected from 64. Lookup table also allows film loop animation and raster smoothing operations to be performed in software via user programming. **Ramtek Corp**, 2211 Lawson Ln, Santa Clara, CA 95050.

Circle 247 on Inquiry Card

LITERATURE

Peripheral Controllers

Photos, illustrations, and comparison tables are furnished by handbook outlining hardware, software, and system considerations for connecting disc and storage subsystems to DEC computers. **Emulex Corp**, Santa Ana, Calif.

Circle 300 on Inquiry Card

Cable Connectors

Illustrated booklet contains reference charts, configurations, dimensional drawings, and spec tables for components in Scotchflex® cable connector and headboard system. **3M Electronic Products Div**, St Paul, Minn.

Circle 301 on Inquiry Card

Synchros and Servomotors

Catalog describing synchros, servomotors, and precision rotating components lists variety of discrete types, most conforming to MIL-S-20708C. **Muirhead Vactric**, Mountainside, NJ.

Circle 302 on Inquiry Card

Power Supplies

Featuring switcher, linear open frame, and computer power supply models in 1-, 2-, 3-, and 4-outputs, booklet provides dimensional drawings, photos, specs, voltage/current ratings, and expansion module descriptions. **Deltron Inc**, North Wales, Pa.

Circle 303 on Inquiry

Data Communications

Brochure illustrates and describes modems, network diagnostic equipment, time and frequency division multiplexers, and communications products and accessories; system configurations, block diagrams, and operations capabilities are included. **General DataComm Industries, Inc**, Danbury, Conn.

Circle 304 on Inquiry Card

Distributed Control System

Brochure presents microprocessor based distributed control system, Network 90,™ describing modular design and system architecture with photos, graphs, and block diagrams. **Bailey Controls Co**, Wickliffe, Ohio.

Circle 305 on Inquiry Card

Cooling Equipment

Design guide features dimensional drawings, performance nomograms, and standard accessories specs for blowers, fans, heat exchangers, and air conditioners; also included is guide for cooling equipment in hostile environments. **Kooltronic, Inc**, Hopewell, NJ.

Circle 306 on Inquiry Card

Analog IC Designs

Fundamental circuits that can be combined to create complex linear ICs are detailed in booklet containing graphs, block diagrams, electrical specs, and Monochip component listings. **Interdesign Inc**, Sunnyvale, Calif.

Circle 307 on Inquiry Card

Open Frame dc Power Supplies

Over 100 types, including 1-, 2-, 3-, 4-, and 5-output models and those for disc drives, printers, and microprocessors are described in catalog. **Condor, Inc**, Camarillo, Calif.

Circle 308 on Inquiry Card

Long Distance Modem

Booklet presents features of high speed SM9600 superModem, along with photos, specs, performance graphs, and block diagrams. **Gandalf Data, Inc**, Wheeling, Ill.

Circle 309 on Inquiry Card

7-Segment Displays

Detailed explanation of large 7-segment and monolithic LED displays includes mechanical construction techniques, character heights, and typical application areas in note that presents extensive set of tables. **Hewlett-Packard Co**, Palo Alto, Calif.

Circle 310 on Inquiry Card

IC Memories

Data sheets, cross-reference, and section on packaging, reliability, testing, P/ROM programming and erasing, and support circuits make up 180-p catalog. Request literature No HLN100 in writing from **Electronic Devices Sales and Service Div, Hitachi America, Ltd**, 1800 Bering Dr, San Jose CA 95112.

Subminiature Switches

Catalog describes TINYSWITCH series for PC and panel mounting as well as related front panel components applicable to instrumentation, computer, and telecommunications industries. **Alco Electronic Products, Inc**, North Andover, Mass.

Circle 311 on Inquiry Card

Test Equipment

Over 50 industrial test instruments for research, development, field maintenance, and production are described in catalog providing photos, specs, and applications information. **B&K Precision/Dynascan Corp**, Chicago, Ill.

Circle 312 on Inquiry Card

Noise Suppressor

Manual on protection of sensitive equipment from ac line noise, transients, and spikes offers typ applications, Ultra-Isolator® performance graphs, block diagrams, and noise attenuation table. **Topaz, Inc, Electronics Div**, San Diego, Calif.

Circle 313 on Inquiry Card

Rotary Switches

Catalog supplies construction details, schematics, dimensions, application engineering data, and switch spec reference chart for microminiature, subminiature, miniature, heavy duty, and power switches. **Centralab, Inc**, Milwaukee, Wis.

Circle 314 on Inquiry Card

Analog to Digital Converter

Performance and system configuration tables, specs, and interfacing information profile GM series conversion systems in pamphlet illustrated with block diagrams and product photos. **Preston Scientific, Inc**, Anaheim, Calif.

Circle 315 on Inquiry Card

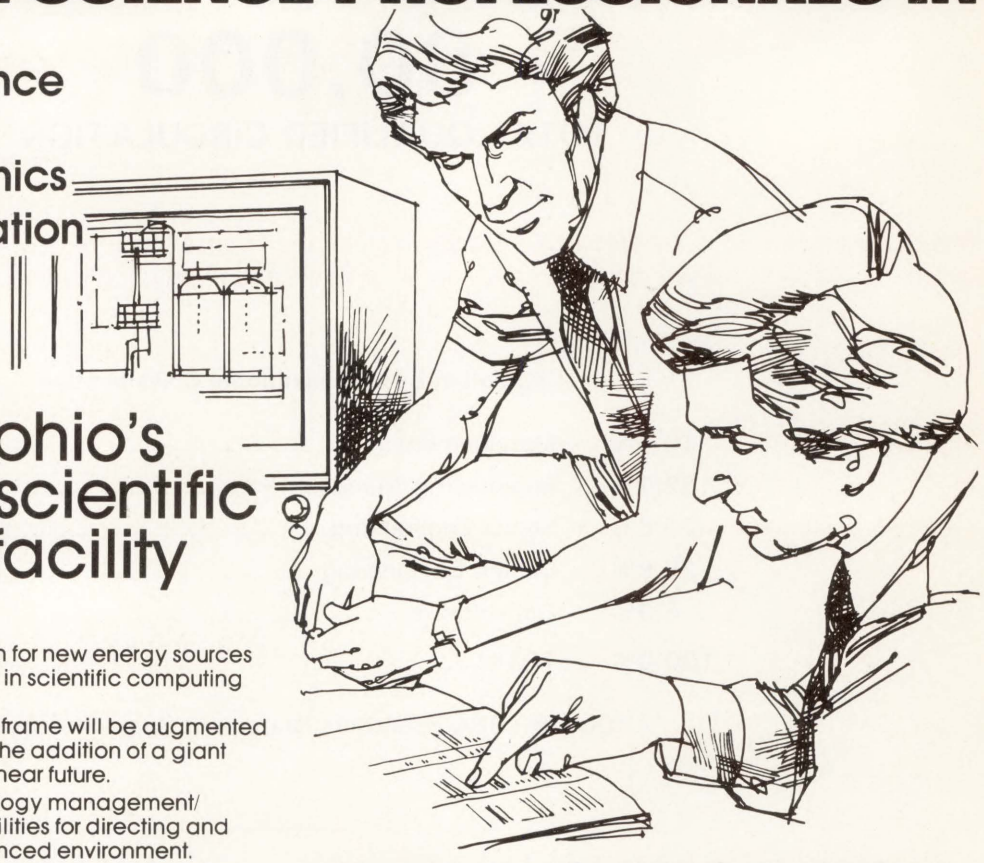
Power Conversion

Handbook lists electrical and mechanical parameters of ac-dc and dc-dc power supplies, detailing specs and case, pin, and socket configurations. **Power General**, Canton, Mass.

Circle 316 on Inquiry Card

COMPUTER SCIENCE PROFESSIONALS IN

- Cyber Performance Monitoring
- Computer Graphics
- Hardware Evaluation Analysis



Grow with Sohio's expanding scientific computing facility

Our rapid expansion in the search for new energy sources has resulted in an explosive growth in scientific computing requirements.

The present CDC Cyber 175 main frame will be augmented with a Cyber 760 by late 1980 and the addition of a giant vector processor is planned for the near future.

Check the following high technology management/ monitoring positions with responsibilities for directing and controlling this dynamic and advanced environment. If your career experience matches our needs, we should discuss the possibilities.

Cyber Computer Performance Monitoring Analyst

You have demonstrated work experience in a measurement and analysis program for a large main frame. Experience with a Cyber 175 and/or 760 would be a definite plus. Typical responsibilities:

- Directing a major program for on-going measurement and analysis of Cyber performance.
- Developing early warning detection procedures for eliminating capacity/bottleneck problems relating to central and peripheral processors, storage devices, communication channels.
- Planning for Cyber disruption recovery, contingency off-loading and computer security.

Computer Graphics Specialist

Your strong professional background, including 4-5 years proven experience with a variety of computer graphics terminals and software (petroleum engineering or exploration related a plus) should have prepared you for this key graphics product manager opportunity.

- You will lead a task force which will determine SOHIO's present and longer range graphics requirements – then develop hardware/software acquisition plans to support these requirements.
- You will assume complete resonsibility for the support of a rapidly expanding graphics products library for our CDC Cyber computer.
- You will provide on-going consulting support on all major graphics applications in SOHIO.

Hardware Evaluation Analyst

To meet the challenges of this position, you should have 2+ years hardware evaluation experience in a main frame environment – and have demonstrated the ability to work independently and follow through with successful hardware acquisitions and installations. We prefer that you have your M.S. in Computer Science, Electronics or related technical area. Your involvement with SOHIO:

- Active participation in the expansion of our scientific computing facility through evaluation of the economics involved and feasibility of the latest in CDC main frame hardware products.
- Provide direction for the acquisition of a wide variety of peripheral equipment – remote-batch and time sharing terminals, storage and sophisticated high-speed plotting devices, and communication equipment – all part of a nationwide distribution network.
- Take responsibility for recommending appropriate main frame and peripheral hardware configurations.

Attractive salaries, generous benefits and advancement possibilities complement these highly responsible positions. **SOHIO's relocation package for qualified new hires includes a mortgage interest differential allowance, third party home purchase option and other features normally restricted to internal transfers.** There's no better time than NOW to JOIN SOHIO! For immediate confidential consideration send your resume and current salary to:

Ms. Sarah Steiner, Executive Recruitment

THE STANDARD OIL COMPANY (Ohio)

1424 Midland Building - 150 • Cleveland, Ohio 44115

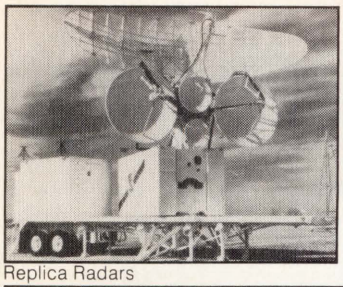
An Equal Opportunity Employer M/F

"Help us Help to Assure America's Energy Future"

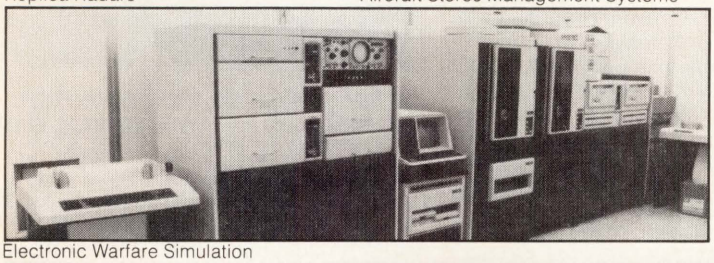
SOHIO

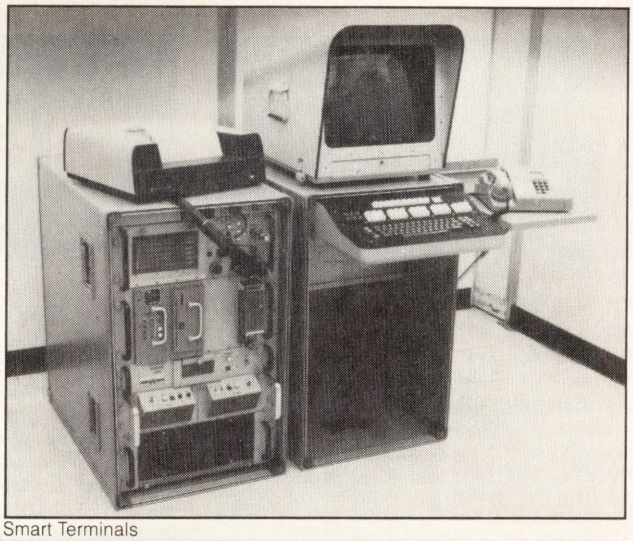
CIRCLE 121 ON INQUIRY CARD

ELECTRONICS ENGINEERS:


Replica Radars


Aircraft Stores Management Systems


Electronic Warfare Simulation


Smart Terminals


Intelligence Systems


C^3 Systems

The F-16. It's just one side of General Dynamics Fort Worth.

You probably know that we have designed and are building the F-16 fighter for the air forces of the United States and its allies, but what you may not know is that we're also a growing, diversified electronics operation. We're currently designing some of the world's most advanced radar simulation systems and command and control systems, in addition to other ongoing projects like airborne stores management systems and replica radars.

We're looking for people who like to see their projects grow from concept through integration and checkout. We need engineers with a minimum of a B.S. in Electrical or Electronics Engineering or Computer Science and with the following backgrounds:

- **Systems Engineering**
- **C^3I Systems**
- **Communications Systems**
- **Computer Systems**
- **Simulation Systems**
- **Radar Systems**
- **Display Systems**
- **Software Development**
- **Digital Circuit Design**
- **RF Circuit Design**
- **Electronic Packaging**
- **Electronic Warfare**

If you qualify and are interested in a career in advanced electronics, send us your resume. We're offering outstanding opportunities with unique potential for advancement.

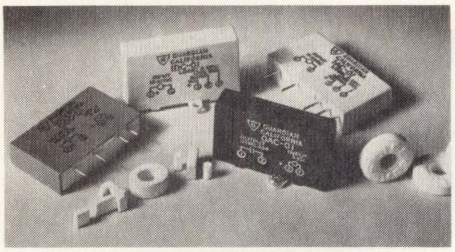
You'll also receive an excellent salary with exceptional benefits, including a savings/stock investment plan, life/medical insurance, dental plan, and access to an 80-acre recreational area and 18-hole golf course for employee/family use.

Send your resume to R.Q. Lee, Director of Electronic Systems and Laboratories, P. O. Box 748-21EE, Mail Zone 1862, Fort Worth, Texas 76101.

GENERAL DYNAMICS

Fort Worth Division

U.S. Citizenship Required. An equal opportunity employer M/F.



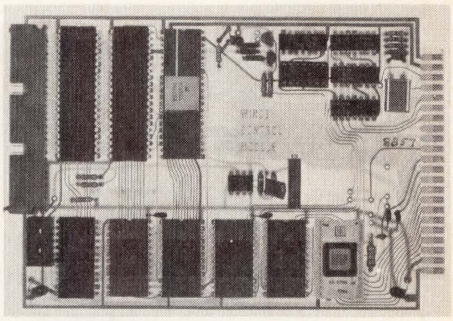
NEW GUARDIAN I/O MODULES CUT SPACE BY 40% With .68in.² footprints and .68in.³ volume (vs.1.02in.² and 1.25in.³ for other makes), Guardian's I/O Modules offer more than 1/3 higher stacking density. Tops are clean, allowing their use for customer markings. Input devices operate from 12-140VAC & 3-120Vdc into 5, 15 or 24Vdc outputs. The 20-280VAC & 60Vdc/2.5A Output Modules have 5, 15 or 24Vdc inputs. Easily removed breakaway screw-mount tab. **GUARDIAN CALIFORNIA** 4030 W. Spencer St., Torrance, CA 90503. 213-542-8651. Duane Heft.

CIRCLE 533

STD BUS?

*Prom Programmer: Software controlled 25v generated from bus 12v static or dynamic RAM, I/O or memory mapped, Z-80, 808X, 680X. Only $165 with software listings. *Floppy Disc Controller: New chip set from WD includes PLL data separation DMA, single/double density 5/8" software selectable. Only $440 with I/O drivers for 8080/Z-80 6800; with CP/M2.2 or FLEX add $250. *CP/M2.2 for MOSTEK MD-FLP. Only $350. **INTELLIGENCE SYSTEMS LTD.,** 124 So. Delaware St., Indianapolis, IN 46204 (317) 631-5514.

CIRCLE 534

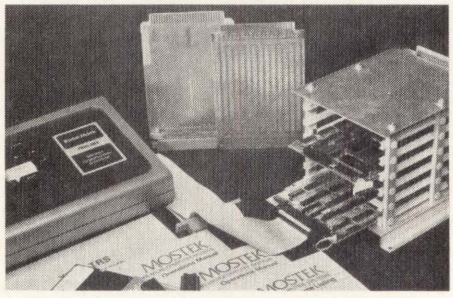


$94.20* SINGLE BOARD COMPUTER 6800 MPU, serial I/O, parallel I/O, RAM, EROM, 44-pin 4½" x 6½" PCB.

EXPANSION MODULES

RAM, ROM, CMOS RAM/battery, analog I/O, serial I/O, parallel I/O, counter/timer, 488 GPIB, EROM programmer, power fail detect/power on reset. *100 piece price, model MCL11. **WINTEK CORP.,** 1801 South Street, Lafayette, IN 47904; 317-742-8428.

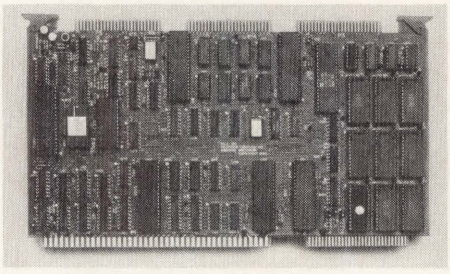
CIRCLE 535



STD BUS PROTOTYPE PACKAGE The TRS-PROTO Package permits STD BUS Z80 Systems to be developed using a TRS-80 for all editing, assembling, and bulk storage. It includes the Mostek CPU2 card and Debug O.S., and is available for $895 as shown ($1050 for 4.0 MHz). A full catalog of STD BUS products from Mostek and other manufacturers is also available.

Contact **QC MICROSYSTEMS,** 9861 Chartwell Dr., Dallas, TX 75243, (214) 343-1282.

CIRCLE 536



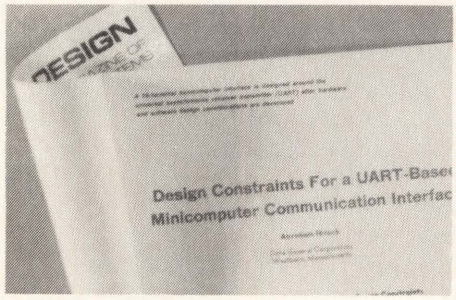
MICROCOMPUTER WITH MORE Heurikon MLZ-90A micro sports Z80A CPU, on-card floppy controller, DMA, 73K on-card addressable memory, 20 bit multibus compatibility, memory mapping RAM, AM9511, four 8 bit ports, four counter/timers, two RS232 ports, dual baud rate generator and XTAL, jumper selectable wait states, and monitor with CP/M bootstrap.

HEURIKON CORPORATION, 3001 Latham Drive, Madison, Wisconsin 53713 (608) 271-8700

CIRCLE 537

RECTIFIER BRIDGES New integral heat sink provides better heat transfer for higher current ratings at lower cost. UP 150 Series: 50A.; 1,000 A. surge; up to 600 PRV. **FREE SAMPLES** Outline your application on company stationery for free test samples. Use reader service number for catalogs and prices. Buy from the specialist. **EDI ELECTRONIC DEVICES** 21 Gray Oaks Ave., Yonkers, N.Y. 10710. (914) 965-4400. TWX 710 560-0021.

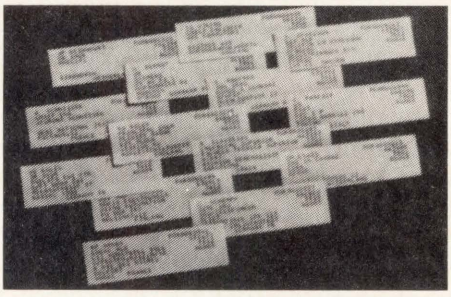
CIRCLE 538



ARTICLE REPRINTS Have you or a member of your company authored an article in COMPUTER DESIGN? If you want to distribute it to your customers and prospects, reprints are available at reasonable cost. Minimum quantity is 500. You can incorporate the CD cover as well as your company ad if you wish, in b&w or full color.

Contact **COMPUTER DESIGN REPRINTS,** 11 Goldsmith Street, Littleton, MA 01460. (617) 486-8944.

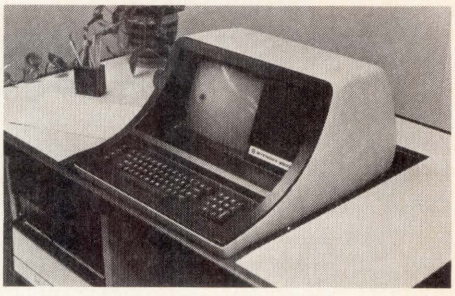
CIRCLE 539



PRODUCT-SPECIFIER MAILING LISTS If you want to evaluate a product or the market for it, why not send a questionnaire to the computer-based systems designers who will specify or approve it for purchase. We can provide the precise direct mail lists you need. You can choose by nature of design work, nature of organization, products specified, geographical area, etc.

COMPUTER DESIGN DIRECT MAIL LISTS 11 Goldsmith Street, Littleton, MA 01460 (617) 486-8944.

CIRCLE 540



SERIES 500: LOW-COST, ENTRY-LEVEL COMPUTER SYSTEM comprising 16-Bit CPU, RTC, 64KB memory, disc controller, printer controller (parallel/serial) and CRT logic. Packaged on single board within video terminal (24-line, 80-character). Asynchronous port for second CRT. Runs under IRIS, BITS, IOS, BUS/COBOL operating systems. **BYTRONIX,** 2701 E. Chapman, Fullerton, CA 92631. (714) 871-8763.

CIRCLE 541

ADVERTISERS' INDEX

CD SALES OFFICES

HOME OFFICE

V.P., Marketing
Ronald W. Evans

Direct Marketing Sales Mgr
Maureen Sebastian

Classified Advertising Mgr
John G. French

11 Goldsmith St.
Littleton, MA 01640
(617) 486-8944

NEW ENGLAND AND UPSTATE NEW YORK

Regional Sales Manager
Gene Pritchard
11 Goldsmith St.
Littleton, MA 01460
(617) 486-8944

LONG ISLAND AND MIDDLE ATLANTIC STATES

DICK BUSCH, INC
Richard V. Busch
6 Douglass Dr., R.D. #4
Princeton, N.J. 08540
(201) 329-2424

SOUTHEASTERN STATES

DICK BUSCH, INC
Richard V. Busch
6 Douglass Dr., R.D. #4
Princeton, N.J. 08540
(201) 329-2424

MIDWESTERN STATES

BERRY CONNERS ASSOCIATES
Berry Conner, Jr.
88 West Schiller St.
Suite 2208
Chicago, IL 60610
(312) 266-0008

WESTERN STATES AND TEXAS

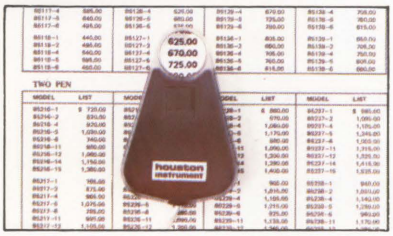
BUCKLEY/BORIS ASSOC., INC.
Terry Buckley
Tom Boris
Rich Molden
22136 Clarendon St.
Woodland Hills, CA 91367
(213) 999-5721
(714) 957-2552

In this age of runaway inflation...

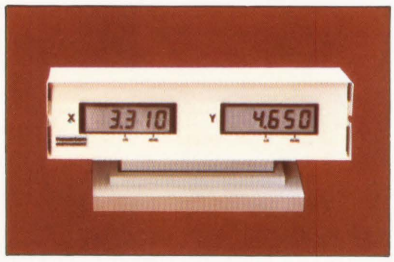
Look what $795* will buy

The HIPAD™ digitizer

The ideal input device for the small system user.



Available with stylus or optional cursor.



Available with optional display.

*U.S. Suggested retail price

Inexpensive input to your computer

The HIPAD™ digitizer can be used for both converting graphic information into digital values and as a menu. Utilizing either the stylus or the optional cursor, the operator can input graphic data into the computer by locating individual points on the digtizers 11″ × 11″ (28cm × 28cm) active area. In the "stream mode" a continuance of placements of coordinate pairs may be input.

Not a kit, the HIPAD™ comes complete with both RS-232C and parallel interfaces and has its own built-in power source. The origin is completely relocatable so coordinates may be positive or negative for a true reference value and oversized material may be input by simply resetting the origin.

Accurate positional information, free form sketches, even keyboard simulation

All can be entered using the multi-faceted HIPAD™ digitizer. Its capabilities and low price make the UL listed HIPAD™ a natural selection over keyboard entry, inaccurate joysticks, or expensive approximating light pens. It's perfect for inputting isometric drawings, schematics, X-rays, architectural drawings, business graphs, and many other forms of graphic information, as well as creating your own graphics.

Use it with Apple II™, TRS-80 Level II™, PET™ or other popular computers

The HIPAD's™ built-in RS-232C and parallel 8 bit interfaces make it all possible. (For Apple II order DT-11A, for TRS-80 or PET order DT-11). Furthermore, you get English or metric scaling, data format (Binary/BCD/ASCII), selectable baud rates, and resolution of either .005″ or .01″.

For complete information contact Houston Instrument, One Houston Square, Austin, Texas 78753. (512)837-2820. For rush literature requests, outside Texas call toll free 1-800-531-5205. For technical information ask for operator #5. In Europe contact Houston Instrument, Rochesterlaan 6, 8240 Gistel, Belgium. Telephone 059/27-74-45.

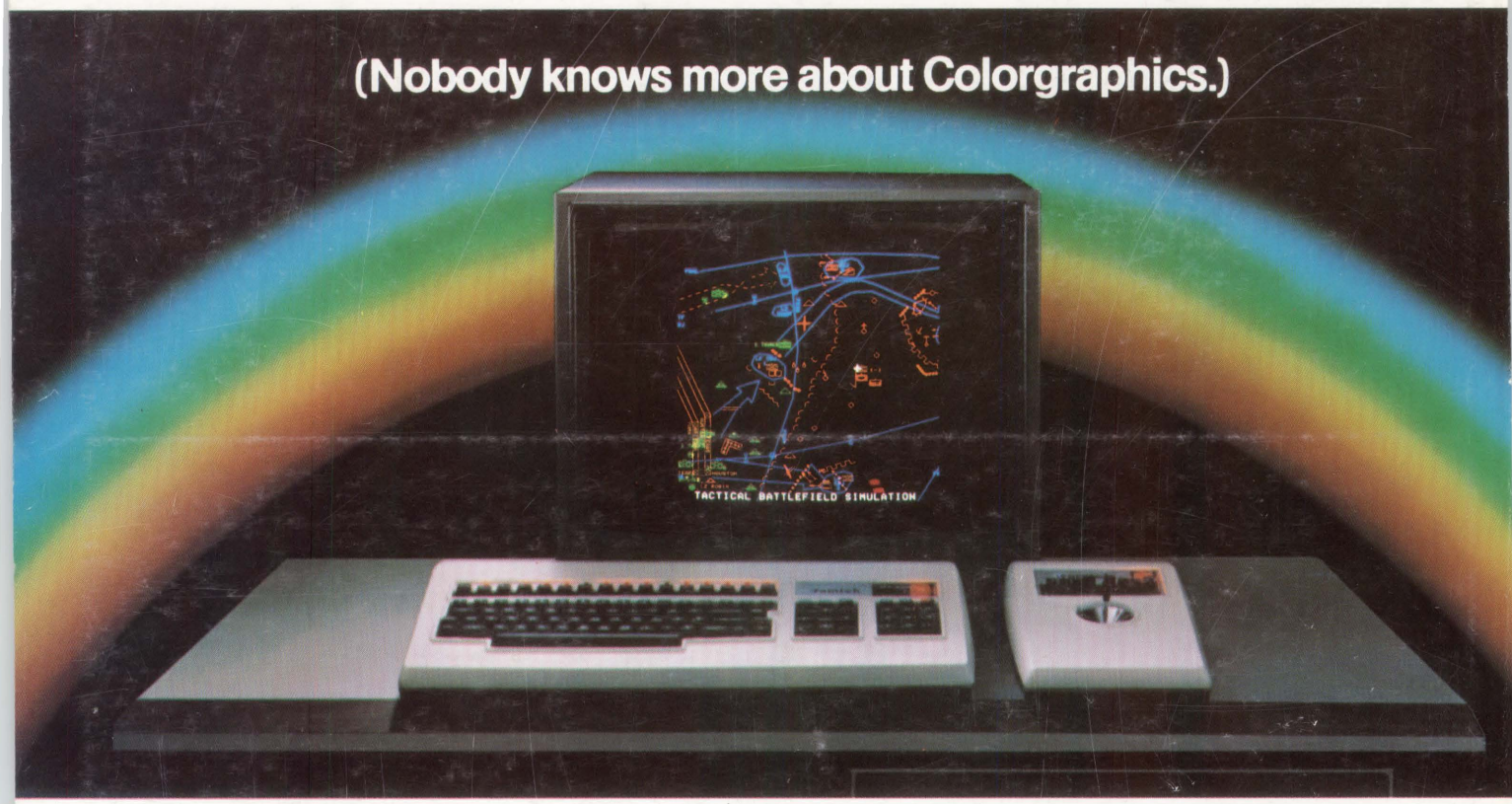
houston instrument
GRAPHICS DIVISION OF
BAUSCH & LOMB

Circle Number 125 for Literature.

Circle 126 to Have a Representative Call.

Ask Ramtek.

(Nobody knows more about Colorgraphics.)



How can a graphics display system save software development time?

By giving you everything you need to start applications programming.

The Ramtek 9400 puts you in the picture fast. We've already solved your graphics problems in the 9400 so you can get your application on line without waiting for—or spending money on—needless systems software development.

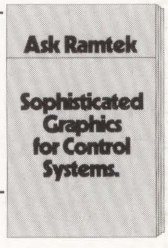
The 9400 puts you in total control. Monitor the situation in real time. Reduce an extremely large or complex picture for a quick look or enlarge portions of it for a closer one without distorting line thickness, texture or character size. At the same time, the 9400 automatically displays the appropriate detail so the picture is always clearly understood.

Need to interact with the picture? Our exclusive entity detection feature lets you identify objects that are pointed out on the screen. Whether a single line or a complex object, let the 9400 find and identify them to the host computer.

Need high resolution or fast response? The 9400 offers a wide range of resolutions up to 1280 X 1024 picture elements in full color. System throughput of over 16,000 vectors per second permits multi-channel operation without sacrificing response time. The bright TV-like picture makes it easy to use in normal room lighting.

For more information on the 9400 and Ramtek monitors and accessories, write: Ramtek, 2211 Lawson Lane, Santa Clara, CA 95050. Or call your nearest Ramtek office.

How much can graphics do?
To find out more about the power of full color interactive graphics, request the booklet "Sophisticated Graphics for Control Systems." It's Issue Number 3 of Ramtek's "USE OUR EXPERIENCE" Series.



Ramtek

Our Experience Shows.

REGIONAL OFFICES: Santa Clara, CA (408) 988-2211, Newport Beach, CA (714) 979-5351, Seattle, WA (206) 838-5196, Albuquerque, NM (505) 884-3557, Dallas, TX (214) 422-2200, Maitland, FL (305) 645-0780, Huntsville, AL (205) 837-7000, Chicago, IL (312) 397-2279, Cleveland, OH (216) 464-4053, Washington, DC (301) 656-0350, Metropolitan NY (201) 238-2090, Boston, MA (617) 273-4590, The Netherlands 31 2968 5056.

CIRCLE 127 ON INQUIRY CARD