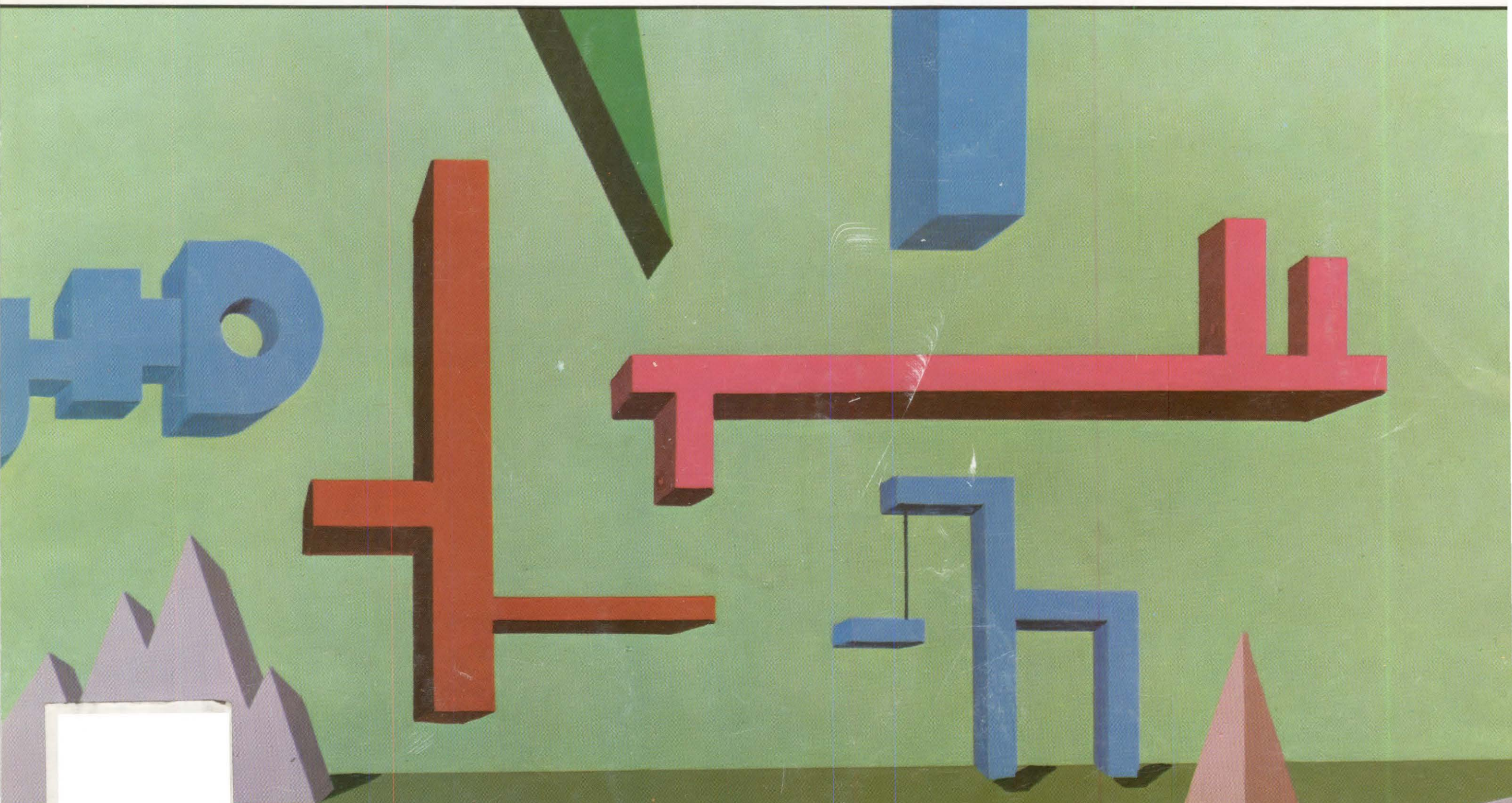
COMPUTER DESIGN

THE MAGAZINE OF COMPUTER-BASED SYSTEMS

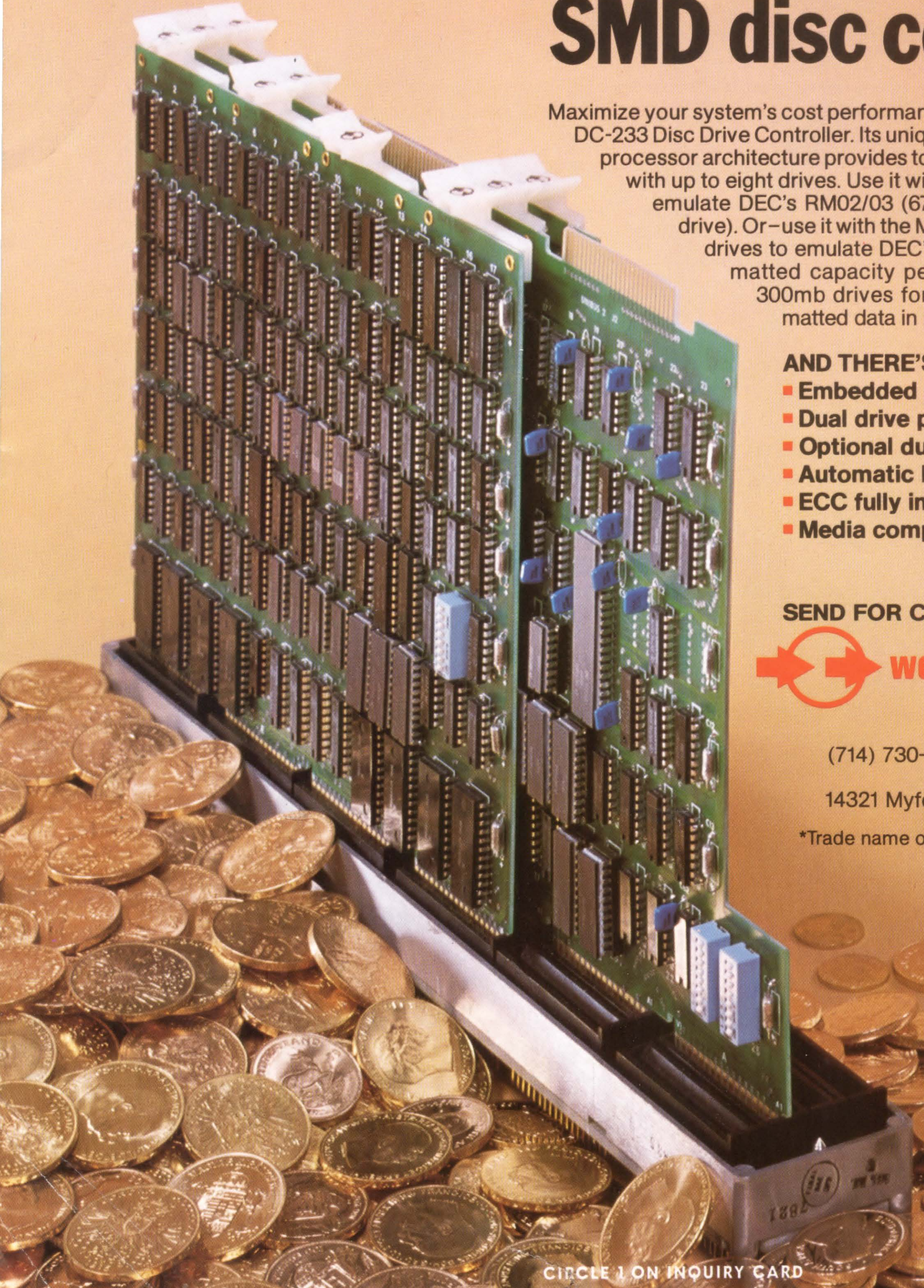
APRIL 1980



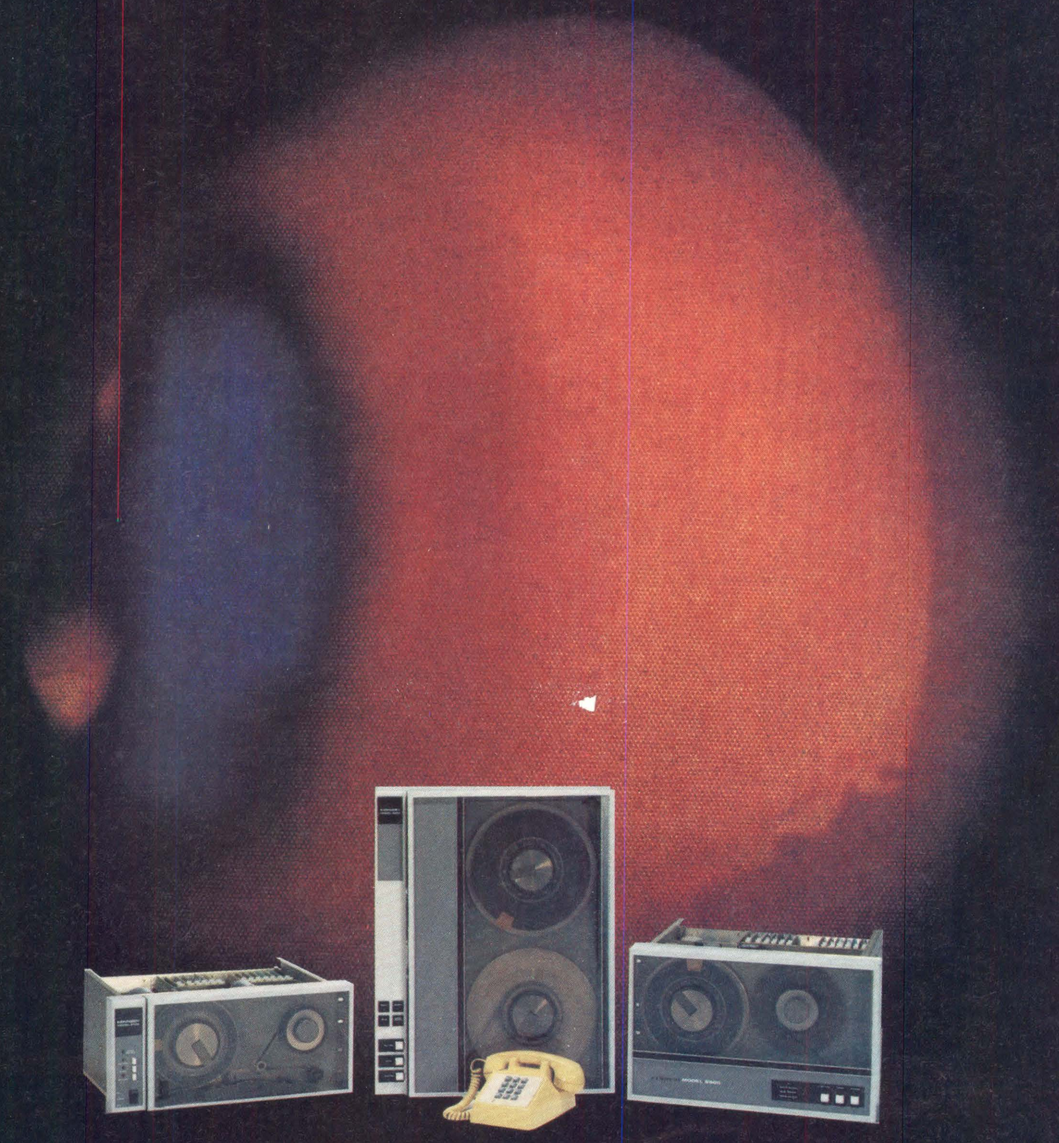
HYBRID TOOL FOR UNIVERSAL MICROPROCESSOR DEVELOPMENT

COMPONENT-BY-COMPONENT TESTING OF DIGITAL CIRCUIT BOARDS

FIELD PROGRAMMABLE LOGIC REPLACES HARDWIRED CIRCUITS WITH MICROCODE



We take calls from Venus...



and Mars, Sweden, Switzerland, Norway, Brazil, Great Britain...

and virtually every other country on Earth. Kennedy Company and its digital tape products were pioneers in such demanding applications as telephone toll-ticketing, usage analysis, message switching control and electronic switching systems.

These years of reliable operation are one of the reasons NASA installations throughout the world utilize Kennedy tape recorders to telemetrically record and digitally reproduce such significant data and photographs from the Viking, Pioneer and Voyager probes of Mars, Venus and Jupiter.

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Photo courtesy of NASA and
Jet Propulsion Laboratory, Pasadena, CA

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CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER-BASED SYSTEMS

APRIL 1980

VOLUME 19, NUMBER 4

FEATURES

CONFERENCES

DEPARTMENTS

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STAFF

Editorial & Executive Offices
11 Goldsmith St
Littleton, MA 01460
Tel. (617) 486-8944
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ADD-ON MEMORY (KBYTES) PLANNED FOR PURCHASE IN 1979/80

SUPPLIER	UNITS TO BE PURCHASED	% SHARE
Digital Equipment	56,650	10.7
CDC	45,228	8.5
Hewlett-Packard	38,756	7.3
Dataram	25,688	4.8
Plessey	23,808	4.5
Data General	15,104	2.8
Prime	13,455	2.5
Mostek	11,276	2.1
IBM	8,308	1.6
Ampex	7,936	1.5
Four Phase	7,138	1.3
Perkin Elmer	7,044	1.3
Texas Instruments	5,533	1.0
Intel	3,568	0.7
Honeywell	3,450	0.7
Other/Unspecified	258,278	48.7
Totals: 1979/80	531,220	100.0

DATAMATION MAGAZINE ASKED* 44,000 MINI USERS AROUND THE WORLD ABOUT ADD-ON MEMORY. THEY NAMED DATARAM OVER ALL OTHER INDEPENDENT SUPPLIERS.

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*Datamation's 1979/80 Mini-Microcomputer Survey.

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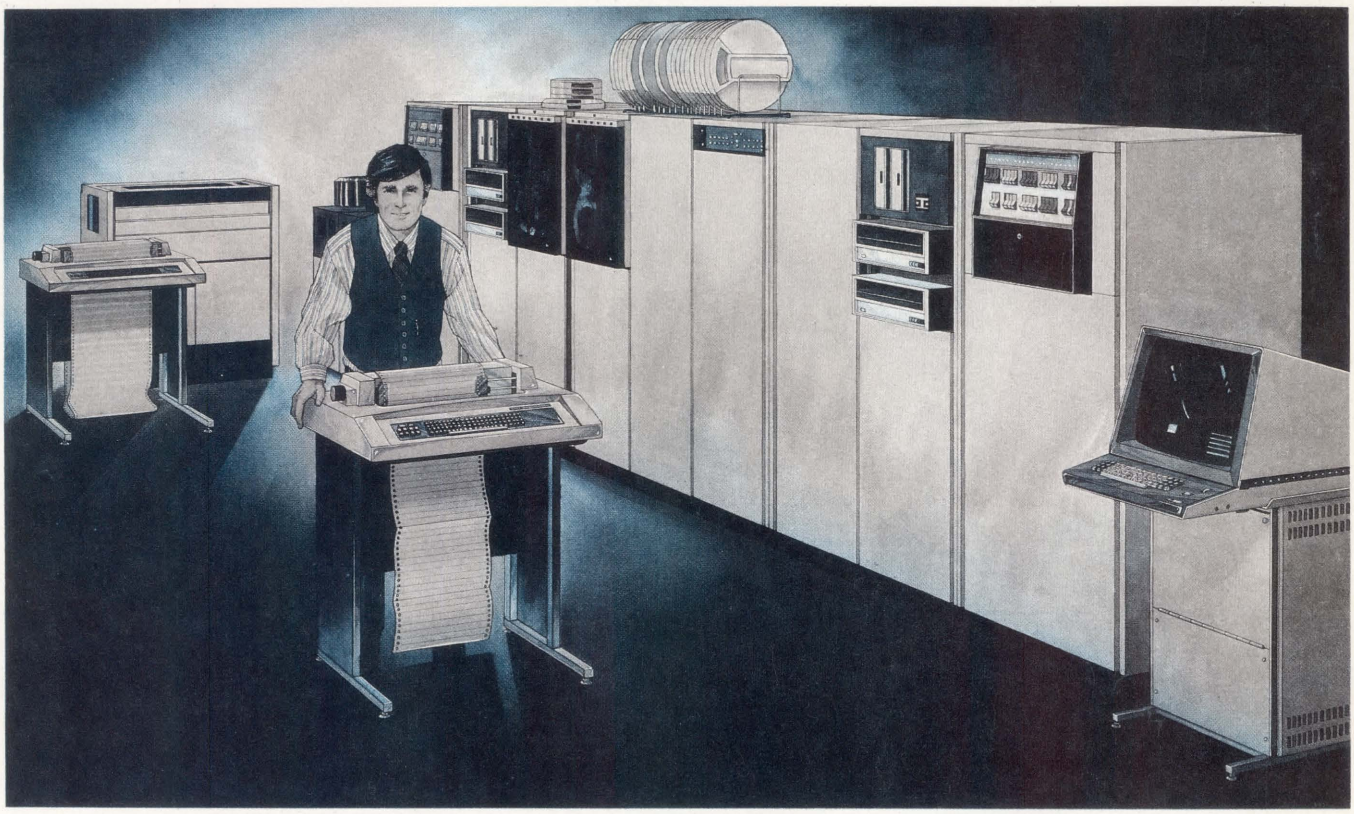

LETTERS TO THE EDITOR

To the Editor:

In reference to Gene Hnatek's article "Semiconductor Memory Update—Part 2: RAMs," in your January 1980 issue (pp 119-131), it looks as though the author did not do a very thorough job in delving into our available products.

On page 131 the author mentions sapphire ribbon technology and square wafer processing. While we look to square wafers in the future, we are not processing that way yet.

Mr Hnatek goes on to indicate that only one part, MWS5114, is an SOS RAM. In fact, if he had referred to our databook, SSD-260, he would have found three other SOS devices. He also indicates on page 130 that we have only two types in our total line of CMOS RAMs. We not only have four SOS types but also four bulk types.

The chart also indicates a 4k x 4 RAM that really is not yet available.

Walter B. Dennen
RCA Solid State Div
Somerville, NJ

Letters to the Editor should be addressed:

Editor, Computer Design
11 Goldsmith St
Littleton, MA 01460

CORRECTION

Please note the following corrections to the Communication Task Program, p 116, of Y. P. Chien's article "Multitasking Executive Simplifies Realtime Microprocessor System Design" (January 1980). Line 6 from the top should read EVG EQU 1 ;Event Flag 1 for receive channel. The seventh line should read ETG EQU 2 ;Event Flag 2 for time-out.

Xerox just gave us the opportunity of the century. And we couldn't be happier.

We're part of Xerox. Diablo Systems, Inc. is, too. And they've got plans for both of us.

Diablo will concentrate on printers. Century will concentrate on disk drives. Makes sense. And it means we now have full responsibility for sales and marketing of the Diablo disk drive product line.

The big winner in this exchange is you, the customer.

If you're a Series 30 customer, count on us for eager-to-please support and a dependable source of supply for years to come.

If you've evaluated the Series 44B and think it is as good a 5440-type drive as we think it is, you're about to see us rewrite the book on enthusiastic marketing and conscientious support.

And if you need spares for Series 10, 20 and 44A Diablo drives, we're pledged to keep you smiling, too.

Here are the specific actions we're taking.

FAST ANSWERS. The man's name is Howard Wing. He's our Diablo Team Captain. His phone number is 714/632-7500. Answers he doesn't have, he'll get. Fast. Think of Howard as your single point of responsibility for Diablo drives from Century.

FAST DELIVERY. We call it our Distribution Center. It's designed to provide off-the-shelf delivery of new orders, spares and critical components, such as spindles. We're building inventories to meet your needs. And even though we're months away from eliminating backlogs, we wouldn't put it in black and white if we weren't committed to it.

SUPPORT, SUPPORT, SUPPORT. Complete Century Data documentation on our Diablo product line is available now. We're conducting Diablo-drive training seminars for our sales force. We've worked out details with Diablo (the company) to ensure continuing quality service for Diablo drives.

In short, we're doing all we can to make Diablo drives from Century the drives you can't resist. We've sunk our teeth into this opportunity. And won't let go.

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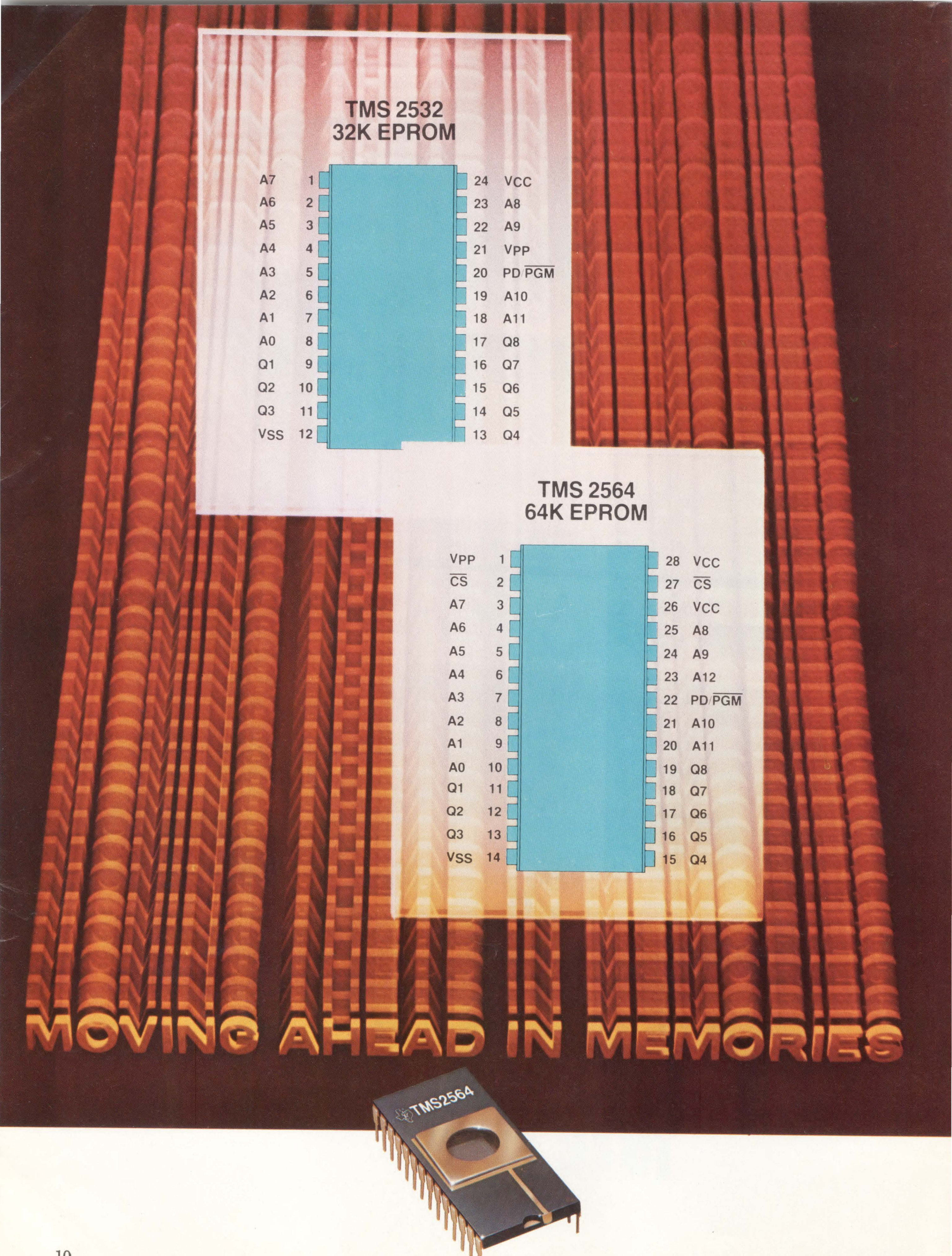
TMS 2532
32K EPROM
A7 1 | 24 VCC
A6 2 | 23 A8
A5 3 | 22 A9
A4 4 | 21 VPP
A3 5 | 20 PD/$\overline{PGM}$
A2 6 | 19 A10
A1 7 | 18 A11
A0 8 | 17 Q8
Q1 9 | 16 Q7
Q2 10 | 15 Q6
Q3 11 | 14 Q5
VSS 12 | 13 Q4
TMS 2564
64K EPROM
VPP 1 | 28 VCC
$\overline{CS}$ 2 | 27 $\overline{CS}$
A7 3 | 26 VCC
A6 4 | 25 A8
A5 5 | 24 A9
A4 6 | 23 A12
A3 7 | 22 PD/$\overline{PGM}$
A2 8 | 21 A10
A1 9 | 20 A11
A0 10 | 19 Q8
Q1 11 | 18 Q7
Q2 12 | 17 Q6
Q3 13 | 16 Q5
VSS 14 | 15 Q4
MOVING AHEAD IN MEMORIES
TMS2564

8Ks, 16Ks, 32Ks, and now...

The first 64K EPROM. From Texas Instruments. Naturally.

Introducing the TMS2564. The industry's first 64K EPROM. The densest yet. With all the high-performance features of TI's 5-V EPROM family. Features like 8-bit word configuration, fully static operation, automatic chip-select/power down, and low-power.

Pin compatibility

TMS2564 is offered in a 600-mil, 28-pin dual-in-line package. But, it's compatible with industry standard 24-pin 64K ROMs, as well as less dense EPROMS.

This is because pins 3 through 26 of the TMS2564 are compatible with pins 1 through 24 of the 24-pin devices. Compatibility is enhanced by reserving both pins 26 and 28 for the 5-V supply. So, with a supply trace to pin 26, both 24 and 28-pin devices can be used, with no jumpering.

Fully static

Like all TI EPROMS, the TMS2564 maintains the fully static tradition that makes designing easier.

No timing signals. No clocks. No strobes. No refresh. No problems. Simply, cycle time equals access time.

Lowest power ever

Operating at an access time of 450 ns with a power dissipation of only 840 mW maximum or less than 13 μW per bit, it's the lowest power per bit ever achieved in EPROMS.

TI'S GROWING EPROM FAMILY

Device	Description	Power Supply	Max Power (0°C) Operating	Standby	Access Time
TMS2564	64K	5 V	840 mW	131 mW	450 ns
TMS25L32	32K	5 V	500 mW	131 mW	450 ns
TMS2532	32K	5 V	840 mW	131 mW	450 ns
TMS2516-35	16K	5 V	525 mW	131 mW	350 ns
TMS2516	16K	5 V	525 mW	131 mW	450 ns
TMS2508-25	8K	5 V	446 mW	131 mW	250 ns
TMS2508-30	8K	5 V	446 mW	131 mW	300 ns
TMS2716	16K	+12, ±5 V	720 mW	—	450 ns
TMS27L08	8K	+12, ±5 V	580 mW	—	450 ns
TMS2708	8K	+12, ±5 V	800 mW*	—	450 ns
TMS2708-35	8K	+12, ±5 V	800 mW*	—	350 ns

*$T_A = 70°C$

Easy programming

The TMS2564 is designed to facilitate rapid program changes in high density, fixed memory applications.

All that's needed for simple, in-system programming, is a single TTL level pulse.

You can program in any order. Individually. In blocks. At random. So, programming time is reduced to a minimum. And, you can use existing 5-V PROM programmers.

Erasing? Simple ultraviolet. Just like any other EPROM.

Widest choice

By adding the new TMS2564 to our fast-growing EPROM family, we offer the designer a product breadth unmatched by any other supplier.

All TI EPROMS are available in 600-mil packages with JEDEC compatible pin-outs.

And they all share the reliable N-channel process technology.

TI's growing EPROM family. For all your present and future memory requirements.

For more information about the first 64K EPROM, or any other family member, call your nearest field sales office or authorized distributor. Or write to Texas Instruments, P.O. Box 1443, M/S 6955, Houston, Texas 77001.

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CALENDAR

CONFERENCES

MAY 1-2—An Assessment and Forecast of Computer Graphics, Stouffers Inn, Westchester, NY. INFORMATION: Bob Sanzo, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038. Tel: 212/233-1080

MAY 13-15—ELECTRO, Boston-Sheraton/Hynes Auditorium, Boston, Mass. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAY 19-21—Custom Integrated Circuits Conf, Americana Hotel, Rochester, NY. INFORMATION: Dr Andras Lakatos, Xerox Corp, Webster Research Ctr, 800 Phillips Rd, Webster, NY 14580. Tel: 716/422-4354

MAY 19-22—National Computer Conf, Anaheim, Calif. INFORMATION: AFIPS, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/243-4100

MAY 20-22—CENCON '80 Industrial Electronics Conf, Public Auditorium Arena, Cleveland, Ohio. INFORMATION: Mike Lapine, Cleveland Electronics Conf, Inc, 2728 Euclid Ave, Cleveland, OH 44115. Tel: 216/214-5515

MAY 29—Computer Networks Protocol Sym, NBS, Gaithersburg, Md. INFORMATION: Helen M. Wood, Conf Chairperson, National Bureau of Standards, Washington, DC 20234. Tel: 301/921-2834

JUNE 2-5—Sym on Incremental Motion Control Systems and Devices, Ramada Inn, Champaign, Ill. INFORMATION: Incremental Motion Control Systems Soc, PO Box 2772, Station A, Champaign, IL 61820

JUNE 3-5—Sym on Multiple-Valued Logic, Northwestern U, Evanston, Ill. INFORMATION: Jon T. Butler, Dept of Electrical Engineering and Computer Science, Northwestern U, Evanston, IL 60201. Tel: 312/492-5628

JUNE 8-11—Internat'l Conf on Communications, Red Lion Inn, Seattle, Wash. INFORMATION: ICC '80, PO Box 88465, Seattle, WA 98188

JUNE 16-18—ATE Seminar/Exhibit, Hynes Auditorium, Boston, Mass. INFORMATION: ATE Seminar/Exhibit, c/o Benwill Publishing Corp, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JUNE 19—Computer System Integrity, Technical Sym of the ACM and NBS Institute for Computer Sciences and Technology, National Bureau of Standards, Gaithersburg, Md. INFORMATION: Angela Turvey, 4910 Butternut Dr, Rockville, MD 20853

JUNE 23-25—Design Automation Conf, Minneapolis, Minn. INFORMATION: E. B. Hassler, Texas Instruments, Inc, PO Box 225621, MS 3907, Dallas, TX 75265. Tel: 214/238-5781

JUNE 25-27—IFAC Sym on Large Scale Systems: Theory and Applications, Toulouse, France. INFORMATION: Symposium Secretariat, AFCET-156, Bd Péreire-75016, Paris, France

JULY 22-24—The 1980 Microcomputer Show and Internat'l Conf, Wembley Conf Ctr, London, England. INFORMATION: TMAC, 680 Beach St, Suite 428, San Francisco, CA 94109. Tel: 415/474-3000

AUG 12-14—Computer Graphics 80 Internat'l Conf and Exhibition, Birmingham, England. INFORMATION: Paula Stockham, Online, Cleveland Rd, Uxbridge UB8 2DD, England

AUG 19-21—National Conf on Artificial Intelligence, Stanford U, Stanford, Calif. INFORMATION: American Association for Artificial Intelligence, Stanford U, PO Box 3036, Stanford, CA 94305

SEMINARS

MAY 19-20 AND JUNE 11-12—Database Management; MAY 19-20 AND JUNE 23-24—Data Communications; JUNE 16-17—Minicomputers: Selection and Use; AND JUNE 23-24—Computer Graphics: Update on Applications and Technology, Harvard U, Cambridge, Mass; Harvard U, Cambridge, Mass and L'Enfant Plaza, Washington, DC; L'Enfant Plaza, Washington, DC; and Harvard U, Cambridge, Mass. INFORMATION: Barbara Tarlin, Ctr for Management Research, 850 Boylston St, Chestnut Hill, MA 02167

JUNE 23-25—Error Correcting and Detecting Codes, Washington, DC. INFORMATION: Hellman Associates, 299 S California Ave, Suite 307, Palo Alto, CA 94306. Tel: 415/328-4091

SHORT COURSES

MAY 28-30—Peripheral Array Processors, UCLA, Los Angeles, Calif. INFORMATION: Continuing Education in Engineering and Mathematics, UCLA Extention, PO Box 24902, Los Angeles, CA 90024. Tel: 213/825-1047

JUNE 2-6—Modern Data Communications; JUNE 10-13—Pascal Computer Programming; JUNE 16-20—Digital Transmission Systems Engineering; JUNE 18-20—Software Design for Data Communications; AND JUNE 23-26—Computer Graphics Systems: Design and Applications, George Washington U, Washington DC. INFORMATION: Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

JUNE 3-6—Very Large Scale Integration, American U, Washington, DC. INFORMATION: Jennifer Murphy, Office of Summer/Special Session, American U, Washington, DC 20016. Tel: 202/686-2697

JUNE 16-27—Designing Microprocessor Based Systems, Massachusetts Institute of Technology, Cambridge, Mass. INFORMATION: Francis F. Lee, Professor of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139. Tel: 617/253-2598

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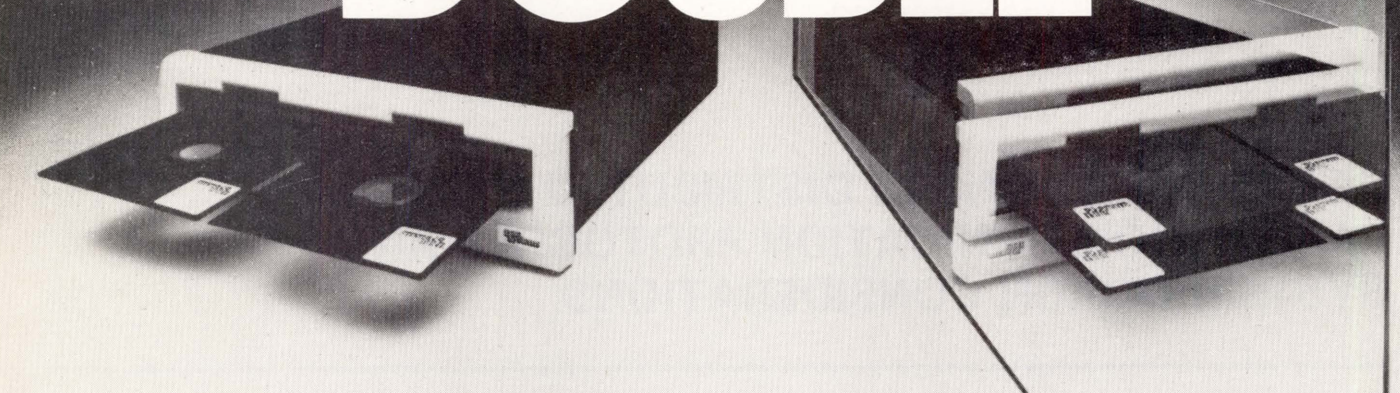

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CIRCLE 10 ON INQUIRY CARD

COMMUNICATIONS IN DISTRIBUTED SYSTEMS — PART 3: COMMUNICATION PROTOCOLS AND SYSTEM DESIGN CONSIDERATIONS

Melvin G. Gable

Ford Motor Company
Dearborn, Michigan

To define the language that accesses and updates shared variables in a distributed system a protocol is required. This is simply the set of rules that establishes an orderly way of exchanging information between two or more parties. The physical link (communication channel) carries two sets of information, data and control, and the link protocol must be capable of distinguishing between them. The protocol also insures the correct sequencing and integrity of data transmitted over the link. Basic protocol functions are to control data transfer and to provide data transparency, frame synchronization, and error checking and recovery.

Due to the activities of various standards organizations—Electronic Industries Association (EIA), International Standards Organization (ISO), American National Standards Institute (ANSI), and the International Consultative Committee for Telephone and Telegraph (CCITT)—electrical interfaces and serial protocol standards have been adopted.[1] These standards have eased the marriage of heterogeneous processors into a given system architecture.

Communication Control

In all the various protocols, the general format for information transfer includes a header, a data body, and a trailing check-field. In order to control the transmission of data, the header contains address information, block or packet sequence control, and acknowledgment information. Control flags indicate packet sequence, and whether data or control messages are being transmitted. Control messages are used to perform handshake functions as well as to acknowledge good or bad frames of data. Sequencing insures that data are received in the proper order, and that packets are not lost or duplicated.

Data Transparency

The physical link carries both transmitted data and link control characters. Since it is often necessary to transmit binary data, there must be a way to permit the use of all bit patterns in the data field and still have the capability to detect data link control characters in the frame. The techniques used for achieving this transparency differ from protocol to protocol.

Synchronization

Some form of frame synchronization is required between transmitting and receiving parties in synchronous data transmission. Most common of the methods is to precede the block with a unique bit pattern sequence. The receiver

The NEC Disk Drive. A Head of its time.

High-performance Winchesters. Available right now.

When you need Winchester-type disk drives in 20-, 40- or 80-megabyte capacities, take a hard look at the NEC D-1200 Series disks.

You'll find packaging, features, reliability and technology that are the results of 15 years of building high-performance disk systems.

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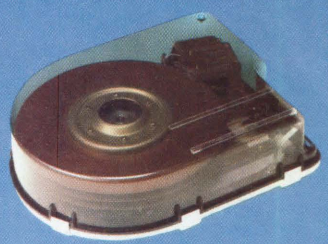
And every NEC D-1200 disk drive has reliability-plus. Its MTBF exceeds 10,000 hours. Because all of its components are NEC-designed and NEC-built—the unique rotary actuator, the circuitry, the sealed disk module, and the read/write heads.

Join the growing number of systems builders who rely on NEC D-1200 disk drives to make their total system more attractive. For more information, contact our nearest sales office.



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NEC Information Systems, Inc.

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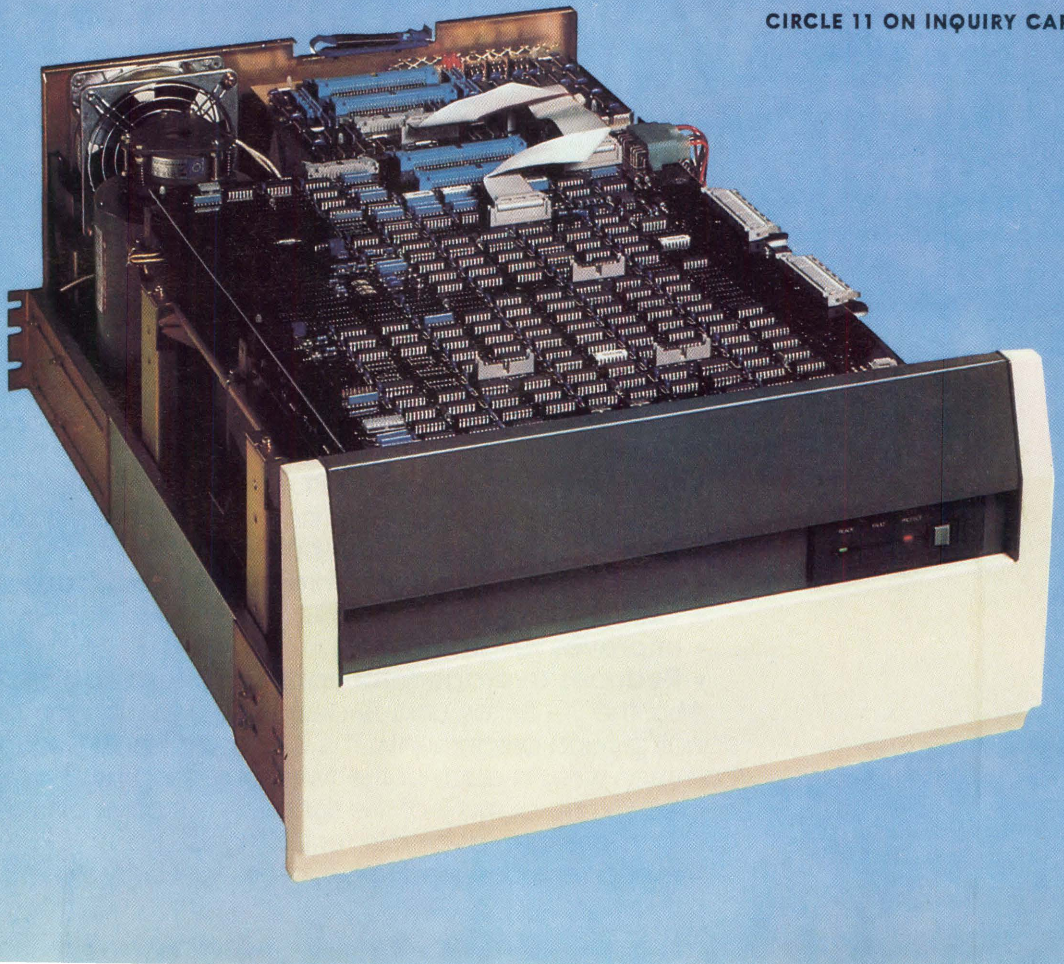
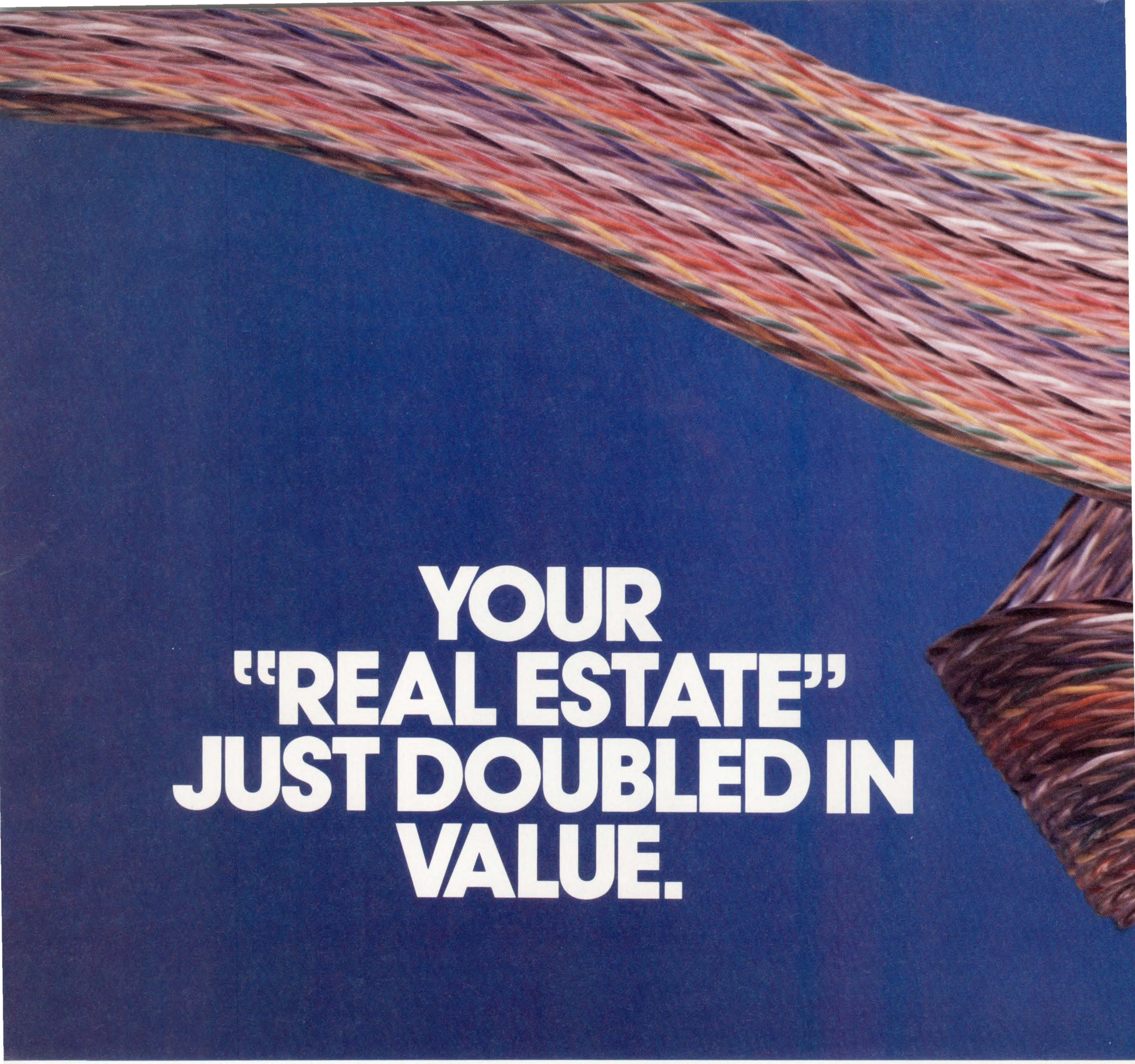
CIRCLE 11 ON INQUIRY CARD





Augat's new generation selective grounding (SG Series) IDC socket assembly and header system offers several important and unique customer advantages over conventional systems. For example, the SG Series:

- **Doubles I/O capacity of PC board "real estate"**
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- **Maximizes efficiency in wire and PC trace routing**
- **Cuts use of gold up to 75%**
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- **Reduces average total applied system cost by 20%**

Also, the SG Series' unique design permits any combination of signal/ground assignments. This is accomplished through grounding common wires in each of the two cable lengths with a buss bar connected to one or more of the signal pin-out contacts. All other pin-out contacts are then available for I/O signal use.

The header is designed to be the new industry standard. It provides:

- **Improved strength and durability**
- **Better contact protection**
- **Stronger latch and eject mechanism**
- **16-position polarizing**
- **Cable shield disconnectable grounding**

The SG system is configured to be readily designed into most new and retrofit applications.

All of this is accomplished at substantial total applied cost savings for most customer requirements.

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CIRCLE 12 ON INQUIRY CARD

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Earlier to market, the fatter the profits.

So don't tie up months and months developing your own controller/formatter for dual-head, double-density floppy disk drives.

We've done it all for you. Our new Remex RFS 4800 intelligent drive packs an IBM-compatible, microprocessor-based controller/formatter onto the same board as the drive electronics.

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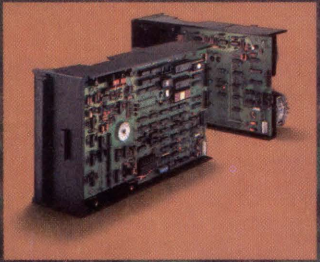

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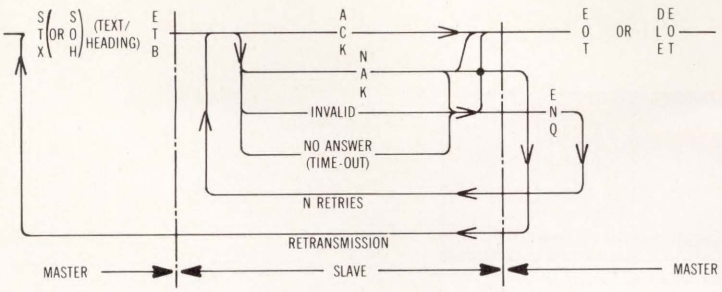

Fig 1 Stop and wait protocol. Transmitter must wait for ACK, NAK, or time-out before sending data block

searches for this unique pattern so that it can obtain proper frame synchronization. The number of bytes and the synchronization code employed differ among the various protocols.

Error Checking

Insuring a high probability of accurate data reception is an important function of the link protocol. The communication link itself is error prone, and to compensate for this, check bits or bytes are generated for testing on reception. Vertical redundancy checking (VRC), longitudinal redundancy checking (LRC), and cyclic redundancy checking (CRC) are the conventional checking methods.[2]

VRC is an odd or even parity check performed on each character, and requires a parity bit per data character. The LRC technique is used for checking an entire data block, and is frequently used in conjunction with VRC. LRC is generated by the exclusive-OR of all data bits within the block transmitted. CRC is a more sophisticated algebraic polynomial generation technique. The 1s and 0s of the data block become the coefficients of the polynomial. The remainder of the polynomial serves as the cyclic redundancy check. Standard polynomials used in serial transmission are: CRC-16 ($x^{16} + x^{15} + x^2 + 1$); CRC-CCITT ($x^{16} + x^{12} + x^5 + 1$); and CRC-12 ($x^{12} + x^{11} + x^3 + 1$). CRCs are capable of detecting burst or multiple-bit errors, common error modes on conventional communication channels.[3]

Automatic Request for Retransmission

There are two basic methods of acknowledging that a transmitted data frame has been correctly received. In the stop-and-wait scheme (Fig 1) the transmitter waits for a positive or negative acknowledgment after sending each data block. If an acknowledgment (ACK) is received, the next data frame is sent. However, if a negative acknowledgment (NAK) is received due, for example, to a redundancy check error, the same block is retransmitted. If no response is received after a given time-out period, the communication session is aborted. An example of a stop-and-wait protocol is IBM's binary synchronous communications (BSC) protocol (Fig 2.)

A variation of this method is the positive acknowledgment-only protocol. Since a time-out mechanism is normally needed to detect failure of a receiving parity, it can also be used to trigger retransmission, instead of a NAK response. The transmitter sends a data block and waits for a positive acknowledgment. If an ACK is not received before the time-out period, the block is retransmitted. Multiple transmissions are used to detect receiver failure.

In a go-back-N scheme, separate transmit and receive sequence numbers are maintained by the transmitting and receiving stations. When an acknowledgment is sent by the receiver, it contains the sequence number of the last correctly-received frame. The difference between the two sequence numbers "N" represents the number of frames that must be retransmitted. A variation in this scheme is defined in the advanced data communications control procedure

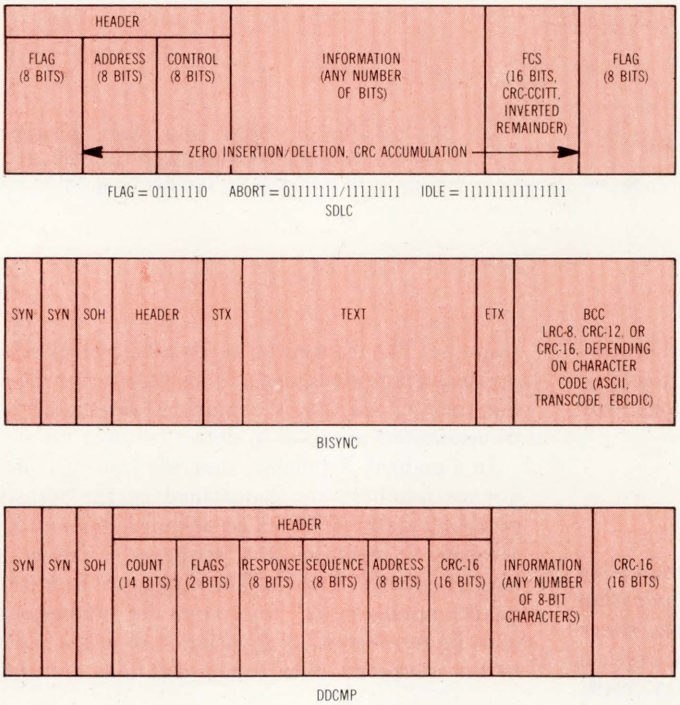

Fig 2 Three standard data transparency techniques. SDLC is bit-stuffing; Bisync, byte-stuffing; and DDCMP, word-count. (See Panel)

(ADCCP) protocol. This allows the receiver to send a selected reject supervisory command that requests retransmission of a single frame. An advantage of the go-back-N scheme is that long delays between receiver and transmitter, such as on a satellite channel, can be accommodated more efficiently. The major disadvantage is that the transmitter must contain enough buffer space to retransmit the entire set of data frames if a positive acknowledgment is not received.

Design Considerations

In implementing a given system, the designer has a wide choice of standardized protocols. Bit-oriented protocols such as synchronous data link control (SDLC), high-level data link control (HDLC), and ADCCP offer improved performance and flexibility over older byte-oriented protocols such as BSC. The bit-stuffing technique reduces transparency overhead. Such protocols allow the designer to select a window size with the desired number of message frames to be outstanding. This flexibility permits improving the efficiency when the communication channel has long delays between transmitter and receiver. Nevertheless, bit-stuffing usually requires special hardware to perform the data transparency function, while byte-stuffing can be done easily in software, using conventional parallel-to-serial and serial-to-parallel hardware.

The traditional hardware approach has been strongly impacted by the emergence of the multiprotocol chip. This device performs the basic task of assembling received serial data characters, and serializing transmitted characters. It also performs the data transparency function of bit-stuffing or byte-stuffing, as well as CRC polynomial generation and checking. Many of the devices incorporate modem control functions, the interchange signals between the data circuit and the data terminal equipment. Most devices are bus-oriented and contain multiple registers, designed to interface with an 8- or 16-bit data bus of a microprocessor.[4] The advantage of a multiprotocol chip is that it reduces the number of support circuits and permits adaptability to various line protocols on the same hardware interface. Nonetheless, these protocols have been designed to operate over synchronous serial transmission interfaces. However, a word count protocol such as digital data communications message protocol (DDCMP) can operate over synchronous and asynchronous serial or parallel interfaces.

The choice between serial or parallel bus structures depends on the system application. When the system is oriented around the exchange of global variables and words, parallel techniques offer an advantage. The increased bandwidth usually associated with a parallel bus diminishes the delays in accessing and updating variables.

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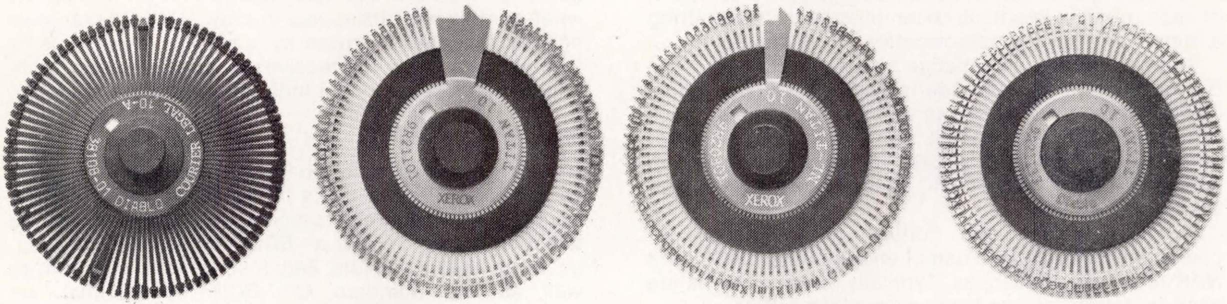

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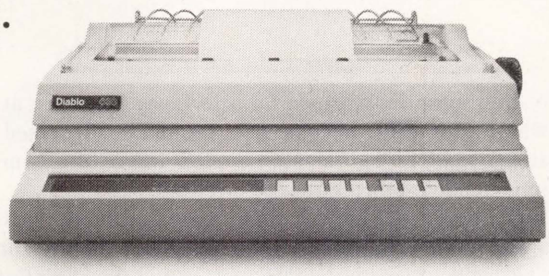

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Protocol Characteristics

Bisync

Binary synchronous protocol (BSC), also known as Bisync, has been widely accepted by the industry since its early use by IBM in 1968. The general form of the link level frame (Fig 2) is that of start of text (STX), the data body, end of text (ETX), followed by a block check field (BCC). The header is optional and its contents are defined by the user. Addressing of multiple stations is accomplished through separate control messages, and not by using the header field of the frame.

In the non-transparent operating mode, information in the data body must not contain link control characters. The text field is preceded by the STX character only.

For binary data transmission, a transparent mode is defined by starting the data field with data link escape (DLE), followed by the STX character. When a bit pattern equivalent to the DLE appears within the data, a second DLE is inserted in the transmission. When received, the first DLE is discarded, and the other is treated as data. This technique is called byte-stuffing. Synchronization of each frame in Bisync is accomplished by transmitting a minimum of two synchronization (SYN) characters.

Three information exchange codes are defined in the Bisync protocol. If the code is ASCII, a vertical redundancy check (VRC) and longitudinal redundancy check (LRC), an 8-bit BCC on the frame, are used for error checking. For EBCDIC, a CRC-16 is performed, which results in a 16-bit BCC. A CRC-12 is generated when 6-bit Transcode is used.

Acknowledgment and control of frames is accomplished through the use of enquiry (ENQ), ACK, and NAK response sequences. Typically, several retries are used to determine line loss and receiver failure.

DDCMP

The Digital Equipment Corp digital data communication message protocol (DDCMP) of Fig 2 can operate over synchronous and asynchronous serial or parallel transmission interfaces. DDCMP uses the ASCII control characters start of header (SOH), DLE, and ENQ to distinguish between different types of messages. Data within the frame are transparent.

Transparency is achieved by a word-count field in the header that determines the length of the data field, up to 16,383 bytes max. The header word-count is validated by its own CRC-16 check field. The valid word-count is then used when receiving to determine the end-of-frame where the second CRC-16 field is located. The second CRC-16 is calculated over the data field.

Synchronization on the DDCMP format is accomplished through the use of two ASCII SYN characters that precede link control characters SOH, DLE, and ENQ.

SDLC

Synchronous data link control, announced in 1973 by IBM, is a bit- rather than a byte-oriented protocol. The data message (Fig 2) is framed by a flag character whose bit pattern is 01111110, used to synchronize between message frames. Format of the block is flag character, fixed-length header with an 8-bit address and an 8-bit control field, variable-length information field, 16-bit check field, and trailing flag character. The CRC-CCITT polynomial is used to detect transmission errors.

The technique used to achieve data transparency is referred to as bit-stuffing. To insure that a flag character does not appear in the data field, a zero-bit is inserted wherever five one-bits appear in a row. When the receiver detects five ones followed by a zero-bit, it removes or deletes the zero-bit. If it receives six ones and a zero, it is a legal flag character that indicates end-of-message.

ADCCP and HDLC

ANSI's advanced data communications control procedure (ADCCP) and ISO's high-level data link control (HDLC) are bit-oriented protocols. Both employ the same basic bit-pattern format as SDLC for link control: flag, abort, go-ahead, and idle. Zero insertion and deletion, as well as the standard CRC-CCITT polynomial are employed, respectively, for data transparency and link error checking.

The major differences between IBM's SDLC and these two bit-oriented protocols are in the areas of message control and addressing. The address can be either a single octet or an extended address field. When the first bit of an address octet is zero, the following octet is an extension of the address. The control field can also be an extended length of two octets. This permits the send and receive sequences to be as many as 128 outstanding frames. The commands and responses differ greatly from those of SDLC. ADCCP and HDLC support a balanced link protocol, whereas SDLC assumes a master and slave configuration or an unbalanced link.

Due to their simplicity, bit-serial interfaces are more attractive where processors become geographically dispersed. Such systems tend to be loosely coupled where the communications become more message oriented.

To a large degree, the logical organization of the processing units and their functional dependency will dictate the performance of the communication system and the choice of interface. The frequency at which variables must be updated in remote processors will define the delay and throughput of the system. In general, the communication bus performance will determine the level of realtime process interaction and system integration that it can support. The designer must study the organization of the overall tasks in the system before determining whether it requires a serial, parallel, or shared memory scheme to achieve the desired performance.

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4. A. J. Weissberger, *Data Communications Handbook,* Signetics Corp, Sunnyvale, Calif, 1977

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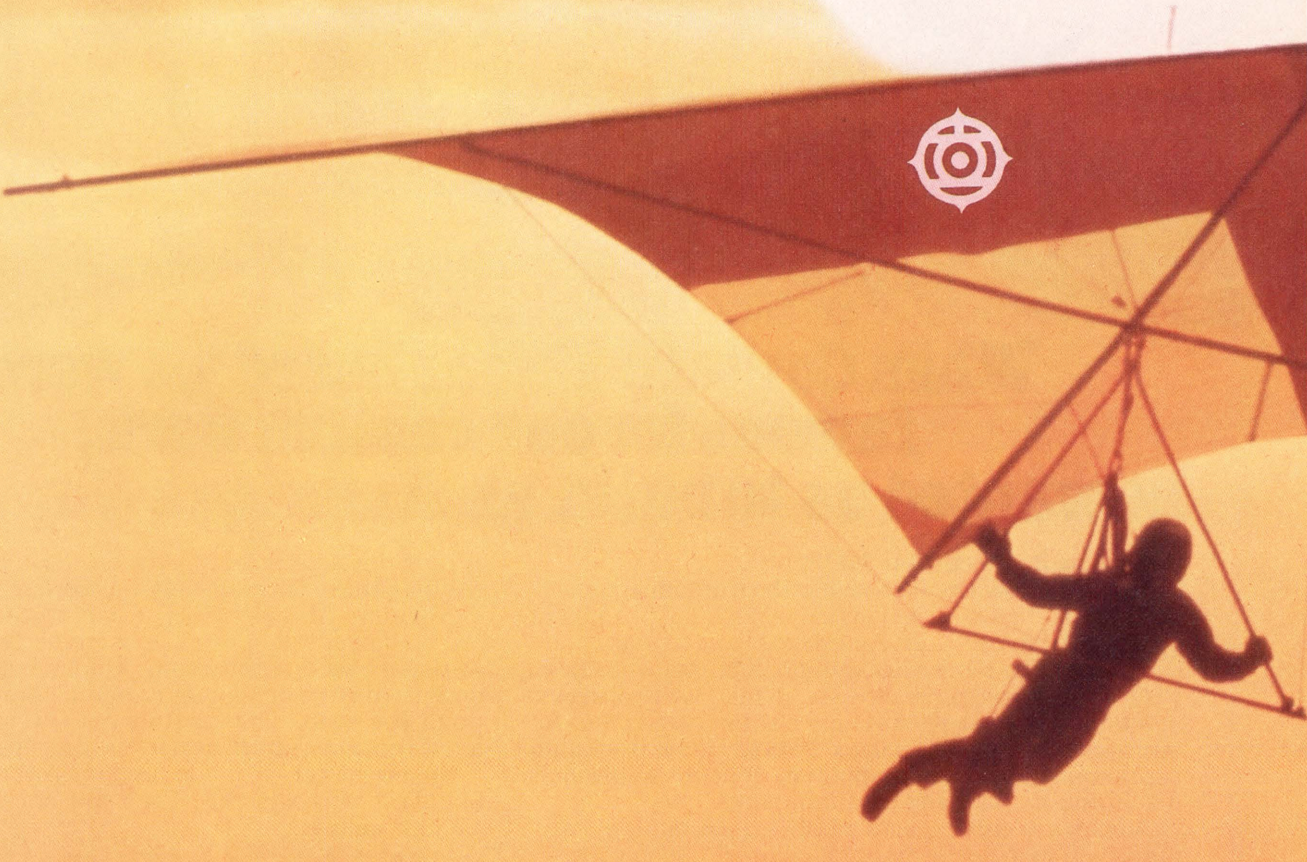

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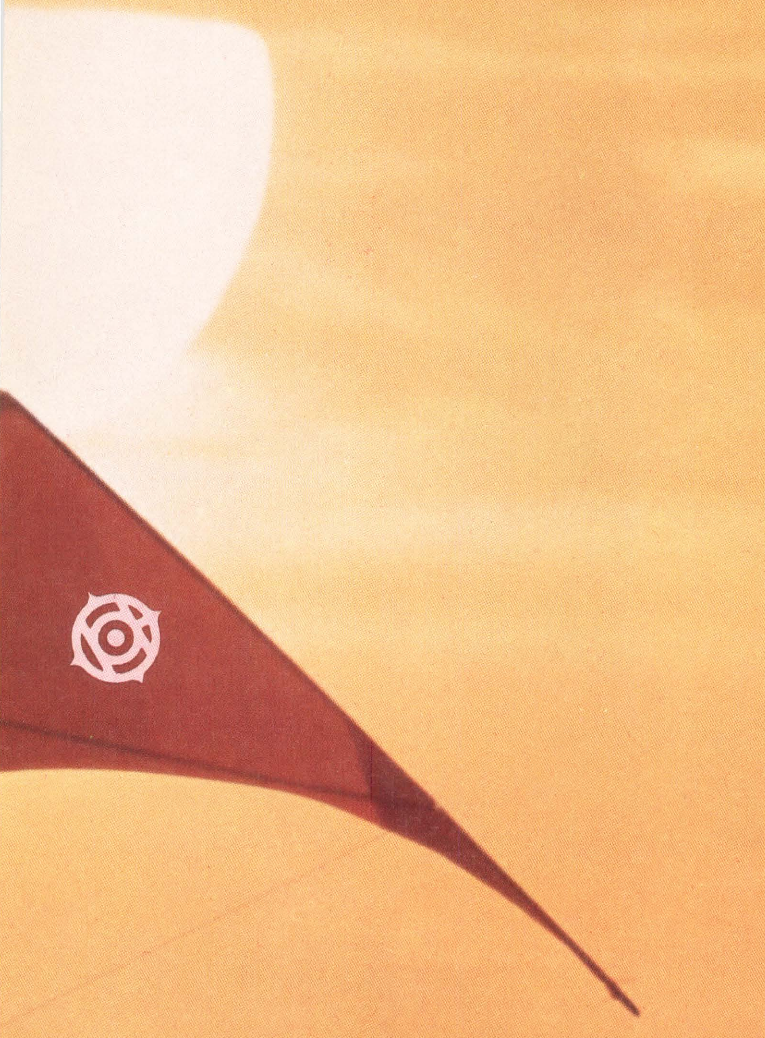

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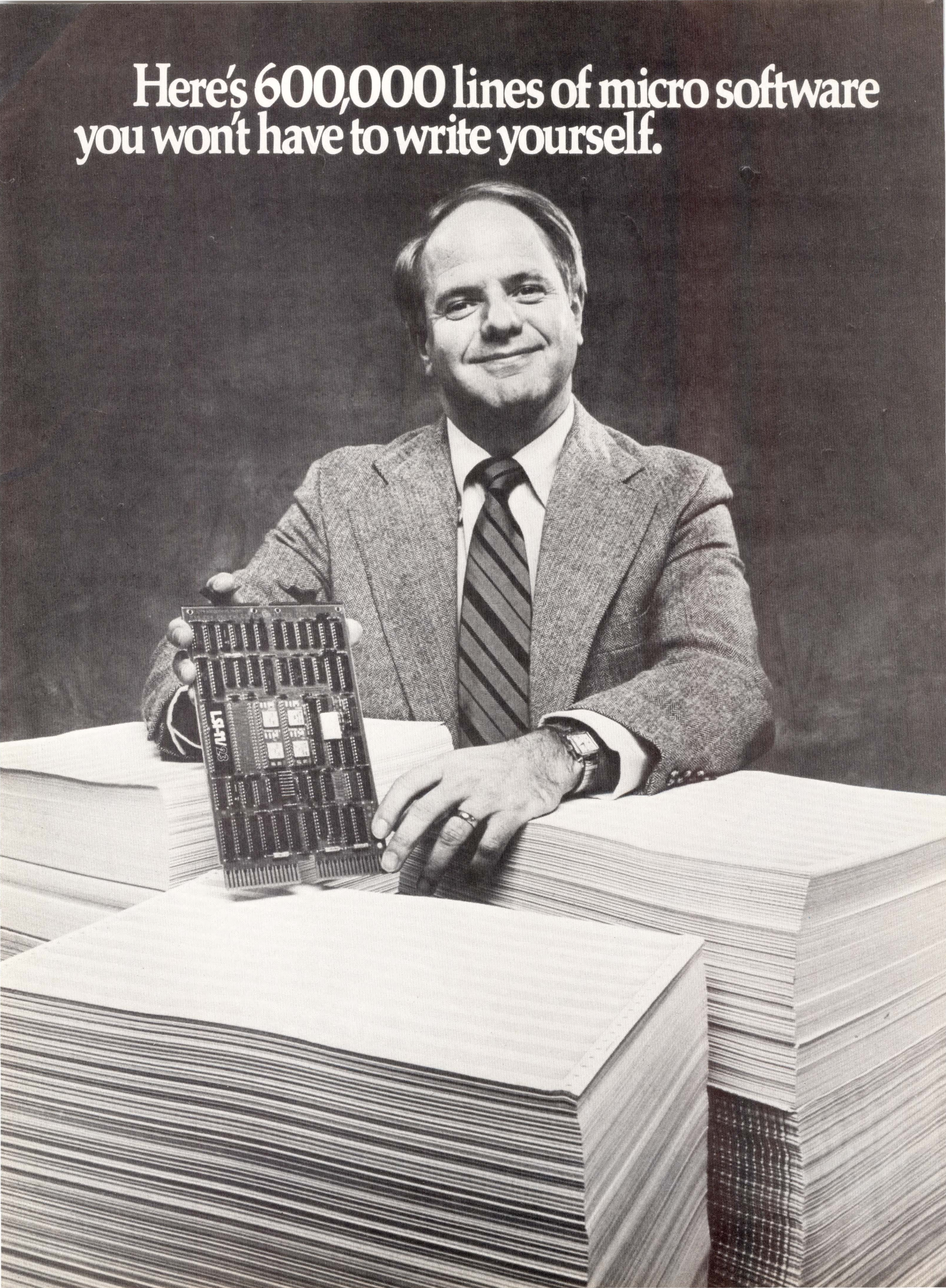
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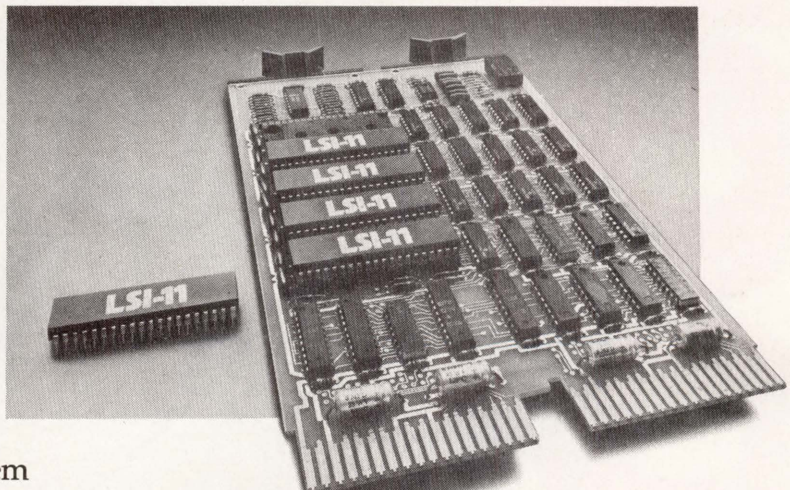

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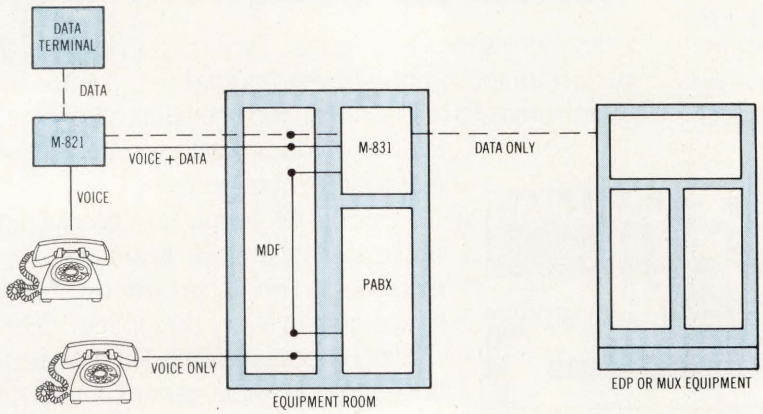

Data carrier system configuration. M-821 station unit and M-831 channel termination card convert any standard PABX station pair to simultaneous data transmission and telephone service

Data carrier system DCS-2B uses high frequency carrier techniques to add a data communications link to an existing PABX telephone pair. The derived point to point link is capable of 0 to 9600-bit/s full duplex asynchronous operation, and does not interfere with normal telephone service. Need for RS-232-C cable, additional twisted pair, or short haul modems is eliminated, according to the system developer, Teltone Corp, 10801 120th Ave NE, Kirkland, WA 98033.

Basic components of the system are the M-821 station unit and the M-831 channel termination card (see Figure). The station unit interfaces a data terminal and is connected in series between a telephone handset and a single-pair loop. It establishes a derived data channel using above-voiceband frequencies.

The channel termination card is located at the main distribution frame (MDF) or PABX equipment closet, and connects in series with the telephone pair to separate the voice loop from the derived carrier.

In operation, the telephone uses the customary 0 to 4-kHz band, and the M-821 station unit derives a full-duplex data channel by transmitting at 36 to 40 kHz and receiving at 72 to 80 kHz. Modulation is phase coherent frequency shift keying. The M-831 channel termination card at the PABX site separates the physical voice loop from the derived data channel. Appropriate filtering prevents mutual interference between the voice and carrier systems. Each M-831 card contains circuitry for two data channels. A card file, M-830-100, is available for mounting up to 16 channel termination cards.

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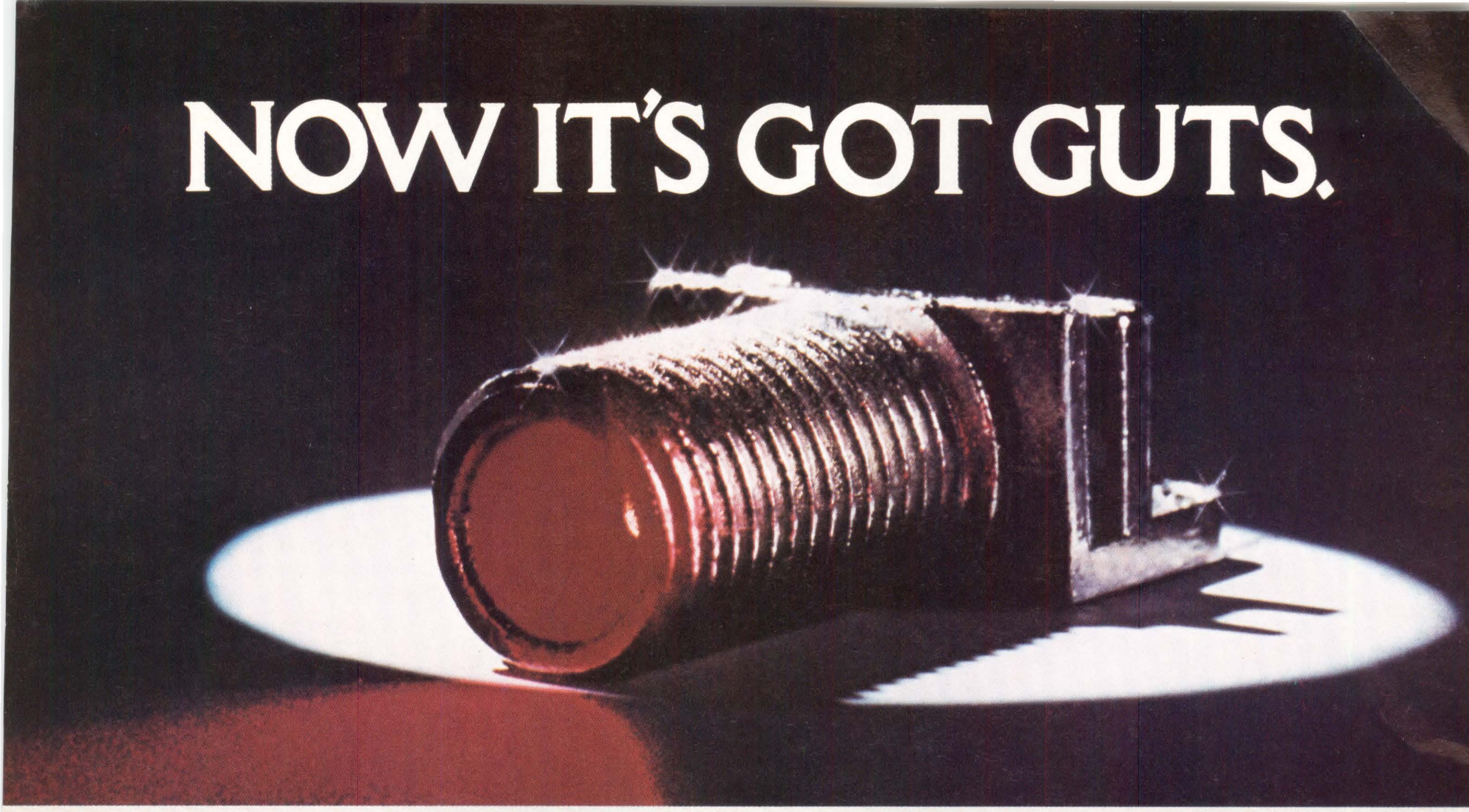

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Of course, its low profile and easy coupling advantages are still the same. But the Sweet Spot gives it much more design flexibility.

For example, now it can be used with practically any cable. And coupled with the widest selection of optical receivers yet. Everything from high speed PIN diodes to low speed high sensitivity detectors. Plus, it provides the simplest circuit interface and most practical opto-mechanical interface available. Here are some Sweet Spot detector options:

SPX 4690 Medium Speed Detector

This high sensitivity detector utilizes an on-chip transistor preamplifier to simplify circuit design and has a broad operating bias range of up to 15V.

SPX 4691 Sweet Spot PIN Diode

With a response time of one nanosecond and 5V operating bias, this high speed detector opens the door to hundreds of new possibilities.

SPX 4692 High Sensitivity PIN Diode

For interfacing large core fibers of 200 microns or more, this 15V PIN diode provides a performance level that will simplify many applications.

SPX 4693 Schmitt Detector

This fully integrated detector/interface circuit represents a major technology breakthrough. It's TTL and CMOS compatible and features a Schmitt Trigger output with total on-chip conditioning circuitry.

These are just a few of the endless new design solutions created by Sweet Spot LED power.

TYPICAL TRANSMISSION DISTANCE (METERS)

SPX 4689*(SWEET SPOT LED) WITH:	DUPONT PFXP140	DUPONT PFXPIR140	SIECOR 142	SIECOR 133	ITT T433	MAXIMUM DATA RATE (Mb/s)
SPX 4690*– MEDIUM SPEED DETECTOR	10	40	1400	400	500	1
SPX 4691*– SWEET SPOT PIN DIODE	10	35	—	650	950	30
SPX 4692*– HIGH SENSITIVITY PIN DIODE	16	60	2400	1300	1900	10
SPX 4693*– SCHMITT DETECTOR	13	35	1700	700	1000	0.1

*Part number describes component/connector assembly

Solutions that, coupled with AMP's sophisticated connector technology, bring fiber optics out of the lab — once and for all.

Contact Spectronics for more information at 830 East Arapaho Road, Richardson, Texas 75081. Telephone (214) 234-4271.

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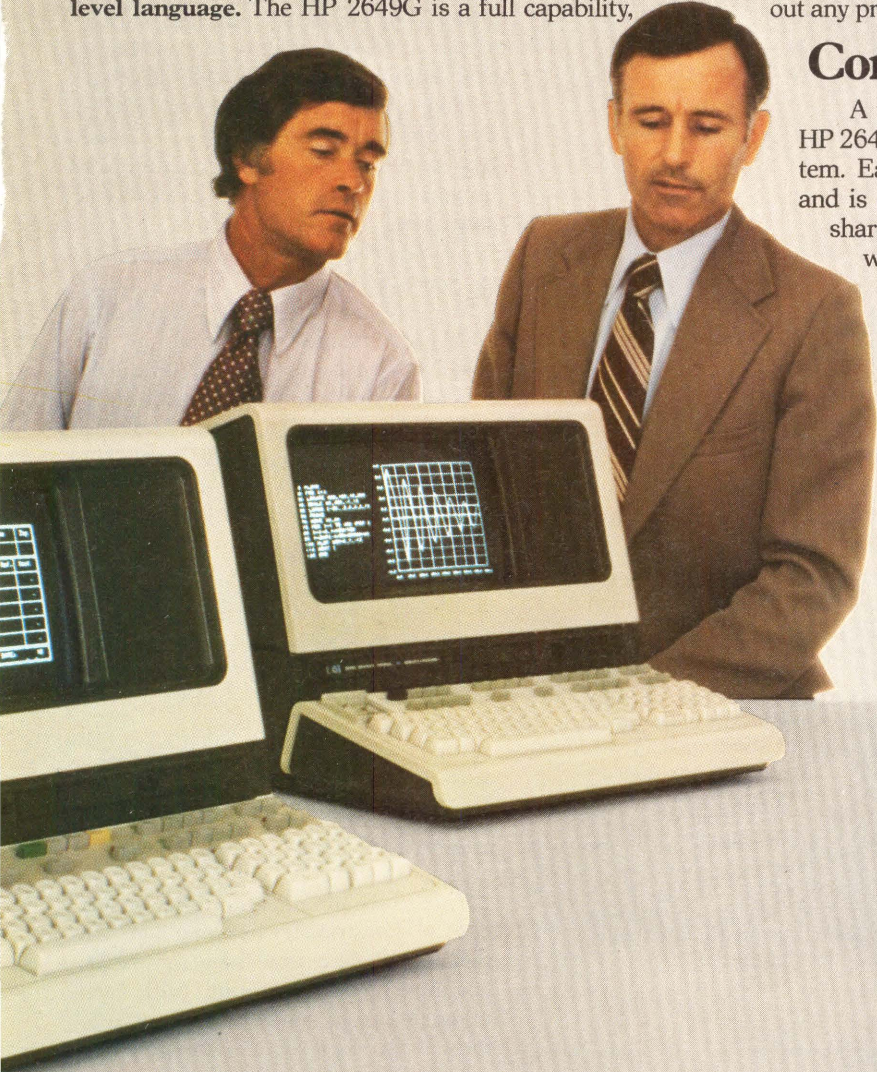
Light years ahead.

CIRCLE 20 ON INQUIRY CARD

some very smart OEMs

eight programmable keys provide menu-like instructions to guide the operator step-by-step through the job. You can even split the HP 2649I memory into four separate user areas for rapid switching between data sets, instruction menus, or data entry forms.

The HP 2649G. High-level graphics with a high-level language. The HP 2649G is a full capability, OEM-discounted graphics station, with raster scan technology, selective erase, pattern definition, and much more. And with AGL, our high-level extension to BASIC, graphics is a snap. Set axis, scaling, and location, for example, with a simple three-statement program. Or you can use our powerful Multi-Plot feature to run simple pie, bar, or linear charts without any programming at all.



Communications made easy.

A variety of serial and parallel interfaces make the HP 2649 terminals an extremely versatile tool in any system. Each works with the RS232C interface standard, and is compatible with most modems. And the optional shared peripheral interface provides communication with a wide range of printers, plotters, and other devices.

Whether you're designing a specialized terminal, controller, microcomputer or graphics display station, the HP 2649 Series gives you a real head start in building your product. And that's what being a smart OEM is all about.

If you'd like to know more about HP's 2649 Series terminals, just call your nearest HP office listed in the White Pages and ask for full details. Or send us the coupon below. We'll be glad to fill you in.

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"Productivity '80: The Computer—Its *New* Role." Hewlett-Packard seminars and practical demonstrations on how to get more from your resources in the coming decade. Watch your local newspaper for details.

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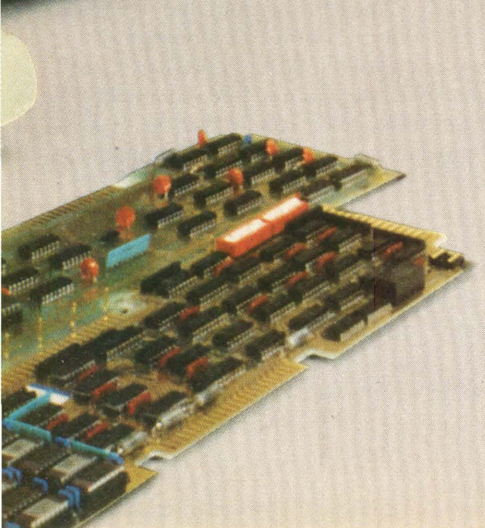


I'm interested in the HP 2649 Series terminals. Please send me more information about the:

☐ HP 2649A Microcomputer/Controller ☐ HP 2649I Intelligent Terminal
☐ HP 2649G Intelligent Graphics Terminal ☐ Please have a salesman call.

Name ____________ Title ____________
Company ____________
Address ____________
City/State/Zip ____________
Phone ____________

Mail to: Hewlett-Packard, Attn: Ed Hayes, Dept. 1263
19400 Homestead Road, Cupertino, CA 95014

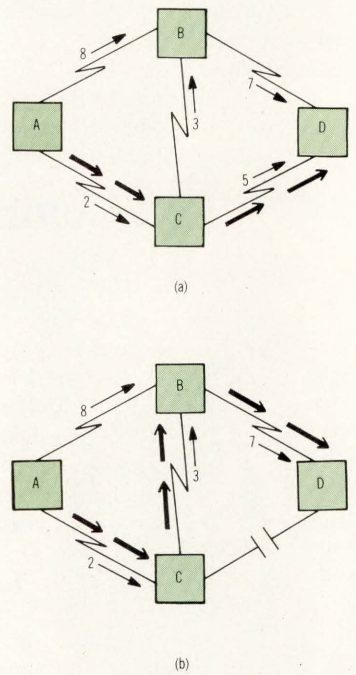
Phase III Software Offerings Broaden DECnet Communications Capabilities

Phase III software modules, designed to extend communication functionality among DECnet computers to include message routing, multipoint communications, and network command and management, have been announced by Digital Equipment Corp, Maynard, MA 01754. Phase III products are compatible with those released under Phase II (*Computer Design*, May 1978, p 22), and Phase II and Phase III nodes can participate in the same network. Also announced was a separate product, the RSX-11M/SNA protocol emulator, which enables PDP-11 computers using the RSX-11 operating system to conduct up to 61 concurrent data exchange transactions with an IBM host by emulating a remote systems network architecture (SNA) device.

Initial Phase III products are DECnet-11M-PLUS, and new versions of DECnet-11M and -11S, for use with PDP-11 computers using RSX-11M-PLUS, -11M, and -11S realtime operating systems.

Adaptive path routing is a major feature of the offering. It allows one node to send messages to another using intermediate nodes (see Figure). Routing tables, updated whenever changes in line or system status occur, are maintained at each node. Where there is more than one path between source and destination nodes, the least-cost path is chosen according to line values assigned by the network manager. The network automatically reroutes the message to the next-least-cost path if service should be interrupted on any line. Phase III networks comprise both routing nodes, which can send, receive, and forward messages, and end nodes, which can only send and receive.

Multipoint, or multidrop capability allows up to six remote (slave) systems to communicate over a single line with a host (master) system, which controls communication and polls each slave in turn. Multipoint configurations can exist as subgroups within larger networks, where both master and slave systems can participate in message routing, file transfer, and resource access with other systems.



DECnet adaptive path routing. Four-system network is interconnected by lines whose values are based principally on line speed (low value = high speed). In (a) system A uses routing table to select path with lowest total value to send messages to system D. In (b) system C detects line failure, sets an infinite value for that line, and updates routing tables at other nodes. System A then selects next-lowest-value path to transmit to system D. Routing process is automatic and entirely user-transparent

The network command function allows a terminal at one DECnet node to perform standard terminal functions on any other node that uses the same operating software. Interaction is carried on as if the terminal were local to the remote system, and the network interface is user-transparent. Direct access to programs and devices on remote systems anywhere in the network is provided by the network command function.

Efficient monitoring of communication load factors, error rates, line condition, and node status at all points in the network is enabled by network management capability. This can be either centralized or fully distributed across all nodes. The software allows evaluation of overall network efficiency and optimization of traffic flow by dynamic adjustment of line values. System, interface, and line testing can be performed while network operation continues.

License fees for initial releases of the new software are $5000 for DECnet-11M-PLUS, $3500 for -11M, and $1500 for -11S. Single-use license fee for the RSX-11M/SNA protocol emulator, with documentation and support, is $7000.

Looking to the future, the company also announced support of the CCITT X.25 recommendation for public packet-switched network implementation as one of its distributed data processing goals.

Communications Processors Provide Flexibility in Remote DDP Operations

CP series communications processors control data transfer between nodes in distributed data processing networks, and link remote operations with each other or with central computers to form large scale communication networks. The series, from Burroughs Corp, Detroit, MI 48232, includes two levels, CP 9400 and the more powerful CP 9500; they allow the company's computers and terminals to communicate readily with other manufacturers' equipment.

The CP 9500 architecture uses four independent processor elements, each dedicated to separate functions: operating control, data file management, compilation and execution of user application programs, and data communications. Processor elements

The World of the 600 Series Digitizer

The Talos **600 Series** offers the most complete line of digitizer configurations available. Three types of surfaces are offered, which include — solid with a formica top, translucent for backlighting, or a special finish for rear projection. Each surface type is offered in six active surface areas ranging from 11″ x 11″ to 44″ x 60″, giving the user tremendous versatility in applications.

The technology employed in the 600 Series is the electrostatic "active inch" principle. This principle allows the activation of only the square inch surrounding the pen or cursor. High accuracy and stability can be maintained because we resolve only one square inch regardless of tablet size. Resolution is 1000 lines per inch with accuracy of ±.01 standard, and ±.005 optional.

Our **Smart One** option can be added to the 600 Series tablet to provide a new dimension to your interactive graphics processing. The Smart One is an 8080 microprocessor located in the electronic control box with the digitizer. It provides local processing of digitized data which allows:

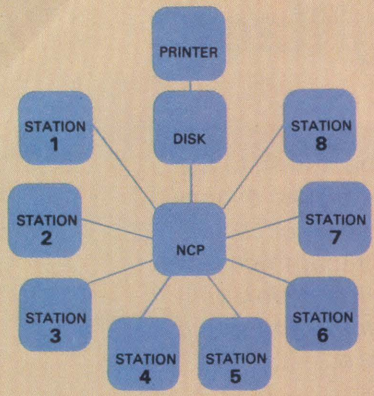
- Movable menus
- Switch selectable features
- Relocatable origin
- Assign user's values to origin (X and Y)
- Scaling and increment distance selection
- Skew corrections
- Dual port RS232C capability
- Distance, area and volume calculations
- CRT prompted readout

Because these routine calculations can be performed by the digitizer, valuable computer time will be saved, making your operation economical and efficient.

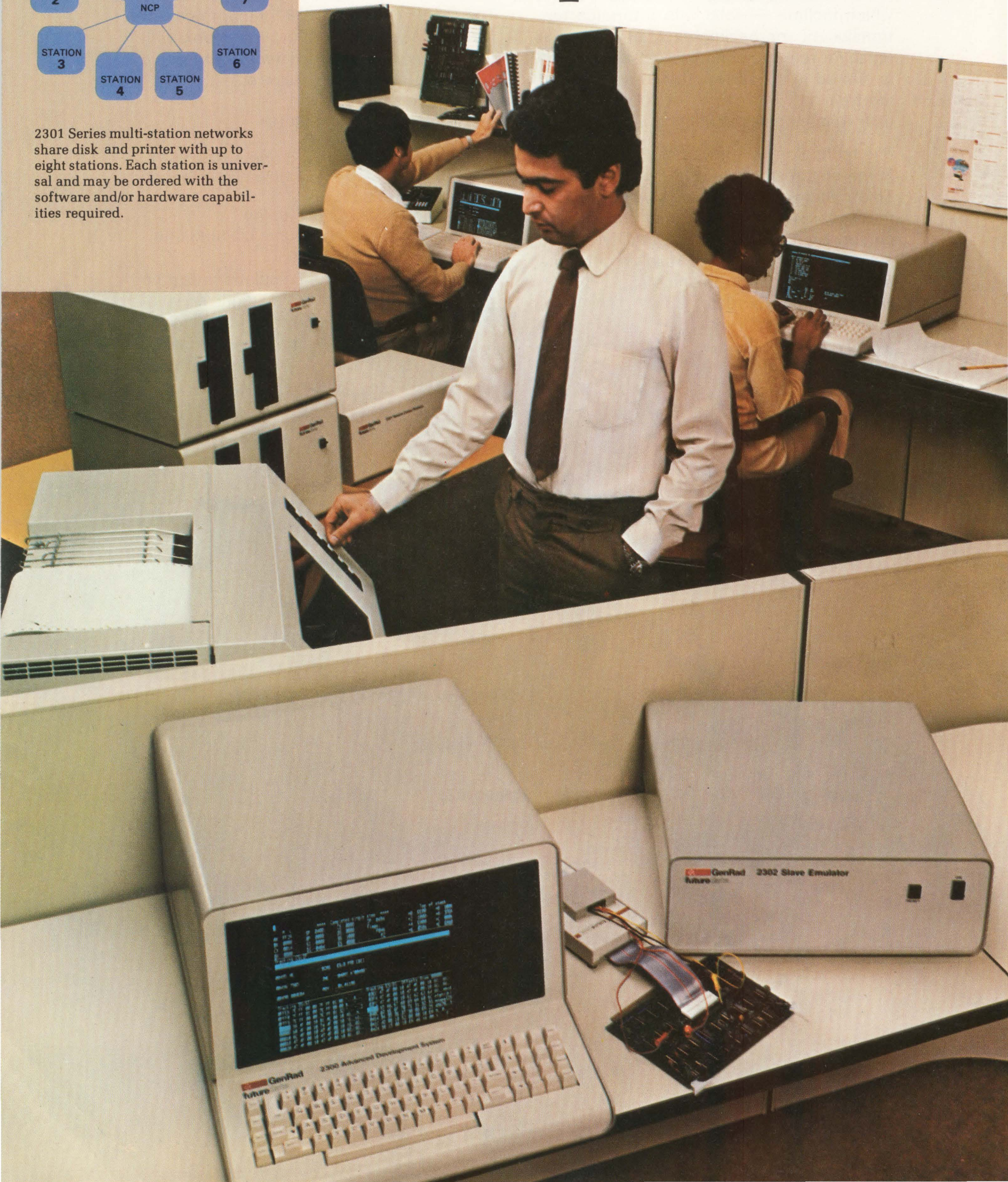
talos

CIRCLE 22 ON INQUIRY CARD

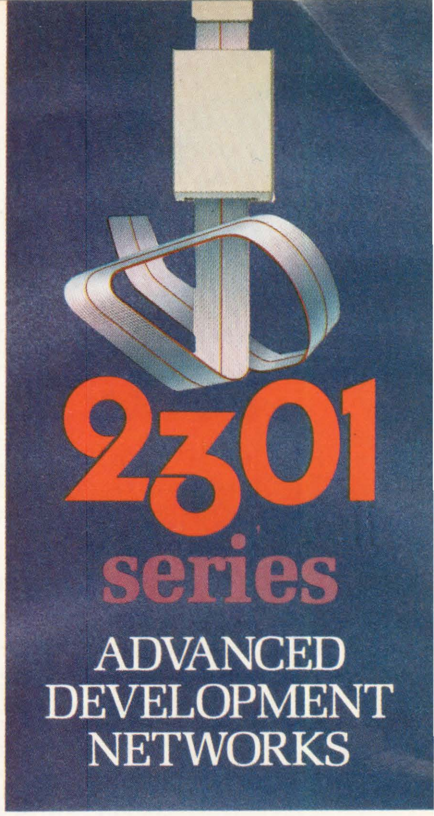
Multiply your micro capabilities with



2301 Series multi-station networks share disk and printer with up to eight stations. Each station is universal and may be ordered with the software and/or hardware capabilities required.



processor based design our universal network



ADVANCE YOUR SMART-PRODUCT DEVELOPMENT PROGRAMS—Our universal, multi-user development system network is the most cost-effective means of implementing a multi-station, microprocessor-based design facility. It's also the most versatile and productive solution to smart-product design.

MORE SUPPORT FOR MORE CHIPS FOR MANY USERS—Our network stations already support all of the most popular microprocessors. Our unique slave emulation system permits us to add support for new chips faster than anyone else. With eight stations tied into our network you can stop paying designers to wait in line. All eight can be developing products simultaneously with different chips.

MULTI-PROCESSOR EMULATION—Our slave emulation system provides transparent, non-stop, full-speed emulation to 10 MHz. And, it's the only system that allows simultaneous emulation of many different processors. Up to eight emulators can be tied into one network station. Our transparent in-circuit emulation and logic analysis take all the guesswork out of processor evaluation and design, even for products using several different chips.

SHARE AND SAVE—By sharing costly and under-utilized resources (disks, printers, slave emulators, design aids and software), a network system lowers your cost-per-station dramatically. Without trade-offs! Each user has his own CPU, CRT and keyboard. The same powerful software supplied with our stand-alone development systems is provided to each network station. Each station can be equipped with any combination of software and/or hardware capabilities you require, including local disk storage.

SPEED UP YOUR PROGRAMMING—With our interactive, high-speed CRT, complete operating system software, and assembly and high-level language programming capabilities, things happen fast—sometimes instantaneously. Now available with highly block-structured PASCAL compilers, our system can cut your programming time by 50% or more.

RELY ON THE LEADER—We started delivering network systems over one year ago. For a complete understanding of how these cost-effective systems can multiply your capabilities, contact one of our worldwide sales and service offices today.

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CIRCLE 23 ON INQUIRY CARD

Choosing a 16-bit MPU is no easy job. We know. We went through it ourselves back in '78.

We chose the Z8000 because we believed you'd choose the Z8000. Because it's better. Here's why:

"The AmZ8000 has a better architecture."

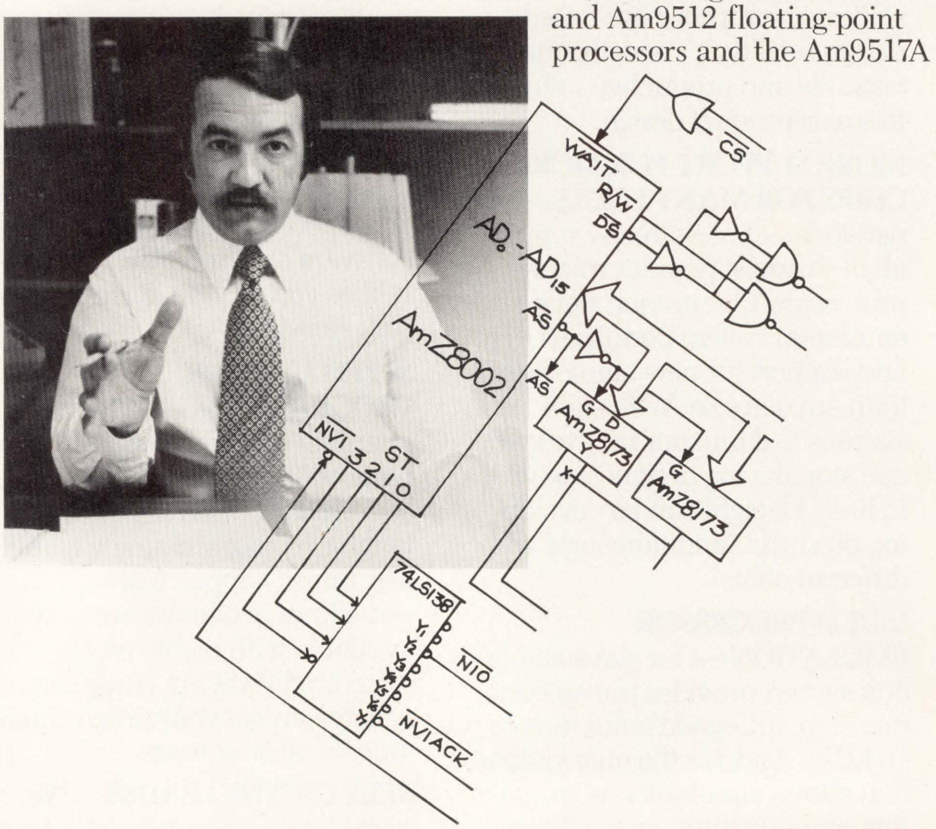
It has 16 registers. All general. All for you. Use them for data or addresses. Use them to write more efficient software with less code and faster execution.

The AmZ8000 has gobs of address space: 8M bytes of direct addressing in each of four possible address spaces. It has memory management with sophisticated relocation and protection features. It has a rich instruction set that operates on data types from quad length words right down to single bits. You can even map the I/O into memory or keep it separate.

As if all that weren't enough, the AmZ8000 has a whole series of string-oriented instructions to move, translate or compare up to 64K bytes of data in a single instruction.

"The AmZ8000 has a better future."

The AmZ8000's architecture and instructions fit perfectly with today's computation, communications and instrumentation markets. So do the peripherals. And all the popular existing parts for the 8080A/8085A, including the Am9511A and Am9512 floating-point processors and the Am9517A



Sven Simonsen, Vice President and Technical Director, Advanced Micro Devices

"The AmZ8000 is better for your application."

operate concurrently, each at maximum rate, allowing the system to continuously use all its resources at peak efficiency and maintain a consistently high throughput. Peripheral options for the CP 9500 include a lower cost printer series and lines of fixed and flexible disc drives. Both CP 9400 and 9500 have a comprehensive system software package, transaction control system (TCS), for online transaction processing. The series can be configured in networks of Burroughs and non-Burroughs host systems and terminals, or as communicating standalone computers supporting peripherals and terminals.

CP series systems can be tailored to specific requirements of individual sites through combinations of processor power, memory size, peripheral subsystems, and data communications capabilities. The series includes several models which range in memory size from 96k to 640k bytes, offer disc storage capacities of 6M to 520M bytes, and provide from two to 32 data communication lines.

A typical CP 9400 system would include 96k bytes of memory, a 1M-byte Super Minidisk drive, 18M bytes cartridge disc storage, two data communication lines, and operator console. Purchase price of such a system is $26,500; on 3-year lease, the cost is $736/month.

Typical CP 9500 system would include 384k bytes main memory, dual flexible 6M-byte capacity disc drives, 77M bytes fixed disc storage, four data communication lines, and operator console. This system's purchase price is $36,029, or $1092/month on a 3-year lease.

Circle 402 on Inquiry Card

Prototype 8M-Bit/s Fiber Optic System Tests Equipment Characteristics

A complete 8M-bit/s fiber voice and data transmission system, said to be the first commercially available equipment of its kind, has been installed and demonstrated in Great Britain. First delivery of the production line equipment is planned for mid-1980 to meet the requirements of contracts received from the British Post Office for the supply of 14 systems on five transmission routes in England and Wales. The system is a joint development of BICC Telecommunication Cables Ltd, Prescot, Merseyside L34 5SZ, and Plessey Telecommunications Ltd, Transmission Div, Beeston, Nottingham NG9 1LA.

While the prototype system is designed to operate at the CCITT/CEPT rate of 8.448M bits/s, the engineering configuration allows future operation at different bit rates by modification of units. This permits the system to be used as a test bed for other systems as may be required. The test system route runs from Maidenhead to Slough, a distance of about 14 km. One dependent repeater is used, located about 4 km from Slough.

Specifications for the cable subsystem called for 36-dB max optical power attenuation at 900 nm and approximately 10-MHz optical bandwidth. The installed cable has two optical fibers, plus four copper wires that provide order wire and power facilities to the repeater (Fig 1). The Corning Glass Works fibers have a 62.5-μm nominal core diameter, and a cladding diameter of 125μm. The graded index core glass provides a 200-MHz/km minimum bandwidth.

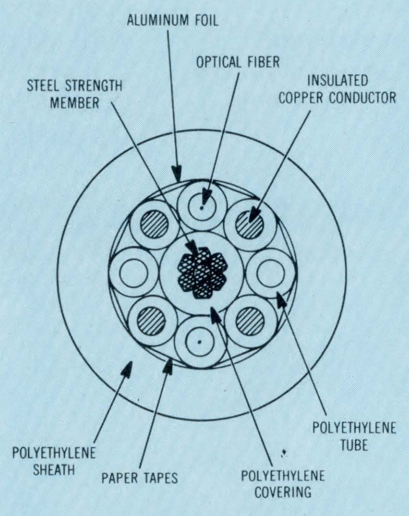


Fig 1 Cross section, optical fiber cable. Fibers are protected by loose tube rather than by tight buffer coating per BICC fiber packaging technique. This protects against fiber surface damage during cabling, and in conjunction with central strength member, isolates fibers from forces encountered during installation. Resulting cable is very stable and relatively unaffected by handling or changes in temperature

System optical connectors comprise two male connectors joined by screw coupling to a common "uniter", whose self-centering mechanism correctly aligns and spaces the opposing ferrules of the connectors (Fig 2). A

See page 99

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We're out to build the biggest, best OEM base in the industry. And we've decided to do it the fastest, surest way possible. By offering OEMs the best deal in the business.

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Have you ever been interested in becoming a supplier to a specific vertical market only to find you already had too much invested in software to warrant conversion to a new system with an expensive start-up price tag?

We've got a plan that provides you with a specific vertical market software package. We know where to find software that runs on our hardware with all the necessary capabilities. So we can practically eliminate start-up time and make your new system profitable with your very first sale.

WE WANT TO SUPPORT YOU.

Opening doors to vertical markets is only the first step in our plan. After we get you started, we keep you going. We'll provide marketing support suited to your specific market. And we'll provide leads from your geographic area.

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Because we're out to win. And we've got the support that can make it happen. Sperry Univac was first in the computer industry. And we're growing from the success established by Sperry Univac with over $10 billion in installed systems worldwide.

That total support includes a heavy commitment to the kind of research and development that produced some of the first systems to run COBOL, FORTRAN, PASCAL, RPG II, TOTAL, Timesharing, Transaction Processing and a mix of communications protocols concurrently.

And we're going to keep it up. Providing a wide-range of products at the forefront of technology is as much our business as selling and delivering equipment.

We've done just about everything we can think of to make working with Sperry Univac easy. And of course, all our products are supported by 10,000 technicians servicing our hardware worldwide.

If you can think of anything else we can do for you, give us a call right now. We mean business.

For more information write to us at Sperry Univac Mini-Computer Operations, Marketing Communications, 2722 Michelson Drive, Irvine, CA 92713. Or call (714) 833-2400, Marketing Communications.

In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

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CIRCLE 26 ON INQUIRY CARD

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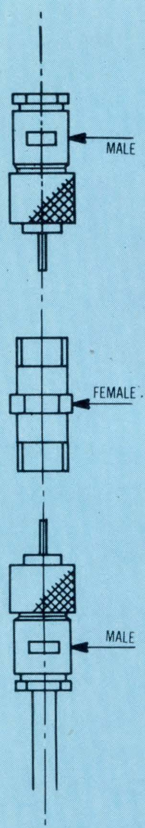


Fig 2 Uncoupled fiber cable connectors. Units are designed for graded index silica glass fiber with numerical aperture of 0.23 max. Connector assembly imparts low stress to anchored fiber. Other fiber types and sizes can be used with small modification to connector

constant 1-dB insertion loss is maintained during repeated matings and unmatings.

LEDs were chosen as optical sources because of their proven reliability, performance, and ruggedness, although laser sources were given serious consideration. While lasers have greater power output, LEDs can be used effectively at the medium and low bit rates used in this system. The devices chosen have been in production for some years at Plessey Optoelectronics and Microwave at Towcester. They use an etched-well structure for efficient coupling of optical power into the fibers. A microlens is included between fiber and emitting area to increase coupled power.

Significant from a systems viewpoint, another factor in the choice of an LED as the optical source is that the LED device operates at 900 nm. Most lasers operate at wavelengths between 800 and 850 nm, and since the fiber attenuation falls with increasing wavelength, the LED provides an approximate 0.5-dB/km saving in fiber attenuation. This is worth 5 dB over a 10-km route length, offsetting the larger power normally available from a laser source. An RCA avalanche photodiode (APD) was selected from commercially available devices to meet performance requirements as the optical receiver.

To insure presence of timing information and maintenance of dc level the CCITT 3B4B alphabetical code was chosen as suitable for the system. This code also provides a slight advantage on noise performance, and is expected to prove more adaptable at higher line rates.

The line terminal unit (Fig 3) consists of a transmit and receive unit. Input signal is in CCITT HDB3 interconnection format. When the input signal fails, an alarm indication signal (AIS) of all 1s is transmitted forward from a local clock.

The transmit unit is mounted on one PC board and contains the HDB3 binary converter, scrambler, 3B4B coder and driver amplifier/LED combination.

Two boards comprise the receive unit. The first has circuitry primarily concerned with retiming and regeneration from the APD detector. Outputs are the optical line data rate and a clock signal derived from the recovered line signal clock. After timing recovery and level detection, the signal is passed on to board 2, which contains the decoder, reframe and error detection, descrambler, and binary-to-HDB3 converter stages. The decoder proper is based on a read only memory (ROM) which enables the bit error rates and reframe indications to be readily obtained.

Regenerator equipment consists primarily of PC board 1 from the line terminal receive unit with the LED driver/amplifier combination added. Space is available to incorporate supervisory and error-rate circuitry later should this be necessary.

Based on the design and components used in the system, mean times between failures (MTBFs) have been estimated for terminals and repeaters. A one-way regenerator worked out at 122 years, and a complete terminal including power units and alarms at nearly 15 years. These figures indicate that optical fiber systems are potentially more reliable than their conventional cable counterparts because their designs are generally less complex and use fewer components.

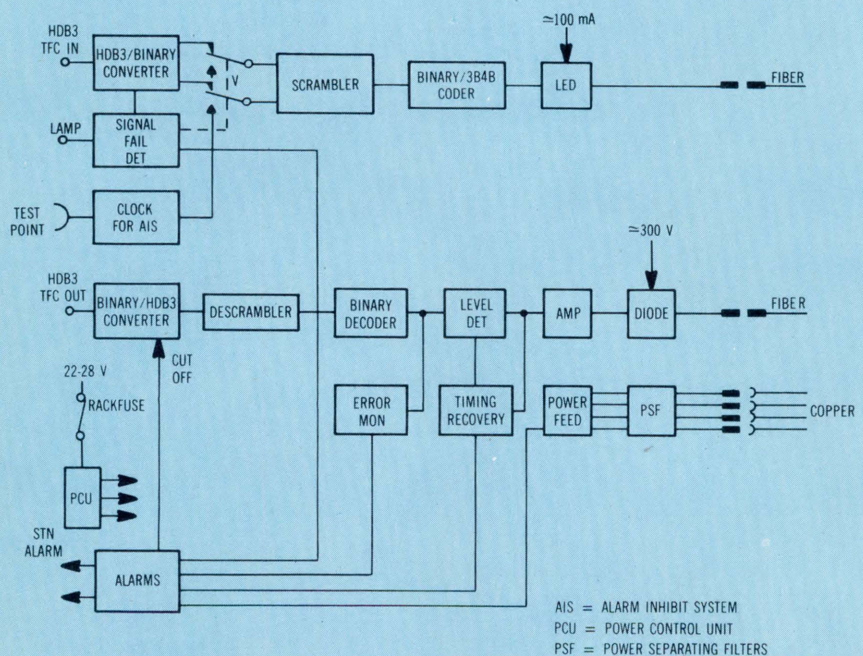
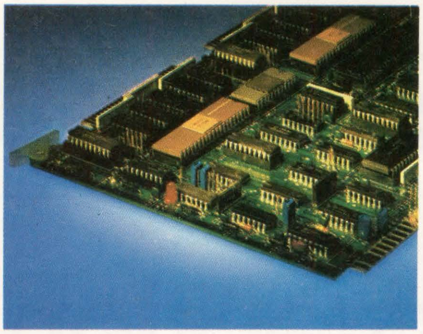


Fig 3 Line terminal equipment. HDB3-to-binary converter and LED driver stages are of discrete component construction in general, but coder/scrambler uses seven DIPs for compactness. Coder technique is based on use of ROM

Expand with the MSC 8001



The MSC 8001 is a MULTIBUS™ compatible single board computer designed to provide new dimensions in function and versatility. Built around the powerful eight-bit Z80™ CPU, the MSC 8001 provides a flexible memory addressing scheme and extensive input/output capabilities at prices well below competing single board computer products. Using the MSC 8001 as a master module, you can select I/O and special feature modules to configure a system of virtually any complexity or refinement.

Expand SBC 80 systems Upgrade existing SBC 80 systems that are being slowed down by limited memory size or restricted execution cycles. All existing I/O boards and memory expansion cards will operate with the MSC 8001.

Expand to meet future needs The MSC 8001 is designed to accommodate a wide range of versatile configurations. Almost any combination of memory, inferface complement, and other options can be configured to meet your specific requirements without hardware modification.

For additional information on the MSC 8001 and our other 41 Monolithic Systems Corp. products and systems, please contact us at 14 Inverness Drive East, Englewood, Colorado 80112. (303) 770-7400. Telex: 45-4498.

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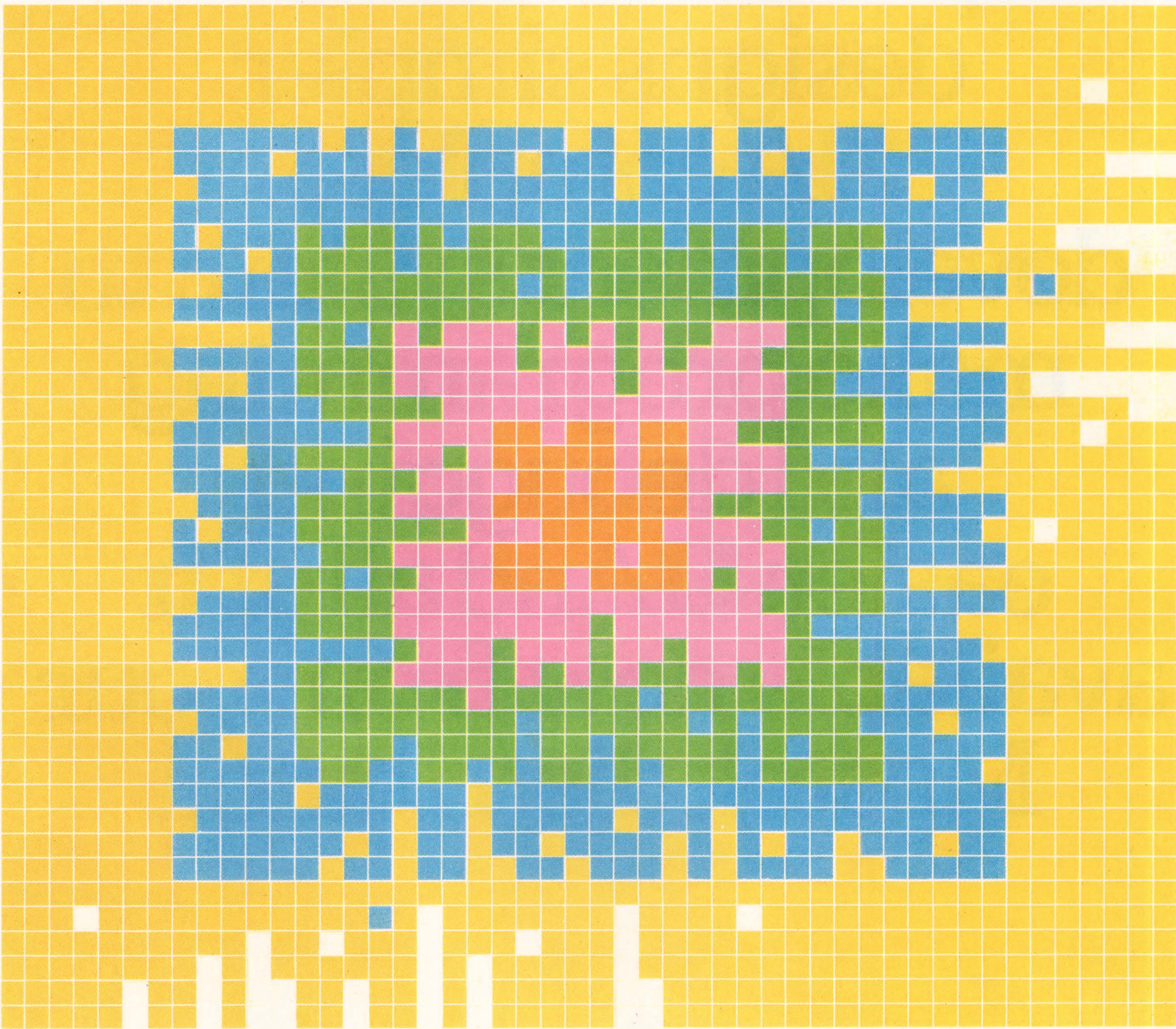
Extending the limits of information.



MSC Regional Sales Offices: Eastern Region 1101-B9 State Road, Princeton, NJ 08540, (609) 921-2240; **Central Region** 7200 East Dry Creek Road, Suite #B203, Englewood, CO 80112, (303) 773-1060; **Western Region** 49 South Baldwin, Suite D, Sierra Madre, CA 91024, (213) 351-8717

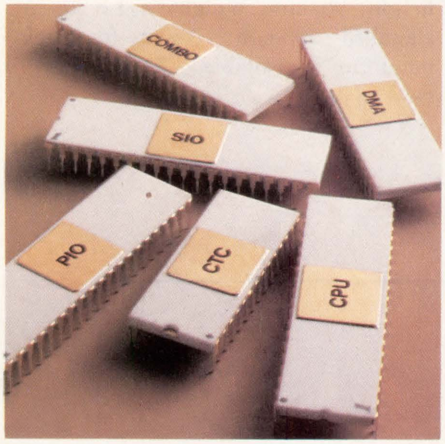
CIRCLE 27 ON INQUIRY CARD

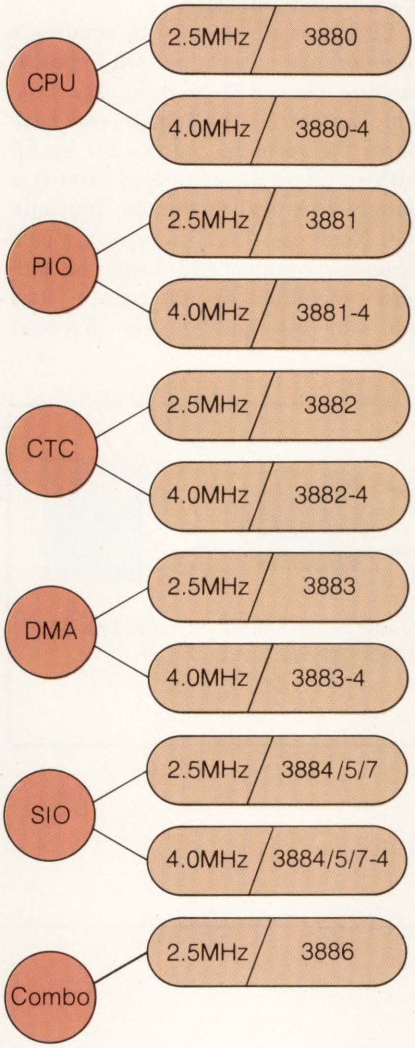
1 Now you can choose.

The choice? 2.5MHz or 4.0MHz parts from a full product line that includes the SIO and DMA. But other reasons to pick Mostek's Z80 family are equally impressive.

First of all, the Mostek Z80 is recognized and accepted as the industry's foremost 8-bit microprocessor. It's a proven design that's been in volume production for several years.

Then there's the inherent design advantages over the 8085: 158 instructions vs. 80. Fourteen 8-bit CPU registers vs. 7. Ten addressing modes vs. 7. An automatic dynamic RAM refresh. Enhanced 16-bit arithmetic ability. Automatic prioritization of interrupts instead of a separate control device. The list goes on.

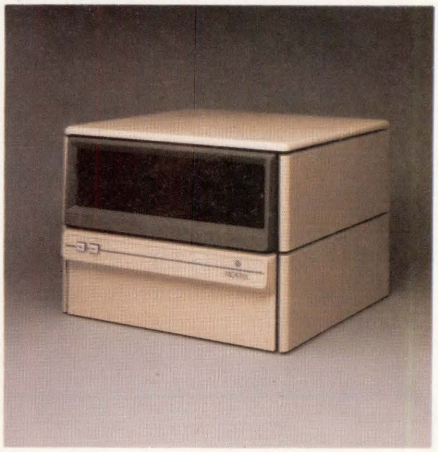




2 A practical solution for lower system cost.

Mostek's Combo™ Chip gives you more versatility with fewer parts. It's ideal for minimum chip configuration designs because this single 40-pin circuit contains 256 bytes of RAM with a low power standby mode for 64 bytes. A serial I/O port. Two programmable timers, one of which can be a programmable baud rate generator. Three external interrupts with a programmable vector for each channel. And, of course, a single +5 Volt power supply. So now you can design a complete system with just 3 chips: a Z80 CPU, ROM, RAM, or EPROM memory, and the Combo Chip.

3 A flexible development system.



Mostek's development support includes a variety of choices ranging from single cards to our Matrix™ floppy disk development system with 4.0MHz real time in-circuit emulation. The Matrix system offers a sophisticated resident software package that uses simple commands and comprehensive error messages to save valuable time during program development and debug. Macro Assemblers, BASIC, and FORTRAN are also available for use on the Matrix development system.

4 For all your Z80 needs.

Mostek's complete Z80 family is available now at your local Mostek distributor. So are factory-trained distributor FAEs and demonstration centers at most locations. Contact them for complete information and/or a product demonstration. Military versions are also available. For more information call or write Mostek, 1215 W. Crosby Road, Carrollton, TX 75006, phone 214/323-6000. In Europe, contact Mostek Brussels; phone 660.69.24.

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CIRCLE 28 ON INQUIRY CARD

Portable Test Set Performs Functional Tests On Data Links

Linktest[R] is an MSI based handheld test set designed for computer room or field isolation of faults in modems, lines, computers, or remote terminals. It operates at asynchronous data rates of 300, 600, 1200, 2400, 4800, 9600, and 19,200 bits/s, and synchronous from 0 to 100k bits/s as determined by the clock from the modem under test. The set is a product of Kapusi Laboratories, 2121 S El Camino Real, San Mateo, CA 94403.

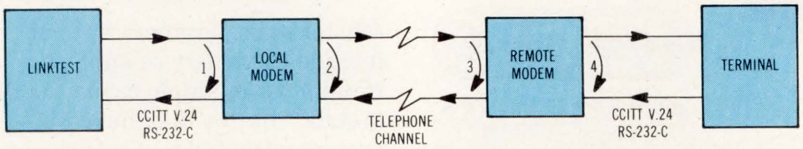
Linktest conforms to CCITT, ICC, EIA, Bell, and ISO specifications, and performs functional testing of the data link by monitoring the RS-232-C/CCITT V.24 modem interface.

Bit errors are counted by sending a pseudorandom bit pattern approximating normal data down the link. The Linktest at the remote end compares the received pattern bit by bit with an internally generated error-free pattern identical to the one transmitted. Numbers of bits in error are continuously counted and displayed. Patterns generated do not contain start and stop bits and are not character oriented; thus, the set is not suitable for testing certain multiplexers.

For bias distortion measurement, useful on asynchronous links, a distortion-free square wave of alternate 1s and 0s is transmitted. Deviations from equal mark/space ratio in the received data pattern are averaged by the test set at the remote end and displayed as percentage bias distortion.

RTS/CTS delay indicates modem turnaround or access time. RTS/CTS readout is up to 999 ms, with ±1 ms resolution and accuracy. Interface monitors indicate status of the modem's control, timing, and data circuits. An integral selftest capability checks out the integrity of the test set. The display is a 3-digit 7-segment high intensity LED display.

Linkabit is powered from the ac lines, 110/220 V, 45-65 Hz. A power line filter provides interference rejection of better than 40 dB at 500 kHz. Dimensions of the portable unit are length, 200 mm; width, 119 mm; and height, 96 mm. Weight is 1.8 kg. A standard 483-mm version for rack mounting is available.



Loop testing using one Linktest. Unit permits local digital (1), local line (2), remote line (3), and remote digital (4) loopback testing

Circle 403 on Inquiry Card

Intelligent Communications Controller Provides DMA Facilities for 32-Bit Systems

DMA I/O Subsystem (DIOS) is a high performance intelligent communications controller for the 32-bit systems family of Perkin-Elmer Corp, Computer Systems Div, 2 Crescent Pl, Oceanport, NJ 07757. These systems include models 7/32, 8/32, and MOS-based 3220 and 3240. The controller provides direct memory access (DMA) facilities between main memory and the company's hardware communications adapters. With DIOS, system throughput is improved and processor degradation minimized because data transfers take place without processor intervention.

Two versions are offered. The first broadens capabilities of the company's recently announced Reliance software package by accommodating asynchronous protocols. It is priced at $6000 (U.S.). Second version, priced at $7500 (U.S.), accommodates asynchronous, character synchronous, and bit-oriented protocols such as SDLC, HDLC, and ADCCP which require zero-bit insertion/deletion. Automatic flag insertion/deletion is also provided.

DIOS fully supports Bisync, enabling higher level data communications software such as 2780/3780 RJE emulation and HASP to operate through it without modification. Data rates are up to 56k baud/line, and peak throughput is 100k char/s.

The controller supports chained or queued buffer handling in a bit-synchronous environment, and also handles device status checking and frame check sequence generation/validation. Used in conjunction with the company's ZDLC channel termination manager software package, DIOS provides a comprehensive high throughput support package for all three industry standard bit-oriented protocols: SDLC, HDLC, and ADCCP.

Circle 404 on Inquiry Card

The new VISUAL 200 terminal has the features of competitive terminals and will code-for-code emulate them as well. A flick of a switch on the rear panel programs the VISUAL 200 for compatibility with a Hazeltine 1500, ADDS 520, Lear Siegler ADM-3A or DEC VT-52. This allows you to standardize on the new, reliable VISUAL 200 for virtually all of your TTY compatible video terminal applications, with no change in the software you've written for the older, less powerful terminals. And you're not limited to mere emulation; you can outperform them at the same time by taking advantage of the additional features and human engineering of the VISUAL 200, such as:

- Detachable Solid State Keyboard
- Smooth Scroll
- Tilt Screen (10° to 15°)
- Large 7 x 9 Dot Matrix Characters
- Others in the Feature Comparison Chart

For a pleasant surprise on prices, call or write us today.

FEATURE COMPARISON CHART

FEATURE	Visual 200	Hazeltine 1500	Hazeltine 1420	Lear Siegler ADM-3A	Digital VT-52	ADDS 520	ADDS Regent 20	ADDS Regent 40
24 x 80 Screen Format	STD	STD	STD	STD	STD	STD	STD	STD
7 x 9 Dot Matrix	STD	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Background/Foreground	STD	STD	STD	**NO**	**NO**	**NO**	**NO**	STD
Insert/Delete Line	STD	STD	**NO**	**NO**	**NO**	**NO**	**NO**	STD
Insert/Delete Character	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Clear End Line/Field/Page	STD	STD	**NO**	**NO**	STD	**NO**	**NO**	**NO**
Blink	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**	STD
Security Mode	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**	STD
Columnar and Field Tab	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**	STD
Line Drawing	STD	**NO**	**NO**	**NO**	STD	**NO**	**NO**	STD
Upper/Lower Case	STD	STD	STD	**OPT**	STD	**NO**	STD	STD
Numeric Pad	STD	STD	STD	**OPT**	STD	**NO**	**NO**	STD
Composite Video	STD	**NO**	**NO**	**NO**	**NO**	STD	**NO**	**NO**
Current Loop	STD	STD	**NO**	**OPT**	**OPT**	STD	STD	STD
Serial Copy Port	STD	STD	**OPT**	STD	**OPT**	**NO**	STD	STD
Hold Screen	STD	**NO**	**NO**	**NO**	STD	**NO**	**NO**	**NO**
Detachable Keyboard	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	STD
Solid State Keyboard	STD	**NO**	**NO**	**NO**	**NO**	**NO**	STD	STD
Typamatic Keys	STD	STD	STD	**NO**	**NO**	**NO**	STD	STD
Cursor Addressing	STD	STD	STD	STD	STD	STD	STD	STD
Read Cursor Address	STD	STD	STD	**NO**	**NO**	**NO**	**NO**	STD
Cursor Control Keys	STD	**NO**	STD	**NO**	STD	**NO**	**NO**	STD
Secondary Channel	STD	**NO**	**NO**	STD	**NO**	STD	**NO**	**NO**
Self Test	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**	STD
Baud Rate to 19,200	STD	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**
Smooth Scroll	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Microprocessor	STD	STD	STD	**NO**	STD	**NO**	STD	STD
Tilt Screen	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Switchable Emulations	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**

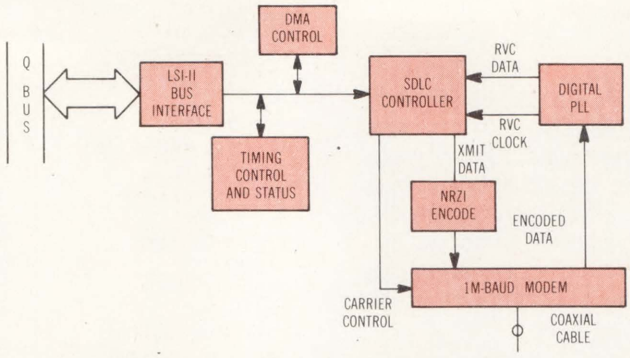
The new VISUAL 200 obsoletes competitive terminals without obsoleting the software.

VISUAL See for yourself

Visual Technology Incorporated
Railroad Avenue, Dundee Park, Andover, MA 01810
Telephone (617) 475-8056

CIRCLE 29 ON INQUIRY CARD

Q-bus Compatible Interface Enables High Speed DMA Transfer in LSI-11 Networks



Megalink 11-0011 system block diagram. LSI bus interface and control logic provide access to Q-bus, control system operation, and control interrupts. DMA address and word count registers allow buffer area of 32,767 words max. SDLC controller hardware performs data encoding and decoding, address checking, and error checking. Digital PLL recovers receive clock from data stream to time data into registers

1M-bit/s DMA block transfers among as many as 255 LSI-11 microprocessors over a single coaxial cable up to 32,000 ft (9754 m) long are permitted by the model 11-0011 Megalink Q-bus compatible interface. The processor network can be operated half duplex in point to point or multidrop partyline configuration. The unit, packaged on two standard 8.5 x 5" (21.6 x 12.7cm) half-quad boards, plugs directly into LSI-11 backplanes. It is available from Computrol Corp, 15 Ethan Allen Hwy, Ridgefield, CT 06877.

Bus interface chip set, DMA controller, SDLC protocol generator/stripper, phase lock loop (PLL), and gated carrier (3 MHz) FSK modem comprise the hardware (see Figure). SDLC protocol, being implemented in hardware, requires no program intervention for protocol and control functions.

Data format is 8-bit byte, and block check is by CRC-16 polynomial. Error checking and recovery are provided by the protocol at primary and secondary stations. The computer can retransmit on error, or request retransmission. NRZI with bit stuffing is the encoding technique.

Connection to the coaxial line is via a BNC T-connector. Maximum data transfer distance varies with coaxial line types: RG-59, 5000 ft (1524 m); RG-11 foam, 12,000 ft (3658 m); and JT-3750J, 32,000 ft (9754 m). Power requirements are 5 V at 1.5 A and 12 V at 50 mA.

Circle 405 on Inquiry Card

SIEMENS

Printers should be seen and not heard.

For applications where carbons are not required, Siemens' Ink-Jet Printer should be your only choice.

Ink-Jet Printers are much quieter and faster than impact printers. Whereas conventional impact printers make as much noise as a busy traffic street (about 85 dB), the Siemens Ink-Jet Printer is as quiet as a library (about 50 dB). Therefore, for many applications our Ink-Jet Printer is the obvious choice.

No other Ink-Jet Printer can compare with the Siemens PT80i in reliability and cost-effectiveness. It provides high quality bi-dimensional printing in a variety of type styles, at 270 CPS.

The addition of an extended interface lets you externally connect network selectors, data sets, and storage devices such as floppy disks. The PT80i also features automatic testing for 96 characters with two test programs and LED displays.

Choose the complete terminal in a variety of platen widths, paper feeds, and configurations ...or the module alone...or the Ink-Jet Print Head with support electronics.

For the full story, quietly told, contact Siemens soon.

Conventional impact printers are 85 dB noisy.

The Siemens Ink-Jet Printer is 50 dB quiet.

District Offices:

Boston, MA	(617) 449-3450
Iselin, NJ	(201) 494-1000
Chicago, IL	(312) 671-2810
Dallas, TX	(817) 461-1673

Siemens Corporation
OEM Data Products Division
240 East Palais Road
Anaheim, California 92805
(714) 991-9700

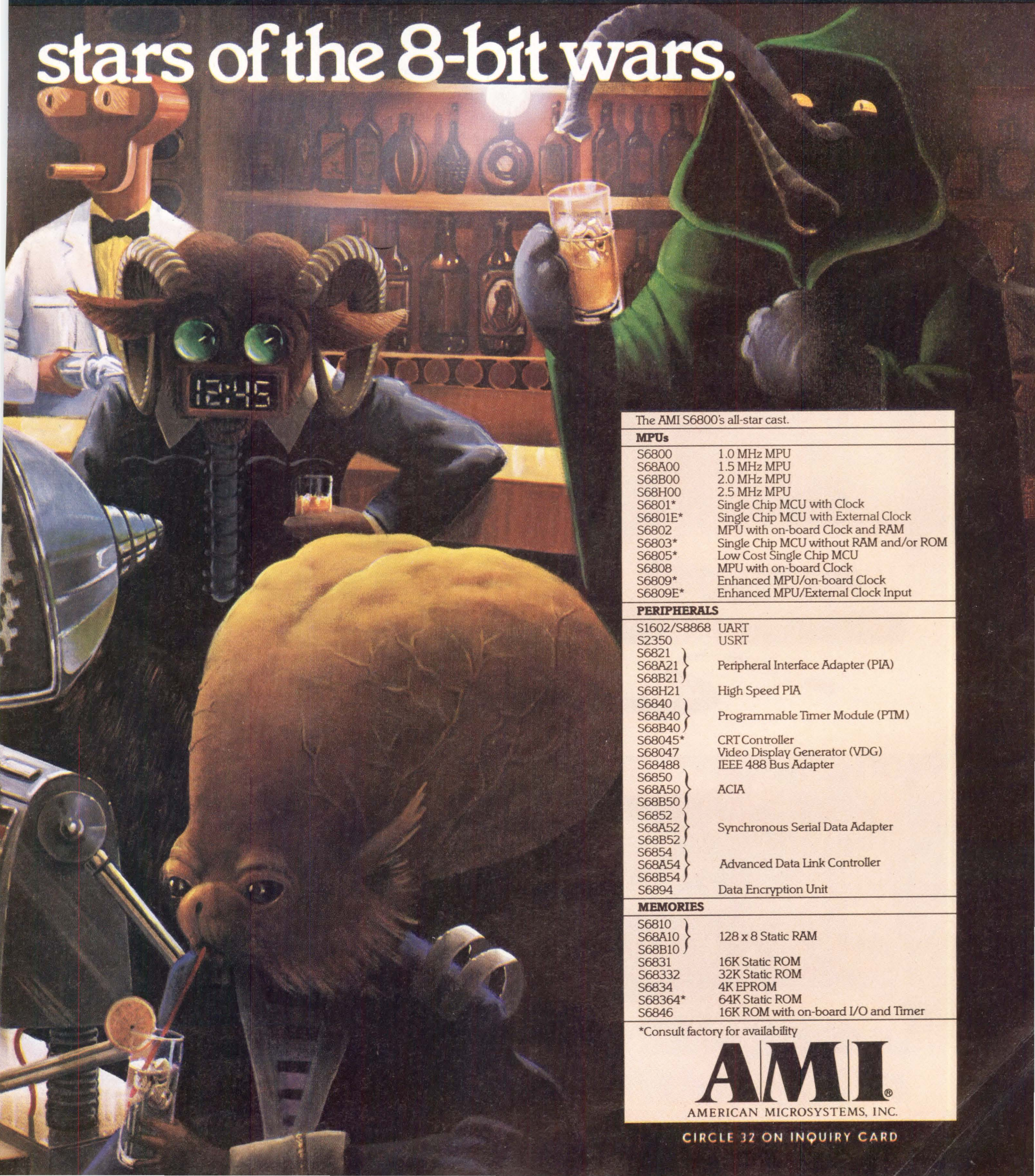
Siemens. The technology to do more.

CIRCLE 31 ON INQUIRY CARD

S6800 system, including both standard and custom parts. Perhaps even customizing the MPU.

So let's put our heads together and find the best way to control your product without putting your budget into orbit. Call up your nearest AMI distributor. Or contact us at AMI S6800 Marketing, 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330.

However far-out your plans are, our family will make light work of them.



The AMI S6800's all-star cast.

MPUs	
S6800	1.0 MHz MPU
S68A00	1.5 MHz MPU
S68B00	2.0 MHz MPU
S68H00	2.5 MHz MPU
S6801*	Single Chip MCU with Clock
S6801E*	Single Chip MCU with External Clock
S6802	MPU with on-board Clock and RAM
S6803*	Single Chip MCU without RAM and/or ROM
S6805*	Low Cost Single Chip MCU
S6808	MPU with on-board Clock
S6809*	Enhanced MPU/on-board Clock
S6809E*	Enhanced MPU/External Clock Input
PERIPHERALS	
S1602/S8868	UART
S2350	USRT
S6821, S68A21, S68B21	Peripheral Interface Adapter (PIA)
S68H21	High Speed PIA
S6840, S68A40, S68B40	Programmable Timer Module (PTM)
S68045*	CRT Controller
S68047	Video Display Generator (VDG)
S68488	IEEE 488 Bus Adapter
S6850, S68A50, S68B50	ACIA
S6852, S68A52, S68B52	Synchronous Serial Data Adapter
S6854, S68A54, S68B54	Advanced Data Link Controller
S6894	Data Encryption Unit
MEMORIES	
S6810, S68A10, S68B10	128 x 8 Static RAM
S6831	16K Static ROM
S68332	32K Static ROM
S6834	4K EPROM
S68364*	64K Static ROM
S6846	16K ROM with on-board I/O and Timer

*Consult factory for availability

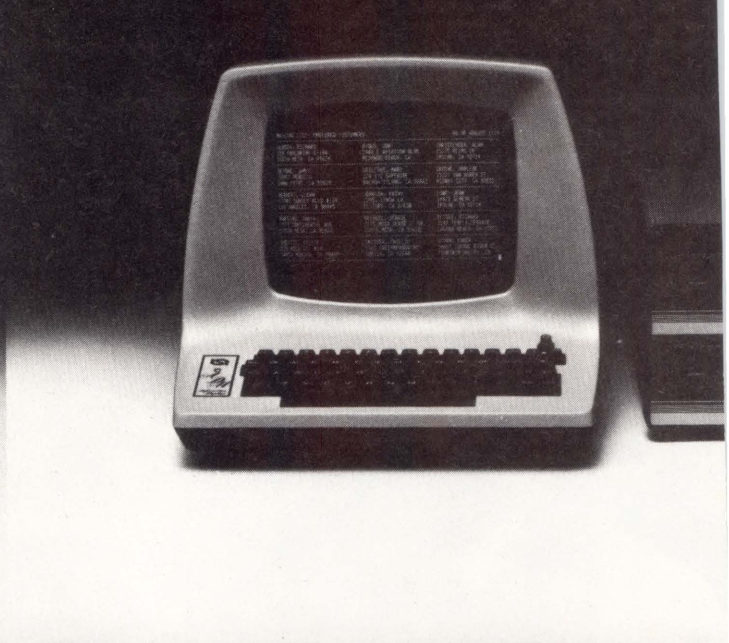
AMI®

AMERICAN MICROSYSTEMS, INC.

CIRCLE 32 ON INQUIRY CARD

SOPHISTICATED GRAPHICS TERMINAL

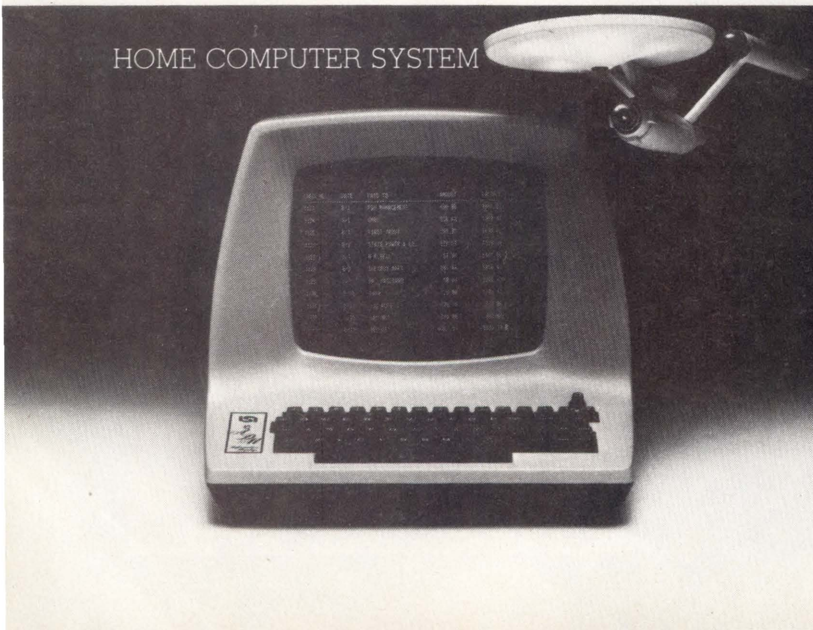
SMALL BUSINESS SYSTEM



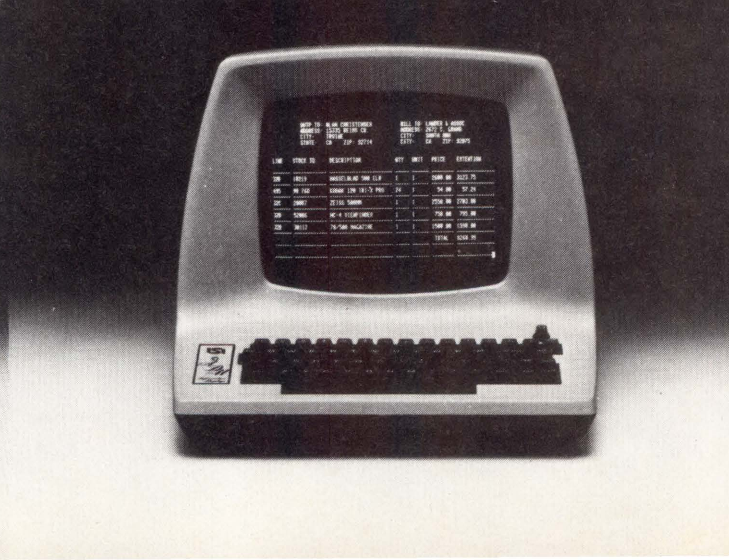
INVENTORY CONTROL

PORTABLE I/O DEVICE

HOME COMPUTER SYSTEM



VERSATILE DATA TERMINAL



What could anyone possibly do with 85,000 Dumb Terminals®?

That's how many ADM-3A's there are out in the field working right now. And more being shipped each day. Now just what accounts for such remarkable popularity?

Sure, it's the definitive dumb terminal, adaptable enough to fit a host of applications. It has a 12-inch diagonal screen. Full or half duplex operation at 11 selectable data rates. 1920 easy-to-read characters in 24 rows of 80 letters. 59 entry keys. An RS232C interface extension port. And direct cursor addressing.

But we wondered if all 85,000 Dumb Terminals were being used for just everyday data entry. So we checked around.

And found that people are using Dumb Terminals for things even we never thought of.

THE ADM-3A GOES INTO BUSINESS.

More and more OEM's are putting the Dumb Terminal into small business systems. They assemble a package that usually contains a disk, memory, a printer, and a video display terminal — the adaptable ADM-3A.

So the chances are that when you buy a small business system from someone, it'll contain, you guessed it, the amazing Dumb Terminal.

IT TAKES STOCK OF THE SITUATION.

Many businesses are using the Dumb Terminal, along with a light pen (Universal Product Code Decoder), to keep track of their inventory. The decoder is interfaced to the Dumb Terminal, and when a piece of merchandise imprinted with a Universal Product Code passes under it, the item is entered into a computer for tallying.

Simultaneously, the item is also displayed on the ADM-3A's screen — so it's instantly available for quick double-checking.

PROGRAMMERS LIKE IT, TOO.

Surprisingly enough, many computer programmers use the ADM-3A as an effective, portable I/O device. They can take it into a back room or, along with an acoustic coupler, to their homes if they wish, and compile programs nearly anywhere.

By using telephone lines, they can have direct access to a computer. Or, with the addition of an inexpensive cassette, the programmer can store the program on tape and enter it into the mainframe at a later date — with no loss of data.

THE DUMB TERMINAL PUTS ON A NEW FACE.

Some of our more ambitious customers have transformed their ADM-3A's into sophisticated graphics terminals. Simply by installing another PCB, they've enabled their terminals to perform complex plotting, graphics, and even draw charts.

And the Dumb Terminal is so adaptable that these industrious people had no trouble with installation — the graphics PCB required not the slightest cutting or soldering. It simply slipped right in and started working, all in a matter of minutes.

YOU CAN EVEN TAKE IT HOME TO MEET THE FAMILY.

We discovered that many computer buffs are using the Dumb Terminal as an inexpensive way to upgrade their systems. After all, the equipment found on most microcomputers leaves a lot to be desired. Such as the tiny five or six-inch screen, for instance.

By upgrading to the ADM-3A, they get a full 12-inch screen that's easy on the eyes. Not to mention a lot of capabilities they wanted, but just didn't get on their systems.

All for only $895.

THE DUMB TERMINAL. THE HALLMARK OF VERSATILITY.

When you get right down to it, the Dumb Terminal's applications are pretty amazing.

It can be interfaced with a staggering variety of RS232 devices. Such as cassettes, disks, floppy disk drives, printers, paper tapes, and readers, to mention just a few.

In fact, the ADM-3A is compatible with just about any RS232 device you can name. Even other video terminals, if you wish.

And people call this a "dumb" terminal?

WHAT WILL THEY THINK OF NEXT?

Who knows? But it seems that as long as there are Dumb Terminals, people will find new, unsuspected uses for them.

Of course, the ADM-3A will continue to be the same dependable data entry terminal that's made it an industry legend.

With good, reliable features and a minimum of frills. Nothing could change that. The fact is, we think that's probably the main reason that so many people have come up with so many uses for the ADM-3A.

Who said you can't teach a Dumb Terminal new tricks?

Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803. (800) 854-3805. In California (714) 774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices: San Francisco (408) 263-0506. Los Angeles (213) 454-9941. Chicago (312) 279-5250. Houston (713) 780-2585. Philadelphia (215) 968-0112. New York (212) 594-6762. Boston (617) 423-1510. Washington, D.C. (301) 459-1826. England (4867) 80666.

DUMB TERMINAL SMART BUY

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

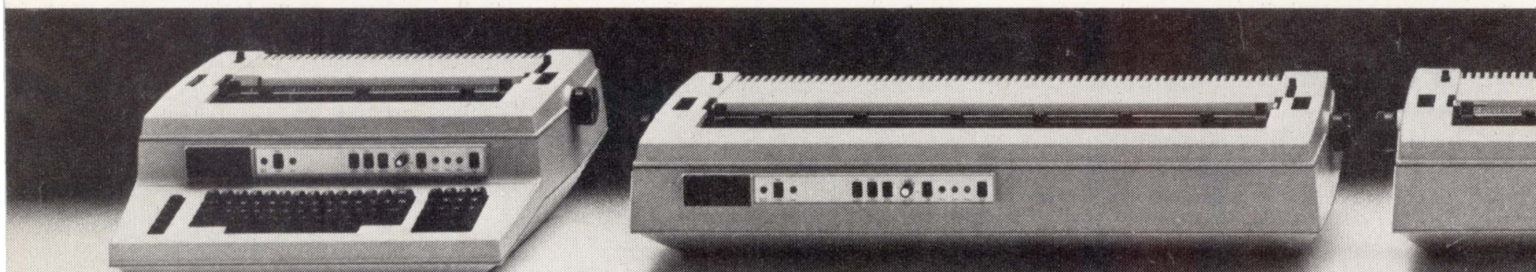
CIRCLE 33 ON INQUIRY CARD

Introducing the Family Plan from Qume.

We've developed a simple plan to help you enhance your system. Or to make you more successful at selling them if you're an OEM. Just rely on Qume's entire family of letter-perfect printers, terminals, memory devices and printing supplies. With it, you can be sure you're using the highest-quality products available.

The world's leading word processor printers.

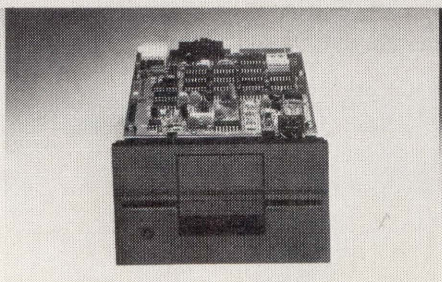
Qume's Sprint Micro 3,™ a third-generation daisywheel printer, sets the standards for quality printing and in-use reliability. Available in 35, 45 and 55 CPS speeds, there are no faster daisywheel printers in the world.



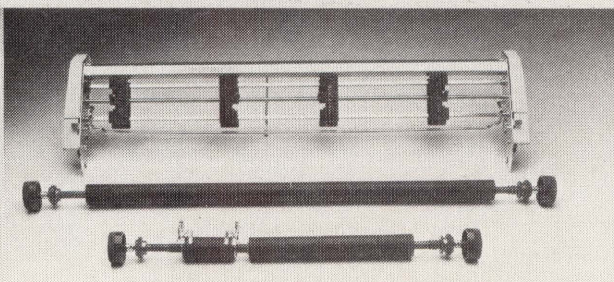
Sprint 5™

Sprint 5 WideTrack™

DataTrak 8™



DataTrak 5™



Platens & Forms Tractors

Our Sprint 5™ data terminal is a letter-perfect direct descendant of the Sprint Micro 3. The Sprint 5 features an RS-232C Serial interface and a full ASCII keyboard, and has achieved a reputation for being the easy-to-use leader in letter-perfect terminals.

We widen your horizons.

Now, Qume can take you a step wider with our 264-column wide printers. Select from either the WideTrack,® with parallel interface; or our newest member, Sprint 5 WideTrack,™ with RS-232C Serial interface; the TwinTrack,® with dual-headed printing capabilities, is still unmatched in the industry.

We're a well-fed family.

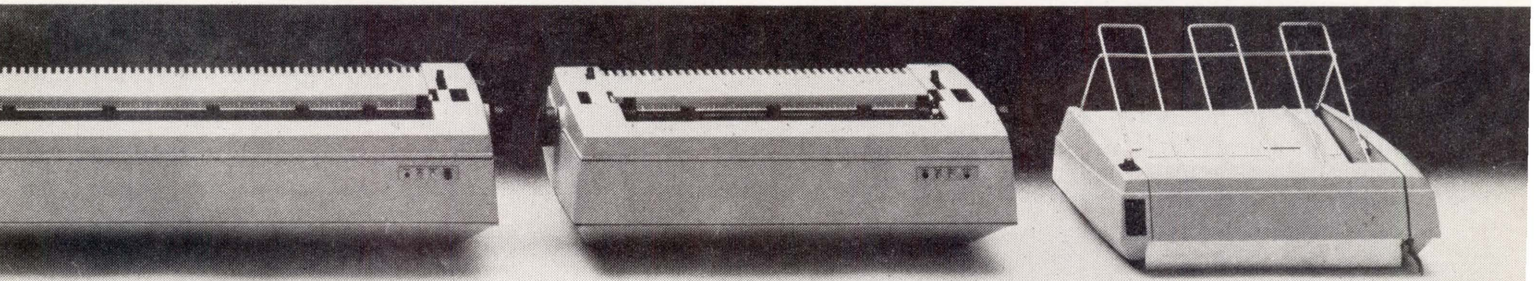
We manufacture one of the widest accessory lines in the business. Ranging from our industry-leading SpeedFeed® single-sheet feeder to special platens and paper-handling devices. We manufacture the world's most complete line of daisywheels and ribbons; 94 economical plastic printwheels in 30 typestyles and 12 languages. And we also manufacture 20 different types of high-quality ribbons in a variety of colors.

Unforgettable memories.

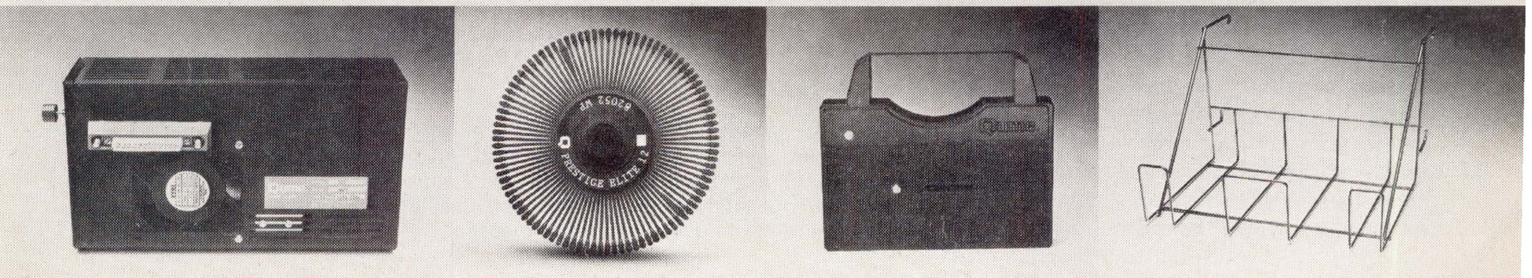
Qume's commitment to quality extends into another very important area: memory products. And it's here that the name DataTrak™ stands out. DataTrak 8 and DataTrak 5 are dual-sided, dual-density floppy disk drives that provide high data reliability without media wear.

Whether you're an OEM or a dealer, you can have a lot more going for you in today's competitive business world when you follow Qume's family plan and use our entire family of products. For more information, just contact Qume at 2350 Qume Drive, San Jose, California 95131. Telephone: (408) 942-4000. TWX: 910-338-0232.

Qume®



TwinTrack® | Sprint Micro 3™ | SpeedFeed®



Power Supplies | Printwheels | Ribbons | Paper Handling Accessories

CIRCLE 34 ON INQUIRY CARD

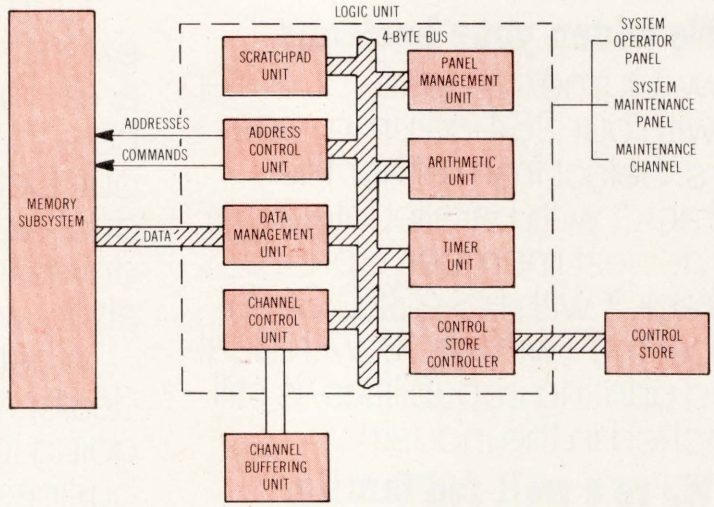
Medium Scale Computer System Offers Onsite Performance/Capacity Upgrades

Flexibility and configurability inherent in the Level 64/DPS-330 medium scale computer provide for three levels of instruction execution speeds, memory sizes from 512k to 2048k bytes, and various peripheral and communications subsystems. The system, introduced by Honeywell, United States Information Systems Group, 200 Smith St, Waltham, MA 02154, increases central processor efficiency through the use of extensive microprogramming, integrated mass storage and unit record processors, and an integrated communications controller.

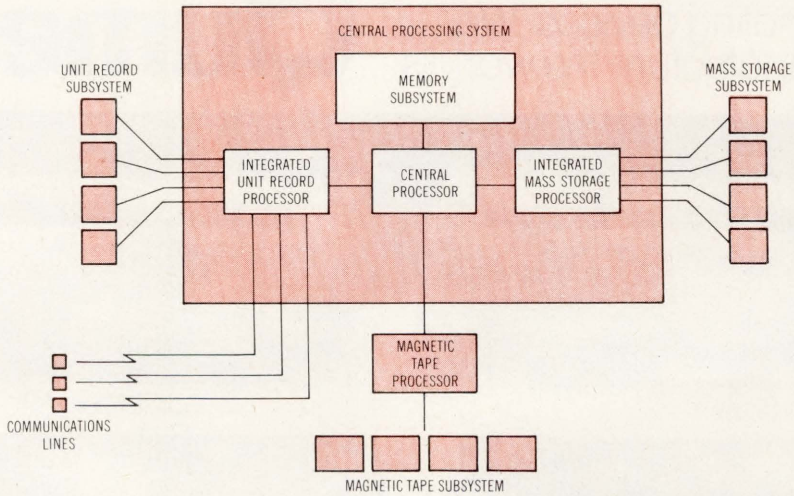
Software overhead is reduced and instruction execution is increased through replacement of hardwired or programmed logic with firmware microcode. This firmware also facilitates architectural concepts such as process synchronization and ring protection to automatically control the execution of concurrently running jobs and to prevent interference between them. Functionally separate peripheral processors, each having its own memory, firmware, microcode, and logic units, free the CPU for other internal processing concurrent with executing peripheral and communications activities. The system's communications capabilities are implemented by up to three communications controllers, each capable of supporting as many as 15 synchronous and/or asynchronous lines.

A basic system consists of central processor, 512k bytes of memory, mass storage processor with addressing for two disc units, unit record processor, communications controller, two I/O channels for mass storage and unit record processors, and freestanding console with CRT and keyboard. Processing capability is distributed between the central processor subsystem and up to seven peripheral subsystems, which operate asynchronously with the central processor subsystem and with each other for maximum throughput.

Central processor subsystem consists of memory subsystem and central



DPS-330 central processor consists of control store and channel buffering unit. Logic unit is formed of eight separate asynchronous units grouped together. Logic unit can execute up to five microinstructions in parallel in total of 315 ns



Processing capability of Honeywell's Level 64 DPS-330 is distributed between the central processor subsystem and up to seven peripheral processors, which operate asynchronously with CPU and with each other. CPU subsystem consists of memory subsystem and CPU. Each class of peripheral devices is controlled directly by its own peripheral processor

ROLM'S 1602B: An Army Standard Computer Designed for Full Integrated Logistics Support

IT'S A COMPLETE PROCESSOR IN A SINGLE 20″ CHASSIS.

The 1602B (AN/UYK-19) has space for 7 I/O modules, control panel interface, CPU and 64K of directly addressable memory. An additional 15 I/O slots can be made available with ROLM's 2150 Expansion Chassis.

IT HAS SINGLE SIDED ACCESS.

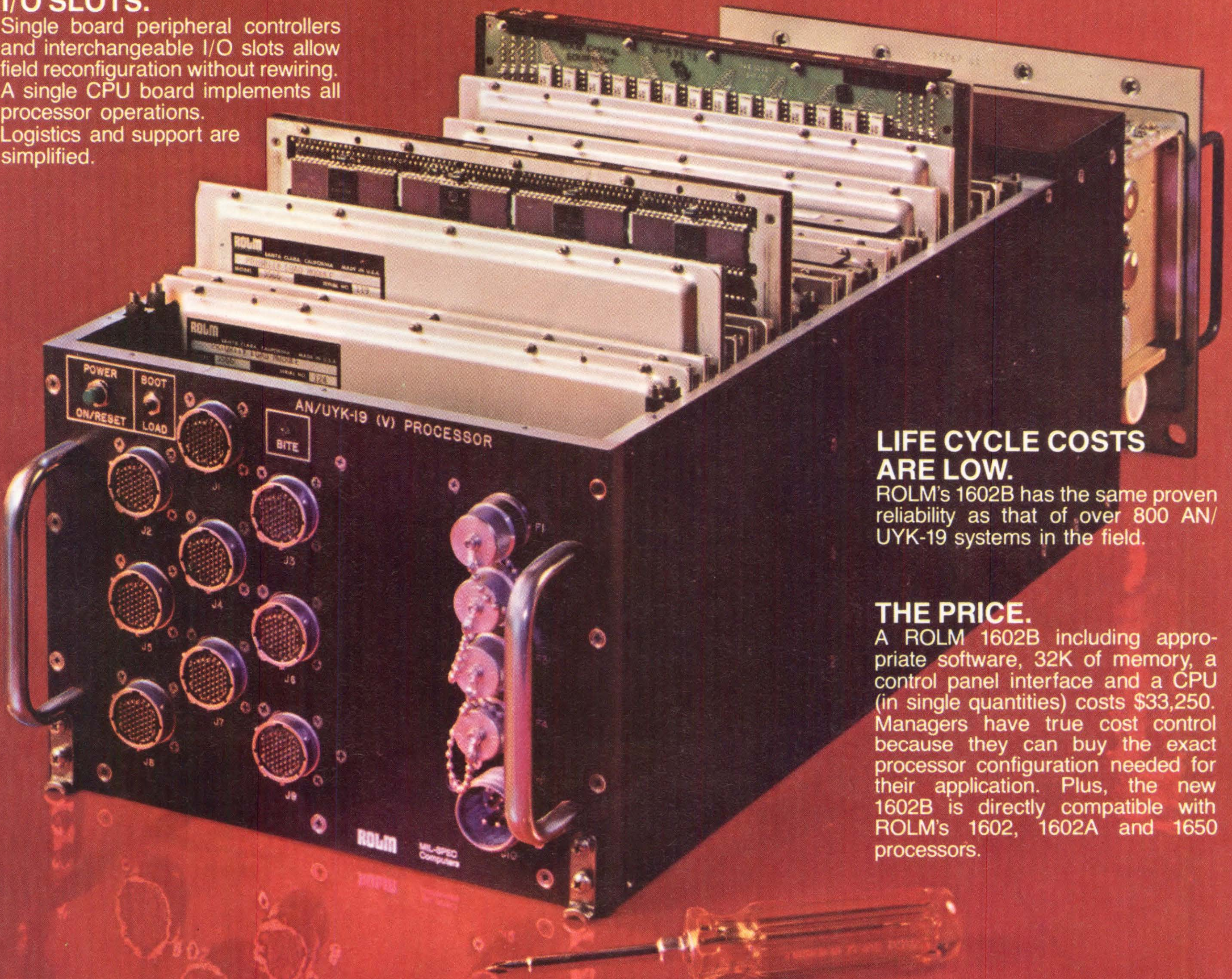
Maintenance is simplified by quick, easy access to the interior of the conductively cooled chassis. The 1602B also has a new plug-in AC or optional DC power supply.

EXCELLENT DELIVERY WITH FULL SUPPORT.

Since AN/UYK-19 processors are in continuous production, delivery is no problem. They are fully mil-qualified and backed up by complete training and documentation. And ROLM's extensive software has really impressed program managers. They find that our total support program can't be matched.

INDEPENDENT CARDS & INTERCHANGEABLE I/O SLOTS.

Single board peripheral controllers and interchangeable I/O slots allow field reconfiguration without rewiring. A single CPU board implements all processor operations.
Logistics and support are simplified.



LIFE CYCLE COSTS ARE LOW.

ROLM's 1602B has the same proven reliability as that of over 800 AN/UYK-19 systems in the field.

THE PRICE.

A ROLM 1602B including appropriate software, 32K of memory, a control panel interface and a CPU (in single quantities) costs $33,250. Managers have true cost control because they can buy the exact processor configuration needed for their application. Plus, the new 1602B is directly compatible with ROLM's 1602, 1602A and 1650 processors.

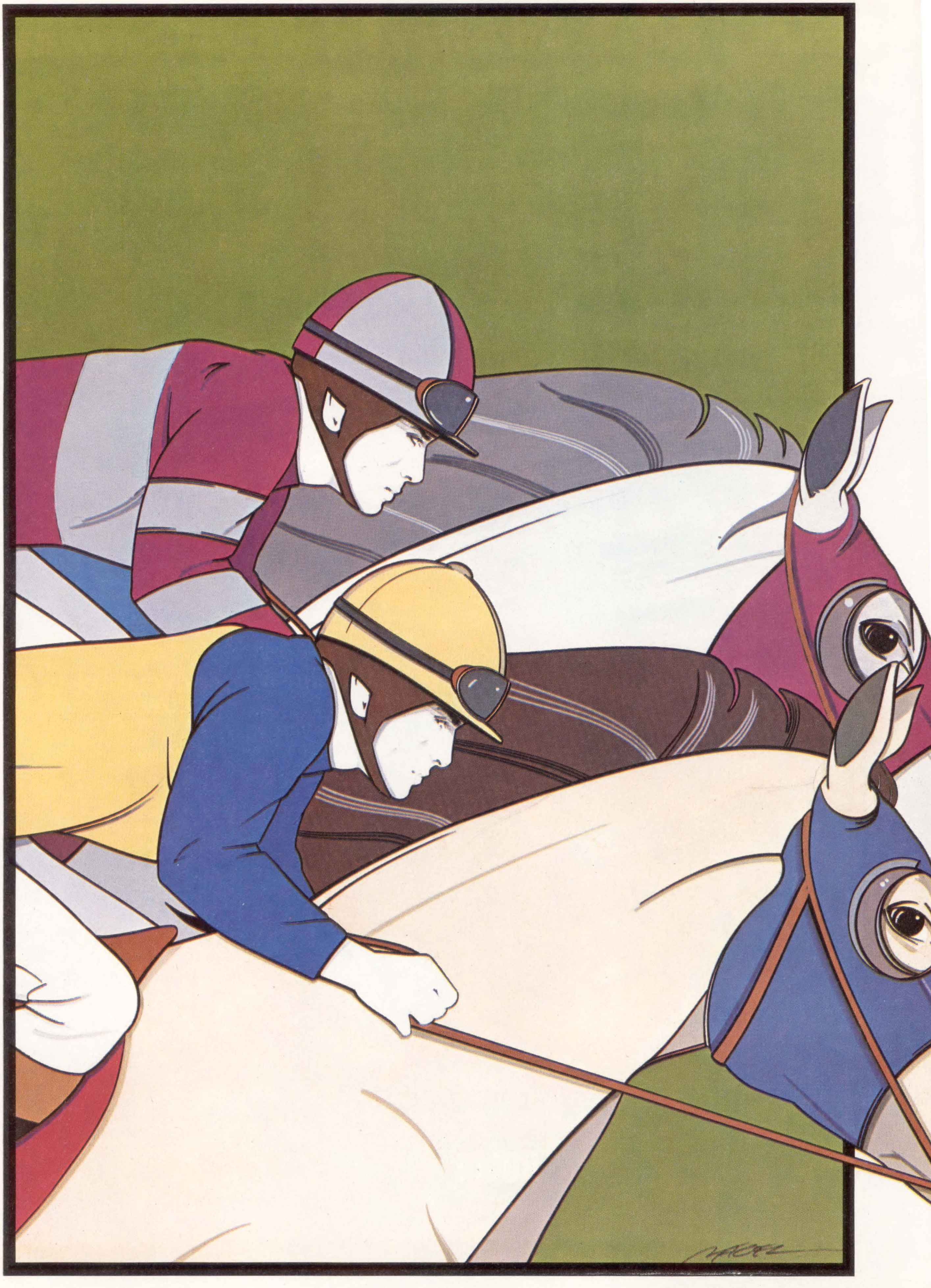
That's Why We're #1 in Mil-Spec Computer Systems

ROLM MIL-SPEC Computers

4900 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-2900. TWX 910-338-7350.

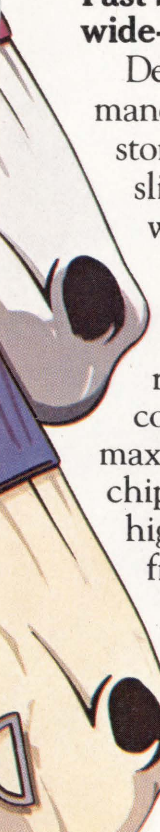
In Europe: Muehlstrasse 19 D-6450, Hanau, Germany, 06181 15011, TWX 4-184-170.

CIRCLE 35 ON INQUIRY CARD



Two New Winners

Take the lead with Intel's two new 4-bit wide fast static RAMs, our 45ns 2149H and our 55ns 2148H. Either way, you win.



There's a fast new pace in wide-word memory, and Intel's two new 1Kx4-bit static RAMs are way out in front. Introducing the high speed, lower power 2148H and the fast chip select 2149H. They're both products of Intel's HMOS II technology and both are high performance descendants of our industry standard 4K x 1-bit 2147H. Best of all, Intel's track record in static RAMs assures you of the quality, reliability, economy and delivery you need for today's competitive system designs.

Fast break for wide-word designs

Designers of high performance writeable control store, cache, buffer and bit slice processor memories will appreciate both these new 4-bit-wide devices. Intel's 2149H delivers the fastest response ever in a TTL-compatible 1Kx4—45ns maximum access with 20ns chip select. It's the logical, high performance upgrade from 1K designs, delivering higher density, lower power and a lower parts count.

For power sensitive applications, use the 55ns 2148H. Like the 2147H, the 2148H provides automatic power down on chip deselection. With maximum power consumption as low as 125mA active/20mA standby.

2148H/2149H 1K x 4 STATIC RAMs

Part Number	Address Access Time (t_{AA})	Chip Select Access Time (t_{ACS})	Current Active/Stby
2149H-2	45ns	20ns	180mA
2149H-3	55ns	25ns	180mA
2149HL-3	55ns	25ns	125mA
2149H	70ns	30ns	180mA
2149HL	70ns	30ns	125mA
2148H-3	55ns	55ns	180mA/30mA
2148HL-3	55ns	55ns	125mA/20mA
2148H	70ns	70ns	180mA/30mA
2148HL	70ns	70ns	125mA/20mA

Both the 2148H and 2149H are 18-pin, 5-volt devices, so you're totally compatible with memories like our 1Kx4 industry standard 2114A and 2148 RAMs. Whichever of these new fast statics you choose, you're sure to improve performance: higher speeds, lower power, and simpler designs.

HMOS II for the competitive edge

For years, Intel's HMOS* technology has produced high performance, highly reliable 1K and 4K RAMs. Today, over 50 Intel® HMOS static RAMs give system designers the largest selection of microprocessor and main memory components in the industry. We've already delivered over 18 million of these producible, field-proven HMOS devices, including our industry standard microprocessor, the 8086. Now HMOS II* has arrived, delivering even higher performance, and reliability statistics just as impressive as HMOS.

Pull ahead today

Intel's new 2148H and 2149H are in volume production and on distributor shelves today. So are data sheets and our new HMOS II Reliability Report, #RR26. To get a head start on your competition, contact your local Intel sales office or distributor. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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*HMOS and HMOS II are patented processes of Intel Corporation.

processor unit (CPU). Each class of peripheral devices is controlled directly by its own specialized peripheral processor. The 512k bytes of main memory included in the central system can be increased in three steps to 2048k bytes using two 256k-byte and one 1024k-byte memory module; maximum expansion requires a memory expansion unit and power upgrade module.

The CPU consists of control store—eight separate asynchronous units grouped together to form the logic unit—and a channel buffering unit for I/O control. The byte oriented CPU can handle byte, half-word, word, double-word, and quad-word data formats. Its instruction set provides instructions for handling fixed point binary, packed and unpacked decimal, byte strings, bit strings, and long and short floating point binary code. Adding two power modules increases instruction execution speed of the basic system 1.55 and 2.3 times.

Control store, bipolar ROM with an access time of 100 ns/4 byte word, stores CPU firmware. The logic subunit can execute up to five microinstructions in parallel in a total of 315 ns. I/O microprograms are separate from those of the CPU and are graded to give precedence to high speed devices.

Peripheral processors, connected to the CPU by high speed I/O channels, eliminate the need for CPU management of I/O operations after they have been initiated. A channel buffering unit that connects to the channel control unit provides 16-byte buffers between each channel and the CPU. Channel transfer rate on each of the two integrated I/O channels (expandable to 12) is 1250k bytes/s. These channels are occupied by the two peripheral processors. Additional channels allow one or two optional magnetic tape processors and two mass storage processors to be attached.

Peripheral processors are microprogrammed and include read only storage, read/write memory, an arithmetic and logic unit, and maintenance panel. Microprogrammed functions can be executed at the peripheral subsystem level considerably reducing CPU busy time for I/O operations.

Up to three data communications controllers attach to the system, controlling up to 15 lines, allowing mixes of synchronous and asynchronous transmission modes at line speeds from 45 to 19,200 bits/s. One controller comes with the integrated unit record processor, the second and third attach to the second unit record processor. Each line can handle 32 terminals, polling them automatically as well as performing automatic transmission error detection and retry operations.

Batch processing, transaction processing, distributed processing, and interactive timesharing are supported by the Level 64 GCOS operating system which features COBOL, FORTRAN, RPG, and BASIC language processors, TDS/64 transaction processing system, and I-D-S/II, a CODASYL compatible data base management system. Interactive capabilities and ease of use are enhanced with immediate step activation to provide interactive execution of COBOL, FORTRAN, and RPG language processors, the linker and user object programs and interactive program checkout facility for interactive program debugging from a terminal. Preforms permits the creation, modification, and storage of formats for VIP 770 and 7760 visual display terminals. Multiple logic data store (MLDS) provides an indexed access method for easy transition from System/3 computers to the Level 64/DPS, and can serve as an entry level database management product.

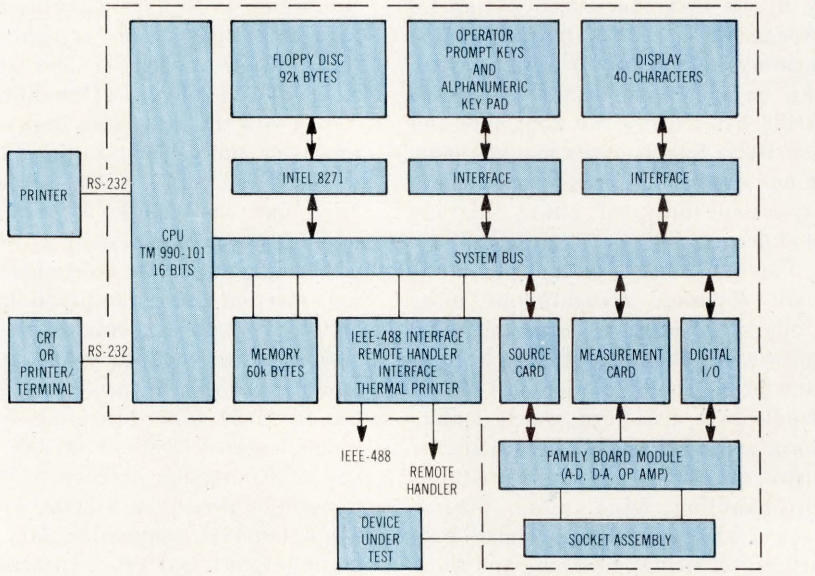
Purchase price of the basic DPS-330 with 512k-bytes memory, two I/O channels, two peripheral processors, one communications controller, and free-standing console with CRT is $79,675. The 256k memory expansion module is priced at $7500; a 1M-byte memory module sells for $30,000.

Circle 280 on Inquiry Card

Benchtop Test System Handles ADCs/DACs, And Linear Amplifiers

LTS 2000 automatically tests A-D and D-A converters, and other analog functions such as operational amplifiers, comparators, voltage regulators, isolation amplifiers, and CMOS switches. In the system, Analog Devices, Inc, Rt 1 Industrial Pk, Norwood, MA 02062, has provided capability for statistical analysis with printout or display of test results, and additional communication through an IEEE-488 controller.

Devices are interfaced to the system through family boards and socket assemblies. Family boards contain all circuitry necessary to measure a general class of components. Socket assemblies which interface specific devices with the system and family boards plug directly into the machine. Designed for easy configuration, setting up the socket requires no soldering, only connection of a few jumpers, as a connector is included. An automatic handler interface provides necessary handler control signals.



Analog Devices' programmable benchtop test system uses plug-in family board modules to provide capability for parametric testing on A-D or D-A converters as well as linear operational amplifiers. Integral 16-bit microprocessor and memory allow unit to perform statistical analysis on test results. IEEE-488 interface provides communications capability

To operate the system, the operator inserts a device, presses a button, and a pass-fail message appears on the 40-char dot matrix display. Grading, selection, and binning messages can be displayed as well, and/or printed on the integral 20-column thermal printer.

System hardware consists of a 16-bit microcomputer, the Texas Instruments TM-990, 4k-bytes EPROM, 60k-bytes RAM, and system power supply. A BASF 5.25" (13.33-cm) single-sided floppy disc provides 92k bytes of storage, sufficient for 300 devices. Also standard are the integral 20-column thermal printer, 40-character dot matrix display, alphanumeric keypad, IEEE-488 controller capability, bidirectional RS-232 port, and unidirectional RS-232 port. Optional equipment for the system includes Texas Instruments' 132-col model 820 KSR bidirectional 9 x 7 dot matrix printer and the Perkin-Elmer model 550 Bantam CRT terminal.

The machine is configured with either a fill-in-the-blanks programming method with complete prompting or with supplied programs. Test supervisors can within minutes select order and number of all test parameters from the menu and set up the system from the keyboard. Entered items may include test parameters and test limits as well as statistical analysis to provide displayed or printed tables, graphs, or histograms.

Software controlled voltage sources are used to generate test levels on measured devices. Automatic calibration and internal accuracy of 16 bits permits testing to 12-bit accuracy (or $\pm 0.01\%$) for A-D and D-A converters and op amps; all values are software corrected. In addition, device resolutions up to 16 bits can be tested. Automatic self-calibration occurs every hour; users may recalibrate on manual command.

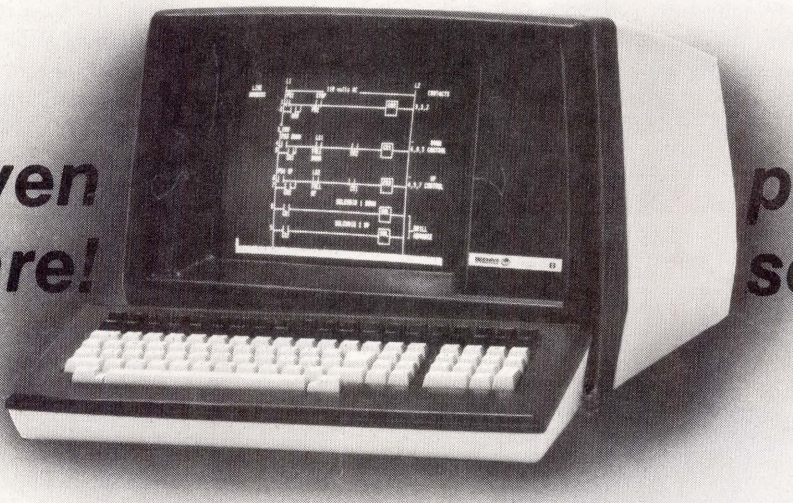
An optional calibration interface board used in conjunction with a Hewlett-Packard 3455 meter controlled through the system's IEEE-488 port permits the user to obtain an NBS traceable calibration. This routine also provides a paper tape readout of errors and their locations. Another error check feature allows the user to stop the system at any test number and probe individual pins with a measuring instrument.

Included in the system's repertoire are capability to test virtually every parameter of interest to the designer. This includes op amp slew to 1000 V/μs and gain bandwidth product to 128 MHz; microprocessor compatible A-D and D-A converters; fabrication technologies including bipolar, CMOS, and IIL; current switching and segment D-A conversion schemes and dual- and quad-slope and successive approximation A-D converters; and A-D comparator indecision.

System price is $25,900 complete in 1-4 quantities, including an op amp family board. D-A and A-D family boards sell for $3000 and $4000, respectively.

Circle 281 on Inquiry Card

Beehive's family of custom OEM terminals



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CIRCLE 39 ON INQUIRY CARD

Cartridge Tape Drives Provide Backup for Small Winchester Discs

Streaming digital cartridge tape accepts data in a continuous nonstop stream to serve as save and restore medium for backing up Winchester technology fixed disc drives having less than 30M-bytes capacity. With capacities of 10M and 20M bytes, the S-3 series drives, manufactured by Data Electronics, Inc, 10150 Sorrento Valley Rd, San Diego, CA 92121, use standard 0.25" (0.635-cm) ANSI/ECMA data cartridges and are physically compatible with industry standard slots for flexible disc drives.

The streaming drive allows essentially all available tape in the cartridge to be used for data storage by eliminating the traditional starting and stopping between data blocks and associated interblock gaps. Elimination of the gaps permits data to be recorded in what appears to be a continuous stream on the tape using a serpentine track arrangement (ie, bidirectional recording with read-while-write checking).

Because this recording technique makes starting and stopping infrequent, tape speed can be increased from 30 to 90 in/s (76 to 228 cm/s) with the resulting transfer rate increasing to 675k bits/s. Streaming also eliminates the necessity for rapid stop/start servo electronics and mechanics. This results in cost savings as well as reduced power requirements and associated heat dissipation.

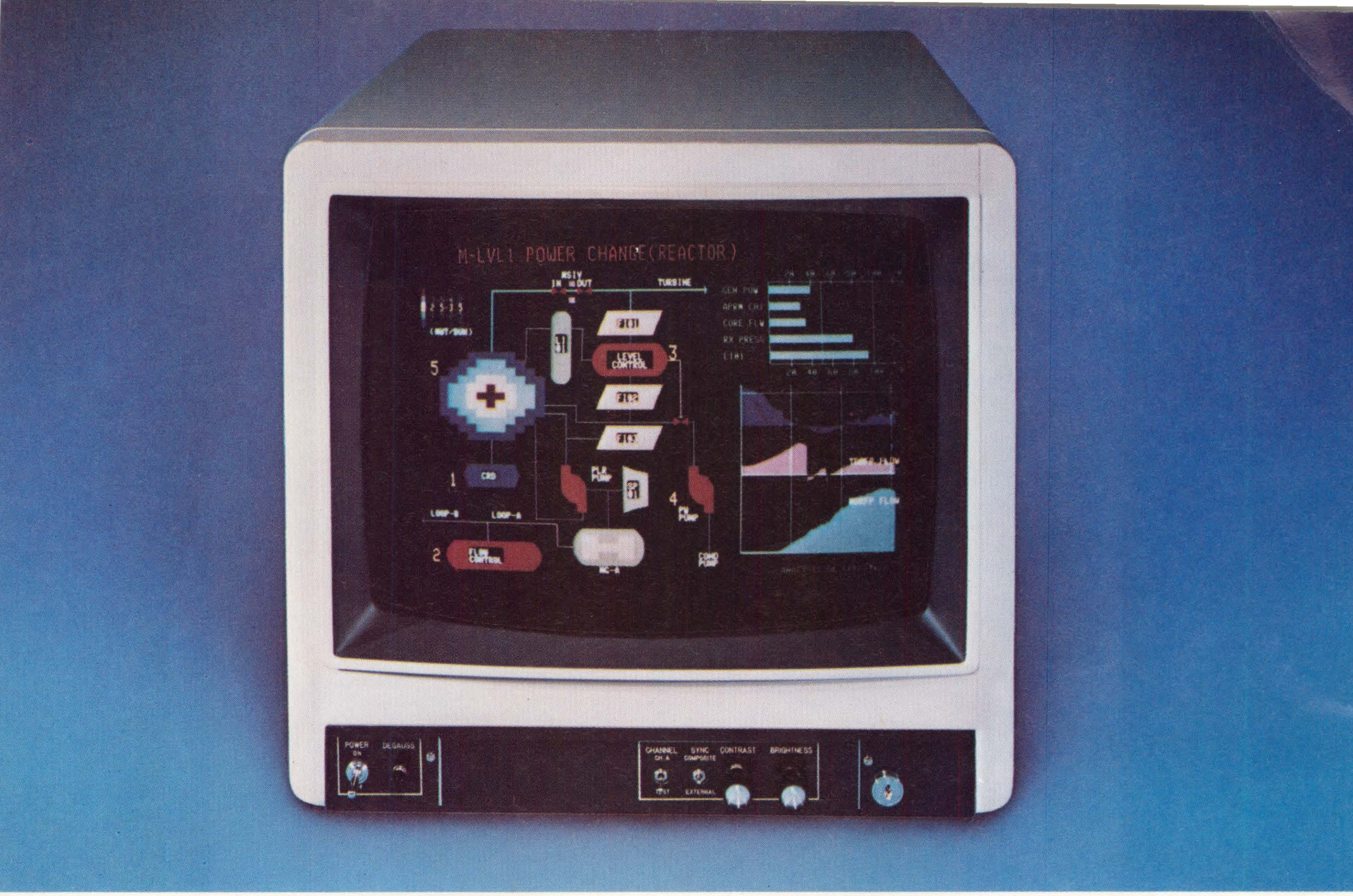
The unit's streaming formatter/controller separates incoming data into blockettes, and inserts internal address, resync, and error detection and correction characters between blockettes. These data are verified within the drive during write mode and are stripped during read mode to return only data to the host.

The controller interface looks like a semiconductor memory element, and the unit may be thought of as a nonvolatile FIFO memory. Since complex timing and data handling requirements are eliminated, it can be readily integrated into a system. Integration is also enhanced by industry standard dimensions that allow the unit to mount in the same space as a flexible disc drive using standard mounting hole locations.

Both 10M- and 20M-byte models record at 7500 bits/in (2953/cm) in 2- or 4-track serpentine mode on 450' (137-m) ANSI X3.55-1977 tape cartridges. The dual-gap read while write head with separate erase provides data reliability that is less than 1 error in 10^{10} bits with optional error correction.

All models have identical interfaces, and dimensions that provide for maximum systems flexibility and upward compatibility as future increases in capacity are made available. The 10M-byte 2-track unit is priced at $746 with formatter/controller in OEM quantities; the 20M-byte, 4-track unit sells for $788. In stripped-down format, prices are $415 and $525 for 10M- and 20M-byte units in OEM quantities.

Circle 282 on Inquiry Card



SEEING IS BELIEVING HITACHI'S SUPERIOR RGB COLOR MONITORS.

Clearly the finest color monitors are available from Hitachi, a company that produces some of the finest instruments in the electronics business. For over a decade engineers and scientists have relied on Hitachi technology and products to expand research and production world-wide. Hitachi's dedication to excellence has made its color monitors the best in the industry.

The Hitachi RGB color monitors are designed for use in computer data and graphic display application. These units are ideal for industrial control, image processing, CAD and any situation where color displays of computer-generated images are needed. Hitachi's advanced tube technology coupled with quality electronic circuitry results in color monitors with superior performance and reliability. In addition the wide range of models available with a host of options can solve any application requirements.

Our model HM 2619/13 and 2719/13 with self convergence and in-line gun are examples of the most advanced state of the art technology developed by Hitachi. Check the chart and specifications and you'll clearly see the advantages of Hitachi's RGB color monitors. For further information call (415) 981-7871.

MODEL	HM-2519	HM-2619/2613	HM-2719/2713	HM-1519
Screen Size	19V"	19V"/13V"	19V"/13V"	19V"
Resolution	High	High	High	Standard
Convergence	High	Self-convergence	Self-convergence	Conventional
Number of Lines	Max 720 525/625 std	Max 720 525/625 std	Max 720 525/625 std	Max 720 525/625/std
CRT	Delta gun Dot shadow mask 0.31mm dot pitch	In-line gun Dot shadow mask 0.31mm dot pitch	In-line gun Dot shadow mask 0.31mm dot pitch	Delta gun Dot shadow mask 0.61mm dot pitch
Display Capability	4,000 char. Analog	4,000/2,000 char. Analog	4,000/2,000 char. Analog	2,000 char. Analog
Video Amplifier Bandwidth	25 MHz ± 3 dB	25 MHz ± 3 dB	25 MHz ± 3 dB	25 MHz ± 3 dB

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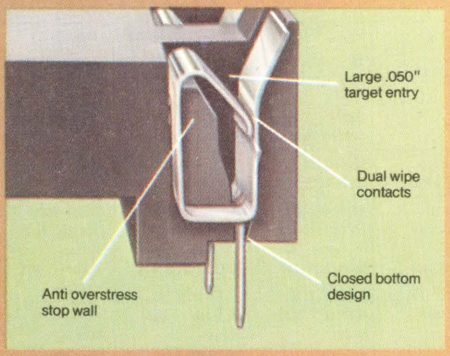
"For reliability I'll take AMP 175 Profile DIP Sockets every time."

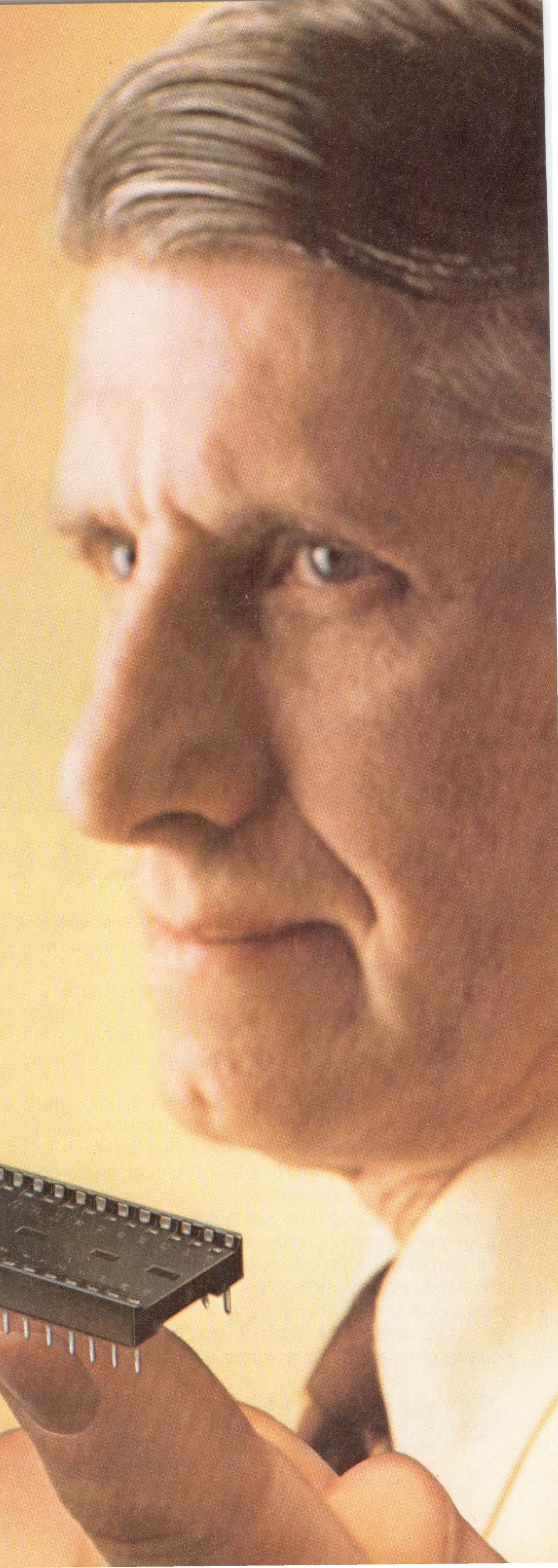
Your IC's are only as good as the sockets they go into. That's why we designed the DIPLOMATE Socket in the first place—to protect IC performance. And we do it with features that set industry standards for reliability and performance—in both gold and tin versions.

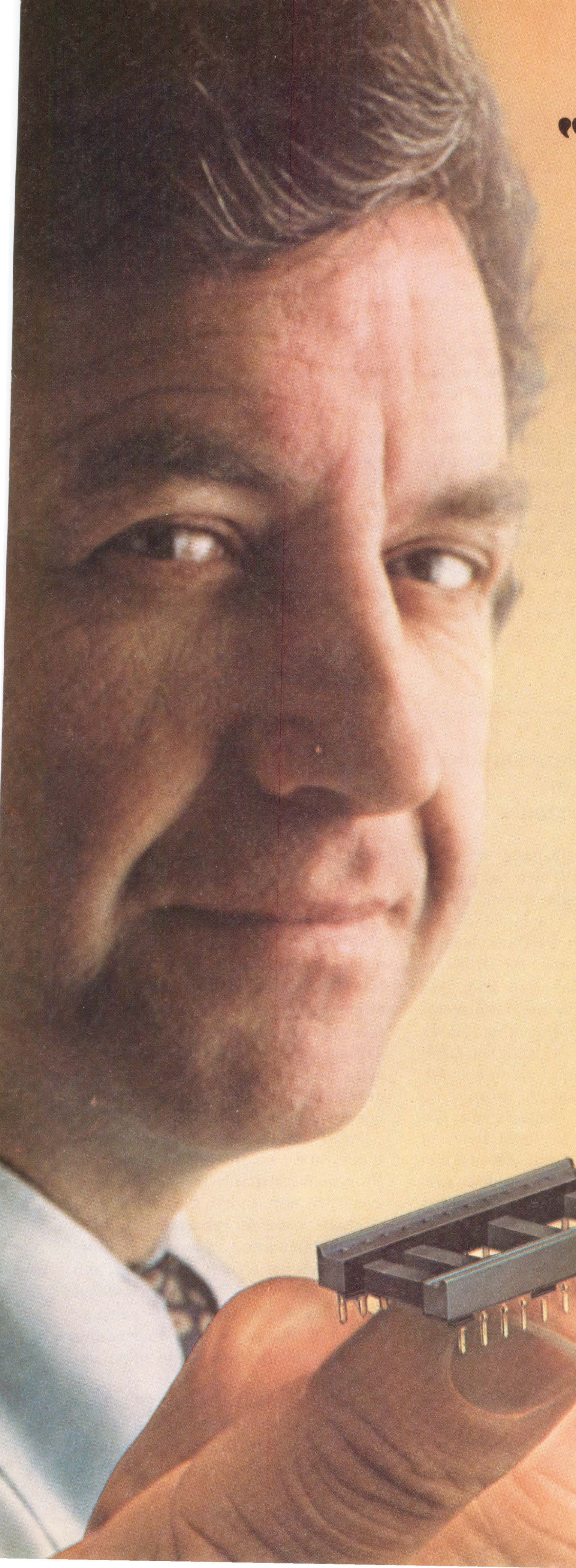
Features like a large entry target area and an internal contact anti-overstress stop wall to prevent contact damage. A closed bottom to inhibit solder wicking and flux contamination. Dual wiping contacts for a more dependable interface. And for easy, cost-effective application, the housings are compatible with commercially available automatic insertion equipment for socket-to-board or DIP-to-socket operations.

DIPLOMATE Sockets are available in 8 through 40 position sizes. And every one of them meets the requirements of MIL-S 83734.

What's more, you can get DIPLOMATE .175" Profile Sockets immediately, thanks to AMP's computer-linked regional inventory system. For delivery details or for more information, call the AMP DIPLOMATE 175 Socket Information Desk at (717) 780-8400. Or write us. AMP Incorporated, Harrisburg, PA 17105.







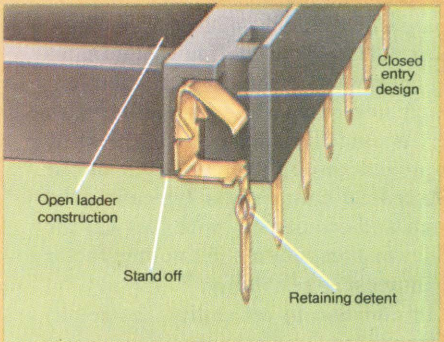
"For reliability I'll take AMP 160 Profile DIP Sockets every time."

Besides their proven reliability in tin or select gold-plated styles, AMP .160" DIP Sockets offer one of the lowest profiles in the industry. At a price to match. And with features that make them the intelligent choice for your low profile applications.

They're available with up to 44 positions. And have anti-wicking, anti-bridging contact design. Plus one piece housings with side chamfered lead cavities for easy IC insertion.

AMP 160 Sockets also feature a ladder design which allows for easy cleaning and viewing of the circuit traces after insertion. And for added versatility, styles are available in single row form for use with packages having non-standard spacings.

These sockets meet or exceed MIL-S 83734, and are available through our computer-linked regional inventory system. For the delivery details or for more information, call the AMP .160" Profile Socket Information Desk at (717) 780-8400. Or write us. AMP Incorporated, Harrisburg, PA 17105.



AMP has a better way.

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CIRCLE 42 ON INQUIRY CARD

Add-In Memory Boards For IBM 303X Offer Low Cost Alternative

STOR/3000 universal add-in memory systems plug directly into the storage backplane of IBM 303X series computers. Cambridge Memories, Inc, 360 Second Ave, Waltham, MA 02154 has designed the systems to use existing IBM circuitry and signals wherever possible. This approach eliminates the need for complex interface logic, failure prone interconnect cables, and redundant logic and power supplies, and provides a high performance alternative at 40% lower cost.

The memory system was developed along two parallel paths. One criterion was to follow IBM technology and component selection to enable the memory systems to appear completely transparent to and therefore to accommodate all IBM hardware, software, and maintenance capability without alteration. The second was to develop and integrate a packaging technique that would increase memory capacity and improve reliability.

Based on 64k MOS RAM storage devices, the boards provide four times the capacity of identically sized IBM boards using 16k modules. However, to guarantee maximum production capacity, alternate systems use more readily available 32k and 16k MOS RAM devices on higher density memory boards of identical overall size. Standard MST compatible logic eliminates the need for complex transition circuitry necessary when logic other than MST is used. Reliability is significantly improved through replacement of the 600 trilead connections typically used in an add-on memory with just 12; use of fewer components is another factor in increasing reliability.

In addition to reliability, the reduced number of connections allows faster and simpler installation. The memory system has two active card types—storage and address. Each type is interchangeable in any similar card location. Address and storage cards are one for one equivalents of IBM's, except that one storage card can replace up to four IBM storage cards. Similar to IBM, the system, when necessary, adds storage protect cards for each increment of additional memory. Storage protect cards are also interchangeable and compatible between systems.

The system's simplicity and modular nature permits rapid problem resolution. Maintenance is performed from the console using diagnostic and debugging procedures similar to IBM's. Reconfiguration capability of the add-in memory enables the system operator to logically reassign or take offline any multiple of 2M-byte increments of memory on a 3033 or 3032; this increment is 1M bytes on a 3031. Reduced power, floor space, and air conditioning requirements all serve to conserve energy for additional savings.

Circle 283 on Inquiry Card

Models, Hardware Options Extend Family of Commercial Systems

Three CS/50 models expand the commercial systems family to a compatible range covering single station up to 17-terminal systems. Included in the announcement made by Data General Corp, Rt 9, Westboro, MA 01581 is availability of 12.5M- and 25M-byte Winchester discs with integral diskette and an upgrade option that allows CS/40 users to grow to a CS/50 or CS/60 and CS/50 users to upgrade to a CS/60.

Units support from one to nine interactive Dasher™ terminals with fast response time, up to 760M bytes of disc storage, and 600- and 900-line/min printers. Addition of the disc subsystems injects Winchester reliability and low cost into the systems, while upgrade options provide the potential for economic expansion as applications grow.

CS/50 supports interactive operations such as order entry or customer inquiry, with concurrent activities supporting data communications, file maintenance, or program development. Larger users with distributed sites can use RJE80 (2780/3780) and HASP II communications.

The CS/50 Mod C3 supports 64k bytes of MOS memory and up to three active terminals. This configuration offers a choice of integrated 12.5M- or 25M-byte disc/diskette subsystem or 20M-byte disc, and supports 800- or 800/1600-bit/in magnetic tape drives. Mods C5 and C6 offer greater system capability through 128k- or 256k-byte main memory capacities. The C5 supports 80M bytes of disc storage, and the C6 up to 760M bytes. Both attach up to nine terminals. Prices range from $32,450 to $76,050.

Because the systems are data and program compatible, applications programs developed on one need not be completely rewritten for use on other systems. In addition, all systems run under the interactive COBOL operating system (ICOS) which supports an interactive version of the industry standard ANSI '74 COBOL programming language. Features include special screen formatting and file management capabilities. Also available are program development software packages: FIRST, a program generator; MASTER, a menu access and security system; and JOBS, a batch stream processor.

Program development packages running under ICOS significantly reduce program development time. FIRST and MASTER are organized around a system of menus and data entry screens. This saves the programmer from the task of writing lines of COBOL code to implement applications software, reducing development costs as well as simplifying computer operation.

FIRST automatically generates complete COBOL source code programs. Programmers simply respond to questions displayed by the system to generate code for programs such as file maintenance, inquiry handling, report writing, screen generation, and transaction entry. By storing code in copy files on the system, the package creates a library of function modules for later incorporation into other applications.

Working similarly, MASTER allows the programmer to generate both a menu system, to tie an application's programs together, and a security

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8085A	✓		✓		✓		✓		✓		✓	
8049	✓		✓		✓		✓		✓		✓	
8039	✓		✓		✓		✓		✓		✓	
8039-6	✓		✓		✓		✓		✓		✓	
8035	✓		✓		✓		✓		✓		✓	
8021	✓		✓		✓		✓		✓		✓	
8048	✓		✓		✓		✓		✓		✓	
6802	✓		✓		✓		✓		✓		✓	
6800	✓		✓		✓		✓		✓		✓	
F8	✓		✓		✓		✓		✓		✓	
3870	✓		✓		✓		✓		✓		✓	
3872	✓		✓		✓		✓		✓		✓	
Z80A	✓		✓		✓		✓		✓		✓	
TMS9900	✓		✓		✓		✓		✓		✓	
SBP9900*	✓		✓		✓		✓		✓		✓	
1802	✓		✓		✓		✓		✓		✓	

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CIRCLE 44 ON INQUIRY CARD
CIRCLE 84 ON INQUIRY CARD

system to protect computer programs and data. The menu system lets users plan and automatically create uniform menu structures with no additional programming and simplify program execution. Authorization and access schemes offer security for files and functions.

The job oriented batch system (JOBS) increases system productivity by processing batch queries unattended during off hours. An operator can define and then execute a stream of batch programs rather than starting each program individually. If an interrupt occurs the system's current status information display allows the operator to see just where it occurred and to restart the process anywhere in the queue.

Circle 284 on Inquiry Card

Desktop Computer System Incorporates Diskettes In Lower Cost Unit

IBM 5120 computing system integrates two direct access diskette drives and a 9" (23-cm) diagonal CRT screen in a unit priced in the $9340 to $23,990 range. Introduced by International Business Machines Corp, General Systems Div, PO Box C-1645, Atlanta, GA 30301, the system provides BASIC and/or APL language, from 16k to 64k of main memory, and a 120-char/s printer.

Packaged in a desktop unit, like its predecessor the 5110 (see *Computer Design*, Mar 1978, p 55), the system can be purchased for less than $13,500 in a configuration that includes 32k characters of main storage, a 120-char/s printer, and the BASIC programming language. Applications packages introduced with the system allow users to perform inventory, billing, payroll, accounts payable, accounts receivable, and general ledger accounting on the system.

Based on the IBM 5110 model 3 computer, the system is composed of 5103 models 11 or 12 bidirectional matrix printers with speeds up to 80- and 120-char/s, respectively, and the 5114 diskette unit that provides up to 2.4M bytes of direct access storage. Standard features of the 5110 model 3 include 9" (23-cm) CRT that displays 1024 characters on 16 lines of 64 characters each with upper and lower case under program control.

Screen management is fully programmable including automatic cursor position and CRT on/off control. System control switches and status indicator lights are readily accessible to the right of the CRT. An audible alarm signals the operator whenever attention is required by way of system or user program control. A composite video adapter provides the capability for simultaneous display of CRT data on additional TV monitor screens.

The typewriter like keyboard indicates special characters for BASIC or APL depending on the model. The separate 10-key numeric pad also contains four operator keys that provide arithmetic functions.

Available as options on the system are a ROM-resident diskette sort that handles full record or record address sorting from either BASIC or APL programs. The sort key can contain up to six sort control fields; control statements can be stored on diskette or entered from the keyboard via a prompting message. A serial I/O adapter, operating in conjunction with user programs, attaches to external devices and operates with 5-, 6-, 7-, and 8-bit transaction codes.

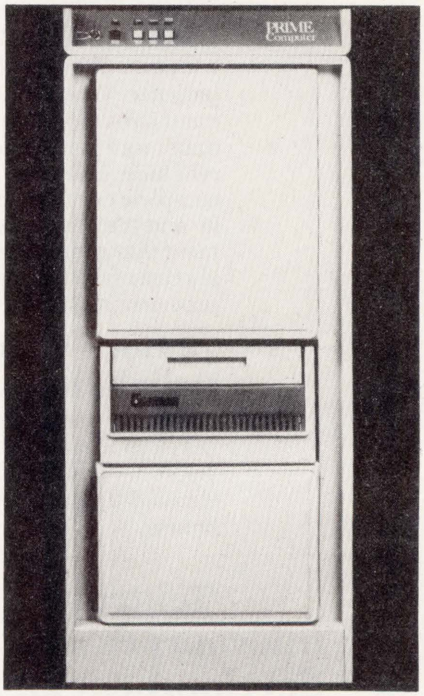
With the binary synchronous communications adapter, the 5120 can function with switched or nonswitched communications lines at transmission rates up to 4800 bits/s as a processor terminal emulating 3741 line protocol or 2770 in conjunction with program control. 2741 compatibility is attained using the asynchronous communications adapter that uses start/stop discipline at transmission speeds of 134.5 or 300 bits/s over switched lines.

Applications packages introduced with the systems allow interrelated applications through generation and passing of transaction data on diskettes for direct input as appropriate. Operating complexity is reduced through their approach to program documentation and use of menu driven selection of procedures and screen prompting. Built-in audit ability and control is gained through zero balancing and control totals.

Circle 285 on Inquiry Card

Computer System Lowers Entry Cost Into 32-Bit Family

Price/performance advantages of two general purpose 32-bit computer system models are claimed to make interactive mainframes available to those previously forced to settle for typical low end minicomputers. Serving as a low end entry into the fully compatible 50-series line, these units provide functionality and communications capabilities of larger systems at low prices. Models 250 and 150 are fully compatible with other systems from Prime Computer, Inc, 3 Newton Executive Pk, Newton, MA 02165 and offer power, speed, and functional



Configured and supported for implementation of dedicated or distributed processing systems in multiple locations and providing the large memory space necessary to run mainframe programs, the 32-bit PRIME 150 boosts throughput by use of microcode and high speed cache memory

Both sides now

North Star Announces —
Double Density x 2 Sides = Quad Capacity!

The North Star Horizon now delivers quad capacity by using two-sided recording on our new mini drives! That's 360,000 bytes per diskette! A four drive North Star system accesses over 1.4 megabytes of information on-line! Think of the application flexibility that so much information storage can give you!

North Star has quadrupled the disk capacity of the Horizon computer but prices have increased a modest 15 percent. On a dollar per byte basis, that's a bargain that is hard to beat!.

The proven North Star disk controller was originally designed to accommodate the two-sided drives. North Star DOS and BASIC are upgraded to handle the new capacity, yet still run existing programs with little or no change. Of course, single sided diskettes are compatible with the new disk system.

North Star Horizon OEM Prices (includes 32K RAM, one parallel and two serial I/O ports),* assembled, burned-in and tested:

Horizon-1-32K-Q	$1890
Horizon-2-32K-Q	$2265
Horizon-1-32K-D	$1890
Horizon-2-32K-D	$2265

*In quantities of 100 or more

Get both sides now! Call Bernard Silverman for more information.

NorthStar

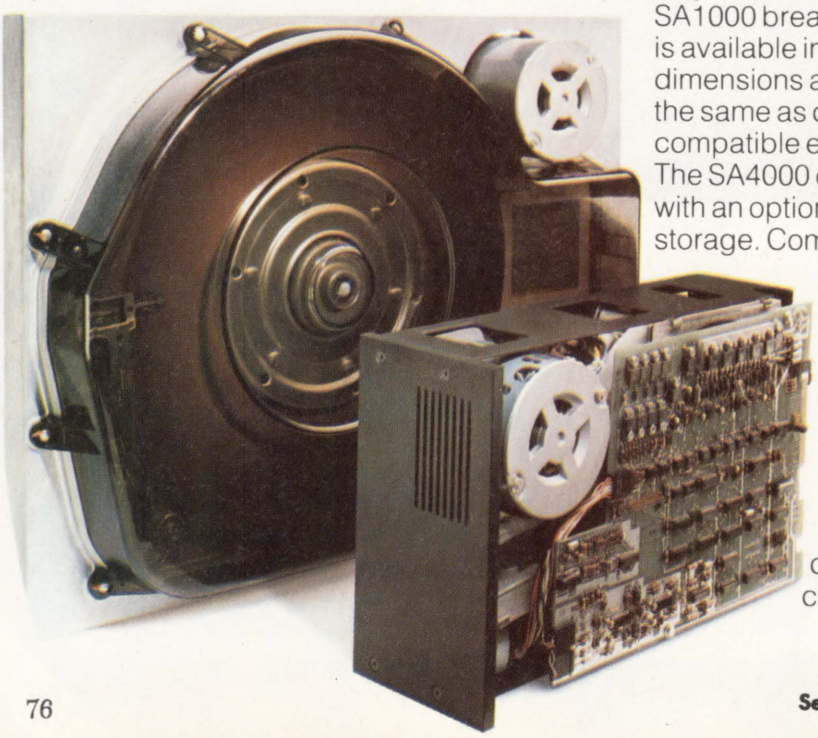
North Star Computers, Inc.
1440 Fourth Street
Berkeley, CA 94710
(415) 527-6950 TWX/Telex 910-366-7001

CIRCLE 45 ON INQUIRY CARD

Want 800-1600 KBytes? Choose our SA801/851 series. With the SA801 8-inch floppy, you have a choice of 400 or 800 KBytes in single or double density, on the same drive for the same price. Well over half a million of these standard-setting drives have been specified by OEM's around the world. They know that they can count on Shugart's proprietary read/write head technology to deliver media life of over 3.5 million passes per track, and head life of more than 15,000 hours. That's headstrong performance. And the double-sided SA851 drive gives you even more capacity. It stores 800 to 1600 KBytes using single or double density recording. The 851's proprietary Fasflex™ band actuator improves track-to-track access time to a fast 3 ms. There's also a programmable door lock and write protect. The headstrong SA801/851. Solid performers from the leader in floppy technology.

The head
Choose your

Moving up to 5-29 MBytes? Check Shugart's SA1000 and SA4000 fixed disk drives with the lowest cost per MByte in their capacity range. The new 8-inch SA1000 breaks the $1,000 price barrier and is available in 5 and 10 MByte versions. Its dimensions and mounting holes are exactly the same as our floppy drives, and it's more compatible electrically than competitive drives. The SA4000 offers 14.5 and 29 MByte capacity with an optional 144 KBytes of head-per-track storage. Compact and lightweight, it uses only 5¼ inches of panel space and weighs only 35 pounds. All Shugart fixed disk drives use proven Winchester head and media technology to ensure better data integrity and longer life. And system integration is easy because both the SA1000 and SA4000 can share a power supply with your floppy drives. Shugart fixed disk drives. The head of the family in capacity and cost/performance.



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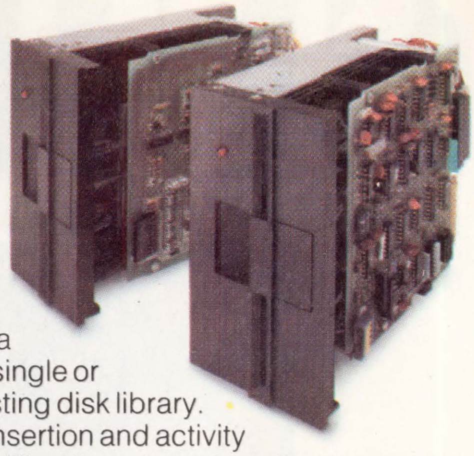
See us at NCC, Booth 4309



Need 220-440 KBytes? The famous Minifloppy™ is the right choice. Choose the original SA400 Minifloppy or the double-sided SA450. You can store up to 218.8 KBytes single-sided and up to 437.5 KBytes double-sided (unformatted, double density). Both are the same compact size and weigh only three pounds. Both are I/O compatible, and use Shugart's own glass bonded ferrite/ceramic read/write heads. The double-sided SA450 uses our new Bi-Compliant™ head assembly for superior compliance and data reliability. Both drives allow you to read and write data on any single or double-sided minidiskette, so you can continue to use your existing disk library. Low heat dissipation, DC drive motor, write protect, positive media insertion and activity light are all standard. Since we invented the Minifloppy, over half a million have been installed in systems like yours—proof that this is the 5¼-inch floppy with the right capacity and the right price/performance. Choose the original. Minifloppy.

strong family. capacity.

Choose the Headstrong Shugart disk drives. No matter which disk drive you select from our family, you get the competitive edge when you go with Shugart. We are Headstrong about helping to keep you competitive too, with high volume deliveries of drives that offer superior reliability, quality, and value. This Shugart commitment is also backed by all the support you need including helpful technical services, in-depth documentation, and design assistance. And when your product line grows, we'll be there with a complete family of floppy, Minifloppy, and fixed disk drives in a full range of capacities. Reliable products, volume delivery, superior quality, and value. That's what we're Headstrong about at Shugart. □

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Sales & Service: Sunnyvale, CA; Costa Mesa, CA; Minneapolis, MN; Richardson, TX; Waltham, MA; Landing, NJ; Atlanta, GA; Toronto, Ontario; Paris, France; Munich, Germany. □ *Shugart products are also available off the shelf from local Hamilton/Avnet outlets.*

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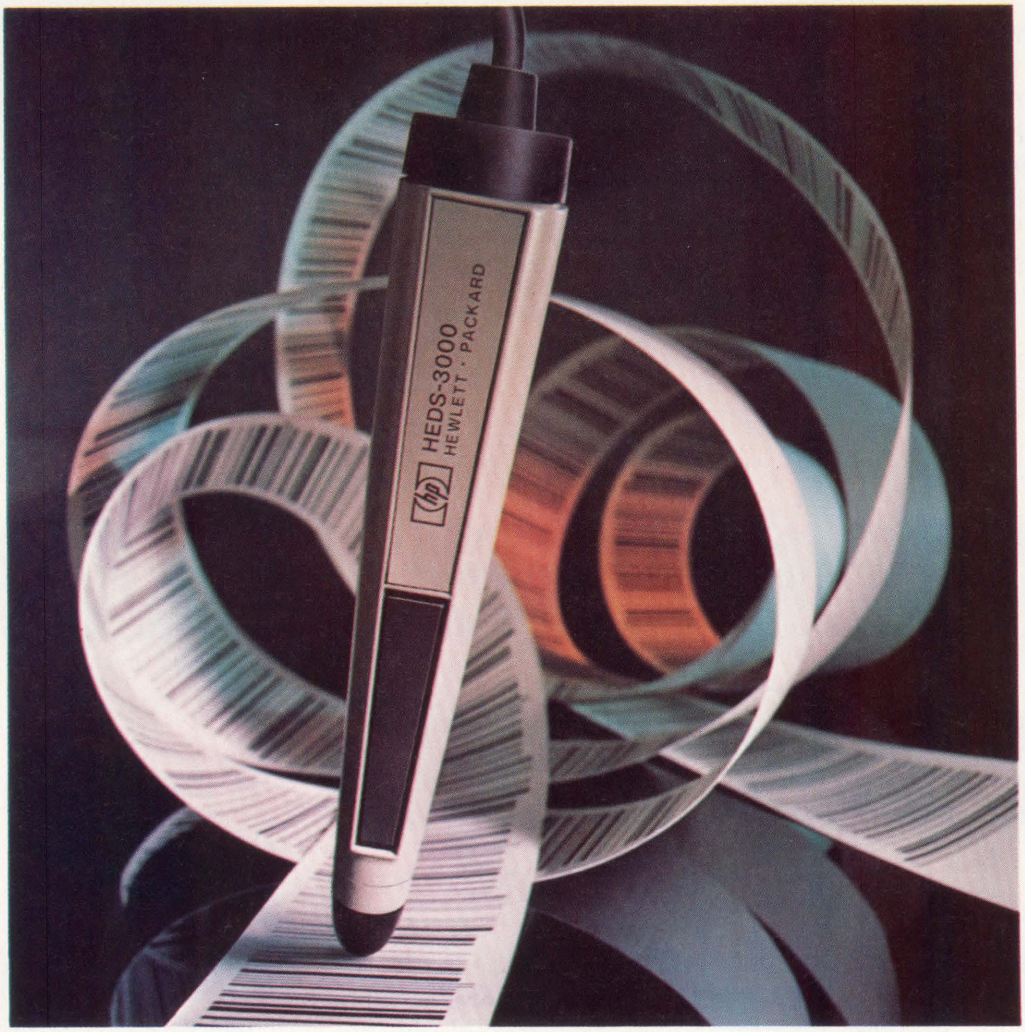


HP Introduces the World's First Digital Bar Code Wand.

Anyone now using a keyboard or push buttons for data entry could benefit from using bar codes.

Depending on the number of characters being entered, bar code scanning has been shown to be from two to four times faster than key entry.

HP's new HEDS-3000 Digital Bar Code Wand can scan black-and-white bar codes and convert the codes to microprocessor-recognizable digital output. Fully specified and guaranteed, the Wand contains a push-to-read switch which conserves power. It is well suited to portable systems as well as those with line power. The Wand is housed in a rugged, stylized, molded plastic case with attached cord and connector. Of even further interest to OEM's, the HEDS-3000 can be manufactured in custom colors with desired logos.

In quantities 1-99, the Wand is priced at $99.50* each.

For more information or immediate off-the-shelf delivery, contact your nearest HP Components franchised distributor.

In the U. S. contact Hall-Mark, Hamilton/Avent, Pioneer Standard, Schweber, Wilshire or the Wyle Distribution Group (Liberty/Elmar). In Canada, call Hamilton/Avnet or Zentronics, Ltd.

HEWLETT PACKARD

01906

*U. S. Domestic Price Only

breadth, enhanced with distributed processing and networking capabilities.

Designed for 5 to 8 users and based on the model 550 (see *Computer Design,* Mar 1979, pp 63-64), the 250 is designed for end users who need 550 capabilities but a less powerful package. Configured for system builders, the model 150 provides many of the 450's capabilities at a lower price.

Providing about 60% of the 550's performance and based on the same architecture, the 250 offers main memory up to 1M bytes, runs programs as large as 32M bytes, and supports up to 16 simultaneous users. It is packaged with a 32M-, 64M-, or 96M-byte cartridge module disc system.

Compatible with the company's peripherals, controllers, and I/O interfaces, the processor has 32-bit architecture, high speed integer arithmetic unit, 128 32-bit hardware registers for system management, and stack architecture to provide fast, efficient computation. Another feature is the multilevel hardware controlled ring memory protection system.

In an entry level configuration, the 250 has 512k bytes of error checking and correcting MOS main memory, PRIMOS operating system, floating point instructions, 2k-byte, 80-ns access cache memory, business instruction set, virtual control panel, 32M-byte cartridge module disc subsystem, CRT console, and 8-line asynchronous multiline controller. This system is priced at $59,500.

Model 150 offers 60% of the performance of the 450 and is configured and supported for software houses that want to develop and implement dedicated or distributed processing systems in multiple locations, and require large memory capacity to run mainframe programs. Configured with 256k bytes of ECC MOS main memory, PRIMOS operating system, floating point instructions and business instruction set, 2k-byte, 80-ns access cache memory, 32M-byte cartridge disc system, virtual control panel, and 8-line asynchronous multiline controller, this system is priced at $49,000.

Both models are fully supported by PRIMENET™ networking capabilities giving users local and remote network communication services. In geographically dispersed network configurations, systems can communicate among themselves via a local high speed loop, with terminals over low cost packet switching networks, or via private synchronous lines. Systems can be interfaced to various terminals and communication lines with multiple protocols that include IBM BISYNC for HASP and 2780, HDLC for X.25 packet switching networks, Control Data 200UT, Univac 1004, and ICL 7020.

Circle 286 on Inquiry Card

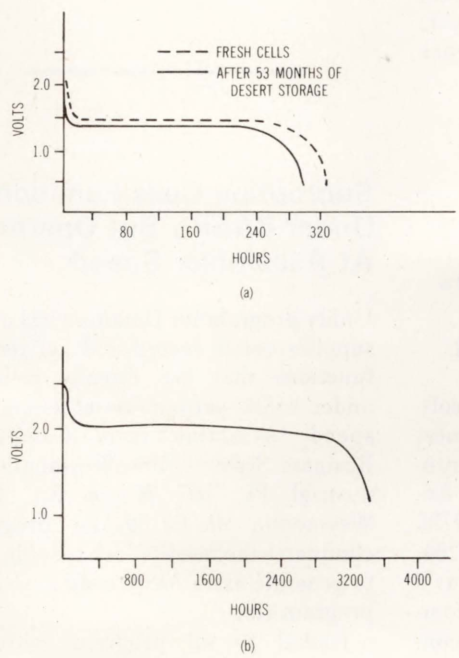
Lithium/Copper Oxide Batteries Serve as Long Term Energy Source

Lithium/copper oxide batteries offer three to four times the longevity of zinc carbon cells, and can serve as an efficient energy source for electronic systems. The result of long term research and development by the Saft Corp of America, 711 Industrial Blvd, PO Box 1284, Valdosta, GA 31601, the system provides 1.5-V compatible with currently used circuitry and requires no circuit changes.

LC-01, -02, and -07 cells (AA, ½AA, and ¼AA) sizes have a proven 10-year shelf life as indicated by 5-year desert storage test data. The stable chemical system ensures safety to the user and functions efficiently over a wide temperature range. Specific battery packs have been designed and tested to operate for 100 hours at 150 °C. Known for its light weight, the lithium system produces three to four times the energy of zinc carbon cells and twice that of alkaline manganese cells.

Fresh AA cells show a life time approximately 60 hours longer than cells stored for 53 mo in "desert conditions." (Desert storage is from room temperature to 50 °C for 6 h/day and 4 days/wk.) Life varies from approximately 340 to 280 h between fresh cells and those stored for 18 mo at a temperature of 158 °F (70 °C). ½AA and ¼AA cells show comparable performance.

Circle 287 on Inquiry Card



LC-01 lithium copper oxide batteries developed by Saft have long shelf life as demonstrated by comparison (a) of fresh cells with those stored for 53 months in desert conditions (from room temperature to 50 °C for 6 h/day and 4 days/wk). Efficiency of the cells can be seen in discharge curve (b) obtained with 1.5-kΩ constant load at a temperature of 20 °C

SOFTWARE

Pascal Programming Language Offered For HP 1000 Computers

Pascal/1000 compiler adapts to both systems and applications programming on HP 1000 computers. Offered by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, the language runs only in the multiuser environment of the RTE-IVB disc based operating system.

A full implementation of the Pascal language, the compiler allows coding and debugging to be done two to four times faster than in assembly language. In addition, the language enables a clean well-structured, well-documented program to be implemented with only a few easily located logic errors.

Instruction sets are compatible across the HP 1000 line. The compiler offers the ability to link Pascal programs to external Pascal, FORTRAN, and assembly language routines as well as to proprietary software such as IMAGE, GRAPHICS, and DATACAP. Features such as separate compilation, direct access I/O, double-word integer, and double-precision real data types are incorporated.

Circle 288 on Inquiry Card

Software Package Enables Diagnosis/Repair of Software on Remote Unit

Remote Disc Operating System software facilitates remote maintenance, diagnosis, and repair of software running on dispersed processors. Announced by Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, REMDOS allows any of the company's processors with synchronous communications capability to assume control over another similar processor's functions. Utility and applications programs can be initiated at a remote site, results observed, and alterations made via phone lines.

A link can be achieved between two processors with REMDOS software and synchronous communications adapters with Bell-compatible modems. Communications are supported at rates of up to 9600 baud over dialup or leased lines. Software is compatible with all processors using a 5500 instruction set, including the 1800, 3800, 5500, 6000, and 6600 processors.

In addition to standard DOS commands, the package has a message switching facility to allow operators to communicate with each other via keyboards and display screens. The remote console can be made to display commands and information as they are keyed in. Other special commands enable transfer of disc files in either direction, and initiation of programs or utilities at remote sites. Although some diagnostic and maintenance jobs may require operators at both processors, the system can run with the remote processor unattended.

Circle 289 on Inquiry Card

Subroutine Calls Functions Under BASIC, But Operates At Assembler Speed

Utility program for Data General users supplies delete record and get record functions that are directly callable under BASIC, yet operate at assembler speed. Available from Computer Business Systems, Inc, Weymouth Industrial Pk, 167 Moore Rd, East Weymouth, MA 02189, the program eliminates the need to lock records and to generate extra BASIC code to reduce program size.

Global to all programs without modifications, the subroutine requires no preextension of random data files or updating of file size, as it is system wide in real time. All users can access records as soon as they are written.

The control record is updated automatically on disc each time a change is initiated, eliminating data loss during system crashes. Standard error codes for RDOS, user, and data file errors are all returned. In addition, the error amplifier provides data that covers control flag-2, chain pointer, free chain pointer, status flag, record length, and total number of records available in file. A subfile handler and automatic file positioning for writing in get record are also featured.

Circle 290 on Inquiry Card

DBMS Release Increases Efficiency In Large Operational Applications

Release 2.0 of the RAMIS II database management system increases support for large day to day operational applications, increasing its efficiency and applications areas. Issued by Mathematica Products Group, Inc, 14 Washington Rd, Princeton, NJ 08540, the release removes practically all limits in the system, permitting records to contain up to 32,000 fields and 90,000 bytes.

A PROFILE command provides environmental controls by allowing a set of user-defined values to be assigned to system parameters. Values may be modified at any time by a single word command. In this way, installation standards can be set for inexperienced users and the efficiency of systems using large files can be optimized.

Extension of the network structure capability of the data base allows the report writer to relate non-RAMIS files to RAMIS files. Reporting efficiency improvements ranging from 10 to 50% are achieved through replacement of fixed work areas by variable work areas in memory and acquiring them dynamically as needed.

Circle 291 on Inquiry Card

Our 64K ROM is like our 32K ROM is like our 16K ROM.

For new system designs and for upgrading existing systems, the flexibility of our totally static 64K ROM gives you that extra edge. And it's backed to the hilt with proven high performance.

The SY2364 is the latest addition to our family of 24-pin ROMs designed around a common industry standard pinout. That means maximum system flexibility. All three — 16K, 32K and 64K ROMs — can plug into the same socket. System upgrades are just a matter of substituting the new ROM for the old. With no increase in power.

We offer compatibility that's more than pin deep. All our ROMs are fully static (no clocks to worry about), so they all have the same timing waveforms. If speed is your concern, you can select one of our standard 450nsec versions or upgrade to our high performance 300nsec versions. All six are available now in quantity production.

	300ns	450ns
2K x 8	SY2316B-3	SY2316B
4K x 8	SY2332-3	SY2332
8K x 8	SY2364-3	SY2364

No matter what your needs, we have just the ROM for you. And that includes the SY2316A, SY4600 and SY2333 (pin compatible with the 2732/2732A 32K EPROM). For further information, contact Memory Product Marketing direct at (408) 988-5611. For Area Sales Offices and distribution references, call Headquarters Sales direct at (408) 988-5607. TWX: 910-338-0135.

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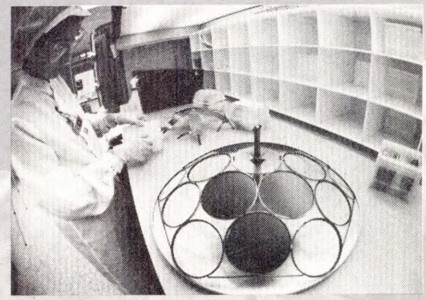

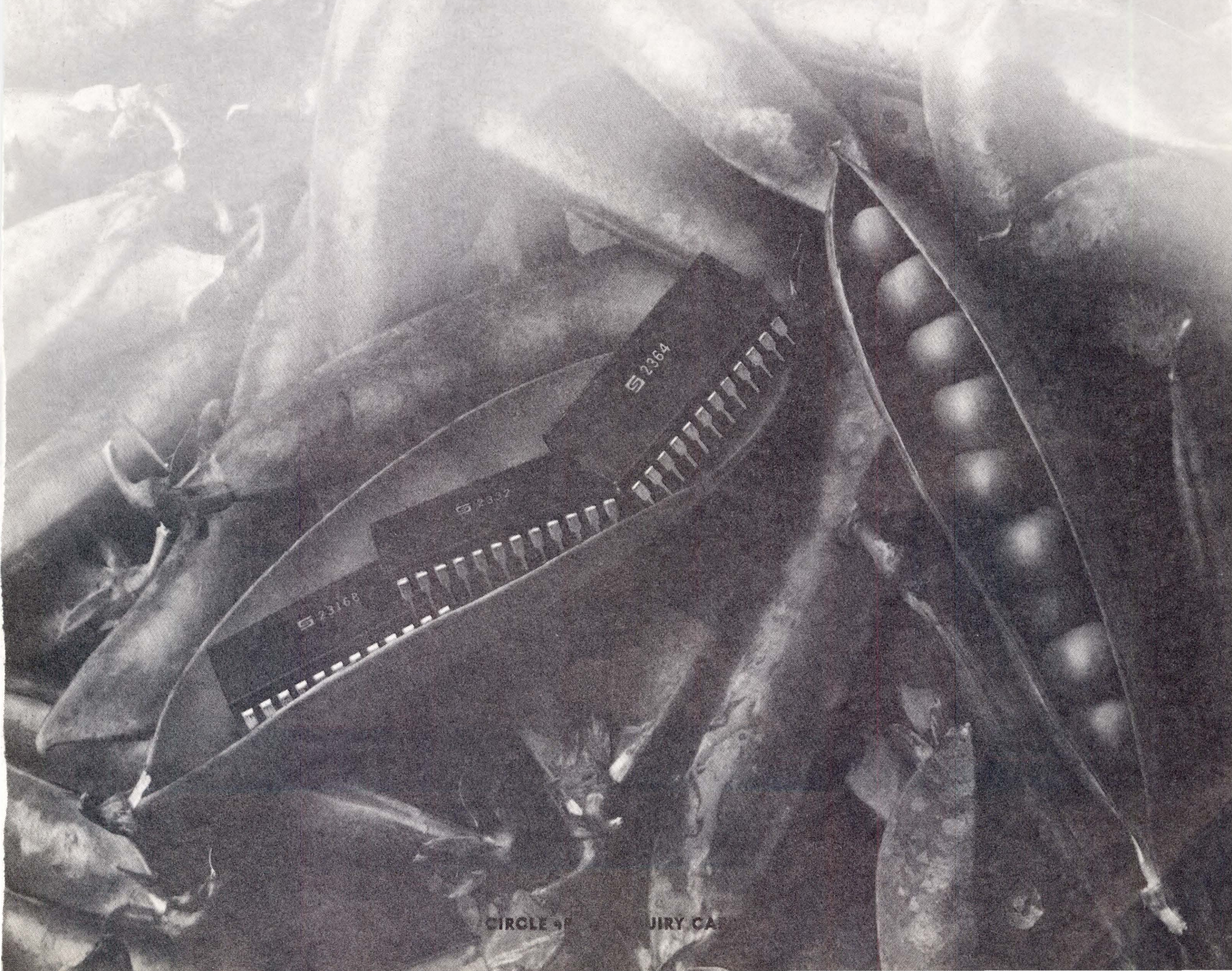

Logic Simulation/Test Generation Software Operates on VAX

Availability of TESGA4 on VAX-11/780 and DECsystem-20 computer systems permits economical operation with faster turnaround time. Previously restricted to conventional computer center operations, the program can now be run on a dedicated departmental computer or can share the system with engineering tasks.

TESGA4, a logic simulation and test pattern generation system, enables engineers to examine logic designs, and develop tests to determine the operational capabilities of the hardware implementation. Available from Comprehensive Computing Systems and Services, Inc, 4105 Tablerock, Austin, TX 78713, the package performs four basic types of functions: logic verification, design verification, fault simulation, and test generation. Running on a VAX, the system should reduce per problem costs by an order of magnitude compared with those of conventional mainframe operations.

The device library supplied with the package includes more than 100 macro models for standard integrated circuits. The system also has many register and functional type models to meet demands of LSI/VLSI designers. License fee is $150,000 for both VAX and DECsystem-20.

Circle 292 on Inquiry Card

Data Dictionary Features Added Security And Extensibility

Functional security and extensibility support features enhance the Integrated Data Dictionary. Offered by Cullinane Corp, Wellesley Office Pk, 20 Williams St, Wellesley, MA 02181, Release 2.0 also provides increased flexibility and simplification, permitting an element to be defined with multiple data formats and making definitions of communications entities available to any teleprocessing monitor for documentation purposes.

Functional security is supplied by the release's support for its own user identification and password security which gives protection from unauthorized updates on two levels. Users attempting to update a data base or teleprocessing entity are required to provide proper identification. When different departments use the same entity within the dictionary environment specific occurrence of an entity can be secured against unauthorized updates.

The concept of extensibility enables the user to customize the syntax by adding unlimited keywords. This feature allows users an unlimited language repertoire in establishing the scope of entity definitions.

Entry of record definitions in COBOL record format increases simplification. In addition, the text editing facility permits complete manipulation of comments and module source code on a line by line basis.

The release is operational with IBM 360/370, 303X, and 4300, and compatible hardware. It operates under MVT, MFT, SVS, MVS, VS1, VS2, DOS/VS, DOS/VSE, and VM/CMS. License fee is $15,000.

Circle 293 on Inquiry Card

Editing Software Reduces Host Overhead In Distributed Systems

Overhead requirements of computers operating under IBM's timesharing option or other interactive editing software system drop sharply with RAYCODE distributed editing software. Developed by Raytheon Data Systems Co, 1415 Boston-Providence Tpk, Norwood, MA 02062, the software runs on PTS/1200 distributed processing systems improving the speed with which programmers edit text and source code on 3270 type terminals controlled by the TSO/SPF programming facilities of an IBM host computer.

In addition to reducing host computer resources needed to support terminal editing functions, the editor improves terminal response time, allows programmers to continue editing when the host is down because of system, software, or communications failure, and assures predictable resource availability to maximize programmer productivity. Cost savings and improved productivity are provided because the editor allows host computer editing cycles to be offloaded to local or remote processing systems. The ability to store, edit, and develop programs in local mode, while retaining the ability to communicate with the host's TSO/SPF facilities results in improved programmer productivity.

Full screen context oriented facilities of the system also offer the capability of allowing operator terminals to be used in conventional 3270 emulation mode. This provides users


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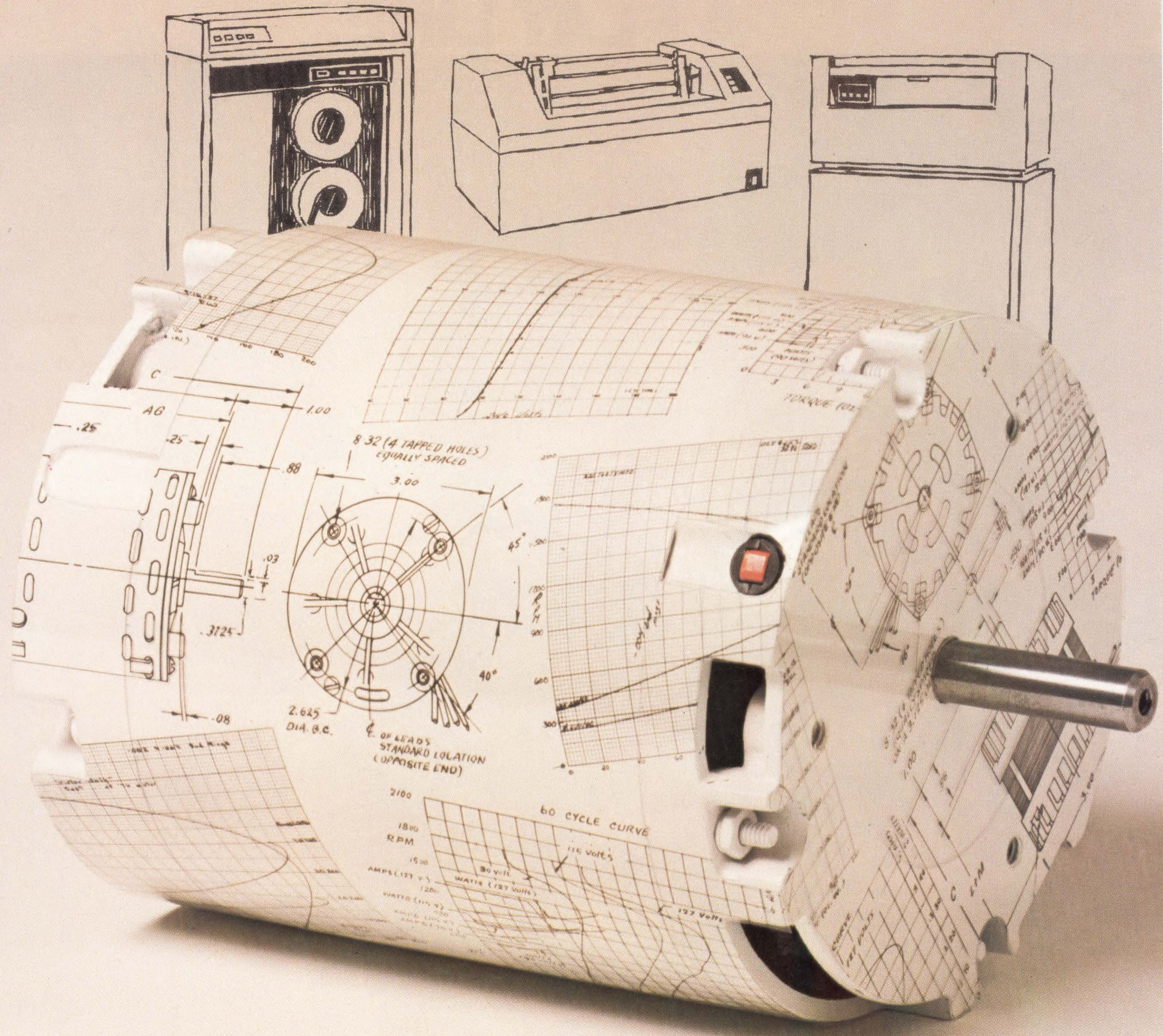
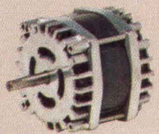
CIRCLE 49 ON INQUIRY CARD

HOWARD® motor-makers do great things with *your* specs for induction drive motors...



...and they price them very, very competitively



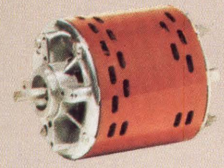
26 Frame Induction Motor

When you need an induction drive motor you want it designed exactly as you need it. Without hassles, without design headaches. That's the way Howard's motor-makers operate. They respond to your needs with fast action.

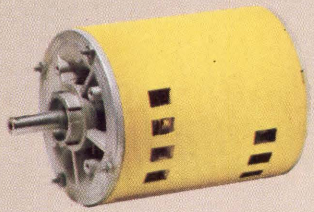
Tough and demanding customers such as IBM, Burroughs, Storage Technology, 3M (as well as scores of others) have found that Howard's engineering flexibility and adaptability makes it easy to get just exactly the induction drive motors they need.

We're small enough to react positively to your development time-tables — big enough and experienced enough (over 11,300,000 motors in the past 10 years) to deliver quality motors at a very competitive price.

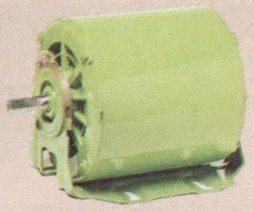
Check with Howard's motor-makers for any or all of your induction drive or motor parts sets needs. You'll discover that Howard's custom engineering approach makes your projects go smoother, faster — without paying premium prices.



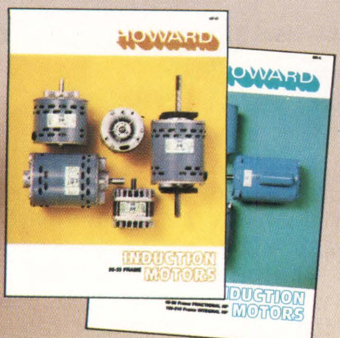
33 Frame Induction Motor



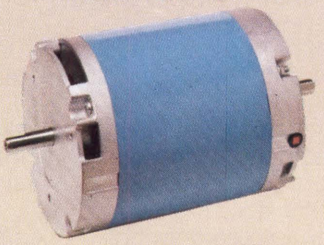
42 Frame Induction Motor



48 Frame Induction Motor



WRITE TODAY for TWO NEW INDUCTION MOTOR CATALOGS that provide torque curves, ratings, dimensional drawings on the complete line of 26, 33, 42, 48 and 56 Frame induction drive motors and motor parts sets.



56 Frame Induction Motor

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CIRCLE 50 ON INQUIRY CARD

Imagine...

from mind to matter. With Megatek.

Imagine a computer-aided graphics system that interfaces directly to the mind's eye, that takes a designer's visual perception of his design and does everything but weld it together.

Manufacturing and Consulting Services, Inc. has done it with their AD-2000 software package... CAD/CAM software that does it all—from design to fully annotated drawings to complete numerical control tapes. It can even calculate and assemble a bill of materials for an entire project.

The visual interface that enables the designer to communicate directly with the computer is a Megatek vector refresh terminal. Dr. Patrick Hanratty, MCS president, tells why.

"Megatek's refresh display is an extremely powerful tool for visualizing, manipulating, experimenting and altering design parameters.

"Megatek systems interface easily to a broad range of computers and enhance the engineer's feeling of direct interaction with his design."

Dr. Hanratty summarized his enthusiasm for Megatek with this graphic display of confidence:

"Customers for our software package can select any graphics terminal they want. A large percentage choose Megatek. Price/performance is the reason why. If I were going to put down dollars for a production refresh terminal, I'd put my money on Megatek."

For details call or write Megatek Corporation, 3931 Sorrento Valley Boulevard, San Diego, California 92121. (714) 455-5590.

MEGATEK/WHIZZARD

COMPUTER GRAPHIC SYSTEMS

CIRCLE 51 ON INQUIRY CARD

with alternate access to local or host data base in either TSO or 3270 mode.

The batch transmission system is completely queued so that transmission time required to receive or transmit data to the host is transparent to the user. Once data has been stored on the PTS/1200 it may be repeatedly edited and submitted to the host, and then stored on the local system or sent to the host for archiving.

Minimum configuration to run the editor consists of PTS/1200 series Mark I or II processor with a minimum 10M-byte disc system, and up to 10 display stations. The editor will also support local printers for program listing and other tasks.

Circle 294 on Inquiry Card

Host Resident Message Control Integrated Into Data Communications Systems

A host resident message control package, DCS model 50 interfaces with Burroughs NDL to add access control as well as message control and routing. This package provided by Systems Research, Inc, 2400 Science Pkwy, Okemos, MI 48864, gives Burroughs users a choice of four entry levels to online processing and the flexibility to upgrade their systems to match growth.

The software serves as a transaction based message control system and provides features necessary for operation of an online system in a multiapplication, multiuser environment. Compatible with Burroughs' data communication hardware, the package contains a host resident message control system, prototype application handler, online systems management, forms generation and management, audit and recovery, multilevel security, and user transaction activity analysis.

Under the system, applications programs are designed to be independent of the specifics of the communications network. Maintaining information of various terminal device types in the network, the system handles control character differences external to user written application programs, thus reducing program development time.

The security system provides maximum control over user access with minimum interference or inconvenience. To gain access, a user signs on by identifying himself with a valid name and password. Passwords are scrambled within the system to discourage unauthorized access. Security is maintained on five levels, and may be managed loosely or tightly and may be centrally controlled or distributed.

Circle 295 on Inquiry Card

Realtime Monitor Allows Rapid Diagnosis/Correction Of User's Problems

CICS/INFORM, a realtime monitor for CICS online systems, serves as a tool to diagnosis and correction of system problems. The software, released by Communication Software Aids, 80 Boylston St, Suite 618, Boston, MA 02116, allows systems programmers to retrieve information internal to CICS as well as receive updated information.

The monitor includes an offline program that preprocesses system dsects and places the screen image formats on a data set for display by one of its online programs. Both global and specific monitoring facilities are provided. Any monitoring and updating functions can be performed using a single CICS transaction.

The monitor operates as a normal CICS transaction and is completely release independent. The software is available at an introductory price of $4800 until June 30.

Circle 296 on Inquiry Card

Software Performance Monitor Expanded to Provide Logging/Analysis

Enhancements to EXPLORE/DISCOVER include a statistics logging and performance analysis facility and a partition STOP/START feature. The software performance monitor from Goal Systems Corp, PO Box 29481, Columbus, OH 43229 was developed to provide the ability to control and monitor the operating environment of the DOS/VS(E) system.

Users gain capability to gather, edit, archive, and selectively analyze performance data through the added statistics logging and performance analysis facility. The performance report generation program produces 29 separate reports plus variations based on sampling intervals, time period, and scaling factors.

A partition STOP/START feature permits operators to selectively stop and restart active partitions, giving the operator greater control over a badly performing system. The channel utilization report has been enhanced to show the percentage of I/Os which failed due to channel busy or device busy conditions.

Circle 297 on Inquiry Card

Entry Level COBOL Operating System Adds Modules to Match Growth

Mini-BLIS, an entry level turnkey COBOL operating system for business minicomputer systems, enables users to begin with COBOL, bypassing the costly step of converting from another entry level language. Consisting of individual modules for 1-, 2-, 3-, and 4-user capacities, the software, offered by Information Processing Inc, 1850 Lee Rd, Suite 320, Winter Park, FL 32789, provides multiuser capabilities in online and virtual memory environments.

Compatibility with peripherals offered by more than 50 manufacturers fits the system for use in distributive data base networks. CPUs from eight manufacturers are supported. Options include concurrent communications between minicomputers and/or host computers. Upward transparency protects the user's application programming and hardware investment since total compatibility with BLIS/COBOL allows up to 30 online terminals to be added as well as other multiuser environmental functions.

Circle 298 on Inquiry Card

Graphing Software Expanded to Run On Eclipse Systems

Revised PLOT 10 Easy Graphing software runs on midsized Data General Eclipse machines under RDOS with 64k bytes. Announced by Tektronix, Inc, PO Box 500, Beaverton, OR 97077, the FORTRAN package is also available in a color version that supports the 4027 color graphics terminal or 4660 series interactive plotters.

With the package, simple command verbs are used in a conversational manner to enter data and create graphs, resulting in presentation quality graphing without the burden of programming. Data may be entered from keyboard, read from files, or generated from algebraic expressions. Hooks are provided to link with user written forecasting or data handling algorithms.

As a graphing tool, the color version provides for painting color under the curves on a graph. With a single command, colored graphs can be implemented on model 4662 or 4663 interactive digital plotters for camera ready color plots, slides, transparencies, or full size color flipcharts.

Subroutines Enhance CRT Terminal Usage With PDP-11 Computers

VIDIO/11 and SCRNIO/11 subroutines provide independence from terminal model and video screen management for CRT terminals. Announced by Pennington Systems, Inc, 65 S Main St, Pennington, NJ 08534, the packages enhance the use of video terminals on DEC PDP-11 computers under the RT-11, RSX-11M, RSX-11D, and IAS operating systems. Both support various terminals including those manufactured by DEC, Hazeltine, Infoton, and others.

VIDIO/11, a library of subroutines callable from FORTRAN, BASIC+2, or COBOL, offers the applications programmer independence from specific terminal model. It provides protected fields on any terminal, cursor control on terminals supporting it, human engineering for terminal input, and a "no echo" option for sensitive data input.

Using SCRNIO/11 subroutines and utilities, users can develop a screen format, store the format, then retrieve it through an applications program, and manipulate the format and defined fields through subroutine calls. Multiple formats can be used simultaneously, with one defining the top half of the screen and others defining the lower half. Last line of the screen is reserved for error messages and operator interaction.

VIDIO/11 is supplied as an object library on magnetic tape; SCRNIO/11 (including VIDIO/11) is provided as an object library and set of standalone utility programs on magnetic tape. Prices for one CPU and operating system are $1500 and $3500, respectively. Circle 299 on Inquiry Card □

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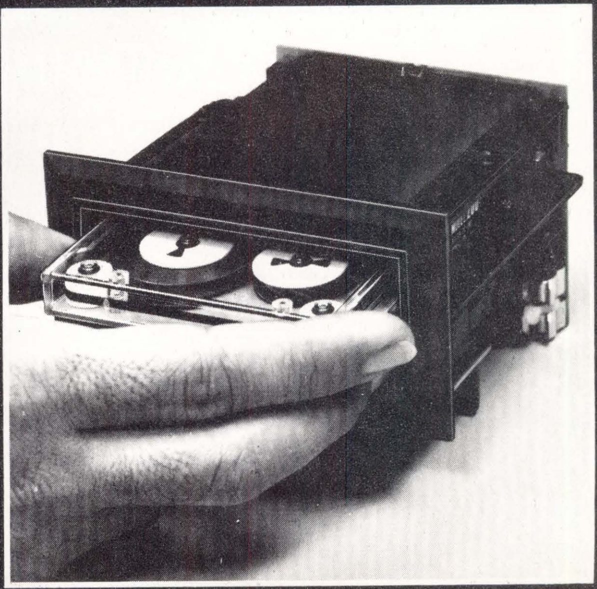

APPLYING MICROPROCESSORS TO MACHINE TOOL CONTROLLER DESIGN, PART 2

Thomas A. Seim

Desert Microsystems, Incorporated, Pasco, Washington

As pointed out in Part 1 of this discussion which appeared in March, numerical control of machine tools, once strictly the province of specialized controllers and minicomputers, is now commonly handled by microcomputers. In such applications, the mix of hardware and software can be the difference between success and failure.

Parabolic Interpolation

Machining of curved surfaces presents a problem for linear interpolation. One solution segments the curved surface into many short chords; the number of segments required is determined by the accuracy necessary and the radius of curvature. Another solution is higher-order interpolation. Parabolic (second-order) interpolation uses an acceleration term as well as velocity and position. Fig 5(a) illustrates one axis under parabolic control. Acceleration, $\ddot{x}$, is constant throughout the movement, and velocity, $\dot{x}$, varies linearly. Under linear interpolation, velocity is constant. An arbitrary contour can be approximated with parabolic segments; actually, the parametric functions of time are approximated. In Fig 5(b) the circular arc segment is representative of an application of parabolic interpolation. The x and y axes are commanded to follow parabolic paths that approximate a circular path. Several arcs can be combined to form a complete circle [Figs 5(c) and 5(d)]. The surface finish, or smoothness, of a contour, machined using several parabolic segments, is better than with linear segments even if the contour errors are the same.

Two difference equations are used in the contour generation software

$$\dot{x}_{k+1} = \dot{x}_k + \Delta T \cdot \ddot{x} \qquad (6)$$

$$x_{k+1} = x_k + \Delta T \cdot \dot{x}_k \qquad (7)$$

Incremental position values are computed as before by multiplying the time step by the velocity, but velocity is constant, and now it also is computed by a second difference equation using acceleration. Output of the velocity difference equation is an input to the position difference equation; and as velocity changes linearly with time, position changes parabolically.

Programming the two difference equations is complicated by the $\Delta T \cdot \dot{x}_k$ multiplication. By choosing the value of ΔT to be a power of two, the time required for a 16-bit multiplication is avoided. The time step of 1/128 s is close enough to the original design choice of 1/100 to be inconsequential, and the rest of the code is multiple precision additions.

Contour Path Termination

All contouring methods require some method of testing for the stopping point. This is an obvious necessity, but presents some less than obvious problems. For instance, the current position can be continuously compared to the final position, commanding the interpolation process to stop when reached. However, that comparison cannot be continuous; more realistically, it occurs only at sampling intervals (128/s). Likely, the endpoint would be missed for velocities above 128

Because this is a continuation of the discussion begun last month, all figure and equation numbers follow those assigned to Part 1.

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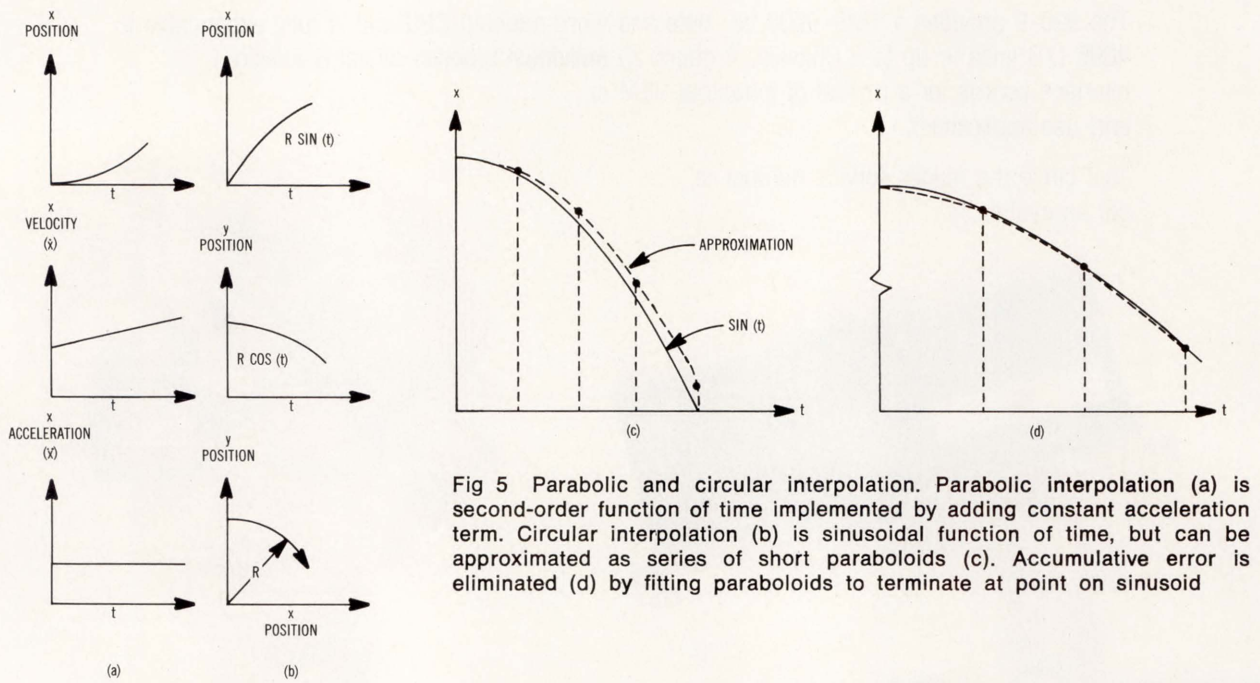

Fig 5 Parabolic and circular interpolation. Parabolic interpolation (a) is second-order function of time implemented by adding constant acceleration term. Circular interpolation (b) is sinusoidal function of time, but can be approximated as series of short paraboloids (c). Accumulative error is eliminated (d) by fitting paraboloids to terminate at point on sinusoid

mils/s [7.68″ (19.51 cm)/min]. The machine tool would overshoot the endpoint by an amount not greater than the distance traveled during sampling points, but would return to the correct final position.

An alternative software technique modifies the desired velocity slightly to assure that the total travel time is a multiple of the sampling interval. The number of time steps initializes a counter decremented every sampling interval until it is zero, which terminates the contour. Unitizing time eliminates comparing 24-bit numbers, keeping track of direction and axis, and any external hardware. However, while it is easily applied to linear interpolation, the correction is more difficult for circular and parabolic interpolation. The first step calculates the total travel time, T, for linear interpolation: $T = \Delta x/\dot{x}$. Then, T is corrected to be a multiple of the sampling interval (for 1/128 s, T is truncated to seven fractional bits), and velocities are recomputed with T′, the new value of T:

$$\dot{x}' = \dot{x}(T'/T)\,;\ \dot{y}' = \dot{y}(T'/T) \qquad (8)$$

Servo Control

Choice of the servo is highly application dependent, but basically two types are used: dc servos and stepping motors. Stepping motors are purported to be more compatible with computers, being quasi-digital in nature. However, little simplification is actually achieved using stepping motors, and their peculiarities can be rather troublesome.

Fig 6 illustrates a typical dc servo control system. This system has two feedback control loops: a velocity and a position control loop. The former uses a tachometer for velocity feedback to the amplifier—no software function is necessary. A digital shaft encoder, mechanically connected to the servomotor (either directly or through gearing), provides position feedback. If this is an incremental encoder, an up/down counter is needed for short range position tracking. Other types give absolute angular position. Linear position encoders may also be used. These eliminate measurement errors due to gearing by measuring the position of the slide directly.

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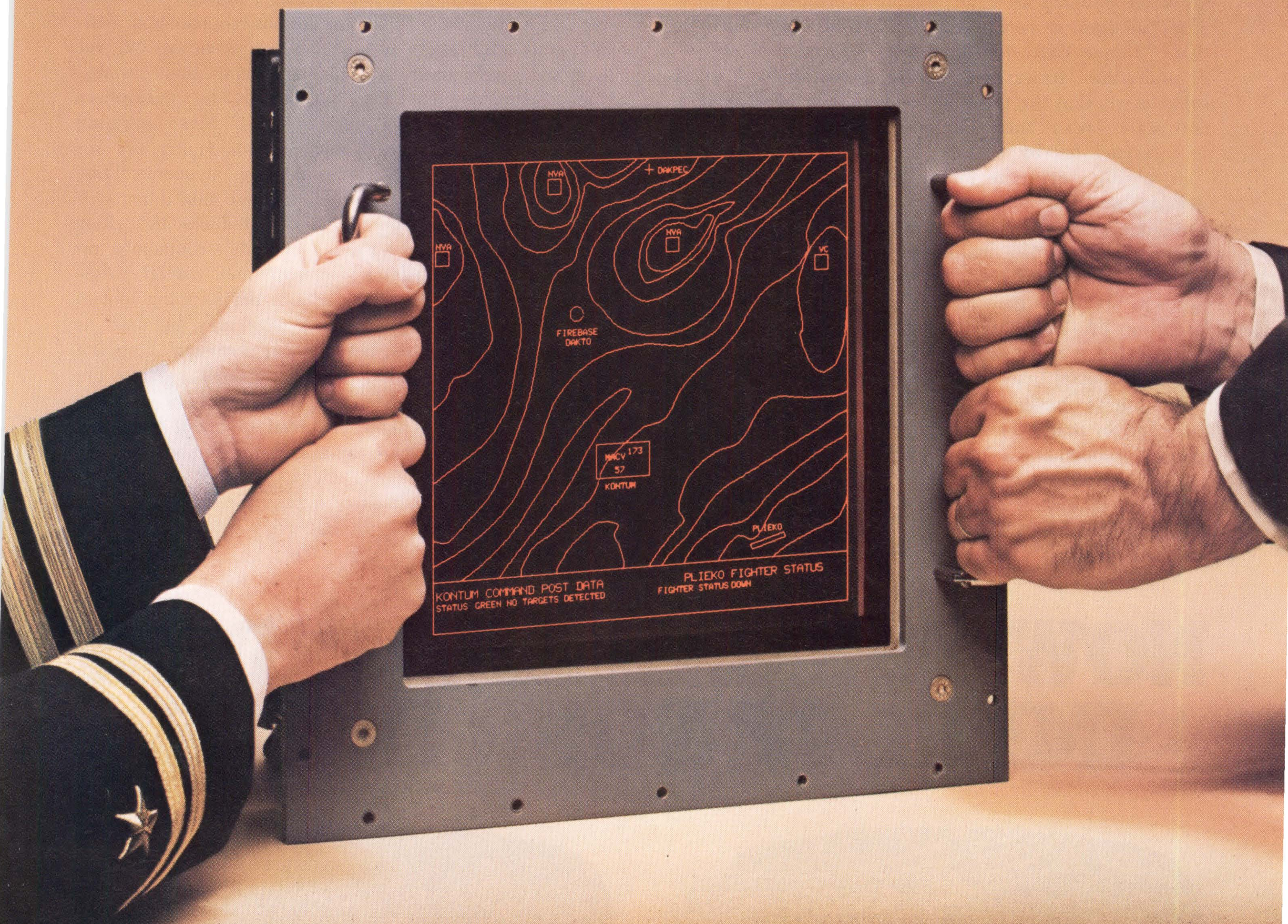

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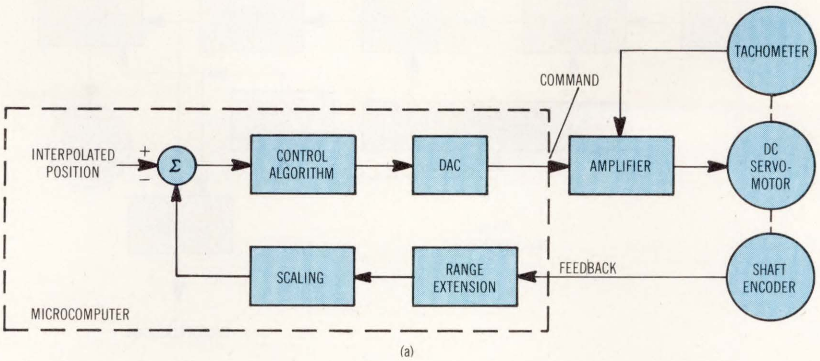
Regardless of what type of encoder is used, it is likely that extension of the encoder range will have to be provided in software. A lead-screw driven slide, for instance, has to be turned many revolutions during its full travel; an absolute encoder attached to the lead screw is counted to give complete position feedback. This function is performed by software; the box entitled "Range Extension" monitors for encoder overflow or underflow (forward or reverse revolutions). A possibility exists that the position feedback will have a different scale factor than the interpolated position; this is corrected for by a scale-factor adjustment.

A position error is found by comparing the interpolated position to the feedback position at every sampling point. This error is processed by a control algorithm, consisting mainly of proportional gain, and is used to command a velocity to the servo drive. Proper adjustment of the control gain prevents the servo from speeding up suddenly at each sampling point, and assures that it will turn smoothly under velocity control. Integral control may also be included in the control algorithm to minimize position error during interpolation and to bring the machine slide exactly to the endpoint (proportional control would leave it a small distance from the endpoint). Derivative control is used in the small number of machine tools requiring high dynamic performance (very fast feed rates).

Stepping motors must be driven by a pulse train. Because this can be difficult to generate with software (and would completely occupy the processor), hardware is used. The method shown in Fig 7 utilizes two 6-bit rate multipliers (SN7497) under microprocessor control. Rate multipliers are devices of great utility, yet they are rarely used in frequency generation designs. One reason is that the output of the multipliers has a large amount of pulse "jitter." Since stepping motors stall under such conditions, rate multipliers are generally unsuitable for commanding steppers. This, however, is solved by dividing the rate multiplier output by a 2-decade counter, which reduces the jitter to 1% of its original value. A module—commonly referred to as a "translator"—converts the digital pulses to the appropriate drive currents to the stepping motor.

A shaft or linear position encoder may be used as with the dc servomotors, but it is not necessary. Stepping motors have no cumulative error as long as they are operated within specifications. Position is known by counting steps; a counter is added to count a limited number of steps (at least the maximum number between sampling points).



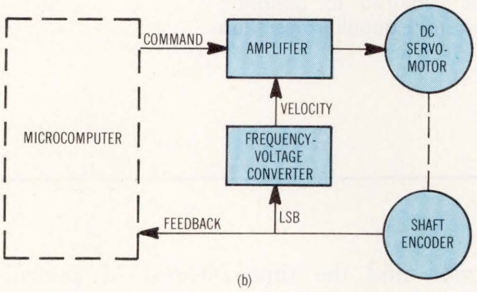


Fig 6 Typical dc servo control system. Feedback control of position servos (a) is implemented partly in software (elements within dashed box) and partly in hardware. Inner velocity feedback control loop is entirely hardware. Tachometer can be eliminated (b) by frequency to voltage converter driven from shaft encoder least significant bit

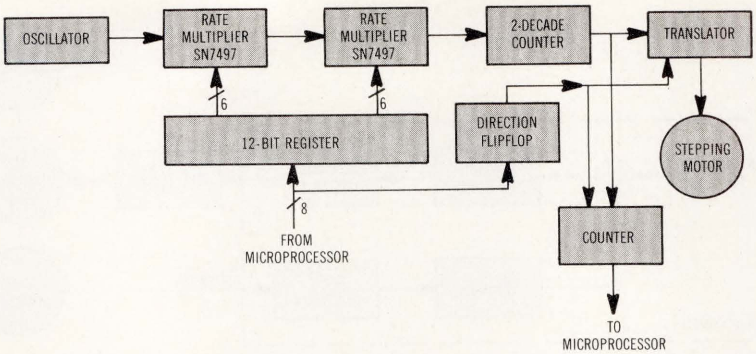


Fig 7 Stepping motor drive. Unlike dc servo in Fig 6, no encoder is coupled to shaft. However, feedback control is required to generate command frequency. Steppers also have more inherent peculiarities than do dc servos (eg, resonances)

Control Loop Software

Fig 6(a) illustrates a 2-loop system controlling velocity (the inner loop) and position. Portions implemented in software include range extension scaling, differencing, and the control algorithm. Remaining hardware components—digital to analog converter (DAC), amplifier, dc servomotor, tachometer, and shaft encoder—are commercially available to meet a wide range of applications. The position control loop uses both hardware and software, while the velocity control loop is entirely in hardware. It is possible to derive velocity information from the shaft encoder, eliminating the need for the tachometer, and control velocity with software, but this can create control problems due to quantization effects in the velocity computation. Solutions to this problem are beyond the scope of this discussion. A compromise that still eliminates the tachometer is illustrated in Fig 6(b). Velocity information is derived from the shaft encoder with a frequency-voltage converter.

Proportional-integral (PI) action in the control algorithm is satisfactory for most applications (derivative, or velocity, control is exercised in hardware). Proportional control generates a control action (velocity command to the servo in this case) that is proportional to the control error. Control error, computed as a triple-precision 24-bit number, is converted to a single-precision 8-bit number. Values greater than eight bits are limited to the maximum positive or negative 8-bit representation. The complete proportional calculation takes less than 350 μs with the 8080 microprocessor.

Integral control is used to trim small offset errors. Any error will eventually integrate to a value large enough to cause a control action. This assures that the machine will move to a new commanded position and not just to a nearby, but different, position. Integral control is computed as the product of the integral control gain and the time integral of control error (the integration is approximated by summation). The time integral is stored as a 16-bit double-precision number. Control error, limited to eight bits, is added to the integral at the sampling frequency. A full-scale error saturates the integral in 2.56 s.

Programming integral control requires dealing with both control system and software design problems. It is possible that the integral will saturate—reach the maximum 16-bit value. It must not be allowed to "wrap-around," the term for overflowing during signed arithmetic, which is catastrophic to the control system. This is prevented by using a signed addition subroutine that checks for overflow and limits the result to the maximum values.

Summary

A machine tool controller is basically a digital sampled data control mechanism. Properly designed algorithms can be adapted to currently available 8-bit microprocessors. The availability of high performance 8- and 16-bit microprocessors such as the 8086 will ease the implementation problems, particularly with the availability of hardware multiply and divide.

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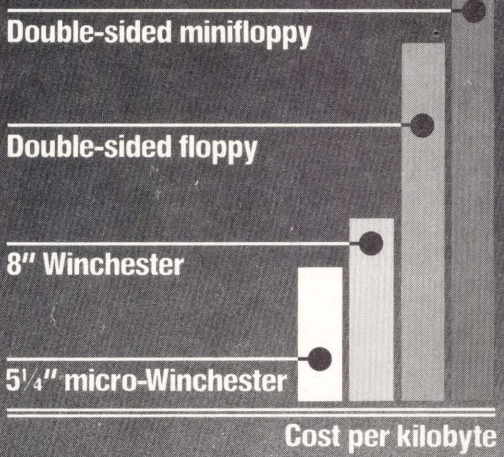

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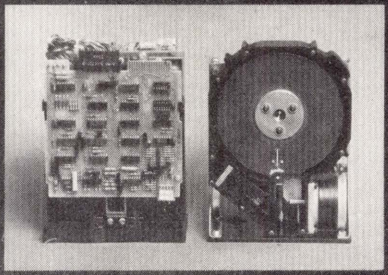

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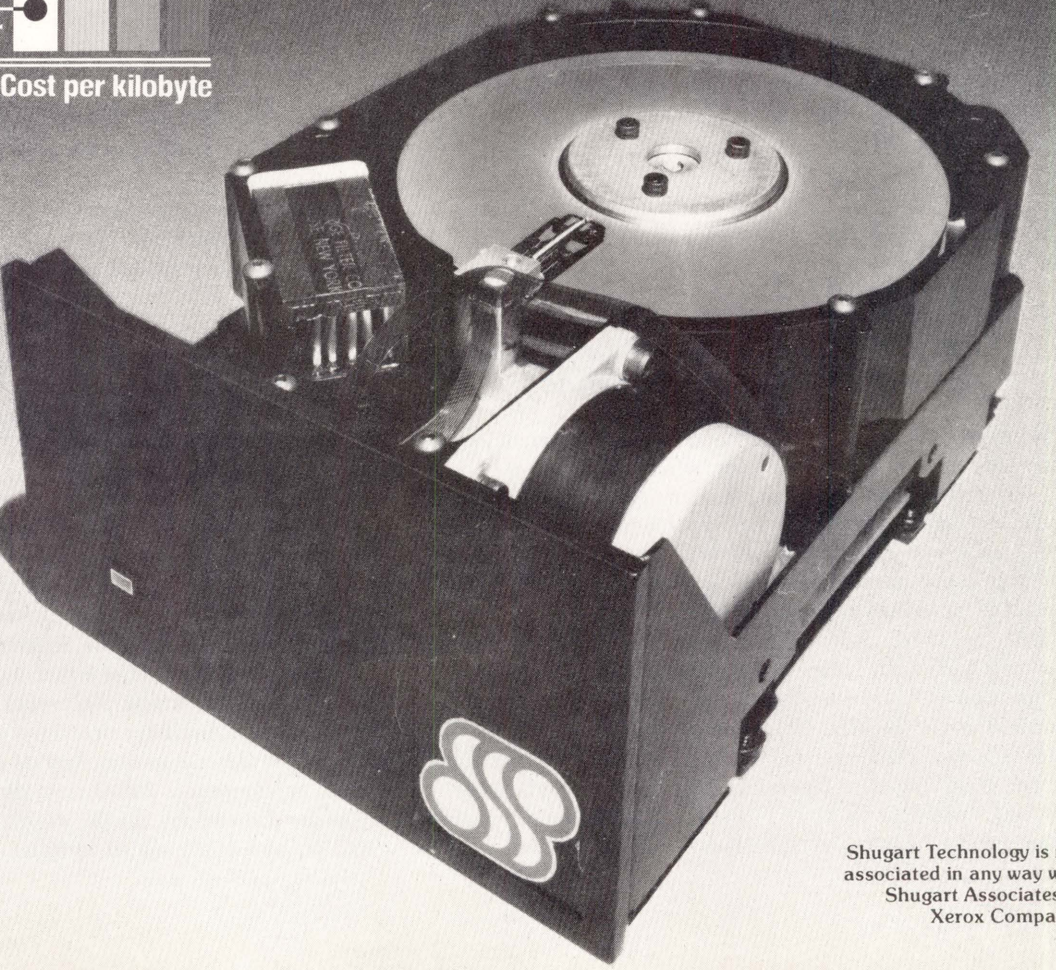

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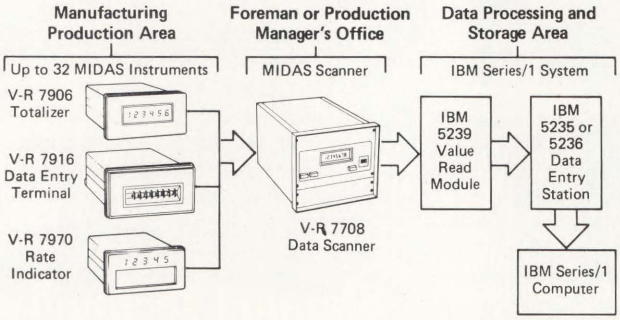

Transfer of machine data from production areas directly to an IBM Series/1 computer can be accomplished with a system introduced by Veeder-Root, 70 Sargeant St, Hartford, CT 06102. Data from as many as 32 MIDAS (modular industrial data acquisition system) components can be fed to a data scanner located at a distance of up to 3000 ft (475 m). A front panel thumbwheel switch on the scanner allows a foreman to select a display of data from a particular station. Count data are converted by the interface into bit serial format at either 3840 or 110 baud.

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Interfaces are independent, with data transfers made through each with either programmed I/O or data channel. Resolution is 12 bits in four different voltage ranges. A-D throughput is 22 kHz. Software support provided by the Sensor Access Manager (SAM), which runs under the company's Realtime Disc Operating System (RDOS), allows sensor I/O applications to be quickly and efficiently programmed in FORTRAN IV, FORTRAN 5, and assembler.

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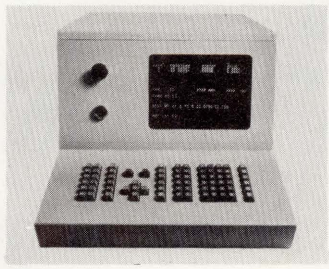

Each axis can be shrunk or expanded through independent programmable scaling, and is program correctable for temperature and machine inaccuracies. Automatic alignment by sensing an edge either mechanically or electrically compensates for wrong placement of a part or a fixture on the machine. Auxiliary proximity sensors enable automatic tool offset determination. Inputs can be from floppy disc, tape, or computer. P/ROM is available as internal memory. Worker dimensions can be digitized off a part or drawing and automatically scaled to finish size.

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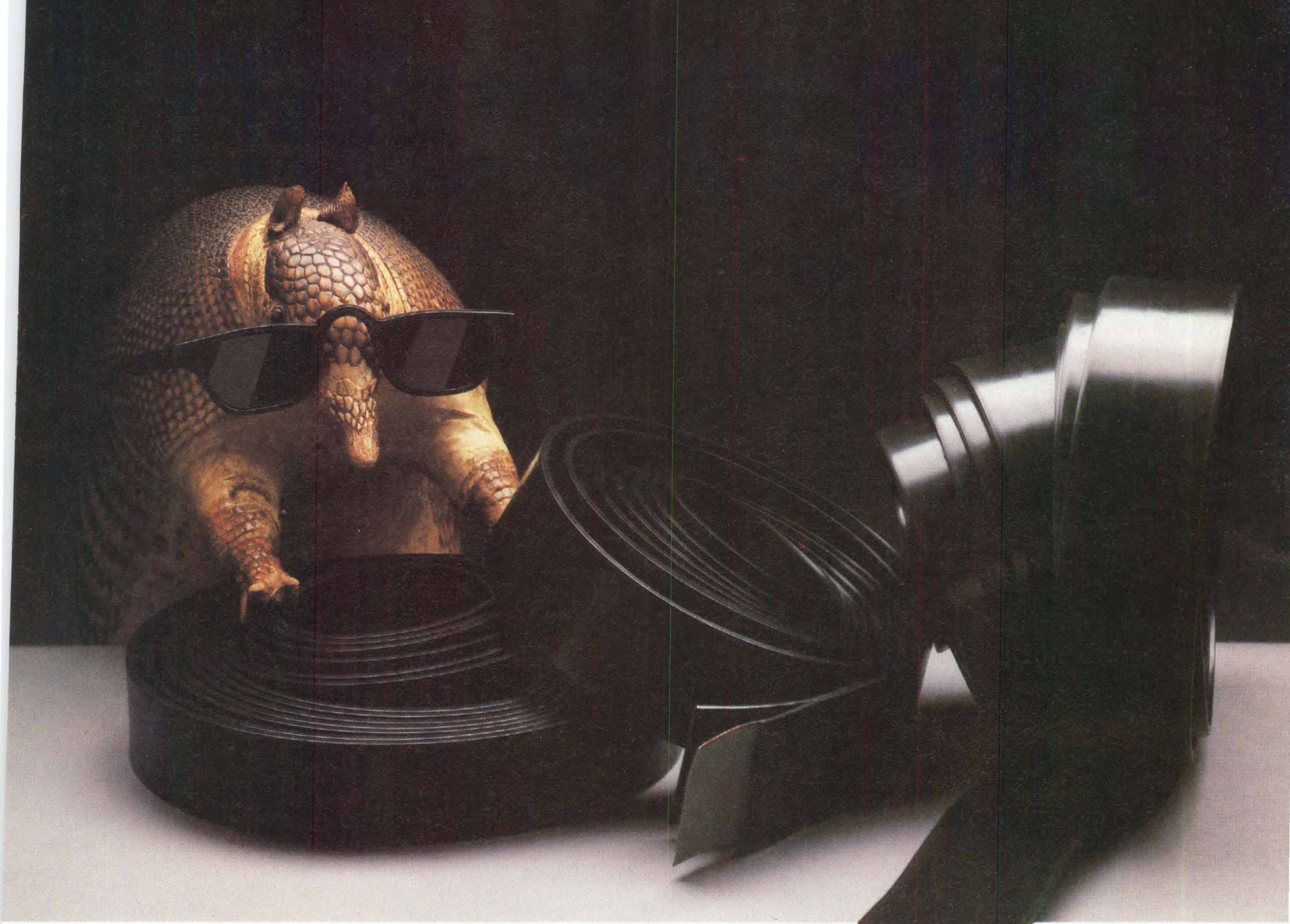

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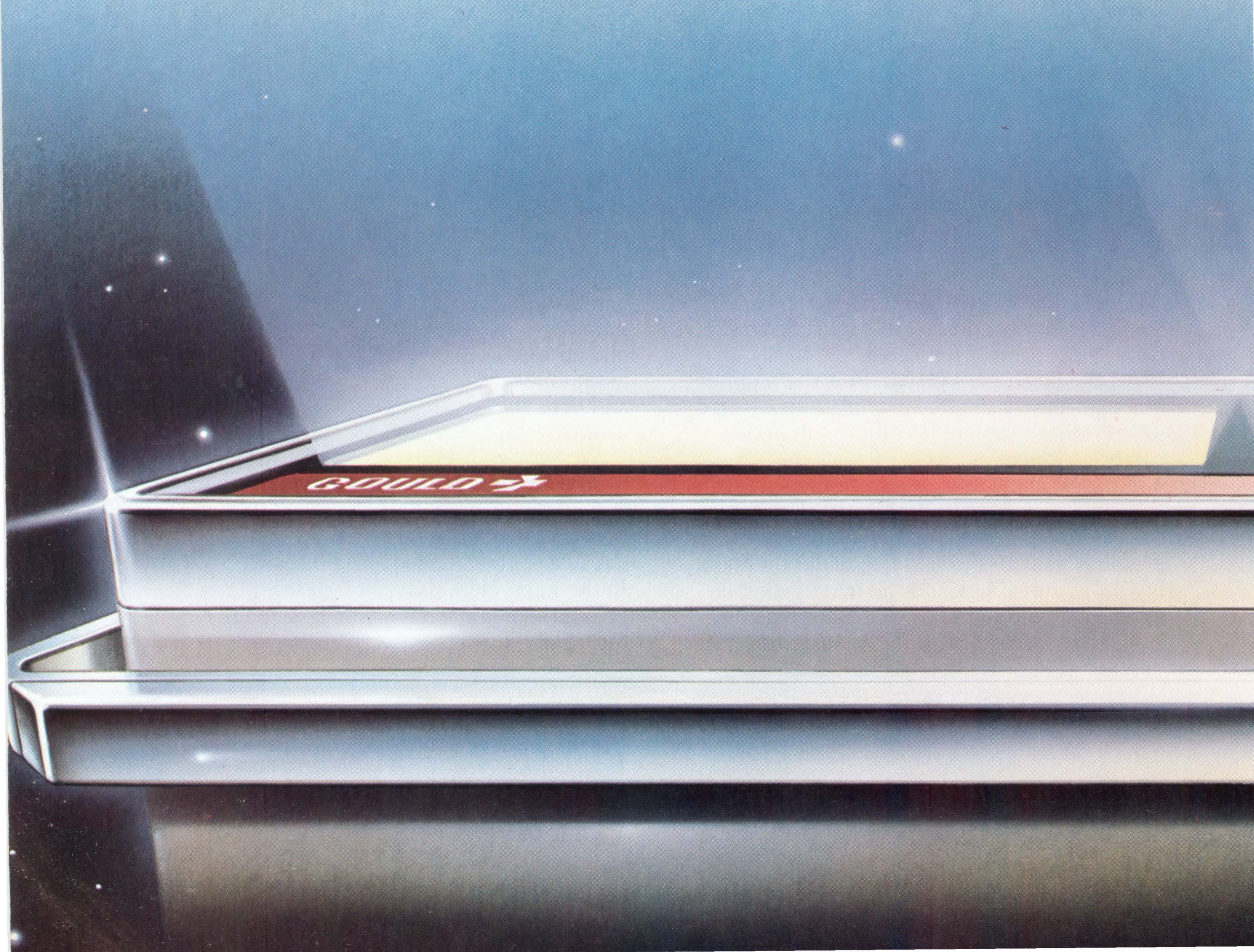

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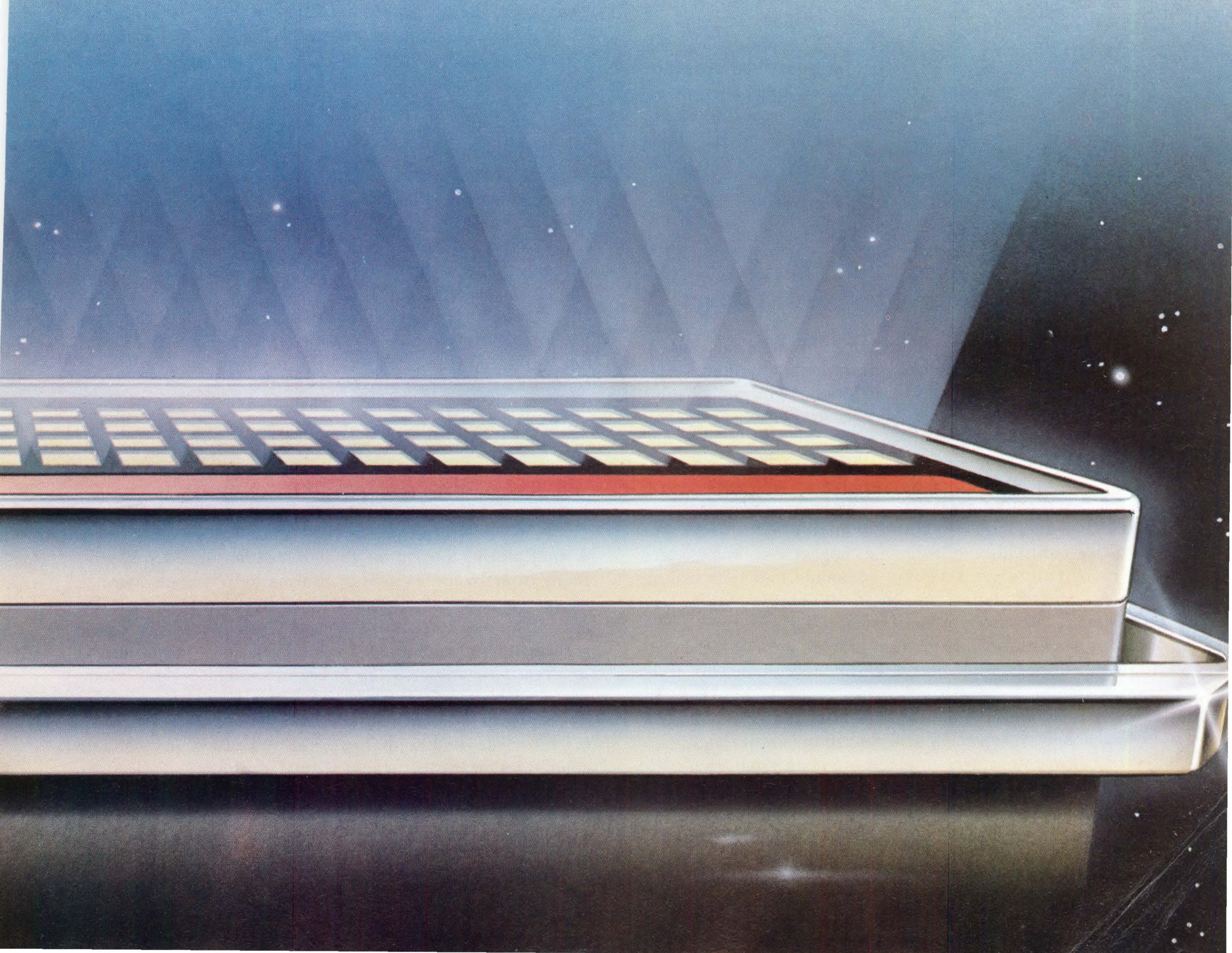
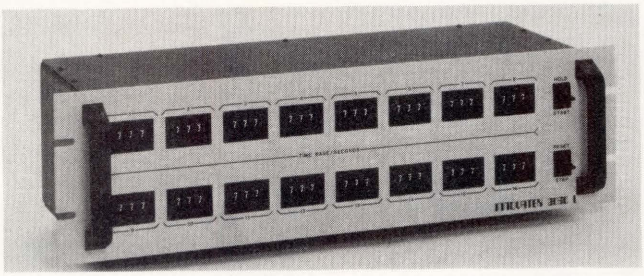


16-Channel Programmable Controller Maintains ±1-ms/Channel Repeatability



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Circle 454 on Inquiry Card

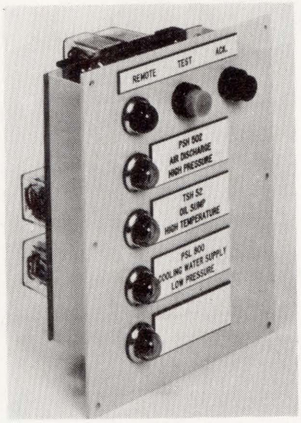
Color Graphics Video Display Aids Realtime Remote Monitoring

Centralized monitoring and control of material flow or levels of liquid in remote vessels can be maintained by the microprocessor controlled Tru-View™ graphic display system. Simultaneous colored bar graph displays show levels in up to 24 vessels with 4- to 20-mA controls. Designed by Drexelbrook Engineering Co, 205 Keith Valley Rd, Horsham, PA 19044, the system contains a self-check alarm system that warns of open circuits or shorts in a control loop by closing an alarm relay and changing the vessel's bar graph to blinking yellow. The operator acknowledges alarms by entering a keyboard command and then calling up a system malfunction display to pinpoint the fault.

Normally the operator sees green bar graph representations of vessel levels, which are updated approximately 20 times/min for realtime control. Optional high and low level alarms change a vessel's green bar graph to blinking red and sound an alarm to alert the operator that a setpoint has been reached. When the alarm condition is relieved, the affected bar graph returns to green to indicate the true level. Setpoints are entered and changed through the operator's keyboard.

Circle 455 on Inquiry Card

Annunciators Monitor Process Points

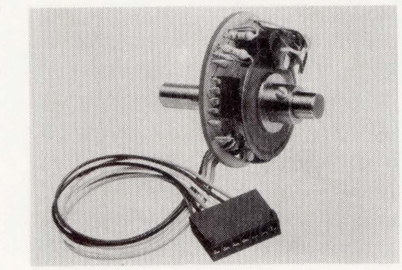


Self-contained units with weatherproof faces suitable for indoor or outdoor applications, RAS alarm systems and RSM shutdown monitors from Maverick Controls, Inc, 636 Sheridan Dr, Tonawanda, NY 14150, include 1 spdt contact/system and 1 spdt contact/point for customer use. Relay alarm systems monitor contacts and turn on a trouble light if a contact opens. Shutdown monitors turn on a light and open a contact when trouble is located.

Circle 456 on Inquiry Card

Incremental Encoder Provides Manual Interface to Digital System

The Digipot[R] incremental encoder introduced by Sensor Technology, 21012 Lassen St, Chatsworth, CA 91311, serves as an input device for up/down counters, NC machines, and speed or position controls. It provides manual control for positioning X-Y tables or stepper motors. Resolution is up to 256 counts/rev. TTL compatible single- or double-channel output provides 10-mA max source or sink current. The device operates over a 0 to 70 °C range at up to 100% relative humidity noncondensing. It will withstand a 5-G shock for 11 ms and 2-G vibration at 0 to 60 Hz.



Circle 457 on Inquiry Card

Data Acquisition System Operates at Remote Sites

A multiplexing system for remote location data acquisition scans from 16 to 224 sensor information channels at rates up to 16k samples/s. Data are then digitized to 8- to 12-bit resolution and the resultant serial bit stream is either recorded on magnetic tape for later recovery or transmitted to a receiving station at up to 2M bits/s. The series 300, introduced by the Data-Control Systems Div of General Indicator Corp, PO Box 860, Danbury, CT 06810, consists of up to 15 cards and a power supply housed in modular assemblies or NEMA boxes. Digital encoder and decoder cards are available for low frequency data, and frequency modulated analog encoders for high frequency applications.

Circle 458 on Inquiry Card

International Cooperation Sought For CAD/CAM Development Project

In an attempt to foster international cooperation on CAD/CAM research and development, Computer Aided Manufacturing-International, Inc (CAM-I) has announced the CAM-I Framework Project. The purpose of this long-term cooperative development project is to set up a general system architecture that will serve as a framework for all CAM-I and user developed applications. Project results will define the nature of a CAD/CAM framework, the constraining boundaries for applications, and the necessary interfaces and interactions between applications. The project was initiated in order to gain the advantage of an international effort that would exceed the capacity of individual companies, and because each of the individual companies tend to be biased toward particular environments. It will also permit the costs to be shared more evenly.

In general, the framework will be independent of present or predicted computer hardware/software configurations. It will enable simple orientation by individual companies, will permit easy and efficient replacement or enhancement of unique applications systems, and will allow users to evolve into the total CAD/CAM system at their own paces. Overall, it will provide a central point for absorbing and dispensing worldwide research and development information. Information is available from CAM-I, Research Management Dept, 611 Ryan Plaza Dr, Suite 1107, Arlington, TX 76011.

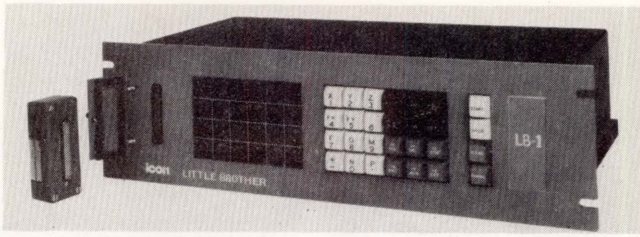
I/O Interface Subsystems Complement Process Control Computers

Four process input/output interface subsystem packages for the company's MODACS III family of process industry products have been introduced by Modular Computer Systems, Inc, PO Box 6099, Ft Lauderdale, FL 33310. Each includes cabinet and support software and is complete except for application interface modules.

The 1800-A16A and -A32A intelligent remote process interface systems include an 1800-4 CPU board with 128k bytes of solid state memory, system protect, control panel and MAX II/III operating system. Adding peripherals provides standalone capabilities. The -A16A supports 16 process I/O interface cards and two additional I/O bus options such as communications links and secondary controllers. All digital and analog power is included. The -A32A supports 32 process I/O interface cards and two additional I/O bus options. It contains all features of the -A16A plus an additional expansion file. Both systems can be field expanded to support up to 64 process interface cards. Operation as a remote node is possible with the addition of a supported compatible communication link and remote diagnostics. -Z16A and -Z32A function as local process I/O interface subsystems operating as peripherals on the CPU I/O bus, but do not include internal CPU level intelligence.

Circle 459 on Inquiry Card

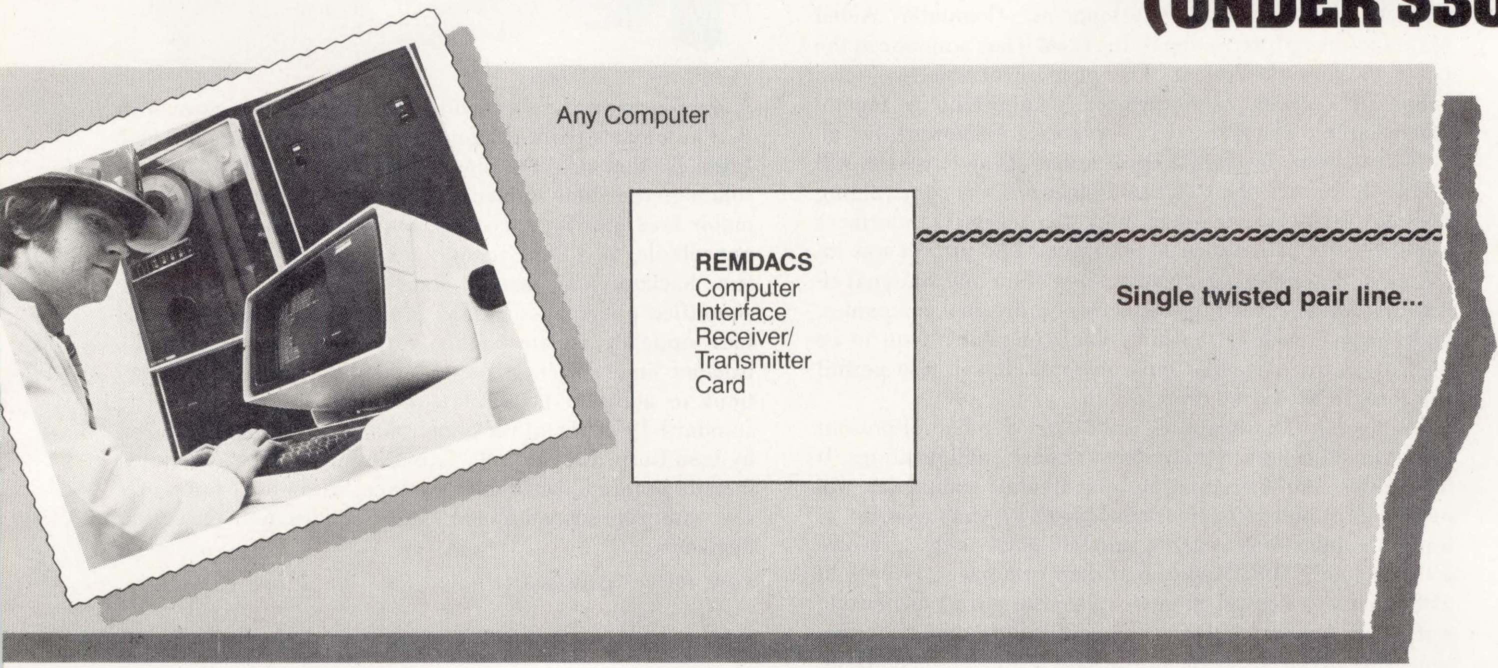
Programmable Control Automates 2-Axis Positioning System



A microprocessor based computer numerical control unit that automates point to point positioning systems, the LB-1 Little Brother provides simultaneous 2-axis control for absolute/incremental dimensions, with separate programmable feedrates for each axis. Standard features include a nonvolatile, 1k x 8-bit memory (expandable to 4k) with battery backup, and manual data input via keyboard for simplified programming. The programmable unit contains four optically isolated relay outputs and four optically isolated limit switches. An LED display indicates all functions in addition to absolute position of each axis. The standard 19" (48-cm) rackmountable unit is manufactured by Icon Corp, 156 Sixth St, Cambridge, MA 02142. Features include program dwell, mirror image, absolute position preset, subprogram/call/repeat, and conditional execution demands. □

Circle 460 on Inquiry Card

REMOTE DATA MADE (UNDER $30



A NEW CONCEPT. A NEW PRODUCT.

REMDACS™ is Intersil's *Remote Data Acquisition and Control System*. It handles remote analog and digital data. For monitoring, logging and control. It communicates with up to 512 remote stations. Up to a mile away. Very accurately. And inexpensively. Over a single twisted-pair line.

A LOW-COST SYSTEM.

REMDACS is a simple, economical system. Averaging $30 per channel for typical systems. Even less for larger systems. Installation costs are reduced because REMDACS uses a single twisted-pair line. No multiple cable runs. No conduit in most cases, since power is only 24 VAC. (Many installations can even utilize existing wiring.) And remote stations all daisy-chain onto one twisted-pair. So you can add on more inputs or controls very inexpensively.

DIGITIZE AT THE SOURCE.

REMDACS uses smart remote stations. Each containing a 16-channel multiplexer, a 12-bit A/D and a microcomputer. They gather and digitize temperature and voltage data right near the source for higher accuracy and lower signal degradation. Then they send the data back to the host computer in serial format. With auto error-checking at both ends of the transmission.

TRANSPARENT TO THE HOST COMPUTER.

A central receiver/transmitter station polls all remote stations. Up to 95 channels/second. In a high-security, serial-message format. The host provides only address and action commands. REMDACS provides system control and communications protocol. Converting the data for virtually any host computer. To the host, REMDACS is transparent, looking like a simple data source or control device. Up to 512 remote stations may be attached to one receiver/transmitter, providing thousands of data input channels and control outputs.

A KIT FOR EASY START-UP.

Here's a good way to get familiar with the concept fast. And come out with a working system. The REMDACS Evaluation Kit provides all you need: Two remote station cards, a receiver/transmitter card, an RS-232 serial interface card, a detailed technical manual, a 24 VAC transformer, cables and connectors. All data acquisition and control routines are debugged and stored in firmware. Total tab: $995. And worth every penny. Just in man-hours saved.

Electro/80

Electronic Show and Convention
Boston — Hynes Auditorium
May 13—15, 1980

Daniel T. Carroll
Keynote Luncheon Speaker

Arthur G. Foyt
Chairman of Program Committee

Electronics Leads the Way—theme of the 1980 East Coast Electronic Show and Convention, to be held in Boston, Mass from Tuesday, May 13 through Thursday, May 15—is demonstrated by concentration of the technical program on microprocessors and associated technology. Nearly one-half of the 34 conference sessions relate to instrumentation and microprocessors and over three-quarters are of interest to engineer/designers of digital circuits. Arthur G. Foyt of the MIT Lincoln Laboratory, chairman of the Electro/80 program committee, emphasizes that "special attention is on microprocessors, including chip configuration, memories, distributed systems, and software/hardware considerations." The range of subjects extends to include analog subsystems and devices, interfaces and bus architecture, and fiber optics for digital communications. A separate special tutorial seminar will cover very large scale integrated (VLSI) circuits.

Schedule of Events

Professional sessions are organized into three 2-hour blocks each day starting at 9 am, 12 noon, and 3 pm, with 1-hour breaks. The special-fee seminar on VLSI will be conducted on Monday, May 12. A Keynote Luncheon Address, by Daniel T. Carroll, president of Gould, Inc, will also take place on Monday.

All professional sessions will be held in the Boston-Sheraton Hotel. Exhibits will be on both floors of the adjacent Hynes Memorial Auditorium, with exhibition hours from 9 am to 6 pm Tuesday and Wednesday and 9 am to 5 pm on Thursday. A film theater, covering technology ranging from the microprocessor to aerospace, will operate continously each day in the hotel from 10 am to 4 pm. The traditional All-Industry reception will be held in the Grand and Constitutional Ballrooms of the hotel on Tuesday evening. (Price per person of $12 will include hors d'oeuvres, soft drinks, wine and beer, entertainment, and two liquor beverages.)

Professional Program

Because so much of the Electro/80 professional program is related to the everyday work activities of a significant portion of *Computer Design*'s readers, more than 25 of the total of 34 sessions are summarized briefly in the following sections. In addition, a complete listing of all sessions is provided in the Conference Map, with those of interest emphasized by colored blocks. The information included on both summaries and map is based on the latest preliminary material available at press time, but changes could occur later in final dates, times, and places. Therefore, the Electro/80 official program should be checked when setting up a final schedule of sessions to attend.

Microprocessor/Microcomputer State of the Art

Increasing weight of the development and maintenance of software, recognized for some time as a major trend in the organization of microprocessor based system, continues to tip the software/hardware cost ratio farther from equality. As will be pointed out in session 19, users are no longer satisfied with systems that require a great deal of engineering in order to be practical. They expect both ease of use and reasonable prospects that neither software nor hardware will become rapidly obsolete. Considerable architectural symmetry, however, has resulted from the growth of 16-bit devices.

Further implementation of high level language support has helped alleviate the inherent problems. This trend to high level languages, accelerated by the increased computing capacity per processor plus falling memory costs, necessitates a knowledge of the strengths and weaknesses of those languages. Session 31 will complement the software/hardware ratio discussion by explaining language selection criteria and their influence on future trends in education and computer architecture. Particular emphasis will be on Pascal, C, and ADA.

Impact of the 16-bit microprocessor, high performance microcomputers, and multiprocessor systems, as well as the high level languages, has influenced changes in the requirements for development systems. Evolution of next generation systems and their expected characteristics will be defined by session 23, starting with recognition of what is needed and whether or not existing systems can be extended with new emulators and software to meet those needs. Direct comparison of some existing development systems and how each relates to specific requirements will be covered in session 27. Representatives from four competitive companies will offer formal presentations and then take part in a panel discussion.

Single-chip microcomputers as well as their functions with other components in complete systems will be handled by sessions 29 and 33, respectively. The discussions will follow the evolution of single-chip microprocessors to single-chip microcomputers and then to systems applying such devices. Parallel and serial slave interfaces added to master bus interfaces have modified some single-chip devices. The result has been multiprocessor systems with potential for multitasking, slave processing, and loosely coupled systems. True single-chip "total" solutions, with interface circuits onchip, will be discussed to make designers aware of what they can expect in the future, as well as of the expected economies.

Influence of the microprocessor on instrumentation is often considered close to revolutionary. "Intelligent" instruments are no longer a rarity; instead they are becoming close to universal. As will be explained by session 9 speakers, a modern test instrument contains as much computing power as a calculator controller. Designers and manufacturers must determine how to use this capability to benefit the users, rather than to tie it on as practically a mere gimmick to enhance sales.

Whatever the original concept might have been, and no matter how accurate or erroneous that concept proved to be, the "personal computer" has progressed far from a device to be used by hobbyists. Today the great majority are used in laboratories, in offices, and in a myriad of other applications, few of which are classed in the hobby category. Some uses will be illustrated in session 1, but these hardly touch upon the possible total. If the statement that 500,000 personal computers are in use and 30,000 more are purchased each month is accurate, there is no question that acceptance has progressed far beyond the range of the not completely descriptive term "personal computer."

Communications

As might be expected, two of the four sessions concerning communications are on fiber optics. Session 24 will be devoted to the current status of fiber optic communications system components: light sources, detectors, and fibers. Emphasis will be on the two wave length ranges centered on 0.83 and 1.2 μm and on considerations for an optical link. Session 28, in turn, will review bus components and systems, the status of each, and applications. Speakers will be from both industrial and military organizations.

Further communications related papers will be presented in sessions 30 (electronic movement of information) and 34 (application of digital technology in telephone loop plants). The first session will include methods of conveying information from the chip through the board, and then to the computer. Both current and proposed techniques will be included in the discussion. In the second session much of the presentation will be on experiences, how to cope with present requirements, and what to expect as future solutions to existing problems.

Memories

Three distinct areas of memory technology—floppy disc, solid state bulk, and microprocessors—will be highlighted in sessions 7, 10, and 11, respectively. The first of these will portray the expansion of floppy disc technology for data storage. It will examine the impact of developments in speed, density, and error correction for the floppy, and then compare the impact of the 8" rigid disc. In the second session, the influence of both serial and random access solid state devices on bulk storage memory applications will be discussed, with a portion devoted to considerations for the next generation. Dynamic RAM, CCD, bubbles and ROM-P/ROM will be included. The final session of this trio will be devoted to the key issues involved in choosing memories for microprocessors—particularly those that will be available for the next five years.

Bit-slice circuits and their influence on reliability and performance of microprogrammed machines will be covered by session 25. Emphasis will be on devices and techniques for error detection and correction in memory systems, plus techniques and devices available as bipolar LSI microprogrammed sequences.

Floating Point Processors

1980, according to the speakers in session 14, will be the year that removes hardware floating point processors from the status of expensive options available only on high performance computers. On some minicomputers it will become a standard feature; furthermore, the semiconductor industry will introduce single-chip floating point processors. Major hardware alternatives for floating point processors—from the single-chip approach to a fully parallel approach requiring several hundred ICs—will be discussed. In addi-

Electro/80 Session Map*

	GRAND BALLROOM	CONSTITUTION BALLROOM	REPUBLIC BALLROOM	INDEPENDENCE BALLROOM
Tuesday May 13 9-11 am	1/Personal Computers in OEM, Scientific, and Industrial Applications	2/Integrated Solid State Microwave Amplifier Design	3/IEEE-488: User Fundamentals	4/State of the Art Data Acquisition Systems
Noon to 2 pm		5/Recent Developments in Communications Receiver Design	6/IEEE-488 Case Histories: Progress and Problems	7/New Advances in Floppy Disc Technology
3-5 pm		8/Current Developments and Applications in the RF Power Device Field	9/The Future of Intelligent Measurement Instruments and Systems	10/The Influx of Solid State Memory into Bulk Storage Applications
Wednesday May 14 9-11 am	11/Memories for Microprocessors	12/Applying the New Generation of Analog Computational ICs	13/Starting and Operating a Small High Technology Business	14/Hardware Alternatives for Floating-Point Processing
Noon to 2 pm	15/A Turning Point in Engineering Education (Panel Discussion)	16/The Frontiers of High Temperature Electronics	17/Techniques for Bridging the Gap Between Linear Applications and the Microcomputer	18/Floating Point Standards for Micros and Minis
3-5 pm	19/Advanced Architectures: Hardware and Software Considerations for the New 16-Bit Microprocessors and Beyond	20/A-D and D-A Converter Technology	21/New Ideas for Engineering Managers	22/High Performance Digital Gate Array —Structure, Design Methodology, and Applications
Thursday May 15 9-11 am	23/Evolution or Revolution to Next Generation Development Systems	24/Fiber Optics Communications Systems: Current Status	25/New Bipolar Circuits Enhance High Performance Microprogrammed Bit-Slice Machine Design	26/Array Processor Architecture
Noon to 2 pm	27/But How Does Your Microprocessor Development System Develop My System	28/Fiber Optic Data Bus Status and Applications	29/Total Solution on a Single Chip	30/Interdevice Communications and Bus Architecture
3-5 pm	31/Microcomputer Languages for the 80s	32/Static Protection of High Circuit Density Components and Assemblies	33/Single-Chip Microcomputers as System Components	34/Digital in the Telephone Subscriber Loop Plant

*Sessions in colored blocks are of particular interest to *Computer Design* readers

tion, tradeoffs such as performance vs chip count and precision vs complexity will be clarified.

Session 18 will focus on several proposals for floating point arithmetic. However, the discussions will also cover a number of controversial aspects that must be considered by minicomputer as well as microcomputer manufacturers. Some of these include the handling of exceptions, safe treatment of overflow and underflow conditions, and an LSI implementation.

Instrumentation

The IEEE-488 bus and its effect on instrumentation will be discussed from two user oriented bases. In session 3, manufacturers of IEEE-488 compatible products will stress the impact made by this bus on the design of systems, which specifications should be considered by system designers (and which are not important), the expected future for the bus, and the necessary communications protocol.

Session 6 will consist of a review of progress and problems, based on case histories. Users of instrumentation based on this bus will describe the system functions they have achieved, the problems they encountered, and the solutions they worked out. Part of the discussion will cover the future application of the bus. In addition, one paper in session 9 will point out IEEE-488 capabilities for enhancing oscilloscope applications.

Data Acquisition

Interfacing an essentially analog environment to the more efficient and economical digital world has caused a number

Electro/80

of problems, few of them insurmountable. Sessions 4, 12, 17, and 20, and well as part of 9, will consider those problems, particularly as they relate to data acquisition. Some of the areas to be covered in sessions 4 and 17 are the use of LSI in analog applications, microprocessor based systems with analog I/O, applications for process control, multitasking, I/O interfaces with the general purpose interface bus, how to design the necessary interface, and how to overcome difficult analog applications.

Session 12 will discuss analog IC technology, particularly as it applies to analog to digital conversion. Included will be a family of monolithic rms to dc converters, multiplier/dividers, and logarithmic amplifiers. Additionally, part of session 9 will cover microcomputer A-D subsystems for automated test and measurement.

The numerous technologies used in the manufacture of converters will be discussed in session 20. Application areas will be emphasized. Included will be monolithic converters, hybrid devices, and discrete components.

Miscellaneous

Array processors and the implications of several generally available commercial array processors will be discussed in session 26 by representatives of some of the major manufacturers of such systems. In session 22, the structure, design, methodology, and application of high performance digital gate arrays will be reviewed. Part of the discussions will include low power ECL and high speed LSI: an advanced gate array, a 400-gate array, and a 500-gate low power Schottky array.

The upper level for high temperature electronics is moving beyond the conventional 125 °C boundary, particularly in energy exploration, process instrumentation and control, and military systems. Session 16 will provide information on high temperature hybrid thick film circuits, functioning of commercial analog and digital ICs at high temperatures, operation of IIL circuits, and silicon, GaAs, and GaP semiconductors.

Registration

Only persons 18 years of age or older will be permitted to attend Electro/80. Registration at the door will cost \$9; advance registration provides a \$4 discount. Courtesy registration cards are available from some exhibitors, and companies can register their employees at a \$2 fee per person by purchasing and distributing "gold cards" in advance. In addition, members of an Attendance Committee will visit major electronics firms in the northeastern U.S. to provide advance registration cards to engineers, managers, and technicians requesting them. For further information contact the Electro offices at 999 N Sepulveda Blvd, Suite 410, El Segundo, CA 90245 (Tel: 213/772-2965) or at 1387 Washington St, West Newton, MA 02165 (Tel: 617/527-6944). □

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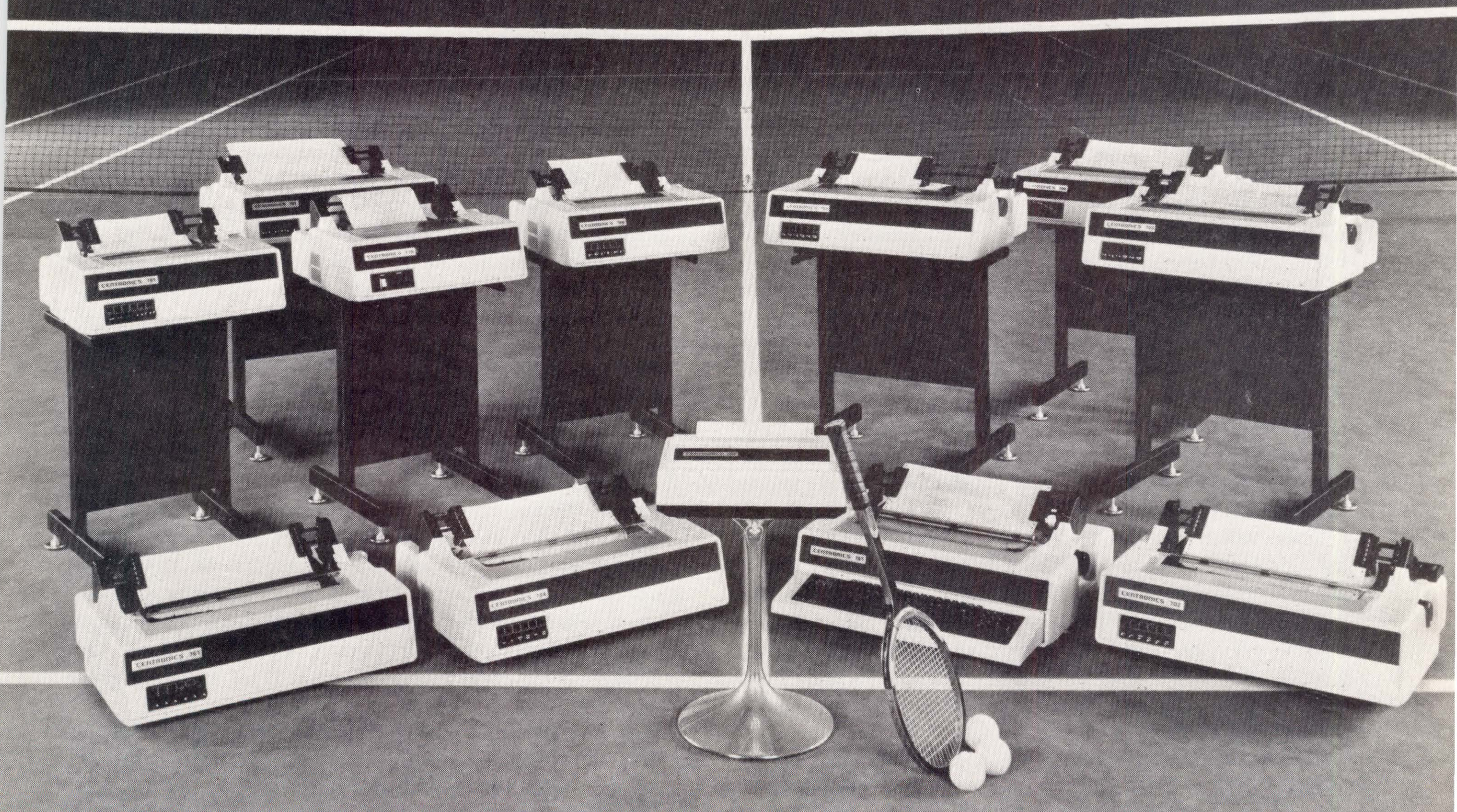

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1980 National Computer Conference

May 19-22
Anaheim Convention Center
and
Disneyland Hotel
Anaheim, California

Herbert B. Safford
Conference Chairman

Dr. Don B. Medley
Program Chairman

AFIPS' annual National Computer Conference returns to Anaheim, California this year after a record breaking 1979 meeting in New York City. Both technical sessions and exhibits for NCC '80 will be located at the Anaheim Convention Center complex; the associated Personal Computing Festival—including both a technical program and exhibits—will be at the nearby Disneyland Hotel conference area.

Details on many areas of the Conference were still not available at press time, but the following information should at least help readers determine what portions of the overall 4-day meeting will be of interest to them. Note that some details are based on preliminary information and very likely will change before the Conference is held.

As in past years, much of the computer industry will be represented—both in the nearly 100 technical sessions and in the displays provided by the more than 400 exhibitor companies (in over 1400 booth spaces). Included are micro, mini, and mainframe computers and architecture; peripherals; software engineering; applications; data base management; data communications; simulation; and image processing, as well as office automation and social dynamics.

There will be three and a half days of technical sessions at the Convention Center: 1:30 to 4:45 pm on Monday and 8 am to 4:45 pm on Tuesday, Wednesday, and Thursday. As in past years, five full-day Professional Development Seminars will be held each day. In addition, however, this year an innovative series of half-day Seminars will be held each morning, supplemented by related technical session presentations in the afternoon.

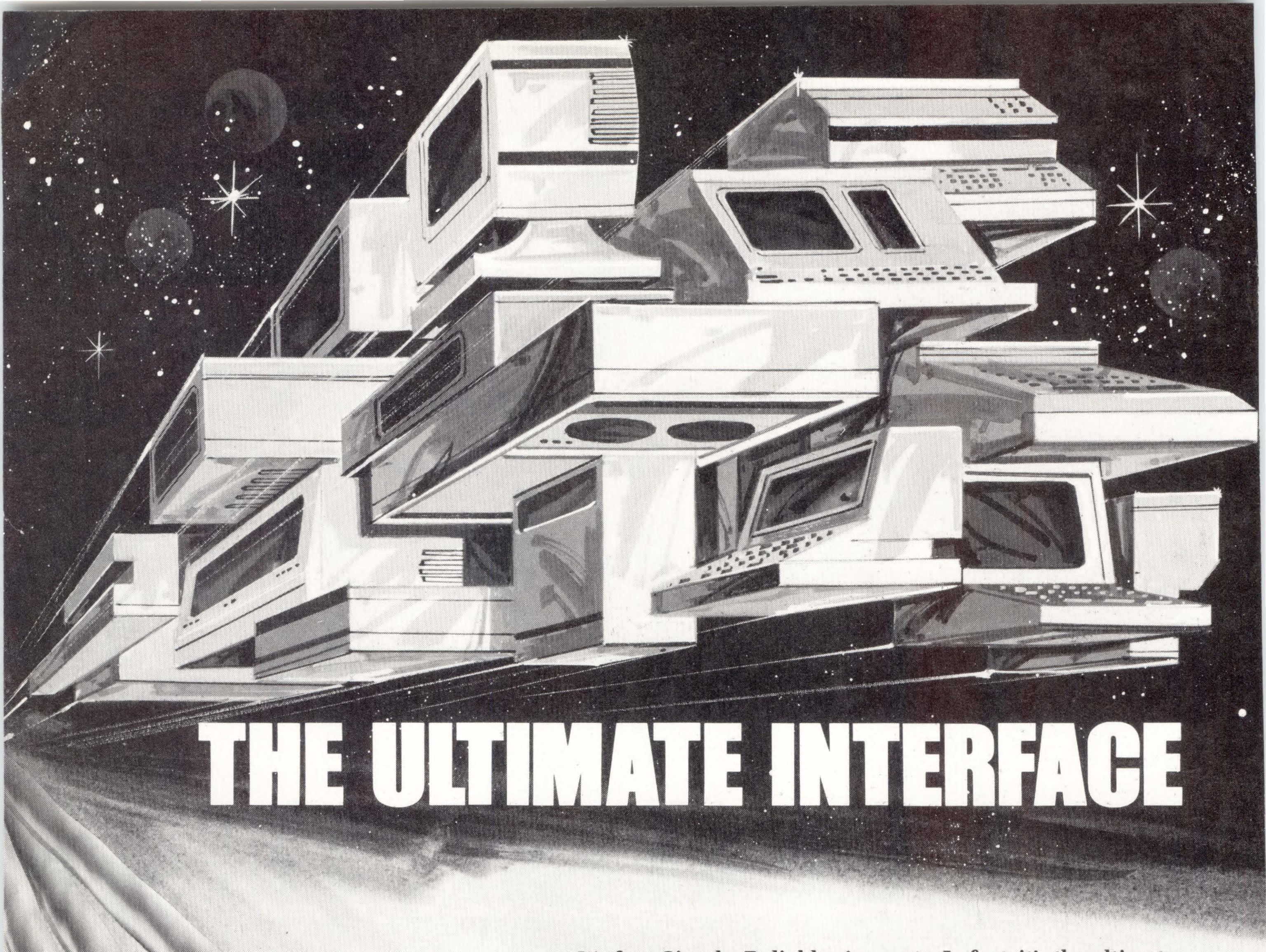
Convention Center exhibit hours will be 11 am to 7 pm on Monday, 10 am to 6 pm on Tuesday and Wednesday, and 10 am to 4 pm on Thursday. Personal Computing Festival exhibit hours will be during the same time periods, but only on Tuesday through Thursday.

NCC '80 general chairman is Herbert B. Safford of GTE Data Services; program chairman is Don Medley of Moorpark College. Personal Computing Festival general chairman is Robert R. White of Informatics, with Lewis A. Whittaker of Innovative Computer Products and Lawrence Press of Small Systems Group as cochairmen.

In a telephone interview, Dr Medley said that the overall approach in choosing the technical sessions was to develop, wherever possible, very practical, user-oriented sessions—sessions that tell the attendees how to make "effective use of those particular tools called computers." For instance, there will be "about five sessions that deal with the use of computers in the entertainment industry—not for entertainment, but for supporting the entertainment industry. That is, how do you use them in producing a play? How do you use them in actually creating animation? How do you use them on a stage to control the lights? It's behind the scenes, using the computer as a tool."

Dr Medley said that there also will be stress on technical information, particularly in the approximately 21 sessions that deal with software engineering. These cover a broad spectrum including reliability, standards, and education. "We think that we have a very strong coverage of the language area. We're going to have an entry on ADA; we're going to have an entry on MUMPS, we're going to have an entry on Pascal, and we'll have one for high level languages for microprocessors. We're pretty well covered in the language area, especially in the needs of the emerging languages."

Additionally, about seven sessions dealing with electronic mail and the automated office will stress technical aspects, such as simulating office automation to determine if a suggested system will work correctly. Company modeling or simulation will also cover other subjects, such as their use in solar energy projects.



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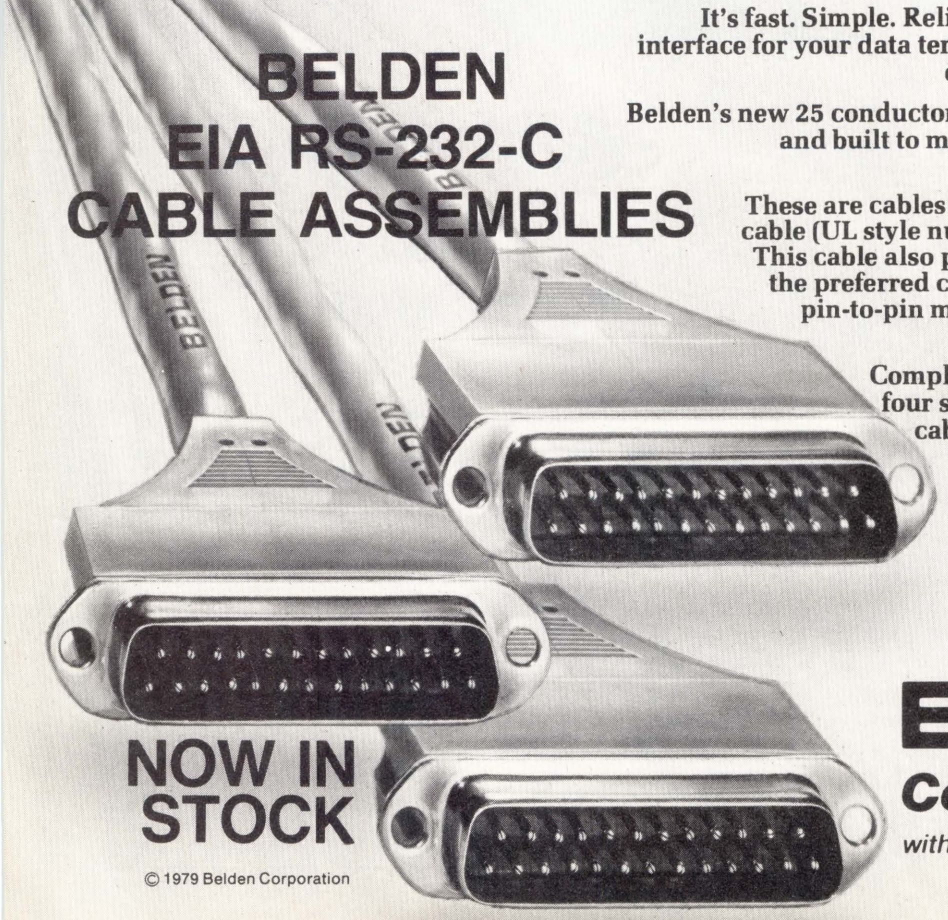
Belden's new 25 conductor molded cable assemblies are designed and built to meet EIA standard RS-232-C and types A through M standard interfaces.

These are cables you can count on. Belden's rugged 8459 cable (UL style number 2576) is used in these assemblies. This cable also passes the FR-1 vertical flame test and is the preferred cable for critical interfaces. And positive pin-to-pin mating using subminiature "D" type plug connectors means no mix-up.

Complete cable assemblies are now in stock in four standard lengths of up to 70′ (21m). Bulk cable is available in put-ups of up to 1000′. Custom designed assemblies are also available on special request. Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, IN 47374; 319-966-6661. Out West contact our Regional Sales Office in Irvine, CA 714-833-7700.



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8-15-9

Although not complete segments, stress has also been placed on the use of computers in medical imaging and medical education. These sessions will be set up such that attendees can register for even one day and still find something of interest to them.

Technical Program

Judging from information that was available at press time, it appears that three out of the eight planned categories of technical sessions will contain most papers of particular interest to the majority of *Computer Design*'s readers. However, some sessions within the other five categories will also very likely be of value to many readers. Since the available information was at best sketchy, NCC '80 attendees should obtain and review copies of the final program as guides before deciding on which sessions to attend. To request these programs in advance of the Conference, contact AFIPS Headquarters, 1815 N Lynn St, Arlington, VA 22209 (Tel: 703/243-4100).

The first category of interest, Computer Architecture, will contain 10 sessions spread through the full three and a half days. On Monday afternoon there will be two sessions, "Data Base Translation or Distributed Data Base Architecture," chaired by Steve Kimbleton of the U.S. Department of Commerce, from 1:30 to 3, and "Survival Systems," by Richard Merwin of IEEETC, Washington, DC, from 3:15 to 4:45. Tuesday will have nearly a full day of sessions in this category: "Network Architecture," by Ira W. Cotton of the U.S. Department of Commerce, from 8 to 9:30 am; "Intelligent Memory" by Charles R. Vick of BMDATC, Huntsville, Ala, and "Supersystems of the 80s, Problems of Designing and Programming," by Steven and Svetlana Kartashev of the University of Nebraska, concurrently from 1:30 to 3 pm; and "Data Base Machine Architecture," by Dave Hsiao of Ohio State University, from 3:15 to 4:45 pm.

Wednesday will have only one computer architecture session, "Issues of Data Base Machine Design," in the 8 to 9:30 am time slot. However, on Thursday there will be three sessions: "Commercial Data Base Processors," by Eugene Leventhal of Intel, from 9:45 to 11:15 am; "Formal Construction Method for Hardware Description Language Derivation," 1:30 to 3 pm; and "Impact of VLSI (I/O Chips)," by Ray Voith of Motorola, 3:15 to 4:45 pm.

Considerable overlap will exist between the Computer Architecture category just described and the 13 periods in the second category of interest—Data Base Management and Communications. This category will begin with a double session from 1:30 to 4:45 on Monday afternoon covering the subject of "Design Practicum," presented by Jeffrey Holder of Case Western University and Donna Shepherd Rund of Pacific Telephone; plus a single session concurrently in the 3:15 to 4:45 period on "Architecture of the Next Generation of Data Base Management Systems," by Mike Hammer of the Massachusetts Institute of Technology, Bill Kent of International Business Machines, and Dennis McLeod.

Tuesday morning's lone session in this category, in a panel format moderated by Bharat Bharagava of the University of Pittsburgh, will run from 8 to 9:30 and will cover "Concurrency, Consistency, and Reliability in Distributed Data Base Management." Afternoon sessions will concentrate on aspects of communications. The 1:30 to 3 slot will be filled by another panel, "Distributed Minicomputer Networks," with participants from Digital Equipment Corp, Hewlett-Packard, Modular Computer, and Aerospace Corp. "Telecommunications from the Terminal User's Viewpoint" will be discussed in the 3:15 to 4:45 period by T. G. Albright of Printer Terminal Comm, David Peters of Racal-Vadic, and M. F. Schumann of Honeywell.

Wednesday sessions will include "Keys to Distributed Processing," from 8 to 9:30 am; "Data Base Technology," by Peter Chen of IBM, from 9:45 to 11:15 am; and "The Many Voices of Data Base Management," by Edward L. Glaser of Ampex, E. F. Codd of IBM, Fred Heath of Herriot-Watt University in Scotland, and Paul Pitt, in the 1:30 to 3 pm period.

On Thursday morning the sessions will cover "A Workable Approach to Implementing a Data Management Plan," by Daniel Appleton and Linda Taylor of System Development Corp, from 8 to 9:30; and "Tightly Coupled Distributed Architecture Design," with panelists from Carnegie Mellon University, Honeywell, and TRW, from 9:45 to 11:15 am. Concurrent afternoon sessions from 3:15 to 4:45 will cover "Practical Natural Language Access to Data Base," and "A Federated Architecture for Decentralized Data Bases," with panelists from TRW, University of Southern California, and Washington University.

Software Engineering Technology, the third category of interest, will contain 20 periods on software and languages, including two double sessions. The one session to be held on Monday, from 1:30 to 3 pm, "ADA—Where it Stands Now," concerns the Department of Defense high order programming language for military computer systems and will be chaired by Hal Hart of TRW. On Tuesday, however, there will be a total of six periods, on Wednesday there will be seven, and on Thursday there will again be six.

Tuesday morning sessions will include "MUMPS—The Multipurpose Data Management Oriented Standard Programming Language," subtitled "The David and Goliath Story in Software Engineering." The session will be conducted by Henry Heffernan of Washington, DC and will be in the 8 to 9:30 time slot. Also beginning at 8, but continuing for a double period through 11:15, will be "Implementing a Software Management Discipline," chaired by Richard H. Thayer of the U.S. Air Force Sacramento Air Logistics Center. Speakers will include Joan P. Bateman of Boeing Computer Services, Tom Gila of Norway, Anthony P. Lee of the Department of Finance, Sacramento, John H. Manley of the The Johns Hopkins University, and Arthur B. Pyster of the University of California. Concurrent with the 9:45 to 11 period will be "Pascal in the Real World," with A. Windsor Brown of General Automation chairing the session.

Afternoon sessions on Tuesday will begin with "High Level Languages for Microprocessors," conducted by John Brackett of Softech Microsystems, San Diego, in the 1:30 to 3:15 period. That will be followed, from 3:15 to 4:45, by "Economics of Software—How Can We Improve It?" presented by Ed Dodson of GRC, Santa Barbara.

There will be three sessions on Wednesday morning, with two of them held at the same time. From 8 to 9:45 will be "Software Reliability—Needs and Responses," by John Bowen and Dean Lindstrom of Hughes Aircraft. In the 9:45

to 11:45 period will be "Current Trends in Software Reliability," chaired by Myron Lipow of TRW and with Irving Doshay of TRW, Kurt F. Fischer of Computer Sciences Corp, Randall Jensen of Hughes Aircraft, and Jack McKissick of General Electric as speakers. Concurrently will be "Software Requirements Engineering—An Interdisciplinary View," chaired by Raymond T. Yeh of The University of Texas, and with four other speakers: Robert Balzer, Harlan Mills, Nick Roussopoulos, and Gerald Weinberg.

Wednesday afternoon will have four sessions, beginning at 1:30 with "Tools for Verification and Validation, A State of the Art Report," conducted by Sarina Saib of GRC, Santa Barbara. Two related sessions, the first starting at 1:30 and the other at 3:15, will cover "Software Requirements Engineering." The first, presented by Alan Davis of GTE, Mack Alfrod of TRW, Carl G. Davis of the U.S. Army, Chuck Elberhart of Teledyne Brown Engineering, Earl Hershey of the University of Washington, Larry Peters of Boeing, Ward Stanke of Martin Marietta, and Dan Teichrow, will be "From the Viewpoint of Tool Developers." Following that will be one from "The Functional User's View," by John Mitchell of Georgia Institute of Technology. Also during the 3:15 to 4:45 period will be "Software Tools/The Program Development Environment," by Leon Stucki of Boeing Computer Services.

A double session on "Software Engineering Technology Transfer," will be held from 8 to 11:15 on Thursday morning. Chaired by Lorraine M. Duvall of IIT Research Institute, these sessions will have six other participants: Victor Basili, Dennis Fife, Frederick Gallegos, Richard Maitlen, Jon Martens, and Michael McGill. Also in the 8 to 9:30 period will be "Software Quality Assurance," conducted by Kurt F. Fischer of Computer Sciences Corp and with Robert Dunn of ITT, William R. Gallant of Sperry, Frank S. Ingrassia of TRW, B. Max Knight of IBM, and Marvin Weisbein of RCA as speakers.

There will be three software sessions on Thursday afternoon to close the Conference. "Quantitative Measures of the Quality of Programs and Systems" will be in the 1:30 to 3 period and "Software Standards" will be from 3:15 to 4:45. Also in the latter time period will be a session called "Software Testing."

Professional Development Seminars

Seminars, both full- and half-day versions, will be held on May 20, 21, and 22. Representative of the full-day format on Tuesday will be "Performance Measurement In Systems and Programming," presented by John Toellner of Spectrum International; "Structuring the Data Base System Project," by Leo Cohen of Performance Development Co; and "Software Design Techniques," by Peter Freeman, consultant.

Two of the Seminars on Wednesday will be "Update on Small Computer Systems," offered by Raymond Wenig of International Management Services; and "An Overview of Distributed Processing," by Ira W. Cotton, U.S. Department of Commerce. Thursday Seminars will include "Data Base Machines Are Coming," by David K. Hsiao of Ohio State University; "Future Computing," by Portia Isaacson of Electronic Data Systems; and "Software Engineering that Works," by Gopal Kapur of Kapur Associates.

The half-day Seminars, which relate to regular Conference technical sessions that will take place on the same day, include two of particular interest on Tuesday: "A Pragmatic View of Distributed Processing Systems," presented by Kenneth A. Thurber, consultant; and "Quality Control for Software," by Ned Chapin of Information Sciences. Wednesday morning Seminars will be "Software Tools," by Donald J. Reifer of Software Management Consulting; and "Designing and Programming Parallel Systems with Dynamic Architecture," by Steven and Svetlana Karatashev. Another interesting seminar, "Design by Objectives," will be presented by Tom Gill, a consultant from Norway, on Thrusday morning.

Registration

At-conference registration fees will be $75 for the full three and a half days of program, exhibits, and Personal Computing Festival, including a copy of the *Conference Proceedings*; $10 for all of the above, but without the *Proceedings*, for students; $25 for exhibits only Monday through Thursday; $25 for any one day of program and exhibits; and $10 for any one day of exhibits only. Preregistration fee for the full conference is only $60. There will be an additional registration fee of $50 for each full-day and $25 for each half-day Professional Development Seminar. Registration fees for the Personal Computing Festival alone will be $15 for program, exhibits, and *Personal Computing Proceedings*; $9 for only program and exhibits from Tuesday through Thursday; and $5 for any one day of program and exhibits. □

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CIRCLE 71 ON INQUIRY CARD

HYBRID TOOL FOR UNIVERSAL MICROPROCESSOR DEVELOPMENT

A single-board universal interface attached to a personal computer can act as an intelligent ROM emulator for software upgrading of an existing product, or it can function with CPU personality cards as a development system for a new product design

David McCracken Thera Institute, Aptos, California

Microprocessor development tools presently available suffer substantial drawbacks. One-processor, dedicated, single-board products allow inexpensive development of a simple product but offer limited program diagnostic capabilities because of their restricted input/output facility. Also, they provide no means of benchmarking different processors in a given application. More flexible and powerful emulators can be used to benchmark different processors but are correspondingly more expensive. Both approaches restrict engineers to use of only those microprocessors for which development systems are manufactured.

A hybrid approach interfaces the microprocessor under development to a low cost, interactive, personal computer to afford a complete development environment with all the features of an emulator at the approximate cost of a dedicated single-board system. Since all of the hardware and most of the software are microprocessor independent, the hybrid may be adapted for use with virtually any microprocessor. It is flexible enough to be used with both 8- and 16-bit microprocessors.

Integration of a computer and a microprocessor requires a means of controlling the microprocessor without interfering with its application operating system. In addition, the implementation must use hardware and software that are easily adapted to any microprocessor, including, hopefully, future products. The described integrated approach developed hardware and software simultaneously for the first half of the design cycle, enabling tradoffs that were crucial in making the interface transparent to the microprocessor. Once the transparency problem was solved, the remaining goal of hardware and software adaptability was achievable.

Communication Channel

Under control of the host computer, a Superboard II, the interface serves as a sophisticated, writable program store for the microprocessor. The interface also provides a bidirectional communications channel between the microprocessor, which is completely unaware of its presence, and the host computer. In many cases, the interface can be attached to the microprocessor by means of a simple ribbon cable connection to a read only memory (ROM) socket. Alternately, a central processing unit (CPU) personality card, or satellite, including data memory if needed, plugs into the interface to provide a development environment for new applications (Fig 1).

The host computer writes application programs into shared memory, called program memory, for subsequent execution by the microprocessor. It also sets the microprocessor's particular state by initializing registers and flags to selected values. Finally, the microprocessor reports its state at various times, such as at breakpoints, and supplies information for video displays generated by the host computer.

Two communication channels are offered by the interface: a program channel to access shared program memory and handshake channel to pass control information to the microprocessor and return status information to the host computer via shared handshake memory. Under host computer control, the interface multiplexes 16 data lines, 10 address lines, and 8 control lines, allowing either the host computer or the microprocessor to access the shared program and handshake memory banks (Fig 2).

An operating system is necessary for the microprocessor to communicate with the interface; therefore, it must be programmed to interact in a development environment. This is a common requirement in microprocessor development tools, many of which dedicate certain addresses to a development communication channel and almost invariably require use of restart routines during development, making it difficult to test new application software fully until the hardware is built and the memory is programmed. Of course, the application restart routine cannot coexist with the development restart routine because both must reside at the same address. The entire address mapping is similarly restricted until the final hardware has been constructed. By then, it is difficult to modify microprocessor system software because the development system cannot coexist with the application system.

These problems are solved by overlapping development (handshake) memory and application (program) memory within the microprocessor address space. Now, the microprocessor can have two restart routines: an application routine in the program bank and a development routine at the same address in the handshake memory. Program and handshake memory distinctions remain transparent to the microprocessor, which need

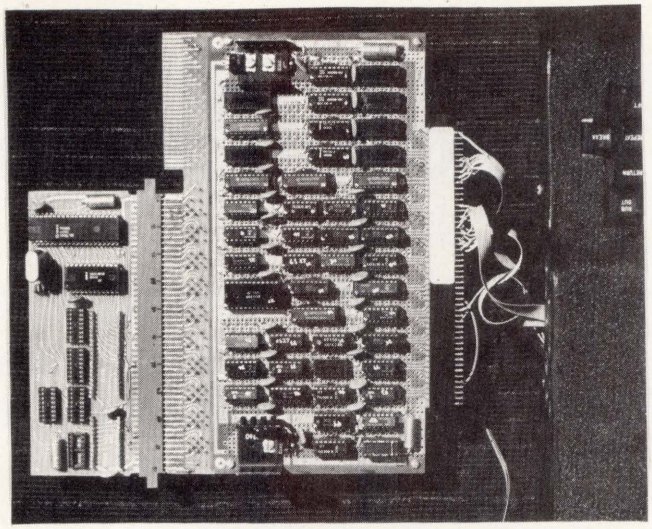

Fig 1 Universal interface. Simple 8035 satellite plugs into edge connector at lower left. Ribbon cable at right attaches to host computer. Edge connector at upper left allows expansion of multiplexed program RAM. Satellite may be replaced by ribbon cable connection to application system ROM socket

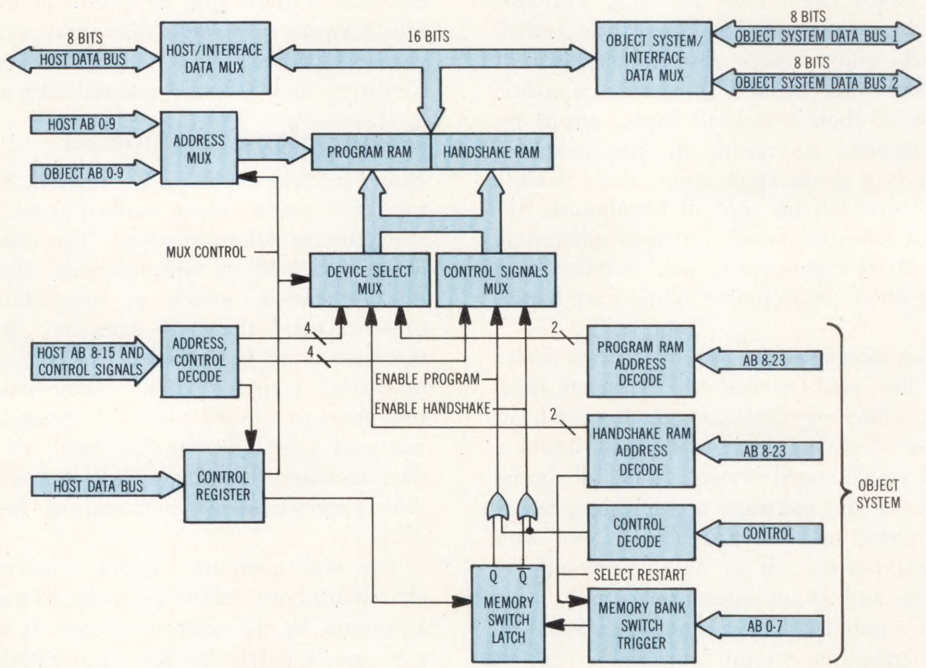

Fig 2 Universal interface block diagram. Multiplexers give either object microprocessor or host computer access to shared memory. Control register determines which of these gains memory access. Memory bank switch latch is key to microprocessor transparent operating system

not be programmed to select an appropriate restart routine. In practice, the two restart routines must be invoked in strict alternating sequence, beginning with the development restart routine that prepares the microprocessor to run a program—either the application restart routine or the continuation of some other routine previously interrupted, perhaps by a breakpoint.

The host computer initially sets a memory bank switch (Fig 2), that directs all microprocessor instruction fetches to handshake memory. When the microprocessor reset pin is released by the host computer, it is the development routine generated by the host computer in handshake memory that executes on the microprocessor. The last instruction of the development restart routine resides at a specific address (F7), which is decoded by hardware when fetched by the microprocessor and is used to trigger the memory bank switch. Subsequent instruction fetches now reference program memory, and the memory bank switch can be restored only by the host computer. As shown in Fig 3, memory bank switching occurs only on the trailing edge of the read signal. This avoids a race condition between the switch and the microprocessor memory access.

A mechanism for transferring breakpoint information from the microprocessor to the host computer completes the transparent communication requirements. Breakpoint—the interruption of program execution at an arbitrary, preselected location—ranks among the most valuable program development aids. Necessary data include extensive microprocessor status information used by the host to generate a video display, along with information required to resume microprocessor program execution. Breakpoints can be implemented in hardware or software. A hardware solution compares the current instruction address with the breakpoint address and switches microprocessor instruction fetches to the handshake memory, when these match, to execute a breakpoint routine. This approach allows breakpoints to be placed anywhere in the application program. A software solution, in which the breakpoint entry routine replaces a block of instructions beginning at the breakpoint address, prevents use of breakpoints within about 15 locations of the end of actual memory space. Despite this restriction, a software implementation was adopted to dispense with about ten extra integrated circuits (ICs) required for a hardware solution.

The host computer loads the breakpoint routine at the specified address in program memory. When the microprocessor executes the breakpoint routine, it records microprocessor status information in handshake memory. Interface hardware decodes control signals and directs all microprocessor write accesses to handshake memory, so that neither breakpoint nor unplanned program writes can modify program memory.

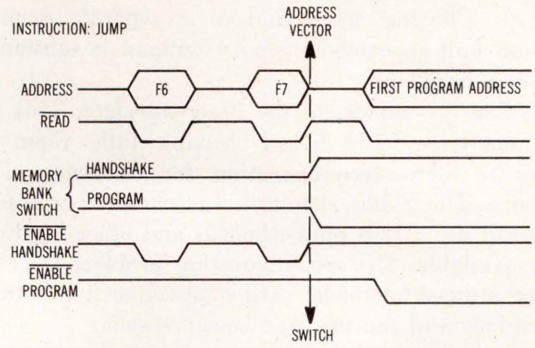

Fig 3 Memory bank switching. Microprocessor access to last restart instruction (F7, program starting address vector) initiates switching from handshake memory to program memory. Switching occurs on trailing edge of READ to avoid race condition

Interface Implementation

The interface can be adapted to virtually any microprocessor having external program memory. Individual microprocessor timing and control requirements must be considered during implementation. This is particularly true for 16-bit microprocessors such as the Z8000 with 24 address lines, using A0 to distinguish between high and low order bytes, or the 8086 with 20 address lines, using A0 to select low order bytes and an additional signal, BHE, to select high order bytes.[1,2]

Still, microprocessor similarities outweigh their differences, and a nearly universal communication protocol requires the interface to make only minor changes to the microprocessor control signals. For example, the protocol assumes that read and write are low true signals, invariably generated when the address and data are valid. If a microprocessor lacks the read signal, as with the 6502, read is generated automatically. If the microprocessor system uses high true read and write signals as on the S-100 bus, these are inverted by the interface.

OR and NAND gates allow further manipulation of control signals such as MEMRQ in the Z80, and the 8035 PSEN program store enable used to read program memory.[3,4] Microprocessor system address lines in Fig 2 are decoded by two different hardware subsystems during device selection to allow mapping of program memory anywhere in the microprocessor address space.

The host computer loads the high order address into program memory address decode circuitry registers under operator direction. These are compared with microprocessor address lines to select the appropriate memory bank. Meanwhile, handshake memory decode circuitry selects handshake memory whenever the high order address is 000XXX or FFFXXX, chosen to match the microprocessor restart location. Again, these addresses may overlap because microprocessor control signals combine with memory bank switch status to arbitrate the actual memory selection. Both memory banks are 16 bits wide; the program bank is 1k bytes by 16 bits in size, and the handshake bank is 256 bytes by 16 bits. The program bank can be treated as 2k by 8-bit memory for 8-bit microprocessors.

The host, assumed to be an 8-bit computer, addresses all memory and control registers as sequential memory locations within a 4k-byte block. Pertinent control signals and all multiplexed lines to the memory array are brought to the edge connector in the upper left corner of Fig 1, allowing connection of a separate memory expansion unit to extend memory without a substantial increase in hardware.

Forty-five ICs implement the basic interface. This fills out a standard S-100 board, leaving little room for switches to allow reconfiguration for different microprocessors. The S-100 standard was chosen because its widespread use makes motherboards and other hardware readily available. The reconfiguration problem is solved by using a quasi-intelligent card edge connection between the interface and the microprocessor system.

Interface address, data, and control signals are brought to an edge connector at the lower left corner in Fig 1. Here, a microprocessor satellite attaches directly to that edge connector. Alternately, a ribbon cable would be installed between the edge connector and a microprocessor application system ROM socket, allowing the interface to function as a ROM emulator. The plug-in board (or ribbon cable) is microprocessor specific and completes all connections necessary for reconfiguration. Because the simple 8035 satellite attaches directly to the edge connector in Fig 1, this typical configuration requires only one additional cable connection to the host computer.

Hardware and Software Flexibility

The 6502 CPU was chosen as host because of its widespread use in inexpensive personal computers and its associated ease of programming. The Superboard II was selected for its low price and easy expansion to accommodate the interface. This single-board computer includes a built-in, programmable, full-size keyboard and a 25 by 25 element television display interface for operator interaction, as well as a cassette tape interface for storage of both the development operating system and the application software. The 8035 object microprocessor implementation demonstrates the flexibility of the design because, since the 8035 is a single-chip microcomputer with its own memory, input/output (I/O), and unusual protocol for external circuit communication, the task of fitting it to a universal standard appears difficult. Other existing implementations support the 6502 and 8086 microprocessors.

Flexibility was the primary software development goal, with efficiency secondary. One of the most powerful aspects of the device is provision of a development environment for virtually any microprocessor. To achieve this, adaptation to different microprocessors must be as easy in software as in hardware. Flexibility has been achieved in that 65% of the software is totally object microprocessor transparent. The remaining 35% was kept microprocessor specific, because of gross inefficiencies required to generalize the routines; however, once the software functions were well defined by the first implementation, the problem of generating equivalent software for different object microprocessors became less difficult.

Rigid adherence to rules of structuring allows software flexibility. There are no program jumps, even when a subroutine call requires additional instructions. Subroutines are used in preference to straight-line programming wherever there is no associated memory penalty. All parameters are passed between subroutines through page zero, making the index registers, accumulator, and stack fully available for most flexible use within the subroutines.[5] These characteristics simplify coding long sequences of subroutine calls and allow future software to utilize all existing subroutines.

All tables, which are largely object microprocessor dependent, reside in a dedicated memory block isolated from the software routines. Table expansion and alteration therefore occur without program relocation. Table manipulation was identified as the area in which to concentrate programming effort because it provides both flexibility and efficiency.

Design Complications

Two unusual aspects of the interface complicate the software design more than a cursory inspection would indicate. One problem develops because shared memory is accessed by different addressing schemes in the host computer and the object microprocessor. This results from the operator's need to reference program memory from the object microprocessor viewpoint, while the host computer employs a different addressing convention.

Memory addressing is further complicated because the interface itself can be mapped into any 4k segment within host computer address space. Furthermore, the operator can change the location of program memory, as accessed by the microprocessor, to allow development of application software anywhere in microprocessor address space. While handshake memory addresses change when the interface is remapped, they do not change when program memory is remapped; in fact, handshake memory addressing must never change in the object microprocessor system, because handshake memory provides the development restart.

Dual memory addressing constraints define a scheme of virtual addresses and physical addresses, either of which can be translated to the other by an algorithm. The operator employs only the virtual addresses used by the object microprocessor. If the operator relocates program memory within microprocessor address space, the virtual mapping changes while handshake memory remains fixed at the physical restart location. The host computer uses physical addressing to access both the program and the handshake memory banks. It converts the operator specified virtual addresses to physical addresses by subtracting the lowest program memory bank virtual location, adding the interface lowest physical address, and checking to guarantee that the result falls within program memory physical space. If the result is not a program memory physical address, it must reference an object microprocessor memory location not shared by the host computer. Since the host cannot manipulate microprocessor memory that is not shared, it passes the virtual address to the microprocessor, along with a communication program, via handshake memory.

For example, suppose the interface is mapped to host physical addresses 9000 through 93FF. If program memory begins at virtual address 1000 and an address reference designates virtual address 1200, the virtual address is converted to a physical address by subtracting the lowest program memory virtual address and adding the interface lowest address: 1200 − 1000 + 9000 = 9200. In contrast, virtual address 1600 corresponds to host physical address 1600 − 1000 + 9000 = 9600, an unimplemented program memory bank address; therefore, an address reference of 1600 must designate the object microprocessor address of a memory location not shared by the host.

The second unusual problem that complicated software development is that handshake routines must be written simultaneously in both host computer assembly language and object microprocessor assembly language, because of tradeoffs required to achieve program efficiency. This problem was most evident when writing the 8035 restore status and continue routine, which directs the host computer to assemble a program in handshake memory for the object microprocessor to execute. Unless the operator designates status changes, the program in 8035 assembly language restores the 8035 to its exact condition at the location where a breakpoint was encountered and then jumps to the required application program address.

The major tradeoff consideration is whether the object microprocessor should pick up its status information through a table access loop or through a straight-line routine. A table access loop, the obvious choice in most situations, requires less memory. In this case, however, a high efficiency table access loop cannot access memory outside the 8035 internal random access memory (RAM) because the additional status words are directed to unique destinations such as the 8035 timer, program status word (PSW), and I/O port.[6]

Another consideration is the 8035's unusual addressing technique to retrieve data from its program memory, which it generally considers to be only a source of instructions. The MOVPA, @A instruction concatenates the accumulator content with the current program page to address program memory data; the data are retrieved to the accumulator where they overwrite the original address.[7] This architecture precludes forming efficient loops to pick up status information. A standard alternative would be straight-line programming, where each word is loaded directly into the desired location. For example, MOV R0,#FF in only two bytes restores register 0 to the designated value.

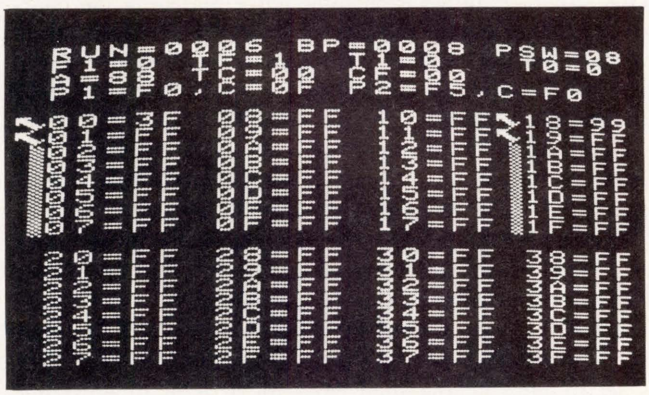

Fig 4 Breakpoint status display. Standard television set displays extensive 8035 status information including full 64 bytes of internal RAM

Thought must be given to how the host 6502 computer would set up such a program for the object 8035 to execute. Because the 6502 is unaware of 8035 instructions, the program must be moved as a data string into the proper location, using a table and loop for efficiency. If a straight-line approach were used on the 8035, the 6502 would have to determine where to insert status information into the 8035 program it handles as an arbitrary data string. This is possible, but very inefficient. Instead, the host computer loads a complete, straight-line, 8035 restore program, which specifies data sources through a table that is modified by the host computer using other, unrelated subroutines.

Table Structure

Development operating systems for different microprocessors require equivalent software routines such as the program/display routine, which allows the operator to examine and modify object programs, and additional routines used to insert breakpoints, run programs, continue execution, single step through a program, display breakpoint status, modify status at breakpoints, disassemble program code, and transfer application software to or from tape. There are 52 such subroutines in the entire program.

To reduce future programming effort, adaptability of the routines for use with any object microprocessor was an important goal. This was achieved by writing microprocessor independent routines that are driven by microprocessor dependent tables. Extension to additional microprocessors by changing predefined table entries is much easier than changing software routines, especially when each routine interacts with many others. This is reflected by the final result, in which 65% of the executable code and only 4% of the table code are microprocessor independent.

Status Display

A breakpoint display routine does not appear to be easily generalized. Every microprocessor has a unique internal architecture. The 8035 is a good example, because as a single-chip computer it maintains considerably more internal information than other microprocessors, as shown in Fig 4. The 8035 breakpoint display routine must show a standard, internal status form, filling in the blanks with information passed by the object microprocessor via handshake memory when the breakpoint is encountered. The difficulty is that while the blank form can originate in ROM, the fill-in information cannot.

One solution is to devise a table containing both the American Standard Code for Information Interchange (ASCII) characters to be displayed and the addresses of the sources of data to fill in the blanks. This table also contains control characters that use character codes not defined in the limited ASCII character set. Table extracts in Fig 5 show the four ASCII table entries representing PSW. The next characters displayed would be the breakpoint value of the program status word. The display routine knows that codes directing it to a data location will follow any "=" character. A packed control word as the next entry designates the number of display digits and indicates whether the source is the host computer zero page or the handshake memory. The following entry is the low byte address.

The display routine fetches the data, converts to ASCII format, and displays the required digits. Because the number of digits is specified, the same routine can handle 16-bit addresses, 8-bit data, and 1-bit flags. The multiple space character, followed by the number of spaces required, saves table space when long, empty fields are required in the display. Use of the end of transmission (EOT) character makes table driven software independent of table entry length.

An addressing limitation of the host 6502 computer is most noticeable in this situation because the remappable interface must be addressed indirectly. The 6502 offers two forms of indirect addressing: indexed indirect with the X register as a pre-index, and indirect indexed with the Y register as a post-index.[8] The post-indexed form addresses breakpoint information in handshake memory, and should also be used to show status information if a full screen is to be displayed.

Competition between these applications for the Y register would create substantial problems, but this was avoided by displaying only eight video lines comprising 256 entries in the video memory. This allows use of an absolute address indexed by X for the video, reserving indirect addressing indexed by Y for exclusive use in handshake memory access. Eight lines suffice to display the internal state of any general purpose microprocessor. While the 8035 status display uses a full screen, most of this information is an orderly internal RAM array loaded into video memory by a relatively simple program loop.

Command Parsing

The next table handling example demonstrates the use of table lookup to generalize a sequential keystroke parsing routine employed by the breakpoint processor change status utility. With this debugging tool the operator can change any object microprocessor internal status information before resuming program execution. The procedure is to examine each keyboard entry until a specified register or other microprocessor resource has been entered correctly and identified, then to use subsequent keys as new data to be stored in the register. The program will actually modify a table in handshake memory. Host computer page zero may also change, in which case another routine uses the page zero information to modify a table in handshake memory because the object microprocessor cannot access host computer page zero. Then, as previously described, the restore status and continue routine sets up the object microprocessor to retrieve table data for restoring status before continuing program execution.

The unique microprocessor architecture and nomenclature rule out keyboard parsing with prior knowledge of the actual keys to be entered or the number of entries required to identify a resource, particularly when abbreviations are permitted to reduce operator effort and program length. Handshake memory or page zero table destination corresponding to the resource is also unknown. All of this information must be stored in a microprocessor specific table.

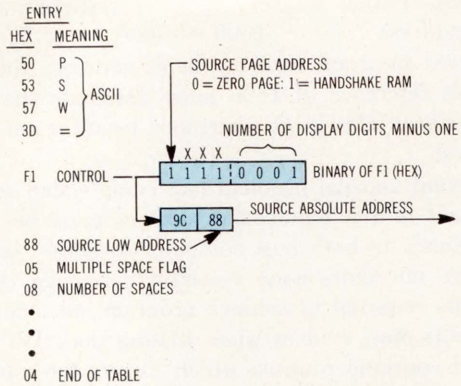

Fig 5 Breakpoint display table entry format. General purpose routine driven by table entries displays status of virtually any microprocessor. ASCII "=" preceeds reference to data outside table. Subsequent entries serve to locate, adjust, and format data

For program efficiency, keyboard parsing is synchronous with operator input so that data need not be stored and then deciphered. Fig 6(a) shows the table divided into numbered key fields for the first key entered, the second key, and so on. These fields are further divided into subfields, each of which contains all possible characters that might follow a particular character in a valid input string.

Each table entry comprises three bytes. First is an ASCII character to be compared with the input keystroke. This is followed by two control bytes. Generally, the first control byte directs the parsing routine to the starting address of the next sequential key subfield, linking the entries for all keys that could follow to produce valid input. The second control byte supplies the subfield length used to terminate searching for a key match. If no match is found, the parsing routine waits for another key entry and searches the subfield again with the new character. This structure allows each table entry matching the character entered by the operator to direct the parsing routine to the next set of table entries, so that much of the parsing operation is controlled by the table rather than the parsing routine.

Because the routine cannot know the required number of entries in advance, the table must also terminate parsing. The second control byte, which is the third byte of each complete table entry, normally supplies the number of entries in the following subfield. Only a few bits of this word are needed as there are never many characters that could follow a particular character in a valid input string. By convention, bit 7 of the second control byte is set to indicate the final entry in a valid input string [Fig 6(b)]. In the same way, bit 6 is used as a special control flag, and bit 0 distinguishes between host page zero locations and handshake memory locations.

Disassembly

Disassembly is achieved by searching a table to find a match for each instruction operation code, in sequence, skipping over the operands. A match directs display of a character string corresponding to the instruction mnemonic. Both the instruction operation code and the character string mnemonic are supplied by a single table. Each entry consists of a hexadecimal operation code and its associated ASCII mnemonic.

Microprocessor instruction mnemonics may vary in length. Mnemonics for the 8035 range in fact from two to nine characters (Fig 7); therefore, a control word in each table entry supplies the length of each mnemonic. Fig 8 shows the table structure, beginning with the control word that addresses the operation code. Since this requires no more than four bits for mnemonics up to 16 characters long, the unused high order bits afford additional table control. Bit 7 is set to signal a decrease in operation code length, relative to the previous entry, while bit 6 is set to indicate an increase in mnemonic length. Organizing table entries in decreasing order by operation code length and in increasing order by mnemonic length permits the search routine to keep track of these parameters with very little overhead.

Many character strings are used in more than one mnemonic, such as MOV, which appears in 17 different 8035 instructions.[9] A multicharacter table entry is addressed by a special character, with bit 7 set, and the remaining bits supplying an offset to the address of the character string. Use of a multicharacter table conserves memory by handling frequently needed strings as an extension of the single character processing.

This disassembly table structure appears efficient but overlooks an important characteristic of all microprocessor instruction sets—the property of operation code regularity. The table structure treats every operation code as an isolated entity when, in reality, instruction sets tend to use a sequence of consecutive operation codes to perform a sequence of related operations. For example, the 8035 uses F8 through FF, A8 through AF, 28 through 2F, and nine similar operation code sequences for related operations that manipulate registers R0 through R7, with the low order three bits of the operation code designating the particular register.[10] To save memory, operation codes for this class of instructions, branch instructions, and I/O instructions are presorted by an 8035-specific routine before a general table search is attempted. While the operation code presort requires more than 20% of the microprocessor specific programming, the resulting economies are worth the investment.

Summary

Built-in flexibility makes the universal interface a valuable engineering tool at every stage of product development. Typically, the design of a microprocessor based product begins with a problem description. This should lead to a list of microprocessor requirements such as word length, controller or data manipulator orientation, single chip or bus orientation, and so on. These requirements, in turn, form the basis for a list of potential microprocessors. At this point, the interface can be used with the desired satellites, which are inexpensive because they are small printed circuits containing the central processor and data memory, to benchmark the microprocessor in operations characteristic of the application.

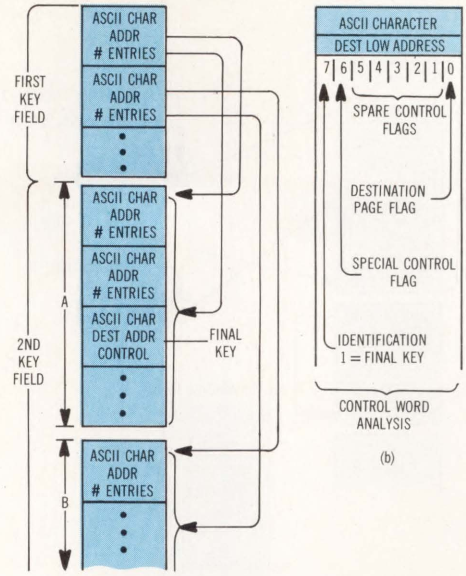

Fig 6 Breakpoint status change table entry format. General purpose routine driven by this table parses operator input to identify both microprocessor register and new data to be placed in register. Entry triplet (a) consists of ASCII character and pointer to either next key subfield or register destination. Final key triplet (b) terminates entry and supplies destination page address

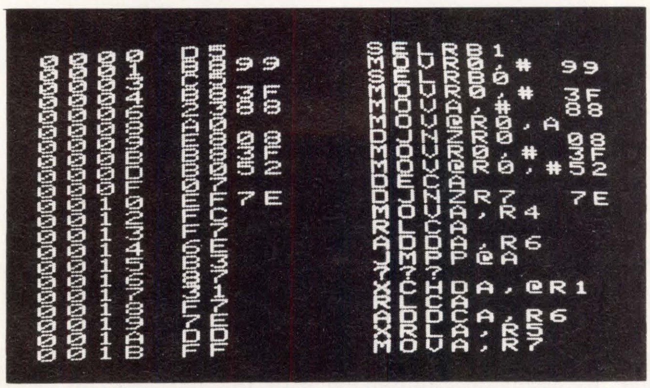

Fig 7 Program disassembly display segment. General purpose routine generates two-to-nine character mnemonic plus operands from machine instructions in program memory. Typical 8035 instructions are shown, but virtually any microprocessor instruction set is handled. Disassembly is a powerful aid to locating both software errors and program entry errors

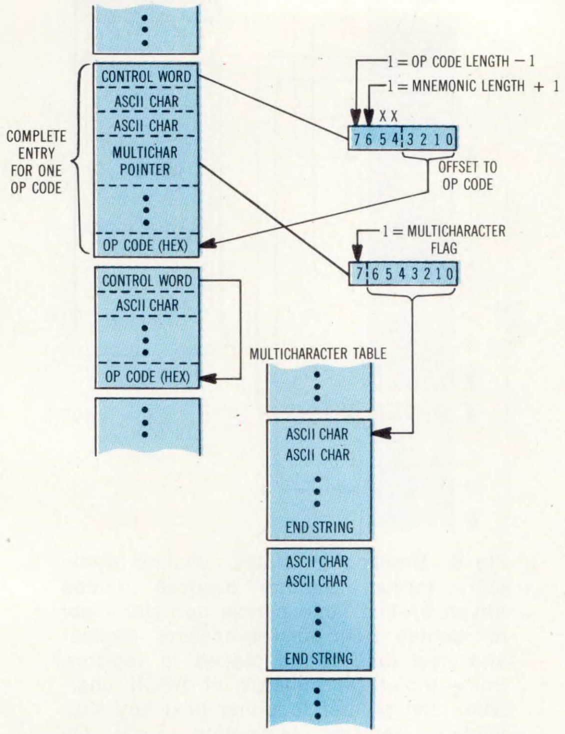

Fig 8 Operation code table entry format. Multiple byte entries headed by control words specify offset to start of hexadecimal op code. Control word may show increment of mnemonic length or decrement of op code length. Character entries are either single ASCII codes or pointers into multiple character table

Once a microprocessor has been selected, application hardware and software specification begins. As the hardware prototype is being designed and built, software can be developed using the universal interface. Then, once the application hardware prototype is ready, the microprocessor satellite is no longer needed and a ribbon cable attached to the application ROM sockets allows the interface to function as a ROM emulator, retaining all development capabilities.

At this point problems can be solved quickly through software modification; engineers can be assisted by the development system while checking the actual application hardware. Even after production begins, the universal interface helps remedy problems discovered in the field and extends the useful life of the product through software upgrading. In addition, using one development system at all stages of the design cycle reduces design time by assuring familiarity with the development environment.

Availability of development systems is limited to those microprocessors that are widely enough used to warrant the high cost of emulation (or a dedicated board), or those that are supported by development systems from their manufacturer, which tend to be expensive. Simplicity of the satellite and ease of rewriting software for different microprocessors give designers an inexpensive way to produce a development system for any microprocessor, regardless of obscurity or infancy, using the universal interface.

Although the universal interface is in every way superior to a dedicated development system, it does have one deficiency not found in emulators: it cannot be used to develop products based on a single-chip computer that lacks a companion, external ROM CPU. The 8035 is this companion to the 8048.

The universal program development interface affords a microprocessor development tool with all the power of an emulator, and some additional advantages, for a small fraction of the cost. Hardware and software work together to create a flexible and efficient development environment that is easily modified for use with virtually any microprocessor.

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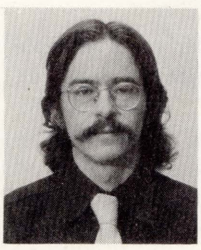

David McCracken works as the principal engineer at Thera Institute, designing automated laboratory equipment for in-house biochemical research. His work ranges from extensive multiprocessor controlled test environments to miniature computerized field data acquisition systems. Before that, he was an industrial control systems consultant. He studied civil engineering at the University of California, Berkeley.

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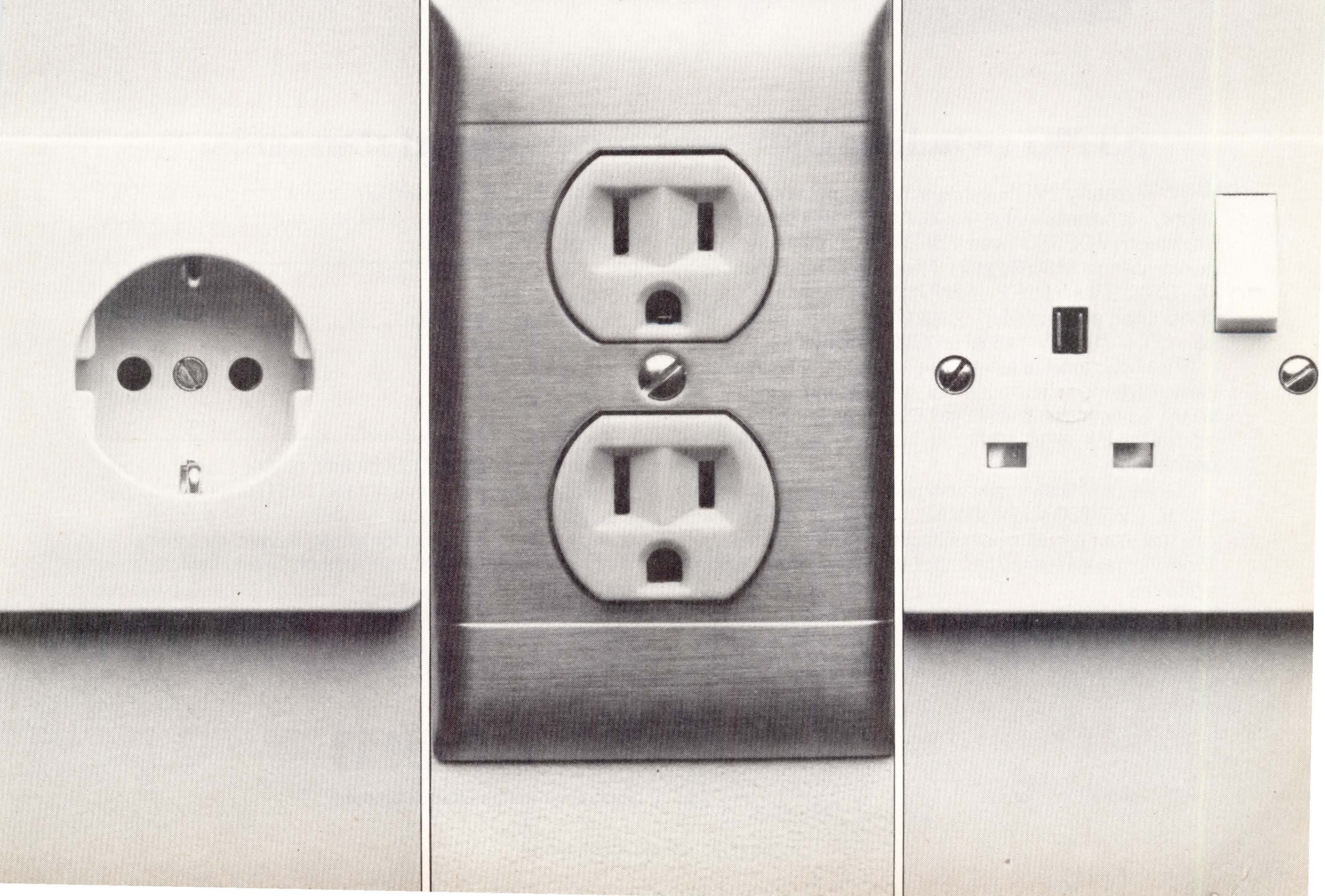

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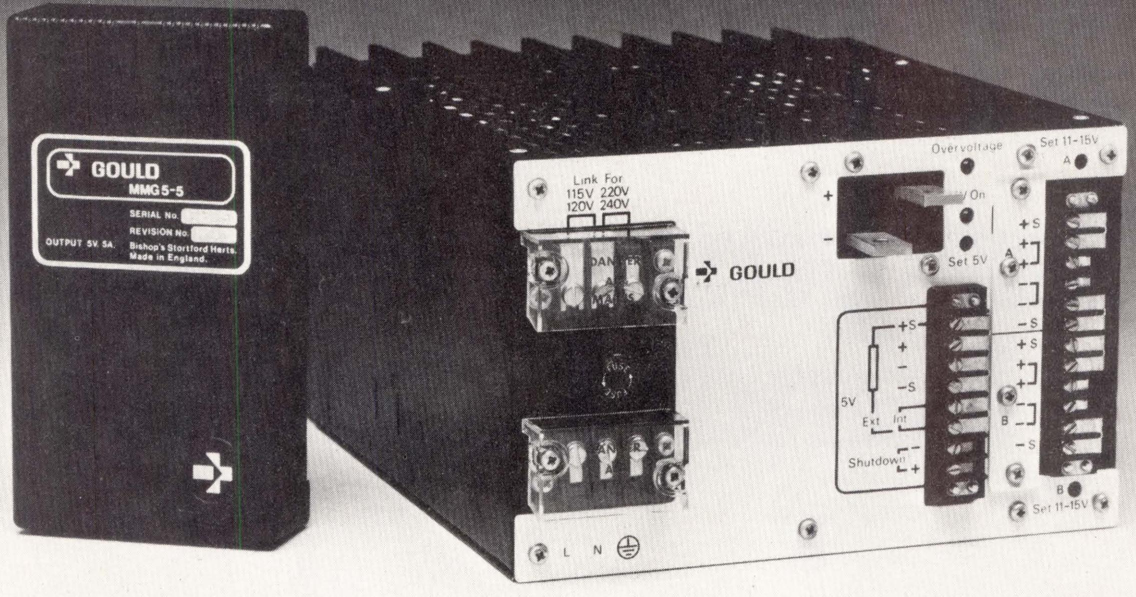

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15	X	X	X		X			X
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COMPONENT-BY-COMPONENT TESTING OF DIGITAL CIRCUIT BOARDS

Signature analysis techniques speed testing of complex digital circuit boards, and use of an interpretive processor simplifies test program debugging

Douglas W. Raymond Plantronics/Zehntel, Incorporated, Walnut Creek, California

Developing viable procedures for production testing of digital circuit board assemblies has become almost as complex as the task of designing the circuits themselves. With the increasing growth in complexity of electronic systems in the 1960s, it became apparent that there were limitations in the traditional "functional" test procedures. A component by component test technique known as in-circuit testing was investigated as an alternative approach and was soon demonstrated to be capable of highly cost-effective fault isolation on the production line. Now, after a decade of evolution, in-circuit testing has come of age. The latest systems can test every component on a circuit board, from simple resistors to complex microprocessors, within seconds. These systems also incorporate software that enables test engineers to systematically build and debug in-circuit test programs in a fraction of the formerly required time.

Comparison of Functional and In-Circuit Testing

A functional test system tests an entire circuit assembly *as a whole* with respect to the functions it is designed to perform. The circuits on the board are powered up and input signals applied, matching as closely as possible the inputs that would be encountered in actual operation. Outputs are measured and performance is compared with design specifications. Values of the various parameters at internal circuit nodes are not measured during a functional test. Connections between the test apparatus and the circuit under test are generally via a cardedge connector. A different program controls the test routine for each different circuit configuration.

In-circuit testing, on the other hand, electrically isolates each *component* on a board, tests it for its own characteristics, and ignores its function in the overall circuit. All circuit board components are tested one by one. Connections between the in-circuit test system and the board are via a vacuum-actuated, multiple-pin, "bed of nails" fixture, with each distinct circuit board type having its own unique fixture.

However, once a component test program has been developed for a given component, it may be called upon any time in the future regardless of where it appears or how it is employed on a particular circuit board. With such a library of test segments, a test engineer can generate an entire in-circuit test program from a list of components and their locations, by appropriately sequencing component test segments already stored in memory. When a component fails an in-circuit test, a printed diagnostic message explains the location of the component and the nature of the failure.

In essence, in-circuit testing determines whether or not a circuit is assembled properly, while functional testing determines whether or not it works. Nevertheless, a consideration of the limitations of functional testing will make it apparent why many test engineers are turning to in-circuit testing as a prior step to, or even as a replacement for, functional testing on the production line.

Limitations of Functional Testing

Functional tests test circuits. If a circuit fails a functional test, the next step is to locate the fault within the circuit assembly. This can be a monumental task because many different circuit board faults can create the same functional test failure symptom. In the case of a functional test system, locating even a simple short on a circuit board containing hundreds of components may require sophisticated software modeling and minutes, or even hours, of guided probing by a skilled technician. These costly diagnostic procedures generally locate only one faulty component at a time. Multiple component failures frequently require several test/diagnose/repair iterations.

Sometimes two or more out-of-tolerance components produce effects that offset one another, so that they defy detection during a functional test but cause failure later in actual operation. A short or a component failure occurring while an entire board is powered up for a functional test can damage other components as well.

Finally, functional tests are themselves difficult to program, particularly in the case of digital circuits. Ideally all possible input and output states for the entire circuit board should be exercised. Programming a functional test for a digital board frequently requires detailed knowledge of the internal operation of the board being tested. Once programmed, a functional test is "dedicated" to a particular circuit board type. A board having a different set of overall functions will require a different functional test program.

In-Circuit Testing Advantages

In-circuit tests test components, not circuits. By electrically isolating each device and each point-to-point circuit board trace or continuity, an in-circuit test system can rapidly test a circuit board for shorts and opens, and inspect every component for proper connection and performance.

In practice, shorts and opens are located and repaired before proceeding with component tests, thereby avoiding contamination of test results or even damage to costly components at later stages of the test routine. Typically, a 200-component board can be tested in under 100 s, with the important feature that multiple component failures do not slow this process. Since each test segment is associated with only one component, no guided probing is necessary to locate a defect and expensive manual diagnosis is not required. In fact, since appropriate diagnostics are automatically printed for each component failure that occurs during an in-circuit test, the operator simply attaches the diagnostic printout to the board, and this serves as an instruction for the repair operator.

Functional and In-Circuit Testing Compared

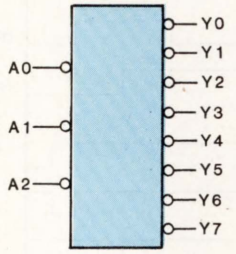
Functional Testing	In-Circuit Testing
Tests functioning of assembly taken as a whole.	Tests individual components.
Isolation of component faults requires complex software simulation and/or manual probing. Costly and time-consuming.	Readily isolates all component faults.
Multiple component failures require repeated iterations to diagnose.	Multiple component failures diagnosed in a single test sequence.
Defective components may not be exercised.	All components are exercised.
Powering up a defective board can damage components.	Non-destructive. Shorts and opens are located and repaired early in the test routine. Discrete components are tested without powering up the entire board.
Complex programming task. Programming requires detailed knowledge of circuits contained on the board assembly.	Simple programming task. Programming requires knowledge only of components and their locations.
Can use same cardedge connector in testing different circuit board types.	Unique "bed of nails" fixture required for each different circuit board type.
Different test program required for each different circuit.	Different test segment for each different component. Programs for different circuits easily generated from library of component test segments.

Test system software can be programmed to tabulate and process component failure data. If the data reveal a fault such as solder splash or missing component at the same location on a number of boards, the problem can be corrected before large numbers of faulty boards are manufactured. Automatic recording of failure data greatly simplifies the preparation of reports on component reliability and production yields.

Programming of an in-circuit test is relatively simple, because each program segment deals with only one component. In-circuit testing is highly cost-effective, because each component is tested for its own characteristics without regard to its function in a circuit. The user can build up a software library of component test segments that may be applied to the same components on any circuit board.

While it is true that in-circuit testing requires fabrication of a unique "bed of nails" fixture to establish an electrical interface between the test system and each particular circuit board type to be tested, the cost of fixturing, typically $2500 for a 600-node board, is almost always offset by lower programming and operating costs, and by higher throughput as compared with functional testing. An engineer might spend up to two months programming a functional test, but an in-circuit test for the same board can be programmed by a technician in one or two weeks.

It is generally agreed that currently available in-circuit test equipment can isolate as many as 90% of all circuit board faults. This is often a sufficiently high fault-detection level to justify omission of functional testing altogether, for it may be more cost effective to pass the boards on to a system-level test and discard any that fail there. However, test engineers sometimes require a higher confidence level, or are reluctant to assume that a circuit will work if its components work. In such cases, functional testing is still employed. A properly designed functional test can raise the fault-detection level to 98%, but only if an in-circuit test has been performed first. The table summarizes the advantages and disadvantages of both forms of testing.



		TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6	TEST 7	TEST 8
INPUTS	A0	0	0	0	0	1	1	1	1
	A1	0	0	1	1	0	0	1	1
	A2	0	1	0	1	0	1	0	1
OUTPUTS	Y0	0	1	1	1	1	1	1	1
	Y1	1	0	1	1	1	1	1	1
	Y2	1	1	0	1	1	1	1	1
	Y3	1	1	1	0	1	1	1	1
	Y4	1	1	1	1	0	1	1	1
	Y5	1	1	1	1	1	0	1	1
	Y6	1	1	1	1	1	1	0	1
	Y7	1	1	1	1	1	1	1	0

Fig 1 Classical approach to testing 3- to 8-line encoder. Truth table values are applied to inputs and corresponding output values measured. Testing all possible states requires eight separate tests. Writing code to generate distinct input states takes time and resulting test programs are unwieldy, especially for testing complex devices that incorporate sequential logic

Digital In-Circuit Testing

In the last few years, advances in integrated circuit (IC) technology have dramatically increased the percentage of complex digital devices mounted, and needing to be tested, on circuit boards. Around 1974, the first procedures were developed to apply in-circuit testing to digital components.

Early Techniques

At first, digital components were in-circuit tested by creating known logic states at the device inputs and comparing the resultant output states with expected truth table values (Fig 1). The stimuli were of short duration, typically less than 1 ms, in order to minimize heating and possible damage to the device; they were of low impedance, about 5 Ω, to override any inputs created by other circuit components wired to the same nodes.

Unfortunately, because truth table testing required preparation of a distinct set of programming instructions to test each state, programming proved to be time-consuming and costly, particularly for complex digital components. To keep programming within reasonable bounds, compromises in test coverage were common, and the test engineer frequently would have to rely on a statically-based confidence level. Moreover, the one-state-at-a-time test technique proved cumbersome in the testing of memories and other complex sequential circuits. It soon became clear that unless a technique could be developed to effectively and quickly test complex, large scale integrated devices without requiring costly software, the utility of in-circuit testing would be severely limited.

Signature Analysis

The problem was solved by introducing digital signature analysis, a technique used for decades in performing data error analysis on computer storage devices, and more recently in field service tests for digital systems. Fig 2 illustrates this technique as applied to the device shown in Fig 1. The same logic states are generated at the inputs, and the same truth table values are expected at the outputs. However, in this case the inputs are a set of harmonically-related signals called coherent, time-dependent bit streams. All are square waves alternating between logic states 0 and 1.

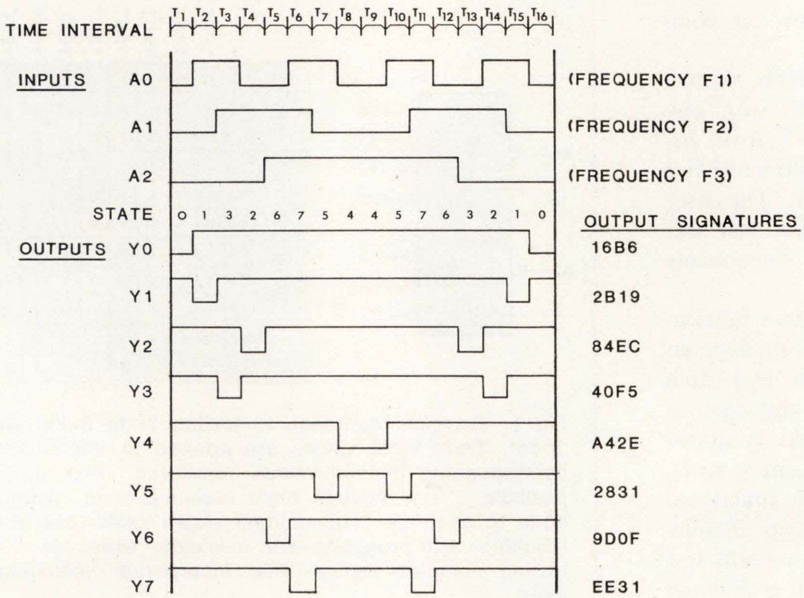


Fig 2 Signature analysis approach. Coherent stream of time-varying inputs is used, with input A1 at half frequency of input A0 and input A2 at half frequency of input A1. All possible input states are exercised within one full period of input A2. Each output is sampled over same time period and fed into signature-generating register which produces unique 4-digit hexadecimal signature from each output. This is compared with signature obtained from corresponding pin on known good device. One test investigates all possible states

Input A1 is a square wave at half the frequency of input A0, and, similarly, input A2 is at half the frequency of input A1. A master clock maintains the proper phase relationships among the inputs, and creates a pattern stream that exercises every combinatorial state, provided the stimuli are applied for at least one period of the lowest-frequency input.

Each output, sampled over exactly the same time period, is fed into a signature-generating register that produces a 4-digit hexadecimal number, or signature. This signature is compared to that of a similar device known to be free of defects, stored in memory. If the two 4-digit numbers agree, the component passes inspection. If not, a diagnostic message is printed identifying the component as defective. One simple set of instructions programs the entire test.

The signature analysis technique eliminates the need to analyze the expected output of the device. It is only necessary to compare the signature of the device with the expected signature stored in memory, and the expected signature is determined empirically. Thus, for example, there is no need for the test programmer to be familiar with the program contained in a programmable read only memory (P/ROM) under test. He simply stores in memory the signature from a properly functioning P/ROM and uses this as a standard for testing other P/ROMs of the same type that have been programmed in the same manner. If there is an engineering change at a later date in the P/ROM program, it is a simple matter to determine the new signature.

Currently available digital in-circuit testing equipment provides a series of parallel, coherent input streams related by the same power-of-two formula: F_1 is twice F_2, F_2 is twice F_3, etc. With F_1 typically set at 500 kHz, the device in the example in Fig 2 can be tested in just eight μs. In-circuit test equipment also provides stimuli for initializing a device and for maintaining constant logic 1s or 0s at selected inputs where required for testing certain functions.

The in-circuit test programmer is not entirely relieved from the responsibility of knowing the internal states of a complex component. For devices employing sequential logic, such as microprocessors and memories, the programmer does have to take timing into account, because the same pins may be used for input and output, or for address and data. Nevertheless, the ease with which program segments can be written, and, once written, reused for testing the same components on different circuit board types, makes in-circuit testing highly viable for even the most complex large scale integration (LSI) devices.

Programming an In-Circuit Digital Test

Documenting the Test Fixture

The test fixture is the interface between the in-circuit test system and the circuit board under test (Fig 3).

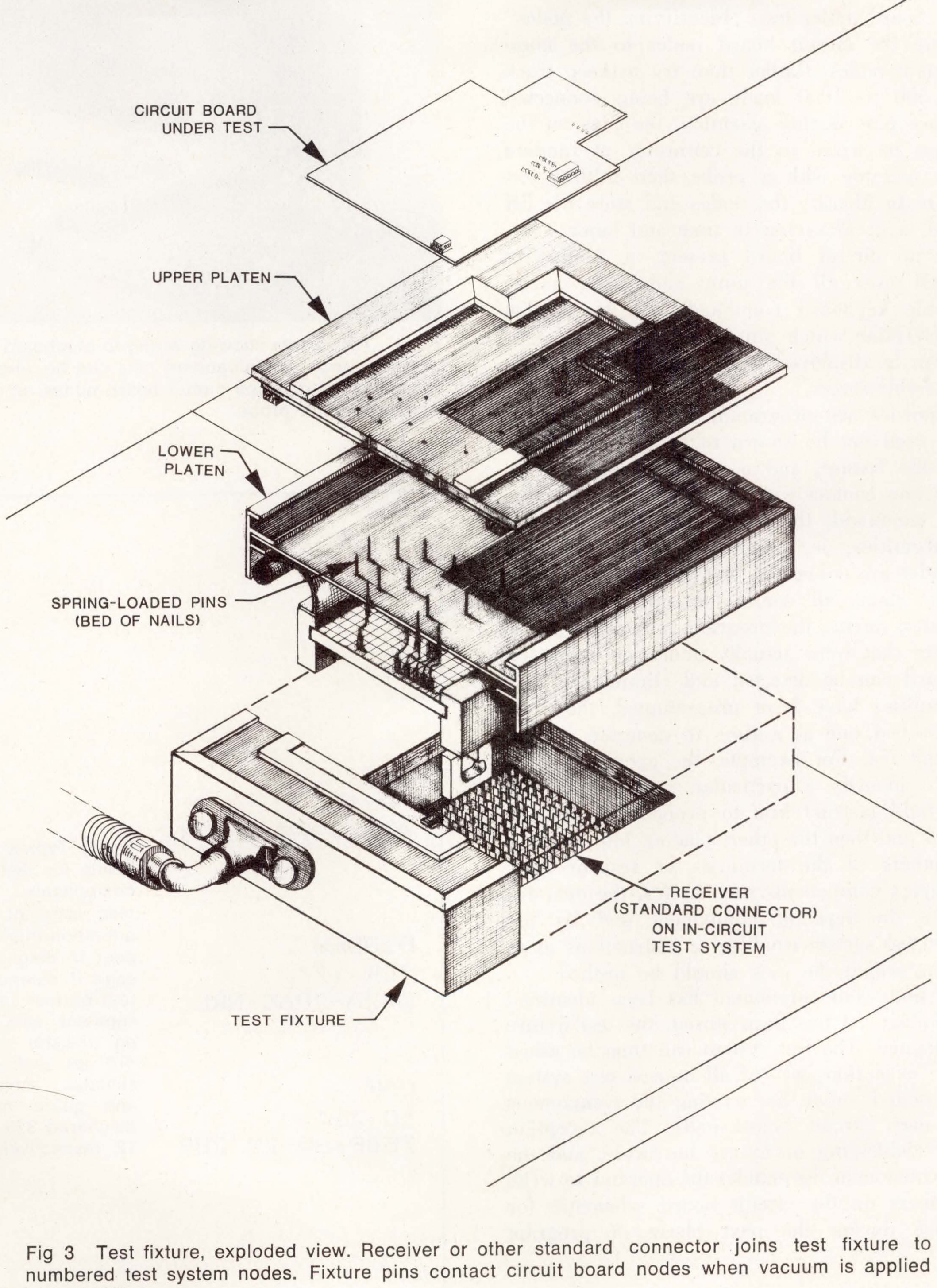


Fig 3 Test fixture, exploded view. Receiver or other standard connector joins test fixture to numbered test system nodes. Fixture pins contact circuit board nodes when vacuum is applied to test fixture

The first phase of programming an in-circuit test is to document the test fixture, ie, identify the nodes and generate a component list.

The bottom of the test fixture connects to the test system nodes via a standard connector. Leads within the test fixture connect the test system nodes to the fixture pins, which in turn are used to contact the nodes on the circuit board under test. "Identifying the nodes" means mapping the circuit board nodes to the numbered test system nodes. Rather than try to keep track of which of 600 to 1000 leads are being connected to which fixture pins during assembly, the pins on the test fixture can be wired to the connector at random (Fig 4.) An operator with a probe then utilizes test system software to identify the nodes and store the list of components, a great saving in time and labor.

First, with no circuit board present, a conductive plate is placed over all the pins, and interconnects them. A simple keyboard command instructs system software to determine which pins are unconnected. This information can be displayed later as an aid in rectifying fixture assembly errors.

Next, continuities are programmed. A model circuit board, which need not be known to be free of defects, is placed on the fixture, and a vacuum is applied to force the pins into contact with the circuit board nodes. On keyboard command, the test system identifies and stores all continuities; ie, determines which numbered test system nodes are connected to which via the circuit board. At this stage, all continuities are assumed to be desired. Later, during the program generation phase, any continuities that were actually undesired shorts on the model board can be detected and eliminated.

Once continuities have been programmed, the components are probed one at a time to generate a complete component list. For example, the operator would type "R13" to identify a particular resistor, and the test system would instruct him to probe first one end of resistor R13 and then the other, placing into memory the node numbers of the terminals of resistor R13. For more complex components such as ICs, the operator would indicate the type of component and its pin count, and the test system would give instructions as to the sequence in which the pins should be probed.

Once every node and component has been identified and the component list has been stored, the test fixture is fully documented. The test system can then be asked to display an "exception list" of all unused test system nodes, and a node-by-node list naming the components connected to each circuit board node. The exception list allows for debugging of fixture hardware, and the node-by-node component list enables the operator to write the node numbers on the circuit board schematic for ready reference during the next phase of program development.

Program Generation

The information that was stored during the fixture documentation phase is now used to generate a list of components and their locations, to serve as input to the program generator portion of system software. For analog devices, the program generator traces out

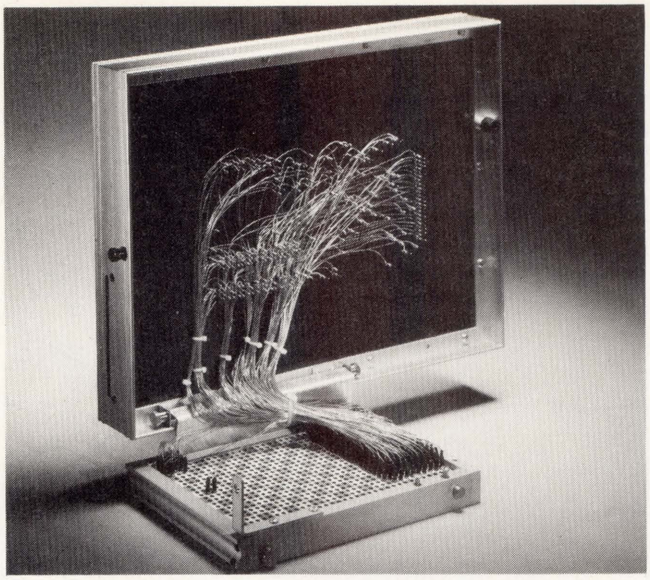


Fig 4 Test fixture showing wiring to plugboard. Connections between probe and plugboard pins can be wired at random. System software maps circuit board nodes as operator contacts them with probe

```
RES
"R 13"
470K,375-922/12

DIODES
"CR 17"
542A-286C NRL

CAP
"C 26"
750P,85-23/289
```

Fig 5 Typical user segments for testing board components. In each test segment, item in quotation marks will appear in diagnostic message if component fails test. Bottom line of each segment specifies test, eg, resistor test is for 470 kΩ resistor whose stimulus, measurement, and guard nodes are numbered 375, 922, and 12, respectively

```
"T5 74LS138"
41,F1       'A0
42,F2       'A1
104,F3      'A2
CRC 16B6   M43    'Y0
CRC 2B19   M77    'Y1
CRC 84EC   M52    'Y2
CRC 40F5   M117   'Y3
CRC A42E   M137   'Y4
CRC 2831   M48    'Y5
CRC 9D0F   M56    'Y6
CRC EE31   M107   'Y7
```

Fig 6 Testing for 3- to 8-line decoder of Fig 1. Only nodes where input frequencies are to be applied (41, 42, and 104), and expected signature at each output node (eg, 16B6 expected as signature of output Y0, to be measured at node 43), need be specified. For simplicity, decoder in this example is considered permanently enabled

the paths that connect to each component, and produces a heuristic design that will isolate or "guard" each component from all others during testing. The validity of this design is determined later, during program debugging. The program generator also structures the test program itself, using built-in component test segments. For more complex analog devices, test "templates" stored in memory are used with a classical macro expansion technique to produce the test for each device. For digital devices, a template library also exists for generating the coherent input stimuli used in signature analysis. The programmer can create his own templates to test devices for which no standard template already exists.

Any programmable machine must be equipped with a suitable language that provides the user with an efficient means of controlling operations the machine is capable of performing. Computers require languages specific to computing; testing machines require languages specific to the operations involved in testing. Coded in a language specific to one particular in-circuit test system, sample test segments for a resistor, a diode, and a capacitor are shown in Fig 5. The items in quotation marks are the diagnostic/repair messages printed if the component fails the test. In each case the following line specifies values for the test parameters.

A test segment for testing the 3- to 8-line decoder of Fig 1 is shown in Fig 6. Note that the entire test segment for this 8-output device is coded in only 12 lines. Even more dramatic is the brevity of the code (shown in Fig 7) for testing a 6100 microprocessor. Just 15 lines are sufficient to test the entire timing and state control logic of this device.

```
"IC E124 61S00"
'TEST MICROPROCESSOR TIMING OUTPUTS
530,F1 'OSC
475,F6 'RUN/HLT
708,F9 'RESET
537,F12'WAIT
658,F3 'SCOPE REF E175 PIN 5
CLOCK 8 '2 US/STATE
CRC BB48 M472 FROM F12 TO F14 'XTA
CRC 5618 M552 'XTB
CRC 531E M541 'XTC
CRC 7180 M344 'RUN
CRC 5E7A M543 'LXMAR
CRC 70D5 M464 'IFETCH
CRC 66EB M465 'MEMSEL
```

Fig 7 Complex LSI device test. Entire program for testing timing and state control logic of 6100 microprocessor fits easily on CRT screen

Test system software, with the help of the programmer, builds up the test routine for an entire circuit board following the flow chart shown in Fig 8. Gross defects (shorts and opens), the most common circuit board faults, are identified and repaired first. Any failures here could mean either contamination of later tests or damage to components when power is applied to them individually. Debugging, normally the most time-consuming portion of program generation, can be greatly simplified by means of interactive programming capabilities and an interpretive processor.

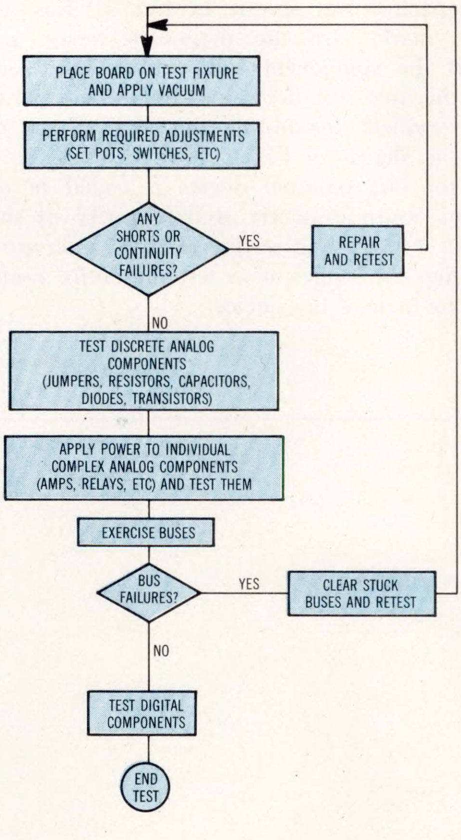


Fig 8 In-circuit testing flow chart. More common defects are checked out first. Test ends if shorts or stuck buses are encountered, since these may contaminate later portions of test

Interpretive Processor Optimizes Program Debugging

Because an in-circuit test program comprises many discrete component test segments, an interpretive processor is the ideal debugging tool. An individual test segment, eg, for testing a microprocessor, can be repeatedly modified by the programmer and exercised by the interpretive processor without the necessity of compilation every time.

The interpretive processor is still used when performing actual production line tests, even though exercising a program via an interpretive processor is slower than exercising the same program after compilation. Unlike classical electronic data processing, in which throughput is governed by the speed of the central processing unit, in-circuit test throughput is governed more by hardware considerations such as setting relays, waiting for capacitors to discharge, manually changing circuit boards, and applying vacuum to the test fixture for each circuit board under test. Thus, speed of execution, one of the main advantages of compilation, proves to be no advantage at all for in-circuit testing, while the interpretive processor's advantage of convenient debugging proves to be paramount.

A recently-designed in-circuit test system incorporates an interactive programming capability called DEVELOP mode. With the test system in this mode, the operator can call up a particular test segment, causing it to be displayed on the left side of the CRT for instantaneous editing. Pauses inserted in the test permit the operator to read displayed information before allowing the test to proceed. This information includes measurement data, eg, resistance, capacitance, or digital signature, for the device under test, and the number of the node at which the data are being measured. These values are displayed in the "data window" in the upper right corner of the screen. (Fig 9).

For analog devices, a "linearity index" is displayed as well, even though not specifically called for in the program. To determine the linearity index for a component, the test system divides the specified input in half, applies this reduced input to the device, measures the resulting output, divides the new output by the old output, and multiplies by two. A device producing a linear response has a linearity index of 1.0. A linearity index differing significantly from 1.0 indicates either a nonlinear device or a linear device that has been improperly guarded. In the latter case, the means used to guard the device can be modified until a linearity index of 1.0 is achieved.

In the system being described, the letters CRC, for cyclic redundancy check, are utilized in specifying the signature analysis test of a digital device. Alternatively, the programmer may use the COUNT instruction, which produces a count of the number of positive-going transitions on the output node of the device, or the HIGH instruction, which produces a count of the number of transitions of master clock pulses over a given measurement interval when the output is at a logic one. COUNT is selected when a device cannot be initialized and the beginning state is unknown. In such a case, the CRC signature would vary from test to test, but over a given

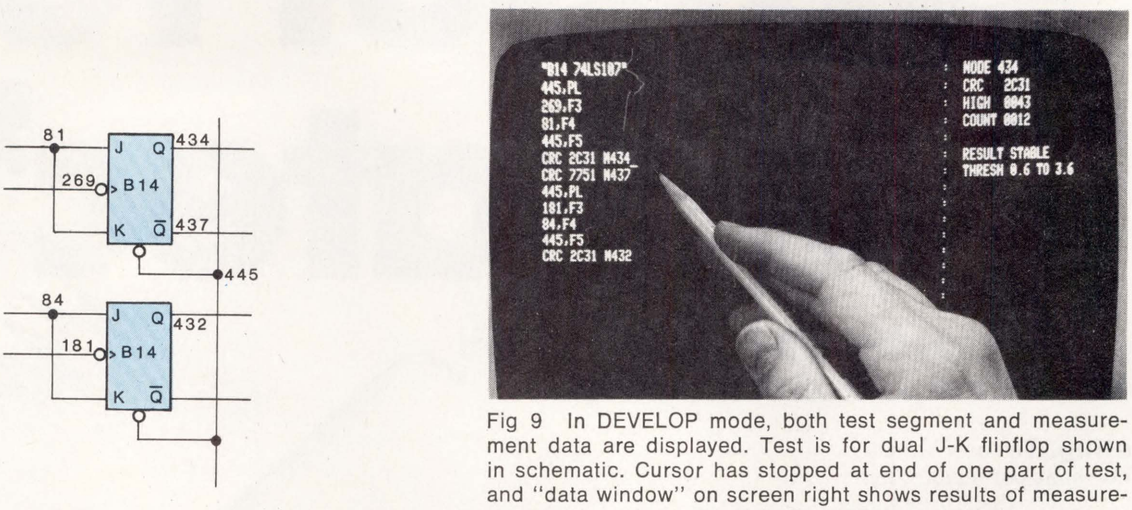


Fig 9 In DEVELOP mode, both test segment and measurement data are displayed. Test is for dual J-K flipflop shown in schematic. Cursor has stopped at end of one part of test, and "data window" on screen right shows results of measurements taken at node 434. Parameters useful for program development are displayed in window even if not specified in program. For clarity, pin numbers have been omitted in schematic; only node numbers are indicated

measurement interval the number of positive-going transitions would always be the same. HIGH is useful for testing 1-shots, since it can measure the duration of a logic high pulse at the output.

When in DEVELOP mode, all three signatures, CRC, COUNT, and HIGH, appear in the upper right corner data window, even if only one is called for in the program, further facilitating debugging. Additional useful feedback is generated automatically regardless of user code, and includes an indication of whether an output pin is permanently high or low, and a diagnostic that tells if certain input stimuli do not affect the output when they should. Either situation would indicate a malfunctioning device or a test segment that needs revision.

Once a test segment is debugged so that the desired data appear in the display window, the edited test is replaced in user memory. During program debugging, possible defects in the model board itself become apparent. A programmer quickly learns which kinds of out-of-tolerance measurements are due to errors in the test routine and which stem from faulty components on the model board. Once a component test segment produces the correct data in the display window, finding incorrect data during the same test on the next board would generally indicate that the second board is defective. However, it could also mean faults in both the model board and the test. Here, too, the programmer quickly learns how to perform the appropriate troubleshooting in order to be sure that the test program itself is valid.

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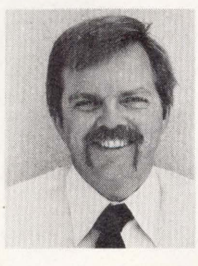

Douglas W. Raymond is currently a project manager at Plantronics/Zehntel, where he has been involved in hardware and software development of the company's line of in-circuit test equipment. He was manager of the group that developed the Troubleshooter 800, an in-circuit test system incorporating signature analysis for testing complex digital components. He holds BScME and MScME degrees from the University of California at Berkeley.

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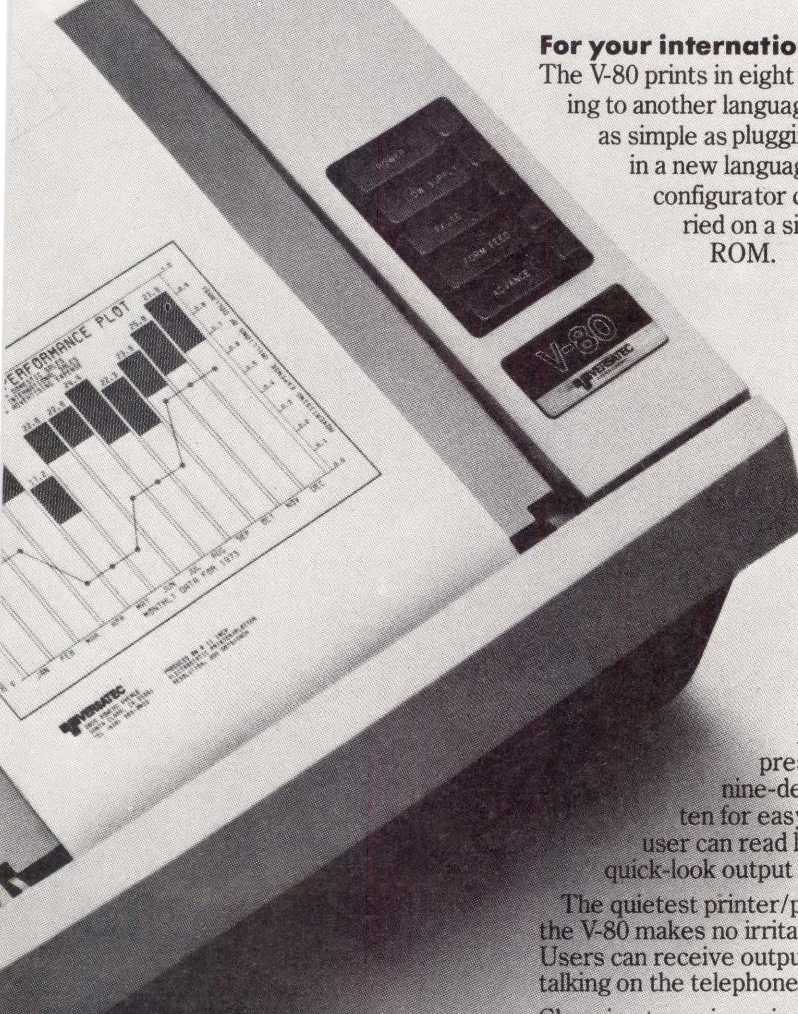

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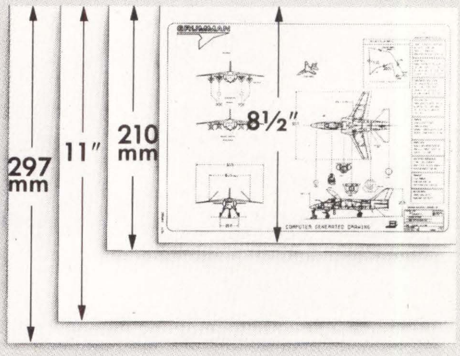

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FIELD PROGRAMMABLE LOGIC REPLACES HARDWIRED CIRCUITS WITH MICROCODE

Field programmable logic can perform keyboard scanning, debouncing, and encoding functions in a typical application with substantial savings in time, components, and cost

Stephen J. Durham Signetics, Incorporated, Sunnyvale, California

The recent surge in design activity involving microprocessors and microprogramming techniques reflects the growing trend toward replacement of hardwired logic and the associated separate circuit elements with microcode. This usually results in additional system flexibility at lower cost. One way to achieve this is with the field programmable logic approach, a technique that provides a dense array of logic gates and flipflops. Many connections or logic choices among these functions are bridged by fusible nichrome links, which can be programmed in the field using one of several widely available programming devices.

Fusible links form an array of crosspoint connections (Fig 1). To produce a desired logic function, the crosspoints are selectively opened by passing a programming current through them. Fuse links that remain intact connect all the logic blocks required to perform a desired function. The Signetics Field Programmable Logic Sequencer (FPLS) circuit has 904 programmable gates; this is equivalent to 442 medium scale integration transistor-transistor logic (MSI TTL) packages, and is useful for implementing almost any synchronous state machine. A keyboard scanner would be one such application. A single FPLS circuit can scan, debounce, and soft-encode a 60-character key set, with substantial savings in time, components, and cost.

Designing a Keyboard Encoder

Requirements for four critical functions are involved in the design approach: keyboard scanning, key debouncing, key encoding, and indication of key data availability. The rate at which a keyboard encoder scans keys determines to a large extent the size of the keyboard (number of keys) to which the encoder can be linked. For instance, if an encoder requires 10 ms to scan a single

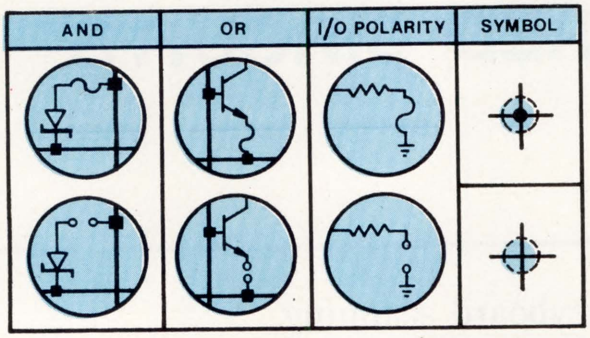

Fig 1 Crosspoint couplings. Intact NiCr fusible links at crosspoints are opened selectively by programming current

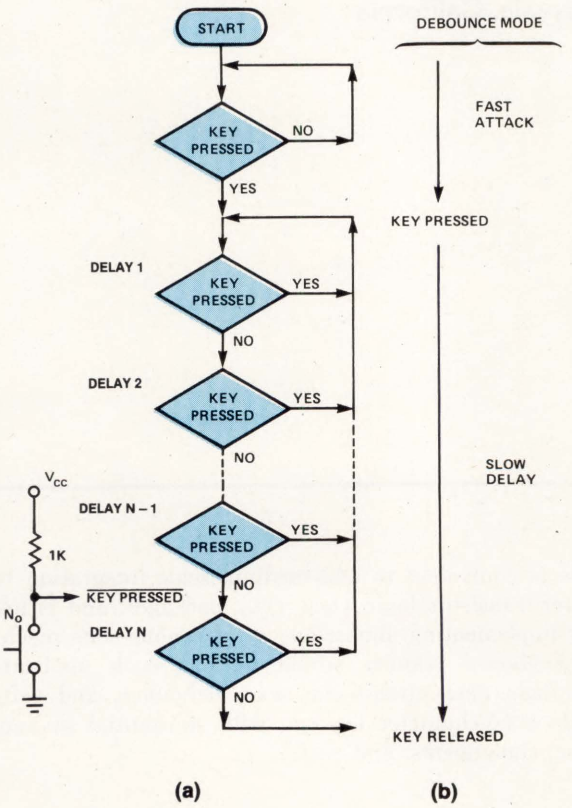

Fig 2 Scanned key (a) and sampling debounce algorithm (b). Each key acts as contact to ground, pulled up through resistor to V_{cc}, producing encoded zero output when closed. Fast attack detects closure in one sampling period. Slow delay takes several samples to determine that key was released

key, it would take 0.6 s to scan a 60-key layout. This scan time would allow data entry no faster than 1.6 keys/s, and such relatively slow scanning speed has only limited utility.

Two basic scanning operations may be performed simultaneously to increase scanning speed to a more useful rate. This involves scanning the keyboard and scanning or debouncing a particular key at the same time. The arrangement requires two scan counters: one to scan the entire keyboard and the other to scan a particular key that has been depressed. Concurrent performance of these two functions allows much shorter scan time across the entire keyboard.

Another technique increases scanning speed by using a single counter that scans very quickly and marks or increments an additional counter to indicate how long each key has been depressed. The shortcoming of this method is that every key requires a counter to keep track of how long the key has been depressed. However, most counters that use this technique do not encode, or do not provide N-key rollover, and allow only a single key to be depressed at any one time. Thus, only a single counter is needed to debounce each key.

There are two generally accepted techniques for key debouncing. The first employs a resistance-capacitance (RC) network on each line that effectively serves as a lowpass filter. During a switch transition, on to off or off to on, switch bounce occurs at a frequency high enough to be rejected by the low pass filter. The knee of the filter is usually around 100 Hz.

The second technique employs a modified low pass filter; specifically, a digital filter. The procedure is implemented by sampling the switch waveform to determine the stability of either the on or the off voltage state. For a typical scanned key, the digital filter performs a fast attack, slow delay algorithm (Fig 2), in which each decision block represents one sample.

When a depressed key is first detected, the digital filter enters the "key pressed" mode. For the algorithm to enter "key released" mode, there must be N consecutive no-key-pressed samples. For a given sampling rate, the knee of the filter can be adjusted to accommodate a key bounce of any duration. For a 10-ms debounce period, or a 100-Hz filter knee, the number of delays, N, is the quotient of the sampling rate divided by the filter knee, or N = 10. Thus, for a 1-kHz sampling rate, there must be 10 sample delays before a key can be considered released.

After a depressed key has been detected and debounced, the key signal must be encoded into the format required by the application. With so called hard encoders, the encoding translation is fixed by the manufacturer and no variation is possible. Soft encoding permits the designer to program one or more keys for an arbitrary output code, providing far greater flexibility in the application.

After the output code is asserted, the encoder must indicate that valid key data are available. This indication can be obtained in one of two forms, either through a strobe asserted during the time that the key is depressed, or through a clock pulse generated only once per key depression.

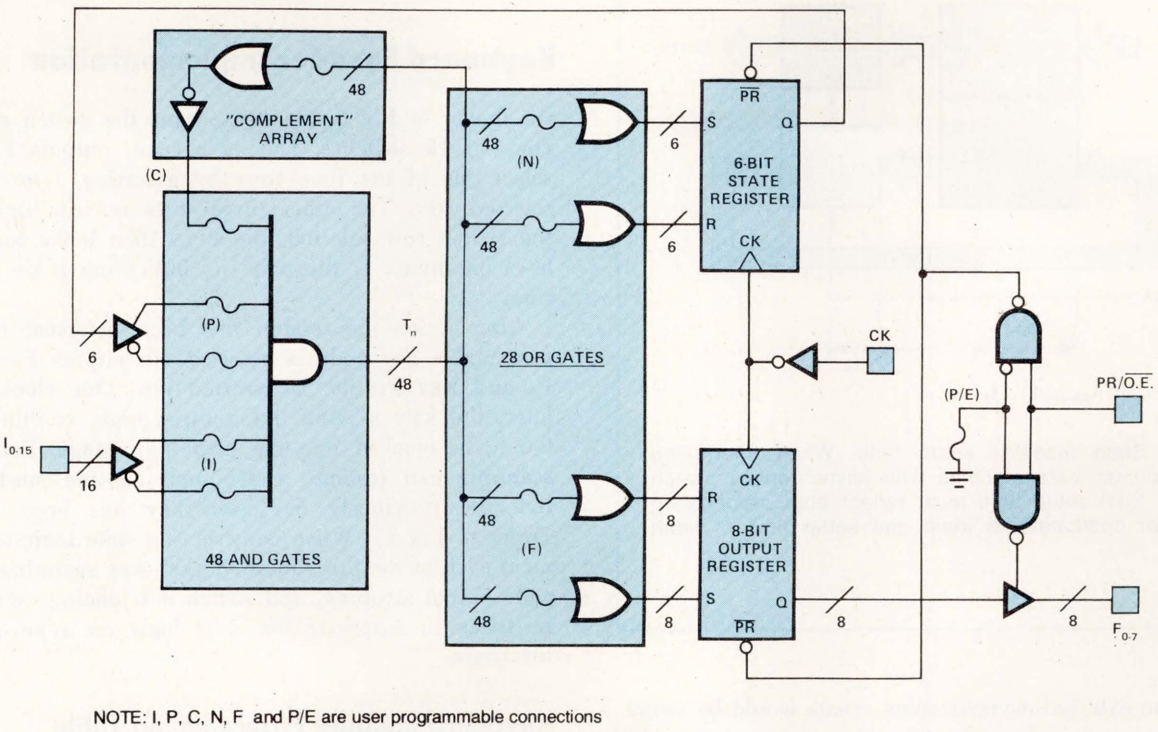

Fig 3 FPLS block diagram. AND gate array combines 16 external inputs (I_0-I_{15}) to form up to 48 transition terms (AND terms). All terms may include true, false, or don't care variable designators and are merged in OR array to issue next state and next output commands. Both true and complement transition terms can be generated by optional use of internal input variable (C) from complement array

Many keyboard encoders are currently available; however, most of these cannot operate without microprocessor control or do not provide the flexibility needed to customize debounce time, key codes, and type of data available indication. The ideal keyboard encoder for optimum circuit and physical design benefits would be a single chip with programmable operational parameters. The 82S105 FPLS is one device that meets these requirements.

The 82S105 is a bipolar programmable state machine, of the Mealy type, whose output is a function of both the present state and the present input. It contains AND-OR gate logic with programmable connections that control the inputs to onchip state and output registers. The state and output registers comprise positive, edge-triggered, R-S flipflops of six and eight bits, respectively (Fig 3).

Preliminary Design Considerations

Interfacing a synchronous state machine, such as the FPLS, with an asynchronous keyboard switch matrix requires a unique state machine algorithm. In order to avoid erroneous outputs, the grouping of combinational logic and a latch in a synchronous circuit must provide a setup time that adds the propagation delay of the combinational logic block to the setup time of the latch (Fig 4). Failure to establish setup time limits can result in undesired state or output transitions (Fig 5). With a keyboard interfaced to the input of the state machine, there is virtually no method for controlling setup time because a key can be pressed at any moment; however, there are design approaches that will circumvent the problem.

One technique inserts a latch between the keyboard and the state machine, with the latch using the same clock edge as the state machine. Since the state machine clock period must exceed the setup time in order to satisfy the logic delays in the internal state register path, each keyboard line will have at least one clock period setup time. Although the latch adds another component to the encoder, this approach still reflects minimal hardware.

Another technique uses segregated logic. Under this method, state machine logic is separated so that any external asynchronous event affects no more than one state or one output register bit. In a keyboard encoder appli-

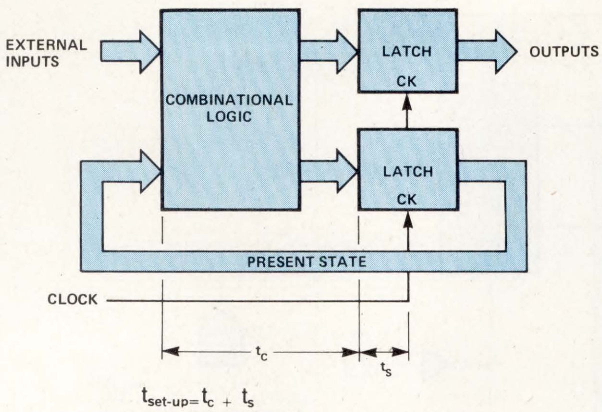

Fig 4 State machine setup time. When interfacing synchronous state machine with asynchronous switch matrix, total setup time must reflect both propagation delay of combinatorial logic and setup time of latch

cation, the external asynchronous events would be switch transitions, and only one state or output register bit should be affected by each. With the FPLS architecture, such setup time violations produce only time delays, not erroneous state or output changes, because machine operation simply halts until the next clock cycle when setup time is adequate (Fig 5).

Keyboard Encoder Implementation

As shown in Fig 6, the FPLS scans the switch array in rows of 15 switches. During a scan, outputs F_0 to F_3 select one of the four rows by asserting a low on the selected row. The other three rows remain high. With the switch row selected, the FPLS then looks for a low level on inputs I_1 thorugh I_{15}, indicating a key depression.

After a key depression has been detected, the programmable key code is asserted on outputs F_0 through F_6 and KEY STROBE is asserted low. One clock period later, the KEY STROBE line returns high, enabling DATA 0-6 to be clocked into the next logic stage. Before key scanning can resume, a debounce routine must assure that the previously depressed key has been released (refer to Fig 2). When constructing state logic to implement each of the three major tasks—key scanning, switch code output strobing, and switch debouncing—care must be taken to segregate the state logic on a per-register-bit basis.

Keyboard Encoder Programming Table

The keyboard encoder programming table (Fig 7) shows, in fuse form, the algorithm required to perform a keyboard scan of 60 keys. There are five basic sections in

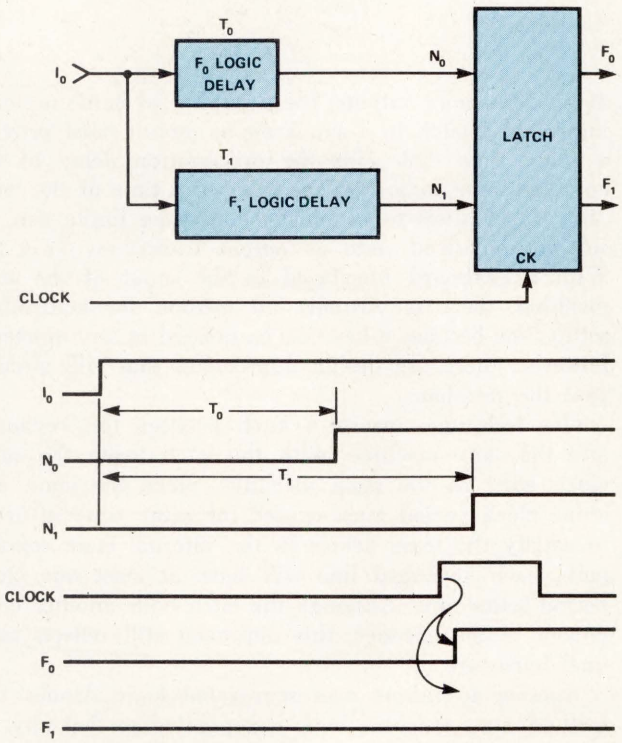

Fig 5 State machine setup time violation. Signal on I affects two different outputs, F_0 and F_1. When I_0 is asserted high, both F_0 and F_1 are to assume high next output state. However, since F_1 has propagation path longer than F_0 and requires full setup time, any setup time violation results in next state of $(F_1, F_0) = (0, 1)$ instead of correct output, $(F_1, F_0) = (1, 1)$

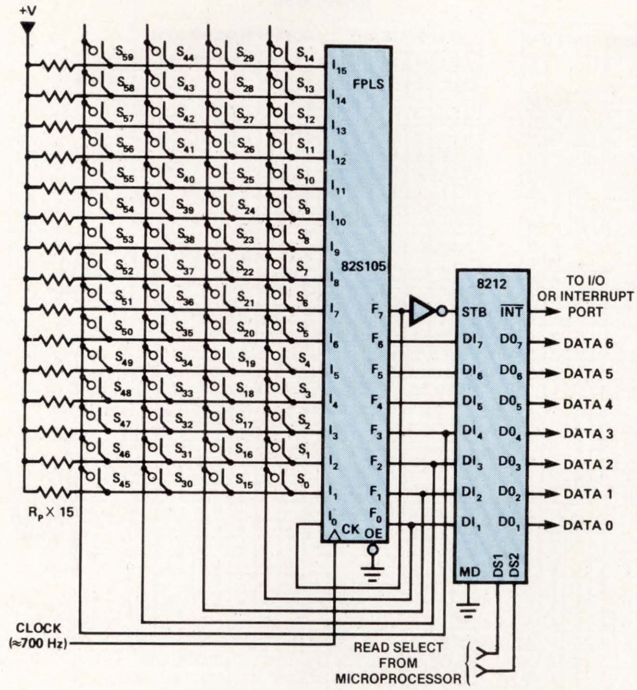

Fig 6 Keyboard encoder circuit diagram. FPLS scans switch array in 4 rows of 15 switches. Once switch row is selected by low level indication, FPLS seeks low level within that row to locate depressed key. At right, 8212 provides holding register function for microprocessor interface

the programming table. The leftmost section, labeled "C," determines how the complement array is programmed. The next section to the right is the Input Variable section that defines how the 16 external inputs are fused into the respective AND gates. For example, a dash specifies no connection for the associated input, an "L" denotes an inverting connection, and an "H" indicates a noninverting connection. Similarly, the Present State sector, the next section to the right, also specifies connections to the same AND gates. Each AND gate in the FPLS has 22 inputs, 16 external inputs and 6 inputs for the present state register. The Input Variable and Present State columns in the programming table indicate how each AND gate is to be programmed.

Next State and Output Function columns of the table indicate how the conditions defined on the left side of the table, in the Input Variable and Present State columns, establish the next output code and the next state code. In this section of the table, a dash specifies no change in the corresponding register bit position, "H" specifies that the bit position will go to a 1 level, and "L" specifies that the bit position will go to a 0 level.

In the upper right-hand corner of the table, an additional option feature, Option P/E, accepts an "H" entry to allow the preset/output enable lead to act as a preset line for all internal registers. If an "L" were inserted here, that lead would act as an output enable lead.

Key Scanning State Logic

Scanning is done by a modulo 60 counter (Fig 8). At each state, a different key is sampled for a change of state. The cyclic count continues until the KEY STROBE line, STB in the state diagram, is asserted low. Logic to implement this counting sequence appears in lines 0 to 8 of the FPLS Programming Table (Fig 7).

The FPLS monitors a different key in each scanning state. When a monitored key is depressed, the KEY STROBE line is asserted low after the next clock pulse, thereby stopping the scanning count. This count represents the key code of the depressed key. By changing the key that is monitored during each state, the code associated with that key may be changed. The map that associates a monitored state switch with each key appears in lines 9 through 23 of Fig 7.

Switch Code Output Strobing

The switch code, DATA 0-6, is held in the state register after low assertion of the KEY STROBE line. During scanning, all but the least significant state bit are updated continuously at the FPLS outputs. Programming

																								OPTION (P/E)													H	
TRANSITION TERM																								OUTPUT TERM														
		INPUT VARIABLE (Im)																PRESENT STATE (Ps)						NEXT STATE (Ns)						OUTPUT FUNCTION (Fn)								
No.	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	•	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	L	—	—	—	—	—	H	—	—	—	—	—	—	—	—	
1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	L	H	—	—	—	—	H	L	—	—	—	H	—	—	—	—	
2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	—	L	H	H	—	—	—	H	L	L	—	—	H	L	—	—	—	—	
3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	L	H	H	H	—	—	H	L	L	L	—	H	L	L	—	—	—	—	
4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	L	H	H	H	H	—	H	L	L	L	H	—	L	L	L	—	—	—	—	
5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	L	H	H	H	H	H	H	L	L	L	L	H	—	L	L	L	H	L	H	H	
6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	H	H	H	H	H	L	L	L	L	L	H	—	L	L	L	H	H	H	L	
7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	L	L	H	H	H	H	—	—	—	—	—	—	—	—	—	—	H	H	L	H	
8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	L	H	H	H	H	—	—	—	—	—	—	—	—	—	—	L	H	H	H	
9	—	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	L	L	L	H	—	—	—	—	—	—	L	—	—	—	—	—	—	—	
10	—	—	L	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	L	L	H	L	—	—	—	—	—	—	L	—	—	—	—	—	—	—	
11	—	—	—	L	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	L	L	H	H	—	—	—	—	—	—	L	—	—	—	—	—	—	—	SCAN LOGIC
12	—	—	—	—	L	—	—	—	—	—	—	—	—	—	—	—	H	—	—	L	H	L	L	—	—	—	—	—	—	L	—	—	—	—	—	—	—	
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17	—	—	—	—	—	—	—	—	—	L	—	—	—	—	—	—	H	—	—	H	L	L	H	—	—	—	—	—	—	L	—	—	—	—	—	—	—	
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24	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	—	—	—	—	—	H	L	L	L	L	L	L	—	—	—	—	H	—	—	—	
25	•	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	—	—	—	—	—	L	L	L	L	L	L	L	—	—	—	—	L	—	—	—	OUTPUT LOGIC
26	A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	L	L	L	—	—	—	—	—	—	H	—	—	—	—	—	—	—	
27	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	L	L	L	L	
28	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	—	H	—	—	—	—	—	—	—	—	L	L	L	L	
29	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	L	H	L	L	L	L	—	L	—	—	—	—	—	—	—	—	L	L	L	L	
30	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	L	L	L	L	H	—	—	—	—	—	—	—	—	—	—	—	—	—	
31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	L	L	L	L	L	—	H	—	—	—	—	—	—	—	—	—	—	—	—	
32	—	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	
33	—	—	L	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	
34	—	—	—	L	—	—	—	—	—	—	—	—	—	—	—	—	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	
35	—	—	—	—	L	—	—	—	—	—	—	—	—	—	—	—	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	
36	—	—	—	—	—	L	—	—	—	—	—	—	—	—	—	—	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	DEBOUNCE LOGIC
37	—	—	—	—	—	—	L	—	—	—	—	—	—	—	—	—	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	
38	—	—	—	—	—	—	—	L	—	—	—	—	—	—	—	—	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	
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44	—	—	—	—	—	—	—	—	—	—	—	—	—	L	—	—	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	
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46	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H	L	L	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	
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Fig 7 Keyboard encoder programming table. In logic form, table shows algorithm required to scan 60 keys. Lines 0-8 reflect cyclic key scanning count. Lines 9-23 map states into particular key. Lines 24-25 complete output key code. Line 26 completes output cycle. Remaining lines reflect debounce logic

table lines 24 and 25 transfer this remaining bit to output F_4, completing the output key code. Programming table line 26 then returns the KEY STROBE line high, completing the output cycle. Devices that receive key codes from the FPLS should clock DATA 0-6 in on the low to high transition of the KEY STROBE line.

Switch Debounce Routine

After the code output cycle is complete, but before scanning can resume, a switch debounce routine must be completed. For proper operation of this routine, all keys must be released for a time span greater than the period of the digital debounce filter. By ensuring that no keys are depressed, instead of checking only the detected key, the FPLS guards against multiple, simultaneous key entries. Fig 9 shows the debounce state logic programmed in the FPLS Programming Table, lines 27 to 47.

Encoder Interface to a Microprocessor

A keyboard encoder can interface with a microprocessor in either a scanned or interrupt driven mode. In a scanned system, the microprocessor periodically monitors the encoder to determine whether any switches have been pressed. If it detects a switch depression, the microprocessor collects and processes the key data. In an interrupt driven system, a key depression interrupts the microprocessor program flow and causes an interrupt service routine to process the key data.

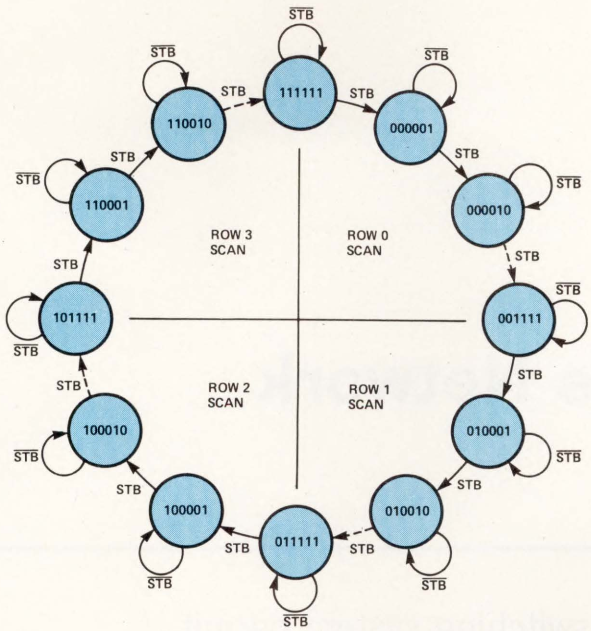


Fig 8 Key scanning state diagram. Modulo 60 counter forms sequence required to monitor all 60 keys. At each state, different key is sampled for change of state. When monitored key is depressed, KEY STROBE line (STB) is asserted low after next clock pulse, thereby stopping key scanning count, which signals unique code for each depressed key

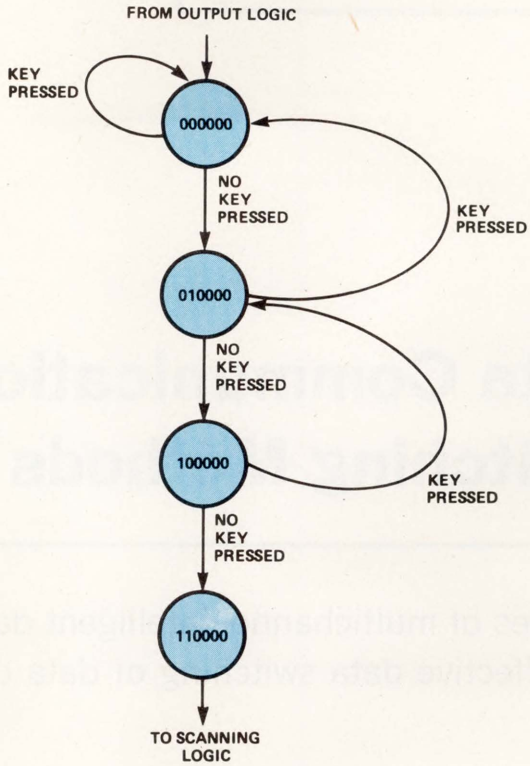


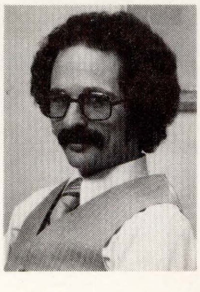
Fig 9 Switch debounce state diagram. Sequence of events that must occur to properly debounce a key are shown. FPLS programming to establish this procedure appears in programming table lines 27-47

With the addition of a key data holding register, the FPLS based keyboard encoder can support either processor interface. In Fig 6, the 8212 8-bit register forms a latch that provides the holding register function and serves as the primary interface between the encoder and the microprocessor. Note that although the 8212 is an 8-bit device, only seven bits are used for this interface application. The INT output is asserted low when the FPLS KEY STROBE line pulses the key data, DATA 0-6, into register inputs DI_{1-7}. This line may be connected to the microprocessor I/O port for a scanning interface, or it may be connected to the microprocessor interrupt request port for interrupt driven operation. In either mode, once the microprocessor has been notified, key data may be read from the holding register outputs, DO_{1-7}.

Data are read from the latch by asserting the two chip select leads on the latch, DS1 and DS2, to their enabled condition. This instructs the latch's 3-state buffers to assert the key data onto the microprocessor bus. It also clears the interrupt port to the idle condition so that it can scan for the next key. In both a scanned mode and interrupt mode, the interrupt lead from the latch is the commanding element.

Conclusion

In every microprocessor based system, the software and the system architect must be concerned with the partitioning of functional tasks. Each task requires a decision to implement in software or to implement in external hardware. Once that decision is made, it is usually a simple task to find appropriate peripheral support circuits for use in a hardware approach. The FPLS offers the ability to customize a specific external function for optimum efficiency in this case.



Stephen Durham is marketing manager for Signetic's bipolar RAM product line, responsible for assisting developments in this technology. He has participated in the design of various microprocessor based telecommunications systems including a mobile telephone system, a vehicular status reporting system, and a custom PBX processor. He holds a BSEL degree in electronics from California State Polytechnic University.

TECH NOTE

Data Communications Network Switching Methods

Features of multichannel intelligent data switching system permit cost-effective data switching of data communications networks

David A. Kane Develcon Electronics Incorporated, Doylestown, Pennsylvania

Today's data communications networks are considerably more complex and larger than the systems in use just a few years ago. Too often, however, these networks have been limited in their rate of growth and usefulness due to the lack of adequate data switching facilities to interconnect system elements. More direct, selective, interterminal communications links are needed to meet the requirements of increasingly intelligent data communications systems. The technology required to effectively interconnect data in these systems has grown in proportion with the advances in data processing's state of the art.

Previously, there were two popular methods of connecting the various hardware in the network: the dial-up lines of common carrier facilities, and dedicated channels and contention hardware. Recently a multichannel, intelligent data switch system has been developed. Connection methods are chosen depending on criteria such as the distances involved and the amount of time a device in the network must remain online with another device.

Common Carrier Facilities

The common carrier or dial-up facilities connect each device in the data processing network to separate multiline rotary exchanges (see Fig 1). This connection enables an unlimited group of users to contend for service port groups through the common carrier switched network—all on a first come, first serve basis.

In a typical timesharing application, the telephone rotary contention allows support of up to four terminals per computer. This permits realization of significant savings in computer port hardware. In addition, there is improved utilization of the computer ports installed. When the computer is busy or connected, the user receives these indications via the telephone rotary. Moreover, terminal users may gain access to different computer systems or support different applications programs on the same computer system, so dial-up access may be used to provide a port selection facility.

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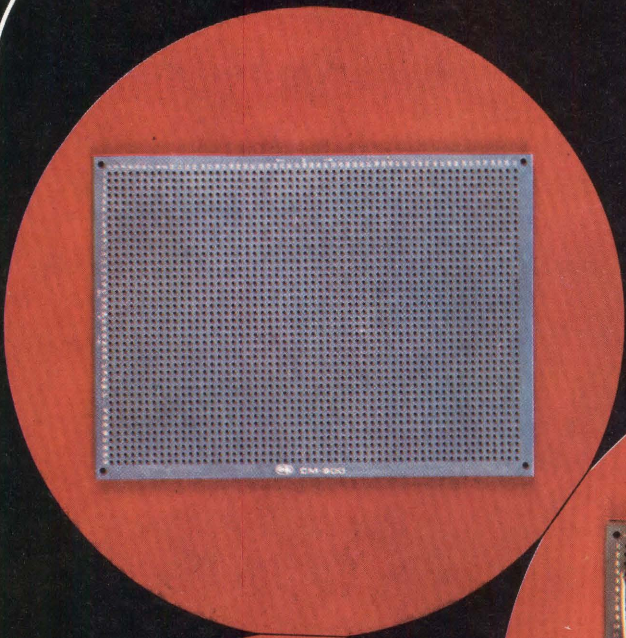

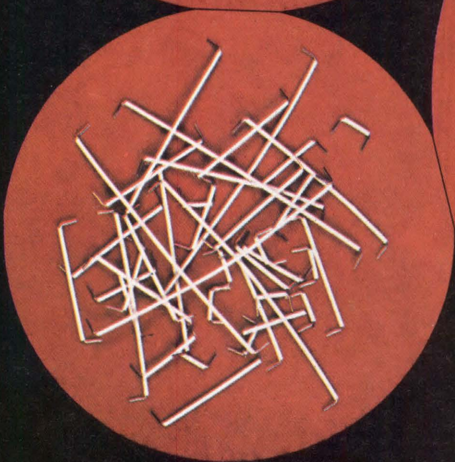

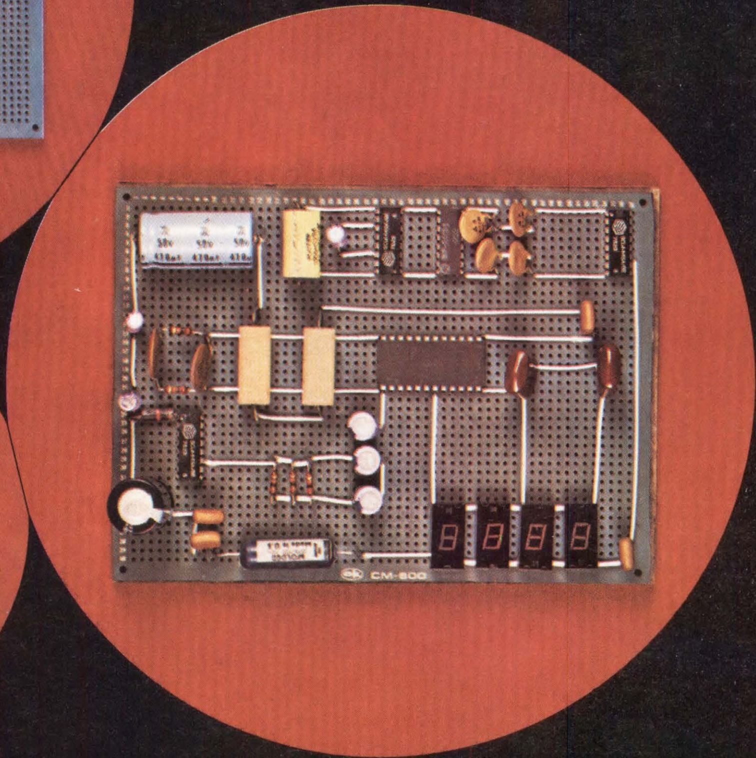

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Since dial-up access is dependent upon the telephone, many of this system's advantages are negated by the ever increasing telephone and equipment costs and by limiting performance factors. Because this approach operates on a 2-wire circuit, there are data transmission speed restrictions. Even with the new modems available, the maximum speed is only 1200 baud. Controlled carrier operations with synchronous speeds up to 9600 baud are possible, however, many terminals don't have the required interface control signals for these operations.

With common carrier facilities, no statistical information as to system usage is available. There is no way to exactly determine how many users dialed but were unable to connect with the computers. There are also no statistics for the number of successful calls. If this type of information were available, computer center managers could determine more accurately the efficiency of their operations.

Another problem facing common carrier facility users is the increasingly higher tariffs charged by the telephone company for use of its facilities. Originally the tariffs were based on voice usage. The typical phone call lasted three to five minutes and billings were charged for the number of these short calls. Now, since so many computer users connect to the data terminal by the switched telephone network, phone calls are much longer. Many terminal users are connected for eight or ten hours through the common carrier facility every business day.

The phone company wants to be compensated for this type of usage and now penalizes terminal users with a new tariff in which business usage is measured in increments of five minutes or less. Single message units are charged for each 5-min increment. These tariffs may adversely affect users with PABX and Centrex services. Heavier reliance on these services may result in larger systems—even though voice traffic may not warrant it.

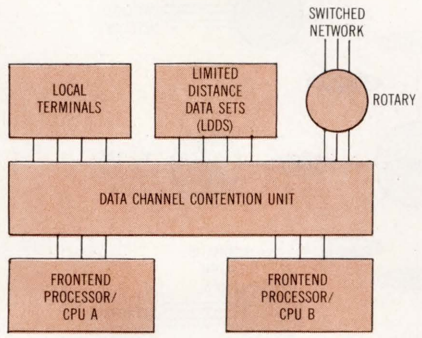


Fig 2 Dedicated channels and contention hardware. More economical than common carrier system, however, interprocessor connections are difficult and number of ports and terminals are limited by hardware

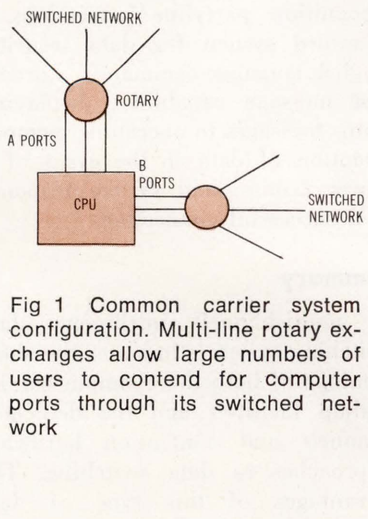


Fig 1 Common carrier system configuration. Multi-line rotary exchanges allow large numbers of users to contend for computer ports through its switched network

Dedicated Channels and Contention Hardware

This method, commonly known as port contention, eliminates some of the problems associated with the dial-up access approach. Service requests are hardware generated. It is more economical—channels are normally leased or owned. The response to service requests is fast. Also, statistical information on system usage may be available.

The dedicated channels and contention hardware approach (Fig 2) does have limiting factors. It presumes that associated equipment are either ports or terminals, and the hardware limits the number of ports and terminals that can be utilized. Inter-processor (port to port) connections are difficult. This method may not provide connect and busy indications.

Multichannel Intelligent Data Switch

There is yet another means of connecting terminals to computers, one that eliminates all of the shortcomings of the other two methods, as well as offers many additional advantages. The technique, called multichannel intelligent data switching, is comparable to the typical central office in a modern switched telephone network. With this approach (see Fig 3), any device in the network can access any other device in the network. Computers

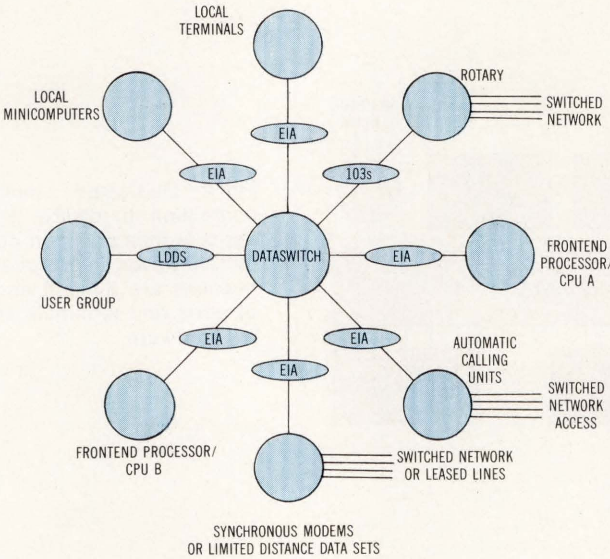


Fig 3 Multichannel intelligent data switching system. Similar in theory to central office in modern switched telephone network, any device in system can communicate with any other. System hardware is not limited

can communicate with terminals, terminals can talk with printers, printers with computers, and peripheral devices can talk with each other.

Through a unique combination of hardware and software the data switch system controls and coordinates all ports, integrating both the dial-up and dedicated access approaches. The system permits non-biased use by operating on a first come, first serve basis. All subscribers (devices in the system) have an equal opportunity to originate requests to any other subscriber. The subscribers contend for a number of incoming channels, or lines, and for computer communications interfaces (ports).

The data switch intercepts a subscriber's request for service, reviews whether the service is available, and then either completes the connection or advises the calling subscriber that the connection cannot be made. Up to 2048 subscribers may be connected, and the system will allow up to 1023 simultaneous full-duplex connections. Communications links in a data communications network incorporating a data switching system may be by dial-up, leased line with limited distance modems, by local terminals, or through any device with an EIA standard RS-232 interface.

Devices with different bit rates or character sets in the network are responded to automatically with a data switching system. A 1200-baud terminal contending for the same deck with a 2400-baud device, will automatically be connected to the first 1200-baud port available in that deck; the 2400-baud device will automatically be connected to the first 2400-baud port available. Essentially, all mixing of transmission speeds is handled by the system. Once port to port connections are made, full-duplex conversations proceed without further intervention. When one party desires to end a connection, the system disconnects both devices simultaneously.

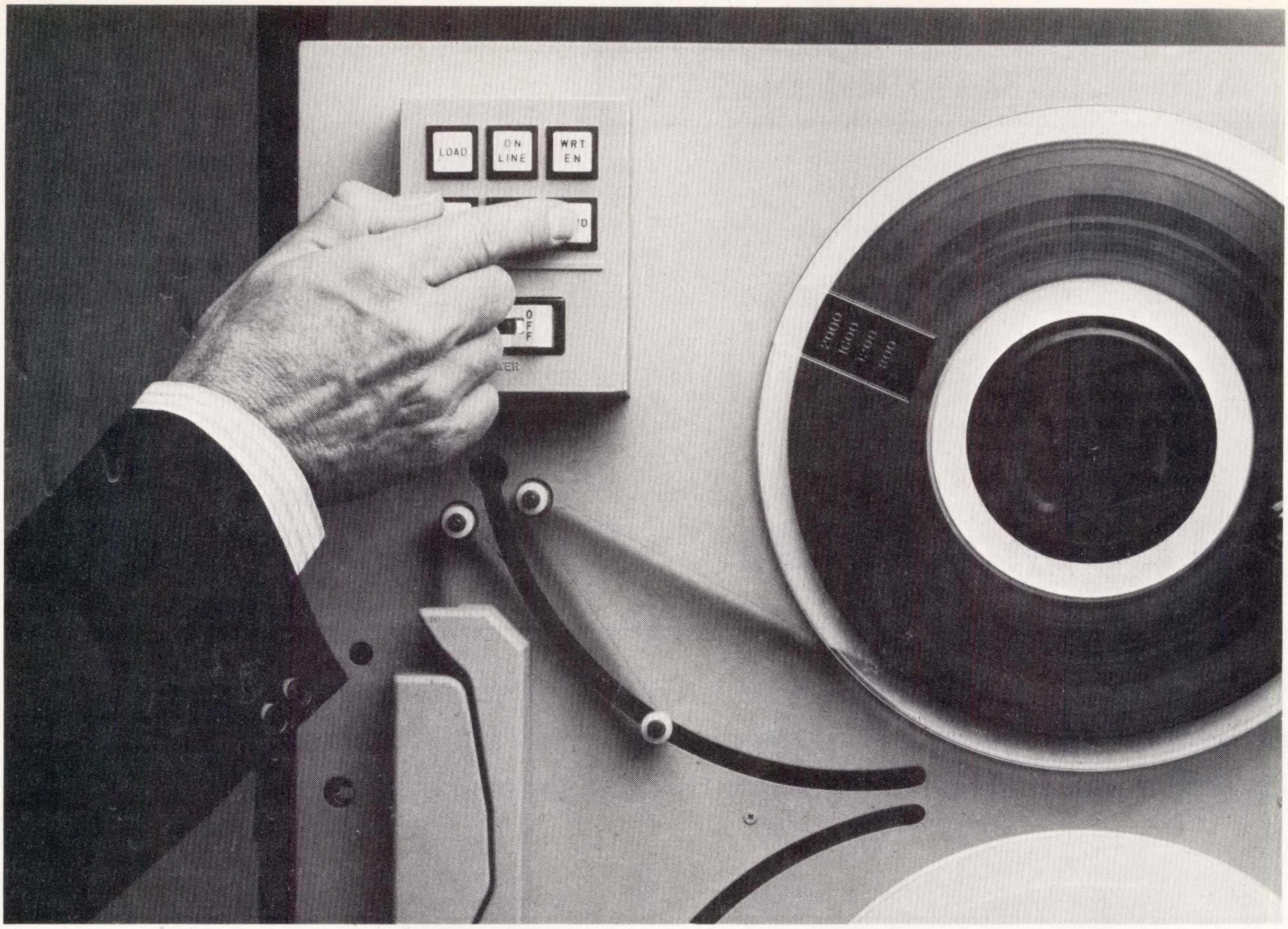
Data switching methods improve computer utilization by expanding data communications line capacities of a realtime computer system. They can be used to optimize computer port utilization for such applications as university campuses, military bases, and hospital complexes where private wires and terminal connections are often required to minimize transmission costs when dedicated channels are uneconomical due to low usage. The data switching method also circumvents the single message unit tariff imposed by the telephone company, without the use of leased or private lines.

Several considerations will insure continued cost-effectiveness, usefulness, and even growth of the system. Maximizing the number of possible terminals, ports, and subscribers will expand the data communications network. The ability to accommodate different codes and transmission speeds ranging from 1200 to 19.2k baud will also assure future growth. The highest possible synchronous and asynchronous transmission speeds will help maximize the cost-effectiveness of the system.

For a truly effective data communications network, the central switching device must be capable of permitting universal access to all devices in the network. In addition, the number of simultaneous connections at any one time should be sufficiently high to allow maximum operating efficiency. Other desirable features include prioritized queuing, account recognition, partyline connections. a password system for data security, English language commands, a broadcast message capability, displaying status messages to operators, memory retention of data in the event of a power failure, and system response to a successful connection.

Summary

A multichannel intelligent data switching system eliminates the short comings of both the common carrier dial-up facilities and the dedicated channels and contention hardware approaches to data switching. The advantages of this type of data switch help lower overall costs of data communications, improve efficiency, and enhance network performance. □



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CRT controller permits improved video display system design by means of flexible, multiple operating modes; with a few additional components, controller will function simultaneously as a simple keypad scanner

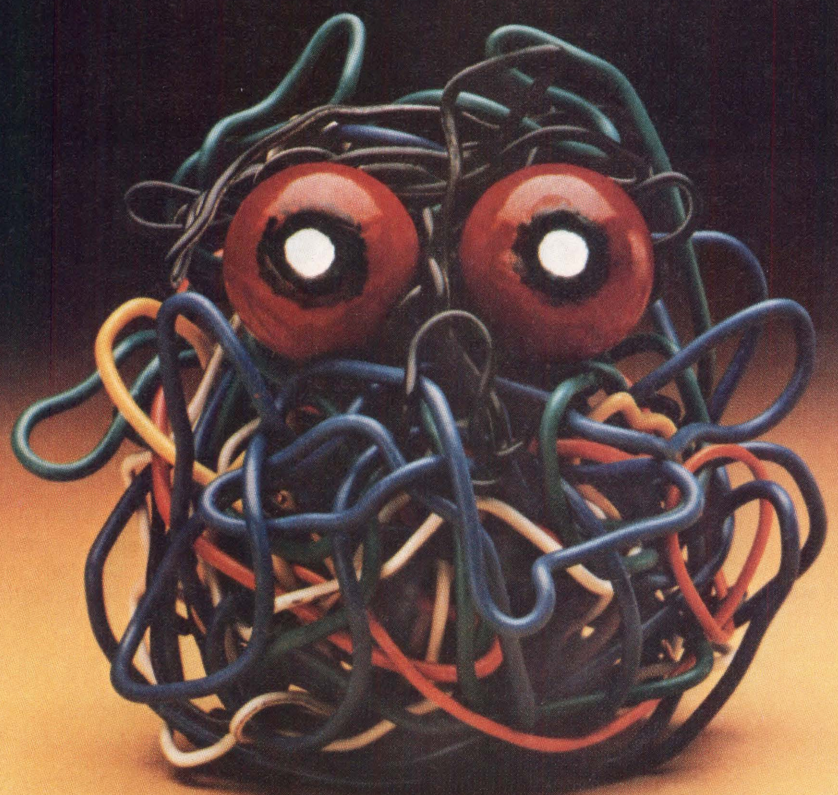
Conrad J. Boisvert Synertek Incorporated, Santa Clara, California

Single-chip microcomputers extend the impact of microprocessors toward the low performance end of systems applications. Characteristics that lend themselves effectively to this technology are small size, low cost, relatively simple tasks, and high production volume. The high performance end of the applications spectrum is supported by programmable, dedicated controllers, including devices such as floppy disc controllers, keyboard encoders, communications controllers, IEEE-488 bus interfaces, direct memory access controllers, and interrupt controllers. Main advantages of these devices are low parts count for small system design, low system cost, high level of controller autonomy to relieve microprocessor burden of control, flexible system design gained by programmability, and inventory simplification by requiring only one device type for several different system designs. The evolution from teleprinter terminals to video terminals has been achieved in part by the utilization of microprocessor based designs. Next in evolution will be even more sophisticated systems and lower prices due to dedicated metal oxide semiconductor/large scale integration controller devices.

The wide variety of available cathode ray tube (CRT) controllers permits system design to be tailored specifically to desired capabilities. In some applications, skillful design of a particular CRT controller can result in system capabilities not foreseen when the controller was originally designed. In this case, the CRT system can gain an application advantage if one or more of these capabilities are exploited.

CRT Controller

The SY6545 CRT controller peripheral chip (Fig 1) interfaces with 6500/6800 microprocessors in CRT applications. Fully programmable, this chip permits implemention of a wide variety of CRT screen display formats. Included in the controller are counter outputs for memory addressing



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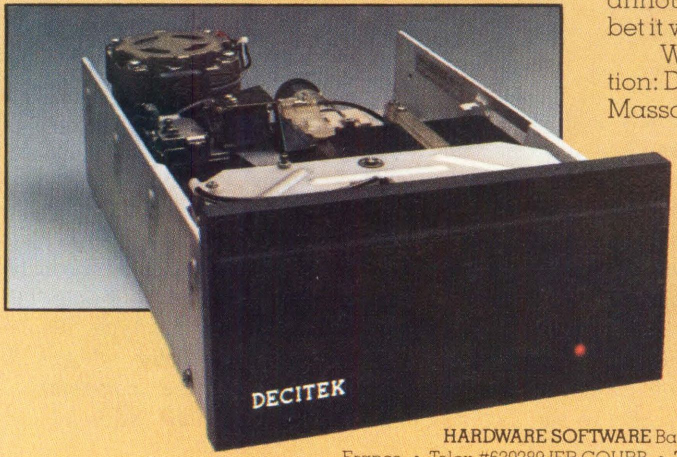

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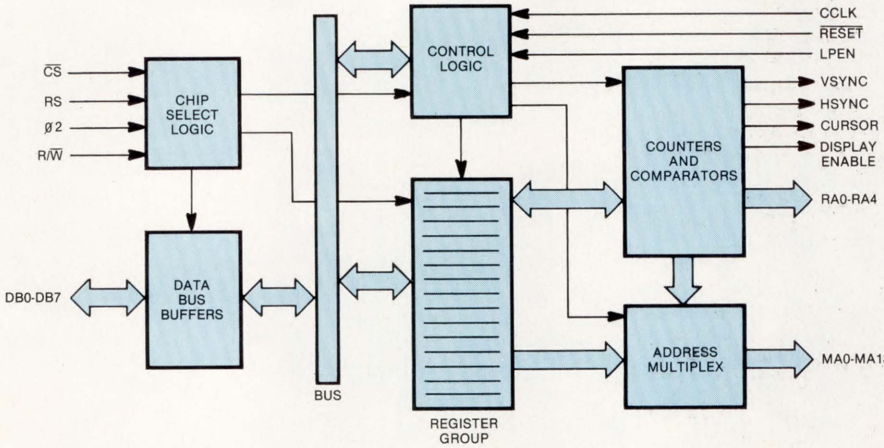


Fig 1 Internal block diagram of SY6545 CRT controller. Register group contains all programmable parameters to fully define video display formats. Counters and comparators are employed extensively to generate scan address and video signals

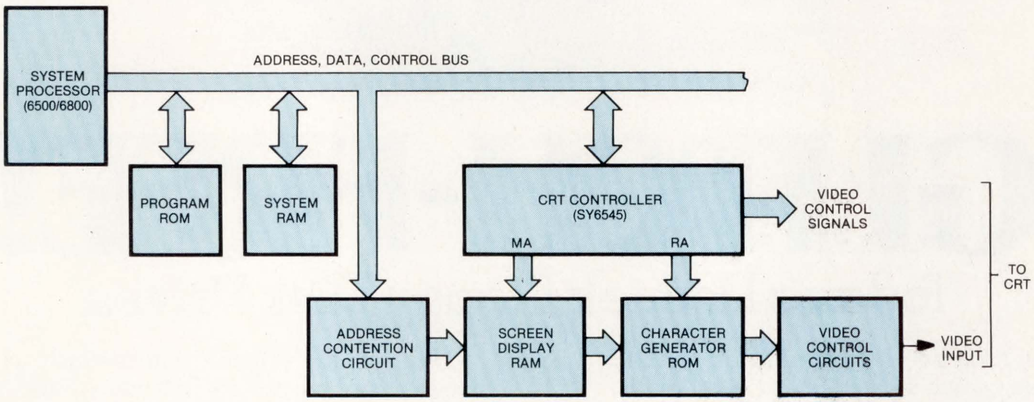
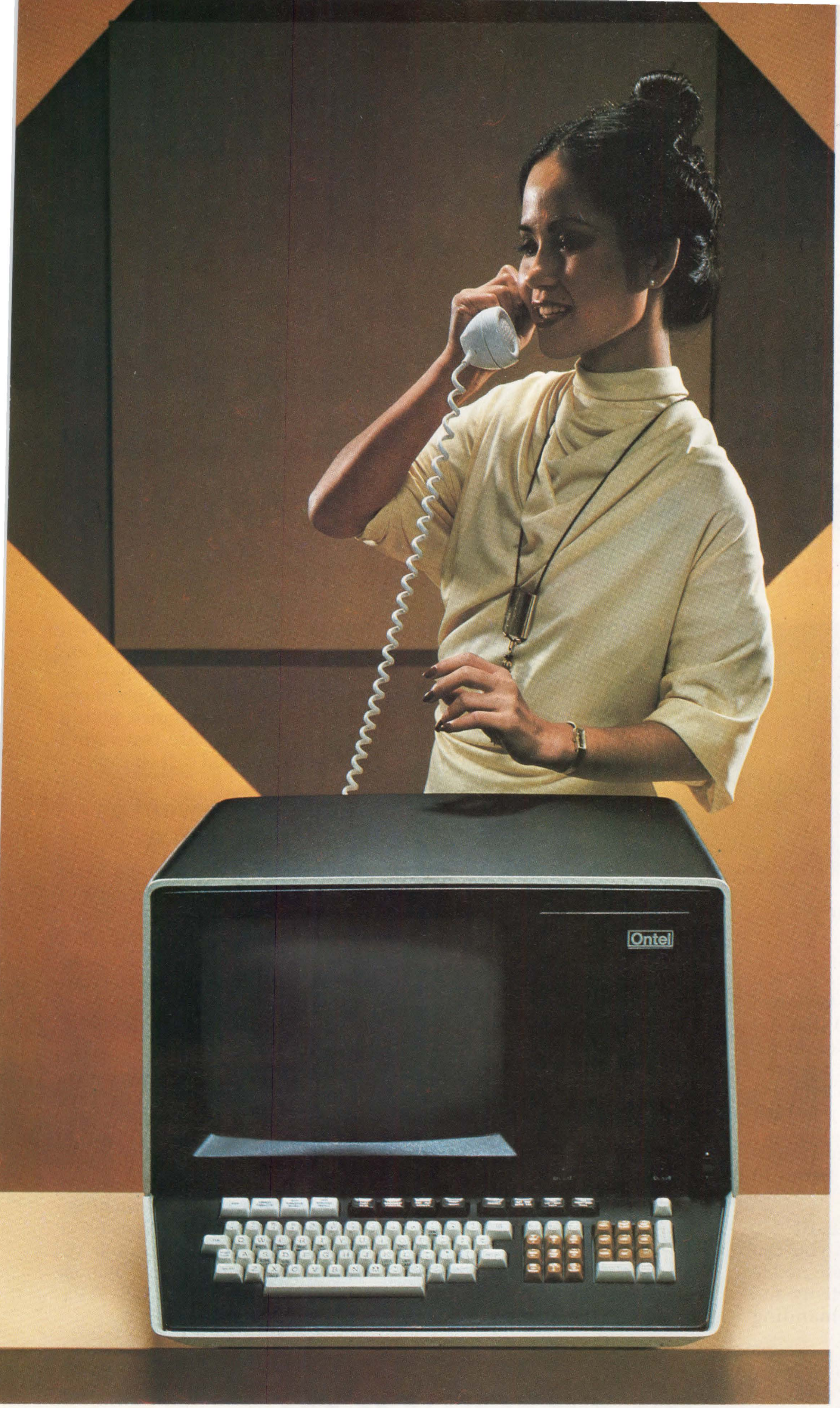


Fig 2 Microprocessor-based CRT system. CRT controller addresses both screen display RAM and character generator ROM. Sizes of RAM and ROM needed depend upon number of characters to be displayed, character font, and size of character set. Address contention circuits permit processor to gain access to screen display RAM in order to read or change its contents

and a strobe input (LPEN) for lightpen applications. These pin functions allow their lines to be used as keypad drive and sense signals without affecting normal CRT operation. The chip's inherent capabilities suit it for simultaneous use as a CRT controller and keypad scanner.

See Fig 2 for a simplified block diagram of a microprocessor based CRT control system. The CRT controller sequentially addresses the screen display random access memory (RAM) to fetch successive characters for display. The character output of the RAM serves as part of the character generator read only memory (ROM) input; the other part is the scan line number generated by the CRT controller. The ROM outputs the dot pattern to be serially generated as the video signal to the CRT monitor. In addition, the CRT controller generates the following video signals: vertical sync, horizontal sync, cursor, and display enable. These signals are necessary, because to keep the screen alive data must be repetitively generated as video inputs to the CRT monitor or TV-type display. As a result, controller address lines MA0 to MA13 are constantly counting from the start address (address of



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first character to be displayed) to the end address (last character displayed). A display size of 80 columns and 24 rows results in 1920 characters, or a block of 1920 addresses, start to finish.

The LPEN input pin on the controller is intended as a strobe input for lightpen applications. Internally, a signal on this pin gates the scanning counter state (MA0 to MA13) into a lightpen holding register. In this manner, when the CRT electron beam passes across the activated lightpen held at the surface of the video screen, a signal generated by the lightpen and applied to the LPEN input of the controller effectively identifies the location of the lightpen relative to the scanning addresses. In most CRT systems, no lightpen capability is required. Thus, the system is not affected if this capability is used as a keypad strobe instead of for its intended lightpen function.

Simplified Keypad Scanning Configuration

The hardware configuration of the CRT controller with an 8 x 8 crosspoint keypad matrix is illustrated in Fig 3. Note that address lines MA0 to MA5 are utilized to scan the crosspoint keypad, but that their operation with the screen display RAM is totally unaffected. Keypad scanning and LPEN input signal generation do not cause interruption of address sequencing on the MA lines. Thus, using MA0 to MA5 to drive the keypad requires no special programming steps, only a 1-of-8 decoder (with active-low outputs) to drive the keypad lines and a 1-of-8 data selector (with active-high outputs) to sense the keypad and to drive the LPEN strobe pin. However, use of the LPEN line for keypad scanning precludes its use for lightpen applications.

Addresses MA0 to MA13 are generated as a result of the character clock input. This clock signal occurs once every character time and automatically increments the scan counter for the MA lines. Closure of a key in the crosspoint keypad has no effect until the specific drive line is energized, and the specific sense line is gated to the LPEN input. At this time, the LPEN strobe occurs, and

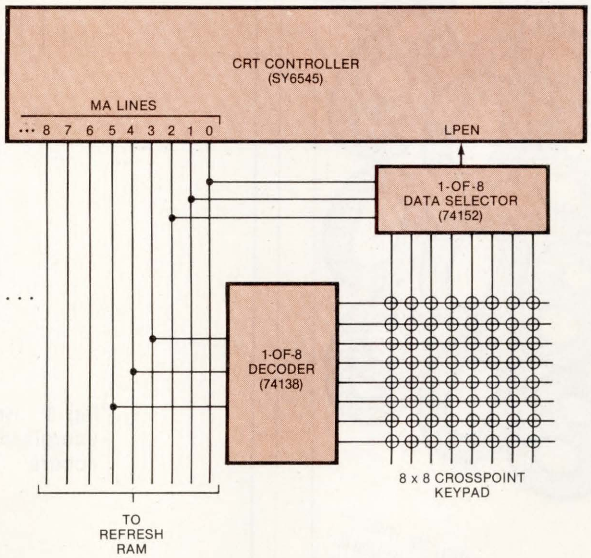

Fig 3 Keypad scan circuits for controller. LPEN line capability is used as keyboard strobe. 1-of-8 decoder drives, while data selector senses keypad matrix; both are driven by sequentially operating address outputs of controller

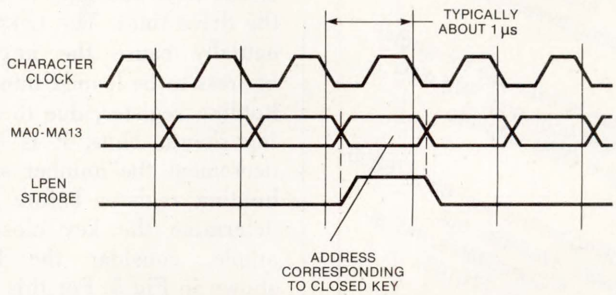

Fig 4 LPEN strobe timing for keypad scan. When address appearing on MA lines matches coordinates of closed key, then drive line and sense line for that key are selected, and LPEN strobe activates

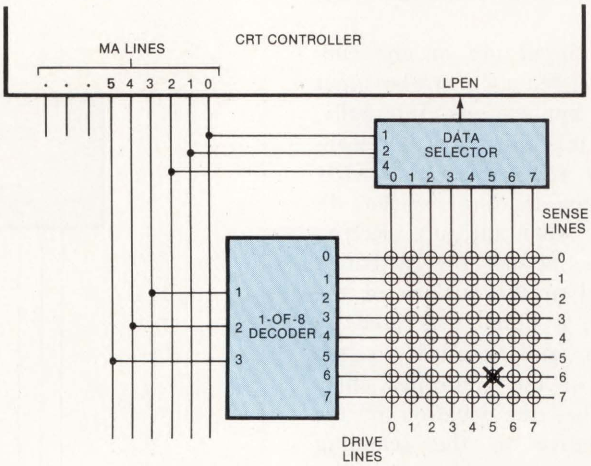

Fig 5 Key closure example. After drive line 6 is energized and sense line 5 is selected, LPEN strobe occurs

the MA0 to MA13 counter contents are loaded into the LPEN holding register (Fig 4).

Programming Considerations For Key Identification

In this application, six address lines are used for the keypad: MA0 to MA2 identify the sense lines for the closed key, and MA3 to MA5 identify the drive lines. The LPEN strobe will actually cause the next sequential address to be loaded into the internal holding register, due to internal timing skews. Thus, it is important to decrement the number stored in the holding register before decoding to determine the key closed. For example, consider the key closure shown in Fig 5. For this case, the MA lines that cause the LPEN strobe are

5	4	3	2	1	0
1	1	0	1	0	1
DRIVE LINE 6			SENSE LINE 5		

However, the LPEN register will contain the next sequential address

7	6	5	4	3	2	1	0
—	—	1	1	0	1	1	0
		6			6		

This is easily corrected in the system program by decrementing one after the contents of the LPEN register are read out.

A lightpen status indication, available in the controller, identifies that a strobe has occurred. This indication is used by the system processor as a means of determining that a key has been pressed and that the LPEN register may be interrogated. The status bit is not usable with the interrupt facility of the processor; so, the processor must periodically scan the status register to check for key closure. This can be accomplished either by hardware timers to initiate the processor status check or by programming periodic checks.

Key debounce must also be handled by software. After a key is determined to be closed, several iterations checking the LPEN status bit and the holding register must be made to verify that the key is indeed closed, and not simply caused by system noise. Likewise, key release must be determined over several iterations.

Bibliography

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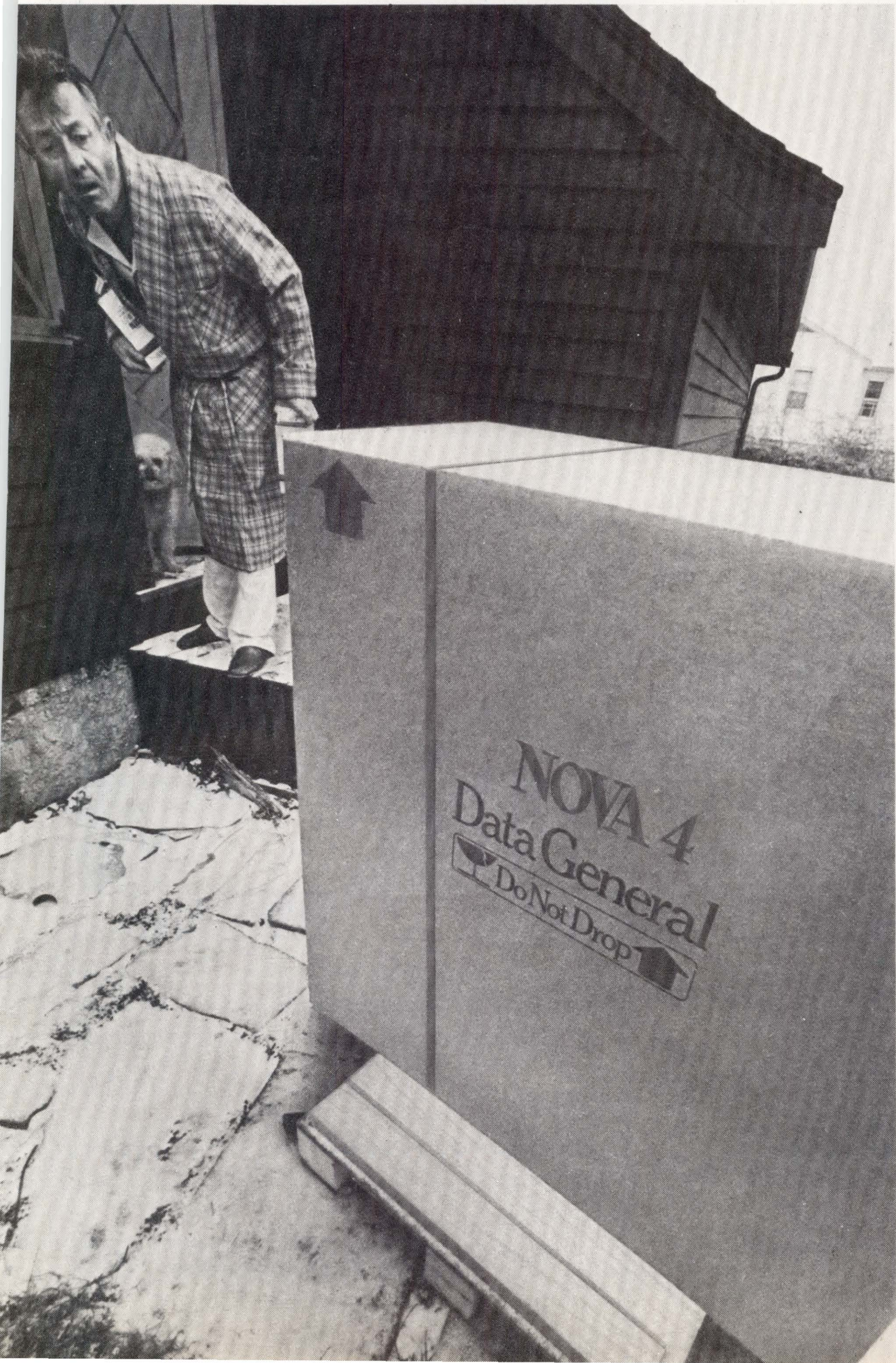

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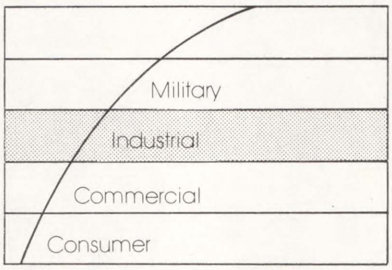
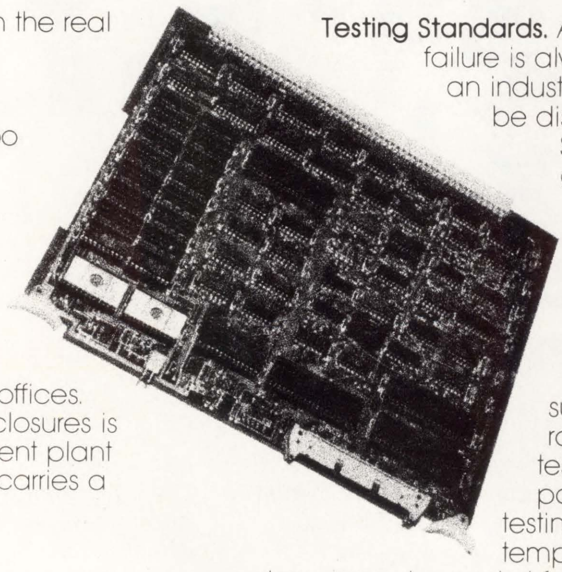


Industrial specifications for military computers are too stringent and too costly to be practical for industrial applications.



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INTERFACING FUNDAMENTALS: CONDITIONAL I/O USING A SEMAPHORE

Peter R. Rony
Virginia Polytechnic Institute and State University
Blacksburg, Virginia

Conditional input/output techniques generally employ a single flipflop, either a flag or a semaphore, to synchronize the data transfer between a microcomputer and a peripheral device. The output from the flag goes only to the microcomputer, whereas the output from the semaphore goes both to the microcomputer and the input/output device.* In view of the trend toward distributed and parallel processing in microcomputer systems, it is worthwhile to investigate in some detail the use of semaphores and flags. This month's column will concentrate on semaphores.

The simplified flowchart in Fig 1 depicts the data transfer between a source of data and an acceptor of data in the presence of a semaphore. There are two semaphore states. A high (logic 1) condition indicates that data are available to the acceptor from the buffer; a low (logic 0) condition indicates that data have been received by the acceptor from the buffer and that the buffer is now empty and can accept new data from the source. The dotted lines, which represent the semaphore output, indicate how the source and acceptor influence each other's sequence of events. For example, as long as the semaphore is sensed low by the source, no new data can be provided to the buffer; while the semaphore is sensed high by the acceptor, this acceptor cannot acquire new data from the buffer.

Fig 2 provides the timing diagrams for another situation in which the source is an input device, such as an analog to digital converter, and the acceptor is a microcomputer. $\overline{\mathrm{STB\ X}}$ is a timing signal that inputs data to the buffer from the input device.* "X" represents a device code that is associated with input device X, distinguishing it from other input devices that are also present in the system. Typically, $\overline{\mathrm{STB\ X}}$ is generated by input device X. $\overline{\mathrm{RD\ X}}$ is a timing signal generated by the microcomputer to input data from the buffer. A logic 0 condition for $\overline{\mathrm{STB\ X}}$ sets the semaphore, and a positive-edge transition in $\overline{\mathrm{RD\ X}}$ clears the semaphore. The sequence of events in Fig 2 can be summarized as follows:

(1) Input data become available from the input device.

(2) The semaphore is set high.

(3) Data are input to the buffer with the aid of the $\overline{\mathrm{STB\ X}}$ signal.

(4) The microcomputer detects the availability of new data in the buffer.

(5) After a period of time, the microcomputer enables the data bus to permit the input of data.

(6) The computer inputs data to the accumulator (or other internal register).

(7) The computer finally resets the semaphore low to indicate to the input devices that the buffer is "empty."

A final situation (Fig 3) uses a microcomputer as the source and an output device, such as a display terminal, as the acceptor. $\overline{\mathrm{ACK\ X}}$ is a timing signal from the output device that acknowledges the acceptance of data.* The microcomputer generates timing signal $\overline{\mathrm{WR\ X}}$ to output data to the buffer. Both the normal (Q) and complementary ($\overline{Q}$) outputs from the semaphore are shown. A logic 0 condition for $\overline{\mathrm{ACK\ X}}$ clears the semaphore, while a positive-edge transition in $\overline{\mathrm{WR\ X}}$ sets the semaphore. As a summary of events, output data are accepted by the output device (acceptor) and acknowledged by the $\overline{\mathrm{ACK\ X}}$ signal; the

*P. R. Rony, "Interfacing Fundamentals: A Comparison of Block Diagrams for I/O Techniques," *Computer Design*, Feb 1980, pp 175-177

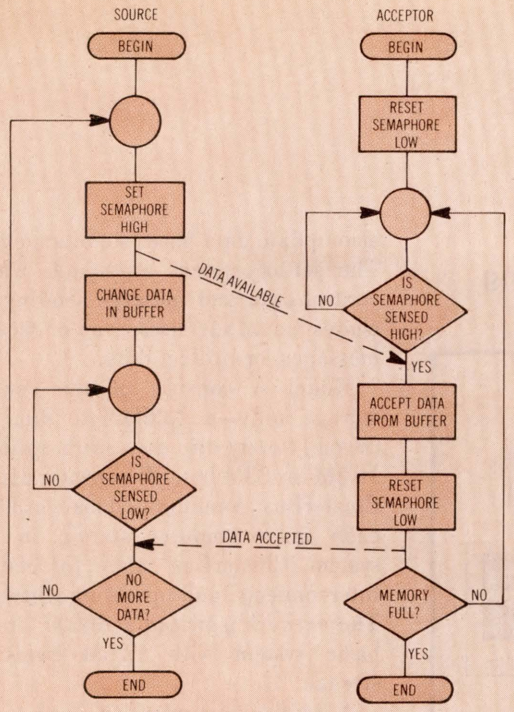


Fig 1 Flowcharts for source and acceptor. Communication between source and acceptor is shown by dotted lines, which represent two output states of single semaphore

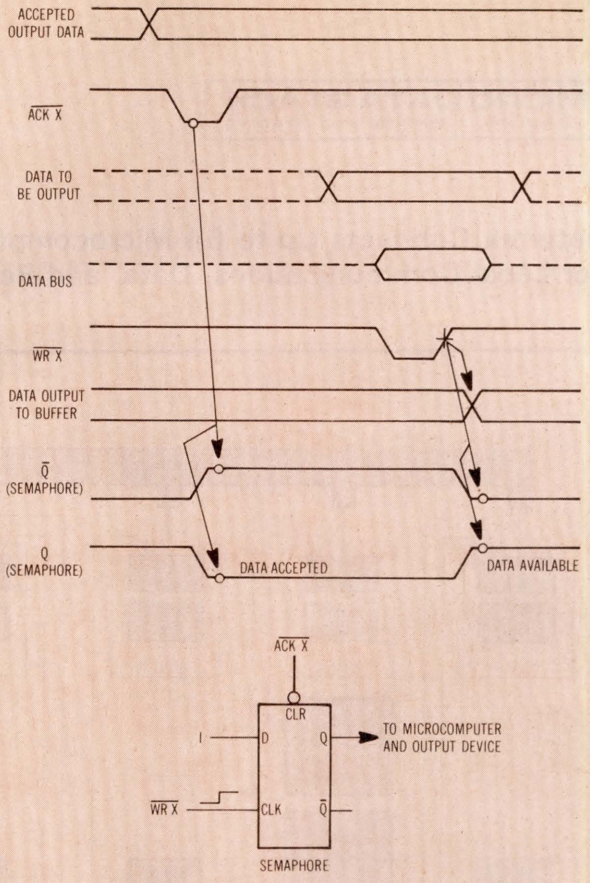


Fig 3 Conditional output with semaphore. Sequence of timing signals and data transfers are demonstrated by timing diagrams for microcomputer output using semaphore

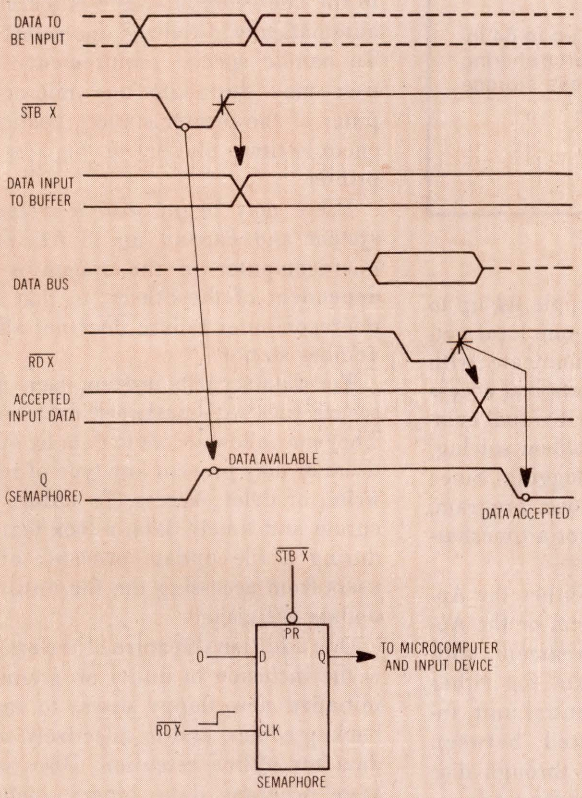


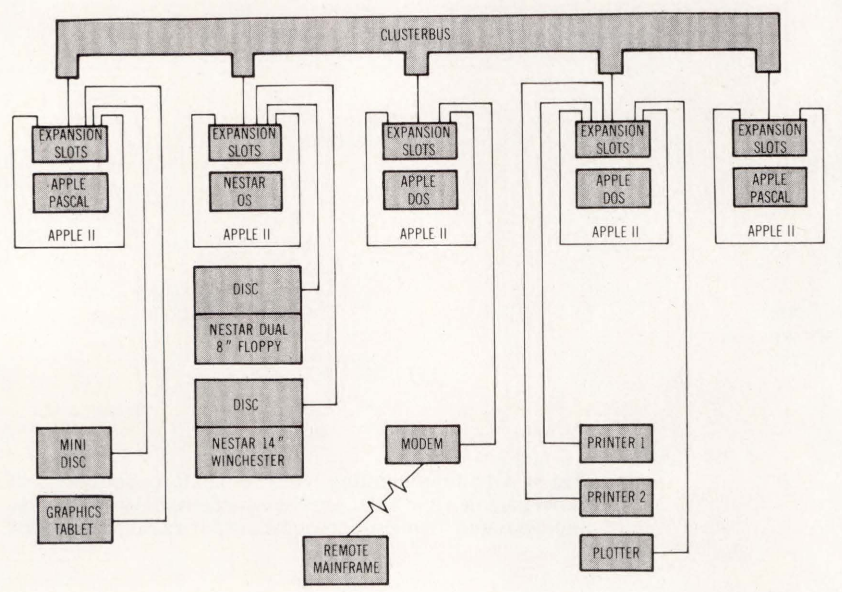
Fig 2 Conditional input with semaphore. Timing diagrams demonstrate sequence of timing signals and data transfers for microcomputer input using semaphore shown

semaphore is reset low; the microcomputer detects the acceptance of output data, and later selects new data to be output, enables the data bus to permit the output of data, sets the semaphore high to indicate that the buffer is full, and finally outputs the new data to the buffer.

Clearly, a semaphore synchronizes data transfer between a microcomputer and an input/output (I/O) device; each knows when the other has acted. In Fig 2, the input device (source) does not input new data to the buffer until the semaphore is reset. The microcomputer (acceptor) does not accept data from the buffer until the semaphore becomes set. In Fig 3, the microcomputer, as source, does not output new data to the buffer until the semaphore is reset. With both cases, the acceptor—the microcomputer and output device, respectively—does not acquire data from the buffer until the semaphore becomes set. In these Figures, only the source can set the semaphore and only the acceptor can reset it, but both can test it.

Integrated circuits (ICs) that exhibit conditional I/O typically present the semaphore output bit both as an internal status register bit, to be input and tested by the central processing unit, and as an external output pin, to be connected to the I/O device. The timing diagrams for individual ICs may differ somewhat from those shown in Figs 2 and 3, but the principle remains the same. For users interested in experimenting with this type of I/O technique, an 8255 programmable peripheral interface chip is recommended as a buffer between two 8-bit microcomputers.

Network Connects Up to 64 Microcomputers For Local Communications, Data, and Resource Sharing



Nestar's Clustershared model A computer system is composed of up to 64 independent Apple II microcomputers in a local communications resource sharing network. System uses one dedicated microcomputer as central mass storage manager which connects with all user stations through ClusterBus

Hardware and software combined in the Clustershared™ microprocessor based system creates and operates a multistation local network of personal computers, capable of exchanging data and programs among stations, similar microcomputer clusters, shared peripherals, or remote mainframes. Nestar Systems, Inc, 430 Sherman Ave, Palo Alto, CA 94306, has designed the Cluster/One, model A for the Apple II microcomputer, as a high performance alternative to having separate discs and other peripherals on each microcomputer in a system. It adds local networking and resource sharing features, with communications capabilities, data file access, and security features.

Based on the Apple II computer as the host controller at each station, the system will support 64 Apple IIs, up to 1000 ft (305 m) away, in one local network. Users may communicate with one another and share data and access files, while leaving the individual computer free to handle problem solving, data storage, and data logging. Since each computer runs its own program, the clustered system is not a timesharing system.

Programs execute in either the Apple Disk Operating System or the Apple Pascal System environment, with programs, files, and data for either system residing in the central unit. Information is transmitted between machines without going through disc files and without the need for modems. All stations share access to private data or to a common read only library of programs and data; all stations can also update data bases simultaneously. The set of system commands which control data and message sending includes mount for discs, send or receive messages, or protect data.

Model A consists of the central storage unit—a 1.26M-byte dual 8" (20-cm) floppy disc drive with optional 16.5M- or 33M-byte Winchester disc, a ClusterBus communications card for each microcomputer station in the system, ClusterBus cables for station interconnects, and operating software. The network is priced at $6000 for the basic system with 1.26M bytes of storage.

A $400 communication card is required for each user station; these cards contain 2k bytes of ROM, 1k bytes of RAM, and all bus electronics. Compatible with standard Apple interface cards, including those for mini discs, serial and parallel printers, modems, sound, and graphics tablets, the card plugs into any of the peripheral connectors inside the microcomputer. It appears as a mini disc controller card to the microcomputer and is therefore automatically initialized upon start up. To handle special requirements, the user may designate one microcomputer as the printer station, hosting a check writer, plotter, or high speed printer.

Users may begin with a 3-station system and expand up to 64. Each microcomputer in the system is independent of the others, so that one microcomputer failure does not affect another station.

For data security, system users may secure files with password protection. They may allow access to data by other users or may prevent any type of read, write, or delete access. To ensure accurate and timely data, a lock feature during a file update prevents other users from accessing the file until the update is finished.

One additional feature of the system is the inclusion of utility programs to initialize new floppy discs, to make backup copies, and to selectively copy data for offline retention. Discs may store program, data, binary, picture, and either random access or sequential text files.

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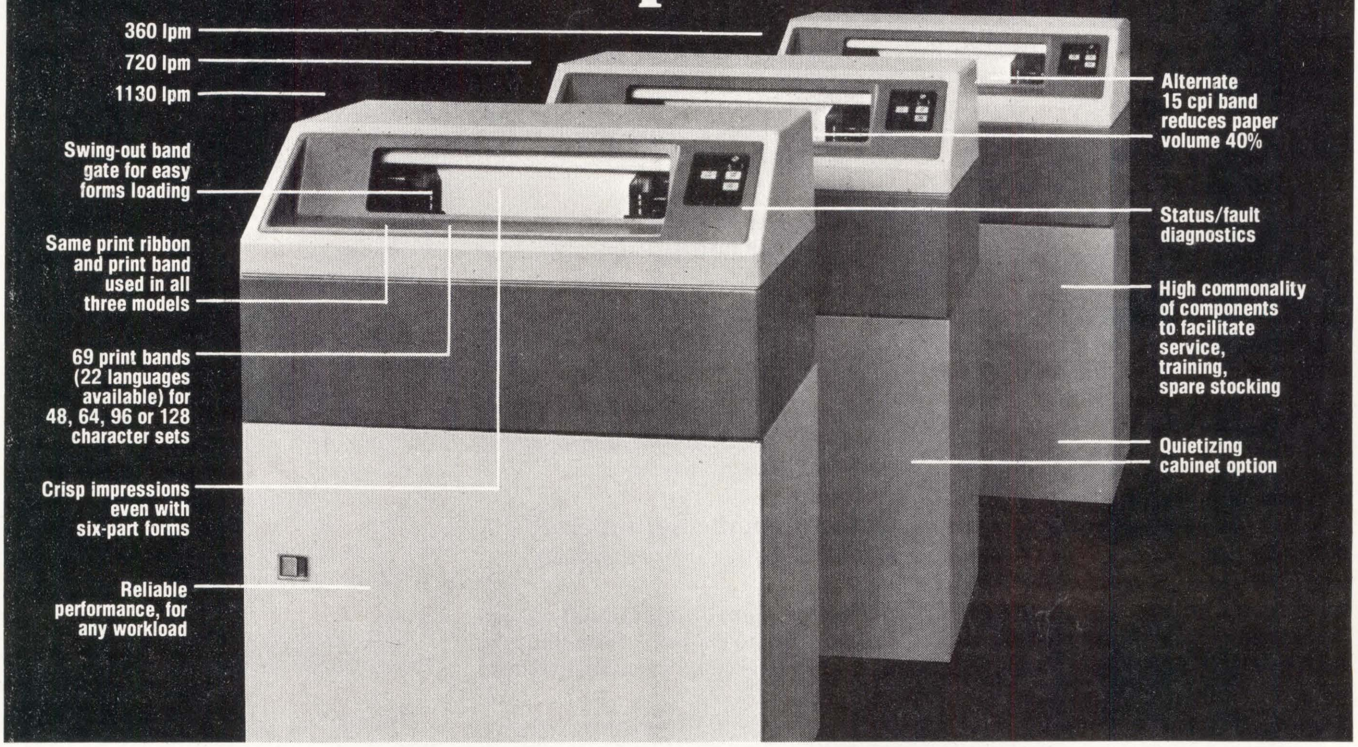

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Richard Burt, Product Sales Manager
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CONTROL DATA CORPORATION

Addressing society's major needs

CIRCLE 86 ON INQUIRY CARD

Development System Advances Design Of Microcomputers

EXORmacs, a modular development system, supports the 16-bit capability of the MC6800 and anticipates requirements of the next generation 32-bit machines. The basic chassis houses a switching power supply, cooling fans, and front panel controls. Holding up to 15 modules, the internal card cage contains four in the basic system. The remaining slots facilitate expansion through separate, compatible VERSAbus modules.

Constituent parts of the system are the chassis and functional modules, intelligent CRT terminal, 132-column printer, and 1M-byte dual-drive floppy disc mechanism. Software complements are an advanced operating system, symbolic debug assembler/editor, and Pascal compiler.

Containing the MC68000 chip, the MPU module includes the clock system, a 4-segment memory management unit, and firmware diagnostics. The memory management unit permits the system to allocate memory under control of the operating system and provides multitasking operation which speeds program development by allowing concurrent tasks. The debug module houses MACSbug firmware, primary and secondary map switching logic, bus arbitration logic, a parallel printer port, RS-232 terminal port, and downline load RS-232 host port.

The intelligent floppy disc controller module uses an MC6801 microprocessor to handle data requests from the M68000 system and to provide self-contained module diagnostics for the floppy disc. Multiprocessing increases system performance for more efficient allocation of the user's time.

The dynamic 128k bytes of RAM includes byte parity, which is read during memory access, providing the MC68000 MPU with soft error status. The user can set base address through switch inputs. Additional RAM modules result in over 1M bytes of directly addressable resident memory.

VERSAdos is a multitasking, multiprogramming operating system, which supports sequential and random record access. Programs execute in dynamically assigned, variable length segments. Separate memory segments hold instructions and data. Communication between independent programs or nodes of a distributed system occurs through a process to process facility.

The realtime executive is responsible for task services, memory management, intertask communication, system interrupts, and exception monitor facilities. The I/O subsystem supports device independence, logical I/O, overlapped computation, and physical I/O. Additional device drivers do not impact the central core of the operating system.

A file management system supports contiguous, variable length, and indexed file structures. Other features are disc and file protection, temporary files, checkpoint capability, proceed I/O, shared file access, and dynamic file access permission.

Software complements offered by Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, are comprised of a resident assembler, linkage editor, text editor, debug program, and Pascal compiler. Containing macro and conditional assembly capabilities, the assembler translates source statements to relocatable machine code, assigns instruction and data storage locations, performs auxiliary assembler action, and produces an optional cross reference listing.

Two or more separately compiled object units merged by the linkage editor produce a loadable object module file. In the process, it determines segment attributes, calculates address space, searches libraries, relocates object code, issues error messages, and prints a report with a module map, table of externally defined symbols, and unresolved or duplicate symbols.

Running under the operating system, the CRT oriented text editor creates and modifies source programs. Command and page editing are performed using the cursor, control characters, and function keys of the EXORterm 155 CRT terminal to insert, delete, or change lines and characters.

Programs for the 68000 with source code written in any Motorola-provided assembly or high level language are debugged by SYMbug. The debug program utilized with USE (User System

Evaluator) hardware handles software and hardware debugging in symbolic terminology. Capabilities allow examination, insertion, and modification of program elements; use of breakpoints; trace execution; program and data search; and creation of macro commands.

The Pascal compiler simplifies program writing. Extensions consist of address specification for variables, alphanumeric labels, string types, exit, runtime error checking, runtime file assignment, nondecimal integers, and separate compilation and linking.

Circle 411 on Inquiry Card

Large Read Only Memory Highlights Single-Chip Microcomputer

An advanced 8-bit general purpose microcomputer, μPD7801 contains 4k bytes of RAM, coupled with 128 bytes of onchip RAM and two 8-byte register banks. Using an 8080A compatible bus, the device can access 60k bytes of external memory.

A 64-pin quad-inline package houses the microcomputer. In addition, it offers 48 I/O lines and five vectored interrupts. The 5-V NMOS device operates with a 2-μs instruction time. Combined 8080A, Z80A, and μCOM-4 instructions comprise the 125-instruction set, which provides block moves and nine addressing modes.

NEC Microcomputers, Inc, 173 Worcester St, Wellesley, MA 02181, has accounted for software and hardware development as well. Cross assemblers run on the company's PDA-80 and Intel's MDS-200 series development systems. The ROMless μPD7800 and the EVAKIT-87, a standalone development board with debug and trace capability, perform hardware development.

Circle 412 on Inquiry Card

ROM Simulation Module Tests Program Prior To Final P/ROM Burn-in

With the P/ROM emulation personality module for the IM1010 P/ROM programming system, users can test and change programs before committing them to P/ROM, thus saving time and speeding product development. Move, list, verify, insert, delete, search, checksum, fill, and invert are the editing functions that enable program debugging.

The ROSI (ROM simulation) module has a 4k x 8 RAM for emulation; one 2732, two 2716s, or four 2708s are possibilities that can be emulated. This RAM also allows P/ROM addresses to line up with RAM addresses. Standard RAM access time is 300 ns; faster RAMs can be used for bipolar P/ROM emulation. A switch relocates the first address of the emulation P/ROM on any 32-byte boundary of the simulation module.

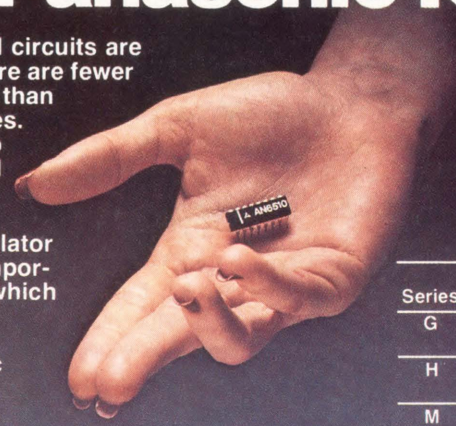
Emulation occurs with any 4- or 8-bit P/ROM or ROM starting with 32 x 8, up to 4k x 8 organizations. Either standard IM1010 socket adapters or ROSI special socket adapters developed by International Microsystems, Inc, 11554 C Ave, Auburn, CA 95603, can be made to emulate the necessary P/ROM or ROM pinout.

Circle 413 on Inquiry Card

ROSI ROM simulation module located in lower left corner of International Microsystems' 1010 programmer debugs programs before they are committed to P/ROM. Module is complete with 24-pin cable and standard socket adapter

There's a little something in this Panasonic switcher the other guys wish they had:

a Panasonic IC



To begin with, switchers with IC control circuits are reliable switchers. Reliable because there are fewer components – and fewer connections – than power supplies made with only discretes.

But Panasonic switchers don't stop there. We use our own IC, designed and built for us by our parent company. It holds pulse width modulation, operational amplifier, reference voltage, oscillator and several protective circuits. More important, it permits us to design switchers which operate effectively in the lower power ranges.

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Series	Type	Power Ratings (W)	Output Voltages (VDC)
G	Single-input	25, 50, 100, 150	+5 to +24
H	Dual-input	125, 250, 375	+2 to +24
M	Triple-output	40, 70, 120	Combinations from −15 to +15
E	Single-input	25, 50, 100, 150	+5 to +24

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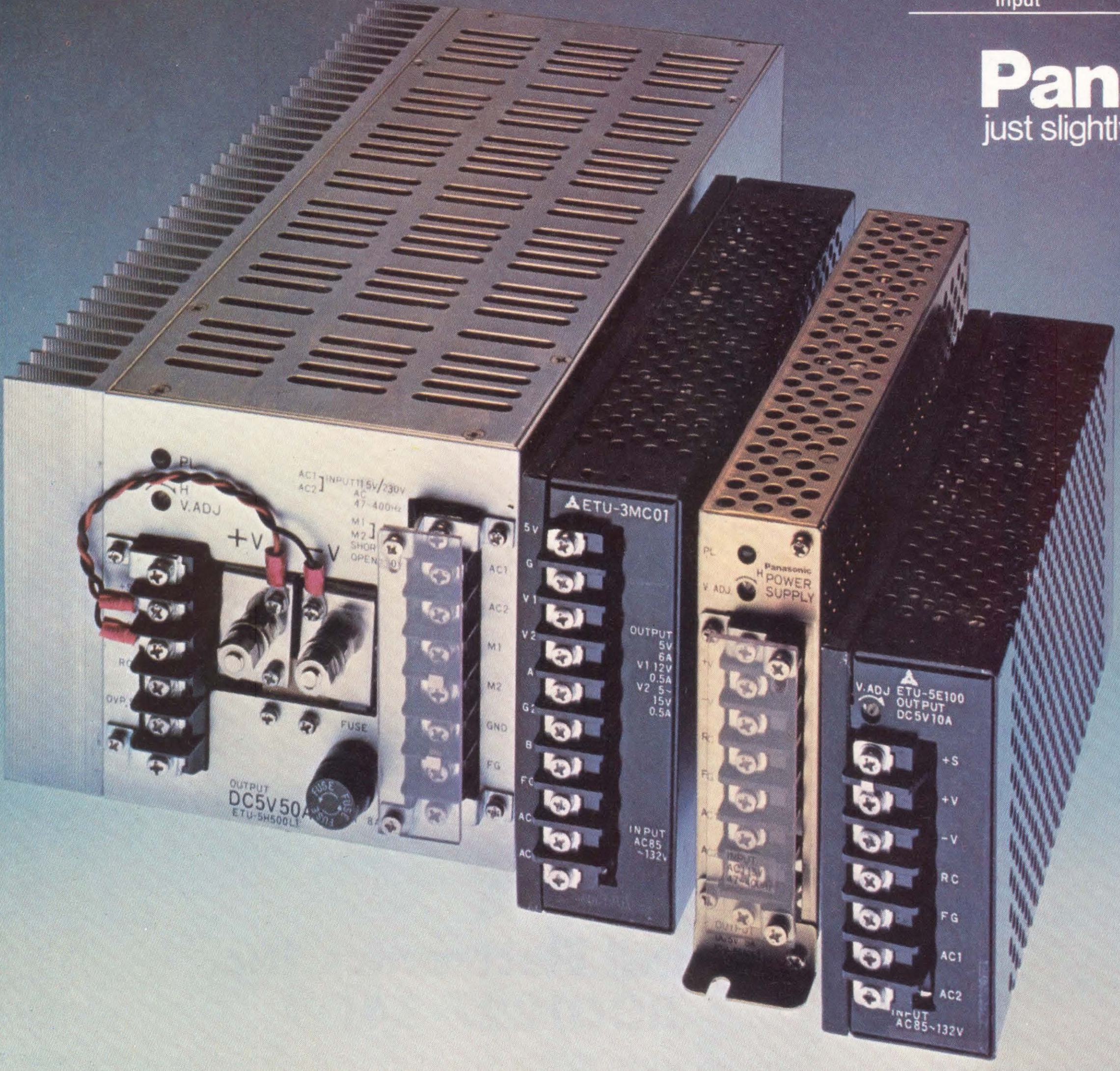
just slightly ahead of our time



CIRCLE 91 ON INQUIRY CARD

Bus Converter Offers Dual-Purpose μComputer System Operation

The Qniverter™ bus converter operates in either of two ways with Digital Equipment Corp PDP-11 and LSI-11 systems. With the quad-width board, a PDP-11 Unibus system can access LSI-11 compatible controllers and memories, or an LSI-11, -11/2, -11/23, PDP-11/03, or -11/23 system can access Unibus compatible controllers and memories.

The board installs into a quad slot of the LSI-11 backplane, remaining software transparent to the host computer. Either type of system is then equipped with two bus structures—the Unibus and the Q-bus. Any diagnostic appropriate to the system devices may be used to verify system operation.

The memories and controllers may reside on both the Unibus and Q-bus. The result is that available Unibus devices are available for the LSI-11 systems, and inexpensive LSI-11 devices can be used in Unibus systems.

Able Computer, 1751 Langley Ave, Irvine, CA 92714, has devised the converter to support such LSI-11/23 features as 4-level interrupt structure, memory parity, and full 256k-byte addressing. Extended bus load capabilities allow the addition of 19 Unibus loads to an LSI-11 system or a Q-bus drive capability to a Unibus system.

Circle 414 on Inquiry Card

Lower Cost Processors Change Design and Memory Packaging

Additions to the current GA-220 offering of General Automation, 1055 South East St, Anaheim, CA 92803, have reduced price and increased performance by using HYPAK memory technology. The resulting set of three systems gives users a range of memory configurations, with the potential for inexpensive growth to meet increasing application complexities.

The GA-230 processor, costing 30% less than the -220, contains a CPU and 128k-byte memory service module with full byte parity. The chassis has a built-in power supply. Autoload with an interactive console interface, as well as RS-232 and current loop serial I/O interface, is also included.

Increased performance and 10% price reduction over -220 systems are obtained from the compact -240. A CPU with extended instruction set, 128k-byte memory with 22-bit error correction capability, memory service module, RS-232 and current loop serial I/O interface, autoload with interactive system console, and chassis with built-in power supply comprise the microcomputer. The memory is expandable to 512k bytes on a single board. Jumbo configurations of these two systems offer more I/O slots and a larger rack-mounting power supply.

Circle 415 on Inquiry Card

Intelligent Cartridge Disc Controller Stores 80M Bytes Online

Resident on a single Multibus compatible board, model 410 can control up to four disc drives with a Diablo 44B interface. A single 50-conductor flat cable connects to the first disc drive via a latching connector at the PC board edge; the other drives connect to this first drive via a daisy chain cable.

A 16-bit 2900 based bipolar microcomputer provides operating and diagnostic commands. Use of channel control technique allows command chaining and concurrent processor and controller operation. The operating system issues disc commands by setting up the command I/O parameter block in system memory. Programming the controller's onboard registers with the block address initiates a command; the controller then reads the command block from system memory by direct memory access. Extensive commands include a pack format, implied seek, and overlap seeks. Some command chaining occurs for complex operations without operating system intervention between commands.

Other features that Xylogics, Inc, 42 Third Ave, Burlington, MA 01803, has incorporated are 20-bit Multibus addressing, 8- or 16-bit I/O addressing, and support of bus and nonbus vectored interrupts. In addition, the controller handles 8- and 16-bit data transfers simultaneously.

Circle 416 on Inquiry Card

Intelligent Controllers Interface Discs to Two Bus Structures

Microcomputers based on either the Multibus or IEEE-488 can use the MSC-1086 and -1088 controllers, respectively, to add extra storage economically. Three versions of the first board are the -1086A, which controls up to four 58M-byte SA4000 Winchester drives; -1086B, connecting four SA850 or equivalent floppy disc drives with four SA4000 drives; and -1086C, handling four SA4000 plus a 3M HCD-75, 70M-byte tape unit. Based on a bipolar microprocessor, all members of the MSC-1080 series control multiple drives that include the 14.5M-byte SA4004, the 28M-byte SA4008, and 58M-byte SA4100.

Controllers contain control and maintainability features, along with generally required formatting and operating functions. They can be used in OEM systems or in floppy disc replacement applications with simple modifications to system software.

Features are command chaining, error checking and correction, write protection, automatic head and cylinder switching, relative addressing, automatic seek to alternate tracks, implied overlapped seeks, variable interleave, disc copy commands, and search. In addition, the controllers can verify positioning for the CPU, test themselves, and buffer data transfers to eliminate overrun and underrun programs. They also perform extended microdiagnostics.

High level commands unburden the host microprocessor and simplify program development. Two techniques are offered for software compatability: the high level commands can be used to write disc operating tasks, or as an option in volume applications. Microcomputer Systems Corp, 432 Lakeside Dr, Sunnyvale, CA 94086, supplies software integration versions with custom firmware for the onboard bipolar microprocessor.

Circle 417 on Inquiry Card

Portable Microcomputer Moves Computing Power To Business Sites

Easy to use Findex system employs BASIC language operating system for handling general business, as well as engineering, functions. Small unit stores 128k bytes of data in magnetic bubble memory. Printer and plasma display round out the package

A line of general purpose microcomputers combine the power of a central computer with the size and portability of a terminal for individual applications in locations that were previously considered impractical. Business, scientific, engineering, and design computations are accomodated. Expansion for multiuse applications is handled by adding more units as interactive, intelligent terminals; each offers 49k bytes of RAM for scratchpad computing, independent of the central computer.

The major model, system #128TD, has 128k bytes of magnetic bubble memory for mass storage, expandable in 128k-byte increments. With no mechanical moving parts, the memory retains stored information even if system power is disconnected. This type of storage is also practical in process control environments.

Findex, Inc, 1625 W Olympic Blvd, Suite 808, Los Angeles, CA 90015, offers System #100TD as a lower cost alternative, with 200k bytes of mass storage in a mini-floppy disc housed inside the computer case. Floppy storage is expandable to 400k bytes. Built-in memory of the two systems is the same: 48k bytes of dynamic RAM and 1k bytes of static RAM, expandable to over 2M bytes, plus 8k bytes of ROM which expands to 32k. Interfacing external disc drives provides added megabytes of mass storage.

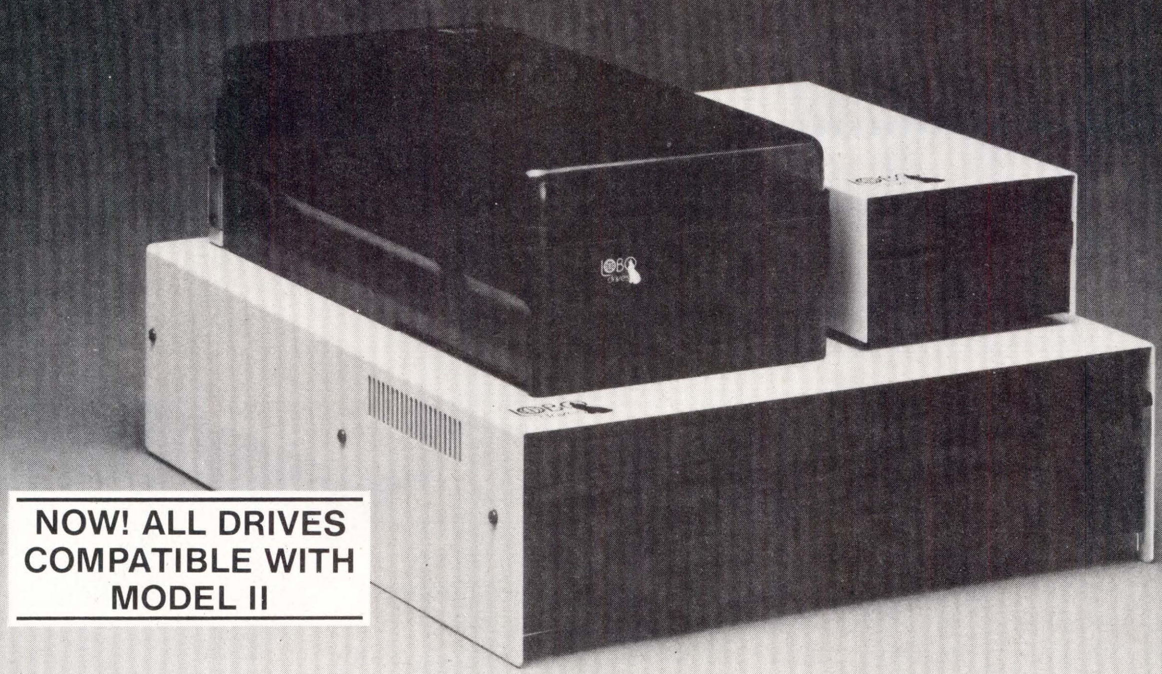
Serial, parallel I/O, and S-100 capability allow interfacing with peripheral units ranging from external printers and cassette recorders to larger computers. An integral 80/132-column, plain paper printer and flat upper/lower case alphanumeric, gas plasma display complete the unit. The scrolling display provides six rows of 40 dot matrix characters. The field of view can be scanned over any data base which eliminates the need for a large screen.

Programmed in Business BASIC, the computer also supports a FORTRAN and COBOL compiler. A comprehensive file management capability eliminates sorting and supports a large library of business application programs.

Circle 418 on Inquiry Card

See page 99

NEW FROM LOBO:

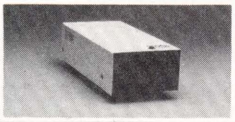


An Entire Family of Disk Drives for APPLE, TRS-80*, and S-100 Computers

Only LOBO DRIVES offers you an entire family of fully-compatible disk drives to select from. Whatever computer you're using, APPLE, TRS-80, or S-100, you can add a LOBO drive now, with the peace-of-mind of knowing there's a whole family of drives available when you're ready to expand.

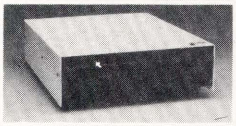
And every drive you order comes complete with chassis and high reliability power supply. Each drive is 100% calibrated, burned-in, and performance tested on either an APPLE, TRS-80, or S-100 computer before it's shipped. We are so proud of our drives . . . our quality, reliability, and performance, that we back-up every drive with a one year, 100% parts/labor warranty.

400 SERIES FLOPPY DISK DRIVES



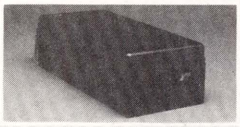
Meet our low-cost 5.25-inch mini drive that records data in either hard or soft sectored format. It is available in single or double density configurations, with a total storage capacity of 220K bytes.

800/801 SERIES FLOPPY DISK DRIVES



Here is our dual 8-inch Floppy disk memory unit. It records and retrieves data on standard 8-inch diskettes to provide 800K bytes of data storage unformatted, or 512K bytes in IBM format per drive. It is also available with double-sided, double-density capabilities, for a maximum storage capacity of 1.6 Megabytes.

7000 SERIES HARD DISK DRIVES



The latest member of our drive family, the Series 7000 is an 8-inch, 10 Megabyte Winchester Technology, hard disk drive. It is fully hardware/software compatible and comes complete with disk controller. Now you can have the convenience, speed, reliability, and all the storage capacity you need.

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☐ 5 1/4-in. Floppy drive
☐ 8-in. Winchester hard disk, 10 Mbyte drive
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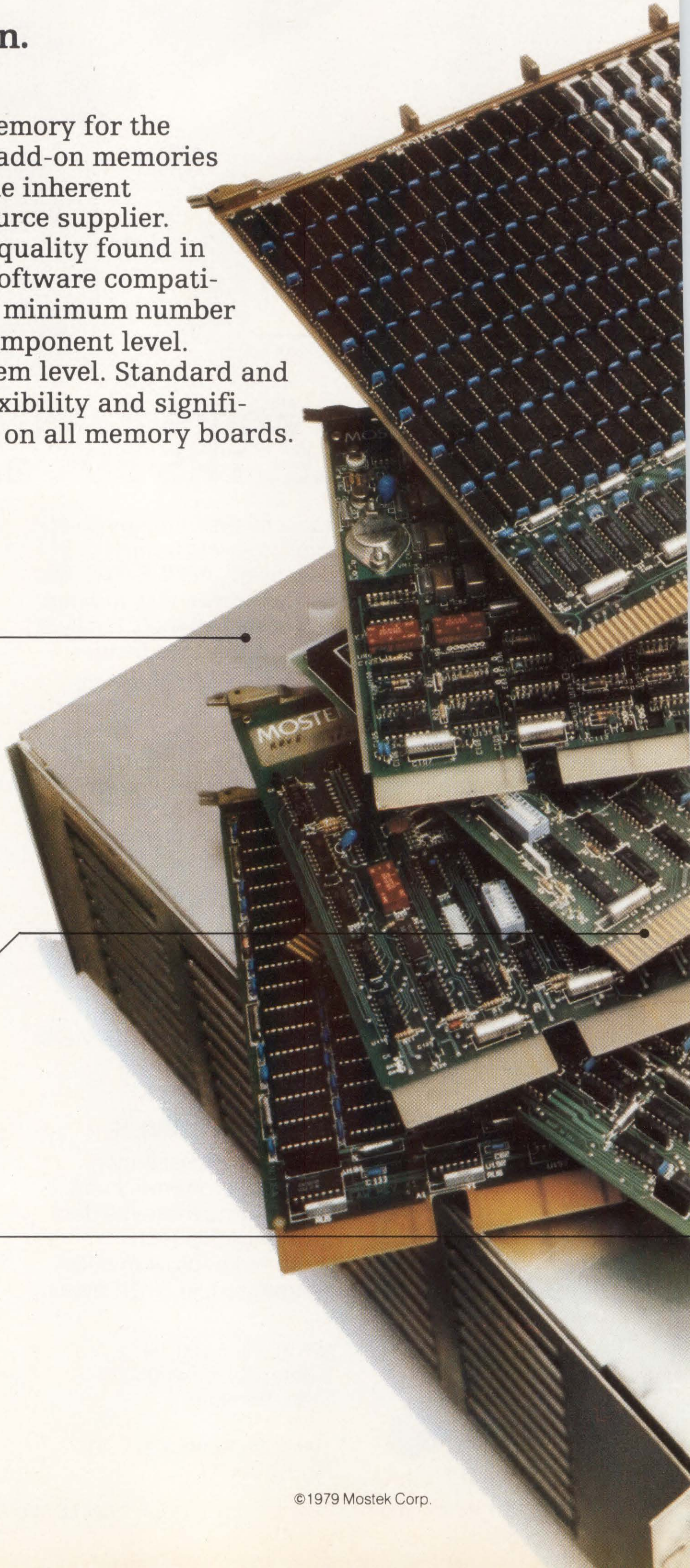
CIRCLE 180 ON INQUIRY CARD

Full DEC*

Introducing the Mostek VAX Add-In. Now we have all the cards.

With the addition of our 256K byte add-in memory for the VAX-11/780, we now have a full line of add-in, add-on memories for DEC minicomputers. Your advantage? All the inherent advantages of dealing with a reliable single source supplier.

The new Mostek VAX incorporates the same quality found in all our memory systems: Total hardware and software compatibility. High density for maximum capacity in a minimum number of card slots. Burn-in and stress tests at the component level. Pre-burn, burn and post-burn tests at the system level. Standard and optional system features for greater system flexibility and significant cost savings. And a full one-year warranty on all memory boards.



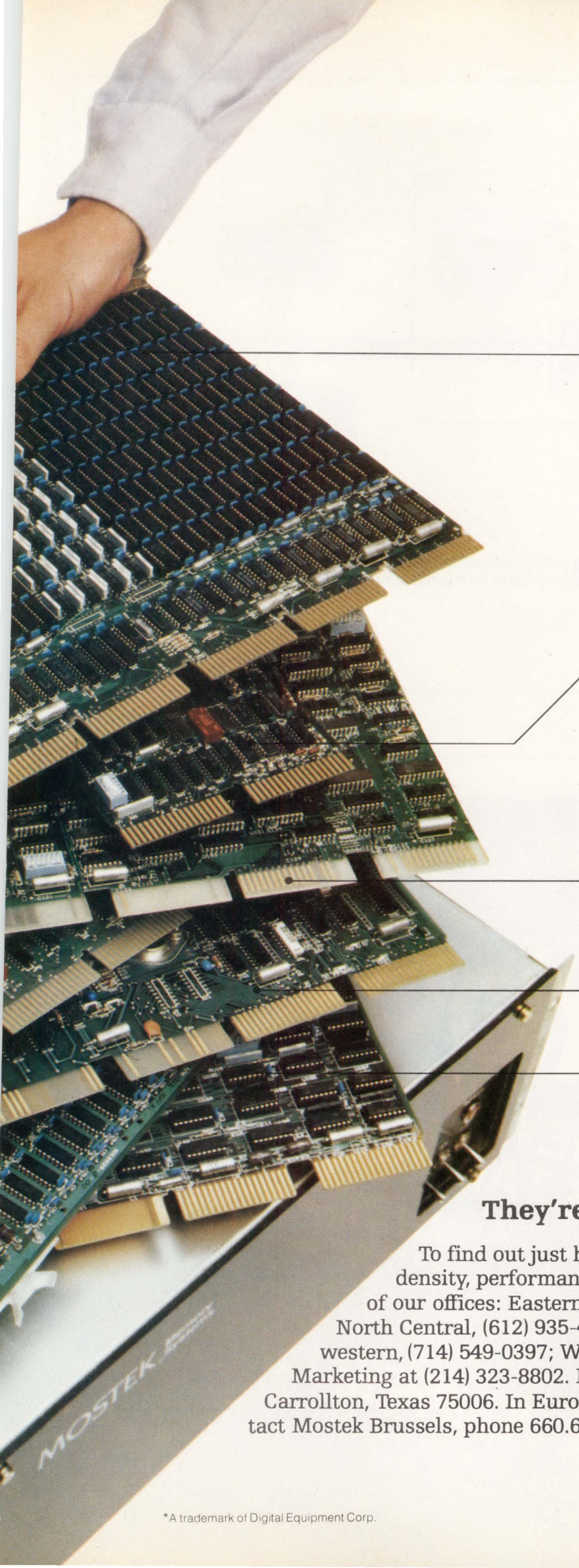
PDP-11/70*

MK 8601
Total capacity of two megabytes in a 7″ chassis. 256KB or 512KB increments with ECC standard. Can operate in the serial and interleave modes simultaneously. Maintenance program available.

PDP-8*

MK 8009 A1"X" (PDP-8A)
16K, 32K, 48K, or 64K words x 12 bits. Compatible with DEC memory management to extend total capacity to 128K x 12 with just two cards.

MK 8009 A0"X" (PDP-8E,F,M)
16K or 32K words x 12 bits. Single +5V supply with synchronous "hidden" refresh control.



VAX-11/780*

MK 8016
256KB single board capacity (32K words x 72 bits with 64 bits data and 8 bits ECC). Totally hardware and software compatible.

LSI-11/2* or LSI-11/23*

MK 8005 (PDP-11/03,* 23)
8K, 16K, or 32K words x 18 bits with optional byte parity generation and checking.

PDP-11/04* through 60

MK 8011
16K, 32K, or 64K words x 18 bits with on-board parity generation and checking.

MK 8001
16K, 32K or 64K words x 18 bits with parity standard.

MK 8012
64K x 18, 96K x 18, or 128K words x 18 bits with parity standard.

They're available out of stock.

To find out just how well Mostek Memory Systems stack up in density, performance, reliability, availability and price, call one of our offices: Eastern, (201) 842-5100; Northeastern, (617) 256-1500; North Central, (612) 935-4020; South Central, (214) 386-9141; Southwestern, (714) 549-0397; Western, (408) 287-5081; or Memory Systems Marketing at (214) 323-8802. Mostek Corporation, 1215 West Crosby Road, Carrollton, Texas 75006. In Europe, contact Mostek Brussels, phone 660.69.24.

MOSTEK® Memory Systems

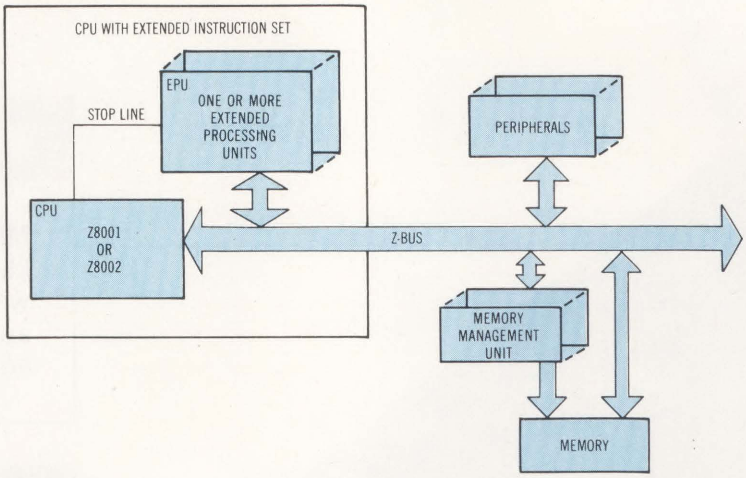
CIRCLE 181 ON INQUIRY CARD

*A trademark of Digital Equipment Corp.

Extended Processing Architecture Specializes 16-Bit Microprocessor

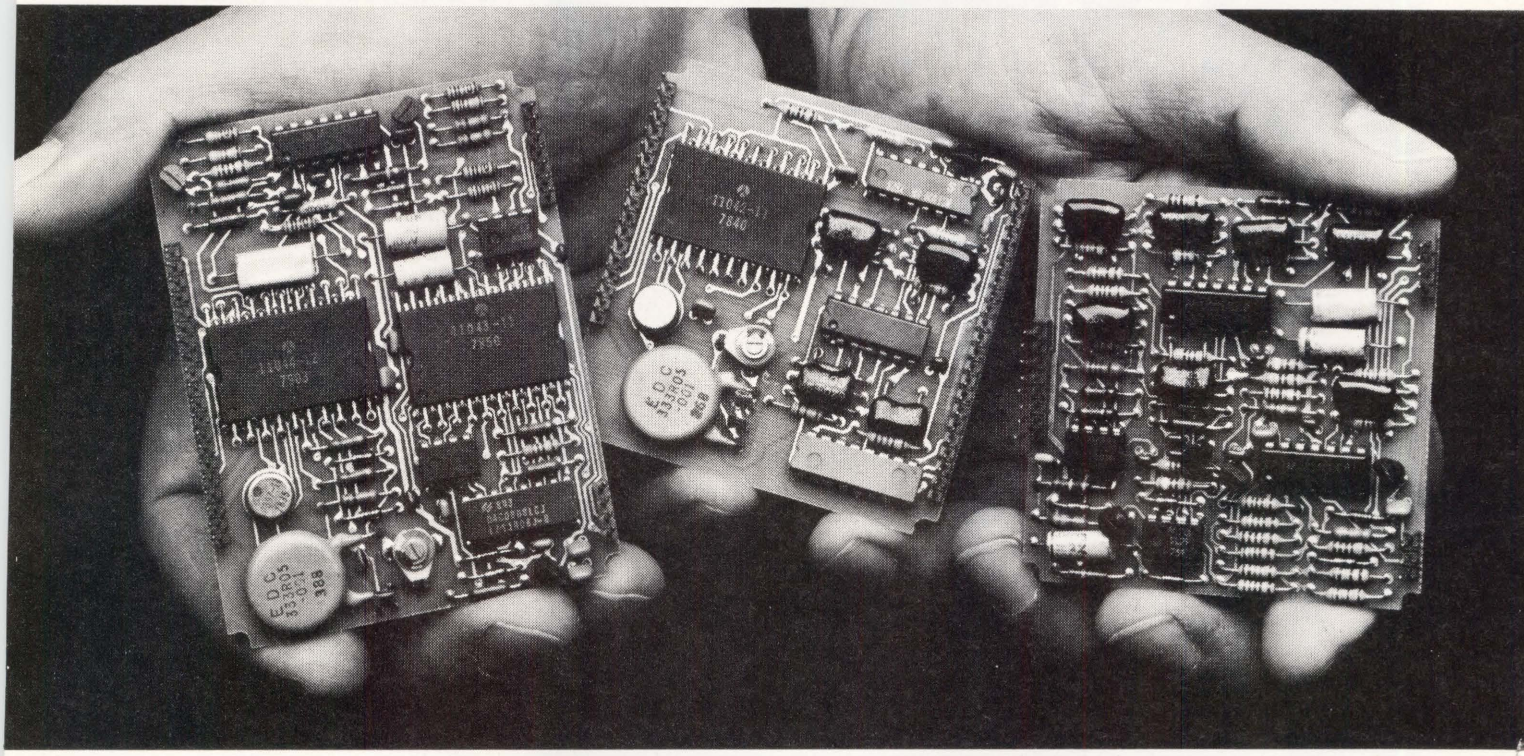
An architectural feature uses special purpose processors to extend the instruction set of the Z8000 microprocessor. Four types of instructions are EPU (extended processing unit) internal operations, data transfers between memory and EPU, data transfers between EPU and the Z8000 CPU, and status transfers between EPU and Z8000 status flags.

Manipulating data types up to 16 words long, these instructions are executed in the stream along with other Z8000 instructions. The set is expanded by more than 256 instructions. Six of the Z8000 operation codes are reserved for the extended instructions. Five main CPU address modes transfer data to and from an EPU.



System configuration shows Zilog's Z8000 CPU employing one or more extended processing units to handle time consuming CPU tasks more efficiently

R24. The first 2400 bps modular modem.



Rockwell's compact MOS-LSI modem gives new physical design freedom.

Micro power

Rockwell's R24 Modem is the most compact 2400 bps MOS-LSI modem available today. Its small size and modularity give designers a whole new form factor flexibility. Requiring only 25 square inches of system area, the R24 is ideal for terminals and communications equipment.

The R24 provides functional flexibility also. Of its 3 modules, one is the transmitter, two the receiver. Terminal designers can offer transmit-only or receive-only options. And, the R24 is Bell 201 B/C and CCITT V.26 and V.26 bis compatible.

With its major functions in LSI circuits, the R24 is solid-state reliable and economical. It can be configured for operation on either leased lines or the general switched network. And, each low-profile module can be plugged into standard connectors or wave soldered onto system PC boards.

A new generation of modems from the company that's delivered more high-speed modems than anyone in the world. That's Rockwell Micropower!

For more information, contact Modem Marketing, Electronic Devices Division, Rockwell International, P.O. Box 3669, RC 55, Anaheim, California 92803. (714) 632-5535.

Rockwell International

...where science gets down to business

CIRCLE 183 ON INQUIRY CARD

Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014, is adapting the architecture to Z8001 and Z8002 microprocessors after mid-1980; it will use Z8000 processors, EPUs, and extended instructions. Each EPU operates simultaneously with and independently of other EPUs in a system.

Specialized tasks such as floating point arithmetic, database search and maintenance operations, and network interfaces that consume considerable CPU time benefit from the EPUs. The CPU moves data into and out of the EPU's internal registers, and indicates the operations that the EPU should perform.

Circle 419 on Inquiry Card

8-Bit Microcomputer For Small Business Uses Operates At 7 MHz

Computing speed of the Centurion system is 7 MHz due to hardware enhancements incorporated by Artec Electronics, Inc, 605 Old County Rd, San Carlos, CA 94070. Built around the Intel 5-MHz 8085A-2 microprocessor, the system has a higher overall speed due to the floating point math chip that handles all number crunching calculations. The higher speed is achieved in applications where the computer performs many relatively simple computations.

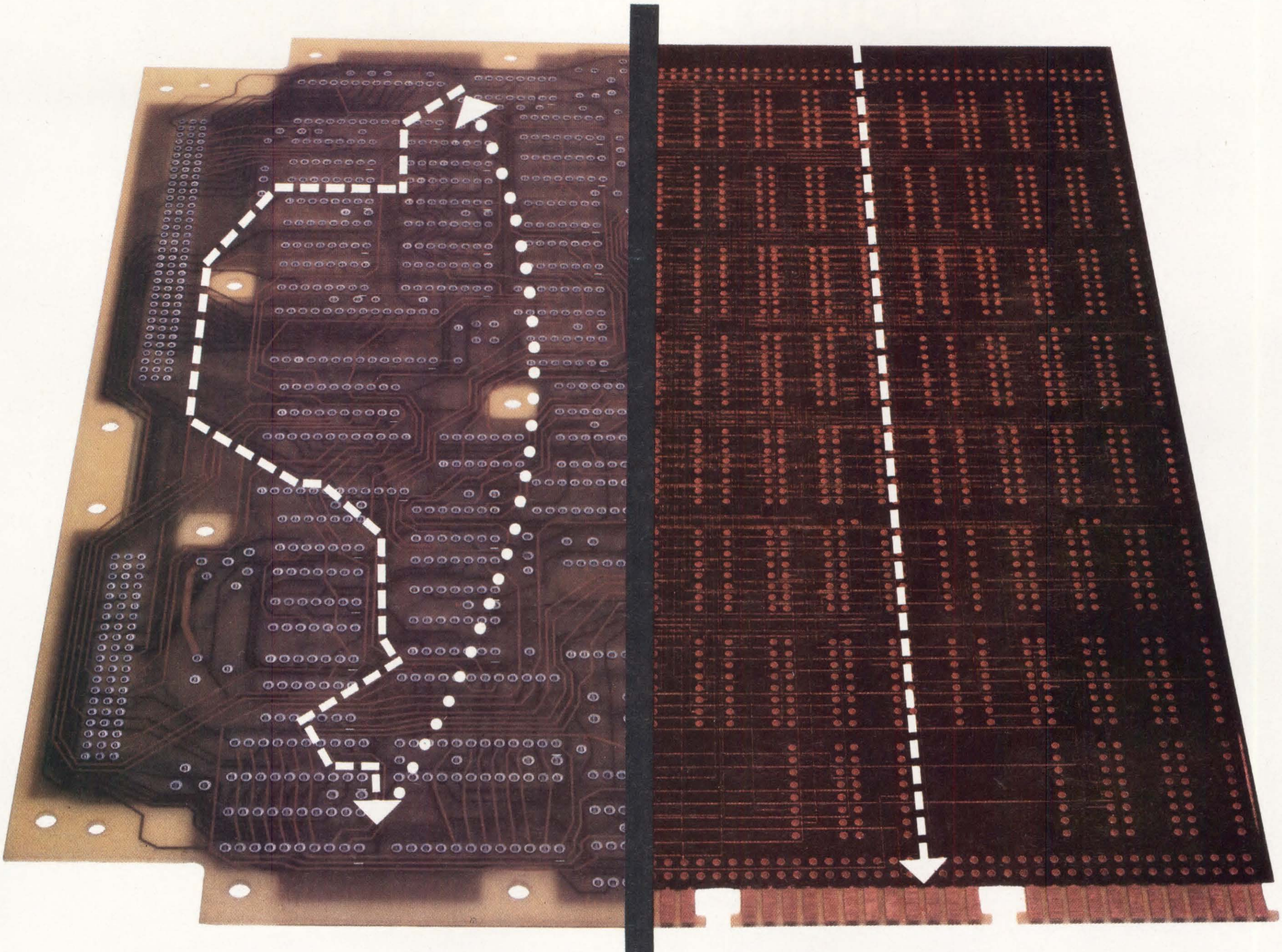
Components are 16k of internal P/ROM, 64k of RAM, a floppy disc controller, and CP/M operating system. Built on the company's shielded motherboard, it operates with a CRT terminal and up to four single-sided, double-density, 8" (20-cm) floppy disc drives, and is compatible with any printer having an RS-232 interface.

Three configurations offer differing packaging and peripheral options. Centurion I is a microcomputer housed in a custom enclosure with a 16-slot shielded motherboard; a Hazeltine 1500 CRT terminal and two Shugart 8" (20-cm) drives and a power supply, separately housed, are included.

A microcomputer combined with an 8-slot shielded motherboard and two 8" (20-cm) disc drives in one enclosure comprises the Centurion II. The final version, Centurion III equips the microcomputer with an 8-slot motherboard and two 5.25" (13.34-cm) disc drives in a single unit. A packaged power supply and two 8" (20-cm) drives provide an additional 1M bytes of disc storage capacity for the first two systems.

Circle 420 on Inquiry Card

The Shortest Line Between Design Points is Multiwire.

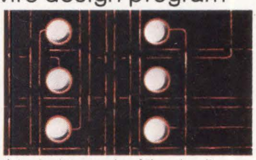


MULTILAYER

Regardless of what design technique you use — even with a computer aided system — designing multilayer PC boards can be a guessing game. Many times, in the last 5% of the routing, you find yourself up a "blind alley" and you have to go back to "start".

MULTIWIRE

With Multiwire, you can easily avoid such blind alleys . . . for design-time savings in your circuit boards. Routing is under complete computer control. All you have to do is prepare artwork for the power and ground planes, the net or "from-to" list, and a fabrication print showing component location and board configuration. The Multiwire design program takes over from there. Results: your design time is cut. And, when design changes are needed, Multiwire lets you make them . . . quickly, easily. Electrical characteristics are consistent and controllable, inspection costs are cut and production yields go up.



A typical example of the circuit density achievable with Multiwire circuit boards.

Why wait? For complete details write or call today. Multiwire, 31 Sea Cliff Avenue, Glen Cove, NY 11542. Phone (516) 448-1307.

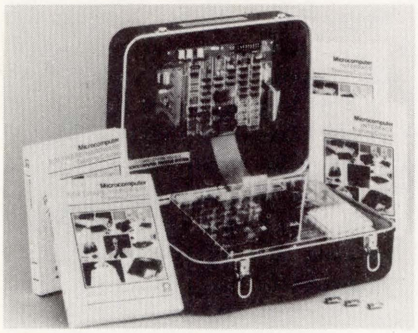
MULTIWIRE DIVISION

KOLLMORGEN CORPORATION

CIRCLE 112 ON INQUIRY CARD

Portable Microprocessor Training Lab Teaches Software And Interfacing

Mounted in a sturdy carrying case, the microprocessor training lab teaches microprocessor software and realtime interfacing with hands-on exercises. Hardware consists of an assembled and tested 8080A based microcomputer that is equipped with an integral power supply, RAM, P/ROM, programmable I/O, keyboard, display and audio cassette interface, and educational firmware monitor.



Integrated Computer Systems' kit provides hardware in portable case together with self-study manuals to solve organization's training needs for microcomputer software, hardware, and realtime interfacing

The interface training system features a 50-pin system bus connector for cabling to the microcomputer training system. Also included are multiple interval timers, programmable I/O ports, A-D and D-A converters, priority interrupt logic, and communication interfaces. An experimental parts assembly contains optical and thermal sensors, motor, and other interfacing components mounted on a PC card to facilitate experimentation.

An S-100 interconnect board contains all necessary bus buffers, sense switching, and restart circuits to plug directly into a standard S-100 bus chassis. A ribbon cable attaches to the S-100 bus connector on the training system and to the S-100 interconnect board. The instruction manual details adding 64k bytes of external memory and interfacing to such peripherals as CRT terminals, TV monitors, printers and floppy discs.

Integrated Computer Systems, Inc, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405, has developed four volumes of 20 self-training modules. Coverage is included of programming fundamentals, realtime interrupt handling, control of programmable interfacing devices, and implementation of closed loop control systems. Each module guides the user through hands-on experiments that cover the coding and execution of programs on the microcomputer, as well as interfacing hardware provided in the training lab.

Circle 421 on Inquiry Card

Dual-Height, LSI-11/2 Analog Interface Boards Have 14/16-Bit Resolution

Single-board analog interface systems having backplane and protocol compatability with Digital Equipment Corp's LSI-11/2 microcomputer offer a choice of 14- or 16-bit A-D conversion, as an outgrowth of the standard 12-bit resolution systems. Mounted on DEC standard dual-height cards, the models have expandable multiplexer inputs with either 16 single-ended or 8 differential analog input channels.

An optional software programmable gain amplifier provides a PGH option for gains of 1, 2, 4, and 8 with high level input systems and a PGL option for gains of 1, 10, 100, and 500 for low level input systems. It is the resolution/software programmable gain combination that permits the system to resolve, measure, and confirm values of minute signals which otherwise are masked by ambient system noise.

Three high level systems cover full-scale analog input ranges of 0 to 5 V, ±5 V, ±10 V, and 0 to 10 V. Data Translation, Inc, 4 Strathmore Rd, Natick, MA 01760, also announced three low level, wide range systems that accept full-scale analog inputs between 10 mV and 10 V. All six versions are extended to 14 or 16 bits, performing to 10 and 2.5 kHz, respectively.

General purpose DT2762 analog input system is a DEC ADV-11A type converter for 1- to 10-V inputs. DT2782 is a high throughput analog input system with standard DMA and optional data acquisition module types. The company's TRANSLATE-BUS™ allows direct interchange of DATAX II™ data acquisition modules with diverse performance features; pin assignment and pattern are identical, however. Also available in the grouping of high level devices is DT2781, a general purpose I/O system.

Low level offerings include the general purpose, analog input DT2764; DT2784, a high throughput analog input system with standard DMA and choice of optional high speed data acquisition modules; and the general purpose DT2785 analog I/O system for inputs between 5 mV and 10 V.

Common specifications are linearity of ±0.009/0.006% FSR, differential linearity of ±½/1 LSB, and system accuracy of ±0.02/0.01% FSR for a gain of 100 (gain error reduces to ±0.01/0.0075% FSR for a gain of 1). With a 100-dB common mode rejection ratio (at 60 Hz) and 1-kΩ source unbalance, the boards have a 100-MΩ input impedance and 1-μV rms input voltage noise.

Analog output portions of all I/O systems feature two input buffered, 12-bit DAC channels and a pulse output channel for Z axis brightening. Outputs are contained on the same board as the input system and microcomputer interface logic. All bus related data, status, and control parts use 3-state logic for connection to the microcomputer interface structure. Multiplexer address selection modes are random, sequential, or overlapped.

Circle 422 on Inquiry Card

DS BRIEFS

High Speed Dynamic Memory System Consumes Low Power—Model 460 64k-byte memory is organized into four blocks, each deselectable under program control for memory mapping. Manufactured by Industrial Micro Systems, Inc, 628 Eckhoff St, Orange, CA 92668, the board supports 8080 or Z80 CPUs and operates at 4 MHz with no wait states. . . .**Microcomputers Convert Terminals to Complete Systems**—COMMANDER series MX and FX computers from Columbia Data Products, Inc, 9050 Red Branch Rd, Columbia, MD 21045, contain a Z80A processor, 64k-byte RAM, 8k-byte P/ROM, 1M-byte disc, four RS-232 ports, and a parallel I/O port. When combined with an RS-232 compatible CRT terminal, they form a complete system. . . .**Multibus Card Cage Holds Nine Cards**—Maintaining the 0.6" (1.5-cm) center to center spacing, the SBC 609 manages to add an extra ninth card slot. Additionally, Electronic Solutions, Inc, 5780 Chesapeake Ct, San Diego, CA 92123, has added the capability of one card slot that accepts a 2-level wirewrap card.

Rugged Monitor Features 80-Char x 24-Line Display—The 12" (31-cm) black and white VIDEO 100-80 monitor for industrial use includes a 90° deflection picture tube, front panel controls, and mounting space for a mini-floppy disc. Leedex Corp, 2300 E Higgins Rd, Elk Grove Village, IL 60007, has also allowed space within the cabinet for an 11 x 14" (28 x 36-cm) custom controller electronics board. . . .**Realtime Development Tool Modifies Large Programs Online**—Written in position independent code, the IAS990 immediate assembler for the TI TM990/100M-1 microcomputer requires less than 2k bytes. The listing produced is similar to TI's format. Available from Alpha Dot Software Marketing, 98 W Heath Rd, Farnborough, Hampshire GU14 8QY, England, the assembler quickly writes complete modules and patches.

Multitasking Computer System Supports Up to 48 Users—A Zilog Z8000 CPU and up to 640M bytes of Winchester disc storage are employed by Taurus Research, Inc, 2880 S Main St—220, Salt Lake City, UT 84115, in the T8000 series computers. Entry level T8000/2 has two floppy disc drives and two serial ports; mid-level /40 has eight serial I/O ports, a 40M-byte hard disc, and one backup floppy disc drive. . . .**Bank Selectable Memory Board Attaches to S-100 Bus Microcomputers**—Using output port addressing for the bank select feature, DMB6400 is configured as four totally independent 16k banks of memory. Components included by Measurement Systems & Controls, Inc, 867 N Main St, Orange, CA 92668, are a dynamic memory array, bus interface/control logic, and voltage regulators. Invisible onboard refresh logic is used.

Memory Resident and Transient Commands Provide Disc Operating System's Flexibility—HA-CP/Z8000, an interrupt driven, microcomputer disc operating system, is characterized by device independent I/O, sequential and random file access methods, and chaining and overlaying of user programs. Hemenway Associates, Inc, 101 Tremont St, Suite 208, Boston, MA 02108, allows use of the Peripheral Interchange Program (PIP) to transfer data between diverse physical devices. . . .**Speaker Trained, Isolated Word System Recognizes Speech**—The TRS-80 VOXBOX™ can be programmed with a 32-word vocabulary, permitting the computer to respond to spoken words with 85 to 95% accuracy. Words or phrases may enter data, control, and instruct the TRS-80 microcomputer without keyboarding. Radio Shack, a div of Tandy Corp, 1300 One Tandy Center, Fort Worth, TX 76102, considers the device as an entertainment and experimentation unit. . . .**Two Realtime Executive Versions Aid Software Management**—REX-80 V03 that supports 8080/8085 and Z80 microcomputers with two separate versions is fully event driven, allowing asynchronous operation of up to 255 independent tasks, each with 16 local event flags. Other features of the executive that Systems & Software, 2801 Finley Rd, Suite 101, Downers Grove, IL 60515, has included are an orthogonal data structure and virtual processor approach.

Supply Powers Microcomputer System And Two Floppy Discs—Model CP134 supplies three regulated dc outputs in an openframe chassis for two 5.25" (13.34-cm) disc drives and a microcomputer. Microcomputer Power, Inc, 2272 Calle de Luna, Santa Clara, CA 95050, has manufactured the unit with dc outputs of 5 V at 6 A, 12 V at 3.4 A/4 A peak, −12 V at 0.5 A or −5 V at 0.25 A. . . .**12k BASIC Acts As An Interpreter For 6800 Microprocessor**—Wintek Corp, 1801 South St, Lafayette, IN 47904, has released its 12k BASIC to support numeric, string, and Boolean data types. Floating point scientific functions and a random number generator suit it to engineering, scientific, and data processing uses; direct memory read/write, assembly language subroutines, and flexible I/O are oriented toward both process control and data acquisition applications.

64k-Byte Memory For S-100 Bus Computer Uses 16-Bit Mode—Organized as 32k words by 16 bits, M990064K from Marinchip Systems, 16 St Jude Rd, Mill Vallley, CA 94941, works with the M9900 CPU. Designed to run at 3.3 MHz, the memory triples servicing speed of CPU memory requests. A 16-bit I/O port controls bank selection on the board. . . . **Adapter Attaches Up To Four Cartridge Drives As Removable Media**—Cameo Data System's (1626 Clementine St, Anaheim, CA 92803) TRS-80 model II adapter for the company's DC-500 cartridge disc controller adds four 2.5M- to 20M-byte cartridge drives to the microcomputer. Removable cartridges permit exchange of data bases among applications. . . . **Multitasking Executive Monitors And Controls Realtime, Asynchronous Events**—Framework of the AMX realtime executive for 8080/8085 and Z80 systems supports user routines and interrupt service procedures, allowing the user to specify task priorities. The executive coordinates the execution according to asynchronously occurring interrupts. Intertask communication and circular list facility are also included by KADAK Products Ltd, 206-1847 W Broadway, Vancouver, BC V6J 1Y5, Canada.

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SOFTWARE

Realtime Executive Offers Compactness And Speed For Industrial Use

Expanding the software offerings for industrial microprocessors, the Real Time Executive (RTX) is an alternative to the PCS Industrial Pascal recently introduced by Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176. They both run on the company's 180 and Superboard based MicroHost/development packages, including the 3800B, 3900A, and 3905A. Specific applications are industrial control, monitoring, and source data acquisition.

Similarities between the two programming approaches are that they are event oriented, interrupt driven with multitasking capabilities. In addition, users can write target machine programs which monitor and respond to events as they occur.

RTX requires 2.1k bytes of ROM, being more compact than the 15k-byte Industrial Pascal. Execution times are 600 to 800 μs and 3 to 5 ms, respectively. The latter is suited to target environments where average event occurrence is slower than 10 ms. Below 5 ms between events (more than 200 events/s), RTX is more suitable. It is also useful when one program is to be implemented in more than 100 target/remote machines. Programmed in assembly language, it executes as native machine code and is machine dependent.

Circle 423 on Inquiry Card

Compiler/Interpreter Provides Easy to Learn High Level Language

BASIC 1 compiler/interpreter CDP18S834 simplifies and accelerates program development on the COSMAC DOS development system (CDP18S007). The user has the option of developing and running programs directly in BASIC 1 or of converting these programs to executable object code capable of running at a greater speed.

With the interpreter, the user can write BASIC 1 programs with line numbers for later execution and without line numbers for immediate execution. Disc related statements allow programs to be saved on floppy disc for later recall. The interpreter also detects errors in a statement and generates an error message.

The compiler translates any stored BASIC 1 program into assembly language; the programmer may specify where in memory the program, variables, and stack are to reside. The COSMAC Macroassembler then assembles the compiler output into executable object code.

BASIC 1 is an easy to learn language that allows beginning programmers to develop elementary application programs. As the core of a system, it permits facilities to be extended with the addition of machine language routines; the only limit is the system memory. Language functions include MOD, AND, OR, XOR, MAX, MIN, SGN, ABS, HEX, RND, INP, and USR.

Developed by RCA Solid State Div, Rt 202, Somerville, NJ 08876, the software handles lines up to 70 characters long. Line numbers range from 1 to 32,767; multiple statements per line are acceptable. Decimal or hexadecimal numbers may be entered. A single capital letter designates a variable.

Fixed point arithmetic expressions are composed of numbers, variables, and/or functions joined by operators and possibly grouped by parentheses. Expressions are evaluated modulo 2^{16}.

Circle 424 on Inquiry Card

Software Packages Handle Strings And Symbol Tables

Two separate collections of string and symbol table handling routines have been designed to operate on 8080 and Z80 microcomputers. Machine independent STRING 80, which also runs on the 6800 microcomputer, requires a FORTRAN IV compiler to compile the package as a set of subroutines. Isolation of the actual storing/fetching of a character from a string into two machine dependent primitive routines achieves the machine independence.

String/substring functions supported are moves, fills, comparisons, and concatenation. Complex functions supported by the Software'70 package (Box 3623, Anaheim, CA 92803) are substring searches of single or multiple occurrence, substring replacements of the same or different length, substring insertions, and substring deletions, as well as a full set of functions to maintain ordered lists of symbols. All of the functions operate on variable length strings and substrings. Available on cards, paper tape, or magnetic tape, the software is priced at $150.

Circle 425 on Inquiry Card

STRING/80 Bit from Key Bits Inc, PO Box 592293, Miami, FL 33159, requires CP/M to operate; the assembly language relocatable routines use Microsoft's FORTRAN convention of register handling. Single strings, tables (2-dimensioned strings), and matrices (3-dimensioned strings) are handled. Strings may be up to 255 characters in length.

Functions offered are merging; comparing and creating strings; extracting left, right, or middle portion of a string; scanning for the presence of another string; and determining string length. CP/M calls of kill, rename a file, directory search, reset, and disc drive assignments are supported, as is ability to chain or pass control from one program to another by calling the program name. CP/M routines reside in a separate utility library with their source codes. Software, with source code for the utility library and all demonstration programs, is distributed on 5.25" (13.34-cm) or 8" (20-cm) CP/M compatible soft-sectored floppy discs for $95. □

Circle 426 on Inquiry Card

BIT-SLICE DESIGN APPROACHES

Hank Brineen

National Semiconductor Corporation
Santa Clara, California

The variable microcycle approach was developed when 2900-type bit-slice components were slower and were used predominately in complex central processing unit designs where synchronism was not a prime consideration. This approach is rapidly becoming outmoded. Today a large number of applications are controller oriented, and synchronism to external events is very important. In such designs it is crucial to know both what the precise microcycle period is and when a sequence of microcycles begins and ends. With the variable microcycle approach, establishing a precise time period is not generally feasible. (See *Computer Design,* Oct 1979, pp 168-174.)

Assume that in a particular design it is necessary to vary the microcycle period only 10% of the time. However, there are different delays for various different instructions. For a few standard microcycles after one extended microcycle execution period, it might be possible to predict the beginning and ending of successive microcycle periods. With the addition of other extended microcycle intervals having different values, synchronization suffers, since the timing point at which an interrupt may be serviced is variable.

One straightforward approach to synchronization is to define a specific maximum microcycle period and design the system so that the large majority of operations are performed within that period. The few remaining longer operations would be performed by using multiples of standard periods.

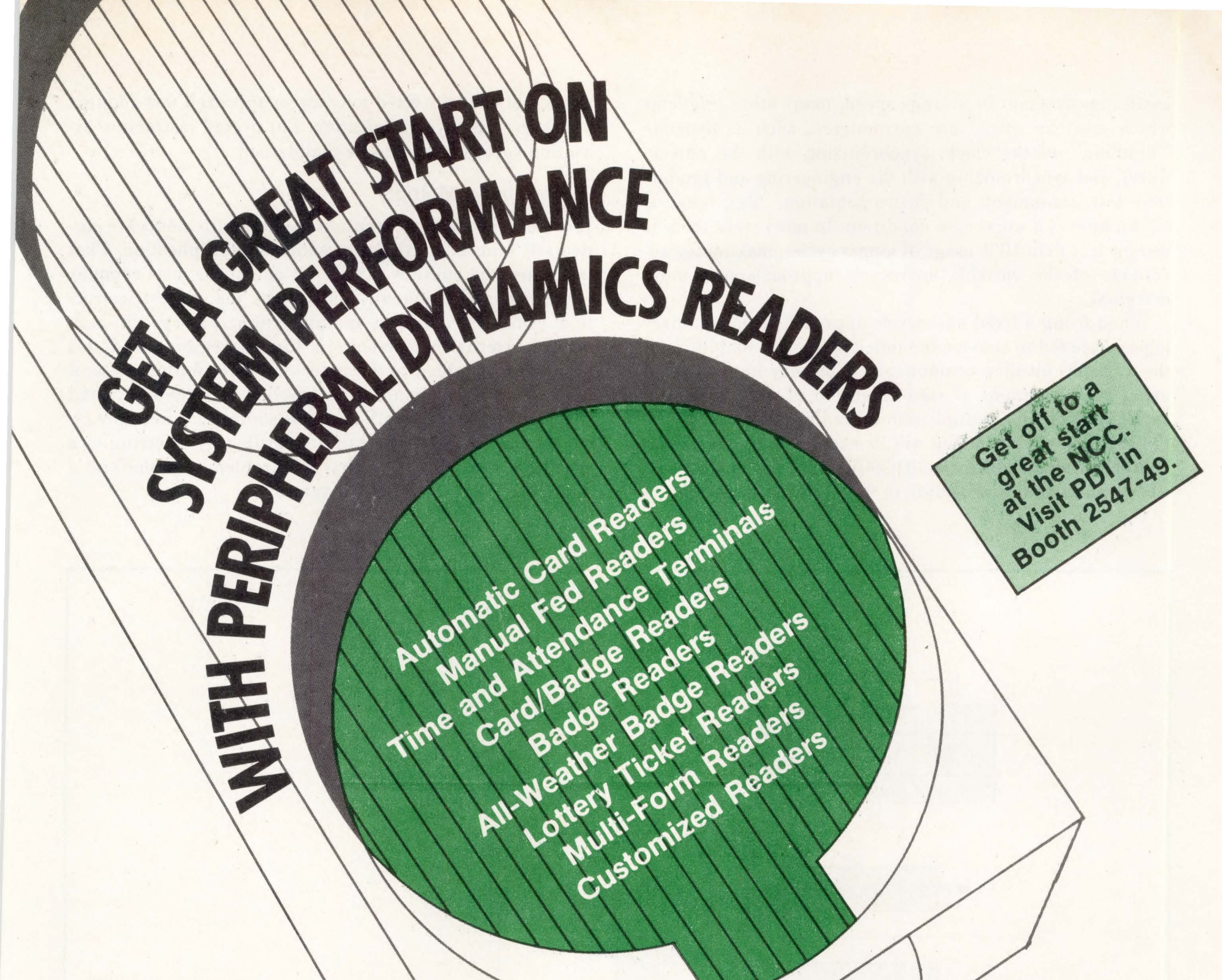
In a design where 10% of the cycles need to be 140 ns while the other 90% are 100 ns, the average time for the variable microcycle approach would be

$$t_V = 0.9(100 \text{ ns}) + 0.1(140 \text{ ns}) = 104 \text{ ns}$$

For the multiple fixed cycle approach, where an extra microcycle is taken rather than varying the basic interval, the average time can be expressed as

$$t_m = 0.9(100 \text{ ns}) + (0.1)(2)(100 \text{ ns}) = 110 \text{ ns}$$

At first glance, the variable microcycle approach may appear best. After a little thought, however, it becomes clear that in most cases it is not. In the particular case chosen, the variable microcycle approach averages 6 ns faster than the multiple fixed microcycle approach. But for this relatively



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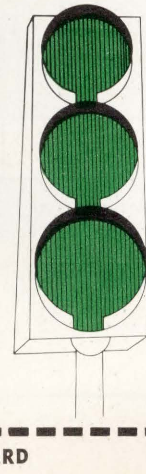

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small improvement in average speed, many other problems which must be solved are encountered, such as dynamic "diddling" of the clock, synchronizing with the outside world, and synchronizing with the engineering and production test equipment and instrumentation. Also, what is shown here is a worst case condition. In most cases there is usually less than 10% usage of longer cycles, making the advantage of the variable microcycle approach even more marginal.

When using a fixed microcycle approach, some auxiliary logic is needed to achieve the inherent speed capabilities of the variable bit-slice components. This may be illustrated using such functions as sign extension of data, shift and rotate control, and multiplication. For illustrative purposes, the multiplication function will be examined here, utilizing National Semiconductor's IDM2901A bit-slice component, whose architecture is shown in Fig 1. It is important to remember that the fixed microcycle approach was adopted to achieve easy synchronization. But overall instruction execution speeds must also be maintained.

Performing a Multiply

Processor instruction execution speed requirements are particularly crucial in the performance of multiplication. That is because the multiply function is one of the most complex operations and frequently determines the longest instruction cycle time. To do multiplication, passage through several external components is usually required and this time must be added to the processor time. With the use of high speed components, it is possible to circumvent and shorten this external path and thus shorten the multiply cycle time. This technique can be clarified by referring to a specific example. Assume that the problem is to perform a multiply of two signed 16-bit values.

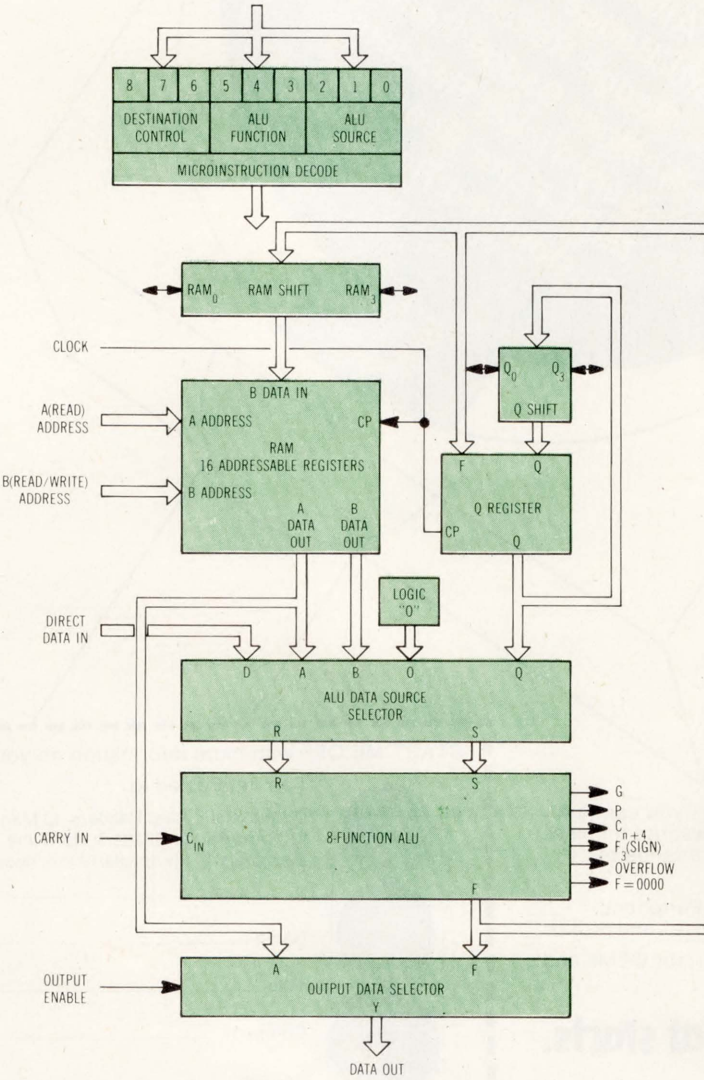
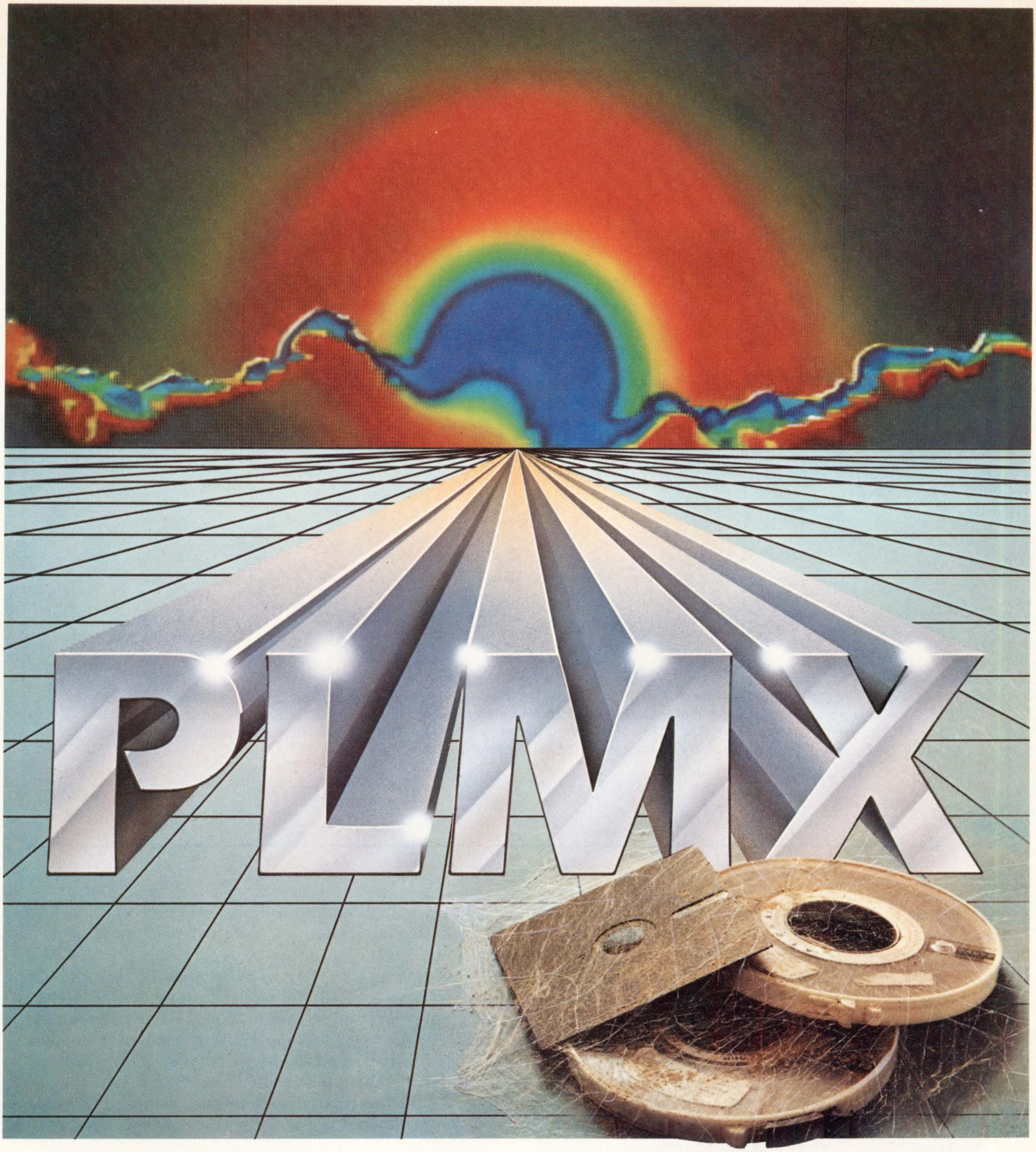


Fig 1 Bit-slice component. Architecture of National Semiconductor's IDM2901A 4-bit bipolar microprocessor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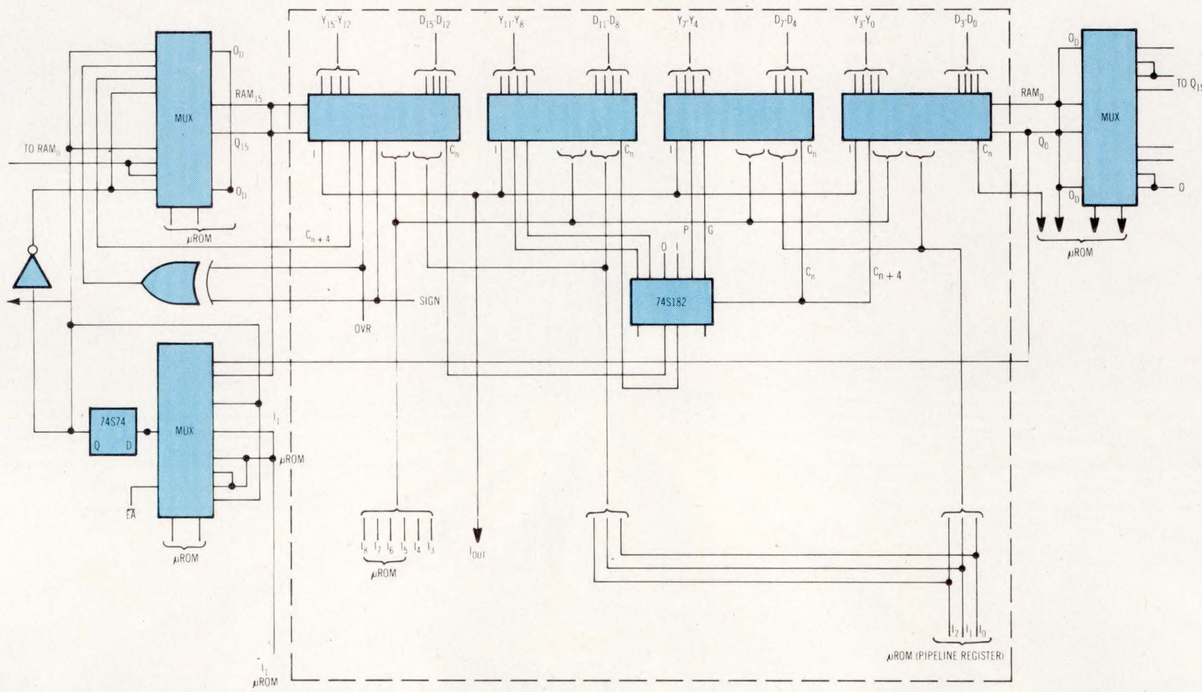

Fig 2 Logic circuit implementation. Fixed microcycle bit-slice design (within broken lines) is limited to use of 100-ns IDM2901A components, allowing general multiply execution time no lower than 124 ns. Expanded diagram adds one or more MUXs, external exclusive-OR gate, and simple flipflop (74S74). This allows faster bit-slice components (IDM2901A-2), and execution time for same operation is reduced to 79 ns

In Fig 2, a logic circuit is implemented using a high speed 100-ns Schottky coupled logic bit slice, which allows a multiply to be performed 30 to 70 ns faster per cycle than standard low power Schottky bipolar bit-slice components. For the number of cycles needed for a multiplication of two 16-bit numbers, this is a total speed improvement of 480 to 1120 ns at the system level. The standard microcycle time of the bit-slice component can be used, so no special multiply cycle intervals are required. This operation, therefore, makes possible a processor or controller with a less complicated clock control circuit, for easier synchronization.

As shown in Fig 3, which is a timing flowchart for Fig 2, almost all multiply operations require loading the multiplier into the Q register ($I_{678} \rightarrow Q$) and clearing the partial product register (Q, MUX delay), since with this bit-slice design it is not possible to do both in the same cycle. If (as the flowchart shows) the A and B register file addresses are set up on the clear register cycle, $A + B \rightarrow \overline{G}/\overline{P}$ (where $\overline{G}$ and $\overline{P}$ are carry generate and propagate outputs), and thereafter these addresses do not change. Therefore, they do not enter into the timing equations. The critical path, in an operation with a positive signed multiplicand, is to the I_{012} inputs and through the bit slices ($I_{012} \rightarrow \overline{G}/\overline{P}$). In a normal add and shift operation, the data path then continues through C_n to the RAM_0 input and back to the RAM_3 input (Fig 3). But if a negative multiplicand is involved, as there often is in a fully signed general multiply, a different path must be considered.

This path goes from C_n to overflow or F_3, and through the additional exclusive-OR gate and multiplexer, to the RAM input. Maximum delay path is 20 ns, from overflow and F_3 outputs, back to the RAM input. Using standard techniques, common to previous 2900 bit-slice designs, 15 conditional adds, followed by a shift and one conditional subtract, and then a shift, are required to do a signed multiply in 2's complement notation.

Achieving Higher Performance

Note that in the expanded version of Fig 2 there is an extra external 74S74 positive edge triggered flipflop, adding an additional stage of register storage to the Q register, compared to traditional designs. It is, therefore, necessary to shift Q one time, storing the partial product, without shifting the file register. But, using the added circuitry may be compensated for in other ways, as is illustrated in the timing diagram in Fig 4.

For example, if the A and B address lines are set up one cycle ahead of the multiply sequence (during clock to Q), it would be possible to use the much faster 60-ns IDM2901A-2s, instead of the 100-ns IDM2901As. As shown in Fig 4, the max

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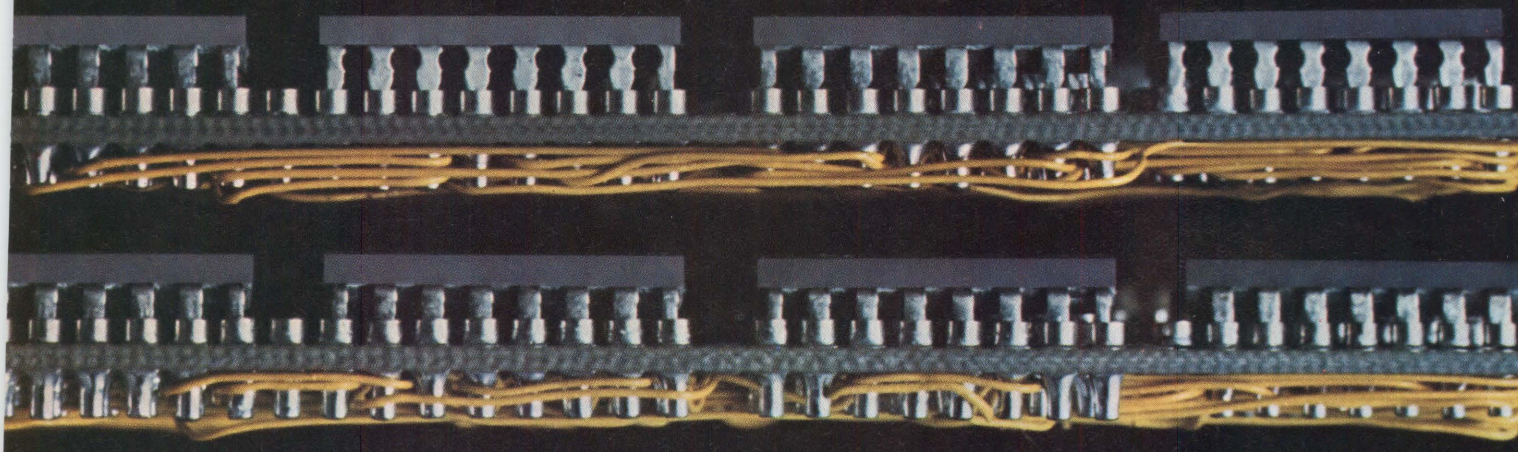

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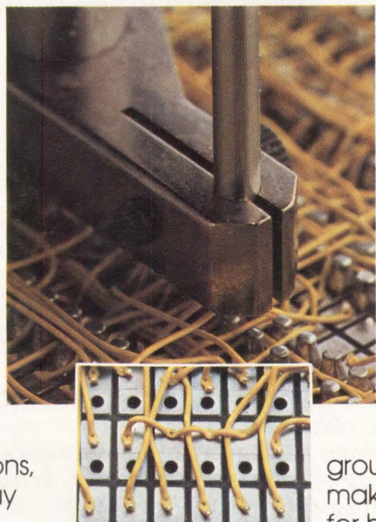

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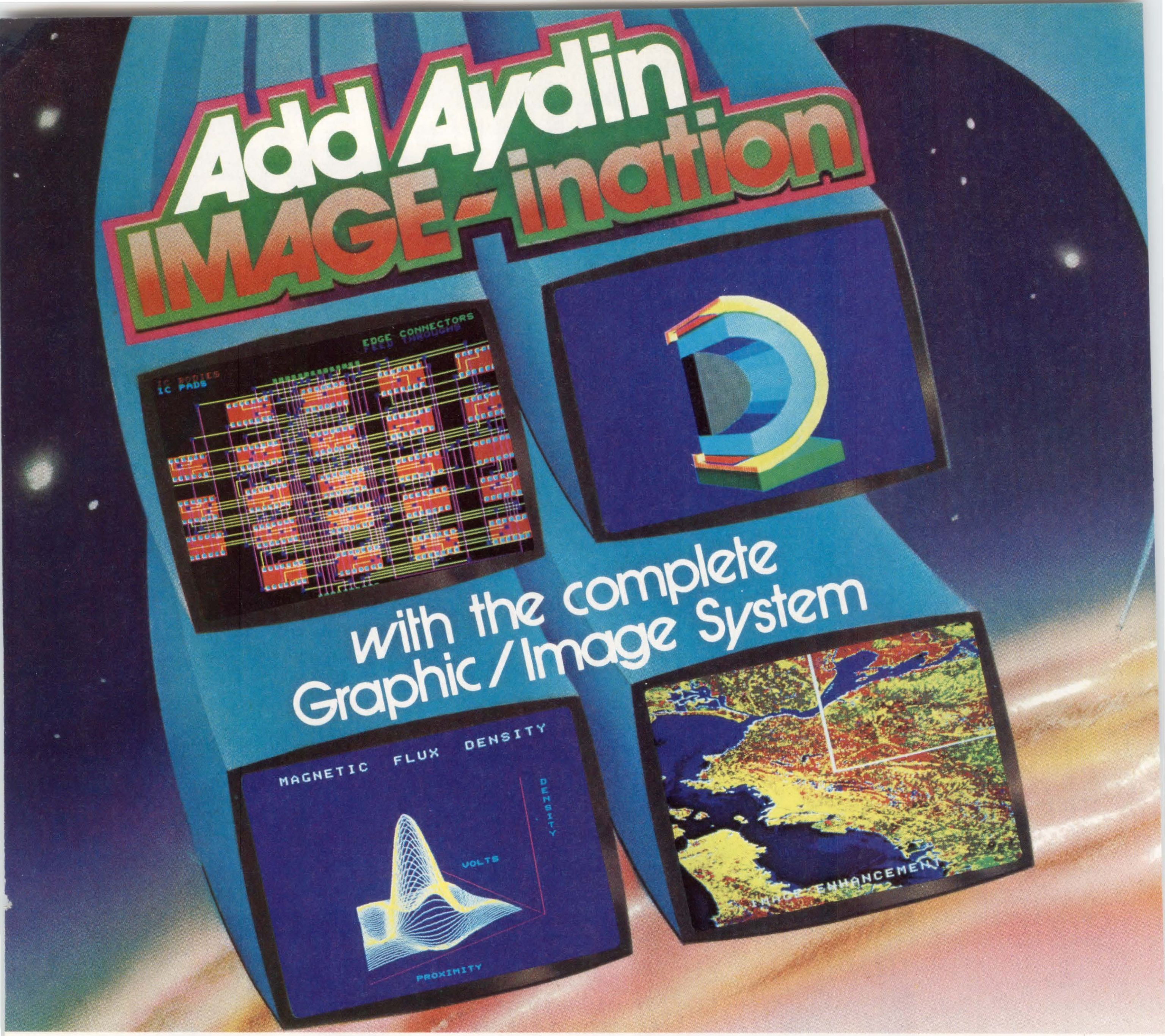

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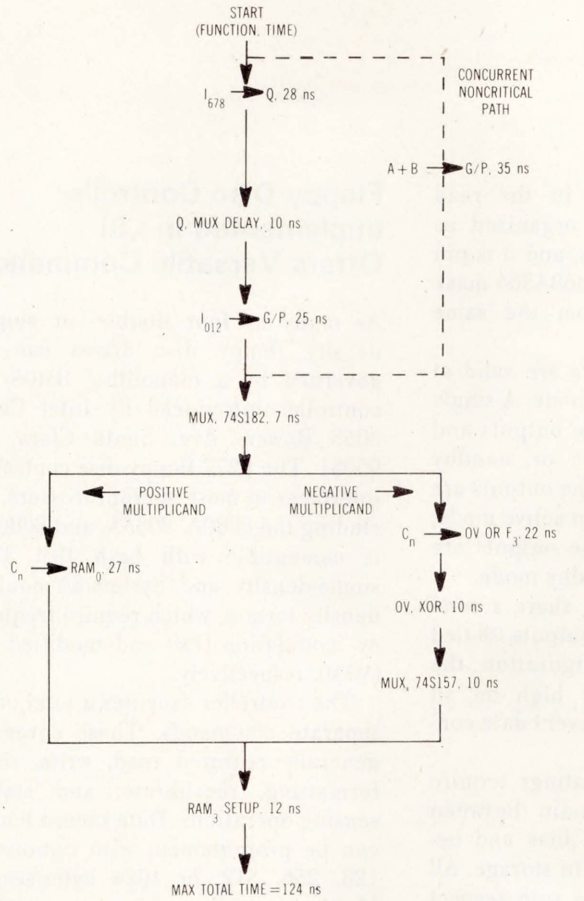


Fig 3 Timing diagram for Fig 2. Alternate paths are shown for positive and negative multiplicands

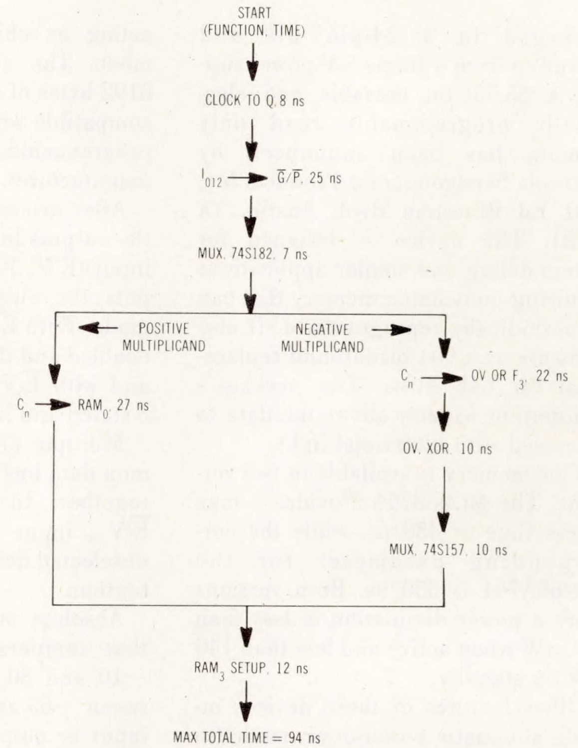


Fig 4 Timing diagram for Fig 2, expanded. 60-ns bit-slice components are substituted for standard 100-ns slices

total time for a fully signed multiply is 94 ns, a net savings of 30 ns per microcycle, for a 25% reduction in cycle time. If slower, low power Schottky bit-slice components were used, microcycle time would be slowed to about 167 ns. In that context, the approach taken here results in a 73-ns decrease per cycle, almost a two-to-one improvement in performance.

If only positive multiplicand multiplies are considered, the maximum time is 79 ns, 15 ns faster per cycle than the general fully signed multiply. To avoid the time penalty for a negative multiplicand, all that is necessary is to microprogram the circuit to test for that possibility. If the multiplicand is negative, it is converted to 2's complement form and a positive multiplicand multiply is performed, with reconversion at the end, as needed. Although this requires three additional cycles to do the multiply, it does not cost much in total microcycle time. For example, positive multiply/test = (18 + 3 cycles) x 79 ns = 1659 ns, as compared with fully signed multiply = (18 cycles) x 94 ns = 1692 ns. As can be seen, the positive only multiply is 33 ns faster, even though it takes three additional cycles. The most important consideration is that with this technique all cycles can operate at the 79-ns cycle time, resulting in a total improvement of 15%.

Conclusions

As component speeds have improved, the multiple fixed cycle approach to bit-slice design has become increasingly advantageous. This technique is cleaner and simpler than that of using variable microcycles, a solution that was practical when components were slower. The use of variable microcycles involved reliance on intricate strategies and makeshift measures designed to provide fast circuits based on chips of marginal speed. In constrast, the use of multiple fixed microcycles relies on the strength of the component itself, and benefits from an operational cycle that is modular in time rather than linked to contingencies.

UV Erasable, Electrically Reprogrammable 64k Memory Joins ROM Compatible Family

Packaged in a 24-pin DIP and operating from a single 5-V power supply, a 65,536-bit erasable and electrically programmable read only memory has been announced by Motorola Semiconductor Products Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721. The device is designed for system debug and similar applications requiring nonvolatile memory that can be periodically reprogrammed. It also finds use as a fast turnaround replacement for 64k ROMs. The package's transparent window allows the data to be erased with ultraviolet light.

This memory is available in two versions. The MCM68764 provides a max access time of 450 ns, while the corresponding parameter for the MCM68A764 is 350 ns. Both versions share a power dissipation of less than 880 mW when active and less than 140 mW on standby.

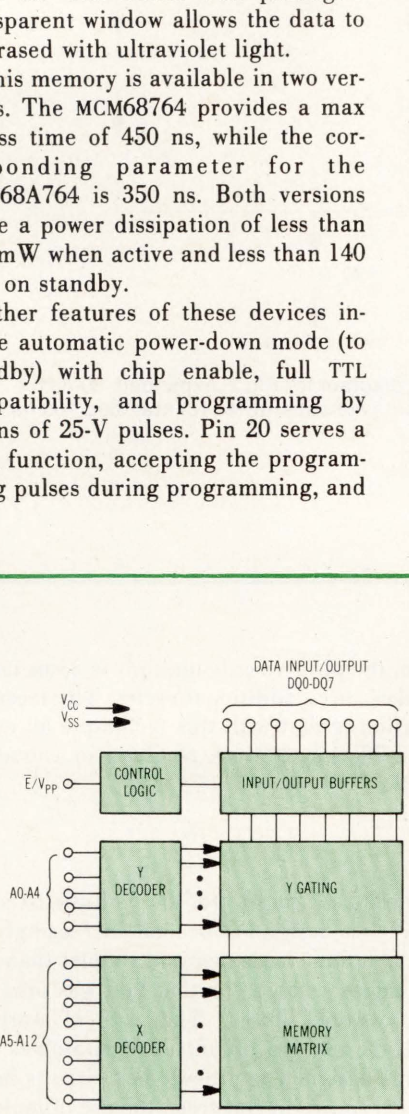
Other features of these devices include automatic power-down mode (to standby) with chip enable, full TTL compatibility, and programming by means of 25-V pulses. Pin 20 serves a dual function, accepting the programming pulses during programming, and acting as chip enable in the read mode. The memory is organized as 8192 bytes of 8 bits each, and it is pin compatible with the MCM68A364 mask programmable ROM from the same manufacturer.

After access time, data are valid at the outputs in the read mode. A single input ($\overline{E}/V_{PP}$) enables the outputs and puts the chip in active or standby mode. With $\overline{E}/V_{PP} = 0$ the outputs are enabled and the chip is in active mode, and with $\overline{E}/V_{PP} = 1$ the outputs are 3-stated and it is in standby mode.

Multiple EPROMs may share a common data bus with like outputs OR-tied together. In this configuration the $\overline{E}/V_{PP}$ input should be high on all unselected devices to prevent data contention.

Absolute maximum ratings require that temperatures remain between -10 and 80 °C under bias and between -65 and 125 °C in storage. All input or output voltages with respect to V_{SS} during read are limited to a range of 6 to -0.3 Vdc. Supply voltage V_{PP}, relative to V_{SS}, must stay between 28 and -0.3 Vdc.

Circle 350 on Inquiry Card



Structure of 64k EPROM. MCM68764/68A764 memory from Motorola is compatible with 24-pin, 64k ROMs

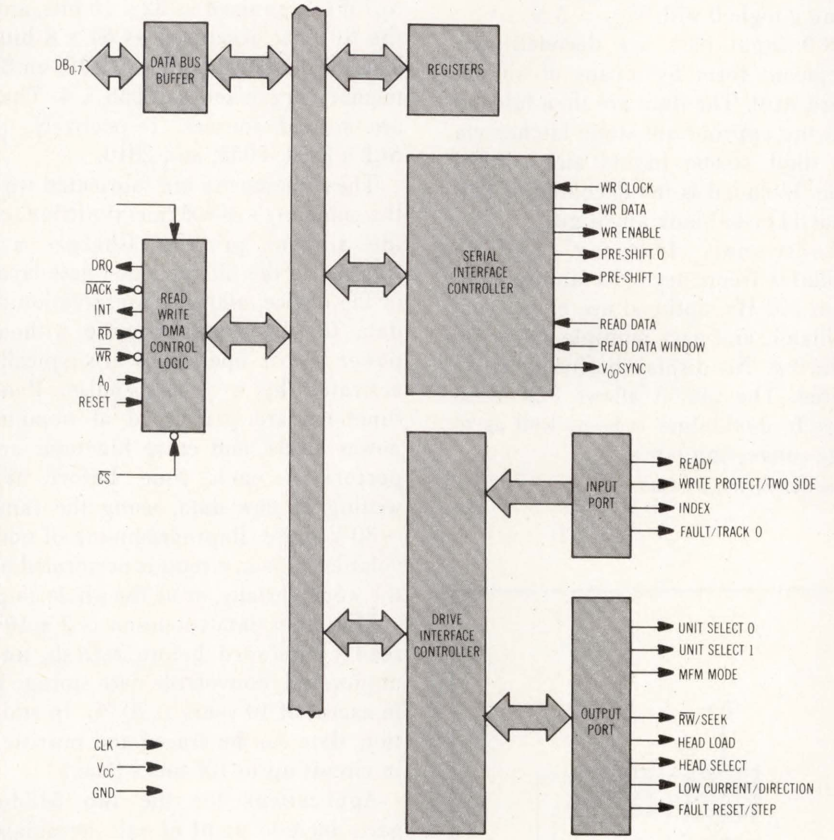
Floppy Disc Controller Implemented in LSI Offers Versatile Commands

As many as four double- or single-density floppy disc drives can be governed by a monolithic HMOS LSI controller introduced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. The 8272 floppy disc controller interfaces to most microprocessors, including the 8080A, 8085A, and 8086. It is compatible with both IBM 3740 single-density and System/34 double-density format, which require frequency modulation (FM) and modified FM (MFM), respectively.

The controller executes a total of 15 separate commands. These cover all generally required read, write, scan, formatting, recalibrate, and status-sensing operations. Data record length can be programmed, with options of 128, 256, 512, or 1024 bytes/sector. Multitrack and multisector transfers are also programmable. Another function that can be selected is the scanning of up to a cylinder's worth of data fields to compare data byte by byte with data in the processor's main memory. Parallel seeks on up to four drives can be programmed. In this seek mode, the controller keeps track of all four head operations.

Read commands include read data, read ID, read deleted data, and read a track. Scan commands include scan equal, scan high or equal, and scan low or equal. Write commands include write data, write deleted data, and format a track. Other commands are used to specify operational changes, seek data, recalibrate, sense interrupt status, and sense drive status.

Additional features include a single-phase 8-MHz clock, operation from a single 5-V power supply, select lines for multiple heads, and programmable loading and unloading of heads. The device provides control signals that simplify the design of an external phase locked loop and write-precompensation circuitry. It offers equipment manufacturers a 20 to 1



Single- or double-density floppy disc controller, Intel's 8272, can interface to four drives. Monolithic device features set of 15 commands for programming read, write, scan, formatting, recalibrate, and status-sensing operations

reduction in part counts compared to conventional controller boards.

In addition, the design is pin and function compatible with the Nippon Electric Company's μPD 765 controller chip. It is claimed that the two devices effectively establish the first standard for LSI floppy disc controllers.

To enhance system performance, the chip will typically be used with a direct memory access controller, such as the 8237 DMA controller chip from the same manufacturer. The processor has only to load a single command into the disc controller to accomplish a complete block transfer.

Absolute maximum ratings require that supply voltage (V_{CC}) and all input and output voltages stay between −0.5 and 7 V. Maximum allowable power dissipation is 1W. Temperature must remain between −10 and 70 °C in operation and between −40 and 125 °C in storage. Circle 351 on Inquiry Card

CMOS Chip Functions As 4-Digit LCD Decoder Driver

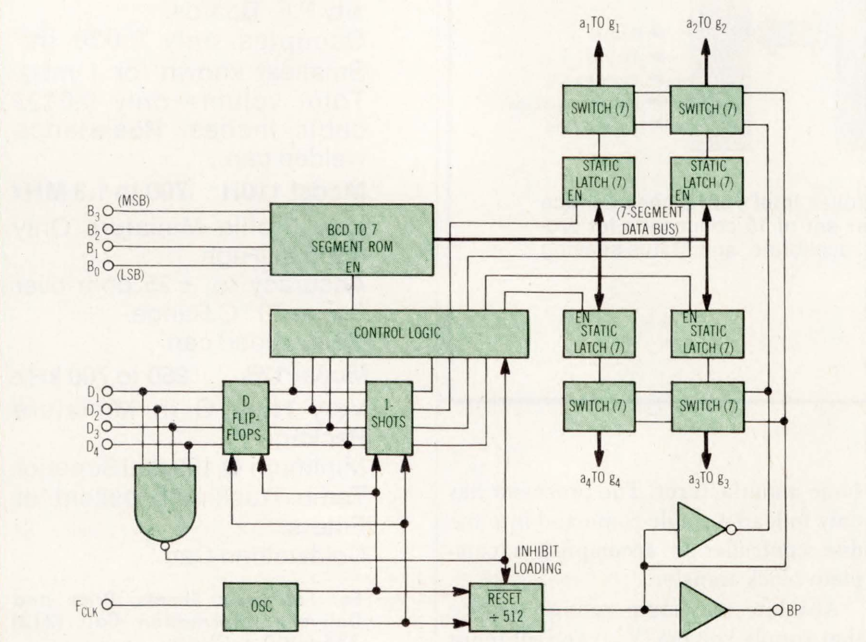
A monolithic CMOS decoder driver, the DF412, contains all of the circuitry needed to decode up to four digits of multiplexed liquid crystal display information. Produced by Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054, this chip operates with a power consumption of 1.5 mW (typ).

An internal oscillator, its frequency controlled by an external capacitor, develops a backplane (BP) signal that is a square wave swinging between ground (V_{SS}) and the positive supply (V_{DD}). Segment drivers supply square waves of the same frequency as the backplane but either in phase for an off segment or out of phase for an on segment. In this type of LCD digit driving, the net dc potential applied between segment and backplane is zero, a necessary requirement for long display life. Digital input levels are defined as input voltages >4 V being a logic 1 and input voltages <0.8 V being a logic 0 with V_{DD} = 5 V.

BCD input data are decoded into 7-segment form by means of an onboard ROM. The data are then latched into the appropriate static latches via the digit strobe inputs and control logic. Included is the decoding of BCD input 1111 to blank any digit.

Additional features include oscillator frequency selectability from 30 to 100 Hz, optional use of external oscillator, and easy multiple driver interfacing. No display buffering is required. The pinout allows PCB interfaces to dual-inline LCDs as well as to edge-connecting types.

Circle 352 on Inquiry Card



Decoder driver, DF412 from Siliconix, interfaces with 4-digit LCDs. Onchip ROM converts BCD inputs to 7-segment display signals

EAROMS Provide 10 Years of Nonvolatile Storage

Three models of nonvolatile, fully decoded, electrically erasable and reprogrammable read only memories have been announced by Nitron Inc, 10420 Bubb Rd, Cupertino, CA 95014. Two of the chips each provide storage capabilities of 512 bits. These are the NC7051, organized as 32 x 16 bits, and the NC7055, organized as 64 x 8 bits. The third EAROM is the NC7810, an 8k memory organized as 2048 x 4. They are second sources, respectively, to NCR's 2051, 2055, and 2810.

These memories are fabricated with the company's MNOS (metal nitride oxide silicon) process. Charges are trapped in the nitride/oxide gate layer of the device, allowing preservation of data for 10 years or more without power. Write operations are typically activated by a −30-V pulse. Read functions are performed at nominal power levels, and erase functions are performed each time before the writing of new data, using the same −30-V pulse. Reprogramming of nonvolatile chips in circuit is performed by the word, serially, or by the whole chip.

Minimum data retention is 2 x 10^{11} read cycles/word before refresh, and unpowered, nonvolatile data storage is in excess of 10 years at 70 °C. In addition, data can be erased and rewritten in circuit up to 10^5 times (max).

Applications for the two 512-bit parts include point of sale terminals, security systems, inflight recorders, and navigation systems. The 8k memory finds use in applications requiring a high density organization, such as navigational control, data processing, and test and instrumentation.

Circle 353 on Inquiry Card

Low Priced 256k Bubble Memory Occupies Small Area

Low cost and a compact 16-pin package, said to be the smallest in the industry, characterize a newly announced quarter-megabit magnetic bubble memory, currently being sampled. The NBM2256 uses a dual block-replicate architecture consisting

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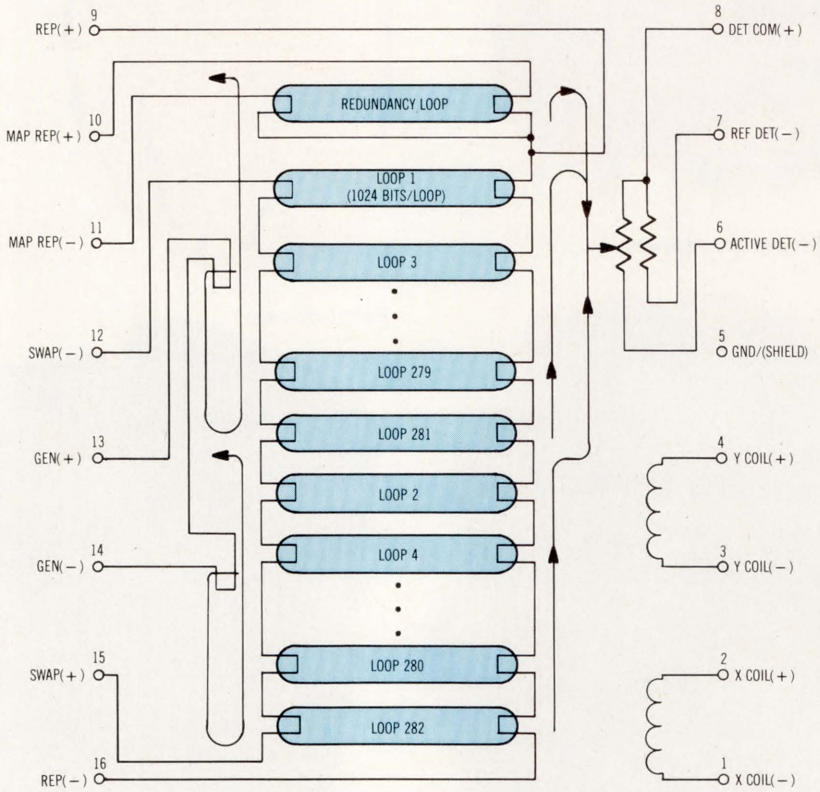
of 282 minor loops of 1024 bits each, which are loaded through swap gates and read via replicate gates at opposite ends of the loops. These loops, organized into even and odd subsets, include 256 data loops, 20 redundancy loops, and 6 error correction loops. An additional dedicated loop provides an onchip redundancy map.

The manufacturer, National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, uses direct-step-on-the-wafer projection lithography to provide a minimum device geometry of 1.5 μm and a storage cell size of 12 x 12.5 μm. This results in a density of 6.7 $(10)^5$ bits/cm^2 and an overall die size of 300 x 320 mils. Layout space is defined as a footprint of 1.1 x 1.1" (2.8 x 2.8 cm), height of 0.36" (0.91 cm), and standard 0.100" (0.254-cm) pin spacing.

Other features include an operating frequency of 100 kHz, a data rate of 100k bits/s, and a 7-ms avg access time to the first bit of a random data block. Power dissipation (typ) is approximately 750 mW. Standard 5- and 12-V power supplies are used.

This memory will be complemented by associated support circuits to provide a complete subsystem of five ICs. These circuits, produced by the same manufacturer, are to consist of the INS82851 bubble memory controller, DS3615 function driver, DS3616 coil driver, and DS3617 sense amplifier. A modular expansion capability will provide systems up to 256k-bytes.



Architecture for National Semiconductor's NBM2256 quarter-megabit bubble memory incorporates 282 minor loops, including 256 data loops and 6 ECC loops. Redundancy map is provided in additional dedicated loop

The controller is implemented using high density NMOS technology fabricated with a proprietary XMOS process. Fabrication of the other three circuits is accomplished through bipolar processes suited to the high currents and high voltages required to drive the bubble memory.

All of the basic timing and control functions are provided by the controller. At power-up it resets all control and status registers and reads the bubble memory redundancy map from the map loop to an onchip buffer. It accepts commands and data over the MICROBUS™ interface, designed for easy use with most standard MOS/LSI microprocessors. With the addition of a few low cost TTL components, it can operate with one, two, four, or eight bubbles in parallel, allowing the cost of the device to be spread over as many as eight bubble modules. Availability of controller samples is scheduled for late 1980.

High voltages required for the generate, swap, replicate and map inputs to the bubble memory are provided by the 18-pin function driver using a voltage boost that runs off the 12-V supply. Other features of this circuit include low current pnp inputs, power-up/down glitch-free protection and current control capability.

The 16-pin coil driver produces the high current drive capability needed for triangular current waveforms. In conjunction with high current, onchip clamp diodes, it provides low current logic inputs to minimize loading of the controller. Two of these units are used to drive the two coils in each bubble memory.

A peak sensing approach is used by the 16-pin sense amp to detect the differential change between a reference and active detector caused by the bubble's magnetic field as it passes under a permalloy conductor. For those applications requiring other than nominal levels a pin is provided to set the sense threshold. Tri-state® data outputs are provided to allow multiplexing.

All three DS-series support circuits are scheduled for summer 1980 availability. Until the complete set of

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support circuits becomes available, an evaluation board containing all basic subsystem functions and standard ICs is offered. The evaluation board, as well as a companion memory expansion board, will be sampled in the second quarter of 1980. Compatible with this manufacturer's Series/80 microcomputer boards and systems, the NBS100 evaluation board contains 256k bits of bubble memory, all drive and support circuitry, and a microprocessor based controller. The NBS101 expansion board offers 1024k bits of memory storage and utilizes the controller from the evaluation board. Up to eight expansion boards may be controlled by one evaluation board, allowing expansions up to 1M bytes. The board set is multibus compatible and will plug into most standard microprocessor development systems.

In sample quantities (1 to 4 devices) the memory is $500 each. The evaluation board is priced at $1300 and the expansion board at $2500 in single-unit quantities.

Mil-Temp Version Of 8-Bit ADC Performs at Video Speeds

An 8-bit fully parallel (flash) analog to digital converter introduced by TRW LSI Products, PO Box 1125, Redondo Beach, CA 90278, can digitize an analog input signal at rates from dc to 30M samples/s. The TDC-1007J-M is a mil-temp version of the commercial TDC-1007J, introduced in late 1978, and is guaranteed to operate over a case temperature range from −30 to 125 °C.

Like its predecessor, this ADC, operating without an external sample and hold circuit, will accurately sample input signals having frequency components up to 7 MHz, with a 3-dB comparator bandwidth of 40 MHz. A single convert signal controls the operation of the unit, which consists of 255 sampling comparators, combining logic, and an output buffer register. Recovery from a full scale step input occurs within 20 ns. Controls are provided for straight binary or offset 2's complement output coding, in true or inverted sense.

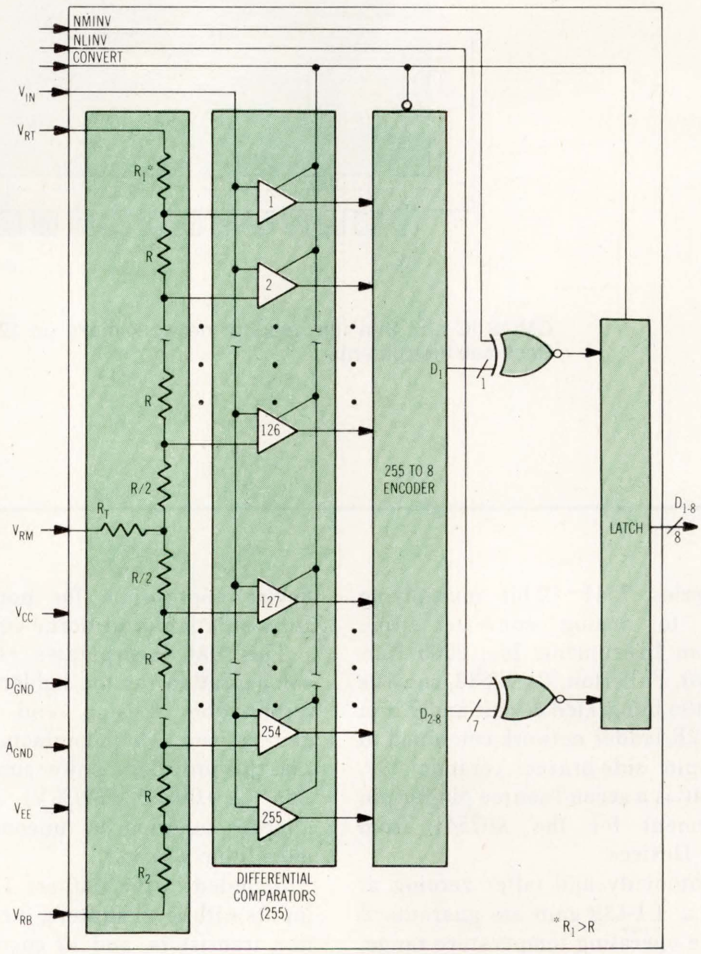
Intended to replace bulky discrete and hybrid circuits in high performance military radar and image acquisition systems, the converter can perform 30-M conversions/s while drawing only 2.5 W of power. It is implemented as a fully parallel, single chip containing 20k closely matched bipolar components.

The device finds application in radar data conversion or in high speed multiplexed data acquisition. It is used also in video data conversion, at three or four times the color subcarrier frequency for either the NTSC or PAL standard.

Additional characteristics include TTL compatibility, a 30-ps aperture jitter, 0.5° differential phase, and 1.5% differential gain. It is provided in a 64-pin ceramic DIP, and is available tested to any of the MIL-STD-883B environmental conditions.

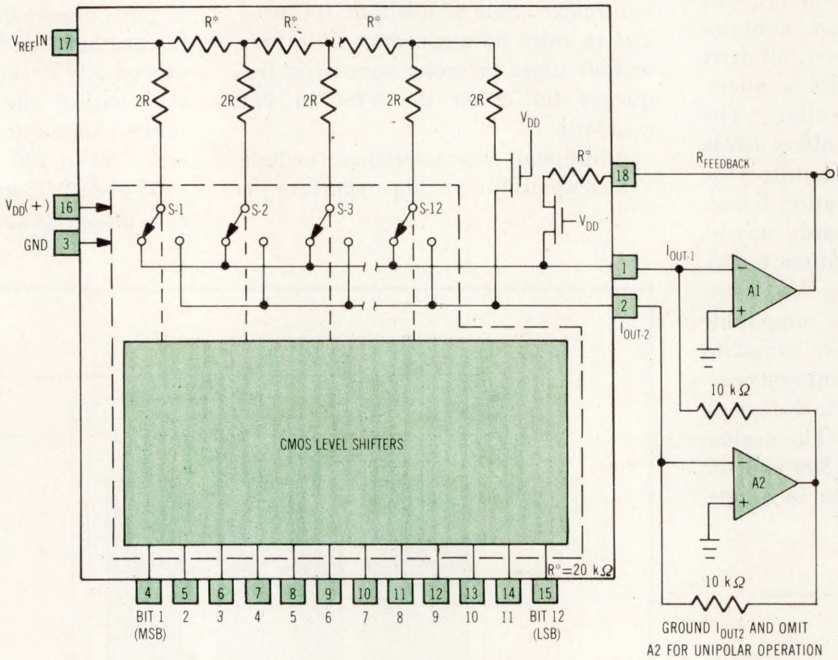
Absolute maximum ratings require that supply voltage, V_{CC}, and output voltage stay between −0.5 and 7 V. The allowable range for V_{EE} is 0.5 to −7 V, and for A_{GND} it is −1 to 1 V. Digital input voltage is constrained to a range from −0.5 to 5.5 V, while analog input voltages V_{IN}, V_{RT}, and V_{RB} lie between 0.5 V and V_{EE}. The difference between V_{RT} and V_{RB} must not exceed 2.5 V. Input current, I_{IN}, must stay within the −100- to 100-mA range. Allowable temperature ranges are −60 to 130 °C in operation and −65 to 150 °C in storage.

Circle 354 on Inquiry Card



Block diagram of TRW's 8-bit flash ADC. Device uses 255 differential comparators to sample at 30M samples/s

12-Bit DAC Combines CMOS IC And Thin Film Ladder



CMOS IC and thin film resistor network make up 12-bit multiplying DAC, 7541, from Beckman Instruments

The series 7541 12-bit multiplying digital to analog converter from Beckman Instruments Inc, 2500 Harbor Blvd, Fullerton, CA 92634, consists of a CMOS integrated circuit and a thin film R-2R ladder network combined in an 18-pin side-brazed ceramic DIP. This DAC is a second-source pin for pin replacement for the AD7541 from Analog Devices.

Monotonicity and (after zeroing at 25 °C) a ±1-LSB gain are guaranteed over the operating temperature range. A ±½-LSB linearity is guaranteed over 0 to 70 °C for the commercial (C-suffix) version and over −55 to 125 °C for the military (M-suffix) version. Power consumption is 20 mW typ, making this device appropriate for portable instrumentation or airborne equipment.

This DAC incorporates FET switch compensation for the ladder network, termination resistor, and feedback gain resistor. The manufacturer states that this provides a power supply rejection (±0.002% FSR/%V) and gain tempco superior to uncompensated monolithic versions.

Included in the DAC are 12 parallel inputs with level shifters, 2 compensation transistors, and 12 current steering switches. Each 2R leg of the inverted R-2R ladder is connected to a pair of N-channel transistors. These transistors switch the binary weighted currents that flow in each 2R leg to either the I_{OUT1} bus (logic high input) or to the I_{OUT2} bus (logic low input). Normal operation maintains I_{OUT1} and I_{OUT2} at ground or virtual ground.

Circle 355 on Inquiry Card

Octal Transceiver Provides Versatile Processor Interface

An octal bus transceiver introduced by Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, allows asynchronous, 2-way communication between data or address buses connecting processors, con-

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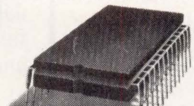

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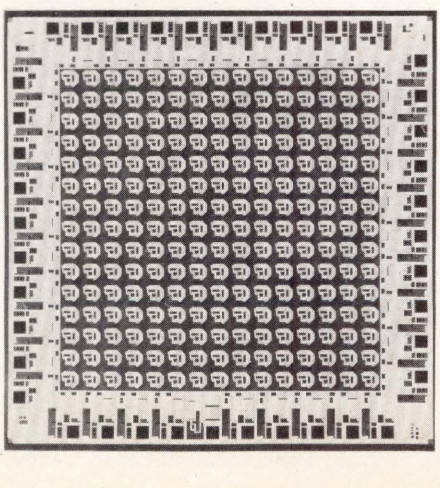

Typical Applications

Disk and CRT Controllers
Dynamic and Static Memory Controllers
Keyboard Scanners
Memory Interface Logic
Control Logic — CPU Boards
ALU Accumulators
D/A — A/D Controllers

Interdesign is a Ferranti Company

trollers, and memories. The SN74LS645, a low power Schottky bipolar device, consists of eight receiver/driver pairs, forming a complete bidirectional bus interface. It is a second source for the like-numbered part from Texas Instruments.

The 8-bit structure of this transceiver is compatible with 8-, 16-, 24-, and 32-bit data widths, making it suitable for digital design applications that range from high performance microprogrammed digital processors and controllers to single-board MOS microcomputer systems. Other characteristics include 3-state TTL compatible outputs, single 5-V power supply, low current pnp inputs that reduce loading, max supply current of 110 mA and max output sink current of 24 mA. A control input determines the direction of data flow; a separate input disables the device and establishes bus isolation.

Absolute maximum ratings limit supply voltage (V_{CC}) and input voltage to 7 V and off-state output voltage to 5.5 V. Operating free-air temperature is specified over a range of 0 to 75 °C for the commercial version and −55 to 125 °C for the military. Storage temperature must remain between −65 and 150 °C for both versions. The device is packaged in a compact 20-pin plastic or ceramic Skinny DIP™.

Circle 356 on Inquiry Card

Transimpedance Preamp Features Low Noise

Suited for use in a number of communications applications, the model 9923 preamplifier from Optical Electronics Inc, PO Box 11140, Tucson, AZ 85734 features a 5-nV/$\sqrt{\text{Hz}}$ max spectral density with a 100-GΩ input impedance. Main function of the preamp is to perform as a transimpedance type amplifier.

This device also provides a ±150-V/μs slew rate and a 30-fA/$\sqrt{\text{Hz}}$ current noise. The commercial grade unit can operate over the military temperature range of −65 to 125 °C. It is provided in a 14-pin DIP. □

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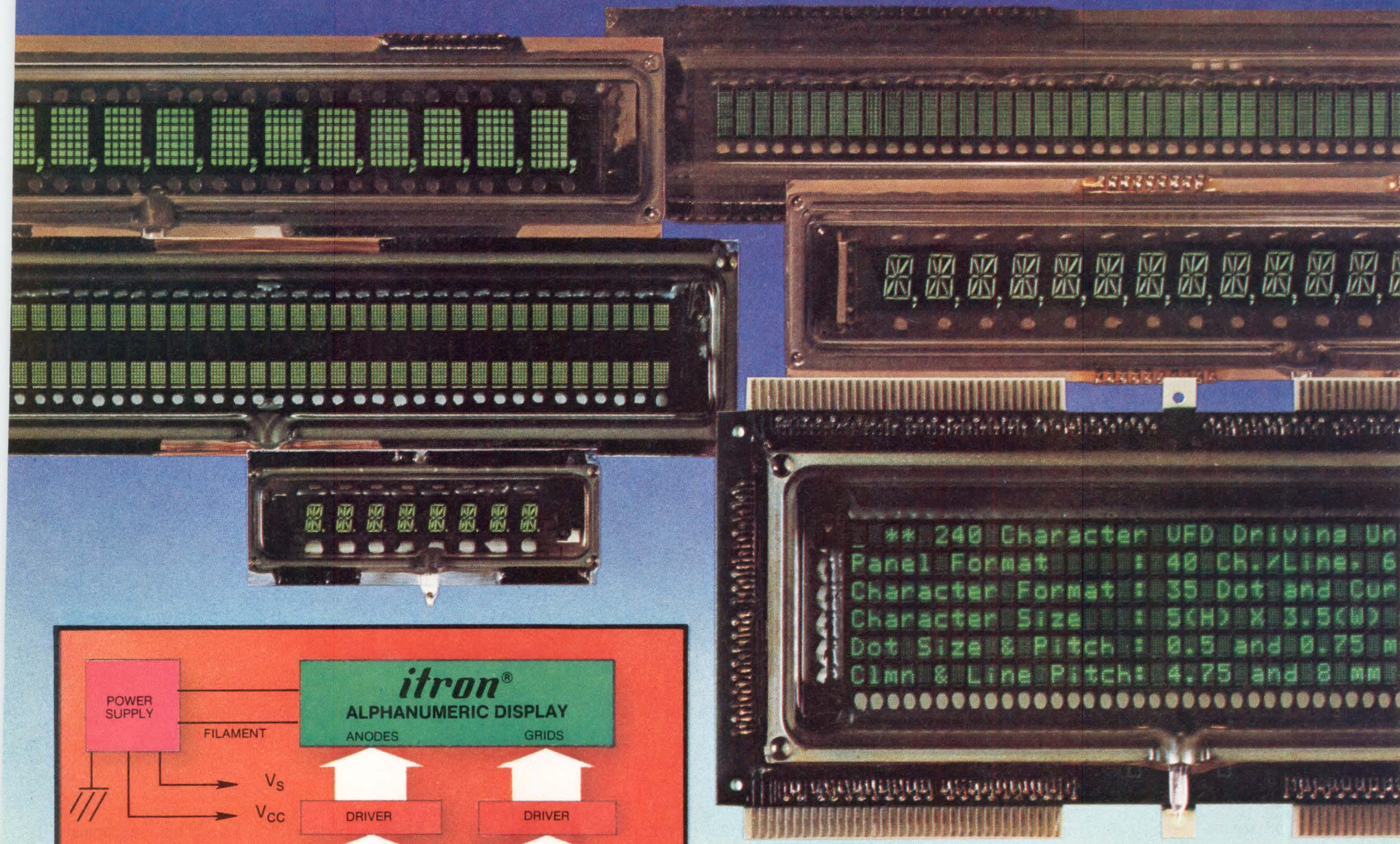

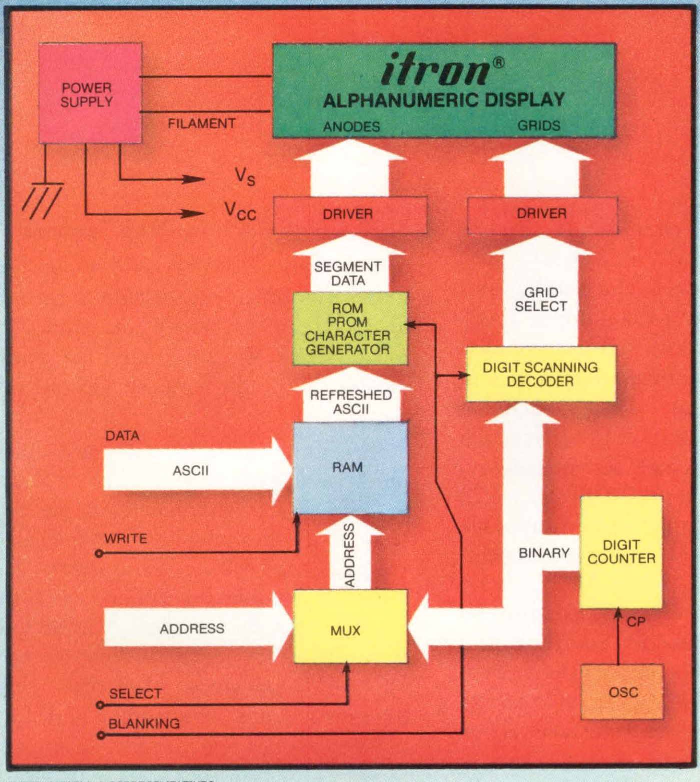

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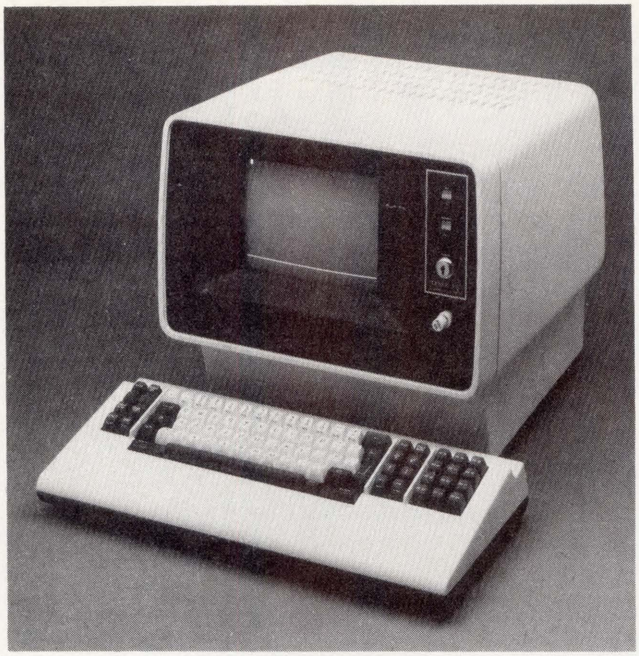


IBM 3278 compatible interactive terminal

Terminal Designs Facilitate Interaction With Computers

Human engineering factors and "user-friendly" considerations have influenced the physical design of two interactive keyboard/display terminals recently announced by Telex Computer Products, Inc. The units are the Telex 310, a Teletype[R] compatible ASCII terminal, and the 278E, an IBM 3278 compatible unit designed to fit easily on standard sized office desktops or in other areas where available space usually prohibits the use of such equipment. Both terminals include such convenience features as detachable keyboards, operator handrests, high definition displays, and integral self-diagnostics, status indication, and operator prompting.

Design Features

TTY Compatible ASCII Terminal

Model 310 is designed for applications such as education, timesharing, program development, and inquiry/retrieval for minicomputer based systems where there is a need for ASCII/TTY terminals. It has a high resolution 15" (38-cm) CRT, 7 x 11-dot matrix characters, and 24-line x 80-char format for a 1920-char display. A 25th line is provided for diagnostic information and operator prompting. The detachable keyboard has 128 ASCII characters plus numeric keypad. Keyboard layout is typewriter/3270/Telex 278 style and includes programmable function keys and typamatic repeating keys.

The microprocessor based unit includes self-diagnostic routines and supports ASCII communications from 110 to 9600 bits/s, asynchronous, half- or full-duplex. Interface is RS-232-C/current loop.

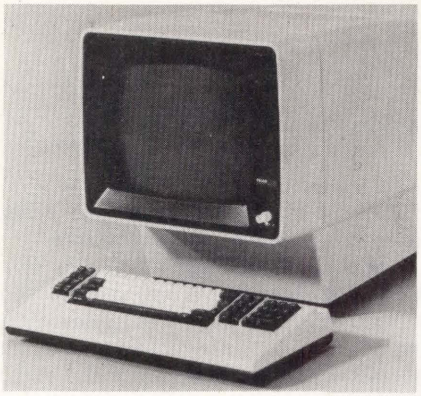
Optional features include reverse video, programmable brightness levels, and character/field and cursor blink. Dimensions are 18.5 x 16 x 19.4" (47 x 40.6 x 49.3 cm). Depth with keyboard is 29" (73.7 cm). Weight is 49 lb (22 kg). Power requirement is 117 Vac 60 Hz 1.0 A, or 235 Vac 50 Hz 0.5 A.

3278 Compatible Desktop Terminal

The compact 278E is said to be the first IBM 3278 compatible terminal designed to fit easily on standard office sized desktops, and is compatible with all features except for a lightpen.

The unit has a 9" (23-cm) diagonal nonglare screen that accommodates 1920 characters in an 80-char x 24-line display without sacrificing readability. Characters are switch selectable for upper case only or for upper/lower case. A 25th line is included for status indicators and operator messages. Integral self-diagnostics are standard. Field formatting modes are: protected, unprotected, alphanumeric, normal intensity, intensified field, nondisplay, or numeric lock.

The keyboard is attached by a 6-ft (1.8-m) cable. There are 12 programmable function keys on the main keyboard as alternate functions to the top row (numeric) keys, as well as 10 programmable function



TTY compatible keyboard/display terminal

keys on the data entry keypad. Keys for local print, cursor home, and cursor mode are also included, and an audible alarm fitted with volume and tone controls is provided.

As many as seven 278Es can be connected to a Telex 276 or IBM 3276 display/controller to form multistation clusters for data entry or inquiry/retrieval operations. The terminal can also be connected to an IBM 3274 controller for use in large cluster configurations. The unit can support printers with speeds ranging from 40 char/s to 400 lines/min. When connected to an appropriate IBM controller, the terminal can work under systems network architecture (SNA) and synchronous data link control (SDLC).

Maximum dimensions for the console are 15.75 x 15.25 x 15″ (40 x 38.7 x 38.1 cm) and for the keyboard 19 x 3 x 8.5″ (48.3 x 7.6 x 21.6 cm).

Price and Delivery

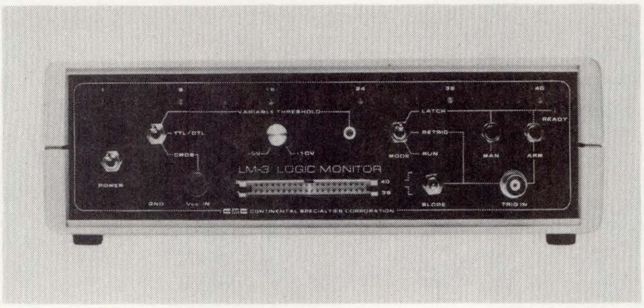
The 310 ASCII compatible terminal is priced at $1250 per single unit or $900 in quantities of 100 or more. Delivery is 30 days ARO.

The 278E is priced at $2200 in single-unit quantity, with delivery 60 days ARO beginning third quarter 1980. Lease plans are available. Telex Computer Products, Inc, 6422 E 41st St, Tulsa, OK 74135. Tel: 918/627-1111.

For additional information circle 199 on inquiry card.

See at NCC Booth 2553

Triggerable Logic Monitor Tracks Up to 40 Points Simultaneously



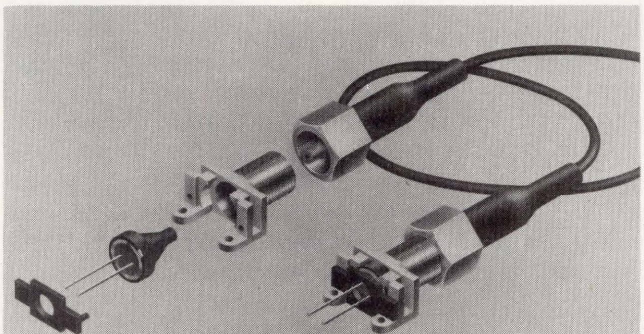
Any logic family and supply voltage can be studied with the LM-3 triggerable, 40-channel logic monitor. Connected to IC pins, test points, breakpoints, or bus line through a 40-conductor ribbon cable, the monitor displays measured data on 40 precision-threshold, high speed, high impedance logic state LED indicators, 1 for each channel. Logic threshold levels can be provided through a fixed 2.2-Vdc threshold for logic operation at standard TTL levels, by front panel control of a variable threshold between −5 and 10 Vdc at standard TTL levels, or by sampling a supply-dependent threshold (70% of the V_{cc} of the circuit under test) through front panel, dual banana jack connectors.

At the IC level, it is possible to connect all 40 pins of a microprocessor, UART, PIA, or memory, or any combination of leads; at the gate level, up to 40 logic tree checkpoints can be followed; at the bus level, 40 lines can be monitored; at the board level, 40 test points on a single board or 20 pins on a test board and 20 pins on a known-good board can be measured; and in a process control application, the status of 40 digital signal lines can be monitored simultaneously. For a system test application, 40-point patterns in the display LEDs can be compared against known-good patterns; and in a training situation, the display can be used either in standard fashion or as 40 separate remote logic indicators.

Main input specifications are impedance of 0.5 MΩ at connector and cable; response of 100-ns min pulse, 5-MHz max trigger frequency; and ±18-V max dc turn-on threshold voltage. The trigger input is switch selectable for rising or falling edge. Power requirements are 105 to 135 Vac, 57 to 63 Hz, 20 VA max or 215 to 250 Vac, 50 to 60 Hz. Unit size is 3 x 10 x 7" (7.6 x 25.4 x 17.8 cm); weight is 2.4 lb (2 kg). Op temp range is 0 to 40 °C. **Continental Specialties Corp,** 70 Fulton Ter, New Haven, CT 06509.

Circle 200 on Inquiry Card

Fiber Optics Detector and Emitter Provide Greatly Increased Speeds



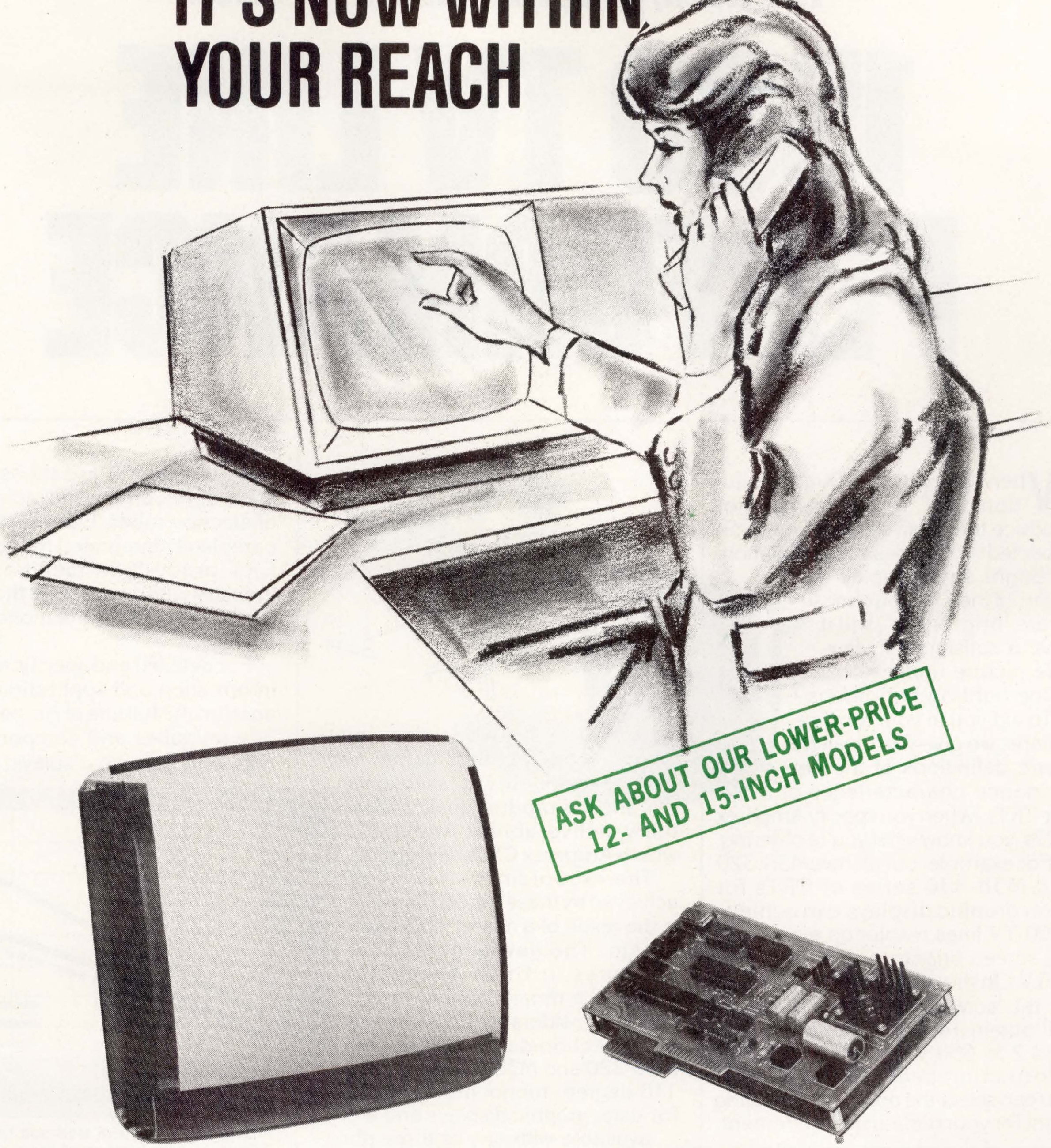
A PIN photodiode with 10 times faster response time than that of the next best previously available ferruled detector and an infrared LED with nearly twice the speed of existing ferruled emitters, the MFOD104F and MFOE103F, respectively, are designed specifically for fiber optics applications. Both are packaged in the company's fiber optic active component cases and fit directly into Optimate connectors (made by AMP Inc), which also provide rfi immunity. In 5-V data communications links, the detector functions at up to 110M baud and the emitter at up to 20M baud.

The detector has a typ response time of 2 ns at 20 V and 6 ns at 5 V. It can be used in analog fiber optics systems requiring bandwidths up to 100 MHz or in digital systems with speed requirements up to 200M baud. Max ratings at 25 °C include 100-V reverse voltage, 100-mW total device dissipation (0.57 mW/°C derate above 25 °C), −30 to 85 °C op temp range, and −30 to 100 °C storage temperature range. Electrical characteristics include 2.0-nA dark current, 200-V typ reverse breakdown voltage, 0.82-V typ forward voltage, 4.0-pF max total capacitance, and 50 fW/$\sqrt{Hz}$ noise equivalent power. Optical characteristics are 0.4-μA/μW responsivity and 2-, 4-, or 6-ns response time, both at 900 nm.

Max emitter ratings are 3-V reverse voltage, 100-mA continuous forward current, 250-mW total device dissipation at 25 °C (2.5-mW/°C derate above 25 °C), −30 to 85 °C op temp range, and −30 to 100 °C storage temperature range. Electrical characteristics at 25 °C are 50-nA typ reverse leakage current, 3.0-V min reverse breakdown voltage, 1.2-V typ forward voltage, and 45-pF typ total capacitance. Optical characteristics include 70-μW typ total power output from optical port, 0.48 typ numerical aperture of output port, 900-nm typ peak emission wavelength, 50-nm typ spectral line half width, and 15-ns typ optical turn-on and turn-off times. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.

Circle 201 on Inquiry Card

THE TRUE TOUCH SCREEN... IT'S NOW WITHIN YOUR REACH



To put the personal touch within everyone's reach, TSD is now providing high- and low-resolution 12- and 15-inch Touch Screens. In many cases the more economical low-resolution models provide all the touch power required for your application.

And why should you select a TSD Touch Screen? Because it is the best unit on the market today that can be activated directly by the touch of a finger. No previous experience necessary, no keyboard, no cumbersome light pens—just touch the screen to access a data base. And the screen matches the curvature of most CRT's.

To find out how the TSD Touch Screen can enhance the versatility and marketability of your product, contact Steven Sloan. He will gladly tell you more or have our local rep contact you.

TSD

TSD DISPLAY PRODUCTS, INC.

35 Orville Drive • Bohemia, New York 11716/Tel. 516-589-6800 • Telex 14-4659

CIRCLE 109 ON INQUIRY CARD

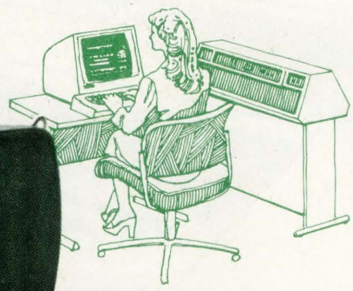
Amperex announces a new High Resolution CRT for data/graphic displays, with

1500 TV LINE PERFORMANCE

When you specify a "high resolution" CRT, it may or may not produce the clear, sharp images you expected: What does 'high resolution' or 'bright, sharp display' really mean? If the CRT you choose offers 'brightness', will it have a satisfactory, viewable picture under normal office lighting conditions?

To aid you in your tube decisions, we give you clear, numeric definitions of the performance characteristics of our CRTs. When you specify Amperex CRTs, you know what you're ordering.

For example, our all-new M38-320 and M38-330 series of CRTs for data/graphic displays can achieve 1500 TV lines resolution even at 20 ft-L screen brightness with Grid 2 at 630 V. On the other hand, if you need 40 ft-L screen brightness, you can still obtain 1400 TV lines by raising Grid 2 to 650 V. By referring to our information-packed spec sheets, you can select the optimum operating point for your particular requirement.



Anyone can "play the numbers game" with specs, but what still counts most is product quality/reliability/deliverability. And that's where Amperex CRTs really shine.

The extraordinary resolution achieved by these tubes (Figure 1) is the result of a new electron-gun design. The new gun has finer apertures in Grids 1 and 2 to produce a more compact beam that is considerably less affected by deflection-defocussing. Our M38-320 and M38-330 series are 110-degree, monochrome tubes for data/graphic displays and are available with any of three phosphors: P4, P31 and P39 (Figure 2.)

For improved reliability, we are utilizing the highly successful quick-heating cathode used in literally millions of consumer color TV tubes. With this cathode, warm-up time is only about 5 seconds.

A major reason for our ability to offer tubes of such high and well-defined performance is our total control over every step in their manufacture, from glass and phosphors to yokes and flyback transformers.

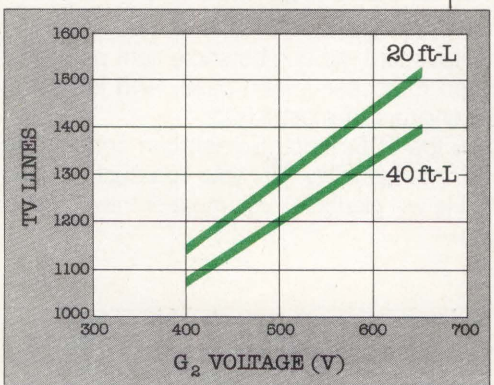


FIG. 1 — M38-320 and M38-330 CRT Resolution (TV lines) as a function of Grid #2 potential with P-4 phosphor.

We've spent 40 years as leaders in the development and manufacture of electron tubes. Ours are the most completely integrated monochrome CRT production facilities in the industry...and comprise the world's largest single source of monochrome CRTs.

For detailed and specific technical information and applications assistance on the full line of Amperex cathode ray tubes and components for data and graphic displays, contact:

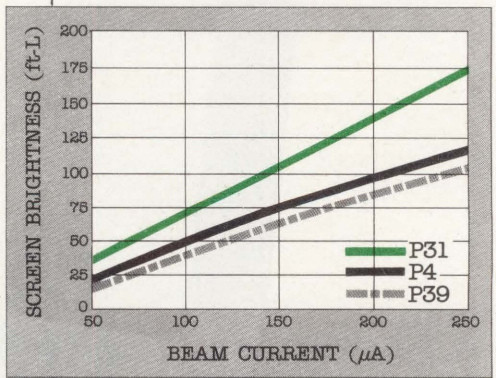


FIG. 2 — M38-320 and M38-330 CRT Screen Brightness as a function of beam current with screen potential 17 kV. (P4, P31 and P39 phosphors.)

Amperex Electronic Corporation, Display Products Group, Slatersville Division, Slatersville, Rhode Island 02876. Telephone: 401-762-3800.

Amperex®

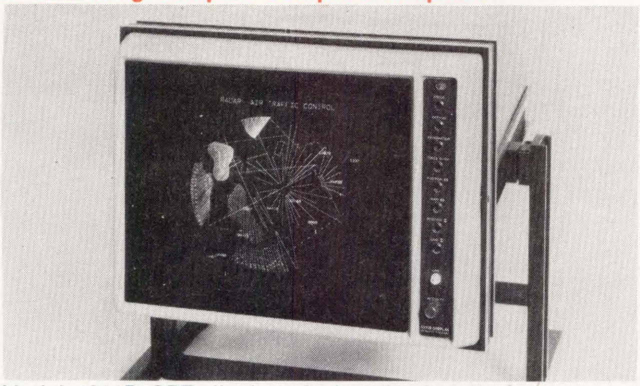
...dedicated to product excellence

A NORTH AMERICAN PHILIPS COMPANY

CIRCLE 110 ON INQUIRY CARD

PRODUCTS

High Resolution CRT Display Capable Of Providing Complex Computer Graphics

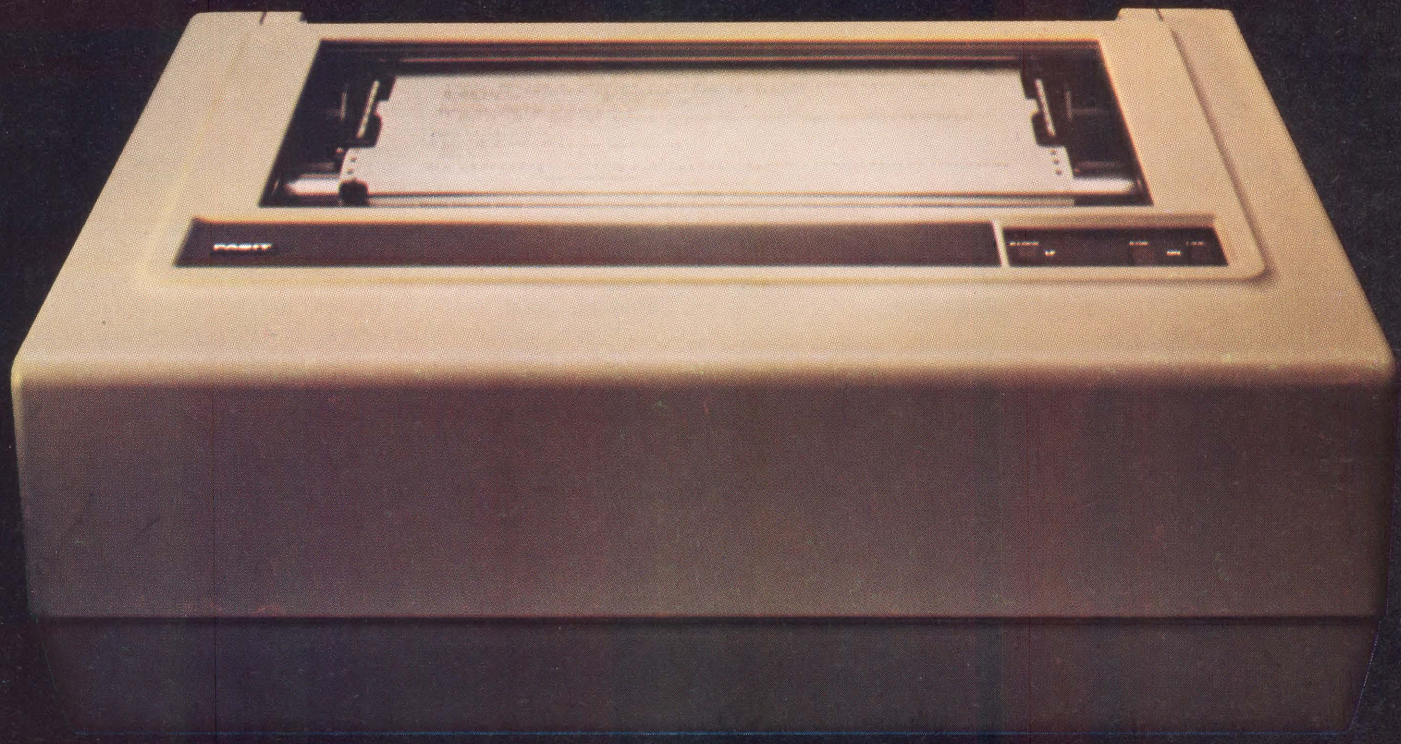


Model 1311B CRT display, designed primarily for use as a graphics computer peripheral, has resolution of 24 lines/cm at center screen with minimum corner defocusing. Using a 14" (35-cm) diag screen, unit includes high speed deflection circuits, fast rise time Z-axis amplifier, and regulated power supplies.

Spot resolution of the display is 0.43 mm. The spot remains well-focused on all parts of the screen, which solves the problem of writing many characters around the picture edges, while showing great detail in curves, graphs, or diagrams. An aluminized screen with 28.5-kV accelerating potential provides sufficient brightness to assure a crisp presentation of complex computer graphics under adverse lighting conditions. Image quality is maintained with a contrast control circuit which assures constant intensity with variable contrast. A flat, optical glass contrast filter eliminates trace diffusion and minimizes glare to provide sharp traces and high contrast.

Maximum picture detail with minimum flicker is obtained by the display's ability to make any size on-screen movement in less than 500 ns including settling time. Rise times of both X and Y amplifiers are less than 75 ns and the Z-axis amplifier has a rise time of less than 25 ns. The electrostatically deflected CRT requires only 115-VA power max. Yokeless, electrostatic deflection also simplifies operation by eliminating geometric correction circuits and unnecessary delay lines while reducing power requirements and weight. **Hewlett-Packard Co**, 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 202 on Inquiry Card



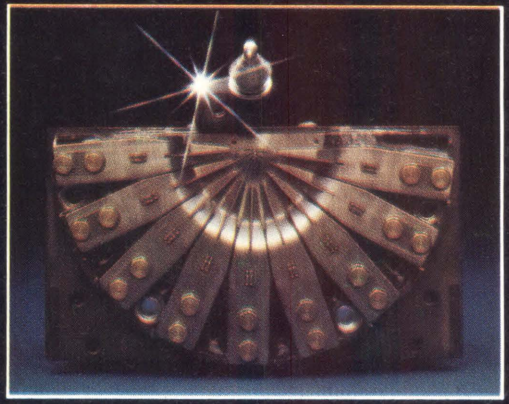
THE FACIT 4540 PRINTER REALLY USES ITS HEAD.

The printhead on the Facit 4540 Serial Matrix Printer is so advanced, it practically thinks for itself.

A new concept of printhead design uses 9 stored force flexible hammers to print a 9 x 9 dot matrix pattern bi-directionally at 250 cps.

The printhead movements have been reduced to a minimum. The printing principle assures extraordinarily long printhead life. With no adjustment, no lubrication and practically no wear. In fact, outstanding sharp and consistent printing results are guaranteed for more than a minimum of 500 million characters before any service might be required on the printhead.

The Facit 4540 is a prime example of the integration of mechanics and electronics which has made Facit peripheral data products world famous.



Our revolutionary printhead makes Facit 4540 a matrix printer with line printer speed.

Write for more detailed information on how the 4540 Printer can get the most out of your system.

Facit, Inc., 66 Field Point Road, Greenwich, CT 06830

FACIT
DATA
PRODUCTS

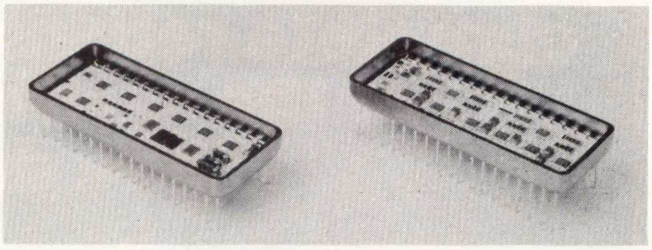
CIRCLE 185 ON INQUIRY CARD

DIGITAL DATA COMMUN'CATIONS LINE MONITOR AND DIAGNOSTIC AID

DLM III, available in a passive model with an 8k memory that provides full monitoring and trap capabilities and an interactive model that also supports data transmission and performs bit error rate tests, contains a 5" (12.7-cm) CRT screen for visual fault analysis, supports an external ASCII serial printer, and can accommodate TapeTrap, a programmable fault storage unit that selectively stores up to 1M-char on a 3M cartridge to allow capture of questionable transmission streams for fault analysis. The portable, self-contained unit weighs 17 lb (8 kg) making it suitable for hand carrying. Key features include bit or byte protocols including TTY, BSC, SDLC, NRZI, HDLC, BDLC, DDCMP, ADCCP, and X.25. Selectable synchronous and asynchronous data rates range from 50 to 19,200 bits/s; transmission modes provide half- or full-duplex transmission, receive only and send only; and codes include any 5- through 9-level code (including parity) such as EBCDIC, ASCII, or Baudot. Stream mode loads data without framing and is useful for resolving unknown asynchronous data by bit shifting; asynchronous transmission allows selection of 1, 1.5, or 2 stop bits/char; parity is selectable as odd, even, none, all 1s, or all 0s. Memory captures up to 250 displayable lines when monitoring transmission streams. **Digi-Log Systems, Inc,** Babylon Rd, Horsham, PA 19044.

Circle 203 on Inquiry Card

2-MODULE HYBRID MULTIPLEXED 14-BIT S-D, R-D CONVERTER



HMSDC-8700 converts 4 synchro or resolver channels to 14-bit digital data. The 2-module system is comprised of a 4-channel input processor module and a central converter module. Multiple input modules can be used with a single central converter for increased capability and reduced cost; the central converter can be replaced with an A-D converter and a microprocessor. The design's algorithm achieves accuracies of 5.2 arc minutes and conversion times of 100 μs max per channel. All common synchro and resolver line to line voltages and frequencies are available. Signal and reference input channels can be interconnected in any combination, including frequency; either module can be interchanged with its discrete module counterpart in the MSDC-700 multiplexed series. Differential solid state signal inputs with substantial common mode rejection eliminate the need for transformer isolation in most cases. **ILC Data Device Corp,** Airport International Plaza, Bohemia, NY 11716.

Circle 204 on Inquiry Card

CIRCLE 115 ON INQUIRY CARD

PRODUCTS

BANDSPLITTING 9600-BIT/s MODEM WITH MULTIPLEXING FOR FOUR TERMINALS

Permitting several terminals and/or modems at one location to share one line, the microprocessor controlled DL9600 allows users to combine up to 4 medium speed channels over a single high speed line. Each channel operates independently. The unit saves multiple line costs and eliminates need for separate modems for each. Inputs can be any combination of 2400-, 4800-, and 7200-bit/s channels. The automatic equalization unit can withstand line transients lasting up to 2 s without retraining. It operates point to point in full duplex on a 4-wire 3002 private line at 4800 or 9600 bits/s, switch selectable. All digital filters eliminate drift and provide error rate of <1 bit in 10^6 at 9600 bits/s on an unconditioned line with a signal to noise ratio of 22 dB. Low power consumption results in less stress on components and lower failure rates. MTBF is 15k hours. Self-testing capabilities include digital and analog loopback of remote unattended units. Operator can perform both local and system diagnostics and can select all mark or all space transmission. There are 15 front panel switches and 9 LED indicators, including one to signal that the telephone line is degrading. The modem is packaged in a 3.5 x 17.5" deep (8.9 x 44.4-cm) rackmount or tabletop unit. **Infotron Systems Corp,** Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003.

Circle 205 on Inquiry Card

OVERTEMPERATURE PROTECTION SYSTEM FOR DEC SYSTEMS

C-XX is a complete overtemperature protection system designed for all std DEC minicomputer and mainframe systems. Operating automatically in attended or unattended mode, the unit produces a loud audible alarm to advise computer room personnel to take action when sensor detects the first temperature limit of 79 °F (26 °C). An optional control function is provided for external customer alarm or standby air conditioning system actuation during a detected overtemperature condition. Automatic total power shutdown occurs at the second overtemperature limit of 83 °F (28 °C), for all equipment powered via the DEC std power distribution/control system in the cabinets to which the unit is connected. The operator is given the opportunity to gracefully terminate computer software operation while manually overriding the automatic power shutdown function, during an overtemperature condition. Factory-set first and second overtemperature limits can be changed by the customer via a simple procedure. An overtemperature incident is locked in the unit until it is reset. Fully compatible with all DEC standard equipment and systems, the unit installs in a few minutes with no tools or special skills. The system consists of a small desktop control unit connected by a 25' (7.6-m) cable to a temperature sensor which is suspended in the circulating air stream inside the computer equipment cabinet. A second 25' length of cable links the control unit to the cabinet power distribution and control system for overall system power shutdown, via a 3-pin mate-n-lock connector. **Nassau Systems,** PO Box 19329, Cincinnati, OH 45219.

Circle 206 on Inquiry Card

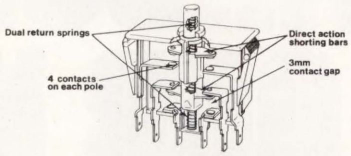
BELL COMPATIBLE 2400-BIT/s SMALL SYNCHRONOUS MODEM

TATA201C is an LSI circuit data modem that transmits and receives 2400-bits/s synchronous, serial binary data half-duplex over the 2-wire DDD switched network or private line, and full-duplex over a 4-wire private line. A line control card converts from private line to DDD version. End to end compatible with the Bell 201B and 201C data modems and 801 automatic calling units as well as T201C modems, it may be intermixed with other DDD or private line modems in the multimodem mounting. Units can be configured for adjustable, programmable, permissive, or fixed loss loop transmit level applications. A differentially coherent, 4-phase modulation technique provides improved tolerance to phase jitter. A switch selectable, internal, antistreaming timing circuit inhibits the request to send signal, automatically removing a streaming terminal in a multipoint system. Test features include analog loopback, digital loopback, local self-test, and end to end self-test. Front panel LEDs offer continuous visual status of terminal leads and internal circuits. Five front panel test switches—RO, AL, ST, RT, and DL—are used in conjunction with the visual indicators to enable rapid isolation of system malfunctions. **Rixon, Inc,** 2120 Industrial Pkwy, Silver Spring, MD 20904.

Circle 207 on Inquiry Card

LINE INTERRUPT SWITCH FOR WORLDWIDE SAFETY STANDARDS

F80 series is designed with 3-mm contact gap, 4 contacts on each pole, and 2 return springs to insure positive line interruption when switch button is released. Electrical ratings include 10 A/250 Vac, ¾ hp 125 Vac, 1½ hp 250 Vac (F81), 16 A/125/250 Vac, ¾ hp 125 Vac, 1½ hp 250 Vac (F82), 0.1 A 125/250 Vac with gold crosspoint contacts for low energy switching (F83), and combination of any types (F84). Switch case housings include basic case with exposed buttons or case with button protected between parallel baffles to prevent accidental actuation. Contact variations include version A—2 circuits, spst NO DM (2 form X contacts); J—2 circuits, spst NO DM (1 form X contact), spdt DM-DB (1 form Z contact), and D—2 circuits, spst, NO DM (1 form X contact), spst NC DB1 form Y contact). Version X has 1 spst NO DM (1 form X contact), Y consists of 1 spst NC DB (1 form Y contact) and Z provides 1 spdt DM-DB (1 form Z contact). All switches are front mounted by snapping into a 14 x 37-mm cutout in a panel ranging from 1.14 to 2.54-mm thick. Terminal sizes include a 6.35-mm and 4.75-mm standard male type that accepts push-on connector. Sizes may be mixed on one switch to assist in wiring identification. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60085.



Circle 209 on Inquiry Card

IT'S A GOOD CARTRIDGE WHEN YOU SEE OUR NAME ON IT.

AND EVEN WHEN YOU DON'T.

Chances are, the data cartridge in your system is ours. Even though it may not say so. That's because most of the world's top manufacturers of systems like yours specify our 3M Data Cartridges.

Why? Because we build more quality performance features into our cartridges than anyone else. Features that computer builders know will bring out the best in their equipment. Like a metal base plate that helps maintain constant tape speed and tension because it's unaffected by changing environmental conditions.

Which means accurate playback of data even when it's recorded on one machine and played back on another.

You see, systems manufacturers know a good cartridge when they see it. And we think you will too. Even if our name's not on it.

Check with your systems manufacturer when you need additional supplies. Or simply call 800-328-1300 for more information. (In Minnesota, call collect: 612-736-9625.) Or write: Data Products, 223-5E, 3M Company, St. Paul, MN 55101.

3M

CIRCLE 124 ON INQUIRY CARD

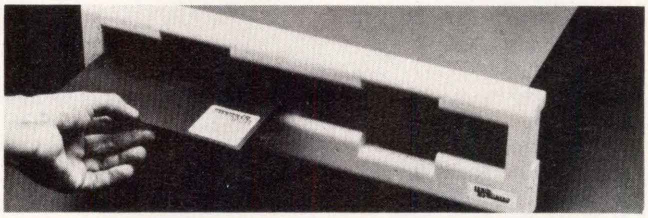
30-CHAR/s TELEPRINTER AND 600-LINE/MIN BAND PRINTER

A 300-baud unit, the 3365 Teleprinter features extensive LSI circuitry, a matrix printhead with a life cycle exceeding 200M char, and fewer mechanical functions for dependable performance. Both RO and KSR versions are available. For flexibility, unit operates at 10 or 30 char/s in half- or full-duplex mode with optional parity capabilities. The pinfeed utilizes full 132-char lines, consisting of 13 char/in (5/cm) on 12 x 8.5" (30 x 21.6-cm) fanfold paper, which, when serrated margins are removed, converts to 11 x 8.5" (28 x 21-cm) size. The printer provides an original and 2 duplicates. Built-in self-test programs and 5 plug-in components reduce downtime. A solid font impact band printer, the 3450 operates at 300 or 600 lines/min. Features include microprocessor based electronics, friction-free hammers, custom IC hammer drivers, and steel print band. Accuracy of the hammer along with simplicity of mechanics assures reliable print quality to 6 copies. Print band can be changed by the operator in <1 min. Output is easily read through a large window, while paper and ribbon motion and paper out is detected by sensors. Long-life ribbon cartridges reduce handling and make ribbon loading quick and simple. This unit's built-in diagnostic system has a digital display that constantly monitors printer status, allowing rapid identification of a fault and enabling the operator to determine the feasibility of local correction. Equipped with a 64-standard upper case char set band for maximum speed, the printer provides a 96-char set band with lower case as an option. **General Automation,** 1055 S East St, Anaheim, CA 92803.

Circle 208 on Inquiry Card

DEC/IBM COMPATIBLE DOUBLE-DENSITY, DOUBLE-SIDED FLOPPY DISC SYSTEM

Compatible with all DEC and IBM diskette formats, including IBM double-density, double-sided, model 480 reads and writes on both sides of industry standard 8" (20-cm) diskettes for a formatted capacity of 1M bytes/diskette, or 2M bytes of online storage. Hardware, software, and media compatible with LSI-11 and PDP-11 computers, the system allows users to conveniently transfer data and programs between DEC and IBM computers. Capability to transfer utilities and applications programs written for IBM machines directly to DEC computers, and vice versa, forms an inexpensive method of interchanging data and programs between systems. Features include built-in hardware bootstrap, offline diskette formatting, and "Hyperdiagnostics," a library of built-in user selectable routines that perform system self-tests independent of the computer. Diagnostics are particularly useful for performing incoming inspection or diagnosis without tying up computer or test equipment resources. The unit is packaged in a low profile 5.25" (13.33-cm) chassis for easy rackmounting or tabletop operation. Simple operation and complete documentation facilitate system integration. **Data Systems Design, Inc,** 3130 Coronado Dr, Santa Clara, CA 95051.



Circle 210 on Inquiry Card

Cartridge shot travels the length of a gun barrel while a 16-bit Plessey Miproc executes over 14000 instructions.

If your application needs a fast real-time processor or you have to cope with high data rates, then you need Miproc. The same goes for very fast interrupt response times. Because Miproc is the fastest there is. Anywhere.

Only Miproc has the dedicated get-up-and-go microcomputing power to free you from the hassles of DIY, and all that entails.

In industrial, university, military and government applications around the world, Miproc is handling all kinds of high speed computing tasks that would otherwise need multimicro systems.

It's now available in commercial and military versions, with an extended range of memory cards, processor enhancements, digital and analogue interfaces and software development tools. With its 250 nanoseconds macroinstruction cycle and its ability to handle data at 10 megawords a second, context changes in less than 2 microseconds, Miproc is the straightforward approach to no-nonsense high speed processing. Discover today how Miproc can make life easier for you by contacting your nearest Plessey Microsystems sales office.

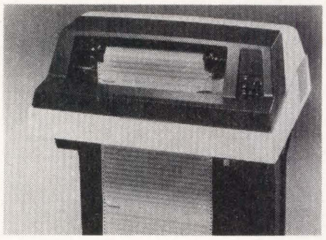
PLESSEY MICROSYSTEMS

Plessey Microsystems Inc., 19546 Clubhouse Road, Gaithersburg, Maryland 20760.
Telephone: (301) 840 9455 & 948 2791 TWX: 710 828 9708 & Irvine, California (714) 540 9931.
France: Paris (01) 776 43 34. Holland: Noordwijk 01719 19207. Germany: Munich (089) 23 62 270. Japan: Eiji Kitahara, Tokyo 244 3782. UK: Towcester (0327) 50312.

654 2086

300-LINE/MIN BAND PRINTERS AND SUBSYSTEMS

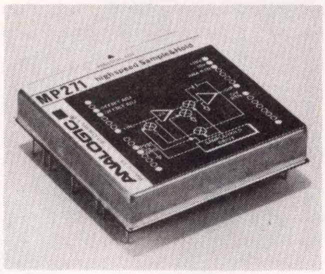
Available for integration into microNova, Nova, Eclipse, and Commercial Systems computers, models feature high quality printing, reliability, and built-in diagnostic displays. Design features include friction-free hammer actuators, low power consumption, and a minimum of mechanical parts which permit cooler operation and increased reliability. In addition, high energy magnets, custom IC hammer drivers, and steel band font carrier contribute to performance. The easily replaced steel band font carrier provides accurate vertical and horizontal registration of characters, and offers a choice of fonts. LED diagnostic display records printer cycle in event of offline condition, allowing unit to run independently of computer system for user correction of common fault conditions. Models 4323 and 4324, designed for microNova systems, feature forms length selector, 12-channel direct access vertical format unit, forms receiver tray, 30′ (9-m) I/O cable, and are pedestal mounted. Built around these models, the 4325 and 4326 include a programmed I/O controller for operation with Nova and Eclipse systems, and the 4327 and 4328 also include a data channel controller. Commercial Systems models 9260 and 9261 are programmed I/O subsystems, and 9262 and 9263 include a data channel controller. All come equipped with either 64- or 96-char sets. **Data General Corp,** Rt 9, Westboro, MA 01581.



Circle 211 on Inquiry Card

PRECISION HIGH SPEED SAMPLE AND HOLD AMPLIFIER

Intended for high resolution, high throughput applications, the MP271 features linearity of 0.003% and feedthrough of 0.001% at 500 kHz typ. The 2 x 2″ (5 x 5-cm) module with aperture uncertainty of 0.2 ns, acquisition time of 1.0 μs to 0.005%, and pedestal variation of $\pm$0.002% max, $\pm$0.003% linearity, is suited for use in data acquisition systems with sampling rates up to 300 kHz and resolutions up to 16 bits. Low hold mode feedthrough significantly increases system throughput by allowing the A-D conversion time to overlap the multiplexer switching time without degrading system accuracy. The unit's 2-μV/μs droop rate guarantees high accuracy even when used with a slower speed moderate cost ADC. Max throughput is achieved by switching the multiplexer to the next channel while the S/H holds the previous channel value. The multiplexer settles fully to the new value while the A-D conversion is completed on the previous channel value. At the end of conversion the unit switches to sample mode; it acquires the new input and the new conversion is triggered. High frequency components present at the S/H input come from ultrafast multiplexer switching of full scale step inputs or high frequency data. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.



Circle 212 on Inquiry Card

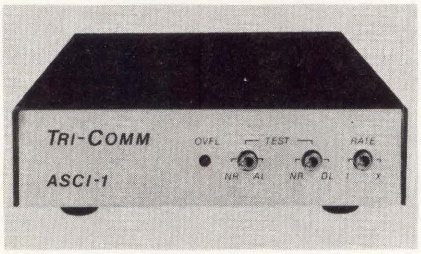
CIRCLE 128 ON INQUIRY CARD

CIRCLE 129 ON INQUIRY CARD

PRODUCTS

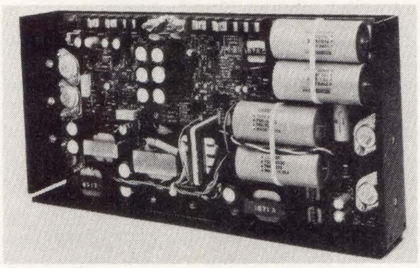
ASYNCHRONOUS-SYNCHRONOUS CONVERTER

Interface converter, ASCI-1, makes asynchronous terminals compatible with synchronous transmission systems. The unit will operate from 1200 to 19.2k baud. Loopback switches provide reliable diagnostics for isolating a malfunction in any part of the system, or confirming proper operation of the network components. Low power CMOS design allows the unit to operate on power from input signals of the terminal and modem. **Tri-Communications Industries, Inc,** 1555 Main St, Danbury, CT 06810.



Circle 213 on Inquiry Card

5-OUTPUT OPEN FRAME SWITCHER



Four outputs on 5HMP meet regulation specs equal to or better than 0.5%; the fifth provides an 8.0% regulation spec. Other specs are 0.15% for 5-V/45-A, 12-V/5-A, and −12-V/5-A outputs, and 0.5% for −5 V/1 A. All are for 0 to 100% load change. Each output is capable of delivering its specified voltage and current. Total simultaneous output is 325 W. Dissipation is specified for 0 to 40 °C operation at full rated load and 0 to 70 °C at half rated load. **Sierracin/Power Systems,** 20500 Plummer St, Chatsworth, CA 91311.

Circle 214 on Inquiry Card

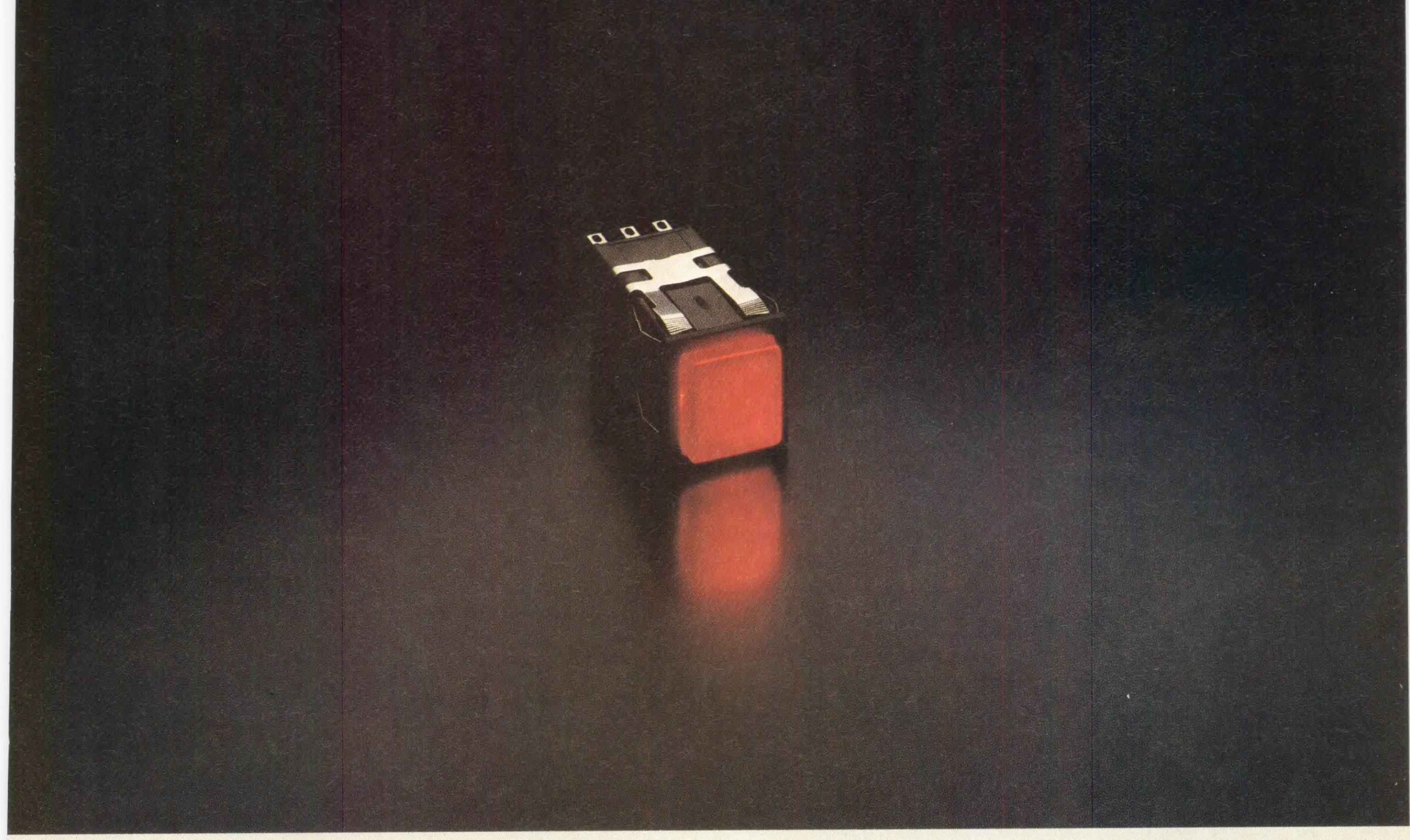
3.088M-BIT/s SIMPLEX MODEM

High speed modulator 2300T is a transmitter only version that operates point to point at speeds of 1.544M and 3.088M bits/s over unloaded twisted pairs or coaxial cables at distances up to 7000′ (2134 m). Internally or externally timed, the unit contains a bipolar violation technique, a scrambler, and a bipolar transmission method. An alarm circuit and front panel indicator provide online diagnostic capability. **Avanti Communications Corp,** Aquidneck Industrial Pk, Newport, RI 02840.

Circle 215 on Inquiry Card

CIRCLE 131 ON INQUIRY CARD

The first LED pushbutton that's as bright as an incandescent, but doesn't burn out like one.



Our AML pushbuttons, indicators, paddles and rockers have a new light source. A unique, dual chip LED.

Like other LED's, this one will last a long time (its half-life is 100,000 hours or more). It resists shock and vibration. It uses only half the current of an incandescent. It will save you money on repairs. And comes in red, yellow and green.

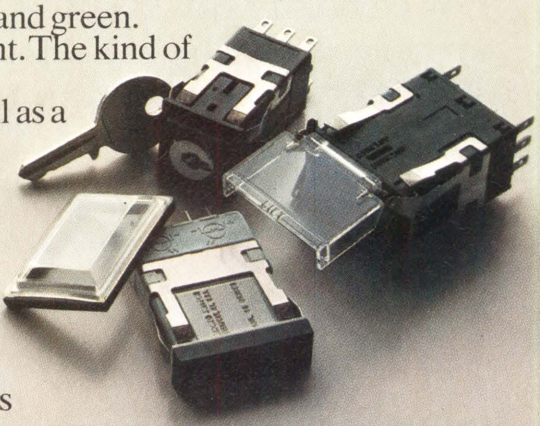
But unlike all other LED's, this one is very bright. The kind of brightness you'd expect from an incandescent.

And a special adapter makes it as easy to install as a standard T1¾ wedge base.

In addition to this one very 'bright' idea, we've made some other additions to the Advanced Manual Line. Like a keylock switch, a protective panel seal, and a switch guard.

Not to mention a new solid state LED annunciator, with more room for legends.

For details about these and other bright ideas for control panels, and the locations of our sales offices and distributors around the world, write MICRO SWITCH, Freeport, Illinois 61032. Or call 815-235-6600.



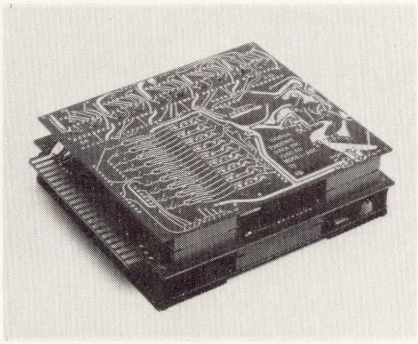
MICRO SWITCH
a Honeywell Division

Visit us at ELECTRO '80, Booth # 21, 51-57

CIRCLE 132 ON INQUIRY CARD

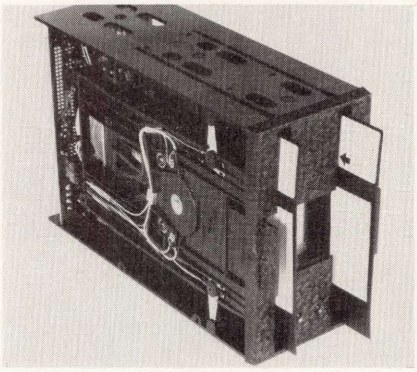
PRODUCTS

PRECISION A-D CONVERTER



Conversion time of 6 μs, accuracy of ±0.003% with 16-bit binary or 2's complement resolution, and linearity of ±0.0015% are provided by the ADC 1216F. Designed for digitizing high speed, broad band analog input signals, the converter incorporates a single foldback technique in conjunction with successive approximation conversions to achieve an equivalent conversion rate of 375 ns/bit. All output and control signals are fully TTL compatible. **Phoenix Data, Inc,** 3384 W Osborn Rd, AZ 85017.
Circle 216 on Inquiry Card

DOUBLE 5.25" FLOPPY DISC DRIVE



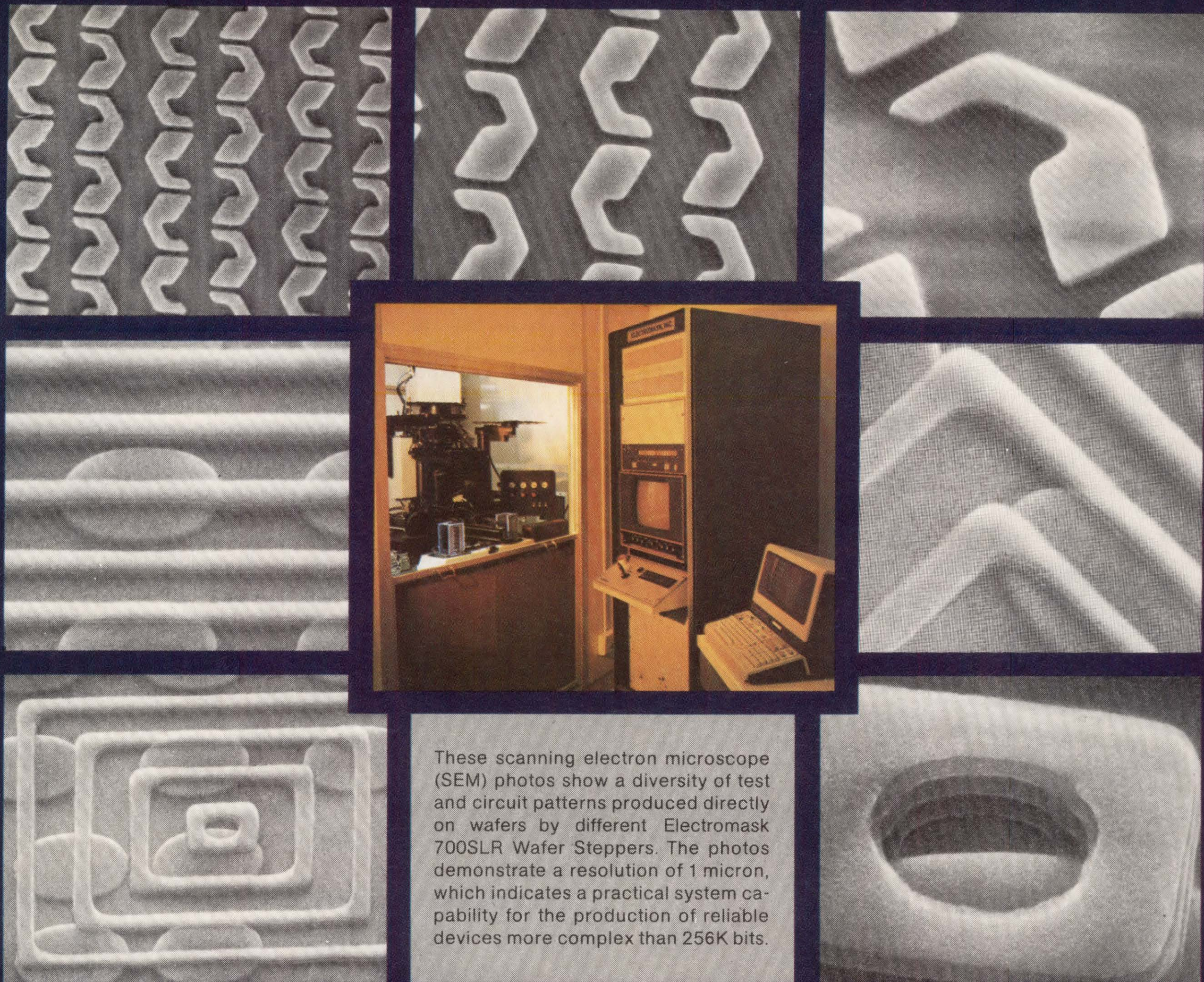
Handling 2 independent 5.25" (13.33-cm) diskettes while maintaining size and interface compatibility with other single 5.25" drives, "DAM" floppy model A-40 provides single-sided, dual-density recording on 40 tracks of each diskette. Track to track access time of 12 ms produces a random average seek time of 170 ms. Unformatted storage is 256k bytes/diskette or 512k bytes/drive. **T and E Engineering, Inc,** 1010 W 190th St, Gardena, CA 90248.
Circle 217 on Inquiry Card

PC BOARD TEST SYSTEM

Functional test system model 231 accomplishes testing functions using a high level test language. Controlled by a Motorola 6809, it is augmented by a high speed arithmetic processing unit. Multiple test stations can be serviced by a single central software development system for different devices under test. Software development package is written in ANSI FORTRAN IV. Test programs stored on a central computer may be downloaded to the system. **SIR-Atlanta, Inc,** 331 Luckie St, Atlanta, GA 30313.
Circle 218 on Inquiry Card

HANDHELD MODEM TESTER

Microtest internally generates 4 data patterns, including the std CCITT 511-bit pseudorandom pattern, and detects, counts, and displays errors via its LED display window. It troubleshoots problems in transmission lines and in most modems and data sets. Test points and display for RS-232 interface voltages are provided together with self-test capability, RTS and DTR control, force error, and operator controlled transmission. **Multi-Tech Systems, Inc,** 82 Second Ave SE, New Brighton, MN 55112.
Circle 219 on Inquiry Card



PRODUCTS

UNIVERSAL BAR CODE READER

Reading up to 8 bar codes and 3 code combinations (with Code 39[R]), model 9300 includes 1236 Ruby Wand[R] light pen. Code is selected through panel mounted program switches. Asynchronous serial data communication capability is provided. Control switches allow selection of transmission speed (110 to 9600 baud), 4 parity options, end of message, full/half duplex, and block transfer. Reader has dual RS-232-C interface for terminal and modem connection. **Interface Mechanisms, Inc,** PO Box N, Lynnwood, WA 98036.

Circle 220 on Inquiry Card

HIGH COMMON MODE A-D CONVERTER MODULE

A020 handles analog signal inputs for the IP11x, IP300, and DPM50 industrial I/O subsystems. As an isolated, 14-bit plus sign, selectable gain converter, it can be used with 16 2-wire or 8 3-wire inputs, and offers 14 selectable gain settings. Typ performance is up to 37 conversions/s for 60-Hz operations and 31 conversions/s for 50-Hz operation. Other specs are min of 500-V isolation and up to 150 dB of common mode rejection. **Digital Equipment Corp,** Maynard, MA 01754.

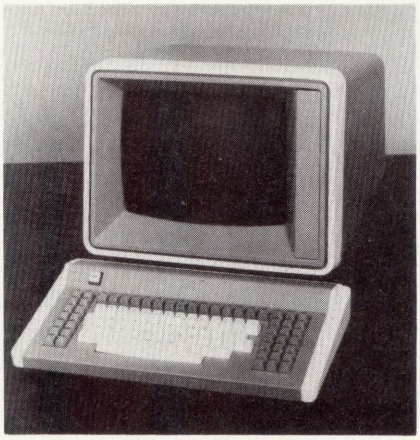
Circle 221 on Inquiry Card

PRECISION RESISTOR NETWORKS

Type T912 provides the pair characteristics and stability required by accurate amplifier, voltage reference, and precision bridge circuits. Constructed with Tetrinox™ resistance films, the networks have ratio tolerances from ±0.1% to ±0.01%; ratio tempcos of either 10, 5, or 2 ppm/°C; and ratio stability of resistance at full load (2000 h) within ±0.01%. All 12 models are available in the thin profile configuration. **Caddock Electronics, Inc,** 3127 Chicago Ave, Riverside, CA 92507.

Circle 222 on Inquiry Card

PROGRAMMABLE CRT TERMINAL



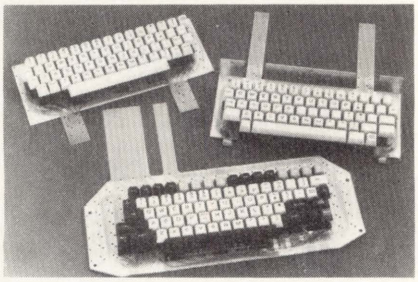
Satellite display terminal 850 includes up to 8k of P/ROM for programming and 4k or 16k of RAM for buffer and screen storage; 4k bits of EAROM are optional. Features of the intelligent standalone terminal include a separate current loop that enables the terminal to assume receive functions of a Telex machine, pass words, telephone numbers, and delimiters. The 15" (38-cm) screen has a display format of 80 char by 25 lines. **Megadata Corp,** 35 Orville Dr, Bohemia, NY 11716.

Circle 223 on Inquiry Card

PRODUCTS

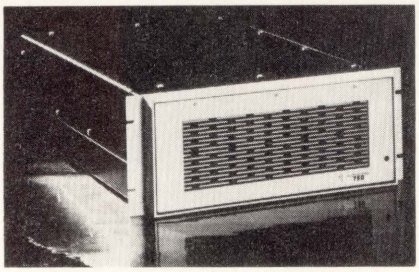
HIGH RELIABILITY MEMBRANE SWITCH KEYBOARD

Full travel alphanumeric keyboards that can be tailored to OEM applications use a membrane switch technology for a life rating of 50M operations/key and a contact bounce typically <2 ms. Modular FASTYPE™ units operate with a consistent force of 3 to 5 oz (0.8 to 1.4 N)/key and 5 to 7 oz (1.4 to 1.9 N)/space bar over a 0.150" (0.381-cm) travel. Key will not loosen or rattle in frames. Flextail terminations are std. **Chomerics, Inc,** 77 Dragon Ct, Woburn, MA 01801.



Circle 224 on Inquiry Card

4.8M-BYTE DISC MEMORY UNIT



Model 750 features a closed recirculating air system that provides extended operation is nonsevere environments without periodic maintenance. Head and disc enhancements double capacity of the model 700, providing capacity for 4.8M bytes max, without adding tracks or components. Available controllers allow attachment to DEC and Data General computer systems. **Digital Development Corp,** 8650 Balboa Ave, San Diego, CA 92123.

Circle 225 on Inquiry Card

FRACTIONAL HORSEPOWER DC MOTORS

Measuring 1.37" (3.48-cm) in dia, series 3540 and 3557 motors are furnished in ball bearing or sintered bearing versions with double-ended shafts. They are also available with optical encoders (15, 100, and 200 pulses/r) and screw-on gearheads with ratios ranging from 12:1 to 54,880:1. Power outputs are up to 15 W; 7 std nom operating voltages range from 6 to 32 V. Continuous duty ratings include speeds over 5000 r/min and stall torque up to 6.4 oz-in (0.04 N•m). **Micro-Mo Electronics, Inc,** 3691 Lee Rd, Cleveland, OH 44120.

Circle 226 on Inquiry Card

2-PORT INTELLIGENT MUX

DE-2 Data Express statistical multiplexer concentrates 2 asynchronous devices onto a single line. Features are total data transparency, ARQ error correction, and fast propagation of data using addressed char block. Buffering supports error correction and allows terminal data rates to temporarily exceed the modem composite speed. Diagnostics indicate status of the communications link; loop test mode allows data to be looped from the terminal through the multiplexer, and back. **Compre Comm, Inc,** 51 E Chester St, Champaign, IL 61820.

Circle 227 on Inquiry Card

CIRCLE 138 ON INQUIRY CARD

CIRCLE 139 ON INQUIRY CARD

Love at First Byte

A versatile 128K by 22 semiconductor memory on a single card... multi-card systems, too.

Not Ruggedized, but Rugged

Our hard nosed EMM/SESCO inspector has fallen in love with the new Model 3500 NMOS semiconductor memory... and so will you.

Although designed and priced for the commercial user, the 3500 is built with the same exacting care that has made EMM/SESCO's ruggedized memories so popular. It's fast, too, with 300ns access and 400ns cycle time. Even faster in the page mode.

Options Abound

Many options are available to make your task easier. These include ECC (single and multiple bit error correction), word or byte parity generation and checking, page mode, byte mode, error stop, LED failure isolation and display, and battery backup.

More Words or Less Words

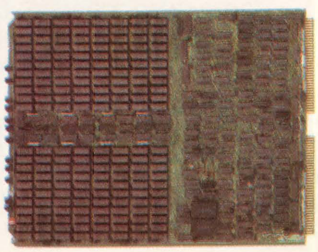
The 11.75″ × 15.4″ card can be configured with 128K words of up to 22 bits or 256K words of up to 11 bits. It can be depopulated down to 32K if that fits your immediate needs.

512K Word System

A 5¼″ high rack holds up to 4 memory cards, providing capacities to 512K × 22 bits, plus custom interface, self-test, cooling fans, and power supply.

Plenty of Memories

There are plenty of memories in store for you at EMM/SESCO. Such as a non-volatile Megabyte core memory system. A complete line of ruggedized memories for military and industrial use. Even a ruggedized version of Intel's popular iSBC* 80/10A microcomputer.



So when you're looking for memories... Buy SESCO... they work!

EMM SESCO

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CIRCLE 140 ON INQUIRY CARD

PRODUCTS

120-CHAR/s BIDIRECTIONAL PRINTER

Improving medium volume throughput for model 8000 interactive terminal systems, the desktop 3165 is available in two models. One uses a 7 x 7 dot matrix to print 64 ASCII or EBCDIC upper case char, the other prints 96 upper case and lower case ASCII and EBCDIC char using a 7 x 9 dot matrix. Unit accepts paper widths up to 17.3" (43.9 cm) and prints on 6 part forms. Horizontal spacing is 10 char/in (3.9/cm) in 132-char lines; vertical spacing is 6 lines/in (2.3/cm). **Harris Corp, Data Communications Div,** 16001 Dallas Pkwy, Dallas, TX 75240.

Circle 228 on Inquiry Card

LINE PRINTER CONTROLLER

DLP-II features an onboard long lines option that is switch selectable and enables data to be sent to a printer up to 3000' (914 m) from the computer. The 1-board unit provides interface for Dataproducts, Centronics, and DEC LA-180, as well as printers emulating any of these interfaces. Self-test capability simplifies installation and maintenance. Easy address change is another time saving feature. **Datasystems Corp,** 8716 Production Ave, San Diego, CA 92121.

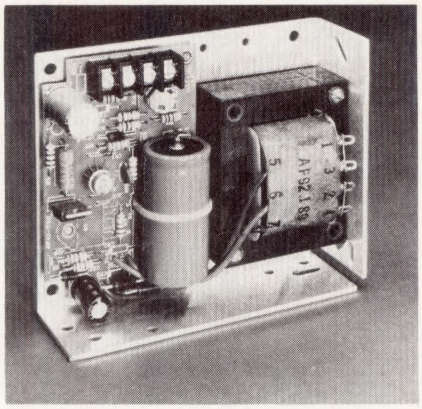
Circle 229 on Inquiry Card

TRANSIENT VOLTAGE SUPPRESSORS

Shunt devices, installed across power distribution lines, conduct small leakage current as long as the voltage across it remains below a preset level. When voltage exceeds the clamping level, the device conducts sufficient current to hold the voltage at the clamping level. Developed with silicon PN junction technology, units are coupled with heavy duty crowbar circuits to handle extended overvoltage conditions on the ac power system. **W. N. Phillips, Inc,** 356 Bacon St, Lake City, MI 49651.

Circle 230 on Inquiry Card

ECONOMY THIN PROFILE DC POWER SUPPLIES



Interchangeable with other manufacturers' units, openframe EAPS "U" series operate from an ac input of 103 to 130 V/206 to 260 Vac, 47 to 63 Hz. Output power ratings are 5 V at 3 A, 12 V at 1.6 A, 15 V at 1.5 A, and 24 V at 1 A dc. Regulation is ±0.05% for line and ±0.1% for load. Ripple is 5-mV pk-pk max. Furnished in industry std chassis, the unit's dimensions are 4 x 4.87 x 2.07" (10.1 x 12.37 x 5.26 cm). Features include full rated power to 50 °C. **Adtech Power, Inc,** 1621 S Sinclair St, Anaheim, CA 92806.

Circle 231 on Inquiry Card

CIRCLE 142 ON INQUIRY CARD

THE MOST FIELD PROVEN IS NOW THE MOST VERSATILE.

Telex introduces the new Tri-Density 6250 Tape Subsystem for OEM's.

In 1978, Telex introduced and delivered the first high speed 6250 BPI tape transport for OEM mini-computers. It lets you compact more data. In less space. At faster speeds. Since then we've built up more field proven reliability than any other 6250 OEM tape drive manufacturer.

Now this rack-mounted 6200 Series tape family has been expanded to include the 6253 tri-density tape subsystem. The high performance drive and formatter combines three densities—6250 BPI (GCR), 1600 BPI (PE), and 800 BPI (NRZI)—into a single unit. And as with all 6200 models, tape speeds of 50, 75 or 125 IPS are available. Telex formatters attach up to four 6200 Series drives and up to eight with an expansion option.

One key to the reliable operation of the 6200 Series is our patented Supr-Lite™ Capstan. It weighs only 1.9 grams, and combined with our patented new tape path, lets us use a smaller, more efficient drive motor. Tape handling at high program rates is improved.

Most importantly, the 6200 Series now offers you extreme versatility in matching and field converting a wide range of features and system options. The 800/1600 BPI dual density model 6240 can be easily field upgraded to tri-density. And such options as a 360/370 channel adaptor, high altitude and seismic feature, and dual speed capability will enhance your system configurations and performance many times over.

For more information about the 6200 Series—including its price/performance competitiveness—call your nearest Telex OEM representative. Or phone our OEM Marketing Department in Tulsa at (918) 627-1111.

***The innovation continues...* TELEX**

Telex® Computer Products, Inc.
Terminals/Peripherals/Data Entry and Word Processing Systems/OEM Products

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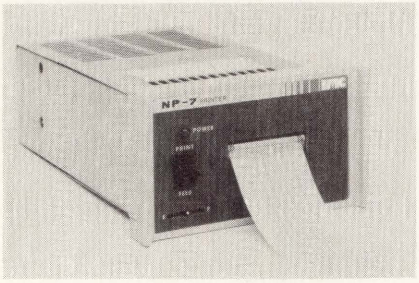
PRODUCTS

THERMAL NUMERIC PRINTER



Series NP-7 printers with up to 7 columns accept TTL BCD parallel data through rear connector and convert to 7-segment format for the monolithic printhead to print on 2" (5-cm) wide temperature sensitive paper. The only moving part is the paper advance mechanism. Print paper advance, test, polarity, digit blanking and standard inputs, busy and data hold outputs are available at the rear connector. Line density is 5 lines/in (2/cm), and max printing rate is 4 lines/s. **International Microtronics Corp,** 4016 E Tennessee St, Tucson, AZ 85714.
Circle 232 on Inquiry Card

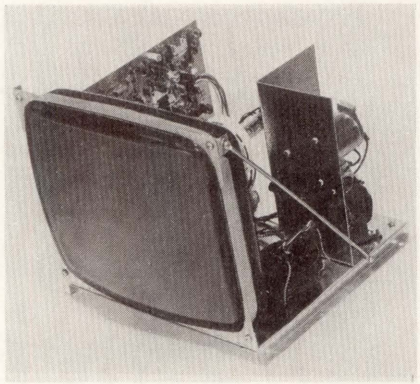
14- AND 16-BIT RESOLUTION ANALOG INTERFACE BOARDS

Analog input and I/O systems with choice of 14- or 16-bit A-D conversion have fully expandable multiplexer inputs with 8 differential or 16 single-ended channels. Hardware and software compatible with DEC's PDP-11 backplane, these peripherals function with the DEC RT-11 and RSX-11 operating systems. Software programmable gain amplifier PGH option for high level application has gains of 1, 2, 4, and 8; PGL for low level use gives gains of 1, 10, 100, and 500. **Data Translation, Inc,** 4 Strathmore Rd, Natick, MA 01760.
Circle 233 on Inquiry Card

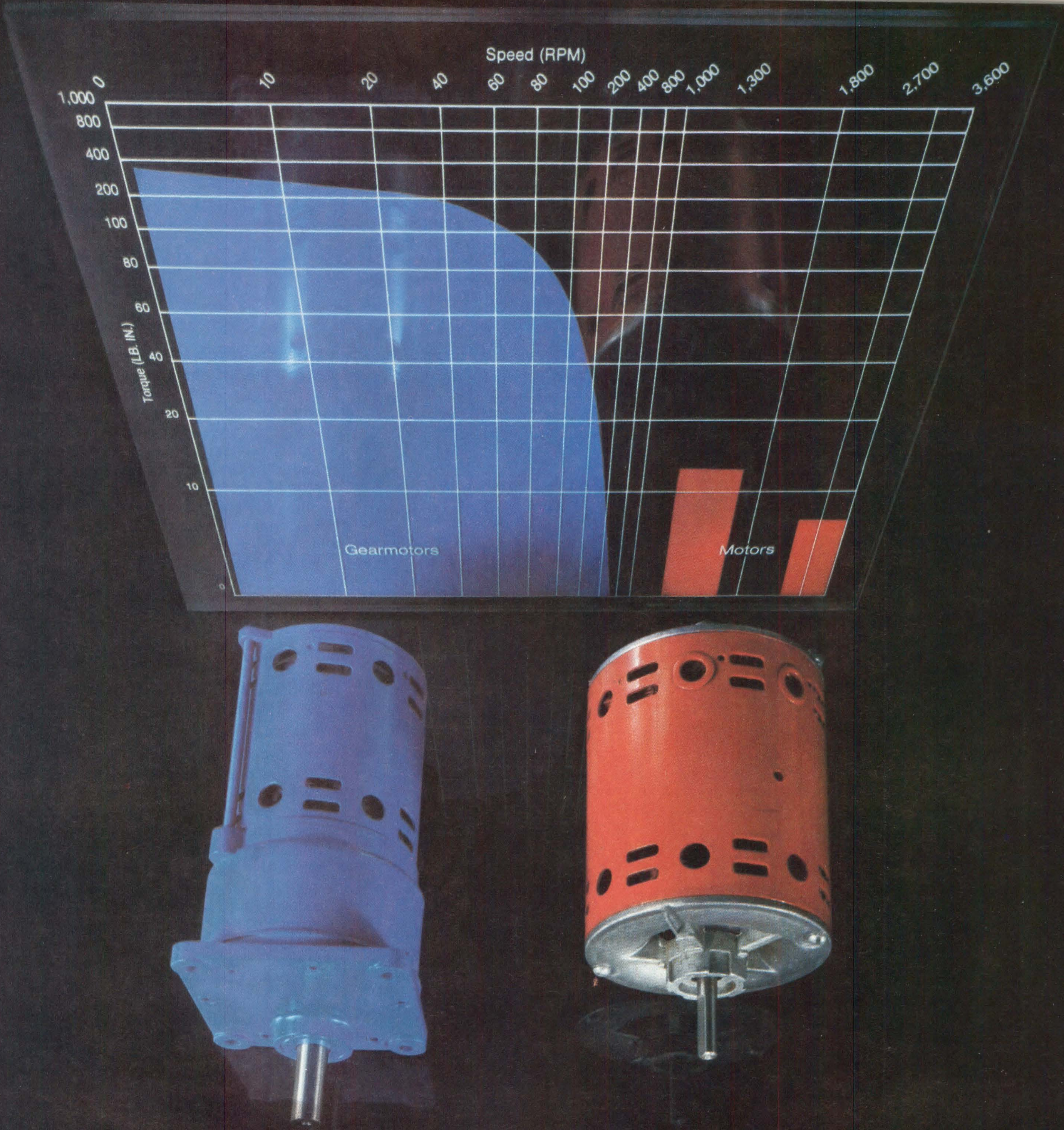
5.25" OEM FLOPPY DISC DRIVE

Single-sided CDC 9408 floppy disc unit is available in single- and double-density versions. Formatted capacities are 71.6k bytes in single-density and 143.3k bytes in double-density formats. IBM format compatibility is featured, as is industry standard mechanical and electrical interface compatibility. Head positioning is handled through a band stepper mechanism. **Control Data Corp,** Box O, Minneapolis, MN 55440.
Circle 234 on Inquiry Card

HIGH RESOLUTION RASTER CRT MODULES



Two CRT monitors are the 15" (38-cm) M15P1024H and 20" (51-cm) M20L512H, which respectively define 1024 and 512 lines in 1/60 s for non-interlaced operation or 2048 and 1024 lines in 1/30 s for interlaced operation; approx scan frequencies are 64 and 30.5 kHz. Separate synchronizing TTL inputs are provided. Modules handle video bit streams to 80M bits/s with the wide bandwidth video amplifier, and either ECL or linear video inputs for gray scale applications. **Video Monitors, Inc,** 3833 N White Ave, Eau Claire, WI 54701.
Circle 235 on Inquiry Card



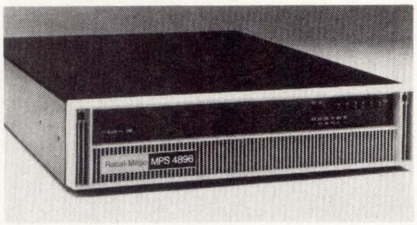
Drive at the right speed

If your speed-torque need falls within the blue or red areas of the chart, Robbins & Myers can get you the gearmotors or speed reducers, motors, and controls to give you the exact output that's right for your application. No compromise. Request Catalog D-1120 for full details on: **Gearmotors.** Comprehensive line of face and foot mounted spur gearmotors rated to 1/6 HP. **Speed reducers.** Three basic spur gearheads with 226 standard ratios from 3.5:1 to 2544:1, with output torques from 16 to 176 in. lb. **A.C. Subfractional HP motors.** Specially sized for OEM needs up to 1/2 HP with millions of standard design variations in diameters from 3 1/8″ to 4 11/16″. **Variable speed control.** SCR controls for DC gearmotors give constant torque performance from near zero to rated rpm. Get expert help! Electric Motor Division, Robbins & Myers, Inc., 1949 Lagonda Ave., Springfield, OH 45501. Tel. 513-327-3329.

ROBBINS MYERS

CIRCLE 146 ON INQUIRY CARD

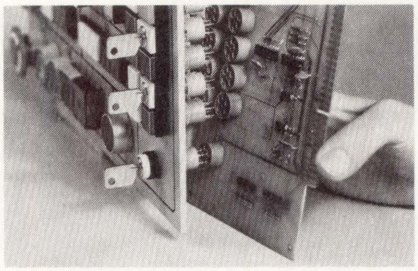
4800/9600-BIT/s REMOTE SITE MODEM



MPS 4896 Fastran, when installed at remote sites, transmits data at 4800 bits/s and receives data at 9600 bits/s, operating on less expensive unconditioned multidrop lines. It is useful when the bulk of the data is sent to remote sites and responses are short. Equipped with a microprocessor digital equalizer, in conjunction with Fastran high speed training, the modem provides a 30-ms RTS/CTS response time. Half-duplex operation occurs over 4-wire dedicated unconditioned channels. **Racal-Milgo, Inc,** 8600 NW 41st St, Miami, FL 33166.

Circle 236 on Inquiry Card

PCB CONNECTORS FOR LOWER LEVEL SWITCHES



Switches may be wave soldered directly to the PC board, eliminating hand soldering and prewiring. Connectors with straight or 90° pins mate with low level and electronic switching elements in series 01, 11, 14, 21, 31, and 41 switches. They are permanently soldered to the PC board and pressed onto the switches already mounted on the panel. Low level switches are suited to current <100 A and 60 V. **EAO Switch Corp,** 255 Cherry St, Milford, CT 06460.

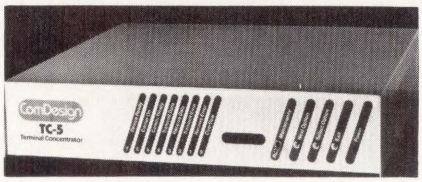
Circle 237 on Inquiry Card

100M-BYTE BACKUP FOR 8" WINCHESTER DISC

Providing reliable, large capacity backup for 8" Winchester drives, Mirror uses inexpensive std video cassettes with a total capacity of 100M bytes onto which the entire 10M bytes of data on the hard disc can be transferred in <10 min. The unit interfaces data signals on the disc to a separate customer supplied video cassette recorder of the VHS, Beta, or U-Matic format. The device will interface to a variety of host computers including Apple, TRS-80, S-100, and LSI-11. **Corvus Systems,** 900 S Winchester Blvd, San Jose, CA 95128.

Circle 238 on Inquiry Card

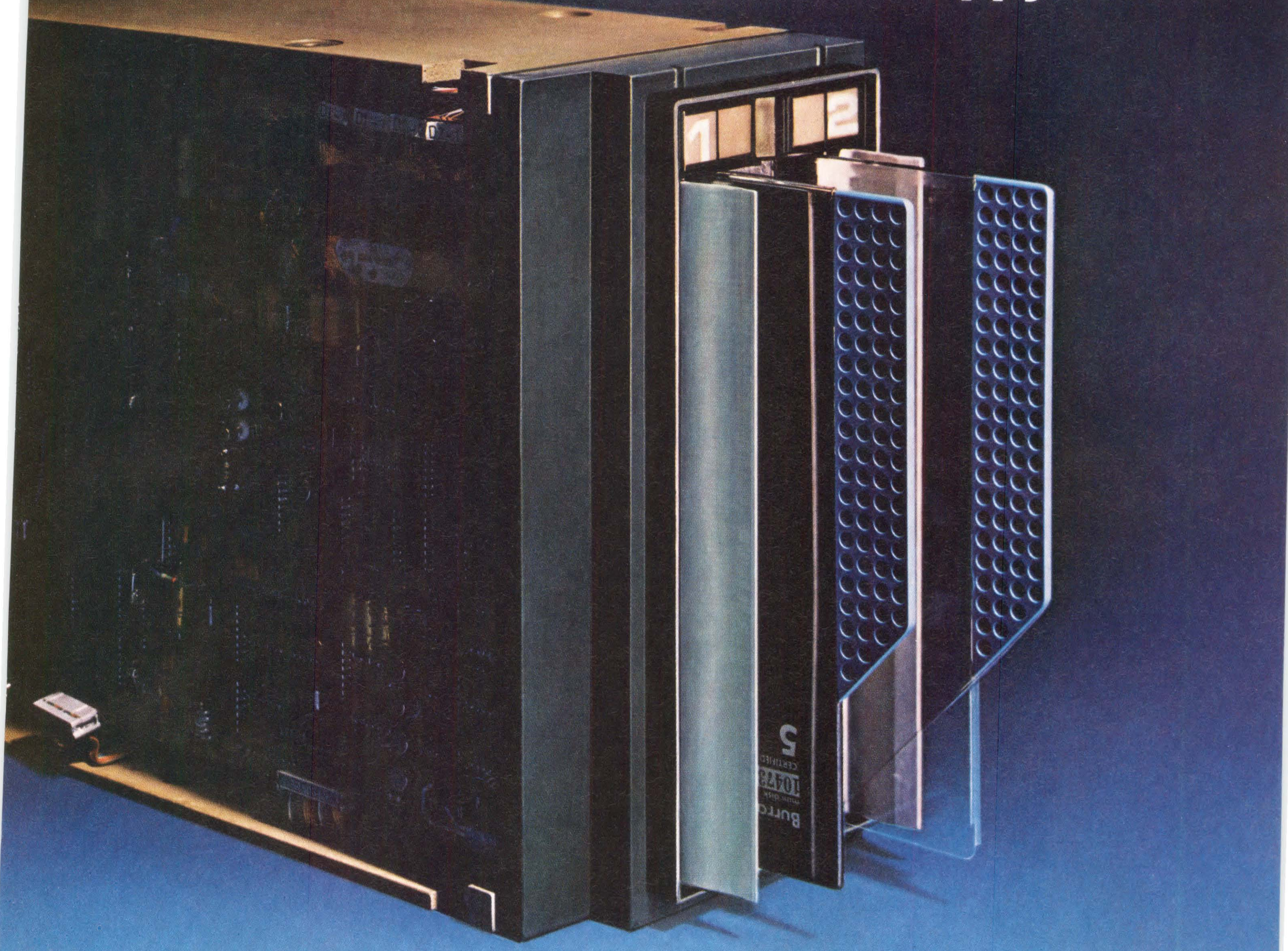
ASYNCHRONOUS TERMINAL MUX



TC-5 concentrator statistically multiplexes from 4 to 16 asynchronous terminals to communicate over a single telephone line. Features include convenient setup, complete self-test, and high compression ratios. The concentrated line uses an async or sync communications facility from 1200 to 9600 baud. Communications protocol eliminates data errors through automatic retransmission. **Comdesign, Inc,** 340 S Kellogg Ave, Goleta, CA 93017.

Circle 239 on Inquiry Card

Presenting the first 6 megabyte floppy drive!



Now get 6 megabytes of memory in about the same space as a 1 megabyte drive.

That's right. Until now, the only way you could build up to 6 megabytes of floppy disk memory into your product was to add on drive after drive.

The new Burroughs MD122 memory unit drives two 8-inch, double-sided floppies, each with a formatted capacity of 3 megabytes.

Now you can do all these applications that require more capacity, yet keep the advantages of low cost, removable media. And your system's performance will improve, too, due to the MD122's voice coil actuator with a 100 ms average access time.

We've already built in an Advanced Microprocessor Controller (AMC) which performs many of the functions normally required of the host system controller and the host CPU.

We've already interfaced it!

- CRC generation
- Error detect/correct
- Sector relocation
- File search
- Error logging & analysis
- Confidence/diagnostic tests
- Media wear monitoring and warning to host

Now you can expand your memory and save on space and cost. Call or write today for our low evaluation unit price and complete specifications.

Burroughs OEM Marketing, Burroughs Place, Detroit, MI 48232, (313) 972-8031. In Europe, High Street, Rickmansworth Hertfordshire, England, Telephone 09237-70545.

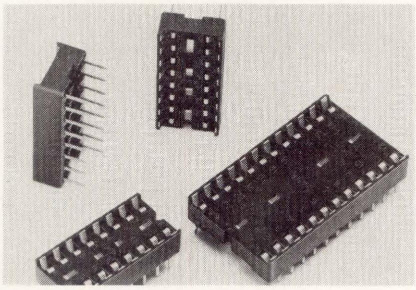
Burroughs

For General Information Circle 148

For Detailed Specifications Circle 149

PRODUCTS

SOLDER OR RETENTION TAIL DIP SOCKETS



Available with straight solder tails for clinching or retention tails for use without clinching in PC board holes from 0.033 to 0.039" (0.083 to 0.099 cm) dia, Diplomate sockets are designed for automatic machine insertion. Tapered lead-in ramps ease DIP insertion; an anti-overstress wall protects contacts from damage by oversize or bent DIP leads. Self-extinguishing, 94 V-O glass-filled polyester housings have closed bottom to prevent solder wicking and flux contamination of solder area. **AMP Inc,** Harrisburg, PA 17105.
Circle 240 on Inquiry Card

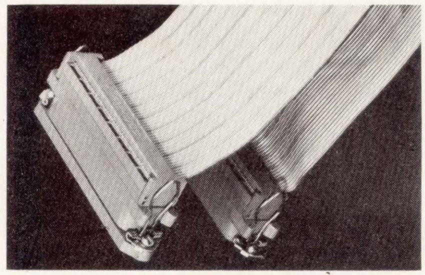
HERMETIC RESISTOR

Featuring load-life stability as tight as 0.01% typ ΔR (0.05% max) under full rated power of 0.3 W at 125 °C (0.6 W at 70 °C) for 2k h, the HS555 has a shelf life of 0.0005% max ΔR after 1 yr and 0.0001% max after 3 yr. Resistance range is 1 to 100k Ω with tolerances from ±0.0005% to ±1.0%. HS555 is a hermetically sealed version of the S555. **Vishay Resistive Systems Group of Vishay Intertechnology, Inc,** 63 Lincoln Hwy, Malvern, PA 19355.
Circle 241 on Inquiry Card

LSI-11 LINE PRINTER CONTROLLER

Hardware and software compatible with all LSI-11 and PDP-11/03 computers, LPCL11 provides a parallel interface to variety of line printers. Address selection is made by use of onboard 10-position DIP switch, giving user full control and ease of selection of address. Vector address is selected via a 6-position DIP switch providing choice of 000 to 370 octal. Unit is transparent to host diagnostics, drivers, and operating systems. **Computer Extension Systems, Inc,** 17511 El Camino Real, Houston, TX 77058.
Circle 242 on Inquiry Card

BAIL MOUNT EAR RIBBON CONNECTOR

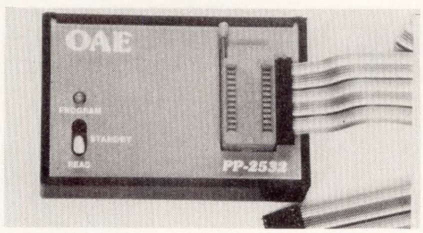


Both male and female ribbon connectors are available with bail mount or notched ears. Designed for mass termination to std 26 AWG solid or 26 and 28 AWG stranded round conductor cable for intracabinet applications, the connectors can also be mass terminated to 26 or 28 AWG stranded UL listed jacketed cable. Features include insulation displacing Tulip[R] contacts on 1.27-mm centers, and I/O mating ribbon contacts on industry std 2.16-mm centers. **T & B/Ansley Corp,** 3208 Humboldt Ave, Los Angeles, CA 90031.
Circle 243 on Inquiry Card

LCD CONNECTOR WITH CLEAR BEZEL

Zebra strips, alternating layers of conductive and nonconductive silicone rubber, provide electrical connection and gas-tight seal between connector frame and LCD. Mask frames LCD, and bezel fits over assembly, protecting the LCD. Entire unit, assembled and secured to PC board with 2 self-tapping screws, protects 1.2 x 2.0" (3.0 x 5.1-cm) LCDs against shock and vibration. **Tecknit,** 129 Dermody St, Cranford, NJ 07016.
Circle 244 on Inquiry Card

P/ROM PROGRAMMER



PP-2532 for the 4k x 8, 5-V only, TMS 2532 EPROM converts a P/ROM socket to a table top programmer using a 4' (1-m) flat ribbon cable that connects this device to any P/ROM socket via a 24-pin plug. With the P/ROM socket interface, data are sent over the 8 lower address lines to program the P/ROM. Each tabletop unit contains an internal dc to dc switching regulator and zero insertion force socket. **Oliver Advanced Engineering, Inc,** 676 W Wilson Ave, Glendale, CA 91203.
Circle 245 on Inquiry Card

SYSTEM 19 NOW PROGRAMS MORE THAN 200 DIFFERENT PROMS WITH ONLY ONE SOFTWARE SELECTABLE MODULE.

Our new System 19/UniPak lets you program most MOS and bipolar PROM'S from AMD, Fairchild, Harris, Intel, MMI, Motorola, National, Raytheon, Signetics and Texas Instruments. UniPak's software assembles the programming algorithm and selects the correct socket for 16, 18, 20, 24 and 28-pin PROMS.

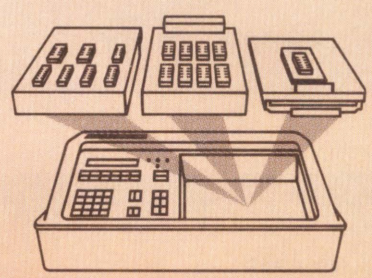
System 19/UniPak gives you design and purchasing freedom. This means you can select the best PROM for each application, and you can second-source for the best price and availability.

Semi-house approvals and easy calibration help maintain higher device yields. UniPak has earned written approval from device manufacturers. And easy calibration lets you keep performance within PROM manufacturers' specifications.

UniPak algorithms shorten programming time enhancing System 19's use as a production tool. UniPak is the first module to use a newly developed algorithm which makes it possible to program a 64K EPROM in less than half the time it takes to program a 16K EPROM using standard methods.

And the System 19/UniPak is easy to operate, with a minimum of operator training.

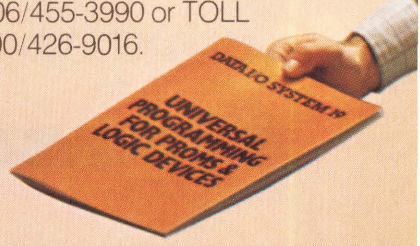
New System 19 concept is open ended to keep it state of the art. The System 19 is designed around a standard main frame and plug-in modules.



Modules available now include the UniPak, a gang programming pak for MOS devices, and a series of programming paks for logic devices and individual PROM families.

23 communication formats including six for development systems. Development systems, computers, teletypes and CRT terminals interface easily with the System 19. The System 19 accepts micro-processor instruction codes from Motorola, Intel, Tektronix, Fairchild, FutureData and other development systems without intermediary equipment.

Let us show you the future. The new Data I/O System 19/UniPak is available now. To make arrangements for a demonstration or to get your free copy of this valuable 32-page book, circle reader service number or contact Data I/O, P.O Box 308, Issaquah, WA 98027. Phone 206/455-3990 or TOLL FREE: 800/426-9016.

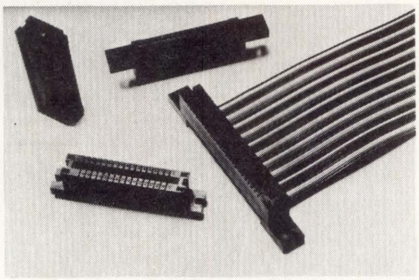


DATA I/O

CIRCLE 151 ON INQUIRY CARD

PRODUCTS

INSULATION DISPLACEMENT CONNECTORS



Capable of being recycled or repaired after mass termination, 807 series card-edge connectors reduce total applied cost of flat cable assemblies. Further labor and materials savings stem from optional availability of 2-piece connector with cover not installed, and ability to remove cover for inspection and reuse after mass termination. Device is available in 7 sizes ranging from 10 to 60 pins, 3 mounting configurations, and with optional polarizing key. **Spectra-Strip, Div of Eltra Corp,** 7100 Lampson Ave, Garden Grove, CA 92642.
Circle 246 on Inquiry Card

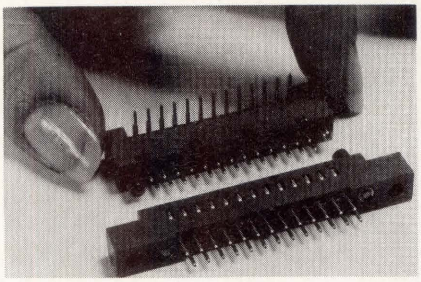
SUBMODULAR DC POWER SUPPLIES

Available off the shelf, the 12 models in the 25 series are offered with the building block concept of single, kit, or custom configurations. Outputs are 5, 12, 15, and 24 Vdc at current ranges of 2.5 to 6 A for model 25C, 5 to 12 A for 25D, and 7.5 to 18 A for 25E. Features include voltage adjustment; current limiting; remote sense; output rectifying, filtering, and regulation; and output overcurrent and short circuit protections. **Powertec, Inc,** 20550 Nordhoff St, Chatsworth, CA 91311.
Circle 247 on Inquiry Card

P/ROM PROGRAMMING BOARD SET

SuperMOS, a single-board set, offers an alternative to use of three separate Data I/O MOS programming boards. Only one card set is required to program all N-channel EPROMs, including 32k types. Onboard microprocessor allows superior wave form characteristics and built-in diagnostic capability. With the plug-to-plug compatible card set, operators can program 2704, 2708, TMS 2716, 2758, 2516, 2716, 2532, and 2732 type EPROMs. Basic operation remains unchanged. **Advant, Inc,** 650 Almanor Ave, Sunnyvale, CA 94086.
Circle 248 on Inquiry Card

MULTILAYER PCB CONNECTOR

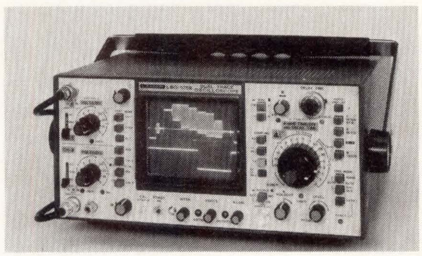


Designed for use with multilayer PC boards or flexible printed, wiring, and conforming to MIL-C-55302, connector features include repairable socket contacts replaceable from the connector engaging face; low mating force resulting from use of stamped socket contacts; and high contact reliability provided by beryllium copper contacts. Device is available in 10 through 70 contact positions and a variety of terminal types and coupling styles. **Hughes Connecting Devices,** 17150 Von Karman Ave, Irvine, CA 92714.
Circle 249 on Inquiry Card

DUAL-CHANNEL IEEE-488 BUS

Model 417-DC, a dual-channel version of the 417 interface for Data General computers consists of 2 independent 417 IEEE bus interfaces on a single board occupying one I/O slot. All functions of talker, listener, and controller modes are implemented for each channel. Simultaneous independent operation of 2 channels provides adaptive system configuration/programming, editing, and selective data transfer/merge capabilities. **RBI Systems,** PO Box 6393, Silver Spring, MD 20906.
Circle 250 on Inquiry Card

30-MHz OSCILLOSCOPE



Upgraded in bandwidth from 25 to 30 MHz, the LBO-515B oscilloscope offers a 10-turn calibrated delay time function control to more accurately measure time intervals. Sensitivity is 5 mV in both sweep and X-Y display modes. Dual channel displays can be chopped or alternated; the sum or differences of the two channels can also be displayed. Trigger controls include CH-1, CH-2, external sources, and ac code coupling. **Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11787.
Circle 251 on Inquiry Card

Break out with our breakthrough

Add a UDS 103 LP modem to your small system design

- No AC connection
- FCC certified
- Fits under the phone
- $195 (quantity one)

Add the world's only line-powered modem to your small system design. Forget about AC connections and external power supplies while accessing the whole dial-up telephone network.

Thanks to our breakthrough, the added system cost is only $195.00 (quantity one) for a fully Bell-compatible, originate only, Model 103 modem. It gives your system full duplex communications capability at any speed up to 300 bps.

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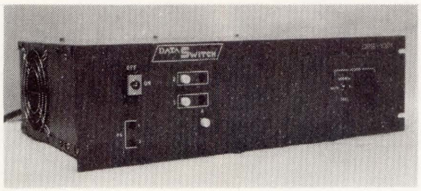
Booths 1700, 1701, 1703, 1800.

CIRCLE 153 ON INQUIRY CARD

MULTIPURPOSE COMPUTER SWITCHING SYSTEM

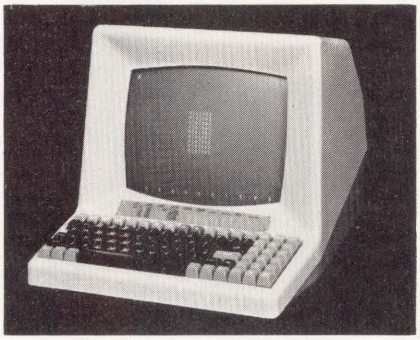
Four models of the CPS-1021 feature redundant power systems and remote control capability. Model 1 basic crossover or 2 x 1 switch allows 1 control unit to be switchable between 2 computers, while model 2 computer/peripheral switch permits 3 control units to be switchable between 2 computers. Model 3 channel extender system amplifies and redrives IBM data signals. Installation crossover system (model 4) facilitates the addition of computers for multiple system users. **Data/Switch Corp,** Landmark Sq, Norwalk, CT 06851.



Circle 252 on Inquiry Card

Z8 BASED CRT DISPLAY TERMINAL

Designed for large volume applications, miniMAS 2, which weighs approx 20 lb (9 kg), can emulate other terminals. Components are a 12" (30-cm) CRT, 7 x 9 dot matrix in a 9 x 13 field displaying all 128 ASCII codes, 24 lines of 39 or 80 char, and 16 baud rates for I/O and auxiliary ports. Keyboard contains numeric pad, cursor and editing function keys, and reset key. An external power supply is used. Software support is also included. **Micro Application Systems, Inc,** 5575 N County Rd 18, Minneapolis, MN 55442.



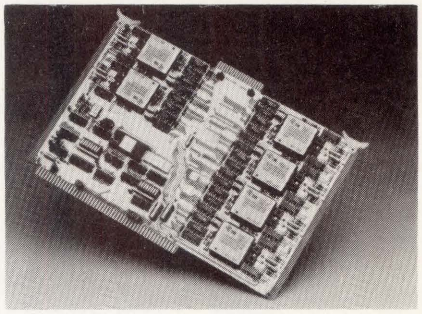
Circle 253 on Inquiry Card

PRECISION MIL OP AMP

3510VM/MIL, a low drift op amp, is laser trimmed to less than ± 2 μV/°C from -55 to 125 °C. Precision trimming also provides initial input offset (25 °C) of less than ± 120 μV. Open loop gain is 120 dB, min; CMR is 110 dB; and input bias current is less than ± 25 nA. Fast thermal response and balanced thermal design produce low change in input offset voltage as temp increases. Input impedance is 1.5 MΩ in parallel with 3 pF. Device is packaged in a TO-99 case. **Burr-Brown,** International Airport Industrial Pk, Tucson, AZ 85734.

Circle 254 on Inquiry Card

768k-BYTE BUBBLE MEMORY SYSTEMS



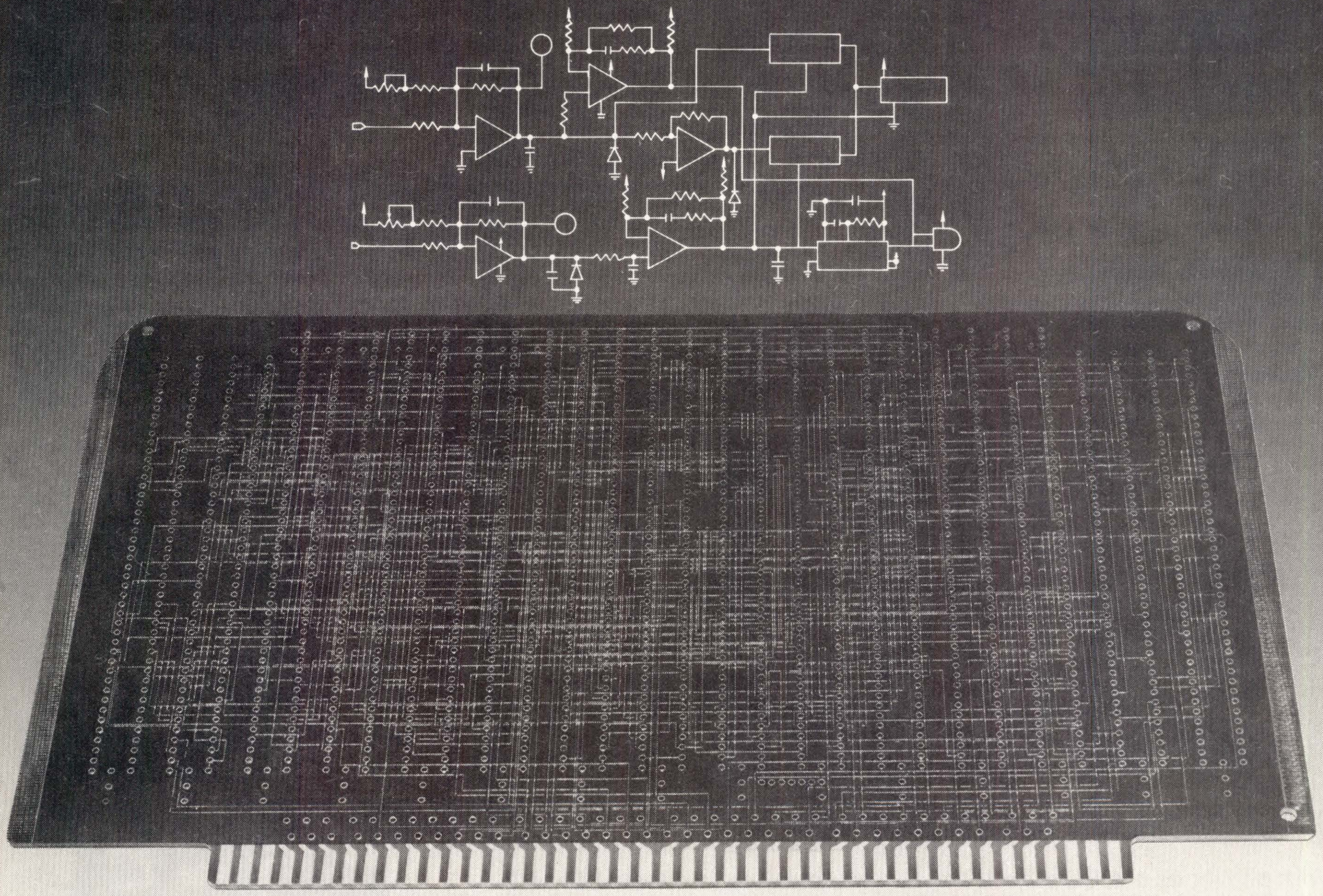
TM990/211 offers up to 768k bytes of nonvolatile storage capacity, using 1M-bit TIB 1000. An onboard custom controller, the TIB 0903 provides complete interface to the TM990 bus. Data transfers are via CRU mode. Module can do single or multipage transfers at a max data transfer rate of 85k bits/s. Board is available with 1M-, 2M-, 4M-, or 6M-bit devices to provide 128k, 256k, 512k, or 768k bytes of storage, respectively. Avg access time is 11.2 ms. **Texas Instruments, Inc,** M/S 308, Dallas, TX 75265.

Circle 255 on Inquiry Card

PANEL SEALED PUSHBUTTON SWITCHES

Snap action basic switch assemblies of types 76-911 and 78-2510 use form Z double-break switching mechanism for simultaneous control of 2 isolated circuits—1 NC and 1 NO—with 1 single-pole switch. All metal switch parts are corrosion resistant. Momentary action versions are offered. Type 76 with quick disconnect or bottom solder terminals is offered in white, red, green, blue, yellow, and black. Type 78 in black only provides bottom solder terminals. **Licon, a div of Illinois Tool Works Inc,** 6615 W Irving Park Rd, Chicago, IL 60634.

Circle 256 on Inquiry Card



PRODUCTS

VT-100 COMPATIBLE CRT TERMINAL

Key positions and LED indicators on the VISUAL 100's detached solid state keyboard are placed identical to those of a DEC VT-100. All codes and features, including double-height/double-width characters and 80/132-col screen are identical to the VT-100. Offered as standard are blink, underline, half-intensity, reverse video, and current loop interface. Other enhancements include a nonglare screen and an all-steel case. **Visual Technology Inc,** Railroad Ave, Dundee Pk, Andover, MA 01810.
Circle 257 on Inquiry Card

PRINTER INTERFACE

Intelligent Qume Commander CS-1 interface provides complete text processing and plotting capability. Features include word/char, line, and page manipulation. Printer control functions include 150 to 9600 baud, 16k buffer, host computer look-away, auto status report on command, and user selectable special char for function control. Vector plotting with complete pen absolute and relative movement commands in simple format is supported, providing 0.0069" (0.1753-mm) vertical and 0.0083" (0.2108-mm) horizontal resolution. **Data Capitol Co,** 702 Whitney St, San Leandro, CA 94577.
Circle 258 on Inquiry Card

3.6- TO 28-V LED INDICATOR LIGHTS

High brightness bi-pin 560 series lamps as replacements for incandescent indicator lights have 7 operating voltages ranging from 3.6 to 28 V. Red, yellow, or green light emitting colored units feature a wide angle diffused or narrow angle nondiffused intense light source, integral current limiting resistor for various operating points, and package design for positive seating and spacing of the light source. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 259 on Inquiry Card

13.4M-BYTE CARTRIDGE TAPE SUBSYSTEM

Interface links up to 4 DEI DC-300 high density cartridge tape drives to an RS-232-C port to increase storage capacity by up to 13.4M bytes. Supporting serial transfer rates up to 175k baud, it also provides offline copy firmware to make distribution or archival copies of a tape without host interaction. The DRS-232 subsystem consists of an interface, power supply, and optional table cabinet or 19" (48-cm) rack mount. **Alloy Engineering Co, Inc,** 85 Speen St, Framingham, MA 01701.

Circle 262 on Inquiry Card

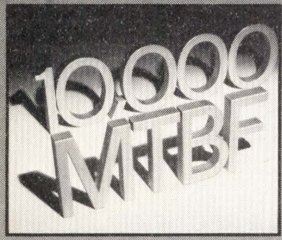
TRIPLE-OUTPUT CHASSIS-MOUNT POWER SUPPLIES

PM390 series units for data conversion applications provide dc outputs of ±12 V at 120 mA and 5 V at 500 mA (PM391), ±12 V at 180 mA and 5 V at 300 mA (PM395), ±15 V at 100 mA and 5 V at 500 mA (PM390), and ±15 V at 150 mA and 5 V at 300 mA (PM394). Line regulation is ±0.02%; load regulation is ±0.02% for ±12- and ±15-V outputs and ±0.05% on the 5-V output, which also features overvoltage protection. **Power Products, Div of Computer Products, Inc,** 1400 NW 70 St, Fort Lauderdale, FL 33309.
Circle 261 on Inquiry Card

VT-52 COMPATIBLE CRT DISPLAY TERMINAL

ASCII and APL versions of the concept 520 series, with either 1 or 4 full pages of display memory, emulate std features of the DEC VT-52, including cursor control, reverse line feed, clear functions, and alternate keypad mode. All 4 members are compatible with DEC software. Other features are windowing, programmable function keys, business graphics, multiple char sets, and multiple I/O ports. **Human Designed Systems, Inc,** 3700 Market St, Philadelphia, PA 19104.
Circle 260 on Inquiry Card

RELIABILITY. IT'S WHAT MAKES FUJITSU THE WORLD'S LARGEST MANUFACTURER OF OEM WINCHESTERS.



That's right! Fujitsu produces more Winchester technology disk drives for the OEM market than any other manufacturer in the industry. The reason for this success is the unequalled reliability of Fujitsu products.

For instance, Fujitsu's M228X Winchester drive delivers more than 10,000 MTBF power on hours of high performance. That's 40% better than the industry standard. And the M228X is fast: 6ms track-to-track (27 ms average) access time. With this kind of performance, up to 169 megabytes of unformatted storage, and Fujitsu's competitive pricing—there is no other choice! Optional head-per-track capacity of 655 kilobytes also available with this series.

80 and 50 MB cartridge drives with SMD interfacing

Fujitsu's advanced technology does not stop at Winchesters! The two front-loading cartridge drives with SMD capability shown here, have statistics only Fujitsu could guarantee. Like access times of 6ms track-to-track (30 ms average), and a reliability factor of over 6,000 poh MTBF. That's 50% better than the industry standard.

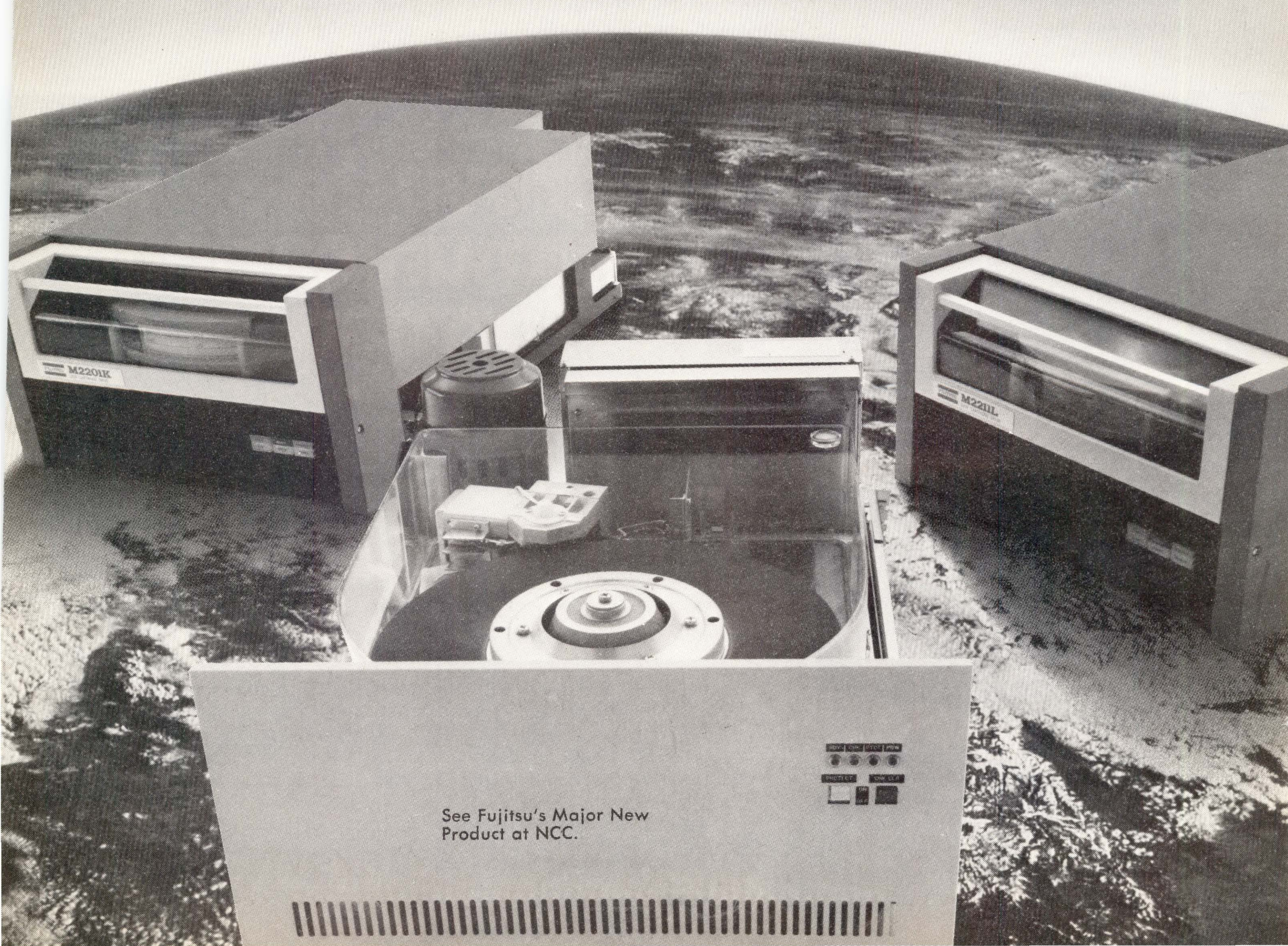
And whether you order the M2211 (80 MB) or the M2201 (50 MB) drive you can say goodbye to data staging. Plus you get a servo/track record system that assures the cartridge interchangeability you need. With features like these it's no wonder Fujitsu's got the world on a platter.

For technical information, (outside California only) phone toll-free 800-538-8175. For sales and service, or evaluation unit, contact: Fujitsu America, Inc., 2945 Oakmead Village Court, Santa Clara, CA 95051. Phone 408-985-2300, Telex 357-402, TWX 910-338-0047.

FUJITSU

The first word in reliability.
The last word in performance.

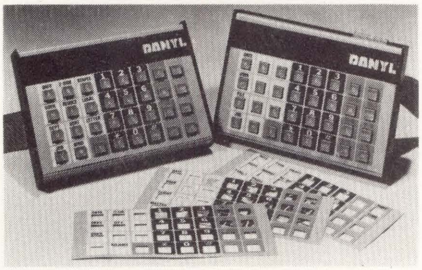
CIRCLE 157 ON INQUIRY CARD



PRODUCTS

KEYBOARD ASSEMBLY WITH OVERLAYS

Basic 32-key, matrix keypad housed in a beige and brown metal case has letters and fixed function codes for start, complete, cancel, clear entry, letter, and space engraved on the key tops. All other key titles and legends are printed on an overlay material which is available with or without adhesive backing. Each key title may contain up to 6 char of information printed to match customer specs. With no electronics, KA2 optionally has a 9-position, 7-segment, 0.3″ LED display. **DANYL Corp,** 310 Cooper Ctr, Pennsauken, NJ 08109.



Circle 263 on Inquiry Card

EXTREME ENVIRONMENT FLEXIBLE DISC

Optima series XE™ was developed for extreme environment conditions, where very low and very high temps are encountered. Full op temp range is claimed to be 10 to 71 °C; temps well outside the normal office or computer room range, but often found in military and industrial applications. The medium can be used in all flexible disc applications but will find major use with mil spec computer systems. **Verbatim Corp,** 323 Soquel Way, Sunnyvale, CA 94086.

Circle 264 on Inquiry Card

FIBER OPTIC RS-232 CABLE

For short distance applications in both point to point and loop configurations, Data Cable consists of a 25-pin D connector with integral fiber optic transmitter and receiver circuits that are attached, via strain reliefs, to each end of a 2-fiber cable. The link carries duplex asynchronous data at rates to 100k baud over spans up to 500 m. Power is supplied through the connector itself or externally via a 3-wire cable. **Optelecom, Inc,** 15940 Luanne Dr, Gaithersburg, MD 20760.

Circle 265 on Inquiry Card

PDP-11/70 DISC CONTROLLER

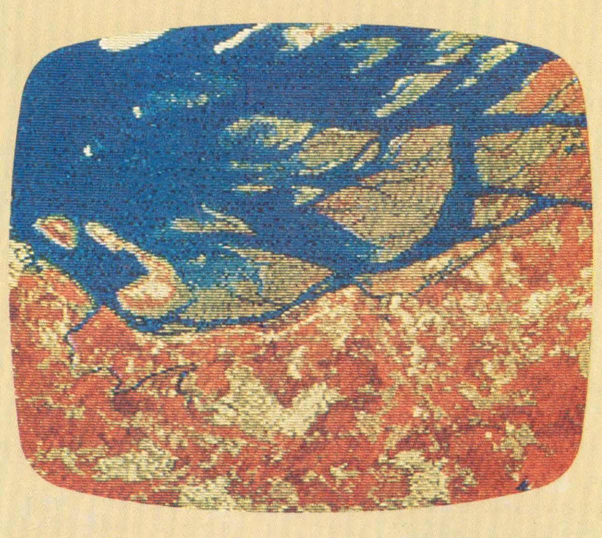
Handling disc drives as large as 600M bytes, the SC70 family consists of two versions that functionally emulate current disc subsystems offered with DEC PDP-11/70 computers. SC70/B1 emulates the RH70/RM03 subsystem and the /B2 model emulates the RH70/RP06 subsystem. Both models handle both fixed and removable media SMD class drives. Up to 4 drives may be connected per controller. Contained on 4 PC cards, the unit needs no SPC slots. **Emulex Corp,** 2001 E Deere Ave, Santa Ana, CA 92705.

Circle 266 on Inquiry Card

HIGH VOLTAGE RECTIFIER DIODE FOR CRT TERMINALS

Easily assembled and encapsulated into the high voltage inline anode cap and lead assembly, silicon diode TVR-20 has a 100-ns recovery time for CRT applications. High temp operation is assured by the diode's 100 °C leakage rating of 10 μA max. Electrical specs are peak reverse voltage of 20,000 V, average forward current of 1 mA in pulse rectifier service, and reverse recovery time of 100 ns max. **Electronic Devices, Inc,** 21 Gray Oaks Ave, Yonkers, NY 10710.

Circle 267 on Inquiry Card



LITERATURE

Winchester Fixed Drives

Describing the SA1000 and SA4000 8 and 14" (20- and 36-cm) series, brochure highlights performance, reliability, and functional features of the Winchester drives. **Shugart,** Sunnyvale, Calif.
Circle 300 on Inquiry Card

Front and Rear Release Connectors

Included in MIL-C-5015G connector catalog are receptacle mounting dimensions, contact configurations, assembly instructions, tools, and accessories. **Stanford Applied Engineering,** Santa Clara, Calif.
Circle 301 on Inquiry Card

Data Conversion Technology

Handbook and application guide outlines procedures for determining parameter tradeoffs relative to resolution, accuracy, linearity, offset, and temperature coefficient. **Analogic Corp,** Wakefield, Mass.
Circle 302 on Inquiry Card

Radio Frequency Interference

Engineering handbook on rfi suppression filters includes diagrams on interference paths, together with technical data on high performance power line filters. **Power Dynamics Inc,** South Orange, NJ.
Circle 303 on Inquiry Card

Linear and Data Acquisition Analog Chips

Specs, chip layouts, dimensions, and chip geometries are featured in data book that is available by letterhead request to **Harris Semiconductor Products Div,** PO Box 883, Melbourne, FL 32901.

Standalone Printer

Folder details features and capabilities, and supplies photos and specs for Model 7000+ dot matrix impact printer that interfaces with personal computer systems. **LRC,** Riverton, Wyo.
Circle 304 on Inquiry Card

Port Selector

Brochure furnishes specs, block diagrams, and descriptions of the Micro600 port selector that allows terminal users to contend automatically for computer ports attached to the Micro600. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 305 on Inquiry Card

Switching Power Supplies

Catalog furnishes features, specs, photos, and performance charts for MLG and LC series of switching power supplies that meet MIL specs. **Lambda Electronics, Div of Veeco Instruments, Inc,** Melville, NY.
Circle 306 on Inquiry Card

Multichannel Signal Analyzer

Specs of 6080 FFT analyzer plus keyboard operation and display formats of 6081 realtime display terminal are supplied in this catalog. **Zonic Technical Laboratories, Inc,** Cincinnati, Ohio.
Circle 307 on Inquiry Card

Midrange Minicomputers

PDP-11/44 midrange minicomputer and its commercial counterpart, the DEC DATASYSTEM 540 are introduced in separate brochures available by requests on letterhead to **Digital Equipment Corp,** 146 Main St, Maynard, MA 01754.

Data Modems

Product bulletin contains photos, system diagrams, technical notes, and a description of the diagnostic features of the T209A data modem with integral 4-channel multiplexer. **Rixon Inc,** Silver Spring, Md.
Circle 308 on Inquiry Card

Peripheral Switches

Series 3000, compatible with Digital Equipment Corp's Unibus PDP-11 family, permits multiple computers to share peripherals; features and specs for series are presented in folder. **T-Bar Inc,** Wilton, Conn.
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LITERATURE

Discrete Semiconductor Test Systems

T300 family illustrated in brochure, may be used for wafer probe, final test, incoming inspection, in-line quality assurance and marking, or device evaluation. **Teradyne, Inc**, Boston, Mass.
Circle 310 on Inquiry Card

Data Gathering Centers

Described in brochure is the 2300 series of microprocessor controlled data gathering centers that may be configured with from 16 to 254 I/O points in any mix of analog and digital. **Logicon Process Systems Div**, Fairfax, Va.
Circle 311 on Inquiry Card

Network Management System

The Roadrunner™ network management system, described in brochure, is a voice communications network switching system configurable in master, satellite, and remote systems. **Plantronics Action**, Dallas, Tex.
Circle 312 on Inquiry Card

Microprocessor Based Programmable Controllers

Brochure presents ICM series of production and processing machinery controllers for applications requiring relatively few inputs and outputs. **Divelbiss Corp**, Fredericktown, Ohio.
Circle 313 on Inquiry Card

Universal High Level Language

Described in brochure is PLMX language that communicates with all 8- or 16-bit microprocessors; the compiler currently runs under TEKDOS and CP/M operating systems. **Systems Consultants Inc**, San Diego, Calif.
Circle 314 on Inquiry Card

Custom Modular Power Supplies

Modular design of C-MOD™ supplies with ac, dc, or ac/dc inputs; multiple regulated outputs; and module to module interface using a PC backplane is described in brochure. **Lorain Products Corp**, Lorain, Ohio.
Circle 315 on Inquiry Card

Memory System Test Program

Outlined in brochure is the system environment approach to memory component testing that ensures rejection of units that experience a single soft error at any time the system is under test. **National Semiconductor**, 2900 Semiconductor Dr, MS16-250, Santa Clara, CA 95051

Electrically Conductive Coatings

Folder describes application techniques, applications, and special conductive coating materials that achieve electromagnetic compatibility by shielding against emi and rfi. **PennDixon**, Sharon Hill, Pa.
Circle 316 on Inquiry Card

Power Supply Programmers

Digital programmers that control the output of power supply by digital input signals are profiled in catalog with specs, dimensional drawings, block diagram, and tutorial on writing instructions. **Kepco Inc**, Flushing, NY.
Circle 317 on Inquiry Card

Entry Level Scientific Computer

Brochure introduces the ECLIPSE™ S/140 scientific system with discussions on hardware features, high performance options, software, peripherals, and its upward compatibility. **Data General Corp**, Westboro, Mass.
Circle 318 on Inquiry Card

Miniature Sealed Pushbutton Switches

Data sheet includes dimensional and electrical specs, operating characteristics, and materials for switches sealed by O rings between plunger and bushing and between bushing and panel. **Grayhill, Inc**, La Grange, Ill.
Circle 319 on Inquiry Card

Rocker Switch

Specs, dimensional drawing, printed circuit layout, and a listing of materials for GR-29-326 snap-action dpdt rocker switches are given in technical bulletin. **CW Industries**, Warminster, Pa.
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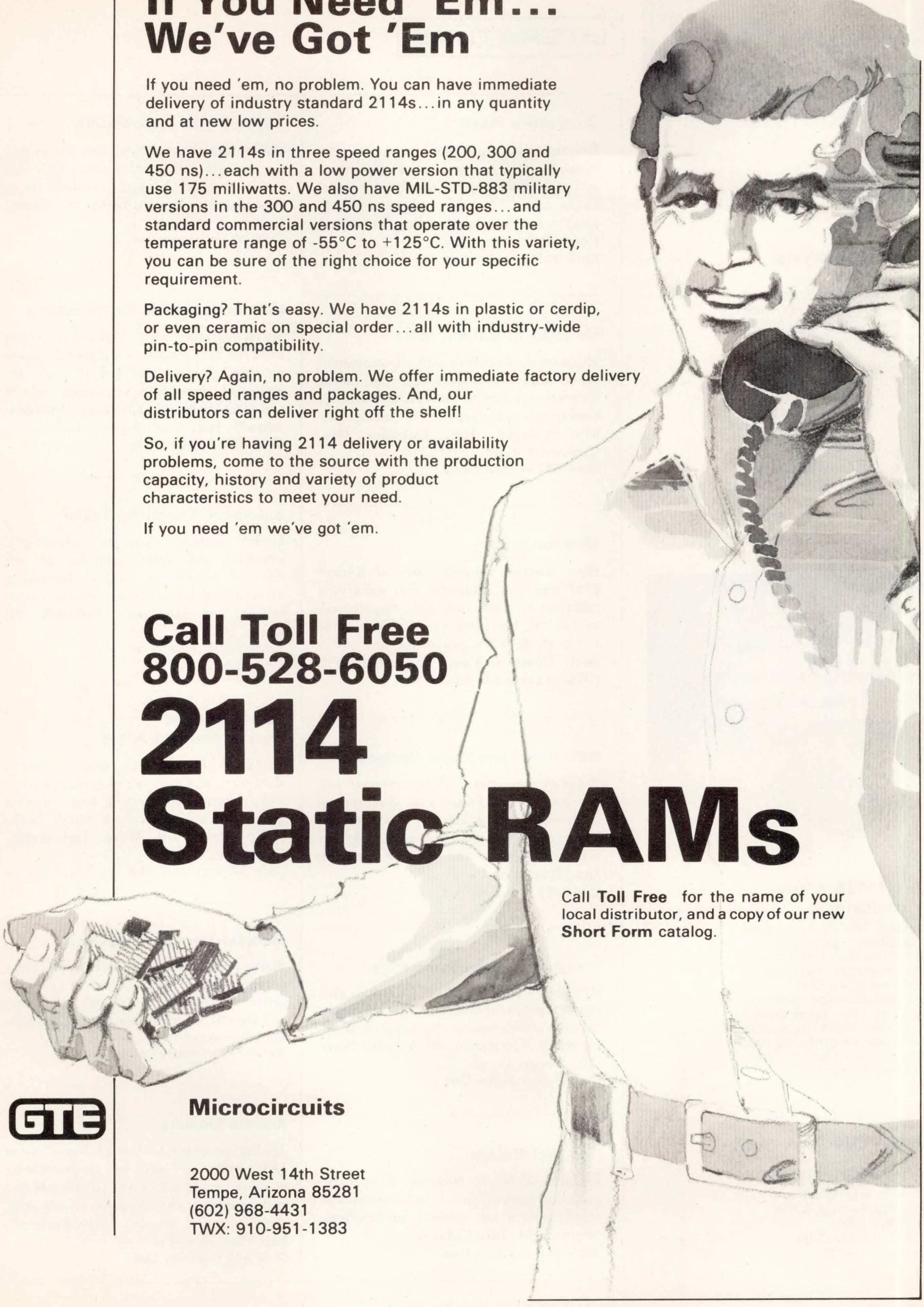

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LITERATURE

Conductive Plastics

Brochure lists applications; compares electrical, thermal, and mechanical properties; and projects savings for nonabrasive metal flakes and fibers that, when added to plastics, increase emi shielding. **Transmet Corp**, Columbus, Ohio.
Circle 321 on Inquiry Card

Modular Optical Encoders

Mechanical, electrical, and environmental specs; dimensional drawings; and timing diagrams for line of kit-type, modular optical encoders are supplied in catalog. **Litton Systems, Inc, Encoder Div**, Chatsworth, Calif.
Circle 322 on Inquiry Card

Wire Insulation

Case histories spotlight uses of Kynar[R] PVDF lead wire insulation that withstands radiation to 200M rads and temperatures to 176 °C, has good chemical resistance and high dielectric properties, and colors easily. **Pennwalt Corp**, Philadelphia, Pa.
Circle 323 on Inquiry Card

Data Communications Devices

Protocol converter, cables, terminal use monitor, asynchronous and synchronous modem eliminators, and line of test sets are among the items featured in catalog that gives descriptions and specs. **Expandor Inc**, Pittsburgh, Pa.
Circle 324 on Inquiry Card

Power Darlington Transistors

Brochure includes specs and characteristics for 6 npn families and 3 pnp families of transistors; also supplied is applications information. **RCA Solid State Div**, Somerville, NJ.
Circle 325 on Inquiry Card

Compact Motors

Features of dc, ac inductor, ac synchronous, and stepper motors; tachometers; and pump motors are outlined in brochure. **Magnafield, Inc**, Cedar Grove, NJ.
Circle 326 on Inquiry Card

2-Wire Signal Transmitters

Guide furnishes applications, specs, and dimensional drawings for series 3300 and 2300 2-wire signal transmitters. **Rochester Instrument Systems**, Rochester, NY.
Circle 327 on Inquiry Card

Uninterruptible dc Power Supply

Specs, operating modes, and features of the UPS-2708 that supplies regulated dc power for MOS memory and refresh logic are presented, along with performance charts and block diagrams, in brochure. **Stevens-Arnold, Inc**, South Boston, Mass.
Circle 328 on Inquiry Card

Automatic Continuity Tester

Folder presents features, advantages, benefits, and self-diagnostics of the CBT-128 tester for cables, harnesses, wirewrapped boards, bare printed circuit boards, and backplanes. **Sensitek**, Mt Laurel, NJ.
Circle 329 on Inquiry Card

Resistance and Heating Element Alloys

Technical booklet on copper, nickel, aluminum, and alloy wires covers physical and electrical properties and supplies gauge to millimeter conversion table. **MWS Precision Wire Industries**, Chatsworth, Calif.
Circle 330 on Inquiry Card

Modular Terminal Blocks

Photos and specs for feed-through blocks are provided in catalog that is one of a series covering terminal blocks, strips, and accessories. **Weidmuller Terminations, Inc**, Richmond, Va.
Circle 331 on Inquiry Card

Add-On Memory

Application note cites how addition of up to 128k bytes of core or semiconductor memory in one 5.25 x 19" (13.34 x 48-cm) rackmountable chassis expands minicomputer memory. **Digital Data Systems, Inc**, Plantation, Fla.
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Note: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

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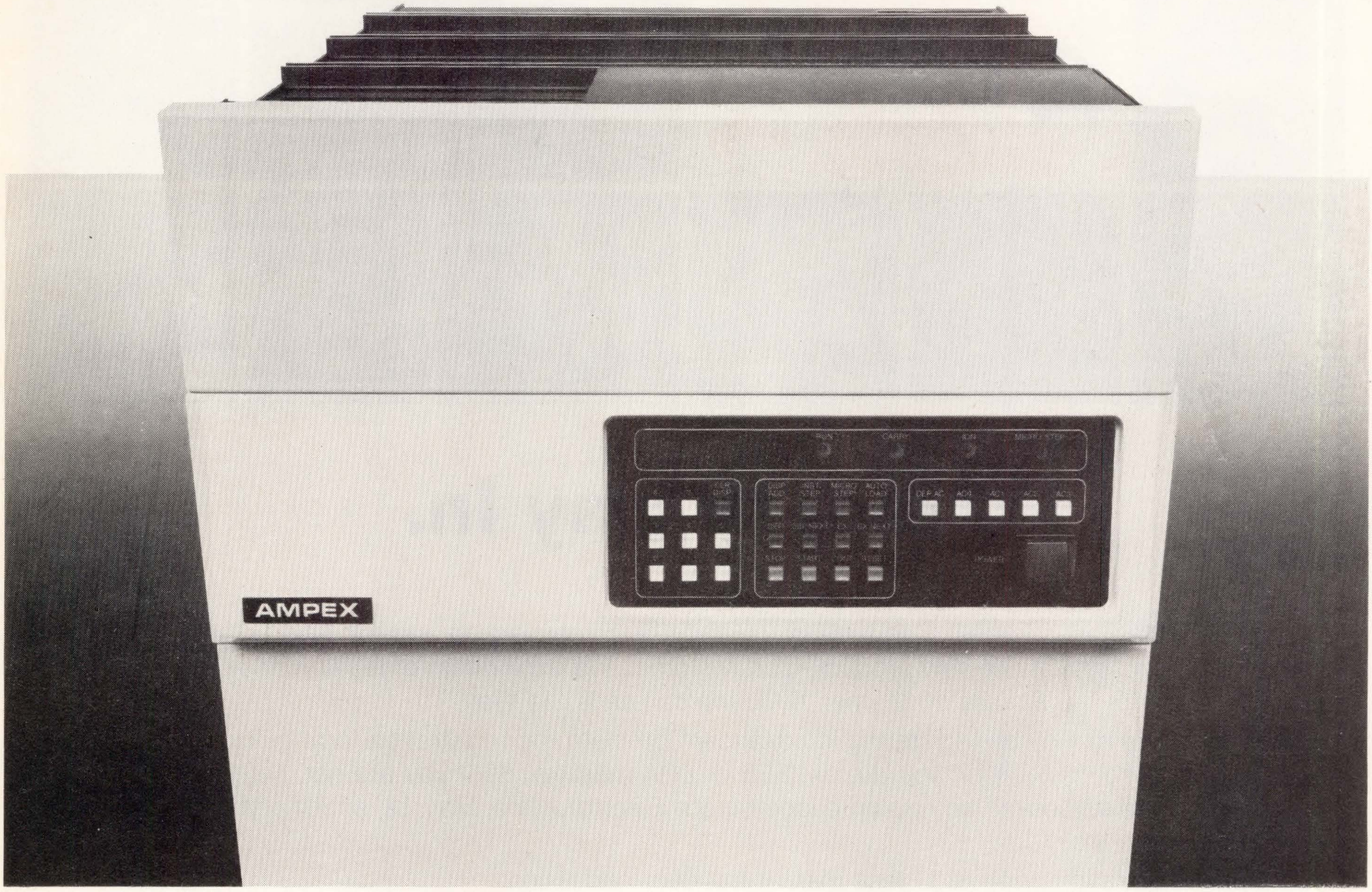

When is a mainframe not a mainframe? When it's an Ampex minicomputer.

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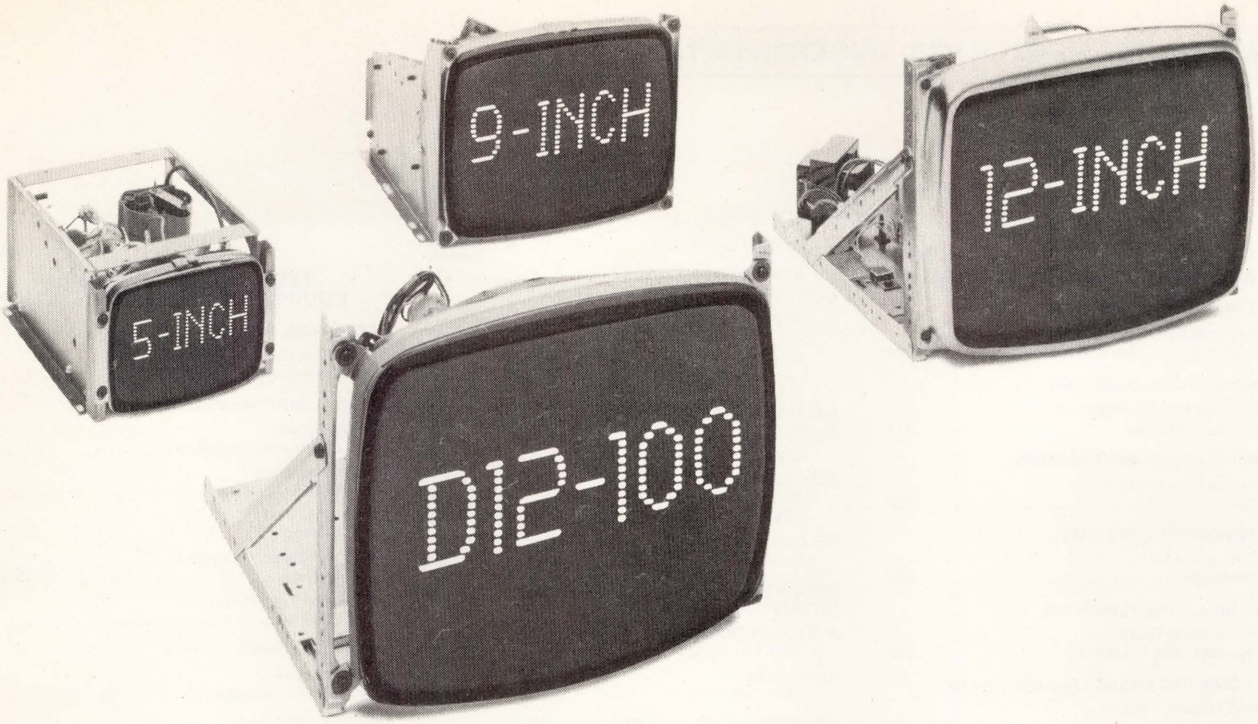

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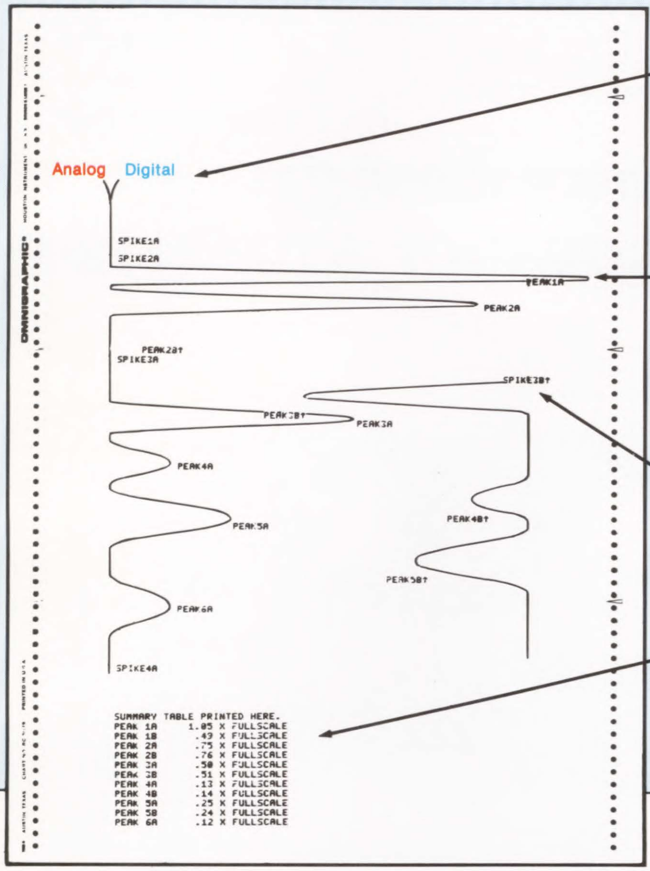

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